TLP: A Deep Learning-Based Cost Model for Tensor Program Tuning

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ABSTRACT
Tensor program tuning is a non-convex objective optimization problem, to which search-based approaches have proven to be effective. At the core of the search-based approaches lies the design of the cost model. Though deep learning-based cost models perform significantly better than other methods, they still fall short and suffer from the following problems. First, their feature extraction heavily relies on expert-level domain knowledge in hardware architectures. Even so, the extracted features are often unsatisfactory and require separate considerations for CPUs and GPUs. Second, a cost model trained on one hardware platform usually performs poorly on another, a problem we call cross-hardware unavailability.

In order to address these problems, we propose TLP and MTL-TLP. TLP is a deep learning-based cost model that facilitates tensor program tuning. Instead of extracting features from the tensor program itself, TLP extracts features from the schedule primitives. We treat schedule primitives as tensor languages. TLP is thus a Tensor Language Processing task. In this way, the task of predicting the tensor program latency through the cost model is transformed into a natural language processing (NLP) regression task. MTL-TLP combines Multi-Task Learning and TLP to cope with the cross-platform unavailability problem.

We incorporate these techniques into the Ansor framework and conduct detailed experiments. Results show that TLP can speed up the average search time by 9.1× and 3.0× on CPU and GPU workloads, respectively, compared to the state-of-the-art implementation. MTL-TLP can achieve a speed-up of 4.7× and 2.9× on CPU and GPU workloads, respectively, using only 7% of the target hardware data. To the best of our knowledge, TLP is the first tensor program cost model to extract features directly from schedule primitives, and MTL-TLP is the first open-sourced work that effectively addresses the cross-platform unavailability problem. The code is available at https://github.com/zhaiyi000/tlp.

CCS CONCEPTS
• Computing methodologies → Machine learning; • Software and its engineering → Source code generation.

KEYWORDS
tensor program, cost model, compiler optimization, deep Learning

1 INTRODUCTION
The main challenge of tensor program tuning is that measuring tensor program latency is excessively time-consuming. The time-consuming measurement of the tensor program latency is due to
the following three reasons. First, the measurement pipeline consists of multiple steps, including compilation, loading, and execution. Two network transfers are required if the remote procedure call method is used. The compilation is particularly time-consuming, requiring lowering to multiple intermediate representations (IRs) and performing extensive optimizations on these IRs. Second, to guarantee accuracy, it is often necessary to repeat the measurement multiple times. If the measurement is performed on CPUs, the cache needs to be flushed between two consecutive measurements. Finally, the measurement task often monopolizes the computing resources to avoid noises, preventing the potential parallel execution mode. In our experience, measuring the latency of a tensor program for a fusion operator often takes hundreds of milliseconds (on Intel i7-10510U CPU and NVIDIA GeForce 2080Ti).

The time-consuming problem makes it impossible to place all the generated tensor programs on the target hardware platform for latency measurement during the tuning process. To address this issue, many deep learning compilers [6, 10, 31] resort to the cost model [5, 11, 21, 38, 39]—using the predicted latency from the cost model as the criterion. Dozens of candidates are selected to be measured on target hardware from tens of thousands of tensor programs. Recent works [5, 30, 39] have demonstrated that deep learning-based cost models perform far better than other methods. However, existing deep learning-based cost models rely heavily on complex feature engineering. Ansor [38] manually extracts 164 features from five aspects for the innermost assignment statement, including computation, memory access, and arithmetic strength. The TIRAMISU cost model [5] manually extracts 2534 features and the abstract syntax tree (AST) structure; it takes the AST structure as a computational stream to forward propagate input features. Complex feature engineering can be problematic. First of all, only domain experts well-versed in hardware architecture can be qualified for the job. Even so, the hand-picked cost models still fall short in many cases, largely affected by the limitation of prior knowledge. More importantly, the features extracted on CPUs and GPUs are different; even when extracted on CPUs, the features cannot achieve stable performance simultaneously on different architecture CPUs such as Intel, ARM, and AMD CPUs. In order to take into consideration the different hardware architectures, more engineering endeavors are required, making feature extraction a laborious and cumbersome process.

This time-consuming problem also hinders us from collecting large-scale tensor program datasets on every possible hardware platform. Furthermore, the performance of a cost model trained offline on one hardware platform drops dramatically on another, which we call the problem of offline cost model unavailability across hardware. A tensor program has different execution times on different hardware, sometimes with a considerable variance due to domain gaps in hardware architecture and hardware performance. Such discrepancy makes it hard for a model to apply simultaneously on multiple hardware platforms. To address this issue, TenSet [39] and Moses [37] use transfer learning and model distillation, respectively.

In response to these problems, we present TLP and MTL-TLP. TLP is a deep learning-based cost model for tensor program tuning. We do not extract features from the tensor program source code for two reasons. First, the source code of the tensor program is tree-structured data with nested loops, and the AST information in it is difficult to extract and utilize. The second is that there are too many unrelated character tokens in the source code, resulting in sparse features. We extract features from schedule primitives. We treat schedule primitives as tensor language and turn the task of predicting tensor program latency into an NLP regression task.

For the problem of the offline cost model being unavailable across hardware, we use multi-task learning techniques to solve it. Multi-task learning has led to successes in many deep learning applications, from language translation [17, 26] and text classification [24] to scene analysis [22] and autonomous driving [12, 13]. Similar to the idea that the tensor compiler uses high-level graph IR and low-level tensor IR to abstract hardware-independent and hardware-dependent features, we use shared and non-shared parameters to fit hardware-independent and hardware-dependent features. One tensor program has different latencies (labels) on different hardware platforms. We set up multiple tasks, each corresponding to a hardware platform.

We integrate the above techniques into Ansor [38], a state-of-the-art search framework in the TVM compiler. We conduct comprehensive experiments and show that TLP and MTL-TLP comprehensively outperform the state-of-the-art implementation on various CPU and GPU workloads. Compared with Ansor, reaching the performance of Ansor tuning 2,000 times, TLP can speed up the average search time by 16.7× and 16.0× on CPU and GPU workloads. MTL-TLP can achieve a speed-up of 10.0× and 15.8× on CPU and GPU workloads, respectively. In many experiments, there is still a big gap between the performance of Ansor tuning 2000 times and the performance of TLP/MTL-TLP tuning the minimum times. The minimum times refers to the total times of tuning one round for each subgraph of the workload only. If Ansor is given more tuning time budgets, this speed-up can be much larger. Compared with TenSet, TLP can speed up the average search time by 9.1× and 3.0× on CPU and GPU workloads, reaching the performance of TenSet MLP tuning 2,000 times. MTL-TLP can speed up the search time by 4.7× and 2.9× on CPU and GPU workloads, respectively. Among them, MTL-TLP only uses 7% of the target hardware platform data.

It is worth noting that TLP and MTL-TLP are not specifically designed for Ansor. TLP and MTL-TLP apply to all automatic search frameworks that lower high-level graph IR into low-level tensor IR via schedule primitives.

In summary, this paper makes the following contributions:

- A simple yet efficient and general feature extraction mechanism for tensor programs;
- A multi-task learning method to address offline cost model unavailability across hardware platforms;
- An implementation and comprehensive evaluation of the TLP and MTL-TLP demonstrate that the above techniques outperform state-of-the-art implementation on various deep learning models and hardware platforms.

2 BACKGROUND

Search-based compilers. Figure 1 shows the pipeline of common deep learning compilers. These compilers accept deep learning
workloads as input and output executables for specific hardware platforms. A deep learning workload is essentially a computational graph written in various high-level programming languages. After several computational graph optimizations, some partitioning algorithms divide the long computational graph into computational subgraphs. Each subgraph has its own search space, determined by the input/output tensor shapes, data types, data layouts, and the target hardware platform. The search space is usually in the order of millions on CPUs and billions on GPUs. Guided by genetic algorithms (GA), Model Carlo tree search (MCTS), simulated annealing, etc., the compiler applies various combinations of schedule primitives to each subgraph. In the process, tens of thousands of tensor programs are generated, and the compiler uses a cost model to filter out candidates with the best possible performance. Then put these candidates on the target hardware to measure to find the highest performing tensor program. These high-performance tensor programs are finally delegated to specific accelerated backends or well-developed LLVM/CUDA to generate the final executable. Figure 2 takes a computational subgraph as an example to expand the red dashed box in Figure 1. The three tensor programs are computationally equivalent, only with different latencies.

TenSet. TenSet [39] proposes a large-scale tensor program dataset and builds a multilayer perceptron (MLP) tensor program cost model pre-trained with the dataset. Later, we use the TenSet dataset and TenSet MLP to represent its dataset and cost model, respectively. The TenSet dataset was collected on 6 hardware platforms, including Intel CPUs, AMD CPUs, ARM CPUs, and NVIDIA GPUs. On each hardware platform, 2,308 subgraphs divided from 120 typical deep learning workloads such as ResNet, MobileNet, and BERT are collected, a total of 2,308 × 6 = 13,848 subgraphs on the 6 hardware platforms. For each subgraph, at most 4,000 tensor programs are generated by the automatic search framework Ansor integrated in TVM. In total, this dataset includes approximately 51.57 million tensor programs and their latency. Each hardware platform has approximately 8.59 million data. TenSet is a continuation of Ansor. Compared to Ansor, the TenSet MLP can speed up the search time by up to 10×. We use Ansor and the TenSet MLP as the baselines for TLP and MTL-TLP.

We extensively analyze the TenSet dataset and use the dataset to train and evaluate TLP and MTL-TLP. At the same time, we also spent more than 50 days collecting a TenSet CPU dataset on an Intel i7-10510U CPU, which contains approximately 8.65 million data. In the following, we call this dataset the TenSet-TLP dataset. Natural language processing. As a branch of artificial intelligence technology, natural language processing (NLP) uses deep learning to process and interpret text data. It has achieved great success in sentiment analysis, chatbots, machine translation, and more. The processing objects of an NLP task are usually sentences, ordered sequences composed of words. For many NLP tasks, they first project each word of sentences to a corresponding number called a token, then convert each token into a high-dimensional vector (denoted as embedding vector), and this convert operation is usually called embedding. A suitable embedding method can make certain distances between synonyms, such as Euclidean distance and cosine distance, short.

3 SYSTEM OVERVIEW

Figure 3 shows the process of generating tensor programs from computational subgraphs by an automatic search framework (abbreviated as auto-tuner) integrated with TLP. The black box on the right is the pipeline of TLP. The figure depicts the two states of TLP training and inference. When training, the auto-tuner generates several schedule primitive sequences according to the received computation subgraph. The auto-tuner then invokes the code generator to generate tensor programs in combination with the computational subgraph and the schedule primitive sequence and measures the latency of these tensor programs on the target hardware. TLP takes the schedule primitive sequence as input. After preprocessing, feature extraction, and post-processing, the TLP cost model forwardly propagates the finally extracted features and normalizes the latency of the corresponding tensor program as a label to calculate the loss. Finally, the loss is back-propagated to update the weights of the cost model. When inference, after generating the schedule primitive sequences, the auto-tuner obtains the prediction score through the cost model and screens out the top-k potential candidates (yellow blocks in the figure) according to the prediction score. The auto-tuner finally generates tensor programs for these candidates and measures their latency on the target hardware.

In the pipeline of TLP, the concrete primitive refers to the schedule primitive in an automatic search framework. The abstract primitive refers to the primitive conforming to the TLP feature extractor’s input specification after preprocessing. We describe the preprocessor, extractor, and postprocessor in detail in Section 4.

4 TLP

Feature extraction is the core of building a cost model. It determines the upper bound of the performance that the cost model can achieve. Ansor manually extracts 164 features from five aspects for the innermost assignment statement, including computation, memory access, and arithmetic strength. TenSet MLP follows Ansor’s feature extraction and adds 10 high-level computational graph IR features. The TIRAMISU cost model is also extracting features from the innermost assignment statement. It extracts 2534 features, but most are zero, so its features are sparse. Unlike Ansor, the TIRAMISU cost model extracts the AST structure as a computational stream to forward propagate input features. However, in
Figure 2: Subgraph, a fused dense + ReLU activation, applies combinations of different schedule primitives to generate tensor programs. The mathematical expression, DAG, and naive tensor program contained in the computational subgraph above are logically equivalent but in different forms. Schedule primitives are written in pseudocode. The schedule primitives in the red long dashed box are the feature extraction objects of TLP, and the tensor programs in the blue short dashed box are the feature extraction objects of Ansor [38], TIRAMISU cost model [5], etc.

Figure 3: The process of generating tensor programs from computational subgraphs by an automatic search framework integrated with TLP. The black box on the right is the pipeline of TLP. Tensor programs and latency (label) blocks with dark green on the left and yellow on the right are seen as dark green during training and yellow during inference. When training, the dashed arrows, dashed boxes, and “Inference Only” arrows in the figure are invalid. When inference, the “Train Only” arrows in the figure are invalid.

our opinion, treating the AST structure as a computational stream is an impracticable solution. The AST of each tensor program is different, so that the cost model can only forward propagate one by one without parallelism. The TIRAMISU cost model can only run on CPUs. Other pitfalls of these methods have been discussed in previous chapters.

4.1 Feature Extraction of TLP

To the best of our knowledge, TLP is the first tensor program cost model to extract features directly from schedule primitives. It is challenging to efficiently extract features from schedule primitives and retain all valuable information significantly. There are three methods here. Method 1: Treat the schedule primitive sequence as character text and then use NLP tasks to do text processing. Method 2: Treat each schedule primitive as an NLP word, so a complete schedule primitive sequence is an NLP sentence. Then, convert each word into a token. Method 3, adopted by TLP, regards schedule primitive as a combination of three basic elements, i.e., primitive type, numeric parameters, and character parameters. Extract features for the three elements separately and then concatenate the extracted features together. This paper does not discuss the first method, for this simple and crude end-to-end method is challenging to achieve good performance. We think the second method misses some helpful information on the table. For example, primitives of the same type but different parameters will be encoded into two tokens without any relationship. Only the embedding algorithm and deep learning network can mine the synonymous relationship between them. Method 3 powerfully preserves this synonym relationship. The detailed description is as follows.

TLP feature extraction first preprocesses the input schedule primitive sequence. For each primitive in the sequence, TLP feature extraction only retains three basic elements: primitive type, numeric parameters, and character parameters. Extraneous characters will be stripped. In fact, these three elements basically contain
all the semantic information in the schedule primitive. The prepro-
cessing algorithm implementation is related to the specific au-
tomatic search framework. In most frameworks, this preprocessing
algorithm is reversible, i.e., the schedule primitive sequence can
be recovered from these three basic elements since each primitive
has its semantics and input specification. Figure 4a depicts an abstract
representation of schedule primitives. A schedule primitive sequence
(PrimitiveSequence) consists of several schedule primitives (Prim-
itive). Each primitive starts with the primitive type (PrimitiveType),
followed by several numeric parameters (Number) and character
parameters (NameParam). The primitive type is determined by the
specific automatic search framework. Figure 4b is an implementa-
tion of the extractor for TLP feature extraction. For primitive types,
convert it to a one-hot vector. The one-hot vector is determined
by the specific automatic search framework. For numeric param-
eters, leave their value unchanged. For character parameters, con-
vert them into tokens, the same way NLP tasks deal with words.
We map different character parameters to different tokens. Finally,
all the features are concatenated according to the element’s origi-
nal position. After that, the extracted features are post-processed
by methods such as cropping, padding, and normalization.

We take Figure 5 as an example to illustrate the process of TLP
feature extraction. The tensor program 3 and schedule primitive 3
in Figure 5 are extracted from Figure 2. First of all, it is clear that
the task of TLP is to estimate the latency of the tensor program, that is,
to estimate the latency of tensor program 3 in Figure 5. We regard
tensor program 3 and schedule primitive 3 as equivalents, and the
theoretical basis will be analyzed later. Figure 5 shows an exam-
ple of TLP feature extraction from top to bottom, i.e., the Schedule
primitives, the Extracted Features, and the Extracted Features Fi-
nal. Figure 5 has no post-processing process.

We can think of a primitive as an NLP word and the encoded re-
sult as the embedding vector of the NLP task after going through
the embedding layer. The TLP feature extraction is a word embed-
dding algorithm, which significantly preserves the synonym rela-
tionship. Since the encoding results of two primitives of the same
type but different parameters have many of the same values, the
Euclidean distance between the two primitives after normalization
is relatively short. In addition, TLP directly extracts features from
schedule primitives, eliminating the need to generate tensor pro-
grams and reducing tuning time.

4.2 TLP Feature Extraction on TenSet dataset

Terminology. We define some terminologies used in the rest of
this paper. Sequence length: the length of a schedule primitive se-
quence. Embedding size: the number of features extracted from
a schedule primitive. Feature size: the number of all features ex-
tracted from a schedule primitive sequence for a tensor program,
i.e., sequence length × embedding size.

Let us take a look at the TLP feature extraction on the TenSet
dataset to gain an intuitive understanding. TenSet uses the auto-

Table 1: The maximum embedding sizes of each schedule
primitive in the TenSet CPU dataset. “RE”, “FU”, etc. in the
table are the abbreviations of schedule primitives, which re-
fer to primitives such as reorder and fuse, respectively.
matic search framework Ansor to dump the tensor programs. Ansor uses 11 types of schedule primitives in CPUs and GPUs, respectively, so the types of all schedule primitives are replaced by an 11-dimensional one-hot vector. According to our statistics, in the TenSet CPU dataset, the schedule primitive sequence of tensor programs contains up to 54 primitives, each primitive type plus its parameters up to 40 (after the type is changed to an 11-bit one-hot vector). Figure 6 shows the distribution of sequence lengths of tensor programs in the TenSet CPU dataset. Of these, at most 1,807,960 tensor programs have schedule primitive sequences of the same length 21. The embedding size for a primitive is indeterminate. For example, a split primitive can split a loop variable to 3 or 4 loop variables. Table 1 shows the maximum embedding sizes of each schedule primitive in the TenSet CPU dataset. These data suggest that even limiting the feature size of a tensor program from $54 \times 40 = 2,160$ to $25 \times 22 = 550$ would not hurt the vast majority of features. Subsequent analysis and experiment also prove this. The statistics of the TenSet GPU dataset are similar and will not be repeated here.

4.3 Feasibility Analysis of TLP Feature Extraction

Are schedule primitive sequences definitely different for different tensor programs? The answer to this is no. Nevertheless, we think the probability of different tensor programs having the same schedule primitive sequence is low. The same computational subgraph combined with the same schedule primitive sequence must generate the same tensor program. For different computational subgraphs, either their computational flow is different, or their computational parameters are different. We think that a high-performance schedule primitive sequence contains most or even all computational parameters of a computational subgraph, and the schedule primitive sequence is tailored according to the computational flow of the computational subgraph. This results in a low collision probability of different computation subgraphs but the same schedule primitive sequence. Taking a step back, even if this collision probability rises, the feature extraction scheme of TLP is still available. The optimal value of the labels of multiple tensor programs corresponding to a schedule primitive sequence can be used as the label of the schedule primitive sequence. The disadvantage of this approach is that it may cause the cost model to misjudge a low-performance tensor program as a high-performance tensor program, resulting in a longer tuning time. Nevertheless, it guarantees that a high-performance schedule primitive sequence will not be missed.

We analyze the TenSet CPU database and find that there are 8.56 million different schedule primitive sequences in a total of 8.65 million tensor programs. The repetition rate is only 1.0430%. Even if the features are limited to $25 \times 22$, there are 8.53 million differences out of 8.56 million tensor programs, with a repetition rate of 1.4034%. Therefore, we can approximately think that a schedule primitive sequence uniquely characterizes a tensor program. That is, we consider a schedule primitive sequence equivalent to a tensor program.

The advantages of schedule primitive sequences are apparent. First, as mentioned above, in the TenSet CPU dataset, a tensor program can be characterized almost entirely by 550 features. These features are dense and preserve all information considerably. Second, the schedule primitive sequence is a regular sequence that can take advantage of some existing NLP techniques. Third, there are very few kinds of schedule primitives, such as only 14 (including for CPUs and GPUs) in Ansor, and most of them are common to both CPUs and GPUs. Finally, For schedule primitives, we do not need complex feature engineering. We just record the type and parameters of schedule primitives. It is possible to avoid operating on complex nested loops in the AST.

As such, the schedule primitive sequence and the tensor program have an almost one-to-one correspondence, containing the same amount of semantic information. The source code of the tensor program is a nested loop tree structure, and the schedule primitive sequence is a regular sequence structure. From the perspective of language, the structure of a schedule primitive sequence is the same as that of natural language, both with sequential structures. We call schedule primitives the tensor language. Thus, TLP is a Tensor Language Processing task that transforms the task of predicting tensor program latency with a cost model into an NLP regression task.

4.4 Model Architecture

Figure 7 is the model architecture of TLP. The parameters on the left are the layer’s input shape and output shape, where $N$ refers to the batch size, $L$ refers to the sequence length, and $E_l$ and $E_h$ refer to the embedding sizes. We call the red dashed box backbone and the blue dashed box head. These will be used in the multi-task learning chapter.
capture contextual features. Then two residual blocks follow. Finally, multiple linear layers and a sum operation are used to obtain a prediction score. The target label is the normalized latency. The formula is as follows: \( \text{label} = \text{min}_i \text{latency} / \text{latency} \), where \( \text{min}_i \text{latency} \) refers to the minimum value among all tensor programs of a subgraph. In the TenSet dataset, the number of tensor programs for a subgraph varies from dozens to 4,000. The value range of the label is \((0, 1]\). We use the Mean Square Error (MSE) loss function or the rank loss function to calculate the loss.

5 MTL-TLP

Table 2 shows the development of tensor program cost models. Early on, researchers directly used empirical formulas to evaluate the performance of tensor programs. For example, Halide16 used the data reuse rate and floating-point computation amount to evaluate the pros and cons of different loop-blocking and stage-folding strategies. Then, researchers began using simple deep learning models such as MLP, machine learning models such as XGBoost, reinforcement learning models, etc. These models are characterized by simple structures and low computational costs. In recent years, researchers have begun experimenting with complex deep learning models, such as TIRAMISU using the dynamic computational flow LSTM model and the work of Benoit Steiner et al. using the complex bilateral LSTM model. The law of this evolution is that the amount of data required has grown significantly simultaneously as performance has grown significantly. The online cost model only uses the measurement data generated during the tuning process and does not use any offline datasets. Offline cost models rely on massive offline datasets. The performance of the offline cost model is highly correlated with the size of the dataset.

### 5.1 Cross-Hardware Unavailability

The data collected offline are invalid across hardware caused by domain gaps in hardware architecture and hardware performance. This leads to a significant decrease in the performance of offline-trained cost models across hardware platforms. The empirical formula cost model and the online learning cost model do not suffer from this problem because they do not use offline datasets.

This presents a challenge: how to use a small amount of target hardware data to train a cost model with high performance. The first thing that comes to mind is that when using a small amount of labeled data to obtain a high-performance model is the self-supervised learning method such as BERT [16, 19] and GPT [8, 27, 28]. However, it is worth noting that BERT generally uses 6-12 transformers layers, and the input data dimension is 512x768, etc. Nevertheless, our feature size is much smaller than that, not an order of magnitude with BERT’s number of weights. For example, as mentioned earlier, the extracted features in TenSet are only 25x22. Such a large number of weights not only easily overfits the model but also severely slows down tuning, which is unacceptable during compilation. Another way to obtain a high-performance model with a small amount of data is transfer learning. There are many types of transfer learning, such as fine-tuning, training a local model to predict the gap between two domains, multi-task learning.

We think that multi-task learning techniques are most suitable for solving the problem of offline models being unavailable across hardware, mainly for the following three reasons:

- The cross-hardware unavailability problem fits the scope of multi-task learning nicely, mitigating model performance degradation caused by domain gaps.
- Multi-task learning and the tensor compiler’s multi-layer IRs share common design philosophy. The tensor compiler uses graph IR and tensor IR to abstract the hardware-independent and hardware-dependent features, respectively. Multi-task learning is a nice fit here: it can use shared parameters to fit hardware-independent features and non-shared parameters to fit hardware-dependent features.
- Our validation results also demonstrate that multi-task learning performs best among fine-tuning, multi-task learning, training a local model, and self-supervised learning. We will present these comparative data in the experimental section.

### 5.2 MTL-TLP

The model structure of MTL-TLP is similar to that of TLP. The difference is that MTL-TLP sets up multiple heads, that is, multiple tasks, and each task corresponds to a hardware platform, as shown in Figure 8. If a labeled data of TLP is represented as a tuple such as \((\text{input features}, \text{label})\), then the corresponding tuple of MTL-TLP is \((\text{input features}, \{\text{label}_1, \text{label}_2, \ldots, \text{label}_n\})\). We set task 1 as the task of the target platform. When the data has no label on the target platform, the tuple is \((\text{input features}, \{\text{None}, \text{label}_2, \ldots, \text{label}_n\})\),
and this target task will be ignored when calculating the loss, and the weights of this head will not be updated during whole backpropagation. The loss function is designed as follows:

$$loss = \sum_{i=1}^{n} loss\_fun_i(\text{pred}_i, \text{label}_i), \text{ where } \text{label}_i \text{ is not None.}$$

where $loss\_fun_i$ is the loss function of each task (usually the same), such as the MSE loss function, rank loss function, etc.

The tensor program is not universal between CPUs and GPUs, so we do not discuss multi-task learning across them.

5.3 Feasibility Analysis of MTL-TLP

MTL-TLP plays a big role mainly due to the following points:

- MTL effectively increases the sample size that we are using for training our model. Although there is only a small amount of labeled data on the target platform, there is indeed a large amount of data on other platforms. The target platform cost model can be trained using data from other platforms as auxiliary tasks.
- In single-task learning, back-propagation of gradients tends to get stuck in local minima. In multi-task learning, the local minima of different tasks are in different positions. The interaction of different tasks can help the hidden layer escape from the local minima.
- MTL acts as a regularizer by introducing an inductive bias. Multiple tasks share weights in shallow layers, which may weaken the network's ability, reduce network overfitting, and improve generalization.
- MTL-TLP can use shared parameters to fit hardware-independent features and non-shared parameters to fit hardware-dependent features.

6 EVALUATION

There are two types of evaluation metrics to evaluate and compare the performance of cost models: dataset-based and search-based. The dataset-based metrics evaluate the model’s accuracy on a static dataset. Search-based metrics evaluate the end-to-end search efficiency or search quality after integrating the cost models into the search algorithms.

6.1 TLP with Dataset-Based Metrics

We use data from the TenSet and TenSet-MLP datasets. At each hardware platform, we hold out a test set that consists of five networks, ResNet-50, MobileNet-V2, ResNext-50, BERT-tiny, and BERT-base, with batch size 1 and image size 224 (or sequence length 128). Divide all the remaining data into training and validation sets at a ratio of 9:1. Use the top-1 score and top-5 score as evaluation criteria, which have been proven effective in TenSet. The expression of top-k is as follows:

$$top - k = \frac{\sum_m \sum_s \min_{\text{latency}_{m,s}} \times \text{weight}_{m,s}}{\sum_m \sum_s \min_{\text{latency}_{m,s}} \times \text{weight}_{m,s}}, 1 \leq i \leq k$$

where $\min_{\text{latency}_{m,s}}$ is the minimum latency among all tensor programs of subgraph s of model m, $\text{weight}_{m,s}$ is the number of times the subgraph s appears in model m, and $\text{latency}_{m,s,i}$ is the latency corresponding to the i-th largest value of the output score of the cost model for all tensor programs of subgraph s of model m. If not explicitly stated, all top-1 scores in the following text refer to the top-1 scores on the five models in the above test set. The same goes for top-5.

6.1.1 Loss Function & Backbone Basic Module. First, we experiment with the loss function and the backbone basic module. For the loss function, the label of TLP is a normalization value in the range of [0,1], so MSE loss is an option. In addition, lambda rank loss designed for ranking tasks is also an option. For the backbone basic module, since the input feature of TLP is a sequence composed of schedule primitives, both LSTM and self-attention are suitable.

We use the TenSet CPU dataset collected from Intel Xeon Platinum-8272. Table 3 shows the top-k scores for different combinations of loss functions and backbone basic modules. We can find that self-attention + lambda rank loss is slightly more suitable for TLP than the other combinations. If not explicitly stated, all experiments in the following text use the combination of self-attention + lambda rank loss.

6.1.2 Feature Size Cropping. As we discussed earlier, all schedule primitive sequences in the TenSet CPU dataset contain up to 54 schedule primitives, and each schedule primitive extracts up to 40 features. However, many are zero, leading to sparse features and affecting the cost model accuracy. We analyzed that reducing the feature size to 25x22 is a good choice. We do experimental verification on this.

We use the TenSet CPU dataset collected from Intel Platinum-8272. Table 4 shows the top-k scores for different combinations of sequence lengths and embedding sizes. The results show that reducing the sequence length and embedding size to 25 and 22, respectively, reduces the amount of computation and storage space while improving the accuracy of the cost model. We think this is because the features are denser at the cost of harming very few features, avoiding many zeros. If not explicitly stated, all experiments below use the combination of sequence length 25 + embedding size 22.

| Table 3: The top-k scores for different combinations of loss functions and backbone basic modules. |
|---------------------------------|-----------------|-----------------|
|                               | Top-1 Score     | Top-5 Score     |
| Attention + Rank              | 0.9194          | 0.9150          |
| Attention + MSE               | 0.9228          | 0.9542          |
| LSTM + Rank                   | 0.9119          | 0.9069          |
| LSTM + MSE                    | 0.9061          | 0.9540          |

| Table 4: The top-k scores for different combinations of sequence lengths and embedding sizes. |
|---------------------------------|-----------------|-----------------|
|                               | Seq Len 25 + Emb Size 22 | Top-1 Score     | Top-5 Score     |
|                               | 0.9194          | 0.9150          |
| Seq Len 25 + Emb Size 40      | 0.9171          | 0.9558          |
| Seq Len 54 + Emb Size 22      | 0.9076          | 0.9877          |
| Seq Len 54 + Emb Size 40      | 0.9076          | 0.9877          |
6.1 Other Model Architecture Details. We also perform extensive experiments to determine some details of the model architecture. Here, we list the results. It is sufficient that shallow linear layers in the model upsample the embedding size from 22 to 256, and 512 or larger is not required. The self-attention module sets 8 heads with the highest accuracy. Using one layer of the self-attention module is enough, and there is no need to use multiple layers or transformers. The self-attention module followed by two residual blocks is more accurate than zero, one or more residual blocks. If not explicitly stated, these settings are used in subsequent experiments.

6.1.4 Compare with TenSet MLP. After the experiments above, the model architecture of TLP is determined. We compare it with the state-of-the-art TenSet MLP cost model. Compared with Ansor, TenSet MLP pre-trained on the TenSet dataset can accelerate the search time by up to 10x. We employ the TenSet and TenSet-TLP datasets collected from all platforms, including 5 CPUs and 2 GPUs.

Table 5 shows the top-k scores of TLP and TenSet MLP on all hardware platforms of the TenSet and TenSet-TLP datasets. It can be found that on all CPUs, TLP exceeds TenSet MLP by a large margin. On GPUs, TLP and TenSet MLP each have their strengths. However, later experiments prove that since TLP extracts features from schedule primitives rather than tensor programs, this saves much tuning time for TLP. TLP still outperforms TenSet MLP on GPUs. As seen from the top-5 scores, TLP has stable performance on different CPUs and GPUs. It is worth mentioning that TenSet MLP performs special feature extraction for CPUs and GPUs, and TLP uses the same mechanism to extract CPU and GPU features.

We can say that TLP feature extraction is a simple yet effective and general method. This is mainly due to a shift in our thinking about feature extraction. We do not extract features from the tensor program itself but schedule primitives. In the feature extraction process, we are not limited by prior knowledge and prune any features in advance because it cannot be proven that pruned features are detrimental to improving accuracy. We delegate this process to a neural network to weigh the importance of features through learnable weights.

6.2 MTL-TLP with Dataset-Based Metrics

6.2.1 Effectiveness of MTL-TLP. To determine the effectiveness of MTL-TLP, we conduct experiments on CPUs and GPUs, respectively. We set up 4 experiments on CPUs, specifying Intel E5-2673 as the target hardware platform. The first experiment set up a task using 500K data collected from Intel E5-2673. The second experiment sets up two tasks: the first uses 500K data collected from Intel E5-2673, and the second uses all data collected from Intel Xeon Platinum 8272. The settings for the remaining two CPU experiments are similar. We set up 2 experiments on GPUs, specifying NVIDIA Tesla T4 as the target hardware platform. The experimental setup for GPUs is similar to that for CPUs.

Tables 6 and 7 show the top-k scores of multi-task learning for CPUs and GPUs, respectively. The top-k scores here are for the target hardware. The results show that using multi-task learning can significantly improve the accuracy of the cost model. Combining with Table 5, it can be found that even using only 500K data exceeds the TenSet MLP using all data and is on par with TLP using all data but without multi-task learning. Table 6 also shows that appropriately increasing the number of tasks can improve the accuracy of the cost model. However, if there are too many tasks, it will hinder the accuracy increase. This is because appropriately increasing the number of tasks can make the features learned by the MTL-TLP backbone more general and have a stronger generalization ability. However, if too many tasks exist, the interference between tasks increases, and sharing parameters cannot make the target platform task reach the optimal point.

6.2.2 Transfer Learning & Self-supervised Learning. In this part, we will discuss various transfer learning and self-supervised learning methods. We set up 4 experiments: 1) Pre-training the cost model with all Intel E5-2673 data, then fine-tuning with 500K Intel i7-10510U data; 2) Training the cost model with multi-task learning techniques, task 1 uses 500K Intel i7-10510U data, task 2 uses all Intel E5-2673 data; 3) Use the cost model as a downstream task of GPT, first use all Intel i7-10510U data (without label) to pre-train a GPT model, and then use 500K Intel i7-10510U data training the cost model; 4) Similar to 3, but trains a BERT model. Table 8 shows the top-k scores for the above 4 experiments. Compared with fine-tuning, MTL is more suitable for solving the problem of unavailability across hardware. The two methods of GPT and BERT, as analyzed in the previous chapters, have a huge amount of parameters that are a burden for small-sized input features and are prone to overfitting.

6.2.3 Multi-task Learning Between Architectures. We think that the effect of multi-task learning on the accuracy improvement of the target platform is different between different hardware architectures. To verify this, we set up four experiments with Intel i7-10510U as the target platform, and all experiments set up two tasks. All the first tasks use 500K data collected from Intel i7-10510U. The second task uses all data collected from Intel Platinum 8272, Intel E5-2673, AMD EPYC 7452, and ARM Graviton2, respectively.

Table 9 shows the top-k scores for multi-task learning between architectures. The target hardware Intel i7-10510U is the Intel X86 architecture, and Intel Platinum 8272 and Intel E5-2673, both of which are X86, have the most considerable precision improvement on the target hardware. AMD and ARM CPUs also have improved precision on the target hardware, but they are not as good as the Platinum 8272 and Intel E5-2673.

6.2.4 Multi-task Learning with Data Size. We explore the relationship between MTL-TLP accuracy and target platform data size. The experiments set up two tasks, the second task uses all the data collected from Platinum 8272, and the first task uses 50K, 100K, 300K, 500K, 700K, 900K, 1.2M, 1.5M, and 2.0M data respectively. The results are shown in Figure 9. When the data size increases to 500K, we see the most improvement, and the accuracy of MTL-TLP exceeds that of TenSet MLP.

Combining Sections 6.2.3 and 6.2.4, when using MTL-TLP, we recommend setting up two to three tasks, with non-target platform tasks using all data from the same instruction set architecture hardware platform and the target platform task using at least 500K data.
Table 5: The top-k scores of TLP and TenSet MLP on all hardware platforms of the TenSet and TenSet-TLP datasets.

| Hardware Platform                        | TenSet Top-1 Score | TenSet Top-5 Score | TenSet-TLP Top-1 Score | TenSet-TLP Top-5 Score |
|------------------------------------------|--------------------|--------------------|------------------------|------------------------|
| Intel Platinum 8272CL @ 2.60GHz (16 cores) | 0.8748             | 0.9527             | 0.9194                 | 0.9710                 |
| Intel E5-2673 v4 @ 2.30GHz (8 cores)     | 0.8332             | 0.8977             | 0.8941                 | 0.9633                 |
| ARM EPYC 7542 @ 2.350GHz (16 cores)      | 0.7979             | 0.9049             | 0.8207                 | 0.9226                 |
| Intel E5-2673 v4 @ 2.3GHz (8 cores)      | 0.8510             | 0.9175             | 0.9055                 | 0.9494                 |
| ARM Graviton2 (16 cores)                 | 0.7736             | 0.9049             | 0.8207                 | 0.9226                 |
| NVIDIA Tesla K80                         | 0.9083             | 0.9629             | 0.9055                 | 0.9494                 |
| NVIDIA Tesla T4                          | 0.8737             | 0.9328             | 0.8647                 | 0.9250                 |

Figure 9: Accuracy curves of MTL-TLP using different data sizes.

6.3 Search-Based metrics

End-to-end search efficiency and search quality are still the golden standards for checking the performance of a cost model. We integrate all the techniques discussed earlier into the auto-tuning framework Ansor and perform extensive experiments on both CPU and GPU.

The hardware platform of the CPU experiment is a notebook with an 8-core Intel i7-10510U, 16GB memory, and 2GB NVIDIA MX350. The hardware platform for GPU experiments is an 8-core Intel Platinum 8255C, 32GB memory, and 16GB NVIDIA Tesla T4. We perform the following four experiments on five representative models, ResNet-50, MobileNet-V2, ResNext-50, BERT-tiny, and BERT-base with batch size 1 and image size 224 (or sequence length 128): 1) Tuning with Ansor; 2) Tuning with TenSet MLP; 3) Tuning with TLP; 4) Tuning with MTL-TLP-500K. Among them, MTL-TLP-500K sets up two tasks. When training the model for the CPU platform, task one uses 500K Intel i7-10510U data, and task two uses all Intel Platinum-8272 data. When training the model for the GPU platform, task one uses 500K NVIDIA Tesla T4 data, and task two uses all NVIDIA Tesla K80 data.

TenSet transfer learning trains a local model to predict the gap between the source and target platforms. However, it does not rely on offline datasets of the target platform. For fairness, MTL-TLP trained with 500K target platform data is not directly compared with TenSet transfer learning but with TenSet MLP trained with all target platform data.

Here we briefly introduce Ansor’s tuning process. Ansor will first generate some initial tensor programs for a subgraph according to predefined rules. Then use the cost model to pick out potential tensor programs. Use these potential tensor programs to generate more tensor programs through the genetic algorithm and use the cost model again to prune the poor performers. This step will iterate multiple times. Put the last selected n tensor programs on the target machine to measure the latency. The above is called a tuning round. After Ansor tunes all subgraphs in a workload for one round, it divides the remaining time budgets into each subgraph according to the task schedule algorithm. All our experiments are tuned for 200 rounds, each round picking 10 tensor programs to measure, a total of 2,000 measurements, which we call tuning 2,000 times in the following.

Table 8: The top-k scores for various transfer learning and self-supervised learning methods.

| Method                        | Top-1 Score | Top-5 Score |
|-------------------------------|-------------|-------------|
| Fine-tuning E5-2673 (Pre-trained) | 0.7897      | 0.9175      |
| MTL E5-2673 (Task 1) | 0.8331      | 0.9672      |
| GPT E5-2673 (Task 2) | 0.6863      | 0.8431      |
| BERT E5-2673 (Task 2) | 0.6316      | 0.8135      |

Table 9: The top-k scores between architectures.

| Architecture | Top-1 Score | Top-5 Score |
|--------------|-------------|-------------|
| i7-10510U Platinum-8272 | 0.8413 | 0.9202 |
| i7-10510U E5-2673 | 0.8331 | 0.9672 |
| i7-10510U EPYC-7452 | 0.8082 | 0.9122 |
| i7-10510U Graviton2 | 0.7711 | 0.8909 |
TLP: A Deep Learning-Based Cost Model for Tensor Program Tuning

7 RELATED WORK

Recently, the rapid development of tensor compilers has spawned several schemes, including Halide [29], TVM [10], Tensor Comprehensions [32], TACO [23], DeepCuts [20], nGraph [15], XLA [31], and TIRAMISU [6].

Auto-tuners and cost models. AutoTVM [11] is a template-based automatic search framework, the first search framework integrated in TVM. Subsequently, to deal with the limited search space caused by predefined templates, Anson [38] proposed an automatic search framework based on hierarchy. Bolt [36] bridges the huge performance gap between tensor compilers and hardware-native libraries using hardware-native templated search enabled by modular and configurable libraries provided by hardware vendors. Benoit Steiner et al. [30] use the value learning of reinforcement learning and a bidirectional LSTM cost model to solve the automatic tuning problem. It adopts a reinforcement learning-based search strategy, using the cost of the tensor program as the reward value during reinforcement learning. ProTuner [18] uses Monte Carlo tree search to solve the inaccurate estimation problem in the Halide auto-scheduler. The TIRAMISU cost model [5] extracts loop information, buffer access matrix, and AST information from the tensor program and propagates the data forward recursively according to the AST structure. FlexTensor [40] proposes a general template to cover multiple operators, and its template is designed for single operator granularity. The polyhedral compilation model [4, 7, 33, 34] formalizes the problem of automatic code optimization as an integer linear programming (ILP) problem. It optimizes a program with affine loop transformation that minimizes the data reuse distance between dependent statements. DeepTune [14] proposes to predict whether an OpenCL kernel should be mapped to CPU or GPU.

Tensor program datasets. TenSet [39] is a large-scale tensor program dataset that continues Anson’s work. The TIRAMISU cost model and the work of Benoit Steiner et al. [30] also collect some tensor program datasets, but neither is open source.

Cross-hardware solutions. There are few studies on cost models across hardware platforms. TenSet builds a local model to predict the latency gap between the source and target hardware. Moses [37] uses model distillation to distill out transferable and non-transferable parameters.

8 DISCUSSION

Limitation. Although we significantly address the unavailability of cost models across platforms, MTL-TLP trained with only 7% of the target platform data outperforms TenSet MLP with all data. However, it still takes tens of hours to collect 500K data. The cross-hardware unavailability requires more research.

Future Work. We have demonstrated the feasibility of schedule primitives as tensor program equivalents. We implement TLP and MTL-TLP in Ansor, which can be easily migrated to other tensor compiler automatic search frameworks. We have transformed the tensor program tuning into an NLP regression task. Based on this,
it can be tried to use more mature NLP techniques to solve tensor program problems.

9 CONCLUSION

This paper proposes TLP and MTL-TLP. TLP designs a simple yet effective and general feature extraction mechanism for tensor program tuning. MTL-TLP utilizes multi-tasking techniques to solve the offline cost model cross-hardware unavailability. We analyze the feasibility and advantages of schedule primitives as objects for feature extraction. We theoretically analyze the reasons why MTL-TLP is effective. In the experimental part, we verify the effectiveness of TLP and MTL-TLP from database-based and search-based metrics. Experiments show that TLP and MTL-TLP outperform state-of-the-art implementations by a large margin.

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REFERENCES

[1] Andrew Adams, Karima Ma, Luke Anderson, Riyadh Baghdadi, Tzu-Mao Li, Michael Gharbi, Benoit Steiner, Steven Johnson, Kayvon Fatahalian, Frédou Durand, et al. 2019. Learning to optimize halide with tree search and random programs. ACM Transactions on Graphics (TOG) 38, 4 (2019), 1–12.

[2] Byung Hoon Ahn, Prannoy Pilligundla, Amir Yazdanbakhsh, and Hadi Esmaeilzadeh. 2020. Chameleon: Adaptive code optimization for expedited deep neural network compilation. arXiv preprint arXiv:2001.08743 (2020).

[3] Luke Anderson, Andrew Adams, Karima Ma, Tzu-Mao Li, and Jonathan Ragan-Kelley. 2020. Learning to schedule halide pipelines for the gpu. arXiv preprint arXiv:2012.07145 (2020).

[4] Riyadh Baghdadi, Ulysse Beaugnon, Albert Cohen, Tobias Grosser, Michael Kruse, Chandan Reddy, Sven Verdoolaege, Adam Betts, Alastair F Donaldson, Jeroen Ketema, et al. 2015. Pencil: A platform-neutral compute intermediate language for accelerator programming. In 2015 International Conference on Parallel Architecture and Compilation (PACT). IEEE, 138–149.

[5] Riyadh Baghdadi, Massinissa Merouani, Mohamed-Hicham Leghettas, Kamel Abdou, Tahar Arbaoui, Karima Benatchba, et al. 2021. A deep learning based cost model for automatic code optimization. Proceedings of Machine Learning and Systems 3 (2021), 181–193.

[6] Riyadh Baghdadi, Jessica Ray, Malek Ben Romdhane, Emanuele Del Sozzo, Abdurrahman Akkas, Yunming Zhang, Patricia Suriana, Shoaib Kamil, and Saman Amarasinghe. 2019. Tiramisu: A polyhedral compiler for expressing fast and portable code. In 2019 IEEE/ACM International Symposium on Code Generation and Optimization (CGO). IEEE, 193–205.

[7] Uday Bondhugula, Albert Hartono, Jagannathan Ramanujam, and Ponnuswamy Sadayappan. 2008. A practical automatic polyhedral parallelizer and locality optimizer. In Proceedings of the 29th ACM SIGPLAN Conference on Programming Language Design and Implementation. 101–113.

[8] Tom Brown, Benjamin Mann, Nick Ryder, Melanie Subbiah, Jared D Kaplan, Prafulla Dhariwal, Arvind Neelakantan, Pranav Shyam, Girish Sastry, Amanda Askell, et al. 2020. Language models are few-shot learners. Advances in neural information processing systems 33 (2020), 1877–1901.
[9] Zhe Cao, Tao Qin, Tie-Yan Liu, Ming-Feng Tsai, and Hang Li. 2007. Learning to rank: from pairwise approach to listwize approach. In Proceedings of the 24th international conference on Machine learning. 129–136.

[10] Tianqi Chen, Thierry Moreau, Ziheng Jiang, Liannin Zheng, Eddie Yan, Haichen Shen, Meghan Cowan, Leyuan Wang, Yuwei Hu, Luis Ceze, et al. 2018. [TVM]: An Automated [End-to-End] Optimizing Compiler for Deep Learning. In 10th USENIX Symposium on Operating Systems Design and Implementation (OSDI 18). 578–594.

[11] Tianqi Chen, Liannin Zheng, Eddie Yan, Ziheng Jiang, Thierry Moreau, Luis Ceze, Carlos Gusteun, and Arvind Krishnamurthy. 2018. Learning to optimize tensor programs. Advances in Neural Information Processing Systems 31 (2018).

[12] Yaran Chen, Dongbin Zhao, Le Lv, and Qichao Zhang. 2018. Multi-task learning for dangerous object detection in autonomous driving. Information Sciences 432 (2018), 559–571.

[13] Sathuwardha Chowdhuri, Tushar Pankaj, and Karl Zipser. 2019. Multinet: Multi-modal multi-task learning for autonomous driving. In 2019 IEEE Winter Conference on Applications of Computer Vision (WACV). IEEE, 1496–1504.

[14] Chris Cummins, Pavlos Petoumenos, Zheng Wang, and Hugh Leather. 2017. End-to-end deep learning of optimization heuristics. In 2017 26th International Conference on Parallel Architectures and Compilation Techniques (PACT). IEEE, 219–232.

[15] Scott Cyphers, Arjun K Bansal, Anahita Bhawandwalla, Jayaram Bobba, Matthew Brookhart, Avijit Chakraborty, Will Constable, Christian Convey, Leona Cook, Omar Kanawi, et al. 2018. Intel igraph: An intermediate representation, compiler, and executor for deep learning. arXiv preprint arXiv:1801.08058 (2018).

[16] Jacob Devlin, Ming-Wei Chang, Kenton Lee, and Kristina Toutanova. 2018. Bert: Pre-training of deep bidirectional transformers for language understanding. arXiv preprint arXiv:1810.04805 (2018).

[17] Daixiang Dong, Hua Wu, Wei He, Dianhai Yu, and HaiFeng Wang. 2015. Multi-task learning for multiple language translation. In Proceedings of the 53rd Annual Meeting of the Association for Computational Linguistics and the 7th International Joint Conference on Natural Language Processing (Volume 1: Long Papers). 1723–1732.

[18] Ameer Haj-Ali, Hasan Gene, Qiqing Huang, William Moses, John Wawrzynek, Krot Anasovic, and Ion Stoica. 2020. Protouner: tuning programs with monte carlo tree search. arXiv preprint arXiv:2005.13685 (2020).

[19] Xiaoqi Jian, Yichun Yin, Lifeng Shang, Xin Jiang, Xiao Chen, Linlin Li, Fang Wang, and Qun Liu. 2019. Tinybert: Distilling bert for natural language understanding. arXiv preprint arXiv:1909.10351 (2019).

[20] Wooleun Jung, Thanh Tuan Dao, and Jaein Lee. 2021. DeepCut: A deep learning optimization framework for versatile GPU workloads. In Proceedings of the 42nd ACM SIGPLAN International Conference on Programming Language Design and Implementation. 198–205.

[21] Sam Kaufman, Phitchaya Phothilimthana, Yanqi Zhou, Charith Mendis, Sudip Roy, Amit Sabne, and Mike Burrows. 2021. A learned performance model for optimization framework for versatile GPU workloads. In Proceedings of the 42nd ACM SIGPLAN International Conference on Programming Language Design and Implementation (OSDI 20). 863–879.

[22] Alex Kendall, Yarin Gal, and Roberto Cipolla. 2018. Multi-task learning using uncertainty to weigh losses for scene geometry and semantics. In Proceedings of the IEEE conference on computer vision and pattern recognition. 7482–7491.

[23] Fredrik Kjolstad, Shoaib Kamil, Stephen Chou, David Lugato, and Suman Amarasinghe. 2017. The tensor algebra compiler. Proceedings of the ACM on Programming Languages 1, OOPSLA (2017), 1–29.

[24] Pengfei Liu, Xiqeng Qu, and Xiaojing Huang. 2016. Recurrent neural network for text classification with multi-task learning. arXiv preprint arXiv:1605.0101 (2016).

[25] Ravi Teja Mullapudi, Andrew Adams, Dillon Sharlet, Jonathan Ragan-Kelley, and Kayvon Fatahalian. 2016. Automatically scheduling halide image processing pipelines. ACM Transactions on Graphics (TOG) 35, 4 (2016), 1–11.

[26] Jan Niehues and Eunah Cho. 2017. Exploiting linguistic resources for neural machine translation using multi-task learning. arXiv preprint arXiv:1708.00993 (2017).

[27] Alec Radford, Karthik Narasimhan, Tim Salimans, Ilya Sutskever, et al. 2018. Improving language understanding by generative pre-training. (2018).

[28] Alec Radford, Jeffrey Wu, Rewon Child, David Luan, Dario Amodei, Ilya Sutskever, et al. 2019. Language models are unsupervised multitask learners. OpenAI blog 1, 8 (2019), 9.

[29] Jonathan Ragan-Kelley, Connelly Barnes, Andrew Adams, Sylvain Paris, Frédéric Durand, and Suman Amarasinghe. 2018. Halide: A language and compiler for optimizing parallelism, locality, and recomputation in image processing pipelines. Acm Sigmod Notices 48, 8 (2013), 519–530.

[30] Benoit Steiner, Chris Cummins, Horace He, and Hugh Leather. 2021. Value learning for throughput optimization of deep learning workloads. Proceedings of Machine Learning and Systems 3 (2021), 323–334.

[31] TensorFlow. [n.d.]. XLA: Optimizing Compiler for TensorFlow. https://www.tensorflow.org/xla. [Online; accessed 19-September-2019].

[32] Nicolas Vaslachle, Oleksandr Zinenko, Theodoros Theodoridis, Priya Goyal, Zachary DeVito, William S Moses, Sven Verdoolaege, Andrew Adams, and Albert Cohen. 2018. Tensor comprehensions: Framework-agnostic high-performance machine learning abstractions. arXiv preprint arXiv:1802.04730 (2018).

[33] Sven Verdoolaege. 2016. Presburger formulas and polyhedral compilation. (2016).

[34] Sven Verdoolaege, Juan Carlos Juega, Albert Cohen, Jose Ignacio Gomez, Christian Tennlaid, and Francy Catthoor. 2013. Polyhedral parallel code generation for CUDA. ACM Transactions on Architecture and Code Optimization (TACO) 9, 4 (2013), 1–23.

[35] Xuanhui Wang, Cheng Li, Nadav Golbandi, Michael Bendersey, and Marc Njork. 2018. The lambdaloss framework for ranking metric optimization. In Proceedings of the 27th ACM international conference on information and knowledge management. 1313–1322.

[36] Jiarong Xing, Leyuan Wang, Shang Zhang, Jack Chen, Ang Chen, and Yibo Zhu. 2022. Bolt: Bridging the Gap between Auto-tuners and Hardware-native Performance. Proceedings of Machine Learning and Systems 4 (2022), 204–216.

[37] Zhihe Zhao, Xian Shiui, Yang Bai, Naiwen Ling, Nan Guan, Zhenyu Yan, and Guoliang Xing. 2022. Moses: Efficient Exploitation of Cross-device Transferable Features for Tensor Program Optimization. arXiv preprint arXiv:2001.07572 (2022).

[38] Liannin Zheng, Chengfan Jia, Minmin Sun, Zhao Wu, Cody Hao Yu, Ameer Haj-Ali, Yida Wang, Jun Yang, Danyang Zhao, Koushik Sen, et al. 2020. Amor: Generating [High-Performance] Tensor Programs for Deep Learning. In 14th USENIX Symposium on Operating Systems Design and Implementation (OSDI 20).

[39] Tianqi Chen, Chengliang Jia, Minmin Sun, Zhihe Zhao, Yuanhui Wu, WokieunJung, Thanhtuan Dao, and Jie Jin. 2021. 845

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