Performance characterization for high frequency CMOS voltage control ring oscillators

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Abstract. This article mainly emphases on the performance study and characterization of CMOS voltage control ring oscillator (VCRO). The performance analysis is based on high frequency, low area, and low phase noise for different kind of techniques of VCRO at various supply voltages. The results shows higher frequency and less phase noise which can be suitable for different domain applications. Further advantage is as go on reducing the supply voltage the frequency of the VCRO is increasing rapidly. This paper helps the designers in order to choose the most suitable voltage control ring oscillator (VCRO) for their specific applications.

Keywords: Voltage control oscillator, Inverters, Ring oscillator, Delay stages

1. Introduction

The utmost important, efficient, and critical part of any electronic and communication systems are voltage control ring oscillator (VCRO). They widely used electronic applications like phase locked loop (PLL) [17], frequency synthesizer and telecommunications [37] i.e. digital wireless domain in which the VCO is the internal crucial element. An oscillator is defined as the output frequency is dependent and organized by the input control voltage which produces an episodic output with frequency of oscillation and definite amplitude.

The CMOS VCO can be designed by using LC resonator circuit, ring oscillator and relaxation oscillator [9, 10]. The LC oscillator design strategy provides better phase noise and high frequency of oscillation nevertheless small tuning range. Still, adding of large inductors increase the price and difficulty of chip i.e. bulky design. Whereas CMOS ring oscillator design do not need inductor which deteriorate the area and will have wide tuning range, easy for integration and can design any CMOS design process flow, but it has worst noise performance and lower operating frequency.

The output frequency for ideal VCO is given by equation

\[ f_{\text{vco}} = f_0 + K_{\text{vco}} V_{\text{ctr}} \]  

(1)

Where \( f_0 \) = Centre frequency of VCO

\( K_{\text{vco}} \) = Gain of the VCO

\( V_{\text{ctr}} \) = Input Control voltage

Due to the reasons mentioned above the CMOS ring oscillator are more flexible when compared to other type CMOS VCO for on chip fabrication.
The organization of the remaining work will go along with: section II explains about the overview of the conventional ring oscillators. Section III deals with the different types of methods in VCRO which increases the performance parameters of circuit. To end with, Section IV concludes the paper.

2. CMOS Ring Oscillator
A CMOS VCRO can be simply made by an odd sum of inverters cascaded in form of chain with a feedback path, where output of the latter step is feedback to the input of the leading step then each inverter has an equal propagation delay ($\Delta t$).

In order to get sustained oscillations the ring oscillator has to satisfy the barkhausen criteria which states as:

1. Where the signal continues from input over amplifier, feedback network backwards to the input yet again completing a loop, the overall phase shift round the loop is 0 degree or 360 degree.
2. The magnitude of the product of the open loop gain of the amplifier ($A$) and feedback factor ($\beta$) is unity. (i.e.) $|A\beta|=1$.

The schematic diagram of the ring oscillators with N delay stages is shown in figure 1 and the conventional ring Oscillators employing 3 delay stages are shown in figure 2. The delay stage comprises of NMOS and PMOS transistors which are linked in series i.e. as inverter.

![Figure 1: CMOS ring oscillator](image)
The frequency of oscillations can express as

\[ F_0 = \frac{1}{2N(\Delta t)} \]  

(2)

Where N= Number of delay elements

\( \Delta t \) = Propagation delay of each inverter.

In order to enhance this circuit beneficial, the oscillation frequency should be manageable. As understood in (2), the major constraints which disturb the frequency are the N number of stages, and the delay per each stage \( \Delta t \). So it is challenging to execute the existing method which can change the number of stages in the ring. Thus, \( \Delta t \) must be flexible in order to provide voltage controlled oscillator. Unique technique to regulate the lag of time is to regulate the quantity of current offered to charge or discharge the capacitive load of every stage. This category of circuit is entitled as current starved ring oscillator.

3. Various design methods of VCRO: Performance characteristics Analysis

3.1 Voltage controlled ring oscillator based on biasing method:

As mentioned above we already know that conventional ring oscillator are compact in design and provide extensive broadband range, with less phase noise and attractive for the digital applications because of the integration. The proposed article states that the current starved ring oscillator provide high tuning range, less size in area, lesser phase noise when compared to the conventional ring oscillators [1]. This work offers the frequency until 1GHz which has a supply voltage 1.8V with 180nm technology. The circuit proposed in this paper is like the conventional voltage control ring oscillator (VCRO) which is exposed in figure 3.
Figure 3: single delay stage of current starved ring oscillator

From the figure 4 the transistors M5 and M8 operate as an inverter which are connected in series and while M1 and M11 act as current sources. Which will bind the availability of currents to the M5 and M8 transistors the currents are same for each inverter. Control voltage ($V_{\text{ctrl}}$) via current mirror is used to modulate the on resistances of the pull-up and pull-down transistors. The controlling of current to charge or discharge the load capacitances is done by variable resistances. Large value of control voltage permits a huge current to flow, responsible of small resistance, less delay and high frequency. Basically, this type of VCO employ variable bias current to ensure complete command on frequency of oscillation, which leads to high oscillation frequency.

Figure 4: Current starved ring oscillator with 3 delay stages.
With the support of small signal corresponding ideal of single delay cell of current starved ring vco, the
final gain of single stage CS ring VCO can be expressed as
\[
\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} = 2
\]  
(3)

The frequency of oscillations \(f_{\text{osc}}\) for current starved ring oscillator can be expressed in accordance
with the total capacitance \((C_{\text{total}})\), input control voltage \((V_{\text{ctr}})\), current \((I_d)\) and count of delay stages \((N)\)

\[
f_{\text{osc}} = \frac{I_d}{2 \times N \times C_{\text{total}} \times V_{\text{ctr}}}
\]  
(4)

Where
- \(C_{\text{total}}\) = Total capacitance
- \(V_{\text{ctr}}\) = Input control voltage
- \(I_d\) = Current
- \(N\) = count of delay stages

The considered VCO over a temperature range from -40°C to 125°C it is producing a frequency of
1.06GHz & the elongation is accomplished above a kind of frequency as of 970MHz to 1.03GHz.

3.2 An Enhanced Performance Ring Oscillator Design:
The policy is to improve recurrence execution of CMOS ring oscillator. In order to support exchanging
rate of oscillator delay cell it depends on the expansion of MOS semiconductor. The technique utilized
here is for basic and differential oscillator and suggests a basic method to actualize frequency tuning
short of presentation of some extra stage phase noise [2]. Utilizing 130nm CMOS innovation, simulation
outputs demonstrates that applying this method to the basic ring oscillator permits a recurrence uncertain
development of 80%. Likewise, simulation shows that frequency development can arrive at 300 % if the
process is related near a ppositive input.

Figure 5: Proposed VCRO circuit
The conventional ring oscillator with the addition of MOS transistors will give the improved
performance in frequency of oscillations this technique improves the switching speed of delay cell of
the oscillator. The diagrammatic representation of three stage ring VCRO is exposed in figure 5 and
outputs are executed by spectre RF in AMS 0.35-m CMOS technology with \(V_{\text{dd}} = 3V\). The transistors
pull-up and pull-down or of same size W/L=10m/0.3m. We chose W/L=1m/3m for transistor M2 and W/L=1m/0.3m for transistor M3 correspondingly. When compared with the conventional VCO the proposed oscillator displays an oscillation frequency of 4.4 GHz in contradiction of 2.7 GHz so the oscillation frequency shoot up to 78%. The power consumption of the offered VCRO at 4.4GHz is 12.5 which increase twice that of the conventional one at 2.7 GHz. There is no drop of the phase noise for the suggested VCRO related with the standard design: -98 dBc at 1 MHz from 4.4 GHz for the earlier and -96 dBc at 1MHz from 2.7 GHz. For next as already mentioned, the gate control M3 transistor can tune the oscillation frequency of the suggested oscillator. The substrate bias voltage $V_{bb}$ extending to 3.3V from 0.5V, the oscillation frequency changes to 4.4GHz from 4.2 GHz.

3.3 Voltage-Controlled Ring Oscillator established on resistive element:
A model of a VCRO will be introduced for the execution of low frequency ring oscillator is quiet minor devices and will have lesser amount of stage. This will be executed by applying .18um technology and will deliver by TSMC technology applying 3.3v power resource [3]. The VCRO network process presents are full tuning range from 2Hz to 368.9MHz. The quick voltage fluctuation and 48% duty cycle are also comprised, which are hard to attain from traditional oscillator. Its dissipation of power is 35.05mW at the highest oscillation frequency. A framework job in CMOS ring oscillators to model the phase noise. For executed circuits, phase noise is -88dBc while the offset frequency is 105 HZ. The scheme of a circuit is shown in the below figure 6. The variable resistor $R_v$ at the input terminal of every inverter is added here. As seen, the inverter itself is made of PMOS and NMOS transistors are shown in figure 7. It is also possible to calculate the delay of each stage $t_p$ from figure 7.

![Figure 6: proposed voltage control ring oscillator](image)

Subsequently the MOS transistors can be considered as switches in each inverter, a resistance $\frac{1}{G_m}$ can be replaced as shown in figure 6. If the transconductances of $G_m$s and $C_g$s of NMOS and PMOS transistors are identical to the parasitic capacitances, then delay of each step of the inverter ($t_p$) will be approximately.

$$t_p = \frac{C_g (1 + G_M R_v)}{G_m}$$  \hspace{1cm} (5)

For a very large $R_v$ such as $G_M R_v >> 1$, the time constant of $R_v C_g$ irrespective of the value of $G_m$ will calculate the delay. If $R_v = 0$ gives

$$t_p = \frac{C_g}{G_m}$$  \hspace{1cm} (6)
For a simple inverter process, this is a delay. Finally, it is possible to discover the oscillation frequency as

\[ f_{\text{osc}} = \frac{G_{M}}{2Nc_{C}(1 + G_{M}R_{\nu})} \]  

(7)

The above equation shows that the frequency of oscillation is influenced by \( G_{M} \) transconductance values, \( R_{\nu} \) resistance, \( C_{G} \) capacitance. \( G_{M} \) and \( C_{G} \), however, are system parameters and are believed to be constant. In conclusion, it is possible to monitor the oscillation frequency by adjusting the value of the \( R_{\nu} \).

3.5 FGMOS transistor based voltage controlled ring oscillator:

This work exhibits the voltage control ring oscillator (VCRO) which has delay element consists of floating gate metal oxide semiconductor (FGMOS) transistor [7]. The expected performance of the VCRO is projected with the further systems by using Berkeley predictive technology model (BPTM) by using 45nm method by power supply voltage = 1V. It doesn’t require any additional components needed the voltage control behaviour is done by the delay element only. The VCRO based on FGMOS transistor has better linearity from 0V to maximum supply voltage.

Figure 8: An FGMOS centred VCRO (a) NMOS meticulous transistor (b) PMOS meticulous transistor

The FGMOS has 2 types of gates: floating gate and control gate. The floating gate metal oxide semiconductor (FGMOS) the as the name suggests floating gate terminal is electrically isolated creating a floating node to the DC which is surrounded by the oxide layer and the control gate where multiple inputs are given on top them. The inputs are capacitively connected and as the floating gate is surrounded with oxide layer which is extremely resistive element the charge accommodate in it is unbothered for more duration of time considering the conventional VCRO there is a delay element which is an inverter circuit consisting of basic NMOS and PMOS transistors and this FGMOS VCRO is replaced with the FGMOS transistor with the conventional NMOS and vice versa. Usually altogether the phases in regular ring oscillator are alike so the frequency of oscillation (\( f_{\text{osc}} \)) can be controlled by changing the delay time (\( t_{\nu} \)) which can be diverse by change in current in every stage of VCRO, as shown in the figure 8(a) & (b) the control voltage(\( V_{\nu} \)) is linked to one of the terminal of control gate and other terminal of the control gate is connected to the input supply. Thus the voltage is controlled by the delay element itself which reduces the area and power consumption without adding any extra element. Subsequently the channel in the FGMOS transistor is encouraged by benefit of the applied voltages on every control gates,
here is not any certain on the control voltage in demand to go on the FGMOS transistor and accordingly control $F_{osc}$. Hence, one of the significant benefits of the obtainable VCRO is that a range that is greater than VDD can be used for controlling $F_{osc}$.

3.6 Voltage Controlled Ring Oscillator by Inductive Loading:
This paper presents the hybrid VCRO with the inductor loading which provides improved phase noise and figure of merit (FOM) [6]. This circuit can be utilised as the drop in replacement of ring VCO phase locked loop (PLL) to achieve expected enlargement in FOM. There is a prototype exhibited by improvement of FOM with 8db when compared to conventional VCRO. The proposed paper includes the regular ring VCO with output of inverter at each stage is connected to the identical inductor through the centre node as shown in figure (10).

![Figure 9: VCRO circuit with inductive load](image)

Here is no DC current can run over the inductors as they are symmetric to three phases of the voltage control ring oscillator at a voltage $V_c \approx \frac{V_{ring}}{2}$, is a “virtual ground” at $F_0$ and its harmonics. At multiples of $3F_0$, however, it seems as an open circuit this circuit resembles the open circuit as the 3 uniform cells are connected as shown in the linear model of the circuit. Even though this technique doesn’t meat to be nonlinear in nature for a conventional VCRO but it reaches the requirement of improving the FOM of the ring oscillator.

3.7 Voltage-controlled ring oscillator with reverse substrate bias process:
The proposed paper exhibits high oscillation frequency with small discharge voltage. A perfect methodology is provided for the given body biasing method for decrease of power utilization. The experimental consequences are implemented at room temperature 27°C by cadence virtuoso 45nm CMOS method with supply voltage Vdd = 0.7V which is flexible [9]. The outcomes concludes that the voltage controlled ring oscillator (VCRO) has described as low force voltage controlled oscillator (VCO) with respect of least discharge power (1.23 nW) and greatest swinging frequency (4.76 GHz) by combined positive channel metal oxide semiconductor (PMOS) and negative channel metal oxide semiconductor (NMOS) capsize body bias method.
Figure 10: Ring oscillator with NMOS reverse substrate bias
Normally controlling the body terminal of the MOSFETS provides enhanced performance in power consumption and to increase the standard of standby leakage which can be achieved by CMOS transistor arrangement with inverse body biasing. In substrate biasing method it utilises the body connection up to maximum extent as another controlling point which helps in tuning the threshold voltage [11]. Body biasing technique includes NMOS body bias, PMOS body bias and combined form of both MOS transistors substrate bias VCRO. In order to decrease the leakage power supply the body connections are joined to input supply voltage in reverse body bias technique as shown in figure 10. It’s concluded that Power can be saved by giving inverse biasing with constant voltage ($V_{dd} = 0.7V$).

3.8 steady state response of an ultra-bandwidth range CMOS ring VCO with inductor peeking:
As we know that there are 2 types of oscillators in which LC VCO has exceptional phase noise accomplishment and great oscillator frequency which is suitable for wireless and optical transceivers and the drawbacks are it has minor perfection range and dropping the data range rate in which a transceiver operates. Whereas the ring VCO are most suitable for the digital applications and it produces the copper-based wire line transceiver to have for wider tuning range, easy integration, and smaller chip size. It is an innovative thought to combine these two different ideas of VCO together to have numerous advantages keeping the basic constraints into mind [12]
In this proposed paper we inculcate peeking inductors with a distinctive RO-VCO arrangement, to gain combined outputs of more-broad band tuning range and lesser die area [4]. In this work the circuit is implemented in 130nm and 65nm technology in order to achieve parameters of the circuit. Where at 65nm technology can function up to 25.07 GHz with the tuning range.
In order to achieve the high oscillator frequency and primarily appreciated inductor is injected in order to offer a booming capacitance in each delay cell. This technique is called inductor peeking which is a basic method which is choose as for great speed amplifier scheme which is shown in figure 11.
Figure 11: Ring oscillator with inductor peaking

The transfer function is given by

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{-g_{m1}(R_{eff}+sL)}{s^2CL+sCR_{eff}+1}$$

(8)

Rearranging (8) we get (9)

$$\frac{V_{out}}{V_{in}} = g_{m1}R_{eff}\frac{s+2\zeta\omega_n}{s^2+2\zeta\omega_n s+\omega_n^2} \cdot \frac{\omega_n}{2\zeta}$$

(9)

Here the nature frequency $\omega_n$ and damping factor $\zeta$ are expressed by (10)

$$\omega_n = \frac{1}{\sqrt{LC}}; \quad \zeta = \left(\frac{R_{eff}}{2}\right) \cdot \sqrt{C/L}$$

(10)

From equation (10) we can conclude 2 interesting points which are useful for our work. First interesting fact, for fixed damping factor the capacitance $C$ is proportionate to inductance $L$ which helps in progressive CMOS method which has lesser gate capacitance then the essential inductance can also be condensed which leads to smaller size in area with more condensed design. Second is that the smaller the damping factors the lesser the $R_{eff}$ which leads to high oscillation frequency.

3.9 An improved performance combined ring VCO:

In this article the combined structure of CMOS inverter and current starved inverter has been proposed to achieve the high oscillation frequency, better stability and small on chip area. The most prominent feature is it provides higher tuning range, less phase noise and reduced area when equated with standard current starved ring VCO. The current steering technique is used to attain great oscillation frequency [8].

As this paper is the combination of both current starved ring oscillation and ring VCO by current steering technique to achieve high frequency. The simulated outputs results of current starving ring oscillator can produce continuous amplitude across the maximum range of frequency band. On contrary the oscillation frequency of an inverter is directly proportionate to power supply but is in reverse proportionate in case of current starved delay cell which effects in less power consumption. Thus, these two inverters exhibit different performance against power supply charging by observing these facts the combined ring oscillator in figure 13 can produce high stable oscillation frequency versus power supply variation.
Figure 12: Proposed combined ring oscillator

The circuit is planned by odd number of inverter stages with the transistor pairs (M5,M6;M7,M8 and M9,M10). The transistor pairs M1,M3 and M2,M4 acts as the current bases which are castoff to provide current to VCO is controlled by M3 essentially the bias current varies the parasitic current of the phases. As the current changes faster the charging and discharging time will increase which results in less delay time[18-20] the proposed circuit has 3 stages which produces 3 delay stages $\tau_1, \tau_2$ and $\tau_3$ and the total delay ($\tau$) will be the summation of all three delays of each stage which results in less sensitivity towards power supply variation. In the modified design the number of transistors are reduced by 4 which obviously represents the efficient area. As all the stages are not connected directly which makes design more efficient. For small signal analysis the condition for oscillation can be obtained as

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = 1$$

(11)

The simulation results of the proposed design depicts various results of swinging frequency and power utilization variations with control voltage. 3GHz of frequency can be achieved at 180nm method at supply voltage 1.8 V, 5.6 GHz are observed at 130nm CMOS technology at supply voltage 1.8V and 7GHz of frequency can be obtained at CMOS 90nm technology at 1.8 V supply voltage.

Table 1. Performance summary and comparison
4. Conclusion:
The review of numerous voltage control ring oscillator (VCRO) has obtained in this paper, and decided that with the progression in technology, there would permanently be the necessity of effective organization strategies with respect to the wanted outcomes, with trade-offs among transistor sizing, frequency, speed, and interruption and power utilization of the circuits. The most important characteristic is the high frequency and low phase noise. The change in supply voltages can vary the oscillation frequency which is implemented by current starved ring oscillator circuits with different biasing techniques can provide controllable oscillation frequency, high tuning range. The VCRO with inductive loading and inductive peeking circuits can provide the low phase noise compared to other circuits. The results that are summarised can show the overall view of the different parameter analysis in order facilitate the respective applications.

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