Parallel Core-Shell Metal-Dielectric-Semiconductor Germanium Nanowires for High Current Surround Gate Field Effect Transistors

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Abstract

Core-shell germanium nanowire (GeNW) is formed with a single-crystalline Ge core and concentric shells of nitride and silicon passivation layer by chemical vapor deposition (CVD), an Al₂O₃ gate dielectric layer by atomic layer deposition (ALD) and an Al metal surround-gate (SG) shell by isotropic magnetron sputter deposition. Surround gate nanowire field effect transistors (FETs) are then constructed using a novel self-aligned fabrication approach. Individual SG GeNW FETs show improved switching over GeNW FETs with planar gate stacks owing to improved electrostatics. FET devices comprised of multiple quasi-aligned SG GeNWs in parallel are also constructed. Collectively, tens of SG GeNWs afford on-currents exceeding 0.1mA at low source-drain bias voltages. The self-aligned surround gate scheme can be generalized to various semiconductor nanowire materials.

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GeNWs have attracted much attention as building blocks for future nanoelectronic components owing to their low temperature synthesis and high bulk mobility. An active area of research has been the continual optimization of FETs based on individual NWs. Such devices are typically fabricated in the plane of a substrate with either a top or bottom gate. It is well known that a surround gate structure, whereby the gate fully wraps around the channel, is optimal for electrostatic control over charge carriers in the channel. Chemically synthesized NWs offer an advantage over top-down lithographically patterned semiconductor wafers for the realization of SG FETs. Vertical SG NW FETs have already been demonstrated using epitaxially grown NWs, although the fabrication generally requires multiple complex steps and high temperatures. Another area of research is the fabrication of FETs with multiple, parallel NWs in each FET in order to reach sufficiently high on-currents to drive practical circuits.

Here, we present SG GeNW FETs based on individual and parallel arrays of core-shell metal-dielectric-semiconductor GeNWs, with on-current exceeding 0.1mA for the latter. The cylindrical GeNW is fully surrounded by a concentric shell of Al$_2$O$_3$ gate dielectric and Al gate metal for optimum electrostatic control of the channel. A self-aligned fabrication process is developed to minimize the un-gated length of NWs and parasitic capacitance. The wrapped around geometry improves on/off ratios and sub-threshold swings of GeNW FETs with planar gate stacks. Our fabrication process is simple and can be generalized to obtain SG FETs of various types of semiconducting NWs, especially for those that are difficult to grow epitaxially on substrates or require low thermal budget processes. For multiple-wire FETs, the use of SG NWs is
advantageous since each wire has its own surrounding gate shells. Electrostatic shielding and interference by neighboring or crossing NWs is avoided or minimized.

GeNWs were synthesized by CVD of GeH₄ at 295°C on Au nanocolloids (20nm in diameter) densely dispersed on SiO₂ substrates.²⁻³ As grown NWs formed a forest and were observed by cross sectional SEM to be standing out of the substrate with most NWs pointing within 30° of the plane normal (Fig. 1a). The wires were in-situ annealed in 10% NH₃ in Ar followed by 1.99% SiH₄ in Ar at 400°C to afford a thin passivation layer of nitride and silicon (Fig.1b, step i, thickness ~ 1.25nm ).¹⁸,¹⁹ Only the first monolayer of Ge is nitrided for low temperature NH₃ annealing below 600°C.²⁰ We then deposited 4 nm of Al₂O₃ conformally around the GeNWs (Fig.1b, step ii) by ALD²¹,²² in a separate reactor at 100 °C using a precursor of trimethyl aluminum (TMA) followed by 15nm of Al by nearly isotropic magnetron sputter deposition (Fig.1b, step iii). The Si overlayer was oxidized by ambient air to form SiOₓ when exposed to air during transferring to the ALD reactor. Due to the nearly free-standing nature of as-grown GeNWs (Fig.1a), isotropic and conformal dielectric ALD, and non-directional metal deposition by sputtering, our process afforded core-shell Al/Al₂O₃/Ge NWs with approximate cylindrical geometry, as confirmed by transmission electron microscopy (TEM, Fig.1b).

The core-shell GeNWs were then sonicated off the substrate in isopropanol alcohol (IPA) to afford a suspension. For fabrication of SG FETs of individual NW, droplets of the suspension were spin-coated onto a Si substrate with 500nm of thermally grown SiO₂. Lithographic patterning was used to open windows in polymethyl methacrylate (PMMA) over source (S) and drain (D) regions (Fig.2a, step i) of a nanowire and define a ~3μm channel length. The Al and Al₂O₃ shells on a GeNW in the opened PMMA windows
were etched for 4 minutes by a dilute solution of 0.01M KOH in 95% H₂O and 5% IPA (Fig.2a, step ii). Since the wet etching is isotropic, the Al and Al₂O₃ on the GeNWs were undercut at the PMMA edges of the opened windows. Directional electron-beam evaporation of 60nm Ti followed by liftoff was used to complete the S/D contacts. A second patterning step was then carried out to contact the outer Al shell of the SG GeNW by a narrow Pt electrode (Fig. 2a, step iii) to complete the gate connection. Lastly, the sample was annealed in forming gas at 300°C for 30 minutes to improve the contacts between the S/D and the GeNW.

The undercutting process during KOH etching of Al and Al₂O₃ shells in the source and drain regions was important to preventing the deposited S/D metal from短路 to the SG metal, and affording self-aligned S/D and SG, with a small gap (~40nm due to undercutting, visible in the inset of Fig. 2c) between the edges of S/D contacts and the surround metal gate shell. The GeNW in the gap remained passivated by SiOₓ due to its low etch rate by dilute KOH (~0.1A/min). The use of Al/Al₂O₃ shells and isotropic KOH etching can be generalized to the fabrication of self-aligned SG FETs for various semiconductor NWs. The relative ease of KOH etching of Al₂O₃ makes Al₂O₃ an advantageous dielectric material for SG NW FETs using our process. Other high κ dielectrics such as HfO₂ and ZrO₂ tend to be more difficult to etch.

The electrical properties of our SG GeNW FETs (Fig.3a) exhibit p-type characteristics (due to light, unintentional p-doping in our growth system) with an on/off current ratio (I_{on}/I_{off}) of ~10⁵ at -0.1V source-drain bias (V_{ds}) and a sub-threshold slope (SS) of 120mV/decade (Fig. 3b). The transconductance (g_{m}) at V_{ds} = -0.1V is 0.33μS. It is known that the GeNW without passivation quickly forms an unstable oxide at the
surface and the Ge/GeO₂ interface has been shown to introduce a high density of surface states.²⁴ Significant hysteresis during a double sweep of the unpassivated GeNW devices is caused by these surface states.²⁵ In contrast, a double sweep of our passivated SG structure shows no appreciable hysteresis (Fig. 3b inset). This suggests that the nitride and silicon passivation layer prevents oxidation of the GeNW surface. In addition, the SS and I_on/I_off are significantly improved over our earlier results obtained with GeNW FETs with planar topgate stacks (see ref. 8 where SS~300mV/decade typically). These indeed suggest better switching characteristics of SG GeNW FETs. Current-gate voltage (I_ds-Vgs) transfer characteristics recorded at various biases up to -1V (Fig. 3b) show similar SS at high V_ds as low biases, further suggesting good electrostatic control over the GeNW channel by the SG. I_ds-V_ds curves at various gate biases (Fig. 3c) show a saturation on-current of ~ 4µA for a typical SG GeNW FET.

We estimated that the hole mobility (µ) in our SG GeNW is ~ 197cm²/Vs, calculated using the square law charge control model²⁶ at low bias g_m:

\[ \mu = \frac{g_m L^2}{V_{ds} C} \]  

where L = 3µm is the channel length and C ~ 1.54fF is the gate capacitance calculated using a 2-D finite element electrostatic simulator (Estat 6.0, Field Precision Software) with geometry and thicknesses identical to our SG GeNWs (Fig. 1b). We used dielectric constants (ε₀) of 1.7 for the SiOₓ layer (~1.25nm thick) and 7.3 for the Al₂O₃ layer (~4nm thick), which were determined by direct capacitance-voltage measurements of planar Ge-SiOₓ-Al₂O₃ stacks.²⁷
Our SG mobility is lower than the best reported mobility in GeNW FETs of 730cm²/Vs and can be attributed to several factors. First, square law model assumes a transparent ohmic S/D contact where the current is not limited by the contact resistance. Our SG GeNW FETs have significant contact resistance due to Ti-Ge Schottky barriers and about 40nm ungated region near the S/D edges. Our contacts are not ohmic without heavy doping of the NWs in the source and drain regions like in a metal-oxide-semiconductor FET (MOSFET). Our work here focuses on developing the SG aspect of nanowire FETs without optimization of other elements such as doping and contacts. Second, the SG GeNW may still have significantly high density of interface states with an amorphous SiOₓ passivation layer. The combination of interface states and small bandgap of Ge may explain the high off-current. The best reported mobility was obtained for GeNW FETs when 1.7nm of crystalline Si was epitaxially grown around a GeNW core. Heteroepitaxially deposited Si could better passivate the GeNWs and minimize interfacial roughness. In addition, the valence band offset of an epitaxially grown crystalline Si shell affords ohmic contacts by shifting the Fermi level in the Ge core below the valence band. Further improved performances and electrostatic control are expected when integrating SG structures into epitaxial Si/Ge NW FETs.

Next, we fabricated GeNW FETs with multiple SG NWs in parallel in each transistor (Fig.4a). GeNWs were deposited onto a Si substrate with 500nm of thermally grown SiO₂ by flowing suspended Al/Al₂O₃/Ge core-shell NWs across the substrate. A stream of N₂ was pointed towards the substrate surface while simultaneously depositing a suspension of SG NWs one drop at a time. The resulting fluid flow across the surface was unidirectional and aligned the GeNWs into approximately parallel arrays. After flow
deposition, the remaining fabrication steps were identical to those of the single connection SG GeNW FET with the exception of wider S/D electrodes (100μm) to afford higher number of connections as shown in Fig. 4b. While most wires lie roughly parallel to each other, variation in the orientation of the wires still resulted in some NWs crossing each other (Fig. 4b inset). SG GeNW FETs with various numbers of wires up to 50 were fabricated this way. The $I_{ds}$-$V_{gs}$ curves of a FET with 35 SG GeNW connections (Fig. 4c) show an $I_{on}/I_{off} \sim 10^4$ for $V_{ds}$ up to -1V and $SS \sim 300mV/\text{decade}$. The on-currents of such devices reach $\sim 110\mu A$ (Fig. 4d) at $V_{ds} = -2V$, consistent with the on-current of individual SG GeNW FETs. Despite of crossing of the wires, the SG scheme prevents shielding effects since each wire has its own gate stack in close proximity with the NW core. This scheme could be extended to fabricate high performance devices with SG NWs packed in three dimensions. In devices we fabricated with top-gated FETs comprised of multiple GeNWs without a surround gate, we found the on/off ratio is generally worse due to occasional crossing, stacking and thus electrostatic screening of wires.

In summary, we have demonstrated fabrication of single and multiple connection SG GeNW FETs. Our method is relatively simple and can be generalized to various semiconductor NWs to form self-aligned SG FETs on various substrates with low thermal budget. SG devices with ohmic contacts and epitaxially deposited Si shell on GeNWs are expected to afford optimum NW FETs in the future. The SG NW concept should enable new type of devices by packing SG NWs densely both in the substrate plane and into a three dimensional stack.

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**Figure Captions**

**Fig.1** Core-shell nanowires. (a) A scanning electron microscopy (SEM) image of GeNWs as-grown on a SiO$_2$ substrate with densely deposited ~20nm Au seed particles. The average diameter of GeNWs synthesized in the current work was ~20nm. (b) Schematic and TEM images of GeNWs after various processing steps: (i) nitride and silicon interlayer passivation by CVD, followed by (ii) atomic layer deposition of ~4nm Al$_2$O$_3$ and then (iii) isotropic sputter deposition of ~15nm Al. These steps led to core-shell Al/Al$_2$O$_3$/Ge nanowires with a thin nitride and Si passivation layer between Al$_2$O$_3$ and Ge.

**Fig.2** Surround gate nanowire transistor with self-aligned source/drain and gate. (a) Schematic cross sectional views of the key fabrication steps: (i) opening of PMMA windows over the source and drain contact areas of a core-shell nanowire; (ii) KOH etching to remove Al and Al$_2$O$_3$ shells in the contact regions (notice undercutting in the outer shells); (iii) directional Ti deposition in source and drain regions, lift-off, followed by patterning of Pt gate electrode for contacting the surround gate. The source/drain are self-aligned with the SG shell and electrically isolated from the gate shell by the undercutting. (b) A schematic top view of the surround gate device. (c) An SEM image of a surround gate device. The surround gate (SG) metal shell is contacted by the Pt gate line (in the middle) and extends to the edges of the S/D electrodes. The inset shows a zoom-in of the drain edge next to which thinning of the SG wire (due to undercutting) is seen. Scale bar in inset is 200 nm.
**Fig.3** Electrical characteristics of a typical SG GeNW FET. (a) A 3-D schematic presentation of the device. (b) Transfer characteristics $I_{ds}$-$V_{gs}$ at various biases. The inset shows a double gate sweep of $I_{ds}$-$V_{gs}$ at $V_{ds} = -0.1V$ without any hysteresis. (c) Current-voltage characteristics $I_{ds}$-$V_{ds}$ at various gate voltages.

**Fig.4** A transistor comprised of multiple surround-gate nanowires in parallel. (a) An idealized schematic presentation of a device. (b) SEM image of a device with $\sim 35$ SG nanowires in parallel. Crossing wires (each with its own gate shell) are seen in the zoomed-in image (scale bar = 1μm). (c) and (d) are transfer and $I_{ds}$-$V_{ds}$ characteristics of the device respectively.
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(a) GeNW (b) GeNW 5 nm Al₂O₃ 50 nm Si Al

(i) (ii) (iii) 2 μm
(a)
(i) PMMA
Al₂O₃
GeNW
Al
SiO₂

(ii)

(iii) S G D

S G D

1 um

(b)

(c)

S G

SG

D

1 um
