On-Chip Error-triggered Learning of Multi-layer Memristive Spiking Neural Networks

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Abstract—Recent breakthroughs in neuromorphic computing show that local forms of gradient descent learning are compatible with Spiking Neural Networks (SNNs) and synaptic plasticity. Although SNNs can be scalably implemented using neuromorphic VLSI, an architecture that can learn using gradient-descent in situ is still missing. In this paper, we propose a local, gradient-based, error-triggered learning algorithm with online ternary weight updates. The proposed algorithm enables online training of multi-layer SNNs with memristive neuromorphic hardware showing a small loss in the performance compared with the state-of-the-art. We also propose a hardware architecture based on memristive crossbar arrays to perform the required vector-matrix multiplications. The necessary peripheral circuitry including presynaptic, post-synaptic and write circuits required for online training, have been designed in the subthreshold regime for power saving with a standard 180 nm CMOS process.

I. INTRODUCTION

The implementation of learning dynamics as synaptic plasticity in neuromorphic hardware can lead to highly efficient, lifelong learning systems [1]–[4]. While gradient Backpropagation (BP) is the workhorse for training nearly all deep neural network architectures, gradients’ computation involves information that is not spatially and temporally local [5]. This non-locality can result in a large area overhead for routing which makes it very expensive to implement in neuromorphic hardware [6]. Recent work addresses this problem using Surrogate Gradient (SG), local learning and an approximate forward-mode differentiation [6]–[8]. SGs define a differentiable surrogate network used to compute weight updates in the presence of non-differentiable spiking non-linearities [7], [9]. Local loss functions enable updates to be made in a spatially local fashion [8]. The approximate forward mode differentiation is a simplified form of Real-Time Recurrent Learning (RTRL) [10] that enables online learning using temporally local information [7]. The result is a learning rule that is both spatially and temporally local, which takes the form of a three-factor synaptic plasticity rule.

The SG approach reveals, from first principles, the mathematical nature of the three factors, enabling thereby a distributed and online learning dynamic.

In this article, we design a hardware architecture, learning circuit and learning dynamics that meet the realities of circuit design and mathematical rigor. Our resulting learning dynamic is an error-triggered variation of gradient-based three factor rules that is suitable for efficient implementation in Resistive Crossbar Arrays (RCAs). Conventional backpropagation schemes require separate training and inference phases which is at odds with learning efficiently on a physical substrate [5]. In the proposed learning dynamic, there is no backpropagation through the main branch of the neural network. Consequently, the learning phase can be naturally interleaved with the inference dynamics and only elicited when a local error is detected. Furthermore, error-triggered learning leads to a smaller number of parameter updates necessary to reach the final performance, which positively impacts the endurance and energy efficiency of the training, by factor up to 88x.

RCAs present an efficient implementation solution for Deep Neural Networks (DNNs) acceleration. The Vector Matrix Multiplication (VMM), which is the cornerstone of DNNs, is performed in one step compared to \(O(N^2)\) steps for digital realizations where \(N\) is the vector dimension. A surge of efforts focused on using RCAs for Artificial Neural Networks (ANNs) such as [11]–[14] but comparatively few work utilize RCAs for spiking neural networks trained with gradient-based methods [7], [9], [15]. Thanks to the versatility of our proposed algorithm, RCAs can be fully utilized with suitable peripheral circuits. We show that the proposed learning dynamic is particularly well suited for the RCA-based design and performs near or at deep learning proficiencies with a tunable accuracy-energy trade-off during learning.

A. State-of-the-art and Related Work

Learning in neuromorphic hardware can be performed as off-chip learning, or using a hardware-in-the-loop training, where a separate processor computes weight updates based on analog or digital states [4], [16]. While these approaches lead to performance that is on par with conventional deep neural networks [17], [18], they do not address the problem of learning scalably and online.

In a physical implementation of learning, the information for computing weight updates must be available at the synapse. One approach is to convey this information to the neuron and synapses. However, this approach comes at a significant cost in wiring, silicon area, and power. For an efficient implementation of on-chip learning, it is necessary to design an architecture that naturally incorporates the local information at the neuron and the synapses. For example, Hebbian learning or its spiking counterpart Spike Time Dependent Plasticity
and a circuit implementation. This paper significantly extends
the data between the memory and the processing units.
Neumann bottleneck and is thus power hungry due to shuttling
use high precision processors and a separate memory block. In
Although effective for inference stages, the learning dynamics
is enabled by three embedded x86 processor cores, and Arm
consumption. For example, Loihi and Spinnakers’s flexibility
This is achieved at the cost of more power and chip area
substrate that can implement a vast set of learning algorithms.

In this work, we target the general multi-layer learning prob-
le by taking into account the neural dynamics and multiple
layers. Currently, Intel Loihi research chip, Spinnaker 1 and
2, and the Brainscales-2 have the ability to implement a vast
variety of learning rules [1], [29], [30]. Spinnaker and Loihi
are both research tools that provide a flexible programmable
substrate that can implement a vast set of learning algorithms.
This is achieved at the cost of more power and chip area
consumption. For example, Loihi and Spinnakers’s flexibility
is enabled by three embedded x86 processor cores, and Arm
cores, respectively. The plasticity processing unit used in
Brainscales-2 is a general-purpose processor for computing
weight updates based on neural states and extrinsic signals.
Although effective for inference stages, the learning dynamics
do not break free from the conventional computing methods or
use high precision processors and a separate memory block. In
addition to requiring large amounts of memory to implement
the learning, such implementations are limited by the von-
Neumann bottleneck and is thus power hungry due to shuttling
the data between the memory and the processing units.

In [31], we presented the concept of error-triggered learning and
a circuit implementation. This paper significantly extends
the theory, system architecture and circuits of that work to
improve scalability, area and power. The contributions of this
paper are summarized as follows:

- We extend the error-triggered learning algorithm to make
the learning fully ternary to suit the targeted memristor-
based RCA hardware.
- We propose a complete and novel hardware architecture
that enables asynchronous error-triggered updates according
to the algorithm.
- We propose an implementation of the neuromorphic core, including
memristive crossbar peripheral circuits, update
circuitry, pre-and post-synaptic circuits.

This paper is organized as follows: Sec. II introduces the
error-triggered learning algorithm. Sec. III discusses large
scale simulation experiments performed using PyTorch [32].
The hardware architecture is presented in Sec. IV. Then,
the implementation of the inference and training circuits are
presented in Sec. V and results of circuit simulations using
Cadence Spectre are reported. Sec. VI discusses the limitation
and potential of the proposed hardware and algorithm. Finally,
the conclusion and future works are given.

II. ERROR-TRIGGERED LEARNING ALGORITHM

A. Neural Network Model

The proposed model consists of networks of plastic
integrate-and-fire neurons.

Here, the models are formalized in discrete-time to make
the equivalence with classical artificial neural networks more
explicit. However, these dynamics can also be written in
continuous-time without any conceptual changes. The neuron
and synapse dynamics written in vector form are:

\[ U^l[t] = W^l P^l[t] - \delta R^l[t], \quad S^l[t] = \Theta(U^l[t]) \quad (1) \]
\[ P^l[t + 1] = \alpha^l P^l[t] + Q^l[t], \]
\[ Q^l[t + 1] = \beta^l Q^l[t] + S^{l-1}[t], \]
\[ R^l[t + 1] = \gamma^l R^l[t] + S^l[t]. \]

where \( U^l[t] \in \mathbb{R}^{N^l}, \quad l \in [1, L] \) is the membrane potential of
\( N^l \) neurons at layer \( l \) at time step \( t \), \( W^l \) is the synaptic
weight matrix between layer \( l - 1 \) and \( l \), and \( S^l \) is the binary
output of this neuron. \( \Theta \) is the step function acting as a spiking
activation function, i.e. \( \Theta(x) = 1 \) if \( x \geq 0 \), and \( \Theta(x) = 0 \)
otherwise. The terms \( \alpha^l, \gamma^l, \beta^l \in \mathbb{R}^{N^l} \) capture the decay
dynamics of the membrane potential, the synapse and the
refractory state \( R^l \), respectively. States \( P^l \) describe the post-
synaptic potential in response to input events \( S^{l-1} \). States \( Q^l \)
can be interpreted as the synaptic dynamic state. The decay
terms are written in vector form, meaning that every neuron
is allowed to have a different leak. It is important to take
variations of the leak across neurons into account because
fabrication mismatch in subthreshold implementations may
lead to substantial variability in these parameters [33].

\( R \) is a refractory state that inhibits the neuron after it has
emitted a spike, and \( \delta \in \mathbb{R} \) is the constant that controls its
magnitude. Note that Eq. (1) is equivalent to a discrete-time
version of a type of Leaky Integrate & Fire (LIF) [3]
and the Spike Response Model (SRM) with linear filters [34].

The same dynamics can be written for recurrent spiking
neural networks, whereby the same layer feeds into itself, by
adding another connectivity matrix to each layer to account
for the additional connections. This SNN and the ensuing
learning dynamics can also be transformed into a standard
binary neural network by setting all decay terms and \( \delta \) to 0,
which is equivalent to replacing all \( P \) with \( S \) and dropping \( R \)
and \( Q \).

B. Surrogate Gradient Learning

Assuming a global cost function \( L[t] \) defined for the time
step \( t \), the gradients with respect to the weights in layer \( l \)
are formulated as three factors

\[ \nabla_{W^l} L[t] = \frac{\partial L}{\partial S^l} \frac{\partial S^l}{\partial U^l} \frac{dU^l}{dW^l} \]  

where we have used \( \frac{d}{dt} \) to indicate a total derivative,
because the differentiated state may indirectly depend on the
differentiated parameter \( W \), and dropped the notation of the
time \([t] \) for clarity. The rightmost factor describes the change
of the membrane potential changes with the weight \( W^l \). This
term can be computed as \( P^l[t] - \delta \frac{dR^l[t]}{dt} \) for the neuron defined
by Eq. (1). Note that, as in all neural network calculus, this
term is a sparse, rank-3 tensor. However, for clarity and the
ensuing simplifications, we write it here as a vector. The term
with \( R \) involves a dependence of the past spiking activity of
the neuron, which significantly increases the complexity of
the learning dynamics. Fortunately, this dependence can be ignored during learning without empirical loss in performance [9]. The middle factor is the change in spiking state as a function of the membrane potential, i.e. the derivative of $\Theta$. $\Theta$ is non-differentiable but can be replaced by a surrogate function such as a smooth sigmoidal or piecewise constant function [7]. Our experiments make use of a piecewise linear function, such that this middle factor becomes the box function [7]. Our experiments make use of a piecewise linear function, such that this middle factor becomes the box function [7]. Our experiments make use of a piecewise linear function, such that this middle factor becomes the box function [7]. Our experiments make use of a piecewise linear function, such that this middle factor becomes the box function [7]. Our experiments make use of a piecewise linear function, such that this middle factor becomes the box function [7]. Our experiments make use of a piecewise linear function, such that this middle factor becomes the box function [7]. Our experiments make use of a piecewise linear function, such that this middle factor becomes the box function [7]. Our experiments make use of a piecewise linear function, such that this middle factor becomes the box function [7]. Our experiments make use of a piecewise linear function, such that this middle factor becomes the box function [7].

We define then $B^l$ as the diagonal matrix with elements $B(U^l_i) = 1$ if $u_- < U^l_i < u_+$ and 0 otherwise. We make. Using this encoding, the parameter update rule written

\[ \Delta W^l = -\eta \nabla_{W^l} L = -\eta (\text{error}^l B^l)^T P^l, \]

in scalar form becomes:

\[ \Delta w^l_{ij} = -\eta \text{error}^l_{ij} P^l, \text{ if } u_- < U^l_i < u_+, \]

where $\eta$ is the learning rate.

C. Error-triggered Learning

By virtue of the chain rule of calculus, Eq. (2) reveals that the derivative of loss function in a neural network (the first term of the equation, $\frac{\partial \mathcal{L}}{\partial S^l}$) depends solely on the output state $S$. The output state is a binary vector with $N^l$, and can naturally be communicated across a chip using event-based communication techniques with minimal overhead. The computed errors ($\frac{\partial C}{\partial S^l}$) are vectors of the same dimension, but are generally reals, i.e. defined in $\mathbb{R}^{N^l}$. For in situ learning, and as previously discussed, the error vector must be available at the neuron. To make this communication efficient, we introduce a tunable threshold on the errors and encoded them using positive and negative events as follows:

\[ E^l_i = \text{sign}(\text{error}^l_i)(|\text{error}^l_i| \div \theta^l), \]

where $\theta^l \in \mathbb{R}$ is a constant or slowly varying error threshold unique to each layer $l$ and $\div$ is an integer division. Fig. 3 illustrates this function. Note that in the formulation above, $E_i$ can exceed -1 and 1. In this case, multiple updates are made. Using this encoding, the parameter update rule written in scalar form becomes:

\[ \Delta w^l_{ij} = -\tilde{\eta} E^l_i B(U^l_i) P^l_{ij}, \]

where $\tilde{\eta} = \eta \theta$ is the new learning rate that subsumes the value of $\theta$. Thus, an update takes place on an error of magnitude $\tilde{\eta}$ and its magnitude $\tilde{\eta} P^l_{ij}$. Provided that the layer-wide update magnitude can be modulated proportionally to $\tilde{\eta}$, this learning rule implies two comparisons and an addition (subtraction).

D. Approximate gradient estimation

When implementing the rule in memristor crossbar arrays, using analog values for $P$ would require coding its value as a number of pulses, which would require extra hardware. In order to avoid sampling the $P$ signal and simplify the implementation, we further discretize $P$ value to a binary signal by thresholding (using a simple comparator):

\[ \frac{dU^l}{dW^l} = \tilde{P}, \text{ with } \tilde{P} = \Theta(P - \bar{P}) \]

where $c$ and $\bar{P}$ are constants, and $\tilde{P}$ is the binarized $P$. This comparator is only activated upon weight updates and the analog value is otherwise used in the forward path. Since $\tilde{P} \in \{0, 1\}$, the constant $c$ can be subsumed in the learning rate $\tilde{\eta}$ and the parameter update becomes ternary $\Delta W^l_{ij} \in \{-\tilde{\eta}, 0, \tilde{\eta}\}$. The full implementation of the encoder and CMOS sampler circuits are discussed in [31].

Algorithm 1: Error-triggered Learning Algorithm for layer $l$

Require: a minibatch of inputs and targets $(S^{in}, Y)$, previous weights $W$, previous $\theta$, and previous learning rate $\eta$

Ensure: updated weights $W$, updated parameter $\theta$.

1. Forward propagation:

\[ Q = \beta Q + S^{in} \]

\[ P = \alpha P + Q \]

\[ U \leftarrow WP - \delta R \]

\[ S \leftarrow \Theta(U) \]

2. Gradient Computation:

\[ \mathcal{L} = \text{Loss}(S, Y) \]

\[ err \leftarrow \frac{\partial C}{\partial S} = B(U) \frac{\partial C}{\partial Y} \]

for $i = 1$ do

\[ E_i = -\text{sign}(\text{error}_i)(|\text{error}_i| \div \theta) \]

> Error triggered

if $E_i \neq 0$ then

if $B(U_i) \neq 0$ then

for $j = 1$ do

if $P \geq \bar{P}$ then

$W_{ij} \leftarrow W_{ij} + \tilde{\eta}E_i$

end if

end for

end if

if $\bar{P} > P$ then

$W_{ij} \leftarrow W_{ij} - \tilde{\eta}E_i$

end if

$\theta \leftarrow \text{Update}(\theta, E)$

end for

Figure 1: Illustration of the error discretization used for error-triggered learning. $E$ here is the error magnitude as a function of the real valued error $err$. Not that although the magnitude of $E$ can be larger than 1, these events are 1) rare after a few learning iterations and 2) represented as multiple ternary events.
E. Separation of Learning as Extrinsic and Intrinsic Factors

Up to now, we have side-stepped the calculation of $\text{err}[n]^l$. As discussed earlier, the factorization of the learning rule in three terms enables a natural distribution of the learning dynamics. The factor $E_i^l$ can be computed extrinsically, outside of the crossbar, and communicated via binary events (respectively corresponding to $E = -1$ or $E = 1$) to the neurons. A high-level architecture of the design is shown in Fig. 6.

The computations of $E_i^l$ can be performed as part of another spiking neural network, or on a general-purpose processor (see PC and NC in Sec. IV). In this article, we are agnostic to the implementation of this computation, provided that the error $E_i^l$ is projected back to neuron $i$ in one time step and that it can be calculated using $S_i^l$. Below, we describe an example of how these extrinsic errors can be computed.

a) Deep Local Losses: If $l < L$, meaning it is not the output layer, then computing $E_i^l$ requires solving a deep credit assignment problem. Gradient BP can solve this, but is not compatible with a physical implementation of the neural network [5], [35], and is extremely memory intensive in the presence of temporal dynamics [36]. Several approximations have emerged recently to solve this, such as feedback alignment [37], [38], and local losses defined for each layer [8], [40], [41]. For classification, examples of local losses are layer-wise classifiers (using output labels) [40] and supervised clustering, which can perform on par with BP in classical ML benchmark tasks [41]. For simplicity, in this article we use a layer-wise local classifier using a mean-squared error loss defined as $L_i^l = ||\sum_{k=1}^C (J_{ik}^l - \hat{Y}_k)||_2$, where $J_{ik}^l$ is a random, fixed matrix, $\hat{Y}_k$ are one-hot encoded labels, and $C$ is the number of classes. The gradients of $L_i^l$ involve backpropagation within the time step $t$ and thus requires the symmetric transpose, $J_{ik}^l$. If this symmetric transpose is unavailable, then $L$ can be optimized directly. To account for the case where $J_{ik}^l$ is unavailable, for example in mixed signal systems, we train through feedback alignment using another random matrix $H^l$ [37] whose elements are equal to $H_{ij}^l = J_{ij}^{l,T} \omega_{ij}^l$ with Gaussian distributed $\omega_{ij}^l \sim N(1, \frac{1}{2})$, where $T$ indicates transpose. This strategy was also used in our previous work [8].

Using this strategy, the error can be computed with any loss function (e.g. mean-squared error or cross entropy) provided there is no temporal dependency, i.e. $L[i]$ does not depend directly on variables in time step $t - 1$ [6]. If such temporal dependencies exist, for example with Van Rossum spike distance, the complexity of the learning rule increases by a factor equal to the number of post-synaptic neurons [9]. This increase in complexity would significantly complicate the design of the hardware. Consequently, our approach does not include temporal dependencies in the loss function.

The matrices $J^l$ and $H^l$ can be very large, especially in the case of convolutional networks. Because these matrices are not trained and are random, there is considerable flexibility in implementing them efficiently. One solution to the memory footprint of these matrices is to generate them on the fly, for example using a random number generator or a hash function. Another solution is to define $J^l$ as a sparse, binary matrix [5]. Using a binary matrix would further reduce the computations required to evaluate $\text{err}$.

The resulting learning dynamics imply no backpropagation through the main branch of the network. Instead, each layer learns individually. It is partly thanks to the local learning property that updates to the network can be made in a continual fashion, without artificial separation in learning and inference phases [8].

III. LARGE SCALE EXPERIMENTS

An important feature of the error-triggered learning rule is its scalability to multi-layer networks with small and graceful loss of performance compared to standard deep learning. To demonstrate this experimentally, we simulate the learning dynamics for classification in large-scale, multi-layer spiking networks on a GPU. The GPU simulations focus on event-based datasets acquired using a neuromorphic sensor, namely the N-MNIST and DVS Gestures dataset for demonstrating the learning model. Both datasets were pre-processed as in [8]. The N-MNIST network is fully connected (1000–1000–1000), while the DVS Gestures network is convolutional (64c7-128c7-128c7). In our simulations, all computations, parameters and states are computed and stored using full precision. However, according to the error-triggered learning rule, errors are quantized and encoded into a spike count. Note that in the case of box-shaped synaptic traces, and up to a global learning rate factor $\eta$, weight updates are ternary (-1,0,1) and can in principle, be stored efficiently using a fixed point format. For practical reasons, the neural networks were trained in mini-batches of 72 (DVS Gestures) and 100 (N-MNIST). We note that the choice of using mini-batches is advantageous when using GPUs to simulate the dynamics and is not specific to Eq. 4.

Our model’s parameters are similar to previous work [8], except that the time constants were randomized. The error rate, denoted $|E[t]| / 1000$, is the number of non-zero values for $E[i]$ during one second of simulated time. The
rate can be controlled using the parameter $\theta$. While several policies can be explored for controlling $\theta$ and thus $|E|$,[42], our experiments used a proportional controller with set point $\bar{E}$ to adjust $\theta$ such as the error rate per simulated second during one batch, denoted $\langle|E(t)|\rangle$, remains near $\bar{E}$. After every batch, $\theta$ was adjusted as follows:

$$\theta[t + 1] = \theta[t] + \sigma(\bar{E} - \langle|E(t)|\rangle).$$

where $\sigma$ is the controller constant and is set to $5 \times 10^{-7}$ in our experiments. Thus, the proportional controller increases the value of $\theta$ when the error rate is too large, and vice versa.

The results shown in Tab. 4 demonstrate a small loss in accuracy across the two tasks when updates are error-triggered using $\bar{E} = .05$, and a more significant loss when using $\bar{E} = .01$. Published work on DVS Gestures with spiking neurons trained with backpropagation achieved 5.41% [42], 6.36% [15], and 4.46% [8] error rates and 1.3% [43] for N-MNIST with fully connected networks. We emphasize here that the N-MNIST results are obtained using a multi-layer perceptron as opposed to a convolutional neural network. Spiking convolutional neural networks are capable of achieving lower errors on N-MNIST [8, 44].

The results show final errors in the case of exact and approximate computations of $\frac{\partial U}{\partial W}$. Using the approximation $\tilde{P}$ instead of $\frac{\partial U}{\partial W}$ incurs an increase in error in all cases. This is because the gradients become biased. Several approaches could be pursued to reduce this loss: 1) using stochastic computing and 2) multi-level discretization of $\frac{\partial U}{\partial W}$. A third conceivable option is to change the definition of $P$ in the neural dynamics such that it is also thresholded, so as to match $\tilde{P}$. However, this approach yielded poor results because $P$ became insensitive to the inputs beyond the last spike.

Fig. 3 illustrates the signals used to compute $\Delta W_{ij}^l$ in the case of one N-MNIST data sample, at the beginning, middle and end of learning. There are many updates to the synaptic weights at the beginning of the learning, and several steps where $|err| > 1$. However, the number of updates regress quickly after a few epochs. The initial surge of updates is due to 1) a large error in early learning and 2) a suboptimal choice of $\theta_0$, the initial value of $\theta$. The latter could be optimized for
each dataset to mitigate the initial surge of updates.

It is conceivable that the role of event-triggered learning is merely to slow down learning compared to the continuous case. To demonstrate that this is not the case, we show task accuracy vs. the number of updates \( \langle |E| \rangle \) relative to the continuously learning case in Fig. 4. These curves indicate that values of \( E < 1 \) indeed reduce the number of parameters updates to reach a given accuracy on the task compared to the continuous case. Even the case \( E = .05 \) leads to a drastic reduction in the number of updates with a reasonably small loss in accuracy. However, a too low error event rate, here \( E = .01 \) can result in poorer learning compared to \( E = .05 \) along both axes (e.g. Fig. 4, bottom right, \( E = .01 \)). This is especially the case when the approximate traces \( \hat{P} \) are used during learning. This implies the existence of an optimal trade-off for \( E \) that maximizes accuracy vs. the error rate.

The weight updates are achieved through stochastic gradient descent (SGD). We note that SGD refers to how gradients are applied to the parameters, which is different from how the gradients are estimated. In this sense, SGD is consistent with the fact that errors are not backpropagated through the multiple layers of the network. We used here SGD because other optimizers with adaptive learning rates (such as ADAM) with momentum involve further computations and states that would incur an additional overhead in a hardware implementation. To take advantage of the GPU parallelization, batch sizes were set to 72 (DVS Gestures) and 200 (N-MNIST). Although, batch sizes larger than 1 are not possible locally on a physical substrate, training with batch size 1 is just as effective as using batches [45]. Our earlier work demonstrated that training with batch size 1 in SNNs is indeed effective [38], [46], but cannot take advantage of GPU accelerations.

IV. HARDWARE ARCHITECTURE

In this section, we discuss the general hardware architecture that supports the error-triggered learning, which comprises Neuromorphic Cores (NCs) and Processing Cores (PCs) as depicted in Fig. 5. The NCs are responsible for implementing the neuron, synapse dynamics Eq. (1), and the estimation of \( \delta s \). Each core additionally contains circuits that are needed for implementing training provided the error signals. The error signals are calculated on the PCs and communicated asynchronously to the NCs.

The separation in PC and NC is directly motivated by the separation of Eq. (6) in extrinsic and intrinsic factors as follows:

\[
\Delta W_{ij} \propto \frac{E_i}{U_i} B(U_i^{l}) P_j^{l}.
\]

This separation results in an elegant, and largely local estimation of the gradients since \( P_j^{l} \) above is already available in the neural dynamics, and \( B(U_i^{l}) \) is simply a thresholded copy of \( U_i^{l} \). Thus, the NC contributes to inference and gradient estimation, whereas the estimation of the error \( E_i \) is carried out in the PC and communicated to the NC. The ternary nature of the error further reduces the overhead of communicating these errors across the two types of cores.

A. Processing Core

In addition to data and control buses, the PC consists of four main blocks, namely for error calculation, error encoding, arbitration, and handshaking. The PC can be shared among several NCs, where communication across the two types of cores is mediated using the same address event routing conventions as the NCs.

The error calculation block is responsible for calculating the gradients and the continuous-value of the error updates (i.e., \( err^t \) signals). The PC also compares the error signal \( err \) with the threshold \( \theta \) as discussed in (5) and (6) to generate integer \( E \) signals that are sent to error encoder. A natural approach to implement this block is by using general-purpose Central Processing Unit (CPU) in addition to a shared memory which is similar to the Lakemont processors on the Intel Loihi research processor [1]. CPUs offer high speed, high flexibility, and programming ability that is generally desirable when calculating loss functions and their gradients. The shared memory can be used to store the spike events while calculating a different layer error.

The calculated error update signals \( E \) are rate-encoded in the error encoder into two spike trains \( E \to \{ \delta_u, \delta_s \} \) where \( \delta_u \) is the update signal and \( \delta_s \) is the polarity of the update.

The arbiter is used to choose only one NC to update at time. This choice can be based on different policies, for instance, least frequently updated or equal policy. Once the \( \{ \delta_u, \delta_s \} \) signals are generated, they need to be communicated to the corresponding NC.

For this communication, a handshaking block is required. The generated error events send a request to the PC arbiter, which acknowledges one of them (usually based on the arrival times). The address of the acknowledged event along with a request is communicated to the NC core in a packet. The handshake block at the NC ensures that the row whose
address matches the packet receives the event and takes control over the array. This block then sends back an acknowledge to the PC as soon as the learning is over. The communication bus is then freed up and is made available for the next events.

An alternative to implementing the PC is to use another NC, as it is a SNN that can be naturally configured to implement the necessary blocks for communication and error encoding. General-purpose functions can be computed in SNNs, for example, by using the neural engineering framework [47]. In this case, the system could consist solely of NCs. The homogeneity afforded by this alternative may prove desirable for specific technologies and designs.

B. Neuromorphic Core

Emerging technologies, such as Resistive RAM (RRAMs), Phase Change Memories (PCMs), Spin Transfer Torque RAMs (STT-RAMs), and other MOS realizations such as floating gate transistors, assembled as an RCA enable the VMM operation to be completed in a single step [48]. This is unlike general-purpose processors that require $N \times M$ steps where $N$ and $M$ are the weight matrix’s size. Recently, there has been impressive development in maturing the technology and large array sizes for PCM and OxRAMs have already been reported [49], [50]. These emerging technologies implement only positive weight (excitatory connections). However, to fully represent the neural computations, negative weights (inhibitory connections) are also necessary. There are two ways to realize the positive and negative weights [51]. 1) Balanced realization where two devices are needed to implement the weight value stored in the devices conductances where $W = G^+ - G^-$. If the $G^+$ is greater/less than $G^-$, it represents positive/negative weight, respectively. 2) Unbalanced realization where one device is used to implement the weight value with a common reference conductance $G_{ref}$, set to the mid-value of the conductance range. Thus, the weight value is represented as $W = G - G_{ref}$. If the $G$ is greater/less than $G_{ref}$, it represents a positive/negative weight, respectively. In this work, we use an unbalanced realization since it saves area and power at the expense of using half of the device’s dynamic range. Thus, the memristive SNN can be written as:

$$U_i^t[t] = \sum_j (G_{ij} - G_{ref}) P_j^t[t] - \delta R_i[t]. \quad (7)$$

By following the same analysis in section III-A, the dynamics are the same as Eq. 4. NCs implement the presynaptic potential circuits that simulate the temporal dynamics of $P$ in Eq. 4. In addition, the NC implements the memristor write circuitry which potentiate or depress the memristor with a sequence of pulses depending on the error signal that is calculated in the PC. The NC continuously works in the inference mode until it enters the learning mode by receiving an error event from the PC.

The circuit then deactivates all rows except the row where the error event belongs to.

The memristors within this row are then updated by a positive or negative pulse based on the $\tilde{P}$ value, which would potentiate or depress the device by $\pm \Delta G$ as shown in Tab. 11. Thus, the control signals can be written as follows:

$$UP_j = \delta_s \tilde{P}_j \quad DN_j = \delta_u \tilde{P}_j $$

$$lrn_i = B_i \delta_u \quad LRN = \sum_i lrn_i$$

where $LRN$ is the mode signal which determine the mode of the operation either inference ($LRN = 0$) or weight update mode ($LRN = 1$). The update mode is chosen if any of the $lrn$ signals is turned ON. The full details of the neuromorphic core is discussed in Sec. V.

It is worth to mention that we considered local learning where each layer learns individually. As a result, there is no backpropagation as known in the conventional sense. The loss gradient calculations are performed in the processing core with floating point precision to calculate the error signals. These are then quantized and serially encoded into ternary pulse stream to program the memristors. Strategies for reduced precision learning (e.g. stochastic rounding) are compatible with error triggered learning [52].

C. Network On Chip

The neuromorphic and processing cores are linked together with a Network on Chip (NoC) that organizes the communication among them based on the widely used Address Event Representation (AER) scheme [53], [54]. Different routing techniques have been proposed to trade off between flexibility (i.e., degree of configurability) and expandability [55]. For instance, TrueNorth and Loihi chips use 2D mesh NoC [1], [56]. SpiNNiker uses torus NoC [57] and HiAER uses tree NoC.
Assuming that the maximum firing rate of the neuron is $f_{\text{max}}$, a condition on maximum error frequency can be derived as

$$f_{\text{err max}} < \frac{1}{10N f_{\text{max}} T_p}$$

This shows a trade off between the fan-out per NC and the maximum error frequency. If we considered $T_p = 100\,\text{ns}$ and $f_{\text{max}} = 100\,\text{Hz}$, the maximum error frequency under this definition is $78\,\text{Hz}$ for $N = 128$ (a typical size of the current fabricated RCA) and $10\,\text{Hz}$ for $N = 10^3$. As previously evaluated in Sec. III the higher the error frequency, the better the performance. The hardware would set the upper limit for the error frequency to $10\,\text{Hz}$ for $N = 10^3$, which causes $2.68\%$ and $4.22\%$ drop in the performance. Depending on the distribution of the spike trains from the error calculation block, this constraint can be further loosened. While a buffer can also be added to the PC to queue the error events which are blocked as a result of the busy communication bus, this translates to more memory and hence area on the PC and lead to biased gradients.

**Input frequency:** A similar analysis can be done to calculate the maximum input dimension of the array. Assuming there is no structure in the incoming input (or that the structure is not available a priori), a Poisson statistic can be considered for the input spikes. In that case, the probability of the next spike in any of the $M$ inputs occurring within the pulse width of the write pulse $T_p$ is equal to $P(\text{Event}) = 1 - e^{-M f_{\text{in}} T_p}$ where $f_{\text{in}}$ is the frequency of the input spikes. To keep this probability low (e.g., $< 0.01$), the fan-in can be calculated. Considering a biologically plausible maximum rate of $f_{\text{in}} = 100\,\text{Hz}$, in the worst case where all input neurons fire and for $T_p = 100\,\text{ns}$, the maximum $M$ would be 1000. The SNN test benches, such as DVSGesture and N-MINeST that have been discussed in [11-B] have peak event rates around 30 Hz and 15 Hz [43] respectively which would triple the fan-in of the NC.

**Number of NCs per PC:** Assuming that the PC runs at frequency $f_{\text{clk}}$, and it takes $2N/f_{\text{clk}}$ on average to calculate the error signals (which can be $2/f_{\text{clk}}$ in the case of a RCA or $2N^2/f_{\text{clk}}$ in case of a von-Neumann architecture). The factor 2 is added for $J$ and $H$ multiplications in addition to loss calculation evaluation time $T_l$. Thus, the total error calculation per NC takes $T_{pc} = 2N/f_{\text{clk}} + T_l$. Updates have to be performed faster than the time constant for computing the gradient. Thus, the maximum number of NCs is $N = T_{pc}/T_{u_{\text{max}}}$. For example, for $f_{\text{clk}} = 500\,\text{MHz}$ and $N = 1000$ and $T_{u_{\text{max}}} = 1\,\text{ms}$, 4000 NCs can be used per RCA-based PC on average and 4 NCs for von-Neumann-based PC. It is worth noting that handshaking, arbiter and the error encoder are operating in parallel with the error calculations and thus we did not include them in the estimation.

**V. NEUROMORPHIC CORE IMPLEMENTATION**

In this section, we will first introduce the neuromorphic learning architecture compatible with a $1T - 1R$ RCA, and the signal flow from the input events to the learning core. We will then detail the circuits that implement the building blocks of the architecture.

**A. Learning Architecture**

**a) Overall information flow:** Our SNN circuit implementation differs from classical ones used in mixed-signal neuromorphic chips [59]. Generally, the rows of crossbar arrays are driven by spikes and integration takes place at each column [24], [60]–[62]. While this is beneficial in reducing read power, it renders learning more difficult because the variables necessary for learning in SNNs are not local to the crossbar. Instead, we use the crossbar as a VMM of pre-synaptic trace vectors $P^l$ and synaptic weight matrices $W^l$. Using this strategy, the same trace $P^l$ per neuron supports both inference and learning. This property has the distinctive advantage for learning in that it is immune to the mismatch in $P^l$, and can even exploit this variation. AER is the conventional scheme for communication between neuronal cores in many neuromorphic chips [33]. Fig. [6] depicts the details of the neuromorphic learning architecture as a crossbar compatible with the AER. The information flows from the AER at the input columns to the integrators, then to the VMM and finally to the spike generator block which sends the output spikes to the row AER. Through the row AER, information then flows to the PC to calculate the error, which in turn sends error events back to the VMM to change the synaptic weights.

**b) Details of the architecture:** Pre-synaptic events communicated via AER are integrated in the $Q$ blocks, which are then integrated in $P$ blocks as shown in Fig. [6]. This doubly integrated signal then drives the RCA during inference mode. The RCA model used here is a $1T - 1R$ array of memristive devices with the gate and source of the transistor being driven by the WL and BL respectively and the bottom electrode of the device being driven by the SL. The voltages driving the WL, BL and SL are $\text{MUX}$-ed at the periphery to drive the array with the appropriate voltages depending on the inference or learning mode. It is worth noting that in our simulations, we did not use a specific model for the devices. Any type of device whose conductance can be changed with a voltage

| $\eta E$ | $\delta u$ | $\delta x$ | $B$ | $\hat{P}$ | $W$ | LRN | UP | DN |
|---------|-----------|-----------|-----|-----------|-----|------|-----|-----|
| 0 ×     | ×         | ×         | 0   | 0         | 0   | 0    | 0   | 0   |
| 1 ×     | 0         | ×         | 0   | 0         | 0   | 0    | 0   | 0   |
| 1 ×     | ×         | 0         | 0   | 0         | 0   | 0    | 0   | 0   |
| 1 0 1   | 1         | +ΔG      | 1   | 1         | 1   | 0    | 1   | 0   |
| 1 1 1   | 1         | −ΔG      | 1   | 1         | 0   | 0    | 1   | 1   |

**Table II: Truth table of the error-triggered ternary update rule.** Signals $B$, and $P$ are local to the NC, while signals $E$, LRN, UP and DN are local to the PC.

[55] HiAER offers high flexibility and expandability, which can be used in the proposed architecture for communication among neuromorphic cores during inference and between the processing core and neuromorphic cores during training.

**D. Hardware Limits**

Error frequency: A full update cycle of the NC is $T_{u_{\text{max}}} = N \times f_{\text{err max}} \times T_p$ where $N$ is the fan-out per NC, $f_{\text{err max}}$ is the maximum error frequency and $T_p$ is the width of the memristor update period. $T_{u_{\text{max}}}$ should be much smaller than the inter-spike interval (i.e. factor of 10 will be sufficient). Assuming that the maximum firing rate of the neuron is $f_{\text{max}}$, a condition on maximum error frequency can be derived as

$$f_{\text{err max}} < \frac{1}{10N f_{\text{max}} T_p}$$

This shows a trade off between the fan-out per NC and the maximum error frequency. If we considered $T_p = 100\,\text{ns}$ and $f_{\text{max}} = 100\,\text{Hz}$, the maximum error frequency under this definition is $78\,\text{Hz}$ for $N = 128$ (a typical size of the current fabricated RCA) and $10\,\text{Hz}$ for $N = 10^3$. As previously evaluated in Sec. III the higher the error frequency, the better the performance. The hardware would set the upper limit for the error frequency to $10\,\text{Hz}$ for $N = 10^3$, which causes $2.68\%$ and $4.22\%$ drop in the performance. Depending on the distribution of the spike trains from the error calculation block, this constraint can be further loosened. While a buffer can also be added to the PC to queue the error events which are blocked as a result of the busy communication bus, this translates to more memory and hence area on the PC and lead to biased gradients.

Input frequency: A similar analysis can be done to calculate the maximum input dimension of the array. Assuming there is no structure in the incoming input (or that the structure is not available a priori), a Poisson statistic can be considered for the input spikes. In that case, the probability of the next spike in any of the $M$ inputs occurring within the pulse width of the write pulse $T_p$ is equal to $P(\text{Event}) = 1 - e^{-M f_{\text{in}} T_p}$ where $f_{\text{in}}$ is the frequency of the input spikes. To keep this probability low (e.g., $< 0.01$), the fan-in can be calculated. Considering a biologically plausible maximum rate of $f_{\text{in}} = 100\,\text{Hz}$, in the worst case where all input neurons fire and for $T_p = 100\,\text{ns}$, the maximum $M$ would be 1000. The SNN test benches, such as DVSGesture and N-MINeST that have been discussed in [11-B] have peak event rates around 30 Hz and 15 Hz [43] respectively which would triple the fan-in of the NC.
Figure 6: Details of the neuromorphic learning architecture compatible with the AER communication scheme. The event integrators, VMM array, switches, front end, neural circuits, and Error calculation block are highlighted in green, yellow, orange, light blue, gray and pink respectively. The color code matches the high-level architecture in Fig. 2. The 1T-1R array of memristive devices is driven by the appropriate voltages on the Word Line (WL), Source Line (SL), Bit Line (BL) for inference and learning. During inference the voltages across the memristor are proportional to the respective $P$ value. The current from the RCA gets normalized in the $\text{Norm}$ block which is fed to the $\text{box}$ and $\text{spike gen}$ blocks. The spikes $S$ from the $\text{Spike gen}$ are given to the $\text{error calculation}$ block which sends the arbitrated error events with the address of the learning row to the handshaking blocks ($\text{HS}$). This communication gives the control of the array to the learning row which sends back the $\text{lrn}_i$ signals back to the RCA.

Figure 7: Double integration scheme using $Q$ and $P$ integrators as is explained in Fig. 5. $Q$ integrator is a Differential-Pair Integrator (DPI) circuit in pink whose output current is converted to a voltage by the pseudo resistor highlighted in green. $P$ integrator is a $G_{m}C$ filter.

pulse can be used in this type of architecture. Specifically, our architecture matches well with Oxide-based Resistive RAM (OxRAM) [64] and Conductive Bridge RAM (CBRAM) type of devices [65].

In inference mode, WL is set to $V_{dd}$ which turns on the selector transistor, BL is driven by buffered $P$ voltages, and the SL is connected to a Transimpedance Amplifier (TIA) which pins each row of the array to a virtual ground. The current from the RCA is dependent on the value of the memristive devices. To ensure subthreshold operation for the next state of the computation, a normalizer block is used. The normalized output is fed both to a spike generator ($\text{spike gen}$) and a learning block (box). The pulse generator block acts as a neuron that only performs a thresholding and refractory function since its integration is carried out at the $P$ block. The generated $S$ spikes are communicated to the error generator block through the AER scheme as well as other layers. The learning block generates the box function described in Eq. (4).

In the learning mode, the array will be driven by the appropriate programming voltages on WL, BL and SL to update the conductance of the memristive devices. Since the whole array will be affected by the BL and SL voltages, at any point in time only one row of devices can be programmed. Since in our approach, the updates will be done on the error events which are generated per neuron, this architecture maps naturally to the error-triggered algorithm as the error events are generated for each neuron and hence per row. The error events are generated through the $\text{error calculation}$ block shown in Fig 6. This block can be implemented by another SNN or any non-linear function of $S$ implemented by a digital core (e.g. as explained in Sec. IV-A). The calculated errors are encoded in $\text{UP}$ and $\text{DN}$ learning events for every neuron of the array. Since only one neurons’ synapses can be updated at any point in time, these learning signals are arbitrated and the access to the learning bus will be granted to the learning signals of one neuron. As is explained in Sec. IV-A the address of
the acknowledged neuron is sent to the Handshaking blocks (HS) at each row (through Addr bus shown in Fig. 6) along with the sign of the update (\( \delta_i \)). The corresponding row \( i \) whose address matches Addr receives the address and its box block generates the \( lrn_i \) signal depending on the \( B \) value as specified in Tab. II. The WL\(_i\) remains at \( V_{dd} \) and all the other WL\(_j\), \( j \neq i \) switch to zero such that neuron \( i \) takes control over the array (implemented by gates \( N_1 \) in Fig. 6) which performs the AND operation between \( lrn_i \) and LRN signals which is the output of the OR operation between all \( lrn_j \) signals; Once in the learning mode indicated by the OR output (LRN signal), SL is switched to a common mode voltage (virtual ground) which blocks learning signals to the neurons. The voltage on BL\(_i\) (hence the \( V_{ij} \) in the figure) depends on the state of \( P_j \) which is a binary value as a result of comparing \( P_j \) with a threshold as is shown in Fig. 6. In accordance with the truth table Tab. II on the arrival of the \( UP \) or \( DN \) event, if \( B_i \) and \( P_j \) are non-zero, voltage \( V_{set} \) or \( V_{rst} \) will get applied to \( BL_j \) respectively. 

Once learning is over, the handshaking block elicits an acknowledge signal to the error calculating block which frees up the array and the Addr and \( \delta_i \) wait for the next request. 

**B. Detail of the Neuromorphic Circuits**

At the arrival of the \( Pre_i \) events from the AER input, the trace \( Q_j \) is generated through a DPI circuit shown in pink in Fig. 7 which generates a tunable exponential response in the form of a sub-threshold current [66]. The current is linearly converted to voltage using pseudo resistors in the block highlighted in green in Fig. 7. The first-order integrated voltage is fed to a \( G_mC \) filter giving rise to a second-order integrated output \( P_j \) which is buffered to drive the entire crossbar column in accordance with Eq. (1).

Output voltage \( P_j \) is applied to the top electrode of the corresponding memristive device (\( W_{ji} \)) whose bottom electrode is pinned by the crossbar front-end TIA. This block pins the entire row to virtual ground (in our case common mode voltage is set as half \( V_{dd} \)) and reads out the sum of the currents generated by the application of \( PS \) across the memristors in the row. As a result, voltage \( V_{FEi} \) is developed on the gate of the transistor at the output of the TIA which feeds to a normalizer circuit shown in Fig. 8. This circuit is a differential pair which re-normalizes the sum of the currents from the crossbar to \( I_{norm} \), ensuring that the currents remain in the sub-threshold regime for the next stage of the computation which is (i) the box function \( B(U) \) as is specified in Eq. (5) implemented by the box block and (ii) the spike generation block which gives rise to \( S \).

(i) is carried out by a modified version of the Bump circuit [67] which is a comparator and a current correlator that detects the similarity and dissimilarity between two currents in an analog fashion, as shown in the red box of Fig. 8. The width of the transfer characteristics of the Bump current directly implements the box function \( B(U) \) where \( I_U \) is close to \( I_L \) (condition \( u_- < U_i < u_+ \) from Sec. II-B). Unlike the original Bump circuit, Variable Width Bump (V WBump) [68] enables configurability over the width of the box function by changing the well potential \( V_{well} \). Moreover, the tunability of \( I_L \) allows setting the offset of the box function with respect to the normalized crossbar current. The details of using this circuit for learning is explained in [69]. The output of V WBump circuit gates the arbitrated \( UP \) and \( DN \) signals from the PC to indicate the sign of the weight update (up or down) or stop-learning (no update).

(ii) is carried out via a simple current to frequency (C2F) circuit, which directly translates \( I_U \) to spike frequency \( S \). The highlighted part implements the refractory period, which limits the spiking rate of this block.

**C. Circuit Simulations Results**

In this section, we report the simulations results for a standard CMOS 180nm process, showing the characteristics and output of the learning blocks. Moreover, we present the voltages across the memristive devices in a learning loop. Fig. 9 shows the output of the double integration of the input events \( Pre_i \) coming from the AER. \( Pre_0 \) and \( Pre_1 \) and subsequently \( P_0 \) and \( P_1 \) are plotted as examples. \( P_i \) smoothly follows the instantaneous firing rate of \( Pre_i \) as is expected. Fig. 10 shows the characteristics of the box function and its configurability using the circuit parameters. In Fig. 10a, the width of the box is tuned by the well potential shown in Fig. 8 and in Fig. 10b bias parameter \( I_L \) controls the offset...
and high respectively. Therefore, the voltage across the devices in the second row. Thus, the voltages $V_{10}$ and $V_{11}$ are both equal to $V_{set}$ to increase the conductance as a result of the $UP$ signal.

VI. DISCUSSION

A. Always-on, online learning

Our architecture supports an always-on learning engine for both inference and learning. By default, the RCA operates in the inference mode where the devices are read based on the value of $P$ voltages. On the arrival of error events, the array briefly enters a learning mode, during which it is blocked for inference. During this mode, input events are missed. The length of the learning mode depends on the pulse width required for programming the memristive devices, which could be less than $10 \text{ ns}$ up to $100 \text{ ns}$ depending on their type. Therefore, based on the frequency of the input events, the maximum size of the array can be calculated. The $1T - 1R$ memory can be banked with this maximum size. The details of this calculation is discussed in section IV-D.

B. Power and Area Evaluation

In this subsection, we report the area and power of the learning circuit in our learning architecture.

Neuronal circuits The average power and area of the neuronal circuits including the normalizer and box function is estimated to be about $100 \text{ nW}$ and $1000 \mu m^2$ respectively. Spike generator block The power of this block depends on the time constant of the refractory period which bounds the frequency of the C2F block. If we set the time constant to $10 \text{ ms}$ to limit the frequency to $100 \text{ Hz}$, the average power consumption of the block is about $10 \text{ uW}$. The area of the block is about $400 \mu m^2$.

Filters and RCA drivers The average power and area of these presynaptic circuits including $P$ generation are estimated around $2 \text{ mW}$ and $3000 \mu m^2$, respectively. We estimated the area and power of the buffer for the case where it can support up to $1 \text{ mA}$ of current. This current is dictated by the size of the array which we discuss in Sec. VI-C.

C. Scalability

a) Algorithm and architecture: By proceeding from first principles, namely surrogate gradient descent, this article proposes the design for general-purpose, online SNN learning machines. The factorization of the learning algorithm as a product of three factors naturally delineates the memory boundaries for distributing the computations. In our work, this delineation is realized through NCs and PCs. The separation of the architecture in NCs and PCs is consistent with the idea that neural networks are generally stereotypical across tasks, but loss functions are strongly task-dependent. The only non-local signal required for learning in an NC is the error signal $E$, regardless of which task is learned. The ternary nature of the three-factor learning rule and the sparseness afforded by the error-triggering enable frugal communication across the learning data path.

This architecture is not as general as a Graphical Processing Unit (GPU), however, for the following reasons: 1) the RCA inherently implements a fully connected network and 2) due to

Figure 9: Input events on two different input channels and their double integrated output $P_0$ and $P_1$.

Figure 10: Configurability on the box function. (a) shows how the width of the box function can be varied and (b) depicts how the box function midpoint can be moved by changing the $I_L$ value in Fig. 8.
reasons deeply rooted in the spatiotemporal credit assignment problem, loss functions must be defined for each layer, and these functions may not depend on past inputs. The first limitation 1) can be overcome by elaborating on the design of the NC, for example by mapping convolutional kernels on arrays [70]. There exists no exact and easy solution to the second limitation. However, recent work such as random backpropagation and local learning [8], [37], [39], [40], [71] are likely to provide new strategies to address this limitation in the future. Finally, although only feedforward weights were trained in our simulations, the approach is fully compatible with recurrent weights as well.

b) Crossbar array: Although relatively large arrays of Phase Change Memory (PCM) and ReRAM devices have been already implemented [49], [50], nano-scale effects such as IR drop and electromigration may limit the crossbar size. Partitioning the larger layers into smaller memory banks and summing up the output current can be employed as a solution for scaling up RCAs [72], [73].

Access transistor: Since learning is error-triggered, every event can only have one sign and hence for every update, the devices on a row \( i \) corresponding to non-zero \( R_j \)'s are updated either to higher or lower conductances together and not both at the same time. This allows sharing the MUXes at the periphery of the array, making the architecture scalable, since the size of the peripheral circuits grow linearly, while the size of the synapses grows quadratically with the number of neurons.

Peripheral circuits: The size of the \( P \) buffer and TIA at the end of the row is dependent on the amount of its driving current \( I_{\text{drive}} \) which is a function of the fan-out \( N \). Specifically, in the worst case where all the devices are in their low resistive state, the driving current of the buffer should support:

\[
I_{\text{drive}} = N * V_{\text{read}} / LRS
\]

where LRS is the low resistive state and \( V_{\text{read}} \) is the read voltage of the memristive devices. Assuming \( V_{\text{read}} \) of 200 mV which is a typical value for reading ReRAM and a low resistance of 1 \( \Omega \) [74], in the worst case when all the devices are in their low resistive state, to drive an array with fan-out of 100 neurons, the buffer needs to be able to provide 2 mA of current. This constraint can be loosened by having a statistic of the weight values in a neural network. For more sparse connectivity this current will drop significantly.

D. Error-triggered Learning Impact on Hardware

As explained in Sec. III the error-update signals are reduced from 8\( e6 \) to 96.7\( e3 \) and from 1.3\( e6 \) to 14.7\( e3 \) for DVSGesture and NMINST, respectively, after applying the error-triggered learning with a small impact of the performance. This reduction is directly reflected on improving the total write energy and lifetime of the memristors with \( 82.7 \times \) and \( 88.4 \times \) for DVSGesture and NMINST, respectively which are considered bottleneck for online learning with memristors [75]. A variant of the error-triggered learning has been demonstrated on the Intel Loihi research chip, which enabled data-efficient learning of new gestures [76] where learning one new gesture with a DVS camera required only 482\( mJ \). Although the Intel Loihi does not employ memristor crossbar arrays, the benefits of error-triggered learning stem from algorithmic properties, and thus extend to the crossbar array.
VII. CONCLUSION AND FUTURE WORK

In this article, we derived a local and ternary error-triggered learning dynamics compatible with crossbar arrays and the temporal dynamics of SNNs. The derivation reveals that circuits used for inference and training dynamics can be shared, which simplifies the circuit and suppresses the effects of fabrication mismatch. By updating weights asynchronously (when errors occur), the number of weight writes can be drastically reduced. The proposed learning rule has the same computational footprint as error-modulated STDP but is functionally different in that there is no acausal part, the updates are triggered on errors if the membrane potential is close to the firing threshold (rather than post-synaptic spike STDP). A more detailed comparison of the scaling of this family of learning rules is provided in [8]. In addition, the proposed hardware and algorithm can be integrated into spiking sensors such as neuromorphic Dynamic Vision Sensor [77] to enable energy-efficient computing on the edge thanks to the learning algorithm discussed in Sec. VI-D.

Despite of the huge benefit of the crossbar array structure, memristor devices suffer from many challenges that might affect the performance unless taken into consideration in the training such as asymmetric non-linearity, precision, and retention [75]. Solutions studied to address these non-idealities, such as training in the loop [16] or adjusting the write pulse properties to compensate them [78], are compatible with the learning approach proposed in this article. Fortunately, on-chip learning helps with other problems such as sneak path properties to compensate them [75], are compatible with the learning approach proposed in this article. Fortunately, on-chip learning helps with other problems such as sneak path (i.e. wire resistance), variability, and endurance. Combining these solutions and our learning approach will be addressed in future work. Interestingly, with error-triggered learning, only selected devices are updated and thus has a direct positive impact on endurance by reducing the number of write events. The reduction of write events is directly proportional to the set error rate $\langle |E| \rangle$, and can thus be adjusted based on the device characteristics. This leads to extending the lifetime of the devices and less write energy consumption.

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