Analysis and Implementation of Improved Software Phase-Locked Loop for Single-phase Grid-connected Inverter

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Abstract. For single-phase grid connected inverter, based on the traditional closed-loop structure of three-phase phase-locked loop (PLL), an improved software PLL was proposed. The basic principle of the phase-locked loop was analyzed and its mathematical model was deduced. In addition, the software implementation method of the phase-locked loop was presented. Then, the influence resulted from the change of amplitude, frequency and phase on the grid voltage was simulated with PSIM software. The results show that the software phase-locked loop can realize the phase tracking at any time in the cycle effectively and quickly, without waiting for the zero crossing of the grid. Finally, the software phase-locked loop proposed in this paper was implemented respectively by using TI's DSP TMS320F28035 and TMS320F2808 and applied to the 500W dual-channel single-phase grid-connected micro-inverter and 5kW single-phase grid-connected inverter. The simulation and experiment results verify the proposed software phase-locked loop.

1. Introduction

With the development of new energy technology, the photovoltaic grid-connected inverter has entered a stage of rapid growth. And the relevant international and domestic standards have strictly regulated and restricted the quality of grid-connected current. For example, the frequency and phase of the current must be synchronized with the grid in the grid-connected inverter, which is one of the key technologies to meet the grid-connected standards. However, the phase-locked loop is essential to ensure that the current can accurately and quickly track the phase and frequency of the grid voltage [1]. Compared with the traditional hardware phase-locking, software phase-locking, with fast speed and high precision, does not need to design and build the corresponding hardware circuit, which can save the cost for a grid-connected inverter. At present, the most widely used PLL technique is the zero-crossing detection phase-locked method. Although the structure is simple and easy to be realized, its dynamic performance is not good, and the dependence of zero-crossing voltage is very high, which limits the response speed of PLL [2]. Simultaneous frequency and phase modulation, and phase locking in multi-periods are mentioned in document [3]. However, these methods only capture the zero-crossing point of grid by using the digital signal processor (DSP) to correct the phase when the voltage of the power grid is on the zero-crossing point, thus the phase correction is not real-time control. In addition, it needs three timers and two capture units in DSP.

In this paper, an improved software PLL control method for a single-phase grid-connected inverter is proposed. When the voltage phase, frequency and amplitude of the power grid change, it is effective, fast and accurate to realize the phase-locking at any time, without waiting for the zero-crossing point of the grid, thus realizing the phase synchronization of the grid-connected current and the grid frequency.
Meanwhile, the program code is simple and of high portability. The method in this paper is simulated by PSIM and applied to 500W single-phase grid-connected micro-inverter and 5kW single-phase grid-connected inverter, and the expected results are obtained.

Firstly, the paper studies and analyses the operating principle of the single-phase phase-locked loop, and then studies its implementation method. Finally, the simulation verifies the ability of the proposed phase-locked loop to suppress the voltage disturbance, frequency disturbance, phase disturbance and high-order harmonic disturbance. And two application examples are given to verify the feasibility.

2. The Principle of Software Phase-locked Loop

2.1. The Principle of the Phase-locked Loop

Using the closed-loop structure of three-phase PLL for reference, the single-phase software phase-locked loop presented in this paper is realized by constructing two virtual orthogonal signals $\alpha$ and $\beta$, where $\nu_\alpha=\nu_{grid}$, $\nu_\beta=0$, and then the $v_d$ and $v_q$ are obtained by Park transformation.

$$\begin{align*}
\nu_d &= \nu_{grid} \cos \theta \\
\nu_q &= \nu_{grid} \sin \theta
\end{align*}$$

(1)

$\theta$ represents the phase angle obtained by the phase-locked loop, and $\nu_{grid}$ represents the grid voltage.

$$\begin{align*}
\nu_d &= \nu_{grid} \cos \theta \\
\nu_q &= -\nu_{grid} \sin \theta
\end{align*}$$

(2)

Let the grid voltage $\nu_{grid}$ be equal to $V_{grid} \sin \theta$, where $V_{grid}$ denotes the voltage amplitude of the power grid, $\varphi$ denotes the voltage phase of the power grid, and the following can be obtained by replacing these to the equation (2):

$$\begin{align*}
\nu_d &= V_{grid} \sin \varphi \cos \theta \\
\nu_q &= -V_{grid} \sin \varphi \sin \theta
\end{align*}$$

(3)

Using the product to sum equation of trigonometric function, we can obtain:

$$\begin{align*}
\nu_d &= \frac{V_{grid}}{2} \left[ \sin (\varphi - \theta) + \sin (\varphi + \theta) \right] \\
\nu_q &= \frac{V_{grid}}{2} \left[ \cos (\varphi - \theta) - \cos (\varphi + \theta) \right]
\end{align*}$$

(4)

As shown in the equation (4), $\theta=\varphi$ and $\sin (\varphi - \theta)=0$ when the phase-locking is successful. Therefore, if $\sin (\varphi + \theta)$ in the upper equation is eliminated, the phase-locking can be realized by controlling $\sin (\varphi - \theta)=0$. Then, we obtain the following equation (5) with the partial derivation of $\nu_\theta$, where $\omega_f=2\pi f$, $\theta=\omega_\theta t$, $\varphi=\omega_\varphi t$.

$$\begin{align*}
\frac{d\nu_d}{df} &= \frac{V_{grid}}{2} \left[ \sin (\varphi - \theta) + \sin (\varphi + \theta) \right] \omega_f \\
\frac{d\nu_q}{df} &= \frac{V_{grid}}{2} \left[ \sin (\varphi - \theta) + \sin (\varphi + \theta) \right] \omega_f \\
\omega_f &= \omega_f + \Delta \omega_f \\
\frac{d\nu_d}{dt} &= \frac{d\nu_d}{df} \frac{df}{dt} + \frac{d\nu_d}{d\theta} \frac{d\theta}{dt} \\
\frac{d\nu_q}{dt} &= \frac{d\nu_q}{df} \frac{df}{dt} + \frac{d\nu_q}{d\theta} \frac{d\theta}{dt}
\end{align*}$$

(5)

If the system is stable, $\omega_\varphi$ can be approximated as $\omega_f$. Equation (8) can be obtained by reorganizing equation (8).
\[
\frac{dv_q}{dt} = \frac{V_{\text{grid}}}{2} \left[-\sin(\varphi + \theta)\right](2\omega_f)
\]  

(8)

Insert equation (8) into equation (4) to get the following equation, then:

\[
\omega_{\text{err}} = \frac{dv_q}{dt} - \frac{1}{2\omega_f} + v_d = \frac{V_{\text{grid}}}{2} \sin(\varphi - \theta)
\]  

(9)

As shown in figure 1, \(\omega_{\text{err}}\) as the angular velocity error of power frequency is sent to the input end of the PI regulator, and the output of the PI regulator is \(\omega_{\text{ff}}\). The phase angle output of PLL can be obtained by the integral operation of \(\omega_{\text{ff}}\). If the PI regulator is controlled steadily, \(\omega_{\text{err}}\) is equal to zero, that is, the power frequency angular velocity in accordance with the power grid by the phase-locked loop is obtained. In figure 1, \(\text{mod}(2\pi)\) denotes that the phase-locked loop takes \(2\pi\) as a periodic output phase angle.

![Figure 1. Control block diagram of the phase-locked loop.](image1)

![Figure 2. Schematic diagram of phase superposition.](image2)

2.2. Implementation of Software Phase-locked Loop

It can be seen from the control block diagram of PLL that the output \(\omega_{\text{ff}}\) of PI regulator needs an integral operation, but it is very complicated to realize an integral part of the actual programming. As \(\sin(\Delta\omega)\) and \(\Delta\omega\) approximately equal when the angular radian \(\Delta\omega\) is very small, the period of the power grid can be divided into \(N\) equal parts, thus the fixed step value \(\omega = 2\pi/N\) can be obtained, and the fixed radian \(\omega + \Delta\omega\) can be added in the software interrupt to realize the output of the phase angle. The phase superposition diagram is shown in Figure 2 and the implementation flow chart of the PLL program is shown in Figure 3.

![Figure 3. Program flow chart of PLL.](image3)
\[ G(z) = \frac{z^{-1}v_q - \frac{1}{T_s}v_y - \frac{1}{T_s}z^{-1}v_y}{1 - \frac{1}{T_s}z^{-1}}v_y = f_s v_q - f_s v_q z^{-1} \]  

(10)

In which, \( f_s \) is the sampling frequency. The following can be further obtained:

\[ \frac{1}{2\omega_f}G(z) = f_s \frac{1}{2\omega_f}(v_y - v_y z^{-1}) \]  

(11)

The final indication is:

\[ \frac{f_s}{2\omega_f}(v_y(k) - v_y(k-1)) \]  

(12)

On this basis, the first-order low-pass filtering is carried out in the program.

\[ \Delta v_y(k) = 0.4\Delta v_y(k-1) + 0.6 \cdot \frac{f_s}{2\omega_f}(v_y(k) - v_y(k-1)) \]  

(13)

Figure 4. Simulation circuit diagram of the phase-locked loop.

3. Simulation and Experiment on Software Phase-locked Loop

3.1. Simulation on Software phase-locked Loop

In order to verify the effectiveness of the above PLL control method, the software PLL method is simulated by using the power simulation (PSIM) software. The simulation conditions are as follows: the power grid amplitude \( V_{\text{grid}} \) is 314V, the power grid frequency \( f \) is 50Hz, \( \omega = \frac{2\pi}{N} = 0.0154 \text{rad} \), \( N \) is 400, and the sampling frequency \( f_s \) is 20 kHZ. The algorithm proposed in this paper is implemented in the simulation module MCU, and the module combination is used to simulate the changes in the power grid.

The simulation circuit diagram of the phase-locked loop is shown in figure 4.

Figure 5. Simulation waveforms of voltage mutation.

Figure 6. Simulation waveforms of frequency mutation.
The simulation waveform of amplitude mutation of the power grid is shown in figure 5. It can be seen that the amplitude of power grid changes from 314V to 200V at 0.4s, and returns to normal at 0.6s. And the PLL output is consistent with the phase of the power grid, thus realizing the accurate phase locking. The frequency of the actual 50Hz power system varies from 49.42Hz to 50.42Hz. Power grid frequency mutation simulation: the frequency is abrupt to 48Hz at 0.4s, and 48Hz is changed to 51Hz at 0.6s. The waveform is shown in figure 6.

Phase mutation simulation of the power grid: the phase delays $\pi/6$ at 0.4s, and returns to normal at 0.6s. The waveform is shown in figure 7, and the phase-locked loop is locked successfully in a power grid cycle.

Simulation of the power grid with high harmonic components: the voltage of the power grid is superimposed with the high harmonic at 1s, whose waveform is shown in Fig.8. As shown in figure 8, the phase output of the PLL has not been affected, and it always follows the voltage phase of the power grid, which shows that the software PLL also has the function of filtering high-frequency harmonics.

The improved software PLL control method proposed in this paper has been verified by the PSIM simulation, which can efficiently and quickly realize phase-locked when the voltage amplitude, frequency or phase changes in the power grid. Meanwhile, the software PLL can also filter the high-frequency harmonics. To further verify the PLL control algorithm proposed in this paper is portable in the photovoltaic grid-connected inverter system, the algorithm is applied to the dual-channel flyback grid-connected micro-inverter and 5kW single-phase grid-connected inverter with H6 bridge. These two inverter systems are firstly modeled and simulated with PSIM software, then are verified through corresponding experiments.

![Figure 7. Simulation waveforms of phase mutation.](image1)

![Figure 8. Simulation waveforms of phase-locking with high order harmonics.](image2)

![Figure 9. Simulation model for micro-inverter system.](image3)
3.2. Simulation of Software PLL Algorithm for Dual-channel Grid-connected Micro-inverter

The simulation model for the main circuit of dual-channel grid-connected micro-inverter is shown in figure 9.

Figure 10 shows the output current and grid voltage waveforms of the dual-channel grid-connected micro-inverter. For the convenience of the display, the grid voltage is reduced by 200 times. It can be seen that the phase of the output current can well track the phase of the grid voltage, which proves the feasibility of the proposed software PLL algorithm.

![Figure 10. Simulation Waveforms of the dual-channel grid-connected micro-inverter.](image1)

3.3. Simulation of Software PLL Algorithm for an Inverter with H6 Bridge

The simulation model of a single-phase grid-connected inverter system with an H6 bridge in PSIM software is shown in figure 11, which is mainly composed of photovoltaic modules as DC input source, inverter with H6 bridge module, power grid module and inverter control module. And the system simulation waveforms is shown in figure 12.

![Figure 11. Simulation model of single-phase grid-connected inverter system.](image2)

![Figure 12. Simulation waveforms of single-phase grid-connected inverter.](image3)
3.4. Experimental Results of Software Phase-locked Loop

The software PLL method proposed in this paper is applied to the 500W dual-channel grid-connected micro-inverter system, in which TMS320F28035 is chosen as the main control chip, and the 5kw single-phase grid-connected inverter, in which TMS320F2808 is chosen as the main control chip. The frequency of the power grid is represented by $\omega(15)$, and the minimum precision is $1/32768 = 3\times10^{-5}$. The phase-locking program is placed in the interruption of 50μs, and angular radians add $\omega + \Delta\omega$ per interruption, where $\omega$ is 0.0154 rad. By configuring the register Timer0 of DSP, the desired sampling frequency 20kHz is obtained. After interruption occurs, the following steps are taken by DSP: Enable the A/D port to sample the grid voltage, carry out park transform, output the step angle by an integral part of the PI controller, and then wait for the next interruption.

![Figure 13. Simulation diagram of phase mutation.](image)

The parameters $k_\alpha$ and $k_\beta$ of the PI controller can be achieved by simulation. The 100V power grid voltage generated by the voltage regulator is used to test PLL control performance, which is shown in figure 13. The waveform is displayed by the host computer, where $\sin(\theta)$ is amplified by 100 times. Figure 14 is the experimental prototype of the dual-channel grid-connected micro-inverter. Figure 15 shows the actual grid-connected waveform of the dual-channel grid-connected micro-inverter system. Figure 16 is the experimental prototype of a 5kW single-phase grid-connected inverter and figure 17 is the actual grid-connected waveform of the 5kW single-phase grid-connected inverter. It can be seen that the phase of the grid-connected current is consistent with that of the power grid. The experimental results show that the software PLL can track the phase and frequency of the power grid effectively and quickly, which achieves the desired control performance.

![Figure 14. Experimental prototype of the dual-channel micro-inverter.](image)

![Figure 15. Experimental waveforms.](image)
4. Conclusion

In view of the application of a single-phase grid-connected inverter, an improved software PLL control method is proposed in this paper. When the voltage amplitude, frequency or phase of the power grid changes, the phase-locking can be realized with high-precision at any time in the period effectively and rapidly, without waiting to detect the zero-crossing point of the grid voltage, thus realizing the phase-locking of the grid-connected current effectively. Meanwhile, the software PLL has the function of filtering the high-frequency harmonics, which improves the precision, safety, and stability of phase-locking of the grid-connected inverter, without the need for a hardware circuit, thus improving the performance-price ratio of the grid-connected inverter system. Meanwhile, the program code is simple and of high portability. The correctness of the improved software phase-locked loop control method and the portability of the phase-locked loop program code have been verified in the 500W dual-channel grid-connected micro-inverter and 5kw single-phase grid-connected inverter. In addition, it has a certain application value in engineering practice.

Acknowledgments

This paper was supported in part by the National Natural Science Foundation of China under Grant 61873346, in part by the Science and Technology Cooperation Fund of Yangzhou City Hall project under Grant YZ2018136, in part by the Intelligent Energy Internet Research Institute Joint Fund of State Grid Yangzhou Power Supply Company and Yangzhou University under Grant SGTYHT/17-JS-202, and in part by the Open Project Fund of Yangzhou University Jiangdu Institute of High-end Equipment Engineering Technology under Grant YDJ201902.

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