On Mitigating Random and Adversarial Bit Errors

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Abstract

The design of deep neural network (DNN) accelerators, i.e., specialized hardware for inference, has received considerable attention in past years due to saved cost, area, and energy compared to mainstream hardware. We consider the problem of \textit{random and adversarial bit errors in quantized DNN weights} stored on accelerator memory. Random bit errors arise when optimizing accelerators for energy efficiency by operating at low voltage. Here, the bit error rate increases exponentially with voltage reduction, causing devastating accuracy drops in DNNs. Additionally, recent work demonstrates attacks on voltage controllers to adversarially reduce voltage. Adversarial bit errors have been shown to be realistic through attacks targeting individual bits in accelerator memory. Besides describing these error models in detail, we make first steps towards DNNs robust to random and adversarial bit errors by explicitly taking bit errors into account during training. Our \textit{random or adversarial bit error training} improves robustness significantly, potentially leading to more energy-efficient and secure DNN accelerators.

1 Introduction

The success of deep neural networks (DNNs) is partly due to parallel hardware, such as mainstream GPUs. Recently, \textit{DNN accelerators}, i.e., specialized hardware for inference, have been used to reduce and limit energy consumption alongside cost and space. In particular, accelerators make use of highly parallel computational units, reduced precision, as well as custom memory organization and data flow to improve energy efficiency, e.g., see \cite{1,2,3,4,5}. Low voltage operation is an effective strategy to lower energy consumption significantly. However, low voltage operation can lead to bit-level failures in memory \cite{6,7}. Additionally, recent work demonstrated severe security threats by intentionally manipulating operating voltage \cite{8}, or explicitly injecting bit errors in memory \cite{9} to reduce DNN accuracy \cite{10}. Such hardware related design and security constraints are typically not taken into account in DNN design. Obtaining \textit{robustness against random or adversarial bit errors in quantized DNN weights} presents a challenging and unique problem for the machine learning community with direct impact on energy consumption and security of DNN accelerators.

DNN accelerators generally feature on-chip SRAM memory arrays used as scratchpads to store weights and inputs. In order to reduce energy consumption, operating voltage is reduced below \( V_{\text{min}} \), the minimum voltage at which error-free operation is guaranteed. This “low-voltage” operation causes bit failures in SRAMs with devastating effect on DNN accuracy. The rate \( p \) of bit errors is shown to increase exponentially as supply voltage is scaled down \cite{6,11,12,13}. For example, Fig. 1 (left) shows that obtaining robustness against, e.g., \( p = 1\% \) bit errors at 0.83\( V_{\text{min}} \) has the potential to reduce SRAM energy by roughly 30\% compared to operation at \( V_{\text{min}} \). Circuit techniques such as error detection via redundancy \cite{14} and supply voltage boosting \cite{13} have been explored to guarantee robust DNN operation below \( V_{\text{min}} \). Such approaches allow significant reduction in energy, however, there is still an energy overhead incurred due to error mitigation in hardware. Therefore, \cite{12,15} trained DNNs robust to low-voltage induced SRAM and DRAM errors, respectively, by injecting

Preprint. Under review.
Figure 1: Impact and Energy-Savings of Random Bit Errors. Left: Exemplary SRAM bit error rate $p$ and normalized energy per SRAM access [13], which has large impact on accelerator energy consumption as supply voltage is scaled below $V_{\text{min}}$. Middle: Original weight value, quantized with 16 bits in $[-0.15, 0.15]$ on CIFAR10, plotted against the weight with random bit errors of rate $p = 1\%$; 5.5M weights shown. Color indicates error magnitude: zero (diagonal, violet) to $\sim 0.225$ (yellow). Right: Impact of bit errors on test error for CIFAR10. Reducing quantization range, i.e., clipping, to $[-0.15, 0.15]$ and random bit error training (RANDBET) clearly improves robustness.

*profiled* bit errors during training, i.e., chip-specific spatial distributions of bit failures in memory arrays. Thus, for every chip and operating voltage, the memory needs to be profiled and the DNNs need to be re-trained, both of which are not scalable.

Only few works consider robustness of DNNs in terms of quantized weights. In [16], the authors consider Gaussian noise on weights and, in [17, 18, 19, 20], the robustness of DNNs towards quantization is studied. Weng et al. [21] consider adversarial $L_{\infty}$ perturbations on weights, also with an application to quantization. However, as shown in Fig. 1 (middle), bit errors represent a unique and challenging noise model where few bit errors, e.g., in the most significant bits (MSBs) can induce large changes. This is in stark contrast to Gaussian, $L_{\infty}$ or quantization noise. Thus, the authors of [10] directly identify and adversarially flip bits in quantized weights to reduce accuracy. In concurrent work, He et al. [22] argue that training on such adversarially injected bit errors does not improve robustness and propose a binarization approach instead. In contrast, we demonstrate an adversarial bit error training technique that improves robustness and additionally consider the more realistic case of random bit errors, crucial for energy efficiency *and* security in DNN accelerators. Similar to [10], we do *not* provide an end-to-end demonstration of a security attack with adversarial bit flips on memory. Instead we identify and train on adversarial bit errors to improve robustness.

**Contributions:** We consider the problem of random and adversarial bit errors in DNN weights with fixed-point quantization. We demonstrate that random bit errors can cause severe drops in accuracy and adversarial bit errors are able to devastate accuracy with only few, but specific, bit flips. We incorporate completely random bit errors into the training procedure, resulting in robust operation across multiple bit error patterns and multiple voltage operating points. Furthermore, we present a min-max formulation of training with adversarial bit errors, resulting in significantly improved robustness against adversarially-induced bit failures, e.g., via attacks demonstrated in [9], as well as random bit errors caused by maliciously reducing operating voltage, as demonstrated in [8]. On MNIST [23], Fashion-MNIST [24] and CIFAR10 [25], we present extensive experiments showing that our approach leads to more secure *and* energy-efficient DNN accelerators.

## 2 Related work

**Weight Robustness:** Few works explicitly consider robustness to weight perturbations: [21] certify the robustness of weights with respect to $L_{\infty}$ perturbations and [16] study Gaussian noise on weights. More related to our work, [10] considers identifying and flipping few vulnerable bits in quantized weights. In concurrent work, He et al. [22] propose a binarization approach to obtain robustness against such adversarial bit errors. Moreover, they argue that training with adversarial bit errors does *not* lead to improved robustness. Several works [17, 18, 19, 20] also consider the robustness of DNNs against quantization errors. Fault tolerance, in contrast, describes structural changes such as removed units, and is rooted in early work such as [26, 27] utilizing approaches similar to adversarial training [28]. Finally, some works [29, 30] explicitly manipulate weights in order to integrate backdoors. In contrast to [21, 16], we study robustness against random and adversarial *bit errors*. In contrast to [10], we propose a projected gradient ascent approach to obtain adversarial bit flips. And despite [22], we show that our adversarial bit attack allows a min-max training formulation, similar to [28], that improves robustness significantly. While we also consider fixed-point quantization [31, 32, 33], quantization errors are significantly less severe than bit errors.
Bit Errors in DNN Accelerators: Recent work [6,11] demonstrates that bit flips in SRAMs increase exponentially when reducing voltage below $V_{min}$. The authors of [13] study the impact of bit flips in different layers of DNNs, showing severe accuracy degradation. Similar observations hold for DRAM [34]. To prevent accuracy drops at low voltages, Minerva [14] combines SRAM fault detection with logic to set faulty data reads from the SRAM to zero when faults are detected. [13] uses supply voltage boosting for SRAMs to achieve robustness at low voltages, while [35] proposes storing critical bits in specifically robust SRAM cells. However, such methods incur power and area overhead. Thus, [12] injects profiled SRAM bit errors during training and [15] trains with DRAM errors and maps the model to DRAM in a way to guarantee a certain accuracy. Besides low-voltage operation for energy efficiency, recent work [8] shows that an attacker can reduce voltage maliciously. Similarly, works such as [36,9] demonstrate software-based approaches to induce few, but targeted, bit flips in DRAM. Our bit error training improves robustness against random or adversarial bit errors and, in contrast to [12], generalizes across chips with different memory bit error patterns.

3 Random and Adversarial Bit Errors in Quantized DNNs

We consider two bit error models: First, random bit errors occur due to low voltage operation. Here, bit flips occur with probability $p$ (in %). Second, we consider adversarial bit errors as motivated by recent attacks on memory [36,9,10]. In this setting, we consider a fixed budget of bit errors, e.g., a maximum of $p\%$ of bits can be flipped.

Notation: The DNN $f$ predicts a probability distribution $f(x; w) \in \mathbb{R}^K$ for an input $x \in [0,1]^D$ and weights $w \in [-w_{max}, w_{max}]^W$, where $W$ is the total number of weights of the network. Given an input $x$ and label $y$, the prediction is correct iff $y = \text{argmax}_k f_k(x; w)$. The DNN is trained by minimizing the cross-entropy loss $\mathcal{L}$. For quantized DNNs, $m$ denotes the number of bits per weight value and $Q$ is a quantization function such that $v := Q(w)$ denotes the quantized weight vector. In practice, $v_i$ is an $m$-bit signed integer representing the underlying $m$ bits. In the following, we use $v_i \in \{-2^{m-1}, \ldots, 2^{m-1} - 1\}$ corresponding to the underlying bits $v_i \in \{0,1\}^m$. De-quantization is expressed as $w_q := Q^{-1}(v)$. By $v = \text{BErr}_p(v)$, we denote random bit errors with probability $p$. On expectation, $\bar{v}$ has $pmW$ bits flipped compared to $v$, as measured using the bit-level Hamming distance between $m$-bit signed integers $d_H(v, \bar{v})$.

Fixed-Point Quantization: Quantization determines how weights $w \in \mathbb{R}^W$ are represented, e.g., in SRAM. Following related work [31,32,33], we consider a fixed-point quantization: $m$ bits allow to represent $2^m$ distinct values. For an arbitrary but fixed maximum absolute weight $w_{max}$, the range $[-w_{max},w_{max}]$ is quantized into bins of width $\Delta$. We consider a quantized weight $w_i$ to be represented by a signed $m$-bit integer $v_i = Q(w_i)$ (in two’s complement representation) corresponding to the underlying bits $v_i \in \{0,1\}^m$. De-quantization is expressed as $w_q := Q^{-1}(v)$. By $v = \text{BErr}_p(v)$, we denote random bit errors with probability $p$. On expectation, $\bar{v}$ has $pmW$ bits flipped compared to $v$, as measured using the bit-level Hamming distance between $m$-bit signed integers $d_H(v, \bar{v})$.

Low-Voltage Induced Random Bit Errors: Following [6,12,13], the probability of SRAM bit cell failures increases exponentially as operating voltage is scaled below $V_{min}$, i.e., the minimal voltage required for reliable operation, see Fig. 1(left). This is done intentionally to reduce energy consumption, e.g., [13,12,15], or adversarially by an attacker, e.g., [9]. Process variation during fabrication causes a variation in the extent of vulnerability of individual bit cells. For a given memory array, bit cell failures are assumed to be random and independent of each other, and there is a fixed spatial distribution of bit cell failures. As shown in [11], if a bit error occurred at a given voltage, it is likely to occur at lower voltages, as well. Across different SRAM arrays in a chip or different chips, the patterns or spatial distribution of bit errors is usually different and can be assumed random [13]. We condense these observations into the following bit error model used throughout the paper:

The probability of a bit error is $p$ (in %) for all weight values and bits. For a fixed chip, bit errors are persistent across supply voltages, i.e., bit errors at probability $p'$ also occur at probability $p$. A bit error flips the currently stored bit. We denote random bit error injection by $\text{BErr}_p$.

We assume the quantized weights are stored linearly within the memory. Thus, in practice, for $W$ weights and $m$ bits per weight value, we sample uniformly $u \sim U(0,1)^{W \times m}$. Then, the $j$-th bit in
An adversary can flip up to $\epsilon$ bits.

We will adversarially inject bit errors based on the gradient of Eq. (2) and perform a projection onto $v$.

Algorithm 1 Adversarial Bit Errors and Training.

**Left:** We maximize cross-entropy loss using projected gradient ascent while ensuring that at most $\epsilon := [pmW]$ bits are flipped ($W$ weight values, $m$ bits each). Line 9 may include backtracking and Line 10 may include gradient normalization. Right: Our average-gradient adversarial weight training using adversarial bit errors or random bit errors. For illustration, we color the original floating-point weights $w$ in magenta, the quantized weights as signed $m$-bit integers $v = Q(w)$ in red and the de-quantized weights $w_q = Q^{-1}(v)$ in blue.

### Algorithm 1: Adversarial Bit Errors and Training

1: **procedure** ADVBitErrors($w$, $p$)
2: $v = Q(w)$, $\epsilon = [pmW]$
3: initialize: $d_H(\tilde{v}(0), v) \leq \epsilon, d_H(\tilde{v}(0), v_i) \leq 1$
4: for $t = 0, \ldots, T - 1$ do (fixed $\{x_b, y_b\}_b = 1$)
5: $\tilde{w}(t) = Q^{-1}(\tilde{v}(t))$
6: forward pass using de-quantized weights:
7: $\Delta(t) = \nabla_w \sum_{b=1}^B L(f(x_b, \tilde{w}(t)), y_b)$
8: update without quantization:
9: $\tilde{w}(t+1) = \tilde{w}(t) + \gamma \Delta(t)$
10: project: $d_H(\tilde{v}(t+1), v) \leq \epsilon, d_H(\tilde{v}(t+1), v_i) \leq 1$
11: return $\tilde{w}(T) = Q^{-1}(Q(\tilde{w}(T)))$

### Adversarial Bit Errors:

Following recent attacks on memory [36, 43, 9, 10], we also consider adversarial bit errors. Our model assumes that the flipped bits at lower probability $p' \leq p$ are a subset of the flipped bits at probability $p$ and that bit flips to 1 and 0 are equally likely. The unique noise pattern of random bit errors is illustrated in Fig. 1 (middle): for example a single bit flip in the most-significant bit (MSB) of the signed integer $v_i$ can result in a change of roughly half of the quantized range, i.e., $\pm w_{\text{max}}$.

### Adversarial Bit Errors:

Following recent attacks on memory [36, 43, 9, 10], we also consider adversarial bit errors. We constrain the number of injected bit errors by $\epsilon := [pmW]$, similar to the $L_p$-constrained adversarial inputs. Furthermore, we consider only one bit flip per weight value to simplify the projection onto the discrete constraint set. Then, given knowledge of memory layout and addressing schemes, an adversary can use, e.g., RowHammer [36], in order to flip as many of the adversarially selected bits. Note that, in practice, not all of these bits will be vulnerable to an end-to-end RowHammer attack on memory, which we do not focus on. However, from a robustness viewpoint, it makes sense to consider a slightly stronger threat model than actually realistic. Overall, our white-box threat model is defined as follows:

An adversary can flip up to $\epsilon := [pmW]$ bits, at most one bit per (quantized) weight value, in order to reduce accuracy and has full access to the DNN, its weights and gradients.

Following the projected gradient ascent approach of [28] and letting $d_H$ be the (bit-level) Hamming distance, we intend to maximize cross-entropy loss $L$ on a mini-batch $\{x_b, y_b\}_b = 1$ of examples:

$$\max_{\epsilon} \sum_{b=1}^B L(f(x_b; Q^{-1}(\tilde{v})), y_b) \quad \text{s.t.} \quad d_H(\tilde{v}, v) \leq \epsilon, \quad d_H(\tilde{v}, v_i) \leq 1$$ (2)

As made explicit in Eq. (2), we work on bit-level, i.e., optimize over the signed integer representation $\tilde{v}_i \in \{2^{m-1}, \ldots, 2^m - 1\}$ corresponding to the underlying bits of the perturbed weights $\tilde{w} = Q(\tilde{v})$.

We will adversarially inject bit errors based on the gradient of Eq. (2) and perform a projection onto the Hamming constraints $d_H(\tilde{v}, v) \leq \epsilon$ and $d_H(\tilde{v}, v_i) \leq 1$ with respect to the quantized, clean weights $v = Q(w)$. This means that we maximize Eq. (2) through projected gradient ascent where the forward and backward pass are performed in floating point:

$$\tilde{w}(t+1) = \tilde{w}(t) + \gamma \Delta(t) \quad \text{with} \quad \Delta(t) = \sum_{b=1}^B \nabla_w L(f(x_b; \tilde{w}(t), y_b), \tilde{v}(t)) = Q^{-1}(Q(\tilde{w}(t)))$$ (3)

followed by the projection of $\tilde{v}(t+1) = Q(\tilde{w}(t+1))$ onto the (bit-level) Hamming constraints of Eq. (2). Here, $\gamma$ is the step size. The updates are performed in floating point, while the forward pass is performed using the de-quantized weights $\tilde{w}(t)$. The perturbed weights $\tilde{w}(0) = Q^{-1}(\tilde{v}(0))$ are initialized by uniformly picking $k \in [0, \epsilon]$ bits to be flipped in $v = Q(w)$ in order to obtain $\tilde{v}(0)$.

Overall, our adversarial bit attack is summarized in Alg. 1.
We aim to obtain robustness against random and adversarial bit errors through random bit error training as in Alg. [1] when λ = 1. Here, BErr_p injects random bit errors in the signed m-bit integers \( u^{(t)} = Q_v(w^{(t)}) \), resulting in \( \tilde{v}^{(t)} \), while the forward pass is performed on the de-quantized perturbed weights \( \tilde{w}_q^{(t)} = Q_v^{-1}(\tilde{v}^{(t)}) \), i.e., fixed-point arithmetic is not emulated. The weight update during training is not affected by bit errors and computed in floating point. Color coding follows Alg. [1]

The Hamming-projection is similar to the \( L_0 \) projection used for adversarial inputs, e.g., in [44]. Dropping the superscript \( t \) for brevity, in each iteration, we solve the following projection problem:

\[
\min_w \|Q_v^{-1}(\tilde{v}) - Q_v^{-1}(\tilde{v}')\|_2^2 \quad \text{s.t.} \quad d_H(v_i, \tilde{v}_i') \leq 1, \quad d_H(v, \tilde{v}') \leq \epsilon \quad (4)
\]

where \( \tilde{v} = Q_v(w) \) are the quantized, perturbed weights after Eq. (3), \( \tilde{v}' = Q_v^{-1}(\tilde{v}') \) will be the perturbed weights after projection, and \( v = Q_v(w) \) are the quantized, clean weights. This can be solved in two steps as the objective and the constraint set are separable: The first step involves keeping only the top-\( \epsilon \) changed values, i.e., the top-\( \epsilon \) weights with the largest difference \( |w_i - \tilde{w}_i| \). The second step can be solved by keeping only the most significant bit changed in \( \tilde{v} \) compared to \( v \).

The optimization problem in Eq. (2) is challenging due to the projection onto the non-convex set of Hamming constraints. We adopt best practices from computing adversarial inputs: normalizing the gradient [44] and backtracking [45]. Gradient normalization includes dividing by the \( L_1 \) norm \( \|\Delta^{(t)}\|_1 \), and then by the corresponding maximum absolute value. Using backtracking, the update in each iteration is only kept if the cross-entropy loss increases, otherwise, the step size \( \gamma \) is reduced. In spite of these optimization tricks, Alg. [1] remains very sensitive to hyper-parameters.

### 4 Robustness through Random and Adversarial Bit Error Training

We aim to obtain robustness against random and adversarial bit errors through bit error training. Robustness against random bit errors of probability \( p \), caused by low-voltage operation, has to induce robustness for bit errors with lower probability \( p' \leq p \), as well. In practice, this allows to operate accelerators over a wider range of voltages. Here, we aim to preserve the average-case robust test error, i.e., the test error under the influence of bit errors, and keep the standard deviation low in order to generalize to many different bit error patterns or spatial distribution of errors corresponding to different chips. Robustness to adversarial bit errors is measured in terms of worst-case robust test error that an adversary can obtain within a fixed budget of allowed bit flips, i.e., \( \epsilon := \lceil pmW \rceil \). Additionally, robustness against random bit errors with significantly higher \( p \) is desirable to “defend” against malicious reductions in operating voltage.

**Aggressive Clipping:** As first step towards robustness, we aggressively reduce the quantization range \( w_{\text{max}} \). This is similar in spirit to learning quantization ranges [46, 38], but with robustness in mind. Smaller \( w_{\text{max}} > 0 \) will increase resolution of the quantization, by reducing \( \Delta \) in Eq. (1), while restricting the range of allowed weight values. Weight values are clipped to \( [-w_{\text{max}}, w_{\text{max}}] \) which is then quantized with \( m \) bits, i.e., \( 2^m \) distinct values. Bit flips are injected post quantization such that reducing \( w_{\text{max}} \) has the effect of restricting the range of perturbed weights, as well.

**Random Bit Error Training (RAND BET):** Injecting random bit errors with probability \( p \) during training results in the following learning problem, which we optimize as illustrated in Fig. 2:

\[
\min_w \mathbb{E}[\mathcal{L}(f(x; \tilde{w}), y) + \lambda \mathcal{L}(f(x; w), y)] \quad \text{s.t.} \quad \tilde{w} = Q_v^{-1}(\tilde{v}), \tilde{v} = \text{BErr}_p(v), v = Q_v(w). \quad (5)
\]
Random Bit Errors on MNIST

| Training | $w_{\text{max}}$ | Err | avg RErr in % | $\mu_{\text{max}}$ | Err | avg RErr in % |
|----------|-----------------|-----|---------------|-------------------|-----|---------------|
| Normal   | 0.1             | 0.36 | 89.92 89.98   | 0.25              | 5.37 | 91.04 90.85   |
| Normal   | 0.1             | 0.29 | 3.71 68.67    | 0.25              | 5.58 | 88.67 90.71   |
| Normal   | 0.05            | 0.29 | 1.30 22.37    | 0.2               | 6.26 | 81.33 90.17   |
| RandBet  | 1               | 0.63 | 90.16 90.12   | 1                 | 10.24 | 42.33 47.54   |
| RandBet  | 0.1             | 0.31 | 0.45 0.62     | 0.25              | 7.26 | 9.63 11.67    |
| RandBet  | 0.05            | 0.37 | 0.52 0.69     | 0.2               | 6.76 | 8.99 10.78    |

Table 1: Effect of Clipping on Robustness. Clipping, i.e., lowering $w_{\text{max}}$ in Eq. (1), improves robustness against random bit errors and allows to train with large error rates, e.g., 2.5% on MNIST. Too aggressive clipping increases test error (red), cf. F-MNIST, and reduces confidences (right).

where \( v = Q(w) \) denotes the quantized weights \( w \) which are to be learned. \( \text{BErr}_{p}(v) \) injects random bit errors with rate \( p \) in \( v \) and \( \lambda = 1 \) (fixed in all experiments) means that we also consider the loss on clean weights. This is desirable to avoid an increase in (clean) test error and stabilize training compared to \( \lambda = 0 \) which corresponds to training only on bit errors in the weights. We use stochastic gradient descent to optimize Eq. (5), by performing the gradient computation using the perturbed weights \( \tilde{w} = Q^{-1}(\tilde{v}) \), while applying the gradient update on the clean weights \( w \). In spirit, this is similar to data augmentation, however, the perturbation is applied on the weights instead of the inputs. We found that introducing bit errors right from the start may prevent the DNN from converging. Thus, we start applying bit errors as soon as the (clean) cross-entropy loss reaches 1.75 or below.

Adversarial Bit Error Training (AdvBET): Training with adversarial bit errors follows the formulation of Eq. (5). However, instead of random bit errors, adversarial bit errors are used, resulting in a min-max formulation similar to (28):

\[
\min_w \mathbb{E}[\max_{\tilde{v}, \hat{v}} \mathcal{L}(f(x; Q^{-1}(\tilde{v})), y) + \lambda \mathcal{L}(f(x; w), y)] \quad \text{s.t.} \quad d_H(\hat{v}, v_i) \leq \epsilon, d_H(\tilde{v}, v_i) \leq 1
\]

where the maximization problem, i.e., the attack, is constrained in the number of bits that may be changed by \( \epsilon := \lfloor \mu MW \rfloor \). Details are provided in Alg. 1. In addition to not training on adversarial bit errors for a (clean) cross-entropy above 1.75, we clip gradients to \([-0.05, 0.05]\). This is required as the cross-entropy loss on adversarially perturbed weights \( \tilde{w} \) can easily be one or two magnitudes larger than on the clean weights. Similarly, we found smaller learning rates for training to be necessary. Finally, training is very sensitive to the hyper-parameters of the attack in Alg. 1 including the step size, gradient normalization and backtracking. This holds both for convergence during training as well as for the obtained robustness after training. To overcome these problems, and in contrast to common practice in adversarial training on adversarial inputs (28), we randomize the attack hyper-parameters during training. This has the advantage of added stochasticity regularizing training and not over-fitting to a particular attack, providing improved robustness at test time.

5 Experiments

We conduct experiments on MNIST (23), Fashion-MNIST (F-MNIST) (24) and CIFAR10 (25). We use SimpleNet (47) as it provides comparable performance as, e.g., VGG (48), with limited number of weights: roughly 5.5M on CIFAR10 vs. 14M for VGG16. On MNIST and F-MNIST, we halve all channel widths, resulting in roughly 1M weights. Additionally, we use group normalization (GN) (49) instead of batch normalization (BN) (50), as we found BN to reduce robustness significantly. We use \( m = 16 \) bits for quantization (during training and for injecting bit errors).

We report (clean) test error \( \text{Err} \) (lower is better, \( \downarrow \)), corresponding to clean weights, and robust test error \( \text{RErr} \) (\( \downarrow \)), the test error on perturbed weights, on 9000 test examples. For random bit errors with rate \( p \) in %, we report average \( \text{RErr} \) and its standard deviation across 50 samples of random bit errors with rate \( p \), simulating 50 different chips. Random bit error training (RandBET) uses \( \lambda = 1 \) in Eq. (5) and a fixed error rate \( p \) (for evaluation, \( p \) might be different). In contrast to (15), we do not change \( p \) during training. For adversarial bit errors, we report worst-case \( \text{RErr} \) and run 14 attacks with varying step sizes/gradient normalization/backtracking, three random restarts each (3 \( \times \) 14 = 42 individual attacks) and up to \( T = 100 \) iterations, computed on 100 held-out test examples. In adversarial bit error training (AdvBET), we use \( T = 10 \) iterations, randomize step size/gradient normalization/backtracking, consider both \( \lambda = 0 \) as well as \( \lambda = 1 \) and disable learnable scale/bias of group normalization.
Random Bit Errors on MNIST with $w_{max} = 0.1$

| Training, $p$ in % | $Err$ in % ↓ | $Average$ $RErr$ in % ↓, $p$ for evaluation in % |
|-------------------|-------------|-----------------------------------------------|
| NORMAL, $w_{max} = 1$ | 0.36 | 89.96 ± 1.41 | $90.21 ± 1.23$ |
| NORMAL | 0.29 | 89.92 ± 1.24 | $90.89 ± 1.17$ |
| RANDBET, $p = 1.5$ | 0.30 | 0.33 ± 0.02 | $0.52 ± 0.06$ |
| RANDBET, $p = 2.5$ | 0.37 | 0.39 ± 0.02 | $0.51 ± 0.04$ |
| ADVBET$_{λ=1}$, $p = 0.01$ | 0.49 | 0.51 ± 0.01 | $0.60 ± 0.03$ |

Random Bit Errors on F-MNIST with $w_{max} = 0.25$

| Training, $p$ in % | $Err$ in % ↓ | $Average$ $RErr$ in % ↓, $p$ for evaluation in % |
|-------------------|-------------|-----------------------------------------------|
| NORMAL, $w_{max} = 1$ | 5.37 | 14.87 ± 4.05 | $19.04 ± 1.62$ |
| NORMAL | 5.58 | 6.44 ± 0.14 | $8.87 ± 2.14$ |
| RANDBET, $p = 0.1$ | 5.57 | 6.03 ± 0.09 | $7.73 ± 0.31$ |
| RANDBET, $p = 0.5$ | 6.19 | 6.44 ± 0.05 | $7.22 ± 0.17$ |
| ADVBET$_{λ=1}$, $p = 0.005$ | 8.44 | 8.70 ± 0.08 | $9.47 ± 0.17$ |

Random Bit Errors on CIFAR10 with $w_{max} = 0.15$

| Training, $p$ in % | $Err$ in % ↓ | $Average$ $RErr$ in % ↓, $p$ for evaluation in % |
|-------------------|-------------|-----------------------------------------------|
| NORMAL, $w_{max} = 1$ | 8.32 | 27.39 ± 3.67 | $90.93 ± 0.53$ |
| NORMAL | 8.13 | 8.87 ± 0.12 | $51.31 ± 7.91$ |
| RANDBET, $p = 0.5$ | 8.23 | 8.63 ± 0.06 | $9.63 ± 0.17$ |
| RANDBET, $p = 1$ | 8.89 | 9.27 ± 0.08 | $12.59 ± 0.38$ |
| ADVBET$_{λ=1}$, $p = 0.001$ | 10.11 | 10.72 ± 0.12 | $22.40 ± 2.03$ |

Table 2: Random Bit Errors. Clean test error $Err$ and average robust test error $RErr$ for 50 samples of random bit errors of rate $p$. For $RErr$, we also report the standard deviation (in gray). RANDBET, with $λ = 1$, allows to operate with higher bit error rates, i.e., at lower voltages: $p = 2.5\%$ on MNIST and $p = 0.1\%$ on F-MNIST/CIFAR10 are tolerable. ADVBET, although trained with significantly fewer adversarial bit errors, generalizes to more, but random bit errors.

We refer to our supplementary material for more details on our error models and additional experiments regarding clipping, baselines, batch normalization, and bit error training.

5.1 Evaluation on Random Bit Errors

Clipping: Tab. 1 shows the impact of aggressive clipping, i.e., reducing $w_{max}$, on $Err$ and $RErr$ against random bit errors. Both on MNIST and F-MNIST, reducing $w_{max}$ clearly improves robustness: clipping at $w_{max} = 0.05$ on MNIST yields 1.3% $RErr$ against bit errors with probability $p = 0.1\%$. However, as shown on F-MNIST (in red), extreme clipping can increase test error: $w_{max} = 0.2$ with 6.26% $Err$ compared to 5.37% with $w_{max} = 1$ (i.e., no aggressive clipping). Similarly, clipping can reduce predicted confidences as shown in Tab. 1 (right) for MNIST and $w_{max} = 0.1$ where the confidences are limited to $≈ 0.7$. Clipping is also essential for successfully training with bit errors, i.e., RANDBET, as shown on F-MNIST where training with $p = 1\%$ bit errors and without aggressive clipping, i.e., $w_{max} = 1$, increases $Err$ to 10.24%. We provide additional experiments on the influence of clipping (logit distribution, activations etc.) in the supplement. Overall, we chose $w_{max} = 0.1$ on MNIST, 0.25 on F-MNIST and 0.15 on CIFAR10.

Baseline: To emulate a robust DNN for a specific chip and operating voltage, similar to [12] [15], the rate $p$ and spatial distribution of bit errors is fixed for training and testing. A DNN trained with $p = 1\%$ on MNIST obtains 1.3% $RErr$ when tested against the same bit errors. However, $RErr$ increases to 86% for the same model during testing with lower rate $p = 0.1\%$. This is uninformative as the bit errors at $p = 0.1\%$ constitute a subset of those at $p = 1\%$. Moreover, $RErr$ increases to 90% on injecting random bit patterns during testing with $p = 1\%$. We suspect that DNNs treat fixed bit errors as “additive biases” and start to rely on them, see the supplement for more results. Thus, there is no generalization to other bit error patterns, i.e., other chips/memory arrays or operating voltages. Voltage, however, is usually controlled dynamically [13] and training a model for each operating voltage and chip is clearly infeasible.

Bit Error Training: Tab. 2 reports average $RErr$ on random bit errors for different error rates $p$ for training and evaluation. The shown bit error rates $p$ for training (in blue) are chosen to keep $Err$ close
We studied random and adversarial bit errors on (quantized) DNN weights. Random bit errors occur in SRAM and DRAM of DNN accelerators when operating with low voltage in order to save energy, e.g., [13, 15, 12]. Additionally, random bit errors can be provoked by an adversary maliciously reducing voltage. Adversarial bit errors have been shown realistic in recent work [56] and, thus, pose a severe security threat. We made first steps towards training DNNs robust to random and adversarial bit errors, by explicitly taking such errors into account during training. We obtain DNNs robust to random bit errors, allowing low-voltage operation at multiple operating voltages and across many chips with their unique bit error patterns. Furthermore, we can reduce the worst-case test error under adversarial bit attacks significantly, while additionally providing robustness to random bit errors from maliciously reduced voltage.

### 6 Conclusion

We studied random and adversarial bit errors on (quantized) DNN weights. Random bit errors occur in SRAM and DRAM of DNN accelerators when operating with low voltage in order to save energy, e.g., [13, 15, 12]. Additionally, random bit errors can be provoked by an adversary maliciously reducing voltage. Adversarial bit errors have been shown realistic in recent work [56] and, thus, pose a severe security threat. We made first steps towards training DNNs robust to random and adversarial bit errors, by explicitly taking such errors into account during training. We obtain DNNs robust to random bit errors, allowing low-voltage operation at multiple operating voltages and across many chips with their unique bit error patterns. Furthermore, we can reduce the worst-case test error under adversarial bit attacks significantly, while additionally providing robustness to random bit errors from maliciously reduced voltage.
Broader Impact

On the positive side, this paper aims at increasing robustness of deep neural networks (DNNs) which we consider as an important goal to ensure positive impact of machine learning on our society. In particular, robustness against bit errors, as discussed in this paper, has the potential to lead to improved energy-efficiency of DNN accelerators due to low-voltage operation. Obviously, improved energy-efficiency while maintaining the same prediction performance is a desirable goal.

On the negative side as we are discussing defenses against adversarial manipulation of the DNN weights on a bit-level we also have to discuss attacks to challenge the defense. Thus, we introduce and discuss bit-level adversarial attacks on the weights which, in principle, could be abused to attack an “undefended” model. However, this kind of conflict is unavoidable when discussing security relevant issues of machine learning systems.

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A Overview

In the main paper, we studied the impact of random and adversarial bit errors on quantized deep neural network (DNN) weights. Random bit errors occur when optimizing DNN accelerators for energy efficiency [6, 11, 12, 13], while adversarial bit errors are motivated through recent attacks on accelerator memory [8, 9]. As first steps towards obtaining robust DNNs, we proposed random bit error training (RANDBET) and adversarial bit error training (ADV BET) leading to more robust DNNs and potentially improving energy-efficiency and security of DNN accelerators. This document provides further details on our random and adversarial bit error models and includes additional results regarding clipping, batch normalization, baselines, and our bit error training.

Outline: In Sec. B we discuss our introductory figure from the main paper in more detail, i.e., regarding the measurements for SRAM energy consumption. After a discussion of related work in the broad areas of adversarial robustness, fault tolerance, backdooring and quantization, we discuss our random and adversarial bit error models in more depth, cf. Sec. D.2 and Sec. D.3 respectively. Finally, Sec. E contains additional details on the experimental setup, in Sec. E.1 and further experiments: Results regarding clipping in Sec. E.2, a discussion of batch normalization in Sec. E.3, more results on random bit errors in Sec. E.4 and adversarial bit errors in Sec. E.5.

B Energy Savings in Figure 1

Fig. 3 corresponding to Fig. 1 of the main paper, shows bit error rate characterization results of SRAMs in the DNN accelerator chip described in [13], fabricated using 14nm FinFET technology. The average bit error rate is measured from 32 SRAMs, each SRAM array of size 4KB (512 × 64 bit), as supply voltage is scaled down. Bit error rate p (in %) at a given supply voltage is measured as the count of read or write bit cell failures averaged over the total number of bit cells in the SRAM. A bit cell failure refers to reading 1 on writing 0 or reading 0 on writing 1. For a more comprehensive characterisation of SRAMs in 14nm technology, the reader is referred to [6]. Fig. 3 also shows the energy per write and read access of a 4KB (512 × 64 bit) SRAM, obtained from Cadence Spectre simulations. Energy is obtained at the same constant clock frequency at all supply voltages. The voltage (x-axis) shown is normalized over $V_{min}$ which is the lowest measured voltage at which there are no bit cell failures. Energy shown in the graph (secondary axis on the right) is also normalized over the energy per access at $V_{min}$.

Accelerators such as [1, 2, 13, 14, 5, 3, 4] have a large amount of on-chip SRAM to store weights and intermediate computations. Total dynamic energy of accelerator SRAMs can be obtained as the total number of SRAM accesses × energy of a single SRAM access. Optimized dataflow in accelerators leads to better re-use of weights read from memories in computation, reducing the number of such memory accesses [1][2][5]. Low voltage operation focuses on reducing the memory access energy, leading to significant energy savings as shown.
C Related Work

In the following, we briefly review work on adversarial robustness, fault tolerance, backdooring, and quantization. These areas are broadly related to the topic of the main paper.

Adversarial and Corruption Robustness: Robustness of DNNs against adversarially perturbed or randomly corrupted inputs received considerable attention in recent years, see, e.g., relevant surveys \[54, 55\]. Adversarial examples \[56\], i.e., nearly imperceptibly perturbed inputs causing misclassification, consider an adversarial environment where potential attackers can actively manipulate inputs. This has been shown to be possible in the white-box setting, with full access to the DNN, e.g., \[28, 57, 58, 59, 60\], as well as in the black-box setting, without access to DNN weights and gradients, e.g., \[61, 62, 63, 64\]. Such attacks are also transferable between models \[65\] and can be applied in the physical world \[66, 67\]. Obtaining robustness against adversarial inputs is challenging, recent work focuses on achieving certified/provable robustness \[68, 69, 70, 71\] and variants of adversarial training \[72, 73, 28\], i.e., training on adversarial inputs generated on-the-fly. Adversarial training has been shown to work well empirically, and flaws such as reduced accuracy \[74, 75\] or generalization to attacks not seen during training has been addressed repeatedly \[76, 77, 45, 78, 79\]. Adversarial inputs have also been considered for quantized DNNs \[80\]. Corrupted inputs, in contrast, consider “naturally” occurring corruptions to which robustness/invariance is desirable for practical applications. Popular benchmarks such as MNIST-C \[81\], Cifar10-C or ImageNet-C \[82\] promote research on corruption robustness by extending standard datasets with common corruptions, e.g., blur, noise, saturation changes etc. It is argued that adversarial robustness, and robustness to random corruptions is related. Approaches are often similar, e.g., based on adversarial training \[45, 83, 84\]. In contrast, we consider random and adversarial bit errors in the weights, not the inputs. Nevertheless, our adversarial bit error training is similar to adversarial training.

Fault Tolerance: Fault tolerance, describes structural changes such as removed units, and has been studied in early works such as \[26, 27\]. These approaches obtain fault tolerant NNs using approaches similar to adversarial training \[27, 26, 85\]. Recently, weight dropping regularization \[86\] or GAN-based training \[87\] has been explored. Additionally, fault tolerance of adversarially robust models has been considered in \[88\]. We refer to \[89\] for a comprehensive survey. In contrast to such works, we do not consider structural changes/errors in DNNs.

Backdooring: The goal of backdooring is to introduce a backdoor into a DNN, allowing to control the classification result by fixed input perturbations at test time. This is usually achieved through data poisoning \[90, 91, 92\]. However, some works also consider directly manipulating the weights \[29, 30\]. However, such weight perturbations are explicitly constructed not to affect accuracy on test examples without backdoor. In contrast, we consider random or adversarial bit errors (i.e., weight perturbations) that degrade accuracy significantly.

Quantization: Due to their high applicability, efficient architectures \[93, 94, 95\], compression of DNN weights \[96, 97\] and DNN quantization, see \[98\], received considerable attention. While compression mainly focuses on reducing space requirements, quantization is usually motivated by more efficient DNN inference, e.g., through fixed-point quantization and arithmetic \[31, 32, 33\]. To avoid reduced accuracy, quantization is considered during training \[18, 99\], enabling low-bit quantization such as binary DNNs \[37, 100\]. Some works also consider quantizing activations \[37, 38, 39\] or gradients \[40, 101, 42\]. Finally, works such as \[17, 18, 19, 20\] study the robustness of DNNs against quantization, however, not on bit-level. Following common practice in DNN accelerators \[13\], we use a deterministic fixed-point quantization for training and evaluation (i.e., injecting bit errors).

D Bit Errors in Quantized DNN Weights

We provide a more detailed discussion of the considered error models: random bit errors, induced through low-voltage operation of SRAM or DRAM commonly used on DNN accelerators \[12, 15\]; and adversarial bit errors, motivated through attacks on accelerator memory \[9\].
D.1 Fixed-Point Quantization of Weights

We consider a simple fixed-point quantization of the floating point weights $w \in [-w_{\text{max}}, w_{\text{max}}]$. The range $[-w_{\text{max}}, w_{\text{max}}]$ is quantized using $m$ bits into bins of width

$$\Delta = \frac{w_{\text{max}}}{2^{m-1} - 1} \quad (7)$$

where $w_{\text{max}}$ is the maximum absolute weight that can be chosen based on the a pre-trained model or pre-determined. In our case, as we train with quantization, we pre-determine $w_{\text{max}}$ and additionally reduce it aggressively to improve robustness against bit errors as discussed in Sec. 2. The quantized weights $v := Q(w)$ are signed $m$-bit integers (in two’s complement representation) corresponding to the underlying bits. The quantization function $Q : \mathbb{R} \mapsto \{-2^{m-1}, \ldots, 2^{m-1} - 1\}$ is defined as

$$Q(w) = \left\lfloor \frac{\max(-w_{\text{max}}, \min(w_{\text{max}}, w))}{\Delta} \right\rfloor \quad \text{and} \quad Q^{-1}(v) = v \cdot \Delta \quad (8)$$

Note that quantization includes clipping the weights to $[-w_{\text{max}}, w_{\text{max}}]$ before quantization. Thus, by construction, $Q^{-1}(Q(w_i)) \in [-w_{\text{max}}, w_{\text{max}}]$.

D.2 Low-Voltage Bit Errors

Work such as [13, 15] model the effect of low-voltage induced bit errors using two parameters: the probability $p_{\text{flt}}$ of bit cells in accelerator memory, e.g., SRAM or DRAM, being faulty and the probability $p_{\text{err}}$ that a faulty bit cell results in a bit error on access. Following measurements in works such as [11, 12], we assume that these errors are not transient errors by setting $p_{\text{err}} = 100\%$ such that the overall probability of bit errors is $p := p_{\text{flt}} \cdot p_{\text{err}} = p_{\text{flt}}$. In doing so, we consider the worst-case where faulty cells always induce bit errors. However, the noise model from the main paper remains valid for any arbitrary but fixed $p_{\text{err}} \neq 100\%$. For the reminder of this document, we assume the probability of bit error $p = p_{\text{flt}}$, with $p_{\text{err}} = 100\%$, as in the main paper. In the following, we describe the two parameters, $p_{\text{flt}}$ and $p_{\text{err}}$, in more details.

Faulty Bit Cells. Due to variations in the manufacturing process, SRAM bit cells become more or less vulnerable to low-voltage operation. For a specific voltage, the resulting bit cell failures can be
assumed to be random and independent of each other. We assume a bit to be faulty with probability $p_{flt}$ increasing exponentially with decreased voltage $\epsilon$ [6,11,12,13]. Furthermore, the faulty bits for $p_{flt} \leq p_{err}$ can be assumed to be a subset of those for $p_{flt}$ [11]. For a fixed chip, consisting of multiple memory arrays, the faulty cells are pre-determined through the manufacturing process, i.e., the pattern (spatial distribution) of faulty cells is fixed for a specific supply voltage. Across chips/memory arrays, however, faulty cells are assumed to be random and independent of each other.

**Bit Errors in Faulty Bit Cells:** Faulty cells may cause bit errors with probability $p_{err}$ upon read/write access. We note that bit errors read from memory affect all computations performed on the read weight value. We assume that a bit error flips the currently stored bit, where flips 0-to-1 and 1-to-0 are assumed equally likely.

**Illustration:** The impact of random bit errors on quantized weights is illustrated in Fig. 4 (top) on F-MNIST and MNIST for bit error rate $p = 1\%$. Here, the diagonal in violet represents zero error (i.e., no bit errors) while large absolute errors are depicted in yellow. For $p = 1\%$, the majority of the roughly 1M weights are not affected by bit errors. Additionally, the separation between positive and negative weights is clearly visible: bit errors not affecting the most significant bit (MSB) do not change the sign. Nevertheless, few bit errors can easily induce large errors, as shown in the weight difference histogram, Fig. 4 (bottom right): many weight values are changed by more than half of the quantization range, i.e., absolute errors of at least $w_{max}$. Overall, random bit errors result in a unique error pattern, significantly different from Gaussian, $L_p$ or quantization errors studied in related work [16,21,17,18,19,20].
Table 5: Clipping and Random Bit Errors. Average RErr against random bit errors with rate \( p \) considering varying degrees of clipping, i.e., reducing the quantization range \([-w_{\max}, w_{\max}]\). RANDBET was trained on \( p = 1\% \) (in blue). Clipping aggressively clearly improves robustness: RErr against random bit errors with \( p = 0.1\% \) and \( p = 1\% \) may decrease significantly. However, test error might increase for small \( w_{\max} \) (in red) and confidences might be constrained, as seen in an increased cross-entropy loss \( L \) on test examples (also red).

### D.3 Adversarial Bit Errors

As introduced in the main paper, our adversarial bit error attack can be formulated as the following optimization problem on a fixed mini-batch of examples \((x_b, y_b)\)_{\text{b}=1}^{B}:

\[
\max_{\tilde{v}} \sum_{b=1}^{B} L(f(x_b; Q^{-1}(\tilde{v})), y_b) \quad \text{s.t.} \quad d_H(\tilde{v}, v) \leq \epsilon, \quad d_H(\tilde{v}_i, v_i) \leq 1
\]

(9)

where \( \tilde{v} \) are the quantized weights (signed \( m \)-bit integers) and \( d_H \) denotes the (bit-level) Hamming distance. The total number of bit errors \( d_H(\tilde{v}, v) \) is constrained by \( \epsilon := \lfloor pmW \rfloor \) for a bit error rate \( p \), and we allow at most one bit error per weight value, i.e., \( d_H(\tilde{v}_i, v_i) \leq 1 \). These constraints are enforced through projection, after iteratively computing:

\[
\tilde{w}^{(t+1)} = \tilde{w}^{(t)} + \gamma \Delta^{(t)} \quad \text{with} \quad \Delta^{(t)} = \sum_{b=1}^{B} L(f(x_b; \tilde{w}^{(t)}_q), y_b), \quad \tilde{w}^{(t)}_q = Q^{-1}(Q(\tilde{w}^{(t)}))
\]

(10)

where \( \gamma \) is the step size. We note that the forward pass is performed on the de-quantized weights \( \tilde{w}^{(t)}_q = Q^{-1}(Q(\tilde{w}^{(t)})) \), while the update is performed in floating point.

The projection after the update of Eq. (10) requires solving the following optimization problem:

\[
\min_{\tilde{v}} \|Q^{-1}(\tilde{v}) - Q^{-1}(\tilde{v}^\prime)\|_2^2 \quad \text{s.t.} \quad d_H(\tilde{v}_i, v_i^\prime) \leq 1, \quad d_H(v, \tilde{v}^\prime) \leq \epsilon
\]

(11)

where we dropped the superscript \( t \) for simplicity. Here, \( \tilde{v} = Q(\tilde{w}) \) are the quantized, perturbed weights after Eq. (10) and \( \tilde{v}^\prime = Q^{-1}(\tilde{v}) \) will be the projected weights. As the objective and the constraint set are separable, this problem can be divided into the following two problems: First, we rank the weights by their corresponding changes

\[
|Q^{-1}(Q(w_i)) - Q^{-1}(\tilde{v}_i)| = |w_i - \tilde{w}_i|
\]

(12)

where \( w \) are the original, clean weights and \( \tilde{w}_i \) the corresponding de-quantized weights. Then, only the top-\( \epsilon \) changes are kept. All other perturbed weights \( \tilde{w}_{i,q} \) are reset to the original, clean weights \( w_{i,q} \). For the selected weights, only the most significant changed bit is kept. In practice, considering \( \tilde{v}_i \) and \( v_i \) from Eq. (11) corresponding to one of the top-\( \epsilon \) changes, if \( d_H(\tilde{v}_i, v_i) > 1 \), only the highest changed bit is kept. In practice, this can be implemented (and parallelized) easily on the signed \( m \)-bit integers \( \tilde{v}_i \) and \( v_i \), while computing the (bit-level) Hamming distance \( d_H \).

The optimization problem Eq. (9) is challenging due to the non-convex constraint set that we project onto after each iteration. Therefore, we use several random restarts, each initialized by randomly selecting \( k \in [0, \epsilon] \) bits to be flipped in \( v \) to obtain \( \tilde{v}^{(0)} \). We note that initialization by randomly flipping bits is important as, without initialization, i.e., \( \tilde{v}^{(0)} := v \), the loss \( L \) in Eq. (9) will be close to zero. We also found that initializing with \( k = \epsilon \) leads to difficulties in the first few iterations, which is why we sample \( k \in [0, \epsilon] \) uniformly. Additionally, we normalize the gradient \( \Delta^{(t)} \) in Eq. (10) following [44]:

\[
\tilde{\Delta}^{(t)} = \frac{\Delta^{(t)}}{\|\Delta^{(t)}\|_1}, \quad \bar{\Delta}^{(t)} = \frac{\Delta^{(t)}}{\max_i |\Delta^{(t)}|}
\]

(13)
Figure 5: Impact of Clipping on Logits and Confidences. We plot normalized logit and confidence histograms where the confidence is $\max_k f_k(x; w)$, i.e., the maximum predicted probability, and we plot normalized histograms. For logits, we plot all logits, resulting in bi-modal histograms. We considered 5000 test examples. In blue, we show confidence/logits on clean, unperturbed weights; in red, we plot confidence/logits on perturbed weights (i.e., with bit errors). On MNIST, for example, we use $w_{\max} = 0.1$ for our experiments. This is justified by the significantly reduced confidences for $w_{\max} = 0.05$, even though $w_{\max} = 0.05$ could potentially increase robustness further.

...before applying the update, i.e., $\tilde{w}^{(t+1)} = \tilde{w}^{(t)} + \gamma \hat{\Delta}^{(t)}$. Additionally, we apply backtracking [45]: Using an additional forward pass in each iteration, we evaluate whether $\tilde{w}^{(t+1)}$ actually increases the cross-entropy loss $\mathcal{L}$ after projection compared to the previous iterate $\tilde{w}^{(t)}$. The update is kept, only if this is the case. Otherwise, $\tilde{w}^{(t+1)}$ is rejected and the step size $\gamma$ is divided by $\beta > 1$. Finally, instead of considering $\tilde{w}^{(T)}$, i.e., the perturbed weights after exactly $T$ iterations, we use

$$
\tilde{w}^{(t^*)} \quad \text{with} \quad t^* = \argmax_t \sum_{b=1}^B \mathcal{L}(f(x_b; \tilde{w}^{(t)}), y_b)
$$

instead. Nevertheless, despite these optimization tricks, the attack remains very sensitive to hyper-parameters, especially regarding the step-size. Thus, in practice, we use varying step sizes, with or without gradient normalization and backtracking and use several random restarts.

E Experiments

In the following, for reproducibility, we discuss our experimental setup in more detail. Subsequently, we include additional experiments regarding clipping, batch normalization, baselines as well as random and adversarial bit error training.
Table 6: Random Bit Errors with Batch Normalization (BN) and ResNets. We report Err, the robust cross-entropy loss $\mathcal{L}$ (i.e., with bit errors) and RErr for normal training and random bit error training (RANDBET) with various configurations of BN [50] (in red) and architectures. We consider SimpleNet with group normalization (GN) [49] or BN and ResNets [51] with BN (also in red): ResNet-20 on MNIST/F-MNIST on CIFAR10. RANDBET is trained using $p = 1.5\%$ on MNIST and $p = 0.5\%$ on F-MNIST/CIFAR10 (marked in blue). As can be seen, using BN or ResNets, which are dependent on BN for reliable training [52], results in considerably worse RErr in all cases.

### E.1 Experimental Setup

**Datasets:** We conduct experiments on MNIST [23], Fashion-MNIST (F-MNIST) [24] and CIFAR10 [25]. MNIST consists of 60k training and 10k test images. These are gray-scale and of size $28 \times 28$ pixels. Similarly, F-MNIST consists of 60k training and 10k test images of size $28 \times 28$ pixels. Finally, CIFAR10 consists of 50k training and 10k test images of size $32 \times 32 \times 3$ (i.e., color images). All three datasets represent classification tasks with 10 classes.

**Architecture:** The used SimpleNet architectures [47] for MNIST/F-MNIST and CIFAR10 are summarized in Tab. 4 including the total number of weights $W$. On CIFAR10, this results in a total of roughly $W \approx 5.5M$ weights. Due to a lower resolution on MNIST and F-MNIST, channel width in each convolutional layer is halved, and one stage of convolutional layers including a pooling layer is skipped. This results in a total of roughly $W \approx 1M$ weights. In both cases, we replaced batch normalization (BN) [50] with group normalization (GN) [49]. The learnable scale/bias parameters of group normalization make up for less than $10k \approx 0.15\% \cdot W$ of the weights on CIFAR10. Tab. 4 also includes the expected/maximum number of bit errors given various rates $p$ for random/adversarial bit errors. Regarding the number of weights $W$, SimpleNet compares favorably to, e.g., VGG [48]: VGG-16 has 14M weights on CIFAR10. Additionally, we found SimpleNet to be easier to train without BN, which is desirable as BN reduces robustness to bit errors significantly, cf. Sec. E.3. This is also the reason why we do not use ResNets [51], which depend strongly on BN [52].

**Training:** For training, we use stochastic gradient descent in order to minimize cross-entropy loss, with batch size 100, learning rate 0.01, momentum 0.9, weight decay 0.0005 and learning rate decay of 0.98 for 100, 150 and 200 epochs on MNIST, F-MNIST and CIFAR10, respectively. Initialization follows [102]. We implemented architectures and training in PyTorch [103]. On all datasets, the full training set is used for training and we do not use early stopping. For adversarial bit error training (ADVBET), we reduce the learning rate to 0.005, clip gradients to $[-0.05, 0.05]$, and disable learnable scale/bias in GN. We randomize the step size $\gamma$ in Eq. 9 over $\{0.1, 1, 3\}$ and also randomize over backtracking and gradient normalization (i.e., with or without). As for random bit error training (RANDBET), we start injecting bit errors whenever the loss reduced below 1.75.

**Random Bit Errors:** Following Sec. D.2, we simulate 50 different chips with multiple memory arrays, by drawing uniform samples $u_c \sim U(0, 1)^W \times m$ for each chip $c$ and all $m$ bits for a total of $W$ weights. Then, for chip $c$, bit $j$ in weight $w_i$ is flipped iff $u_{ij}^{(c)} \leq p$. This assumes a linear memory layout of all $W$ weights. The pattern, i.e., spatial distribution, of bit errors for chip $c$ is fixed by $u^{(c)}$, while across all 50 chips, bit errors are uniformly distributed. We emphasize that we pre-determine $u^{(c)}$, $c = 1, \ldots, 50$, once for all our experiments. Thus, our robustness results are

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http://yann.lecun.com/exdb/mnist/
https://github.com/zalandoresearch/fashion-mnist
https://www.cs.toronto.edu/~kriz/cifar.html
https://pytorch.org/
| Fixed Bit Error Pattern on MNIST | F-MNIST | CIFAR10 |
|---------------------------------|---------|---------|
| Training, $p_m$ in % | $p_n=0.1$ | $p_n=1$ | $p_n=0.1$ | $p_n=1$ | $p_n=0.1$ | $p_n=1$ |
| $p = 0.1$ | $p = 1$ | $p = 0.1$ | $p = 1$ | $p = 0.1$ | $p = 1$ |
| $p_{ATT} = 0.1$ | $p_{ATT} = 1$ | $p_{ATT} = 0.1$ | $p_{ATT} = 1$ | $p_{ATT} = 0.1$ | $p_{ATT} = 1$ |

Table 7: Chip-Specific Baselines. We consider training on a fixed pattern ($p_{ATT} = 0.1$) of bit errors, corresponding to chip-specific training as in [12,15], as briefly discussed in the main paper. We report average $RErr$ against the same, fixed bit error patterns, as well as random bit errors. As shown, $p_{ATT} = 0.1$ does not generalize to lower bit error rates, e.g., when trained on $p = 1\%$ but tested against a subset of the same bit errors with $p = 0.1\%$ (in red), as well as completely random bit errors.

Adversarial Bit Errors: During evaluation, we consider the worst-case across step sizes 0.1, 0.5, 1, 3 and with and without backtracking, $T = 20$ iterations and three random restarts; for step sizes 0.5 and 1 we additionally consider $T = 100$ iterations. This totals 14 attacks with 3 restarts, i.e., $14 \cdot 3 = 42$ individual attacks. We consider error rates $p \in \{0.0001, 0.0005, 0.001, 0.01, 0.05\}$, where adversarial bit errors are constrained to $\epsilon = |pw|W$. The corresponding values for $\epsilon$ are summarized in Tab. 4. Furthermore, for $p' < p$, all attacks computed for $p'$ are included in the evaluation of $p$. e.g., evaluating robustness against $p = 0.0005$ includes 2·42 individual attacks for $p = 0.0005$ and $p = 0.0001$. For $T = 20$ iterations, we use $\beta = 2$ for backtracking; for $T = 100$, we use $\beta = 1.5$, cf. Sec. 3.3. Adversarial bit error attacks are computed, i.e., “trained”, on one mini-batch of size 100 corresponding to the last 10 test examples.

Metrics: We report (clean) test error $Err$, computed as the fraction of mis-classified test examples on clean, unperturbed weights, and robust test error $RErr$, computed as the test error on perturbed weights (i.e., after injecting random or adversarial bit errors). Both are computed on the first 9000 test examples of each dataset. For random bit errors, we report average $RErr$ and its standard deviation in % across 50 samples of random bit errors of rate $p$. Regarding adversarial bit errors, we report worst-case $RErr$ across all attacks, corresponding to the maximum $RErr$ across all attacks.

Quantization: We use the fixed-point quantization outlined in Sec. 4.1 using $n = 16$ bits in all our experiments, i.e., both for training and injecting random/adversarial bit errors. Bit error injecting was implemented as custom modules for PyTorch in C/CUDA and directly operates on the $m$ bit signed integer representation of quantized weights, i.e., $v_i = Q(w_i) \in \{2^{m-1}, \ldots, 2^{m-1} - 1\}$. When using BN with quantization, as the forward pass is performed using the “de-quantized model” $w_q = Q^{-1}(Q(w))$ while the update is applied to the corresponding “floating-point model” $w$, the statistics need to be updated accordingly. As Eq. (8) includes clipping the weights to $[-w_{max}, w_{max}]$, this clipping needs to be applied to the floating point weights $w$, as well.

E.2 Clipping

In Tab. 5, we report additional results regarding more aggressive clipping, i.e., reducing $w_{max}$ to obtain robustness against random bit errors. Specifically, we report average $RErr$ against random bit errors with probability $p = 0.1\%$ and $p = 1\%$. Complementary, Fig. 5 shows the corresponding logit and confidence histograms. As shown, clipping can improve robustness significantly: on MNIST and CIFAR10, normal training with clipping ($w_{max} = 0.05$ and $w_{max} = 0.1$, respectively) yields 1.3\% and 11.07\% $RErr$ against $p = 0.1\%$. This is close to RANDBET. However, in all cases, extreme clipping leads to an increased test error (marked in red). This is supported by Fig. 5 showing reduced logits and confidences for very low $w_{max}$, i.e., overly aggressive clipping. This also results in a significantly higher cross entropy loss $\mathcal{L}$ in Tab. 5. Intuitively, with extremely constrained weights, the DNN is not able to obtain large logits in order to reduce the loss during training. On more difficult datasets such as F-MNIST and CIFAR10 this leads to an increase in $Err$. We also found that the logits...
from clean, unperturbed weights and those from perturbed weights with bit errors have more overlap when clipping aggressively, e.g., for $w_{\text{max}} = 0.05$ on MNIST.

### E.3 Batch Normalization

Table 8: **Random Bit Errors.** We report average-case RErr on MNIST, F-MNIST and CIFAR10, with complementary results not included in the main paper. In addition to random bit errors with rate $p$ in %, we also evaluate against bit errors in most-significant bits (MSBs): for bit error rate $p$, we only keep the bit errors in MSBs, on average resulting in $p/m\%$ bit errors, where $m = 16$ is the number of bits per weight value. We also use bit errors in MSBs during training (MSBBET). RANDBET tends to increase Err with larger $p$. However, RANDBET does not generalize to “more” (i.e., higher $p$) bit errors than seen during training, creating a trade-off between RErr and Err. Also, a significant part of the RErr on random bit errors is, in fact, caused by bit errors in MSBs.
As shown, both Table 9: Adversarial Bit Errors. A p errors with rate p u this is achieved by considering Tab. 7 reports results of our chip-specific baselines, similar to [12, 15]. In this scenario, E.4 Random Bit Errors Overall, these experiments demonstrate that DNNs utilizing BN are significantly less robust against 9 and CIFAR10, RErr roughly doubles for 0 . However, it does not generalize to larger error rates. Furthermore, ADVBET proved difficult to train for large rates, e.g., 69%. against bit error rate 74%. ADVBET is able to improve robustness significantly for adversarial bit error rates p seen during training, or lower. However, it does not generalize to larger error rates. Furthermore, ADVBET proved difficult to train for large rates, e.g., p = 0.05% on MNIST or p = 0.01% on F-MNIST. Except on F-MNIST, training only on adversarial bit errors, i.e., λ = 0, results in better robustness compared to λ = 1, however, also increases Err. from 0.69% to 9.74% against bit error rate p = 1.5% which is also used for training. On F-MNIST and CIFAR10, RErr roughly doubles for p = 0.5% (also used for training). Worse results are shown for ResNets. For example, on MNIST, RErr increases further from 9.74% to 26% RErr for p = 1.5%. Overall, these experiments demonstrate that DNNs utilizing BN are significantly less robust against random bit errors, justifying our choice of using SimpleNet with GN.

E.4 Random Bit Errors

Baseline: Tab. 7 reports results of our chip-specific baselines, similar to [12, 15]. In this scenario, we fix the bit error pattern, i.e., the spatial distribution, for both training and evaluation. In practice, this is achieved by considering w(1) only, cf. Sec. E.1 We train and evaluate with p = 0.1% and p = 1% where the bit error pattern for p = 0.1% is a subset of the pattern corresponding to p = 1%. As shown, (fixed) bit error pattern training (PATTBET) with p = 1% does not generalize to bit errors with rate p = 0.1%, as marked in red. On MNIST, as mentioned in the main paper, RErr
is 1.3% against \( p = 1\%\), but increases to 86% for \( p = 0.1\%\). This is surprising as the DNN “saw” all bit errors for \( p = 0.1\%\) during training. Thus, we suspect that DNNs treat fixed bit errors as “additive biases” in the corresponding weight values. For example, a bit error in the least significant bit (LSB) of a weight value results in a constant, additive bias of \( \pm \Delta\), cf. Eq. (7), depending on the sign bit. As weight values do not change their sign frequently during training, this bias can be assumed fixed throughout training, allowing DNNs to overfit to particular bit error patterns. This prevents generalization to higher supply voltages, as would be necessary for, e.g., dynamic voltage scaling [13]. Tab. 7 also shows average RErr and its standard deviation when evaluated on random bit errors, i.e., considering all \( u^{(c)}\) in Sec. [E.1]. It becomes apparent, that PATTBET does not generalize to random bit errors, i.e., other chips. On all datasets, RErr increases to roughly 90%, even for \( p = 0.1\%\). This means that these DNNs need to be trained for specific voltages and chips. This, however, is clearly infeasible in practice.

Random Bit Error Training: Tab. 8 presents average RErr and its standard deviation (in gray) for random bit error training (RANDBET), complementing the results in the main paper. Specifically, we report results for various error rates \( p \) used for training (in blue) and evaluation. In red, we mark the RErr if RANDBET is trained and evaluated on the same bit error rate \( p \). As can be seen, RANDBET provides robustness against bit error rates lower or equal to \( p \), but generalizes poorly to significantly larger bit error rates. This is emphasized on F-MNIST and CIFAR10: for example, training with \( p = 0.1\%\) on F-MNIST yields 7.73% RErr against error rate \( p = 0.1\%\). However, RErr increases to 52.51% against \( p = 0.5\%\) and 88.46% against \( p = 1\%\). Additionally, standard deviation increases significantly. On F-MNIST and CIFAR10, Err is shown to increase quickly when training with more bit errors, i.e., higher bit error rate \( p \). On F-MNIST, training with \( p = 1.5\%\) results in 7.93% Err compared to 5.37% of a normally trained model without clipping (i.e., \( w_{\max} = 1\) ). Emphasizing the impact of bit errors in the most-significant bits (MSBs), we also report results against random bit errors in MSBs only, cf. right-most column. Here, for bit error rate \( p \), we only keep bit errors in MSBs, resulting in roughly \( p/16\) bit errors in total. Nevertheless, for \( p = 1\%\) on F-MNIST, bit errors in MSBs likely contribute most to the overall RErr: 10.78% considering only bit errors in MSBs, and 11.37% considering all, i.e., 16 times more, bit errors against RANDBET trained with \( p = 1.5\%\) (marked in bold). Vice-versa, random MSB bit error training (MSBBET), results in surprisingly robust models even though only \( 1/16\) of the bit errors are seen during training. Similarly, ADVBET provides robustness against (random) bit error rates \( p \) several magnitudes larger than seen during training.

E.5 Adversarial Bit Errors

In Tab. 9 we consider the worst-case RErr on adversarial bit errors. We mark in red, if adversarial bit error training (ADVBT) with \( \lambda = 0\) or \( \lambda = 1\) is trained and evaluated using the same error rate \( p \). On MNIST, we are able to train with significantly higher error rates compared to F-MNIST and CIFAR10. For example, \( p = 0.01\%\) corresponds to a maximum of \( \epsilon := [pmW] = 1727\) bit errors. However, our SimpleNet models on CIFAR10 also contain significantly more weights, such that even \( p = 0.001\%\) corresponds to \( \epsilon = 879\). On MNIST and F-MNIST, we show that we are not able to train ADVBET with \( p = 0.05\%\) and \( p = 0.01\%\), respectively. Additionally, ADVBET does not generalize to larger error rates than seen during training. Similar observations have been made using adversarial training on adversarial inputs [28]. Except for \( p = 0.005\%\) on F-MNIST, training only with adversarial bit errors (ADVBT\( _{\lambda=0}\)) results in lower RErr compared to training both on clean and perturbed weights (ADVBT\( _{\lambda=1}\)). However, ADVBT\( _{\lambda=0}\) increases Err significantly. This observation is also similar to training on adversarial inputs [24]. Finally, Tab. 8 shows that ADVBET can be trained to generalize to larger error rates \( p \), often in the order of two or three magnitudes, than seen during training as long as these errors are injected randomly. As result, ADVBET proves effective against both adversarially injected bit errors as well as adversarially reduced voltage.