Memristive Transfer Matrices
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ABSTRACT

An electrical analysis is performed for a memristor crossbar array integrated with operational amplifiers including the effects of parasitic or contact resistances. It is shown that the memristor crossbar array can act as a transfer matrix for a multiple input-multiple output signal processing system. Special cases of the transfer matrix are described related to reconfigurable analog filters, waveform generators, analog computing, and pattern comparison.

Keywords: transfer matrix, memristor, analog electronics, crossbar, operational amplifier, reconfigurable electronics

1 INTRODUCTION

The memristor (i.e. memory resistor) is a fundamental new type of circuit element offering dynamic capabilities beyond the static characteristics of ordinary resistors. Reference to the theoretical and practical development of memristive materials is given by [1-5]. It is notable that, while the memristance effect of TiO_2 has attracted much recent attention based on the publications from HPLabs, original research on the memory resistance effects of TiO_2 was performed in the 1960’s [6]. In addition, numerous other materials have long been known to exhibit memory resistance effects [7], although the connection to the later developed memristor theory was not realized until recently. It is also worth noting that a similarly named “memistor” was developed by Bernard Widrow and Ted Hoff in the 1960’s as a component of one of the first implementations of a neural network named ADALINE [8]. However, the Widrow-Hoff memistor was a 3-terminal device as opposed to the 2-terminal memristor and was implemented using an electroplating cell rather than solid state circuitry compatible with integrated circuit fabrication.

The most common applications suggested for memristors have so far been in the areas of non-volatile memory and neuromorphics. However, the market of non-volatile memory is well-developed with existing solutions that continue scaling despite the continual prediction of the end to Moore’s Law. In addition, many other more fully developed technologies such as phase change memory, FeRAM, and MRAM are also competing for non-volatile memory market share which will make it very difficult for a memristor solution to compete.

Memristive neuromorphics offers more promise as an emerging technology but, lacking an association with any existing market need, it has an unclear present value. More conventional analog electronics applications may offer an easier entry point for memristors into commercial products. There has been some analysis given toward general analog applications of individual memristors [9,10] as well as discussion of analog applications of memristor arrays arranged in a crossbar configuration [11,12]. However, there has been little analysis of memristor crossbar arrays integrated with analog electronics. Section 2 describes a design approach to analog circuitry based on memristor arrays in a crossbar configuration integrated with operational amplifiers. Section 3 includes an electrical analysis of the memristive transfer matrix. Section 4 describes special cases of the memristor transfer matrix for specific applications.

2 MEMRISTOR TRANSFER MATRIX

In modern control systems, transfer matrices are used to define a functional relationship between a set of input signals u_i(t) (0 ≤ i ≤ n) and a set of output signals y_j(t) (0 ≤ j ≤ m). For linear systems (or linear approximations of non-linear systems) this relationship may be written in the Laplace domain in terms of a matrix transformation:

\[ Y_j(s) = \sum_i T_{ij}(s)U_i(s) \]  

(1)

where T_{ij}(s) represents transfer matrix elements. For systems having a memory dependence the elements T_{ij} need to reflect this memory dependence. When building circuits using circuit elements such as resistors, capacitors, and amplifiers such memory effects are not readily achievable. Software controlled processors are more conventionally used to implement such a transfer matrix and can provide both adaptability and memory to the elements T_{ij}. However, for large matrices high operational speeds are required to simultaneously update the matrix elements and calculate new output signals resulting in a limit to real time response rates. This is in sharp contrast with the observed rate of firing of neurons in the human brain (<100Hz) which perform pattern recognition and real-time response in a fashion far superior to any known computer. The implementation of (1) using memristive junctions could provide memory to the elements T_{ij} thus integrating the adaptability of software solutions with the real time response of hardware.
For the purposes of this discussion a memristive junction is used to refer to a voltage-controlled memristive system junction defined by a generalized version of Ohm’s law relating a voltage signal \( v(t) \) and a current signal \( i(t) \) such that:

\[
i(t) = v(t)/R(w(t))
\]

(2)

where \( R(w(t)) \) is a memristance function dependent upon a state parameter \( w(t) \) defined in accordance with a differential equation having the form:

\[
\frac{dw(t)}{dt} = f(w(t), v(t))
\]

(3)

In terms of thin film materials the function \( f(w(t), v(t)) \) may either represent the voltage dependence of ionic or oxygen vacancy drift or the growth rate of metallic filaments in a thin film junction. Such functional dependence has been shown to obey an exponential dependence by [4] and, while high electric fields produce fast switching, small signals applied for short durations produce negligible alteration the state parameter (i.e. \( dw/dt=0 \)). Thus for small signals the memristive junction may be approximated as a linear resistor having a value dependent on the duration and amplitude of a previously applied large voltage signal.

Fig.1 illustrates a memory cell designed for applying both programming voltages and small signal voltages to a memristive junction. A memristive junction is indicated by an impedance value \( Z_\alpha(w) \) accounting for capacitance as well as the programmable resistance of the junction. As suggested by [10] a p-type MOSFET is included to controllably decrease the resistance of the memristive junction while an n-type MOSFET is included to controllably increase the resistance. When both transistors are in the OFF state a small signal current may be applied via diode D. The diode is included in the memory cell to prevent sneak current paths when incorporated into a crossbar architecture.

Fig. 2 illustrates a 2x2 signal processing matrix formed using the memristive memory cells arranged in a crossbar configuration and including operational amplifiers connected to the outputs. Parasitic impedances at the input to the crossbar are denoted by \( Z_{p,in}(1) \) and \( Z_{p,in}(2) \) and parasitic impedances at the output of the crossbar are denoted by \( Z_{p,out}(1) \) and \( Z_{p,out}(2) \). The effects of such parasitics may be more substantial at the nanoscale in which defects and non-negligible contact resistances become significant. Row selection transistors are provided to control the connection of memristive junctions to ground during the programming of the memristive state. The operational amplifiers include feedback impedances indicated by \( Z_{f,out}(1) \) and \( Z_{f,out}(2) \).

3 ELECTRICAL ANALYSIS

Fig. 3 illustrates the electrical diagram of Fig. 2 in which the operational amplifiers are represented in terms of their input impedances \( Z_{op,in} \), output impedances \( Z_{op,out} \) and voltage gains \( A_v \). An approximate linear system analysis may be performed assuming that the DC level of the input voltages \( V_{in} \) are greater than the diode thresholds \( V_{th} \) and that \( V_{in} \) has a sufficiently small magnitude and is applied for a sufficiently short time so as to avoid memristance drift. In this case the superposition theorem may be applied and the total output signal voltages may be calculated as the sum of the partial output voltages produced from the individual input voltage signals with the other input signal grounded. The relationship between column wire voltage \( V_c \) and input voltage \( V_{in} \) may be calculated based on Kirchhoff’s current law applied to the column wire (assuming zero current from the reverse biased diodes \( D_{2x1} \) and \( D_{2x2} \)) producing:

\[
\frac{V_{in1} - V_c}{Z_{p,in1}} = \frac{V_c - V_{th11}}{Z_{11}(w) + Z_{p,out1} + Z_{op,in1}((Z_{F1} + Z_{op,out1})}
\]

\[
+ \frac{V_{in2} - V_{th12}}{Z_{12}(w) + Z_{p,out2} + Z_{op,in2}((Z_{F2} + Z_{op,out2})}
\]

(4)

from which it is straightforward to calculate \( V_c \) in terms of \( V_{in} \).

For the more general case of a crossbar including \( N \) columns and \( M \) rows the relationship between the input voltages and the column wire voltages may be expressed as:

\[
V_{in,i} - V_{c,i} = \sum_{j} \alpha_{ij} (V_{c,i} - V_{th,ij})
\]

(5)

where \( \alpha_{ij} \) is given by:

\[
\alpha_{ij} = \frac{Z_{p,in}}{Z_{ij}(w) + Z_{p,outj} + Z_{op,inj}((Z_{Fj} + Z_{op,outj})}
\]

(6)

and \( i \) and \( j \) are indices ranging from \( 1 \leq i \leq N \) and \( 1 \leq j \leq M \).

Back to the 2x2 case of Fig. 3 an application of Kirchhoff’s voltage law from \( V_{c1} \) on row 1 produces two coupled equations:

\[
V_{c1} - V_{th11} - i_1 (Z_{11}(w) + Z_{p,out1}) - (i_1 - i_2)Z_{op,in1} = 0
\]

(7)

\[
(i_1 - i_2)Z_{op,in1} - i_2 (Z_{F1} + Z_{op,out1}) - A_v(v_p - v_n) = 0
\]

(8)

where \( i_1 \) is the current flowing through the memristive junction, \( i_2 \) is the current flowing through the feedback impedance of the operational amplifier connected to row 1,
and \( v_p - v_n = (i_1 - i_2)Z_{\text{op,in1}} \) \hspace{1cm} (9)

and the output voltage \( \text{Vout1} \) may be calculated based on the amplified differential voltage.

The result of this analysis produces an amplified differential voltage equal to:

\[
\text{Vout} = \frac{Z_{\text{f1}} + Z_{\text{op,1}}}{1 - A_v + \frac{Z_{\text{f1}} + Z_{\text{op,1}}}{A_v Z_{\text{op,in1}}}} \times (V_{\text{c,1}} - V_{\text{th,11}})
\]

\[
Z_{\text{c,1}}(w) + Z_{\text{p,1}} + Z_{\text{op,1}} = \frac{Z_{\text{op,in1}}^2(1 - A_v)}{Z_{\text{op,in1}}(1 - A_v) + Z_{\text{f1}} + Z_{\text{op,1}}}
\]

For an ideal operational amplifier where \( Z_{\text{op,1}} = \infty \), \( A_v = \infty \), and \( Z_{\text{op,1}} = 0 \) this simplifies to:

\[
\text{Vout1} = -\frac{Z_{\text{f1}}}{Z_{\text{c,1}}(w) + Z_{\text{p,1}}}(V_{\text{c,1}} - V_{\text{th,11}}).
\] \hspace{1cm} (11)

Applying the superposition theorem for a MxN crossbar (11) may be generalized to find the total output voltage signals based on all of the input signals applied simultaneously:

\[
\text{Vout,j} = -\sum_i \frac{Z_{\text{fij}}}{Z_{\text{cij}}(w) + Z_{\text{p,ij}}}(V_{\text{c,ij}} - V_{\text{th,ij}}).
\] \hspace{1cm} (12)

where \( \text{Voutj} \) is the operational amplifier output from the \( j \)th row. In cases where the coefficients \( a_{ij} \) from (6) are negligible (which may be designed by increasing the sum of the crossbar output impedances and op-amp feedback impedances relative to the crossbar input impedances) the column voltages reduce to the input voltages and (12) is representative of a signal transfer matrix as in (1) where the memristive resistance states \( Z_{ij}(w) \) effectively determine the magnitude of the elements of the transfer matrix.

4 APPLICATIONS

Several possible applications of memristive transfer matrices were discussed at the 1st Memristor and Memristive Systems Symposium [13]. Depending on the resistive and/or capacitive values of the fixed impedances different functionalities can be achieved as explained below.

4.1 Programmable Analog Filters

In the case where the impedances are chosen such that \( a_{ij} \) are negligibly small (e.g. \( |Z_{\text{p,ij}}| < |Z_{\text{p,ij}} + Z_{ij}| \)), the output impedance of the crossbar are purely resistive \( (Z_{\text{p,ij}} = R_{\text{out}ij}) \), and the feedback impedances \( Z_{ij} \) of the operational amplifiers are implemented by resistors \( R_{\text{f,ij}} \) in parallel with capacitors \( C_{ij} \). Eq.(12) expressed in the Laplace domain reduces to:

\[
\text{V}_{\text{out},j}(s) = -\sum_i \frac{R_{\text{fij}}}{1 + sR_{\text{fij}}C_{ij}}(Z_{ij}(w) + R_{\text{p,ij}}) V_{\text{in},i}(s)
\] \hspace{1cm} (13)

where \( V_{\text{in},i}(s) \) represents the Laplace Transform of the small signal inputs and \( \text{Vout,j}(s) \) represents the Laplace Transform of the small signal outputs. The transfer matrix elements of (13) are representative of a low pass filter having a tunable gain dependent upon the memristive states \( Z_{ij}(w) \).

In a similar case to that above but in which the output impedance of the crossbar are implemented by capacitors \( (Z_{\text{p,1}} = C_{\text{out},1}) \) and the feedback impedances \( Z_{ij} \) of the operational amplifiers are implemented by resistors \( R_{\text{f,ij}} \) Eq.(12) may be expressed in the Laplace domain as:

\[
\text{V}_{\text{out},j}(s) = -\sum_i \frac{sR_{\text{fij}}C_{\text{p,ij}}}{sZ_{ij}(w)C_{\text{p,ij}}} + \frac{1}{s} V_{\text{in},i}(s)
\] \hspace{1cm} (14)

The transfer matrix elements of (14) are representative of a high pass filter having a tunable half-power frequency dependent upon the memristive states \( Z_{ij}(w) \). By cascading multiple memristive transfer matrices which perform the operations of (13) and (14) bandpass filters may be constructed in which both amplitude and frequency tuning can be performed.

4.2 Waveform Generators

If the signal voltage inputs to the columns wires of the memristive transfer matrix include a relative delay period \( T \) between adjacent rows and resistors \( (R_{f,j}, R_{p,ij}) \) are used for the feedback impedance and crossbar output impedance (12) reduces to:

\[
\text{V}_{\text{out},j}(t) = -\sum_i \frac{R_{\text{fij}}}{sZ_{ij}(w) + R_{\text{p,ij}}} V_{\text{in}}(t - iT).
\] \hspace{1cm} (15)
For this implementation the memristive states can be used to determine modified pulse trains based on the basic pulse train in which the amplitude of pulses are modified based on the magnitude of $Z_{ij}(w)$. In a similar case in which the input signals are harmonics of a sine wave having an angular frequency $\omega$ (12) reduces to:

$$v_{out,j}(t) = -\sum \frac{R_{f,j}}{Z_{ij}(w) + R_{p,\text{out}j}} \sin(\omega t). \quad (16)$$

In this implementation tuning of the memristance states may be used in the generation of approximate Fourier series representations of periodic signals.

### 4.3 Analog Arithmetic

For the purposes of analog arithmetic the high resistance state of a memristive junction may represent a logic 0 in which very little current is passed while the low resistance state of the memristance junction may be represent a logic 1. In this case each column of the crossbar may be interpreted as storing a binary string representative of a numerical value and selection of the input voltages to the columns may be used to control a summation operation. In order to separate the crossbar rows from a least significant value to a most significant value precision resistors at the outputs of the crossbar may be set to multiples of 2 times the feedback resistance ($R_{p,\text{out}j} = 2R_{f,j}$). In this case (12) reduces to:

$$v_{out,j}(t) = -\sum \frac{1}{Z_{ij}(w)/R_{f,j} + 2} v_{in,i}(t). \quad (16)$$

This implementation produces analog output signals having a magnitude in proportion to the summation of the memristive states of the crossbar rows. Further discussion of this approach to analog arithmetic is found in [14].

### 4.4 Pattern Comparison

In terms of binary logic the comparison between two individual bits (A,B) is performed using the XNOR function:

$$X = AB + \bar{A}\bar{B} \quad (17)$$

where $X = 1$ when A and B are identical and $X = 0$ when A and B are different. A more generalized comparison function may be defined between M strings of binary data $A_i$ wherein each string has a length N and a string of binary data $B_i$ having a length N where $1 < i < N$ and $1 < j < M$:

$$X_i = \sum (A_iB_j + \bar{A}_i\bar{B}_j). \quad (18)$$

In this case $X_i$ is an integer ranging from 0 to N depending upon the number of bits in $A_i$ and $B_i$ which are identical.

The function of (18) may be implemented using two memristive transfer matrices each performing the function (12) but with complementary resistance states in which bit patterns $A_i$ and its complement (not $A_i$) are implemented by the memristive junctions set to the maximum resistance $R_{\text{HIGH}}$ (logic 0) or minimum resistance $R_{\text{LOW}}$ (logic 1) and $B_i$ are implemented by the binary voltage states of the input signals and the equivalent inverted pattern (not $B_i$). Further discussion of this implementation is found in [15].

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Fig. 1. Memristor memory cell.

Fig. 2. 2x2 Memristor signal transfer matrix.
Fig. 3. Electrical diagram of 2x2 Memristor signal transfer matrix with Vin2=0.