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ABSTRACT

Ferroelectric semiconductor field effect transistors (FeSmFETs), which employ ferroelectric semiconducting thin crystals of $\alpha$-In$_2$Se$_3$ as the channel material as opposed to the gate dielectric in conventional ferroelectric FETs (FeFETs), were prepared and measured from room to liquid-helium temperatures. These FeSmFETs were found to yield evidence for the reorientation of electrical polarization and an electric field-induced metallic state in $\alpha$-In$_2$Se$_3$. Our findings suggest that FeSmFETs can serve as a platform for the fundamental study of ferroelectric metals as well as the exploration of potential applications of semiconducting ferroelectrics.

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Ferroelectricity is defined by the formation of spontaneous electrical polarization in a non-centrosymmetric crystal and the reorientation of the polarization between crystallographically defined directions by the application of an external electric field.1 Ferroelectrics have been used to store data in either a capacitor or a ferroelectric field-effect transistor (FeFET)2 configuration, the latter of which features a ferroelectric gate dielectric and a non-ferroelectric semiconducting channel. FeFETs provide not only fast and non-volatile data storage but also a pathway toward “logic in memory” functions. However, the commercialization of FeFETs has encountered multiple obstacles ranging from the retention time originating from the depolarization interface charge traps.5 A FeFET variation, which replaces the semiconducting channel in the conventional FET with a ferroelectric semiconducting channel but retains the non-ferroelectric gate dielectric, was demonstrated recently. This produces an “on” (or “off”) state without an applied gate voltage, similar to a traditional FeFET. Such a device is referred to as a ferroelectric semiconductor field effect transistor (FeSmFET).

It is interesting to ask whether the “on” state in the FeSmFET can be a metallic state, which will make the transition from the “on” to the “off” state a ferroelectric metal-insulator transition. Anderson and Blount7 examined the structural transition found in metallic V$_3$Si and suggested that the formation of ionic displacements along a polar axis, which led to the loss of inversion symmetry, would be required for the occurrence of the apparent continuous phase transition seen in V$_3$Si. Furthermore, they suggested that such a state should be called a “ferroelectric metal.” Being a metal appears to be inconsistent with the accepted definition of ferroelectricity as mobile charge carriers in a bulk metal will effectively screen any electric field, making the reorientation of the polarization unlikely. Nevertheless, metals showing the presence of electrical dipoles from ionic displacements along with a well-defined polar axis, such as LiOsO$_3$8,9 Ca$_3$Ru$_2$O$_7$,10 and other materials,11 have attracted much attention in recent years even though the issue of whether the dipoles found in these materials are spontaneously ordered and reversible has not been resolved. Interestingly, the difficulty in reversing the polarization in a metal can be circumvented for a ferroelectric 2D crystal. A vertical electrical field, applied to a 2D crystal of 1T$'$/WTe$_2$, by a top and a bottom gate, was shown to lead to sharp jumps in sample conductance, which was attributed to polarization reversal.12 However, direct evidence for ferroelectricity in 2D 1T$'$/WTe$_2$ is still lacking.

In$_2$Se$_3$, a layered transition metal chalcogenide (TMC) featuring a van der Waals interlayer coupling and an energy gap of 1.4 eV, was
predicted\textsuperscript{11} to be ferroelectric down to a 1-unit-cell thickness in both $\alpha$- and $\beta$-phases. Supporting evidence for ferroelectricity in $\alpha$-$\text{In}_2\text{Se}_3$ was found via piezoelectric force microscopy (PFM)\textsuperscript{14-18} and second harmonic generation (SHG)\textsuperscript{18,20} with a transition temperature up to 700 K.\textsuperscript{11} Extensive device work carried out in the last few years also supports ferroelectricity in this layered TMC. An on/off state was found in rectifying devices by sweeping the source-drain voltage,\textsuperscript{14,17,21} revealing distinct hysteresis loops suggesting complex orientations of the polarization.\textsuperscript{14,16,19} In the pioneering work of the FeSmFET featuring thin crystals of $\alpha$-$\text{In}_2\text{Se}_3$ and a gate dielectric of 90-nm-thick SiO$_2$ or 15-nm-thick HfO$_2$, respectively, large clockwise and counterclockwise hysteresis loops were found in gate voltage sweeps.\textsuperscript{22} The hysteresis was shown to persist down to 80 mK, making it unlikely that the observed hysteresis at such a low temperature is due to charge traps. These observations strongly support the existence of ferroelectricity in $\alpha$-$\text{In}_2\text{Se}_3$. However, the most explicit demonstration of ferroelectricity in $\alpha$-$\text{In}_2\text{Se}_3$ was obtained in a stacked capacitor/FET device.\textsuperscript{22} This device consists of monolayer graphene on a SiO$_2$/Si substrate that functions as a bottom gate. Graphene is also the bottom electrode for a capacitor featuring a two-layer dielectric combining an insulating monolayer or bilayer of hexagonal boron nitride (hBN) and an atomically thin, semiconducting crystal of $\alpha$-$\text{In}_2\text{Se}_3$, which was covered by a top metal electrode/gate. The electric field applied between graphene and the top electrode was used to reorient the polarization in $\alpha$-$\text{In}_2\text{Se}_3$. Graphene sandwiched between SiO$_2$ and hBN functioned as a charge detector through the position of the charge neutral point (CNP) in sample resistance vs the gate voltage curves. From the clear and systematic shift in the CNP as the polarization was flipped, a polarization value of 0.92 $\mu$C/cm$^2$ was estimated under an external field of $5 \times 10^5$ V/cm, which is reasonably close to the theoretically predicted\textsuperscript{12} value of 0.6 $\mu$C/cm$^2$.

The in- and out-of-plane resistivities of $\alpha$-$\text{In}_2\text{Se}_3$ crystals grown by a modified Bridgman method used in this work, obtained from a four-point probe on bulk crystals using electrical contacts made by Ag paint, showed a variable-range hopping (VRH) conduction at low temperatures [below $\sim$40 K, see Fig. 1(a)] after the unintentionally doped charge carriers are frozen out. Thin crystals of $\alpha$-$\text{In}_2\text{Se}_3$ were obtained by mechanical exfoliation from a bulk crystal and deposited onto a heavily doped silicon chip with a 300-nm thick thermally grown surface of SiO$_2$. The thickness of a thin crystal of $\alpha$-$\text{In}_2\text{Se}_3$ was determined by atomic force microscopy (AFM) after the transport measurements were carried out. Two types of FeSmFETs featuring a Hall bar [Fig. 1(e)] and traditional FET [Fig. S1(a) in the supplementary material] pattern, respectively, were prepared by photolithography with electrodes of 5 nm of Ti and 45 nm of Au. The parameters for the four devices used in the present study are shown in Table S1 in the supplementary material. DC electrical transport measurements were carried out using a Quantum Design Physical Property Measurement System (PPMS) equipped with a 9 T superconducting magnet that features a base temperature of 1.8 K. For temperature varying measurements, the device was cooled/warmed at zero gate voltage unless otherwise specified.

To characterize the thin crystals of $\alpha$-$\text{In}_2\text{Se}_3$, Raman spectroscopy, photoluminescence (PL) and second harmonic generation (SHG) measurements were used. The Raman spectra [Fig. 1(b)] confirmed that the crystals used were $\alpha$-$\text{In}_2\text{Se}_3$.\textsuperscript{19} An energy gap value of 1.4 eV was revealed in the PL measurements [Fig. 1(c)], consistent with that found in the literature.\textsuperscript{23} Strong SHG signals with the expected sixfold symmetry were also found [Fig. 1(d)], demonstrating that our $\alpha$-$\text{In}_2\text{Se}_3$ crystal indeed belongs to the $R3\bar{m}$ space group.\textsuperscript{17-19}

Source-drain current vs voltage ($I_D$ vs $V_{DS}$) characteristics were measured on the FeSmFETs at fixed gate voltages ($V_G$). The results for sample A [Fig. 1(e)] with a channel length of 12 $\mu$m and a thickness of 110 nm are shown in Fig. 2 for $V_G$ increasing from $\sim$75 to 75 V and back to $\sim$75 V. No saturation in $I_D$ was observed in this range of gate voltages up to 10 V for all $V_G$ values. Similarly, a marked change in the slope was found in most $I_D$ vs $V_{DS}$ curves, showing that $I_D$ increases much faster at low $V_{DS}$ than at high $V_{DS}$ values. The sharp rise in $I_D$ at low $V_{DS}$ values (below a few tenths of volts) may be related to the presence of two back-to-back Schottky diodes studied previously in other materials.\textsuperscript{24-26} Behavior seen at high $V_{DS}$ values, in particular, in the linear plots (Figs. S2 and S3), is similar to that reported previously.\textsuperscript{6}

Clockwise transfer curves of $I_D$ vs $V_G$, starting at $V_G = \sim$75 V, were measured on our FeSmFET devices at fixed temperatures, $T$, from 300 to 2 K (Figs. 3 and S5). These results are consistent with

FIG. 1. (a) In- and out-of-plane resistivities of bulk single-crystals $\alpha$-$\text{In}_2\text{Se}_3$ showing Mott variable-range hopping conduction behavior, $\rho_{in-plane out-of-plane}(T) \sim \exp[T/T_0^{1/4}]$, where $T_0$ is a constant, below around $T = 160$ K. Also shown are results of Raman spectroscopy (b), photoluminescence (c), and second harmonic generation (d) measurements. A schematic of an FeSmFET in the Hall bar pattern is shown in (e). Inset: optical image of a FeSmFET device following this design with the 10-$\mu$m scale bar also shown.
those seen in the previous work. The clockwise hysteresis loop points to the presence of a polarization in the n-type \( \text{a-In}_2\text{Se}_3 \) semiconductor. Basically, at a sufficiently large negative \( V_G \) say, \(-75 \, \text{V}\), the downward pointing electric field will force the polarization inside the \( \text{a-In}_2\text{Se}_3 \) crystal downward (Fig. S1), resulting in positive bound surface charge on the bottom surface of the crystal due to the presence of the polarization. Consequently, the energy bands will band upward (Fig. S1). The gate voltage-induced positive charge carriers will deplete the conduction band (the existing negative charge carriers will be “drained” from the channel), which will shut down conduction channels between the source and the drain. On the top of the \( \text{a-In}_2\text{Se}_3 \) crystal, however, the negative bound charge from the downward pointing polarization will push down the conduction band, placing the Fermi energy within the conduction band (Fig. S1). However, even though the low density of the gate voltage-induced positive charge carriers cannot deplete the conduction band fully because the gate electric field is weak on the top surface of the crystal, no conduction channel between the source and the drain is expected there either because of the low carrier density. An “off” state of the FeSmFET is, thus, expected, which was indeed observed.

As \( V_G \) increased from \(-75 \, \text{V}\) to 0 and then 75 \, \text{V}, the polarization will start to reverse locally. The depletion layer on the bottom surface of the \( \text{a-In}_2\text{Se}_3 \) crystal will be reduced, helping push down the conduction band. A conduction channel between the source and the drain will eventually be established, leading to the “on” state of the FeSmFET. The device will continue to be in the “on” state as \( V_G \) is increased further to 75 \, \text{V}. Now, the polarization will switch to point upward so that the bound charge from the polarization will be negative on the bottom surface of the crystal, featuring negative mobile charge carriers induced by the positive gate voltage. Ramping \( V_G \) from 75 \, \text{V} to 0, the polarization will turn downward locally, leading to positive bound charge from the polarization on the bottom surface of the crystal. The existing and gate induced negative charge carriers could be bound to the positive surface charge from the polarization, creating local areas that are non-conducting. As the gate voltage decreases further, the polarization will continue to flip, leading to continuous growth of non-conducting areas and a decreasing \( I_D \). Eventually, all conduction channels disappear, leading to vanishingly small \( I_D \). A clockwise hysteresis loop as shown in Fig. 3 will be obtained. Our observation is, therefore, fully consistent with the existence of polarization in \( \text{a-In}_2\text{Se}_3 \), as argued previously.

The overall hysteresis decreased as the temperature \( T \) was lowered (Fig. 3). Thus, it is natural to ask whether the reduction in hysteresis was a result of a change in the coercive field as the temperature was lowered. This seems to be unlikely given that the ferroelectric transition temperature, \( T_c \), of \( \text{a-In}_2\text{Se}_3 \) was reported to be 700 \, \text{K} as the coercive field of a ferroelectric material would increase as \( T \) is lowered below \( T_c \) or remain constant far below it. The more likely scenario is the decrease in hysteresis as \( T \) was lowered was due to the presence of charge traps in our sample. Charge traps in FETs are known to lead to a hysteresis loop. At higher temperatures, the hysteresis originating from charge traps and that from polarization appear to coexist in our samples. However, at a liquid-helium temperature, at which the binding and unbinding of mobile charge carriers from their traps are expected to be suppressed, the observed hysteresis should be only due to the reversal of the polarization, as argued previously.

Values of two-point resistance \( R_{DS} (= I_D/V_{DS}) \) taken from the top of the hysteresis loop are plotted against \( T \) in Fig. 4(a), showing decreasing \( R_{DS} \) with the lowering \( T \) and the emergence of a metallic
state. The four-point sample resistance, $R(T)$, of the same crystal was also measured as a function of $T$ [inset of Fig. 4(a)], showing that $R_{00}(T)$ and $R(T)$ have similar behavior. This suggests that the contact resistance between Ti/Au and $\chi$-In$_2$Se$_3$, which was measured at room temperature (Fig. S7), did not make a big difference in the behavior of $I_D$. Data obtained for $V_G = 75$ V in samples B and C showed a positive $dR/dT$ at higher temperatures and a complete flattening-off in $R_{00}(T)$ down to 4 K [Figs. 4(b) and S6]. A small negative $dR/dT$ was seen at the lowest temperatures in sample A; even at $V_G = 75$ V, the density of gate voltage-induced mobile charge carriers is the largest, which appears to be due to sample specific disorder. Weak localization in a weakly disordered metallic sample can lead to a negative $dR/dT$ when $T$ is sufficiently low. The maximum 2D electric conductivity obtained from the four-point measurements was found to be around 80 $\sigma_0$, where $\sigma_0 = e^2/h = (4.08 \times 10^{-5}$ $\Omega^{-1}$) is the quantum conductance, $e$ is the electron charge, and $h$ is Planck’s constant. Above $\sigma_0$, a negative $dR/dT$ is expected due to weak localization, along with possible negative magnetoconductance (MC) depending on the strength of the spin–orbital coupling. Our measurements showed positive MC at 1.8 K [Fig. 4(c)], as well as 10 K and 50 K (data not shown), consistent with the weak spin–orbital coupling expected for $\chi$-In$_2$Se$_3$. The MC data are shown in Fig. 4(c) to fit Maekawa–Fukuyama theory of 2D weak localization quantitatively.

In the metallic state, the negative mobile charge carriers should be accumulated near the bottom of the $\chi$-In$_2$Se$_3$ crystal, while the rest of the crystal remains semiconducting. This layer of mobile charge will tend to screen the gate electric field, making the polarization in the semiconducting region of the crystal less affected by the gate electric field. However, as shown in the data, some polarization can still be reoriented by the field even in the metallic state. As a result, the 2D metallic sheet of electrons and the polarization must coexist in $\chi$-In$_2$Se$_3$.

The interesting question is how the bound charge of polarization on the crystal bottom will affect the accumulation of the mobile electrons. At $V_G = 75$ V, the electric field is expected to induce an electron density of $5 \times 10^{12}$/cm$^2$. Hall measurements showed that the Hall voltage is a linear function of the magnetic field, suggesting that only electrons are present in the sample. The density of electrons at 4 K is roughly what would be expected solely from that induced by the gate electric field, unaffected by the polarization [Fig. 4(d)]. At higher temperatures, however, the electron density obtained by the Hall measurements is larger than that induced by the gate voltage. This is reasonable, as the existing unintentionally doped electrons that are bound to the positive charge traps at low temperatures would start to be released as the temperature was raised, consistent with the observation of the broadening hysteresis noted above.

The observations presented above demonstrate a well-functioning FET with a large $I_D$ even when gate voltage is at zero. Such a FeFET can be used for logic operations as well as a memory device in the microelectronic circuitry with the “logic in memory” functionalities. In addition, ultrathin $\chi$-In$_2$Se$_3$ was shown to provide a test bed for fundamental research on ferroelectric metals as well as ferroelectric metal-insulator transitions tuned by a gate voltage.

See the supplementary material for additional device schematics, band diagram representation, additional sample data, and device parameters.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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