ABSTRACT
As energy efficiency became a critical factor in the embedded systems domain, dynamic voltage and frequency scaling (DVFS) techniques have emerged as means to control the system’s power and energy efficiency. Additionally, due to the compact design, thermal issues become prominent. State of the art work promotes software decoupled access-execute (DAE) that statically generates code amenable to DVFS techniques. The compiler builds memory-bound access phases, designed to prefetch data in the cache at low frequency, and compute-bound phases, that consume the data and perform computations at high frequency.

This work investigates techniques to find the optimal balance between lightweight and efficient access phases. A profiling step guides the selection of loads to be prefetched in the access phase. For applications whose behavior vary significantly with respect to the input data, the profiling can be performed online, accompanied by just-in-time compilation. We evaluated the benefits in energy efficiency and performance for both static and dynamic code generation and showed that precise prefetching of critical loads can result in 20% energy improvements, on average. DAE is particularly beneficial for embedded systems as by alternating access phases (executed at low frequency) and execute phases (at high frequency) DAE proactively reduces the temperature and therefore prevents thermal emergencies.

Keywords
Decouple access-execute, compiler techniques, energy efficiency, high performance, profiling, just-in-time compilation

1. INTRODUCTION
Embedded systems evolved dramatically since the early designs, with a significant rise in processing power and functionality, providing nowadays a wide range of functional-
in targeting the critical loads and rips the benefits of timely software prefetching. Using the program slicing approach to generate access phases (as opposed to static heuristics to simplify the control-flow and target indirect memory accesses employed in DAE [14]), PDAE contains the required control instructions to reach all critical loads. We have evaluated the performance of statically generated access phases and just-in-time compiled phases, underlining the overhead of JIT-ing. We recommend using JIT only for applications whose critical loads are input dependent and for cross-compiled applications (in which case the critical loads may vary with respect to the underlying architecture). Otherwise, an offline profiling step is sufficient to identify long latency loads and generate efficient access phases with no additional cost.

PDAE brings (1) energy efficiency, by scaling down frequency during memory bound phases; (2) with a minimal impact on performance (5% slowdown on average, and up to 20% speed-up on memory bound codes); and (3) improvements in the system’s thermal profile, by alternating high- and low-frequency execution phases, which naturally regulates the chip’s temperature. Overall, this yields higher energy efficiency and performance and leads to increased reliability and diminished cooling costs.

2. METHODOLOGY

PDAE targets loops, which are executed in slices. The decoupled access-execute scheme is applied to each loop-slice to ensure that the data prefetched during the access phase is consumed by the execute phase before being evicted from the cache. The access phase prefetches a selection of loads, while the execute version represents the original loop code, which now became compute-bound since the required data is available in the cache. The compiler passes are implemented in the LLVM compilation framework [19].

2.1 Statically generated Access versions

First, an offline profiling step is performed to identify long latency loads. The compiler then proceeds as follows: (1) slices the loops and (2) generates Access - Execute versions for each loop-slice. Access phases contain the control-flow instructions and the computation of addresses in order to prefetch the target addresses of the critical loads. The instructions of the access phase are identified following the use-def chain. Hence, the access version is derived from the original code, but includes only a subset of its instructions. The process is detailed in Figure 1.

2.2 Dynamically generated Access versions

Similarly, (1) the loop is first sliced, (2) then the compiler generates Access-Execute versions per loop slice, however, since no profiling information is yet available, all loads are prefetched in the base-Access phase. Next, (3) the access version is extracted in a new function and support for just-in-time (JIT) compilation is added. Only access phases are JIT-ed, while (4) the rest of the code is statically compiled, to reduce the overhead.

At runtime, (1) a profiling step is used to identify critical loads and to map them to the corresponding prefetch instructions in the access version. The first invocation of the access phase will trigger (2) a JIT compilation, which will filter out prefetch instructions which do not map a critical load and will clean dead code, yielding a lean and efficient access phase. Future invocations of the access version will directly call the already generated access code. The static and dynamic compilation steps are shown in Figure 2.

The execution model is shown in Figure 3. To complete the first loop-slice, the original (execute) version of the loop is invoked and the long latency loads identified by profiling are mapped to the corresponding prefetch instructions in the access version. The second slice of the loop invokes the access version for the first time, triggering a JIT compilation, while the remaining slices will complete loop execution without further compilation overhead.

2.2.1 Profiling

The profiling can be performed statically or dynamically on one loop-slice or based on sampling to reduce the overhead. As low-overhead profiling was discussed in numerous previous work [21, 26, 12], this proposal does not attempt to design new profiling methods. For this work, the experiments were conducted using an offline profiling step to annotate critical loads (even for the JIT-ed version) and we leave for future work integration with state-of-the-art low-overhead profiling techniques [12], tailored to identify long latency loads.

2.2.2 Generating decoupled access-execute code

The compiler proceeds by generating a base-Access version which includes software prefetch instructions for all loads in the original code, their requirements, and instructions that maintain the control flow (branches and computa-
2.2.3 JIT optimizations

To enable dynamic optimizations of the base-Access version, we rely on the LLVM MCJIT engine [1]. The program is compiled into a dynamic library loaded by the JIT engine and the calls to the access version are replaced with JIT callbacks, which enable optimizing and generating the access version on demand. JIT callbacks return a function pointer to the access version.

At execution time, the JIT engine loads the code of the access version (in the LLVM intermediate representation) on start-up, together with the dynamic library which contains the program and continues by calling the “main” function to start the execution of the program. Upon a callback, the JIT first checks whether the callback for this access version has been resolved previously. On the first invocation, the JIT finds the code in LLVM IR corresponding to the access version and runs a pass to remove extraneous prefetches, namely prefetch instructions that do not carry metadata information which indicates that they map critical loads. A dead code elimination pass follows to remove extraneous prefetches, corresponding to the eliminated prefetch instructions. This leads a lightweight but efficient access version, which is then JIT compiled to an in-memory executable binary. The corresponding function pointer is stored within the JIT so that future calls of the access version do not trigger a new dynamic compilation. Finally the JIT returns the function pointer to the generated access phase, and the program continues execution by calling that function, followed by the execute phase.

2.3 The Power Model

We used the same power model [27] as the one employed to measure the energy expenditure in previous DAE proposals [14, 16]. The model approximates power usage based on the metric Instructions per Cycle (IPC) which is collected using the PAPI library [22].

3. EVALUATION

We perform our measurements on an Intel Sandybridge i7-2600K processor with 16GBytes of DDR3 1333MHz memory. PDAE was evaluated on a subset of benchmarks from the SPEC CPU-2006 benchmark suite ranging from compute...
Figure 4: Distribution of execution time and energy for a selection of SPEC 2006 benchmarks, on an Intel i7-2600K.

4. RELATED WORK

Dynamic voltage and frequency scaling techniques have been widely used for optimizing embedded systems for power and energy efficiency [2, 13, 17, 20, 15, 1, 11, 6]. As thermal issues became a concern, some of these proposals focused on controlling the peak temperature. Liu et al. [18] propose design-time DVFS planning and provide solutions to ensure optimal peak temperature, which may not correspond to the optimal energy solutions. Hence, the outcome is a thermal-constrained energy optimization. Bhatti et al. [7] study the interplay between state of the art Dynamic Power Management (DPM) and Dynamic Voltage & Frequency scaling (DVFS) policies, and propose a scheme that selects at runtime the best-performing policy for any given workload. Genser et al. [11] acknowledged the importance of DVFS techniques for embedded systems and developed a power emulator to enable designers determine the most suitable voltage regulator and meet performance, power and energy demands. While these approaches enhance the design of the embedded system, our focus is on adapting the applications to better suit the already available hardware.

5. CONCLUSIONS

As DVFS techniques became popular for managing power...
and energy efficiency, we demonstrate a compiler method to transform applications to better suit the hardware DVFS capabilities. In particular, we target applications which contain irregular memory accesses and dynamic control flow and generate decoupled access-execute code versions. Accesses phases, dedicated to prefetch data to the cache, are generated automatically by the compiler, guided by profiling to ensure their efficiency. Being memory bound, access phases are run at low frequency, thus saving energy. Execute phases represent the original code, but become compute bound as they consume the data brought by the corresponding access phase to the cache. Execute phases are run at high frequency to maintain high-performance. Alternating access (low frequency) and execute (high frequency) phases naturally regulates the chip’s temperature, with a positive side-effect on thermal related aspects (cooling costs, reliability, peak temperature, etc). We have evaluated both a static and a dynamic compilation approach, assisted by offline and online profiling respectively. PDAE assumes perfect profiling for identifying critical loads whose prefetch during the access phase provides energy benefits. The static scheme provides 25% energy savings and 7% performance improvement, compared to the original code run at maximum frequency. The dynamically compiled scheme adds the JIT-overhead and yields energy savings of 18% on average (20-35% for memory bound applications) with only 5% performance degradation on average (up to 20% speed-up for memory bound applications).

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