Learning to Schedule Halide Pipelines for the GPU

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\textbf{Abstract}

We present a new algorithm to automatically generate high-performance GPU implementations of complex imaging and machine learning pipelines, directly from high-level Halide algorithm code. It is fully automatic, requiring no schedule templates or hand-optimized kernels, and it targets a diverse range of computations which is significantly broader than existing autoschedulers.

We address the scalability challenge of extending previous approaches to schedule large real world programs, while enabling a broad set of program rewrites that take into account the nested parallelism and memory hierarchy introduced by GPU architectures.

We achieve this using a hierarchical sampling strategy that groups programs into buckets based on their structural similarity, then samples representatives to be evaluated, allowing us to explore a large space by only considering a subset of the space, and a pre-pass that ‘freezes’ decisions for the lowest cost sections of a program, allowing more time to be spent on the important stages. We then apply an efficient cost model combining machine learning, program analysis, and GPU architecture knowledge. Our method scales combinatorially better with respect to the deeper nested parallelism required by GPUs compared to previous work. We evaluate its performance on a diverse suite of real-world imaging and machine learning pipelines. We demonstrate results that are on average 1.66× faster than existing automatic solutions (up to 5×), and competitive with what the best human experts were able to achieve in an active effort to beat our automatic results.

\textbf{1. Introduction}

There is an increasing demand for high-performance array programs for imaging and machine learning code. These programs manipulate arrays with many stages of deeply nested loops. Writing high-performance array programs on GPUs typically involves non-trivial trade-offs between parallelism, memory locality, and recomputation. Some optimization choices include splitting and reordering loops in various configurations and assigning them to GPU blocks and threads, fusing different stages into a single GPU kernel, and caching intermediate results in shared memory for better locality. Manually implementing these options is highly time-consuming, as they often involve making global changes to the program structure, and it is difficult to predict ahead of time whether a change will be beneficial to performance.

Our goal is to automatically optimize programs that extend into the tens or hundreds of stages of computation. We build on Halide, a domain-specific compiler that decouples the algorithm – what we compute – from the the schedule – how we compute it. This separation makes it easier to explore different schedules for a given algorithm but finding high-performance schedules remains a challenge. The space of possible schedules for these programs is extremely large so we cannot feasibly compile and benchmark all of them. We need a solution that can explore a large search space efficiently and evaluate the performance of potential options without needing to compile and benchmark programs excessively.

Previous approaches to automatically optimizing array programs have achieved impressive results for programs in their scope, but face a scalability problem when applied directly to programs with a larger scheduling space. Adams et al.’s Halide autoscheduler \cite{halide} focuses on CPU schedules and its algorithm does not scale to evaluate all the nested parallel tiling options for GPUs. Sioutas et al.’s Halide GPU scheduler \cite{sioutas} only uses block level tiling and does not consider optimizations such as register blocking. Polyhedral compilers also focus on a limited set of scheduling options. Other tensor optimization work (e.g., AutoTVM \cite{autotvm}, Tensor Comprehension \cite{tenscom}, FlexTensor \cite{flextensor}, and TASO \cite{taso}) focuses on neural networks with high arithmetic intensity and dense connections, where computation can be easily broken up into individual components (such as a convolution layer). This allows them to explore a large scheduling space on a single operator.

We aim to efficiently explore a rich space of schedules and achieve high performance on a broad range of applications. To solve the scalability problem, we apply two strategies. First, we use a pre-pass where the program is autoscheduled with a restricted set of search options and the cheapest stages of computation are identified by a learned cost model. These stages have their schedule options ‘frozen’: they will retain the same schedule and not be considered as part of the regular autoscheduling process. Second, we introduce a hierarchical sampling strategy that allows us to explore a large space of possible schedules by only considering a subset of options substantially smaller than the entire space. We use a structural hash to group schedules that share a similar structural organization and evaluate only representatives of each group. As a result, we are able to enumerate a rich space schedules of while making it possible to search the larger space efficiently.

Even with our hierarchical sampling, there are still too many schedules for us to compile and benchmark. We employ

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implementing. We explore the trade-off between compile time and performance. Our scheduler operates in three modes. In One Shot mode, we generate a batch of \( N \) samples and take the best according to the cost model. This requires no compiling or benchmarking. In Top 5 mode we generate a batch of \( N \) samples and of the fastest \( k \) according to the cost model, return the actual best after compiling and benchmarking. In autotuning mode batches of samples are generated, compiled, benchmarked and used to retrain a cost model for as long as desired.

Our paper contributes:

- A new automatic scheduling algorithm that scales asymptotically better than prior work by using hierarchical sampling, making it possible to efficiently explore a large, rich space of GPU schedules.
- A set of schedule features that capture the architectural intricacies required to predict performance of GPU programs.
- A GPU cost model that combines the schedule features from program analysis with machine learning. We train the model on a large set of random pipelines and a hold-one-out set of real world application programs.
- State of the art results on a suite of real world imaging and machine learning pipelines. We outperform the state of the art GPU autoscheduler [20] with a geomean speedup of 1.21\( \times \) in One Shot mode, 1.31\( \times \) in Top 5 mode, and 1.66\( \times \) with autotuning. Autotuning, we obtain results (0.98\( \times \)) competitive with what the best human experts were able to achieve in an active effort to beat our automatic results.

2. Why is There a Scalability Problem?

Consider a program consisting of a chain of stencils, where each point to be computed depends on a stencil of points from a previous stage of the program (Figure 1). This computation pattern is common in deep learning architectures (e.g., a sequence of depthwise separable convolution layers), image processing algorithms, and physics simulation. How would you implement this program for high performance on the GPU? Any implementation will need to balance the tradeoff between memory locality, redundant recomputation, and parallelism.

**Separate Kernels** The simplest approach is to schedule each stage of the chain in a separate kernel. In this case, both \texttt{intermed} and \texttt{output} will be computed in separate kernels:

```python
allocate intermed
for col_o, row_o in ?, ? @blocks
    compute intermed
allocate output
for col, row in output.W, output.H @blocks
    compute output
```

Every point of \texttt{intermed} will be computed first, and stored in global memory, then every point of \texttt{output} will be computed, loading them. As written, this implementation is inefficient. It uses parallelism at the block level but makes no use of thread parallelism.

**Tiling the Blocks** A more efficient implementation would *tile* the blocks by splitting the outer loops into outer block loops and inner thread loops:

```python
allocate intermed
for col_o, row_o in ?, ? @blocks
    for col_i, row_i in ?, ? @blocks
        compute intermed
allocate output
for col_o, row_o in ?, ? @blocks
    for col_i, row_i in ?, ? @threads
        compute output
```

But we now have *choices* for how big the tiles of each stage should be. As we consider more complex schedules, these choices will affect things like locality and redundant computation, but for now they mostly impact parallelism: Small tiles produce many blocks, but few threads per block—plenty of parallelism across streaming multiprocessors (SMs), but potentially too little thread parallelism within each to keep it busy. Large tiles make the opposite tradeoff: less (block) parallelism across SMs, and more (threads) within each one. 16, 32, and 64 are typical choices for the innermost thread dimension, while powers of 2 are common choices for the remaining dimensions.

Importantly, by introducing block tiling, we have created
$O(T^d)$ possible options to consider (where $T$ is the number of tile sizes and $d$ is the number of dimensions to tile, in this case 2). If the size of the iteration domain is small, the number of options is smaller. Larger arrays, especially if they have multiple dimensions, will have many more options. Large three- and four-dimensional tensor operations are common in image processing and machine learning. Even for this seemingly straightforward implementation, there are still many possibilities to consider.

**Tiling the Threads** A further optimization we can consider is tiling the thread level, as well:

```python
allocate intermed
for col_o, row_o in ?, ? @blocks
    for col_i, row_i in ?, ? @threads
        for col_ii, row_ii in ?, ? @serial, unrolled
            compute intermed
allocate output
for col_o, row_o in ?, ? @blocks
    for col_i, row_i in ?, ? @threads
        for col_ii, row_ii in ?, ? @serial, unrolled
            compute output
```

Each thread is then responsible for computing a sub-tile’s worth of points, instead of just one. This gives coarser-grained parallelism, and provides opportunities to exploit input reuse (fetching shared values once and reusing them in registers) and instruction-level parallelism, especially if the serial subtiles are unrolled. But it also comes with tradeoffs: it reduces parallelism at the block and thread levels, and may increase the stride of memory accesses across threads, reducing bandwidth efficiency.

Typical choices for thread tiling options are small constants, and the loops are often unrolled. This introduces a further $O(T^d)$ possible tiling options to consider. Critically, this compounds with the choices at the thread level, and introduces the major challenge of enumerating schedule options for GPUs: scalability. By attempting to exploit nested parallelism, the total number of options across both levels – and including fusion decisions – introduces a quadratic factor, becoming $O((T^d)^2) = O(T^{2d})$.

Even for a modest number of tiling options and a small number of dimensions, this total quickly grows into the hundreds or thousands – and these are only options for a single stage of the program. Real applications can have 100s of stages, many with 4 or more dimensions. For example, a 3 dimension stencil chain with input size 1536x2560x8 can generate almost 3 million possible options, even for a chain of length 14. And computing each stage in its own kernel is hardly the only option we need to consider to achieve high performance.

**Fusion Options** The options we considered so far all exhibit poor memory locality: all intermediate values produced by `intermed` are computed and stored to slow global memory before any are used to compute `output`, at which point they have likely fallen out of cache. An alternative is to move (or fuse) the computation of `intermed` inside the loop nest of `output`:

```python
allocate output
for col_o, row_o in ?, ? @blocks
allocate intermed @shared_mem
    for col_i, row_i in ?, ? @threads
        for col_ii, row_ii in ?, ? @serial, unrolled
            compute intermed
    for col_i, row_i in ?, ? @threads
        for col_ii, row_ii in ?, ? @serial, unrolled
            compute output
```

In doing so we improve memory locality, and the smaller intermediate working set can be stored in faster local memories – shared memory if fused at the block level like here, or registers if fused one step further, all the way inside the thread level:

```python
allocate output
for col_o, row_o in ?, ? @blocks
    for col_i, row_i in ?, ? @threads
        allocate intermed @shared_mem
        for col_ii, row_ii in ?, ? @serial, unrolled
            compute intermed
        for col_ii, row_ii in ?, ? @serial, unrolled
            compute output
```

However, these fusion choices come at the cost of redundant recomputation of all the points in `intermed` where the the stencil needed by `output` overlaps from one tile to the next (the orange region in Figure 1). Fusion introduces additional choices for the level in the loop nest at which to fuse each stage, and additional tiling options within those fused blocks, further exacerbating the scalability problem.

**The Cost of Evaluating an Option**

The space of choices we have to consider to optimize a program like this for the GPU is large, rapidly reaching into the millions for real programs. Fully compiling and benchmarking each choice is prohibitive, as it can take tens of seconds to minutes per choice. We therefore rely on a cheaper, but still rich cost model (Sec. 7.2) to more quickly evaluate choices. But even this is far from free: to accurately predict the performance of complex programs on complex hardware, it applies both a wide array of static analyses to extract performance-relevant features of a given choice, and a small deep neural network to compute the nonlinear mapping from these features to ultimate performance. Our cost model is highly optimized, but it still often takes tens of microseconds to evaluate – orders of magnitude more than simply enumerating a choice. And the cost function introduces an additional quadratic scalability challenge: the number of choices to evaluate grows with the number of stages in the program $n$, but the cost of evaluating the cost model also grows with $n$, producing a total cost model evaluation time that scales with $n^2 \times T^2d$. In all, this makes it infeasible to directly optimize GPU schedules using the tree search techniques introduced by prior work [2], since autoschedule times increase substantially as programs grow.
3. Hierarchically Sampling the Search Space

The space of options we want to consider is too large to feasibly explore and evaluate in its entirety. How can we efficiently explore the space without fearing to evaluate the cost model for all the possible states? Our key idea is that the search space can be partitioned into buckets based on structural similarity, and it is sufficient to randomly select candidates from within each group as representatives to be featurized and evaluated by the cost model (Figure 2). Intuitively, the representatives chosen from each group should give some sense of the expected performance of the group as a whole i.e. the expected performance of a schedule with that same structural layout. This approach stratifies the search space based on fundamental structural changes to the program’s schedule.

We compute the hash of each option up to a given depth (Figure 3), where the depth considered increases as the search process continues [2] (Section 6.5). For example, all options that have the same functions computed in their own kernels will have the same hash at depth 0, regardless of which other computations are fused into their kernels. But those same schedules may have different hash values at depth 1 if they have different computations at their block levels. At greater depth values, the hash function will take into account more levels of fusion: it becomes more fine grained and more buckets result. Intuitively, this allows us to control the amount of variation amongst the options in each bucket: low depth values mean few buckets where the options may only share coarse structural similarity and greater depth values mean many buckets where the options share more fine grained structural similarity.

When selecting representatives, we randomly choose only $\log_2(B)$ options from each bucket (where $B$ is the number of schedules within the bucket) to be featurized and evaluated by the cost model. This reduces the number of options we evaluate for each stage from $O(T^2d)$ down to $O(\log_2(T^2d)) = O(2d \log_2(T))$, which makes it feasible to evaluate all the chosen representatives.

4. Freezing Low Cost Stages

Inspired by how human experts approach scheduling by focusing their attention on the parts of the program they think will be the most costly, the second thing we do to improve scalability is to ‘freeze’ the lowest cost stages of the program and focus our attention on the higher cost stages. During a pre-pass that only considers options that compute stages in their own kernels or inline, we enumerate options as normal, using the hierarchical sampling strategy. For the resulting schedule produced, we examine the lowest cost stages according to the cost model and ‘freeze’ the options that were chosen for them. We then schedule the unfrozen stages without restriction. We ‘freeze’ all but $\log_2(N)$ stages, improving the scalability for programs with many stages.

5. Overview of the Autoscheduler

Similar to Adams et al. [2] and many other autoschedulers, our algorithm consists of 3 major components. First, we enumerate a large space of plausible GPU schedules for a given Halide program. Second, we featurize the schedules and provide them to a learned cost model that predicts program run time. And third, we use a variant of beam search to explore the space of possible schedules. The beam search uses our hierarchical sampling strategy to make the search space exploration scalable and is guided by the cost model to search for the best performing programs. Our algorithm supports different modes of operation. It can be used to schedule a program quickly in a one-shot fashion, without any compiling or benchmarking. It can also be used for autotuning: we can generate many possible schedules, compile and benchmark them on the target GPU and use these programs to retrain the cost model, improving its ability to accurately predict program run times. This process can be repeated as desired.

6. Our Search Algorithm

We use a variant of beam search to guide the process of enumerating options, selecting them using hierarchical sampling for evaluation by the cost model. It can be run for multiple passes, during which it uses information from previous passes to prioritize states to explore during the current pass. It maintains a priority queue of $k$ candidate states, each representing a partially scheduled loop nest. The beam search operates in 2 phases for each Func.

To help illustrate this process, we introduce a Halide pipeline based on our previous stencil chain example (simplified to use a 1D stencil across columns):

```
@Func intermed, output;
intermed(x, y) = input(x-1, y) + input(x, y) + input(x+1, y);
output(x, y) = intermed(x-1, y) + intermed(x, y) + intermed(x+1, y);
```

Halide will represent this algorithm as a directed acyclic graph of Funcs, where output is a consumer of producer intermed, which in turn is a consumer of in.

The search begins with a completely unscheduled pipeline and makes decisions for each Func in the program in sequence, starting from the output. The schedule during this process is represented as a loop nest structure, where each level of the loop nest represents a given tiling. Every scheduling decision our algorithm makes transforms this loop nest, so we refer to this structure throughout as a natural way of describing this process. Different levels of the loop nest are labelled according to the type of parallelism they provide. The outer loops correspond to blocks. Immediately inside the outer block loops are thread loops, inside of which are serial loops.

At this point we start enumerating possible options but none
Figure 2: Our Hierarchical Sampling Strategy. A large, rich space of candidate options are enumerated. They are then grouped into buckets based on their structural similarity. We sample \( \log_2(B) \) representatives from each bucket. The representatives from each bucket become the final candidate states.

Figure 3: Structural Hashing: we hash options up to a given depth to stratify our search. Here, two different schedules have the same structure at depth 1 (which only considers block-level choices), but different structure at depth 2 (which considers both block- and thread-level choices). Equal hashes at low depth indicate at least coarse grained structural similarity. Equal hashes at high depth values indicate more fine grained structural similarity.

of them are actually evaluated by the cost model until they are chosen by our hierarchical sampling.

For each \texttt{Func} we make 2 decisions:
1. Where in the currently scheduled loop nest should we compute this \texttt{Func}?
2. How should we tile this \texttt{Func}?

In the first phase of the search process, we start by making decision 1. As described in Sec. 2, the options include computing the \texttt{Func} in its own kernel, fusing it into one of its consumers, or inlining it, all of which introduce a tradeoff between parallelism, locality, and redundant computation.

The coarsest granularity is to compute it at the root level of the loop nest. This corresponds to launching the \texttt{Func} in its own separate kernel. It requires no redundant recomputation but will likely exhibit poor memory locality. Its allocation will be stored in global memory, which is slow, and launching a separate kernel will incur some overhead. For \texttt{Func} output this is the only option, since it is the output of the program.

For \texttt{Funcs} that are not outputs of the program (\texttt{intermed}), they can also be computed at the root level but there are additional options. Each of these \texttt{Funcs} can be computed at the block level of their consumer for better memory locality, since output can access a tile of \texttt{intermed} right after they are computed. We further place the allocation in shared memory, which is faster than global memory and L2 cache. However, as demonstrated in Section 2, fusing may introduce redundant recompute. There is also a hardware limit on the amount of shared memory available. If a \texttt{Func} is scheduled at this level, its loops will become thread loops.

We can also compute the \texttt{Func} inside the thread level of its consumer. This further improves memory locality. Its allocation will be stored at the register level, which is the fastest type of memory. But this option may introduce significant redundant recompute and sacrifices parallelism since it will be computed serially by a single thread. Register memory is a very limited resource and large and/or dynamic allocations at this level may introduce costly local memory spilling.

The final option is to inline the \texttt{Func} directly into its consumers. This option avoids storing memory altogether so exhibits the best memory locality but can easily introduce unacceptable levels of redundant recomputation. If a \texttt{Func} consists of a single stage and is called point-wise by its consumer, we always inline it. If a \texttt{Func} is cheap to compute, it will always be considered for inlining but may be rejected later if our featurization determines that the state requires excessive recomputation.

Inline options and \texttt{Funcs} fused inside their producer’s thread loop are not considered for tiling.

Next, we need to make decision 2 of tiling the functions. \texttt{Funcs} stored at the block level of their producer will be tiled immediately, since their tiling choice will have a significant impact on the featurization and cost of their producer and
other siblings that are fused at the same block. For them we enumerate serial loop sizes so they become a set of thread loops outside serial loops.

6.1. Choosing Serial Loops

First, we enumerate inner serial loop options. These options allow loaded points to be stored in registers for faster accesses and the goal is for them to be unrolled so inputs can be reused across the unrolled loops. We do not want them to be too large because they would then reduce the amount of parallelism available at the block and thread levels and potentially increase the stride of memory accesses, which can negatively impact memory efficiency by decreasing global memory coalescing and/or increasing shared memory bank conflicts. We enumerate serial tile sizes that are small powers of 2: 1, 2, 4, and 8 in each dimension. We also consider small odd tilings (3, 5, 7) if they will enable the resulting thread loop’s extent to be a multiple of the warp size (e.g. tiling an extent of 96 with a serial loop of size 3 would enable a thread loop of 32).

At this point, the compute location has been chosen and candidates scheduled at their producer’s block have been tiled.

If we decide to compute the Func in its own kernel, we defer its tiling to the second phase of the search to reduce the number of options to be enumerated in a single phase. At that point, it will be tiled into 3 levels. First, serial loops are chosen as above.

6.2. Choosing Thread Loops

After enumerating the serial loop options, we then enumerate thread loop options. Our goal in this step is to make effective use of thread parallelism while also ensuring an adequate number of blocks at the outer level. We enumerate thread loop sizes that encourage favourable warp sizes: 16, 32, 64 in the innermost loop dimension, and powers of 2 up to 16 in the other dimensions. We select as the innermost loop dimension the first dimension with extent >= 16. If there are none, we use the first dimension.

6.3. Block Loops

The remaining loop extents after choosing thread sizes will become the outer block loops. A good schedule should aim to have sufficient parallelism (at least 2x the number of SMs on the GPU) to keep all the SMs busy and a balanced number of blocks that does not leave too many SMs idle.

Tiling decisions are made depending on the Func’s chosen compute location. If computed at the root level, we enumerate all serial and thread loop options. If computed at the block level, we enumerate all serial loop options only: the outer loop after tiling becomes a thread loop and there is no need to tile it because it is already surrounded by a block loop. And if computed inside the thread loops, tilings are not enumerated: the resulting bounds of the Func are likely too small to make tiling worthwhile.

6.4. Hierarchical Sampling

At the end of each phase, once we have enumerated the search space options for a given Func, we want to featurize and evaluate them with the cost model. But as described in Section 2, it’s not feasible to evaluate them all. Instead we apply our hierarchical sampling strategy (Section 3).

Before featurizing and evaluating the cost model, we organize all the enumerated options into buckets based on a structural hash of their loop nest. We randomly sample representatives from each bucket. These final selected options are then featurized and evaluated by the cost model and added to the beam.

6.5. Avoiding Known Bad States

The search algorithm can be run in multiple passes. During each pass, as candidate options are taken from the beam, we first compute their structural hash up to the depth dictated by the current pass. If we have previously seen that hash and the cost model informed us that it’s not a promising state, we apply a cost penalty and move it back in the priority queue. Intuitively, this helps us avoid wasting time not just on the exact state under consideration, but all states that have the same hash. If we previously sampled a state as a representative during hierarchical sampling and it is evaluated poorly by the cost model, it will serve as a negative example for all the other members of its structural hash bucket and help guide us towards structural hashes that either show promise or have not yet been explored. When computing the hash, we use the pass index as the depth (Figure 3). This means that during earlier passes an equal hash value will indicate that 2 options have at least coarse grained structural similarity. During later passes, the depth increases and an equal hash value indicates more fine grained similarity. Intuitively, in the earlier passes, we explore considering only coarse structure, then in later stages start to look at more fine grained differences between options. Our results use samples with beam search (beam size 32 with 5 passes), which will consider hashes up to depth 5, as well as greedy samples (beam size 1 with 1 pass), which will only consider hashes up to depth 1, i.e. the block level.

6.6. Pruning

The goal when enumerating the search space is to include as many plausibly good states as possible. We want to ensure we include serial tilings because register blocking and input reuse is an important optimization on some applications. We also want to ensure there are enough blocks to keep the SMs busy, while avoiding configurations that leave SMs idle, and enough warps to promote adequate latency hiding, while avoiding states that leave excess warp lanes idle. We prune states in the following situations:

• States with excessive recompute, usually caused by inlining
• States that leave too many SMs idle
• States that exhibit poor warp lane utilization
We extend Adams et al.’s schedule specific featurization to compute both algorithm specific features and schedule specific features. We design an efficient cost model for evaluating the performance of a schedule on GPU. The cost model takes a set of features generated from a program, and feeds them into a light-weight neural network. We then train the cost model to predict the performance.

We build our cost model on top of Adams et al.’s work [2]. We compute both algorithm specific features and schedule specific features. We inherit Adams et al.’s algorithm specific features, which are histograms of various arithmetic and memory operations over the entire algorithm.

7. Features

We extend Adams et al.’s schedule specific featurization to capture important characteristics of GPU architectures. These include features for capturing how the schedule uses the different types of memory available on the GPU, how effectively it utilizes the GPU’s parallelism at the block and thread levels, and the level of occupancy it achieves. In Halide, a `Func` can have multiple update stages that write to the same memory buffer. The features are computed for each update stage of the computation.

Memory access. We analyze the memory access pattern by looking at the strides of the array index access with respect to loop parameters. A suboptimal stride will typically result in poor coalescing at the global memory level or bank conflicts at the shared memory level. We use the stride to compute the number of global memory transactions or shared memory transactions required for each stage of the pipeline. We do this once for a representative regular warp of the stage and once again if there is a tail warp (when the loop size is not divisible by the warp size), which may exhibit different memory access behavior because its lanes might be underutilized. These memory access counts account for amortized loads that can be reused across unrolled inner serial loops and stores that can be moved outside the block of unrolled serial loops. In addition, we have a feature for the efficiency of loads and stores at both the global and shared levels. The efficiency is defined as the ratio of bytes used to bytes actually loaded or stored. We also compute the memory footprint accessed at various levels of a given loop nest, including per iteration of the innermost serial loop, per thread, and per block. These footprints are delineated by memory type (global, shared, register). In the case of global and register memory, the memory footprint gives a hint to the cost model as to expected cache behavior and register pressure.

Effective Parallelism To capture how effectively the GPU’s parallelism is used, we compute its number of blocks, number of warps per block, and number of threads. We compute each stage’s warp utilization, which measures how many threads of a stage’s warps are idle as a percentage of the number of threads in use across all stages computed at the block level. A low warp utilization indicates that a stage is fused alongside another stage at the block level in a way that sacrifices thread parallelism. We also compute the ratio of threads that are idle as a percentage of the total number of threads made available by the hardware.

Occupancy We compute for each stage warp, block, and shared memory occupancy. We compute the ratio of maximum active warps to the maximum number of active warps hardware limit and the ratio of maximum active blocks to the maximum number of active blocks hardware limit. We also compute the ratio of shared memory to the hardware shared memory limit. We use this to compute how much block occupancy is impacted by shared memory usage.

A complete list of our features is available in Appendix A.

7.2. Cost model

Once we have the features for each stage in the computation, we feed the features for each stage into a small neural network to predict a vector of coefficients. We then use these coefficients along with our features in a cost model to predict the performance per stage and sum over all stages. We inherit our cost model design from Adams et al.’s autoscheduler [2], but with more GPU-specific features and cost model components.

Our network accepts as input the algorithm-specific and schedule-specific features, takes the logarithm of the schedule-specific features to compress the dynamic range, and feeds both of them into a fully-connected network to produce two embedding vectors. These two embeddings are then stacked together and passed into a fully-connected network to produce a vector of positive weights.

These features and weights are then used for computing the following costs: compute, load, store, parallelism and working set. The compute cost accounts for the number of points computed and how effectively the warp lanes and SMs are utilized to compute them. The load and store costs differentiate between the different types of memory (global, shared,
One Shot:

Top 5:

Autotuned:

Figure 4: We test our autoscheduler in three different modes, which trade increased compile time and the need to take ground-truth benchmarks for increased performance. One Shot uses the cost model alone to rank choices. Top 5 compiles and benchmarks the top 5 choices as ranked by the cost model. Autotuned iteratively compiles and benchmarks sampled programs, fine-tuning the cost model to the specific application as it goes.

register). They take into account memory access patterns and the footprints of memory loaded and stored at various levels of the loop nests. The parallelism cost estimates the number of kernels and blocks launched. The working set cost captures register pressure and cache usage. The learned coefficients are applied as weights to each of these cost components. Full details are available in Appendix B.

7.3. Training Procedure

We train our cost model on a combination of random pipelines constructed from common image processing and machine learning operation building blocks [2]. Additionally, for each app in our test suite we train in a hold-one-out fashion: every other app contributes samples to the target app’s training set.

8. Results

We evaluate our autoscheduler on a diverse set of 17 imaging and machine learning programs, including 15 applications from the Halide repository: bilateral grid, local laplacian, non-local means, lens blur, camera pipe, a 32-stage stencil chain, Harris corner detection, histogram equalize, max filter, unsharp mask, interpolate, a neural network conv layer with ReLU activation, SGEMM (Single float precision General Matrix Multiply), an IIR blur, BGU (bilateral guided upsampling). To this we added a depthwise-separable convolution [23], and a learned demosaicing algorithm based on Li et al. [13].

We compare our autoscheduler against the best Halide schedules experts are capable of writing by hand, using the entire scheduling language. Our experts iteratively improved these schedules during the course of this work using the best runtimes found by the autoscheduler as a target to beat (but without looking at the generated schedules), so they represent a very high bar. In many cases these human schedules substantially improve on the ones found in the Halide repository, which were used as-is by prior work. We also compare to the best existing Halide GPU autoscheduler [20]. We use our technique in 3 different modes of operation, which trade off compile time and the ability to benchmark for quality of results:

One Shot For each application, we generate 80 samples using a cost model trained on random pipelines and all applications beside the one being tested. We take the schedule ranked best by the cost model. No benchmarking is involved in selecting the schedule. This approach is directly comparable to Sioutas et al. [20], and can run in seconds.

Top 5 Same as One Shot, but we consider the top 5 schedules according to the cost model, compile and benchmark them, and take the best. This is more representative of what a human might do – construct and benchmark several promising candidates – and it takes on the order of a minute.

Autotuning We tune each application for 20 iterations, with 80 samples per iteration. All 80 samples are compiled, benchmarked, and then used to retrain the model. This mode starts from random weights, so it does not benefit from transfer learning from other applications or random pipelines, and is in fact slower than the above two modes on one application. A total of 1600 samples are generated for each application. We take the fastest schedule found during this process. This takes tens of minutes to a few hours, depending on the program.

In all 3 modes of operation, we generate batches with 1 beam search sample (beam size = 32, 5 passes) and 79 greedy samples (beam size = 1, 1 pass).

8.1. Post-Compile Filtering

For the One Shot and Top 5 cases, we apply additional post-compile filtering: any samples that spill registers to local memory are removed from consideration. This performance cliff is hard to predict pre-compilation, because it depends on the vagaries of the underlying PTX compiler, which issues a warning when this happens. In one case (lens blur), all samples experienced register spilling. In this case we took the best sample that was within 50% of the least spilling.

All our results were generated on an IBM AC922 with 2×20 core Power9 CPUs and 4×NVIDIA V100 SXM2 cards with 32GB of memory. While this is an unusual processor, in no case was the time spent on the CPU a significant fraction of total runtime. All benchmarks were performed on a single V100 in isolation.
8.2. Analysis

We achieve a geomean speedup over Sioutas et al.\cite{20} of \(1.21 \times\) in the One Shot case, \(1.31 \times\) in the Top 5 case, and \(1.66 \times\) in the autotuning case. Our autotuned results are on par with our best known manual schedules (0.98\(\times\)).

Sioutas et al.\ generate code that fails to run on the conv layer, and performs poorly on several apps, especially those outside its test set (BGU, depthwise separable conv, and learned demosaic). Its single largest weakness is a search space issue with workloads that include matrix multiply or conv layer. A fast matrix multiplication contains an inner unrolled block over a tile of \(O(MN)\) accumulators, which share the \(O(M+N)\) loads required to compute each term. Sioutas et al. do not consider this form of unrolling. On BGU, Sioutas et al. launch every step of a per-pixel 4x4 matrix solve as its own kernel. We suspect this is due to a weakness in the manually-designed cost model.

8.3. Manual Schedules Outside the Search Space

The manual schedules outperform our autoscheduler in several instances. For both the conv layer and IIR blur, the expert schedules split and unroll the reduction loops. In BGU and histogram equalization the manual schedules use atomic floating point adds to memory to expose more data parallelism. In the conv layer, the IIR blur, the learned demosaic, and matrix multiply, the manual schedule uses warp-shuffle instructions to share data between the threads in a warp without requiring a full barrier across the entire thread block. These transformations can have significant performance advantages but are not currently in the search space of our autoscheduler. Other common patterns in the manual schedules not exploited by our autoscheduler are SIMD vectorization of load instructions to reduce the total number of memory transactions, and pre-staging of stencil inputs into shared memory to reduce the total number of loads to device memory.

Despite operating without all of these features, the autoscheduler was able to beat the manual schedules the majority of the time, and has geomean performance on par with our best efforts at manual schedules. The large gains come in the most complex, heterogeneous applications, which are intractably difficult for humans to schedule.

9. Related work

Earlier work on automatic array program optimization focused on affine transformations of loop nests (e.g., PLUTO\cite{5}, Polly\cite{8}, and PPCG\cite{25}). These works proposed that loop nests can be treated as polyhedra, and affine loop transformations can be treated as transformations on the polyhedra. This abstraction allows them to concisely express and explore many different loop optimizations, often in the form of solving an integer linear programming problem to minimize a simple cost function related to parallelism and locality.

Halide\cite{18,19} takes a slightly different approach by defining a set of domain specific rewrites to a loop nest. This allows Halide to handle a generalized form of loop fusion (called compute_at and store_at in Halide), which is essential, but was difficult to express in prior polyhedral optimizers. Early automatic schedulers in Halide used genetic algorithms
over randomly generated schedules [19, 3]. PolyMage [16] combines ideas from the polyhedral literature and Halide, and develops an automatic scheduling technique using a heuristic cost model and a greedy stage grouping algorithm, and then compiling and benchmarking over different tile sizes. This was later extended with a richer cost model and better search algorithms [11]. A parallel line of work uses a similar heuristic cost model and greedy stage grouping to handle a broader range of algorithms and schedules in Halide [15, 21], and was recently extended to target GPUs [20]. Li et al. also developed a Halide GPU autoscheduler specialized to gradient code [13], which only considers trivial loop fusion.

Adams et al. [2] noted that most previous approaches on automatically scheduling Halide programs focused on a rather restricted set of rewrites, and the heuristic cost models do not capture well the complexity of real machines. Adams et al. design a general search algorithm that can handle a broad set of scheduling rewrites, while developing a hybrid-manual-learning-based cost model that can learn the complexity of modern hardware while being efficient. Unfortunately, as we discussed throughout the paper, Adams et al.’s approach does not scale well when applied to GPU architectures, due to the significant increase of tiling options, and the lack of GPU-specific features and search pruning techniques. Adams et al. report preliminary GPU results that are 29%-33% faster than a baseline [13] that has been superseded by [20], which reports a 2×improvement over it.

Recent tensor frameworks such as TensorFlow [1] and TVM [6] are equipped with graph rewrite systems to optimize the composition of coarse-grained operators. XLA [22] applies a set of template rewrites to the computation graph using heuristic rules. TASSO [12] takes a superoptimization approach to this problem, and generates a large collection of graph rewrites from a small set of tensor relation axioms, and formally verifies them. Others attack the problem using reinforcement learning agents [17]. These techniques focus on coarse-grained rewrites of large graphs, and not the detailed decisions of how to schedule the many dimensions within each coarse-grained operator or operator group.

Complementary work focuses on optimizing individual tensor operators (or, equivalently, small local clusters as output by a higher-level graph rewritter). AutoTVM [7] automatically searches over parameters of hand-written schedule templates, using a reinforcement learning algorithm with a statistical cost model with gradient boosted trees or tree-based recurrent neural networks. FlexTensor [27] removes the need to manually specify templates by directly enumerating from a set of Halide-like program rewrites. Tensor Comprehensions [24] employs polyhedral rewrites and autotuned tile sizes. Because these systems focus on neural network workloads, dominated by individual high arithmetic intensity kernels with limited opportunity for long-range fusion due to very large stencils in the channel dimensions, they are able to focus separately on small local computation graphs where scalability is less of a challenge. In contrast, we aim to schedule a broader set of programs made up of many, more diverse, and lower arithmetic intensity operations (such as the stencil chain). Fusing and jointly scheduling stages over long ranges is crucial to performance in these cases.

Some previous works used machine learning in compiler optimization (e.g., [4, 9, 14]). In contrast to most approaches in this domain, our cost model operates on a more abstract loop representation, leverages explicit program analysis and GPU architecture knowledge.

Concurrently with our work, Haj et al. [10] recently proposed a Halide autoscheduling algorithm using Monte Carlo tree search. Zheng et al. [26] propose a tensor optimization algorithm using program sampling similar to ours. These approaches share a similar spirit to our work but with different focuses. Haj et al. focuses on CPU autoscheduling, without the scalability challenges we address, while Zheng et al. focuses on individual deep learning kernels much like AutoTVM and FlexTensor. Both approaches focus exclusively on autotuning with benchmarking and long compilation time, while we also enable fast One Shot results.

10. Limitations & Future Work

Even though we consider a large space of schedules, the space of all Halide schedules is much larger still. We currently make tiling decisions on a per-Func basis, but could make those decisions for all the update stages in a Halide function. This would allow us to tile and unroll reduction variables (sequential loops that are not directly parallelizable) in update stages, which has proven an important optimization on applications like conv layer and IIR blur. Making tiling decisions on a per-stage basis is likely also necessary to support parallelizing reductions (including the Halide scheduling options rfactor and atomic), which is an important optimization on histogram equalize.

Register spilling often has large performance impacts on the GPU, but the spilling behavior of the downstream PTX compiler can be unpredictable. Our cost model captures factors that estimate register pressure, but can sometimes fail to predict machine-assembly-level optimizations. In our one-shot mode, we include a post-processing pass to remove programs with excessive register spilling. It would be useful to extend our cost model to predict register spilling more accurately.

11. Conclusion

We present a system for automatically scheduling Halide programs on GPUs that scales to a large set of scheduling options and complex pipelines. It generates code that matches experts’ best effort to beat it with unconstrained manual schedules, and significantly outperforms the current state-of-the-art Halide GPU autoscheduler. We believe the key concepts of our method are likely useful for other array compilers outside of Halide.
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A. Featurization

We use the following GPU specific features (basic features e.g. number of productions, total points computed, etc. are reused from [2]):

- num_scalars
- points_computed_per_thread

num_scalars: The total product of the loop extents

points_computed_per_thread: The number of points of this stage computed by each thread. The product of the inner serial loops for this stage

unique_global_bytes_read_per_realization: Number of unique bytes loaded from global memory to compute a single realization of this stage

unique_shared_bytes_read_per_realization: Number of unique bytes loaded from shared memory to compute a single realization of this stage

unique_registersBytes_read_per_realization: Number of unique bytes loaded from register memory to compute a single realization of this stage

a single realization of this stage

unique_globals_lines_read_per_realization: Number of contiguous lines loaded from global memory to compute a single realization of this stage

unique_shared_lines_read_per_realization: Number of contiguous lines loaded from shared memory to compute a single realization of this stage

unique_registers_lines_read_per_realization: Number of contiguous lines loaded from register memory to compute a single realization of this stage

A. Featurization

We use the following GPU specific features (basic features e.g. number of productions, total points computed, etc. are reused from [2]):

- num_scalars
- points_computed_per_thread

num_scalars: The total product of the loop extents
**unique_global_bytes_read_per_thread** Number of unique bytes loaded from global memory to compute a single thread of this stage

**unique_shared_bytes_read_per_thread** Number of unique bytes loaded from shared memory to compute a single thread of this stage

**unique_register_bytes_read_per_thread** Number of unique bytes loaded from register memory to compute a single thread of this stage

**unique_global_lines_read_per_thread** Number of contiguous lines loaded from global memory to compute a single thread of this stage

**unique_shared_lines_read_per_thread** Number of contiguous lines loaded from shared memory to compute a single thread of this stage

**unique_register_lines_read_per_thread** Number of contiguous lines loaded from register memory to compute a single thread of this stage

**global_allocation_bytes_read_per_realization** Total sum of global memory allocation bytes accessed compute a single realization of this stage

**shared_allocation_bytes_read_per_realization** Total sum of shared memory allocation bytes accessed compute a single realization of this stage

**register_allocation_bytes_read_per_realization** Total sum of register memory allocation bytes accessed compute a single realization of this stage

**global_bytes_at_task** Number of bytes written by this stage to global memory per block

**shared_bytes_at_task** Number of bytes written by this stage to shared memory per block

**register_bytes_at_task** Number of bytes written by this stage to register memory per block

**global_innermost_bytes_at_task** Number of bytes written by this stage to global memory per block, along the innermost storage dimension

**shared_innermost_bytes_at_task** Number of bytes written by this stage to shared memory per block, along the innermost storage dimension

**register_innermost_bytes_at_task** Number of bytes written by this stage to register memory per block, along the innermost storage dimension

**num_blocks** Number of blocks used when computing this stage

**num_warps_per_block** Total number of warps per block for this stage

**num_active_warps_per_block** Number of warps per block for which this stage has at least 1 active thread

**num_threads_per_block** Number of threads per block that are used for computing this stage

**expr_branching** This stage’s Strahler number: the minimum number of registers required to evaluate this stage’s computation

**block_occupancy** Ratio of number of threads used to the hardware thread limit

**warp_lane_utilization** The ratio of active threads used by this stage to the total number of active threads available (32 × number of active warps)

**idle_lane_wastage** The ratio of idle threads in active warps to the hardware thread limit

**num_shared_mem_loads_per_block** Number of shared memory load transactions issued per block. Accounts for the number of bank conflicts of the access

**num_global_mem_loads_per_block** Number of global memory loads transactions issued per block. Accounts for the coalescing of the access

**num_shared_mem_stores_per_block** Number of shared memory stores transactions issued per block. Accounts for the bank conflicts of the access

**num_global_mem_stores_per_block** Number of global memory stores transactions issued per block. Accounts for the coalescing of the access

**shared_mem_load_efficiency** Ratio of bytes needed by the stage from shared memory to total bytes transferred by shared memory load transactions

**shared_mem_store_efficiency** Ratio of bytes stored to shared memory to total bytes transferred by shared memory store transactions

**global_mem_load_efficiency** Ratio of bytes needed by the stage from global memory to total bytes transferred by global memory load transactions

**global_mem_store_efficiency** Ratio of bytes stored to global memory to total bytes transferred by global memory store transactions

**shared_mem_store_efficiency** Ratio of bytes stored to shared memory to total bytes transferred by shared memory store transactions

**shared_mem_load_efficiency** Ratio of bytes needed by the stage from shared memory to total bytes transferred by shared memory load transactions

**global_mem_load_efficiency** Ratio of bytes needed by the stage from global memory to total bytes transferred by global memory load transactions

**working_set_at_thread** Sum of the allocation sizes at the thread level. Hint as to register pressure

**shared_mem_occupancy** For compute_ stages, ratio of total shared memory allocated at this stage’s block level to shared memory hardware limit

**shared_mem_block_limit_factor** Ratio of maximum active blocks allowable with the amount of shared memory allocated to the maximum active block hardware limit

**max_warp_occupancy** Ratio of maximum active warps to maximum active warp hardware limit

**max_block_occupancy** Ratio of maximum active blocks to maximum active block hardware limit

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**B. Cost Model Components**

In the following $c_i$ represents the $i$th coefficient predicted by the neural network.

Let $\text{select}(\text{cond}, t, f) = \text{if cond then } t \text{ else } f$;

```plaintext
compute_cost = \text{select}(\text{inlined_calls} == 0, 
num_scalars \times c_1, 
num_scalars \times c_3);
```

```plaintext
num_threads = num_blocks \times num_threads_per_block;
points_computed = num_threads \times points_computed_per_thread;
```
compute_cost += select(inlined_calls == 0,
   (points_computed * c19),
   (points_computed * c4));

idle_core_wastage = ceil(num_tasks / num_cores)
   / max(1, tasks_per_core);

compute_cost *= idle_core_wastage;
compute_cost /= select(inlined_calls == 0,
   1 - idle_lane_wastage, 1.f);

load_cost = num_realizations *
   (c5 * unique_global_lines_read_per_realization
   + c16 * unique_shared_lines_read_per_realization
   + c8 * unique_register_lines_read_per_realization
   + c6 * unique_global_bytes_read_per_realization
   + c20 * unique_shared_bytes_read_per_realization
   + c7 * unique_register_bytes_read_per_realization
   + c18 * unique_global_lines_read_per_thread
   + c17 * unique_shared_lines_read_per_thread
   + c13 * unique_global_bytes_read_per_thread
   + c11 * unique_shared_bytes_read_per_thread
   + c10 * unique_register_lines_read_per_thread
   + c12 * num_scalars * unique_bytes_read_per_point
   + c14 * num_tasks * unique_bytes_read_per_task
   + c15 * num_tasks * unique_lines_read_per_task);

global_mem_load_cost = num_blocks *
   num_global_mem_loads_per_block;
global_mem_load_cost *= select(inlined_calls == 0,
   1.f / global_mem_load_efficiency, 1);
shared_mem_load_cost = num_blocks *
   num_shared_mem_loads_per_block;
shared_mem_load_cost *= select(inlined_calls == 0,
   1.f / shared_mem_load_efficiency, 1);

load_cost += global_mem_load_cost
   + shared_mem_load_cost;

shared_mem_store_cost = c29 * num_blocks *
   num_shared_mem_stores_per_block;
global_mem_store_cost = c21 * num_blocks *
   num_global_mem_stores_per_block;
global_mem_store_cost *= select(inlined_calls == 0,
   1.f / global_mem_store_efficiency, 1);

store_cost = shared_mem_store_cost
   + global_mem_store_cost;

cost_of_false_sharing = select(inner_parallelism > 1,
   c22 * (num_scalars) /
   max(1, global_innermost_bytes_at_task), 0.0f);
store_cost += cost_of_false_sharing;

cost_of_malloc = c24 * num_realizations;

cost_of_parallel_launches = num_productions *
   select(inner_parallelism > 1, c25, 0.0f);
cost_of_parallel_tasks = num_productions *
   (inner_parallelism - 1) * c26;
cost_of_parallelism = cost_of_parallel_tasks
   + cost_of_parallel_launches;

cost_of_working_set = working_set * c9;

cost = compute_cost + store_cost + load_cost +
   cost_of_malloc + cost_of_parallelism +
   cost_of_working_set;