Trade-off analysis between PLC and FGPA for the system platform of instrumentation and control system experimental power reactor: A preliminary study

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Abstract. Programmable logic controller (PLC) has become commonly used in industrial machinery for sequence control. However, the PLC program is easy to replicate and to analyse. This factor should become a security consideration for using it as a platform for a nuclear power reactor for the Instrumentation and Control (I&C) system. Since the PLC-based system has the possibility of common cause failure, as well as cybersecurity attacks and PLCs, have to handle many complex systems. Therefore field programmable gate array (FPGA) technology is possible to be implemented as a control program with hard-wired logic for experimental power reactor (RDE) I&C system. However, another factor should become a consideration. This trade-off analysis studies are presents a systematic method to compare the performance of implement a hard-wired sequence control with FPGA and PLC using a ladder diagram. Productive PLC programs were examined with Omron CQM1 and Altera Stratix II FPGA and were shown to fit into a common FPGA chip. Straightforward Sequential design and a performance-oriented flat design was estimated to be used for time response performance. By this analysis, it hope that development of I&C system for RDE will have a unanimous decision to determine which platform to be implemented, with the consideration that the chosen platform meets the criteria as the requirement analysis from the stakeholders which it refers to the user needs to develop an availability, maintainability and reliability system essential to safety.

Keywords: PLC, FPGA, Trade-off Analysis, Ladder Diagram

1. Introduction
Since 1954, Indonesia becomes one of the countries that researches nuclear for National interest (energy, Medic and Agriculture). In 1964, the Indonesia government created the National Nuclear Energy Agency of Indonesia (BATAN) for nuclear research and development. The current development, Indonesia had developed the basic design of Experimental Power Reactor (RDE) that refers to the design of High-Temperature Gas-cooled reactor-test Module (HTR-10) type. This design is developed by Tsinghua University (China) since 1995[1]. Since the high temperatures and
potentially corrosive is the big issue is High-Temperature Gas-Cooled Reactor (HTGR) type to be combine with instrumentation system [2], for development of RDE an HTR-10 type which applying pebble bed reactor technology should be designed with a very safe covered with reliable design of system platform of Instrumentation and control.

HTR-10 is a 10 MW thermal design that early developed by Siemens Germany since 1979 and finalises by Tsinghua University (China) in 2000 [3]. The Modular HTGR is recognised for its excellent safety regarding the following features; capacity of retaining all fission products in the coated particles up to the temperature of 1600 °C. Large fuel temperature margin and negative temperature reactivity coefficient sufficient to accommodate reactivity insertion, the large heat capacity of the core to mitigate temperature transition, a small amount of excess reactivity in the core, and passive decay heat removal, also become another reasons. Figure 1 represents the design of HTR-10.

![Figure 1. Cross Section of HTR-10 Module [3].](image)

The improvement of Instrumentation and control (I&C) for the RDE design are chosen for the digital I&C system. Technology digital of Instrumentation and Control (I&C) system with Programmable Logic Controller (PLC) platform had been implemented and licensed in several types of reactor since 1980 [4] The advantage of using digital system is, easy to do verification, automatic testing, automatic calibration, and no set point drifting even though digital technology also has a lack of cybersecurity, common cause failure[5]. For this reasons, Field Programmable Gate Array (FPGA)
become the new technology that can replace PLC because this platform that is relatively easy to verify, validate, and ultimately license [6].

However, before deciding to choose PLC platform or FPGA platform for the I&C-based system, we have to develop trade-off analysis to compare the availability, maintainability and reliability this platform so that RDE will be developed with verified and reliable based system.

2. Theory

2.1. Trade-off Analysis

Trade-off analysis is a project management activity which covered by system engineering approach, that will help the project manager to decide from two or more item that becomes an important issue which the best choice that can be overwhelming the project. In the RDE design, for keep using PLC, we still need to develop reverse engineering program because we cannot only refer to the previous design from Tsinghua University, but we must find the lack of previous design or doing research for the improvement. After that, trade-off analysis is developed to compare the performance of PLC and FPGA as a platform for Instrumentation and control Figure 2 is representing the analytical hierarchy process to check the performance of the system. These studies can be developed by collecting data from the previous platform which is PLC, then compare with FPGAs performance.

![Analytical Hierarchical Process](image)

**Figure 2.** Analytical Hierarchical Process.

2.2 Programmable Logic Controller (PLC)

PLC was produced for use generally in industrial environments. The programmable logic controller is commonly used by manufacture as Machinery controller and can handle more than 10,000 I/O, for different control processes many input and output ports are integrated on PLC. In addition to this some communication protocols which are being used in industrial application, are present on PLC. As a short description PLC is a microcomputer which has communication protocols, input and output ports to control and manage the processes or systems [7]. Figure 3 shows the basic internal structure of the PLC.

For programming language of PLC are primarily based on the International Electrotechnical Commission (IEC) 61131-3 standard. This standard contains two types of programings such as Text Style Programming (IL and Mnemonics) and Graphics style programming (LD, FB and SFC) [8]. For
further development, the Instruction List (IL) PLC programming can be developed become Object Oriented Programming (OOP) based [7].

![Figure 3. Basic Internal Structure of PLC](image)

2.3 Field Programmable Gate Array (FPGA)

Field-programmable gate arrays (FPGAs) are reprogrammable silicon chips that invented the first FPGA in 1985 by Ross Freeman; the co-founder of Xilinx. FPGA chip adoption across all industries is driven by the fact that FPGAs combine the best parts of application-specific integrated circuits (ASICs) and processor-based systems. FPGAs provide hardware-timed speed and reliability, but they do not require high volumes to justify the significant upfront expense of custom ASIC design [9].

![Figure 4. Basic Internal Structure of FPGA](image)

Reprogrammable silicon also has the same resilience of software running on a processor-based system, but the number of processing cores available does not limit it. Unlike processors, FPGAs are truly capable in parallel processing, so different processing operations do not have to compete for the same resources. Each independent processing task is assigned to a dedicated section of the chip and can function autonomously without any influence from other logic blocks. As a result, the performance of one part of the application is not affected when another processing adds. Figure 4 shows the basic internal structure of FPGA.
3. Methodology
For developing trade-off analysis, there is an activity that can be managed by comparing the PLC platform with FPGA platform:

- Develop Analytical Hierarchy Diagram
- Timing analysis between PLC and FPGA
- Ladder diagram analysis

4. Discussion

4.1. Background
Programmable logic controller (PLC) has played a crucial role in the automatic control field (e.g., for industrial automation) since the 1970s. However, the efficiency of PLC usually relies on the CPU frequency, due to the design of PLC used to adopt the following processor solution. This is had limited the application of PLC. To fulfil the requirements from these fields, the conventional millisecond-level PLC controller, in itself, must be improved to respond to the peripherals rapidly, to have high-speed communications, and to execute the control logic concurrently. This called as a PLC cyclic time as the process and the time measure of the process are called Scan Time as described in Figure 5. The shorter time of scan time, represent more responsive The PLC.

![Figure 5. PLC Scan Time](image)

Within the development of digital technology, the development of a programmable logic device (PLD) and a field-programmable gate array (FPGA) nowadays, it can achieve of having high-speed process such as PLCs which are based on FPGA because of the parallel execution mechanism. In this manner, the performance of the controller can be improved. Therefore, designing high-speed, FPGA-based PLCs becomes a trend [10][11].

4.2. Ladder Diagram to FPGA Hardware
To generate a logic circuit from the ladder diagram, it is straightforward to design a sequential circuit, which activates one rung for each cycle in due order. This design is illustrated in Figure 6 and is designated by Sequential design in the following discussion. Although Sequential design reproduces the exact behaviour of a ladder program, it requires $\rho + 2$ cycles for each scan. Here, $\rho$ is the number of rungs of a ladder, and two additional cycles are required for input phase and output phase described in Section 3.1. The circuit is driven by $(\rho + 2)$-phase non overlapping clocks $(\phi_0, ..., \phi_{\rho+1})$. For further reduction of scan time, it is essential to utilise parallelism in the control program [13]. For example, that will be tested in this study are display in Figure 7.
To measure the Performance between PLC and FPGA, the design of ladder diagram and logic graph in FPGA can be performed in 2 type design.

4.2.1. Levelized Design.
The levelized design is which activates in one rung for each cycle in due order. In this design, the overlapping program will be impacted to scan time and can become dependence on each other. In Figure 8 the 3 cases of dependencies can be used to measure the scan time.
4.2.2. Straightforward Design.

Straightforward design is a Sequential design activates that the circuit of each rung, one for each cycle, in due order. Levelized design activates the circuit block of each level, one for each cycle, from upstream to downstream. This brings up the question of why a sequential logic circuit implements it at all. It is not necessary to split the execution phase into cycles, because the inputs and outputs are revised only at the end of each scan. In fact, it is possible to implement the execution phase by a combinatorial logic circuit.

4.3. Analyses

This section will be presenting some evaluation results of two sample PLC programs. Broken lines in Fig 8 show the evaluation flow. First, the scan time of PLC (H) is estimated from its instruction sequence (B) according to the execution time for each instruction. Since the execution time of each instruction is dependent on the value of the corresponding condition part, the worst-case scan time is estimated in this evaluation. The PLC instruction sequence is then translated into the hardware description in VHDL by Software translator (C) and implemented in FPGA Device.

As proposed by Shuishi [13], the sample result analysis for a scan time of PLC and FPGA can be seen in Table 1. However, the PLC that proposed is different.

| Device | Design | Arithmetic unit | Number of states | Maximum frequency (MHz) | Logic scale (ALUT) | Memory (bit) | DSP elements | Scan time (s) |
|--------|--------|-----------------|-----------------|-------------------------|-------------------|-------------|--------------|---------------|
| PLC    | Sequential | Dedicated       | 74              | 8.47                    | 5850              | 1280        | 56           | 1.61 x 10^-3 |
|        | Shared ×1 | 74              | 6.50            | 2859                    | 1280              | 8           | 8            | 8.74 x 10^-6 |
|        | Levelized | Dedicated       | 12              | 8.09                    | 5681              | 0           | 56           | 1.14 x 10^-5 |
|        | Shared ×1 | 17              | 6.81            | 2704                    | 0                 | 8           | 8            | 1.50 x 10^-6 |
|        | Shared ×2 | 14              | 6.48            | 3961                    | 0                 | 16          | 8            | 2.50 x 10^-6 |
|        | Shared ×3 | 13              | 6.35            | 5010                    | 0                 | 24          | 8            | 2.05 x 10^-6 |
|        | Shared ×4 | 12              | 6.57            | 6309                    | 0                 | 32          | 8            | 1.83 x 10^-6 |
| Flat   | Dedicated | 1               | 5.00            | 4624                    | 0                 | 56          | 8            | 2.00 x 10^-7 |

5. Conclusion

This study outlined a systematic method to implement a hardwired sequence control from PLC software, which includes a converter that translates PLC instruction sequence into the logic description, a control logic library to support various PLC instructions and peripheral devices, a design
framework that integrates control logic and peripheral functions on an FPGA chip, and an experimental FPGA control board. The purpose is to compare the advantages of PLC and FPGA with two sample ladder programs were examined and evaluated. The PLC that propose is OMRON CQM1 and Altera Stratix II FPGA. From other research, the performance advantage FPGA over PLC technology was obvious. In case of a productive ladder program, the Sequential design was estimated to be 184 times faster than PLC, and Flat design was 44 times faster than Sequential design (i.e., 8050 times faster than PLC) [13].

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