A 700µW 1GS/s 4-bit Folding-Flash ADC in 65nm CMOS for Wideband Wireless Communications

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Abstract—We present the design of a low-power 4-bit 1GS/s folding-flash ADC with a folding factor of two. The design of a new unbalanced double-tail dynamic comparator affords an ultra-low power operation and a high dynamic range. Unlike the conventional approaches, this design uses a fully matched input stage, an unbalanced latch stage, and a two-clock operation scheme. A combination of these features yields significant reduction of the kick-back noise, while allowing the design flexibility for adjusting the trip points of the comparators. As a result, the ADC achieves SNDR of 22.3 dB at 100MHz and 21.8 dB at 500MHz (i.e. the Nyquist frequency). The maximum INL and DNL are about 0.2 LSB. The converter consumes about 700µW from a 1-V supply yielding a figure of merit of 65fJ/conversion step. These attributes make the proposed folding-flash ADC attractive for the next-generation wireless applications.

I. INTRODUCTION

Next-generation 5G wireless communications would use millimeter wave bands between 30 and 300GHz [1]. The use of such wide spectrum allows the implementation of transceivers with high-dimensional antenna arrays for analog or digital beamforming. For many applications, however, the overall power consumption of the transceiver would be a key design parameter. In analog beamforming, the incoming signals from the antenna array are combined in the analog domain and processed by a single pair of ADC. In contrast, the digital beamforming uses a pair of ADC for each antenna element. The architecture of the digital beamforming is more flexible than the analog beamforming, thus making the digital beamforming more popular for the implementation of cellular transceivers [1]. However, for a transceiver with large antenna array, the high number of ADCs might lead to significant increase in the power consumption. A recent report by Orhan et. al shows the possibility of reducing the overall power consumption of a fully digital transceiver without compromising its performance by reducing the bit resolution of the high-speed ADCs [2].

Previous works have shown high-speed flash ADCs with low-bit resolution for applications in wideband transceivers [3], [4]. Although conventional flash ADCs have high speed, their power consumption is high because they require $2^N - 1$ comparators for an N-bit conversion. The application of signal folding technique in flash ADCs can reduce the number of comparators while maintaining the high conversion rates, thereby giving rise to significant improvement of key design parameters including the power consumption, the kickback noise, and the chip area [5], [6].

In this work, we introduce a low-power 4-bit 1GS/s folding-flash ADC with folding factor of two. We propose an unbalanced comparator, which significantly improves the power consumption and the kick-back noise of the ADC. The ADC consumes as low as 700µW from a 1V supply, giving a figure of merit (FoM) of 65fJ/conversion step. The paper structure is as follows: section II describes the system architecture, section III describes the key design considerations of the comparator, and section IV presents the simulation results.

II. SYSTEM ARCHITECTURE

Fig. 1 shows the architecture of the proposed folding-flash ADC. The ADC comprises a track-and-hold (T/H) circuit, a 1-bit folding stage, a 3-bit flash ADC, and a digital encoder. Two important design parameters in high-speed folding-flash ADCs are the linearity of the folding stage and the kick-back noise, where the kick-back noise arises from the high frequency switching in comparators. To increase the linearity, the sampling capacitor ($C_s$) should be larger than the total parasitic capacitance at the input nodes of the comparator [5]. A sufficiently large $C_s$ can also reduce the kick-back noise, generated primarily by the comparators in the 3-bit ADC [6]. The optimal value of $C_s$ in our design is 500fF.

Fig. 2a illustrates the timing diagram of the clock signals. All clock waveforms are generated by feeding an external clock to an inverter chain to produce the desired timing of these signals, shown in Fig.2b. To improve the accuracy of the ADC, $CK_1$ and $CK_2$ signals are generally out of phase with respect to the $CK_{TR}$ signal. In our design, $CK_1$ occurs 100ps after the hold phase to accommodate for the settling time of $C_s$, while $CK_2$ takes place 100ps before the next track cycle to account for the 3-bit ADC decision time.
The chopper circuit shares the charge on the sampling capacitor $C_s$ with the parasitic input capacitance of the 3-bit flash ADC during $CK_1$. The parasitic input capacitance of the 3-bit ADC is reset to zero during the tracking phase to remove the residual charge from the previous sample. In our design, the comparators in the 3-bit ADC are unbalanced with built-in references to quantize the input signal. The output signals of the 3-bit flash ADC are in the form of a thermometric code. The code is then passed to a digital encoder, which incorporates a first-order bubble correction for producing a more accurate gray code.

### III. Circuit Design

#### A. Conventional double-tail comparator

Fig. 3a shows the transistor-level architecture of a double-tail comparator. The double-tail comparator is commonly used in data converters due to its high speed, low offset, and low static power consumption [7].

To eliminate the conventional resistor ladder in the flash ADC architecture, it is desirable to implement built-in references. This is typically done by introducing an intentional offset at the input of the comparator. There are different methods for implementing this offset. One approach involves using different size input transistors [3], [4] to make their transconductance different from one another. This, however, makes the input capacitance highly imbalanced, which can result in unpredictable kick-back noise and degrade the linearity.

Another approach to program the offset is by varying the capacitive load difference at the $mid_p$ and $mid_n$ nodes of the circuit ($C_{diff} = C_{midp} - C_{midn}$) and keeping the input $M_1$ and $M_2$ transistors balanced. The shift in the trip point (i.e. $V_{offset}$) is given by the following expression [9]:

$$V_{offset} = \frac{I_D}{g_{m1,2}} \frac{C_{diff}}{C_{sum}} = \frac{V_{out,2}}{2} \frac{C_{diff}}{C_{sum}}$$  \hspace{1cm} (1)$$

where $C_{sum}$ is the total load capacitance in the balanced case, $I_D$, $g_{m1,2}$ and $V_{out,2}$ are the drive current, transconductance, and overdrive voltage of the input pair in saturation region. To implement the capacitive load difference, Verbruggen et al. added an MOS capacitor at the $mid_p$ node of the circuit [5]. This modification changes the slew rate of the input transistors, and the resulting regenerative action of the cross-coupled inverters for implementing the built-in reference. The potential drawbacks of this approach are the reduced linearity and larger comparator size. Alternatively, D’Amico et al. has implemented the offset by mismatching the size of the $M_3$ and $M_4$ transistors [6]. One shortcoming of this implementation is the difference in the amount of the charge.

Fig. 3: Schematic of (a) conventional double-tail comparator and (b) proposed double-tail comparator.
injection at the mid_p and mid_n nodes during the discharge phase, which can potentially give rise to an erroneous decision by the comparator.

B. Proposed double-tail comparator

To overcome the aforementioned shortcomings of the previous implementations, we introduce a new double-tail comparator, shown in Fig.3b. The new features of our design include: (1) implementation of the built-in reference by choosing different size reset transistors M1 and M2, (2) reduction of the kick-back noise by adding the intermediate M_k transistors and implementing a two-clock operation. It should be noted that the use of a two-clock operation without adding the M_k transistors results in the increase of the power consumption. We describe these features in the subsequent sections.

1) Implementation of built-in reference: The 3-bit ADC consists of 7 comparators with different trip points. For each comparator, we implement the offset by mismatching the size of the reset transistors. To explain the mechanism for creating the built-in offset in our circuit, we refer to Fig.3a. Transistors M1, M2, M3, M4, M_R1 and M_R2 contribute to the total parasitic capacitance (C_sum) at the mid_p and mid_n nodes. Assuming that M1, M2, M3, and M4 transistors are fully matched, only the reset transistors contribute to the difference in the capacitive loads at those nodes:

\[ C_{diff} = C_{gsR1} + C_{gdr1}(1 + A_{cc}) - [C_{gsR2} + C_{gdr2}(1 + A_{cc})] \]  
(2)

where A_{cc} is the gain of the cross-coupled inverter. Further, given the large gain of the cross-coupled inverter, we ignore the contribution of the M1, M2, M3, M4 transistors to C_sum. We can therefore express C_sum as:

\[ C_{sum} = C_{gsR1} + C_{gdr1}(1 + A_{cc}) + [C_{gsR2} + C_{gdr2}(1 + A_{cc})] \]  
(3)

Since the reset transistors are operating in the triode region, the parasitic capacitance of the transistors is given by:

\[ C_{gs} = C_{gd} = C_{ox} \times W \times L \]  
(4)

Combining the equations 2, 3, and 4, and also assuming that the reset transistors have similar gate length L, we re-write the equation 1 as:

\[ V_{offset} = \frac{V_{ov} W_{R1} - W_{R2}}{2 W_{R1} + W_{R2}} \]  
(5)

We use this simplified model to estimate the size of the reset transistors. Although the offset can be easily implemented by mismatching the size of the reset transistors, it is critical to match the capacitive load at the out_p and out_n nodes. Otherwise, this might result in a significantly large, undesirable offset [9]. Therefore, to match the load at these nodes, we connect the output nodes of each comparator to a buffer inverter.

2) Reduction of kick-back noise: The kick-back noise occurs due to high-frequency voltage swings across the input transistors of a comparator. The cumulative kick-back noise of all comparators in the 3-bit ADC can be large enough to corrupt the sampled signal. Therefore, it is essential to reduce the kick-back noise of each comparator. We now proceed to explain the origin of the kick-back noise and strategies for mitigating it.

In a double-tail comparator, the decision phase starts when the CK signal transitions from the low state to the high state. At this time, the mid_p and mid_n nodes begin to discharge into the ground. This subsequently lowers the drain-source voltage of the input transistors and pushes them from the saturation region into the triode region. The change in the operating region of the input transistors creates a kick-back charge that results in a noise (i.e. kick-back noise) at the input nodes of the comparator. Therefore, the kick-back noise corrupts the sampled signal in a single-clock operation scheme. To mitigate this problem, we used a two-clock scheme for operating the 3-bit ADC comparators, shown in Fig.3b. In our scheme, there is enough time to refresh the input of the 3-bit ADC during \( t_{rfsh} \) before the decision phase, thereby mitigating the effect of the kick-back noise. However, using the two-clock operation for a conventional double-tail comparator will significantly increase the static power consumption due to the direct path between the supply voltage \( V_{DD} \) and the ground during \( t_{rfsh} \). To alleviate this problem, we have added the intermediate M_K transistors. The size of these transistors influence the kick-back noise. Therefore, we optimized the size of these transistors to diminish the kick-back noise during the decision phase.

We also used the proposed architecture shown in Fig.3b for implementing the front-end folding comparator. Unlike the comparators in the 3-bit ADC, this comparator is fully balanced (no mismatch between M_R1 and M_R2) and uses a single-clock operation scheme. Finally, we have verified the possibility to calibrate the ADC against any process variations using the bulk voltage trimming [10].

IV. SIMULATION RESULTS

The proposed ADC was designed in a standard 65nm CMOS process with a supply voltage of 1V to operate at
A differential signal of $500mV_{p-p}$ is given to the input of the ADC. According to our simulation results, the conventional double-tail comparator exhibits a kick-back noise of around $20mV$ (0.64LSB) while this value is about $3mV$ (0.1LSB) for the unbalanced comparator with a double-clock operation scheme. Fig. 5 shows the simulation results for the system linearity, where the maximum DNL and INL are less than 0.2LSB.

The FFT plots for the input frequencies of 100MHz and 500MHz are shown in Fig. 6. The SNDR and ENOB are 22.3dB and 3.42 bits at 100MHz while they are 21.8dB and 3.34 bits at 500MHz. Table I summarizes the performance of the ADC. The ADC consumes about 700µW of which the T/H circuit, the comparators, the clock generator, and the encoder consume about 10%, 25%, 45% and 20%, respectively. Figure of Merit (FoM) of the system was evaluated using the following expression [11]:

$$FoM = \frac{\text{power}}{2\times\text{ENOB} \times f_{\text{sample}}}$$

We deduced the FoM of the ADC to be 65fJ/conversion step. These attractive specifications of our ADC make it promising for emerging applications in wideband communications such as fully digital transceivers [2].

### V. ACKNOWLEDGMENTS

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**Fig. 5: DNL and INL for different output code words.**

**CONCLUSION**

We introduced an unbalanced comparator architecture for realizing ultra-low power high-speed ADCs with low-bit resolution. We designed a 4-bit 1GS/s ADC in 65nm CMOS, which consumes 700µW. This translates into an FoM of 65fJ/conversion step. These attractive specifications of our ADC make it promising for emerging applications in wideband communications such as fully digital transceivers [2].

### TABLE I: Performance summary

| Technology       | 65nm CMOS |
|------------------|-----------|
| Supply voltage   | 1 V       |
| Sampling rate    | 1GS/s     |
| Number of Bits   | 4         |
| Input Swing      | $500mV_{p-p}$ |
| SNDR at 100MHz   | 22.3 dB   |
| SNDR at 500MHz   | 21.8 dB   |
| Power            | 700µW     |

### TABLE II: Comparison of the proposed folding-flash ADC with other high-speed ADCs

| Ref. | Architecture | Power (mW) | Fs (GHz) | Res. (Bits) | SNDR (dB) | FoM (fJ/conv.) |
|------|--------------|------------|----------|-------------|-----------|----------------|
| [3]  | Flash        | 2.5        | 1.25     | 4           | 25.8      | 160            |
| [5]  | Folding Flash| 2.2        | 1.75     | 5           | 28.5      | 50             |
| [6]  | Folding & Int. Flash | 7.65 | 1 | 5 | 27.4 | 390 |
| [8]  | Delay line   | 1          | 1        | 4           | 21.3      | 126            |
| This Work | Folding Flash | 0.7      | 1 | 4 | 22.3 | 65         |

**Fig. 6: Power spectral density of 100MHz and 500MHz input signals sampled at 1GS/s.**