Fast Simplified Successive-Cancellation List Decoding of Polar Codes

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Abstract—Polar codes are capacity achieving error correcting codes that can be decoded through the successive-cancellation algorithm. To improve its error-correction performance, a list-based version called successive-cancellation list (SCL) has been proposed in the past, that however substantially increases the number of time-steps in the decoding process. The simplified SCL (SSCL) decoding algorithm exploits constituent codes within the polar code structure to greatly reduce the required number of time-steps without introducing any error-correction performance loss. In this paper, we propose a faster decoding approach to decode one of these constituent codes, the Rate-1 node. We use this Rate-1 node decoder to develop Fast-SSCL. We demonstrate that only a list-size-bound number of bits needs to be estimated in Rate-1 nodes and Fast-SSCL exactly matches the error-correction performance of SCL and SSCL. This technique can potentially greatly reduce the total number of time-steps needed for polar codes decoding: analysis on a set of case studies show that Fast-SSCL has a number of time-steps requirement that is up to 66.6% lower than SSCL and 88.1% lower than SCL.

I. INTRODUCTION

Polar codes are a class of error-correcting codes introduced by Arıkan in [1]. They can provably achieve channel capacity on a memoryless channel when the code length $N$ tends to infinity. The first polar code decoding algorithm to be proposed is the successive-cancellation (SC), that can be represented as a binary tree search with complexity $O(N \log_2 N)$. The full search can be completed in $2N − 2$ time-steps [2]. Various works in the past [3], [4] have analyzed the nature of the nodes of the SC tree, noting that nodes whose leaves present certain patterns of information and redundancy bits, do not need to be traversed.

While SC decoding is very effective when applied to polar codes with $N \to \infty$, its error-correction performance degrades very quickly with short and medium codes. Alternative decoding algorithms have been proposed to overcome this issue, among which successive-cancellation list (SCL) is one of the most promising [5]: instead of focusing on a single candidate codeword like SC, the $L$ most probable candidate codewords are allowed to survive concurrently. The error-correction performance of polar codes under SCL decoding, when concatenated with a cyclic redundancy check, has been shown to be comparable to that of some low-density parity-check codes used in current standards. SCL yields better error-correction performance than SC at the cost of additional latency, requiring $2N + K − 2$ time-steps to be completed [6], where $K$ is the number of information bits in the code. The technique proposed in [7] applies the tree pruning methods devised for SC to SCL, but is based on heuristics and needs to be redesigned every time code parameters are modified.

The authors proposed in [8], [9] a sphere-based approach to list decoding of polar codes, that has led to the development and implementation of the simplified successive-cancellation list (SSCL) decoding algorithm [10], [11]. SSCL guarantees significant reduction in the number of required time-steps with respect to SCL without relying on approximations or code-specific design. Thus, it can be applied to any code and yields exactly the same error-correction performance of SCL.

This work proposes a simpler decoder for one of the special nodes used in SCL and SSCL, the Rate-1 node. Without any kind of error-correction performance degradation, it is able to decode a Rate-1 node of length $N_v$ in $\min\{L − 1, N_v\}$ time-steps, against the $N_v$ and $3N_v − 2$ required by SSCL and SCL respectively. This Rate-1 node decoder is then used instead of the Rate-1 node decoder of SSCL. We call the decoder that incorporates the new Rate-1 decoder “Fast-SSCL”. Given that in practical polar codes there are many instances of Rate-1 nodes where $L \ll N_v$, we show that the proposed Fast-SSCL can speed up the SSCL decoder of up to 66.6%.

The rest of the paper is organized as follows. Section II briefly introduces polar codes and the SC, SCL and SSCL decoding algorithms. Section III describes the novel decoding approach for the Rate-1 node, and provides proof of its exactness. In Section IV the reduction in the number of decoding time-steps is quantified and compared to previous results for a set of polar codes. Section V draws the conclusions.

II. POLAR CODES ENCODING AND DECODING

A polar code is represented by $P(N, K)$ and can be constructed by concatenating two polar codes of length $N/2$. This recursive construction can be denoted as a matrix multiplication as $x = u G_{\otimes n}$, where $u = \{u_0, u_1, \ldots, u_{N-1}\}$ is the sequence of input bits, $x = \{x_0, x_1, \ldots, x_{N-1}\}$ is the sequence of coded bits, and $G_{\otimes n}$ is the $n$-th Kronecker product of the polarizing matrix $G = \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix}$. The encoding process involves the determination of the $K$ bit-channels with the best channel characteristics and assigning the information bits to them. The remaining $N − K$ bit-channels are set to a known value known at the decoder side. They are thus called frozen bits with set $\mathcal{F}$. Since the value of these bits does not have an impact on the error-correction performance of polar codes on a symmetric channel, they are usually set to 0. The codeword $x$ is then modulated and sent through the channel. In
this paper, we consider BPSK modulation which maps \{0, 1\} to \{+1, -1\).

### A. Successive-Cancellation Decoding

The binary tree shown in Fig. 1 represents the SC decoding process of \(P(8, 5)\). For a node of length \(N_v\), soft logarithmic likelihood ratio (LLR) values \(\alpha = \{\alpha_0, \alpha_1, \ldots, \alpha_{N_v-1}\}\) pass from parent to child nodes, while the hard bit estimates \(\beta = \{\beta_0, \beta_1, \ldots, \beta_{N_v-1}\}\) follow the opposite direction.

The \(\frac{N_v}{2}\) elements vectors \(\alpha' = \{\alpha_0', \alpha_1', \ldots, \alpha_{N_v-1}'\}\) and \(\alpha' = \{\alpha_0', \alpha_1', \ldots, \alpha_{N_v-1}'\}\) can be computed as

\[
\alpha_i' = \arctan \left( \frac{\tanh \left( \alpha_i + \frac{N_v}{2} \right)}{2} \right), \quad (1)
\]

\[
\alpha_i' = \alpha_i + \frac{N_v}{2}, \quad (2)
\]

whereas the \(N_v\) values of \(\beta\) are calculated by means of the left and right messages \(\beta' = \{\beta_0', \beta_1', \ldots, \beta_{N_v-1}'\}\) and \(\beta' = \{\beta_0', \beta_1', \ldots, \beta_{N_v-1}'\}\) as

\[
\beta_i = \begin{cases} 
\beta_i + \beta_i', & \text{if } i < \frac{N_v}{2}, \\
\beta_i' - \frac{N_v}{2}, & \text{otherwise}, 
\end{cases} \quad (3)
\]

where \(\oplus\) is the bitwise XOR operation. Bits in the left and right child nodes are distinguished by \(i < \frac{N_v}{2}\). At leaf nodes, the \(i\)-th bit \(\hat{u}_i\) can be estimated as

\[
\hat{u}_i = \begin{cases} 
0, & \text{if } i \in \mathcal{F} \text{ or } \alpha_i \geq 0, \\
1, & \text{otherwise}. 
\end{cases} \quad (4)
\]

Equation (1) can be reformulated in a more hardware-friendly (HWF) version that has first been proposed in [2]:

\[
\alpha_i = \text{sgn}(\alpha_i) \text{sgn}(\alpha_{i+\frac{N_v}{2}}) \min(|\alpha_i|, |\alpha_{i+\frac{N_v}{2}}|). \quad (5)
\]

### B. Successive-Cancellation List Decoding

The error-correction performance of SC when applied to codes with short to moderate length can be improved by the use of list-based decoding. The SCL algorithm estimates a bit considering both its possible values 0 and 1. At every estimation, the number of codeword candidates (paths) doubles; in order to limit the increase in the complexity of this algorithm, only a set of \(L\) codeword candidates is memorized at all times. Thus, after every estimation, half of the paths are discarded. To this purpose, a path metric (PM) is associated to each path and updated at every new estimation: it can be considered a cost function, and the \(L\) paths with the lowest PMs are allowed to survive. In the LLR-based SCL [6], the PM can be computed as

\[
\text{PM}_i = \sum_{j=0}^{l} \ln \left(1 + e^{-(1-2\hat{u}_j)\alpha_{ij}}\right), \quad (6)
\]

where \(l\) is the path index and \(\hat{u}_j\) is the estimate of bit \(j\) at path \(l\). A HWF version of Equation (6) has been proposed in [6]:

\[
\begin{align*}
\text{PM}_{i-1} &= 0, \\
\text{PM}_i &= \begin{cases} 
\text{PM}_{i-1} + |\alpha_{ij}|, & \text{if } \hat{u}_j \neq \frac{1}{2} (1 - \text{sgn}(\alpha_{ij})), \\
\text{PM}_{i-1}, & \text{otherwise}, 
\end{cases} \quad (7)
\end{align*}
\]

which can be rewritten as

\[
\text{PM}_i = \frac{1}{2} \sum_{j=0}^{l} \text{sgn}(\alpha_{ji})\alpha_{ji} - (1 - 2\hat{u}_j)\alpha_{ji}. \quad (8)
\]

### C. Simplified Successive-Cancellation List Decoding

SC decoding requires the traversal of the whole decoding tree. The Fast Simplified SC (Fast-SSC) algorithm in [4] reduces the SC time requirements by exploiting the fact that polar codes are constructed by concatenation of smaller codes. It identifies different constituent codes which can be decoded with efficient maximum likelihood decoding techniques, avoiding traversing parts of the decoding tree. In particular, Fast-SSC makes use of Rate-0 nodes which have only frozen bits, Rate-1 nodes consisting of information bits only, Repetition (Rep) nodes which have only frozen bits except for the rightmost one, and Single Parity-Check (SPC) nodes that are made of information bits only except for the leftmost one. The advantage of Fast-SSC is that not only it requires fewer time-steps than SC to finish the decoding process, but also it provides an exact match to SC with no error-correction performance loss.

The SSCL algorithm in [10] provides efficient decoders for Rate-0, Rep, and Rate-1 nodes in SCL without traversing the decoding tree while guaranteeing the error-correction performance preservation. For example in Fig. 1 the black circles represent Rate-1 nodes, the white circles represent Rate-0 nodes, and the white triangles represent Rep nodes. The pruned decoding tree of SSCL for the example in Fig. 1 is shown in Fig. 2 which consists of a Rep node and a Rate-1 node.

Let us consider that the vectors \(\alpha_i\) and \(\alpha_i = 1 - 2\beta_i\) are relative to the top of a node in the decoding tree. It was shown...
in [11] that Rate-0 nodes can be decoded in a single time-step as
\[ \text{PM}_{N_0-1} = \begin{cases} \sum_{i=0}^{N_0-1} \ln (1 + e^{-\alpha_i}), & \text{Exact, (9a)} \\ \frac{1}{2} \sum_{i=0}^{N_0-1} \text{sgn}(\alpha_i) \alpha_i - \eta_i, & \text{HWF. (9b)} \end{cases} \]

Rep nodes can be decoded in two time-steps as
\[ \text{PM}_{N_0-1} = \begin{cases} \sum_{i=0}^{N_0-1} \ln (1 + e^{-\eta_{N_0-1} \alpha_i}), & \text{Exact, (10a)} \\ \frac{1}{2} \sum_{i=0}^{N_0-1} \text{sgn}(\alpha_i) \alpha_i - \eta_i \alpha_i, & \text{HWF. (10b)} \end{cases} \]

where \( \eta_{N_0-1} \) represents the bit estimate of the information bit in the Rep node. Finally, Rate-1 nodes can be decoded in \( N_0 \) time-steps as
\[ \text{PM}_{N_0-1} = \begin{cases} \sum_{i=0}^{N_0-1} \ln (1 + e^{-\alpha_i}), & \text{Exact, (11a)} \\ \frac{1}{2} \sum_{i=0}^{N_0-1} \text{sgn}(\alpha_i) \alpha_i - \eta_i \alpha_i, & \text{HWF. (11b)} \end{cases} \]

While the SSCL algorithm reduces the number of required time-steps to decode Rate-1 nodes by almost a factor of three, it fails to address the effect of list size on the maximum number of required bit estimations. In the following section, we prove that the number of required time-steps to decode Rate-1 nodes depends on the list size and that the new Fast-SSCL algorithm is faster than both SCL and SSCL without incurring any error-correction performance degradation.

III. FAST SIMPLIFIED SUCCESSIVE- cancellation LIST DECODING

In this section, we propose a fast decoding approach for Rate-1 nodes and use it to develop Fast-SSCL. In order to prove that it is exact and that no approximation is introduced with respect to SCL and SSCL decoding, we first introduce the following lemma.

Lemma 1. For two positive real numbers \( a \) and \( b \) where \( a < b \), the following holds:
\[ \ln (1 + e^{-a}) + \ln (1 + e^b) > \ln (1 + e^a) + \ln (1 + e^{-b}) \]  (12)

Proof: We prove
\[ \ln (1 + e^{-a}) + \ln (1 + e^b) - \ln (1 + e^a) - \ln (1 + e^{-b}) > 0. \]

We can write
\[ \ln (1 + e^{-a}) + \ln (1 + e^b) - \ln (1 + e^a) - \ln (1 + e^{-b}) = \ln \left( \frac{1 + e^{-a}}{1 + e^a} \right) + \ln \left( \frac{1 + e^b}{1 + e^{-b}} \right) = \ln (e^{-a} + 1 + e^b) + \ln \left( \frac{1 + e^b}{1 + e^{-b}} \right) = \ln (e^{-a}) + \ln (e^b) = b - a > 0, \]  (13)

which proves the lemma.

The fast Rate-1 decoder can be summarized by the following theorem and its subsequent proof.

Theorem 1. In SCL decoding with list size \( L \), the maximum number of bit estimations in a Rate-1 node of length \( N_0 \) required to get the exact same results as the conventional SCL decoder is
\[ \min (L - 1, N_0). \]  (14)

The proposed technique improves the required number of time-steps to decode Rate-1 nodes when \( L - 1 < N_0 \). Every bit after the \( L - 1 \)-th can be obtained through hard decision on the LLR as
\[ \beta_i = \begin{cases} 0, & \text{if } \alpha_i \geq 0, \\ 1, & \text{otherwise,} \end{cases} \]  (15)

without the need for path splitting. On the other hand, in case \( \min (L - 1, N_0) = N_0 \), all bits of the node need to be estimated and the decoding automatically reverts to the process described in [10]. The following proof is nevertheless valid for both \( L - 1 < N_0 \) and \( L - 1 \geq N_0 \).

Proof:

Let us consider the path metrics associated with the \( L \) surviving paths at bit estimation step \( i \) as \( \text{PM}_i = \{ \text{PM}_{i_0}, \ldots, \text{PM}_{i_{L-1}} \} \) and the LLR values associated with the Rate-1 node at path \( l \) as \( \alpha_l = \{ \alpha_{l_0}, \ldots, \alpha_{N_{N_0-1}} \} \). For the purpose of this proof, let us also consider the vectors \( \text{PM}_i \) and \( \alpha_l \) sorted as follows:
\[ \text{PM}_{i_0} \leq \text{PM}_{i_{i+1}}, \quad 0 \leq l < L - 1, \]
\[ |\alpha_{i_l}| \leq |\alpha_{l_{i+1}}|, \quad 0 \leq i < N_0 - 1. \]

At each estimation step \( i \), the corresponding bit is estimated as either 0 or 1, and the PMs are updated as
\[ \text{PM}_i = \sum_{j=0}^{i} \ln \left( 1 + e^{-\eta_i \alpha_{i_j}} \right), \]  (16)

which is a monotonic and non-decreasing function of \( i \). At any given estimation step \( i \) within the Rate-1 node, the least reliable LLR among those still to be estimated is \( \alpha_{i_i} \).

We now prove the theorem by contradiction. Let us suppose that step \( L - 1 \) splits path \( l \) into two surviving paths. The corresponding PMs will be
\[ \text{PM}_{L-1} = \sum_{j=0}^{L-2} \ln \left( 1 + e^{-\eta_{j} \alpha_{j}} \right) + \ln \left( 1 + e^{-|\alpha_{L-1}|} \right), \]  (17)
\[ \text{PM}_{L-1} = \sum_{j=0}^{L-2} \ln \left( 1 + e^{-\eta_{j} \alpha_{j}} \right) + \ln \left( 1 + e^{\alpha_{L-1}} \right), \]  (18)

where \( 0 \leq p < q < L \). We now show that there are at least \( L \) bit estimation sequences that result in PMs which are less than \( \text{PM}_{L-1} \). To this end, we demonstrate that there are \( L \) paths originated from path \( l \) with smaller PMs than \( \text{PM}_{L-1} \) that are generated before estimating bit \( L - 1 \).
Let us consider the lowest possible value that $\text{PM}_{L-1_q}$ can assume:

$$\text{PM}_{L-1_q} = \sum_{j=0}^{L-2} \ln \left(1 + e^{-|\alpha_{ji}|}\right) + \ln \left(1 + e^{\alpha_{L-1_i}}\right), \quad (19)$$

which represents the case where the bits estimated in steps $0 \leq j \leq L - 2$ match the hard decision of their corresponding LLR values, and the $L - 1$-th does not. Let us now consider the bit sequences differing from path $q$ in that the bit that does not match the LLR hard decision is at step $w$, where $0 \leq w \leq L - 2$, while the $L - 1$-th matches. The corresponding PM would be

$$\text{PM}_{L-1_w} = \sum_{j=0}^{L-2} \ln \left(1 + e^{-|\alpha_{ji}|}\right) + \ln \left(1 + e^{\alpha_{w_l}}\right) + \ln \left(1 + e^{\alpha_{L-1_i}}\right). \quad (20)$$

Rewriting Equation $(19)$ as

$$\text{PM}_{L-1_q} = \sum_{j=0}^{L-2} \ln \left(1 + e^{-|\alpha_{ji}|}\right) + \ln \left(1 + e^{\alpha_{w_l}}\right) + \ln \left(1 + e^{\alpha_{L-1_i}}\right), \quad (21)$$

and using the fact that $|\alpha_{L-1_i}| > |\alpha_{w_l}|$, we can use the result in Lemma 1 to conclude

$$\text{PM}_{L-1_q} > \text{PM}_{L-1_w}, \quad (22)$$

which in turn results in $q > v$. Since $w$ can assume $L - 1$ values, and taking in account the bit sequence represented by path $p$ where all the bits agree with their corresponding LLR hard decision, there are at least $L$ bit sequences which result in a smaller PM than $\text{PM}_{L-1_w}$. Therefore, $q \geq L$ which contradicts the assumption that $q < L$ and confirms that path $q$ will be discarded. In other words, this proves that paths that consider bits not matching the LLR hard decision after the $L - 1$-th step will always be discarded: it is thus useless to split paths after the $L - 1$-th. Theorem 1 is consequently proven.

The proposed theorem remains valid also for the HWF formulation that can be written as

$$\text{PM}_{i_q} = \begin{cases} 
\text{PM}_{i-1_q} + |\alpha_{i_q}|, & \text{if } \eta_i \neq \text{sgn}(\alpha_{i_q}), \\
\text{PM}_{i-1_i}, & \text{otherwise},
\end{cases} \quad (23)$$

At each step $i$, depending on the value of $|\alpha_{i_q}|$, two cases arise.

A $|\alpha_{i_q}| \geq |\text{PM}_{i-1_L_q} - \text{PM}_{i-1_i}|$

From $(23)$, we can see that the modulus of the least reliable bit $|\alpha_{i_q}|$ is the minimum quantity that can be added to the PM in case $\eta_i \neq \text{sgn}(\alpha_{i_q})$. If this quantity is greater than the difference between the currently considered path metric $\text{PM}_{i-1_q}$ and the largest surviving path metric $\text{PM}_{i-1_L_q}$, every estimation that sees $\eta_i \neq \text{sgn}(\alpha_{i_q})$ will lead to $\text{PM}_{i-1_L_q} + |\alpha_{i_q}| \geq \text{PM}_{i-1_L_{-1}}$, and thus to a discarded path. Consequently, for all the remaining estimations in the Rate-1 node, paths need not to be duplicated, and bits are estimated as $\eta_i = \text{sgn}(\alpha_{i_q})$.

B $|\alpha_{i_q}| < |\text{PM}_{i-1_L_q} - \text{PM}_{i-1_L_{-1}}|

Let us consider positions $p$ and $q$ in the ordering of PMs such that

$$\text{PM}_{i_p} = \text{PM}_{i-1_i}, \quad \text{PM}_{i_q} = \text{PM}_{i-1_i} + |\alpha_{i_q}|,$$

where $l \leq p < q < L$. In this case, both bit estimates for the least reliable bit have to be taken into account since their corresponding paths will be ordered among the first $L$. In turn, the path in position $L - 1$ at step $i - 1$ is moved to position $L$ at step $i$ and thus discarded. The following estimation step $i + 1$ must be evaluated independently, to see if it falls in case A or B.

As soon as case A is encountered in path $l$, that path does not need to undergo any subsequent splitting, and the remaining $\beta_{il}$ can be obtained through LLR hard decision of Equation $(15)$. While case B requires continued path splitting, this can occur a limited amount of times before case A is encountered. The maximum amount of consecutive case B occurrences can be identified by the following worst case analysis.

1) Case B occurs at $i = 0$ and $l = 0$.
2) Considering that $\text{PM}_{L-1_0}$ is the PM at $l = 0$ before the first bit of the Rate-1 node is estimated, if $p = 0$ and $q = 1$ then

$$\text{PM}_{0_0} = \text{PM}_{L-1_0}, \quad \text{PM}_{0_1} = \text{PM}_{L-1_0} + |\alpha_{0_0}|, \quad \text{PM}_{0_2} = \text{PM}_{L-1_1}, \quad \vdots$$

3) Case B occurs at $i = 1$ and $l = 0$.
4) Since $|\alpha_{0_0}| \leq |\alpha_{1_0}|, q > 1$. For $p = 0$ and $q = 2$,

$$\text{PM}_{1_0} = \text{PM}_{L-1_0}, \quad \text{PM}_{1_1} = \text{PM}_{L-1_0} + |\alpha_{0_0}|, \quad \text{PM}_{1_2} = \text{PM}_{L-1_0} + |\alpha_{1_0}|, \quad \vdots$$

5) Since at every step $|\alpha_{i-1_q}| \leq |\alpha_{i_q}|$, then $q > i$. If at every case B step $p = 0$ and $q = i + 1$, a total of $L - 1$ consecutive case B are possible, after which $q > L - 1$, resulting in case A. At $i = L - 2$, the $L$ surviving PMs after $L - 1$ consecutive case B are the following:

$$\text{PM}_{L-2_0} = \text{PM}_{L-1_0}, \quad \text{PM}_{L-2_1} = \text{PM}_{L-1_0} + |\alpha_{0_0}|, \quad \text{PM}_{L-2_2} = \text{PM}_{L-1_0} + |\alpha_{1_0}|, \quad \vdots$$

$$\text{PM}_{L-2_{L-2}} = \text{PM}_{L-1_0} + |\alpha_{L-2_0}|.$$


Much like the case considered in the proof for Theorem 1, the above analysis shows that at most $L - 1$ bit estimations are required to guarantee the exact same results as the conventional SCL. Thus, the theorem is valid also with the HWF Equation (23).

In the presented proof and discussion, $\alpha_i$ and $PM_i$ are assumed to be sorted at every step for the sake of simplicity. PMs are sorted every time paths are split, i.e. when an information bit is estimated. When the decoding process considers frozen bits, paths are not split and even if modified, PMs retain their ordering. On the other hand, $\alpha_i$ is not ordered, but at each step $i$ the full vector sorting can be substituted with the identification of the minimum $|\alpha_i|$.

The result of Theorem 1 provides an exact number of bit-estimations in Rate-1 nodes for each list size in SCL decoding in order to guarantee error-correction performance preservation. The Rate-1 node decoder of [7] states that two bit-estimations are required to preserve the error-correction performance, but this result is found empirically. The following remarks are the direct results of Theorem 1.

**Remark 1.** The Rate-1 node decoder of [7] for $L = 2$ is redundant.

Theorem 1 states that for a Rate-1 node of length $N_v$ when $L = 2$, the number of bit-estimations is $\min(L - 1, N_v) = 1$. Therefore, there is no need to estimate the bits after the least reliable bit is estimated. [7] for $L = 2$ is thus redundant.

**Remark 2.** The Rate-1 node decoder of [7] falls short in preserving the error-correction performance for higher rates and larger list sizes.

For codes of higher rates, the number of Rate-1 nodes of larger length increases [11]. Therefore, when the list size is also large, $\min(L - 1, N_v) \gg 2$. The gap between the empirical method of [7] and the result of Theorem 1 can introduce significant error-correction performance loss. Fig. 3 provides the frame error rate (FER) and bit error rate (BER) curves obtained with Fast-SSCL decoding ($L = 128$) for a $P(1024, 860)$ code. The code is concatenated with a cyclic redundancy check of length 32, and different curves are provided for the Rate-1 node decoder in Theorem 1 and the empirical method of [7]. It can be seen that the error-correction performance loss reaches 0.25dB at FER of $10^{-5}$.

The proposed Rate-1 node decoder is used in the Fast-SSCL algorithm, while the decoders for Rate-0 and Rep nodes remain similar to those used in SSCL [10]. In the following section, we show that in a polar code, there are many instances where $L - 1 < N_v$ for Rate-1 nodes and using the Fast-SSCL algorithm can significantly reduce the number of required decoding time-steps with respect to both SCL and SSCL.

**IV. TIME-STEP REDUCTION**

In Section III, we have demonstrated that when $L - 1 < N_v$, up to $L - 1$ bit estimations are necessary when decoding Rate-1 nodes to match the performance of SCL and SSCL. The time-step reduction for the complete polar code decoding that can be gained through this technique, however, depends on the structure of the code itself. As an example, Table I shows the number of time-steps required to decode a polar code of length $N = 1024$ optimized for $E_b/N_0 = 2$ dB: results are given for three different rates, five list sizes, and SCL, SSCL and Fast-SSCL decoding algorithms.

**TABLE I**

| Rate | $L$ | SCL | SSCL | Fast-SSCL |
|------|----|-----|------|-----------|
| 1/2  | 2  | 2302| 533  | 394       |
|      | 4  | 2302| 533  | 474       |
| 1/4  | 8  | 2302| 533  | 451       |
|      | 16 | 2302| 533  | 532       |
|      | 32 | 2302| 533  | 533       |

**Fig. 3.** FER and BER performance comparison of decoding $P(1024, 860)$ with Fast-SSCL and the empirical method of [7] when $L = 128$. The cyclic redundancy check length is 32.
The number of decoding time-steps for the Fast-SSCL algorithm, on the other hand, depends on $L$: a small list size will result in a fast decoding process, that will however yield lower error-correction performance with respect to a larger list size, but will not degrade it with respect to SCL and SSCL with the same $L$. The larger advantages can be observed for high rates, where Rate-1 nodes are more numerous and are larger: with $L = 2$ and rate $3/4$, Fast-SSCL requires 66.6% and 88.1% fewer time-steps than SSCL and SCL respectively, without causing any deterioration in error-correction performance.

V. Conclusion

In this work, we have proposed a faster approach to the decoding of Rate-1 nodes in polar codes which resulted in the development of Fast-SSCL decoding algorithm. We have postulated and demonstrated that the number of bit estimations and consequent path splitting of a Rate-1 node of length $N_ν$ necessary to exactly match the error-correction performance of SCL or SSCL decoding with list size $L$ is $\min(L - 1, N_ν)$. Considering a set of codes as a case study, we have shown that the whole polar code decoding process can benefit in time-step reduction of up to 88.1% with respect to SCL, and 66.6% with respect to SSCL decoding algorithm without any kind of error-correction performance degradation.

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