External reset system prediction time of LAPAN satellite using IC 4536 programmable timer circuit

A R Sastaviyana* and A B Erwindu

Satellite Technology Center, LAPAN, Indonesia
*adelia.revani@gmail.com

Abstract. For ensuring missions continuity in every satellite, all satellite systems are required to be active non-stop. But, for important maintenance reason, satellite system also needs reset condition when all satellite systems, except TTC unit, can be refreshed for a while every determined time. IC 4536 programmable timer circuit has main function to count every about 14 days then give signal reset for about 200 milliseconds. High level output voltage duration time can be adjusted by determining the values of capacitor and decode out, while low level output voltage duration time can be adjusted by determining resistor value. External reset system prediction time calculation shows that using capacitor C2 value 300 nF and decode out value 24 can achieve 14 day 18 hour 39 minute 31 second 172 millisecond high level output voltage duration time. Observation result shows that using resistor R3 value 2 kΩ can give 230 millisecond reset signal time. High level output voltage duration time target test shows that using capacitor C2 value 300 nF and decode out value 20 can give counting time up to 21 hours 41 minutes 59 seconds 792 milliseconds.

1. Introduction
LAPAN Satellite Technology Center has developed and orbited 3 generations of micro-satellites, that are LAPAN-A1/TUBSAT, LAPAN-A2/ORARI, and LAPAN-A3/IPB which have their respective main missions. For supporting these missions continuity, payload and bus systems in these satellites must be active at all time. But, sometimes hardware or software errors could happen in satellite systems and can cause hardware or software systems work incorrectly [1]. Moreover, some errors that are caused by environmental effects must also be considered [1]. A method that can be used for tolerating those errors, faults, or any failures during operation process is to design a special circuitry which can reset the satellite systems [1][2], except Tracking, Telemetry, and Command (TTC) unit [3][4][5], automatically and regularly in every determined time. Timer circuit has a main role to count, while giving high level output voltage, then give reset signal (low level output voltage) to satellite systems after every determined time continuously [6][7][8]. External reset system that has been developed in these 3 satellites used IC CD 4060, SN 74292, and MAX 703 [9]. This system can give 14.76 day high level output voltage duration time and 19.45 second low level output voltage duration time [9]. IC 4536 is a programmable timer IC that can be used in designing an external reset system. Designing an external reset system using IC 4536 programmable timer circuit is expected to offer alternative more simple system but still be able to meet high and low level output voltage duration time target in the next A generations of LAPAN micro-satellites, LAPAN-A4 and LAPAN-A5, that are now being developed. LAPAN satellites are designed to have reset condition every 2 weeks, so
timer circuit high level output voltage duration time target is about 14 days [10], while reset time required by satellite system is about 200 milliseconds.

2. Methodology
Methods used in this paper to achieve IC 4536 programmable timer circuit design that can predict external reset system time every about 14 days and give required reset signal duration time are described as flowchart in figure 1.

![Methodology flowchart.](image)

2.1. Literature review of IC 4536 programmable timer circuit
IC 4536 is a programmable timer consisting of 24 ripple-binary counter stages. IC 4536 can count from $2^0$ until $2^n$, where $1 \leq n \leq 24$ and can be determined by setting the high or low input voltage to 8-BYPASS, D, C, B, and A pins [11]. Decode out (n) value follows the truth table explained in table 1. IC 4536 functional diagram is shown in figure 2. The more decode out value, the longer timer circuit can count [11].
Table 1. Truth table determining decode out value (0 = low level, 1 = high level).

| D | C | B | A | Decode Out Value |
|---|---|---|---|------------------|
|   |   |   | 0 | 8-BYPASS = 0     |
| 0 | 0 | 0 | 0 | 9                |
| 0 | 0 | 0 | 1 | 10               |
| 0 | 0 | 1 | 0 | 11               |
| 0 | 1 | 0 | 0 | 13               |
| 0 | 1 | 0 | 1 | 14               |
| 0 | 1 | 1 | 0 | 15               |
| 0 | 1 | 1 | 1 | 16               |
| 1 | 0 | 0 | 0 | 17               |
| 1 | 0 | 0 | 1 | 18               |
| 1 | 0 | 1 | 0 | 19               |
| 1 | 1 | 0 | 0 | 21               |
| 1 | 1 | 0 | 1 | 22               |
| 1 | 1 | 1 | 0 | 23               |
| 1 | 1 | 1 | 1 | 24               |
|   |   |   | 1 | 8-BYPASS = 1     |

Figure 2. IC 4536 functional diagram.

Duration of timer circuit using IC 4536 to give high level output voltage can be adjusted by changing decode out value [12] and capacitor value that is connected to OUT1 pin, while changing low level output voltage can be done by changing resistor value that is connected to DECODE OUT pin.

2.2. IC 4536 programmable timer circuit hardware design

Timer circuit high-level output voltage duration time target is about 14 days, while reset time target is about 200 milliseconds. Capacitor C2 and decode out values can be adjusted to reach timer circuit high level output voltage duration time target while to reach required reset time can be done by adjusting the value of resistor R3. IC 4536 programmable timer circuit hardware design is shown in figure 3.
2.3. Observation of capacitor C2 value changes correlation to high level output voltage duration time
Before determining fixed value of capacitor C2 to reach high level output voltage duration time target for 14 days, correlation of capacitor C2 value changes to high level output voltage duration time must be observed first. Observation was performed by using varying capacitor values and decode out value was fixed at 9. Table 2 explains correlation of capacitor C2 value changes to high level output voltage duration time.

**Table 2. Correlation of capacitor C2 value changes to high-level output voltage duration time.**

| C2 Capacitance Value in nF | High Level Output Voltage Duration Time | Total High Level Output Voltage Duration Time in Milliseconds (a) | Ratio of C2 Capacitance Value to Value in Row Above (b) | Ratio of a Value to Value in Row Above (c) | \(|b - c|\) |
|---------------------------|----------------------------------------|-------------------------------------------------|---------------------------------|---------------------------------|-------|
| 10                        | 1                                      | 243 | 1243 | - | - | - |
| 15                        | 1                                      | 939 | 1939 | 1.500 | 1.560 | 0.060 |
| 22                        | 2                                      | 731 | 2731 | 1.467 | 1.408 | 0.058 |
| 33                        | 4                                      | 68 | 4068 | 1.500 | 1.490 | 0.010 |
| 39                        | 4                                      | 814 | 4814 | 1.182 | 1.183 | 0.002 |
| 47                        | 5                                      | 772 | 5772 | 1.205 | 1.199 | 0.006 |
| 56                        | 6                                      | 814 | 6814 | 1.191 | 1.181 | 0.011 |
| 82                        | 10                                     | 244 | 10244 | 1.464 | 1.503 | 0.039 |
| 100                       | 12                                     | 563 | 12563 | 1.220 | 1.226 | 0.007 |
| 220                       | 27                                     | 808 | 27808 | 2.200 | 2.213 | 0.013 |
| 300                       | 38                                     | 651 | 38651 | 1.364 | 1.390 | 0.026 |
| 470                       | 58                                     | 159 | 58159 | 1.567 | 1.505 | 0.062 |
| Mean                      |                                        |      | Mean |      |      | 0.027 |

Based on observation result in Table 2, it can be concluded that correlation of capacitor C2 value changes to high level output voltage duration time follows this equation:

\[
\frac{C_1}{C_2} \approx \frac{High\ Level\ Output\ Voltage\ Duration\ Time_1}{High\ Level\ Output\ Voltage\ Duration\ Time_2}
\]  

(1)

2.4. Observation of decode out value changes correlation to high level output voltage duration time
Observation of decode out value changes correlation to high level output voltage duration time has to be performed because changes in decode out value can change high-level output voltage duration time too. This observation used varying decode out values from 9 to 20, while capacitor C2 value was fixed
to 9 nF. Correlation of decode out value changes to high level output voltage duration time is explained in table 3. Based on observation result in table 3, it can be concluded that when decode out value is increased by one, then high level output voltage duration time will be multiplied by about 2.001 times.

**Table 3.** Correlation of decode out value changes to high level output voltage duration time.

| Voltage Level in Pin | Decode Out Value | High Level Output Voltage Duration Time | Total High Level Output Voltage Duration Time in Milliseconds (a) | Ratio of \( a \) Value to Value in Row Above |
|----------------------|------------------|-----------------------------------------|----------------------------------------------------------------|---------------------------------------------|
| 8-BYPASS             | D C B A          | Minutes  | Seconds | Milliseconds |                                |                                                |
| 0                    | 0 0 0 0 0        | 9        | 0       | 1           | 243                            | 1243                                           |
| 0                    | 0 0 0 0 0        | 10       | 0       | 2           | 509                            | 2509                                           |
| 0                    | 0 0 0 0 0        | 11       | 0       | 4           | 998                            | 4998                                           |
| 0                    | 0 0 0 0 0        | 12       | 0       | 9           | 994                            | 9994                                           |
| 0                    | 0 0 1 0 0        | 13       | 0       | 20          | 177                            | 20177                                          |
| 0                    | 0 0 1 0 0        | 14       | 0       | 40          | 380                            | 40380                                          |
| 0                    | 0 1 1 0 0        | 15       | 1       | 20          | 327                            | 80327                                          |
| 0                    | 0 1 1 1 1        | 16       | 2       | 40          | 74                             | 160074                                         |
| 0                    | 1 0 0 0 0        | 17       | 5       | 19          | 0                              | 319000                                         |
| 0                    | 1 0 0 0 0        | 18       | 10      | 41          | 63                             | 641063                                         |
| 0                    | 1 0 1 0 0        | 19       | 21      | 18          | 886                            | 1278886                                        |
| 0                    | 1 0 1 1 1        | 20       | 42      | 40          | 415                            | 2560415                                        |
| Mean                 |                 |          |         |             |                                | 2.002                                          |

2.5. Observation of resistor R3 value changes correlation to low level output voltage duration time

To reach required reset signal duration time, resistor R3 value changes correlation to low level output voltage duration time must be observed by using varying resistor R3 values and decode out value fixed at 9. Table 4 shows correlation of resistor R3 value changes to low level output voltage duration time.

**Table 4.** Correlation of R3 resistor’s value changes to low level output voltage duration time.

| R3 Resistance Value in kΩ | Low Level Output Voltage Duration Time in Milliseconds (a) | Ratio of R3 Resistance Value to Value in Row Above (b) | Ratio of \( a \) Value to Value in Row Above (c) | \(|b - c| \) |
|---------------------------|----------------------------------------------------------|------------------------------------------------------|---------------------------------------------|---------|
| 2                         | 231                                                      | -                                                    | -                                           | 0.165   |
| 3.3                       | 343                                                      | 1.650                                                | 1.485                                       | 0.143   |
| 5.1                       | 481                                                      | 1.545                                                | 1.402                                       | 0.127   |
| 8                         | 683                                                      | 1.569                                                | 1.420                                       | 0.149   |
| 10                        | 767                                                      | 1.250                                                | 1.123                                       | 0.127   |
| 12                        | 865                                                      | 1.200                                                | 1.128                                       | 0.072   |
| 15                        | 988                                                      | 1.250                                                | 1.142                                       | 0.108   |
| 18                        | 1080                                                     | 1.200                                                | 1.093                                       | 0.107   |
| 22                        | 1230                                                     | 1.222                                                | 1.139                                       | 0.083   |
| Mean                      |                                                          |                                                      |                                             | 0.113   |

Based on observation result in table 4, resistor R3 value changes correlation to low level output voltage duration time can be concluded as equation below:

\[
\frac{R_1}{R_2} \approx \frac{Low \ Level \ Output \ Voltage \ Duration \ Time_1}{Low \ Level \ Output \ Voltage \ Duration \ Time_2}
\]

(2)

Observation result also shows that using resistor R3 value 2 kΩ, low-level voltage output duration time target is already achieved.
2.6. Observation of decode out value changes correlation to low level output voltage duration time

Observation of decode out value changes correlation to low level output voltage duration time was performed by using resistor R3 value 2 kΩ and decode out values 9–13, the result is shown in table 5.

Table 5. Observation result of decode out value changes correlation to low level output voltage duration time.

| Voltage Level in Pin | Decode Out Value | Low Level Output Voltage Duration Time in Milliseconds |
|----------------------|-----------------|-----------------------------------------------------|
| 8-BYPASS D C B A     |                 |                                                     |
| 0 0 0 0 0 0          | 9               | 231                                                 |
| 0 0 0 0 0 1          | 10              | 234                                                 |
| 0 0 0 1 0 0          | 11              | 234                                                 |
| 0 0 1 1 0 0          | 12              | 236                                                 |
| 0 1 0 0 0 0          | 13              | 230                                                 |

According to observation result in table 5, it can be concluded that decode out value changes does not affect significantly to low level output voltage duration time. It can be an advantage when calculating required decode out and capacitor C2 values to reach high level output voltage duration time target.

2.7. Calculation of estimated decode out and capacitor C2 value for reaching high level output voltage duration time target

As described above, high level output voltage duration time target is about 14 days which is equivalent to 1,209,600,000 milliseconds. If this time target is reached using decode out value 24, then time target that has to be reached using decode out value 9 can be calculated as follows:

\[
Time Target using Decode Out Value 9 = \frac{1,209,600,000}{200} \text{ ms} = 36,175.64 \text{ ms}
\]  

(3)

Then, considering equation (1) and high level output voltage duration time when capacitor C2 value is 10 nF (see table 2), capacitor C2 value target can be calculated as follows:

\[
Capacitor C2 Value Target \approx \frac{36,175.64 \text{ ms}}{1,243 \text{ ms}} \times 10 \text{ nF} \approx 294.590 \text{ nF}
\]  

(4)

Based on calculation in equation (4), capacitor C2 value that is used is 300 nF. According to high level output voltage duration time when capacitor C2 value is 300 nF and decode out value is 9 information in table 2, estimated high level output voltage duration time when capacitor C2 value is 300 nF and decode out value is 10–24 can be predicted as in table 6.

Table 6. Estimated high level output voltage duration time when capacitor C2 value is 300 nF and decode out value is 10–24.

| Voltage Level in Pin | Decode Out Value | Estimated High Level Output Voltage Duration Time |
|----------------------|-----------------|--------------------------------------------------|
| 8-BYPASS D C B A     |                 |                                                 |
| 0 0 0 0 0            | 10              | Days Hours Minutes Seconds Milliseconds         |
| 0 0 0 1 0            | 11              | 0 0 2 34 770                                  |
| 0 0 1 1 0            | 12              | 0 0 5 9 707                                  |
| 0 1 0 0 0            | 13              | 0 0 10 19 747                                 |
| 0 1 0 1 0            | 14              | 0 0 20 40 161                                 |
| 0 1 1 0 0            | 15              | 0 0 41 21 656                                 |
| 0 1 1 1 0            | 16              | 0 1 22 45 982                                 |
| 1 0 0 0 0            | 17              | 0 2 45 37 305                                 |
| 1 0 0 1 0            | 18              | 0 5 31 25 299                                 |
| 1 0 1 0 0            | 19              | 0 11 3 11 986                                 |
| 1 0 1 1 0            | 20              | 0 22 7 6 772                                  |
| 1 1 0 0 0            | 21              | 1 20 15 39 188                                |
2.8. High level output voltage duration time target test

Before reaching high-level output voltage duration time target for 14 days, test was performed to reach high-level output voltage duration time target for about 1 hour, 6 hours, 12 hours, and 24 hours. According to estimated high level output voltage duration in table 6, decode out values used to perform test are 15, 18, 19, and 20. Table 7 describes high-level output voltage duration time target test result when capacitor C2 value is 300 nF and decode out values are 15, 18, 19, and 20.

**Table 7. High level output voltage duration time target test result.**

| Decode Out Value | Estimated High Level Output Voltage Duration Time | High Level Output Voltage Duration Time Target Test Result | Time Difference |
|------------------|-----------------------------------------------|----------------------------------------------------------|-----------------|
|                  | Hours Minutes Seconds Milliseconds             | Hours Minutes Seconds Milliseconds                        | Minutes Seconds Milliseconds |
| 15               | 0 41 21 656                                   | 0 40 43 507                                               | 0 38 149         |
| 18               | 5 31 25 299                                   | 5 23 38 678                                               | 7 46 621         |
| 19               | 11 3 11 986                                  | 10 48 21 467                                              | 14 50 519        |
| 20               | 22 7 6 772                                   | 21 41 59 792                                              | 25 6 980         |

3. Conclusion

IC 4536 programmable timer circuit high level output voltage duration time target is about 14 days, while the low-level output voltage duration time target is about 200 milliseconds. Observation result shows that using resistor R3 value 2 kΩ can achieve low-level output voltage duration time 230 milliseconds. External reset system prediction time based on calculation result shows that using capacitor C2 value 300 nF and decode out value 24 can achieve high level output voltage duration time 14 days 18 hours 39 minutes 31 seconds 172 milliseconds. High level output voltage duration time target test using capacitor C2 value 300 nF and decode out value 20 can reach 21 hours 41 minutes 59 seconds 792 milliseconds. This result is 25 minutes 6 seconds 980 milliseconds less than estimated high level output voltage duration time. A longer high-level output voltage duration time target test should be performed to ensure that IC 4536 programmable timer circuit could reach 14 day high level output voltage duration time target.

Acknowledgments

Authors sincerely appreciate Wahyudi Hasbi and Rommy Hartono for their supervision and encouragement in IC 4536 programmable timer circuit research and development in LAPAN and thank LAPAN Satellite Technology Center for supporting in funding and providing this research and development facility.

References

[1] Apgar H et al 2005 Space Mission Analysis and Design Third Edition ed W J Larson and J R Wertz (California: Microcosm Press and Dordrecht: Kluwer Academic Publishers) chapter 11 pp 401-403 chapter 16 pp 659-660

[2] Agasid E et al 2015 *Small Spacecraft Technology State of the Art* ed R Shimmin (California: NASA) chapter 8 pp 95-96

[3] Triharjanto R H, Mukhayadi M and Hasbi W 2007 LAPAN-TUBSAT system budget *LAPAN-TUBSAT: from Concept to Early Operation* ed S Hardhienata and R H Triharjanto (Bogor: LAPAN) pp 18-20

[4] Mukhayadi M 2007 LAPAN-TUBSAT attitude determination and control system *LAPAN-TUBSAT: from Concept to Early Operation* ed S Hardhienata and R H Triharjanto (Bogor: LAPAN) pp 24-26
[5] Saifudin M A and Karim A 2013 Analisis manajemen power satelit LAPAN-ORARI/A2 Pengembangan Teknologi Satelit di Indonesia: Sistem, Subsistem, dan Misi Operasi ed A Rahman and R H Triharjanto (Bogor: PT Penerbit IPB Press) pp 11-20
[6] Siebert W M 1986 Circuits, Signals, and Systems (Cambridge: The MIT Press) chapter 1 pp 39-40
[7] Elektuur 1985 Kumpulan Data Penting Komponen Elektronika translated by Wasito S (Jakarta: PT Multimedia, Gramedia Grup) pp 54-56
[8] Malvino A P 1987 Prinsip-Prinsip Elektronika Edisi Ketiga vol 2 translated by M Barmawi and M O Tjia (Jakarta: Erlangga) chapter 20 pp 246-254
[9] Karim A 2010 Perancangan Sistem Reset Eksternal Satelit Mikro Satelit Mikro untuk Mitigasi Bencana dan Ketahanan Pangan ed A P Sunaryati and S Tanoemihardja (Bogor: PT Penerbit IPB Press)
[10] Widipaminto A 2007 LAPAN-TUBSAT power control and data handling LAPAN-TUBSAT: from Concept to Early Operation ed S Hardhienata and R H Triharjanto (Bogor: LAPAN) pp 32-35
[11] Anonymous 2017 Datasheet CD4536B Types CMOS Programmable Timer (Texas: Texas Instruments)
[12] Velleman NV 2004 K6200 0 to 60 Hour Start / Stop Timer (Gavere: Velleman NV)