Measurement of Variations in FPGAs under Various Load Conditions

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Abstract: This paper presents experimental evaluations of operating speed, power consumption, and chip temperature under various load conditions on commercial FPGAs. To measure the operating speed of FPGAs, we count the oscillation frequency of a ring oscillator (RO), which is implemented on one 4-input look-up table (LUT). The load condition on FPGAs can be controlled by the number of activated ROs in parallel around the measurement RO. The measurement results show that operating speed may be decreased more than 10% with 142 ROs as load circuits and the degradation rates depend on the measurement location in an FPGA. The evaluation of die-to-die variations using four more FPGA boards show that there exists a non-negligible speed variation.

Keywords: FPGA, load condition, variation, ring oscillator

1. Introduction

With the advancement in transistor performance and integration scale, reliability issues, such as within-die and die-to-die process variation, soft errors, and Negative Bias Temperature Instability (NBTI), are considered as serious problems [1]. Reliability issues in FPGAs are also discussed in Refs. [2], [3], [4]. For measurement of delays and temperature distribution on FPGAs, Built-In Self-Test (BIST) method and on-chip thermal monitoring method are proposed in Refs. [5] and [6], respectively. The performance degradation caused by heavy load conditions and voltage fluctuation is also well known as inevitable problems. When an application is implemented on FPGAs, the circuit structure and load distribution depend on its mapping results. However, performance variations under various load distribution on FPGAs are not reported.

This paper presents the measurement of operating speed, power consumption, and chip temperature under various load conditions on FPGAs. This paper is organized as follows. Section 2 explains the measurement circuit and its FPGA implementation. Section 3 describes the measurement methods followed by the experimental results in Section 4. Concluding remarks are given in Section 5.

2. Measurement Circuit on FPGAs

To measure the operating speed on FPGAs, we count the oscillation frequency of an RO. As shown in Fig. 1, the measurement circuit consists of a 1-stage RO and an asynchronous counter by 32 flip-flops (FFs). As the enable signal of RO is asserted for one second, the value of an oscillation frequency is stored in the counter.

Fig. 1 Measurement circuit with 1-stage RO and 32-bit counter.

The target FPGA is Altera Cyclone IV EP4CE115F29C7 on Terasic DE2-115 board. Cyclone IV devices [7] mainly consist of Logic Array Blocks (LABs), embedded multipliers, and embedded memory blocks. LABs contain 16 Logic Elements (LEs), which are the smallest unit of logic in Cyclone IV device architecture and are composed of a 4-input LUT and a flip-flop (FF).

The oscillation frequency of an RO implemented on an FPGA depends on its fitting results. However, in our experiments, it should be stable regardless of fitting results. First, we employ 1-stage RO, which can be implemented on a single LE and can remove the effects of routing delay variations. Second, we select the oscillation path on a LE in order to achieve the highest oscillation frequency, because path delays depend on its transition paths. As shown in Fig. 2, we can implement four types of ROs using one LE. The measurement results of oscillation frequencies are shown in Fig. 2 (b). The RO with data_2 type oscillation path achieves the highest oscillation frequency and is adopted as the
RO for our measurement circuit. On the other hand, the ROs with data_3 type or data_4 type oscillation path does not oscillate.

3. Measurement Method

In order to evaluate the impact of load conditions on an FPGA, we implemented load circuits around the measurement circuit, as illustrated in Fig. 3. Load conditions around the measurement circuit can be controlled by changing the number of load circuits, which are ROs mapped around the measurement circuit and operating concurrently with the measurement circuit. The 32-bit counter of measurement circuit is located away from the measurement RO so as to avoid the effect on load conditions around the measurement RO. Because the oscillation frequency of measurement RO is very high, only the 1st FF of the 32-bit counter is mapped on the LAB, in which the measurement RO is mapped. The 2nd-32th FFs are mapped on separated LABs. In order to remove the effect caused by a biased load condition, 2nd-32th FFs are mapped on 16 LABs, as shown in Fig. 3.

To evaluate the impact of chip temperature on oscillation frequencies, oscillation frequencies were measured at two levels of temperatures: a stable temperature and a normal temperature. Let the chip temperature rise without removing the heat of an FPGA, and we can obtain a stable chip temperature. Our preliminary experiments found that 30 sec. operation is enough to obtain stable chip temperatures. On the other hand, the normal chip temperature, which is 30°C, can be kept by using a cooling heatsink and a fan. We measured chip temperatures using a contact type digital thermometer and a non-contact digital Infrared thermometer.

As for the measurement of power consumption of FPGA boards, we use a digital wattmeter in our experiments. Within-die variations of FPGA are reported in some papers [2], [4]. In this paper, we measure oscillation frequencies on five locations in an FPGA, as shown in Fig. 4.

Die-to-Die performance variation is one of the most important problems for LSI fabrications in the nanometer era. We, therefore, evaluate die-to-die variations using four more FPGA boards which have the same FPGA device, Cyclone IV.

4. Measurement Results

In this section, we demonstrate the measurement results and evaluate the operating speed variations considering the impacts of load condition, chip temperature, within-die variation, and die-to-die variation. In each experiment, we obtained the results based on an average value of five measurements.

4.1 Within-die Operating Speed Variations

Figure 5(a) and Fig. 5(b) show oscillation frequencies and its degradation rates at stable chip temperature under various load conditions on five locations in an FPGA. We can find that oscillation frequencies vary depending on the measurement locations in an FPGA. Within-die variations are 0.08 GHz (3.3%) without any load circuits and 0.17 GHz (7.6%) with 142 load circuits. Therefore, within-die variation increased twice depending on load conditions in this experiment. Figure 5(c) and Fig. 5(d) shows power consumptions and chip temperatures under various load conditions on five locations. Both are getting higher depending on the increasing number of load circuits and vary depending on the measurement locations in an FPGA.

In order to remove the dependency on chip temperatures, we evaluate the impacts of load conditions and within-die variations on operating speed at normal chip temperature of 30°C. Figure 6(a) and Fig. 6(b) show oscillation frequencies and power consumptions at normal chip temperature under various load conditions on five measurement locations in an FPGA. Power consumptions are similar to those at stable chip temperature. On the other hand, the degradation rate and within-die variation of oscillation frequencies are lower and smaller than those at stable chip temperatures, respectively.
4.2 Die-to-die Operating Speed Variations

To evaluate die-to-die operating speed variation, we performed the same experiment as described in Section 4.1 with the use of four more FPGA boards which have the same FPGA device.

Table 1 shows the measurement results on location 1–5 of five FPGAs at stable chip temperatures and normal chip temperatures. According to the increase of the number of load circuits, at stable chip temperatures, the operating speed variations are also increasing except for location 5. As for locations 1–4, the operating speed variations range from 4.8% on location 1 without any load circuits to 11.9% on location 3 with 142 load circuits.

In contrast to the results at stable chip temperatures, die-to-die operating speed variations at the normal chip temperature do not depend on load conditions. The die-to-die operating speed variations range from 5.1% on location 1 to 10.2% on location 5.

5. Conclusion

In this paper, we measured and evaluated the operating speed, power consumption, and chip temperature under various load conditions on commercial FPGAs. The quantitative evaluation results indicate that the trends of operating speed degradations are similar between FPGAs. Non-negligible variations of operating speed and power consumption under various operating conditions exist and depend on within-die/die-to-die variations.

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