The Fractional-N All Digital Frequency Locked Loop with Robustness for PVT Variation and Its Application for the Microcontroller Unit

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SUMMARY This paper describes the Fractional-N All Digital Frequency Locked Loop (ADFLL) with Robustness for PVT variation and its application for the microcontroller unit. The conventional FLL is difficult to achieve the required specification by using the fine CMOS process. Especially, the conventional FLL has some problems such as unexpected operation and long lock time that are caused by PVT variation. To overcome these problems, we propose a new ADFLL which uses dynamic selecting digital filter coefficients. The proposed ADFLL was evaluated through the HSPICE simulation and fabricating chips using a 0.13 μm CMOS process. From these results, we observed the proposed ADFLL has robustness for PVT variation by using dynamic selecting digital filter coefficient, and the lock time is improved up to 57%, clock jitter is 0.85 nsec.

key words: all digital frequency locked loop, fractional-N, PVT variation, microcontroller unit

1. Introduction

The microcontroller unit (MCU) is one of the most important units for various equipment such as internet of thing (IoT), medical equipment, car and so on. The MCU has the many functions, such as processor, timer, analog-to -digital converter, and so on, that need the clock to operate itself. On the other hands, many researchers are interested in network system, neural network and integrated circuits using multiple valued logic [1]–[4]. The multiple valued logic is one of the effective methods for large capacity communication, high speed operation and small chip area. Generally, phase locked loop (PLL) is often used for generating any clocks to operate for the many applications. The PLL needs large chip area and more power because the PLL is two pole system and complex. In the recent year, many researchers are interested in all digital frequency locked loop (ADFLL) [5]–[10]. The ADFLL is constructed with digital circuit, and it is expected to achieve small chip area and low power consumption because it is one pole and simple system. However, conventional PLL can’t achieve the required specification by scaling down of CMOS process. In the scaling down of CMOS process, parameters of the MOS transistors are drastically changed such as threshold voltage \( V_{th} \), transconductance \( g_m \), drain conductance \( g_d \) and so on. These parameters are important parameters to design the output frequency of ADFLL. In addition, the lock time of ADFLL is also sensitive to these parameters. In many cases, the trimming is often used for insensitivity the PVT variation, however it needs more cost and is not effective for the improve the lock time. To overcome these problems, we proposed the novel Fractional-N ADFLL with robustness for the PVT variation which is not necessary the trimming [11]. However, it considered only process variation from HSPICE simulation, and it was not indicated the experimental result of fabricated chip. In this study, we indicate the robustness for the Temperatures and the Voltages and the experimental result of fabricated chips.

In this paper, the Fractional-N all digital frequency locked loop with robustness for PVT variation and its application for the microcontroller unit is described. The proposed ADFLL adds the only one functional block that selects the value of digital filter coefficient. Therefore, the value of digital filter coefficient can be selected according as the PVT variation. The proposed ADFLL is evaluated through the HSPICE simulation and actual chips using 0.13 μm CMOS process. Simulation and experimental results are shown in this paper.

2. Architecture of the Proposed ADFLL

Figure 1 shows architecture of the proposed ADFLL. The proposed ADFLL is constructed with frequency divider, frequency detector, adder, digital filter, filter select, and DCO. All of these blocks are constructed with digital circuits. Next, we explain about operation of each circuit blocks. The detail of DCO is explained in next section.

2.1 Frequency Divider

The frequency divider is constructed with delay flip flop (D-
FF), it outputs half the input frequency. And output pulse is kept 50% duty.

2.2 Frequency Detector

The frequency detector compare the reference clock ($f_{ref}$) and feedback clock ($f_{fb}$). This circuit counts the number of $f_{fb}$ pulse when $f_{ref}$ is high. Therefore, the relationship between $f_{fb}$ and $f_{ref}$ is given by Eq. (1). Where $N_{count}$ is the number of pulse which is the output of this circuit (Eq. (2)). When the output frequency is locked to the design value, $N_{count}$ equals $N_{multi}$.

$$f_{fb} = 2 \cdot N_{count} \cdot f_{ref}$$  (1)
$$N_{count} = \frac{1}{2} \cdot \frac{f_{fb}}{f_{ref}}$$  (2)

2.3 Adder

The adder outputs difference between the $N_{multi}$ and $N_{count}$ which is given by Eq. (3). When the output frequency is locked to design value, $N_{count} = N_{multi}$, the output of this circuit equal 0.

$$F_{delta} = N_{multi} - N_{count}$$  (3)

2.4 Digital filter with Filter Select

The digital filter outputs summation between the $F_{delta}$ and $Z_{n-1}$ which given by Eq. (4).

$$Z_{n} = A_{fil} \cdot (F_{delta} + Z_{n-1})$$  (4)

Where $Z_{n}$, $Z_{n-1}$ and $A_{fil}$ mean the output of digital filter, the output of digital filter which is before one clock, and the coefficient of digital filter, respectively. $A_{fil}$ can change the gain of digital filter, however conventional ADFLL are almost using fixed value. If the parameter of MOS transistors are changed by PVT variation, the gain is not optimal value. For this reason the output of conventional ADFLL has a overshoot or needs a long lock time.

To overcome the sensitive for process variation, we add the circuit block of the filter select. This circuit select the $A_{fil}$ according to the value of $F_{delta}$. The signal of $adj_{out}$ is the signal that decides to operate the filter select. The $Coef_{sel}$ is n-bit output signal which selects the value of $A_{fil}$. Figure 2 shows the block diagram of digital filter. The digital filter is constructed with an adder, a delay element, and a selector. The input signal of an adder uses $F_{delta}[13:0]$ which is one bit extended from $F_{delta}$. The $Z_{n}$ is selected by using $Coef_{sel}$. In this study, $Coef_{sel}$ set to the 2 bit, and the variety of $Z_{n}$ has four types. If the $Coef_{sel}$ is 0b00, $Z_{n}$ is $D_{fil,preout}[10:1]$. In other cases, if the the $Coef_{sel}$ is 0b11, $Z_{n}$ is $D_{fil,preout}[13:4]$. That is to say, the value of $A_{fil}$ takes the value of $1/2^n$. In this study, we target improvement of the lock time, so the value of $A_{fil}$ are decided 4 types (1/2, 1/4, 1/8 and 1/16). The variety of $A_{fil}$ and its value should be predetermined through the pre-simulation of the PVT variation. And, these values are enough to obtain the robustness against PVT variation for a 0.13 $\mu$m CMOS process. However, in the case of advanced process, which is less than 100 nm CMOS process, we should consider to need more choice of $A_{fil}$.

Operation of outputting the $Coef_{sel}$ is as follows: 1) setting the initial value to the DCO, 2) outputting the initial frequency ($f_{init}$) from the DCO, 3) comparing $f_{init}$ and $f_{ref}$, 4) outputting the initial value of the adder which is differ-
ence of \( f_{\text{init}} \) and \( f_{\text{ref}} \), 5) evaluating the variation, 6) outputing the \( \text{Coef}_{\text{sel}} \) from the filter select. The output frequency of DCO is changed by the PVT variation, therefore \( f_{\text{init}} \) is also changed. The filter select evaluates difference of each \( f_{\text{init}} \) and outputing \( \text{Coef}_{\text{sel}} \) according as the PVT variation. Generally, \( \text{Coef}_{\text{sel}} \) will be set once when evaluating the output frequency. Therefore, the value of \( A_{\text{fil}} \) is automatically determined.

3. Digital Controlled Oscillator

In this section, we present Fractional-N digital controlled oscillator (DCO). Firstly, we explain about operation of the proposed DCO. After that, we explain about open-loop gain of the proposed DCO.

3.1 Proposed DCO

Figure 3 shows proposed DCO based on ring oscillator. The proposed DCO is constructed digital controlled current sources and unit cell (inverter). The proposed DCO has 10 bits input signal, signal 2 to 9 are directly connect to the output of digital filter, signal 0 to 1 are connect output of Fractional-N circuit. The output frequency of DCO is given by Eq. (5). Where \( m \), \( T_{\text{HL}} \), and \( T_{\text{LH}} \) mean number of cascade connection of unit cell, delay time which output changes High to Low, and delay time which output changes Low to High, respectively. \( m \) must be set to more than two. In this paper, \( m \) is set to five, because we consider stable oscillation. \( T_{\text{HL}} \) and \( T_{\text{LH}} \) depend on MOS transistor’s transconductance and drainconductance and parasitic capacitance. The MOS transistor’s transconductance and drainconductance can be designed by using drain current of MOS transistor. Therefore, the proposed DCO can design output frequency by using 10 bits input signal.

\[
f_{\text{DCO}} = \frac{1}{m(T_{\text{HL}} + T_{\text{LH}})}
\]

3.2 Fractional-N Circuit

Figure 4 shows Fractional-N circuit. The Fractional-N circuit is constructed with D-FF, nand, not, and selector.

The Fractional-N circuit generates pulse width modulation (PWM) signal of \( f_{\text{out}} \). By using PWM signal, the current of unit cell can control less than 100%. For example, when duty of \( DCO_{\text{frac}} \) is 75%, current of unit cell is \( 0.75 \times I_{\text{base}} \). Where \( I_{\text{base}} \) mean current of digital controlled current sources. In this paper, we set duty of PWM signal to following values 75% (frac11), 50% (frac10), 25% (frac01), 0% (frac00). And \( \text{frac} \) is input signal of selector which select the frac00 to frac11. Therefore, the proposed DCO can finely control the output frequency by using Fractional-N circuit.

3.3 Analysis Model of Open-Loop Gain

Figure 5 shows analysis model of open-loop gain. The proposed ADFLL is constructed with the discrete time circuit, so we replace the discrete time circuit with the continuous time circuit to analyze the open-loop gain, where \( K_{FD} \), \( K_{\text{sigma}} \), \( K_{DCO} \), and \( A_{\text{fil}} \cdot H(s) \) mean gain of the frequency detector, gain of the adder, gain of the DCO, and transfer function of the digital filter, respectively. The gain of the proposed ADFLL can be given by following equation.

\[
A_{\text{OL}} = K_{FD} \cdot K_{\text{sigma}} \cdot K_{DCO} \cdot A_{\text{fil}} \cdot H(s)
\]

Where \( A_{\text{OL}} \) mean open-loop gain of the proposed ADFLL. From Eq. (6), \( A_{\text{OL}} \) can control the gain of each circuit blocks. Furthermore, \( K_{FD} \) and \( K_{\text{sigma}} \) can be given by these equations.

\[
K_{FD} = \frac{1}{\frac{f_{\text{ref}}}{2} + 1}
\]

\[
K_{\text{sigma}} = -1
\]

The denominator of Eq. (7) is considered DC bias point. And \( K_{\text{sigma}} \) equals \( -1 \) because the adder express difference. Next, from relationship between input and output of DCO, \( K_{DCO} \) can be approximately given by Eq. (9).

\[
K_{DCO} \approx 2a \cdot DCO_{\text{in}} + b
\]

Where \( a \), \( b \), and \( DCO_{\text{in}} \) mean coefficient, and operating point of DCO, respectively. \( a \) and \( b \) are identified through the simulation.

Finally, the transfer function of digital filter can express same with first order analog filter, it can be given by Eq. (10).
Fig. 5 open-loop gain analysis model of the proposed ADFLL

\[ A_{fil} \cdot H(s) = \frac{A_{fil} \cdot f_{ref}}{s} \]

(10)

Therefore, \( A_{OL} \) can be given by Eq. (11).

\[ A_{OL} \approx -2a \cdot DCO_{in} + b \cdot \frac{A_{fil} \cdot f_{ref}}{s} \]

(11)

The gain of DCO cannot control the external signal, it that to say, \( A_{fil} \) must use to control the open-loop gain.

4. Simulation Results

Table 1 shows the simulation conditions and simulation results of the proposed ADFLL. In this simulation, we use HSPICE and 0.13 \( \mu \)m CMOS process. In this paper, we apply the proposed ADFLL to the MCU which operates condition shown in Table 1. The simulation result of the static current consumption is calculated using an average of current consumption from 1 msec. to 1.4 msec. when the output frequency has reached a specified value. The simulation result of the output frequency is calculated using an average of output frequency from 1 msec. to 1.4 msec. Figure 6 shows output waveform of the proposed ADFLL. In the Fig. 6, the vertical and horizontal axes mean the output voltage of \( f_{out} \) and the time, respectively. The simulation results indicate that the proposed ADFLL achieved all of design specifications.

4.1 Open-Loop Gain

Figure 7 shows simulation result of the open-loop gain. In the Fig. 7, the vertical and horizontal axes mean the gain and the frequency, respectively. And solid line, dotted line, dashed line and dashed-dotted line mean \( A_{fil} \) (the coefficient of digital filter) equal 1/2, 1/4, 1/8 and 1/16, respectively. The simulation result indicates that the open-loop gain of the proposed ADFLL achieve less than 0 dB when \( A_{fil} = 1/8 \) and \( A_{fil} = 1/16 \).

Generally, a target value of the open-loop gain will be achieved –10 dB when the target frequency. If the open-loop gain is small, the lock time is longer. Furthermore, the open-loop gain and the lock time are in a trade-off relationship. In this study, target frequency is half of the input frequency (16.384 kHz), guaranteed when the open-loop gain is less than or equal to 0 dB in the target frequency. Therefore, we make the improvement of the lock time a priority, and we set the \( A_{fil} \) to 1/8 or 1/16. On the other hands, the stability of the system is very important, because the proposed ADFLL has feedback loop. The stability of the system is guaranteed when the open-loop gain is less than or
equal to 0 dB in the target frequency. The simulation result indicates In the case of the proposed ADFLL, the stability of the system is guaranteed when \( A_{fil} \) is set 1/8 and 1/16.

4.2 Lock Time

Figure 8 shows simulation result of the Lock time each process variation. In the Fig. 8, the vertical and horizontal axes mean the output frequency and the time, respectively. And dashed line solid line, and dotted line mean fast, typical, and slow, respectively. In this simulation, an initial value of DCO is set to 8 and \( A_{fil} \) is fixed to 1/8 in the case of without proposed method. We define the time when the output frequency has reached 99.5% of design value as the lock time. Table 2 shows the comparing result of proposed method and without proposed method. In the case of the fast and the typical, the proposed method cannot be very effective in improvement of the lock time. Because of this, we didn’t select the effective values of \( A_{fil} \) such as 1/2 and 1/4. If we choose 1/2 and 1/4, the overshoot is appeared in the output response of the proposed circuit. The overshoot causes unstable operation. Therefore, we didn’t chose it. However, in the case of the fast and the typical, the lock time can be improved if the overshoot is accorded. In the case of the slow, the lock time is drastically improved. Because \( A_{fil} \) is set to large value (1/4) when the input of digital filter is large (greater than or equal to 1760). It indicates the open-loop gain is increased on a temporary basis. Figure 8 and Table 2 indicate that the proposed ADFLL is reached design value without overshoot, it that to say the proposed ADFLL is robustness for the process variation. And the lock time is improved up to 57%.

5. Experimental Results

Figure 9 shows physical layout design of the proposed AD-FLL. The logic circuits area includes all of digital circuits that are an adder block, a frequency divider block, a frequency detector block, a digital filter block and a filter select block. The DCO area includes a current source block with its bias circuit (a register and a capacitor). And the chip area is 100 × 280 µm².

Figures 10 to 12 show experimental results of the output frequency. In these experiments, a constant-temperature bath was used to keep the temperature conditions. Where the mark of diamond and blue line, the mark of rectangle and red line, the mark of triangle and green line show the case of temperature 40 °C, the case of temperature 25 °C, the case of temperature 125 °C, respectively. And the vertical axis means the \( N_{multi} \), the horizontal axis means the output frequency, respectively. These experimental results indicate that the output frequency is affected according to the power supply voltage and temperature.

Figures 13 to 16 show experimental results of the sta-
standard deviation (clock jitter). Where the mark of diamond and blue line, the mark of rectangle and red line, the mark of triangle and green line show the chip 1, the chip 2, the chip 3, respectively. And the vertical axis means the temperature, the horizontal axis means the standard deviation (clock jitter), respectively. These experimental results indicate that the standard deviation (clock jitter) is affected according to the process variation and the temperature. Especially, Fig. 14 shows the dynamic selecting digital filter coefficient by using Coef_sel is effective for the process variation. As the result, the proposed ADFLL improves the clock jitter, and it value is 0.85 ns.

Table 3 summarizes the comparison of the proposed ADFLL. This results indicate that our proposed ADFLL, which includes the compensation for PVT variation, achieves small chip area without overshoot of output response. However, the clock jitter is worst, so we continue to improve the clock jitter.

6. Conclusion and Future Works

This paper describes the Fractional-N ADFLL with robust-
ness for PVT variation and its application for the microcontroller unit. The proposed ADFLL uses dynamic selecting digital filter coefficient to improve the long lock time and to achieve robustness with the PVT variation. The proposed ADFLL is evaluated through the HSPICE simulation and actual chips using a 0.13 µm CMOS process. These results indicate that the proposed ADFLL is achieved robustness for the PVT variation, and improved lock time up to 57%.

The proposed ADFLL have short lock time (32 clocks) and 0.85 ns jitter.

The future works are as follows; 1) comparing to the other ADFLL, 2) applying any multiple valued logic circuits.

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