A Customized NoC Architecture to Enable Highly Localized Computing-On-the-Move DNN Dataflow

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Abstract—The ever-increasing computation complexity of fast-growing Deep Neural Networks (DNNs) has requested new computing paradigms to overcome the memory wall in conventional Von Neumann computing architectures. The emerging Computing-In-Memory (CIM) architecture has been a promising candidate to accelerate neural network computing. However, data movement between CIM arrays may still dominate the total power consumption in conventional designs. This paper proposes a flexible CIM processor architecture named Domino and “Computing-On-the-Move” (COM) dataflow, to enable stream computing and local data access to significantly reduce data movement energy. Meanwhile, Domino employs customized distributed instruction scheduling within Network-on-Chip (NoC) to implement inter-memory computing and attain mapping flexibility. The evaluation with prevailing DNN models shows that Domino achieves 1.77-to-2.37× power efficiency over several state-of-the-art CIM accelerators and improves the throughput by 1.28-to-13.16×.

Index Terms—Deep Neural Networks, Computing-In-Memory, Network-on-Chip, Computing-On-the-Move Dataflow

I. INTRODUCTION

The rapid development of Deep Neural Network (DNN) algorithms has led to high energy consumption due to millions of parameters and billions of operations in one inference [8] [12]. Conventional processors such as CPUs and GPUs are power-hungry devices and inefficient for AI computations. Therefore, accelerators that improve computing efficiency are under intensive development to meet the power requirement in the post-Moore’s Law era.

One of the most promising solutions is to adopt Computing-In-Memory (CIM) scheme to increase the parallel computation speed with much lower computation power. Recently, both volatile memory and non-volatile memory have been proposed as computing memories for CIM [16] [5]. However, existing works mainly focus on the design of CIM arrays but lack a flexible top-level architecture for configuring storage and computing units of DNNs. These designs need to access off-chip memory frequently, leading to high power consumption and long latency. Therefore, new flexible top-level architecture and efficient dataflow should be studied to meet various requirements of DNNs while achieving high hardware resource utilization and energy efficiency.

Network-on-Chip (NoC) with high parallelism and scalability has attracted lots of attention. In particular, NoC can optimize the process of computing DNN algorithms by organizing multiple cores uniformly under specified hardware architectures [3] [4]. The conventional NoC based CIM architectures such as [9] are inefficient for various convolution kernel sizes and need to load the input activation multiple times. This paper proposes a customized NoC architecture called Domino to enable highly localized inter-memory computing for DNN inference to minimize data reload. Inter-memory computing means that computing like partial sum addition, activation, and pooling is performed in the network when data are moving between CIM arrays. Consequently, “Computing-On-the-Move” (COM) dataflow is proposed to maximize data locality and significantly reduce the energy of data movement. Dataflow is controlled by distributed local instructions instead of an external/global controller or processor. Evaluation results show Domino improves power efficiency and throughput by more than 77% and 28%, respectively.

The rest of the paper is organized as follows: Section II describes the architecture and building blocks of Domino; Section III illustrates the dataflow model; Section IV presents the evaluation setup, experimental results and comparisons; finally, Section VI draws the conclusion.

II. DOMINO ARCHITECTURE

From a top view, Domino mainly consists of an array of tiles interconnected in a 2-D mesh NoC. Weights of each layer (e.g., convolution (CONV) and fully connected (FC) layer) of a neural network will be mapped to a certain group of tiles on Domino, as shown in Fig. 1 (a). By this means, Domino achieves a flexible and distributed computation architecture for DNN acceleration.

A. Domino Tile

A tile includes a CIM array called a Processing Element (PE), a router transferring Input Feature Maps (IFMs) called an RIFM, and a router transferring Output Feature Maps (OFMs) and partial-sums in convolution computation called an ROFM. The basic structure of a tile is illustrated in Fig. 1 (b). The RIFM receives input data from one out of four directions in each tile and controls input dataflow to a remote RIFM, the...
local PE, and the local ROFM. In-memory computing usually starts from the RIFM buffer and ends at Analog-to-Digital Converters (ADC) in a PE (if adopting ReRAM-based CIM arrays). Outputs of a PE are sent to an ROFM for temporary storage or partial-sum addition. The ROFM is controlled by periodic instructions to receive either computation results or input data via a shortcut from an RIFM and maintain dataflow to add up partial-sums.

The ROFM is configured and ruled by localized instructions fitting inter-memory dataflow to support the COM procedure. The compiler generates instructions and configuration for each tile based on initial input data and the DNN structure. The instruction format is shown in Tab. I. Details about inter-memory computing functions are listed in Tab. II.

After cycle-accurate analyses and mathematical derivation, instructions reveal an attribute of periodicity. During the convolution computation, C-type instructions are fetched from the schedule table and executed periodically. When convolution stride \( S_c = 1 \), the period \( p = 2(P + W) \) \( (P \) is the padding size and \( W \) is the width of the IFM) is determined by neural network configuration. When \( S_c \neq 1 \), the compiler will shield certain bits in control words to “skip” some actions in the corresponding cycles to make a correct computation. When an ROFM is mapped and configured to process the last row of a layer in a Convolution Neural Network (CNN), it will generate activation and pooling instructions of M-type. Its period is related to pooling stride \( S_p \), \( p = 2 S_p \). The instructions for pooling layers and FC layers are also periodic.

Partial-sums are added to group-sums when they are transferred between tiles. The group-sums are queued in the buffer for other group-sums to be ready and then form a complete computation result. This method enables inter-memory computing when data are moving between tiles. With localized and customized instructions, Domino manages to reduce the bandwidth demand for transmitting data or instructions through NoC, while maintaining the flexibility for various DNNs.

D. Domino PE

Our main focus is top-level architecture and dataflow rather than the design of CIM cores. Therefore, Domino adopts existing CIM arrays to enable flexible substitution. In our design, each crossbar array has \( N_c \) rows and \( N_m \) columns.

III. DATAFLOW MODEL

Weight Stationary (WS), Output Stationary (OS), and Row Stationary (RS) are three widely used dataflows [14]. However, conventional dataflows are inefficient for CIM schemes. In
this paper, we propose COM dataflow based on WS dataflow to reduce data movement for both partial-sums and IFMs. COM dataflow is customized for CIM architecture with two innovative features: (1) though weights are stationary, the conversion from IFMs to Toeplitz matrices is not required for convolution. Similar to RS dataflow, input activations are reused among different tiles. Therefore, there is no data reload or duplication and the data movement of IFMs is minimized. While in RS, IFMs and weights must be loaded repeatedly during runtime. (2) Partial- and group-sums are stored in tile buffers instead of external global buffers, greatly reducing energy for data movement. Partial-sums are accumulated in the local buffer or when they are transmitting along the array of routers, further minimizing data movement of partial-sums.

A. Dataflow in FC layers

FC layers perform Matrix-Vector Multiplication (MVM) which can be formulated as \( y = xW \), where \( x \in \mathbb{R}^{1 \times C_i} \), \( y \in \mathbb{R}^{1 \times C_{out}} \), and \( W \in \mathbb{R}^{C_i \times C_{out}} \) are input vector, output vector, and weight matrix, respectively. In most cases, an \( N_c \times N_m \) crossbar array is insufficient to map the complete weight matrix in an FC layer. Therefore, an array of tiles with \( \lceil \frac{C_i}{N_c} \rceil \) rows and \( \lceil \frac{C_{out}}{N_m} \rceil \) columns is allocated to efficiently handle Blocked Matrix Multiplication (BMM).

COM dataflow in FC layers is similar to WS dataflow in systolic arrays, but without weights reload during computation. As shown in Fig. 2, each tile maps to a block matrix and the PE multiplies weights with a slice of input. Multiplication results (\( \mathbf{0} \) to \( \mathbf{9} \)) are added while transmitting along a column of tiles. Final addition results in the last tiles of four columns, \( U \) to \( Z \), are small slices of an output vector. Concatenating small slices in all columns gives the complete BMM result.

B. Dataflow in CONV Layers

CONV dataflow in CONV layers varies from existing WS dataflow. Matrix conversion (e.g., im2col) is compulsory in WS dataflow to support convolution operations, which not only requires additional circuits but also greatly increases costs of accessing data in IFMs. We propose a novel dataflow that the matrix conversion is no longer required.

The dimension of a weight tensor in a CONV layer is \( K \times K \times C \times M \), where \( K \) is the filter size, \( C \) is the number of input channels, and \( M \) is the number of output channels. In a simple case that \( N_c = C \) and \( N_m = M \), a slice of a tensor with a size of \( C \times M \) is mapped to a CIM array and the complete weight tensor is mapped to \( K^2 \) tiles. If the size of the CIM array is too small, an array of \( \lceil \frac{C}{N_c} \rceil \times \lceil \frac{M}{N_m} \rceil \) tiles are required for a \( C \times M \) tensor slice. Therefore, a total number of \( K^2 \times \lceil \frac{C}{N_c} \rceil \times \lceil \frac{M}{N_m} \rceil \) tiles are allocated for a weight tensor.

The computation of a data in an OFM is the sum of point-wise MAC resulting from a sliding window. As shown in Fig. 3, we show the weight mapping strategy. Pixels in kernels are mapped to CIM arrays according to their locations and channels in sequence, which is different from that flattens kernels on a single CIM array. Fig. 3 (b) demonstrates the COM dataflow. We define the \( N_m \) point-wise MAC result as the partial-sum, \( U_1 \) to \( U_{K^2} \), and row-wise addition result as the group-sum, \( U_{g1} \) to \( U_{gK} \). Partial-sums and group-sums are sequentially generated and summed up one by one, in different timing and tiles. Partial-sums are generated and transmitted in a pipeline along tiles. Thereby partial- and group-sums are “computed on the move”. Every \( K \) partial-sums (\( U_1 \) to \( U_K \)) are summed up as a group-sum (\( U_{g1} \)). Each group-sum is stored in an ROFM buffer to wait for another group-sum to be ready. In the last tile, \( K \) group-sums (\( U_{g1} \) to \( U_{gK} \)) complete accumulation and an activation function is applied.
in the computation unit of the ROFM.

C. Pooling Dataflow

Computations of CONV and FC layers are processed within an array of tiles, while computations of pooling layers are performed during data transmission between arrays. If a pooling layer follows a CONV layer, with pooling filter size \( K_p = 2 \) and pooling stride \( S_p = 2 \), every four activation results produce a pooling result. As shown in Fig. 4 (b), Domino duplicates weights to produce four activation results \( T \) to \( Y \) in every cycle, which aims to maintain synchronization among layers. When transmitting across tiles, data are compared, and the pooling result \( Z \) is produced. Fig. 4 (c) shows the block reuse scheme that activation results are computed and stored in the last tile. A comparison is taken when the next activation result is computed. The ROFM outputs a pooling result \( Z \) once the comparison in a pooling filter is completed. In this scenario, computation frequency before pooling layers is 4× higher than succeeding blocks.

IV. Evaluation

This section evaluates Domino’s characteristics and performances in detail. We also compare Domino against other state-of-the-art CIM-based architectures.

A. Experiment Setup

The configuration of Domino and its tile is displayed in Tab. III. Buffer parameters are based on the silicon-proven SRAM array in [15]. On-chip data transmission energy is simulated by Noxim [1], and the rest is analyzed by PrimeTime with a 45 nm CMOS process. The step frequency for the execution of one instruction is 10 MHz and thus the bandwidth between tiles is 40 Gbps. Frequency division multiplexing with 160 MHz clock frequency is implemented in peripheral circuits to reduce the hardware area. Eight 80 Gbps transceivers, adopted from [11], serve as inter-chip connections. The supply voltage is 1 V and the precision is 8 bits. Our model adopts CIM arrays whose size is \( 256 \times 256 \), and the number of total CIM arrays depends on the scale of neural networks. We run several prevailing CNN models in Domino architecture built by SystemC.

In Tab. IV, the counterpart results on the adjacent column are normalized to our aforementioned settings. The array size and bit precision are normalized by linear scaling factors. Let \( B_{wt} \), \( B_{at} \), \( B_{ad} \) and \( B_{wd} \) be the weight precision of target architecture, activation precision of target architecture, weight precision of Domino, and activation precision of Domino, respectively. The scaling factor is \( \frac{B_{wt} B_{at} B_{wd}}{B_{ad} B_{at}} \) for MAC and \( \frac{B_{wt} B_{wd}}{B_{ad}} \) for the rest of operations and data movement. To make a fair energy efficiency comparison, we further normalize technology nodes and supply voltage using equations given in

### TABLE III

| Component      | Descript. | Energy/Compo. | Area (\( \mu m^2 \)) |
|----------------|-----------|---------------|---------------------|
| Buffer         | 256B×1    | 281.3 pJ      | 826.5               |
| Control circuits |          | 10.4 pJ       | 1400.6              |
| RIFM total     |           |               | 22271               |
| Adder          | 8b×8×2    | 0.02 pJ/8b    | 0.07                |
| Pooling        | 8b×8      | 7.7 fJ/8b     | 34.06               |
| Activation     | 8b×8      | 0.9 fJ/8b     | 7.07                |
| Data buffer    | 16KB      | 281.3 pJ      | 52896               |
| Schedule table | 16b×128   | 2.2 fJ/16b    | 826.5               |
| Input buffer   | 64b×2     | 42.1 fJ/64b   | 878.9               |
| Output buffer  | 64b×2     | 42.1 fJ/64b   | 878.9               |
| Control circuits |         | 28.5 fJ       | 2451.2              |
| ROFM total     |           |               | 59792.7             |
| Inter-chip Conn. | 80 Gbps×8 | 0.55 fJ/b    | 8E5                 |

### TABLE IV

**Domino’s evaluation results and pairwise comparisons under different DNN models.**

| Dataset | CIFAR-10 | | | | ImageNet | |
|---------|----------|----------|----------|----------|----------|--------|
| Model   | VGG-11 [9] | ResNet-18 [7] | VGG-16 [12] | VGG-19 [12] | |
| Architecture | [2] Ours | [17] Ours | [16] Ours | [10] Ours | [6] Ours |
| CIM type | SRAM     | SRAM     | SRAM     | ReRAM    | ReRAM    | ReRAM  |
| Technology (nm) | 16 | 45 | 65 | 45 | 40 | 45 | 65 | 45 |
| Technology (V) | VDD (V) | 0.8 | 1 | 1 | 1 | 0.9 | 1 | 1 | 1 |
| Frequency (MHz) | 200 | 10 | 10 | 10 | 100 | 10 | 1200 | 10 | 1200 | 10 |
| Activation & Weight precision | 4 | 8 | 4 | 8 | 8 | 8 | 16 | 8 | 16 | 8 |
| # of CIM cores/chip & chips | 16 | 240×5 | 4 | 240×6 | 1 | 240×10 | 160 | 240×10 | 80 - 112 | 240×10 |
| Active area (\( mm^2 \)) | 17.5 | 343.2 | 5.68 | 655.2 | 0.44 | 381.6 | 6.89 | 192.0 | 0.99 | 125.5 |
| Execution time (us) | 128 | 137.3 | 1890 | 206.3 | 670K | 3481.8 | 6920 | 3582.9 | n.a. | 3582.9 |
| Power (W) | 0.15 | 11.03 | 2.78m | 18.10 | 11.05m | 4.26 | 4.8 | 8.73 | 3m | 4.57 |
| On-chip data power (W) | 0.036 | 3.53(3.50) | 1.76m | 2.95(2.93) | 1.47m | 0.64(0.63) | 0.54 | 0.72(0.71) | 0.7m | 0.72(0.71) |
| Off-chip data power (W) | 0.06 | 0.34 | n.a. | 0.10 | 4.76m | 0.005 | 1.32 | 0.01 | 0.9m | 0.01 |
| CE (TOPS/W) | 71.39 | 17.22 | 6.91 | 6.30 | 4.15 | 9.29 | 0.68 | 5.73 | 1.96 | 10.95 |
| Normalized CE (TOPS/W)-1 | 9.53 | 17.22 | 2.82 | 6.30 | 3.92 | 9.29 | 2.73 | 5.73 | 6.18 | 10.95 |
| Throughput (TOPS/mm²) | 0.7 | 0.55 | 0.006 | 0.17 | 0.10 | 0.10 | 0.36 | 0.22 | 0.10 | 0.66 |
| Normalized throughput (TOPS/mm²)-1 | 0.088 | 0.55 | 0.013 | 0.17 | 0.081 | 0.10 | 0.18 | 0.22 | 0.21 | 0.66 |
| Images/second | 488 | 2604 | 8 | 2604 | n.a. | 53 | n.a. | 53 | n.a. | 53 |
| Accuracy(%) | 91.51 | 89.85 | 91.15 | 91.57 | 46 | 70.71 | n.a. | 72.38 | n.a. | 72.38 |

*1 Adapted and normalized from average statistics. *2 In parentheses is power of on-chip data movement included. *3 Normalized to 8-bit, 1 V, and 45 nm according to [13]. *4 Normalized to 8-bit, 45 nm.
B. Performance Results

1) Computational Efficiency: Domino achieves higher Computational Efficiency (CE) than its state-of-the-art counterparts. Results show Domino has 77% (compared to 6) to 137% (compared to 16) improvement of CE. The reason is Domino largely reduces the energy consumption of both on- and off-chip data movement. Some unique “skip” operations appeared in ResNet only affects performances slightly. Data locality and COM dataflow are very efficient in reducing overall energy consumption for CNN inference. Thereby, peripheral energy decreases and system CE increases.

2) Throughput: Domino has an obvious advantage over other architectures in terms of throughput with respect to area. The area per chip is determined by two factors: the area of one tile including substituted CIM arrays and Domino’s routers, and the number of tiles according to mapping strategy. We calculate the area of an equivalent CIM array of 256×256 from counterpart models. Throughput is improved by 1.28× to 13.16×.

We also compared the inference speed of different neural network models. To make a fair comparison, we normalize the inference speed to one CIM core (images per second per CIM core). Results show that the inference speed is improved by more than five times. This improvement is benefited from layer synchronization, weight stationary, data locality, and COM dataflow, which help to reduce the computing latency and maximize parallelism.

3) Power Breakdown: We break down the total power consumption into three parts: CIM power, on-chip data power and off-chip data power. Because Domino uses others’ CIM arrays, power consumption of CIM is not listed. On-chip data power includes on-chip data movement and computation power except CIM, while off-chip data power is responsible for inter-chip communication. When a DNN is too large to be mapped onto a single chip, e.g., ResNet-50, VGGNet, off-chip access is inevitable, involving inter-chip data movement such as IFMs and OFMs. However, as listed in Tab. IV, data movement only accounts for a small portion (8% to 32% for on-chip and 0.1% to 3% for off-chip), which means Domino efficiently reduces the overhead of data movement.

V. Conclusion

This paper has presented a customized NoC architecture called Domino with highly localized inter-memory computing for DNNs. Key contributions and innovations can be concluded as follows: (1) Domino changes the conventional NoC tile structure by using dual routers for different usages, and enables substitution of PEs; (2) Domino utilizes an efficient COM dataflow to minimize data movement; and (3) a set of periodical instructions is defined to maximize the data locality. Compared with several conventional architectures, Domino has improved computational efficiency and throughput by 1.77-to-2.37× and 1.28-to-13.16×, respectively.

References

[1] V. Catania, A. Mineo, S. Monteleone, M. Palesi, and D. Patti, “Cycle-accurate network on chip simulation with noxim,” ACM Trans. Model. Comput. Simul., vol. 27, no. 1, Aug. 2016. [Online]. Available: https://doi.org/10.1145/2953878
[2] K. Chellappilla, S. Puri, and P. Simard, “High performance convolutional neural networks for document processing,” 10 2006.
[3] Y. Chen, T. Yang, J. Emer, and V. Sze, “Eyeriss v2: A flexible accelerator for emerging deep neural networks on mobile devices,” IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 9, no. 2, pp. 292–308, 2019.
[4] Y.-H. Chen, J. Emer, and V. Sze, “Eyeriss: A spatial architecture for energy-efficient dataflow for convolutional neural networks,” in Proceedings of the 43rd International Symposium on Computer Architecture, ser. ISCA ’16. IEEE Press, 2016, p. 367–379. [Online]. Available: https://doi.org/10.1109/ISCA.2016.60
[5] Y. D. Chih, P. H. Lee, H. Fujusawa, Y. C. Shih, C. F. Lee, R. Naous, Y. L. Chen, C. P. Lo, C. H. Lu, H. Mori, W. C. Zhao, D. Sun, M. E. Sinangil, Y. H. Chen, T. L. Chou, K. Akarvardar, H. J. Liao, Y. Wang, M. F. Chang, and T. Y. J. Chang, “16.4 an 890tops/w and 16.3tops/mm2 all-digital sram-based full-precision compute-in-memory macro in 22nm for mac-based learning edge applications,” in 2021 IEEE International Solid-State Circuits Conference (ISSCC), vol. 64, 2021, pp. 252–254.
[6] T. Chou, W. Tang, J. Botimer, and Z. Zhang, “Cascade: Connecting rrams to extend analog dataflow in an end-to-end in-memory processing paradigm,” in Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture, ser. MICRO ’52, New York, NY, USA: Association for Computing Machinery, 2019, p. 114–125. [Online]. Available: https://doi.org/10.1145/3352460.3358328
[7] K. He, X. Zhang, S. Ren, and J. Sun, “Deep residual learning for image recognition,” 06 2016, pp. 770–778.
[8] J. Hu, L. Shen, and G. Sun, “Squeeze-and-excitation networks,” in 2018 IEEE/CVF Conference on Computer Vision and Pattern Recognition, 2018, pp. 7132–7141.
[9] H. Jia, M. Ozatay, Y. Tang, H. Valavi, R. Pathak, J. Lee, and N. Verma, “15.1 a programmable neural-network inference accelerator based on scalable in-memory computing,” in 2021 IEEE International Solid-State Circuits Conference (ISSCC), vol. 64, 2021, pp. 236–238.
[10] X. Qiao, X. Cao, H. Yang, L. Song, and H. Li, “Atomlayer: A universal reram-based cnn accelerator with atomic layer computation,” in 2018 55th ACM/EDAC/IEEE Design Automation Conference (DAC), 2018, pp. 1–6.
[11] B. Razavi, “Design techniques for high-speed wireline transmitters,” IEEE Open Journal of the Solid-State Circuits, vol. 1, pp. 53–66, 2021.
[12] K. Simonyan and A. Zisserman, “Very deep convolutional networks for large-scale image recognition,” in 3rd International Conference on Learning Representations, ICLR 2015, San Diego, CA, USA, May 7-9, 2015, Conference Track Proceedings, Y. Bengio and Y. LeCun, Eds., 2015. [Online]. Available: http://arxiv.org/abs/1409.1556
[13] A. Stillingmaker and B. Baas, “Scaling equations for the accurate prediction of cmos device performance from 180nm to 7nm,” Integration, the VLSI Journal, vol. 58, 02 2017.
[14] V. Sze, Y. Chen, T. Yang, and J. S. Emer, “Efficient processing of deep neural networks: A tutorial and survey,” Proceedings of the IEEE, vol. 105, no. 12, pp. 2295–2329, 2017.
[15] S. L. Wu, K. Y. Li, P. T. Huang, W. Hwang, M. H. Tu, S. C. Lung, W. S. Peng, H. S. Huang, K. D. Lee, Y. S. Kao, and C. T. Chuang, “A 0.5v-28nm-256kb mini-array based 6t sram with wrap-tracking write-assist,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 7, pp. 1791–1802, 2017.
[16] J. H. Yoon, M. Chang, W. S. Khwa, Y. D. Chih, M. F. Chang, and A. Raychowdhury, “29.1 a 40nm 64kb 56.67tops/w read-disturb-tolerant compute-in-memory/digital sram macro with active-feedback-based read and in-situ write verification,” in 2021 IEEE International Solid-State Circuits Conference (ISSCC), vol. 64, 2021, pp. 404–406.
[17] J. Yue, Z. Yuan, X. Feng, Y. He, Z. Zhang, X. Si, R. Liu, M. Chang, X. Li, H. Yang, and Y. Liu, “14.3 a 65nm computing-in-memory-based cnn processor with 2.9-to-35.8tops/w system energy efficiency using dynamic-sparsity performance-scaling architecture and energy-efficient inter/intra-macro data reuse,” in 2020 IEEE International Solid-State Circuits Conference - (ISSCC), 2020, pp. 234–236.