±25 ppm repeatable measurement of trapezoidal pulses with 5 MHz bandwidth

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ABSTRACT: High-quality measurements of pulses are nowadays widely used in fields such as radars, pulsed lasers, electromagnetic pulse generators, and particle accelerators. Whilst literature is mainly focused on fast systems for nanosecond regime with relaxed metrological requirements, in this paper, the high-performance measurement of slower pulses in microsecond regime is faced. In particular, the experimental proof demonstration for a 15 MS/s, ±25 ppm repeatable acquisition system to characterize the flat-top of 3 µs rise-time trapezoidal pulses is given. The system exploits a 5 MHz bandwidth circuit for analogue signal processing based on the concept of flat-top removal. The requirements, as well as the conceptual and physical designs are illustrated. Simulation results aimed at assessing the circuit performance are also presented. Finally, an experimental case study on the characterization of a pulsed power supply for the klystrons modulators of the Compact Linear Collider (CLIC) under study at CERN is reported. In particular, the metrological characterization of the prototype in terms of bandwidth, repeatability, and linearity is presented.

KEYWORDS: Data acquisition circuits; Instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons); Accelerator Subsystems and Technologies; Accelerator Applications

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1 Introduction

Pulsed power supplies are widely applied to radars, pulsed laser, electromagnetic pulse generators, and particle accelerators. In this framework, the full characterization of power pulses is needed, both in time and frequency domains, in order to guarantee an adequate quality to power supply. The market interest and the research on pulse measurements are significantly dedicated to improving the immunity to interferences demanded by the transmission protocols in ultra-wide band applications [1]. This trend was highlighted in the state of the art for time-domain pulse waveform measurements in the nanosecond regime, produced by the National Institute of Standards and
Figure 1. Pulse parameters definition.

Table 1. Typical pulse characteristics.

| Pulse specification                  | Acronym | Value  |
|--------------------------------------|---------|--------|
| Nominal Pulse Amplitude Level        | $V_{kn}$| 150 kV |
| Nominal Pulse Current Level          | $I_{kn}$| 160 A  |
| Pulse Peak Power                     | $P_{mod-out}$| 24 MW  |
| Positive Going Transition Duration   | $t_{rise}$| 3 µs   |
| Negative Going Transition Duration   | $t_{fall}$| 3 µs   |
| Transition Settling Duration         | $t_{set}$| 5 µs   |
| Flat-Top Duration                    | $t_{flat}$| 140 µs |
| Repetition Rate                      | REPR    | 50 Hz  |
| Voltage Overshoot                    | $V_{ovs}$| 1%     |
| Flat-Top Tolerance                   | FTT     | 0.85%  |
| Pulse-to-Pulse Repeatability         | PPR     | ±100 ppm|
| Frequency Range of Interest          | FRI     | 1 kHz–5 MHz |

Technology (NIST) [2]. The main evolution efforts were dedicated to push the technology toward to the sub-nanosecond regime. Even if the reference standards concerning pulse measurements [3] give both definitions and procedures to evaluate the pulse parameters, a full characterization procedure in time-domain is not provided; thus, custom methods have to be identified along the specific applications. New, more demanding applications arise from particle accelerators for high-energy physics. At CERN, a new particle accelerator is currently under study, the Compact Linear Collider (CLIC). Its klystron modulators [4] will be operated in pulsed mode with a pulse length of 140 µs [5, 6]. In figure 1 and table 1, an input pulse and its typical specifications, respectively, are reported. To meet the requirements for the RF power quality, derived directly from the accelerator performance specifications, the modulator precision and flat-top pulse-to-pulse repeatability,
should be guaranteed by a specific reference acquisition system. Whilst pulse measurement literature is mainly focused on fast systems with relaxed metrological requirements, in this paper a new research trend on slower signals with stringent metrological requirements is explored. In particular, an acquisition system to characterize the flat-top of 3 μs rise-time trapezoidal voltage pulses, with bandwidth of 5 MHz, repeatability of ±25 ppm, and noise RMS level in the order of 3 ppm, is proposed. In section 2, the requirements for the proposed acquisition system as well as the definition of the main target parameter, the Pulse-to-Pulse Repeatability (PPR), are defined. Afterwards, in section 3, the proposal of an analogue front-end for improving the measurement conditions is presented together with its design choices. This circuit is a proof demonstrator for validating the feasibility and effectiveness of the proposed architecture. In section 4 and 5, Pspice simulations and experimental results are presented in order to highlight a good match between the simulated demonstrator and the actual prototype. In section 6, a Differential Sensing Circuit (DSC) for decoupling the upstream voltage divider (discussed afterwards) and its load, the presented acquisition system, is illustrated. Finally, in section 7, the conclusions as well as the future developments of the proposed architecture are discussed.

2 Requirements

The complete measurement system consists of a high-precision high-voltage divider, able to convert 150 kV pulses into 10 V pulses [7], and a high-speed high-repeatability acquisition system. However, the interest of this paper is limited only to the acquisition system; as a matter of fact, all the contribution of the upstream voltage divider are neglected so far, focusing only on the custom analogue front-end and the digitizer.

2.1 Pulse-to-Pulse Repeatability

The Pulse-to-Pulse Repeatability (PPR) is defined as (figure 2):

$$\text{PPR} = \max|V_{i,j} - V_{i,j+1}|$$

(2.1)

By considering two consecutive pulses flat-tops and their instantaneous voltage values in the same (in equivalent time) sampling instant $i$ within the waveform flat-top (figure 2), $V_{i,j}$ and $V_{i,j+1}$, the main goal of the measuring system is to verify that:

$$\text{PPR} \leq \text{PPR}_{\text{max}}$$

(2.2)

ANSI/NCSL Z540.3-2006 states: (i) “The laboratory shall ensure that calibration uncertainties are sufficiently small so that the adequacy of the measurement is not affected” and (ii) “Collective uncertainty of the measurement standards shall not exceed 25% of the acceptable tolerance” [8], defining the Test Uncertainty Ratio (TUR) as 1 : 4. As a consequence, in order to adequately characterize the pulses with repeatability tolerance (PPR$_{\text{max}}$) e.g. of ±100 ppm, the target repeatability of the measurement system should be better than ±25 ppm.
2.2 The acquisition system

The project CLIC of CERN requires the repeatability specification to be respected only during the pulse flat-top, for the range of frequencies (1 kHz, 5 MHz) [5]. To prove pulse-to-pulse repeatability up to 5 MHz, the acquisition system has to sample at least at a rate of 10 MS/s according to the Nyquist criterion. In addition, if the acquisition system has a suitable stability within the repetition period of the pulses train (20 ms), the only factor that could affect PPR is noise (including quantization noise). By assuming a known distribution for the system’s noise, a statistical relation between RMS noise and peak-based PPR exploits the concept of confidence interval (such as usual for type-A uncertainty in the ISO Guide of Uncertainty [9]). Furthermore, the resolution is often used as the first-approach index for evaluating the suitability of an instrument for a measurement. In this case, an instrument with an LSB greater than 25 ppm cannot ensure a PPR better than 25 ppm. For taking into account the actual non-ideality of the acquisition board, the effective resolution in terms of ENOB (Effective Number Of Bits) is considered (as usual in experimental physics under suitable assumptions about the actual quantizer model underlying the ENOB definition). Under these hypotheses, the specification on repeatability can be translated into a corresponding constraint on noise. In this case, for a direct sampling of the pulse with an input range of (0, 10) V, a necessary (but not sufficient) condition to assess signal variations in the order of 25 ppm is:

$$\text{LSB} = \frac{\text{Input Range}}{2^{\text{ENOB}}} = \frac{10V}{2^{\text{ENOB}}} < 25 \text{ ppm} = 250 \mu V \iff \text{ENO} > 15.3$$

(2.3)

3 Analogue conditioning system

3.1 Basic ideas

Nowadays, state-of-the-art acquisition systems on the market, operating at sampling rates equal or higher than 10 MS/s with a full scale of at least 10 V, do not exceed 14 nominal bits. Conversely, acquisition boards (such as NI-PXI-5922 from National Instruments) reach also 15 MS/s with a nominal resolution of 16 bits, but with a maximum input range of ±5 V. This does not allow direct
measurements of the 10 V pulses, therefore an analogue pre-conditioning front-end is needed. The basic idea is to conceive a conditioning system that subtracts the nominal value of the flat-top from the pulse and amplifies the resulting signal (figure 3). This allows the requirements of the digitization to be relaxed, by amplifying the most significant part of the input signal, the pulse flat-top. As a matter of fact, the repeatability specification (PPR) has to be verified only during the flat-top of the pulse; by placing the flat-top around zero, the analogue front-end of the conditioning system improves the dynamic range of the digitization. However, this conditioning circuit introduces a certain amount of noise, much higher than the quantization noise of the acquisition board, which needs to be carefully minimized in the design.

3.2 Concept design

The architecture of the front-end is outlined in figure 4. The upper input buffer provides very-high input resistance to the preceding high-voltage divider, while the lower buffer centers the 10 V pulse flat-top around zero, in order to improve the dynamic range of the digitization. The subsequent gain stage amplifies the pulse flat-top, in order to best fit the acquisition board range ±5 V. The clipping stage avoids saturation of the subsequent acquisition board input circuitry. This ensures all the devices of the circuit work in their linear region of operation, in order to assure their long-
term performance. The range ±5 V is used because the ±1 V is not compatible with the adopted clipping strategy. In fact, clipping with levels as low as ±1.25 V is unfeasible owing to the over-voltage handling of the NI PXI-5922, that shows an unexpectedly long recovery time. Lower clipping rails would reduce the useful range and give rise to high non-linearity arising from the diodes behavior in the clipping region. With a ±5 V full-scale, the clipping levels are set to about ±4.7 V dedicating a useful range of ±2.5 V for the flat-top. The flat-top tolerance of about 85 mVpp is fit into the ±2.5 V range by means of a total amplification of about 50 V/V.

3.3 Physical design

A circuit performing the above mentioned tasks is depicted in figure 5. The overall gain of about 50 V/V, chosen for the above mentioned reason, is realized by two separated stages since no adequately low-noise operational amplifiers have a bandwidth of at least 5 MHz for such a gain. In the proof demonstrator, the two input signals are firstly filtered through two simple RC low-pass filters in order to reduce the input noise (indeed the final version of the system will be equipped by the mentioned interface to the voltage divider discussed in 6); the 10VDC channel is heavily filtered (16 Hz) whereas the input pulse channel needs to be wide-band (20 MHz). The two buffers (model OPA627 of Texas Instruments) have the following characteristics:

- Supply voltage range up to ±18 V (±15 V rails were used in order to have an input voltage range of at least ±10 V).
- High input resistance, in order to minimize input bias current (10 pA is the maximum input bias current specified on the datasheet).
- Low input capacitance (7 pF specified on the datasheet), in order to not affect the compensation of the voltage divider (taking into account also the capacitance of the long connection cables in the order of hundreds of pF).
- A current noise spectral density of 2.5 fA/√Hz and a voltage noise of 4.5 nV/√Hz. At to date, the high-voltage divider has not been designed yet at CERN by the CLIC Team. Thus,
the actual value of its lower-arm equivalent resistance is not available. In any case, even if an equivalent resistance of 100 kΩ is assumed, a voltage noise of 0.25 nV/√Hz is achieved on the buffer, still negligible with respect to its voltage noise.

- Very good dynamic performance, in order to have a bandwidth of at least 5 MHz, in particular for the positive input buffer (16 MHz at gain of 1 is declared).

Two fast diodes (model LL4148) in anti-parallel clip the input differential signal in order to not saturate the difference amplifier (nominal gain of 7.5) when the signal on the inverting input is zero (i.e., without pulse). In this stage, the input resistors (R3 and R4) are split in order to limit the current flowing through the diodes when they are active; in particular, R3' and R4' limit the current before and after the flat-top of the pulse. R3 = R3' + R3'' together with R5, as well as R4 = R4' + R4'' together with R6, set the gain during the flat-top (when the diodes are OFF). The voltage drop across the diodes, when they are ON, is conversely amplified by the ratio R5/R3'' = R6/R4''. Therefore, by choosing R3' = R3'' and R4' = R4'', the flat-top gain is half of the gain seen by the voltage drop across the diodes when they are active. Obviously, the same clipping operation has to be repeated at the output of the same stage. Also for this stage, the same fast diodes were chosen (model LL4148). The clipping voltage is conveniently set by means of two opposite rails in this stage. A non-inverting stage (nominal gain of 6.9) was chosen owing to its high input impedance, making resistor R7 ininfluent for the gain setting. Two identical amplifiers (model ADA4898 of Analog Devices) were chosen for the two amplifying stages owing to their excellent performance in terms of:

- Input noise (0.9 nV/√Hz declared);
- Bandwidth (65 MHz at gain of 1 allows the 7.5 amplification assuring more than 8 MHz bandwidth);
- Supply voltage range of ±15 V allowed in order to have an input voltage higher than 10 V.

Finally, after the second amplification stage, a last pair of clipping diodes (same model LL4148) are needed to avoid over-range in the input stage of the subsequent acquisition board (the two rail voltages can be set according to the input stage limits). The last consideration is about the requirements on resistor quality; in figure 5, all the resistors in red affect the overall gain stability and CMRR [10]. An array of 8 matched precision resistors can guarantee at the same time high gain stability (low temperature coefficient can easily be achieved) and high CMRR (low relative tolerances down to 0.01% can be specified).

4 Simulation results

The performance of the analogue front-end was assessed in simulation, by analyzing:

- Amplitude frequency response, in order to verify the required 5 MHz bandwidth (the phase delay was not assessed because not relevant for repeatability measurements);
- Noise, in order to estimate the RMS noise introduced by the conditioning system, directly affecting PPR (according to what already mentioned in 2.2);
4.1 Amplitude frequency response

In figure 6, the result of the frequency response simulation is shown. The $-3$ dB point is located around 5 MHz, therefore the first specification is proved to be achievable.

4.2 Noise analysis

Under the hypotheses of a good system stability within the repetition period of the train of pulses, the system noise is the only factor affecting PPR and its assessment is essential for achieving the required target. A behavioral model-based analysis of the analogue front-end allows the RMS value of the noise power spectral density (PSD) to be assessed as:

$$N_{\text{rms}} = \sqrt{\int_{f_L}^{f_H} \text{PSD}(f)df}$$

(4.1)

where the integration boundaries $f_L$ and $f_H$ used in simulation are 1 kHz and 100 MHz, respectively. Initially, the accuracy of the amplifiers noise model was verified by comparing the results of the noise simulation of each device and the datasheet specification. In figure 7, a RMS noise of about 4.7 ppm Referred To Input (RTI), obtained by PSpice, is shown. This is the amount of noise expected at the input of the acquisition board. The final value of noise of the acquisition as a whole...
can be assessed by considering the filtering effect of the limited bandwidth of the downstream acquisition board. As an example, the NI-PXI-5922 has a nominal bandwidth of 6 MHz when sampling at its maximum speed of 15 MS/s. As a first approximation, the filtering effect of the board can be taken into account by considering the simulation results up to 6 MHz (instead of 100 MHz): a RMS value of about 3.1 ppm RTI is estimated in this case.

### 4.3 Linearity

This test allowed the linearity error RTI, shown in figure 8, to be calculated. By statically varying the differential input, the input-output characteristic can be evaluated and the linearity error calculated as:

\[
E_{\text{ppm}} = \frac{V_{\text{out}} - G \cdot V_{\text{in}} - \text{Offset}}{G \cdot 10 \mu V}
\]

The simulation was obtained in Pspice by performing (i) a DC primary sweep from \(-\text{FTT}/2\) (FTT: Flat Top Tolerance) to \(\text{FTT}/2\) (rigorously from \(-42.5\) mV to \(+42.5\) mV but, in order to include some additional margins the input sweep was performed from \(-60\) to \(+60\) mV), and a (ii) temperature secondary sweep from 20 to 50°C in order to obtain the variation of the linearity error with temperature. The maximum error occurs at 50°C and is less than 4 ppm.

### 4.4 Settling time

An input step from 0 to 10 V with rise time of 10 ns is applied at the positive input of the analogue front-end (the negative input is connected to a 10V\(_{\text{DC}}\) source) by measuring the output transition. Figures 9 show a settling time comfortably shorter than the required 5 \(\mu\)s (table 1); in particular, in figure 9(a), the whole transition is shown for both input and output signals, while in figure 9(b), a zoom on the settling point is depicted (in this case the output signal is Referred To Input, RTI, and translated in ppm of the full scale). However, in nominal working conditions, a step signal with a rise time shorter than 3 \(\mu\)s is not expected, thus the settling time is expected not to be a critical issue for this application.
Figure 8. Non-linearity curves at different temperatures.

Figure 9. Response to 10 V–10 ns step (input step in green, output step in blue): (a) whole response, (b) zoom (in ppm Referred To Input, RTI).

5 Experimental results

The design of the proposed circuit was validated experimentally within a case study for the CLIC project at CERN, summarized in table 1.

5.1 Amplitude frequency response

The measurement setup, shown in figure 10(a), consists of an arbitrary waveform generator (Agilent 33220A) and two digital multimeters (HP 3458A). The two multimeters were firstly characterized up to 10 MHz and, in the worst case, their difference was smaller than 0.6 dB. A set of sine waves of small amplitude (20 mVpp) was generated by the arbitrary waveform generator with frequency ranging from 10 kHz to 100 MHz and sent both to a multimeter and the analogue front-end. At each step, the rms values of the two signals (input and output of the analogue front-end) were measured by the two multimeters in AC voltage mode in order to obtain the corresponding
point on the Bode diagram. The experimental results, shown in figure 10(b), are compatible with the simulation ones. Moreover, a good flatness is observed up to 5 MHz, where the $-3$ dB point is located.

5.2 Noise analysis

The measurement setup shown in figure 11(a) allows the noise affecting the system composed by the analogue front-end and the acquisition board NI PXI 5922 to be assessed. Preliminarily, the NI PXI 5922 internal noise with its inputs shorted to ground was proved to be negligible with respect to the analogue front-end’s one. The noise of the analog front-end was tested with the measuring channel in unbalanced differential configuration and a RMS noise of about 3.0 ppm RTI was assessed. The results proved that the experimental and simulated noise levels of the circuit, respectively 3.0 ppm and 3.1 ppm at 6 MHz, are compatible. However, this proof demonstrator is not optimized in terms of noise immunity (e.g. it is not shielded), therefore, a lower noise can be achieved in an engineered version of the circuit.
5.3 Linearity

This test allows the linearity error to be assessed in the same conditions as the analogous simulation analysis. The measurement setup of figure 12(a) consists of a 10 V DC reference named PBC [12] and a DAC (AN 3200) with a resolution of 10 µV. At each step, the DAC generates a DC voltage ranging from 9.940 V to 10.060 V in order to obtain the same differential input sweep used in simulations. Both multimeters are set for DC voltage measurements with an aperture of 50 power line cycles. For each input value, N = 5 samples are acquired in order to evaluate the measurement repeatability (σ/√N). The test results, calculated according to equation (4.2) and depicted in figure 12(b), match the simulation ones, with a non-linearity error of less than 2 ppm of 10 V at a temperature of 21°C.

5.4 Repeatability results

Once the main performance forecast by simulation has been experimentally confirmed on the prototype, twofold tests of repeatability aimed at validating the design as a whole were carried out: (i) in short circuit, for assessing the intrinsic repeatability of the circuit without any input signal, and (ii) in operation, for assessing the Common Mode Rejection, because, during the pulse flat-top, both input voltages are around 10 V.

5.4.1 Short-circuit test

For this test, a laboratory setup analogous as for noise characterization with both the inputs at ground (figure 11(a)) was used. The Pulse-to-Pulse Repeatability was computed according to eq. (2.1) by means of two noise acquisitions lasting 150 µs each (2250 samples at 15 MS/s) and spaced by an idle time of 20 ms in order to emulate the acquisition of two consecutive pulses. The procedure was repeated 300 times (emulating 300 pulses) to obtain the histogram of PPR in figure 13. The mode of the distribution is about 15 ppm while the maximum, obtained as the maximum amongst 675000 samples (2250 · 300), is below 25 ppm. This confirms the suitability of the design for the reference acquisition system.
Figure 13. Repeatability measured in short circuits.

![Diagram of Fluke 732A or PBC with 10 V DC input](image)

Figure 14. Setup for repeatability measurement with 10 V$_{DC}$ at both inputs.

![Histograms showing PBC and Fluke 732A](image)

Figure 15. Estimated repeatability with 10 V$_{DC}$ at both the inputs.

5.4.2 Common Mode Rejection test

The test setup depicted in figure 14 allows the CMRR of the system to be tested when a DC common voltage of 10 V is connected to both the analogue front-end inputs. Two different reference DC generators were used, the PBC [12] and the Fluke 732A, in order to evaluate the generator contribution. The results, of figures 15 show that the repeatability as assessed by the generator Fluke732A (figure 15(b)) is significantly worse than by the PBC (figure 15(a)), by considering both the mode and the tails of the distribution. This difference is caused both by a higher instrumental noise of the 732A (producing a higher common mode noise because the 732A is applied to both the inputs).
and by the CMRR of the circuit. As stated in 3.3, CMRR is heavily affected by the quality of the resistors used in the prototype [10]. In fact, the CMRR of a difference amplifier is given by:

$$CMRR \approx \frac{1}{2} \left( \frac{G_{DIFF} + 1}{\frac{1}{2}(G_{DIFF} + 1)\left(\frac{1}{CMRR_{AMP}}\right)} + \frac{\Delta R}{R} \right)$$

(5.1)

where:

- $G_{DIFF}$ is the differential gain of the amplifier ($\approx 7.5$);
- $CMRR_{AMP}$ is the CMRR declared on the datasheet of the amplifier ($\approx 120$ dB);
- and $\frac{\Delta R}{R}$ is the tolerance of the resistors involved in differential gain setting (0.1% are used in the prototype).

This highlights a CMRR of about 66 dB by considering the worst case of resistors with combined maximum relative uncertainty of 0.2%. CMRR can be improved by replacing the presently used 0.1% resistors by a set of matched 0.01% resistors. In this circumstance, a worst-case CMRR of about 86 dB is estimated. The higher common mode noise of the generator Fluke732A is expected to be rejected by the circuit, and the PPR improved accordingly. However, this test allows measuring the repeatability performance of a generator plus the acquisition system; since the real interest of this paper is limited to the characterization of the acquisition system repeatability, the short circuit test should be considered as the reference.

6 The Differential Sensing Circuit

In the final version of the analogue front-end, a Differential Sensing Circuit (DSC) is needed for the positive input (replacing the $R_2/C_2$ filter and the buffer in figure 5). The circuit aims at solving twofold issues (figure 16):

- Reject the Common Mode Voltage between acquisition system and voltage divider arising from the ground loop related to separated and far grounds, by means of a suitable difference amplifier (again based on the ADA4898);
- Decouple the voltage divider from the analogue front-end by means of two input buffers (model OPA627).

In figure 17, the amplitude frequency response of the analogue front-end with the DSC assessed in simulation is shown. The cut-off bandwidth is still localized around 5 MHz demonstrating that the DSC does not affect the amplitude frequency response of the analogue front-end. Furthermore, figure 18 shows that the new RMS noise of the front-end is approximately 3.4 ppm RTI.

7 Conclusion and future developments

A low-noise 5 MHz bandwidth analogue front-end based on the concept of flat-top removal has been proposed for fast trapezoidal voltage pulses measurement. During the design, its main features were assessed by Pspice simulations. Experimental tests at CERN, on a proof demonstrator
matching the specifications of a case study for the CLIC project, confirmed the expected performance. In particular, bandwidth, noise, and linearity requirements were shown to be fully satisfactory, whereas the CMRR performance can still be enhanced. An engineered circuit can be equipped easily with precision matched resistors that will improve CMRR and, mostly, overall gain stability.

In the final application for CLIC, the differential sensing of figure 16 is foreseen for the positive input of the analogue front-end. This is aimed at both (i) rejecting the common mode between acquisition system and voltage divider, and (ii) decoupling the voltage divider from the proposed analogue front-end by means of two input buffers (OPA627). Moreover, the PBC [12] will be used as 10-V$_{DC}$ reference generator on the DC channel, which is heavily filtered (bandwidth $\leq 16$ Hz), as discussed in 3.3. However, even if the system’s performance already meets the requirements with the lower quality resistors used in the current prototype, precision matched resistors are going to be used in the final version of the system to improve CMRR.
Figure 18. Simulated RMS noise with differential sensing on positive input.

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