A short circuit protection circuit for SiC MOSFET with self-adjustive blanking time

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Abstract This paper proposed a desaturation (DESAT) short circuit (SC) protection circuit for SiC MOSFET, where a blanking time setting module and an SC detection module are designed. The fall time of the drain-source voltage \(V_{DS}\) for each switching period of SiC MOSFET is recorded and set as the blanking time for the hard switching fault (HSF) detection in the next switching period. Consequently, the detection delay for HSF is self-adjustive and can respond quickly to the operating state of SiC MOSFET. FPGA and discrete components are used to implement the proposed circuit. The function of the proposed circuit is verified using the double pulse test. The experiment results show that the blanking time automatically increases with the increase of load current. The default detection delay of the proposed protection circuit is set 240ns for HSF and can be adjusted during the subsequent switching period. So in the test under a 400V bus voltage, the detection delay is 240ns for HSF at the first switching period. And for HSF occurs at the second switching period, the detection delay is 200ns adjusted according to the operating state of the first switching period. Meanwhile, the detection delay for fault under load (FUL) is 72 ns.

keywords: SiC MOSFET, short-circuit protection, blanking time

Classification: Power devices and circuits

1. Introduction

Compared to silicon(Si), silicon carbide(SiC) has a high electron saturation velocity, wide bandgap, and high thermal conductivity [1,2,3,4,5]. Consequently, SiC MOSFET presents low on-resistance, high switching speed, and high operating temperature [6,7,8,9,10,11,12]. However, at the certain gate bias, the drain current of SiC MOSFET continues to increase with drain voltage \(V_{DS}\), and the transition from the linear region to the saturation region is not sharp [13,14,15]. Moreover, the current density is very high due to the small die size, which leads to its SC withstand time as short as 3us, while it is typically 10us for Si IGBT [16,17]. The commercial gate drivers for SiC MOSFET still use the DESAT protection method at present [18,19,20,21,22,23,24,25], where a blanking time is used to avoid false trigger during switching transients, and it is determined by the blanking capacitor and the DESAT reference voltage. Furthermore, the blanking time is always set a longer time to avoid the false trigger in practical applications.

Compared to IGBT, SiC MOSFET requires a shorter blanking time and a more robust anti-oscillation capability for DESAT method. Various circuit design options are available to enhance the performance of the DESAT method. The paper [26] proposed a desaturation detection circuit with adjustable DESAT reference voltage by adding the extra DESAT diode. The paper [27] utilized digital ICs to generate the easily configurable blanking time for SiC MOSFET gate driver circuit. In [28], a resistor connecting the blanking capacitor and the gate of SiC MOSFET is added to accelerate the charging of the blanking capacitor to reduce the blanking time. In [29], the separated detection paths for HSF and FUL are used to shorten the detection delay of FUL. However, all these DESAT methods encounter the problem of the fixed blanking time, which can not be adjusted dynamically during the switching periods once the system is powered up. In addition, switching oscillation of \(V_{DS}\) may also falsely trigger the detection circuit, especially for FUL detection. So the automatically adjusted blanking time is very attractive for the quick and robust response of the SC protection of SiC MOSFET.

In this paper, a DESAT SC protection circuit for SiC MOSFET is proposed. The blanking time to detect HSF is adjusted automatically with a blanking time setting module and an SC detection module. And the fixed detection delay is provided for the detection of FUL to enhance the oscillation immunity of the SC protection circuit.

2. The blanking time analysis for SiC MOSFET.

During turning on of SiC MOSFET, it takes time for \(V_{DS}\) to fall from bus voltage to on-state voltage. The SC protection circuit should not be triggered during this time. This period is generally referred to as the blanking time [18]. As shown in Fig.1, by analyzing the turn-on process
of SiC MOSFET, the blanking time can be calculated [30]. The blanking time \( TB \) can be expressed as:

\[
TB = t_3
\]

where:

\[
t_3 = t_2 + \frac{R_G C_{GD,sw}}{(V_{CC} - V_{MP})} [V_{BUS} - I_L R_{ON}(V_{MP})]
\]

\[
t_2 = R_G [C_{GS} + C_{GD}] \ln \left( \frac{V_{CC} \mu_n C_{ox} W}{V_{GS} \mu_n C_{ox} W - I_1 V_{TH} \mu_n C_{ox} W} \right)
\]

\[
V_{MP} = V_{TH} + \sqrt{\frac{I_1 V_{CH}}{\mu_n C_{ox} W}}
\]

where \( R_G \) is the gate resistance, \( V_{CC} \) is the power supply voltage of the driver circuit, \( V_{TH} \) is the threshold voltage of SiC MOSFET, \( \mu_n \) is the mobility for electrons, \( C_{ox} \) is the capacitance of the gate oxide, \( L_{CH} \) is the channel length, \( W \) is the channel width, \( I_1 \) is the load current, \( V_{MP} \) is the miller plateau voltage, \( V_{BUS} \) is the bus voltage, \( C_{GD,sw} \) and \( R_{ON}(V_{GD}) \) are the \( C_{GD} \) and \( R_{ON} \) of the SiC MOSFET during the miller plateau, respectively.

The equation (1) to (4) indicate that \( R_G, V_{BUS}, \) and \( I_L \) will affect the blanking time \( TB \). Fig. 2 shows the simulated minimum blanking time needed for SiC MOSFET C2M0040120D [31], and it varies with \( R_G, V_{BUS}, \) and \( I_L \). Therefore, a fixed \( TB \) will increase the SC enduring time to burn out SiC MOSFET or affect the normal turn-on of devices. It is necessary to adjust \( TB \) automatically during the switching of SiC MOSFET.

3. The proposed DESAT SC protect circuit with self-adjustive blanking time

As shown in Fig. 3, the proposed protection circuit mainly includes a blanking time setting module and an SC detection module.

The blanking time setting module sets the appropriate blanking time for the subsequent switching period by monitoring the \( V_{DS} \) fall time of the previous switching period. Moreover, compared to the conventional DESAT circuit, the proposed circuit doesn’t require an external blanking capacitor to set the blanking time.

The input signals of the blanking time setting module are \( V_{IN} \) and \( V_{COMP} \). A comparator monitors the change of \( V_{DS} \). When \( V_{DS} \) is lower than \( V_{REF} - V_{FD} \), \( V_{COMP} \) is pulled down. \( V_{FD} \) is the forward voltage of the high voltage diode. Considering the delay and the anti-interference capability of the detection circuit, here \( V_{REF} \) can be adjusted by changing the value of \( R_1/R_2 \).

\( Data2[8:0] \) is the output signal of this module, reflecting the fall time of \( V_{DS} \) each time the SiC MOSFET is turned on. The voltage fall time refers to the time that \( V_{DS} \) falls from the bus voltage to the preset reference voltage \( V_{REF} - V_{FD} \). According to \( Data2[8:0] \), the SC detection module will read the \( V_{COMP} \) voltage after a corresponding delay time and determine whether \( V_{DS} \) is normally changing. The operating mechanism of the proposed protection circuit will be described in detail as follows.

3.1 Operating mechanism for normal operation

Fig. 4 depicts the structure of the proposed SC protection circuit in detail. When the system powers up, the \( Data1[8:0] \) in register Flag1 is all-zero, and \( Data2[8:0] \) in register Flag2 is all-one. Each time \( V_{IN} \) is pulled up, the Clk_gen module will generate \( N \) rising edges of pulse, and Flag1 will read \( V_{COMP} \) at each rising edge. The time interval \( T_{CLK} \) of each rising edge can be configured to meet different blanking time requirements. \( N \) is the number of bits in Flag1 and Flag2 and is designed to 9.
considering the complexity of the protection circuit. $V_{COMP}$ is pulled down only when $V_{DS}$ falls below $V_{REF} - V_{FD}$. After that, $Data1[8:0]$ in Flag1 records the fall time of $V_{DS}$ at each turn-on transient. And $Data1[8:0]$ is copied to $Data2[8:0]$ at each turn-off transient of the SiC MOSFET. The three D-flip-flops with the consecutive trigger delay time are added to improve the noise immunity of the detection. The delay from $V_{S2}$ to $V_{S3}, V_{S4}, V_{SS}$ is set to $T_{CLK}, 2T_{CLK}, 3T_{CLK}$, respectively.

$Data1[8:0]$ varies with the fall time of $V_{DS}$, as shown in Fig. 5. $Data1[8:0]$ and $Data2[8:0]$ in Fig. 5, Fig. 6, and Fig. 7 depict the working process and don’t represent the real data.

For the first turn-on pulse of the SiC MOSFET, $Data2[8:0]$ is in the initial all-one state and a maximum allowed blanking time is set to $9T_{CLK}$. The blanking time for the subsequent pulse can be expressed as:

$$TB = nT_{CLK} \quad (n \leq 9)$$

where $n$ is the number of bits in $Data2[8:0]$ that are 1.

In the normal switching operations of SiC MOSFET, $V_{S1}$ pulls up at each turn-on transient with a delay of blanking time that $Data2[8:0]$ sets and pulls down at each turn-off transient. When $V_{S1}$ is high, $V_{S2}$ equals to $V_{COMP}$ that is 0 with $V_{DS}$ below $V_{REF} - V_{FD}$. When $V_{S3}, V_{S4}, V_{SS}$ are not pulled up with the delay of $T_{CLK}, 2T_{CLK}, 3T_{CLK}$, respectively. The 0 states of $V_{COMP}, V_{S2}, V_{S3}, V_{S4}, V_{SS}$ set the signal Fault to 0. And Fault is always 0 when the logic input signal $V_{IN}$ is 0, as shown in Fig. 6.

### 3.2 Operating mechanism for HSF operation

The blanking time of the proposed SC protection circuit for HSF is set according to the previous switching period. So for HSF occurs at the first switching period, there is no previous period to reference, and a default maximum blanking time will be set initially. For HSF occurs at other switching periods, the blanking time is adjusted according to the previous switching period. These two different HSF cases are described in detail below.

**Case 1:** HSF occurs at the first switching period for SiC MOSFET, and the operating waves are shown in Fig. 7 (a). At the rising edge of the first pulse, $Data2[8:0]$ remains at the default all-one value, and the detection delay $TB1$ is set to the maximum blanking time $9T_{CLK}$. $V_{COMP}$ keeps high for $V_{DS}$ does not fall below $V_{REF} - V_{FD}, V_{S1}$ pulls up with a delay of $TB1$; after this, $V_{S2}$ pulls up. $V_{S3}, V_{S4}, V_{SS}$ pull up with trigger delay of $T_{CLK}, 2T_{CLK}, 3T_{CLK}$, respectively. The simultaneous pulling up of $V_{COMP}, V_{S2}, V_{S3}, V_{S4}, V_{SS}$ sets the Fault signal to 1. In this case, the detection delay is $12T_{CLK} (9T_{CLK} + 3T_{CLK})$.

**Case 2:** HSF occurs at other switching periods for SiC MOSFET, and the operating waves are shown in Fig. 7 (b). Supposing that HSF occurs at the second switching period, and the detection delay $TB2$ is set to $6T_{CLK} (3T_{CLK} + 3T_{CLK})$ according to the $V_{DS}$ fall time at the first switching period. Consequently, the detection delay is automatically adjusted according to the previous switching period.

### 3.3 Operating mechanism for FUL operation

For the FUL situation, $V_{DS}$ rises rapidly to $V_{BUS}, V_{COMP}$
will be pulled high. Since \( V_S1 \) is already high, \( V_S2 \) pulls up. After that, \( V_S3, V_S4, V_S5 \) pull up, and DFF1, DFF2, DFF3 read the value of \( V_{COMP} \) in turn at each pull-up transient. The Fault is 1 only when the outputs of DFF1, DFF2, DFF3 are simultaneous all 1. This mechanism can effectively cope with the interference of \( V_DS \) oscillation to FUL detection. The detection delay of FUL is \( 3T_{CLK} \), as Fig. 7 (c) shows.

4. Experiment results

The proposed SC protection circuit is verified by FPGA and discrete components, where Cree’s E3M0280090D (A 900V/12A SiC MOSFET) acts as the switching device. As shown in Fig. 8, the test PCB contains three parts: Double pulse power loop, Driving and \( V_DS \) sampling, and FPGA board (EP4CE15-AX415). The driving and \( V_DS \) sampling part is responsible for driving the SiC MOSFET and monitoring the change of its \( V_DS \). FPGA board is responsible for generating the logic driving signal \( V_IN \) and implementing the proposed SC protection function.

Referring to the \( V_DS \) fall time given in the datasheet and the propagation delay of the driving signal, \( T_{CLK} \) set to 20ns is appropriate, and \( T_{CLK} \) can be configured easily by FPGA. Considering \( V_DS \) oscillation, \( V_{REF} \) is set to 12V by adjusting the value of \( R_2/R_1 \), \( R_G \) is set to 4.7\( \Omega \).

4.1 Test results under continuous switching periods

Tests are conducted with gradually increasing load currents. Due to the rated current limitation of the load inductor and SiC MOSFET, the total turn-on time of the SiC MOSFET is set to 12us, and \( V_{BUS} \) is set to 300V in this 8-periods continuous switching test. As seen in Fig. 9, the blanking time (TB) of the first turn-on period is 180ns, equal to the designed \( 9T_{CLK} \). Moreover, the blanking time of subsequent pulses for HSF varies from 120ns to 160ns as the load current increases. It is worth noting that the nonlinearity of load current is caused by the saturation of the power inductor in the power loop.

4.2 Test results under HSF condition

As Fig. 10 (a) and Fig. 10 (b) shown, for HSF occurs at a \( V_{BUS} \) of 400V, the detection delay of the proposed protection circuit is 240ns for the case of HSF occurring at the first switching period, and 200ns for the case of HSF occurring at the second switching period. The HSF detection delay of 240ns at the first turn-on pulse is in line with the designed 12\( T_{CLK} \).
5. Conclusion

This paper presents a self-adjustive blanking time detection circuit for SC protection of SiC MOSFET. With the blanking time setting module and the SC detection module, the proposed circuit monitors the fall time of $V_{DS}$ and sets it as the blanking time for HSF detection that happens at the next switching period. Consequently, the detection delay can be adjusted automatically at each switching period and respond quickly to the operating state of SiC MOSFET. Moreover, the proposed DESAT circuit does not require a blanking capacitor and can be integrated into gate driver IC. The proposed DESAT circuit is verified by FPGA and discrete components. Experiment results show that the blanking time for HSF increases as the load current increases. The default detection delay of the proposed protection circuit is set 240ns for HSF in our test circuit and can be adjusted during the subsequent switching period. Under a 400V $V_{BUS}$, the detection delay for HSF is 240ns when HSF happens at the first switching period and is 200ns for the case of HSF occurring at the second switching period. The detection delay for FUL is 72ns.

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4.3 Test results under FUL condition

For FUL during the first and second switching period, as shown in Fig. 10 (c), the SC detection delays are 72ns when $V_{BUS}$ is 400V, which is slightly larger than the designed 60ns. This additional delay mainly comes from the switching time of the high voltage DESAT diode.

Fig. 10 Test waveforms of the proposed circuit under different SC conditions: (a) HSF occurs at the first period; (b) HSF occurs at the second period; (c) FUL occurs at the first and second periods.
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