A Fully Integrated Dual-Band WLP CMOS Power Amplifier for 802.11n WLAN Applications

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Abstract

A fully integrated dual-band CMOS power amplifier (PA) is developed for 802.11n WLAN applications using wafer-level package (WLP) technology. This paper presents a detailed design for the optimal impedance of dual-band PA (2 GHz/5 GHz PA) output transformers with low loss, which is provided by using 2:2 and 2:1 output transformers for the 2 GHz PA and the 5 GHz PA, respectively. In addition, several design issues in the dual-band PA design using WLP technology are addressed, and a design method is proposed. All considerations for the design of dual-band WLP PA are fully reflected in the design procedure. The 2 GHz WLP CMOS PA produces a saturated power of 26.3 dBm with a peak power-added efficiency (PAE) of 32.9%. The 5 GHz WLP CMOS PA produces a saturated power of 24.7 dBm with a PAE of 22.2%. The PA is tested using an 802.11n signal, which satisfies the stringent error vector magnitude (EVM) and mask requirements. It achieved an EVM of −28 dB at an output power of 19.5 dBm with a PAE of 13.1% at 2.45 GHz and an EVM of −28 dB at an output power of 18.1 dBm with a PAE of 8.9% at 5.8 GHz.

Key Words: CMOS, Integrated Circuit, Power Amplifier, Transformer, WLAN.

1. INTRODUCTION

The rapid development of handheld devices has necessitated the transmission and reception of high data-rate signals. Despite the developments in wireless communication technologies, the design of CMOS power amplifiers (PA) continues to pose challenges in the design of wireless transceivers because of the low breakdown voltage in CMOS devices, the no-substrate via-hole in the CMOS process, and the low quality of the passive components. In addition, in WLAN applications, especially those meeting the IEEE 802.11n standard, a highly linear PA is required because of the high peak-to-average power ratio (PAPR) and the wide data bandwidth signal. Therefore, PAs are required to operate in a large back-off point from the in a saturation power region, resulting in decreased efficiency [1]. Hence, the design of WLAN PAs using CMOS technology is a challenging task.

Current communication standards require that PAs support dual or multi-bands. Therefore, the demand for dual-band PAs has increased. In 802.11n applications, 2 GHz and 5 GHz bands must be supported. In dual-band operation, the design of the output transformer is crucial because it must provide optimal impedance with low loss performance. However, no detailed design for the optimization of dual-band PA (2 GHz/5 GHz PA) output transformers has been reported. In wafer-level package (WLP) technology, an integrated circuit is used as the
wafer level. WLP is essentially a true chip-scale package technology because the resulting package is almost the same size as the die [2]. Because WLP is intrinsically a chip-size package, its primary advantage is its small form factor. Another advantage is its low packaging cost compared to die-level packaging [3]. WLP technology also allows the chip to be reliably attached directly to a printed circuit board (PCB) [4]. However, unlike other packaging methods, it is difficult to design a dual-band PA in a compact die area using WLP technology because there are several limitations in the usage of WLP technology in RF PA designs. Without proper design considerations, the required die area is greatly increased because of the minimum distance rule between the balls and their large diameter. Although a dual-band PA using WLP technology was developed in [5], the considerations and details related to the design of a dual-band PA using WLP technology have not been addressed.

In this work, several design issues in a dual-band PA using WLP technology are addressed and a design method is proposed. In addition, a detailed design for the optimal impedance of dual-band PA (2 GHz/5 GHz PA) output transformers with low loss is presented. In the optimal dual-band operation presented here, the selection of the number of turns in the primary and secondary windings of the output transformers is investigated to provide optimal impedance. We design and implement a fully integrated dual-band CMOS PA for 802.11n applications using WLP technology. The fully integrated 2 GHz CMOS PA exhibits a 19.5-dBm output power and a PAE of 13.1% at the −28 dB error vector magnitude (EVM) point; the 5 GHz CMOS PA achieves an 18.1-dBm output power and a PAE of 8.9% at the −28 dB EVM point.

II. OUTPUT TRANSFORMER DESIGN FOR THE DUAL-BAND CMOS PA

The output transformer is a major component affecting the overall performance of the PA. In designing a highly efficient linear PA, the selection of the optimal impedance is crucial. In the initial design stage, load-pull simulations are typically performed to find the optimal region of the input impedance in the transformers (Z_{IN}). Therefore, an output transformer is required to provide the corresponding optimal impedance region with low loss performance.

Fig. 1(a) depicts the layouts of 1:2 and 2:2 transformers. The equivalent model of a magnetic-coupled transformer is shown in Fig. 1(b). L1 is the net inductance of the primary winding and L2 is the net inductance of the secondary winding. R1 and R2 are the net resistances of the primary and secondary windings, respectively. Considering the effect of the voltage induced through mutual coupling,
Fig. 2. (a) Simulated \( R_{\text{IN}} \) of the 2:2 and 1:2 transformers, (b) simulated minimum insertion loss of the 2:2 and 1:2 transformers.

Fig. 3. (a) 2 GHz PA output transformer with input and output capacitors, (b) 5 GHz PA output transformer with input and output capacitors.

Fig. 4. (a) Simulated minimum insertion loss of the 2-GHz and 5-GHz output transformers, (b) optimum \( Z_{\text{IN}} \) of 2 GHz PA output transformer, (c) optimum \( Z_{\text{IN}} \) of 5 GHz PA output transformer.
spaced at 10-μm intervals. The windings of the 1:2 transformer used in the 5 GHz PA are 15 μm wide and spaced at 5-μm intervals. Typically, for high target frequencies, the optimal size for maximizing passive efficiency is smaller in on-chip transformer designs. Increasing the size of the transformer increases the Q of the transformer at lower frequencies, while it can degrade the Q of the transformer at higher frequencies mainly because of the large coupling between the transformer and the lossy substrate. Therefore, the optimized size of the 5 GHz output transformer is much smaller than that of the 2 GHz output transformer. The size of the 2:2 transformer is 495 μm × 495 μm, whereas that of the 1:2 transformer is 235 μm × 235 μm. Fig. 4(a) shows the minimum insertion loss in the output transformers. With the proper section of transformer size, the peak of the minimum insertion loss is located on the target frequencies. When each transformer is plugged into the power stage circuit, input and output capacitors are added in parallel, as shown in Fig. 3, to provide the optimal performances of not only PAE and output power but also linearity. Through a careful process of the iteration of the total circuit simulation to maximize overall performance, the optimal \( Z_{in} \) of the 2-GHz/5-GHz PA output transformers are selected, as shown in Fig. 4(b) and (c).

III. WLAN DUAL-BAND WLP PA DESIGN

Among the most recent packaging solutions, WLP is the preferred method because the packaging size is small and the required cost is low. Careful considerations are required for a dual-band PA design using WLP technology in order to minimize the required die area. To save the die area, a method placing an active device or passive transformers under the WLP balls can be considered. Placing active devices that operate at low frequency, such as digital circuits, under WLP balls may not cause any difference in performance. However, placing active devices or passive transformers that operate at 2 GHz or 5 GHz frequency ranges causes the performance degradations because of the electric and magnetic coupling between the active devices and the WLP balls. In particular, the passive transformer should be kept outside the area of the balls in order to minimize their impact. Because the increasing distance between the designed transformer and the balls also increases the required die area, the selection of the proper distance is important to save the die area without causing the performance to degrade. Based on EM simulations, a minimum distance of 40-μm between the transformers and balls was chosen in this work.

Fig. 5 shows the schematic of the PAs. Both the 2 GHz and the 5 GHz PAs have differential amplifiers with a cascode structure. To achieve a high gain, the 2 GHz PA has two stages (i.e., the driver stage and the power stage), and the 5 GHz PA has three stages (i.e., driver stage 1, driver stage 2, and the power stage). An adaptive bias circuit is added to improve the EVM performance of the 2 GHz and 5 GHz PAs [9]. Fig. 6(a) shows
Fig. 8. (a) Full EM model for 2-GHz inter-stage including wafer-level package (WLP) balls and routings, (b) full EM model for 2-GHz output stage including WLP balls and routings.

IV. MEASUREMENT RESULTS

The fully integrated 802.11n CMOS PA was fabricated using a standard process of 65 nm CMOS. The size of the chip, including the test pads, was 2.04 mm², as shown in Fig. 7. During the measurement procedure, the losses in the PCB trace were carefully de-embedded, but the pad and bond wire losses were not de-embedded. Fig. 9(a) shows the measured gain and the PAE versus the output power at 2.45 GHz. The input signal was a single-tone continuous wave (CW) at 2.45 GHz. With a 3.3-V supply, the measurement results showed a 27.7 dB power gain. The saturated output power was approximately 26.3 dBm with a 32.9% PAE.

Fig. 9(b) shows the measured EVM and PAE versus the output power at 2.45 GHz using an MCS7 802.11n signal (64-QAM 65 Mbps with a 20-MHz BW and 9.6 dB PAPR). In the 802.11n standard, the specification for EVM is typically required to be below −28 dB. At the −25 dB EVM point, the output power was 20.3 dBm with a 15% PAE. At the −28 dB EVM point, the output power was 19.5 dBm with a 13.1% PAE.
PAE. The measured output spectrum for the 2.45 GHz MCS7 802.11n signal is shown in Fig. 10. The output spectrum satisfied the mask specification at an output power of 19.5 dBm with a −28 dB EVM. Fig. 11(a) shows the measured gain and PAE versus the output power at 5.8 GHz. The input signal was a CW of 5.8 GHz. With a 3.3 V supply, the measured gain was approximately 40 dB. The saturated output power was 24.7 dBm with a 22.2% PAE. Fig. 11(b) shows the measured EVM and PAE versus the output power at 5.8 GHz using an MCS7 802.11n signal (64-QAM 65 Mbps with a 20-MHz BW and 9.6 dB PAPR). At the −25 dB EVM point, the output power was 18.8 dBm with a 9.8% PAE. At the −28 dB EVM point, the output power was 18.1 dBm with an 8.9% PAE. The measured output spectrum for a 5.8 GHz MCS7 802.11n signal is shown in Fig. 12. The output spectrum satisfied the mask specification at an output power of 18.1 dBm with a −28 dB EVM.

Table 1 shows the comparison with a recently reported dual-band 802.11b/g/a CMOS PA. The PAPR of the 802.11n MCS7 in HT20 was 0.5 dB higher than that of the 802.11g or the 802.11a [11]. Therefore, the PA that uses an 802.11n signal should operate more linearly than the PA that uses an 802.11g/a signal. Without applying predistortion, the performance of the implemented 802.11n CMOS PA was comparable to those reported in [5, 10].

V. CONCLUSION

In this work, we developed a fully integrated dual-band CMOS PA for 802.11n WLAN applications using WLP technology. The output transformer structures were investigated and

Table 1. Comparison with recently reported WLAN WLP CMOS PAs

| Ref.   | Technology | WLP  | Signal            | $P_{\text{sat}}$ (dBm) | $P_{\text{out}}$ (dBm) | 2 GHz | 5 GHz | 2 GHz | 5 GHz | 2 GHz | 5 GHz |
|--------|------------|------|-------------------|------------------------|-------------------------|-------|-------|-------|-------|-------|-------|
| [5]    | 45 nm CMOS | Yes  | 802.11b/g/a (54 Mbps) | 29, 26                | 20.8$^*$, 17.3$^*$       | N/A   |
| [10]   | 55 nm CMOS | No   | 802.11 LG54M (54 Mbps) | 27, 26                | 20.8$^*$, 18.4$^*$       | N/A   |
| This work | 65 nm CMOS | Yes  | 802.11n (65 Mbps)   | 26.3, 24.7            | 19.5, 18.1               | 13.1  | 8.9   |

PA = power amplifier, WLP = wafer-level package, EVM = error vector magnitude.

$^*$ With predistortion.
optimized for optimal dual-band operations. A 2:2 output transformer was chosen as the output transformer for the 2 GHz PA, and a 1:2 output transformer was chosen as the output transformer for the 5 GHz PA. The 2 GHz CMOS PA produced a saturated output power of 26.3 dBm with a 32.9% PAE. The 2 GHz PA achieved $-28$ dB EVM at an output power of 19.5 dBm with a 13.1% PAE. It also satisfied the mask requirements without the need to apply predistortion. The 5 GHz CMOS PA produced a saturated output power of 24.7 dBm with a 22.2% PAE. The 5 GHz PA achieved $-28$ dB EVM at an output power of 18.1 dBm with an 8.9% PAE. It also satisfied the mask requirements without the need to apply predistortion.

This work was supported by a 2-year Research Grant of Pusan National University.

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