Exploiting RapidWright in the Automatic Generation of Application-Specific FPGA Overlays

Joel Mandebi Mbongue*, Danielle Tchuinkou Kwadjo*, Christophe Bobda*

*ECE Department, University of Florida, Gainesville FL, USA

Email: jmandebimbongue@ufl.edu, dtchuinkoukwadjo@ufl.edu, cbobda@ece.ufl.edu

Abstract—Overlay architectures implemented on FPGA devices have been proposed as a means to increase FPGA adoption in general-purpose computing. They provide the benefits of software such as flexibility and programmability, thus making it easier to build dedicated compilers. However, existing overlays are generic, resource and power hungry with performance usually an order of magnitude lower than bare metal implementations. As a result, FPGA overlays have been confined to research and some niche applications. In this paper, we introduce Application-Specific FPGA Overlays (AS-Overlays), which can provide bare-metal performance to FPGA overlays, thus opening doors for broader adoption. Our approach is based on the automatic extraction of hardware kernels from data flow applications. Extracted kernels are then leveraged for application-specific generation of hardware accelerators. Reconfiguration of the overlay is done with RapidWright which allows to bypass the HDL design flow. Through prototyping, we demonstrated the viability and relevance of our approach. Experiments show a productivity improvement up to 20× compared to the state of the art FPGA overlays, while achieving over 1.33× higher Fmax than direct FPGA implementation and the possibility of lower resource and power consumption compared to bare metal.

Index Terms—FPGA, Overlay, RapidWright, LLVM, Kernel.

I. INTRODUCTION

Over the past decades, FPGAs have continuously matured and now contain millions of logic gates, thousands of DSP blocks, megabytes of BRAMs, and other types of resources. This development opens doors to unprecedented hardware acceleration in several computing domains such as deep learning, image and scientific processing, and cloud computing. For instance, Xilinx recently released the U250 Alveo card powered by UltraScale+ FPGAs for data center and artificial intelligence acceleration. The U250 gathers four super logic regions each containing approximately 340000 logic elements, 20MB of BRAM, 90MB of UltraRAM, and 3000 DSP slices [1][2]. The Intel Arria 10 in Microsoft Cloud delivers about 1.1 million logic elements, 3036 DSP logics, and 67MB of BRAM [3][4]. Nevertheless, these feature improvements have not translated into widespread use of FPGAs. One reason is that designing for FPGAs remains a challenging endeavour including required hardware expertise and long compilation time, which limits the efficient use of FPGA accelerators to niche disciplines involving highly skilled hardware engineers.

To help addressing that limitation, High Level Synthesis (HLS) have been proposed [5][6]. It focuses on high-level functionality rather than low level implementation. However, the hardware expertise and the prohibitive compilation times (especially placement and routing) still limit productivity and mainstream adoption. The need to make FPGAs more accessible to application developers who are accustomed to software API abstractions and fast development cycles therefore remains.

FPGA overlays have been developed to promote FPGAs to a wider user community and for increased design productivity. In general, overlays use coarse-grained processors, which can be programmed from a function call, in a 2D intercommunication infrastructure that allows parallel processing and data exchange among the processors [7][8][9][10][11]. The software nature of the coarse-grained processors makes it possible to develop efficient compilers for automatic mapping of sequential applications, thus increasing their acceptance in the software community.

Unfortunately, these advantages come at the cost of area and performance, limiting overlays to relatively small to moderate applications. Indeed, FPGA overlays are usually an order of magnitude slower than bare metal implementations, and consume way more resource and power. Because the main purpose of FPGAs is hardware acceleration, overlays have therefore not been able to breakthrough.

In this work, we introduce Application-Specific FPGA Overlays (AS-Overlays), a novel form of FPGA overlays designed for Data Flow Applications. AS-Overlays provide the flexibility of state-of-the-art overlays on one hand and bare metal performance on the other hand. It leverage application specific architectural components for efficient bare metal implementation of functions needed by run-time applications, effectively eliminating the intermediate layers of conventional overlays. We propose an approach for automatic generation of overlay kernels from applications. The proposed approach differs from traditional HLS in that kernels are identified from a set of high-level programming language (HLPL) applications, with no hardware description language (HDL) generation and no usage of domain-specific language (DSL). Specifically, our contribution includes:

1. An application-specific FPGA overlay generation flow for productivity, performance, and power consumption improvement.
2. An automatic identification of application kernels through intermediate representation inspection using the Low Level Virtual Machine (LLVM) [12], a compilation and code instrumentation framework.
In the rest of the paper, section II revisits recent research, section III describes our proposed AS-Overlays design flow, section IV discusses RapidWright features and defines data flow application in the context of this work, section V details kernels mining within applications, section VI discusses systematic hardware generation, section VII presents experimental observations, and section VIII concludes the paper.

II. RELATED WORK

Published work in coarse-grained reconfigurable architectures and FPGA overlays such as [14], [15], [8] are essentially dataflow machines, usually consisting of small arithmetic and logic units, registers, all of which are immersed in a switch-based interconnect structure. The processors are homogeneous and programmable, and not tailored for specific applications. Overlays such as Hoplite [15], FLeXiTASk [7], and Quattor [11] have dedicated optimization, mostly focusing on the interconnect and communication infrastructure. The Hoplite-DSP [16] is the closest to the approach proposed in this work in that it leverages DSP blocks on the FPGA for dedicated implementation. However, Hoplite-DSP is still a generic architecture with homogeneous processing units.

Several research in the literature have discussed solutions for automating the generation of hardware accelerators on FPGAs. Ma et al. [17] proposed a flow relying on presynthesized functions for runtime generation of FPGA accelerators. It nevertheless requires mastering a specific DSL and is not optimized for performance. Ishebabi et al. [18] presented methods for automatic synthesis targeting arrays of multiprocessors on chip using exact formulations such as integer linear programming of answer set programming. However, the search for kernel is done using profiling. In the same line of idea, Koepflinger et al. [19] present a framework for automatic generation of efficient application specific FPGA accelerators. Parallel pattern inputs aim to raise the level of abstraction of programmers in addition to providing purposeful information to the compiler. Their approach nevertheless relies on parallel inputs which do not necessarily reflect how developers would typically implement applications. Other tools such as LegUp [20] and Vivado HLS [5] allow designers to write code in HLPL and then compile to a register transfer level (RTL) design specification. Though Vivado HLS can deliver competitive quality of results (QoR) compared to manual RTL [21], it still incurs design efforts and long compilation time. LegUp provides a built-in profiler to identify computation intensive code regions for acceleration. Applications are then modified to run partially on MIPS CPU and hardware accelerator on FPGA. Runtime communication between CPU and accelerator coupled with potential cache coherency issues might limit performances achievable by the platform. The work of Cong et al. [22] is similar to ours in that they applied graph-based techniques to identify frequent patterns by analyzing graph edit distances. That work nevertheless differs from ours as patterns

are detected for optimized FPGA resource sharing during the binding in behavioral synthesis.

In contrast to the aforementioned research, our AS-Overlays generation flow leverages advanced graph mining techniques to find kernels in applications and builds a library of accelerators that can be combined into an FPGA overlay to improve performance, productivity, and power consumption.

III. DESIGN FLOW

The major limitation of FPGA overlays resides in that they most often feature more resources than what is actually needed, resulting in increased power consumption and performance lost. They are regularly made of several processing elements (PEs) and interconnect. PEs generally contain some registers and a functional unit capable of executing a set of functions, resulting in architectures not optimized for specific tasks. In Figure 1 we propose a Design Flow to build FPGA overlays that can compete with bare metal implementations. Few steps are necessary to produce an AS-Overlay:

1) Specify the application with a HLPL.
2) Inspect the bytecode or intermediate representation (IR) of the application at compile time to extract compute-intensive code sections that we identify as kernels.
3) Optimize kernels to remove unneeded instructions.
4) Manually pre-synthesize basic operations from the IR instruction set using vendor tools: this step is done exactly once, and the synthesized netlists can be reuse in several other applications.
5) Combine the pre-synthesized basic operations according to kernel descriptions to generate hardware circuits.

Figure 1 also illustrates the overall Architecture supporting the proposed design flow. After the identification of kernels, the LLVM Pass generates a new source code equivalent to the input program, in which kernels’ instructions are replaced by hardware calls.

We use LLVM to search for kernels as it allows transparent optimization on applications written in arbitrary HLPL. Each application is parsed with an LLVM Frontend to output an IR. The produced LLVM IR is then converted into data flow graphs ("Overlay Abstract Representation” in Figure 1).
for analysis, and kernels are identified. RapidWright is further leveraged to automatically generate kernel netlists by assembling as in a puzzle, a set of pre-synthesized LLVM IR operations. We use RapidWright because it is designed to quickly stitch together pre-implemented modules with minimal QoR loss. Finally, hardware kernels are embedded within PEs of an arbitrary overlay architecture (“Overlay Concrete Representation” in Figure 1), and Vivado is used to place and route the AS-Overlay. In the Utilization flow, a new optimized C/C++ code alongside the mapping library can now be compiled and run on a SoC. The mapping library is made of a set of functions handling data copy to/from the FPGA, removing the need for hardware expertise. In the rest of the paper, the focus is mainly set on kernel mining and hardware generation.

IV. PRELIMINARY

RapidWright [13] is an open source Java framework from Xilinx Research Labs that provides a bridge to Vivado backend at different compilation stages through design checkpoint (DCP) files. By making available logical/physical netlist data structures and functions, it enables custom netlist manipulation and direct access to logic and routing resources such as lookup tables (LUT), flip-flops (FF) and programmable interconnect points from a Java API (see Figure 2). As opposed to vendor tools that are closed source, we believe the full access to RapidWright internal features and design resources makes it suitable for design flow exploration and the implementation of targeted FPGA solutions.

Data Flow Applications: the data flow concept refers to a way of looking at the execution flow of instructions in an application. It gives a perspective on operations and their interactions. For modeling purposes, we use the data flow graph (DFG) representation in which nodes represent machine operations, internal edges, data flowing between pairs of operations, and external edges, connections with inputs/outputs. We study these applications because they represent the base of calculation in several computing domains such as image and video processing, or deep learning. In the subsequent sections, we will study how kernels are identified and corresponding hardware is generated. In the rest of the paper, we will refer to “data flow applications” as “applications”.

V. KERNEL MINING

This section discusses how compute-intensive code portions are extracted from the IR of applications. We begin with background definitions necessary to understand terminologies, then we detail data structures and the kernel mining algorithm.

A. Background Definitions

Definition 1. A Control Data Flow Graph (CDFG) is a directed graph $G = (V, E, L, l)$, where $V$ represents the set of vertices, $E \subseteq V \times V$ the set of edges, and $L$ the set of labels, with $l : V \cup E \rightarrow L$ being the labeling of vertices and edges. In the context of this work, a graph is a CDFG defined at a basic block (BB) level.

Definition 2. An isomorphism between a graph $G$ and a graph $H$ is a bijective function: $f : V(G) \rightarrow V(H), l_G(u) = l_G(f(u)), \ for \ u \rightarrow V(G)(f(u), f(v)) \in E(H), \ l_G(u, v) = l_G(f(u), f(v)), \ for \ u, v \rightarrow E(G).$ It measures the similarity between $G$ and $H$, and therefore prevents recording multiple instances of the same graph when a function $f$ can be found. A subgraph isomorphism from $G$ to $H$ is an isomorphism from $G$ to subgraph $H$.

Definition 3. Let $G$ be a set of CDFGs. The support is the minimum frequency of appearance of a subgraph $g$ in $G$.

Definition 4. Given a set of CDFGs $G = \{g_i | i = 1..n\}$ and a threshold $\alpha$ (in this case the minimum support value), the kernel mining consists in finding graphs $g$ in $G$, such that $\text{support}(g) \geq \alpha$. Kernels will then represent the set of graphs $g$.

Definition 5. A Depth First Search (DFS) traversal of a graph defines the order in which its edges are visited: that sequence of edges represent the DFS code of the graph.

B. Kernel Mining

Prior to kernel mining, we build a DFG with properties that best capture the input program. Each vertex is labeled with the operation of the instruction it represents, while edges display the order of precedence between operations. The mining algorithm is summarized in Algorithm 1.

In the control-flow kernel mining, a CDFG normally consists of several DFGs. Nevertheless, the labeling is done such that all the DFGs belonging to a BB remain in the same hierarchy (line 24-26), even if no common edge exists between them. Overall, the kernel mining follows several steps among which:

1) Generate candidates using a DFS-based approach (line 2),
2) Prune the candidates to remove infrequent vertices and edges (line 3 to 7),
3) Evaluate the support value to decide whether a candidate is a kernel or not (line 8 to 16).

However, the isomorphism search during candidate pruning is known to be NP-complete [23], and several subgraphs isomorphism techniques as the ones described in [24] and [25] lead to high computation overhead. One way to mitigate that high overhead consists in computing the canonical form of graphs [26]: if the canonical form of two graphs is identical, the graphs are considered isomorphic. We therefore construct...
Algorithm 1: LLVM Pass for Kernel Mining

Input : LLVM IR, minSup
Output: C++ source file

1 Function kernelMining (GS, Fsubgraphs, minSup):
2   sort labels of the vertices and edges in GS by frequency (using DFS code);
3   remove infrequent vertices and edges;
4   relabel the remaining vertices and edges (descending);
5   S1 := all frequent l-edge graphs;
6   sort S1 in DFS lexicographic order;
7   Fsubgraphs := S1;
8   foreach edge e in S1 do
9       init g with e;
10      set g.DS = (b, b ∈ GS, e ∈ E(b));
11      subgraphMining(GS, Fsubgraphs, g);
12      GS := GS - e;
13      if | GS | < minSup then
14         break;
15   end
16 return

17 Function codeInjection (Fsubgraphs):
18   setLines lines;
19   setVariables var;
20   set files;
21   foreach graph in Fsubgraphs do
22      foreach Instruction inst in graph do
23         var := getVariables(inst);
24         files := getFileName(inst);
25         lines := getInstructionLine(inst);
26         injectFunctions();
27      end
28   end
29 return

30 Function generatedDFG (Module M):
31   setGraphs GS;
32   setGraphs Fsubgraphs;
33   foreach Function FF in M do
34      foreach BasicBlock BB in FF do
35         Graph BBgraph;
36         foreach Instruction II in bb do
37            var := getVariables(inst);
38            files := getFileName(inst);
39            lines := getInstructionLine(inst);
40            setLines lines;
41            setVariables var;
42            codeInjection (Fsubgraphs);
43      end
44   end
45 return

" /* Main function defined as a ModulePass */ */
46
47

canonical form of DFS codes as in [27], which the minimum code that can be derived from a graph g. Specifically, the strategy consists in:

(1) Building frequent subgraphs bottom-up, using DFS code as regularized representation.
(2) Eliminating redundancies via minimal canonical DFS code based on lexicographic ordering.

Given that there is a considerable amount of DFS codes, we build a DFS code tree using a lexicographic ordering [27] between DFS codes as follows: A DFS code $a = (a_0, a_1, ..., a_m)$ is parent of DFS code $b = (a_0, a_1, ..., a_m, b)$ and $b$ is child of $a$ if: (1) each node represents DFS code.

(2) The relationships between parents and children conform to the lexicographic ordering. (3) The siblings are consistent with DFS lexicographic order.

The DFS code tree structure is particularly useful in the kernel mining as it allows to make the following two assumptions: (1) If a DFS code $\gamma$ is frequent, then every ancestor of $\gamma$ is frequent. (2) If $\gamma$ is not frequent then every descendant of $\gamma$ is not frequent (line 11).

Finally, the custom C/C++ code is generated by replacing kernels’ instructions by high-level functions for hardware acceleration. Original names of the variables and their location are retrieved by inspecting the debug metadata (line 23 - 27) attached to each instruction in the IR. LLVM uses the DWARF [28] standardized debugging data format like several other compilers and debuggers to support source layer debugging. The metadata provides the relationships between the generated code and the source code of the original program.

Once kernels are actually extracted from an application, there is still a need to undergo a final graph pruning. It consists in selecting operations that can actually be mapped on FPGAs. This pruning follows two main stages: (1) Removing Load/Store: codes initially being written for Von Neumann architectures, LLVM IR introduces a set of load and store instructions that are not needed on FPGA. We therefore only consider operations different from such instructions as illustrated in Figure 3.

(2) Avoiding Conversions: LLVM often inserts casting operations like zext that are not qualified for FPGA acceleration.

We further study dependencies between basic blocks, searching for additional optimization possibilities. We mainly seek to merge kernels displaying dependencies to save resources and reduce the global latency. As example, Figure 4 pictures three kernels spread across basic blocks BB0, BB1, and BB2 (the kernels are encircled with dotted lines). Because of the data dependencies between BB0-BB1 (content of the register $b0$) and BB0-BB2 (content of register $a0$), we generate the more complex kernel illustrated in Figure 5. We insert demuxes for conditional branches and FFs for temporary storage. Instead of having the kernels deployed over three PEs, we can then use a single processing core.

The following section describes how a placed and routed AS-Overlay is obtained from LLVM kernels.

VI. HARDWARE GENERATION OF KERNELS

Initially, the function implemented by a PE in the overlay layout is defined as a black-box. We leverage the pre-implemented design flow of RapidWright [15] to produce netlists from kernels previously identified with LLVM. The first step consists in synthesizing basic operations from LLVM IR out-of-context (OOC) with Vivado to create a library of
Modules. Modules are built OOC to ensure that I/O buffers and global clocks are not inserted into kernel netlists [29]. This stage implies a manual implementation (through HDL or HLS) of operations to combine into kernels by an engineer, with the advantage that this step is done once. In the following stage, an application built on the RapidWright API stitches pre-implemented modules following the LLVM kernel DFG descriptions. The hardware kernels thus generated are returned as design checkpoint files and define the functions to be executed in PEs. Finally, the RapidWright application opens the netlist of the overlay (EDIF or DCP files), browses through the design cells, and reads-in kernel DCPs into PE black-boxes. Figure 6 illustrates AS-Overlays generation steps. From an application, the LLVM tool identifies kernels and generates corresponding DFGs. Each DFG is dumped into a list of vertices and edges. Vertices start with the character v, and are characterized by an identifier and a label denoting the operation. Edges are introduced by a letter e, and are defined with an identifier, the two vertices it connects, and a letter (L for left, and R for right) specifying if the edge gets into the sink vertex through the left or right input. In the next step, a DCP/EDIF containing the layout of the overlay (with the PE functions still being black-boxes) is opened within the RapidWright application, and the generated hardware kernels are successively read-in in PEs, and a new DCP is created for the overlay, this time with each PE implementing a specific function derived from the LLVM kernel mining. Finally, placement and routing are run with Vivado, and a bitstream of the overlay is produced for FPGA deployment. As opposed to the traditional RapidWright pre-implemented flow, which implies synthesizing, placing, and routing modules OOC [13], basic operations from LLVM IR are only synthesized. Undeniably, for accurate Vivado post-routing timing analysis, partition pin constraints must be defined on input ports of OOC modules, with the consequence of attaching pre-implemented modules to specific FPGA regions [29]. Since kernel netlists are automatically generated with RapidWright from DFGs, it is not possible to know in advance what FPGA resources will be used and how they will actually be assembled into hardware kernels. We therefore limit the pre-implementation of LLVM IR operations to the synthesis stage.

A. Datapath Regularization

To reduce overall latency and data management overhead, datapaths must be regularized. Each operation within a kernel comes with its own latency in number of clock cycles. We must therefore ensure that operands arrive at the boundary of each module at the same time to expect correct results. Figure 7a shows an example of graph needing regularization. If we assume that addition and multiplication respectively require 1 and 6 clock cycles, the right operand of vertex ",mul,1" and the left operand of vertex "sub,2" must be delayed by 1 and 7 clock cycles. This task is done by the RapidWright application which inserts FFs on the path as illustrated in Figure 7b. Inserting FFs do not increase overall latency as the number of FFs is the cumulative latency of operations on the datapath.

B. Processing Elements

We do not discuss interconnection topology between PEs as the focus is not on obtaining improved/flexible communication; rather, we emphasize architectural features supporting the automatic generation of hardware kernels. In addition, the proposed AS-Overlay generation flow is designed and well suited for any interconnect topology (mesh, torus, mixed topology, etc [30]) as only the PE processing core will be changed. We therefore look at the minimum architecture set-up that should be embedded in each PE. Figure 8 illustrates the architecture of PEs. To handle kernels of multiple inputs/outputs as shown in Table IV, the I/O buses have parameterizable sizes and are split into 32-bits channels. Inputs and outputs are temporarily stored in I/O queues to avoid data lost in case of multiple clock domains crossing. The control module is configured with the latency of the kernel programmed in the PE, allowing to orchestrate when fetching data from input queues, and when writing results into output queues. The Black-box is the core of the PE as it implements one or multiple kernels derived from LLVM code inspection.

VII. EXPERIMENTAL OBSERVATIONS

A. Evaluation Platform and Setup

For evaluation purposes, designs are implemented on a Xilinx Kintex UltraScale+ FPGA (xcku5p-fvd900-2-i). Hardware generation is conducted with Vivado HLx Editions v2018.2, and RapidWright v2018.2.5-beta allows assembling hardware kernels. We ran Vivado, RapidWright, and the LLVM kernel
mining on a computer equipped with an Intel Core i3-8130U CPU @ 2.20GHz x4 and 8Gb of RAM. We study image processing and matrix-based applications. Though kernels from applications can altogether be deployed on the AS-Overlay, we run applications individually with the purpose of assessing achievable performances, in particular: (1) global latency, (2) Fmax and productivity, (3) resource utilization, and (4) power consumption, when comparing AS-overlays to regular overlays and bare metal implementations. For each application, we design a $3 \times 3$ PE brownfield with the three flavors: (i) **Bare Metal**: functions are implemented in HDL, embedded in PEs for multitasking, and compiled with Vivado. (ii) **Regular Overlay**: Each PE implements an ALU offering a dozen arithmetic and logic operations. The regular overlay is implemented in HDL and also compiled with Vivado. (iii) **AS-Overlay**: Kernels are implemented into PEs using the design flow described in Figure [1].

### B. Evaluation Results

Data are sent to the FPGA through a set of custom C functions as mentioned in the utilization flow of Figure [1]. Execution times recorded in Table I come from placing the bare metal, regular overlay, and AS-Overlay implementations of each application alongside a MicroBlaze CPU with a 300MHz global clock. It shows that AS-Overlays can effectively compete with bare metal implementations in several test cases. The bare metal nevertheless outperforms AS-Overlays on the image smoothing and matrix multiplication because of the additional clock cycles introduced by the RapidWright application.

In fact, to ensure timing closure when integrating kernels within the AS-Overlay fixed sections (PE architecture + interconnect), FFs are injected on the datapath after each operation. Table I also shows that AS-Overlays compute faster that regular overlays when clocked with identical frequency. Figure 9 actually presents about $3 \times$ improved execution time when averaging all the execution times of the tested applications. This performance gain is amplified by the Fmax study as higher clocked circuits can significantly reduce execution times. To carry out Fmax and productivity studies summarized in Table III for each application, we introduced a Phase-Locked Loop generating a 300MHz (requesting higher frequencies like 400MHz or 500MHz returned negative slacks too high in some of the bare metal implementations) clock on each flavor of overlay. The idea was to observe the maximum frequency and how long would the compilation take. As first observation, AS-Overlays can achieve up to $1.47 \times$ improved Fmax compared to regular overlays on tested applications (the AS-Overlay tops at 447MHz while the regular overlay caps at 304MHz). This is caused by general-purpose ALUs of regular overlays that contain several muxes introducing substantial delays on datapaths. On the other hand, bare metal implementations achieved higher Fmax compared to AS-Overlays on outer product and Robert cross filter. It comes down to an observation made in [13]: vendor tools such as Vivado often produce high performance results for small modules of a design. In this case of figure, outer product and Robert cross are respectively a set of independent multiplications, and subtractions followed by comparisons, which gives to bare metal a $1.09 \times$ Fmax advantage over AS-Overlays. That advantage is nevertheless lost on more complex functions such as image smoothing (the AS-Overlay achieved a $1.33 \times$ higher Fmax), which computes the average of adjacent pixels, highlighting the benefits of using the RapidWright pre-implemented flow as smaller modules can be pre-implemented to achieve maximum frequency, and later be assembled with minimal QoR loss. Reported compilation times show that Kernel netlist generation and loading within PE black-boxes with the RapidWright application, outperforms up to $7 \times$ Vivado synthesis both in Regular overlays and bare metal implementations. Table III finally demonstrates that the proposed AS-overlay generation flow can provide up to $20 \times$ productivity improvement over regular overlays on tested benchmarks.

One way to load hardware kernels into PE black-boxes could have been to use the Vivado read_checkpoint TCL command in place of the RapidWright API like we did in the proposed approach. Vivado loading nevertheless outcomes in higher time and memory overhead as shown in Table II. Vivado in TCL mode or with the graphical user interface (GUI) incurs higher time penalty and RAM utilization than doing the same operation from RapidWright. While the RapidWright application uses few hundreds of Megabytes of the RAM on the testing computer, and loads kernels in about 2 seconds, Vivado launched both with the GUI and the command line interface (CLI), uses about a Gigabyte of RAM and requires up to 6.19 seconds to complete loading hardware kernels. This observation justifies why we only use Vivado for the placement

| Matrix Mult | Outer Product | Robert Cross | Smoothing |
|-------------|---------------|--------------|-----------|
| Bare Metal  | Regular Overlay | AS Overlay | Bare Metal  | Regular Overlay | AS Overlay | Bare Metal  | Regular Overlay | AS Overlay |
| Size        | Size          | Size         | Size      | Size          | Size         | Size      | Size          | Size         |
| $8 \times 8$ | $16 \times 16$ | $32 \times 32$ | $64 \times 64$ | $256 \times 256$ | $1024 \times 1024$ | $4096 \times 4096$ | $16384 \times 16384$ | $65536 \times 65536$ |

### Table I

**Execution Time Comparison on 3x3 PE in μs**

| PE | Bare Metal | Regular Overlay | AS Overlay | Bare Metal | Regular Overlay | AS Overlay | Bare Metal | Regular Overlay | AS Overlay |
|----|------------|-----------------|------------|------------|-----------------|------------|------------|-----------------|------------|
| Size | $8 \times 8$ | $16 \times 16$ | $32 \times 32$ | $64 \times 64$ | $256 \times 256$ | $1024 \times 1024$ | $4096 \times 4096$ | $16384 \times 16384$ | $65536 \times 65536$ |

- **Bare Metal**: Functions are implemented in HDL, embedded in PEs for multitasking, and compiled with Vivado.
- **Regular Overlay**: Each PE implements an ALU offering a dozen arithmetic and logic operations. The regular overlay is implemented in HDL and also compiled with Vivado.
- **AS-Overlay**: Kernels are implemented into PEs using the design flow described in Figure [1].

Figure 9. Execution Improvement

![Figure 9](image-url)

![Matrix Multi][Outer Product][Robert Cross][Smoothing]
and routing.

Figure 10 summarizes the utilization of FPGA resources only for the matrix multiplication (because of page limitation, it was not possible to present the same study for each of the tested applications) as an illustration of how the fabric is progressively occupied as the number of PEs is scaled up. In general, the total amount of resources used by AS-Overlays is close to that of the bare metal, and both far below regular overlays. Figure 10c nevertheless displays the same number of DSPs (the purple, red, and yellow lines are superimposed, so only the yellow line is visible) simply because PEs on the three platforms implement only one multiplier using 4 DSP48E2s.

Pre-implementing basic functions from LLVM IR also have the potentiality of reducing resource utilization as illustrated in Figure 10d. Vivado optimizes individual hardware implementation from LLVM IR without BRAM insertion while adding such resources when compiling bare metal and regular

Fig. 11. CLB Spreading

Fig. 12. Power Consumption

overlays, which translates into a higher power consumption after \(8 \times 8\) PEs (see Figure 12): with 10 PEs, the bare metal uses 1344mW while the AS-Overlay consumes 1224mW, about \(1.10 \times\) less power. Figure 10b reports a higher utilization of FFs in AS-Overlays as opposed to bare metal. This is due to FFs insertion during datapath regularization in addition to input, config and output registers from the PE architecture (check Figure 8). While injecting FFs on the datapath as explained in section VI-A do not incur delays in kernel execution, it obviously increases the number of FFs used depending on the structure of kernel DFGs. This is nevertheless a price to pay to ensure the correctness of results produced by hardware kernels.

Ma et al. [17] reported a productivity improvement between \(170 \times\) and \(214 \times\), which unfortunately only accounts synthesis (no details are provided on placement and routing time). Further, they did not discuss data size. Finally, they used benchmarks, a Vivado version, and an FPGA different
from ours, with no information on the characteristics of the machine used for compilation. Similar observations can be made on other works from section [ ] Overall, establishing a fair comparison of results with previous work is particularly challenging because of the impossibility of reproducing identical experimental environments.

VIII. Conclusion

In this paper, we presented an approach aiming the automatic generation of Application-Specific FPGA Overlays for data flow applications capable of providing bare metal performances. The approach extracts kernels from applications at compile time, and automatically builds accelerators tailored for the application needs. Experimental evaluations demonstrated the viability of our approach with significant productivity improvement, power consumption reduction, and lower execution time over regular FPGA overlays. Future work will investigate the replicability feature of RapidWright coupled with LLVM code instrumentation to build more efficient FPGA accelerators.

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| Applications          | Kernel Inputs | Kernel Outputs | LLVM Compilation | LLVM + Kernel Mining |
|-----------------------|---------------|----------------|-------------------|----------------------|
| Matrix Mult           | 3             | 1              | 4.12s             | 4.59s (1.1 × ↓)      |
| Outer Product         | 4             | 1              | 0.048s            | 0.12s (2.5 × ↓)      |
| Robert Cross          | 4             | 1              | 0.15s             | 0.26s (1.6 × ↓)      |
| Smoothing             | 10            | 1              | 0.16s             | 0.26s (1.6 × ↓)      |

TABLE IV KERNEL I/O & COMPILATION TIME COMPARISON