Transient current effect on the dye sensitized solar cells \(I–V\) characterization

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Abstract
A choosing process for the sampling delay in the dye sensitized solar cells \(I–V\) characterization method was established. The presented method is based on the stepwise varying bias voltage technique. The analyses were based on the solar cell transient current impact on the cell \(I–V\) acquisition. This process presents a method to correctly fix the \(I–V\) scan sampling delay concerning the cell settling time to obtain accurate dye sensitized solar cells performance measures. It allows a faster acquisition compared to classical measurement method to avoid the solar cell heating. All tests were performed on a typical TiO\(_2\) natural-dyed solar cell, dedicated to laboratory tests. The cell manufacturing process was also discussed. Measures were operated by a laboratory developed digital acquisition board. The system architecture, as well as its operating algorithm, was presented.

1 | INTRODUCTION

The dye-sensitized solar cells (DSSCs) are one of the promising photovoltaic (PV) devices nowadays [1]. This is due to their simple low-cost production process, their composition flexibility and their clean manufacturing techniques comparing to the conventional Silicon (Si) cells [2–5]. Subsequent to about three decades, researches still incessantly strive to increase the DSSCs efficiency by enhancing its manufacturing process and constituting materials. Hence, these PV devices exist in a very large number of morphologies with several built-up procedures and various assembling materials.

To accurately evaluate the different reported cells occurrence, a unified process for DSSCs current versus voltage \((I–V)\) characterization and performance measures is required. The most used characterization process is built on previous researches and standards [6,7]. Its approach is to setup and apply a stepwise \((\Delta V)\) varying bias voltage supply on the solar cell (SC) to obtain its \(I–V\) characteristics as shown in Figure 1. Where the scan sampling delay \((T_d)\) should be more than four times as long as the cell settling time \((\tau)\) [7]. Usually, a DSSC characteristic capacitance can achieve tenths to tens of mF/cm\(^2\) [8–11]. Accordingly, the \(I–V\) characterization sampling time must be about one to ten seconds, depending on the DSSC morphology, to achieve the cell transient current equilibrium. Though, long-time measures under projected solar simulator irradiation beam provides cell heating which misleads the \(I–V\) characterizations dramatically [8].

This article comes to present an investigation on the DSSC capacitive behaviour and its transient output current. The results are used to implement a practical method that performs accurate DSSC \(I–V\) measurements.

2 | EXPERIMENTAL DETAILS

2.1 | Solar cell preparation

A typical natural DSSC has been made for all this work experiments [12–15]. The cell electrodes are a Fluorine doped Tin Oxide (FTO) Glass Substrates. Their dimensions are 25 mm × 25 mm × 2.2 mm each with an approximately 7 Ω/cm\(^2\) of conductive surface resistivity. 2 g of nanocrystalline titanium dioxide (TiO\(_2\)) nanoparticles powder (P25), purchased from Degussa Chemicals (Hanau, Germany), are used to prepare the cell N-type thin film. The TiO\(_2\) particles are sized of 21 nm and an 80% / 20% anatase / rutile composition. The powder was mixed with 2.5 mL of absolute ethanol solution (>99.5%). Three drops
FIGURE 1  I–V measurement scanning wave considering DSSC high characteristic capacitance. Where “τ” is the cell settling time. “T_m” is the measurement time. “T_d” is the scan sampling delay. “T_hold” is the holding time that considers the setup delay of the system after the solar cell installation.

FIGURE 2 (a) The titanium dioxide paste arrangement on the SC electrode using the doctor blade technique, (b) The final sealed DSSC where the two electrodes were fit together using binder clips.

 FIGURE 3 Illustration of the assembled DSSC where (1) is the shading mask superposed on the cell top electrode, (2) is the dyed TiO_2 nanostructure, (3) is the Triiodide electrolyte, (4) is the Surlyn tapes, (5) is the thin carbon layer, (6) are the electrode glass, (7) are the FTO films on the cell substrates.

The cell dye is a natural juice extracted from the blackberry fruit. The fruitlets have been crashed and mixed with 250 mL of a pure ethanolic solution and the result was then filtered. The Anode substrate was dipped in the mixture to acquire the blackberry color as shown in Figure 2(b) [25–27].

The encapsulated electrolyte, shown in Figure 3, is a few drops of volatile iodide/tri-iodide redox couple solution (Triiodide). The inhouse thickness was maintaining by using two hollow Surlyn tapes (2 x 0.254 mm). This fixes the cells geometric properties regarding the characteristic capacitance along the different manipulations. A shading mask, with 1 cm² of aperture area (-f) was used to set up the cell active area.

DSSCs are known by their high characteristic capacitance. This specification comes from the existence of two charged layers (Helmholtz Layers) in the cell composition as shown in the Figure 3. The use of nanoparticles, such as the TiO_2, increases the internal surface of the porous electrode from 100 to 1000 X greater than the geometric area of the electrode. Hence the surface capacitance of the TiO_2 interface / Dye / electrolyte in the cell becomes of the order of mF/cm². This flaw increases the DSSC settling time, and causes noticeable transient current once the cell is scanned with ΔV varying bias voltage supply [8].

2.2 Test bench

The test bench is presented in the Figure 4(a). The DSSC measures including the I–V characteristics, transient output current and substrate temperature were performed using a laboratory developed digital acquisition board (DAQ) illustrated in Figure 4(b). The system is developed to be suitable for DSSC measuring process. The design is based on a Cortex M4 Microcontroller Unit (MCU) that includes a digital to analog converter (DAC) to generate the scan waves. The two functions f_1(v) and its reverse f_2(v) level-adjust voltages on the force and measurement lines between the MCU DAC and analog to digital converter (ADC) and the SC terminals. They are based on a rapid rail-to-rail junction field effect transistor (JFET) operational amplifiers (OpA) network. The function f_3(i) is based on a high slew rate (17 V/μs) JFET OpA network to adapt the sensing current to the MCU ADC measuring voltage.

The system is connected to the SC with kelvin clips. The test leads presented in the Figure 4(b) are Forcing/Sensing couple terminals termed H1+/H1−, for the cell positive side (HI), and
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FIGURE 4 (a) Photograph of the assembled DSSC installed in the Kelvin clips (System Testbed) underneath the lighting source. (b) The acquisition board architecture. Were “τ” and “θ” sensing wires represent the cell settling time and temperature signals. “V_{off}” and “V(I_{off})” are two potentiometers that allow offset adjustment while the circuit calibration.

The system allows a nearby 20 μV / 0.5 nA of voltage/current scanning resolution. A universal asynchronous receiver transmitter (UART) to universal serial bus (USB) connection is set to connect the board to a personal computer (PC). All the processing is executed upon a supervision graphic user interface (GUI). Besides the DAQ, the test bench covers a PC and a digital oscilloscope (Rigol DS2102A-S) to take the transient I–V measures buffered from the system.

The characterization process was performed using a lab calibrated lighting source with 100 mW/cm² power density. Its irradiance spectrum is given in Figure 5.

The microscopically DSSC observations and measures were taken using an ultra-nano-indenter CSM Instruments optical microscope.

To complete the cell examination, the X-ray diffraction (XRD) pattern of the used sample was recorded, and the test was carried out by means of the Malvern Panalytical diffractometer Empyrean.

Figure 6 shows the system software flow chart. The manipulation routine can be described as follows. After starting the system, the DAQ remains in hold until the DSSC installation in the testbed. Next, the process starts by measuring the SC parameters: Open circuit voltage (V_{OC}) and short circuit current (I_{SC}). During all the measurements, the system acquires the cell temperature variation (Δθ) for featured corrections. Thereafter, the system determines the DSSC settling time by performing a quick transient testing scan, around the “V_{OC}” point.

After fixing “τ”, the manipulator is called to choose the scanning parameters referring to the obtained results on the GUI. These preferred factors, also presented on Figure 1, are the scan sampling delay “T_{d}”, the voltage changing level “ΔV”, the scan direction and the holding time “t_{hold}” between scans. The system validates the selected parameters if the total measuring time does not exceed 1 min. Afterward, the I–V characterization could be launched, and all results are stored, analysed and displayed within the GUI.

3 | RESULTS AND DISCUSSIONS

3.1 | The DSSC electrode verification

The DSSC thin film XRD (X-ray Diffraction) patterns are given in Figure 7. The characteristics shows the crystalline peaks of both anatase and rutile TiO₂ structure in the 500 °C annealed
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**FIGURE 6** The experiment software flowchart

**FIGURE 7** The thin film TiO$_2$ XRD patterns annealed at 500 $^\circ$C. Anatase crystalline peaks are on 25.39$^\circ$, 36.15$^\circ$, 48.1$^\circ$, 53.98$^\circ$ and 55.13$^\circ$ of 2$\theta$ values. TiO$_2$ rutile structure peaks appear on 30.28$^\circ$, 68.83$^\circ$ and 70.34$^\circ$. Peaks at 27.49$^\circ$, 37.9$^\circ$, 62.84$^\circ$ and 75.12$^\circ$ represent the SnO$_2$ crystalline structure of the conductive glass substrate. The estimated TiO$_2$ particles size is 13 nm using the Scherrer equation [21].

**FIGURE 8** (a) Structure of the TiO$_2$ thin film at ×800 zoom ratio, (b) Ultra Nanoindenter images of the cell TiO$_2$ thin film layer thickness

**FIGURE 9** Transient DSSC photocurrent signal capture after the scanning voltage wave application around “$V_{OC}$” point

3.2 | The DSSC $I$–$V$ characterization results and discussions

Figure 9 was acquired using the digital oscilloscope. It presents the DSSC transient current wave around the $V_{OC}$ point in a substrate. Anatase crystalline peaks are on 25.39$^\circ$, 36.15$^\circ$, 48.1$^\circ$, 53.98$^\circ$ and 55.13$^\circ$ of 2$\theta$ values. TiO$_2$ rutile structure peaks appear on 30.28$^\circ$, 68.83$^\circ$ and 70.34$^\circ$. Peaks at 27.49$^\circ$, 37.9$^\circ$, 62.84$^\circ$ and 75.12$^\circ$ represent the SnO$_2$ crystalline structure of the conductive glass substrate. The estimated TiO$_2$ particles size is 13 nm using the Scherrer equation [21].

Figure 8(a) shows the TiO$_2$ thin film structure. The DSSC electrode optical observations, presented on Figure 8(b), was used to estimate the TiO$_2$ thin-film thickness. The measure is about 35 µm [18].
direct scan with 200 ms of sampling delay. The DSSC settling time of the overshoot current was estimated using the DAQ and validated by the graphic reading to 50 ms. Therefore, the transient current settling time can reach several seconds. Hence, performing measures under the transient photocurrent equilibrium makes the scan sweep time reach several minutes. This produces an immense DSSC temperature variation due to the illumination. Consequently, an appropriate sampling delay is needed.

Previous researches show that using the average values of the both sweep direction could strongly minimize the total scan time \([8]\). The main manipulation in this work consists in making \(I–V\) sweepings in both directions, direct and reverse. Every sweeping was made with a defined speed, related to the DSSC settling time, to obtain the point from where the tests can be considered as accurate.

The cell characteristic in Figure 10 shows multiple current density versus voltage \(\langle I–V \rangle\) scans under several sampling delays, where the values are according to the DSSC settling time (50 ms) and their values are \([\tau; (200 \text{ ms})]; \tau (100 \text{ ms}); \tau (50 \text{ ms}); \frac{1}{2}\tau (25 \text{ ms}); \frac{1}{2}\tau (10 \text{ ms}); \frac{1}{10}\tau (5 \text{ ms})\}. Measures were carried from \(-0.2 \text{ to } +0.7 \text{ V}\) for the direct scan, and vice versa for the reverse one.

A noticeable dependence between the measures and the scan sampling delay and sweeping direction is obviously shown in the curves.

The measured cell performances are presented in Table 1. Results are given for both scan directions: Direct (D) and Reverse (R). The SC short circuit current–density \(J_{SC}\) and efficiency \(\eta\) values are calculated using the Equations (1) and (2) \([17, 28]\).

\[
J_{SC} (\text{mA/cm}^2) = \frac{I_{SC}}{A} \tag{1}
\]

Where “\(I_{SC}\)” is the DSSC Short Circuit Current in “mA” and “\(A\)” is the cell active area in “cm²” \([29]\).

\[
\eta (\%) = \frac{P_{max}}{E_{tot}} \times 100 \tag{2}
\]

Where “\(P_{max}\)” is the DSSC maximum recorded power value in “mW” and “\(E_{tot}\)” is fixed by the lighting source at 100 mW/cm².

The results show the DSSC under test response versus the “\(T_d\)” changes. The cell “\(V_{OC}\)” value in the direct sweep

| \(T_d\) | \(J_{SC} [\text{mA/cm}^2]\) | \(V_{OC} [\text{V}]\) | \(P_{max} [\text{mW}]\) | \(\eta [\%]\) | \(\varepsilon [\%]\) | \(\eta_{avg} [\%]\) | \(\varepsilon_{avg} [\%]\) | \(\Delta\theta [\degree C]\) |
|---------|------------------|--------|--------------------|--------|--------|--------|--------|--------|
| 4 \(\tau\) | D 0.878 | 0.513 | 0.288 | 0.30 | – | 0.30 | – | + 4.3 |
| R 0.879 | 0.515 | 0.299 | 0.30 |
| 2 \(\tau\) | D 0.875 | 0.513 | 0.269 | 0.27 | 10.0 | 0.30 | 00.0 | +2.5 |
| R 0.879 | 0.518 | 0.328 | 0.32 | 06.7 |
| \(\tau\) | D 0.872 | 0.512 | 0.249 | 0.25 | 16.7 | 0.31 | 01.7 | +1.6 |
| R 0.880 | 0.520 | 0.357 | 0.36 | 02.0 |
| \(\frac{1}{2}\frac{\tau}{\tau}\) | D 0.867 | 0.508 | 0.225 | 0.22 | 26.7 | 0.32 | 03.3 | +1.3 |
| R 0.882 | 0.525 | 0.398 | 0.40 | 03.3 |
| \(\frac{1}{3}\frac{\tau}{\tau}\) | D 0.866 | 0.504 | 0.196 | 0.20 | 33.3 | 0.35 | 03.5 | +0.8 |
| R 0.897 | 0.534 | 0.503 | 0.50 | 06.7 |
| \(\frac{1}{10}\frac{\tau}{\tau}\) | D 0.865 | 0.501 | 0.169 | 0.17 | 43.3 | 0.42 | 04.0 | +0.3 |
| R 0.910 | 0.546 | 0.671 | 0.67 | 123 |

**Classical method results**\(^2\)

| \(\tau\) | D 0.851 | 0.513 | 0.271 | 0.27 | 10.0 | NA \(^3\) | +15.3 |
| R 0.877 | 0.509 | 0.281 | 0.28 | 06.7 |

\(^1\)These values are estimated.
\(^2\)These results are corrected in relation to the cell temperature.
\(^3\)NA: Not applicable in classical method.
has fallen from 0.513 to 0.501 V meeting the “$T_d$” decrease. Inversely, “$V_{OC}$” has increased from 0.515 to 0.546 V in the reverse scan. Also, the DSSC short-current density “$J_{SC}$” value has decreased in direct scan from 0.878 to 0.865 mA/cm² and increased in the reverse scan from 0.879 to 0.910 mA/cm².

The DSSC efficiency relative error ($\varepsilon$) is calculated using the Equation (3), where the cell efficiency ($\eta$) at “$T_d$” is considered as the accurate “$\eta$” value. “$\eta_{avrg}$” is the direct and reverse efficiencies average calculated using the Equation (4) and its relative error is extracted from the Equation (5) [30].

$$\varepsilon_{avrg} = \frac{|\eta_{avrg}(T_d) - \eta_{avrg}(T_R)|}{\eta_{avrg}(T_R)} \times 100$$  (3)

$$\eta_{avrg} (%) = \frac{\eta(D) + \eta(R)}{2}$$  (4)

$$\varepsilon(r) = \frac{\eta(T_d) - \eta(40)}{\eta(40)} \times 100$$  (5)

Unlike in the new proposed approach, $\eta_{avrg}$ and $\varepsilon_{avrg}$ are not calculated for the classical method because it does not use averaging between direct and reverse scanning values. It takes only one scan direction into consideration [7].

Observing the DSSC performances, the cell efficiency has changed dramatically vis-à-vis the scan speed variation. Results show an efficiency decrease in the direct scan from 0.30%, which is considered as the accurate value, to 0.17% when “$T_d$” vary from “4.$\tau$” to “$1.6$.10$” value. Differently, “$\eta$” has increased from 0.30% to 0.67% in reverse scan. It is important to mention that the reverse measures presented at 5 ms are estimated; otherwise, the last value of real measure in reverse sweeping is $\eta = 0.50 \%$, which is taken for 10 ms as sampling delay.

Figure 11 shows the variation of the cell efficiency after averaging the both directions values for each $T_d$ value. It shows also the related relative error regarding the considered correct efficiency $\eta = 0.30 \%$. Results shows that measures are considered highly faulty if the sampling delay is shorter than “$1.\tau$”, which gives 1.7 % of relative error. Hence, choosing a “$T_d$” value over “$1.\tau$” rate (50 ms) gives accurate performances results after averaging the two sweeps measures.

As it was mentioned in the introduction. The classic $I$–$V$ characterization sampling delay must be about one to ten seconds. Although, increasing the sampling delay increase the DSSC temperature variation as shown in Table 1. The temperature variation of the dye solar cell in the classical method has reached +15.3 °C. The Standard Testing Conditions (STC) necessitate that measurement must be done under ±1 °C of cell temperature variation ($\Delta \theta$). Getting much deviation make the $I$–$V$ characteristics susceptible to many errors and further corrections are needed [31–33]. Also, the classical method results for cell performances present a high relative error, 10% in direct scan mode and 6.7% in the reverse one. These values are relatively high comparing to the new method results which use a fast scan averaging procedure.

Considering the obtained results, the eventual measurement sampling delay is “$1.\tau$” because it gives a reasonably temperature variation $\Delta \theta = +1.6$ °C and its measures relative error after averaging is relatively low (1.7%). Increasing “$T_d$” more than “$1.\tau$” risks to heat the cell more than +2 °C which is wide out of the STC requirement. Due to the numerous morphologies of this SCs, researches show that the DSSC dependence regarding the temperature variation is bound to the materials and the used techniques for its manufacturing [33–36]. However, our approach of “$T_d$” value choice remains valid, slightly exceeding beyond the “$1.\tau$” value is desirable only if the DSSC did not undergo a temperature variation remarkably superior to $|\Delta \theta| = +1$ °C. Otherwise, a data correction must be applied to the measures. This process guarantees that the calculated performances translate correctly the real case of the cell [33].

4 | CONCLUSION

This study presented a practical and generic solution to perform accurate electrical characterization for DSSC with high characteristic capacitance. The analyses were based on the scan sampling delay impact on the cell $I$–$V$ acquisition. The examination has shown that the influence of the cell capacitance on the performances measures can be overcome if the results are given by averaging a double direction sweep measures. This hypothesis was effective with 1.7% of performance measuring accuracy if the sampling delay is equal to the cell settling time. Measures can be considered more accurate if the sampling delay passes this minimal value once the cell temperature variation does not get more than +1 °C. Otherwise, a data correction will be needed.

Unlike the classic method where the sampling delay is over one second, this method allows faster scan to avoid the solar cell heating. However, the conventional method gave an error of 6.70% at least and 15.3 °C of cell total heating. When the proposed process was more accurate with only +1.6 °C of cell temperature rise.
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