A Learned Performance Model for the Tensor Processing Unit

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Abstract

Accurate hardware performance models are critical to efficient code generation. They can be used by compilers to make heuristic decisions, by superoptimizers as an minimization objective, or by autotuners to find an optimal configuration of a specific program. However, they are difficult to develop because contemporary processors are complex, and the recent proliferation of deep learning accelerators has increased the development burden. We demonstrate a method of learning performance models from a corpus of tensor computation graph programs for the Tensor Processing Unit (TPU). We train a neural network over kernel-level sub-graphs from the corpus and find that the learned model is competitive to a heavily-optimized analytical cost model used in the production XLA compiler.

1 Introduction

Performance models are used in compiler optimizations [18,11], reinforcement learning [20], and Neural Architecture Search (NAS) [8,9,13]. A performance model is particularly useful for compiler optimizations because collecting performance numbers (e.g., execution time) from a real machine can be expensive or infeasible, such as during ahead-of-time compilation when we have no access to the target hardware. For example, LLVM’s loop vectorizer uses a performance model to compute the optimal vectorization and unroll factors [18]. GCC’s auto-vectorizer uses a performance model to decide when to apply loop-peeling, loop-versioning, outer-loop vectorization, and intra-iteration vectorization [11]. In addition, a performance model can be used by a compiler autotuner as a faster alternative to evaluate candidate configurations in a search space [15,16,21].

It is challenging and time-consuming to develop an accurate analytical performance model to predict program performance metrics, such as the execution time, on a modern processor. Program performance is tightly coupled with the underlying complex processor architecture as well as the performance-affecting decisions that are made during compilation [3]. However, a performance model often lacks an in-depth view of the processor architecture and low-level generated code. The recent proliferation of deep learning accelerators has only exacerbated this problem as it demands rapid, repeated development of performance models targeting new accelerators.

∗Work done at Google Research.

2 An autotuner automatically searches a space of configurations of a program, and selects the best-performing configuration according to a performance metric, such as execution time, throughput, or power consumption.
In this paper, we propose to automatically learn a performance model to predict execution time of tensor programs on a Tensor Processing Unit (TPU), an accelerator for machine learning workloads [17]. Similar to prior work [2,5,19], we formulate the runtime estimation problem as a regression task. Our approach extracts features directly from an unmodified program representation, minimizing manual effort to develop; in contrast, Halide’s learned performance model requires additional performance counters generated from a static analyzer [2]. Note that tensor programs contain complex, multi-level nested loops, whose runtimes are harder to predict than those of loop-free instruction sequences, such as those tackled by Ithemal [19]. To represent a tensor program naturally and generalize the performance model to unseen programs, we use a graph-based neural network. We show that our model generalizes relatively well to unseen tensor kernels and is retargetable to different optimization tasks.

We evaluate our performance model on predicting runtimes for two different tensor compiler optimization tasks — operator fusion and tile size selection — on a TPU. The trained performance model is applied to evaluate program configurations generated by an autotuner for the Accelerated Linear Algebra (XLA) compiler [23], in replacement of the real hardware, as depicted in Fig. 1.

In summary, this paper presents the following contributions:

- We develop the first learned performance model for tensor programs, which contain multi-level nested loops, that (1) is generalized to unseen programs, (2) is retargetable for different compiler optimization tasks, and (3) does not rely on any additional static analysis.
- We show better generalization results using a graph neural network. The test accuracy on the fusion optimization task is 13% and 10% better than a sequential model’s and the hand-tuned analytical model built into the compiler’s respectively.
- We integrate our learned performance model into an XLA fusion autotuner, and demonstrate that when access to real hardware accelerators is limited, the performance model helps the autotuner discover fusion configs that are up to 19% faster than the default configs.

2 Related Work

Ithemal uses a hierarchical recurrent neural network to estimate the throughput of x86-64 basic blocks running on highly complex processors [19]. Basic blocks are relatively short, loop-free sequences of instructions (6.06 instructions on average). In contrast, our work addresses larger machine learning kernels with implicit nested loops (which are represented naturally as graphs), containing up to a thousand operators. Ithemal was evaluated on its ability to generalize to held-out basic blocks. However, our method is tested for its ability to generalize to wholly novel tensor programs and targeting a drastically different processor.

Both the code-feature-based performance model [7] and Halide’s performance model [2] use simple neural nets to predict runtime from manually-engineered features produced by a static analyzer that examines an optimized program. Since extracting these features from an XLA graph is non-trivial,
we train a more complex neural net, using features that can be extracted directly from the XLA graph, with sufficient capacity to recover similarly powerful representations.

AutoTVM also uses a learned performance model to optimize tensor kernels, by ranking candidates [5]. However, AutoTVM’s model shows limited ability to generalize between kernels and is trained for per-kernel search over a kernel-specific set of parameters. In contrast, our model can be used to both estimate the runtime of an entire tensor program and rank configuration candidates per kernel, and our model generalizes to novel kernels and applications.

Additionally, approaches to NAS often employ a closely related idea, learning models to predict the error or error curve of an deep learning model architecture [6, 14, 24]. Others, such as ReNAS [25], learn to rank sets of candidate neural architectures rather than predict runtimes in isolation.

3 Target Tasks and Hardware

Our goal is to predict runtime of XLA programs on a TPU. XLA — a machine learning compiler for multiple hardware targets — is used as a backend for various machine learning programming frameworks, including TensorFlow [1], PyTorch [22], and JAX [10]. An XLA program consists of basic blocks, called computations; loop bodies and conditions in a computation are represented as pointers to other computations. Each computation is represented by a directed acyclic graph called a computation graph. A node in a computation graph represents a tensor operation, processing one or more input tensors into a single output. An edge connects an output tensor from one node to an input tensor of another node. In this paper, we apply a performance model to two specific optimization tasks — operator fusion (program-level) and tile-size selection (kernel-level) — for XLA programs running on the TPU v2.

3.1 Operator Fusion

Operator fusion is an important program-level optimization that merges multiple operations into a single unit. Before this pass, a node in a computation graph is a single primitive tensor operation (e.g. convolution, element-wise add, etc). When two producer-consumer ops are fused, the intermediate data is immediately consumed by the consumer, without the need to perform read and write transactions with main memory, thereby reducing data communication. After the fusion pass, a node in a computation graph is either a single primitive op or a fused op with many primitive ops. In this paper, we call a node in an optimized computation graph a kernel, as illustrated in Fig. 2.

We have developed a fusion autotuner that searches for the fastest fusion configuration of an XLA program. It has found up to 15% speedup on some production deep learning models, but the autotuning process is slow, with most of its time spent compiling and executing programs on the TPU. The search space is also extremely large, containing up to $2^{40,000}$ configuration candidates, so we need a fast mechanism to evaluate as many candidates as possible within a time budget. Therefore, we propose using a learned performance model to reduce evaluation time on real hardware. Currently, there is no manual performance model built for this task in XLA.

3.2 Tile-Size Selection

Tile-size selection is a performance-critical, kernel-level optimization. The goal is to select an optimal tile size for a kernel’s output tensor that fits in the fast scratchpad memory; one tile is computed at a time and copied to the slower main memory before the next tile is computed. The number of valid tile sizes ranges from two to 500,000 depending on the kernel. XLA selects the tile size based on a manually-written analytical performance model. This model is extremely complex, taking several person-years to develop. Ultimately, we would like to replace this manual performance model with the learned performance model, demonstrating a new, less costly way of developing compilers.

3.3 Hardware Accelerator

Our performance model is developed for the TPU, a fast, energy-efficient deep learning accelerator. Its architecture is in some ways simpler and in others more complex than modern general-purpose processors like x86. It has no out-of-order execution, hardware caching, or virtual memory. However, it incorporates a VLIW instruction set, 2D registers, a matrix multiplication unit, and a cross-lane
Figure 2: Optimized XLA graph, in which each node (called kernel) in turn contains a graph of primitive op(s).

unit. This TPU does not support multi-threading; one kernel is executed at a time, reading from and writing to main memory at start and termination respectively. Thus, we can compute the total runtime of an entire program by summing the runtimes of its kernel executions. This approach of estimating the total program runtime from kernels’ runtimes can be applied to many accelerators; prior work has shown that this technique is sufficiently accurate for graph rewrites \cite{15} and parallelization configurations autotuning \cite{16, 21} on GPUs.

4 Method

Our approach first decomposes a XLA program into kernels and formulates the kernel runtime estimation problem as a regression task. We can then compute the program’s total runtime by summing the kernel runtimes. This approach confers two benefits. First, this simple decomposition remains general enough that we can apply the neural network model to various tasks, including both whole-program optimizations and kernel-level optimizations. Second, it introduces a restriction consistent with how a compiler transforms a high-level program into a set of optimized kernels, reducing the size of the graphs for which our model will be trained to produce embeddings by orders of magnitude, therefore improving the sample-parameter ratio and at no cost. This improves our model’s ability to generalize to unseen programs.

The rest of this section focuses on our neural network model that predicts the execution time of each individual kernel. For the purpose of predicting cost, we represent a kernel as a directed graph with nodes corresponding to primitive operations.

4.1 Model Architecture

Figure 3 depicts the architecture of our performance model for predicting the execution time ($y'$) of a kernel. Inputs to the model are opcodes ($x^o$), non-opcode features of the ops ($X^f$), and a directed adjacency matrix ($A$) that captures the connections of ops in the kernel. A row of $X^f$ includes attributes extracted from an XLA program representation, such as an output tensor shape, tensor layout, striding, padding, tile size, and where applicable, convolution filter size. Kernel inputs are expressed by nodes with the parameter opcode, and outputs are expressed via an extra feature associated with the output nodes. The opcode ($x^o_i$) of an operation $i$ is embedded into a vector of floats via a simple embedding lookup table. An op’s features occupy a fixed region of the $X^f_i$ vector.

**Neighborhood Embedding** We use a single feedforward layer $f_1$ followed by GraphSAGE \cite{12} (without edge sampling) to combine information from the opcode, the op’s features, and the graph structure to generate the node’s embedding. The embedding of node $i$ considering $k$-hop neighbors can be computed as follows:

$$
\varepsilon^k_i = l_2\left(f^k_3\left(\text{concat}\left(\varepsilon^{k-1}_i, \sum_{j \in \text{neighbors}(i)} f^k_2(\varepsilon^{k-1}_j)\right)\right)\right)
$$

when $k > 0$; $\varepsilon^0_i = f_1(X_i)$ (1)

where $f^k_{2, 3}$ denote feedforward layers specific to depth $k$. $l_2$ denotes L2 normalization. neighbors$(i)$ is a set of immediate neighbors of node $i$. $\sum$ is a reduction chosen during hyperparameter search.
We employ GraphSAGE because (i) a tensor computation kernel is naturally represented as a graph, and (ii) learning node representations conditioned only on their own features and local neighborhoods has shown to improve generalization. In our setting, we expect the effect of most ops to be determined by their own properties and nearby ops’. These are the sorts of features that can be learned from neighborhood, so our choice of model encourages an inductive bias toward mostly local contributions.

**Kernel Embedding** Once we have node embeddings $\epsilon^k$, we create the embedding ($\kappa$) of the kernel by computing sum, mean, and max over rows of $\epsilon^k$. Then, we pass $\kappa$, the concatenation of a combination of the sum, mean, and max vectors into the final feedforward layer (without activation), to produce the estimated execution time ($y'$) of the kernel; the exact combination of sum, mean, and max vectors is tuned via hyperparameter search.

### 4.2 Objectives & Training

**Shared Architecture** For both fusion and tile-size selection tasks, we use the same neural net model architecture and node features $X^f_i$, which include a tile size feature of the kernel the node belongs to. We represent the tile size feature as a fixed-length sub-vector, in which elements are the sizes of a tile from minor to major dimensions, ending with their sum and product; including the product of all dimensions’ sizes is crucial as it represents the volume of the tensor.

**Fusion Task** In this task, we would like the neural network to predict kernel runtimes in an absolute unit (nanoseconds) so that we can use the predictions to compute total program runtime. Thus, we train the neutral network model using the common squared error loss, $(y'_i - y_i)^2$, against log-transformed targets. We apply log transformation because targets vary widely, ranging from a nanosecond to a second. Using this loss function, our model is biased towards fitting long-running kernels more than short-running kernels. This is desirable because small kernels do not contribute much to overall program runtime.

**Tile-Size Selection Task** In this task, we are interested in the relative speed between different tile sizes within each kernel. Therefore, the performance model does not need to predict runtime, but instead should be able to rank tile sizes by speed within each kernel. With this intuition, we train the model with a pairwise rank loss [4]:

$$L = \sum_{i=1}^n \sum_{j=1}^n \phi(y'_i - y'_j) \cdot pos(y_i - y_j) \cdot \frac{n \cdot (n - 1)/2}{n \cdot (n - 1)/2}$$

where $n$ is the number of samples in each batch; $pos(z)$ is 1 if $z > 0$, or 0 otherwise; $\phi(z)$ is either the hinge function $(1 - z)_+$ or logistic function $\log(1 + e^{-z})$, tuned via hyperparameter search. With this loss function, we modify our batching mechanism by grouping samples of different tile sizes of the same kernel into the same batch.

Alternatively, we can use the same MSE loss as in the fusion task, but weight a loss value of each sample appropriately so that the model is optimized for all kernels equally.

### 5 Dataset

Our dataset consists of computation graphs from 104 XLA programs that implement either production models or common models used in research.

**Fusion Dataset** We run our fusion autotuner with a random search strategy to generate 50,000 fusion configurations or until timeout (four hours using 50 machines) for each input computation graph. The graphs are then decomposed according to these fusion configurations, yielding 207 million fused kernels (examples) after duplicate elimination. We observe that program runtimes differ by no more than 4% between runs on the TPU. To improve stability, we execute each kernel 3 times, then interpret the minimum runtime as our targets. Examples in this dataset are heavily skewed. Approximately half have runtimes below $5\mu s$, but they contribute little to total program runtimes, so the kernels that take at least $5\mu s$ are of more interest.
Table 1: The number of unique programs and kernels in the fusion and tile-size datasets. M = million.

| Split   | Manual Split Programs | Kernels Fusion | Tile-Size | Random Split Programs | Kernels Fusion | Tile-Size |
|---------|-----------------------|----------------|-----------|-----------------------|----------------|-----------|
|         | Fusion Tile-Size      | Fusion Tile-Size | Fusion Tile-Size | Fusion Tile-Size | Fusion Tile-Size | Fusion Tile-Size |
| Train   | 79 92 198.6M 23.0M    | 78 93 157.5M 21.8M |
| Val.    | 6 6 2.6M .8M         | 8 8 30.1M 1.6M   |
| Test    | 6 6 6.1M .5M         | 8 8 20.3M 1.4M   |

**Tile-Size Dataset** We compile each XLA program using the compiler’s default fusion heuristics, obtaining an optimized computation graph that we decompose into kernels. For each kernel, we query the compiler for a list of valid tile sizes. The target for each kernel/tile-size pair (example) is the minimum runtime from three runs. A kernel may have as many as 500,000 valid tile sizes, so we measure runtimes for as many as possible for each kernel within 30 minutes across 50 machines.

**Dataset Splitting** We estimate our approach’s ability to generalize in two ways, corresponding to two separate test splits: one split where held-out test programs were chosen randomly, and another where held-out test programs were manually chosen to minimize their (subjective) similarity to programs in the training set. See Table 1 for relevant statistics.

### 6 Evaluation

In this section, we show that our learned performance model is comparable to the manually-written model used in XLA for TPU: 10% more accurate on the fusion dataset (Section 6.1) while performing slightly worse on the tile-size dataset (Section 6.2). Additionally, we integrated the model into the XLA fusion autotuner, and show that it can help the autotuner discover faster programs when access to real hardware accelerators is limited (Section 6.3).

For all experiments, we trained our models on a single NVidia V100 instance, 96GB of RAM, with 10 CPU cores for data processing. For all the learned models, we did a hyperparameter search (presented in Supplementary Material) and selected the best-performing models on the validation split.

#### 6.1 Fusion Task Accuracy

To understand the accuracy of our proposed performance model, we compare mean absolute percentage error (MAPE) and rank correlation between our model and two baselines. We compare our approach’s ability to generalize to novel programs against both an existing analytical performance model and an LSTM baseline. We run separate experiments, including separate hyperparameter searches, for each dataset split described in Section 5.

**Analytical Baseline** The XLA compiler backend has a mature analytical performance model that estimates the execution time of a kernel on a TPU, as described in Section 3.2. However, this analytical model was not intended for predicting the runtime of an entire computation graph, so estimated costs of different types of kernels (e.g., fused kernels with and without convolutions) are in different scales. Hence, we map the model’s output to an estimated runtime by scaling with a coefficient associated with the kernel’s type. Coefficients are determined by executing each program in the test set on the real hardware target with a default fusion configuration, and dividing the actual total runtime for all kernels of each type by the estimate in its original scale.

**LSTM Baseline** Prior work proposes an LSTM-based performance model for x86 basic blocks [19]. To understand the effect of representing program examples as graphs rather than sequences, we compare our proposed graph neural network to an LSTM trained over topologically sorted sequences of nodes, whose embeddings are the same per-node representations used in our proposed model.

**Results** As seen in Table 2, our model, the LSTM baseline, and the analytical model have median MAPE of 13.9, 26.6, and 23.9 on longer-running kernels when considering the random dataset.

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3The analytical performance model does not support kernels without tile-size options, which account for 1% of kernels in our dataset. We ignore these kernels in our comparisons in Section 6.1.
Table 2: Fusion dataset: Mean absolute percentage error of predicted kernel runtimes for kernels with $\geq 5\mu s$ true runtimes, which account for the majority of total runtime in our programs, on the random-split test set.

| Model          | MAPE Our Model | LSTM  | Analytical | Kendall’s $\tau$ Our Model | LSTM  | Analytical |
|----------------|----------------|-------|------------|-----------------------------|-------|------------|
| ConvDRAW       | 42.6           | 62.3  | 21.6       | 0.65                        | 0.52  | 0.77       |
| WaveRNN        | 8.5            | 29.7  | 322.9      | 0.91                        | 0.73  | 0.70       |
| NMT Model      | 17.0           | 68.9  | 26.3       | 0.91                        | 0.82  | 0.91       |
| SSD            | 24.1           | 49.3  | 55.9       | 0.86                        | 0.70  | 0.76       |
| RNN            | 15.5           | 23.5  | 20.5       | 0.91                        | 0.85  | 0.86       |
| ResNet v1      | 7.2            | 14.4  | 11.5       | 0.91                        | 0.84  | 0.88       |
| ResNet v2      | 6.7            | 14.3  | 13.3       | 0.90                        | 0.83  | 0.86       |
| Translate      | 12.3           | 22.4  | 27.2       | 0.83                        | 0.81  | 0.74       |
| Median         | 13.9           | 26.6  | 23.9       | 0.90                        | 0.81  | 0.81       |

Table 3: Tile-size dataset: Mean Kendall’s $\tau$ between targets and predictions within each kernel, on all applications in the random-split test set.

| Model          | Our Model (Rank Loss) | Our Model (MSE Loss) | Analytical |
|----------------|------------------------|----------------------|------------|
| ConvDRAW       | 0.64                   | 0.66                 | 0.79       |
| WaveRNN        | 0.46                   | 0.56                 | 0.65       |
| NMT Model      | 0.74                   | 0.66                 | 0.81       |
| SSD            | 0.64                   | 0.60                 | 0.77       |
| RNN            | 0.42                   | 0.37                 | 0.55       |
| ResNet v1      | 0.72                   | 0.67                 | 0.73       |
| ResNet v2      | 0.74                   | 0.69                 | 0.73       |
| Translate      | 0.76                   | 0.62                 | 0.92       |
| Median         | 0.68                   | 0.64                 | 0.75       |

6.2 Tile-Size Task Accuracy

In this experiment, we drop the LSTM baseline as it is inferior to the graph-based model for our application domain. We train our model with two different loss functions — MSE and rank loss — as explained in Section 4.2 and compare our model against the same analytical model. In this task, we are interested in only relative runtimes between different tile sizes within each kernel. Thus, we measure the models’ accuracy only on the Kendall correlation, and not MAPE. We compute the correlation between targets and predictions of tile-size runtimes within each kernel, and then compute the average over all kernels in each program. Recall that the analytical model is developed specifically for this task, and we do not need to predict runtime in nanoseconds; as a result, the scaling coefficients used in the fusion task are no longer needed.

Table 3 displays the result on the random dataset split. Our best learned performance model (trained using pairwise rank loss) performs slightly worse than the analytical performance model: .07 lower
correlation; on the harder split: .16 lower correlation. Regarding the loss function, we found that the model trained using the pairwise rank loss performs better than with MSE: .04 and .13 higher correlation on the random and hard splits respectively. This result confirms our intuition that training a model to predict relative speeds is easier than absolute runtimes.

6.3 Fusion Autotuner Integration

We integrate the best learned performance model from Section 6.1 in the XLA fusion autotuner. We modify the autotuner to support evaluating fusion configs by either executing generated kernels on real hardware or estimating their runtimes using the learned model, running prediction on a CPU. The analytical model is not used in this experiment because it cannot estimate runtimes for kernels that do not have tile-size options; kernels that are not fusion, convolution, or data formatting operations.

Experiment Setup. Since our target hardware is in demand and more scarce than CPUs, we aim to minimize the time we use the accelerators during autotuning. Hence, we limit the time to use the accelerators to five minutes in our experiment setup. We run simulated annealing search using the learned performance model (from Section 6.1) for one hour on a CPU. After that, we run as many top fusion configs in the order ranked by the predicted costs on the real hardware within the five-minute time limit. The baseline is the original autotuner, which uses only the real hardware to evaluate fusion configs, running for five minutes. We run the autotuner in two modes: starting the search from (i) a default config and (ii) a random config. A default config is the configuration generated by the default heuristic algorithm in the compiler given a specific program.

In this experiment, we run the autotuner on a set of programs that gain significant speedup from autotuning according to our prior data. Although some programs (Transformer, Char2Feats, and ResNet-parallel) are in our training set, most kernels are not because our training data is not generated from the simulated annealing search starting from a default fusion configuration.

Result. We run the autotuner on each program 20 times and report the best speedup found over the default configuration in Fig. 4a. Using the learned performance model together with the hardware, we are able to discover fusion configurations that are on average 2% faster than using the hardware alone, and they are on average only 1% slower than the best known configurations found when running the autotuner on hardware for four hours. When running simulated annealing starting from a random configuration (Fig. 4b), the benefit from the performance model is even more pronounced. On average, using the performance model led to discovering 8% faster configurations compared to not using the performance model. This result demonstrates that the learned performance model can indeed help generate faster code in practice when an access to a hardware target is limited.

7 Conclusion

We have presented first steps toward learning a performance model for tensor programs. We have found that a model trained on our corpus of research and production models can generalize well to programs with some similarity to our training set, usually matching or improving upon the
performance of the best known analytical baseline for our target hardware, and performs acceptably well on programs which differ substantially. When evaluating on the task for which the analytical model is heavily-optimized (e.g. tile-size selection), our learned model is slightly worse. However, while the learned cost model is less accurate, its requires much less effort to develop. Finally, we demonstrated that the learned cost model can be employed by an autotuner to discover faster tensor programs than using hardware targets alone when hardware access is limited.

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