Microscopy needs for next generation devices characterization in the semiconductor industry

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Abstract. In this paper we present the different imaging based techniques used in the semiconductor industry to support both manufacturing and R&D platforms at STMicroelectronics. Focus is on fully processed devices characterization from large structure (3DI, Imager sensors) to advanced MOS technologies (28-20 nm). Classical SEM and TEM (mainly EFTEM) based techniques are now commonly used to characterize each step of the semiconductor devices’ process flow in terms of morphology and chemical analysis. However to address specific issues, dedicated imaging techniques are currently being investigated. With the “High-k Metal Gate” stack involved in the more advanced MOS devices (28-20 nm), new challenges occur and therefore advanced characterization is mandatory. Some relevant examples are pointed out through (STEM) EELS and EDX experiments. Analysis of stressors mainly used to improve carrier mobility in next generation devices, is also presented with different approaches (NBD, CBED and Dark-field holography). Advanced STEM and AFM based techniques applied to characterize dopants and junction in MOS devices and also in more relaxed structure such as imager sensors is discussed too. Concerning back-end (interconnects) and 3D integration (3DI) issues, focus is on nano-characterization of defects by classical techniques (EFTEM, STEM EELS-EDX) and with dedicated ones still in development. To illustrate this topic some 3D FIB/SEM and E-beam tomography experiments are presented. Examples of microstructure and texture determination in poly-crystalline materials such as copper line by coupling SEM/EBSD and TEM techniques are also shown.

1. Introduction

Scanning and Transmission Electron Microscopy (SEM and TEM) coupled with Focused Ion Beam (FIB) are essential techniques to ensure the process development of future devices in the semiconductor industry. At STMicroelectronics Crolles, these tools are now commonly used to support both Manufacturing (200 mm and 300 mm fabs) and R&D platforms. In this industrial context with fast process evolution, large numbers of sites have to be analyzed with short turn-around-times (TAT) but new and innovative characterization techniques have also to be run up.

Nowadays, physical characterization faces some challenges: on the one hand, analysis of very small scale defects and features with the highest resolution (at nanometer and atomic scales) is required. Furthermore, in parallel with this miniaturization, new smart structures and complex materials are incorporated into devices. Also new transistor architectures that have appeared during the last years extended the classical “Moore” law towards the “More Moore” concept.

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On the other hand, the functional diversification of semiconductor-based devices for derivative applications have also emerged, designed as “More than Moore” approach. In this case, more relaxed structures (like 70x70 µm Through Silicon Via (TSV), copper pillars, objects in 3D chips integration (3DI) scheme, imager sensors or MEMS…) have also to be characterized with dedicated techniques or tools.

2. Down-scaling of CMOS transistors in the “More Moore” approach

Following the “Moore law”, device shrinking has continued for forty years from micrometric nominal dimension to about 40 nm. This was possible without great innovation of the CMOS architecture based on Si/Si0/poly-Si stack. Down-scaling of CMOS transistors for the 32/28 nm node and beyond now needs the introduction of new materials in the devices process’ flow. For instance, concerning MOS gate, the implementation of a High-\(k\) (HK) dielectric with a metal gate (MG) stack is now required for advanced technology. Moreover, atomic mono-layers (known as capping layers in the “gate first” approach) of specific elements are used to tune the metal work function for N and PMOS transistor. Regarding backend (BE) flow, some impurities as aluminium (Al) or cobalt (Co) have to be added in copper (Cu) metal lines to limit electromigration phenomenon in interconnects and therefore ensure reliability of the chips.

So, new challenges have occurred and manufacturing processing have raised a need for development of advanced characterization techniques to address specific issues like HKMG, silicide, dopants profiling, stressors and interconnects characterization as described in the following paragraphs.

2.1. High-\(k\) Metal Gate (HKMG) and silicide characterization

The solution chosen for the 28 nm technology developed at the IBM Fishkill ISDA alliance (in which STMicroelectronics is a partner) is to incorporate: lanthanum (La) for NMOS and aluminium (Al) for PMOS at the metal (TiN)/High-\(k\) (HSiON) interface. The quantitative measurement of the initial La and Al doses (about one monolayer) and their post anneal diffusion observation is crucial for the process development. These analyses thus require atomic resolution which fortunately is available in the TEM Cs corrected microscopes. Figure 1 presents HRSTEM images of a Si/SiON/HSiON/La/TiN (gate) stack before and after 1050° C RTP annealing. The observations were carried out using the MINATEC’s TITAN microscope integrating a Cs probe corrector (CEOS Company). The combination of bright field (BF) STEM image (blue), with dark field (DF) HAADF image (red), highlights the heavy and light elements distribution. It is shown that the annealing process induces diffusion and modification of the bottom SiON/HSiON interface.

![Figure 1](image_url)

Figure 1. HRSTEM images combining HAADF signal (red) with Bright Field detector signal (blue): a) before annealing, b) after 1050°C RTP annealing. (TITAN 200 keV probe Cs corrected at CEA Grenoble-LETI MINATEC).
During the last years, analytical TEM developments (high brightness sources, SDD EDX detectors, fast EELS spectrometers) have drastically improved the STEM spectroscopy techniques. Fast chemical mapping with sub-nanometre resolution is now possible. STMicroelectronics have now a FEI TECNAI-Osiris on Crolles site, which integrates such technical advances: high brightness electron source (XFEG), four SDD windowless EDX detectors giving 0.9 srad collection angle (SuperX), and a Gatan FS1 Enfina EELS spectrometer [1]. Large EELS and EDX spectrum images can now be acquired in a short time using an electron probe with a small diameter (~0.3 nm) and a high beam current (1 nA). Figure 2 presents a STEM HAADF image of a cross section of a 28 nm SRAM bit cell cross section. A STEM-EELS map (top right) obtained using the Osiris TEM at 120 keV, shows the Hf, La and Si elemental distributions at the bottom of a NMOS gate. The lanthanum which was deposited on top of the HfSiON layer is now observed after annealing as distributed near the SiON/HfSiON bottom interface. This lanthanum diffusion creating a dipolar layer at the High-k/SiON interface is beneficial for the optimisation of the NMOS threshold voltage.

As is shown in Figure 2, nickel silicide containing platinum (NiSiPt) is used for the 28 nm technology at gate, source and drain level. Past studies for 40 nm technology have shown anomalous nickel silicide growth [2] can induce electric failure. In order to diminish this effect for advanced technology, the platinum concentration inside the Ni target is increased (10 at % instead of 5 at %). However the effect of this higher Pt concentration on the silicide kinetics formation, the redistribution of dopants and platinum must be studied inside real devices. Figure 3 presents STEM-EDX maps of a 28 nm NMOS transistor showing in particular Ni, Pt and As distributions. The platinum is poorly incorporated inside the Ni silicide, whereas As atoms are rejected at external interfaces. This shows that the annealing steps are not efficient for the Pt incorporation inside the NiSi silicide. Figure 4 now shows STEM EDX maps of a laser annealed NiSi(Pt) layer. In this case, part of the platinum has been incorporated inside the silicide, particularly at grain boundaries. The arsenic is still rejected at the NiSiPt outsides interfaces. This confirms that laser annealing is promising for the 28-20 nm technologies, but other extensive studies will be needed in order to validate this assessment.

Figure 2. STEM HAADF image of a cross section of a 28 nm SRAM bit cell. At the right top a STEM-EELS map presents the Hf, La and Si distributions. (TEM Osiris at 120 keV).

Figure 3. STEM EDX maps of a cross section of a 28 nm NMOS transistor showing mainly Ni, Pt and As distributions. The platinum seems to stay at the NiSi surface. (TEM Osiris at 120 keV).
Knowledge of the dopant (As, P, B) distribution in today’s transistors junctions is necessary to improve their electrical properties. The detection and visualization of those impurities in nanoscale silicon devices has been highlighted by the ITRS\(^2\) as a mandatory and difficult task for the development of future generation devices. Today, few characterization techniques are able to map dopant distribution both with a spatial resolution at the nanometer scale coupled with a high sensitivity.

Conventional transmission electron microscopy, despite atomic resolution, gives a too weak dopant contrast. However phase change contrast (revealed by holography technique) or inelastic interactions (measured in spectroscopy mode) can be exploited and provide alternative solutions. Using holography, it is possible to map the electrically active dopants [3]; however specific specimen preparation (parallel side milling, low amorphisation, no gallium contamination) using Focused Ion Beam (FIB) tool is mandatory to perform resolved electron holography experiments [4]. This technique is not used in our lab anymore since the specimen preparation and the minimum specimen thickness are not compatible with nowadays SRAM transistors size (< 100 nm).

Recent STEM, EELS and EDX spectroscopy developments (high brightness sources [5], new spectrometers, aberrations correctors…) place these techniques as candidates for sub-nanometer characterization of doped areas. However, sensitivity detection limit is obtained at the price of high local electron doses and silicon radiation damages at 200 keV become unavoidable. Those undesirable effects have been experimentally evaluated and it has been shown that they are significantly reduced if the electron probe acceleration is lowered to 120 keV or below [6]. During these studies, the STEM EELS technique, which is compatible with classical FIB lamella preparation, has been optimized on a TECNAI F20, for two-dimensional dopant maps from high density SRAM circuits. Using the Spectrum-Imaging approach [7], the first quantitative maps of arsenic dopant have been demonstrated from a 40 nm device gate length by recording more than 10 000 EEL spectra during an hour [1, 8]. Figure 5 shows that using this approach, arsenic dopant distribution from Source, Drain and Low Doped Drain (LDD) regions is revealed with a spatial resolution close to 2 nm and a dopant sensitivity in the low 10\(^{19}\) at.cm\(^{-3}\) (0.01%). This two-dimensional quantitative dopant map clearly reveals the presence of As inside the poly-silicon gate and local segregations at the gate edges are evidenced. Arsenic concentration profiles may be extracted across the LDD-Channel length to measure the chemical channel length. This kind of information is relevant for process engineering in order to optimize implantation conditions and, in consequence, maximize the devices electrical performances.

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Two-dimensional (non quantitative) arsenic (left) and phosphorous (right) dopant maps acquired from a 40 nm gate length transistor using the STEM EDX spectrum imaging approach (Osiris TEM).

In the past EDX spectroscopy compared to EELS suffered from poor signal level detection. This has recently changed with the introduction of Silicon Drift Detectors (SDD). With the new S/TEM Osiris\(^3\) [9], at STMicroelectronics Crolles, it is now possible to retrieve nanoscale chemical compositional analyses using STEM EDX. Figure 6 presents arsenic and phosphorous dopant maps acquired from a 40 nm transistor with a total of (800 x 400) pixels for a complete acquisition time of 20 minutes. Arsenic and phosphorus distributions from Source and Drain are clearly revealed using the STEM EDX approach with a high probe current (4 nA) and a probe size estimated lower than 1 nm. The dopant inside the gate seems to segregate at the poly-silicon gate edges. Following the example of STEM EELS, the STEM EDX approach leads to precise chemical channel length measurements inside “real” nanoscale silicon devices. Besides, it is interesting to note the presence of As and P at the top of nitrite spacers which played their role by protecting the LDD from the high energy implant of the Source and Drain regions.

Figure 5. Two-dimensional quantitative arsenic dopant map acquired from a 40 nm gate length transistor using the STEM EEL spectrum imaging approach (Osiris TEM).

Figure 6. Two-dimensional (non quantitative) arsenic (left) and phosphorous (right) dopant maps acquired from a 40 nm gate length transistor using the STEM EDX spectrum imaging (Osiris TEM).

2.3 Stressors integration and characterization
To enhance carrier mobility and drive current in MOS transistors, several approaches based on strain engineering have been used in the semiconductor industry [10, 11, 12]. Unfortunately, till very recently, no physical characterization techniques were available to measure strain through the transistor channel with a sufficient sensitivity and spatial resolution. Considered for a long time as one of the most powerful techniques to measure lattice parameters [13, 14], Convergent Beam Electron Diffraction (CBED) technique suffers from some drawbacks largely described in the literature [15, 16, 17] leading to some difficulties to apply this technique in case of real devices analysis. For a few years now, two TEM based techniques have emerged as very promising techniques for the semiconductor field: Nano Beam Diffraction (NBD) [18] and Dark-field holography (DF Holography) recently developed by the CEMES lab at Toulouse [19].

\(^3\) The first worldwide S/TEM Osiris system has been installed at STMicroelectronics Crolles in April 2010.
The NBD technique uses a nearly parallel electron beam that can be obtained in a 2-condenser system by lowering the C2 aperture size down to about 10 µm. The corresponding semi-convergence angle classically obtained is 0.3 mrad with a probe size around 5-8 nm in a FEI Tecnai F20. Recent development on this technique using an FEI Titan with a 3-condenser system at CEA/Leti shows very promising results with strain sensitivity as low as 6x10⁻⁴ [20]. The main interest of this technique compared to CBED one is the device on-axis analysis capability. So, no sample tilt is required anymore and spatial resolution is then directly linked to probe size. Figure 7 shows NBD results obtained on a 45 nm PMOS transistor with SiGe source and drain stressors. Compressive strain through Si channel along x direction is clearly measured with the corresponding tensile strain along z direction.

![Figure 7](image)

**Figure 7.** NBD results on a 45 nm metal gate PMOS transistor with SiGe source and drain. (a) STEM image of the investigated device. Strain components values along x and z directions along line scan (B) under the gate (b), along line scan (A) through source, channel and drain regions (b) and along line scan (C) just below one stressor (d).

However strain mapping remains difficult to obtain with this technique due to large and time consuming data processing. Furthermore, NBD technique is still tricky to apply on low stressed devices.

In this case, dark-field electron holography based on the analysis of a hologram obtained by the interference between one diffracted beam through the region of interest with another through an unstrained (reference) region, could be an alternative. The main advantage of this technique is the principal strain components mapping feasibility on real devices. STMicroelectronics is involved in the development of this technique for microelectronics field applications through the “HDStrain” ANR project carried out by the CEMES lab in Toulouse.

We have developed in particular dedicated sample preparation by coupling backside milling (to avoid curtaining effects) with low energy milling at 8 kV (to limit amorphous layers thickness) in dual beam system. The aim is then to obtain parallel sided lamella with no bending and uniform thickness through a large field of view to ensure high-quality dark-field holography experiments.

### 2.4 Interconnection issue

Concerning transistors interconnects (backend, BE) issue, one of a main failure modes in IC technology is electromigration (EM). This phenomenon is the migration of atoms under electron flow in metal lines leading to formation of voids (figure 8b) and thus to the loss of chip functionality. To
characterize reliability of interconnects, dedicated EM structures (figure 8a) are tested in accelerated conditions (high temperature and current density) and monitored on resistance evolution with time. Some studies are currently performed to understand what drives EM (influence of copper microstructure?) and to find best process conditions to improve interconnect resistivity (surface treatment, impurities adding…).

The first relevant information after an EM test is the localization of the void(s) that need to be performed on very small features: 45 nm wide (W) and 100 nm thick (T) EM copper line geometry for the 28 nm node technology (figure 8a). In case of SEM imaging, interconnect is revealed by classical FIB cut whereas in case of TEM imaging, lamella preparation is required with thickness less than 45 nm in this case to avoid any 3D effects as illustrated in Figure 8b.

![Figure 8. a) Electromigration test structure sample b) TEM image of copper interconnect with small void localized under the via.](image)

Some experiments are actually performed [21] to show if local microstructure inside a metal line can influence or not electromigration mechanism. For this, electron back-scattered diffraction (EBSD) technique in an SEM is used to obtain texture and grain size information. Figure 9 illustrates an example of global microstructure analysis for 140 nm wide copper lines where changing copper deposition process results in much higher (111) texture but also much smaller mean grain size. This explains why reliability performances decrease for this process variation.

![Figure 9. EBSD maps for two different copper deposition conditions (reference on the right)](image)

Unfortunately, drift issue induced by charge effect is a major concern for EBSD experiments due to the presence of dielectric material separating copper lines. Thus a compromise must be made between mapping size and resolution to restrain this drift. Moreover, limits of EBSD technique begin to appear for these very small dimensions where grain size (mainly defined by line width) is comparable with SEM spot size in EBSD mode (with a 70° tilted stage). An alternative is to define process dedicated to EBSD analyses to limit sample preparation which can be complex (with top-down polishing) and take advantage of cleanliness of wafer going out of manufacturing.

To further understand EM phenomenon, we also need to access local information of void environment and ideally at the beginning of the void nucleation process step. In this case SEM-EBSD technique is not sufficient anymore and must be coupled with (S)TEM technique allowing a more precise void localisation (as illustrated in figure 10) [22,23]. Through this example we demonstrate the
interest in combining several characterization techniques and get complementary information. The localization of a void on EBSD maps (thanks to STEM image) shows that its place corresponds to multiple boundaries with five grains common in void.

For such analysis, sample preparation has become a key parameter to ensure relevant results. As STEM imaging requires a lamella preparation, we have to take into account possible damage induced by FIB on crystallography. So an optimum FIB voltage and current must be found to make compatible sample preparation with EBSD analysis.

Finally, it seems obvious that for actual developed technology, EBSD performed in SEM is limited. We must consider TEM imaging for highly resolved microstructure characterization. A commercialized system known as ASTAR allows performing equivalent of EBSD with indexing by template matching in a TEM. This system combines advantages of EBSD (with the TEM spatial resolution) to determine orientation grain, misorientation and localize small defects like voids at the beginning of growth which is less sensitive to sample preparation, contrary to EBSD.

2.5 Advanced morphology characterization: towards 3D visualization?
With even smaller dimensions of devices being developed in the semiconductor industry, physical characterization faces a challenge to provide information about the structures being developed: a relevant TEM analysis relies on the ability to prepare TEM lamellae with a thickness less than the feature to be observed, to not get projection effects of overlapping structures. For advanced technology nodes, such a sample preparation becomes a critical operation to pinpoint the exact location of the device, while thinning down a lamella to a few tens of nanometers.

As it allows analyzing specific features within ‘large’ volumes without projection effects, Electron Tomography (ET) overcomes these hard points in the physical characterization process. In the ET process, images of the sample to characterize are recorded in HAADF STEM mode every 1°, along a large tilt range, [-90°; +90°]. The obtained tilt series is then processed using the FEI Inspect3D™ software (for image alignment and tilt axis definition), to finally reconstruct a three dimensional volume from the aligned series using either weighted or iterative back projection techniques. Volume rendering and slice extraction from this virtual volume is then performed using ResolveRT™ software; it is thus possible to isolate a specific feature within the virtual volume without projection effect.

As the sample containing the feature of interest is tilted to record the ET series, the effective thickness of a TEM lamella as seen by the incident beam would drastically increase with the tilt angle, with a result of poor information extracted from the recorded images. Therefore, a specific sample preparation dedicated to ET is preferred to conventional TEM lamellae [24]: a chunk with the feature of interest is prepared and placed on top a probe, and then milled to obtain a cylinder-shaped sample (to keep a constant effective thickness all along the tilt range). The probe is then used in a specific sample holder, compatible with such specimens and allowing a full tilt range without shadowing effect (no ‘missing wedge’ effect).
With materials in the devices to be analyzed presenting large variation in atomic number $Z$, images recorded in HAADF STEM mode exhibit a large contrast between high $Z$ and low $Z$ compounds. Therefore, the camera length, i.e. the sample-to-detector distance, needs to be tuned to get a correct ratio between high $Z$ and low $Z$ signals, with the constraint to restrict it to the lower acceptable value, to not get diffraction contrast (that is tilt-angle sensitive). From an experimental point of view, such a compromise may be difficult to achieve, with the result to get poor information from compounds of low $Z$ in the reconstructed volume. As a consequence, ET appears to be more adapted to characterize back-end interconnected structures (with metallic compounds such as Cu, Ta, Ti, Al) rather than front-end structures, where a large variety of compounds - from Si, C, N to Hf, La, W, will alter the quality of the reconstructed volume) [25].

Figure 12 presents an ET study of a shared contact in a SRAM cell in C45 technology node. The shape of this tungsten plug can be easily resolved, as well as the NiSi silicide layer on top of the gate and under the plug. On the contrary, almost no contrast difference is observed between silicon (bulk), polysilicon (gate), SiCN (spacers), SiOC (dielectric). This example highlights the advantages of the technique to characterize metallic interconnects, and its limits where materials of low $Z$/high $Z$ co-exist.

3. Dedicated physical characterization techniques for “More than Moore” approach

3.1. FIB/SEM 3D for 3DI application
For some devices to be analyzed, physical characterization through either surface or cross section observation of the structure may not be sufficient to provide relevant results. As a fact, the need for physical characterization all along the volume of the device pushes for alternative solutions, such as FIB/SEM 3D.
This technique relies on the use of a dual column system, with the consecutive use of SEM imaging and FIB milling (figure 13): the structure is peeled in multiple cross sections, using the FIB to guarantee a constant thickness of the slices milled. After every milling operation, a SEM image of the physical cross section is recorded. The final data stack, that consists of typically several hundreds of images, will be treated (images alignment, volume filtering) to obtain a reconstructed volume. This allows 3D visualization and cross sections in the 3 directions (one real and two reconstructed).

To illustrate the technique, an example of 3D integration device is presented figure 14. Reliability tests have been performed on a (2x15 µm) Through Silicon Via (TSV) with cycles of heating ramps. This particular TSV has failed the electrical test. The origin of the failure is assumed to be due to the presence of a void in the metal pad under the TSV. The goal of this analysis is therefore to confirm the presence of the void and characterize it (location, volume). Exact location of the void with respect to the TSV can be given as well as the surface within the pad and the volume of the void. These provide useful data about the failure mode of the TSV.

In addition to the 3D information provided, FIB/SEM 3D demonstrates the advantage of top-down virtual deprocessing without any induced artifact; as a fact, such data would not have been obtained using step by step top-down deprocessing of this structure by mechanical polishing of the surface, as the void would have been filled during the polishing process and the structure would have been degraded.

Devices with micrometer scale dimensions are well adapted for the FIB/SEM 3D technique. As the technique is based on SEM imaging, the technique faces the same limitations of conventional SEM imaging: the achievable resolution restricts the use of such a technique to a minimum voxel size of $2^3$ nm$^3$. Furthermore, mechanical instabilities even make data acquisition at high magnification very difficult. Consequently, FIB/SEM 3D is better suited for devices in the 100 nm to 30 µm range, while other 3D techniques such as E-beam tomography or X-ray tomography fill the gap for devices of, respectively, lower or higher dimensions.
3.2. Dopant characterization in relaxed structures
Scanning Capacitance Microscopy (SCM) and Scanning Spreading Resistance Microscopy (SSRM) are two AFM based techniques able to characterize doping through respectively capacitance and resistance measurement. The detection limit of these techniques scales from $10^{17}$ at.cm$^{-3}$ to $10^{20}$ at.cm$^{-3}$. The advantage of both SCM and SSRM technique is the very high dynamic range of the detection limit compared to TEM based techniques like EELS or EDX. However, they suffer from difficult sample preparation. Indeed, for such experiments, the sample surface must be cleaned with no damage, so the use of FIB (which induces amorphisation and ion implantation) is forbidden for cross-section analysis. That is why these techniques are currently dedicated to relaxed structures (~ µm) like imager sensors characterization (figure 15) for which sample preparation by simple cleaving is possible.

![SCM map on vertical junction in relaxed structures](image)

**Figure 15.** SCM map on vertical junction in a relaxed imager structure performed at CEA/Leti. Distance between two consecutive DTI (Deep Trench Isolation) corresponds to pixel size (~1.5 µm). TCAD simulation and SCM map are in very good agreement.

4. Sample preparation
In semiconductor industry, one of today’s lab challenges is to provide in a volume mode and with shortest turn-around-times, high quality sample preparation methods allowing advanced physical characterizations of both very small and large scale features.

4.1. Sample preparation for small scale features
In case of small scale features, dual beam systems (FIB/SEM) are the preferred solutions serving failure analysis and process control applications (Figure 16). These tools are used very extensively. After localisation of the site of interest, cross-sections can be FIB-cut manually to obtain very precise single cross-sections or automatically with successive slices to provide 3-D information on defects or integrated features. They offer defect localisation within failing structures like memory cells and SEM characterizations capability without time consuming sample pre-preparation and without handling the sample after cutting.

Furthermore, if SEM resolution is insufficient to reveal the defect origin or the necessary process details, it is possible to prepare TEM samples using a controlled, easy to learn in-situ process and to efficiently continue the characterization with a high resolution TEM. FIB/SEM systems have revolutionized sample preparation for TEM. Several FIB based techniques exist to perform extraction of a TEM lamella: the conventional technique (using a sawed bar extracted from the wafer), the ex-situ and in-situ lift-out techniques. The in-situ lift-out technique is the privileged one providing lamella free from material re-deposition, compatible with plasma cleaning and if necessary, further lamella
thinning. When the lamella has been carefully prepared, TEM imaging is the final step of the analysis, TEM results can be available within 5 to 6 hours.

![Figure 16](image16.png)

**Figure 16.** a) SEM view showing an open contact in 28nm cell memory b) general SEM view of metal stacks in 45nm products.

The continuous development of ion columns leads to sample preparation improvement. In fact, the use of low energy milling can now be used easily in dual beam tools to limit the amorphous layer thickness on both sides of the TEM lamella. Alternative methods for sample preparation are also under investigation like backside milling to produce very thin parallel-sided lamellae for specific application like holography in TEM.

4.2. Sample preparation for large scale features

For the larger structures, like 70 µm x 70 µm Through-Silicon-Vias (TSV’s), bumps and copper pillars that are integrated in 3DI technologies or new packaging solutions, standard dual beams are not appropriate because the gallium based FIB milling rate (from 0.2 to 2.0 mm³/s) does not allow to remove high material volumes.

The use of conventional mechanical polishing techniques and / or cross-polishers is more suitable. The mechanical polishing action can induce scratches and other artifacts that reduce image quality. That is the reason why cross-polishers (CP) are now commonly used in semiconductor lab’s for larger scale features (figure 17). Use of broad argon ion beam eliminates this problem and can provide wide section fields of view (up to 2 mm), high quality sections free from artefacts for SEM imaging and EDX analysis if necessary (figure 18). The main drawback of methods using cross-polisher is that it requires several sample pre-preparation steps, essentially if the sample surface is not planar or protected:

1-sample sawing
2-capping with resist
3-mechanical polishing to approach the site of interest and
4- cross-polishing.

Therefore, the sample preparation is time-consuming (from 8 hrs to 12 hrs, depending on the section height). Another disadvantage of the method is that it allows neither successive sections nor SEM imaging to localize defects nor 3D-information. It is well appropriate for random construction analysis of large feature which does not require precise localisation (<15µm).
Figure 17. Sections of 70 x 70µm Through Silicon Vias: a) after mechanical polishing b) after final milling using a cross-polisher (high quality sample surface allowing high quality characterizations).

Figure 18: a) General SEM view of a cross-polisher section integrating a few bumps, b) zoom of bump base with EDX analysis of the RDL/bump interface.

To overcome these drawbacks (lack of precision, time consuming sample preparation, no capability to offer 3D information) semiconductor plants are very interested in new high current FIB milling that, recently, has been introduced to market. The FIB columns integrated in new systems are capable of high material removal rates at wider apertures (beam currents of 60-65nA). The SEM characterisation of a 80µm deep TSV as shown in figure 19b would take around 12hrs with standard dual-beams; with the new generation tools, the time is ~4 hrs.

Figure 19. a) SEM views of Cu pillars, b) high aspect ratio vias cut with a high ion beam current (FEI Helios 450 dual beam).
5. Conclusion
In this paper an overview of the different SEM and TEM based techniques to address specific issues at STMicroelectronics have been shown. Some needs have been raised for the future both in term of high resolution (at atomic scale in TEM) to measure very thin layers but also in terms of detection sensitivity for chemical analysis. Stressors integration in future technology will also require advanced techniques to precisely measure strain in the transistor channel of real devices.

Sample preparation (for both SEM and TEM) has now become a key parameter to ensure physical characterization reliability leading to some developments on FIB/SEM systems for both small and large features to analyse. We have also shown that 3D analysis (with E-beam tomography) could be an alternative for the future to avoid 3D effects in TEM lamella for very small structures characterization.

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