System integration of ATLAS ITK Pixel DCS ASICs

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ABSTRACT: During the ATLAS phase II upgrade, the tracking system of the ATLAS experiment will be replaced by an all-silicon detector called the inner tracker (ITK) with a pixel detector as the most inner part. The monitoring data of the new system will be aggregated from an on-detector ASIC called Monitoring Of Pixel System (MOPS) and sent to the Detector Control System (DCS) using a new interface called MOPS-HUB. The hardware components of the MOPS-HUB, firmware specifications for the FPGA of the MOPS-HUB and its integration plan will be presented. In addition, an irradiation plan for the new system will be introduced.

KEYWORDS: Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Digital signal processing (DSP); Front-end electronics for detector readout; Radiation-hard electronics

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1 Introduction

The ATLAS experiment will get a new inner tracker (ITk) during the phase II upgrade, the innermost part will be a pixel detector. The new ATLAS pixel detector will use a serial powering scheme to reduce the number of services inside the detector volume [1, 2]. To fulfill the control and monitoring requirements of the new pixel detector, a Detector Control System (DCS) is being developed [3]. The new DCS will have an on-detector ASIC called Monitoring Of Pixel System (MOPS) to monitor the voltages and temperatures of the detector modules and other sub-detector components [4]. A system integration plan of the MOPS chip that includes powering and communication with the MOPS-HUB interface as the central unit is under development. The MOPS-HUB will act as a bidirectional interface between the new MOPS chips and the local control stations of the DCS.

2 The Monitoring of Pixel System chip (MOPS)

The DCS for the ATLAS ITk Pixel detector consists of three separate paths which are Diagnostics, Control & Feedback, and Safety. The Control & Feedback path implements the control and monitoring of the power supplies and an independent monitoring of individual detector modules [5]. The monitoring of the detector modules will be done using a new ASIC called MOPS with a CAN-open based protocol implemented in it for data transfer. The new MOPS chip was developed to perform these tasks under high radiation exposure (up to 500 Mrad). One MOPS chip can monitor temperature and voltage of up to 16 detector modules in a serial power chain [4].
3 Integration of the MOPS chip

The MOPS-HUB is an FPGA based interface. Its main task is the aggregation of monitoring data between the MOPS chips (installed at the vicinity of the detector modules) and the DCS computer. Beside that, the MOPS-HUB will monitor information per CAN bus (voltage/current) and send it to the DCS computer as part of the data stream. In addition, it will have a full power control over the connected CAN buses.

Depending on the configuration, the MOPS-HUB FPGA can interface simultaneously up to 16 CAN buses in the vicinity of the detector modules direction (see figure 1). Each CAN bus is a serial communication bus, which allows several CAN nodes on the same CAN bus (up to 4 MOPS). The MOPS-HUB itself will be placed in racks on the walls of the ATLAS cavern which is roughly 70 m away from the vicinity of the detector modules. The data collected from the CAN buses are forwarded through low power differential signals called elinks to the Embedded Monitoring and Control Interface (EMCI) which is also placed in racks on the walls of the ATLAS cavern [6]. The aim of the EMCI, is to work as a further data aggregator between the MOPS-HUB and the DCS. It combines all signals to one bidirectional channel and interfaces with an optical transceiver, which then transmits the data through an optical link to the Embedded Monitoring Processor (EMP) [6]. The EMP device will be placed in the counting room (see figure 1). It will drive up to 12 EMCI’s and interfaces them to the control network (Ethernet). Both EMCI and EMP are ATLAS standard DCS components. In addition, the MOPS-HUB will distribute the power (VCAN-PSU), which is delivered from the main power supplies, onto the individual MOPS services. Where, the FPGA powering is independent of the CAN bus power scheme.

![Figure 1: The complete MOPS-HUB network.](image)

4 Firmware description

Figure 2 presents a block diagram of the MOPS-HUB FPGA firmware.
Figure 2: Firmware design of the MOPS-HUB FPGA. The black bold lines represent data lines while the light gray lines represent the control signal from/to the top State Machine (FSM).

Figure 3: The MOPS-HUB FPGA board with Xilinx’s Artix 7 Series FPGA (XC7A200T) on a SOM-board (Alinx AC7A200) as a core component.

The firmware consists of eight components:

- **CAN node interface**: collects the signals from all the inputs and send them to the next step for processing. It includes all blocks needed for CAN communication.

- **The TX writer**: instantiates the memory blocks (Upstream FIFO module and the 8B10B encoder). The data coming from the 8B10B encoder will be multiplexed out on 2 bit port before transmission on the elink port. In this stage the 8B10B encoder will encode the data so that a DC-Balanced code will be transmitted over each elink data line.

- **The RX reader**: instantiates the memory blocks (Downstream FIFO and the 8B10B decoder). The data in this block is synchronized, deserialized and aligned to 8B10B symbols once
received from the elink side.

- **The elink transceiver**: provides all necessary building blocks needed for transmission and serialization over the elinks. All the sub-modules included (OSERDESE2, ISERDESE2, IBUFDS and OBUFDS) are supported from the manufacturer (Xilinx).

- **Bus control**: enables/disables the VCAN of the connected buses using SPI communication. The module is designed in a way that the status of VCAN is preserved. Where, even if the FPGA is power cycled for any reason, the status of VCAN will be unchanged.

- **Bus monitoring**: transfers the monitoring data read by external ADCs to the data stream over elinks. Where, the monitoring information per CAN bus (voltage/current of VCAN) will be acquired via an SPI bus.

- **State Machine (FSM)**: brings up the system in a working state, synchronizes the signal and manage processes between all the design components. Beside that, it will supervise the data transfer between CAN buses and elinks.

- **Watchdog**: monitors the status of the top FSM after powering up. Once the FSM hangs for about 1–2 seconds due to errors, a timeout signal (generated by the Watchdog Timer) will be generated and an automatic recovery from interruptions will be activated. This automatic recovery will bring the system into a safe state.

### 5 Re-configuration

To protect the system from firmware malfunction, the Watchdog module described in section 4 is developed to recover the system internally without requiring an external reset or power-cycle.

The radiation effects related to SRAM based FPGAs will be mitigated by comparing the checksum derived from the SRAM with an external image of the design saved in a multi-boot memory. The process will be done continuously so that once a mismatch is detected, a fresh copy of the configuration will be loaded to the external memory through an elink.

Besides the stable recent image stored in the external memory, another golden image of the design will be stored at a different address. The golden image acts as a fallback image that allows the design to communicate through elinks in the event of configuration memory corruption due to SEUs. A full automatic re-configuration of the MOPS-HUB FPGA will be applied to the FPGA if it does not respond. In this scenario, the design will be able to reset and reconfigure itself.

### 6 Firmware simulation

The functional simulation of the MOPS-HUB design has been performed. where, the Design under test as well as 16 MOPS chips connected were instantiated within a self-checking test bench that is able to automatically compare actual outputs to expected outputs. The simulation mechanism includes data exchange between the MOPS-HUB and the MOPS chips via CAN communication and decoding/encoding the data stream through a debug module that is able to deal with 8B10B encoding/decoding. With the help of simulation, the MOPS-HUB was able to communicate
successfully with the MOPS chips and read the ADC values out of each connected MOPS in the chain. Other tests include enabled many fault conditions to be created (e.g CAN error messages) and the response to them validated, if necessary by the intervention of the watchdog unit.

7 Hardware implementation and experimental results

The performance of the new MOPS-HUB interface is evaluated using a test system (see figure 4). The FPGA chosen for the MOPS-HUB core is the XC7A200T from Xilinx’s Artix 7 Series [7]. The system setup is divided into four sections. First, the MOPS chain composed of three MOPS chips, each mounted on a carrier board, allows communication to each MOPS chip via the CAN bus network. The carrier board provides the required powering for the MOPS Module (VCAN) which is controlled by the firmware logic as described in section 4 using the bus Control module. Each MOPS in the chain is connected to a dummy module that emulates the behavior of the sub detector modules in a serial powering chain by introducing some predefined value to the ADC of MOPS through different NTCs and resistors. The second section includes a custom board called CAN Interface Card (CIC) which houses the physical layers of the CAN data lines and allows for monitoring the voltage/current of the VCAN lines. The third section includes the device under test, the MOPS-HUB FPGA board shown in figure 3. It provides access to the FPGA logic of the target FPGA, and acts as a bridge between the CAN chain (through CIC at 125 kbit/sec) and the elink side (at 80 MHz). The forth section consists of a Xilinx ZCU102 FPGA evaluation board called the MOPS-HUB Measurement board, which controls the MOPS-HUB. The board is deployed as a remote controller for the setup. It monitors and reads out the MOPS-HUB data over the elinks and decodes the 8B10B data received from the MOPS-HUB before sending it to the main computer via dedicated Ethernet link (at 1 Gbit/sec). The payload of a complete data packet received/transmitted is made up of 76 bits grouped into 32 bit data frames. The information regarding MOPS Id and CAN bus Id was extracted in real time over a 24 hour period and saved for off-line analysis. No error was found in the dataset.

8 Radiation tolerance

Table 1 shows the expected radiation at the walls of the ATLAS cavern based on the radiation background simulation results in the ATLAS hall using FLUKA (The simulation results are provided by ATLAS collaboration). In order to minimize radiation induced errors and enhance data reliability,
TMR technique is applied to the design. A disadvantage of this approach is the increased resource utilization of the FPGA by no less than three times. In an effort to keep the hardware utilization on a level which would allow for upgrades or additions to the system, an approach of only triplicating Flip-Flops is chosen.

Table 1: Expected radiation at racks on the walls of the ATLAS cavern.

| TID     | Neutron fluence | Hadron fluence (>20 MeV) |
|---------|-----------------|--------------------------|
| 3 krad  | $5 \times 10^{11} \text{N}_{eq}/\text{cm}^2$ | $2 \times 10^{-7} \text{cm}^2/\text{pp}$ |

9 Summary and outlook

A new interface called MOPS-HUB for data aggregation between the monitoring chip, MOPS, of the ITk pixel detector and the DCS has been presented. The central unit of the MOPS-HUB is an FPGA which supervises the data transfer between MOPS and the DCS and manages processes between all the hardware components. The MOPS-HUB will be operating in a radiation environment which poses special requirements on the design and firmware. Prototypes exist, all firmware blocks are defined, the functional simulation has been performed successfully and first experimental data of MOPS have been collected. In a next step special testing in a radiation environment will follow.

References

[1] ATLAS collaboration, Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment, CERN-LHCC-2012-022, LHCC-I-023 (2012).

[2] L. Gonella et al., A serial powering scheme for the ATLAS pixel detector at sLHC, 2010 JINST 5 C12002.

[3] S. Kersten et al., Control, Safety, and Diagnostics for Future ATLAS Pixel Detectors, in 14th International Conference on Accelerator & Large Experimental Physics Control Systems, San Francisco, CA, U.S.A., 6–11 October 2013, p. tuppc050 (2014) [https://cds.cern.ch/record/1696966].

[4] A. Walsemann et al., A CANopen based prototype chip for the Detector Control System of the ATLAS ITk Pixel Detector, PoS TWEPP2019 (2020) 013.

[5] ATLAS collaboration, Technical Design Report for the ATLAS Inner Tracker Pixel Detector, CERN-LHCC-2017-021 (2017) [DOI: 10.17181/CERN.FOZZ.2P3Q].

[6] D. Blasco Serrano et al., Description and status of the EMCI-EMP interface, 2022 JINST 17 C06012.

[7] Xilinx, Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics, (2022), https://docs.xilinx.com/v/u/en-US/ds181_Artix_7_Data_Sheet.