Abstract—This paper introduces new perspectives on analog design space search. To minimize the time-to-market, this endeavor better cast as constraint satisfaction problem than global optimization defined in prior arts. We incorporate model-based agents, contrasted with model-free learning, to implement a trust-region strategy. As such, simple feed-forward networks can be trained with supervised learning, where the convergence is relatively trivial. Experiment results demonstrate orders of magnitude improvement on search iterations. Additionally, the unprecedented consideration of PVT conditions are accommodated. On circuits with TSMC 5/6nm process, our method achieve performance surpassing human designers. Furthermore, this framework is in production in industrial settings.

Index Terms—transistor sizing, artificial intelligence, reinforcement learning, electronic design automation

I. INTRODUCTION

The annual increment of computing power described by Moore’s law is pioneering unprecedented possibilities. This remarkable progress has been accompanied by a collinearity with tremendous increases in chip design complexity. One example of this is the growth in PVT (process, voltage, temperature) corners.

Despite the majority of the SoC area is occupied by digital circuitry, analog circuits are still essential for the chips to be able to communicate with and sense the rest of the world. However, the design effort of the analog counterpart is more onerous due to the heavy requirements of human expertise, and the absence of automation tools similar to digital circuit design.

One of the labor intensive task in analog design is transistor sizing. Currently, it is mostly done by labouring trial-and-error. The designers begin by applying their knowledge about the characteristics of analog circuits and transistors to select a reasonable range of candidate solutions, next explore the space with grid search. Then, get feedback from SPICE circuit simulations. Afterward, repeat the procedure until the specifications are met. The main challenge of automating sizing is that it has a very large design space, which prior arts suffered from convergence problems and poor scalability.

In this paper, we propose a general learning-based search framework (Fig. 1) to help increase R&D productivity during analog front-end sizing task (Fig. 2). Experiment results demonstrate that our agents can efficiently and effectively accomplish search in state-of-the-art designs with superior performance while achieving area enhancement over human. The contributions of our work are severalfold on different levels.

- **System level** We propose a general framework for IC design space search. The standardized API allows fast migration provided well-formulated problems. The ultimate goal of the framework is to increase R&D productivity with minimal extra efforts required.
- **Algorithm level** The proposed model-based reinforcement learning (RL) approach directly mimic the dynamics of the SPICE simulation instead of estimating cumulative future reward in model-free learning. This enables a more adequate implementation for usages in the industry.
- **Verification level** Considerations on PVT conditions better suits practical needs. The negligence of PVT conditions on previous works make them far from industrial adaptation.

II. PRIOR ARTS

Sizing automation could be framed as an optimization problem. Bayesian optimization (BO) is a popular choice...
because of the sample efficiency in finding the global optimum \[2\][3]. Despite of the promising results, the scalability is a major drawback. Note that the scalability addressed is the cubical increment of the number of samples, rather than the dimensionality of the space.

Recently introduced methods primarily leverage the current success in deep learning. Model-based RL trained with well-developed supervised learning methods, were established as not suitable for IC design space search due to the difficulty in providing sufficient data samples for training \[11][4]. Some models demand re-training when a new set of specifications is assigned, hence, cannot be reused \[5].

In later publications, model-free RL comes prominence. AutoCkt \[6\] aims to train an efficient agent to explore and gain knowledge about the design space. The agents will then be used to generate trajectories during inference. Yet, it is rarely necessary to traverse the space in the industry.

L2DC \[7\] exploits sophisticated sequence-to-sequence modeling using an encoder-decoder technique. GCN-RL \[8\] employs the latest innovation - graph convolutional neural networks - to learn features from the structures. This enables the model to reach better transferability between nodes and topologies. In spite of their ability to exceed human-level performance, the amount of human-engineering efforts in observation selection, network architecture design, and reward engineering reduce the feasibility of becoming a generalizable automation tool.

III. PROBLEM FORMULATION

Transistor sizing (Fig. 2) is an iterative process to determine a suitable set of lengths, widths, and multiplicities for each transistor in the topology in order to achieve the desired specifications. This scheme is often regarded as a trade-off between constraints. Larger transistor sizes normally lead to greater performance, but consume more power and area.

Analog circuit sizing can be formulated as a constrained multi-objective optimization problem, defined in \[1\].

\[
\begin{align*}
\text{Minimize} & \quad F_{m,c}(X) \quad m = 1, 2, \ldots, N_m \\
\text{subject to} & \quad C_{d,c}(X) < 0 \quad d = 1, 2, \ldots, N_d \\
& \quad X \in D_s
\end{align*}
\]

where \(X\) is a vector of variables to be optimized; \(D_s\) is the design space; \(F_{c,m}(X)\) is the \(m^{th}\) objective function under the \(c^{th}\) PVT condition; \(C(X)_{d,c}\) is the \(d^{th}\) constraint under the \(c^{th}\) PVT condition.

IV. PROPOSED FRAMEWORK

The proposed framework is shown in Fig. 1. Deep RL is believed to be a robust methodology for solving combinatorial search problem in various disciplines without human in the loop, such as games \[9][10][11], robotic control \[12][13], neural architecture search \[14][15], and IC design \[16][17]. We thus cast the transistor sizing task as a DRL framework. This allows us to automate the process, while being able to adapt to the environment fast based on past experiences, and evolve over time. This system consists of several subsystems described in the following sections.

A. Problem reformulation

Transistor sizing (Fig. 2) has long been formulated as an optimization problem, in which agents and optimizers are implemented to search for optimal points in objective functions. However, it is worth a rethink of what is an adequate implementation to integrate with the flow of a designer. With the exponential growth in PVT corners during fast technological advances, finding the global optimum is often infeasible.

In contrast, meeting the constraints assigned by designers is more practical.

In this manner, the problem can be reduced to a constraint satisfaction problem (CSP), where the objective function in \[1\] is replaced as a 0 constant function. More generally, CSP is defined as a triple \((X, D, C)\) \[2\].

\[
X = \{x_1, x_2, \ldots, x_n\} \\
D = \{D_1, D_2, \ldots, D_n\}, \quad D_i = \{b_1, b_2, \ldots, b_l\} \\
C = \{C_1, C_2, \ldots, C_k\}, \quad C_j = (t_j, r_j)
\]

Fig. 2. Analog circuit pre-layout design flow
supervised learning as per the metric of global goodness of fit. However, it still works given that the local landscape can be captured. Moreover, no reward is involved in the training of model-based agents, making it insensitive to reward engineering. 3) Easier implementation and convergence: model-free agents behave based on a surrogate network modeling the relationship between past trajectories and the next actions to take. Nonetheless, this custom model tends to complicate the problem which makes it hard to converge. Whereas the training routine of supervised learning is relatively trivial.

All virtues combined actuates a model-based approach, where a direct modeling of the compact circuit space $\mathcal{D}_L$ from transistor sizes $X$ to circuit measurements $S_{\text{pice}}(X)$ is mapped, imitating the behavior of a SPICE simulator. A simple feed-forward neural network $f_{\text{NN}}(X; \theta)$ with 3 layers can be used as a SPICE function approximator (3).

$$\hat{y} = f_{\text{NN}}(X; \theta) \approx S_{\text{pice}}(X), X \in \mathcal{D}_L$$  \hspace{1cm} (3)

where $\hat{y}$ is a vector of predicted measurements (e.g., gain, phase margin, etc) w.r.t. a vector of sizes $X$ estimated with weights $\theta$.

The loss function $J(\theta)$ is simply obtained by the mean squared error (MSE) (4).

$$J(\theta) = \frac{1}{m} \sum_{i=1}^{m} (S_{\text{pice}}(X^{(i)}) - f_{\text{NN}}(X^{(i)}; \theta))^2$$  \hspace{1cm} (4)

Model-based agent is an obscured choice in recent RL solutions. It aims to learn a predictive model $f_{\text{NN}}$ to mimic the dynamics of the environment $S_{\text{pice}}$, then plan on the model. From this, the number of iterations can be thus reduced. A recent novel publication (4) use such agents in Atari game play. They claimed that humans can learn fast thanks to the intuitive understanding of the physical processes, and we can apply it to predict the future. Therefore, agents who possess such skill could be more sample efficient.

Each search starts by a random exploration in the design space. Next, the most optimal point will be selected as the local area $\mathcal{D}_L$ to dive in. The policy is that by modeling the local landscape, a candidate solution can be chosen in the local domain as the next step based on the expected value (discussed in IV-D) computed with predicted measurements $\hat{y}$. The properties of the local area is granted by the trust region method (TRM), explained in IV-C. Even though an optimization or another policy network can be incorporated to find the candidate with the maximum value, to take the advantage of the fast inference time of a neural network, a more vanilla Monte Carlo sampling-based planning is used. The pseudocode of the realization is detailed in Algorithm [IV-B].

### C. Trust region method

The transition of search space size from a global landscape to a local area is the key factor to the performance of our agents. Thus, the definition of the local properties plays a role in the algorithm efficiency. If the compact domain is statically fixed throughout the search, the neural network model could have bad extrapolation properties at the beginning of the episode, when only few samples exist.

Trust region method defines an iteration-dependent trust region radius $\Delta r_i$ where we trust the model $V_{\text{value}} \circ f_{\text{NN}}$ to be an adequate representation of the objective function $V_{\text{value}} \circ S_{\text{pice}}$. At each iteration $i$, a trust region algorithm first solves the trust region subproblem (5) to obtain $d^{(i)}$. In our case, this is realized by Monte Carlo sampling as mentioned in IV-B.

$$d^{(i)} = \arg\max_{X^i + d \in \mathcal{D}^i_{\text{tr}}} V_{\text{value}} \circ f_{\text{NN}}(X^i + d),$$

$$\mathcal{D}^i_{\text{tr}} = \{ X \in \mathcal{D} : \| X - X^i \| \leq \Delta r_i \}$$  \hspace{1cm} (5)

where $d^{(i)}$ is a vector of optimal trial steps, $\| \cdot \|$ is a norm, $\mathcal{D}^i_{\text{tr}}$ is the trust region.

Then, compute the ratio $\rho^i$ of the estimated reduction and the actual reduction. A criterion is set to accept the trial step, i.e. if the ratio is not significant, then the trial point will be rejected. Finally, the radius is updated based on the $\rho^i$. If the neural network closely approximate the objective function $V_{\text{value}} \circ S_{\text{pice}}$, then the trust region will be expanded, shrank otherwise.

### D. Reward (value) engineering

For our agents, there is a value function to estimate the merit of a set of circuit measurements after SPICE simulation. This is served as an indication of where to go next. Unlike model-free actor-critic methods, values do not participate in training. Consequently, the design of the formula does not affect the convergence of the model.

In the spirit of simplicity and generalization, we utilize a naive tactic where the value is the sum of normalized measurements. This way, no extra information is acquired. However, in terms of the trade-off between constraints, a second-stage value function could be implemented to explicitly encode the importance of each measurement once the agent enters a optimal local area.
E. PVT exploration strategy

In order to push the system to production, one important aspect to consider is the PVT conditions. To guarantee that a chip is able to work under the variations of fabrications, power supplies, and environments, a number of corners have to be signed off before tape-out. Nonetheless, to best of our knowledge, no prior art has accommodated such regime.

A simple way to explore the conditions would be to test all PVTs every time a new set of assignments is obtained. Yet for deployment, this strategy would pose a waste in computing resources and EDA (electronic design automation) tool licenses if the agent is not yet ready for verification.

Inspired by heuristics of designers, first focus the search on a single condition, usually the most difficult condition to search, assuming that by overcoming the hardest PVT, easier ones would be easy. Once all the specifications are met, verifications will be conducted to confirm that the set of assignments are legal under all other conditions as well. Accordingly, the proposed progressive strategy is that if the initial condition does not apply, the corner with the least value will be chosen to be searched next, until all constraints are satisfied under all conditions (Fig. 3). If multiple corners are under search, the candidate solution will be taken as the complete assignments with the lowest expected value. Note that each PVT condition has its own independent model.

In Algorithm 1, the search is demonstrated in an uniform condition. However, it is painless to generalize to our progressive strategy.

F. API

A framework with a powerful search algorithm could be wasteful if the user interface is unfriendly or requires extra effort to use. In the introduced API, only information that the designers need in their original flow is acquired. In particular, human experts will need to identify the transistor sizes to tune, the ranges of variables, the circuit topology, the measurements to observe from SPICE simulations, and the specifications for each corner. Once the configuration is set, an automatic script will construct necessary components, namely the neural network architectures and hyperparameters of the network, which are also dynamically scheduled on the fly. That is to say, our framework is equivalent to a SPICE decorator where the DRL agents are encapsulated, which seamlessly automates transistor sizing with generalization.

V. EXPERIMENT RESULTS

A. Experimental setup

Our experiments are conducted on both academic and industrial settings to evaluate the feasibility and the capability of the DRL agents.

During the development phase, the agents are tested on a two-stage opamp with BSIM 45/22nm processes simulated on an open sourced NGSPICE simulator developed by UC Berkeley. Two scenarios that are often encountered in practice, specifically, process porting and PVT exploration are analyzed.

To demonstrate that the proposed framework is beneficial in production, we cooperate with industrial professional designers and evaluate the agents on two industrial cases with the most advanced TSMC 5nm and 6nm technologies. Simulations are conducted in Cadence Spectre.

B. 45nm two-stage opamp

First, we benchmark our method with various baseline models including random search, customized BO (designed, implemented, and tuned by ourselves), Advantage Actor Critic (A2C) [20], Proximal Policy Optimization (PPO) [21], and Trust Region Policy Optimization (TRPO) [22] implemented by Stable-Baselines [23]. The customized BO utilizes dynamic balancing of exploration & exploitation, and also substitutes Gaussian Process with extra-tree regressor. All model-free agents follow the same observation design in AutoCkt [6], and use the same reward function as our agents. This experimental environment is set on a BSIM 45nm process two-stage opamp simulated in a single PVT with a design space size of $10^{14}$. The comparison is shown in Table I.

Each experiment has a 10k-step limitation. For the customized BO and our model-based agents, 100 experiments are ran to prove the stability, whereas for agents in stable-baselines, only 10 are executed since it would have taken about a month to complete.

| TABLE I | PERFORMANCE OF AGENTS IN 45NM TWO-STAGE OPAMP |
|---------|-----------------------------------------------|
|         | Success rate | Average iterations |
| Random search | 100% | 8565 |
| Customized BO | 100% | 330 |
| A2C [20] | 90% | 3497 |
| PPO [21] | 40% | 31503 |
| TRPO [22] | 20% | 16350 |
| Our method | 100% | 36 |

The experiments show that random search is a strong baseline in which model-free agents (A2C, PPO, TRPO) failed to reach its performance. The reason is that there exists a trade-off between gain and phase margin, which are two constraints of opamp. Circuits with high gains often come with unstable phase margins. Hence, if the reward formula of model-free
agents do not encode such information, the agent can be easily stuck in a local maxima where this happens.

The customized BO states a solid stability among our experiments, however, the nature to estimate the global distribution gains iterations compared with our local model-based agents. As for model-based agents, all specifications can be met within 36 steps on average. Moreover, the standard deviation is 16 steps, which indicates that the search is stable. This comparison demonstrates that our idea of implementing an agent good at local exploration is feasible, and can outperform model-free agents by orders of magnitude.

C. Process porting

Many circuit topologies have to go through a process migration. To avoid reinventing the wheels every time a new process node is applied, AIP (analog intellectual property) reuse is an important topic worth discussing. To better understand how the information obtained from the previous nodes can help speeding up the sizing of the new node, a migration from BSIM 45nm to 22nm process is prepared. Each experiment is ran for 100 times in the BSIM 22nm circuit to account for the randomness.

\[
\text{TABLE II} \quad \text{RESULTS OF PROCESS PORTING FROM 45NM TO 22NM}
\]

| Baseline (random weights, random starting point)\(^a\) | Average steps | Min steps | Max Steps |
|-----------------------------------------------------|---------------|-----------|-----------|
| Weight sharing, starting point sharing\(^b\)         | 29.22         | 3         | 310       |
| Random weights, starting point sharing\(^c\)         | 20.74         | 2         | 88        |

\(^a\) Directly deploy our method on 22nm without process porting  
\(^b\) Use the optimal network weights and optimal solution as starting points that the model found in 45nm process  
\(^c\) Apply random weight initialization but start the agent on different optimal solutions found in 45nm process

All three strategies can find solutions 100% of the time, so the success rate is omitted. Table II shows that optimal points from previous nodes are reliable. However, the results state impotent network weights transferability, implying that the distributions between processes are distinctive. Interestingly, this phenomenon matches designers’ experiences: previously sized circuits are strong references, but the equations describing the physics of transistors could be distinguishing.

D. PVT exploration

Finding a sufficient set of sizes in a single condition is only a part of the story. Thus, we test PVT exploration strategies on our method using the two-stage opamp with BSIM 22nm process. The results are illustrated in Table III

\[
\text{TABLE III} \quad \text{COMPARISON OF PVT EXPLORATION STRATEGIES}
\]

| Random search | Average steps | Min steps | Max steps |
|---------------|---------------|-----------|-----------|
| Brute force (test all cond.) | 359.4 | 36 | 1305 |
| Progressive (random cond.) | 89.52 | 29 | 450 |
| Progressive (hardest cond.) | 72.60 | 15 | 279 |

is not sensitive to the initial condition, which is positive for cases where the toughest PVT corner is unidentifiable owing to the number of permutations.

E. Industrial cases

LDO (Low-Drop regulator) on TSMC 6nm process The first industrial example is a LDO with TSMC 6nm process. In this case, the design space possesses about 10\(^{29}\) possible combinations.

The number of iterations of human designers is untraceable. Nevertheless, our agent achieved the specification in all corners within 2609 iterations, which is considered fast in designers’ opinion. Furthermore, the performance obtained surpass designers while producing even lower area, shown in Table IV. An interesting discovery is that even some of the device sizes decided by both AI and human are the same, AI still managed to illustrate an area enhancement.

In comparison with our customized BO, it cannot satisfy all the constraints within a reasonable time. However, the best parameters searched are very close to the specifications.

\[
\text{TABLE IV} \quad \text{BENCHMARK OF LDO CIRCUIT SIZING WITH DIFFERENT AGENTS}
\]

| Specification | # iterations | Loop gain | Area |
|---------------|--------------|-----------|------|
| Human         | untraceable  | >40dB     | <650nm² |
| Customized BO | failed       | 38.2dB    | 604nm² |
| Our method    | 2609         | 40.0dB    | 632nm² |

\(^3\) Customized BO did not satisfy the constraints (not shown here), however, it gives very close results

ICO (Current-Controlled oscillator) on TSMC 5nm process An ICO is tested as the second case with TSMC 5nm process. The design space size is 20\(^4\).

The AI-sized ICO realized a performance on a par with human designers. A comparable result is also exhibited in the customized BO. Yet, as mentioned before, the global search strategy cause 4.5 times more iterations than our local search algorithm (Table V).

\[
\text{TABLE V} \quad \text{BENCHMARK OF ICO CIRCUIT SIZING WITH DIFFERENT AGENTS}
\]

| Specification | # iterations | Phase noise | Frequency |
|---------------|--------------|-------------|-----------|
| Human         | untraceable  | <7/1dB      | >3GHz     |
| Customized BO | 194          | 3.1/3dB     | 8.8GHz    |
| Our method    | 43           | 1.7/6dB     | 9.1GHz    |
Although the design space of the second case is relatively small, this leads to a declaration. Numerous concerns in the community are raised on AI safety [24]. As an initial assessment, the ability and the characteristics of the designed circuits are unfamiliar. Therefore, to ensure that the agents act as intended and to secure the safety of the products, designers have to fix a subset of the parameters, only letting the agents to search for the rest. To that end, not until we have a comprehensive rule for regulating the agents can we unlock the full capability of AI. Thus in our evaluations, designers went through a rigorous screening process to examine the designed circuits. Fortunately, the sized circuits are ready to tape out.

From both cases described earlier, the outcome is akin to what is addressed in SimPLLe [11]. Transistor sizing is one of the task that benefits from the sample-efficient advantage of model-based agents.

In summary, the results state the contributions of this framework in two ways:

- provides better performance within a reasonable time
- automates the process, leaving human intervention while obtaining granting satisfactory performance

This also indicates that the model is generalizable across different circuit schematics and process nodes. The term generalization here does not refer to network weight level transfer as the convention in machine learning genre, but rather algorithm architecture level.

**DISCUSSION**

As the results of this work shows, the proposed search algorithm can achieve automation at human level in analog block circuit sizing. Even though some sections of the flow could be accomplished by AI agents, but AI would not be useful if the upstream tasks such as system-level architecture design and circuit-level topology selection were not carefully executed by human experts with their rich experiences and knowledges.

In concern with the real capability of the scalability, certainly, AI is not trained, nor designed to achieve full analog system circuit design since it is computationally infeasible. Rather we can embrace current limitations by divide-and-conquer. One can feed an appropriate amount of design to our search framework, and by recursion, we can avoid such scalability problem. Once again, it is the merit of designers to come up with a segmentation that allows us to leverage the current AI technology.

**CONCLUSIONS**

In this work, we propose a generalizable search framework using learning-based algorithms for solving the analog circuit sizing problem. We take a novel direction where a trust-region method is adopted using model-based agents trained with supervised learning. This enables fast design space adaptation. Moreover, a PVT exploration strategy is also proposed to account for different working conditions, which is not considered in previous works.

Practical evaluations on industrial products with advanced TSMC 5/6nm process shows exceptional results. Our agent achieves performance beyond human level while producing smaller area. Furthermore, the presented framework is not limited to this specific stage of the flow. Any section that could be cast as a search problem can be transferred and leverage the assistance of this DRL agents.

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