Automated Formal Equivalence Verification of Pipelined Nested Loops in Datapath Designs

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Abstract—The ever-growing complexity of digital systems has made designers move toward using Electronic System Level (ESL) design methodology at a higher abstraction level. The designs at ESL are then automatically synthesized to Register Transfer Level (RTL) by means of High Level or behavioral Synthesis (HLS) tools. Due to possibility of buggy synthesis, especially when the target design must be manipulated or optimized (i.e., pipelining), an efficient equivalence checking method is necessary to check functional equivalency of the ESL specification and the RTL implementation. This problem is even more serious in the case of loop pipelining, since several challenges such as overlapping execution, retiming and forwarding occur which make traditional sequential equivalence checking approaches inapplicable. At the same time, the growing market for datapath dominated applications such as DSP for multimedia applications and embedded systems requires a suitable Computer-Aided Design (CAD) support for their verification. In this paper, we present an efficient formal approach to check the equivalence of synthesized RTL against the high-level specification in the presence of pipelining transformations. To increase the scalability of our proposed method, we dynamically divide the designs into several smaller parts called segments by introducing cut-points. Then we employ Modular Horner Expansion Diagram (M-HED) to check whether the specification and implementation are equivalent or not. In an iterative manner, the equivalence checking for each segment is performed. At each step, the equivalent nodes and those nodes which have an impact on them are removed until the whole design is covered. Our proposed method enables us to deal with the equivalence checking problem for behaviorally synthesized designs even in the presence of pipelines for nested loops. The empirical results demonstrate the efficiency and scalability of our proposed method in terms of run-time and memory usage for several large designs synthesized by a commercial behavioral synthesis tool. Average improvements in terms of the memory usage and run time in comparison with SMT- and SAT-based equivalence checking are 16.7× and 111.9×, respectively.

Index Terms—Formal verification, equivalence checking, pipelined nested loop, HED

1. INTRODUCTION

The complexity of next generation of digital systems has overtaken traditional time consuming handcrafted RTL design methods. Therefore, some approaches are desirable to generate RTL codes automatically. High Level Synthesis (HLS) tools have been provided to respond to such needs. The HLS is the process of generating RTL design from higher level programs such as C, C++, SystemC, or so on [6]. Using HLS tools leads to more productive designs for next-generation, computationally intensive applications. When we make use of HLS tools, however, we need to make sure that synthesized RTL is bug free. This indicates that the transformation correctness of high level or behavioral synthesis phase is very important [2, 3].

A large amount of work has been done to verify the RTL against its specification. A combinational equivalence checking approach between designs in SystemC and RTL has been suggested in [4]. The authors of [7], [8] and [9] presented Sequential Equivalence Checking (SEC) approaches between software specification and hardware implementation. During equivalence checking, several optimization techniques such as cut-point, cut-plane and cut-loop are used. The cut-point optimization is to find internal equivalent nodes of specification and their corresponding circuit implementations. Cut-points reduce the size of symbolic expressions by replacing verified subcircuits with new symbolic values [28]. Cut-plane is considered as a set of cut-points while cut-loop is considered as a cut-plane at the end of a loop [30]. Some techniques have been proposed to check the equivalency between combinational circuits with some structural similarities using bit-level decision diagrams [28, 31] SAT-based approaches [38, 39, 43, 44], probabilistic methods [46] and directed test generations [47]. The structural similarities enable them to find identical internal nets as cut-points to partition the whole design into a set of smaller segments. However, their approach to problem of equivalence checking is limited to bit level verification and hence cannot handle large RTL designs. In [30], the authors have proposed a novel approach to verify equivalence of C-based system level description versus RTL model by looking for merge-points as early as possible to reduce the size of equivalence checking problems. This method however is suggested for hand crafted RTL codes. In addition, it makes use of cut-loop techniques which are inapplicable to pipelined designs as will be discussed in Section 2.

Lots of work has been performed for equivalence checking of generated RTL using HLS tools against its specification [5, 10, 11, 12, 13, 14]. The authors of [5] have...
used a bi-simulation correspondence checking to validate designs generated by the SPARK behavioral synthesis tool. A suite of optimizations for the SEC framework has been presented by [10] which exploit both the explicit control and data flow representations in the Clocked Control and Data Flow Graph (CCDFG) and the module structures in the ESL description. The authors of [12] proposed a SEC framework to compare an ESL design with its behaviorally synthesized RTL in the presence of optimizations such as operation gating and global design variables. The work in [13] has tried to solve the equivalence checking problem for compiler transformations in behavioral synthesis.

The process of behavioral synthesis consists of several transformation phases including compilation, scheduling, allocation, binding, and control generation [6, 18]. On the other hand, when the target design must be pipelined, loop pipelining is employed as part of scheduling and binding phases which results in several challenges, such as overlapping execution, retiming, forwarding, and losing direct one to one mapping between the specification and the pipelined RTL. Hence, traditional sequential equivalence checking approaches are becoming inefficient. Despite the existence of numerous methods to verify pipelined microprocessors [15, 16, 17], there are a few published approaches on formal equivalence checking of behaviorally synthesized pipelined loop designs.

The comparison of input-output relations between the specification and the high level synthesized pipelined RTL is prohibitively expensive for loops with many iterations. A reference pipelining transformation on the CCDFG was proposed in [11] to deal with the problem of loop pipelining without using approaches based on input-output comparison. The proposed method is based on building reference pipeline model with a certified specific transformation and checking the equivalence between the reference model and synthesized RTL using dual-rail symbolic simulation. However, it requires several parameters whose values are needed to be obtained from the HLS tool. Additionally, although it can handle SEC of pipelined designs with nested loops, it cannot make use of proposed SEC optimization techniques for internal loops and hence has to unroll internal loops. The authors of [14] solved the problem of equivalence checking for function pipelining (instead of loop pipelining) in behavioral synthesis.

Tackling the equivalence checking problem of high level synthesized designs, requires a scalable representation model. In recent years, a strong and scalable high-level decision diagram called M-HED has been proposed [25, 27, 33]. This decision diagram has a compact and a canonical form, and is also close to high-level descriptions of a design. The other properties of M-HED such as a facility for expressing primary outputs of a design in terms of primary inputs in a polynomial form, presenting state variables in terms of integer equations in a formal model, and availability of arithmetic operations in a word-level, has made it a powerful and scalable platform for verification [25, 27, 33, 37, 41, 42].

In this technical report, we present a scalable formal equivalence checking methodology for pipelined loop designs synthesized at high level while nested loops are pipelined and no information from the HLS tool is necessary. The short version of the presented method has been published in [45] as a ASP-DAC paper. In this version, we describe our proposed method in more details with several examples. As Figure 1 shows, first we perform a symbolic simulation to create a list of assignments of specification (LAASC) and behavioral synthesized design when all loops are pipelined (LAPRTL). These lists completely describe the behavior of specification and implementation. For equivalence checking, we employ an efficient canonical hybrid bit- and word-level decision diagram called M-HED [25, 27, 33]. The key idea to increase the scalability of our framework is to avoid cost-prohibitive input-output comparison by introducing dynamic cut-points instead of fixed cut-points used in [28].

Although the authors of [28] used BDDs and cut-loops for equivalence checking, their method is not able to handle large designs and those designs that contain pipelined loops. As we stated before, loop pipelining is one of the most intricate transformations [40] that arises challenges in developing automated equivalence checking methods. In addition, unlike the method presented in [11], these cut-points are not operation mapping between the specification and the RTL design. Moreover, in contrast with [11], our proposed method doesn’t need several parameters whose values are obtained from HLS tool and also doesn’t make use of sophisticated concepts of formal verification such as theorem proving for certification framework. This property allows other researchers to understand and replicate it easily. The cut-points in our method are inserted into parts of the code where the size of its corresponding M-HED is maximized. This way, the design is divided into several smaller segments. Therefore, the size of the equivalence checking problem significantly reduces. We continuously check the equivalence of corresponding segments from specification list and pipelined loop synthesized implementation list to detect the equal nodes. Then, we cut out the equivalent nodes and introduce them as new primary inputs for the rest of the segments. These primary inputs are used while next segments should be checked. If no match is found while comparing segments, we make use of an internal equivalence approach that enables us to incrementally remove outputs of corresponding segments, expose temporary nodes as new output nodes, and explore them to check whether they are equivalent or not.

We employ CatapultC [1] as an HLS tool to automati-
Hence directly using of several optimizations such as cut-as controlling finite and out-

pears. It means that i+1

the overlapping execution of consecutive iterations ap-

while loop when both inner and middle loops are pipelined is

tion interval is one, the result of a single iteration of outer

iteration of the outer loop when none of the middle and

level nested loops shown in Figure 2. The result of a single

ion that allows the next

ditions and lastly one multiplication must be performed.

Figure 5. The RTL schematic is obtained by CatapultC[1]

when the specification is synthesized at the frequency of

0 MHz. In each iteration, four multiplications, two add-

ditions and lastly one multiplication must be performed.

In this case, one can use fixed cut-loop optimization tech-

ique for equivalence checking. That is because an iter-

ation of specification equals to two cycles of implementa-

tion.

Figure 2. An example of a pair of three-level nested loop.

Figure 3. Execution order of three-level nested loops with no pipeline

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with when a C code is synthesized into RTL code, let us

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Figure 4. Execution order of tree-Level nested loops (a) when middle

and inner loops are pipelined, (b) when outer, middle, and inner

loops are pipelined.

In other words, the symbolic values on a cut in the spec-

ification always equal to the symbolic values of a specific
cut in the implementation. However, when a design is

pipelined such a correspondence is lost and it would not

be possible to determine fixed cut-loops. In the fixed cut-

loop we must be able to find a location in such a way that
always after a fixed number of cycles in the implementa-

tion, all points in the specific cut of implementation and

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tion.
Suppose that five multipliers and two adders are available during the high level synthesis phases. Hence, four multiplications in the second iteration of the inner loop (Figure 5) are being computed before the computation of the first iteration is finished. Such reordering deprives us of the opportunity to select a fixed cut-loop in the implementation (cutIi; i = 1 to 6 in Figure 6) and the specification (cutSi; i = 1 to 6 in Figure 6) in such a way that a regular behavior in the ordering of operations in the implementation and the specification is observed. For example, suppose that we want to find a corresponding cycle in the implementation for the first iteration of the specification (i.e., cutS3) and check whether this cycle can be used as a fixed cut-loop or not. By moving forward in successive cycles of the implementation, cutI3 is found. But several multiplication and addition operations in cutI3 have no corresponding operations in the cutS3 of specification. Based on definition of cut-loop in Section 2, the cutI3 cannot be considered as a cut-loop because no equivalent statement for other statements in cutI3 can be found in cutS3. With proceeding in remaining cycles of the implementation we observe that neither cutI3 nor any other cuts can be used as a cut-loop in a way that always after fixed number of cycles all statements in that cut become equivalent to all statements in a specific cut in the specification. This example shows that in the case of pipelined loop implementation, using optimization techniques such as cut-point, cut-loop, or cut-plane for equivalence checking purposes are not straightforward. These challenges motivate us to come up with an efficient methodology for equivalence checking between the specification and synthesized pipelined loop implementation.

3. **Modular Horner Expansion Diagram (M-HED)**

In order to make this paper self-contained, we introduce a graph-based representation called Horner Expansion Diagram (HED) for functions with a mixed Boolean and integer domain, and an integer range to represent arithmetic operations at a high level of abstraction [25, 33]. By contrast, other Word Level Decision Diagrams (WLDDs) are graph-based representations that provide a concise representation of integer-valued functions defined over binary variables as a bit vector. On the other hand, Binary Decision Diagrams (BDDs) or Satisfiability (SAT) based methods suffer from size explosion problems when designs grow in size and complexity. BDD-based verification tools have not been very successful for designs containing large arithmetic data-path units due to prohibitive memory requirements. In HED, we assume that the set of variables is totally ordered and all vertices that have been constructed obey this ordering.

Figure 5. Using a high level synthesis tool (CatapultC) to generate RTL without pipelining nested loop.

Figure 6. Demonstration of inability to use fixed cut-loops in order to check the equivalence of specification and pipelined RTL implementation when loops are unrolled.
been drawn in Figure 8(c).

In Figure 8(b), \(24 \cdot 6x \cdot 6z\) based on \((1)\), \(\text{const}\) and \(\text{linear}\) parts will be 24-8z+12y+12yz and -66xz, respectively. The \(\text{linear}\) part is decomposed w.r.t. variable \(x\) again due to \(x\) sub-monomial. After that, the decomposition is performed w.r.t. variable \(y\) and then \(z\) as shown in Figure 8(b). In order to reduce the size of the \(\text{HED}\) representation, redundant nodes are removed and isomorphic sub-graphs are merged. In Figure 8(b), 24-8z, 12+12z and -6z are rewritten by \(8[3+z(-1)], 12[1+z(1)]\) and \(-6[0+z(1)]\), respectively. In order to normalize the weights, \(\gcd(12,12) = 12\), \(\gcd(8,12) = 4\) and \(\gcd(-6,-6) = -6\) are taken to extract common factors. Finally, Figure 8(c) shows the normalized graph where \(\gcd(-4,-6) = 2\) is taken to extract the common factor between out-going edges from \(x\) node. In this representation, dashed and solid lines indicate \(\text{const}\) and \(\text{linear}\) parts, respectively. Note that in order to have a simpler graph, paths to 0-terminal have not been drawn in Figure 8(c).

\[ F(X, Y, \ldots) = F(X=0, \ldots) + X \cdot F(Y=0, \ldots) + \ldots = \text{const} + X \cdot \text{linear} \quad (1) \]

The \(\text{HED}\) is a directed acyclic graph \(G = (\text{VR}, \text{ED})\) with vertex set \(\text{VR}\) and edge set \(\text{ED}\). While the vertex set \(\text{VR}\) consists of two types of vertices; Constant (C) and Variable (V), the edge set indicates integer values as weight attribute. A Constant node \(v\) has as its attribute a value \(\text{val}(v) \in \mathbb{Z}\). A Variable node \(v\) has as attributes an integer variable \(\text{var}(v)\) and two children \(\text{const}(v)\) and \(\text{linear}(v) \in \{V, C\}\).

### 3.1 Reduction Rules and Canonicity

Analogous to BDDs and \(*\text{BMDs}\), \(\text{HED}\) can be reduced by removing redundant nodes and merging isomorphic nodes. In order to do so, the following reduction rules have been employed:

**Rule 1:** Remove a node if its \(\text{linear}\) portion (right child) is 0-terminal or its right edge has 0 weight. Then replace this node with its \(\text{const}\) portion (left child). Figure 7(a) illustrates this situation where node \(v\) contains only \text{const} part and therefore the function computed at that node is independent of variable \(\text{var}(v)\).

**Rule 2:** Merge isomorphic nodes. This merging rule identifies isomorphic sub-graphs. Two nodes are isomorphic if they not only have the same \(\text{const}\) and \(\text{linear}\) portions but also their variable IDs should be the same. Figure 7(b) shows that nodes \(v1\) and \(v2\) are isomorphic and then merged together as a new node \(v\).

Figure 8 illustrates how \(f(x, y, z) = 24 \cdot 6x \cdot 6z\) is represented by the \(\text{HED}\). \(\text{HED}\) is a binary graph level representation where the algebraic expression \(F(X, Y, \ldots)\) is expressed by a first-order linearization of the Taylor series expansion \([30]\). Suppose variable \(X\) is the top variable of \(F(X, Y, \ldots)\). Equation (1) shows \(F(X, Y, \ldots)\), where \(\text{const}\) is independent of the variable \(X\), while \(\text{linear}\) is the coefficient of variable \(X\).

In this graph basic arithmetic operators such as addition, unary addition, subtraction, unary subtraction and multiplication are available that work for symbolic integer variables. In order to represent Boolean functions, logical bitwise operations including \(\text{NOT, AND, and OR}\) have been provided that are discussed in the following subsections \([32, 33]\).

### 3.2 Boolean Logic

In order to have an integrated representation of Boolean and integer variables, the logical operations need to be supported as well as arithmetic expressions. Boolean operations are defined based on the arithmetic operations illustrated in Figure 9. To address bit-slicing problem, in \([32]\) we have introduced a hybrid method to check the equivalence between a high level specification and the RTL implementation. In our hybrid equivalence checking approach, we have proposed a decomposition technique as shown in Figure 10 that enables us to deal with bit-slicing problem. The main idea is those word-level variables whose bit-slices are used in the Boolean part of the design are decomposed into other word-level variables. For example, if \(i\)-bit of variable \(\text{Tmp}\), i.e. \(\text{Tmp}[i]\), is used in the Boolean part, the related word-level variable, i.e., \(\text{Tmp}\), is decomposed into other word-level variables according to \(\text{Tmp} = 2 \cdot \times \text{Tmp} + \times \times \text{Tmp} + \times \times \times \text{Tmp}\), where \(\text{Tmp}\) and \(\text{Tmp}\) are new integer variables and \(y\) is \(\text{Tmp}[i]\).

### 3.3 Arithmetic Operations

Addition (\(W = X + Y\)) and subtraction (\(W = X - Y\)) can be represented canonically based on decompositions in (2) and (3) respectively, as shown in Figure 11(a) and Figure 11(b):

\[ W = X + Y = X + \star(1) + X \star(1) \quad (2) \]
\[ W = X - Y = X + -\star(1) + X \star(1) \quad (3) \]

Multiplier (\(W = X \cdot Y\)) can be represented canonically based on (4), as shown in Figure 11(c).

![Figure 7. Reduction rules: (a) redundant nodes, (b) isomorphic sub-graphs.](image)

![Figure 8. HED representation of 24-8z+12y+12yz-6x-6xz: (a) decomposition with respect to variable \(x\), (b) decomposition with respect to variables \(x\) and \(y\), (c) decomposition with respect to variables \(x\), \(y\) and \(z\).](image)
The following cases should be considered

\[ W = X \cdot Y = 0 + X \cdot (Y) = 0 + X[0 + Y \cdot (1)] \tag{4} \]

1. \( \text{NOT} \ x \Rightarrow 1 - x \)
2. \( x \text{ AND} y \Rightarrow x \cdot y \)
3. \( x \text{ OR} y \Rightarrow x + y - x \cdot y \)

Figure 9. Logical operations in HED graph.

In order to describe how arithmetic operators such as addition and multiplication are applied to two HED nodes and as a result a new node is generated, let \( u \) and \( v \) be two nodes to be composed, resulting in a new node \( q \). Let \( \text{var}(u) = x \) and \( \text{var}(v) = y \) denote the decomposing variables corresponding to the two nodes to be decomposed. The following cases should be considered:

1. If both nodes are \( \text{Constant} \) nodes \((u, v \in C)\), a new \( \text{Constant} \) node \( q \) is computed as follows:
   - Addition \( q = u + v \cdot \text{val}(q) = \text{val}(u) + \text{val}(v) \)
   - Multiplication \( q = u \cdot v \cdot \text{val}(q) = \text{val}(u) \cdot \text{val}(v) \)

2. If one of the nodes is \( \text{Constant} \) node \((v \in C)\), a new \( \text{Variable} \) node \( q \) is created as follows. For addition operation, the \( \text{const} \) part of result, i.e., \( q_{\text{const}} \), is obtained by adding constant \( \text{val}(v) \) to \( \text{const} \) part of \( u \) (\( u \)). The \( \text{linear} \) part of result will be \( \text{linear} \) part of \( u \) (\( u \)). For multiplication operation, \( \text{val}(v) \) should be multiplied with both \( \text{const} \) and \( \text{linear} \) parts of \( u \) (\( u \)), and \( \text{var} \) part of \( u \) (\( u \)) to create \( \text{const} \) and \( \text{linear} \) parts of the result \((q_{\text{const}} \) and \( q_{\text{linear}} \)) respectively.
   - Addition \( q = u + v \cdot q_{\text{const}} = (u + \text{val}(v)) + x \cdot u \)
   - Multiplication \( q = u \cdot v \cdot q_{\text{const}} = \text{val}(v) \cdot x \cdot u \cdot \text{val}(v) \)

3. If both nodes are \( \text{Variable} \) nodes \((u, v \in V)\), proceed according to variable order. Suppose order\((x) > \text{ordery}\).

   a. Where the two nodes are indexed by different variables, \( \text{var}(q) = \max(\text{var}(u), \text{var}(v)) = x \). For addition operation, the \( \text{const} \) part of result, i.e., \( q_{\text{const}} \), is computed by adding \( v \) node to \( \text{const} \) part of \( u \) (\( u \)). The \( \text{linear} \) part of result will be \( \text{linear} \) part of \( u \) (\( u \)). For multiplication operation, \( v \) node should be multiplied with both \( \text{const} \) and \( \text{linear} \) parts of \( u \) (\( u \)) and \( u \) to generate \( \text{const} \) and \( \text{linear} \) parts of the result \((q_{\text{const}} \) and \( q_{\text{linear}} \)) respectively.

   b. Where the nodes have the same index then \( \text{var}(q) = x \). In this case, the \( \text{const} \) part of \( q \) is created by pairing the \( \text{const} \) parts of two nodes \((u+\text{v} \) for addition and \( u \cdot v \) for multiplication). The \( \text{linear} \) part of \( q \) is obtained as a sum of two cross products of \( \text{const} \) and \( \text{linear} \) parts when multiplication should be done. Furthermore, the quadratic term, i.e., \( q_{\text{linear}} \), is taken into account in linear portion of \( q \).

   - Addition \( q = u + v \cdot q_{\text{const}} = (u + v) + x \cdot (u + v) \)
   - Multiplication \( q = u \cdot v \cdot q_{\text{const}} = \text{val}(v) \cdot x \cdot (u \cdot v) \)

### 3.4 Shift Operations

While shift left operator, \(<<\), can be viewed as scalar multiplication, shift right operator, \(>>\), can be modeled as a division by \( 2N \). In order to compute the division on HED, while assuming the divisor is a constant integer number and also powers of two, \( 2N \), the following recursive algorithm is applied until terminal cases are reached. At terminal nodes, the division is converted to a numerical division problem which is performed easily. If, however, constant values at terminal nodes are less than \( 2N \), the related variable, \( \text{Var} \), is replaced by \( \text{Var}/2N \) [34].

\[ Z = f / 2^N = (f_{\text{const}} + X \cdot f_{\text{linear}}) / 2^N = (f_{\text{const}}/2^N) + X \cdot (f_{\text{linear}}/2^N) \]

If terminal < \( 2^N \); replace \( \text{Var} \) by \( \text{Var}/2^N \)

### 3.5 Conditional Statements

In order to handle conditional statements such as if-then-else statement and case statement, variables from different branches of conditional statements are rewritten by different indices (e.g., \( \text{variable } \) \( m \) is defined as \( n1, n2, \ldots, nm \) variables for \( m \) cases to consider both if and else parts in different iterations). Then these new variables are added to the design in place of conditional statements as shown in Figure 12.

![Conditional Statements](image)

### 3.6 Modular Horner Expansion Diagram (M-HED)

In order to verify polynomial data paths over bit-vectors, we have extended the HED to manipulate modular arithmetic [25]. Although the equivalence verification over \( Z \) is known to be NP-hard when \( m \geq 2 \) [29], analyzing polynomials over arbitrary finite integer rings and their properties are useful to deal with the equivalence checking problem [20]. The theory of univariate vanishing polynomials over \( Z_m \), \( m \in \mathbb{N}, m>1 \); i.e., those polynomials \( f \) such that \( f(x) \mod m = 0 \), has been presented in [24]. The authors of [26] have extended the concepts of the work [24] and derived a unique form representation of a multivariate polynomial over finite integer rings of the form
\( \mathbb{F}_p^* \), where \( p \) is any prime integer. Let us consider a simple example that defines functions \( f[3:0] = 15Y[3:0] - 5Y[3:0] + 19Y[3:0] + 6 + 3Y[3:0] + 6 \) and \( f[3:0] = 7Y[3:0] + 3Y[3:0] + 3Y[3:0] + 6 \). While \( f \) is not equivalent to \( f \) as polynomial functions over \( \mathbb{F}_p^* \), they are equivalent over \( \mathbb{Z}_p^* \), i.e. \( f \mod 2 = f \mod 2 \). Computing their difference over \( \mathbb{Z}_p^* \), results in \( f[3:0] - f[3:0] = 8Y[3:0] - 8Y[3:0] + 16Y[3:0] \). While the result is non-zero polynomial, \((8Y^2 - 8Y^2 + 16Y)\mod 16 = 0, \forall Y \in \{0,1,\ldots,15\} \) and we say \( 8Y^2 - 8Y + 16Y \) vanishes in \( \mathbb{Z}_p^* \). In general, it is not straightforward at all to see whether given polynomials are vanishing ones or not. Actually, a straightforward approach which expands everything into Boolean domain does not clearly work.

We have discussed how the properties of polynomial functions over finite integer ring allow us to reduce two polynomial functions to a canonical form based on the HED [25]. We follow the basic idea proposed in [22] but make use of the HED for efficient implementations and manipulations of polynomials with fixed bit-width that results in a new package called M-HED. Therefore, equivalent polynomial functions over finite integer rings, i.e., data paths with finite bit-width in hardware designs, are automatically identified due to the canonical representation of the M-HED. Since we only use the M-HED to check the equivalence between two polynomials over finite word-length, and manipulating polynomials with fixed bit-width is not our contribution in this paper, we will not discuss further details and we refer the interested reader to our previous work [25].

4. Proposed Equivalence Checking Approach

In this section we explain our methodology in more details. First, it is worthwhile explaining how a specification and an RTL implementation with pipelined loop are converted to a list of assignments, so they can be represented by M-HED.

4.1 Symbolic Simulation

Algorithmic Specification in C (ASC) and RTL with pipelined loop in Verilog generated by CatapultC (PRTL) are treated as inputs of SEC-PIPED algorithm. Then execution of specification and implementation are translated into several assignments by using symbolic simulation (SymSim function in lines 1-2 of Figure 15). In symbolic simulation, symbolic values rather than concrete ones (integer or binary values) are used as input vectors. As a clarifying example, consider the C code of 4-point FFT shown in Figure 13. The intent of this code sequence is to perform the butterfly computations with three main loops. The outside loop counts through 2 stages of the FFT computation and it causes huge data-dependent computations. The inner loops perform the individual butterfly computations of each stage. The heart of the FFT algorithm is the block of the code that performs each butterfly computation in the third loop. Note that \( w \) and \( w_\text{p} \) parameters are commonly known as twiddle factors and can be computed before the algorithm is fulfilled. To symbolically simulate such a code, the loops are unrolled and therefore a list of assignments is obtained. Then, controlling assignments are removed and the indexes of the arrays are adjusted. Figure 14 illustrates the list of assignments after removing controlling assignments and adjusting the indexes of the arrays in such a way that multiple assignments to a single variable don’t happen while data dependencies are preserved. The result of symbolic simulation is a list of assignments which exactly mimics the behavior of given C code. In a similar manner, RTL codes are symbolically simulated.

Note that in the list of assignments, we have three variable types; inputs which are appearing only on the right hand side, outputs which are only in the left hand side and intermediate signals which are in both sides. The objective of equivalence checking is to check whether the functionality of the output variables in the generated assignment list according to the specification and implementation are equivalent or not.

```c
//buttefly computation
for (index = j; index < 4; index = index + len1)
    index2 = index + len;
    tmr = aar[index] - aar[index2];
    tmi = aai[index] - aai[index2];
    aar[index] = aar[index] + aar[index2];
    aai[index] = aai[index] + aai[index2];
    if (windex == 0)
        aar[index2] = tmr;
        aai[index2] = tmi;
    else
        aar[index2] = tmr*C - tmi*S;
        aai[index2] = tmr*S + tmi*C;
    windex = windex + iner;

Figure 13. 4-point FFT specification.
```

4.2 SEC Algorithm using M-HED

As mentioned in Section 2, the main idea is introducing dynamic cut-points (CPs) to deal with reordering and out of order execution problem. In addition, CPs divide the list of assignments into several smaller segments making large designs tractable by M-HED.
In other words, dynamic CP insertion increases the scalability of M-HED for addressing equivalence checking problem. Selecting the right number and location of CPs is a challenge. While choosing too few CPs leads to a blow up of the forward M-HED construction, choosing too many CPs results in lots of re-substitutions for false negative elimination. In our proposed method, in an iterative way, a CP is inserted in a location so that the size of corresponding M-HED becomes as large as possible. This way, two segments are generated.

One segment in which the corresponding M-HED size is equal to the maximum allowed M-HED size and the other one in which the corresponding M-HED size can be even larger than the maximum allowed M-HED size. The first generated segment of the specification (\texttt{sasc}) and the implementation (\texttt{sprtl}) are compared to check for equivalency. Although in HLS due to resource sharing, the mapping between specification and RTL implementation usually is many to one, it is not necessary to compare each node in the segment of specification with all nodes in the segment of RTL implementation. That is because we make use of a canonical decision diagram, i.e. M-HED, so that two nodes that are functionally equivalent are automatically detected. In each iteration of the SEC-PIPE algorithm, the following operations are done.

If \texttt{LAASC} is not empty (line 6 of Figure 15), we insert a CP in the assignment list. As a result, two segments are generated. The size of corresponding M-HED of the first segment (\texttt{sasc}) is equal to the maximum size allowed by M-HED. A segment in \texttt{LAASC} (\texttt{sasc}) is chosen by \texttt{segmentSelector} function and removed from \texttt{LAASC} (lines 7-8). Next, M-HED of all statements in \texttt{sasc} is created (\texttt{Hsasc} in line 9). In the same way, if \texttt{LAPRTL} is not empty (line 13), a CP is inserted in \texttt{LAPRTL}. Then a segment in \texttt{LAPRTL} (\texttt{sprtl}) is chosen by using \texttt{segmentSelector} function again and removed from \texttt{LAPRTL} (lines 14-15). Next, M-HED representation of \texttt{sprtl} (\texttt{Hsprtl}) is created (line16).

Please note that the maximum size of a design that can be handled by M-HED is dependent on the structure of design. Typically, M-HED can handle 30000 assignment lines. Based on this information as well as the structure of designs to be verified the proper location of CP is automatically determined. After creating \texttt{Hsasc} and \texttt{Hsprtl}, they are compared using M-HED and the equivalent output nodes are specified by \texttt{eo} (line 20). As mentioned in Section 4-1, the output nodes are those that appear only the left-hand side in a segment. As a result of equivalence checking, the equivalent output nodes as well as those nodes that equivalent outputs are dependent on them (\texttt{dni} and \texttt{dns}) are removed from \texttt{sasc} (lines 24-26) and \texttt{sprtl} (lines 29-31). New primary inputs for equivalent nodes in their places are introduced that are used in the next segments of \texttt{LAASC} and \texttt{LAPRTL}. Note that remaining segments are updated using \texttt{UpdateSegment} function in lines 27 and 32 in order to reflect the effect of these new primary inputs.

**Figure 14. List of assignments after symbolic simulation, removing controlling variables and adjusting array indexes.**

\begin{verbatim}
len = 4; incr = 1;
//stage = 0
len1 = 4; len = 2; windex = 0;
//j=0
C = wr[0]; S = wi[0];
index = 0; index2 = 1;
tmr = aar[0] - aar[2];
aar[0] = aar[0] + aar[2];
aar[2] = tmr;
aai[2] = tmi;
index = 1; index2 = 3;
tmr = aar[1] - aar[3];
tmi = aai[1] - aai[3];
aai[1] = aai[1] + aai[3];
aar[3] = tmr*C - tmi*S;
aai[3] = tmi;
index = 2; index2 = 3;
tmr = aar[0] - aar[1];
tmi = aai[0] - aai[1];
aai[0] = aai[0] + aai[1];
aar[1] = aar[1] + aar[1];
aar[1] = tmr;
aai[1] = tmi;
index = 2; index2 = 3;
tmr = aar[2] - aar[3];
tmi = aai[2] - aai[3];
aai[2] = aai[2] + aai[3];
aar[2] = tmr;
aai[2] = tmi;
index = 3; index2 = 3;
tmr = aar[0] - aar[0];
tmi = aai[0] - aai[0];
aai[0] = aai[0] + aai[3];
aar[3] = tmr*C - tmi*S;
aai[3] = tmi;

Figure 15. Sequential equivalence checking (SEC) of pipelined data path designs.

Another point to be noted here is that removing internal nodes when they have impact on equivalent nodes is not always safe. That is because these nodes...
may also have impact on other nodes that are checked yet. Replacing them with primary inputs would remove useful correlation among other nodes. To avoid this unsafe operation, during updating remaining segments by UpdateSegment function, if internal nodes are used in unprocessed segments, they are described in terms of primary inputs. To do so, we utilize useful embedded feature of M-HED described in Section 3 that help us to do it easily.

It should be noted that the while loop of SEC-PIPED algorithm is finished when all segments in both LAASC and LAPRTL become empty. If the last updated sasc and sprtl are empty, it means that for all output nodes in sasc, there is an equivalent node in sprtl and vice versa which necessitate the specification and implementation to be equal (lines 34-35). Otherwise they are not equivalent (line 37).

Figure 16 illustrates the main idea behind SEC-PIPED algorithm. In this figure, p, i, s and n are primary input, implementation node, specification node, and finally new primary input defined in the place of equivalent nodes. As shown in this figure, the first segment of the implementation (sprtl) and specification (sasc) are compared using M-HED. The equivalent output nodes of these segments (i, i, s, s) are detected and segments are updated by introducing new primary inputs in the place of equivalent nodes (n and n Figure 16(b)). Besides, during equivalence checking that impact on equivalent nodes are removed except nodes that may affect on other nodes to be checked (i in Figure 16(a)). These nodes are detected during updating segments and described in polynomial form in terms of primary inputs using the useful property of M-HED (p.p. in Figure 16(b)). Section 3 described how this polynomial can be written. The new segments are compared again and equivalent output nodes (i, s, in Figure 16(b)) are detected.

4.3 Finding Internal Equivalent Nodes

Suppose we follow the SEC-PIPED algorithm, but in the given segment size, no equivalent nodes exist (lines 21-23 of Figure 15). In this case no nodes can be moved from sasc or sprtl and therefore M-HED construction is blocked. Since the size of the corresponding M-HED of sasc or sprtl is equal to the maximum allowed M-HED size, in the next iteration no statement can be added to the selected segment and therefore this segment is selected again and again and the algorithm falls into an endless loop. In fact, because of several redundancies or optimizations added during pipelined RTL generation, the size of assignment lists of specification (LAASC) and implementation (LAPRTL) would be different. Hence, when we choose one pair segment for comparison (sasc and sprtl) equivalent output nodes may not exist. The question that rises in the mind of reader is whether or not our methodology can handle such a case.

In order to avoid blocking forward M-HED construction, INTERNAL-EQU algorithm shown in Figure 17 is proposed. The basic idea is to look for non-output (internal) equivalent nodes. To do so, first we compare output nodes of Htsprtl and a modified version of Htsasc while output nodes of Htsprtl and the original Htsasc are not equivalent. To obtain the modified Htsasc, sasc and sprtl are reserved in temporary locations (tasc and tsprtl in lines 1-2 of Figure 17). We omit output statements of sasc, and append these statements to LAASC (lines 9-11 of Figure 17). After such deletions, some previously intermediate nodes appear as new output nodes. Afterwards, the M-HED of the modified tasc is constructed (line 12). If all statements are removed and we are not able to obtain any new equivalent nodes, the process is repeated for tsprtl (lines 17-24). This is because output nodes of sprtl may be equivalent to internal nodes of sasc or vice versa. To perform such an operation, first, sasc is retrieved and the corresponding M-HED is reconstructed (lines 15-16). Then all processes of the first while loop is repeated for sprtl to obtain internal nodes which are equivalent to some output nodes of sasc. In this algorithm, when an equivalent pair of nodes is found, sasc, sprtl, LAASC, LAPRTL are updated and returned as results (lines 7 and 19). This way, we are able to detect equivalent nodes based on an iterative deletion approach.

Figure 16. Illustrations of the main part of SEC-PIPED function (a) when the first segments (sasc and sprtl) are compared (b) when the second segments (sasc and sprtl) are compared.
and Figure 18. Illustration of the main part of INTERNAL function (LAASC, LAPRTL, sasc, sprtl)

1. $t\text{sasc} = \text{sasc}$;
2. $t\text{sprtl} = \text{sprtl}$;
3. $H\text{sasc} = \text{HEDGen}(\text{sasc})$;
4. $H\text{sprtl} = \text{HEDGen}(\text{sprtl})$;
5. WHILE ($t\text{sasc} \neq \emptyset$)
6. IF $\text{EquChecking}(H\text{sasc}, H\text{sprtl}) \neq \emptyset$
7. RETURN LAASC, LAPRTL, tsasc, tpsprtl;
8. ELSE
9. $\text{onsasc} = \text{outputs statements in tsasc}$;
10. $\text{tsasc} = \text{tsasc - ontsasc}$;
11. $L\text{AASC} = \text{LAASC} \cup \text{ontsasc}$;
12. $H\text{sasc} = \text{HEDGen}(\text{tsasc})$;
13. END IF
14. END WHILE
15. $\text{tsasc} = \text{sasc}$
16. $H\text{sasc} = \text{HEDGen}(\text{tsasc})$;
17. WHILE ($\text{tpsprtl} \neq \emptyset$)
18. IF $\text{EquChecking}(H\text{sasc}, H\text{sprtl}) \neq \emptyset$
19. RETURN LAASC, LAPRTL, tsasc, tpsprtl;
20. ELSE
21. $\text{ontsprtl} = \text{outputs statements in tpsprtl}$;
22. $\text{tpsprtl} = \text{tpsprtl - ontsprtl}$;
23. $H\text{sprtl} = \text{HEDGen}(\text{tpsprtl})$;
24. $L\text{APRTL} = \text{LAPRTL} \cup \text{ontsprtl}$;
25. END IF
26. END WHILE
27. RETURN “UNEQUIVALENT Designs”

Figure 17. Procedure of finding internal equivalent nodes.

Figure 18 demonstrates how to use this algorithm. Suppose that the maximum size of M-HED only allows us to construct eleven nodes of implementation and six nodes of specification. As shown in Figure 18(a), because $s$ and $s$ are equivalent to $i$ and $i$, and also $i$ and $i$ are considered as internal nodes (output nodes are $i$ and $i$), no output nodes are equivalent. Hence, by using INTERNAL-EQU algorithm, output nodes of sprtl (i and i) are removed and internal nodes (i and i) are introduced as new outputs. This way, equivalent output nodes are appeared and constructing M-HED can be resumed similar to Figure 16(a) as seen in Figure 18(b).

4.4 Example

In this subsection we illustrate our methodology with an example. As mentioned before, Figure 5 and Figure 6 show a nested loop in C code as an ASC block and related synthesized hardware. As you can see in Figure 5, in the ASC the results of two multiplications are added and stored in temporary variables (tempf and temps). These temporary variables are multiplied and stored in a res array. The RTL code synthesized by CatapultC is not pipelined and therefore finding cut-loop is possible.

However, Figure 6 indicates a sequence of cycles when a RTL code with a loop pipelined is synthesized. As mentioned in Section 2, pipelining makes the equivalence checking hard. Figure 19 demonstrates the three steps of equivalence checking using our methodology. In this figure, output nodes in each segment of implementation and specification are colored as blue and green respectively. Suppose that the first segment of the specification (segment.) includes temp0 and temps0 as output nodes and the first segment of the implementation (segment.) includes mul1, mul2, and add0 as output nodes. After creating M-HEDs for all assignments in these segments, add0 $\in$ segment. and temp0 $\in$ segment. are detected as equivalent nodes. However, because add1 $\notin$ segment., neither add1 nor any other node is detected as an equivalent node to temp0. At this point, a new primary input is defined instead of equivalent nodes (NEW PI in Figure 19(b)) and $\{\text{mul0, mul1, add0}\} \in$ segment. and $\{\text{temp0}\} \in$ segment. are removed.

Since $\{\text{mul1, mul2}\} \in$ segment. have no impact on add0 and $\{\text{temps0}\} \in$ segment. has no equivalent node in segment., they are not removed from segment. and segment.. In the next phase, as shown in Figure 19(b), new segments segment. and segment. are taken into account so that $\{\text{NewPI, temps0, res00}\} \in$ segment. and $\{\text{NewPI, mul2, mul3, mul4, mul5, add1}\} \in$ segment.. During equivalence checking, no output node is matched and therefore INTERNAL-EQU algorithm needs to be called. In this algorithm, first of all, output res00 is removed from segment. which makes temps0 a primary output of segment. (Figure 19(c)). Then, M-HEDs of updated segments are constructed again and SEC-PIPEd is resumed. At this point, the equivalent nodes temps0 and add1 are detected. Next, they are removed and new primary inputs are defined instead of them. This procedure is continued so that all nodes can be removed from sasc and sprtl. If all segments have been processed, LAASC and LAPRTL, and also the final sasc and sprtl have become empty, the algorithm returns EQUIVALENT Designs. As it can be observed, our proposed solution can be applied to RTL designs with pipelined nested loops and complex structure.

Figure 18. Illustration of the main part of INTERNAL-EQU function. (a) before finding internal-equivalent nodes when the first segments (sasc and sprtl) are compared. (b) after finding internal-equivalent nodes when the first segments (sasc and sprtl) are compared.
5. **Limitations of Proposed Methodology**

False negatives are failing properties that unintentionally raise a wrong flag as a sign of unequal design while there is no bug in the design. Verification engineer must eliminate false negatives to make sure only real bugs lead to failing properties [19]. It is well known that using each type of cut-points in each kind of decision diagrams and even equivalence checking approaches can potentially lead to false negatives. In the proposed methodology we try to avoid false negatives in different ways.

First, we move nonequivalent nodes in a given segment \( i \) into another segment \( j \) and repeat the checking process until nodes become equivalent or all segments are covered (i.e. at the end of statements). In fact, our methodology doesn't decide about the results of equivalence checking immediately after finding nonequivalent nodes in a pair of checked segments. Because two nodes in a specific \( sas \) and \( sprtl \) (e.g. \( sas \) and \( sprtl \)) may not be equivalent, while moving a node from \( sas \) into \( sas \), we can find equivalent nodes (like \( tempsd \) in Figure19). The scalability of the proposed methodology can be kept by removing equivalent nodes and nodes that effect on them. These eliminations reduce the size of equivalence checking significantly.

Second, whenever internal nodes those effect on equivalent nodes as well as other nodes in the unprocessed segments are removed, new inputs are introduced instead of them. These inputs are described in terms of primary inputs of design in polynomial form using M-HED that provides facilities to avoid false negative results as much as possible (like \( i \) in the Figure16(a)). Note that false positives do not occur on M-HED due to its canonical representation.

6. **Experimental Results**

Our methodology for equivalence checking has been implemented in C++ and carried out on an Intel 2.8 GHz Corei7 with 8 GB main memory running Linux with Qt creator as an IDE. In order to demonstrate the effectiveness of the proposed equivalence checking technique, we apply our technique to several designs common in Digital Signal Processing (DSP) and multimedia applications. The benchmarks include ColorConversion as an algorithm enabling different conversion standards to be supported with the same hardware, Sobel as a convolution algorithm which is the core of many image processing algorithms, Finite Impulse Response with two sizes (FIR4, FIR32) as the most common digital filter, Discrete Cosine Transform (DCT16, DCT32) and Fast Fourier Transform (FFT32, FFT64, FFT256, FFT512). These designs come from a variety of problem domains such as mathematics, digital signal processing and multimedia. Furthermore, we employ CatapultC as an HLS tool to automatically generate RTL codes from C code of these benchmarks[1]. Each circuit has been piped in a certain frequency. In addition we use Minisat [35] as a SAT-solver and Z3 [36] which is generally considered the fastest SMT solver. The time out (TO) is set to 1000 seconds.

Table I shows the experimental results with and without using our methodology. The first column (Benchmark) is the benchmark name. The second column (#LRTL) shows the number of RTL lines of each benchmark generated by CatapultC. The Third column (#LS) shows the number of lines obtained after symbolic simulation. Loop information column indicates the loop information such as the number of single, 2-nested and 3-nested loops in the design. The major column **without our methodology** shows the results when primary outputs are directly expressed in terms of primary inputs and then represented by M-HED. The last major column, **with our methodology**, shows the results in terms of memory usage (MemoryUsage) and required processing time (CpuUsage) after applying the proposed method.

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**Figure 19. Demonstration of steps of our proposed equivalence checking methodology**
dissimilar theories such as solvers with different mathematical theories. In these solvers on arithmetic designs by combining SAT III. SMT form to represent symbolic expressions but also is scalable. To verify our method not only uses an efficient canonical as Boolean SAT based technique but also reduces the run time significantly even for small circuits. Obviously, when using our methodology, the run time for equivalence checking is reduced by 111.9× on average, i.e., two orders of magnitude of average speedup. As opposed to low level methods such as Boolean SAT based techniques, the results indicate that our method not only uses an efficient canonical form to represent symbolic expressions but also is scalable even on large circuits.

| Benchmark   | # LRTL | #LS | Loop information | without our methodology | with our methodology |
|-------------|--------|-----|------------------|-------------------------|----------------------|
|             |        |     | Singles | 2-nested | 3-nested | MemoryUsage (MB) | CpuTime (s) | MemoryUsage (MB) | CpuTime (s) |
| ColorConversion | 141    | 712 | 0         | 1         | 0        | 1                   | 0.1         | 1              | 0.1         |
| FIR4        | 170    | 848 | 2         | 0         | 0        | 1.9                 | 0.2         | 1.9             | 0.2         |
| FIR32       | 243    | 2212| 2         | 0         | 0        | 5.2                 | 6.1         | 2.6             | 1.3         |
| DCT16       | 854    | 3996| 0         | 0         | 2        | MO                  | NA          | 5.2             | 6.1         |
| DCT32       | 1258   | 6352| 0         | 0         | 2        | MO                  | NA          | 11.7            | 9.2         |
| Sobel       | 2268   | 9765| 0         | 3         | 0        | MO                  | NA          | 12.1            | 12.7        |
| FFT32       | 2742   | 10156| 0          | 0         | 1        | MO                  | NA          | 15.6            | 14.2        |
| FFT64       | 2986   | 14258| 0          | 0         | 1        | MO                  | NA          | 38.5            | 31.1        |
| FFT256      | 3378   | 32568| 0          | 0         | 1        | MO                  | NA          | 89.5            | 82.7        |
| FFT512      | 3976   | 88682| 0          | 0         | 1        | MO                  | NA          | 121.6           | 219.2       |

(MO : Out of 8GB memory; NA : Not applicable, due to the memory out, time is not reported; CPU time is given in seconds)

As the results show, in some cases (ColorConversion, FIR4, and FIR32) without our methodology and with our methodology can handle the problem of equivalence checking, but in other cases our methodology can handle it efficiently, while without our methodology, we have faced with memory out (MO) problem. These results convince us that equivalence checking without our methodology is prohibitively expensive and even impossible for large designs. Furthermore, as stated in Section 2, directly using of several optimizations for equivalence checking such as cut-loop and cut-plane techniques is inapplicable when the loops of the design is pipelined. In this situation, our methodology can solve the problem of equivalence checking efficiently. In fact, M-HED can represent arithmetic operations at word level representation and there is no need to encode them to bit-level operations. Besides, it can handle bit-level operations as well as word level. Indeed M-HED is a strong and scalable decision diagram for representing and verification of datapath circuits [27, 30].

In another experiment, we have tried to solve the equivalence checking by using a SAT-solver. The results reported in Table II show that using SAT-solvers in datapath circuits especially with many arithmetic components is inefficient. As it can be seen, using SAT increases verification run time significantly even for small circuits. Obviously, when using our methodology, the run time for equivalence checking is reduced by 111.9× on average, i.e., two orders of magnitude of average speedup. As opposed to low level methods such as Boolean SAT based techniques, the results indicate that our method not only uses an efficient canonical form to represent symbolic expressions but also is scalable even on large circuits.

In order to complete the set of results, we compared our results against using Z3 as an SMT-solver in Table III. SMT-solvers try to handle the weakness of SAT-solvers on arithmetic designs by combining SAT-solvers with different mathematical theories. In these engines, the input design is first simplified by using different theories such as linear arithmetic, theory of arrays, and bit-vectors approaches.

| Benchmark   | # LRTL | #LS | Loop information | without our methodology | with our methodology |
|-------------|--------|-----|------------------|-------------------------|----------------------|
|             |        |     | Singles | 2-nested | 3-nested | MemoryUsage (MB) | CpuTime (s) | MemoryUsage (MB) | CpuTime (s) |
| ColorConversion | 141    | 712 | 0         | 1         | 0        | 1                   | 0.1         | 1              | 0.1         |
| FIR4        | 170    | 848 | 2         | 0         | 0        | 1.9                 | 0.2         | 1.9             | 0.2         |
| FIR32       | 243    | 2212| 2         | 0         | 0        | 5.2                 | 6.1         | 2.6             | 1.3         |
| DCT16       | 854    | 3996| 0         | 0         | 2        | MO                  | NA          | 5.2             | 6.1         |
| DCT32       | 1258   | 6352| 0         | 0         | 2        | MO                  | NA          | 11.7            | 9.2         |
| Sobel       | 2268   | 9765| 0         | 3         | 0        | MO                  | NA          | 12.1            | 12.7        |
| FFT32       | 2742   | 10156| 0          | 0         | 1        | MO                  | NA          | 15.6            | 14.2        |
| FFT64       | 2986   | 14258| 0          | 0         | 1        | MO                  | NA          | 38.5            | 31.1        |
| FFT256      | 3378   | 32568| 0          | 0         | 1        | MO                  | NA          | 89.5            | 82.7        |
| FFT512      | 3976   | 88682| 0          | 0         | 1        | MO                  | NA          | 121.6           | 219.2       |

(MO : Out of 8GB memory; NA : Not applicable, due to the memory out, time is not reported; CPU time is given in seconds)

Table II. Improvements in comparison with SAT-based method

| Benchmark   | Using SAT | Improvements by using our methodology |
|-------------|-----------|----------------------------------------|
|             | MemoryUsage (MB) | CpuTime (s) | MemoryUsage (MB) | CpuTime (s) |
|             | MemoryUsage (MB) | CpuTime (s) | MemoryUsage (MB) | CpuTime (s) |
| ColorConversion | 9.2     | 411×         | 9.2×    | 411×          |
| FIR4        | 10.1    | 54.6          | 5.3×    | 273×          |
| FIR32       | 28.2    | 121           | 10.9×   | 93.1×         |
| DCT16       | 32.2    | 301.2         | 6.2×    | 49.4×         |
| DCT32       | 47.2    | 518.6         | 4.1×    | 56.4×         |
| Sobel       | 78.2    | 872.7         | 6.5×    | 68.7×         |
| FFT32       | 87.2    | 923.5         | 5.6×    | 65.1×         |
| FFT64       | NA      | TO            | NA      | 48.2×         |
| FFT256      | NA      | TO            | NA      | 36.3×         |
| FFT512      | NA      | TO            | NA      | 18.3×         |

Average Improvement by using our methodology | NA | 111.9×

TO: Out of 1000 sec; NA: Not applicable, due to the timeout, the memory usage is not reported

Hence, the remaining instance is smaller and easier to solve. Although the most useful theories in equivalence checking are related to bit-vector and array, in small cases, using these theories for abstraction and simplification versus solving the problem by M-HED is a time-consuming task and therefore the run time increases. For DCT16 and DCT32 benchmarks, the results obtained by SMT-solver are better than those of M-HED. That is because, in these benchmarks, the synthesized designs have many bit-level descriptions. Although M-HED has features to handle bit-level operations efficiently, SMT-solvers are strong and powerful tool for verification when word-level and many bit-level operations are mixed in a single design. In comparison with M-HED, they are not good enough to handle datapath designs which are described mostly in word level. In addition, without using our methodology, word level engines cannot handle the equivalence checking problem of datapath pipelined loop design.
In this paper, we have introduced a formal equivalence checking methodology for behavioral synthesized pipelined designs with nested loops based on a canonical decision diagram called M-HED that supports modular polynomial computations. For increasing the scalability of our methodology, we employ dynamic cut-points which enable us to effectively perform sequential equivalence checking. To the best of our knowledge, this is the first work that formally checks the equivalence of pipelined nested loops by using high level decision diagrams. The experimental results demonstrate that our proposed methodology can support designs with arbitrary structures and large data path. Average improvements in terms of the memory usage and run time in comparison with SMT- and SAT-based equivalence checking are 16.7x and 111.9x respectively.

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