Predictive Data Race Detection for GPUs

Sagnik Dey*
mail.sagnik.dey@gmail.com
Department of Mathematics and Statistics
Indian Institute of Technology Kanpur, India

Parth Sharma
prthsharma20@iitk.ac.in
Department of Computer Science and Engineering
Indian Institute of Technology Kanpur, India

Mayant Mukul*†
mayantmukul@gmail.com
Dream11, India

Swarnendu Biswas
swarnendu@cse.iitk.ac.in
Department of Computer Science and Engineering
Indian Institute of Technology Kanpur, India

Abstract
The high degree of parallelism and relatively complicated synchronization mechanisms in GPUs make writing correct kernels difficult. Data races pose one such concurrency correctness challenge, and therefore, effective methods of detecting as many data races as possible are required.

Predictive partial order relations for CPU programs aim to expose data races that can be hidden during a dynamic execution. Existing predictive partial orders cannot be naively applied to analyze GPU kernels because of the differences in programming models. This work proposes GWCP, a predictive partial order for data race detection of GPU kernels. GWCP extends a sound and precise relation called weak-causally-precedes (WCP) proposed in the context of multithreaded shared memory programs to CPU kernels. GWCP takes into account the GPU thread hierarchy and different synchronization semantics such as barrier synchronization and scoped atomics and locks.

We implement a tool called PreDataR that tracks the GWCP relation using binary instrumentation. PreDataR includes three optimizations and a novel vector clock compression scheme that are readily applicable to other partial order based analyses. Our evaluation with several microbenchmarks and benchmarks shows that PreDataR has better data race coverage compared to prior techniques at practical run-time overheads.

Keywords: CUDA, concurrency errors, data races, debugging

1 Introduction
Recent GPU architectures have evolved from supporting bulk-synchronous applications to allowing fine-grained inter-thread communication [26, 27, 39]. Current synchronization mechanisms in CUDA are arguably more varied and complicated to use correctly than synchronization on CPUs. Programmers use involved mechanisms composed of barriers, fences, and atomic operations, augmented with scope qualifiers, to protect concurrent accesses to shared variables [45].

The rapidly evolving GPU architecture and the involved synchronization schemes in GPUs introduce concurrency challenges in writing correct but efficient programs. Concurrency errors, such as data races, give rise to undesired nondeterminism that can lead to incorrect output or program crashes and make debugging difficult [18, 20, 28, 37]. A data race in a GPU kernel involves concurrent accesses to the same global or shared GPU memory location with incorrect synchronization, such that both the accesses are not atomic\(^1\), and at least one access is a write. Several techniques have been proposed to detect data races in shared and global GPU memory [13, 22, 26, 27, 35, 36, 50, 73, 74].

The problem. Data races are hard to reproduce and debug as they may only manifest non-deterministically with specific thread interleavings and inputs. Therefore, it is desirable to detect as many data races as possible by observing only a few (ideally one) executions. However, rapidly evolving GPU architecture and programming models complicate reasoning about potential concurrency bugs, tripping up even state-of-the-art dynamic race detectors [13, 27, 50].

There has been a spurt of work on predictive data race detection for CPU programs [19, 23, 24, 31, 41, 42, 54, 55, 61]. Predictive techniques observe one dynamic program execution and use partial order relations to reason about valid alternate ordering among accesses to shared variables. A predictable race manifests when the events during the execution of a program can be reordered to make unsynchronized memory accesses to shared data variables happen next to each other. Dynamic predictive techniques are useful because they can scale to large programs and are sound (i.e., reports true data races). Techniques that track the happens-before (HB) relation have limited predictability, since the number of races detected is impacted by spurious ordering among concurrent events. Most existing dynamic data race detectors for GPUs are not predictive [7, 13, 22, 26, 35, 36, 50, 73, 74], i.e., they do not reason about data races in other possible interleavings. The ScoRD race detector [27] uses lockset analysis [56] and therefore has limited predictive capabilities but misses some classes of predictable data races (Section 3).

\(^1\)Atomic operations on shared memory accesses do not guarantee atomicity to regular stores to the same address.

*†Both authors contributed equally to this work.
*The author contributed to the work when he was affiliated with Indian Institute of Technology Kanpur.
**Our approach.** This work explores predictive dynamic race detection for GPUs. Predictive partial order relations for GPU kernels need to encode the programming and execution model semantics, which a direct port of CPU partial orders will fail to do. This paper proposes a predictive partial order relation, GWCP, for race detection on GPUs. GWCP is based on a sound (has no false positives) and complete (finds all races given constraints) partial order relation called weak-causally-precedes (WCP) [31] proposed for multithreaded CPU programs. GWCP builds on WCP to correctly account for modern GPU capabilities and execution semantics.

We implement PreDataR, a dynamic analysis that tracks the GWCP relation using vector clocks for CUDA programs. Using vector clocks for GPU kernels can lead to prohibitive run time and memory overheads [13]. The proposed version of PreDataR includes several key optimizations to help keep the overheads low in commonly occurring patterns by exploiting redundancies in per-thread vector clocks. PreDataR includes a flexible vector clock compression scheme that is effective in the presence of new scheduling features on NVIDIA GPUs [10]. We evaluate PreDataR against state-of-the-art dynamic data race detectors for GPUs like Barracuda [13], ScoRD [27], and iGUARD [26]. Our evaluation shows that while prior work can both miss data races and raise false alarms, PreDataR provides better data race coverage with no false positives. This work is the first to explore predictive data race detection for GPU programs to the best of our knowledge.

**Contributions.** This paper makes the following contributions.

- it explores predictive partial orders for high-coverage data race detection on GPUs
  - we show that existing race detectors either miss or report false data races with several examples;
  - the proposed GWCP relation correctly accounts for the GPU thread hierarchy and different synchronization mechanisms to report true races;
- a general vector clock compression scheme for per-thread vector clocks exploiting thread hierarchy redundancies and applicable to all vector clock based analyses
- comparison of PreDataR with state-of-the-art techniques to show improved race coverage at practical overheads
- an implementation of Barracuda that has been upgraded to deal with modern semantics such as warp-level barriers, intra warp races and scoped atomics

2 Background and Related Work

The presentation assumes NVIDIA GPUs and the CUDA programming model. However, the ideas presented should work with other GPU programming models like OpenCL [63].

| Line | Code |
|------|------|
| 1    | __global__ void kernel(int *data) {
| 2    |     data[threadIdx.x] = 2;
| 3    |     data[1 - threadIdx.x] = 1;
| 4    | } |
| 5    | int main(void) {
| 6    |     int * d_data;
| 7    |     cudaMalloc(&d_data, 2 * sizeof(int));
| 8    |     kernel<<<1,2>>>(d_data);
| 9    |     return 0;
| 10   | } |

**Figure 1.** A race exposed only with ITS. Lines 2 and 3 do not race with lockstep execution.

2.1 CUDA Programming Model

Compute Unified Device Architecture (CUDA) is a parallel programming model to accelerate GPU programs (kernels) on NVIDIA GPUs [45]. A CPU (host) driver program allocates resources, specifies the hierarchy of threads to be used (grid) and launches the kernel on the GPU. A grid consists of a 1/2/3-dimensional collection of thread blocks, and a block is a 1/2/3-dimensional collection of CUDA threads. A warp is the unit of execution on NVIDIA GPUs, typically 32 CUDA threads form a warp. All the threads in a warp execute the same program statement in lockstep on the SIMD hardware for pre-Volta architectures. From Volta onward, every thread within a warp has its own Program Counter (PC) and call stacks, relaxing the lockstep rule from older architectures, a feature known as Independent Thread Scheduling (ITS) [10].

CUDA supports barriers (e.g., __syncthreads()), atomic read-modify-write instructions (e.g., atomicCAS()), and memory fence instructions (e.g., __threadfence()) for synchronization. For atomics and fences, CUDA exposes three scope qualifiers: block, device, and system, to limit data communication to a subset of relevant threads for better performance. CUDA does not provide device-wide barriers and provides no standard method for interblock synchronization. CUDA also does not yet expose lock APIs for synchronization, although there are acquire/release PTX instructions [45]. Therefore, programmers often implement ad-hoc lock operations in CUDA: an atomic compare-and-swap followed by a fence is considered a lock acquire, and an atomic exchange preceded by a fence is considered a lock release.

Intrawarp races occur when threads from the same warp write to the same memory location. While lockstep execution implies two instructions executed by a warp cannot race, we consider synchronization-free intrawarp communication as a data race due to ITS [50] (e.g., Figure 1). Interwarp races arise when the threads are from different warps. Incorrect usage of scopes with atomics, fences, and locks also lead to data races [27]. Figure 2 shows an intrawarp data race and a race due to insufficient scope. We ignore inter-kernel data races in this work.
2.2 Dynamic Detection of Data Races

In the following, we discuss state-of-the-art techniques for dynamic data race detection on GPUs.

Barracuda [13] checks whether concurrent accesses from different threads are separated by the happens-before (HB) [32] relation extended with GPU execution semantics. The HB relation is a partial order defined over the events in a dynamic kernel trace $\alpha$. Given two events $a, b \in \alpha$ such that $a$ is before $b$ in the trace (denoted by $a <^\alpha b$), event $a$ happens before (i.e., is ordered with) event $b$ if (i) $a$ and $b$ are performed by the same thread (intra-thread order), (ii) $a$ is part of a warp that executes before $b$’s warp (interwarp order), (iii) $a$ or $b$ is a barrier, or a barrier separates $a$ and $b$, or (iv) $a$ and $b$ access the same synchronization variable where $a$ is a release and $b$ is an acquire operation, and both operations are either at the block scope within the same thread block or at least one operation is at the global scope (inter-thread synchronization). A data race occurs when $a$ and $b$ access the same location, one of the accesses is a write, the operations are not both atomic, and neither $a$ nor $b$ happen before each other.

We refer to the partial order used in Barracuda as scoped HB in future discussions.

Barracuda pushes operations executed on the GPU to a queue shared with the host, and the host consumes the operations and runs the race detection logic. Barracuda tracks intrawarp races by taking the join of all vector clocks currently active in the warp after every instruction. Barracuda considers scopes in only fence operations and ignores scopes in other synchronization operations such as atomics and locks.

CURD [50] speeds up race detection when the synchronization in the kernel only involves barriers. CURD identifies such kernels using static analysis and uses compiler instrumentation to track the read and write accesses in synchronization-free regions. CURD intersects read and write sets on the GPU to check for data races. We focus on Barracuda in this work since CURD does not aim to improve race coverage over Barracuda.

ScoRD [27] uses lockset analysis to identify scoped races induced due to misuse of lock-based critical sections. Lockset-based algorithms assume a consistent locking discipline for accessing shared variables [56], a condition difficult to enforce due to ad-hoc lock implementations. Since lockset analysis cannot detect data races in kernels that use only atomics or barriers for synchronization [50, 73], ScoRD extends the HB mechanism to detect scoped races due to barriers and atomics. ScoRD proposes hardware extensions for efficient race detection. To keep the hardware overhead bounded, ScoRD maintains metadata for every 4 B of global memory and only stores metadata for recent accesses, leading to both missed and false races. Furthermore, ScoRD maintains metadata at the warp granularity and does not detect intrawarp races.

In recent work, iGUARD [26] addresses the shortcomings of ScoRD by using binary instrumentation instead of hardware extensions. iGUARD achieves good performance by moving all race detection logic to the GPU and uses Unified Shared Memory for maintaining metadata. Besides supporting ITS, the core analysis in iGUARD is largely similar to ScoRD.

The ITS mechanism necessitates a thread-level analysis rather than a warp-level analysis. Both Barracuda and ScoRD fail to detect the race in Figure 1; Barracuda models lockstep execution within a warp and ScoRD maintains metadata at warp granularity. ITS also makes it challenging to design metadata compression schemes [13] which rely on per-thread vector clock entries being the same for all threads in a warp as individual threads can now synchronize with each other.

3 Predictive Data Race Detection

Given the non-deterministic nature of reproducing data races and the high cost in subsequent debugging [20, 28, 37], researchers have explored ways to improve race detection coverage for CPU programs (i.e., detect as many true races as possible). A few techniques randomize the thread scheduler and perturb the execution to explore different valid interleavings to maximize detecting races that can occur across schedules [8, 16, 57]. Predictive race detection techniques observe one dynamic program execution and aim to detect data races that can occur in other correct reorderings of memory.
We have also verified that using a lock to protect one of the weak-doesn’t-commute (WDC) [55], and sync-preserving races (SyncP) [42]. This work uses the WCP relation as the baseline and extends it to the GPU programming model. We ignore other partial order relations like CP and M2 since they are expensive to track [25]. Recent work has shown the SHB relation to be imprecise [42]. Even though DC and WDC can potentially find more data races than WCP, the relations can report false positives and require additional “vindication” analysis to prune the false races. Recent work on sync-preserving-races [42] show interleavings where WCP may miss reporting predictable races. However, WCP can re-order critical sections while SyncP cannot and hence miss races, which can be a limitation in GPU kernels with massive parallelism.

WCP. The key insight in WCP [31] is that release-to-acquire ordering of conflicting critical sections is conservative and can be further relaxed based on the order of events within critical sections. WCP only orders the release of the first critical section to the conflicting event of the second critical section. Given a trace \( \alpha \) of events in a multithreaded execution, \( \langle \alpha \rangle_{WCP} \) is the smallest relation that satisfies the following conditions.

(i) For a release event \( r \) on lock \( l \) and a read/write event \( e \) on memory location \( x \) in a critical section on the same lock with \( r < e \) (i.e., \( r \) is ordered before \( e \) in \( \alpha \)), if the critical section of \( r \) contains an event conflicting with \( e \), then \( r \) is WCP-ordered with \( e \).

(ii) For two release events \( r_1 \) and \( r_2 \) on lock \( l \) with \( r_1 < r_2 \), if the critical sections corresponding to \( r_1 \) and \( r_2 \) contain WCP-ordered events, then \( r_1 \) is ordered before \( r_2 \) via WCP.

(iii) WCP composes with the happens-before (HB) order. That is, \( \langle \alpha \rangle_{WCP} \circ \langle \alpha \rangle_{HB} = \langle \alpha \rangle_{HB} \circ \langle \alpha \rangle_{WCP} \).

The relation \( \langle \alpha \rangle_{WCP} \subseteq \langle \alpha \rangle_{HB} \subseteq \langle \alpha \rangle_{TO} \) is the program order, is defined to be the WCP partial order.

Figure 3 shows a predictable race on \( x \), via the interleaving \( e5 \rightarrow e1 \rightarrow e6 \), that is detected by WCP. However, HB orders releases to acquire on the same lock and composes with program order leading to \( e1 \leq \langle \alpha \rangle_{TO} e4 \leq \langle \alpha \rangle_{HB} e5 \leq \langle \alpha \rangle_{TO} e6 \), hiding the race. With WCP, only the release operation \( e4 \) is ordered before the conflicting access at \( e7 \) by rule (i).

However, the WCP relation always reports true data races (or results in a deadlock), which is a desirable trait not to waste developer time and effort [40]. Furthermore, WCP can also be efficiently implemented compared to other partial order relations. These properties make WCP an attractive candidate for implementing a predictive race analysis for GPU kernels.

### 4 Extending WCP to GPU Programs

Directly applying predictive partial orders for CPUs, such as WCP, does not work on GPUs. In the following, we discuss the challenges in encoding GPU synchronization semantics in a partial order. We ignore modeling lockstep execution since it is not guaranteed in newer GPU architectures.

**Barrier synchronization.** Kernels may use scoped barriers to synchronize threads [50], and memory accesses separated by a barrier can never race. A predictive partial order must explicitly order such accesses to avoid false positives.

| Event | Thread 1 | Thread 2 |
|-------|----------|----------|
| e1    | wr(\(x\)) |          |
| e2    | threadfence | wr(\(x\)) |
| e3    |           |          |

Figure 4. The interleaving is not racy if the accesses are from the same block, but indicates a predictable race missed by ScoRD.
**Scoped atomics.** Atomic operations on a CPU do not race, but atomic operations that are insufficiently scoped can race on a GPU. A predictive partial order for GPUs should encode the notion of scopes for atomic operations and should not order two insufficiently scoped atomic accesses to a memory location.

**Scoped locks.** Scoped atomics or fences constitute scoped locks. Two locks overlap in scope if either one of them is device-scoped or threads from the same block hold both the locks. Mutual exclusion is not guaranteed for non-overlapping critical sections. A predictive partial order for GPUs should encode logical time used to capture the GWCP relation \( \leq_{GWCP} \). The analysis maintains the following metadata.

- Per-thread local time \( \mathbb{N}_t \) and vector clocks \( \mathbb{P}_l \) and \( \mathbb{H}_l \),
- Per-lock vector clocks \( \mathbb{P}_l \) and \( \mathbb{H}_l \) and read and write sets \( R_l \) and \( W_l \),
- Per-location read and write vector clocks \( R_x \) and \( W_x \),
- Per-thread locksets \( L_t \),
- Acquire and release event queues \( Acq_l(t) \) and \( Rel_l(t) \),
- Vector clocks \( L^{r}(t) \) and \( L^{w}(t) \) per combination of memory location, lock pair, where \( l \) represents the location and \( s \) represents the scope.

\( \mathbb{P}_l \) refers to the per-thread vector clock (PTVC) corresponding to the relation \( \leq_{GWCP} \). \( \mathbb{P}_l \) is the corresponding lock vector clock. \( \mathbb{N}_t \) is combined with \( \mathbb{P}_l \) to form \( \mathbb{C}_l \) which represents the actual logical time used to capture the GWCP relation \( \leq_{GWCP} \). \( \mathbb{H}_l \) and \( \mathbb{H}_l \) are per-thread and lock vector clocks for HB ordering. The happens-before ordering rules are similar to that used by Barracuda. \( L_t \) is the lockset for the thread \( t \), and tracks the set of locks currently held by \( t \) along with the lock scopes. \( Acq_l \) and \( Rel_l \) queues store acquire and release events on lock variables along with the scopes.

\( R_l \) and \( W_l \) are read and write sets for critical sections on \( l \). \( R_x \) and \( W_x \) represent vector clocks to track the last reader/writer thread(s) and the corresponding access times for a memory location \( x \). \( W_x \) is an epoch, which is a pair of the local time of the last accessing thread and its ID [17]. \( R_x \) and \( W_x \) are used to check for ordering between accesses, and are updated with \( \mathbb{C}_l \) on each access.

The lock identifier in certain data structures has been expanded from a memory value to a pair to allow GWCP to take scopes into account. The algorithm stores the scope with which a lock has been acquired. We omit the updates to \( R_l \), \( W_l \), and \( L_t \) in the pseudocode to save space. \( L_t \) is the per thread lockset and is maintained by inserting a lock into the set on acquires and removing it on a release. \( R_l \) and \( W_l \) are the read set and write sets for a particular thread respectively. These

### 4.1 Tracking GWCP

Algorithms 1 and 2 show the rules to track the GWCP relation via an on-the-fly dynamic analysis. We use the same notation used in the WCP work [31].

| Event | Blk 1, Thr 1 | Blk 1, Thr 2 | Blk 2, Thr 3 |
|-------|-------------|-------------|-------------|
| e1    | wr(\(x\))  |             |             |
| e2    | acq(\(m\)) |             |             |
| e3    | wr(\(y\))  |             |             |
| e4    | rel(\(m\)) |             |             |
| e5    |             | acq(\(m\)) |             |
| e6    |             | wr(\(y\))  |             |
| e7    |             | rel(\(m\)) |             |
| e8    |             | acqblk(\(n\)) |             |
| e9    |             | wr(\(z\))  |             |
| e10   |             | relblk(\(n\)) |             |
| e11   |             |             | acqblk(\(n\)) |
| e12   |             |             | wr(\(z\))  |
| e13   |             |             | relblk(\(n\)) |
| e14   |             |             | wr(\(x\))  |

**Figure 5.** Predictable race detected by GWCP.
are updated on reads and writes by checking the current lockset and inserting into the appropriate sets. On a release, \( R_t \) and \( W_t \) are reset.

In Procedure \texttt{sync}, the parameter \texttt{scope} is a set of TIDs that are part of the scope of the current synchronization operation \( \_\text{syncthreads}() \) or \( \_\text{syncwarp}() \). \( t \) is the parameter to specify the calling thread. In the acquire and release procedures, \( l \) parameter is the lock variable accessed and the \( s \) parameter is the aforementioned scope that specifies the scope with which the current lock variable was used.

The four major differences in GPU synchronization have been addressed as follows:

### Algorithm 1 Tracking GWCP for sync operations

```plaintext
1: procedure \texttt{sync}(\texttt{scope})
2: \texttt{joined} := \texttt{joined}_{\text{HB}} := \phi
3: for all \( t \) ∈ \texttt{scope} do
4: \( C_t := P_t \{ t := N_t \} \)
5: \texttt{joined} := \texttt{joined} \cup C_t
6: \texttt{joined}_{\text{HB}} := \texttt{joined}_{\text{HB}} \cup \mathbb{E}_t
7: for all \( t \) ∈ \texttt{scope} do
8: \( P_t := \texttt{joined} \)
9: \( \mathbb{E}_t := \texttt{joined}_{\text{HB}} \)
10: \( N_t := N_t + 1 \)
11: \( \mathbb{H}_t := \mathbb{H}_t[t := \mathbb{H}_t(t) + 1] \)
12: procedure \texttt{acquire}(\( l, t \))
13: \( P_t := P_t \cup \mathbb{P}_{(l,t)} \)
14: \( \mathbb{H}_t := \mathbb{H}_t \cup \mathbb{H}_{(l,t)} \)
15: if \( s = \text{DEVICE} \) then → Device-level lock
16: for all \( blk \) ∈ \texttt{grid} do
17: \( P_t := P_t \cup \mathbb{P}_{(l, \text{DEVICE})} \)
18: \( \mathbb{H}_t := \mathbb{H}_t \cup \mathbb{H}_{(l, \text{DEVICE})} \)
19: else
20: \( P_t := P_t \cup \mathbb{P}_{(l, \text{device})} \)
21: \( \mathbb{H}_t := \mathbb{H}_t \cup \mathbb{H}_{(l, \text{DEVICE})} \)
22: for all \( t^\prime \neq t \) do
23: \( \texttt{Acq}(t^\prime).\texttt{enque}((C_t, s)) \)
24: procedure \texttt{release}(\( l, t \))
25: while \( \texttt{Acq}(t).\texttt{front}() \not\subseteq C_t \) do
26: \( \texttt{Acq}(t).\texttt{dequeue}() \)
27: \( (\mathbb{V}_t, \texttt{scope}) \leftarrow \texttt{Rel}(t).\texttt{dequeue}() \)
28: if \( \texttt{scope} = \text{DEVICE} \) or \( \texttt{scope} = \text{blk} \) then
29: \( P_t := P_t \cup \mathbb{P}_{(l, \text{DEVICE})} \)
30: for all \( s \in R \) do
31: \( L_t^r_{(l,s)} := L_t^r_{(l,s)} \cup \mathbb{H}_t \)
32: for all \( s \in W \) do
33: \( L_t^w_{(l,s)} := L_t^w_{(l,s)} \cup \mathbb{H}_t \)
34: \( \mathbb{H}_{(l,s)} := \mathbb{H}_t \)
35: \( P_{(l,s)} := P_t \)
36: for all \( t^\prime \neq t \) do
37: \( \texttt{Rel}(t^\prime).\texttt{enque}((\mathbb{H}_t, s)) \)
38: \( N_t := N_t + 1 \)
39: \( \mathbb{H}_t := \mathbb{H}_t[t := \mathbb{H}_t(t) + 1] \)
```

### Algorithm 2 Tracking GWCP for memory accesses

```plaintext
1: procedure \texttt{read}(\( l, x, L \))
2: for all \( (l, x) \in L \) do
3: \( P_l := P_l \cup L^w_{(l,x)} \)
4: if \( s = \text{DEVICE} \) then
5: for all \( blk \in \text{grid} \) do
6: \( P_l := P_l \cup L^w_{(l, \text{DEVICE})} \)
7: \( \mathbb{E}_t := P_l \)
8: \( \mathbb{E}_t := P_l \cup \mathbb{E}_{l, \text{DEVICE}} \)
9: procedure \texttt{write}(\( l, x, L \))
10: for all \( (l, x) \in L \) do
11: \( P_l := P_l \cup L^w_{(l,x)} \)
12: \( P_l := P_l \cup L^w_{(l, \text{DEVICE})} \)
13: if \( s = \text{DEVICE} \) then
14: for all \( blk \in \text{grid} \) do
15: \( P_l := P_l \cup L^w_{(l, \text{DEVICE})} \)
16: \( P_l := P_l \cup L^w_{(l, \text{DEVICE})} \)
17: \( \mathbb{E}_t := P_l \)
18: \( \mathbb{E}_t := P_l \cup \mathbb{E}_{l, \text{DEVICE}} \)
19: \( \mathbb{E}_t := P_l \cup \mathbb{E}_{l, \text{DEVICE}} \)
```

### Shared memory.

GPUs have a hierarchy in memory that mimics the hierarchy in threads. This leads to two different kinds of memory we monitor: \textit{shared} and \textit{global} memory. While global memory is accessible to the entire GPU device, shared memory by definition, is private to a threadblock and thus, can never be involved in an inter block race. To address this, we promote every memory location to indicate whether it is a global or shared memory and for shared memory we maintain which block it belongs to. This helps us treat shared memory per block as a different memory location.

### Scoped atomics.

We maintain if the last memory access to a location was atomic, along with its scope. Before reporting a race we check whether both accesses are atomics with overlapping scopes, in which case we omit the race report.

### Scoped locks.

Our modification to the WCP algorithm treats differently scoped locks as different locks. On release operations we join PTVCs into the held lock’s clock at the appropriate scope, as shown in lines 25 – 29 in Algorithm 1. On acquire operations, PTVCs are joined with block and/or device scoped lock clocks depending on the scope of the lock. For device level locks, we need joins with both device lock clocks and also with every other block’s lock clocks, as shown in lines 16 – 21 in Algorithm 1. This allows us to have an edge when at least one of the scopes used is sufficient to cover both events.

### Barriers.

At a barrier, all threads involved synchronize with each other. Thus, we take a join of all PTVCs involved in the barrier. This means every thread in the block for a \( \_\text{syncthreads}() \) and for active threads in the warp for a \( \_\text{syncwarp}() \) instruction. At this point, the \( C_t \) clocks need
to be joined and not just \( P_i \)'s since \( C_i \) is the vector clock maintaining actual logical time (line 4 in Algorithm 1).

5 Implementation

We implement a prototype tool, PreDataR, to track GWCP. PreDataR uses the NVBit\(^3\) dynamic binary instrumentation framework [65] from NVIDIA. The Barracuda\(^4\) implementation uses a custom binary instrumentation framework developed in-house. The ScoRD artifact\(^5\) uses GPGPU-Sim [30], a simulator for NVIDIA GPUs. Therefore, we have also reimplemented Barracuda and ScoRD with NVBit to allow a fair comparison of the techniques. Using binary instrumentation has the advantage of not relying on source code and provides flexibility in place of the closed-source NVIDIA toolchain.

The NVBit tools inspect SASS instructions and register callbacks on memory accesses and synchronization operations. All the implementations instrument the same instructions. The callbacks create event objects and push them to a communication queue shared with the host. The host cores consume the events from the channels and run the race detection analysis. In the following, we discuss optimizations to improve the performance of our implementations.

Coalesced event processing. The instrumentation of memory accesses and block and warp synchronization generate only one event per warp. For memory accesses, the event captures the memory accesses of all threads in the warp, and is processed in one invocation of the event handler. Warp synchronization is handled similarly.

For barrier synchronization, a barrier ID is passed with the event on a per-warp basis. Each warp involved in the barrier operation generates an event. A counter keeps track of when the last warp participating in the barrier has generated its event, and the active masks of all the participating warps are stored until this point. On detecting the final warp, the counter is reset, and the accumulated active mask information is used to correctly process the vector clocks for all active threads involved in the barrier operation. The implementations do not coalesce events for lock acquires and releases.

Thread exit. The metadata corresponding to a thread is cleared once it exits. This helps control memory overheads when a group of threads finish execution earlier and thus frees up resources. Specifically for PreDataR, this also helps performance as we omit pushing metadata to acquire/release queues corresponding to exited threads.

Inactive threads. A major part of the memory overhead of PreDataR is from the acquire and release queues maintained on a per-thread basis. Algorithm 1 shows that an acquire and a release operation pushes data onto queues for every other thread. For threads that are never involved in an acquire or a release, these queues will look identical. Thus, PreDataR maintains only one copy of these queues representing the vector clock for all inactive threads and switches back to maintaining a private copy when needed. A thread that only accesses memory may also be considered inactive since a memory access does not change any per-thread vector clocks when the lockset is empty.

Block-level barrier. After a \( __syncthreads() \), the vector clock is identical for every thread in a block except for the entry corresponding to a thread’s local clock. This is because the final step after a \( __syncthreads() \) is to do an increment after taking a join with every other thread’s vector clock. This redundancy can be exploited by keeping only one copy of the vector clock for the entire block after a \( __syncthreads() \), ensuring that a read of a thread’s own clock will return an appropriately incremented value. On participating in any other form of synchronization, the implementations revert back to maintaining a private copy of the vector clock. This optimization is expected to improve memory overheads for kernels that synchronize purely with barriers, but we have not included it in the present implementation.

Our implementations currently use a single channel for GPU-to-CPU communication since it is important for the CPU cores to process dependent events in the same order as the GPU execution trace for correctness. PreDataR’s primary goal is to improve data race detection coverage. As a result, we have omitted exploring additional performance optimizations such as supporting multichannel communication between the host and the GPU, and using Unified Shared Memory to track GWCP relations and detect data races (e.g., iGUARD [26]).

5.1 Improving Barracuda

A small contribution in this work is our extension to Barracuda to support newer (Volta onward) GPU architectures.

Scoped atomics. Barracuda supports scoped fences and assigns a scope to each inferred lock based on the scope of the associated fence. Our extension supports the use of scoped atomics. Before reporting a race, our implementation ensures that for two atomic accesses, the lesser of the two scopes does not cover both accesses. An atomic access is reported as a race only if both previous and current accesses are block-level atomics and the accesses are from different blocks.

ITS. Barracuda models lockstep-based execution in pre-Volta architectures (rules EndInsn, If, and ElseEndif in Figure 2, [13]), which are broken with the introduction of ITS. We omit these rules and instead rely on the %laneid PTX register [11] and per-thread metadata for synchronization.

Barracuda also detects intrawarp races when warps diverge along different branches of an if-else statement. The accesses to data are racy because the interleaving order for the branches is not defined. A per-thread analysis covers such races with no extra adjustments. Finally, intrawarp races while

\(^3\)https://github.com/NVlabs/NVBit
\(^4\)https://github.com/upenn-acg/barracuda
\(^5\)https://github.com/csl-iisc/ScoRD
executing the same instruction are also detected by our implementation. We iterate over all active threads in the warp at each memory access to check if two threads perform writes to the same memory location.

**Warp-level barriers.** Volta introduces the \_syncwarp() synchronization primitive, a companion to ITS that forces re-convergence of a warp. We handle this primitive similar to block-level barriers by joining the per-thread vector clocks of each thread involved in the barrier.

We refer to our extension of Barracuda as Barracuda+. We have also added support to detect intrawarp races on the same SASS instruction to our reimplementation of ScoRD.

![Figure 6. Common lock for entire warp.](image)

### 5.2 Vector Clock Compression

A naïve per-thread vector clock (PTVC) has a memory requirement of $O(n^2)$, where $n$ is the number of threads. This makes it challenging to implement vector-clock-based race detectors for GPUs since the number of threads can be in millions. Barracuda exploits redundancies in warp-level vector clocks and stores them in a lossless compressed format whenever possible [13]. Figure 6 shows a lock acquire pattern from the ScoR benchmarks that allows a warp to acquire a single lock for the entire warp while remaining in lockstep, since warp divergence hurts performance. The resultant vector clock will have the same logical time for each thread in a warp but will have different times across different warps. Barracuda’s compression technique specializes to distinct vector clock states and does not exploit such redundancies. Thus, PreDataR implements a more general-purpose PTVC compression logic that uses the GPU thread hierarchy to maintain compressed versions of a PTVC for any partial order.

Figure 7 shows PreDataR’s idea for compression. At the top level, PreDataR maintains an array of block-level vector clocks (denoted by blockVCs). Each blockVC is in one of two states, compressed and expanded. In the compressed state, a blockVC maintains a common logical clock which is the same for every thread in the block. In the expanded state, blockVC is an array of warp-level vector clocks (warpVCs). Each warpVC can also be in one of two states, compressed and expanded. In the compressed state, a warpVC has a common logical time which is the same for every thread in the warp. In the expanded state, the warpVC is a map from thread ID to the (nonzero) logical clock for that thread. PreDataR implements two ideas to improve compression and reduce memory overheads.

![Figure 7. Generic vector clock data structure in PreDataR that is amenable for compression.](image)

**Re-compression attempts.** At every join, PreDataR checks to see if the vector clocks involved in the join can be compressed post the join. Figure 8 shows an example where post join, the warp-level vector clock (VC) is compressed. If every other VC in the block is also compressed and contains the same value, the entire block is compressed.

**Forced compression at barriers.** PreDataR implements a novel idea to compress vector clocks at barriers. Instead of joining every thread at a barrier, PreDataR sets the vector clock entries involved in the join to the highest clock value among the entries. One can view this as an intrawarp join following the standard join for the block involved in \_syncthreads(). The update preserves ordering among threads because a barrier implies every thread involved will restart execution after reaching the barrier. Thus, their logical times for each other can be said to be equal after the barrier completes. For every block not involved in the barrier, PreDataR retains...
the normal join semantics to maintain correctness. The approach allows for a guaranteed compression of a blockVC for each thread in the block. A similar strategy can be applied for __syncwarp(). Figure 9 shows the sequence of compression opportunities exploited by PreDataR when two threads from the same block synchronize with a barrier.

In summary, PreDataR’s vector clock compression scheme is generic, naturally follows the GPU thread hierarchy, and can eliminate any redundancy found during the execution.

6 Evaluation

This section compares the data race coverage and performance of PreDataR with Barracuda+, ScoRD, and iGUARD.

6.1 Experimental Setup

Benchmarks. We use microbenchmarks from the ScoR suite⁶ as litmus tests for the correctness of our implementations and to evaluate data race coverage. Since these benchmarks are not designed for predictable races, we have also created new microbenchmarks to demonstrate the shortcomings of Barracuda+, ScoRD, and iGUARD, and showcase the predictive power of PreDataR. We use large applications to compare the data race coverage and the run time of the techniques. We use the following three applications from the ScoR suite: 1dconv, reduction, and rule-110, and the following seven applications from the Barracuda benchmark suite⁷: hotspot, kmeans, needle, streamcluster (denoted by strmcls), pathfinder, shocbfs, and threadFenceReduction (denoted by thrfenred). Further, we add a new benchmark, stencil, that showcases predictable races in large applications. We omit benchmarks whose unmodified executables fail to run or hang with NVBit. Finally, we omit benchmarks that take too long to run with our binary instrumentation-based implementation.

We will make our benchmarks and the NVBit-based implementations publicly available.

Platform. The experiments execute on an Intel Xeon Silver 4210 system with hyperthreading turned off, 128 GB DDR4 primary memory, running Ubuntu Linux 20.04.3 LTS with kernel version 5.11.0. The GPU is NVIDIA Quadro RTX 5000 with Turing architecture and has 16 GB memory. We use NVIDIA driver version 495.29.05 and CUDA Toolkit version 11.5. All benchmarks have been compiled for sm_70.

6.2 Data Race Coverage with Microbenchmarks

We classify our microbenchmarks into three categories: no-race, dynamic, and predictable. The dynamic benchmarks have races in all interleavings, while the predictable benchmarks have their non-racy interleavings enforced through flags. The use of flags without fences does not guarantee ordering among memory accesses, and thus the microbenchmarks contain true dynamic races. Table 1 summarizes our results; BC+ denotes Barracuda+, SRD denotes ScoRD, IG denotes iGUARD, and PD denotes PreDataR. The race detectors do not report any false positives. We investigate cases where the tools miss races from the dynamic category. Barracuda+ and PreDataR can detect both races. ScoRD catches the first due to our extension (Section 5.1), but misses the second. The ScoRD implementation maintains metadata at warp granularity and performs race detection with warp identifiers, with no emphasis on individual threads. The authors recommend expanding the metadata by 5 bits to maintain thread identifiers to support ITS intrawarp races [27], but such modifications may be prohibitive on hardware platforms. While iGUARD claims to handle ITS-related races, it still fails to detect the two intrawarp races. Interestingly, although ScoRD catches the race in Figure 10 in every interleaving, iGUARD fails to detect the race. iGUARD can detect the race only if \( e_7 \) happens before \( e_1 \) in a particular run.

Predictable races. The predictable category has 13 races. Barracuda+ can catch 6 races in programs that use just fences to order memory accesses incorrectly or have unprotected memory accesses. It misses detecting races where the enforced interleaving introduces HB edges between the racy memory accesses. ScoRD catches such races owing to its lockset detection. However, ScoRD misses races that are exposed when the execution order of the critical sections is changed. ScoRD also misses races between strong memory accesses separated only by a fence. PreDataR catches 11 out of the 13 races, demonstrating its effectiveness at improving race coverage for GPU programs. It catches races where

| Event | Thread 1 | Thread 2 |
|-------|----------|----------|
| e1    | acq(m)   |          |
| e2    | wr(x)    | acq(m)   |
| e3    | rel(m)   | rel(m)   |
| e4    |          |          |
| e5    |          | wr(x)    |
| e6    |          | rel(m)   |
| e7    |          | wr(x)    |

Figure 10. iGUARD fails to find this race

| Event | Thread 1 | Thread 2 |
|-------|----------|----------|
| norace| 11 0 0 0 0 0 |
| dynamic| 16 16 15 14 16 |
| predictable| 13 6 7 7 11 |

Table 1. Comparison of the number of data races detected by the different dynamic analyses with our microbenchmarks.

https://github.com/csl-iisc/ScoR
https://github.com/upenn-acg/barracuda/benchmarks
unprotected accesses overlap on permuting interceding critical sections, a case which neither Barracuda+ nor ScoRD detect. Finally, the two races that PreDataR misses demonstrate GWCP’s limitations: GWCP composes with HB which can hide races [55]. Furthermore, it fails if critical sections conflict early [31], which interestingly ScoRD catches due to lockset detection. The coverage of iGUARD is identical to ScoRD in our predictable benchmarks, as is expected.

### 6.3 Data Race Coverage with Benchmarks

Table 2 summarizes the number of unique data races found by each detector. The stencil benchmark contains predictable races in the interleavings we enforce. A simplified snippet for this benchmark is shown in Figure 11. The benchmark performs a stencil operation in-place. The rows of the output matrix are divided into chunks for each block to process, with each thread processing a column. Each thread also updates a current variable with their thread ID before starting work. In an interleaving where threads go one after the other, read-write races on adjacent accesses are hidden by a spurious HB edge between critical sections for updating the output and current. Furthermore, in this interleaving, all racy accesses are separated by a fence. Therefore, while Barracuda+ and ScoRD are unable to detect the intra-block races, PreDataR catches all such races.

Across all the benchmarks, Barracuda+ and PreDataR detect races where only a fence separates memory accesses. The benchmark reduction contains such races, along with write-read races on accesses separated by insufficiently-scoped fences or no fences at all. ScoRD only reports the latter two, while Barracuda+ and PreDataR detect all three. Similar fence races exist in rule-110. All four detectors detect races on insufficiently-scoped atomics. 1dconv contains a racy usage of a block-scoped atomic add. rule-110 contains access patterns of the form where each thread \( t \) updates indices \( i_{t-1}, i_t, \) and \( i_{t+1} \) on an array using atomics of insufficient scope. The remaining races are on global or shared memory; all three detectors catch them. thrfened contains global and shared memory races, along with concurrent non-atomic and atomic accesses to the same location. The races on shared memory are ITS intrawarp races, which ScoRD misses. All four tools report the remaining two race types.

### 6.4 Performance Comparison

Table 3 shows the performance of different configurations of our tools. Column UM shows the time taken to run the unmodified program natively. NVB shows the time taken to run the unmodified program through NVBit without instrumentation, and BLK shows the time taken when the application is instrumented with empty callbacks. BC+, SRD, IG, and PD denote Barracuda+, ScoRD, iGUARD, and PreDataR, respectively. The two columns BC+–CP and PD–CP, show the run times of Barracuda+ and PreDataR with our compression scheme enabled. Each value is the average of five trials.

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**Table 2.** Comparison of the number of unique kinds of data races detected by the different dynamic analyses on our benchmarks.

|         | Total | BC+ | SRD | IG | PD |
|---------|-------|-----|-----|----|----|
| 1dconv  | 5     | 5   | 5   | 5  |
| reduction | 19   | 2   | 12  | 19 |
| rule-110 | 30   | 24  | 5   | 30 |
| hotspot | 0     | 0   | 0   | 0  |
| kmeans  | 0     | 0   | 0   | 0  |
| needle  | 0     | 0   | 0   | 0  |
| thrfened | 31   | 6   | 0   | 34 |
| pathfinder | 2    | 2   | 0   | 5  |
| shocbfs | 4     | 3   | 2   | 4  |
| stencil | 1     | 0   | 0   | 2  |

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**Figure 11.** Code for the stencil benchmark.
Predictive Data Race Detection for GPUs

| Column  | BLK | NVB | UM |
|---------|-----|-----|----|
| BC+     | 10.6| 6.53| 1.18|
| PD      | 47.69| 232.28| 12.68|
| BC+-CP  | 42.42| 21.93| 3.2|
| PD-CP   | 3.59| 24.48| 26.7|
| IG      | 7.73| 11.63| 44.47|
| 1dconv  | 0.83| 0.83| 0.65|
| reduction | 3.18| 3.42| 0.35|
| rule-110 | 3.18| 3.42| 0.25|
| hotspot | 5016| 6822| 505|
| kmeans  | 1065| 2069| 305|
| needle  | 6580| 6445| 1747|
| pathfinder | 305| 495| 238|
| strmcls | 305| 495| 305|
| thrfenred | 305| 495| 305|
| shocfs  | 138| 476| 120|
| stencil | 120| 120| 119|

Table 3. Comparison of the run times (in seconds) of the different dynamic analyses.

| SRD | BC+| PD |
|-----|----|----|
| BC+CP | 1052| 1052|
| PD-CP | 10218| 10218|
| 1dconv | 494| 742|
| reduction | 5016| 6626|
| rule-110 | 1065| 2092|
| hotspot | 505| 861|
| kmeans | 6580| 6360|
| needle | 1747| 1829|
| pathfinder | 305| 397|
| strmcls | 138| 477|
| thrfenred | 238| 287|
| shocfs | 120| 120|
| stencil | 119| 119|

Table 4. Comparison of the memory overheads (in MB) of the different dynamic analyses.

Column BLK shows that the instrumentation with NVBit has a comparatively higher overhead for the Barracuda benchmarks compared to the ScoR benchmarks. The overhead is especially high for strmcls because it performs more memory accesses. Barracuda+, ScoRD, and PreDataR incur an overhead of 72.3X, 35.8X, and 97.5X over the native execution. The respective overheads over the BLK configuration are 5.2X, 2.6X, and 7.1X, which is a more fair representation of the analyses overheads. Barracuda+ and PreDataR have overheads of 39.6X and 77.3X over ScoRD in the worst case (for hotspot), which primarily comes from maintaining read and write vector clocks and performing vector clock joins. ScoRD is efficient since it only maintains locksets, and the number of locks used in CUDA programs are relatively less.

BC+CP and PD-CP show the performance of Barracuda+ and PreDataR with compression. As expected, compression incurs additional overhead on all benchmarks due to the extra computation, excepting pathfinder. BC+CP and PD-CP have overheads of 1.35X and 1.65X over Barracuda+ and PreDataR respectively. The reasonable overheads of compression compared to the benefits in memory requirements (discussed next) show that the compression schemes can be an effective choice while developing CUDA applications.

IG presents performance of the publicly available iGUARD implementation. iGUARD has very low overhead over the unmodified application since it performs the race detection analysis in parallel on the GPU, and does not incur the overhead of communication between the GPU and the CPU. We emphasize that the PreDataR implementation focuses on race coverage; we include iGUARD results for completeness.

**Memory overhead.** Table 4 shows the peak memory overhead of different configurations of our tools. The two columns, BC+-CP and PD-CP, show the memory overheads of Barracuda+ and PreDataR with our compression scheme enabled. Each value is the average of five trials. We estimate the memory overhead by invoking `getrusage()` at the end of the execution. ScoRD has the lowest memory overhead compared to Barracuda+ and PreDataR. BC+-CP has a worst-case memory overhead of less than 4X time that of ScoRD, with the overhead being less than 2X of ScoRD in all other cases. PD has to maintain more metadata to keep track of conflicting critical sections and thus has the highest overheads. However, PD-CP has less than 4X the overhead of ScoRD in the worst case as well. The results show the generality of our compression scheme, which significantly improves memory overheads of both PreDataR (up to 1.59X) and Barracuda+ (up to 6.47X) analyses on the host.

**Scalability.** Figure 12 shows the scalability plots for those benchmarks where the number of thread blocks can be easily configured. Note that PD-CP on `kmeans` failed with 4096 blocks. hotspot and needle scale well on all tools. In general, PreDataR has poorer scalability than Barracuda+ and ScoRD, because of the additional computation required for predictive race detection.

Given that the expected use case for predictable race detectors is during application development and debugging, our
experiments show that PreDataR provides a good data race coverage and performance tradeoff.

7 Related Work

In the following, we discuss other related work that has not already been discussed.

7.1 Race Detection and Program Analyses on GPUs

Boyer et al. [7] propose a dynamic analysis that instruments kernels and tracks shared memory accesses from different threads to detect data races between reads and writes (ignores write-write races). GRace [73] and GMRace [74] use static analysis to limit instrumentation so that the instrumentation overhead is reduced. These techniques separate intrawarp and interwarp race detection; the intrawarp detection logic runs after each instruction, and heavier interwarp logic runs at barriers or kernel exit. LD [35, 36] detects data races by comparing the values of updated memory locations and avoids the overhead of synchronized metadata updates via instrumentation. LD can miss data races when the old and the new values are the same. HaCCRgR [22] uses hardware support to track cross-thread data dependences but limits tracking of concurrent readers.

Many existing race detectors detect races on shared memory accesses and ignore monitoring global memory accesses for better performance (e.g., [7, 46, 73, 74]). For example, the Racecheck tool from NVIDIA uses dynamic binary instrumentation to detect data races on shared memory [46]. Furthermore, early work on GPU race detection assume lock-step execution and barrier-based synchronization, and ignore synchronization with atomics or fences [7, 35, 36, 73, 74].

Program analyses of GPU kernels primarily target automated detection and fixing of synchronization and performance bugs. Data races are correctness problems because of incorrect synchronization, while barrier divergence and redundant barriers hurt performance. PUG [33] symbolically models barrier synchronization in kernels and uses SMT solvers to detect data races. GPUVerify uses SMT solvers to find data races and barrier divergence bugs [2]. GKLEE generates a trace of the program and uses concolic execution-based verification to identify synchronization bugs [34]. However, symbolic execution methods may not scale well to large input kernels and can report false alarms. Simulee is a dynamic analysis that generates test inputs using evolutionary programming to exercise the buggy regions of code [69].

Compared to multithreaded shared-memory programs on CPUs, it is relatively complex to write efficient CUDA programs and utilize the GPU memory hierarchy. Several performance profiling tools help optimize CUDA programs [9, 47, 60, 62], but these techniques do not help with concurrency correctness.

7.2 CPU race detection

Static data race detection techniques can potentially detect all feasible data races across all possible executions (i.e., no false negatives), but usually do not scale to large programs and suffer from false positives [4, 14, 43, 44, 53, 66]. Dynamic data race detection analyses mostly extend the popular happens-before relation to infer data races [5, 29, 52, 58, 59, 67]. Hybrid techniques integrate both HB and lockset analysis [48, 70], but continue to suffer from the disadvantages of both techniques. Other techniques sacrifice soundness for performance by sampling memory accesses [3, 5, 15, 40, 71] or
require hardware support to speed up the race detection analysis [12, 51, 68, 72, 75]. Data race detection analyses have also been proposed for other parallel programming models such as OpenMP [1, 6, 21, 64].

8 Conclusion

Designing GPU race detectors with good coverage is challenging, given the sophisticated and evolving synchronization idioms. This work proposes (i) the GWCP predictive partial order relation for sound and precise race detection, (ii) discusses the implementation of a tool, PreDataR, to track GWCP, and (iii) discusses several optimisations to reduce memory and performance overheads in vector clock based approaches. Our evaluation shows that PreDataR provides a good tradeoff between the number of data races detected and the performance overhead compared to prior work.

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