Electrical testing of small-series multi-chip microcircuit samples combining Wire Bond and Flip-Chip technologies

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Abstract. The paper provides a technical solution and methodology for conducting automated electrical and functional testing of small series samples of multi-chip assemblies. The results of multi-chip assembly samples testing combining Wire Bond and Flip-Chip technologies are presented. Based on the test results, defects that occur during the packaging process are localized and the assembly stages at which these defects occur are determined.

1. Introduction
The main development trend of modern microelectronics is to continuously reduce product mass and dimension, increase their performance and reliability. In this regard, it is promising to use an electronic component base integrated into a system in package (SiP) [1, 2]. SiP is a set of processor crystals, memory, digital signal processing units or other components interconnected and located in a single package on a substrate. The crystals are arranged on the same level or one above others and are supplemented with passive or other necessary components. Several substrates with crystals can be stacked according to the Package on Package (PoP) technology with the soldering of the ball leads on the upper substrates to the contact pads on the lower substrates [3]. As a rule, either Flip-Chip or Wire Bond technology is used for mounting crystals. The Flip-Chip crystal is mounted on the board with the active side down and fixed using ball contacts. In case of Wire Bond technology, the crystal is directly mounted on a substrate with the wire contacts attached to the substrate or another element by welding [4]. Each microelectronic component of SiP has one or several independent purposes. Also, each component can be the part of other elements in the SiP. An important advantage of the SiP paradigm is that all elements of the system can be manufactured separately, using different technologies, and then assembled into one final electronic device [5]. This approach is beneficial both for chip manufacturers, allowing large-scale production of microelectronic components, and their customers, providing the ability to quickly and easily design specialized electronic devices based on these components [5].

One of the important stages in the development of new integrated circuits (ICs) based on SiP/PoP technologies is prototyping. The prototyping involves creating a model of the product being developed, with the main functional components (crystals) partially or completely replaced by dummy chips with the same size and number of outputs [6, 7]. On the prototype, the entire production line is adjusted, including testing the integrated circuits, marking, scanning and packaging stages.

During the production of integrated circuits, various defects affecting its functionality can occur in the electrical part of the product. For instance, defects can form at the Flip-Chip crystal soldering stage, such as bridges between adjacent ball leads, unsoldered connections of the crystal with the
substrate, and lack of contact with the substrate due to angular and linear displacement of the crystal. During the process of filling the microchips with the mold compound, the insufficiently strong joints of Wire Bond crystals can break off or shorten. Each sample undergoes electrical and functional testing to determine manufacture quality. Then defective samples are subjected to structural analysis using X-ray screening, scanning acoustic microscopy, infrared thermography, etc. [8]

As a rule, electrical and functional testing at microelectronics enterprises is carried out at specialized industrial testing facilities. To conduct the testing procedure, it is necessary to develop a special hardware interface between the prototype and industrial test equipment and to allocate the operating time of this test equipment. These actions are mandatory at the production stage, but lead to the cost increase of the development and prototyping stages, especially for a small-scale production case. This paper presents a technical solution to conducting automated electrical and functional testing of small-scale samples of integrated circuits in order to test the capabilities or adjust the parameters of the manufacturing line for the target device.

2. Production of experimental samples
The development of the methodology for testing prototypes using the computer appliance presented below was performed on special prototypes. The PoP prototype model presented in Figure 1 consists of upper and lower substrates (printed circuit boards) with one dummy crystal and two NOR flash memory crystals. Dummy crystal with 3721 ball leads is mounted on the lower substrate with the Flip-Chip technology. The contact diameter of a dummy crystal is 90 μm, and the pitch is 150 μm. NOR flash memory crystals are mounted on the upper substrate with the Wire Bond technology and filled with mold compound. The substrates are interconnected by soldering of 144 solder balls. The space between the substrates is filled with the underfill compound. The lower side of the lower substrate has 293 contact ball leads for placing an integrated micro-assembly in a socket.

![Figure 1. PoP prototype model: 1 – lower substrate; 2 – upper substrate; 3 – dummy crystal; 4 – NOR flash memory crystals.](image)

Bridges which are located on the lower substrate and dummy crystal (Figure 2) are used for electrical testing of Flip-Chip soldering quality. Bridges connect the solder points and are grouped into 133 daisy-chains passing in alternate way through the substrate and the crystal. The quality control of the electrical connection of the two substrates is carried out using two daisy-chains going through the soldering places of the substrates. The ends of the daisy-chains and the leads of the memory chips are connected to the IC pads. Such a large number of chains are made for reducing structural analysis time to localize installation defects, which leads to decreasing the cost of prototyping.

![Figure 2. Fragments of daisy-chains layouts on the lower substrate (a) and dummy-crystal (b). Red lines indicate the ends of the daisy-chains.](image)
3. Testing equipment and methods

Electrical and functional testing of PoP prototype samples was performed using a developed system for testing integrated circuits. The function block diagram of the test system is shown in Figure 3. The system consists of a printed circuit board with electronic components and electrical connectors installed on it and software running on a personal computer (PC). The printed circuit board contains a socket for connecting the micro-assembly under test, two microcontrollers STM32F429BIT, performing the test procedure; LEDs to indicate the test result; buttons for rebooting the device and running a pre-loaded test, and auxiliary electronic components. The software running on a PC interacts with the master microcontroller MCU1 via the USB interface. The slave microcontroller MCU2 is paired with the MCU1 via the SPI interface. MCU2 is added due to the lack of input/output ports of the master microcontroller. The free outputs of the I/O lines microcontrollers are connected to 293 pads on the socket. The device is USB powered.

![Diagram](image)

**Figure 3.** The function block diagram of the testing system.

The software running on the PC is used to set an input/output map of the tested micro-assembly, to draw up electrical and functional test scenarios, and to receive and log test results. Based on the settings specified in the program, the testing device automatically generates and executes an electrical testing plan and returns the results back to the program. The graphical user interface of the software and a photo of the testing board are presented in Figure 4.

![Software Interface](image)

**Figure 4.** The graphical user interface of the testing software (A) and the testing board photo (B).

During the electrical testing, the input/output signal lines were tested for open-circuit and short-circuit faults in order to identify problems in the signal lines of the micro-assembly components that occur at the packaging stage. Sequential testing of all daisy-chains was carried out by setting a signal on the input and reading on the output contacts of the micro-assembly.
During the functional testing of the samples, the operation of the memory chips located on the upper substrate was verified. For each integrated circuit a unique microcircuit identifier (UID) was read through the SPI interface. Then the contents of the memory microcircuit were erased (Chip erase). After that the data generated by the checkerboard pattern (5555₁₆) and the reverse checkerboard pattern (AAAA₁₆) were recorded into flash memory, then the data was read from the flash memory again, and the conformance to the pattern was checked.

Electrical and functional testing was also carried out at various ambient temperatures using the Espec ARG-0680-AE camera. A typical temperature profile is shown in Figure 5. The temperature changed at a rate of 2 °C/min. At the beginning of the test, the device was placed on a testing board and powered on. The sample was kept at elevated operation temperature at point 1 (operating and storage temperature limits match). Then electrical and functional testing at elevated temperature was conducted. At point 2 the device was maintained to equalize the temperature and tested at a low operating temperature. At point 3 the test sample was powered off and was cooled to the low storage temperature (at point 4). Finally, the sample was heated to a room temperature and tested (point 5). The test cycle was repeated 100 times in order to verify the quality of the assembly at different temperatures.

4. Results and discussion

During the work, 200 samples of integrated micro-assemblies made using PoP technology were manufactured and tested. 182 samples successfully passed electrical testing. There were breaks in signal lines in 18 micro-assemblies. Both in the process and after manufacture X-ray analysis did not reveal any defects in 15 out of 18 rejected samples (Figure 6a). Visual inspection of the micro-assemblies crosscuts along a torn chain of bridges under a microscope revealed non-soldered ball contacts between the dummy crystal and the lower substrate (Figure 6b). This type of defect is supposedly caused by insufficient heating during soldering of the crystal on the substrate. That leads to ball lead detaching from the contact pad at the stage of underfill filling and polymerization.

Figure 5. Environmental parameters testing temperature profile

Figure 6. X-ray of the prototype (a) and photo of the crosscut at the defect site. The red circle indicates the contact breaking point.
186 test samples successfully passed functional testing. 14 of them had problems with recording/reading at over 10 MHz data transfer rates. As the reason for reading/recording errors, spurious capacitive pickups from the SPI clock line are present on the data line of the SPI interface was found by Time Domain Reflectometry. These capacitive pickups are caused by the proximity of the Wire Bond connections of the memory microcircuit formed during the mold compound filling stage (Figure 7).

![Figure 7. X-ray of displaced wires.](image)

Then electrical and functional testing of 182 passed samples was performed with multiple heating/cooling cycles according to the temperature profile shown in Figure 5. Open-circuit faults were observed in 5 samples due to ball contact detachment after 100 cycles. All samples passed functional testing.

5. Conclusions
As a result of this work, 200 samples of SiP package assemblies were manufactured and tested. Each sample includes one Flip-Chip technology mounted crystal and two Wire Bond technology mounted NOR flash memory crystals. A test system for electrical and functional testing of ICs was developed and testing samples were performed at various ambient temperatures. The capabilities of the manufacturer product line were evaluated based on the test results. There are 88% of successfully tests passed samples. Testing makes it possible to localize defects having occurred during the manufacturing process and to configure the product line for the end line device to reduce the number of defects.

It should be noted that the system for electrical and functional testing described in the paper is a multifunctional system that allows testing a wide range of integrated circuits. The socket on the testing board can be replaced in case of non-compliance of the test assembly footprint.

Acknowledgments
This work was supported by the Ministry of Science and Higher Education of the Russian Federation (project No. 05.577.21.0293, unique identifier RFMEFI57718X0293).

References
[1] Santagata F, Sun J, Iervolino E, Yu H, Wang F, Zhang G, Sarro P M and Zhang G 2018 System in package (SiP) technology: fundamentals, design, and applications Microelectron. Int. 35 231–43
[2] Lei H, Ellassaad S, Shi Y, Hu Y, and Yao W 2011 System-in-package: electrical and layout perspectives Foundations and trends in electronic design automation 4(4) 223-306
[3] Koh W 2005 System in Package (SiP) technology applications 6th Intern. Conf.on Electronics Packaging Technology 2005
[4] Elenius P and Levine L 2000 Comparing flip-chip and wire-bond interconnection technologies Chip Scale Review 08 81-87
[5] Appello D, Bernardi P, Grosso M, and Reords M S 2006 System-in-package testing: problems
and solutions *IEEE Design and test of computers* **23**(3) 203-11

[6] Patel D A 2016 *Test and characterization methodologies for advanced technology nodes* (Electronics Université Montpellier)

[7] Laung-Terng W, Cheng-Wen W and Xiaoqing W 2006 *VLSI Test Principles and Architectures* (Morgan Kaufmann Publishing House) 2 pp 37-103

[8] Aryan P, Sampath S and Soch H 2018 An Overview of non-destructive testing methods for integrated circuit packaging inspection *Sensors* **18**(7)