The Study on the Key Hardware Development of Single-Phase Photovoltaic Grid-Connected Inverters

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Abstract. High-efficiency inverter topology design on single-phase photovoltaic grid-connected equipment is the core of bringing considerable benefits to the society and the investors. In order to study the key hardware design of the inverter that meets the leakage current requirement and achieve the maximum efficiency, this paper analyses the H-bridge based topology (H5 and H6) and DPB topology. Firstly, this paper discusses the working principle of these topologies and concludes that the DPB topology involves fewer MOSFETs than the H-bridge based topology. Additional studies of power device analysis and other component losses in these topologies have concluded that DPB topology typically has lower power device losses at different load ratios. For instance, when the load ratio (Po / Pe) is 100, the power device loss of the H5 topology is 77 W, and the loss of the H6 topology is 68.7 W. Under the same conditions, the loss of the power device in the DPB topology is only 53.6 W.

1. Introduction
Distributed Generation (DG) is one of the cutting-edge technologies in modern power grid systems. As a highly promising renewable energy application, DG has been world widely used in various fields[1, 2]. For instance, photovoltaic (PV) grid-connected system in cities and communities, and the agricultural land[3, 4], which have brought many opportunities and benefits to the society[5].

A typical PV grid-connected system consists of four subsystems [6]: PV array, inverter, power grid and control subsystem. Many PV modules combine the PV array with a set of series and parallel structure, which transforms solar energy into DC electrical energy by the photo-electric effect. The inverter is the core element connecting both the PV array (as input) and the power grid (as output), which converts DC power generated from PV array to AC power in the power grid. The control subsystem monitors voltage, frequency and other characteristics of a power grid in real-time and ensures the inverter output AC power with the same frequency and phase as the power grid, with the use of power electronics technology.
Among all of them, the efficiency of power conversion through the inverter will directly affect the investment return of the PV power station. Every 1 per cent increase in the efficiency of PV grid-connected equipment brings enormous economic value to society. With the improvement of inverter power, the initial investment costs can be shortly recovered, which is conducive to promote the development of distributed PV power generation of PV energy system in cities and communities.

Professor Remus Teodorescu et al. from Aalborg University proposed an inverter circuit topology without transformer based on HB-ZVR characteristics [7]. Araujo S V et al. from Kassel University developed a Dual-Paralleled-Buck (DPB) topology [8] based on the classical DC Step-down Circuit, by which high power conversion is realised. Victor M et al. proposed an H5 topology, whose circuit control problem such as low ground leakage current was discussed [9, 10].

This paper firstly analyses the topology structure of H5 and DPB. Then, the working principle of those topologies and their usage as a high-efficiency medium-power inverter circuit are discussed.

2. Single-Phase PV Grid-Connected Inverter Topology Studies
The determination of a PV grid inverter topology structure is closely related to its efficiency, investment costs and reliability, which are the core of necessarily designing an inverter. Particularly the choice of PV inverter topologies for the case of no isolated transformer are highly related to the efficiency of voltage conversion and the current leakage caused by common-mode voltage. Since there is no isolated transformer, the leakage current will affect the operation of the residual current detector (RCMU) as usual, resulting in the current loop failing to trip due to the line contact damage to the positive or negative pole of the photovoltaic plate, and the protection of the human body will be invalid.

Traditional circuit topologies are: 1) H-bridge based topology [11] and 2) Neutral-point clamping (NPC) topology [12]. This paper compared the novel H5 and H6 inverter topology and the Dual-Paralleled-Buck (DPB) topology with the calculation of their common-mode voltage and their circuit design advantages.

2.1. H5 Inversion topology
H5 inversion topology [13] was first introduced by SMA Solar Technology, and its schematic diagram is shown in Figure 1. On the basis of Classical H-bridge, the 5th switch is added on the DC bus. With the control of S5, the common-mode voltage is kept in constant. Therefore, the current leakage is reduced.

The advantages of this circuit design are: 1) Small loss to the inductance magnetic core due to the voltage on the filter is unipolar. 2) The zero-volt mode reduces the switching loss because one of the branches is a lower frequency switch, which improves its efficiency. 3) The voltage of PV panels to the ground is only at the distributed power grid frequency, so the leakage current and EMI are small.

The disadvantages of this design are: 1) Three switches are energized during the conduction period, resulting in high conduction loss, but the overall high frequency is not affected. 2) An additional switch is required.

![Figure 1. The schematic diagram of Single-Phase Grid-Connected H5 Inverter Topology](image-url)
2.2. DPB topology

Dual-Paralleled-Buck (DPB) inverter topology was designed by Kassel University and SMA Solar Technology in Germany in 2010, as shown in Figure 2.

The main advantage of this design is that only four MOSFETs are involved in the circuit as switches. Only two of the MOSFETs in the circuit are operated in every half cycle, which is very efficient.

The drawbacks are: 1) the circuit requires two inductors and four diodes. 2) There are potential risks on the two MOSFETs directly connecting to the grid where short-circuit could occur. Dead zones need to be set for the purpose of controlling the device to avoid short-circuit, which increases the costs.

![Diagram of Single-Phase Grid-Connected DPB inverter topology](image)

Figure 2. Schematic diagram of Single-Phase Grid-Connected DPB inverter topology

2.3. Discussion

In comparison between the two topologies, the common points are that 1) the common-mode voltage of the inverter remains constant during both the positive and negative half cycles while inverting, which is equal to the half voltage of PV panels, and 2) The voltage of the PV panel to the ground is only at the distributed power grid frequency, so the current leakage and EMI are small.

3. High Efficiency DPB Inverter Circuit Design and Loss Analysis

From the DPB topology workflow, it can be seen that the string inverters have wider input range and applications due to a DC/DC structure in the front. On the other hand, the string inverters control the PV modules by MPPT[14] so that it can maximize its performance if the inverters are containing Boost circuit[15]. Therefore, this paper proposed a DPB design where the first stage uses DC/DC boost circuit, followed by DC/AC inverters, the input and output parameters are given in the following table:

| Specifications                  | Parameters |
|---------------------------------|------------|
| Rated Input Voltage             | 360 V      |
| MPPT Voltage Range              | 90–560 V   |
| Maxim Input Voltage             | 600 V      |
| Maxim Input Current             | 10 A       |
| Rated Output Power              | 3000 W     |
| Rated Grid Voltage              | 220 Vac    |
| Grid Voltage Range              | 180–276 Vac|
| Rated Operating Frequency       | 50 Hz      |
3.1. DC/DC Circuit Design

DC/DC conversion uses Boost circuit, which transfers lower voltage to higher output voltage. From volt-second balance formula [16], the following relation can be obtained:

\[ \frac{V_{PV}}{L} DT + \frac{(V_{PV} - V_{dc})}{L} (1 - D) T = 0 \]  

Simplified to:

\[ \frac{V_{dc}}{V_{PV}} = \frac{1}{1 - D} \]  

Boost Converter can be divided into current-discontinuous-mode (DCM) and current-continuous-mode (CCM). Compared with DCM mode, CCM is more suitable for high-power applications. On the other hand, the stress of the switch under CCM condition is relatively small, so the output DC voltage ripple is small. The 3 kW inverters studied in this paper adopt CCM mode in Boost circuit design.

3.2. DC/AC Circuit Design

According to the analysis of 2.2, this paper adopts the DPB topology cause the DPB to have higher efficiency.

DPB topology workflow is as follows: In the positive half cycle of the operation, MOSFET S2 and S3 conduct as a switch, S1 and S4 are off. At the same time, inductor L2 is active in the loop. When S2 is off, current flows through the diode (D2). A similar condition applies to S1, S4, L2 and D4 when the inverter is operating at the negative half cycle.

The DC/AC circuit design depends on the loss, which can be expressed as the following formula:

\[ P_{tot} = P_s + P_L + P_{other} \]  

\( P_s \) is power device loss, which can be divided into conduction loss \( P_{con} \) and switching loss \( P_{sw} \). \( P_L \) is inductance loss, and \( P_{other} \) represents other losses.

1) The S1 and S2 are high-frequency components, whose loss containing both conduction loss and switching loss. The “ON” state duty ratios of those switches can be expressed as:

\[ d_{S1}(t) = M \sin(\omega t) \]  

where, \( M \) represents the modulation ratio. The switch components can select MOSFET or IGBT, and their working principles are different.

Taking S1 as an example to calculate the loss of high-frequency equipment, the conduction voltage-drop characteristics of MOSFET and IGBT can be simplified as:

MOSFET:

\[ v_{ds}(t) = i(t)R_{ds} \]  

IGBT:

\[ v_{ce}(t) = V_t + i(t)R_{ce} \]  

The output current \( i(t) \) of the inverter can be expressed as:

\[ i(t) = I_m \sin(\omega t) \]  

MOSFET conduction loss:

\[ P_{S1,con,MOSFET} = \frac{1}{2\pi} \int_0^\pi i(t)v_{ds}(t)dS_{1}(t)d(\omega t) = \frac{2M}{3\pi}I_m^2R_{ds} \]  

IGBT conduction loss:

\[ P_{S1,con,IGBT} = \frac{1}{2\pi} \int_0^\pi i(t)v_{ce}(t)dS_{1}(t)d(\omega t) = \frac{M}{4}I_mV_t + \frac{2M}{3\pi}I_m^2R_{ce} \]  

The switching loss of MOSFET needs to be calculated based on the typical parameters of the switching characteristics. Generally, it can be divided into the loss caused by junction capacitance, the loss of zero-phase diode reverse recovery and the switch recovery loss caused by the diode, respectively.

\[ P_{S1,sw,MOSFET} = f_{sw}E_{oss}(V_{ds}) \]  

\[ P_{d,rr} = \frac{1}{2\pi} \int_0^\pi f_{sw} \left[ V_{dc}I_m \sin(\omega t) t_a + V_{dc} \frac{l_{rr}}{4} (2t_a + t_b) \right] d(\omega t) \]  

\[ P_{d,sw} = f_{sw} (0.5I_m)(0.5V_{dc})t_b \]
where, \( t_a, t_b \) represents the time parameter of the recovery current, \( I_{rr} \) represents the peak value of reverse recovery current.

The switching loss of IGBT is mainly divided into turn-on loss and turn-off loss, which can be expressed as:

\[
P_{on,SW} = \frac{1}{2\pi} \int_0^\pi f_s h_I M k_{gon} V_{ds} \frac{\Gamma(k+1)}{\Gamma(\frac{k+1}{2})}
\]

\[
P_{off,SW} = \frac{1}{2\pi} \int_0^\pi f_s m_I M k_{goff} V_{ds} \frac{\Gamma(n+1)}{\Gamma(\frac{n+1}{2})}
\]

where, \( \Gamma(x) \) is Gamma function; \( h \) and \( k \) are the energy factors when turned on; \( m \) and \( n \) are the energy factors when turned off; \( k_{gon} \) and \( k_{goff} \) are the correction factors based on IGBT gate resistance and \( V_{test} \) represents the test voltages at the time of parameters \( h, k, m \) and \( n \) obtained.

Similarly, the anti-parallel diodes of the IGBT have the conduction loss \( P_{d,sw} \) and the reverse recovery current loss \( P_{dr,sw} \) as well as the previously analyzed MOSFET. So, the loss of S1 can be expressed as:

\[
P_{S1,MOSFET} = P_{S1,CON,MOSFET} + P_{S1,SW,MOSFET} + P_{d,rr} + P_{d,sw}
\]

or \( P_{S1,IGBT} = P_{S1,CON,IGBT} + P_{S1,ON,sw} + P_{off,sw} + P_{d,rr} + P_{d,sw} \)

2) The S3 and S4 is low-frequency device. The loss is mainly conduction loss. Generally, the switching devices with low on-resistance or low on-voltage are selected. The duty cycles of S3 and S4 conduction can be expressed as:

\[
d_{s3}(t) = 1
\]

If MOSFET is chose, the conduction loss is

\[
P_{S3,CON,MOSFET} = \frac{1}{2\pi} \int_0^\pi i(t)v_{sw}(t)d_{s3}(t)d(wt) = \frac{1}{4} I_M^2 R_{ds}
\]

If IGBT is chose, the conduction loss is

\[
P_{S3,CON,IGBT} = \frac{1}{2\pi} \int_0^\pi i(t)v_{sw}(t)d_{s3}(t)d(wt) = \frac{1}{4} I_M^2 V_t + \frac{1}{4} I_M^2 R_{ce}
\]

So, the S3 loss can be expressed as:

\[
P_{S3,MOSFET} = \frac{1}{4} I_M^2 R_{ds}
\]

Or

\[
P_{S3,IGBT} = \frac{1}{4} I_M V_t + \frac{1}{4} I_M^2 R_{ce}
\]

3) The D1, D2 mainly achieves freewheeling conduction, the duty cycle of D1, D2 conduction can be expressed as:

\[
d_{d1}(t) = 1 - M \sin(wt)
\]

The conduction loss of the diode is

\[
P_{D1,CON} = \frac{1}{2\pi} \int_0^\pi V_{diode}(t)d_{diode}(t)d(wt)
\]

\[
= I_d V_f \left( \frac{1}{\frac{2\pi}{4}} + I_M^2 R_{ak} \right)
\]

The reverse recovery loss is

\[
P_{D1,rr} = \frac{1}{2\pi} \int_0^\pi f_s [V_{dc} I_m \sin(wt) t_a + V_{dc} \frac{Lr}{4} (2t_a + t_b)]d(wt)
\]

\[
= \left( \frac{1}{M} t_a + \frac{1}{rr} (2t_a + t_b) \right) V_{dc} f_s
\]

So, the loss of the diode is

\[
P_{D1} = P_{D1,CON} + P_{D1,rr}
\]

In summary, the power device loss \( P_S \) in the DPB inverter topology can be expressed as

\[
P_S = P_{S1} + P_{S2} + P_{S3} + P_{S4} + P_{D2} + P_{D4} = 2P_{S1} + 2P_{S3} + 2P_{D1}
\]
3.2.1. Inductor loss Analysis

Inductance loss can be divided into copper loss ($P_{\text{cu}}$) and iron loss ($P_{\text{fe}}$). Copper loss is the loss of the wire, mainly caused by the resistance of the wire. The iron loss is eddy current loss, hysteresis loss and residual loss.

Assuming the inductor is wound with a multi-strand or a Litz wire with a diameter less than twice the penetration depth, it can be simplified to that the AC resistance is equal to the DC resistance, so the copper loss is:

$$P_{\text{cu}} = R_w I_{\text{rms}}^2$$  \hspace{1cm} (27)

where, $R_w$ is the DC resistance of the wire; $I_{\text{rms}}$ is the total effective value of the inductor current including the switching ripple.

Hysteresis loss can be simplified based on the graph of core loss and flux density per unit volume provided by the manufacturer:

$$P_{\text{fe}} = N_s V_e P_e$$  \hspace{1cm} (28)

where, $N_s$ is the DC resistance of the wire; $I_{\text{rms}}$ is the total effective value of the inductor current including the switching ripple.

Wherein, $N_s$ is the number of cores connected in parallel; $V_e$ is single core volume, and $P_e$ represents the core loss corresponding to the working flux per unit volume.

3.2.2. Other loss Analysis

Other losses, mainly including auxiliary power supply, loss caused by parasitic parameters in the line, and so on, which need to be obtained according to actual circuit analysis and measurement.

3.2.3. Comparison of DPB loss and loss of other topologies

In order to compare the losses among the DPB and other different topologies, the same power devices are used for comparison. The MOSFET uses Infineon's IPW60R041C6, the diode uses MICROSEMI's APT30DQ60BG, and the IGBT uses IR's IRGP4063D. According to the application case in Table 2, the working states of the high-efficiency topologies H5, H6 and DPB power tubes (as shown in Table 3) and the loss values are analysed.

### Table 2. Device operation of each topology in the power frequency half cycle

| Topologies          | High Frequency Devices 20kHz | Power Frequency Devices 50Hz | Diode 20kHz |
|---------------------|-----------------------------|-----------------------------|-------------|
|                      | Two MOSFETs                 | Two MOSFETs                 | One MOSFET  |
|                      | One IGBT                    | One MOSFET                  | One IGBT    |
|                      | One Diode                   | One Diode                   | One Diode   |

### Table 3. Loss of power devices of various topologies at different load ratios

| Po/Pe (%) | H5 (W) | H6 (W) | DPB (W) |
|-----------|--------|--------|---------|
| 100       | 77.0   | 68.7   | 53.6    |
| 75        | 51.2   | 43.0   | 34.6    |
| 50        | 30.7   | 23.9   | 20.1    |
| 30        | 17.9   | 13.2   | 11.9    |
| 20        | 12.8   | 9.5    | 8.9     |
| 10        | 8.5    | 7.8    | 6.6     |

The total loss of the H5 topology is higher than that of DPB because the loss of the IGBT switch in the “ON” state is higher than MOSFET. The loss efficiency of the H6 topology is about 1% of the total power, but there is no hidden danger of the short circuit of the switch on the grid side. The loss of the DPB topology is minimal because only two switches are required in the on state, and H5 has three switching devices. In actual working conditions, it is necessary to set the dead time of the switching tube to prevent the short circuit, so the working efficiency will be reduced. In summary, the DPB is a topological structure with high efficiency and with reasonable working stability.
4. Conclusion
In this paper, based on the working principle of the H-bridge topology (H5 and H6) and the DPB topology, and the loss analysis of the power device, the key hardware design of the inverter that meets the leakage current requirement and achieves the maximum efficiency is studied. According to the number of MOSFET or IGBT switching components required in different topologies and the losses under different load ratios, it can be concluded that DPB is a relatively efficient and stable topology suitable for the development and application of single-phase photovoltaic grid-connected inverters.

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