FBCT fast intensity measurement using TRIC cards

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ABSTRACT: At the CERN PS complex, precise fast intensity measurements are very important in order to optimize the transfer efficiencies between the different accelerators. Over the last two years a complete renovation has been ongoing, where the old electronics, based on analogue integrators, have been replaced by a fully digital system enclosed in a single VME based card. This new system called TRIC (Transformer Integration Card) is based on a 12 bit, 212 MS/s ADC and an FPGA for the signal processing. Also located on the same board one finds a 250 V/1.5 W DCDC converter used to generate precise calibration pulses.

KEYWORDS: Instrumentation for particle accelerators and storage rings - low energy (linear accelerators, cyclotrons, electrostatic accelerators); Hardware and accelerator control systems; Beamline instrumentation (beam position and profile monitors; beam-intensity monitors; bunch length monitors)

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1 Introduction

The CERN PS complex (figure 1) consists of a series of interconnected accelerators. Protons are created and pre-accelerated in LINAC2 (Linear Accelerator), before being separated into 4 slices injected into the PSB (Proton Synchrotron Booster). The PSB consists of 4 superimposed synchrotrons. After an acceleration cycle, beams are recombined and injected into the Proton Synchrotron (PS) accelerator. The PS is a highly versatile particle accelerator. It delivers beams of protons with a variety of properties not only for use in LHC (Large Hadron Collider), but also to many experiments at the PS or the SPS (Super PS) on a cycle-to-cycle basis. These include experiments at the PS East Hall, neutron time of flight measurements at the PS, fixed target experiments or neutrino experiments at the SPS. In addition the PS is able to accelerate heavy ions created by LINAC3 and LEIR (Low Energy Ion Ring).

Beam intensity is one of the most important parameters when describing a particle beam and fundamental in transfer efficiency optimization among different accelerators. The standard fast measurement method uses an inductive coupling of the magnetic field produced by the beam to the measurement device called FBCT (Fast Beam Intensity Transformer) to obtain a beam signal.

This document describes how the beam intensity is measured using TRIC (Transformer Integrator Card), a complete digital system that measures the analogue signal provided by FBCTs. This system has to be sufficiently versatile to measure intensities ranging from 0.5 to $3000 \cdot 10^{10}$ charges, and able to manage different beam formatting schemes as well as bunch lengths from 500 ns in transfer-lines to 150 us in the linacs.
2 FBCT signal processing and data acquisition

Beam intensity measurements are typically based on the inductive coupling of the magnetic field produced by the beam to a high permeability magnetic material. In the case of the Fast Beam Current Transformers (FBCT) where the observation of short beam pulses is required, a bandwidth in the order of 100 MHz is needed. In order to transmit the FBCT signals out of the accelerator tunnel using long cables a preamplifier (Head Amplifier) is added in the tunnel, mainly to improve the signal-to-noise ratio (S/N) for low intensity beam signals.

Due to the large dynamic range and bandwidth variety of beam signals to be measured, selectable gain and high speed sampling is required to translate the analogue beam signal into the digital domain. A calibrator which simulates the beam by injecting a well-defined current into a calibration winding is also necessary in order to maintain accuracies in the order of 1%. Summarizing all these conditions, a VME 64X based electronics card has been developed to fulfil all the requirements of the system. This new card, known as the TRIC (Transformer Integration Card), is based on an Altera Cyclone EP2C20F484C6 (20,000 logic entities) FPGA which contains the entire control of the system and signal processing. A VME bridge between the FPGA and VME controller has been implemented using an Altera EPM2210F256C3 CPLD (570 logic entities), allowing remote upgrades to the firmware. Two 30 MHz analogue bandwidth, 12 bits 212 MS/s ADC channels are used for FBCT signal acquisition, connected to a low gain (no head amplifier) and high gain (head amplifier included) signal path. These are both equipped with three remotely programmable attenuators (0, 14 dB, 28 dB) to adjust the gains for different beams. The calibrator uses a miniature 250 V/1.5 W DCDC converter to have two different calibration methods either by voltage (charge) or by current. The “Voltage calibration” uses a 10 nF, 250 V/1 % capacitor discharge, while the “Current calibration” uses a switched current source to inject a selectable (up to
100 mA), highly reproducible (< %0.1 standard deviation) current into the system, the schematic block diagram is shown in figure 2.

2.1 Analogue front-end

As illustrated in figure 3, the BCT consists of a toroid of a high frequency ferrite mounted over a ceramic tube which acts as an insulating gap in a vacuum chamber of the transfer line. The beam current acts as a single turn primary winding of the toroid transformer while the number of turns around the toroid forms the secondary winding. The load resistor Rl (see figure 4) across the secondary winding of ‘n’ turns gives a voltage signal corresponding to the instantaneous beam intensity. The BCTs can be calibrated by passing a known signal through a calibration winding and observing the signal across the secondary winding.

To better cope with the different beam intensities, the signal path is split using a −6 dB resistive splitter, one branch without gain (low gain, 120 MHz bandwidth) and the other using a 29 dB amplifier (high gain, 30 MHz bandwidth) and over voltage protection.

Figure 2. FBCT beam intensity/current measurement chain.
Signals are transported out of the tunnel using coaxial cables to feed 3 MHz non reflective Gaussian filters. This filter acts as integrator on the time domain beam signal, conserving the beam intensity information as a “stretched” signal. This solution allows more ADC samples to be acquired in order to maintain accuracies in the order of 1 % for signals (in the order of $\approx 500$ nano seconds after 3 MHz filtering), and therefore improving the resolution by further integration (averaging). Figure 5 summarize the signal bandwidth on the different system stages.
2.2 Data acquisition, control and signal processing

Due to the large variety of beam types with different timing structures a read-out electronics system with adaptable data acquisition and signal processing is needed.

This readout has also to control acquisition and calibration ruled by the central timing for the later post processing of the sampled data in order to give an intensity measurement. This digital acquisition and control system is embedded into the TRIC card and the main advantages of this solution are listed below:

- Large dynamic range from 0.5 to 3000·10^{10} charges, 76 dB
- Remote setup
- Maintainability, one module embeds all elements needed
- Fast upgrade, FPGA remote programming.

2.2.1 Measurement concept

Beam intensity $N_{\text{Beam}}$ is measured by acquiring the integration of four different gates, the first integrator measures the beam area, a second integrator will measure the base line in order to subtract the offset (see figure 6). Using a well-known signal (Calibrator), and also applying an offset measurement for the calibration integration we can determine how many charges correspond to the calibrator area $N_{\text{Cal}}$ to later obtain beam intensity by computing:

$$N_{\text{Beam}} = \frac{A_{\text{Beam}} - A_{\text{Beam,offset}}}{A_{\text{Cal}} - A_{\text{Cal,offset}}} \cdot N_{\text{Cal}}$$

where

$$N_{\text{cal}} = \frac{C \cdot V}{q} \quad \text{for voltage calibration or} \quad N_{\text{cal}} = \frac{I \cdot t}{q} \quad \text{for current calibration}$$

![Figure 6. TRIC Intensity measurement concept.](image)

2.2.2 TRIC description

The measurement system is built as a standard VME 6U card. The schematic block diagram is shown in figure 7 and its main characteristics are summarized in table 1. The system is based on an Altera Cyclone EP2C20 FPGA. The card is equipped with an Active Serial configuration protocol and requires a tiny serial FLASH memory to hold its configuration. Remote FPGA upgrade
is possible directly via the VME interface. To achieve a high dynamic range of the intensity measurement, the card is equipped with two ADC 12 bits 212 Ms/s channels operating simultaneously on the high and low gain signals. Since the signal amplitudes are linked to the beam type, the amplitude regime is known in advance, and it is possible to adjust the input attenuator to fit the signal into the appropriate range, by means of three different levels of attenuation 0, 14 and 28 dB. Both channels are protected against too high input signals.

To ensure a high accuracy, current and charge calibrators are implemented. The calibrator circuitry requires max 200 V DC to generate the high energy pulses which are in the order of maximum beam intensity. The programmable miniature DCDC converter (250 V/1.5 W), delivers the required voltage. Thanks to this solution, the calibrator does not need any external high voltage supply that would complicate the system, with this solution the entire system fits on a single electronics board.

The output voltage of the converter is measured using the 12bit ADC for precise calibration. Two calibrator types are implemented on the same board, a voltage, and current calibrator. The voltage calibrator is implemented by a high voltage and low tolerance capacitor (10 nF, 250 V/1%) discharge previously charged to a well-known voltage over a 50 Ohm load on the FBCT. This process generates a peak current of maximum 4 A, and falls exponentially to zero. Unfortunately this method depends on the cable attenuation between FBCT and TRIC which varies and can be in some cases substantial because the distance in some cases is bigger than 300 meters.

On the other hand the constant current calibrator is based on a switched current source. Since the duty cycle of the calibrator is very low in comparison with measurement frequency, it is possible to use charged capacitors to regulate the discharge as a current pump in order to generate the negative constant current pulses. After calibration, the capacitors are slowly (1s) charged to be ready for the next cycle. The circuit can generate calibration pulses from 15 us to 1 ms and a maximum current of 100 mA at the 50 Ohm load with 50 uA resolution.
Table 1. TRIC specification summary.

| Parameter                                      | Value                                                                 |
|------------------------------------------------|----------------------------------------------------------------------|
| Number of independent ADC channels             | 2                                                                   |
| ADC ENOB                                         | 10.7                                                                |
| Linearity                                       | 0.209%                                                              |
| Input Low Pass Filter cut-off Frequency         | 50 MHz, 6th order LC filter                                         |
| Measurement ranges                              | 1V, 10V, 14V, 28V attenuation                                      |
| Over voltage protection                         | Yes, both channels, clipping at ±3.3V                               |
| Sampling rate                                   | 242.5 MHz                                                           |
| Remote firmware upgrade                         | Yes, FLASHE update and direct FPGA configuration                     |
| Measurement resolution limit                   | 9.2 ns                                                              |
| Input offset compensation                       | Yes                                                                 |
| Calibrator onboard                              | Current Voltage                                                     |
| Calibration pulse amplitude (current mode)      | 10 mA - 100 mA at 50 Ohm load                                      |
| Calibration pulse time (current mode)           | < 12 ns                                                             |
| Calibration pulse time (current mode)           | 0.01-1000 ms                                                       |
| Calibration pulse amplitude (charge mode)       | 200 V                                                               |
| Calibration mode                                | Before or after measurement                                        |
| Remote control of all the functions (including calibration procedure) | Yes, embedded VME controller running Lynx09                        |
| Digital inputs/outputs                          | 8x TTL, LEMO connectors, over voltage protected                     |
| Dedicated high speed interface                  | Yes, 8 channel bi-directional LVDS                                  |
| Communication interface                         | VME 54x mechanical form, 24bit address, 32bit data                  |
| Burst VME transfer support                      | Yes                                                                 |
| Programmable logic resources                    | ~20,000 Logic Elements (LE) of FPGA + 710 (LE) of CPLD              |

High accuracies on calibrators are necessary to obtain total system accuracy below 1%. Measurements demonstrates a good reproducibility of the calibration signal, sigma < 0.1% for current (see figure 8), and sigma < 0.3% for voltage calibrator.

TRIC cards are also cross-calibrated to reduce relative measurement error between the boards.

![Current calibrator repeatability for 1000 measurements](image)

Figure 8. TRIC current calibrator repeatability.
2.2.3 TRIC FPGA firmware

The FPGA acts as the control unit of TRIC (see figure 7). It is in charge of all the necessary tasks to achieve the required intensity and current measurements. The FPGA firmware has been done and tested in pure VHDL avoiding any vendor IP (Intellectual Property) preserving in this way its portability. A block diagram of the different entities on the code is shown in figure 9. The main duties for the FPGA included on the firmware are listed below.

- Communication with the CPLD using MPCI (Mini PCI) and hence with VME
- ADC data formatting for integrators
- Base line recovery and compensation
- Integration of the data coming from the ADCs using several integrators with different time settings
- Calculation of the intensities
- Calibrator control

![FPGA firmware block diagram](image)

**Figure 9.** FPGA firmware block diagram.

2.3 Software

One important advantage for TRIC is its remote configuration and control via VME. In order to utilize this feature, remote configuration software was implemented. This code covers all front-end and expert application features, and allows full remote control over the board. Currently two versions are implemented in PS complex:
1. **BCTTRIC** is designed for linacs, where only a portion of long beam signals (several $\mu$s) is necessary to quantify the beam average current, therefore also calibration is done by current (see figure 10).

2. **BCTFPS** is designed for transfer and ejection lines, where short beam signals (in the order of hundreds of nano seconds) are utilized, in this case all beam signals are used to quantify the beam using in this case beam intensity, therefore the calibration is done by voltage (charges).

![Figure 10. BCTTRIC Monitor expert GUI.](image)

Figure 10 shows the beam and calibration signals (1), measurement gates and its respective offset measurements are the white traces over the beam and calibration signals. Upper left part (2) shows the list of the selectable beams in the cycle while upper right part (3) shows current beam in the cycle. The different settings and acquisitions are shown in the left side (4).

The software architecture [3] for the new TRIC acquisition system is shown in figure 11. It is based on:

1. **BCTFPS/BCTTRIC**, a FESA (Front End Software Architecture) [2] acquisition server running locally under Linux on the VME FrontEnd Computers (FEC).

2. **BCTFPS Monitor or BCTTRIC Monitor**, a Java based expert graphical interface used for configuration and control of all the settings.

The BCTFPS/BCTTRIC is based on the FESA framework at CERN, and offers a variety of features e.g. realtime scheduling, beam-cycle synchronization, user notifications and the use of a shared memory model.

3 **Conclusions**

TRIC has become the new standard for beam intensity measurement in the PS complex. With 59 units installed: LINAC2 (9), LINAC3 (4), LINAC4 (5), AD (5), LEIR (8), PSB injection (11),
PSB ejection (3), TOF (1), TT2 (8), ISOLDE (4), PS (1) and 9 more planned in LINAC4, TRIC has completely replaced the old analogue system with very successful results [1]. It has upgraded intensity measurements making configuration and maintenance much easier and introducing a standard acquisition in order to obtain better results in the transfer efficiencies among different accelerators.

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