Training of Quantized Deep Neural Networks Using a Magnetic Tunnel Junction-Based Synapse

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Abstract. Quantized neural networks (QNNs) are being actively researched as a solution for the computational complexity and memory intensity of deep neural networks. This has sparked efforts to develop algorithms that support both inference and training with quantized weight and activation values, without sacrificing accuracy. A recent example is the GXNOR framework for stochastic training of ternary and binary neural networks (TNNs and BNNs, respectively). In this paper, we show how magnetic tunnel junction (MTJ) devices can be used to support QNN training. We introduce a novel hardware synapse circuit that uses the MTJ stochastic behaviour to support the quantize update. The proposed circuit enables processing near memory (PNM) of QNN training, which subsequently reduces data movement. We simulated MTJ-based stochastic training of a TNN over the MNIST, SVHN, and CIFAR10 datasets and achieved an accuracy of 98.61%, 93.99% and 83.02%, respectively (less than 1% degradation compared to the GXNOR algorithm). We evaluated the synapse array performance potential and showed that the proposed synapse circuit can train TNNs in situ, with $18.3 \frac{TOPs}{W}$ for feedforward and $3 \frac{TOPs}{W}$ for weight update.

Keywords — Magnetic Tunnel Junction, Memristor, Deep Neural Networks, Quantized Neural Networks
1. Introduction

Deep neural networks (DNNs) are the state-of-the-art solution for a wide range of applications such as computer vision and natural language processing. The classic DNN approach requires frequent memory accesses and is compute-intensive, requiring numerous multiply and accumulate (MAC) operations. For example, the ResNet50 network requires 3.9 billion MAC operations, while storing and accessing 25.5MB of weights [1]. As such, DNN performance is limited by computing resources and power budget. Therefore, efforts have been made to design dedicated hardware for DNNs [2, 3, 4]. These solutions support training with high resolution, such as 32-bit floating point. Still, DNN models are power-hungry and tend not to be suitable to run on low-power devices.

Ternary neural networks (TNNs) and binary neural networks (BNNs) are being explored as a way to reduce the computational complexity and memory footprint of DNNs. By reducing the weight resolution and activation function precision to quantized binary \([-1, 1]\) or ternary \([-1, 0, 1]\) values, the MAC operations are replaced by much less demanding logic operations, and the number of required memory accesses is significantly reduced. Such networks are also known as quantized neural networks (QNNs) [5]. The potential efficiency of QNNs has motivated research efforts to design novel algorithms that can support BNNs and/or TNNs without sacrificing solution performance (usually measured by prediction accuracy). These efforts include data quantization during training. In this work, we focus on the GXNOR training algorithm [6]. This algorithm uses a stochastic update function to facilitate the training phase. Unlike other algorithms [7, 8, 5], GXNOR does not require storing the full value (e.g., in a floating point format) of the weights and activations. Hence, GXNOR enables further reduction of the memory capacity during the training phase.

Emerging memory technologies, such as spin-transfer torque magnetic tunnel junction (STT-MTJ), can be used to design dedicated hardware to support in-situ DNN training, with parallel and energy-efficient operations. The near-memory computation enabled by these technologies also reduces overall data movement. The MTJ is a binary device, with two stable resistance states. Switching the MTJ device between resistance states is a stochastic physical process. While typically, stochastic switching is not a desirable property for memory cells to have, we exploit this feature to support QNN training.

Previous works used the stochastic behavior of the STT-MTJ, or other memristive technologies such as resistive RAM (RRAM), to implement hardware accelerators for BNNs [9, 10, 11, 12]. In [9], the research focus was on the architecture level of BNN accelerators, without supporting training. Other works implemented hardware for bio-inspired artificial neural networks (ANNs), using the spike-timing-dependent plasticity (STDP) training rule [10, 11]. Although STDP is widely used for bio-inspired ANNs, common DNNs are trained with gradient-based optimization such as stochastic gradient descent (SGD) and adaptive moment estimation (ADAM) [13]. A recently proposed MTJ-based binary synapse comprising a single transistor and a single MTJ device (1T1R) [12] supports training QNNs with binary weights and real value activations. [12] exploited analog computation to support processing near memory (PNM). Their design, however, requires two update operations to execute the SGD updates. Using real-valued activation will require high-resolution data converters, thereby increasing the area and power consumption of the proposed solution.

In this paper, we explore the stochastic behavior of the MTJ and leverage it to support fully quantized training (GXNOR). Our solution reduces the overall weight and read operations and the cost of the update phase. We propose a four-transistor, two-MTJ (4T2R) circuit for a ternary stochastic synapse and a two-transistor, single-MTJ (2T1R) circuit for a binary stochastic synapse, where the intrinsic stochastic switching behavior of the MTJ is used to perform a stochastic update function. Such a design enables highly parallel, energy-efficient, and accurate in-situ computation. Our designed synapse can support various DNN optimization algorithms, such as SGD and ADAM, which are used regularly in practical
applications.

We evaluated TNN and BNN training using the proposed MTJ-based synapse with PyTorch over the MNIST [14], SVHN [15], and CIFAR10 [16] datasets, where the circuit parameters were extracted from SPICE simulations using a GlobalFoundries 28nm FD-SOI process. Our results show that using the MTJ-based synapse for training yielded similar results as the ideal GXNOR algorithm, with a small accuracy loss of 0.7% for the TNN and 2.4% for the BNN.

This paper makes the following contributions. It

- Exploits the MTJ stochastic properties to support QNN stochastic training.
- Demonstrates MTJ applicability within the GXNOR framework. We show that PNM of stochastic QNN training is enabled using the MTJ-based synapse, with only a small accuracy reduction.
- Offers MTJ-based ternary and binary synapse circuits. These circuits:
  - Exploit the stochastic switching of the MTJ device to support a stochastic weight update algorithm,
  - Support in-situ weight update of standard optimization algorithms such as SGD and ADAM, without reading the weight data out of the synapse array,
  - Support near-memory processing of the feedforward and backpropagation computations, enabling high parallelism.

The rest of the paper is organized as follows. In Sections 2, background on DNN and QNN training and MTJ is given. Section 3 addresses the motivation of MTJ-based training. Section 4 describes the proposed MTJ-based ternary synapse. In Section 5, the ability of the proposed circuits to support TNN training is evaluated as well as their energy efficiency. In Section 6, a comparison to previous works is given. A conclusion is provided in Section 7. In the supplementary we explain how to modify the proposed circuits to support BNNs.

### 2. Preliminaries

#### 2.1. Deep Neural Networks

DNNs are machine learning models, that use connected layers, composed of neurons, to learn a desired functionality $F$. The different neuron layers are connected through weighted connections called synapses. For simplicity, this section focuses on a fully connected (FC) layer; however, a similar computation is done for layers with other weight connections, such as convolution layers (CONV) [2, 7, 8, 17]. In FC, the output is given by a matrix-vector multiplication

$$\tilde{\sigma} = W \tilde{x},$$

where the elements of matrix $W$ are the synapse weights, $\tilde{x}$ is the input neuron vector and $\tilde{\sigma}$ is the output. Hence, each element in the output vector $o_m$ is the weighted sum of the input,

$$o_m = \sum_{n=1}^{N} w_{mn} x_n,$$

where $N$, $o_m$, $w_{mn}$, and $x_n$ are, respectively, the number of input neurons, the output $m$, the synapse weights between neuron $m$ and neuron $n$, and the value of input neuron $n$. The following neuron layer is computed by passing $\tilde{\sigma}$ through a non-linear function, called an activation function $\sigma(\cdot)$ and is, therefore, given by

$$x^{(l+1)} = \sigma(\tilde{\sigma}^{(l)}) = \sigma(W^{(l)} x^{(l)}),$$

where $l$ is the layer index.
2.2. Training a DNN

In supervised learning, the network is trained to find the set of parameters, i.e., synapse weights, which approximates the desired functionality. The network is trained using a dataset \( D = \{ \mathbf{x}^{(0)}_i, \mathbf{d}_i \}_{i=1}^n \), where \( \mathbf{x}^{(0)}_i \) is the input vector of the network and \( \mathbf{d}_i \) is the desired output. During training, the network parameters \( w \) are calibrated to find the desired relation \( \mathbf{d} = \mathbf{F}(\mathbf{x}^{(0)}, W) \). To this end, a measure of quality is defined: the cost function \( C(\mathbf{d}, \mathbf{O}) \), where \( \mathbf{O} = \mathbf{F}(\mathbf{x}^{(0)}, w) \) is the output of the network. The goal of the learning algorithm is to find \( w \) that minimizes the value of \( C(\mathbf{d}, \mathbf{O}) \) with respect to the dataset. Hence, optimization algorithms are used to find the minimum of \( C \). Different optimization algorithms, such as SGD and ADAM, are used during DNN training [13]. During training, first the output and the cost function are computed in a stage called feedforward. After the cost function is known, the error of each layer \( \mathbf{y}^l \) is computed in a stage called backpropagation. The error is computed using the chain rule and is given by

\[
\mathbf{y}^{(l)} \triangleq (W^{(l+1)}(\mathbf{y}^{(l+1)})) \cdot \sigma'(\mathbf{O}^{(l)}),
\]

where \( W^T \) is the transpose of the weight matrix \( W \), and \( \sigma' \) is the derivative of \( \sigma \) with respect to \( \mathbf{y} \). Taking the computed error of the layer, the weight gradients are computed and used to update the weights. Usually, the weight update rule is given by

\[
W^{(l)} = W^{(l)} + f_{opt}(a^l, y^l, W^l),
\]

where \( f_{opt} \) is defined by the optimization algorithm that is used.

General DNNs do not limit the value of the weights, which can be any real value. Typically, the unconstrained parameters are represented by precision higher than 1 or 2-to-32-bit floating point. The following section describes a framework to train QNNs.

2.3. Training Quantized Neural Networks with a Stochastic Update Rule

In recent years, efforts have been made to make DNN models more hardware-compatible. Quantization methods have been explored, where the DNN weights and activation functions are constrained to being discrete values such as binary \( \{-1, 1\} \) or ternary \( \{-1, 0, 1\} \) values. For BNNs and TNNs, MAC operations are replaced with the simpler XNOR or Gated-XNOR (GXNOR) logic operations, respectively. The memory footprint of the quantized network is dramatically reduced (for example, for ResNet50, with ternary weights and activations, the memory capacity is cut in half during training and by 16 during inference).

This section describes the GXNOR framework [6] that constrains the weights and activations to the quantized space while training the QNN. We focus on the differences between the GXNOR training algorithm and regular DNN training.

2.3.1. Quantized Weights and Activations

The quantized space \( Z_N \) is defined by

\[
Z_N = \left\{ \frac{n}{2^N-1} - 1 | n = 0, 1, \ldots, 2^N \right\} \in [-1, 1],
\]

where \( N \) is a non-negative integer that defines the space values. For example, the binary space is given for \( N = 0 \) and the ternary space for \( N = 1 \). The quantized space resolution, i.e., the distance between two adjacent states, is given by

\[
\Delta z_N = \frac{1}{2^{N-1}}.
\]
2.3.2. Feedforward and Backpropagation

In QNNs, the quantized activation function is a step function, where the number of steps is defined by the space. To support backpropagation through the quantized activations ($\varphi_r$), the derivative of the activation function is approximated. In this work, the ideal derivative is approximated by a sum of window functions. The window function is given by

$$\frac{\partial \varphi_r(x)}{\partial x} = \begin{cases} \frac{1}{2a}, & \text{if } r - a \leq x \leq r + a, \\ 0, & \text{others} \end{cases}$$

where $r$ and $a$ are positive hyperparameters, defining the sparsity of the neurons (i.e., the quantization range) and the window function width, respectively. Using the approximated derivative, the backpropagation of the GXNOR training algorithm is computed with no further changes compared to regular DNNs.

2.3.3. Weight Update

To support training with weights constrained to the discrete weight space (DWS), the GXNOR algorithm uses a stochastic gradient-based method to update the weights. First, the update value is computed by an optimization algorithm (e.g., SGD, ADAM, RMSprop). Then, a boundary function is defined to guarantee that the updated value will not exceed the $[-1,1]$ range. The boundary function is

$$\varrho(W^l_{ij}(k), \Delta W^l_{ij}(k)) = \begin{cases} \min(1 - W^l_{ij}(k), \Delta W^l_{ij}(k)), & \text{if } \Delta W^l_{ij}(k) > 0, \\ \max(-1 - W^l_{ij}(k), \Delta W^l_{ij}(k)), & \text{else} \end{cases}$$

where $W^l_{ij} \in \mathbb{Z}_N$ is the synaptic weight between neurons $j$ and $i$ of the following layer $(l+1)$, $\Delta W^l_{ij} \in \mathbb{R}$ is the gradient-based update value, and $k$ is the update iteration. Then, the update step is given by

$$W^l_{ij}(k + 1) = W^l_{ij}(k) + \Delta w^l_{ij}(k),$$

where $\Delta w^l_{ij}(k) = \mathcal{P}(\varrho) \in \mathbb{Z}$ is the discrete update value, obtained by projecting $\varrho(\Delta W^l_{ij}(k))$ to a quantized weight space. $\mathcal{P}(\varrho)$ is a probabilistic projection function defined by

$$\mathcal{P}(\varrho) = \begin{cases} \kappa_{ij} \Delta z_N + \text{sign}(\varrho) \Delta z_N, & \text{w.p. } \eta(\nu_{ij}) \\ \kappa_{ij} \Delta z_N, & \text{w.p. } 1 - \eta(\nu_{ij}) \end{cases},$$

where $\kappa_{ij}$ and $\nu_{ij}$ are, respectively, the quotient and remainder values of $\varrho$ divided by $\Delta z_N$, and

$$\eta(\nu) = \tanh \left( m \cdot \frac{\nu}{\Delta z_N} \right) \in [0,1],$$

where $m$ is a positive hyperparameter. Hence,

$$\Delta w^l_{ij} = \kappa_{ij} \Delta z_N + \text{sign}(\nu_{ij}) \text{Bern}(\eta(\nu_{ij})) \Delta z_N,$$

where $\text{Bern}(\eta(\nu_{ij}))$ is a Bernoulli random variable with parameter $\eta(\nu_{ij})$.

In this paper, which focuses on TNN, the ternary weight space (TWS) is given by $N = 1$ and $\Delta z_1 = 1$. Figure 1 illustrates examples of TNN weight updates for $W = -1$ and $W = 0$. Further discussion of the BNN implementation is found in the supplementary material.

Dedicated hardware for TNN and BNN can fully exploit the potential of these networks. In this paper, we propose to use emerging memory technology, i.e., STT-MTJ, to support PNM of TNNs and BNNs.
2.4. Magnetic Tunnel Junction

An MTJ device comprises two ferromagnetic layers, a fixed magnetization layer and a free magnetization layer, separated by an insulator layer, as illustrated in Figure 2. The resistance of the device is defined by the relative magnetization of the free layer as compared to the fixed magnetization layer to the free layer, the resistance may switch to a parallel magnetization state (P) leads to low resistance ($R_{on}$) and an anti-parallel state (AP) leads to high resistance ($R_{off}$). The device resistance can be switched by the current flow through the device. When the current flows from the free layer to the fixed layer, the resistance may switch to $R_{on}$. Likewise, when the current flows from the fixed layer to the free layer, the resistance may switch to $R_{off}$. The switching probability of the MTJ device depends on the current’s magnitude, when three work regimes are defined as: 1) low current, low switching probability, 2) intermediate current, and 3) high current, high switching probability [11]. As we are interested in fast switching time, this work focuses on the high current regime. Therefore, current $I$ is substantially higher than critical current $I_{cr}$, and is given by

$$I_{cr} = \frac{2|e|\alpha V(1\pm P)}{P} \mu_0 M_s M_{eff}$$

where $\alpha$, $M_s$, $V$, $P$, $M_{eff}$ are, respectively, the Gilbert damping, the saturation magnetization, the free layer volume, the spin polarization of the current, and the effective magnetization [18]. The switching time is, therefore,

$$\tau = \frac{2}{\alpha \gamma \mu_0 M_s} I - I_{cr} \log \left( \frac{\pi}{2|\theta|} \right),$$

where $\gamma$ is the gyromagnetic ratio, and $\theta$ is the initial magnetization angle [18], given by a normal distribution $\theta \sim \mathcal{N}(0, \theta_0)$, $\theta_0 = \sqrt{k_B T/(\mu_0 H_k M_s V)}$, where $H_k$, $K_b$ and $T$ are the shape anisotropy field, the Boltzmann constant and temperature, respectively. In this work, we use current pulses with varying time intervals to control the MTJ switching probability and to support the stochastic weight update given by (13).

3. Stochastic In-Situ Training

The training scheme suggested in [6] reduces the memory footprint of the training phase. Still, every update iteration (Eq. (10)) requires reading the weights, computing the stochastic update step, and writing the new weight value. Computing the stochastic update will require the use of a random number generator (RNG). Adding RNG will increase the complexity of the design, in terms of having to transfer the random numbers to all the weights, area overhead of the RNG circuit and the resulting power consumption. For example, assume 128 weights are read in 100ns [17], to generate 128 8-bit random numbers at this rate, the RNG design requires 64 PRNG circuits [19]. We suggest replacing the RNG functionality with the stochastic write operation of the MTJ device. Our approach replaces the read-PRNG-write loop with a single stochastic-write operation. Moreover, working with the
MTJ in a stochastic write regime allows us to work with shorter write intervals. Other emerging memory technologies also have stochastic write models that might be a good fit to the expression in (12). Nevertheless, training requires numerous write operations; for example, one network training with 1000 training epochs requires $5 \cdot 10^7$, and $10^8$ writes per device for CIFAR-10 and ImageNet datasets, respectively. Thus, a STT-MTJ device, which has the high reported endurance, is a leading candidate for stochastic in-situ training [20].

4. MTJ-Based Ternary Synapses

We now describe the proposed ternary synapse circuit that supports stochastic GXNOR training. In the supplementary, we explain how the proposed synapse can support binary weights as well.

4.1. Training TNN Using an MTJ-Based Synapse

First, we describe how we leverage the stochastic switching behavior of the MTJ device to perform the stochastic update function. Two MTJ devices are needed to represent ternary weight, where the weight is defined and stored as the combination of the resistances of the two MTJs. Table 1 lists the different values of the synapse weight as a function of the MTJ’s resistance. To support the stochastic weight update, both MTJ devices might be switched during an update. To switch the state of the MTJ device, a voltage pulse $V_{up}$ is applied across the device, for time interval $\Delta t \in [0,T_{up}]$. For a fast update operation, the update is performed in the high current domain guaranteed by $V_{up}$. The resultant current direction and the pulse time interval determine the switching probability. Using (15) and the voltage pulse, the switching probability of the MTJ is

$$P_{sw}(\Delta t) = 1 - \text{erf} \left( \frac{\pi}{2\sqrt{2\theta_0} \exp \left( \frac{\Delta t V_{up}}{CR} \right)} \right),$$

(16)

where $C = \frac{2I_c}{\alpha \gamma \mu}$, and $R$ is the device resistance. As indicated in Eq. (16), $P_{sw}$ is a function of the voltage pulse amplitude and time interval. Therefore, $T_{up}$ is set to guarantee that if $\Delta t = T_{up}$, then $P_{sw} \approx 1$. Moreover, $P_{sw}$ is a function of the current direction flows through the MTJ and the state of the MTJ device.

To better understand the update operation of a single synapse, in this section we consider the simplified synapse illustrated in Figure 2. Each MTJ update is independent; this is guaranteed by applying different voltage pulses $V_1, V_2$ on each synapse and connecting the node between the MTJs to the ground. In this manner, each MTJ is updated according to (16). To support the GXNOR update, we need to control the switching probability of each MTJ device according to the update value ($\Delta W$) and the synapse weight. To this end, we (i) define $V_{app} = V_1 - V_2$, (ii) enforce opposite polarities of $V_1$ and $V_2$ (i.e., $\text{sign}(V_1) \neq \text{sign}(V_2)$), and (iii) set $\text{sign}(V_{app}) = \text{sign}(\Delta W)$.
Training of Quantized Deep Neural Networks Using a MTJ-Based Synapse

Figure 2: Simplified model of the ternary synapse. The synapse weight is defined by the resistance combination of $R_1$ and $R_2$. As listed in Table 1 each weight has four possible values $w \in \{-1, 0_s, 0_w, 1\}$.

Following this work scheme, if $\Delta W > 0$, the current directions guarantee that only a synapse with weight $W = -1$ or $W = 0_s$ can switch. Similarly, if $\Delta W < 0$, the current directions guarantee that only a synapse with weight $W = 1$ or $W = 0_w$ can switch.

Next, we need to ensure that the switching probability will follow Eq. (13) and will be a function of the update value $\Delta w = \kappa + \text{sign}(\nu) \text{Bern}(\eta(\nu))$. As indicated by Eq. (16), the pulse duration $\Delta t$ sets the switching probability. To support (13), we set the pulse duration of $V_1$ and $V_2$ to be a function of $\kappa$ or $\nu$, where $\kappa = \{0, 1, 2\}$ and $\nu \in [0, 1]$. If $\Delta W > 0$, the pulse duration of $V_1$ is set by $\kappa$. Hence, $\Delta t_{V_1} = f(\kappa) = \mathbb{1}_{\kappa \neq 0} \tau_{up}$. The pulse duration of $V_2$ is set by $\nu$; so, $\Delta t_{V_2} = f(\nu) = \nu \tau_{up}$. Similarly, if $\Delta W < 0$, then $\Delta t_{V_1} = f(\nu)$ and $\Delta t_{V_2} = \mathbb{1}_{\kappa \neq 0} \tau_{up}$.

Following this methodology, at each weight update, one MTJ is updated as a function of $\kappa$, while the other is updated as a function of $\nu$, depending on the sign of $\Delta W$. Thus, if $\kappa \neq 0$, the MTJ switching probability is approximately 1 and the switching probability is given by the indicator variable $P_{sw, \kappa} = \mathbb{1}_{\kappa \neq 0}$. Since $\nu$ is a fraction, the switching probability of the other MTJ with respect to $\nu$ is a Bernoulli variable with probability $P_{sw, \nu} = P(\nu \tau_{up})$. Therefore, the MTJ-based synapse update is given by

$$\Delta w = \text{sign}(\Delta W)(P_{sw, \kappa} + P_{sw, \nu}) = \text{sign}(\Delta W)(\mathbb{1}_{\kappa \neq 0} + \text{Bern}(P(\nu \tau_{up}))); \quad (17)$$

see examples in Section 4.4.

The MTJ-based synapse update differs from the ideal GXNOR update in that it supports two zero states, and uses similar, but not identical, switching probabilities ($P_{sw} \approx \eta$).

4.2. Proposed Synapse Circuit and Synapse Array

Synapse Circuit A schematic of the proposed ternary synapse is shown in Figure 3a. The ternary synapse is composed of two MTJ devices connected via their fixed layer port. The free layer port of each MTJ is connected to two access transistors. This synapse is inspired by previous work [4, 21], but we replace the RRAM by the MTJ device, and two synapse structures are added together to support the ternary weight. In contrast to [4, 21] which supports full-precision analog weight values, the MTJ-based synapse supports quantized weights and stochastic weight updates. Sections 4.3 and 4.5 describe how our design is optimized to support quantized weights.

Synapse Array The synapse circuit shown in Figure 3a is the basic cell of an array structure, as shown in Figure 3b. The synapses are arranged in an $M \times N$ array, where
each synapse is indexed by \((m, n)\). Each synapse in column \(n \in [1, N]\) is connected to four inputs \(\{u_{n1}, u_{n2}, u_{n3}, u_{n4}\}\), where all the input voltages are shared among all synapses in the same column. Likewise, each synapse in row \(m \in [1, M]\) is connected to control signals \(\{e_{m(1, n)}, e_{m(1, p)}, e_{m(2, n)}, e_{m(2, p)}\}\). The control signals are shared among all synapses in the same row. The synapse located in \((m, n)\) produces an output current \(I_{mn}\), which contributes to the current through output row \(m\). The operations on the synapse array are performed in the analog domain and accumulate according to Kirchoff’s current law (KCL), where the GXNOR output is represented by the current.

### 4.3. Stochastic Weight Update

We now explain how the synapse circuit is designed and how the input and control signals are set to support the GXNOR stochastic update scheme. Unlike weight updates in standard DNN, the proposed synapse supports the quantized update scheme suggested in [6].

#### 4.3.1. Weight Update Step

Similar to [4, 22], four transistors are added to support parallel synapse updates. The control signals of these transistors dictate the weight update functionality by controlling the current direction and the voltage pulse time interval in the synapse array. The update step can be performed in parallel for all the synapses in the same array, depending on the optimization algorithm used. Since the GXNOR algorithm can use any optimization algorithm to compute the gradient-based update value (Section 2.3.3), we consider two update cases: (i) supporting general optimization algorithms, such as ADAM, and (ii) supporting the SGD algorithm. Table 2 summarizes the circuit level signals as a function of the GXNOR variables.

**Support of General Optimization Algorithms** To support general optimization algorithms, the update value \(\Delta W\) is computed in a peripheral circuit to the synapse array; thus, \(\Delta W\) is given as an input to the array. The array columns are updated sequentially, i.e., a single column is updated per iteration. During this operation, the input voltages are set to \(u_1 = u_2 = V_{up} > 0\) in the active column, \(u_1 = u_2 = -V_{dd}\) for the rest of the columns, and the output row interface connects the rows to ground. To support the stochastic update
(Section 4.1), the control signals are given by

\[
\begin{align*}
\epsilon_{1,p} &= -\epsilon_{2,p} = -\text{sign}(\Delta W)V_{dd}, & \text{if } \kappa \neq 0 \\
\epsilon_{1,p} &= \epsilon_{2,p} = V_{dd}, & \text{else}
\end{align*}
\]

\[\tag{18}\]

\[
\epsilon_{1,n} = \begin{cases} 
-\text{sign}(\Delta W)V_{dd}, & 0 < t < |\nu|T_{up} \\
-V_{dd}, & |\nu|T_{up} < t < T_{up}
\end{cases}
\]

\[\tag{19}\]

\[
\epsilon_{2,n} = \begin{cases} 
\text{sign}(\Delta W)V_{dd}, & 0 < t < |\nu|T_{up} \\
-V_{dd}, & |\nu|T_{up} < t < T_{up},
\end{cases}
\]

\[\tag{20}\]

where \(\Delta W, \nu, \text{ and } \kappa\) are as defined in Section 2.3. Hence, the MTJ is updated proportionally to \(\kappa = |\Delta W|\) and \(\nu = \text{remainder}(\Delta W/\Delta z_1)\), meaning that for a single synapse, one MTJ is updated using a pulse width of \(\Delta t = 1_{|\kappa| \geq 0}T_{up}\), while the other is updated using a pulse width of \(\Delta t = |\nu|T_{up}\). We assume that \(\kappa\) and \(\nu\) are inputs to the synapse array.

**Support of Stochastic Gradient Descent**

This update scheme is similar to the update scheme proposed in [3]. When the SGD algorithm is used to train the network, all the synapses in the array are updated in parallel. Therefore, in this section, we denote the array row and column indexes by \(i\) and \(j\), respectively. To support SGD training, minor changes need to be made to the general update scheme. Using SGD, the update is given by the gradient value, and is equal to \(\Delta W = xy^T\), where \(y\) is the error propagated back to the layer, achieved using the backpropagation algorithm, and \(x\) is the input. For TNNs and BNNs, the input activations are \(u \in \{-1,0,1\} = \{-V_{up}, 0, V_{up}\}\) and \(u \in \{-1,1\} = \{-V_{up}, V_{up}\}\), respectively; thus, \(\Delta W_{ij} = y_iu_j\) or \(\Delta W_{ij} = 0\) for \(u_j = 0\). In this scheme, the voltage sources retain the activation values, so \(u_1 = u_2 = V(x)\) (whereas in the general scheme they are set to \(u_1 = u_2 = V_{up}\)). The control signals are a function of the error \(y\); so, \(\kappa_{ij} = |y_i|\) and \(\nu_{ij} = \text{remainder}(y_i/z_1)\) (whereas in ADAM and other optimization algorithms they are a function of the update value \(\Delta W\)). The control signal functionality for SGD is

\[
\begin{align*}
\epsilon_{i,(1,p)} &= -\epsilon_{i,(2,p)} = -\text{sign}(y_i)V_{dd}, & \text{if } \kappa_{ij} \neq 0 \\
\epsilon_{i,(1,p)} &= \epsilon_{i,(2,p)} = V_{dd}, & \text{else}
\end{align*}
\]

\[\tag{21}\]

\[
\epsilon_{i,(1,n)} = \begin{cases} 
-\text{sign}(y_i)V_{dd}, & 0 < t < |\nu_{ij}|T_{up} \\
-V_{dd}, & |\nu_{ij}|T_{up} < t < T_{up}
\end{cases}
\]

\[\tag{22}\]

\[
\epsilon_{i,(2,n)} = \begin{cases} 
\text{sign}(y_i)V_{dd}, & 0 < t < |\nu_{ij}|T_{up} \\
-V_{dd}, & |\nu_{ij}|T_{up} < t < T_{up},
\end{cases}
\]

\[\tag{23}\]

The functionality of the control signals remains unchanged compared to the general update scheme, except that the voltage source is selected according to \(y\), and the voltage sign and the effective update duration are set as a function of the integer \(\kappa\) and the fraction \(\nu\) values of \(y\), respectively. Therefore, the update equation is given by

\[
\Delta W_{ij} = \text{sign}(y_i)\text{sign}(u_j)(1_{\kappa \neq 0} + \text{Bern}(P_{sw}(\nu_{ij}))),
\]

\[\tag{24}\]

where \(\text{sign}(y_i)\text{sign}(u_j) = \text{sign}(\Delta W_{ij})\).

**4.4. Ternary Synapse Update Examples**

To demonstrate the proposed update scheme, two examples of synapse updates are given. Each example shows how a different weight is updated based on a calculated \(\Delta W\). The control signals open the transistors according to the \(\Delta W\).
Table 2: Weight Update – Summary of Circuit Level Signals as a Function of GXNOR Variable Values

| Update Case | Row signal | $u_1 = u_2$ | $e_{1,n}$ | $e_{1,p}$ | $e_{2,n}$ | $e_{2,p}$ |
|-------------|------------|-------------|-----------|-----------|-----------|-----------|
| $\Delta W > 0$ | $\Delta W > 0$ | $y > 0$ | $V_{up}$ | $u$ | $-V_{dd}$ | $-V_{dd}$ | $\left\{ \begin{array}{ll} V_{dd}, & 0 < t < |\nu_j| \tau_{up} \\ -V_{dd}, & |\nu_j| \tau_{up} < t < \tau_{up} \end{array} \right.$ | $V_{dd}$ |
| $\Delta W < 0$ | $\Delta W < 0$ | $y < 0$ | $V_{up}$ | $u$ | $-V_{dd}$ | $-V_{dd}$ | $\left\{ \begin{array}{ll} V_{dd}, & 0 < t < |\nu_j| \tau_{up} \\ -V_{dd}, & |\nu_j| \tau_{up} < t < \tau_{up} \end{array} \right.$ | $V_{dd}$ |
| $\Delta W/\kappa/\nu = 0$ | $\Delta W$ | $y$ | $V_{up}$ | $u$ | $-V_{dd}$ | $-V_{dd}$ | $-V_{dd}$ |

4.4.1. Example 1: $W = -1$ and positive update value  
Figure 1a shows the case where a synapse weight is $W = -1$ and the update value is $\Delta W = 1.5$. Thus, $\kappa = 1$ and $\nu = 0.5$. Hence, $e_{1,p} = -e_{2,p} = -V_{dd}$; therefore, $P_1$ is ON and $P_2$ is OFF for time interval $\tau_{up}$. $e_{1,n} = -V_{dd}$ for $\tau_{up}$ and $e_{2,n}$ is ON for $0.5 \tau_{up}$, as given by

$$e_{2,n} = \left\{ \begin{array}{ll} V_{dd}, & 0 < t < 0.5 \tau_{up} \\ -V_{dd}, & 0.5 \tau_{up} < t < \tau_{up}. \end{array} \right.$$ (25)

Hence, the probability of $R_1$ and $R_2$ switching is $P_{sw,1} \approx 1$ and $P_{sw,2} = P(0.5 \tau_{up})$, respectively. In this example, the synapse weight will be updated from $W = -1$ to $W = 0$ with a probability of

$$P_{-1 \rightarrow 0} = P_{-1 \rightarrow 0_n} + P_{-1 \rightarrow 0_s} = P_{sw,1}(1 - P_{sw,2}) + (1 - P_{sw,1})(1 - P_{sw,2}) \approx (1 - P_{sw,2}),$$ (26)

and can switch to 1 with a probability of

$$P_{-1 \rightarrow 1} = P_{sw,1}P_{sw,2} \approx P_{sw,2}.$$ (27)

Note that when $W = -1$, $\{R_1, R_2\} = \{R_{off}, R_{on}\}$. Thus, if $\Delta W < 0$, due to the current that flows from $R_2$ to $R_1$, both MTJs cannot switch and the state will remain unchanged.

4.4.2. Example 2: $W = 0$ and negative update value  
Figure 1b shows the case where a synapse weight is $W = 0$ and the update value is $\Delta W = -0.5$. Thus, $\kappa = 0$ and $\nu = -0.5$. Consequently, $e_{1,p} = e_{2,p} = V_{dd}$, so both $P_1$ and $P_2$ are closed for $\tau_{up}$. $e_{2,n} = -V_{dd}$ for $\tau_{up}$ and the transistor connected to $e_{1,n}$ is open for $0.5 \tau_{up}$, as given by

$$e_{1,n} = \left\{ \begin{array}{ll} V_{dd}, & 0 < t < 0.5 \tau_{up} \\ -V_{dd}, & 0.5 \tau_{up} < t < \tau_{up}. \end{array} \right.$$ (28)

Therefore, only $R_1$ can switch with a probability of $P_{sw,1} = P(0.5 \tau_{up})$. In this example, the synapse weight is updated from $W = 0$ to $W = -1$, with a probability $P = P_{sw,1}$. Although, theoretically, no current should flow through $R_2$, it might switch from $R_{on}$ to $R_{off}$ due to leakage currents with probability $P_{sw,2} << 1$.

4.5. Feedforward and Backpropagation

TNN training requires the circuits to support the feedforward and backpropagation stages [21]. The feedforward stage requires to compute matrix-vector or matrix-matrix multiplication; in TNNs, the multiplication is replaced with the gated XNOR (GXNOR) operation. The GXNOR logic outputs zero if one of the inputs is zero; otherwise, it outputs the XNOR operation between the inputs.
In this section, we first explain how our synapse performs the GXNOR operation and then how the synapse array is used to perform the near-memory quantized matrix-vector multiplication. When supporting training, the feedforward stage is followed by computation of the error of each layer, known as the backpropagation stage. This stage requires computation of the matrix-vector multiplication between the transposed weight matrix \((W^T)\) and the layer error vector \((y)\). In the following sections, we denote the matrix-vector multiplication of \(W^Ty\) as “backpropagation”.

### 4.5.1. Gated XNOR

To perform the GXNOR logic operation between the synapse and activation values [3], we denote the input neuron values as the voltage sources. Accordingly, \(u = V(a)\) is the voltage representing input value \(a\). The logic values of the input neuron \(a \in \{-1, 0, 1\}\) are represented by \(u \in \{-V_{vd}, 0, V_{rd}\}\). \(V_{rd}\) is set to guarantee the low current regime of an MTJ, so the switching probability is negligible. During this operation, \(u_1 = u, \bar{u}_2 = -u, \{e_{1, 1}, e_{1, 0}, e_{2, 1}, e_{2, 0}\} = \{-V_{dd}, -V_{dd}, V_{dd}, V_{dd}\}\) and the synapse output node is grounded. The result is given by the output current sign,

\[
I_{out} = (G_1 - G_2)u,
\]

where \(G_{1, 2}\) is the conductance of each MTJ device, respectively. As listed in Table [1] the polarity of \(I_{out}\) depends on the input voltage and the synapse weight. If \(u = 0\) or \(W = \{0_u, 0_a\}\), the output current is \(I_{out} \approx 0\). If the weight and input have the same polarity, then \(\text{sign}(I_{out}) = 1\), else \(\text{sign}(I_{out}) = -1\).

#### 4.5.2. Feedforward

The quantized feedforward operation is given by

\[
O_m = \sum_{n=1}^{N} GXNOR(W_{mn}, x_{n}), \forall m \in [1, M],
\]

where \(O_m\) is the result of row \(m\). During this operation, each column voltage is mapped to the corresponding input activation \((u_n = V(a_n), \forall n \in [1, N])\), the output row interface

![Diagram](image-url)

**Figure 4:** Examples of synapse updates. Blue circles represent the logic state of the weight, where the initial state is marked by an orange outline.
connects the rows to ground. Thus, each synapse computes the GXNOR operation between its input and stored weight and the output currents from all synapses are summed based on KCL. Thus, the current through row \(i\) is

\[
I_{\text{row},i} = \sum_{j=1}^{N} (G_{ij,R_1} - G_{ij,R_2}) u_j = \frac{R_{\text{off}} - R_{\text{on}}}{R_{\text{off}} R_{\text{on}}} (N_{+1,i} - N_{-1,i}) V_{rd},
\]

where \(G_{ij,R_{(1,2)}}\) is the conductivity of each MTJ, \(N\) is the number of synapses per row, \(N_{+1,i}\) is the total number of positive products in row \(i\), and \(N_{-1,i}\) is the total number of negative products in row \(i\).

### 4.5.3 Backpropagation

To train the TNN, backpropagation of the error must be performed. Therefore, the synapse array also supports the matrix-vector multiplication \(W^T y\). Rather than storing \(W^T\) in a dedicated array, we reuse the same array, which stores \(W\), similarly to [4]. During this operation, the output row interface is used as an input and the output is given by the current measured in the columns. Due to the synapse structure, the current is separated into two columns, as shown in Figure 3c. Therefore, the operation result is given by the current difference

\[
I_{\text{col},j} = \sum_{i=1}^{M} (I_{ij,R_1} - I_{ij,R_2}) = \sum_{i=1}^{M} (G_{ij,R_1} - G_{ij,R_2}) y_i,
\]

where \(y_i\) is the layer’s error. The current through each column pair is converted to voltage, and the result is computed using a voltage comparator.

### 5. Evaluation and Design Considerations

This section presents the performance evaluation of the MTJ-based QNN training. The functionality, power and area of the synapse circuit and array were evaluated in Cadence Virtuoso and used for the training simulations. The MTJ-based design of the GXNOR algorithm (MTJ-GXNOR) is compared to a software implementation of the algorithm (GXNOR in our terminology).

#### 5.1. Methodology

Our proposed circuit is a hardware implementation of the GXNOR framework used to train QNNs [6]. We evaluate our design using four metrics:

(i) **Circuit Evaluation (Section 5.2)**. We validated the circuit operations needed to support the MTJ-GXNOR framework. Our circuit needs to support a stochastic update, the GXNOR, and backpropagation operations. The MTJ switching operation was evaluated by running Monte Carlo simulation of the MTJ transient response. We evaluated the GXNOR and backpropagation operations using SPICE simulations.

(ii) **Training Simulation (Section 5.3)**. To validate that our proposed synapse can be used to train QNNs and reach comparable results to the GXNOR algorithms and other state-of-the-art QNN frameworks [6, 7, 8], we simulated MTJ-GXNOR training in PyTorch with the hardware circuit parameters extracted from the circuit evaluation.

(iii) **MTJ-GXNOR Sensitivity to Process Variation (Section 5.4)**. The MTJ-GXNOR training performance is influenced by the device variation and environmental changes. Hence, we evaluated the sensitivity of the MTJ-GXNOR test accuracy considering process and environmental variations.

(iv) **Hardware Performance Evaluation (Section 5.5)**. Our design can be integrated into different architectures, each leading to a different performance. Here, we report on the performance of our basic cells – the hardware synapse and synapse array. We also consider a simple system test case comparable with previous solutions.
5.2. Circuit Evaluation

The synapse circuit was designed and evaluated in Cadence Virtuoso for the GlobalFoundries 28nm FD-SOI process. The MTJ device is based on device C from [15] and its parameters are listed in Table 3. To achieve higher switching probability, the magnetization saturation ($\mu_0 M_s$) was changed according to [23].

The read voltage, $V_{rd}$, was set to guarantee a low-current regime and negligible switching probability for the feedforward and backpropagation operations. Likewise, the update voltage, $V_{up}$, was set to guarantee a high-current regime. The update time period was set to match $P_{sw}(T_{up}) \approx 1$.

5.2.1. Circuit Schematic Model

The transistors and interconnect affect the circuit’s functionality and performance. Therefore, we adopted a circuit model that considers the parasitic resistance and capacitance of wires and transistors. The model considers the location of the synapse. An illustration of the schematic circuit model appears in the supplementary material (Section 2). Using the schematic circuit model, and SPICE simulations, we evaluate the circuit array and operations. We considered the corner cases, i.e., the synapses located at the four corners of the synapse array, to evaluate the worst-case scenario for the effect of the wires and transistors on operation results, latency, and power consumption. For all circuit simulations, we considered the worst case, where the wire resistance and capacitance are the most significant, i.e., for an array of size $M \times N$, the synapse located at [M,1].

5.2.2. MTJ Switching Simulation

To evaluate the transition in the resistance of the MTJ and its impact on the operation of the synapse, we performed a Monte Carlo simulation of the MTJ operation. The simulation numerically solves the Landau–Lifshitz–Gilbert (LLG) [24, 11] differential equation (assuming the MTJ is a single magnetic domain) with the addition of a stochastic term for the thermal fluctuations [25] and Slonczewski’s STT term [26]. For each iteration of the Monte Carlo simulation, a different random sequence was introduced to the LLG equation and the resulting MTJ resistance trace was retrieved. The equation was solved using a standard midpoint scheme [27] and was interpreted in the sense of Stratonovich, assuming no external magnetic field [28] and a voltage pulse waveform. The resistance of the MTJ was taken as $R_{on} \frac{1 + P^2}{1 + P^2 \cos \theta}$ [29], where $\theta$ is the angle between magnetization moments of the free and fixed layers and $P$ is the spin polarization of the current. To approximate the time-variation resistance of an MTJ during the switch between states, all the traces from the Monte Carlo simulation were aligned using the first time that the resistance of the MTJ reached $\frac{R_{on} + R_{off}}{2}$. After the alignment, a mean trace was extracted and used for the fit. This fit was used as the time-variation resistance when the MTJ made a state switch.

5.2.3. GXNOR Operation

The GXNOR operation for a single synapse is shown in Figure 5. When either the activation (input) or the weight ($W$) is zero, the output current is one order of magnitude lower than in the other cases.

5.3. MTJ-GXNOR Training Simulation

To evaluate the training performance of our solution, we determined the test accuracy, and compare it to the original GXNOR algorithm implemented in software and to other state-of-the-art frameworks. We denote our results as ‘MTJ-GXNOR’ and the ideal GXNOR algorithm as ‘GXNOR’. We tested the quantized networks over the MNIST, SVHN and CIFAR10 datasets [14, 15, 16]. The following three quantization resolutions were simulated in PyTorch: (i) a full ternary network (‘MTJ-GXNOR TNN’), (ii) a full binary network (‘MTJ-GXNOR BNN’), and (iii) a network with ternary weight and binary activations (‘MTJ-GXNOR Bin-Activation’). For the MNIST and SVHN dataset we
Table 3: Circuit Parameters

| MTJ, device C \[18\] | Parameter | Value | Parameter | Value |
|------------------------|-----------|-------|-----------|-------|
|                        | \(a\) [nm] | 50    | Temp. [K] | 300   |
|                        | \(b\) [nm] | 20    | \(R_{on}\) [\(\Omega\)] | 1500 |
|                        | \(t_f\) [\(\text{nm}\)] | 2.0   | \(R_{off}\) [\(\Omega\)] | 2500 |
|                        | \(\mu_0 M_s\) [T\(\uparrow\)] | 0.5   | \(\alpha\) | 0.01  |
|                        | \(I_{co}\) [\(\mu\text{A}\)] | 157   | \(\theta_0\) | 0.345 |

| CMOS                   | Parameter | Value | Parameter | Value |
|------------------------|-----------|-------|-----------|-------|
|                        | \(V_{DD}\) [V] | 1     | \(W/L_{PMOS}\) | 33    |
|                        | \(V_{SS}\) [V] | \(-1\) | \(W/L_{NMOS}\) | 20    |
|                        | \(V_{up}\) [V] | 1     | \(T_{up}\) [\(\text{ns}\)] | 2     |
|                        | \(V_{rd}\) [V] | 0.1   | \(T_{rd}\) [\(\text{ns}\)] | 0.5   |

\(\dagger\) To achieve higher switching probability, the value of \(\mu_0 M_s\) was changed according to \[23\].

Figure 5: GXNOR operation between the input voltage \(V_{in} \in \{-1, 0, 1\} = \{-V_{rd}, 0, V_{rd}\}\) and the weight value (\(W\) in the figure). During the GXNOR operation (read operation), \(V_{rd}\) is 0.1V to guarantee a low-current domain and low switching probability. For \(V_{in} \neq 0\) and \(W = 0\) \(w/s\), the output current is not zero. This is a source for error when the GXNOR results are summed to compute the activation value. Limiting the dimensions of the synapse array can mitigate this effect.

trained the same convolution neural networks described in \[6\]. The network architecture is “32CONV5-MP2-64CONV5-MP2-512FC” for the MNIST dataset, and “2\(\times\)(128CONV3)-MP2-2\(\times\)(256CONV3)-MP2-2\(\times\)(512CONV3)-MP2-1024FC” for the SVHN dataset, where CONV, MP and FC are the convolution layer, maxpool layer and fully connect layer, respectively. For the CIFAR10, we trained the VGG16 network \[30\]. We trained the networks using ADAM optimization algorithms with batch sizes of 100 for the MNIST, 1000 for SVHN and 750 for CIFAR10. Table 4 lists the test accuracy of MTJ-GXNOR compared to GXNOR and other state-of-the-art algorithms (ideal software implementations). For the MNIST and SVHN datasets our solution achieved accuracy similar to that of the state-of-the-art algorithms, implemented in software. For the CIFAR10, the MTJ-GXNOR reached accuracy comparable to that of GXNOR, but lower compared to the other algorithms. Notwithstanding, considering the application and the hardware performance improvement, some accuracy degradation might be acceptable.

Although the BNN \[7\] and BWN \[8\] frameworks achieve better results compared to the GXNOR BNN \[6\], they retain the full-precision weights during the training phase, which increases the frequency of memory accesses and requires support of full-precision arithmetic. Hence, their potential hardware implementation will be much less efficient than GXNOR. The MTJ-GXNOR TNN results are similar to the results of the GXNOR training, showing
Table 4: Accuracy of State-of-the-art Algorithms

| Methods            | Datasets       |
|--------------------|----------------|
|                   | MNIST          | SVHN | CIFAR10 |
| BNNs [3]          | 98.6%          | 97.20% | 89.85% |
| TWNs [31]         | 99.35%         | N.A  | 92.56% |
| BWNs [8]          | 98.82%         | 97.70% | 91.73% |
| BWNs [31]         | 99.05%         | N.A  | 90.18% |
| GXNOR TNN [6]     | 99.32%         | 94.12% | 83.51% |
| GXNOR BNN [6]     | 98.54%         | 91.68% | N.A   |
| MTJ-GXNOR TNN     | 98.61%         | 93.99% | 83.02% |
| MTJ-GXNOR Bin-Activation | 98.6% | 93.62% | –     |
| MTJ-GXNOR BNN Full | 97.84% | 89.46% | –     |

less than 1% accuracy degradation. Compared to GXNOR BNN, the MTJ-GXNOR BNN results led to less than 1% accuracy degradation for the MNIST dataset, but 2.4% degradation for the SVHN dataset. The test accuracy of the MTJ-GXNOR Bin-Activation, which used ternary weights and binary activations, is closer to that of GXNOR TNN.

5.4. Training Performance Sensitivity to Process Variation

Device variation and environmental changes may affect the performance of the proposed circuits, including their training performance. In this section, we evaluate the sensitivity of the TNN training performance to process variation.

5.4.1. Resistance Variation and $\theta$ Distribution Variation

Two cases of process variation were considered: (i) resistance variation and (ii) variation in the distribution of $\theta$. These variations may lead to a different switching probability for each MTJ device. To evaluate the sensitivity of the training to the device-to-device variation, we simulated the MNIST-architecture training with variations in the resistance and $\theta$ distributions. Several Gaussian variabilities were examined with different relative standard deviations (RSD), where the mean values are shown in Table 3. Table 5 lists the training accuracy for resistance variation and variation in $\theta$. Typically, resistance RSD is approximately 5% [11], while our simulations show that the training accuracy is robust to resistance variation even for higher RSD values (e.g., only 0.46% accuracy degradation for RSD= 30%).

The training accuracy is more sensitive to variations in $\theta$. Nevertheless, high standard deviation of $\theta$ values resulted in better test accuracy. To further evaluate the test accuracy dependency on $\theta$, we simulated training for different $\theta$ values. Table 6 lists the training results. Larger $\theta$ values, which correspond to higher switching probability, resulted in better test accuracy. Thus, we conclude that the performance of the MTJ-GXNOR algorithm improves for higher switching probabilities, which corresponds to larger $\theta$ values.

5.4.2. Sensitivity to Voltage Non-Ideality

Since the weight update probability is a function of the voltage drop across the MTJ device ($V_{up}$), it is sensitive to voltage source variation. Higher voltage leads to higher current. We tested training with $V_{up}$ in the range of [0.5V, 2.5V]. Our results show that the test accuracy improves when increasing $V_{up}$. The voltage magnitude can, therefore, be used to control the stochastic switching process and to improve the network training performance when using an MTJ device with low $\theta$ variance. In our setup, this effect is bounded and diminished when $V_{up}$ exceeded 1.1V and only marginally
Table 5: Test Accuracy vs. Process Variation for MNIST

| RSD Variation | Resistance Variation | $\theta_0$ Variation |
|---------------|----------------------|----------------------|
| 0%            | 98.61%               | 98.61%               |
| 1%            | 98.13%               | 97.98%               |
| 5%            | 98.13%               | 97.92%               |
| 10%           | 98.1%                | 97.98%               |
| 30%           | 98.15%               | 98.05%               |
| 35%           | 97.94%               | 98.05%               |

Table 6: Test Accuracy vs. $\theta_0$

| $\theta_0$[rad] | Test Accu. |
|-----------------|------------|
| 0.0913          | 94.28%     |
| 0.1141          | 94.98%     |
| 0.2739          | 97.39%     |
| 0.345           | 98.61%     |

improves the test accuracy; hence, in this work, we set $V_{up} = 1V$ to constrain the power consumption of our design.

5.4.3. Sensitivity to Temperature The MTJ dependency on temperature has several aspects. First, the switching behavior depends on the ambient temperature \(15\). For higher temperatures, the mean switching time \(\tau\) is shorter \(32\). Second, higher temperatures lower \(R_{off}\). The resistance of \(R_{on}\), however, has a much weaker temperature dependency and it is nearly constant \(33\). The transistors are also influenced by the temperature. For high temperatures, the current drivability of the MOS transistors is degraded since the electron mobility is lower. Hence, ambient temperature affects the switching probability by lowering \(R_{off}\) and degrading the CMOS current drivability. Furthermore, the initial magnetization angle, \(\theta\), depends on the temperature by the normal distribution \(\theta \sim N(0, \theta_0)\), where the standard deviation is \(\theta_0 = \sqrt{k_B T/(\mu_0 H_k M_s V)}\). Hence, \(\theta_0\) increases for higher temperatures.

As shown in Section 5.4.1 and Table 5, the training performance is influenced by the value of \(\theta\), when in this work we do not include the effect of the transistors. Thus, to evaluate the sensitivity of the MTJ-GXNOR training to ambient temperature, we focused on \(\theta_0\). We simulated MTJ-GXNOR training with different temperatures in the range \([260K, 373K]\), with the associated resistance based on \(32, 33\). Table 7 lists the test accuracy obtained for different temperatures. Although better accuracy was obtained for higher temperatures, the improvement was less than 1%. The minor variations in accuracy imply that the test accuracy is agnostic to the temperature. Figure 6 shows the test accuracy over the training phase for the MNIST network. Higher temperatures increased the convergence rate of the network, while the network converged to similar test accuracy for all the temperatures in the examined range.

5.5. Performance Evaluation

QNNs aim to reduce the computation and memory-capacity requirements of DNNs; therefore, in this section, we evaluate the potential performance benefits of our solution. The overall performance is highly dependent on the exact system structure and functionality. For example, our solution can be integrated into a fully analog or digital architecture and
Figure 6: Test accuracy during the training phase for temperature range [273K, 373K]. Increasing the temperature leads to higher θ₀ variance, thereby increasing the randomness of the MTJ switching time. Therefore, higher temperature leads to faster convergence.

Table 8: Area and Power

| Cell                  | Area        | Power XNOR+Sum | Power Update |
|-----------------------|-------------|----------------|--------------|
| Single synapse        | 3.63µm²     | 1.89µW         | 2.72µW       |
| 64 × 64 Syn. array    | 0.015mm²    | 7.31mW         | 1.64mW       |
| 128 × 128 Syn. array  | 0.059mm²    | 28.5mW         | 3.25mW       |

can support different general optimization algorithms, including SGD, as in GXNOR [6]. Each configuration will produce different performance and should be compared to a similar configuration. First, we evaluate the performance of our circuit when it is not connected to the peripheral circuit. Then, we consider a simple test system to evaluate the potential of our solution with its associated peripheral circuits and supporting units.

5.5.1. TNN Power and Area The power consumption and area were evaluated for a single synapse and different synapse arrays simulated in Cadence Virtuoso, including the interconnect parasitic. The results are given in Table 8. During the read operation, all the synapses are read in parallel; therefore, the feedforward power is higher than the write power, when each column is updated separately.

5.5.2. System Performance (Test Case) To evaluate the performance of the synapse array when integrating our design in a full system, we consider the following setup, illustrated in Figure 7:

(i) The synapse array stores the ternary weights. The array can perform the GXNOR, backpropagation, and GXNOR operation, as described in Section 4.

(ii) A 127 × 127 synapse array. This size is broadly accepted as mitigating the parasitic effects on the circuit performance that is limited by the ADC resolution [17, 3, 34]. Since the size of a single DNN layer is larger than the array size, the layer will be divided between different arrays and the partial results are accumulated. To support a
Figure 7: System configuration – test case. A $127 \times 127$ synapse array is connected to the peripheral circuits through the row and column interfaces. The FF, BP, and UP control signals configure the interfaces to support the feedforward, backpropagation, and weight update, respectively. $\kappa$ and $\nu$ are inputs to the array. The IsZero signal indicates if $\kappa$ is zero.

multi-array per layer, the binary activation is done after accumulating the results from the array. Thus, this system requires conversion of the partial results ($I_{out}$), from each array, to digital using analog-to-digital converters (ADC).

(iii) For the feedforward, 1-bit DACs are used to support the inputs per column, and 8-bit ADCs are used to convert the row current to digital outputs. For a $127 \times 127$ array, the output of each row is an integer value in the range $[-127, 127]$; thus an 8-bit ADC is sufficient. Furthermore, due to the high energy consumption of the ADC, we use only eight ADCs, which are shared among the 127 output rows [17]. Accordingly, the overall latency to produce 127 sum results is 8ns.

(iv) For the backpropagation, we consider the bit-streaming method with 8-bit precision as suggested in [17]; thus, we used a 1-bit DAC in the row interface and an 8-bit ADC in the column outputs.

(v) To generate the control signals, an 8-bit DAC, and voltage comparators are needed. To generate the sawtooth signal, we use the circuit from [22].

(vi) The system supports an in-situ SGD algorithm. Therefore, no additional circuit is needed to compute the update values. The columns are updated sequentially.

Table 9 lists the power of the additional peripheral circuits. The energy efficiency of each stage for this setup is listed and compared to previews works in Table 10. The power consumption of the data converters significantly limits the overall performance.

6. Comparison to Previous Work

Most previous work on in-situ hardware implementations of BNN and TNN only support inference. In [37], a CMOS-based computation-near-memory engine was designed and fabricated. The design's energy efficiency during inference is $532 \, \text{TOPs/W}$. The authors assumed that the binary activation can be done immediately after the convolution, thereby eliminating
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Table 9: Test Case Model

| Component               | Number | Power [mW] |
|-------------------------|--------|------------|
| ADC 8-bit               | 17     | 16         |
| DAC 8-bit               | 35     | 5.47       |
| DAC 1-bit               | 17     | 0.5        |
| Voltage Comparator     | 36     | 127        |
|                         |        | 0.455      |

Table 10: Energy Efficiency of the Synaptic Array.

| Paper                  | Tech. | FF   | BP   | WU       | Delay     | Power     | Area     | Comment                              |
|------------------------|-------|------|------|----------|-----------|-----------|----------|---------------------------------------|
| This paper             | MTJ   | $18.3 \frac{TOPs}{W}$ | $1.43 \frac{TOPs}{W}$ | $3 \frac{TOPs}{W}$ | 100ns/8.25ns | 178mW / 9.73mW | 0.068mm$^2$ | –                                    |
| w/o data converters    | MTJ   | $334 \frac{TOPs}{W}$  | Not evaluated          | $12.4 \frac{TOPs}{W}$ | 2ns/2ns     | 22.3mW/2.18mW | Not evaluated | Binary weights, FP activations. Original evaluation does not include data converters. |
| w data converters      | MTJ   | $0.29 \frac{TOPs}{W}$ | Not evaluated         | $0.14 \frac{TOPs}{W}$ | 108ns/16.5ns | 177mW/27.3mW | Not evaluated | Evaluation based on Table 9           |
| RRAM                   | –     | –    | –    | –        | –         | 0.25mW/–    | 0.0012mm$^2$ | Support Inference of BNN              |
| CMOS                   | –     | –    | –    | –        | –         | –         | –        | Support Inference of BNN Assuming no use of data converters. |

FF, BP, WU are acronyms for feedforward, backpropagation, and weight update, respectively. The delay and power cells format stand for $<\text{read value}>/<\text{write value}>$.

the ADC. A similar assumption for our setup will increase the inference energy efficiency of our design to $180\frac{TOPs}{W}$. Supporting training in such an accelerator will include additional arithmetic units and will also lead to frequent accesses to the memory to fetch the next layer and will require larger memory capacity to store the intermediate results. BNN inference without the need for an ADC is also supported in [34], where energy efficiency of $1326\frac{TOPs}{W}$ was reported. In that work, an RRAM device was used instead of an MTJ. The RRAM-based synapse can use smaller access transistors than the MTJ-based device, which is current-driven. Moreover, a 1T1R synapse is sufficient when supporting only inference, thereby reducing the complexity and overall power consumption of each synapse. [38] simulated MTJ-based memory, which supports digital XNOR and XOR operations. By modifying the array drivers, they performed XNOR or XOR operation between operands given to the write driver. The result is written into the memory cell and read by the sense amplifier. Thus, this solution requires three stages to perform the XNOR or XOR operation: preset, XNOR (write), and read, and can perform the operation on a single row each time. They used the MTJ only as a memory cell and did not exploit its stochastic behavior.

Other works exploit the stochastic behavior of the MTJ device. [39] exploits the MTJ stochastic switching to design a stochastic neuron. In their work, the training is done off-line, and the weights can be stored in any memristive technology, while the neuron circuit includes an MTJ device. In [40], a STT-MTJ-based synapse is used to support BNN training. This solution works in the low current regime; thus, the MTJ switching follows an exponential distribution. Although such distribution is mathematically suitable to train QNNs, our simulations showed that working in the low current regime requires long update periods (approximately ms). Our approach is to train in the high current regime, so the stochastic update will occur in a realistic time period. In [12], 1T1R and 1R structures were proposed, and the stochastic behavior of the MTJ was leveraged to support in-situ training of DNNs with binary weights and full-precision activation. Two update operations are required for the
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1T1R and four for the 1R, whereas our synapse can perform positive and negative operations in parallel, thus requiring only one update operation. Moreover, a high-resolution DAC is necessary to convert the full-precision input value to voltages. Using the DAC circuits listed in Table 9, the 8-bit DAC consumes 5× more energy than the 1-bit DAC. The power consumption and complexity of their synapse array are, therefore, greater than those of our MTJ-GXNOR.

Numerous works, which include MTJ-based synapse, focused on the Spike Timing Dependent Plasticity (STDP) learning rule used in bio-inspired ANNs [11, 18]. Nevertheless, common DNNs are trained with gradient-based optimization [13]. Our work focuses on how the MTJ stochastic behavior can be used to train TNNs and BNNs with a stochastic gradient-based update rule.

7. Conclusions

In this paper, we demonstrated the potential of MTJ-based synapse to support in-situ TNN and BNN stochastic training, without sacrificing accuracy. The proposed circuit enables highly parallel and low power execution of weight-related computation. We demonstrated its great potential to achieve high energy efficiency in different DNN systems. To fulfill the potential of the MTJ-based synapse, the next step is to integrate it into a full system design.

The stochastic behavior of the MTJ can support different training algorithms. For example, while in this work we used MTJ stochastic switching to quantize the gradients, it can be used in algorithms that use stochastic quantization of the weights and activations. Moreover, other optimization algorithms, such as simulated annealing, might benefit from these properties. The high energy efficiency and the flexibility in functionality enable different algorithms and systems that can accelerate QNN inference and training on low-power devices such as IoT and consumer devices.

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