Supplemental information

Second-order associative memory circuit hardware implemented by the evolution from battery-like capacitance to resistive switching memory

Guangdong Zhou, Xiaoyue Ji, Jie Li, Feichi Zhou, Zhekang Dong, Bingtao Yan, Bai Sun, Wenhua Wang, Xiaofang Hu, Qunliang Song, Lidan Wang, and Shukai Duan
## Supplemental Table

**Table S1 Memristor circuit model.** Related to Figure 5 and Figure 6. Sub-Circuit Description of the Memristor Model.

| Description of the Memristor Model. |
|--------------------------------------|

* Memristor model  
**Connection**  
**Plus-top electrode**  
**Minus-bottom electrode**  
**XSV-External connection to plot state variable that is not used otherwise**  

.SUBCKT Memristor model Plus Minus XSV PARAMS:  
+Alpha1=1 Alpha2=1 Beta1=0.729 Beta2=0.224 Beta3=1 Beta4=0.525 a1=2.329e-2 a2=4.614e-3 a3=4.013e-2 a4=0.035  
b1=1.3e-6 b2=0.16e-4 n1=0.091 n2=60.074 n3=0.760 n4=3.218e-3 m1=0.527e-2 m2=1.074e-2 aon= aoff=0.5757 wc=0.14  

**********Functiondx/dt=F(x(t),v(t))**********  
.func foff(x,aoff,wc)={exp(-exp((x-aoff)/wc))}  
.func fon(x,aon,wc)={exp(-exp((aon-x)/wc))}  

Alpha1,Alpha2,Beta1,Beta2,Beta3,Beta4={if(v>=0,Alpha1*(exp(Beta1*v)-exp(-Beta2*v)),Alpha2*(exp(Beta3*v)-exp(-Beta4*v))*fon(x,aon,wc))}  

********IV Response – Hyperbolic sine due to MIN structure**********  
.func f1(x,v,a1,a2,b1,n1,n2,m1)={a1*x^n1*v^b1+a2*(1-x^n2)*(1-exp(-m1*v))}  
.func f2(x,v,a3,a4,b2,n3,n4,m2)={a3*x^n3*v^b2+a4*(1-x^n4)*(1-exp(-m2*v))}  

.IVRel(x,v,a1,a2,a3,a4,b1,b2,n1,n2,n3,n4,m1,m2)={if(v>=0,f1(x,v,a1,a2,b1,n1,n2,m1),+f2(x,v,a3,a4,b2,n3,n4,m2))}  
Gm Plus Minus value={IVRel(V(x),V(Plus,Minus),a1,a2,a3,a4,b1,b2,n1,n2,n3,n4,m1,m2)}  

**********Circuit to determine state variable**********  
Gx 0 x value={F(V(x),V(Plus,Minus),aon,aoff,wc,Alpha,Beta,Gama)}  
Cx x 0 1 IC={x0}  
Raux x 0 1T  

.ENDS Memristor model