CHARTER: Identifying the Most-Critical Gate Operations in Quantum Circuits via Amplified Gate Reversibility

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Abstract—When quantum programs are executed on noisy intermediate-scale quantum (NISQ) computers, they experience hardware noise; consequently, the program outputs are often erroneous. To mitigate the adverse effects of hardware noise, it is necessary to understand the effect of hardware noise on the program output and more fundamentally, understand the impact of hardware noise on specific regions within a quantum program. Identifying and optimizing regions that are more noise-sensitive is the key to expanding the capabilities of NISQ computers.

Toward achieving that goal, we propose CHARTER, a novel technique to pinpoint specific gates and regions within a quantum program that are the most affected by the hardware noise and that have the highest impact on the program output. Using CHARTER’s methodology, programmers can obtain a precise understanding of how different components of their code affect the output and optimize those components without the need for non-scalable quantum simulation on classical computers.

Index Terms—Quantum Computing, NISQ Computing, Quantum Error Detection, Quantum Error Mitigation

I. INTRODUCTION TO CHARTER

The field of quantum computing, which has applications in many areas, such as high-performance computing (HPC), has seen considerable advancement recently. While the hardware has been increasing in size, individual qubits still remain quite noisy. These noise effects include errors that are generated due to qubit state decoherence, qubit state preparation and measurement, gate operation, and cross-talk among neighboring qubits [38], [42]. Due to these noise effects, when a quantum program is executed on these noisy intermediate-scale quantum (NISQ) computers, the program output experiences a considerable error [8], [29], [38], [42], [58].

As practical hardware error correction has not been widely implemented on NISQ computers in a cost-effective manner [23], [47], [52], [54], recent software efforts have attempted to reduce the output error using software-level compiler optimizations [6], [13], [26], [49]. These software efforts rely on relatively simple noise models—in particular, individual-qubit noise data generated during qubit calibration [39], [51]—to obtain the decoherence times and error rates of gate operations on individual qubits. This data is then used to perform just-in-time compilation to best map the logical quantum program to the physical quantum computer in a manner that reduces the number of gate operations and potentially reduces the overall error in the output of the program [34], [37], [39], [51], [57].

However, due to the difficult-to-model complex interactions of the different noise characteristics, how different quantum program components contribute to the overall output error of a quantum program can vary from program to program and program region to program region [8], [29], [38], [58]. Fig. 1 shows the error impact of a two-qubit gate being run on the same pair of physical qubits at five different times during the program execution. These results show that the magnitude of impact on the program output of the same gate is quite different depending on its position in the program (i.e., the TVD changes depending on the location of the erroneous two-qubit gate operation). The fundamental reason behind our observation is that the crosstalk and interference from gates being applied to neighboring qubits affects a particular gate operation’s impact on the error in the program output. Unfortunately, quantifying, characterizing and modeling this complex effect is challenging, and currently, the HPC quantum systems community does not have the appropriate methodology and tools to determine how the specific components/regions of a quantum program contribute to its output error. Novel methods and tools in this domain will enable further program-
specific compiler optimizations and debugging support.

**CHARTER:** In order to address the above challenges, this paper proposes CHARTER, a simple yet effective method to compute how specific gates within a program contribute to its overall output error. CHARTER enables the programmer to pinpoint specific gate operations and regions within a quantum program that are the most affected by the hardware noise and that have the highest impact on the output error of the program. The spirit of this effort is similar to development of program vulnerability factor (PVF) and architecture vulnerability factor (AVF) for classical computing systems [33], [46] – however, developing similar closed-form models for highly accurate vulnerability assessment for quantum circuits is not possible.

The key insight behind CHARTER is to leverage the reversibility property of quantum computing to understand the impact of individual quantum gate operations on the observed error in the program output. CHARTER is the first method to leverage the quantum circuit reversal to identify and quantify the criticality of individual quantum gate operations on the program output error (Sec. IV). CHARTER demonstrates how to systematically reveal the impact of individual quantum gate operations without the need to perform quantum simulation on classical computers, which is not scalable to large programs [11], [21], [22], [24]. CHARTER breaks this barrier and demonstrates how quantum programmers can identify the most critical operations on erroneous NISQ hardware without relying on expensive simulation of quantum programs. Using CHARTER’s methodology, programmers can identify particularly problematic program regions and focus their debugging and optimization efforts on those areas.

A prior technique, QRAFT [40], demonstrated the use of the quantum circuit reversibility toward improving the answer fidelity of quantum programs on the NISQ computers (i.e., circuit reversal as a noise-mitigation technique). This work, CHARTER, demonstrates another unique and useful application of quantum circuit reversibility – estimating the high-impact quantum circuit components. QRAFT reverses the full quantum circuit to mitigate the noise and estimate correct program output [40]. Unlike, QRAFT, CHARTER considers the quantum circuit as a series of smaller circuit gate operations, and applies quantum circuit reversal at the gate-level. CHARTER demonstrates the significance of applying circuit reversals multiple times for a given circuit gate and across multiple circuit gates – which is necessary to identify the high-impact program components.

The contributions of this work are as follows:

- The proposed technique, CHARTER, is a simple and effective way to determine high-error-impact gate operations and regions in any given quantum program using quantum reversibility property. It gives programmers a scalable utility to perform optimizations that are specific to their program structure, as opposed to relying on simplistic assumptions and noise models.
- CHARTER is evaluated using multiple quantum programs of varying characteristics and sizes. These results have revealed some surprising, interesting, and useful trends:
  - While most existing works have primarily focused on ranking the criticality of qubits based on their error rates [34], [37], [39], [51], [57], CHARTER demonstrates that prior approaches alone are not always sufficient and complete. Type and location of gate operations are equally critical. Across different algorithms, the top 25% high-impact gates are located on almost all qubits used to run the program, which indicates that criticality of gates varies more based on the gate’s position in the circuit.
  - Prior techniques have largely focused on specifically reducing two-qubit gates [3], [41], [45], [55], [64], as they generally have a high error in isolation. Interestingly, CHARTER reveals that, in some cases, one-qubit gates can have worse impacts on the output error.
  - CHARTER demonstrates that the error impact of specific gates can vary depending on the input to the program. For example, input \( i \) can increase the error impact of gates in a certain region of a quantum program, while input \( j \) can affect a different region. This observation opens up the opportunity for input-aware quantum compilation.
  - We provide a technique to identify the program input with the highest impact on the output error by extending CHARTER to multi-gate reversals. Based on this identification, we propose the use of selective serialization of high-impact gates to reduce the effect of crosstalk, which reduces output error by up to 7% points.
  - CHARTER shows that the gates near the end of the program do not always have the worst impact, although some existing techniques optimize those regions due to the assumed impact of qubit state decoherence [27], [44], which increases as program length increases [31], [53].
- CHARTER’s code to apply reversals and use them for characterization, and its evaluation datasets are open-sourced at https://doi.org/10.5281/zenodo.6875324.
TABLE I: Different types of noise effects that NISQ computers experience when running a quantum circuit.

| Noise Type                     | Description                                                                 |
|--------------------------------|-----------------------------------------------------------------------------|
| Operation Errors               | Errors caused by inaccuracies in applying a specific desired quantum gate.   |
| [14], [43]                     |                                                                             |
| State Preparation and          | Errors caused when initializing and preparing the qubit state and measuring the final state after execution. |
| Measurement Errors             |                                                                             |
| [50]                           |                                                                             |
| Decoherence Effects            | Errors caused due to the prepared qubit superposition state decaying over time to the ground (i.e., \( |0\) ) state. |
| [31], [53]                     |                                                                             |
| Crosstalk Effects              | Errors caused to a qubit due to interference effects from neighboring qubits. |
| [35], [59], [60]               |                                                                             |

II. RELEVANT BACKGROUND FOR CHARTER

Quantum States, Gates, and Circuits. The computational state of a qubit can be represented using a superposition of the \( |0\) and \( |1\) basis states: \( |ψ⟩ = α_1 |0⟩ + α_2 |1⟩ \). Here, \( |ψ⟩ \) is the superposed state of the qubit and \( α_1 \) and \( α_2 \) are complex coefficients such that \( |α_1|^2 + |α_2|^2 = 1 \). Similarly, the superposed and entangled state of an \( n \)-qubit quantum system can be represented as: \( |ψ⟩ = \sum_{k=0}^{2^n-1} α_k |k⟩ \) such that \( \sum_{k=0}^{2^n-1} ||α_k||^2 = 1 \). When the qubit state is measured, the state superposition collapses and it can be found in one of the \( 2^n \) states, with the probability of finding it in state \( k \) being \( ||α_k||^2 \).

Qubits are prepared by applying quantum gates or operations. Quantum gates are unitary operations that evolve the state of the qubit from one state to another. For example, the \( X \) quantum gate flips the state of the qubit from \( |0⟩ \) to \( |1⟩ \) and from \( |1⟩ \) to \( |0⟩ \). A set of universal quantum basis gates can be used to represent all quantum gates. The specific choice of basis gates depends on the hardware. For example, the IBM quantum computing hardware, which is used to evaluate CHARTER, uses the \( R_Z, S_X, X, \) and \( C_X \) gates to form the universal basis set. As Fig. 2(a) shows, \( R_Z, S_X, X, \) and \( X \) are one-qubit gates, and \( C_X \) is a two-qubit gate. The \( X \) gate is the qubit-flip gate, the \( S_X \) gate performs the square root operation of the \( X \) gate, and the \( R_Z \) gate is a virtual gate that changes the frame of reference of the quantum system (it is not performed on the physical hardware). The two-qubit entangling \( C_X \) gate performs the \( X \) operation on the “target” qubit depending on the state of the “control” qubit as shown in Fig. 2(a).

When these quantum gates are performed in succession of one another on an \( n \)-qubit system they form a quantum program, also known as a quantum circuit. While a quantum program can be written using any high-level quantum logic gates, the program then has to be mapped to the hardware-compatible physical basis gate set in order to execute the circuit on a quantum computer. Fig. 2(b) shows an example three-qubit quantum circuit with nine operations. Once all the operations are executed, the measurement operator is applied to all the qubits to generate the output state.

Hardware Noise Effects. A NISQ computer experiences a variety of noise effects when a quantum program is initialized, executed, and measured. These noise effects have been summarized in Table I. These noise effects are challenging to model, especially the impact of their combined expression is difficult to simulate or predict [8], [14], [42]. When a quantum circuit is run, these individual noise effects compound and accumulate to cause error in the output of the program.

Quantum Output and Output Error. The output of a quantum program is obtained as a probability distribution over its output states. The same quantum state is prepared and measured multiple times (each measurement producing one output state), which then generates the probability distribution over the output states. However, because of the hardware noise effects, this observed output distribution can be quite different from the ideal or correct output distribution. A typical metric that is used to measure the deviation of the observed output distribution from the ideal output distribution is the Total Variation Distance or TVD [16]. As shown in Fig. 3(a), the TVD between two probability distributions is calculated by summing up the absolute differences in the probabilities of the individual states and dividing by two. With a value between 0 and 1, the closer the TVD is to 0, the more the two probability distributions are similar. We will use this metric going forward to compare two probability distributions.

Quantum Reversibility Property. Unlike classical gates, all quantum gates are reversible. The input state can be obtained by applying the inverse of the original gate to the output state. Because all quantum gates can be represented using unitary matrices \( U \), their inverse is simply the complex conjugate transpose (also known as the Hermitian adjoint) of \( U \), which can be represented as \( U^\dagger \). Therefore, for any initial state \( |ψ⟩ \), if \( U \) is applied to it, the initial state can be recovered by applying \( U^\dagger (|ψ⟩ = U^\dagger U |ψ⟩) \). In this paper, we represent the inverse of a quantum operation using a dashed line as shown in Fig. 3(b). QRAFT has leveraged this property for improving the answer fidelity of quantum programs on NISQ machines [40]. CHARTER leverages this quantum reversibility property to identify high-impact circuit components.
TABLE II: Algorithms and benchmarks used for the design, evaluation, and analysis of CHARTER.

| Algorithm   | Description                                                                 |
|-------------|-----------------------------------------------------------------------------|
| HLFI        | Hidden Linear Function [7]                                                  |
| QFT         | Quantum Fourier Transform [56]                                              |
| QAOA        | Quantum Alternating Operator Ansatz [15]                                    |
| VQE         | Variational Quantum Eigensolver [32]                                        |
| Adder       | Quantum Adder Program [12]                                                  |
| Multiplier  | Quantum Multiplier Program [17]                                             |
| Heisenberg  | Time-independent Heisenberg Hamiltonian [4]                                 |
| TFIM        | Transverse Field Ising Model [4]                                            |
| XY          | XY Quantum Heisenberg Model [4]                                             |

III. CHARTER’S METHODOLOGY FOR EXPERIMENTS

Before we describe the design of CHARTER, we first discuss the methodology to construct and execute the experiments used for the design, evaluation, and analysis of CHARTER.

Experimental Setup. We use the IBM quantum cloud platform [10] to execute the experiments to evaluate CHARTER. We use the corresponding Python-based (Python version 3.9.7) Qiskit programming language [1] (Qiskit version 0.17.4) to program the quantum algorithms and benchmarks and apply reversals for CHARTER. We run the experiments on the 7-qubit ibm_lagos quantum computer and the 16-qubit ibmq_guadalupe quantum computer (computer qubit layouts shown in Fig. 4), depending on the size of the algorithm being executed; algorithms of size seven qubits or less are run on ibm_lagos and the rest are run on ibmq_guadalupe. The quantum volume of both computers is 32; this metric measures the performance of gate-model quantum computers in terms of the size (width and depth) of the circuits they can run. Each experiment is run with 32,000 trials to generate the output probability. We use Qiskit’s StateVector simulator to run simulations of the quantum programs on classical computers to get the ideal output of the programs. Note that this output is only used to validate the effectiveness of CHARTER and is not a part of the CHARTER technique. In fact, CHARTER is specifically designed to not rely on classical simulations in order to ensure scalability to large quantum algorithms. Python’s SciPy package [20] is used to calculate statistical metrics such as correlation for the design and analysis of CHARTER.

Quantum Algorithms and Benchmarks. CHARTER uses algorithms and benchmarks listed in Table II, which have a variety of sizes (3-16 qubits) and use cases for high-performance computing. HLFI is a search algorithm, while QFT is the quantum version of the Fourier transform. QAOA and VQE are quantum variational algorithms, and Adder and Multiplier are standard quantum arithmetic circuits. Heisenberg, TFIM, and XY are time-evolution Hamiltonian programs for material simulations. The TFIM model has non-zero coupling interaction between nearest neighbor spins along the z axis, XY has for x and y axes, and Heisenberg has for all three axes. All algorithms are mapped to the physical quantum hardware using all of the compiler optimizations available via Qiskit, including noise-aware logical-to-physical mapping, gate routing and SWAP insertion depending on hardware connectivity, gate cancellation based on commutativity and combination, gate deletion by detecting redundany, and gate re-synthesis for two-qubit unitary blocks (peep-hole optimization) [1]. All algorithms are converted to the \( \{ \text{CX, Rz, SX, X} \} \) basis gate set (Fig. 2) during the mapping process to run on the IBM hardware. Once CHARTER’s techniques are applied to the circuit, the compiler optimization level is set to 0 to ensure that the techniques are not optimized out, because CHARTER is applied to pre-mapped circuit and no additional compilation steps necessary.

Metrics. We use the TVD (described in the previous section: Sec. II) to measure the difference between two probability distributions. To measure the correlation relationship between two random variables, we use the Pearson correlation [5], which is the square-root of the coefficient of linear regression \( (R^2) \). A value of 1 indicates a perfect positive linear correlation, \(-1\) indicates a perfect negative linear correlation, and 0 indicates no correlation. We also show the p-value to show the significance of the correlation (a p-value < 0.01 indicates a statistically strong correlation).

IV. CHARTER: DESIGN AND TECHNIQUE

The core of CHARTER’s design is grounded in the reversibility principle of quantum computing. CHARTER leverages this property by applying a pair consisting of the “reversed” gate and the “original” gate to each of the gates in the quantum circuit (referred to as the “reversed pair”). Fig. 5 shows how this pair is applied to different operations: (a) the first SX gate on qubit 0 and (b) the first CX gate on qubits 1 and 2. This is done for each of the gates in the circuit. The original circuit has nine gates; therefore, a total of nine “reversed circuits” are generated, each with one reversed pair of gates corresponding to one of the gates in the original circuit. In general, \( g \) reversed circuit are generated for a circuit with \( g \) gates.

CHARTER employs this method for two useful reasons. First, applying the pair of the reversed gate + the original gate to a gate \( U \) does not alter the ground truth output of the circuit (on an ideal quantum computer). This is because of the
TABLE III: Pearson correlation between the TVD of the output of the $r$-reversals runs with the output of the original run for different number of reversals ($r$). The number in brackets next to the algorithm name shows the number of qubits. The highest correlation is seen with five reversals.

| Algorithm | One Reversal Correlation | Three Reversals Correlation | Five Reversals Correlation | Seven Reversals Correlation |
|-----------|--------------------------|-----------------------------|----------------------------|----------------------------|
|           | $p$-value | $p$-value | $p$-value | $p$-value | $p$-value | $p$-value |
| HLF (5)   | 0.02 | 0.91 | 0.08 | 0.58 | 0.40 | 6.85e−3 | 0.17 | 0.26 |
| HLF (10)  | 0.11 | 0.06 | 0.18 | 0.12 | 0.49 | 3.04e−3 | 0.13 | 0.62 |
| QFT (3)   | 0.43 | 3.69e−3 | 0.96 | 3.76e−24 | 0.99 | 2.18e−35 | 0.99 | 2.95e−40 |
| QFT (7)   | 0.61 | 3.16e−31 | 0.61 | 9.21e−31 | 0.64 | 3.32e−34 | 0.63 | 2.31e−34 |
| Adder (4) | 0.52 | 3.29e−7 | 0.94 | 9.57e−41 | 0.98 | 3.97e−61 | 0.99 | 5.40e−68 |
| Adder (9) | 0.43 | 5.12e−56 | 0.89 | 5.89e−23 | 0.94 | 4.12e−43 | 0.95 | 2.31e−30 |
| Multiply (5) | 0.76 | 2.98e−17 | 0.96 | 1.32e−48 | 0.99 | 1.04e−67 | 0.99 | 7.85e−75 |
| Multiply (10) | 0.89 | 7.35e−221 | 0.89 | 1.45e−219 | 0.89 | 3.16e−220 | 0.88 | 7.20e−217 |
| QAOA (5)  | 0.82 | 4.34e−35 | 0.70 | 1.13e−21 | 0.79 | 6.02e−31 | 0.80 | 1.80e−31 |
| QAOA (10) | 0.38 | 6.65e−15 | 0.35 | 4.21e−13 | 0.38 | 2.46e−10 | 0.30 | 1.11e−9 |
| VQE (4)   | 0.51 | 1.69e−29 | 0.38 | 4.11e−16 | 0.21 | 9.97e−6 | 0.19 | 6.85e−5 |
| Heisenberg (4) | 0.69 | 2.28e−28 | 0.74 | 2.27e−29 | 0.90 | 4.75e−36 | 0.91 | 4.50e−47 |
| TFIM (4)  | 0.70 | 1.06e−18 | 0.78 | 1.61e−25 | 0.88 | 4.70e−38 | 0.92 | 1.50e−49 |
| TFIM (8)  | 0.38 | 1.37e−20 | 0.53 | 7.67e−16 | 0.71 | 7.05e−14 | 0.60 | 1.07e−12 |
| TFIM (16) | 0.42 | 2.73e−19 | 0.55 | 4.09e−18 | 0.72 | 8.14e−16 | 0.59 | 2.61e−13 |
| XY (4)    | 0.49 | 6.50e−7 | 0.84 | 1.54e−26 | 0.91 | 2.13e−36 | 0.92 | 6.70e−39 |
| XY (8)    | 0.67 | 0.11 | 0.76 | 3.87e−4 | 0.80 | 9.87e−6 | 0.89 | 5.44e−11 |

reversible principle of unitary matrices: $U(U^\dagger U) = U1 = U$. Therefore, applying this pair does not alter the mathematical functionality of the quantum program, and does not affect the output of the program. (2) However, due to the introduction of additional two operations within the reversed pair, this will impact the output error of the circuit when it is run on a real noisy quantum computer. This impact on the output error will be the amplified, but it will be proportional to the impact of the original gate. This is because the two gates in the reversed pair are operationally similar to the original gate, meaning they will experience the same operation errors. Moreover, the two gates in the reversed pair are also applied at the same location of the original gate, which means that they will also experience the same decoherence effects. Thus, the output of the original circuit (i.e., the circuit with no reversals) and the output of the circuit with the reversed pair can be compared to gauge the impact of the gate in question.

These outputs are compared in the following manner. Let $O_{\text{orig}}$ be the output of the original circuit. $O_{\text{orig}}$ is a probability distribution with probabilities $p^k_{\text{orig}}$ for each of the $k^{th}$ state in the $2^n$ states, where $n$ is the number of qubits. Similarly, let $O_{\text{rev}}$ be the output of the reversed circuit for a particular gate with $p^k_{\text{rev}}$ probabilities for each of the $2^n$ states. The difference in these outputs can then be calculated using the total variation distance: $\text{TVD}(O_{\text{orig}}, O_{\text{rev}}) = \frac{1}{2} \sum_{k=0}^{2^n-1} |p^k_{\text{orig}} - p^k_{\text{rev}}|$. Using this TVD, CHARTER can estimate the impact that a particular gate has on the output of a circuit. Note that this TVD is calculated between the noisy outputs of the original circuit and the reversed circuit. It does not rely on the output of an ideal quantum simulation, which is not scalable as it has to be executed on classical computers [11], [21], [22], [24]. Instead, CHARTER relies on noisy outputs of real-computer runs. To get the error impact of all the gates, the TVD can be calculated between the output of the original circuit and the reversed circuits corresponding to all the gates. Going forward, we refer to gates whose circuits have high TVD with the original circuit as “high-impact” gates as these are the ones of particular importance.

As a note, the TVD measures the relative error between the two output probability distributions. As a result, the absolute rates of errors unrelated to gate operations, including state preparation and measurement errors, remain the same for both of the circuits and therefore, do not affect CHARTER’s results. Note also that this methodology of CHARTER is not affected by intermediate measurements and resets. For example, to gauge the impact of a particular gate before an intermediate measurement, one can apply reversals before the measurement. A gate can similarly be reversed after the intermediate measurement and its impact will be observed in the succeeding measurement.
TABLE IV: The number and percentage of RZ and CX gates in different algorithms and their corresponding depths. The percentage of RZ gates in a circuit is high across algorithms.

| Algorithm  | Num. RZs | % RZs | Num. CXs | % CXs | Depth |
|------------|----------|-------|----------|-------|-------|
| HLF (5)    | 14       | 41%   | 10       | 29%   | 31    |
| HLF (10)   | 62       | 22%   | 171      | 61%   | 79    |
| QFT (3)    | 18       | 42%   | 9        | 21%   | 28    |
| QFT (7)    | 121      | 12%   | 88       | 30%   | 141   |
| Adder (4)  | 35       | 41%   | 24       | 28%   | 61    |
| Adder (9)  | 99       | 28%   | 212      | 60%   | 209   |
| Multiply (5) | 32    | 37%   | 29       | 34%   | 58    |
| Multiply (10) | 206  | 31%   | 332      | 51%   | 321   |
| QAOA (5)  | 51       | 37%   | 55       | 40%   | 84    |
| QAOA (10) | 107      | 26%   | 222      | 53%   | 173   |
| VQE (4)   | 172      | 40%   | 132      | 31%   | 264   |
| Heisenberg (4) | 171 | 33%   | 201      | 39%   | 338   |
| TFIM (4)  | 48       | 41%   | 33       | 28%   | 62    |
| TFIM (8)  | 223      | 41%   | 137      | 25%   | 168   |
| TFIM (16) | 1032     | 36%   | 1000     | 35%   | 499   |
| XY (4)    | 35       | 37%   | 31       | 33%   | 64    |
| XY (8)    | 178      | 36%   | 149      | 30%   | 183   |

Next, we look at why identifying high-impact gates in noisy environments is a challenge and how CHARTER mitigates it.

A. CHARTER: Multiple Reversals for Noise Mitigation

While designing CHARTER, we discovered that although the idea of gate-specific reversed circuits is intuitive and promising, it is often not as effective as expected in practice. This is because, due to the high noise levels on NISQ computers, applying one pair of reversals does not help us effectively identify the differences between the outputs of the two circuits with high statistical confidence—the TVD between the original circuit and the reversed circuit may be close to zero in some cases. This is especially true for large circuits with many qubits and gates as there is a large enough accumulated impact from other gates, so as to obscure the impact of one particular gate. To overcome this challenge, CHARTER designs a novel multiple-reversal technique. CHARTER applies the reversed pair multiple times in succession of one another. Fig. 5(c) shows how “two reversals” can be applied to the first SX gate on qubit 0. We note that CHARTER’s design does not require any additional effort in terms of calculating more reversals or running more circuits. In fact, only one reversed circuit still needs to be run per gate. However, the reversed circuit now contains multiple reversals in order to amplify the error impact of a particular gate on the output of large high-noise circuits.

However, the questions is: are multiple reversals effective and can we determine the number of reversals that are the most effective? We answer this question with experimental evidence. We compare the success of identifying the impact of gates for different reversals across the different algorithms and benchmarks. The success is measured by calculating the Pearson correlation between the TVD obtained by comparing the output of the original circuit and the reversed circuit (the metric we saw above: $TVD(O_{orig},O_{rev})$) and the TVD obtained by comparing the ideal output with the output of the reversed circuit ($TVD(O_{orig},O_{ideal})$). Because getting $O_{ideal}$ requires simulation, it is not practical to calculate as a part of CHARTER’s technique. However, here we use it to validate the success of the technique. If $TVD(O_{ideal},O_{rev})$ is correlated with $TVD(O_{orig},O_{rev})$ across all gates in a circuit, it means that both metrics produce the same relative impact scores for all the gates. This in turn implies that $O_{orig}$ can be used as a scalable alternative to $O_{ideal}$. So we calculate this correlation for different number of reversals and identify the number for which the correlation is the highest.

Table III shows the results of these correlations across all the algorithms and benchmarks used for evaluating CHARTER for one reversal, three reversals, five reversals, and seven reversals (i.e., seven back-to-back reversed pairs). As the table shows, the correlation values for one reversal are low across different algorithms. In general, the three reversals observe a higher correlation than one reversal and five reversals observe a higher correlation than three reversals. Beyond five reversals, the correlation values either remain steady or drop slightly due to noise. For example, for the 5-qubit Multiply algorithm, the one reversal correlation is 0.76, for three reversals, it is 0.96, and for five and seven reversals, it is 0.99. On the other hand, for the 8-qubit TFIM algorithm, the one reversal correlation is 0.38, the three reversal correlation is 0.53, the five reversal correlation is 0.71, but for seven correlations, it drops down to 0.60. Based on this empirical evidence, CHARTER selected five reversals as it was experimentally confirmed to be effective at identifying the impact of the gates on the final output error. However, we note that CHARTER’s design allows the number of reversals to be configurable and changed if needed. In our experience, the insights and trends generated by CHARTER are consistent for number of reversal beyond three.

As the above results show, CHARTER requires one run per gate in the circuit, which adds up as the number of gates increases. Therefore, next we look at how we can reduce the number of runs required to figure out the impact of gates.

B. CHARTER: Reducing the Number of Runs

As CHARTER only takes $g$ circuit runs for $g$ gates operations, it only scales linearly in terms of the number of gate operations: its time complexity is $O(g)$. However, the number of runs can be further reduced if we consider the gate type. Recall that on IBM computers, the basis gates are CX, RZ, SX, and X. While CX, SX, and X are physical gates that are implemented on the quantum computers, the RZ gate performs a frame-of-reference change virtually and is not implemented on the physical quantum computers [9]. Therefore, these gates have negligible to no impact on the output error of a quantum program (as we will also see in the evaluation section: Sec. V). As a result, they can be disregarded for the purposes of characterizing the error impact of different gates and their reversed runs can be eliminated from consideration.

Table IV shows the percentage of all quantum gate operations that are the RZ operation across different quantum algorithms. The table also shows the percentage of CX gates (the remaining gates are SX or X) and the circuit depth (number of gates in the critical path of the algorithm circuit).
for completeness. The table demonstrates that in general, around 20-40% of the gates in quantum algorithm tend to be RZ gates. For example, for algorithms like QFT (7) and TFIM (8), this the percentage of RZ gates can be as high as 42%. This directly implies that the number of runs required by CHARTER can be reduced by 20-40% in practice depending on the algorithm, even though the complexity remains \( O(g) \) in the worst case.

Next, we summarize the overall approach of CHARTER.

### C. CHARTER: Putting it All Together

In Fig. 6, we summarize the different steps of CHARTER. CHARTER takes the quantum program and maps it onto the quantum hardware and converts it into the hardware basis gates. Then, for each of the gates, it generates reversed circuits, each with their own pair of the reversed gate + the original gate applied right next to the original gate. The pair application is repeated five times over to generate the best success in terms of identifying the high-impact gates in the circuit. This is done for all gates except for the RZ gates as these gates are virtual and have negligible error impact. The next step is to run the original circuit and all the reversal circuits on the quantum computers. Once the runs are completed, the TVDs between the original circuit and the reversed circuits can be calculated and the high-impact gates can be determined by identifying the reversed circuits with high TVDs.

In the following section, we evaluate the effectiveness of CHARTER in identifying such high-impact gates and derive some surprising and interesting insights in the process.

## V. CHARTER: EVALUATION, ANALYSIS, AND INSIGHTS

This section is organized as following: we perform different types of analyses and present a summary of observations and insights for each of those. These analyses are performed for all the algorithms and benchmarks used for evaluation and general trends are highlighted. We also note diverging patterns when they are significant, and we provide strategies to mitigate the error impact of high-impact gates.

### Before we present these general results, we first perform a detailed case study using the three-qubit QFT algorithm, in order to better appreciate the insights derived from the combined trends presented later. This case study includes a breakdown of the error impact of individual gates in the QFT algorithm and an examination of how this error impact varies with the input provided to the algorithm.

#### QFT(3) Case Study and the Influence of the Input.

Fig. 7(a) shows the circuit structure of the three-qubit QFT algorithm. We see that the algorithm has 39 operations in total: 9 \( \text{CX} \), 18 RZ, 12 SX. So we run 39 reversed circuit runs + 1 original circuit run = 40 runs (combined runtime of < 0.5 hours on the IBM computers). We also see that the 39 operations are organized in 27 layers of parallel executions. Note that for this algorithm, we also run the reversed runs for the RZ gates to demonstrate that the RZ gates have negligible impact (but, in general, we do not need to execute the runs corresponding to the RZ gates). We calculate the 39 TVDs of the output of the reversed runs to the output of the original run.

Fig. 7(b) shows these TVDs. For easier interpretation, the figure has been structured into three sub-figures that show the results for the three qubits (qubit 0 at the top, 1 in the middle, and 2 at the bottom). The x-axis shows the layer at which the operation took place, corresponding to the layers indicated at the bottom in Fig. 7(a). The bars show the TVD for the individual gates on different qubits. The positions of the bars correspond to the positions of the gates in Fig. 7(a) (the bar colors also correspond to the operation colors). For two-qubit \( \text{CX} \) gates, the bar is drawn twice on both the qubits. For example, the bar corresponding to the \( \text{CX} \) gate on qubits 0 and 1 in layer 12 is drawn twice: at layer 12 on qubit 0 and at layer 12 on qubit 1. As the TVD ranges between 0 and 1, the y-axis of all three figures is from 0 to 1.

The first observation we make is that the RZ gates have negligible impact. The bars corresponding to the RZ gates are not visible due to the TVD being very low. For example, there are two RZ gates in layer 0 and layer 2 on qubits 1 and 2 in Fig. 7(a). However, when we look at layers 0 and 2 in Fig. 7(b), the bars are not visible due to their low impact. The lack of a visible bar can be verified for all RZ gates in the circuit. This demonstrates that the runs corresponding to the RZ gates can be eliminated from the characterization process. In the case of the three-qubit QFT algorithm, this means that the number of runs can be reduced from 40 to \( 40 - 18 = 22 \), which is a reduction of 45% in terms of the execution overhead.

Next, we identify the gates with the highest impact on the output error. In Fig. 7(b), we ran the three-qubit QFT circuit with input specified to ensure that the output has a hamming weight of zero (i.e., “000”). Fig. 7(c), (d), and (e) shows what happens for other inputs. In Fig. 7(c), we ran the three-qubit QFT circuit for a hamming weight of one (i.e., “001” or “010” or “100”). Similarly, Fig. 7(d) shows the results for
Fig. 7: (a) The circuit structure of the three-qubit QFT algorithm. TVD of the three-qubit QFT circuits between the reversed circuits and the original circuit when it is run with input such that the output has a hamming weight of (b) 0, (c) 1, (d) 2, and (e), 3. The results show that depending on the input, the impact of the different gates in the circuit can vary.

Changing the input for the QFT algorithm has a considerable effect on the impact that different gates have on the overall output error of the circuit. For example in Fig. 7(b), the gates with the highest impact include the CX gate on qubits 0 and 1 in layer 28. However, the SX gate on qubit 0 in layer 13 has a higher impact. In fact, in general, SX gates in the middle and end sections tend to have a high impact in Fig. 7(b). It is notable that in terms of the physical implementation, the same SX gate is being applied to qubit 0 in layers 11, 13, 16, 25, and 26. However depending on its position, it has a varying impact on the output error. On the other hand, in Fig. 7(c), the tallest TVD bars exist corresponding to four CX gates: (I) qubit 1 and 2 in layer 19, (II) qubits 1 and 2 in layer 21, (III) qubits 0 and 1 in layer 22, and (IV) qubits 0 and 1 in layer 24. SX gates are not high-impact for this input. In contrast, in Fig. 7(d), the CX and SX gates in the middle section of the circuit (layers 9 to 15) on qubits 0 and 1 have the highest impact compared to the CX gates at the end, and in Fig. 7(e), the CX and SX gates all across the length of the circuit (layers 1-2, 10-16, and 21-23) on qubits 0 and 1 have a high impact on the overall output error.

**Use case: CHARTER for Discovering High-Impact Inputs.** To figure out which input has the highest impact on the output error, CHARTER is leveraged as a technique to apply reversals to all input-related gates together (instead of one gate at a time) to estimate their combined impact. All input related gates are bunched together and reversed within the same circuit, instead of in different circuits. Applying this technique produces TVDs of the outputs of the reversed circuits to the output of the original circuit as following: TVD = 0.06 for hamming weight zero input (Fig. 7(b)), 0.02 for hamming weight one input (Fig. 7(c)), 0.06 for hamming weight two input Fig. 7(d), and 0.07 for hamming weight three input (Fig. 7(e)). CHARTER reveals that the input in Fig. 7(e) (hamming weight of three) has the highest impact, which is also evidenced by the fact that it is the only input with high-impact gates in layers 1-2.

**Observation 1.** Previous works that focus on reducing the output error on noisy quantum computers using...
compiler optimizations focus on high-level optimizations based on simplistic assumptions [34], [37], [39], [57]. As an instance, previous works have focused on optimizing the mapping to hardware based on error information of the gates obtained during computer calibration in isolation or via micro-benchmarking, that is, one number is used per physical gate type [49], [51], [57]. However, CHARTER has shown that the same physical gate can have very different impact based on its position within the circuit – this requires critical consideration for compiler optimizations which is currently lacking in existing quantum compiler solutions.

**Observation II.** Using CHARTER, we also showed that depending on the changes in the input, which changes the gate structure at the beginning of the circuit, the impact of the different gates will vary even if the rest of the circuit structure is the same. This means optimizations that are based purely based on circuit structure [6], [13], [26] (e.g., gate deletion and synthesis [2], [41], [48], [56] and layout mapping and routing [25], [62], [63]) may be sub-optimal due to the lack of input-awareness. An effective demonstrated use case of CHARTER’s includes performing a combined reversal on all input-related gates to identify the inputs with the highest impact on the output error.

**The Effect of Gate Position Along the Length of the Circuit.** In the three-qubit QFT examples for different inputs, we saw that gates in any layer position along the circuit length can be high-impact gates (e.g., Fig. 7(e)). However, conventional wisdom suggests that error impacts are especially worse near the end of the circuits due to the qubit state losing coherence. Recall that over time, the qubit state tends to lose its phase and amplitude and decay to the ground (i.e., the $|0\rangle$ state [31], [53]). So this effect gets particularly worse at the end layers of a quantum circuit execution.

While previously there did not exist a way to test the above conventional wisdom, now CHARTER enables us to determine if this conventional wisdom is true. To perform this test, we correlate the impact of the gates (i.e., the TVD between the reversed circuit corresponding the gate and the original circuit) with the layer in which it is positioned. If the correlation is high, it suggests that as the layer index increases, the gate impact also increases, that is, it suggests that the assumption is true. For example, say we have gates $G = \{g_1, g_2, g_3, g_4, g_5\}$ with TVDs $T = [0.1, 0.2, 0.3, 0.32, 0.4]$; the gates are positioned in layers $L = [1, 2, 3, 3, 4]$. If we correlate the TVD vector $T$ with the layers vector $L$, we would observe a high correlation. If instead, $T = [0.2, 0.1, 0.1, 0.2, 0.1]$, we would observe a low correlation.

CHARTER performs this correlation for all evaluated algorithms and the results are reported in Table V. The table shows the Pearson correlation numbers along with the corresponding p-values. As the table shows, for most algorithms (e.g., HLF (5), QFT (3), Adder (9), Multiply (5), TFIM (4), and XY (4)), the correlation numbers are not high and the p-value numbers are high (> 0.01), which indicates that no strong correlation exists between the impact of a gate and the layer in which it is located. The highest correlation among all algorithms of 0.58 can be seen for the Multiply (10) algorithm. On the other side of the spectrum, the QFT (7) algorithm has a correlation of $-0.66$. The negative correlation indicates that most of its high impact gates are located in the front section of the circuit.

**Analysis of Multiple Architectures using VQE.** To demonstrate that CHARTER’s analysis are applicable to different quantum computing architectures and topologies, we run the VQE circuit on ibmq_quadalupe, along with the default execution on ibm_lagos. As the VQE circuit is a four-qubit circuit, we choose the first four qubits of the two computers for execution to make use of different topologies; Fig. 4 shows qubits 0, 1, 2, and 3 form a T-shape on ibm_lagos and a line on ibmq_quadalupe. Due to this difference in topologies, when VQE is mapped to ibmq_quadalupe, it has 135 RZ gates – as opposed to the the default of 172 on ibm_lagos – and 74 CX gates – as opposed to 132 on ibm_lagos. However, in spite of these differences, the correlation between the error impact of a gate and its position within the program is 0.41 (p-value: 1e−13) on ibmq_quadalupe; it is 0.21 on ibm_lagos. The low correlation on both computers shows that CHARTER’s analysis is applicable to different computer architectures and topologies.

**Observation III.** Due to the property of NISQ qubits of losing their coherence over time, it has been assumed that a large portion of the output error is accumulated near the end of the circuit based on the study of decoherence effects in isolation [31], [53]. In fact, some
TABLE VI: Percentage of all program qubits that appear in top 5%, 10%, 25% and 50% of high-error-impact gates. High-impact gates can exist across different qubits for all algorithms.

| Algorithm     | Top 5% | Top 10% | Top 25% | Top 50% |
|---------------|--------|---------|---------|---------|
| HLF (5)       | 40%    | 40%     | 60%     | 100%    |
| HLF (10)      | 70%    | 100%    | 100%    | 100%    |
| QFT (3)       | 67%    | 67%     | 100%    | 100%    |
| QFT (7)       | 57%    | 71%     | 86%     | 100%    |
| Adder (4)     | 100%   | 100%    | 100%    | 100%    |
| Adder (9)     | 78%    | 100%    | 100%    | 100%    |
| Multiply (5)  | 40%    | 60%     | 100%    | 100%    |
| Multiply (10) | 90%    | 100%    | 100%    | 100%    |
| QAOA (5)      | 40%    | 60%     | 60%     | 100%    |
| QAOA (10)     | 90%    | 90%     | 100%    | 100%    |
| VQE (4)       | 100%   | 100%    | 100%    | 100%    |
| Heisenberg (4)| 100%   | 100%    | 100%    | 100%    |
| TFIM (4)      | 75%    | 100%    | 100%    | 100%    |
| TFIM (8)      | 88%    | 100%    | 100%    | 100%    |
| TFIM (16)     | 94%    | 100%    | 100%    | 100%    |
| XY (4)        | 50%    | 50%     | 100%    | 100%    |
| XY (8)        | 100%   | 100%    | 100%    | 100%    |

previous works have proposed software-level compiler optimizations that are especially catered toward the end or the beginning of the quantum circuit [27], [44].

**CHARTER** demonstrate that these conventional assumptions do not hold true for many real-world quantum algorithms with complex circuit structures that face the combined effect of all different types of hardware noises, when they are executed on different quantum computer architectures and topologies. Depending on the circuit properties of the algorithm, the high-impact gates can be evenly distributed, they can be bundled in the front section of the circuit, or they can be bundled in the back section.

The Impact of Individual Qubit’s Error Rates. In the QFT (3) results in Fig. 7, we observed that most of the high-impact gates were situated on qubit 0, then there were a few on qubit 1, and there were no high-impact gates on qubit 2. This example is a good representation of the common way of performing noise characterization of quantum computers. Many works focus on characterizing the noise effects at the level of individual qubits or at the level of specific types of operations performed on individual qubits [8], [14], [29], [38], [43], [58]. For example, previous works have relied on data obtained during computer calibration to estimate the error rates of qubits to perform noise-aware compilation and reduce the gate count on high-error qubits [34], [37], [39], [51], [57].

**CHARTER**’s novel methodology enables us to investigate if this broad classification of qubits as being high-error or low-error based on simplistic noise models or isolation noise analysis holds true when we look at the impact of individual gates. In other words, we want to study if all the high-impact gates are concentrated on a few qubits (which would encourage us to broadly classify those qubits as high-error) or if these high-impact gates are distributed across the different qubits that are involved in the quantum circuit.

First, we note that, unlike the case of studying the concentration of high-impact gates across the length of the circuit, we cannot use correlation to perform this check as the actual qubit ids are not of relative significance. For example, layer 1 is after layer 0 for a correlative study but qubit ids have no relative relationship. Therefore, instead, in Table VI, we show the percentage of all qubits in a circuit that are involved in the top 5% (i.e., gates with the top 5% highest TVD between the corresponding reversed circuits and the original circuit), 10%, 25%, and 50% of high-impact gates. Note that we do not use just one threshold to define high impact, as this threshold may vary from algorithm to algorithm and use-case to use-case.

As the results show, for most of the algorithms, a majority of the qubits are involved in top 5% of the high-impact gates and a 100% of the qubits are involved in the top 25% of high impact gates. Even for relatively larger algorithms like TFIM (16), 15/16 qubits (94%) are involved in the top 5% of high impact gates. If we look at the top 50% column, we see that a 100% of the qubits are involved in high-impact gates across all of the evaluated algorithms. These results suggest that most qubits can have gates that have a high-impact on the output error and it is preferable to identify the error of specific gates, than to broadly classify qubits as being high error or low error.

The Role of One-Qubit Gates in Output Error. In the QFT (3) results in Fig. 7, we observed that both \( CX \) and \( SX \) gates can be high-impact gates, depending on the input to the program. However, due to the fact that \( CX \) gates tend to have an order of magnitude higher error rate than \( SX \) or \( X \) gates when measured in isolation [38], [39], many software-level compiler works have specifically focused on minimizing the number of \( CX \) gates in the circuits. This has been in the form of directing trying to reduce the \( CX \) gates using mathematical equivalencies based on the commutativity and unitary properties of gates.
TABLE VII: Number and percentage of one-qubit $SX$ and $X$ gates that have a greater error impact than the $CX$ gate with the least error impact (compared to other $CX$ gates). A large portion of one-qubit gates have a higher impact than $CX$ gates.

| Algorithm   | Num. $SX+X$ | % $SX+X$ | Algorithm   | Num. $SX+X$ | % $SX+X$ |
|------------|-------------|----------|------------|-------------|----------|
| HLF (5)    | 7           | 70%      | QAOA (5)   | 22          | 71%      |
| HLF (10)   | 45          | 92%      | QAOA (10)  | 58          | 89%      |
| QFT (3)    | 9           | 56%      | VQE (4)    | 119         | 98%      |
| QFT (7)    | 78          | 98%      | Heisenberg (4) | 141     | 96%      |
| TFIM (4)   | 30          | 83%      | Adder (4)  | 20          | 74%      |
| TFIM (8)   | 179         | 95%      | Multiply (5) | 20     | 80%      |
| TFIM (16)  | 772         | 98%      | Multiply (10) | 117    | 100%     |
| XY (4)     | 21          | 75%      | -          | -           | -        |
| XY (8)     | 158         | 98%      | -          | -           | -        |

within the circuit [45], [64], and in the form of trying to reduce the number of $SWAP$ operations, each of which is implemented using three $CX$ gates [3], [55].

While these techniques are effective at reducing the number of $CX$ gates, they also have a significant compilation time overhead. $CHARTER$ can be used to study if these techniques are worth the overhead considering that they only focus on $CX$ gates, which are assumed to be high-impact due to their relatively higher isolation error rates. We also saw for the QFT (3) example, that some $SX$ gates can have a much higher impact than $CX$ gates. To investigate if this is the case across different algorithms, in Table VII, we present the percentage of one-qubit $SX$ and $X$ gates in the circuit that have a greater error impact than the $CX$ gate with the least error impact compared to other $CX$ gates in the circuit. We compare to the $ CX$ gate with the least error impact as all $CX$ gates are targeted for compiler optimizations regardless of their specific error impact. So the one-qubit $SX$ or $X$ gates that have a higher impact than that $CX$ gate can be judged to have a high impact overall – this can be caused by potentially higher crosstalk effects and neighboring gate operations around the qubits where $SX$ and $X$ gates are being performed.

The results in the table show that across different algorithms, 50% to over 90% of all $SX + X$ gates tend to have a higher impact than the $CX$ gate with the least error impact in the circuit. For example, for the XY (8) algorithm, 98% of the $SX + X$ gates have a higher error impact. These results highlight the need to focus on impact-aware compiler optimizations for gates instead of type-aware.

$CHARTER$’s Mitigation Strategy. This above observation about high-impact one-qubit gates is also evidenced by the fact that the $SX$ gates on qubit 0 in layers 1 and 2 have some of the highest impact in Fig. 7(e). This is because there are parallel $SX$ gates on qubits 2 and 3 in layers 1 and 2 for this input, which causes increased crosstalk effect on qubit 0. As a mitigation strategy, we inserted barriers to make sure the gates in these two layers are executed serially instead of in parallel and observed the output error (TVD of the observed output to the ideal output) drop from 0.19 to 0.12 (i.e., 7% points reduction). Note that all operations in a circuit cannot be serialized as this would increase circuit depth and decoherence effects. However, this strategy is effective when used selectively for the highest-impact gates.

**Observation V.** Due to the fact that $CX$ gates have an order of magnitude higher error rate when the error rate is measured in isolation [38], [39], it is often assumed that these gates also have the highest error impact in quantum circuits when run on NISQ computers [3], [45], [48]. Previous works have focused on minimizing the impact of $CX$ gates by trying to reduce their number in quantum circuits [2], [41], [55], [56], [64].

In contrast, we have leveraged $CHARTER$ to demonstrate an interesting insight: one-qubit $SX$ and $X$ gates also have a high impact on the output error, and in some cases this impact is higher than that of $CX$ gates. In fact, across different quantum algorithms, 50%-98% of all $SX + X$ gates have a higher error impact than the $CX$ gate with the least error impact in the algorithm circuit. $CHARTER$ serves as a useful utility for the programmer to not rely on generalized assumptions and determine gate-specific error impact. As show by $CHARTER$, identification and selective serialization of gates can act as an effective mitigate strategy for reducing the impact of high-impact gates.

VI. WORK RELATED TO $CHARTER$

Previous works relevant to $CHARTER$ are as following:

**Noise Characterization.** Previous works have focused on characterizing different aspects of the noise on NISQ computers, from examining a specific type of noise such as decoherence effects [31], [53], to benchmarking and micro-benchmarking different gates and algorithms on quantum computers to figure out the kinds of errors they experience [8], [14], [29], [38], [43], [58]. For example, Erhard et al. [14] perform cycle benchmarking on quantum computers to figure out how their noise characteristics manifest in different algorithms. However, none of these works characterize the impact that a specific gate has on the output error of a quantum program. $CHARTER$ makes a novel contribution in that space.

**Program Debugging.** Previous works have introduced debugging techniques for quantum code [18], [19], [28], [30], [61]. Some of these works propose the use of statistical assertions to debug the functionality of the circuits [19], [28], [30], while others propose new programming interfaces and frameworks for semantics-based debugging [18], [61]. $CHARTER$ can further enhance the capability of these works by enabling gate-specific debugging of errors.

**Compiler Optimizations.** Different types of software-based compiler optimizations have been proposed to reduce the impact of noise when quantum algorithms are run on quantum computers, including works that mitigate the effect of crosstalk [35], [59], perform noise-optimal compilation using
isolation noise characteristics [34], [37], [39], [51], [57],
synthesize circuits to reduce their length [2], [41], [48], [56],
perform layout-aware routing and mapping [25], [62], [63],
leverage optimizations targeting specific circuit regions (e.g.,
end of the circuit) [27], [44], reduce the number of C×
gate operations [3], [41], [45], [55], [64], perform optimizations
without considering the input [6], [13], [26], [49], and even
use the reversibility property at the circuit level to improve
the output error (although, it requires ideal simulations on
classical computers) [40]. While none of these works provide
a methodology like CHARTER’s to help programmers learn
about the impact that specific gates have on the output of their
program, many of them can benefit from this functionality
to further improve the compiler optimizations that are applied.

VII. CHARTER: CONCLUDING REMARKS

In this paper, we proposed CHARTER, a simple and effective
technique that leverages reversibility property of quantum
circuits to identify high-impact error-prone gate operations in
quantum programs. CHARTER demonstrates the usability of
quantum operation reversibility for identifying most critical
quantum operations – extending the application of quantum
operation reversibility beyond estimating and improving an-
swer fidelity of quantum programs [40].

By applying CHARTER to a variety of quantum algorithms
and benchmarks with different characteristics, we highlighted
several surprisingly and counter-intuitive trends, such as the
observation that high-impact error-prone gates can be located
anywhere within a quantum program. CHARTER’s open-source
implementation and dataset is available to future innovations
in compiler optimization and algorithm debugging techniques.

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SUMMARY OF THE EXPERIMENTS REPORTED
Below is the experimental methodology.

(1) **Experimental Setup.** We use the IBM quantum cloud platform to execute the experiments to evaluate Charter. We use the corresponding Python-based (Python version 3.9.7) Qiskit programming language (Qiskit version 0.17.4) to program the quantum algorithms and benchmarks and apply reversals for Charter. We run the experiments on the 7-qubit ibm_lagos quantum computer and the 16-qubit ibmq_quadalup quantum computer, depending on the size of the algorithm being executed. Each experiment is run with 32,000 trials to generate the output probability. We use Qiskit’s StateVector simulator to run simulations of the quantum programs on classical computers to get the ideal output of the programs. Note that this output is only used to validate the effectiveness of Charter and is not a part of the Charter technique. In fact, Charter is specifically designed to not rely on classical simulations in order to ensure scalability to large quantum algorithms. Python’s SciPy package is used to calculate statistical metrics such as correlation for the design and analysis of Charter.

(2) **Quantum Algorithms and Benchmarks.** Charter uses algorithms and benchmarks, which have a variety of sizes (3-16 qubits) and use cases for high-performance computing. HLF is a search algorithm, while QFT is the quantum version of the Fourier transform. QAOA and VQE are quantum variational algorithms, and Adder and Multiplier are standard quantum arithmetic circuits. Heisenberg, TFIM, and XY are time-evolution Hamiltonian programs for material simulations. The TFIM model has non-zero coupling interaction between nearest neighbor spins along the z axis, XY has for x and y axes, and Heisenberg has for all three axes. All algorithms are mapped to the physical quantum hardware using all of the compiler optimizations available via Qiskit, including noise-aware mapping and routing, gate cancellation and deletion based on commutativity and combination, and gate synthesis. All algorithms are converted to the cx rz, sx, x basis gate set during the mapping process to run on the IBM hardware.

(3) **Metrics.** The output of a quantum program is obtained as a probability distribution over its output states. The same quantum state is prepared and measured multiple times (each measurement producing one output state), which then generates the probability distribution over the output states. However, because of the hardware noise effects, this observed output distribution can be quite different from the ideal or correct output distribution. A typical metric that is used to measure the deviation of the observed output distribution from the ideal output distribution is the Total Variation Distance or TVD. The TVD between two probability distributions is calculated by summing up the absolute differences in the probabilities of the individual states and dividing by two. With a value between 0 and 1, the closer the TVD is to 0, the more the two probability distributions are similar. We will use this metric going forward to compare two probability distributions. To measure the correlation relationship between two random variables, we use the Pearson correlation, which is the square-root of the coefficient of linear regression ($r^2$). A value of 1 indicates a perfect positive linear correlation, −1 indicates a perfect negative linear correlation, and 0 indicates no correlation. We also show the p-value to show the significance of the correlation (a p-value < 0.01 indicates a statistically strong correlation).

Instructions to reproduce main results in the paper (results shown in Fig. 6) are provided below. Note that we provide the code in a python virtual environment, because it is not possible to provided it in a container due to the requirement of enter IBM credentials (using free IBM account) before the code is executed.

(1) **Create Virtual Environment.** Run with python version 3.9.10 installed: python -m venv venv

(2) **Activate Virtual Environment.** source venv/bin/activate

(3) **Install Requirements.** pip install -r requirements.txt

(4) **Insert IBM Credentials.** In line 26 of code/apply_charter_to_qft.py, insert IBM Quantum access token. The instructions to create a free account and obtain a token can be found here https://quantum-computing.ibm.com/lab/docs/iql/manage/account/ibmq and will enable connection to IBM Quantum resources.

(5) **Execute.** In the code directory, run python apply_charter_to_qft.py to run Charter. The results of this will be generated in the “output” directory. In the code directory, view results afterwards with python process_qft_output.py. The results of the plots will be generated in the “plots” directory. NOTE: Output Directory may download as a file instead of a directory due to git convention. If this is the case, creating an empty “output” and “plot” directory at the root level will be necessary.

**AUTHOR-CREATED OR MODIFIED ARTIFACTS:**

Artifact 1
Persistent ID: https://doi.org/10.5281/zenodo.6875323
Artifact name: Virtual Environment Setup Instructions and Code

URL

Reproduction of the artifact with container: Instructions to reproduce main results in the paper (results shown in Fig. 6) are provided below. Note that we provide the code in a python virtual environment, because it is not possible to provided it in a container due to the requirement of enter IBM credentials (using free IBM account) before the code is executed.

Create Virtual Environment:
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