Gate-controlled non-volatile graphene-ferroelectric memory

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In this letter, we demonstrate a non-volatile memory device in a graphene FET structure using ferroelectric gating. The binary information, i.e. “1” and “0”, is represented by the high and low resistance states of the graphene working channels and is switched by controlling the polarization of the ferroelectric thin film using gate voltage sweep. A non-volatile resistance change exceeding 200% is achieved in our graphene-ferroelectric hybrid devices. The experimental observations are explained by the electrostatic doping of graphene by electric dipoles at the ferroelectric/graphene interface.

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The discovery of graphene in 2004 [1, 2, 3] has triggered enormous experimental and theoretical efforts [4, 5]. As a gapless semiconductor, charge carriers in graphene can be tuned continuously from electrons to holes crossing the charge neutral Dirac point using an external electric field. Unlike conventional semiconductors, the doping process does not influence the mobility of charge carriers in graphene, which can exceed $10^5$ cm$^2$V$^{-1}$s$^{-1}$ at low temperature [6, 7]. Such doping-independent mobility leads to the field-dependent conductance in graphene. Based on these two properties, many novel graphene-based device applications have been predicted or demonstrated [8, 9, 10, 11, 12, 13, 14, 15, 16], including the heavily-explored graphene-based field-effect transistor (GFET) [17, 18, 19, 20, 21, 22]. However, a paradigm shift in the microelectronics industry from Si to graphene also requires graphene-based memory applications. Despite graphene intrinsically having a high resistance state at the Dirac point and a low resistance state when heavily doped, reports on graphene for non-volatile information storage is rarely seen. This is due to the difficulty in maintaining the resistance states in graphene without an external electric field. One chemical modification approach to achieve non-volatile switching in graphene has been recently proposed by Echtermeyer et al [19]. Although this method can achieve very high on-off ratio, it alters the unique crystalline structure of graphene upon which many of the extraordinary electronic properties and hence most novel device concepts are based [4, 5].

In this letter, we show non-volatile switching in graphene by using ferroelectric gating without having to break the lattice symmetry. We demonstrate basic writing and reading processes of this novel graphene-ferroelectric memory device structure combining the field-dependent conductance of graphene with the remnant electric field of ferroelectric thin films. A bistable state of high and low resistance value is realized by controlling the electrical doping level in graphene hysteretically, which is caused by a hysteretic switching of the polarization in the ferroelectric thin film.

The sample geometry of our graphene-ferroelectric memory devices is shown in Fig. 1a. The bottom electrodes, patterned by electron-beam lithography, were prepared by thermal evaporation of Cr/Au (5/30 nm). A ferroelectric thin film of poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) was then spin-coated with a thickness of approximately 0.7 µm. From atomic force microscopy (AFM), we conclude that P(VDF-TrFE) forms a continuous thin film on graphene devices.

FIG. 1: (a) Sample geometry of a finished graphene-ferroelectric memory device. (b) Optical image of a graphene sample showing the Hall-bar geometry of the bottom electrodes. (c) R vs $V_{BG}$ of the graphene sample before P(VDF-TrFE) coating, measured in two-terminal configuration. (d) AFM image of another graphene sample after P(VDF-TrFE) spin-coating. The contrast comes from the slightly different crystallization of P(VDF-TrFE) on SiO$_2$, Graphene and Au electrodes respectively. (e) Optical image of a finished device.

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FIG. 2: Electric hysteresis loop; R as a function of V_{TG} for the graphene-ferroelectric sample. The resistance peak at 44 V (-32 V) corresponds to the flipping of electric dipoles in P(VDF-TrFE) from upward (downward) to downward (upward). From the linear part of this curve at high voltage, the charge carrier mobility is estimated to be 700 cm²V⁻¹s⁻¹, taking κ_{PVDF} = 10 [23].

For all devices, resistance R vs the bottom gate voltage (V_{BG}) has been recorded for reference before P(VDF-TrFE) coating. After thermally evaporating the top gate electrodes (Fig. 1), samples were electrically characterized at room temperature in vacuum in a four-contact configuration using a lock-in amplifier with an ac excitation current of 10 nA. The number of graphene layers is confirmed by Raman spectroscopy. In total, we have successfully studied 15 samples. For the representative sample used here, the charge carrier mobility before P(VDF-TrFE) is ~ 1500 cm²V⁻¹s⁻¹, estimated from the linear slope of the R vs V_{BG} curve [8], as shown in Fig. 1.

We now present the main experimental observations. As shown in Fig. 2, the most important feature for all measured samples is a pronounced hysteresis in resistance measurements when the top gate voltage (V_{TG}) is swept in a closed loop: 0 V to 85 V, 85 V to -85 V, and finally from -85 V back to 0 V. Similar to the magnetoresistance measurements of a giant magnetoresistance (GMR)/tunneling magnetoresistance (TMR) device, we observe a hysteretic switching between the maximum resistance (R_{max}) and the minimum resistance (R_{min}), but now as a function of the applied electric field, E. For the sample in Fig. 2 the resistance change ratio, ΔR/R = (R_{max} - R_{min})/R_{min}, is larger than 350%.

This hysteretic behavior and the double peak structure in R vs V_{TG} curves are closely related to the polarization of P(VDF-TrFE) thin film. As illustrated in the inset a of Fig. 3, the continuity of electric displacement field, D, at the ferroelectric/graphene interface requires D = \varepsilon_0κ_{ferro}E_{ferro} + P(V_{TG}) = -n(V_{TG})e, where E_{ferro} and n(V_{TG}) are the electric field in ferroelectric and the charge carrier concentration in graphene respectively [24]. Here, the dielectric response of the ferroelectric separates into a linear part (\varepsilon_0κ_{ferro}E_{ferro}) and a hysteretic part (P(V_{TG})). While the linear dielectric part induces electrical doping in graphene with an opposite sign to V_{TG}, P(V_{TG}) can induce electrical doping with either sign. These two components compete with each other such that graphene can remain p-doped (n-doped) even with a positive (negative) V_{TG} until either the doping contribution from the linear part exceeds P(V_{TG}) or the polarization direction of the ferroelectric is switched. It is this behavior which leads to the hysteretic doping of graphene as a function of V_{TG}. Considering that the conductance of graphene is σ = n(V_{TG})/μ, the observed resistance hysteresis loop is now directly related to P(V_{TG}) by

\[
D = \varepsilon_0κ_{ferro}E_{ferro} + P(V_{TG}) = -n(V_{TG})e = \sigma/μ. \quad (1)
\]

Using this equation, we convert the R vs V_{TG} curve in Fig. 2 into D vs E characteristics, which is further compared with the direct electric displacement measurement of P(VDF-TrFE) thin film alone, D'. As shown in Fig. 3 D and D' have very similar coercive fields (E_{C}) of ~ 50 MV/m, consistent with the typical E_{C} reported in literature [25]. This agreement strongly suggests that the hysteresis observed in the transport measurements is indeed caused by the hysteretic polarization of the ferroelectric gate dielectric. From Fig. 3 we can also see that the left and right resistance peaks in Fig. 2 correspond to the flipping of electric dipoles from upward to downward and from downward to upward, respectively, while R_{min}
FIG. 4: (a) Writing “0” into graphene-ferroelectric memory by a full loop sweep of $V_{TG}$ ($\pm 85$ V). The memory bit is in “0” state before writing. (b) Writing “1” into graphene-ferroelectric memory by an asymmetrical loop sweep of $V_{TG}$ (85 V to -34 V). The memory bit is in “1” state before writing. (c) Writing “0” into graphene-ferroelectric memory by a full loop sweep of $V_{TG}$. The memory bit is in “1” state before writing. (d) Writing “1” into graphene-ferroelectric memory by an asymmetrical loop sweep of $V_{TG}$. The memory bit is in “0” state before writing.

in Fig. 2 is related to the maximum polarization point in Fig. 3. Another important parameter in Fig. 2 is the zero-field resistance $R_{P_{t}}$, corresponding to a remnant polarization $P_{r}$ of P(VDF-TrFE) in Fig. 3.

For device operation, we utilize the maximum resistance peak ($R_{1} \simeq R_{max}$) as bit “1”, while bit “0” is represented by $R_{P_{t}}$. As shown in Fig. 4a and 4d, a major hysteresis loop, corresponding to a full symmetrical $V_{TG}$ sweep ($\pm R_{max}$), can set the memory to “0”, independent of the existing state. In Fig. 4a, “0” has been rewritten into “0”, while in Fig. 4d, the binary information has been reset from “1” to “0”.

In contrast, writing “1” into graphene-ferroelectric memory requires a minor hysteresis loop with an asymmetrical $V_{TG}$ sweep to minimize the polarization in P(VDF-TrFE) thin film when $V_{TG}$ is back to zero. As shown in Fig. 4b and 4c, a minor hysteresis loop with $V_{max} = 85$ V and $-V_{max} = -34$ V can set the resistance state of graphene channel to near $R_{max}$, independent on the initial state of “1” (Fig. 4b) or “0” (Fig. 4c).

Thus, using major and minor hysteresis loops, we can realize non-volatile switching in graphene-ferroelectric memory. Note that the switching voltage can be reduced by one order of magnitude by simply scaling the thickness of P(VDF-TrFE) to the range of 100 nm. The difference between the two resistance states ($\Delta R/R = (R_1 - R_{P_{t}})/R_{P_{t}}$) is decided by the difference between the minimum polarization ($P_{min}$) and the remnant polarization ($P_{r}$) in P(VDF-TrFE). For the sample discussed here, the resistance change $\Delta R/R \sim 200\%$. The read-out of the binary information of graphene-ferroelectric memory can be simply done by measuring the device resistance using an excitation current as low as 1 nA. Note that this hybrid memory structure can in principle retain the high charge carrier mobility in graphene, which is crucial for ultra-fast device applications. In fact, the reading speed of an ideal device can be as fast as several tens of femtoseconds when operating at 1 V with a channel length of 1 $\mu$m and charge carrier mobility of $\mu = 200,000$ cm$^2$V$^{-1}$s$^{-1}$.

Before concluding, we discuss how to improve the performance of graphene-ferroelectric devices. First, $\Delta R/R$ can be much improved by removing contaminant residues on the graphene surface (enhancing interfacial coupling) and more importantly, by improving the charge carrier mobility in graphene. For a ideal ferroelectric/graphene interface, $\Delta R/R$ can be as large as $\sim (1/\mu_{min})/(1/\mu_{r})$, where $\mu'$ is the mobility at $P_{max}$. Another important approach is to increase the remnant polarization by applying larger electric field. A better approach would be the preparation of graphene sheets directly on ferroelectric substrates, which would allow the use of other ferroelectric materials with much higher remnant polarization. Other strategy would be to open a band gap in graphene, either by using bilayer graphene or graphene nanoribbons.

In conclusion, we have demonstrated the working principle and real device operation of a novel hybrid non-volatile memory device using graphene and ferroelectric thin film. Reversible non-volatile switching between the high resistance state and the low resistance state in graphene has been realized by choosing major or minor hysteresis loops. Using the electric displacement continuity equation, we show that the resistance hysteresis loop and the switching between the high and low resistance states are due to the electric dipole induced doping in graphene by the ferroelectric thin film. Currently, the resistance change, $\Delta R/R$, exceeds 200% and can be further improved by improving the quality of ferroelectric/graphene interface, the charge carrier mobility in graphene, and by increasing the remnant polarization of ferroelectric thin film. These make this new memory structure a promising candidate for the next generation of ultra-fast non-volatile memory.

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