Adaptive 3D-IC TSV Fault Tolerance Structure Generation

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Abstract—In three dimensional integrated circuits (3D-ICs), through silicon via (TSV) is a critical technique in providing vertical connections. However, the yield and reliability is one of the key obstacles to adopt the TSV based 3D-ICs technology in industry. Various fault-tolerance structures using spare TSVs to repair faulty functional TSVs have been proposed in literature for yield and reliability enhancement, but a valid structure cannot always be found due to the lack of effective generation methods for fault-tolerance structures. In this paper, we focus on the problem of adaptive fault-tolerance structure generation. Given the relations between functional TSVs and spare TSVs, we first calculate the maximum number of tolerant faults in each TSV group. Then we propose an integer linear programming (ILP) based model to construct adaptive fault-tolerance structure with minimal multiplexer delay overhead and hardware cost. We further develop a speed-up technique through efficient min-cost-max-flow (MCMF) model. All the proposed methodologies are embedded in a top-down TSV planning framework to form functional TSV groups and generate adaptive fault-tolerance structures. Experimental results show that, compared with state-of-the-art, the number of spare TSVs used for fault tolerance can be effectively reduced.

Index Terms—3D-IC, fault-tolerance, TSV planning, TSV yield.

I. INTRODUCTION

As device feature sizes continue to rapidly decrease, the interconnect delay is becoming a bottleneck limiting IC performance. Three dimensional integrated circuits (3D-ICs) technology involves vertically stacking multiple dies connected by through silicon vias (TSVs), providing a promising way to alleviate the interconnect problem and achieve a significant reduction in chip area, wire-length and interconnect power [1]. Study indicates that the average wire-length of a 3D-IC varies according to the square root of the number of layers [2]. Moreover, 3D-ICs also offer the potential for heterogeneous integration, which is essential for More than Moore (MtM) technology [3]. 3D integration has already seen commercial applications in the form of 3D memory but there are still significant open problems in both research and implementation [4]. In this work, we will focus on the TSV reliability problem.

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TSVs may be affected by various reliability issues such as undercut, misalignment, or random open defects [5]. Because there exist a large number of TSVs in a chip, these issues in turn lead to low chip yield. For example, [5], [6] reported a 60% chip yield for a chip with 20000 TSVs and only 20% yield for 55000 TSVs in IMEC process technology. Since yield and reliability is a primary concern in 3D ICs design, a robust fault-tolerance structure is imperative. In general, there are two types of yield losses in 3D-ICs: the yield loss due to defects in stacked dies and the yield loss due to defects occurred during assembling process [7]. For the former case, it is critical to conduct pre-bond testing to avoid the stacking of defective dies [8]. A number of die/wafer matching and inter-die repair strategies have also been proposed to increase the stack yield [9]–[12]. For the latter case, adding spare TSVs (referred to as s-TSVs) to repair fault functional TSVs (referred to as f-TSVs) is an effective method for enhancing yield.

One key problem in TSV fault-tolerance design is the fault-tolerance structure generation, where a number of functional TSVs and one or several spare TSVs are grouped together to provide redundancy. Chen et al. [6] proposed a minimum spanning tree based method to group f-TSVs and form one-fault-tolerance structures. However, the method is difficult to be applied to multiple-fault-tolerance structure generation. Wang et al. [13] presented a regular TSV replacing chain structure that can repair faulty TSVs based on a realistic clustered defect model. Xu et al. [14] further considered the physical information of the TSV groups, and developed an ILP formulation for fault-tolerance structure generation. They model replaceable relations between f-TSVs, so the maximum input-port number of individual multiplexers can be effectively reduced. However, all previous works [13], [14] are under an assumption that a predetermined number of s-TSVs are assigned to each TSV group. To ensure that K common s-TSVs can be allocated to each f-TSV group, in each group f-TSV number is usually quite small, which introduces a large number of TSV groups. Since the total number of s-TSVs is proportional to the TSV group number, it may cause overuse of s-TSVs.

To overcome the above issue, in this paper we propose an adaptive fault-tolerance structure, in which the number of tolerant faults is adaptively determined by the distribution of the f-TSVs and their candidate s-TSVs. A set of s-TSVs will be selected from a large amount of candidates. Our adaptive fault-tolerance structure generation method can achieve minimal multiplexer delay overhead, as well as minimal number of required s-TSVs. Key technical contributions of this work...
The method for determining the maximum number of tolerant faults is presented in Section III. Section IV and Section V present the proposed ILP formulation and heuristic method.

Experimental results show that, compared with state-of-the-art, the proposed framework can reduce the number of used s-TSVs and maximum port number of multiplexers.

The remainder of this paper is organized as follows. Section II presents the motivation and gives the problem formulation. The method for determining the maximum number of tolerant faults is presented in Section III. Section IV and Section V present the proposed ILP formulation and heuristic method. Section VI describes the proposed fault tolerance TSV planning methodology. Section VII provides experimental results, followed by conclusion in Section VIII.

II. PRELIMINARIES

A. Chip Yield and TSV Yield

Consider a 3D IC containing $l$ layers, and the yield of $i^{th}$ layer die is $Y_{die_i}$. The yield for wafer-to-wafer (W2W) stacking $Y_{stack}$ can be roughly modeled as [7]:

$$ Y_{stack} = \prod_{i=1}^{l} Y_{die_i}. \tag{1} $$

Therefore, the defects in each die will certainly affect the overall chip yield after stacking.

Besides, during bonding, any foreign particle caught between the wafers can lead to peeling, as well as delamination, which dramatically reduces bonding quality and yield [15]. $Y_{Bonding}$ captures the yield loss of the chip due to faults in the bonding processes.

According to the cumulative yield property, the yield of a 3D chip $Y_{3D-chip}$ can be formulated as follows [7]:

$$ Y_{3D-chip} = Y_{stack} \cdot \prod_{i=1}^{l-1} (Y_{Bonding(i)} \cdot Y_{TSV(i)}), \tag{2} $$

where $Y_{Bonding(i)}$ is the yield of the $i^{th}$ bonding step, and $Y_{TSV(i)}$ is the TSV yield in the $i^{th}$ layer. In our work, we focus on the yield enhancement of 3D chip in terms of TSV yield $Y_{TSV}$ [13]. The total TSV yield $Y_{TSV}$ is calculated by multiplying all f-TSV group yield $Y_{gj}$ as follows.

$$ Y_{TSV} = \prod_{j=1}^{N} Y_{gj}, \tag{3} $$

where $N$ is the number of f-TSV groups. In this paper we adopt the algorithm described in [13] for the calculation of group yield $Y_{gj}$.

B. TSV Fault-Tolerance Structure

By inserting the multiplexers (including control circuits) and carefully designing the reconfigurable TSV replacing paths, we can construct TSV fault-tolerance structures, where the s-TSVs can be used to transfer signals in the presence of faulty f-TSVs [5].

Given an f-TSV planning result, we know the number and positions of all f-TSVs. Then we perform a top-down iterative f-TSV partitioning to form f-TSVs groups and allocate s-TSVs in the whitespace for each group. The number and positions of used s-TSVs for each f-TSV group are determined simultaneously in the f-TSV partitioning stage. Fig. 1(a) shows an example of a TSV group with four f-TSVs ($f_1 \cdots f_4$) and two s-TSVs ($s_1$ and $s_2$). Here $f_1 \cdots f_4$ belong to nets $nt_1 \cdots nt_4$, respectively. The dashed large rectangles represent the bounding boxes of different nets. Without loss of generality, we denote the bounding box of an f-TSV $f_i$ as the bounding box of the net $f_i$ belonging to. We say that an f-TSV $f_i$ can be replaced by another TSV $v$, if and only if $v$ is located inside or nearby the bounding box of $f_i$. Note that here the TSV $v$ can be either f-TSV or s-TSV. For example,
Given a TSV group with some f-TSVs and $K$ s-TSVs, a $K$-fault tolerance structure includes $K$ independent directed TSV-replacing paths from each f-TSV to s-TSVs. In this structure we can repair at most $K$ faulty f-TSVs through multiplexer rerouting. For instance, for the TSV group shown in Fig. 1(a), a 2-fault tolerance structure with two s-TSVs can be generated as in Fig. 1(b), where each f-TSV is directly connected to all s-TSVs. Although the design scheme is very simple, this structure suffers from large delay overhead due to large multiplexer input size. Some recent works [13], [14] proposed regular $K$-fault tolerance structure, as shown in Fig. 1(c). Here each f-TSV is regularly connected to two right side neighbouring TSVs and the rightmost f-TSVs are connected to s-TSVs. Instead of 4-port multiplexers occupied in Fig. 1(b), here only 3-port multiplexers and 2-port multiplexers are needed. For each f-TSV, the independent TSV-replacing paths are listed as follows.

$$f_1: \{f_1 \rightarrow s_1\}, \{f_1 \rightarrow f_2 \rightarrow f_3 \rightarrow f_4 \rightarrow s_2\}.$$  
$$f_2: \{f_2 \rightarrow f_5 \rightarrow f_6 \rightarrow f_7 \rightarrow f_8 \rightarrow s_2\}.$$  
$$f_3: \{f_3 \rightarrow s_1\}, \{f_3 \rightarrow f_4 \rightarrow s_2\}.$$  
$$f_4: \{f_4 \rightarrow s_1\}, \{f_4 \rightarrow s_2\}.$$  

To ensure the existence of fault-tolerance structures in TSV groups, the previous works (e.g. [13], [14]) form TSV groups under two constraints: (1) $K$ fault-tolerance structures use exactly $K$ s-TSVs and (2) an f-TSV in a group can be replaced by any s-TSV within the group. Fig. 1(a) shows an example of TSV group having two-fault tolerance structures, where all the f-TSVs, $f_1$, $f_2$, $f_3$, and $f_4$, can be replaced by both $s_1$ and $s_2$ considering the net bounding boxes. Unfortunately, general cases may violate these constraints. Fig. 2(a) shows a generalized example, where five f-TSVs ($f_1 \cdots f_5$) and four s-TSVs ($s_1 \cdots s_4$) are involved. The replaceable relations between TSVs are shown in Fig. 3(a). In this TSV group, the constraint (1) is violated since we cannot find two-fault tolerance structures if only two s-TSVs are used. The constraint (2) is also violated even if the group is partitioned into smaller groups since $f_2$ have no replaceable s-TSVs. Consequently, the method in [13] cannot generate cost-effective fault-tolerance structures for this TSV group, because $f_2$ has no candidate s-TSVs. The ILP-based method in [14] cannot generate fault-tolerance structures for this TSV group since the number of tolerant faults is unknown. However, the f-TSV group definitively includes a two-fault tolerance structure as shown in Fig. 3(c), where three out of four s-TSVs are used in the fault-tolerance structure. The possible TSV replacing paths are as follows.

$$f_1: \{f_1 \rightarrow s_1\}, \{f_1 \rightarrow f_2 \rightarrow f_3 \rightarrow f_4 \rightarrow s_2\}.$$  
$$f_2: \{f_2 \rightarrow f_5 \rightarrow f_6 \rightarrow f_7 \rightarrow f_8 \rightarrow s_2\}.$$  
$$f_3: \{f_3 \rightarrow s_1\}, \{f_3 \rightarrow f_4 \rightarrow s_2\}.$$  
$$f_4: \{f_4 \rightarrow f_3 \rightarrow s_1\}, \{f_4 \rightarrow s_2\}.$$  
$$f_5: \{f_5 \rightarrow f_1 \rightarrow s_1\}, \{f_5 \rightarrow s_3\}.$$  

In reality, there is no essential difference between the f-TSVs and s-TSVs. Therefore, the existing TSV testing technique can be directly adopted to test the f-TSVs and s-TSVs [16]. And the control signal of multiplexers can be set to determine the direction of signal transfer. As shown in Fig. 2(b), the control signal of 2-to-1 and 3-to-1 multiplexer are 1-bit and 2-bit, respectively. When all TSVs are fault-free or existing faulty s-TSVs, the control signals of each multiplexer are set to transfer signal through their corresponding f-TSVs. But once an f-TSV is faulty, the reconfigurable routing paths can be determined by the corresponding control signal of multiplexers. For instance, when f-TSV 1 is faulty, the control signals of multiplexer 6 and 7 are set to 0 and 10, causing s-TSV 1 to reroute the signal $A$.

**C. Hardware Cost and Multiplexer Delay Overhead**

The hardware cost incurred by the fault-tolerance structure can be divided into several parts, including the area overhead due to inserted s-TSVs, related control logic (i.e., MUXes), and re-routing interconnect [13]. And the cost is dominated by the first two parts [12]. Jiang et al. [17] point out that the area of control logic is negligible compared with the TSV size and the TSV manufacturing cost is much larger than logic gates. Therefore, in order to reduce the hardware cost,
Fig. 3: (a) The corresponding directed graph $G$ of layout in Fig. 2(a); (b) The corresponding splitting graph $G'$; (c) 2-fault tolerance structure on graph $G$.

we should reduce the number of s-TSVs used in the fault-tolerance structures.

The delay of a multiplexer is increased along with the number of ports. Therefore, a large multiplexer will introduce large delay overhead. Moreover, the proposed TSV fault tolerance planning is performed in floorplanning stage and we have no exact timing information. If we minimize the multiplexer delay overhead in this stage, we could alleviate the timing closure issue in next placement and routing stage. Therefore, in our work, we consider the multiplexer delay overhead as one of the optimization objectives.

D. Problem Formulation

From the example in Fig. 2, we can see that we confront new design challenging if not all s-TSVs can be occupied in constructing $K$-fault tolerance structure. Given a TSV group with $m$ f-TSVs and $n$ s-TSVs, we first construct a directed graph $G(V, E)$ consisting of all TSV replaceable relations. Here vertex set $V = V_1 \cup V_2$, where $V_1 = \{f_i | i = 1, \ldots, m\}$ is the f-TSVs set and $V_2 = \{s_i | i = 1, \ldots, n\}$ is the s-TSVs set. Besides, the edge set $E = \{(u, v) | u \in V_1 \land v \in V_2 \land u$ can be replaced by $v\}$. Given the TSV group in Fig. 2(a), the corresponding replaceable relation graph is shown in Fig. 3(a).

We define the problem of TSV fault-tolerance structure generation as follows.

Problem 1. Given a TSV group with $m$ f-TSVs and $n$ s-TSVs, and the directed graph $G(V, E)$, we search for the maximum number of tolerant faults $K$. Then we generate a $K$-fault tolerance structure, which includes $K$ independent TSV replacing paths (vertex-disjoint) for each f-TSVs, to minimize both the multiplexer delay overhead and the number of used s-TSVs.

Notice that the yield of the TSV group is evaluated based on the allocated s-TSVs and the f-TSVs. With the yields of the TSV groups, the total TSV yield can be calculated as discussed in Section II-A. If the target TSV yield is not satisfied, a TSV group will be selected and partitioned into two smaller new TSV groups, where the above TSV fault-tolerance structure generation problem will be solved again. New TSV groups will be iteratively generated until the target chip yield is satisfied.

III. MAX FLOW BASED METHODOLOGY

Given a TSV group with replaceable relation graph $G$, we say the TSV group has a $K$-fault tolerance structure if each f-TSV $f \in V_1$ has $K$ paths to s-TSV vertices in $G$. Besides, for each f-TSV $f$, the paths are vertex-disjoint except the $f$ itself. In this section, we develop a polynomial time algorithm to determine the $K$ value in a TSV group. Our methodology is based on the Menger’s theorem as follows.

Lemma 1 (Menger’s theorem [18]). Let $G$ be a directed graph, and let $S$ and $T$ be distinct vertices in $G$. Then the maximum number of vertex-disjoint $S$-$T$ paths is equal to the minimum size of an $S$-$T$ disconnecting vertex set.

Here the $S$-$T$ disconnecting vertex set represents a vertex set whose removal will cause no paths from any vertex in $S$ to any vertex in $T$. According to Lemma 1, for each f-TSV $f$, the number of vertex-disjoint paths $Nd(f)$ equals to the minimum size of the $\{f\}$-$V_2$ disconnecting vertex set in $G$. For example, in Fig. 3(a), $\{f_2, s_1\}$ is a minimum $\{f_1\}$-$V_2$ disconnecting vertex set. Therefore, the number of vertex-disjoint paths, $Nd(f_1)$, equals to 2. Based on above lemma, we reach the following theorem:

Theorem 1. Given the replaceable relation graph, the maximum number of tolerant faults, $K$, can be determined in polynomial time, as follows:

$$K = \min_{f \in V_1} \{Nd(f)\}. \quad (4)$$

Since vertex-disjoint problem is not easy to model, we perform vertex splitting on $G(V, E)$ so that it can be transformed to an edge-disjoint problem, which can be appropriately modelled in a maximum flow problem. Each vertex $u \in V$ is split into two vertices $u$ and $u'$, respectively, corresponding to the vertex’s input and output, and an extra edge $(u, u')$ with zero cost is also added. A new directed graph $G'(V', E')$ is constructed as follows.

- The vertex set $V' = V \cup V_1' \cup V_2'$, where $V_1'$ is the split vertex set of $V_1$ and $V_2'$ is the split vertex set of $V_2$.
- The edge set $E' = E_1' \cup E_2'$, where $E_1' = \{(u, u') | u \in V \land u' \text{ is the corresponding split vertex of } u\}$ and $E_2' = \{(u', v) | (u, v) \in E(G) \land u' \text{ is the corresponding split vertex of } u\}$. If there is a directed edge from $u$ to $v$ in $E(G)$, a corresponding directed edge from $u'$ to $v$ is added in $E'(G')$. 

Based on the splitting graph, the maximum number of tolerant faults $K$ can be determined in polynomial time by solving a max-flow problem [18] for each f-TSV. For instance, given the replaceable graph $G(V, E)$ in Fig. 3(a). Fig. 3(b) illustrates the splitting graph $G'(V', E')$. The number of edge-disjoint paths for each f-TSV are as follows, $N d(f_1) = 2$, $N d(f_2) = 2$, $N d(f_3) = 3$, $N d(f_4) = 3$ and $N d(f_5) = 3$. Since $f_1$ and $f_2$ have only two edge-disjoint paths, the maximum number of tolerant faults, $K$, equals to 2.

The fault-tolerance structure can be generated by finding $m \times K$ paths, which begin with each split f-TSV in $V'_1$ and end with split s-TSV in $V'_2$. In addition, all the paths sharing one same source vertex should be edge-disjoint. In the next two sections, we will propose an ILP based algorithm and a min-cost max-flow based heuristic method to generate the $K$-fault tolerance structure in minimizing both the used s-TSV number and the multiplexer delay overhead.

IV. INTEGER LINEAR PROGRAMMING FORMULATION

In this section, we discuss how the $K$ edge-disjoint path search problem can be formulated as an integer programming. For convenience, some notations used in this section are listed in TABLE I.

First, an integer programming formulation in [14] is given to generate the fault-tolerance structures with minimization of the multiplexer delay overhead.

To model the delay of each multiplexer, it is of importance calculating indegree of each vertex $u \in V$. As shown in Fig. 3(b), the edge $(f'_2, f_3)$ is on the path from $f'_1$ to $s'_2$, as well as the path from $f'_2$ to $s'_2$. Although the same edge is traversed by two paths, it only increases the indegree of $f_3$ by one. Meanwhile, there may be several edges directed into same TSV vertex on the paths. For instance, due to edges $(f'_2, f_3)$ and $(f'_4, f_3)$, the indegree of $f_3$ should be increased by two. Given a vertex $u \in V$, its indegree is calculated by the following equation:

\[
\text{indegree}(u) = \sum_{v \in \{(u,v) \in \mathcal{E}^r\}} \min\left(\sum_{s \in V'_1, t \in V'_2} x^{(s,t)}_{v*u}, 1\right).
\]  

(5)

The starting integer programming formulation of fault-tolerance structure generation problem in [14] is shown in Formula (6). The objective function in Formula (6) is to minimize the maximum indegree of all the vertices. The number of binary variables $x^{(s,t)}_{v*u}$ is $m \times n \times |E'|$, where $m$ is the number of f-TSVs, $n$ is the number of s-TSVs, while $|E'|$ is the number of edges in split directed graph $G'$. The constraint (6a) defines a unit flow from $s \in V'_1$ to $t \in V'_2$, which corresponds a path from $s$, an f-TSV, to $t$, an s-TSV. The number of this set of constraints is $m \times n \times |V'|$. The constraint (6b) ensures that a set of $V'_2$ paths, which have the same source $s \in V'_1$, are edge-disjoint. The number of this set of constraints is $m \times (m + n)$.

\[
\min \max_{u \in V} \text{indegree}(u) \quad \text{s.t.} \quad \sum_{v \in \{(u,v) \in \mathcal{E}^r\}} x^{(s,t)}_{v*u} = \begin{cases} 1, & \text{if } u = s, \\ 0, & \text{if } u \in V' - \{s, t\}, \forall s \in V'_1, t \in V'_2, \\ -1, & \text{if } u = t; \end{cases}
\]

\[\sum_{t \in V'_2} x^{(s,t)}_{u*t} \leq 1, \forall s \in V'_1, (u, u') \in E'_1, \quad (6b)\]

\[x^{(s,t)}_{v*u} \in \{0, 1\}, \forall (v, u) \in \mathcal{E'}', s \in V'_1, t \in V'_2. \quad (6c)\]

Though the integer programming method in [14] can generate $K$ fault-tolerance structures using $K$ s-TSVs, the method cannot be directly applied for the generation of adaptive fault-tolerance structures, where the number of s-TSVs might be larger than $K$ in $K$ fault-tolerance structures. Then a new integer programming formulation is proposed to generate adaptive fault-tolerance structures in minimizing both the used s-TSV number and the multiplexer delay overhead. The number of s-TSVs used in the structure can be calculated by the Equation (7).

\[
\text{usedstsv} = \sum_{w \in V'_2} \min(\sum_{s \in V'_1, t \in V'_2} x^{(s,t)}_{w*u}, 1).
\]  

(7)

Based on the above notations, the edge-disjoint path search problem can be formulated as the following integer programming (8).

Compared with the integer programming (6), in constraint (8a) a new binary variable $u^{(s,t)}$ is introduced to indicate whether a unit flow (path) exists from source $s \in V'_1$ to sink $t \in V'_2$. Besides, a new constraint (8b) is defined to ensure that there will be $K$ paths from each source $s \in V'_1$ to vertices in $V'_2$. The number of this set of constraints is $m$. By this way, Formula (8) can be applied for any $K \leq n$ and additionally minimize the number of required s-TSVs in the structure, while Formula (6) can only be applied for the case $K = n$.  

TABLE I: Notations used in ILP.

| $V', V''$ | set of f-TSVs and s-TSVs, set of split f-TSVs and split s-TSVs |
|-----------|---------------------------------------------------------------|
| $V_1, V'_1$ | set of f-TSVs, set of split f-TSVs |
| $V_2, V'_2$ | set of s-TSVs, set of split s-TSVs |
| $f_1, f'_1$ | f-TSV in $V_1$, split f-TSV in $V'_1$ |
| $s_1, s'_1$ | s-TSV in $V_2$, split s-TSV in $V'_2$ |
| $E'$ | set of all edges in graph $G'$ |
| $E'_1$ | set of all splitting edges in graph $G'$ ($f_1 \rightarrow f'_1$ and $s_1 \rightarrow s'_1$) |
| $E'_2$ | set of all replaceable edges in graph $G'$ |
| $(u, u')$ | edge in $E'_1$ and $u \in V_2$ |
| $s, t$ | split f-TSV in $V'_1$, split s-TSV in $V'_2$ |
| $v(s,t)$ | binary variable; if a unit flow (path) exists from $s$ to $t$ then $v(s,t) = 1$, otherwise $v(s,t) = 0$ |
| $(v, u)$ | edge in $E'$ |
| $x^{(s,t)}_{v*u}$ | binary variable; if a unit flow (path) from $s$ to $t$ goes through edge $(v, u)$, then $x^{(s,t)}_{v*u} = 1$, otherwise $x^{(s,t)}_{v*u} = 0$ |
| $d_{uv}$ | binary variable on edge $(v, u)$; if a unit flow (path) goes through edge $(v, u)$, then $d_{uv} = 1$, otherwise $d_{uv} = 0$ |
min \left\{ \max \text{ indegree}(u) + \text{ usedstv} \right\} \quad (8)
\text{s.t.} \quad \sum_{v:(v,u)\in E'} x_{vu}^{(s,t)} - \sum_{v:(u,v)\in E'} x_{vu}^{(s,t)} = \\
\begin{cases} g(v,s,t), & \text{if } u = s, \\
0, & \text{if } u \in V' - \{s, t\}, \forall s \in V'_1, t \in V'_2, \\
-g(v,s,t), & \text{if } u = t; \\
\end{cases} \\
\quad \sum_{t\in V'_2} y(t,s) = K, \quad \forall s \in V'_1. \quad (8a)
\quad y(t,s) \in \{0, 1\}, \quad \forall s \in V'_1, t \in V'_2, \\
(6b) - (6c). \tag{8b}

Formula (8) is non-linear due to the min-max-min and min-min operations in the objective function. Through linearizing the objective function, Formula (8) can be transformed into an integer linear programming (ILP) Formula (9). For each edge \((v, u) \in E'\), an extra binary variable \(d_{vu}\) and extra constraints (9a)-(9c) are introduced to replace the min operation in Formula (5) and (7). Besides, the extra constraint (9d) ensures that the indegrees of all TSVs will not be greater than \(\lambda_1\). Another extra constraint (9e) ensures that the number of s-TSVs used in the structure equals to \(\lambda_2\).

\begin{align*}
\min & \quad (\lambda_1 + \lambda_2) \quad (9) \\
\text{s.t.} & \quad d_{vu} \geq x_{vu}^{(s,t)}, \quad \forall s \in V'_1, t \in V'_2, (v, u) \in E', \\
& \quad d_{vu} \leq \sum_{s\in V'_1; t\in V'_2} x_{vu}^{(s,t)}, \quad \forall (v, u) \in E', \quad (9a) \\
& \quad d_{vu} \in \{0, 1\}, \quad \forall (v, u) \in E', \quad (9b) \\
& \quad \sum_{v:(v,u)\in E'} d_{vu} \leq \lambda_1, \quad \forall u \in V, \quad (9c) \\
& \quad \sum_{(w,w')\in E'_1} d_{ww'} = \lambda_2, \quad \forall w \in V_2, \quad (9d) \\
& \quad (6b) - (6c), (8a) - (8c). \tag{9e}
\end{align*}

For instance, as shown in Fig. 3(b), the blue lines present edge-disjoint paths for each split f-TSV, and the corresponding generated 2 fault-tolerance structure is shown in Fig. 2(b).

V. HEURISTIC FRAMEWORK

For large TSV groups, the ILP based method is very time consuming. Consequently, in this section, we propose a min-cost-max-flow (MCMF) based heuristic method to solve the edge-disjoint path problem. The basic idea is to deal with the f-TSVs one by one and, for each f-TSV, a min-cost-max-flow algorithm is used to find \(K\) independent paths. The edge costs are defined to keep the input port number of multiplexer and the number of s-TSVs as small as possible.

A. Network graph model

In order to find \(K\) \((K \leq n)\) edge-disjoint paths for an f-TSV \(f \in V_1\), we construct a directed graph \(G_a(V_s, E_s)\) from \(G'\) by adding an extra sink vertex \(t\) and some edges. The vertex set \(V_s\) contains two portions, \(V_s = V' \cup \{r\}\), and \(r\) is the sink vertex. The edge set \(E_s = E' \cup \{(V'_2 \to r)\}\).

When finding edge-disjoint paths for a certain TSV \(f_i \in V_1\), the edge capacities are defined as follows: the capacity of the edge from \(f_i\) to its splitting vertex \(f'_i\) equals to \(K\); while the capacities of all the other edges are set to 1. The capacity constraints ensure that we can find up to \(K\) edge-disjoint paths from \(f'_i\) to s-TSV vertices, which correspond to \(K\) independent TSV-replacing chains for the TSV \(f_i\).

For the splitting edges corresponding to f-TSVs, the edge costs are defined as zero while the splitting edges of s-TSVs are defined as follows.

\begin{align*}
ec_s(w, w') &= \begin{cases} 0, & \text{if } (w, w') \in E'_1, w \in V_2, \text{ and } w \text{ has been used}. \\
C^K, & \text{if } (w, w') \in E'_1, w \in V_2, \text{ and } w \text{ has not been used}. \\
\end{cases} \\
C & \text{ is constant, which represents the costs of introducing a new s-TSV for constructing the fault-tolerance structure.} \\
\end{align*}

And the edge costs tend to restrict the use of s-TSVs. In the experiment, we set \(C\) to 3 by the experimental results shown in Section VII-A.

For the edges in \(E'_2\), which correspond to the replaceable relations between TSVs, the edge costs are defined as follows.

\begin{align*}
ec_u(v, u) &= \begin{cases} 0, & \text{if } (u, v) \in E'_2 \text{ and } (u, v) \text{ corresponds to a TSV connection} \\
C^{tc[v]}, & \text{if } (u, v) \in E'_2 \text{ and } (u, v) \text{ does not correspond to a TSV connection} \\
\end{cases} \\
\text{In the edge cost function (11), } tc[v] \text{ is defined to be the number of edges that end at } v \text{ and have been used as TSV connections in the generated partial fault-tolerance structure, that is, the edges that have been traversed by edge-disjoint paths of some other f-TSVs. Therefore, } tc[v] \text{ corresponds to the input port number of the multiplexer in the input side of the TSV } v. \\
\text{With this edge costs function, firstly, we tend to make full use of existing TSV connections to build the edge-disjoint paths for the current f-TSV since it will not increase the input ports of the multiplexers.} \\
\text{Secondly, to minimize the maximum size of multiplexers, the costs of the edges that do not correspond to TSV connections are defined as the exponential function of } tc[v]. \\
\end{align*}

B. Algorithmic flow of heuristic

The algorithmic flow of the proposed heuristic is summarized in Algorithm 1. Because the quality of solution depends on the order of f-TSVs selected, an iterative post-processing stage is used to improve the generated fault-tolerance structures. In the post-processing stage, we randomly select an f-TSV, and define the edge costs based on the TSV paths of all the other f-TSVs. Then we re-solve the min-cost-max-flow model to find edge-disjoint paths for the selected f-TSV.
The input side of the TSV can find two edge-disjoint paths from the input to s-TSVs by making use of the existing TSV connections as many as possible, which potentially reduces the TSV connections on individual TSVs and minimizes the maximum number of the input ports of multiplexers. The bottom part of Fig. 4(b) shows the TSV connections in the updated partial fault-tolerance structure.

Repeating the same process until the min-cost-max-flow model is solved for all f-TSVs, we obtain 2 edge-disjoint paths from each split f-TSV vertex in \( V'_f \), \( f'_1 \cdots f'_9 \), to split s-TSV vertices in \( V'_s, s'_1 \cdots s'_9 \), as shown in Fig. 5. Here the solid edges are TSV connections.

Algorithm 1 Pseudo code of our heuristic method

**Input:** A directed graph \( G'(V', E') \), which contains \( m \) f-TSVs and \( n \) s-TSVs.

**Output:** A repairable structure including \( m \times K \) paths.

1: for f-TSV \( f_i \leftarrow 1 \) to \( m \) do
2: Construct a directed graph \( G_s(V_s, E_s) \) for \( f_i \);
3: \( \triangleright \) Find \( K \) edge-disjoint paths for \( f_i \);
4: Solve the MCMF model for \( f_i \);
5: end for
6: \( \triangleright \) Perturb the repairable structure;
7: while no coverage do
8: Randomly select an f-TSV \( f_i \);
9: Resolve edge-disjoint paths for \( f_i \) by MCMF;
10: Record the maximum number of TSV connections on all TSVs;
11: end while

Fig. 4: Label on edges represents (capacity, cost): (a) The min-cost-max-flow network for f-TSV \( f'_1 \), where the two edge-disjoint paths for \( f'_1: \{ f'_1 \rightarrow s_1 \rightarrow s'_1 \} \) and \( \{ f'_1 \rightarrow f_2 \rightarrow f_3 \rightarrow s_2 \rightarrow s'_2 \} \); (b) After solving \( f'_1 \), the min-cost-max-flow network for f-TSV \( f'_2 \), where the two edge-disjoint paths for \( f'_2: \{ f'_2 \rightarrow f_5 \rightarrow f'_3 \rightarrow f_1 \rightarrow s'_1 \rightarrow s_1 \} \) and \( \{ f'_2 \rightarrow f_3 \rightarrow f'_3 \rightarrow s_2 \rightarrow s'_2 \} \); (c) After solving \( f'_1 \) and \( f'_2 \), the min-cost-max-flow network for f-TSV \( f'_3 \), where the two edge-disjoint paths for \( f'_3: \{ f'_3 \rightarrow s_1 \rightarrow s'_1 \} \) and \( \{ f'_3 \rightarrow s_2 \rightarrow s'_2 \} \).

Fig. 5: The generated 2-fault tolerance structure by solving edge-disjoint paths for all f-TSVs, where the TSV connections are shown in solid edges.

The iteration number.

In this section, we discuss a top-down fault tolerance TSV planning framework to form f-TSV groups and generate adaptive fault-tolerance structures. The number of f-TSV groups is greatly reduced as well as the total number of s-TSVs because of adaptive fault-tolerance structures.

Given an f-TSV planning result and the floorplan of the blocks, we know the number and positions of all f-TSVs. Then f-TSV groups are firstly formed using a top-down iterative f-TSV partitioning under the yield constraint and, then, the adaptive fault-tolerance structures are generated for each group. In each iteration of the f-TSV partitioning stage, the group with the smallest yield will be partitioned into two new f-TSV groups using the min-cut bi-partitioning algorithm and the required s-TSVs are also allocated for evaluating the group yield. The iterative f-TSVs partitioning is repeated until the target chip yield is satisfied. Therefore, the number and position of required s-TSVs for each f-TSV group are determined simultaneously in the f-TSV partitioning stage.

The chip yield is the product of group yield, which depends on the maximum number of tolerant faults ($K$), the number of TSVs, and the defect probability of TSVs as discussed in Section II-A. We construct the replaceable relation graph $G$, whose vertex set includes the f-TSVs in the group and the corresponding candidate s-TSVs, for computing $K$ and allocating s-TSVs. The maximum number of tolerant faults, $K$, can be determined in polynomial time by solving a max-flow problem on $G$, as discussed in Section III. The min-cost-max-flow based heuristic in Section V is used to temporarily generate an adaptive fault-tolerance structure, thus the number of required s-TSVs are determined.

Finally, the ILP based method in Section IV and the min-cost-max-flow (MCMF) based heuristic in Section V can be adopted to generate adaptive fault-tolerance structures with minimization of both the multiplexer delay overhead and the hardware cost. Fig. 6 illustrates the proposed TSV planning framework.

In [13], a greedy method is used to partition f-TSVs into groups and then an ILP formulation is adopted to allocate s-TSVs for each group. The generation of fault-tolerance structure is not considered since they assume regular structures always exist. In [14], the TSV planning framework includes a top-down partitioning followed by a bottom-up iterative merging (clustering) for reducing the number of f-TSV groups. Then, a min-cost-max-flow based method is used to allocate s-TSVs for each group and an ILP model is adopted to generate fault-tolerance structures. The same number of s-TSVs are allocated to all the f-TSV groups in [13], [14] and, for an f-TSV group, the key point is to ensure enough number of candidate s-TSVs that can be shared by all the f-TSVs in the group. As a result, many small f-TSV groups are formed, which potentially causes an overuse of s-TSVs.

Compared with the above mentioned two works, the proposed TSV planning framework includes a similar top-down partitioning stage, but the allocation of s-TSVs during the partitioning is very different. That is because adaptive fault-tolerance structures with various number of s-TSVs are built temporarily by solving a sequence of min-cost max-flow problem.

The proposed algorithms have been implemented in C++ language and tested on a 12-core 2.0 GHz Linux server with 64 GB RAM. The TSV pitch is assumed to be $5\mu m \times 5\mu m$ [3]. LEDA [19] is adopted to solve the max-flow and the min-cost-max-flow problems. GLPK [20] is used as the ILP solver. hMetis [21] is adopted on f-TSVs partitioning.

A. Effectiveness and Efficiency of Fault-Tolerance Structure Generation Method

We generate several TSV replaceable relation graphs $G_{11}$–$G_{18}$ by using the proposed TSV planning framework on MCNC and GSRC benchmarks. Each graph contains f-TSVs and the corresponding candidate s-TSVs, which are covered by at least one of the bounding boxes of the f-TSVs. In order to compare the proposed ILP model with the ILP method in [14] on $G_{11}$–$G_{18}$, we adapt the ILP formulation in [14] here. To generate the $K$-fault tolerance structure on a TSV replaceable relation graph $G$, we select $K$ s-TSVs in all $n$ s-TSVs, and unit flow constraints are defined from all f-TSVs to those chosen $K$ s-TSVs. If the $K$-fault tolerance structure is still not achieved after solving all $K$ combinations, we think the ILP method in [14] cannot generate the $K$-fault tolerance structure on this TSV replaceable relation graph $G$.

In addition, the previous work in [14] deals with a special type of TSV fault-tolerance structure generation. That is, they are under an assumption that a predetermined number of s-TSVs are assigned to each TSV group, and an f-TSV in a group should be replaced by any s-TSV within the group. We also generate some specific TSV replaceable relation graphs $G_{21}$–$G_{28}$ by using the TSV planning methods in [14] on MCNC and GSRC benchmarks. Since the f-TSVs can be replaced by all $n$ s-TSVs in each graph, the $n$-fault tolerance structure always exists.

First, we show the effectiveness of the proposed ILP model. TABLE II shows the experimental results, where “ILP” and “Heuristic” denote results of the proposed ILP model.
and min-cost-max-flow based heuristic method, respectively. Columns “m”, “n”, “#Edges”, and “K” list the number of f-TSVs, the total number of available s-TSVs, the number of edges, and the number of maximumly tolerant faults on each TSV replaceable relation graph. Besides, columns “#Port” and “#us” show the maximum port number of multiplexers and the number of s-TSVs used in the generated fault-tolerance structure. “IWire” shows the sum of incremental half-perimeter wirelength overhead of all f-TSVs incurred by the fault-tolerance structure, and the ratio of “IWire” to the sum of net wirelength of all f-TSVs is listed in “ratio”. “RT” reports the total computational time in seconds. “NA” represents that the K-fault tolerance structure cannot be achieved within the time limit (3600s). As shown in TABLE II, the ILP method in [14] generates the fault-tolerance structure only on two smallest graphs. However, the proposed ILP formulation can achieve the fault-tolerance structure on six graphs.

Second, we show the efficiency of the proposed heuristic method. TABLE II also compares the proposed heuristic method with the proposed ILP method. It can be noticed that, on small graphs $G_{11}$–$G_{16}$ and $G_{21}$–$G_{24}$, the fault-tolerance structure generated by ILP has smaller maximum port number of multiplexers and used less s-TSV numbers than that generated by the heuristic method. Therefore, for small TSV replaceable relation graphs, ILP can achieve an optimal solution, which can be used to verify the accuracy of the solution of the heuristic method. But since ILP is an NP-hard problem, its runtime increases dramatically with the size of TSV replaceable relation graphs. As shown in TABLE II, the ILP method cannot generate the fault-tolerance structure on large graphs $G_{17}$–$G_{18}$ and $G_{25}$–$G_{28}$ within the time limit (3600s). Therefore, for large TSV replaceable relation graphs, the ILP based method is very time consuming, which can indirectly demonstrate the efficiency of the proposed heuristic method.

In addition, the parameter $C$ in edge cost functions (10) and (11) is also set through experimental results. The experiment is performed on MCNC and GSRC benchmarks. In the experiment, if $C$ is set to 4, some edge cost values are out of bound, which cannot be solved by min-cost-max-flow based model. And we also set $C$ to 2 and 3, the number of used s-TSVs and maximum port number of multiplexers varied with $C$, which is shown in TABLE III. Columns “#s-TSV” and “#Port” list the total number of allocated s-TSVs and the maximum port number of multiplexers among all f-TSV groups. We noticed that compared with $C = 2$, $C = 3$ can achieve a fault tolerance structure with less number of used s-TSVs and smaller maximum port number of multiplexers. Therefore, in the experiment, we set $C$ to 3.

B. Comparison with Previous TSV Fault Tolerance Planning Work

We use simulated annealing-based multi-layer floorplanning [22] to generate the block floorplan and the f-TSV planning method in [14] to generate f-TSV planning result as the input to the proposed fault-tolerance TSV planning framework. Based on the same f-TSV planning result, we run the flow in [13], [14], and the proposed heuristic based framework, respectively. The experiment is tested on MCNC and GSRC benchmarks, including two MCNC circuits (ami33 and ami49), and four GSRC circuits (n50, n100, n200 and n300). We adopt one more industrial 2D design, which contains 403266 cells and 448514 nets. hMetis [21] is adopted to partition the design into several blocks for floorplanning. Based on different block numbers, two benchmark cases, $t_{337}$ and $t_{469}$, are generated. That is, $t_{337}$ has 337 blocks and 1836 nets, while $t_{469}$ has 469 blocks and 5479 nets. Since the square has the smallest perimeter among all the rectangles with the same area [23], here the shapes of all the

### TABLE II: Comparison between ILP [14] and our methods for generating adaptive fault-tolerance structure.

| Graph | m | n | #Edges | K  | ILP [14] | ILP | Heuristic |
|-------|---|---|--------|----|---------|-----|-----------|
|       | #Port | #us | IWire(um) | RT(s) | #Port | #us | IWire(um) | RT(s) |
| $G_{11}$ | 9 | 4 | 72 | 3 | 3 | 3 | 32.90 (0.51%) | 353.20 |
|       | 3 | 3 | 32.90 (0.51%) | 301.53 |
| $G_{12}$ | 13 | 4 | 129 | 2 | 3 | 3 | 6.85 (0.18%) | 603.68 |
|       | 3 | 2 | 9.65 (0.25%) | 67.80 |
| $G_{13}$ | 14 | 4 | 101 | 1 | NA | NA | $>$3600 |
|       | 2 | 4 | 29.77 (1.77%) | 1.09 |
| $G_{14}$ | 15 | 5 | 177 | 2 | NA | NA | $>$3600 |
|       | 3 | 4 | 32.50 (0.62%) | 96.90 |
| $G_{15}$ | 18 | 5 | 215 | 2 | NA | NA | $>$3600 |
|       | 3 | 4 | 65.20 (0.96%) | 240.07 |
| $G_{16}$ | 18 | 6 | 199 | 2 | NA | NA | $>$3600 |
|       | 3 | 6 | 90.03 (1.76%) | 155.74 |
| $G_{17}$ | 21 | 7 | 255 | 2 | NA | NA | $>$3600 |
|       | NA | NA | NA | $>$3600 |
| $G_{18}$ | 26 | 13 | 529 | 4 | NA | NA | $>$3600 |
|       | NA | NA | NA | $>$3600 |

### TABLE III: Effect of $C$ on s-TSV numbers and maximum port number of multiplexers.

| Benchmark | $C = 2$ | $C = 3$ |
|-----------|---------|---------|
|           | #s-TSV | #Port | #s-TSV | #Port |
| ami33     | 52 | 4 | 46 | 4 |
| ami49     | 80 | 6 | 66 | 6 |
| n50       | 108 | 7 | 98 | 7 |
| n100      | 181 | 8 | 169 | 7 |
| n200      | 267 | 7 | 250 | 7 |
| n300      | 395 | 8 | 381 | 6 |
TABLE IV: Comparisons among [13], [14], and the proposed adaptive fault-tolerance structure (AFTS) under 3-fault-tolerance structures (target yield = 99.7%, \( p = 0.001 \)).

| Bench | #f-TSV | #s-TSV | *H* | Yield | K | #f-TSV | #s-TSV | #H | #Port | K | Yield |
|-------|--------|--------|-----|-------|---|--------|--------|---|-------|---|-------|
| ami33 | 55     | 48     | 16  | 100%  | 48 16 4 3 | 100% | 31   | 2    | 3    | 3 | 100%  |
| ami49 | 130    | 72     | 24  | 100%  | 66 22 5 3 | 100% | 54   | 2    | 5    | 3 | 99.99% |
| n50   | 386    | 210    | 70  | 99.97%| 204 68 7 3 | 100% | 82   | 5    | 6    | 2 | 99.96% |
| n100  | 592    | 294    | 98  | 99.6% | 291 97 7 3 | 99.94%| 136  | 7    | 6    | 3 | 99.91% |
| n200  | 1127   | 396    | 132 | 99.86%| 393 131 6 3 | 99.86%| 179   | 8    | 5    | 3 | 99.85% |
| n300  | 1232   | 501    | 167 | 99.81%| 498 166 6 3 | 99.83%| 246   | 9    | 5    | 3 | 99.78% |
| t337  | 640    | 315    | 105 | 99.9% | 309 103 4 3 | 99.91%| 158   | 8    | 5    | 3 | 99.88% |
| t469  | 1546   | 600    | 200 | 99.71%| 588 196 6 3 | 99.73%| 313   | 11   | 6    | 3 | 99.71% |
| avg.  | 714    | 305    | 102 | 99.9% | 300 181 6 3 | 99.91%| 150   | 7    | 5    | 3 | 99.89% |

blocks are set to square. The experiment is executed 20 times independently for each benchmark.

In fault-tolerance structures, the multiplexers are used to reroute signals, and the delay of a multiplexer is increased along with the number of input ports. Besides the hardware cost incurred by the fault-tolerance structure is related to the number of s-TSVs. In this experiment, we compare the number of s-TSVs and the maximum port number of multiplexers of [13], [14], and the proposed TSV planning framework under 3-fault tolerance structures. The layer number is set to 3. The target chip yield is set to 99.7% and the TSV defect probability \( p \) is set to 0.001. The yield results in experiment and accurate to the fourth decimal place. 3 s-TSVs are assigned to each f-TSV group in [13], [14], that is, the maximum number of tolerant faults \( K \) equals to 3.

TABLE IV lists the statistic results averaged over 20 independent experiments. All results listed in table satisfy the target chip yield. Column “#f-TSV” represents the total number of f-TSVs. Since the three frameworks are run on the same f-TSV planning result, the number of f-TSVs is the same. Columns “#s-TSV”, “#gp”, and “Yield” list the total number of allocated s-TSVs, the number of groups, and the chip yield, respectively. Besides, column “#Port” provides the maximum port number of multiplexers among all groups, while column \( K \) gives the number of tolerant faults in that group, respectively. Since the generation of fault-tolerance structure is not considered in [13], the maximum port number of multiplexers is not listed. As shown in TABLE IV, the number of f-TSV groups is greatly reduced in the proposed method. Compared with [13] and [14], the proposed fault tolerance TSV planning framework can reduce the number of used s-TSVs by 32.79% and 31.67% on average, respectively. In addition, in the proposed framework, if the maximum \( K \) is used for each group, it will cause larger multiplexers. Because the maximum number of tolerant faults \( K \) in adaptive fault-tolerance structures is often much greater than that of [14], which is fixed at 3. As a result, the maximum port number of multiplexers is increased accordingly in the generated fault-tolerance structures.

To reduce the size of required multiplexers, we also run
the proposed fault tolerance TSV planning framework with $K \leq 3$, that is, we set $K$ to 3 if the maximum number of tolerant faults $K$ in a group is greater than 3. As shown in TABLE IV, compared with [14], the proposed fault tolerance TSV planning framework with $K \leq 3$ has comparable maximum port number of multiplexers. But the required s-TSVs are surprisingly reduced by 50% on average under the same target yield, as shown in TABLE IV.

The TSV defect probability $p$ in [12] ranges from 0.001 to 0.01. In order to see the impact of $p$ on performance, we also execute the experiment when $p$ is set to 0.01 under 3-fault tolerance structures. The layer number is set to 3. The target chip yield is set to 99.5%. TABLE V lists the statistic results averaged over 20 independent experiments. All results listed in table satisfy the target chip yield. Based on the same f-TSV planning result, we run the flow in [13], [14], and the proposed heuristic based framework, respectively. Compared with [13] and [14], the proposed fault tolerance TSV planning framework can reduce the number of used s-TSVs by 32.24% and 31.01% on average, respectively. In order to reduce the size of required multiplexers, we also run the proposed fault tolerance TSV planning framework with $K \leq 3$. As shown in TABLE V, compared with [14], the proposed fault tolerance TSV planning framework with $K \leq 3$ has comparable maximum port number of multiplexers. But the required s-TSVs are surprisingly reduced by 46.50% on average under the same target yield, as shown in TABLE V.

Besides, in [6], 1-fault tolerance structures are generated using minimum spanning tree based method. However, it is difficult to apply the method to the fault-tolerance structure using more than one spare TSVs. In addition, the delay overhead introduced by the multiplexers, which are used for rerouting signals in the generated fault-tolerance structures, is not considered. In the worst-case the input port number of a multiplexer could be the number of f-TSVs in the group if the tree is a star structure, which introduces large delay overhead. In this experiment, we consider 1-fault tolerance structures case, that is, the maximum number of tolerant faults $K$ equals to 1. Since the chip yield is lower under 1-fault tolerance structures, the target chip yield is set to 99.5% and the TSV defect probability $p$ is set to 0.001. And we compare [6], [13], [14], with the proposed heuristic based model under 1-fault tolerance structures. One s-TSV is assigned to each f-TSV group in [13] and [14]. And we also set $K$ to 1 in the proposed fault tolerance TSV planning framework, if the maximum number of tolerant faults $K$ in a group is greater than 1. Based on the TSV planning method in [14], we run the minimum spanning tree method in [6]. Therefore, the s-TSV numbers and chip yield of [6] and [14] are same in the experiment.

TABLE VI lists the statistic results averaged over 20 independent experiments. As shown in TABLE VI, compared with [6] and [14], the proposed fault tolerance TSV planning framework can reduce the number of s-TSVs and the maximum port number of multiplexers when generating 1-fault tolerance structures.

Fig. 7 shows the required s-TSV numbers under various target yields, in comparison among [13], [14], and our proposed framework. The experiment is performed on n100 benchmark. Each data point in the figure is an average of 20 independent experiments. It can be observed that the number of required s-TSVs increases along with increasing target yield and is significantly reduced by the proposed framework for all target chip yields.

VIII. CONCLUSION

In this paper, we focus on the generation of adaptive TSV fault-tolerance structure. An integer linear programming (ILP) based model and an efficient min-cost-max-flow based heuristic method are proposed to generate the adaptive fault-tolerance structures in minimizing both the multiplexer delay overhead and the used s-TSV number. In the end, a fault-tolerance TSV planning methodology is also proposed to provide yield awareness in TSV planning. Experimental results show that, compared with state-of-the-art, the proposed fault tolerance TSV planning methodology can effectively reduce the number of s-TSVs used for fault tolerance.

Besides, in this work, the proposed TSV fault tolerance planning is performed in floorplanning stage and we have no accurate timing information. Therefore, we only use the wirelength to reflect the wire delay in floorplanning stage. In future we plan to evaluate the delay more accurately by executing time-consuming routing.

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REFERENCES

[1] S. J. Souri, K. Banerjee, A. Mehrotra, and K. C. Saraswat, “Multiple Si layer ICs: Motivation, performance analysis, and design implications,” in ACM/IEEE Design Automation Conference (DAC), 2000, pp. 215–220.
[2] J. W. Joyner, P. Zarkesh-Ha, and J. D. Meindl, “A global interconnect design window for a three-dimensional system-on-a-chip,” in IEEE International Interconnect Technology Conference (IITC), Jun. 2001, pp. 154–156.
[3] “International technology roadmap for semiconductors,” [Online].http://www.itrs2.net.
[4] T. Lu, C. Seray, Z. Yang, S. K. Samal, S. K. Lim, and A. Srivastava, “TSV-Based 3-D ICs: Design Methods and Tools,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 36, no. 10, pp. 1593–1619, 2017.
[5] I. Loi, S. Mitra, T. H. Lee, S. Fujita, and L. Benini, “A low-overhead fault tolerance scheme for TSV-based 3D network on chip links,” in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2008, pp. 598–602.

[6] Y.-G. Chen, W.-Y. Wen, Y. Shi, W.-K. Hon, and S.-C. Chang, “Novel spare TSV deployment for 3-D ICs considering yield and timing constraints,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 4, pp. 577–588, 2015.

[7] Q. Xu, L. Jiang, H. Li, and B. Eklow, “Yield enhancement for 3D-stacked ICs: Recent advances and challenges,” in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Feb. 2012, pp. 731–737.

[8] H.-H. S. Lee and K. Chakrabarty, “Test challenges for 3D integrated circuits,” *IEEE Design & Test of Computers*, vol. 26, no. 5, pp. 26–35, 2009.

[9] C. Ferri, S. Reda, and R. I. Bahar, “Strategies for improving the parametric yield and profits of 3D ICs,” in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2007, pp. 220–226.

[10] C.-W. Chou, Y.-J. Huang, and J.-F. Li, “Yield-enhancement techniques for 3D random access memories,” in *International Symposium on VLSI Design, Automation, and Test (VLSI-DAT)*, Apr. 2010, pp. 104–107.

[11] L. Jiang, R. Ye, and Q. Xu, “Yield enhancement for 3D-stacked memory by redundancy sharing across dies,” in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2010, pp. 220–234.

[12] L. Jiang, Q. Xu, and B. Eklow, “On effective TSV repair for 3D-stacked ICs,” in *IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE)*, Mar. 2012, pp. 793–798.

[13] S. Wang, M. B. Tahoori, and K. Chakrabarty, “Defect clustering-aware spare-TSV allocation for 3D ICs,” in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2015, pp. 307–314.

[14] Q. Xu, S. Chen, X. Xu, and B. Yu, “Clustered fault tolerance TSV planning for 3D integrated circuits,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 8, pp. 1287–1300, 2017.

[15] Y. Chen, D. Niu, Y. Xie, and K. Chakrabarty, “Cost-effective integration of three-dimensional (3D) ICs emphasizing testing cost analysis,” in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2010, pp. 471–476.

[16] B. Noia and K. Chakrabarty, *Design-for-Test and Test Optimization Techniques for TSV-based 3D Stacked ICs*. Switzerland: Springer, 2014.

[17] L. Jiang, Q. Xu, and B. Eklow, “On effective through-silicon via repair for 3-D stacked ICs,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 4, pp. 559–571, 2013.

[18] A. Schrijver, *Combinatorial Optimization: Polyhedra and Efficiency*. Berlin: Springer Science & Business Media, 2002, vol. 24.

[19] K. Mehlhorn and S. Naher, *LEDa: A Platform for Combinatorial and Geometric Computing*. Cambridge University Press, 1999.

[20] A. Makhorin, “GLPK (GNU linear programming kit),” 2008.

[21] G. Karypis, R. Aggarwal, V. Kumar, and S. Shekhar, “Multilevel hypergraph partitioning: applications in VLSI domain,” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 7, no. 1, pp. 69–79, 1999.

[22] S. Chen and T. Yoshimura, “Multi-layer floorplanning for stacked ICs: Configuration number and fixed-outline constraints,” *Integration, the VLSI Journal*, vol. 43, no. 4, pp. 378–388, 2010.

[23] ——, “Fixed-outline floorplanning: Block-position enumeration and a new method for calculating area costs,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 27, no. 5, pp. 858–871, 2008.