Design of servo control system based on Nios soft core CPU

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Abstract. This paper presents a control scheme of AC servo motor based on NIOSII soft core CPU as System controller. The system uses FPGA as the core device, and in the Quartus II 10.0 Software Environment, the related control parts are designed to form an executable control system. The control signals from the control system are isolated and amplified, and output to the drive to realize the control of the AC servo motor. According to the characteristics of Nios soft core CPU, it is expounded from two aspects of hardware and software, which provides a solution for the design of servo control system.

1. Introduction
With the development of large-scale integrated circuit technology, especially the emergence of hardware description language, the application of FPGA (Field-Programmable Gate Array) devices in the field of control is becoming more and more widespread[1]. Nios embedded processor is a soft-core CPU developed by Altera, a manufacturer of FPGA. It is a user-oriented, flexible and customizable embedded processor. It integrates data bus, various peripherals (such as timer, SRAM, FLASH) and interfaces (such as UART, PIO, SPI, PWM, SDRAM interface) to combine the advantages of microprocessor with the exceptionally powerful parallel functions of PLD. In this paper, NiosII soft core CPU is used as the system controller to realize the control scheme of AC servo motor. Nios soft core CPU is used to process the information of servo system, PID algorithm is used to output the power driver, and SPI bus communication module is used to communicate with the host computer to complete the control of servo system.

2. System composition and working principle
The servo system is an important part of the control system. Its main function is to control the load displacement to track the instructions accurately. The servo control system is mainly composed of upper computer, servo controller, driver, AC motor and position detection device. The system structure is shown in figure 1. The position detection device provides the position to the servo controller. The position can be corrected the error and filtered by the servo controller. Combining with the position and speed instructions of the host computer, the speed instructions at the next moment are given by a specific control algorithm, and the command signals are provided to the driver. The instructions are integrated and converted to current by the driver to drive the motor. The servo controller is the direct emitter of motion control instructions, and is at the core of the servo system. The position detection of the system is output by coarse-fine dual-channel selsyn. The output is introduced into the selsyn-digital converter (SDC) module of servo controller to complete the conversion from analog signal to digital signal. Through the control program acquisition and control of the servo controller, the position signals with the specifications of -180°~ +180° are processed.
3. System composition and working principle

In the application of this system, the soft-core Nios processor is used as the core of the whole servo controller to realize the functions of command receiving and processing, error-correcting filtering of position signal, command output controlled by combination algorithm, and system motion state feedback. The hardware structure of the whole system is shown in figure 2.

- **Figure 1. The composition of servo control system**

- **Figure 2. Hardware circuit diagram of servo control module**

  The servo control module consists of the following parts:

  1) **Host Computer**

  2) **Servo controller**

  3) **Driver**

  4) **Servo Motor**

  5) **Executing Agency**

  6) **Position Detection**

  **Figure 2. Hardware circuit diagram of servo control module**

  The servo control module consists of the following parts:

  1) The core processor is EP1C12Q240, a Cyclone series of FPGA chips produced by Altera Company. It mainly completes the reception of digital input and error correction of the position detection module SDC module, receives the position and speed control instructions of the host computer, performs interpolation iteration, completes position and speed PID control, switching input and output control, and communicates with the host computer.

  2) **SDC module**, using dual-channel selsyn/resolver-digital converter M2S44RDC/SDC chip to complete position extraction and digital conversion.

  3) **SPI bus communication module**, which uses self-customized SPI bus module inside the FPGA to communicate with the host computer, to complete the information interaction with the host computer.

  4) **SRAM**: ISSI's high-speed asynchronous SRAM chip IS61LV25616AL with capacity of 256K*16Bit is adopted. Word Enabler signal is independent and can operate on each Byte.

  5) **SDRAM**: K4S32323232F of SAMSUNG company is adopted, and its capacity is 2M*32Bit.

  6) **FLASH**: AMD's Am29LV160D with a capacity of 1M*16Bit is adopted.

  7) **Bus control module**: The driver outputs the data bus signal. The bus control chip SN74LVCC3245 is used for bus control, which has the functions of direction control, signal isolation and amplification.

  8) **AS interface**: The EPCS device is programmed directly through AS interface.
9) JTAG interface: It can download the configuration to FPGA, debug program, program for Flash, and program for EPCS device.

4. System composition and working principle

4.1. Development flow of Nios soft core CPU
On the basis of system hardware design, a project is built in the development software Quartus II; a hardware system based on Nios soft core CPU is built by SOPC Builder; a hardware system based on Nios CPU is compiled and configuration files are generated in the Quartus II project; and establish application software program for hardware system in NiosII IDE development environment; compile executor to generate executable file; burn the execution file into the FPGA to debug and run the system.

4.2. System Module Interface Design

4.2.1. Design of SDC Module Interface. The SDC module used in this system is M2S44RDC/SDC chip to complete position extraction and digital conversion. The pin description of the chip is shown in Table 1. Among them, the control pins have digital output ports, an output enabling port and a channel selection port. The interface signals are shown in figure 3.

| Pin Number | SYMBOL | FUNCTION |
|------------|--------|----------|
| 1~7        | D8~D14 | Digital Output |
| 8          | /OE    | output enable |
| 9          | A/B    | channel selection |
| 10         | Bit    | error detection |
| 11         | Rlo(A) | A Channel Reference Input Lower End |
| 12         | Rhi(A) | A Channel Reference Input High-end |
| 13~16      | S4~S1(A) | A Channel Signal Input |
| 17~20      | S1~S4(B) | B Channel Signal Input |
| 21         | Rhi(B) | B Channel Reference Input High-end |
| 22         | Rlo(B) | B channel reference input low end |
| 23         | GND    | power GND |
| 24         | −Vs    | -15V Power Supply |
| 25         | +Vs    | +15V Power Supply |
| 26~32      | D1~D7  | digital output |

**Table 1. Pin Definition of M2S44RDC/SDC Chip**

![Table 1](image)

**Figure 3. SDC custom module signal interface**
4.2.2. Design of Driver Module Interface. The driver module used in this system is the AC driver of a company. The AC driver receives 16-digit digital signals and drives the AC servo motor through internal control. The driver's pin instructions are shown in Table 2. Among them, the control pins have digital output ports, an output enabling port and an address port. The interface signals are shown in figure 4.

| Pin Number | SYMBOL | FUNCTION          |
|------------|--------|-------------------|
| 1~16       | D0~D15 | Digital Output    |
| 17         | /OE    | output enable     |
| 18         | Address| Address selection |

Figure 4. Driver custom module signal interface

4.3. System SOPC Integrated Design
On the basis of hardware design, SOPC integration design is carried out. The SOPC integrated design of the system is described as: constructing Nios CPU under SOPC Builder environment; adding 10ms timer from the library to complete the system timer interruption control; adding on-chip memory; combining the designed hardware, adding external memory SDRAM; adding self-customized SDC interface controller; adding serial SPI communication controller to complete information exchange with host computer; adding self-customized driver interface controller; adding I/O interface control logic and so on; composing a complete system. Finally, SOPC system files are compiled and generated in SOPC Builder. After integrating the system into Quartus II 10.0 project, pins are allocated and compiled and downloaded to the FPGA chip. The whole SOPC system is developed. Figure 5 shows the Nios CPU controller generated by the system. Figure 6 is the top-level file diagram of the system after pins are allocated.
5. System composition and working principle

After the construction of SOPC hardware system, a user software development kit (SDK) is generated in the development environment. SDK defines the software view of user hardware, including memory mapping and access to the data structure of hardware module in the system. On the basis of hardware construction, software design is established and application program development is carried out. The application software is developed under NiosII IDE environment. The main functions of the system software are: after receiving the control instructions and parameters of the host computer through SPI communication bus, calling the corresponding control program, comparing with the current feedback value of the control object, and completing the high-precision control of the position and speed of the system through intelligent control algorithm. The control software mainly includes the main program and timer interrupt processing program. Among them, the main program mainly completes system
initialization and upper computer command response processing. The interrupt function mainly reads the external data periodically, including speed instruction, position instruction, speed feed-forward and so on. According to the upper computer instruction and the current state of the system, it completes the algorithm control of the servo system, and outputs the control instructions to the driver. It also completes the functions of sending the current position and status to the host computer. The flow chart of the software program is shown in figure 7 and figures 8.

![Figure 7. Main program flow chart](image1)
![Figure 8. Flow chart of timer interrupt program](image2)

6. Conclusions
In this paper, an embedded servo control module based on NiosII soft core CPU is designed, which is described in detail from the aspects of software and hardware. The outstanding advantages of embedded system design based on NiosII soft core CPU are: fast and flexible hardware design, strong expansibility, shortened hardware development cycle, and improved design reliability. Software development is fast. CPU is implemented by soft core. Its functions can be customized according to needs. SOPC Builder provides more IP modules. This paper provides some references for the design of servo system, and can also be applied to other soft-core-based design schemes.

References
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