VLSI Implementation Of High Speed Low Power Design Using Hybrid Power Gating Technique

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Abstract

Nowadays, low power high speed CMOS design is one among the challenging issues. As the technology is scaling down, the static power consumption has turned into a remarkable concern. The proposed methodology incorporates the following technique such as sleep technique, stack technique, sleepy stack technique, sleepy keeper technique, leakage control transistor technique (LECTOR) and sleepy keeper leakage control transistor technique (SK-LCT) for leakage power reduction. The proposed power gating technique leads to low power, high speed CMOS design. The xor gate, xnor gate, half adder & 6T sram cell is outlined using newly proposed power gating technique for a low power high speed design. When compared to the conventional methodology xor gate saves 19.95 % of power & 33.75% of delay, xnor gate saves 12 % of power & 23.29% of delay, half adder saves 35.29% of power & 25.69% of delay and sram cell saves 14.29% of power & 34.37 % of delay. Simulation is done using Tanner EDA tool and the outcomes demonstrate a noteworthy change in leakage power utilization and speed.

Keywords: Static Power, Tanner EDA, Power gating, CMOS design

1. INTRODUCTION

In very large scale integration (VLSI) design increase in transistor density, power consumption and scaling of CMOS size become a very important constraint. The power dissipation of CMOS circuit includes both dynamic and static power dissipation. When the system is in active mode, dynamic power occurs in the circuit. In CMOS circuit the switching and short circuit power is calculated. Charging and discharging of load capacitance (CL) causes switching power and charging of internal node leads to short circuit power dissipation. The subthreshold leakage, gate induced drain leakage, oxide tunneling, junction leakage and gate leakage, are the foremost factor of leakage power dissipation [1]. The leakage current increases as device scaling takes place which increases the total power dissipation of CMOS circuit[2].

The battery lifetime of mobile device is determined by their leakage during sleep mode. Many static approach have urbanized to diminish the static current in CMOS circuit [3]. The power gating techniques is widely used in recent scenario, where static power can be reduced by NMOS footer or a PMOS header with high threshold voltage [4]. By turning on/off power switches, the amount of switching energy can be lowered by using the novel power gating with charge recycling technique. At both sleep-in and active mode, the charge sharing of switching energy happens between a virtual VDD & virtual VSS lines. Here, virtual VDD and VSS lines are coupled to power and ground supply through the PMOS switch and NMOS switch respectively. The charge recycled scheme can lose more energy than in sleep mode than the conventional power gating techniques without using charge sharing. In equalizing virtual VDD and VSS lines, the charge recycled power gating desires additional time and therefore wake-up time is longer. The coarse grain leakage suppression is shorter than...
the sleep mode of fine grain leakage. In the active mode of fine-grain leakage, a power gating technique activates the logic block of the circuit as fast as possible. The dual power gating scheme leads to low leakage power compared to conventional power gating scheme [5]. To accomplish low static power, the cost of the circuit will be increased in dual power gating. The parameter such as size of the power gate, slew rate, switching capacitance and leakage of power gate are needed to be considered for a successful implementation.

The high speed, low leakage power consumption power gating scheme such as single switch (SSPG), dual switch (DSPG) and charge recycled (CRPG) with different CMOS circuit are analyzed. In this paper, the work is extended by proposing a novel leakage reduction technique and comparing it with different CMOS circuit.

2. POWER GATING TECHNIQUES

In VLSI design, when the transistor is in idle condition, the static power occurs in the transistor channel. The power gating approach used in the integrated CMOS circuit; the static power dissipation is reduced by shutting off the block of the circuit for a small duration. The power gating technique enables Idq testing and also minimizes the static power of CMOS circuit.

![Power gating technique](image1)

**Figure 1.** Power gating technique

Figure 1 illustrates the power gating technique. The basic outline of this technique is to switch the power supply externally and achieve leakage power reduction. Static power dissipation is prohibited by power gating scheme and the CMOS circuitry requires less power. In CMOS circuit, a large sector of the power is idle during standby mode, since leakage power is the overwhelming part in CMOS circuit power utilization. The most commonly used power gating techniques are sleep technique, stack technique, sleepy stack technique, sleepy keeper technique & lector technique are used to shrink the static power dissipation.

![Sleep technique](image2)

**Figure 2.** Sleep technique

In sleep technique, sleep PMOS transistor (S) is implanted in between VDD & PUN and sleep NMOS transistor (S bar) is implanted in between PDN & gnd as shown in figure 2. The wakeup time of the sleepy method has a significantbrunt on the competency of the CMOS design [6].

Stack approach has the drawback of enlarged area and delay[7]. The PMOS & NMOS transistor is splitted into two transistor based on aspect ratio (W/L). The stack technique combined with sleep mode leads to increase the delay significantly & also diminish the expediency of this technique [8]. Figure 3 & Figure 4 illustrates stack technique and sleepy stack technique.
In sleepy keeper technique, the keeper transistor is positioned in parallel with a sleep transistor (S&S Bar) and gate of keeper circuit is coupled to the output of the circuit for performance enhancements as shown in figure 5. The leakage control transistors (LCT 1 & LCT 2) of lector technique is located in between the pull up device & pull down device. The static power dissipation of lector technique is reduced with small delay consumption [9]. By placing sleep transistor, the data preservation occurs in the circuit can be reduced [10]. LECTOR technique is illustrated in figure 6.

The PMOS leakage control transistor gate (LCT1) is tied with the drain of pull down device and NMOS leakage control transistor gate (LCT2) is tied with the drain of pull up device. In sleepy mode, NMOS is the only terminal connected parallel to VDD & pull up device and PMOS is the only terminal connected parallel to ground & pull down device.

Figure 3. Stack technique  
Figure 4. Sleepy stack technique  
Figure 5. Sleepy keeper technique  
Figure 6. LECTOR technique  
Figure 7. SK-LCT Technique
3. NEW POWER GATING TECHNIQUE

The existing power gating is upgraded and the new power gating technique is proposed for high speed, low power CMOS circuit. Figure 8 demonstrates the power gating technique. The new technique is obtained by combining existing sleepy stack keeper technique and lector technique. Here, sleep PMOS and sleep NMOS transistor (S & S Bar) is placed above and below the pull up network and pull down network. The pull up device & pull down device is stacked to shrink the leakage power of the circuit. As NMOS is faster compared to PMOS; the aspect ratio (W/L) of NMOS device is smaller than PMOS. LCT1 & LCT2 shrink the static power dissipation of the CMOS circuit which is placed in between pull up and pull down network. The gate of LCT1 is connected to the source of LCT2 and vice-versa. The keeper circuit is placed in parallel with the sleep transistor (S & S Bar) and both the gate terminal of the keeper circuit is linked to the output port. Here, the speed of the CMOS circuit is enhanced using the keeper circuit. There are two modes of operation in the proposed technique. They are,

(a) Active mode (AM)
(b) Sleep mode (SM)

In Active mode (AM), the logic ‘0’ & logic ‘1’ is given to sleep transistor and both the sleep transistors (S & S Bar) turns ON. The virtual node (Vss) is pulled down to the ground potential and virtual node (Vdd) is pulled up to the power potential. Here, both the sleep transistors offer very low resistance to pull up and pull down device. By combining stack and sleepy transistors, the fluctuations in the power supply will be minimized. The power gating methodology uses a sleep transistor where the high threshold device is used to minimize static power while stacked sleepy structure can shrink the leakage power with a normal threshold device. During Sleep mode (SM), both the sleep PMOS & NMOS transistors remain OFF. The virtual Vss node potential is disconnected to the gnd potential and virtual Vdd node potential is disconnected to the power potential. Here, both the sleep transistors offer very high resistance to pull up and pull down device. There is no connection path between pull up network & pull down device and offers very high resistance during sleep mode. A high speed, low power CMOS circuit is projected using the power gating technique with the improved performance.

4. LOW POWER HIGH SPEED CMOS CIRCUIT USING PROPOSED TECHNIQUE

The conventional design of CMOS circuits leads to high power dissipation and delay increases drastically. To overcome the disadvantages of the existing method, the CMOS circuit is designed using power gating technique. The XOR gate, XNOR gate, SRAM cell & halfadder are outlined using the power gating technique for the performance enhancement. The low power high speed XOR gate, XNOR gate, half adder & 6T SRAM cell is obtained and the power & delay of the circuit is analyzed. In high speed microprocessors such as adders, multipliers & comparators; XOR/XNOR gates are the basic block used for performing arithmetic operations. In CMOS arithmetic and counting circuits, the adder circuit plays an important role. SRAM gives fast access to data and it is used primarily for CPU internal registers and cache memory.
4.1. **XOR gate**
The digital logic XOR gate gives an output “1” when the inputs in the logic gate are at different logic level. If both the inputs in the logic gate are at the same logic level, the output “0” is obtained. It is used to implement binary addition in computers. Other uses of XOR include subtractor, controlled inverters, multiplier and comparators. A high speed, low power XOR gate is outlined using the power gating technique. Figure 9 illustrates XOR gate using the newly proposed power gating technique.

![Figure 9. XOR gate using proposed technique](image1)

4.2. **XNOR gate**
The XOR gate and NOT gate are combined to form “ExclusiveNOR” gate. If both of its inputs in the logic gate are at the same logic level either ‘0’ or ‘1’, the output “1” is obtained. If the inputs in the logic gate are at the different logic level, the output “0” is obtained. The Boolean expression of XNOR gate is given: Out = \(A \oplus B\) = \(AB + \overline{AB}\). A low power, high speed XNOR gate is obtained by designing the gate using power gating scheme. Figure 10 illustrates the XNOR gate using the newly proposed power gating technique.

![Figure 10. XNOR gate using proposed technique](image2)

4.3. **Half adder**
The binary bit (A and B) is added using half adder circuit and the output sum (S) and carry (C) is generated. The half adder circuit adds two input bit (ie. augend & addend bits) and the carry signal represent an overflow in the circuit. In half adder, XOR gate is used to perform sum operation (S) and an AND gate is used to perform carry operation (C). The adder designs using the existing power gating scheme shrink the leakage power dissipation and enhances the speed of adder circuit with some drawbacks. The newly proposed power gating approach leads to the design of low power, high speed adder circuit with the improved performance. Figure 11 illustrates CMOS half adder circuit using the newly proposed power gating technique.

![Figure 11. Half adder using proposed technique](image3)
4.4. 6T SRAM cell
A SRAM cell uses six MOSFET to store one bit binary information and has two stable states to write the data in memory cell. During read and write operation, the NMOS transistor is used to access the memory cell. SRAM cell is projected using the proposed scheme to diminish the leakage power dissipation of memory cells. When word line is high, access NMOS transistors are turned ‘ON’ in order to perform read and write operation. Two complementary bit lines (BL & BLB) are connected to the NMOS access transistor of memory cell and the data bit ‘0’ or ‘1’ is stored. The stored value in the memory remains unchanged until word WL is turned ‘ON’. Figure 12 illustrates a SRAM cell using newly proposed power gating technique.

5. SIMULATION RESULTS
The implementation of the power gating technique is projected using Tanner EDA Software. The circuit is designed in S-edit window and the output is simulated in W-edit window. To obtain the power and delay, the Spice command is typed in T-Spice window. The XOR gate, XNOR gate, half adder & 6T SRAM cell is outlined using new power gating method. The power & delay of conventional and the proposed circuits is analyzed and the entire work is conveyed in Tanner EDA 180nm technology.

5.1. Simulation result for XOR gate using proposed power gating technique
The XOR gate is designed using the proposed technique and the leakage power & delay of the gate is reduced. The low power, high speed XOR gate is utilized in many digital circuits and the performance of the CMOS circuit is improved. Figure 13 illustrates the simulation waveform for XOR gate using the new power gating technique.

5.2. Simulation result for XNOR gate using proposed power gating technique
The leakage power & delay of the XNOR gate is reduced using the power gating technique. The low power, high speed XNOR gate is used in many digital circuits. Figure 14 illustrates the simulation waveform for XNOR gate using the new power gating technique.

Figure 12. 6T SRAM cell using proposed technique
Figure 13. Simulation waveform for XOR gate using proposed power gating technique
Figure 14. Simulation waveform for XNOR gate using proposed power gating technique
5.3. Simulation result for half adder using the proposed power gating technique

A CMOS half adder circuit adds two input data (i.e. augend and addend bits) and sum&carry outputs of a half adder circuit is generated. The adder circuit using sleepy stack keeper & LECTOR technique leads to reduction of power and delay with few disadvantages. The newly proposed power gating technique leads to low power, high speed adder circuit with the improved performance. The simulation waveform for a Half Adder circuit using the proposed technique is illustrated in Figure 15.

5.4. Simulation result for 6T SRAM cell using the proposed power gating technique

If Word line=1 and BLB=1 & BL=0, the data ‘0’ is written in the memory cell. If Word Line=1 and BL=1 & BLB=0 the data ‘1’ are written in the memory cell. A high speed, low power SRAM cell is designed using the new technique and enhance the efficiency of the overall memory circuit. The simulation waveform of SRAM cell is projected using the newly proposed technique is illustrated in Figure 16.

Table 1 & 2 demonstrates the power and delay analysis of circuit such as XOR gate, XNOR gate, half adder & 6T SRAM cell. By utilizing the existing power gating, the power of CMOS circuit can be diminished with some drawback. The power gating technique is upgraded and XOR gate, XNOR gate, half adder & 6T SRAM cell are designed using the proposed technique. The power & delay of CMOS circuit are reduced compared to conventional method.

| CMOS circuit       | Power (µW) | Conventional method | Proposed Technique |
|--------------------|------------|---------------------|--------------------|
| XOR gate           | 10.87      | 8.701               |
| XNOR gate          | 10.12      | 8.905               |
| Half adder         | 23.91      | 15.47               |
| 6T SRAM cell       | 34.76      | 29.79               |

| CMOS circuit       | Delay (ns) | Conventional method | Proposed Technique |
|--------------------|------------|---------------------|--------------------|
| XOR gate           | 29.73      | 19.696              |
| XNOR gate          | 39.96      | 30.65               |
| Half adder         | 42.852     | 31.84               |
| 6T SRAM cell       | 49.88      | 32.732              |

6. CONCLUSION

The conventional design of CMOS circuits leads to high power dissipation and delay increases drastically. To overcome the drawback, the CMOS circuit is designed using the power gating technique. The CMOS circuit is outlined using the new technique and power & delay of the circuit is analyzed. By utilizing the existing power gating, the power & delay parameter of the CMOS circuit is reduced with some disadvantage. The power gating technique is upgraded and XOR gate, XNOR gate, half adder & 6T SRAM cell are designed using the newly proposed power gating technique. XOR gate saves 19.95% of power & 33.75% of delay, XNOR gate saves 12% of power & 23.29% of delay, half adder saves 35.29% of power & 25.69% of delay and SRAM cell saves...
14.29% of power & 34.37% of delay than the conventional method. From the result, it is evident that the proposed power gating technique provides efficient low power, high speed CMOS circuit with improved performance and the complete work is carried out in Tanner EDA tool.

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