Abstract—Enclaves, such as those enabled by Intel SGX, offer a powerful hardware isolation primitive for application partitioning. To become universally usable on future commodity OSes, enclave designs should offer compatibility with existing software. In this paper, we draw attention to 5 design decisions in SGX that create incompatibility with existing software. These represent concrete starting points, we hope, for improvements in future TEEs. Further, while many prior works have offered partial forms of compatibility, we present the first attempt to offer binary compatibility with existing software on SGX. We present RATEL, a system that enables a dynamic binary translation engine inside SGX enclaves on Linux. Through the lens of RATEL, we expose the fundamental trade-offs between performance and complete mediation on the OS-enclave interface, which are rooted in the aforementioned SGX design restrictions. We report on an extensive evaluation of RATEL on over 200 programs, including micro-benchmarks and real applications such as Linux utilities.

I. INTRODUCTION

Commercial processors today have native support for trusted execution environments (TEEs) to run user-level applications in isolation from other software on the system. A prime example of such a TEE is Intel Software Guard eXtensions (SGX) [17]. The hardware-isolated environment created by SGX, commonly referred to as an enclave, runs a user-level application without trusting privileged software.

Enclaved TEEs offer a powerful new foundation for compartmentalization on commodity OSes. Enclaves remove privileged software layers (OS or hypervisor) from the trusted code base of isolated components. Therefore, they crucially differ from existing isolation primitives like processes, virtual machines, and containers. Enclaves offer the intriguing possibility of becoming ubiquitously used abstractions in the future, much like processes, but this demands a scale of usage not originally envisioned with SGX. Enclaves would need to be compatible with a large fraction of the existing software and OS abstractions. Arguably, compatibility is the most important challenge facing future enclave TEEs. One would only be concerned with additional enclave security threats if they could run the desired application in the first place.

Right from the inception, compatibility with existing x86_64 binaries has been a recognized issue with SGX [22]. Prior works have proposed a number of different ways of achieving partial compatibility—offering specific programming languages for authoring enclave code [4], [54], keeping compatibility with container interfaces [3], [35], or conformance to specific versions of library interfaces provided by library OSes [6], [17], [58], [61], [64].

While these approaches are promising and steadily maturing, none of them offer binary compatibility with existing software. In existing approaches, applications are expected to be relinked against specific versions of libraries (e.g., musl, libgc, glibc), ported to a customized OS, or containerized. Such modifications require significant changes to the complex build systems in place, often demanding developer involvement and even access to source code. More importantly, most prior works have enabled sufficient SGX compatibility to handle specific applications [38], [52], [53], standard libraries, or language runtimes [20], [30]–[32], [72] that these platforms choose. Trade-offs arising between compatibility, security, and performance are often resolved in the favor of performance in prior designs. Thus, the complete picture of these fundamental trade-offs has never been presented.

The purpose of this paper is two-fold. First, we believe that future designs of enclave TEEs would benefit from understanding which design choices made in SGX create binary incompatibility. In particular, we pinpoint at 5 specific SGX restrictions and explain how they create a sweeping incompatibility with existing OS abstractions of multi-threading, memory mapping, synchronization, signal-handling, shared memory, and others. These challenges affect other compatibility approaches too. However, our emphasis on full binary compatibility brings them out more comprehensively.

Second, we study the feasibility of a new approach that can offer binary compatibility for unmodified applications in SGX enclaves. Our approach enables interposition of enclave applications via dynamic binary translation (DBT). DBT is a mature technique for cross-platform binary compatibility available even before SGX [11]. It works by instrumenting machine instructions on-the-fly to provide a layer of transparency to the underlying system. This is sometimes referred to as application-level virtualization.

We report on our experience of running a widely used DBT framework called DynamoRIO inside SGX enclaves [14]. The resulting system called RATEL enables DBT on Intel SGX enclaves for unmodified x86_64 Linux binaries. RATEL aims to ensure that it adheres to enclave threat model: it does not trust the OS in its design. The challenges of enabling a full-fledged DBT engine is instructive in exposing a set of fundamental trade-offs on SGX—one has to choose “2 out of 3” between security, binary compatibility, and performance. RATEL chooses to resolve these in favor of security and binary

---

Part of the research was done while at National University of Singapore.
compatibility.

The main challenge addressed by RATEL is that it offers secure and complete mediation on all data and control flow between the OS and the application. Our main finding is that the problem of complete mediation suffers from the “last mile” phenomenon: We pay modestly in performance to get to partial mediation, as seen in many prior works, but significantly for the full binary compatibility on SGX.

As a standalone tool, RATEL offers its own conceptual utility. It offers complete mediation on all application-OS interactions, which is useful for security interposition. This side steps challenges of static source-code based solutions, which expect changes ahead of time, and can work for dynamically generated or self-modifying code. Further, RATEL provides the facility of instruction-level instrumentation. This can be useful in many ways: inlining security monitors, sandboxing, fine-grained resource accounting, debugging, or deployment of third-party patches in response to newly discovered flaws (though these are not our focus) [12], [13], [25], [39], [44].

Contributions & Results. RATEL is the first system that targets binary compatibility for SGX, to the best of our knowledge. Our proposed design enables an industrial-strength dynamic binary translation engine inside SGX enclaves. We evaluate compatibility offered by RATEL extensively. We successfully run a total of 203 unique unmodified binaries across 5 benchmark suites (58 binaries), 4 real-world application use-cases (12 binaries), and 133 Linux utilities. These encompass various work-load profiles including CPU-intensive (SPEC 2006), I/O system call intensive (FSCQ, IOZone), system stress-testing (HBenchOS), multi-threading support ( Parsec-SPLASH2), a machine learning library (Torch), and real-world applications demonstrated in prior works on SGX. RATEL offers compatibility but does not force applications to use any specific libraries or higher-level interfaces.

Our work pin-points 5 specific design choices in SGX that are responsible for incompatibility. We believe these create challenges for prior approaches providing partial compatibility as well. We hope future enclave TEE designs pay attention to addressing these 5 points from the outset.

II. Why is Binary Compatibility Challenging?

Intel SGX allows execution of code inside a hardware-isolated environment called an enclave [22]. SGX enforces confidentiality and integrity of enclave-bound code and data. All enclave memory is private and only accessible when executing in enclave-mode. Data exchanged with the external world (e.g., the host application or OS) must reside in public memory which is not protected. At runtime, one can only synchronously enter an enclave via ECALLs and exit an enclave via OCALLs. Any illegal instructions or exceptions in the enclave create asynchronous entry-exit points. SGX restricts enclave entry and exits to pre-specified points in the program. If the enclave execution is interrupted asynchronously, SGX saves the enclave context and resumes it at the same program point at a later time. Our challenge is to interpose securely and completely on all the control and data transfers between the enclave and the OS.

A. Restrictions Imposed by SGX Design

Intel SGX protects the enclave by enforcing strict isolation at several points of interactions between the OS and the user code. We outline 5 SGX design restrictions.

R1. Spatial memory partitioning. SGX enforces spatial memory partitioning. It reserves a region that is private to the enclave and the rest of the virtual memory is public. Memory can either be public or private, not both.

R2. Static memory partitioning. The enclave has to specify the spatial partitioning statically. The size, type (e.g., code, data, stack, heap), and permissions for its private memory have to be specified before creation and these attributes cannot be changed at runtime.

R3. Non-shareable private memory. An enclave cannot share its private memory with other enclaves on the same machine.

R4. 1-to-1 private virtual memory mappings. Private memory spans over a contiguous virtual address range, whose start address is decided by the OS. Private virtual address has one-to-one mapping with a physical address.

R5. Fixed entry points. Enclaves can resume execution only from its last point and context of exit. Any other entry points/contexts have to be statically pre-specified as valid ahead of time.

B. Ramifications

Next, we explain the impact of these design restrictions on various OS and application functionality (see Table I).

R1. Since SGX spatially partitions the enclave memory, any data which is exchanged with the OS requires copying between private and public memory. In normal applications, an OS assumes that it can access all the memory of a user process, but this is no longer true for enclaves. Any arguments that point to enclave private memory are not accessible to the OS or the host process. The enclave has to explicitly manage a public and a private copy of the data to make it accessible externally and to shield it from unwanted modification when necessary. We refer

| OS abstraction                      | Restrictions Affecting Abstraction |
|-------------------------------------|-----------------------------------|
| System call arguments               | R1                                |
| Dynamic Loaded / Gen. code          | R2                                |
| Thread Support                      | R5, R2                            |
| Signal Handling                     | R1, R5                            |
| Thread Synchronization              | R3, R1                            |
| File / Memory Mapping               | R1, R2, R3, R4                    |
| IPC / Shared Memory                 | R3, R4                            |

TABLE I: Ramifications of SGX design restrictions on common OS abstractions.

1Unless stated otherwise, we use the term Intel SGX v1 to refer to the hardware as well as the trusted platform software (PSW) and the trusted software development kit (SDK), as shown in Figure 2.
to this as a *two-copy mechanism*. Thus, $R_1$ breaks functionality (e.g., system calls, signal handling, futex), introduces non-transparency (e.g., explicitly synchronizing both copies), and introduces security gaps (e.g., TOCTOU attacks [18], [29]).

**R2.** Applications often require changes to the size or permissions of enclave memory. For example, memory permissions change after dynamic loading of libraries (e.g., `dlopen`) or files (e.g., `mmap`), executing dynamically generated code, creating read-only zero-ed data segments (e.g., `.bss`), and for software-based isolation of security-sensitive data. The restriction $R_2$ is incompatible with such functionality. To work with this restriction, applications require careful semantic changes: either weaken the protection (e.g., read-and-execute instead of read-or-execute), use a two-copy design, or rely on some additional form of isolation (e.g., using segmentation or software instrumentation).

**R3.** SGX has no mechanism to allow two enclaves to share parts of their private memory directly. This restriction is incompatible with the synchronization primitives like locks and shared memory when there is no trusted OS synchronization service. Keeping two copies of locks breaks the semantics and create a chicken-and-egg issue: how to synchronize two copies of a shared lock without another trusted synchronization primitive.

**R4.** When applications demand new virtual address mappings (e.g., `malloc`) the OS adds these mappings. The application can ask the OS to map the same physical page at several different offsets—either with same or different permissions. For example, the same file is mapped as read-only at two places in the program. Since, SGX doesn’t allow the same physical address to be mapped to multiple virtual addresses, any such mappings generate a general protection fault in SGX.

**R5.** SGX starts or resumes enclave execution only from controlled entry points i.e., the virtual address and the execution context. However, there are several unexpected entry points to an application when we run them unmodified in an enclave (e.g., exception handlers, library functions, illegal instructions). Statically determining all potential program points for re-entry is challenging. Further, when the enclave resumes execution, it expects the same program context. This does not adhere with typical program functionality. Normally, if the program wants to execute custom error handling code, say after a divide-by-zero (SIGFPE) or illegal instruction (SIGILL), it can resume execution at a handler function in the binary with appropriate execution context setup by the OS. On the contrary, SGX will resume enclave execution at the same instruction and same context (not the OS setup context for exception handling), thus re-triggering the exception.

Intel is shipping SGX v2, wherein an enclave can make dynamic changes to private page permissions, type, and size. We discuss their specifics in Section VII. Note that, SGX v2 only addresses $R_2$ partially, while all the other restrictions still hold true. Thus, for the rest of the paper, we describe our design based on SGX v1.

### III. Overview

Before we present our design, we emphasize our key empirical takeaway that led to it: *Working with restrictions $R_1 – R_5$, we are faced with a “choose 2-out-of-3” trilemma between security, performance, and binary compatibility.* We explain these trade-offs in Section III-B. Our design picks security and compatibility over performance, wherever necessary. In this design principle, it fundamentally departs from prior work.

Several different approaches to enable applications in SGX enclaves have been proposed. In nearly all prior works, performance consideration dominate design decisions. A prominent way to side-step the performance costs of ensuring compatibility and complete mediation is to ask the application to use a prescribed program-level interface or API. The choice of interfaces vary. They include specific programming languages [20], [28], [30], [73], application frameworks [40], container interfaces [3], and particular implementation of standard `libc` interfaces. Figure 1 shows the prescribed interfaces in three approaches, including library OSes and container engines, and where they intercept the application to maintain compatibility.

Given that binary compatibility is not the objective of prior works, they handle subsets of $R_1 – R_5$. One drawback of these approaches is that if an application does not originally use the prescribed API, the application needs to be rewritten, recompiled from source, or relinked against specific libraries.

Our work poses the following question: Can full *binary compatibility* be achieved on SGX, and if so, with what trade-offs in security or performance? Application binaries are originally created with the intention of running on a particular OS and we aim to retain compatibility with the OS system call interface (e.g., Linux). In concept, applications are free to use any library, direct assembly code, and runtime that uses the Linux system call interface. The central challenge we face is to enable *secure and complete mediation of all data and control flow* between the application and the OS. We do this by enabling a widely used DBT engine inside enclaves.

#### A. Background: Dynamic Binary Translation

Dynamic binary translation is a well-known approach to achieving full binary compatibility. It was designed to secure and complete mediation: the ability to intercept each instruction in the program before it executes. DBT works by first loading the binary code that is about to be executed into its own custom execution engine. It then updates the code in-situ, if required, and then dispatches it for execution. To contrast it with the approach of changing `libc`, DBT intercepts the application right at the point at which it interacts with the OS (see Figure 1).

In this paper, we choose DynamoRIO as our DBT engine, since it is open-source and widely used in industry. [11] DynamoRIO is itself an example of just-in-time compilation engine which dynamically generates code. At a high level, DynamoRIO first loads itself and then loads the application code in a separate part of the virtual address, as show in

\[\text{2The other option is Intel Pin [36], but it is not open-source.}\]
Fig. 1: Different abstraction layers for compatibility. Black shaded regions are untrusted, gray shaded regions are modifications or additions, thick solid lines are enclave boundaries, clear boxes are unmodified components, zig-zag lines show break in compatibility. (a) Container abstraction with musl libc interface (Scone [3]). (b) Library OS with glibc interface (Graphene-SGX [17]). (c) Process abstraction with POSIX interface (Panoply [64]). (d) Dynamic Binary Translation with DynamoRIO in RATEL (This work).

Figure 2] Similarly, it sets up two different contexts, one for itself and one for the application. DynamoRIO can update the code on-the-fly before putting it in the code-cache by re-writing instructions (e.g., convert syscall instruction to a library function call). Such rewriting ensures that DynamoRIO engine takes control before each block of code executes, enabling the ability to interpose on every instruction. Instrumented code blocks are placed in a region of memory called a code cache. When the code cache executes, DynamoRIO regains control as the instrumentation logic desires. It does post-execution updates to itself for book-keeping or to the program’s state. Additionally, DynamoRIO hooks on all events intended for the process (e.g., signals). The application itself is prevented from accessing DynamoRIO memory via address-space isolation techniques [59]. Thus, it acts as an arbiter between the application’s binary code and the external environment (e.g., OS, filesystem) with secure and complete mediation.

RATEL retains the entire low-level instruction translation and introspection machinery of DynamoRIO, including the code cache and its performance optimizations. This enables reusing well-established techniques for application transparency, instrumentation, and performance enhancements. We eliminate the support for auxiliary plugins to reduce TCB.

B. RATEL Approach

Our design must provide compatibility for both the DynamoRIO DBT engine as well as any application binary code that runs translated. We provide a high-level overview of RATEL and then explain the key trade-offs we face when forced with compliance to SGX restrictions R1 – R5.

High-level Overview. We modify DynamoRIO to adhere to SGX virtual memory limitations (R1-R4) by setting up our custom layout. Specifically, we analyze DynamoRIO code to identify its entire virtual address layout. This allows us to load RATEL and start its execution without violating the memory semantics of SGX. We register a fixed entry point in RATEL when entering or resuming the enclave. This entry point acts as a unified trampoline, such that upon entry, RATEL decides where to redirect the control flow, depending on the previously saved context. In DynamoRIO code, we manually replace instructions that are illegal in SGX with an external call that executes outside the enclave. Thus, RATEL execution itself is guaranteed to never violate R5.

The same challenges show up when RATEL starts loading and running the translated application binary. However, we have the advantage of dynamically rewriting the application logic to adapt it to R1-R5. We statically initialize the virtual memory size of the application to the maximum allowed by SGX; the type and permissions of memory is set to the specified type in the binary. We add a memory management unit to DynamoRIO to keep track of and transparently update the applications layout. At runtime, when the application makes direct changes to its own virtual memory layout via system calls, RATEL dynamically adapts it to SGX (e.g., by making two copies or relocating the virtual mappings). RATEL intercepts all application interactions with the OS. It modifies application parameters, OS return values, OS events for monitoring indirect changes to the memory (e.g., thread creation). In the other direction, RATEL also intercepts OS events on the behalf of the application. Upon re-entry, if the event has to be delivered to the application, it sets/restores the appropriate execution context and resumes execution via the trampoline.

Lastly, before executing any application logic, RATEL scans the code cache for any instructions (e.g., syscall, cpuuid) that may potentially be deemed as illegal in SGX and replaces it.
with an external call. Thus, RATEL remedies the application on-the-fly to adhere to R1-R5.

Key Design Trade-offs. RATEL aims for secure and complete mediation on all data and control flow between the application and OS, through the use of DBT. This makes RATEL useful for a wide variety of reasons: in-lining security monitoring, software sandboxing, and even profiling and debugging. We do not assume that the application is written to help RATEL by adhering to restrictions beyond those specified by a normal OS, nor do we trust the OS. SGX restrictions R1–R5 give rise to trade-offs between security, compatibility, and performance. We point out that these are somewhat fundamental and apply to RATEL and other compatibility efforts equally. However, RATEL chooses security and compatibility over performance, whenever conflicts between the three arise.

Whenever the application reads from or writes outside the enclave, the data needs to be placed in public memory due to R1. Computing on data in public memory, which is exposed to the OS, is insecure. Therefore, if the application wishes to securely compute on the data, a copy must necessarily be maintained in a separate private memory space, as R2 forbids making changing data permissions. This leads to a “two copy” mechanism, instances of which repeat throughout the design. The two-copy mechanism, however, incurs both space and computational performance overheads, as data has to be relocated at runtime. Further, certain data structure semantics which require a single memory copy (e.g., futexes) become impossible to keep compatibility with (see Section IV-D).

R3 creates an “all or none” trust model between enclaves. Either memory is shared with all entities (including the OS) or kept private to one enclave. R4 restricts sharing memory within an enclave further. These restrictions are in conflict with semantics of shared memory and synchronization primitives. To implement such abstractions securely, the design must rely on a trusted software manager which necessarily resides in an enclave, since the OS is untrusted. Applications can then have compatibility with lock and shared memory abstractions and securely, but at the cost of performance: Access to shared services turn into procedure calls to the trusted manager.

Restriction R5 requires that whenever the enclave resumes control after an exit, the enclave state (or context) should be the same as right before exit. This implies that the security monitor (e.g., the DBT engine) must take control before all exit points and after resumption, to save-restore contexts—otherwise, the mediation can be incomplete, creating security holes and incompatibility. Without guarantees of complete mediation, the OS can return control into the enclave, bypassing a security checks that the DBT engine implements. The price for complete mediation on binaries is performance: the DBT engine must intercept all entry/exit points and simulate additional context switches in software. Prior approaches, such as library-OSes, sacrifice complete mediation (security) for better performance, by asking applications to link against specific library interfaces which tunnel control via certain points. But, this does not enforce complete mediation as applications can make direct OS interactions or override entry handlers, intentionally or by oversight. There are several further security considerations that arise in the details of the above design decisions. These include (a) avoiding naïve designs that have TOCTOU attacks; (b) saving and restoring the execution context from private memory; (c) maintaining RATEL-specific metadata in private memory to ensure integrity of memory mappings that change at runtime; and (d) explicitly zeroing out memory content and pointers after use. We explain them inline in Section IV.

C. Scope

Many challenges are common between the design of RATEL presented here and other systems. These include encryption/decryption of external file or I/O content [3, 35, 61, 69], sanitization of OS inputs to prevent Iago attacks [18, 37, 66, 71], defenses against known side-channel attacks [8, 34, 56, 62, 63], additional attestation or integrity of dynamically loaded/generated code [30–32, 72], and so on. These are important but largely orthogonal to the focus of this work. These can be implemented on top of RATEL in the future.

Our focus is to expose the compatibility challenges that SGX creates with rich process-level abstractions. These require careful design to eliminate additional security threats. One limitation of RATEL is that the present implementation of RATEL has support for majority but not all of the Linux system calls. The most notable of the unsupported system calls is fork which is used for multi-processing. We believe that the basic design of RATEL can be extended to support fork with the two-copy mechanism, similar to prior work [64]. Our experience suggests that adding other system calls is a tedious but conceptually straightforward effort in RATEL. We expect to expand the syscall coverage over time, possibly with the help of automated tools.

IV. RATEL Design

Our main challenge is to execute the system functionality securely while faithfully preserving its semantics for compatibility. We explain how RATEL design achieves this for various sub-systems that are typically expected by applications.

A. System Calls & Unanticipated Entry-Exits

SGX does not allow enclaves to execute several instructions such as syscall, cpuid, rdtsnc. If the enclave executes them, SGX exits the enclave and generates a SIGILL signal. Gracefully recovering from the failure requires re-entering the enclave at a different program point. Due to R5, this is disallowed by SGX. In RATEL, either DynamoRIO or the application can invoke illegal instructions, which may create unanticipated exits from the enclave.

RATEL has three ways to handle them: (a) entirely delegate the instruction outside the enclave (e.g., file, networking, and timer operations); (b) execute the instruction outside the enclave while explicitly updating the in-enclave state (e.g.,
thread operations, signal handling); or (c) completely simulate instruction inside the enclave.

RATEL changes DynamoRIO logic to convert such illegal instruction to stubs that either delegate or emulate the functionality. For the target application, whenever RATEL observes an illegal instructions in the code cache, it replaces the instruction with a call to the RATEL syscall handler function.

Syscalls are a special case—they access process memory for input-output parameters and error codes. Since enclaves do not allow this, for delegating the syscall outside the enclave, RATEL creates a copy of input parameters from private memory to public memory. This includes simple value copies as well as deep copies of structures. The OS then executes the syscall and generates results in public memory. Post-call, RATEL copies back the explicit results and error codes to private memory.

Memory copies alone are not sufficient. For example, when loading a library, the application uses `d1_open` which in turn calls `mmap`. When we execute the `mmap` call outside the enclave, the library is mapped in the untrusted public address space of the application. However, we want it to be mapped privately inside the enclave. As another example, consider when the enclave wants to create a new thread local storage (TLS) segment. If RATEL executes the system call outside the enclave, the new thread is created for the DynamoRIO runtime instead of the target application. Thus, when a syscall implicitly changes application state, RATEL has to explicitly propagate those changes inside the enclave.

Alternatively, RATEL selectively emulates some syscalls inside the enclave. For example, `arch_prctl` is used to read the FS base, RATEL substitutes it with a `rdfsbase` instruction and executes it inside the enclave. We outline the details of other syscall subsystems that are fully or partially emulated by RATEL in Sections IV-B, IV-C, IV-D, IV-E.

RATEL resumes execution only after the syscall state has been completely copied inside the enclave. This allows it to employ sanitization of OS results before using it. Further, all the subsequent execution is strictly over private memory to avoid TOCTOU attacks.

B. Memory Management

For syscalls that change process virtual address layout, RATEL has to explicitly reflect their changes inside the enclave. First, this is not straightforward. Due to R1-R4, several layout configurations are not allowed for enclave virtual memory (e.g., changing memory permissions). Second, RATEL does not trust the information provided by the OS (e.g., via `procmap`).

To address these challenges, RATEL maintains its own `procmap`-like structure. Specifically, RATEL keeps its own view of the process virtual memory inside the enclave, tracks the memory-related events, and updates the enclave state. For example, after `mmap` call succeeds outside the enclave, RATEL allocates and records the new virtual address located inside the enclave.

Further, RATEL synchronizes the two-copies of memories to maintain execution semantics. For example, after `mmap`, RATEL creates a new memory mapping inside the enclave and then copies the content of the `mmap`-ed memory inside the enclave. On subsequent changes to `mmap`-ed memory, RATEL updates the non-enclave memory via a write. This is done whenever the application either unmaps the memory or invokes `sync` or `fasync` system call.

With mediation over memory management, RATEL transparently side-steps SGX restrictions. When application makes requests that are not allowed in SGX (e.g., changing memory permissions), RATEL replaces it with a sequence of valid SGX operations that achieve the same effect (e.g., move the content to memory which has the required permissions). Subsequently, when the application binary accesses memory, RATEL can pre-emptively replace the addresses to access the correct enclave copy of the memory. This allows us to safely and transparently mimic disallowed behavior inside the enclave.

RATEL does not blindly replicate OS-dictated memory layout changes inside the enclave. It first checks if the resultant layout will violate any security semantics (e.g., mapping a buffer to zero-address). It proceeds to update enclave layout and memory content only if these checks succeed. To do this, RATEL keeps its metadata in private memory.

C. Multi-threading

SGX requires the application to pre-declare the maximum number of threads before execution (R2). Further, it does not allow the enclave to resume at arbitrary program points or execution contexts (R5). This creates several compatibility and security challenges in RATEL.

DynamoRIO and the target application share the same thread, but they have separate TLS segment for cleaner context switch. DynamoRIO keeps the threads default TLS segment for the target application and creates a new TLS segment for itself at a different address. DynamoRIO switches between these two TLS segments by changing the segment register—DynamoRIO uses `gsbase`, application uses `fsbase`. SGX allocates one TLS segment per enclave thread. SGX uses the same mechanism as DynamoRIO (i.e., changing the segment) to maintain a shadow TLS segment for itself when executing enclave code.
Multiplexing Base Registers. When we attempt to run DynamoRIO inside SGX, there are not enough registers to save three offsets (one for DynamoRIO, one for SGX, one for the application). To circumvent this limitation, RATEL adds two TLS segment fields to store $f_{base}$ and $g_{base}$ register values. We use these TLS segment fields to save and restore pointers to the segment base addresses. This allows us to maintain and switch between three clean TLS segment views per thread.

Primary-secondary TLS Segment Design. Since RATEL is in-charge of maintaining the view of multiple-threads, it has to switch the TLS segment to a corresponding thread every time the execution enters or exits the enclave. We simplify these operations with a primary-secondary TLS segment design. RATEL adds a new field to the SGX thread data structure—a flag to indicate if the TLS segment is the primary or not.

RATEL marks the default first TLS segment created by SGX as the primary. To do this, it sets the flag of the TLS segment when the execution enters the enclave for the first time after creation. All the subsequent TLS segment, if created, are marked as secondary. If the flag is false, the base value stores the pointer to the addresses of the primary TLS segment. Otherwise, it points to the secondary TLS segment required to execute DynamoRIO. With this mechanism, upon enclave entry, RATEL circulates through the TLS segment pointers until it finds the addresses for the primary TLS segment.

Dynamic Threading. Since the number of TCS entries is fixed at enclave creation time, the maximum number of threads supported is capped. RATEL multiplexes the limited TCS entries, as shown in Figure 3. When an application wants to create a new thread (e.g., via clone), RATEL first checks if there is a free TCS slot. If it is the case, it performs an OCALL to do so outside the enclave. Otherwise, it busy-waits until a TCS slot is released. Once a TCS slot is available, the OCALL creates a new thread outside the enclave. After finishing thread creation, the parent thread returns back to the enclave and resumes execution. The child thread explicitly performs an ECALL to enter the enclave and DynamoRIO resumes execution for the application’s child thread.

For all threading operations, RATEL ensures transparent context switches to preserve binary compatibility as intended by DynamoRIO. For security, RATEL creates and stores all thread-specific context either inside the enclave or SGX’s secure hardware-backed storage at all times. It does not use any OS data structures or addresses for thread management.

D. Thread Synchronization

SGX provides basic synchronization primitives (e.g., SGX mutex and conditional locks) backed by hardware locks. But they can only be used for enclave code. Thus, they are semantically incompatible with the lock mechanisms used by DynamoRIO or legacy applications which use OS locks. For example, DynamoRIO implements a sophisticated mutex lock using `futex` syscall, where the lock is kept in the kernel memory. Supporting this requires trusting the OS for sharing locks. Given R1 and R3, SGX does not offer any memory sharing model, making it impossible to support `futexes`.

Need for a Lock Manager. A naive design would be to maintain a shadow `futex` variable in public memory, such that it is accessible to the enclave(s) and the OS. However, the OS can arbitrarily change the lock state and attack the application. As an alternative, we can employ a two-copy mechanism for locks. The enclave can keep the lock in private memory. When it wants to communicate state change to the OS, RATEL can tunnel a `futex OCALL` to the host OS. There are several problems even with this approach. Threads inside the enclave may frequently update the locks in private memory. Polling or accessing the `futex` outside the enclave (including the kernel and the untrusted part of the enclave) requires the latest state of lock every time there is an update in private memory. This creates an opportunity for the OS to launch TOCTOU attack. Even without TOCTOU attacks, it is challenging to synchronize the two copies in benign executions. Specifically, private lock states can be changed while the public state is being updated. This results in threads inside and outside the enclave with inconsistent views of the same lock (i.e., private and public copy). The more frequent the local updates, the higher is the probability of such inconsistencies. In general, the only way to avoid such race condition bugs is to use locks for synchronizing the private and public state of the enclave locks. This is impossible with SGX because it does not support secure memory sharing between the OS and the enclave(s). Figure 4 shows the schematics of design choices for implementing synchronization primitives.

RATEL Lock Manager. Given the `futex`-usage of DynamoRIO, we identify that we can avoid sharing an enclave’s lock directly with the OS or other enclaves. The DynamoRIO usage of `futexes` can be replaced with a simpler primitive such as spinlocks to achieve the same functionality. Specifically, we implement a lock manager in RATEL. We use the hardware spinlock exposed by SGX to do this securely and efficiently inside the enclave. In RATEL we invoke our lock manager implementation wherever DynamoRIO tries to use `futexes`. The other instance of `futex` usage is in the application binaries being executed with RATEL. To handle those cases, when RATEL loads application binary into the code cache, it replaces
thread-related calls (e.g., pthread_cond_wait) with stubs to invoke our lock manager to use safe synchronization.

E. Signal Handling

RATEL cannot piggyback on the existing signal handling mechanism exposed by the SGX, due to R5. Specifically, when DynamoRIO executes inside the enclave, the DynamoRIO signal handler needs to get description of the event to handle it (Figure 5(a)). However, Intel’s SGX platform software removes all such information when it delivers the signal to the enclave. This breaks the functionality of programmer-defined handlers to recover from well-known exceptions (divide by zero). Further, any illegal instructions inside the enclave generate exceptions, which are raised in form of signals. Existing binaries may not have handlers for recovering from instructions illegal in SGX.

SGX allows entering the enclave at fixed program points and context. Leveraging this, RATEL employs a primary signal handler that it registers with SGX. For any signals generated for DynamoRIO or the application, we always enter the enclave via the primary handler and we copy the signal code into the enclave. We then use the primary as a trap to route the control to the appropriate secondary signal handler inside the enclave, based on the signal code. At a high-level, we realize a virtualized trap-and-emulate signal handling design. We use SGX signal handling semantics for our primary. For the secondary, we setup and tear down a separate stack to mimic the semantics in the software. The intricate details of handling the stack state at the time of such context switched are elided here. Figure 5(b) shows a schematic of our design.

Registration. Original DynamoRIO code and the application binary use sigaction to register signal handlers for itself. We refer to them as secondary handlers. In RATEL, first we change DynamoRIO logic to register only the primary signal handler with SGX. We then record the DynamoRIO and application registrations as secondary handlers. This way, whenever SGX or the OS wants to deliver the signal for the enclave, SGX directs the control to our primary handler inside the enclave.

Since this is a pre-registered handler, SGX allows it. The primary handler checks the signal code and explicitly routes execution to the secondary.

Delivery. A signal may arrive when the execution control is inside the enclave (e.g., timer). In this case, RATEL executes a primary signal handler code that delivers the signal to the enclave. However, if the signal arrives when the CPU is in a non-enclave context, SGX does not automatically invoke the enclave to redirect execution flow. To force this, RATEL has to explicitly enter the enclave. But it can only enter at a pre-registered program point with a valid context (R5). Thus we first wake up the enclave at a valid point (via ECALL) and copy the signal code. We then simulate the signal delivery by setting up the enclave stack to execute the primary handler.

Exit. After executing their logic, handlers use sigreturn instruction for returning control to the point before the signal interrupted the execution. When RATEL observes this instruction in the secondary handler it has to simulate a return back to the primary handler instead. The primary handler then performs its own real sigreturn. SGX then resumes execution from the point before the signal was generated.

V. IMPLEMENTATION

We implement RATEL by using DynamoRIO. We run DynamoRIO inside an enclave with the help of standard Intel SGX development kit that includes user-land software (SDK v2.1), platform software (PSW v2.1), and a Linux kernel driver (v1.5). We make a total of 9667 LoC software changes to DynamoRIO and SDK infrastructure. We run RATEL on an unmodified hardware that supports SGX v1.

RATEL design makes several changes to DynamoRIO core (e.g., memory management, lock manager, signal forwarding). When realizing our design, we address three high-level implementation challenges. Their root cause is the way Intel SDK and PSW expose hardware features and what DynamoRIO expects. There are several low-level challenges that we do not discuss here for brevity.

Self-identifying Load Address. DynamoRIO needs to know its location in memory mainly to avoid using its own address space for the application. In RATEL, we use a call – pop mechanism to self-identify our location in memory. These contiguous instructions, allow us to dynamically retrieve our own address. Specifically, we align this address and decrease it at a granularity of page-size to compute our start-address in memory.

Insufficient Hardware Slots. By default, SGX SDK and PSW assume two SSA frames, which are sufficient to handle most of the nested signals. Since RATEL design needs one SSA frame for itself, we increase the SSA frames to three to ensure we can handle the same set of nested signals as SGX. The SGX specification allows this by changing the NSSA field in our PSW implementation.

Preserving Execution Contexts. For starting execution of a newly created thread, RATEL invokes a pre-declared ECALL to enter the enclave. This is a nested ECALL, which is not supported by SGX SDK. To allow it, we modify the SDK to facilitate the entrance of child threads and initialize the thread data structure for it. Specifically, we check if the copy of thread arguments inside the enclave matches the ones outside before resuming thread execution. We save specific registers so that the thread can exit the enclave later. Note that the child thread has its own execution path differentiating from the parent one. RATEL hence bridges its return address to the point in the code cache that a new thread always starts. After the thread is initialized, we explicitly update DynamoRIO data structures to record the new thread (e.g., the TLS base for application libraries) This way, DynamoRIO is aware of the new thread and can control its execution in the code cache.
Propagating Implicit Changes & Metadata. Thread uses exit/exit_group syscall for terminating itself. Then the OS zeros out the child thread ID (cttid). In RATEL, we explicitly create a new thread inside the enclave, so we have to terminate it explicitly by zeroing out the pointers to the IDs. Further, we clean up and free the memory associated with each thread inside and outside the enclave.

VI. EVALUATION

We primarily evaluate the compatibility of RATEL and highlight the advantages gained due to binary compatibility. We further provide a TCB breakdown of RATEL and point out the performance ramifications, which are common and comparable to state-of-the-art other approaches.

Setup. All our experiments are performed on a Lenovo machine with SGX v1 support, 128 MB EPC configured in the BIOS of which 96 MB is available for user-enclaves, 12 GB RAM, 64 KB L1, 256 KB L2, 4096 KB L3 cache, 3.4GHz processor speed. Our software setup comprises Ubuntu version 16.04, Intel SGX SDK v2.1, PSW v2.1, driver v1.5, gcc v5.4.0, DynamoRIO v6.2.17. All performance statistics reported are the geometric mean over 5 runs.

A. Compatibility

Selection Criteria. We select 310 binaries that cover an extensive set of benchmarks, utilities, and large-scale applications. They comprise commonly used evaluations target for DynamoRIO and enclave-based systems [3], [10], [17], [21], [33], [65], [66] that we surveyed for our study. Further, they represent a mix of memory, CPU, multi-threading, network, and file I/O workloads. Our 69 binaries are from micro-benchmarks targets: 29 from SPEC2006 (CPU), 1 from IOZone (I/O) v3.487, 9 from FSCQ v1.0 (file API), 21 from HBenchOS v1.0 (system stress-test), and 9 from Parsec-SPLASH2 (multi-threading). We run 12 binaries from 3 real-world applications—cURL v7.65.0 (server-side utilities), SQLite v3.28.0 (database), Memcached v1.5.20 (key-value store), and 9 applications from Privado (secure ML framework). We test 220 Linux utilities from our system’s /bin and /usr/bin directories.

Porting Efforts. For benchmarks and applications, we download the source code and compile them with default flags required to run them natively on our machine. We directly use the existing binaries for Linux utilities. We test the same binaries on native hardware, with DynamoRIO, and with RATEL. Thus, we do not change the original source-code or the binaries. We test the target binaries on native Linux and on vanilla DynamoRIO. 278/310 of targets execute successfully with these baselines.

The remaining 32 binaries either use unsupported devices (e.g., NTFS) or do not run on our machine. So we discard them from our RATEL experiments, since vanilla DynamoRIO also does not work on them. Of the remaining 278 binaries that work on the baselines, RATEL has support for the system calls used by 203 of these. We support all of these and directly execute them with RATEL, with zero porting effort.

System Call Support & Coverage. RATEL supports a total of 212/218 (66.66%) sycalls exposed by the Linux Kernel. We emulate 6 sycalls purely inside the enclave and delegate 193 of them via OCALLs. For the remaining 13, we use partial emulation and partial delegation. Table II gives a detailed

| Subsystem                      | Total | Impl | Implementation Covered |
|--------------------------------|-------|------|------------------------|
| File name or descriptor based | 19    | 9    | 9                      |
| File descriptor based         | 65    | 53   | 48                     |
| Inter process communication   | 12    | 4    | 0                      |
| File descriptor or descriptor based | 19 | 9    | 9                      |
| Networks                      | 19    | 17   | 15                     |
| Misc                           | 124   | 79   | 79                     |
| Total                         | 318   | 212  | 193                    |
breakdown of our syscall support. Syscall usage is not uniform across frequently used applications and libraries [70]. Hence we empirically evaluate the degree of expressiveness supported by RATEL. For all of the 278 binaries in our evaluation, we observe total 121 unique syscalls, RATEL supports 115 of them. Table II shows the syscalls supported by RATEL and their usage in our benchmarks and real-world applications (See Appendix A).

Figure 6a and 6b show the distribution of unique syscalls and their frequency as observed over binaries supported by RATEL. Thus, our empirical study shows that RATEL supports 115/121 (95.0%) syscall observed in our dataset of binaries. To support 212 syscalls, we added 3233 LoC (10 LoC per syscall on average). In the future, RATEL can be extended to increase the number of supported syscalls.

Table III summarizes the breakdown of the LoC included in the trusted components of the PSW, SDK, and DynamoRIO as well as the code contributed by each of the sub-systems supported by RATEL. Original DynamoRIO comprises 353,139 LoC. We reduce it to 129,875 LoC (trusted) and 66,629 LoC (untrusted) by removing the components that are not required or used by RATEL. Then we add 8,589 LoC to adapt DynamoRIO to SGX as per the design outlined in Section IV. Apart from this, as described in Section V, we change the libraries provided by Intel SGX (SDK, PSW, Linux driver) and add 1,078 LoC.

Library vs Binary Compatibility. We maintain full binary compatibility with all 203 binaries tested for which we had system call support in RATEL. For them, RATEL works out-of-the-box in our experiments. We report that, given the same inputs as native execution, RATEL produces same outputs. With the aim of true binary compatibility, RATEL supports binaries without limiting them to a specific implementation or version of libc. To empirically demonstrate that our binary compatibility is superior, we test RATEL with binaries that use different libc implementations. Specifically, we compile HBenchOS benchmark (12 binaries) with glibc v2.23 and musl libc v1.2.0. We report that RATEL executes these system stress workloads out-of-the-box with both the libraries. We do not make any change to our implementation. Lastly, we report our experience on porting our micro-benchmarks to a state-of-the-art library-OS called Graphene-SGX in Appendix B.

Table III (columns 2-4) summarizes the breakdown of the LoC included in the trusted components of the PSW, SDK, and DynamoRIO as well as the code contributed by each of the sub-systems supported by RATEL. Original DynamoRIO comprises 353,139 LoC. We reduce it to 129,875 LoC (trusted) and 66,629 LoC (untrusted) by removing the components that are not required or used by RATEL. Then we add 8,589 LoC to adapt DynamoRIO to SGX as per the design outlined in Section IV. Apart from this, as described in Section V, we change the libraries provided by Intel SGX (SDK, PSW, Linux driver) and add 1,078 LoC.

B. TCB Breakdown

Since we aim to run applications inside enclaves, we trust Intel SGX support software (SDK, PSW) that allows us to interface with the hardware. This choice is same as any other system that uses enclaves. RATEL comprises one additional trusted components i.e., DynamoRIO. Put together, RATEL amounts to 277,803 LoC TCB. This is comparable to existing SGX frameworks that have 100K to 1M LoC [3], [17], but only provide library-based compatibility.

Table III (columns 2-4) summarizes the breakdown of the LoC included in the trusted components of the PSW, SDK, and DynamoRIO as well as the code contributed by each of the sub-systems supported by RATEL. Original DynamoRIO comprises 353,139 LoC. We reduce it to 129,875 LoC (trusted) and 66,629 LoC (untrusted) by removing the components that are not required or used by RATEL. Then we add 8,589 LoC to adapt DynamoRIO to SGX as per the design outlined in Section IV. Apart from this, as described in Section V, we change the libraries provided by Intel SGX (SDK, PSW, Linux driver) and add 1,078 LoC.

Of the 277,803 LoC of trusted code, 123,322 LoC is from the original DynamoRIO code base responsible for loading the binaries, code-cache management, and syscall handling. 110,848 LoC and 37,080 LoC are from Intel SGX SDK and PSW respectively. RATEL implementation adds only 6,553 LoC on top of this implementation. A large fraction of our added TCB (27.5%) is because of the OSCALL wrappers that are amenable to automated testing and verification [37], [66].
TABLE IV: RATEL statistics for benchmarks and real-world applications. Columns 2–3: total application LoC and binary size. Columns 4–7: total OCALLs, system calls, pagefaults, and context switches during one run. Columns 8–9: execution time on vanilla DynamoRIO and RATEL. Column 10: RATEL’s execution overhead of RATEL w.r.t. DynamoRIO. RATEL performs better than DynamoRIO in some cases because of eager binary loading which improves cache hits.
Rest of the 4,752 LoC are for memory management, handling signals, TLS, and multi-threading interface.

RATEL relies on, but does not trust, the code executing outside the enclave in the host process (e.g., OCALLs). This includes 2,391 LoC changes, Table III (columns 6-10).

C. Performance Analysis

RATEL explicitly trades-off performance for secure and complete mediation, by design. We present the performance implications of these design choices. We have two main findings. First, the performance overheads vary significantly based on the application workload. Second, we find that most of the overheads come stem from the specific SGX restrictions R1-R5 and due to limited physical memory available.

To measure these, we collect various statistics of the execution profile of 58 program in our micro-benchmarks and 4 real-world applications (12 binaries in total). Specifically, we log the target application LoC, binary size, number of OCALLs, ECALLs, syscalls, enclave memory footprint (stack and heap), number of page faults, and number of context switches. Table IV shows these statistics for the benchmarks and applications evaluated with RATEL. Interested readers can refer to Appendix C, D for detailed performance breakdowns. There are three main avenues of overhead costs.

First, fundamental limitations of SGX result in increased memory-to-memory operations (e.g., two-copy design) or usage of slower constructs (e.g., spin-locks instead of fast futexes). Our evaluation on system stress workloads for each subsystem measure the worst-case cost of these operations. We report that on an average, SPEC CPU benchmarks result in 40.24% overheads (Figure 8a), while I/O-intensive workloads cost 75% slowdown (Figure 8c for IOZone benchmarks). Further, the performance overheads increases with larger I/O record sizes. The same is observed for HBenchOS binaries as reported in Table V. The expensive spin-locks incur cost that increases with number of threads (Figure 8b for Parsec-SPLASH2 benchmarks). Overall, we observe that benchmarks that require large memory copies consistently exhibit significant slow-downs compared to others, highlighting the costs imposed by the two-copy design. The cost of signal handling also increases due to added context saves and restores in RATEL, as seen in a dedicated benchmark of HBenchOS (see last two rows in Table V).

We believe some of these observed costs will be common to other compatibility engines, while the remaining stem from our preference for binary compatibility in designing RATEL. As an example, our evaluation on Graphene-SGX (Appendix B) shows memory-intensive workloads exhibit a similar increase in overheads. Graphene-SGX does not use spin-locks and tunnels all signal handling through futexes). Our evaluation on system stress workloads for each subsystem measure the worst-case cost of these operations. We report that on an average, SPEC CPU benchmarks result in 40.24% overheads (Figure 8a), while I/O-intensive workloads cost 75% slowdown (Figure 8c for IOZone benchmarks). Further, the performance overheads increases with larger I/O record sizes. The same is observed for HBenchOS binaries as reported in Table V. The expensive spin-locks incur cost that increases with number of threads (Figure 8b for Parsec-SPLASH2 benchmarks). Overall, we observe that benchmarks that require large memory copies consistently exhibit significant slow-downs compared to others, highlighting the costs imposed by the two-copy design. The cost of signal handling also increases due to added context saves and restores in RATEL, as seen in a dedicated benchmark of HBenchOS (see last two rows in Table V).

We believe some of these observed costs will be common to other compatibility engines, while the remaining stem from our preference for binary compatibility in designing RATEL. As an example, our evaluation on Graphene-SGX (Appendix B) shows memory-intensive workloads exhibit a similar increase in overheads. Graphene-SGX does not use spin-locks and tunnels all signal handling through futexes). Our evaluation on system stress workloads for each subsystem measure the worst-case cost of these operations. We report that on an average, SPEC CPU benchmarks result in 40.24% overheads (Figure 8a), while I/O-intensive workloads cost 75% slowdown (Figure 8c for IOZone benchmarks). Further, the performance overheads increases with larger I/O record sizes. The same is observed for HBenchOS binaries as reported in Table V. The expensive spin-locks incur cost that increases with number of threads (Figure 8b for Parsec-SPLASH2 benchmarks). Overall, we observe that benchmarks that require large memory copies consistently exhibit significant slow-downs compared to others, highlighting the costs imposed by the two-copy design. The cost of signal handling also increases due to added context saves and restores in RATEL, as seen in a dedicated benchmark of HBenchOS (see last two rows in Table V).
memcached

when applications reach a critical point in memory usage as in Figure 7b. We observe similar loss of latency and throughput for these applications in Appendix D. Similarly, when we execute varying sizes of ML models that require increasing size of code page memory, we observe increase in page faults and lowered performance (Figure 7d). Detailed performance breakdown for these applications is in Appendix D.

The added overhead is solely because of RATEL is the cost of dynamic binary translation itself. In the original DynamoRIO, the DBT design achieves close to native or better after the code-caches warm up [11]. In RATEL, we expect to preserve the same performance characteristics as DynamoRIO. However, the SGX physical memory limits directly impact the execution profile of DynamoRIO running in the enclave. Specifically, RATEL may result in an increase in physical memory for its own execution that may slow-down the target binary. It is difficult to directly measure the exact cost incurred by this factor because we cannot increase the hardware physical memory in our setup.

Lastly, we observe that the performance costs variation based on workloads are common to other platforms. As a direct comparison point, we tested HBenchOS—a benchmark with varying workloads—with Graphene-SGX. Graphene-SGX is a popular and well-maintained library-OS has been under active development for several years as of this writing. Interested readers can refer to Appendix B, D for details. RATEL offers better binary compatibility as opposed to Graphene-SGX which provides compatibility with glibc.

VII. RELATED WORK

Several prior works have targeted SGX compatibility. There are two main ways that prior work has overcome these challenges. The first approach is to fix the application interface. The target application is either re-compiled or is re-linked to use such interfaces. The approach that enables the best compatibility exposes specific Libc (glibc or musl libc) versions as interfaces. This allows them to adapt to SGX restrictions at a layer below the application. Container or libraryOS solutions use this to execute re-compiled/re-linked code inside the enclave as done in Haven [6], Scone [3], Graphene-SGX [17], Ryoan [35], SGX-LKL [58], and Occlum [61]. Another line of work is compiler-based solutions. They require applications to modify source code to use language-level interface [28], [50], [64], [73].

Both style of approaches can have better performance than RATEL, but require recompiling or relinking applications. For example, library OSES like Graphene-SGX and containerization engines like Scone expose a particular glibc and musl version that applications are asked to link with. New library versions and interfaces can be ported incrementally, but this creates a dependence on the underlying platform interface provider, and incurs a porting effort for each library version. Applications that use inline assembly or runtime code generation also become incompatible as they make direct access to system calls, without using the API. RATEL approach of handle R1-R5 comprehensively offers secure and complete mediation, without any assumptions about specific interfaces beyond that implied by binary compatibility.

Security Considerations. As in RATEL, other approaches to SGX compatibility eventually have to use OCALLs, ECALLs, and syscalls to exchange information between the enclave and the untrusted software. This interface is known to be vulnerable [18], [71]. Several shielding systems for file [15], [66] and network IO [5], provide specific mechanisms to safeguard the OS interface against these attacks. For security, defense techniques offer compiler-based tools for enclave code for memory safety [41], ASLR [60], preventing controlled-channel leakage [62], data location randomization [8], secure page fault handlers [56], and branch information leakage [33].

Performance. Several other works build optimizations by modifying existing enclave-compliant library OSES. One such example is Hotcalls [74], Eleos [55] which add exit-less calls to reduce the overheads of OCALLs. These well-known optimizations are also available as part of the default Intel SGX SDK now.

Language Run-times. Recent body of work has also shown how executing either entire [72] or partial [20] language runtimes inside an enclave can help to port existing code written in interpreted languages such as Python [48], [59], Java [20], web-assembly [31], Go [30], and JavaScript [12].

Programming TEE Applications. Intel provides a C/C++ SGX software stack which includes a SDK and OS drivers for simulation and PSW for running local enclaves. There are other SDKs developed in memory safe languages such as Rust [28], [50], [73]. Frameworks such as Asylo [4], OpenEnclave [54], and MesaTEE [49] expose a high-level front-end for writing native TEE applications using a common interface. They support several back-end TEEs including Intel SGX and ARM TrustZone. Our experience will help them to sidestep several design challenges as well as improve their forward compatibility.

Future TEEs. New enclave TEE designs have been proposed [15], [23], [26], [42], [65]. Micro-architectural side channels [7] and new oblivious execution capabilities [23], [45] are significant concerns in these designs. Closest to our underlying TEE is the recent Intel SGX v2 [1], [46], [75]. SGX v2 enables dynamically memory and thread management inside the enclave, thus addressing F2 to some extent. The other restrictions are largely not addressed in SGX v2, and therefore, RATEL design largely applies to it as well. Designing envelope TEEs that do not place the same restrictions as SGX remain promising future work.
VIII. Conclusion

We present the design of RATEL, the first work to offer binary compatibility with existing software on SGX. RATEL is a dynamic binary translation engine inside SGX enclaves on Linux. Through the lens of RATEL, we expose the fundamental trade-offs between performance and ensure secure mediation on the OS-enclave interface. These trade-offs are rooted in 5 SGX design restrictions, which offer concrete challenges to next-generation enclave TEE designs.

Acknowledgments

We thank David Kohlbrenner, Zhenkai Liang, and Roland Yap for their feedback on improving earlier drafts of the paper. We thank Shipra Shinde for help on formatting the figures in this paper. This research was partially supported by a grant from the National Research Foundation, Prime Ministers Office, Singapore under its National Cybersecurity R&D Program (TSUNAMI project, No. NRF2014NCRNCR001-21) and administered by the National Cybersecurity R&D Directorate. This material is in part based upon work supported by the National Science Foundation under Grant No. DARPA N66001-15-C-4066 and Center for Long-Term Cybersecurity. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of the National Science Foundation.

Availability

RATEL implementation, including modified Intel SGX SDK, PSW, and driver, is available at [https://ratel-enclave.github.io](https://ratel-enclave.github.io). Our project webpage and GitHub repository also contains unit tests, benchmarks, Linux util, and case studies evaluated in this paper.

References

[1] Software Guard Extensions Programming Reference Rev. 2. software.intel.com/sites/default/files/329298-002.pdf. Oct 2014.
[2] Aex vector error graphene. https://github.com/oscarlab/graphene/issues/1135.
[3] Sergei Arnaout, Bohdan Trach, Franz Gregor, Thomas Knauth, Andre Martin, Christian Priebke, Joshua Lind, Divya Muthukumaran, Daniel O’Keefe, Mark L Stillwell, David Goltzsche, Dave Eyers, Rüdiger Kapitza, Peter Pietzuch, and Christof Fetzer. SCONE: Secure Linux Containers with Intel SGX. In OSDI, 2016.
[4] Google asylo: An open and flexible framework for enclave applications. https://asylo.dev/. 2019.
[5] Pierre-Louis Aubin, Florian Kelbert, Dan OKeefe, Divya Muthukumaran, Christian Priebke, Joshua Lind, Robert Krahn, Christof Fetzer, David M. Eyers, and Peter R. Pietzuch. Talos : Secure and transparent tls termination inside sgx enclaves, 2017.
[6] Andrew Baumann, Marcus Peinado, and Galen Hunt. Shielding Applications from an Untrusted Cloud with Haven. In OSDI, 2014.
[7] Thomas Bourgeat, Ilia A. Lebedev, Andrew Wright, Sizhuo Zhang, Arvind, and Srinivas Devadas. Mfe: Secure Enclaves in a Speculative Out-of-Order Processor. In MICRO, 2019.
[8] Ferdinand Brasser, Srđjan Ćapkun, Alexandra Dmitrienko, Tommaso Frassetto, Kari Kostiainen, Urs Müller, and Ahmad-Reza Sadeghi. DR.SGX: hardening SGX enclaves against cache attacks with data location randomization. CoRR, abs/1709.09917, 2017.
[9] Aaron B. Brown. HBench-OS Operating System Benchmarks. https://www.eecs.harvard.edu/margo/papers/signetics97-os/hbench/, 2019.
[10] D. Bruening and Q. Zhao. Practical memory checking with dr. memory. In International Symposium on Code Generation and Optimization (CGO 2011), 2011.
[11] Derek Bruening, Evelyn Duesterwald, and Saman Amarasinghe. Design and implementation of a dynamic optimization framework for windows. In ACM Workshop on Feedback-Directed and Dynamic Optimization, Austin, Texas, Dec 2001.
[12] Derek Bruening, Timothy Garnett, and Saman Amarasinghe. An infrastructure for adaptive dynamic optimization. In Proceedings of the International Symposium on Code Generation and Optimization: Feedback-Directed and Runtime Optimization, CGO 03, 2003.
[13] Derek Bruening and Qin Zhao. Practical memory checking with dr. memory. In Proceedings of the IEEE/ACM International Symposium on Code Generation and Optimization, 2011.
[14] Derek L. Bruening and Saman Amarasinghe. Efficient, Transparent, and Comprehensive Runtime Code Manipulation. PhD thesis, USA, 2004. AAI0807735.
[15] Dorian Burihabwa, Pascal Felber, Hugues Mercier, and Valerio Schiavoni. Sgx-fs: Hardening a file system in user-space with intel sgx. In 2018 IEEE International Conference on Cloud Computing Technology and Science (CloudCom), pages 67–72. IEEE, 2018.
[16] D. Champagne and R. B. Lee. Scalable architectural support for trusted software. In HPCA - 16 2010 The Sixteenth International Symposium on High-Performance Computer Architecture, pages 1–12, Jan 2010.
[17] Chia the Tsai, Donald E. Porter, and Mona Vij. Graphene-sgx: A practical library OS for unmodified applications on SGX. In 2017 USENIX Annual Technical Conference (USENIX ATC 17), pages 645–658, Santa Clara, CA, 2017. USENIX Association.
[18] Stephen Checkoway and Hovav Shacham. Iago attacks: Why the system call api is a bad untrusted rpc interface. In Proceedings of the Eighteenth International Conference on Architectural Support for Programming Languages and Operating Systems, ASAPLOS ’13, 2013.
[19] Haogang Chen, Daniel Ziegler, Tej Chajed, Adam Chipalapa, M. Frans Kaashoek, and Nickolai Zeldovich. Using crash hoare logic for certifying the fsgx file system. In Proceedings of the 25th Symposium on Operating Systems Principles, SOSP ’15, 2015.
[20] Tsai Chia-Che, Jeongseok Son, Bhushan Jain, John McAvey, Raluca Ada Popa, and Donald E. Porter. Civet: An efficient java partitioning framework for hardware enclaves. In 29th USENIX Security Symposium (USENIX Security 20), Boston, MA, August 2020. USENIX Association.
[21] JaeWoong Chung, Michael Dalton, Hari Kannan, and Christos Kozyrakis. Thread-safe dynamic binary translation using transactional memory. In 2008 IEEE 14th International Symposium on High Performance Computer Architecture, 2008.
[22] Victor Costan and Srinivas Devadas. Intel sgx explained. Cryptology ePrint Archive, Report 2016/086, 2016. http://eprint.iacr.org/2016/086.
[23] Victor Costan, Ilia Lebedev, and Srinivas Devadas. Sanctum: Minimal hardware extensions for strong software isolation. In USENIX Security ’16.
[24] curl Home Page. https://curl.haxx.se/, 2019.
[25] Github - zwimer/drshadowstack: A software defined dynamic shadow stack utilizing dynamorio. https://github.com/zwimer/DrShadowStack.
[26] Andrew Ferraiuolo, Andrew Baumann, Chris Hawblitzel, and Bryan Parno. Komodo: Using verification to disentangle secure-enclave hardware from software. In SOSP, 2017.
[27] File map error graphene. https://github.com/oscarlab/graphene/issues/435.
[28] fortanix-rust-sgx: The fortanix rust enclave development platform. https://github.com/fortanix/rust-sgx.
[29] Tal Garfinkel, Mendel Rosenblum, and Dan Boneh. Flexible OS support and applications for trusted computing. In Michael B. Jones, editor, Proceedings of HotOS’03: 9th Workshop on Hot Topics in Operating Systems, May 18-21, 2003, Lahue (Kauai), Hawaii, USA. USENIX, 2003.
[30] Adrien Ghosn, James R. Larus, and Edouard Bugnion. Secured routines: Language-based construction of trusted execution environments. In 2019 USENIX Annual Technical Conference (USENIX ATC 19). USENIX Association, July 2019.
[31] David Goltzsche, Manuel Nieke, Thomas Knauth, and Rüdiger Kapitza. Acctee: A webservice-based two-way sandbox for trusted resource accounting. In Middleware, 2019.
[32] David Goltzsche, Colin Wulf, Divya Muthukumaran, Konrad Rieck, Peter Pietzuch, and Rüdiger Kapitza. Trustjs: Trusted client-side execution platform. In Middleware, 2016.
[33] Karan Grover, Shruti Tople, Shweta Shinde, Ranjita Bhagwan, and Ramachandran Ramjee. Privado: Practical and secure dnn inference with enclaves, 2018.
A. Details of Compatibility Tests with RATEL

Linux Utilities. We test the compatibility offered by RATEL with all the Linux built-in binaries on our experimental Ubuntu system. These comprise 229 shared-objected binaries in total, which are typically in the directories /bin and /usr/bin.

We run each utility with the most representative options and outputs. Out of 229, our test machine natively and with DynamoRIO work with 195. Of these 195 binaries, a total of 138 have all system calls presently supported in RATEL, all of which worked correctly in our tests out-of-the-box. The 57 programs that did not work fail for 2 reasons: missing syscall support and virtual memory limits imposed by SGX. Table VII and Table VIII list all Linux utilities and binaries from real-world applications and benchmarks that ran successfully, and present the number of unique system calls for each. Table VII and Table VIII summarize the reasons for all binaries that fail in RATEL and in native and DynamoRIO, respectively.

45 of the failing utilities are due to lack of multi-processing (fork) support in RATEL. 5 utilities use certain POSIX signals for which we have not supported completely (e.g., real-time signals SIGRTMIN + n.). 6 utilities fail because they invoke other unsupported system calls in RATEL, most of which the restriction R3 in SGX fundamentally does not permit (e.g., shared memory syscalls such as shmat, shmdt, shmctl, etc.). 1 utility fails because of the virtual memory limit in SGX, as it loads more than 100 shared libraries. It should be noted that the ioctl syscall involves more than 100 variable parameters, RATEL syscall stubs currently does not cover all of them.

Other Benchmarks & Applications. From the 81 binaries from micro-benchmarks and real applications, 7 do not work with RATEL. 5 binaries from HBenchOS (lat_proc, lat_pipe, lat_CTX, lat_CTX2, bw_pipe) either use fork or shared memory system calls disallowed by R3. 2 binaries (lat_memszie from HBenchOS, mcf from SPEC2006) with DynamoRIO require virtual memory larger than SGX limits on our experimental setup.

B. Comparison to Graphene-SGX

To compare RATEL’s binary compatibility and performance with other approaches, we have chosen Graphene-SGX, a library-OS which runs inside SGX enclave. Graphene-SGX offers the lowest compatibility barrier of all prior systems to our knowledge, specifically offering compatibility with glibc.

Compatibility. Applications using Graphene-SGX have to work only with a specific library interface, namely a custom glibc, which requires re-linking and build process changes. RATEL, in contrast, has been designed for binary compatibility which is a fundamental difference in design. To demonstrate the practical difference, we reported in Section VI-A that HBenchOS benchmark works out-of-the-box when if built with both glibc and musl, as an example.

Graphene-SGX requires a manifest file for each application, that specifies the main binary name as well as dynamic-libraries, directories, and files used by the application. By default Graphene-SGX does not allow creation of new files during runtime. We use the allow_file_creation to disable this default. We tested all 77 benchmark and application binaries (HBench-OS, Parsec-SPLASH2, SPEC, IOZone, FSCQ, SQLite, CURL, Memcached, Privado), out of which 64 work with Graphene-SGX. Of the 13 that fail on Graphene-SGX, all except 1 work on RATEL, with the only failure being due to virtual memory limits.

For Graphene-SGX, 3/9 Parsec-SPLASH2 binaries (water_square, waterSpatial and volrend) failed due to I/O error, (e.g., 27) which is an open issue. 3/25 binaries from SPEC2006 failed. Graphene-SGX fails for cactusADM due failed due to a signal failure, which is mentioned as an existing open issue on its public project page [2]. The omnetpp could not process the input file in-spite of making the input file as allowed in the corresponding manifest file. 4 networking related binaries from HBench-OS namely lat_connect, lat_tcp, lat_udp and bw_tcp could not run, resulting in a “bad address” error while connecting to localhost. lat_memszie from HBench-OsS fails on Graphene-SGX as it fails on RATEL too due to the virtual memory limit.

Performance. We report the performance overheads of Graphene-SGX for HBenchOS benchmarks in Table IX as compared to DynamoRIO baseline and RATEL. The slowdown in both the systems is comparable for I/O benchmarks, since both of them incur two copies. Graphene-SGX is significantly faster than DynamoRIO baseline and RATEL for system call and signal handling, because it implements an library OS inside the enclave and avoids expensive context switches. RATEL delegates most of the system calls to the OS and does not emulate it like Graphene-SGX, offering compatibility with multiple libraries in contrast. Further, RATEL offers instruction-level instrumentation capability.

C. Performance: Micro-benchmarks

We measure the performance for targeted workloads that stress system APIs, CPU, and IO. The breakdown helps is to explain the costs associated with executing diverse workloads with RATEL.

Methodology For each target binary, we record the execution time in two following settings:

- Baseline (DynamoRIO). We execute the application binary directly with DynamoRIO.
- RATEL. We use RATEL to execute the application binary in enclave. We offset the execution time by deducting the overhead to create, initialize, load DynamoRIO and the application binary inside the enclave, and destroy the enclave.

System Stress Workloads. We use HBench-OS [9]—a benchmark to measure the performance of primitive functionality provided by an OS and hardware platform. In Table IX we show the cost of each system-level operation such as system calls,
TABLE VI: List of GNU utilities (138) tested with RATEL along with the number of unique system calls called during a single run.

| Utility | # of syscalls | Utility | # of syscalls | Utility | # of syscalls | Utility | # of syscalls | Utility | # of syscalls | Utility | # of syscalls |
|---------|---------------|---------|---------------|---------|---------------|---------|---------------|---------|---------------|---------|---------------|
| ed      | 18            | pppd    | 29            | dismrg  | 21            | hciotol | 20            | systemcl | 32            | systemd-cgtp | 25            |
| cvt     | 13            | epsnp   | 21            | bcahome | 21            | vim basic | 20            | systemd-escape | 25            | systemd-escape | 13            |
| eqn     | 36            | eslam   | 13            | epdflf  | 15            | btattach | 18            | system-escape | 18            | system-escape | 18            |
| gff     | 18            | gnfconf | 15            | fswapd  | 18            | bfrty-cb | 21            | system-escape | 19            | system-escape | 19            |
| pic     | 13            | aconvec | 25            | fswaps  | 19            | bfrty-cb | 21            | system-escape | 19            | system-escape | 19            |
| tbl     | 13            | hex2cid | 24            | fupdate | 15            | fswaps  | 19            | system-escape | 19            | system-escape | 19            |
| xad     | 14            | btmung  | 24            | fupdate | 15            | fswaps  | 19            | system-escape | 19            | system-escape | 19            |
| curl    | 32            | btselcl | 37            | fupdate | 15            | fswaps  | 19            | system-escape | 19            | system-escape | 19            |
| derb    | 23            | catman  | 16            | fupdate | 15            | fswaps  | 19            | system-escape | 19            | system-escape | 19            |
| find    | 27            | cd-diffl | 21          | lexspace | 13            | fupdate | 15            | system-escape | 19            | system-escape | 19            |
| gawk    | 25            | expary  | 15            | lexspace | 13            | fupdate | 15            | system-escape | 19            | system-escape | 19            |
| grep    | 21            | genrule | 14            | manpatch | 14           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| fcop    | 26            | genrule | 14            | manpatch | 14           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| kmod    | 17            | gottrty | 14            | maspace  | 14           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| pppd    | 30            | lppplat | 20            | maupdate | 14           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| pgpd    | 30            | lannom  | 23            | MAKEO v  | 14           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| gpf    | 14           | pshbok  | 20            | maupdate | 14           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| pgf2    | 27           | pstpos  | 21            | mus-update | 20           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| wget    | 29           | rtestc  | 25            | nss-update | 20           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| bmon    | 23           | soellem | 12            | nephvrm   | 27          | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| gauth   | 13           | whatis  | 20            | nshell    | 15           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| grops   | 14           | fcommm  | 19            | nshell    | 15           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |
| mandb   | 27           | btselcl | 19            | nshell    | 15           | fwupdate | 19            | system-escape | 19            | system-escape | 19            |

TABLE VII: List of applications (12) and individual programs (63) tested with RATEL along with the number of unique system calls used during a single run.

| Property | Sub-property | Performance |
|----------|--------------|-------------|
| Utility  |             |             |
| gcc      | dealII       | lesiu3d     |
| fmm      | soplex       | calculex    |
| curl5    | povray       | GemAllTD    |
| nmc      | barsn        | specrland   |
| namd     | ionome       | specrland   |
| bzip2    | lat_fs       | lenteppet   |
| gobnum   | bwzipcode    | vgg9apap    |
| hammer   | b2zip        | yarrcmap    |
| sjeng    | onemotep     | ocean_cmap  |
| tonto    | gromacs      | volocard    |
| aster    | lat_jig      | bw_bzrzo    |
| sglite   | lat_jcpc     | bw_mmap     |
| zensmp   | lat_judp     | bw_mmap     |

TABLE IX: Summary of reasons for failure of all 38 unsuccessful binaries tested with native and DynamoRIO.

| Reason category | # of the unsuccessful | Case examples |
|-----------------|-----------------------|---------------|
| Memory leak     | 16                    | mtr-3g, mtr-3g-probe, mtr-3g-accurate, etc. |
| Scanner related | 3                     | sdn-find-scanner, scannermiş, etc. |
| Failure in native run | 5                  | memex, cd-create-profile, and varbose from SPEC2006, etc. |
| Failure in DynamoRIO run | 8               | ssh, ssh-keygen, dig, etc. |

TABLE X: Summary of HbenchOS benchmark results for Graphene-SGX along with DynamoRIO and RATEL.

| Property | Sub-property | Performance |
|----------|--------------|-------------|
| Memory   | Rare Memory Road | 24974.73 |
| Interest | Buzo Benchmark | 12915.12 |
| Operations | Memory copy libc aligned | 60770.04 |
| Bandwidth (MB/s) | Memory copy libc unaligned | 12915.12 |
| More Iteration | Memory copy libc aligned | 12915.12 |
| Less Chunk | Memory copy unaligned | 12915.12 |
| File Read | 2915.12 |
| File Write | 12915.12 |
| System Read | 74115.12 |
| System Write | 74115.12 |

TABLE VIII: Summary of the reasons for failure of all 64 unsuccessful binaries tested with RATERL.

| Reason category | # of the unsuccessful | Case examples |
|-----------------|-----------------------|---------------|
| Memory leak     | 16                    | mtr-3g, mtr-3g-probe, mtr-3g-accurate, etc. |
| Scanner related | 3                     | sdn-find-scanner, scannermiş, etc. |
| Failure in native run | 5                  | memex, cd-create-profile, and varbose from SPEC2006, etc. |
| Failure in DynamoRIO run | 8               | ssh, ssh-keygen, dig, etc. |

memory operations, context switches, and signal handling. Memory-intensive operation latencies vary with benchmark setting: (a) when the operations are done with more iterations (in millions) and less memory chunk size (4 KB) the performance is comparable; (b) when the operations are done with less iterations (1 K) and less memory chunk size (4 MB) RATERL incurs overhead ranging from 117% to 651%. This happens because when the chunk size is large, we need to allocate and de-allocate memory inside enclave for every iteration as well as copy large amounts of data. These file operation latencies match with latencies we observed in our I/O intensive workloads (Figure [Sc]). Specifically, the write operation incurs large overhead. Hence, the create workload incurs 25% overhead because the bench-
mark creates a file and then writes predefined sized data to it. Costs of system calls that are executed as OCALLs vary depending on return value and type of the system call. For example, system calls such as getpid, sbrk, sigaction that return integer values are much faster. Syscalls such as getusage, gettimeofday returns structures or nested structures. Thus, copying these structures back and forth to/from enclaves causes much of the performance slowdown. RATEL has a custom mechanism for registering and handling signal (Section IV-E), it introduces a latency of 19.71% and 89.11% respectively. Registering signals is cheaper because it does not cause a context switch as in the case of handling the signal. Further, after accounting for the OCALL costs, our custom forwarding mechanism does not introduce any significant slowdown.

CPU-bound Workloads. RATEL incurs 40.24% overhead averaged over 23 applications from SPEC 2006 [67] with respect to DynamoRIO. Table [IV] shows the individual overheads for each application with respect to all baselines. From Table [IV] we observe that applications that incur higher number of page faults and OCALLs suffer larger performance slow-downs. Thus, similar to other SGX frameworks, the costs of enclave context switches and limited EPC size are the main bottlenecks in RATEL.

IO-bound Workloads. RATEL performs OCALLs for file I/O by copying read and write buffers to and from enclave. We measure the per-API latencies using FSCQ suite for file operations [19]. Table [IV] shows the costs of each file operation and file access patterns respectively. Apart from the cost of the OCALL, writes are more expensive compared to reads in general; the multiple copy operations in RATEL amplify the performance gap between them. Next we use IOZone [51], a commonly used benchmark to measure the file I/O latencies. Figure 8c shows the bandwidth over varied file sizes between 16 MB to 1024 MB and record sizes between 4 KB to 4096 KB for common patterns. The trend of writes being more expensive holds for IOZone too. RATEL incurs an average slowdown of 75% over all operations, record sizes, and file sizes.

Multi-threaded Workloads. We use the standard Parsec-SPLASH2 [57] benchmark suite. It comprises a variety of high performance computing (HPC) and graphics applications. We use it to benchmark RATEL overheads for multi-thread applications. Since some of the programs in Parsec-SPLASH2 mandate the thread count to be power to 2 (e.g., ocean_ncp), we fixed the maximum number of threads in our experiment to 16. RATEL changes the existing SGX design to handle thread creation and synchronization primitives, as described in Section IV-C and IV-D. We measure the effect of this specific change on the application execution by configuring the enclave to use varying number of threads between 1-16.

Figure [8b] shows a performance overhead of 83.2%, on average, across all benchmarks and thread configurations. For single-threaded execution, RATEL causes an overhead of 28%. With the increase in threads, it varies from 416%, 910%, 1371%, 1438% respectively. We measure the breakdown of costs and observe that, on average: (a) creating each thread contributes to a fixed cost of 57 ms; (b) shared access to variables becomes expensive by a factor of 1 − 7 times compared to the elapsed time of futex synchronization with increase in number of threads. This is expected because synchronization is cheaper in DynamoRIO execution, in which it uses unsafe futex primitives exposed by the kernel. On the other hand, RATEL uses expensive spinlock mechanism exposed by SGX hardware for security. Particularly, some of the individual benchmarks, such as water_spatial, ffm and raytrace that involve lots of lock contention events and have extremely high frequency of spinlock calls (e.g., the spinning counts of about 423,000 ms in RATEL while the futex calls of about 500 ms in DynamoRIO for the raytrace with 8 threads). Thus, they incur large overheads in synchronization.

D. Performance:Real-world Case-studies

We work with 4 representative real-world applications: a database server (SQLite), a command-line utility (cURL), a machine learning inference-as-a-service framework (Privado), and a key-value store (memcached). These applications have been used in prior work [64].

SQLite is a popular database [68]. We select it as a case-study because of its memory-intensive workload. We configure it as a single-threaded instance. We use a database benchmark workload [43] and measured the throughput (ops/sec) for each database operation with varying sizes of the database (total number of entries). Table [IV] shows the detailed breakdown of the runtime statistics for a database with 10,000 entries. Figure 7c shows the average throughput over all operations. With RATEL, we observe a throughput loss of 25.14% on average over all database sizes. The throughput loss increases with increase in the database size. The drop is noticeable at 500K where the database size crosses the maximum enclave size threshold and results in significant number of page faults. This result matches with observations from other SGX frameworks that report SQLite performance [3].

cURL is a widely used command line utility to download data from URLs [23]. It is network intensive. We test it with RATEL via the standard library test suite. Table [IV] shows detailed breakdown of time execution time on RATEL. We measure the cost executing cURL with RATEL for downloading various sizes of files from an Apache (2.4.41) server on the local network. Figure 7a shows the throughput for various baselines and file sizes. On average, RATEL causes a loss of 142.27% throughput as compared to DynamoRIO. For all baselines, small files (below 100 MB) have smaller download time; larger file sizes naturally take longer time. This can be explained by the direct copying of packets to non-enclave memory, which does not add any memory pressure on the enclave. The only remaining bottleneck in the cost of dispatching OCALLs which increase linearly with the requested file size.

Privado is a machine learning framework that provides secure inference-as-a-service [33]. It comprises of several state of the art models available as binaries that can execute on an input
image to predict its class. The binaries are CPU intensive and have sizes ranging from 313 KB to 140 MB (see Table IV). We execute models from Privado on all the images from the corresponding image dataset (CIFAR or ImageNet) and measure inference time. Figure 7A shows the performance of baselines and RATEL for 9 models in increasing order of binary size. We observe that RATEL performance degrades with increase in binary size. This is expected because the limited enclave physical memory leads to page faults. Hence, largest model (140 MB) exhibit highest inference time and smallest model (313 KB) exhibit lowest inference time. Thus, RATEL and enclaves in general can add significant overheads, even for CPU intensive server workloads, if they exceed the working set size of 90 MB.

Memcached is an in-memory key-value cache. We evaluate it with YCSB’s all four popular workloads A (50% read and 50% update), B (95% read and 5% update), C (100% read) and D (95% read and 5% insert). We run it with 4 default worker threads running in DynamoRIO and RATEL settings. We vary the YCSB client threads with Load and Run operations (to load the data and then run the workload tests, respectively). We fix the data size to 1,000,000 with Zipfian distribution of key popularity. We increase the number of clients from 1 to 100 to find out a saturation point of each targeted/scaled throughput for the settings. Here, we only present workload A (throughput vs average latency for the read and update); the other workloads display similar behavior.

As shown in Figure 7d, the client latencies of the two settings for a given throughput are slightly similar until approximately 10,000 ops/sec. Then, RATEL jitters until it achieves maximum throughput around 17,000 ops/sec, while DynamoRIO is flat until 15,000 ops/sec (the maximum is 21,000 operations per second). The shared reason of the deceleration for both is that DynamoRIO slows down the speed of Read and Update. For RATEL, the additional bottleneck is the high frequency of lock contention with spin-lock primitive. For e.g., RATEL costs 18,320,000 ms while DynamoRIO’s the futex calls cost only around 500 ms for a given throughput of 10000 with 10 clients.