ABSTRACT
Creating high performance implementations of deep learning primitives on CPUs is a challenging task. Multiple considerations including multi-level cache hierarchy, and wide SIMD units of CPU platforms influence the choice of program transformations to apply for performance optimization. In this paper, we present machine learning powered compiler techniques to optimize loop nests. We take a two-pronged approach to code optimization: We first apply high level optimizations to optimize the code to take optimal advantage of the cache memories. Then, we perform low level, target-specific optimizations to effectively vectorize the code to run well on the SIMD units of the machine. For high level optimizations, we use polyhedral compilation techniques and deep learning approaches. For low level optimization, we use a target specific code generator that generates code using vector intrinsics and Reinforcement Learning (RL) techniques to find the optimal parameters for the code generator. We perform experimental evaluation of the developed techniques on various matrix multiplications that occur in popular deep learning workloads. The experimental results show that the compiler techniques presented in the paper achieve 7.6X and 8.2X speed-ups over a baseline for sequential and parallel runs respectively.

1 INTRODUCTION
Deep learning (DL) has become pervasive in various domains of computing. Image recognition [14, 17], language modeling [10], language translation [31], speech recognition [15] make extensive use of deep neural networks (DNNs). Deep Learning inference is an important workload across applications, such as object classification & recognition, text and speech translation etc. A 2018 Mc Kinsey study [5] pointed out that in datacenters, 75% of the inference tasks are run on CPUs. Optimizing DL workloads on CPUs is a challenging proposition because of architectural complexities of CPU platforms. Multi-level cache hierarchies, TLBs (Translation Look-aside Buffers), hardware data prefetchers, SIMD (a.k.a vector) units present particular challenges in writing high performance code. Therefore, the current state-of-practice is to use expert-coded high performance libraries such as Intel oneDNN [3] in deep learning frameworks such as TensorFlow and PyTorch to achieve good performance. However, being reliant on libraries for performance is not scalable. First, it would increase the time-to-market: from the time a new DL operator is invented to its being supported in a library could take a considerable amount of time. Second, even expert programmers must invest significant amount of effort to tune the implementations on the target platforms. Therefore, an attractive alternative solution is to develop compilation techniques that automate code optimization and achieve similar performance levels as expert-coded libraries.

In this paper, we develop a systematic approach to automatic code optimization. We categorize the program optimizations into two phases: high level and low level optimizations. High level optimizations perform loop optimizations such as loop reordering and tiling to derive a loop structure that utilizes the cache hierarchy of the computer system to the fullest extent possible. Low level optimizations generate vector code using the target machine’s intrinsics; reinforcement learning methodology guides the derivation of high performance vector code. For high-level and low-level optimizations we leverage artificial intelligence (A.I.) techniques. We evaluate our automated compiler system on GEMMs which lie at the heart of deep learning [1]. The results indicate our compiler workflow delivers competitive performance compared to Intel oneDNN library and significantly higher performance compared to a state-of-the-art DL compiler, viz., AutoTVM [9].

The contributions of the paper are as follows.
We first describe the overall compiler workflow. We input vectorization strategy for effective use of the SIMD vector matrix-multiplications that occur in the innermost loops of this work, we build the low-level optimizer to optimize the in terms of matrix-multiplication. Matrix multiplication is at the heart of many workloads (MLPs, CNNs, and LSTMs) can be formulated as matrix multiplication using the target-specific vector intrinsics. Further, reordering and tiling transformations are applied and the advantage of the multi-level caches of the CPU platform. The loop techniques we apply for loop optimization.

The iteration space of the loop in Figure 2 is defined as the domain of a relation. The read and write access functions of a loop nest can be defined for a relation that will map well to the hardware architectures. The lexicographical operations on the iteration space are used to illustrate the workings of the data reuse algorithm.

3 HIGH-LEVEL POLYHEDRAL LOOP OPTIMIZATIONS

We use the polyhedral model [11], which is an advanced mathematical framework to reason about dependences and loop transformations, to develop our data reuse algorithm.

3.1 Preliminaries

We use the Integer Set Library (ISL) [27] for performing polyhedral operations in this work and we use the same notation as used in ISL to elucidate the concepts and the algorithm. The matrix multiplication code shown in Figure 2 will be used to illustrate the workings of the data reuse analysis.

A relation is a mapping from input tuple variables to output tuple variables. In addition, a set of constraints can be defined for a relation that will place constraints on the input/output tuple variables. The read and write access functions of a loop nest can be modeled with relations. The read relations in the Figure 2 code are shown below: The sole write relation in the loop is: The domain of a relation is denoted by dom r.

Apply operation. When a relation r is applied on a set s, the domain of r will be intersected with s and the resulting range will be a new set s’.

4 EXPERIMENTAL EVALUATION

We use the Integer Set Library (ISL) [27] for performing polyhedral operations in this work and we use the same notation as used in ISL to elucidate the concepts and the algorithm. The matrix multiplication code shown in Figure 2 will be used to illustrate the workings of the data reuse analysis.

Sets. A set is a tuple of variables along with a collection of constraints defined on the tuple variables.

Relations. A relation is a mapping from input tuple variables to output tuple variables. In addition, a set of constraints can be defined for a relation that will place constraints on the input/output tuple variables.

The read and write access functions of a loop nest can be modeled with relations. The read relations in the Figure 2 code are shown below: The sole write relation in the loop is: The domain of a relation is denoted by dom r.

Apply operation. When a relation r is applied on a set s, the domain of r will be intersected with s and the resulting range will be a new set s’. The set s’ is said to be the result of the apply operation. The operation is mathematically defined as: The data footprint of the loop can be computed by applying read and write relations on the iteration space set: The lexicographical operations. The lexicographical operations can be applied on sets. s1 << s2 outputs all the elements

Loop nest
E.g., gemm
![Diagram](image.png)

The data dependencies of the matrix multiplication code in Figure 2 are shown below. Read-After-Read (RAR), Read-After-Write (RAW, a.k.a. developed in §3.2, we consider four kinds of dependences – involved in the dependence. For cache data reuse analysis expressed as maps from source iterations to target iterations of 𝑠 denoted by 𝑠. The largest element is obtained using

\[ \text{exmin}(s) = \max\{1, j, k : j < k < N \} \]

3.2 Loop transformations

We create a number of code variants by applying loop re-ordering and tiling transformations and using the Polyhedral techniques [25] select the top code variants.

Working set size computation. We perform cache data reuse analysis to characterize a loop-nest’s behavior with respect to a given cache hierarchy. The analysis computes the various existing data reuses of a program and then for the input cache hierarchy determines which data reuses are exploitable at various levels of cache. Each data dependence in a loop is also an instance of data reuse – the source and target iterations involved in the dependence touch the same data element and therefore, the data is reused. For a data dependence and hence data reuse to be realizable in a given level of cache, all the data elements accessed between the source and target iterations of the dependence – the working set – have to be retained in the cache so that when the execution reaches the target iteration, the data element(s) used in the source iteration will still be present in the cache.

We illustrate the computation of the working set sizes using the running example in Figure 2. Let us examine the following dependence carried by the loop arising because of the array reference A[i][k]. The dependence 𝑑₂ is induced by array reference A[i][k]. An element of array A, say A[i][k] which is accessed in source iteration \( [i = 0, j = 0, k = 0] \) gets reused in target iterations \( [i' = 0, j' > 0, k' = 0] \). The source to target iteration relationships such as this are expressed in a parametric fashion as the relation 𝑑₂.

The exact data dependences in Polyhedral dependences. The exact data dependences in loop nests can be computed in the polyhedral model and are expressed as maps from source iterations to target iterations involved in the dependence. For cache data reuse analysis developed in §3.2, we consider four kinds of dependences – Read-After-Read (RAR), Read-After-Write (RAW, a.k.a. flow), Write-After-Read (WAR, a.k.a. anti), and Write-After-Write (WAW). The data dependencies of the matrix multiplication code in Figure 2 are shown below.

\[
\begin{align*}
\text{for } (i = 0; i < M; i++) \{ \\
\quad \text{for } (j = 0; j < N; j++) \{ \\
\quad\quad \text{for } (k = 0; k < K; k++) \{ \\
\quad\quad\quad C[i][j] += A[i][k] \cdot B[k][j]; \\
\quad\quad \} \\
\quad \} \\
\} 
\end{align*}
\]

Figure 2: Matrix multiplication code

of 𝑠₁ that are lexicographically strictly smaller than all the elements of 𝑠₂, while 𝑠₁ <= 𝑠₂ gets us the elements of 𝑠₁ that are lexicographically smaller than or equal to the elements of 𝑠₂. The lexicographically smallest element of a set 𝑠 is queried using lexmin 𝑠. Similarly, the lexicographically largest element is obtained using lexmax 𝑠.

Set difference. The set difference between set 𝑠₁ and 𝑠₂ is denoted by 𝑠₁ \(\setminus\) 𝑠₂, i.e., the resulting set will have elements of 𝑠₁ that do not appear in 𝑠₂.

\[
\begin{align*}
\text{for } (i = 0; i < M; i++) \{ \\
\quad \text{for } (j = 0; j < N; j++) \{ \\
\quad\quad \text{for } (k = 0; k < K; k++) \{ \\
\quad\quad\quad C[i][j] += A[i][k] \cdot B[k][j]; \\
\quad\quad \} \\
\quad \} \\
\} 
\end{align*}
\]
The number of data elements of the three arrays – A, B, C accessed between I_{source} and I_{min,tar} is derived by applying the read and write relations on the intervening iteration set and it is:

\[ WS_{\text{min}} = 2K + 3 \]

The \( K \) elements of array \( A - A[0][0, 1, \ldots, K-1] \), the \( K+1 \) elements of array \( B - B[0, 1, \ldots, K-1][0] \) and \( B[0][0] \), and finally 2 elements of array \( C - C[0][0], C[0][1] \) accessed between the source iteration \( S[i = 0, j = 0, k = 0] \) and the target iteration \( I_{\text{min,tar}} = S[i = 0, j = 1, k = 0] \) lead to the \( WS_{\text{min}} \) size of \( 2K + 3 \).

The maximum working set size – the number of data elements touched between \( I_{\text{source}} \) and \( I_{\text{max,tar}} \) is:

\[ WS_{\text{max}} = N \times K + N + 1 \]

The \( WS_{\text{max}} \) size is arrived at by counting the number of array elements accessed between the source iteration - \( S[i = 0, j = 0, k = 0] \) and the target iteration - \( I_{\text{max,tar}} = \{ S_{j}[i = 0, j = N - 1, k = 0] \} \). As far as array \( A \) is concerned, \( K \) elements of it - \( A[0][0, 1, \ldots, K-1] \) are read. Array \( B \)’s elements - \( B[0, 1, \ldots, K-1][0, 1, \ldots, N-2] \) plus \( B[0][N-1] \) are read which total \( K \times (N - 1) + 1 \). \( N \) elements of array \( C \) are read and written - \( C[0][0, 1, \ldots, N-1] \). Therefore, a total of \( N \times K + N + 1 \) are read and written.

We have built a code generator to emit a number of program variants. The code generator creates the loop variants by applying tiling and loop interchange program transformations. The tile sizes are varied as well. The working set size computation analysis is performed on each program version generated. Among the many variants generated, the ranking algorithm described below picks the top \( k \) best performing versions, where \( k \) is a parameter.

**DNN-based code ranking algorithm.** We assume fully associative, and exclusive caches. If the working set size corresponding to a data reuse in the program is smaller than the cache size then the data reuse is exploitable in the cache. The ranking system considers caches at different levels (typically L1, L2, and L3) and for each data reuse, determines at what level of cache hierarchy is the data reuse realizable. We now describe the algorithm to determine the cumulative working set sizes at each level of cache. The inputs to the algorithm are the working set sizes computed for a loop nest, and the cache sizes of the target system. The algorithm determines the fastest level of cache where the working set size corresponding to each data reuse fits and adds it to that cache’s working set size. If a working set does not fit in any cache, then the data reuse happens out of the main memory. Consequently, the memory’s working set size is updated.

We use a deep neural network (DNNs) for ranking of code variants. For the purposes of training the DNN model, we collect the performance data of code variants generated and compute their working set sizes at different levels of the memory hierarchy. We train the DNN model to perform relative ordering of two code variants. We then use a tournament based ranking system to assign ranks to the different code versions created – we play each code variant against every other code variant. For each variant, we record the number of wins it has accumulated. We then rank the variants based on the number of wins – the higher the number of wins, the higher the rank.

We use a four layer feed forward neural network architecture shown in Figure 3. We normalize the compiler generated working set sizes using min-max scaling: \( \frac{x - x_{\text{min}}}{x_{\text{max}} - x_{\text{min}}} \). Each value is subtracted with the minimum value in that feature column and divided by the feature range. The output layer consists of two neurons and we use the softmax function for the output layer. The values of the two output neurons, because of the use of the softmax function, sum to 1. If the output value is above a threshold - \( \theta \), we consider it a 1, otherwise a 0. If the first neuron fires a 1, then the first variant is considered the winner. If the second neuron fires a 1, then the second variant is considered the winner. If both of them are zero because none of them are above the threshold, then it is a draw between the two variants. In this work, we set the threshold \( \theta \) to 0.7. We experimented with deeper models as well. However, depth beyond four did not have any discernible effect on accuracy.

### 4 LOW-LEVEL TARGET SPECIFIC INNER LOOP OPTIMIZATIONS

The high level optimizations as described in §3 are first applied to the input code and then the inner loops are handed over the low level optimizer. The low level optimizer focuses on vectorization and assumes that the data used by the inner loops is resident in L1 cache. The inner loops are analyzed to find out which loops are parallel and hence, vectorizable. The different vectorizable loops present us multiple choices for vectorization. Further, unroll-and-jam (the loops are unrolled and the unrolled statements are combined in the inner-most
for (i = 0; i < M; i++) {
    for (j = 0; j < N; j+=16) {
        for (k = 0; k < K; k++) {
            C[i][j] += A[i][k] * B[k][j];
            C[i][j+1] += A[i][k] * B[k][j+1];
            C[i][j+2] += A[i][k] * B[k][j+2];
            ...
            C[i][j+15] += A[i][k] * B[k][j+15];
        }
    }
}

M_full = (M / 1) * 1;
N_full = (N / 16) * 16;
K_full = (K / 1) * 1;
for (i = 0; i < M_full; i += 1) {
    for (j = 0; j < N_full; j += 16) {
        vecC = _mm512_load_ps(&C[i*CStride+j]);
        for (k = 0; k < K_full; k += 1) {
            vecA = _mm512_set1_ps(A[i*AStride+k]);
            vecB = _mm512_load_ps(&B[k*BStride+j]);
            vecC = _mm512_fmadd_ps(vecA, vecB, vecC);
        }
        _mm512_store_ps(&C[i*CStride+j], vecC);
    }
}

// The residue code for non-full M, N, K
// values omitted for brevity.

Figure 4: Unrolled GEMM code for unroll factors 1, 16, 1

vectorized code using the vector intrinsics of the target CPU platform. Figure 5 shows the generated code using AVX-512 intrinsics to run on vector units that can work on 512 bits of data simultaneously. The datatype of the variables in the shown code is 32 bit floating point numbers. Therefore, we can perform arithmetic operations on 16 floating point numbers (16 × 32 = 512) at the same time. In Figure 4, we observe that the same array element - “A[i][k]” is used in all 16 arithmetic operations. Therefore, it is broadcast to all elements of the vector register using the _mm512_set1_ps vector intrinsic. The 16 elements of the C array - “C[i][j]” through “C[i][j+15]” are loaded using the _mm512_load_ps vector intrinsic. Since the loaded C elements are reused in all of the inner-most k loop, the loading is hoisted out of the k loop. In a similar fashion, the 16 elements of the B array - “B[k][j]” through “B[k][j+15]” are loaded using the _mm512_load_ps vector intrinsic. The 16 addition and multiplication operations are performed using the fused-multiply-add operation through the intrinsic _mm512_fmadd_ps. After the C vector is accumulated into in the k loop, the results are stored back loop) can present various data reuse opportunities. Thus, the various unroll factors for the loops give rise to multiple ways of vectorizing the loops and we have to select a scheme that leads to the highest performance. To help select the best vectorization parameters, namely, the unroll factors for the loops, we use Reinforcement Learning (RL).

4.1 Vector intrinsic based code generation

We illustrate the workings of the vectorization scheme and the use of RL on GEMM inner loops. Figure 4 shows the matrix multiplication code where the j loop is unrolled by a factor of 16 and the statements are moved to the inner most loop (unroll-and-jam). Because the j loop is parallel, it is vectorizable. We have built a code generator that generates the

Figure 5: Auto-generated GEMM code using AVX-512 intrinsics for unroll factors 2, 16, 2

loop
The choices of unroll factors for the inner loops constitute the state space for reinforcement learning (RL). The agent will suggest whether to increase unroll factors or to decrease them. The increment/decrement of the unroll factors form the actions. The target specific code generator will carry out the actions suggested by the agent by generating code with the new unroll factors and the code is run on the target platform. The actions will either lead to a higher performance or a lower performance vis-à-vis the performance of the prior state. If the action leads to a higher performance, we will encode it as a positive reward – the relative performance increase. If the action causes the performance to degrade, it is denoted as a negative reward – the relative performance decrease. Figure 7 shows the RL set-up.

The agent will use a neural network to suggest next actions to undertake. While the state space exploration is being conducted, we will have two phases – exploration, and exploitation. In the exploration phase, the agent will recommend random actions and the reward obtained will be used to continually train the neural network to predict actions that will lead to larger positive rewards and thus higher performance states. In the exploitation phase, the agent will query the neural network for the best actions – actions that will lead to the biggest rewards. The transitions between the exploration and exploitation phases are controlled by the exploration decay rate. We set it in such a way that at initial stages exploration is selected more often, and later exploitation is chosen more.

We train a neural network to encode the policy for RL – whether to increment the unroll factors or two decrement them. The neural network comprises of six intermediate layers – two blocks of Dense, Batch Normalization and Dropout layers. For Dense layers we use Relu as the activation function. We set the drop-out rate of 0.25 for Dropout layers to avoid overfitting. The output layer is a dense layer which has as many neurons as the number of actions. For matrix multiplication, there are 7 actions possible: 2 actions for each unroll factor (whether to increment or to decrement) and a special state to indicate no further action is necessary.

### 5 EXPERIMENTAL EVALUATION

We evaluate the performance of our compiler framework on the GEMM operation for a range of matrix sizes. The GEMM operation is, \( C = A \times B \) where \( A, B, \) and \( C \) are matrices. Matrix \( C \) is of size \( M \times N \), \( A \) of size \( M \times K \) and \( B \) of size \( K \times N \). We compare our compiler optimizations against three other systems: 1) The matrix multiplication code shown in Figure 2 optimized to the highest levels using the Intel C compiler – icc version 19.1.3.304 with the optimization flag -O3. For parallel runs, we parallelize the outermost – ‘i’ loop with OpenMP pragmas. We consider the resulting performance to be the baseline. 2) The latest version of Intel oneDNN library version v2.2. The oneDNN library is an expert coded library for inter alia, GEMMs. 3) The latest release of TVM [8] v0.7.0. We use the optimization guide published on the TVM website for GEMMs [2] to obtain its performance. Additionally, we tune the performance of TVM by exploring a number of tile sizes and report the best performance among the different tile sizes explored. The experiments are run on

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Figure 7: Reinforcement Learning for target specific low level optimization.
Intel(R) Xeon(R) Platinum 8280 (Cascade Lake) servers running at the frequency of 2.70 GHz. A single socket processor has 28 cores, 32KB private L1 cache, 1MB private L2 cache, and 39MB shared L3 cache.

5.1 Evaluation of Low-level optimizations

We first assess the efficaciousness of the low-level optimization scheme we described in Section 4. To do so, we select matrix sizes such that all the matrices will fit in in the private L1/L2 cache of the processor and thus the code does not require any loop transformations to enhance data locality.

We show the performances achieved on a single core of the Xeon processor in Figure 10 by the ICC compiler – baseline, our toolchain, and the oneDNN library. We run each code a 100 times and report the average performance observed. The baseline performance ranges from 0.18 GFLOPS/s (for M = 16, N = 16, and K = 16) to 7.53 GFLOPS/s (for M = 128, N = 128, and K = 128). The peak performance of a core of the said Xeon system is ~118 GFLOPS/s. Thus, without any further optimizations such as the ones we have described in the paper, we observe that we obtain very low performance. The oneDNN performance for all problem sizes save for M = N = K = 128 is lower than ours. Our toolchain reaches a sizable percentage of the machine’s peak performance. The lowest performance gotten is 39.10 GFLOPS/s for M = N = K = 16, and the highest performance reached is 84.34 GFLOPS/s for M = N = K = 128. As the problem size increases, the work to be performed increases, and due to Instruction Level Parallelism (ILP) and because the SIMD units can be kept more busy, the performance goes up. The experiments show that our target-specific code generation and reinforcement learning scheme is extremely effective in vectorizing the code well.
Figure 9: The speed-ups achieved over the baseline by various systems. The absolute performances in GFLOPS/s obtained by our compiler toolchain for all problem sizes are shown.

5.2 Evaluation of High-level and Low-level optimizations together

We next conduct experiments to evaluate how well our compiler toolchain performs when we need to apply both high-level and low-level optimizations: when matrix sizes are larger and therefore necessitate loop transformations including tiling to enhance data reuse in cache memories. Table 1 lists the matrix sizes we perform the experiments with. The matrix sizes are drawn from various deep learning applications. We note that the matrix sizes are wide ranging and therefore, test the versatility of our system in being able to come up with high performance implementations for varied matrix sizes.

Two-level tiling is applied on the matrix multiplication code. Consequently, there are six tile sizes that need to be selected. We choose the best tile sizes using the high level optimization methodology described in Section 3: We first create a number of code variants by varying the tile sizes. The data reuse analyzer is run on each code variant and it outputs the working set sizes. We execute the code variants on the target machine and measure their performance. The working set sizes and the performance data are used together to train the DNN model for ranking of code variants. While training the model, we use the training data corresponding to 70% of the code variants. Once the model is trained, for each GEMM size, we use the DNN model to select the top 10% best tile sizes from the space of candidate tile sizes. For the top 10% tile sizes thus selected, we apply low-level transformations (Section 4) to vectorize the code.

Figure 9 shows the speed-ups achieved over the baseline by our system, AutoTVM, and oneDNN library for sequential runs. We show the performance obtained by our compiler in absolute terms – in terms of GFLOPS/s for each problem size. When dealing with problem sizes that are odd numbers or when the optimal unroll factor for a loop does not divide the corresponding tile size, then that leads to executing some parts of the computation in scalar mode (and not vectorized). For example, the “residue” code shown in Figure 5. It leads to lower performance compared to when everything is run in the vector mode. For example, for the problem sizes $M = 31999$, $N = 1024$, and $K = 84$, the optimal unroll factors through the high-level and low-level optimizations are determined to be 4, 32, and 1 for the three loops respectively. Because 4 does not divide 31999 exactly, it causes some part of the computation to be run using scalar units. Our toolchain achieves the highest performance of 60.7 GFLOPS/s for the problem size $M = 1632$, $N = 36548$, $K = 1024$. For this problem size, the highest speed-up relative to the baseline code achieved is: 17.96X. The lowest performance of 1.4 GFLOPS/s is observed for $M = 2048$, $N = 1$, $K = 128$. The reason is, vectorization on the “j” loop as shown in Figure 5 is not possible.
because the loop length of the “j” loop is 1. If we were to vectorize on the “i” loop, that will induce non-contiguous data accesses for the A and C matrices and loading of data through vector-loads will not be possible. That explains the low performance when N = 1. We obtain on average (geometric mean) speed-up of 7.6X over the baseline. The speed-ups achieved by the AutoTVM system and the oneDNN library are 4.9X and 13.7X respectively. In 8 out of 10 cases, our compiler outperforms AutoTVM. In oneDNN implementations, data prefetch instructions are carefully inserted. For example, low-level prefetch instructions such as prefetcht0 and prefetcht2 which fetch data to all levels of cache and to L2 cache respectively are used extensively and that minimizes the number of instances when the processor has to wait for the arrival of data from memory. Inter alia, such software data prefetching strategies employed in oneDNN explain its higher performance.

We measure the performance of parallel code when it is run on all 28 cores of the Xeon server. Figure 10 shows the speed-ups over the baseline for the three systems. The baseline code is parallelized as well. The average speed-ups over the baseline for our compiler, AutoTVM, and oneDNN are 8.2X, 5.4X, and 15.3X respectively. For the first two problem sizes, namely M = 128, N = 2048, K = 4096, and M = 320, N = 3072, K = 4096, our compiler delivers higher performance even compared to oneDNN. Our tool achieves the highest performance of 1408 GFLOPS/s for the problem size M = 1632, N = 36548, K = 1024. Incidentally, the highest performance in sequential experiments is seen for the same problem size. For that problem size, it represents the parallel speed-up of 23.2X on a 28-core machine. When the number of tiles of the parallelized loop is not a multiple of the number of cores (28), that leads to slight load imbalance among the cores. Consequently, we are hindered from achieving a perfect linear speed-up as the number of cores is increased.

6 RELATED WORK

In recent years, there has been a renewed interest in the application of Artificial Intelligence (A.I.) techniques for program optimization. The use of A.I. has been explored broadly for two purposes: 1) for program representation in an embedding space [4, 6, 18, 26], and 2) for performance optimization [8, 9, 12, 20, 34, 35]. In the former use case, once a program representation has been obtained then it has been used for tasks such as code comprehension, similar code search etc. In the latter case when A.I. has been applied for program optimization, it has been used to find optimal program transformations and optimal parameters for program transformations (such as loop unroll factors). Our work presented in the paper fits the mold of the latter category where we use
A.I. for performance enhancement. Below, we describe several closely related works and detail how our present work improves upon and/or is different from prior works.

AutoTVM [9] uses machine learning approaches to derive efficient execution schedules for tensor programs. It explores the use of two distinct machine learning techniques: In the first approach, from a given tensor program, domain specific features such as memory access count, data reuse ratio etc are extracted. Then, XGBoost, a form of decision tree based learners are trained to perform relative ranking of schedules based on their performance. In the second approach, the tensor program is encoded into an embedding vector using the TreeGRU method [24]. The relative performance prediction of the schedules is performed on the encoding thus obtained.

FlexTensor [35] is a tensor computation optimization framework for heterogeneous architectures. The hardware targets for which FlexTensor can create high performance code include CPUs, GPUs, and FPGAs. FlexTensor uses machine learning techniques to derive optimized execution schedules. It uses two machine learning approaches: neural networks for performance prediction, and reinforcement learning for navigating the space of possible schedules. The schedule space is navigated using Q-learning [29] based reinforcement learning. The Q-learning approach will guide the search – along the directions of the search space with the best performance. The performance prediction for different schedules which is an input to the Q-learning algorithm is performed using a feed-forward neural network.

Ansor [34] is a latest addition to the slew of TVM-based auto-tuning systems. Ansor considers a larger schedule space compared to the prior auto-tuning frameworks. Some of the innovations in Ansor include, 1) organization of the search space in a hierarchical manner 2) use of evolutionary search techniques 3) specification of schedules by recursive application of derivation rules 4) sampling of the search space – by periodically running random schedules on the target hardware to better guide the search.

Park et al [20] use machine learning to select the best program transformation sequence among the available set of program transformation recipes. They run a given input program and obtain hardware counter values such as L1 cache misses. Then, they also apply a sequence of program transformations and observe the achieved speed-up. The hardware counters and the program transformations together are used as features for training a machine learning model to predict the speed-ups. Once the machine learning model is trained, it is used as follows for selecting the best program transformation sequence among a multitude of possibilities for a given program. The unseen input program is run on the target hardware and the hardware counters are read. The hardware counters along with a transformation sequence will be input to the trained machine learning model to predict the speed-up that could be obtained for the transformation sequence. The transformation sequence delivering the highest speed-up among various transformation sequences will be selected.

Various hand written implementations of basic linear algebra operations have been provided in various libraries like oneDNN [3], BLIS [33], OpenBLAS [32], GotoBLAS [13]. ATLAS [30] is an autotuner where it generates various low-level C-implementations and finds the best performing one by executing the code on the target machine. POCA [23] generates LLVM-IR based vectorized GEMM micro-kernel where architecture independent optimizations can be applied. AUGEM [28] is a template based code generator for DLA (Dense Linear algebra) operations. It replaces the common predefined C-code with the generated assembly level code. Kevin et al. [22] use assembly level features for analytical modeling of the SIMD code with Machine learning and find the best loop transformations for vectorization. Monsifrot et al. [19] use a Machine learning approach to find the best unrolling factors.

Polyhedral compilation techniques have been developed for source-to-source code transformation for better cache locality and parallelization. The Pluto compiler [7] derives an execution schedule for the code that attempts to minimize data reuse distances. The effect of the Pluto transformation will be that iterations that use the same data will be executed close to each other in time and therefore, the code will be cache friendly. However, the performance obtained by polyhedral tools including Pluto’s can be only slightly better than that of back-end compiler’s such as Intel ICC’s and far from other approaches such as AutoTVM’s [25]. In this paper, we show that our techniques outperform AutoTVM. The reason for the inability of the purely polyhedral approaches is, they operate at a high level (source-to-source) and therefore, do not perform low-level orchestration of vectorization, vector register allocation, detailed instruction scheduling (e.g., the kinds of low level optimizations we have described in Section 4). The latter aspects are crucial to achieving high performance.

In our present work, we identified two distinct program optimizations that we need to concern ourselves with in order to obtain high performance on the target architectures. Because the high-level and low-level optimizations are different, we developed different A.I. techniques for them. For high level optimizations we employed polyhedral compilation techniques to extract features from loops and used a deep learning model to identify loop transformations that will yield high performance. For better vectorization, we combined an intrinsics based code generator with reinforcement learning (RL) to derive optimal parameters for the code generator. We have combined traditional compiler techniques with A.I. where appropriate. In particular, we have
used A.I. where an accurate cost model is difficult to define and hence, we take advantage of A.I.’s unique ability to learn from performance data.

7 CONCLUSION
In this paper we presented CPU-focused compiler techniques for high-level and low-level program optimizations. The high-level optimizations enhance data locality of programs and the low-level transformations effectively vectorize code. A.I. techniques in conjunction with polyhedral compilation algorithms and target-specific code generator help us achieve high levels of performance. We demonstrated that matrix-multiplications which lie at the heart of deep learning can be effectively optimized using the developed compiler toolchain.

The presented approach will help re-target the toolchain to newer computer architectures seamlessly – only a new target-specific code generator need be created, and the rest of the toolchain can be repurposed without modifications. Thus, the compiler framework described will enable realizing good performance out-of-the-box for new hardware architectures and new DL operators.

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