A V-Band Phase-Locked Loop with a Novel Phase-Frequency Detector in 65 nm CMOS

Waseem Abbas, Zubair Mehmood and Munkyo Seo *

Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, Korea; waseem1694@skku.edu (W.A.); zubair@skku.edu (Z.M.)

* Correspondence: mkseo@skku.edu; Tel.: +82-31-299-4321

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Abstract: A 65–67 GHz phase-locked loop (PLL) with a novel low power phase-frequency detector (PFD) in 65 nm LP CMOS is presented. The PLL consists of a V-band voltage-controlled oscillator (VCO), a divide-by-two injection-locked frequency divider (ILFD), and a current-mode logic (CML) divider chain. A charge pump (CP) and a 2nd-order loop filter are used with PFD for VCO tuning. The PFD is implemented with 16 transistors with dead-zone-free capability. The measured locking range of the PLL is from 65.15 to 67.4 GHz, with $-11.5 \text{ dBm}$ measured output power at 66.05 GHz while consuming 88 mW. The measured phase noise at 1 MHz offset is $-84.43 \text{ dBc/Hz}$. The chip area of the PLL is 0.84 mm$^2$ including probing pads. The proposed PLL can be utilized as a frequency synthesizer for carrier signal generation in IEEE 802.11ad standard high data rate transceiver circuits.

Keywords: phase locked loop (PLL); injection locked frequency divider (ILFD); phase and frequency detector (PFD); voltage-controlled oscillator (VCO)

1. Introduction

Phase-locked signal sources are a critical building block for millimeter-wave radio systems, since they provide a stable frequency and phase reference as a local oscillator (LO) [1–5]. A recent advance in CMOS technologies has enabled the implementation of low-power, low phase-noise integrated phase-locked loops (PLL) operating at millimeter-wave frequencies [6,7]. In [8], a V-band PLL was developed in 65 nm CMOS. In [9], a 40, 60, and 80 GHz bands PLL, using multi-mode LC-based injection-locked frequency divider (ILFD), is designed in 90-nm CMOS. A 64 GHz PLL for 16-QAM modulation is presented in [10]. An 81–86 GHz frequency synthesizer is demonstrated in [11]. In [12], a 60 GHz low power PLL is demonstrated in 65 nm CMOS.

The phase and frequency detection play a key role in the locking of the PLL. The two different circuits for phase and frequency detection consume more power as compared to a single phase-frequency detector (PFD), which operates for both phase and frequency detection.

A high-frequency synthesizer having a pure output signal with less output phase noise is required in wireless communication applications, specifically transceivers. The proposed V-Band PLL can be utilized for IEEE 802.11ad standard high data rate transceivers for carrier signal generation with low power consumption and less phase noise.

In this paper, we present a 65–67 GHz PLL based on a V-band voltage-controlled oscillator (VCO), a V-band injection-locked frequency divider (ILFD), and a novel phase-frequency detector (PFD), which is simpler and consumes less power than conventional ones. Section 2 describes the PLL architecture. The design details of the proposed PLL are explained in Section 3. The measured results are shown in Section 4.
2. PLL Architecture

Figure 1 shows the block diagram of the proposed PLL. The VCO is in cross-coupled configuration and provides dual outputs: a V-band fundamental output at $f_0$ and an optional output at 2nd-order harmonic, $2f_0$. The divider chain consists of a V-band divide-by-two ILFD and six-stage current-mode logic (CML) dividers. The overall division ratio of the PLL is, thus, 1/128. Details of the PLL building blocks are described in the following section.

![Figure 1. Block diagram of Proposed phase-locked loop (PLL).](image)

3. Design Details

3.1. Voltage-Controlled Oscillator (VCO)

Figure 2a shows the schematic of the dual-output V-band VCO that was used in this work. $M_{1,2}$ are biased at $V_{gs} = V_{ds} = 1.2$ V, forming a cross-coupled pair with $g_m = 4.8$ mS. The oscillation frequency is determined by the symmetrical inductor $L_2 = 80$ pH, the total capacitance at the drain of $M_{1,2}$ (25 fF) and the varactors $C_1$ and $C_2$. The quality factor of $L_2$ is 18 at 70 GHz according to electromagnetic (EM) simulation. One of the differential outputs of the cross-coupled core drives the divide-by-two ILFD, and the other output is connected to probe pads for off-chip testing. The differential outputs at $f_0$ drive $M_{3,4}$ in push-push configuration, generating an optional VCO output at $2f_0$. $L_1$ and $C_3$ are optimized for the highest output power at $2f_0$. All of the transistors in Figure 2a have 1 µm of unit finger width. In the simulation, the VCO can be tuned from 69.5 GHz to 76 GHz, as seen in Figure 2b, while providing $-5$ dBm and $-18$ dBm of output power at $f_0$ and $2f_0$, respectively, while dissipating 28 mW.

![Figure 2. (a) Schematic of proposed voltage-controlled oscillator (VCO), (b) Simulated tuning range w.r.t tuning voltage.](image)
3.2. Injection-Locked Frequency Divider (ILFD)

Figure 3a shows the schematic of the divide-by-two ILFD. M_{6,7}, together with the symmetric inductor L_{3} and varactors C_{5} and C_{6}, form a cross-coupled pair where its oscillation frequency is centered at 1/2 f_{0}. The VCO output at f_{0} is injected to the cross-coupled pair through M_{5}. According to the simulation, the ILFD achieves locking across the entire VCO tuning range from 69.5 GHz to 76 GHz, by properly biasing the varactor tuning voltage V_{tune}, as shown in Figure 3b. Specifically, the locking range of the ILFD is 3.6 GHz and 7 GHz, when the injected power at f_{0} is −12 dBm and 0 dBm, respectively. The designed ILFD consumes 24 mW.

3.3. CML Frequency Divider Chain

The frequency of the ILFD output is approximately 35 GHz, which is sufficiently low to drive static frequency dividers. The ILFD output is followed by a six-stage CML frequency divider chain, where the frequency of the final output is 500 MHz for phase comparison. Figure 4 shows the schematic of a single-stage CML frequency divider. To minimize the power consumption, the bias current and drain resistors are properly scaled for each stage. The designed CML frequency divider chain consumes 36 mW.

3.4. Phase-Frequency Detector (PFD)

Figure 5 shows the different architectures of PFDs. The block diagram of conventional PFD is shown in Figure 5a, which is commonly used for phase and frequency error detection. The conventional PFD is comparing a low-frequency reference signal with divided VCO’s output and controls the tuning voltage while sub-sampling PD, as shown in Figure 5b, samples the VCO’s output directly with a
high-frequency reference signal and detects only the phase error. If the reference $V_{ref}$ is on rising edges, it yields a rising edge on $V_{up}$. Similarly, if the VCO output $V_{vco}$ is on rising edges, it yields a rising edge on $V_{dn}$. If both outputs are high, both D-FFs are reset. Circuit schematic of D flip-flop (D-FF) in conventional PFD is shown in Figure 6, where high-speed CML D-FF is used for fast switching, low noise, and low power consumption [13,14]. In one such D-FF, 14 transistors are used. In an AND-gate as shown in Figure 7, five transistors are employed [15].

![Figure 5](image) Figure 5. Phase-frequency detector (PFD) Architecture: (a) Conventional PFD and (b) Sub-sampling PD.

![Figure 6](image) Figure 6. D flip-flop (D-FF) circuit schematic.

Figure 8 shows the schematic of the proposed PFD in this paper. The circuits in Figure 8a and Figure 8b each create $V_{up}$ and $V_{dn}$, respectively. In Figure 8a, $M_1$ is operating on negative edges of $V_{ref}$, $M_2$ on positive edges of $V_{ref}$ and $M_3$ on positive edges of $V_{vco}$. After the $M_{4,5}$ inverter, $M_6$ is operating on the positive edges of $V_{ref}$. The $M_{7,8}$ inverter finally converts the output into $V_{up}$ due to its high input impedance. The $V_{dn}$ generator in Figure 8b works similarly. The switches $M_6$ and $M_{14}$ are controlled by the input signals to pass or block the pulses, thus achieving dead-zone free condition. Figure 9 shows the difference between dead-zone free and dead-zone exist state. In Figure 9a, the ideal PFD works for all phase errors and controls the output voltages accordingly. The dead-zone exists state, as shown in Figure 9b, is clearly depicted that PFD is non-operative for a wide range of phase errors. The behavior of proposed PFD is shown in Figure 9c which shows the PFD is dead-zone free except for a phase error of $2\pi/15$. To minimize glitches when both input signals are in the same state, feedback from $V_{up}$ to drain of $M_3$ and $V_{dn}$ to drain of $M_{11}$ are utilized, because, when both inputs are in-phase, then it directly grounds the output.
Figure 7. AND-gate schematic.

Figure 8. Schematic of the proposed PFD: (a) up-pulse and (b) down-pulse generator.
The proposed PFD uses 16 transistors, thus more area-efficient than the conventional one, where 33 transistors are necessary. The proposed PFD is potentially low-power, too, due to the lack of CML gates. In the simulation, the proposed PFD consumes 2.3 μW at a 500 MHz reference clock. Simulation confirms the functionality of the proposed PFD as a phase and frequency detector. In Figure 10, both input signals $V_{ref}$ and $V_{vco}$ are in-phase. It is seen that the proposed PFD exhibits smaller glitches than the conventional one due to feedback from $V_{up}$ to drain of $M_3$ and, similarly, for $V_{dn}$ to drain of $M_{11}$. The active chip area, including PFD, CP, and LPF is 0.171 mm$^2$.

3.5. Charge Pump (CP) and Loop Filter (LF)

The schematics of the charge pump (CP) and loop filter (LF) used for the presented PLL are shown in Figure 11. $M_3$ and $M_2$ switch the current formed by $M_1$ and $M_4$. The LF is 2nd-order low-pass filter with 25.5 MHz of the loop bandwidth.
3.6. Layout Designing

The layout is designed using 65nm LP CMOS PDK. All of the transistors are used with a configuration of M2, M3, and M4 metals for the gate, source and drain respectively. The capacitors used for DC block and bypass are metal-insulator-metal (MIM) capacitor designed with OA metal layer for high-quality factor as compared to other PDK VNCAP, and NCAP capacitors. The inductors are designed for VCO and ILFD using the OA metal layer with 3 µm thickness and highest conductivity of $5.3 \times 10^7$ Siemens/m as compared to all other metal layers used in substrate configuration. The probing pads are designed while using the LB layer for signal line and metal M1 for the ground path not only for pads, but also for the whole layout ground. Figure 12 shows the stack information of substrate configuration.

4. Measured Results

The designed PLL is fabricated in 65 nm LP CMOS process. Figure 13 shows the chip photograph of the PLL. Its active die area is 0.37 mm$^2$ excluding pads.
The fabricated PLL chip is tested using an on-wafer test setup. The PLL reference clock is provided by Keysight J-BERT N4903B. The PLL output is down-converted by a V-band sub-harmonic mixer, VDI WR15SHM, with a 30 GHz LO input. Figure 14 shows a close-in spectrum of the PLL output at $f_0 = 66.05$ GHz with 515 MHz of the reference clock. The measured phase noise of the PLL is $-84.43$ dBc/Hz and $-100$ dBc/Hz, at 1 MHz and 10 MHz offset frequencies, respectively, as shown in Figure 15.

The output power of the PLL is measured using a V-band power sensor, Keysight N8488A, and a power meter, Keysight N1914A. The PLL achieves locking from 65.15 GHz to 67.4 GHz with the output power greater than $-11.6$ dBm, as shown in Figure 16. The measured PLL output frequency is lower than the simulation by 6–7 GHz, and the discrepancy is attributed to inaccuracies in EM modeling of layout parasitics and process variations. The PLL chip consumes 88 mW from a single 1.4 V supply. The optional PLL output at $2f_0$ was not tested due to the lack of spectrum and power testing capability at around 130 GHz. Table 1 compares the presented PLL with prior work. The PLL achieves an FoM of 132.58 dBc/Hz. The locking range of the PLL can be improved with a capacitor bank based tuning network for a wider tuning range VCO and ILFD for better FoM. Table 2 compares the proposed PFD with prior work, where it is seen that the proposed PFD consumes relatively low power.

$$FOM = 20 \log \left( \frac{f_H - f_L}{\Delta f} \right) - PN - 10 \log \left( \frac{P_{DC}}{1 \text{ mW}} \right)$$  (1)
Figure 14. Measured output spectrum of the PLL at $f_0 = 66.05$ GHz (uncalibrated).

Figure 15. Measured phase noise of the PLL at $f_0 = 66.05$ GHz.
Figure 16. Measured output power of the PLL.

Table 1. Comparison of recently published millimeter-wave PLL.

| Parameter               | [8]  | [9]  | [10] | [11] | [12] | [16] | [17] | Our Work |
|-------------------------|------|------|------|------|------|------|------|----------|
| Technology (nm)         | 65   | 90   | 40 LP| 65   | 65   | 28   | 65   | LP       |
| Frequency (GHz)         | 58.5–58.9 | 60.2–62.4 | 63–70 | 70–78 | 53–61 | 65–69 | 54.1–57 | 65.15–67.4 |
| Supply Voltage (V)      | 1.2  | 1.5  | 1.1  | 1    | 0.8  | 1.2  | 1.2  | -        |
| PN@1MHz (dBc/Hz)        | –83.5| –69.92| –85  | –83  | –88  | –98.5** | –93  | –84.43   |
| Ref. Frequency (MHz)    | 150  | 78   | -    | -    | 56   | 67   | 2280 | 515      |
| Power Consumption (mW)  | 43   | 106.6| 79.2 | 65   | 48   | 72.44| 10   | 88       |
| Active Chip Area (mm²)  | 1 *  | 1.12 * | 0.192| 0.31 | 0.32 | 3.24 * | 0.19  | 0.37     |
| Output Power (dBm)      | –14  | –9.5 | -    | -    | -    | -    | -    | –11.6    |
| FOM (dBc/Hz)            | 119.16| 116.5| 142.9| 142.9| 148.6| 152.58| 152.24| 132.58   |

*: with Probing Pads. **: From Simulations

Table 2. Comparison of recently published PFD.

| Parameter                                    | [18] | [19] | [20] | [21] | Our Work |
|----------------------------------------------|------|------|------|------|----------|
| Technology (nm)                              | 180  | 180  | 180  | 180  | 65 LP    |
| Frequency (GHz)                              | 1    | 3    | 2.5  | 0.5  | 0.515    |
| Supply Voltage (V)                           | 1.8  | 1.8  | -    | 2.4  | 1.2      |
| Power Consumption (mW)                       | 1.36 | 3.51 | 0.005| 0.5  | 0.0023   |
| Active Chip Area (including CP and LPF) (mm²)| -    | -    | -    | -    | 0.171    |
| No. of Transistors                           | -    | -    | 20   | -    | 16       |

5. Conclusions

This paper presents a V-band PLL with a novel PFD circuit. A cross-coupled VCO has been used as an RF signal generator with dual-frequency outputs. The fundamental frequency output has been injected to ILFD for 2nd order division and to the RF output probing PAD. The ILFD has been implemented using cross-coupled topology in order to yield similar parasitic effects as VCO. A novel PFD was employed for its simplicity and low-power consumption. The PFD has been implemented with only four logic NOT gates in a combination of two controlled switches. This controlled switched technique reduces the glitches which improve the tuning voltage efficiency. The PLL is fabricated in a
65-nm LP CMOS process, and it achieves an FoM 132.58 dBc/Hz. The PLL measured output power is −11.6 dBm with a locking range of 65.15 GHz to 67.4 GHz and phase noise of −84.43 dBc/Hz at 1 MHz offset while consuming 88 mW DC power. The proposed PLL can be utilized as a frequency synthesizer for carrier signal generation in high frequency transceiver circuits.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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