MC simulation of ultrafast transistor using ballistic electron in intrinsic semiconductor and its fabrication feasibility

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Abstract. Ultrafast operation of a transistor using ballistic electron concepts and its fabrication feasibility are shown by Monte Carlo simulation and experiment, respectively. The transistor consists of InP/GaInAs heterojunction launcher of 20 nm-width and a subsequent propagation layer of 80 nm-length intrinsic GaInAs. Schottky metal gates attached on both sides of the propagation layer are biased in the forward direction so that potential barriers at Schottky junctions are flattened and hot electrons are extracted from the launcher. Hot electron velocity is as fast as 7-8x10^7 cm/s through the whole propagation layer. From stationary and step-response simulations, the cutoff frequency is higher than one THz. The emitter charging and the transit times are discussed to confirm the simulation. Finally, fabrication and operation of the transistor with 25 nm-width emitter using GaInAs/InP organo-metallic vapor phase epitaxy, electron-beam lithography, ultrafine process are demonstrated.

1. Introduction

Toward ultrafast transistors, the concept of ballistic electron transport with a hot electron launcher was proposed[1]. Following the concept, fast FETs were predicted by Monte Carlo (MC) simulations[2], a fabrication of vertical electron transistors[3] and the experimental transconductance enhancement in vertical FETs (VFETs)[4] were reported. VFET was revisited by MC simulations and predicted 225 GHz operation[5]. These devices featured GaAs/AlGaAs, sizes of 100-600 nm wide and 200 nm long and FET like operation principle. There were donor atoms and thermal-equilibrium electrons at concentrations of around 7 x 10^{16} cm^{-3} in the channel shielding the source against the drain. Potential barriers at Schottky contacts prevented thermal-equilibrium electrons flow into gates. The drain current was essentially modulated by the channel width as in a FET.

We have revisited the previous devices with respect to thorough utilization of the ballistic electron concept taking ultrafine process technology and InP/GaInAs material systems developed in last 20 years into account. Then we have proposed a new vertical transistor with following features[6],
An electron propagation layer (PL) is intrinsic semiconductor so that impurity scatterings are eliminated. Length of PL is less than 100 nm so that LO-phonon emissions are suppressed. There are gate electrodes on both sides of PL as shown in Fig. 1. Width of PL is much less than 100 nm so that an emitter is shielded electrostatically from a collector by the gate electrodes and therefore output conductance is low. We have fabricated[7] and demonstrated voltage and current gains of proposed devices[8].

This paper reports the cutoff frequency of InP/GaInAs transistors evaluated by MC simulation and measured DC characteristics of fabricated devices with the essential structure proposed.

2. Monte Carlo Simulation
We studied the device shown in Fig.1 by Monte Carlo simulation using DAMOCLES software[9]. The device consisted of n-InP emitter (length of 20 nm, doping concentration of $1 \times 10^{18}$ cm$^{-3}$), i-GaInAs PL (80 nm, $10^{16}$ cm$^{-3}$) and a Schottky collector with barrier height of 0.6 eV. Widths of the device were 20-30 nm. Schottky metal gates on both sides of the PL were apart from the emitter by 10 nm. Cross sections of gates were 10 nm by 20 nm.

Common emitter IV characteristics from stationary simulations are shown in Fig.2. At a collector voltage of 1.1 V and a gate voltage of 0.8 V, the transconductance $g_m$ is 16 S/cm and the output conductance $g_o$ is 0.26 S/cm. The ratio of $g_m/g_o$ is 60. At this operation point, energy distributions of gamma- and L-valleys and electrons are shown in Fig.3. Electrons stay in gamma valley and keep high energy obtained at the launcher through PL.

Potential profile convex upward attributes to the space charge of hot electrons injected into the intrinsic semiconductor. Potential profile in the transverse direction is almost flat and therefore the electric field at the launcher is uniform. Average electron velocity in PL was 7-8 x $10^7$ cm/s.

Total electron charges in the device and collector currents were obtained from stationary analyses. The delay time $\tau$ is determined to be 0.13 ps from $(Q_{H}-Q_{L})/(I_{H}-I_{L})$ where $Q_{H}$ and $I_{H}$ are the total electron charge and the collector current, respectively when the gate voltage was 0.84 V while $Q_{L}$ and $I_{L}$ are those when the gate voltage was 0.83 V. The cutoff frequency is 1.2 THz ($=1/(2\pi \tau)$).

The ratio of the collector current to the emitter current was 0.74. This ratio was improved to 0.95 by decreasing the gate length from 20 nm to 10 nm.
Step responses were simulated for devices of 30 nm width and gate cross section of 10 x 10 nm². Two gates were connected to a voltage source through series resistances of 1/gₘ, where gₘ was the transconductance of the device obtained from stationary simulations. From the step response of the collector current, the 60% rise time is determined to be 0.14 ps, shown in Fig. 4. According to an analysis using a small-signal equivalent circuit, 60% rise time is equal to the delay time τ and consequently the cutoff frequency is 1.2 THz.

3. Transit, Emitter Charging times and Output Conductances

Results of MC simulation are discussed by theoretical estimations of factors determining the cutoff frequency.

3.1. Ballistic Velocity

The velocity of the electron without any scatterings is determined by the dispersion relation, E-k characteristics, of the semiconductor. From the band structure of GaInAs[10], in (100)-direction the ballistic velocity is 1.1 x 10⁸ cm/s at maximum for the energy lower than the L-valley bottom, 0.62 eV. For a hot electron of 0.23 eV from the InP/GaInAs launcher, the ballistic velocity is 9 x 10⁷ cm/s.

3.2. LO-phonon scattering

When an electron emits one LO-phonon, on the average, the total velocity decreases by 7%, propagation direction deflects by 36°, and consequently electron velocity is 75% of its initial value. Assuming Poisson distribution with the average probability 5.0 ps⁻¹, the number of LO-phonons emitted in PL of 80 nm is less than two at high probability more than 0.9. Therefore, the electron velocity in PL is from 6.8 (= 9 x 0.75) - 9 x 10⁷ cm/s explaining the simulation result. The real transit time of our device is estimated as 0.1 ps (80 nm / 8 x 10⁷ cm/s). Taking the displacement current effect into account, the effective transit time is 0.05 ps.

3.3 Intrinsic Emitter Charging Time

At InP/GaInAs heterojunction, a potential barrier and a carrier depletion region are formed in InP by the conduction band discontinuity. Under application of an electric field normal to the junction, an increase in the field ΔF causes decreases in the height of the barrier seen from the emitter and in the length of the depletion region. These decreases cause the increase in the emission current density ΔJ and the decrease in the surface charge density Δσ = -εΔF/ε, where ε is the dielectric constant of the semiconductor. The intrinsic emitter charging time τ₀ is given by 0.04 ps at minimum at the current density of 2000 kA/cm² and 0.07 ps at 600 kA/cm² corresponding to present simulation[11].

3.4 Charging Time Including Parasitic Capacitances

In the present device structure, parasitic capacitances should not be ignored. The total capacitance between the gate and the emitter is divided into an intrinsic and external, or parasitic, parts, Cₑₑ and Cₑₑₑ, respectively by an electrostatic analysis. The emitter charging time taking the parasitic capacitance into account is given by τₑₑ (1+Cₑₑₑ/Cₑₑ) and is 0.077 ps. The total charging time including the gate-collector capacitance is 0.1 ps. Then total delay time is 0.15 ps (= 0.05+0.1) close to that obtained by MC simulation.
3.5 Output Conductance
Gate electrodes on both sides of PL electrostatically shield the emitter against the collector. This shielding sharply depends on the width of PL. The ratio $g_m/g_o$ from the simulation agrees well with electrostatic analysis.

4. Fabrication Feasibility
Feasibilities of fabrication and operation of the simulated devices were experimentally examined. We focused into the emission control by gate electrodes on both sides of PL. We fabricated the structure shown in Fig. 5 where the space between two gate electrodes was narrow.

Using the InP/GaInAs organo-metallic vapor phase epitaxy, the electron beam lithography, the reactive ion etching and the wet chemical etching, devices with 25 nm-width emitter mesa and self-aligned gate electrode were created[12].

A common emitter current voltage characteristics measured at 30 K is shown in Fig.6. With the DC characteristics, we confirmed that in 25 nm-width InP/GaInAs emitter mesa, electron emission was controlled by the extraction field caused by the gate voltage. The current saturation indicates electrostatic shielding by the gate electrodes.

Low current in the present device is attributed to the oxidation of Al in the double barrier structure(Fig.5). This current suppression problem is being improved.

5. Conclusion
Monte Carlo simulations and consequent discussions indicate THz operation in our proposed transistor embodying of the ballistic electron concept. One of keys to realize the device, fabrication of the ultrasmall width was shown to be feasible.

Acknowledgement Authors thank S. Arai, M. Asada and M. Watanabe for fruitful discussions, S. Tamura for technical assistances in the electron beam lithography.

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