Delay Optimization of Combinational Logic by AND-OR Path Restructuring

Ulrich Brenner and Anna Hermann
Research Institute for Discrete Mathematics, University of Bonn
{brenner,hermann}@dm.uni-bonn.de

Abstract—We propose a dynamic programming algorithm that constructs delay-optimized circuits for alternating AND-OR paths with prescribed input arrival times. Our algorithm fulfills best-known approximation guarantees and empirically outperforms earlier methods by exploring a significantly larger portion of the solution space.

Our algorithm is the core of a new timing optimization framework that replaces critical paths of arbitrary length by logically equivalent realizations with less delay. Our framework allows revising early decisions on the logical structure of the netlist in a late step of an industrial physical design flow. Experiments demonstrate the effectiveness of our tool on 7nm real-world instances.

I. INTRODUCTION

In VLSI design, logic synthesis turns the abstract logic specification of a chip into a concrete representation in terms of gates. This happens very early in the design process, and for the following steps, the logical description typically remains fixed. However, during physical design, it may turn out that the chosen implementation of the logic functionality was not the best choice, e.g., with respect to placement or timing. Now it would be desirable to find a better suited logically equivalent representation.

We propose an algorithm that improves timing by logic restructuring of critical combinational paths. Optimizing a path boils down to optimizing an AND-OR path, i.e., a Boolean function of type

\[ t_0 \land (t_1 \lor (t_2 \land (t_3 \lor (t_4 \land \ldots t_{m-1}) \ldots)) \text{, see } [24]. \]

Besides, AND-OR paths have an important application in the construction of adder circuits. The carry bit computation in an adder (which is the critical part) is equivalent to the evaluation of an AND-OR path. The tasks of AND-OR path and adder optimization are actually equivalent concerning timing if circuit size is disregarded.

Many efficient adder circuits (e.g., [4], [13], [14]) have been proposed in the previous decades and could hence be used for optimizing AND-OR paths. In terms of depth, the best approximation guarantee for AND-OR path circuits has been proven by [8]. However, these approaches optimize circuit depth, yielding fast circuits only if all input signals arrive simultaneously. In our setting on the most timing-critical path, this will rarely be the case. Instead, we minimize circuit delay, a generalization of circuit depth that takes into account individual prescribed input arrival times.

Some algorithms for adder optimization regard input arrival times, but most lack provable guarantees: For adders with general arrival times, there are a greedy heuristic [25] and a dynamic program [16], but for both, no approximation ratio can be shown. In [21], the delay of adders is evaluated regarding arrival times computed after physical design, but the optimization goal is depth and not delay.

Algorithms for AND-OR path optimization with input arrival times that achieve provably good approximation ratios are presented in [3], [20] and [10]. We will explain their ideas in Section II-B. The method of [20] is used in [24] to optimize general logic paths.

Our goal is to restructure critical paths of any length with provably good approximation guarantees. In contrast, many other approaches synthesize whole netlists and thus arbitrary Boolean functions. As in general, finding a logically equivalent implementation of a given circuit with, say, minimum depth is an NP-hard problem, these approaches only replace sub-circuits of constant size by alternative realizations (see e.g., [1], [5], [17], [19], [22]). Here, the new solution is logically correct by construction, but an extension to larger sub-circuits is hardly possible.

Our main contributions are:

- We propose a new dynamic program for delay optimization of AND-OR paths. In fact, the algorithm solves a more general problem, the optimization of so-called extended AND-OR paths. We describe how decisions on the structure of sub-solutions can be postponed until these sub-solutions are combined. This reduces rounding effects that are inherent in previous algorithms.
- Our algorithm fulfills best known theoretical delay guarantees as it is a common generalization of all previously best approaches [3], [10], [20]. Moreover, we demonstrate in experiments that we improve delay significantly compared to those.
- We compute lower bounds on the best possible delay of AND-OR paths. On 89% of our test instances, the result of our algorithm matches the lower bound and is thus provably optimum.
- We propose a framework for timing optimization of combinational paths of arbitrary length based on [24] with our AND-OR path restructuring algorithm as a core routine. The generic delay model used in our core algorithm allows incorporating physical locations. Our framework contains several classical timing-optimization tools and – in contrast to the simple mapping used in [24] – an evolved technology-mapping method [6].
- Experiments on recent industrial 7nm chips show the efficiency and effectiveness of our framework. We improve worst slack and total slack considerably without any impact on other metrics.

The rest of the paper is organized as follows. In Section II, we define the AND-OR path optimization problem, survey known approaches, and present our new approximation algorithm. Section III describes our logic restructuring framework. Experimental results are shown in Section IV, and Section V contains concluding remarks.

II. AND-OR PATH OPTIMIZATION

Note that in this section, we use a simplified linear delay model with unit gate delay and zero wire delay. In Section III-A, we will generalize this model to adapt to our application in physical design.

A. Problem formulation

For us, a circuit \( C \) is a connected acyclic digraph whose nodes can be partitioned into two sets: inputs with no incoming edges representing Boolean variables, and gates representing an elementary Boolean function (mostly AND2 or OR2, i.e., AND and OR gates with fan-in two), where only a single gate out(C) called output has no outgoing edges. An AND-OR path on inputs \( t_0, \ldots, t_{m-1} \) is a Boolean formula of type

\[ g(t_0, \ldots, t_{m-1}) = t_0 \land (t_1 \lor (t_2 \land (t_3 \lor (t_4 \land \ldots t_{m-1}) \ldots)) \text{ or } \]

\[ g^*(t_0, \ldots, t_{m-1}) = t_0 \lor (t_1 \land (t_2 \lor (t_3 \land (t_4 \lor \ldots t_{m-1}) \ldots)) \text{ and } g^*(t_{m-1}) = t_{m-1}. \]

On the left-hand side of Figure 1, a circuit for the AND-OR path \( g(t_0, t_1, t_2, t_3, t_4) \) is shown. Given individual arrival times \( a(t_i) \in \mathbb{R} \)

\[ a(t_i) = 1, \]

\[ a(t_0) = 0.5, \]

\[ a(t_1) = 0.7, \]

\[ a(t_2) = 0.9, \]

\[ a(t_3) = 1.1, \]

\[ a(t_4) = 1.2, \]

\[ a(t_{m-1}) = 2.3. \]

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that both realize the A
is the maximum of its predecessors’ arrival times plus
a lower bound for the
path, we define for
and

Figure 1 shows how gate arrival times are computed in two circuits
that both realize the AND-OR path \( g(t_0, t_1, t_2, t_3, t_4) \). The circuits have a delay of 7 and 6, respectively. Note that in the special case when all input arrival times are 0, circuit delay is exactly circuit depth, i.e., the length of a longest directed path.

Given an instance consisting of inputs \( t_0, \ldots, t_{m-1} \) with arrival times \( a(t_0), \ldots, a(t_{m-1}) \), we define the weight \( W := \sum_{i=0}^{m-1} 2^a(t_i) \).
It is not too difficult to see that \( \log_2(W) \) is a lower bound for the delay of any binary circuit computing an AND-OR path for inputs \( t_0, \ldots, t_{m-1} \) with arrival times \( a(t_0), \ldots, a(t_{m-1}) \in \mathbb{N} \) (this boils down to Kraft’s inequality [15]; see [20] for a concise proof).

Optimizing \( g(t) \) and \( g^*(t) \) is equivalently hard: By the duality principle of Boolean algebra, any circuit for \( g(t) \) consisting of AND and OR gates can be transformed into a circuit for \( g^*(t) \) with the same delay by exchanging AND and OR gates and vice versa.

### B. Previous Algorithms

A common approach for AND-OR path optimization is the application of recursion formulas that allow reducing the problem to the construction of circuits for AND-OR paths with fewer inputs.

The algorithm by Rautenbach et. al [20] is based on the following equation (for \( \lambda \in \mathbb{N} \) with \( 2\lambda < m - 2 \)):

\[
g(t_0, \ldots, t_{m-1}) = g(t_0, \ldots, t_{2\lambda-1}) \lor (t_0 \land t_{2\lambda} \land t_{2\lambda+1} \land g(t_{2\lambda+2}, \ldots, t_{m-1}))
\]

To see the correctness of (1), check that \( g(t_0, \ldots, t_{m-1}) \) is true exactly in the following two cases:

- \( g(t_0, \ldots, t_{2\lambda-1}) \) is true (then the other inputs do not matter)
- \( g(t_{2\lambda}, \ldots, t_{m-1}) \) is true and the value “true” is propagated to the output because the inputs \( t_0, t_2, t_4, \ldots, t_{2\lambda-2} \) are all true

See [20] for a detailed proof. Using formula (1), an AND-OR path circuit on inputs \( t_0, \ldots, t_{m-1} \) can be constructed by combining AND-OR path circuits on inputs \( t_0, \ldots, t_{2\lambda-1} \) and on inputs \( t_{2\lambda}, \ldots, t_{m-1} \) and a circuit for a multi-input AND on the inputs \( t_0, t_2, \ldots, t_{2\lambda-2} \).

Using (1) in a dynamic program with running time \( O(m^3) \), the authors of [20] construct AND-OR path circuits with delay at most

1.441 \( \log_2(W) \)+3. Held and Spirlk [10] obtain a slightly better delay bound of 1.441 \( \log_2(W) \) + 2.673 using the dual of the following equation (for \( \lambda \) with \( 2\lambda < m - 1 \)):

\[
g(t_0, \ldots, t_{m-1}) = g(t_0, \ldots, t_{2\lambda}) \land \left( (t_1 \lor t_5 \lor \ldots \lor t_{2\lambda+1}) \lor g(t_{2\lambda+2}, \ldots, t_{m-1}) \right)
\]

Their algorithm runs in time \( O(m \log_2^2 m) \) as they explicitly choose \( \lambda \) in each recursion step. The proof of (2) is analogous to the proof of (1), but here one should check in which cases the two formulas are false. We will use (2) in a slightly different equivalent form (note that \( t_{2\lambda+1} \lor g(t_{2\lambda+2}, \ldots, t_{m-1}) = g^*(t_{2\lambda+1}, \ldots, t_{m-1}) \)):

\[
g(t_0, \ldots, t_{m-1}) = g(t_0, \ldots, t_{2\lambda}) \land \left( (t_1 \lor t_5 \lor \ldots \lor t_{2\lambda+1}) \lor g^*(t_{2\lambda+1}, \ldots, t_{m-1}) \right)
\]

As (1) and (3) contain functions combining a multi-input AND or OR with an AND-OR path, we define for \( t = (t_0, \ldots, t_{m-1}) \) and \( 0 \leq i \leq j \leq k < m \) even the extended AND-OR paths

\[
\phi_{i,j,k} := t_i \land t_{i+2} \land \ldots \land t_{j-2} \land g(t_{j}, \ldots, t_k)
\]

and

\[
\phi^*_{i,j,k} := t_i \lor t_{i+2} \lor \ldots \lor t_{j-2} \lor t_{j} \lor t_{j+2} \lor \ldots \lor t_{k}.
\]

The extended AND-OR path \( \phi_{0,4,12} \) is depicted in Figure 2(a). From the splits (1) and (3), using extended AND-OR paths as a more flexible replacement for sub-functions, we deduce the splits

\[
\phi_{0,0,m-1} = \phi_{0,0,2\lambda-1} \lor \phi_{0,2\lambda,m-1} \quad \text{for } 1 \leq \lambda \leq \frac{m-1}{2}
\]

\[
\phi_{0,0,m-1} = \phi_{0,0,2\lambda} \land \phi_{0,2\lambda,m-1} \quad \text{for } 0 \leq \lambda \leq \frac{m-1}{2}
\]

that can be generalized to extended AND-OR paths as

\[
\phi_{i,j,k} = \phi_{i,j+2\lambda-1} \land \phi_{i,j+2\lambda,k} \quad \text{for } 1 \leq \lambda \leq \frac{j-k}{2}
\]

\[
\phi_{i,j,k} = \phi_{i,j+2\lambda} \land \phi^*_{i,j+2\lambda+1,k} \quad \text{for } 0 \leq \lambda \leq \frac{j-k}{2}
\]

Note that in (6) and (7), the functions on the right-hand side depend on fewer inputs than \( \phi_{i,j,k} \). Figure 1 shows an example for split (5) with \( \lambda = 1 \), and Figures 2(a) and 2(b) for split (7) with \( \lambda = 2 \).

Using split (7) and its dual, Grinchuk [8] proves the upper bound \( \log_2 m + \log_2 \log_2 m + 3 \) on the depth of AND-OR path circuits, and Brenner and Hermann [3] give an algorithm for arbitrary integer arrival times with running time \( O(m^4 \log^2 m) \) and a delay bound of

\[
\log_2 W + \log_2 \log_2 W + \log_2 \log_2 \log_2 W + m + 4.3.
\]

In the special case when \( k-j \leq 1 \), \( \phi_{i,j,k} \) is actually a multi-input AND, and the function can be realized by a delay-optimum circuit using a greedy algorithm called Huffman coding:

**Theorem 1** (Golumbic [7], based on Huffman [11]), Given inputs \( t_0, \ldots, t_{m-1} \) with arrival times \( a(t_i) \), a delay-optimum circuit for the Boolean function \( t_0 \land \ldots \land t_{m-1} \) (or \( t_0 \lor \ldots \lor t_{m-1} \)) can be constructed in \( O(m \log_2 m) \) time. If \( a(t_i) \in \mathbb{N} \) for all \( i = 0, \ldots, m-1 \), then the delay of an optimum circuit is \( \lceil \log_2 W \rceil \).

**C. Our Approach**

We present an algorithm for AND-OR path optimization with prescribed input arrival times that generalizes any of the algorithms in [3], [10], [20]. In particular, on any instance, the delay of our solution is at least as good as the delay computed with any of the three algorithms, and on most instances, it is better, cf. Section IV.

To simplify notations, hereafter we assume that all arrival times are integral. Still, our implementation allows arbitrary arrival times.

Recall that in the AND-OR path optimization problem, we aim at computing a circuit containing only fan-in-2 gates. However, in intermediate steps, we allow a larger fan-in for the gate computing the output of the circuit. This leads to the following definition.
Definition 2. An undetermined circuit is a Boolean circuit $C$ consisting of AND and OR gates only such that all gates with the possible exception of $\text{out}(C)$ have fan-in two. With given input arrival times, the weight of $C$ is $\text{weight}(C) := \sum_{i=1}^{d} 2^{d_i}$, where $d_1, \ldots, d_k$ are the arrival times at the predecessors of out$(C)$.

In Figure 1, the weight of the left and right undetermined circuit is $2^2 + 2^6 = 68$ and $2^3 + 2^4 = 48$, respectively. Figure 2(c) displays an undetermined circuit with fan-in 5 at the output gate.

For undetermined circuits, we do not yet specify how we realize the output gate by fan-in 2-gates. This allows greater flexibility when combining several such circuits to a larger circuit. The following lemma shows that optimizing the weight of an undetermined circuit can be used to compute fan-in 2-circuits with small delay.

Lemma 3. Given an undetermined circuit $C$, we can construct a Boolean circuit using AND2 and OR2 gates only that computes the same Boolean function as $C$ with delay at most $\lceil \log_2(\text{weight}(C)) \rceil$.

Proof. Apply Huffman coding with the predecessors of out$(C)$ as inputs (see Theorem 1).

Algorithm 2 states our overall dynamic programming algorithm for AND-OR path optimization on inputs $t_0, \ldots, t_{m-1}$, which works as follows: We compute a cubic-size table that contains undetermined circuits $A_{i,j,k}$ and $O_{i,j,k}$ realizing the extended AND-OR path $\phi_{i,j,k}$ for all $0 \leq i < j \leq k \leq m - 1$ and $j - i$ even, where out$(A_{i,j,k}) = \text{AND}$ and out$(O_{i,j,k}) = \text{OR}$. In particular, this computes circuits for the entire AND-OR path $\phi_{0,m-1} = g(t_0, \ldots, t_{m-1})$.

Note that when $k = j$ or $k = j + 1$, the function $\phi_{i,j,k}$ is a multiple-input AND, hence, in Line 4, an optimum solution can be found by Huffman coding (see Theorem 1). To compute undetermined circuits for $\phi_{i,j,k}$ with $j - i$ even and $k > j + 1$, we assume that we have already computed undetermined circuits for $\phi_{i,j,k}$ with $j - i$ even and $k = j + 1$. The solution is enumerating all possible choices of $\lambda$ in (6) and (7) to recursively compute a circuit $C$ for $\phi_{i,j,k}$ from pre-computed solutions (while dualizing one sub-circuit according to split (7)). Since the combination of two undetermined circuits is not necessarily an undetermined circuit, we apply Algorithm 1. Here, in Line 7, we fix the structure of the undetermined sub-circuit $C_i$ as a circuit $C_i'$ over $\{\text{AND2}, \text{OR2}\}$. Figure 2 shows an example of split (7). In Algorithm 2, the circuit $C$ is stored in a candidate list $C$ of undetermined circuits for $\phi_{i,j,k}$. The undetermined circuits among $C$ with the best weight with an AND or OR gate at the output are stored as $A_{i,j,k}$ in Line 9 and $O_{i,j,k}$ in Line 8, respectively.

As final circuit for $\phi_{0,0,m-1}$, we choose the weight-minimum circuit among $A_{0,0,m-1}$ and $O_{0,0,m-1}$ in Line 10 of Algorithm 2, which is actually constructed.

Algorithm 1: Merging 2 undetermined circuits.

Input: Undetermined circuits $C_1$ and $C_2$ computing Boolean functions $h_1$ and $h_2$; a gate type $\circ \in \{\text{AND}, \text{OR}\}$.

Output: An undetermined circuit $C$ computing $h_1 \circ h_2$.

1. Add a $\circ$ gate $c_0$ to the union of the circuits $C_1$ and $C_2$.
2. for $i \leftarrow 1$ to 2 do
3. Let $c_1, \ldots, c_k$ be the predecessors of out$(C_i)$.
4. if out$(C_i)$ is a $\circ$ gate then
5. Remove out$(C_i)$ and add edges $(c_1, c_0), \ldots, (c_k, c_0)$.
6. else
7. Use Lemma 3 to construct a circuit $C'_i$ from $C_i$.
8. Add an edge from out$(C'_i)$ to $c_0$.

Algorithm 2: AND-OR path optimization.

Input: Boolean variables $t_0, \ldots, t_{m-1}$ with arrival times $a(t_0), \ldots, a(t_{m-1}) \in \mathbb{N}$.

Output: A Boolean circuit computing $g(t_0, \ldots, t_{m-1})$.

1. for $l \leftarrow 1$ to $m$ do
2. for $0 \leq i < j < k < m, j - i$ even s.t. $\phi_{i,j,k}$ has $l$ inputs do
3. if $k \in \{j, j + 1\}$ then // $\phi_{i,j,k}$ multi-input AND
4. $A_{i,j,k} :=$ circuit computed by Huffman coding.
5. else
6. $C :=$ list of undetermined circuits for $\phi_{i,j,k}$ arising from applying split (6) or (7) with any valid $\lambda$, followed by a call to Algorithm 1.
7. $A_{i,j,k} := \text{argmin}\{W(C) : C \in C, \text{out}(C) = \text{AND}\}$.
8. $O_{i,j,k} := \text{argmin}\{W(C) : C \in C, \text{out}(C) = \text{OR}\}$.
9. $C := \text{argmin}\{W(A_{0,0,m-1}), W(O_{0,0,m-1})\}$.
10. return Circuit $C'$ resulting from applying Lemma 3 to $C$.

Theorem 4. Algorithm 2 computes a circuit with delay at most $\log_2(W) + \log_2 \log_2(m) + \log_2 \log_2 \log_2(m) + 4.3$ and can be implemented to run in time $O(m^4)$.

Proof. (SKETCH) Algorithm 2 considers, in particular, all recursion steps from [3]. Using this, one can show that for any sub-instance $\phi_{i,j,k}$, the algorithm computes a solution which is at least as good as the solution computed by the algorithm from [3] and thus also meets the delay bound (8). The running time is dominated by $O(m^4)$ calls to Algorithm 1, which can be implemented to run in constant time if only weights and delays are computed and only the final circuit $C'$ in Line 10 of Algorithm 2 is actually constructed. 

Fig. 2: A possible way to construct circuit $C_{i,j,k}$ realizing $\phi_{i,j,k}$ in Algorithm 2 with $i = 0$, $j = 4$, $k = 12$ and split (7) with $\lambda = 2$. In this example, we use naive implementations for $C_1$ and $C_2$. 

Add an edge from $c_j$ to $c_i$.

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We conjecture that a stronger theoretical delay bound can be proven for our algorithm.

In Section IV, we will see that in our practically applied logic optimization framework, the running time of Algorithm 2 is negligible.

In order to take care of the circuit size, we can modify Algorithm 2 as follows: For each sub-instance \( \phi_{i,j,k} \), we store not just one circuit with the best delay per output gate type, but all non-dominated circuits. Here, circuit \( C \) dominates circuit \( C' \) if both weight and size of \( C \) are at least as good as in \( C' \) and if the gate types of \( \text{out}(C) \) and \( \text{out}(C') \) coincide. In the end, we choose \( C \) to be the smallest among all weight-optimus circuits. This does not affect the delay of the circuit (and Theorem 4 still holds), but often reduces its size.

### III. Logic Optimization Framework

We propose a timing optimization framework (cf. Figure 3) based on Werber et al. [24] with Algorithm 2 as an essential component that is used in production in a late pre-routing stage of an industrial physical design flow. Our framework revises the logical structure of critical paths using placement and timing information. In Section III-A, we adapt the delay model used in Algorithm 2 to respect placement, buffering and gate sizing effects. As we do not fully account for different kinds of gates or different gate sizes that might be available, our framework involves a technology mapping step (Section III-B) and powerful gate sizing and buffering routines (Section III-C).

We iteratively optimize the worst slack of the currently most timing-critical combinational path until overall worst slack does not improve significantly anymore. A single iteration works as follows:

1. **Preoptimization step**: We first try to improve the slack of \( P \) without changing its logical structure in order to diminish disruptions. To this end, we apply detailed optimization to \( P \) as described in Section III-C. If a threshold slack improvement of \( \delta_{\text{min}} \) is exceeded, we keep the changes imposed by preoptimization and start the next iteration.

   Otherwise, we discard the preoptimization’s changes and perform the path restructuring step (central, green part of Figure 3). This step works on internal data structures; the netlist is not changed before detailed optimization (Section III-C). We consider the possibility to optimize any sub-path \( S \) of \( P \) up to a maximum length of \( m_{\text{max}} \). First, we apply a normalization (Section III-A) in order to extract an AND-OR path \( S' \) from \( S \) on which we run Algorithm 2. Then, the technology mapping routine from [6] (see also Section III-B) locally modifies \( S \) to benefit from all available gate types. After having optimized all sub-paths of \( P \), we store all restructuring possibilities in a list \( L \), sorted by decreasing estimated slack gain.

   For only the most promising fraction of restructuring options, we apply the time-consuming detailed optimization (cf. Section III-C). First, we tentatively apply detailed optimization to the topmost \( k \) candidates in \( L \). If the actual slack gain of the best solution exceeds \( \delta_{\text{target}} \), we choose this solution; otherwise, we iteratively decrease \( \delta_{\text{target}} \) by a fixed value and try out the next \( k \) candidates in \( L \) until we reach \( \delta_{\text{target}} \) or \( L \) is empty. Afterwards, we choose the restructuring candidate \( C \) with best actual slack gain \( \delta_{C} \) for \( P \) among all detailed-optimized solutions. This way, we usually apply detailed optimization to only a few instances, but still find the overall best restructuring option. If \( \delta_{C} \geq \delta_{\text{min}} \) and if no side path slack has worsened beyond the initial slack of \( P \), we implement this netlist change, possibly retaining parts of \( P \) needed for side outputs. If the change is implemented and the slack gain over the last \( n_{\text{num}} \) iterations exceeds a threshold \( \delta_{\text{th}} \), we start the next iteration; otherwise, we stop.

   Note that this is a simplified flow description. E.g., in practice, we optimize the second critical path or the most critical latch-to-latch path when \( P \) cannot be further optimized.

#### A. Normalization

Our AND-OR path optimization algorithm from Section II expects as an input an alternating path of AND2 and OR2 gates with prescribed input arrival times, and assumes that gates have a unit delay and connections do not impose any delay. However, the most critical path \( P \) contains arbitrary gates with varying delays, and the physical locations of the path inputs might be far apart, inducing undeniably high wire delays even after buffering. A normalization step thus transforms \( P \) into a piece of netlist whose core part is an AND-OR path with appropriately modified input arrival times.

As we work on the most critical path, the buffering routine applied in Section III-C will compute delay-optimum solutions. Thus, we can assume a linear wire delay and estimate the wire delay between two physical positions \( p_1 \) and \( p_2 \) by \( d_{\text{dist}} = |p_1 - p_2| \) for a constant \( d_{\text{max}} \in \mathbb{R} \). The traversal time through a gate is approximated by a constant \( d_{\text{gate}} \in \mathbb{R} \). The constants \( d_{\text{gate}} \) and \( d_{\text{dist}} \) are chosen based on an analysis of typical values on the respective design. As on the critical path, there are rather low fan-outs and slws, the delay of gates with different types and sizes still varies, but not much in comparison to
the differences in arrival times. Hence, assuming a realistic constant
gate delay suffices to determine the logical structure of the circuit.

Since we work on the most timing-critical part of the design, we
place the circuit $C$ computed by Algorithm 2 such that each path is
embedded delay-optimally, implying that each path from an input $t_i$
to out($C$) has a wire delay of $d_{\text{wire}} \cdot ||l(t_i) - l(\text{out}(C))||_1$, where $l$ indicates physical coordinates on the chip. Thus, the delay of $C$ is
max$_{t_i \rightarrow \text{out}(C)} \{a(t_i) + d_{\text{wire}} \cdot ||l(t_i) - l(\text{out}(C))||_1 + d_{\text{gate}} \cdot |Q|\}$, where the maximum ranges over all paths $Q$ in $C$ from any input $t_i$
to out($C$). Applying Algorithm 2 with modified arrival times $a'(t_i) := \frac{1}{d_{\text{gate}}}(a(t_i) + d_{\text{wire}} \cdot ||l(t_i) - l(\text{out}(C))||_1)$ hence yields a circuit with optimum wire delay with respect to
physical locations. In fact, we choose a placement that is
netlength-optimum among all delay-optimum placements: We determine $l(\text{out}(C))$ based on its successors in the netlist and place each
gate at the median position of its predecessors and out($C$).

Now, we can describe our normalization. Let $x$ denote the most
critical input of a sub-path $S$ of $P$. We represent each gate in $S$ using
AND2 and INV gates only. This does not necessarily yield a path, but we can recover the original critical path by following the signal flow of $x$, obtaining a path $S'$. By applying De Morgan transformations in reverse topological order, we ensure that $S'$ contains AND2 and
OR2 gates only, possibly adding inverters at the inputs of $S'$. We use Huffman coding (Theorem 1) on chains of AND2 gates (or OR2 gates) in $S'$ to move less critical gates into $S', S''$ respecting physical locations by modifying arrival times as above. This way, $S''$ becomes an AND-OR path that – with input arrival times $a''$ – can be passed
to Algorithm 2. Figure 4 depicts the normalization on a path $S$ (left)
containing inverters (bubbles), NOR, and OA1 gates. On the right, we
show $S$ after normalization with the AND-OR path $S''$ colored.

B. Technology Mapping

The purpose of our technology mapping step is to change the newly
created circuit locally to improve worst slack and the physical area
occupied by gates by making use of all gates available on the design.
We use the dynamic programming algorithm from Elbert [6] which
covers the input circuit by graphs representing the available gate
types. With respect to any fixed tradeoff of arrival time (regarding
our timing model from Section III-A, but with specific estimated
delays per gate type) and number of gates, this algorithm computes
an optimum technology mapping, but the running time grows exponentially
in the number $l$ of gates with more than one successor. In our
application, $l$ is usually very small, hence we can effort this running
time (cf. the end of Section IV). For constant $l$, [6] also provides
a fully polynomial-time approximation scheme. On general circuits,
computing a size-optimum technology mapping is NP-hard [12].

C. Detailed Optimization

Depending on the actual stage of the design, our detailed optimization step invokes buffering, layer assignment and gate sizing tools. When used in late physical design, we apply Held’s gate sizing routine [9], followed by the buffering tool with an integrated layer assignment by Bartoschek et al. [2]. After buffering, we apply gate sizing again, in particular on newly inserted buffers. As we work on the most critical fraction of the design, $V_l$ assignment can be done conveniently by using the fastest gates available.

An incremental placement legalization makes sure that the placement
remains legal throughout all netlist changes.

IV. EXPERIMENTAL RESULTS

In a first set of experiments, we examined the AND-OR path optimization algorithm from Section II separately. To this end, we created AND-OR path instances with $4$ to $28$ inputs and random integral arrival times chosen uniformly from the interval $[0, \#inputs]$. For each number of inputs, we created $1000$ instances.

We compared our results with the previously best methods [3], [10], and [20]. For each instance, we ran all three algorithms and compared the best result in terms of delay to our algorithm's output. Figure 5 visualizes our results. Instances are grouped by their numbers of inputs, and colors indicate the absolute delay difference of computed solutions. Our algorithm covers all recursion options from [3], [10], [20], so our solutions can never be worse. In fact, on almost all instances, the delay of our circuit is better, and already for $18$ inputs, on every other instance better by $2$ or more.

For each instance, we computed a lower bound on delay based on
the following ideas: First, Kraft’s inequality [15] imposes a lower
bound on the delay of any binary circuit; secondly, we enumerate
possible local gate configurations near the output of an AND-OR
path circuit $C$ and recursively compute lower bounds for sub-circuits. We compared our delay to the resulting lower bound. Among all our solutions, $89\%$ achieve the lower bound and hence are provably delay-optimum, and only $0.012\%$ exceed the lower bound by $2$.

Figure 6 compares our realization with [10] on an example
instance. In our circuit, the splits (6)*, (7) and (7)* were applied,
and the ability to optimize undetermined circuits was used twice.
This way, our delay of $22$ is better than the delay found by [10], and it is even optimum since the input with arrival time $20$ has to traverse at least $2$ gates in any solution. On this instance, we need one more
gate than [10]. In general, the number of gates used by our algorithm
(with our modification for size reduction) is typically higher than in
[3], [10], [20], but mostly in the range of $20\%$.

In a second set of experiments, we examined our logic optimization framework as a whole. Table 1 shows results on recent $7nm$
pre-routing designs using the RICE delay model. The 'init' row displays
the state of the chips as in our application in industry: a timing-driven

![Diagram](https://example.com/diagram1.png)

Fig. 4: A subpath $S$ of the critical path $P$ before (left) and after
normalization (right). On the right, the extracted AND-OR path $S''$
is colored. Critical wires are drawn in red.

![Diagram](https://example.com/diagram2.png)

Fig. 5: Delay gain of the solutions computed by Algorithm 2
compared to the best solution among [3], [10], [20] on instances
with random integral input arrival times.
placement has been computed, followed by various timing optimization steps, among those our buffering and gate sizing sub-routines. The initial netlist cannot be improved any further by classical timing optimization. The ‘LO’ row shows results after applying our logic optimization. This does not disrupt global objectives as area, delay, and size.

V. CONCLUSION

We presented a new approximation algorithm for delay optimization of AND-OR paths and a logic optimization framework using this algorithm to improve critical paths in large, physical design. Regarding a simple, but realistic delay model, our algorithm fulfills best known mathematical guarantees, outperforms previously best approaches and is often optimum. Results on industrial 7nm designs demonstrate that our logic optimization framework improves timing when traditional timing optimization tools are at an end.

| Unit | Run | WS [ps] | TS [ns] | #Gates | Area | Netlength | ACES | T [s] |
|------|-----|---------|--------|--------|------|-----------|-------|------|
| i1   | init | 201     | 15.3   | 40 636 | 85 % |           |       | 86 % | 12  |
| i2   | init | 62      | 52.2   | 62 185 | 96 % |           |       |      |     |
| i3   | init | 109     | 192.9  | 69 049 | 107% |           |       |      |     |
| i4   | init | 5       | 0.1    | 78 030 | 99 % |           |       |      |     |
| i5   | init | 159     | 345.8  | 210 828| 94 % |           |       |      |     |
| i6   | init | 34      | 13.0   | 260 744| 89 % |           |       |      |     |
| i7   | init | 92      | 251.5  | 272 020| 96 % |           |       |      |     |
| i8   | init | 136     | 850.1  | 327 807| 90 % |           |       |      |     |

**TABLE I:** Performance of our logic restructuring framework on 7nm real-world instances.

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