Design, modelling and simulation of controlled sepic DC-DC converter-based genetic algorithm

Mohammed Omar Ali¹, Ali Hussein Ahmad²
¹Department of Electrical Power Techniques Engineering, Al-Hussain University College, Karbala, Iraq
²Medical Instrumentation Techniques Department, Al-Hadi University College, Baghdad, Iraq

ABSTRACT

This paper discusses various aspects of a single-ended primary inductance DC-DC converter (SEPIC). The focus is on design, modelling, and simulation results of a SEPIC converter. The study analyses the principle of SEPIC operation when operated in continuous conduction mode (CCM). Additionally, the mathematical equations for the design modules are calculated as per converter requirements. State-space equations are used to formulate the state-space model of the SEPIC converter. To satisfy the best-performance criterion of the system, the parameters for controller (K_p, K_i, K_d) should be tuned or optimized using the genetic algorithm (GA) optimization technique. Controller parameters are determined using an objective function that minimises the integral time absolute error (ITAE). Simulations performed on a closed-loop system reveal that the step response with a PID controlled based GA displayed superior performance. A closed-loop system has a substantially bigger stability region compared to an open-loop system. The simulation optimised performance metrics like maximum overshoot percentage (M_p), rise time (t_r), and settling time (t_s).

MATLAB/Simulink R2018a® and m-file code are used for the system modelling, simulation, and optimization of the PID controller parameters based on the GA.

This is an open access article under the CC BY-SA license.

1. INTRODUCTION

The power shortage relative to the cumulative demand for load is considered to be a major problem in many countries where it has become impossible to generate sufficient energy using traditional means. These difficult situations have led researchers to focus on finding alternative ways to generate energy [1, 2]. Power electronic converters such as DC-DC converters (sometimes called switching regulators) are primarily implemented to improve energy conversion efficiency when extracting electric power [3]. DC-DC converters are circuits which typically supply a constant output and convert DC voltage to a different voltage level. These are used for obtaining stabilized or changing DC voltage(s) by increasing, decreasing, or multiplexing from any DC source [4, 5].

There are two types of DC-DC converters, isolated and non-isolated. Flyback and forward converters are variants of isolated DC-DC converters [6]. These use a high-frequency transformer to place an electrical barrier and isolate both the input and output of these converters. A significant advantage of isolated converters is that they protect sensitive loads [7]. On the other hand, non-isolated DC-DC converters have no
Design, modelling and simulation of controlled sepic DC-DC converter-based … (Mohammed Omar Ali)
The corresponding equations to state I of CCM using KVL and KCL are shown in (1), (2), (3), and (4).

\[
\begin{align*}
V_S &= L_1 \frac{di_{L1}}{dt} = 0 \quad (1) \\
\frac{dV_{C1}}{dt} + i_{L1} &= 0 \quad (2) \\
L_2 \frac{di_{L2}}{dt} - V_{C1} &= 0 \quad (3) \\
C_2 \frac{dV_{C2}}{dt} + \frac{V_{C2}}{R} &= 0 \quad (4)
\end{align*}
\]

2.1.2. State I (0 < t < D)

When switch \( S_1 \) is turned off, the capacitor input current \( (I_{C1}) \) equals the current through the inductor \( (I_{L1}) \). Current \( I_{L2} \) remains in the negative direction and does not reverse its direction. Diode \( D_1 \) actively conducts. SEPIC converter operation mode with switch \( S_1 \) OFF is depicted in Figure 3.

The corresponding equations to state II of CCM using KVL and KCL are shown in (5), (6), (7), and (8).

\[
\begin{align*}
V_S &= L_1 \frac{di_{L1}}{dt} + V_{C1} + V_{C2} \quad (5) \\
L_2 \frac{di_{L2}}{dt} + V_{C2} &= 0 \quad (6) \\
\frac{dV_{C1}}{dt} - i_{L1} &= 0 \quad (7) \\
\frac{dV_{C2}}{dt} - i_{L1} - i_{L2} + \frac{V_{C2}}{R} &= 0 \quad (8)
\end{align*}
\]

2.2. State space modelling of SEPIC DC-DC converter

The general state space equations for the SEPIC operating under state I of CCM can be given as in equations (9) and (10).

\[
\begin{align*}
\dot{x}(t) &= A_1 x(t) + B_1 u(t) \\
y(t) &= C_1 x(t)
\end{align*}
\]

Then, the state matrix for the SEPIC operating under state I is given in (11) and (12).

\[
\begin{align*}
\begin{bmatrix}
\frac{di_{L1}}{dt} \\
\frac{di_{L2}}{dt} \\
\frac{dV_{C1}}{dt} \\
\frac{dV_{C2}}{dt}
\end{bmatrix} &=
\begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{L_2} & 0 \\
0 & {1 \over C_1} & 0 & 0 \\
0 & 0 & 0 & \frac{1}{RC_2}
\end{bmatrix}
\begin{bmatrix}
i_{L1} \\
i_{L2} \\
V_{C1} \\
V_{C2}
\end{bmatrix} +
\begin{bmatrix}
1 \\
0 \\
0 \\
0
\end{bmatrix} V_S \\
y(t) &= \begin{bmatrix}
0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
i_{L1} \\
i_{L2} \\
V_{C1} \\
V_{C2}
\end{bmatrix}
\end{align*}
\]
Similarly, the general state equations for the SEPIC converter operating under state II of CCM are given in (13) and (14).

\[
\dot{x}(t) = A_2 x(t) + B_2 u(t) \quad \text{(13)}
\]

\[
y(t) = C_2 x(t) \quad \text{(14)}
\]

Then, the state matrix for the SEPIC converter operating under state II can be given as shown in (15) and (16).

\[
\begin{bmatrix}
\frac{d}{dt}i_{L1} \\
\frac{d}{dt}i_{L2} \\
\frac{d}{dt}v_{C1} \\
\frac{d}{dt}v_{C2}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\
0 & 0 & 0 & -\frac{1}{L_2} \\
\frac{1}{C_1} & 0 & 0 & 0 \\
\frac{1}{C_2} & 0 & 0 & -\frac{1}{RC_2}
\end{bmatrix}
\begin{bmatrix}
i_{L1} \\
i_{L2} \\
v_{C1} \\
v_{C2}
\end{bmatrix} +
\begin{bmatrix}
\frac{1}{L_1} \\
\frac{1}{L_2} \\
0 \\
0
\end{bmatrix} V_S \quad \text{(15)}
\]

\[
y(t) =
\begin{bmatrix}
i_{L1} \\
i_{L2} \\
v_{C1} \\
v_{C2}
\end{bmatrix} \quad \text{(16)}
\]

The average form of the state matrix over a switching cycle for the SEPIC converter is as given in (17) and (18).

\[
\begin{bmatrix}
\frac{d}{dt}i_{L1} \\
\frac{d}{dt}i_{L2} \\
\frac{d}{dt}v_{C1} \\
\frac{d}{dt}v_{C2}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & \frac{D-1}{L_1} & \frac{D-1}{L_1} \\
0 & 0 & \frac{D-1}{L_2} & \frac{D-1}{L_2} \\
\frac{1-D}{C_1} & 0 & -\frac{D}{C_1} & 0 \\
\frac{1-D}{C_2} & 0 & 0 & -\frac{1}{RC_2}
\end{bmatrix}
\begin{bmatrix}
i_{L1} \\
i_{L2} \\
v_{C1} \\
v_{C2}
\end{bmatrix} +
\begin{bmatrix}
\frac{1}{L_1} \\
\frac{1}{L_2} \\
0 \\
0
\end{bmatrix} V_S \quad \text{(17)}
\]

\[
y(t) =
\begin{bmatrix}
i_{L1} \\
i_{L2} \\
v_{C1} \\
v_{C2}
\end{bmatrix} \quad \text{(18)}
\]

Where A represents the system matrix, B represents the input matrix, C represents the output matrix, and D represents the duty cycle of the SEPIC converter within the range of (0–1).

2.3. Component design of SEPIC DC-DC converter

It is necessary that the selection of the main components in the converter design improve the output power efficiency without increasing cost, especially in high-volume power electronic applications. Based on the above, this section of paper focuses on choosing components and deriving their mathematical expressions when designing a SEPIC DC-DC converter to meet the requirements tabulated in 1.

2.3.1. Component design of SEPIC DC-DC converter

The principle of volt-second balance takes into account the voltage drops at diode (D1), i.e. according states to the volt-second balance for a converter operating in a steady state, the average voltage during one switching cycle of the inductor must be zero [16]. Firstly, the voltage can be seen by L1 during interval \((0 < t \leq D_T)\) equals to \((V_{L1} = V_s)\), while, during the interval \((D_T < t \leq T)\), it equals \((V_{L1} = V_S - V_{C1} - V_D - V_O)\). Taking the average over the entire interval and making it equal to zero, equation (19) can be obtained as:

\[
\frac{1}{T} \left( \int_{0}^{T} V_{L1} dt \right) = \frac{1}{T} \left[ \int_{0}^{D_T} V_S dt + \int_{D_T}^{T} (V_S - V_{C1} - V_D - V_O) dt \right] = 0 \quad \text{(19)}
\]

Finding the integral and rearranging the above equations yields equation (20)

\[
V_{C1} + V_D + V_O = \frac{V_S}{1-D} \quad \text{(20)}
\]
Similarly, by taking the volt-second balance for $L_2$. Hence, the voltage can be seen by $L_2$ during interval $(0 < t \leq D_T)$ is equal to $(V_{L2}=V_{C1})$, while during the interval $(D_T < t \leq T)$, the voltage is equal to $V_{L2}=V_{O}+V_{D}$ which gives (21).

$$\frac{1}{T}\left(\int_0^T V_{L2} dt\right) = \frac{1}{T}\left[\int_0^{DT} V_{C1} dt + \int_{DT}^T (-V_{O} - V_{D}) dt\right] = 0$$

(21)

$$V_{C1} + V_{O} + V_{D} = \frac{V_{O}+V_{D}}{D}$$

(22)

By combining (20) and (22), the transfer ratio or voltage gain $(G)$ of the SEPIC converter in terms of $(D)$ can be obtained as shown in (23).

$$G = \frac{V_{O}+V_{D}}{V_S} = \frac{D}{1-D}$$

(23)

The value of $(G)$ can be greater than or less than one, depending on the value of the duty cycle $(D)$.

### 2.3.2. Calculation of minimum and maximum duty cycle

Depending on the voltage gain in equation (23), the minimum duty cycle $(D_{\text{min}})$ occurs when the input voltage is at a maximum value $(V_{S_{\text{max}}})$ and it can be expressed as shown in (24).

$$D_{\text{min}} = \frac{V_{O}+V_{D}}{V_O+V_D+V_{S_{\text{max}}}}$$

(24)

However, the maximum duty cycle $(D_{\text{max}})$ may occur when the input voltage is at a minimum value $(V_{S_{\text{min}}})$, as given in (25).

$$D_{\text{max}} = \frac{V_{O}+V_{D}}{V_O+V_D+V_{S_{\text{min}}}}$$

(25)

### 2.3.3. Inductor $L_1$ and $L_2$ selection

In switch mode power supply (SMPS), the main function of the inductors is to store energy in their magnetic field and attempt to maintain a constant current, or equivalently, to limit the rate of change in current flow to the output. Selecting an inductor is necessary to the overall design of a converter. Normally, the inductance value of a converter should be set to limit the peak-to-peak ripple current flowing to the output. The inductance value that satisfied the requirements in the design of the SEPIC converter was estimated by rearranging (1), presented in the previous section, and substituting $(dL = \Delta L, \ dt = DT, \ T = \frac{1}{f_s})$, to yield (26).

$$L_1 = L_2 = \frac{V_{S_{\text{min}}}D_{\text{max}}}{f_s\Delta L}$$

(26)

### 2.3.4. Coupling capacitor $C_1$ selection

Capacitors have several functions in SMPS design, such as energy storage, filtering, compensation, etc. Typically, SMPS stages, the capacitance stores energy as an electric field due to the voltage applied and attempts to maintain a constant input and output voltage. To calculate the optimal value of $(C_1)$ in the SEPIC converter circuit shown in Figure 1 with an acceptable level of voltage ripple to satisfy the requirements and stability of the converter, the capacitance formula shown in (27) was used.

$$C = \frac{\Delta Q}{\Delta V}$$

(27)

Equation (27) can then be rewritten, as the change in voltage is proportional to the change in charge over its capacitance, which yields (28).

$$\Delta V = \frac{\Delta Q}{C}$$

(28)

However,

$$\Delta Q = \int i(t) dt$$

(29)
Thus, (29) is substituted into (28) to determine the value of input capacitor ($C_1$) as shown in (30). Hence, it should be noted that ($C_1$) is charged by ($I_{L2} = I_{O_{max}}$) during the time interval ($0 < t \leq DT$).

$$C_1 = \frac{\int_{0}^{DT} I_{o} \, dt}{\Delta V_{C1}}$$

(30)

Solving the integration shown in (30) gives (31).

$$C_1 = \frac{I_{o_{max}} \cdot D_{max}}{\Delta V_{C1} \cdot f_s}$$

(31)

2.3.5. Output capacitor $C_2$ selection

Likewise, as in the coupling capacitor ($C_1$) calculation, the value of output capacitor ($C_2$) as obtained in (32) should supply the output current ($I_{O_{max}}$) which is loaded during the ON state.

$$C_2 = \frac{I_{o_{max}} \cdot D_{max}}{\Delta V_{C2} \cdot f_s}$$

(32)

Where $D_{min}, D_{max}$ are the maximum and minimum duty cycles respectively, $V_{s_{max}}, V_{s_{min}}$ are maximum and minimum input voltages respectively, $V_o$ is the output voltage in volts, and $\Delta I_L$ is the same peak-to-peak ripple current in amperes for both inductors $L_1$ and $L_2$ when the minimum input voltage ($V_{s_{min}}$) and switching frequency ($f_s$) are applied, it may be expressed as approximately ($\Delta I_{L}=20\% \cdot I_{in \, max}$). $\Delta V_{C1}$, $\Delta V_{C2}$ are the peak-to-peak voltage ripples in volts at capacitors $C_1$ and $C_2$, respectively. The acceptable percentage value of ripple voltage used in this paper is ($\Delta V_{C1}=1\% \cdot V_{s_{min}}$ and $\Delta V_{C2}=1\% \cdot V_o$).

2.4. Matlab simulation of SEPIC DC-DC converter

The open loop SEPIC DC-DC converter was implemented using the MATLAB® simulation platform R2018b Simulink [18]. For the purpose of simulation, the components of the SEPIC converter and their values tabulated in the Table 1 depend on the equations derived in pervious sections.

| No. | Parameter | Symbol | Value |
|-----|-----------|--------|-------|
| 1   | Minimum input voltage | $V_{s_{min}}$ | 100 V |
| 2   | Maximum input voltage | $V_{s_{max}}$ | 120 V |
| 3   | Output voltage | $V_o$ | 311 V |
| 4   | Maximum output power | $P_{o_{max}}$ | 2 Kw |
| 5   | Maximum load resistance | $R_{L_{max}}$ | ~ 50 Ω |
| 6   | Maximum load current | $I_{o_{max}}$ | 6.43 A |
| 7   | Switching frequency | $f_s$ | 25 kHz |
| 8   | Diode drop voltage | $V_d$ | 0.7 V |
| 9   | Minimum duty cycle | $D_{min}$ | 0.722 |
| 10  | Maximum duty cycle | $D_{max}$ | 0.757 |
| 11  | Current ripple at $L_1$, $L_1$ | $\Delta I_L$ | 4.01 A |
| 12  | Voltage ripple at $C_1$ | $\Delta V_{C1}$ | 1 V |
| 13  | Voltage ripple at $C_2$ | $\Delta V_{C2}$ | 3.11 V |
| 14  | Coupling capacitor | $C_1$ | 195 μF |
| 15  | Output capacitor | $C_2$ | 63 μF |
| 16  | Inductor 1 | $L_1$ | 755 μH |
| 17  | Inductor 2 | $L_2$ | 755 μH |

The output to the input voltage transfer function, $G(s)$ can be derived from the average state (17) and (18) by using the formula to convert the state-space matrix to a transfer function, shown in (33), and substituting the values of the design parameters and components to obtain (34).

$$G(s) = C \cdot (S \cdot I - A)^{-1} \cdot B$$

(33)

$$\frac{V_o(s)}{V_{in}(s)} = \frac{5.135 \cdot 10^9 \cdot S^2 + 1.824 \cdot 10^{-6} \cdot S + 2.64 \cdot 10^{15}}{S^4 + 330.2 \cdot S^3 + 6.79 \cdot 10^6 \cdot S^2 + 1.419 \cdot 10^9 \cdot S + 8.478 \cdot 10^{12}}$$

(34)
2.5. Genetic algorithm (GA)

GAs are stochastic global search engines that simulate the creation of natural processes. A GA starts with an initial population of chromosomes, each of which represents a possible solution to the problem, and the reliability of the chromosomes is evaluated by a fitness function (FF) [19, 20]. The GA consists of three main steps: mutation, crossover and selection [21]. GAs are used to determine the representation of the chromosomes that are created by three values corresponding to the gains or parameters of the PID controller \((K_p, K_i, K_d)\) that have been modified to attain a desired behavior [22–24]. The \((K_p, K_i, K_d)\) gains are real numbers, which are to be measured individually. The equation for the PID controller is shown as (35) [25]. In this study, the integral time absolute error (ITAE) is taken as the objective function, given as (36). The reciprocal of the objective function is called FF. The FF is the measurement of the chromosome’s quality.

\[
G_c(s) = K_p + \frac{K_i}{s} + K_d s
\]  
\[
ITAE = \int_0^T t |e(t)| dt
\]  

Where \(K_p\) is the proportional gain, \(K_i\) is the integral time, \(K_d\) is the derivative time, \(e(t)\) is the error-controlling signal = 1 – \(y(t)\) and \(y(t)\) is the tuned control system step response. Figure 4 shows a flowchart for GA. The parameters of the GA are listed in Table 2.

| No | Parameter          | Type / Value       |
|----|--------------------|--------------------|
| 1  | No. of iteration   | 100                |
| 2  | Population size    | 50                 |
| 3  | Encoding           | Binary             |
| 4  | Selection scheme   | Stochastic Uniform |
| 5  | Crossover probability \(P_c\) | 0.8         |
| 6  | Crossover type     | Single Point       |
| 7  | Mutation probability \(P_m\) | 0.2        |
| 8  | Recombination probability \(P_r\) | 0.09      |
| 9  | Fitness function   | ITAE               |

Figure 4. Flowchart for genetic algorithm (GA)

The block diagram for the GA-optimized or tuned PID controller parameters for the SEPIC DC-DC converter can be seen in Figure 5. The reference signal or set point \(R(s)\) is input as the desired voltage and is compared with the actual value of the output voltage \(Y(s)\) for the SEPIC converter. The error signal \(E(s)\) is given as the input signal to the PID controller after its parameters are tuned using GA technique. The output signal generated by the PID controller \(U(s)\) is used as the input signal to control the suitable range of duty cycle \(D\) in a suitable range for the SEPIC converter, and the required output voltage is then obtained [26].
3. RESULTS AND DISCUSSION

MATLAB® R2018b Simulink software was used to simulate the SEPIC DC-DC converter and verify its performance. Figure 6 (a) shows the step response of the open-loop transfer function for the SEPIC DC-DC converter without the PID controller. It is observed that the response matches the step response for a second-order system. However, the maximum overshoot percentage (close to 73%) is higher than that of the second-order system. Slow rise and settling times are also observed. Figure 6 (b) depicts the closed-loop step response for a GA optimised PID controller. The PID controller parameters ($K_p, K_i, K_d$) are set to their optimal value using the GA technique. This technique helps minimise the objective function (ITAE) and the optimisation process depends on the code specified in the MATLAB m-file. Table 3 specifies the optimisation criteria and the performance characteristics for the step response like ($M_p, t_r, t_s$).

![Figure 5](image_url)

**Figure 5.** Block diagram of PID controller optimized by GA

![Figure 6](image_url)

**Figure 6.** Simulation results, (a) Step response for SEPIC converter without controller, (b) Step response for SEPIC converter with GA-PID controller

| Performance Parameters | Type of controller |
|------------------------|--------------------|
| Without PID controller | With GA-PID controller |
| $K_p$                  | N/A                | 69.805 |
| $K_i$                  | N/A                | 290.779 |
| $K_d$                  | N/A                | 339.306 |
| % $M_p$                | 73                 | 0 |
| $t_r$ (sec)            | 8.9246 e-04        | 1.2610 e-11 |
| $t_s$ (sec)            | 0.0301             | 2.2454 e-11 |
| ITAE                   | N/A                | 2.7182 e-06 |

Table 3 Performance Parameters for step response
4. CONCLUSION

This paper presents design, modelling and simulation of controlled SEPIC DC-DC converter-based GA. The study comprised the mathematical model, state-space modelling, design components, simulation, and analysis of the SEPIC DC-DC converter. MATLAB R2018b SIMULINK was used to carry out the simulations. The SEPIC DC-DC converter is a time-invariant, linear system of the fourth order. A PID controller was utilised to change the output of the SEPIC converter to optimise the values of the performance parameters. PID controller parameters $K_p$, $K_i$, $K_d$ were manipulated using the GA technique to determine their optimal values intelligently. Optimisation was performed with ITAE serving as the fitness function. The results of the simulation and the study indicate that the closed-loop step response system performed best in conjunction with a PID controller with optimised parameters. Maximum overshoot percentage rise and settling times were optimised. Additionally, the GA-PID controller was more accurate and better sensitivity against disturbances when compared to using it without the PID controller.

REFERENCES

[1] M. Gaetani, T. Huld, E. Vignati, F. Monforti-Ferrario, A. Dosio, and F. Raes, “The near future availability of photovoltaic energy in Europe and Africa in climate-aerosol modeling experiments,” Renew. Sustain. Energy Rev., vol. 38, pp. 706–716, 2014.

[2] Z. Ming, L. Ximei, L. Na, and X. Song, “Overall review of renewable energy tariff policy in China: evolution, implementation, problems and countermeasures,” Renew. Sustain. Energy Rev., vol. 25, pp. 260–271, 2013.

[3] Y.-P. Hsieh, J.-F. Chen, T.-J. Liang, and L.-S. Yang, “Novel high step-up DC-DC converter for distributed generation system,” IEEE Trans. Ind. Electron., vol. 60, no. 4, pp. 1473–1482, 2011.

[4] D. W. Hart, “Power electronics,” Tata McGraw-Hill Education, 2011.

[5] F. L. Luo and H. Ye, “Advanced dc/dc converters, Second. cpe Press, 2016.

[6] R.-J. Wai, C.-Y. Lin, R.-Y. Duan, and Y.-R. Chang, “High-efficiency DC-DC converter with high voltage gain and reduced switch stress,” IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 354–364, 2007.

[7] B. York, W. Yu, and J.-S. Lai, “An integrated boost resonant converter for photovoltaic applications,” IEEE Trans. Power Electron., vol. 28, no. 3, pp. 1199–1207, 2012.

[8] N. Siddharthan and B. Balasubramanian, “Performance evaluation of SEPIC, Luo and ZETA converter,” International Journal of Power Electronics and Drive System, vol. 10, no. 1, p. 374, 2019.

[9] R. K. Pachauri and Y. K. Chauhan, “Modeling and simulation analysis of PV fed Cuk, Sepic, Zeta and Luo DC-DC converter,” in 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), pp. 1–6, 2016.

[10] F. L. Luo, H. Ye, and M. H. Rashid, “Digital power electronics and applications,” Elsevier, 2010.

[11] I. Alhamrouni, M. K. Rahmat, F. A. Ismail, M. Salem, A. Juoh, and T. Sutikno, “Design and development of SEPIC DC-DC boost converter for photovoltaic application,” International Journal of Power Electronics and Drive System, vol. 10, no. 1, pp. 406–413 2019.

[12] S. J. Chiang, H.-J. Shieh, and M.-C. Chen, “Modeling and control of PV charger system with SEPIC converter,” IEEE Trans. Ind. Electron., vol. 56, no. 11, pp. 4344–4353, 2009.

[13] R. Palanisamy, K. Vijayakumar, V. Venkatachalam, R. M. Narayanan, D. Saravanakumar, and K. Saravanan, “Simulation of various DC-DC converters for photovoltaic system,” International Journal Electrical and Computer Engineering, vol. 9, no. 2, p. 917, 2019.

[14] H.-J. Chiu, Y.-K. Lo, J.-T. Chen, S.-J. Cheng, C.-Y. Lin, and S.-C. Mou, “A high-efficiency dimmable LED driver for low-power lighting applications,” IEEE Trans. Ind. Electron., vol. 57, no. 2, pp. 735–743, 2009.

[15] T. Arunkumari, I. Jagadeesh, and V. Indragandhi, “Design and implementation of modified multilevel sepic converter for PV applications,” Indones. J. Electr. Eng. Comput. Sci., vol. 14, no. 3, pp. 1125–1133, 2019.

[16] M. R. M. N. Venkatanarayanan, “Design and Implementation of SEPIC and Boost Converters for Wind and Fuel Cell Applications,” Int. J. Innov. Res. Sci. Eng. Technol., vol. 3, no. 3, pp. 378–383, 2014.

[17] S. A. Yasin, J. Kumar, Y. Kumar, S. Athikhal, and J. Peter, “Analysis of a Dual Input DC-DC Converter Topology Based on SEPIC Configuration,” in 2019 International Conference on Power Electronics Applications and Technology in Present Energy Scenario (PETPES), pp. 1–6, 2019.

[18] G. Sureshkumar, N. Kannan, S. Thomas, and S. P. Karthikeyan, “Matlab/simulink simulations based modified sepic dc to dc converter for renewable energy applications,” J. Adv. Res. Dyn. Control Syst., vol. 11, no. 4, pp. 285–295, 2019.

[19] I. A. Humied, “Solving N-Queens Problem Using Subproblems based on Genetic Algorithm,” IAES International Journal Artificial Intelligence, vol. 7, no. 3, pp. 130–137, 2018.

[20] R. L. Haupt and S. E. Haupt, “Practical genetic algorithms,” second edi. John Wiley & Sons, 2004.

[21] J. J. Roberts, A. M. Cassula, J. L. Silveira, P. O. Prado, and J. C. F. Junior, “GAtoolbox: a Matlab-based Genetic Algorithm Toolbox for Function Optimization, “ in the 12th latin-american congress on electricity generation and transmission-clagee, vol. 12, 2017.

[22] N. A. M. Kamari, I. Musirin, A. A. Ibrahim, and S. A. Halim, “Intelligent swarm-based optimization technique for oscillatory stability assessment in power system,” IAES International Journal Artificial Intelligence, vol. 8, no. 4, pp. 342-351, 2019.
Design, modelling and simulation of controlled sepic DC-DC converter-based … (Mohammed Omar Ali)

BIOGRAPHIES OF AUTHORS

Mohammed Omar Ali was born in Babylon, Iraq, in 1986. He received the B.Sc. degree in Electrical Engineering from Babylon University, Iraq, in 2008, the M.Sc. degree in Power and Machines from Baghdad University, Iraq, in 2014. He is currently working towards the Ph.D. degree in Electric Power at department of Electrical Engineering, University of Technology Baghdad, Iraq. His research interests modeling, simulation, analysis, and implementation of fractional order regulated electric power converters. He is Assistant Lecturer with Al-Hussein University College, Karbala, Iraq, from 2014 until the present.

Ali Husain Ahmad was born in Fadellia, Ninavah, Iraq, in 1951. He received the B.Sc. degree in Electrical Engineering/Power and machine in 1976, the P.G. Diploma in Electrical Engineering/Power and Machine in 1977, the M.Sc. in Electrical Engineering/Power Electronics in 1979, all from university of Mosul College of Engineering, Electrical Eng. Dept., and the Ph.D. degree from Technical University Sofia, Bulgaria in 1990. He worked as a dean scientific assistant in control and computer engineering department University of Technology, Baghdad, Iraq for the academic year 2002/2003. He became an assistant professor in 2003. Now he is working with Al-Hadi University College as a head of Medical Instrumentation Techniques Engineering Department from October 2019 up to now. The fields of his research interests are control and power electronics.