Mitigation of Harmonics for Eleven-Level Cascaded Multilevel Inverter using SPWM and SHE Techniques

S Sreelakshmi, M S Sujatha
1Department of Electrical and Electronics Engineering, Jawaharlal Technological University, Anantapuramu, AP, India
2Center for Energy, Sree Vidyakethan Engineering College, Tirupati, AP, India

Abstract
Multilevel inverters became special attention in power electronics. The advantage of multilevel inverters is several levels of DC voltages are synthesized into a desired sinusoidal waveform. There are many topologies existed in literature like 1) Diode-clamped multilevel inverter, 2) Flying capacitor multilevel inverter, and 3) Cascaded multilevel inverter. First two topologies have a disadvantage of more number of components and gate driver circuits. This will lead to increase in losses and the total harmonic distortion is also more. So the quality of power is reduced. To overcome these drawbacks cascaded multilevel topology has been developed which is having less number of components and gate driver circuits. Thereby losses and THD (Total Harmonic Distortion) reduces and quality of power increases. The developed topology is analyzed for 11-level by using Phase Opposition Sinusoidal Pulse Width Modulation (PO-SPWM) Technique and also compared with novel SHE(Selective Harmonic Elimination) technique in terms of THD and quality of power for different modulation indices. The work is carried with MATLAB 2017b version.

Keywords
Cascaded Full-bridge Inverter, Total Harmonic Distortion (THD), Phase Opposition Sinusoidal Pulse Width Modulation and Selective Harmonic Elimination (SHE).

Introduction
An inverter can convert the dc power to ac power. If conversion efficiency of the inverter is more, the quality of power conversion from dc to ac is also more. To increase the quality of power needed to decrease the losses. To reduce the losses number of components has to reduce. For this many topologies have developed. Further, the topologies are controlled by different PWM techniques and modulation index are stated in [1]-[11]. Some of them discussed briefly. Kahwa [12] et.al has developed a new topology with less number of components without changing the advantages of the basic H-bridge inverter using SPWM technique. The THD is less but the complexity of the circuit increases. Gowrishankar and Edward [13][14] has developed symmetrical and asymmetrical multilevel inverters with respect to equal and unequal dc voltage sources using phase disposition PWM technique for 15-level and also developed 31-level cascaded inverter with unequal DC sources with low-frequency pulse width modulation. J.Lakwal and Dubey [15] has developed a single phase multilevel inverter for the application of PV system with DC sources having unequal magnitude using Super Imposed Carrier Pulse Width Modulation Technique. Ehsan Najafi[16][17] et.al, has developed a topology with reversing the voltage across a component to improve the inverter performance. It is operated at high and low switching frequencies; the control technique used is Phase Disposing-Sinusoidal Pulse Width Modulation. Gui-Su [18] has developed a topology containing multilevel cell unit with DC source and an inverter bridge connected through a DC-link. The levels of DC voltage are synthesized to the desired sine wave with or without performing the PWM technique. The multi-cell unit contains the number of components and the losses become more. Vraj Shah and Jariwala has developed two topologies, topology-I only discussed 7, 9 &11 levels and topology-II for 19-level using direct pulse modulation technique. The drawback is the complexity of the circuit is more, capacitors are used which is more costly. Armi, Faouzi, Lazhar Manai, and Mongi Besbes [21] have given the Selective Harmonic Elimination algorithm for harmonic elimination. Sanka and Machineni [22] have discussed recent progress on multilevel inverters and its applications.

The proposed work gives the comparison of THD for PO-SPWM (at 10 KHZs) and SHE (at 50 HZs) techniques for different modulation indices.

Eleven Level Cascaded Inverter
The principle of inverter is to convert direct voltage/power to alternating voltage/power. The conversion efficiency of the inverter is more than 96%. Still the conversion efficiency can be increased by improving the design of inverter and control strategy. Fig 1 shows the block diagram for the inverter and its classification. The advantages and disadvantages of the diode-clamped, flying capacitor and cascaded multilevel inverters are discussed in [18][21]. All the structures are containing more number of components; the losses are more the efficiency of the inverter is decreased, to achieve better output voltage and THD decrease the switching components or change the Modulation Index (MI) in the range of zero to one.
The schematic diagram for the eleven-level cascaded full-bridge inverter is shown in Fig 2. The number of full-bridge cells used is \((m-1)/2 = 5\), where \(m\) indicates the number of output voltage levels. Each cell contains four MOSFETs and one DC source. The source voltage is equal in magnitude taking 100V each. The switching frequency of MOSFET is 10 KHz and a resistive load of 100 ohms is considered. Switching pulses are generated by Sinusoidal Pulse Width Modulation and Selective Harmonic Elimination techniques.

**Switching Techniques**

**Eleven Level Cascaded Inverter With PO-SPWM Technique**

The SPWM technique contains multiple carrier waves (saw tooth) and reference (sinusoidal) wave. Whenever the carrier wave cuts the reference wave pulses will be generated. The magnitude of the pulses will be depending on the reference wave and also on the range of modulation index. Fig 3 shows the block diagram of SPWM technique for cascaded H-bridge inverter.
Fig 4 shows the ten carrier waves and one reference wave for 11 level generation using SPWM technique. As we know the SPWM technique will give unequal widths and magnitudes of pulse rather than equal magnitudes and widths. The distortion of magnitude and widths will give the less harmonic distortion.

![Fig 4: Carrier Waves and Reference Waves for 11 Level Generation PO-SPWM.](image)

Modulation Index (MI) is defined as the ratio of $V_r$ to $V_c$ and it controls the triggering pulses of the gate driver circuit of cascaded MLI. Where $V_r$ is reference voltage and $V_c$ is carrier voltage amplitudes. In general, MI is considered between ‘0’ to ‘1’; here MI is assigned to a range of 0.166 to 1.

![Fig 5: Generation of Pulses for 11 Level Inverter using PO-SPWM Technique](image)

Fig 5 gives the pulses for the 11 level cascaded multilevel inverter, the levels are +1V, +2V, +3V, +4V, +5V, 0V, -1V, -2V, -3V, -4V, -5V.

**Simulation Results**

Fig 6 shows the simulation results for eleven level cascaded multilevel inverter using PO-SPWM technique having Modulation Index of 0.866. This is giving less harmonic distortion.
Fig 6: Simulation Results for Eleven Level Cascaded Multilevel Inverter using PO-SPWM Technique.

Fig 7 (a), (b), (c), (d), (e), (f), (g), (h), (i), (j) gives THD values of 11 level multilevel inverter for Modulation Index, MI=0.166, 0.266, 0.366, 0.466, 0.566, 0.666, 0.766, 0.866, 0.966, 1.0 respectively.
Table 1: THD Values for Different Modulation Indices

| Modulation index | PO-SPWM %THD(simulation) |
|------------------|---------------------------|
| 0.166            | 31.60                     |
| 0.266            | 28.38                     |
| 0.366            | 16.43                     |
| 0.466            | 14.17                     |
| 0.566            | 12.46                     |
| 0.666            | 9.67                      |
| 0.766            | 9.90                      |
| 0.866            | 7.30                      |
| 0.966            | 9.39                      |
| 1.000            | 9.83                      |

Table 1 shows the THD values for different modulation index range of 0.166 to 1 for eleven level cascaded multilevel inverter by PO-SPWM. From the Table 1, it is noticed that for Modulation Index (MI) = 0.866 giving better results when compared to the other modulation values.

Eleven Level Cascaded Inverter with Selective Harmonic Elimination (SHE) Technique.

Fig 8 shows block diagram of SHE technique for cascaded H-bridge inverter. This is worked on fundamental switching frequency. In the fundamental frequency switching technique the lower THD is obtained by suppressing some selected harmonics through the optimized switching angles. These optimized switching angles are generated by solving the nonlinear equations. To solve nonlinear equations Fourier analysis is used.
To solve the above nonlinear equations the following matrix equations are needed in the Newton Rapson method.

Where Modulation Index (MI) is equal to $\frac{V_1}{V_{1_{\text{max}}}}$, Where MI is modulation index

The Modulation Index and generated switching angles can give pure sine with the low THD by solving the following transcendental nonlinear equations (4) known as SHE equations that characterize the selected harmonics. The challenge lies here is to guess the initial switching angles in the range of $0 \leq \theta_1 < \theta_2 < \ldots < \theta_s \leq \pi/2$ for SHE technique. This technique allows only fundamental frequency and eliminates the 5th, 7th, 11th, 13th higher harmonics in the line-to-line voltages.

The equations for this condition can be written as,

$$(\cos(\theta_1) + \cos(\theta_2) + \ldots + \cos(\theta_s)) = \text{SMI}$$

$$(\cos(5\theta_1) + \cos(5\theta_2) + \ldots + \cos(5\theta_s)) = 0$$

$$(\cos(7\theta_1) + \cos(7\theta_2) + \ldots + \cos(7\theta_s)) = 0$$

$$(\cos(11\theta_1) + \cos(11\theta_2) + \ldots + \cos(11\theta_s)) = 0$$

$$(\cos(13\theta_1) + \cos(13\theta_2) + \ldots + \cos(13\theta_s)) = 0$$

Where Modulation Index (MI) is equal to $rac{\pi V_1}{4SV_{dc}}$, for $0<\text{MI} \leq 1$. To solve the above nonlinear equations the following matrix equations are needed in the Newton Rapson method.

1) The initial guessing of switching angles is given in equation (5).

$$\theta^0 = [\theta_1 \; \theta_2 \; \theta_3 \; \theta_4 \; \theta_5]$$

Where $\theta_1 = (4.6983)$, $\theta_2 = (16.9596)$, $\theta_3 = (23.5486)$, $\theta_4 = (39.706)$, $\theta_5 = (59.4157)$, taken from reference [4].

2) The nonlinear function matrix is given by (6).

$$[F(\theta)] = \begin{bmatrix}
\cos(\theta_1) + \cos(\theta_2) + \ldots + \cos(\theta_s) \\
\cos(5\theta_1) + \cos(5\theta_2) + \ldots + \cos(5\theta_s) \\
\cos(7\theta_1) + \cos(7\theta_2) + \ldots + \cos(7\theta_s) \\
\cos(11\theta_1) + \cos(11\theta_2) + \ldots + \cos(11\theta_s) \\
\cos(13\theta_1) + \cos(13\theta_2) + \ldots + \cos(13\theta_s)
\end{bmatrix}.$$
Jacobian of matrix $F$ after simplification is given by
\begin{align}
\frac{dF(\theta)}{d\theta} = \begin{bmatrix}
    -\sin(\theta_1) & -\sin(\theta_2) & -\sin(\theta_3) & -\sin(\theta_4) & -\sin(\theta_5) \\
    -5\sin(5\theta_1) & -5\sin(5\theta_2) & -5\sin(5\theta_3) & -5\sin(5\theta_4) & -5\sin(5\theta_5) \\
    -7\sin(7\theta_1) & -7\sin(7\theta_2) & -7\sin(7\theta_3) & -7\sin(7\theta_4) & -7\sin(7\theta_5) \\
    -11\sin(11\theta_1) & -11\sin(11\theta_2) & -11\sin(11\theta_3) & -11\sin(11\theta_4) & -11\sin(11\theta_5) \\
    -13\sin(13\theta_1) & -13\sin(13\theta_2) & -13\sin(13\theta_3) & -13\sin(13\theta_4) & -13\sin(13\theta_5)
\end{bmatrix}; \quad (7)
\end{align}

3) The solution matrix
\begin{align*}
T &= [5MI 0 0 0 0]^T; \text{ where MI is (0.1 to 1)}
\end{align*}
\begin{align}
\frac{d\theta}{dF} &= \begin{bmatrix}
    dF(\theta) & 1 \\
    (T-\theta) & dF(\theta)
\end{bmatrix} \\
\theta_{\text{new}} &= \theta_{\text{old}} + d(\theta) \quad \text{(8)}
\end{align}

4) Calculate THD for each iteration, continue the process where the optimized switching angles and lower THD are obtained.

This is a system of five transcendental equations with five unknowns $\theta_1, \theta_2, \theta_3, \theta_4, \theta_5$ from equation (4) which mean that the output voltage of the 11-level inverter would not contain the 5th, 7th, 11th, and 13th order harmonic components. Fig 9 gives the flow chart for the SHE technique using the Newton Rapson method.

Fig. 9 gives the flow chart for the SHE technique using the Newton Rapson method. The steps followed in flowchart are, first guess the initial values of switching angles equation (5), next find the nonlinear function matrix equation (6), then find the Jacobean function matrix(7), next find the solution matrix equation (8), and then find the new switching angles and THD for the modulation range 0.166 to 1. Evaluate the results for better switching angles and THD.
Update values of $\theta_{new} = \theta_{old} + d(\theta)$

Find Jacobean matrix $d(\theta)$

Solve for $d(\theta)$

$\quad$ Sufficient to accuracy

Calculate THD

Evaluate THD for each

End

Fig 9: Flowchart for Newton Rapson Method.
Table 2: Comparison of THD for SPWM and SHE Techniques

| Modulation index | PO-SPWM %THD | SHE(mat lab coding) %THD |
|------------------|--------------|------------------------|
| 0.166            | 31.60        | 42.35                  |
| 0.266            | 28.38        | 29.04                  |
| 0.366            | 16.43        | 18.52                  |
| 0.466            | 14.17        | 11.063                 |
| 0.566            | 12.46        | 5.73                   |
| 0.666            | 9.67         | 4.37                   |
| 0.766            | 9.90         | 1.73                   |
| 0.866            | 7.30         | 1.51                   |
| 0.966            | 9.39         | 7.14                   |
| 1.000            | 9.83         | 8.09                   |

Table 2 shows the comparison of THDs for 11 levels cascaded multilevel inverter using SPWM and SHE technique (MATLAB coding) with different Modulation Indices. From the Table 1 and Table 2 it is noticed that Modulation Indices (MI) = 0.866 is giving better results when compared to the other modulation values in both SPWM and SHE techniques. But THD obtained is less for SHE technique compared to SPWM technique. This shows that the SHE technique is superior to SPWM technique.

Conclusions
The work carried out for cascade eleven level multilevel inverter using SPWM and SHE techniques for different modulation indices between (0.666 to 1). In this range the lowest harmonic distortion is obtained for MI=0.866 in both techniques. But THD obtained for SHE technique is less (1.51) compared to SPWM technique (7.3). From this it is concluded that SHE technique is better than the SPWM technique for higher order harmonics elimination.

References
1. Booma, N., and Nagisetty Sridhar. "Nine level cascaded H-bridge multilevel DC-link inverter." In Emerging Trends in Electrical and Computer Technology (ICETECT), 2011 International Conference on, pp. 315-320. IEEE, 2011.
2. Lai, Jih-Sheng, and Fang Zheng Peng. "Multilevel converters-a new breed of power converters." In Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS'95., Conference Record of the 1995 IEEE, vol. 3, pp. 2348-2356. IEEE, 1995.
3. Panagis, Panagiotis, Fotis Stergiopoulos, Pantelis Marabeas, and Stefanos Manias. "Comparison of state of the art multilevel inverters." In Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, pp. 4296-4301. IEEE, 2008.
4. Abdalla, I., J. Corda, and L. Zhang. "Multilevel DC- link inverter and control algorithm to overcome the PV partial shading." IEEE Transactions on Power Electronics 28, no. 1 (2013): 14-18.
5. Ramkumar, S., V. Kamaraj, S. Thamizharasan, and S. Jeevanantham. "A new series parallel switched multilevel dc-link inverter topology." International Journal of Electrical Power & Energy Systems 36, no. 1 (2012): 93-99.
6. Rahim, Nasrudin A., and Jeyraj Selvaraj. "Multistring five-level inverter with novel PWM control scheme for PV application." IEEE transactions on industrial electronics 57, no. 6 (2010): 2111-2123.
7. Kouro, Samir, Pablo Lezana, Mauricio Angulo, and Jose Rodriguez. "Multicarrier PWM with DC-link ripple feedforward compensation for multilevel inverters." IEEE Transactions on Power Electronics 23, no. 1 (2008): 52-59.
8. Ahmed, Mahrous, and Essam Hendawi. "A new single-phase asymmetrical cascaded multilevel DC- link inverter." Journal of Power Electronics 16, no. 4 (2016): 1504-1512.
9. Rodriguez, Jose, Jih-Sheng Lai, and Fang Zheng Peng. "Multilevel inverters: a survey of topologies, controls, and applications." IEEE Transactions on industrial electronics 49, no. 4 (2002): 724-738.
10. Du, Zhong, Leon M. Tolbert, Burak Ozpineci, and John N. Chiasson. "Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter." IEEE Transactions on Power Electronics 24, no. 1 (2009): 25-33.
11. Kanimozhi, M., and R. Ramaprabh. "Design of 500W standalone photovoltaic system with reduced switch count multilevel inverter." In Trends in Industrial Measurement and Automation (TIMA), 2017, pp. 1-7. IEEE, 2017.
12. Kahwa, Almachius, Hidemine Obara, and Yasutaka Fujimoto. "Design of 5-level reduced switches count H-bridge multilevel inverter." In Advanced Motion Control (AMC), 2018 IEEE 15th International Workshop on,
13. Shankar, J. Gowri, J. Belwin Edward, K. Sathish Kumar, and I. Jacob Raglend. "A 31-level asymmetrical cascaded multilevel inverter with DC-DC flyback converter for photovoltaic system." In High Voltage Engineering and Power Systems (ICHVEPS), 2017 International Conference on, pp. 277-282. IEEE, 2017.
14. Shankar, J. Gowri, and J. Belwin Edward. "Design and Implementation of 15-Level Asymmetric Cascaded H Bridge Multilevel Inverter." Journal of Electrical Engineering 17, no. 2 (2017).
15. Lakwal, Jaydeep, and Manisha Dubey. "Modeling and simulation of a novel multilevel inverter for PV systems using unequal DC sources." In Advanced Communication Control and Computing Technologies (ICACCT), 2014 International Conference on, pp. 296-300. IEEE, 2014.
16. Najafi, Ehsan, and Abdul Halim Mohamed Yatim. "Design and implementation of a new multilevel inverter topology." IEEE transactions on industrial electronics 59, no. 11 (2012): 4148-4154.
17. Najafi, E., A. H. M. Yatim, and A. S. Samosir. "A new topology-Reversing Voltage (RV)-for multi level inverters." In Power and Energy Conference, 2008. PECCon 2008. IEEE 2nd International, pp. 604-608. IEEE, 2008.
18. Su, Gui-Jia. "Multilevel DC-link inverter." IEEE Transactions on Industry Applications 41, no. 3 (2005): 848-854.
19. Shah, Vraj S., and Urvi T. Jariwala. "Development of Multilevel Inverter Topology with Reduced Device Count Using Smart Control Technique." In 2018 Second International Conference on Electronics, Communication and Aerospace Technology (ICECA), pp. 690-696. IEEE, 2018.
20. Jammala, Venkataramanaiah, Suresh Yellasiri, and Anup Kumar Panda. "Development of a New Hybrid Multilevel Inverter Using Modified Carrier SPWM Switching Strategy." IEEE Transactions on Power Electronics (2018).
21. Armi, Faouzi, Lazhar Manai, and Mongi Besbes. "Newton Raphson algorithm for selective harmonic elimination in asymmetrical CHB multilevel inverter using FPGA." In Proceedings of Engineering & Technology (PET), pp. 887-894. 2016.
22. Sanka, Sreelakshmi, and M. S. Sujatha. "Recent progress on multilevel inverters and its applications." In AIP Conference Proceedings, vol. 2039, no. 1, p. 020016. 2018.