DISPATCH: Design Space Exploration of Cyber-Physical Systems

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Abstract—Design of cyber-physical systems (CPSs) is a challenging task that involves searching over a large search space of various CPS configurations and possible values of components composing the system. Hence, there is a need for sample-efficient CPS design space exploration to select the system architecture and component values that meet the target system requirements. We address this challenge by formulating CPS design as a multi-objective optimization problem and propose DISPATCH, a two-step methodology for sample-efficient search over the design space. First, we use a genetic algorithm to search over discrete choices of system component values for architecture search and component selection or only component selection and terminate the algorithm even before meeting the system requirements, thus yielding a coarse design. In the second step, we use an inverse design to search over a continuous space to fine-tune the component values and meet the diverse set of system requirements. We use a neural network as a surrogate function for the inverse design of the system. The neural network, converted into a mixed-integer linear program, is used for active learning to sample component values efficiently in a continuous search space. We illustrate the efficacy of DISPATCH on electrical circuit benchmarks: two-stage and three-stage transimpedance amplifiers. Simulation results show that the proposed methodology improves sample efficiency by 5-14× compared to a prior synthesis method that relies on reinforcement learning. It also synthesizes circuits with the best performance (highest bandwidth/lowest area) compared to designs synthesized using reinforcement learning, Bayesian optimization, or humans.

Index Terms—Active learning; cyber-physical system synthesis; evolutionary algorithm; mixed-integer linear program; multi-objective optimization; neural networks; sample efficiency.

1 INTRODUCTION

Cyber-physical systems (CPSs) form the foundation of various applications that include healthcare, smart grid, transportation, and smart home [1], [2]. These systems consist of many interacting digital, analog, physical, and human components designed to perform specific functions through integrated physics and logic. CPS designs can be quite complex especially when they involve multidisciplinary analysis like optimizing the operating cost and range of an aircraft. For instance, conceptual designs account for around 80% of the development cost in aircraft manufacturing [3]. Hence, it is important to develop search techniques that minimize the number of costly CPS simulations and efficiently sample the design search space [4].

CPS design entails finding both the system architecture as well as the appropriate component values with the goal of obtaining a final design that meets predefined system specifications. For example, a drone can have multiple architectures (quadcopter, pentacopter, hexacopter) and each architecture requires selecting geometry, motor position, and orientation [5]. Classical techniques for CPS design rely on humans for architecture selection [6]. The architecture is simulated over a range of component values to select the combination that meets the system requirements. Such a CPS design process limits the search space and costly CPS simulations increase development time.

The development of more efficient design space exploration techniques must rely on a combination of novel automated search techniques with the flexibility of incorporating existing knowledge from architectures designed by humans. CPS design can be formulated as a multi-objective optimization (MOO) problem to capture different system design objectives constrained by the components available for synthesis. For instance, when designing a drone, the constraints arise from the maximum torque the motor can produce with the objective of maximizing the payload and the distance the drone can travel.

To address the CPS design problem, we propose DISPATCH, a two-step design methodology that solves the problem in a sample-efficient manner. The first step of DISPATCH either explores architectures as well as component values or only component values for a fixed architecture. We use a genetic algorithm (GA) to harness its benefits for exploration in a discrete design space and for the ease of encoding architectures with it. We terminate the GA even before meeting the design requirements since GA is sample-inefficient and requires a large number of iterations to meet the requirements. We thus obtain a coarse design in the first step.

In the second step, we fine-tune the coarse design to search for component values in a continuous search space. This step uses a neural network (NN) as a surrogate function to model system response. We convert the NN into a mixed-integer linear program (MILP) to incorporate the constraints imposed by the inputs (i.e., component values), outputs (i.e., desired response), and the NN. We use this formulation to obtain an inverse design of the system to find the component values that satisfy a set of system constraints. A feasible solution of the MILP yields the component values that are used to simulate the system. Otherwise, we simulate the system with a random combination of permissible component values. The
NN thus enables active learning through generation of input samples until the system requirements are satisfied or the sampling budget is exhausted. The MILP solution to the NN acts like an acquisition function.

We summarize the major contributions of this article as follows:

- We formulate CPS design as an MOO problem and propose DISPATCH, a two-step method for sample-efficient CPS synthesis.
- In the first step of DISPATCH, we explore a large discrete search space using GA and synthesize a coarse design.
- In the second step of DISPATCH, we explore a continuous search space of component values using an NN as a surrogate function. We use an MILP formulation of the NN to obtain an inverse design of the system.
- We demonstrate that DISPATCH requires much fewer simulations to synthesize valid designs compared to methodologies that are based on reinforcement learning (RL), Bayesian optimization, or human design.

The rest of the article is organized as follows. In Section 2, we discuss related work. Section 3 provides the necessary background, followed by a simple motivational example in Section 4. In Section 5, we introduce the methodology for sample-efficient CPS design. We apply the methodology to the synthesis of electrical circuits in Section 6. Finally, Section 7 concludes the article.

2 RELATED WORK

In this section, we review past work on solving MOO problems and automated system synthesis. For the latter, we review existing design techniques for analog circuits that we use later as benchmarks to validate our methodology. Like CPS, the design of analog circuits requires searching over a large space of possible architectures and component values with the goal of optimizing specific circuit objectives.

2.1 Search techniques

CPS design often has multiple objectives that need to be optimized based on system requirements [7]. GA, a type of evolutionary algorithm (EA), is known to be suitable for addressing MOO problems [8]. A seminal work in this field is the NSGA-II algorithm [9] that uses a fast non-dominated sorting approach to reduce computational complexity by an order of magnitude. EAs have several variants, e.g., differential evolution that perturbs randomly selected population members based on the difference between selected individuals [10], swarm intelligence that includes ant colony optimization [11], and particle swarm optimization [12]. Genetic programming [13] is another evolutionary approach that evolves computer programs represented as tree structures. Though EAs are good at exploration, lack of gradient information during search makes them sample-inefficient.

Gradient-based search, such as RL, can address the sample-inefficiency problem of EAs [14] at the cost of poorer exploration. RL is used for system design by learning a policy to obtain component values based on the current system state [15], [16]. The recent spurt in interest involving the use of RL combined with deep learning is due to [17]. This approach is based on training a convolutional NN to learn a policy for playing Atari games. This work was extended to the continuous action space in [18] to solve simulated physics tasks and learn end-to-end policies that are more sample-efficient than those discussed in [17].

2.2 System synthesis

EA was widely used in the 1990’s and early 2000’s for synthesis of electrical circuits [8]. The use of EA to obtain the topology of analog circuits was pioneered in [19]. Parallel GA and circuit-construction primitives were used to create circuit graphs to evolve designs for an analog filter and amplifier in [20]. Similarly, EA and simulated annealing were combined for analog circuit synthesis in [21]. In [22], surrogate modeling with EA was proposed to synthesize a low-noise amplifier. Synthesis of amplifiers and filters was done by solving constrained MOO with NSGA-II in [23].

More recent works have primarily focused on determining component values for a fixed architecture in a sample-efficient manner. The method proposed in [14] uses deep deterministic policy gradient (DDPG), a form of RL, for sample-efficient synthesis of two-stage and three-stage transimpedance amplifiers, for this purpose. The method in [24] proposes deep RL combined with transfer learning over a sparse design space to synthesize analog circuits. The method in [25] uses Bayesian optimization with an ensemble of acquisition functions to tackle complex mathematical functions and synthesize electrical circuits.

The drawbacks of existing search techniques can be summarized as follows:

- GA is sample-inefficient and often needs to repeat costly simulations multiple times to obtain an acceptable design.
- The CPS design problem is formulated as a weighted sum of multiple objectives. In the optimization process, the weights are determined using domain expertise or through multiple simulations, making the design procedure inefficient.
- Most CPS design formulations assume that the architecture is fixed and only focus on selecting component values, thereby limiting the search space and possibly missing out on novel designs.
- Bayesian optimization based design techniques require a large amount of time to select the next sampling point for simulation [14], thereby making the optimization process very slow.

3 BACKGROUND

Fast CPS synthesis warrants exploration in a sample-efficient manner. To this end, we formulate CPS design as an MOO problem and propose DISPATCH, a two-step CPS design methodology based on GA and inverse design. Next, we provide background on MOO formulation of CPS design problems, GA, and inverse design.

3.1 CPS design through multi-objective optimization

When designing CPS, the designer is interested in achieving multiple system objectives under various constraints. This
can be done by formulating CPS design as an MOO problem. The solutions to the MOO problem indicate a set of choices that enable the best tradeoffs among competing objectives. These solutions constitute a non-dominated set and lie on a surface called the Pareto front [26]. When some decision variables can only take integer values, and the constraints and objectives are linear, the problem can be formulated as an MILP. Many CPS designs fall into this category. For instance, in the design of multicopters, the number of motors is an integer and the constraint on the torque produced by the motor is linear [5]. The multicopter design objective may be to maximize the payload and distance it can travel. More formally, the problem of CPS design can be formulated as follows:

\[
\begin{align*}
\text{minimize} & \quad f_m(x, y), \quad m = 1, 2, \ldots, M \\
\text{subject to} & \quad g_j(x, y) \geq 0, \quad j = 1, 2, \ldots, J \\
& \quad h_k(x, y) = 0, \quad k = 1, 2, \ldots, K \\
& \quad x_i^L \leq x_i \leq x_i^U, \quad i = 1, 2, \ldots, n
\end{align*}
\]

where \( y \) represents the search space over all possible architectures, \( x \) is the search space over all possible component values, and \( f_m(x, y) \) is the \( m \)th objective. The system must also satisfy \( J \) inequality constraints given by \( g_j(x, y) \) and \( K \) equality constraints given by \( h_k(x, y) \). As an example, for electrical circuits, the constraints may be on the maximum power the system can consume or the minimum bandwidth that it must achieve. The lower bound for the value \( x_i \) of component \( i \) is \( x_i^L \) and the upper bound is \( x_i^U \). Next, we introduce GA and NN-based inverse system design.

### 3.2 Genetic algorithm

CPS designs often rely on human expertise. However, this may lead to failure to find an architecture that meets all system requirements or require long simulation runs to explore the large design space. In the first step of DISPATCH, we harness GA’s exploration capability and ease of encoding an architecture [27] to solve the MOO formulation of CPS design. GA evolves a population of individual solutions through multiple generations. The main steps of GA are as follows:

1. Each individual in the first generation of a population is represented with a chromosome. A chromosome is a sequence of genes.
2. Each individual is evaluated on the basis of how well it meets its multiple objectives.
3. A subset of these individuals is selected to produce children for the next generation.
4. Pairs of randomly chosen individuals (parents) from this subset undergo reproduction using crossover by combining the genes of the parents to create children.
5. The genes of each child are mutated by perturbing them with low probability to facilitate exploration across its various dimensions.
6. The best performing individuals in the current generation and the children (after step 5) are retained.
7. Steps 2-6 are repeated until one of the stopping criteria is met.

In our case, we use GA to evolve CPS architectures. A chromosome corresponds to an architecture. Genes encode details of a particular component, like its type, connecting nodes, and value. We evaluate the architecture through a CPS simulator. We use tournament selection to select the individuals that undergo reproduction [28]. Fig. 1 shows a population of individuals, i.e., chromosomes, and genes. Here, the system architecture corresponds to an electrical circuit. GA requires a large number of simulations to obtain a design that meets all specifications, thereby pointing to the need for a sample-efficient design procedure.

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**Fig. 1.** Details of different elements of GA. Each component is color-coded (resistor in blue and capacitor in grey). Gene depicted in a red box, chromosome in a green box, and population in a blue box.

### 3.3 Inverse system design using NN

We overcome the sample inefficiency of GA by terminating it at an intermediate stage (before necessarily reaching a valid or acceptable design) and then using a sample-efficient gradient-based search to meet system requirements for a fixed architecture. Akintunde et al. [29] proposed an MILP formulation of an NN in the context of neural agent-environment systems to solve the reachability problem for an NN-based policy trained using RL. Reachability indicates whether the NN can output the desired values using permissible inputs. An NN is converted into an MILP by representing all hidden neurons with constraints defined as follows:

\[
C_i = \begin{cases} 
\bar{x}_j^{(i)} \geq W_j^{(i)} \bar{x}^{(i-1)} + b_j^{(i)}, \\
\bar{x}_j^{(i)} \leq W_j^{(i)} \bar{x}^{(i-1)} + b_j^{(i)} + Q \bar{\delta}_j^{(i)}, \\
\bar{x}_j^{(i)} \geq 0, \bar{x}_j^{(i)} \leq Q \left(1 - \bar{\delta}_j^{(i)}\right) \text{, } j = 1, \ldots, L^{(i)}.
\end{cases}
\]

In Eq. (2), \( \forall i, j, \bar{x}_j^{(i)} \) corresponds to the \( j \)th neuron in the \( i \)th layer, \( L^{(i)} \) is the number of neurons in the \( i \)th layer, \( W_j^{(i)} \) represents weights that determine the input to \( \bar{x}_j^{(i)} \), \( \bar{x}^{(i-1)} \) represents outputs from the \((i-1)\)th layer, \( b_j^{(i)} \) is the bias for neuron \( \bar{x}_j^{(i)} \), \( Q \) is larger than the largest possible magnitude of \( W_j^{(i)} \bar{x}^{(i-1)} + b_j^{(i)} \), and \( \bar{\delta}_j^{(i)} \) is defined as follows:

\[
\bar{\delta}_j^{(i)} \triangleq \begin{cases} 
0 \text{ if } \bar{x}_j^{(i)} > 0 \\
1 \text{ otherwise}
\end{cases}
\]
The constraints imposed by the hidden neurons of the network are obtained from the union of all the constraints \( (C_i) \) shown in Eq. (2).

This formulation is used in a system called CNMA\(^1\) [30] to obtain the input sample points while designing a system. If the solution to the MILP problem is feasible, the input that satisfies the constraints is used as the next sample point to simulate the CPS, otherwise the CPS is simulated using a random sample. The NN is trained to predict the output corresponding to the inputs by minimizing the mean-squared error for all the simulated points.

Next, we illustrate the design of a simple electrical circuit as a motivational example to show how DISPATCH deals with architecture and component selection, which are generic CPS design problems.

4 Motivation

We propose DISPATCH as a solution to the CPS design problem. Next, we illustrate its working through the design of a low-pass filter. The objective is to obtain a unity gain (0 dB) and a bandwidth of 1 kHz while minimizing the number of circuit components. The following discrete components are available:

- **Resistors:** [1, 10, 600, 1200] Ω
- **Capacitance:** [1e-12, 119.37e-9, 155.12e-9, 1e-5] F
- **Inductance:** [1e-6, 15.24e-3, 61.86e-3, 1e-2] H

The seed design is a Butterworth low-pass filter adapted from [31] and shown in Fig. 2. We evolve it through GA till the point it gets close to meeting the specifications. We use a maximum of five nodes and 10 components in the circuit architecture to expand the search space even though it is known that a low-pass filter can be synthesized within these ranges of component values. The next step is to fine-tune the component values in a continuous search space thus yielding a standard low-pass filter. The next step is to simulate the CPS, otherwise the CPS is simulated using a random sample. The NN is trained to predict the output of a first-order low-pass filter and the observed response. The weights are the same as above.

3) Number of active components: a lower value implies fewer components.

![Fig. 2. Low pass Butterworth filter architecture and component values used as seed design.](image)

Fig. 3 shows the chromosome representation of a circuit. A gene encodes the details of a component, including its type, connecting nodes, and value (shown in the top row). The bottom row shows whether the component is active (1) or inactive (0) [8]. We define the following objectives to find the coarse design by searching the architecture and component space using GA:

1) Weighted sum of the difference between the desired magnitude response of a first-order low-pass filter and the observed response. We set the weights in the passband to 40 and 1 in the stopband to give more importance to the response in the passband. Note that since GA synthesizes a coarse design, other values may work too. We use weighted sum here to cover the entire frequency range.

2) Weighted sum of the difference between the desired phase response of a first-order low-pass filter and the observed response. The weights are the same as above.

3) Number of active components: a lower value implies fewer components.

![Fig. 3. Chromosome representation of a low-pass filter. The top row represents details of all the 10 components. It shows the component type given by (R, L, C) and its connecting nodes (n1, n2, n3, …) and value. The bottom row indicates whether the component is active (1) or inactive (0) in the circuit.](image)

We use GA for architecture search using 50 individuals comprising the seed design and other randomly generated individuals evolved over 100 generations. Fig. 4 shows the scaled mean (with respect to the seed design) of the three objectives for the entire population from the 10\(^{th}\) generation onwards. We plot the mean objective values after the 10\(^{th}\) generation because the initial GA generations have very high objective values. The x-axis shows the generation number and the y-axis shows the mean value for the three objectives. Since the mean values are scaled, the y-axis has no unit. There is a trade-off among the three objectives across generations, as evident from the figure. After 100 generations, we select a non-dominated individual from the Pareto front based on the first two objectives (magnitude and phase). This individual (circuit) has a bandwidth of 966 Hz, phase of -46 degree, gain of 0 dB, and a total of three components. Since this is a coarse design, it does not meet the requirements yet. Fig. 5 shows the GA-evolved circuit. The circuit synthesized by GA can be simplified using human intervention by replacing the two parallel capacitors with a single equivalent capacitor, thus yielding a standard low-pass filter. The next step is to fine-tune the component values in a continuous search space using a gradient-based search technique.

We perform fine-tuning through an NN with a hidden layer consisting of 100 neurons that is converted into a MILP. The NN inputs are component values (resistor and capacitor) that are either derived from a feasible solution to the MILP or else a random sample if a feasible solution does not exist. The continuous search space is [400, 800]Ω for resistor and [0.01, 1]μF for capacitance. Since this is a simple design, through prior knowledge we know that a low-pass filter can be synthesized within these ranges of component...
Fig. 4. Scaled mean objectives across all individuals in a generation for (a) magnitude, (b) phase, and (c) component values from the 10th generation onwards for architecture search for low-pass filter design.

Fig. 5. Low-pass filter architecture evolved by GA.

Fig. 6. Gain and bandwidth during fine-tuning using gradient-based search.

Fig. 7. Low-pass filter architecture (after human intervention on the GA schematic) at the end of the second step.

values to meet the specifications. The targeted outputs of the NN are gain, bandwidth, and response of the filter at 200, 500, and 2000 Hz. The responses at these frequencies sufficiently capture the behavior of the filter below and above the desired bandwidth. The output constraints are as follows: gain (from input to output) in the range $[-0.92, 0.83]$ dB and bandwidth in the range $[990, 1010]$ Hz. We generate 10 random input samples to initialize the NN for training to minimize the mean-squared error. The solutions suggested by MILP meet the requirements after 20 more simulations. We show these simulations (10 for initialization of the NN and 20 during the MILP step) in Fig. 6: initialization points in the orange part and MILP ones in the blue part. The outcomes during initialization can be seen to be random as they are far from meeting the requirements. However, the points suggested by the MILP have a response closer to the requirements until finally the suggested point meets the specification. The circuit with the values of the components on termination of the second step is shown in Fig. 7.

5 SYNTHESIS METHODOLOGY

In this section, we describe DISPATCH in detail. The first step explores a large search space using GA based on gradient-free search. The outcome of the first step is a coarse design that is fine-tuned through gradient-based, sample-efficient search to obtain better component values.

5.1 Step 1: Coarse design

We show the flow involved in the synthesis of the coarse design in Fig. 8. We evolve individuals across generations using NSGA-II [9] that yields non-dominated solutions of the CPS design that is formulated as an MOO problem. In architecture search, we initialize some individuals in the first GA generation with seed designs from the literature to exploit prior knowledge. When performing only component selection, we initialize the individuals in the first generation with component values to cover the search space. This enables comparisons with other designs from the literature that do not use prior knowledge.

During architecture search, a gene has three constituents: type of component, nodes connecting the component, and the component value, as shown in Fig. 3. In the case of component selection, the gene encodes the value of the component in the chromosome that represents the circuit. We evaluate each circuit represented by a chromosome using HSPICE.

Algorithm 1 describes how architecture search is performed using GA. We generate $P$ individuals in a generation. Some of these are from seed designs ($S$) whereas others are randomly generated. We generate random individuals by selecting a random component, choosing the number of nodes (e.g., a resistor requires two nodes whereas a MOSFET requires three nodes) connected to that component, and the component value. We select the component values for random individuals from quasi-random Sobol samples in the range ($R$) of each component. Sobol samples are distributed uniformly over a unit hypercube [32]. Then we scale the samples to lie within the specified range for each component. We postprocess individuals to ensure that some components are connected to the fixed terminals of
the architecture, e.g., ground, supply voltage, input/output terminals in the case of a circuit, to ensure a valid design. We simulate all individuals in a generation to compute the objective functions. This is followed by ranking using the NSGA-II algorithm [9]. We use tournament selection for selecting some individuals in a generation to undergo reproduction through crossover and mutation to produce \( P \) children. We use NSGA-II again to select \( P \) individuals out of the \( 2P \) individuals for the next generation. This process continues until one of the stopping criteria (stop) is met. These criteria are based on individuals not improving over a fixed number of generations, exhausting the simulation budget or on attaining the required performance. Finally, we select one individual from the final generation based on a CPS performance metric. The metric (lower the better) in our case is one of the multiple CPS objectives. We select an individual from the final generation since ranking using NSGA-II ensures that we never lose an individual from the Pareto front within a generation. We select only one individual since GA only synthesizes a coarse CPS design although it is also possible to select another individual to undergo fine-tuning in the next step.

Component selection for a fixed architecture using GA is done using a setup similar to Algorithm 1. Instead of initializing some individuals in the first generation by seed designs, we initialize all the individuals using Sobol samples. The rest of the procedure remains the same.

### 5.2 Step 2: Fine-tuning

At the end of Step 1, we have a coarse CPS design. When using Step 1 for architecture search, we use human intervention to refine the synthesized design if needed. We fine-tune this design through a modified version of CNMA [30] by searching in a continuous space. In contrast to CNMA where the selection is stopped when the simulation budget is exhausted, we adaptively replace the design from Step 1 if a successful design is not found within a fixed number of simulations. We model the response of the system to the inputs using an NN. The NN converted to MILP acts as an acquisition function and determines the sample point for CPS simulation. We train the NN to minimize the mean-squared error of the CPS response to the inputs. Fig. 9 shows the high-level overview of this step through an example. The designer specifies the system requirements shown on the right in green. The feasible solution of the MILP determines the potential component values shown on the left in blue that achieve the desired response.

**Algorithm 1** Step 1: Architecture synthesis using GA

**Input:** \( S \): Seed design(s); \( N \): #generations; \( P \): population size; \( C \): Components; \( R \): Component range; \( node \): Nodes; \( max\_comp \): Max # components; \( stop \): Stopping criteria

- Generate Sobol samples for \( C \) within \( R \)
- Initialize individuals with \( S \) and others randomly

**while** not \( stop \) **do**
- Compute objectives for all \( P \)
- Rank \( P \) using NSGA-II
- Use tournament selection to create mating population of size \( P \)
- Use reproduction based on crossover and mutation to create \( P \) children
- Select \( P \) from \( 2P \) members using NSGA-II

**end while**

**Output:** Best individual from the final generation using a metric.

Fig. 8. Evolution using GA.

Fig. 9. Overview of gradient-based search through an example.
Step 1 yields. In the flowchart, \( N \) denotes the number of simulations in a particular trial out of a total of \( T \) trials. We effectively repeat the fine-tuning step \( T \) times, allowing a maximum of \( N \) simulations in a trial. We obtain Sobol samples from the range of each component in the design from Step 1, followed by simulation of these points to determine the output. The samples are generated around the nominal values of each component (e.g., \( \pm 70\% \) of \( 10 \Omega \) for resistor). The samples are clipped to ensure that the values of the components are within the permissible range for each type of component. We train an NN with these input-output pairs that are range-normalized to \([0, 1]\). We convert the NN into an MILP using Eq. (2) to see if there is a feasible solution. The range of available components determines the constraints on the input whereas system requirements determine the output constraints. We use Gurobi [33] to find a feasible solution. If such a solution exists, it indicates that the desired output is reachable by the NN from this input. This corresponds to a feasible solution. We simulate the system with the suggested input. The simulation terminates if the system requirements are met. Otherwise, we use the input-output pair to train the NN further. The procedure continues until a maximum number of permissible simulations (\( N \)) is exhausted. After finishing a trial, the input corresponding to the least absolute fractional deviation of the output from the requirement replaces the design from Step 1. Fractional deviation is computed as follows:

\[
\sum_i \frac{|obsi - spec_i|}{spec_i} I\{obsi \leq spec_i\}, \tag{4}
\]

where \( spec_i \) is the specification for the \( i^{th} \) objective or constraint, \( obs_i \) is the observed response of the CPS for the \( i^{th} \) objective or constraint. We use the inputs that yield the minimum fractional deviation over the sum of all the objectives in a trial. \( I\{obsi \leq spec_i\} \) is an indicator function that takes the value 1 in the case of violation of \( spec_i \) determined by \( obs_i \) (can be greater or less than) and 0 otherwise. We retain the feasible solutions obtained from the MILP formulation to further train the NN in subsequent trials. After the last trial, we return the input that corresponds to the output that satisfies all the hard constraints (like maximum power consumption for a valid design) and comes closest to satisfying the target objective of the system. This indicates a failure as the system does not meet the requirements exactly.

6 Experimental Results

In this section, we evaluate how DISPATCH performs architecture search and component selection. We first show the architecture search and component selection results for a two-stage transimpedance amplifier and then the component search results for both two-stage and three-stage transimpedance amplifiers. We compare our results with those in [14] that are synthesized by humans, RL, and Bayesian optimization. The technology files specifying the device physics for simulation are from [34] and are the same as in [14]. We implement DISPATCH using Keras [35], scikit-learn [36], Gurobi [33], and PyGMO [37]. The simulations are performed on an Intel Xeon processor with 128 GB of DRAM.

6.1 Architecture search and component selection

We use the standard design of a two-stage transimpedance amplifier presented in [14] as the seed design for our methodology in order to take advantage of prior human knowledge and make improvements in all the metrics. Fig. 11 shows this seed design. The objective is to maximize the bandwidth of the amplifier while minimizing the sum of gate areas of all the MOSFETs in the circuit and satisfying hard constraints on noise, gain, peaking, and power. The search space comprises three components: two types of MOSFETs (PMOS transistor, NMOS transistor) and resistor. In the human-designed circuit, the MOSFETs are of minimum length (0.18 \( \mu \)m), based on the technology used, whereas the width is variable. Our search also uses minimum-length MOSFETs and only selects their width. We discretize the search space during architecture search (Step 1) by generating 100 Sobol samples for resistors in the \([50, 5k]\) \( \Omega \) range and width in the \([0.18, 80]\) \( \mu \)m range. In the human-designed circuit, the resistor values are 420 \( \Omega \) and 3 \( k\)\( \Omega \), and the width is in the \([0.9, 51]\) \( \mu \)m range. During evolution, we allow the circuit to have a maximum of 11 nodes and a total of 10 components, whereas the seed design has six nodes and eight components, to enable search for novel designs. Since we need 10 components for a chromosome, we initialize two additional genes as resistors with a small resistance of 2.2 \( \mu \)\( \Omega \) whose terminals are shorted and not connected to any of the nodes in the seed design. This ensures the response of the seed design remains unaffected.

We use GA to evolve a generation of 100 individuals and set the maximum number of generations to 200. We choose these numbers to achieve at least about 50% sample efficiency (i.e., 50% fewer simulations) compared to the design methodology in [14]. We simultaneously search for the architecture and the component values whereas the method in [14] only searches for component values. Hence, our method searches through a much larger design space, albeit with the seed design. We formulate an MOO problem with three objectives: bandwidth, noise, and power. The objectives are described next.

1) Bandwidth: This objective corresponds to the weighted sum of the absolute difference between the desired and observed responses, with a passband weight of 40 and a stopband weight of 1, as shown in Fig. 12 with weights \( \{w_i\} \) in each region in text.
A reward/penalty is applied to this objective as follows.

- Assessing the level of reward/penalty is based on the operating region of the MOSFET: reward for MOSFET operating in the saturation region, else a penalty, as follows:
  - **Saturation region**: Reward of 1 divided by the number of MOSFETs.
  - **Linear region**: Penalty of 2 divided by the number of MOSFETs.
  - **Cutoff region**: Penalty of 3 divided by the number of MOSFETs.

The penalty encourages MOSFET operation in the saturation region.

- A penalty of 15 is assessed based on the fractional deviation in gain below 58.1 dB (since 58.1 dB is the gain achieved by RL based synthesis in [14]).
- A penalty of 15 is assessed based on the fractional deviation in peaking above 0.963 (achieved by RL in [14]).
- A penalty of 15 is assessed based on the fractional deviation in bandwidth below 5.81 GHz (this is slightly higher than the bandwidth achieved by RL in [14]: 5.78 GHz).

We scale the bandwidth objective by dividing it by the objective of the seed design.

2) **Noise**: This objective corresponds to the ratio of measured noise and the noise achieved by the RL-based design in [14] (19.2 pA/√Hz). An additional penalty of 15 is assessed based on the fractional deviation in noise above this value.

3) **Power**: This objective corresponds to the ratio of measured power and the power achieved by the RL-based design in [14] (3.18 mW). No penalty is assessed in this case due to the large room for optimization available for power consumption.

The objective for noise is given by,

$$\frac{N_m}{N_{ref}} + \alpha \frac{N_m - N_{ref}}{N_{ref}} I_{\{N_m > N_{ref}\}},$$

where $N_{ref}$ is the noise of RL-designed circuit, $N_m$ is the measured noise, $\alpha$ is the penalty factor (15 in our case) and $I_{\{N_m > N_{ref}\}}$ is the indicator function that takes a value of 1 if $N_m > N_{ref}$ and 0 otherwise. The second term is a penalty applied only when the measured noise ($N_m$) is worse than $N_{ref}$. The total penalty scales linearly with deviation from $N_{ref}$. Other objectives are defined analogously.

We club together all the sub-objectives related to bandwidth (gain, desired bandwidth, peaking) into one to minimize the number of objectives that need to be tackled while capturing the entire frequency response. The penalty terms encourage the target response to be better than the response of the designs in [14]. We do not tune the penalty to the circuit since the aim of Step 1 is to synthesize a coarse design. In case the simulation is unsuccessful for a circuit that does not meet the objectives, we set the objective values to a very large number to indicate this fact.

We use a tournament size of 10, mutation rate of 0.1, and crossover probability of 0.9 that are typical values for GA. The evolution stops under any of the following circumstances:

- The scaled bandwidth objective falls below 0.9 since the aim is to improve it by about 10% relative to that of the seed design.
- The number of generations exceeds 100 and the bandwidth objective stays the same for more than 100 generations, indicating saturation in GA performance.
- The maximum number of generations (200) is reached.

Fig. 13 shows the evolution of objective values across GA generations. It depicts the mean values of all the objectives i.e., (a) bandwidth, (b) power, and (c) noise, across all individuals in a generation after the second generation, shown in blue. As the $y$-axis shows scaled objectives, it has no units. We plot from second generation onwards due to the high objective values in the first generation. There is a trade-off among the three objectives. The dotted-orange curve shows the individual with the best objective for bandwidth in each generation and the corresponding objectives for power and noise in Fig. 13(b) and Fig. 13(c), respectively. In the first seven generations, the seed design with a scaled bandwidth objective of 1 is the lowest among all the designs generated by GA. In the eighth generation, a design is evolved with a lower objective value for bandwidth compared to the seed design. The simulation stops at this point as the bandwidth objective is below 0.9, thereby meeting the stopping criteria.

We choose the circuit with the best objective for bandwidth as the coarse design in Step 1 since this circuit addresses several sub-objectives. We fine-tune the coarse design to meet the specifications in the next step. We remove dangling nodes through human intervention as they are redundant. We also remove a MOSFET operating in the cutoff region as it does not contribute to gain. Fig. 14 shows the circuit before and after human intervention. Table 1 shows the values of objectives and constraints before and after human intervention. GA requires less than an hour for synthesis. After human intervention, the circuit does not meet the hard constraint for peaking. This can be remedied in Step 2 through fine-tuning. The seed design has six MOSFETs. This one uses only four MOSFETs.

The next step is selecting the component values to meet the specifications. In addition, our goal is to have the synthesized circuit dominate all the designs in [14]. In Step 2, we specify the range of each component in the circuit.
We increase it to 500 for each subsequent trial. The intuition behind the choice is that the NN learns a better system representation over time and is, hence, permitted to make more guesses in subsequent trials. We derive 100 Sobol samples based on the circuit synthesized in Step 1 to train the NN in the first trial. For subsequent trials, we only use one Sobol sample based on the design selected in the previous trial. We use the remaining feasible points from previous iterations to train the NN before formulating the MILP in Step 2. The NN has three hidden layers with 40, 20, and 8 neurons, respectively. We generate training data over time, thereby making it robust to the choice of the NN as long as the NN can model sufficient complexity. We use MLP Regressor from the Scikit-learn [36] package along with the Adam optimizer [38], an initial learning rate of 0.0001, adaptive learning, and a maximum iteration count of 100000 to train the NN. Other parameters are set to their default values. We run Step 2 for a maximum of 144 hours or 20 trials whichever occurs first. Unless specified, the same setup is used for all the experiments.

TABLE 1
Comparison of the GA-synthesized circuit with the human-designed circuit for architecture search for the two-stage transimpedance amplifier. Hard constraint violations are shown in a circle.

| Spec.             | #Samples | Time       | Noise (µA/√(Hz)) | Gain (dB) | Peaking (dB) | Power (mW) | Gate area (µm²) | Bandwidth (GHz) |
|-------------------|----------|------------|------------------|-----------|--------------|------------|-----------------|-----------------|
| GA                | 1,600    | 0.15 hr    | 18.0             | 58.0      | 0.915        | 7.97       | 35.59           | 5.93            |
| Human Design [14] | 1,289,618 months | 18.6 | 57.7 | 0.927 | 8.11 | 25.11 | 5.95 |
| GA+Human          | -        | -          | 17.9             | 58.0      |              |            |                 |                 |

Fig. 13. Scaled objectives across generation for (a) bandwidth, (b) power, and (c) noise from the second generation onwards for architecture synthesis of the two-stage transimpedence amplifier. The solid blue line shows the mean objectives averaged across all individuals in a generation and the dotted-orange line shows the individual with the best objective for (a) bandwidth and the corresponding (Corr.) objectives for (b) power, and (c) noise.

Table 2 shows a comparison of designs synthesized using our methodology with designs obtained by humans, DDPG, and Bayesian optimization [14]. The last row depicts a design that satisfies all the hard constraints while maximizing bandwidth. We save simulation results at the end of every trial. The time column includes the time required for Step 1 and the time elapsed until the last saved trial. The number of samples simulated is cumulative over the two steps (GA and fine-tuning). For the designs from [14], the number of samples only accounts for component selection. DISPATCH synthesizes designs that are better at meeting the objectives across the board relative to the weighted sum approach taken in [14]. We also obtain a valid design with the highest bandwidth compared to all the designs in [14]. This bandwidth corresponds to the design that meets all the hard constraints and has the highest bandwidth among all the simulations performed. There is a also a significant reduction in synthesis time: ours in CPU hours and for the designs from [14] in GPU hours. We set the required area to be less than 0.85× of the human design when dominating the human design, less than 0.75× of the human design when dominating the DDPG design, less than 0.85× of the human design when dominating the Bayesian optimization based design, and less than 0.9× of the human design when maximizing bandwidth. The correct area is not available for all the designs in [14]. Hence, we use the human-designed circuit as a reference for area computation.

Fig. 14 shows the simulation results for Step 2 during circuit synthesis with the aim of dominating the human design in all metrics. We show the values predicted by the NN in dotted-red, the result of applying that input and simulating it on the system in solid blue, and the requirement depicted by a black line (also shown in text). As the NN learns a better system representation with the help of more

2 Gate area is shown only for designs for which this information is available. There was a problem in area calculation in [14] that was confirmed after contacting the authors.
training instances, the deviation of the value predicted by the NN from the actual simulation result reduces. A dominating circuit design is obtained in only 311 more simulations (in addition to the 1600 simulations required in Step 1) within 2 CPU hours. Fig. 16 shows the simulation results for Step 2 during circuit synthesis to maximize bandwidth while meeting all the hard design constraints. While maximizing the bandwidth, we encourage the method to perform better by increasing the bandwidth requirement that needs to be met by 0.5% starting from 6 GHz.

6.2 Component selection

Next, we evaluate DISPATCH when the architecture is fixed and component values need to be selected. We illustrate it with the architecture for two-stage and three-stage transimpedance amplifier architectures presented in [14].

6.2.1 Two-stage transimpedance amplifier

We use DISPATCH to determine the width of all the MOSFETs and the resistors with the goal of minimizing the objectives defined in Section 6.1. We discretize the search space during GA-based component selection in Step 1 by generating 250 Sobol samples for resistors in the [100, 5k] Ω range and width in the [0.2, 50] µm range. These value ranges include those for the human-designed circuit. Table 3 shows a chromosome for this case where \( W_i \) corresponds to the width of MOSFET \( T_i \), and \( R_F \) and \( R_b \) are the values of the resistors in Fig. 11.

**TABLE 3**

| #Samples | Time | Noise (pA/√Hz) | Gain (dB) | Peaking (dB) | Power (mW) | Gate area (µm²) | Bandwidth (GHz) |
|----------|------|----------------|-----------|--------------|------------|-----------------|-----------------|
| Human Design [14] | 1,289,618 | months | 18.6 | 57.7 | 0.992 | 8.11 | 23.11 | 5.95 |
| Human Design (DISPATCH) | 1,291 | 1.2 hrs | 18.4 | 57.7 | 0.878 | 5.77 | 17.91 | 6.00 |
| DDPG [14] | 50,000 | 30 hrs | 19.2 | 58.1 | 0.963 | 3.18 | - | 5.78 |
| DDPG (DISPATCH) | 2,291 | 4.7 hrs | 19.2 | 58.1 | 0.953 | 3.16 | 11.81 | 5.80 |
| Bayesian Opt. [14] | 380 | 30 hrs | 58.6 | 0.629 | 4.24 | 5.10 |
| Bayesian Opt. (DISPATCH) | 1,751 | 0.5 hr | 58.8 | 0.260 | 3.84 | 15.25 | 3.50 |
| Max. Bandwidth (DISPATCH) | 4,176 | 106.3 hrs | 19.2 | 57.6 | 0.984 | 5.85 | 20.13 | 6.18 |

We evolve a generation of 30 individuals for a maximum of 400 generations. We use a smaller population size than in architecture search because the problem is simpler due to a smaller search space. We use a tournament size of 10, mutation rate of 0.1, and crossover probability of 0.9: same as in architecture search. The stopping criteria are:

- The scaled bandwidth with respect to the human design falls below 1.
- The number of generations exceeds 100 and bandwidth stays the same for more than 100 generations, indicating saturation.
- The maximum number of generations, i.e., 400, is reached.

Fig. 17 shows the evolution of objective values across GA generations. The first few generations have high objective values as we do not use a seed design in component selection. GA stopped after the 210th generation due to saturation in performance. Other observations are similar to those in Fig. 13. Synthesis required 0.9 CPU hour. Table 4 shows the values of various objectives obtained after architecture synthesis. The bandwidth is inferior to human design although it is better in other metrics. Hence, in Step 2, we fine-tune this design through component selection to improve its performance.

Table 5 shows comparisons of designs synthesized using DISPATCH with baseline designs. We set the required area to be the same as for architecture search. Our methodology performs better across the board relative to the human design with only 8 CPU hours of effort and 7168 simulations. Our design has 0.5% lower bandwidth than the DDPG design, but performs better or same in terms of the other metrics. Our design performs better than Bayesian optimization based design across the board while also satisfying all the constraints (the former does not satisfy the noise constraint). Finally, the last row shows the design that meets all the hard constraints while maximizing bandwidth. Fig. 18 shows the simulation results for maximizing bandwidth while meeting all the hard constraints. The bandwidth requirement is increased by 0.5% starting from 5.96 GHz.

6.2.2 Three-stage transimpedance amplifier

Next, we discuss component selection for the three-stage transimpedance amplifier shown in Fig. 19, which is adapted from [14]. The blue and green dotted boxes contain subcircuits that are mirror images of each other. Hence, we obtain the component values for only one subcircuit and mirror them in the other. We determine the width and length of all the MOSFETs, including the bias transistor T1. There are 19 components in all: width/length of nine MOSFETs and a resistor \( R_b \).

The requirement is to minimize the sum of the gate areas of all the MOSFETs while meeting hard constraints for gain, bandwidth, and power. We discretize the search space during component selection in Step 1 by generating 250 Sobol samples with width in the [2, 30] µm, length in the [1, 2] µm, and resistor in the [50k, 500k] Ω range. The human-synthesized circuit has width in the [2, 44] µm range, length in the [1, 2] µm range, and a resistor of 291 kΩ. We reduce the search space for width by around 30% to encourage Step 1 to obtain designs with a smaller area. We also round the length to the nearest 0.2 units since the technology only permits the length to be an integer multiple of 0.2 µm. We use this rounding in Step 2 as well.
Fig. 15. Step 2 simulation results: Component selection for the GA-synthesized design (architecture+component) with the aim of improving upon the human design. Results shown for iterations with a feasible solution to the MILP formulation.

Fig. 16. Step 2 simulations results: Component selection for the GA-synthesized design (architecture + component) with the aim of maximizing bandwidth while meeting all the hard constraints. The bandwidth requirement is increased gradually by 0.5% on meeting the specified value in a trial.

Fig. 17. Scaled objectives across generation for (a) bandwidth, (b) power, and (c) noise from the second generation onwards for component selection of the two-stage transimpedence amplifier. The solid blue line shows the mean objectives averaged across all individuals in a generation and the dotted-orange line shows the individual with the best objective for (a) bandwidth and the corresponding (Corr.) objectives for (b) power, and (c) noise.

TABLE 4
Comparison of GA-synthesized circuit with the human-designed circuit for component selection for a two-stage transimpedence amplifier.

| Spec          | #Samples | Time   | Noise (pA/√Hz) | Gain (dB Ω) | Peaking (dB) | Power (mW) | Gate area (µm²) | Bandwidth (GHz) |
|---------------|----------|--------|----------------|-------------|--------------|-------------|-----------------|-----------------|
| Human Design  | 1,289,618 months | 18.6   | 19.3           | ≥ 57.6      | 1            | 8.11        | 17.30           | 5.95            |
| GA            | 6,480    | 0.9 hr | 16.9           | 35.4        | 0.801        | 4.61        | 17.30           | 5.35            |

Fig. 18. Step 2 simulations results: Component selection for the GA-synthesized (component only) two-stage transimpedence amplifier with the aim of maximizing the bandwidth while meeting all the hard constraints. The bandwidth requirement is increased gradually by 0.5% on meeting the specified value in a trial.
Comparison of designs synthesized with DISPATCH with those in [14] for the two-stage transimpedence amplifier (hard constraint violation shown in a circle).

| Spec | #Samples | Time | Noise (pA/√Hz) | Gain (dBΩ) | Peaking (dB) | Power (mW) | Gate area (μm²) | Bandwidth (GHz) |
|------|----------|------|----------------|------------|-------------|------------|----------------|----------------|
| Human Design [14] | 1,289,618 | months | 18.4 | 57.8 | 0.943 | 5.4 | 2531 | 5.73 |
| Human Design (DISPATCH) | 7,168 | 7.8 hrs | 18.4 | 57.8 | 0.943 | 5.4 | 2531 | 5.73 |
| Bayesian Optim. (DISPATCH) | 6,661 | 1.4 hrs | 18.0 | 59.2 | 0.536 | 4.18 | 14.00 | 5.51 |
| Max. Bandwidth (DISPATCH) | 8,911 | 82.1 hrs | 19.2 | 57.6 | 0.921 | 5.16 | 19.33 | 6.12 |

3) **Power:** We define this objective as the ratio between measured power and the power consumed by human-designed circuit which is 1.37 mW. We levy a penalty of 15 based on the fractional deviation in power above this value.

Fig. 20 shows the evolution across GA generations. Mean objectives across all individuals in a generation after the fifth generation for bandwidth, power, and area are shown in blue. There is a trade-off among the three objectives. These observations are similar to those in Fig. 17. GA is terminated after 74 generations as the objective for bandwidth is reduced to less than 1. Table 6 shows a comparison of the circuit synthesized using GA with human design. The circuit obtained by GA violates the hard constraints on bandwidth and power and is hence not an acceptable design. The area of this circuit is much higher than the human-designed circuit.

| Spec | #Samples | Time | Bandwidth (MHz) | Gain (dBΩ) | Power (mW) | Gate area (μm²) |
|------|----------|------|----------------|------------|------------|----------------|
| Human Design [14] | 10,000,000 | months | 50 | 20 | 1 | 1000 |
| GA | 2,220 | 0.31 hrs | 50 | 20 | 1 | 1000 |
| DDPG | 50,000 | 30 hrs | 50 | 20 | 1 | 1000 |
| Bayesian Optim. | 6,661 | 1.4 hrs | 50 | 20 | 1 | 1000 |

In the next step, we fine-tune the component values to obtain designs that dominate the benchmark designs from [14] or perform close to it. Besides, we also synthesize a circuit that meets all the hard constraints while minimizing the gate area. Table 7 shows a comparison of designs obtained using DISPATCH with other designs. DISPATCH synthesizes a design that performs close to human design in 129 CPU hours, using 5025 simulations, while meeting all the hard constraints. The circuit consumes 0.05 mW more power compared to the human design but is better in all other metrics. A dominating design compared to DDPG is obtained in 20 CPU hours with about 14× fewer samples. Fig. 21 shows the simulation results for Step 2 during circuit synthesis for this case. The dominating design in comparison to Bayesian optimization based design is attained in less than 1 CPU hour of total simulation time. DISPATCH synthesizes a design that has the least area compared to all other designs with a reduction of about 25% from the best design achieved by DDPG. The initial requirement of area of 80 μm² is gradually reduced by 5% as soon as the requirement is met.

**7 Conclusion**

We formulated CPS design as an MOO problem and proposed DISPATCH, a two-step CPS synthesis methodology.
Fig. 20. Scaled objectives across generation for (a) bandwidth, (b) power, and (c) area from the fifth generation onwards for component selection of the three-stage transimpedance amplifier. The solid blue line shows the mean objectives averaged across all individuals in a generation and the dotted-orange line shows the individual with the best objective for (a) bandwidth and the corresponding (Corr.) objectives for (b) power, and (c) area.

**TABLE 7**
Comparison of designs synthesized using DISPATCH with those synthesized in [14] for the three-stage transimpedance amplifier (hard constraint violations shown in a circle).

|                  | #Samples | Time  | Bandwidth (MHz) | Gain (kΩ) | Power (mW) | Gate area (µm²) |
|------------------|----------|-------|-----------------|-----------|------------|-----------------|
| Spec             | -        | -     | > 90            | > 20      | < 3        | -               |
| Human Design [14]| 10,000,000 months | 90.1 | 20.2 | 1.37 | 211.0 |
| Human Design (DISPATCH) | 5,025 | 128.5 hrs | 91.0 | 20.3 | 1.42 | 174.7 |
| DDPG [14]        | 40,000   | 40 hrs | 92.5 | 20.7 | 2.50 | 90.0 |
| DDPG (DISPATCH) | 2,869    | 19.9 hrs | 93.2 | 25.9 | 2.37 | 88.6 |
| Bayesian Opt. [14]| 1,160    | 40 hrs | 99.4 | 25.7 | 3.00 | 120.5 |
| Min. Area (DISPATCH) | 4,695 | 124.1 hrs | 90.0 | 20.7 | 2.97 | 67.2 |

Fig. 21. Step 2 simulation results: Component selection for the GA-synthesized (component only) three-stage transimpedance amplifier with the aim of improving upon the DDPG design. Results shown for iterations with a feasible solution to the MILP formulation.

for solving it. We used gradient-free search through GA for exploration and an NN to enable sample efficiency by formulating it as an MILP problem to generate samples based on active learning. The methodology provides a flexible framework for discovering efficient architectures and component values or simply the component values for a fixed architecture. Using this framework, we were able to improve the sample efficiency by a factor of $5-14 \times$ compared to the most sample-efficient designs synthesized by DDPG.

As part of future work, we plan to represent CPS as graphs to explore different architectures through manipulation of these graphs and explore other sample-efficient techniques for active learning. We also plan to enhance the efficacy of the methodology by combining it with RL.

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