Radiation Hardness of CCD Vertex Detectors for the ILC

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Results of detailed simulations of the charge transfer inefficiency of a prototype CCD chip are reported. The effect of radiation damage in a particle detector operating at a future accelerator is studied by examining two electron trap levels, 0.17 eV and 0.44 eV below the bottom of the conduction band. Good agreement is found between simulations using the ISE-TCAD DESSIS program and an analytical model for the 0.17 eV level. Optimum operation is predicted to be at about 250 K where the effect of the traps is minimal which is approximately independent of readout frequency. This work has been carried out within the Linear Collider Flavour Identification (LCFI) collaboration in the context of the International Linear Collider (ILC) project.

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Abstract—Results of detailed simulations of the charge transfer inefficiency of a prototype CCD chip are reported. The effect of radiation damage in a particle detector operating at a future accelerator is studied by examining two electron trap levels, 0.17 eV and 0.44 eV below the bottom of the conduction band. Good agreement is found between simulations using the ISE-TCAD DESSIS program and an analytical model for the 0.17 eV level. Optimum operation is predicted to be at about 250 K where the effect of the traps is minimal which is approximately independent of readout frequency. This work has been carried out within the Linear Collider Flavour Identification (LCFI) collaboration in the context of the International Linear Collider (ILC) project.

I. INTRODUCTION

Particle physicists worldwide are working on the design of a high energy collider of electrons and positrons (the International Linear Collider or ILC) which could be operational sometime after 2016. Any experiment exploiting the ILC will require a high performance vertex detector to detect and measure short-lived particles. One candidate for such a device would consist of a set of concentric cylinders of charge-coupled devices (CCDs).

An important requirement of a vertex detector is to remain tolerant to radiation damage for its anticipated lifetime.

CCDs suffer from both surface and bulk radiation damage. However, when considering charge transfer losses in buried channel devices only bulk traps are important. These defects create energy levels between the conduction and valence band, hence electrons may be captured by these new levels. These electrons are also emitted back to the conduction band after a certain time. For a signal packet this may lead to a decrease in charge as it is transferred to the output and may be quantified by its Charge Transfer Inefficiency (CTI), where a charge of amplitude $Q_0$ transported across $m$ pixels will have a reduced charge given by

$$Q_m = Q_0 (1 - CTI)^m. \quad (1)$$

The CTI value depends on many parameters, some related to the trap characteristics such as: trap energy level, capture cross-section, and trap concentration (density). Operating conditions also affect the CTI as there is a strong temperature dependence on the trap capture rate and also a variation of the CTI with the readout frequency. Other factors are also relevant, for example the occupancy ratio of pixels, which influences the fraction of filled traps in the CCD transport region. Previous studies have been reported [1]–[5].

II. SIMULATIONS

The UK Linear Collider Flavour Identification (LCFI) collaboration [6], [7] has been studying a device produced by e2V Technologies, with a manufacturer’s designation ‘CCD58’. It is a 2.1 Mpixel, three-phase buried-channel CCD with 12 $\mu$m square pixels.

Simulations of a simplified model of this have been performed with the ISE-TCAD package (version 7.5), particularly the DESSIS program (Device Simulation for Smart Integrated Systems). It contains an input gate, an output gate, a substrate gate and nine further gates (numbered 1 to 9) which form the pixels. Each pixel consists of 3 gates but only one pixel is important for this study—gates 5, 6 and 7. The simulation is essentially two dimensional but internally there is a nominal 1 $\mu$m device thickness (width). This is equivalent to a thin slice of the device with rectangular pixels 12 $\mu$m long by 1 $\mu$m wide. The overall length and depth of the simulated device are 44 $\mu$m and 20 $\mu$m respectively (Fig. 1).
Parameters of interest are the readout frequency, up to 50 MHz, and the operating temperature between 120 K and 300 K although simulations have been done up to 500 K. The charge in transfer and the trapped charge are shown in Fig. 2.

The signal charge used in the simulation is chosen to be similar to the charge generated by a minimum ionising particle (MIP), amounting to about 1620 electron-hole pairs for CCD58. DESSIS has a directive for generating heavy ions and this is exploited to create the charges. The heavy ion is made to travel in a downwards direction starting at 1.2 µm below gate 2 at 1 µs before charge transfer begins. This provides ample time for the electrons to be drawn upwards to the transport channel which is 0.25 µm beneath the gate electrodes.

The signal charge density, almost at output gate. Lower: Trapped charge density, from transfer of signal charge. The legend box refers to the region with positive depth values. The thin brown line is an oxide layer and the thin yellow line is a nitride layer.

A. Calculating CTI

Charge Transfer Inefficiency is a measure of the fractional loss of charge from a signal packet as it is transferred over a pixel, or three gates. After DESSIS has simulated the transfer process, a 2D integration of the trapped charge density distribution is performed independently to give a total charge under each gate.

The CTI for transfer over one gate is equivalent to

$$CTI = \frac{e_T - e_B}{e_S}$$

where:

- $e_S$ = electron signal packet density,
- $e_B$ = background trapped electron charge density prior to signal packet transfer,
- $e_T$ = trapped electron charge density under the gate, after signal transfer across gate.

In this way the CTI is normalised for each gate. The determinations of the trapped charge take place for gate $n$ when the charge packet just arrives at gate $n + 1$. If the determination were made only when the packet has cleared all three gates of the pixel, trapped charge may have leaked out of the traps. The total CTI (per pixel) is determined from gates 5, 6 and 7, hence

$$CTI = \sum_{n=5}^{7} \frac{e_T - e_B}{e_S}$$

where $n$ is the gate number. The background charge is taken as the trapped charge under gate 2 because this gate is unaffected by the signal transport when the charge has just passed gates being processed.

B. Initial tests of the DESSIS program

DESSIS simulations have been carried out with a zero concentration of electron traps as in unirradiated silicon. The DESSIS program is steered with a command file which contains electrode voltage values for each of the three phases as a function of time. For these simulations the voltage values (peak value 7 V), which were originally digitised from real experiments with CCD58, were replaced by reduced values without altering the frequency or phase.

Since there were no traps there was no trapped charge so a different estimator of CTI is required. The electron charge density left under gate $n$ when the charge packet has moved to gate $n + 1$ gives the partial CTI estimator. It is normalised by the original electron charge density. As before, the CTI for a pixel is computed by adding the partial CTI’s for gates 5, 6, and 7.

Figure 3 shows the variation of CTI with temperature for simulations with no traps at a clocking frequency of 50 MHz.

- $e_B$ = background trapped electron charge density prior to signal packet transfer,
- $e_T$ = trapped electron charge density under the gate, after signal transfer across gate.

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operates with a negligible CTI above 3 V and has a large CTI below 1 V. Also the CTI grows with temperature.

Examination of snapshots of electron density plots produced by DESSIS during a simulation run confirm that electrons leak out of the main charge packet during transfer at reduced clock voltages leading to an even distribution of electrons under all of the gates.

C. 0.17 eV and 0.44 eV traps

This CTI study, at nominal clock voltage, focuses only on the bulk traps with energies 0.17 eV and 0.44 eV below the bottom of the conduction band. These will be referred to simply as the 0.17 eV and 0.44 eV traps. An incident particle with sufficient energy is able to displace an atom from its lattice point leading eventually to a stable defect. These defects manifest themselves as energy levels between the conduction and valence band, in this case the energy levels 0.17 eV and 0.44 eV; hence electrons and/or holes may be captured by these levels. The 0.17 eV trap is an oxygen vacancy defect, referred to as an A-centre defect. The 0.44 eV trap is a phosphorus-vacancy defect—an E-centre defect. The 0.44 eV trap is an oxygen vacancy defect—an A-centre defect. The 0.44 eV trap is a phosphorus-vacancy defect—an E-centre defect—that is, a result of the silicon being doped with phosphorus and a vacancy manifesting from the displacement of a silicon atom bonded with the phosphorus atom [2].

In order to determine the trap densities for use in simulations, a literature search on possible ILC radiation backgrounds and trap induction rates in silicon was undertaken. The main expected background arises from $e^+e^-$ pairs with an average energy of 10 MeV and from neutrons (knocked out of nuclei by synchrotron radiation).

Table 1 shows results of background simulations of $e^+e^-$ pairs generation for three proposed vertex detector designs (from three ILC detector concepts).

| Simulator      | SiD | LDC | GLD |
|----------------|-----|-----|-----|
| CAIn/Jupiter   | 2.9 | 3.5 | 0.5 |
| GuineaPig      | 2.3 | 3.0 | 2.0 |

Table 1. Simulated background results for three different detector scenarios. The values are hits per square centimetre per $e^+e^-$ bunch crossing. SiD is the Silicon Detector Concept [8], LDC is the Large Detector Concept [9] and GLD is the Global Linear collider Detector [10].

Choosing the scenario with the highest expected background, that is the LDC concept, where the innermost layer of the vertex detector would be located 14 mm from the interaction point, one can estimate an $e^+e^-$ flux around 3.5 hits/cm$^2$/bunch crossing which gives a fluence of $0.5 \times 10^{12}$ cm$^{-2}$/year. In the case of neutrons, from two independent studies, the fluence was estimated to be $10^{10}$ n/cm$^2$/year [11] and $1.6 \times 10^{10}$ n/cm$^2$/year [12].

Based on the literature [13]–[21], the trap densities introduced by 1 MeV neutrons and 10 MeV electrons have been estimated with two established assumptions: the electron trap density is a linear function of dose, and the dose is a linear function of fluence. A summary is given in Table 2.

| Particle type | $E_e$ (eV) | Type   | $C$ (cm$^{-3}$) | $\sigma$ (cm$^2$) |
|---------------|------------|--------|----------------|------------------|
| 10 MeV e$^-$  | $0.17 \times 10^{11}$ | Acceptor | $1 \times 10^{14}$ | $1 \times 10^{-14}$ |
| 1 MeV n       | $0.44 \times (4.5 \ldots 7.1) \times 10^{8}$ | Acceptor | $1 \times 10^{11}$ | $3 \times 10^{-15}$ |

Table 2. Estimated densities of traps after irradiation for one year. For neutrons, the literature provides two values.

The actual trap concentrations and electron capture cross-sections used in the simulations are shown in Table 3.

| $E_e - E_c$ (eV) | Type   | $C$ (cm$^{-3}$) | $\sigma$ (cm$^2$) |
|-----------------|--------|----------------|------------------|
| 0.17            | Acceptor | $1 \times 10^{14}$ | $1 \times 10^{-14}$ |
| 0.44            | Acceptor | $1 \times 10^{11}$ | $3 \times 10^{-15}$ |

Table 3. Trap concentrations (densities) and electron capture cross-sections as used in the DESSIS simulations.

D. Partially Filled Traps

Each electron trap in the semiconductor material can either be empty (holding no electron) or full (holding one electron). In order to simulate the normal operating conditions of CCD58, partial trap filling was employed in the simulation (which means that some traps are full and some are empty) because the device will transfer many charge packets during continuous operation.

In order to reflect this, even though only the transfer of a single charge packet was simulated, the following procedure was followed in all cases. From $t = 0$ seconds to $t = 98 \mu$s, the gates ramp up and are biased in such a way to drain the charge to the output drain. The device is in a fully normal biased state then at 98 $\mu$s. To obtain partial trap filling, the simulation waits $2 \mu$s between 98 $\mu$s and 100 $\mu$s to allow traps to partially empty. The test charge is generated at 99 $\mu$s. The simulation then starts the three clock phases, varying voltage with time to cause the transfer of the signal charge packet through the device.

III. ANALYTICAL MODELS

The motivation for introducing the following two simple analytical models is to understand the underlying effects and to make comparisons with the DESSIS simulations (referred to as the “full simulations”).

2This waiting time is calculated from a 1% mean pixel occupancy with a 50 MHz readout frequency.
A. Simple CTI Model

Firstly, a simple analytical model is considered, based upon a single trapping level—a so-called Simple CTI model. This is significantly faster than a full simulation. It also provides a simple method to see the effect of changing parameters and demonstrates physics understanding.

The charge transfer process is modelled by a differential equation in terms of the different time constants and temperature dependence of the electron capture and emission processes. In the electron capture process, electrons are captured from the signal packet and each captured electron fills a trap. This occurs at the capture rate \( \tau_c \). The electron emission process is described by the emission of captured electrons from filled traps back to the conduction band, and into a second signal packet at the emission rate \( \tau_e \).

1) Capture and emission time constants: The Shockley-Read-Hall theory [22] considers a defect at an energy \( E_t \) below the bottom of the conduction band, \( E_c \), and gives

\[
\tau_c = \frac{1}{\sigma_e \nu_{th} n_s} \quad \tau_e = \frac{1}{\sigma_e \chi_e \nu_{th} n_c} \exp \left( \frac{E_c - E_t}{k_B T} \right)
\]

where:
- \( \sigma_e \) = electron capture cross-section
- \( \chi_e \) = entropy change factor by electron emission
- \( \nu_{th} \) = electron thermal velocity
- \( n_s \) = density of states in the conduction band
- \( n_c \) = density of signal charge packet.

It is assumed that \( \chi_e = 1 \).

At low temperatures, the emission time constant \( \tau_e \) can be very large and of the order of seconds. The charge shift time is of the order of nanoseconds. A larger \( \tau_c \) means that a trap remains filled for much longer than the charge shift time. Further trapping of signal electrons is not possible and, consequently, CTI is small at low temperatures. A peak occurs between low and high temperatures because the CTI is also small at high temperatures. This manifests itself because, at high temperatures, the emission time constant decreases to become comparable to the charge shift time. Now, trapped electrons rejoin their signal packet.

2) Charge Transfer Equation: From the fraction of filled traps, the following differential equation can be derived:

\[
\frac{dr_t(t)}{dt} = \frac{1 - r_t(t)}{\tau_c} - \frac{r_t(t)}{\tau_e}
\]

where \( r_t(t) \) is the time-dependent fraction of filled traps

\[
r_t(t) = \frac{n_t(t)}{N_t}
\]

\( n_t(t) \) = density of traps filled by electrons
\( N_t \) = density of traps

Considering that the traps are partially filled and using the initial condition:

\[
r_t(0) = r_t(0)e^{-t_{w}/\tau_e}
\] where \( r_t(0) \) is the fraction of filled traps after a mean waiting time, \( t_w \), the differential equation can be solved to provide an expression for the CTI:

\[
CTI = \frac{3N_t}{n_s} (r_t(t) - r_t(0))
\]

\[
r_t(t) = (r_t(0) - \tau_s/\tau_c)e^{-t/\tau_s+\tau_c/\tau_e} \frac{1}{\tau_s} + \frac{1}{\tau_e}
\]

\[
CTI = \frac{3N_t}{n_s} \left( \frac{\tau_s}{\tau_c} - r_t(0) \right) \left( 1 - e^{-t_{sh}/\tau_e} \right)
\]

where \( t_{sh} \) is the shift-time. For one gate, \( t_{sh} = 1/(3f) \), where \( f \) is the readout frequency.

This definition is for CTI for a single trap level. The factor of three appears since there is a sum over the three gates that make up a pixel.

3) Matching the CTI definition of the simulation: The Simple Model has been adapted by including initially filled traps and by the incorporation of a so-called \( P \) factor to CTI:

\[
P = e^{-t_{sh}/\tau_e} + e^{-2t_{sh}/\tau_e} + e^{-3t_{sh}/\tau_e}
\]

This models the situation where the trapped charge under gate 5 started to empty at time \( t \) minus three shift-times, that under gate 6 at \( t \) minus two shift-times and that under gate 7 at \( t \) minus one shift-time. An alternative factor, called \( P' \), has also been used to compare with simulated data. This is defined as:

\[
P' = 1 + e^{-t_{sh}/\tau_e} + e^{-2t_{sh}/\tau_e}
\]

and models the situation one shift-time earlier than for \( P \).

B. Improved Model

The second analytical model that has been developed is referred to as the Improved Model (IM), based on the work of T. Hardy et al. [23]. It is improved by adjusting initial assumptions to fit the study of CCD58. The Improved model also considers the effect of a single trapping level, but only includes the emission time in its differential equation:

\[
\frac{dn_t}{dt} = \frac{n_t}{\tau_e}
\]

where \( n_t \) is the density of filled traps. The traps are initially filled for this model and \( \tau_c \ll t_{sh} \). Nevertheless, to be consistent with the full DESSIS simulations (that use partially filled traps) the Improved Model uses a time constant between the filling of the traps such that the traps remain partially filled when the new electron packet passes through the CCD. The solution of this differential equation leads to another estimator of the CTI:

\[
CTI' = \left( 1 - e^{-t_{sh}/\tau_e} \right) \frac{3N_t}{n_s} \left( e^{-t_{join}/\tau_e} - e^{-t_{emit}/\tau_e} \right)
\]

\( t_{emit} = t_w \) is the total emission time from the previous packet.
\( t_{join} \) is the time period during which the charges can join the parent charge packet.
IV. SIMULATION RESULTS

The CTI dependence on temperature and readout frequency was explored using ISE-TCAD simulations.

1) 0.17 eV traps: Figure 5 shows the CTI for simulations with partially filled 0.17 eV traps at different frequencies for temperatures between 123 K and 260 K, with a nominal clock voltage of 7 V.

A peak structure can be seen. For 50 MHz, the peak is at 150 K with a CTI of $27 \times 10^{-5}$. The peak CTI is in the region between 145 K and 150 K for a 25 MHz clock frequency and with a value of about $43 \times 10^{-5}$. This is about 1.6 times bigger than the charge transfer inefficiency at 50 MHz. The peak CTI for 7 MHz occurs at about 142 K, with a maximum value of about $81 \times 10^{-5}$, an increase from the peak CTI at 50 MHz ($27 \times 10^{-5}$) by a factor of about 3 and an increase from the peak CTI at 25 MHz ($43 \times 10^{-5}$) by a factor of nearly 2. Thus CTI increases as frequency decreases. For higher readout frequency there is less time to trap the charge, thus the CTI is reduced. At high temperatures the emission time is so short that trapped charges rejoin the passing signal.

2) 0.44 eV traps: Simulations were also carried out with partially filled 0.44 eV traps at temperatures ranging from 250 K to 500 K. This is because previous studies [5] on 0.44 eV traps have shown that these traps cause only a negligible CTI at temperatures lower than 250 K due to the long emission time and thus traps remain fully filled at lower temperatures. The results are depicted in Fig. 6.

The peak CTI is higher for lower frequencies with little temperature dependence of the peak position.

3) 0.17 eV and 0.44 eV traps together: The logarithmic scale view (Fig. 7) of the simulation results at the different frequencies and trap energies clearly identifies an optimal operating temperature of about 250 K.

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A. Comparisons with Models

Figure 8 shows that the basic Simple Model does not agree well with the full simulation. Applying the $P$ and $P'$ factors and the Improved Model.

Fig. 5. CTI values for simulations with 0.17 eV partially filled traps at clocking frequencies 7, 25 and 50 MHz.

Fig. 6. CTI values for simulations with 0.44 eV partially filled traps at clocking frequencies 7, 25 and 50 MHz.

Fig. 7. CTI values for simulations for partially filled 0.17 eV and 0.44 eV traps. Comparison of CTI at frequencies 7, 25 and 50 MHz for different trap energy level on a logarithmic scale.

Fig. 8. CTI values against temperature for different models with 50 MHz readout. See text for details of the Simple Model and its adaption with the $P$ and $P'$ factors and the Improved Model.
to overcompensate for the deficiencies and the $P'$ factor gives a reasonable but not perfect agreement.

Figure 9 compares the full DESSIS simulation for 0.17 eV and 0.44 eV traps and clocking frequency of 50 MHz to the Improved Model. It emphasises the good agreement between the model and full simulations at temperatures lower than 250 K with 0.17 eV traps, but shows a disagreement at higher temperatures for the 0.44 eV traps.

If the 0.44 eV trap electron capture cross-section in the Improved Model is increased to $10^{-14}$ cm$^2$, a somewhat better agreement is found, as shown in Figure 10. However it is clear that there are limitations with the Improved Model. They could relate to a breakdown of the assumptions at high temperatures, to ignoring the precise form of the clock voltage waveform, or to ignoring the pixel edge effects. Further studies are required.

V. CONCLUSIONS

The Charge Transfer Inefficiency (CTI) of a CCD device has been studied with a full simulation (ISE-TCAD DESSIS) and compared with analytical models.

Partially filled traps from the 0.17 eV and 0.44 eV trap levels have been implemented in the full simulation and variations of the CTI with respect to temperature and frequency have been analysed. The results confirm the dependence of CTI with the readout frequency. At low temperatures ($< 250$ K) the 0.17 eV traps dominate the CTI, whereas the 0.44 eV traps dominate at higher temperatures.

A large emission time constant $\tau_e$ results in a trap remaining filled for much longer than the charge shift time. Further trapping of signal electrons is not possible so the CTI is small at low temperatures. At high temperatures the emission time constant decreases to become comparable to the charge shift time. Trapped electrons rejoin their signal packet and, because most are emitted during the charge transfer time, there is again a small CTI. For intermediate temperatures, a clear peak structure is observed.

Good agreement between simulations and a so-called Improved Model has been found for 0.17 eV traps but not for 0.44 eV traps. This shows the limitations of the Improved Model with respect to the full simulation.

The optimum operating temperature for CCD58 in a high radiation environment is found to be about 250 K.

Interest is now moving to alternative CCD designs, particularly 2-phase column-parallel readout devices. The extensive amount of research that has been carried out on CCD58 contributes to the development of future CCD designs.

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