Realization of Radar Signal Calibrator Based on FPGA

Anzhong Jin 1,*, Shiyu Xue 2 and Axin Jin 3

1 2 3 Xi’an Institute of Space Radio Technology, Xi’an, China

* Corresponding author e-mail: jinanzhong@163.com

Abstract. In view of the shortcomings of pulse radar signals that are easily affected by internal and external conditions, a pulse radar signal calibrator is designed based on FPGA. The radar's transmitted signals are pulsed by the calibrator in real time, and the radar signals can be calibrated by inversion analysis. At the same time, the functions of timing reception of the status information of each extension and saving of the collected data to the USB mobile hard disk are controlled by the host computer. After testing, the measurement accuracy error caused by the transmission path during the radar system's working process can be calibrated by this radar signal calibrator, the accuracy of the radar system link is improved, and the accuracy of the radar system measurement is guaranteed. Therefore, it can be widely used in ground calibration equipment of pulse radar.

Keywords: Radar signal, FPGA, Calibrator, Remote sensing

1 Introduction
Remote sensing technology is a technology that uses artificial satellites, airplanes, or other aircraft as a platform to collect electromagnetic radiation signals from ground objects, so as to identify information such as the earth's environment and resources. The electromagnetic radiation signal is the collected radar signal. The accuracy of this signal seriously affects the subsequent data processing and the accuracy of the final inversion result.

However, the radar signal in the acquisition process due to components, path attenuation, and antenna pattern changes will cause the problem of inaccurate acquisition signals [1] At present, there is no radar calibrator at home and abroad that can reduce external influences.

The FPGA-based radar signal calibrator is used to ensure the accuracy, stability and continuity of the radar signal measurement data. Therefore, the radar signal calibrator can be widely used in remote sensing equipment [2].

2 Scheme Design
The radar signal calibrator based on FPGA designed in this paper includes 5 functional modules, which are: the status information of each module of the timing receiving system; AD acquisition enable control; frequency synthesizer output acquisition clock control; extraction of GPS receiver position and time information; Time counting and time reference setting of remote sensing packet. The following analysis of these five modules [3].
2.1 Timely Receiving System Status Information of Each Module
The status information in this design includes digital status information and analog status information. The reception of digital state information includes the digital state information in the servo controller, receiving channel, forwarding channel and frequency synthesizer in this design. The above information is input to the FPGA through the driver module, and the FPGA receives this information at a regular time (1s cycle) and stores it in the FPGA in memory. The simulation status information includes the remote measurement of the power of the receiving channel and the power of the forwarding channel. The sampling period is 0.1 ms. The maximum value is 1s of sampled data. The value of this 1s peak power is stored in the internal memory of the FPGA. [4].

2.2 AD Acquisition Enable Control
The pulse radar signal collector includes two working modes of calibration within the gain and radar signal acquisition. When set to in-gain calibration mode, the FPGA outputs AD acquisition enable signals, and AD collects 1s data (for the solution's own calibration); when set to radar signal acquisition mode [5], the control signal board receives the acquisition mode control instruction sent. The AD acquisition enable signal is output. After the control signal board receives the continuous acquisition mode instruction, AD continuously acquires 20s.

2.3 Frequency Synthesizer Output Acquisition Clock Control
When the control signal board receives the working mode control instruction, that is, in-calibration mode and radar signal acquisition mode (continuous acquisition mode), it controls the frequency synthesizer calibration signal enable signal, triggers an external trigger signal for AD acquisition, and controls the frequency synthesizer. Output 40MHz for AD acquisition.

2.4 Extracting GPS Receiver Position and Time Information
The control signal board receives the data packets periodically sent by the GPS receiver through the 422 bus, extracts the X, Y, Z coordinates in the data packets and the UTC time in the data packets, and stores the data in the FPGA internal memory [6].

2.5 Time Counting and Time Reference Setting of Remote Sensing Packet
Taking the rising edge of the GPS second pulse as a reference, a counter with a frequency of 40MHz is used for counting. The flowchart is shown in Figure 1. When the control signal board sends an enable signal to the AD acquisition, the GPS time and time count value at this moment are stored in the internal memory of the FPGA. In the subsequent data processing, the time count value is extracted to make a timing comparison with the radar transmission signal [7].

3 Hardware Design
The above five function modules are integrated in the control signal board, and the core is an FPGA module, which is externally connected with the Ethernet PHY module, AD module, DDR3 module, MsATA module, QSPI flash module, and RS485 and RS422 interface chip modules. The functional block diagram of the control signal board is shown in Figure 1.
3.1 FPGA Unit

The FPGA selected Xilinx’s ZYNQ-7000 series FPGA. Each product of the Zynq-7000 embedded processing platform series uses a dual-core ARM Cortex-A9 MPCore processing system with NEON and a double-precision floating-point engine. The system is completed by hard wiring. Full integration including L1, L2 cache, memory controller, and common peripherals [8].

FPGA performs level control on the receiving channel, forwarding channel, and frequency synthesizer through the level conversion chip. The FPGA collects the power measurement values of the receiving, forwarding, and frequency synthesis channels through the SPI interface; the temperature values are collected through the I2C interface; and the current and voltage detection values of the power module are collected through the RS422 interface [9]. The host computer indirectly controls the PL logic through the 485 interface of the PS. The PL unit is connected to an mSATA solid state hard disk to realize the real-time storage of AD sampling data; the TX / RX port is connected to an RS422 interface chip to communicate with the GPS receiver and the power module current and voltage monitoring module. The functional block diagram of the control signal board is shown in Figure 2.

![Functional block diagram of the control signal board](image-url)

**Fig. 2.** Functional block diagram of the control signal board

There are three main modes of FPGA operation, and the schematic diagram of the FPGA engineering process in each mode is shown in Figure 3. The host computer uses the 485 interface to control the PL indirectly through PSGIO, as shown by arrow 1 in the figure below. Low-speed protocol reading and writing, device status reading, and device configuration are implemented in this way.
3.2 USB unit

Zynq-7000 comes with a USB2.0 controller and an external USBPHY. The USB is in Host mode. The USBPHY selects the USB3320 of the SMSC company. This module conforms to the USB2.0 specification version 1.0 USB2.0 peripherals; 480Mbps USB2.0PHY conforming to PIPE2.0; has an 8bit-ULPI interface.

3.3 Clock scheme

Because each module of FPGA has different clock requirements, the clock scheme is summarized as shown in Table 1.

| frequency (MHz) | Demand device | Level standard | Note                                |
|----------------|---------------|----------------|-------------------------------------|
| 33.33          | ZYNQ-PS       | 3.3LVCMOS      | PS system reference clock           |
| 25             | ZYNQ-PL       | 3.3LVCMOS      | PL system reference clock           |
| 25             | ETH-PHY       | 3.3LVCMOS      | Ethernet PHY reference clock        |
| 12             | USB-PHY       | 3.3LVCMOS      | USB PHY reference clock             |
| 16             | ADS1158       | 3.3LVCMOS      | ADC acquisition clock               |

4 Software Design

The device software is divided into embedded software and host computer software. The embedded software mainly completes functions such as hardware initialization and hardware interface implementation. The host computer software provides a human-machine interface, which can conveniently control the device. The host computer and embedded the communication is through RS485 serial port. The soft armor structure is shown in Figure 4:

4.1 Embedded Software Design

When the embedded software runs, it initializes and configures each interface of the control device, so
that it can run normally. Then receive the command from the host computer, parse and execute the corresponding action after receiving it, at the same time receive the data and status information sent from the control device, and send it to the host computer in a package.

4.2 PC software
The host provides a human-machine interface. This design is divided into three control parts according to functions: data acquisition, equipment management, and equipment maintenance functions.

The device collection function is to control the device to collect through AD, collect data into the device's memory, at the same time can manage the internal storage of the device, view the storage list, and export the internal storage to the outside through the network and USB.

Click "Start" on the interface to perform data collection, and the device will automatically generate a file. After data collection is completed, click "Stop". At this time, the file can be exported. The host computer can monitor the USB insertion status on the device, display the device list, and export the file to an external storage device. The file list of the device can be refreshed and deleted for maintenance operations. When using a network connection, internal data can be exported via the network[10].

5 System test
Test the host computer and the control board online. The host computer software controls the acquisition of radar signals, and the signal board is responsible for signal processing. The specific test process is as follows.

First, set the acquisition speed to 40MBps, the acquisition byte to 1265MB, the export speed to 50, and the export byte to 50MB on the host computer. Next, click "Start" to collect data; finally, click "Stop" after data collection is complete. View the data stored in the USB storage device. Pulse radar power accuracy verification oscilloscope shows: frequency 1.0000000MHz; amplitude 2.000Vpp; offset 0.000Vdc; pulse width 50.0ns; rising edge 8.4ns.

In addition to meeting the above two indicators, the program can also meet other indicators. A summary of all functional compliance is shown in Table 2.

| Indicator demand | Compliance |
|------------------|------------|
| AD acquisition enable control | Match |
| Frequency synthesizer calibration signal output enable control | Match |
| Frequency synthesizer 40MHz, 40 / 3MHz clock signal selection | Match |
| Extract GPS receiver position and time information | Match |
| Time count | Match |
| Remote Sensing Packet Time Base | Match |
| Execute industrial computer control command | Match |
| AD acquisition data is placed on the USB mobile hard disk | Match |
| AD collects data through the network interface (with file system) | Match |

6 Conclusions
This paper proposes a design scheme of pulse radar signal calibrator based on FPGA. The pulse radar signal calibrator realizes timing reception of the status information of each extension of the system through the host computer control, AD acquisition card enable control, frequency synthesizer calibration signal output enable control, frequency synthesizer output clock signal, and GPS receiver position. The function of saving time information, time reference of remote sensing package and AD acquisition data to USB mobile hard disk. The pulse radar signal calibrator can be used to calibrate the radar signal to ensure its accuracy, stability and continuity. The online test results can be validated by the above design method and can be used in pulse radar ground calibration equipment.
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