Volcano: Stateless Cache Side-channel Attack by Exploiting Mesh Interconnect

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ABSTRACT

Cache side-channel attacks lead to severe security threats to the settings that a CPU is shared across users, e.g., in the cloud. The existing attacks rely on sensing the micro-architectural state changes made by victims, and this assumption can be invalidated by combining spatial (e.g., Intel CAT) and temporal isolation (e.g., time protection). In this work, we advance the state of cache side-channel attacks by showing stateless cache side-channel attacks that cannot be defeated by both spatial and temporal isolation.

This side-channel exploits the timing difference resulted from interconnect congestion. Specifically, to complete cache transactions, for Intel CPUs, cache lines would travel across cores via the CPU mesh interconnect. Nonetheless, the mesh links are shared by all cores, and cache isolation does not segregate the traffic. An attacker can generate interconnect traffic to contend with the victim’s on a mesh link, hoping that extra delay will be measured. With the variant delays, the attacker can deduce the memory access pattern of a victim program, and infer its sensitive data. Based on this idea, we implement Volcano and test it against the existing RSA implementations of JDK. We found the RSA private key used by a victim process can be partially recovered. In the end, we propose a few directions for defense and call for the attention of the security community.

1 INTRODUCTION

Isolation is one of the fundamental security principles to protect sensitive information. As a concrete implementation, virtual memory isolation, which separates the memory space between processes managed by an operating system (OS), and virtual machines (VMs) managed by a hypervisor, is universally deployed. Yet, isolation at the memory level is not sufficient, as there are many other shared hardware resources that can be exploited. One prominent example is CPU cache. Since the memory access also leads to updates on cache but memory isolation is not directly mapped to the cache, a plethora of previous works exploit the shared cache as a side-channel to carry out timing attacks, and various sensitive information has been found unprotected from the lens of cache, resulting in the leakage of user input [65], cryptographic key [55], etc.

Existing Cache Side-channel Attacks and Defenses. By timing the interval of accessing a cache line, existing attacks learn whether the associated memory addresses have been loaded by a victim program, and further deduce the sensitive information. Many techniques have been proposed, like Flush+Reload [72], Prime+Probe [11], and the recent Xlate [61], based on different assumptions, e.g., using shared libraries [72], sharing LLC (Last-level Cache) across cores [43], and sharing MMU (Memory Management Units), etc.

These attacks can be categorized to stateful cache attacks, as the victim program introduces micro-architectural state changes that can be sensed by an attacker [15], e.g., through creating eviction sets. However, this attack condition may not be fulfilled nowadays, due to rise of spatial and temporal isolation. For example, Intel Xeon CPUs introduces Cache Allocation Technique (CAT) [47], which was designed to maintain QoS of cache usage, but later found to be a panacea for cache attacks [42]. CAT assigns LLC cache ways to cores exclusively, which spatially isolate LLC and break all attacks based on eviction set conflict on LLC (e.g., [43]). Academic proposals extend the protection realm to other cache units, like directories [71]. Besides spatial protections, [13] proposed an OS abstraction for temporal isolation, which is effective against nearly every cache attack with the existing hardware support.

Stateless Cache Side-channel Attack. Given that spatial and temporal partition can eliminate the root cause of cache side-channel attacks, or micro-architectural state change, is it possible to evolve the attack to make it stateless? It sounds counter-intuitive but there is hope. According to Ge et al. [13], there exist a few stateless channels, e.g., on memory bus contention [69], that do not incur micro-architectural state change. These stateless channels were uncovered a long time ago [69], but they are all limited to construct covert channels [13]. If one can use the stateless channel as the medium to attack the cache, the goal might be achievable. A more important feature is that even the highly secured scheme like temporal isolation is admittedly ineffective against stateless channels, due to the lack of hardware support on bandwidth partition [13], indicating that stateless attacks could hardly be defeated.

In this work, we revisit the direction of stateless channels and explore the possibilities of combining them with cache attacks. By investigating the latest architecture of Intel CPU, e.g., Xeon Scalable Processor [31], we identified a new stateless channel, and found it can be exploited for our goal. In these CPUs, the interconnect between cores and other units (e.g., I/O units) is turned into a mesh network, consisting of a 2D matrix of tiles. Figure 1 right shows the mesh network. Although mesh interconnect shows great advantage in latency and bandwidth on multi-core CPUs [2, 62], it could leak information about the cache transactions of a program, because different cache transactions share the mesh links. Hence, there exists bandwidth contention when cache lines run across mesh, and the attacker might use that to infer the victim’s secret.

Based on this insight, we propose stateless cache side-channel attacks, or Volcano. Our key idea is to let a core occupied by an attacker program keeps probing the path that the cache transaction of a victim program pass by, and measure the interval. When the core occupied by the victim program accesses a remote LLC slice, the accumulated mesh traffic volume will rise, hence increasing the interval observed by the attacker, especially when the mesh link is congested. By probing the mesh link at high frequency, the attacker
could reconstruct the execution flow of the victim program, and further deduce the secret.

**Challenges.** Although Volcano is easy to understand, implementing an effective attack is challenging. Here we list the key challenges.

- **Locating the traffics on the CPU layout.** Though the attacker and the victim threads run within the same CPU, the attacker does not know where the victim traffic originates from and to.
- **Synthesizing targeted probe traffic.** The mesh interconnect is invisible to the upper-layer application, and there is no API to let an attacker direct mesh traffic to a given destination.
- **Sampling a mesh link.** Though Intel provides tools like PMON [30] to measure mesh traffic for each mesh link, we found they require root privilege and are unable to sample a mesh link at a high rate.
- **The coarse-grained probe.** Volcano can only observe whether there are traffics from/to a core rather than the status of a specific cache line.

**Attack Techniques.** To tackle the above challenges, we design a new method to reverse engineer the CPU layout and map the core/CHA (Cache Home Agent) IDs to all the tiles. Based on the layout, we carry out a theoretic analysis of the distribution of mesh traffic from/to a core, to guide the selection of mesh links to be contended with. To enable targeted and robust probes, we carefully construct an eviction set, which can be mapped to a specific LLC slice, and contained in a L2 set. Accessing the eviction set generates stable mesh traffics and the attacker can rely on the timing to measure the congestion on mesh. **To notice is that the eviction set does not conflict with the victim.** It is only used to trigger mesh traffics. Therefore, defenses trying to prevent adversarial cache eviction can be evaded under Volcano.

As a showcase for the attack effectiveness, we analyzed fast modular exponentiation algorithm and sliding windows algorithm of RSA respectively, by using Volcano to recover the 2048-bit private RSA key. For the fast modular exponentiation algorithm, we found the attacker has 47% chances to recover 2040 bits correctly. For the sliding windows algorithm, which was included in the crypto library of JDK, the attacker can recover over 30% of the 2048 bits, with the help of a cryptographic method [3].

**Contributions.** We summarize the main contribution of our work as follows.

- We identify a new security implication of CPU mesh interconnect, and show it can be exploited to construct a powerful stateless side-channel.
- We propose a new method to reverse-engineer the CPU layout, which allows an attacker to precisely locate the victim core on the mesh structure and analyze the traffic on mesh.
- We develop Volcano, using the stateless channel as a probe to conduct cache side-channel attack.
- To show the consequences of Volcano, we evaluate our attack on the off-the-shelf RSA implementations.

## 2 BACKGROUND AND RELATED WORKS

In this work, we investigate the security of the cache architecture of Intel Xeon Scalable Processors [31], which have gained a prominent market share in cloud computing [34]. We first overview their cache design. Then, we briefly introduce the prior cache side-channel attacks and the corresponding defenses. Finally, we overview the research of stateless channels that serve as our attack primitives.

### 2.1 Cache Architecture of Intel Xeon Scalable Processors

Though at the high level, the Intel Xeon Scalable Processors inherit the L1/L2/L3 (LLC) cache hierarchy from their predecessors, cache management is upgraded under mesh interconnect. We introduce this feature first. Then we describe the general cache hierarchy and how it is evolved.

**Mesh Interconnect.** When a CPU chip contains multiple cores, the connection topology among them, or on-chip interconnect is a key factor determining the CPU performance. The old design of interconnect (e.g., in Intel Xeon E5) mimics the multiprocessor architecture, in that a shared ring-bus connects all cores together [16], as illustrated in Figure 1 left. However, the core-to-core latency could increase linearly along with the growth of cores within one CPU die, because the communication between two cores could be routed through all other cores.

Since Xeon Skylake-SP server CPU family [58] (released in 2017), Intel revamped the interconnect design with mesh, which is also adopted by the latest generation of Intel server CPUs, e.g., Xeon Cooper Lake-SP, and expected to be the default design in the near future [57]. Besides Intel CPUs, mesh interconnect has also been adopted by other processors, like Tile Processors [2, 54, 62], and ARM server CPUs [15]. In essence, the chip is structured as a 2D matrix of identical tiles [67] and each tile either consists of a core (together with cache), or a non-core component like IMC (Integrated Memory Controller), UPI (Ultra Path Interconnect), and I/O unit. Each tile is connected to its vertical and horizontal neighbors, and the traffic of each direction (in total 4) is managed through a mesh stop inside the tile. Figure 1 right illustrates the mesh structure. Mesh interconnect caps the core-to-core latency at a much lower rate, because the number of hops between any pair of tiles is only proportional to the square root of the number of tiles. In addition to reducing latency, mesh interconnect also enlarges the bandwidth available to each core, because the communication traffic is distributed across more tiles and less likely to congest a route.

It is worth mentioning that the mesh of Intel chips implements a simple XY routing protocol, as such the route is always the same given a pair of source and a destination tiles [58]. Specifically, a packet always flows to the row of the destination tile vertically, and then moves to the destination horizontally. This static routing mechanism simplifies the implementation of mesh, but on the other hand opens up new cache side-channels, when the adversary carefully crafts cache requests, and we elaborate the attack method in Section 5.

**Cache Hierarchy.** Modern processors all feature a hierarchy of cache to localize the frequently accessed data and code, in order to reduce access latency. Each core has its own private cache, e.g., L1 and L2 cache. And there is also L3 cache, or last-level cache (LLC).
2.2 Cache Side-channel Attack

Cache side-channel attack bypasses memory isolation and it is particularly concerning in the cloud setting, where multiple users share the same physical machines [32, 43, 74]. Below we overview the existing attack methods, and classify them by whether they assume memory sharing between victim and attacker.

Sharing Memory. Running processes often share identical memory pages, e.g., through the shared libraries, to reduce memory overhead. Shared memory leads to shared cache, and flush+reload exploits such condition for cache side-channel attack. It takes three steps. First, the attacker sets all the cache lines mapped to the shared memory as invalid, by using cache clearance instruction clflush. Then, the attacker waits a period of time for the victim to access the addresses of the shared memory. Finally, the attacker accesses the shared addresses and counts the cycles (e.g., through rdtsc) to measure the latency, and infer the code/data access pattern of the victim. Flush+Reload has been demonstrated effective on LLC [72] of a PC and cloud instances [74], resulting in leakage of encryption keys [32] and keystroke events [65]. It has been evolved to variations [14] like flush+flush [23], which is stealthier by avoiding the extra memory access. On the other hand, this attack can be mitigated when clflush is banned [46]. To address this limitation, evict+reload [24] was proposed, which uses cache conflicts as a replacement for clflush.

Not Sharing Memory. When memory is not shared, an attacker can still cause cache contention, due to memory addresses of different programs can share a cache set. Prime+Probe exploits such feature, and it also takes three steps. First, the attacker collects a set of cache lines that can fill a cache set and access the related memory addresses. Next, the attacker waits for the victim to evict the cache lines. Finally, the attacker measures the access latency. Though Prime+Probe initially targeted L1 cache [49], LLC that is inclusive has also been attacked [32, 43]. A number of variations have been developed [14]. For instance, Prime+Abort [11] measures the Intel TSX (Transactional Synchronization Extensions) abort rather than access latency. Instead of letting the victim evict the cache lines, evict+time let the attacker evict a cache set, and then invokes the victim operation [19, 38].

Indirect Attacks. Recently, researchers started to investigate the interplay between other CPU units and cache, to make the attack more evasive. For instance, Xlate [61] and Tlbbleed [18] exploited MMU (Memory Management Units) and TLB (Translation Lookaside Buffers) to leak victim’s cache activity. The recent Intel Xeon Scalable Processors started to use non-inclusive LLC, which raised the bar for LLC cache attacks. Yet, Yan et al. [70] showed that by targeting cache directories (or Snoop Filter), the units tracking which core contains a copy of a cache line, attacking non-inclusive LLC is feasible.

One major assumption of the prior attacks is that the attacker’s code is on the same machine as the victim’s. Recently, attacks over network connections were studied. By exploiting RDMA (Remote Direct Memory Access) and DDIO (Data Direct I/O), a remote attacker can access LLC [56] of CPU and cache inside NIC [37], launching side-channel attacks.

On an orthogonal direction, transient execution attacks [7] like spectre [36], meltdown [41] and foreshadow [60] modulate the state of the cache to construct covert channels, and exfiltrate information from speculatively executed instructions. Volcano focuses on side channels and we will investigate whether Volcano can be leveraged by transient execution attacks in the future.

2.3 Defenses against Cache Side-channels

Software Defenses. Since OS controls the allocation of memory to programs, the access to the physically-indexed caches can be isolated along with memory. Page colouring takes the advantage of the overlapping bits between cache set index and page index (for virtual-to-physical address translation). Pages can be assigned with different “colours” (i.e., the overlapping bits), and the colour decides which cache sets they are mapped to. Therefore, cache accesses are isolated along with memory access. Initially being used to improve system performance [4, 33, 73], page colouring has...
been re-purposed to build defenses, by isolating the cache that the
untrusted code can directly access [35, 75].

**Hardware Defenses.** Another perspective to defeat cache side
cannels is hardware-based isolation. To provide better cache QoS,
Intel has implemented a technique named *Cache Allocation Tech-
nology (CAT)* [47]. It allocates different cache ways to different COS
class of service). Each core is also associated with one or more COS.
A core can access a cache way only when they share at least one
common COS. Still, directly enforcing cache isolation with CAT is
not straightforward, as the provided COS is limited to 4 or 16.
CATalyst [42] adjusted CAT to protect LLC by separating it into a
secure and a non-secure partition, and forced the secure partition
to be loaded with cache-pinned secure pages. On ARM, hardware
mechanism like Cache Lockdown, can enable similar protection by
pinning whole sets of the L1-I and L1-D caches [1].

Hardware-based cache isolation and its extension are supposed to
mitigate the attacks that bypass the software defenses. For exam-
ple, by partitioning the page table and TLB with CATalyst,
Xlate [61] and TLBleed [18] can be mitigated. To defend against
directory-based attack [70], Yan et al. proposed SecDir to partition
and isolate directories [71].

In addition to CAT, another hardware feature of Intel, TSX has
been used as defense [22]. Intel TSX introduces hardware transac-
tion, in which case transactions would abort if it were interfered.
By putting sensitive data and code in a transaction and pin it to a
cache set, cache eviction triggered by adversaries will lead to abort.

**Temporal Isolation.** Both hardware and software defenses aim at
isolating resources spatially, which cannot be isolated due to not
enough page coloring granularity. Ge et al. proposed to enforce
temporal isolation with OS abstraction [13], so the existing cache
cside-channels [11, 70] can be mitigated when combining with spatial
isolation techniques (hardware and software). However, the defense
is only applicable to x64 microkernel.

Table 1 summarizes the existing cache side-channels and how they
are impacted under the existing defenses.

### 2.4 Stateless Channels

According to Ge et al. [13], microarchitectural side-channels exploit
the competition of hardware resources, which can be classified into
two categories: *microarchitectural state* and *stateless interconnects.*
The first category includes caches, TLBs, branch predictors, and
DRAM row buffers, on which resource contention leads to the
state changes observable to the adversary. The second category
includes buses and on-chip networks. Though the concurrent access
leads to a reduction of available bandwidth, no interference on the
microarchitectural state should be observed.

Exploiting stateless interconnects for attacks is not brand new. I/O
bus contention [20, 21, 26, 27] and memory bus lock [69] have
been exploited to construct covert channels. However, we found
the research on this direction has been *stalled* probably due to that
the exploited hardware features are outdated (e.g., VAX security
kernel [20, 21]). So far, no practical side-channel attacks through
interconnect are known [14]. In this work, we aim to revive this
direction and demonstrate that stateless interconnects can be ex-
ploded for side-channel attacks.

### 3 ATTACK OVERVIEW

In this section, we first introduce the threat model and compare it
with the ones of prior related works. Then, we demonstrate why
the leakage from mesh interconnect matters. Finally, we overview
the steps of our attack Volcano.

#### 3.1 Threat Model

We assume the attacker who intends to extract secret information,
e.g., encryption keys, shares the same CPU with the victim,
but resides in different cores from the victim. We envision Vol-
cano is effective in the cloud environment, when co-residency is
achieved [63]. We also assume all the existing hardware and soft-
ware defenses against the cache side-channel attacks are deployed
and turned on, like page coloring and CATalyst. We target the lat-
est high-end CPU, Intel Xeon Scalable CPUs, where core-to-core
communication goes through mesh interconnects.

Here we compare our setting to the existing cache attacks. The
strongest assumption made by the prior works is the sharing of
memory addresses (shown in Figure 2 left), like FLUSH+RELOAD.
However, memory sharing can be turned off for the critical data/c/
code. A weaker assumption is that cache sets are shared (shown in
Figure 2 right), so the attacker can evict cache lines of the victim (or
vice versa), like PRIME+PROBE. Under this assumption, the attacker
either shares in-core private L1/L2 cache with the victim [49], or out-
of-core LLC (either inclusive LLC [32] or non-inclusive LLC [70]).

\[\text{Table 1: Comparison of cache side-channel attacks. "✓" means the attack can be defended. "-" means the defense is ineffective.}\]

| Co-location Assumption | Attack Channel | Page Coloring | Hardware Isolation | Temporal Isolation | Key Feature |
|------------------------|----------------|--------------|-------------------|-------------------|-------------|
| Flush+Reload [72]       | Memory LLC     | ✓            | CAT               | ✓                 | Exploit shared memory |
| Prime+Probe [32, 43]    | Cache LLC      | ✓            | CAT               | ✓                 | No need to share memory |
| TLBleed [18]           | Core TLB       | -            | Disable HT        | ✓                 | Attack TLB not cache |
| Attack Directories, not caches [70] | Cache Directory | ✓ | SecDir [71] | ✓ | Work on non-inclusive cache |
| Prime+Abort [11]       | Cache TSX Status | ✓ | CAT | ✓ | Does not rely on timing instruction |
| Xlate [61]             | Cache MMU      | -            | -                 | ✓                 | Lure MMU to access cache |
| Volcano                | Mesh Mesh      | -            | -                 | -                 | No need to co-locate in cache |
3.3 Challenges

Though creating the contention-based side-channel on mesh interconnect seems easy, there are multiple challenges we need to address. 1) The attacker needs to know where the victim program is located on the mesh layout, and where the victim traffic flows from and to. But the mapping between the high-layer program primitives, like processes and threads, to the low-layer hardware units, like mesh tiles, is obscured. In fact, Intel even keeps the CPU layout, e.g., which tile has which core, as proprietary information. Besides, the relation between cache transactions and mesh traffic is unknown. 2) There is no ISA support for the attacker to generate direct mesh traffic between two cores. The attacker can only access her own memory to indirectly produce mesh traffic. Though Intel provides a tool, PMON [50], for users to profile mesh traffic, the statistics are aggregated over a long period of time. Besides, PMON can only be used by root users. We want the attacker to be able to sample the mesh traffic at high frequency as a non-root user. 3) Comparing with the stateful cache side-channels, where the operand address of an instruction can be evicted and probed individually, VOLCANO only has visibility to traffic from/to a core, which is more coarse-grained. We will address the above challenges with novel techniques in reverse engineering, probe design, and decoding.

3.4 Attack Steps

VOLCANO consists of three steps summarized below. Step 1 is done before attacking the victim.

**Step 1: Layout Reverse-engineering (Section 4).** Before launching VOLCANO, the attacker could build the mapping between a core/CHA ID to its geometric location on the CPU layout, to help the later stage. We use core/CHA IDs to fill the layout map because they are bounded with applications, and the tools to obtain the IDs are accessible to non-root users. Since the layout should be the same for all CPUs of the same model and stepping level, this only has to be done once.

**Step 2: Probe & Measurement (Section 5 and 6.1).** When launching attacks, the attacker runs an application on the target machine, sharing CPU with the victim. The attacker could first identify the geometric location of the cores hosting the victim application, by querying the core ID associated with the victim process and locate the tile on the reverse-engineered layout. The information is leveraged to identify the paths that contend with the victim’s mesh traffic at high probabilities. If the victim process is invisible to the attacker, e.g., on the virtualized platforms, the attacker can select a random path. Our evaluation shows the information leakage from the random path contention is still prominent. To direct mesh packets over the selected paths, the attacker constructs an eviction set, and probes the memory addresses within it. The probe is issued repeatedly and the interval consumed by each probe is logged. To notice is that the eviction set does not conflict with the victim in the cache, hence the existing defenses can be evaded.

**Step 3: Secret Inference (Section 7).** After the last step, the attacker obtains a sequence of intervals, and the secret underlying...
the sequence is to be decoded. This step is application-specific, as different victim programs produce different delay sequences. This step can be done at the attacker’s own machine. In particular, we use RSA to showcase how to decode a delay sequence.

4 REVERSE ENGINEERING THE CPU LAYOUT

In this section, we propose a new method to reverse engineer the CPU layout to help the later attack stage. To notice, this step requires root privilege to execute some profiling instructions, but during the actual attack, the root privilege is unnecessary. This step only needs to be carried out once for a targeted CPU model (and stepping level). We demonstrate the method on two Intel Xeon Scalable CPUs, 8260 and 8175, and the two steps are elaborated below. Due to the space limit, we leave the layout of 8175 in the appendix, as 8260 is the CPU for our attack evaluation.

4.1 Identifying the Enabled Tiles

There are three types of CPU dies, named LCC, HCC, XCC (for low, high, and extreme core counts), for Intel Xeon family, with 10, 18 or 28 cores in a die respectively [59]. However, when a CPU is shipped to the customers, Intel might intentionally disable some cores. For example, the Xeon Scalable 8175 CPU has 24 active cores, because Intel disabled 4 cores. Without knowing which cores are enabled, the attacker cannot find the best route to congest.

Here, we exploit the hardware feature of Intel CPUs to reveal such information. According to Intel’s document [30], a user can query the CAPID6 register to learn the ID of the tile whose CHA is disabled. When this is the case, the whole tile including the core and LLC inside are also disabled. Take Xeon Scalable 8175 as an example. Its CAPID6 contains 28 bits to indicate the status of all tiles, and a CHA is disabled if its associated bit is 0. By reading all bits of CAPID6, we found bit 1, 4, 24, 27 are set to 0. Then we leverage a previous research [44], which maps tiles to the CPU layout, and mark the tiles as disabled based on the CAPID6 bits. Table 8 in Appendix D shows what has been inferred on Xeon Scalable 8175. For Xeon Scalable 8260, though it has the same number of cores, the disabled tiles are different, (the IDs are 2, 3, 21 and 27).

4.2 Mapping CHAs and Cores to Tiles

As described in Appendix A, a requesting core talks to the CHA of a target core to initiate a cache read transaction. To direct the transaction between two tiles for mesh traffic, the attacker needs to know the ID of the requesting core and the ID of the target core. Yet, the relation between the core/CHA IDs and the tile IDs is not documented anywhere. We infer such information in this step.

According to [44], CHAs are sequentially numbered along with tiles, but when a tile is disabled, the CHA ID is skipped. As such, CHA is numbered from 0-23 for Xeon Scalable 8175, and tile #2 has CHA #1 because tile #1 is disabled. Table 9 in Appendix D shows the mapping of CHAs to tiles of Xeon Scalable 8175, and the first number of each pair is CHA ID.

Regarding cores, the task becomes non-trivial, as they are not sequentially numbered. McCalpin proposed a method to infer how the cores are aligned by reading “mesh traffic counters” [44]. However, the author also admitted the result needs to be disambiguated [28]. To improve the accuracy of the inferred layout, we propose a new method. Specifically, we bind a thread to a core (by setting its affinity [40] to the core ID), and use it to access 2GB memory. We monitor the Intel performance counter LCORE_PMA GV [30] and found the CHA yields the highest value when it co-locates with the core in the same tile. LCORE_PMA GV indicates the global power states of the core. When the increase of LCORE_PMA GV is observed, we assign the core ID to the tile. We repeat the process for every core, and the layout can be reconstructed. The second number of each pair shown in Table 9 in Appendix D is the core ID, for Xeon Scalable 8175. In Table 2, we show the inferred layout for Xeon Scalable 8260, which is different from 8175.

5 THE PROBE DESIGN

After the layout of the target CPU is inferred, the attacker uses a probe to contend with the mesh traffic generated from/to the victim’s core, and measure the probe latency to infer the victim’s activities. In this section, we describe the probe design.

5.1 Characterization of Mesh Traffic

How to select the paths that contend with the victim’s mesh traffic is a non-trivial problem, since different types of traffic are involved and each tile issues/receives traffic from different directions. Below we introduce the types of mesh traffic (termed T1-T7), summarized from the existing documents [45]. Then, we describe how traffic is distributed and the strategy of path selection. We use r and t to refer to the entity issuing the request and the target. Hence, the requesting core is termed Core_r, and the co-located L2, LLC slice and CHA are termed L2_r, LLC_r and CHA_r. For the target, the terms are Core_t, L2_t, LLC_t and CHA_t. We focus on the movement of cache lines or memory blocks, which take a much larger size than the mesh messages. The typical flow of cache access is described in Appendix A.

- **T1**: Core_r to LLC_t. When Core_r encounters L2 cache miss, it will compute the LLC slice ID and send messages to CHA_t (same or different tile with Core_r) co-located with LLC_t, asking if the cache line is presented. Also, when L2_r is about to evict a line to LLC_t, e.g., when the L2 cache set to be inserted is full, the memory sub-system of the core will pass the line from L2_r to LLC_t (same or different tile with L2_r).

- **T2**: LLC_t to Core_r. Following T1, if the cache line is in LLC_t, LLC_t will send the cache line to Core_r.

Table 2: Layout of Xeon Scalable 8260 CPU, with the same setting as Table 9.

| UPI | PCIE | PCIE | RLINK | UPI2 | PCIE |
|-----|------|------|-------|------|------|
| 0, 0 | 2, 16 | 7, 19 | 12, 3 | 17, 16 | 21, 17 |
| IMC0 | 3, 18 | 8, 2 | 13, 15 | 18, 10 | IMC1 |
| 1,12 | 4, 1 | 9, 14 | 14, 9 | 22, 11 |
| 5, 13 | 10, 8 | 15, 21 | 19, 22 | 23, 23 |
| 6, 7 | 11, 20 | 16, 4 | 20, 5 |

It is the abbreviation of Core Power Management Agent Global system state Value, according to [30].
• **T3: IMC to Core**. Alternatively, if the cache line is not present in LLCs, CHAs will ask the IMC to fetch the line from memory and send it to Core. To be noticed is that the line is directly sent to Core, when LLC is non-inclusive.

• **T4: LLC to IMC.** When LLC is full, to accept new cache line insertion, it will evict the least recently used cache line to the IMC.

• **T5: Core to Core.** Core can access a cache line in the private cache of Core when they share memory. L2 will pass the cache line to Core through mesh.

• **T6: LLC to I/O Unit.** Intel CPUs allow I/O devices to directly access LLC and bypass memory for better performance, under Data Direct I/O (DDIO) [16]. In this case, cache lines will be passed between a PCIe stop (stop inside a PCIe tile) and LLC.

• **T7: Other traffic.** It characterizes the mesh traffic undocumented by Intel, which is expected to have a smaller volume than T1-T6.

While different applications exhibit different memory access patterns, we found the applications we are interested in, e.g., RSA, distribute most of the mesh traffic through T1-T3. Below we use RSA as an example. Since it repeatedly accesses the same region of data/code (see Appendix B, which has a while loop), most of the accesses can be served by L1/L2/LLC, scaling down the share of T4 and T6. The implementation of RSA does not use multi-threads, so T5 is also small. On the other hand, we acknowledge there are applications with different patterns, e.g., more traffic on T4 - T6, and we discuss this case in Section 8.

That T1-T3 shares the majority of mesh traffic is an ideal condition for Volcano, because they are directly related to the core occupied by the victim application. Therefore, we can select the attack path based on where the victim core is located and the direction of mesh traffic from/to the core. To make Volcano stealthy, we aim to use the least number of cores to construct the attack paths. A key question here is how the traffic from/to victim’s core is distributed in the 4 directions. We attempt to answer this question based on analyzing the geometry and routing pattern of the evaluated CPU. In Section 6.2, we use a profiling experiment to support our theoretical analysis.

For T1, all LLC slices should have a similar probability to be visited, because the LLC hashing function by Intel strives to achieve this goal [25]. Hence, the traffic volume going out from a core in one direction is proportional to the number of tiles reachable on that direction. According to XY routing, a mesh packet first goes vertically to the row of the target tile. For one vertical direction (north/south), assuming the number of tiles per row is $T$, the number of rows is $R$ and the number of disabled tiles is $D$, the estimated traffic volume $S$ from the victim core will be $S = T \times R - D$. Then the mesh packet goes horizontally at the same row of the target. For one horizontal row (east/west), the traffic volume from a core will be $S = C - D'$, where $C$ and $D'$ are the numbers of columns and disabled cores on the row. Figure 3 left shows an example.

For T2, the distribution of traffic volume is reversed, as the core becomes the receiver. The packet from every tile east/west to the core has to move vertically firstly to the row where the core resides, and then horizontally till reaching the core, so the traffic volume to the core from east/west is $S = T \times C - D$ ($T$ being the number of tiles per column now). The remaining packet flows to the core only vertically, so the volume becomes $S = C - D'$. Figure 3 right shows an example.

For T3, our analysis is different. We assume that the LLC miss rate is $x$. The probability $p$ of a LLC slice being responsible to send a cache line is $(1-x)/n$ where $n$ is the number of cores, as the LLC hashing algorithm gives each slice an equal chance to serve a L2 miss. Then, the pattern of T3 depends on $n$ and $x$. For Xeon Scalable CPUs, $n = 24$. When $x$ is around 4%, $p$ will be a similar value, so the traffic from it would resemble T2. If $x << 4\%$, the traffic from IMC could be ignored. When $x$ is significantly more than 4%, the traffic volume $S$ should be increased proportionally to $x/4\%$, though the ratio between directions is the same as T2.

![Figure 3: Mesh traffic to and from a core. The number inside the arrow show the number of tiles that may receive/send traffic.](image)

When the attacker program is able to learn the core ID, the optimal paths can be selected to increase the chances of bandwidth contention. Appendix F describes the details. However, in the virtualized environment, the core ID cannot be learnt. Yet, our analysis in Section 6.2 shows the impact of lacking such knowledge is moderate. To simulate this situation, during evaluation, we assign a random core ID to the attacker and make the victim core ID oblivious to the attacker.

5.2 Probe based on Cache Eviction

Different from routing a packet on the Internet, in mesh interconnect, a program cannot explicitly sends traffic to the destination, because the CPU chip determines the route. To address this challenge, we adapt the existing methods for constructing evictions sets [43, 70]. An eviction set is a set of memory addresses that are mapped to a cache set and able to evict all lines of the cache set. Because the cache set is set-associative, at least $w$ addresses are needed for an eviction set if a set has $w$ ways. Previous attacks, e.g., Prime+Probe, use an eviction set to evict lines of the private caches in the victim core. Though Volcano uses eviction set, our goal is not to evict victim addresses. To the contrary, Volcano evicts lines of its own private L2 cache, in order to generate mesh traffic of T1-T3 flowing to a designated LLC slice on the selected path. As such, Volcano stays out of the protection realm of any existing defenses (see Section 2.3). In Figure 4, we illustrate the concept of our probe.

**Constructing Eviction Set.** We use the approach described as follows to construct an eviction set. Firstly, the attacker prepares a
set of memory addresses (denoted as \( EV \)) that are mapped to one L2 cache set. The number of addresses (denoted as \( n \)) in \( EV \) is set to be larger than the number of ways (denoted as \( w \)) a L2 set has (i.e., \( n > w \)), therefore when requesting addresses of \( EV \), L2 cache misses always happen after \( w \) requests. From \( w + 1 \) to \( n \) requests, each time a line is evicted from L2 to LLC, and a new line from memory will be inserted to L2. After that, when requesting \( EV \) again, \( n \) lines will be evicted from L2 to LLC, and \( n \) lines will be passed from LLC to L2 in return, resulting in stable bi-directional mesh traffic on the attack path.

\textsc{Volcano} needs to force all L2 misses to be served by one LLC slice. Thus, \( EV \) is not only mapped to a set of L2, but also a set of a LLC slice. To find addresses for such \( EV \), we use the two routines proposed in [70], \texttt{check\_conflict} and \texttt{find\_EV}, which are designed for non-inclusive LLC. In essence, \texttt{check\_conflict} tries to test if removing an address of a set makes cache conflict disappear. \texttt{find\_EV} tries to utilize \texttt{check\_conflict} to filter out a set of addresses that are all mapped to the same LLC slice. In Appendix C, we describe them in detail. To also force \( EV \) mapping to only one L2 set, we split the \( EV \) into \( EV_0 \) and \( EV_1 \) of equal size, and set the 16th bit different (0 and 1). As shown in Figure 7, bits 15:6 of a memory address points to a L2 set, while bits 16:6 points to a LLC slice set. As such, \( EV_0 \), \( EV_1 \), and their union \( EV \) are associated with a single L2 cache set.

Even when all cache lines fall into one LLC set, the attacker cannot decide which LLC slice serves the \( Core_r \). Yet, though as shown in Figure 7, there is a hash function mapping a memory address to a LLC slice ID, the hash function is not disclosed, and the difficulty of reverse engineering is tremendous [70]. Instead of recovering the hash function, [70] suggests testing an \( EV \) (multiple \( EV \) have been constructed as candidates) to see if it co-locates with \( Core_r \). We let the attacker enumerate every core on her own CPU, and measure its access time to an \( EV \). When the serving LLC slice is local to the core, the access latency is the lowest, and we link \( EV \) to the LLC slice ID.

Finally, the size of \( EV \) (\( n \)) has to be tuned carefully by the attacker. Not only \( n \) should be larger than \( w \) to force L2 misses, it should also avoid being too large to overflow LLC and L2 together. Otherwise, a line will be evicted from LLC to memory (T4), a request that takes much longer time to respond than T1-T3, reducing the probing frequency. As the Xeon Scalable Professors use 11-way LLC set and 16-way L2 set [31], we varied \( n \) of \( EV \) from 18 to 38 (\( 2^{11} + 16 \)), and found when \( n \) equals to 24 (\( EV_0 \) and \( EV_1 \) each has 12 addresses), the mesh traffic generated within an interval is the highest.

### Measuring Mesh Traffic

When the victim application is running, the attacker sequentially visits every address within \( EV \) immediately after receiving the response to the prior request, and records the timestamp of each request (e.g., using the instruction RDTPSC to read the CPU counter). The interval between consecutive requests reflects the cache latency. When the interval is increased, the victim is supposed to have cache transactions concurrently. The attacker repeatedly visits the \( EV \) for \( x \) times (we set \( x \) to 20 during the experiment) to obtain a sample for an interval, and analyzes the interval sequence to infer the access patterns of the victim applications (detailed in Section 6).

### Using Huge Page

Huge pages are used to find \( EV \) easier. A recent work [64] proposes to construct eviction sets without huge page, which may help us relax the huge page requirement.

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**Algorithm 1:** The pseudo-code of \textsc{Volcano} probe

```plaintext
//Start attack;
set_affinity(best_path.src);
while True do
    for i in range(20) do
        access(EV);
    end
    IntervalSeq.append(access_time);
end
```

5.3 **The Pseudo-code**

Here we summarize all steps covered in this section and show them in Algorithm 1. To notice, the process of \( EV \) generation is adapted from [70], by setting the size of the set of candidate \( EV \) (\( EVs \)) three times as the number of LLC slices, in order to increase the chance of getting an \( EV \) for a designated LLC slice. We verified the generated \( EV \) indeed belongs to the same cache set and LLC slice with the help of PMU.
6 ANALYSIS OF THE VOLCANO SIDE-CHANNEL

In this section, we provide quantitative analysis about the assumptions made in the previous sections. We first assess whether mesh congestion introduces measurable delays. Then, we analyze the impact of core locations on the attack program. Finally, we assess the capacity of the proposed side-channel.

6.1 Impact of Mesh Congestion

The key assumption that VOLCANO can succeed is that the probe delay increases when the mesh is congested. We try to validate this assumption and uncover the root cause with an experiment.

**Settings.** We emulate a victim by using a process to access memory and an attack program to access the same data. We measure the probe delay at different locations and under different conditions.

**PMU event comparison.** Table 3 lists the PMU events that are changed most rapidly.

| Events | w/o victim | w/ victim |
|--------|------------|-----------|
| HORZ_RING_AD_IN_USE | 1004151 | 822149631 |
| HORZ_RING_AK_IN_USE | 1952646432 | 2530753880 |
| HORZ_RING_BL_IN_USE | 3914059524 | 4665246823 |
| HORZ_RING_IV_IN_USE | 35639 | 102218 |
| TxR_HORZ_OCCUPANCY | 4414430426 | 5346595687 |
| AG1_BL_CRD_OCCUPANCY | 60996 | 482979 |
| RxR_OCCUPANCY | 4690 | 141706754 |
| STALL_NO_TxR_HORZ_CRD_BL_AG1 | 350 | 5005 |
| RxR_BUSY_STARVED | 9227 | 41261801 |
| RxR_CRD_STARVED | 2041 | 65177026 |
| TxR_HORZ_STARVED | 6942 |
| TxR_HORZ_NACK | 38951 | 188482 |
| TxR_VERT_NACK | 2 | 19405478 |

Table 3: PMU events that are changed most rapidly.

6.2 Impact of Tile Location

In Section 5.1, our theoretical analysis shows T1-T3 take the major share of mesh traffic, and we attempt to verify it here. In the virtualized setting like cloud, the physical core ID is invisible to attackers. In this case, the attacker is unable to select the best path, even when the attacker knows the model and layout of the CPU. Below we show though information leakage is less acute, it is still significant under VOLCANO.

**Settings.** We use Signal to Noise Ratio (SNR) of the square-wave alike interval sequence to quantify the information gain of the VOLCANO channel. To learn SNR, we first convert the interval sequence from the time domain into frequency domain with a simple Fast Fourier Transform (FFT). We denote the magnitude value at the square wave frequency (i.e., 5kHz) as signal strength and the average magnitude at other frequencies as noise strength. SNR is their ratio. We fix the victim to tile 9 and assign the attacker to each other tile to obtain its SNR.

**Results.** We consider the max and median SNR over all paths for each attacker tile. Table 4 shows our results. Tile 14 yields the best SNR, which aligns with the analysis of Section 5.1. Specifically, T2 should be the major traffic source, as the right side of the victim tile has the most tiles, and tile 14 indeed carries most of the traffic. For other tiles, the SNR values are sufficient for recovering 1 bit, suggesting VOLCANO is potentially effective even when the key path cannot be selected. In Section 7.3, we evaluate this hypothesis.

6.3 Covert Channel Throughput

Transient execution attacks [36, 41, 60] turned cache side-channel to covert channel for information exfiltration. Similarly, our stateless side channel could be re-purposed as a covert channel, and we are interested in its throughput. Hence, we construct a sender and the pseudo-code is shown in Appendix E. In essence, it repeats the pseudo-code is shown in Appendix E. In essence, it repeats the process of accessing an EV for \( \frac{T}{i} \) (turn on the mesh traffic) and then running NOP loops for \( \frac{T}{i} \) (turn off the mesh traffic), assuming \( T \) is the execution time. The receiver program runs the VOLCANO probe to collect a sequence of intervals and decodes the patterns.

We run the experiment with different \( T \), and Figure 5 shows the interval sequence observed by the receiver, for a period of around 100us. When \( T \) is 30us and 5us, we expect around 3 and 20 peaks to be observed, and the interval sequence proves it. However, when \( T \) drops to 2us, we are unable to identify 50 peaks. As such, we conclude the channel capacity is around 200 kbps (one bit per 5 us).
It also means that if a victim program accesses memory (including cache) at the latency of less than 5us, the attacker program cannot decode its access pattern.

7 ATTACKING RSA

In this section, we evaluate the step 3 (Secret Inference) described in Section 3.4. We choose two Java RSA implementations as the target, one is known vulnerable to the conventional timing side-channel attacks, and another is hardened with sliding window. We first describe the platform for the attack evaluation. Then, we elaborate the attack results and our findings.

| UPI | PCIE | PCIE | RLINK | UPI2 | PCIE |
|-----|------|------|-------|------|------|
| 0   | 22.79| 21.03| 10.30 | 11.74| 11.92|
|     | 9.74 | 10.30| 11.74 | 11.92| 10.24|
| IMC0| 21.82| 11.63| 11.30 | 9.60 | 7.31 |
|     | 1.5  | 10.30| 11.30 | 9.60 | 7.31 |
| 1   | 15.60| 16.92| 17.17 | 17.17| 18   |
|     | 9.52 | 11.77| 11.77 | 11.77| 10.37|

Table 4: Layout of Xeon Scalable 8260 CPU with the measured SNR. Numbers in every core die represents the Tile ID, maximum and median SNR values respectively.

Figure 5: Interval sequence collected by the receiver of different T. The x-axis is the running period of the sender. The three sequences have the same number of sample points.

7.1 Experiment Settings

Table 5 shows the hardware and software specification of our experiment platform. The CPU belongs to the latest generation Intel CPU, i.e., Cascade Lake-SP, which can be purchased from retailers. The layout of the CPU has already been reverse-engineered by us, showing in Table 2.

To validate our claim that Volcano bypasses cache partition, we turn on Intel CAT for the entire experiment duration. This is the same setting as the recent advanced cache attacks like Xlate [61]. We did not enforce the stronger protection, temporal isolation [13], because it builds on seL4. However, as Volcano is based on the stateless channel, which admittedly is out of the mitigation scope [13], we expect Volcano is effective. For Intel CAT, we create two COS. The core running the victim program is bond with COS 1, while other cores are bond with COS 2, by using the command `pqos cat set COS`. We evaluate Volcano against Java programs because Java yields more distinguishable patterns of mesh traffic, comparing to other languages without automated memory management, like C++. Java Virtual Machine (JVM) creates a new object for the same variable references two different objects before and after its execution. The allocation of the second object causes cache misses, which introduces more memory read/write over mesh interconnect. In contrast, in languages like C, the developer may reuse the object to save memory, in which case the memory access may be completed within the private cache of the core.

We assume a 2048-bit private key is used. The private key consists of an exponent d and a modulus n. The message to be encrypted is segmented into 2048-bit groups (m). Therefore, d, m, and n are all 2048 bits. The attacker aims to infer the bit sequence of d.

7.2 Attacking Fast Modular Exponentiation

We implemented the basic fast modular exponentiation (Algorithm 2) in Java following the code found in [5]. As described in Section 3.2, different key bit leads to different memory access patterns. This algorithm is also implemented in GnuPG 1.4.13, which is evaluated by other cache side-channel attacks (e.g., [70]). We tested 100 different keys with this RSA program as victim, and for each key, we let the program run 20 times. Hence, there are in total 2,000 traces collected by the Volcano probe.
Selection of Key Path. We simulate the non-virtualized setting here, of which the attacker learns the core ID. We assume the victim program runs in a core randomly assigned by the OS and the attacker can select a core among the rest to construct key paths. In Section 7.3, we simulate the virtualized setting, and obscure the core ID.

According to Section 5.1, the attacker can estimate the traffic reaching/leaving the victim core. Though the attacker has the freedom to select multiple paths based on the estimation, we found one vertical path is sufficient to collect clear-enough signals about the victim RSA program. Therefore, we select the top-ranked vertical path and place the attacker program to one end of the path.

Analyzing the Interval Sequence. Figure 6a shows the interval sequence mapped to the first 8 bits of a $d$, which is 01001010. Differentiating bit 0 and 1 turns out to be more challenging than the stateful cache attacks, because their probe tracks the cache access of each function (e.g., $\text{sqr}$ and $\text{mul}$ [70]), while VOLCANO works at the granularity of a program. Yet, with the heuristics described below, bit 0 and 1 can be differentiated.

Figure 6: (a) The raw interval sequence collected by attacker’s probe. (b) The sequence after filtering. (c) The sequence after smoothing, with circles and stars representing the starting time of bit 0 and 1. The key stream is 01001010. The max value of y-axis of (c) reduces to 1.5k because smoothing averages the values in a window.

Specifically, when 0 is encountered, a sharp rise will be observed, which we call A rise. When 1 is encountered, A rise will be observed first, followed by one or two smoother rises, which we call B rise. Besides, it takes longer time to process a bit 1 than bit 0.

As A rise is more discernible than B rise and other irrelevant data points, we use a threshold (2900, 4200) to keep A rises first. Figure 6b shows the data points after filtering. After then, the data points are smoothed, i.e., taking the average of the points in a window, so B rises are expected to be diminished and A rises become more distinguishable, as shown in Figure 6c. With the smoothed sequence, the attacker starts to find the peaks over 600 cycles, which are expected to be A rises. Then, she examines the peaks in the execution time window of bit 0 and 1 close to a A rise respectively. The window with a higher peak indicates which bit it is.

Results. For each key used by the victim program, we compute the edit distances between all the inferred keys with the ground truth, and take the smallest value. Table 6 row “Smoothed” shows the distribution of the edit distances. Out of the 100 keys, for 17 keys the edit distances are at most 10, 84 (17+67) are at most 50. We look into the 84 keys, and compute the average edit distance and two other metrics: the longest common sub-string (LCSStr) and the longest common sub-sequence (LCSSeq). The result suggests a large portion of the key has been inferred. For instance, the average LCSStr is 760.6, meaning that a chunk of 760 consecutive bits can be precisely recovered.

Moreover, we found the inference accuracy can be enhanced with error-correction techniques. We chose De Bruijn graph [39], a technique widely used to correct gene sequence errors, for this task. In essence, for a group of long sequences, it breaks each one to subsequences and drops the less frequent ones. Then it concatenates the remaining sub-sequences back to a complete sequence.

With the De Bruijn graph, for a group of 20 inferred keys, we can correct the errors and generate 1 key. We compare each generated key to the ground truth, and the row “Corrected” of Table 6 shows the result. This time, 47 inferred keys have an edit distance less than 10, and we further compute the average edit distance, LCSStr, and LCSSeq for them. It turns out the average LCSStr can be as high as 2040, meaning that only 8 bits are incorrectly predicted.

Since LCSStr is highly close to LCSSeq in this case, the errors are expected to be distributed in the head and tail of the key stream. To recover the exact key, the attacker only needs to enumerate $9 \times 2^8$ combinations of bits.

7.3 Attacking Sliding Window RSA

Fast Modular Exponentiation was known to be vulnerable to timing side-channel attacks. To defeat timing attacks, the recent RSA implementations have been upgraded to use the Sliding Window algorithm, which decouples key stream from $\text{mul}$/sqr execution sequence. For example, the Crypto suite of JDK (i.e., javax.crypto.Cipher) uses Sliding Window, and GnuPG has adopted Sliding Window after version 1.4.13.
However, a recent work [3] showed that mul/sqr execution sequence can still be utilized to crack RSA that is based on Sliding Window. Given a mul/sqr sequence, their algorithm (Sliding right into disaster, or SRID for short) is able to either output the 100% correct inference for a key bit (i.e., either 0 or 1), or output X, meaning the algorithm is unable to get a correct inference. With SRID to crack 2048-bit RSA key, 5-bit sliding window RSA implementation leaks 33% of the key bits. JDK uses 7-bit sliding window, in which case around 30% bits is expected to be recovered theoretically.

Volcano can make full use of SRID to recover key bits. The attacker needs only firstly recover mul/sqr sequence with the similar approach as Section 7.2, then SRID is applied to output 0, 1 and x.

**Settings.** We tested the official JDK implementation of RSA (javax. crypto.Cipher) as the victim, and placed the program in a fixed tile. At the same time, we place probes at random positions to collect interval sequences and infer keys, simulating virtualized setting where the attacker cannot use core ID to select the key path. The experiments were repeated 1000 times.

We aim to recover mul/sqr from the interval sequence, which is different from the analysis described in Section 7.2 because three new patterns have been observed, and none of them overlap with A and B rises. In Appendix G, we elaborate how to map them to mul/sqr sequences.

**Results.** Among all these 1000 traces, 32 exhibit obvious patterns, and mul/sqr were recovered without error. Assuming the victim repeatedly runs RSA and the attacker keeps profiling mesh traffic, it will take on average 31 (1000/32) rounds to get a perfect mul/sqr sequence. Then, we implemented the SRID algorithm and tested on the 32 mul/sqr sequences. In average, 31.05% key bits can be inferred. A recent work [48] also pointed out that the SRID algorithm has room to be improved for a better recovery ratio. Therefore, we believe more key bits can be recovered pending on the new algorithms.

8 DISCUSSION

**Limitations.** 1) Volcano attempts to congest T1-T3 traffic, but T4-T7 may also leak sensitive information about the victim application. For example, I/O intensive applications could introduce prominent mesh traffic between PCIe stop and LLC slices. We plan to test such applications in the future. 2) Volcano bypasses the existing defenses at the cost of obtaining coarser-grained information about cache activities. In stateful cache attacks like Prime+Probe, the attacker can precisely evict a cache set shared with a victim and then learn the which memory address/range accessed by the victim. However, Volcano only tells when the victim accesses memory/cache. As such, we choose the Java-based RSA implementations which leak more information. 3) Our evaluation is done on a single Xeon Scalable CPU. In the future, we plan to test other Intel CPUs and the ARM server CPU Neoverse [15].

**Implications of Volcano.** The key take-away message from our study is that the cache side-channel attack can be done without changing the microarchitectural state through the stateless interconnect. This is counter-intuitive at first sight, but the new interconnect design intertwines the cache lines on the move from different applications, introducing new types of resource contention that enables our attack.

To prevent the interconnect from leaking an application’s status, the cache traffic could be regulated under the non-interference property [17]. Previous works verified the code of programs to detect the vulnerable ones that violate this property [8], but doing so on the interconnect traffic has to model the highly complex microarchitecture. Like cache partition, if interconnect bandwidth can be partitioned, Volcano might be thwarted. However, as mentioned in [13], “no support for bandwidth partition exists on contemporary mainstream hardware”. Though Intel recently proposed a technique named Memory Bandwidth Allocation (MBA) [29], which limits the bandwidth a core can issue to memory. The limit is an approximation and insufficient for threat mitigation [13].

**Potential Defenses.** Instead of strong mitigation based on the non-interference property or partition, we believe mechanisms that increase the attack difficulty is more likely to be adopted. We discuss a few directions that might lead to a successful defense.

One important prerequisite of Volcano is that when a mesh stop is congested, the packets through it would not be detoured. Under the simple YX routing, the routes between two tiles are fixed, easily satisfying the attack prerequisite. Horro et al. [25] explored dynamic routing to optimize the coherence traffic. Though their goal is to reduce the access latency, it has the potential to break the attack prerequisite.

Volcano mainly targets the cross-tile T1-T3 traffic related to LLC. Intel CAT allocates different cache ways to different applications to implement cache isolation, but it does not partition the cross-tile LLC accesses. If cache partition can be done at the level of LLC slice, e.g., placing the data frequently accessed by an application to the LLC slice local to its occupied cores, Volcano might be deterred. Farshin et al. [12] designed a slice-aware memory management mechanism and showed it can realize cache partition, which holds promises. On the other hand, such a mechanism does not prevent attackers who exploit T4-T7, e.g., the traffic associated with IMC. Hence, a new memory management mechanism might still be needed.

Cache randomization is another potential direction. By forcing the mapping between physical addresses and cache set index, dynamic and unpredictable, finding the right eviction sets is expected to be more difficult, which could make the probe of Volcano unstable. However, recent studies [6, 50, 52] have shown the state-of-the-art approaches like CEASAR-S [51] and ScatterCache [68] are broken under new attack methods. Though Song et al. proposed a fix to address the new attacks [52], the defense is demonstrated on a RISC-V simulator. When the commercial processors adopt such defenses is yet unknown.

9 CONCLUSION

In this work, we reveal stateless cache side-channel, or Volcano, that can leak memory access patterns of a victim program, by exploiting the traffic contention on the CPU mesh interconnect. The side-channel is different from previous cache side-channels, in that it does not rely on stateful micro-architectural state changes made by the victim. Therefore it can bypass both spatial and temporal isolation. To reveal the consequences of Volcano, we conducted an analysis on RSA implementations to infer the private key from the collected delay sequences. The results show that Volcano is
very effective. We believe mesh interconnect opens up new opportunities for security research, and its implications should be further examined.

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A INTEL SKYLAKE-SP CACHE SPEC

We introduce the cache specification of Intel Xeon Scalable family processors, which we used as our platform.

Address Mapping. The lowest 6 bits reflect the block offset within a cache line. The bits in the middle indicate the index of the cache set containing the line (bits 15:6 for L2 and 16:6 for LLC). The upper bits form a cache tag, which indicate whether the data is in the cache.

As LLC requests are all managed by CHA inside a core, for a LLC access, CPU has to decide which CHA to talk to. The decision is based on a proprietary hash function which is not fully reverse-engineered yet [70].

Cache Structure. For Skylake-SP processors, LLC is designed as non-inclusive to the private caches. Before Skylake-SP processors, LLC is inclusive, meaning that a cache line in L2 cache has a replicate in LLC. For non-inclusive LLC, a L2 cache line may or may not have replicate in LLC, which is determined by the cache eviction policy. As a result, Xeon scalable CPUs have much larger effective cache size (the sum of L2 and LLC) compared to the previous generations (LLC only).

| Offset | L2 Tag | L2 set index | LLC Tag | LLC set index | Hash to LLC slice ID |
|--------|--------|--------------|--------|--------------|---------------------|
| 63:17  | 16     | 15:6         | 5:0    |              |                     |

Figure 7: Mapping between memory address (physical) and cache.
Table 7: Cache configuration for Skylake-SP, Cascade Lake-SP and Cooper Lake-SP CPU families [59]. L1-I and L1-D are for instruction and data separately.

|       | Size   | Associative | Set |
|-------|--------|-------------|-----|
| L1-I  | 32KB   | 8-way       | 64  |
| L1-D  | 32KB   | 8-way       | 64  |
| L2    | 1 MB   | 16-way      | 1024|
| LLC slice | 1.375MB | 11-way      | 2048|

Table 8: The disabled tiles of Xeon Scalable 8175 CPU. Gray cell indicates the tile is disabled, including its core, CHA, SF and LLC. The number in each cell is the ID of tile. The tiles without numbers like “UPI” do not have cores.

| UPI | PCIE | PCIE | PCIE | PCIE | UPI | PCIE |
|-----|------|------|------|------|-----|------|
| 0   | 4    | 9    | 14   | 19   | 24  |
| IMC0| 5    | 10   | 15   | 20   | IMC1|
| 1   | 6    | 11   | 16   | 21   | 25  |
| 2   | 7    | 12   | 17   | 22   | 26  |
| 3   | 8    | 13   | 18   | 23   | 27  |

Table 9: Layout of Xeon Scalable 8175 CPU. Gray cell indicates the tile is disabled. The two numbers in each cell indicates the ID of CHA and core respectively.

| UPI | PCIE | PCIE | PCIE | UPI | PCIE |
|-----|------|------|------|-----|------|
| 0   | 4    | 7    | 19   | 12  | 3    |
| IMC0| 3    | 18   | 12   | 15  | 10   |
| 1   | 4    | 9    | 14   | 19  | IMC1|
| 2   | 6    | 7    | 11   | 20  | 5    |
| 3   | 5    | 13   | 10   | 23  | 27  |

Algorithm 2: Fast modular exponentiation algorithm

Input: \( m, d, n \)

Output: \( res := m^d \mod n \)

\[ res = 1; \]

while \( d > 0 \) do

if \( d \mod 2 \neq 0 \) then

\[ res = (res \times m) \mod n \]

end

\[ d = d >> 1; \]

\[ m = m^2 \mod n \]

end

B FAST MODULAR EXPONENTIATION ALGORITHM

The pseudo-code of RSA’s fast modular exponentiation algorithm is shown in Algorithm 2.

C CHECK_CONFLICT AND FIND_EV

According to [43, 70], The check_conflict function checks if an address \( x \) conflicts with a set of addresses \( U \), by checking if \( x \) is evicted when traversing \( x \) followed by \( U \). If \( x \) is evicted by \( U \), it indicates \( U \) conflicts with \( x \), otherwise, it does not. [70] adapted this function to CPUs with non-inclusive LLC, by pushing all lines in a L2 set to LLC before measuring accessing time of \( x \), which reduces false positives and negatives.

According to [70], the find_ev function tries to find a minimal \( EV \) within a given set of addresses \( CS \). It starts by randomly picking out an address \( x \) from \( CS \) and assigning the rest addresses in \( CS' \). It then repeatedly deletes addresses from \( CS' \) except those addresses making \( CS' \) no longer conflict with \( x \). Those addresses should be in the \( EV \). \( EV \) could be further extended by picking out those addresses in \( CS \) but conflict with \( EV \).

D LAYOUT OF XEON SCALABLE 8175

Table 8 and 9 show the reverse-engineered layout of Xeon Scalable 8175.

E PSUEDO-CODE OF COVERT CHANNEL

Algorithm 3 shows the pseudo-code of the covert-channel sender.
Algorithm 3: The sender program used to test channel capacity

```python
Input: T, bits, EV
for bit in bits do
    ts = time();
    if \( bit = t \) then
        while \( time() \leq ts + \frac{T}{2} \) do
            access(EV);
        end
    else
        while \( time() \leq ts + \frac{T}{2} \) do
            NOP;
        end
    end
end
```

**F SELECTION OF THE KEY PATH**

If the attacker program does not run in the virtualized environment, it can learn the core ID of the victim, and select the key path. Assuming the attack is running on Linux, the attacker can query a file `/proc/PID/stat` to obtain the process ID of the victim’s program, and uses `ps -o pslr` with the process ID as input [53], to learn the core ID. The file and command are open to non-root users. After that, the attacker maps the ID to the inferred CPU layout, compute \( S \) of the four directions for T1-T3, and sends the probe packets. Here we give an example about how to choose an attack path. Assume the victim is running at (5, 13) of Table 9, the attacker can bind a thread to core 8 (10, 8) and then probe CHA 23 (23, 23). In this case, \( \frac{18}{23} \) of the mesh traffic sent to the victim core is supposed to contend with the attacker’s traffic (the east and west traffic share bandwidth). To increase the probabilities of contention, the attacker could occupy multiple cores and probe multiple CHAs. For example, she can also occupy core 21 (15, 21) and access CHA 22 (22, 11) at the same time. Yet, our evaluations suggest one path is enough.

**G ANALYZING THE SEQUENCE OF SLIDING WINDOW RSA**

Figure 9 shows three different patterns. For Pattern A, each `mul` incurs an obvious rise, while for pattern C, each `mul` incurs a discernable pit. For pattern B, each `sqr` incurs a rise. Take pattern C as an example, the attacker needs only firstly deduce the positions of `muls`, then can she know how many `sqr`s are there between consecutive `muls`, according to the interval between consecutive `muls`.

The method of processing the patterns is similar to that in Section 7.2, i.e., clipping first and then smoothing. But each pattern requires customized parameters. We adjusted three different parameters to handle them respectively. We firstly check if the pattern is obvious enough and then identify which category an observation falls into. Then we use sequence recovery with corresponding parameters accordingly.