High-Level Synthesis for Packet-Processing Pipelines

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ABSTRACT

Compiling high-level programs to target high-speed packet-processing pipelines is a challenging combinatorial optimization problem. The compiler must configure the pipeline’s resources to match the high-level semantics of the program, while packing all of the program’s computation into the pipeline’s limited resources. State of the art approaches tackle individual aspects of this problem. Yet, they miss opportunities to efficiently produce globally high-quality outcomes.

We argue that High-Level Synthesis (HLS), previously applied to ASIC/FPGA design, is the right framework to decompose the compilation problem for pipelines into smaller pieces with modular solutions. We design an HLS-based compiler that works in three phases. Transformation rewrites programs to use more abundant pipeline resources, avoiding scarce ones. Synthesis breaks complex transactional code into configurations of pipelined compute units. Allocation maps the program’s compute and memory to the hardware resources.

We prototype these ideas in a compiler, CaT, which targets the Tofino pipeline and a cycle-accurate simulator of a Verilog hardware model of an RMT pipeline. CaT can handle programs that existing compilers cannot currently run on pipelines, generating code faster than existing compilers, while using fewer pipeline resources.

1 INTRODUCTION

Reconfigurable packet-processing pipelines (RMT [22]) are emerging as important programmable platforms, found in high-speed network switches and network interface cards (NICs). Examples include the Tofino [8], Trident [4], Jericho switches [3], the Pensando [1], and Intel IPU NICs [7].

Programmable pipelines are organized into multiple stages, where each stage processes one packet in parallel, and hands it off to the next stage (§2.1). Each stage contains memory blocks to hold tables containing packet-matching rules and state (e.g., counters) maintained across packets. Header fields are extracted from packets to match the table rules. Once the packet’s fields are matched against a rule, the packet or state can also be updated using an action.

P4 [11] is emerging as a popular language to program these pipelines. P4 offers the ability to parse packets according to custom header definitions, and specify the match types and actions on parsed packets. A P4 action may modify packet header fields and state.

The Compilation Problem. The community has developed P4 solutions targeting programmable pipelines for many use cases, such as in-network computation [33], monitoring [19], load balancing [40], and security [39]. A compiler translating P4 programs to high-speed pipelines must solve a hard combinatorial optimization problem with several aspects:

1) Resource balance: There are multiple pipeline resources, with some resources being scarce (stages, gateways, etc.) and others being abundant (ALUs). Some resources must be allocated hand in hand (e.g., match memory and ALUs).

2) Semantics preservation: P4 actions are transactional [13], executing to completion on each packet before processing the next one. If a user wishes to perform an algorithmic action on packet data that requires multiple stages, the compiler must be able to split the action into multiple ALUs and stages, ensuring the implementation respects the transactional semantics of the computation [44].

3) All-or-nothing fit: A program targeting a high-speed pipeline will either run at the full pipeline rate, or cannot run at all. It is paramount to “pack” all of the P4 program into the pipeline’s limited resources.

Prior work has tackled several individual aspects of this compilation problem (§2.2). A piecemeal approach loses opportunities to globally reduce resource usage (e.g., stages), which is necessary to fit complex programs on the pipeline. However, it is intractable to solve a single combinatorial optimization problem. Our goal is to find the right decomposition of the large problem into smaller pieces, enabling global optimization of resource use with modular solution to each piece.

Our Approach. In this paper, we present an end-to-end compiler, CaT, that unifies prior approaches and translates high-level P4 programs into a low-level representation suitable for hardware execution. Our main idea is to adapt high-level synthesis (HLS)—a technology for improving productivity of hardware design for ASICs [12] and FPGAs [6]—to the domain of packet-processing pipelines.

Informally, HLS [24] takes as input a high-level algorithmic description of the hardware design with no reference to clocks or pipelining, and with limited parallelism in the description. An HLS compiler then progressively lowers this high-level description down to an optimized hardware implementation, pipelining the implementation if possible, executing multiple computations in parallel, and mapping computations down to a register-transfer level (RTL) design.
We believe that adapting HLS for compilers targeting packet-processing pipelines will raise the user’s level of programming abstraction, while retaining the performance of low-level pipeline programming. For a user developing algorithmic programs in P4 (such as those used for in-network computation, e.g., [33, 42, 52]), HLS techniques eliminate the labor of manually breaking the high-level algorithmic computation into actions spread over many pipeline stages (§2.3). At the same time, HLS techniques offer many distinct advantages for targeting packet-processing pipelines (§2.3).

The workflow of our compiler, CaT, is shown in Figure 1. It consists of three phases that roughly mirror a traditional HLS compiler. The input consists of P4 code that contains tables with matches and action code blocks manipulating packet headers and state. The action code blocks may be written without regard to its feasibility in a single pipeline stage. The first phase of CaT employs resource transformations that rewrite a high-level P4 program to another semantically-equivalent high-level P4 program; these rewrites are used to transform a computation’s use of one scarce resource to its use of a relatively abundant resource, and potentially reduce the number of stages as well. The second phase performs resource synthesis to lower transactional blocks of statements in the high-level P4 program to a lower-level program suitable for hardware execution. In this step, individual ALUs in hardware are configured to realize the programmers’ intent in the transactional action blocks, while respecting their computational capabilities. The third phase performs resource allocation to allocate the computation units corresponding to the lowered program to physical resources such as ALUs and memory in the pipeline. Notably, our HLS workflow works within the confines of the widely used P4 ecosystem without requiring the development of a new DSL for packet processing.

Our Contributions. The main technical contribution of CaT’s three-phase approach is the modularization of the large combinatorial optimization problem of compilation into smaller problems, whose solutions still enable a high-quality global result (§3). Additionally, we improve upon the state of the art and introduce new techniques in each phase. In particular, our resource transformations (§3.1) are driven by a novel guarded dependency analysis that identifies false dependencies, thereby exposing more parallelism opportunities when performing rewrites. Our resource synthesis phase (§3.2) uses a novel synthesis procedure that quickly finds pipelined solutions with good-quality results for complex actions. It separates out stateful updates from stateless updates, to decompose a large program synthesis problem into smaller and more tractable subproblems. Stateless code is synthesized into a minimum-depth computation tree, i.e., with the minimum number of stages. In comparison to prior work [29], this new synthesis algorithm allows CaT to handle many large actions, in a much shorter time, and with far fewer computational resources needed for compilation. Finally, our resource allocation phase (§3.3) uses a constraint-based formulation that extends prior work [34] to handle complex multi-stage transactional actions. Our techniques can support general P4 programs (including @atomic constructs) efficiently, including programs translated into P4 from higher-level domain-specific languages developed for pipeline programming [28, 29, 32, 44, 47].

Our prototype of CaT can target: (1) the Tofino pipeline, and (2) an open-source RMT pipeline called Menshen (that was implemented into an FPGA) [9, 51]. Existing commercial switches have proprietary instruction sets that preclude the kind of low-level resource allocation and control over ALU configurations implemented by CaT. Therefore, our backend for Tofino [8] generates low-level P4 in lieu of machine code. To evaluate CaT in full generality, we extend Menshen’s open-source register-transfer level (RTL) Verilog model with additional resources for our experiments. We generate code for the cycle-accurate simulator of Menshen, and also use it for testing the CaT prototype. Our results (§4) show that CaT can automatically compile programs that require manual changes to be accepted by the Tofino compiler. On other challenging benchmarks, CaT produces close-to-optimal code and does so about 3 times faster (on average) than prior work [29].

2 BACKGROUND AND RELATED WORK

2.1 Packet-Processing Pipelines

The compiler target in this paper is a programmable packet-processing pipeline following the Reconfigurable Match-Action Tables (RMT) architecture [22]. Such pipelines are present in commercially available programmable switches such as the Barefoot Tofino [8], Broadcom Trident, and Mellanox Spectrum, and NICs such as the Pensando DPU. An RMT-style pipeline consists of (i) a programmable packet parser, (ii) a number of processing stages structured around match-action computation. We describe these components briefly below.

A programmable parser takes in a user-specified parsing grammar, and extracts packet header fields. These set of fields, termed the packet header vector, are permitted to be both read and written in each pipeline stage. One match-action stage
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extracts relevant fields from the PHVs using a crossbar circuit. The fields are then matched against user-inserted rules in stage-local match memory. The memory may also contain state, i.e., values maintained on the switch and updated by every packet, such as a packet counter. Once a packet matches a rule, a corresponding set of actions is invoked. The actions are implemented using Very Long Instruction Word (VLIW) ALUs which may modify multiple PHV fields in one shot. Some match-action tables may be skipped entirely (e.g., due to control flow) through circuit components called gateways.

Two factors limit the available resources and expressiveness of packet-processing pipelines. First, to support high throughput (e.g., 6 Tbit/s in Tofino), pipelines are clocked at high frequencies (e.g., 1 GHz for Tofino). Second, the pipeline must admit a new packet every clock cycle. Hence, stateful computations (read-modify-write) must finish in one clock cycle. Further, stage-local memories are limited in density and size, to support fast lookup. Finally, constraints on chip area and power limit the number of pipeline stages (e.g., 12 match-action stages in Tofino) and control circuitry (e.g., number of gateways and crossbars).

Such exacting hardware constraints would challenge any compiler. Program behavior is all-or-nothing: a program that fits into the pipeline resources would run at clock rate, otherwise it simply cannot be run. There is no graceful degradation between these extremes.

2.2 Related Work

There has been significant interest in developing compilers and domain-specific languages (DSLs) for packet-processing pipelines. We categorize the existing compiler efforts based on their support for: program rewriting, code generation, and resource allocation.

**DSLs for programming packet pipelines.** P4 and NPL are the most widely used languages to program packet pipelines. They share many syntactic and semantic aspects. Several academic projects have proposed new DSLs or extensions to P4 to remedy many of P4’s shortcomings. For instance, microP4 [48] adds modularity to P4. Lyra [28] addresses the issue of portability of programs across multiple devices. Lyra and FlightPlan [49] address the problem of partitioning a program automatically across multiple devices. Lucid [47] introduces an event-driven programming model for control applications in the data plane. P4All [32] extends P4 to support ‘elastic’ data structures, whose size can grow and shrink dynamically based on the availability of switch resources. Domino [44] is a DSL that supports transactional packet processing: a programmer specifies a block of code that is executed on each packet in isolation from other packets. These languages can all be translated into P4, and in this paper, we directly take P4 programs as our starting point. This provides opportunities to explore complementary combinations of their techniques. One limitation is that CaT does not currently handle the problem of partitioning a network-wide program into per-device programs, like Lyra and Flightplan. Instead, our goal is to build a high quality compiler that inputs a P4 program for a single device and outputs a high-quality implementation for that device.

**Program rewriting.** The open-source reference P4 compiler [10], which is the foundation for most P4 compilers including the widely-used Tofino compiler [8], employs rewrite rules to turn an input P4 program into successively simpler P4 programs. These rewrite rules consist of classical optimizations like common sub-expression elimination and constant folding. Rewrite rules are also employed by Cetus [38] and Lyra [28] to merge tables in different stages (under certain conditions) into a single “cartesian-product” table in a single stage, thereby saving on the number of stages. CaT uses rewrite rules to transform uses of scarce resources (gateways, stages) to more abundant ones (tables, memory, ALUs).

**Code generation for complex actions.** Domino [44] and Chipmunk [29] tackle the problem of code generation, i.e., selecting the right instructions (that configure ALU opcodes) for a program action expressed in a high-level language. These compilers have to respect the limited capabilities of each stage’s VLIW ALUs while correctly implementing state updates according to @atomic semantics for transactions (§2.1). Domino largely uses rewrite rules and employs program synthesis to code-generate just the stateful fragments in the action, but it may fail on some semantically-equivalent programs. Chipmunk employs program synthesis to exhaustively search for ALU configurations for any semantically-equivalent program, but at the expense of high compile time. Lyra [28] uses predicate blocks, chunks of code predicated by the same path condition, to break up algorithmic code into smaller blocks that have only inter-block (but no intra-block) dependencies. CaT’s resource synthesis is faster than Chipmunk’s and more reliable than Domino’s (Table 4, §4.3). It generalizes Lyra’s predicate block approach by considering ALUs expressed via a parameterizable grammar, such that the procedure is independent of the operations in the program’s source code or intermediate representation.

**Resource allocation.** The problem of allocating specific resources required by a P4 program (e.g., match memory blocks, a specific number of ALUs, etc.) can be posed as an integer linear programming problem (ILP) [32, 34] or as a constraint problem [28] for Satisfiability Modulo Theory (SMT) solvers [18]. If the constraints of the hardware are modeled precisely, ILP-based techniques can improve resource allocation relative to greedy heuristics for resource allocation. CaT’s resource allocation (§3.3) indeed uses a fine-grained constraint-based formulation that models detailed pipeline
resources and enables global optimization by considering dependencies across tables as well as within actions.

2.3 Why HLS?
CaT is an end-to-end compiler for P4-16 programs that takes inspiration from HLS to provide both: (1) a high-level of abstraction for specifying packet-processing functionality, and (2) high quality of the compiler-produced implementation. While prior approaches to HLS for ASICs and FPGAs have sometimes resulted in poor quality of the generated implementation, we believe that the narrower domain of packet-processing pipelines is particularly well-suited for applying HLS more gainfully than has been done before. First, HLS techniques are designed to systematically explore tradeoffs between the functionality (e.g., which ALU can implement an operation?), capacity (e.g., how many ALUs, gateways, etc.?), and scheduling (which stage should run an operation?) of resources—a core challenge in compiling to packet-processing pipelines. Second, HLS techniques can be effective in pipelining code with memory state updates, to enable transactional semantics, an abstraction that provides the illusion that all previous packets have finished their computation over the state. Importantly, an HLS workflow can combine these ideas with code rewrite and program synthesis.

Today, developers write down actions in P4 programs with the assumption that each action must finish in one stage. However, tracking the hardware-level feasibility of an action leads to an unnecessarily low level of abstraction, especially when developing high-speed algorithmic code. Consider the example pseudocode (motivating example ME-1) shown in Figure 2. This function implements the SipHash algorithm, used as a hash function to prevent collision-based flooding attacks [17]. The developer of a P4-version of this algorithm (distinct from the authors of this paper) started with a high-level description of the algorithm (Table 3, [52]). The developer then manually changed it into a pipelined implementation (Table 4, [52]), because the algorithm as expressed cannot be compiled by the Tofino compiler since it cannot be finished in one stage. We argue that a good compiler should automate this. Indeed, CaT can successfully handle this example (discussed in §4.3), without requiring an expert developer to manually pipeline their code.

To produce high quality implementations, CaT combines ideas from several prior projects (Table 1) into an end-to-end system for the first time. The HLS workflow of CaT divides up the process of compiling a P4-16 program into three phases—their correspondence with traditional HLS steps [24] and relation with prior work are highlighted in Table 2. As shown, our resource transformation corresponds to the code transformation step in HLS, our resource synthesis corresponds to operation binding (or module selection [6]) in HLS, and our resource allocation corresponds to the scheduling step in HLS. To further improve the effectiveness of HLS in our setting, we customize these phases to RMT pipelines. Specifically, our resource transformations focus on scarce resources (pipeline stages, gateways). Our resource synthesis procedure leverages the strict requirement that stateful updates must fit in a single stage to ease the task of pipelining, which is often challenging for HLS in general. Our resource allocation phase uses the result of synthesis on action blocks, to pack multiple action blocks in each pipeline stage. Thus, while these phases build on top of well-known prior work including HLS efforts (Column 3), there are significant differences and novelties in our work (Column 4). The last column lists complementary techniques that could be combined in our compiler.

3 COMPILER DESIGN
The general problem of optimal code generation in compilers is known to be NP-complete [14], and most compilers decompose the problem in some way to tradeoff optimality for reasonable performance. In our HLS-based approach, Phases 2 and 3 can be viewed as an action-level modularization of the overall compilation problem, where we perform local resource synthesis for each action block in the P4 program, and then use these results to perform a global resource allocation for all actions blocks. This keeps the synthesis runtime manageable in practice while providing good-quality results on resource usage. Note that we support rich computations in actions that could require multiple stages as well as transactional (@atomic) semantics. In the remainder of the paper, we refer to such rich action-computations as transactions. We now describe the three phases of our compiler in detail.

3.1 Phase 1: Resource Transformation
In the first phase of our compiler, we perform source-to-source rewrites in P4, with the goal of transforming a program that makes use of scarce resources, to one that makes use of more abundant resources. Rewrite rules provide a flexible and general approach for this purpose, and can be easily extended by adding more rules for new backend targets and resources. CaT includes rewrite rules for if-else statements in the control
### Table 1: CaT unifies prior work on program rewriting, code generation, resource allocation, and does so within the context of the P4 language, without needing a new DSL.

| Project            | Program Rewriting | Code Generation | Resource Allocation | Retargetability | Language Constructs |
|--------------------|-------------------|-----------------|---------------------|-----------------|---------------------|
| Domino [44]        | Yes               | No              | X                   | X               | Packet transactions |
| Chipmunk [29]      | No                | Yes             | X                   | X               | Packet transactions |
| Lyra [28]          | Yes               | No              | X                   | X               | Network-wide programs |
| Flightplan [49]    | No                | No              | X                   | X               | Network-wide programs |
| Cetus [38]         | No                | No              | X                   | X               | Elastic data structures |
| P4All [32]         | No                | No              | X                   | X               | Event-driven programming |
| Jose et al. [34]   | No                | No              | X                   | X               | P4’s atomic construct |
| Lucid [47]         | Yes               | No              | X                   | X               | ALU DSL |
| CaT (this work)    | Yes               | Yes             | X                   | X               | ALU grammar |

| CaT compiler phase | Technique | Builds on prior work | Differences in CaT | Other complementary work |
|--------------------|-----------|----------------------|--------------------|--------------------------|
| 1: Resource transfor-| Rewrite   | LLVM [37], HLS [6, 24], p4c [10] | Rewrite rules target RMT, based on novel guarded dependency analysis | p4c [10] uses platform-independent rewrites, Cetus [38] merges tables |
| mation (corresponds |           |                      |                    |                          |
| to HLS code transfor-|           |                      |                    |                          |
| mation)             |           |                      |                    |                          |
| 2: Resource synthesis| Preprocessing: branch removal, SSA,           | Domino [44], SSA [25], VLPW [36] | No backward control flow (like Domino) | Lucid [47] uses syntactic rules to ensure operations map to Tofino |
| (corresponds to HLS operation |  | LLVM [37], HLS code transforma- | No backward control flow |                          |
| binding and HLS module selection) | | | | |
|  | Uses program synthesis for mapping operations to ALUs | Chipmunk [29] | Novel synthesis procedure: faster, more scalable, uses smaller queries |                          |
|  | Target portability via parameterizable grammars for ALUs | Sketch [46], Chipmunk [29] | Generate resource graph (used in Phase 3), not low-level ALU config |                          |
|  |  |  | | |
| 3: Resource allocation| Constraints for match memories | Jose et al. [34], Lyra [28] | Associates match memories with corresponding action resources | |
| (corresponds to HLS scheduling) | Constraints for multi-stage actions | Domino [44], Chipmunk [29] | Uses result of Phase 2 for intra-action dependencies and ALU output propagation | |
|  | Constraints for multiple transactions | Domino [44], Chipmunk [29] | Enforces inter-table and intra-action dependencies for global optimization | |
|  | Modeling real hardware constraints in backend FPGA target | Menshen provides a FPGA backend target [51] | Extended functionality of resources available in Menshen | |
|  |  |  | | |

### Table 2: CaT in relation to HLS and other related work.

#### 3.1.1 Guarded dependency analysis. The sequence of program statements inside the apply {...} block of a P4 control block can be treated as a well-structured branching program (without loops) with (possibly nested) if-statements, reads and writes to PHV fields, and apply statements, which apply match-action tables. This program induces Read-after-Write (RAW), Write-after-Read (WAR), and Writer-after-Write (WAW) dependencies between pairs of program statements. These dependencies must be respected during synthesis and resource allocation. Conventionally, these dependencies are defined between pairs of program statements without accounting for path conditions [35], i.e., conditions under which a control path in a program is executed. Specifically, a dependency pair denoted as (v@S1 → v@S2, t) represents a t-dependency, t ∈ {RAW, WAR, WAW}, due to variable v between statements S1 and S2.

Consider the motivating example ME-2 shown in Figure 3, also inspired by a part of a real SipHash P4 program developed by other users [52]. The WAW dependencies (shown on the right) lead to requiring 3 pipeline stages. However, these WAW dependencies are not real, since the if-conditions guarding these assignments are disjoint. Indeed, a developer

Figure 3: Motivating Example ME-2: The control flow graph of a P4 control block (left), simplified from SipHash [52]. Dependencies shown as dotted red edges. v1 ≠ v2 ≠ v3 are constants.
of this program recognized the disjoint conditions and manually changed the program to use nested-if statements, which requires 1 stage. We would like to automate such rewrites. In particular, P4C and the Tofino compiler miss these rewrites in ME-2, likely due to a conservative dependency analysis.

To solve this issue, we propose guarded dependencies, which take into account path conditions along control paths. Given a control-flow graph (CFG) \( C \) for a P4 control block, a guarded dependency between nodes \( (n_1, n_2) \in C \) is defined as a tuple \( (v \in \mathcal{S}_1 \rightarrow \mathcal{S}_2, t, \phi) \), where \( v \) is the variable of concern at statement \( s_1 \) (in node \( n_1 \)) and statement \( s_2 \) (in node \( n_2 \)), \( t \in \{ \text{RAW}, \text{WAR}, \text{WAW} \} \), and \( \phi \) (called a guard) is a formula that describes all the path conditions under which node \( n_2 \) may be visited after node \( n_1 \) is visited. We now focus on (possibly nested) if-else statements where the branch conditions are tests on packet fields that can be implemented as keys in a match-action table. Based on the guarded dependency analysis, if there is no dependency between the branches, then we can rewrite them into a match-action table. The key of the generated table is comprised from packet fields used in the if-else conditions, and the actions are the computations within each branch. For example, Figure 4 illustrates our rewrites on two P4 programs – ME-2, and another motivating example ME-3 taken from a UPF Rate_enforcer example (provided by others). After rewriting, both ME-2 and ME-3 use only match-action tables and thus no gateway resources.

3.2 Phase 2: Resource Synthesis

For the second phase, we propose a novel procedure to perform resource synthesis on each P4 action block. Like Chipmunk [29], we too use the SKETCH [46] program synthesis tool to generate semantically equivalent code where operations are mapped to hardware ALUs. However, there are two important differences from Chipmunk. First, we aim to reduce synthesis time by creating smaller synthesis queries for SKETCH, rather than invoking it for synthesis of the entire transaction. Second, rather than creating low-level holes in the ALU grid architecture that are filled by SKETCH (as done by Chipmunk), our synthesis queries are parameterized by a grammar that specifies hardware ALUs. These parameterizable grammars enable the same synthesis procedure to be used for different hardware backends, thereby improving compiler retargetability. Our compiler currently supports three different grammars: Tofino ALUs [8], Banzai ALUs [44], and ALUs for our simulation of Menshen [51]; more can be supported as needed. We now describe details of resource synthesis.

3.2.1 Preprocessing of a P4 action block. We preprocess each action block of the P4 program to prepare for synthesis. We first use some standard preprocessing steps (similar
3.2.2 Computation graph construction. After preprocessing, we construct a dependency graph (similar to Domino), with nodes for each program statement (a conditional assignment) and an edge for each RAW dependency.\(^1\) Edges are also added between the pre/post-state fields of each stateful variable. The strongly connected components (SCCs) of this graph correspond to stateful updates, which are condensed to form a computation graph \(G\). Thus, \(G\) is a directed acyclic graph (DAG) with nodes for program computations (some with stateful updates) and edges for RAW dependencies. Nodes in \(G\) are partitioned into two sets: stateful nodes are formed from SCCs on the dependency graph, containing a set of program statements that describe an atomic stateful update; stateless nodes are the other nodes in the dependency graph. Each edge \((u, v)\) is mapped to a packet field variable that appears in the LHS of the assignment at \(u\) and in the RHS of the assignment at \(v\). We call sources of \(G\) (excluding stateful variables) primary inputs (PIs) – these represent input packet fields. Inputs to stateful nodes and outputs of sinks of \(G\) that are not temporaries (such as pre/post-state fields, created during preprocessing) are called primary outputs (POs) – these represent the final values written to packet fields.

3.2.3 Synthesis Procedure for a P4 Action. Synthesis for a P4 action is now performed on the computation graph \(G\). Our procedure, detailed below, consists of four main steps: 1) normalization; 2) folding and predecessor packing optimizations; 3) synthesis of stateful updates; 4) synthesis of minimum-depth solutions for stateless code. Pseudocode for the procedure is shown in Algorithm 1 in Appendix A.

One main novelty of our synthesis procedure is that it decomposes the overall problem into multiple SKETCH queries, many of which are much simpler than a query for an entire transaction. In particular, Step 3 checks that each stateful update fits into a single stateful ALU. If any such query fails, then we terminate the procedure and provide feedback to the user about the reason for failure. We also use small queries to perform optimizations in Step 2, to help Step 3 succeed.

Finally, Step 4 uses queries to perform synthesis for computations that provide inputs to the stateful nodes and the POs in \(G\). Another novelty is that Step 4 synthesizes solutions of minimum-depth (i.e., minimum number of pipeline stages) for the stateless code in \(G\), by using SKETCH in an iterative loop. This enables CaT to handle rich stateless computations in multi-stage actions, while searching the space over all possible equivalent programs. Although Chipmunk can also handle multi-stage actions and an exhaustive search space, its queries consider an entire transaction, which makes it much slower in comparison (§4.3).

Step 1: Normalization of computation graph. In the typical hardware backends that we target (e.g., Menshen, Tofino), a stateful ALU can output a single value that is either the pre-state or the post-state value of one of its stateful registers. In this step, we normalize \(G\) to a graph such that each stateful node has only one output, and each packet field labelled as an out-edge from a stateful node is either the pre-state field or the post-state field.

Step 2: Folding and predecessor packing optimizations. We iterate the following two optimizations until convergence.

Folding to reduce input edges. A stateful node with too many in-edges could cause Step 3 to fail, due to a limited number of inputs available in ALUs. The folding optimization finds opportunities to reduce the number of in-edges to a stateful node. We consider dependent inputs, i.e., inputs that are themselves functions of other inputs to a stateful node. For each such candidate \(i\), we query SKETCH to check if the function that computes \(i\) can be folded into the stateful node itself, such that the enlarged node fits into a stateful ALU. If the synthesis query is successful, \(i\) is removed. An example benchmark (BLUE (decrease) [27]) where this works well is shown in Figure 5. Here, folding reduces an edge between the top two nodes, thereby reducing the pipeline usage by 1.

Predecessor packing to merge nodes. Even after folding, the stateful update in a single node in \(G\) might not fully utilize an available stateful ALU. Consider again the BLUE (decrease) example in Figure 5, where the middle box shows \(G\) after folding. Here, a single Tofino stateful ALU can actually implement both stateful updates (in blue boxes) in a single stage, as shown by a merged node on the right. To achieve this, we use a simple heuristic called predecessor packing, inspired by technology mapping for hardware designs [23]. The idea is to pack more into a stateful ALU by attempting a merge of nodes \(u\) and \(v\), where at least one node is stateful and where predecessor \(u\) has only one out-edge (to \(v\)). Again, we implement a merge-attempt via a SKETCH query, and merge the nodes if the query is successful. In our evaluations (§4.3), we show that these optimizations are effective in compiling to fewer stages in the pipeline.

\(^1\)Conversion to SSA form removes WAW and WAR dependencies.
Stateful nodes shown in blue, stateless nodes shown in yellow, pre/post-state fields shown in red, modified parts shown in bold.

**Step 3: Synthesizing stateful updates.** To preserve the transactional semantics of the program, each stateful update must be completed within a single stage, i.e., it must fit in a single stateful ALU. For each stateful node in $G$, we generate a SKETCH query to check if the stateful update can be implemented by a stateful ALU using a grammar $A_1$. We assert that the query succeeds; if it fails, our procedure terminates with an error (and feedback to the user).

**Step 4: Minimum-depth solutions for stateless code.** In the last step, we synthesize code for the inputs to the stateful ALUs and the POs of $G$. For each variable $o$ to be synthesized, we first compute its backwards cone of influence (BCI), which is often used in verification/synthesis tasks to determine the dependency region up to some (boundary of) inputs [31]. Essentially, a BCI provides the functional specification for $o$ in terms of PIs and outputs of stateful nodes in $G$. Note that these specifications are stateless, i.e., they do not include any stateful nodes. We model a switch’s stateless ALU functionality using a grammar $A_2$, and then use SKETCH to find a minimum-depth tree solution for $o$, where each tree node represents a stateless ALU. Since SKETCH cannot directly optimize for depth, we invoke it in a loop. An example computation graph with a single stateful update (blue box) and the associated synthesis query results are shown in Figure 6.

**3.2.4 Final Result of Phase 2.** The final result of the synthesis procedure is represented in the form of a resource graph $R$ for a given P4 action block, where each node $v$ in $R$ represents a stateful/stateless ALU, and an edge $(u, v)$ in $R$ indicates that the output of ALU $u$ is connected to an input of ALU $v$. These resource graphs play an important role in resource allocation, the next phase of our compiler. Our claim of correctness for the synthesis procedure along with a proof are provided in Appendix B.

**3.3 Phase 3: Resource Allocation**

After performing synthesis for each P4 action block, our third phase of the compiler performs global resource allocation for the full P4 program by using a constraint-based formulation, shown in Table 3. The top part lists the definitions of constants, indices, variables, and sets that are used to automatically generate the constraints. The bottom part shows the full set of constraints, divided into a first set that is similar to prior work [34, 38], and a second set that is new in our work. Our new constraints address: (1) ALU resources in action computations, (2) multi-stage actions, (3) fitting multiple action blocks in the same pipeline stage, and (4) propagation of ALU outputs. Prior efforts either do not consider allocation of ALU resources and multi-stage actions [34, 38], or do not address multiple action blocks [29, 44]. Another novel feature of our approach is that we use the resource graph $R$ synthesized for each action block (in Phase 2), to perform global optimization in this phase.
ALU allocation (1,2) ensure that each ALU in each action is assigned to some pipeline stage $s$.

Table dependency constraint, this allows ALUs from multiple stages to be assigned in the same pipeline stage.

Two consecutive stages, such that if a packet matches entry $m$ in table $t$ in stage $s$, it will match entry $m$ in table $t$ in stage $s + 1$ as well, resulting in action $A$ being executed completely over the two stages.

To allow flexibility in allocating multiple action blocks in the same pipeline stage, we also allow Action $A$ to be assigned to non-consecutive stages. In this case, we need to allocate additional ALUs to propagate the intermediate results to other stages (required by both Tofino and Menshen backends).

The ALU allocation constraints (1-4) handle these additional ALUs, where the sets $U_m$, $Needs_u$ (defined in the top part of Table 3) are computed from $R_{tia}$. (For ILP, ALU propagation 3 constraint can be formulated using the well-known Big-M method as shown in Appendix C.)

### Solving the constraint problem

We can use either an ILP solver (Gurobi [5]) or an SMT solver (Z3 [26], which supports optimization) to find an optimal or a feasible solution. We specify an objective function for finding an optimal solution, e.g., we add the constraint $\min cost$ to minimize the number of stages, where $cost$ is the stage assigned to any ALU. i.e., $\forall t, i, a, u \in V_{tia} : cost \geq stage_u$. To find a feasible solution, we use a trivial objective function ($\min 1$) with Gurobi (none is needed with Z3).

### Implementation and Evaluation

We implement the CaT compiler with the workflow shown in Figure 1. The resource transformation phase is implemented on top of p4c [10]. We also use p4c to identify the action blocks and table dependencies needed in CaT’s resource synthesis and resource allocation phases. For the backend, ideally the CaT compiler should directly output machine code for the targets. However, due to the undocumented and proprietary machine code format of the Tofino chipset, we generate a low-level P4 program by using a best-effort encoding for the resource constraints, based on known information about the Tofino chipset. For the Menshen backend, we extend the open-source RMT pipeline [9, 51] by writing additional Verilog to support richer ALUs, e.g., the IfElseRAW ALU from the Domino paper [44]. The CaT compiler directly outputs machine code to configure various programmable knobs (e.g., ALU opcodes, operands, etc.) within Menshen’s Verilog code.

### Sanity checking of CaT prototype

We check CaT’s output for Menshen using its cycle-accurate simulator, which can be fed input packets to test the generated machine code. We create P4-16 benchmarks starting with a subset of the switch.p4 program [45], consisting of 2–6 tables randomly sampled.
from switch.p4. Then, we add new actions to the tables using @atomic blocks for transactional behavior. The logic within these atomic blocks consists of one of 8 Domino benchmark programs [44]. (The IfElseRaw ALU in our simulator is not expressive enough for the remaining 6.) We also test the 8 benchmark programs in isolation, generating 24 benchmarks in total, many of which have multiple transactions and thus stress both resource synthesis and resource allocation. We randomly generate test input packets and inspect the output packets from the simulation. So far, all our sanity checks on CaT’s outputs have passed.

4.1 Evaluation Setup and Experiments
We address the following evaluation questions for components of the CaT compiler.

Q1: Resource Transformation. How much does the CaT’s resource transformation help in terms of the resource usage? We select 3 benchmarks [2] extracted from real P4 applications and compare the resource usage for pre- and post-transformed programs (§4.2).

Q2: Resource Synthesis. How does CaT’s resource synthesizer compare to existing ones? We compare CaT with Chipmunk over several dimensions (§4.3) using ALUs drawn from Tofino [8] and Banzai [44]. Appendix (D) shows a deeper analysis on the benefits of the predecessor packing and preprocessing optimizations.

Q3: Resource Allocation. How good is the CaT compiler in terms of resource usage? We use Gurobi as the default for resource allocation and compare the runtime of the Gurobi and Z3 solvers. In addition, we compare the two modes of finding either an optimal or a feasible solution (§4.4).

Q4: Retargetable Backend. Can CaT easily perform compilation for different hardware targets? Our synthesis experiments with the Banzai and Tofino ALUs already demonstrate this feature. Additionally, we run the CaT compiler on different simulated hardware configurations, compile the switch.p4 under varying constraints and report the results (§4.4).

Benchmark selection.
- Resource transformation: 3 benchmarks (ME-1, ME-2, ME-3) extracted from SipHash and UPF (real P4 programs developed by P4 users).
- Resource synthesis: 14 benchmarks together with their semantically equivalent mutations (10 for each benchmark, so 140 in total) from the Chipmunk paper [29].
- Resource allocation: Same as the benchmarks we use for sanity checking our prototype. We use the full switch.p4 program for experiments that vary hardware resource parameters in the Menshen backend.

Machine configuration. We use a 4-socket AMD Opteron 6272 (2.1 GHz) with 64 hyperthreads and 256 GB RAM to run all our experiments for both CaT and Chipmunk. Note that Chipmunk runs more complex SKETCH queries and uses many identical machines to concurrently explore different-sized ALU grids, whereas CaT only uses one machine, saving a lot of computation resources.

4.2 Results for Resource Transformation
The resource transformation phase of CaT compiler rewrites if-else statements in the P4 program into match-action tables as much as possible. For benchmarks ME-1, ME-2, and ME-3, the post-transformed programs reduced the usage of gateway resources. In addition, since the rewriting merges many default tables from if-else branches into one big table, the total number of tables is reduced. We also confirm that the transformed programs use fewer stages than the original programs by compiling them using the Tofino compiler.

4.3 Results for Resource Synthesis
We compare the CaT and Chipmunk compilers on the SipHash benchmark (cf. Figure 2) and on all benchmarks used in the Chipmunk work [29]. For the latter, we consider targeting both Tofino ALUs and Banzai ALUs, to test the performance of CaT on different instruction sets and various input programs. This also demonstrates CaT’s retargetability via different ALU grammars.

Results for SipHash. CaT successfully compiles the SipHash P4 program [52] with Tofino ALU in around 40 hours. This runtime is much higher than for other benchmark examples due to two main reasons. First, the compiled program takes 4 pipeline stages due to a single multistage action, resulting in a large synthesis search space. Second, the SipHash example involves bitvector operations in addition to integer arithmetic, making the synthesis problem harder for SKETCH (the program uses 32-bit bitvectors, whereas SKETCH’s default for integers is 5 bits). To reduce the CaT compile time, we experiment with further decomposing the synthesis queries in the computation graph, after which the total time for synthesis is reduced to ≈10s. In comparison, Chipmunk fails to output the result even after 150 hours.

Results for Chipmunk benchmarks. The results are shown in Table 4, for Tofino ALUs and Banzai ALUs, respectively. We report the runtime of full compilation; for CaT, this includes the resource allocation time, which Chipmunk does not perform. We consider 10 semantically equivalent mutations of each of the benchmarks, and report the mean and standard deviation of compilation time across all mutations. The running times in Table 4 are similar to, but slightly different from that in Table 2 of the Chipmunk paper [29]. The differences arise due to Chipmunk’s use of SKETCH’s parallel mode, which is non-determinism.
Table 4: CaT vs. Chipmunk and Domino; with Tofino or Banzai ALUs. (pred: Predecessor packing, ppa: Preprocessing, ✓: succeeded)

| Program | ALU         | CaT default | Chipmunk [29] | Domino [44] |
|---------|-------------|-------------|---------------|-------------|
|         | Avg Time (s) | Std Time (s) | Avg #stages w/o pred | Avg #stages w/o ppa | Avg Time (s) | Std Time (s) | Avg #stages w/o pred | Avg #stages w/o ppa |
| BLUE (increase) [27] | 19.04 | 0.43 | 1 | 2 | 1 | 159.78 | 59.03 | 2 | 8.39 ✓ |
| BLUE (decrease) [27] | 18.72 | 0.84 | 1 | 2 | 1 | 142.5 | 42.5 | 2 | 7.61 ✓ |
| Flowlet switching [43] | 19.76 | 0.69 | 2 | 2 | 1 | 962.83 | 1170.16 | 2 | 48.73 ✓ |
| Marple new flow [41] | 6.65 | 0.52 | 1 | ✓ | 1 | 5.2 | 1.71 | 1 | 0.78 ✓ |
| Marple TCP NMO [41] | 13.24 | 0.53 | 2 | ✓ | ✓ | 6.56 | 0.36 | 2 | 0.50 ✓ |
| Sampling [44] | 14.03 | 0.57 | 1 | ✓ | 1 | 22.87 | 10.68 | 1 | 1.63 ✓ |
| RCP [50] | 20.19 | 0.59 | 1 | ✓ | 1 | 65.13 | 20.93 | 1 | 3.23 ✓ |
| SNAP heavy hitter [16] | 3.58 | 0.25 | 1 | 1 | 1 | 26.83 | 13.63 | 1 | 7.49 ✓ |
| DNS TTL change [1] | 20.84 | 1.97 | 2 | 3 | ✓ | 36.34 | 50.55 | 2 | 1.74 ✓ |
| CONGA [15] | 10.24 | 0.43 | 1 | ✓ | 1 | 3.02 | 0.17 | 1 | 0.29 ✓ |
| BLUE (increase) [27] | 40.69 | 1.41 | 4 | 4 | 4 | 166.88 | 36.59 | 4 | 4.10 ✓ |
| BLUE (decrease) [27] | 38.83 | 1.48 | 4 | 4 | 4 | 1934.82 | 1611.66 | 4 | 49.83 ✓ |
| Flowlet switching [43] | 25.37 | 0.94 | 3 | 3 | 3 | 185.84 | 81.41 | 3 | 7.33 ✓ |
| Marple new flow [41] | 13.79 | 0.44 | 2 | 2 | 2 | 12.31 | 0.18 | 2 | 0.89 ✓ |
| Marple TCP NMO [41] | 28.12 | 2.60 | 3 | 4 | ✓ | 15.3 | 0.49 | 3 | 0.54 ✓ |
| Sampling [44] | 11.52 | 0.65 | 2 | 2 | 2 | 33.39 | 11.09 | 2 | 2.90 ✓ |
| RCP [50] | 25.08 | 0.85 | 2 | 2 | 2 | 31.21 | 7.35 | 2 | 1.24 ✓ |
| SNAP heavy hitter [16] | 3.45 | 0.23 | 1 | 1 | 1 | 69.07 | 19.36 | 1 | 20.02 ✓ |
| DNS TTL change [1] | 32.63 | 34.91 | 3 | 5 | ✓ | 211.67 | 22.65 | 3 | 6.49 ✓ |
| CONGA [15] | 10.27 | 0.55 | 1 | 1 | 1 | 19.47 | 8.05 | 1 | 1.90 ✓ |
| Stateful firewall [16] | 2499.43 | 4638.58 | 4 | 4 | ✓ | 6749.89 | 6349.94 | 4 | 2.70 ✓ |
| Flowlet switching [43] | 31.04 | 0.73 | 3 | 3 | 3 | 212.12 | 4.47 | 3 | 6.85 ✓ |
| Spam Detection [16] | 3.51 | 0.21 | 1 | 1 | 1 | 59.95 | 17.75 | 1 | 17.08 ✓ |
| STFQ [50] | 20.99 | 2.04 | 3 | 3 | 3 | 22.73 | 6.94 | 2 | 1.08 ✓ |

We also report the resource consumption of the generated code produced by CaT, in terms of the total number of pipeline stages required on average across mutations ("#stages default" column). This is the most important scarce resource in network substrates (e.g., 12 stages for Tofino). For evaluating the effectiveness of our predecessor packing optimization (pred) and the preprocessing analyses (ppa) (§3.2.3), we also report the number of stages without these turned on in columns "#stages w/o pred", "#stages w/o ppa", respectively. Gray-ed entries indicate a difference from the default setting (more detailed analysis in Appendix D).

Our results show that CaT is able to compile all programs successfully compiled by Chipmunk, with almost all compiled results having a matching number of pipeline stages. Furthermore, CaT is often much faster and more stable (in running time) than Chipmunk. Specifically, for the Tofino ALUs (Table 4), CaT finishes compilation within a few seconds, 2.75x faster on average (geometric mean) than Chipmunk. The max speedup is 48x for flowlet switching, a minutes-to-seconds improvement (≈16 minutes in Chipmunk vs. 20 seconds in CaT). In BLUE(increase) and BLUE(decrease), CaT generates a solution with less number of stages than Chipmunk. In all other benchmarks the number of stages is the same. For the BLUE benchmarks, since the Tofino stateful ALU contains two registers, CaT’s optimizations enabled it to pack a successive pair of stateful updates into a single stateful ALU (§3.2.3). In comparison, Chipmunk mapped the two stateful updates to two ALUs in two stages. This shows that CaT’s approach can find additional opportunities for fully utilizing the functionality of available hardware resources. Predecessor packing is also effective in 9 of 10 benchmarks, enabling compilation to succeed or reducing the number of stages; preprocessing is also useful in 2 benchmarks.

For the Banzai ALUs (Table 4), we additionally report results on stages required by the Domino compiler [44] (that only handled Banzai ALUs), with the average number of stages across different program mutations shown in the last column (as reported in [29]). Note first that CaT takes no more than 1 minute on most successful benchmarks. Although it takes 40 minutes for stateful firewall, Chipmunk is much slower, requiring more than 1.5 hours. CaT provides 3.94x speedup on average (geometric mean) and 49x maximum, with respect to Chipmunk. CaT is slower only on Marple new flow and Marple TCP NMO, but finishes both within 30 seconds. Note that Chipmunk uses multiple machines and only reports the minimum running time across all, while CaT only uses one machine to do the synthesis. In terms of number of stages, CaT generates code with the same number of stages as Chipmunk for all benchmarks except the STFQ example (3 in CaT vs. 2 in Chipmunk). Upon investigation, we find that this is due to separation between queries for stateful and stateless nodes in our synthesis procedure. Although our predecessor packing optimization can often mitigate this negative effect, we plan to improve it further in future work. Still, both predecessor packing and preprocessing optimizations are effective in some benchmarks here as well. Finally, note that Domino either fails to compile (8 of 14 examples), or uses many more stages (other 6 examples). Overall, our results show that CaT can generate high-quality code comparable to Chipmunk, but in much less time and with less powerful compute resources.
4.4 Results for Resource Allocation

We experiment with two solvers (Gurobi and Z3) and two modes (optimal and feasible) on our benchmark examples. The detailed data (CDFs of runtime and stage count) are shown in Appendix E (Figure 7). The results show that for checking feasibility, Gurobi returns suboptimal solutions that use all the pipeline stages, while Z3 finds feasible solutions that are better than Gurobi’s but takes marginally more time. However, Gurobi finds an optimal solution in almost the same time as it takes to find a feasible solution. For these benchmarks, Gurobi is faster than Z3. Thus, Gurobi with optimization is a good default.

We also study the resource allocation time of switch.p4 as a function of the parameters of the Menshen backend target. We vary the maximum number of entries per table, number of stages, and number of tables per stage, and plot the runtime of Gurobi in both optimal and feasible modes. The results (in Appendix E, Figures 8, 9, 10) show that the runtime is similar for optimal and feasible modes, but varies significantly on different instances depending on whether there is a solution.

5 CONCLUSIONS

This paper introduces a new approach to building compilers for packet-processing pipelines based on high-level synthesis. We adopt this approach to develop CaT, a compiler for P4 programs. CaT can handle more programs, reduce pipeline resource usage, and compile faster and with fewer compute resources than existing compilers. We hope these results encourage compiler engineers for such packet-processing pipelines to adopt similar ideas for production-quality compilers.

This work does not raise any ethical issues.

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A PSEUDO-CODE FOR SYNTHESIS PROCEDURE

Our synthesis procedure is shown in Alg. 1. It consists of four main steps: 1) normalization; 2) folding and predecessor packing optimizations; 3) synthesis of stateful updates; 4) synthesis of minimum-depth solutions for stateless code.

B CORRECTNESS OF SYNTHESIS PROCEDURE

THEOREM 1 (CORRECTNESS). The result of the CaT synthesis procedure (Alg. 1) on a computation graph $G$ is correct.

PROOF SKETCH. Our synthesis procedure works by decomposing $G$ (after correctness-preserving normalization and optimizations in Steps 1 and 2 of Alg. 1, respectively) into disjoint subgraph components of stateful nodes and stateless BCIs of P0s. Each such subgraph of $G$ corresponds to a specification of either a PO or a stateful update. Each of these is then synthesized into a subgraph of $R$, by Steps 3 and 4 of Alg. 1, respectively. Each synthesized subgraph corresponds to an implementation of the specification of either a PO or a stateful update. Based on correctness of program synthesis in SKETCH [46], the stateful updates and POs in $R$ are functionally equivalent to those in $G$. Hence the resource synthesis result is correct. 

C ILP ENCODING FOR ALU PROPAGATION CONSTRAINTS

We use the big-M method to obtain an ILP formulation of the constraint

$$\forall u \in I, \forall s (beg_u < s \land s < end_u) \leftrightarrow prop_{us} = 1$$

For each $u \in I$ and $s \in \{1, \ldots, N_S\}$, we use a binary variable $lo_{us}$ as an indicator for $beg_u < s$ and a binary variable $hi_{us}$ as an indicator for $s < end_u$. $M$ is a large constant (e.g., $N_S + 5$).

The following constraints ensure that $lo_{us}$ is 1 if $beg_u < s$ and 0 otherwise.

$$s - beg_u \leq Mlo_{us} \quad (1)$$

$$s - beg_u > -M(1 - lo_{us}) \quad (2)$$

If $s - beg_u > 0$ then $lo_{us} = 1$ (1) and if $s - beg_u \leq 0$ then $lo_{us} = 0$ (2).

The following constraints ensure that $hi_{us}$ is 1 if $s < end_u$ and 0 otherwise.

$$s - end_u < M(1 - hi_{us}) \quad (3)$$

$$s - end_u \geq -Mhi_{us} \quad (4)$$

If $s - end_u < 0$ then $hi_{us} = 1$ (4) and if $s - end_u \geq 0$ then $hi_{us} = 0$ (3).
The following constraints use $lo_{us}$ and $hi_{us}$ to make $prop_{us}$ an indicator for $beg_{u} < s < end_{u}$,

\[
lo_{us} + hi_{us} - 2 < Mprop_{us} \quad (5)
\]
\[
lo_{us} + hi_{us} - 2 \geq M(1 - prop_{us}) \quad (6)
\]
If $lo_{us} + hi_{us} - 2 \geq 0$ then $prop_{us} = 1$ (5) and if $lo_{us} + hi_{us} - 2 < 0$ then $prop_{us} = 0$ (6). This means that $prop_{us} = 1$ only if both $lo_{us} = 1$ and $hi_{us} = 1$. Hence, $prop_{us} = 1$ if $s > beg_{u}$ and $s < end_{u}$, otherwise $prop_{us} = 0$.

### D DISCUSSION OF RESOURCE SYNTHESIS RESULTS

We performed controlled experiments to evaluate two optimizations (§3.2.3): (1) Predecessor packing, and (2) Preprocessing analyses (constant folding, algebraic simplification, dead code elimination). The results for the Banzai ALUs are shown in Table 4 for CaT (with both optimizations enabled), CaT without predecessor packing (CaT w/o pred), and CaT without preprocessing analyses (CaT w/o ppa).

**Predecessor packing.** As for Banzai ALUs, without predecessor packing, CaT uses additional stages to compile two examples (Marple TCP NMO, and DNS TTL change), showing that predecessor packing can reduce the number of pipeline stages. With the Tofino ALU (results in Table 4), predecessor packing was even more beneficial: disabling predecessor packing resulted in compilation errors for 6 examples (flowlets, Marple new flow, Marple TCP NMO, Sampling, RCP, and CONGA), since the Tofino ALU supports very limited stateless computation and cannot handle relational or conditional expressions. Packing such expressions into adjacent stateful ALUs allowed compilation to succeed.

**Preprocessing analyses.** As for Banzai ALUs, without preprocessing analyses, three of the examples could not be compiled. For all other examples, the number of stages is identical with and without this optimization. We observe similar trends when the Tofino ALU is used (Table 4). The runtime of the preprocessing analyses itself is negligible, less than 0.1 sec in all examples. Overall, our results show the effectiveness of these optimizations in providing a sweet spot for CaT, such that it is much faster than Chipmunk while generating optimal or close-to-optimal number of stages.

### E ADDITIONAL RESULTS FOR RESOURCE ALLOCATION

We experiment with two solvers (Gurobi vs. Z3) and two modes (optimal and feasible solutions) on all our 24 benchmarks. We report both time spent running the solvers and the final number of stage usage to compare between different solvers and different modes. Table 5 shows the detailed results.
We also run experiments on different simulated hardware configurations for finding feasible vs. optimal solutions using Gurobi. The results are shown in Figures 8, 9, 10. We plot a vertical line indicating the transition from reject to accept for the constraint solver. Across a variety of hardware configurations, we find that the runtime of both modes are quite similar. Figure 8 shows that the runtime increases as the maximum number of entries decreases because of the increase in the number of partitions of a table (and hence number of variables) as the maximum number of entries decreases. Figure 9 shows that runtime as the number of stages increases because of the increase in the number of indicator variables tracking which stage a table belongs to. In Figure 10, the number of Gurobi variables is constant as we vary the number of tables per stage; however, whether a program can be rejected or accepted given the hardware constraints affects the runtime of the ILP procedure.
Figure 7: Gurobi vs. Z3: Running time, Num of stages.

Figure 8: Varying # of max. entries/table.

Figure 9: Varying # of stages.

Figure 10: Varying # of tables per stage.