Enabling Flexibility for Sparse Tensor Acceleration via Heterogeneity

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Abstract—Recently, numerous sparse hardware accelerators for Deep Neural Networks (DNNs), Graph Neural Networks (GNNs), and scientific computing applications have been proposed. A common characteristic among all of these accelerators is that they target tensor algebra (typically matrix multiplications); yet dozens of new accelerators are proposed for every new application. The motivation is that the size and sparsity of the workloads heavily influence which architecture is best for memory and computation efficiency. To satisfy the growing demand of efficient computations across a spectrum of workloads on large datacenters, we propose deploying a flexible ‘heterogeneous’ accelerator, which contains many ‘sub-accelerators’ (smaller specialized accelerators) working together. To this end, we propose: (1) HARD TACO, a quick and productive C++ to RTL design flow to generate many types of sub-accelerators for sparse and dense computations for fair design-space exploration, (2) AESPA, a heterogeneous sparse accelerator design template constructed with the sub-accelerators generated from HARD TACO, and (3) a suite of scheduling strategies to map tensor kernels onto heterogeneous sparse accelerators with high efficiency and utilization. AESPA with optimized scheduling achieves 1.96× higher performance, and 7.9× better energy delay product (EDP) than a Homogeneous EIE-like accelerator with our diverse workload suite.

I. INTRODUCTION

Large datacenters are expected to compute a wide variety of workloads such as deep neural networks, graph neural networks, and scientific computing [13], [30], [37], [38], [44]. These workloads utilize tensors (a matrix is a two-dimensional tensor, and a vector is a one-dimensional tensor) of different dimension sizes and sparsity characteristics. For example, matrix dimension sizes span from single digits to millions while matrix sparsity spans from ∼10−5% dense to fully dense [9]. The vast amount of workloads has led to many accelerator architecture proposals, as they achieve higher throughput than CPUs, and higher energy efficiency than GPUs [21], [46], [48]. There are numerous types of sparse accelerators because they typically target a specific application, which often have tensors with similar dimensions, sparsity, and structure.

Many of these accelerators are rigid in both the dataflow choice as well as the sparsity format employed. This makes them perform extremely well for certain workloads, but poorly for other workloads. For instance, a systolic array is most energy-efficient for dense computations, but not for workloads of high unstructured sparsity. ExTensor [19], on the other hand, performs well for workloads of high unstructured sparsity, but not for dense computations due to its sparse controller overhead. Large datacenters require flexibility, as in they must have the compute and memory resources to perform all current and future workloads efficiently. To address this challenge, we propose a new heterogeneous sparse accelerator and scheduling techniques to enable high efficiency across a diverse set of workloads. To realize this architecture, we identify three challenges that we address in this work.

Challenge 1: Building Blocks. The first challenge is to identify the right sparse sub-accelerator building blocks. Recently, numerous sparse architectures have been proposed for different applications [5], [15], [15], [18], [19], [40], [42], [43], [52], [53], [56], [59], [62]. There seems to be dozens of new sparse matrix multiplication accelerators proposed for every new application. This is a growing problem because there are many sparse accelerators that are similar. For example, both MatRaptor [52] and Gamma [59] utilize Gustavson’s Algorithm. Detailed explanation is in Section III.

To address this challenge, we turn to TACO, a popular

| Accelerator Type | # PEs (With area constraint) | Peak TFLOPS/s | Relative EDP Benefits† | MK Sparsity Support | KN Sparsity Support | Matrix Mult. Parallelism Dimension Bound |
|------------------|-------------------------------|---------------|------------------------|---------------------|---------------------|-----------------------------------------|
| Homogeneous TPU-like (SpGEMM) | 17280 | 34.56 | 0.13x | No | No | M×N |
| Homogeneous EIE-like (SpGEMM) | 10176 | 20.35 | 1.0x | No | Yes | N |
| Homogeneous ExTensor-like (SpGEMM) | 4992 | 9.98 | 2.6x | Yes | Yes | M or N |
| Homogeneous OuterSPACE-like (SpGEMM) | 12032 | 24.06 | 0.4x | Yes | Yes | K |
| Homogeneous MatrixRaptor-like (Gustavson’s SpGEMM) | 8320 | 16.64 | 0.6x | Yes | Yes | N |
| Homogeneous Hybrid (TPU + EIE + ExTensor-like) | 4480 | 8.96 | 6.2x | Yes | Yes | M×N, N, or M |
| AESPA (This work) | 11008 | 16.90 | 7.9x | Yes | Yes | Variable (Flexible) |

Fig. 1: Design characteristics of homogeneous sparse accelerators (consisting of one type of sub-accelerator) versus heterogeneous sparse accelerators (consisting of 2+ types of sub-accelerators). Matrix A is M × K and Matrix B is K × N.
sparse tensor compiler [7], [8], [25]. Many of the sub-accelerators can be described at an algorithmic level using insights from TACO. ‘Dense’ sub-accelerators operate on uncompressed input tensor operands, while ‘sparse’ sub-accelerators operate on compressed input tensor operands. The compression format combination of the input tensors influence the type of dataflow the sparse sub-accelerator utilizes, which is discussed in Section II. We propose a new sparse sub-accelerator design methodology named HARD TACO that can generate the RTL for different distinct sub-accelerators for fair performance, power, and area estimates. HARD TACO contains a hardware fine-tuning stage that adds pragmas on top of the TACO output kernel C++ code (shown in Fig 2). The updated code then goes to a HLS tool to generate functional sparse accelerators and controllers. Similar high productivity hardware generation tools include MAGNet [54] and Deepburning-GL [34], but they cannot generate all types of sparse sub-accelerators that HARD TACO can.

Challenge 2: Hardware Design-space Exploration. The second challenge relates to identifying the appropriate design-point using the sub-accelerator building blocks and contrast it against homogeneous alternatives. From a physical die perspective, different sub-accelerators consume different area and power overhead. Under a given area constraint, sub-accelerators with smaller PE sizes can achieve higher TFlops/second than sub-accelerator with larger PE sizes which have significantly more control overhead. On the other hand sub-accelerator with larger PEs due to control logic can handle sparsity more efficiently. Additionally, to build a heterogeneous sparse accelerator, it is important to allocate the right amount of compute and memory resources. Some sub-accelerators require more memory accesses than others, and often lead to lower operational intensity. Fig 1 shows different types of homogeneous accelerators (consisting of one type of sub-accelerator). A homogeneous TPU-like accelerator [21] computes GEMM operations (dense matrix × dense matrix), and a homogeneous EIE-like accelerator [18] computes SpMM operations (sparse matrix × dense matrix or dense matrix × sparse matrix). Homogeneous ExTensor [19], OuterSPACE [40], and MatRaptor-like [52] accelerators all compute SpGEMM operations (sparse matrix × sparse matrix); utilizing inner product, outer product and Gustavson’s algorithm respectively. The different microarchitecture and sparse controller for each sub-accelerator results in different processing element (PE) sizes. With a normalized area constraint, a Homogeneous TPU-like accelerator can achieve 3.4× higher peak TFLOPS/second. Additionally, the type of dataflow used for these accelerator can limit which the amount of parallelism achieved within the accelerator. The OuterSPACE accelerator is bounded by the workload’s K dimension; therefore, there will be underutilization if the K dimension is smaller than the number of OuterSPACE PEs available. Fig 1 also presents homogeneous hybrid accelerators. These type of accelerators contain the necessary sparse controller to support multiple types of operations at the cost of lower max TFLOPS/s.

To address this challenge, we propose AESPA (a heterogeneous sparse accelerator) that efficiently interconnect many different sub-accelerators and scratchpad memories. AESPA provides flexibility (variable parallelism dimension bounds) through heterogeneity by having many types of sub-accelerators while achieving higher TFLOPS/s than the homogeneous hybrid approach across a diverse set of workloads.

Challenge 3: Scheduling/Mapping. The third challenge, is to determine what scheduling strategies provide the best performance, energy efficiency, and utilization. This is actually the first work (to the best of our knowledge) to unravel the challenges of scheduling on heterogeneous sparse sub-accelerators while previous works look solely into heterogeneous dense sub-accelerators [3], [6], [16], [27].

To address this challenge, we propose various scheduling strategies aimed at utilizing all sub-accelerators. Specifically, we look into strategies that can (1) partition a single tensor kernel to utilize all sub-accelerators, and/or (2) partition independent tensor kernels across diverse sub-accelerators for multi-tenancy. Different sparse sub-accelerators may require input tensors to be of a certain format before computation (discussed in Section III), which we address by placing custom hardware format converters into AESPA.

In summary, the key contributions of this paper are:

- We propose a new class of sparse tensor accelerators that leverages the idea of heterogeneous sub-accelerators, each optimized for a specific sparse dataflow (and corresponding compression format).
- We develop HARD TACO, a productive sparse and dense sub-accelerator generation design flow for quick performance, area, and power analysis. (Refer to Section III.)
- We design AESPA, a heterogeneous sparse accelerator that stitches different types of sub-accelerators together. (Refer to Section IV.)
- We propose various scheduling strategies for heterogeneous sparse accelerators. (Refer to Section V.)
- Our findings show that AESPA with optimized scheduling achieves 1.96× higher performance, and 7.9× better energy delay product (EDP) than a Homogeneous EIE-like accelerator with our diverse workload suite.

To the best of our knowledge, this is the first work to analyze how to build a heterogeneous sparse accelerator with various sub-accelerator types, and the first work to propose scheduling policies for such accelerators.

II. BACKGROUND

This section first introduces the main compression formats used in this work. We use a taxonomy to express matrix multiplication algorithms and and sparse accelerator dataflows based on the operands’ compression format.

A. Sparse Compression Formats

There are numerous types of compression formats, both structured and unstructured. For this taxonomy, we focus on
unstructured compression formats used directly for computation. We refer to it as `compute compression format (CCF)` throughout the rest of the paper. To express CSR or CSC (shown in the top section of Fig 3), we follow a naming scheme inspired by TACO [7] and ExTensor [19]. Each dimension of a matrix (two-dimensional tensor) can be uncompressed or compressed. With this method, CSR and CSC can be thought of as the same format, but compressed in a different mode orientation [31].

Following the \( M \times N \times K \) matrix multiplication convention, Matrix \( A \) has dimensions \( M \times K \) and Matrix \( B \) has dimensions \( K \times N \). If Matrix \( A \) is stored in CSR format, then there is a row pointer for every row and a column index for every nonzero value. We represent CSR by \( U_M C_K \) with ‘U’ meaning ‘uncompressed’ and ‘C’ meaning ‘compressed’. The subscript variables represent the dimensions of the matrix. Dimension \( M \) is considered uncompressed as CSR follows a row-major ordering, and each row location must be specified by the row pointer. Alternatively, if Matrix \( A \) is stored in CSC format, we represent it by \( U_K C_M \). If Matrix \( B \) is stored fully uncompressed (dense), it is \( U_K U_N \).

### B. Proposed Taxonomy with TACO

Real world tensors are often sparse, which lead to ineffectual computations (e.g. multiplications with zero-valued operands) on dense hardware. CCFs enable algorithms that can skip these computations by utilizing bookkeeping metadata to indicate where the nonzero elements are located. Each tensor operand has its own compression format. Throughout the rest of the paper, we only read the CCFs in concordant fashion (following the same mode orientation). We propose a taxonomy for matrix multiplications that follows:

\[
(A, B) : \text{format}(\text{Tensor}A), \text{format}(\text{Tensor}B)
\]

To illustrate the taxonomy template and how ineffectual computations are skipped, we use TACO (a tensor algebra compiler for kernel generation) to generate five different matrix multiplication kernels shown in Fig 2. For example, Fig 2c shows a SpGEMM kernel with Matrix \( A \) compressed in \( U_M C_K \) and Matrix \( B \) compressed in \( U_N C_K \).

Using our template, we refer to this as:

\[
(A, B) : U_M C_K, U_N C_K
\]

Fig 2a shows a TACO generated kernel with both matrices computed uncompressed (\( U_M U_K, U_K U_N \)). All loops depend on the dimensions of the GEMM operation. Since there is no way to distinguish whether the input matrices’ elements are zero-valued or non-zero-valued, all computations are scheduled regardless of sparsity. Fig 2b shows a TACO kernel with the CCF combination of \( U_M U_K, U_N C_K \). Matrix \( B \) is compressed with only nonzero values along the \( K \) dimensions, as shown in line 22. Matrix \( A \) is uncompressed, so a zero-value (from Matrix \( A \)) \( \times \) non-zero-value (from Matrix \( B \)) computation can still occur. To completely eliminate any ineffectual computations from zero-value multiplications, both matrices must be compressed. Fig 2c shows a TACO kernel with the CCF combination of \( U_M C_K, U_K U_N \). Both matrices hold position indices (also commonly referred to coordinates) of the nonzero values along the \( K \) dimension, and both indices must match (refer to line 46) to indicate a valid nonzero computation. Fig 2d shows a TACO kernel with the CCF combination of \( U_K C_M, U_K U_N \). Line 57 shows that the kernel

with the CCF combination of \( U_M C_K, U_N C_K \). Both matrices hold position indices (also commonly referred to coordinates) of the nonzero values along the \( K \) dimension, and both indices must match (refer to line 46) to indicate a valid nonzero computation.
is iterating over the uncompressed K dimension, while line 59 and line 61 show that it is iterating over compressed M and N dimension respectively. Different CCFs will generate different TACO outputs. Although the compression format of the output matrix (O) may vary, we default it to fully uncompressed (dense) for the rest of the paper, and can be hidden within the taxonomy unless compressed otherwise. The TACO kernels with different CCFs can be correlated to the computation behaviors of dense and sparse accelerators. The next section will describe more in detail on how Fig 2a,b,c,d,e correlate to TPU [21], EIE [18], ExTensor [19], OuterSPACE [40], and MatRaptor [52] respectively.

III. HARD TACO: SPARSE SUB-ACCELERATORS GENERATOR

This section first introduces different sparse sub-accelerator microarchitectures, each utilizing a TACO kernel discussed in Section II. Then, this section proposes HARD TACO for productive generation of hardware for fast performance, power, and area estimates.

A. Classifying Custom Sparse Accelerators

In this subsection, we use the TACO based taxonomy to classify state-of-the-art sparse accelerators. The examples following show exactly how the compression formats are used for sparse computations, and which matrix dimension(s) is unrolled spatially on hardware, as presented in the most right column in Fig 1. The tensors are compressed in \( (A, B) \) order. 

\( U_M U_K, U_K U_N \) (GEMM, TPU-like). Fig 3a shows an output stationary systolic array [47]. Both input matrices are in dense (uncompressed) format and are fed into the Processing Element (PE) array in a store-and-forward manner. Each PE receives input data from the top and left side, computes a MAC operation, stores the partial sum locally, and forwards out data from the bottom and right side. Once all computations are finished, the completed partial sums are sent to the output accumulation buffer. With a flexible interconnect [15], [19], [28], it is possible to utilize \( M \times N \) PEs in parallel.

\( U_M C_K, U_K U_N \) or \( U_M U_K, U_N C_K \) (SpMM, EIE-like). Based on the accelerator EIE [18], Fig 3b shows a scenario in...
which Matrix A is in dense (uncompressed) format, and Matrix B is in $U_N C_K$ format. Each column of Matrix B (row ids and values) is loaded into the buffer of a PE, hence it is possible to utilize a maximum of N PEs in parallel. Matrix A is streamed through a bus to all PEs. An index comparison module is used to find valid nonzero computations by using the bus position of Matrix A and row ids of Matrix B. The valid computations are then scheduled onto the MAC Queue. Each PE has an output register to accumulate the partial sums. Note that the architecture also support a scenario in which matrix A is compressed in $U_M C_K$ and matrix B is uncompressed.

$U_M C_K, U_N C_K$ (SpGEMM, ExTensor-like). Based on the accelerator Extensor [19] (inner-product), Fig 3d shows Matrix A in $U_M C_K$ format, and Matrix B in $U_N C_K$ format. Comparing each row of Matrix A with every column of Matrix B, Matrix A’s col_ids and B’s row ids go into a hardware intersection unit that quickly finds matching indices. Using the indices, the corresponding values are fetched from both matrices. The values are then distributed through a Network-on-Chip (NoC) to the corresponding PEs for computation. When comparing each row of Matrix A with every column of Matrix B, the maximum PE utilization is N. When comparing each column of Matrix B with every row of Matrix A, the maximum PE utilization is M.

$U_K C_M, U_K C_N$ (SpGEMM, OuterSPACE-like). Based on the accelerators OuterSPACE [40] and SCNN [42] (outer-product), Fig 3d shows a scenario in which Matrix A is in $U_K C_M$ format, and Matrix B is in $U_K C_N$ format. Iterating over the K dimension, the accelerator fetches the indices (row_ids, col_ids) and nonzero data (values) for outer product computation. Each PE owns a partition of the output matrix accumulation, and a NoC sends the fetched input meta(data) to the corresponding PE. Necessary Matrix B’s (meta)data is first loaded into the PEs’ B buffers, and then Matrix A’s (meta)data is streamed in. Each PE also has its own accumulation buffer that contains the partial sums of each output matrix position the PE owns. The indices (row_ids, col_ids) are used to read and write to the correct location.

$U_K C_M, U_N C_K$ (SpGEMM, MatRaptor-like). Based on the accelerator MatRaptor [52] (column-wise-product or Gustavson’s algorithm), Fig 3e shows a scenario in which Matrix A is in $U_K C_M$ format, and Matrix B is in $U_N C_K$ format. Iterating over Matrix B’s columns, a controller reads Matrix A’s columns that corresponds to Matrix B’s row_ids. Each PE owns a column partition of the output matrix, hence the maximum PE utilization is N. Necessary Matrix B’s (meta)data is first loaded into the PEs’ B buffers, and then Matrix A’s (meta)data is streamed in. Matrix A’s col is used to compare with Matrix B’s row_ids to schedule useful computations into the MAC Queue. Matrix A’s row_ids are used to read and write to the correct location within the accumulation buffer. Note that Gamma [59] also uses Gustavson’s algorithm, although Gamma traverses row-wise through the matrices rather than column-wise.

B. Hard TACO Design Flow

Hard TACO generates the sparse sub-accelerators in Section III-A to get fast performance and hardware resource consumption for design space exploration. Fig 4 shows our design flow at a high level. First, matrix multiplication operations using different CCFs are sent as inputs into the TACO compiler. The TACO compiler generates C++ code to the ‘Fine Tuning Stage’ along with user defined hardware constraint parameters, which includes number of PEs, memory type, etc.

The ‘Fine Tuning Stage’ inserts pragmas and reordered the TACO output to meet the hardware constraints. Fig 2 shows where HLS UNROLL pragmas are inserted to unroll a loop spatially, which creates multiple hardware instances for parallel computations. The PIPELINE pragma attempts to achieve low initiation interval within a code block. BIND_OP pragma hints operations to be synthesized using LUTs or DSPs. For this work, we use the BIND_OP pragma to synthesize the accelerator PEs onto the DSPs. ALLOCATE pragma limits how many hardware instances can be generated of a particular compute function. ARRAY_PARTITION pragma determines the local buffer bandwidth by modeling memory instances to behave like SRAMs or registers.

Next, the fine-tuned kernels go directly into the HLS tool. Many HLS tools translate code written in a high level language, such as C++, into RTL. For this work, we use Xilinx Vitis HLS, though we note that any other HLS tool could be used. The outputs include RTL, FPGA hardware consumption, and performance estimates. The RTL then goes through an ASIC flow to get more detailed timing, area, and power reports.

Hard TACO generates quick hardware cost estimates of various sparse sub-accelerators, which become building blocks for a larger heterogeneous accelerator design.

IV. AESPA Architecture Template

This section proposes AESPA, a heterogeneous sparse accelerator. Fig 5 shows the high level architecture template and specification for building AESPA. The die size is capped
at 600 mm², which is approximately the same size as TPU v2 [22]. HBM memory size and bandwidth is set to 32 GB and 1 TB/second respectively. Global scratchpad size and bandwidth is set to 64 MB and 8.192 TB/second respectively. We utilize a highly flexible NoC, often used in previous works [5], [15], [19], [28], to send data from the global buffer to all PEs.

A. Sub-Accelerator Cluster

The conglomerate of sub-accelerator type, memory system, workload dimension, and sparsity ratio determines the operational intensity and performance of a given kernel. AESPA enables flexibility by having various sub-accelerator clusters (shown in Fig 5). The number of PEs in each sub-accelerator cluster is decided based on performance and energy metrics across a diverse workload set. It is a parameter for design space exploration in the evaluation section (Section VII). Using the accelerator template, we create many possible configurations of AESPAs.

The number of PEs also depend on the available area for compute allocated on the die. After accounting for the memory and peripheral logic area, only 202.96 mm² of space is left for compute. Depending the type and quantity of sub-accelerators allocated, the peak TFLOPS/second ranges from 9.98 to 34.56.

B. Flexible Global Buffer

AESPA consists of a double buffered and flexible Global scratchpad which can support flexible-sized partitions for different matrices and sub-matrices (Section V-A). The Global scratchpad is distributed such that each sub-accelerator is backed by one slice of the scratchpad. The Global scratchpad can store matrix and sub-matrix data and meta-data in multiple layouts and multiple compression formats as required by the sub-accelerators. For example, Outer-space like sub-accelerator requires both matrices in a K-major layout with M and N ranks compressed while Extensor-like sub-accelerator requires matrix A in the M-major layout and matrix B in the N-major layout, both matrices having K rank compressed.

C. (De)compressor and Format Conversions

Decompresors are used so that the data in HBM can be stored in a format with low memory footprint [45]. This feature allows faster transfer time and better energy efficiency, as a word of memory transfer from main memory is ~6400× greater in energy consumption than a single integer add operation [18]. It is possible to bypass decompression if the sparse sub-accelerator needs to compute on the compressed format directly. Additionally, format converters are used to enable sub-accelerators under a scenario in which the data transferred from host is compressed in a format that does not match the accelerator’s CCF. For example, a $U_K C_M, U_K C_N$ based accelerator is instantiated, but the input tensor is transferred from host to accelerator as $U_M C_K$; therefore, a $U_M C_K \rightarrow U_K C_M$ hardware block next to the accelerator is required. A typical workaround is to convert the tensors to the right format in the host before transferring, but at the cost of potentially increasing the transfer size. Recent works propose hardware units that do format conversion on the fly [1]. The AESPA template determines the type and quantity of sub-accelerators used to create a large heterogeneous sparse accelerator. Different AESPA configurations are explored in the evaluation section.

V. SCHEDULING FOR AESPA

Scheduling matrix multiplication kernels onto sparse accelerators has its own set of problems. Input tensors are expected to be compressed in a specific format for computation. For example, a $U_M U_K, U_N C_K$ sub-accelerator requires Matrix A to be in $U_M U_K$ and Matrix B to be in $U_N C_K$. Homogeneous accelerators contain PEs that can utilize a specific compute format combination. Heterogeneous accelerators, on the hand, contains different PEs with unique sparse controller and microarchitectures. If the entire tensor matrix is compressed in one format, a portion of the PEs will remain underutilized.

The first scheduling technique (discussed in Section V-A) partitions the input tensors into different compression formats to maximize compute utilization of all sub-accelerators within a heterogeneous accelerator. This maximizes peak performance of a single kernel for latency critical tasks.

The second scheduling technique (discussed in Section V-B) allocates many independent kernels onto to the heterogeneous accelerator in parallel. This is similar in concept to multitenancy proposed in recent works [6], [16].

A. Single Kernel Scheduling (Max TFLOPS) Example

Fig 6 shows the benefit of single kernel scheduling on a single matrix multiplication operation. The examples model a heterogeneous accelerator with four sub-accelerators: $U_M U_K, U_K U_N$ (TPU-like), $U_M U_K, U_N C_K$ & $U_M C_K, U_K U_N$ (EIE-like), $U_M C_K, U_N C_K$ (ExTensor-like),
and $U_K C_M, U_K C_N$ (OuterSPACE-like). Each sub-accelerator has two PEs each for a total of 8 PEs. This example assumes that the system is compute bounded, and that there is sufficient memory bandwidth.

Fig 6a shows a baseline case of $U_M U_K, U_K U_N$. Only the TPU-like sub-accelerator can compute this CDF combination. As a result, 6 of the total 8 PEs remain idle. The runtime is approximated by the number of iterations from the nested loop shown in Fig 2a. In the case of Fig 6a, given that the M, N, K dimensions are all four, the total number of iterations is 64. With two parallel PEs for this TPU-like sub-accelerator, the total execution is 32 cycles.

Fig 6b shows an example with Matrix A split in half across the M dimension. The top half is uncompressed ($U_{M0} U_K$) and the bottom half is compressed in $U_{M1} C_K$. The hybrid format can be preprocessed beforehand, or converted with the hardware format converters found in AESPA. Both TPU and EIE like sub-accelerators are active. Note that the number of iterations for sparse sub-accelerators depends on the sparsity of the input tensor. In Fig 6b, there is approximately one nonzero element per row of $U_{M1} C_K$, which determines the loop count of line 22 of Fig 2. The TPU-like runtime is half of the previous example because the M dimension is split in half. The EIE-like runtime is 4 cycles, calculated by $M1 \times K \times N \times M$ divided by number of PEs.

Fig 6c has Matrix A split across the M dimension and Matrix B split across the N dimension. This scenario activates three out of the four sub-accelerators (TPU-like, EIE-like and ExTensor-like). The TPU-like sub-accelerator cluster has a runtime of 8 cycles, from $M0 \times K \times N0$ / number of PEs.
The EIE-like accelerator is utilized for two computation parts, highlighted in Fig 6c computation 2 and 3. Part 2 runtime is half of Fig 6b’s, as the N dimension is split by half. Part 3 runtime is similar to 2. The total computation cycle for EIE-like is 4 cycles. ExTensor-like runtime is a cycle, approximated by \( M \times K \times N \times MK \) density \( \times KN \) density divided by number of PEs.

Fig 6d is split across the K dimension for both input matrices. The TPU-like runtime is 16 cycles, from \( M \times K0 \times N \) / number of PEs, while the OuterSPACE-like runtime is a cycle, approximated by \( M \times K1 \times N \times MK \) density \( \times KN \) density divided by number of PEs. Since the reduction dimension (K) is split, remaining partial output matrices are merged at the end.

Fig 6e is split across the M, N, and K dimension. This allows all of the sub-accelerator types to compute a single kernel together. The TPU-like sub-accelerator cluster has a runtime of 4 cycles, from \( M0 \times K0 \times N0 \) / number of PEs. The EIE-like accelerator is utilized for two computation parts, highlighted in Fig 6e computation 2 and 3. The runtime for EIE-like is 2 cycles (1 cycle for 2, and 1 cycle for 3). ExTensor-like runtime is a cycle, approximated by \( M1 \times K0 \times N1 \times MK \) density \( \times KN \) density divided by number of PEs. OuterSPACE-like runtime is a cycle, similar to that of Fig 6d. Since the reduction dimension (K) is split, remaining partial output matrices are merged at the end.

Our single kernel scheduling strategy for heterogeneous sparse accelerators enables high utilization for all available PEs of various sub-accelerator types. As shown in Fig 6e, the strategy improves performance, which is important for latency critical kernels. The performance benefit depends on the AESPA configuration, memory bandwidth, and workload. (Discussed in more detail in (Section VII).

### TABLE I: Tensor characteristics found in various applications.

| Name           | Application             | Dimension (M,K,N) | Density % |
|----------------|-------------------------|-------------------|-----------|
| chem97ZtZ      | Stat Problem            | 2.5k×2.5k×1.2k    | 0.11,100  |
| journals       | Weighted Graph          | 124×124×62        | 78.5,100  |
| m3plates       | Acoustics               | 11k×11k×5.5k     | 0.0054,100|
| synthetic dense| Varies                  | 5k×5k×2.5k       | 100,100   |
| bibt_8i_3      | Combinatorial           | 3.2k×83k×43k     | 0.093,100 |
| speech         | Deep Learning           | 7.7k×2.6k×1.3k   | 5,100     |
| gnn            | Deep Learning           | 1.6k×K×36k       | 50,30     |
| transformer    | Deep Learning           | 32k×84×1k        | 50,30     |
| citeseer       | GNN                     | 3.3k×3.3k×3.7k   | 0.11,0.85 |

### B. Many Kernels Scheduling Example

For large datacenters, it is common to have many kernels in a queue waiting to be executed. Rather than partitioning the tensors into hierarchical formats to achieve high TFLOPS/second per kernel as observed in the ‘single kernel scheduling’, ‘many kernels scheduling’ optimizes for multiple kernels, each with tensors compressed in one format. Fig 7 shows a high level figure with four matrix multiplication kernels in the task queue. The figure also shows an AESPA configuration of four sub-accelerator types (TPU, EIE, ExTensor, and OuterSPACE-like) with 16 PEs each.

The first task (red) is ideal for the TPU-like sub-accelerator. This is because the tensors are completely dense, and all 16 PEs can be utilized from the M \( \times N \) bound (refer to the parallelism dimension bound table in Fig 1). The second task (blue) is ideal for the EIE-like sub-accelerator. This is because the M dimension can be fully unrolled onto the PEs, and there is one input matrix that is relatively sparse. The third (green) and fourth (orange) tasks have two matrices that are relatively sparse, so they run more efficiently on sub-accelerators that support SpGEMM. The third (green) has a K dimension that can fully unrolled onto an OuterSPACE-like sub-accelerator, and the fourth (orange) has a N dimension that can be fully unrolled onto an ExTensor-like sub-accelerator.

Our many kernel scheduling strategy enables good utilization for multiple kernels running in parallel. However, this again depends heavily on the memory bandwidth, workload, and AESPA configuration. (Discussed in more detail in (Section VII).

### VI. METHODOLOGY

We first model each basic sub-accelerator class (refer to Sec III-A) using the Hard TACO design flow. For HLS tool, we used Xilinx Vitis and ran hardware emulation on Alveo U50. Functional correctness was verified for all sub-accelerators. We get the RTL, estimated FPGA hardware resource consumption and performance from Vitis. The generated RTL then goes through an ASIC flow using 28nm technology for a more detailed area, power, and timing report. Synopsys DC compiler was used for synthesis and Cadence Innovus was used for place and route.

The hardware generation time on Vitis was significant when modeling large designs (128 PEs +), so we designed small sub-accelerator cores, each utilizing 16 int32 PEs. Each core was...
also implemented to have a local buffer, which stores three 16 × 16 tiles (one for each tensor operand). The local buffer size is different for sparse sub-accelerators as they require more metadata storage. Floating point units were not enabled when generating the sub-accelerators from Vitis. To approximate the cost of enabling floating point operations, we add the ASIC area and power costs of our internal FP units to the post-ASIC flow sub-accelerator reports. We scale the area and power of the generated small sub-accelerator units to larger designs (4196 PEs +) linearly. Though not realistic, we believe that it is still a fair estimation, given each generated sub-accelerator is self sufficient on its own (contains its own local buffers and controllers). With the generated sub-accelerators, we are able to approximate the amount of TFLOPS/s achievable given an area constraint.

To generalize how an architecture will behave for realistic workloads (HPC [9], DNN [10], and GNN [24], [57]) shown in Table I, we developed an analytical model that approximates the performance by first estimating the tripcount of the compute loop of each matrix multiplication kernel shown in Fig 2. The number of iterations depend on the tensor dimension and sparsity. We assume uniform random sparsity. The memory bandwidth of the AESPA system is also integrated into the model, as sparse computations are often memory bounded [19], [52], [62]. For energy cost, we consider the utilization of the accelerator and the on-chip data movement.

To schedule operations onto heterogeneous accelerators, we conduct a search to find the best way to partition/configure a certain operation derived from our proposed strategies. For simplicity, we assume that the data compressed in the desired format(s) is sent directly from the host. Different configurations of AESPA are evaluated against state-of-the-art accelerator designs presented in Fig 1.

VII. EVALUATION

This section first analyzes the sub-accelerator costs using HARD TACO. Then, we evaluate the performance of AESPA with our scheduling techniques against state of the art accelerator designs.

A. Hard TACO Reports

Fig 8 shows the Xilinx U50 FPGA results on different sub-accelerators. There are 16 PEs in each HLS design, hence why there are 16 DSPs. The number of FFs is high for ExTensor and MatRaptor-like sub-accelerators, while the number of LUTs is high for ExTensor, OuterSPACE, and MatRaptor-like sub-accelerators. TPU-like design has the least number of FFs and LUTs. This is intuitive because it does not need any extra metadata controller or index indirections that are required in sparse sub-accelerators. This TPU-like property is confirmed by the initiation interval of 1. An initiation interval of 1 means that it is completely pipelined, while a high initiation interval will induce a lot of stalls. EIE, Extensor, and MatRaptor-like all have initiation intervals of 17, 17, and 16 respectively. OuterSPACE-like design has a relatively lower initiation interval of 6. The period of ExTensor-like on the FPGA is almost 2× greater than the others. The inner product dataflow that ExTensor implements contain lots of metadata intersections, which may not be efficient on the FPGA fabric.

To gain better understanding on the sub-accelerator designs, we synthesize the generated RTL on a 28nm process. Fig 9 shows the area and power report. All sub-accelerators met timing at 1 GHz. Floating point units overhead are added on top. Additionally, 32 32-bit wide FIFOs of depth 10 are added per initiation interval. This is a rough estimate to predict what the sub-accelerator overhead would be if it is fully pipelined with custom ASIC implementations. ExTensor-like’s area is the largest, with almost 3× greater than a TPU-like design. MatRaptor-like design is the most power-hungry among all, while OuterSPACE-like design is relatively low in area and power. We emphasize that custom hand-designed ASIC implementations may differ from the results gathered from the HLS tool, though we believe they are fair estimates of the building blocks for design space exploration. We utilize the area overhead of each sub-accelerator to find the peak TFLOPS/second of various accelerator types shown in Fig 1.

B. AESPA Single Kernel Scheduling Evaluations

Fig 10 and Fig 11 shows how AESPA compares to other baselines when computing individual matrix multiplications.
Fig. 10: Evaluation against Homogeneous EIE-like with limited memory bandwidth. (a) shows speedup and effective utilization. (b) shows normalized energy and EDP improvement.

Fig. 11: Evaluation against Homogeneous EIE-like with unlimited memory bandwidth. (a) shows speedup and effective utilization. (b) shows normalized energy and EDP improvement.

The first six baselines are homogeneous accelerators. A homogeneous accelerator only contain one type of sub-accelerator. We also compare against a homogeneous hybrid design, in which the sub-accelerator can support the dataflows of all TPU-like, EIE-like, and ExTensor-like. The cost of this flexibility is extra area and power, which then reduce the peak TFLOPS/s achievable under an area constraint. Fig 1 shows that the TFLOPS/s of a homogeneous hybrid is just 8.96. For heterogeneous designs (AESPA), it is possible to achieve flexibility while still using basic sub-accelerators that can only support one type of sparse dataflow.

Fig 10 and Fig 11 show performance graphs with 1 TB/s and unlimited memory bandwidth respectively. Both figures Part A shows the speedup over Homogeneous EIE-like design on the left Y axis and effective utilization on the right Y axis. Effective utilization is the percentage of effectual work done by the accelerator. It depends on (1) the parallelism dimension bound and the sparsity support the sub-accelerator enables (shown in Fig 1). Part B left Y axis shows the energy efficiency improvements over a Homogeneous EIE-like design, and the right Y axis shows the normalized EDP improvement.

M3plates (refer to Table I) has a very sparse Matrix A. The operational intensity is low and gets limited by the memory bandwidth, as shown by the low utilization points across all
designs in Fig 10a. Fig 11a shows that with unlimited bandwidth, the performance utilization points increase drastically. Homogeneous TPU-like’s utilization is still low because it does not have any sparsity support. Citeseer also follows a similar pattern. Fig 10a shows significant performance degradation for Homogeneous Outerspace-like on Transformer. This is because the K dimension for the workload is small (value of 84), and Outerspace-like is generated with the K dimensions unrolled spatially; therefore, the utilization is bounded by the dimension of the workload. AESPA is able to have variable parallelism bounds, hence why AESPA (Half TPU/Outerspace) is able to achieve higher utilization. We compared against four configurations of AESPA, the first three have fixed ratios of sub-accelerators, while the last is the highest performance configuration searched by our model. Homogeneous hybrid has the highest effective utilization, for both limited and unlimited bandwidth. However, the smaller peak TFLOPS/s prevent it from obtaining larger speedup.

AESPA with our single kernel scheduling strategy is able to achieve 1.96× speedup and 7.9× EDP geometric improvement over Homogeneous EIE-like at a 1 TB/s memory bandwidth. With unlimited bandwidth, AESPA is able to achieve 3.3× speedup and 14.1× EDP geometric improvement. Against a Homogeneous Hybrid design, AESPA achieves 1.03× speedup and 1.28× EDP geometric improvement. With unlimited bandwidth, it becomes 1.13× speedup and 1.20× EDP geometric improvement.

C. AESPA Many Kernel Scheduling Insights

Rather than achieving peak performance for a single kernel, as shown in the previous section, it is also possible to run multiple kernels in parallel on AESPA. The workload characteristics and resource availability determine which kernel gets mapped to which sub-accelerator cluster. In Fig 12, we evaluated all designs with unlimited bandwidth. AESPA is able to stay within 6% of the best baseline configuration for total runtime. With limited bandwidth, we observe more memory contention across parallel kernels, significantly impacting performance. We note that this analysis is very dependent on the workloads given, but it shows that there are many valid ways to run applications on a heterogeneous sparse accelerator.

VIII. RELATED WORK

Pre-RTL accelerator DSE: Aladdin is a pre-RTL, power-performance accelerator simulator [49]. Aladdin is an alternate methodology to HARD TACO to quickly get hardware and performance estimates. Interstellar [58], MAESTRO [26] and Timeloop [41] are analytical performance models for DNN accelerators. Herald [27] is an optimization framework for heterogeneous accelerator substrates for dense DNN workloads. It finds the optimal resource allocation for multiple-sub accelerators and determines the optimal schedule of multi-DNN workloads on the dense heterogeneous substrate. However, Herald only looked into dense accelerators, while we expand it to sparse accelerators. Numerous other works look into exploring parallelism for popular workloads [4], [12], [20], [51], [56].

Accelerator RTL Generators: Spiral is a HLS wrapper for FFTs [14] and MAGNet is a modular accelerator generator for neural networks [54]. DeepBurning-GL is a framework that generates different accelerators for GNNs. [34]: Hard TACO takes a unique approach by utilizing the output of an established sparse tensor compiler [8] to generate RTL. This allows people with compiler/algorithms background to intuitively understand what each sparse sub-accelerator is doing and their differences.

Sparse accelerators: Sparsity has been a key optimization target for HPC and AI workloads. Numerous accelerators have been proposed for SpMM and SpGEMM acceleration [2], [5], [11], [15], [17], [18], [19], [23], [29], [32], [34], [35], [39], [40], [43], [50], [52], [53], [56], [60]. Though there are a lot of unique sparse accelerators, we believe that they can all be grouped into classes based on their computation dataflow.

Recent works look into co-designing for sparse architectures. Sanger prunes the attention matrix for its reconfigurable architecture to exploit [36]. ESCALATE utilized kernel decomposition to accelerate CNN models [33]. G-Cos does a co-search on both the GNN and the accelerator to maximize accuracy and hardware efficiency. The authors also looked into sub-architecture designs with various sparse dataflows [61]. SpAtten does pruning and quantization to achieve high energy efficiency [55].

IX. FUTURE WORKS AND DISCUSSION

There is a wide range of sparse accelerators presented in industry and academia, each with some unique optimizations that cannot be modeled efficiently with HLS. These optimizations include load balancing mechanisms, structured sparsity support, etc. Although HLS is perfect for fast architecture exploration, it is more realistic to build custom IPs for deployment. Additionally, the field of scheduling on heterogeneous sparse accelerators is relatively unexplored compared to its dense counterpart. There are numerous opportunities for new hierarchical compression formats to utilize different sparse sub-accelerators.
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