High-Precision Tuning of State for Memristive Devices
by Adaptable Variation-Tolerant Algorithm

Fabien Alibart\textsuperscript{1}, Ligang Gao\textsuperscript{1}, Brian Hoskins\textsuperscript{2}, and Dmitri Strukov\textsuperscript{1}

\textsuperscript{1}Department of Electrical and Computer Engineering
\textsuperscript{2}Materials Department
University of California Santa Barbara
Santa Barbara, CA 93106, USA

Abstract
Using memristive properties common for the titanium dioxide thin film devices, we designed a simple write algorithm to tune device conductance at a specific bias point to 1\% relative accuracy (which is roughly equivalent to 7-bit precision) within its dynamic range even in the presence of large variations in switching behavior. The high precision state is nonvolatile and the results are likely to be sustained for nanoscale memristive devices because of the inherent filamentary nature of the resistive switching. The proposed functionality of memristive devices is especially attractive for analog computing with low precision data. As one representative example we demonstrate hybrid circuitry consisting of CMOS summing amplifier and two memristive devices to perform analog multiply and accumulate computation, which is a typical bottleneck operation in information processing.

Keywords: Resistive switching, thin film metal oxide, memristor, analog computation
In order to fully realize analog properties of resistive switching devices [Saw08, Was09, Per11, Kim11, Yan09, Lik08], which are also called “memristive devices” [Chu11], one has to deal with significant variations in the switching behavior. In some applications such variations can be tolerated by the structure of the circuits, such as the case with some versions of artificial neural networks in which memristive devices are implementing synapses [Lik11, Sni07, Yu11b, Seo11, Cha11, Jo10a]. However, for all other applications, e.g., multilevel memory [Bec00, Yu11a, Cho06], configurable filters [Dri10], and analog computing circuits (see, e.g., various theoretical proposals in Refs. [Wei11, Shi11, Per10, Lai10, Pro10]), the performance directly depends on how accurately the resistive state can be set.

A natural way to tackle variations in switching behavior is to utilize active feedback scheme, e.g. applying iterative write and read (test) pulses to converge to certain desired conductive state of the device. Such scheme has been successfully applied to phase change memories to achieve multilevel memory operation [Pap11, Bed09]. A similar idea to use closed-loop circuitry has been proposed and theoretically simulated using Spice model for TiO$_2$ devices [Yi11]. In this paper, we experimentally demonstrate a simple feedback algorithm which takes into account specific memristive behavior of titanium dioxide devices to tune resistance state of the device within 1% relative accuracy within all the dynamic range. We then use our algorithm to demonstrate one of the most important operations in information processing - analog multiply and accumulate (MAC).

The Pt/TiO$_2$(30nm)/Pt devices have been implemented in “bone-structure” geometry with active area $\sim$ 1 $\mu$m$^2$ by atomic layer deposition technique (see supplementary information for details). The electrical measurements were carried out with a B1500 Agilent parameter analyzer in ambient conditions.
Figure 1 shows typical resistive switching in titanium dioxide devices. The full loop is obtained by quasi-DC triangular voltage sweep between 0 and -1.5V followed by a quasi-DC triangular current sweep between 0 and 750 µA with a sweeping period of about 4s. Alternatively, the device can be switched continuously between ON and OFF states. The incremental RESET switching is obtained by applying voltage sweeps of increasing amplitude from -0.8V to -1.5V with a step of 10 mV. Similarly, incremental SET transition is obtained with current sweeps of increasing amplitude from 100 to 750 µA with a step of 50 µA.

A more accurate control of the device is possible using sequence of relatively large amplitude write pulses followed by smaller non-disturbing read pulses [Pic09]. Note that for all experiments described below we use voltage-controlled pulses for SET switching also. The main reason is that current-controlled switching (or alternatively the utilization of a compliance transistor) is not compatible for large scale crossbar circuits, even though it could be more natural for SET switching in the context of single devices because it allows avoiding overshooting and overheating. In particular, the measurement is composed of two different sequences of pulses: (i) the read pulses of -200 mV and 1 ms width are used to probe the state of the device which is represented by the resistance or by current measured at -200 mV) and (ii) the write pulses which are used to change the state of the memristive device, whether by changing the pulse width and/or the pulse amplitude. The two pulses (read and write) are alternated at a frequency of 0.5 Hz to prevent the accumulative Joule heating effect from single write pulses.

Figure 2 shows the evolution of the state as a function of both the write pulse amplitude and cumulative time (i. e. summation of the write pulses duration). Before the pulse measurements, the devices are set to a low (high) resistance state with a quasi-DC current (voltage) control loop in order to start the SET (RESET) transition from the same initial state.
condition. In particular, on Figure 2a each curve shows the dynamic evolution of the device's state, as a result of the application of fixed amplitude pulses with an exponentially increasing duration from 200 ns to 1 ms. Figures 2c and d show in detail the dynamic evolution of the device’s state for the most relevant stress conditions (i.e. faster switching) for RESET and SET transition, respectively, when both the amplitude and the width of the write pulses are fixed (a constant pulse width of 200 ns has been used in these measurements).

Figures 2a, b, c clearly demonstrates that the device can be switched fast - of the order of 1 us for both transitions for maximum applied voltages and retain its state for at least longer than 1 s if the applied voltage is within (-0.6 V < v < 0.5 V) region. Moreover, Figures 2b, c highlights that the switching dynamics is exponential with voltage for SET switching and roughly follows power low for RESET (at least before it saturates) – See supplementary information for more details on fitting. This is similar to previously reported dynamics [Pic09] – though it should be noted that in our case the state is defined as a conductance (or resistance) at specific bias rather than phenomenological parameter such as barrier width. Our experimental results support that the retention (at, say -0.2V) to write ratio (at maximum amplitude) is at least larger than $10^6$ but likely to be much higher. First of all, we did not apply stress long enough to see significant drift of the state so that the retention time is certainly longer. Secondly, exponential nature of SET dynamics is most likely a result of thermal effects [Stra11, Bor09, Shk09, Iel11]. As a result, the switching time could be made much faster if larger write voltages are applied [Iel11, Pic09, Str09]. In our case we avoid checking this hypothesis because experimental setup does not allow applying short pulses, while relative long high-amplitude pulses lead to overstressing and damaging of the device.
While the general dynamics for all our devices after forming is qualitatively similar there are significant variations – both from device to device and for the same device upon cycling, which prevents from using calculated stress voltage to drive the device to the desired state. In principle, such variations can be coped with by overstressing the device when only two extreme resistive states in the device are needed. To tune the device to a specific intermediate state overstressing strategy is clearly not an option and instead we use the feedback algorithm. Our algorithm is based on the fact that large-amplitude pulses can be used to reach desired state faster but also at much cruder precision (Figs. 2 a, b, c) due to the fixed minimum pulse duration (which is limited by experimental setup). Once the device is driven close to the vicinity of the desired state smaller amplitude pulses can be used for fine tuning. (Note that using pulses of relatively small fixed amplitude only is not an attractive option because it may require exponentially long write time.) To take advantage of such switching dynamics our algorithm (Fig. 3) is based on a sequence of increasing amplitude voltage ramps of appropriate polarity (which depends on the initial and the desired state of the devices). In particular, we apply 10 µs-long voltage pulses (starting from 0.5V for the SET sequence and starting from -0.5V to the RESET sequence) with a step of 5mV. Similar to previous measurements the device state is checked with read pulse after each write pulse and the voltage ramp is applied until it reaches and overshoots the desired state. At this point the new voltage ramp of opposite polarity is started. Because this time the initial state is closer to the desired one the maximum amplitude of the voltage pulse in the new ramp (i.e. before the ramp is stopped) is smaller which in turn ensures even better precision. Using this algorithm we were able to tuned the device to 1% precision with respect to the desired state within the whole dynamic range of the device (Fig. 3a).
In principle, even more accurate tuning might be possible by using more ramps (i.e. more time) though in this particular experiment we stopped our algorithm when 1% accuracy was achieved.

Theoretically, i.e. from physical noise analysis, any computation at signal precision below 8-bit (for robotics, distributed sensor networks applications, etc.) could be done much more efficiently in analog or mixed signal circuits [Str07], with wires carrying multiple bits of information [Sar98]. However, even low precision analog processing in conventional CMOS technology is cumbersome, due to the lack of suitable hardware, e.g. to implement multilevel (analog) weights. On the other hand, low precision analog information processing can be implemented with hybrid circuits, which combine single conventional CMOS chip and layer(s) of quasi-memristive devices [Lik08]. Figure 4 illustrates such circuit consisting of discrete chip CMOS summing amplifier and two memristive devices programmed to high precision state with proposed algorithm (See supplementary info). In particular, to realize MAC circuits, the memristive devices implement density-critical configurable low precision weights, while CMOS is used for the summing amplifier, which provides gain and signal restoration. As a result, individual voltages applied to memristive device can be multiplied by the unique weight (conductance) of memristor and summed up by CMOS amplifier - all in analog fashion.

The results demonstrated on Figures 1-4 are for microscale devices, however we strongly believe that it can be sustained in nanoscale devices based on previously reported experimental scaling analysis [Lee11] and the fact that forming process produces nanoscale filaments with active area localized to few nanometers spots [Stra10, Kwo10]. In fact, the nanoscale memristive devices have typically less variations [Jo10b] and, therefore, we expect better precision could be achieved within shorter amount of time using our algorithm.
It is also worth mention that our algorithm was studied in the context of single devices. In the passive crossbar structures semi-selection and leakage currents might present additional challenges. However, at least the former issue should not be a problem for our devices because of the strong nonlinearity in the switching dynamics (Fig. 2a). Also, while there is a natural tradeoff between the tuning time and resulting accuracy one can expect certain physical limit to the precision, e.g. defined by the shot ionic noise and temporal instabilities, which is certainly worthwhile investigating.

Acknowledgments

We thank Konstantin Likharev and Ashok Ramu for helpful discussions. This work was supported via NSF grant NSF grant CCF-1028336.
Figure 1: Typical $I$-$V$ showing incremental resistive switching of the TiO$_{2-x}$ thin film. The RESET is obtained by a sweep of voltage between 0 and -1.5V and the SET by a sweep of current between 0 and 750uA.
Figure 2: Switching dynamics characterized by voltage pulse stress with variable amplitude and duration. Panel (a) shows general switching behavior and volatility characteristics over large duration range. Panels (b) and (c) show detailed transitions over shorter (and more relevant duration range for write operation) and with fitting curves for SET and RESET transitions, correspondingly. Note that before each measurement, the device is set to the same high (low, respectively) resistance state by a voltage (current) sweep.
Figure 3: Tuning of the device state within 1% accuracy: (a) Demonstration of the algorithm to tune the resistive state of the device to 7µA, 15µA, 30µA, 60µA, 120µA within an accuracy of 1% using the algorithm shown on panel (b). Panel (c) shows zoom-in of the particular intermediate state.
**Figure 4:** Illustration of analog multiply and add circuitry operation with CMOS summing amplifier and memristive devices set with high precision with proposed algorithm.
References

[Bec00] A. Beck, J.G. Bednorz, Ch. Gerber, C. Rossel, and D. Widmer, “Reproducible switching effect in thin oxide films for memory applications”, Applied Physics Letters, vol. 77 (1), pp. 139-141, 2000.

[Bed09] F. Bedeschi, R. Fackenthal, C. Resta, E.M. Donze, M. Javasivanami, E. C. Buda, F. Pellizzer, D.W. Chow, A. Cabrini, G. M. A. Calvi, R. Faravelli, A. Fantini, G. Torelli, D. Mills, R. Gastaldi, and G. Casagrande, “A bipolar-selected phase change memory featuring multi-level cell storage”, IEEE Journal of Solid-State Circuits, vol. 44(1), pp. 217-227, 2009.

[Bor09] J. Borghetti, D.B. Strukov, M.D. Pickett, J.J. Yang and R.S. Williams, “Electrical transport and thermometry of electroformed titanium dioxide memristive switches”, Journal of Applied Physics, vol. 106, pp. 124504, 2009.

[Cha11] T. Chang, S.-H. Jo, K.-H. Kim, P. Sheridan, S. Gaba, and W. Lu, “Synaptic behaviors and modeling of a metal oxide memristive device”, Applied Physics A, vol. 102, pp. 857-863, 2011.

[Cho06] D. Choi, D. Lee, H. Sim, M. Chang, and H. Hwang, “Reversible resistive switching of SrTiO\textsubscript{x} thin films for nonvolatile memory applications”, Applied Physics Letters, vol. 88, art. 082904, 2006.

[Chu11] L. O. Chua, “Resistance switching memories are memristors”, Applied Physics A, vol. 102, pp. 765-783, 2011.

[Dri10] T. Driscoll, J. Quinn, S. Klein, H.T. Kim, B. J. Kim, Y.V. Pershin, M. Di Ventra, and D.N. Basov, “Memristive adaptive filters”, Applied Physics Letters, vol. 97, art. 093502, 2010.
[Iel11] D. Ielmini, F. Nardi, and C. Cagli, “Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories”, *Nanotechnology*, vol. 22, art. 254022, 2011.

[Jo10a] S. H. Jo, T. Chang, I. Ebong, B. Bhavitavya, P. Mazumder and W. Lu, “Nanoscale memristor device as synapse in neuromorphic systems”, *Nano Lett.*, vol. 10, pp. 1297-1301, 2010

[Jo10b] K.-H. Jo, C.-M. Jung, K.-S. Min, and S.-M. Kang, “Self-adaptive write circuit for low-power and variation-tolerant memristors”, *IEEE Transactions on Nanotechnology*, vol. 9(6), 2010.

[Kim11] K. M. Kim, D. S. Jeong, and C. S. Hwang, “Nanofilamentary resistive switching in binary oxide systems; a review on the present status and outlook”, *Nanotechnology*, vol. 22, art. 254002, 2011.

[Kwo10] D.-H. Kwon, K. M. Kim, J. H. Jang, J.M. Jeon, M.H. Lee, G.H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim and C. S. Hwang, “Atomic structure of conducting nanofilaments in TiO$_2$ resistive switching memory,” *Nature Nanotechnology*, vol. 5, pp. 148-153, 2010.

[Lai10] M. Laiho and E. Lehtonen, “Arithmetic operations within memristor-based analog memory”, in: *Proc. International Workshop on Cellular Nanoscale Networks and Their Applications*, Berkley, CA, February 2010, pp. 1-4.

[Lee11] J. Lee, J. Park, S. Jung, and H. Hwang, “Scaling effect of device area and film thickness on electrical and reliability characteristics of RRAM”, in: *Proc. International Technology Conference and Materials for Advanced Metallization*, Dresden, Germany, May 2011, pp. 1-3.
[Lik08] K.K. Likharev, “Hybrid CMOS/nanoelectronic circuits: Opportunities and challenges”, *J. Nanoelectronics and Optoelectronics*, vol. 3, pp. 203-230, 2008.

[Lik11] K.K. Likharev, “CrossNets: Neuromorphic hybrid CMOS/nanoelectronic networks”, Science of Advanced Materials, vol. 3, pp. 322-331, 2011.

[Pap11] N. Papandreou, H. Pozidis, A. Pantazi, A. Sebastian, M. Breitwisch, C. Lam, and E. Eleftheriou, “Programming algorithm for multilevel phase-change memory”, in: *Proc. IEEE International Symposium on Circuits and Systems*, Rio de Janeiro, Brazil, May 2011, pp. 329-332.

[Per10] Y. V. Pershin and M. Di Ventra, “Practical approach to programmable analog circuits with memristors”, *IEEE Transactions on Circuits and Systems – I*, vol. 57 (8), pp. 1857-1864, 2010.

[Per11] Y.V. Pershin and M. Di Ventra, “Memory effect in complex materials and nanoscale systems”, *Advances in Physics*, vol 60, pp. 145-227, 2011.

[Pic09] M. Pickett, D.B. Strukov, J. Borghetti, J. Yang, G. Snider, D. Stewart, and R.S. Williams, “Switching dynamics in a titanium dioxide memristive device”, *J. Applied Physics*, vol. 106, art. 074508, 2009.

[Pro10] T. Prodromakis and C. Toumazou, “A review on memristive devices and applications”, in: Proc. *IEEE International Conference on Electronics, Circuits, and Systems*, Athens, Greece, Dec 2010, pp. 934-937.

[Sar98] R. Sarpeshkar, “Analog versus digital: Extrapolating from eletronics to neurobiology”, *Journal of Neural Computation*, vol. 10 (7), pp. 1601-1638, 1998.

[Saw08] A. Sawa, “Resistive switching in transition metal oxides”, *Materials Today*, vol. 11, pp. 28-26, 2008.
[Seo11] K. Seo, I. Kim, S. Jung, M. Jo, S. Park, J. Park, J. Shin, K. R. Biju, J. Kong, K. Lee, B. Lee, and H. Hwang, “Analog memory and spike-timing-dependent plasticity characteristics of a nanoscale titanium oxide bilayer resistive switching device”, *Nanotechnology*, vol. 22, art. 254023, 2011.

[Shi11] S. Shin, K. Kim, and S.-Mo Kang, “Memristor applications for programmable analog ICs”, *IEEE Transactions on Nanotechnology*, vol. 10, (2), pp. 266-274, 2011.

[Shk09] A. Shkabko, M. H. Aguirre, I. Marozau, T. Lippert, and A. Weidenkaff, “Measurements of current-voltage-induced heating in the Al/SrTiO$_{3-x}$N$_y$/Al memristor during electroformation and resistance switching”, *Appl. Phys. Lett.*, vol. 95, art. 152109, 2009.

[Sni07] G.S. Snider, “Self-organized computation with unreliable, memristive nanodevices”, *Nanotechnology*, vol. 18, art. 365202, 2007.

[Str07] D.B. Strukov and K.K. Likharev, “Hybrid CMOS/nanodevice circuits for digital signal processing”, *IEEE Trans. Nanotechnology*, vol. 6, pp. 696-710, 2007.

[Str09] D.B. Strukov and R.S. Williams, “Exponential ionic drift: Fast switching and low volatility of thin film memristors”, *Applied Physics A*, vol. 94, pp. 515-519, 2009.

[Stra10] J.P. Strachan et al., “Direct identification of the conducting channels in a functioning memristive device”, *Advanced Materials*, vol. 22, pp. 3573-3577, 2010.

[Stra11] J.P. Strachan, D.B. Strukov, J. Borghetti, J.J. Yang, G. Medeiros-Ribeiro, and R.S. Williams, “The switching location of a bipolar memristor: Chemical, thermal, and structural mapping”, *Nanotechnology*, vol. 22, art. 254015, 2011.
[Yan09] J.J. Yang, M.D. Pickett, X. Li, D.A.A. Ohlberg, D.R. Stewart, and R.S. Williams, “Memristive switching mechanism for metal/oxide/metal nanodevices”, *Nature Nanotechnology*, vol. 3, pp. 429-433, 2009.

[Yi11] W. Yi, F. Perner, M.S. Qureshi, H. Abdalla, M.D. Pickett, J.J. Yang, M.-X.M. Zhang, G. Medeiros-Ribeiro, and R.S. Williams, “Feedback write scheme for memristive switching devices”, *Applied Physics A*, vol. 102, pp. 973-982, 2011.

[Yu11a] S. Yu, Y. Wu, H.-S. P. Wong, “Investigation the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory”, *Applied Physics Letters*, vol. 98, art. 103514, 2011.

[Yu11b] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H.-S. P. Wong, “An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation”, *IEEE Transactions on Electron Devices*, vol. 58 (8), pp. 2729-2736, 2011.

[Was09] R. Waser, R. Dittman, G. Staikov, K. Szot, “Redox-based resistive switching memories – nanoionic mechanisms, prospects, and challenges”, *Advanced Materials*, vol. 21, pp. 2632-2663, 2009.

[Wei11] T.A. Wei and W.D. Jemison, “Variable gain amplifier circuit using titanium dioxide memristors”, *IET Circuit, Devices & Systems*, vol. 5 (1), pp. 59-65, 2011.
Device fabrication

The Pt/TiO₂(30nm)/Pt devices have been implemented in “bone-structure” geometry with active area ~ 1 µm² (fig. S1). An evaporated Ti/Pt bottom electrode (5nm/25nm) has been patterned by conventional optical lithography technique on a Si/SiO₂ substrate (500 µm/200 nm, respectively). Then, a 30 nm TiO₂ switching layer has been realized by atomic layer deposition at 200°C using Titanium Isopropoxide (C₁₂H₂₅O₄Ti) and water as a precursor and reactant, respectively. A Pt/Au electrode (15nm/25nm) was evaporated on top of the TiO₂ blanket layer. A rapid annealing of the device was finally applied at 500° C under N₂ and N₂+O₂ atmosphere for 5 min to improve the crystallinity of the TiO₂ material.

Electrical characterization

We used conventional 2-probe technique for the electrical characterization of the device because electrode resistance is much smaller (~of the order 80 Ω) compared to that of the ON-state of the
device. Each device was formed by a negative voltage sweep between 0 and -10V (the forming voltage was around -8V) and a current compliance of 300 µA ensured by a transistor connected in series to the TiO₂ device. After this forming process, the compliance transistor is removed. Few sweeps between -1.5 V and 1.5 V were applied before obtaining a stable bipolar behavior of the device.

The extended wave form capability of the tool (B1530) was used for the pulse measurement presented in this paper (sampling rate of 10 ns and rise/fall time between 0 and 5V of 80 ns). The Op-amp circuit was realized with a TL072 op amp. During the programming, the devices are disconnected from the OpAmp circuit and programmed using the high precision algorithm setup (B1530 wave form generator and measurement unit). After programming the devices are connected externally to the CMOS chip and the output is measured with an oscilloscope (Agilent 3000 series) while the input pulses are generated with a waveform generator (Agilent 33520).

The state of the devices on MAC circuit where set to 15, 30 and 60uA (read current at -200mV).

- Fitting of SET and RESET transitions

We present in this paper the fitting of both SET and RESET transitions. The physical interpretation of the fitting is beyond the scope of this paper and will necessitate more detail analysis and measurements. We are only interesting in the phenomenological behavior and trends of both transitions in order to implement an effective algorithm using the two transitions in an analog way.

We describe the current during the RESET transition with a power law

\[ I = A_0 t^{-\beta} \]
where $\beta$ and $A_0$ are function of voltage $V$. Figure 2b shows the good agreement between measurement and fitting and figure S2 present the dependence of $A_0$ and $\beta$ with voltage.

The current during the SET transition has been fitted with a sigmoidal function:

$$I = A_0 + \frac{A_1 \ln(Bt + 1)}{1 + e^{-\frac{1}{\tau_1}(t-\tau_2)}}$$

Where $A_0$ and $A_1$ are constant ($9 \times 10^{-6}$ A and $7.84 \times 10^{-5}$ A, respectively) fixe to the same value for all the SET transitions and $B$, $\tau_1$ and $\tau_2$ depends on voltage $V$. We present in figure 2c the fitting of the measurement and in figures S3 a and b the dependence of $B$, $\tau_1$ and $\tau_2$ with voltage. The first stage of the SET transition is well described by an exponential dependence with time (at least before the pseudo saturation that follows a logarithmic dependency). We can also underline the exponential dependence of $\tau_1$ (equivalent to the time for switching) and $\tau_2$ (equivalent to the time for starting switching) with voltage that is consistent with the extrapolation of ns switching time for TiO$_2$ devices.

Figure S2: fitting parameters of the RESET transition
Figure S3 a and b: fitting parameters of the SET transition