On-chip jitter tolerance measurement technique with independent jitter frequency modulation from VCO in CDR

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Abstract: We present an on-chip measurement technique to characterize the jitter tolerance of a clock and data recovery (CDR) circuit. The proposed jitter modulation scheme incorporates a modulated-charge-pump and a pulse generation circuits to apply a periodic triangular form voltage directly to the control voltage of CDR circuit. This jitter frequency generation scheme independent from the VCO in the CDR allows a wide and linear control of jitter. The modulated jitter amplitude range was 0.05–2 UIpp at 10 MHz, and the jitter frequency range was 100 KHz–20 MHz. The circuit was fabricated in 65 nm CMOS, and the jitter tolerance was successfully measured at 5 Gbps with a 2^7−1 PRBS pattern. The accuracy was within 10% error from the external BER equipment measurement result. The whole CDR circuit consumes 29.9 mW at a supply voltage of 1.2 V.

Keywords: on-chip jitter tolerance measurement, CDR (Clock/Data Recovery), VCO (Voltage Controlled Oscillator)

Classification: Integrated circuits

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1 Introduction

Modern high-speed interconnects often adopt clock and data recovery (CDR) techniques to increase the data rate per pin and to save on the costs of an extra clock pin. However, the test cost to measure the characteristics of CDR circuits on a per-chip basis is a significant portion of chip production cost. This is because high-accuracy test hardware is required and operated for a long time.

Jitter tolerance measurement in particular takes a substantial amount of time, since it relies on trial and error for bit error rate (BER) extraction. For this reason, on-chip jitter tolerance test circuits have been researched to mitigate this problem [1, 2]. Previous approaches utilize frequency divider circuits in the feedback path of CDR to generate jitter frequencies. Therefore, the modulated jitter frequency is closely correlated to oscillator frequency. This dependency prevents accurate prediction of jitter frequency. Furthermore, the realization of small frequency change and wide modulation range accompanies complexity of divider circuits. Another approach is a jitter tolerance measurement technique injecting jitter using a numerical control oscillator (NCO) and a sine DAC which are separated from the CDR [3]. In [3], jitter generation is done independently from the CDR, but this digital approach costs a large silicon area.

We propose a compact two-step jitter modulation technique for binary CDR circuits with a very small chip area. For the jitter generation, a separate jitter frequency generation block is adopted and the following charge pump converts it to a triangular pulse with predictable jitter amplitude. The resultant waveform is applied directly to the control voltage in the CDR loop to modulate the jitter amplitude and frequency of the VCO output. Thus, the modulation of jitter frequency can be independently achieved with a separate frequency source from VCO in CDR. Also, a continuous control on the independent frequency source enables wide range and linear changes of jitter modulation frequency. The resolution of jitter modulation can be achieved by simply increasing the ADC resolution of the control signals. In the proposed scheme, BER measurement circuit is also implemented for full on-chip characterization of jitter tolerance.

2 Architecture and operation

The block diagram of the proposed circuit is shown in Fig. 1. The scheme includes a CDR circuit using the bang-bang phase detector (BBPD), jitter modulation block, and bit error measurement block. The jitter modulation block consists of a jitter amplitude modulator and jitter frequency modulator. The bit error measurement block consists of a PRBS generator and bit error detector. When the amplitude and frequency of injection jitter are set by the jitter modulation block, the information is converted to a periodic triangular shape signal and applied to the control voltage of the CDR circuit. The control voltage is then converted to the amplitude and frequency of the jitter in the sampling clock. The binary phase detector samples input data with the modulated clock. Finally, an error bit is detected by comparing recovered data with the reference PRBS stream in the bit error measurement block. The BER is calculated with an external FPGA chip by collecting the error count.
The proposed jitter modulation scheme is shown in Fig. 2(a). For the frequency modulation, the operating current \( (I_{m,p}) \) of the ring oscillator is controlled to modulate the period of the output pulse. The inverter based charge-pump (CP) circuit modulates the amplitude of the triangular output pulse by controlling its pumping current \( (I_{f,p}) \). The output triangular pulse is applied to the control node of the CDR circuit. Therefore, the periodicity and the peak value of the triangular pulse determine the frequency and amplitude of jitter in the VCO output clock, respectively.

When the modulated signal is applied, the waveform of the control voltage is shown in Fig. 2(b). The modulated control voltage can be expressed as:

\[
V_{ctrl} = \begin{cases} 
\frac{2\Delta V}{T} t + V_C - \frac{\Delta V}{2}, & \left( 0 \leq t \leq \frac{T}{2} \right) \\
-\frac{2\Delta V}{T} t + V_C + \frac{3\Delta V}{2}, & \left( \frac{T}{2} \leq t \leq T \right).
\end{cases}
\]  

(1)

The period T of the triangular signal is equal to the square pulse period from the pulse generator. \( V_C \) and \( \Delta V \) represent the initial control voltage without modulation and the peak-to-peak amplitude of the triangular pulse, respectively. The peak-to-peak modulated voltage is given by:

\[
\Delta V = I_{m,p} Z_p.
\]  

(2)

where \( I_{m,p} \) is the bias current of the modulating charge pump, and \( Z_p \) is the impedance of the loop filter. The output frequency of the VCO is given by:

\[
\omega_{VCO} = \omega_o + K_{VCO} V_{ctrl}.
\]  

(3)

where \( \omega_o \) and \( K_{VCO} \) represent the initial angular frequency and VCO gain, respectively. The resulting phase amplitude can be obtained by integrating frequency variation (\( \omega_{vco} \)) over one period (T):
The modulated input jitter in the binary CDR is expressed as:

$$\Phi_{in} = \Phi_{in,p}\cos(\omega_{\Phi}t + \delta).$$

(5)

where $\Phi_{in,p}$ and $\omega_{\Phi}$ are the modulated jitter amplitude and frequency, respectively. Then, the maximum phase error $\Delta\Phi_{\text{max}}$ becomes:

$$\Delta\Phi_{\text{max}} = \sqrt{4\Phi_{in,p}^2 - \pi^2 K_{VCO}^2 I_p^2 R_p^2} / 2\omega_{\Phi}.$$  

(6)

where $I_p$ is the bias current of the charge pump in the CDR. Therefore, in the full-rate CDR, the maximum tolerable input jitter $\Phi_{in,p}$ or jitter tolerance ($G_{JT}$) can be obtained by letting $\Delta\Phi_{\text{max}} = \pi$:

$$|G_{JT}| = \Phi_{in,p} = \pi \sqrt{1 + \frac{K_{VCO}^2 I_p^2 R_p^2}{4\omega_{\Phi}^2}}.$$  

(7)

This jitter tolerance $|G_{JT}|$ falls at a rate of 20 dB/dec if the jitter frequency ($\omega_{\Phi}$) is less than the CDR bandwidth, and it becomes constant if the jitter frequency goes beyond the bandwidth.

Fig. 2. (a) Proposed jitter modulation and (b) modulated control voltage.
3 Experimental results

The proposed CDR with the on-chip jitter tolerance measurement module was fabricated with 65 nm CMOS. The whole chip area and jitter tolerance module occupy 0.047 mm² and 0.0036 mm², respectively. A photograph of the die is shown in Fig. 3. For initial calibration of the jitter tolerance measurement module, the peak-to-peak jitter profile is monitored from the data and clock outputs at each set of jitter amplitude and frequency control inputs.

Fig. 4 shows the modulated data eye-diagrams at 2.5 Gbps with different jitter amplitude with the jitter frequency fixed at 5 MHz. The peak-to-peak jitter amplitudes to the CDR were 0.21, 0.37, 0.51, and 0.75 UIpp, respectively. Fig. 5(a) shows the possible modulated jitter amplitude range for various jitter frequencies under a given BER criteria. For example, the ‘o’ symbol indicates the possible modulated jitter amplitude range that satisfies BER of less than $10^{-9}$. The theoretical upper bound (maximum phase jitter amplitude) was calculated from

![Die photograph of the proposed circuit](image)

Fig. 3. Die photograph of the proposed circuit

![Eye-diagrams](image)

(a) (b) (c) (d)

Fig. 4. Measured data eye diagram (@ 2.5 Gbps) with modulated jitter amplitude; (a) 0.21 UIpp, (b) 0.27 UIpp, (c) 0.32 UIpp, and (d) 0.40 UIpp at 5 MHz jitter frequency.
Eq. (4) at given circuit parameters \(K_{vco} = 2\pi \cdot (1.35 \times 10^5)\) rad/V, \(I_p = 50\) uA, and \(R_p = 300\) \(\Omega\). A 3-bit ADC is used for 8-step amplitude and frequency control. The amplitude range was 0.05 to 2 UIpp at 10 MHz, and the controllable frequency range was 100 KHz to 20 MHz.

To compare the accuracy of BER testing, the jitter tolerance is measured in two ways. First, a real BER test equipment is connected directly to the recovered data and clock outputs and measure the BER under various jitter frequencies generated from the equipment. Secondly, BER of the CDR using the proposed on-chip jitter tolerance circuit was measured with the on-chip BER checker. The measured jitter tolerance was compared to the testing result using the actual BERT equipment and plotted in Fig. 5(b). A dash line is the theoretical limit calculated from Eq. (7). At low jitter frequencies, the difference was relatively large due to the amplitude modulation resolution limitation. At the jitter frequency range of 1 to 20 MHz, the
measured jitter amplitude was less than 10% off from using an external equipment testing for $10^{-9}$ BER when the data rate at 5 Gbps with a $2^7$-1 PRBS pattern.

The whole chip consumes 29.9 mW at a data rate of 5 Gbps with a supply voltage of 1.2 V. The performance of the on-chip jitter tolerance module was compared to prior approaches, as shown in Table I. The proposed on-chip jitter tolerance modulation scheme generates a VCO-independent jitter frequency. The scheme is simpler than other works [1, 2, 3], so it consumes less chip area and power.

| Table I. Performance comparison with prior works |
|-------------------------------------------------|
| Technology | This work | [1] | [2] | [3] |
| Supply Voltage | 65 nm CMOS | 90 nm CMOS | 65 nm CMOS | N/A |
| Data Rate | 1.2 V | 1.2 V | 1.35 V | N/A |
| Data Pattern | 5 Gb/s | 6 Gb/s | 10.2 Gb/s −12.5 Gb/s | 12 Gb/s |
| CDR type | $2^7$-1 PRBS | $2^7$-1 PRBS | $2^{15}$-1 PRBS | N/A |
| Jitter tolerance measurement circuit type | Analog: VCO-independent jitter freq. generation | All digital: VCO-dependent jitter freq. generation | Analog: VCO-dependent jitter freq. generation | NCO and sine-DAC VCO-independent jitter freq. generation |
| Modulating frequency range | 100 KHz −20 MHz | 178 KHz −11.3 MHz | 340 KHz −104 MHz | 3 MHz −150 MHz |
| Error compared to Equipment | <10% | <13% | <10% | N/A |
| Total Circuit Area | 0.047 mm² | 0.054 mm² | 0.58 mm² | N/A |
| Power consumption | 29.9 mW | 44.4 mW | N/A | N/A |

4 Conclusions

We have proposed an efficient on-chip jitter modulation scheme that independently modulates jitter frequency, which is uncorrelated to VCO in the CDR and applies a modulated waveform directly to the CDR loop. An error detection module was also implemented to evaluate the on-chip BER. The proposed on-chip jitter tolerance scheme achieves independent jitter modulation frequency with a wide and linear frequency range. The designed CDR was measured for jitter tolerance with a jitter amplitude range of 0.05−2 Ulpp at 10 MHz and with a jitter frequency range of 100 KHz−20 MHz. Compared to the external equipment measurement, the proposed on-chip scheme shows less than 10% difference in the range of 1 to 20 MHz jitter frequency at BER = $10^{-9}$. The simplicity of proposed scheme also helps to reduce silicon area and power consumption comparing to previous works.
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