High-Linearity Direct Conversion Receiver with the Transconductance Equalization Technique and DCOC Method

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Abstract: To improve the linearity of direct conversion receivers (DCRs), two high-linearity methods for high second-order intercept points (IP2s) and high third-order intercept points (IP3s) are proposed. To improve IP3s, a transconductance equalization technique for a complementary input operational amplifier (OPAMP) is proposed in an active-RC low-pass filter (LPF), while a digital-analog hybrid DC offset calibration (DCOC) method is proposed to improve IP2s. For one thing, the proposed transconductance equalization technique employs a pair of resistors to guarantee high voltage gain for an OPAMP with two-stage Miller topology under a high-input voltage swing to improve linearity with little deterioration of the noise performance. For another, during the DCOC method, the low-noise amplifier is turned off and replaced by an equivalent resistance of the output impedance of the low-noise amplifier to ensure the accuracy and effectiveness of the DCOC method. Fabricated in 40-nm CMOS technology, the receiver with proposed methods can realize a noise figure of 2.6–3.5 dB in the full frequency band, with an OIP3 of 28 dBm, an IM2 more than 70 dBc, and a remaining DC of −53.2 dBm under the total voltage gain of 60 dB.

Keywords: direct conversion receiver; operational amplifier; DC calibration; active RC filter

1. Introduction

The direct conversion receiver (DCR) has the advantages of high integration, strong reconfigurability, and low cost, making it a preferred architecture for most radio frequency receivers [1]. In a high linearity design, improving the second-order intercept point (IP2) and the third-order intercept point (IP3) is a critical requirement of the DCR and the overall system.

First of all, for a high IP3, an RC-active filter is the preferred topology when achieving high linearity is the most critical design metric, because RC-active filters can realize high linearity and be capable of supporting a large voltage swing based on an operational amplifier (OPAMP) with finite high gain and bandwidth [2]. However, under a high input swing, it is difficult to realize an OPAMP with a voltage gain high enough and with low output impedance [3]. To achieve high loop gain, the OPAMP always needs a complicated multi-stage topology, such as the Miller compensation two-stage architecture, nested compensation three-stage architecture, and so on [4]. Recently, several works have been reported to improve the linearity of the RC-active filters by employing OPAMPs or OTAs with multi-stage topologies and compensated structures to realize high loop gain [3,5–9], while some solutions considered low-voltage and low-power applications [10,11]. Among this research, the multi-stage Miller architecture with the gain boost technique has been widely employed to implement high-gain OPAMPs of over a 50-dB gain. However, the loop gain of a multi-stage topology can be limited by a large voltage swing. The total transconductance of the second and third stage can be seriously limited under a high output swing, especially when the gain of the LPF is large enough, resulting in the output swing of the first stage exceeding the maximum input swing of the second stage.
Secondly, the DCR has a very serious DC offset problem which will not only reduce the IP2 of the receiver but can even saturate the subsequent circuit [1,12]. AC coupling [13] and a DC negative feedback loop [14–16] are popular methods to eliminate DC offset, but these methods often occupy a large amount of chip area and require a long DC stabilization time [17–19]. More and more receivers have eliminated DC offsets by digital methods, employing digital algorithms to control digital-to-analog converters (DACs) to compensate for DC offsets. These digital methods often need to cut off the low-noise amplifier from the antenna during the calibration process through an off-chip RF switch. However, due to the limited isolation of the radio frequency switch, the receiver suffers from the interference from the signal received by the antenna during the calibration process [1,20]. In addition, some DC offset cancellation methods in the digital domain employ digital filters to filter out the DC component of the signal [21], which not only requires complex digital algorithms but also filters out useful signals in low-frequency components [22].

In this paper, two high linearity methods are proposed to solve the previous problems. To realize high linearity, a transconductance equalization technique is employed in a complementary OPAMP-based LPF, and an effective DC offset calibration (DCOC) method combined with analog and digital circuits is employed to achieve a high IP3 and IP2, respectively. In the transconductance equalization technique, the gate terminals of the NMOS transistors and PMOS transistors in the second stage are biased at different DC voltages by employing a pair of resistors in the first stage to avoid the transconductance limitation caused by a large voltage swing. On the other hand, during the DCOC process, an equivalent resistance is used to replace the output impedance of the low-noise amplifier so that the transfer function of the DC offset is kept consistent during calibration and operation. This calibration method with a digital-analog hybrid function greatly reduces the design requirements for analog circuits such as DACs. In addition, this DCOC method will not distort the low-frequency signal, since it is only activated before the receiver is powered on.

The transconductance equalization technique and DCOC method are discussed in Section 2 of this paper, while Section 3 presents the circuit designs of the proposed methods. The measurement results are reported in Section 4. The conclusion is drawn in Section 5.

2. High-Linearity Methods

2.1. Transconductance Equalization Technique

Figure 1a shows a conventional two-stage Miller OPAMP with a complementary input structure, where the Common Mode Feedback (CMFB) circuits are omitted for a succinct purpose.

![Figure 1a](image)

Stage 1 Stage 2

(a) (b)

Figure 1. (a) Diagram of conventional two-stage complementary input OPAMP. (b) Diagram of two-stage complementary input OPAMP with proposed transconductance equalization technique.

The complementary input topology can realize a higher voltage gain than the OPAMP with a single transistor at the cost of the same current due to the current reuse in the
push-pull principle [4]. However, the output swing of the first stage can be very large, owing to the high voltage gain of the LPF. Although the output terminal of the first stage can be biased at an adequate DC voltage to guarantee all the transistors in the second stage not entering the cutoff region, the large output swing can make half of the transistors in the second stage enter the linear region, which still seriously limits the voltage gain of the OPAMP. As is shown in Figure 2a, NMOS transistors M1 and M2 enter the linear region when the output voltage swings to the maximum point, while PMOS transistors M3 and M4 enter the linear region when the output voltage swings to the minimum point. Therefore, the voltage gain is limited when the input terminals of M1–M4 are biased at the same DC voltage.

**Figure 2.** (a) Transconductance of the input transistors in the second stage without $R_{dc}$. (b) Transconductance of the input transistors in the second stage with $R_{dc}$.

Figure 1b shows the OPAMP topology with the transconductance equalization technique proposed in this paper. With a pair of resistors $R_{dc}$, NMOS and PMOS transistors are biased at different DC voltages to avoid M1–M4 entering the linear region. As shown in Figure 2b, with the $V_{dc}$ generated by the $R_{dc}$, NMOS transistors M1 and M2 are biased at a lower DC voltage to be prevented from entering the linear region when the output signal swings to the maximum point, while PMOS transistors M3 and M4 are biased at a higher DC voltage to be prevented from entering the linear region when the output signal swings to the minimum point. Although the voltage gain can still be limited by the channel length modulation under a large input swing, all transistors of the second stage operating in the saturation region can alleviate transconductance limitation effectively.

2.2. DCOC Method

The IM2 of the DCR is mainly introduced by mismatches between the N path and P path of the mixer, TIA, and LPF, which are mainly introduced by DC offsets from the input terminals of the mixer, TIA, and LPF. Consequently, the IM2 can be depressed by reducing the DC offset [23,24]. More precisely, the output signal of the N and P terminals $y_p(t)$ and $y_n(t)$ responds to an input signal $x(t)$ as shown by Equation (1). Note that we only consider the second-order distortion:

$$y_p(t) = a_{1p}x(t) + a_{2p}x^2(t)$$
$$y_n(t) = a_{1n}x(t) + a_{2n}x^2(t)$$

$$y_p(t) - y_n(t) = (a_{1p} - a_{1n})x(t) + (a_{2p} - a_{2n})x^2(t)$$

(1)
where $a_{1p}$ and $a_{1n}$ are the responses of the first order and the second order, respectively. From the third equation in Equation (1), we can see that $(a_{2p} - a_{2n})x(t)^2$ is introduced as the second-order distortion by mismatches between the N and P paths due to the DC offsets. Therefore, a hybrid DCOC method is proposed to depress mismatches of the TIA and the LPF in Figure 3 to depress the IM2.

The proposed DC offset calibration method is shown in Figure 4. The initial value of the DAC is set to 10,000,000 at the beginning so that the DAC offers almost the same current (only 1 LSB of difference) to the differential ends of the mixer and the LPF circuits. To ensure that the signal received by the antenna has not interfered during the DC calibration process, the LNA should be powered down by connecting to $R_{replace}$ the equivalent resistance of the LNA. With the mixer path connected to $R_{replace}$, the transfer function of the DC offset is stabilized during calibration to validate the calibration results. During the process of calibration, the DAC is controlled by a successive approximation algorithm (SAR) to compensate for the DC offset. Finally, the DAC output is averaged by a digital averaging circuit to obtain the remaining DC offset, which is restored in registers together with the previous calibration results of the DAC.

![Figure 3. The block diagram of the direct conversion receiver.](image)

The proposed DC offset calibration method is shown in Figure 4. The initial value of the DAC is set to 10,000,000 at the beginning so that the DAC offers almost the same current (only 1 LSB of difference) to the differential ends of the mixer and the LPF circuits. To ensure that the signal received by the antenna has not interfered during the DC calibration process, the LNA should be powered down by connecting to $R_{replace}$ the equivalent resistance of the LNA. With the mixer path connected to $R_{replace}$, the transfer function of the DC offset is stabilized during calibration to validate the calibration results. During the process of calibration, the DAC is controlled by a successive approximation algorithm (SAR) to compensate for the DC offset. Finally, the DAC output is averaged by a digital averaging circuit to obtain the remaining DC offset, which is restored in registers together with the previous calibration results of the DAC.

![Figure 4. The flow diagram of the DCOC method.](image)
3. Circuit Designs

The architecture of the DCR with proposed high-linearity methods in this paper is shown in Figure 3, including the broadband low-noise amplifiers, mixers, low-pass filters, analog-to-digital converters (ADC), and DC offset calibration circuits.

Among them, the DC offset calibration circuit includes two programmable resistors used to replace the output impedance of the low-noise amplifier during the calibration process, four DACs, and four comparators for the compensation and detection of the DC offset, respectively, in the analog domain. Two digital averaging circuits are employed for detecting the residual DC offset and DC offset calibration control algorithm.

3.1. RC-Active LPF Based on a Complementary OP AMP with the Proposed Transconductance Equalization Technique

The proposed DCR adopted a two-stage Tow-Thomas biquad structure to implement a four-stage Chebyshev low-pass filter. The circuit block diagram is shown in Figure 5. By configuring the resistance and capacitance value, a gain range of 0–23 dB and a bandwidth range of 1–32 MHz could be achieved, and together with the previous transconductance amplifier in the mixer, a gain range of 5–65 dB could be achieved. The parameters of the transconductance amplifier of the mixer and the LPF are shown in Table 1.

![Figure 5. The block diagram of the LPF.](image)

Table 1. Parameters of the mixer and LPF.

| Transconductance Amplifier of the Mixer | First-Stage OPAMP of the LPF | Second-Stage OPAMP of the LPF |
|----------------------------------------|-------------------------------|-----------------------------|
| Gain                                   | $R_f$ (Ω)                     | Gain                        | Gain                        | $R_6$ (Ω)                       |
| 15–27 dB                               | 500–2700 Max BW               | 0–18 dB                     | 100–800 Max BW              | 340–600 Max BW                 |
|                                        |                               |                             | 400–3200 Min BW             | 1360–2400 Min BW               |
|                                        |                               |                             | 0–5 dB                      |                               |

The linearity of the LPF was determined by the overdrive voltage of the input transistors of the OPAMP and the loop gain of each stage of the LPF, so the OPAMP must have had a sufficiently high DC gain and gain bandwidth (GBW) [25,26]. The OPAMP adopted a two-stage Miller topology, and the circuit diagram is shown in Figure 6.
The amplifier employed cascade and gain boost technology to achieve an extremely high DC gain. The OPAMP with the largest input and output voltage swing was adopted in the simulation. The linearity of the LPF was determined by the overdrive voltage of the input transistors of the last-stage OPAMP of the LPF, operated in the linear region. In addition, the operational amplifier employed cascade and gain boost technology to achieve an extremely high DC gain. The $R_{dc}$ was 638 ohms, while the Miller capacitor $C_c$ was configurable to adjust the gain bandwidth of the OPAMP to meet the requirements of different IF bandwidths.

To confirm this, the total transconductance $g_{m,\text{total}}$ of the input transistors of the second stage of the OPAMPs with and without $R_{dc}$ as the differential output voltage of the LPF was swept from 0 to 625 mV (1.3 $V_{pp}$, maximum output power 6 dBm) is plotted in Figure 7. To confirm that the simulation results were valid for all IF frequencies, voltage gains, and all OPAMPs in the LPF, the voltage gain and bandwidth of the LPF were set to 23 dB and 32 MHz, respectively, while the $g_{m,\text{total}}$ of the last-stage OPAMP of the LPF, operated in the largest input and output voltage swing, was adopted in the simulation.

From Figure 7, we can see that the transconductance of the second stage of the OPAMP with $R_{dc}$ was less suppressed than that of the OPAMP without $R_{dc}$ under an increasing voltage swing than that without $R_{dc}$. Furthermore, the DC simulation results show that all the input transistors of the second stage of the OPAMPs with $R_{dc}$ when the differential output swing was less than 313.3 mV ($627 V_{pp}$, output power 0 dBm), while those operating in the saturation region in the OPAMP without $R_{dc}$ when the differential output swing was less than 125.1 mV. Although the maximum $g_{m,\text{total}}$ of the OPAMP without $R_{dc}$ was a little bit larger than that with $R_{dc}$,attributed to the channel length modulation effect, the linearity of the LPF could be improved by $R_{dc}$ for a more stable voltage gain of the OPAMP, especially under a large output swing. To validate this, the simulation of OIP3 for two closely spaced tones (1 MHz) with a total output amplitude of $632 V_{pp}$ (total output power 0 dBm) as their frequency was swept from 0.25 $f_0$ to 1.75 $f_0$ ($f_0 = 16$ MHz) is plotted in Figure 8. To confirm that the results could be adopted in all IF frequencies and voltage gains, the bandwidth and voltage gain of the LPF were set to 32 MHz and 23 dB, respectively.
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All saturation

Figure 7. Simulation results of $g_{m,\text{total}}$ of the second stage of the OPAMPs with and without $R_{dc}$ versus the differential output voltage.

Figure 8. Simulation results of OIP3 of the LPF with and without $R_{dc}$ versus the IF frequency from 4 to 28 MHz under a total output swing of 632 mV (each tone being 316 mV).

From Figure 8, we can see that the OIP3 of the LPF was improved by approximately 7 dB under an output swing of 632 mV in all IF frequencies, while the LPF could realize a maximum OIP3 of 40.7 dBm with a voltage gain of 23 dB. The simulation results of the frequency response of the gain with and without $R_{dc}$ of the proposed Opamp and the 1-dB compression point of the LPF with the proposed OPAMP are shown in Figure 9a,b, respectively. Note that the 1-dB compression point was simulated with a gain of 0 dB.
From Figure 8, we can see that the OIP3 of the LPF was improved by approximately 115 dB, and the $R_{dc}$ had little influence on the frequency response of the OPAMP. Furthermore, the output 1-dB compression point of the LPF with the proposed OPAMP are shown in Figure 9a, b. We can see from Figure 9a that the DC gain of the proposed OPAMP could achieve 115 dB, and the $R_{dc}$ had little influence on the frequency response of the OPAMP. Furthermore, the output 1-dB compression point was about 12.6 dBm, which would not influence the linearity of the whole system because the maximum output power of the LPF was less than 6 dBm.

3.2. DCOC Circuits

To calibrate the DC offset effectively and prevent the DC offset from the RF front end being amplified by the LPF, the calibration was operated at the output terminal of the RF front end and the LPF. The DC offset of the RF front end was mainly introduced by the circuit mismatches and that of the RF front end. It was assumed that the equivalent DC offset of the mixer at the input terminal of the OPAMP of the TIA was $V_{osin}$, as shown in Figure 10.

Figure 9. (a) Simulated frequency response of the gain with and without $R_{dc}$ of the proposed OPAMP. (b) Simulated 1-dB compression point of the LPF with the proposed OPAMP. We can see from Figure 9a that the DC gain of the proposed OPAMP could achieve 115 dB, and the $R_{dc}$ had little influence on the frequency response of the OPAMP. Furthermore, the output 1-dB compression point was about 12.6 dBm, which would not influence the linearity of the whole system because the maximum output power of the LPF was less than 6 dBm.

Figure 10. The block diagram of the RF front end.
Consequently, the DC offset of the mixer could be given by

$$V_{out_{mix}} = \left(1 + \frac{R_f}{R_{outIF}}\right)V_{osin} + (I_n - I_p)R_f$$  \hspace{1cm} (2)$$

where $R_{outIF}$ is the equivalent output resistance of the mixer and $R_f$ is the feedback resistor of the TIA. Since the passive mixer could transform the impedance at both ends of itself at the frequencies, the equivalent output resistance $R_{outIF}$ of the passive mixer was proportional to the output impedance of the transconductance stage \cite{27–29}. Therefore, $Z_{outRF}$ could be expressed as follows:

$$Z_{outRF} = \left(\frac{1}{2\pi f_{LO}C_{1_{para}}} + R_{out}\right)\left(\frac{1}{2\pi f_{LO}C_{1_{para}}R_{out}}\right)\left(\frac{1}{G_m}\right)\left(\frac{1}{2\pi f_{LO}C_{2_{para}}}\right)$$  \hspace{1cm} (3)$$

where $R_{out}$ is the output impedance of the LNA, $C_{1_{para}}$ and $C_{2_{para}}$ are the parasitic capacitances that are less than 80 fF according to the simulation, and $G_m$ is the transconductance of the mixer. With $R_{out}$ being different under different gains of the LNA and the increasing $f_{LO}$, the equivalent output resistance of the mixer would drop dramatically \cite{30}. Therefore, to confirm the accuracy of the DC offset calibration, $R_{out}$ should be replaced by $R_{replace}$ with a constant resistance, as shown in Figure 10. Moreover, the DC offset needed to be recalibrated for different local oscillator frequencies and gains \cite{31}.

On the other hand, the DC offset of the LPF mainly came from that of the mixer and the circuit mismatches. It was assumed that $V_{osin1}$ and $V_{osin2}$ were the equivalent input DC offset voltages of the first and second stage of the low-pass filter, respectively. The output DC offset could be expressed as

$$V_{out_{LPF}} = \frac{R_2}{R_1} \frac{R_7}{R_6} V_{out_{mix}} - \left(1 + \frac{R_2}{R_1}\right) \frac{R_7}{R_6} V_{osin1} + \left(1 + \frac{R_7}{R_6}\right) V_{osin2} - (I_n - I_p) \frac{R_2}{R_6}$$  \hspace{1cm} (4)$$

where $R_2 / R_1$ and $R_7 / R_6$ are the voltage gain of the first stage and second stage of the LPF, respectively. It can be seen from Equation (4) that for different gains and IF bandwidths, the DC offset should be recalibrated.

According to the previous calculation, the parameters of the DAC could be confirmed. The calibration accuracy and range of the DC offset depended on the circuit parameters of the DAC \cite{32}. Therefore, the least significant bit (LSB) of the DAC should be less than the minimum DC offset of the mixers and LPF, while the total current of the DAC should be larger than the maximum DC offset of the mixers and the LPF \cite{30}. According to the equivalent input DC offset voltage of the OPAMP through Monte Carlo simulation \cite{33} and the gain of the mixers and LPF shown in Table 1, the DAC employed in the DCOC circuits is shown in Figure 11. This was an 8-bit, full-thermometer, current-steering DAC with an LSB current of 120 nA, which could ensure that the output DC offset of the mixer and low-pass filter could be limited to less than −50 dBFS (differential of 1.4 mV, ADC full swing of 6.5 dBm) after calibration in the analog domain.

![Figure 11. The block diagram of the DAC.](image-url)
4. Measurement Results

Based on the RF transceiver system with two receivers and two transmitters, the DCR was fabricated in 40-nm CMOS technology. The chip photo of the receiver is shown in Figure 12. The chip area of the whole receiver (excluding ADC) was 1.15 mm$^2$, and it consumed 126 mA of current under a voltage supply of 1.3 V.

![Figure 12. Chip microphotograph of the receiver.](image)

Figure 13a shows the S11 result of the receiver. It can be seen that this DCR could achieve $-10$ dB input matching in the full frequency band. Through the frequency spectrum analysis of the ADC output signal, it can be seen in Figure 13b that the receiver could achieve a noise figure of 3.5 dB at a frequency offset of 3 MHz in the full frequency band.

![Figure 13. (a) Measured S11 results. (b) Measured noise figure results.](image)

In order to measure the linearity of the receiver under the maximum IF bandwidth, the receiver gain was configured to 60 dB (low noise amplifier: 15 dB; mixer: 27 dB; and filter: 18 + 0 dB), while the full swing of the ADC was 6.5 dBm. Figure 14a,b shows the linearity test results of the receiver at an RF frequency of 2.5 GHz before and after DC offset calibration. It can be seen that the receiver could achieve an OIP3 of 28 dBm. After DC offset calibration, the IM2 was improved by more than 10 dBc to more than 70 dBc, and the remaining DC was reduced by 21 dBm to $-53.2$ dBm.
Figure 13. (a) Measured S11 results. (b) Measured noise figure results.

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Figure 14. (a) Measured linearity without the DCOC at 2.5 GHz. (b) Measured linearity with the DCOC at 2.5 GHz.

Table 2 is the performance comparison between the proposed DCR and other references in recent years. It can be seen that this DCR could achieve a better noise figure and higher linearity of better suppression for both IM2 and IM3 in a wideband range.

|               | [34]  | [35]  | [36]  | This Work |
|---------------|-------|-------|-------|-----------|
| Technology    | 65 nm CMOS | 65 nm CMOS | 22 nm FD-SOI | 40 nm CMOS |
| Supply (V)    | 1.0   | 1.2   | 0.8   | 1.3       |
| RF (MHz)      | 2400  | N/A   | 700–5700 | 200–2500  |
| IF (MHz)      | N/A   | 0.07–10 | N/A   | 1–32      |
| Gain Range (dB) | 2–62 | 18.2–70.6 | 41    | 0–60      |
| IM2 (dBc)     | 31.1  | N/A   | N/A   | >70       |
| OIP3 (dBm)    | N/A   | 7.8   | 22    | 28        |
| DC Remaining (dBm) | N/A   | N/A   | N/A   | −53.2    |
| Noise Figure (dB) | 3.0   | N/A   | 6.8–9.2 | 2.6–3.5  |
| Total Area (mm²) | 0.75  | N/A   | 0.52  | 1.15      |
| Total Power (mW) | 3.55  | N/A   | 19.25–34.75 | 160      |

5. Conclusions

This paper presents two high-linearity methods for a DCR to realize better IP2 and IP3 values. In order to improve IP3, a complementary input operational amplifier in the LPF was adopted in the DCR. To improve IP2, a digital-analog hybrid DC offset calibration method was proposed based on the structure of the mixer and LPF. After being fabricated in 40-nm CMOS technology, the measurement results show that the DCR could achieve a noise figure of 2.6–3.5 dB in the full frequency band, an IIP3 of 10 dB, an OIP3 of 28 dBm, an IM2 of more than 70 dBc, and a remaining DC offset of $-53.2$ dBm under a total voltage gain of 60 dB.

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