Thermal and electromechanical characterization of top-down fabricated p-type silicon nanowires

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Abstract
In this paper we report thermal conductivity and piezoresistivity measurements of top-down fabricated highly boron doped \((N_A = 1.5 \times 10^{19} \text{ cm}^{-3})\) suspended Si nanowires. These measurements were performed in a cryogenic probe station respectively by using the 3 omega method and by in situ application of a longitudinal tensile stress to the nanowire under test with a direct four point bending of the Si nanowire die. Nanowires investigated have a thickness of 160 nm, a width in the 80–260 nm range and a length in the 2.5–5.2 μm range. We found that for these geometries, thermal conduction still obeys Fourier’s law and that, as expected, the thermal conductivity is largely reduced when the nanowires width is shrunk, but, to a lower extent than published values for nanowires grown by vapor–liquid–solid (VLS) processes. While a large giant piezoresistance effect was evidenced by various authors when a static stress is applied, we only observed a limited nanowire size dependence of the piezoresistivity in our experiments where a dynamical mechanical loading is applied. This confirms that the giant piezoresistance effect in unbiased Si nanowires is not an intrinsic bulk effect but is dominated by surface related effects in agreement with the piezopinch effect model.

Keywords: silicon nanowires, piezoresistivity, thermal conductivity, four point bending, three omega method
Classification numbers: 2.08, 4.08, 5.01

1. Introduction
Owing to their small cross section area, their large surface-to-volume ratio and their specific mechanical and transport properties when compared to bulk silicon, silicon nanowires are attractive nanomaterials for strain gauges [1–7], for chemical [8–10] and biological [11, 12] sensors, for photovoltaic conversion [13, 14] and for many other applications. Silicon nanowires can be fabricated by a bottom-up approach, typically by vapor–liquid–solid (VLS) growth processes, or by a top-down approach, generally by surface nanomachining of a thin silicon-on-insulator (SOI) wafer. VLS growth allows collective fabrication of nanowires with a very low cross section but with faceted surfaces in a non-homogeneous way along their length and with possible surface contamination by clusters of catalyst dots (generally gold) used in the process. Despite eventual residual stress issues [15], the top-down approach has significant advantages for the integration of nanowires in test or sensing devices: it allows an accurate alignment with electrodes and other devices such as micro-electromechanical systems (MEMS) [5, 7, 16], it makes easier their electrical contacts and doping, it is CMOS compatible, and it provides a flexible choice and a good control of nanowire geometry. Top-down fabricated nanowires with a
width down to less than 30 nm can be achieved when e-beam lithography is used for patterning. In this paper all measurements were performed on Si nanowires fabricated by a top-down approach.

Various theoretical and experimental works demonstrated that the thermal conductivity of semiconducting thin films and nanowires can be much lower than the corresponding bulk values and that it is largely affected by size reduction, doping and surface roughness because of increased phonon–phonon scattering, phonon boundary scattering and other mechanisms limiting phonon transport [17–21]. A low thermal conductivity associated with a high electrical conductivity is an interesting feature both from a fundamental point of view, for thermal insulation and for thermoelectrical applications [17]. For example, the figure of merit ZT of thermoelectrical generators can be increased by a factor up to 60 by using Si nanowires instead of bulk silicon [22]. More generally, knowing the thermal conductivity of nanowires is useful for sensors based on them such as Pirani pressure gauges, strain nanogauges etc. Thermal conductivity measurements of Si nanowires are not numerous and were mainly performed on nanowires grown by the VLS technique. In this work, instead of using a complex-to-fabricate microdevice with integrated heating source and thermometer [17–19], thermal conductivity measurements were performed directly on the Si nanowires by the 3 omega method [21, 22] which is increasingly used for thermal measurements of nanomaterials.

Concerning the piezoresistivity of Si nanowires, there is a controversy about the existence or not of a bulk giant piezoresistance effect. A comprehensive and critical review of this topic was reported recently [23]. While a large giant piezoresistance effect was observed by various authors when a static stress is applied (see references [2, 3]), bulk silicon piezoresistivity values were measured for micro and nano-wires submitted to a dynamic mechanical loading [4]. To check this point, our piezoresistivity measurements were performed by applying a sinusoidal longitudinal stress to the nanowires.

2. Experimental details

2.1. Sample fabrication

All samples investigated in this work were realized by CEA-LETI by the CAL2 process depicted in figure 1. This process was implemented for (100) SOI wafers having a 400 nm thick buried oxide layer and a thin (160 nm) top Si layer. This structural top Si layer defines the thickness of the Si nanowires.

It is first uniformly doped by Boron implantation ($N_A = 1.5 \times 10^{19} \text{cm}^{-3}$) and annealed at high temperature (figure 1(a)). Then it is patterned by a hybrid lithography followed by reactive ion etching (RIE): the anchor pads are patterned by deep ultraviolet (DUV) lithography while the nanowires are patterned by electron beam lithography (figure 1(b)). A SiO$_2$ protective and insulating layer is subsequently deposited and patterned by UV lithography and RIE etching to open contact holes (figure 1(c)). A thick AlSi film is then deposited and patterned to form metallic electrodes on the anchor pads (figure 1(d)). Finally, the nanowires are released by vapor HF etching of the protective and buried SiO$_2$ layers (figure 1(e)). This process was applied to the fabrication of devices with 160 nm thick nanowires having a length $L$ in the 2.5–5.2 μm range, a width $w$ in the 80–260 nm range, a $L/w$ ratio in the 10–30 range and an orientation along the ⟨110⟩ crystallographic direction. An example of scanning electron microscopy (SEM) picture of a fabricated device is shown in figure 2 with a zoom in the nanowire area. Contrary to nanowires fabricated by the VLS method, these nanowires have a rectangular cross section. They likely exhibit greater sidewalls roughness resulting from the patterning techniques but their geometry is well mastered as well as their alignment and anchoring to contact pads. The experimental techniques that were developed for thermal and electromechanical characterizations of these nanowires are described in the next sections.

**Figure 1.** Flow chart of the nanowire devices fabrication process.

**Figure 2.** SEM picture of a $4 \mu m \times 200 \text{nm} \times 160 \text{nm}$ Si nanowire device.
2.2. Thermal conductivity measurements

The nanowires’ thermal conductivity was measured by the $3\omega$ method [22]. In this method a sinusoidal current $I(\omega)$ with a radial frequency $\omega$ is injected in the nanowire under test. This induces a heating by joule effect at a radial frequency $2\omega$ and a partial modulation of the nanowire temperature at the same frequency. For small temperature changes $\Delta T = T - T_0$ where $T_0$ is the ambient temperature, the nanowire resistance is a linear function of temperature at any position $x$ along the nanowire so the resistance variation profile is also varying at twice the radial frequency $\omega$. The resulting voltage drop $V = RI$ has then 2 components: one large component $V_{1\omega}$ related to ohm law with mean resistance variation, and a much smaller component at radial frequency $3\omega$. At low modulation frequency, the thermal response is not limited by the thermal constant of the nanowire. It can be shown that for our nanowires, this condition is fulfilled if the current modulation frequency is much lower than a few MHz. Then the RMS value of the third harmonic of the voltage drop is given by [24]:

$$V_{3\omega} = \frac{4I_{RMS}^3R_0^2}{\pi^4\kappa S},$$

where $I_{RMS}$ is the RMS value of injected current, $R_0$ the nanowire resistance at $T_0$, $\alpha$ the linear temperature coefficient of resistance (TCR), $\kappa$ the thermal conductivity at nanowire mean temperature, and $S$ is the area of the nanowire cross section.

Equation (1) was established by assuming heat transport by Fourier’s law. It shows that if thermal transport is diffusive, the thermal conductivity can be computed from measured values of $V_{3\omega}$, $R_0$ and $\alpha$. All our measurements were performed in the vacuum chamber (background pressure $<10^{-5}$ mbar) of a cryogenic probe station Janis ST-500. A dc or ac current was injected in the nanowire device under test with a Keithley 2182 nanovoltmeter while $V_{3\omega}$ measurements were performed with a Signal Recovery 7280 lock-in amplifier. For the nanowires investigated here, the $V_{3\omega}/V_{1\omega}$ ratio is in the $10^{-2}$–$10^{-5}$ range and if a standard lock-in detection scheme is used, the input of the lock-in amplifier can be easily saturated by the 1 $\omega$ component of the signal. This can be avoided by using a very low injected current but a long integration time is then required to get measurable values of $V_{3\omega}$ [21].

In order to use larger injected currents and thus get faster and lower noise measurements, the $V_{1\omega}$ component of the signal must be reduced or removed before detection. This is often realized by a Wheatstone bridge configuration but this solution generates an unwanted parasitic third $3\omega$ component in the injected current [25]. Instead we used a better performing cancellation circuit based on instrumentation amplifiers (figure 3). This circuit generates, from a shunt resistance in series with the nanowire, a voltage at radial frequency $\omega$ which is tuned and subtracted to the input signal of the lock-in amplifier. In addition the circuit was designed to allow a compensation of parasitic capacitances of the nanowire device which induces a phase lag in the 1 $\omega$ signal.

The ac current injection also induces an increase of the mean temperature of the nanowire. This increase was estimated from an electrothermal modelling of the nanowire. If we assume that thermal transport is diffusive, the temperature profile can be calculated by solving the 1D heat diffusion equation with a Joule heating source and by considering nanowire ends at room temperature $T_0$ as the boundary conditions. Because measurements are performed in vacuum, convection losses can be safely neglected. Radiative losses were also considered negligible because of the small nanowire area and the low temperature rises. The very good accuracy of this assumption and of a 1D model was checked by numerical solving the 1D heat equation including conduction and radiation losses and by comparison with 3D finite element simulations. We also checked that temperature variation of the resistance can be neglected for temperature profile calculations. With all these validated simplifying assumptions, it can be shown that the longitudinal temperature profile (along direction $x$) is simply given by the following simple expression [25]

$$T = T_0 + \frac{I_{RMS}^2R_0}{2\kappa}x(L-x),$$

where $V = L \times w \times t$ is the volume of the nanowire. The maximum temperature at the midle of the nanowire ($x = L/2$) is then given by:

$$T_{Max} = T_0 + \frac{I_{RMS}^2R_0L}{8\pi^4\kappa}.$$ (3)

The temperature rise computed from equation (3) is plotted in figure 4 as a function of injected current for the highest and lowest resistivity nanowires investigated. To get low noise measurements while minimizing the temperature rise, all measurements were performed with an injection in the 10–60 $\mu$A range.

The validity of the 3 $\omega$ method and the performances of our measurement set-up were checked from a measurement at room temperature on a 2.5 $\mu$m long, 260 nm wide and 160 nm thick boron doped Si nanowire ($N_A = 1.5 \times 10^{19}$ cm$^{-3}$). Measured values of the nanowire resistance $R_0$ and $\alpha$ for this nanowire are 1.5 k$\Omega$ and $7 \times 10^{-4}$ K$^{-1}$, respectively. The variation of $V_{3\omega}$ with the injected current for a modulation frequency equal to 1.007 kHz is displayed in figure 5. This
frequency was chosen to be much lower than the cut-off frequency of the thermal response and not a multiple of power supply frequency (50 Hz). The inset in figure 5 shows that the variation \( V_3 \) with the cube power of injected current is highly linear in agreement with equation (1). The computed value of the thermal conductivity is 140 W m\(^{-1}\) K\(^{-1}\) which is close to the value for bulk silicon with the same doping level (130 W m\(^{-1}\) K\(^{-1}\)).

2.3. Piezoresistivity measurements

Bending of the substrate and measurement of the resulting device resistance variation is the most common technique for piezoresistance or piezoresistivity measurements of strain gauges made in nanomaterials. We considered that the following conditions should be fulfilled to get high quality and complete measurements by this technique:

(i) A direct application of stress on the nanowire die. In most works, the method used to apply stress on the nanowire under test is bending of a plate on which the nanowires die is glued. Such indirect bending produces a stress field transmitted to the nanowire die which is largely dependent on the glue layer stiffness and which can be inhomogeneous. Consequently a reference strain gauge must be integrated in the nanowires die to get accurate, although relative, measurements,

(ii) The ability to apply a static or a dynamic stress. Indeed, a dynamic stress loading was found necessary to avoid resistance variations due to charges exchanges between native oxide trap and bulk of Si nanowires which can lead to an apparent giant piezoresistance [4],

(iii) An homogeneous stress field in a sufficiently large area to allow a comparison of a set of nanowires with various dimensions and fabricated in the same run,

(iv) Measurements as function of temperature to get temperature coefficients of piezoresistivity,

(v) Measurements in vacuum to avoid resistance variations due to humidity or other adsorbed species and to avoid thermal exchanges by convection.

In this work, the piezoresistance measurements were performed with the set-up depicted in figure 6 which follows these recommendations. It is based on \textit{in situ} four point direct bending of the nanowire die in the vacuum chamber of the same cryogenic probe station as for thermal conductivity measurements described above. As expected, this system allows simultaneous application of a tensile stress on nanowires and measurements under probes of their resistance. The additional benefits of this system are its operation in vacuum (\( \leq 10^{-5} \text{ mbar} \)) and its ability to allow dynamic stress loading, measurements below and above room temperature (from 200 K to 400 K), as well as a simultaneous optical visualization or measurement. More details on the set-up design and mechanical modelling can be found in [26] and its operation and characteristics will only be summarized here. The silicon die mechanical loading is obtained by an external large range (180 \( \mu \text{m} \)) and large maximum force (500 N) piezoelectric actuator with an embedded strain sensor for close loop control. This actuator pushes, with the help of two columns, an aperture rigid frame holding the fixed outer loading rods of the four point bending system. The inner bottom rollers of the four point bending system are supported by a tilting mechanical part which rests on button force sensor. The force sensor manufacturer electronics was replaced by a home-made low current electronics to avoid excessive sensor heating which prevented operation at low temperature. Tests with calibrated weights showed that the force sensor can then be operated at temperatures down to 200 K. Measurements at lower temperatures can be performed by replacing force measurement by an optical measurement of the die deformation [26]. The set-up was designed to minimize loading and supporting rods misalignments and asymmetries. For an ideal and symmetric four point bending system, the uniform surface stress generated in the area between inner supporting
bars is given by:

\[ \sigma = \frac{3Fa}{W_D t_D^2} \]

where \( W_D \) and \( t_D \) are, respectively the width and thickness of the die, \( a \) is the distance between outer and inner bars (see figure 6), and \( F \) is the applied force. In the developed system \( a = 8.5 \text{ mm} \) and a surface stress higher than 250 MPa can be applied on a 20 mm × 20 mm × 725 \( \mu \text{m} \) Si(100) die. This stress value is in the range of bending fracture strength values that we measured for such dies (217–540 MPa) in agreement with the ones reported for 525 \( \mu \text{m} \) thick polished Si wafers [27].

An example of nanowire piezoresistance measurement at room temperature is shown in figure 7. It shows that the piezoresistance is highly linear in the investigated stress range (0–50 MPa) and that good quality measurements in terms of noise and stability can be achieved with the developed set-up.

3. Results and discussion

3.1. Thermal conductivity of Si-p nanowires

Equation (1) above shows that thermal conductivity measurements by the \( 3\omega \) method require additional static measurements of the nanowire resistance and of the temperature coefficient of resistance (TCR) \( \alpha \). Despite some scattering of measured values, some general trends could be observed. When the nanowire size was reduced, its resistance was found to increase faster than the variation expected from a purely geometrical variation in agreement with a larger effect of depletion width due to positive surface charges. The temperature dependence of the resistance was found linear in the 200–380 K range although some departure from linearity could not be excluded for the narrowest (80 nm) nanowires. A trend towards an increase of the TCR when the nanowire width is decreased and possibly when the nanowire length is increased was observed (see table 1) but no well-defined dependence could be evidenced. Consequently, as a first approximation, the average value \( \alpha = 7.6 \times 10^{-6} \text{ K}^{-1} \) was used for the evaluation of thermal conductivity from \( 2\omega \) measurements of nanowires with different dimensions.

Our experimental results consistently showed that the behavior of the third harmonic of the voltage drop was well described by equation (1) for the investigated nanowires. This shows that heat conduction in the measured devices obeys Fourier’s law of heat conduction as this is the basic assumption of the \( 3\omega \) method. In semiconductors, heat conduction can generally proceed through the motion of charge carriers and through the propagation of phonons related to lattice vibrations. In the case of silicon, heat conduction is generally dominated by phonon transport and is known to decrease with doping. So thermal transport by diffusion is not obvious because in nanowires the mean free path of phonons can be larger than nanowire dimensions, notably its cross section. In that case ballistic transport can occur and the \( 3\omega \) method becomes questionable. Our results show that inelastic phonon scattering at the walls of the nanowires is likely sufficiently high and the nanowires sufficiently long to get a heat transport limited by diffusion. This could be different for...
nanowires with smoother side walls, such as nanowires etched by silicon anisotropic chemical etching limited by crystal planes.

Our results of thermal conductivity measurements are shown in figure 8. As expected, they consistently show a large decrease of thermal conductivity compared to bulk silicon value when the nanowire width is reduced. Comparison with published work shows that values are lower than those of thin Si films [19] but larger those of VLS nanowires having a similar width but lower thickness [28].

3.2. Piezoresistivity of Si-p nanowires

The longitudinal piezoresistive coefficients $\pi_L$ of Si-p (100) nanowires aligned along (110) direction with different widths have been measured as a function of temperature. It was extracted from the measured relative variations of resistance $\Delta R/R$ and the longitudinal stress values $\sigma$ computed from equation (4) by using the following equation:

$$\frac{\Delta R}{R} = \pi_L \sigma.$$  \hspace{1cm} (5)

If geometrical piezoresistance effect is neglected, for a p-type silicon nanowire oriented along (110) direction, $\pi_L$ is related to the coefficients $\pi_{ij}$ of the piezoresistive tensor in the crystallographic coordinate system by:

$$\pi_L = \frac{1}{2}(\pi_{44} + \pi_{12} + \pi_{11}) \approx \pi_{44}/2,$$  \hspace{1cm} (6)

where the second approximate equality comes from the much lower values of $\pi_{11}$ and $\pi_{12}$ with respect to $\pi_{44}$ in p type doped silicon [29]. All measured nanowires had the same width (160 nm) and the same boron dopant concentration ($1.5 \times 10^{19} \text{ cm}^{-3}$). The results of $\pi_L$ measurements are compared with values for bulk silicon and the same doping level in figure 9. These raw data show an increase of the piezoresistive coefficient of the nanowires when their width is reduced below about 260 nm. This would indicate that a slight giant piezoresistance effect is observed despite the high doping level and the relatively large sizes of the nanowire cross section. Let us emphasize that a dynamic stress loading at 0.02 Hz was applied for these measurements. According to [4], a giant piezoresistance effect should not be observable in this condition as it is mainly due to the variation of Si depletion width near the surfaces due to stress-induced charge exchanges between silicon and slow water traps in the native oxide. Our values are measured in vacuum, thus without humidity, but, like in all other published works, they are likely overestimated by a factor decreasing with nanowire width because of a variable stress concentration. This stress

Figure 8. Thermal conductivity of boron doped (110) Si nanowires with various dimensions (a) as a function of ambient temperature and (b) at 300 K as a function of nanowire width, and comparison with bulk silicon (dashed line). Nanowire thickness: 160 nm, boron doping: $N_A = 1.5 \times 10^{19} \text{ cm}^{-3}$.

Figure 9. Compilation of measured longitudinal piezoresistive coefficients versus temperature of Si-p (110) nanowires with different widths and comparison with bulk silicon. Nanowires thickness: 160 nm, Boron dopant concentration $1.5 \times 10^{19} \text{ cm}^{-3}$.
concentration is expected because of the width difference between the Si part released by lateral underetching near the anchors and the nanowire. For a width reduction by a factor 3.25 (from 260 nm to 80 nm) the ratio of piezoresistive coefficient is also close to 3. Finally, figure 9 also shows that the temperature coefficient of the longitudinal piezoresistive constant of Si nanowires is similar to the one of bulk silicon with the same doping level (−0.9 TPa K⁻¹) [29] and only weakly variable with nanowire width.

4. Conclusion

In this work we measured the thermal conductivity and longitudinal piezoresistive coefficient of silicon nanowires fabricated by surface machining of an (100) SOI wafer and aligned along (110) direction. The thermal conductivity was measured in vacuum by the 3ω method with relatively large driving currents owing to the implementation of a cancellation circuit of the 1 ω component of the signal. Measurements show that heat conduction in 80–260 nm wide, 160 nm thick and a few μm long nanowires follows Fourier’s law likely because of the inelastic scattering on slightly rough sidewalls. Despite a scattering of the data due to variations of initial resistance and TCR values, a large decrease of the thermal conductivity was unambiguously observed when the nanowire size was reduced. Piezoresistance measurements were performed by a four point die bending system implemented in situ in a cryogenic probe station. The size effect on nanowire piezoresistance was found limited when a dynamic stress loading was applied. This supports the assumption that a large giant piezoresistance effect can only be observed in static mode.

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References

[1] Toriyama T, Tanimoto Y and Sugiyama S 2002 J. Microelectromech. Syst. 11 605

Table 1. Temperature coefficient of resistance of Si-p nanowires with different lengths L and widths w. Average value: α = 6.7 × 10⁻³ K⁻¹.

| w (nm) | 80 | 140 | 140 | 200 | 200 | 200 | 260 |
|--------|----|----|----|----|----|----|----|
| L (μm) | 5.2 | 2.8 | 2.5 | 2.5 | 2.5 | 4  | 5.2 |
| α (×10⁻³ K⁻¹) | 1.13 | 1.1 | 0.58 | 0.36 | 0.51 | 0.28 | 0.77 |

[2] He R and Yang P 2006 Nat. Nanotechnology 1 42
[3] Reck K, Richter J, Hansen O and Thomsen E V 2008 Proc. IEEE Conf. Microelectromech. Syst. (Tucson AZ, January 13–17, 2008) 1 71
[4] Milne J S, Rowe A C H, Arscott S and Renner C 2010 Phys. Rev. Lett. 105 226802
[5] Mile E, Jourdan G, Bargatin I, Labarthet S, Marcoux C, Andreucci P, Hentz S, Kharrat S, Colinet E and Duraffourg L 2010 Nanotechnology 21 165505
[6] Fernandez-Reguzel M, Plaza J A, Lora-Tamayo E and San Paulo A 2010 Microelectronics. Eng. 87 1270
[7] Allain P E, Bosseboeuf A, Parrain F, Maoroufi, S, Coste P and Walther A 2013 IEEE J. Microelectromech. Syst. 22 716
[8] Cao A, Sudhîsîter J J and de Smet L C 2014 Sensors 14 345
[9] Denami F, Ni L, Rogel R, Salan A C and Pichon L 2012 Sensors Actuators B 170 158
[10] Park I, Li Z, Pisano A P and Williams R S 2010 Nanotechnology 21 015501
[11] Patolsky F, Zheng G and Lieber C M 2006 Anal. Chem. 78 4260
[12] Zhang G J and Ning Y 2012 Anal. Chim. Acta 749 1
[13] Hu L and Chen G 2007 Nano Lett. 7 3249
[14] Peng K-Q and Lee S-T 2010 Adv. Mater. 23 198
[15] Allain P E, Le Roux X, Parrain F and Bosseboeuf A 2013 J. Micromech. Microeng. 23 015014
[16] Lehee G, Parrain F, Bosseboeuf A and Riuo J C 2014 Proc. IEEE Design Test Int. and Packaging of MEMS/MOEMS (Cannes, France 1–4 April 2014)
[17] Bandaru P R and Pichanaskom P 2010 Semicond. Sci. Technol. 15 024003
[18] Ashegi M, Kurabayashi K, Kasnavi R and Goodson K E 2002 J. Appl. Phys. 91 5079
[19] Li D, Wu Y, Kim P, Yang P and Majumdar A 2003 Appl. Phys. Lett. 83 2934
[20] Liu L and Chen X 2010 J. Appl. Phys. 107 033501
[21] Bourgeois O, Fournier T and Chaussy J 2007 J. Appl. Phys. 101 016104
[22] Cahill D G, Fischer H E, Klitsner T, Swartz E T and Pohl R O 1989 J. Vac. Sci. Technol. A7 1259
[23] Rowe A C H 2014 J. Mater. Res. 29 731
[24] Lu L, Yi W and Zhang D L 2001 Rev. Sci. Instrum. 72 2996
[25] Parrain F, Allain P E, David-Grignot S, Bosseboeuf A and Walther A 2013 Instrumentation et interdisciplinarité: capteurs chimiques et physiques N Jaffrezic-Renault (Les Ulis, France: EDP Sciences) pp 291–300
[26] Bosseboeuf A, Allain P E, Parrain F, Jacob S, Poisat A, Isac N, Perrot S and Walther A 2013 Instrumentation et interdisciplinarité: capteurs chimiques et physiques N Jaffrezic-Renault (Les Ulis, France: EDP Sciences) pp 307–14
[27] Kahn H, Troyer M J, Prabhu V R, Shih C L, Phillips S M, Huff M A and Heuer A H 1998 Ceram. Trans. 86 119
[28] Ashegi M, Kurabayashi K, Kasnavi R and Goodson K E 2001 J. Appl. Phys. 91 5079
[29] Cho C H, Jaeger R C and Shulting J C 2008 IEEE Sensors J. 8 1455