SoAx: A generic C++ Structure of Arrays for handling particles in HPC codes

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Abstract

The numerical study of physical problems often require integrating the dynamics of a large number of particles evolving according to a given set of equations. Particles are characterized by the information they are carrying such as an identity, a position other.

There are generally speaking two different possibilities for handling particles in high performance computing (HPC) codes. The concept of an Array of Structures (AoS) is in the spirit of the object-oriented programming (OOP) paradigm in that the particle information is implemented as a structure. Here, an object (realization of the structure) represents one particle and a set of many particles is stored in an array. In contrast, using the concept of a Structure of Arrays (SoA), a single structure holds several arrays each representing one property (such as the identity) of the whole set of particles.

The AoS approach is often implemented in HPC codes due to its handiness and flexibility. For a class of problems, however, it is know that the performance of SoA is much better than that of AoS. We confirm this observation for our particle problem. Using a benchmark we show that on modern Intel Xeon processors the SoA implementation is typically several times faster than the AoS one. On Intel’s MIC co-processors the performance gap even attains a factor of ten. The same is true for GPU computing, using both computational and multi-purpose GPUs.

Combining performance and handiness, we present the library SoAx that has optimal performance (on CPUs, MICs, and GPUs) while providing the same handiness as AoS. For this, SoAx uses modern C++ design techniques such template metaprogramming that allows to automatically generate code for user defined heterogeneous data structures.

Keywords: C++, Heterogeneous data, Template metaprogramming, Generic programming

PROGRAM SUMMARY/NEW VERSION PROGRAM SUMMARY

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Nature of problem: Structures of arrays (SoA) are generally faster than arrays of structures (AoS) while AoS are more handy. This library (SoAx) combines the advantages of both. By means of C++(11) meta-template programming SoAx achieves maximal performance (efficient use of vector units and cache of modern CPUs) while providing a very convenient user interface (including object-oriented element handling) and flexibility. It has been designed to handle list-like sets of particles (similar to struct int id; double[3] pos; float[3] vel;) in the context of high-performance numerical simulations. It can be applied to many other problems.
Solution method: Template Metaprogramming, Expression Templates
Reasons for the new version: *
Summary of revisions: *
Restrictions: *
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References
[1] Reference 1

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Particles are at the heart of many astrophysical, environmental or industrial problems ranging from the dynamics of galaxies over sandstorms to combustion in diesel engines. Investigating such problems require generally integrating the dynamics of a large number of particles evolving according to a given physical laws. Examples are N-body simulations in cosmology [1][2], particle in cell codes (PIC) exploring plasma physics [3][4] or hydrodynamic simulations studying Lagrangian turbulence problems [5][6]. Such kind of numerical simulations have in common that they are numerically expensive meaning that they rely on number crunching, i.e. an enormous number of floating point operations. Studying the particle dynamics during a finite time interval requires the numerical integration of the underlying equations of motion over many time steps so that the particle data (position, velocity, ...) is used in simple but numerous repeated operations. The performance of such operations depend in a crucial way on how the particle data is stored and accessed. For instance, the importance of spatial locality in memory access is a well known issue when it comes to the scalability of code performance on parallel architectures [7].

Modern supercomputers are often indispensable for studying challenging problems. Their architecture got more and more complex in recent years. The today’s fastest computers consists of several performance sensible components such as multi-level caches, vector units based on the ’single-instruction multiple-data’ (SIMD) concept, multi-core processors, many-core (MIC) and GPU accelerators. Evidently it is important to make use of all these components to optimize the performance of a numerical code.

Particles can carry different properties such as an identity, a position or a mass. In programming languages such as Fortran, C or C++, the data types int, double and float, could be chosen to represent the former particle properties. In this paper codelets (serving as implementation examples) will always be chosen to represent the former particle properties. In this paper...

This way, individual particles can easily be generated as objects (Particle p;) and modified (p.id = 42). A set of particles is then often handled by an array- or list-like structures (std::list<Particle> pList;) providing functionalities such as access, adding and removal of particles. Such an organization is called array of structures (AoS) as the particles are represented by a structure that is hold by an array (or list).

Another implementation strategy for handling a set of many particles is to use one structure that holds several arrays; one array for each particle property:

```cpp
Listing 3: Member function to allocate memory for particle property arrays

class PartArr {
    public:
        int* id;
        double* position;
        float* mass;
    }
```

It is then convenient to add member functions to this class that perform operations on all the properties such as allocating memory:

```cpp
Listing 3: Member function to allocate memory for particle property arrays

void PartArr::allocate(int n) {
    number = new int[n];
    position = new double[n];
    mass = new float[n];
}
```

In the same way, member functions for adding, removing and other functionalities could be added. This kind of implementation is called structure of arrays (SoA) from the fact that in this case one structure handles a set of particles whose properties are represented by different arrays. PartArr pArr; creates a set of particles and an individual particle is referenced by the array index (pArr.position[42] returns the position of particle 42). A priori, particles cannot be extracted as individual objects from the structure PartArr. For this, a structure Particle (see codelet above) would be needed together with a function copying the array data for one index to the Particle member variables. From these considerations it is clear that AoSs are easier to implement and to use than SoAs.
tion for a slightly different particle type that requires the addition of a property such as a charge. AoS are more flexible than SoA for this task: the novel property could be added to the Particle structure by simply adding the member variable float charge;. In the case of a SoA an array (through float* charge;) could be added to PartArr. But in turn, all member functions such as allocate would also have to be updated in order to treat the added array.

AoS seem to be the better candidate to store particles than SoA. However, SoA are faster in many circumstances (especially on MIC and GPUs) \[8,9,10\] than AoS and we show that this is also the case for typical manipulations (such as trajectory integration) on particle data. By means of a benchmark modeling floating-point operations used in real codes we show that SoAs are typically several times faster than AoSs and that the performance of an AoS depends on the size (in terms of bytes) of the structure (Particle in the example above). In order to cope with the seemingly contradicting properties handiness, flexibility and performance, the implementation has to use advanced programming techniques. C\*\* allows for abstractions that permit to access data via a AoS pattern while data is arranged in memory as a SoA. In this paper, we present another generic implementation of a SoA called SoAx that has optimal performance while providing the same handiness and flexibility of an AoS.

This paper is organized as follows. In section 2 we benchmark the performance of AoS and SoA on CPUs. In section 3 we discuss a similar benchmark on GPUs and MICs. The generic C\*\* implementation of SoAx is presented in section 4. Conclusions are drawn in 5.

2. Benchmarking AoS and SoA on CPUs

In order to compare the performance of SoA and AoS we measure the execution time of a benchmark computation. The latter consists in performing an Euler advection time step for the position \( x \) of a set of particles

\[
x^+ = x + dtv,
\]

where \( dt \) denotes the time step (a floating point number) and \( v \) the velocity of the particle. This equation is a simple prototype for typical operations appearing in numerical codes. It consists, for each component, of two loads from the heap memory plus one for the constant \( dt \), usually from the stack, and one store in heap memory.

For benchmarking AoS we use the structure

```c++
// Listing 4: Particle structure used in the benchmark. SIZE is the number of supplementary floats.

template<int SIZE>
class Particle
{
    public:
        float x[3];
        float v[3];
        float temp[SIZE];
};
```

where temp is a place holder for additional particle properties that might be necessary for the physical problem under consideration (such as a mass, an electric charge...) or the numerical algorithm (such as temporary positions and velocities for a Runge-Kutta scheme). In the case of SoA we simply use three heap-allocated C\*\* arrays for \( x \) and \( v \), respectively.

Typically, in numerical simulations many successive time steps are performed in order to integrate the particle dynamics. In our benchmark we therefore loop many times over the numerical implementation of \( f \) and average. The code is compiled with gcc 5.1. As optimization flags we use -O3 and SIMD hardware specific flags such as -avx2.

Figure 2 compares the normalized execution time for the SoA and AoS as a function of the particle number. The SoA is much faster than the AoS. Their relative performance is shown in Fig. 3. The SoA implementation is up to 25 times faster than the AoS and one gains at least a factor of two to three by using a SoA instead of an AoS.

The measured performance depends on the number of particles which is a consequence of the different cache levels of modern CPUs. Usually they provide three levels with sizes of 32 kByte (L1), 256 kByte (L2), and 8–40 MByte (L3). The colored arrows in Fig. 2 show the cache limits in terms of a the number of particles of a certain size (in terms of bytes). One observes that the performance is maximal when the L1 cache is filled and all particle data still fits into the L2 cache. When the particle data size exceeds the L2 cache, the execution time slightly increases. An important performance drop happens when data becomes larger than the L3 level. At that point data has to be transferred from the main memory that has a significantly lower bandwidth than the caches.

![Figure 2](image-url)
One architectural component that has changed over the years is the performance measured with a given benchmark naturally depends on the architecture of the CPU. However, it is important to note that the just discussed relative performance (SoA vs. AoS) will not or only weakly depend on the clock speed. But other differences, especially the vectorization units are important as we will show now. We will consider two different CPU architectures distinguished by the date of their commercial release. This sheds light on how the ‘SoA vs AoS’ performance ratio changed over time. We compare the SoA performance to the maximal AoS performance (using the smallest possible particle size together with a stl vector). In Fig. 4 we compare Xeon CPUs from 2010 and 2014. For the two CPU generations SoA clearly wins over AoS. But the modern chip has a higher performance gain. Over only four years the gain has nearly doubled.

Figure 4: Benchmark comparing SoA and AoS for different CPU generations distinguished by the date of their commercial launch. 2014: Intel Xeon E5-2680 v3 (Haswell EP); 2010: Intel Xeon X5650 (Westmere EP)

This also explains the observed differences between the two CPU architectures. From one CPU generation to the other, the register width and the set of instruction has been augmented. The old CPU from 2010 has 128 bit vector register containing eight single precision floating point values. At intermediate particle numbers (10^3-10^6) the gain is around two and vanishes for higher particle numbers. The origin of these regimes can be found in the three cache levels: The gain is maximal if all data fits into the L2 cache. The second regime corresponds to data fitting into the L3 cache. However, when the data size exceeds the latter the vectorization gain vanishes because the data has to be loaded from the main memory which is too slow to efficiently fill the vector registers.

Vectorization does not speed up AoS computations. Apparently, the auto-vectorizer of the compiler does not manage to create a substantial gain if a AoS is used. This means that a part of the SoA superiority can be explained by the fact that SoA effectively use the CPU vector units.

This drawback can be overcome when the ordering of particles is not important. In that case, a particle can be removed by simply overwriting it with the last particle. This strategy is used by default by SoAx.

The performance measured with a given benchmark naturally depends on the architecture of the CPU. However, it is important to note that the just discussed relative performance (SoA vs. AoS) will not or only weakly depend on the clock speed. But other differences, especially the vectorization units are important as we will show now. We will consider two different CPU architectures distinguished by the date of their commercial release. This sheds light on how the ‘SoA vs AoS’ performance ratio changed over time. We compare the SoA performance to the maximal AoS performance (using the smallest possible particle size together with a stl vector). In Fig. 4 we compare Xeon CPUs from 2010 and 2014. For the two CPU generations SoA clearly wins over AoS. But the modern chip has a higher performance gain. Over only four years the gain has nearly doubled. The CPU architecture is more and more constructed in a way that favors the SoA layout.

One architectural component that has changed over the years is the performance of the vector unit. All today’s CPUs possess so-called single instruction multiple data (SIMD) register and associated instruction sets. These allow to perform the same instruction (such as an addition) to many floating-point number at a time (in one cycle) that can significantly speed up code. In Fig. 5 we compare the performance of SoA and AoS with and without the use of the vector unit. The vectorization gain of a SoA reaches four to five for small particle numbers of the order of 100-1000 particles. The theoretical gain is eight as the used CPU has a 256 bit vector register containing eight single precision floating point values. At intermediate particle numbers (10^3-10^6) the gain is around two and vanishes for higher particle numbers. The origin of these regimes can be found in the three cache levels: The gain is maximal if all data fits into the L2 cache. The second regime corresponds to data fitting into the L3 cache. However, when the data size exceeds the latter the vectorization gain vanishes because the data has to be loaded from the main memory which is too slow to efficiently fill the vector registers.

This also explains the observed differences between the two CPU architectures. From one CPU generation to the other, the register width and the set of instruction has been augmented. The old CPU from 2010 has 128 bit vector register with a SSE4.2 instruction set and the most recent CPU from 2014 has a 256 bit vector register with an AVX2 instruction set. The factor of two between the 128 bit and 256 bit register explains the differences in Fig. 4 for intermediate particle numbers. Of course other features than the vector unit changed among CPU architectures but it seems that most of the changes in the ‘SoA vs AoS’ performance ratio over the years are due to optimizations of the vector units.
3. Benchmarks on MICs and GPUs

Today’s supercomputer often use accelerators to speed up computationally intensive parts of numerical codes. Mainly two different accelerator types exist:

Intel recently introduced the ‘many integrated core’ (MIC) concept with the Xeon Phi co-processor (Knights Corner) that assembles many computing cores (around 60) on one chip. The used computing cores are simplified versions of commonly used CPUs so that numerical code compile without changes on a Xeon Phi.

Nvidia and AMD/ATI developed graphics processing units (GPU) that are now often used in high performance computing. This architecture uses hundreds to thousands of very simple computing cores to speed up high parallel algorithms. For these GPUs the numerical code has to be especially designed.

The importance of these accelerators for HPC is underlined by the fact that they are massively employed by the fastest supercomputers in the world (according to the TOP 500 list, www.top500.org).

3.1. MIC

During the last decade, the performance of supercomputers grew essentially by increasing the number of (standard) computing cores so that high performance computing demanded more and more for parallel numerical algorithms and codes. Intel pushes now further in the direction of massive parallel programming by introducing co-processors, called Xeon Phi, with around 60 integrated cores each. A single core is in general compatible to standard CPUs but exhibits some architectural differences that are important for the performance of SoAs and AoSs: A Xeon Phi has no L3 cache but only a 32 kByte L1 and a 512 kByte L2 cache per core. Another aspect is that the vectorization capacities have been improved by extending the SIMD registers to 512 bits which means that either 16 single precision floating point number or 8 double precision number can be processed in one cycle.

These design differences show up in the relative performance of AoS compared to SoA (as before, we will only study the single-core performance). Our benchmark (compiled with intel’s icc 15) shows the the MIC cores favor SoAs over AoS and that even more than standard CPUs. For small size objects and intermediate particle numbers the tested SoA is roughly ten times faster than the AoS (see Fig. 5). If the stored particle has a considerable size, this difference even varies between twenty and forty.

The reason is the extended vector performance of the MIC cores. Up to the point when the L2 cache is filled, vectorization speeds up the computation by a factor of roughly ten (see Fig. 7) which is below the optimal value of sixteen but twice the speed-up measured for a standard CPU. Again, the cache size limits the particle number range for this speed-up.

3.2. GPU

The architecture behind the General Purpose Graphical Processing Units (GPU) uses a divide and conquer philosophy, by
providing a many-core device, separated from the CPU, and typically connected to this one via a PCIe band. Graphic cards are widely used as accelerators in computer clusters, and power many of the TOP500 fastest supercomputers.

A few thousand of threads can run concurrently on the graphic card, thus providing the possibility to process many elements at a time. Furthermore, the architecture, labeled SIMT (for Single Instruction, Multiple Thread) is somewhat different from the SIMD in that every single thread has its own register state and can have independent behaviors from the others, a feature allowing a thread-based as well as coordinated threads development.

Another important difference from the CPU is the role of the L1 cache. Different caches co-exist, each one belonging to a given streaming multiprocessor, a structure responsible to dispatch the work among the threads. This cache is mainly used for register spilling and some stack variables. It does not promote temporal locality so that repeated operations on the same memory locations will not necessarily benefit from this cache. The L2 cache, shared among all streaming multiprocessors, will be used instead. We thus expect the SoA pattern not to benefit from the L1 cache, but the AoS will in fact benefit from it: indeed, loading a large structure into memory allows threads to reuse close memory.

A benchmark similar to those listed above is performed. The graphic card used is a Nvidia Tesla M2050, a middle-range, widespread computing device. The card has 448 cores, spread among 14 multiprocessors and the L2 cache size is \( \sim 786 \) kBytes. In the SOA algorithm, three functions are launched, one per position and velocity component, with a number of threads such that each thread has a single element to process. The L2 cache, shared among all streaming multiprocessors, will be used instead. We thus expect the SoA pattern not to benefit from the L1 cache, but the AoS will in fact benefit from it: indeed, loading a large structure into memory allows threads to reuse close memory.

The major drawback of the AoS approach is the well know effect of uncoalesced memory access, hence threads fetch unneeded data in the cache lines. This is particularly damageable in the case of GPU computing because the major weak point is the latency of memory access. Accessing data is done by a single, indivisible group of 32 threads, called a warp. Loading a large structure in a thread memory, only to read a small part of it, degrades badly the memory access performance up to a factor of 32. The case AoS with \( SIZE = 0 \) packs 6 values and will then have a memory performance of \( 1/6 \approx 16\% \) compared to SoA, and the highest values of \( SIZE \) will display a performance down to \( 1/32 \approx 3\% \). This is shown in Fig. 8. As a result, one can clearly see that the performance per particle saturates for a sufficiently large number of particles, with SoA pattern outperforming the AoS with \( SIZE = 32 \) by a factor of 20 and the AoS with \( SIZE = 0 \) by a factor of 2. For small particle numbers, performance is hindered by a less effective usage of memory, additional to the uncoalesced access pattern, as can be seen in Figure 10.

It is also noticeable that the performance of SoA is slightly worse than AoS for small particle numbers (up to 1000). This can be attributed to the fact that when the number of particles is small enough, the L1 cache and the threads registers are large enough to keep the whole particles close in memory, hence allowing faster access to other position and velocity components for successive operations, while the SoA pattern has to make a request to global memory for every needed data. Nevertheless, this effect only brings advantage when the particle number is small. When this number increases, the cache cannot hold the data anymore and so that the global memory is used and another long latency fetch has to be performed. The caching advantage is thus eventually taken over by the poor memory access performance, and the crossing between SoA and AoS (with \( SIZE = 0 \)) occurs around \( 2000 \) particles. This corresponds to a full utilization of the L1 cache which is \( 48 \) kB, the size of one SoA (\( SIZE = 0 \)) particle being \( 6 \times 4 = 24 \) bytes.

![Figure 8: Benchmark comparing the execution time of AoS vs SoA implementation of the Eulerian update step in single precision.](image)

We also performed this simple benchmark on another multi-purpose graphic card boarded on a desktop computer. For this example, we used the Nvidia Geforce GT755M, composed of 384 cores on 2 multiprocessors, with \( \sim 262 \) kbytes. Timings were \( 2 - 3 \) times slower, irrespective of the number of particles and both for AoS and SoA (not shown here), illustrating the benefit of using a graphic card specifically dedicated to high performance computing exhibiting more parallelism.

The benchmarks have been performed with relatively old graphic cards. However, although the performances are expected to be better for both SoA and AoS cases with a more modern graphic card, we do not expect the qualitative comparison between these two memory layouts to vary. Modern GPUs are capable of exposing more parallelism, which we expect to result in an even greater gap between the two memory layouts.
for each particle property, the associated access functions and member functions that allow efficient handling of all arrays.

4.1. Using SoAx

Before discussing details of the implementation let us first show a short listing presenting some functionality of SoAx. Let us assume that we want our particles to have an identity, a position, a velocity, and a mass of types int, double, double, and float, respectively. Let us further assume that we need three-dimensional coordinates for the position and velocity. Here is what one could write using SoAx:

```cpp
Listing 5: Example code showing typical usage of SoAx

// Define particle properties through macro
SOAX_ATTRIBUTE(id, 'N'); // identity
SOAX_ATTRIBUTE(pos, 'P'); // position
SOAX_ATTRIBUTE(vel, 'V'); // velocity
SOAX_ATTRIBUTE(mass, 'M'); // velocity

// Specify types and dimension and
// concatenate attributes using std::tuple
typedef std::tuple<
    id<int, 1>,
    pos<double, 3>,
    vel<double, 3>,
    mass<float, 1>> ArrayTypes;

// create SoA for 42 particles
Soa<ArrayTypes> soax(42);

// access properties of particle 23
soax.id(23) = 0; // set identity
soax.pos(23, 0) = 3.14; // set x-coordinate

// operations on all particles (x=v_x-v_i)
soax.posArr(0) = soax.velArr(1) - soax.velArr(2);

// allocate memory of 100 particles
soax.resize(100);
```

4.2. Implementation of SoAx

SoAx uses inheritance in combination with template meta-programming. The basic idea is to inherit all arrays (particle properties) into one single structure. The different property types of the particle are passed to the SoAx class using

```cpp
Listing 6: Example of using SoAx elements

auto particle = soax.getElement(7);
particle.id() = 42;
particle.pos(0) = 3.14;
soax.push_back(particle);
```

We have payed attention to the fact, that user might want to extract and treat particles as objects (in the spirit of struct Particle). With SoAx one can write

```cpp
4. Generic C++ implementation of a structure of arrays (SoAx)

In the introduction we have seen that implementing, maintaining and using a structure of array can be annoying. We present now an implementation of a structure of array using modern C++ (in fact C++11), called SoAx (see https://sourceforge.net/projects/soax for updates and bugfixes), that provides a handy interface, high flexibility and optimal performance. We use C++ because it enables powerful mechanisms to build abstractions without loss of performance. We discussed in the introduction that adding a property (such as a charge) to a particle requires the modification of all member functions (such as PartArr::allocate) that handle the different arrays. C++ allows to pass this task to the compiler. Using template meta-programming [12], the needed code can be automatically generated during the compilation. The result is a class that contains an array

![Figure 9: Loading efficiency from the main GPU memory. This is the ratio between requested memory and effectively used memory.](image)

![Figure 10: L1 cache hit rate for global memory load requests, in percents.](image)
standard::tuple. This is a component of C++11 storing heterogeneous data types.

A SoAx attribute consists of an array for storing and member-functions for accessing data. We have chosen to generate these attribute classes by macros to avoid repetitive implementations as they have all the same structure. Macros permit to give custom names to the attributes: From SOAX_ATTRIBUTE(pos, 'p'); the compiler creates a class with a member-function pos to access individual particles and posArr to access directly the complete array. The character p is only a descriptive string that can be used by the user for other purposes. pos<double, N> is an instantiation of the class template holding a N-dimensional array of type double.

Let us here mention that advanced programming techniques can be used to provide usage safety. The dimensionality is for example automatically taken into account for the member function pos. In the case of pos<double,3>, pos(42,0) gives the expected access to the first coordinate of particle 42 while pos(42) yields a compile-time assertion (through ‘substitution failure is not an error’ (SFINAE, [13])). The behavior is the opposite in the case of id<int,1>, where id(42) is the identity of particle 42 and id(42,0) results in a compile-time assertion.

Advanced programming techniques also allow to enable the library user to write automatically optimized code. The line soax.posArr(0) = soax.velArr(1) - soax.velArr(2); in List.5 performs an operation on all particles. The library user does not need to write a custom for-loop for CPUs or a CUDA kernel for GPUs. For this, SoAx uses a technique called expression templates [14, 13] where a computation such as a sum is encoded in a template. Chained arithmetic operations are analyzed at compile time and an optimized code without unnecessary copies is generated by the compiler. This technique is nowadays used in linear algebra software [15].

4.2.1. Adding functions

The user can easily add custom functions to SoAx that he wants to be applied to all arrays. For this, it is not necessary to touch the code of the library. The user only has to define a structure containing a doIt member-function (see List.7 for an example). The first template parameter of this member doIt is a reference to one of the SoA arrays. Other parameters can be freely chosen (internally SoAx uses variadic templates). Here is an example of a function that sets the values of all arrays to a certain value:

```cpp
struct SetToValue
{
    template<T, class Type>
    static void doIt(T& t, Type value)
    {
        for(int i = 0; i < t->size(); i++)
            t->operator[]()[i] = value;
    }
};
```

Passing this function to a SoAx object soax as a template argument,

```cpp
soax.apply<SOAX::SetToValue>(42);
```

This is achieved via recursive templates. We discuss this programming technique here as a showcase for the doIt function as it explains how templates can be used to make the compiler generate code without loss of performance (see List.8). In fact, the SoAx member-function apply calls the member-function doIt of the class template TupleDo with the particle attribute tuple (Tuple), its size (N) and the user defined template (DoItClass = e.g. SetToValue) as template arguments. The member-function doIt calls recursively TupleDo::doIt for the attribute tuple but passing a decremented size. This recursion continues until the passed size is one so that the compiler chooses the partially specialized case below. Its doIt member-function calls the doIt function of the user provided DoItClass that terminates the treatment of the first entry of the attribute tuple Tuple. After that the DoItClass::doIt is called for the second entry. This process continues for all attributes. As the code for all calls is generated at compile time, there is no performance overhead compared to a hand-written code.

Listing 8: Example explaining compile time code creation by recursive templates

```cpp
#define TupleDo
template<TUPLE, N, class DoItClass>
struct TupleDo
{
    template<Args...>
    static void doIt(Tuple& t, Args... args)
    {
        TupleDo<Tuple, N-1, DoItClass>::doIt(t, args...);
        DoItClass::doIt(std::get<N-1>(t), args...);
    }
};

#define DoItClass
template<class Tuple, class DoItClass>
struct DoItClass
{
    template<Args...>
    static void doIt(Tuple& t, Args... args)
    {
        DoItClass::doIt(std::get<0>(t), args...);
    }
};
```

4.2.2. GPU implementation

Several restrictions apply when working with GPU processors. A first one is the costly data transfer between CPU and GPU: one has to design a solution in which those transfers are minimized. Data should reside mainly on the GPU and be transferred to the main memory only when needed by the CPU, for example for output to a hard drive. One thus cannot make use of solutions that would result in dereferenciation by the CPU of each elements one at a time, but must rely on device functions that process all data at once on the device. In addition, when processing multiple vectors with several operations, pro-
cessing them all together is faster than successively, an optimization sometimes referred to as loop fusion (see Wikipedia for an example). These constraints lead us to make again use of expression templates for device data.

Another constrain comes from the fact that C++-stl vectors are not designed to work on GPU processors within the CUDA framework, as far as the version 7.0, and another type of data storage is then needed. To allow expression templates to work with GPUs, we build a custom class, called deviceWrapper, encompassing a pointer to data living on the device. In addition, we used the THRUST library [16], version 1.8.0, as it provides the best mimic of stl vectors structure and algorithms to our knowledge. This allows us to keep trace of the associated device vector to allow efficient operations to be performed on the data.

When an assignment (of the form `soax.posArr(0) = soax.velArr(1)-soax.velArr(2)`; ) is performed, a kernel is called and passed a copy of the underlying deviceWrapper object, accessing the data with the expression template objects. The copy constructor of the deviceWrapper class then needs to be overloaded in order to copy only the raw device pointer and not all the data at each call.

Fig. 11 shows a benchmark evaluating the performance of this implementation for the operation (1) as a function of the particle number, along with the SoA and AoS (with SIZE = 32) implementations as references. The time is measured this way with a std::chrono rather then with the kernel profiler, allowing to assess the possible overhead of the SoAx solution. The version of the used CUDA version is 7.0. With this benchmark, we confirm that the performance of SoAx is the same as the SOA also on GPUs. Indeed, the SoAx GPU implementation comes down in fine to call a kernel on the stored data addressed through expression templates.

5. Conclusions

The goal of the work is two-fold. First, it shows that heterogeneous data (such as particles) should be implemented in an array of structure (AoS) fashion rather than in a structure of array (SoA) one if performance is crucial. AoS are generally much faster on modern CPUs as well as on GPUs. The reason is that AoS better uses cache and vectorization resources that can speed up typical number crunching algorithms on particles by more than one order of magnitude. However, implementing and maintaining AoS can be cumbersome especially if the the number of numerical types representing a particle change from one application to another. SoA are in general more handy and flexible. This consideration leads to the second contribution of this work showing that modern C++ programming techniques permits to combine the advantages of both concepts (SoA and AoS) to build a generic library that has the performance of SoAs and the flexibility and handiness of AoS. We demonstrate the benefit of template meta programming for scientific codes. This technique delegates code generation to the compiler and allows for highly readable, maintainable and fast application code. The presented library SoAx runs on CPUs as well as on GPUs.

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