Research on Control Method of Neutral Point Potential Balance of T-Type Three-level Inverter Based on PLECS

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Abstract. The T-type three-level inverter topology has the advantages of low electromagnetic interference, high efficiency, and low output harmonic content. This article combines constant power inverter, independent control of active and reactive power output, Analyzed and studied the neutral point potential balance control of the T-type three-level inverter topology. Through PI adjustment control on the amount of charge of the capacitor, the midpoint voltage of the capacitor is always maintained in a balanced state, and the fluctuation of the midpoint voltage is controlled within ±0.23%. This method can effectively avoid the influence of the difference of capacitance parameters on the DC side on the midpoint voltage. The PLECS software simulation verifies the reliability of the capacitor voltage equalization circuit under the condition of the voltage imbalance at the midpoint of the DC side voltage source supply capacitor voltage equalization.

1. Introduction

The T-type three-level inverter has the advantages of low output voltage harmonic content, low voltage change rate, and low EMI. At present, it has very important applications in medium and high voltage and high power applications. The T-type three-level topology is improved on the basis of the diode-clamped three-level inverter. Two clamp diodes are reduced on each arm of the circuit, which can reduce conduction loss and reduce inverter Volume. It is a promising inverter topology \textsuperscript{[1]}. However, the three-level midpoint clamped inverter circuit structure has the inherent defect that the midpoint potential of the DC side will fluctuate. The fluctuation of the midpoint potential is harmful to the stability of the system, so it is necessary to solve it \textsuperscript{[2]}.

On the basis of the above research, according to the principle of PWM modulation, by obtaining the capacitor midpoint voltage error function, choose the optimal PID factor to apply to the three-phase modulation wave of the PWM controller, and apply the obtained switching state signal to the inverter, eliminates the traditional modulation steps, and a T-type three-level inverter neutral-point potential balance control method based on capacitor neutral-point voltage error control is studied. The control is flexible and simple, and it can obtain good tracking effects. The response is fast, and the balance control of the midpoint voltage can be realized.
2. Topological structure of T-type three-level inverter

2.1. Mathematical model and test circuit of T-type three-level inverter

The circuit topology of the T-type three-level photovoltaic grid-connected inverter is shown in Figure 1. Here, a DC voltage source is used to replace the output voltage of the photovoltaic cell. The three-phase output of the inverter is connected to the grid through the RL load. The phase inverter consists of 12 switching devices (IGBT). Each phase of the inverter contains 4 switching devices. VTi1 and VTi2 are respectively connected to the positive bus and negative bus of the DC supply voltage. VTi3 and VTi4 are connected to the midpoint and The load constitutes a two-way switch, where i=a,b,c. C1 and C2 are voltage divider capacitors.

![Fig.1 T-type three-level inverter test main circuit](image)

2.2. Mathematical model and test circuit of T-type three-level inverter

Due to the structural characteristics of the T-type three-level inverter circuit, the output terminal of each phase bridge arm of the inverter is connected to the midpoint of the DC side voltage divider capacitor under certain switching states. Therefore, when the inverter is working normally, it will have current flowing in or out of the midpoint of the series capacitor, charging and discharging C1 and C2 unbalancedly, causing the midpoint potential to change continuously. Through the analysis and summary of the data, it can be seen that the main reasons for the unbalance of the neutral point potential of the neutral point clamped three-level inverter are: The capacitance parameters cannot be caused by the difference in the manufacturing process of the capacitor or the aging of the capacitor application They are completely consistent, so the charging and discharging are not uniform, causing the midpoint potential to shift; the presence of switching delay characteristics; the impact of changes in the grid current; the power factor will also affect the midpoint potential \[3\].

The unbalanced midpoint potential will cause many harms to the inverter system. When connected to the grid, the output voltage waveform of the inverter will be distorted, and the output voltage waveform distortion will aggravate the imbalance of the midpoint potential; at the same time, it will cause damage to the switching devices; the voltage divider capacitor is continuously charged and discharged, which also shortens the service life . Therefore, the balance control of the midpoint potential is very critical \[4, 5\].

When the midpoint current flows into and out of the DC side capacitor, it will inevitably cause the stored charges of the two capacitors to change, which will cause the midpoint potential to fluctuate. At this time, the equivalent circuit of the inverter's DC side is shown in Figure 2.
In the figure, $R_e$ represents the equivalent resistance of the line equivalent resistance, the equivalent impedance of the capacitor, and the equivalent resistance of the inverter loss. $I_s$ is the output current of the DC side of the inverter, $I_{in}$ is the input current of the inverter, and $U_{dc}$ and $i_{dc}$ are the DC bus voltage and current.

Based on the above reasons, considering the realization of the balance control of the midpoint potential, the voltages on the two capacitors need to be equal, then there is

$$V_{C1}(t) = V_{C2}(t) = \frac{U_{dc}}{2}$$  \hspace{1cm} (1)

Assuming that the current at the midpoint of the DC side capacitors $C1$ and $C2$ is $i0$, ideally, it is expected that $C1=C2=C$, then

$$i_{C1}(t) = i_{C2}(t) = \frac{i0(t)}{2}$$  \hspace{1cm} (2)

It can be seen that when the DC voltage source is fixed, the main reason for the midpoint potential imbalance is caused by the size of the midpoint current value, and this current value directly reflects the change of the capacitor midpoint potential deviation value:

$$\Delta V = \frac{i0}{C}$$  \hspace{1cm} (3)

Comprehensive production practice, because the capacity of the bus capacitor is a certain value, the midpoint current value can be reduced by controlling the change of the midpoint voltage, and the balance control of the midpoint potential can be realized.

3. Design of midpoint voltage balance controller

3.1. Control strategy and active and reactive constant power control

The control principle is shown in Figure 3. It controls the entire system by detecting the variable of the voltage at the midpoint of the balancing capacitor. The degree of control depends on the processing of the error signal of the voltage at the midpoint of the two capacitors.

Fig.3 Block diagram of model predictive control principle
Combined with the circuit of Figure 1, when the voltages on the voltage-balancing capacitors C1 and C2 are inconsistent for some reason, it corresponds to the voltage difference $\Delta V = V_{C1} - V_{C2}$ is not zero. $V_{C1}$, $V_{C2}$ in the circuit are taken from both ends of the capacitor.

In order to solve the voltage imbalance and inverter failure, the solution adopted is when the voltage on the capacitor C1 is greater than the voltage on the capacitor and C2, that is, when $V_{C1} > V_{C2}$, in order to make the midpoint potential of the capacitors C1 and C2 in a balanced state, it is necessary to accelerate the release of the energy stored on C1 and slow down the release of the energy stored on C2; on the contrary, when the voltage on the capacitor C1 is less than the voltage on the capacitor and C2, that is, when $V_{C1} < V_{C2}$, in order to make the center of the capacitors C1 and C2 When the point potential is in a balanced state, it is necessary to slow down the release of the energy stored on C1 and accelerate the release of the energy stored on C2.

First, the Vabc signal of the power grid is used to obtain the synchronization signal $\omega t$ through coordinate transformation and a three-phase synchronous phase-locked loop SRF-PLL circuit.

Then perform abc/dq transformation from the three-phase current $I_{3ph}$ to obtain the $I_d$ and $I_q$ components, which are respectively approximated with the PID output of the active power setting parameter $P^*$ and the reactive power setting parameter $Q^*$, and the approximated error signal is output through the PID respectively. The dq/abc inverse transform obtains a three-phase synchronously modulated sine wave signal, which is input to the m terminal of SPWM.

In the circuit of Figure 4, P and Q are the active and reactive feedback values of the system respectively, and m is the input end of the sine wave modulation wave, and the signal amplitude is usually $m \leq 1$, which corresponds to the modulation coefficient. When m increases, the output current, line-to-line voltage and line-to-neutral voltage all increase.

3.2. Implementation of control strategy

According to the above analysis, the steps to realize the balance control of the capacitor midpoint potential are as follows:

1. Voltage error signal sampling. The voltage signal is directly taken from the capacitors C1 and C2, and the sine wave modulation coefficient $m \leq 1$. It is necessary to ensure that the offset ratio superimposed on m is less than 20%. For this purpose, a scheme is designed:

$$\Delta V = (V_{C1} - V_{C2}) \left/ \sqrt{\frac{(V_{C1} + V_{C2})}{2}} \right.$$

2. PI proportional integral transformation. In order to achieve better balance control, the $\Delta V$ error signal is subjected to PI calculation by a proportional integrator to obtain a tiny modulation wave compensation variable and then superimposed on the modulation signal m. This method can be attributed to a fuzzy control method.
4. Simulation and result analysis

Use PLECS Version 4.1.2 for simulation experiment, DC bus voltage \( V_{dc} = 900V \), inductance \( L = 1.372e-4H \), resistance \( R = 4.309e-3\Omega \), \( C = 1e-3F \), \( RC = 4.7e2\Omega \), grid frequency \( f_1 = 50Hz \), Carrier signal frequency \( f_c = 2450Hz \), \( T_s = 1e-6 \). When \( RC = 470\Omega \) is connected in parallel with the capacitor \( C_2 \), the capacitor midpoint voltage balance control is applied in the first 1s, and then the capacitor midpoint voltage balance control is cancelled. The waveform is shown in Figure 5.

![Waveform](image)

(a) Complete waveform within 2s  (b) Partial waveform within 0.4s

Fig. 5 Comparison waveforms of whether the voltage balance control at the midpoint of the capacitor is applied or not

Figure (a) is the result of applying the capacitor midpoint voltage balance control in the first 1s, and then canceling the capacitor midpoint voltage balance control. From Figure (a) and Figure (b), it can be obtained that the balance control circuit is applied to stabilize within 0.35s; without balance control, the voltage at the midpoint of the capacitor is completely unbalanced in more than 1s. Enlarging the graph (a) in the stable interval of the waveform, it can be obtained that the voltage difference between the two voltage divider capacitors on the DC side is maintained at ±2.0V, and the fluctuation amplitude is small. From this, the control range can be obtained: \((451.025 - 450)/450 = 0.23\% \) or \((450 - 448.975)/450 = 0.23\% \), and the control range can be controlled within ±0.23%. At the beginning of the circuit work, the midpoint potential of the capacitor showed a convergence trend, which proved that the adopted control method realized the balance control of the midpoint potential.

Next, verify that the power factor will affect the midpoint potential. The reactive current component will cause the periodic fluctuation of the midpoint potential, and the active current component will cause the offset of the midpoint potential and gradually accumulate. In the simulation process, the reactive current component and the active current component are artificially controlled to obtain the waveform in Figure 6.
The implementation of the above control strategy verifies the effectiveness of the control. This control scheme also has a good control effect for load imbalance.

5. Conclusion
This paper studies the control method of the T-type three-level inverter based on the proportional integral fuzzy control. It starts from the circuit topology of the T-type three-level inverter and analyzes the reasons that affect the potential imbalance at the midpoint of the capacitor. Start with the effect of the three-phase modulation wave of the three-level three-level inverter, and design the capacitor midpoint voltage error controller. Compared with the traditional method, this method has: (1) The realization process is simple and flexible, and does not require complex process processing; (2) The dynamic response speed is fast, and the simulation results show that the capacitor midpoint voltage is stable at 0.35s. The grid-connected current is stable in 0.02s; (3) It can balance the midpoint potential of the T-type three-level inverter, and can output high-quality waveforms. The results of PLECS simulation test prove that the proposed control method is correct and effective, and the control scheme is easy to realize and has practical application value.

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