This letter presents a wide dynamic range (WDR) feature extraction (FE) readout scheme for machine vision applications using CMOS image sensors (CISs). The proposed scheme with the proposed pixel structure has two operating modes, the normal and WDR modes. In the normal operating mode, the proposed CIS captures a normal image with high sensitivity. In addition, as a unique function, a bi-level image is obtained for real-time FE even if a pixel is saturated in strong illumination conditions. Thus, compared to typical CISs for machine vision, the proposed CIS can reveal object features that are blocked by light in real time. In the WDR operating mode, the proposed CIS produces a WDR image with its corresponding bi-level image. A prototype CIS was fabricated using a standard 0.35-μm 2P4M CMOS process with a 320 × 240 format (QVGA) with 10-μm pitch pixels. At 60 fps, the measured power consumption was 5.98 mW at 3.3 V for pixel readout and 2.8 V for readout circuitry. The dynamic range of 73.1 dB was achieved in the WDR operating mode.

Introduction: CMOS image sensors (CISs) have been used in a wide variety of applications, including mobile devices and computer vision-based intelligent systems [1]. The field of machine vision systems has rapidly grown in recent years. As a result, object detection and recognition using CISs have become important functions for extracting the features of a target object. In addition, consumer demand for real-time feature extraction (FE) is increasing for applications such as the Internet of Things and augmented reality.

FE from a target object is mainly based on obtaining a bi-level image from a human-friendly image. Therefore, the accuracy of the FE is closely related to CIS performance in terms of dynamic range, sensitivity, and frame rate. For example, when there is a weak contrast between an object and its surrounding environment, it becomes difficult to identify object features owing to the limited sensitivity of typical CISs. In addition, when an object is illuminated by strong light that is out of its dynamic range, the object is shown as covered by light. That is, light intensity information is lost because pixels are saturated. Thus, in machine vision, high sensitivity and a wide dynamic range (WDR) are essential for accurate FE. Furthermore, considering the operating latency in digital image processing for FE, it is desirable to simultaneously obtain a human-friendly image with its bi-level image for real-time FE.

Until now, various studies have achieved high sensitivity and WDR performance for mobile applications [2, 3]. Based on these studies, we propose a WDR-FE readout scheme for a machine vision CIS. The proposed CIS has two operating modes, the normal and WDR modes, and bi-level images are obtained for real-time FE. In the normal operating mode, the proposed CIS simultaneously captures an image with high sensitivity and extracts its bi-level image. In addition, as a unique function, it reveals the features of a target object even when the image is saturated by strong light. In the WDR operating mode, the dynamic range of the proposed CIS is extended, and a WDR image is obtained along with its bi-level image.

Structure and operating principles: The simplified pixel layout and equivalent proposed pixel structure schematic are shown in Figure 1. The proposed pixel structure is designed based on a conventional 3T-APS structure [4], which is composed of a high-sensitivity photosensing region on the odd side (PD_odd) and a low-sensitivity photosensing region on the even side (PD_even). The ratio of the area of each sub-region and the entire photosensing region is approximately 0.5. The sensitivity of PD_odd is reduced by shielding its photosensing region with metal layers. This reduces the amount of light that illuminates the PD_even photosensing region. Note that the sensitivity (S) of a pixel is given by $S = \frac{A_{pixel}}{FF} \cdot \eta \cdot (1.24 \cdot CP_D)$ [5], where $A_{pixel}$ is the pixel area, $FF$ is the fill factor, $\lambda$ is the wavelength, $\eta$ is the quantum efficiency, and $CP_D$ is the integration capacitance of the photodiode. A photogate is located in the middle of PD_odd and PD_even, and it can be electrically connected to $C_{PD_odd}$ and $C_{PD_even}$ through the channel formed under the photogate with a positive bias voltage ($VPXO$). $C_{PD_odd}$ and $C_{PD_even}$ represent the integration capacitance of PD_odd and PD_even, respectively. Here, a negative bias voltage is used for electrically disconnecting $C_{PD_odd}$ and $C_{PD_even}$.

Figure 2 shows the simplified schematic of the proposed single-column single-slope (SS) ADC. It consists of a conventional SS ADC and an inverter-based bi-level detector. Every readout column shares a ramp generator based on a current digital-to-analogue converter (I-DAC). There are two outputs in the proposed pixel structure, that is, $VPXD$ from PD_odd and $VPXE$ from PD_even. These outputs are selectively read out through an analogue multiplexer according to the operating mode. When pixel readout begins, the bi-level detector starts to observe whether the pixel output ($VPXO$) exceeds the predetermined reference ($V_{REF} - V_a$) or not. Here, $V_a$ is a threshold voltage of $MP$ in the bi-level detector.

The basic concept of the proposed WDR-FE readout scheme is to obtain the feature information of a target object even when an image is saturated. In other words, $VPXD$ is used for normal imaging with high sensitivity, and $VPXE$ is used for representing object features that are out of the dynamic range. This results in a WDR-FE. When pixel readout begins in the normal mode, the SS ADC first digitises $VPXD$ and the bi-level detector simultaneously extracts bi-level information for $VPXD$. If
the result of A/D conversion ($D_{OUT}$) for $V_{PD0}$ represents the maximum code in the full ADC reference ($D_{FULL}$), then $V_{PXi}$ is selected and only the bi-level detector operates again to obtain its bi-level value. Based on this value, the object feature can be represented in the form of bi-level information (same as a binary image) even when pixels are saturated. When pixel readout begins in the WDR mode, a positive voltage $V_{PG}$ is applied to the photogate for electrically connecting $C_{PDE}$ and $C_{PDE}$; this gives $C_{PDE} = C_{PD0} + C_{PDE} + C_{PDE}$. Hence, the proposed pixel structure exhibits the dynamic characteristics of $(Q_{PDE} + Q_{PDE})C_{PD0}$, which can be expressed as $V_{PXE} = (Q_{PDE} + Q_{PDE})/C_{PD0}$ ($C_{PD0} \approx C_{PD0} \gg C_{PG}$). This is equivalent to averaging $V_{PD0}$ and $V_{PE}$ (i.e., $V_{PEX}$). Hence, the noise performance and dynamic range of the pixel structure are improved and WDR imaging is achieved.

Figure 3 shows the operation timing diagram and its waveform in two operating modes to provide an explicit explanation of the proposed readout scheme. In the normal mode (Figure 3(a)), when $\Phi_{SE}$ becomes high, the analogue correlated double sampling operation for $V_{PXi}$ is performed at node $V_{PD}$ of the first comparator. Note that $V_{PD0}$ is selected by default ($\Phi_{SD0}$ is high). When $\Phi_{SE}$ is high, $V_{PXE}$ changes to ‘logic high’ because $V_{PXi}$ exceeds $V_{REF} - V_{pb}$. Its result ($D_{SD0}$) ‘1’ is stored in the additional latch (2-bit latch) as the FE result with high sensitivity. Then, the SS A/D conversion is performed when $\Phi_{CE}$ is high. If $D_{OUT}$ is equal to $D_{FULL}$, then $\Phi_{SE}$ becomes high for obtaining additional information from the pixel represented as $D_{FULL}$. The bi-level detector checks $V_{PXE}$ when $\Phi_{SD0}$ is high. If $V_{PXE}$ exceeds $V_{REF} - V_{pb}$, $V_{PXE}$ changes to ‘logic high’, and its result ($D_{SE}$) is stored as the FE result with low sensitivity. If $D_{SE}$ is ‘1’, it implies that there is an object blocked by light. $D_{SD0}$ is utilised as the object feature information under the condition of pixel saturation, resulting in WDR-FE. Note that the bi-level image is synthesised by adding $D_{SE}$ and $D_{SD0}$ in off-chip digital processing. Finally, $\Phi_{SE}$ and $\Phi_{SD0}$ become high for sampling the pixel reset value in the same manner as the conventional CIS with 3T-APS. In contrast, in the WDR mode (Figure 3(b)), $\Phi_{PG}$ is high during the pixel readout period. Then, the A/D operation for $V_{PXi}$ is performed in the same manner as the normal mode. Therefore, in the normal mode, WDR-FE is performed while maintaining high sensitivity. In addition, in the WDR mode, noise performance and the dynamic range are improved by the proposed pixel structure.

Experimental results: The prototype chip was implemented using a standard 0.35-μm CMOS process. The microphotograph of the chip is shown in Figure 4. The size of the chip is 4 × 4 mm. It consists of a 320 × 240 format (QVGA) with 10-μm pitch pixels and a 10-bit column-parallel SS ADC array with the ramp generator, including control circuitry and I/O pads. The fill factor of the proposed pixel structure is 75.8% on the odd side ($PD_0$) and 84.8% on the even side ($PD_1$). Additional test channels are added to the prototype chip to evaluate the performances of the proposed pixel structure and single-column SS ADC. The performance of the prototype CIS is verified in various test conditions by applying a control voltage ($V_{	ext{REF}}$) through an external DAC mounted on the evaluation board. Note that $V_{	ext{REF}}$ can be changed according to the desired FE condition. A negative voltage of 0.5 V and a positive voltage of 4 V are applied for $V_{PD0}$ in the proposed pixel structure.

Figure 5 shows the measured response of the proposed pixel structure according to light intensity. The linearity of the proposed pixel structure was verified by performing the measurement in two operating modes, that is, $PD_0$ and $PD_1$ in the normal mode and $PD_{SUM}$ in the WDR mode. The results demonstrate that the proposed CIS provides a dynamic range of 73.1 dB in the WDR mode while maintaining linearity for light intensity.

The measured maximum differential non-linearity and integral non-linearity of the proposed SS ADC are 0.87 and 1.24 LSB, respectively, as shown in Figure 6. Table 1 summarises the performance of the prototype CIS. The power consumption was 5.98 mW at 60 fps. Off-chip digital offset adjustment was performed to reduce fixed-pattern noise as described in [6].

Sample images in the two operating modes were captured by the prototype CIS when the left side of the object was illuminated by strong light. The images are shown in Figure 7. In the normal mode with $V_{	ext{REF}}$ at approximately 0.7 V (Figure 7(a)), the left side of the object is indistinguishable because the image is saturated. Real-time bi-level images are captured with and without the proposed WDR-FE readout scheme. With the proposed readout scheme, the bi-level image reveals perceptible object features even outside the dynamic range of the prototype CIS. In the WDR mode with $V_{	ext{REF}}$ at approximately 0.55 V (Figure 7(b)), the
Table 1. Performance of the proposed CMOS image sensor (CIS)

| Parameter          | Value                  |
|--------------------|------------------------|
| Technology         | 0.35 μm CMOS process   |
| Total area         | 4 × 4 mm               |
| Supply voltages    | 3.3 V (pixel), 2.8 V (circuit) |
| Number of pixels   | 320 (H) × 240 (V)      |
| Detector type      | p-n junction diode     |
| Fill factor        | PDO: 38.5% (8.4% (PDE))|
| Sensitivity        | PDO: 327 mV/lx·s (PDE: 56 mV/lx·s) |
| Random noise       | 0.92 LSB rms           |
| Total fixed-pattern noise | 1.89 LSB max         |
| ADC resolution     | 10 bits                |
| ADC input range    | 1.2 V                  |
| Dynamic range      | 59.4 dB (in normal mode) |
| WDR-FE             | X                      |
| Power consumption  | 5.98 mW                |
| Frame rate         | 60 fps                 |

Fig 7 Sample images captured by the proposed CMOS image sensor. (a) Normal image and its bi-level image in normal mode. (b) WDR image and its bi-level image in WDR mode.

Table 2. Performance comparison

| Parameter                  | [7] | [8] | [9] | This work |
|----------------------------|-----|-----|-----|-----------|
| WDR method                 | DCG | DSMT| LOFITreC| PDS       |
| Process technology         | CIS | CMOS| CMOS| CMOS      |
| Supply (V)                 | -   | 3.3 | 3.3 | 3.3/2.8   |
| Pixel size (μm²)           | 1.5 | 7.1 | 16  | 10        |
| FF (%)                     | -   | 27.3| 52.8| 38.5 (PDO3) |
| DR (dB)                    | 83.8| 104 | 130 | 73.1      |
| WDR-FE                     | X   | X   | X   | O         |

Abbreviations: DCG: Dual conversion gain; DSMT: Dual storage and multiple transfers; LOFITreC: Lateral overflow integration trench capacitor; PDS: Photo-diode summation.

Conclusion: In this letter, a WDR-FE readout scheme is introduced for machine vision CISs. The proposed CIS has two operating modes, that is, the normal and WDR modes, and bi-level images are extracted in real time. In the normal mode, the proposed CIS captures the normal image with high sensitivity. Additionally, as a unique function, the bi-level image is extracted even when the pixel is saturated. In the WDR mode, the proposed CIS obtains the WDR image with its bi-level image. From a commercial perspective, the proposed scheme could be utilised in machine vision applications to track the movement of a target object under strong light intensity.

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