Analysis of MEMS electrostatic energy harvesters electrically configured as voltage multipliers

Binh Duc Truong, Cuong Phu Le and Einar Halvorsen, Member, IEEE

Abstract—This paper presents the analysis of an efficient alternative interface circuit for MEMS electrostatic energy harvesters. It is entirely composed by diodes and capacitors. Based on modeling and simulation, the anti-phase gap-closing structure is investigated. We find that when configured as a voltage multiplier, it can operate at very low acceleration amplitudes. In addition, the allowed maximum voltage between electrodes is barely limited by the pull-in effect. The parasitic capacitance of the harvester and non-ideal characteristics of electronic components are taken into account. A lumped-model of the harvesting system has been implemented in a circuit simulator. Simulation results show that an output voltage of 22 V is obtained with 0.15 g input acceleration. The minimum necessary ratio between the maximum and minimum capacitances of the generators which allows operation of the circuit, can be lower than 2. This overcomes a crucial obstacle in low-power energy harvesting devices. A comparison between the voltage multiplier against other current topologies is highlighted. An advantage of the former over the latter is to generate much higher saturation voltage, while the minimum required initial bias and the minimum capacitance ratio in both cases are in the similar levels.

Index Terms—MEMS, electrostatic energy harvester, voltage multiplier, low-power system, diode-capacitor network

I. INTRODUCTION

Vibration-based energy harvesting can provide reliable alternative power sources for emerging miniaturized-electrical devices such as implant medical/wireless sensors [1], [2]. As a key element connecting the harvester and storage component or electrical load, power electronic interface circuitry has gained significant interest in recent years. Abundant research on circuit topology with functions of voltage regulation, optimal power extraction and damping control for energy harvesting systems has been conducted and presented [3]–[7]. In this paper, we focus on the power electronics for micro capacitive energy harvester.

Several topologies of power electronic interface circuit for MEMS electrostatic energy harvesters are reported. For instance, Yen et al. proposed a simplified circuit in which a charge pump was used with a fly-back circuit to store and transfer extracted energy [8]. The major drawback of this architecture is that the storage capacitor acts as parasitic capacitance to the energy converter, reducing the net power harvested. The power consumption of the control unit of the switch is also a challenging concern as it must be supported by the generator, even in ASIC implementations [9], [10].

In addition, the use of bulky inductor is not applicable to miniaturization of the harvesting system.

Besides the switched-inductor topologies, diode-capacitor voltage multipliers are widely used for converting an AC input voltage into a DC output voltage. Based on Bennett’s doubler of electricity, de Queiroz et al. proposed an inductor-less and switch-less doubler circuit [11], [12]. The major advantage of this topology is a simple and robust implementation. However, the circuit requires a ratio $C_{\text{max}}/C_{\text{min}}$ between maximum and minimum capacitances of the variable capacitors to be greater than 2. This is a critical challenge in practice since MEMS harvesters tend to exhibit small variable capacitances, limited by standard fabrication processes and device size.

An advanced topology for vibration electrostatic energy harvesters was recently proposed by Lefeuvre et al. [13], [14]. An argument based on theoretical analysis using a rectangular Q-V cycle suggests that this voltage multiplier can operate with a minimum necessary capacitance ratio lower than 2. However, one may have concerns regarding the accuracy of this assumption for the complex dynamic behavior of the circuit. Also, both simulations and experiments were for a macro-scale rotating variable-capacitor with $C_{\text{min}} = 45$ pF and $C_{\text{max}} = 155$ pF which clearly has $C_{\text{max}}/C_{\text{min}}$ much larger than 2.

This paper presents a new adaption of a voltage multiplier circuit to MEMS energy harvesting. This capacitor-diode network is based on the Greinacher’s voltage doubler which is the basic stage of a multiplier circuit first proposed by Greinacher in 1920 [15]. Since the micro energy harvesting system typically provides low output voltage that is not acceptable to switching converters, the multiplier topology is also a potential solution to initially boost such voltage to start-up the active elements of converter circuit [16]–[18]. A complete lump model including both mechanical and electrical domains is investigated. Parasitic capacitance of the generators and diode losses are taken into account. System dynamics are analyzed using a SPICE simulator. The performance of the introduced multiplier configuration is then compared to several circuits of the same family [13], [19].

II. ENERGY HARVESTER MODEL

Figure 1 shows the 2D geometry of the electrostatic energy harvester, which is used as a vehicle to explore the operation of a voltage multiplier configuration. The device includes two fixed electrodes attached to the frame and two variable electrodes on the proof mass suspended by four non-linear springs. The maximum displacement $x_{\text{max}}$ is limited by mechanical end-stops. Though an in-plane anti-phase gap-closing
asymmetric transducer is early used in sensing applications [20], [21], it is the first time introduced as an energy generator through this paper. An advantage of such structure is the capability to obtain large range of capacitance variation with small displacement, which allows the device to operate efficiently at relatively low input excitations. Meanwhile, the pull-in voltage is kept to a remarkably high value due to the anti-phase behavior of the two transducers. These characteristics make the structure interesting to investigate.

The capacitances $C_1$ and $C_{11}$ as functions of the proof mass displacement are

$$ C_{1/11}(x) = C_p + C_{1/2}(x), \quad (1) $$

$$ C_1(x) = C_0 \frac{1}{(1 + \frac{x}{g_1})(1 - \frac{x}{g_2})}, \quad (2) $$

$$ C_2(x) = C_0 \frac{1}{(1 - \frac{x}{g_1})(1 + \frac{x}{g_2})}, \quad (3) $$

where $C_0$ is the nominal capacitance of transducers, $C_p$ presents for the parasitic capacitance. The gaps between movable electrode and fixed electrodes $g_1$ and $g_2$ must be satisfied the condition $X_{\text{max}} < g_1 < g_1 + 2X_{\text{max}} < g_2$ so that the anti-phase characteristics is fulfilled $\frac{dC_1}{dx} < 0, \frac{dC_2}{dx} > 0$.

The nonlinear squeeze-film damping is proved to be essential to capture the device behavior [22], [23]. Meanwhile, the hardening restoring force could be useful to increase the device stability during operation. Along with the power conversion circuitry, the effect of the mechanical end-stops on the performance of a harvesting system is significant and cannot be ignored [24]. Therefore, all of them needs to be taken into account in device modeling. The dynamic of the spring-mass-damper system is then given by

$$ m\ddot{x} + B(x)\dot{x} + F_m(x) + F_e(x) + F_s(x) = F \quad (4) $$

where $m$ is the inertial mass and $F = mA\cos(\omega t)$ is the external force. Including the squeeze-film damping of the gap-closing capacitor structure [25] and an additional linear damping, the total damping force of the harvesters is $B(x)\dot{x}$, where

$$ B(x) = b_1 + \frac{b_n}{(1 + \frac{x}{g_1})^3} + \frac{b_n}{(1 - \frac{x}{g_2})^3} + \frac{b_n}{(1 + \frac{x}{g_1})^3} + \frac{b_n}{(1 - \frac{x}{g_2})^3}. \quad (5) $$

$F_m$ is the mechanical restoring force, which we consider on the Duffing-spring polynomial form

$$ F_m(x) = k_1x + k_3x^3. \quad (6) $$

The electrostatic force is represented by

$$ F_e(x) = \frac{1}{2}q_1^2 \frac{d}{dx} \frac{1}{C_1(x)} + \frac{1}{2}q_2^2 \frac{d}{dx} \frac{1}{C_2(x)} + C_p \quad (7) $$

where $q_1$ and $q_2$ are the charges on the two transducers. A stray capacitance $C_p$ in parallel with the variable capacitance is also included in the model. $F_s$ is the impact force between the movable mass and the rigid end-stops at the ultimate displacement $|x| > X_{\text{max}}$, which can be simplified as [26]

$$ F_s(x) = k_s\delta + b_n\dot{x} \quad (8) $$

where $k_s$ is the impact stiffness, $b_n$ is the damping coefficient accounting for the impact loss and $\delta = |x| - X_{\text{max}}$ is the deformation displacement between the proof mass and the end-stops during impact.

Based on the above equations, the equivalent circuit for the anti-phase gap-closing electrostatic energy harvesters is shown in Figure 2. Along with that is the proposed interface circuit, which includes two, namely, biasing capacitor $C_{b1}$ and $C_{b2}$ and five low-leakage diodes $D_1$, $D_2$, $D_3$, $D_4$ and $D_5$ (abbreviation, $D_{1-5}$). The output of the interface circuit is connected to a storage capacitor $C_s$ where the generated energy is stored. $C_s$ is initially precharged to a voltage of $V_0$. All model parameters are listed in Table I and are chosen close to the parameters of the MEMS electrostatic energy harvesters in [27].

III. OPERATION AND DYNAMICS OF THE TWO-STAGE VOLTAGE MULTIPLIER

In order to investigate the potential benefit of the circuit, the MEMS transducers are designed so that the capacitance variation ratio is

$$ \eta = \frac{C_{\text{max}} + C_p}{C_{\text{min}} + C_p} = 1.55. \quad (9) $$

Fig. 1. Anti-phase gap-closing vibration energy harvester.

Fig. 2. Lumped-model of electrostatic energy harvester configured as a voltage multiplier.
It is also the minimum ratio that is required for the harvester to work as a voltage multiplier. Note that the critical ratio for operation of the Bennet’s doubler is $\eta_{cr} = 2$, or even larger when the electrical losses are included. The variable capacitors here vary between $C_{min} = 30.79 \, \text{pF}$ and $C_{max} = 52.53 \, \text{pF}$. The capacitance variation of the two transducers are shown in Figure 3.

A dynamic model of the low-leakage diode BAS716 [28] is used for simulations in LT-SPICE, taking into account non-ideal properties such as built-in junction voltage, leakage current and $p$-$n$ junction capacitance. The SPICE model is much more complicated and realistic than constant-voltage-drop model or piecewise linear model. The capacitance value of the storage capacitor is first arbitrarily chosen large enough $C_s = 10 \, \text{nF}$ to minimize the ripple voltage at the DC output, while the biasing capacitance is kept much smaller $C_{b1} = C_{b2} = C_b = 0.5 \, \text{nF}$ to minimize start-up time.

Figure 4 shows waveforms of the voltages across capacitors and currents through diodes together with the proof mass displacement in the same time interval. The voltages across $C_{b1/b2}$ and $C_s$ increase slowly as functions of period of time, while that of variable capacitors have AC characteristics depending on the amplitude and frequency of the input acceleration. Use of the non-ideal diode model results in

![Figure 3](image1.png)

**Fig. 3.** The capacitance variation in anti-phase gap-closing transducers.

![Figure 4](image2.png)

**Fig. 4.** Simulated waveforms of the proof mass displacement, voltages across capacitors and currents through diodes. The input acceleration amplitude is $A = 0.5 \, \text{g}$. The driving frequency is kept at the constant value $f_0 = \sqrt{\frac{k}{m}} = 750 \, \text{Hz}$ and the initial bias voltage is $V_0 = 12 \, \text{V}$.

| Parameters                          | Values             |
|-------------------------------------|--------------------|
| Proof mass, $m$                     | 30.4 mg            |
| Linear stiffness, $k_1$             | 675.1 Nm$^{-1}$    |
| Hardening nonlinear stiffness, $k_2$| 2.7e7 Nm$^{-3}$    |
| Slide-film air damping, $b_1$       | 2.5e-5 Ns$^{-1}$   |
| Squeeze-film air damping, $b_2$     | 2.7e-5 Ns$^{-1}$   |
| Nominal capacitance, $C_0$          | 36.26 pF           |
| Parasitic capacitance, $C_p$        | 8.5 pF             |
| Lower gap between movable and fixed electrodes, $g_1$ | 16 µm |
| Upper gap between movable and fixed electrodes, $g_2$ | 40 µm |
| Maximum displacement, $X_{max}$     | 6.5 µm             |
| Impact stiffness, $k_s$             | 3.36e6 Nm$^{-1}$   |
| Impact damping, $b_s$               | 0.44 Ns$^{-1}$     |
| Bias capacitance, $C_{b1/b2}$       | 0.5 nF             |
| Storage capacitance, $C_s$          | 10 nF              |

**TABLE I**

**MODEL PARAMETERS**
strongly complex behavior of the diode currents. To analyze the complicated operation of the circuit, a sequence of four stages can be identified during a cycle.

In the first stage, from \( t_0 \) to \( t_1 \), \( C_1 \) (\( C_2(x) \)) starts increasing (decreasing) from the minimum (maximum) value. Conditions \( V_{C2} + V_{Ch1} > V_{C1} \), \( V_{C1} > V_{Ch2} \), and \( V_{out} + V_{Ch2} > V_{C1} > V_{out} \) are satisfied. All the diodes are blocked and the charges of \( C_1 \) and \( C_2 \) can be treated as constants.

The second stage is from \( t_1 \) to \( t_2 \). At the beginning, \( V_{C1} \) continues decreasing while \( V_{C2} \) is increasing. When \( V_{C2} > V_{C1} \), \( D_1 \) is conducting and \( C_1 \) is charged by \( C_2 \). Also, \( V_{Ch1} + V_{Ch2} > V_{C1} \) leads to conduction of the diode \( D_3 \) and the current flows from \( C_{b1} \), \( C_{b2} \) to \( C_1 \). This stage ends when \( C_1 \) reaches the minimum value \( C_{min} \) and \( V_{out} \) starts to rise.

In the next stage from \( t_2 \) to \( t_3 \), all diodes \( D_1-5 \) are reverse-biased, for the same reasons as above. However, \( C_1 \) now is decreasing from the maximum value \( C_{max} \) and the voltage across it increases again. The opposite happens to \( C_2 \).

In the final stage from \( t_3 \) to \( t_4 \), \( V_{C1} \) first continues increasing while \( V_{C2} \) decreases. This situation prevails until \( V_{C1} \) becomes larger than \( V_{C2} + V_{Ch1} \) and the diode \( D_2 \) begins to conduct transferring charge from \( C_1 \) and \( C_2 \) to \( C_{b1} \). Then, the voltage across \( C_1 \) changes only very slightly. In addition, when \( V_{C1} > V_{out} + V_{Ch2} \), the current flows from \( C_1 \) and \( C_{b2} \) to \( C_s \) while \( D_4 \) is conducting. When \( C_1 \) reaches \( C_{max} \), all conditions mentioned in the first stage occur and a new cycle starts. Note that the condition \( V_{out} > V_{C1} \) is rarely satisfied. The current that transfers the charge from \( C_s \) to \( C_1 \) through the diode \( D_5 \) is small and negligible. However, \( D_5 \) still plays a vital role for pre-charging \( C_1 \) at the very beginning of operation. In principle, \( D_5 \) can be disconnected through a switch in series after the first several cycles. This technique could result in higher saturation voltage [29], but is not our objective in this paper. Therefore, we choose to keep \( D_5 \) as part of the voltage multiplier, so that the attractive simplicity of the circuit is not compromised.

Figure 5 shows the time evolution of the output voltage with drive frequency \( f = f_0 = \frac{1}{2\pi} \sqrt{\frac{k}{m}} = 750 \) Hz, acceleration amplitudes \( A = 0.15 \) g and \( A = 0.25 \) g and initial pre-charge voltage \( V_0 = 8 \) V. The energy stored in \( C_s \) initially increases. The steady state is obtained after several cycles of operation and the accumulated voltage \( V_{out} \) is saturated at a certain level due to the effect of the electromechanical coupling [30]. Higher voltages result in stronger electrostatic forces causing a decrease of the proof mass displacement, and therefore \( \eta \). Higher input acceleration leads to a larger value of saturation voltage \( V_{sat} \). For instance, \( A = 0.25 \) g gives \( V_{sat} = 29.36 \) V while that of \( A = 0.15 \) g is \( V_{sat} = 22.32 \) V.

If the variable capacitor \( C_1 \) is replaced by a sinusoidal input voltage source \( v(t) = V_{in} \cos(\omega t) \) and all losses in diodes are neglected, the value of \( V_{out} \) is supposed to be two times higher \( V_{Ch1} \) and therefore \( V_{out} = 4V_{in} \). However, the relation becomes much more complicated when the input source is the actual voltage generated by MEMS energy harvester, i.e. \( V_{C1} \), since this voltage is now dependent on the mechanical vibration and may have time-varying amplitude. For example, the ratio of \( V_{out}/V_{Ch1} \) are 1.61 and 1.58 for \( A = 0.25 \) g and \( A = 0.15 \) g respectively. Simulation results also show that \( A = 0.12 \) g is the minimum required acceleration for efficient operation of the circuit, at the resonant frequency \( f = f_0 \).

Figure 6 shows variation of the output voltage at steady state obtained from simulations for each pair of acceleration amplitude and frequency (\( A, f \)). At a particular acceleration, when the vibration frequencies are within a certain range around the mechanical resonance, the system harvests energy and the voltage increases towards saturation. For frequencies outside this range, the necessary condition \( \eta \geq 1.55 \) is not satisfied due to small proof mass displacement. All the stored energy from precharge of the capacitor will then be dissipated resulting in zero output voltage after a certain time. It is clear that larger excitation strengths create a wider band of useful drive frequencies.

In order to understand the characteristics observed in Figure 6, we first consider dynamics of the proof mass at steady state. A comparison of normalized signal waveform \( x/X_{max} \) for
different acceleration amplitudes is shown in Figure 7 where $A = 0.15 \text{ g}$ and $A = 0.35 \text{ g}$ are taken as examples. Further simulation results show that, in the range of $A = 0.15 \text{ g} - 0.30 \text{ g}$, the displacement barely reaches the maximum value $X_{\text{max}}$ and hence $F_s = 0$. For higher excitation levels, the electrostatic force drives the proof mass toward (closer to) one side of the end-stop and the impact force between them periodically occurs.

We now examine an effective stiffness $K_{\text{eff}}$ of the anti-phase gap-closing device at steady state, which is given by

$$K_{\text{eff}} = \Re \left\{ \frac{\int_0^T F_{\text{ME}}(t) e^{-j\omega t} dt}{\int_0^T x(t) e^{-j\omega t} dt} \right\}, \quad (10)$$

where $F_{\text{ME}} = F_m + F_c + F_s$. The signals of $x(t)$, $F_m(t)$, $F_c(t)$ and $F_s(t)$ are extracted from simulations. The ratio between the effective resonant frequency $f_{\text{eff}} = \sqrt{K_{\text{eff}}/m}/2\pi$ and the mechanical resonant frequency is then

$$f_r = \frac{f_{\text{eff}}}{f_0} = \sqrt{\frac{K_{\text{eff}}}{k}}. \quad (11)$$

Figure 8 shows the changes of $f_r$ versus acceleration amplitude. In case of $A \in [0.15 \text{ g}, 0.30 \text{ g}]$, the resonant peak of the transducer is shifted downwards along with the rise of bias voltage due to the softening effect of the nonlinear electrostatic force. Therefore, lower input frequencies result in higher voltages. When $A > 0.30 \text{ g}$, the impact force dominates the electrostatic force and performs the hardening nonlinearity. The resonant peak thus increases in accordance with acceleration amplitudes and the output responses tend to increase with higher frequencies.

Our previous work showed that the saturation voltage of the Bennet’s doubler circuit does not depend on the initial bias $V_0$, and can be optimized by increasing the mechanical quality factor and adjusting stiffness [30]. These statements are still valid with the voltage multiplier configuration. In this paper, we continue exploring other aspects of the circuit such as effect of the biasing capacitor on start-up time (i.e., the time duration from the beginning to when the output voltage is saturated) and dependence of the ripple voltage on the storage capacitor. It is clearly that minimum start-up time and minimum ripple voltage would be desirable.

For simplification, all fixed capacitances are chosen equal $C_{b1} = C_{b2} = C_b$. Figure 9 depicts the effect of $C_b$ on the evolution of output voltage over time. The biasing capacitance $C_b$ almost does not affect the saturation voltage $V_{\text{sat}}$, but has strong influence to the required time duration until $V_{\text{sat}}$ is achieved. Therefore, the start-up time can be minimized with respect to $C_b$ so that the circuit can produce the same expected amount of the DC voltage faster. The start-up time used to distinguish between the transient and steady states is determined once the output voltage reaches 98% of the saturation.

Fig. 7. Comparison of the proof mass displacement at steady state for different acceleration amplitudes.

Fig. 8. Dependence of the ratio between the effective resonant frequency and the resonant frequency on input acceleration.

Fig. 9. The time evolution of the output voltage $V_{\text{out}}$ across $C_b$ for different values of $C_b$.

Fig. 10. Start-up time for different values of $C_b$. 
voltage. Simulation results obtained for a wide range of $C_b$ are shown in Figure [10]. The saturation voltage can be considered unchanged, while the shortest start-up time $t_{\text{min}} \approx 7.5$ s is found around $C_b = 0.4$ nF. Larger capacitances result in longer changing time for each multiplier-stage and thus slow down the start-up, but too small ones even increase the time sharply due to the undesired dynamic loading condition. From another perspective, $C_b$ has a significant impact on the cycle-to-cycle multiplication factor $z$ of the output voltage. The argument is similar to the one that was used to explain the influence of the storage capacitor on $z$ for the Bennet’s doubler circuit [11], [30].

Simulation results for the voltage ripple and the corresponding saturation voltage versus the storage capacitances are shown in Figure [11]. The ripple is determined as $(V_{\text{max}} - V_{\text{min}})/2$, where $V_{\text{max}}$ and $V_{\text{min}}$ are the highest and lowest peaks of the output voltage at steady state. Meanwhile, the saturation voltage is $V_{\text{sat}} \approx (V_{\text{max}} + V_{\text{min}})/2$. The ripple is found to be about 35 mV when $C_s = 0.5$ nF and increase with decrease of $C_s$. $V_{\text{sat}}$ is slightly reduced when $C_s < 50$ pF is used. Since our objective is to obtain a DC output voltage, it is desirable to choose as large a value of the capacitance $C_s$ as possible in order to minimize the ripple. However, the analysis presented in Figure [10] also holds for $C_s$, meaning that larger capacitances result in longer start-up time. Therefore, a good trade-off is needed here to keep both the ripple and start-up time at reasonable levels that are dependent on particular requirements of the output specifications.

At the input acceleration $A = 0.12$ g and the drive frequency $f = f_0$, simulations obtained for the low-losses diode BAS716 show that $V_0 = 6$ V is the minimum required initial bias for efficient operation of the circuit, so-called critical voltage $V_{\text{cr}}$. In previous work we proved that the use of a MOSFET connected in a diode-configuration as an alternative to the $p^+n$ diode could significantly reduce $V_{\text{cr}}$. Moreover, the diode-connected MOSFET is also a convenient option for integrated circuits. With the same MOSFET parameters given in [30], the value of $V_{\text{cr}}$ can be further lowered to 1.9 V.

### IV. Generalized N-stage Voltage Multiplier

The introduced circuit can be generalized to an N-stage voltage doubler as depicted in Figure [12] where $N$ is an integer and $N \geq 3$. Each intermediate stage $j \in [2, N - 1]$ includes two biasing capacitors $C_b[(j-1)]$, $C_b[(j-1)+1]$ and two rectifier diodes $D_{2j-1}$, $D_{2j}$. The fly-back diode $D_{2N+1}$ is connected between the storage capacitor $C_s$ of the final stage and the variable capacitor $C_1$. $D_{2N+1}$ plays exactly the same role as $D_5$ does in Figure [2].

![Fig. 12. Multi-stage voltage doubler circuit - Configuration (I).](image)

![Fig. 13. Operation of multi-stage voltage doubler circuit: stage II and IV.](image)

Despite of complex dynamics of the voltage multiplier configuration, we can also simplify and divide its operation over one cycle into four sequence stages that are similar to the Section III. Since all diodes $D_i (i \in [1, 2N + 1])$ are blocked in the first and the third stages, we consider two main topologies regarding directions of the parallel currents across diodes and capacitors. Both are represented in Figure [13]. Though diode $D_{2N+1}$ is required for initially charging $C_1$, its conduction is insignificant during operation of the harvesting system, and therefore is disregarded. In the first topology, only $D_{2j-1}$ ($j \in [1, N]$) are conducting. Charges are pumped from capacitor $C_1$ and $C_b[(k-1)-1]$ into $C_2$ and $C_b[(2k-1)]$ ($k \in [2, N]$) respectively. This stage stops when...
the proof mass displacement reaches the maximum value \( x = X_{\text{max}} \). The second topology corresponds to discharge of \( C_2 \) and \( C_{b_2[k(k-1)]} \) into \( C_{b_2(k-1)[k-1]} \) and \( C_s \) due to conduction of diodes \( D_{2j} \). When \( x = -X_{\text{max}} \), all \( D_i \) are blocked again and a new cycle starts. Observing that the currents flow in parallel branches in the conducting regime and the doubler stages are connected in series, such a voltage multiplier configuration can be classified as a parallel-series charge-pump or parallel-series switched/diode-capacitor network.

Based on the dynamic simulation, the operation of capacitor \( C_1(x) \) can be approximated by a Q-V cycle depicted in Figure 14. In the left and the right sides, the Q-V diagram is bounded by the lines corresponding to maximum and minimum values of the variable capacitance: \( Q_t = C_{\text{max}}V \) and \( Q_R = C_{\text{min}}V \).

The area of each parallelogram is roughly equal to the harvested energy per cycle \([31]\), and is modified over cycles in a complicated manner. It is very small at the beginning and gradually increases in the conversion regime. When the output voltage across the storage capacitor \( C_s \) approaches the saturation voltage \( V_{\text{out}} \approx V_{\text{sat}} \), the shape of the Q-V cycle becomes thinner. At \( n \to \infty \), it degenerates to the line, meaning that the mechanical energy is no longer captured. Here, \( n \) is the number of cycles. The similarity was observed from the Q-V cycle represented for the charge-pump circuit with resistive fly-back \([32], [33]\).

Figure 15 shows the saturation voltage of the circuit versus the input accelerations for various number of stages \( N \). Considering the two-stage voltage doubler \( N = 2 \), there is a rapid increase of the saturation voltage corresponding to increase of \( A \in [0.15 \text{g}, 0.30 \text{g}] \). However, higher acceleration amplitudes result in very slight rise of \( V_{\text{sat}} \). Similar behaviors are also observed for \( N \geq 3 \). To understand the reason for this phenomenon, we consider the relation between the work done against both electrostatic and impact forces and the energy lost in mechanical damping per cycle, which is characterized by the ratio

\[
L_{ct} = \frac{\int_0^T [F_e(t) + F_s(t)] \dot{x}(t) \, dt}{\int_0^T B(t) \dot{x}(t)^2 \, dt}
\]

where the electrostatic force \( F_e(t) \), the impact force \( F_s(t) \), the time-dependent damping \( B(t) \) and the proof mass velocity \( \dot{x}(t) \) are extracted from simulations at steady state. The variation of \( L_{ct} \) versus acceleration amplitude for \( N = 2 \) and \( N = 3 \) are depicted in Figure 16 as examples. Sufficiently high accelerations (i.e., \( A > 0.3 \text{g} \) with \( N = 2 \) and \( A > 1.0 \text{g} \) with \( N = 3 \)) result in collisions between the proof mass and the end-stops even at steady state. The coincidence between the figure 15 and 16 shows that the energy losses due to impacts make the saturation voltage increase very little with \( A \).

In addition, there is a range of input excitation that N-stage multiplier circuit with \( N \geq 3 \) performs worse than the case of \( N = 2 \). For instance, the 3-stage voltage multiplier only gives more benefit on the saturation voltage than the 2-stage configuration when \( A \) is equal or greater than a certain value called critical acceleration, in detail \( A \geq A_{cr} = 0.94 \text{g} \). It is also observed that \( A_{cr} \) decreases with increase of \( N \), e.g. \( A_{cr} \approx 0.84 \text{g} \) with \( N = 7 \). All those behaviors are due to effect of the strong nonlinear electrostatic force.
One important criteria to evaluate and highlight the performance of the voltage multiplier is its capability to work with micro-scale energy harvesters or low power systems. The minimum value of the capacitance ratio \( \eta_{\text{min}} \) for different \( N \) is given in Figure 7 with input acceleration \( A = 0.5 \) g. In the ideal case, the prerequisite condition for operation of the circuit is that \( \eta \) must be greater than the threshold \( \eta^* = \frac{N+1}{N} \) [34]. It is interesting to note that \( \eta^* \) and \( \eta_{\text{min}} \) can be decreased by increasing \( N \). When the electrical losses are taken into account, \( \eta_{\text{min}} \) is slightly higher than \( \eta^* \). Even so, the presented configuration is a promising solution to overcome the challenging obstacle of MEMS devices which typically have \( \eta < 2 \) due to the limitation of device size, microfabrication process and presence of parasitic capacitance.

Based on the analyses above, it can be concluded that with the use of the anti-phase gap-closing devices, 2-stage voltage multiplier is a better option for transducers with higher ratio \( \eta \) operating at low input acceleration amplitudes while 3- or more-stage ones are prefer in the opposite cases.

V. COMPARISON OF DIFFERENT TOPOLOGIES OF THE VOLTAGE MULTIPLIER

Due to mentioned problems, there are only a few circuits for which successful realizations, at least in theory, have been reported so far. A topology proposed by Lefeuvre et al. [13] was given that the minimum necessary ratio \( \eta \) for its operation can be lower than 2. The argument is based on theoretical analysis of the rectangular Q-V cycle alone, there are no concrete evidences in both dynamic simulations and measurements. Instead, the experimental validations were carried out using a single rotating variable capacitor driven by a DC motor, with nearly \( C_{\text{max}} = 45 \) pF and \( C_{\text{min}} = 155 \) pF. From the same group, a similar contribution was made in [18], where \( C_{\text{min}} = 25 \) pF and \( C_{\text{max}} = 125 \) pF. It is clearly that the ratio \( C_{\text{max}}/C_{\text{min}} \) in both cases is much larger than 2. In the same manner, the work of Karami et al. [19] presented a series-parallel charge-pump conditioning circuits which are generalized from the Bennet’s doubler. However, this contribution is limited to an electrical domain study only. One may concern about the effect of the electromechanical coupling on the full dynamics of the energy harvesters.

In this paper, we choose to compare our voltage multiplier configuration with the one in [13]. The series-parallel voltage doubler [19] is explored and discussed afterward, due to some limitations that are revealed by our simulation results.

Besides the circuit shown in Figure 12, an anti-phase structure may provide us another configuration where each transducer produces a single output voltage, see Figure 18. The insignificant anti-phase AC signals referred as ripple voltages are neglected. The two output voltages can be considered equal \( V_1 = V_2 \), which is the symmetric characteristics of the circuit. Similarly, we can divide the circuit configurations proposed by Lefeuvre et al. into two varieties that are depicted in Figure 19. Each cell \( 2 \leq N \) is an adaptation of the Greinacher voltage doubler. In configuration (IV) we also get \( V'_1 = V'_2 \). For a fairly comparison, we classify four different configurations into two group: (I)/(III) and (II)/(IV), as each group shares the same number of electrical outputs.

Figure 20 and 21 shows the evolution of output voltage for
configuration (I)/(III) and (II)/(IV) respectively, with the input acceleration $A = 1.5 \text{ g}$, drive frequency $f = f_0$, initial bias $V_0 = 8 \text{ V}$ and the number of stage $N = 3$. It should be noted that $\eta = 1.55$ is not enough for efficient operation of both configurations (II) and (IV) with $N = 2$. The end-time of simulations are $t_{\text{end}}^{(I)} = 2.8$, $t_{\text{end}}^{(II)} = 65$, $t_{\text{end}}^{(III)} = 1.3$, $t_{\text{end}}^{(IV)} = 4$ seconds. A major disadvantage of the configuration (II) over the others is its long start-up time, which however can be shortened by carefully choosing the biasing/storage capacitor and increasing $V_0$. For example, the start-up time of the configuration (II) reduces from 30.6 s with $V_0 = 8 \text{ V}$ and $C_b = 0.5 \text{ nF}$ to 7.4 s with $V_0 = 9 \text{ V}$ and $C_b = 0.2 \text{ nF}$. We see that the output voltage of configuration (I) saturates at much higher value than that of configuration (III). The same phenomenon is observed when configuration (II) is compared to configuration (IV).

These above simulations are extended for various stage number $N$ with different input acceleration amplitudes. The saturation voltage results are presented in Figure 22 and 23. In both cases, the introduced topology shows the superiority in comparison with previous work by Lefeuvre et al. Not only that, the remarkable gap of saturation voltage between the two topologies also raises with increase of $N$. The number of stage has a strong influence on the saturation voltage of the circuits. For configurations (III) and (IV), $V_{\text{sat}}$ decreases as $N$ increases due to parasitic effect of the constituent capacitor of each stage and power losses in diodes. Though the configuration (I) can overcome this challenge, the voltage gain is less than linear as more stages are introduced. The behavior of the configuration (II) is a bit more complicated, however, the voltage changes are small in general.

The difference in performance between the configurations (I) and (III) can be explained by their physical mechanisms. For configurations (I), each stage is a modified voltage doubler, it also acts as an intermediate charge reservoir. An amount of energy stored in stage $j - \text{th}$ is transferred into stage $(j+1) - \text{th}$ in the next operation cycle, which keeps going until it reaches and then is stored in $C_s$. Meanwhile, only a small amount of charge is transferred from $C_s$ into $C_1$, making the voltage across $C_1$ to be built up very slowly. Considering configuration (III), in contrary, the harvested energy is pumped from $C_1$ to $C_2$ through the intermediate capacitor $C_3$ alone. However, both $C_1$ and $C_2$ are charged by a built-in voltage multiplier circuit that may include up to $N$ cells. This process causes the voltages across the two variable capacitors to increase too fast, leading to rapid rise of the electrostatic force and decrease of the proof mass displacement as a consequence. Hence, the output voltage saturates at a lower level. That is also the reason why configuration (I) tend to have longer start-up time than configuration (III). Similar behaviors can be correspondingly inferred for the other configurations (II) and (IV).

The minimum required values of $\eta$ and $V_0$ for four configurations are compared in pairs in Table II. Since the differences between them are not so significant, advantages
of the proposed topologies are not overshadowed.

![Series-parallel charge-pump circuit](image)

Fig. 24. Series-parallel charge-pump circuit with $N = 2$, by Karami et al. [19].

![Evolution of output voltage](image)

Fig. 25. Evolution of the output voltage for different values of the initial bias $V_0$ ranging from 3 to 10 V.

The topology reported by Karami et al. is shown in Figure 24 for $N = 2$, adapted from [19]. The same switch-capacitor configuration can be found in [35]. Simulation results show that the circuit cannot operate with $\eta = 1.55$. Instead, the minimum required ratio of the capacitance variation is much higher than that, $\eta_{\text{min}} = 2.1$. Unlike other voltage multiplier circuits, the saturation voltage here strongly depends on the initial bias, but the voltage gain $V_{\text{sat}}/V_0$ is very small, e.g., $V_{\text{sat}} \approx 22$ V when $V_0 = 20$ V. Moreover, $V_{\text{sat}}/V_0 > 1$ only if $V_0 > 6$ V.

The saturation voltage could be significantly improved when the device with high ratio of $\eta = 2.61$ is used. The corresponding maximum displacement is now $X_{\text{max}} = 11 \mu$m. The time evolution of the output voltage across the storage capacitor $C_s$ is presented in Figure 25 with various values of the initial bias $V_0$. Since higher $V_0$ results in higher $V_{\text{sat}}$, the investigation of the minimum pre-charge voltage is irrelevant in this case. Such a phenomenon has not been revealed in [19] since only electrical domain was investigated. These results confirm the essential role of the electromechanical coupling on the circuit performance, which cannot be ignored in studying the system dynamics.

### VI. Conclusion

This paper presents a new configuration of a voltage multiplier for MEMS electrostatic energy harvesters. The anti-phase gap-closing transducers were modeled and utilized in the study. Without switches and inductive elements, the circuit proved to be suitable for ultra-low power implementation. Effect of the component imperfections such as parasitic capacitance of the transducer and diode non-idealities on the system performance are taken into account. The influence of biasing capacitances on start-up time and the dependence of the ripple voltage on the storage capacitor were explored. The analyses shown that the saturation voltage depends on both the nonlinearities of the electrostatic force and the impact force at high acceleration amplitudes. In comparing to previously reported circuits that are also based on the voltage doubler, the alternative topology presented in this paper can operate with a ratio of capacitance $\eta$ lower than 2. The minimum value of $\eta$ can be reduced by increasing the number of doubler stages $N$. The introduced configuration has shown the superiority on the saturation voltage compared to earlier work published in the literature.

With the assessment that the electrostatic force of the in-plane overlap-varying harvester is proportional to the proof mass displacement (i.e., which is very different from the anti-phase gap-closing devices), performance of such a transducer structure when configured as N-stage voltage multiplier is interesting for further investigation.

### Acknowledgment

Financial support from the Research Council of Norway through Grant no. 229716/E20 is gratefully acknowledged.

### References

[1] S. Roundy and P. K. Wright, “A piezoelectric vibration based generator for wireless electronics,” Smart Materials and Structures, vol. 13, no. 5, pp. 1131–1142, 2004.

[2] P. Mitcheson, “Energy harvesting for human wearable and implantable bio-sensors,” in IEEE EMBC, pp. 3432–3436, 2010.

[3] G. Ottman, H. Hofmann, and G. Lesieutre, “Optimized piezoelectric energy harvesting circuit using step-down converter in discontinuous conduction mode,” IEEE Transactions on Power Electronics, vol. 18, no. 2, pp. 696–703, 2003.

[4] X. Cao, W.-J. Chiang, Y.-C. King, and Y.-K. Lee, “Electromagnetic energy harvesting circuit with feedforward and feedback dc-directed pwm boost converter for vibration power generator system,” IEEE Transactions on Power Electronics, vol. 22, no. 2, pp. 679–685, 2007.

[5] P. D. Mitcheson, T. C. Green, and E. M. Yeatman, “Power processing circuits for electromagnetic, electrostatic and piezoelectric inertial energy scavengers,” Microm system Technologies, vol. -, pp. -, 2007.

[6] X. Zuo, Lei, “Circuit optimization and vibration analysis of electromagnetic energy harvesting systems,” in ASME 2009 International Design Engineering Technical Conferences and Computers and Information in Engineering Conference - San Diego, California, USA (August 30-September 2, 2009), 2009.

[7] R. D’hulst, T. Sterken, R. Paers, G. Deconinck, and J. Driessen, “Power processing circuits for piezoelectric vibration-based energy harvesters,” IEEE Transactions on Industrial Electronics, vol. 57, pp. 4170–4177, dec. 2010.

### Table II

| Configuration | (I) | (III) | (II) | (IV) |
|---------------|-----|-------|------|------|
| $\eta_{\text{min}}$ | $1.55$ | $1.44$ | $1.68$ | $1.62$ |
| $V_{0\text{min}}$ | $6.0$ | $4.5$ | $10.0$ | $10.0$ |

Comparision of minimum required $\eta$ and $V_0$ between four configurations with $N = 2$.
B. C. Yen and J. H. Lang, “A variable-capacitance vibration-to-electric energy harvester,” IEEE Transactions on Circuits and Systems—Part I: Regular Papers, vol. 53, pp. 288–295, Feb. 2006.

A. Dudka, P. Basset, F. Cottone, E. Blokhina, and D. Galayko, “Wide-band electrostatic vibration energy harvester (e-veh) having a low start-up voltage employing a high-voltage integrated interface,” Journal of Micromechanics and Microengineering, vol. 476, no. 1, p. 012127, 2013.

T. N. Phan, M. Azadmehr, C. P. Le, and E. Halvorsen, “Low power electronic interface for electrostatic energy harvesters,” Journal of Physics: Conference Series, vol. 660, no. 1, p. 012087, 2015.

A. C. M. de Queiroz and M. Domingues, “Electrostatic energy harvesting using doublers of electricity,” in Circuits and Systems (MWSCAS), 2011 IEEE 34th International Midwest Symposium on, pp. 1–4, Aug 2011.

A. C. M. de Queiroz and M. Domingues, “Analysis of the doubler of electricity considering a resistive load,” in Circuits and Systems (MWSCAS), 2013 IEEE 56th International Midwest Symposium on, pp. 45–48, Aug 2013.

E. Lefeuvre, S. Risquez, J. Wei, M. Woytasik, and F. Parrain, “Self-biased inductor-less interface circuit for electret-free electrostatic energy harvesters,” Journal of Physics: Conference Series, vol. 557, no. 1, p. 012052, 2014.

J. Wei, S. Risquez, H. Mathias, E. Lefeuvre, and F. Costa, “Simple and efficient interface circuit for vibration electrostatic energy harvesters,” in 2015 IEEE EESENS, pp. 1–4, Nov 2015.

W. Hauschild and E. Lenk, High-Voltage Test and Measuring Techniques. Springer-Verlag Berlin Heidelberg, 1 ed., 2014.

R. Dayal, S. Dwari, and L. Paria, “Design and implementation of a direct AC-DC boost converter for low-voltage energy harvesting,” IEEE Transactions on Industrial Electronics, vol. 58, pp. 2387–2396, June 2011.

A. C. M. de Queiroz and M. Domingues, “The doubler of electricity used as battery charger,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 58, pp. 797–801, Dec 2011.

J. Wei, E. Lefeuvre, H. Mathias, and F. Costa, “Electrostatic energy harvesting circuit with dc-dc converter for vibration power generation system,” Journal of Physics: Conference Series, vol. 773, no. 1, p. 012045, 2016.

A. Karami, D. Galayko, and P. Basset, “Series-parallel charge pump conditioning circuits for electrostatic kinetic energy harvesting,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, pp. 227–240, Jan 2017.

Y. Sun, S. N. Fry, D. P. Potasek, D. J. Bell, and B. J. Nelson, “Characterizing fruit fly flight behavior using a microforce sensor with a new comb-drive configuration,” Journal of Microelectromechanical Systems, vol. 14, pp. 4–11, Feb 2005.

K. Kim, X. Liu, Y. Zhang, and Y. Sun, “NonNewton force-controlled manipulation of biological cells using a monolithic microgripper with two-axis force feedback,” Journal of Micromechanics and Microengineering, vol. 18, no. 5, p. 055013, 2008.

S. Kaur, E. Halvorsen, O. Srsen, and E. M. Yeatman, “Characterization and modeling of nonlinearity in in-plane gap closing electrostatic energy harvester,” Journal of Microelectromechanical Systems, vol. 24, pp. 2071–2082, Dec 2015.

B. D. Truong, C. P. Le, and E. Halvorsen, “Experimentally verified model of electrostatic energy harvester with internal impacts,” in 2015 28th IEEE International Conference on Micro Electro Mechanical Systems (MEMS), pp. 1125–1128, Jan 2015.

L.-C. J. Blystad, E. Halvorsen, and S. Husa, “Piezoelectric MEMS energy harvesting systems driven by harmonic and random vibrations,” IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 57, pp. 908–919, April 2010.

M. Bao and H. Yang, “Squeeze film air damping in MEMS,” Sensors and Actuators A: Physical, vol. 136, no. 1, pp. 3–27, 2007. 25th Anniversary of Sensors and Actuators A: Physical.

C. P. Le and E. Halvorsen, “Mems electrostatic energy harvesters with end-stop effects,” Journal of Micromechanics and Microengineering, vol. 22, no. 7, p. 074013, 2012.

D. S. Nguyen, E. Halvorsen, G. U. Jensen, and A. Vogl, “Fabrication and characterization of a wideband mems energy harvester utilizing nonlinear springs,” Journal of Micromechanics and Microengineering, vol. 20, no. 12, p. 125009, 2010.

N. Semiconductors, “BAS716 Spice model,” Documentation, 2012. https://assets.nexperia.com/documents/ datapages/model/BAS716.pdf.

B. D. Truong, C. P. Le, and E. Halvorsen, “Theoretical analysis of electrostatic energy harvester configured as Bennet’s doubler based on Q-V cycles,” arXiv:submit/2016218, 25 Sep 2017.

Binh Duc Truong received the B.E. degree in Mechatronics from the Ho Chi Minh City University of Technology, Vietnam, in 2012 and the M.Sc. degree in Micro- and Nano System Technology from the Bilkent and Vestfold University College, Norway, in 2015. He is currently pursuing the Ph.D. degree with Department of Microsystems, University College of Southeast Norway, focusing on MEMS electrostatic energy harvesters and wireless power transfer systems.

Cuong Phu Le Cuong Phu Le received the B.S. degree in telecommunications engineering from the University of Technology, Ho Chi Minh City, Vietnam, in 2005, the M.S. degree in microsystem technology from Vestfold University College in Horten, Norway in 2009 and the Ph.D. degree in microsystems technology from University of Oslo, Norway in 2013. He is currently a research scientist in Department of Microsystems, University College of Southeast Norway in Horten. His current research interests include microsystem design, modelling and MEMS vibration energy harvesting.

Einar Halvorsen (M’03) received the Siv. Ing. degree in physical electronics from the Norwegian Institute of Technology (NTH), Trondheim, Norway, in 1991, and the Dr. Ing. degree in physics from the Norwegian University of Science and Technology (NTNU, formerly NTH), Trondheim, Norway, in 1996. He has worked both in academia and the microelectronics industry. Since 2004, he has been with University College of Southeast Norway in Horten, Norway, where he is a professor of micro- and nanotechnology. His current main research interest is modelling of microelectromechanical devices.