Extended flag gadgets for low-overhead circuit verification

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Flag verification techniques are useful in quantum error correction for detecting critical faults. Here we present an application of flag verification techniques to improving post-selected performance of near-term algorithms. We extend the definition of what constitutes a flag by creating error-detection gadgets based on known transformations of unitary operators. In the case of Clifford or near-Clifford circuits, these unitary operators can be chosen to be controlled Pauli gates, leading to gadgets which require only a small number of additional Clifford gates. We show that such flags can improve circuit fidelities by up to a factor of 2 after post selection, and demonstrate their effectiveness over error models featuring single-qubit depolarizing noise, crosstalk, and two-qubit coherent overrotation.

\section{I. INTRODUCTION}

In current quantum computers, qubit and gate counts are both at a premium due to system size and gate error limitations. Algorithms which will be productive in this regime cannot require fault-tolerant quantum computation, as even the smallest quantum error correcting proposals require seven to fifteen physical qubits per logical qubit, once fault-tolerant syndrome extraction is taken into account [1–5]. An obvious question is whether there are lower overhead solutions which might help for these algorithms, such as the sampling problems which many expect to be the first promising quantum applications [6–9]. Some low overhead error mitigation techniques have been considered, like error extrapolation [10, 11], random compiling [10, 12, 13], and coherent cancellation [14, 15].

We propose an additional technique, which is an extension of the flag qubit framework [3, 4, 17–19]. Flag qubits have been employed in the field of quantum error correction to catch critical faults which damage the distance of the code [20–24]. In these cases the flag consists of a small entangle-evolve-disentangle-measure gadget in which the gates that make up the flag commute with the circuit being flagged. In our construction, the flag does not necessarily commute with the circuit but instead has a known propagation through the circuit. We build our flags around verifying that this evolution has occurred correctly. If such a check fails, we know that the circuit application has had an error and it should be discarded. In this way we are able to postselect on these flag outcomes and improve our confidence in the samples we accept. Through this we may be able to reduce the number of experimental runs needed to yield high accuracy results. Our methods supplement existing work on circuits that detect mid-circuit failures through quantum run-time assertions [25].

This paper will be organized as follows: In Section I we introduced the problem, in Section II we explain the general scheme to extend flag gadgets to larger classes of circuits, in Section III we discuss the performance of our flags in simulation against a spectrum of error models, and in Section IV we conclude.

\section{II. EXTENDING FLAGS TO VERIFICATION OF CIRCUITS}

In syndrome extraction circuits, there are often specific fault locations which can propagate dangerously to the data. Flag gadgets verify that these specific faults have not occurred. In the case the fault does occur, the flag gives the decoder enough information to correctly identify and correct the error. A standard flag gadget is shown in Fig. 1. In this case, the critical error being caught is an error after the second CNOT gate in the stabilizer measurement. If an X-type error on the ancilla occurs after this gate, it would propagate to two errors on the data. Depending on the code being implemented, this might lead to a distance drop. When the flag is implemented, it can detect that this error may have occurred. The stabilizers can then be remeasured and, using this additional piece of information, the code can catch these possible correlated errors. In the standard setup, the entangling and disentangling operators are identical and commute with the circuit.
Our main contribution is extending this framework to the case where the entangling operation does not commute with the circuit (Fig. 2a). Given an n-qubit operator $F$ and an n-qubit unitary $U$, we construct flag gadgets using a $|+\rangle$ state, a controlled-$F$ operator, and a controlled-$F'$ where

$$F' = UF^\dagger U^\dagger. \tag{1}$$

An error in $U$ that results in $F$ not propagating to $F'^\dagger$ will prevent perfect disentanglement and become a detectable error on the flag qubit when measured in the $X$ basis.

Whether postselection on this flag actually improves performance is determined by the number of errors detected by the flag relative to the number of errors added by the flag. Here we construct low-overhead flag gadgets that can verify large circuit sections. As a result, postselection can lead to significant reduction in error rates, increasing confidence in circuit executions which pass all tests.

A. Pauli flags for Clifford circuits

One way to limit the overhead cost of the flag gadget is to limit our entangling operator to a controlled Pauli operator, and the circuit to a Clifford circuit. Since Clifford operators map Pauli operators to other Pauli operators, the disentangling operator is guaranteed to also be a controlled Pauli operator. As a result we can be assured that our flag gadget is composed of at most $2n$ two-qubit gates, where $n$ is the number of qubits in the unflagged circuit (Fig. 2b).

While a quantum algorithm requires non-Clifford elements in order to be useful, one could imagine flagging sections of a larger circuit in order to catch errors in each section. In Section III B we present the performance of Clifford flags when applied to the circuit seen in Fig. 3.

![FIG. 2: Circuits demonstrating flags for multiple cases. In (a.) we show a general flag gadget for a general n-qubit unitary $U$. In (b.) we show that for a Clifford subcircuit (here shown surrounded by $T$-gates) this can be simplified to Pauli flags. In (c.) we show how Pauli flags can be used for a circuit with non-Clifford elements. Lastly in (d.) we show how multiple flags can be used to verify a single circuit.](image)

![FIG. 3: Circuit from [26] which is used to improve the fidelity of magic states. The Clifford block after the $T$-gate layer can be flagged by a Pauli flag following Fig. 2b. We do not consider the measurements at the end of the circuit in order to make our results more general. Flags accounting for these measurements could focus on catching only errors which flip the outcome, further optimizing performance.](image)

B. Pauli flags for circuits with low non-Clifford gate density

A circuit which has few non-Clifford elements can also be flagged with Pauli operators in some cases, however more care must be put into finding the appropriate Pauli operators. Specifically, in order to avoid having to consider Pauli propagation through non-Clifford gates, it would be ideal for the flags to never interact with these gates.

The goal is to find a Pauli operator $P$ such that, as it is propagated layer-by-layer through the circuit, it acts as an identity operator on all qubit lines that have a non-Clifford gate, as shown in Fig. 2a. In the figure, this class of entangling flags $P$ is constrained by the fact that as you propagate $P$ through to layer A, its action must commute with the non-Clifford gate on qubit 2, and on layer B, the propagated Pauli operator must commute with the non-Clifford gate on qubit 5. This could either
FIG. 4: A circuit for $Z^\theta Z^\theta Z^\theta Z^\theta Z^\theta\theta$ that has a single non-Clifford element. This circuit can still be flagged with Pauli operators by designing the flags to avoid or commute with the non-Clifford gate, as shown in Fig. 2.

mean that the Pauli operator on those layers acts as identity on that qubit, or if the red gates are arbitrary angle Pauli rotations, the propagated Pauli operator must be along the same axis. Finding such flags will get more difficult as the density of non-Clifford gates increases, but for a circuit like the non-Clifford Pauli rotation circuit in Fig. 4 such a flag can be found easily by starting with a Pauli operator in the middle of the circuit that avoids the non-Clifford gate and propagating outwards in both directions. We show the value of flags of this type in Section III C.

C. Implementing multiple flags on one circuit

Since the flag leaves the circuit unchanged, multiple flags can be checked on the same circuit execution. The flags must be nested such that the order of entangling flags is reversed when checking the disentangling flags, as shown in Fig. 2h. As long as this condition is respected and each flag is compatible with the circuit, the logic will be unchanged. What we see in our simulations is that in the cases where the flags are doing well on their own, combining them seems to be productive. The data shown in the following section (Sec. iii) is representative of this behavior. In error models where the flags are not performing as well on their own, additional flagging does not generally seem to flip that behavior. When designing these flag pairs, it is beneficial to have the flags disagree on most qubits, so that they can catch a wider range of errors. Additionally, the penalty in terms of extra fault locations is somewhat alleviated for the inner flag since some of its faults will be caught by the outer flag.

D. Finding good flags

If these flags are to be useful for larger circuits and more general applications, it is imperative that we are able to predict which flags will be successful without full simulation. To that end, there are a few guidelines which lead to an effective flag:

- The circuit being flagged should have a high gate density, meaning many gates on relatively few qubits. Such circuits will have a large number of error locations which can be effectively flagged without adding significant overhead.

- If the algorithm ends with measurements, the final flag should match the basis of the measurement. For example if an algorithm ends with measurements on all qubits in the $Z$-basis, then having the final flag be a $Z$-type operator will detect the widest set of errors which flip the results of the measurement. This will also minimize the impact of gate error if the error model is one in which gate error is along the axis of the gate.

- If multiple flags are being used, they should be designed so each catches different errors on each qubit, to increase sensitivity to a variety of errors. This also allows for the gate errors from the inner flag to be caught by the outer flag in error models like those discussed in the previous point.

On top of this, it is useful to note that since these flags do not lead to schemes which possess a distance, the dominant term in the error polynomial will be the linear term. For a given error model, it is easy to find the effective error model at the output layer of the circuit by propagating single errors through the circuit from each fault location. By checking how many of these errors each flag detects, balanced against the number of extra error locations introduced by the flag, one can efficiently guess

FIG. 5: Data verifying that the metric in Eq. 2 effectively captures the performance of flags within the magic state distillation circuit in Fig. 3. The fidelities of the flagged circuits are shown in green, with the three flags with the highest values of $q(P, P')$ shown in dark green. The raw circuit is shown in black. The data shows that the three flags with the highest values of $q(P, P')$ were also the top three performers in terms of fidelity. This metric might not perform as well at higher error rates where the higher order terms in the polynomial are more important.
FIG. 6: The (a.) single-qubit depolarizing, (b.) single-qubit depolarizing with crosstalk, and (c.) overrotation error models we consider. Gray rectangles are the desired gates in the circuit, while colored rectangles are errors. In the first two models the errors are depolarizing errors, where in the crosstalk model nearest neighbors experience a $\frac{1}{10}$ × the gate failure rate. For the overrotation model, every gate is followed by a slight overrotation along the same axis by an amount $\epsilon$.

which flags in a set will be the highest performing. An example of this method is shown in Fig. 5 for the single-qubit depolarizing error model. We create a set of all possible Pauli errors on the output of the circuit from a single fault, and define a quality metric on a flag \( \{ P, P' \} \):

$$q(P, P') = N_{\text{detected}} - 6w(P) - 6w(P'), \tag{2}$$

where \( N_{\text{detected}} \) is the number of faults in the output error set that anticommute with \( P' \), and \( w(P) \) is the weight of a Pauli operator \( P \). The weights are multiplied by 6 since each two-qubit gate adds 6 possible faults to the system, 3 on the control and 3 on the target, under the error model described in Fig. 6. We calculated this metric and found that the flags which had the three largest values of \( q(P, P') \) also performed the best in terms of fidelity. This supports the effectiveness of this quality metric in Eq. 2 and calculating this metric is polynomial in the number of gates in the circuit.

III. RESULTS

All results in this section are acquired by density matrix simulations written using Cirq [27]. Final fidelities are exact values calculated using entanglement fidelity before any measurements in the initial circuit. Data is shown for 500 Pauli flags that were randomly generated for each circuit. It should be noted that this is a computationally efficient procedure [28]. The data for multiple flag systems are created using 100 pairs of randomly generated flags.

A. Error Models

In this work we consider a set of three error models, shown in Fig. 6, which are pulled from the spectrum of errors seen in physical systems today.

Firstly, we consider a single-qubit depolarizing model where single-qubit depolarizing errors follow all two-qubit gates. This model has been previously looked at by the Google team in [29]. Secondly, we consider a simplified crosstalk model which takes this single-qubit depolarizing model and adds weak depolarizing noise to the qubits adjacent to any two-qubit gate. Lastly, we consider a coherent overrotation error model based on ion trap quantum computers. These errors have also been studied in previous works [5, 15], and the data presented for them are for circuits compiled down to ion trap gates [30]. Through this set of models we show that our techniques succeed against a wide variety of errors seen in physical hardware.

B. Clifford Example: Magic State Distillation

In Fig. 7 we show the performance of 500 randomly generated flags on the circuit in Fig. 3. As this circuit is densely populated with gates, a majority of the flags succeed in improving the performance of the circuit. The depolarizing and crosstalk models are much easier to flag, as they give off discrete errors which can be caught by the flags. The coherent gate error model is more damaging in general, and also can easily create error patterns where multiple errors anticommute with the flag at the same time. Since the flag will only detect an error when an odd number of errors anticommute with it, there will still be unitary errors on the system after measurement. Additionally any coherent error model can have overrotations which combine coherently, so the gate error may constructively interfere with our flags themselves.

The wider spread on the coherent case is because that error model creates the most structured error model on the output. The depolarizing and crosstalk channels will have some asymmetry on the output errors, due to the
a. Distillation  

b. ZZZZZ  
c. Distillation - Two Flags

FIG. 7: Data for flagging the (a.) magic state distillation circuit in Fig. 3, the (b.) ZZZZZ(θ) circuit in Fig. 4, and the (c.) magic state distillation circuit with two flag gadgets. The data for each error model is colored to match Fig. 6, where the best performing flag has both its fidelity (solid line) and survival probability (dashed line) shown darker, and is labeled within the figure by its disentangling operator. Raw circuit fidelities are shown in black. Due to being higher in gate density, the magic state distillation circuit is more appropriate for flagging. Similarly, the multiple flag solutions work better in the single-qubit depolarizing and crosstalk error models, which lend themselves better to flagging as well.

Fact that errors can only propagate in certain ways. However in the coherent overrotation case, the asymmetry on the gate errors themselves also carries over directly to the output. As a result, flags have a wider spread under this error model, in both positive and negative contributions. Due to the extremely structured error model, systems that exhibit overrotation errors would be able to strongly benefit from flags that are specifically designed to take advantage of this error asymmetry.

C. Non-Clifford Example: Arbitrary Angle Pauli Rotations

In Fig. 4b we present data from 500 flags on the ZZZZZ(θ) circuit in Fig. 4. This circuit is significantly less dense than the magic state distillation circuit in Fig. 3 and as a result the flags do not perform as well on average. This is especially true in the case of the coherent overrotation model, as this circuit’s structure propagates errors in damaging ways. If a circuit would require consecutive multi-qubit Pauli rotations, the product of all of them could be flagged instead. This would lead to a better tradeoff between error locations added and subtracted from the system, at the expense of missing some error patterns which would be caught by a scheme which flagged each rotation individually.
D. Multiple Flag Results

In Fig. 7c we show how pairs of Pauli flags can perform on the magic state distillation circuit in Fig. 3. The pairs of flags behave as one would expect, in cases where the initial flags were performing well, they improve things further. Specifically, in the single-flag simulations for the depolarizing and crosstalk models, there was a good number of flags which performed worse than the unflagged case. In the two-flag case, these two error models almost always saw improvements over the raw circuit. In the overrotation error model the main impact was an increased spread in the outcomes for different flags. This is due to the fact that a coherent error model can see significantly worsened performance when the gate errors from the flag coherently add with the gate errors from the circuit, as opposed to a depolarizing case where a poorly chosen flag adds the same amount of error as a well chosen one, but simply detects fewer errors.

IV. CONCLUSION

In this work we have presented a method for applying flag verification techniques to error detection in Clifford and near-Clifford circuits. These flags can be efficiently computed and ranked, meaning that even circuits that are outside of the range of full simulation can be protected. The flagged circuits show improvements in performance when postselected for flag success, even in cases where there are relatively few gates. Additionally, the survival probabilities for these techniques are high enough relative to the performance boosts they provide such that postselecting on them should improve performance in sampling problems. There is also a potential value in investing resources into finding optimal flags for common Clifford subroutines which occur often within algorithms.

Recent work on understanding the Clifford hierarchy may offer interesting non-Clifford operators that possess guarantees on the existence of commuting Pauli operators [31]. In situations where there exist known propagations for certain operators through a relevant non-Clifford block, flags of the type shown in this paper should provide similar improvements. Through these techniques, this idea could be extended beyond Clifford and near-Clifford circuits. These techniques may be invaluable in near-term experiments where the overhead costs of more effective error correction techniques are prohibitive.

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