Programmable Switch as a Parallel Computing Device

Li Chen
lchenad@ust.hk
Ge Chen
gchenaj@connect.ust.hk
Justinas Lingys
jlingys@connect.ust.hk
Kai Chen
SING Group
CSE,HKUST
kaichen@cse.ust.hk

ABSTRACT
Modern switches have packet processing capacity of up to multi-tera bits per second, and they are also becoming more and more programmable. We seek to understand whether the programmability can translate packet processing capacity to computational power for parallel computing applications. In this paper, we first develop a simple mathematical model to understand the costs and overheads of data plane computation. Then we validate the the performance benefits of offloading computation to network. Using experiments on real data center network, we find that offloading computation to the data plane results in up to $20\times$ speed-up for a simple Map-Reduce application. Motivated by this, we propose a parallel programming framework, p4mr, to help users efficiently program multiple switches. We successfully build and test a prototype of p4mr on a simulated testbed.

1. INTRODUCTION
The undeniable trend in datacenter networks (DCN) is that the switches in the data plane are becoming more and more programmable [1, 2, 3, 4]. With recent advances in switch architecture [2], novel hardware component design [5], and programming language support [2, 6], user-defined functions have been shown to perform on programmable switches at line rate of 10/40Gbps.

With programmable switch, many applications have been proposed (switch-based key-value store [7], transport layer load balancing [8], in-band telemetry [9], consensus algorithm [10], etc.). Among all these applications, one of the guiding principle is to minimize the per-packet computation done on the switches. This minimal computation principle (MCP) serves to reduce per-packet latency and overhead on the switches, to lower memory footprint, and to increase throughput.

The merits of MCP is easily recognized, and we concede that this principle should be followed in general for data plane applications. However, we cannot ignore the fact that the packet processing power is up to 6.5Tbps [11] for modern programmable switches. Tempted by such raw computational potential, in this paper, we aim to explore the opposite of MCP: we try to understand whether programmable switches can be used as a parallel computing device. Our insight is drawn from the success of using GPU to offload massively parallel tasks from CPU. We envision that (some) parallel computing tasks can be offloaded to the network from the servers. In other words, while the data is being transmitted in the network, we program the switches to perform some computation on the data, so that when the data reaches the destination, they are already processed.

To this end, the following questions must be answered.

• What are the primitive computations that can be supported by programmable switches?
• What is the performance penalty of doing computing tasks on programmable switches?
• What are benefits of doing computing tasks on programmable switches?
• How to program a network of switches to perform computing tasks?

In this paper, we describe our initial efforts to allow programmable switches to support data plane computation, and provide some preliminary answers to the above questions. In particular, we use the Word-Count application as a running example. First we describe the primitive functions (written in P4) that can be implemented with one programmable switch, and show that a network of programmable switches with different primitive functions can work together to complete the Word-Count application (§2). Then, we develop a mathematical model to understand the performance penalty of offloading computation to the network (§3). We also use experiments to demonstrate the performance benefits of doing data plane computations (§4). Finally, we propose a parallel programming framework, p4mr, that facilitates programming a network of programmable switches (§5).

2. OFFLOADING WORD-COUNT TO DATA PLANE
In this section, we use the well-known Word-Count applications to introduce computation in data plane.

In a conventional Map-Reduce framework (Hadoop [12], Spark [13], etc.), Word-Count runs as follows on multiple servers. Text files (or word lists) are located on different servers, and Map tasks are assigned to these servers. Map
Figure 1: Example: Word-Count

tasks maps each word ("alice", "bob", etc.) in the text file to tuples (<"alice", 1>, <"bob",1>, etc.). These tuples are send from the mappers (servers running Map task) to the reducers (servers running Reduce tasks) based on their hash values. For the Reduce task, it accumulates the total appearance of words (<"alice", 5>, <"bob",1>, etc.). Each reducer is responsible for a subset of all the possible words. The final result of Word-Count is then the combination of all the results from all the reducers.

Due to the simplicity of Word-Count, we use it as an example of data plane computation. Suppose the data set of word lists are distributed among a set of servers. Performing Word-Count using a network of programmable switches is very similar to that in a Map-Reduce framework. Servers serialize their own word lists into stream of packets, and send them to mappers. The mapper is running on programmable switch. It processed each word, and forwards the word to a corresponding reducer based on the hash value of the word. The reducers are also running on a programmable switch, and it accumulates the count for each word. After a word is counted, it is discarded at the reducer.

However, we emphasize that there are some key differences from conventional Map-Reduce frameworks: Firstly, In the data plane, the smallest unit of computation is packet, and each packet should have a fixed format for the switch to process. Secondly, routing/forwarding based on matched field(s) is part of computation. Finally, to extract the final result, each server need to send a final packet after it has sent all the data packets, so as to trigger all the switches hosting the reducer to send to the destination hosts.

This example also reveals many unanswered design questions: 1) how should the servers serialize their data sets, or should serialization be also offloaded to the network? 2) should we do partial offload or full offload of Map and Reduce tasks to the network? 3) how to program multiple switches to perform the same job efficiently? In what follows, we attempt to provide some initial answers.

3. COST OF DATA PLANE COMPUTATION

In this section, we look at the overhead of doing computation in the data plane. In particular, we examine the overhead of serialization — the cost of transforming the data set into packets (each containing a single data item) that can be processed by the switch.

We make the following assumptions on the data set: 1) the data set contains multiple data items; 2) each data item is less than the MTU (maximum transmission unit [14]) size of the network; 3) each data entry have the same size.

The overhead of serialization mainly come from sending data packets. Given a data set, the servers can either 1) send each data item as an individual packet, or 2) send a MTU-sized packet packed with many data items.

Assume the server is sending MTU-size packets at rate \( r \)

\[ \text{Only an integral number of data items can be packed into one packet.} \]
the network in Scenario 2&3, we assume that it is processed at the maximum rate (for Scenario 3, we apply a rate-limiter at each server to enforce the throughput penalty).

For the experiment hardware settings, we use 24 servers with Intel E5-2630 CPU and 32GB memory. Each server has a NetXtreme BCM5719 Gigabit Ethernet Network interface card (NIC), and are all connected to a Gigabit Ethernet switch (Figure 3).

To test raw performance and avoid unnecessary software overheads, we choose not to use existing Java-based parallel computing frameworks [13, 15]. Instead, we implement a bare-bone Word-Count applications using C++. This application use the same mechanism as Map-Reduce to parallelize among multiple servers. In each server, we have a data set of a same size, one mapper, and one reducer; thus for \( n \) servers, we have \( n \) mappers and \( n \) reducers.

**Results.** We vary the total size of data set from 500MB, 1GB, to 5GB, and increase the number of servers from 3 to 24. The results are plotted in Figure 4&5. The metric we use is job completion time (JCT) speed-up against Scenario 1, which does not use data plane computation. For each experiment, if JCT of Scenario 1 is \( J_1 \), and \( J \) for another scenario, then the speed-up is calculated as \( J_1 / J \).

Figure 4 demonstrate the gain from offloading the Reduce task to the data plane, and we observe up to 5.32× speed-up. We can also see that, with larger data set, the gain is more obvious, because the larger data size requires more CPU computation for the Reduce task. Finally, with more servers added, the speed-up is decreasing. This is because the total data size is the same, and with more servers, the data size on each server is decreasing, resulting in less CPU processing on each server. As shown in Figure 6&7, the decrease in CPU processing time for Map and Reduce task corresponds to the decrease in speed-up.

For Figure 5, we can make the same observations. In addition, by comparing Figure 4&5, we can see the gain from offloading the Map task to the data plane. Even with the throughput penalty (the servers sent packets at a rate of \( C/e=1000Mbps/2.718=367.92Mbps \)), the speed-up of Scenario 3 is at least 4.61× higher than that of Scenario 2. We conclude that doing serialization of data items using CPU is much less efficient than offloading to the data plane.

In summary, we have shown with the above experiments that it is beneficial to offload some computation to the data plane.
5. **P4MR: PROGRAMMING MODEL FOR DATA PLANE COMPUTATION**

Although offloading computation to the data plane do have benefits, it is still difficult to program the multiple switches to carry out a computation task in cooperation. The users can handcraft the programs in each switch. In this section, we propose a parallel programming framework based on P4, p4mr.

### 5.1 High-Level Design

p4mr has three design goals: 1) p4mr should provide primitive functions that programmable switches can support; 2) p4mr should transparently parallelize user program onto multiple switches. With p4mr, users can accelerate their parallel computing application by offloading certain computations to the data plane.

As depicted in Figure 8, users compose their program using p4mr-provided primitives, and submit to a cluster-wide p4mr compiler. p4mr compiler maintains cluster information relevant to the compilation process, such as topological, routing, and memory constraints. The compilation process follows Figure 9: the user program is parsed into a direct acyclic graph of primitives. Given the constraints, the compiler attempts to place the primitives to the network of programmable switches. If the placement is successful, the compiler then adds appropriate routing for the packets containing data items. After placement and routing, P4 codelets for different switch in the network is generated and compiled to each switch.

### 5.2 Implementation

We have built and tested the primary model of p4mr system in the open source P4 simulator [?]. The simulator resides on a VMware virtual machine based on 64-bit Ubuntu 14.04 Distribution and operates with a base memory of 2GB. The whole system consists of a p4mr raw code compiler, a dependency graph parser and finally a Mininet [16] network simulator. In our simulation, we have mimic a simple workflow of Map-Reduce on three files locate on different places of the P4 Virtual Machine. Next, we are going to explain the detailed implementation of each component with this concrete example.

To start a p4mr workflow, users are required to write down their operations with some basic MapReduce operations to explicitly define the tasks. We provide a simple list of avail-
able operations, including *assignment*, *load*, *map*, *summation*. Take the following code snippet as an example:

```c
A := store < uint_64 >("ip_h1: path_A");
B := store < uint_64 >("ip_h2: path_B");
C := store < uint_64 >("ip_h3: path_C");
D := SUM(A, B);
E := SUM(C, D);
```

The first three lines of codes load data from different file paths to each variable label. The last two lines specify the *summation* operation on these data source. Due to the limited operations supported by P4 Lang, currently our simulator only support summation on 64-bit and 32-bit unsigned integers. After the raw codes are ready, our first component, a raw code compiler implemented with “flex & bison”, parses the codes and generate an abstract syntax tree (AST) under json format. The AST contains the detailed information of each label, such as the unique label index, function type, parameters and so on. Later, our dependency graph parser takes the AST as input and converts it into a directed acyclic graph (DAG). The directed acyclic graph of the previous code listing is shown in Figure 10.

From the dependency graph, we know that label *D* depends on *A* and *B* while label *E* depends on *D* and *C*. Based on these information, we are able to associate each label with one of our network P4 switches. The placement of labels on switches has a significant impact of the overall performance as it determines the routes to forward *p4mr* packets. The objective is to minimize the average number of hops that the whole workflow packets will encounter. As for our preliminary design, we apply a greedy algorithm to assign the minimum burdened switch to new labels. In our simulation, we evaluate the previous example in the topology of Figure 10 comprised of six hosts and six switches.

After the label placement, the first summation labelled *D* is assigned to switch S2 and *E* is associated with S6 since initially each switch has no assignments. Once the label association is done, the Mininet simulator in *p4mr* will generate a routing table and reconfigure each switch from S1 to S6 according to dependency graph. In our simulation, the three files are initially stored on hosts *h1*, *h2* and *h3* respectively. Also, we randomly assign one host *h6* as the results collection end-point, onto which we forward the final results to check correctness. All the intermediate results are updated in the stateful variables in P4 switch. Finally, when the *p4mr* process is launched, packet assembler scripts segment each data file and assemble each integer based on our pre-defined packet header format. The packet format in our simulation is shown in Figure 11.
As described in the packet header format, a preamble field of 64 bits is used to distinguish the P4MR traffic from others. Then, an 8-bit application id aims to separate different labels, collection signal or Map-Reduce functions. Next, an 8-bit routing id helps to route packets to dedicated switches. Another 8-bit collection id is set when the current packet is a collection signal and does not contain any valid data. Finally, a 64-bit field holds the data to update the results.

We have compiled and tested this prototype implementation using Mininet. The results show that this prototype is functionally correct. Since we do not have a switch that support P4, we leave performance evaluation on hardware switch as future work.

6. CONCLUSION

Motivated by the immense computational potential of modern programmable switches, we propose to offload some parallel computing tasks to the data plane, so that the data can be processed while in-transit. We first developed a simple mathematical model to understand the costs and overheads of data plane computation. Then we validate the performance benefits of offloading computation to network. We then described a parallel programming framework, p4mr, to help users efficiently program multiple switches. We built and tested a prototype of p4mr on a simulated testbed.

Future works: p4mr still have many aspects that need improvement and further investigation.

- **Memory footprint.** Operational memory is one of the most precious resource on the switch, and many computational applications have large memory footprint, e.g. Word-Count. Deploying such applications on switch may use up memory and negatively impact the functionality of the switch. It is therefore important to understand the general characteristic of memory usage for each primitive functions that p4mr offers to users, and to develop a predictive memory model to facilitate the compilation process.

- **Multi-job scheduling.** Users of parallel computing frameworks expect to run multiple applications at the same time. Given multiple applications, a scheduling mechanism for p4mr need to be explored.

- **Dynamic job arrivals.** Currently p4mr only support pre-defined user program before the network starts. When the simulated network is running, p4mr cannot change the functions on the switch. Supporting dynamically arriving jobs may require incremental compilation or virtualization mechanisms [17], which we intend to explore further.

7. REFERENCES

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