Design and Performance Analysis of Unified Reconfigurable Data Integrity Unit for Mobile Terminals

L. Thulasimani
Department of ECE
PSG College of Technology,
Coimbatore-641004, India

M. Madheswaran
Centre for Advanced Research, Dept. of ECE
Muthayammal Engineering College
Rasipuram-637408, India

Abstract—Security has become one of the major issues in mobile services. In the development of recent mobile devices like Software Defined Radio (SDR) secure method of software downloading is found necessary for reconfiguration. Hash functions are the important security primitives used for authentication and data integrity. In this paper, VLSI architecture for implementation of integrity unit in SDR is proposed. The proposed architecture is reconfigurable in the sense it operates in two different modes: SHA-192 and MD-5. Due to applied design technique the proposed architecture achieves multi-mode operation, which keeps the allocated area resource at minimized level. The proposed architecture also achieves high-speed performance with pipelined designed structure. Comparison with related hash function implementation have been done in terms of operating frequency, allocated-area and area-delay product. The proposed Integrity Unity can be integrated in security systems for implementation of network for wireless protocol, with special needs of integrity in data transmission.

Index Terms— SDR, reconfigurability, SHA-192, Unified architecture, Hardware utilization

1. INTRODUCTION

Cryptographic hash functions have been widely applied in science of information security. It protects data from theft or alteration and it can also be used for user authentication. Modern cryptography concerns itself with confidentiality, integrity, non-repudiation, and authentication. There is current and growing interest in universal terminals (multi services, multi networks) for wireless networks. The technical approach to these universal terminals includes developing reconfigurable terminals. The reconfigurable terminals can change their hardware configuration and can support multi-operation modes. This idea of reconfigurability leads to the development of software radio techniques which requires secure software downloading for reconfiguration.

Hardware architecture for high performance AES algorithm has been implemented for encryption process which is useful for SDR terminals[1]. Also radio security module that offers a SDR security architecture that enables separate software and hardware certification is being developed[2]. Security encryption is achieved using the characteristics of the Field Programmable Gate Array, which allows the system to be arranged in a variety of different layouts[3]. Cryptographic components are also exchanged for secure download. It includes the possibility to change any of the cryptographic components employed [4]-[5]. In this paper, reconfigurable hardware architecture has been proposed with an aim to provide secure download in SDR terminals. Also the area utilization of proposed architecture is analyzed with an aim to have optimized area and power consumption.

2. MD-5 AND SHA-1 ALGORITHM

2.1. MD5 Algorithm

MD5 [6] was introduced in 1992 by Professor Ronald Rivest. It calculates a 128-bit digest for an arbitrary 1-bit message. It is an enhanced version of its predecessor MD4. The algorithm could be described in two stages: Preprocessing and hash computation. Preprocessing involves padding a message, parsing the padded message into m-bit blocks, and setting initialization values to be used in hash computation. The final hash value generated by the hash computation is used to determine the message digest.

1. Append Padding Bits

The b-bit message is padded so that a single 1 bit is appended to the end of the message, and then 0 bits are appended until the length of the message becomes congruent to 448, modulo 512.

2. Append Length

A 64-bit representation of b is appended to the result of the padding. The resulting message has a length that is an exact multiple of 512 bits. This message is denoted here as Y.

3. Initialize MD Buffer

Let A, B, C, D be 32-bit registers. These registers are initialized to the following values in hexadecimal, low-order bytes first: Word A: 01234567 B: 89abcdef Word C: fedcba98 Word D: 765432
4. Process Message in 16-Word Blocks

This is the heart of the algorithm, which includes four rounds of processing. It is represented by HMD5 in Fig.1 and its logic is given in Fig.2. The four rounds have similar structure but each uses different auxiliary functions F, G, H and I.

\[
\begin{align*}
F(X, Y, Z) &= (X \text{ and } Y) \text{ or } ((\text{not} X) \text{ and } Y) \\
G(X, Y, Z) &= (X \text{ and } Z) \text{ or } (Y \text{ and } (\text{not} Z)) \\
H(X, Y, Z) &= X \text{ xor } Y \text{ xor } Z \\
I(X, Y, Z) &= Y \text{ xor } (X \text{ or } (\text{not} Z))
\end{align*}
\]

Each round consists of 16 steps and each step uses a 64-element table \( T [1 ... 64] \) constructed from the sine function. Let \( T[i] \) denote the i-th element of the table, which is equal to the integer part of 232 times abs(sin(i)), where i is in radians. Each round also takes as input the current 512-bit block \( Y_q \) and the 128-bit chaining variable \( CV_{q} \). An array \( X \) of 32-bit words holds the current 512-bit \( Y \). For the first round the words are used in their original order.

The following permutations of the words are defined for rounds 2 through 4:

\[
\begin{align*}
?2(i) &= (1 + 5i) \mod 16 \\
?3(i) &= (5 + 39) \mod 16 \\
?4(i) &= 7i \mod 16
\end{align*}
\]

The output of the fourth round is added to the input of the first round (\( CV_{q} \)) to produce \( CV_{q+1} \).

5. Output

After all L 512-bit blocks have been processed, the output from Lth stage is the 128-bit message digest. Fig 2 shows the operations involved in single step. The additions are modulo 232. Four different circular shift amounts \( S \) is used each round and are different from round to round. Each step is of the following form,

\[
\begin{align*}
A \rightarrow D \\
B \rightarrow B + ((A + Funs(B, C, D) + X[K1 + T[i]]) < s) \\
C \rightarrow B \\
D \rightarrow C
\end{align*}
\]

2.2. The SHA-1 Algorithm

The Secure Hash Algorithm was developed by National Institute of Standards and Technology (NIST) and published as a federal information processing standard in 1993[7]. It calculates a 160-bit digest for an arbitrary l-bit message. Pre-processing is done same as in MD5 except that an extra 32-bit register \( E \) is added with an initial value of C3D2E1F0. Other registers are assigned with higher order bytes first. For each block, it requires 4 rounds of 20 steps, resulting in a total of 80 steps, to generate the message digest. Fig.3 shows the SHA-1 compression function [8].

Functions

A sequence of logical functions \( f_0, f_1, ..., f_{79} \) is used in the SHA-1. Each \( f_t \), \( 0 \leq t \leq 79 \), operates on three 32-bit words \( B, C, D \) and produces a 32-bit word as output. \( f_t(B,C,D) \) is defined as follows, for words \( B, C, D, \)

\[
\begin{align*}
ft(B,C,D) &= (B \text{ and } C) \text{ or } ((\text{not} B) \text{ and } D), \quad \text{for } 0 \leq t \leq 19 \\
ft(B,C,D) &= B \text{ xor } C \text{ xor } D, \quad \text{for } 20 \leq t \leq 39 \\
ft(B,C,D) &= (B \text{ and } C) \text{ or } (B \text{ and } D) \text{ or } (C \text{ and } D), \quad \text{for } 40 \leq t \leq 59 \\
ft(B,C,D) &= B \text{ xor } C \text{ xor } D, \quad \text{for } 60 \leq t \leq 79
\end{align*}
\]
Constants A sequence of constant words K(0), K(1), ... , K(79) is used in the SHA-1. In hex these are given by

\[ \begin{align*}
K_t &= 5A827999 & (0 \leq t \leq 19) \\
K_t &= 6ED9EBA1 & (20 \leq t \leq 39) \\
K_t &= 8F1BBCDC & (40 \leq t \leq 59) \\
K_t &= CA62C1D6 & (60 \leq t \leq 79)
\end{align*} \]

Computing the Message Digest

The message digest is computed using the final padded message. The computation uses two buffers, each consisting of five 32-bit words, and a sequence of eighty 32-bit words. The words of the first 5-word buffer are labeled A, B, C, D, E. The words of the second 5-word buffer are labeled H0, H1, H2, H3, H4. The words of the 80-word sequence are labeled W0, W1... W79. A single word buffer TEMP is also employed. To generate the message digest, the 16-word blocks M1, M2... Mn is processed in order. The processing of each Mi involves 80 steps. Single step operation of SHA-1 is shown in Fig.4. Before processing any blocks, the \( \{H_i\} \) are initialized as follows in hex:

\[ \begin{align*}
H0 &= 67452301, H1 = EFCDAB89, H2 = 98BADCFE, \\
H3 &= 10325476, H4 = C3D2E1F0.
\end{align*} \]

Now M1, M2... Mn is processed. To process Mi, the following procedure can be executed:

a. Divide Mi into 16 words W0, W1, ... , W15, where W0 is the left-most word.
b. For t = 16 to 79 let Wt = S1(Wt-3 XOR Wt-8 XOR Wt-14 XOR Wt-16).
c. Let A = H0, B = H1, C = H2, D = H3, E = H4.
d. For t = 0 to 79 do
   TEMP = S5(A) + ft(B,C,D) + E + Wt + Kt;
   E = D;
   D = C;
   C = S30(B);
   B = A;
   A = TEMP;
e. Let H0 = H0 + A, H1 = H1 + B, H2 = H2 + C, H3 = H3 + D, H4 = H4 + E.

After processing Mn, the message digest is the 160-bit string represented by the 5 words H0 H1 H2 H3 and H4.

3. Proposed SHA-192 Algorithm

The proposed SHA-192 is another improved version in SHA family. It may be used to hash message, M having a length of l bits, where 0 < l < 2^64. The algorithm uses, Six working variables of 32 bits each, A hash value of six 32-bit words. The final result of SHA-192 is the 192 bit message digest. The words of the message schedule are labeled W0, W1, W2... W79. The six working variables are labeled A,B,C,D,E and F. The words of the hash value are labeled H0(0),... which

\[ \begin{align*}
H0(0) &= 67452301, H1(0) = EFCDAB89, H2(0) = 98BADCFE, \\
H3(0) &= 10325476, H4(0) = C3D2E1F0, H5(0) = F9B2D834.
\end{align*} \]

The compression function of SHA-192 has been illustrated in Fig.4.

3.1. SHA-192 preprocessing

The padding and appending of bits are done same as for MD5 and SHA-1. Before processing any blocks, the \( \{H_i\} \) are initialized as follows (in hexadecimal):

\[ \begin{align*}
H0 &= 67452301, H1 = EFCDAB89, H2 = 98BADCFE, \\
H3 &= 10325476, H4 = C3D2E1F0, H5 = F9B2D834.
\end{align*} \]

The compression function of SHA-192 has been illustrated in Fig.4.

3.2. SHA-192 hash computation

A sequence of logical functions f0, f1,..., f79 is used in the SHA-192. Each ft, 0 <= t <= 79, operates on three 32-bit words B, C, D and produces a 32-bit word as output. ft(B,C,D) is defined as follows, for words B, C, D,
\[ ft(B,C,D) = (B \text{ and } C) \text{ or } ((\neg B) \text{ and } D), \quad \text{for } 0 \leq t \leq 19 \]
\[ ft(B,C,D) = B \text{ xor } C \text{ xor } D, \quad \text{for } 20 \leq t \leq 39 \]
\[ ft(B,C,D) = (B \text{ and } C) \text{ or } (B \text{ and } D) \text{ or } (C \text{ and } D), \quad \text{for } 40 \leq t \leq 59 \]
\[ ft(B,C,D) = B \text{ xor } C \text{ xor } D, \quad \text{for } 60 \leq t \leq 79 \]

A sequence of constant words \(K(0), K(1), \ldots, K(79)\) is used in the SHA-1. In hex these are given by

\[
\begin{align*}
K_t &= 5A827999 \quad (0 \leq t \leq 19) \\
K_t &= 6ED9EBA1 \quad (20 \leq t \leq 39) \\
K_t &= 8F1BBCDC \quad (40 \leq t \leq 59) \\
K_t &= CA62C1D6 \quad (60 \leq t \leq 79)
\end{align*}
\]

Now \(M_1, M_2, \ldots, M_n\) is processed. To process \(M_i\), we proceed as follows:

a. Divide \(M_i\) into 16 words \(W_0, W_1, \ldots, W_{15}\), where \(W_0\) is left-most word.

b. For \(t = 0\) to \(15\), \(W_t = M_i\)

For \(t = 16\) to \(79\), let \(W_t = S_1(W_{t-3} \text{ XOR } W_{t-8} \text{ XOR } W_{t-14} \text{ XOR } W_{t-16})\).

c. Let \(A = H_0, B = H_1, C = H_2, D = H_3, E = H_4, F = H_5\).

d. For \(t = 0\) to \(79\) do

\[
\begin{align*}
\text{TEMP1} &= S_5(A) + ft(B,C,D) + E + W_t + K_t; \\
\text{TEMP2} &= S_5(A) + A + ft(B,C,D) + E + W_t + K_t + F; \\
E &= D; \\
D &= C; \\
C &= S_30(B); \\
B &= S_15(A); \\
F &= \text{TEMP1}; \\
A &= \text{TEMP2}
\end{align*}
\]

e. Let \(H_0 = H_0 + A, H_1 = H_1 + B, H_2 = H_2 + C, H_3 = H_3 + D, H_4 = H_4 + E, H_5 = H_5 + F\).

After processing \(M_n\), the message digest is the 160-bit string represented by the 6 words \(H_0, H_1, H_2, H_3, H_4, H_5\).

4. UNIFIED ARCHITECTURE OF MD-5 AND SHA-192

Many architecture has been used to implement these hash function individually in hardware [8]-[15]. The proposed architecture figure 5, has two built in hash function say MD5 and the proposed SHA-192. Both the algorithms in same architecture so that it can operate for one function one time and for other function next time. In the case of the MD5 operation the data transformation four inputs/outputs B,C,D,E of each one of the four Data Transformation Rounds. The input/output named A,F is not used , for this hash function operation (MD5). This is due to the fact that MD5 processes on 128-bit blocks (4x32-bit) transformation blocks, instead of the 192-bit blocks that are used in SHA-192. The four Data Transformation Rounds are similar, but its one performs a different operation. MA components indicate modulo addition 232, while the shifters components define left shift rotations of the input data block[8]. The Data Transformation Round I operation is based on a Nonlinear Function i transformation of the three of B\textsubscript{In}, C\textsubscript{In}, and D\textsubscript{In}, inputs. Then, this result is added to the fourth input E\textsubscript{In} with the input data block and the constant. That result is rotated to the right and the rotated output data are added with the input D\textsubscript{In}. The each Data Transformation Round, which perform the digital logic transformation according to equations.The Hash the Function Core shown in fig 5 can be used alternatively for the operation SHA-192 hash function also. The data transformation unit and the data transformation rounds process the data in a different way, compared with MD5 operation mode, in order the Hash Function Core to perform efficiently as SHA-192.For the SHA-192 operation each Data Transformation Round operates on all the six 32-bit variables (inputs/outputs) and this is one of the basic differences compared with MD5 mode. Thus the combined architecture of MD-5 and SHA-192 results in reduced hardware utilization compared to the individual implementation of MD-5 and SHA-1.
The data transformation for combined hash computation is described in Fig 6. In the hardware realization, a select line is inserted which selects the functionality of appropriate algorithm at each block.

5. Results and discussion

The hardware architecture is implemented in Verilog, and synthesis is performed with Xilinx ISE 9.2i. Virtex II kit is used for downloading the synthesized code. The power analysis is done using Synopsys Design Vision. The synthesis result for individual implementation of MD5 and SHA-1 is tabulated in Table 1 and 2. For the implementation, FPGA device 2v4000bf957-6 was used and the achieved operating frequency is equal to 57.36 MHZ and the system allocated area are 162 I/Os, 724 Function generators and 406 CLBs and 298 DFFs are utilized. In Table individual implementation of SHA-1 is summarized. The achieved operating frequency is equal to 83.801 MHZ and the system allocated area are 194 I/Os, 2349 Function generator and 1333 CLBs and 1257 DFFs are utilized.

![Figure 7 Hash output of MD5 and SHA-192 in Individual and combined architecture](image_url)
In Table 1, hardware utilization of MD5 and SHA-192 is summarized. The comparative study shows that a unified architecture utilizes less area than individual structures.

| Current Simulation Time: 1e+06 ps | 0.000 | 2.000 | 2.000 | 2.000 | 2.000 |
|-----------------------------------|-------|-------|-------|-------|-------|
| I/Os                              | 162/684 | 23%   |       |       |       |
| Fun. Generators                   | 724/46080 | 1% |       |       |       |
| CLB Slices                        | 406/23040 | 1% |       |       |       |
| Dffs and Latches                  | 298/46080 | 0% |       |       |       |
| frequency                         | 57.36 MHZ |       |       |       |       |
| Power consumption                 | 4.55 MW |       |       |       |       |

In Table 2, hardware utilization of SHA-192 is shown. The comparative study shows that a unified architecture utilizes less area than individual structures.

| Current Simulation Time: 1e+06 ps | 0.000 | 2.000 | 2.000 | 2.000 | 2.000 |
|-----------------------------------|-------|-------|-------|-------|-------|
| I/Os                              | 194/684 | 28%   |       |       |       |
| Fun. Generators                   | 2349/46080 | 5% |       |       |       |
| CLB Slices                        | 1333/23040 | 5% |       |       |       |
| Dffs and Latches                  | 1257/46080 | 2% |       |       |       |
| Frequency                         | 83.801 MHZ |       |       |       |       |
| Power Consumption                 | 15.49 mW |       |       |       |       |

Figure 8: Hash output of MD5 and SHA-192 in combined architecture.
also consumes less power.

**Table 3. Hardware utilization of unified architecture**

| FPGA device: 2v4000bf957-6 |  |
|-----------------------------|--|
| **Allocated area**  | **Used/Available**  | **Utilization** |
| I/Os                      | 195/684              | 28%            |
| Fun.Generators            | 1275/46080           | 2%             |
| CLB Slices                | 757 / 23040          | 3%             |
| Diffs and Latches         | 1033/46080           | 2%             |
| **frequency**             | 105.67 MHZ           |                |
| **Power Consumption**     | 7.092mW              |                |

From the tabulation, it could be inferred that the device utilization is less in unified architecture compared with the individual implementation of MD-5 and SHA-1. The unified architecture of MD-5 and SHA-192 proved to consume less power and also efficient in computing the hash.

**Figure 9. Area Delay Product Comparison.**

Fig 9 shows the area delay product comparison of individual architectures and the unified architecture. From which it could be inferred that the area utilization of proposed combined architecture is less than available logic of FPGA chip used. The requirement of portability of mobile phones and hand held devices places severe restriction on power consumption. In proposed architecture low power design techniques is used to reduce the power consumption.

**Conclusion**

In this work, VLSI architecture of the integrity unit for the reconfigurable receiver is presented. The proposed architecture is reconfigurable in the sense that operates either to give MD-5 hash or the SHA-192 message digest. It guarantees high security level in reconfigurable receivers requiring data integrity and message authenticaiton. The comparisons of synthesis results, proved that the proposed integrity unit is better, compared with the individual implementation of the hash algorithms. The power consumption is also proved to be applicable for the reconfigurable receiver terminals.the introduced Integrity unit can be sed in all types of SHA-1, MD5 application with high speeed demands and with high level security needs at the same time.

**References**

1. Center for Software Defined Radio: Terms, Trends and Perspectives, White Paper, 2007. http://www.csdr.cl
2. Badillo, Claudia Feregino-Urbe, Rene Cumplido, Morales-Sandoval, "FPGA Implementation and Performance evaluation of AES-CCM Cores for Wireless Networks." In Proceedings of 2008 International Conference on Reconfigurable Computing and FPGAs.
3. Lozano, Marianela Garcia Moradi, Farshad Ayani, Rassul " SDR: A Semantic Based Distributed Repository for Simulation Models and Resources" In Proceedings of Modelling & Simulation, 2007. AMS '07, First Asia International Conference on March 2007.
4. Chih Fung lam, Koisakaguchi, Jun-ichi takada, kiyomichiharaki,"Radio Security Module that Enables Global Roaming of SDR Terminal while Complying with Local Radio Regulation" IEEE proceedings 2003.
5. Hironori uchikawa, Kenta umeyashy, Ryuji kohno "Secure download system based on software define radio composed of FPGAs" IEEE proceedings 2002.
6. Rivest, R., The MD5 Message Digest Algorithm, RFC 1321, MIT LCS and RSA Data Security, Inc., April 1992
7. SHA-1 standard, National Institute of standards and technology (NIST),’’Secure Hash Standards’’, FIPS PUB180-1www.itl.nist.gov/fipspub/fips180-1.html 2003.
8. Dominikus, ”A Hardware Implementation of MD4-Family Hash Algorithms”, proceedings of IEEE International Conference on Electronics Circuits and Systems (ICECS’02), Vol. III, pp.1143-1146, Croatia, September 15-18, 2002.
9. J. Deepakumara, H. M. Heys, and R. Venkatesan.” FPGA implementation of MD5 hash algorithm.” In Proceedings of IEEE Canadian Conference on Electrical and Computer Engineering (CCECE 2001), Toronto, Ontario, May 2001.
10. N.sklavos, P. P. kitos K. Papadopoulos O. koufopavlou “Design, Architecture and Performance Evaluation of the Wireless Transport Layer Security” The Journal of Supercomputing, 36, 33–50, 2006 C, 2006 Springer Science + Business Media, Inc. Manufactured in The Netherlands.
11. N.sklavos, P. P. kitos K. Papadopoulos O.Koufopavlou” Open Mobile Alliance Security Layer: Architecture, Implementation and Performance Evaluation of The Integrity Unit,” New Generation Computing: Computing paradigms and computational Intelligence, Springer-Verlag, 2004.
12. Touch, J.D.,”Performance Analysis of MD5,”in proc. Of ACM SIGCOMM’95
13. A Simple Method of Estimating Power In FPGAs, Application Brief XBRF 014v1.0, Xilinx, Sanjose, California USA2003.
14. Handbook of Applied Cryptography, by A. Menezes, P. van Oorschot, and S.Vanstone, CRC Press, 1996.
15. KJarvinen, M.Tomniskaj, Skytta,” Hardware Implementation Analysis Of The MD5 Hash Algorithm," Proceedings Of 38th Annual Hawaii International Conference On System Science,2005
16. R.Tessier and .Burleson,” Reconfigurable Computing for Digital Signal Processing: A Survey,” Journal of VLSI Signal Processing,,Vol.28. No1-2, Pp7-27
17. B.Schineir, Applied Cryptography, Protocol, Algorithms And Source Code In C, 2nd Ed.Newyork: Wiley 1996
18) Randal K. Nicholas and Pannos C. Lekkas, Wireless Security: models, threats and solution, Tata McGraw-Hill 2006.

19) Esam Khan, M. Watheq El-Kharashi, Fayez Geballi, and Mostafa Abd-El-Barr, “Design and Performance Analysis of A Unified Reconfigurable HMAC Hash Unit,” IEEE Transaction on Circuits and Systems, Vol.54, No.12, Pp.2683-2695, December 2007.

L. Thulasimani has obtained her BE and ME degree from Coimbatore Institute of Technology, India in 1998 and 2001 respectively. She has started her teaching profession in the year 2001 in PSNA engineering college, Dindigul. At present she is a Lecturer in department of Electronic and Communication Engineering in PSG college of Technology, Coimbatore. She has published 4 research papers in International and National conferences. She is a part time Ph.D research scholar in Anna University Chennai. His areas of interest are Wireless security, Networking and signal processing. She is a life member of ISTE.

Dr. M. Madheswaran has obtained his Ph.D. degree in Electronics Engineering from Institute of Technology, Banaras Hindu University, Varanasi in 1999 and M.E degree in Microwave Engineering from Birla Institute of Technology, Ranchi, India. He has started his teaching profession in the year 1991 to serve his parent Institution Mohd. Sathak Engineering College, Kilakarai where he obtained his Bachelor Degree in ECE. He has served KSR college of Technology from 1999 to 2001 and PSNA College of Engineering and Technology, Dindigul from 2001 to 2006. He has been awarded Young Scientist Fellowship by the Tamil Nadu State Council for Science and Technology and Senior Research Fellowship by Council for Scientific and Industrial Research, New Delhi in the year 1994 and 1996 respectively. His research project entitled “Analysis and simulation of OEIC receivers for tera optical networks” has been funded by the SERC Division, Department of Science and Technology, Ministry of Information Technology under the Fast track proposal for Young Scientist in 2004. He has published 120 research papers in International and National Journals as well as conferences. He has been the IEEE student branch counselor at Mohamed Sathak Engineering College, Kilakarai during 1993-1998 and PSNA College of Engineering and Technology, Dindigul during 2003-2006. He has been awarded Best Citizen of India award in the year 2005 and his name is included in the Marquis Who’s Who in Science and Engineering, 2006-2007 which distinguishes him as one of the leading professionals in the world. His field of interest includes semiconductor devices, microwave electronics, optoelectronics and signal processing. He is a member of IEEE, SPIE, IETE, ISTE, VLSI Society of India and Institution of Engineers (India).