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Process Conditions for Low Interface State Density in Si-passivated Ge Devices with TmSiO Interfacial Layer

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Abstract
In this work we study the epitaxial Si growth with Si$_2$H$_6$ for Ge surface passivation in CMOS devices. The Si-caps are grown on Ge in the hydrogen desorption limited regime at a nominal temperature of 400 °C. We evaluate the process window for the interface state density and show that there is an optimal Si-cap thickness between 8 and 9 monolayers for $D_{it} < 5 \cdot 10^{11} \text{cm}^{-2}\text{eV}^{-1}$. Moreover, we discuss the strong impact of the Si-cap growth time and temperature on the interface state density, which arises from the Si thickness dependence on these growth parameters. Furthermore, we successfully transfer a TmSiO/Tm$_2$O$_3$/HfO$_2$ gate stack process from Si to Ge devices with optimized Si-cap, yielding interface state density of $3 \cdot 10^{11} \text{eV}^{-1}\text{cm}^{-2}$ and a significant improvement in oxide trap density compared to GeO$_x$ passivation.

Introduction
Germanium based transistors have attracted considerable research interest in recent years as one of the contenders for future CMOS technology nodes due to its high intrinsic electron and hole mobilities. Ge surface passivation with a thin silicon layer (Si-cap) has been shown to be efficient in terms of interface state density ($D_{it}$) and mobility, as well as advantageous over GeO$_x$ passivation regarding bias temperature instability reliability (1), (2). However, the performance of Si-passivated Ge devices is highly dependent on Si-cap growth conditions. For example, The Si-cap thickness is one of the key parameters in achieving low $D_{it}$. An optimal Si thickness in the range of 6-8 monolayers (ML) has been found for different gate fabrication schemes (3)–(6). In thick Si-caps, the interface state density degradation is related to plastic relaxation of the Si layer at around 12 ML thickness (7). On the other hand, when the Si-cap is thin, Ge segregation in the Si layer causes $D_{it}$ generation (3), (4). It has been shown that hydrogen plays an important role in Ge segregation in the Si-caps (4), (8). In the presence of hydrogen, it is more energetically favourable for Si to be at the surface due to lower surface energy of H-covered Si than H-covered Ge. However, a H-free Ge surface has lower energy than H-free Si, giving rise to Ge surface segregation in H-free conditions. As a result, a low temperature hydrogen desorption limited Si-cap deposition process employing higher order Si precursors (Si$_3$H$_8$, Si$_5$H$_8$ or Si$_6$H$_{10}$) is needed. While Si-cap growth using Si$_3$H$_8$ (3), (4), (6), (7) and Si$_6$H$_{10}$ (6) have been explored, the studies of Si growth using the more cost-effective disilane (Si$_2$H$_6$) are mostly limited to ultra-high vacuum chemical vapour deposition (UHV CVD) (9)–(11). In addition, as the process window in terms of Si layer thickness is small and previous studies were performed at fixed temperatures, it is necessary to address the robustness
of the process conditions needed to achieve such precise Si-cap thickness. Furthermore, the Si-cap contributes to the capacitance equivalent thickness of the gate stack. Employing a high-k interfacial layer instead of a chemical SiO$_2$ thus could be beneficial. Thulium silicate (TmSiO) as a replacement of SiO$_2$ interfacial layer has been demonstrated in silicon gates with $D_{it} \sim 10^{11}$ eV$^{-1}$cm$^{-2}$ (12), and we have also shown GeO$_x$/Tm$_2$O$_3$ gate stacks with $D_{it} < 5 \cdot 10^{11}$ eV$^{-1}$cm$^{-2}$ (13). Hence, integrating TmSiO in Si-passivated Ge gates is a viable option.

In this paper, we evaluate the process window for Ge devices with Si-cap passivation using reduced pressure CVD from Si$_2$H$_6$ in the low temperature hydrogen desorption regime. We show that deposition time and growth temperature have a strong influence on the interface state density. Moreover, high-k TmSiO interfacial layer is integrated in the Si-cap process and $D_{it}$ comparable to GeO$_2$ passivation is demonstrated while simultaneously achieving low oxide trap density.

**Experimental**

All epitaxial layers in this work were grown in an ASM Epsilon 2000 CVD tool equipped with a cold wall lamp heated reactor. The temperature in the reactor is measured on the susceptor by thermocouples. The growth pressure was always kept at 20 Torr and the H$_2$ carrier gas flow was kept constant at 20 slm. Ge strain relaxed buffers (SRBs) were grown on (100) Si wafers in a two-step process using a germane precursor (10 % GeH$_4$ in H$_2$) including a post-epi thermal treatment at 890 °C (14) in order to create virtual substrates for Si growth. SRBs had a background doping concentration of $\sim 10^{15}$ cm$^{-3}$, RMS surface roughness < 1 nm and a threading dislocation density $\sim 10^{7}$ cm$^{-2}$. After n-type doping by using a phosphine precursor (5% PH$_3$ in H$_2$) a dopant concentration of $\sim 1 \cdot 10^{16}$ cm$^{-3}$ was achieved. The virtual substrates received an H$_2$ bake at 850 °C for 10 min to desorb any residual Ge oxides before Si growth. The temperature was then slowly ramped down to the growth temperature in H$_2$ ambient. Epitaxial Si layers were grown on Ge virtual substrates using a Si$_2$H$_6$ flow of 50 sccm at temperatures between 400 and 600 °C. After the Si growth, the temperature was ramped down from the growth temperature to <250 °C in H$_2$ ambient before moving the wafers into the N$_2$ purged unload station. The hydrogen coverage of the silicon surface reduces the initial oxidation of Si after unloading. The thicknesses of the Si-cap layers were measured immediately after the growth using spectroscopic ellipsometry. To interpret the ellipsometry measurements we assumed that the optical properties of the Si-cap layers were not affected by any plastic relaxation or surface roughness.

Si-passivated Ge MOS capacitors (MOSCAPs) were fabricated on Ge virtual substrates. Thin Si-caps were deposited at a nominal temperature of 400 °C as described above. The growth temperature was varied by ±3 °C in order to investigate the influence of Si growth temperature variation on the interface state density. In order to minimize Si-cap thickness consumption due to oxidation in air, 400 nm SiO$_2$ was deposited by plasma-enhanced CVD at 400 °C immediately after unloading the wafers from the epitaxy reactor. Active areas were defined by lithography and reactive ion etching was employed to remove $\sim 350$ nm of the SiO$_2$ layer. After removing the remaining SiO$_2$ from the active areas with 1 % HF solution, gate stack layers were deposited by atomic layer deposition (ALD) in a Beneq TFS 200 reactor equipped with a load lock. First, Tm$_2$O$_3$ was deposited at 225 °C using TmCp$_3$ and H$_2$O precursors (15) with a target thickness of 7.4 nm. Thulium silicate (TmSiO) interfacial layer
was then formed by rapid thermal anneal (RTA) at 550 °C for 60 s in N₂. High-k ALD HfO₂ was deposited using HfD04 and H₂O precursors with a target thickness of 5.6 nm at 350 °C followed by a post deposition anneal (PDA) in O₃ for 10 min. After 12 nm ALD TiN gate metal deposition at 425 °C (TiCl₄ and NH₃ precursors), a thick 500 nm Al was deposited by sputtering for electrical probing purposes followed by gate patterning. The device fabrication finished with a forming gas anneal (FGA) of 10% H₂ in N₂ at 400 °C for 30 min. The resulting gate stack is schematically depicted in Figure 1 (a) while Figure 1 (b) shows a cross-section TEM image of the gate stack with Si layer grown at the nominal temperature of 400 °C for 40 min. After Si reaction with Tm₂O₃ forming TmSiO of ~1 nm thickness, the remaining Si-cap has an approximate thickness of 0.5 nm. Reference MOSCAPs with Ge/GeOₓ/Tm₂O₃/HfO₂ gate stacks were also fabricated by a similar process as in (13), with addition of ALD HfO₂ and FGA.

Capacitance voltage (CV) measurements at 10-500 kHz frequencies were performed on the MOS capacitors with Cascade 12000 wafer prober and Keithley SCS 4200. Interface state density in the midgap was evaluated from CV characteristics at 10 kHz for 10 devices (each on a separate die) of each sample using a method described in (16).

**Results and Discussion**

**Epitaxial growth of Si on Ge using disilane**

In order to investigate Si growth with Si₂H₆ for Ge passivation, Si growth kinetics in 400-600 °C temperature range were studied. Figure 2 displays Si thickness as a function of the deposition time at growth temperatures between 400 °C and 500 °C. The thickness was measured on five points over a 100 mm wafer by spectroscopic ellipsometry, and the thickness uniformity (Range/Average) was <3 %. The Si thickness exhibits a linear time dependence, as indicated by simple linear regression. Linear growth dependence was also obtained for higher temperatures (not shown here). There is a clear incubation time before the Si growth starts and the incubation time was determined from the linear regressions intercept with the time axis, see Fig. 2. The incubation time decreases with increasing growth temperature, as shown in Fig. 3. It is possible that the observed incubation time is caused by the hydrogen coverage of the starting Ge surface which prevents Si nuclei formation initially. After a certain incubation period, Si nuclei form and Si growth continues with a constant deposition rate. Hydrogen coverage could also explain the temperature dependence of the incubation time. At higher temperatures, hydrogen surface coverage is lower causing the incubation time to drop, and above 500 °C incubation time becomes negligible. Only a very short incubation time was observed in literature (4) when N₂ carrier gas was used for Si growth on Ge with silane (SiH₄) at 500 °C where the growth rate was high initially and started to drop after 6-7 monolayers. The difference between these results could be attributed to the fact that when N₂ carrier gas is used, the starting surface is not hydrogen terminated and Si nuclei can form faster. On the other hand, H₂ carrier gas was used in this work. After the pre-epi anneal the temperature was ramped down to the growth temperature in H₂ ambient, thus creating an H-terminated growth surface which can hinder the nuclei formation in the initial growth stage.

Silicon growth rates at different temperatures were extracted from the slopes of the linear regression in Fig. 2 to obtain an Arrhenius plot displayed in Fig. 4. As expected, in the examined temperature range Si growth rate is exponentially dependent on the growth
temperature. However, two different activation energies $E_A$ are apparent. Below 475 °C, the observed activation energy is 2.0 eV which is similar to the measured hydrogen desorption activation energies (2-2.5 eV) (17)–(19) as well as the Si growth activation energy values obtained using Si$_2$H$_6$ precursor in other reduced pressure CVD tools (2-2.7 eV) (20), (21) and ultra-high vacuum CVD (2-2.1 eV) (22) and therefore indicates a hydrogen desorption limited regime. At higher temperatures ($T \geq 475$ °C) when hydrogen surface coverage is lower, the apparent activation energy is reduced to 1.3 eV suggesting that hydrogen desorption is not the rate limiting step. We propose two possible explanations for the change in the observed activation energy: (i) another reaction step, such as SiH$_3$ adsorption (Si$_2$H$_6$ $(g)$ → 2SiH$_3$ $(a)$), SiH$_2$ formation (2SiH$_3$ $(a)$ → 2SiH$_2$ $(a)$ + H$_2$ $(g)$) or SiH formation (2SiH$_2$ $(a)$ → 2SiH $(a)$ + H$_2$ $(g)$) (23) becomes rate limiting at these temperatures; or (ii) an alternative reaction path Si$_2$H$_6$ $(g)$ → SiH$_2$ $(a)$ + SiH$_4$ $(g)$ becomes favorable instead of Si$_2$H$_6$ $(g)$ → 2SiH$_3$ $(a)$ as suggested in (24).

For Si-cap growth, higher hydrogen surface coverage is preferred because it reduces Ge segregation in the Si layer during the growth (4). As a result, temperatures below 475 °C are needed for Si-cap growth with Si$_2$H$_6$. Moreover, a careful estimation of the incubation time is required for precise Si-cap thickness control. Even lower growth temperature where incubation time is less temperature dependent ($T \leq 425$ °C in Fig. 3) could thus be advantageous. Finally, low Si growth rate could also be beneficial for the precise control of the Si-cap thickness. Therefore, Si-cap growth at a nominal temperature of 400 °C has been adopted for Ge passivation in this work.

Process window for Ge passivation with Si-cap at 400 °C

In Si-passivated Ge devices, Si layer thickness plays a key role in determining the interface state density of the gate stack (3)–(5). If Si thickness deviates from the optimal value by even 1-2 monolayers, $D_{it}$ increase by more than $1 \times 10^{12}$ eV$^{-1}$cm$^{-2}$ can occur. Interface state density dependence on the Si-cap growth time at a nominal temperature of 400 °C is displayed in Fig. 5. The lowest interface state density of $3 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ is achieved at the optimal growth time of 40 min, and increases for both shorter and longer growth times. As shown above, epitaxial Si growth rate at temperatures below 475 °C exhibits an exponential temperature dependence with an activation energy $E_A = 2.0$ eV. A one degree temperature deviation from the nominal temperature could then change the growth rate by 5% while a three degree deviation by as much as 14%. Therefore, small temperature deviations could potentially alter the Si layer thickness significantly enough to increase the interface state density of the gate stack. In this section, the process window for Ge passivation with Si-cap grown at 400 °C is investigated.

The influence of Si-cap growth temperature on $D_{it}$ was investigated by introducing a small (up to $\pm 3$ °C) deviation from the nominal growth temperature of 400 °C while keeping the growth time constant at 40 min, as this growth time gave the lowest interface state density (Fig. 5). The interface state density as a function of the deviation from the nominal temperature and in turn as deposited Si-cap thickness is displayed in Fig. 6 where each point shows an average over 10 MOSCAPs and the error bars indicate the range. Si-cap thickness was calculated in the following way. First the growth rate was estimated from the temperature deviation given $E_A = 2.0$ eV. Then the thickness was calculated assuming that the incubation time is not dependent on temperature in such a small temperature interval. Finally, the thickness was converted into
monolayers assuming 1 ML = 1.3 Å for strained Si on Ge. Note that by performing this conversion, non-discrete ML thickness can be obtained. This thickness should be regarded as an average thickness over the surface steps of one (or more) ML height, which then corresponds to non-discrete thickness in ML. Also note that Fig. 6 displays the deposited Si-cap thickness, which after TmSiO formation is reduced by ~4 ML. As evident from Fig. 6, even one degree deviation from the nominal temperature increases $D_D$ 1.5-2 times, from $3 \times 10^{11} \text{ eV}^{-1} \text{cm}^2$ to $4.5 \times 10^{11} \text{ eV}^{-1} \text{cm}^2$ and $6.5 \times 10^{11} \text{ eV}^{-1} \text{cm}^2$ for -1 °C and 1 °C deviation, respectively. The average thickness change due to 1 °C temperature deviation corresponds to 0.4 ML. It is larger than the Si thickness variation over a wafer, which corresponds to 0.25 ML for Si-cap grown at 400 °C for 40 min. If the growth temperature deviates from the nominal temperature more (±3 °C), the Si-cap thickness changes by 1.2-1.4 ML and $D_D$ rises to above $10^{12} \text{ eV}^{-1} \text{cm}^2$. This result is consistent with the interface state density dependence on Si-cap thickness reported in literature for Si growth with SiH$_4$ and Si$_3$H$_8$ (3)–(5). When Si-cap thickness deviates from its optimal value, the interface state density not only degrades but also becomes less uniform within a wafer. At the nominal growth temperature, the range is $8 \times 10^{10} \text{ eV}^{-1} \text{cm}^2$ while at ±3 °C deviation from the nominal temperature, the range is more than $5 \times 10^{11} \text{ eV}^{-1} \text{cm}^2$. This could be explained by Si thickness variation over a wafer. When Si-cap thickness is close to an optimal thickness, small thickness variations over a wafer have little influence on the $D_D$. On the other hand, when Si thickness is far from optimal, the relative thickness variation will give a similar relative $D_D$ variation which then results in higher $D_D$ range.

To further investigate the influence of the process parameters on the interface state density in Si-passivated gate stacks, Si-cap deposition time was varied. The interface state density in Ge gates with Si-caps grown at three different temperatures (nominal 400 °C ± 1 °C) for 30-60 min is depicted in Fig. 7 as a function of the grown Si-cap thickness. Here the Si-cap thickness was calculated in a similar manner as described above. The lowest $D_D$ is achieved at 8-9 ML initial Si-cap thickness indicated by a green rectangle. The interface state density increases as the Si-cap thickness decreases, reaching around $10^{12} \text{ eV}^{-1} \text{cm}^2$ at 6 ML initial thickness. Note that due to Si consumption during TmSiO formation this thickness is estimated to be around 2 ML in the fabricated device. The interface state density degradation could be associated with previously reported Ge surface segregation in thin Si-caps (3), (4). Even though hydrogen surface coverage at 400 °C reduces Ge surface segregation (4), (8), some intermixing of Ge and Si can still occur in the thin Si-cap. Moreover, in very thin Si-caps the whole Si layer could be consumed during TmSiO formation, also increasing the interface state density. An increase in the interface state density is also observed in Ge gates with initial Si thickness higher than 9 ML, where $D_D$ reaches more than $10^{12} \text{ eV}^{-1} \text{cm}^2$ in gates with Si-caps thicker than 12 monolayers. The increase in the interface state density is consistent with the plastic relaxation that has been reported to occur above 12 ML thickness (7).

The process window, when the interface state density is below $5 \times 10^{11} \text{ eV}^{-1} \text{cm}^2$, is defined by both growth temperature and time, and corresponds to between 8 and 9 ML initial Si-cap thickness. For a given growth time, a temperature deviation in the epi-reactor of even one degree (+1 °C in Fig. 7) can alter the Si layer thickness enough to be detrimental to the interface state density. Hence, temperature control when depositing Si-caps for Ge surface passivation is of a paramount importance for achieving low interface state density. Care should be taken to maintain a precise temperature in the epi-reactor, especially after routine temperature...
calibrations and reactor cleans. Alternatively, extending the process window could ensure low
$D_t$ even if small temperature drifts occurred. Expanding the process window for thicker Si-
caps is not an option due to the plastic relaxation of the Si layer. On the other hand, thinner Si-
caps could be employed if Si consumption during the TmSiO process would be limited, e.g. by
lowering the silicate formation temperature.

**Ge MOS capacitors with optimized Si-cap and TmSiO interfacial layer**

In the previous section we have identified that at the growth temperature of 400 °C the
optimum Si-cap thickness is achieved at 40 min growth time. Ge MOS capacitors fabricated
with this Si-cap process demonstrated the lowest interface state density. One of the challenges
in Ge gate stacks is to simultaneously achieve high mobility and adequate reliability. While
low interface state density is a good indication of high mobility, low oxide trap density can
show a potential for superior reliability. For this reason, Ge MOS capacitors with optimal Si-
cap thickness were further electrically characterized to determine the oxide trap density $N_{ox}$
and compared to GeO$_2$ passivated Ge MOS capacitors.

Well behaved CV characteristics of a typical MOS capacitor with
Ge/Si/TmSiO/Tm$_2$O$_3$/HfO$_2$/TiN gate are displayed in Fig. 8 (a). Almost no frequency
dispersion is observed. Interface state density and equivalent oxide thickness were extracted
from CV characteristics of 10 MOSCAPs over a 100 mm wafer. $D_t$ in the midgap was found
to be $\sim 3 \cdot 10^{11}$ eV$^{-1}$cm$^{-2}$ and EOT of 3.7-3.8 nm as displayed in Fig. 8 (b). Reference MOSCAPs
with Ge/GeO$_x$/Tm$_2$O$_3$/HfO$_2$ gates exhibit a similar $D_t$ of $2 \cdot 10^{11}$ cm$^{-2}$eV$^{-1}$. The interface state
density of Si-passivated Ge gates is also consistent with TmSiO/Tm$_2$O$_3$ gate stacks previously
shown on Si, which yielded $D_t \sim 10^{11}$ eV$^{-1}$cm$^{-2}$ (12), demonstrating that no significant $D_t$
degradation occurs when transferring the gate stack process to Si-passivated Ge. The interface
state density in the midgap represents the overall $D_t$ tendency while future work could explore
the interface state density near the band edges and determine the suitability of the gate stack
for pFET or nFET applications.

Oxide trap density $N_{ox}$ in both Si-cap and the reference GeO$_x$ MOS capacitors was extracted
from the hysteresis AV of a dual CV sweep. Dual CV sweep of a typical Si-passivated MOS
capacitor is shown in Fig. 9 (a) while Fig. 9 (b) displays $N_{ox}$ as a function of the oxide electric
field $E_{ox}$ which is defined as:

$$E_{ox} = \frac{V_{G,max} - V_{FB}}{CET}$$

[1]

Here $V_{G,max}$ is the highest voltage to which the dual sweep was performed, $V_{FB}$ is the
flatband voltage and CET is capacitance equivalent thickness. The Si-passivated gates exhibit
a hysteresis of only $\sim 3$ mV at $E_{ox}$ of 4 MV/cm corresponding to $N_{ox}$ of $1.5 \cdot 10^{10}$ cm$^{-2}$. It is more
than 20 times lower than the oxide trap density of the reference GeO$_x$ devices, showing the
superiority of Si-passivated gates. Low oxide trap density in Ge/Si/TmSiO/Tm$_2$O$_3$/HfO$_2$/TiN
gate stacks indicates a potential for improved reliability. This makes Si-passivated Ge gates
with high-k TmSiO interfacial layer a viable candidate for future CMOS technology due to
their potential for both high mobility and superior reliability.

**Conclusions**

Si-cap growth on Ge with Si$_2$H$_6$ in the hydrogen desorption limited regime has been
investigated. The process window for an interface state density \( <5 \times 10^{11} \text{ cm}^{-2} \text{eV}^{-1} \) has been demonstrated to be between 8 and 9 ML Si-cap thickness. Due to the narrow process window, \( D_{it} \) has been shown to be very sensitive to Si-cap growth temperature because even one degree growth temperature deviation alters the resulting Si thickness significantly. While care should be taken to maintain a precise temperature in the epi-reactor, the process window could also be extended by reducing the consumption of the Si-cap during TmSiO formation. The optimized Si-cap process has been implemented in Ge MOS devices with high-k TmSiO interfacial layer yielding \( D_{it} \approx 3 \times 10^{11} \text{ eV}^{-1} \text{cm}^{-2} \) and 20 times lower oxide trap density than GeO\(_2\) passivated Ge gates, demonstrating potential for high mobility and superior reliability.

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Figure 1. (a) Schematically depicted Ge/Si/TmSil/O/Tm2O3/HfO2 gate stack; (b) Cross section TEM image of the gate with the Si-cap grown at a nominal temperature of 400 °C for 40 min with the layers indicated. The TmSilO thickness extracted from the TEM image is 1 nm while the remaining Si-cap thickness is 0.5 nm.
Figure 2. Si thickness versus deposition time at various temperatures. Si layer thickness was measured by spectroscopic ellipsometry. The solid lines are simple linear regression fits to the measured points. The Si growth rates were determined from the slope of the lines and the incubation times were extracted from their intercept with the x-axis at zero thickness.

Figure 3. Incubation time observed in Si growth on Ge with Si-H₆ in H₂, as a function of temperature. The line is a guide for the eye. The incubation time decreases with increasing temperature and becomes negligible above 500 °C.
Figure 4. Si growth rate as a function of the reciprocal absolute temperature (Arrhenius plot). Growth rate is exponentially dependent on the reciprocal temperature. Two apparent activation energies can be observed. The activation energy of 2.0 eV below 475 °C is consistent with that Si growth is in hydrogen desorption limited regime.

Figure 5. Interface state density dependence on Si-cap growth time at a nominal temperature of 400 °C. An optimal growth time exists at 40 min growth time, yielding $D_{it}$ of $3 \times 10^{11}$ eV$^{-1}$cm$^{-2}$. At both, higher and lower, growth times interface state density is degraded.
Figure 6. Interface state density in Si-passivated gate stacks with respect to the deviation from nominal growth temperature and initial Si-cap thickness (1 ML = 1.3 Å). Growth time is 40 min. Each point is an average over 10 measured MOS capacitors, and the error bars indicate the range. Growth temperature deviations alter the Si-cap thickness and cause the interface state density to degrade.

Figure 7. Interface state density of Ge/Si/TmSiO/Tm$_2$O$_3$/HfO$_2$/TiN gates as a function of the as deposited Si-cap thickness for three growth temperatures and 30-60 min growth times. The average over 10 measured devices is displayed and the range is indicated with error bars. The green area indicates a process window between 8-9 ML with $D_{it} < 5 \cdot 10^{11}$ eV$^{-1}$cm$^{-2}$. The interface state density increases in devices with thinner and thicker Si-caps.
Figure 8. (a) Well-behaved CV characteristics of Ge/Si/TmSiO/Tm₂O₃/HfO₂/TiN gate stacks with optimized Si-cap grown at nominal temperature of 400 °C for 40 min. Almost no frequency dispersion is observed in 10-500 kHz frequency range. (b) In 10 characterized MOS capacitors interface state density is around 3·10¹¹ eV⁻¹cm⁻² at EOT of 3.7-3.8 nm.

Figure 9. (a) Dual CV sweep of Ge/Si/TmSiO/Tm₂O₃/HfO₂/TiN gate stacks with optimized Si-cap grown at nominal temperature of 400 °C for 40 min showing hysteresis ΔV < 3 mV. Voltage was swept from inversion to Vg, max in accumulation and back. (b) Oxide trap density Nox extracted from CV hysteresis as a function of the oxide electric field Eox. Si-cap devices exhibit more than 20 times lower oxide trap density than the reference GeOₓ devices.