Phase-Shift PWM Converter with Wide Voltage Operation Capability

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Abstract: A soft switching three-level pulse-width modulation (PWM) converter is presented for industrial electronics with wide voltage range operation, such as solar power or fuel cell applications. Phase shift PWM scheme is used on the input-side to accomplish the zero voltage turn-on on power switches and improve the converter efficiency. Three-level diode-clamp circuit topology is adopted in the presented circuit to lessen the voltage ratings on active devices for high voltage applications. Three sub-circuits with the different turns-ratio of transformers can be selected in the presented converter in order to achieve 10:1 \((V_{in,max} = 10V_{in,min})\) wide input voltage operation when compared to the conventional multilevel converter. The proposed circuit is a single-stage converter instead of two-stage converter to realize wide voltage operation. Therefore, the presented converter has less component counts. Finally, the design procedure and experiments with a 300W laboratory circuit are presented and discussed to confirm the circuit analysis and converter performance.

Keywords: Duty Cycle Control; Power Converters; Wide Voltage Operation; Soft Switching Operation

1. Introduction

Renewable energy power conversions have been widely developed to improve and overcome the energy shortage and air pollution from fossil fuels. Wind power and solar power are the most attractive energy sources in modern power generation systems. Power electronic techniques are widely used in the wind power and solar power conversion system to provide the stable voltage output. However, the output voltage of solar panels and wind turbine generators is variable with the wide variation, due to the output voltage value, is related to solar intensity or wind speed. The classical two-stage or three-stage converters are usually adopted \[1–3\] to overcome the wide voltage variation problem of solar panels and or wind turbine generators, and also provide the stable output voltage. Unfortunately, the classical two-stage or three-stage circuit topologies have high power losses and low efficiency. The series-parallel connected converters have been presented in \[4–7\] to have wide voltage operation. However, the drawbacks of these circuit topologies are many circuit switches and components in these circuit topologies and the circuit reliability and efficiency are reduced. Phase shift pulse-width modulation (PWM) full-bridge or half-bridge converters \[8–12\] have developed to present zero voltage switching (ZVS) and wide voltage operation. The control scheme is more difficult to be implemented by the general analog integrated circuit. The resonant converters \[13–19\] are widely used in the consumer power supplies for their advantages of low switching loss, high efficiency, and galvanic isolation. The inductor-inductor-capacitor (LLC) circuit topology is the most practical resonant converter with high frequency operation when compared to the different resonant circuit topologies. Unfortunately, the input or output voltage range in circuit topologies \[4–19\] is less than 4:1 (i.e., \(V_{in,max} \leq 4V_{in,min}\)) voltage range. Three-level or multi-level converters \[20–23\] with neutral-point diode-clamp, flying capacitor, and series-connected full-bridge circuit topologies are often adopted for high voltage operation to reduce the voltage ratings on active devices. Three-level
ZVS converters [24–28] can further eliminate the switching losses for medium voltage applications. However, the wide voltage operation is seldom discussed and investigated in conventional three-level soft switching converters. The input voltage range of the three-level converter that is discussed in [20–28] is less than 4:1 voltage range operation. For some wind power or solar power applications, the input voltage of DC converters might be greater than 6:1 or 8:1 voltage range, i.e., \( V_{in,max} \geq 6 \) or \( 8 \) \( V_{in,min} \).

A ZVS three-level DC/DC converter is discussed and then investigated to have 10:1 (80 V \( \sim \) 800 V) wide input voltage operation and ZVS operation on active devices. The presented three-level converter has three winding turns and three auxiliary switches on the output-side to achieve wide voltage range operation. Three auxiliary switches on the secondary-side are active or inactive and three different turns-ratio of the isolated transformer are connected to the output load based on the input voltage value. Thus, three equivalent sub-circuits can be operated in the proposed converter to achieve wide voltage operation. Three-level neutral-point diode-clamp converter is adopted on the input-side to have the advantages of low voltage rating and soft switching operation on active devices and increase circuit efficiency. The phase shift PWM operation is used to control the active devices of three-level converter. The leading-leg switches are easily turned on under ZVS operation. The presented circuit has less component counts with better circuit efficiency to achieve 10:1 wide voltage operation when compared to conventional two-stage DC converters. The proposed converter has much wider input voltage operation range as compared to conventional single-stage DC converters with 2:1 or 4:1 voltage range (10:1 voltage range from 80 V \( \sim \) 800 V). The paper is organized, as follows. Section 2 discusses the circuit structure. The circuit operation of the presented converter is provided in Section 3. In Section 4, the circuit characteristics and design procedures are provided. In Section 5, the experiments examine the converter performance and advantages of the presented converter. Subsequently, the conclusion of the presented circuit is discussed in Section 6.

2. Circuit Structure

Figure 1a presents the circuit configuration of the presented circuit topology. Three-level diode clamped converter, including \( S_1 \sim S_4, C_1, C_2, C_f, D_o, D_h, L_r, \) and \( T_f \), is adopted to lessen the voltage stress on power switches for medium input voltage applications. On the secondary-side, three different winding turns, \( n_{s1}, n_{s1} + n_{s2} \) and \( n_{s1} + n_{s2} + n_{s3} \), with alternating current power switches \( Q_1 \sim Q_3 \) are used to provide three different DC voltage gains and extend the voltage range operation. Each switch of \( Q_1 \sim Q_3 \) is implemented by two power MOSFETs with back-to-back connection. When \( Q_1 \sim Q_3 \) are off, the back-to-back body diodes of two MOSFETs are reverse biased and no current will flow through \( Q_1 \sim Q_3 \). The presented converter has three sub-circuits, according to the input voltage range. If \( V_{in} \) is in the low voltage range \( V_{in,L} = V_{in,min} \sim 2V_{in,min} \), the switch \( Q_3 \) turns on and \( Q_1 \) and \( Q_2 \) turn off (Figure 1b). The turns-ratio \( (n_{s1}+n_{s2}+n_{s3})/n_p \) of transformer \( T \) is used in Figure 1b to maintain high voltage gain. In the low input voltage operation, diodes \( D_1 \sim D_4 \) are off. If \( V_{in} \) is in the medium voltage range \( V_{in,M} = 2V_{in,min} \sim 4V_{in,min} \), switch \( Q_2 \) turns on and \( Q_1 \) and \( Q_3 \) turn off (Figure 1c). The secondary turns \( n_{s1}+n_{s2} \) are adopted on the secondary-side. Similarly, switch \( Q_1 \) turns on and \( Q_2 \) and \( Q_3 \) turn off in Figure 1d when \( V_{in} \) is in the high voltage range \( V_{in,H} = 4V_{in,min} \sim 10V_{in,min} \). \( D_5 \sim D_6 \) are reverse biased in this sub-circuit. The low turns-ratio \( n_{s1}/n_p \) is used under the high input voltage range. The secondary winding turns \( n_{s1}, n_{s1} + n_{s2} \) or \( n_{s1} + n_{s2} + n_{s3} \), are connected to the output load to achieve three different DC voltage gains, according to the switching states of \( Q_1 \sim Q_3 \). Therefore, the presented circuit can accomplish the wide voltage operation. The soft switching operation on power switches is also realized due to the phase-shift PWM operation.
Figure 1. Presented converter with 10:1 wide input voltage range operation; (a) circuit structure; (b) low voltage range; (c) medium voltage range; and, (d) high voltage range.
3. Circuit Operation

The presented converter is operated with the phase-shift PWM scheme. The corresponding switches \( Q_1 \sim Q_3 \) are controlled to be on or off, so that the proper secondary winding turns \( n_{s1}, n_{s1} + n_{s2} \) or \( n_{s1} + n_{s2} + n_{s3} \) are connecting to the output road to accomplish wide voltage operation due to the input voltage value. In the presented circuit, it assumes that \( L_{in} \gg L_r, C_1 = C_2, C_{S1} = \ldots = C_{S4} = C_{os}, C_f \gg C_{os}, n_{s1} = n_{s2} = n_{s3}/2 \) and \( V_{C1} = V_{C2} = V_{in}/2 \). The circuit can achieve 10:1, i.e., \( V_{in,max} = 10V_{in,min} \), wide input voltage operation. Three sub-circuits, as shown in Figure 2, can be selected in the presented converter based on the input voltage ranges, \( V_{in,L} = V_{in,min} \sim 2V_{in,min}, V_{in,M} = 2V_{in,min} \sim 4V_{in,min}, \) and \( V_{in,H} = 4V_{in,min} \sim 10V_{in,min} \).

![Figure 2. Cont.](image-url)
3.1. Low Input Voltage Range (Q3 on; Q1, Q2 off)

If $V_{in}$ is in the low voltage range $V_{in,min} \approx 2V_{in,min}$, the secondary-side switch Q3 turns on and Q1 and Q2 turn off (Figure 1b). The winding turns $n_{s1} + n_{s2} + n_{s3}$ are connected to the output inductor. The transformer turns-ratio is $n_L = n_{s0}(n_{s1} + n_{s2} + n_{s3})$. The DC voltage gain is calculated as $G_{DC} = V_o/\sqrt{V_{in,L}} = d_e/n_L$, where $d_e$ is the effective duty cycle and $V_{in,L}$ denotes $V_{in}$ in low input voltage range. Figure 2a shows the PWM waveforms under low input voltage range. Figure 2b–k show the equivalent circuits for states 1–10 respectively in a switching period.

**State 1 [$t_0$, $t_1$]** In state 1, $S_1$ and $S_2$ are conducting and $v_{L,m} \approx V_{C1} = V_{in}/2$ owing to $L_m >> L_r$. The diode $D_5$ is forward biased and $v_{L_o} = V_{in}/(2n_L) - V_o$. The primary-side current is given in Equation (1).

$$i_{L_r}(t) = i_{L_m}(t_0) + (V_{in}/(2n_L) - V_o)(t - t_0)/(n_L L_o)$$

(1)

At time $t_1$, $S_1$ turns off. Since $i_{L_r}(t_1) > 0$, $C_{S1}$ is charged from 0 V and $C_{s4}$ is discharged from $V_{in}/2$.

**State 2 [$t_1$, $t_2$]**: $S_2$ turns off at time $t_1$. $C_{S1}$ ($C_{S4}$) is charged (discharged) from 0 V ($V_{in}/2$). $C_{S1}$ and $C_{S4}$ are about several hundreds of picofarads. Therefore, $i_{L_r}$ and $i_{L_o}$ are almost constant in state 2. If the stored energy in $L_o$ and $L_r$ is greater than the stored energy in $C_{S1}$ and $C_{S4}$, i.e., $(L_r + n_L^2 L_o)^2 i_{L_r}(t_1) \geq C_{oss} V_o^2 / 2$, then $v_{CS4}$ will be decreased to zero at $t_2$. The time duration in state 2 is obtained in (2).

$$\Delta t_{12} = t_2 - t_1 = C_{oss} V_o i_{L_r}(t_1) = n_L C_{oss} V_{in} i_{L_o}(t_1)$$

(2)

The dead time $t_d$ between the gate signals of $S_4$ and $S_1$ should be greater than time duration $\Delta t_{12}$ in state 2 to ensure the ZVS operation of $S_4$ after $t_2$.

**State 3 [$t_2$, $t_3$]**: The body diode $D_{S4}$ is forward biased due to $i_{L_r}(t_2) > 0$ and $v_{CS4}(t_2) = 0$. Therefore, $S_4$ turns on after time $t_2$ to accomplish soft switching turn-on. Because $L_m >> L_r$ and the leg voltage $v_{ab} = 0$, it can obtain the primary-side winding voltage and secondary-side winding voltage are all equal to zero. Diodes $D_5$ and $D_6$ are all forward biased, $v_{L_o} = -V_o$ and $i_{L_o}$ decreases. The primary-side current is calculated in Equation (3).

$$i_{L_r}(t) = i_{L_r}(t_2) - \left( V_{D_{a,d}} + V_{S_{2,d}} \right) (t - t_2)/L_r$$

(3)
where $V_{D_{ad}}$ and $V_{S_{2d}}$ are the drop voltages on diode $D_a$ and switch $S_2$. $i_{DS}$ ($i_{D6}$) decreases (increases) in this state. The slopes of $i_{DS}$ and $i_{D6}$ are expressed in Equation (4).

$$\frac{di_{D6}(t)}{dt} = -\frac{di_{DS}(t)}{dt} = n_L(V_{D_{ad}} + V_{S_{2d}})/2L_r$$

(4)

The state 3 ends at time $t_3$ when $S_2$ is off.

**State 4** [$t_3, t_4$]: This state starts at time $t_3$ when $S_2$ turns off. Owing to $i_{Lr}$ at $t_3$ is positive, $C_{S3}$ ($C_{S2}$) is discharged (charged) from $V_{in}/2$ ($0\, V$). $D_5$ and $D_6$ still conduct in this state. The primary-side winging voltage $v_{Lm} = 0$. If the energy in the inductor $L_r$ is greater than the energy in capacitors $C_{S2}$ and $C_{S3}$, i.e., $L_r^2/(t_3) \geq C_{S3}V_{in}^2/2$, then the capacitor $v_{CS3}$ will be decreased to zero. The time duration in state 4 is calculated as $\Delta t_{4} = t_4 - t_3 = C_{\cos}V_{in}/i_{Lr}(t_3)$ ($t_3$). The dead time $\Delta t_d$ between the gate signals of $S_3$ and $S_2$ should be greater than time interval $\Delta t_{4}$ to have the soft switching turn-on of $S_3$.

**State 5** [$t_4, t_5$]: Because $i_{Lr}(t_4) > 0$ and $v_{CS3}(t_4) = 0$, $D_{S3}$ conducts and $S_3$ turns on after $t_4$ to have ZVS operation. The leg voltage $v_{ab} = -V_{C2} = -V_{in}/2$. Since $D_5$ and $D_6$ all conduct, $v_{Lr}$ equals $-V_{in}/2$ and $i_{Lr}$ decreases in this state. $i_{DS}$ ($i_{D6}$) is decreased (increased) to 0 ($i_{Lr}$) at time $t_5$. The slopes of $i_{DS}$ ($i_{D6}$) are calculated in Equation (5).

$$\frac{di_{D6}(t)}{dt} = -\frac{di_{DS}(t)}{dt} = n_LV_{in}/4L_r$$

(5)

At time $t_5$, $i_{DS}$ is equal to zero ampere and the time interval of state 5 is expressed as $\Delta t_{5} = t_5 - t_4 \approx 4L_r(i_{L0}/n_LV_{in})$. The duty loss in state 5 is calculated as $\Delta i_{loss,5} = \Delta i_{DS}/T_{sw} = 4L_r(i_{L0}/n_LV_{in})$, where $T_{sw}$ is the switching frequency and $T_{sw}$ is the switching period, as both $D_5$ and $D_6$ are still conducting in this state.

The PWM waveforms in the states 6–10 are symmetry to waveforms in the states 1–5. Thus, the circuit analysis and discussion of the states 6–10 are neglected.

### 3.2. Medium Input Voltage Range ($Q_2$ on; $Q_1, Q_3$ off)

If $V_{in}$ is in the medium voltage range, $2V_{in,min} \sim 4V_{in,min}$. The secondary-side switch $Q_2$ turns on and $Q_1$ and $Q_3$ turn off (Figure 1c). The winding turns $n_s1 + n_s2$ are connected to the inductor $L_o$. The transformer turns-ratio under medium voltage range is $n_{M} = n_{PW}/(n_{s1} + n_{s2})$. The DC voltage gain is expressed as $G_{DCM} = V_{o}/V_{in,M} = i_{L0}/n_{M}$, where $V_{in,M}$ denotes $V_{in}$ in medium input voltage range. The proposed converter has less voltage gain under medium input voltage range and larger voltage gain under low input voltage range since $n_L < n_{M}$. Figure 3a illustrates the main PWM circuit waveforms under medium input voltage range. There are ten operating states for every switching cycle. Figure 3b–k shows the different equivalent circuits.

**State 1** [$t_{0}, t_{1}$]: This state starts at time $t_0$ when $S_1$ and $S_2$ are conducting. Because $L_r << L_m$, the primary-side voltage $v_{Lm} \approx V_{C1} = V_{in}/2$. $D_3$ conducts and the inductor voltage $v_{L0} = V_{in}/(2n_{M}) - V_{o}$. Power is delivered from $C_1$ to $R_o$ in state 1. The primary-side current $i_{Lr}(t)$ increases and equals $i_{L0}(t)/n_{M}$.

**State 2** [$t_1, t_2$]: This state starts at time $t_1$ if $S_1$ turns off. $C_{S1}$ ($C_{S4}$) is charged (discharged) from 0V ($V_{in}/2$). If the inductor energy $(L_r + n_{s1}^2L_o)\frac{1}{2}V_{Lm}^2(t_1)/2$ is greater than the capacitor energy $C_{\cos}V_{in}^2/4$, then $v_{CS4}$ is equal to zero at $t_2$.

**State 3** [$t_2, t_3$]: This state starts at time $t_2$ when $v_{CS4} = 0$. Owing to $i_{Lr}(t_2) > 0$, $D_{S4}$ is forward biased and $S_4$ turns on after $t_2$ to have ZVS operation. Because $v_{ab} = 0$, the primary-side winging voltage and secondary-side winging voltage are all zero voltage. Therefore, $D_3$ and $D_4$ are conducting, $v_{L0} = -V_{o}$ and $i_{Lr}$ decreases. The state 3 ends at time $t_3$ when $S_2$ turns off.

**State 4** [$t_3, t_4$]: At $t_3$, $S_2$ turns off. Since $i_{Lr}(t_3) > 0$, $C_{S3}$ is discharged from $V_{in}/2$ to 0V at time $t_4$. $D_3$ and $D_4$ still conduct in this state. If the inductor energy $L_r\frac{1}{2}V_{Lm}^2(t_3)/2$ is greater than the capacitor energy $C_{\cos}V_{in}^2/4$, then $v_{CS3}$ is equal to zero at $t_4$.

**State 5** [$t_4, t_5$]: At $t_4$, $v_{CS3}$ is equal to zero. $D_{S3}$ conducts and $S_3$ turns on after $t_4$ to achieve ZVS operation since $i_{Lr}(t_4) > 0$. The leg voltage $v_{ab} = -V_{C2} = -V_{in}/2$. Owing to $D_3$ and $D_4$ conduct in state
5, \( v_{L_F} \) equals \(-V_{in}/2\) and \( i_{L_F} \) decreases. The diode current \( i_{D3} \) will decrease to 0 at time \( t_5 \). The PWM waveforms in states 6–10 are symmetrical to waveforms in states 1–5, so that the circuit analysis and discussion of states 6–10 are ignored.

\[ \text{Figure 3. Cont.} \]
3.3. High Input Voltage Range (Q1 on; Q2, Q3 off)

When $V_{in}$ is in the high voltage range $V_{in,H} = 4V_{in,min} \sim 10V_{in,min}$. Switch Q1 turns on and Q2 and Q3 turn off (Figure 1d). The winding turns $n_{s1}$ are connected to the inductor $L_o$. For high input voltage range, the transformer turns-ratio is $n_{H} = n_{p}/n_{s1}$ and the DC voltage gain is given as $G_{DC,H} = V_{d}/V_{in,H} = d_{o}/n_{H}$, where $V_{in,H}$ denotes $V_{in}$ in high input voltage range. The proposed converter has the lowest voltage gain under high input voltage range since $n_H > n_M > n_L$. Figure 4a gives the PWM waveforms for high input voltage range and Figure 4b–k show the equivalent circuits for ten operating states in every switching cycle.

State 1 [$t_{0}, t_{1}$]: The state 1 starts at time $t_0$ when $S_1$ and $S_2$ both conduct. Then, the magnetizing voltage $v_{Lm} \approx V_{CL} = V_{in}/2$. Since $D_1$ is conducting, the inductor voltage $v_{L0} = V_{in}(2n_H) - V_o$, and $i_{L0}$ increases.

State 2 [$t_{1}, t_{2}$]: At time $t_1$, $S_1$ turns off. $C_{S1}$ ($C_{S4}$) is charged (discharged) from 0 V ($V_{in}/2$). If the inductor energy $(L_o + n_{s1}^2L_o)^2/L_o(t_1)/2$ is greater than the capacitor energy $C_{os}V_{in}^2/4$, then $v_{CS4} = 0$ at time $t_2$.

State 3 [$t_{2}, t_{3}$]: At time $t_2$, $v_{CS4} = 0$. Since $i_{Lr} > 0$, $D_{S4}$ is conducting. Switch $S_4$ can turn on after time $t_2$ to have zero voltage switching operation. The primary-side winding voltage and secondary-side winding voltage are equal to zero and $D_1$ and $D_2$ are both conducting since $v_{ab} = 0$. The inductor voltage $v_{L0} = -V_o$ and $i_{L0}$ decreases.

State 4 [$t_{3}, t_{4}$]: Switch $S_2$ turns off at time $t_3$. $i_{Lr}(t_3) > 0$ discharges $C_{S3}$ from $V_{in}/2$ to 0 V at time $t_4$. As $D_1$ and $D_2$ both conduct in state 4, the primary-side winging voltage $v_{Lm} = 0$. If the inductor energy $L_r^2/(L_o(t_3)/2$ is greater than the capacitor energy $C_{os}V_{in}^2/4$, then $C_{S3}$ will be discharged to zero voltage.

At time $t_4$, $v_{CS3}(t_4) = 0$. Since $i_{Lr}(t_4) > 0$, $D_{S3}$ is conducting and $S_3$ turns on after $t_4$ to achieve ZVS. In this state, $v_{ab} = -V_{C2} = -V_{in}/2$, $v_{Lr} = -V_{in}/2$ and $i_{Lr}$ decreases. At time $t_5$, the commutation interval of $D_1$ and $D_2$ is completed and $i_{L1}$ is decreased to 0. The circuit operation of the states 6–10 are similar to the circuit analysis of the states 1–5. Therefore, the circuit discussion of the states 6–10 are ignored.
Figure 4. Cont.
The presented three-level converter with different secondary winding turns is controlled with phase-shift PWM operation to realize wide input voltage operation. The secondary switches $Q_1$ to $Q_3$ turn on or off to accomplish the different DC voltage gain in order to control the load voltage based on the different input voltage range. The output voltage is calculated in Equation (6).

$$V_o = \begin{cases} 
\frac{d_s V_{in}(n_{s1} + n_{s2} + n_{s3})}{n_p} & \text{if } V_{in,min} < V_{in} < 2V_{in,min} \text{ (low input voltage range)} \\
\frac{d_s V_{in}(n_{s1} + n_{s2})}{n_p} & \text{if } 2V_{in,min} < V_{in} < 4V_{in,min} \text{ (medium input voltage range)} \\
\frac{d_s V_{in}n_{s1}}{n_p} & \text{if } 4V_{in,min} < V_{in} < 10V_{in,min} \text{ (high input voltage range)} 
\end{cases}$$  (6)

where $d_s = d - d_{loss,5}$ and $d$ is the duty cycle of leg voltage $v_{ab}$. The average current on $L_o$ equals to the load current $i_o$. The average diode currents $I_{D1} = \ldots = I_{D6} = I_o/2$. The average switch currents of $Q_1$ to $Q_3$ equal $I_o$. The voltage ratings of switches $S_1$ to $S_4$ equal $V_{in,max}$ according to the three-level converter topology. The voltage ratings of $D_1$ to $D_6$ are expressed as.

$$V_{D1,\text{stress}} = V_{D2,\text{stress}} = V_{in,max}n_{s1}/n_p$$  (7)

$$V_{D3,\text{stress}} = V_{D4,\text{stress}} = V_{in,max}(n_{s1}+n_{s2})/n_p$$  (8)

$$V_{D5,\text{stress}} = V_{D6,\text{stress}} = V_{in,max}(n_{s1}+n_{s2}+n_{s3})/n_p$$  (9)

The output inductance $L_o$ is calculated in Equation (10), based on the given ripple current $\Delta i_{Lo}$.

$$L_o = \left(\frac{V_{in,max}}{2n_{H}} - V_o\right)\frac{I_{e,\text{min}}T_{sw}}{\Delta i_{Lo}} = V_o(0.5-d_{e,\text{min}})T_{sw}/\Delta i_{Lo}$$  (10)

The duty cycle loss in the state 5 depends on $L_r$ and the inductance $L_r$ can be expressed in Equation (11).

$$L_r = n_{s1}V_{in,min}d_{loss,5}T_{sw}/4I_o$$  (11)

The presented circuit is operated under the input voltage range $V_{in}$ from 80 V to 800 V, $V_o = 12$ V, $P_o,\text{rated} = 300$ W, and $f_{sw} = 150$ kHz. The theoretical three input voltage ranges are $V_{in,L} = 80$ V to 160 V, $V_{in,M} = 160$ V to 320 V, and $V_{in,H} = 320$ V to 800 V. If the input voltage is in the low voltage range ($V_{in} = 80$ V to 160 V), the secondary switch $Q_3$ is on and $Q_1$ and $Q_2$ are off. The winding turns $n_{s1}+n_{s2}+n_{s3}$ connect to the output filter inductor $L_o$. When $V_{in}$ is increased and equal to 160 V (in medium voltage range $V_{in} = 160$ V to 320 V), then $Q_2$ is on and $Q_1$ and $Q_3$ are off. Afterwards, the winding turns $n_{s1}+n_{s2}$ connect to the output inductor $L_o$. Similarly, the input voltage is in the high voltage range from 320 V to 800 V. Switch $Q_1$ is on and $Q_2$ and $Q_3$ are off. Only the winding turns $n_{s1}$ connect to $L_o$. There is a ±20 V voltage tolerance with Schmitt trigger circuit between three voltage ranges to avoid the

![Figure 4. PWM waveforms and equivalent circuits of the presented circuit under high input voltage range; (a) PWM waveforms; (b) state 1 circuit; (c) state 2 circuit; (d) state 3 circuit; (e) state 4 circuit; (f) state 5 circuit; (g) state 6 circuit; (h) state 7 circuit; (i) state 8 circuit; (j) state 9 circuit; and, (k) state 10 circuit.](image-url)
signal oscillation at the voltages 160 V between low and medium input voltage ranges and 320 V between the medium and high voltage ranges. The Schmitt comparators and logic gates shown in Figure 5 are adopted to provide the PWM signals for each output voltage range. Therefore, the actual three input voltage ranges are $V_{in,L} = 80 \text{V} \sim 180 \text{V}$, $V_{in,M} = 140 \text{V} \sim 340 \text{V}$, and $V_{in,H} = 300 \text{V} \sim 800 \text{V}$.

![Diagram](image_url)

**Figure 5.** Control block of the proposed converter.

The proposed converter is assumed to have 90% efficiency at $V_{in} = 80 \text{V}$ and full road condition under low input voltage range (80V ~ 180V). The assumed maximum duty cycle $d_{max}$ of the leg voltage $v_{ab}$ under $V_{in} = 80 \text{V}$ is 0.48. The duty cycle loss $d_{loss,5}$ at the state 5 is assumed 0.15 and the effective duty cycle $d_{e,max} = d_{max} - d_{loss,5} = 0.33$. The primary inductance $L_r$ is obtained from (6) and (11).

$$L_r = \eta V_{in,min}^2 d_{loss,5} d_{e,max} T_{sw} / 4 P_o \approx 1.6 \mu H$$

(12)

The turn-ratio $n_L$ can be expected in Equation (13).

$$n_L = d_{e,max} V_{in,min} / V_o \approx 2.2$$

(13)

In the presented circuit, the turns-ratio of transformer $T$ are $n_L = 2$, $n_M = 4$ and $n_H = 8$, with the primary-side turns $n_p = 16$, the secondary-side turns $n_s1 = n_s2 = 2$ and $n_s3 = 4$ and the magnetizing inductance $L_m = 650 \mu H$. For low voltage range, the minimum effective duty cycle $d_{e,min}$ under the maximum input voltage 180 V is calculated as.

$$d_{e,min} = d_{e,max} V_{in,L,max} / V_{in,L,max} \approx 0.147$$

(14)

If the ripple current $\Delta i_{L,o}$ is assumed 30% of $I_o,max$ under $V_{in,L,max} = 180 \text{V}$ (low input voltage range). The output filter inductance $L_o$ can be derived in Equation (15).

$$L_o = d_{e,min} T_{sw} (V_{in,L,max} / n_L - V_o) / \Delta i_{L,o} \approx 8.2 \mu H$$

(15)

The actual output inductance $L_o = 8 \mu H$ is used in the presented circuit. Under the minimum input voltage, the switches $S_1 \sim S_4$ have the maximum current stress. The switch root-mean-square ($rms$) currents are approximated in Equation (16).

$$i_{S1,min} = \ldots = i_{S4,min} = I_{o,\text{rated}} / (n_L \eta \sqrt{2}) \approx 9.8A$$

(16)
The voltage rating of active devices $S_1 \sim S_4$ is $V_{in, max}/2 = 400$ V. The MOSFETs IPW60R070P6 (650V/33A) are used for switch $S_1 \sim S_4$ and $Q_1 \sim Q_3$. The average diode currents $i_{D1, av} \sim i_{D6, av}$ are $I_{o, rated}/2 = 12.5$ A. The maximum voltage stress of $D_1 \sim D_6$ are approximately $V_{in, max}/n_L = 800 V/2 = 400$ V. The ultrafast recovery diodes APT30DQ60BG (600 V/30 A) are adopted for diodes $D_1 \sim D_6$. The other passive components in the prototype circuit are $C_o = 470 \mu F/35$ V, $C_1 = C_2 = 150 \mu F/450$ V, $C_f = 1 \mu F/630$ V, and $D_4$ and $D_6$ are DSEI30-12A with 1200 V/26 A voltage/current stress. The control block of the proposed circuit is given in Figure 5. Two Schmitt comparators and logic gates are adopted to determine three input voltage ranges by using the switching status of $Q_1 \sim Q_3$. The phase-shift PWM control integrated circuit UCC3895 is adopted for producing the PWM signals of $S_1 \sim S_4$. The voltage regulator TL431 and optocoupler PC817 are adopted to control the load voltage. The type 3 voltage control [29] with two zeros and three poles are used to have the enough phase margin at crossover frequency at 8 kHz.

5. Experimental Results

The test results that are based on the circuit components are shown in Table 1 derived in the previous section are demonstrated to confirm the circuit performance. Figures 6–8 show the test waveforms of the presented circuit under low, medium, and high input voltage ranges, and the rated output power. Figure 6a provides the measured PWM waveforms of switches $S_1 \sim S_4$ under $V_{in} = 80$ V and the rated output power 300 W. Figure 6b provides the PWM signals of switches $Q_1 \sim Q_3$ on the secondary-side. Switch $Q_3$ is on and $Q_1$ and $Q_2$ are off due to the $V_{in} = 80$ V being in the low voltage range. Figure 6c,d provide the measured main currents on the input and output sides. It can observe that the diodes $D_5$ and $D_6$ are conducting due to $Q_3$ is in the on-state. The currents $i_{D1} \sim i_{D4}$ are all zero due to $Q_1$ and $Q_2$ are off. Figure 6e–h provide the experimental waveforms of the presented circuit under $V_{in} = 175$ V and $P_o = 300$ W. Figure 6e gives the PWM signals of $S_1 \sim S_4$. $Q_1$ and $Q_2$ are off and $Q_3$ is on as shown in Figure 6f due to $V_{in} = 175$ V is in the low voltage range. Figure 6g,h present the main currents on the input and output sides. From Figure 6c,g, the ripple current $\Delta i_{L,o}$ at 80 V input voltage is less than the ripple current $\Delta i_{L,o}$ at 175 V input voltage due to the duty cycle of the converter leg voltage at $V_{in} = 80$ V case is larger than the duty cycle at $V_{in} = 175$ V condition. The measured waveforms in Figure 6 are almost conformed with the theoretical waveforms in Figure 2 under low input voltage range. Figure 7 presents the test results of the presented circuit under the medium input voltage range ($V_{in} = 140$ V $\sim$ 340 V) and the rated output power. Figure 7a–d gives the experimental waveforms at $V_{in} = 145$ V and $P_o = 300$ W. Figure 7a,b demonstrate the PWM waveforms of switches $S_1 \sim S_4$ and $Q_1 \sim Q_3$. $Q_1$ and $Q_3$ are off and $Q_2$ is on due to the medium input voltage range operation (Figure 7b). Figure 7c,d provide the main currents on the input and output sides. Diodes $D_3$ and $D_4$ are conducted in the medium input voltage range and $D_1$, $D_2$, $D_5$, and $D_6$ are off. Similarly, Figure 7e–h provide the test results of the presented circuit under $V_{in} = 335$ V and $P_o = 300$ W. It is clear that the ripple current $\Delta i_{L,o}$ at $V_{in} = 145$ V (Figure 7c) is less than the ripple current $\Delta i_{L,o}$ at $V_{in} = 335$ V (Figure 7g). Figure 8 gives the test results of the proposed circuit under high input voltage range ($V_{in} = 300$ V $\sim$ 800 V) and the rated output power. Figure 8a–d provide the measured waveforms at $V_{in} = 305$ V and $P_o = 300$ W. Figure 8e–h demonstrate the test results at $V_{in} = 800$ V and $P_o = 300$ W. For high input voltage range, switch $Q_2$ is on and $Q_2$ and $Q_3$ are off (Figure 8b,f). Therefore, diodes $D_3 \sim D_6$ are off (Figure 8d,h). Figure 8a,e show the PWM waveforms of $S_1 \sim S_4$ for $V_{in} = 305$ V and 800 V, respectively. Figure 8c,g provide the measured currents $i_{L,r}$, $i_{D1}$, $i_{D2}$ and $i_{L,o}$ for $V_{in} = 305$ V and 800 V, respectively. Figure 9 shows the test results of $S_1$ (the leading-leg switch) at $V_{in} = 80$ V, 400 V and 800 V conditions. Figure 9a,b show the measured results of $S_1$ at 20% and 100% loads under $V_{in} = 80$ V input. The drain voltage $v_{S1, d}$ is reduced to zero voltage before $S_1$ is turned on. Similarly, Figure 9c,d provide the measured waveforms of $S_1$ at 20% and 100% loads under $V_{in} = 400$ V input. Figure 9e,f demonstrate the measured waveforms of $S_1$ at 20% and 100% loads under $V_{in} = 800$ V input, respectively. The other leading-leg switch $S_4$ has the same turn-on/turn-off characteristics as switch $S_1$. From the experimental waveforms in Figure 9, the leading-leg switches $S_1$
and $S_4$ can turn on at ZVS from 20% to 100% rated load. Figure 10 provides the experimental results of the lagging-leg switch $S_2$ at $V_{in} = 80\,\text{V}, 400\,\text{V},$ and $800\,\text{V}$. Figure 10a,b show the test results of $S_2$ for 20% and 50% rated power under 80V input case. It can be observed that $S_2$ is turned on at hard switching operation at 20% load (Figure 10a) and soft switching operation at 50% load (Figure 10b). Figure 10c,d provide the test results of $S_2$ for $V_{in} = 400\,\text{V}$ and $800\,\text{V}$, respectively, under the rated power. From the experimental waveforms that are shown in Figure 10, the lagging-leg switches $S_1$ and $S_2$ are almost turned on at hard switching operation. Figure 11 gives the measured converter efficiencies under different voltage ranges. Basically, the converter has larger duty cycle at the low input voltage in each voltage range. The larger duty cycle will result in less root mean square current on the primary-side and less conduction losses. The circuit efficiency at $V_{in} = 80\,\text{V}$ is better than the circuit efficiency at $V_{in} = 175\,\text{V}$ under a low input voltage range. Similarly, the circuit efficiency at $V_{in} = 305\,\text{V}$ is better than the circuit efficiency at $V_{in} = 800\,\text{V}$ under high input voltage range operation. The circuit efficiency under the high input voltage range is better than the low input voltage range since the presented circuit has larger the primary-side current under low input voltage range. The synchronous rectifiers with low turn-on resistance instead of rectifier diodes can be adopted on the secondary side to reduce the conduction losses in order to increase the circuit efficiency. The Litz wire [30] can be adopted to avoid the skin effect on winding resistance to reduce the copper losses on transformer and output inductor.

The more power loss analysis of power semiconductors, inductors, transformers, and capacitors on power converters has been discussed in [31].

### Table 1. Prototype Circuit Parameters.

| Items                        | Symbol | Parameter       |
|------------------------------|--------|-----------------|
| Input voltage                | $V_{in}$ | 80 V ~ 800 V |
| Output voltage               | $V_o$  | 12 V           |
| Rated output current         | $I_o$  | 25 A           |
| Switching frequency          | $f_{sw}$ | 150 kHz       |
| Input capacitors             | $C_1$, $C_2$ | 150 $\mu$F/450 V |
| Voltage balance capacitor    | $C_f$  | 1 $\mu$F/630 V |
| Power switches               | $S_1 ~ S_4$, $Q_1 ~ Q_3$ | IPW60R070P6 |
| Rectifier diodes             | $D_1 ~ D_6$ | APT30DQ60BG |
| Clamp diodes                 | $D_a$, $D_b$ | DSEI30-12A |
| Winding turns of $T$         | $n_{p}$, $n_{s1}$, $n_{s2}$, $n_{s3}$ | 16, 2, 2, 4 |
| Magnetizing inductance       | $L_r$  | 1.6 $\mu$H    |
| Output inductance            | $L_o$  | 8 $\mu$H      |
| Output capacitance           | $C_o$  | 470 $\mu$F/35 V |
transformers, and capacitors on power converters has been discussed in [31].

The more power loss analysis of power semiconductors, inductors, wire [30] can be adopted to avoid the skin effect on winding resistance to reduce the copper losses on

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**Figure 6.** Experimental waveforms at the rated output power and low input voltage range.

(a) primary-side switch waveforms \( v_{S1,g} \sim v_{S4,g} \) under \( V_{in} = 80 \) V (b) secondary-side switch waveforms \( v_{Q1,g} \sim v_{Q3,g} \) under \( V_{in} = 80 \) V (c) \( i_{Lr}, i_{D5}, i_{D6}, \) and \( i_{Lo} \) under \( V_{in} = 80 \) V (d) \( i_{D1} \sim i_{D4} \) under \( V_{in} = 80 \) V (e) primary-side switch waveforms \( v_{S1,g} \sim v_{S4,g} \) under \( V_{in} = 175 \) V (f) secondary-side switch waveforms \( v_{Q1,g} \sim v_{Q3,g} \) under \( V_{in} = 175 \) V (g) \( i_{Lr}, i_{D5}, i_{D6}, \) and \( i_{Lo} \) under \( V_{in} = 175 \) V (h) \( i_{D1} \sim i_{D4} \) under \( V_{in} = 175 \) V.
Figure 7. Experimental waveforms at the rated output power and medium input voltage range
(a) primary-side switch waveforms $v_{S1,s} \sim v_{S4,s}$ under $V_{in} = 145$ V (b) secondary-side switch waveforms $v_{Q1,g} \sim v_{Q3,g}$ under $V_{in} = 145$ V (c) $i_{Lr}, i_{D3}, i_{D4}$, and $i_{Lo}$ under $V_{in} = 145$ V (d) $i_{D1}, i_{D2}, i_{D5}$, and $i_{D6}$ under $V_{in} = 145$ V (e) primary-side switch waveforms $v_{S1,s} \sim v_{S4,s}$ under $V_{in} = 335$ V (f) secondary-side switch waveforms $v_{Q1,g} \sim v_{Q3,g}$ under $V_{in} = 335$ V (g) $i_{Lr}, i_{D3}, i_{D4}$, and $i_{Lo}$ under $V_{in} = 335$ V (h) $i_{D1}, i_{D2}, i_{D5}$, and $i_{D6}$ under $V_{in} = 335$ V.
Figure 8. Experimental waveforms at the rated output power and high input voltage range (a) primary-side switch waveforms $v_{S1,g}$ ~ $v_{S4,g}$ under $V_{in} = 305$ V (b) secondary-side switch waveforms $v_{Q1,g}$ ~ $v_{Q3,g}$ under $V_{in} = 305$ V (c) $i_{D1}$, $i_{D2}$, and $i_{Lo}$ under $V_{in} = 305$ V (d) $i_{D3}$ ~ $i_{D6}$ under $V_{in} = 305$ V (e) primary-side switch waveforms $v_{S1,g}$ ~ $v_{S4,g}$ under $V_{in} = 800$ V (f) secondary-side switch waveforms $v_{Q1,g}$ ~ $v_{Q3,g}$ under $V_{in} = 800$ V (g) $i_{Lr}$, $i_{D1}$, $i_{D2}$, and $i_{Lo}$ under $V_{in} = 800$ V (h) $i_{D3}$ ~ $i_{D6}$ under $V_{in} = 800$ V.
Figure 9. Measured results of the leading-leg switch $S_1$ at: (a) $V_{in} = 80$ V and 20% load; (b) $V_{in} = 80$ V and full load; (c) $V_{in} = 400$ V and 20% load; (d) $V_{in} = 400$ V and full load; (e) $V_{in} = 800$ V and 20% load; and, (f) $V_{in} = 800$ V and full load.

Figure 10. Cont.
winding turns connected to output side. The PWM scheme is adopted to control the load voltage in
voltage ranges to supply the stable DC voltage at the output load due to three di... operated at hard switching operation due to the limited energy stored on the leakage inductor of
solar intensity in day and night. The conventional two-level or three-level converter cannot be
solar intensity in day and night. The conventional two-level or three-level converter cannot be

Figure 10. Measured results of the lagging-leg switch $S_2$ at: (a) $V_{in} = 80$ V and 20% load; (b) $V_{in} = 80$ V
and 50% load; (c) $V_{in} = 400$ V and full load; and, (d) $V_{in} = 800$ V and full load.

Figure 11. Measured circuit efficiencies under: (a) low input voltage range; (b) medium input voltage
range; and, (c) high input voltage range.

6. Conclusions

In solar power system, the input voltage from solar panel is wide variation due to the different
solar intensity in day and night. The conventional two-level or three-level converter cannot be operated
under wide voltage operation. In this paper, a three-level diode-clamped DC/DC converter with three
auxiliary secondary turns is presented and then discussed to provide the capability of 10:1 wide voltage
range operation for solar power converters to supply the isolated power supply for control board
demand. Three sets of secondary windings are adopted in the presented circuit to overcome the wide
input voltage variation in solar power converters. The proposed converter can operate at three input
voltage ranges to supply the stable DC voltage at the output load due to three different secondary
winding turns connected to output side. The PWM scheme is adopted to control the load voltage in
each input voltage range. The leading-leg switches in the three-level converter can be realized with
ZVS operation due to the large inductor energy on the output inductor. The lagging-leg switches are
almost operated at hard switching operation due to the limited energy stored on the leakage inductor of
transformer. The large leakage inductor or external inductor can be used on the input side to overcome this disadvantage. However, the large leakage inductor will increase the duty cycle loss in state 5. The future work of this project will investigate the new snubber circuit or auxiliary circuit added on the output side to lessen the freewheel current. Thus, the duty cycle loss can be expected to reduce and the soft switching operation range of the lagging-leg switches can be extended. The proposed converter can be used in the solar power system with wide input voltage variation from solar panel to provide the standalone power unit for control system demand. Finally, the test results prove the performance and feasibility of the presented circuit.

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