An all-digital phase-locked loop demodulator based on FPGA

X F Gong, Z D Cui

1 School of Mechanical Engineering, University of Science & Technology Beijing, NO.30, College Road, HaiDian District, Beijing, China
2532542664@qq.com

Abstract. This paper studied the principle of analogue phase-locked loop demodulation and work process of digital phase-locked loop. It is found that the higher the reference signal frequency is, the smaller the duty ratio of the discriminator output signal is. Carrier detection is achieved by using this relationship. The experimental results indicate that the demodulator based on the principle could realize high-quality transmission of digital signals and could be an effective FM communication mode for studying wireless transmission of digital signals.

1. Introduction
The phase-locked loop (PLL) possesses a wide range of applications in modern communication systems. The all-digital phase-locked loop (ADPLL) has been widely used in digital communication and automatic control field because of the advantages of stable performance, reliable operation and so on. With the development of digital signal processing technology and programmable devices, the on-chip realization of all-digital phase-locked loop has become a hot topic

In the communication system, FSK modulation method is easy to achieve, anti-noise and anti-attenuation performance is better, so it has been more widely used in the field of information transmission. When the central frequency of the ADPLL is fixed, the FSK modulation signal enters the ADPLL as an input signal, and the output of the phase detector reflects the information of the modulation signal. Then the demodulation process is completed. In this paper, the Verilog hardware description language is used to build the system, and the programmable gate array FPGA is used as the experimental platform to realize the good demodulation effect and has high engineering application value.

2. ADPLL demodulation
Phase-locked loop demodulation is known from the traditional demodulation mode. As a new demodulation method, it avoids the large number of multiplication integral operations in traditional demodulation method, which consume a large amount of digital signal processor resources. The control process is implemented as a counter and avoids the effects of system perturbations.

In addition, all-digital signal processing eliminates the impact of the environment on components, improves signal processing accuracy while simplifying the design of the system.

2.1. Digital signal modulation
The system used binary frequency shift keying (2FSK) modulation which modulate the carrier frequency according to the baseband signal. The signals used in this paper are digital signals, so it is easy to use the form of frequency control word to produce phase continuous modulation signal.
expression of the frequency control word is shown in $N = \frac{f_o}{f_r}$. The value of frequency control word responds to the required frequency \[^3\].

2.2. PLL demodulation

In the analog phase-locked loop demodulator, the FM wave is amplified by the amplifier and the output of the voltage-controlled oscillator is sent to the phase detector. The output of the phase detector reflects the phase error information of the two input signals. Then the obtained voltage signal passed loop filter changes with the change of the modulation signal frequency so as to realize the mediation process. The demodulation block diagram is shown in Figure 1.

\[ N = \frac{f_o}{f_r} \]

**Figure 1.** Analog PLL demodulator.

By the characteristics of phase detector, the average value of phase detector output signal can be described as $u_j(t) = K_d \sin(\theta_j)$, $K_d$ represents the gain of the phase detector, and $\theta_j$ represents the phase error of the input signals of phase detector. In order to demodulate FSK signal, the bandwidth of loop filter in the circuit should be wide enough so that all the components of the phase detector output voltage (high frequency and DC component) are able to be outputted. The instantaneous frequency of VCO reflects the change of the input FSK signal; the VCO input voltage reflects the modulation information of FSK signal.

2.3. ADPLL demodulation process

The main parts of the demodulator include not only ADPLL but also the div-phase and detect-module module, which are used to detect the effective input signal, control phase adjustment, and detect phase locking state and so on. The block diagram is shown in Figure 2\[^4\].

**Figure 2.** ADPLL demodulator.

In practical application, the data transmission is not continuous. In the absence of data transmission, the output frequency of ADPLL is center frequency. When there is data to be transmitted, the reference frequency changes. Aiming to achieve that the output frequency of ADPLL tracks reference frequency, the phase adjustment module is used to detected the jump of reference signal and the ADPLL state (whether locked). If the ADPLL is in unlocked state, the div-phase module outputs phase adjustment signal. When the frequency division counter receives the phase adjustment signal, the initial value of the id counter is adjusted immediately so that the output signal can quickly keep up with the frequency of the reference signal.
The key of this paper is shown in Figure 3, it describes three situations: $\theta > 0$, $\theta < 0$ and there is no input signal. When an input signal is present, before the divide _n_sig jump edge, exor _sig keeps low level; when there is no reference signal input, before the divide _n_sig jump edge, the probability of exor _sig at the high and low levels is equal. So we can judge whether there is FM wave signal inputting system according to the above characteristics.

On the other hand, by the demodulation process of analog PLL, the input signal of the VCO reflects the variation of the FSK signal. Similarly, as the Figure 3 shows, the duty ratio of exor _sig reflects the carrier signal information. For example, in the case of $\theta > 0$, it indicates that the frequency of reference signal is greater than center frequency of system which represents that input carrier is a high frequency. On the contrary, in the case of $\theta < 0$, input carrier is a low frequency. In the two cases, the duty ratio of exor _sig is obviously different. After the duty ratio counted, binary data is demodulated according to the designed judge threshold.

In this paper, the 2FSK modulation is adopted. In the engineering application, the system can also implement the MSK modulation method. Equally, the demodulation process is completed according to the output signal of the phase detector.

3. System simulation and experimental verification
Before the experiment verification, ModelSim can be used for timing simulation of the system to verify the correctness of the design. The test result is shown in the Figure 4.

As can be seen from the Figure 4, the relationship of reference _sig, divide _n_sig and exor _sig conforms to the analysis of Figure 3. According to this relationship, it is possible to demodulate the corresponding transmitted data information.
This experiment selects the Cyclone IV series FPGA chip EP4CE6E22I7 of Altera Company to build the experimental platform. After the program timing constraints and pin configuration, the project is downloaded to the chip for hardware verification. Two same pieces of demodulate boards will be used in the experiment. The result of experiment is realizing the asynchronous communication between the host computer and the slave computer[5].

References
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