Influence of Reactive Ion Etching Time on Fabrication of Porous Silicon on Si (110) Substrates

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Abstract. Porous silicon (PSi) has been fabricated by photolithography and Reactive Ion Etching (RIE) with various etching times in the previous study. The PSi surfaces have the pore size in the range of 12.6-28.0 nm for PSi (111) and 17.4-37.7 nm for PSi (100). Meanwhile, the PSi has the resistivity around (1.14-2.60)×10⁻⁴ Ω.cm for PSi (111) and (3.85-9.03)×10⁻⁴ Ω.cm for PSi (100). In this study, N-type Si (110) substrate was used to form PSi with various etching times for 10, 20 and 40 min. The PSi samples were characterized by SEM, Dektak XT profilometer, UV-Vis and FPP equipment. PSi formed into a spherical shape which distributed throughout the Si surface. Pore sizes, pore depths and resistivity of patterned PSi increased as the etching time increases, i.e., 4.04 µm, 30.85 nm and 2.26×10⁻⁴ Ω.cm (10 min); 4.98 µm, 51.93 nm and 3.86×10⁻⁴ Ω.cm (20 min); 6.00 µm, 80.67 nm and 5.77×10⁻⁴ Ω.cm (40 min), respectively. This indicated that the pores could be considered as defects or dislocation inside material which resist electrons diffuse toward the electrode. Moreover, the PSi reflectance value decreases 30% to around 10% on the visible light range with the increasing of etching time.

1. Introduction
Porous silicon (PSi) work in electronics and optical devices increases from annual to annual [1-6], thanks to its excellent physical, chemical and optical properties. For more than a decade, the solar PSi-based photovoltaic was built [7, 8]. In order to enhance the photovoltaic performance, the surface reflection should be diminished. In order to minimize reflection by up to 5 percent in the wavelength range from 400 to 1000 nm, Kwon et al.[7] developed porous silicon on a contoured Si substrate minus further anti-reflection covering films. Macro-porous silicon-based dye-sensitized solar cell (DSSC) was improved by Aliaghayee et al., [8, 9]. As a DSSC photo-anodic, macro-PSi was used to increase the photon trapped. The performance of power conversion improved from 50 percent to 75 percent associated to traditional DSSC. It has been reached the conclusion that the PSI take place as light capture surface and dye load capability. Nonetheless, in an industrial world, there are certain irregular porous drawbacks which are hard to replicate.

The previous research, PSI was manufactured on Si(100) and Si(111) surfaces with photolithographs and reactive ion etching (RIE) [10, 11]. The modulating of an integrated silicon circuit, which allows good regulation of morphological characteristics including homogenous sizes
and shapes, porosity and pores width, has become well-known [12]. For PSi (111) and PSi (100), the PSi surfaces were of uniform pore dimensions ranging from 12.6-28.0 nm and 17.4-37.7 nm, respectively. In the meantime, PSi has the following resistance (1.14-2.60)×10⁻⁴ Ω.cm for PSi (111) and (3.85-9.03)×10⁻⁴ Ω.cm for PSi (100). This research uses the similar approach and the difference in substrate orientation to create regular PSi. The PSi obtained is identified by using Scanning Electron Microscopy (SEM) to perceive morphology of pores on silicon surfaces, Dektak XT profilometer for measuring pores size, Four Points Probe (FPP) for calculating the resistivity in electrical properties and Spectrophotometer UV-Vis to measure PSi reflectance in terms of optical properties.

2. Experimental
The Si (110) 3° n-type was used as a substrate with resistivity 0.1-10 Ω.cm. The sample was placed on a holder in the spin coater. The Z-P-N solution was deposited on the Si(110) as a negative photoresist, which was then spinning at 500-5000 rpm for 33s. Around 90 °C for 90 s, samples were pre-baked. The sample was subjected to UV light for 8 s under a 5 / 5 μm photo-mask in a photolithographic system. The sample was rotated by at 90 ° and exposed again to UV light during 8s. In other samples, identical procedures have been performed. The samples were after treatment for 1 min at about 100 °C and afterward submerged in the developers solution. A digital microscope was able to detect the surface area covered by photoresist or not. The next step was the etching process for shaping pores by means of the RIE technique. CF4 gas was flown into a 10-watt radio frequency chamber. CF4 gasses produce F * radical ions that etch the surface of Si. The period for etching was varied by 10 min, 20 min and 40 min. The samples were eventually washed with boiled solution H2O2: H2SO4 and dried with nitrogen gas. Such samples were analysed using SEM, Dektak profilometer, FPP, and UV-Vis spectrophotometer.

3. Results and discussion
A image of Si(110) surfaces is shown in Figure 1. The surface color shows that the surface has developed porous. PSi can radiate visible photo luminescent at about 27 °C (RT) [13].

![Figure 1. Photograph of PSi on Si (110) surface](image_url)
μm and 6.00 μm for etching time of 10 min, 20 min and 40 min, respectively. It means that depth of the pores increases as the etching period increases as shown in Table 1.

![SEM images of PSi etched by RIE method at various times](image)

**Figure 2.** SEM images of PSi etched by RIE method at various times for (a) 10 min, (b) 20 min and (c) 40 min

The RIE sequential process consists of one etching and two passivation sequences, i.e. oxidation and fluorination [15]. The mechanism of pores formation can be described as follows: The patterned Si was positioned in the RIE compartment with the cathode on a sample holder. The CF4 gas was flown into the RIE compartment, then the RF power will disturb it, thus dissociating it into CF3 gas, F * ions, and electrons. Such electrons were oscillating and colliding with other gas molecules, creating reactive ions of F *. The silicon bonds (Si-Si) were bombarded by F * ions or negative ions on the Si surface till bonding separated, and F * ions acted to Si bonds. As a consequence, the surface of Si becomes damaged and occurs formation of pores [16]. This cycle remains for period of etching that was set for 10 min, 20 min and 40 min. Therefore, depth of the pore can be measured depending on the duration of the etching period.

| Etching time (min) | Pore depth (nm) | Pore diameter (µm) | Resistivity \( \times 10^{-4} \Omega \text{cm} \) |
|--------------------|----------------|--------------------|---------------------------------|
| 10                 | 30.85          | 4.04               | 2.26                            |
| 20                 | 52.93          | 4.98               | 3.86                            |
| 40                 | 80.67          | 6.00               | 5.77                            |

The resistance value is derived from the measurement of the Four Point Probe and is used for calculating the resistivity of PSi for every etching period. Earlier research demonstrated the method for obtaining PSi resistivity [11]. Table 1 shows the PSi resistivity for 10 min, 20 min, and 40 min at etching time. With increased etching time, the resistivity increases. The resistance for each semiconductor material is well known to be constant. A potential difference between two electrodes occurs as a current flows through a semiconductor material. Current increases cause a potential difference to increase so the resistance remains constant. Furthermore, because of the resistivity that is directly proportional to the resistance [17], PSi's resistivity increases with PSi's resistance increasing. In addition, The depth and diameter of the pore on the Si surface will estimate resistivity to PSi. From the relationship in Table 1, it can be defined that both the resistivity and the pore depth value rise with the increase of the etching period. Hence, resistivity also increases as the depth of the pore increases. The presence of a defect within the structure of the semiconductors raises the resistivity value [18]. The pore is thus called a defect in this study, so that it is constraint for the electron to migrate across the surface of silicon.
Figure 3. Reflectance spectra of PSi with various etching times

Figure 3 displays the PSi reflectivity spectra with different etching times. With rising etching time, the PSi reflectance value decreases on the visible light spectrum from 30 percent to around 10 percent. Such modification thus signifies that the more photons will be absorbed the lowest PSi reflectance value accordingly. Coyopol, et al.[19] clarified that the reflectance spectra is important for its potential use as an anti-reflective coating in solar cells. Hence, PSi can be used to enhance solar cell performance.

4. Conclusion
The pores on the n-type Si(110) were successfully manufactured for specific etching time using photolithography and RIE methods. For any etching time the pores are homogenous. The pore sizes, pore depths, and resistivity of patterned PSi increased with increasing etching time. This suggested that the pores can be viewed as cracks or dislocations inside material that prevent diffuse electrons towards the electrode. In addition, the PSi reflectance value on the visible light spectrum decreases from 30 percent to about 10 percent with increasing etching time. Hence, PSi can be used to increase solar cell performance.

Acknowledgments
Authors wish to thank Universitas Sebelas Maret 2019 for financial support through Collaboration International Grant with Contract No. 516/UN27.21/PP/2019. RS would like to thank Kashiwaya Laboratory, Department of Applied Physics, Graduate School of Engineering, Nagoya University, Japan for supporting SEM instrument.

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