Atom Chips: Fabrication and Thermal Properties

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Neutral atoms can be trapped and manipulated with surface mounted microscopic current carrying and charged structures. We present a lithographic fabrication process for such atom chips based on evaporated metal films. The size limit of this process is below 1µm. At room temperature, thin wires can carry more than 107 A/cm² current density and voltages of more than 500V. Extensive test measurements for different substrates and metal thicknesses (up to 5 µm) are compared to models for the heating characteristics of the microscopic wires. Among the materials tested, we find that Si is the best suited substrate for atom chips.

Manipulation of neutral atoms using micro-structured surfaces (atom chips) has attracted much attention in recent years [2]. Atom chips promise to combine the merits of microfabrication and integration technologies with the power of atomic physics and quantum optics for robust manipulation of atomic quantum systems. Extreme and precise confinement in traps with large level spacing is possible. Neutral atoms have been trapped by currents flowing in microscopic wires fabricated on the atom chip surface [2,3], manipulated by electric fields [4], and even cooled to Bose-Einstein condensates [5,6,7].

The demands on atom chips are high current densities to create steep traps, and small structure sizes to create complex potentials at a scale where tunneling and coupling between traps can become important. Exceptional high-quality fabrication is essential, since the smallest inhomogeneities in the bulk of the wire or the fabricated edges can lead to uncontrolled deviations of the current flow and therefore to disorder potentials in the magnetic guides and traps [8,9,10,11,12].

The fabrication process preferred by groups working in the field is to grow thick wires from a thin patterned layer using electroplating [13,14,15], which allow large currents for trapping and manipulating the atoms.

In contrast, we have chosen to directly pattern up to 5µm tall evaporated high-quality layers of gold using a photolithographic lift-off technique (Fig. 1). Wires are defined by thin gaps in the evaporated gold surface. These µm sized gaps only produce an insignificant amount of stray light when the gold surface is used as a (nearly perfect) mirror for laser cooling and atom imaging. This technique was preferred because it results in high surface quality and very smooth structure edges.

In our process, the substrate (Si or GaAs covered with a SiO₂ insulation layer or sapphire) is prepared with an adhesion primer. To allow the evaporation of thick metal layers, we spin up to 5µm thick films of image reversal photoresist (AZ 5214E) onto the sample at low speed. The resist is then exposed to UV-light through an e-beam patterned mask. After developing the resist structure (Fig. 1A), a Ti adhesion layer (35nm) and a thick Au layer (1–5µm) are evaporated at a short distance from the source at a rate of 5–40Å/s. To achieve good surface quality, care has to be taken in controlling the evaporation speed and substrate temperature. The gold covered resist structure is then removed in a lift-off procedure using acetone (if necessary in a warm ultrasonic bath) and isopropanol as solvents. A second gold layer can be added by repeating the above process. Some chips were covered with a thin protective insulation layer of Si₃N₄. Finally, the chips are cut or cleaved to the desired dimensions of 25 × 30mm².

The resulting gold surfaces (Fig. 1D) are smooth (grain sizes < 80nm), and the wire edges are clearly defined. The surface quality depends on adhesion properties and the substrate smoothness. Semiconductor substrates (Si and GaAs) gave better results than sapphire samples.

An important characteristic of atom chips is how much current and voltage the microscopic wires can carry. The achievable confinement of the atoms depends on the maximal potential gradient, which scales with the achievable current density j.

To evaluate the fabrication process and to collect comprehensive data for the operation of the atom chips and
FIG. 2: Temperature evolution of a 5\(\mu\)m wide, 1.4\(\mu\)m tall wire mounted on a 700\(\mu\)m thick Si substrate with a 500nm SiO\(_2\) isolation layer. The solid curves show measured data for 0.6A, 0.5A, and 0.3A current pulses. In one case (0.5A) also the theoretical predictions (without fitting parameters) are shown. The initial fast temperature increase (thin dashed-dotted curve) occurs on a \(\mu\)s timescale. The analytical model for the heat transport through the substrate (dotted curve) holds only as long as the approximation of a half space substrate is valid. A two-dimensional numerical model (dashed curve) accurately reproduces the measurements.

slow rise of temperature, which was observed over the full duration of the current pulses (up to 10s).

In order to gain insight into the relevant processes and parameters, we compared our data with a simple model for the heating of the substrate mounted wires. The heat created in a wire of height \(h\) and width \(w\) carrying a current density \(j = I/wh\) is given by ohmic dissipation. Essentially, the heat is removed through heat conduction to the substrate, as thermal radiation is negligible for the observed temperatures. The temperature evolution of the wire is determined by the heat flow through the interface, which exhibits a thermal contact resistance (thermal conductance \(k\)), and the heat dissipation within the substrate, governed by the heat conductivity \(\lambda\) and heat capacity (per volume) \(C\). This leads to two very different timescales for the heat removal:

The timescale of the first process (heat flow from the wire to the substrate through the isolation layer) is given by \(\tau_{fast} = \frac{CWh}{\alpha \rho}\), where \(C_W\) is the heat capacity (per volume) of the wire, \(\rho\) its (cold) resistivity with a linearly approximated temperature coefficient \(\alpha\). For typical parameters of our chips, this timescale (\(\sim 1\mu s\)) is so short that the temperature difference between the wire and the substrate saturates practically instantaneously, unless \(j\) exceeds the limit of \(\sqrt{k/\rho \alpha}\). In this case, an exponential rise of the temperature will lead to an almost instantaneous destruction of the wire.

Our model for the fast heating process quantitatively agrees with the data. While the initial temperature rise is independent of the wire width (Fig. 3A), it depends on the contact resistance to the substrate (Fig. 3B). The latter effect can clearly be seen by comparing the data for two Si substrates with different insulation layers. A 500nm thick SiO\(_2\) layer leads to stronger heating than a 20nm thick layer. In order to find the
The fitting is necessary, because optimal substrate, the values for the thermal conductivity $k$ were obtained from fitting the model to our data ($k = 6.5, 3.5, 2.6, 2.3 \times 10^6 \text{W/Km}^2$ for Si with 20nm SiO$_2$ sapphire, Si with 500nm SiO$_2$, and GaAs, respectively). The fitting is necessary, because $k$ includes the conductivity through the insulation layer and the contact resistances at the individual material interfaces. The best conductance was found for the Si substrate with the thin SiO$_2$ layer. The differences between the remaining data are mainly due to different wire heights. In our experiments Si substrates with thin isolation layers consistently exhibited the lowest fast heating of typically $\Delta T \sim 50 \text{K}$ corresponding to a $\sim 20\%$ resistance increase at $10^4 \text{A/cm}^2$.

In a two-dimensional model for the heat transport within the substrate, we assume a line-like heat source on the surface of a half space substrate. The temperature increase $\Delta T_s(t)$ at this point is then given by the incomplete $\Gamma$ function

$$\Delta T_s(t) = \frac{h w p j^2}{2\pi \lambda} \Gamma \left(0, \frac{C u^2}{4\pi^2 \lambda t} \right) \approx \frac{\rho I j}{2\pi \lambda} \ln \left( \frac{4\pi^2 \lambda t}{C u^2} \right)$$

Here, the (small) temperature dependence of the resistivity is neglected.

For this slow heating process, the total heat dissipation becomes important. Hence, wider wires heat up faster than narrow ones for equal current density (Eq. 2 and Fig. 3 B). In addition, the heat transport in Si is faster than in the other tested materials due to its larger heat conductivity ($\lambda_{\text{GaAs}} \approx \lambda_{\text{sapphire}} \approx 3.2 \mu\text{m}$). Fig. 4 shows that the thin wires ($1.4\mu\text{m}$) mounted on Si heat up significantly less than the taller wires ($\sim 3\mu\text{m}$) fabricated on sapphire or GaAs. In the latter case, the simple model underestimates the temperature rise for large power dissipation as predicted by the numerical heat equation integration. The analytical model is only as long as the substrate can be treated as a heat sink. For a thin substrate (typically 700μm) the heat transport out of the substrate has to be taken into account for longer times (typically after a few 100ms). Then a two-dimensional numerical calculation accurately reproduces the data (Fig. 3).

To conclude, we have presented a method for fabricating atom chips with a lithographic lift-off process. With this process we produced wires that can tolerate high current densities of $>10^4 \text{A/cm}^2$. We have shown that the temperature evolution of surface mounted microwires agrees with a simple dissipation model. The optimal substrate has a large heat conductivity and capacity and is in good thermal contact with the wire. Si substrates with thin oxide layers showed the best thermal properties of the examined samples as well as good surface qualities. The described fabrication process leads to very accurate edge and bulk features. As a result, the disorder potentials have been observed to be sufficiently small not to fragment a cold thermal atomic cloud ($T = 1\mu\text{K}$) at a distance of $<5\mu\text{m}$ from the wire.

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