RF Waveguide Pattern Engineering to Mitigate Bonding Surface Nonuniformities in CMOS Compatible Fabrication Processes

Nicholas A. Boynton, Forrest G. Valdez, Thomas A. Friedmann, Shawn C. Arterburn, Christina M. Dallo, Andrew T. Pomerene, Andrew L. Starbuck, Douglas C. Trotter, Michael R. Gehl, Christopher T. DeRose, Shayan Mookherjea, Senior Member, IEEE, and Anthony L. Lentine

Abstract—Heterogeneously integrating silicon photonic devices and circuits with other optical materials (III/V semiconductors, LiNbO3, and so on) is a promising approach toward bolstering the capabilities of silicon photonics and improving the manufacturability of other photonic platforms. An approach to heterogeneous integration is to directly bond an optical material to the surface oxide of a silicon photonic circuit or device, which requires locally and globally smooth bonding surfaces to facilitate sufficient bonding quality. However, embedded silicon photonic metal structures, such as RF waveguides for high-speed photonic devices and electrical interconnects, can impact the surface topography during planarization, resulting in nonideal bonding surfaces. In this article, we discuss and demonstrate a method of patterning the ground planes of RF waveguides to achieve a more uniform distribution of embedded metal density, in turn, providing more constant planarization rates. This provides a more uniform bonding surface which is a requirement for the high-volume manufacturing of these technologies.

Index Terms—Bonding, heterogeneous integration.

I. INTRODUCTION

SILICON photonics (SiP) is an enabling technology for dense optical networks which relies on the mature manufacturing environment used to build CMOS electronics. However, the indirect bandgap of silicon makes the fabrication of semiconductor lasers on this platform nontrivial, and the centrosymmetric nature of silicon prohibits its use as a linear electrooptic material. Typically integrated lasers are fabricated using III/V compound semiconductors, and linear modulators are fabricated using noncentrosymmetric materials, such as lithium niobate (LiNbO3), but neither of these platforms has the mature process development SiP features.

An attractive approach to utilizing the benefits of SiP while simultaneously using materials to realize high-performance, high-speed, efficient photonic devices, and systems is heterogeneous integration [1], [2], [3]. This approach offers all the manufacturing benefits of SiP and removes the manufacturing emphasis from other materials by fabricating the optical waveguides, RF waveguides, and high-speed electrical interconnects in the CMOS foundry. In this architecture, the optical waveguides defined in the CMOS foundry must be spatially near the other integrated material in order to allow optical interaction with those materials. Heterogeneous integration can be achieved through the application of adhesives, such as benzocyclobutene (BCB); however, this generally increases the distance between the lithographically formed waveguides and bonded photonic material [4], which can reduce the amount of optical interaction with the bonded materials.

To ensure that the lithographically defined waveguide cores are as close to the integrated material as possible, there should be a minimal amount of oxide between the bonded layer and the waveguide strip. For this reason, direct bonding is the preferred method of integration, which relies on van der Waals forces. The minimum distance between these layers is desirable as this forms a more well-defined waveguide and ensures the mode has maximum overlap with the integrated optical material while also remaining guided. For successful and strong oxide bonding (using van der Waals forces), the two surfaces must be smooth (typically having a root mean square (RMS) roughness of less than one nanometer) and globally flat. These requirements ensure that there are no voids in the bond and that large pieces of material can be bonded for large photonic integrated circuits (PICs) or wafer-scale bonding. Minimum material above the SiP waveguides and sufficient global flatness is achieved inside of the CMOS foundry through the implementation of a chemical–mechanical planarization (CMP) step, in which the planarized SiO2 becomes the bonding surface of the SiP sample.

Heterogeneous integration has been applied between thin-film lithium niobate (TFLN) and SiP to produce high-speed linear electrooptic modulators [5], [6], [7], [8], [9]
and nonlinear optics (NLO) applications, such as wavelength conversion devices [10], [11], [12], [13]. This integrated platform may additionally be expanded to include quantum photonic devices [14], [15], [16]. Heterogeneous integration has also been pursued as a method to bring lasers to SiP through bonding of III/V to SiP waveguides [17], [18], [19], [20]. Other devices that have been demonstrated through bonding with SiP are optical amplifiers [21], photodiodes [22], and magnetooptic isolators [23].

RF waveguides, such as coplanar waveguides (CPWs) are required for high-speed elements in modulation devices and as electrical interconnects between components. In general, CPWs are highly suitable for integrated high-speed devices because they only require a single-metal layer and are required in order to realize any type of high-speed operation. Typical integrated CPWs consist of two ground planes and a center electrode, as depicted in Fig. 1, and result in very dense metal regions in the final PIC.

After polishing, there should be as little variation in SiO₂ thickness as possible throughout the PIC. It can be difficult to achieve planarity and avoid bowing and dishing when a multi-layer wafer that contains metal electrodes undergoes CMP in preparation for bonding.

Conventional high-speed electrode designs can range up to several millimeters, and result in abrupt discontinuities in localized metal density at the boundary between electrodes and other areas of the chip, which contain “fill” or “dummy” metal patterns. These “fill” cells are used primarily to realize smooth, planar surfaces after CMP steps [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], but also are used to meet optimal minimum metal densities to achieve uniform metal etching. The minimum density requirement will vary with every process but is typically between 15% and 25% [37].

It has been shown that significant polishing SiO₂ variations can occur during the CMP process when the metal structures below the polished surface have varying localized density [5], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], which does not provide a flat bonding surface, limits the bonding area, and reduces the overall yield of bonded device fabrication.

In this article, we address the effect of nonuniform planarization during the CMP step [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39] as it relates to the underlying metal pattern density. Aluminum CPW devices are fabricated and characterized using Sandia’s SiP process with both solid and patterned ground planes. We show that the implementation of large metal regions in a chip will result in a systematic variation in the thickness of the planarized SiO₂, which limits the size of the bonding area. We also discuss and implement a mitigation method for this thickness variation by engineering the metal density in our samples. We experimentally show that this has virtually no impact on CPW operation and performance up to 40 GHz and show that this design methodology can be used to improve the global surface uniformity of the bonding surfaces in heterogeneously integrated photonic platforms. These techniques are applicable broadly in both electronics and photonics where globally smooth surfaces are required. CPW performance is explored up to 100 GHz in a simulation where a very slight difference in the loss characteristics is observed.

II. EXPERIMENT AND RESULTS

Two CPW designs, which are depicted schematically in Fig. 2, are fabricated using Sandia’s CMOS fabrication facilities, whose design parameters are listed in Table I. These CPWs consist of the 0.87-μm-thick aluminum layer with a dc sheet resistance of 42 mΩ/sq. The aluminum layer is fabricated above a 3-μm-thick layer of thermally grown oxide. Both of the CPW designs are fabricated with two
different lengths (0.52 and 1.02 cm) using both a standard, solid ground plane design and a patterned ground plane design. The silicon handle resistivity for the CPWs with solid ground plane designs is specified to be greater than 10 kΩ × cm, while the silicon handle wafer used for the CPWs with patterned ground plane designs is specified to be 450 Ω×cm–620 Ω×cm. The resistivity for these wafers is different due to the availability of materials for these experiments. However, simulation results show that the dielectric loss is constant above 100 Ω × cm, making the discrepancy in resistivity inconsequential. The patterned ground plane features “holes,” which are 8 μm × 8 μm and have a center-to-center spacing of 10 μm from each other in both directions along the length of the CPWs. The total metal density [or FF, as defined in Fig. 2(c)] of the patterned ground plane samples is 34.92 %, while the standard, solid ground plane samples have a metal density of 40.231 %. As an ad hoc rule, this pattern begins at a distance of at least three times the signal conductor width (w_{sig}) from the edge of the ground plane nearest the center conductor, such that an integer number of the patterned holes will fit in the total ground plane width. During fabrication, these holes become filled with SiO₂.

**Table 1**

|          | Gap   | Signal Width | Ground Plane Width | Solid Ground Plane Handle Resistivity | Patterned Ground Plane Handle Resistivity |
|----------|-------|--------------|--------------------|-------------------------------------|------------------------------------------|
| CPW 1    | 4 μm  | 6 μm         | 130.5 μm           | > 10×3 Ω×cm                         | 450-620 Ω×cm                             |
| CPW 2    | 8 μm  | 10 μm        | 124.5 μm           |                                     |                                          |

Fig. 2. (a) Schematic of a CPW using solid ground planes and (b) patterned ground planes, which are used in this study. The pattern consists of 8 μm × 8 μm holes in the ground plane with a center-to-center separation of 10 μm, which reduces the overall metal density in each device. (c) Detailed depiction of the unit cell used in the patterned ground plane design shows how the FF is calculated.
The effects of the SiO₂ bonding surface for samples using both the solid ground planes and patterned ground planes are shown in Figs. 3 and 4, which depict the distribution of thickness in each sample. The two chips shown in Figs. 3 and 4 have identical metal patterning with the exception of the patterned ground planes in Fig. 4. These data are collected using a 3-D surface characterization instrument (FRT MicroProf 200), which is a routine tool to perform total thickness variation (TTV) measurements. The variations in the SiO₂ thickness in Figs. 3 and 4 are due to varying planarization speeds during CMP. The planarization speed is faster over less dense patterns (i.e., sparse metal) and slower over dense patterns. Again, for the purpose of direct bonding to achieve heterogeneous integration, the final polished SiO₂ surface will be the bonding interface for the final device. Globally smooth surfaces are necessary in order to improve the bonding quality of integrated devices. The fringes seen in Figs. 3(a) and 4(a) are Moirè patterns and arise from sampling errors in the measurement. The fill pattern used in these designs is an array or checkerboard pattern in both the horizontal and vertical direction with a spatial frequency of 10 μm (present in both the solid ground plane and patterned ground plane samples). The maximum resolution in the instrument’s camera image is 50 μm, and thus, the Nyquist sampling criterion is not satisfied, creating false spatial frequencies (i.e., aliasing) that manifest as the measurement artifacts in Figs. 3(a) and 4(a). In theory, these artifacts can be removed through image processing, but this removes information from the data and is not implemented in this study. Regardless of the presence of these measurement artifacts, the distribution of thicknesses in Figs. 3(b) and 4(b) shows that not only the distribution of thickness narrows when using the patterned ground planes but also that thickness distribution in the solid ground plane sample is unimodal, while the distribution in the patterned ground plane sample is bimodal. The effect of having thicker polished oxide above the CPWs causes interference fringes under the illumination of visual light, which can be observed as the rings seen in the chip using the solid ground planes [Fig. 3(c)]. When the patterned ground plane architecture is utilized, the density of metal is much more uniform throughout the entire chip. In contrast with the solid ground planes, the interference fringes visually disappear, demonstrating that the polished oxide thickness is much more uniform across the chip.

The scattering parameters are measured for all devices using a two-port vector network analyzer (VNA). Due to the fact that the solid ground plane devices and the patterned ground plane devices have different substrate resistivities, there will be different charge accumulations at the interface between the SiO₂ and silicon [40], [41], [42]. To remove any loss dependence on this sheet charge, transmission is maximized (i.e., attenuation is minimized) as a function of applied dc voltage at a frequency of 1 GHz before the scattering parameters are measured while biased at the optimal voltage. This ensures that there is no charge accumulation at the SiO₂/Si interface (i.e., the flat-band voltage) [40], [41]. The flat-band voltage is found here by measuring the minimum propagation loss at 1 GHz as a function of dc bias by using a high-speed bias tee. All measured parameters are in acceptable agreement with each other, indicating that RF performance is not altered when implementing this ground plane patterning.

The propagation loss α and effective index n_eff of the guided RF mode on a transmission line of length L is extracted at frequency f from the measured scattering parameters using (1), where c is the speed of light. The characteristic impedance is extracted using (2), where Z_ref is the reference impedance and is 50 Ω in this study and in general. These expressions are derived from the relationship between the transmission matrix and scattering matrix for a reciprocal two-port network [43], [44], which is the case for the CPWs here. In other words, the transmission from port 1 to port 2 (S_{21}) is the same as the transmission from port 2 to port 1 (S_{12}), and the reflection into port 1 (S_{11}) is the same as the reflection into port 2 (S_{22})

\[
\alpha + j \frac{2\pi f}{c} n_{\text{eff}} = \frac{1}{L} \cosh^{-1} \left( 1 + \frac{S_{21}^2 - S_{11}^2}{2S_{21}} \right)
\]
Fig. 4. (a) Spatial distribution of relative thickness of the chip using the patterned ground plane design. (b) Histogram of the thickness distributions for the patterned ground plane designs. (c) Photograph of the chip with patterned ground plane designs. The region occupied by the array CPWs is enclosed in the white areas in (c), which are all 0.52-cm long for this sample. It is worth noting that the interference fringes are not visible in this sample, attributed to a much more uniform oxide thickness.

\[ Z_0 = Z_{\text{ref}} \sqrt{\frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}}. \]  

The loss mechanisms for these CPWs arise from conductive losses and dielectric losses. In theory, the conductive losses are proportional to the square root of the frequency, while dielectric losses are linear with frequency. However, this is overly simplistic and does not accurately describe the experimentally extracted loss because this model does not consider the frequency-dependent nature of other parameters, such as the dielectric permittivity. The dc-dependent losses due to charge accumulation at the SiO2/Si interface are a consequence of band bending in the semiconductor when the two materials are joined together. The amount of band bending (and charge accumulation) depends on the doping (resistivity) of the semiconductor. However, during thermal processing of the silicon (e.g., growing thermal oxide), the sheet charge characteristics are altered [40], which makes it appropriate to bias the CPWs such that the bias-dependent loss does not contribute to the overall loss in this study in order to compare the effects of the patterned ground plane designs. Another strategy to mitigate this effect is to deposit a thin layer of amorphous silicon between the SiO2 and Si layers [42], which passivates charges at the interface. The frequency-dependent modal parameters are measured for the CPW 1 and CPW 2 designs using both ground plane architectures and plotted in Figs. 5 and 6 where no appreciable difference in modal characteristic was measured up to 40 GHz between the solid and patterned ground plane architectures. The relatively high attenuation in these devices is attributed to a narrow electrode gap, which can be used in the design of an electrooptic modulator as a method of increasing the modulation efficiency. The slight instability measured above roughly 10 GHz is attributed to imperfections present in the S-parameter measurement calibration. Particularly, the phase in the measurement can be difficult to calibrate accurately, which is required to extract the modal parameters.

The scattering parameters are measured from 50 MHz to 40 GHz using a VNA (Agilent E8364B) at RF powers of \(-17\) dBm at each port. The CPWs are probed using Formfactor GSG Z probes rated for operation up to 40 GHz. A high-speed bias tee (Picosecond Pulse Labs 5542-202) was placed between port 1 of the VNA and the probe in order to apply the dc bias previously mentioned to remove any bias-dependent losses. To calibrate the measurement link, an impedance standard substrate was used which contains calibrated broadband 50-\(\Omega\) loads, open circuits, and calibrated throughput waveguides. The dc bias was provided using a Keithley 2400 source meter.

### III. Bonding Results

To assess the bonding quality, one of the CPW samples was bonded to a diced piece of TFLN, which consists of a
Fig. 6. (a) Extracted propagation loss, (b) modal index, and (c) magnitude of characteristic impedance ($|Z_0|$) for 0.52- and 1.02-cm long CPWs using both solid and patterned ground plane designs. The design parameters for CPW 2 are listed in Table I.

nominal 200-nm X-cut LiNbO$_3$ film on top of a 2-$\mu$m layer of SiO$_2$, all on top of a nominally 400-$\mu$m-thick silicon handle wafer. This is in contrast to the bonded TFLN sample in [5] and Fig. 1(a), which feature TFLN atop a LiNbO$_3$ handle wafer. The size of the TFLN chip is $5 \times 11$ mm$^2$, and the size of the CPW sample is $8.1 \times 12.5$ mm$^2$. The TFLN sample is cleaned using an SC1 clean, and the patterned CPW sample is cleaned with solvents. SC1 is avoided for the CPW sample it contains exposed metal pads, which can become corroded when using an SC1 clean. Following this cleaning step, both samples receive an O$_2$ plasma activation for 60 s, followed by a final cleaning step (the same SC1/solvent clean for the TFLN/CPW samples, respectively). After preparation, the bond is initiated by pressing the two samples together with a force of 500 N at a temperature of 150 °C for two hours. The sample is then annealed at 350 °C for ten hours while being under 500 N of force, translating to an applied pressure $9.09 \times 10^6$ Pa between the samples being bonded. The second anneal step was implemented to improve bonding quality, as the first bond and anneal did not sufficiently adhere. A description of both bonding steps is included here for completeness. The bonding quality was then assessed by submerging this bonded sample in water and using a confocal scanning acoustic microscopy (CSAM) instrument, whose results are presented in Fig. 7. In Fig. 7, the dark regions indicate successful bonding, and the lighter regions show voids. The boundary of the smaller TFLN sample is seen as the sharp edges of the black rectangle within the light rectangle, which is the CPW sample itself. This result shows that nearly the entire TFLN chip is successfully bonded. Some of the voids here are systematic (i.e., the straight lines in Fig. 7), which correspond to the solid center conductor of the CPWs. Unfortunately, a comparison between the bonding quality when using the patterned ground planes and the solid ground planes cannot be made using CSAM, as the CPW samples with solid ground planes debond when submerged in water, attributed to poor bond quality.

As discussed previously, the surface roughness and large-scale smoothness impact the bonding quality. In general, the samples to be bonded together should be as smooth and flat as possible. It can be seen from Figs. 3 and 4 that patterning the ground plane significantly improves the large-scale surface planarity of the sample. This can also be characterized by using a profilometer, which is presented in Fig. 8. A profilometer stylus is dragged across the long dimension of both the solid and patterned ground plane samples, which reveals topography toward the center of the chips, which is where the CPW array is located. Patterning the ground plane improves the magnitude of this topography by nearly a factor of four. Ideally, the entire chip surface should be completely flat, indicating that further optimization of the metal patterning can be pursued to further improve topography. Surface roughness on a small scale is measured using atomic force microscopy (AFM) and is also presented in Fig. 8. The AFM measurement is performed in a $1-\mu$m$^2$ area in the bonding region above the CPW array. The roughness here is defined as the arithmetic average of the difference between the mean height and measured height and is found to be 2.21 nm for the solid ground plane sample and 2.28 nm for the patterned ground plane sample. The change in metal
pattern design is not expected to affect this surface roughness, which is largely determined by the CMP process. Notably, there is not a sharp height difference in the area between the CPW array and the rest of the chip, which is due to the CMP step smoothing such features.

The same surface characterization may be performed on the material that is being bonded to, which, in this case, is TFLN. The same profilometer and AFM measurements are repeated on a representative TFLN sample and presented in Fig. 9. The range of the profilometer is substantially smaller than those in Fig. 8, which is an expected result as no patterning is performed on the TFLN sample. The measurement is, however, quite noisy, which is due to noise in the measurement combined with the small deviations in the surface topology. The roughness is again measured via AFM and found to be 0.208 nm. The TFLN surface is expected to be very smooth due to the fact that it does not experience any patterning.

IV. Modeled Effects of Ground Plane Patterning

To explore the effects that patterning the ground plane of CPWs may have on the RF characteristics, 3-D finite-element method (FEM) simulations using EMPro were performed from 0.04 GHz to 100 GHz. Fig. 10 shows the EMPro simulation results of both CPW 1 and CPW 2 with and without the patterning described in Fig. 2 and shows a strong correlation to the measured data in Figs. 5 and 6. Discrepancy between the CPW modal characteristics in the model and experiment is attributed to an imperfect calibration of the VNA prior to the measurement, particularly the phase calibration, which impacts the extracted values of interest. Patterning the ground plane has the largest effect on the RF attenuation of the propagating coplanar mode. The holes in the ground plane have nearly no effect on the RF effective index and impedance (with simulated changes <1% from 1 to 100 GHz), as the coplanar mode is primarily confined to the electrode gap between signal and ground planes. Since the hole pattern is at least $3 \times w_{\text{sig}} \mu m$ away from the inner ground plane edge, the electric field weakly interacts with the hole pattern. Although there is no change in the effective index, the propagation loss of the RF mode increases with the introduction of SiO$_2$ filled holes. This 0.05–1 dB/cm increase in attenuation at high frequencies is due to the surface current flowing along the ground plane being perturbed by the periodic oxide obstructions in the conductor. The propagation loss experienced by a CPW mode is proportional to the surface resistance of the conductors and the integrated surface current density around the conductors [45], [46]. Patterning the ground electrodes with oxide-filled squares alters the resistivity of the electrode, and thus the attenuation. This is evident from looking at the simulated surface current density flowing through the CPW (Fig. 11).

A simulation study was also performed to understand the effect that the fill factor (FF) and the edge factor (EF) have on CPW performance. FF is defined as the ratio of metal
in a unit cell to the total unit cell area [see Fig. 2(c)], while $EF$ is defined as the ratio of the width of the solid section of the ground plane to the width of the CPW signal trace width [see Fig. 2(b)]. The parameter FF for the devices fabricated in this study is 36%, and the parameter EF is 3.42 and 3.05, respectively, for CPW 1 and CPW 2. Fig. 12 shows the simulated RF index, loss, and impedance of CPW 2 as a function of EF with different metal densities. Here, an FF of 100% corresponds to a ground plane with no patterning (i.e., completely solid), whereas an FF of 0% corresponds to a ground electrode that is only $EF \times w_{sig}$ μm wide (i.e., the “patterned” region only consists of SiO$_2$). The size of the holes that are patterned into the electrodes has a negligible effect on the RF index and impedance; however, in the limit, as $FF$ goes to zero, the unit cell of the pattern in Fig. 2 is only SiO$_2$. This effectively narrows the ground plane from 124.5 μm to $EF \times w_{sig}$ μm wide. The narrower ground planes, while generously reducing the metal density of the CPW, also cause variations in the microwave effective index and impedance of the line [Fig. 12(b) and (c), respectively] which will eventually limit the high-speed performance of the CPWs. Although the effective index and impedance of the mode are minimally affected by the metal reduction, the RF attenuation can increase depending on the EF and FF [Fig. 12(a)]. If the metal density is heavily reduced ($FF < 36\%$) then the surface current density becomes disrupted by the periodic oxide fill, increasing the attenuation. For the same reason, if the patterning begins closer to the coplanar mode, the loss will increase. This effect is further explained by Fig. 11, which shows a top view of the buried electrode (CPW 2) simulated in EMPro with the ground plane patterned with different EF and FF combinations, overlaid with the simulated surface current through the electrodes (magnitude of which is given in the color bar). By comparing these surface current distributions with the simulated results from Fig. 12, it can be deduced that the attenuation of the CPW mode can be lessened by designing the ground plane pattern with an appropriate EF and FF, such that the pattern does not interact with the well-confined CPW mode. Thus, depending on the metal fill outside of the CPW structure, an appropriate EF can be chosen that mitigates the effect that patterning the ground plane has on attenuating the propagating mode while maintaining a specified required metal density for planarity.
Fig. 13. Schematic detailing the processing steps for the devices presented in this article. (a) Starting material is 3 μm of thermal oxide grown on the silicon handle wafer. (b) Metal is deposited and (c) etched to form the CPWs. (d) 2.4-μm-thick HDP CVD oxide is deposited on top of the patterned CPWs followed by a CMP step to achieve a nominal 350-nm thick layer of oxide above the metal. A 300-nm-thick film of SiNₓ is (e) deposited (f) and patterned, followed by the same oxide deposition and (g) CMP step to achieve a nominal 375-nm-thick oxide layer above the nitride film. A second SiNₓ film is (h) deposited and (i) patterned. (j) Final oxide deposition and CMP step is performed to achieve minimal oxide thickness between this nitride layer and bonding surface. This topmost waveguide forms part of the modulation region of this device, and the bottom waveguide layer is used to reduce optical loss at the air/TLFN interface [5].

V. CONCLUSION

This work has demonstrated an improvement in the uniformity of planarized surfaces through CMP processes when buried electrodes are implemented. This is significant for the heterogeneous integration of photonic materials, particularly for SiP which uses a CMOS-compatible metal encased in SiO₂. By engineering the metal density of the embedded structures, the local metal density is made to be more uniform throughout the chip layout, reducing systematic thickness variations from the CMP process. Although CMP has been.
demonstrated to provide local planarity. PICs requiring larger interaction lengths demand global planarity to achieve sufficient bond quality.

We experimentally show that this patterning does not detrimentally affect the performance of RF waveguides using patterned and nonpatterned ground planes, indicating no tradeoff in performance and bond quality at least up to 40 GHz and show that in simulation there is a minimal amount of additional attenuation (less than 1 dB/cm) at 100 GHz when using the patterned ground plane architecture. We also show that the ground plane patterning can be modified without significantly affecting performance, implying that many different patterns may be used to achieve our results. This is an important characteristic when applying these methods to other foundries which may have different requirements for minimum metal densities.

This showcases a capability to improve global thickness uniformity through the engineering of embedded metal structures, which is a necessity for high-speed electrical interconnects and high-speed devices. Improvement in global uniformity of planarized oxide thicknesses can have the effect of improving the yield of heterogeneously integrated optical components as more devices can be manufactured with the same structures because the planarized SiO₂ will be more constant throughout the chip. Therefore the ground plane design methodology discussed in this article can allow more devices to be manufactured with the same performance metrics (i.e., improved yield) through the removal of systematic variations within the bonding surface of the sample prepared in the CMOS foundry. Because this method can only improve the uniformity of optical devices and minimally affects the RF performance of CPWs, we can infer that electrooptic and optoelectronic devices manufactured using the patterned ground plane architecture will have nearly equivalent performance compared with devices built using the solid ground plane designs, albeit with a higher yield.

APPENDIX
FABRICATION PROCESS FLOW

The devices described in this article were fabricated following the flow presented in Fig. 13. The starting material is a silicon wafer, with 3 μm of thermally grown oxide on top. The metal layer is deposited and patterned, followed by a high-density plasma deposition (HDP) chemical vapor deposition (CVD) oxide deposition. The thickness of this oxide is nominally 2.4 μm. A CMP step is employed to reach the target oxide thickness above the top of the metal, which in this step is targeted to be 350 nm. The deposition of 2.4 μm thick oxide followed by the CMP step is used throughout device processing. The authors note that the surface topography is not expected to change as the metal thickness changes, predicted by the models described [24], [25], [27], [29], [31], [33], [34], [35], [39]. However, typically the deposited oxide will generally need to be thicker as the metal thickness increases in order to still achieve planarity. A plasma-enhanced CVD (PECVD) silicon nitride layer is deposited and patterned to form optical waveguides, followed by an oxide deposition and CMP step to reach an oxide thickness of 375 nm above the PECVD nitride film. A second PECVD silicon nitride film is deposited and patterned, followed by the same deposition/CMP step to achieve a minimal amount of oxide (~100 nm) between the bonding surface and nitride material.

ACKNOWLEDGMENT

This article describes objective technical results and analysis. Any subjective views or opinions that might be expressed in this article do not necessarily represent the views of the U.S. Department of Energy or the United States Government. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, Albuquerque, NM, USA, a wholly owned subsidiary of Honeywell International, Inc., Charlotte, NC, USA, for the U.S. Department of Energy’s National Nuclear Security Administration under Contract DE-NA0003525. The views, opinions, and/or findings expressed are those of the author(s) and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

The authors would like to thank the useful conversations with Keysight, Santa Rosa, CA, USA.

REFERENCES

[1] S. Fathpour, “Emerging heterogeneous integrated photonic platforms on silicon,” Nanophotonics, vol. 4, no. 1, pp. 143–164, May 2015.
[2] T. Komić, T. M. J. Tran, M. L. Davenport, and J. E. Bowers, “Photonic integrated circuits using heterogeneous integration on silicon,” Proc. IEEE, vol. 106, no. 12, pp. 2246–2257, Dec. 2018.
[3] S. M. Jokris et al., “The heterogeneous integration of optical interconnections into integrated microsystems,” IEEE J. Sel. Topics Quantum Electron., vol. 9, no. 2, pp. 350–360, Mar./Apr. 2003.
[4] S. Keyvaninia, M. Muneeb, S. Stankovic, P. J. Van Veldhoven, D. Van Thorhout, and G. Roelkens, “Ultra-thin DVS-BCB adhesive bonding of III-V wafers, dies and multiple dies to a patterned silicon-on-insulator substrate,” Opt. Mater. Express, vol. 5, no. 1, pp. 35–46, 2012.
[5] N. Boynton et al., “A heterogeneously integrated silicon photonic/lithium niobate travelling wave electro-optic modulator,” Opt. Exp., vol. 28, no. 2, pp. 1868–1884, 2020.
[6] P. O. Weigel et al., “Bonded thin film lithium niobate modulator on a silicon photonics platform exceeding 100 Ghz 3-dB electrical modulation bandwidth,” Opt. Exp., vol. 26, no. 18, pp. 23728–23739, 2018.
[7] P. O. Weigel et al., “Lightwave circuits in lithium niobate through hybrid waveguides with silicon photonics,” Sci. Rep., vol. 6, p. 22301, Mar. 2016.
[8] L. Chen and R. M. Reano, “Compact electric field sensors based on indirect bonding of lithium niobate to silicon microrings,” Opt. Exp., vol. 20, no. 4, pp. 4032–4038, 2012.
[9] L. Chen, J. Chen, J. Nagy, and R. M. Reano, “Highly linear ring modulator from hybrid silicon and lithium niobate,” Opt. Exp., vol. 23, no. 10, pp. 13255–13264, 2015.
[10] J. Zhao et al., “Shallow-etched thin-film lithium niobate waveguides for highly-efficient second-harmonic generation,” Opt. Exp., vol. 28, no. 13, pp. 19669–19682, 2020.
[11] A. Rao et al., “Second-harmonic generation in periodically-poled thin film lithium niobate wafer-bonded on silicon,” Opt. Exp., vol. 24, no. 26, pp. 29941–29947, 2016.
[12] L. Chang et al., “Heterogeneous integration of lithium niobate and silicon nitride waveguides for wafer-scale photonic integrated circuits on silicon,” Opt. Lett., vol. 42, no. 4, pp. 803–806, 2017.
[13] S. Ghosh, S. Yegnanarayanan, M. Ricci, D. Kharas, and P. Juodawlkis, “Low-loss thin film lithium niobate bonded on silicon nitride waveguides,” in Proc. Conf. Lasers Electro-Opt. (CLEO), 2020, pp. 1–2.
[14] J. Zhao, C. Ma, M. Rusing, and S. Mookherjee, “High quality entangled photon pair generation in periodically poled thin-film lithium niobate waveguides,” Phys. Rev. Lett., vol. 124, no. 16, Apr. 2020, Art. no. 163603.
[15] S. Aghaeimeibodi et al., “Integration of quantum dots with lithium niobate photonics,” Appl. Phys. Lett., vol. 113, no. 22, 2018, Art. no. 221102.

[16] O. Allibart et al., “Quantum photonics at telecom wavelengths based on lithium niobate waveguides,” J. Opt., vol. 18, no. 10, 2016, Art. no. 104001.

[17] T. J. Karle et al., “Heterogeneous integration and precise alignment of InP-based photonic crystal lasers to complementary metal-oxide semiconductor fabricated silicon-on-insulator wire waveguides,” J. Appl. Phys., vol. 107, no. 6, 2010, Art. no. 063103.

[18] J. M. Ramirez et al., “III-V-on-silicon integration: From hybrid devices to heterogeneous photonic integrated circuits,” IEEE J. Sel. Topics Quantum Electron., vol. 26, no. 2, pp. 1–13, Mar./Apr. 2020.

[19] Y. Chen, S. Li, and J. Zhang, “A contrast between rule-based and model-based dummy metal fill in ASIC design,” in Proc. Int. Conf. Intell. Control Inf. Process., Aug. 2010, pp. 601–606.

[20] S. Wolf and R. Tauber, “Silicon Processing for the VLSI Era,” vol. 1, 2003.

[21] B. Stine et al., “A closed-form analytic model for ILD thickness variation in CMP processes,” in Proc. CMP-MIC Conf., Feb. 1997, pp. 266–273.

[22] V. Mehrrota, S. L. Sam, D. Boning, A. Chandrakasan, R. Vallishayee, and S. Nassif, “A methodology for modeling the effects of systematic within-die interconnect and device variation on circuit performance,” in Proc. 37th Conf. Design Autom. (DAC), 2000, pp. 172–175.

[23] X. Luo et al., “High-throughput multiple dies-to-wafer bonding technology and III/V-on-Si hybrid lasers for heterogeneous integration of optoelectronic integrated circuits,” Frontiers Mater., vol. 2, p. 28, Apr. 2015.

[24] H. T. Hattori et al., “Heterogeneous integration of microdisk lasers on silicon strip waveguides for optical interconnects,” IEEE Photon. Technol. Lett., vol. 18, no. 1, pp. 223–225, Jan. 1, 2006.

[25] M. L. Davenport, S. Skendzic, M. J. Reck, and J. E. Bowers, “Heterogeneous silicon/III–V semiconductor optical amplifiers,” IEEE J. Sel. Topics Quantum Electron., vol. 22, no. 6, pp. 78–88, Dec. 2016.

[26] D. Van Thourhout, and R. Baets, “Heterogeneous integration of III-V photodetectors and laser diodes on silicon-on-insulator waveguide circuits,” in Proc. 3rd IEEE Int. Conf. Group IV Photon., Sep. 2006, pp. 188–190.

[27] D. Huang, P. Pintus, and J. E. Bowers, “Towards heterogeneous integration of optical isolators and circulators with lasers on silicon,” Opt. Mater. Exp., vol. 8, no. 9, pp. 2471–2483, 2018.

[28] D. O. Ouma et al., “Characterization and modeling of oxide chemical-mechanical polishing using planarization length and pattern density concepts,” IEEE Trans. Semicond. Manuf., vol. 15, no. 2, pp. 232–244, May 2002.

[29] Y. Chen, A. B. Kahng, G. Robins, and A. Zelikovsky, “Practical iterated fill synthesis for CMP uniformity,” in Proc. 37th Conf. Design Autom. (DAC), 2000, pp. 671–674.

[30] L. Di Cioccio, I. Radu, P. Gueguen, and M. Sadaka, “Direct bonding for wafer level 3D integration,” in Proc. IEEE Int. Conf. Integ. Circuit Design Technol., Jun. 2010, pp. 110–113.

[31] B. Stine et al., “The physical and electrical effects of metal-fill patterning practices for oxide chemical-mechanical polishing processes,” IEEE Trans. Electron Devices, vol. 45, no. 3, pp. 665–679, Mar. 1998.

[32] S. Wolf and R. Tauber, Silicon Processing for the VLSI Era, vol. 1, 2003.

[33] V. Mehrotra, S. L. Sam, D. Boning, A. Chandrakasan, R. Vallishayee, and S. Nassif, “A methodology for modeling the effects of systematic within-die interconnect and device variation on circuit performance,” in Proc. 37th Conf. Design Autom. (DAC), 2000, pp. 172–175.

[34] B. Lee, D. S. Boning, and L. Economikos, “A fixed abrasive CMP model,” in Proc. Int. Conf. Chem.-Mech. Polish (CMP) Planarization ULSI Multilevel Interconnection (CMP-MIC), 2001, pp. 395–402.

[35] J. Yota, M. R. Brongo, T. W. Dyer, K. P. Raffsseaeth, and J. A. Bondur, “Integration of ICP high-density plasma CVD with CMP and its effects on planarity for sub-0.5-um CMOS technology,” in Proc. SPIE, vol. 2875, pp. 265–274, Sep. 1996.

[36] X. Chen, S. Li, and J. Zhang, “A contrast between rule-based and model-based dummy metal fill in ASIC design,” in Proc. Int. Conf. Intell. Control Inf. Process., Aug. 2010, pp. 601–606.

[37] J. S. Orcutt and R. J. Ram, “Photonic device layout within the foundry CMOS design environment,” IEEE Photon. Technol. Lett., vol. 22, no. 8, pp. 544–546, Apr. 15, 2010.

[38] B. E. Stine et al., “‘The physical and electrical effects of metal-fill patterning practices for oxide chemical-mechanical polishing processes,” IEEE Trans. Electron Devices, vol. 45, no. 3, pp. 665–679, Mar. 1998.

[39] S. Wolf and R. Tauber, Silicon Processing for the VLSI Era, vol. 1, 2003.

[40] Y. Wu, S. Gamble, B. M. Armstrong, V. F. Fusco, and J. C. Stewart, “SiO2/interfacelayer effects on microwave loss of high-resistivity CPW line,” IEEE Microw. Guided Wave Lett., vol. 9, no. 1, pp. 10–12, Jan. 1999.

[41] C. Schollhorn, W. Zhao, M. Morschbach, and E. Kasper, “Attenuation mechanisms of aluminum millimeter-wave coplanar waveguides on silicon,” IEEE Trans. Electron Devices, vol. 50, no. 3, pp. 740–746, Mar. 2003.