Large-scale Deterministic Transmission among IEEE 802.1Qbv Time-Sensitive Networks

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Abstract—IEEE 802.1Qbv (TAS) is the most widely used technique in Time-Sensitive Networking (TSN) which aims to provide bounded transmission delays and ultra-low jitters in industrial local area networks. With the development of emerging technologies (e.g., cloud computing, many wide-range time-sensitive network services emerge, such as factory automation, connected vehicles, and smart grids. Nevertheless, TAS is a Layer 2 technique for local networks, and cannot provide large-scale deterministic transmission. To tackle this problem, this paper proposes a hierarchical network containing access networks and a core network. Access networks perform TAS to aggregate time-sensitive traffic. In the core network, we exploit DIP (a well-known deterministic networking mechanism for backbone networks) to achieve long-distance deterministic transmission. Due to the differences between TAS and DIP, we design cross-domain transmission mechanisms at the edge of access networks and the core network to achieve seamless deterministic transmission. We also formulate the end-to-end scheduling to maximize the amount of accepted time-sensitive traffic. Experimental simulations show that the proposed network can achieve end-to-end deterministic transmission even in high-loaded scenarios.

Index Terms—deterministic networking, large-scale transmission, DIP, TAS

I. INTRODUCTION

A collection of IEEE 802.1 Ethernet standards, known as Time-Sensitive Networking (TSN) [1], is widely applied to provide deterministic transmission (i.e., zero packet loss, bounded end-to-end delays, and ultra-low jitters) in industrial local area networks [2]. With the development of emerging technologies, such as cloud computing, fog/edge computing, and Virtual Reality (VR)/Augmented Reality (AR), the Internet is needed to become a more reliable infrastructure. Many wide-range time-sensitive network services are necessary in emerging areas, like factory automation, connected vehicles, and smart grids [3]. Due to the strict requirements for time synchronization and short link distances, TSN is not suited for providing wide-range deterministic transmission, and further supporting wide-range time-sensitive network services. Thus, we need to design a new network containing the existing TSN networks to achieve long-distance end-to-end deterministic transmission.

Within TSN, the IEEE 802.1Qbv (Time-Aware Shaper, TAS) [4] is applied broadly. It leverages timed gates that open/close according to a prescribed schedule, allowing frames full access to the egress link with zero interference from other queues. In [5], a TAS-capable switch with scheduled egress queues is designed to provide zero jitter and deterministic end-to-end latencies for software tasks. For achieving large-scale deterministic transmission, the IETF Deterministic Networking (DetNet) group promotes the standardization of deterministic techniques in Layer 3. Several candidate techniques are proposed, such as Cycle Specified Queuing and Forwarding (CSQF) [6] and Deterministic IP (DIP) [7]. Our prior work [8] deploys DIP in real large-scale networks and proves the effectiveness in large-scale deterministic transmission. In research efforts, the Paternoster algorithm [9] uses four queues that alternate every epoch using only frequency synchronization. However, Paternoster still lacks the analysis of effectiveness. iTSN [10] is a methodology for interconnecting multiple TSN networks for V2X communication. However, the communication distance of iTSN is only 1-2 km, which cannot be applied to provide deterministic transmission among TSN networks distributed across a wide area. Besides, all of the above-mentioned large-scale deterministic transmission mechanisms just focus on packet-level transmission. They cannot achieve application-level deterministic transmission.

Based on the research actuality and to tackle the problems in previous works, we propose a hierarchical network and achieve application-level scheduling on it. The hierarchical network contains local area access networks and a large-scale core network. Access networks perform TAS, while the core network uses DIP to provide large-scale deterministic transmission. In source hosts, we extend task-level scheduling in [5] and construct the relationship between application messages and packets. Besides, a traffic shaping mechanism is proposed to increase the number of scheduled applications. At the edge of TAS-D and DIP-D, we design cross-domain mechanisms to guarantee deterministic transmission between TAS and DIP. The optimization of end-to-end scheduling is formulated as a Mixed-Integer Programming (MIP) problem. The target of the optimization is to maximize the number of accepted applications. We design simulation experiments to prove the proposed network and transmission mechanisms are effective to achieve large-scale deterministic transmission among TAS networks, and the optimization can improve the number of scheduled applications.
II. BACKGROUND

A. Time-Aware Shaper (TAS)

In this section, we briefly introduce the functionality of IEEE 802.1Qbv (TAS). Fig. 1 depicts the internals of a TAS switch. Incoming packets pass through switching fabric and are redirected to the desired egress port. Then the priority filter assign packets to different queues (Q1 to Q8) based on the priority code point (PCP) of the IEEE 802.1Q header. Every queue at the egress port buffers packets in FIFO order, and it is associated with a timed gate. An open/close instruction of a timed gate is referred to as a Gate Control Entry (GCE). A GCE dictates which queues are allowed to access transmission medium. The entire cyclic sequence of GCEs is named Gate Control List (GCL). In Fig. 1 the GCE at time instant $t_0$ determine that Q8 is open for transmission and Q1-Q7 are close for receiving. The duration of one GCL cycle is defined in the cycle time ($T_{ct}$). The execution of all GCLs in a TSN domain is synchronized (i.e., the length and start time of $T_{ct}$ in all TAS switches are consistent) via the Precision Time Protocol (PTP) [11].

B. Deterministic IP (DIP)

DIP offers deterministic transmission by assigning packets to specific cycles in every hop. Time in network devices performing the DIP mechanism (DIP routers) is divided into cycles with length $T_{dip}$. The cycles in a DIP-enabled network are frequency synchronized. For a pair of adjacent DIP routers ($v_1$, $v_2$), assume that the packets sent in the cycle $x$ by the upstream node $v_1$ will arrive at the downstream node $v_2$ no later than the cycle $y$ (based on the propagation delay between $v_1$ and $v_2$). Then these packets will be retransmitted by $v_2$ in the cycle $(y + 1)$, and the cycle mapping relationship $x \rightarrow (y + 1)$ is established.

Fig. 2 shows the implementation of the pair of DIP routers ($v_1$, $v_2$). Each queue in an egress port is corresponding to a cycle. During a specific cycle, the queue corresponding to the cycle is open for transmission, while others are close for reception. Take the cycle mapping $x \rightarrow (y + 1)$ as an example. A packet sent in the cycle $x$ by the node $v_1$ carries a identifier $x$. When the node $v_2$ receives this packet, $v_2$ will check the cycle mapping table and find $x \rightarrow (y + 1)$. Then, this packet is assigned to the egress queue $(y + 1)$ and replaces the identifier $x$ with $(y + 1)$. When the cycle $(y + 1)$ comes, the queue $(y + 1)$ is open.

III. NETWORK DESIGN

A. The overview of the hierarchical network

In this section, a hierarchical network is presented to achieve long-distance end-to-end deterministic transmission. As shown in Fig. 3 the network is divided into TAS (TAS-D) and DIP (DIP-D) domains. TAS-D leverages TAS to provide deterministic traffic aggregation in access networks, and DIP-D uses DIP to support long-distance deterministic transmission across the large area core network. TAS-D contains source/destination hosts and TAS (edge) switches, while DIP-D contains DIP (edge) routers. We design hypercycle in DIP-D to unify the scheduling in TAS-D and DIP-D. In TAS, the duration of a cycle is named cycle time with a length $T_{ct}$. The resource allocation unit in TAS-D is $T_{ct}$. The length of a hypercycle $T_{hc}$ is equal to $T_{ct}$. Besides, $T_{hc}$ is a multiple of the duration of a DIP cycle $T_{dip}$. Therefore, $T_{hc}$ satisfies:

$$T_{hc} = T_{ct} = N_{dip}T_{dip} \quad (N_{dip} \in \mathbb{Z}^+)$$

B. Network and traffic model

The network is modeled as a directed graph $G = \{V, L\}$. $V$ is the set of nodes (containing source hosts, destination hosts, TAS switches, TAS edge switches, DIP routers and DIP edge routers, i.e., $V = \{V_{src}, V_{dest}, V_{tas}, V_{edge}, V_{dip}, V_{edge_dip}\}$). $L$ is the set of links. A link $l = (v_1, v_2)$ with $l \in L$, $v_1, v_2 \in V$ is uniquely identified by its source $v_1$ and end $v_2$. It is characterized by a tuple $(l.bw, l.d, l.q)$, where $l.bw$ is the bandwidth of the link $l$, $l.d$ is the link delay, and $l.q$ represents the number of egress queues used for deterministic transmission in the source node of link $l$ (i.e., $v_1$). The link delay $l.d$ refers to the propagation delay on the medium and the processing delay in nodes. We regard $l.d$ as a constant.

In a source host $v_0 \in V_{src}$, a time-sensitive application $\tau$ emits periodic unicast messages. An application is described by a tuple $(\tau_{src}, \tau_{dest}, \tau.e2c, \tau.L, \tau.T)$ where $\tau_{src}, \tau_{dest}, \tau.e2c, \tau.L,$ and $\tau.T$ represent the source host, the
destination host, the maximum acceptable end-to-end delay, the message size, and the period, respectively.

Because the transmission pattern in every $T_{ct}$ is the same in TAS, $T_{ct}$ must be a multiple of the period of the messages of an application $\tau$ (i.e., $T_{ct} = N_{\tau,m} \cdot \tau.T$, $N_{\tau,m} \in \mathbb{N}^+$. The messages within a $T_{ct}$ are denoted by $\mathcal{M}_\tau = \{m_{\tau,i}|i \in [1, N_{\tau,m}]\}$.

In the transmission medium, a message may be divided into multiple packets. The number of packets belonging to the same message of $\tau$ is denoted by $N_{\tau,p}$. The set of packets belonging to the application $\tau$ is expressed as $\mathcal{P}_\tau = \{p_{\tau,i,j}|i \in [1, N_{\tau,m}], j \in [1, N_{\tau,p}]\}$. The packet size of a packet $p_{\tau,i,j}$ is denoted by $r_{\tau,i,j} \cdot L$.

The relationship between messages of the application $\tau$ in the source host $v_0$ and the corresponding packets are shown in Fig. 4. In this example, $N_{\tau,p} = 2$, and $N_{\tau,m} = 3$.

C. Traffic shaping in source hosts

In source hosts, the start time of an application’s transmission is random. Messages belonging to different applications may arrive at the same time. Thus, we need traffic shaping in source hosts to provide deterministic transmission.

For a message $m_{\tau,i}$, the offset between the arriving time and the start time of $T_{ct}$ is denoted by $m_{\tau,i} \cdot \phi$. If a packet $p_{\tau,i,j}$ is derived from the message $m_{\tau,i}$, the offset between the sending time of $p_{\tau,i,j}$ and the start time of $T_{ct}$ is expressed as $p_{\tau,i,j} \cdot \phi_{t_{0}}$, where $v_0$ is the source host. We forbid the transmission across two cycle time in TAS, so $p_{\tau,i,j} \cdot \phi_{t_{0}} \in [0, T_{ct} - r_{\tau,i,j} \cdot L]$.

Fig. 5 shows the traffic shaping of applications $\tau_1$ and $\tau_2$. The messages of $\tau_1$ and $\tau_2$ (i.e., $m_{\tau_1,1}$ and $m_{\tau_2,1}$) arrive simultaneously. We assign different offsets of packets (like $p_{\tau_1,1,1}, p_{\tau_2,1,1}$, etc.) to determine the transmission in the source host.

Implementation: Take the example shown in Fig. 5. The source host $v_0$ performing TAS also has the internals shown in Fig. 3. We assign the packet $p_{\tau_1,1,1}$ to Q8, $p_{\tau_1,1,2}$ to Q7, $p_{\tau_2,1,1}$ to Q6, $p_{\tau_2,1,2}$ to Q5. We can write the following GCEs to the GCL: “$p_{\tau_1,1,1} \cdot \phi_{t_{0}}$: cccccco”, “$p_{\tau_1,1,2} \cdot \phi_{t_{0}}$: ccccecc”, “$p_{\tau_2,1,1} \cdot \phi_{t_{0}}$: ccccecc”, “$p_{\tau_2,1,2} \cdot \phi_{t_{0}}$: ccccccecc”.

D. Transmission from TAS-D to DIP-D

Due to the differences between TAS and DIP, we design a cross-domain mechanism in DIP edge routers. Assume that an application $\tau$ is routed through a link $l = (v_1, v_2)$ with $v_1 \in \mathcal{V}_{\text{tas}}^\text{edge}$ and $v_2 \in \mathcal{V}_{\text{tas}}^\text{edge}$. The start time of a cycle time in $v_1$ is $t_1$, and the start time of a hypercycle in $v_2$ is $t_2$.

The offset of the cycle time and the hypercycle is denoted by $l.\Delta_{h} = t_2 - t_1$, where $t_1 > t_2$. The packets transmitted by $v_1$ should be mapped to the transmission cycles in $v_2$. To improve the resource utilization, we introduce cycle shift like [12] for traffic shaping. The next link of $l$ is denoted by $l + 1$. The cycle shift of the packet $p_{\tau,i,j}$ is $r_{\tau,i,j}$, where $r_{\tau,i,j} \in \mathbb{N} \cap [0, (l + 1)q - 2]$. The mapping relationship is denoted by $\Theta(p_{\tau,i,j})$. The definition of $\Theta(p_{\tau,i,j})$ is:

$$\Theta(p_{\tau,i,j}) = \left(\left\lfloor\frac{p_{\tau,i,j} \cdot \phi_{t_{1}} + p_{\tau,i,j} \cdot L/l.bw + l.d + l.\Delta_{h}}{T_{dip}}\right\rfloor + \Delta_{t_{1},i,j}\right) \bmod N_{dip}$$  (2)

$p_{\tau,i,j} \cdot \phi_{t_{1}}$ is the offset between the sending time of the packet $p_{\tau,i,j}$ and the start time of $T_{ct}$ in node $v_1$. Equation (2) means the packet $p_{\tau,i,j}$ transmitted by $v_1$ will be retransmitted in cycle $\Theta(p_{\tau,i,j})$ by $v_2$. It is apparent that the range of $\Theta(p_{\tau,i,j})$ is $[0, N_{dip} - 1]$. Fig. 6 illustrates the example where $N_{dip} = 5$, and $r_{\tau,i,j} = 1$. The packet $p_{\tau,i,j}$ will be retransmitted by $v_2$ in cycle 4 (i.e., $\Theta(p_{\tau,i,j}) = 4$).

Implementation: Take the example shown in Fig. 6. Assume that the egress queues in $v_2$ open in a circular fashion from queue 0 to queue $((l + 1)q - 1)$. If the queue $x$ in node $v_2$ is open for transmission during cycle 2, the packet $p_{\tau,i,j}$ will be assigned to the queue $((x + r_{\tau,i,j} + 1) \bmod (l + 1)q)$.

E. Transmission from DIP-D to TAS-D

When packets come out from DIP-D, we need to form GCL in TAS edge switches. Thus, we design a cross-domain mechanism in TAS edge switches to recover the transmission in TAS-D.

A link $l = (v_1, v_2)$ with $v_1 \in \mathcal{V}_{\text{tas}}^\text{edge}$ and $v_2 \in \mathcal{V}_{\text{tas}}^\text{edge}$ is contained in the route assigned to the application $\tau$. The start time of a hypercycle in $v_1$ is $t_1$ and the start time of a cycle time in $v_2$ is $t_2$. The offset of the hypercycle and the cycle...
time is denoted by \( l, \Delta^h = t_1 - t_2 \), where \( t_1 > t_2 \). If a packet \( p_{\tau,i,j} \) is sent in cycle \( c \) by \( v_1 \), it will arrive at \( v_2 \) by \( \theta_t(c) \), where \( \theta_t(c) \in [0, T_{ct}) \). \( \theta_t(c) \) is defined as:

\[
\theta_t(c) = (c+1)T_{dip} + l.d + \Delta^h - \frac{(c+1)T_{dip} + l.d + \Delta^h}{T_{ct}}
\]

(3)

The traffic shaping in \( v_2 \) is: we design an extra delay \( \varphi_{\tau,i,j} \) for the packet \( p_{\tau,i,j} \). The packet offset in \( v_2 \) is \( p_{\tau,i,j} = \theta_t(c) + \varphi_{\tau,i,j} \). The next link of \( l \) is denoted by \( l+1 \), and the range of \( \varphi_{\tau,i,j} \) is \([0, T_{ct}]\).

Fig. 7 shows the example where \( N_{dip} = 5 \), and \( c = 1 \). The packet \( p_{\tau,i,j} \) is all sent in cycle \( 1 \) by \( v_1 \), and it will arrive at \( v_2 \) by \( \theta_t(1) \). The extra delay is \( \varphi_{\tau,i,j} \), so the packet will be retransmitted with the packet offset \( p_{\tau,i,j} = \theta_t(1) + \varphi_{\tau,i,j} \).

**Implementation:**

Take the example shown in Fig. 4. Since the packets’ arriving order at node \( v_2 \) is non-deterministic, we cannot use FIFO egress queues. When a queue is open for transmission, we must ensure that the proper packet is in the first place. Thus, we leverage PIFO \([13]\), which allows packets to be enqueued into an arbitrary location in a queue, to guarantee the correct transmission order.

**F. An end-to-end example**

The end-to-end transmission of a message \( m_{\tau,i} \) is illustrated in Fig. 8. The message is divided into 2 packets \( p_{\tau,i,1} \) and \( p_{\tau,i,2} \), and the period of the message is equal to \( T_{ct} \). In DIP-D, one hypercycle contains 5 dip cycles (i.e., \( N_{dip} = 5 \)). A route \( L_r \) is assigned to the application \( \tau \). \( L_r \) is given by:

\[
L_r = (v_0, v_1, v_2, v_3, v_4, v_5) = (l_0, l_1, l_2, l_3, l_4)
\]

(4)

where \( v_0 \in V_{src}, v_5 \in V_{dest}, \{v_1, v_4\} \subseteq V_{edge}, \) and \( \{v_2, v_3\} \subseteq V_{dip}. \) Obviously, the link \( l_k = (v_a, v_a+1) \).

Take the packet \( p_{\tau,i,1} \) as an example. In the source host \( v_0 \), the transmission offset of this packet is \( \varphi_{\tau,i,1} \). Thus, if \( p_{\tau,i,1} \) is enqueued into the egress queue Q8, the GCL in \( v_0 \) must contain a GCE “\( p_{\tau,i,1}, \varphi_{v_0}, ccccccc \)”. When the reception of the packet is finished in the TAS edge switch \( v_1 \), \( p_{\tau,i,1} \) will be forwarded immediately. After receiving the packet, the DIP edge router \( v_2 \) performs the cross-domain transmission mechanism. According to the cycle shift \( r_{\tau,i,1} = 1 \), the value of \( \Theta(p_{\tau,i,1}) \) is 1. Thus, \( p_{\tau,i,1} \) will be transmitted in cycle \( 1 \) by \( v_2 \). The transmission between two DIP edge routers \( v_2 \) and \( v_3 \) is the normal mechanism in DIP. Because the packets sent in \( v_2 \)’s cycle \( 1 \) arrive at \( v_3 \) no later than cycle \( 4 \) in \( v_3 \), those packets are forwarded in the next cycle (i.e., cycle \( 0 \)). In the TAS edge switch \( v_4 \), the offset \( p_{\tau,i,1}, \varphi_{v_4} \) can be calculated based on \( \theta_t(0) \) and \( \varphi_{\tau,i,1} \). Then, \( v_4 \) opens the egress queue with \( p_{\tau,i,1} \) according to the GCE of \( p_{\tau,i,1}, \varphi_{v_4} \). Finally, the destination host \( v_5 \) receives the packet. When the packet \( p_{\tau,i,2} \) is received by \( v_5 \), the transmission of the message \( m_{\tau,i} \) is finished. The application-level end-to-end delay is greater than the packet-level delay of \( p_{\tau,i,1} \). The transmission in every hop is accurately controlled. Thus, the hierarchical network can achieve deterministic transmission delay and zero jitters.

**IV. TRANSMISSION SCHEDULING**

**A. Decision variables**

The decision variables of the application-level schedule contain the following:

**Admission control:** This variable indicates whether an application \( \tau \) is acceptable or not. The variable is denoted by \( x_\tau \). If \( \tau \) is accepted, \( x_\tau = 1 \). Otherwise, \( x_\tau = 0 \). Let \( \mathcal{X} = \{x_\tau | \tau \in \Gamma\} \).

**Route selection:** The route assigned to an accepted application \( \tau \) is \( L_\tau \), and the definition of \( L_\tau \) is in (7). Let \( \mathcal{L} = \{L_\tau | \tau \in \Gamma\} \).

**Packet offset in Source Hosts:** The packet offset of packet \( p_{\tau,i,j} \) in the source host \( v_0 \) is \( p_{\tau,i,j}, \varphi_{v_0}, \) and \( p_{\tau,i,j}, \varphi_{v_0} \in [0, T_{ct} - \frac{p_{\tau,i,j}, L_{\tau}, \varphi_{v_0}}{(v_0, v_1)}] \). Let \( \Phi = \{p_{\tau,i,j}, \varphi_{v_0} | \tau \in \Gamma, \tau_{r,i,j} \in \mathcal{P}_\tau, v_0 = \tau.src\} \).

**Cycle Shift:** In the DIP edge router contained in \( L_\tau \), the cycle shift of packet \( p_{\tau,i,j} \) is \( r_{\tau,i,j} \). If the DIP edge router is the source of link \( l, r_{\tau,i,j} \in \mathbb{N} \cap [0, l - 2] \). Let \( \mathcal{R} = \{r_{\tau,i,j} | \tau \in \Gamma, \tau_{r,i,j} \in \mathcal{P}_\tau\} \).

**Extra Delay in TAS Edge Switches:** In the edge TAS switches whose upstream node is a DIP router, the extra delay of packet \( p_{\tau,i,j} \) is \( \varphi_{\tau,i,j} \), and \( \varphi_{\tau,i,j} \in [0, T_{ct}] \). Let \( \mathcal{O} = \{\varphi_{\tau,i,j} | \tau \in \Gamma, \tau_{r,i,j} \in \mathcal{P}_\tau\} \).

**B. Constraints on the Transmission Mechanism**

**Conflict Constraint:** For a link \( l = (v_a, v_b) \) where \( v_a \in V_{src} \cup V_{edge} \cup V_{dip} \), no two packets that are routed through \( l \) can overlap in the time domain. For any two packets \( p_{\tau_1,i,j_1} \) and \( p_{\tau_2,i,j_2} \)
and $p_{r_2,i_2,j_2}$ routed through the link $l$, the constraint on the packet offsets in $v_a$ is as follows:

$$
\begin{align*}
(p_{r_1,i_1,j_1},\phi_{v_a} & \geq p_{r_2,i_2,j_2},\phi_{v_a} + \frac{p_{r_2,i_2,j_2},L}{l.bw}) \lor \\
p_{r_2,i_2,j_2},\phi_{v_a} & \geq p_{r_1,i_1,j_1},\phi_{v_a} + \frac{p_{r_1,i_1,j_1},L}{l.bw}
\end{align*}
$$

(5)

**DIP Cycle Capacity Constraint:** For a cycle $c$ in a DIP router $v_a \in V_{dip}$ on a link $l = (v_a, v_b)$, if a set of packets $P_c$ is assigned to it, the total size of $P_c$ should not exceed the transmission capacity of $c$:

$$\sum_{p_{r,i,j} \in P_c} p_{r,i,j},L \leq T_{dip} \cdot l.bw$$

(6)

C. Constraints on application-level end-to-end Delay

We define the route assigned to the application $\tau$ as follows:

$$L_\tau = (v_0, v_1, \cdots, v_k, v_{k+1}, \cdots, v_m, v_{m+1}, \cdots, v_n)$$

$$= (l_0, l_1, l_2, \cdots, l_{n-1})$$

(7)

where $v_0 \in V_{src}$, $v_n \in V_{dest}$, and $\{v_1, v_2, \cdots, v_{k-1}\} \subseteq V_{tas}$, $\{v_{k+1}, v_{m+1}\} \subseteq V_{tas}$, $\{v_{m+1}, v_{m+2}, \cdots, v_{n-1}\} \subseteq V_{tas}$, $\{v_{k+1}, v_{m}\} \subseteq V_{dip}$, and $\{v_{k+1}, v_{k+2}, \cdots, v_m\} \subseteq V_{dip}$. The start time of a hypercycle in $v_a$ and $v_b$ is communicated through the link $l_a = (v_a, v_{a+1})$.

In DIP, for a link $l = (v_a, v_b)$, and $v_a, v_b \in V_{dip} \cup V_{edge}$, the start time of a hypercycle in $v_a$ and $v_b$ is denoted by $\Delta^h(l) = t_a - t_b$. A packet $p_{r,i,j}$ sent in cycle $c$ by $v_a$ is retransmitted by $v_b$ in cycle $\vartheta_l(c)$. The definition of $\vartheta_l(c)$ is:

$$\vartheta_l(c) = \left(\frac{(c+1)T_{dip} + l.d + \Delta^h(l)}{T_{dip}}\right) \text{ mod } N_{dip}$$

(8)

The transmission cycles of packet $p_{r,i,j}$ on $(v_{k+1}, v_{k+2}, \cdots, v_m)$ are denoted by $c = (c_{k+1}, c_{k+2}, \cdots, c_m)$. Based on (2) and (5), the cycles can be calculated recursively:

$$c_a = \begin{cases} 
\Theta(p_{r,i,j}) & a = k + 1 \\
\vartheta_{l,a-1}(c_{a-1}) & a \in [k + 2, m]
\end{cases}$$

(9)

The packet-level end-to-end delay of $p_{r,i,j}$ is denoted by $\Delta_{r,i,j}(l_\tau)$. The value of $\Delta_{r,i,j}(l_\tau)$ is:

$$\Delta_{r,i,j}(l_\tau) = \vartheta_{l_\tau}(r_{i,j},\phi_{r_{i,j}} - m_{r,i,j},\phi) + \sum_{a=0}^{k-1} \left(\frac{p_{r_{i,j}},L}{l_{a,bw}} + l_a, d\right)$$

$$+ \left| p_{r_{i,j}},\phi_{r_{i,j}} + \frac{p_{r_{i,j}},L}{l_{a,bw}} + l_k, d + l_k, \Delta^h(l) \right| T_{dip}$$

$$- l_{k-1}, \Delta_h^h(l) + (r_{i,j} + 1)T_{dip} + l_{k+1}, d$$

$$+ \sum_{a=k+1}^{m-2} \left(\frac{c_a + 1}{T_{dip}} + l_a, d + \Delta^h(l_a)\right) T_{dip}$$

$$- c_{m-1}T_{dip} - l_a, d - \Delta^h(l_a) + l_{a+1}, d + \vartheta_{l,a}$$

$$+ \sum_{a=m}^{c_{m-1}} \frac{p_{r_i,j},L}{l_{a,bw}} + l_a, d$$

(10)

The application-level end-to-end delay of the application $\tau$ should be less than $\tau.e_2e$, the constraint is as follows:

$$\max_{i \in [1,N_{r,m}], j \in [1,N_{r,p}]} \Delta_{r,i,j}(l_\tau) \leq \tau.e_2e$$

(11)

D. Objective Function

The target of the scheduling is to accept as many applications as possible. In the five decision variables, the admission control and route selection are discrete variables, while the remaining three variables are continuous. Thus, the problem can be formulated as a Mixed-Integer Programming (MIP):

$$\max_{x, l, e, \Phi, R, 0} \sum_{\tau \in e^l} x_\tau$$

s.t.  $x_\tau \in \{0, 1\}$

(12a) (12b) (12c)

V. SIMULATION

In the simulation, we construct the core network in the proposed hierarchical network based on a real-world network Atlanta [14]. The network is established in OMNet++, and it contains 15 DIP (edge) routers. We set 10 access networks in the simulation. Every access network contains a TAS edge switch connected to a DIP edge router, and a host is connected to the switch. In the core network, the link delay is 150 $\mu$s, and the link capacity is 10 Gbps. The link in access networks has a propagation delay 1.5 $\mu$s, and the capacity 1 Gbps. The period of messages in the network is 1 ms or 2 ms, randomly. Besides, the message size is randomly one or two times the MTU. The duration of a DIP cycle is $T_{dip} = 10 \mu$s. Thus, the duration of a cycle time and a hypercycle is $T_{ch} = T_{hc} = 2$ ms. In the simulation, we leverage genetic algorithm tool box embedded in Matlab to solve the problem (12).

Fig. 9 shows the application-level end-to-end delays of a time-sensitive application. We rewrite the components in OMNet++ to emit interference flows for creating various congestion levels. In Fig. 9 the network utilization is 59%. The end-to-end delays in best-effort transmission vary from 662 $\mu$s to 1151 $\mu$s, while the proposed scheduling can achieve deterministic end-to-end delay 953 $\mu$s with zero jitters. Moreover, the delay of proposed scheduling is lower than the minimum delay of best-effort transmission. Obviously, the control of transmission in every hop may lead to extra delays. Thus, the deterministic end-to-end delay is greater. However, the proposed scheduling can achieve zero jitters, and the delay is significantly less than the maximum delay of best-effort transmission.

Fig. 10 depicts the transmission jitters with the increase of network utilization. We gradually increase the number of interference flows to create different congestion levels. The proposed scheduling can remain zero jitters, while the jitters of best-effort transmission grow exponentially. Due to the isolation of transmission between time-sensitive messages and interference flows, the time-sensitive messages will not interfere with interference flows. In best-effort transmission, the interleaving results in non-deterministic delays in egress queues, which create jitters.
Fig. 9. The application-level end-to-end delays in a medium-loaded scenario with network utilization 50%.

Fig. 10. The transmission jitters in different congestion levels. Jitters in best-effort transmission grow significantly with the increase of network utilization. The proposed scheduling can achieve zero jitters.

Fig. 11 illustrates the ratio of accepted applications using different transmission mechanisms. “No route selection” means that all applications perform “shortest route first”. Moreover, “No shaping” implies that messages are forwarded immediately when they are created in source hosts, and the cycle shifts in DIP edge routers are always 0. The link capacity in TAS-D is 1 Gbps, and we gradually increase the packet rates of time-sensitive packets to create different levels of congestion. Compared with “no shaping”, the proposed scheduling can accept more applications in light-loaded, medium-loaded, and high-loaded scenarios (i.e., 240 Mbps, 480 Mbps, and 720 Mbps, respectively). In extremely high-loaded scenarios (with the packet rate of 960 Mbps), the ratios of accepted applications in proposed scheduling and “no shaping” are the same, because there is little extra transmission resource for traffic shaping. Besides, the acceptance ratios are the same between the proposed scheduling and “no route selection”. Because packets belonging to the same access networks have to pass through the same TAS link to DIP-D, which attenuates the influence of route selection. In conclusion, the proposed scheduling can improve the number of accepted applications.

VI. CONCLUSION

To empower large-scale deterministic transmission among TAS networks, this paper proposes a hierarchical network containing access networks and a core network. In access networks, we exploit TAS to provide deterministic transmission during the aggregation of traffic from source hosts. In the core network, DIP is applied to achieve large-scale deterministic transmission. To achieve end-to-end scheduling, we design a traffic shaping mechanism in source hosts, and cross-domain transmission between TAS and DIP. Moreover, the scheduling is formulated as a MIP to improve the network throughput. Simulation results show that the proposed network can achieve deterministic transmission even in high-loaded scenarios.

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