Saving Moore’s Law Down To 1 nm Channels With Anisotropic Effective Mass

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Scaling transistors’ dimensions has been the thrust for the semiconductor industry in the last four decades. However, scaling channel lengths beyond 10 nm has become exceptionally challenging due to the direct tunneling between source and drain which degrades gate control, switching functionality, and worsens power dissipation. Fortunately, the emergence of novel classes of materials with exotic properties in recent times has opened up new avenues in device design. Here, we show that by using channel materials with an anisotropic effective mass, the channel can be scaled down to 1 nm and still provide an excellent switching performance in phosphorene nanoribbon MOSFETs. To solve power consumption challenge besides dimension scaling in conventional transistors, a novel tunnel transistor is proposed which takes advantage of anisotropic mass in both ON- and OFF-state of the operation. Full-band atomistic quantum transport simulations of phosphorene nanoribbon MOSFETs and TFETs based on the new design have been performed as a proof.

Shrinking the size of metal oxide semiconductor field effect transistors (MOSFETs) has improved the functionality, speed, and cost of microprocessors over the last four decades. However, the advantages of scaling are quickly fading away. For example, the operational frequency of CPUs has stopped improving since 2003 due to power consumption of CPUs reaching their cooling limit ($\approx 100$ W/cm$^2$). Moreover, scaling down $L_{ch}$ towards the few nanometer regime is becoming more challenging due to source-to-drain (SD) leakage current. The gate controlled potential barrier becomes more transparent as channel becomes shorter and direct SD tunneling increases. Another challenge in miniaturizing MOSFETs is scaling down the supply voltage $V_{DD}$. A smaller $V_{DD}$ can be achieved in a switch with sharper ON to OFF transition. However, the steepness of conventional MOSFETs have a fundamental limit due to thermionic injection of carriers over the channel barrier ($60$ mV/decade at room temperature). Accordingly, $V_{DD}$ in MOSFETs does not scale very well. On the other hand, tunnel FETs (TFETs) can, in principle, provide steeper switching. Nevertheless, scaling TFETs is even trickier than MOSFETs, since scaling affects both ON- and OFF-states of the TFETs. Hence, the tremendous improvement in processing power of transistors every few years linked to the dimension scaling and empirically described by Moore’s law has reached a dead end. Fortunately, it is shown here that 2D materials with anisotropic effective mass ($m^*$) can be used to solve these problems and save Moore’s law.

First, we discuss the source-to-drain tunneling challenge of the ultra scaled MOSFETs. Reducing the channel size makes the potential barrier more transparent. To visualize this, the transmission is shown in colormap on a logarithm scale and with an overlayed band diagram of MOSFETs in Fig. 1. The band diagram and transmission profile of a 12 nm and 5 nm long channel GaAs MOSFET are compared respectively in Fig. 1a,b. 5 nm long channel GaAs MOSFET suffers significantly from SD leakage which reduces the gate control. Equation (1) shows the dependence of tunneling current through barrier on $m^*$ of the channel material. According to Equ. (1), an apparent solution to the high transparency of channel barriers in short channel regime is a channel material with higher effective mass.

$$\log(I_{OFF}) \propto -L_{ch}\sqrt{m^*}$$

Although high $m^*$ channel materials block SD tunneling effectively, they have a set of drawbacks too. Quantum capacitance ($C_Q$) of channel material increases as a result of larger density of states (DOS) and $m^*$. Accordingly,
the gate capacitance ($C_G$) which is the net series capacitance of $C_Q$ and oxide capacitance ($C_{ox}$) increases. Hence, a larger $m^*$ translates into a larger switching delay ($\tau = C_G V_{DD}/I_{ON})$.

$$C_G = \frac{1}{C_{ox}} + \frac{1}{C_Q}$$ (2)

Anisotropic effective mass can provide a solution to this problem with reducing $C_Q$ by a factor of $\frac{1}{\sqrt{m_1^*/m_2^*}}$. This reduction of $C_Q$ is the result of the decreased density of states (DOS) in anisotropic materials:

$$C_Q = \frac{q^2 \text{DOS}}{\pi \hbar^2} = \frac{q^2 \sqrt{m_1^* m_2^*}}{\pi \hbar^2}$$ (3)

where $m_1^*$ and $m_2^*$ are low and high effective masses of the channel material along its two main axes. If high $m^*$ axis of channel is aligned with transport direction and low $m^*$ axis is aligned with the confinement direction, both low transparency and small switching delay can be achieved. Note that high $m^*$ along the channel increases the carriers decay rate through barrier exponentially, whereas low confinement $m^*$ reduces DOS and $C_Q$. Hence, a 2D material such as phosphorene can provide an excellent switching performance in MOSFETs ensuring the continuation of Moore’s Law to atomic dimensions.

Here, we discuss the scaling challenge of TFETs. Although TFETs were intended to reduce the power consumption of transistors, scaling TFETs below 10 nm is even more challenging than MOSFETs. The ON-state and OFF-state tunneling currents ($I_{ON}$ and $I_{OFF}$) depend on the same device parameters. Thus decreasing $I_{OFF}$ would reduce $I_{ON}$. Roughly, the ON/OFF ratio of TFETs depends on $\frac{\Lambda}{L_{ch}}$, $\frac{m_1^* E_{g1}}{m_2^* E_{g2}}$, the reduced effective mass and the bandgap of the channel material (source-to-channel junction), respectively.

Shrinking the channel length to few nanometers brings $L_{ch}$ close to $\Lambda$ and reduces $I_{ON}/I_{OFF}$ significantly. One apparent solution can be a heterostructure channel where the term $m_1^* E_{g2}$ is much smaller than $m_2^* E_{g1}$ due to different materials used in the source and channel regions. However, heterostructure TFETs suffer from interface states which deteriorate their OFF-state performance. Although homojunction TFETs do not have the interface states, it is challenging to provide high ON/OFF ratio especially below 6 nm. Anisotropic effective mass can also provide a solution for this challenge by setting source-channel junction along low $m^*$ axis of channel material and the channel barrier along high $m^*$ axis. In this work, a novel TFET is proposed which works based on homojunction channel and anisotropic $m^*$ and hence it is free of interface states between different channel materials in heterojunctions. Although, many novel materials and designs have been proposed to enhance the performance of TFETs such as 2D material TFETs, Nitride heterostructures, dielectric engineering, there are not many proposals for solving the scaling challenge of TFETs. In this work, a new TFET design is proposed to overcome the scaling challenge and enable downsizing to 2 nm channel lengths. Figure 2a shows a novel TFET device structure to take advantage of anisotropic effective mass. Notice that the gate is L-shaped. Figure 2b depicts that the tunneling in the ON-state occurs along the low $m^*$ axis of the channel enhancing the $I_{ON}$. However, the tunneling in the OFF-state occurs along the high $m^*$ axis and results in a very low $I_{OFF}$. Hence, this new TFET design can revive Moore’s law for sub-10 nm TFETs.

Figure 1. The band diagram of (a) 12 nm long GaAs, (b) 5 nm long GaAs, and (c) 5 nm long phosphorene MOSFETs. The colormap shows the transparency of the channel. The potential barrier in the 5 nm long GaAs MOSFET is transparent and hence, the gate efficiency is low. This problem can be solved by using phosphorene with high $m^*$.
In this work, phosphorene nanoribbon has been chosen as the channel material since it has a large effective mass anisotropy in zigzag and armchair directions. The electron and hole effective mass values of phosphorene along zigzag and armchair directions calculated from our tight-binding method (TB) and DFT calculations from literature (HSE0626 and PBE27). Table 1.

|         | $m_{e,arm}$ | $m_{e,zig}$ | $m_{h,arm}$ | $m_{h,zig}$ | Ref.   |
|---------|--------------|-------------|-------------|-------------|--------|
| 1L      | 0.17         | 1.09        | 0.15        | 5.84        | TB     |
|         | 0.17         | 1.12        | 0.15        | 6.35        | HSE0626|
|         | 0.14         | 1.23        | 0.13        | 13.09       | PBE27  |
| 2L      | 0.17         | 1.13        | 0.14        | 2.8         | TB     |
|         | 0.18         | 1.13        | 0.15        | 1.81        | HSE0626|
|         | 0.11         | 1.35        | 0.1         | 2.18        | PBE27  |

Table 1. The electron and hole effective mass values of phosphorene along armchair and zigzag directions calculated from our tight-binding method (TB) and DFT calculations from literature (HSE0626 and PBE27).

Figure 2. (a) The device structure of the bilayer phosphorene TFET with L-shaped gate. (b) The main tunneling paths in the ON-state (blue arrows) and OFF-state (red arrows) of the phosphorene TFET.
As mentioned before, ultra-scaled MOSFETs require large $m^*$ and $E_g$ to block source-to-drain tunneling. Hence, 1L-phosphorene nanoribbon has been chosen here which has the highest $m^*$ and $E_g$ compared to multi-layer phosphorene. The schematic of the 1L-phosphorene MOSFET has been shown in Fig. 4a. The supply voltage is fixed to 0.5 V, much higher than $V_{DD}$ of TFETs, since the Boltzmann limit of subthreshold swing in MOSFETs (i.e. 60 mV/decade in room temperature) does not allow the scaling of $V_{DD}$.

The transfer characteristics of a short channel 1L-phosphorene ($L_{ch} = 3$ nm) with transport direction along low $m^*$ (armchair) and high $m^*$ (zigzag) are compared in Fig. 4b. As expected, the gate efficiency of a phosphorene MOSFET is much better when the high $m^*$ (zigzag) axis is along the transport direction. This better gate efficiency improves the subthreshold slope of MOSFET significantly.

Figure 4c shows $I_{DS}-V_{GS}$ of zigzag scaled phosphorene MOSFETs with channel lengths from 12 nm to 1.6 nm. Notice that for phosphorene MOSFETs with $L_{ch} > 1.6$ nm an $I_{ON}$ larger than 1.1 mA/μm and an $I_{ON}/I_{OFF}$ ratio larger than $10^6$ have been achieved. 1L-phosphorene MOSFETs show a significant advantage over other 2D materials whose performances are diminished below 5 nm channel lengths.

MOSFETs with long channels do not suffer from source-to-drain tunneling. Accordingly, a high transport $m^*$ is not required for blocking this leakage current. Actually, in long channel regime, a low transport $m^*$ can be beneficial and enhance the ON-state performance of the transistor since it leads to a higher carrier injection velocity. Figure 4d shows $I_{ON}/I_{OFF}$ ratio of phosphorene nanoribbon MOSFETs as a function of $L_{ch}$ along zigzag and armchair transport directions. Although zigzag nanoribbon MOSFETs significantly outperform the armchair ones in short channels due to lower source-to-drain tunneling, armchair nanoribbon MOSFETs show a better performance in longer channels due to higher injection velocity. There is a critical channel length (i.e. 6 nm in 1L-phosphorene) in MOSFETs below which having a high $m^*$ becomes critical and above which a low $m^*$ is beneficial.

In summary, the channel materials with anisotropic effective mass can be used to design transistors scalable to 1–2 nm channel lengths. In MOSFETs, the high effective mass along transport direction blocks the direct source to drain tunneling and low effective mass reduces the quantum capacitance and switching delay. On the other hand in TFETs, a novel L-shaped gate design is proposed which can provide advantage of high tunneling rate in the ON-state and low tunneling rate in OFF-state by engineering the tunneling paths along low and high effective mass directions. In summary, anisotropic effective mass can be used in an L-gate design to obtain large ON/OFF ratio in an ultra-scaled homojunction TFET.

Figure 3. (a) The comparison between $I_{DG}-V_{GS}$ of conventional 2L-phosphorene nanoribbons along zigzag and armchair directions with that of the L-gate TFET. (b) ON-current and SS of L-gate TFET as a function of $dL$.
(c) Impact of channel length scaling on $I_{DG}-V_{GS}$ of L-gate TFETs. (d) $I_{ON}/I_{OFF}$ ratio of the L-gate TFET as a function of $L_{ch}$. (e) The top view of edge-less L-gate design.
Methods

The atomistic quantum transport simulation results have been obtained from the self consistent solution of 3D-Poisson equation and Non-equilibrium Green’s Functions (NEGF) method using the Nanoelectronics modeling tool NEMO530,31. The Poisson equation provides the potential for NEGF method and takes the free charge in return. The tight-binding Hamiltonian of phosphorene used in NEGF calculations employs a 10 bands $sp^3d_5s^*\text{model}$. Phosphorene is a material with anisotropic dielectric properties. The details of the Poisson equation with anisotropic dielectric tensor and NEGF equations can be found in our previous works21,22,36,37.

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Author Contributions
H.I. came up with the idea of the L-gate TFET. H.I., T.A. and B.N. worked on the atomistic simulations and analyzed the data. Y.T. provided the tight-binding model for phosphorene. G.K. and R.R. supervised the work. All authors contributed to writing the manuscript.

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