Robustness Evaluation for Harmonic Suppression of LCL-Type Converter Based on Converter-Side Current Feedback Strategy Under Weak and Distorted Grid

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Abstract—Due to the existence of grid impedance, the grid voltage often contains low order background harmonics, which will deteriorate the current quality of grid connected converters. In view of this situation, considering the delay effect and weak grid, the robustness of two single loop control modes of LCL-type grid connected converter, namely grid-side current feedback (GCF) and converter-side current feedback (CCF), is evaluated to improve the current quality of the grid current under distorted grid. Through the analysis and demonstration of above impedance models, CCF has the advantages of excellent stability and excellent power quality. Then, a direct harmonic suppression strategy based on CCF is proposed. The strategy takes the converter side current which contains richer low harmonic as harmonic information source, and the control effect is more effective than the traditional strategy which uses capacitor current as harmonic information source. Without additional control strategy and controller, the hardware cost is reduced and algorithm complexity is simplified. The simulation and experimental results verify the correctness and feasibility of the theoretical analysis.

Index Terms—Grid current, harmonic suppression, LCL-type converter, robustness, voltage distortion.

I. INTRODUCTION

In recent years, renewable energy solutions based on the usage of wind power and photovoltaic panels have been widely studied and used in power system. Due to the long-distance distribution of the source and load (SL) in renewable energy power systems, the transmission line impedance and transformer leakage reactance have to be taken into account. The point of common coupling (PCC) is a common point of weakness in the grid [1]–[2]. This may lead to stability and power quality problems of grid connected converter. Namely, the low-order harmonics generated by a non-linear load leads to the background voltage harmonics at the PCC due to the grid impedance, which further affects the connection between the grid and converter. In addition, the high-order switching harmonics generated by the operation of the equipment connected to the power electronic grid further degrade the grid power quality [3]–[4].

The LCL-type converters have been widely used in renewable energy grid-connected systems due to their excellent performance in high-frequency harmonic attenuation [5]. However, the phenomenon of resonance exists due to the circuit structure of the LCL-type converters. The active damping method can be employed to avoid these problems such as high hardware cost and reduced power transmission efficiency caused by passive damping method [6]–[15]. Besides, the performance of the control system should be studied considering the digital delay, which causes a phase lag in the control system and threatens system stability and anti-disturbance ability. For the converter-side current feedback (CCF) and grid-side current feedback (GCF), stability can be achieved without using a damping strategy if specified digital delay requirements are met [8],[16]. Many measures have been proposed by scholars to reduce the delay, including the double sampling method, the impedance reshaping method and the pole-zero delay compensation method [14]–[17]. An improved sampling technique is proposed in [14], which can reduce the delay time by sampling the signal twice in each carrier cycle. By adopting the state observer, the signal of the previous cycle can be used to predict the signal of the next cycle, so as to reduce the sampling delay caused by digital delay. However, this method requires additional computing resources, and the observer is extremely sensitive to the small range variation of parameters. For example, the parameter values of resistance and inductance will change with the length of current passing time, which may lead to estimation or prediction error [15]. The delay effect can also be effectively reduced by adding low-pass filter [5] and sampling reconstruction [14]. In addition, there are many researches on
converter performance and delay compensation methods in weak grid environment. Among them, reference [16] mainly focuses on the influence of weak grid on the inherent resonant frequency of LCL converter, so as to improve the stability of control system. However, the method to reduce the delay is still double sampling method, which is similar to reference [14]. It should be noted that they will increase the complexity of the control algorithm and the burden of experimental calculation.

In terms of power quality, voltage distortion has an important impact on the control performance of LCL converter. A full voltage feedback control strategy is proposed in reference [7], which achieves ideal harmonic suppression effect theoretically. In fact, proportional voltage feedback can not only suppress most of the low order harmonics, but also improve the dynamic response of the control system. However, in the absence of selective harmonic suppression, low order harmonics, that is, below 10th order harmonics, are suppressed, and the attenuation ability decreases with the increase of harmonic order. Repetitive controller is used to suppress the target harmonic. However, the repetitive controller is more sensitive to noise and has infinite gain at Nyquist frequency [11]–[12]. According to the special structure of LCL converter, the capacitor current is used as the harmonic information source in reference [18]. However, the equivalent circuit model shows that there are many low order harmonics and fundamental frequency currents flowing through the LCL structure under the non ideal grid conditions, which is worthy of further exploration and improvement. In the existing research, there is rarely in-depth analysis on the LCL structure multi loop impedance models, and the influence of distorted voltage on the circuit is not discussed. In addition, for the traditional strategy [18], the input state variable of harmonic controller (HC) represents is sum of converter side current and capacitor current. The control effect may be masked by the converter side current. In addition, in the closed-loop control system, the control of capacitor current will reduce the stability of the system [19], [20].

To address all the mentioned problems, in this paper, a direct, simple and effective strategy has been proposed to enhance the robustness of the LCL-type converter when the grid voltage contains background harmonics. By using the proposed strategy, the quality of the grid-into current can be improved without using an additional sensor to sample the capacitor current.

The main contributions of this paper can be summarised as follows:

i. The delay effect and the digital delay reduction methods are considered, and the reasons for selecting CCF as a control method in this paper are expanded and analysed.

ii. The impedance models of two different loops of the LCL structure under the condition of grid distortion, which are referred to as harmonic impedance models in the following sections, are analysed in-depth. The analysis results indicate that in the distorted grid, at lower-order harmonics, the inductor loop provides richer and more accurate information on harmonics than the capacitor loop.

iii. The change in the converter stability with the adoption of the capacitor current is investigated, and a simple and effective strategy is proposed to suppress the low-order harmonics caused by grid distortion.

The remaining of the paper is organised as follows: In Section II, a mathematical model of the LCL-type converter with a digital delay is introduced. The impedance models under the distorted grid condition are analysed in detail in Section III. In Section IV, the harmonic suppression mechanism and the stability of a system using the traditional control strategy and the proposed control strategy are investigated, and an effective strategy is proposed. In Section V, the simulation and experimental results verify the proposed strategy. Finally, the main conclusions are drawn in Section VI.

II. MODEL OF LCL-TYPE CONVERTER WITH DIGITAL DELAY EFFECT

The structure of the LCL-type grid-tied converter is shown in Fig. 1, and the special parameters of the main and control circuit are given in Table I.

![Fig. 1. Structure of the LCL-type grid-tied converter.](image)

| TABLE I |
|---|
| **PARAMETERS OF THE MAIN AND CONTROL CIRCUITS** |
| Parameter | Value | Parameter | Value |
|---|---|---|---|
| \(U_g\) | 80 V | \(K_p\) | 0.12 |
| \(L_1\) | 1.5 mH | \(K_i\) | 53 |
| \(L_2\) | 1.5 mH | \(k_{HC}\) | 300 |
| \(C\) | 10 \(\mu\)F | \(w_c\) | 25 |
| \(U_{dc}\) | 200 V | \(L_c\) | 3 mH |

In Fig. 1, \(i_1, i_2\) and \(C\) denote the converter-side current, the grid-side current and the LCL structure capacitor, respectively. \(C_{dc}\) denotes the DC side capacitor, and \(Z_g\) denotes the impedance of the grid, which represents the weakness of the grid. The delay link represents the overall time delay including the delays caused by analog-to-digital conversion, controller computation, duty-ratio update and pulse with modulation (PWM) delay. The control structure mainly analyzed in this paper is Fig. 1. Furthermore, the related description and
improvement of the control structure in Fig. 1 will be described later.

The zero-pole figures of the closed-loop trans-function of the GCF and CCF are displayed in Fig. 2, where it is shown that the performances of the GCF and CCF are inversely affected by the delay. In the theoretical analysis and simulation, the Pade function and Taylor formula have been used to approximately equivalent exp(−sTₙ) in s domain.

Unlike the CCF, in the case of the GCF, as Tₙ increases, the system transitions from stable to unstable. In other words, an appropriate delay value is beneficial to the GCF stability, although this is in conflict with the original goal of reducing the delay to enhance converter robustness. In addition, increasing the delay can lead to the phase lag, which potentially threatens system stability. The stable frequency interval of the GCF is f_res ∈ (fₙ/6, fₙ/2), where f_res represents the resonance frequency, and fₙ represents the sampling frequency [21], [22].

Generally, as shown in the blue line in Fig. 3, f_res decreases with the grid impedance Zₙ increases. The resonance frequency is likely to reduce below the critical value due to variations in grid impedance under weak grid conditions. The larger the impedance of the power grid is, the weaker the power grid is and the smaller the resonance frequency is. The larger value of the impedance is, the weaker grid is and the smaller the resonance frequency is. When the critical frequency remains unchanged, it is easy for GCF to cross the critical frequency. At this time, the system changes from stable to unstable, and the greater the impedance of the power grid, the greater the risk of instability. For CCF, the increase of grid impedance is beneficial to system stability.

The stable interval of CCF is f_res ∈ (0, fₙ/6). At the same time, current protection also requires a converter-side current. In [23], the authors proposed a simple and effective unit delay feedback strategy to mitigate the negative effects of delays, the method is adopted in this paper to alleviate the potential instability caused by time delay and grid impedance. The unit delay feedback strategy is shown in Fig. 3. Here is a brief description. The phase near the resonance frequency decreases due to the delay. According to the theory of unit negative feedback in automatic control theory, the most direct way is to connect a lead-lag link in the equivalent delay link of the system in view of the delay effect. The design goal of this link needs to achieve the following effect: The phase at the resonant frequency should be raised. At the same time, the low frequency gain can be guaranteed when the phase lag caused by the delay link is relieved. Considering the above factors, [23] constructs a unit delay feedback link, which is the strategy used in this paper and it will not be discussed in detail in this paper. In Fig. 4, which is a simplified graph of Fig. 1, G_c denotes the overall delay of the control system, G_c denotes the current controller, which is a PR & HC controller, and λ represents the coefficient of the unit delay feedback strategy. The one-order high power filter H_{CCF} could be adopted when necessary.
Based on Fig. 4, the following equations can be obtained.

\[ G_i(s) = e^{-\frac{s}{\tau_p}} \quad (1) \]
\[ i_1 = \frac{G_i(s)G_e(s)e^{-\frac{s}{\tau_p}}}{1 + G_i(s)G_e(s)e^{-\frac{s}{\tau_p}}} - \frac{G_i(s)G_e(s)e^{-\frac{s}{\tau_p}}}{1 + G_i(s)G_e(s)e^{-\frac{s}{\tau_p}}}u_s \quad (2) \]
\[ i_2 = \frac{G_i(s)G_e(s)G_2(s)e^{-\frac{s}{\tau_p}}}{1 + G_i(s)G_e(s)e^{-\frac{s}{\tau_p}}} - \frac{G_i(s)G_e(s)G_2(s)e^{-\frac{s}{\tau_p}}}{1 + G_i(s)G_e(s)e^{-\frac{s}{\tau_p}}}u_s - \frac{G_i(s)G_2(s)G_1(s)e^{-\frac{s}{\tau_p}} + sCG_i(s)G_e(s)G_2(s)e^{-\frac{s}{\tau_p}} + sCG_2(s)}{1 + G_i(s)G_1(s)e^{-\frac{s}{\tau_p}}}u_s \quad (3) \]

where,

\[ G_i(s) = \frac{s^2}{sL_1L_2C + s(L_1 + L_2)} \quad (4) \]
\[ G_e(s) = \frac{1}{sL_2C + 1} \quad (5) \]
\[ G_i(s) = K_p + \sum_{i=1,3,5,...}^{\infty} \frac{K_{HCi}s}{s^2 + w_i^2s + w_i^2} \quad (6) \]

In (1)–(6), \( G_i(s) \) represents the PR&HC controller that consists of the PR and HC sub-controllers; the PR represents the proportional-resonance controller, where \( K_p \) denotes the proportional coefficient, \( w_c \) denotes the bandwidth coefficient, and \( w_0 \) denotes the fundamental angular frequency; the HC represents the harmonic controller that is connected in parallel with the PR, and where \( K_{HCi} \) denotes the gain and \( w_i \) denotes the harmonic-order angular frequency.

III. IMPEDANCE MODEL OF LCL-TYPE CONVERTER IN DISTORTED GRID

Similar to a person with weak health who is prone to illness, a weak grid is highly susceptible to the background harmonic voltages, which can lead to a low-quality grid current. Based on (3), the impedance model under the condition of grid distortion or grid harmonics can be expressed as:

\[ Z_k = \frac{u_k}{i_k} = \frac{1 + G_i(s)G_e(s)e^{-\frac{s}{\tau_p}}}{G_i(s)G_e(s)e^{-\frac{s}{\tau_p}} + sCG_i(s)G_e(s)G_2(s)e^{-\frac{s}{\tau_p}} + sCG_2(s)} \quad (7) \]

The equivalent circuit model of grid connected converter can be obtained, and it is shown in Fig. 5. As presented in Fig. 5, there are two loops for the voltage harmonics, loop A and loop B, which can be presented in the form of harmonic currents. When the voltage at PCC point is distorted, the harmonic voltage will flow through two loops in the form of harmonic current through the output impedance of the converter. At this time, the impedance characteristics of each loop determine the content or proportion of harmonic current in the loop. Also, in Fig. 5, \( K_p \) denotes the proportion gain of the PR controller; \( C_{PR} \) and \( L_{PR} \) denote the capacitor and inductor respectively in the equivalent circuit model of the PR controller; \( C_{HC} \) and \( L_{HC} \) respectively denote the capacitor and inductor in equivalent circuit model of HC controller, where \( i \) denotes the ith order harmonic.

Considering the controller, the impedance frequency domain analysis of the two loops is shown in Fig. 6. When the harmonic frequency is lower than 750 Hz, the amplitude gain or admittance of loop A is higher than that of loop B, and the harmonic current mainly flows through loop A. The traditional control strategy of LCL converter uses the capacitor current as harmonic source whose frequency domain characteristic is loop B [16], [18], [22]. However, loop B presents high impedance characteristics in the low frequency domain, and only the frequency harmonic currents above 750 Hz are allowed to pass through. In practice, the voltage background harmonics are mostly within the 15th harmonic [2], [14]. According to Fig. 6, most of the harmonic current flows to loop A and a small part of that to loop B. The harmonic information in loop A is more abundant and accurate. When control system samples the loop A current, the harmonic information can be obtained more accurately, and the harmonic in grid current could be suppressed more effectively.

Fig. 7 shows the path diagram of all order harmonic currents according to above mentioned. Loop F denotes the current channel in fundamental frequency region, Loop R denotes the current channel in resonance frequency region, and Loop H
denotes the harmonic frequency current channel caused by the background harmonics of voltage.

The frequency domain characteristics of the circuit model determine the main flow direction of the harmonic current, the above analysis is the theoretical basis of the strategy proposed in the next section.

IV. PROPOSED GRID-CURRENT QUALITY ENHANCED STRATEGY FOR CCF CONTROL SYSTEM

A. Harmonic Suppression Mechanism and Stability Analysis

In this paper, an HC is employed as controller to suppress grid current with low-order harmonics caused by distorted voltage at PCC. Fig. 8 shows bode of traditional harmonic suppression strategy. That is, the harmonic source comes from the capacitor current of loop B. In Fig. 8, $Z_{g1}$ denotes the traditional strategy with the PR & HC controller, which are composed of HC5, HC7 and HC9. Then, $Z_{g0}$ denotes the harmonic suppression strategy with a PR controller, which uses the $i_c$ in loop A as the information source of harmonic for controlled.

In additional, series resonance is stimulated by $Z_{g1}$, C and $L_2$ in loop B in Fig. 8. This may lead to the unstable operation and even weaken the control system robustness. Furthermore, $f_0$ represents the fundamental frequency, $f_{H}$ represents the harmonic frequency of the HCs, which, in this paper, is composed of HC5, HC7 and HC9, and $f_s$ represents the series resonance frequency of loop B, where:

$$f_s = \frac{1}{2\pi} \sqrt{\frac{1}{CL_2}}.$$  (8)

When the traditional strategy is adopted, the introduction of $i_c$ into the control loop can bring hidden dangers to system stability, Fig. 9 shows the related control structure. Based on the structure of Fig. 1, an independent analysis of branches of $i_c$ is conducted in this section. In Fig. 9, the symbol $w$ represents the resonance angle frequency, and its expression is shown in (9). In addition, the loop formed by red dotted lines represents the signal loop when the capacitor current is used as a harmonic information source, and its root locus is shown in Fig. 10.

$$w = 2\pi f_{ms} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}}.$$  (9)

In Fig. 10, obviously, the root locus of the control system is always outside the unit circle when the delay effect is considered, which may lead to the system unstable. Therefore, the capacitor current maybe an unstable factor in control system, and it is not a perfect method to mitigate the negative effects caused by distorted voltage.

B. Proposed Grid Current Enhanced Quality Strategy

As shown the control structure in Fig. 9, before the controlled signal enters the controller, the input signal of HC is the sum of converter-side current $i_1$ and capacitor current $i_c$. Based on the analysis in Section II, it could be noted that the only a small amount of low order harmonics carried by $i_c$ and it may lead to instability. In this paper, the $i_c$ is to be adopted as the harmonic current information source. The bode figures of the related open-loop system are shown in Fig. 11, where the $Z_{g0}$ denotes the converter output impedance with the proposed strategy. For comparison, the curve $Z_{g1}$ in Fig. 8, which is represented by the green line, is also redraw in Fig. 11.

Obviously, it can be seen from Fig. 11 that the series resonance frequency caused by loop B has been suppressed, and the proposed strategy ensures a high gain in the fundamental frequency region. The phase frequency curve passes through the zero axis once in the positive and negative directions, the Nyquist stability criterion is satisfied. In addition, by adjusting the gain and bandwidth coefficients, as well as by adding HCs, the same effect of low order harmonic...
current suppression could be realized either.

The loop formed by red solid lines in Fig. 8 represents the signal loop when the converter-side current is used as a harmonic information source. Fig. 12 shows the root locus with the proposed strategy. Compared with the traditional strategy, the proposed strategy does not need sample $i_c$ to form a closed-loop control loop. On the premise of ensuring sufficient low-frequency gain, the root locus falls within the unit circle. Simultaneously, the method reduces the sensitivity to system parameters. When the control parameters are adjusted in a wide range, the system is still stable. So the strategy effectively optimizes the control performance of the grid-tied converter, and improves the stability of the control system.

V. Case Studies

A. Simulation Results

The simulation model was established using PLECS and Matlab/Simulink to verify the previous analysis. The related parameters are listed in Table I. In order to verify the effectiveness of the proposed strategy, the 30% of the 7th order harmonic is injected into the ideal
grid voltage to simulate a distorted and weak grid within background harmonics. Fig. 13 shows the grid voltage $U_g$, the grid current $i_2$ and the capacitor current $i_c$ under distorted grid conditions without any control strategy. Obviously, the background voltage harmonics significantly worsened the quality of the grid current.

Furthermore, according to Fig. 13, the results of FFT analysis for $i_2$ and $i_c$ are shown in Fig. 14. Fig. 14 (a) shows the FFT analysis results of $i_2$. Except for the fundamental frequency current, the 7th order harmonic content is the highest, about 2 A. The resonance frequency is 1.84 kHz. At this time, the THD of $i_2$ is 21.5%, which is seriously affected by the distorted grid. Fig. 14 (b) shows the FFT analysis results of $i_c$. The resonance current content in $i_c$ is the highest, while the 7th order harmonic content is relatively small, about 0.3 A. The content of low frequency harmonics in $i_c$ is much less than that in $i_2$. Which is consistent with the above theoretical analysis.

When the traditional strategy is adopted, that is, the capacitor current $i_c$ in loop B is used as the harmonic information source for harmonic suppression. The waveforms of grid current and voltage at PCC are shown in Fig. 15. It is not difficult to see that compared with Fig. 13, when the traditional strategy is adopted, the harmonics of grid current is effectively suppressed and the waveform quality is improved. However, the overall THD of current waveform is still large, which indicates that the control effect of traditional strategy is limited. In addition, there is still a risk of periodic instability, and the control system needs further optimisation.

When the proposed strategy is adopted, that is, $i_1$ in loop A is sampled as harmonic information source for harmonic suppression. The waveforms of grid current and voltage at PCC are shown in Fig. 16. Compared with Fig. 15, when the proposed strategy is adopted, the harmonic of grid current is effectively suppressed and the waveform becomes highly sinusoidal. The overall distortion rate of the current waveform is small, which shows that the proposed strategy improves the limitation of the traditional control strategy. Without increasing the complexity of the controller, the harmonic suppression effect is realized more effectively. Furthermore, the convergence has been improved and stability of the current waveform has also been enhanced.

To further illustrate the effectiveness of the proposed strategy,
Fig. 16. The waveform of the grid current and PCC voltage of the distorted grid when the proposed strategy is used.

Fig. 17 shows the FFT analysis results of the current waveform in Figs. 15 and 16. At this time, compared with Fig. 14(a), THD of grid current is significantly reduced due to the effective suppression of 7th order harmonic as shown in Fig. 17(a).

Howeover, according to the above analysis, it is difficult to make THD meet the requirements of grid connection standard due to the limited suppression effect of traditional strategy. By comparison, Fig. 17(b) shows the FFT analysis results of grid current with the proposed strategy. On the basis of Fig. 17(a), the lower order harmonics are further suppressed and the overall THD of the current is further reduced. It shows that the controller has more targeted and better effect on harmonic suppression by using state variables with more abundant harmonic content in loop A.

B. Experimental Results

The experimental setup is shown in Fig. 18. In the experiments, the control strategy and algorithm were realised using the dSPACE DS1104 platform, and the non-ideal grid and DC source were implemented using Chroma 61511 and Chroma 62150H-1000, respectively. The LEM LV28-P and LEM LT208-S7/SP1 were used to sample the state variables such as voltage and current at PCC. A K75T60 series insulated gate bipolar transistor (IGBT) produced by Infineon, was used as a switching link in the experimental platform. The experimental parameters are given in Table I.

Here are the experimental results. Fig. 19 shows the current waveform and voltage waveform at PCC point under the ideal grid condition. The pink curve is the result of FFT analysis of phase A current. It can be seen that even in the ideal grid condition, there are still a lot of low order harmonics in the current waveform, among which the 7th order harmonic content is high most.

Fig. 20 shows the waveforms of grid current and voltage when the grid voltage contains the 7th order harmonic. Fig. 21 shows the corresponding capacitor current waveform. In the above two figures, the working condition at this time is consistent with that in Fig. 13. In Fig. 20, the grid current is seriously distorted by the distorted grid voltage, which contains a large number of voltage background harmonics. According to the FFT results, the 7th order harmonic is the main reason for its distortion. In Fig. 21, the capacitor current content is small, and the 7th order harmonic contained in it is approximately
It shows that the background harmonics of the grid voltage mainly flow through the inductor loop in the form of low-frequency harmonic current, and the capacitor current mainly provides the path for the high-frequency current. The low frequency harmonic content of the former is higher than that of the latter.

Figs. 22 and 23 show the waveforms of grid current and voltage at PCC after adopting the traditional strategy and the proposed strategy respectively. It can be seen that in Fig. 22, the traditional strategy can effectively suppress the 7th order harmonic of grid current and restore its waveform to sinusoidal. However, due to the limited low order harmonic content of the harmonic information source, it is difficult for the controller to effectively control the low order harmonic. In addition, the control system also has the risk of instability. In Fig. 23, after using the proposed strategy, the 7th order harmonic can be suppressed to the greatest extent, the current waveform is highly sinusoidal, and the grid current waveform is equivalent to that under the ideal grid condition. It shows that the proposed strategy shows the enhanced robustness even when the grid voltage contains background harmonics.

Furthermore, in order to verify the dynamic characteristics of the proposed strategy before and after enabling. Fig. 24 shows the experimental results of $i_1$, $i_2$ and grid voltage when the proposed strategy is enabled, the current quality of loop A is significantly improved and the harmonics are effectively suppressed. Similarly, Fig. 25 shows the experimental results of three-phase current. It can be seen that after the proposed strategy is enabled, the current waveform has almost no impact and the transient characteristics are good. This shows that the proposed strategy has better transient stability.
Fig. 24. Single phase of the grid current and voltage when the proposed strategy is adopted.

Fig. 25. Grid current and PCC voltage when the proposed strategy is adopted.

Fig. 26. Comparison of the simulation and experimental results.

C. Result Analysis

Table II shows the comparison of the unit value (p.u.) of the seventh-order harmonic current in the grid current and the THD of the grid current based on the experimental and simulation results.

| Case   | 1     | 2     | 3     | 4     |
|--------|-------|-------|-------|-------|
| Simulation | 0.012/1.4 | 0.21/21.5 | 0.078/19 | 0.035/4.33 |
| Experimental | 0.03/3.1 | 0.29/31 | 0.08/9.2 | 0.042/4.8 |

P.u.: the seventh-order harmonic/THD (%).

VI. CONCLUSION

In this paper, the impedance model of different loops in the LCL-type converter is introduced and analyzed in detail to find a simpler and more effective method to improve the quality of the grid current under the distorted grid condition. Firstly, the stability of the two control modes of GCF and CCF is elaborated, and the superiority of CCF is demonstrated. In addition, for the traditional harmonic suppression method of CCF, a theoretical analysis is carried out, and the limitation of using traditional capacitor current as a harmonic information source is analyzed. Furthermore, a direct harmonic current control method is proposed as a supplement to the traditional control method. Compared with traditional control methods, this strategy uses fewer sensors and greatly reduces hardware costs. Due to the simple structure and accurate harmonic information, its performance is better than traditional strategy in terms of grid current quality and system stability. The experiment proves the advantages and effectiveness of the proposed strategy. Related results show that this strategy has better control effect than traditional control strategy.

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