Comparison between Conventional Fast Multipliers and Improved Fast Multipliers using PTL Logic

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Abstract. Multiplier circuit is an important element in majority of the arithmetic operations. In the domain of VLSI industry, obtaining low power consumption by the components and high speed has become a crucial concern for the IC designers. It plays a crucial part in the speed of the ALUs and DSP and dissipates an enormous amount of power. Consequently the functioning operation of the desired circuit can be enhanced by its optimization. By using shift and add operation the multiplication process is also implemented in hardware. So we improved the multiplier with the use of efficient adder circuit. In this paper, the circuits are simulated in Cadence Virtuoso using 90nm technology. The proposed array multiplier circuit and Wallace tree multiplier offers a reduction of approximately 56% and 91% in power consumption and approximately 48% and 90% in product of power and delay respectively.

1. Introduction

With the increase in integration scale, a lot of advanced and compact signal processing systems area unit are required to be actualized on VLSI chip. Processing involve in these applications consume high amount of power and need sensible computation capability. With performance as well as area, power dissipation has also become an additional concern issue for the designing of integrated circuits. There are basically two major factors which led to this building of low power systems. Firstly, increase in the integration which led to increase in processing capacity due to which huge amount of flow of currents takes place that leads to heating up of the chip. And secondly, in portable electronic devices the battery life is restricted and hence prolonged operation of those portable devices are often obtained by achieving low power design. It is known that in most of the signal processing algorithms, multiplication shows an elementary role to play. The performance of system is usually dependent on the multiplier’s performance, as a result multiplier has greatest delay within the system. However, it also consumes most of the area of that system. Hence, enhancing its speed and optimizing its area could also be a serious design issue. All the multipliers use full adders and hence are often optimized using the modified full adders. Here in this paper, we have simulated a proposed and a compact PTL Multiplier structure to fulfil daily needs of high speed applications which consumes low power. Here, improved adder designed and implemented using pass transistor logic is used for the proposed multiplier having 90nm technology. The proposed adder consumes lesser power and area than that of conventional techniques as discussed in literature. The paper consist of following sections which are as follows: Section 2 and 3 discuss the conventional approaches. Section 4 presents the proposed Wallace Tree structures and Array circuit. The Working is discussed in 5th section and results are compiled in 6th section. The last section is conclusion.
2. Wallace Tree Multiplier

The major design consideration for any chip designer are delay, area and power consumption. Speed of the system is totally dependent on the delay of the multiplier. Therefore, to improve the speed of multiplier many research has been done. Wallace Tree has serious significance in high speed applications because of great speed and area efficient multiplier [2]. It multiplies integers using the column compression technique that implements simple and efficient hardware methodology for Wallace multiplier. As compare to array multiplier having linear dependency, Wallace tree offers a quick speed which results in the entire delay is directly proportional to the logarithm of length of word of the operand of multiplier.

Steps involve for the operation of Multiplier are mentioned below:

First: Formation of partial products,
Second: Grouping of those formed partial products,
Third: Addition using adders.

To improve the performance of multipliers numerous analysis and research has been done [3-9]. In Wallace multiplier, to reduce the area and latency both encoding with compressor approach is employed [4]. In conventional multiplier, a full adder circuit is built using 4:1 multiplexer [7]. In [8], full adder circuit is built using 2:1 multiplexer which also results in reducing power. These approaches of implementing full adder has led to power reduction but results in the critical path delay which is more than that of [9] Wallace tree multiplier. From all the previous literature review of multipliers, [9] offers the finest performance that are based on ground of area, power and its speed. The Figure below shows the full adder employed in [9].

![Fig. 1: Conventional Full Adder](image)

3. Array Multiplier

Array multiplier is easier to design because it is very regular in structure. "For multiplication of unsigned numbers Array multiplier is used. Half adders and full adders are connected in diagonally,
horizontally and vertically to obtain the partial products sum. Cin will be taken as ‘0’ if the implementation of partial product’s first row is obtained using only full adders. By simple routing, partial products are properly aligned. Partial products are added to the sum by each row of adders, generating an order of carriers and a new partial sum” [1]. n half adders, n (n-2) full adders and \( n^2 \) AND gates are required in a \( nxn \) Array multiplier.

Total time consumed by the signals to propagate through full adders, half adders and by each AND gate is the effective delay of the Array multiplier. They are very large in size and this is the main disadvantage of an array multiplier. Due to increase in number of operands, the array arise linear in size at a rate equal to the square of the operand size. In design the third input is considered as 0 if the full adder have two inputs data only. The array multiplier with Carry save addition is shown below in Figure 2.

![Fig. 2: Conventional Array Multiplier [1]](image)

4. Methodology

As mentioned above Wallace Tree multiplier and Array multipliers offers best speed compared to other multipliers, therefore we tried to compare both Wallace and Array multiplier based on their existing and proposed structure and various other techniques so to enhance its structure that are proposed in several researches [3-9]. In this paper, a modified structure of Wallace tree and Array Multiplier has been proposed and simulated which results more better performance as compared to existing approaches. The proposed schematics are designed taking care of to reduce the complexity algorithm [10-11] and modified adder sub-circuit which process the intermediate addition of bits. The Figure 4 shows the schematic of improved adder that is designed using Pass Transistor Logic which is based 2:1 multiplexer. Fig.3 shows the Pass Transistor Logic based 2:1 multiplexer. Because of PTL,
there is considerable decrease in number of transistors and area. Apart from this it has the best advantage of least static leakage. The short circuit power is also least because there is very few Vdd to ground connections during the switching. The full adder circuit modified expressions are given as following:

\[
\text{SUM} = A \oplus B \oplus C \\
= (A \oplus B) \oplus C \\
= (AB) + AB \oplus A \oplus AB C
\]

\[
\text{CARRY} = AB + BC + CA \\
= C(B + A) + AB \\
= C(B + A) + B + AB \\
= B(C + A) + AB \\
= BC + ABC + ACB \\
= B(B \oplus C) + A(B \oplus C)
\]

(Expression for Sum and Carry)

The sum and carry expression of improved adder circuit are given by Eq. (1) and Eq. (2)

5. Working

Working of the circuit is explained as follows and is verified from the truth table as shown below.

If B = C = 0/1 then Sum = A and Carry = B.
If B! = C then Sum = A! and Carry = A.

In this proposed structure, modified adder is employed having low complexity algorithm for multipliers [10-11]. On comparable to typical conventional multipliers during which both full adders and half adders are used to process three and two bits respectively, it only uses full adders until and unless the amount of stages remain adequate to that of conventional Wallace algorithm and similar too with Array multiplier. The Functioning operation of multiplier is not suffering from eliminating half adders as they don’t compress the amount of partial bits, two bits added gives two bits in output (Sum and Carry).
Fig. 3: Pass Transistor Logic Multiplexer

Table 1: Truth Table of Improved Adder

| A | B | C | Sum | Carry |
|---|---|---|-----|-------|
| 0 | 0 | 0 | 0(A) | 0(B)  |
| 0 | 0 | 1 | 1(¬A) | 0(A)  |
| 0 | 1 | 0 | 1(¬A) | 0(A)  |
| 0 | 1 | 1 | 0(A)  | 1(B)  |
| 1 | 0 | 0 | 1(A)  | 0(B)  |
| 1 | 0 | 1 | 0(¬A) | 1(A)  |
| 1 | 1 | 0 | 0(¬A) | 1(A)  |
| 1 | 1 | 1 | 1(A)  | 1(B)  |
Fig. 4: Schematic of improved adder

Fig. 5 shows 4x4 bit multiplication using low level complexity algorithm. It often seen that only S3 and C2 are processed as two its bits so that number of stages does not exceed the conventional approach of multiplication. The intermediate additions are performed by using the proposed adder.

![Schematic of improved adder](image)

Fig. 5: 4x4 bit Multiplication using reduced complexity Wallace Algorithm

All partial product rows of proposed Array multiplier are implemented identical to the conventional array multiplier but instead of conventional adder the improved adder is used. The use of improved adder led to considerable reduce in power consumption in array multiplier. Figure (6) shows the suggested Array Multiplier.
6. Results

The simulated results of circuits are shown below. Cadence Virtuoso is used by us using 90nm technology. Here various aspects of proposed adder has been compared with the conventional existing adder in table (2). Also result of proposed adder shown in Fig 7.

| Adder Circuit | Existing     | Proposed     |
|---------------|--------------|--------------|
| Logic used    | CMOS XOR gate + Mux | Pass Transistor Logic |
| Number of transistor | 56           | 18           |
| Power         | 0.124 mW     | 0.043 mW     |
| Delay         | 60.58 ps     | 48.48 ps     |
| Power Delay Product | 7.511        | 2.084        |

Table 2: Comparative Result of Adders
It is observed that the area i.e., number of transistors and therefore the delay of improved adder reduced considerably compared to the conventional adder. Simulated results of the proposed Array Multiplier and Wallace Tree Multiplier are shown below in Figure 8 and Figure 9 respectively. The Table.3 summarizes the obtained results of the Array Multiplier. It can be seen that number of transistors are considerably decreased in proposed Array Multiplier. Table.4 summarizes the obtained results of the Wallace Tree Multiplier. Due to less number of transistors the power dissipation in both proposed multiplier structures i.e. the power that is dissipated due to switching activity of the PT logic is less compared to power that is dissipated by the extra number of transistor in the conventional structures of the multipliers. Also the power delay product is a smaller in proposed multipliers as compared to the conventional multipliers.

| Array Multiplier | Existing   | Proposed |
|------------------|------------|----------|
| Power            | 0.389 mW   | 0.170 mW |
| Number of transistor | 1192      | 432      |
| Power delay product | 0.326    | 0.169    |

Table 3: Analysis of Array Multiplier Using PTL.

Fig. 8: Waveform of Array Multiplier
Table 4: Analysis of Wallace Tree Multiplier Using PTL

| Wallace Tree Multiplier | Existing  | Proposed |
|------------------------|-----------|----------|
| Power                  | 2.283 mW  | 0.192 mW |
| Number of Transistor   | 768       | 312      |
| Power delay product    | 473.72    | 46.28    |

Fig. 9: Waveform of Wallace Tree Multiplier

According to our study, using the pass transistor logic in the 2:1 mux, improved adder of both multipliers, the power dissipation, area and product of power and delay has been minimized by a considerable magnitude. This will results in the increase in demand for greater speed with minimal battery usage and cover less area. This improved adder proves beneficial in all the applications that performs mathematical operations using multiplier which are used in ALU’s and Digital Signal Processors.

7. Conclusion

In this paper, the improved output results of the conventional full adder were proposed along with conventional multipliers on the basis of number of transistor, power dissipation, product of the power and delay. Both multiplier has been studied and then modified multipliers circuit were proposed and simulated using 90nm technology in Cadence Virtuoso. Initially we simulated the inverter and the existing adder [9]. Then we simulated a new mentioned improved adder that uses the pass transistor
logic based 2:1 multiplexer. Here, the number of transistors employed in adder is comparatively less than existing adder. This results in the area which gets minimized and offers a less delay. The proposed Array Multiplier offers an improvement of 56.29% in reduction of power, 48.15% of reduction in power delay product and 63.75% diminishment in the number of transistors used i.e. area. The proposed Wallace tree Multiplier offers an improvement of 91.5% in reduction of power, 90.23% of diminishment in power delay product and 59.37% diminishment in the number of transistors. The consumption of power, area, and product of power and delay of the proposed Multipliers has been minimized by a considerable magnitude. Our proposed structures will prove beneficial in all the applications that perform mathematical operations using multipliers. Some of the applications in which it can be widely used are ALU’s and DSP structures [13-28].

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