A package-level wideband driver amplifier with 134% fractional bandwidth

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Abstract: A wideband package-level driver amplifier in 65 nm CMOS technology is presented in this paper. The inductor-less design is adopted for the inter-stage connection to achieve wide working bandwidth. Bonding wires for the package are modelled and used as the input/output matching networks to minimize the chip size. High-reliability design is adopted and ESD protection circuit, which is able to work under large output voltage swing, are integrated. The proposed amplifier works from 0.72 to 3.65 GHz with 134% fractional bandwidth. The amplifier has 27 dB power gain. The size of the chip is 0.63 x 0.68 mm².

Keywords: Power amplifier, package, CMOS, ESD

Classification: Microwave and millimeter wave devices, circuits, and systems

References

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1 Introduction

The absolute bandwidth of the wireless communication systems is growing fast with rapidly growing communication needs. Microwave and millimeter wave band, such as 28 GHz and 60 GHz [1], attract much attention, since the large available absolute bandwidth. However, the design complexity of the intermediate frequency (IF) and baseband (BB) amplifiers increases rapidly as the fractional bandwidth of these amplifiers are much larger than the microwave or millimeter wave amplifiers as shown in Fig. 1. For example, the 2 GHz absolute bandwidth occupies 7.1% fractional bandwidth at 28 GHz, which occupies 100% fractional bandwidth at the 2 GHz IF band. Several wideband amplifiers have been designed in [2-8] using the transformer matching, feedback technique or inductor-less design. A package-level wideband driver amplifier in 65 nm CMOS is presented in this paper. An improved inductor-less design is adopted for the inter-stage connection to increase wide working bandwidth. Bonding wires for the package are modeled and used as the input/output matching networks to minimize the chip
size. The proposed driver amplifier works from 0.72 to 3.65 GHz with 134% fractional bandwidth. The output referred P1dB is more than 1 dBm over the working bandwidth and is more than 5 dBm from 0.72 to 3.00 GHz.

![Microwave/millimeter-wave Front End Diagram](image)

**Fig. 1.** The diagram of the microwave/millimeter-wave front end

### 2 Wideband amplifier techniques

#### 2.1 Comparison of the wideband amplifier techniques

![Wideband Amplifier Techniques Diagram](image)

**Fig. 2.** The wideband amplifier techniques. (a) High-order matched amplifier. (b) Distributed amplifier. (c) Reconfigurable amplifier. (d) Inductor-less amplifier.

There are several techniques to realize the wideband amplifiers as shown in Fig. 2. The first commonly used technique is employing the high-order matching networks as shown in Fig. 2(a). The high-order networks consist of several pole points at different frequency points in the working band. However, the inductors occupy large chip area and increase the design complexity. The second technique is the distributed amplifier [8] as shown in Fig. 2(b). The distributed amplifiers have the ability to working from DC to the millimeter-wave band, yet with limited performance. Another technique is the reconfigurable amplifier as shown in Fig. 2(c). The matching network is switched to enable the amplifier to work at a broadband frequency range. Therefore, it is a pseudo wideband technique, which cannot amplify the wideband signal across several bands. Furthermore, the switch performance is limited at high frequency. Fig. 2(d) shows the inductor-less amplifier. Since there is no inductor to peak the gain, the inductor-less amplifier can have a broad power gain. However, the inductor-less amplifier cannot work at the high frequency and output large power.

#### 2.2 Improved inductor-less wideband amplifier

To improve the working band, a package-level wideband amplifier is proposed in
this paper as shown in Fig. 3. Four stages amplifiers are employed to have enough power gain. The inductor-less inter-stage connection method is used to enhance the working bandwidth. The bonding wires in the package are used as parts of the input and output matching networks to reduce the port reflection and increase the output power. Both the input and output ports are differential to avoid the influence the ground bonding wires. The differential signal lines is converted to the single-ended ports by the SMT baluns. ESD protection circuits are also integrated on the chip.

![The schematic of the proposed wideband amplifier.](image)

Fig. 3. The schematic of the proposed wideband amplifier.

The first two stages are used to amplify the input voltage and suppress the common mode signal. The common mode signal is generated by the imbalance of the balun and will be amplified by each stage. The unwanted common mode signal destroys the DC bias points of transistors and generates AC voltage drop on the ground bonding wires. Therefore, resistors are set at the common mode signal path, which is the virtual ground for the differential signals. The common-mode signals can be suppressed without influencing the differential signals. The third stage is used to amplify the voltage swing and drive the final power stage. The inter-stage connection is inductor-less to enhance the working bandwidth. If the frequency response of each stage amplifier is \( m \)-order Butterworth frequency response, the require GBW of \( n \) stage cells can be calculated from (1) [9].

\[
GBW_{\text{stage}} = \frac{BW_t}{2\pi \sqrt{2}} \sqrt{A_t}
\]  

(1)

The \( BW_t \) and \( A_t \) represent the bandwidth and gain of total amplifier, respectively. The biasing current and transistors’ size are determined by the GBW requirement and the drive ability. The final power stage uses the cascade structure to withstand high output voltage swing. An on-chip inductor together with the output bonding wires forms the high-order output-matching network. The network enables the high output power.

3 Package-Level Matching Network

In order to reduce the EM simulation time and increases the convergence of the circuit simulator, the input and output bonding wires are modeled using the lumped components in the circuit as shown in Fig. 4(a). Inductors \( L_1 \sim L_2 \) are used to model the self-inductance of the bonding wires. To model the frequency
dependent skin effect, the red R-L ladder circuits are in series with the $L_1 \sim L_2$. As the input and output differential bonding wires are closed with each other, there are capacitors ($C_{M1} \sim C_{M2}$) and mutual coupling ($M$) [10-11] between the inductors. There are also other parasitic capacitors ($C_{p1} \sim C_{p6}$). The coupling inductors form the wideband high-order matching networks with higher quality factor compared with the on-chip inductors. The differential signal lines connect to the SMT baluns on the package substrate as shown in Fig. 4(b). The SMT baluns convert the differential signals to the single-ended signals at the input and output ports.

![Fig. 4.](a) The lumped model of the bonding wires and (b) the 3-D view of the package-level matching.

![Fig. 5.](a) The schematic of ESD protection circuit and (b) the layout implementation.

4 ESD protection circuits
To protect the amplifier chip from destroying by the static electricity, ESD protection circuits are integrated on the chip as shown in Fig. 5. For the signal input ports, the diodes are set between the terminals and the VDD lines for the positive high voltage pulses. The diodes are set between the terminals and the GND lines for the negative voltage pulses. However, the voltage swing for the output ports is close to 1V, which will turn on the diodes. Therefore, the series diodes are used to enhance the turn-on voltage. The diodes are implemented by the PN junctions on the substrate and the layout is shown in the Fig. 5.

5 Measurement Result
The chip is fabricated in the 65 nm CMOS technology and the die photograph is shown in the Fig. 6. The chip size including all pads is 0.63 x 0.68 mm$^2$, while the core area is 0.30 x 0.68 mm$^2$. The supply voltage is 1V and the current for the
whole chip is 22.5 mA. The last stage consumes 14.4 mA current. The measured S-parameter including all of the bonding wires and the SMT baluns is shown in the Fig. 7(a). Benefiting from the inductor-less inter-stage connection and the high-order bonding wires matching network, the 3 dB working bandwidth is from 0.72 ~ 3.65 GHz with 134% fractional bandwidth. The power gain is 27 dB. Up to 4 GHz, the amplifier still has a gain more than 20dB. The measured output referred P1dB versus frequency is shown in Fig. 7(b). The output referred P1dB is more than 1 dBm over the working bandwidth and is more than 5 dBm from 0.72 to 3.00 GHz. The comparison of performance with wideband amplifiers is shown in Table I.

![Image](image_url)

**Fig. 6.** The die photo of the proposed wideband amplifier.

![Image](image_url)

**Fig. 7.** The measured (a) S-parameter and (b) OP1dB.

| Ref. | Tech. (nm) | Gain (dB) | $f_c$ (GHz) | BW-3dB (% ) | OP1dB (dBm) |
|------|------------|-----------|-------------|-------------|-------------|
| [6]  | 40         | 27.6      | 24          | 16.4        | NA          |
| [7]  | 28         | 20.8      | 43          | 65          | 13.4        |
| [12] | 28         | 13        | 53          | 65          | 12          |
| [13] | 65         | 30        | 66          | 51          | 16          |
| [14] | 40         | 22.4      | 63          | 23          | 16          |
| This work | 65         | 27        | 2.2         | 134         | 1           |

**6 Conclusion**

Inductor-less inter-stage connection and bonding wires matching techniques are used to enhance the driver amplifier’s working bandwidth. The package-level driver amplifier reaches 134% fractional bandwidth. ESD protection circuits are integrated on the chip.

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