On Transformations of Load-Store Maurer Instruction Set Architectures

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1 Introduction

Maurer proposes a model for computers from the viewpoint of general function and set theory in [7, 8]. Mathematical machines (Turing machines, push-down automata, etc.) are widely known for their inadequate representation of modern computers, but Maurer’s model gives a leading solution. Maurer machines [1], introduced by Bergstra and Middelburg, are based on this model and basic thread algebra with the operator for applying threads to Maurer machines. Basic thread algebra (BTA), which was introduced as Basic Polarized Process Algebra (BPPA) in [5], is a theory that describes the behaviour of deterministic sequential programs under execution. The behaviours concerned are supposed to be threads in BTA (see more in [3]).

In load-store (or register-register) architectures (see, e.g., [6]), we have explicit instructions that access memory only. Load instructions read data from the memory and copy them to registers. Store instructions write data from registers to the memory. Computers of today use load-store architectures, because (1) register access is faster than memory access; (2) registers allow for compiler optimisations, e.g., an expression may be evaluated in any order of execution; (3) registers can be used to hold all the variables relevant for a specific code segment, so the operations are faster.

In [2], Bergstra and Middelburg introduced the concept of a strict load-store Maurer instruction set architecture (strict load-store Maurer ISA, for short) and studied under what conditions and how these conditions can affect the transformations on the states of the memory of a strict load-store Maurer ISA to be achieved.

There are mainly three parts in a load-store instruction set architecture: a memory that contains data, registers, and an operating unit that processes data. In this paper, we study how certain conditions can affect the transformations, when half of the data memory serves as the part of the operating unit.

The rest of the paper is organised as follows. First of all, we review basic thread algebra and Maurer machines in Section 2 and Section 3 respectively.
Next, in Section 4, we describe the notion of the apply operator. Following this, we explain the strict load-store instruction set architectures in Section 5. After that, in Section 6, we review the concept of thread powered function classes and show two results of the completeness. Then we recall an incompleteness in Section 7. Finally, we give some concluding remarks in Section 8.

2 Basic Thread Algebra

Consider a fixed but arbitrary finite set $A$ of basic actions with $\text{tau} \notin A$. We denote $A \cup \{\text{tau}\}$ by $\mathcal{A}_{\text{tau}}$. The signature of BTA consists of the following constants and operators:

1. the deadlock constant $D$;
2. the termination constant $S$;
3. for each $a \in \mathcal{A}_{\text{tau}}$, a binary postconditional composition operator $\triangleright a \triangleright$.

With $D$ an inactive behavior is indicated and with $S$ a successful terminating behavior is denoted. A single action is not a thread, and finite threads always end in $S$ or $D$. The thread $x \triangleright a \triangleright y$ will first perform $a$ and then proceed as $x$ if the processing of $a$ produces the positive reply $T$, and it will proceed as $y$ if the processing of $a$ produces the negative reply $F$. We abbreviate $P \triangleright a \triangleright P$ using the action prefixing operator: $a \circ P$ and take $\circ$ to bind strongest. The action $\text{tau}$ will always produce a positive reply. The axiom for this action is given in Table 1. Using the action prefixing operator, axiom T1 can be also written for short as: $x \triangleright \text{tau} \triangleright y = \text{tau} \circ x$.

| $x \triangleright \text{tau} \triangleright y$ | $x \triangleright \text{tau} \triangleright x$ |
|-----------------------------------------|--------------------------|
| T1                                      |                           |

Table 1: Axioms for BTA

Every thread in BTA is finite in the sense that the number of consecutive actions it can perform is bounded. Infinite threads can be defined using guarded recursive specifications.

A guarded recursive specification over BTA is a set of recursion equations \{ $X_i = t_i(X)$ | $X_i \in V_E$ \}, where $V_E = \{X_1, X_2, \ldots, X_n\}$ is a set of all variables that occur on the left-hand side of an equation in $E$, $X$ is a vector containing all variables in $V_E$, i.e. $X = X_1, \ldots, X_n$, and $t_i$ is a term of the form $D, S$ or $t \triangleright a \triangleright t'$ (and $t'$ are terms of BTA that contain only variables from $X$).

A solution for a recursive equation is a thread that solves the equation. We use the constant $\langle X_i | E \rangle$ to denote the solution for the recursive equation $\langle X_i = t_i(X) \rangle \in E$. A solution for a guarded recursive specification $E$, with $V_E = \{X_1, \ldots, X_n\}$, is a vector $\langle X_1 | E \rangle, \ldots, \langle X_n | E \rangle$ such that substituting each variable in $V_E$ by its respective solution turns all equations in $E$ into true statements. Once $E$ is declared, $\langle X_i | E \rangle$ can be abbreviated by $\langle X_i \rangle$. We give the axioms for guarded recursion in Table 2. The recursive definition principle (RDP)
states that \( (X_1|E), \ldots, (X_n|E) \) is a solution for \( E \). The recursive specification principle (RSP) states that this solution is the only one.

We write BTA + REC for BTA extended with the constants for solutions of guarded recursive specifications and axioms RDP and RSP.

From now on, we write \( E_{\text{fin}}(A) \), where \( A \subseteq \mathcal{A} \), for the set of all finite guarded recursive specifications over BTA that contain only postconditional operators \( - \preceq a \succeq - \) for which \( a \) ranges over \( A \), and \( T_{\text{finrec}}(A) \), where \( A \subseteq \mathcal{A} \), for the set of all closed terms of BTA + REC that contain only postconditional operators \( - \preceq a \succeq - \) for which \( a \) ranges over \( A \) and only constants \( (X_i|E) \) for which \( E \) ranges over \( E_{\text{fin}}(A) \).

We give the following definition of the set of thread states, which will be used later in Section 4.

**Definition 1.** Let \( \mathcal{A} \) be some model of BTA + REC, and let \( p \) be an element from the domain of \( \mathcal{A} \). Then the set of states of \( p \), written \( \text{Res}(p) \), is inductively defined as follows:

1. \( p \in \text{Res}(p) \);
2. if \( q \preceq a \succeq r \in \text{Res}(p) \), then \( q, r \in \text{Res}(p) \).

In subsequent sections, the following threads, which have more than one initial states, are not used.

\[
\begin{align*}
S & \quad a \circ S \quad b \circ S \\
& \quad S \quad S
\end{align*}
\]

**Figure 1: Connected Thread**

3 **Maurer Machines**

In this section we review Maurer machines, which were first introduced in [1].

Most modern computers use the binary system, i.e., information is exchanged and processed internally using 2 as numerical base. Theoretically we can also use any number as the base, such as 3, 5, 8, etc. Therefore, a computer can be constructed to the base \( n \), which means that information is virtually operated using only the digits from 0 through \( n - 1 \). We assume that the base \( n \) is constant over the whole computer.
Every computer has a memory. We represent the memory of a computer as a set \( M \). Registers are regarded as subsets of \( M \). We consider a set \( B \) as the base set, whose cardinality is the base of the computer. If the base of a computer is \( n \), the base set of this computer is the set of all integers from 0 to \( n-1 \). A state of the computer is represented as an arbitrary map from \( M \) to \( B \). We can change one state to another by performing operations.

Maurer machines are based on this simple model of computers. The memory of a Maurer machine consists of memory elements. Every memory element contains a value from the base set of the Maurer machine as a content. The contents of all memory elements build up a state of the Maurer machine. The Maurer machine processes a basic action by performing the operation associated with the basic action. The execution of an operation carries out the passing from one state to the next. As a result of state changes, the content of the memory element associated with the basic action is changed to the reply produced by the Maurer machine.

Now we give the following definition of a Maurer machine.

**Definition 2.** Let \( M \) be a non-empty set, let \( B \) be a set with \( \text{card}(B) \geq 2 \) (which means \( B \) contains at least two members \( T \) and \( F \)), let \( S \) be a set of functions \( S: M \rightarrow B \), let \( O \) be a set of functions \( O: S \rightarrow S \), let \( A \subseteq A \) be a set, let \( [\cdot]: A \rightarrow (O \times M) \) be a function, satisfying the following conditions:

- if \( S_1, S_2 \in S, M' \subseteq M \), and \( S_3: M \rightarrow B \) is such that \( S_3(x) = S_1(x) \) if \( x \in M' \) and \( S_3(x) = S_2(x) \) if \( x \notin M' \), then \( S_3 \in S \);
- if \( S_1, S_2 \in S \), then the set \( \{ x \in M \mid S_1(x) \neq S_2(x) \} \) is finite;
- if \( S \in S, a \in A, \) and \( [a] = (O, m), \) then \( S(m) \in \{T, F\} \).

Then the 6-tuple \( H = (M, B, S, O, A, [\cdot]) \) is a Maurer machine. The set \( M \) is the memory of \( H \); the set \( B \) is the base set of \( H \); the members of \( S \) are the states of \( H \); the members of \( O \) are the operations of \( H \); the members of \( A \) are the basic actions of \( H \); and the function \( [\cdot] \) is the basic action interpretation function of \( H \).

Every operation \( O: S \rightarrow S \) is associated with two subsets of \( M \). For example, if we want to move the data in the memory \( Y \) to the register \( R \), we are implying \( Y \) and \( R \) are proper subsets of \( M \). We give the relation between \( O \) and these two subsets by the following notions of input and output regions of an operation, which will be used later in Section 5.

**Definition 3.** Let \( H = (M, B, S, O, A, [\cdot]) \) be a Maurer machine, and let \( O: S \rightarrow S \). Then we define the input region of \( O \), written \( IR(O) \), and the output region of \( O \), written \( OR(O) \), which are the subsets of \( M \), as follows:

\[
IR(O) = \{ x \in M \mid \exists S_1, S_2 \in S. (\forall z \in M \setminus \{x\}. S_1(z) = S_2(z) \land \
\quad \exists y \in OR(O). O(S_1)(y) \neq O(S_2)(y)) \},
\]

\[
OR(O) = \{ x \in M \mid \exists S \in S. S(x) \neq O(S)(x) \}.
\]
According to this definition, in the above example, we call \( Y \) the input region and \( R \) the output region of \( O \). Each operation takes data only from its input region and places data only in its output region.

4 Application of Threads to Maurer Machines

The binary apply operator \( \_ \cdot H \_ \) connects a thread and a state of a Maurer machine, and yields either a state of the Maurer machine or the *undefined state* \( \uparrow \). In other words, \( p \cdot H S \) indicates the resulting state after the Maurer machine

\[
H = (M, B, S, O, A, [\_])
\]

executes all the basic actions performed by the thread \( p \in \mathcal{T}_{\text{inrec}}(A) \) from the initial state \( S \in S \). Let \( (O_a, m_a) = [a] \) for all \( a \in A \). \( H \) executes a basic action \( a \) by performing \( O_a \). This leads to a state change. In the resulting state, the reply produced by \( H \) is the content in \( m_a \). If \( p \) is \( S \), no state changes. If \( p \) is \( D \), the result is \( \uparrow \).

Then we give the following defining equations for the apply operator in Table 3, where \( a \) ranges over \( A \), and \( S \) ranges over \( S \).

| \( x \cdot H \uparrow \) | \( = \uparrow \) |
|----------------|----------------|
| \( S \cdot H S = S \) | \( D \cdot H S = \uparrow \) |
| \( (x \preceq a \succeq y) \cdot H S = x \cdot H O_a(S) \) if \( O_a(S)(m_a) = T \) |
| \( (x \preceq a \succeq y) \cdot H S = y \cdot H O_a(S) \) if \( O_a(S)(m_a) = F \) |

5 Strict Load-Store Maurer ISAs

In this section we review a strict load-store Maurer ISA [2, 4].

The basic idea of a strict load-store Maurer ISA is the following: in the setting of Maurer machines, a segmented memory is used as a main memory to contain data, and a small segmented memory is used as an operating unit to process data, as shown in Figure 2. Only load and store instructions can access the data memory, moving data from the memory to the register, or to the memory from the register, respectively. All other instructions (e.g., instructions for data manipulation) can use only register operands. Operations (such as, calculating a data address, add, subtraction, AND, shifts, etc.), taking operands from registers, are executed in the operating unit. The result is stored back to a register. Without loss of generality, we assume that data is restricted to the natural numbers.

A strict load-store Maurer ISA has the following parameters:

- an address width \( k \);
- a word length \( l \);
Figure 2: Strict Load-Store Maurer ISA

- a bit size \( m \) of the operating unit;
- a number \( u \) of pairs of address and data registers for load instructions;
- a number \( v \) of pairs of address and data registers for store instructions;
- a set \( A' \) of basic instructions for data manipulation.

The symbols can be regarded as follows:

- \( k \): the number of bits used for the binary representation of addresses of data memory elements;
- \( l \): the number of bits used to represent data in data memory elements;
- \( m \): the number of bits that the internal memory of the operating unit contains.

The data memory is a fixed but arbitrary set \( M_{data} \) which has a cardinality of \( 2^k \) as shown in Figure 2. Its elements can contain natural numbers as data in the interval \([0, 2^k - 1]\) (written \( B_{data} \)), and can be addressed by natural numbers in the interval \([0, 2^k - 1]\) (written \( B_{addr} \)). Hence, we give a fixed but arbitrary bijection \( m_{data} : B_{addr} \rightarrow M_{data} \).

The operating unit memory is a fixed but arbitrary set \( M_{ou} \) which has a cardinality of \( m \). Its elements can contain natural numbers in the set \( \{0,1\} \) (written \( \text{Bit} \)), i.e., bits.
Registers are used to move data between the data memory and the operating unit memory. **Load address registers** and **load data registers** are fixed but arbitrary sets \(M_{la}\) and \(M_{ld}\) respectively, which have cardinality of \(u\). **Store address registers** and **store data registers** are fixed but arbitrary sets \(M_{sa}\) and \(M_{sd}\) respectively, which have cardinality of \(v\). The contents of \(M_{la}\) and \(M_{sa}\) are taken as addresses which are the members of \(B_{addr}\), while the contents of \(M_{ld}\) and \(M_{sd}\) are taken as data which are the members of \(B_{data}\). Hence, written \([0, u - 1]\) and \([0, v - 1]\) as \(B_{load}\) and \(B_{store}\) respectively, we give fixed but arbitrary bijections \(m_{ld} : B_{load} \rightarrow M_{ld}\), \(m_{la} : B_{load} \rightarrow M_{la}\), \(m_{sd} : B_{store} \rightarrow M_{sd}\) and \(m_{sa} : B_{store} \rightarrow M_{sa}\).

The memory element \(rr\) stores the reply of processing \(O_{a}\), the operation associated with the basic action \(a\).

We assume that \(M_{data}\), \(M_{ou}\), \(M_{ld}\), \(M_{sd}\), \(M_{la}\), \(M_{sa}\) and \(\{rr\}\) are pairwise disjoint sets. The meaning of these sets in reality are shown in Figure 4. Let \(n \in B_{addr}\), \(n' \in B_{load}\) and \(n'' \in B_{store}\). Then \(m_{data}(n)\) is denoted by \(M_{data}[n]\), \(m_{ld}(n')\) by \(M_{ld}[n']\), \(m_{sa}(n'')\) by \(M_{sa}[n'']\) and \(m_{sd}(n'')\) by \(M_{sd}[n'']\).

We give the following definition of a strict load-store Maurer ISA.

**Definition 4.** A strict load/store Maurer ISA with parameters \(k\), \(l\), \(m\), \(u\), \(v\) and \(A'\) is a Maurer machine \(H = (M, B, S, O, A, \llbracket \_ \rrbracket)\) with

\[
\begin{align*}
M &= M_{data} \cup M_{ou} \cup M_{ld} \cup M_{sd} \cup M_{la} \cup M_{sa} \cup \{rr\}, \\
B &= [0, j] \cup \{T, F\} \text{ for } j = \max(2^k - 1, 2^l - 1), \\
S &= \{S : M \rightarrow B \mid \\
&\forall m \in M_{data} \cup M_{ld} \cup M_{sd} \cdot S(m) \in B_{data} \land \\
&\forall m \in M_{la} \cup M_{sa} \cdot S(m) \in B_{addr} \land \\
&\forall m \in M_{ou} \cdot S(m) \in \text{Bit} \land S(rr) \in \{T, F\}\}, \\
O &= \{O_a \mid a \in A\}, \\
A &= \{\text{load} : n \mid n \in B_{load}\} \cup \{\text{store} : n \mid n \in B_{store}\} \cup A', \\
\llbracket a \rrbracket &= (O_a, rr) \text{ for all } a \in A.
\end{align*}
\]
where for all \( n \in B_{load} \), \( O_{load:n} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \):

\[
O_{load:n}(S) \upharpoonright (M \setminus \{M_{ld}[n], rr\}) = S \upharpoonright (M \setminus \{M_{ld}[n], rr\}),
\]

\[
O_{load:n}(S)(M_{ld}[n]) = S(M_{data}[S(M_{sa}[n])]),
\]

\[
O_{load:n}(S)(rr) = T,
\]

and, for all \( n \in B_{store} \), \( O_{store:n} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \):

\[
O_{store:n}(S) \upharpoonright (M \setminus \{M_{data}[S(M_{sa}[n])], rr\}) = S \upharpoonright (M \setminus \{M_{data}[S(M_{sa}[n])], rr\}),
\]

\[
O_{store:n}(S)(M_{data}[S(M_{sa}[n])]) = S(M_{ld}[n]),
\]

\[
O_{store:n}(S)(rr) = T,
\]

and, for all \( a \in A' \), \( O_a \) is a function from \( S \) to \( S \) such that:

\[
IR(O_a) \subseteq M_{ou} \cup M_{ld},
\]

\[
OR(O_a) \subseteq M_{ou} \cup M_{sd} \cup M_{ld} \cup M_{sa} \cup \{rr\}.
\]

We denote the set of all strict load-store Maurer ISAs with parameters \( k, l, m, u, v \) and \( A' \) by \( MISA_{sls}(k, l, m, u, v, A') \).

6 Thread Powered Function Classes

In this section we review the thread powered function classes, which help to answer the following question: under which conditions can we achieve all the
possible state transformations by applying threads to a strict load/store Maurer ISA with certain address width and word length?

A thread powered function class has the following parameters:

- an address width \( k \);
- a word length \( l \);
- an operating unit size \( m \);
- an instruction set size \( d \);
- a state space bound \( e \);
- a working area flag \( f \).

The symbols can be regarded as follows:

- \( d \): the number of basic instructions excluding load and store instructions;
- \( e \): a bound on the number of states of the threads that can be applied;
- \( f \): indicates whether a part of the data memory is taken as a working area. There are two cases. First, if \( f = T \), we use the first half of the data memory as the external memory and the second half of the data memory as the internal data memory. Second, if \( f = F \), we use the whole data memory as the external memory.

The definition of the thread powered function class is given as follows.

**Definition 5.** Let \( k, m \geq 0 \) and \( l, d, e > 0 \), and let \( f \in \{T, F\} \) such that \( f = F \) if \( k = 0 \). We define

\[
\begin{align*}
M^k_{data} &= \{ m_{data}(i) \mid i \in [0, 2^k - 1] \}, \\
S_{data} &= \{ S \mid S : M^k_{data} \rightarrow B_{data} \}, \\
T_{data} &= \{ T \mid T : S_{data} \rightarrow S_{data} \}.
\end{align*}
\]

Then the thread powered function class with parameters \( k, l, m, d, e, f \), denoted by \( TPF(k, l, m, d, e, f) \), which is a subset of \( T_{data} \), is defined as follows:

\[
T \in TPF(k, l, m, d, e, f) \iff \exists A' \subseteq A,
\exists H \in MISA_{abs}(k, l, m, u, v, A'),
\exists p \in T_{finrec}(A_H),
\text{card}(A') = d \wedge \text{card(Res}(p)) \leq e \wedge 
\forall S \in S_H .
\]

\[
\begin{align*}
&((f = F \Rightarrow T(S \mid M^k_{data}) = (p \bullet_H S) \mid M^k_{data}) \wedge \\
&(f = T \Rightarrow T(S \mid M^k_{data}) \mid M^{k-1}_{data} = (p \bullet_H S) \mid M^{k-1}_{data})).
\end{align*}
\]

9
Threads are stored in the data memory. When the internal data memory is used as a part of the operating unit, threads are stored in the external memory.

We say that $TPFC(k, l, m, d, e, f)$ is complete if $TPFC(k, l, m, d, e, f)$ is equal to $T_{\text{data}}$.

The following theorem points out that we can get the completeness if we use 5 data manipulation instructions and threads with at most $6 + w$ states ($w$ is the number of load and store instructions) and take the operating unit size slightly greater than the data memory size.

The 5 data manipulation instructions (recall that load and store instructions are not counted for the instruction set) are as follows: an initialization instruction, a pre-load instruction, a post-load instruction, a pre-store instruction, and a transformation instruction. First, before a data memory element $m_0$ is moved to any register, the address of $m_0$ is sent to the load address register by the pre-load instruction. And then $m_0$ is loaded to the load data register. Next, the post-load instruction moves the content of the load data register to the operating unit. Similarly, before the data is moved from the register to the data memory, the pre-store instruction sends the intended address in the data memory to the store address register. And then the content of the operating unit is moved to the store data register. Next, the content of the store data register is stored to the data memory. The transformation instruction applies the relevant state transformation to the content of the operating unit.

The number of the states of the threads consists of 5 states associated with the above 5 data manipulation instructions, the $w$ states associated with load and store instructions, and the termination state.

**Theorem 1.** Let $k \geq 0$, $l > 0$ and $f \in \{T, F\}$, and let $dms$ be the data memory size, i.e., $dms = 2^k \cdot l$. Then $TPFC(k, l, dms + k + 1, 5, 6 + w, f)$ is complete.

In [2], a proof of the case that there are only one load and one store instructions is given.

The following corollary points out that we can still get the completeness if we use about half of the data memory size as the operating unit size.

**Corollary 1.** Let $k, l > 0$, and let $ems$ be the external memory size in the case that $ems$ is half of the data memory size, i.e., $ems = 2^{k-1} \cdot l$. Then $TPFC(k, l, ems + k, 5, 6 + w, T)$ is complete.

In the cases of Theorem 1 and Corollary 1, we need at least 5 data manipulation instructions to accomplish the job.

### 7 Incompleteness

In this section we show under which conditions it is impossible to achieve all transformations on the states of the external memory taking into account the use of the internal data memory.

The idea of using the internal data memory can be explained in Figure 5. We move data from $\alpha$ to registers, operate them (e.g., adding two numbers) in
\[ \text{data memory} \quad \text{registers} \quad \text{operating unit} \]

\begin{align*}
\text{ems} \quad \text{\(\alpha\)} \\
\text{ems} \quad \text{\(\beta\)} \\
\text{ems} \quad \text{\(\gamma\)} \\
\text{\(m\)}
\end{align*}

\(\alpha\): the first half of the data memory, used as the external memory  
\(\beta\): the second half of the data memory, used as the internal data memory  
\(\gamma\): the small internal memory of the operating unit

**Figure 5: Using the Internal Data Memory**

\(\gamma\), and then move the result back to registers. If it is not possible to process all the operations in \(\gamma\) due to the lack of space, we use \(\beta\) and \(\gamma\) together to process operations.

In [2], \(\beta\) is not used to process operations in the case of the lack of space. Lemma 1 in [2] states that if the operating unit size is at most \(ems/2\), the instruction set size is at most \(2^{ems/2}\), and the number of threads that can be applied is at most \(2^{ems}\), it is impossible to achieve all transformations on the states of the external memory, where \(ems\) (external memory size) is half of the data memory size.

We reformulate this lemma with the use of the internal data memory as follows. It states that it is still impossible to achieve all transformations on the states of the external memory if the total size of the operating unit and the used internal data memory is at most \(ems/2\).

**Lemma 1.** Let \(k > 1, l, m, d, e > 0\) and \(ems = (2^k \cdot l)/2\), and let \(ims\) be the used internal data memory size. Then \(TPFC(k, l, m, d, e, \Gamma)\) is not complete if \(m + ims \leq ems/2, d \leq 2^{ems/2}\), the number of threads that can be applied to the members of

\[ \bigcup_{A' \subseteq A} \mathcal{MISA}_{sls}(k, l, m, u, v, A') \]

is at most \(2^{ems}\).

**Proof.** We know that, if the total size of the operating unit and the used internal data memory is at most \(ems/2\), then the number of bits the operating unit and the used internal data memory have is at most \(ems/2\). As shown in Figure 5, since every bit \(m_i\) has two choices, 0 or 1, for \(1 \leq i \leq ems/2\), the number of states of the operating unit and the used internal data memory (in other words, the number of sequences that \(ems/2\) digits can make up if every digit has 2
choices) is at most \(2^{\text{ems}/2}\). Hence there are at most

\[
(2^{\text{ems}/2}) (2^{\text{ems}/2})
\]

transformations on the states of the operating unit and the used internal data memory for one data manipulation instruction.

It follows that, if there are at most \(2^{\text{ems}/2}\) data manipulation instructions, then there are at most

\[
((2^{\text{ems}/2}) (2^{\text{ems}/2}))(2^{\text{ems}/2})
\]

transformations on the states of the external memory for one thread.

So, if at most \(2^{\text{ems}}\) threads can be applied, then the number of transformations on the states of the external memory is at most

\[
((2^{\text{ems}/2}) (2^{\text{ems}/2}))(2^{\text{ems}/2}) \cdot 2^{\text{ems}}.
\]

This number is less than the number of all possible transformations on the states of the external memory, which is \((2^{\text{ems}})(2^{\text{ems}})\), i.e.,

\[
((2^{\text{ems}/2}) (2^{\text{ems}/2}))(2^{\text{ems}/2}) \cdot 2^{\text{ems}} < (2^{\text{ems}})(2^{\text{ems}}).
\]

Therefore, we get that \(T\mathcal{PFC}(k, l, m, d, e, T)\) is not complete.

We prove (**) by the following computation: Let \(x = 2^{(\text{ems}/2)}\). Then

\[
(*) \Rightarrow (x^2)^x \cdot x^2 < (x^2)(x^2) \Rightarrow \\
(x^2)^x \cdot x^2 < (x^2)(x^2) \Rightarrow \\
x(x^2) < (x^2)(x^2-1)
\]

Applying logarithm to both sides of (**), we have

\[
x^2 \log_2 x < 2(x^2 - 1) \log_2 x \Rightarrow (x^2 - 2) \log_2 x > 0.
\]

If \(x > \sqrt{2}\), then we have \(x^2 > 2\), i.e., \(x^2 - 2 > 0\). Since \(\log_2 x > 1/2\) if \(x > \sqrt{2}\), \((x^2 - 2) \log_2 x > 0\) holds if \(x > \sqrt{2}\), i.e., \(\text{ems} > 1\).

Now we can give the following theorem showing that if the total size of the operating unit and the used internal data memory is at most \(\text{ems}/2\), the instruction set size is at most \(2^k - w - 1\), the maximal number of states of the threads is at most \(2^{k-2}\), then \(T\mathcal{PFC}(k, l, m, d, e, T)\) is not complete.
Theorem 2. Let \( k > 2, l > 1, m, d > 0, e > 1 \) and \( \text{ems} = (2^k \cdot l)/2 \), and let \( \text{ims} \) be the used internal data memory size and \( w \) the number of load and store instructions. Then \( TPFC(k, l, m, d, e, T) \) is not complete if \( m + \text{ims} \leq \text{ems}/2 \), \( d \leq 2^l - w - 1 \), \( e \leq 2^{k-2} \).

Proof. We have \( d \) data manipulation instructions, plus \( w \) load and store instructions, then there are \( d + w \) instructions. Suppose every state of threads can perform either according to the positive reply produced by the associated instruction, or according to the negative reply. Since \( e \) is the maximal number of states of the threads that can be applied, no matter which path it performs, the number of states of each path is at most \( e \). Hence, we have \( d + w \) choices for instructions, \( e \) choices for the path caused by the positive reply, and \( e \) choices for the path caused by the negative reply. Including the termination and deadlock, we have \((d + w) \cdot e^2 + 2\) choices to form a thread. Therefore, the number of threads with \( e \) states is

\[
((d + w) \cdot e^2 + 2)^e.
\]

Since \( k > 2, l \geq 2, e > 1 \), we have

\[
((d + w) \cdot e^2 + 2)^e < \left((d + w) \cdot e^2 + e^2\right)^e \leq 2^\text{ems} \text{ if } l \geq 2k - 4.
\]

Hence, the number of threads with \( e \) states is less than \( 2^\text{ems} \).

It is easy to see that \( 2^l < 2^{l(2^k-2)} = 2^\text{ems}/2 \). Then we can get \( 2^l - w - 1 < 2^\text{ems}/2 \), i.e., \( d < 2^\text{ems}/2 \). Because \( m + \text{ims} \leq \text{ems}/2 \), applying Lemma \ref{lemma1}, we can conclude \( TPFC(k, l, m, d, e, T) \) is not complete if \( m + \text{ims} \leq \text{ems}/2 \), \( d \leq 2^l - w - 1 \), \( e \leq 2^{k-2} \).

8 Conclusion

We have reviewed the concepts of BTA and strict load-store Maurer ISA. We also have shown under which conditions we can achieve all the possible transformations on the states of the external memory of a strict load-store Maurer ISA and under which conditions we cannot.

From Theorem \ref{theorem1} and Corollary \ref{corollary1} we can get completeness with 5 data manipulation instructions and at most \( 6 + w \) states of the threads if we take the operating unit size slightly greater than the data memory size, or half of the data memory size. The completeness is lost by decreasing the number of data manipulation instructions and the number of states of the threads. Theorem \ref{theorem2} stated that it is impossible to achieve all transformations if the total size of the operating unit and the used internal data memory is at most half of the external memory size, the instruction set size is at most \( 2^l - w - 1 \), and the maximal number of states of the threads is at most \( 2^{k-2} \).

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