Power reduction using high speed with saving mode clock gating technique

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Abstract. The demand for low power consumption is motivated by several factors such as the evolution of portable design, reliability effects, and flexibility. The purpose of clock gating is inactive or suppresses change to fragments of the clock route as flip-flop, clock system and rationality under a specific condition processed by clock gating chips. Moreover, the clock is disabled when it is not necessary in clock gating to decrease power dissipation. Clock technique successfully turns off the clock any place it pointless expends power. By following the expressed methodology, the force utilization turns out to be less up to half without influencing the performance of the structure. The extraordinary source of power utilization is the clock. Clock signal is not used to achieve any digital calculation. It is for the most part utilized for synchronization of successive circuits. In this way, clock signal does not carry any data. In this research paper, a new sub module for high speed and saving mode is proposed. It saves more power by switch on only the target module and switch other module off. By using this technique, it may reduce power dissipation up to half. In order to execute encoder and decoder structure, the models of compression and decompression process is created by applying Verilog HDL language Quartus II 11.1 Web Edition with 32-Bit. In addition, operational simulation is executed by using ModelSim-Altera 10.0c (Quartus II 11.1 Starter Edition).

Keywords. Clock gating, Huffman, synchronous circuit, VLSI.

1. Introduction
The evolution of portable tools such as smartphones and laptops are the necessary portion driving the demand for combining these two goals data compression and low power consumption in the design. The need for the portable device is growing each year and is forecasted to grow more in the future. Right from beginning, human beings have always in the need of communication means. Moreover, technology has led to evolution of the best systems that have made life generally easier. In recent decades, there has been explosion of evolution of devices and services which has led to faster and more reliable growth and development of digital designs. These are possible because portable electronic devices have become more robust with increase in computing capability and improvements in communication speed and reliability. However, all the increases in speed and reliability have challenges. Two of the most important challenges are data compression and power consumption. Reduced data size leads to decreases in the amount of area needed for data storage. The reduction is
achieved by removing redundant data. Processing small data size definitely consumes less power than large extent because the power needed for transmitting and storing the new size is less than the original file size. Furthermore, as of late bigger and more productive batteries are being utilized to solve unnecessary power utilization issue. So, recently economic and natural issues have constrained the specialists to think on progress and finding solutions for lessening power utilization and expanding dependability in logical designs. Clock gating as the name proposed, is employed to inactive clock signal that supports sequential blocks in digital design during theirs registers are not being used. This method enables reduction of switching activity answerable for the major a portion of the general power dissipation which is due to the charge/discharge of the load capacitance named dynamic power. Moreover, clock gating is one of the highly important methods designed for decreasing power dissipation in digital circuits. The prime idea is to stop clock in the parts of the design that are idle at a given period to decrease switching activity in the registers and transfer the data from those registers for considerable power saving. Frequency scaling is used to divide the master clock into sub-modules in the design and make each of them work on fast and slow mode. The implementation of frequency scaling involves start of added logic unit to gate the clock and this style is utilized to reduce switching activity. Furthermore, there will be creation of good chance to meet and deal with business environments, advanced technologies and state of the art EDA tools with integration of a system team from one of the world’s brains in EDA tools. Unnecessary power consumption in IC complicates them utilize in portable structures. This also causes high temperatures which lowers the quality of device and decrease chip lifetime [1]. The demands of consumers for more functionality with high performance lead to generation of high temperatures, because high performance need to high frequency, while not all the data need the same frequency for execution, part of data need low frequency implementation. Therefore, putting the design to working in one frequency leads to high temperature and decrease a chip lifetime. In this way, power utilization of logic system has become more significant that the designers invest noteworthy measure of their time improving their structures for insignificant power utilization. Sequential design consumes large amount of power because the clock signal switches at all times [2].

Moreover, reduction of power consumption does not only lengthen the battery life time in portable device, smart phones or the entire modern devices but it also increases the reliability by decreasing the overhead which is very important in keeping the design stable without overheating [3]. The target is to keep the temperature low to avoid design restrictions [4]. The methodology of achieving this aim is to have the performance when it is required barely. The researchers are looking for the best technologies to reduce power without degrading to the performance [5]. To control temperature levels, the chip needs particular and exorbitant pressing and cooling courses of action which would bring about the future acceleration of the system cost [6]. The developing requirement for movable communication design and calculating system has expanded the requirement for enhancement of power utilization in the chip. Generally, low-power configuration is a basic innovation required in the semiconductor industry today [7].

1.1. Huffman Design

In Figure 1 the block illustration of the conventional 8B/9B Huffman design is shown. Figure 1 consist of the main input signals to get two main output signals only, first on represent 9-bit encoder output. While, the second on represent 8-bit output decoder. In addition, the two-output signal named length are optional used to represent the length of input and output cod design. Sub-module design has three input signals. The first one CLK- signal used to switch on and off the total Huffman design, the second one named e-d signal as abbreviation to encoder and decoder used to switch on and off. The third one named h-s signal used to make each module that switch on to work in high performance and saving mode according to the required design.
Figure 1: RTL Viewer of top-level Huffman design.

Table 1. Flow summary for Huffman design.

| Parameters                      | Sub-Module | Encoder | Decoder | Top-Level |
|---------------------------------|------------|---------|---------|-----------|
| Top-level Entity Name           | Sub Module | Enc1    | Dec     | Huffman   |
| Total logic elements            | 2 / 14,400 | 2 / 14,400 | 6 / 14,400 | 10 / 21,280 |
| Total combinational functions   | 2 / 14,400 | 2 / 14,400 | 4 / 14,400 | 8 / 21,280  |
| Total registers                 | 0          | 1       | 4       | 5         |
| Total pins                      | 4 / 81     | 27 / 81 | 18 / 81 | 36 / 81   |
| Total virtual pins              | 0          | 0       | 0       | 0         |
| Total memory bits               | 0 / 552,960 | 2,560 / 552,960 | 0 / 552,960 | 1,536 / 552,960 |

Clear to see from Table 1, that the total number of registers in top-level Huffman design is equal to the total register in all module design, in addition to that, there is no any register used in sub module design. Therefore, no power dissipated in this module because no register used any clock signal in this module.

1.2. HDL Huffman Coding

Hardware Description Language (HDLs) and their test systems permit designers to segment their system into segments that can work effectively and communicate with each other [8]. Huffman configuration comprises of two principle modules which are encoder and decoder, additionally the code of high-level Huffman [9]. That suggests that full structures include three codes, two for modules and one for high-level design. Besides, each code configuration ought to have a matching code for test bench. All code configurations and test bench are penned in Verilog HDL language [10]. Figure 2, shown the block diagram of encoder and code for each character which comes from the tree. Figure 3, show the RTL Viewer of decoder design.
2. Sub Module Design (SMD)

Sub Module Design (SMD) produces a clock signal which involves two techniques of low power consumption, clock gating and frequency scaling to be used in standard Huffman design. To do this, Master Clock Divider (MCD) is constructed to make the Huffman’s module work in high and low frequency. Secondly, clock gating technique to switch on only target module and another module to switch it off are designed [11]. Then, these techniques are combined in a new sub module named Sub Module Design (SMD).

2.1. Master Clock Divider (MCD)

This design is used to reduce the value of master clock signal frequency. The procedures are by using 3-bit binary counter output or cascading them together to type a divide-by-3 binary counter where the number of counter phases used. This is known as the modulus of a counter. It is the quantity of yield expresses the counter experiences before returning itself to zero to have one complete cycle. 3-bit binary counter = $2^3 = 8$ (modul-8 or MOD-8) as shown in Figure 4, and the output waveform in Figure 5.

![Figure 3: RTL Viewer of decoder design.](image)

![Figure 4: 3-Bit master clock divider.](image)
2.2. Full Sub Module Design (SMD)
Sub Module Design (SMD) combines two techniques of low power design to generate a signal that can cause the yield configuration to defeat the impediments of power utilization and information size. First of all, a clock signal that has capability of accomplishing the role of clock result is made. While applying the clock signal toward the high-level segment, the objective module is turned on and the subsequent module is turned off. Through this, power utilization can be essentially decreased. Then, master clock divider (MCD) is embedded to make each sub module slow and fast. The systems for assessing power utilization for every method of Huffman configuration is by isolating each sub-module and present it as a high-level design for power utilization estimation [12].

Total Power Consumption = static power + dynamic power  \hspace{1cm} (1)

Total sub-modules in Huffman design with SMD module consists of three sub modules:

Total Huffman Power = Encoder power + Decoder power + SMD power  \hspace{1cm} (2)

2.3. Power Analysis for Huffman without (SMD)
The main drawback for Huffman compression the overhead created from coding and decoding process [13]. Therefore, using low power techniques leads to overcome this problem by making system fast and slow mode. Power consumption incorporates two categories of it: static power besides dynamic power. Static power is little, and the principle impact of the all-out power utilization is created from dynamic power [14]. For second category, it comprises of inner power and switching action. The principle impact of the low power procedures utilized in this research is to lessen the switching, as a result of the static power is extremely little and the fundamental part for comprising all out power is the dynamic power which incorporate switching action. So as to actualize the encoder and decoder designs, the architectures of compression and decompression process is formed by employing Verilog HDL language Quartus II 11.1 Web Edition with 32-Bit. In addition, functional simulation is done by using ModelSim-Altera 10.0c (Quartus II 11.1 Starter Edition).

Sub Module Design (SMD) has two stages in its method of activity for every module that is constrained by the two-input signal as appeared in Table 2. The first mode is when the design works in high performance as it appears in the waveform. The plus signal is very high in both encoder and decoder. However, if the high saving signal is set to low, the MCD will be on and the SMD clock output will result from a reduction in switching activity. Therefore, more power is saved. After SMD validation step, the Sub Module Design is embedded in Huffman design to simulate full system as shown in the waveform simulation. Figure 6, show the Sub Module Design validation. Figure 7, show Huffman waveform validations.
Table 2. Huffman output operation mode.

| Clock gating(e_d) | Frequency scaling(h_s) | Huffman output phase        |
|------------------|------------------------|-----------------------------|
| 0                | 0                      | Decoder Huffman _Slow_ Mode |
| 0                | 1                      | Decoder Huffman _High_ Performance |
| 1                | 0                      | Encoder Huffman _Slow_ Mode |
| 1                | 1                      | Encoder Huffman _High_ Performance |

Figure 6. Sub Module Design validation.

Figure 7. Huffman waveform validations.
3. Power Analysis in Huffman using SMD

As per Table 2, the yield of the design generates four different equations to estimate the total power utilization for every method of Huffman activity: Total Huffman Power = Total Power Encoder (mode) + Total Power Decoder (mode) + Total Power SMD.

\[ \text{THP} = \text{TPE}_\text{mode} + \text{TPD}_\text{mode} + \text{TP}_\text{SMD} \] (3)

3.1. Huffman Encoder Safe Mode

To derive equation for power calculation, depend on the equation (3), using script of Synopsys tool to assign encoder module as top-level design and switch off decoder module by embedding special block to estimate the exact static power. This procedure enables the designer to compute the specific power utilization in every mode without losing any power.

Total Huffman Power = Total Power Encoder Slow Mode (top-level) + Total Leakage Power Decoder (off) + Total Power SMD.

\[ \text{THP} = \text{TPE}_\text{SM} + \text{TLPD}_\text{off} + \text{TP}_\text{SMD} \] (4)

3.2. Huffman Encoder High Performance

For deriving equation to calculate power consumption, set encoder module as top-level design and put the decoder in switch off mode by embedding special block in code design to estimate exact static power by using available choices of Synopsys tool. This method leads to calculate exact power consumption in each mode without power loss. The special block is abstracted by set the clock signal to zero in way to make this sub module off. Moreover, internal power and switching activity in this case equal to zero and just calculated the leakage power, therefore leakage power represents the total power consumption in this module.

Total Huffman Power = Total Power Encoder High Performance (top-level) + Total Leakage Power Decoder (off) + Total Power SMD.

\[ \text{THP} = \text{TPE}_\text{HP} + \text{TLPD}_\text{off} + \text{TP}_\text{SMD} \] (5)

3.3. Huffman Decoder Safe Mode

To derive the equation for power in this case, assign decoder module as top-level design and make encoder module in switch off mode by embedding special block in code design to estimate the exact static power by the same procedure mentioned above.

Total Huffman Power = Total Power Decoder Slow Mode (top-level) + Total Leakage Power Encoder (off) + Total Power SMD.

\[ \text{THP} = \text{TPD}_\text{SM} + \text{TLPE}_\text{off} + \text{TP}_\text{SMD} \] (6)

3.4. Huffman Decoder High Performance

To derive the equation for power estimation here, assign decoder module as a top-level design, and put encoder module in switch off mode by embed special block in code design to estimate the exact leakage power. Following these procedures leads to compute the specific power consumption in every mode without any power loss. The time is portioned by proposed progress according to Synopsys synthesizer within the time constraints.

Total Huffman Power = Total Power Decoder High Performance (top-level) + Total Leakage Power Encoder (off) + Total Power SMD.

\[ \text{THP} = \text{TPD}_\text{HP} + \text{TLPE}_\text{off} + \text{TP}_\text{SMD} \] (7)

4. Conclusion

In order to make full use of smaller size and save a large part of the consumed power, a Huffman coding for data compression has been proposed using binary tree. Additionally, embedding (SMD) is successful to analyze power in four different cases. Suggested SMD has been executed depend on the
clock gating and frequency scaling to decrease the dynamic power dissipated in Huffman design. Clock technique procedure can be used to spare more power by switching off part of design when its use is redundant. Frequency scaling can be implemented to control the design in fast and slow mode. The strategy for power computation by considering each sub-module separate guided to compute the specific power dissipation in each sub-module and achieve the completed structure. This method characterized by breaking the full system down into subsystems based on their data rates and the drive them with fast and slow clocks. High rate in power utilization is accomplished in Huffman encoder and decoder saving forms. After all, information compression other than low power approaches can develop and create the system totally at a high level. This research provides a strong establishment to the great career as an ASIC planner. Moreover, this work showed that the design of Huffman is a stronger than other compression and decompression mechanisms that target to reducing data size without losing any details. The simplicity of its design and high efficiency in terms of performance and power should be recognized.

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