Abstract—In this paper, TCAD was used to simulate GGNMOS (Grounded-Gate NMOS) as an ESD protection device for 40V BCD. The physic models and the calibration method are discussed in order to get better accuracy on the result. The effects of device parameter on the ESD robustness are investigated by device simulation in order to achieve the desired ESD design window. The simulated holding voltage is in agreement with BJT model that already proven has an agreement with silicon result. Finally, the ESD design window for 40V BCD device can be obtained by changing some device parameters.

Keywords : ESD, GGNMOS, TLP, BCD, Reliability

I. INTRODUCTION

Electrostatic Discharge (ESD) is one of the most important reliability issues in IC industry. Human handling or contact with machines can cause ESD. Normally, several kilo-volts electrostatic charges are accumulated by triboelectric charging in human body. Any contact by a charged human body with a grounded object can result in a discharge for about 100ns and usually give a mild shock to human beings. However, if the same amount of charge is discharged through a semiconductor device, it can result in device’s failure. [1]-[2]

Protection circuits for ESD become the main concern for IC industry. Protection circuit within the IC chip must fulfill the requirement of an ESD design window as shown in Fig. 1. Holding voltage should be higher than operating voltage in order to avoid latch-up problem. Trigger voltage should not exceed gate oxide breakdown voltage to ensure the device’s reliability.

Over the years, IC Industry always use wafer experiment to design a robust ESD protection circuit. Not only highly cost but also a lot of time and resources are required. Nowadays, it has been proven that TCAD can simulate and predict the silicon result accurately. Therefore, TCAD experiment is expected to be one of possibilities which can be used to replace wafer experiment. A device simulation which is well describing the ESD phenomena and giving better accuracy should be established.

II. DEVICE SIMULATION

Device simulation has been performed to investigate the ESD phenomena. ESD physics needs to be considered in order to achieve better accuracy. Device simulation should adopt thermodynamic and hydrodynamic methods to represent electro thermal situation in ESD. In order to describe ESD I-V characteristics, some models are used and calibrated.

A. Mesh Strategy

Mesh design is very important for device simulation in order to get better accuracy on the result. Well designed mesh will help divergence issue and also give a reasonable result. Incorrect mesh design will create an inaccurate doping profile, hence it will lead to inaccurate measurement on parasitic BJT performance. These will cause inaccurate device simulation result.

B. Physics Model

ESD stress will cause current density and temperature in the device higher than under typical operating condition. Mobility, Avalanche, and Recombination models should accommodate this kind of situation. Temperature dependent models should be adopted because we are dealing with high temperature during ESD stress. We need to activate some...
temperature dependent models such as ARORA, VALDINOCI, Shockley-Read-Hall (SRH) and Auger.

C. Model Calibration

In order to achieve better accuracy, we need to calibrate some model parameters based on our device characteristic. Some models including ARORA and VALDINOCI have already been proven for their accuracies [3]-[4]. On the other hand, minority and majority carrier lifetimes need to be considered and well adjusted in recombination model. These carrier lifetimes can be adjusted by calibrating parasitic BJT gain measurement and simulation [5].

D. Thermal Resistance

The crucial part for precise thermal simulations is determining the thermal resistance. One of the approaches is to simulate the thermal environment as similar as possible and estimate a reasonable external thermal resistance. To estimate thermal resistance, we need to consider about 3D geometry of the device since the real heat flow path in the physical device is in 3D. Thermal resistance evaluation in 3D could be estimated by using an approach as published by Hirsch [6].

III. GGNMOS AS ESD PROTECTION DEVICE

We use GGNMOS as ESD protection device which is fabricated using 0.35µm BCD technology and has cross section as shown in Fig. 2.

ESD characteristic of GGNMOS depends on its parasitic NPN bipolar performance as shown in Fig. 3. ESD current will discharge through the low impedance channel which is formed once the parasitic NPN bipolar turns on. Parasitic NPN bipolar current gain performance becomes the major influence on ESD performance of GGNMOS.

The influences of device parameters are investigated to increase ESD robustness of this device in order to achieve the desired ESD design window. Device parameters changing will affect the value of each component in GGNMOS equivalent circuit and this will also influence the ESD performance of GGNMOS.

A. Channel Length Effect

Effective channel length is the base length for parasitic NPN bipolar in GGNMOS and this parameter has strong influence on ESD performance of GGNMOS. Effective channel length also influences a little bit in the parasitic NPN bipolar current gain. With proper n value, holding voltage \( V_h \) dependence on effective channel length \( L_{ch} \) is in agreement with lateral NPN bipolar snapback model as in (1) [7].

\[
V_h = \frac{V_{bd}}{L_{ch}^{2/n}} \frac{1}{k 2^n} \left( \frac{L_{ch}}{L_n} \right)^{2/n}
\]

where \( V_{bd} \) is the breakdown voltage, \( L_n \) is the electron diffusion length in p-type substrate, \( k \) and \( n \) is an empirical constant. Using \( L_n \) of 20µm, our experiment can be fitted with a reasonable value of \( n=7 \) as shown in Fig. 4. The point that we need to consider is longer effective channel length will increase drain to source resistance. These will lead to higher trigger voltage and slower switching speed.

B. Beta Effect

P-Body concentration ( \( N_{aB} \) ) will affect the value of parasitic NPN bipolar current gain \( \beta_F \) as in (2) [8]. As emitter width \( W_E \), base width \( W_B \), electron diffusivities \( D_n \), hole diffusivities \( D_p \) and N+ concentration \( N_{dE} \) is a constant value hence increasing \( N_{aB} \) will affect on lowering \( \beta_F \) as shown in Fig. 5.

\[
\beta_F = \frac{I_C}{I_B} = \frac{N_{dE} D_n W_E}{N_{aB} D_p W_B}
\]
As mentioned in previous section, ESD characteristic of GGNMOS depends on its parasitic NPN bipolar performance. Parasitic NPN bipolar current gain is the most important parameter in NPN bipolar performance. This parasitic NPN bipolar current gain becomes the major parameter for ESD performance of GGNMOS. Investigation of holding voltage dependence on parasitic NPN bipolar current gain is performed and the result is in agreement with NPN bipolar model as in (3) [7].

\[ V_h = \frac{V_{bd}}{\sqrt{1 + k \beta}} \]  

(3)

where \( \beta \) is measured parasitic NPN bipolar current gain. Our experiment can be fitted with a reasonable value of \( n = 3.8 \) as shown in Fig. 6.

C. NBL Effect

Partial N+ Buried Layer (NBL) below HVNW will add another parasitic NPN bipolar path to the device as shown in Fig. 7. The common lateral NPN path is shown in yellow color and the added vertical NPN path is shown in green color. These two parasitic NPN bipolar paths (lateral and vertical) will cause second snapback as shown in Fig. 8. NBL also reduces the resistance between drain-source and leads to lower trigger voltage.

IV. PROPOSED STRUCTURE

We proposed a structure in order to fulfill the requirement of 40V BCD. We need to get holding voltage above 40V from the current holding voltage to avoid latch up problem. In order to increase the holding voltage and reduce the trigger voltage, we add partial NBL below the NDD to create another ESD path or vertical parasitic NPN bipolar path.

In addition to partial NBL, we also lengthen the effective channel length to increase the holding voltage. We can also reduce the \( \beta \) by increasing P-Body concentration in order to achieve high holding voltage. We prefer not to change the P-Body concentration for this case because it will affect all the BCD process and also the BCD performance. The proposed structure is simulated using TSUPREM4 and the result is shown in Fig. 9. The partial NBL layer is implanted deep beneath the NDD.

TLP simulation is performed for this proposed device and the result is compared to the previous GGNMOS device as shown in Fig. 10. The proposed structured can achieve holding voltage above operating voltage 40V and also has lower trigger voltage than the previous structure. The second snapback appears because of the two parasitic NPN bipolar paths in this device.
In this paper, TCAD simulation is used for reliability test instead of using wafer experiment by recreating the same test condition as the real test. Choosing the proper model and calibration are needed to increase the accuracy of the device simulation. TCAD simulation can provide the insight of your device behavior on device parameter dependence. Parasitic NPN bipolar current gain and effective channel length is proven to be the major influence towards the holding voltage. Partial NBL and effective channel length are chosen in order to enhance the ESD performance of GGNMOS. Finally, this proposed structure is able to achieve the desired ESD window for 40V BCD device. This proposed device has holding voltage more than operating voltage 40V and lower trigger voltage than previous structure.

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REFERENCES

[1] A. Amerasekera and C. Duvvury, ESD in Silicon Integrated Circuits, 2nd ed., J. Wiley, New York, 2002
[2] O. Semenov, H. Sarbishaei, and M. Sachdev, ESD Protection Device and Circuit Design for Advanced CMOS Technologies, Springer, 2008
[3] N. D. Arora, J. R. Hauser, and D. J. Roulston, “Electron and hole mobilities in silicon as a function of concentration and temperature,” IEEE Trans. Electron Devices, Vol. ED-29, pp. 292-295, Feb. 1982.
[4] M. Valdinoci, D. Ventura, M.C. Vecchi, M. Rudan, G. Baccarani, F. Illien, A. Stricker and L. Zullino, “Impact-ionization in silicon at large operating temperature,” International Conference on Simulation of Semiconductor Processes and Devices, Sept. 6-8, 1999.
[5] M. Schenkel, S. Mettler, W. Reiner et al., “Measurements and 3D simulations of full-chip potential distribution at parasitic substrate current injection,” Proceeding of European Solid-state Device Research Conference, Cork, Ireland, May, 2000,pp.600-603.
[6] I. Hirsch, E. Berman, and N. Haik, “Thermal resistance evaluation in 3D thermal simulation of MOSFET transistors,” Solid-State Electronics, vol. 36, no. 1, pp. 106–108, 1993.
[7] Y. Fong, C. Hu, “High-current snapback characteristic of MOSFET’s”, IEEE Trans. Electron Devices, Vol. 37 No.9, pp. 2101-2103, Sept. 1990.
[8] Howe, R. T., and C. G. Sodini Microelectronics, An Integrated Approach. Upper Saddle River, NJ: Prentice Hall, 1997