A Stress-Relieved Method Based on Bottom Pattern Design Considering Thermal and Mechanical Behavior of DBC Substrate

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ABSTRACT Currently, stress analysis on direct bonded copper (DBC) is mainly based on a model with symmetrical top and bottom copper layers. These analyses provide thermal-mechanical stress-relieving methods at the outer edge of the copper-ceramic interface in DBC. However, these methods are unsuitable to release the concentrated stress at the inner gap edges where the top copper layer is etched into the circuit pattern. The stress-concentrated phenomenon causes initial delamination at the inner gap edge of the top copper-ceramic interface in DBC usage. Hence, this paper analyzed the mechanism of the phenomenon and proposed a bottom pattern design method to solve this problem. Through stress analysis on a simplified DBC model with etched top copper, the phenomenon can be explained by the large composite stress produced by the opposite bending actions of the top and bottom copper-ceramic interface in DBC. To reduce the effect of bending action on the bottom interface, parallel dimple traces are used on the bottom instead of a mirror-copied gap on consideration of thermal resistance and mechanical strength. The parameters of dimple trace were chosen by simulations on stress-strain results under thermal cycling and thermal resistance calculations in a module packaging. FE results show that the bottom dimple trace with a diameter of 0.4mm and a gap of 2mm can adjust the thermal-induced strain behavior of the singularities at the top copper to be even and sacrifices only a 2% thermal resistance rise of the module packaging. A life prediction model based on strain shows that the bottom design can improve the lifetime of the substrate. The thermal cycling test result on sample DBC and thermal resistance measurement on the module packaged by DBC with bottom pattern design verify the FE analysis. This method can be widely used in the packaging design of power modules using stand-alone DBC substrate.

INDEX TERMS Direct bonded copper, power module, stress reduction, thermal resistance, reliability.

I. INTRODUCTION

Power electronics module based on direct bonded copper (DBC) has been widely used in industrial applications [1]. Commercial module packages for silicon devices under 150°C operation temperature such as EasyPACK 2B [2], and Hybrid Pack DSC [3] remove the metal baseplate in the conventional package and use DBC as a stand-alone substrate for its high thermal conductivity and good dielectric strength [4]. State of art power devices based on wide bandgap semiconductor has a demand for operation temperature higher than 200°C. Under such demand, the DBC substrate will be exposed to higher processing temperatures during die attachment and larger thermal swings in usage. Such high temperature and such high thermal swing induce high thermal-mechanical stress and strain in the metal-ceramic interface of the DBC substrate due to the thermal expansion coefficient (CTE) mismatch of the substrate materials, which affects the fatigue life of the DBC substrate and performance of the power electronics based on the substrate [5], [6], [7]. One way to relieve the stress and strain under high temperatures is to replace substrate materials
with low-modulus materials such as direct bonded aluminum (DBA) [8] and insulated metal baseplate (IMB) [9]. Another way is to improve the manufacturing process to enhance the bonding strength of the material interface by applying thick printed copper (TPC) technology [10] and active metal brazing (AMB) [11]. The other method is to optimize the structure of the copper layer, which is discussed in this paper.

According to the research by Pietranico et al. [12], the elastic-plastic behavior of the copper layer affects the fatigue life of the DBC. The mechanical optimization of the copper layer is another way to improve substrate performance. Researches show that the decrease in copper layer thickness can extend the lifetime of DBC in thermal cycling by 10 times [13]. However, it is not practical to reduce the thickness of the conductor layer under high current application, so the methods to equally reduce the thickness of the copper layer edges are proposed by many researchers. The methods including dimple setting [14], edge tail [15], step edge [16], and lattice mesh [17] are analyzed by the finite element (FE) method and experiments. In these methods, all FEM analyses and tests are based on simplified symmetric models with only one side edge or corner to discuss the stress-strain behavior. However, Higher stress or first delamination is found in ceramic around the inside edge between top copper layers when the top copper layer is separated into parts [18], [19]. But no research has been found on explaining such a phenomenon.

Through theoretical and FEM analysis on a DBC sample used on a diode module, the mechanism of the phenomenon was discussed in this paper and a method to decrease the thermal-induced stress on the ceramic interface was also proposed. This paper is organized as follows: in section II, the influences of the layout difference between DBC top and bottom copper layers on stress distribution on the ceramic interface under thermal cycling are analyzed by theoretical explanation and FE method, which demonstrates the layout difference between the top and bottom DBC copper layers. In section III proposed a bottom design using parallel dimple trace to decrease the thermal-mechanical induced stress and strain influenced by the layout difference between the top and bottom DBC copper layers. In section IV, the increase in the thermal resistance of the sample module with the bottom trace design is analyzed by the FE method and thermal resistance measuring test.

II. DBC FAILURE MECHANISM CONSIDERING COPPER LAYOUT

A DBC model with a top copper layer in two parts and a bottom copper layer in one part is taken as the sample to explain the influence of the copper layout difference in the two copper layers as shown in Fig.1. The sample is simplified as a two dimensions cylindrical bending model in Fig.2. Since the top interface and bottom interface have opposite bending direction, the three layers of DBC are divided into two bi-material systems to analyze the stress by using the simplified Timoshenke’s bi-material model [20] as shown in Fig.2.

The strain in thickness z in Timoshenke’s model can be expressed by:

\[
\varepsilon = \varepsilon_B + \frac{z}{h} (\varepsilon_T - \varepsilon_B)
\]  

where \( h \) is the total thickness of the bi-material system, \( \varepsilon_B \) is the bottom strain of the system, \( \varepsilon_T \) is the top strain of the system, and the stress \( \sigma \) in each layer can be expressed by:

\[
\sigma = \frac{E_i}{1 - \nu_i} (\varepsilon_B + \frac{z}{h} (\varepsilon_T - \varepsilon_B) - \alpha_i \Delta T)
\]

where \( E_i \) is the elastic modulus of the \( i_{th} \) layer, \( \nu_i \) is the portion ratio of the \( i_{th} \) layer, \( \alpha_i \) is the thermal expansion coefficient of the \( i_{th} \) layer, \( \Delta T \) is the temperature difference.

The force and bending moment inside each layer can be expressed by:

\[
P_i = \int_{z_{i-1}}^{z_i} \sigma dz
\]

\[
M_i = \int_{z_{i-1}}^{z_i} z \sigma dz
\]

Considering the system is self-balance, the following conditions must be satisfied:

\[
\sum_{i=1}^{N} P_i = 0
\]

\[
\sum_{i=1}^{N} M_i = 0
\]

Combining (5) and (6), the top and bottom strain can be obtained:

\[
\varepsilon_B = \frac{h \Delta T}{F} [4(D_1 - C_1)(A_3 - B_3) - 3(D_2 - C_2)(A_2 - B_2)]
\]

and

\[
\varepsilon_T = \frac{h \Delta T}{F} [3(D_2 - C_2)(2hA_1 - 2hB_1 + B_2 - A_2) - 2(D_1 - C_1) (3hA_2 - 3hB_2 + 2B_3 - 2A_3)]
\]
is higher at the inner edge than one at the outer edge. The FE result is smaller than the derivation above because the FE analysis has considered the yield effect. Both stress results are higher than the bending strength of AlN ceramic which is 350Mpa. Such DBC under reflowing soldering temperature higher than 250°C may suffer cracks at the inner edge, so some optimization on such DBC is needed to relieve the stress.

A simple method to relieve the stress on the interface is to apply top and bottom copper layers in the same layout. Such a method requires ceramic high mechanical strength as discussed in section III, which is not suitable for the stand-alone DBC substrate. The reduction in bottom copper also reduces the thermal conductivity of module packaging as discussed in section IV. FEM analysis on sample A shows that stress relieving methods like dimple setting at the edge of the copper pattern can decrease the outer edge stress on the top ceramic interface entirely, but the stress at the inner edge is still high as shown in Fig.5(b). Therefore, a method to decrease the concentrated stress by changing the bottom copper pattern is proposed in section III.

### III. MECHANICAL BEHAVIOR OF DBC WITH BOTTOM COPPER DESIGN

A simple way to decrease the stress concentration discussed above is to apply the top and bottom copper with the same layout. But simulation shows that DBC substrate with a bottom gap stands about 40% less mechanical load compared to DBC with a connected bottom copper shown in Fig.6. This method also causes a 5% rise in thermal resistance in the packaging system as discussed in section IV. Under consideration of both the mechanical behavior and thermal behavior of the DBC substrate, a compromised method is discussed as follows.

#### A. DESIGN ON PARALLEL DIMPLE TRACES

A bottom design using parallel dimple traces is proposed to decrease the uneven stress distribution affected by the top and bottom copper layer layout differences. The sample designed to testify the method and the trace setting on the bottom copper pattern is shown in Fig.7, the dimple center is on the line of the bottom copper layer opposite to the inner edge of copper patterns on the top layer. A gap with an adjustable size
is set to relieve the inner corner stress on the top copper layer. Because of the technological limitation, the dimple diameter $d$ (mm) and minimum distance $w$ (mm) between the two dimple circles must satisfy: $d \geq 0.4$, $w \geq 0.2$.

The von-mises stress distributions of models with different $d$ and $w$ under 250°C are shown in Fig.8. The dimple trace can decrease the stress on the top ceramic interface to a safe value lower than the ceramic bending strength 350Mpa. The results show that the maximum stress decrease when $d$ increase and $w$ decrease. Since the accumulated plastic strain of copper affects the fatigue life of DBC [22], The max equivalent plastic strains of top copper at corner points A and B during thermal cycling are analyzed. According to the FE results, the plastic strain at point A changes very little with or without dimple traces on the bottom copper layer. It can be found that the plastic strains at points A and B become close when $d=0.2$, and $w=0.2$. When the diameter $d$ increase to 0.4, the plastic strain at point B becomes lower than the one at point A as shown in Fig.9. The warpage of models after single thermal cycling is smaller when $w$ decreases and $d$ increases as shown in Fig.10.

The ductile metal failure under periodic plastic load is within a limited number of life cycles, e.g. below about $10^5$ cycles. The life of such low cycle fatigue (LCF) can be predicted by the well-known Coffin–Manson law based on
C. Zhang et al.: Stress-Relieved Method Based on Bottom Pattern Design

VOLUME 10, 2022

plastic strain amplitude \([23]\). For DBC fatigue with extremely low cycle fatigue (ELCF) life, the prediction model based on the modified Coffin–Manson law is proposed by Xue \([24]\). The expression is shown below:

\[
N = \frac{1}{2} \frac{e^{\alpha} - 1}{e^{\alpha(\frac{\epsilon_d}{2})^\beta} - 1} \quad (9)
\]

where, \(N\) is fatigue life, \(\alpha\), and \(\beta\) are material constants, and \(\epsilon_d\) is a function of the three principal components of the plastic strain tensor. \(\epsilon_f\) represents the plastic strain when the ductile material has failed. The results of DBC substrate thermal fatigue experiments from the supplier showed that the substrate failed after one thermal cycle at the range of -55°C to 600°C. For DBC substrates under high-temperature cyclic loading, \(\epsilon_f\) and \(\epsilon_d\) can be obtained by the calculation of the corresponding plastic strain of copper using the FE method \([25]\). The material constants in equation (1) were fitted to be \(\alpha = 2.7\), \(\beta = 1.76\) by the experimental results on OFHC in the DBC substrate \([25]\).

Based on the life prediction model and calculated strain from FE methods, the predicted life of DBC substrates with different bottom designs under thermal cycling using the FE method is listed in table 3. The predicted life of the substrates matches the test results in the following section B.

TABLE 3. The predicted fatigue life of DBC substrates with different bottom designs.

| Thermal ranges          | \(d/ w (\text{mm})\) | \(N\)  |
|-------------------------|-----------------------|-------|
| -55°C to 175°C          | No trace              | 72.85 |
|                         | 0.4/0.2               | 100.56|
|                         | 0.8/0.2               | 107.32|
| -55°C to 250°C          | No trace              | 14.22 |
|                         | 0.4/0.2               | 20.50 |
|                         | 0.8/0.2               | 22.04 |

B. THERMAL SHOCKING TESTS

Three groups of samples with parameters listed in the table 4 are tested under a thermal cycling test to verify the effect of dimple trace on DBC fatigue life. The test is designed according to the standard of JESD22-A104D with a higher temperature limit to accelerate fatigue propagation. The measured temperature inside the tested chamber is shown in Fig.11. The capacitance of the same tested sample is measured as a reference to indicate the failure criterion of DBC delamination in Fig.12. The samples shown in Fig.13 are determined failure when the capacitance is reduced by 5% \([16]\), \([23]\). The test results show that DBCs with dimple traces on the bottom copper have a longer lifetime than the DBCs without bottom dimple traces which stands less than average 11 TC times under thermal cycling from -55°C to 250°C. Fig.14 shows that the average lifetime of samples with a dimple diameter of 0.4mm is a little higher than the samples with a dimple diameter of 0.2mm. Less crack is observed at the inner edge of samples with a bottom dimple trace after the tests.

The increase in dimple diameter has benefits on inner edge fatigue life according to the FE analysis and the test results, but it also weakens the supporting strength of the bottom copper and affects the thermal resistance in the packaging system discussed in section IV. If the maximum stress is lower than the bending stress of ceramic under the highest loading...
temperature, the selection criteria of design parameters \( d \) and \( w \) just need to satisfy that corner points of the top copper pattern experience similar strain behavior during thermal swings under lifetime consideration.

### TABLE 4. Dimple trace parameters of tested samples.

| Group | \( d \)(mm) | \( w \)(mm) |
|-------|-------------|-------------|
| A     | No trace    | No trace    |
| B     | 0.4         | 0.2         |
| C     | 0.8         | 0.2         |

### IV. THERMAL PERFORMANCE OF POWER MODULE BASED ON DBC WITH DIMPLE TRACES

Diode modules are fabricated using DBC samples with the different bottom copper layouts listed in the table. 5 to verify the bottom copper layout’s influence on the thermal resistance of the packaging system. The packaging system of the module shown in Fig.15 consists of the terminal, conformal coating, bonding wire, chip, solder, and DBC. The chip position is referred to as a commercial module with a clearance of 1mm to the insulation gap. The material thermal
TABLE 6. Thermal material properties of the diode module.

| Material      | Thermal conductivity /W m⁻¹K⁻¹ |
|---------------|--------------------------------|
| Copper        | 393                            |
| AlN ceramic   | 180                            |
| SiC die       | 490                            |
| Solder        | 57                             |
| Thermal grease| 1                              |

FIGURE 16. (a) Diode module with black conformal coating; (b) Heatsink with hole for thermal couple placement.

FIGURE 17. IR image of sample module under 10A current.

properties of the module are listed in the table.6. The sample module is mounted on a heatsink with thermal grease shown in Fig.16. The thermal resistance measurement is set up under DC forward current heating and air cooling. A thermocouple is set beneath the center of the chip position in the heatsink to measure the top surface temperature $T_H$ of the heatsink. The junction temperature $T_J$ of the single-chip is observed by an IR camera shown in Fig.17. A DC source provides a constant 10A current through the diode and the forward voltage of the diode module is acquired by a voltage probe on a source meter.

The tested thermal resistances of the three modules are shown in the table.7. The junction to heatsink thermal resistance $R_{J−H}$ of module 3 rises by 5% compared to module 1. To better explain the influence of the DBC bottom layout on the thermal resistance of the packaging system, a FE model which consists of the solid parts in Fig.15 is built. The model is simulated under the same heating and cooling conditions. The simulated temperature distribution of the modules is shown in Fig.18. The thermal resistance of each packaging material is listed in the table.8. On the comparison of the thermal resistance difference between the modules, it can be found that the thermal resistance of grease in module 3 is about 10% larger than the one in module 1. From both the test results and FE simulations, the module with dimple parameters $d = 0.4$ and $w = 0.2$ has an $R_{J−H}$ difference of less than 2% from module 1. The analysis discussed above shows that the design on the bottom copper layer should consider the design’s influence on the thermal resistance of the grease or other thermal interface material. When the dimple trace design can even the stress and strain distribution on the top ceramic interface, the parameters $d$ and $w$ should be chosen as small as possible to maintain the thermal resistance of the packaging system.

TABLE 7. Test results of thermal resistance.

| Module | $T_J$/°C | $T_H$/°C | P/W  | $R_{J−H}$/°C·W⁻¹ |
|--------|----------|----------|------|------------------|
| 1      | 79.0     | 49.4     | 15.6 | 1.90             |
| 2      | 82.8     | 51.7     | 16.1 | 1.93             |
| 3      | 83.4     | 53.9     | 14.8 | 1.99             |

TABLE 8. FE results of material thermal resistance in sample module.

| Module | $R_{solder}$/°C·W⁻¹ | $R_{DBC}$/°C·W⁻¹ | $R_{grease}$/°C·W⁻¹ |
|--------|---------------------|------------------|---------------------|
| 1      | 0.31                | 0.33             | 1.12                |
| 2      | 0.31                | 0.33             | 1.16                |
| 3      | 0.31                | 0.33             | 1.24                |
V. CONCLUSION
The influences of the top and bottom copper layout differences on the stress distribution of the ceramic interface under thermal cycling are discussed in this paper. A bottom dimple trace design to decrease the thermal-mechanical stress and strain influenced by the layout difference is proposed and investigated. The thermal resistance of the sample module based on the design is also analyzed by the FE method and thermal resistance measuring test. The design’s influence on mechanical strength and thermal conductivity is analyzed. From the analysis, we concluded that:

1. High stress concentrates on the inner gap edge of the top copper patterns when the DBC top and bottom copper layers have different layouts. The stress is composed of two shear stresses caused by bending actions on two interfaces of DBC.

2. DBC with a designed bottom dimple trace has a longer lifetime than DBC with no treatment under thermal cycling. The bottom dimple trace can optimize the stress distribution on the top ceramic interface and influence the inner corner plastic strain behavior of top copper patterns. The increase in dimple diameter and the decrease in dimple distance can decrease the accumulated plastic strain of copper at the inner corner.

3. DBC bottom design should consider the influence on the thermal resistance of DBC-based modules. The change in the thermal resistance caused by the DBC bottom trace is mainly influenced by the grease layer. Bottom dimple trace with a diameter of 0.4mm and distance of 0.2mm can offer a twice longer life under -55°C to 250°C with only a 2% thermal resistance rise.

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