Design and analysis of high speed low area-power semi-custom standard library cells using 90nm MOCMOS technology

Veera Boopathy.E¹, Usha.M², Swathi.R³, Usha.A⁴, Subhashree.N⁵

¹Assistant Professor, Department of ECE, Er.Perumal Manimekalai College of Engineering, Hosur.
²,³,⁴ UG Scholar, Department of ECE, Er.Perumal Manimekalai College of Engineering, Hosur.

Abstract — In this project, we are designing a standard library cell with 90nm technology using GNU/Electric with MOCMOS technology. The library cell consists of 24 cells with each cell having the following views: Icon, Schematic and Layout. The standard library cell includes Basic Gates, Adder circuits, Flip-flops, Latches and Multiplexers. The parameters: Rise Time, Fall Time and Area for all these cells are calculated and listed in a table. Area of each cell in this library is compared with 180nm (CMOS Cells) and 300nm (MUD Library) technologies. Simulation of each cell is done using LT-SPICE software. GDS file is generated for these cells and 3D view of the layouts is also shown.

Keywords— Standard library cell, 90nm technology, Layout, Schematic, Electric

1. Introduction

The increasing demand for system integration by combination of transistors along with less power dissipation has been in development with the CMOS technology. The recent usage of deep sub-micron tenure was due to the rise in demand for integration of much more components on to a single chip for better performance with less power consumption. ASIC consists of logic blocks which are pre-designed and pre-verified in system library functions which lead to the success for the rapid increase of integrated system. This further helped designers to reduce the time for product development and to manage ramifications by adding more and more transistors. Standard cell methodology is a phenomenon of designing ASICs (Application Specific Integrated Circuits) that is used in designing semiconductors with digital-logic features. It is shown as an example of design consideration by enclosing the low-level VLSI- layout into an abstract logic representation.

A NOR 2 input and NAND 2 input function is adequate to design a random Boolean function set. But in present ASIC design, standard library cell methodology is exercised with a scalable library cells which has many implementations of similar logic function, with varying speed and area. This variety embellishes the drastic amount of efficiency of placement and routing (PNR), automated synthesis tools.

A technology library is formed by a complete group of standard cell descriptions. The choice of library decides the efficiency and economic accomplishment of ASIC design. Hence the design requirement is fulfilled. There are an unlimited number of products like mobiles, processors, televisions etc that uses characterized IC components. A digital IC can be fabricated using similar basic steps with the help of different methodologies. Fabrication steps starts with transistors, wiring etc, which is designed using Computer Aided Design (CAD) tools. This helps in physically realizing the chip. Depending upon the requirements, we have three different design approaches.

Full custom design is the process of developing the layout from the scratch. Designs can be altered for increase in speed, capacitive load, area etc. All the wires in layout are placed manually. The designer has the freedom to properly optimize his designs based on the requirements. There is an accessible advantage in the layout so that it can be created very precisely. Semi-Custom design is the process of
importing cells from already available standard library cells to complete the design. A supplier creates gates such as buffer, NAND, NOR etc. and distributes them as library cell which can be further used by the designer. The designer will place logic blocks in the layout as per the desired specification. The advantage in this approach is the decrease in the required time. The combination of semi-custom and full-custom is a very good approach to create the logic gates manually and optimize.

Automatic Design is a process that generates layouts automatically and checks the circuits by comparing them with the created library cell. The design can be created using HDL (Hardware Description Languages) like VHDL or Verilog. In order to meet the required constraints, optimization of the generated layouts are performed through CAD tools. Though the optimization can be performed in different ways, the designer doesn’t have any control over the layout generation. Using this design less optimized layouts are designed when compared with other two designs. However, automatic design is a very useful tool when the design to be created does not have very strict requirements and when the time to market is more important than a fully optimized design.

A Boolean logic or a storage function can be implemented using a standard library cell which consists of a set of transistors. A NAND or a NOR gate can be used to generate any Boolean function. The design’s area can be reduced by using other logic gates. The basic gates such as Buffer, Inverter, AND, OR, etc. universal gates such as NAND and NOR and other gates such as XOR and memory cells are the components found in any standard library. Complex libraries consist of several other cells such as adders and multipliers.

Initially, the standard cell is designed by implementing the functionality of the cell at a transistor level. It is done by drawing a schematic. Simulation and debugging is done to ensure proper operation. The representation of the schematic of a cell is done using a symbol which is composed of the input and output ports of the cell. Text information can also be included in it. For simulation purposes, the netlist is useful. Hence it is required to design the layout view. Although it is not used for fabrication it is compulsory. Many base layers are combined to form a layout which basically consists of interconnect lines and transistor structures. The layout of a cell represents what will be physically placed on a chip. Though there are many CAD tools that assist the procedure of design, we still face challenges in designing efficient layouts that could meet the required constraints. The designed layouts are repeatedly checked to ensure that the design rules are not violated (called as Design Rule Check). In order to check the consonance of the layout with its corresponding schematic, Layout versus Schematic (LVS) is performed. After the parasitic extraction, post layout simulation is performed. The placement-and-routing tools are given details about the height and width of cells along with dimension and location of their input and output pins. The layouts are directed to the Abstract Generator, where the Library Exchange Format (LEF) file is produced. LEF files also give information about the technology’s spacing and thickness and the minimum width of the layers present. The layout information of the schematics that we create is available as a GDS (Graphic Database System) file which can be sent for fabrication purposes.

The process flow for creating a library cell is shown in fig.1. The creation of standard cell started with schematic diagrams of the circuits which were then converted to their respective symbols. Using the schematics, the layout structure is designed according to the Lambda (λ) rules from transistor level. After the completion of layout, DRC (Design Rule Check) is done to check for errors. In order to ensure that the layout and schematic of circuits are identical, LVS is performed. The simulation for the layout is carried out using an additional software called LTSpice to notify the operation of each circuit. This software also helps us in calculating the necessary parameters like rise and fall time. This software needs to be linked with Electric and the cells need spice code to run the simulation. After verification the node extraction is done and characterization of each cells are performed. Finally, the Standard Cell Library is created by dumping all the cells.
2. Standard cell design

A. Standard Cell

The Standard Cells are made such that the height is fixed with varying width full-custom cells. This enables them to be placed in rows so that the process of programmed digital layout is done easier. Standard Cells are logic elements including gates, adders, flip-flops and latches that are available in a library cell for designing an IC. Custom design corresponds to cell designs and standard cells using MOSFET’s.

B. Standard Cell Architecture

Some important considerations while designing standard cell architecture are:

1. DRC
2. Pitch
3. Power Rail Width
4. Tap Cell
5. Device Size
6. Pin Accessibility

3. Implementation Strategies using EDA Tools

A. Electric EDA

The open source Electric VLSI Design System was written by Steven M. Rubin in the early 1980s. It is an EDA tool which has the following forms of circuit:

- Schematic Capture (digital and analog)
- Custom IC layout
- Textual Languages (such as VHDL and Verilog).

B. LTSpice

LTSpice is free computer software which is used for implementing SPICE simulator for electronic circuits. Semiconductor manufacturer LTC (Linear Technology) created this software. To speed up the simulation of regulators, it provides a waveform viewer with improvements.

C. GDSII file viewer

GDSII is a database file format. This format is used in the industry for an IC fabrication. The GDSII file is in binary format. As the creation of layout is finished the layout file is been exported.
from JELIB format file to gds file and this GDS file format which is in binary form is then given to the foundry for the fabrication of the IC’s.

D. 3D view of CLA layout

Electric has an extra special ability to view the designed layout in a 3 dimension. The fascinating part of 3D viewer is that we are able to view the complete structure if the layout which we have designed. While displaying 3D, we can zoom, pan and rotate the image for better vision, and no changes can be done to the circuit once the 3D window is opened. 3D window can be opened only if the JAVA 3D viewer is installed in the system.

E. Lambda (\(\lambda\)) Rules for Designing IC Layout

![Fig.2. Lambda based rules](image)

Design rules are the basic parameters which are to be followed before implementing the circuit onto the silicon wafer as shown in fig.2. It allows circuit translation into actual geometry in silicon. It also acts as an interface between the layout designer and the fabricator. These rules are used to provide reasonable yield with specific mask geometry. In the figure we can observe that the spacing between metal layer and polysilicon is designed based on lambda rules. The spacing between the two metal-1 layers should be \(3\lambda\). The spacing between two polysilicon’s should be \(3\lambda\). The metal layer and the polysilicon layer can overlap each other as they come in different layers during fabrication. The separation between the contacts should be \(3\lambda\), with contacts having an area of \(2\lambda^2\).

4. Arithmetic and Logic Unit

The ALU (Arithmetic and Logic Unit) is a main and crucial part in a CPU (Central Processing Unit). The ALU is used in almost every computing application for all logical and mathematical operations. It is a multi-functional circuit which can perform many operations such as AND, NOR, addition, subtraction, etc. without depending on control units. Figure 3.1 shows a 1-bit ALU, which is formed with AND gate, OR gate, full adder, and three 2to1 multiplexers. It performs AND, OR, addition and subtraction operations. Here the AND gate and OR gates are used for directly performing AND OR operations and the full-adder performs the addition and subtraction operations. A multiplexer is used to control the operations. The other two multiplexers are used for sending the right operation result to the output. Hence, the 1-bit ALU is formed with six gate level components [3].
5. Design of 90nm Standard Cells

A. NAND Gate

NAND gate is formed with two PMOS transistors connected in parallel and two NMOS transistors connected in series. Fig.3. shows logic diagram and fig.4 shows the schematic diagram of a 4 input NAND gate.

![NAND_4 icon](image)

Fig.3. NAND_4 icon

The PMOS transistor's source is connected to VDD and NMOS transistor's source is connected to ground. The inputs A and B are the inputs of the NAND gate, and A NAND B is the output. When both the inputs A and B are HIGH, the output A NAND B is LOW while rest of all cases the output is HIGH.

![NAND_4 schematic](image)

Fig.4. NAND_4 schematic
Fig. 6 shows the simulation results for the NAND gate. Fig. 5 shows the layout diagram of a NAND gate. Polysilicon-1 contact is used for input A and B while the metal-1 pin is used for output A NAND B. Table 1 shows rise time and fall time simulation results for 4 input NAND gate.

| TABLE 1 NAND_4 RESULTS |
|-------------------------|
| RISE TIME (NS)          |
| FALL TIME (NS)          |
| AREA (PM^2)             |
| 146.5                   |
| 183.8                   |
| 7.29                    |

B. Inverter

The inverter is a most important and central block of all digital designs. The working principle of the inverter is that when the input is connected to ground, the output is pulled to VDD through the PMOS. When the input is connected to the source, the output is pulled down to ground through the NMOS. The inverter has one p-channel transistor and one n-channel transistor which are connected to source and ground, respectively [3].

Fig. 7 shows the transistor level diagram of an inverter. It has a PMOS and NMOS connected in series, and also a voltage source VDD and ground are connected to these transistors.
Fig. 8. Inverter Schematic

Fig. 9. Inverter Layout

Fig. 10. Inverter Simulation
Fig. 9 shows the physical diagram of an inverter, the PMOS and NMOS transistors are drawn as devices. The input port \( V_{in} \) formed with Polysilicon-1 contact and Metal-1 pin is used for the \( V_{out} \) port. Only Metal-1 arc and polysilicon arc is used for connecting the devices. The layout area of the implemented Inverter is 58.3 \( \mu \)m \( \times \) 12.2 \( \mu \)m. Fig. 10 shows the simulation result for an inverter. When \( V_{in} \) is HIGH the output at \( V_{out} \) is LOW. Similarly, when \( V_{in} \) is LOW the output at \( V_{out} \) is HIGH. The rise time, fall time and layout area analysis of the implemented inverter is tabulated in table 2.

### Table 2 Inverter Results

| Rise Time (NS) | Fall Time (NS) | Area (PM\(^2\)) |
|----------------|---------------|-----------------|
| 3.191          | 3.206         | 3.402           |

C. Multiplexer

The multiplexer is a digital switch that has multiple inputs and a single output. It chooses one of many inputs and sends a single output through it with the help of control inputs. Here a 2 to 1 multiplexer is used to build the 8-bit ALU. Transmission gates are used to build the multiplexer. A transmission gate is a complementary switch, which is formed by parallel connection of PMOS and NMOS transistors.

Fig. 11 Multiplexer Icon

Fig. 11 and fig. 12 display the schematic diagram of a multiplexer. It is built with two transmission gates and one inverter. A total of 6 transistors is used to create the multiplexer.

Fig. 12 Multiplexer Schematic
Fig. 13 shows the layout diagram of the multiplexer. Metal-2 contacts are used for inputs A and B, polysilicon-1 contact and metal-1 pin are used for the S and Z respectively. The layout area analysis of the implemented MUX is listed in table 3.

![Fig.13 Multiplexer Layout](image)

| RISE TIME (NS) | FALL TIME (NS) | AREA (PM²) |
|---------------|---------------|------------|
| 6.01          | 5.988         | 9.416      |

D. Full Adder
Adders play a very crucial role in VLSI systems. Microprocessors, digital signal processing architectures, parity checkers, etc. use adders in their applications. Here a full 28 transistor conventional adder is implemented. In static CMOS, the NMOS passes 0’s, and PMOS passes 1’s hence the levels will never be degraded. The advantages of CMOS full adders is that the layout is straightforward since the transistors are complementary, and it has high noise margins and stability at low voltages due to a complementary pair of transistors [1]. Other than the A and B inputs it also has a Cin input which is the carry of the sum from the previous operation. Cout and sum are the outputs of the full adder. Fig.15 shows the schematic diagram of a full adder. Fig.16 shows the layout diagram of a full adder. Here polysilicon-1 is used for A and B inputs, and the metal-2 pin is used for Cin input. The outputs are formed with metal-1 pins. For connections, poly arc, metal-1 arc, and metal-2 are used in drawing the full adder layout circuit. The layout area of the implemented adder is 306.9_m_406.2_m. Fig.17 shows the simulation results for a full adder. When A is 1, B is 0, and Cin is 0 the sum is 1 and Cout is 0. Similarly, when A is 1, B is 0 and Cin is 1 then the sum is 0 and Cout is 1.

**Fig.15 Full Adder Icon**

**Fig.16 Full Adder Schematic**
6. Results and Analysis

The simulation results for area parameter measured in pm2 is listed in table 5 along with comparison analysis of proposed 90 nm library, MUDD library of 300nm and CMOS library of 180nm is also tabulated.

| TABLE 5 AREA COMPARISON |
|-------------------------|
| CELL | OUR LIBRARY | CMOSS CELL S (180) | PERC ENTA GE IMPR | MUD D LIBRARY | PERC ENTA GE IMPR |
|------|-------------|-------------------|-----------------|----------------|------------------|
|      |             |                   |                 |                |                  |

Table 4 FULL ADDER RESULTS

| RISE TIME (NS) | FALL TIME (NS) | AREA (PM²) |
|----------------|----------------|------------|
| 0.1653         | 0.3883         | 33.145     |
|       | Y     | NM)   | OVED | (300 NM) | OVED |
|-------|-------|-------|------|----------|------|
| AND_2 | 5.88  | 30.03 | 80.399 | 890.775  | 99.339 |
| AND_3 | 8.26  | NA    | NA    | NA       | NA   |
| AND_4 | 8.62  | NA    | NA    | NA       | NA   |
| AOI22  | 7.34  | 36.45 | 79.852 | NA       | NA   |
| CLK_B | 4.71  | 26.268| 82.046 | NA       | NA   |
| CLK_I | 3.40  | 20.435| 83.352 | NA       | NA   |
| BUFFER | 4.71  | 25.74 | 81.678 | 317.79   | 98.516 |
| HALF  | 21.4  | 88.775| 75.789 | NA       | NA   |
| ADDER  | 19.4  | 93    | 88.775| NA       | NA   |
| FULL  | 33.1  | 148.40| 77.665| 1319.7   | 97.488 |
| ADDER  | 3.40  | 20.46 | 83.372| 240.75   | 98.586 |
| INVERTER | 9.41  | 48.91 | 80.748| 702.99   | 98.661 |
| MUX    | 9.41  | 48.91 | 80.748| 702.99   | 98.661 |
| D-    | 32.5  | 64.46 | 49.482| NA       | NA   |
| FLIPFLOP | 64    | 64.46 | 49.482| NA       | NA   |
| NAND  | 4.61  | 25.46 | 81.865| 317.79   | 98.547 |
| NAND_2| 4.61  | 25.46 | 81.865| 317.79   | 98.547 |
| NAND_3| 5.94  | 30.82 | 80.724| 394.83   | 98.495 |
| NAND_4| 7.29  | 39.53 | 81.558| 471.87   | 98.455 |
| NAND_5| 8.89  | 39.53 | 81.558| 471.87   | 98.455 |
| NOR_2 | 4.73  | 30.15 | 84.285| 317.79   | 98.509 |
| NOR_3 | 5.46  | 35.175| 84.457| 394.83   | 98.615 |
| NOR_4 | 6.91  | 40.2  | 82.80 | 471.87   | 98.534 |
| NOR_5 | 8.01  | NA    | NA    | NA       | NA   |
From the above table we can conclude that our library is far more area efficient when compared with the other libraries. When compared with MUDD library (300nm) which is older technology, our library (90nm) is much more area efficient than that. And also, it is more area efficient when compared with CMOS library (180nm).

7. Conclusion

A standard cell library for designing Application specific Integrated Circuits (ASIC’s) using 90nm CMOS MOSIS technology is created which includes Basic gates, Adder circuits, multiplexers, flip-flops and latches. The library consists of 24 cells each with the following views: Schematic, Icon and Layout. This cell can be used in complex circuit design. 3D structure is also shown for some circuits. From the table it can be concluded that there is a substantial amount of reduction in area when compared to technologies of 180nm and 300nm. Also, other parameters like Rise Time, Fall Time and Area is given for each cell.

8. REFERENCES

[1] Electric manual 9.07, by Steven M Rubin
[2] RajKumar Mistri, Rahul Ranjan, Pooja Prasad, Anupriya, “IC Layout design of 4-Bit Universal Shift register using electric VLSI Design System”, Vol.6 Issue 4, IJERT, 2017.
[3] Lily Kanotiya, Aparna Guptha, Dr.Soni , “Layout Designing and Transient Analysis of Carry Look Ahead Adder Using 300nm technology-A Review”, Volume 4 Issue 2, IJEDR, 2016.
[4] Upendra Chary Chokkella, Aravind Alampally, “IC Layout Design Of Decoder Using Electric VLSI Design System”, Vol. 3, Issue 7, IRJET, 2016.
[5] Soh Hong Teen and Li Li Lim, Jia Hui Lim, “IC Layout Design of Decoder Using Electric VLSI Design System”, International Journal or Electronics And Electrical Engineering Volume.3, No.1, Feb-2015.
[6] L.Jin, C.Liu and M.Anan, “Open Source VLSI CAD Tools : A Comparative Study”.
[7] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation, John Wiley & Sons, 2010, pp. 6-12.
[8] A. P. Douglas and E. Kamran, Basic VLSI Design, third edition Prentice Hall, 1994, pp. 72-76.
[9] Peter Cheung, “Layout Design”, Department of Electrical & Electronic Engineering Imperial College, London.
[10] About Electric [online] available: www.staticfreesoft.com/electric.html