Complete Double Node Upset Tolerant Latch Using C-Element*

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SUMMARY The recent development of semiconductor technology has led to downsized, large-scaled and low-power VLSI systems. However, the incidence of soft errors has increased. Soft errors are temporary events caused by striking of α-rays and high energy neutron radiation. Since the scale of VLSI has become smaller in recent development, it is necessary to consider the occurrence of not only single node upset (SNU) but also double node upset (DNU). The existing High-performance, Low-cost, and DNU Tolerant Latch design (HLDTL) does not completely tolerate DNU. This paper presents a new design of a DNU tolerant latch to resolve this issue by adding some transistors to the HLDTL latch.

key words: single event upset (SEU), double node upset (DNU), soft error, C-element

1. Introduction

The recent development of semiconductor technology have led to downsized, large-scaled and low-power VLSI systems. However, the incidence of soft error has increased. In past days, for only memory systems, soft errors were a serious issue. However, soft errors on logic circuits as well as memory systems have become of serious in recent years [1]–[3]. So, it is necessary to design logic circuits capable of tolerating soft errors. Soft errors are caused by striking of α-rays and high energy neutron radiation. Collision of α-rays and neutron rays can generate electrons and holes in transistors and then they are then collected at the drain. The collected electrons or holes lead to transient voltage [4]. As a result, the output value of the transistor is temporarily inverted. This is called a single event effect, and the inversion of data stored in a storage element such as a flip-flop is called a soft error. Soft error tolerant schemes have been studied to resolve this issue. Traditional soft error tolerant schemes target single node upsets (SNUs). However recent miniaturization and high integration of VLSI incur double node upsets (DNUs). So, recent soft error tolerant schemes target DNUs as well as SNUs.

The dual interlocked storage cell (DICE) is well-known representative structure having soft error tolerance. The DICE cell has a feedback loop constituted by a clock-controlled input and an inverter. The DICE latch [5] is a primitive latch using DICE cell. This latch does not have DNU tolerant capability. It can tolerate only SNUs. The Delta DICE latch [6], the double node upset tolerant (DONUT) latch [7] and the modified low-power DONUT (DONUT-M) latch [8] are DNU tolerant latches using DICE cell. They have DNU tolerant capability. The DONUT-M latch is based on the DONUT latch. The dynamic power consumption and D-Q delay time of DONUT-M latch are lower than those of the DONUT latch. However, these latches using the DICE structure has low stability because they use middle voltage to tolerate soft errors.

Muller C-element is one of elements well-used in soft error tolerant schemes. The C-element has two or more inputs. The output value changes only when all the inputs have the same value. This feature can prevent soft errors at an input from affecting the output value. The C-element handles only binary values, and so it is more stable than DICE structure. Furthermore it has another advantage that C-element consumes less power than DICE. Several soft error tolerant latches using C-elements have been presented, i.e. the high-performance robust (HIPER) latch [9], the feedback redundant SEU/SET-tolerant (FERST) latch [10], and the low cost and highly reliable radiation hardened (LCHR) latch [11] as SEU tolerant latches. The double node charge sharing SEU tolerant (DNCS) latch [12], the non-temporally and temporally hardened latch (NTHLATCH) [13] and the high-performance, low-cost, and double node upset tolerant latch (HLDTL) [14] have been proposed as DNU tolerant latches. However, they require a number of transistors, which incur several penalties such as large area and high power consumption. The HLDTL latch is better than the other two latches in terms of hardware overhead such as area, power consumption and propagation delay. However the HLDTL latch does not have complete DNU tolerant capability as shown in this paper.

This paper presents a new DNU tolerant design using C-elements. The proposed design is based on the existing HLDTL latch. The proposed latch is capable of tolerating DNUs completely. Furthermore the proposed latch accomplishes good hardware overhead.

This paper is organized as follows. Section 2 introduces the conventional method. Section 3 describes the features and configuration of the proposed latch. Section 4 provides simulation and evaluation result. Section 5 concludes the paper.
2. Previous Soft Error Tolerant Latch Design

This section reviews features and constructions of existing soft error tolerant latches using C-element. 2.1 reviews existing latches using C-element other than the HLDTL latch. 2.2 introduces the HLDTL latch, on which the proposed latch is based. Figure 1 explains the symbols and schematic of C-elements and three-state inverter used in this paper.

2.1 Review of Soft Error Tolerant Latches

The HIPER latch [9] is capable of tolerating SNU. Figure 2 (a) shows the construction of this latch. This latch has two independent feedback loops (FL1, FL2). The gates of a PMOS and the corresponding NMOS are connected to nodes different from each other. Even if an SNU changes one of the nodes, either input of the C-element keeps the correct value. As the result, the error does not affect the output value of the C-element. The HIPER latch does not tolerate DNU.

The FERST latch [10] can tolerate SNU. Figure 2 (b) illustrates the construction of this latch. This latch contains three 2-input C-elements. Two of the three form two feedback loops. The outputs of these two C-elements are connected to the input of other C-elements. These outputs are also connected to the output of the latch passing through the other C-element. So errors at the two C-elements never affect the output of the latch. The FERST latch does not tolerate DNU.

The LCHR latch [11] has SNU tolerant capability. Figure 2 (c) shows the construction of this latch. This latch has three independent feedback loops (Part1, 2, 3). Each feedback loop consists of a normal inverter and a three-state inverter controlled by the clock signal. For CK=1, each input value is stored into every feedback. For CK=0, the feedback loop keeps the stored value. The Part 3 is directly connected to the output of the latch, which guarantees that the output of the latch would never be in a high-impedance state even when a soft error occurs. The LCHR latch does not tolerate DNU.

The SEH latch [15] is an SNU tolerant latch. The soft-error hardened (SEH) latch [15] is an SNU tolerant latch. Figure 2 (d) shows the construction of this latch. The SEH latch uses the direction of errors. The nodes PDH and NDH are driven through only PMOS and only NMOS respectively. At the collision of energetic particles, only electrons are collected at the NMOS, so only an error that changes logic 1 to logic 0 occurs. Similarly, since only holes are collected in the PMOS, only an error that changes logic 0 to logic 1 occurs. Therefore, since either PDH or NDH always holds the correct value, the original data can be held.

The DNCS latch [12] is a DNU tolerant latch. Figure 2 (e) illustrates the construction of this latch. This latch has a feedback loop, which consists of six 2-input C-elements. The output of the i-th C-elements is connected to one of the inputs of the next (i + 1 mod 6)-th and (i + 4 mod 6)-th C-elements. For any SNU and DNU, the flipped node value is recovered finally.

The DNCS latch [12] is capable of tolerating DNU. Figure 2 (f) shows the construction of this latch. In this latch, nine 2-input C-elements and three inverters form a feedback loop. The nine C-elements are arranged in a 3×3 array. For any SNU and DNU, it is guaranteed that at least two out of three elements in every column output the correct value. This latch uses many C-elements, which incurs large hardware overhead.

The NTHLTCH latch [13] is capable of tolerating DNU. Figure 2 (g) shows the construction of this latch. This latch has a feedback loop consisting of C-elements. It is designed so that the output of each transistor is not connected to the input of the transistor.

Figure 2 (h) illustrates the construction of the DONUT-M [8] latch, which is based on the DONUT [7] latch. This latch stores values using nine nodes. This system is capable of tolerating DNU as well as SNU.

2.2 HLDTL

The HLDTL is a DNU tolerant latch [14]. Figure 3 shows the construction of this latch. This latch mainly consists of an SNU Resilient Cell (SRC) and a 3-input C-element. The SRC consists of three 2-input C-elements and two inverters. These form feedback loops. The SNU tolerant capability is given by the 3-input C-element which is placed at the output of the SRC cell.

We explain the normal operation of this latch. For CK=1, the latch is transparent. For CK=0, the latch is closed. For CK=1, the transmission gates TG1, TG2, TG3 and TG6 turn on, and TG4, TG5 and TG7 turn off. Since TG3 turns on and TG7 turns off, the input value is output passing through only TG3. This feature accomplishes very short propagation delay. At the same time the input value is stored at the feedback loops in the SRC (including the nodes N1b and N2b) and the node N4. For CK=0, TG1, TG2, TG3 and TG6 turn off, and TG4, TG5 and TG7 turn on. The SRC cell is closed. Since TG6 turn off, the N4 is in the high-impedance state. The previous value of N4 is kept.
Because the inputs of the 3-input C-element (i.e. N1b, N2b and N4) keeps the previous value, the output Q also keeps the previous value.

Next, we explain the operation when a soft error occurs on HLDTL. Upsets can occur on the closed latch. So we consider for only CK=0. For CK=0, TG4 is open. So, we can regard N2 and N2a as the same node N2. Similarly, N1 and N1a, and Q and Qa are also considered as the same nodes N1 and Q.

1) SNU
SNUs can be categorized into two classes: i) SNU in the SRC and ii) SNU outside the SRC. i) If an error occurs on N1, it affects only N1b. Finally the error is recovered by the C-element ce3. If an error occurs at N1b, it does not affect any other nodes. Finally the error is recovered by N1. Similarly, this latch tolerates errors at N2 and N2b. An error at N3 does not affect any other nodes. It is recovered by the C-element ce1. As the result, no error occurs at the output Q. ii) The error at Q does not affect any other nodes. It is recovered by the 3-input C-element ce4. No upsets occur though a transient error pulse occurs at the output. If an error occurs at N4, it is not recovered until the next clock change. However it does not affect any other node. Eventually the latch keeps the correct output value.

2) DNU
Next, we consider the operation for DNUs. DNUs are categorized into three: i) both errors occur in the SRC, ii) one occurs in SRC and the other occurs outside SRC, iii) both occur outside SRC. Here <A, B> rep-
Fig. 3  HLDTL latch [14].

represents a pair of nodes on which a DNU occurs. \(<A, B>\) also represents a DNU occurring on the nodes A and B. i) The SRC cannot tolerate some DNUs. For example, a DNU \(<N1, N2>\) affects \(N1b, N2b\) and \(N3\). Finally the output values of all C-elements in SRC are affected. However, for any cases, the HLDTL latch tolerates these DNUs. This is because they do not affect \(N4\) because TG6 turns off. So, the DNUs in SRC never affect the output value at \(Q\). (This is not always correct as explained later.) ii) If one occurs in SRC and the other occurs outside SRC, the SRC corrects the error inside the SRC as an SNU as mentioned in 1). The error outside SRC (i.e. at \(Q\) or \(N4\)) is also corrected as a SNU in the manner mentioned in 1).

The HLDTL cannot tolerate DNUs in the category iii). The only error categorized into iii) is \(<N4, Q>\). If \(<N4, Q>\) occurs, the value of \(N4\) is erroneously changed while the value of \(N1b\) and \(N2b\) are correct. So the 3-input C-element ce4 tries to keep the previous value. However, the output value of ce4 (i.e. that of \(Q\)) is also erroneously changed. Finally an upset occurs. The nodes \(Qa\) (considered as the same node as \(Q\)) and \(N4\) are connected to the same gate ce4 and so they are placed close to each other. Thus this issue is serious.

Furthermore, the HLDTL cannot tolerate some DNUs in the category i) such as \(<N1, N3>\). Since TG6 turns off, upsets on \(N3\) do not affect \(N4\) in theory. However some transient pulses on \(N3\) can affect \(N4\) passing through TG6 in actuality. This is because the node voltage can be out of the range from logic 0 to logic 1 when an error occurs. For example, Fig. 4 gives an HSPICE simulation waveform of \(N3, N4\) and \(CK\) on HLDTL for the power supply voltage of 1.0 V. Refer Sect. 4 for detail of the simulation environment. We will consider the NMOS transistor in TG6. The gate, source and drain of the NMOS are connected to \(CK, N3\) and \(N4\), respectively. In this waveform, NMOS is in off-state before the time of 5 ns. The gate voltage at \(CK\) is set to 0 V, which is lower than the source voltage at \(N3\).

A transient pulse occurs on \(N3\) at the time of 5 ns and the source voltage \(V_S\) becomes lower than the gate voltage \(V_G\) of 0 V (to be precise, \(V_G - V_S > V_{th}\), where \(V_{th}\) is the threshold voltage). The NMOS wrongly turns on and then the drain voltage at \(N4\) is discharged. From this, transient pulses on \(N3\) can affect \(N4\) and therefore the DNUs in SRC can flip the output value at \(Q\).

3. Proposed Latch

This section presents the features and construction of two proposed latches. First we present the proposed latch 1 by modifying the HLDTL latch to tolerate the DNU \(<N4, Q>\). Subsequently we present the proposed latch 2. As mentioned in 2.2, some transient pulses on the HLDTL latch can affect through pass transistors turned off. The same is true for the proposed latch 1. We construct the proposed latch 2 by modifying the proposed latch 1 to tolerate these transient pulses. The proposed latch 2 is our final proposal in this paper.

Figure 5 shows the construction of the proposed latch 1. As revealed in Sect. 2, the existing HLDTL latch does not
tolerate the DNU <N4, Q>. The proposed latch is based on the existing HLDTL latch. The proposed construction adds a 2-input C-element and an inverter to tolerate <N4, Q>.

Next we explain the error correction. The proposed latch is a DNU tolerant latch. It tolerates both SNU and DNU errors in theory.

1) SNU
SNU errors are categorized into three groups i) on the SRC, ii) on the additional part (i.e. N4, N4_1, N4_2, and N4_3) and iii) errors on Q. i) The proposed latch tolerates errors on SRC in the same manner as the HLDTL latch. ii) Errors on the additional part are not affected to the output value. If an error occurs on N4_3 or N4, it is recovered by ce4. If an error occurs on N4_1 or N4_2, it is not recovered. However, the C-element ce4 prevents the error affecting output node N4_3. As a result, the error does not affect N4 and the output Q. iii) The proposed latch can tolerate errors on Q in the same manner as the original HLDTL latch.

2) DNU
DNUs are categorized into the following five groups: a) both errors occur on the SRC, b) one occurs on the SRC and the other occurs on the additional part, c) both errors occur on the additional part, d) one occurs on the SRC and the other occurs on the output Q, and e) one occurs on the additional part and the other occurs on the output Q.

i) errors on the SRC
The proposed latch tolerates errors on the SRC in the same manner as the original HLDTL latch.

ii) errors on the SRC and the additional part
If single errors occur on both the SRC and the additional part, the SRC tolerates the error on the SRC. As a result, the proposed latch can tolerate.
iii) errors on the additional part
   The additional part cannot tolerate DNU. For some DNU, the output value of the C-element ce4 can flip. This can be regarded as a single error on the node N4 and so the proposed latch can tolerate it in the same manner as the HLDTL latch.

iv) errors on the SRC and Q
   If single errors occur on both the SRC cell and the node Q, the SRC cell tolerates the error on the SRC cell. As a result, the error on Q can be regarded as a single error, which the proposed latch can tolerate.

v) errors on the additional part and Q
   If single errors occur on both the additional part and the node Q, the additional part tolerates the error on it. Even if the value of N4 is flipped, it is recovered. (This is an important difference between the proposed and the original HLDTL latches.) Eventually, the state of the latch for the DNU becomes the same as that for the single error on Q, which the proposed latch can tolerate.

As mentioned in 2.2, some transient pulses can affect through pass transistors turned off. This can affect the proposed latch 1. We can avoid this by using three-state gates in place of pass transistors. Figure 6 illustrates the construction of the proposed latch 2, which uses three-state inverters in the additional parts. This latch can tolerate SNU and DNU in the same manner as the latch 1 of Fig. 5. In addition, this latch is not affected by pulses passing through opened transistors.

Figure 7 shows the layout of the proposed latch 2. The nodes Qa and N4 are connected to the source/drain of transistors close to each other (the third and sixth transistors from right). However, the proposed latch can tolerate the DNU <N4, Q> like the proposed latch 1.

4. Evaluation

This section evaluates the proposed latch by simulation. In this simulation, we simulated the nine existing latches introduced in Sect. 2 and the proposed latches 1 and 2. The simulation uses HSPICE and a 45 nm PTM [16]–[18]. The power supply voltage is 1.0 V and the temperature is 27°C.

Figure 8 shows a waveform diagram for the DNU <N4, Q> occurring on the proposed latch of Fig. 6. In this simulation, errors were simulated using a current source with the double exponential model [19]. Equation (1) gives the current value of the source.

\[ I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}), \]

where Q is the charge, and was set to 15 (fC). The parameters \(\tau_\alpha\) and \(\tau_\beta\) are constant values given in [19]. These parameters are set to the same values as [19]; specifically \(\tau_\alpha = 0.164\) (ns) and \(\tau_\beta = 0.05\) (ns). The DNU was generated at 100 ns. The flipped output value has been recovered to the correct value immediately. This result supports that the proposed latch has DNU tolerant capability.

Table 1 shows the critical charge (\(Q_{\text{crit}}\)) of the existing and proposed latches. In the rows of “proposed 1 and 2”, the results for the proposed latches (shown in Figs. 5 and 6) are given. The critical charge is defined as the minimum charge amount at which the stored value is inverted. Low critical charge means poor soft error tolerant capability. Simulation was done for any stored value. The charge is injected for any nodes (for SNU) and for any pair of nodes (for DNU). For DNU charges with the same amount are injected to the

| latches | SNU | DNU |
|---------|-----|-----|
| HIPER   | -   | 1   |
| FERST   | -   | 1   |
| LCIR    | 1   | 1   |
| SEH     | -   | 1   |
| DNCS    | -   | -   |
| NTHLTC  | -   | -   |
| HRDNTU  | -   | -   |
| DONUTM  | -   | -   |
| HLDTL   | -   | 8   |
| proposed 1 | -   | 10  |
| proposed 2 | -   | -   |

-” means that \(Q_{\text{crit}}\) is larger than 1000 fC.
Table 2 Number of transistors, CK-Q delay (ps) and power consumption ($\mu$W)

| latch    | transistors | delay | power |
|----------|-------------|-------|-------|
| HIPER    | 16          | 5.8   | 2.13  |
| FERST    | 20          | 28.2  | 2.14  |
| LCHR     | 26          | 18.2  | 3.28  |
| SEH      | 14          | 14.4  | 0.93  |
| DNCS     | 42          | 88.5  | 6.51  |
| NTHLTC   | 66          | 14.6  | 5.49  |
| HRDNUT   | 44          | 12.0  | 4.42  |
| DONUTM   | 44          | 5.6   | 4.20  |
| HLDTL    | 36          | 3.4   | 3.34  |
| proposed 1 | 44      | 3.5   | 4.25  |
| proposed 2 | 46      | 3.5   | 4.43  |

nodes at the same time. The charge is changed by 1 fC. These tables give the worst results (the minimum critical charge).

For the HIPER, FERST and SEH latches, the critical charges for SNUs are very high (higher than 1,000 fC). However those for DNUs are low because these latches are not designed to tolerate DNUs. The critical charge of the LCHR latch is very low even for SNUs under this technology. The DNCS, NTHLTC, HRDNUT, DONUT-M and the proposed-2 latches have the complete DNU tolerant capability. The HLDTL and proposed-1 latches do not tolerate the DNU <N1, N3> as mentioned in the previous sections. The critical charges of these latches are 8 fC and 10 fC, respectively, which are low for practical use.

Table 2 summarizes the characteristics (number of transistors, CK-Q delay and average power consumption) of the existing and proposed latches. The average power consumption is measured with a 1 GHz clock signal and an input pattern with data activity of 0.1.

The numbers of transistors of the proposed latches are smaller than that of the NTHLTC latch and comparable to other DNU tolerant latches. The CK-Q delay times of the proposed latches are comparable to that of the HLDTL and shorter than the other existing latches. The dynamic power consumption of the proposed latch is comparable to that of the HLDTL. It is smaller than that of the other existing latches with complete DNU tolerant capability.

5. Conclusion

This paper has presented a DNU tolerant latch using C-element. The proposed latch is based on an existing DNU tolerant latch which has not complete capability. The evaluation gives evidence that the proposed latch was the complete capability. Specifically, the proposed latch is capable of tolerating charges with 1,000 fC while the existing HLDTL latch does not tolerate charges with 8 fC or higher. Furthermore, the CK-Q delay and dynamic power consumption is similar level to or better than the other existing latches with the complete DNU tolerant capability.

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