An Animal Spinal Cord Neural Signal Regeneration Circuit

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Abstract. An animal spinal cord neural signal regeneration circuit is presented in this paper. The circuit consists of an on-chip amplifier which was designed in TSMC 0.18μm 1P6M standard CMOS process and an output circuit using an off-chip high voltage transistor. A low temperature drift bias circuit and a constant-gm rail-to-rail input circuit employing a novel structure called Max Current Selection are designed in the amplifier. The amplifier occupies a die area of 300μm×300μm. The simulation results show that the consumption of the amplifier is about 1.45mW and gain of the whole circuit is 40dB. The output voltage reaches a wide swing of -1V~4V under +5V and -1.5V off-chip power supplies. The circuit is expected to be used in vitro test for regenerating neural signals of animal’s damaged spinal cord nerve, as a new method for trying to cure nervous injury.

1. Introduction
The damage of Central Nervous System, especially the injury of spines, is very pervasive and it is difficult to cure nerve injury with traditional medical treatment. Neural function depends on the normal transmission of information between neurons. When an external stimulus is applied to a neuron that exceeds a threshold level, neural action potential is generated at the axon on the neuron and will be transmitted from one neuron to another [1]. The damage of nerve function is caused by the interruption of the transmission channel of action potential.

With the quick development in the field of electronic information, Microelectronic adjuvant therapy is on the rise. Professor Zhigong Wang's team at southeast university creatively put forward the idea of Microelectronic Neural Bridge. The concept is shown in figure 1. A microelectronic system is established at both ends of a damaged nerve, as an artificial electrical signal pathway replacing the original signal channel. System structure based on the above concept is displayed in figure 2.

The system is consisted of three functional circuits: detection, signal processing and regeneration. Detection circuit pre-amplifies weak upper nerve signals probed by detection electrode. Then detected signals are extracted with valid information in signal processing circuit. Finally useful signals are amplified by regeneration circuit to enough voltage amplitude so that stimulating electrode can cause axon to produce desired action potential in lower nerve [2]. In animal spinal cord nervous system, stimulating voltage range must achieve -1V~4V to drive the axon to generate action potential [3,4].
The content of this paper is about regeneration circuit in Microelectronic Neural Bridge. Block diagram is shown in figure 3. The amplitude of signals outputted by the front-end circuit is very small, generally in the tens of millivolts or so. In this paper, the input signal of the regeneration circuit is assumed to be a sinusoidal signal with frequency of 1 kHz and amplitude of 50mV.

The relevant circuit has been designed in discrete components before, with low level of integration and relatively large area [5]. In this paper, the regeneration circuit was mostly designed in TSMC 0.18μm 1P6M standard CMOS process to improve the integration and reduce the area.

2. Topological structure
In this paper, the whole system circuit is divided into two parts: 1 the on-chip op-amp, including a high gain operational amplifier and a biasing circuit module; 2 the off-chip circuit, composed of a high voltage MOSFET connected with a resistor Rd at the drain. System diagram of the circuit is shown in figure 4. Rd is the output load of the circuit, equivalent to the impedance of stimulating microelectrode. R1 and R2 are both off-chip feedback resistors, constituting an inverting amplifier. The gain is

\[ A_V = \frac{R_2}{R_1} \]  

(1)
3. Circuit implementation

In practical application, the output common mode voltage of front-end circuit will vary in a large dynamic range and therefore the input of op-amp must be able to handle the voltage ranging from rail to rail. The low temperature drift biasing circuit provides a stable bias current that does not change with temperature for the circuit, so as to improve the temperature stability of operational amplifier. The off-chip output circuit can overcome the process limitation to produce output voltage range of -1V~4V. This section will introduce the specific structure of each circuit module.

3.1 Constant-\(g_m\) rail-to-rail input op-amp

The schematic of the rail-to-rail input op-amp is shown in figure 5. NMOS differential pair and PMOS differential pair are connected in parallel as the differential input stage [6]. The drawback of complementary difference pair is that its transconductance \(g_m\) will vary with common-mode input range (CMIR). A novel structure called Max Current Selection, which is composed of transistors M7~M28, is employed in the input stage to make \(g_m\) constant [7].

3.2 Low temperature drift biasing circuit

The bandgap reference shown in figure 6 is intended to produce a stable voltage that changes very little with temperature. Figure 7 shows a v-to-i circuit which is used to convert the stable voltage into the low temperature drift current. Because the resistance also varies with temperature, two resistors R3 and R4 with inverse temperature coefficient are applied to counteract the effect of temperature. The reference voltage and biasing current can be expressed as

\[
\begin{align*}
V_{\text{REF}} &= I_{R2}R_2 + V_{\text{BE3}} = \frac{V_{\text{BE3}}}{R_1} R_2 + V_{\text{BE3}} \quad (2) \\
I_{\text{BIAS}} &= \frac{V_{\text{REF}}}{R_3 + R_4} \quad (3)
\end{align*}
\]
Figure 5. Schematic of constant-$g_m$ rail-to-rail input op-amp.

Figure 6. Schematic of bandgap reference.

Figure 7. Schematic of v-to-i circuit.

3.3 Off-chip output circuit

The maximum withstand voltage of transistors available in TSMC0.18μm process is only 3.3V. In order to achieve output voltage range of -1V~4V, an off-chip high voltage MOSFET is applied in output circuit. In this paper, MOSFET model of NX1029X_N in NXP Semiconductor Corporation is chosen to be used as the output driving transistor.

The output circuit is common source structure made of Rd and MOSFET, as shown in figure 4, with 5V positive power supply and -1.5V negative power supply. Rd is equivalent to the microelectrode impedance, which is simplified to be a 100Ω resistor.

4. Layout and simulation results

The layout of the on-chip circuit is shown in figure 8 and the die area is 300μm×300μm. The gain of inverting amplifier is set to be 100 by adjusting the ratio of feedback resistors R1 and R2 in Fig.4. For the 50 mV, 1 KHz sinusoidal input signal, the output waveform is shown in figure 9.

As is shown in figure 9, the sinusoidal signal is amplified without distortion, and the output voltage ranges from -1V to 4V. Post simulation results of the regeneration circuit are given in table 1.
5. Conclusion
An animal spinal cord neural signal regeneration circuit is presented in this paper. The simulation results suggest that the circuit can amplify the weak neural signals to enough large amplitude to drive the stimulating electrode. The circuit is expected to be used in vitro test of medical electrical experiments on animals’ spinal cord function recovery.

Acknowledgements
We are sincerely thankful for the support from the project funded by the priority academic Program Development of Jiangsu Higher Education Institutions (PAPD, No. 1104007003) and Top-Notch Academic Programs Project of Jiangsu Higher Education Institutions (TAPP, No. PPZY2015A035).

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