The role of growth temperature on the electron mobility of InAs/In$_x$Ga$_{1-x}$As selective area grown nanowires

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Semiconductor nanowire networks are essential elements for a variety of gate-tunable quantum applications. Their relevance, however, depends critically on the material quality. In this work we study selective area growth (SAG) of highly lattice-mismatched InAs/In$_x$Ga$_{1-x}$As nanowires on insulating GaAs(001) substrates and address two key challenges: crystalline quality and compositional uniformity. We introduce optimization steps and show how misfit dislocations are guided away from the InAs active region and how Ga-In intermixing is kinetically limited with growth temperature. The optimization process leads to a more than twofold increase in electron mobility and shows an advancement toward realizing high quality gatable quantum wire networks.

Considerable advances have been made in the field of hybrid quantum devices by using semiconductor nanowires grown by the vapor-liquid-solid (VLS) method or defined by gating in two-dimensional electron gases (2DEGs) [1–7]. Nevertheless, there are several applications including the study of Majorana-mode braiding, quantum interference, solid state quantum simulations, multi-terminal Josephson junctions, and superconductor-insulator transitions which demand large-scale nanowire networks [7–11]. Obtaining large-scale nanowire networks through the two aforementioned methods is challenging due to basic physical limitations. In the case of VLS networks, the length of the nanowires sets the ultimate limit to how many nanowires can be interconnected [12–13]. In 2DEGs, the number of gates needed to define the nanowires and their on-chip integration can be potentially problematic for networks with a few dozens of interconnected nanowires [6, 7].

A natural approach to surpass these limitations is to grow the nanowire networks through a mask on the substrate, which is known as selective area growth (SAG). Dimensions of SAG nanowires, their positions and relative distances are readily controlled by the design of the mask allowing for growth of arbitrary lattices [16–18]. The method is less explored, however, leaving ample room for optimization to achieve SAG nanowires and nanowire lattices comparable to VLS and 2DEGs.

Within the possible material choices for building nanowire networks, InAs stands out due to its low electron effective mass, high mobility and strong spin-orbit coupling [19]. Several studies have demonstrated successful growth of narrow band-gap InAs SAG nanowires directly on wider band-gap semiconductor substrates; e.g. InP [16, 20, 21] or GaAs [16, 21, 22]. However, transport properties of the nanowires are poor when compared to bulk InAs, in part because the nanowire/substrate interface exhibits a network of misfit dislocations owing to high lattice mismatch. Likewise, transport properties are affected by high interfacial roughness caused by thermal annealing usually performed to remove the native oxide prior to the growth [16]. Finally, material intermixing between layers is a common problem inherent to heteroepitaxial systems [23–26]. The intermixing produces nonuniform composition profiles affecting the band alignment of heterostructures and their transport properties [18, 27, 28].

In this work, we present a step-by-step optimization of InAs/InGaAs SAG nanowires grown by means of molecular beam epitaxy (MBE) on GaAs(001) substrates. The nanowire geometry was controlled by defining windows in a 10-nm silicon dioxide (SiO$_2$) mask layer. We demonstrate atomically smooth trenches after oxide removal with atomic hydrogen (a-H) as an alternative to conventional thermal annealing. We tackle the problem of misfit dislocations by introducing an In$_x$Ga$_{1-x}$As buffer layer before the InAs transport channel. Focusing on growth temperature optimization of InGaAs and InAs, we achieve transport channels with high crystalline quality and high compositional uniformity. The results are validated with the use of scanning transmission electron microscopy (STEM), electron energy loss spectroscopy (EELS) and x-ray diffraction (XRD). The efficiency of the proposed optimization steps is confirmed by the en-
hanced electron mobility of devices measured at 1.7 K.

RESULTS AND DISCUSSION

The sequence of growth steps leading to high quality InAs SAG nanowires is shown in Fig. 1. The substrate fabrication (step 0) is described in [16] and in the following we present results for growth steps 1-4. The choice of growth parameters for each step is discussed in the Supplementary Information (SI) (see Fig. S1).

Step 1. We first discuss the procedure of removing the native oxide from the bottom of GaAs trenches prior nanowire growth (step 1, Fig. 1). The standard approach for the oxide removal is thermal annealing which, however, has the unwanted side effect of also degrading the surface topology due to the temperature activated transformation of the stable Ga$_2$O$_3$ into the volatile Ga$_2$O by consumption of GaAs [29–33]. The results are 15-30 nm deep surface pits as shown in Fig. 2a,b ("step 1:T") and Fig. S2 in the SI. We found that the root-mean-square (rms) roughness of the GaAs surface in the growth windows increases from 0.31±0.11 nm after fabrication process to 3.18±0.35 nm after thermal annealing. In conventional thin film epitaxy, the surface topography after thermal annealing can be readily improved by growing thick buffer layers. In the SAG samples, however, we find that the pits underneath the oxide mask often do not get filled during growth leaving voids easily distinguished in scanning electron microscopy (SEM) (black stripes in Fig. 2a) [16, 18, 21, 34]. These voids can degrade performances of SAG-based devices and thus are unacceptable for many device applications.

As an alternative way of removing the native oxide from GaAs, we investigated the use of a-H which produces atomically smooth GaAs surfaces in thin film epitaxy owing to significantly reduced temperatures required for the Ga$_2$O$_3$ to Ga$_2$O transformation [35]. Yet, to the best of our knowledge, it has not yet been investigated for the use in SAG. As shown in Fig. 2a,b ("step 1:a-H"), exposing GaAs growth windows to 3.0×10$^{-5}$ mbar a-H at 350 °C for 15 min results in atomically smooth GaAs surfaces with 0.37±0.14 nm rms roughness without affecting the surrounding oxide mask. Our findings thus show that a-H is a great tool to smoothly remove the native oxide from substrates partially covered by oxide mask used in SAG.

Step 2. The second step in the process is the growth of a GaAs(Sb) buffer layer (Sb is used as surfactant). It was previously found that this step is essential for improving electronic transport properties of InAs/GaAs SAG nanowire devices [16]. GaAs(Sb) nanowires were grown on both thermally annealed substrates (Fig. 2c) and substrates prepared with a-H (Fig. 2d). In both cases, the nanowires grow continuously indicating that the native oxide was removed successfully. However, in the case of thermal annealing, the nanowires are surrounded by voids in the substrate as discussed above. In contrast, a-H results in a smooth oxide desorption without pits formation.

Figure 2 shows the topography across a typical nanowire grown in a 220 nm wide [1-10]-oriented growth window measured with Atomic Force Microscopy (AFM). The nanowire has a height of 30 nm above the trench and exhibits a flat top (001) facet with the rms roughness of 0.275±0.015 nm. The side facets were assigned to {113}A and {112}A crystal planes based on the slope (SI Table S1). We note that {112}A facets are energetically unfavorable for GaAs grown without any surfactants and that low-energy {111}A facets are observed instead (see comparison between GaAs and GaAs(Sb) nanowires in SI Fig. S3) [32, 36]. One possible explanation is that the facet angle is underestimated in our experiment owing to only a small fraction of the side facet being available. On the other hand, it is likely that the presence of Sb surfactant changes the surface energy densities of GaAs favoring the formation of {112}A facets [37, 38].

Step 3. We now consider the growth of In$_x$Ga$_{1-x}$As on top of GaAs(Sb). The purpose of this buffer is to reduce a 7.2% lattice mismatch between the GaAs(Sb) and the subsequent InAs transport channel. This suggests high In contents. However, at the same time, the buffer must be electrically insulting which favours a lower In fraction. It is known that Ga interdiffusion in InAs grown on GaAs complicates the attempt to form pure InAs at high growth temperatures [16, 22, 23, 39]. Thus, to control the composition of the InGaAs buffer layer, six InAs/InGaAs/GaAs(Sb) samples were grown in a temperature range from 520 °C to 540 °C (SI Fig. S4). Note that the growth temperature of the InAs layer at this
FIG. 2. (a) A set of AFM images (0.5×0.5 μm² image size) demonstrating a [1-10]-oriented GaAs growth window (trench) with a native oxide (step 0), after thermal oxide desorption (step 1: T), after atomic hydrogen oxide removal (step 1: a-H). White dashed lines indicate the position of AFM profiles shown in (b) and averaged over 15 nm. Top-view SEM images (1 μm scale bar) of GaAs(Sb) SAG nanowires grown on a GaAs(001) substrate from which the native oxide was removed either thermally (c) or with a-H (d). The insets show relative temperature T of oxide removal with respect to the GaAs(Sb) growth step with the latter being fixed at 600 °C. (e) AFM profile across a typical GaAs(Sb) SAG nanowire with step 1: a-H showing a faceted structure.

stage is fixed at 520 °C for all samples.

Figure 3a shows an STEM micrograph using the high-angle annular dark-field imaging mode (HAADF) taken across four [1-10]-oriented InAs/InGaAs/GaAs(Sb) nanowires designed for field effect (FE) transport measurements. The nanowires protrude out of the growth window with a slight lateral overgrowth on the SiO₂ mask (the layer with the darkest contrast in this imaging mode). The cross section is symmetrically formed by the (001) top facet, {111}A, {113}A and {110} side facets as can be seen in STEM images and supported by simulated atomic model in SI Fig. S5. The EELS analysis reveals the presence of the GaAs(Sb) buffer layer, followed by an InGaAs region and a thin layer of InAs channel (Fig. 3a). Generally, the GaAs(Sb) layer has a rounded shape without the clear side facets observed earlier in the reference GaAs(Sb) nanowires (Fig. 3b). Moreover, its surface in the vicinity of the substrate as well as the substrate are eroded (Fig. 3b and SI Fig. S6). The InGaAs buffer layer has a non-uniform composition: three Ga-rich regions are well distinguished at the InGaAs/GaAs(Sb) interface (visible as cyan flames in Fig. 3b). Additional EELS maps are shown in SI Fig. S7. The Ga-rich flames penetrate into the InAs channel producing local dips in the In composition profile extracted along the [-111]A nanowire facet (Fig. 3c). This suggests that there exists a constant flow of Ga which diffuses towards areas with abrupt change in composition, and thus highly strained, thereby creating diluted InGaAs alloys. The Ga is most likely supplied from the GaAs(Sb) buffer and the GaAs substrate, consistent with the observed surface erosion. Indeed, similar phenomena of diffusion and material intermixing activated at high growth temperatures in strained epitaxial systems have earlier been reported in quantum dots [23, 25, 26], free-standing axial nanowires, and in-plane nanowires grown on nanomembranes [18, 22, 29, 11]. Among possible mechanisms, bulk diffusion and surface diffusion have been suggested. In the case of Ge/Si quantum dots, it has been shown by both experiment and simulations that at standard growth temperatures the material for intermixing is provided by surface erosion of the Si substrate creating depressions around the growing system [25, 26, 42]. As the bulk diffusion of Ga is negligible at the growth temperatures used in the current work [43], we therefore conclude that the Ga is supplied from the surface of the GaAs(Sb) buffer and/or the underlying GaAs substrate similar to the Si/Ge case.

Overall, we find that the sample grown at the highest growth temperature has on average the lowest In concentration in the InGaAs buffer for both [1-10]- and [100]-oriented nanowires.

To investigate the crystal quality of the samples,
FIG. 3. The role of InGaAs growth temperature on the composition and crystal properties of the InAs/InGaAs/GaAs(Sb) SAG nanowires. (a) Low magnification HAADF-STEM image (scale bar 500 nm) of a lamella taken across [1-10]-oriented field effect nanowires grown at 522 °C. (b) In atomic distribution EELS map (relative to Ga, in percentage, scale bar 100 nm) of the nanowire from (a). Arrows indicate the place of erosion of GaAs(Sb) and GaAs. (c) Relative Ga and In atomic composition profile along the (-1-11) facet in the InAs channel from (b). (d),(e) GPA rotational maps of the nanowire from (b) representing its central part (50 nm scale bar) and the left corner (10 nm scale bar). Misfit dislocations at the InGaAs/GaAs(Sb) buffers are highlighted with black arrows. The insets show the corresponding fast Fourier transform (FFT) with the analysed planes: (111) planes correspond to the left half and (-1-11) planes to the right half of the image in (d). (f) In atomic composition variation $x$ in the In$_x$Ga$_{1-x}$As buffer layer as a function of the buffer growth temperature $T$ extracted from XRD reciprocal space maps. The composition broadening is plotted as well and is measured as $x$ FWHM. The dashed lines are linear fits and are guides to the eye.

we employ Geometric Phase Analysis (GPA) on high-resolution HAADF-STEM images. Figure 3b,e shows GPA rotational maps (planes bending with respect to the substrate). The InGaAs/GaAs(Sb) interface exhibits an array of misfit dislocations. Some part of the mismatch strain is released elastically via $\sim 2^\circ$ bending of planes close to the nanowire corners. The latter is possible owing to free side walls of SAG nanowires similar to free-standing nanowires [44]. On the other hand, the InAs/InGaAs interface, highlighted with dashed lines exhibits a high crystalline quality. Over four analyzed samples, we find only 1-2 misfit dislocations over the entire InAs/InGaAs interface. These are always found at the corners of the nanowires, between the Ga-rich flames and the InAs channel. Our findings highlight the importance of the InGaAs buffer layer introduced between the InAs channel and the GaAs substrate. It efficiently traps misfit dislocations at the InGaAs/GaAs(Sb) interface leaving the InAs channel mainly dislocation-free. This is an important step forward toward high-quality InAs SAG nanowires as compared to the existing literature [16, 21].

To corroborate on the composition differences between the samples, we use XRD. In contrast to EELS, where only local nanowire composition is measured, XRD allows to access an average In composition $x$ in an array of nanowires. In Figure 3f, $x$ is plotted as a function of growth temperature for the [1-10]-oriented nanowires (reciprocal space maps used to extract the data are shown in SI Fig. S8). The maximum value of $x=0.84$ is reached at 520 °C and it gradually decreases down to $x=0.76$ when the temperature is increased to 541 °C. A similar trend is observed for the [100]-oriented nanowires (see Fig. S9 in the SI). We also plot a composition spread within buffers extracted as full-width at half-maximum (FWHM) from XRD peaks. There is a clear tendency toward increased FWHM of $x$ at higher growth temperatures. Our results indicate that lower growth temperatures are beneficial for both higher In concentrations and composition uniformity of the InGaAs buffer layers.

**Step 4.** We now turn our attention toward InAs growth temperature optimization. For this, five samples are grown in the temperature range between 460-524 °C (see SEM images in SI Fig. S10). The InGaAs growth temperature is fixed at 520 °C for all samples.

To study compositional differences between InAs nanowire channels grown at different temperatures, we use EELS as shown in Fig. 4a and SI Fig. S11. From the EELS maps, the In composition $x$ (with respect to Ga) is extracted as a function of position $p$ across the channel as shown in Fig. 4a (see inset to Fig. 4a for definition of $p$). We note that for all samples the outermost layer ($p=0$) is pure InAs owing to surface segregation [42, 43]. However, the composition of the inner layer is significantly different. High growth temperatures result in highly nonuniform compositions, and for temperatures above 500 °C, the In concentration decreases to $\sim 83\%$ across the channel. The relatively large error bars (up to 3%) is a consequence of composition broad-
enancing along the channel as well. On the contrary, when the temperature is as low as 460 °C, the In composition remains above 97% across the entire channel and error bars decrease to ~1% demonstrating high composition homogeneity along the channel.

Based on the composition values extracted with EELS we plot the lattice mismatch $\varepsilon = \Delta d_{inGaAs}/a_{GaAs}$ assuming Vegard’s law (Fig. 4). The mismatch reaches its maximum value of $7.14\pm0.07\%$ at 460 °C corresponding to the pure InAs material. By using GPA applied on atomic resolution HAADF STEM images, we then obtain the in-plane ($\varepsilon_{xx}$) and out-of-plane ($\varepsilon_{yy}$) lattice deformations with respect to the unstrained GaAs (Fig. 4). An identical trend can be seen: $\varepsilon_{xx}$ and $\varepsilon_{yy}$ increase with the decrease in growth temperature. Note, that $\varepsilon_{xx}$ is smaller than $\varepsilon_{yy}$ suggesting that the InAs layer remains compressively strained in the plane of the interface. The latter causes the expansion of the out-of-plane lattice constant owing to the Poisson effect.[10]

We analyzed the InAs/InGaAs interfaces with GPA to look for the presence of misfit dislocations. Most notably, a high crystalline quality is observed for all samples with no obvious dependence on the growth temperature (see Table S2). Overall, the nanowires have 1-2 misfit dislocation(s) per nanowire at the InAs/InGaAs interface along the [1-10] direction. Similarly to the previous set of samples, these are always located at the nanowire corners leaving the major part of the transport channel dislocation-free.

**Electrical transport properties.** Having shown that the In content in the InGaAs buffer and the InAs active region increases by decreasing the growth temperature, we examine if it also affects the electrical properties of InAs SAG channels. Single [1-10]-oriented InAs/InGaAs/GaAs(Sb) nanowires were contacted and the field-effect mobility was extracted by fitting measured conductance versus applied top gate voltage as described in SI Table S2. Overall, the nanowires have 1-2 misfit dislocation(s) per nanowire at the InAs/InGaAs interface along the [1-10] direction. Similarly to the previous set of samples, these are always located at the nanowire corners leaving the major part of the transport channel dislocation-free.

**FIG. 4.** Influence of the growth temperature on the InAs channel composition. (a) In atomic EELS map (relative to Ga, scale bar 50 nm) of the sample with InAs channel grown at 485 °C. Inset: zoomed area of the channel indicating the procedure to obtain data points in (b). (b) In atomic composition $x$ extracted at position $p$ across the InAs channel grown at four different temperatures. For each growth temperature six data points are extracted. Each data point is taken at the position $p$ and averaged over 100 nm (see inset in (a)). The averaging gives the standard deviation as error bars. (c) An example of the out-of-plane lattice mismatch map ($\varepsilon_{yy} = \Delta d_{111}/d_{111}$) obtained with GPA (scale bar 50 nm, GaAs is the reference) for the nanowire from (a). x-axis is rotated 54.75 ° with respect to the original direction: $x' = x + 54.75^\circ$ ($x'$ is parallel to the InAs/InGaAs interface, and thus to the [112] crystallographic orientation, $y'$ is parallel to the [1-11] crystallographic orientation). (d) $\varepsilon_{yy}$ and $\varepsilon_{xx}$ as a function of the InAs growth temperature extracted from GPA. Each data point is averaged over a 50 x 10 nm² box. We also plot $\varepsilon_{m}$ calculated from EELS composition assuming Vegard’s law. In both cases, $\varepsilon$ increases with decreasing InAs growth temperature.

**FIG. 5.** The role of InGaAs and InAs growth temperature on the electrical properties of InAs/InGaAs/GaAs(Sb) nanowires. (a) A representative plot of conductance $G$ as a function of gate voltage $V_g$ from the sample grown at 529 °C InGaAs growth temperature (shown on the inset, 2 μm scale bar). Measured nanowires appear in red, contacts - in yellow, the top gate - in violet. D, G and S denote drain, gate, and source, respectively. (b) Electron mobility $\mu$ as a function of InGaAs growth temperature $T$. Idential designs where used for all growths and devices. Two nanowires per sample are measured: $S_1$ and $S_2$. Inset: Electron mobility $\mu$ as a function of InAs growth temperature $T$. Red (black) symbols correspond to the outer (inner) nanowire from (a).
cm²V⁻¹s⁻¹ at 540 °C to 11500±700 cm²V⁻¹s⁻¹ at 520 °C. The trend is independent of the position of the measured nanowire. We note that the mobility depends much less on the InAs growth temperature (inset in Fig. 3b)). For more data, see Figs. S14-15. This observation suggests that the electron transport happens through both the InAs and InGaAs layers, and since the InGaAs layer has larger volume than InAs, it is the growth parameters of InGaAs which dominate the effect on the mobility. We now speculate why the growth temperature affects the electron mobility. By changing the temperature, we alter the In concentration. The latter directly affects the electron effective mass and thus the carrier mobility [48]. Moreover, as seen in Fig. 3b the InGaAs has significant variations in the In content and exhibits large compositional broadening as estimated from XRD in Fig. 3f at high growth temperatures. The compositional variation can be regarded as impurity scattering, it is thus natural to anticipate further improvement of the crystal quality of InGaAs which dominate the effect on the mobility. The opposite holds for the InAs layers.

CONCLUSION

In conclusion, we have successfully optimized InAs/InGaAs/GaAs(Sb) SAG nanowires achieving more than a twofold improvement in their electron mobility. The carrier mobility obtained in this work is significantly higher than state-of-the-art values for InAs/GaAs and In₀.₅Ga₀.₅As/GaAs SAG nanowires [16] [18] [22], and comparable to the values measured on near surface InAs quantum wells [6]. Our results show that (i) the growth temperature optimization plays a significant role in achieving In-rich layers with high composition uniformity while (ii) an InₓGa₁₋ₓAs buffer layer improves crystal coherency of the materials. We anticipate further improvement of the crystal quality and therefore the transport properties of the structures by growing the InAs segment on the unfinished top (001) facet of the InGaAs buffer layer. The latter ensures axial growth of the segment in a region located far from the highly-strained nanowire corners. A thin barrier layer grown on top of InAs can further ameliorate the device performances [9].

ACKNOWLEDGMENTS

The project was supported by Microsoft Quantum, the European Research Council (ERC) under Grant No. 716655 (HEMs-DAM), the European Union Horizon 2020 research and innovation program under the Marie Skłodowska-Curie Grant No. 722176. The authors acknowledge Dr. Keita Ohtani for technical support and fruitful discussions. D.V.B. is grateful to Dr. Juan Carlos Estrada Saldana and Dr. Thomas Sand Jespersen for careful reading of the manuscript. The authors thank Francesco Montalenti, Marco Albani and Leo Miglio for scientific discussions. ICN2 acknowledges funding from Generalitat de Catalunya 2017 SGR 327. ICN2 is supported by the Severo Ochoa program from Spanish MINECO (Grant No. SEV-2017-0706) and is funded by the CERCA Programme/Generalitat de Catalunya. Part of the present work has been performed in the framework of Universitat Autònoma de Barcelona Materials Science PhD program. The HAADF-STEM microscopy was conducted in the Laboratorio de Microscopias Avanzadas at Instituto de Nanociencia de Aragon-Universidad de Zaragoza. M.C.S. has received funding from the European Union’s Horizon 2020 research and innovation program under the Marie Skłodowska-Curie grant agreement No 754510 (PROBIST). We acknowledge support from CSIC Research Platform on Quantum Technologies PTI-001.

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