CrossStack: A 3-D Reconfigurable RRAM Crossbar Inference Engine

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Abstract—Deep neural network inference accelerators are rapidly growing in importance as we turn to massively parallelized processing beyond GPUs and ASICs. The dominant operation in feedforward inference is the multiply-and-accumulate process, where each column in a crossbar generates the current response of a single neuron. As a result, memristor crossbar arrays parallelize inference and image processing tasks very efficiently. In this brief, we present a 3-D active memristor crossbar array ‘CrossStack’, which adopts stacked pairs of Al/TiO₂/TiO₂-x/Al devices with common middle electrodes. By designing CMOS-memristor hybrid cells used in the layout of the array, CrossStack can operate in one of two user-configurable modes as a reconfigurable inference engine: 1) expansion mode and 2) deep-net mode. In expansion mode, the resolution of the network is doubled by increasing the number of inputs for a given chip area, reducing IR drop by 22%. In deep-net mode, inference speed per-10-bit convolution is improved by 29% by simultaneously using one TiO₂/TiO₂-x layer for read processes, and the other for write processes. We experimentally verify both modes on our 10 × 10 × 2 array.

Index Terms—deep learning, in-memory computing, memristors, neural network, RRAM.

I. INTRODUCTION

Increasing the sizes of artificial neural networks (ANNs) has been the most common response to the copious amount of data being continuously generated. Where training sets are in excess of billions of inputs processed through hundreds of millions of parameters in a neural network [1], new ways to speed up the processing of all this information must be developed. Since 2012, the training runtime of neural networks has doubled every 3–4 months. It is equally important to develop hardware that is not only optimized for running very large scale networks, but is adaptable to the unceasing wave of emerging ANN topologies.

Memristors are now ubiquitous in neuromorphic computing literature due to their long retention [2]–[4], excellent scalability [5], [6], fast read and write speeds [7], [8], compatibility with CMOS technology [9]–[12], and precise weight updates [13], [14]. The development of dense integrated structures with 3-D stacked crossbar arrays enables an increase in the throughput for a given chip area, but thus far, target applications of 3-D RRAM have mostly been limited to digital memory [16]–[23].

It can be difficult for ASIC designs to keep pace with the latest developments in machine learning due to the lag time between algorithm development and the full IC design cycle. With popular machine learning methods in a rapidly evolving state, reconfigurability is of paramount importance to ensure hardware does not become obsolete the moment new network architectures and topologies are introduced. In response to this, we present a reconfigurable stacked pair of memristor crossbars dubbed ‘CrossStack’ that can be operated in one of two modes: 1) expansion mode, and 2) deep-net mode. In expansion mode, the resolution of the network is doubled by increasing the number of inputs for a given chip area, thus reducing IR drop by 22% of an equivalent array. In deep-net mode, inference speed per-10-bit convolution is improved by 29% by simultaneously using one array for read processes, and the other for write processes. This brief will demonstrate how to selectively isolate and couple the two layers using CMOS cell design. We experimentally verify this on our in-house fabricated crossbar stack, using separately controlled CMOS circuitry in the SK Hynix 180nm process.

II. MATRIX-VECTOR MULTIPLICATION

To perform analog-domain multiply-and-accumulate (MAC) using RRAM arrays, a voltage vector \( V \) is applied at the input, multiplied by a conductance matrix \( G \), to generate a current vector of \( i = V^T G \) in accordance with Ohm’s Law and Kirchhoff’s Current Law. On a pre-trained network, the conductance of each memristor is programmed prior to read-out. For further detail on MAC on a crossbar, we recommend referring to [26], [27]. In a conventional crossbar, the memristors must be programmed prior to read-out. Where the number of parameters exceed the memory resources available, RRAM cells must be reprogrammed while the data flow of the activations is stalled. CrossStack avoids possible stalling that may occur by adding the option to pipeline the read and write processes simultaneously across the two layers. How this is achieved will be described in the following section.

III. CIRCUIT OPERATION MODES

A simplified structure of CrossStack is depicted in Fig. 1(a), and the memristor-CMOS cell schematic is given in Fig. 1(b). This work presents two modes in which CrossStack may operate in. These modes are controlled by an active-high read-enable signal \( \text{RE} \).

A. Expansion Mode

Expansion mode enables access to a shared column line from memristors both above and below the wire. Vertical
stacking of memristors doubles the number of possible inputs and weights to each neuron for a given length of column wire which is illustrated in Fig. 1(a) when compared to conventional crossbars. This can be formalized by the following equation:

\[
\begin{bmatrix}
    i_1 \\
    i_2 \\
    \vdots \\
    i_m
\end{bmatrix} =
\begin{bmatrix}
    V_1^T \\
    V_2^T \\
    \vdots \\
    V_n^T
\end{bmatrix}
\begin{bmatrix}
    G_{1,1} & G_{1,2} & \cdots & G_{1,m} \\
    G_{2,1} & G_{2,2} & \cdots & G_{2,m} \\
    \vdots & \vdots & \ddots & \vdots \\
    G_{n,1} & G_{n,2} & \cdots & G_{n,m}
\end{bmatrix}
\]

where \(m\) is the number of columns in the crossbar and \(n\) is the number of rows. In expansion mode, \(n\) is double that of a 2-D array, as there are rows both above and below the shared column contributing to output current.

To activate a cell in expansion mode, the read-enable signal of all cells must be identical. The current pathway from input to output of a single cell is depicted in Fig. 1(c), and a pair of stacked cells is shown in Fig. 1(e). To generate a read-out current at each shared column, \(RE\) must be set high (in our case, \(V \geq V_{Th} = 0.4V\); described in further detail in our experimental results). If transistors \(N1\) and \(N2\) are treated as switches, then \(N2\) would be off and \(N1\) would be on. Therefore, a current pathway is formed from both upper and lower crossbar arrays to the column line. To program a memristor, \(RE\) is set low as in Fig. 1(d). This causes \(N2\) to switch on and \(N1\) off, which forms a pathway from the memristor to ground and prevents current from flowing to the shared column. Therefore, the two crossbars can be programmed independently of one another by isolating them. The transistors are sized to ensure a negligible leakage current, and to sustain a sufficiently low \(ON\) resistance in comparison to the memristance while it is operating in the linear region such that it behaves as an ideal switch.

B. Deep-net Mode

Deep-net mode ensures both pairs of arrays are isolated from one another at all times. Isolation biasing enables each layer to operate independently. The two arrays must have complementary \(RE\) signals as distinct from expansion mode, depicted in Fig. 1(f). This means that while one array generates a read-out current, the other array of memristors are being programmed (in write mode). As described above, when \(RE\) is low the cell does not contribute to read-out current and input voltage \(V\) for the write layer is applied such that the conductances written to the memristors correspond to the weights of the next hidden layer in the neural network. Once the analog output current is digitized as a voltage, the write-layer has been pre-programmed and there is no need to buffer the current or store it in memory, as is required by most other pipelines [27], [29], [30]. This process is repeated, but now the roles of the crossbars are reversed. The original read-layer is now programmed to the next hidden layer of weights, and the original write-layer generates the read-out current. Thus, read-write processes run in parallel. One layer is programmed in anticipation of the output from the other layer, which enables a novel in-situ pipeline.

In describing how to program a memristor, the key difference between expansion and deep-net modes is that in expansion, all cells are identically biased for either read or write at any given time. In deep-net mode, 50% of the cells are biased for read processes and the remaining 50% are biased for write processes, only switching once each operation is complete. The shorter read-out time is subsumed within the programming cycle, but at the expense of half the number of inputs \(n\) in (1). We quantitatively demonstrate this in our experimental results.
Fig. 2. A 10 x 10 x 2 prototype of CrossStack, with a cross-sectional view of the active layer taken using a focus ion beam analyzer.

| Symbol | Parameter | Value |
|--------|-----------|-------|
| \( R_s \) | static resistance of set; \( R_s = \frac{1}{g} \) | 100k\( \Omega \) ± 7\% |
| \( R_r \) | static resistance of reset; \( R_r = \frac{1}{g} \) | 100k\( \Omega \) ± 10\% |
| \( V_{DD} \) | supply voltage | 1.8 V |
| \( V_{read} \) | read voltage | 0.5 V |
| \( V_{write} \) | write voltage | 1.2 V |
| \( t_{read} \) | current-read out time | 10 ns |
| \( t_{write} \) | programming time | 250 ns |
| \( n \) | number of memristors | 200 |
| \( V_{th} \) | threshold voltage | [0.4 V] |
| \( P_{critical} \) | worst case power consumption | 2.9 mW |
| \( R_{wire} \) | wire resistance | 3.20 \( \Omega \)/cell |
| \( A_{cell} \) | cell area | 20 \( \mu m \times 20\mu m \) |
| \( W/L \) | transistor sizing | 450nm/180nm = 2.5 |

### IV. EXPERIMENTAL RESULTS

#### A. Crossbar Fabrication

CrossStack was constructed based on two monolithically integrated crossbar arrays with a shared central electrode which make up the column line, based on a sandwich structure of Al/TiO\(_2\)/TiO\(_2\)/Al layers. A layer of Al (200-nm-thick and 20-\( \mu m \)-wide) was deposited using photolithography on a glass wafer as the bottom electrode (irradiated using mask alignment for 100 s, subsequently developed at 23\(^\circ\)C for 120 s). Any excess Al outside of the channel region was removed via wet etching (H\(_3\)PO\(_4\) : HNO\(_3\) : CH\(_3\)COOH : H\(_2\)O = 80 ml : 5 ml : 5 ml : 10 ml) at a rate of \( \Delta d/t = 300 \text{ nm/min} \). TiO\(_2\) (5-nm-thick) and TiO\(_2\)-x (15-nm-thick) thin films were formed by atomic layer deposition and magnetron sputtering to fabricate the memristor. Another 200-nm-thick layer of Al was sputtered as the top electrode using photolithography to create a 20 \( \mu m \times 20 \mu m \) mask. After a planarization step, the top stack of active layer and metal were also deposited. Note that the polarity of the pair of active layers are mirrored, as distinguishable from [5]. This allows for identical input voltages to be applied when programming the memristors. Fig. 2 shows a working 10 x 10 x 2 prototype of CrossStack, and a cross-sectional view of the memristor taken using a focus ion beam analyzer.

#### B. Cell Test

The CMOS cell was designed in the SK Hynix 180-nm process where \( V_{DD} = 1.8 \text{ V} \), \( V_{th} = 0.4 \text{ V} \), and our parameters are summarized in Table I. We used a read voltage in the range of \{0V, 0.5V\}, a write voltage of 1.2 V, both applied at \( V_{IN} \), with measurements taken with a Micromanipulator tungsten probe tip. The pinched hysteresis loop measured with a 50Hz source is shown in Fig. 3(a).

First, we tested the circuit in expansion mode. In the critical case of a write voltage applied to all devices \( V_{write} = 1.2 \text{ V} \) and \( RE \) is set HIGH (1.8V), we show that IR drop is decreased by approximately 22% compared to a similar planar inference engine in [24]. This is shown by the slower decline of current output across columns in Fig. 3(b) for CrossStack, where the gold standard would be a perfectly straight line. Therefore, we verified that expansion mode reduces line losses for a given number of inputs due to the shorter length of column wire required. The trade-off is that column wires must handle twice the current capacity of an equivalent 2-D array. This demands wide column lines to handle such current capacity without risk of electromigration. But given that RRAM is integrated in the back end of the line, minimum thickness of higher layer routing wires may mitigate this.

Designing for deep-net mode opens up susceptibility to leakage currents through \( N_1 \) during write mode, concurrently with \( N_2 \) in read mode (see Fig. 1). The worst case leakage occurs along the shared column line, when there is a minimal read current and a maximal write current. The read array memristors will all be OFF, \( R_s = 100K\Omega \), and all write array memristors will be ON, \( R_s = 10K\Omega \). To calculate the minimum value for \( V_{read} \), we use 0.5 V as the maximum read voltage and assume an input of 7-bit resolution which requires increments of approximately 500mV/128 \( \approx 4mV \). The output current of a single cell under these conditions was measured to be 39.6 nA, which is 1% off the ideal 40 nA. The accumulated leakage current through a column of 10 memristors being programmed (\( V_{IN}=1.2V; RE=LOW \)) was negligible in our experiments, and simulated to be approximately 2.5 pA per cell (i.e., 2.5pA×10 cells = 25pA column current). This is 6.3 \times 10^{-2}% of the worst-case read-current, and so in the 180-nm process used, we are able to employ minimum transistor dimensions (\( W = 450nm, L = 180nm, W/L = 2.5 \)). Leakage from a single cell is shown as a function of a DC sweep at the input is measured in Fig. 3(c) and (d), with a Monte Carlo parametric sweep of resistance overlaid (10k\( \Omega \)±7%, Gaussian distribution across 200 trials).

Current read-out measurements taken from a transient analysis under a switching input during a read-cycle are given in Fig. 4, where current deviates by 8% from the measured value in the worst-case. This suggests that a single device should be limited to 3.5-bits. We note this is a limitation not of the CrossStack architecture, but rather of memristor variability. In the conservative case of a 1-bit cell across 10 columns, the 10ns read-out is subsumed within the 25ns programming time as opposed to being added to a separate cycle after programming. This confirms improvement in speed due to our in-situ pipelining mechanism by 29%.

### V. DISCUSSION AND CONCLUSION

With two different modes available to the user, how would you decide to use one over another? In short, deep-net is suited for tasks where speed is paramount and expansion mode is for tasks involving a large number of inputs, be it for increased
There are three primary motivations in the use of expansion mode: 1) fully-connected networks typically have a far larger number of connections than in convolutional layers. Expansion mode doubles the number of possible inputs for a fixed area which enables increases the number of possible inputs; 2) a larger number of inputs requires a larger length of column wire. By using expansion mode to double up on inputs, we reduce wire resistance to half the original amount for a given number of inputs. More inputs per unit length of wire enables our crossbar to be resilient to write failures arising from line resistance IR drops by reducing line losses by 22%. 3) The lack of reliable analog memory technology makes it hard to perform hardware multiplexing in analog, and transmitting analog values over long distances or at high speed is not efficient. Restricting each memristor to one of two conductance values (i.e., single-bit memristors) means that one would require \( \log_2(n) \) memristors for \( n \) bits of precision. For crossbars that use conductance states of memristors conservatively, digital computing is more desirable but requires more memristors in a crossbar than analog for the same precision. Expansion mode facilitates this increase in devices whilst halving crossbar area. The drawback is that a larger current must be carried through the wire with more vias.

Deep-net mode is a novel processing scheme where the two crossbar layers are isolated from one another by appropriately biasing \( \text{RE} \), in order to parallelize read and write operations. It is engaged where speed is of greater importance than precision. In the most simplistic way (ignoring max-pooling and dropout), a crossbar performs inference in the following way:

1) Write weights to memristor conductances,
2) Apply a sub-threshold read voltage,
3) Buffer or store read-out signal in memory,
4) Write the next hidden layer weights to the crossbar,
5) Repeat steps 2-5 until output is generated.

In deep-net mode, CrossStack performs steps 2 and 4 simultaneously which enables read and write operations to occur together. By the time an output is generated from step 3, it is ready to be processed by the next hidden layer in step 4 for a speed increase of 29% over an equivalent 2-D array.

The most prevailing issues in realizing large scale crossbar arrays beyond our working prototype are mismatch and endurance. At this stage, our current error rate was 8% which limits the number of bits that can be represented by a single cell. Subthreshold current was hardly an issue in our design, but Fig. 3(d) shows the nonlinearity of voltage across the memristor under high write voltages \( (V_{\text{IN}} > 3V) \), and leakages will become more prevalent at shorter channel lengths. Capacitive coupling as a result of high programming voltages into bit-lines that are reading out poses a degree of risk, but should be tolerable for higher metal layers given the wider spacing. Allowing for heat dissipation in a 3D structure is an ongoing challenge and the subject of significant process-related research, often calling for external heat sinks. In general, the advantages seem to outweigh the drawbacks and CrossStack presents a promising methodology for reconfigurable inference acceleration to adapt to the various types of ANNs being deployed.

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