LETTER

A dV/dt noise canceling circuit of capacitive-isolated gate drivers

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Abstract For capacitive-isolated gate drivers, the pulse width distortion (PWD) and common mode transient immunity (CMTI) are vital factors to evaluate its performance. In this paper, an envelope detection circuit and a dV/dt noise canceling circuit of capacitive-isolated gate drivers is designed based on X-FAB 0.35um CMOS process. With these structures, this gate driver alleviates PWD and improve CMTI. Spectre simulation results show that the gate driver achieves 200kV/µs CMTI with 50ns propagation delay and maximum 7.4ns PWD. Besides, it has better robustness to fabrication process and temperature variation than conventional methods.

Classification: Power devices and circuits

1. Introduction

Isolated gate drivers have been widely used in power electronics, including industrial electronics, automotive electronics and many other fields [1]. They can provide galvanic isolation for two circuits that have different ground references, ensuring the safety of the system and users. Signal is transmitted from low-side to high-side by coupling since there is no direct connection between those two sides. Inductively coupled isolation methods provide the isolation through on-chip micro-transformers [2, 3, 4, 5, 6, 7, 8], and capacitive-coupled isolation methods utilize on-chip SiO2 capacitor as isolation barrier [9, 10, 11, 12]. More work and research were done in these methods. For example, using inductive-coupled to get less power consumption[13], to receive high common-mode transient immunity[14], and using capacitive-coupled to build a high speed fully integrated capacitive digital isolation system[15].

We used silicon-based on-chip capacitors to implement integrated capacitive isolation. The signal is used on-off keying (OOK) modulation to transmit the digital data across the silicon dioxide based the isolation barrier, and then the high-side demodulates the signal and output through a buffer stage. Traditional demodulation method is comparing the demodulated signal with a decision threshold before output [16]. However, the drift of the signal and decision threshold caused by process and temperature can cause the pulse width distortion (PWD) or even the error output.

Besides, in order to improve the power density and reduce the size of magnetic components, the switching speed of converters or inverters continuously increases [17]. High speed switching leads to high slew rate at the floating ground as high as 200kV/µs [18], the fast slew rate of the floating ground voltage will induce dV/dt noise, leading to the incorrect transmission of signals. Therefore, the common mode transient immunity (CMTI) is a key parameter for gate drivers. Most commercial gate drivers provide CMTI from 50kV/µs up to 150kV/µs [19,20,21,22,23] and only a few can achieve higher CMTI, but with large propagation delay. Pulse filters and common-mode noise cancellation circuit are usually adopted to eliminate dV/dt noise [24,25,26,27,28]. However, they bring extra propagation delay, and are sensitive to the process mismatch and affects the reliability of the circuit.

In this paper, an envelope detection circuit is proposed, which ensures the decision threshold and the demodulated signal drift in the same direction to receive lower PWD. And a dV/dt noise canceling circuit is designed to improve the CMTI, which has a logic module to process a enable signal and latch the output to screen dV/dt noise effect. Compared to the conventional method, the proposed circuits have lower PWD, shorter delay time and higher CMTI. Besides, it is insensitive to the process and temperature variation.

2. Structure of capacitive-isolated gate drivers

Fig.1 shows the conventional structure of capacitive-isolated gate drivers based on OOK modulation. It has two drawbacks: one is PWD caused by the conventional envelope detection circuit, and the other is dV/dt noise induced by the floating ground of High-side.

In order to solve those problems, the gate driver is improved as shown in Fig.2. After the isolation capacitors, the modulated signals pass through the proposed envelope detection circuit and the noise canceling circuit, and then output through a buffer. GND1 is the ground of Low-side, and GND2 is the ground of High-side. GND1 is preset to zero and will float from zero to the bus voltage when the next stage devices (eg. SiC MOSFET, converters) work.
There are two kinds of capacitors in the barrier interface, where $C_{iso}$ is for transferring normal signals and $C_{noise}$ is for detecting $dV/dt$ noise. More details about the proposed structures will be discussed in Section 3 and Section 4.

The proposed circuit is composed of a multi-stage amplifier, two envelope detectors and a comparator. Two sets of different gate resistances in the amplifier are used to generate differential signals with magnitude. Then those two sets signals are demodulated separately by the envelope detectors to generate demodulation signals $V_1$ and $V_2$ with different amplitudes. $V_1$ can be act as the threshold voltage. Finally compare them and output $V_Y$.

In Fig.4(b), the blue dashed box shows the active conductive-load in an amplifier. Its input impedance $Z_{in}$ is expressed in Eq. (1).

$$Z_{in} = \frac{1+sR_G C_{GS} C_{DS} + s(C_{GS} + C_{DS}) + s R_m}{s^2 R_G C_{GS} C_{DS} + s(C_{GS} + C_{DS}) + s R_m}$$

For this gate driver, input signals are modulated at about 550 MHz to go through the isolation capacitors. According to Eq. (1), the active inductive-loads are utilized to realize the high gain of the amplifier at 550Mhz. Besides, in the range of -40°C to 125°C, the gain at 550MHz is set to nearly the same to ensure stable operation over this temperature range. In the last stage of the amplifier, two sets of different gate resistances $R_{G1}$ and $R_{G2}$ are used to generate
differential signals with magnitude of $V_{A+}$ and $V_{A-}$, $V_{B+}$ and $V_{B-}$. $V_B$ ($V_B = V_{B+} - V_{B-}$) can be derived in Eq. (2), where $V'_{in}$ ($V'_{in} = V'_{in+} - V'_{in-}$) is output of the front stage amplifier, and $r_{on}$ and $Z_{in}$ are shown by the blue arrows. $V_A$ ($V_A = V_{A+} - V_{A-}$) is derived in Eq. (3). In the case of high frequency, Eq. (3) can be simplified as Eq. (4).

$$V_B = g_m V'_{in} \times \frac{r_{on} Z_{in}}{r_{on} + Z_{in}}$$ (2)

$$V_A = V_B \times \frac{R_{G1} + 1}{R_{G1} + R_{GS}}$$ (3)

$$V_A = V_B \times \frac{R_{G1}}{R_{G1} + R_{G2}}$$ (4)

When the temperature changes, Eq. (3) becomes to Eq. (5) at high frequency. The $\delta_TTC$ and $\delta_TR$ is the temperature offset of capacitance and resistance. At the high frequency, $\frac{1}{s_{GDS}(1+\delta_TTC)}$ can be seen as zero, so the above equation is simplified as:

$$V_A = V_B \times \frac{R_{G1}(1+\delta_TR) + 1}{R_{G1} + R_{G2}(1+\delta_TTC)} = V_B \times \frac{R_{G1}}{R_{G1} + R_{G2}}$$ (5)

It can be seen from Eq. (5) that $V_A$ and $V_B$ are proportional to each other, and $V_B$ is greater than $V_A$. And temperature and process have little influence on Eq. 5. Even if the offset occurs, they drift in the same direction. For the envelope detector module, $V_A$ and $V_B$ are demodulated to $V_1$ and $V_2$. $V_1$ can be set to the threshold voltage $V_{th}$ by setting appropriate parameters of $R_{G1}$, $R_{G2}$, the current source and capacitor. Besides, the $R$ in this module is used to generate the difference between DC level parts of $V_1$ and $V_2$.

It can be concluded that $V_2$ is always higher than $V_1$ when the input signal of the gate driver $V_{PWM}$ is high, and $V_2$ is always lower than $V_1$ when the $V_{PWM}$ is low because if the $R$ (R is used in the envelope detector module to ensure the correct height relationship in the DC state). This relationship does not change depending on temperature and process. Therefore, this proposed circuit can always output correct height information by comparator. Besides, when $V_A$ and $V_B$ drift, their demodulation signals $V_1$ and $V_2$ move with their drift direction. That is, $V_1$ and $V_2$ drift in the same direction too. Therefore, their relative displacement is less than $V_2$’s, which makes the circuit has a lower PWD than the conventional circuit.

Compared to the conventional demodulation circuit, the proposed circuit can always output correct height information signal with lower PWD under the influence of process corners and temperatures. It has no threshold voltage generation circuit and increases only a few resistors and an envelope detector.

4. The proposed dV/dt noise canceling circuit

Fig. 5 shows how the dV/dt noise destroy capacitive-isolated gate drivers. With the devices switching on and off, the floating ground GND2 changes rapidly from zero to the bus voltage.

According to $I = C \times \frac{dV}{dt}$, displacement currents $I_1$ and $I_2$ flow to node $A$ and $B$ of low-side block. The currents will flow to the MOSFETs of low-side output buffers, and form a voltage drop on R to affect the common mode level of high-side block. The displacement currents induce glitches and the demodulator cannot properly recover PWM signal. Therefore, the clamping structures and the dV/dt noise canceling circuit are proposed to solve this problem.

4.1 Clamping structures

As shown in Fig. 6, the clamping structures are composed of diodes and capacitors.

The diodes are added to the signal transmission path for voltage clamping. $C_1$ and $C_2$ are used to shield the voltage drop on R so that Bias can remain stable. Regardless of the arrival of positive or negative dV/dt noise, the diodes on the MOSFETs will conduct the displacement current $I_1$ or $I_2$ to avoid latch-up. Blue and green lines show paths of displacement currents when ±dV/dt noise comes. The
clamping structure on the resistor R further prevents extra transient voltage drops across the resistor.

4.2 dV/dt noise detecting circuit
ENP is defined as an enable signal to detect the dV/dt noise, and the generation circuit are shown in Fig.7. During the transmission of normal signals, the low frequency signal on low-side cannot be transmitted to high-side without modulation. Therefore, the \( C_{\text{noise}} \) does not work if there are no dV/dt noise.

![Fig. 7 ENP signal generation circuit.](image)

\[ \begin{align*}
DN_1 &= \text{control a current mirror branch consisting of } M_1, M_2 \text{ and } R_1, \text{ while } DN_2 \text{ controls another current mirror branch consisting of } M_3, M_4 \text{ and } R_2. \text{ If the voltage across resistor } R \text{ is lower than the sum of the diode conduction threshold and the NMOS threshold voltage, the current mirror branch does not work, so } A \text{ and } B \text{ remain high voltage } V_{\text{DD}}. \text{ } \\
& \text{Fig.7 ENP signal generation circuit.}
\end{align*} \]

When GND drops rapidly, the dV/dt noise will form and cause a current from low-side to high-side, creating a voltage drop across R. Once this voltage drop exceeds the conduction threshold \( (R \times C_{\text{noise}} \times \text{dV/dt}) \), it will cause the current mirror branches of M1 and M2 to conduct and A\((C_{\text{MTI-}})\) is pulled down. Likewise, when GND\(_2\) rises rapidly, B\((C_{\text{MTI+}})\) will be pulled down. That is the voltage of A or B will be dropped down when the dV/dt noise comes. Therefore, with XOR operation, ENP will pull up once GND\(_2\) changes rapidly, which can detect the dV/dt noise.

Besides, a logic and latch module is designed to use RS flip-flop to lock the output, so it can shield the dV/dt noise effect. Based on Table 1, the logical relationship can be derived as Eq. (6)\( (7)\).

\[ \begin{align*}
RN &= \text{ENP} + Y \\
SN &= \text{ENP} + \bar{Y}
\end{align*} \]

Table 1 Logic truth table.

| ENP | Y | RN | SN | Q |
|-----|---|----|----|---|
| 0   | 0 | 0  | 0  | 0 |
| 0   | 1 | 1  | 1  | 1 |
| 1   | 1 | 1  | 1  | Hold |

In Table 1 and Eq. (6)\( (7)\), ENP stands for enable signal, Y is the output of the demodulator and Q is the revised output without the effect of dV/dt noise. The logic module is shown in Fig.8 (a). The buffers in the red dashed box is used to adjust the propagation delay of Y and ENP, in order to ensure that the area of the RN and SN signal are both in a high level (the latch is in a “Hold” state) is able to cover the duration of dV/dt noise.

![Fig. 8 (a) the logic module, (b) Waveforms of proper function.](image)

Fig.8 (b) shows function waveforms, when the dV/dt noise comes, ENP turns high to enable noise canceling circuit. Then RN and SN will become high to make RS latch work at hold state. Finally, the effect of dV/dt noise can be eliminated.

5. Simulation results
The proposed circuits were simulated with X-FAB 0.35μ CMOS process and PDK.

![Fig. 9 Monte Carlo simulation of PWD.](image)

Fig.9 shows results of Monte Carlo simulation with running 200 cases for the envelope detection circuit and conventional circuit. The mean value of PWD also indicate the validation of the proposed envelope detection circuit. Table II displays the PWD comparison in different operation temperatures. The threshold voltage of the conventional circuits is set to the same as the \( V_1 \) at 27℃. In the range of -40℃ to 125℃, the PWD can be reduced by the proposed circuit.
Table II. PWD at different temperature.

| Temperature | -40°C | 27°C | 125°C |
|-------------|-------|------|-------|
| The proposed circuit | 3.4ns | 1.9ns | 7.4ns |
| The conventional circuit | 4.6ns | 2.0ns | 10.2ns |

Table III. Performance summary table.

| Specification            | Our work | [29] | [30] | [31] | Unit |
|--------------------------|----------|------|------|------|------|
| Propagation Delay        | 50       | 70   | 90   | 100  | ns   |
| CMTI                     | 200      | 150  | 150  | 100  | kV/µs|
| Max PWD                  | 7.4      | 35   | 30   | /    | / ns |
| Max Data Rate            | 2        | /    | /    | /    | / Mbps|
| Operating Temperature    | -40-125  | -40-125| -40-125| -40-125 | °C   |

6. Conclusion

In this paper, an envelope detection circuit and a dV/dt noise canceling circuit of a capacitive-isolated gate driver is proposed and simulated. The simulation results which is compared to some commercial capacitive-isolated drivers are summarized in Table III.

Our driver with the proposed circuits has advantages in MOSFETs operate with the actual operating condition. The inductor L was taken to be 150µH and the bus voltage $V_{bus}$ was 1200 V. The SiC MOSFET model used for the simulation is the 1200 V/55A SCT3040KR from Rohm. The input signal is a square wave signal at 1 MHz with 50% duty cycle. The $V_{gs}$ of the power device (which is the output of the driver) is between 0 and 20V with a Miller plateau duration of approximately 55 ns; the $V_{ds}$ floats between the bus voltage 1200V and ground; the current $I_{ds}$ is successfully renewed through the inductor L.
terms of PWD, propagation delay and CMTI, and it is insensitive to process and temperature.

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