ABSTRACT

In recommendation systems, practitioners observed that increase in the number of embedding tables and their sizes often leads to significant improvement in model performances. Given this and the business importance of these models to major internet companies, embedding tables for personalization tasks have grown to terabyte scale and continue to grow at a significant rate. Meanwhile, these large-scale models are often trained with GPUs where high-performance memory is a scarce resource, thus motivating numerous work on embedding table compression during training. We propose a novel change to embedding tables using a cache memory architecture, where the majority of rows in an embedding is trained in low precision, and the most frequently or recently accessed rows cached and trained in full precision. The proposed architectural change works in conjunction with standard precision reduction and computer arithmetic techniques such as quantization and stochastic rounding. For an open source deep learning recommendation model (DLRM) running with Criteo-Kaggle dataset, we achieve $3 \times$ memory reduction with INT8 precision embedding tables and full-precision cache whose size are 5% of the embedding tables, while maintaining accuracy. For an industrial scale model and dataset, we achieve even higher $>7 \times$ memory reduction with INT4 precision and cache size 1% of embedding tables, while maintaining accuracy, and 16% end-to-end training speedup by reducing GPU-to-host data transfers.

1 INTRODUCTION

Machine learning and deep learning in particular has been tremendously successful in tackling tasks that were traditionally considered to require human intelligence or intuition. Deep learning typically accomplishes this feat with massive computations in the Euclidean space on matrices of real numbers. While inputs to many deep learning tasks are naturally represented as matrices of continuous numerical values such as image classification and detection, in the cases where input data is discrete in nature such as categorical features and vocabularies, embedding is at present the de facto technique that maps a discrete set into the continuous Euclidean space. In essence, a good embedding maps discrete entries into $\mathbb{R}^d$ in such a way that preserves natural relationship via the basic operations in Euclidean space.

Naturally, embedding table is an important component of recommendation systems that are important to internet companies (Cheng et al., 2016; Wang et al., 2017; Hazelwood et al., 2018; Naumov et al., 2019), which rely heavily on categorical features to deliver personalized contents based on user-item interactions. Such models customarily contain hundreds of embedding tables representing different users, characteristics of commercial items, news articles’ topics, and are commonly tens of gigabytes in size in commercial ML models (Hazelwood et al., 2018; Park et al., 2018).

Moreover, industry generally believes that further growing the embedding table size will improve the models’ predictive performance. However, such scaling of embeddings poses a challenge in scaling the training system’s memory and computation capacity accordingly. In GPU training systems with highly parallel execution but limited high-bandwidth memory capacity, the cost of training can be significantly increased as embeddings trend towards billions scale. Due to industry’s interest in recommendation models, accommodating the intense memory requirement of embeddings is essential in scaling high-performance training systems.

Figure 1 captures the structure of a representative Deep Learning Recommendation Model (DLRM) (Naumov et al., 2019) developed for personalization tasks. Dense and sparse features are computed via multi-layer perceptron (MLP) and embedding lookups, then joined in sparse-dense interaction and top MLP to compute the final click-through rate prediction. Large embeddings are partitioned across multiple GPUs following model-parallelism with no replication across device. This paper focuses on training large embeddings with reduced memory footprint while maintaining accuracy. Training acceleration via dense computation optimization is not the main subject of this study.
In this work, we propose to train embeddings in low precision with the addition of a small full-precision cache for the most recently or frequently accessed rows. Depending on the specific cache replacement policy in play, some embedding rows may behave as if they were trained in full precision most or even all of the time. Previous work (Zhang et al., 2018) shows that we can train embeddings in FP16 with stochastic rounding while maintaining neutral accuracy. We show that with a small high-precision cache, we can train embeddings with INT8 and INT4 precision, further narrowing the bitwidths and thus the memory consumption at little to no cost of accuracy. While caching is commonly adopted in GPU training systems to utilize CPU host memory (Zhao et al., 2020), we reuse the same architecture with mixed-precision to achieve the purpose of reduced memory footprint for embeddings and maintain a neutral training accuracy.

Specifically, this paper makes the following contributions:

- We propose mixed-precision embedding training with a full-precision cache, and show its effectiveness and generality in reducing embeddings memory (3× memory reduction on an open source DLRM model and 7× memory reduction on an industrial scale model) usage during training and maintaining model accuracy.

- We compare different cache replacement policies: least recently used (LRU), least frequently used (LFU), and the effect of cache associativity on model accuracy and cache hit rate.

- We explore the effect of varying cache sizes on model accuracy with embeddings trained in low precision. While model accuracy improves with large cache sizes, there is diminishing return in accuracy recovery with increasingly large cache size.

- We study the effect of rounding modes on model accuracy with and without cache, and show that stochastic rounding consistently outperforms round-to-nearest in low-precision embedding training by getting rid of systematic rounding bias.

- We achieve 16% end-to-end training speed improvement on an industrial scale recommendation system using our optimized full-precision cache implementation. With 95% cache hit rate, the embedding lookup throughput is improved by 25.8× over that of unified memory.

The rest of the paper is organized as follows. Section 2 reviews prior work on embedding table compression techniques. Section 3 explains our approach and different cache replacement policies. Section 4 discusses the experiments and results with CPU emulation and open source DLRM model. The results support our focus on an associative cache GPU implementation described in Section 5. The GPU implementation enables us to experiment with large-scale data set that would otherwise be prohibitive on GPU. Section 6 recaps our result and discusses future work.

2 RELATED WORKS

A sample of works showing embedding in action are (Mikolov et al., 2013; Pennington et al., 2014; Liu et al., 2015; Peters et al., 2018; Liu et al., 2019) for natural language processing, (Vasileva et al., 2018; Barz & Denzler, 2019) for computer vision, and other areas such as knowledge representation and biology (Wu et al., 2018a; Chiu et al., 2016).

We follow the conceptual classification termed in (Ginart et al., 2019) of algorithmic and architectural compression of embedding tables. Some compression algorithms apply post processing methods on the embedding tables such as low-rank SVD and other factorizations (Bhavana et al., 2019; Andrews, 2015), sparsification (Sattigeri & Thiagarajan; Sun et al., 2016) and quantization (Guan et al., 2019). Other compression algorithms aim at arriving at easily compressible tables through training. These include quantization or compression-aware training (Alvarez & Salzmann, 2017; Park et al., 2018; Naumov et al., 2018; Elthakeb et al., 2019) and gradual pruning (Frankle & Carbin, 2018). These techniques reduce the memory requirement at inference time but use the uncompressed embedding tables during training.

Alternatively, compressed architectures use alternative representation in the ML model architecture of the embedding tables other than the standard 2D-array of FP32 floating-point numbers. Hence memory saving is realized even during training. Along this line, representing the tables in low-precision data type is a natural strategy. Works along this line mainly need to maintain the models’ accuracy despite the models’ parameters have reduced precision. Notable
works using this approach include (Gupta et al., 2015; Chen et al., 2017; De Sa et al., 2018; Wu et al., 2018b; Zhang et al., 2018; Kalamkar et al., 2019). We note that some of the just referenced works try to reduce the memory footprint of weight parameters so as to improve compute performance and not that of embedding table size. Some other works explore more structural changes to the embedding table such as tensor train representation (Khrulkov et al., 2019), mixed-dimension factorization (Ginart et al., 2019) or vector quantization (Fan et al., 2020).

Instead of using algebraic factorization, we use memory hierarchy and varying precision to enable compression. Like the other compression architecture work, the compression benefits training as well as inference. The sequel of this paper explains our design and reports the results on extensive experiments with our CPU and GPU implementations running different models on multiple data sets with different cache size/precision/policy combinations.

3 Mixed-Precision Embedding Table with a Cache

A common embedding table $T$ consists of $N$ rows of $d$-dimensional vectors of FP32 numbers. Each row corresponds to some categorical features, for example a particular user, and any production grade ML model such as a recommendation system can consist of hundreds of such tables. Expanding the capacity of embedding tables – by increasing the total number of tables or dimensions of individual ones – can increase model performance, motivating active research in embedding table compression that does not sacrifice the tables’ representation capacities.

To explain our compression method of mixed-precision with a cache, it suffices to consider the workflow involving a single row of one table $T$ during a training iteration. During a forward pass, a particular index-$i$ row $x$ of $T$ is needed and obtained by a fetch operator $x \leftarrow \text{fetch}(T, i)$. This row will participate in the model evaluation as input to some layers and eventually contribute to the loss function $L$. During the corresponding backward pass, the gradient of $L$ with respect to $x$, $\frac{\partial L}{\partial x}$, is computed and $x$ updated via $x \leftarrow x - \eta \frac{\partial L}{\partial x}$ for example with a simple SGD algorithm with learning rate $\eta$. This update to the embedding table is denoted as $\text{update}(T, i, x)$.

Our method has two main components. The first is the use of a reduced-precision embedding table similar to (Zhang et al., 2018). Table $T$ is in a precision lower than FP32. During a forward pass, the $\text{fetch}$ operator $x \leftarrow \text{fetch}(T, i)$ up-converts the row in its low-precision representation to FP32. Computations are carried out in FP32 including the computation $x \leftarrow x - \eta \frac{\partial L}{\partial x}$. The update step $\text{update}(T, i, x)$ uses either a round-to-nearest or stochastic rounding (Zhang et al., 2018) approach to down convert $x$ into the precision of $T$’s entries. (Zhang et al., 2018) applies this approach to an FP16 embedding table $T$ and uses stochastic rounding to store the updated row back into $T$.

Our second component augments the low-precision embedding table $T$ with a cache $C$ of FP32 entries. $C$ only has $n$ rows, which is a fraction of $T$’s row dimension $N$. Similar to cache memory architecture, an embedding row may be residing both in the cache $C$ and the table $T$, albeit with different precision. We use and preserve the high precision version whenever possible.

Combining these two components, the method is encapsulated by the $\text{fetch}$ and $\text{update}$ operators as $x \leftarrow \text{fetch}(T, C, i)$ and $\text{update}(T, C, i, x)$. The operator $\text{fetch}$ returns the higher-precision version if the row $i$ resides in cache, or return the up converted result of the lower-precision version in $T$. In updating the table and cache with the updated row $x$, the $\text{update}$ operator checks that if this row is cache resident, simply replaces the row in cache with the updated $x$. Otherwise, one of two scenarios happen that is determined by the cache policy in effect. Either $x$ does not have priority to evict the current cache content whose space it conflicts with, or that it does. In the former, $x$ is placed in the cache verbatim while the evicted row is placed in the table $T$ after being down converted. In the latter, one simply down converts $x$ and places it in $T$.

Our design allows four knobs as follows.

- **Precision:** The embedding table $T$ contains entries in precision lower than FP32. We allow the IEEE 16-bit floating-point values FP16 as well as quantization into INT8, INT4, as well as INT2 precision. For integer quantization, each row of the embedding values share one pair of quantization parameters $(s, b)$, scale and bias, represented in FP32. We use row-wise uniform min-max quantization in mapping real values to unsigned quantization domain:

$$x_{\text{quantize}} = \frac{x - b}{s}$$

where $b=\min(x)$ and $s=(\max(x)-\min(x))/(2^N - 1)$. The quantization parameters are chosen so that the quantized embedding values will be in the corresponding range of the unsigned integer datatype: $[0,3]$ for INT8, $[0,15]$ and $[0,255]$ for INT2, INT4 and INT8 quantization, respectively.

- **Rounding:** When a FP32 value has to be placed into a low-precision embedding table, a precision down conversion occurs. Let $x$ be the FP32 value in question. There is a pair of neighboring numbers $(x_-, x_+)$ in the quantized low-precision domain such that $x_- \leq x \leq x_+$ (that is, they differ by one “unit in
Cache Replacement Policy: When we attempt to place a non-cache resident row of index \(i\) into the cache and the set \(h(i)\) is already fully occupied, the replacement policy dictates the appropriate action. We maintain a priority value of each row which can be either access frequency or timestamp of last access, depending on the replacement policy. We also keep track of the lowest priority value of the current cache residents for each set \(s\), \(0 \leq s < n\). When the FP32 Row-\(i\) is to be stored, our policy puts the row in the full-precision cache if and only if its priority value is higher than the lowest priority value of the residents. In this case, the lowest priority row in the cache will be evicted – down converted by a rounding method of choice and placed back into the table \(T\). Otherwise, Row-\(i\) bypasses the cache, and after it is updated in FP32, is put into \(T\) with down conversion. We have two specific policies specified by their respective priority value calculations.

1. Least Frequently Used (LFU). Each embedding row carries with it an access count as the priority value. Access count is a popularity measure; LFU policy naturally let the more popular rows maintain higher precision based on the assumption that the more frequently used rows pull heavier weight on model accuracy. One drawback of this policy is that access count requires extra memory per row, whose size grows linearly with the number of rows in embeddings.

2. Least Recently Used (LRU). Each cached row carries the last access timestamp as the priority value. This policy lets those rows that are often accessed within a time window to maintain higher precision in that duration. Another advantage over LFU is that this priority value needs not be explicitly maintained at all in the case of a direct mapped cache, as the cache resident entry is always evicted in case of a conflict.

We will report on our experiments and results in the next sections.

4 CPU Experiments with DLRM and Kaggle Dataset

We use a CPU emulation to explore our algorithm design space with an open source model and dataset. Section 5 will discuss an implementation in a GPU training system and performance evaluation with an industrial-scale internal model and dataset. The main emulation aspect here is that we do not keep two physical spaces for the embedding table and the cache, but rather use a single FP32 array to emulate a single low-precision table with FP32 cache. We use the simple technique of fake quantization, detailed below, to maintain faithful behavior of low-precision numerics and experimented with all combinations of the four precisions and two rounding methods (discussed in section 3) on each of the following cache settings: direct-mapped cache with LFU and LRU policies and set associative LFU cache with associativity \(\alpha = 2^k\), \(1 \leq k \leq 5\).

4.1 Low-Precision Emulation

We implemented a custom sparse AdaGrad optimizer that uses one high-precision tensor to store the embedding weights, and keep a list of row indices of the current cache residents. All embedding gradient updates are applied in full precision. When Row-\(i\) in table \(T\) is supposed to be stored in low precision, we apply fake quantization (quantization followed by dequantization) to row \(T[i, ;]\) to provide a numerically faithful emulation: In the case of FP16, fake quantization of a FP32 value \(x\) is simply the operation

\[
\text{FP16}_\text{to FP32} (\text{FP32}_\text{to FP16}(x))
\]

With the above conversion, while the result physically remains in FP32, its precision is that of FP16. Fake integer quantization of an FP32 value \(x\) similarly returns an FP32 object but whose precision is the same as if integer quantization was performed. Algorithm 1 shows the fake quantization details.

4.2 Cache Implementations

Numerical faithfulness is paramount in our study; thus we show the exact numerical steps on our single-array emulation of an embedding table and its cache. Here we have a
We use Deep Learning Recommendation Model (DLRM) (Naumov et al., 2019) with Criteo-Kaggle 7D Ads Display Challenge dataset¹ (Criteo AI Lab, 2014) for model accuracy evaluations with different low-precision and cache implementations. The accuracy metric is based on the relative change to the test accuracy of the resulting low-precision models using the full FP32 model as reference. The precise definition of our metric is

\[
\text{Accuracy Drop} = \frac{\text{Acc}_{\text{FP32}} - \text{Acc}_{\text{lowprec}}}{\text{Acc}_{\text{FP32}}} \cdot 100 \quad (1)
\]

In particular, if the low-precision model in fact has higher test accuracy, our metric becomes negative. Our goal is to keep this number below roughly 0.02%.

Our benchmark model has 26 embedding tables with the following sizes shown in Table 1. We configure all 26 embedding tables to use row dimension 128 (total 4.3B parameters), and only apply low-precision with or without caching technique to tables with more than 1K rows for all experiments. Embedding tables with less than 1K rows are trained in FP32.

| Table 1. DLRM benchmark model embedding sizes |
|-----------------------------------------------|
| 4 | 4 | 11 | 16 |
| 18 | 24 | 28 | 105 |
| 306 | 584 | 634 | 1,461 |
| 2,173 | 3,195 | 5,653 | 5,684 |
| 12,518 | 14,993 | 93,146 | 142,572 |
| 286,181 | 2,202,608 | 5,461,306 | 7,046,547 |
| 8,351,593 | 10,131,227 |

4.3.1 Accuracy Recovery with High-precision Cache

We first evaluate accuracy loss of training with low-precision embeddings without a high-precision cache. Table 2 shows the relative test accuracy drop of training embeddings in various low precisions with nearest and stochastic rounding. We observe that neutral accuracy can be achieved with FP16 with stochastic rounding without high-precision caching; but accuracy decreases significantly with progressively narrower bitwidth. The accuracy boost from stochastic rounding is consistent with previous work on low-precision embedding training (Zhang et al., 2018), but not nearly enough for embedding tables represented by 8 or fewer bits. This loss of accuracy was part of the motivation for our high-precision cache.

| Table 2. Test Accuracy Drop without Cache in % |
|-----------------------------------------------|
| FP16 | INT8 | INT4 | INT2 |
| NEAREST | 0.047 | 0.549 | 1.080 | 1.454 |
| STOCHASTIC | **-0.010** | 0.077 | 0.591 | 1.037 |

¹http://labs.criteo.com/2014/02/kaggle-display-advertising-challenge-dataset/
We experiment with direct-mapped high-precision LFU, LRU cache, and set associative LFU cache with varying sizes: 5%, 10%, 30%, and 50% (of the original FP32 table) on top of low-precision tables with nearest/stochastic rounding. 32-Way LFU gives the best accuracy results and as shown in Table 3: we achieve neutral accuracy with INT8, INT4, and INT2 embeddings (with stochastic rounding) at cache sizes of 5%, 30%, and 50%, respectively.

Tables 3, 4, and 5 show that the presence of a high-precision cache with as low as 5% capacity of the original table size, regardless of cache replacement policy, recovers accuracy significantly for various lower precision levels with either nearest or stochastic rounding. With 5% high-precision cache, we recover 70-80% of accuracy drop from low-precision embeddings for 8 bits and lower.

Although larger cache sizes recover more accuracy in Tables 4 and 5, we observe a diminishing return of value in their continued increase. Plotting in Figure 2 the 16 columns of data in Tables 4 and 5 demonstrate the trend.

### 4.3.2 Replacement policy

The previous section shows that the presence of a high-precision cache recovers significantly the accuracy lost due to embeddings trained exclusively in low precisions. When an FP32 cache is present, rows updated while in cache are computed in full FP32 precision. Thus any cache policy that promotes more updates to cache residents improve accuracy. This motivates us to examine the comparative number of updates each row receives during training.

We collected access counts for each row, and plotted cumulative distribution of row counters sorted in descending order. Figure 3 shows four of the representative distribution plots out of 15 embeddings with more than 1K rows. For Criteo-Kaggle dataset, all large embedding tables share the property that a small fraction (< 20%) of rows are responsible for a large fraction (> 80%) of total accesses; some embedding tables show an even greater skew.

We now consider the relative merits of different cache re-

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**Table 3.** High-precision 32-Way LFU cache with varying cache sizes recover accuracy of low-precision embedding tables

| Cache Size | FP16 | INT8 | INT4 | INT2 |
|------------|------|------|------|------|
| % of Table | Rounding | Nearest/Stochastic |
| 5%         | 0.004/-0.005 | 0.013/-0.010 | 0.332/0.325 | 0.602/0.872 |
| 10%        | 0.003/0.004  | 0.144/0.008  | 0.430/0.212 | 0.761/0.336 |
| 30%        | 0.004/-0.008 | 0.093/0.006  | 0.321/0.164 | 0.582/0.245 |
| 50%        | 0.006/0.016  | 0.043/-0.004 | 0.246/0.143 | 0.462/0.352 |

**Table 4.** High-precision LRU cache with varying cache sizes recover accuracy of low-precision embedding tables

| Cache Size | FP16 | INT8 | INT4 | INT2 |
|------------|------|------|------|------|
| % of Table | Cache: LRU, Direct Mapped | Rounding | Nearest/Stochastic |
| 5%         | 0.004/-0.005 | 0.013/-0.010 | 0.332/0.325 | 0.602/0.872 |
| 10%        | 0.003/0.004  | 0.144/0.008  | 0.430/0.212 | 0.761/0.336 |
| 30%        | 0.004/-0.008 | 0.093/0.006  | 0.321/0.164 | 0.582/0.245 |
| 50%        | 0.006/0.016  | 0.043/-0.004 | 0.246/0.143 | 0.462/0.352 |

**Table 5.** High-precision LFU cache with varying cache sizes recover accuracy of low-precision embedding tables

| Cache Size | FP16 | INT8 | INT4 | INT2 |
|------------|------|------|------|------|
| % of Table | Cache: LFU, Direct Mapped | Rounding | Nearest/Stochastic |
| 5%         | -0.006/-0.001 | 0.087/0.014 | 0.335/0.147 | 0.533/0.423 |
| 10%        | -0.011/-0.003 | 0.063/0.008 | 0.270/0.138 | 0.430/0.375 |
| 30%        | -0.004/-0.003 | 0.044/0.009 | 0.175/0.090 | 0.280/0.243 |
| 50%        | -0.018/-0.008 | 0.014/0.008 | 0.136/0.056 | 0.217/0.193 |

**Figure 2.** Diminishing return of accuracy recovered vs. cache sizes

**Figure 3.** CDF of sorted row access counts vs. fraction of rows
replacement policies in light of the inequalities in access frequency. If the access pattern that produces these access count is non-stationary (Agarwal et al., 1989) and highly phased, a direct-mapped LRU cache can be effective in promoting cache hit rate. An advantage is that direct-mapped LRU is the easiest to implement among all the choices in Algorithm 2. On the other hand, if the access pattern is stationary, then the relative priority rankings among the rows based on access counts will more or less stabilize after some initial stages of training. Consequently, an LFU policy in general promotes the highly accessed rows be cache resident, increasing the number of cache hit. Along this line, an associative cache, with LFU policy in our case, is well known to improve cache hit rate further.

Table 6 reports the cache hit rate statistics of various cache configurations. 32-way LFU provides noticeable increase in hit rate than direct-mapped LFU, while direct-mapped LFU has higher hit rates than direct-mapped LRU. These statistics are consistent with the hypothesis that the current model’s embedding access pattern is somewhat stationary on the data set in question, making LFU and in particular with set-associative highly effective. The resulting model accuracy is well correlated positively with hit rate, as shown in Figures 4 and 5. Figure 4 shows that LFU outperforms LRU when both are direct mapped; Figure 5 shows the superiority of set-associative LFU. That said, Figure 6 shows that accuracy gain from increased set associativity plateaus after a while, succumbing to the law of diminishing return.

4.3.3 Results Summary

We summarize our CPU experiments with DLRM and Criteo-Kaggle dataset. Most importantly, the use of a low-precision embedding table in conjunction with a high-precision cache is effective for maintaining accuracy as we have demonstrated. Stochastic rounding helps maintain training accuracy on low-precision embedding tables. We also see that set associative cache architecture is preferable to direct mapped, and that the LFU replacement policy serves this model/dataset better than LRU.

Concentrating then on a 32-way associative LFU cache with stochastic rounding, Figure 7 plots the best accuracy obtained at each memory compression factor with or without a high-precision cache. Memory compression factor with non-cached low-precision embedding is calculated from bitwidths, taking into quantization parameter storage overhead, i.e., compression for FP16 and INT8 is 0.5 and 0.265, respectively. Compression factor with cached implementation is calculated from bitwidths and cache sizes, taking into account quantization parameter storage overhead and caching overhead such as access counters and tags: i.e., for INT8 embedding with 10% high-precision LFU cache, its memory compression factor is 0.374, or a $2.7\times$ memory compression. Please refer to Appendix A for more details for computing the memory compression factor.

Model accuracy degrades with increasingly large compression factors introduced by low-precision embeddings regardless of the presence of a high-precision cache. However with

### Table 6. Cache hit rates for varying replacement policies and sizes (relative to embedding tables)

| CACHE SIZE | LRU    | LFU    | 32-WAY LFU |
|------------|--------|--------|------------|
| 5%         | 68.22% | 75.65% | 77.66%     |
| 10%        | 75.18% | 81.21% | 83.63%     |
| 30%        | 85.66% | 89.07% | 92.45%     |
| 50%        | 90.12% | 92.43% | 96.13%     |

![Figure 4. Direct-mapped LFU vs. LRU](image)

![Figure 5. 32-Way Associative LFU vs. Direct-mapped LFU vs. LRU](image)
INT2 Stochastic
INT4 Stochastic
30
INT2 Stochastic
25
30
25
15
15
20
20
15
30
25
15
20
INT2 Stochastic
INT4 Stochastic
10
INT4 Stochastic
30
20
10
25

Figure 6. Diminishing return with associativity for set associative LFU cache

Figure 7. Accuracy vs. memory compression factor with and without high-precision cache on Criteo-Kaggle dataset. Please refer to Figure 10 in Appendix A for the complete figure.

5.1 Implementations
We made the following changes to fully utilize the GPU architecture.

- **32-way only**: We implemented 32-way set-associative cache for: 1) our CPU results showed accuracy improvements over direct-mapped cache and 2) it matches well with the GPU’s warp size of 32, hence achieving training speed similar to that of the direct-mapped case.

- **De-duplicate gradients**: Unlike the Kaggle dataset used for CPU evaluation with one-hot embedding accesses, the large dataset used for GPU evaluation has multi-hot embedding accesses. Therefore, there is a higher chance that multiple examples in a mini-batch access the same rows during sparse optimizer, leading to concurrent update races especially in GPUs with highly parallel execution that typically requires a large batch size. We avoid such races by sorting row indices in each mini-batch and merging gradient updates for the same rows into one update. Suppose one input in the mini-batch accesses rows 1 and 2 with gradient $g_1$, and another input accesses rows 2 and 3 with gradient $g_2$. We sort by the rows, de-duplicate gradients (e.g., $g_1 + g_2$ for row 2), and then apply the dedup’ed gradients.

5.2 Experiments and Results
To validate the feasibility of a high-precision cache on a larger model with larger dataset, we evaluate an industrial scale DLRM-like recommendation model for one ranking application at [institution name removed for double-blind review] on an internal training dataset. The size of the model and dataset are more than $10\times$ bigger than the DLRM model and Kaggle dataset evaluated in the previous section, respectively. Model accuracy is measured by Normalized-Entropy (NE) (He et al., 2014) metric. Lower NE corresponds to higher prediction accuracy for a recommendation model. Similar to the DLRM evaluation on CPUs, we adopt relative accuracy drop in Equation 1, with the goal to keep the threshold below 0.02%.

5.2.1 Accuracy evaluation
Table 7 shows the accuracy drop without cache. Similar to the CPU experiments, FP16 can achieve neutral accuracy. However, accuracy drops more steeply with narrower bit-width of INT8/4/2, and doesn’t even converge without stochastic rounding.

Then, we apply the 32-way high-precision LFU and LRU
Table 7. Accuracy Drop without Cache in %. Note that "N/A" denotes the training cannot converge, resulting not a number (NaN) accuracy.

| Cache Size | Accuracy Drop in % |
|------------|-------------------|
| Table | FP16 | INT8 | INT4 | INT2 |
| nearest | 0.001 | N/A | N/A | N/A |
| stochastic | -0.023 | 4.254 | 5.200 | 4.673 |

Table 8. High-precision LRU cache with varying cache sizes recover accuracy of low-precision embedding tables.

| Cache Size | Accuracy Drop in % |
|------------|-------------------|
| Table | FP16 | INT8 | INT4 | INT2 |
| nearest | 0.000 | 0.005 | 0.002 | 0.002 |
| stochastic | -0.022 | 0.032 | 0.010 | 0.005 |
| 0.1% | -0.016 | -0.024 | -0.002 | -0.001 |
| 1% | 0.002 | 0.003 | 0.002 | 0.001 |
| 10% | -0.000 | -0.030 | -0.014 | -0.021 |

Table 9. High-precision LFU cache with varying cache sizes recover accuracy of low-precision embedding tables.

| Cache Size | Accuracy Drop in % |
|------------|-------------------|
| Table | FP16 | INT8 | INT4 | INT2 |
| nearest | 0.002 | 0.003 | 0.001 | 0.001 |
| stochastic | -0.030 | 0.024 | 0.025 | 0.028 |
| 0.1% | 0.002 | 0.003 | 0.002 | 0.001 |
| 1% | 0.011 | 0.022 | 0.030 | 0.031 |
| 10% | 0.007 | 0.017 | 0.003 | 0.011 |

Cache with different sizes: 0.1%, 1%, and 10% of the original table size, for large embedding tables that collectively account for more than 97% of the total model size. Tables 8 and 9 demonstrate that on the large training dataset, both LFU and LRU can achieve better accuracy for various precisions with nearest/stochastic rounding. Unlike the results with DLRM and Kaggle dataset, LRU performs generally better than LFU. This will be explained in the next section.

5.2.2 Cache hit rate analysis

To understand the data reuse pattern of the large training dataset, we collected the cache hit rate statistics for different cache sizes and replacement policies (Table 10). Contrary to the Criteo-Kaggle 7D Ads display challenge dataset, when we apply caching to 5% of tables that account for 97% of total model size, LRU performs consistently better than LFU for the internal training dataset, especially for smaller cache sizes. However, if we apply caching to more tables, LFU performs better than LRU. One reason for this difference is the “data shift” pattern in the internal dataset for a few large tables, where some entity ids are popular for a continued period of time exhibiting temporal locality but later don’t appear as frequently.

Table 10. Cache hit rates for varying replacement policies and sizes (relative to embedding tables). Caching is applied to two sets of tables. The first set is 5% of embedding tables accounting for 97.1% of total model size.

| Cache Size | 5% of Tables | 55% of Tables |
|------------|--------------|--------------|
| Table | FP16 | INT8 | INT4 | INT2 |
| nearest | 0.001 | N/A | N/A | N/A |
| stochastic | -0.023 | 4.254 | 5.200 | 4.673 |

5.2.3 Memory Reduction

Similar to the analysis in Section 4.3.3, we calculate the memory compression factor for both non-cached and cached implementations of low-precision embeddings on GPUs, taking into account quantization parameter storage overhead and cache-specific access counters as well as tags. For example, the memory compression factor for INT8 embedding with 1% high-precision LRU cache is 0.259. Note that LFU takes a bit more storage than LRU implementations since LFU needs to maintain the extra counters to record the frequency.

Figure 8 shows the correspondences between accuracy and memory compression factor with and without high-precision cache for large training dataset.

For example, with the accuracy drop threshold 0.02%, we can use INT4 stochastic rounding embedding with 1% high-precision cache with 86.6% memory savings on GPUs (more than 7× memory reduction), which significantly mitigates the limited on-device high-bandwidth memory (HBM) capacity of GPUs.
5.2.4 Speed improvement

When embedding tables are too big to fit on-device HBM memory of GPUs, one should use mechanisms like unified memory (UVM, (NVIDIA, 2020). However, UVM operates in a granularity considerably bigger than embedding table rows with non-contiguous access pattern, significantly wasting PCIe bandwidth. By using low-precision embedding tables with high-precision cache, we can either (1) reduce the size of cache plus embedding table small enough to fit the both entirely within device memory, or (2) still put the low-precision embedding table in the unified memory but reducing PCIe traffic.

We want to make sure that our GPU cache implementation is fast enough to outperform UVM when cache hit rate is low, and saturates a large fraction of peak device memory bandwidth when hit rate is high. This is demonstrated by Figure 9.

Figure 9 shows micro-benchmark results evaluated on a Nvidia V100 GPU, where a large low-precision embedding table is allocated on the unified memory (UVM) and a high-precision cache is allocated on the device memory. We plot the effective bandwidth (in GB/s) in correspondence to different cache hit rate for LRU cache during the forward and backward passes. The top and bottom lines show the achieved bandwidth of the forward/backward path on the device memory and on the unified memory, which correspond to the upper and lower bound of the bandwidth. Note that the bandwidth of the device memory is bounded by the HBM peak bandwidth (900 GB/s), while the bandwidth of the unified memory is bounded by the PCIe bandwidth. When the hit rate is high, we get close to the device bandwidth. For lower hit rate, the LRU/LFU implementation is still reasonably faster than the bandwidth achieved by unified memory.

We also measure an end-to-end training speedup of 16% using FP16 LRU cache (cache size is 1% of embedding tables) over the baseline where UVM is used for large embedding tables. This is an example that our technique not only saves memory but can also improve the training speed.

6 Conclusions and Future Work

In this paper we presented low-precision embedding table with a high-precision cache as an effective memory saving technique for training large-scale recommendation models, particularly well suited for systems with high compute bandwidth but limited capacity memory like GPUs. To the best of our knowledge, this is the first time mixed-precision training with a high-precision cache is applied on an industrial-scale recommendation system. Our best results include reducing memory by over $7 \times$ for a large embedding trained in INT4 precision while maintaining neutral accuracy.

As part of future work, we will further experiment with heterogeneous precision and replacement policy assignment for different embeddings. We will potentially assign different precision and cache policy for each embedding based on a light-weight profile in the first few training iterations for the best accuracy. This can be useful to handle dataset with different characteristics as we have seen from the Kaggle and our internal dataset. We will further explore different hash functions and replacement heuristics, and evaluate their impact on model accuracy and performance. Our technique can be applied to other models with embeddings such as language models. Once proven to work for a wider range of models, it can be interesting to add hardware support by augmenting low-precision conversion to the existing hardware cache mechanisms.
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A APPENDIX: MEMORY COMPRESSION FACTOR

Memory compression factor is used to characterize the compressed model size after applying the low-precision embedding table with a high-precision cache. We need to consider the following dominant components:

- Low-precision table size, $M_{T_{\text{lowprec}}}$;
- Quantization parameter storage size, $M_Q$;
- High-precision cache size, $M_C$;
- Cache tags size, $M_{\text{tags}}$;
- Access counters (if using LFU), $M_{\text{cnt}}$;
- Original FP32 embedding table size, $M_{T_{FP32}}$

Specifically, the “memory compression factor” is calculated as

$$\frac{(M_{T_{\text{lowprec}}} + M_C + M_{\text{tags}} + M_{\text{cnt}})}{M_{T_{FP32}}}$$

Specifically, the “memory compression factor” is calculated as

$$\frac{(M_{T_{\text{lowprec}}} + M_C + M_{\text{tags}} + M_{\text{cnt}})}{M_{T_{FP32}}}$$

where:

- Cache tags are INT32 numbers, one per each row in cache;
- Access counters are INT32 numbers, one per each row of the embedding.

Assume the number of embedding rows is $E$, the embedding dimension is $D$, and the low-precision bitwidth is $\text{bitwidth}$, then the low-precision table size is calculated as:

$$M_{T_{\text{lowprec}}} = E \times (\text{bitwidth} \times D + 64),$$

where $64$ is the per-row overhead of quantization parameters (in FP32): 32 bits for the per-row scale and 32 bits for the per-row bias.

Table 11 shows memory compression factors calculated for a sample of precision and cache size combinations using a LFU cache, and the embedding dimension $D = 128$ (used in CPU experiments). As the number of rows per embedding is different for each table, we compute cache and quantization overhead as the number of bits per embedding row.

Figure 10 plots the complete accuracy vs. memory compression trends for CPU experiments with DLRM-Kaggle dataset using compression factors computed by Table 11.
Table 11. Calculation of memory compression factor

| BITWIDTH | CACHE SIZE RATIO | BITS PER ROW (FP32) | BITS PER ROW (QUANTIZED) | ACCESS COUNTER BITS PER ROW | CACHE TAGS BITS PER ROW | COMPRESSION RATIO |
|----------|------------------|---------------------|--------------------------|-----------------------------|-------------------------|-------------------|
| 8        | 0                | 128 × 32            | 8 × 128 + 64             | 0                           | 0                       | 0.25634           |
| 4        | 0                | 128 × 32            | 4 × 128 + 64             | 0                           | 0                       | 0.14063           |
| 2        | 0                | 128 × 32            | 2 × 128 + 64             | 0                           | 0                       | 0.07813           |
| 4        | 0.3              | 128 × 32            | 4 × 128 + 64             | 32                          | 32 × 0.3                | 0.45078           |
| 8        | 0.1              | 128 × 32            | 8 × 128 + 64             | 32                          | 32 × 0.1                | 0.37422           |
| 8        | 0.05             | 128 × 32            | 8 × 128 + 64             | 32                          | 32 × 0.05               | 0.32383           |
| 4        | 0.1              | 128 × 32            | 4 × 128 + 64             | 32                          | 32 × 0.1                | 0.24922           |
| 4        | 0.05             | 128 × 32            | 4 × 128 + 64             | 32                          | 32 × 0.05               | 0.19883           |
| 2        | 0.1              | 128 × 32            | 2 × 128 + 64             | 32                          | 32 × 0.1                | 0.18672           |
| 2        | 0.05             | 128 × 32            | 2 × 128 + 64             | 32                          | 32 × 0.05               | 0.13633           |

Figure 10. Accuracy vs. memory compression factor with and without high-precision cache on Criteo-Kaggle dataset.