A New Concept of PWM Duty Cycle Computation Using the Barycentric Coordinates in a Three–Dimensional Voltage Vectors Arrangement

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ABSTRACT The paper presents a novel approach to the Pulse Width Modulation (PWM) duty cycle computing for complex or irregular voltage vector arrangements in the two (2D) and three–dimensional (3D) Cartesian coordinate systems. The given vectors arrangement can be built using at least three vectors or collections with variable number of involved vectors (i.e. virtual vectors). Graphically, these vectors form a convex figure, in particular, a triangle or a tetrahedron. The reference voltage vector position inside that figure can be expressed by the barycentric coordinates, which are calculated using the second (2D case) or the third–degree determinant (3D case) – without trigonometry and angles. Thus, the speed of the PWM duty cycle computation rises significantly. The use of the triangle area or the tetrahedron volume, instead of the standard vector projection also permits for a well–defined and universal approach to identifying the reference vector position, especially for converters with complex and/or deformed space–vector diagrams (i.e. floating DC–link, multisource DC–link). The proposed computation scheme is based on simple instructions without trigonometry thereby, the DSP processor, or digital solution for field–programmable gate array, can fast–perform this operation using atomic operations. The aim of the presented considerations is not a novel PWM modulation, but a computable idea of a general calculation scheme for cases in which the distribution of vectors is non-trivial. A detailed algebraic and geometric analysis, as well as mathematical proofs on the total consistency of the results with the standard projection method, are also included. Subsequently, the Three–Dimensional Space Vector Modulation (3D–SVM), is considered as a special background to present a novel approach.

INDEX TERMS 3D–SVM, duty cycle calculation, nonlinear loads, space vector, pulse width modulation, 3–level 4–leg inverter.

I. INTRODUCTION

The development of industrial power electronic applications is currently associated with multilevel inverters [1]–[5]. It results from the need for quality of formed voltages, currents and EMI, as well as the necessity to work with multiple sources and higher voltages. To meet these requirements Voltage Source Inverters (VSI) topologies, become more complex with the increasing number of voltage levels and inverter legs. Growing complexity of VSI topologies entails a significant increase in the complexity of Pulse Width Modulation (PWM) methods suitable for these inverters. This paper addresses the above problem by proposing an effective 3D–SVM computing algorithm based on barycentric coordinates [6] for 3–level 4–leg diode-clamped VSI. The proposed algorithm can be applied for 4–wire 3–phase applications such as DSTATCOM, multi-source Hybrid Energy Storage Systems, Active Power Filter [4], [7]–[13], local small power PV generation plant, uninterruptible power supply of various factories, offices, residential houses, etc.
According to the simple modulation algorithms, several references propose transformations of the space–vector diagrams from the Cartesian (or $\alpha \beta$) coordinates to other frames. The $gh$ [14], the 60° [15], $mn$ coordinates [16] or $a' \beta'$ coordinate system proposed in [17] are attempts to simplifying the modulation algorithm. However, all of them relies on balanced DC–link voltages. Moreover, none of the mentioned space–vector diagram transformations are applicable to 4–wire, 4–legs inverters. Analysis and comparison of the mentioned transformation methods with barycentric coordinates for 3–wire system can be found in [6]. One of the few attempts (applicable for 4–wire systems) to compute the duty cycles of the actual (i.e. non–ideal) component vectors for the three-level NPC inverter was presented in [18]. The authors proposed an extension of the $gh$ frame method of [14] to include accurate duty cycle calculations under the DC–link imbalance. The idea, called the method of projections, is quite complex and is derived after a complex analysis of geometric relationships between the basic vectors displaced by the DC–link voltage imbalance. The approach is hardly extendable to other cases, for instance, a different type of component vectors (e.g. virtual vectors) or different inverter topologies (e.g. 4–leg inverters or inverters with more than 3 levels).

A more universal method was proposed in [19]. The calculations of duty cycles are performed in a frame called $abc$ coordinates. This frame is made of three axes – $a$, $b$ and $c$ – corresponding to the respective three phases of the inverter, but forming a three–dimensional orthogonal system rather than the standard planar system with the $abc$ axes rotated by multiples of $2\pi/3$. It permits for quite simple representation of DC–link voltage imbalance and computation of duty cycles under imbalance. The method can be used for multilevel 3-leg and 4-leg inverters however, considering DC–link voltages imbalance requires an additional transformation of coordinates and allows to synthesize voltage only in a three–phase system according to its orthogonal nature.

This paper also proposes a computational approach supporting explicit space–vector PWM computations for multilevel inverters with possible DC–link voltage imbalance. The key idea in the proposed arithmetic is the use of barycentric coordinates for the duty cycle computations and the selection of the modulation triangle/tetrahedron (2D/3D). Unlike the method of [19], which uses a special coordinate frame, the proposed method is applied directly to space–vector diagrams in the natural Cartesian coordinates ($\alpha \beta$) and can be implemented to multiphase systems. The method can be applied to all types of multilevel inverters.

To achieve a better understanding of the proposed concept, the discussion was divided into smaller sections. The new general computation formula for two–dimensional space is presented in detail in Section I. The next section contains analogous considerations for the three–dimensional coordinates system. Section III contains a brief introduction the used 3D–SVM modulation and barycentric coordinates in the modulation algorithm. Proposed modulation algorithm is based on [20] but developed by balancing DC–link voltages [21]–[24], accurate generation of output voltages regardless of unbalanced capacitor voltages [18], [19], fast duty cycles calculations algorithm based on barycentric coordinates [6] and optimal switching state sequence. Experimental results are introduced in Section IV to validate the effectiveness of the proposed duty cycle computation. The article closes with a summary and a brief discussion on the experimental results.

II. PWM DUTY CYCLES COMPUTATION IN A TWO–DIMENSIONAL COORDINATE SPACE

Let $[\vec{w}_1, \vec{w}_2, \vec{w}_3]$ denote a three–element vector collection in the two–dimensional Cartesian $xy$ coordinate system shown in Fig. 1(a). Coordinates of these independent vectors meet the following equation

$$\alpha_1 \cdot \vec{w}_1 + \alpha_2 \cdot \vec{w}_2 + \alpha_3 \cdot \vec{w}_3 = \vec{e}$$  (1)

where $\alpha_1$, $\alpha_2$ and $\alpha_3$ are real numbers for scaling the length of the corresponding vector. The value of scaling coefficients from (1) can be obtained by constructing a graphic solution. However, it is not a suitable form for implementation in the Digital Control System (DCS). In order to formulate a more practical solution, the vectors arrangement in Fig. 1(a), can be transformed into a new equivalent collection represented by $\vec{v}_1$, $\vec{v}_2$, $\vec{u}$ vectors in a local $pq$ reference frame, as shown in Fig. 1(b). Thus, updated coordinates can be calculated using the following formula

$$\vec{w}_2 - \vec{w}_3 = \vec{v}_2$$
$$\vec{w}_1 - \vec{w}_3 = \vec{v}_1$$
$$\vec{e} - \vec{w}_3 = \vec{u}$$  (2)

Note that, all vectors in (2) are obtained by subtracting $\vec{w}_3$ from the other vectors and the reference vector $\vec{u}$ can be represented in a similar way to (1) by

$$\vec{u} = d_1 \cdot \vec{v}_1 + d_2 \cdot \vec{v}_2$$  (3)

where $d_1 = |\vec{u}_1|/|\vec{v}_1|$ and $d_2 = |\vec{u}_2|/|\vec{v}_2|$ are non-negative scaling coefficients referred as PWM duty cycles (PWMDC). The $d_1$ and $d_2$ can be obtained using the vector projection
principle, which is illustrated in Fig. 2. Using expressions on the sine of angles $\phi$ and $\varphi$ and based on the $h$ segment
\[ \frac{h}{|\vec{u}_1|} = \sin(\phi), \quad \frac{h}{|\vec{u}|} = \sin(\phi - \varphi) \] (4)
formally obtain
\[ |\vec{u}_1| = |\vec{u}| \cdot \frac{\sin(\phi - \varphi)}{\sin(\phi)}, \quad |\vec{u}_2| = |\vec{u}| \cdot \frac{\sin(\varphi)}{\sin(\phi)} \] (5)
To eliminate trigonometric expressions $\sin$ containing angles $\phi$ and $\varphi$, the formula of vectors cosine is applied
\[ \cos(\phi) = \frac{\vec{v}_1 \cdot \vec{v}_2}{|\vec{v}_1| \cdot |\vec{v}_2|} \]
\[ \cos(\varphi) = \frac{\vec{v}_1 \cdot \vec{u}}{|\vec{v}_1| \cdot |\vec{u}|} \]
\[ \cos(\phi - \varphi) = \frac{\vec{v}_1 \cdot \vec{v}_2}{|\vec{v}_2| \cdot |\vec{u}|} \] (6)
and also Pythagorean identity formula, which leads to the following equations
\[ d_1 = \frac{|\vec{u}|}{|\vec{v}_1|} \sqrt{1 - \cos^2(\phi - \varphi)} = \frac{|\vec{u}|}{|\vec{v}_1|} \sqrt{1 - \left( \frac{\vec{v}_2 \cdot \vec{u}}{|\vec{v}_2| \cdot |\vec{u}|} \right)^2} \] (7)
\[ d_2 = \frac{|\vec{u}|}{|\vec{v}_2|} \sqrt{1 - \cos^2(\varphi)} = \frac{|\vec{u}|}{|\vec{v}_2|} \sqrt{1 - \left( \frac{\vec{v}_1 \cdot \vec{u}}{|\vec{v}_2| \cdot |\vec{u}|} \right)^2} \] (8)
where the mark ($\circ$) designates the scalar product of two vectors. Both equations (7) and (8) are not satisfying and further optimization can be performed. Despite the elimination of trigonometric functions, they contain the square root operation. In order to obtain a simpler expression for $d_1$ and $d_2$, vectors shown in Fig. 2, can be represented as a collection of points $A, B, C$, and $D$ as illustrated in Fig. 3. Based on the Thales’ theorem, $d_1$ as the ratio of the length of the segment $a$ to the sum of segments $a$ and $b$ in Fig. 3(a),
\[ d_1 = \frac{|\vec{u}|}{|\vec{v}_1|} = \frac{a}{a + b} = \frac{h}{h + y} \] (9)
and analogically for the case illustrated in Fig. 3(b).
\[ d_2 = \frac{|\vec{u}|}{|\vec{v}_2|} = \frac{a}{a + b} = \frac{h}{h + y} \] (10)
As can be seen in Fig. 3(a), triangles $\Delta(A, D, C)$ and $\Delta(A, B, C)$ have the same base length. Thus, $d_1$ and $d_2$ can be expressed as ratio of triangle areas
\[ d_1 = \frac{\Delta_{ADC}}{\Delta_{ABC}}, \quad d_2 = \frac{\Delta_{ADB}}{\Delta_{ABC}} \] (11)
If vertex $A$ is located at the origin $(0, 0)$ of a Cartesian coordinate system and the remaining vertices are represented by point $B(v_{1x}, v_{1y})$, $C(v_{2x}, v_{2y})$ and $D(u_x, u_y)$, the area of each required triangle can be computed as the absolute value of the determinant. Thus, the PWM duty cycle for vector $\vec{v}_1$ can be written as
\[ d_1 = \left| \det \begin{bmatrix} D_x & D_y \\ C_x & C_y \end{bmatrix} \right| = \left| \det \begin{bmatrix} u_x & u_y \\ v_{2x} & v_{2y} \end{bmatrix} \right| \] (12)
and identically for vector $\vec{v}_2$
\[ d_2 = \left| \det \begin{bmatrix} D_x & D_y \\ B_x & B_y \end{bmatrix} \right| = \left| \det \begin{bmatrix} u_x & u_y \\ v_{1x} & v_{1y} \end{bmatrix} \right| \] (13)
The PWMDC for zero vector, which corresponds with point $A(0, 0)$ in Fig. 3, is equal to
\[ d_0 = \frac{\Delta_{BCD}}{\Delta_{ABC}} \] (14)
The sum of all PWMDC, computed for each triangle $\Delta(A, B, C)$, is equal to unity
\[ d_1 + d_2 + d_0 = 1 \] (15)
As pointed out, vectors’ geometric arrangement depicted in Fig. 2, has been transformed into the local triangular area, in which the reference vector $\vec{u}$ resides. Secondly, the PWMDC have been calculated using a simple rational function based on the triangle area, which can be fast computed using the absolute value of determinants. As is evident
from the presented elaboration, only vectors coordinates are
only needed. The proposed calculation scheme is widely
used in mechanics problem solving and has been successfully
adopted in the following paper for the unification of the
PWMDC computation [25]. Graphically, all three selected
vectors form a convex figure – the triangle – and the reference
voltage vector position inside that figure can be expressed
by *barycentric coordinates*, which are just calculated
using (12)–(14).

If the sum (15) is greater then unity, as it is shown in Fig. 4,

![FIGURE 4. Rescaling the length of vector \( \vec{u} \).](image)

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III. PWM DUTY CYCLES COMPUTATION IN A THREE–DIMENSIONAL COORDINATE SPACE

It is assumed that the vector $\vec{p}$ in Fig. 6, is located inside the tetrahedron $V$ with vertices $A$, $B$, $C$, and $D$. The reference vector $\vec{p}$ can be expressed as the following sum

$$\vec{p} = \vec{u} + \vec{v} + \vec{w}$$

(20)

where the vectors $\vec{u}$, $\vec{v}$, and $\vec{w}$ are the effect of a reference vector $\vec{p}$ projection on the base vectors $\vec{AB}$, $\vec{AC}$, and $\vec{AD}$ respectively

$$\vec{p} = d_B \cdot \vec{AB} + d_C \cdot \vec{AC} + d_D \cdot \vec{AD}$$

(21)

The PWMDC from (21) can be written as ratio of appropriate lengths

$$d_B = \frac{\|\vec{u}\|}{\|\vec{AB}\|}, \quad d_C = \frac{\|\vec{v}\|}{\|\vec{AC}\|}, \quad d_D = \frac{\|\vec{w}\|}{\|\vec{AD}\|}$$

(22)
Analogous results can be obtained with respect to the other as the ratio of the volume of these figures $V$. Considering that both tetrahedrons $V_1$ treated in Fig. 6(b) and more detailed in Fig. 7 is consid-

The three-dimensional case: (a) reference vector $\vec{p}$ and base vectors $\vec{u}, \vec{v}, \vec{w}$, (b), (c), and (d) triangular surface parallel to the corresponding sides of the tetrahedron $V(A, B, C, D)$.

FIGURE 6. The three-dimensional case: (a) reference vector $\vec{p}$ and base vectors $\vec{u}, \vec{v}, \vec{w}$, (b), (c), and (d) triangular surface parallel to the corresponding sides of the tetrahedron $V(A, B, C, D)$.

FIGURE 7. Geometric layout for the Thales Theorem application for the case illustrated by Fig. 6(b).

To find a more practical form of (22), the case illustrated in Fig. 6(b) and more detailed in Fig. 7 is consid-

Moreover, the line $n$ is passing through the vertex $D$ and is normal to the surfaces represented by triangles $\Delta(A, B, C)$ and $\Delta(A_D, B_D, C_D)$. Based on the geometric layout in Fig. 7, the PWMDC for vector $\vec{w}$ can be finally described by the following formula

$$d_D = \frac{\vec{w} \cdot \vec{n}}{\vec{AD} \cdot \vec{n}} = \frac{|AA_D|}{|AD|} \frac{|HD|}{|AD|} = \frac{|HH_D|}{|HD|}$$

(23)

Considering that both tetrahedrons $V(A, B, C, D)$ and $V(A, B, C, P)$ have the same base triangle $\Delta(A, B, C)$, the duty cycle $d_D$ can be expressed in barycentric coordinates as the ratio of the volume of these figures

$$d_D = \frac{V_{ABCD}}{V_{ABCP}}$$

(24)

Analogous results can be obtained with respect to the other vertices

$$d_A = \frac{V_{ABCP}}{V_{ABCD}}, \quad d_B = \frac{V_{ADCP}}{V_{ABCD}}, \quad d_C = \frac{V_{ADBP}}{V_{ABCD}}$$

(25)

Tetrahedron volume can be represented in barycentric co-

coordinates as a ratio of absolute values of determinants. Thus, finally the PWMDC can be expressed as follows

$$d_A = \begin{vmatrix} P_x - B_x & P_y - B_y & P_z - B_z \\ P_x - C_x & P_y - C_y & P_z - C_z \\ P_x - D_x & P_y - D_y & P_z - D_z \end{vmatrix} \cdot g$$

(26)

$$d_B = \begin{vmatrix} P_x - C_x & P_y - C_y & P_z - C_z \\ P_x - D_x & P_y - D_y & P_z - D_z \\ P_x - A_x & P_y - A_y & P_z - A_z \end{vmatrix} \cdot g$$

(27)

$$d_C = \begin{vmatrix} P_x - D_x & P_y - D_y & P_z - D_z \\ P_x - A_x & P_y - A_y & P_z - A_z \\ P_x - B_x & P_y - B_y & P_z - B_z \end{vmatrix} \cdot g$$

(28)

$$d_D = \begin{vmatrix} P_x - A_x & P_y - A_y & P_z - A_z \\ P_x - B_x & P_y - B_y & P_z - B_z \\ P_x - C_x & P_y - C_y & P_z - C_z \end{vmatrix} \cdot g$$

(29)

where

$$g = \left( \begin{vmatrix} D_x - A_x & D_y - A_y & D_z - A_z \\ D_x - B_x & D_y - B_y & D_z - B_z \\ D_x - C_x & D_y - C_y & D_z - C_z \end{vmatrix} \right)^{-1}$$

(30)

If the given reference vector $\vec{p}$ resides inside the tetrahedron $V(A, B, C, D)$, the sum of all duty cycles is equal to one,

$$d_A + d_B + d_C + d_D = 1$$

(31)

but if point $P$ lies outside the tetrahedron, as it is shown in Fig. 8, the length of $\vec{p}$ has to be rescaled by factor $\zeta$

$$\zeta = \frac{|AP_A|}{|AP|} \frac{|AP_A|}{|AP| + |AP_P|}$$

(32)

The following tetrahedrons $V(A, B, C, D)$ and $V(B, C, D, P)$ have a common base triangle $\Delta(B, C, D)$. In addition, straight line $n$ is perpendicular to the triangle $\Delta(B, C, D)$ surface. Therefore the scaling factor $\zeta$ can be also calculated based on Thales theorem

$$\zeta = \frac{h_{ABCD}}{h_{ABCD} + h_{BCDP}} \cdot \frac{\Delta_{BCD}}{3} = \frac{V_{ABCD}}{V_{ABCD} + V_{BCDP}}$$

(33)

There are two tetrahedrons shown in Fig. 9. Selection of the appropriate tetrahedron strongly depends on checking the result of duty cycle summation. Only if point $P$ is inside the tetrahedron, the sum (31), by definition, is equal to unity.
IV. THREE-DIMENSIONAL SPACE VECTOR MODULATION FOR THREE-LEVEL FOUR-LEG DIODE CLAMPED INVERTER

A three-dimensional fast algorithm in abc coordinates has been proposed in [4], [19], [26] but that representation limits the potential of space vector modulation. The DC–link voltage balancing [18], [21]–[24], [27], [28] is omitted though it is a critical task, especially in the Active Power Filter application [10], [13], [29], [30]. In addition, the overmodulation aspect of converter control is also not considered [31]. By using the proposed method of PWMDC calculation, balanced and unbalanced systems can be realized with balanced or unbalanced DC–link voltages. Moreover, during the DC–link voltage balancing process, the output average voltages are precisely synthesized and no output current distortion is observed [18]. The main advantage of accurate control of the DC–link voltages, is that it allows to use smaller capacitors in the DC–link. Note that the main purpose of this section is to demonstrate the abilities of the proposed approach of duty cycle computing. In order to achieve a better understanding, the discussion is divided into smaller subsections.

NOMENCLATURE

For the clarity in further consideration, the following nomenclature is proposed:

- $u_{DC}$: DC-link total voltage.
- $u_{C1}$: lower capacitor voltage.
- $u_{C2}$: upper capacitor voltage.
- $u_\Delta$: neutral-point voltage.
- $i_{NP}$: neutral-point (NP) average current.
- $l$: number of converter leg $l = 1..4$.
- $s_{il}$: $i$-switch, $l$-leg, $s_{il} = \{0, 1\}$ switch is [off, on].
- $i_l$: $l$-leg output current.
- $u_{lk}$: $l$-leg output voltage, $k$-switching state.
- $h_{lk}$: $l$-leg switches state, $k$-switching state.

![FIGURE 9. Two tetrahedrons in three dimensional system: (a) vector $\vec{p}$ resides in tetrahedron $V(B_1, B_2, B_3, B_4)$, (b) the sum of PWMDC is greater than one, (c) the sum of PWMDC is equal one.](image)

![FIGURE 10. Three-level four-leg neutral-point clamped converter.](image)

![FIGURE 11. Example switching states sequence.](image)

$B_k = \{b_{1k}, b_{2k}, b_{3k}, b_{4k}\}$: leg neutral-point flag, $k$-switching state.

$h_{lk} = \{h_{1k}, h_{2k}, h_{3k}, h_{4k}\}$: leg $k$-switch state vector.

$u_{lk}$: $l$-leg neutral-point flag, $k$-switching state.

$B = [b_1, b_2, b_3, b_4]^T$: neutral-point flags matrix.

**PRINCIPLE OF OPERATION**

The 3-level 4-leg Diode–Clamped inverter is presented in Fig. 10. A general $k$-switching state of each converter leg can be characterized using three following quantities $u_{lk}, h_{lk}, b_{lk}$:

\[
\begin{align*}
\{u_{lk}, h_{lk}, b_{lk}\} &= \begin{cases} 
\{u_{DC}, 2, 0\} & \iff [s_{1l}, s_{2l}, s_{3l}, s_{4l}] = [1, 1, 0, 0] \\
\{u_{C1}, 1, 1\} & \iff [s_{1l}, s_{2l}, s_{3l}, s_{4l}] = [0, 1, 1, 0] \\
\{0, 0, 0\} & \iff [s_{1l}, s_{2l}, s_{3l}, s_{4l}] = [0, 0, 1, 1] 
\end{cases} 
\end{align*}
\]

The first $u_l$ is the $l$-leg output voltage value, the second one $h_l$ describes the combination of gate signals of power switches $s_{il}$, and the $b_l$ informs whether the load is connected to the neutral-point (NP), marked as a square “1” in Fig. 10. The total number of possible switch state vectors is equal $3^4$. An appropriate description can be found in the Table 5 and Table 6 located in the Appendix section. The grey color of the table row indicates that $u_\Delta$ is not affected by a DC–link voltage asymmetry. Thus, coordinates of this vector in xyz reference frame are independent of $u_\Delta$. The 3D–SVM implementation is performed by the generating proper sequence of four switch state vectors $h_1, h_2, h_3, h_4$ within a period $T$ as it is shown in Fig. 11. In reference to the publications [20], [32] the three-dimensional space contains 24 base tetrahedrons.
There are four base tetrahedrons $\Delta_{1}, \Delta_{2}, \Delta_{3}, \text{and} \Delta_{4}$ per one sector. An example of a base tetrahedron $\Delta_{1}$ resides in sector $s1$ as is illustrated in Fig. 12. Each base tetrahedron can be divided into 8 smaller tetrahedrons, which correspond to an appropriate switch states matrix $H$ in Table 3. Due to the DC–link voltage unbalance phenomena, the $n$-type and $p$-type switch state matrix can be used for capacitor voltage balancing. The flowchart of the proposed algorithm is presented in Fig. 13 and described in next subsection.

**THE ALGORITHM FLOWCHART**

The position of the reference vector $\vec{p}$ is defined by one sector $\{s1, s2, s3, s4, s5, s6\}$ and one base tetrahedron $\{\Delta_{1}, \Delta_{2}, \Delta_{3}, \Delta_{4}\}$. At step 1 the position of $\vec{p}$ is calculated according to the solution given in [20] and is based on a few conditional operations. Next, the six *float vertex* coordinates for $n$-type and $p$-type $H$, from Table 3, are calculated at step 2 using Clarke transform as follows

\[
\begin{bmatrix}
v_{1x} & v_{2x} & v_{3x} & v_{4x} \\
v_{1y} & v_{2y} & v_{3y} & v_{4y} \\
v_{1z} & v_{2z} & v_{3z} & v_{4z}
\end{bmatrix} = \begin{bmatrix}
\frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\
0 & \frac{\sqrt{3}}{3} & -\frac{1}{\sqrt{3}} \\
\frac{1}{3} & \frac{1}{3} & \frac{1}{3}
\end{bmatrix} \cdot U
\]  

where

\[
U = \begin{bmatrix}
u_{11} - u_{41} & u_{21} - u_{41} & u_{31} - u_{41} \\
u_{12} - u_{42} & u_{22} - u_{42} & u_{32} - u_{42} \\
u_{13} - u_{43} & u_{23} - u_{43} & u_{33} - u_{43} \\
u_{14} - u_{44} & u_{24} - u_{44} & u_{34} - u_{44}
\end{bmatrix}^T
\]  

At step 3 all needed duty cycles are computed based on barycentric coordinates (26)-(30). Calculation of the following sum at step 4 for each switch state matrix $H$

\[
\Sigma_{k} = \text{sum}(d_{k})
\]  

and $p$-type $H$, from Table 3, are calculated at step 2 using Clarke transform as follows

\[
\begin{bmatrix}
v_{1x} & v_{2x} & v_{3x} & v_{4x} \\
v_{1y} & v_{2y} & v_{3y} & v_{4y} \\
v_{1z} & v_{2z} & v_{3z} & v_{4z}
\end{bmatrix} = \begin{bmatrix}
\frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\
0 & \frac{\sqrt{3}}{3} & -\frac{1}{\sqrt{3}} \\
\frac{1}{3} & \frac{1}{3} & \frac{1}{3}
\end{bmatrix} \cdot U
\]  

where

\[
U = \begin{bmatrix}
u_{11} - u_{41} & u_{21} - u_{41} & u_{31} - u_{41} \\
u_{12} - u_{42} & u_{22} - u_{42} & u_{32} - u_{42} \\
u_{13} - u_{43} & u_{23} - u_{43} & u_{33} - u_{43} \\
u_{14} - u_{44} & u_{24} - u_{44} & u_{34} - u_{44}
\end{bmatrix}^T
\]  

A simple analysis of the four possible combinations of the signs of the imbalance voltage and the average neutral point
current leads to the conclusion that it is sufficient to compare the following quantities

\[ \varepsilon_n = i_{NPn} \cdot u_{\Delta}, \varepsilon_p = i_{NPp} \cdot u_{\Delta} \]  

where \( i_{NPn} \) and \( i_{NPp} \) are estimates of the expected average neutral point currents corresponding to their respective types of bias

\[ \begin{align*}
   i_{NPn} &= [i_1 \ i_2 \ i_3 \ i_4] \cdot B_n^T \cdot d_n \\
   i_{NPp} &= [i_1 \ i_2 \ i_3 \ i_4] \cdot B_p^T \cdot d_p
\end{align*} \]  

If \( \varepsilon_n \) is greater than \( \varepsilon_p \), then \( H_p \) should be selected; otherwise, the better choice is negative bias represented by \( H_n \). Finally, at step 6, the selected pair \( \{H, d\} \) is sent to the pulse pattern generator implemented in a programmable logic device.

V. EXPERIMENTAL RESULT

An experimental prototype of an inverter is presented in Fig. 14, while the parameters are presented in Table 4. The digital control system (DCS) contains a DSP (Texas Instruments TMS320C6672) and a field-programmable gate array FPGA (Cyclone V). The DC-link is supplied by two adjustable dc-voltage sources \( U_{DC1} \) and \( U_{DC2} \) with additional switch \( S \) for voltage balancing experiments. Schematic of the experimental setup is illustrated in Fig. 15. The experimental research plan included the following issues:

- DC-link capacitors active voltage balancing ability using redundant switch states (Fig. 16),
- Preserving the sinusoidal output currents during the DC-link voltages asymmetry (Fig. 17),
- Proper generation of constant gamma component in output currents by adding the common signal (Fig. 18),

| symbol | value | description |
|--------|-------|-------------|
| \( E_1 \) | 75V, 45V | DC source voltages |
| \( E_2 \) | 75V, 45V | DC source voltages |
| \( C_1 \) | 300\( \mu \)F | upper capacity |
| \( C_2 \) | 300\( \mu \)F | lower capacity |
| \( R \) | 15\( \Omega \) | load resistor |
| \( L \) | 3mH | load inductor |
| \( R_4 \) | 2.2\( \Omega \) | 4-th leg resistor |
| \( L_4 \) | 6mH | 4-th leg inductor |
| \( f_c \) | 5kHz | PWM frequency |
| \( f_n \) | 50Hz | output frequency |
| \( S \) | ON/OFF | neutral point additional switch |

![FIGURE 14. An experimental prototype with DCS.](image1)

![FIGURE 15. Schematic of experiment.](image2)

![FIGURE 16. DC–link capacitors voltage active balancing for referenced vectors without capacitors voltage asymmetry compensation a) \( \beta = [0.57 \cdot \cos(\omega t), 0.57 \cdot \sin(\omega t), 0] \), b) \( \beta = [0.46 \cdot \cos(\omega t), 0.46 \cdot \sin(\omega t), 0] \).](image3)

![TABLE 4. Experiment circuit diagram and modulation parameters.](image4)
Selected higher-order current harmonic injection (Fig. 19),
• The phase current asymmetry generation (Fig. 20).

VI. CONCLUSION
The proposed algorithms using barycentric coordinates based on area – 2D case, solved by (12), (13) – or
TABLE 5. The leg voltages, states and neutral–point flags for Three–Level Four–Leg Neutral–Point Clamped Converter (part I).

| n₁ | n₂ | n₃ | n₄ | b | b |
|----|----|----|----|---|---|
| 1  | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 2  | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 3  | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 4  | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 5  | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 6  | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 7  | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 8  | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 9  | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 10 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 11 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 12 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 13 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 14 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 15 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 16 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 17 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 18 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 19 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 20 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 21 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 22 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 23 | 0  | 0  | 0  | 0  | 0000 | 0000 |
| 24 | 0  | 0  | 0  | 0  | 0000 | 0000 |

TABLE 6. The leg voltages, states and neutral–point flags for Three–Level Four–Leg Neutral–Point Clamped Converter (part II).

| n₁ | n₂ | n₃ | n₄ | b | b |
|----|----|----|----|---|---|
| 1  | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 2  | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 3  | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 4  | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 5  | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 6  | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 7  | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 8  | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 9  | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 10 | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 11 | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 12 | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 13 | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 14 | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 15 | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 16 | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 17 | 0  | 0  | 0  | 0  | 1111 | 1111 |
| 18 | 0  | 0  | 0  | 0  | 1111 | 1111 |

volume – 3D case, solved by (26)–(30) – are proposed as a tool for PWMDC computations, especially for complex and unbalanced lattices of inverter vectors. Results of benchmark presented in Table 2 show the main advantage of the proposed computation idea – a short time of code execution, what leads to the conclusion, that this method is particularly useful for complex systems (multilevel, multiphase inverters, high–frequency systems, virtual vector methods). The concept permits building the modulation algorithms by referring straight to the converter switch state vectors. Thus, the presented computation idea is suitable for multilevel inverters of different types (diode clamped, flying capacitors or matrix converters). The proposed algorithm enables precise voltages and currents forming during unbalanced capacitor voltages (Fig. 17), as well as it allows to balance DC–link voltages (Fig. 16) using redundant vectors. Comparing currents in Fig. 16 and Fig. 17 it is notable, that considering DC–link unbalanced voltages leads to a better quality of output currents. Possibility of injecting chosen harmonics (Fig. 19) and generation of asymmetry (Fig. 20) or constant gamma component (Fig. 18) in currents show that the proposed algorithm can be a suitable tool for Active Power Filters. The use of barycentric coordinates helps in the development of computation schemes. Note that the method does not influence the results of the PWM duty cycle computations at all, so further analysis of formed voltages and currents in this paper seems pointless, because this kind of research is widely reported in the literature.

The presented article shows that trigonometric functions can be eliminated from the modulation algorithm. The presented elaborations lead to the conclusion, that the PWM duty cycle computation can be realized using the simple rational functions and voltages coordinates (in most cases calculated using the Clarke transform). In general, this approach does not give the new spectacular PWM features observed in the frequency spectrum of voltages and currents. The obtained simplification permits for using the low costs FPGA devices because the core of calculation can be based on the parallel add/subtract and multiply operation. If we take into account a very high operating frequency of the GaN or SiC power switches and the limitations of the one-core processors, the undertaken research is purposeful and justified [33]–[36]. The proposed solution is particularly useful when considering the irregular space of voltage vectors. Presented solutions also add uniformity and transparency to the description of PWM–related problems.

The paper authors demonstrated that the proposed PWM duty cycle computation can be successfully applied to the three-dimensional space vector modulation for a three–level four–leg NPC inverter where the volume–based rational functions have been used.

APPENDIX
See Tables 5 and 6.

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