Fabrication of deep-sub-micrometer NbN/AlN/NbN epitaxial junctions on a Si-substrate

Wei Qiu* and Hirotaka Terai

Advanced ICT Research Institute, National Institute of Information and Communications Technology, 588-2 Iwaoka, Nishi-ku, Kobe, 651-2492, Japan
E-mail: qiuwei@nict.go.jp

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We have developed a novel fabrication process for ultra-small, full-epitaxial NbN Josephson junctions on a TiN buffered silicon (Si) substrate. We use an electron beam lithography for junction definition followed by a reactive-ion-etch (RIE). A chemical mechanical polishing and an RIE process with chemical mechanical polishing with CMP, as described in the following section. Full-epitaxial NbN/AlN/NbN junctions with low leakage current were successfully fabricated with a junction size as small as 0.27 μm in diameter. After measuring the current-voltage (I-V) characteristics of the junction, the SiO2 dielectric layer, which served as the isolation between the base electrode and the wiring layer, was removed with a buffered HF (BHF) solution. The I-V characteristics were re-measured and compared to the original properties.

Details of the fabrication process of full-epitaxial NbN/AlN/NbN tri-layer structure on a Si (100) wafer can be found in our early report.22) First, a 40 nm thick TiN film was deposited on a hydrogen-terminated Si substrate at a substrate temperature of 850 °C with a total outgas pressure of 1 × 10\(^{-6}\) Pa by dc magnetron sputtering method. The background pressure without substrate heating was better than 8 × 10\(^{-8}\) Pa. X-ray diffraction (XRD) analysis revealed a single (200)-oriented reflection peak at 42.66° in the \(\theta/2\theta\) scan, resulting in a lattice constant \(a_0 = 0.423\) nm. The TiN film exhibited a superconducting transition temperature \(T_c\) of 5.6 K, a resistivity at 10 K of 3.2 \(\mu\Omega\) cm, and a residual resistivity ratio (the ratio of resistivities at 300 K and 10 K) of 5.4. The lattice constant of TiN (200) film is therefore relatively close to that of a (200)-oriented NbN film deposited at optimal conditions \((a_0 = 0.446\) nm). The thin TiN film serves as a buffer layer for the epitaxial growth of NbN film, as well as for the NbN/AlN/NbN tri-layer.

After the initial growth of (200)-oriented TiN film, the wafer was cooled down below 100 °C before the NbN/AlN/NbN tri-layer deposition in situ by dc reactive sputtering without breaking the vacuum. The 100 nm thick base and 200 nm thick counter NbN layers were deposited in the mixture of Ar and N\(_2\) gases, while a 2 nm thick AlN tunnel barrier was deposited in a pure N\(_2\) gas. The \(T_c\) of the 200 nm thick NbN film on the TiN buffer was 15.3 K, which is almost equal to that of on a MgO (100) substrate.20) We examined the crystal structure of NbN/AlN/NbN tri-layer by XRD analysis and could not identify any other peaks apart from a single (200) peak, which suggests the growth of a cubic structure of AlN barrier with a thickness up to 2 nm. Additional information regarding the AlN thickness dependence of the crystal structure of the counter NbN electrode, as well as the crystal structure of the AlN tunnel barrier, can be found in our early work.20,22)
Figure 1 illustrates the fabrication process of small Josephson junctions with an EBL and a planarization process. Firstly, the base electrodes of the junction were patterned by an i-line stepper (Canon FPA-3030 i5+) using a positive photoresist AZ-MiR 703 (Integrated Micro Material Inc.). The NbN/AlN/NbN tri-layer and the TiN buffer layer was etched by a reactive ion etching (RIE) using CF4 gas for NbN and TiN, and Ar gas for AlN. After removing the photoresist, the junctions were patterned by EBL using a ZEP-520A positive resist with a thickness of 320 nm, where an ELIONIX ELS-F125 system with an EB of 125 kV was employed. A thin Al or MgO layer was deposited by dc sputtering, followed by a lifted-off in NMP solution. This thin layer served as an etching mask for the junction definition in RIE with a CF4 plasma. The mask layer was eliminated by a wet or dry etching subsequently after the junction RIE process.

The SiO2 was deposited by rf sputtering to provide the interlayer isolation between the base electrodes and the wiring layer. Here, the thickness of SiO2 was determined from the thickness of the tri-layer, including the TiN buffer layer, the over-etched Si, and an additional 100 nm for the following planarization process by CMP. A total thickness of 500 nm SiO2 was deposited. To avoid the pattern size dependence of the polishing rate in the CMP process, we employed a caldera-based planarization that has been developed for the SFQ circuitry process.24,25) Caldera walls with a width of 1.5 μm were created at the edges of base electrodes by RIE. By etching the SiO2 for an appropriate time, the surface of SiO2 on the base electrode is approximately at the same height as the surface of SiO2 on the Si wafer, as shown in Fig. 1(e). Then, the wafer was planarized by CMP in a TRCP380 CMP system (Techno Rize Inc.). As a result, as illustrated in Fig. 1(f), the wafer surface can be completely planarized by the CMP process with a relatively short polishing time, with no dependency on the pattern size.

The contact via-holes were patterned by an i-line stepper followed by an RIE to a depth of 200 nm, which equals to the height of the counter electrode. The remaining SiO2 was etched by a CHF3 plasma until the depth of contact via-hole is less than 200 nm. The AlN/NbN acted as an etching stopper for the CHF3 plasma. Multiple etches in the CHF3 plasma of short duration were needed to prevent over-etching of the SiO2. The step profiler verified the etching progress after each step. The caldera-based planarization and CHF3 etching process provide a reliable solution to form the junction and the base contacts without having to measure the thickness of SiO2 with an ellipsometer.

Finally, a NbTiN wiring layer with a thickness of 300 nm was deposited and patterned. Unwanted TLSs in the amorphous SiO2 can contribute towards a significant dielectric loss at low microwave powers and low temperatures. To remove the SiO2 dielectric layer, we immersed the sample in a BHF for 10 min. Figure 2 shows the scanning electron microscope images of the fabricated junctions with the design junction sizes of 0.7 and 0.4 μm in diameters after removing the SiO2 interlayer. Both junctions are smaller than the designed sizes because of the shrinkage during the junction RIE process. The estimation of the actual junction size from its electrical properties will be described in the next section.

To evaluate the junction properties, we measured the I–V characteristics of the fabricated junctions at 4.2 K. The test chip was enclosed in a μ-metal cylinder to shield the sample from ambient magnetic field fluctuations. All coaxial channels connected from 4.2 K to the room-temperature electronics were heavily filtered through the low-pass filter placed.
next to the chips with a cut-off frequency of a few kHz. Figure 3 shows a typical $I-V$ curve of the NbN/AlN/NbN epitaxial junction with a designed junction size of 0.9 $\mu$m in diameter. The black curve and the red curve are the measured $I-V$ curves before and after removing the SiO$_2$ dielectrics layer, respectively. Both curves show a similar trend, indicating that the wet etching process by BHF did not have a significant impact on the properties of the junction, such as the gap-voltage and the sub-gap region (insert in Fig. 3). The normal resistance of the junction, $R_N$, measured at 10 mV, is approximately 24.9 k$\Omega$. The sub-gap resistance, $R_{SG}$, estimated at 3 mV, is 3 M$\Omega$. The ratio of $R_{SG}/R_N$ is 121, which suggests an excellent quality of the tunnel barrier with a very low leak current.

All fabricated junctions show a clear gap structure with designed junction sizes from $20 \times 20$ $\mu$m$^2$ to as small as 0.4 $\mu$m in diameter. A small “knee” structure observed at the gap voltage suggests a slight difference in energy gaps between the base NbN electrode and the counter NbN electrode due to a slightly lower crystallinity for the NbN film very close to the interface than the base NbN electrode. However, as the junctions in this paper have the AlN barrier thickness less than 2 nm, we believe that the cubic structure remains dominant in the AlN tunnel barrier instead of a hexagonal phase of AlN as revealed by XRD analysis.$^{20}$

From the largest junction on the chip ($20 \times 20$ $\mu$m$^2$), we calculated the critical current density of the junction, $J_c$, as $\pi V_G/4R_A A$, where $V_G$ is the gap voltage of the junction, $A$ is the junction area. For a uniformed $J_c$ across the tested chip ($2 \times 5$ mm$^2$), one would expect a constant $R_N A$ product according to the Ambegaokar–Baratoff relation.$^{26}$ However, the $R_N A$ product increases as the junction size decreases, as depicted by the black curve in Fig. 4. This suggests that the actual junction areas are smaller than the designed values, which is quite reasonable due to the shrinkage from over-etching during the junction RIE process.

In Fig. 4, we plot the junction area dependence of $R_N A$ assuming various junction shrinkage values, $\Delta d$. If zero shrinkage is assumed ($\Delta d = 0$ $\mu$m, the black curve in Fig. 5),
there is an inverse proportionality between the junction size and the $R_{N\!A}$ value. Conversely, a $\Delta d$ of $-0.25 \, \mu m$ resulted in a direct proportionality between the junction size and the $R_{N\!A}$ value, as shown in the blue curve in Fig. 5. If we assume a $\Delta d$ of $-0.13 \, \mu m$, the $R_{N\!A}$ product becomes virtually constant regardless of the junction area, as indicated by the red curve in Fig. 5. The designed junction diameters of 0.7 and 0.4 $\mu m$ in Fig. 2 are reduced to 0.57 $\mu m$ and 0.27 $\mu m$.

We verified the global variation of $J_c$ and $\Delta d$. Figure 5 summarizes the measured results of six chips with their relative locations within CHIP-A to CHIP-F, representing different areas across the 2 inch wafer. The junction shrinkage $\Delta d$ of each measured chip was extracted similar to that of the junction area independence of $R_{N\!A}$, as shown in Fig. 4. The extracted $\Delta d$ is virtually constant at $-0.13 \, \mu m$ for CHIP-A to CHIP-E. CHIP-F showed a slightly larger $\Delta d$ value of $-0.15 \, \mu m$. The slightly larger $\Delta d$ is considered within a reasonable error margin due to the non-uniformity in the RIE etching rate across the wafer, being slightly higher at its periphery than in its center. The $J_c$ was distributed within a range from 40 to 59 A cm$^{-2}$ across the wafer. We attribute the variation of $J_c$ to the non-uniformity of the AlN tunnel barrier. The AlN tunnel barrier is deposited by dc reactive sputtering with an 8 inch magnetron cathode. However, a non-uniform magnetic field on the cathode may lead to a thickness distribution of the AlN tunnel barrier. For future work, a rotational substrate holder for the deposition may address this concern.

We have developed a novel fabrication process for deep-sub-micrometer NbN/AlN/NbN epitaxial junctions by EBL and planarization with CMP on a Si substrate. The fabricated junctions showed a clear gap structure with designed junction size as small as 0.4 $\mu m$ in diameter. All junctions have very high sub-gap resistance, $R_{SG}$, with an $R_{SG}/R_{N}$ ratio over 100, suggesting small leakage currents and a high-quality AlN tunnel barrier. After the initial measurement of the $I-V$
curves, the SiO$_2$ dielectric layer used as the isolation between the base and the wiring layers was removed by wet etching in a BHF solution. By comparing the $I$–$V$ curves before and after the removal of SiO$_2$, we found that wet etching with BHF has no significant impact on the junction properties. The junction shrinkage, $\Delta d$, was estimated to be 0.13 $\mu$m from the junction area independence of $R_N$ product, leading to an actual junction diameter of 0.27 $\mu$m for the design size of 0.4 $\mu$m. The $\Delta d$ across the 2 inch wafer is nearly constant at 0.13 $\mu$m. A slightly larger shrinkage $\Delta d$ was found at the periphery of the wafer due to the differences in the etching rate of NbN during the junction definition. The $J_c$ was extracted from chips at different locations and ranged from 40 to 59 A cm$^{-2}$, suggesting a non-uniform AlN tunnel barrier across the wafer. Although we have developed a new fabrication process for deep-sub-micrometer NbN/AlN/Nb tunnel junctions with low-$J_c$ for superconducting qubit application, one can also use this technology in high-$J_c$ tunnel junction fabrication for a broad range of superconducting quantum interference devices, SFQ logic circuits, voltage standards.

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ORCID iDs Wei Qiu https://orcid.org/0000-0001-8195-1171

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