A 2.48Gb/s QC-LDPC Decoder Implementation on the NI USRP-2953R

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Abstract—The increasing data rates expected to be of the order of Gb/s for future wireless systems directly impact the throughput requirements of the modulation and coding subsystems of the physical layer. In an effort to design a suitable channel coding solution for 5G wireless systems, in this brief we present a massively-parallel 2.48Gb/s Quasi-Cyclic Low-Density Parity-Check (QC-LDPC) decoder implementation operating at 200MHz on the NI USRP-2953R, on a single FPGA. The algorithmic innovations leading to an architecture-aware design, central to this work, are presented in [1]. The high-level description of the entire massively-parallel decoder was translated to a Hardware Description Language (HDL), namely VHDL, using the algorithmic compiler [2] in the National Instruments LabVIEW™ Communication System Design Suite (CSDSTM) in approximately 2 minutes. This implementation not only demonstrates the scalability of our initial work in [1] but also, the rapid prototyping capability of the LabVIEW™ CSDSTM tools. As per our knowledge, at the time of writing this paper, this is the fastest implementation of a standard compliant QC-LDPC decoder on a USRP using an algorithmic compiler.

Index Terms—5G, mm-wave, SDR, USRP, QC-LDPC, layered decoding.

I. INTRODUCTION

Wireless data traffic is expected to increase by a 1000 fold [3] by the year 2020 with more than 50 billion devices connected to these wireless networks with peak data rates up to ten Gb/s [4]. To address these challenges, the next generation of wireless cellular technology being envisioned and researched today is collectively termed as Beyond-4G (B-4G) and 5G. However, the envisioned operation of 5G systems in the mm-wave (30-300GHz) spectrum comes with challenges such as, reliance on line of sight (LOS) communication, short range of communication, significantly increased shadowing loss and rapid fading in time, necessitating techniques such as large antenna arrays and rapidly adaptive beamsteering. From a physical layer perspective, the processing budget (especially time) available to the channel encoder and decoder will further decrease (relative to current generation systems such as 4G LTE).

With this in mind, in our ongoing research we focus on high-throughput and low-latency error control coding solutions (primarily based on Low-Density Parity-Check (LDPC) [5] family of codes) specially suited to 5G mm-wave systems. At the time of writing this paper, a detailed progress report focusing on the algorithmic innovations for high-throughput and a subsequent case study leading to a 608Mb/s (at 260MHz) standard compliant Quasi-Cyclic (QC) LDPC decoder is presented in [1] and [6]. To adapt to the evolving specifications for 5G technology, implementations for our ongoing research must be reconfigurable and scalable, and must exhibit state-of-the-art performance, hence we choose the FPGA approach to developing hardware instead of the ASIC approach.

The Universal Software Radio Peripheral (USRP) is a widely used Software Defined Radio (SDR) system that is a flexible and an affordable transceiver with the potential to turn a standard host (such as a PC) into a powerful wireless prototyping system. The availability of state-of-the-art, highly reconfigurable hardware platforms (such as the FPGA) on the USRP has opened up a huge space for implementing theoretical algorithms at high-speeds, crucial for systems such as those required by 5G wireless.

In this brief we present an application of the work in [1], a 2.48Gb/s FPGA-based QC-LDPC decoder implemented on the NI USRP-2953R (which has the Xilinx Kintex7 (410t) FPGA) using the FPGA IP compiler in LabVIEW™ CSDSTM. Massive-parallelization was accomplished by employing 6 decoder cores in parallel without any modification at the HDL level. This compiler translated the entire high-level description of the parallelization (done in a graphical algorithmic dataflow language) to VHDL and further generated an optimized hardware implementation from the algorithmic description. The main contributions of this work are: (1) demonstration of the scalability of our decoder architecture in [1] (2) the ability of the LabVIEW™ CSDSTM tools to rapidly prototype high-level algorithmic description onto FPGA hardware.

The remainder of this paper is organized as follows. Section II outlines the construction of QC-LDPC codes and the decoding algorithm used for the implementation. A brief overview of the techniques leading to the software-pipelined decoder core is given in Section III. The process of implementing the 2.48Gb/s decoder and the performance results are detailed in Sections IV and V respectively, and finally we conclude with Section VI.

II. QUASI-CYCLIC LDPC CODES AND DECODING

Mathematically, given k message bits, an LDPC code is a null-space of its $m \times n$ PCM H, where $m$ denotes the number of parity-check equations or parity-bits and $n = k + m$
denotes the number of variable nodes or code bits \[7\]. In the Tanner graph representation (due to Tanner \[8\]), \(\mathbf{H}\) is the incidence matrix of a bipartite graph comprising of two sets: the check node (CN) set of \(m\) parity-check equations and the variable node (VN) set of \(n\) variable or bit nodes; the \(i^{th}\) CN is connected to the \(j^{th}\) VN if \(\mathbf{H}(i, j) = 1\), \(1 \leq i \leq m\) and \(1 \leq j \leq n\).

QC-LDPC codes are represented by an \(m_b \times n_b\) base matrix \(\mathbf{H}_b\) which comprises of cyclically right-shifted identity and zero submatrices both of size \(z \times z\) where, \(z \in \mathbb{Z}^+, 1 \leq i_b \leq m_b\) and \(1 \leq j_b \leq n_b\), the shift value, \(s = \mathbf{H}_b(i_b, j_b) \in \mathcal{S} = \{-1\} \cup \{0, \ldots, z-1\}\) The PCM matrix \(\mathbf{H}\) is obtained by expanding \(\mathbf{H}_b\) using the mapping,

\[
s \longrightarrow \begin{cases} 
I_s, & s \in \mathcal{S} \setminus \{-1\} \\
0, & s \in \{-1\}
\end{cases}
\]

where, \(I_s\) is an identity matrix of size \(z\) which is cyclically right-shifted by \(s = \mathbf{H}_b(i_b, j_b)\) and \(0\) is the all-zero matrix of size \(z \times z\). Owing to this structure provided by QC-LDPC codes, the decoding of these codes becomes much simpler in hardware (mainly due to the simplified interconnect complexity) compared to unstructured LDPC codes. We believe that the family of structured LDPC codes are highly likely candidates for 5G systems. Thus, to demonstrate the initial phase of our FPGA decoder architecture \[1\], \[6\], we provide a case study for 5G systems. Thus, to demonstrate the initial phase of our FPGA decoder architecture \[1\], \[6\], we provide a case study for 5G systems. Thus, to demonstrate the initial phase of our FPGA decoder architecture \[1\], \[6\], we provide a case study for 5G systems. Thus, to demonstrate the initial phase of our FPGA decoder architecture \[1\], \[6\], we provide a case study for 5G systems. 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Figure 1: Illustration of software pipelining of layers for the case study. (a) Layer-level processing view for the Baseline architecture showing the cascade of the GNPU and LNPU for-loops (b) Layer-level processing view for the Pipelined architecture showing the two for-loops operating in parallel for half of a decoding iteration. Note that, GNPU (LNPU) array refers to a collection of $z$ GNPNUs (LNPNUs) which operate in parallel so as to exploit the structure provided by QC-LDPC codes as shown in [1].

in *LabVIEW*™ CSDSTM translated the high-level description into a VHDL description.

On account of the scalability and reconfigurability of the decoder architecture in [1], it is possible to achieve high throughput by employing multiple decoder cores in parallel. Fig. 2 shows the top-level multi-core decoder virtual instrument (VI), where 6 cores are deployed on a single *Xilinx Kintex7 FPGA* (410t). The high-level operation of the decoder is described in the steps (corresponding to the highlighted sections in Fig. 2):

1) Serial stream of the encoded data is read as frames from the host-to-target Direct Memory Access (DMA) mechanism. Here, host may be an arbitrary processing platform such as a PC or a real-time controller and target is the *Xilinx Kintex7 FPGA* (410t) on the *NI USRP-2953R*. This data is subsequently stored in the Dynamic Random Access Memory (DRAM).
2) Request frames from the DRAM.
3) Read and buffer frames from the DRAM.
4) Distribute incoming frames to the cores in a round-robin manner.
5) Perform decoding with fixed-latency, parallel processing of frames staggered with respect to time. Buffer the decoded frames.
6) Collect the decoded frames and serialize them with respect to the round-robin manner used in step (3).
7) Write frames to the target-to-host DMA mechanism.

**V. RESULTS**

The performance and resource utilization of the Baseline and the Pipelined version is compared in Table I. The resources consumed by the Pipelined decoder are almost the same as that of the Baseline decoder, in spite of the 1.5$x$ increase in throughput performance. The 2.48Gb/s decoder was developed in stages, where at each stage a core was added (except for stage 3) and the performance and resource figures were recorded. The results of each stage are compared in Table II.

The Bit Error Rate (BER) performance of the 2.48Gb/s version (with 6 cores) is shown in Fig. 3.

We have successfully demonstrated this work in *IEEE GLOBECOM’14* [12] where an overall throughput of 2.06Gb/s was achieved by using five decoder cores in parallel on the *Xilinx Kintex7 (410t) FPGA* in the *NI USRP-2953R*.

**VI. CONCLUSION**

This work validates the scalability of our decoder architecture in [1] by deploying multiple decoder cores in parallel. The development was done using an algorithmic compiler that translated the high-level description of the decoding algorithm into an HDL in approximately 2 minutes. The standalone standard compliant decoder achieves an overall throughput of 2.48Gb/s at an operating frequency of 200MHz on the *Xilinx Kintex-7 FPGA* in the *NI USRP-2953R*. With little or no modification this decoder can be applied to a large family of standard compliant QC-LDPC codes such as those specified in IEEE 802.16e and Digital Video Broadcast.
Figure 2: Top-level VI describing the parallelization of the QC-LDPC decoder on the NI USRP-2953R containing the Xilinx Kintex7 (410t) FPGA.
Baseline | Pipelined
--- | ---
Throughput (Mb/s) | 290 | 420
Clock Rate (MHz) | 200 | 200
Time to generate VHDL (min) | 2.02 | 2.08
Total Compile Time (min) | ≈36 | ≈36
Total Slice (%) | 26 | 28
LUT (%) | 16 | 18
FF (%) | 9 | 10
DSP (%) | 5 | 5
BRAM (%) | 11 | 11

Table I: Performance and resource utilization comparison for the Baseline architecture with the Pipelined architecture of the QC-LDPC decoder on the NI USRP-2953R containing the Xilinx Kintex7 (410t) FPGA.

| Cores | 1 | 2 | 4 | 5 | 6 |
|---|---|---|---|---|---|
| Throughput (Mb/s) | 420 | 830 | 1650 | 2060 | 2476 |
| Clock Rate (MHz) | 200 | 200 | 200 | 200 | 200 |
| Time to VHDL (min) | 2.08 | 2.08 | 2.08 | 2.02 | 2.04 |
| Total Compile Time (min) | ≈36 | ≈60 | ≈104 | ≈132 | ≈145 |
| Total Slice (%) | 28 | 44 | 77 | 85 | 97 |
| LUT (%) | 18 | 28 | 51 | 62 | 73 |
| FF (%) | 10 | 16 | 28 | 33 | 39 |
| DSP (%) | 5 | 11 | 21 | 26 | 32 |
| BRAM (%) | 11 | 18 | 31 | 38 | 44 |

Table II: Performance and resource utilization comparison for versions with varying number of cores of the QC-LDPC decoder implemented on the NI USRP-2953R containing the Xilinx Kintex7 (410t) FPGA.

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