A low-noise 71-dBΩ transimpedance 31-GHz bandwidth optical receiver with automatic gain control in 0.13-μm SiGe BiCMOS

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Abstract A low-noise high-gain high-speed optical receiver is fabricated in 0.13-μm SiGe BiCMOS. The transimpedance amplifier incorporating a differential common-base shunt-feedback topology features isolation to input capacitance and high transimpedance limit. Specifically, a comprehensive analytical expression of the input-referred noise current power spectral density of the transimpedance amplifier is derived and investigated, which provides insights for noise optimization. Additionally, the linearity of intermediate stages is improved by a modified variable-gain amplifier operating with automatic gain control. The measured results show a low noise level of 14.5 pA/√Hz, 31-GHz bandwidth, and the maximum 71-dBΩ transimpedance.

key words: optical interconnects, low-noise transimpedance amplifier, variable-gain amplifier, automatic gain control, SiGe BiCMOS

Classification: optical interconnects

1. Introduction

A rapidly growing number of networked devices and users require massive data transmission. As predicted by Cisco, the global data center IP traffic of 2021 will reach 20.6 zettabytes, where the portion of traffic within the data center will still account for 71.5% [1]. These trends present challenges of designing high-speed short-reach optical interconnects, in which the transmission capacity is expected to soon exceed current 100-Gb/s standard [2].

An analog optical receiver (RX) which incorporates a transimpedance (TIA) input stage and post amplifying stages plays a critical role in the whole transmission link. RXs operating at tens of Gb/s must meet such rigid specification budgets as transimpedance, bandwidth, dynamic range, and power efficiency [3, 4, 5, 6]. There are several structures for realizing a TIA, like resistive shunt-feedback (RSF), common-base (CB) or common-gate (CG), and regulated cascode (RGC). The RSF TIA is advantageous for its simplicity and low-noise feature [3, 4, 5], while the drawback is the dependence of bandwidth and stability on input capacitance [7, 8]. Additionally, it is difficult to trade off transimpedance against bandwidth in high-speed applications [9]. By adopting passive networks to tune out parasitic effects [10, 11] or introducing post-amplifier equalization technique [12], the negative impacts of the issues can be mitigated. A CB or CG TIA can be another alternative to relieve the dependence, while lower transimpedance limit and fewer degrees of freedom for noise optimization are unfavorable [9, 13, 14]. By adding a boosting amplifier to form local feedback, the RGC stage shows large effective transconductance and equivalently low input resistance [15]. The combination of a CB, CG or RGC stage and a RSF topology offers isolation to input capacitance and high transimpedance limit, while noise optimization becomes more complicated. Post amplifying stages are generally implemented as cascaded limiting amplifiers (LAs) or variable-gain amplifiers (VGAs). Automatic gain control (AGC) potentially reduces jitter and pulse-width distortion under circumstances of large input current swing.

Several power-efficient 40-Gb/s and beyond TIAs and RXs implemented in CMOS technology were reported [11, 16, 17, 18, 19]. In these designs, series or shunt inductive peaking techniques were employed for bandwidth extension. However, relatively poor noise performance or narrow bandwidth was achieved. Superior performance of SiGe BiCMOS over CMOS makes it possible to design high-speed circuits with high performance, while restrict power consumption to an acceptable level [20]. A couple of chips realized in SiGe BiCMOS were published [3, 4, 5, 6, 21, 22, 23, 24, 25, 26].

A low-noise high-gain high-speed optical RX fabricated in 0.13-μm SiGe BiCMOS is proposed. The differential CB-RSF TIA provides isolation to input capacitance and high transimpedance limit. Specifically, a comprehensive analytical expression of the input-referred noise current power spectral density (PSD) of the TIA is derived and investigated. The features of the expression are used as guidance for noise optimization. Furthermore, the linearity of intermediate stages is improved by a modified VGA tuned by an AGC loop. The paper is organized as follows. Section II presents the architecture of the RX, with the elaboration of noise optimization and transimpedance gain followed in Section III. Experimental results are presented.
in Section IV. The conclusions are drawn in Section V.

2. Architecture

The architecture of the proposed RX is depicted in Fig. 1, which consists of a differential CB-RSF TIA, a pseudo- to truly-differential conversion circuit, VGA stages with AGC, an output buffer, and a DC offset cancellation (DCOC) network. The photodiode parasitic capacitance is modeled by \( C_{PD} \). The differential TIA offers improved suppression on power supply noise and substrate coupling. The conversion circuit utilizes a low-pass filter to extract the common-mode level [27]. The AGC loop incorporating a peak detector and an error comparator adaptively improves the linearity of intermediate stages. The DCOC network compensates for offset induced by mismatch or input imbalance. The output buffer is designed to drive external 50-\( \Omega \) loads.

3. Design Considerations

The proposed differential CB-RSF TIA is shown in Fig. 2. The noise analyses for similar structures were presented in [15, 28]. However, the former was implemented in CMOS, and the contribution of gate shot noise was not included; while the latter only focused on the contributions of the CB stage and the emitter follower. Therefore, a comprehensive analytical expression of the input-referred noise current PSD of the CB-RSF TIA is derived and investigated in detail. Assuming the CB stage operates as a current buffer with unit gain, the input-referral function for the noise contribution of the RSF part is one. As a result, the input-refferred contributions of the two parts are calculated separately; then the results are added up. The small signal equivalent circuits for noise analysis are shown in Fig. 3 and Fig. 4. The main sources that contribute to input-referred noise current include: thermal noise from load, feedback, and base resistance given by \( 4kT/R_b \); base shot noise and collector shot noise denoted as \( 2qI_C/\beta \) and \( 2qI_C \) respectively; and the drain noise generator given by \( 4kTg_m \) from the biasing current source. The input-refferred contribution of the CB stage is given by [7]

\[
i_{n,\text{in,CB}}^2(\omega) = 4kTg_mM_B + \frac{4kT}{R_1} + \frac{2qI_C}{\beta_1} + 2qI_C + 4kTg_mC_1^2\omega^2;
\]

where the drain noise current of \( M_B \) and the base shot noise current of \( Q_1 \) contribute directly to the input-referred noise. \( C_T \) is the total input capacitance including transistor parasitics (\( C_{PD}, C_{PAD}, C_{EESD}, C_{sdB}, C_{sbB}, \) and \( C_{be1} \)), while \( C_1 \) is the input capacitance excluding \( C_{be1} \).

In Fig. 4, the feedback resistance thermal noise current...
contributes directly to the input-referred noise, while input-referral functions are needed to get the input-referred contributions of remaining sources. The input-referral function is obtained by calculating the transfer function from a certain noise current to the output of the TIA and dividing that by the transfer function of the TIA [29]. The input-referral functions of the noise sources from $Q_2$ and $Q_3$ are presented as follows

$$H_{B2}^{-1}(\omega) = 1 - \frac{1}{\frac{1}{R_l} + s(C_A + C_{be2})} \approx 1 - \frac{s(C_A + C_{be2})}{g_{m2} + sC_{be2}},$$

$$H_{C2}^{-1}(\omega) = \frac{1}{\frac{1}{R_l} + s(C_A + C_{be2})} \approx \frac{1}{\frac{1}{R_l} + s(C_A + C_{be2})},$$

$$H_{R2b}^{-1}(\omega) = \frac{R_{b2}}{R_l} + sR_{b2}C_{CB},$$

$$H_{B3}^{-1}(\omega) = H_{C2}^{-1}(\omega),$$

$$H_{C3}^{-1}(\omega) = \left[ \frac{1}{\frac{1}{R_l} + s(C_A + C_{be2})} \right] \frac{s(C_{B2} + C_{be3})}{g_{m3} + sC_{be2}},$$

$$H_{R3b}^{-1}(\omega) = \left[ \frac{R_{b3}}{R_l} + sR_{b3}(C_A + C_{be2}) \right] \frac{sC_{B2}}{g_{m2} + sC_{be2}} + \frac{R_{b3}}{R_l} + sR_{b3}C_{A} \approx \frac{R_{b3}}{R_l} + sR_{b3}C_{A} + \frac{sR_{b3}C_{B2}}{g_{m2}R_{l}},$$

where base resistance is neglected except for calculating the input referral-functions of $l_{n,Rb2}$ and $l_{n,Rb3}$. $C_A$ is the total parasitic capacitance at node $A$ incorporating $C_{cs1}$, $C_{be1}$, and $C_{be2}$; while $C_{CB}$ is contributed by the CB stage only. $C_{B2}$ is contributed by the emitter follower bias. $C_{bc4}$ and $C_{cs4}$ are included in the load capacitance $C_{L}$. With expressions above, the input-referred noise current PSD of the RSF part is given by

$$I_{n,RSF}^2(\omega) = \frac{4kT}{R_l} + \frac{4qI_{c2}}{\beta_2} + \frac{2qI_{c2}}{g_{m2}^2} (C_A + C_{be2})^2 \omega^2 + 4kTR_{b2}C_{A,CB}^2 \omega^2 + \frac{2qI_{c3}}{g_{m2}^2} (C_A + C_{be2})^2 \omega^2 + \frac{4qI_{c3}}{g_{m3}} C_A^2 \omega^2 + 4kTR_{b3}C_{A}^2 \omega^2,$$

where the $f^2$ noise due to the base current of $Q_2$ is negligible compared to that due to the collector current of $Q_2$; and the $f^2$ noise due to the second terms in Eq. (6) and Eq. (7) dominates that due to the third terms in both equations. Given $(g_{m}R_{t})^2 \gg \beta$, and $R_{l} \gg R_{b}$, the white noise due to the collector current and base resistance of $Q_2$, and the white noise from $Q_3$ are also omitted.

Finally, the total input-referred noise current PSD is the sum of Eq. (1) and Eq. (8), which is shown as

$$I_{n,TIA}^2(\omega) = \frac{4kT}{g_{m,Mn}} + \frac{4kT}{R_l} + \frac{4kT}{R_l} + \frac{2qI_{c1}}{\beta_1}$$

$$+ \frac{2qI_{c2}}{\beta_2} + \frac{4kTR_{b1}C_A^2}{g_{m1}^2} \omega^2 + \frac{2qI_{c2}}{\beta_2} + \frac{(C_A + C_{be2})^2}{g_{m2}^2} \omega^2$$

$$+ \frac{4kTR_{b2}C_{A,CB}^2}{g_{m2}} + \frac{2qI_{c3}}{g_{m2}} (C_A + C_{be2})^2 \omega^2$$

$$+ \frac{2qI_{c3}}{g_{m3}} C_A^2 \omega^2 + 4kTR_{b3}C_{A}^2 \omega^2.$$

To reduce the Ogawa’s noise factor $\Gamma$ of $M_B$, a channel length of 500 $\mu$m is chosen, and large overdrive voltage is avoided [30]. Large resistance is desirable to minimize the thermal noise from $R_l$ and $R_1$. HBTs are biased at the optimum noise current density. Consequently, the collector and base currents, transconductance, and parasitic capacitance are in proportion with the emitter length $L_e$, while the base resistance changes inversely with $L_e$. The collector shot noise of $Q_1$ can be reduced when $C_{be1}$ is equal to $C_1$. Similarly, the optimum collector shot noise of $Q_2$ is achieved as $C_{be2} + C_{be3}$ equals $C_{cs1} + C_{be1}$. Taking account of the base shot noise makes the optimum size smaller, while taking account of the base resistance thermal noise makes the optimum size larger. Additionally, small $Q_1$ and $Q_2$ are beneficial to achieve large $R_l$ and $R_1$, and to reduce the collector shot noise and base resistance thermal noise of $Q_1$ as well. The $f^2$ noise due to the base current of $Q_3$ is insignificant compared to that due to the collector current of $Q_2$. Moreover, the collector shot noise and base resistance thermal noise push $Q_3$ to a large size, which is contrary to the case of the base shot noise. The features of Eq. (9) are used as guidance for noise optimization. Finally, large resistances of 700 $\Omega$ and 1500 $\Omega$ are chosen for $R_l$ and $R_1$. The emitter lengths of $Q_1$, $Q_2$, and $Q_3$ are $6 \mu$m, 5 $\mu$m, and 10 $\mu$m, respectively.

The VGA stage shown in Fig. 5 is modified from [16],

![Fig. 5. The schematic of the VGA stage.](image-url)
Degeneration alleviates the Miller effect and improves the linearity. Besides, the removal of peaking inductors is conducive to save chip area. In the proposed design, the maximum transimpedance gain is 74 dBΩ. And the desired differential output swing is set to 500 mV. Accordingly, for current swing larger than 100 μA_pp, the transimpedance gain decreases owing to the adjustment of the AGC [16, 31] loop.

4. Experimental Results

Implemented in 0.13-μm SiGe BiCMOS technology, the die photo of the chip is shown in Fig. 6, where no peaking inductors are used. A whole area of 0.9×0.6 mm² and a core area of 0.6×0.3 mm² are achieved respectively. The core power dissipation is 300 mW.

The frequency domain characteristics are measured by a Keysight’s N5245A PNA-X network analyzer. The S-parameter measurements are done in the 4-port single-ended mode. Moreover, the gain control voltage is adjusted manually to get the performance of the VGA. The simulated and measured single-ended S-parameters are shown in Fig. 7. The measured transimpedance $Z_t$ is obtained as [7]

$$Z_t = Z_0 \frac{S_{21}}{1 - S_{11}}, \quad (10)$$

where $Z_0$ is 50 Ω. The simulated and measured transimpedance is shown in Fig. 8. The simulated results indicate a bandwidth of about 33 GHz, and the measured bandwidth is about 31 GHz. The measured minimum and maximum transimpedance are 46 dBΩ and 71 dBΩ, respectively.

The time domain and noise measurements are performed by a Keysight’s 86100D DCA-X oscilloscope. PRBS data patterns up to 56-Gb/s are applied in transient simulations (see Fig. 9 and Fig. 10), while the maximum data rate available in the lab is 42 Gb/s. The single-ended eye diagrams corresponding to 350-μA_pp and 1.8-mA_pp inputs of 42-Gb/s PRBS31 patterns are shown in Fig. 11 and Fig. 12. The single-ended output swing is about 230 mV.

The noise specifications are derived based on the measurements by using the histogram function of the oscilloscope. With the transimpedance set to the maximum and input signal disabled, the single-ended integrated output noise including noise from the oscilloscope itself is shown in Fig. 13.
The total integrated input-referred noise current is calculated as [16, 23]

$$I_{n,\text{tot}} = \frac{2\sqrt{4.59^2 - 0.64^2} \cdot mV_{\text{rms}}}{3548 \Omega} = 2.56 \mu A_{\text{rms}},$$  \hspace{1cm} (11)$$

where the noise from the oscilloscope (0.64 mV_{\text{rms}}) is subtracted. The average input-referred noise current density [16, 23] is

$$I_{n,\text{avg}} = \frac{I_{n,\text{tot}}}{\sqrt{BW}} = 14.54 \text{ pA}/\sqrt{\text{Hz}},$$  \hspace{1cm} (12)$$

while the simulated input-referred noise current density is shown in Fig. 14.

The performance comparison with prior works is summarized in Table I. In all the listed works, the proposed chip demonstrates the second lowest noise level of 14.54 pA/\sqrt{\text{Hz}} and the third highest transimpedance of 71 dBΩ. Additionally, the chip occupies relatively small area compared with works implemented in SiGe processes. Peaking inductors are employed in [4, 5, 6, 11, 17, 24, 25, 26] to extend bandwidth. Apart from that, technologies in [4, 5] are faster than that of the proposed work. By adopting post-amplifier equalization technique, [5] achieves the lowest noise level. However, the dependence of bandwidth and stability on input capacitance still exists.

### 5. Conclusion

A low-noise 71-dBΩ transimpedance optical RX with 31-GHz bandwidth is successfully fabricated and verified in 0.13-μm SiGe BiCMOS. The differential CB-RSF TIA offers isolation to input capacitance and high transimpedance limit. Specifically, a comprehensive analytical expression of the input-referred noise current PSD of the CB-RSF TIA is derived and investigated. The features of the expression provide insights for noise optimization. Additionally, the linearity of intermediate stages is improved by a modified

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**Table I. Performance comparison**

| Ref. | Tech. | PD (fF) | BW (GHz) | TI (dBΩ) | Noise (pA/√Hz) | Area (mm²) |
|------|-------|---------|----------|-----------|----------------|------------|
| [3]  | 0.13-μm SiGe | N/A | 38.4 | 72* | 14.8 | 2.08* |
| [4]  | 55-nm SiGe | N/A | 92 | - | 17.7 | 0.14 |
| [5]  | 0.13-μm SiGe:C | N/A | 66 | 65* | 7.6 | 0.42 |
| [6]  | 0.18-μm SiGe | N/A | 35 | 70* | 30.46 | 3.12 |
| [11] | 65-nm CMOS | 50 | 50 | 52* | 22.42 | 0.96 |
| [17] | 45-nm SOI CMOS | 100 | 30 | 55** | 20.47 | 0.29 |
| [18] | 65-nm CMOS | 100 | 29.6 | 79* | 53.5 | 0.05** |
| [23] | 0.13-μm SiGe | 300 | 28 | 53.6* | 36.5 | 0.56 |
| [24] | 0.13-μm SiGe | N/A | 86 | 55** | 20.4 | 0.28 |
| [25] | 0.25-μm SiGe:C | N/A | 49 | 49** | 16.3 | 0.8 |
| [26] | 0.13-μm SiGe | 100 | 50 | 41** | 39.8 | 0.58 |
| This work | 0.13-μm SiGe | N/A | 31 | 71* | 14.54 | 0.54 |

*: differential transimpedance, **: single-ended transimpedance, +: 4 channels, ++: core area.
VGA operating with an AGC loop. The experimental results indicate that the traditional trade-offs among bandwidth, transimpedance, and noise level are effectively tackled.

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References

[1] Cisco Systems: Cisco global cloud index – forecast and methodology, 2016-2021 whitepaper (2018) http://www.cisco.com.
[2] S. P. Voinigescu, et al.: “Silicon millimeter-wave, terahertz, and high-speed fiber-optic device and benchmark circuit scaling through the 2030 ITRS horizon,” IEEE Proc. 105 (2017) 1087 (DOI: 10.1109/JPROC.2017.2672721).
[3] K. Honda, et al.: “A 56-Gb/s transimpedance amplifier in 0.13-μm SiGe BiCMOS for an optical receiver with -18.8-dBm input sensitivity,” Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (2016) 1 (DOI: 10.1109/CSSC.2016.7751018).
[4] K. Vasilakopoulos, et al.: “A 92GHz bandwidth SiGe BiCMOS HBT TIA with less than 6dB noise figure,” Proc. IEEE Bipolar/BiCMOS Circuits Tech. Meet. (2015) 168 (DOI: 10.1109/BCTM.2015.7340554).
[5] I. G. López, et al.: “100 Gb/s differential linear TIAs with less than 10 pA/√Hz in 130-nm SiGe:C BiCMOS,” IEEE J. Solid-State Circuits 53 (2018) 458 (DOI: 10.1109/JSSC.2017.2733521).
[6] T. Takemoto, et al.: “A 50-Gb/s high-sensitivity (-9.2 dBm) low-power (7.9 pJ/bit) optical receiver based on 0.18-μm SiGe BiCMOS technology,” IEEE J. Solid-State Circuits 53 (2018) 1518 (DOI: 10.1109/JSSC.2018.2791474).
[7] E. Säckinger: Analysis and Design of Transimpedance Amplifiers for Optical Receivers (Wiley, New Jersey, 2017) 213-251, 285, 301-312.
[8] S. Voinigescu: High-Frequency Integrated Circuits (Cambridge University Press, New York, 2013) 513-514.
[9] E. Säckinger: “The transimpedance limit,” IEEE Trans. Circuits and Syst. I 57 (2010) 1848 (DOI: 10.1109/TCSI.2009.2037847).
[10] B. Analui, and A. Hajimiri: “Bandwidth enhancement for transimpedance amplifiers,” IEEE J. Solid-State Circuits 39 (2004) 1263 (DOI: 10.1109/JSSC.2004.831783).
[11] S. G. Kim, et al.: “A 50-Gb/s differential transimpedance amplifier in 65nm CMOS technology,” Proc. IEEE Asian Solid-State Circuits Conf. (2014) 357 (DOI: 10.1109/ASSCC.2014.7098934).
[12] D. Li, et al.: “A low-noise design technique for high-speed CMOS optical receivers,” IEEE J. Solid-State Circuits 49 (2014) 1437 (DOI: 10.1109/JSSC.2014.2322868).
[13] C. Schow, et al.: “A low-power 20-GHz 52-dBΩ transimpedance amplifier in 80-nm CMOS,” IEEE J. Solid-State Circuits 39 (2004) 885 (DOI: 10.1109/JSSC.2004.827807).
[14] C. L. Schow, et al.: “Low-power 16 × 10 Gb/s bi-directional single chip CMOS optical transceivers operating at < 5mW/Gb/s/link,” IEEE J. Solid-State Circuits 44 (2009) 301 (DOI: 10.1109/JSSC.2008.2007439).
[15] S. M. Park, and H. J. Yoo: “1.25-Gb/s regulated cascode CMOS transimpedance amplifier for Gigabit Ethernet applications,” IEEE J. Solid-State Circuits 39 (2004) 112 (DOI: 10.1109/JSSC.2003.820884).
[16] C. Liao, and S. Liu: “40 Gb/s transimpedance-AGC amplifier and CDR circuit for broadband data receivers in 90 nm CMOS,” IEEE J. Solid-State Circuits 43 (2008) 642 (DOI: 10.1109/JSSC.2007.916626).
[17] J. Kim, and J. F. Buckwalter: “A 40-Gb/s optical transceiver front-end in 45 nm SOI CMOS,” IEEE J. Solid-State Circuits 47 (2012) 615 (DOI: 10.1109/JSSC.2011.2178723).
[18] K. Park, and W. Oh: “A 40-Gb/s 310-Gb/s inverter-based CMOS optical receiver front-end,” IEEE Photonics Tech. Lett. 27 (2015) 1931 (DOI: 10.1109/LPT.2015.2447283).
[19] I. Oszkaya, et al.: “A 64-Gb/s 1.4-pJ/lnZ optical receiver data-path in 14-nm CMOS FinFET,” IEEE J. Solid-State Circuits 52 (2017) 3458 (DOI: 10.1109/JSSC.2017.2734913).
[20] T. L. Nguyen, et al.: “SiGe BiCMOS technologies for high-speed and high-volume optical interconnection applications,” Proc. IEEE Bipolar/BiCMOS Circuits Tech. Meet. (2016) 1 (DOI: 10.1109/BCTM.2016.7738971).
[21] C. Li, and S. Palermo: “A low-power 26-GHz transformer-based regulated cascode SiGe BiCMOS transimpedance amplifier,” IEEE J. Solid-State Circuits 48 (2013) 1264 (DOI: 10.1109/JSSC.2013.2245059).
[22] B. Moeneclaey, et al.: “A 40-Gb/s transimpedance amplifier for optical links,” IEEE Photonics Tech. Lett. 27 (2015) 1375 (DOI: 10.1109/LPT.2015.2421521).
[23] S. B. Amid, et al.: “Fully differential, 40 Gb/s regulated cascode transimpedance amplifier in 0.13 μm SiGe BiCMOS technology,” Proc. IEEE Bipolar/BiCMOS Circuits Tech. Meet. (2010) 33 (DOI: 10.1109/BCTM.2010.5667977).
[24] R. Ding, et al.: “Power-efficient low-noise 86 GHz broadband amplifier in 130 nm SiGe BiCMOS,” Electron. Lett. 50 (2014) 741 (DOI: 10.1049/el.2014.0367).
[25] M. H. Eissa, et al.: “A wideband monolithically integrated photonic receiver in 0.25-μm SiGe:C BiCMOS technology,” Proc. European Solid-State Circuits Conf. (2016) 487 (DOI: 10.1109/ESSCIRC.2016.7598347).
[26] A. Karimi-Bidhendi, et al.: “A silicon-based low-power broadband transimpedance amplifier,” IEEE Trans. Circuits and Syst. 1 65 (2018) 498 (DOI: 10.1109/TCSII.2017.2733521).
[27] B. Razavi: Design of Integrated Circuits for Optical Communications (Wiley, New Jersey, 2012) 2nd ed. 101.
[28] T. Vanisri, and C. Toumazou: “Integrated high frequency low-noise current-mode optical transimpedance preamplifiers – theory and practice,” IEEE J. Solid-State Circuits 30 (1995) 677 (DOI: 10.1109/4.387071).
[29] T. C. Caruso, et al.: Analog Integrated Circuit Design (Wiley, New Jersey, 2011) 2nd ed. 395-397.
[30] E. Säckinger: “On the excess noise factor Γ of a FET driven by a capacitive source,” IEEE Trans. Circuits and Syst. I 58 (2011) 2118 (DOI: 10.1109/TCSI.2011.2112870).
[31] D. Kucharski, and K. T. Kornegay: “Jitter considerations in the design of a 10-Gb/s automatic gain control amplifier,” IEEE Trans. MW Theory and Techniques 53 (2005) 590 (DOI: 10.1109/TMTT.2004.840731).