Hardware Design and Implementation of Image Processing System Based on FPGA

Dongmei Zhao¹*, Bo Zhou¹, Yang Song¹, Ling Li¹

¹Basic Department of Dalian Naval Academy, Dalian, Liaoning, China
*Corresponding author's e-mail: zhaodongmei871201@126.com

Abstract. Discussed the hardware design and implementation of the image processing system with Virtex-XC5VSX95T as the algorithm processing chip. The large-capacity data storage chip XCF128X is selected to store the program flow. The user clock, DDR2 clock, SATA clock and other clock modules are designed. Designed LVDS and SATA as a high-speed data interface for image data transmission. Designed RS-422 as a communication interface for parameter, command and status data transmission. DDR2 memory modules and NAND Flash are as memory for image data caching. Dedicated voltage regulator chip is selected to meet the requirements of each module of the system for DC voltage. The test proves that the hardware design of the image processing system is correct and can realize the expected function.

1. Introduction
In recent years, with the development of computers, various hardware development platforms, and data storage, transmission and display technologies, image processing has become more and more widely used in life, engineering, military and other fields, people’s requirements for image processing technology have become higher and higher [1]. The computer has friendly interface and convenient operation, the FPGA has fast processing speed and flexible design, the image processing system composed of the upper computer (computer-based) and the lower computer (FPGA-based) has the advantages of good human-computer interaction and fast signal processing speed [2]. The working procedure is: the upper computer sends the set parameters and commands, the FPGA-based lower computer receives the image data provided by the image acquisition unit, and performs algorithmic processing on it, the lower computer uploads the image processing state to the upper computer in time, finally, the later image data and algorithm results are sent back to the upper computer for display and storage.

This article mainly introduces the hardware design of the lower computer with FPGA as the core, including the overall scheme, FPGA chip selection, program configuration scheme, clock scheme, data transmission and communication interface design, storage scheme and power module design.

2. Overall hardware design
The hardware structure diagram of the FPGA-based image processing system is shown in Figure 1. FPGA is the core device, equipped with program storage chip and clock generation unit. Design LVDS, SATA and other data transmission interfaces, responsible for receiving and sending image data; RS-422 is used for communication interface. Two storage solutions, DDR2 SODIMM and NAND Flash, are adopted. Considering the scalability of the image processing system, it is equipped with modules such as expansion slots, DIP switches, buttons, and LED displays. According to system requirements, multiple voltage regulator chips are used to provide the DC stable voltage required by different modules.
3. FPGA chip selection

The image processing system focuses on the algorithmic processing of image data. In addition to the high-performance logic resources, the FPGA of Xilinx's Virtex-5-SXT series also contains internal IP core modules and embedded core processors, which have powerful computing functions, the series are especially suitable for the field of digital signal processing. This system chooses XC5VSX95T model, its maximum user I/O number is 640, its clock management module number is 6, the maximum distributed RAM module is 1520Kb, its DSP48E slices number is 640, the chip resource can meet the system demand, cost-effective.

4. Configuration scheme and design of clock module

4.1 Configuration scheme

Program configuration is a key step in FPGA development. Choose Xilinx's dedicated high-density configuration memory Platform Flash XL XCF128X, which has a large capacity of 128Mb, its configuration rate is up to 800Mbps, the memory unit supports eight configuration modes such as Master Serial and Slave Serial. In order to achieve a good configuration effect, the Slave SelectMAP configuration mode should be selected. Assign the FPGA Bank0, Bank1, Bank2 and Bank4 to the configuration circuit, using 3.3V power supply, part of the circuit schematic diagram shown in Figure 2.

Figure 1. Block diagram of the hardware structure of the FPGA-based image processing system
4.2 Clock module

The clock module of the image processing system includes 100MHz user clock, FPGA clock, DDR2 clock, SATA clock and so on, FPGA Bank3 is distributed to the clock module.

The user clock uses a 100MHz crystal oscillator, the 3.3V power supply is filtered by an inductor and a capacitor, and then connected to the power terminal and the enable terminal.

Use Integrated Circuit Systems's low voltage positive emitter-coupled logic Frequency Synthesizer ICS843001_21 and Low Skew 1-to-4 Differential-to-LVDS Fanout Buffer ICS8543I to generate FPGA clock signals and DDR2 clock signals.

Provided crystal oscillators with three frequencies of 25.5625MHz, 19.44MHz and 25MHz for the ICS843001_21 chip. The DIP switch connects the pins of SEL1~SEL0, which clock to be used as the reference clock is selected by the switch. Pins M2~M1 and N2~N0 are also connected to DIP switches, the level of the pins controls the frequency division and multiplication coefficients, the desired output frequency can be obtained. The output level of ICS843001_21 is LVPECL, connect it to the PCLK and nPCLK pins of the clock buffer chip ICS8543I. Configure the OE, CLK_SEL and CLK_EN pins to be high, the FPGA clock and DDR2 clock can be output from the Q0, nQ0 and Q1, nQ1 terminals, its circuit schematic diagram is shown as in Figure 3.
oscillator frequency is 25MHz, the chips are powered by 3.3V. Its circuit schematic diagram is shown in Figure 4.

![Figure 4. SATA Clock Circuit Schematic](image)

5. Design of data transmission and communication interface

5.1 Data transmission interface

In order to meet the huge data transmission needs, this system is equipped with LVDS and SATA interfaces.

LVDS is a low-voltage differential signal technology, which has simple terminal adaptation, low power consumption, fast transmission speed, and strong reliability \(^3\). This system needs to transmit 64 channels of image data signals and 3 channels of data synchronization signals, so for the receiving end, select 4 pieces of Texas Instruments's 16-channel high-speed differential receiver SN65LVDS386 and 1 piece of 4-channel high-speed differential receiver SN65LVDS390; for the transmitting end, use 4 pieces of Texas Instruments's 16-channel high-speed differential driver SN65LVDS387 and 1 piece of 4-channel high-speed differential driver SN65LVDS391. The four chips all use 3.3V power supply. The Bank5 and Bank6 pins of the FPGA are allocated to the LVDS receiving end, and the Bank23 and Bank25 pins are allocated to the LVDS transmitting end.

The Serial Advanced Technology Attachment interface has fast transmission rate, low power consumption, supports hot plugging, and has a simple structure \(^4\). It consists of only 7 wires, of which 3 are ground wires and the remaining 4 are two pairs of differential signal wires. This system designs 4 pairs of SATA interfaces, and allocates Bank5 pins of FPGA to SATA interfaces.

5.2 Communication interface

The communication between the image processing system and the computer adopts the RS-422 interface. The RS-422 interface has fast transmission speed and stable performance. In order to realize full-duplex communication, it needs to two channels of sending and receiving. Since the interface is in a differential form, each channel occupies two signal lines. The full-duplex RS-422 communication chip MAX3490 from Maxim Integrated is selected, and the power supply voltage is 3.3V, and some pins of FPGA Bank11 are allocated to RS-422 interface.

6. Storage module design

In order to provide a cache area for image processing algorithms of large-capacity data, this system is equipped with DDR2 Synchronous Dynamic Random Access Memory and NAND Flash Memory.

6.1 DDR2 Small Outline Dual In-line Memory Modules

DDR2 has high data transmission rate, large storage capacity, and low power consumption. The Virtex-5 series FPGA contains a dedicated IP core, which can easily and quickly realize the control of DDR2\(^5\). In order to facilitate disassembly and replacement, this system uses Micron Technology's 256MB DDR2 SODIMM MT4HTF3264HY, allocates Bank15, Bank17, Bank19, and Bank21 pins of FPGA to DDR2. The working voltage of DDR2 is 1.8V, in order to achieve impedance matching, a 50-ohm reference resistor needs to be connected to the VRN and VRP pins.
6.2 NAND Flash Memory
NAND Flash memory has the advantages of large capacity, low power consumption, and fast rewriting speed \[6\], which is very suitable for storing image data. This system chooses Micron Technology’s MT29F8G08 chip, the data capacity is 8Gbit, the data width is 8bit, some pins of FPGA Bank11 are allocated to NAND Flash, the circuit schematic diagram is shown as in Figure 5.

![NAND Flash Circuit Schematic](image)

Figure 5. NAND Flash Circuit Schematic

7. Power module design
The voltage required for the operation of the FPGA chip includes the core voltage, port voltage and auxiliary voltage, which are 1.0V, 3.3V and 2.5V respectively. The configuration data storage chip requires 3.3V and 1.8V supply voltage, the clock module requires 3.3V supply voltage, LVDS receiving and driving chips need 3.3V voltage, RS-422 interface circuit needs 3.3V voltage, DDR2 needs 1.8V power supply voltage and 0.9V reference voltage, Flash chip power supply voltage is 3.3V. In summary, this image processing system needs 5 kinds of stable voltages.

The system is powered by a 5V DC stabilized power supply and adopts Texas Instruments's dedicated stabilized power supply chip PTH08T240W to design the power supply scheme, which can meet four stable voltage outputs of 3.3V, 2.5V, 1.8V, and 1.0V. PTH08T240W can work in a wide input voltage range of 4.5V to 14V. Different voltage outputs can be obtained by changing the resistance of the resistor RSET. The output voltage range is 0.69V to 5.5V. According to the data manual, when RSET is 1.21kΩ, 2.38kΩ, 4.78kΩ, and 20.8kΩ, the output voltage is 3.3V, 2.5V, 1.8V, 1.0V, which can meet the voltage requirements of system configuration, clock, data transmission, storage modules. Take the output voltage of 3.3V as an example, the circuit diagram is shown in Figure 6.

![3.3V Power Supply Circuit Schematic](image)

Figure 6. 3.3V Power Supply Circuit Schematic

Select Texas Instruments's dedicated DDR power supply regulator chip TPS51100DGQ, its input voltage range is 4.75V ~ 5.25V, the input voltage range of VLDOIN is 1.2V ~ 3.6V, it can output the
voltage of VLDOIN/2. Set the VLDOIN voltage value to 1.8V to get a DDR2 reference voltage of 0.9V. The circuit schematic is shown in Figure 7.

![Figure 7. 0.9V Power Supply Circuit Schematic](image)

8. Conclusions
The physical picture of the circuit board of the FPGA-based image processing system is shown in Figure 8. Firstly, design a simple running light program and download it to the chip, run successfully, and verify the correctness of the FPGA main chip, configuration data storage chip, clock module, power module, and expansion modules. Then, design the DDR2 read and write program, under the control of the upper computer, receiving the image data provided by the image acquisition unit through the LVDS interface, store it in the DDR2, and read the data after simple algorithm processing, finally output the data through the LVDS interface. The same idea is to test NAND Flash and SATA interfaces to verify the correctness of data transmission and communication interfaces and storage modules. The test proves that the design of the image processing system is correct, laying a solid hardware foundation for the realization of the next image processing algorithm.

![Figure 8. Circuit Board of the FPGA-based Image Processing System](image)

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