Determination of the Gate Breakdown Mechanisms in p-GaN Gate HEMTs by Multiple-Gate-Sweep Measurements

Guangnan Zhou*, Fanming Zeng, Yang Jiang, Qing Wang*, Lingli Jiang, Guangrui Xia, and Hongyu Yu*

Abstract—In this work, we studied the gate breakdown (BD) mechanisms of p-GaN gate AlGaN/GaN HEMTs by a novel multiple-gate-sweep-based method. For the first time, three different BD mechanisms were observed and identified separately in the same devices: the metal/p-GaN junction BD, the p-GaN/AlGaN/GaN junction BD, and the passivation-related BD. This method is an effective method to determine the BD mechanisms. The different BD mechanisms were further confirmed by scanning electron microscopy (SEM). Finally, the temperature dependences of the three BD mechanisms were measured and compared. This analysis method was also employed in the devices with a different passivation material and showed its applicability.

Index Terms—Gate breakdown (BD) mechanism, passivation-related breakdown, p-GaN high electron mobility transistor (HEMT), PiN junction breakdown.

I. INTRODUCTION

GALLIUM nitride (GaN) possesses excellent physical properties, such as a high critical electric field and a high saturation velocity [1], [2], which is ideal for power switching applications. Power devices in GaN can be either lateral devices or vertical devices. For higher power (> 50 kW) applications where higher breakdown (BD) voltages (> 1.2 kV) are required, the lateral devices are less attractive both in cost and manufacturability due to large chip areas required by the breakdown voltage (BV) [3]. Meanwhile, for lower voltage (100–1200 V) applications, lateral high electron mobility transistors (HEMTs) are more mature and have demonstrated superior performance in on-resistance ($R_{on}$), BV, and operation switching frequency. Normally-off HEMTs are required to provide adequate safety conditions for switching applications [4], [5]. Among different approaches to realize enhancement mode (e-mode) operation [6]–[9], the p-GaN gate AlGaN/GaN HEMT emerged as a leading solution [10], [11].

However, due to the relative low gate BV (usually 10–12 V), the maximum gate operation voltages for p-GaN gate HEMTs are usually 5–7 V [10], [11]. The small gate voltage swing has imposed significant constraints on the gate driver design. Improving the gate BV remains a critical challenge in p-GaN gate HEMTs. However, the gate BD mechanisms are still controversial among the available reliability studies [12]–[23]. Some works have proposed that the gate BD originated from the BD of p-GaN/AlGaN/GaN junction (PiN) or the AlGaN barrier layer [12]–[16]. Meanwhile, others have ascribed that to the creation of the percolation path in the p-GaN/metal interface [17]–[19]. Especially, I. Rossetto et al. found that the peak electric field across the AlGaN would decrease with the positive gate bias, disapproving the BD of PiN or AlGaN layer [20]. Whether the PiN junction is likely to fail remains indeterminate. A method to determine the BD mechanism is still lacking, which is the motivation of this work.

This article is to propose and demonstrate a multiple-gate-sweep-based gate BD mechanism analysis approach as an effective and generic method to determine a gate BD mechanism. The multiple-gate-sweep is to induce and decouple the BDs of different device regions. For the first time, three different BD mechanisms have been decoupled and identified from the devices of the same structure: 1) the metal/p-GaN junction BD; 2) the PiN junction or AlGaN barrier BD; and 3) the passivation-related BD. The PiN junction BD has been directly observed. The BVs of the different BD mechanisms and their
equivalent circuit; (e) gate leakage characteristics of three gate sweeps

dependence on temperature and passivation technology were also investigated.

II. DEVICE STRUCTURE AND GATE BD

The p-GaN gate HEMTs were fabricated on 75-nm p-GaN/15-nm Al_{0.2}Ga_{0.8}N/0.7-nm AlN/4.5-μm GaN epitaxial structures grown on Si (111) substrates, as shown in Fig. 1(a). The p-GaN layer was doped with Mg to a concentration of \(4 \times 10^{19} \text{cm}^{-3}\). The fabrication started with p-GaN gate definition by a Cl-based plasma etch followed by N\textsuperscript+x implantation to isolate the devices. Then, Ti/Al/Ti/Au metal stack was deposited by e-beam evaporator, followed by rapid thermal annealing (RTA) at 830 °C in N\textsubscript{2} for 45 s. The sheet resistance of the 2DEG is extracted to be 610 Ω/square using the circular transmission line model (CTLM) measurements. Two SiN layers were deposited as the passivation layers by plasma-enhanced chemical vapor deposition (PECVD). A Schottky-type contact was formed between the Ti/Au and the p-GaN gate. The devices under test feature a gate width \(W_G\) of 100 μm, a gate length \(L_G\) of 5 μm, a gate–source distance \(L_{GS}\) of 3 μm, and a gate–drain distance \(L_{GD}\) of 12 μm. On-wafer characterization was performed by Keithley 4200 Analyzer using the sweep mode of “Normal” measurement speed (0.05V/step, delay time = 1 ms, measure time = 53.59 ms) with a floating substrate. Unless specified, the measurement temperature was 25 °C.

As shown in Fig. 1(b) and (c), the threshold voltage \(V_{TH}\) is extracted to be 1.8 V at \(I_D\) of 0.01 mA/mm. A high ON/OFF current ratio of \(5 \times 10^8\) and a low on-resistance \(R_{ON}\) of 13 Ω·mm have been achieved. At \(V_{GS} = 8\) V, the maximum drain current is extracted to be 290 mA/mm. The device exhibited a BV larger than 400 V, defined at the criteria of \(I_D\) reaching 1 μA/mm.

Fig. 1(d) shows the equivalent circuit of the gate and the regions below, which consists of a metal/p-GaN Schottky junction and a p-GaN/AlGaN/GaN PiN heterojunction. The Schottky junction limits \(I_G\) when \(V_G > 0\) V, while the PiN does that when \(V_G < 0\) V. Fig. 1(e) illustrates the gate leakage \((I_G-V_G)\) characteristics of a typical measurement using three consecutive gate sweeps. The device shows two abrupt \(I_G\) increases in the first and second sweeps, consistent with very recent studies [21], [22], indicating the existence of at least two different BD mechanisms. Huang et al. and He et al. have attributed the first-step BD to Schottky junction failure and second-step BD to PiN junction failure. In the following text, we will demonstrate that second-step breakdown should be ascribed to dielectric-related failure. Moreover, it is found that the PiN failure will not result in an increase of \(I_G\) in the positive bias.

III. RESULTS AND DISCUSSION

A. Metal/p-GaN Junction BD in the First Sweep

In Fig. 1, in the first sweep, \(I_G\) increases abruptly when \(V_G\) reaches 9.2 V, suggesting a hard BD of the gate. However, in the second sweep, the reverse \(I_G\) has negligible change compared with the first sweep, indicating that the PiN junction remains functional. The transfer characteristics of the HEMTs before and after the first BD are shown in Fig. 2(a). The device can still be turned OFF/ON with a high \(I_{ON}/I_{OFF}\) ratio. The “gate control” of the channel is preserved. Besides, the device shows a lower threshold voltage, a lower subthreshold swing, and a higher drain current \((I_D)\) after first-step breakdown after the first BD. These features indicate that the first BD should be attributed to the metal/p-GaN Schottky junction failure. The degradation has converted the Schottky junction into an ohmic-like gate. Fig. 2(b) compares the off-state drain leakage \((I_{DSS})\) before and after the Schottky BD, showing that the off-state leakage blocking capability of the gate-stack is maintained.

Although an HEMT cannot function as a normal switch after the first BD, the following BDs in the subsequent sweeps of the HEMTs are still worth investigating: 1) Owing to the device structure and gate technology differences, the first BD mechanism varies in the literature as in [14], [21]–[24]. Further sweeps and BDs can help to determine the first BD mechanism; and 2) To protect a switch system, it is vital to maintain the off-state blocking capability (i.e., a low \(I_{DSS}\)) of the p-GaN HEMTs after the gate BD as argued in [22].

B. Passivation-Related BD and PiN BD in the Second Sweep

As shown in Fig. 1(b), after the second BD, \(I_G\) increases significantly under both forward and reverse bias. However, either PiN junction BD or passivation-related BD may possibly
lead to this phenomenon, which makes it challenging to identify the BD mechanism. In this work, we propose a simple but effective method to determine the mechanism, which is to measure the gate–drain current ($I_{GD}$) and the gate–source current ($I_{GS}$) separately. Fig. 3(a) shows $I_G$, $I_{GD}$, and $I_{GS}$ after the second BD in the third sweep. The $I_{GS}$ component is very close to $I_{GD}$ when $V_{GS} = V_{GD} > V_{TH}$ ($\sim 1.4$ V), while $I_{GS}$ is approximately seven orders of magnitude higher than $I_{GD}$ when $V_G < V_{TH}$. This $I_{GD}/I_{GS}$ difference can be explained by the failure of the passivation on the source side. A leakage path between the G and S terminals has been created either along the passivation/p-GaN left sidewall or through the passivation in the second BD, while the PiN junction below remains intact. The “gate control” of the channel is still preserved. When $V_G < V_{TH}$, the channel under the gate is depleted; thus, $I_{GD}$ maintains at a low level. When $V_G > V_{TH}$, the channel is turned on connecting the S and D terminals, thus $I_{GD}$ is comparable with $I_{GS}$. This conclusion is confirmed by $I_{DSS}$ in Fig. 3(b). Despite the large reverse $I_G$, $I_{DSS}$ maintains at a low level after the second BD.

Furthermore, the PiN junction or AlGaN barrier BD has been successfully observed at higher temperatures thanks to the multiple-sweep measurement instead of step stress or a constant stress measurement. As illustrated in Fig. 4(a), in the second sweep at 175 °C (red), there is no typical abrupt $I_G$ increase when $V_{GS} > 0$ V as an indication of a BD. However, in the third sweep, $I_G$ increased several orders of
magnitude in the $V_{GS} < 0$ V regime without any $I_G$ increased when $V_{GS} > 0$ V. Besides, both $I_{GD}$ and $I_{GS}$ increased when $V_{GS} < 0$ V. $I_{DSS}$ also increased several orders of magnitude, as shown in Fig. 4(b). Based on these, we can infer that a PiN junction BD happened in the second sweep. Its failure will not contribute more leakage current when $V_{GS} > 0$ V. This phenomenon confirms the possibility of the PiN junction failure and reveals that this failure itself will unlikely result in the increase of $I_G$ in the positive bias regime, disapproving the deductions in previous studies [12]–[14], [20]–[22]. This feature makes it difficult to observe the PiN junction BD in a stress measurement due to the lack of a typical breakdown feature. To the best of our knowledge, this is the first report of direct observation of PiN junction failure. The physical origin PiN BD may be closely related to dislocations in GaN/AlGaN. In the literature, it is found that the dislocations in GaN diode can increase the reverse-bias leakage current significantly, whereas they have little impact on the forward-bias current [25]. This conclusion is consistent with our finding that the PiN junction BD will only increase the reverse-bias leakage current.

Meanwhile, it is also possible that the passivation-related BD and the PiN junction BD happen in the same sweep, as illustrated in Fig. 5. The features of different BD mechanisms are summarized in Table I, where the “↑” indicating an increase of the leakage current and the “-” indicating no significant change.

When a device is exposed to higher gate voltage, damages are likely to occur due to the heating effect. The cross sections of the damaged parts have been prepared by focused ion beam etching (FIB) and imaged by scanning electron microscopy (SEM), as illustrated in Fig. 6. Damages originated from the PiN junction failure are clearly shown in Fig. 6(a). Meanwhile, the PiN junction remains intact, while the passivation was severely damaged in Fig. 6(b). These observations confirmed our previous deductions that both PiN BD and passivation-related BD can happen in p-GaN gate HEMTs.

### C. Simulation and Gate BV Comparisons of the Different BD Mechanisms

The electric field across the gate region has been simulated numerically by Silvaco’s Technology Computer Aided Design (TCAD) software, as shown in Fig. 7 [26]. The considered structure is as depicted in Fig. 1(a). Incomplete ionization of magnesium acceptors has been taken into account with an ionization energy of 170 meV [27]. The results of the simulations showed that the electric field can be quite high in two regions of the device: the p-GaN footing and AlGaN/GaN interface, which are close related to the passivation-related failure and PiN junction failure, respectively.

Temperature-dependent measurements were conducted from 25 °C to 175 °C with 37.5 °C per step to get further insights into the BD mechanisms. For each temperature, at least ten devices were measured by multiple-gate-sweep. To extrapolate the BV of PiN junction failure, more than one sweep has been carried out. The maximum forward $V_G$ has been increased by 0.1 V in each sweep until the increased reverse $I_G$ was observed. The maximum $V_G$ in the last sweep was then defined as the PiN junction BV. Fig. 8(a) shows the statistical summary of the gate BVs. The sequence of the BDs depends on the measurement/operation temperature.
Schottky BD has the smallest BV, so it happens before others. At a higher temperature, PiN BD is likely to happen prior to the passivation-related BD, as shown in Fig. 4, which may not be the case for lower temperatures. The different BD mechanisms show different temperature dependence. The Schottky failure has very weak temperature dependence, while the passivation-related failure and PiN failure clearly have different temperature dependences. The Schottky junction failure has a very weak temperature dependence, while the PiN junction failure has a positive temperature dependence. For the passivation-related BD, its dependence on temperature is closely related to the passivation technology. We believe the clarification of BD mechanisms and this BD analysis method will shed more light on improving the gate BV and reliability.

IV. CONCLUSION

In this work, the gate BD mechanisms of p-GaN gate AlGaN/GaN HEMTs were studied thoroughly by the multiple-gate-sweep-based method. Three different BD mechanisms have been observed and confirmed by SEM: the metal/p-GaN Schottky junction BD, the PiN junction BD, and the passivation-related BD. By measuring $I_{GS}$ and $I_{GS}$ separately and doing $I_{DS}$ analysis, the BD mechanisms can be successfully identified. We believe this method is generally applicable to p-GaN gate HEMTs. Especially, it is demonstrated that the PiN junction failure alone does not lead to an increase of $I_{G}$ at $V_{G} > 0$ regime disapproving previous literature. Besides, it is demonstrated that the three BD mechanisms have different temperature dependences. The Schottky junction failure has a very weak temperature dependence, while the PiN junction failure has a positive temperature dependence. For the passivation-related BD, its dependence on temperature is closely related to the passivation technology. We believe the clarification of BD mechanisms and this BD analysis method will shed more light on improving the gate BV and reliability.

ACKNOWLEDGMENT

The work was conducted at SUSTech Core Research Facilities (CRF), and the authors would like to acknowledge the technical support from SUSTech CRF.

REFERENCES

[1] F. Ren and J. C. Zolper, *Wide Energy Bandgap Electronic Devices*. Singapore: World Scientific, 2003, doi: 10.1142/1713.

[2] F. Roccaforte et al., “Recent advances on dielectrics technology for SiC and GaN power devices,” *Appl. Surf. Sci.*, vol. 301, pp. 9–18, May 2014, doi: 10.1016/j.apsusc.2014.01.063.

[3] S. Chowdhury and U. K. Mishra, “Lateral and vertical transistors using the AlGaN/GaN heterostructure,” *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3060–3066, Oct. 2013, doi: 10.1109/TED.2013.2277893.

[4] M. Su, C. Chen, and S. Rajan, “Prospects for the application of GaN power devices in hybrid electric vehicle drive systems,” *Semicodr. Sci. Technol.*, vol. 28, no. 7, Jul. 2013, Art. no. 074012, doi: 10.1088/0268-1242/28/7/074012.

[5] M. J. Scott et al., “Merits of gallium nitride based power conversion,” *Semicodr. Sci. Technol.*, vol. 28, no. 7, Jul. 2013, Art. no. 074013, doi: 10.1088/0268-1242/28/7/074013.

[6] W. Choi, O. Seok, H. Ryu, H.-Y. Cha, and K.-S. Seo, “High-voltage and low-leakage-current gate recessed normally-off GaN MIS-HEMTs with dual gate insulator employing PEALD-SiN/RF-sputtered-HfO2,” *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 175–177, Feb. 2014, doi: 10.1109/LED.2013.2293579.

[7] I. Hwang et al., “P-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current,” *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 202–204, Feb. 2013, doi: 10.1109/LED.2012.2230312.
[8] W. Chen, K.-Y. Wong, and K. J. Chen, “Monolithic integration of lateral field-effect rectifier with normally-off HEMT for GaN-on-Si switch-mode power supply converters,” in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2008, pp. 1–4, doi: 10.1109/IEDM.2008.4796635.

[9] B. Lee *et al.*, “Normally-off AlGaN/GaN-on-Si MOSHFTs with TaN floating gates and ALD SiO$_2$ tunnel dielectrics,” in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2010, pp. 20.6.1–20.6.4, doi: 10.1109/IEDM.2010.5703401.

[10] GaN Systems. (2019). GS66502B 650V. [Online]. Available: https://gansystems.com/gan-transistors/gs66502b/

[11] EPC. (2019). EPC2019 200V. [Online]. Available: https://epc-co.com/epcPortals/0/epc/documents/datasheets/EPC2019_datasheet.pdf

[12] T.-L. Wu *et al.*, “Forward bias gate breakdown mechanism in enhancement-mode p-GaN gate AlGaN/GaN high-electron mobility transistors,” *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1001–1003, Oct. 2015, doi: 10.1109/LED.2015.2465137.

[13] M. Meneghini *et al.*, “Degradation of GaN-HEMTs with p-GaN gate: Dependence on temperature and on geometry,” in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, pp. 4B5.1–4B5.5, doi: 10.1109/IRPS.2017.7936311.

[14] M. Tapajna, O. Hilt, E. Bahat-Treidel, J. Würfl, and J. Kuzmik, “Gate reliability investigation in normally-off P-type-GaN Cap/AlGaN/GaN HEMTs under forward bias stress,” *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 385–388, Apr. 2016, doi: 10.1109/LED.2016.2535153.

[15] M. Ruzzarin *et al.*, “Degradation mechanisms of GaN HEMTs with P-type gate under forward gate bias overstress,” *IEEE Trans. Electron Devices*, vol. 65, no. 7, pp. 2778–2783, Jul. 2018, doi: 10.1109/TED.2018.2836460.

[16] I. Rossetto *et al.*, “Field- and current-driven degradation of GaN-based power HEMTs with p-GaN gate: Dependence on Mg-doping level,” *Microelectron. Rel.*, vols. 76–77, pp. 298–303, Sep. 2017, doi: 10.1016/j.micrel.2017.06.061.

[17] A. N. Tallarico *et al.*, “Investigation of the p-GaN gate breakdown in forward-biased GaN-based power HEMTs,” *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 99–102, Jan. 2017, doi: 10.1109/LED.2016.2631640.

[18] A. N. Tallarico *et al.*, “PBTI in GaN-HEMTs with P-type gate: Role of the aluminum content on $\Delta V_{TH}$ and underlying degradation mechanisms,” *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 38–44, Jan. 2018, doi: 10.1109/TED.2017.2769167.

[19] A. N. Tallarico, S. Stoffels, N. Posthuma, S. Decoutere, E. Sangiorgi, and C. Fiega, “Threshold voltage instability in GaN HEMTs with P-type gate: Mg doping compensation,” *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 518–521, Apr. 2019, doi: 10.1109/LED.2019.2897911.

[20] I. Rossetto *et al.*, “Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate,” *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2334–2339, Jun. 2016, doi: 10.1109/TED.2016.2553721.

[21] J. He, J. Wei, S. Yang, M. Hua, K. Zhong, and K. J. Chen, “Temperature-dependent gate degradation of p-GaN gate HEMTs under static and dynamic positive gate stress,” in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs*, May 2019, pp. 295–298, doi: 10.1109/ISPSD.2019.8757574.

[22] H. Jiang, R. Zhu, Q. Lyu, and K. M. Lau, “High-voltage p-GaN HEMTs with OFF-state blocking capability after gate breakdown,” *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 530–533, Apr. 2019, doi: 10.1109/LED.2019.2897694.

[23] R. L. Kini *et al.*, “An investigation of frequency dependent reliability and failure mechanism of p-GaN gated GaN HEMTs,” *IEEE Access*, vol. 8, pp. 137312–137321, 2020, doi: 10.1109/ACCESS.2020.3011453.

[24] M. Ge *et al.*, “Gate reliability of p-GaN gate AlGaN/GaN high electron mobility transistors,” *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 379–382, Mar. 2019, doi: 10.1109/LED.2019.2893290.

[25] P. Kozodoy *et al.*, “Electrical characterization of GaN p–n junctions with and without threading dislocations,” *Appl. Phys. Lett.*, vol. 73, no. 7, pp. 975–977, Aug. 1998, doi: 10.1063/1.122057.

[26] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel, and J. Würfl, “Normally-off AlGaN/GaN HFET with P-type Ga gate and AlGaN buffer,” in *Proc. 22nd Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, Hiroshima, Japan, Jun. 2010, pp. 347–350.

[27] L. Efthymiou, K. Murukesan, G. Longobardi, F. Udrea, A. Shibib, and K. Terrill, “Understanding the threshold voltage instability during OFF-state stress in p-GaN HEMTs,” *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 1253–1256, Aug. 2019, doi: 10.1109/LED.2019.2925776.

[28] S. Stoffels *et al.*, “Perimeter driven transport in the p-GaN gate as a limiting factor for gate reliability,” in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2019, pp. 1–10, doi: 10.1109/IRPS.2019.8720411.