Unified Virtual Oscillator Control for Grid-Forming and Grid-Following Converters

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Abstract—A unified virtual oscillator controller (uVOC) is proposed, which enables a unified analysis, design, and implementation framework for both grid-forming (GFM) and grid-following (GFL) voltage source converters (VSCs). Oscillator based GFM controllers, such as dispatchable virtual oscillator control (dVOC), offer rigorous analytical framework with enhanced synchronization, but lack effective fault handling capability which severely limits practical application. The proposed uVOC facilitates synchronization with an arbitrarily low grid voltage and fast over-current limiting; this enables effective fault ride-through unlike existing GFM controllers which typically switch to a back-up controller during fault. GFM operation with uVOC is achieved in both grid connected and islanded modes with seamless transition between the two. In GFL converters, bidirectional power flow control and DC bus voltage regulation is achieved with uVOC. No phase-locked-loop (PLL) is required for either GFL or GFM operation circumventing the synchronization issues associated with PLLs in weak grid applications. Detail small signal models for GFM and GFL operation have been developed and systematic design guidelines for controller parameters are provided. The proposed controller is validated through hardware experiments in a hybrid AC-DC microgrid.

Index Terms—unified virtual oscillator control, uVOC, oscillator based control, grid forming converter, grid following converter, weak grid, fault ride-through

I. INTRODUCTION

With the increasing penetration of distributed generation resources into the power system, coordinated control of low-inertia systems has garnered significant research efforts [1]–[3]. Grid-forming (GFM) converters (GFMC) are considered to be a key enabling technology for the future grid with reduced inertia [4]. The prevalent and most widely investigated control strategies for GFMCs have been developed based on mimicking the characteristics of synchronous machines by voltage source converters (VSCs). Droop control [5], [6], power synchronization control (PSC) [7], synchronverter [8], virtual synchronous machine (VSM/VISMA) [9], and synchronous power controller (SPC) [10] are examples of emulation based GFM control methods. Such machine emulation based methods are beneficial since they facilitate intuitive converter level design and implementation. However, it is yet to be proven and demonstrated whether machine emulation based methods provide the best solution for GFMC control in low-inertia networks. To circumvent the phasor based approximate modelling and design, a class of nonlinear time-domain GFM control methods, offering rigorous analytical framework, have been recently proposed [11]–[19]. The so-called dispatchable virtual oscillator control (dVOC), inspired by consensus in multi-agent networks, offers almost global synchronization guarantee in a network with an arbitrarily large number of converters and hence is a promising research direction for GFMC control in future grids with ultra low inertia. However, to the best of the authors’ knowledge, no compatible fault ride-through strategy has been reported for oscillator based GFMC controllers, which severely limits practical application. Moreover, fault-handling in GFM converters, even in conventional droop based VSCs, remains an open research problem till date. In a PSC based converter, a backup PLL is run for fault management; during grid faults the converter control system switches from PSC to PLL based current controlled operation [7]. In droop based GFMC converters, over-current protection may be achieved by directly limiting the reference to the inner current control loop; but this causes wind-up in the outer droop control loops which eventually leads to loss of synchronization and instability [20]. As an alternative, switching to PLL based grid-following operation during faults has been proposed in [21], [22]; dynamic virtual impedance control and adaptive droop control during faults were proposed in [23].

For effective fault ride-through, two key capabilities are required - first, synchronization with arbitrarily low grid voltage and second, fast over-current limiting (OCL). In this work, we build on the rigorous synchronization results of dVOC and propose an oscillator which enables synchronization with grid voltage of arbitrary magnitude. The ensuing controller is labeled as unified virtual oscillator controller (uVOC). In addition to fault ride-through, this form of the oscillator enables grid-following operation without a PLL. Sub-synchronous oscillations or even instability triggered by PLLs in weak grid conditions [7], [24] are well known which can be avoided leveraging the proposed controller. Fast OCL capability is achieved by introducing a series compensator cascaded with the oscillator. We develop a unified analysis, control design, and implementation framework for GFM and GFL operation which enables fault ride-through without the need for switching to a back-up controller. Furthermore, PLL-less grid synchronization in GFL converters with bi-directional power flow control and DC bus voltage regulation is achieved.

It is worth noting that oscillator based time-domain controllers are a class of emerging technology. Performance
comparison of oscillator based time-domain controllers with machine emulation based methods can be found in [25], [26], where significant distinctions in dynamic response are observed between the two despite identical steady-state droop settings. In this work, we develop the analysis and design framework for uVOC building up from the theoretical results for GFM operation developed in [16]–[19]; performance comparison with phasor-domain methods require further comprehensive study and is not within the scope of this work.

The rest of the paper is organized as follows: first, a space vector based nonlinear oscillator is described for grid synchronization in both GFL and GFM operation. Second, the overall implementation structure of uVOC including fault management, emulated virtual impedance and pre-synchronization method is introduced. Third, through steady state and small signal analysis, controller design guidelines are presented. Lastly, simulation and experimental results are presented to validate the proposed controller.

Figure 1. Simplified VSC system connected to an infinite bus through an equivalent impedance for controller development.

II. SPACE VECTOR OSCILLATOR (SVO)

The SVO serves as the synchronization unit for uVOC. For the purpose of development of the SVO, we consider a simplified VSC system, shown in Fig. 1 connected to an infinite bus $v_i = V_{pp}e^{j\omega t}$ through an equivalent impedance $Z_{eq}$; the controller implementation in a real VSC is presented in Section III. Taking average over a switching period, the switch network can be approximated as a unity-gain block, i.e., $v_a \approx v$; here, the three-phase voltage $[v_a \ v_b \ v_c]^T$ is represented as a space vector $v = v_a + jv_b \leftrightarrow [v_\alpha \ v_\beta]^T$ in the stationary $\alpha\beta$-reference frame, where $j = \sqrt{-1}$ denotes the imaginary unit. Similar space vector notation is followed in the discussion that follows. The problem statement can be defined as to determine a dynamic control law on the converter output voltage vector $v$ which enables synchronization in GFL and GFM converters.

Prior to delving into the development of the SVO, we present a brief review of the time-derivative of the voltage vector. The voltage vector $v = V_p(t)e^{j\theta(t)} = V_p(t)e^{j\omega(t)t}$, shown in Fig. 2 is defined by the instantaneous vector magnitude $V_p(t)$ and the instantaneous angle $\theta(t)$. The rate of change of $V_p(t)$ and the instantaneous speed $\omega(t)$ can be derived from the time derivative of the space vector as

$$\frac{d}{dt}(v) = [j\omega + \frac{1}{V_p} \frac{d}{dt}(V_p)]v = \Omega v.$$  

Here, $(t)$ is dropped from all instantaneous variables in the interest of space and this omission will be followed henceforth. It is worth noting that the imaginary part of $\Omega$ denotes the instantaneous speed of rotation, and the real part denotes the normalized rate of change of vector magnitude. We consider a synchronous reference frame aligned with $v$. The real part Re($\Omega t$) and imaginary part Im($\Omega t$) of the time-derivative are exerted on the original vector $v$ along the $d$ and $q$ axes, respectively.

Figure 2. The real and imaginary parts of the time-derivative are exerted along the $d$ and $q$ axes on the original space-vector, respectively.

A. Grid Following (GFL) Operation

We consider a control law on the converter output voltage vector given as

$$\frac{d}{dt}(v) = j\omega_0 v + \eta (i_0 - i)e^{j\phi},$$  

where, $\omega_0$ denotes the nominal frequency and $\eta > 0$ is a design parameter; $\phi$ is another design parameter to rotate the current error $e_t = (i_0 - i)$ for a desired droop relation. The current reference $i_0 = i_{\alpha 0} + j i_{\beta 0} \leftrightarrow i_0 = [i_{\alpha 0} \ i_{\beta 0}]^T$ is obtained using instantaneous power theory [27] as

$$[i_{\alpha 0} \ i_{\beta 0}] = \frac{2}{N} \frac{1}{V_p^2} \left[ v_\alpha \ v_\beta \ v_\beta \ -v_\alpha \right] \left[ \begin{array}{c} P_0 \\ Q_0 \end{array} \right],$$  

where, $V_p^2 = v_\alpha^2 + v_\beta^2$; $P_0$ and $Q_0$ denote the real and reactive power set-points/references, respectively and $N$ denotes the number of phases, i.e., $N = 1$ and $N = 3$ for single and three phase systems, respectively.

Next, we illustrate the principle of operation of (2). The first term $j\omega_0 v$ corresponding to the harmonic oscillator, is applied along the $q$-axis and without the synchronization feedback term, (2) reduces to a simple harmonic oscillator of dimension 2 which results in a voltage vector rotating at $\omega_0$ rad/s with arbitrary magnitude. The synchronization feedback term realigns the voltage vector and adjusts the vector magnitude to track the real and reactive power references. The instantaneous real and reactive power outputs are given as

$$\left[ \begin{array}{c} P \\ Q \end{array} \right] = \left( \begin{array}{c} \frac{N}{2} \\ \frac{N}{2} \end{array} \right) \left[ \begin{array}{c} v_\alpha \\ v_\beta \ -v_\alpha \end{array} \right] \left[ \begin{array}{c} i_{\alpha} \\ i_\beta \end{array} \right].$$  

Using (2) and (4), the current error can be obtained as

$$e_t = \left( \frac{2}{N V_p^2} e_P \right) v + j \left( \frac{-2}{N V_p^2} e_Q \right) v = (e_P + j e_Q)v,$$

where, $e_P = P_0 - P$ and $e_Q = Q_0 - Q$. Evidently, $e_t$ can be decomposed into two components- a $d$-component $e_{i_P}v$ which corresponds to the error in real power tracking and a $q$-component $j e_{i_Q}v$ corresponding to the error in reactive power.
Comparing (1) and (6), the dynamics of the instantaneous frequency and voltage vector magnitude can be obtained as

$$\frac{d}{dt}(v) = [j(\omega_0 + \eta_e i_P) - \eta_e i_Q] v. \tag{6}$$

Comparing (1) and (6), the dynamics of the instantaneous frequency and voltage vector magnitude can be obtained as

$$\frac{d}{dt}(V_p) = -\eta V_p e_i Q, \quad \text{along } d\text{-axis;} \tag{7}$$

$$\omega = \omega_0 + \eta_e i_P, \quad \text{along } q\text{-axis.}$$

The oscillator voltage vector magnitude is adjusted until equilibrium is reached along the $d$-axis as $e_{iQ} = 0 \iff Q_0 = Q$. However, frequency is a network-wide parameter and consequently, along the $q$-axis, a droop response is observed in the real power output as

$$\omega = \omega_0 + \frac{2\eta}{N V_p^2} (P_0 - P). \tag{8}$$

The converter cannot maintain the desired output voltage in absence of a grid while using (2), instead the converter follows the grid voltage magnitude; hence, this mode of operation is denoted as grid-following (GFL) operation. Accurate tracking of either the real power reference or the reactive power reference can be achieved depending on the choice of $\phi$; integral compensation can be used to achieve accurate tracking of the other. For instance, the real power reference $P_0$ can be generated dynamically by a closed-loop compensator for DC bus voltage regulation in an active-front-end rectifier with $\phi = \pi/2$. DC bus voltage regulation is further discussed in Section V-B. Note that the control law given by (3) appears similar to stationary frame integral current control utilizing complex signal rotation. However, the distinctions from conventional PI current regulators become evident once the current reference $i_0$ is substituted using (3). The proposed uVOC enables grid synchronization, whereas a PLL is required to generate the current reference for conventional PI regulators. uVOC enables to avoid the synchronization issues of PLL in weak grid conditions.

B. Grid Forming Operation

For GFM operation, the control law on the converter output voltage vector is taken as

$$\frac{d}{dt}(v) = \frac{\omega_0 v}{\mu} + \frac{\mu (V_p^2 - V_p^2)}{\mu} v + \eta (i_0 - i)e^{j\phi}, \tag{10}$$

where, $\mu > 0$ is a design parameter and $V_p0$ denotes the nominal set-point for the voltage vector magnitude $V_p$. The control law given by (10) is built on the synchronization results reported in [16]–[19]. The principle of operation can be explained using the simplified system shown in Fig. 1. The magnitude correction term is exerted radially along the $d$-axis on the voltage vector and it is opposed by either the error in real power output or the reactive power output depending on the selection of $\phi$. To illustrate the instantaneous droop response, first we consider $\phi = \pi/2$; Fig. 3(a) shows the corresponding operation. Without loss of generality, an arbitrary current error $e_i$ is considered. Using (5), the controller given by (10), can be rearranged as

$$\frac{d}{dt}(v) = [j(\omega_0 + \eta e_i P) + (\mu e_v - \eta e_i Q)] v. \tag{11}$$

Here, $e_v = V_p^2 - V_p^2$. The dynamics along the $d$ and $q$ axes are obtained as

$$\frac{d}{dt}(V_p) = \mu V_p (V_p^2 - V_p^2) - \eta V_p e_i Q, \quad \text{along } d\text{-axis;} \tag{12}$$

$$\omega = \omega_0 + \eta e_i P, \quad \text{along } q\text{-axis.}$$

Along the $d$-axis, unlike GFL operation, the voltage vector magnitude cannot be adjusted freely due to the magnitude correction term; instead, a nonlinear droop in the instantaneous magnitude of the output voltage vector is observed which can be obtained by setting $dV_p/dt = 0$ as

$$V_p^2 = V_p^2 + \frac{2\eta}{\mu N V_p^2} (Q_0 - Q). \tag{13}$$

It is worth noting that the non-linearity in the droop response becomes prominent when the system operates far away from the nominal set-points $Q_0$ and $V_p0$; close to the nominal condition, the droop relation can be approximated as linear.
The closed-form solution for the steady-state voltage is listed in Appendix A. Along the \( q \)-axis, \( P - \omega \) droop, same as (3), is obtained. It is worth noting that the droop response is achieved naturally by the time-domain implementation without explicit regulation of voltage amplitude and frequency using the calculated output power which is required in droop based methods [25].

Using similar analysis, it can be shown that \( P - V \) and \( Q - \omega \) droop responses are obtained along the \( d \) and \( q \) axes, respectively, for \( \phi = 0 \). Fig. 3(b) shows an example of GFM operation with \( \phi = 0 \) for an arbitrary current error \( e_i \) and the infinite bus voltage \( V_g \). Coupled droop relations among \( P, Q, \omega, \) and \( V \) can be achieved using \( \phi \in (0, \pi/2) \). However, for faster synchronization \( \phi = 0 \) and \( \phi = \pi/2 \) should be used in dominantly resistive and inductive networks, respectively. The detail derivation of instantaneous droop response for GFM operation for arbitrary rotation angle \( \phi \) is provided in Appendix A. In essence, the harmonic oscillator term tends to restore the nominal frequency by forcing the voltage vector \( v \) along the \( q \)-axis, whereas, the magnitude correction term forces the voltage vector along the \( d \)-axis to restore the nominal magnitude; however, both are opposed by the synchronization feedback term based on the instantaneous real and reactive power output of the converter. Consequently, a self synchronizing system is obtained.

The fault management block generates two signals \( x_f \) and \( x_r \) to enable fault ride-through operation. During normal operation, defined by \( \{ x_f = 0, x_r = 0 \} \), the controller shown in Fig. 6 excluding the EVI and the pre-synchronization components, effectively implements (2) and (10) for GFL and GFM operations, respectively. Note that the complementary signal is defined as \( \pi_f = \text{NOT}(x_f) \). The circular limiter generates saturated current reference as

\[
i_{0,sat} = \begin{cases} i_0, & |i_0| \leq I_m \\ i_0 \times (I_m/|i_0|), & \text{otherwise} \end{cases}
\]

(14)

Here, \( I_m \) denotes the maximum allowable current. Under normal operating conditions the circular limiter block is transparent and during fault, marked by \( |i_0| > I_m \), the current reference vector is radially limited, i.e., magnitude is limited keeping the angle unaltered, which enables synchronization during fault. In the following subsections, first, SVO parameter selection guidelines are developed; the EVI, single-phase operation, and the fault management block are explained subsequently. Detailed implementation of the pre-synchronization filter is presented in Section V.C after we develop the small-signal model of uVOC.

III. IMPLEMENTATION OF UVOCC

A three-phase voltage source converter (VSC) using uVOC is shown in Fig. 5. The switching duty-ratio \( m \) for the PWM is generated from uVOC output \( v_e \) using appropriate scaling based on the DC bus voltage measurement. The controller, shown in Fig. 6, is implemented based on space vectors in stationary \( \alpha \beta \)-reference frame; either of the converter-side current or the network/grid-side current feedback can be used for controller implementation. GFM operation is used in grid-supporting applications or for decentralized power sharing in an islanded microgrid. GFL operation should be used for interfacing non-dispatchable sources or loads, such as motor drives. Identical control structure is used for GFL and GFM applications; the controller can transition from GFM to GFL operation by simply assigning \( \mu = 0 \). The real power reference \( P_0 \) is dynamically generated if DC bus voltage regulation is desired in GFL applications. The pre-synchronization filter, marked in green in Fig. 6, is used for soft start-up and transition from islanded to grid-tied operation. The emulated virtual impedance (EVI) is used in all modes of operation. The fault management block generates two signals \( x_f \) and \( x_r \) to enable fault ride-through operation. During normal operation, defined by \( \{ x_f = 0, x_r = 0 \} \), the controller shown in Fig. 6 excluding the EVI and the pre-synchronization components, effectively implements (2) and (10) for GFL and GFM operations, respectively. Note that the complementary signal is defined as \( \pi_f = \text{NOT}(x_f) \). The circular limiter generates saturated current reference as

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(14)

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A. SVO Parameter Selection

The SVO parameters \( \eta \) and \( \mu \) are selected based on the desired steady-state response. For GFM operation, the parameter selection process begins with the specification such that the output power of the VSC should be limited to \([-P_{\text{rated}}, P_{\text{rated}}]\) and \([-Q_{\text{rated}}, Q_{\text{rated}}]\) when the voltage and frequency deviation at the PoC varies within the full range, i.e., \( \Delta V_g = (V_0 - V_g) \in [-\Delta V_{\text{max}}, \Delta V_{\text{max}}] \) and \( \Delta \omega_g = (\omega_0 - \omega_g) \in [-\Delta \omega_{\text{max}}, \Delta \omega_{\text{max}}] \), respectively, where \( V_0 = V_{\text{ref}}/\sqrt{2} \) and \( V_g = V_{\text{gsp}}/\sqrt{2} \) denote the respective L-N RMS values. Detail derivation of the design method is provided in Appendix B. Using (33) to (39), the selection of parameter values are summarised in Table I. The analysis is
based on the steady-state droop relation at the poles of the switch network. Due to the LCL filter, the droop response at the PoC differs from that at the poles of switch network. However, the design guidelines listed in Table I ensure that the real and reactive power output at the VSC terminal at PoC are limited within the rated values for variation of network frequency and voltage over the full allowable range. To illustrate the parameter selection process, we consider the three-phase VSC listed in Table II. The passive filter is based on the steady-state droop relation at the poles of the switch network. Due to the LCL filter, the droop response of SVO given by output powers are limited within the rated values. The results in Fig. 7 are obtained numerically from power flow solution for the LCL filter and the steady-state response of SVO given by (31) and (32) in Appendix A. Selection of \( \eta \) for GFL operation is done following identical steps as GFM operation.

| Parameter | For \( \phi = \pi/2 \) | For \( \phi = 0 \) |
|-----------|----------------|----------------|
| \( \eta \)  | \( N \Delta \omega_{\text{max}} V_{\text{max}}^2 / P_{\text{rated}} \) | \( N \Delta \omega_{\text{max}} V_{\text{max}}^2 / Q_{\text{rated}} \) |
| \( \mu \)   | \( 2\eta Q_{\text{rated}} / \sqrt{N[(2V_{\text{max}}^2 - V_0^2)^2 - V_0^4]} \) | \( 2\eta P_{\text{rated}} / \sqrt{N[(2V_{\text{max}}^2 - V_0^2)^2 - V_0^4]} \) |

Table II

| Parameter | Converter Ratings |
|-----------|--------------------|
| \( S_{\text{rated}} \) | 10 kVA |
| \( P_{\text{rated}} \) | Rated real power 9 kW |
| \( Q_{\text{rated}} \) | Rated reactive power 4.4 kVAR |
| \( V_0 \) | Nominal (L-N RMS) voltage 120 V |
| \( \omega_0 \) | Nominal frequency 2\( \pi \) (60) rad/s |
| \( f_s \) | Switching frequency 10kHz |
| \( f_f \) | Sampling frequency 10kHz |
| \( L_{\alpha} \) | Converter-side inductor 7.78 \%pu |
| \( L_{\beta} \) | Network-side inductor 5.24 \%pu |
| \( C_f \) | Filter capacitor 8.79 \%pu |

Figure 7. Real and reactive power outputs of the VSC at PoC are limited within rated values for frequency and voltage variation at the PoC over the entire operating range.

B. Emulated Virtual Impedance (EVI)

EVI is used in all modes of operation and has two key purposes, namely, harmonic compensation and stabilization of SVO. The converter output impedance can be selectively increased to very high values at the harmonic frequencies to suppress harmonic distortion in converter output current originating from non-ideal effects such as dead-time/blanking time of power-devices and/or harmonic distortion in network/grid voltage. EVI is achieved as

\[
Z_v(s) = \frac{R_{\text{vir}}}{s/\omega_c + 1} + \sum_h \frac{1}{s^2 + \omega_{B,h} \beta + \omega_h^2} \text{ for } i = i_h;
\]

\[
Z_v(s) = \frac{R_{\text{vir}}}{s/\omega_c + 1} + \sum_h \frac{1}{s^2 + \omega_{B,h} \beta + \omega_h^2} \text{ for } i = i_a,
\]

where, \( K_h \) and \( \omega_{B,h} \) denote the desired impedance magnitude and the bandwidth of the resonant filter at harmonic frequency \( \omega_h \), respectively. Note that the resonant parts of \( Z_v(s) \) are designed to be inductive or resistive for harmonic suppression when grid-side current or converter-side current feedback is used, respectively. Detail design guidelines for harmonic compensation can be found in [30]. Virtual impedance design guidelines to compensate harmonic voltage distortion at the PoC while feeding nonlinear loads can be found in [31]. However, to ensure dynamic stability of the SVO, a virtual resistance \( R_{\text{vir}} \) with a limited bandwidth of \( \omega_c \) is used in both cases. The control laws given by (2) and (10) are of integral form; the lack of proportional term leads to poor damping. In essence, the virtual resistance \( R_{\text{vir}} \) constitutes a proportional compensation and provides the necessary damping. The damping effect of \( R_{\text{vir}} \) through small-signal analysis is illustrated in Section V-A.

C. Single Phase Operation

uVOC is a vector controller running on both \( \alpha \) and \( \beta \) axis. In a single-phase implementation, the full vector controller is used. However, the virtual impedance \( Z_v(s) \) emulation is required only for the \( \alpha \) axis. The feedback signal \( i_\beta \) can be generated by delaying the actual converter output current \( i_\alpha = i_a \) or \( i_b \) by \( T_b/4 = 2\pi/(4\omega_0) \) and the modulating signal for PWM is obtained from \( v_{\alpha,x} \). All analysis and design guidelines presented in the following sections are generalized to apply identically for single phase and three phase applications using the parameter \( N \).

D. Fault Management

A fault state is latched, i.e., \( x_f \) is pulled high, once \( |i| > I_T \) is detected, where \( I_T \) denotes the over-current threshold. An over-current may be triggered in a GFM converter by an overload or an AC fault while serving local loads; a GFM or GFL converter can be subjected to over-current in grid-tied operation due to an upstream fault or voltage sag at the PoC. The fault state is cleared, i.e., \( x_f \) is pulled low, when the terminal voltage \( v_g \) returns above the low-voltage threshold \( V_T \). Once a fault is detected in a GFM converter, the magnitude correction term is disabled by the complementary signal \( x_f \). For over-current limiting (OCL), a series compensation is applied as
Here, \( \theta(t) = \int \omega dt = \omega t + \theta(t) \). Without loss of generality, the network frequency can be taken as \( \omega \), and the rotating reference frame can be taken to be aligned with \( \omega \). Note that the synchronous reference frame used in Section IV is aligned with the oscillator voltage vector \( v \). In the synchronous dq-frame, the dynamics of the converter output current \( i_{dq} \) can be derived as

\[
\begin{bmatrix}
\dot{i}_d \\
\dot{i}_q
\end{bmatrix} = \begin{bmatrix}
\frac{-R}{L} & \frac{R}{L} & \omega_e \\
\omega_e & \frac{-R}{L} & -\frac{R}{L}
\end{bmatrix}
\begin{bmatrix}
i_d \\
i_q
\end{bmatrix} + \frac{1}{L_e} \begin{bmatrix}
V_o \cos(\theta_e) - V_g \\
V_o \sin(\theta_e)
\end{bmatrix}.
\]

(18)

Here, \( i_{dq} = i_d + j i_q = (I_d + j I_q)/\sqrt{2} \). For the implementation shown in Fig. 3, \( V_g = V \) can be assumed since the instantaneous feedback of the DC bus voltage is used to determine the modulating duty ratio \( m \). However, for real applications, measurement noise propagates directly into the modulating signal if instantaneous DC bus voltage feedback is used; instead, the nominal DC bus voltage reference \( V_{dc} \) can be used which gives \( V_a = (v_{dc}/V_{dc}) V \). The real power \( P \) and reactive power \( Q \) are given as

\[
\begin{bmatrix}
P \\
Q
\end{bmatrix} = \frac{NV_{dc}^2}{V_{dc}^2} \begin{bmatrix}
\cos(\theta) \\
\sin(\theta)
\end{bmatrix} \begin{bmatrix}
I_d \\
I_q
\end{bmatrix}.
\]

(19)

The DC bus voltage dynamics can be derived as

\[
\frac{d}{dt} \left( \frac{1}{2} C_{dc} V_{dc}^2 \right) = P_{dc} - P.
\]

(20)

Using (17), (18), (19) and (20), the small signal model can be obtained as

\[
\begin{bmatrix}
\Delta \dot{x} \\
\Delta \dot{v}_{dc}
\end{bmatrix} = \begin{bmatrix}
A_{11} & A_{12} \\
A_{21} & A_{22}
\end{bmatrix} \begin{bmatrix}
\Delta x \\
\Delta v_{dc}
\end{bmatrix} + \begin{bmatrix}
B_{11} \\
B_{21}
\end{bmatrix} \Delta P_0 - \begin{bmatrix}
\Delta Q_0
\end{bmatrix},
\]

(21)

where, \( x = [\Delta I_d \Delta I_q \Delta V \Delta \theta]^T \) and the detail forms of \( A_{11} \in \mathbb{R}^{4 \times 4}, A_{21} \in \mathbb{R}^{1 \times 4}, A_{12} \in \mathbb{R}^{4 \times 1}, A_{22} \in \mathbb{R}, B_{11} \in \mathbb{R}^{4 \times 2}, \) and \( B_{21} \in \mathbb{R}^{1 \times 2} \) are provided in Appendix C. Note that \( \Delta \) denotes small perturbation around the operating point.

B. Fault Ride-Through Operation

During a fault, the circular limiter saturates the current reference and current error as

\[
i_{0,\text{sat}} = (I_m/i_0) i_{0} = (K_m V) i_0;
\]

(22)

\[
e_1 = 1/(NV^2) \{(K_m V P_0 - P) - \beta(K_m V Q_0 - Q)\} v,
\]

where \( K_m = N I_m/\left(\sqrt{2} (P_0^2 + Q_0^2)\right) \). Now the modified SVO dynamics can be obtained by simply substituting \( P_0 \) and \( Q_0 \) in (17) by \( K_m V P_0 \) and \( K_m V Q_0 \), respectively. Due to the over-current limiting compensation (see Fig. 5), the effective resistance increases as \( R_e = R_{vir} + R_0 \) and an additional term \( + R_0 i_{0,\text{sat}} \) is added on the right side of (18). The output current dynamics in the synchronous frame can be derived as
Following similar steps as the preceding subsection, the small signal model of the system during fault mode operation can be derived.

V. CONTROL DESIGN FOR DYNAMIC PERFORMANCE

The virtual resistance $R_{\text{vir}}$, DC bus voltage regulator, and the pre-synchronization filter are designed to ensure the desired dynamic response.

A. Selection of Virtual Resistance

The small-signal model is used to select $R_{\text{vir}}$ once the SVO parameters are chosen. For GFM operation, we assume that the DC bus voltage is maintained by a DC source or regulated by an AC/DC or DC/DC converter stage; therefore, the DC bus dynamics are ignored. The linearized system dynamics for the GFM operation is given by

$$
\dot{x} = A_{11} x + B_{11} \begin{bmatrix} \Delta P_0 & \Delta Q_0 \end{bmatrix}^T.
$$

The system poles are given by $\lambda(A_{11})$, where $\lambda(\cdot)$ denotes eigenvalue. To illustrate the selection of $R_{\text{vir}}$, we consider the VSC listed in Table II to be connected to a stiff grid with a dominantly inductive network/grid impedance $Z_N \approx sL_N, L_N = 1\, \text{mH} \approx 8.7\% \, \text{pu}$. To account for the worst-case from stability perspective, the LCL filter elements are assumed to be lossless. Table III lists the system poles for different values of the equivalent series resistance $R_c \approx R_{\text{vir}}$. For $R_{\text{vir}} = 0.5\%$, the system becomes unstable, whereas for $R_{\text{vir}} = 1.15\%$ a stable, yet very lightly damped system results which is evident from the real part of the complex-conjugate pole pair. Lastly, a well-damped system response is achieved which is evident from the real part of the complex-conjugate eigenvalue. To illustrate the selection of $R_{\text{vir}}$, once the SVO parameters are chosen. For GFM operation, we assume that the DC bus voltage is maintained by a DC source or regulated by an AC/DC or DC/DC converter stage; therefore, the DC bus dynamics are ignored. The linearized system dynamics for the GFM operation is given by

$$
\dot{x} = A_{11} x + B_{11} \begin{bmatrix} \Delta P_0 & \Delta Q_0 \end{bmatrix}^T.
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The system poles are given by $\lambda(A_{11})$, where $\lambda(\cdot)$ denotes eigenvalue. To illustrate the selection of $R_{\text{vir}}$, we consider the VSC listed in Table II to be connected to a stiff grid with a dominantly inductive network/grid impedance $Z_N \approx sL_N, L_N = 1\, \text{mH} \approx 8.7\% \, \text{pu}$. To account for the worst-case from stability perspective, the LCL filter elements are assumed to be lossless. Table III lists the system poles for different values of the equivalent series resistance $R_c \approx R_{\text{vir}}$. For $R_{\text{vir}} = 0.5\%$, the system becomes unstable, whereas for $R_{\text{vir}} = 1.15\%$ a stable, yet very lightly damped system results which is evident from the real part of the complex-conjugate pole pair. Lastly, a well-damped system response is achieved for $R_{\text{vir}} = 4.9\%$. Following similar steps, $R_{\text{vir}}$ can be selected for GFL operation using (24) for $\mu = 0$.

| $R_{\text{vir}}$ | $\lambda(A_{11})$ |
|------------------|------------------|
| 0.5\% pu        | $9.16 \pm 378.12\, \text{j}$ | $-47.57$ | $-17.90$ |
| 1.15\% pu       | $-1.94 \pm 377.67\, \text{j}$ | $-47.72$ | $-17.91$ |
| 4.9\% pu        | $-66.61 \pm 374.56\, \text{j}$ | $-47.61$ | $-17.68$ |

B. DC Bus Voltage Regulation (GFL Operation)

DC bus voltage regulation can be achieved by using the GFL form of uVOC and dynamically generating $P_0$ using a closed-loop voltage regulator. To design the DC bus voltage regulator, the uncompensated open-loop response $G_{\text{OL}}(s) = \Delta v_{\text{dc}}(s)/(-\Delta P_0(s))$ can be derived from the transfer function as

$$
G_{\text{rec}}(s) = C_{\text{rec}} \begin{bmatrix} sI - A \end{bmatrix}^{-1} B,
$$

where, $G_{\text{rec}}(s) \in \mathbb{C}^{1 \times 2}$ and $I$ denotes the identity matrix of dimension 5, $C_{\text{rec}} = [0 \ 0 \ 0 \ 0 \ 1]$. The definitions of $A$ and $B$ are provided in Appendix C. A lead-lag filter combined with a PI compensator can be used for closed-loop regulation, given as follows:

$$
F_{\text{dc}}(s) = K_{\text{pdc}} \left( 1 + \frac{1}{sT_1} \right) \sqrt{\frac{\omega_p}{\omega_z}} \frac{s + \omega_z}{s + \omega_p}.
$$

Here, $\omega_p$ and $\omega_z$ for the lead-lag filter should be chosen to achieve sufficient phase boost at the gain cross-over frequency $\omega_c$, whereas the integral time-constant $T_1$ should be chosen for sufficient DC gain through bode plot analysis.

C. Pre-Synchronization

The pre-synchronization filter (see Fig. 6) is essentially a first-order low-pass filter in the form of a virtual RL branch taken as

$$
i_{\text{ps}} = Y_{\text{ps}}(s)(v - v_g); \quad Y_{\text{ps}}(s) = 1/(sL_{\text{ps}} + R_{\text{ps}})
$$

The parameters can be chosen as $L_{\text{ps}} \approx (L_a + L_q)$ and $R_{\text{ps}} \approx R_{\text{vir}}$. It is worth noting that exact knowledge of the LCL filter parameters are not required for the parameter selection. To illustrate the functionality, two distinct use-cases can be defined for the pre-synchronization filter.

1) Start-Up in GFL Converters: For GFL converters while serving local loads, the voltages across the STS need to be synchronized prior to closing the STS. In such scenarios, the pre-synchronization block is run to generate a virtual current $i_{\text{ps}}$, which is added to the actual converter output current and the resultant total current is used as feedback to the SVO. The virtual current $i_{\text{ps}}$ gives an estimate of the current that would flow between the VSC and the network at the PoC if the STS were closed. Due to the virtual current $i_{\text{ps}}$ feedback, SVO adjusts the oscillator voltage vector to minimize the virtual real and reactive power flow. When the amplitude of the virtual current $|i_{\text{ps}}|$ stabilizes, the STS can be closed safely.

2) Start-Up in GFL Converters: For GFL operation, the STS can be closed before the switching of the power devices are initiated. For instance, during start-up of an active-front-end rectifier, the DC bus may be charged by using the switch network as an uncontrolled diode bridge. Meanwhile, the SVO can be synchronized with the measured voltage $v_g$ using the pre-synchronization filter and once $|i_{\text{ps}}|$ stabilizes, the DC bus voltage control loop and the switching of the power devices can be initiated without large transients.

VI. SIMULATION RESULTS

All simulations are performed in PLECS standalone using detailed switching model of a three-phase VSC with parameters listed in Table II.

A. Small Signal Model Validation

To validate the small signal model, we consider the DC bus voltage regulation for active rectifier operation of the VSC listed in Table II. The DC bus voltage reference is set as $v^* = 400 \, \text{V}$ and $\phi = \pi/2$ is used. The control parameters are selected as $\eta = 16.63, \mu = 0, R_{\text{vir}} = 0.21 \, \Omega (=4.9\% \, \text{pu}), \omega_c = 1.2 \, \text{krad/s}, K_{\text{pdc}} = 75 \, \text{W/V}, T_1 = \ldots$
0.4 s, $\omega_z = 5\pi$ rad/s, and $\omega_p = 30\pi$ rad/s. To validate the analytical model, loop-gain measurement is performed; multi-tone small signal perturbation is injected in the feedback loop and the loop gain is calculated at discrete frequency points from the recorded response [33]. Fig. 9 shows the comparison between the analytical and measured responses.

**B. GFL Operation with Weak Grid**

To illustrate the GFL operation with weak grid, we consider the three-phase VSC described in Section VI-A connected to a grid with short-circuit ratio (SCR) of 1.9. Through small signal analysis, the controller is redesigned as $R_{vir} = 23.6$ p.u. and $K_{pdc} = 335$ W/V while keeping the other parameters same. The compensated open-loop response is shown in Fig. 10. Fig. 11 shows the simulated response. After charging the DC bus, the closed-loop regulation is initiated at $t_1$. Subsequently, no-load to full-load and full-load to no-load transitions are introduced across the DC bus at $t_2$ and $t_3$, respectively. In both cases, the desired DC bus voltage is quickly restored.

**C. Fault Ride-Through**

Next, the VSC is operated as a GFM converter using $\phi = \pi/2$, $\eta = 16.63$, $\mu = 5.2 \times 10^{-4}$, and $R_{vir} = 0.21$ Ω; a voltage source is used to maintain the DC bus. The grid is modelled by an ideal AC source with an inductor to emulate different SCRs. First, we consider an SCR of 5. The control parameters are set as $V_T = 0.9$ p.u., $I_T = 1.1$ p.u., $I_m = 1$ p.u, $R_0 = 5.25$ V/A, $t_f = 100$ ms and $\tau_f = 28$ ms, whereas the real power reference is set as $P_0 = 0.5$ p.u. To emulate a symmetrical AC fault, the AC source voltage magnitude is suddenly stepped down from 1 p.u. to 0.3 p.u. at $t = 2$s (see Fig. 12). Once the fault is detected, the reactive power reference $Q_0$ is raised to utilize remaining current capability of the VSC as $Q_0 = \sqrt{S_{rated}^2 - P_0^2}$. The converter clamps the output current at 1 p.u. and once the fault is cleared, i.e. source voltage returned to 1 p.u. at $t = 2.3$s, the VSC resumes normal operation. The experiment is repeated for an SCR of 1.9 and the corresponding result is shown in Fig. 13.

Note that for relatively stronger grids, to limit the initial current overshoot at the instants when a fault occurs and clears, a band-limited virtual inductance can be used in addition with the virtual resistance as $(R_{vir} + sL_{vir})/(s/\omega_c + 1)$ in (15); $L_{vir}$ can be included in $L_e$ for small signal analysis and parameter
selection described in Section IV and V. $L_{\text{vir}} = 1 \text{ mH}$ is used for the simulation result shown in Fig. 12.

D. Validation of Droop Response

The VSC is run in GFM operation using $\phi = \pi/2$ and the grid frequency and voltage are varied to validate the droop response given by (8) and (13). Fig. 14 shows the comparison between the simulated and analytical droop responses.

VII. EXPERIMENTAL RESULTS

The GFL and GFM operations of uVOC are validated through hardware experiments using laboratory prototypes. For all the experiments described in the following subsections, digital control is implemented using Texas Instruments’ C2000 digital signal processor (DSP) TMS320F28377S.

A. DC Bus Voltage Regulation (GFL Operation)

A single-phase active rectifier with parameters listed in Table II is used. For single phase operation the rated real and reactive powers are given as $P_{\text{rated}} = 3 \text{ kW}$ and $Q_{\text{rated}} = 1.5 \text{ kVAR}$, respectively. To prevent propagation of measurement noise, the nominal DC bus voltage reference is used for calculating the modulating signal $m$. The nominal DC bus voltage is set as $v^* = 200 \text{ V}$; $\phi = \pi/2$ is used and the control parameters are selected as $\eta = 16.63$, $R_{\text{vir}} = 0.21 \text{ }\Omega$, $K_{\text{dc}} = 40 \text{ W/V}$, $T_I = 0.4 s$, $\omega_z = 5\pi \text{ rad/s}$, and $\omega_p = 30\pi \text{ rad/s}$ for a control bandwidth of $\approx 7\pi \text{ rad/s}$ with gain margin of $\approx 25.6 \text{ dB}$ and phase margin of $\approx 71.5^\circ$ at no load condition.

First, an AC voltage source is used to emulate a strong grid. Fig. 15(a) shows the start-up transient. DC bus charging and soft start-up is achieved by using the method presented in Section V-C2. DC bus voltage regulation and converter switching are initiated at $t_1$. The DC bus voltage is quickly stabilized at the reference value. Fig. 15(b) shows the steady-state voltage and current shapes when serving $\approx 1.5 \text{ kW}$ load and the reactive power reference is set as $Q_0 = 0$. Next, reactive power dispatch is introduced. The rectifier serves $\approx 1.2 \text{ kW}$ DC load, when a step change in the reactive power reference ($Q_0 = 500 \text{ VAR}$ to $Q_0 = -500 \text{ VAR}$) is introduced; the corresponding waveshapes are shown in Fig. 16(a). The reactive power reference $Q_0$ and the output reactive power $Q$ measured by the DSP are shown on the scope using two Digital-to-Analog (DAC) channels on the DSP. The opposite step response from $Q_0 = 500 \text{ VAR}$ to $Q_0 = -500 \text{ VAR}$ is shown in Fig. 16(b). In both cases, accurate tracking of the reactive power reference is obtained with minimal transient. The steady-state voltage and current shapes for $Q_0 = -500 \text{ VAR}$ and $Q_0 = 500 \text{ VAR}$ are shown in Fig. 17(a) and Fig. 17(b), respectively.
VSC, which gives an SCR of \( \approx 1.9 \). The converter response to a step change in the DC load from 0 to \( \approx 1.4 \) kW is shown in Fig. 18(a) and the corresponding steady-state response is shown in Fig. 18(b). For weak grid operation, the control parameters were redesigned as \( R_{\text{vir}} = 1 \Omega, K_{\text{pdc}} = 120 \text{ W/V} \), while keeping the other parameters same as that for strong grid operation. For the chosen values, the small signal model given by (25) estimates a control bandwidth of \( \approx 4.4 \text{ Hz} \) at \( P = 1.4 \text{ kW} \) with a gain margin of \( \approx 23 \text{ dB} \) and phase margin of \( \approx 107^\circ \) which suggests a damped response with a settling time on the order of \( 1/(4.4\text{Hz}) = 227 \text{ ms} \), whereas during the experiment the DC bus voltage exhibits damped response and settles within \( \approx 250 \text{ ms} \) (see Fig. 18(a)). It is worth noting that for this configuration the space vector oscillator achieves stable operation with an effective \( X/R \) ratio of \( \approx 2.8 \) since \( R_{\text{vir}} \) appears in the equivalent resistance seen by the oscillator; hence, assumption of a dominantly inductive grid is not required for the the SVO to retain synchronization.

Next, the inductor is removed and the load is connected at the PoC. An effective dead-short is introduced at the PoC and the response is shown in Fig. 19. The converter utilizes its full current capability to provide voltage support at the PoC. Once the short circuit is removed, normal operation is resumed quickly.

C. GFM Operation

uVOC GFM operation is validated in a hybrid AC-DC microgrid. The microgrid structure is shown in Fig. 22. Two battery storage units are connected to 380V DC buses through non-isolated DC/DC converters. Two interlinking converters (ILCs) are used to connect the DC systems to the AC side. Each ILC can connect/disconnect to/from the AC microgrid using static transfer switches (STS\(_1\) and STS\(_2\)) and the AC microgrid can be islanded using another STS\(_g\). The front-ends of the ILCs are rated at \( P_{\text{rated}} = 3 \text{ kW}, Q_{\text{rated}} = 1.5 \text{ kVAR} \), and \( V_0 = 240.0 \text{ V} \). The control parameters are chosen as \( \eta = 133, \mu = 5.3 \times 10^{-4} \), and \( R_{\text{vir}} = 0.2 \Omega \) for \( \phi = 0 \) following the guidelines presented in Sections III-A and IV.
1) Islanded Operation: Islanded operation ($ST_S^g$ open) of the hybrid AC-DC microgrid system is illustrated in Fig. 23. where the two interlinking converters ILC1 and ILC2 serve the AC load. Fig. 24 shows the pre-synchronization process for ILC1, when $ST_S^g$ is closed and $ST_S^1$ is open. Before synchronization, a large phase mismatch is observed between $v_{f1}$ and $v_{g1}$ (Fig. 24(a)). Using the proposed pre-synchronization method, synchronization is achieved, shown in Fig. 24(b). The speed of the pre-synchronization process varies as a function of the initial phase, frequency, and voltage magnitude difference; trajectory analysis or numerical simulation may be used to determine the expected longest time required under various initial conditions. During the experiment shown in Fig. 24 pre-synchronization is achieved within $< 1$ s. At this condition, ILC1 can be connected to the grid by closing $ST_S^1$. The corresponding transient is shown in Fig. 25.

2) Grid-Connected Operation: In grid-connected operation, the converter output current without using the harmonic compensation method is illustrated in Fig. 26(a). Evidently, higher order harmonics are present in the output current. Using resonant filters given in (15) at $h = 3, 5, 7, 9, 11,$ and $13$, the distortion is compensated and the corresponding current shape is shown in Fig. 26(b). Next, unintentional islanding is demonstrated in Fig. 27. Prior to disconnecting from the grid by opening $ST_S^g$, the ILC1 draws real power from the grid ($i_{dc1} < 0$). At the opening of $ST_S^g$, marked by the transition in grid current $i_{gt}$, the power-flow through the ILC1 reverses immediately and the load current $i_L$ does not experience any noticeable disturbance.

Oscillator based control, such as dVOC, was initially conceived based on a number of simplifying assumptions; all sources in the network were assumed to be oscillator based and the power converters were treated as ideal voltage sources ignoring the nonidealities of real systems such as harmonic distortion originating from network/grid side or deadtime/blanking time of the power devices. However, such simplifying assumptions are not required for the analysis and design of uVOC which is validated through the experimental results showing grid-tied operation for both GFL and GFM applications and harmonic current suppression. It is worth noting that uVOC is still an emerging technology in its early developmental phase. Established methods such as VSM...
enables synthetic inertia emulation and decades of research has established standard practices and implementation guidelines under a variety of application conditions. The established controllers offer intuitive insight into their synchronization mechanism leading to simplified design. In this work, physical interpretation of the synchronization process of uVOC is presented. Furthermore, effective fault-ride-through capability and operation under weak grid conditions have been demonstrated. Overall, the key distinctions of uVOC in context of the state-of-the-art GFM controllers are summarized in Table IV.

### APPENDIX B

**DESIGN OF \( \eta \) AND \( \mu \)**

First, we consider \( \phi = \pi/2 \) which relates real power with instantaneous frequency and reactive power with instantaneous voltage vector magnitude.

1) \( P - \omega, \ Q - V \) DROOP (\( \phi = \pi/2 \)): For \( \phi = \pi/2 \), the operating point is given by

\[
V = \frac{V_0}{\sqrt{2}} \left[ 1 + \left[ 1 + \frac{2\eta}{N\mu V_0^2} (Q_0 - Q) \right]^{\frac{1}{2}} \right]^{\frac{1}{2}};
\]

\[
\omega = \omega_0 + \frac{\eta}{N V^2} (P_0 - P).
\]

For the selection of \( \mu \) and \( \eta \), we set \( P_0 = 0, \ Q_0 = 0 \) which results in \( V = V_0, \ \omega = \omega_0 \) for \( P = 0, \ Q = 0 \). The real power output should reach the rated value at the maximum allowable frequency deviation as

\[
P_{\text{rated}} = \frac{N V_{\text{max}}^2}{\eta} \Delta \omega_{\text{max}},
\]

where, \( V_{\text{max}} \) denotes the maximum voltage RMS. \( \eta \) can be selected using (35). The reactive power output for a given voltage \( V \) can be obtained from (33) as

\[
Q = \frac{N \mu}{2\eta} \{ V_0^4 - (2V_0^2 - V_0^2)^2 \}.
\]

For a given \( \Delta V_{\text{max}} \), \( |Q|_{V=V_{\text{max}}} > |Q|_{V=V_{\text{min}}} \) and therefore, to ensure \( |Q| \leq Q_{\text{rated}} \) over the entire operating range, \( \mu \) is selected using

\[
\mu = \frac{2Q_{\text{rated}}}{N} \frac{1}{(2V_{\text{max}}^2 - V_0^2)^2 - V_0^4}.
\]

2) \( P - V, \ Q - \omega \) DROOP (\( \phi = 0 \)): For \( \phi = 0 \), similar analysis can be done to obtain

\[
Q_{\text{rated}} = \frac{N V_{\text{max}}^2}{\eta} \Delta \omega_{\text{max}};
\]

\[
\mu = \frac{2P_{\text{rated}}}{N} \frac{1}{(2V_{\text{max}}^2 - V_0^2)^2 - V_0^4}.
\]
\[
\begin{bmatrix}
A_{11} & A_{12} \\
A_{21} & A_{22}
\end{bmatrix}
= \begin{bmatrix}
\omega_s & -R_s & k_v & -k_v V_{dc} & \frac{V_{dc}}{V_{dc}^2} \\
-\omega_s & \frac{R_s}{L_s} & k_v \cos(\theta_s) & k_v \sin(\theta_s) & \frac{V_{dc}}{V_{dc}^2} \\
-\eta_k v \sin(\theta_s) & \eta_k v \cos(\theta_s) & 2\mu(V_o^2 - 3V^2) - \frac{\eta Q_s}{V^2} & -\eta_k v \xi_1 & -\xi_2 / V_{dc}^2 \\
-\frac{\eta_k v}{C_{dc} V_{dc}} \cos(\theta_s) & -\frac{\eta_k v}{C_{dc} V_{dc}} \sin(\theta_s) & -2n_P f_s / V^2 + \frac{\eta_k v}{V} & \eta_k v \xi_2 / V \\
-\frac{\eta Q_s}{C_{dc} V_{dc}} \cos(\theta_s) & -\frac{\eta Q_s}{C_{dc} V_{dc}} \sin(\theta_s) & -N_\xi / (C_{dc} V_{dc}^2) & N_\xi_2 / (C_{dc} V_{dc}^2) & 0
\end{bmatrix}
\]

\[
B_{11} = \begin{bmatrix}
0 & 0 & \frac{n}{N V} \cos(\phi) \\
0 & 0 & \frac{n}{N V} \sin(\phi) \\
0 & 0 & -\frac{n}{N V} \cos(\phi)
\end{bmatrix}^T, \quad B_{22} = \begin{bmatrix} 0 & 0 \end{bmatrix}, \quad \text{where} \quad \begin{bmatrix}
\xi_1 \\
\xi_2
\end{bmatrix} = \begin{bmatrix}
I_d \cos(\theta_s) + I_s \sin(\theta_s) \\
I_d \sin(\theta_s) - I_s \cos(\theta_s)
\end{bmatrix}.
\]

APPENDIX C

SMALL SIGNAL MODEL OF uVOC BASED VSC

Using [17], [18], [19], and [20], the dynamics of the uVOC based VSC can be organized as

\[
\dot{x}_c = F(x_c, u).
\]

Here, \(x_c = [\Delta I_d \Delta I_q \Delta V \Delta \theta_s \Delta V_{dc}]^T\) and \(u = [\Delta P_0 \Delta Q_0]^T\). The linearized system is obtained as

\[
\dot{x}_c = Ax_c + Bu;
\]

\[
A = \left[\frac{\partial F}{\partial x_c}\right]_{(x_c, u_c)}, \quad B = \left[\frac{\partial F}{\partial u}\right]_{(x_c, u_c)}.
\]

For ease of analysis for different forms of the controller, the state vector \(x_c\) is partitioned as \(x_c = [x_c^T \ v_{dc}]^T\) and the linearized matrices \(A\) and \(B\) are partitioned accordingly to obtain [21]. The details of the forms of the different matrices in [21] are given in [22].

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