AMOLED Pixel Circuit Using LTPO Technology Supporting Variable Frame Rate from 1 to 120 Hz for Portable Displays

Ching-Lin Fan 1,2,*, Chun-Yuan Chen 1, Shih-Yang Liu 2 and Wei-Yu Lin 1

1 Graduate Institute of Electro-Optical Engineering, National Taiwan University of Science and Technology, Taipei 10607, Taiwan
2 Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, Taipei 10607, Taiwan
* Correspondence: clfan@mail.ntust.edu.tw; Tel.: +886-2-27376374; Fax: +886-2-27376424

Abstract: This paper proposes a new 6T1C pixel circuit based on low-temperature polycrystalline oxide (LTPO) technology for portable active-matrix organic light-emitting diode (AMOLED) displays with variable refresh rates ranging from 1 to 120 Hz. The proposed circuit has a simple structure and is based on the design of sharing lines of switch-controlling signals. It also provides low-voltage driving and immunity to OLED degeneration issues. The calculation and analysis of programming time are discussed, and the optimal storage capacitor for the proposed circuit’s high-speed driving is selected. The results of the simulation reveal that threshold voltage variations in driving thin-film transistors of ±0.33 V can be well sensed and compensated with a 1.8% average shift of OLED currents in high-frame-rate operation (120 Hz), while the maximum variation in OLED currents within all gray levels is only 3.56 nA in low-frame-rate operation (1 Hz). As a result, the proposed 6T1C pixel circuit is a good candidate for use in portable AMOLED displays.

Keywords: low-temperature polycrystalline silicon and oxide (LTPO); active-matrix organic light-emitting diode (AMOLED); low frame rate; high frame rate; variable frame rate; portable displays

1. Introduction

Because of the benefits of outstanding color characteristics, short response time, high contrast ratio, and low power dissipation, active-matrix organic light-emitting diodes (AMOLEDs) have been widely used in display technologies [1–3]. The recent trend of display panels in high-end portable devices requires not only high resolution and pixels per inch but also low power consumption. Furthermore, portable products with adjustable frame rates are displayed with cutting-edge technology. High-frame-rate (HFR) technologies are used to achieve superior image quality in high-performance applications such as gaming or watching movies. In contrast, low-refresh-rate pixel designs are used in applications that require energy saving, such as smartwatches. In recent years, an increasing number of portable AMOLED displays have begun to incorporate LTPO technologies into pixel circuits. Low-temperature poly-Si (LTPS) thin-film transistors (TFTs) and metal-oxide-semiconductor (oxide) TFTs make up the LTPO structure. LTPS TFTs have been mainly adopted in mobile applications because of their high carrier mobility and excellent current driving capability, which make LTPS technologies beneficial to pixel circuit driving with low power consumption [4,5]. However, the characteristics of LTPS TFTs, such as the threshold voltage ($V_{TH}$), would be significantly affected by the crystallization process [6,7]; additionally, due to the properties of polysilicon materials, LTPS TFTs generally suffer from high off-state leakage current [8,9]. Oxide TFTs, on the other hand, have advantages over LTPS TFTs due to their outstanding uniformity, extremely low off-leakage current, and low process complexity [10,11]. Both dynamic image quality and power consumption are important considerations for portable AMOLED displays, and using the LTPO structure is advantageous for achieving these two goals. Because of the high carrier mobility, driving
the AMOLED pixel circuit with LTPS TFTs can dramatically reduce the programming period, allowing the pixel circuit to operate at HFR. Furthermore, to achieve low power consumption, the use of the LTPS TFT operates the pixel circuit with low-voltage driving due to its exceptional current driving capability; additionally, the low-frame-rate operation is a feasible way to realize power savings [12,13]. Holding the gate voltage of the driving TFT (DTFT) is required to support low-refresh rate driving; thus, oxide TFTs can be used to suppress the off-state current. Furthermore, the design of the storage capacitor is critical because the pixel circuit requires a relatively small capacitor to operate high-speed programming at HFR.

As a result, numerous compensating pixel circuits based on LTPO have been published to alleviate DTFT threshold voltage variations. Apple Inc. [14] pioneered the LTPO concept with the 6T1C pixel circuit, which was mass-produced in the Apple Watch Series 4, enabling an adjustable frame rate between 1 and 60 Hz. Nevertheless, the control signal lines of the circuit were complicated, thus restricting the screen resolution and bezel area. Sharp Inc. [15] demonstrated a 7T1C pixel circuit with LTPO technology that drove an AMOLED panel favorably between 1 and 120 Hz using a GOA circuit. However, operating the circuit at 1 Hz consumed a significant amount of electricity because the emission control signal was still charged and discharged 120 times in one second. Following that, Fu et al. [16] proposed a 7T1C pixel circuit that successfully solved the frequent charging–discharging problem by holding the gate voltage of the LTPS driving TFT, allowing the circuit to drive between 1 and 120 Hz. Nonetheless, this 7T1C circuit is confronted with the IR-drop issue and intricate control signal line design.

This paper proposes a novel 6T1C pixel circuit with an LTPO structure for portable displays with variable frame rates ranging from 1 to 120 Hz. To reduce the number of control signal lines and TFTs in the proposed circuit structure, a holding period is used. In addition, the proposed circuit is independent of variations in the $V_{TH}$ of OLED that provide immunity to OLED degeneration issues. The proposed circuit is provided with low-voltage driving of 5 V, operating at 120 Hz, with an average error rate of 1.8% of OLED currents, while the DTFT’s $V_{TH}$ variations are ±0.33 V. Furthermore, although the proposed pixel circuit operates at 1 Hz, the overall variations in OLED driving currents are less than 3.56 nA. As a result, the proposed 6T1C pixel circuit is a good candidate for use in portable AMOLED displays.

2. The Operation of the Proposed Pixel Circuit

Figure 1a shows the circuit construction of the proposed 6T1C LTPO pixel circuit, which adopts the top-anode OLED configuration or the inverted top-emitting OLED (ITOLED) structure [17,18]. The proposed 6T1C pixel circuit is composed of one driving LTPS TFT (T1), two switching LTPS TFTs (T4 and T6), three switching oxide TFTs (T2, T3, and T5), and one storage capacitor ($C_{ST}$). Furthermore, nodes N1 and N2 are the DTFT’s gate ($V_{GS}$) and source voltages ($V_{S}$), which play an important role in controlling pixel currents. The corresponding timing diagram is shown in Figure 1b. To reduce the complexity of the pixel circuit, both $Scan[n]$ and $Scan[n - 1]$ control signals ($Em[n]$ and $Em[n - 1]$) have the same pulse width. The operation of the proposed circuit is divided into four phases, as shown in Figure 2, presented in detail as follows.

2.1. Reset Stage

In the beginning stage of the operation, $Scan[n - 1]$ and $Em[n]$ are high to turn on T3 and T6. $Scan[n]$ and $Em[n - 1]$ are low to turn off T2, T5, and T4. The purpose of this stage is to reset the $V_{GS}$ of the DTFT. The ELVDD is applied to N1 through T3, while node N2 is discharged to ELVSS. Furthermore, the OLED is completely turned off during the reset stage to prevent image flicker.
Figure 1. (a) The schematic of the proposed 6T1C pixel circuit and (b) the timing diagram of the control signals.

Figure 2. Schematic of pixel circuit operation, including (a) reset, (b) programming, (c) holding, and (d) emission periods.

2.2. Programming Stage
During this stage, Scan\([n-1]\) and Em\([n]\) are low to turn off T3 and T6. Em\([n-1]\) remains at a low voltage to prevent current from flowing through the OLED. The programming stage is intended to compensate for DTFT \(V_{TH}\) variations while simultaneously inputting data voltage signals. Scan\([n]\) is raised to turn on T2 and T5, and a data voltage is applied to node N2 via T5. The diode-connected structure, which comprises T1, T2, and T5,
discharges node N1 from ELVDD to $V_{\text{DATA}} + V_{\text{TH\textunderscore DTFT}}$. As a result, the voltage $V_{\text{DATA}} + V_{\text{TH\textunderscore DTFT}}$ is stored in $C_{\text{ST}}$ at the end of the programming stage.

### 2.3. Holding Stage

Scan$[n]$ becomes low during the holding period to turn off T2 and T5. To turn off T3 and T6, Scan$[n-1]$ and Em$[n]$ are kept low. The N2 node is now floating, and the DTFT is turned off. As a result, even though Em$[n-1]$ turns on the switching T4, the OLED remains dark. Furthermore, the stored charges of $C_{\text{ST}}$ are well held due to the low leakage current of oxide TFTs T2 and T3.

### 2.4. Emission Stage

In the final operating stage, Scan$[n]$ and Scan$[n-1]$ remain low to turn off T2, T3, and T5, and Em$[n-1]$ remains high. Because the gate voltage (N1) is held at $V_{\text{DATA}} + V_{\text{TH\textunderscore DTFT}}$ and the ELVSS is applied to the source voltage (N2) while Em$[n]$ becomes high to turn on T6, the driving TFT operates in the saturation region. The emitting OLED current can be calculated using the following equation:

$$I_{\text{OLED}} = \frac{1}{2} \mu_n C_{\text{OX}} \left( \frac{W}{L} \right)_{\text{DTFT}} (V_{\text{GS}} - V_{\text{TH\textunderscore DTFT}})^2$$

$$= \frac{1}{2} \mu_n C_{\text{OX}} \left( \frac{W}{L} \right)_{\text{DTFT}} (V_{\text{DATA}} + V_{\text{TH\textunderscore DTFT}} - \text{ELVSS} - V_{\text{TH\textunderscore DTFT}})^2$$

$$= \frac{1}{2} \mu_n C_{\text{OX}} \left( \frac{W}{L} \right)_{\text{DTFT}} (V_{\text{DATA}})^2. \quad (1)$$

Based on Equation (1), $V_{\text{TH\textunderscore DTFT}}$ is removed, so the OLED currents are solely determined by $V_{\text{DATA}}$. As a result, the proposed pixel circuit not only compensates for variations in DTFT threshold voltage but is also unaffected by variations in ELVDD and $V_{\text{TH\textunderscore OLED}}$, improving image uniformity. In low-frame-rate applications, node N1 must be held at $V_{\text{DATA}} + V_{\text{TH\textunderscore DTFT}}$ to generate a constant driving current during the emission period. As a result, to reduce the voltage fluctuation of N1 caused by the leakage currents of T2 and T3, the switching TFTs connected to node N1 are implemented as oxide TFTs. In HFR applications, the proposed pixel circuit has to adopt an adequate storage capacitor to operate with high-speed discharging. Furthermore, the LTPS DTFT enables the proposed circuit to supply the OLED driving current with low-voltage power. As a result, the proposed pixel circuit can operate at rates ranging from 1 to 120 Hz with low-voltage driving, making it suitable for use in portable displays.

### 3. Analysis of Storage Capacitor

In HFR operation, using an appropriately sized storage capacitor to compensate for $V_{\text{TH\textunderscore DTFT}}$ variations is critical. To validate the storage capacitor design, the discharging process of the programming stage, as shown in Figure 3, is explained and analyzed in detail as follows.

In the equivalent circuit of the programming stage, the transient current ($I_{\text{CST}}$) flowing through the storage capacitor can be expressed as

$$I_{\text{CST}} = (C_{\text{ST}}) \frac{dV_{\text{N1}}}{dt} \quad (2)$$

where $V_{\text{N1}}$ is the voltage of N1 as well as the voltage being stored in $C_{\text{ST}}$. In addition, as the Scan$[n]$ signal turns on T2 and T5, a data voltage is supplied to N2 through T5. The diode-connected structure starts discharging N1 from ELVDD to $V_{\text{DATA}} + V_{\text{TH\textunderscore DTFT}}$ in an ideal operating situation. The discharging current ($I_{\text{T1}}$) can be presented as

$$I_{\text{T1}} = \frac{1}{2} \mu_n C_{\text{OX}} \left( \frac{W}{L} \right)_{\text{DTFT}} (V_{\text{N1}} - V_{\text{DATA}} - V_{\text{TH\textunderscore DTFT}})^2 \quad \text{(3)}$$
where $V_{N1} - V_{DATA}$ is the gate-to-source voltage ($V_{GS}$) of the DTFT. Based on the principle of charge conservation, Equation (4) must be followed.

$$I_{CST} + I_{T1} = 0. \quad (4)$$

From Equations (2) and (3), Equation (4) can be derived as

$$\frac{1}{V_{N1} - V_{DATA} - V_{TH_{DTFT}}} = \frac{1}{2} \mu_h C_{OX} \left( \frac{W}{L} \right)_{DTFT} \left( \frac{1}{C_{ST}} \right) \tau + A \quad (5)$$

where $\tau$ is the total time of the discharging process as well as the programming period in the proposed circuit, and $A$ is the constant of integration. At the beginning of the discharging process, $\tau$ is equal to zero, and $V_{N1}$ is ELVDD; thus, the constant of integration, $A$, can be calculated as

$$A = \frac{1}{ELVDD - V_{DATA} - V_{TH_{DTFT}}} \quad (6)$$

Further, at the end of the discharging process, $\tau$ is the total programming time, and $V_{N1}$ is assumed to be discharged to $\beta \times (V_{DATA} + V_{TH_{DTFT}})$, where $\beta \geq 1$, representing the actual voltage of $V_{N1}$. Therefore, the formula for discharging period $\tau$ can be presented as

$$\tau = \frac{2L}{\mu_h C_{OX} W} \times C_{ST} \times \left[ \frac{1}{\beta(V_{DATA} + V_{TH_{DTFT}}) - V_{DATA} - V_{TH_{DTFT}}} - \frac{1}{ELVDD - V_{DATA} - V_{TH_{DTFT}}} \right] \quad (7)$$

Equation (7) shows that as the mobility of the DTFT or $V_{TH_{DTFT}}$ increases, the programming period can be reduced, which benefits high-refresh-rate driving. Furthermore, the storage capacitor $C_{ST}$ is proportional to the programming time; thus, a relatively small $C_{ST}$ is required for high-speed operation. To confirm the appropriate size of the storage capacitor used in the proposed 6T1C pixel circuit, a few LTPS driving TFT parameters and experimental data are required. The LTPS driving TFT had a geometry of 3 $\mu$m/10 $\mu$m, a threshold voltage of 1.5 V, mobility of 102 cm$^2$/Vs, and a 30 nm SiO$_2$ insulator $C_{OX}$ of 115 nF/cm$^2$. According to the simulation data, the parameter $\beta$ was approximately equal to 1.0054, while $V_{DATA}$ was $-0.1$ V when operating at the lowest gray level. Furthermore, to operate the proposed pixel circuit at 120 Hz with FHD resolution, the discharging time (data-inputting time) of the programming period must be less than the line-scanning time, which can be calculated as

$$\text{line - scanning time} = \frac{1 \text{ s}}{\text{frame rate} \times \text{FHD resolution}} \quad (8)$$
where ’FHD resolution’ represents the row number of the FHD resolution display, and the ’frame rate’ is 120 Hz. The discharging times of the proposed circuit have to be set below 7.716 µs for a frame rate of 120 Hz with an FHD resolution; as a result, the proposed storage capacitor \( C_{ST} \) must be limited as follows:

\[
7.716 \mu s > \frac{2L}{\mu C_{OX} W} \times C_{ST} \times \left[ \frac{1}{\beta(V_{DATA} + V_{TH_{DTFT}}) - V_{DATA} - V_{TH_{DTFT}}} - \frac{1}{ELVDD - V_{DATA} - V_{TH_{DTFT}}} \right] (9)
\]

In the calculation results of Equation (9), the storage capacitor \( C_{ST} \) needs to be lower than approximately 103 fF. As a result, we set 100 fF as the value of the proposed \( C_{ST} \).

4. Results and Discussion

LTPS and a-IZTO TFT devices were fabricated to validate the performance of the proposed 6T1C pixel circuit, and the measured and simulated transfer curves are shown in Figure 4. The a-IZTO TFTs, using a bottom-gate structure, can achieve a low leakage current. The LTPS TFTs, using a top-gate structure, are able to provide high carrier mobility and excellent current driving capability. The a-IZTO and LTPS TFTs used in the proposed pixel circuit were measured by a semiconductor parameter analyzer (HP 4145B) to obtain the transfer curves. Furthermore, the characteristics of the a-IZTO and LTPS TFTs were fitted by software to acquire the model parameters before the circuit simulation. The proposed circuit was simulated using AIM-Spice, and the parameters are listed in Table 1.

Herein, the storage capacitor \( C_{ST} \) is set to 0.1 pF to operate the proposed pixel circuit at an HFR of 120 Hz with FHD resolution. Furthermore, designing the Scan and Emm with the same voltage range reduces the complexity of GOA and is advantageous for narrow-bezel applications.

![Figure 4. Measured and simulated (a) LTPS TFT and (b) a-IZTO TFT transfer curves.](image)

Table 1. Specifications of proposed 6T1C pixel circuit.

| Parameter       | Value                      |
|-----------------|----------------------------|
| \((W/L)_{T1}\) (µm) | 3/10                       |
| \((W/L)_{T2}~\_T6\) (µm) | 3/3                       |
| \(C_{ST}\) (pF)   | 0.1                       |
| \(C_{OLED}\) (pF) | 0.4                       |
| Emission period for 120 Hz (ms) | 8.33                     |
| Emission period for 1 Hz (s)      | 1                         |

![Figure 5a](image)

Figure 5a shows the simulated transient waveforms of node N1 of the proposed pixel circuit operating at 120 Hz when \( V_{TH} \) variations in DTFT are −0.33, 0, and +0.33 V. Node N1 is reset to ELVDD (5 V) at the start of the operation and then discharged to approximately \( V_{DATA} + V_{TH} \) (3 V) with an input data voltage of 1.5 V after the programming period. Furthermore, the proposed circuit senses variations of 0.33 and 0.32 V, which are nearly equal to the actual variation of 0.33 V. Furthermore, at the end of the holding period, node N1 drops from 3 to 2.85 V due to the parasitic capacitance issue caused by clockfeedthrough effects. Figure 5b shows the simulated OLED currents versus data voltage...
from $-0.1$ to $1.9$ V for $\pm 0.33$ V DTFT threshold voltage shifts with an average error rate of 1.8%, demonstrating the proposed pixel circuit’s high compensating capability for threshold voltage variations when driven at 120 Hz.

Table 1. Specifications of proposed 6T1C pixel circuit.

| Parameter | Value |
|-----------|-------|
| (W/L) T1  | 3/10  |
| ELVDD (V) | 5     |
| (W/L) T2−T6 | 3/3 |
| ELVSS (V) | 0     |
| CST (pF)  | 0.1   |
| Scan, Em (V) | $-1$ to $5$ |
| OLED (pF) | 0.4 V |
| DATA (V)  | $-0.1$ to $1.9$ |
| Emission period for 120 Hz (ms) | 8.33 |
| Emission period for 1 Hz (s) | 1 |

Figure 5a shows the simulated transient waveforms of node N1 of the proposed pixel circuit operating at 120 Hz when $V_{\text{TH}}$ variations in DTFT are $-0.33$, 0, and $+0.33$ V. Node N1 is reset to ELVDD (5 V) at the start of the operation and then discharged to approximately $V_{\text{DATA}} + V_{\text{TH}}$ (3 V) with an input data voltage of 1.5 V after the programming period. Furthermore, the proposed circuit senses variations of 0.33 and 0.32 V, which are nearly equal to the actual variation of 0.33 V. Furthermore, at the end of the holding period, node N1 drops from 3 to 2.85 V due to the parasitic capacitance issue caused by clock-feed-through effects. Figure 5b shows the simulated OLED currents versus data voltage from $-0.1$ to $1.9$ V for $\pm 0.33$ V threshold voltage shifts with an average error rate of 1.8%, demonstrating the proposed pixel circuit’s high compensating capability for threshold voltage variations when driven at 120 Hz.

Figure 5. The (a) simulated transient waveforms of node N1 voltage operating at 120 Hz when $V_{\text{TH}}$ variations in DTFT are $-0.33$, 0, and $+0.33$ V. (b) Simulated OLED driving currents versus data voltage of the proposed 6T1C pixel circuit for $\pm 0.33$ V threshold voltage shifts of DTFT.

Figure 6 depicts the simulated voltage waveforms of node N1 operating at a low frame rate of 1 Hz when the $V_{\text{TH}}$ variations in the driving TFT are $-0.33$, 0, and $+0.33$ V. After the reset, programming, and holding operations, the voltage of node N1 ought to be sustained within the long period emission stage of 1 s. It can be seen that the voltage of node N1 is fine and holds that the maximum variation is about 0.23%. Furthermore, at the end of the emission period, the proposed circuit detects voltages of 0.328 V and 0.326 V, indicating that the proposed pixel circuit is highly resistant to DTFT threshold voltage variation when driven at a low frame rate of 1 Hz.

Figure 7a depicts the simulated OLED currents at the low gray level in the proposed circuit structure using all-LTPS TFTs or LTPO for a 1 s emission period. Within the long emission time, being lower than the ELVDD, the voltage of node N1 ($V_{\text{DATA}} + V_{\text{TH, DTFT}}$) is mainly charged by the path of the leakage current of T3. As a result, the OLED current increases dramatically as the voltage of node N1 rises. Because of the extremely low off-current characteristic of oxide TFTs, leakage currents can be limited in LTPO applications. Figure 7b depicts the simulated OLED currents emitting continuously for 1 s at various gray levels while the proposed 6T1C pixel circuit operates at a low frame rate of 1 Hz. The overall variations in OLED driving currents are less than 3.56 nA, indicating excellent stability when operating at a low frame rate of 1 Hz.
Figure 6. Simulated waveforms of the voltage of node N1 operating at 1 Hz when $V_{TH}$ variations in DTFT are $-0.33$ V, 0 V, and $+0.33$ V.

Figure 7. (a) Simulated OLED currents at the low gray level in the proposed circuit structure using all-LTPS TFTs or LTPO for a 1 s emission period. Within the long emission time, being lower than the ELVDD, the voltage of node N1 ($V_{DATA} + V_{TH_{DTFT}}$) is mainly charged by the path of the leakage current of T3. As a result, the OLED current increases dramatically as the voltage of node N1 rises. Because of the extremely low off-current characteristic of oxide TFTs, leakage currents can be limited in LTPO applications. (b) Simulated OLED currents emitting continuously for 1 s at various gray levels while the proposed 6T1C pixel circuit operates at a low frame rate of 1 Hz. The overall variations in OLED driving currents are less than 3.56 nA, indicating excellent stability when operating at a low frame rate of 1 Hz.

In addition, in Table 2, a comparison between the proposed and previously published pixel circuits demonstrates the advantages of the proposed 6T1C circuit, including a simple structure, a minimum number of signal lines, wide refresh rate support, and low voltage driving. The total number of signal lines, in this case, includes ELVDD, ELVSS, $V_{DATA}$,
Finally, based on the simulated results, it is confirmed that the proposed 6T1C pixel circuit has good performance when operating at various refresh rates ranging from 1 to 120 Hz, making it suitable for portable displays.

Table 2. Comparison between proposed and previously published pixel circuits.

| Reference          | This Study | Ref. [14] | Ref. [16] | Ref. [19] | Ref. [20] |
|--------------------|------------|-----------|-----------|-----------|-----------|
| Structure          | 6T1C       | 6T1C      | 7T1C      | 6T2C      | 7T1C      |
| Total signal lines | 5          | 8         | 7         | 7         | 6         |
| Frame rate         | 1–120 Hz   | 1–60 Hz   | 1–120 Hz  | 120 Hz    | 15–60 Hz  |
| Resolution         | 1920 × 1080| 368 × 448 | 1920 × 1080| 1920 × 1080| 320 × 360 |
| Power voltage (V_{DD} − V_{SS}) | 5 V       | N/A       | 7 V       | 4.8 V     | 6.6 V     |

The layout of the proposed pixel circuit using the method of line sharing is shown in Figure 8. The target display specifications in this paper are designed for portable applications, including full high-definition (FHD) resolution, a high ppi of 525, and 1 Hz to 120 Hz frame rate support. With the small subpixel dimension of 48.5 μm × 24.25 μm, it is believed to reach a high pixel density for portable applications.

Figure 8. The layout of the proposed 6T1C pixel circuit.

5. Conclusions

This paper proposes a new 6T1C pixel circuit for AMOLED portable displays based on LTPO technology that supports variable frame rates ranging from 1 to 120 Hz. To use it in narrow-bezel applications, identical switch-controlling signals can be used to reduce circuit complexity.
Furthermore, the proposed circuit could not only be driven with a low power voltage of 5 V but also be free of the OLED degeneration problem. According to the results of the calculation and analysis, the storage capacitor of the proposed circuit, being suitable for HFR driving, is chosen as 100 ff. The results of the simulation show that the average error rate of OLED currents with ±0.33 V threshold voltage variations in the DTFT is 1.8% in the HFR driving scheme (120 Hz); additionally, during low-frame-rate operation (1 Hz), the maximum shift of OLED currents at all gray levels is about 3.56 nA. As a result, the proposed pixel circuit can be successfully operated at a variety of refresh rates ranging from 1 to 120 Hz, which is advantageous for portable AMOLED displays.

**Author Contributions:** Conceptualization, C.-L.F. and S.-Y.L.; formal analysis, S.-Y.L.; software, S.-Y.L.; writing—original draft, S.-Y.L.; writing—review and editing, C.-L.F., C.-Y.C., S.-Y.L. and W.-Y.L. All authors have read and agreed to the published version of the manuscript.

**Funding:** The authors would like to acknowledge the financial support from the National Science Council (NSC) under Contract nos. NSC 110-2212-E-011-106-.

**Acknowledgments:** The corresponding author is grateful to H.-H. Wu, Syskey Technology Co., Ltd. (Taiwan), for his assistance in device fabrication. We also thank the National Center for High-performance Computing (NCHIC) of National Applied Research Laboratories (NARLabs) in Taiwan for providing computational and storage resources.

**Conflicts of Interest:** The authors declare no conflict of interest.

**References**

1. Tang, C.W. An overview of organic electroluminescent materials and devices. *J. Soc. Inf. Disp.* 1997, 5, 11–14. [CrossRef]
2. Choi, S.; Kang, C.M.; Byun, C.W.; Cho, H.; Kwon, B.H.; Han, J.H.; Yang, J.H.; Shin, J.W.; Hwang, C.S.; Cho, N.S.; et al. Thin-film transistor-driven vertically stacked full-color organic light-emitting diodes for high-resolution active-matrix displays. *Nat. Commun.* 2020, 11, 2732. [CrossRef] [PubMed]
3. Park, Y.-J.; Jung, M.-H.; Park, S.-H.; Kim, O. Voltage-Programming-Based Pixel Circuit to Compensate for Threshold Voltage and Mobility Using Natural Capacitance of Organic Light-Emitting Diode. *Ipn. J. Appl. phys.* 2010, 49, 03CD01. [CrossRef]
4. Vosniadis, P.; Siskos, S. A new threshold-voltage compensation technique of IGZO and LTPS for AMOLED display pixel circuit. In Proceedings of the 2017 Panhellenic Conference on Electronics and Telecommunications (PACET), Xanthi, Greece, 17–18 November 2017; pp. 1–4.
5. Watakabe, H.; Jinmai, T.; Suzumura, I.; Hanada, A.; Onodera, R.; Tada, M.; Mochizuki, K.; Tanaka, H.; Itô, T. 39-2: Development of Advanced LTPS TFT Technology for Low Power Consumption and Narrow Border LCDs. In SID Symposium Digest of Technical Papers; Wiley: Hoboken, NJ, USA, 2019; Volume 50, pp. 541–544.
6. Lin, C.-L.; Hung, C.-C.; Chen, P.-S.; Lai, P.-C.; Cheng, M.-H. New Voltage-Programmed AMOLED Pixel Circuit to Compensate for Nonuniform Electrical Characteristics of LTPS TFTs and Voltage Drop in Power Line. *IEEE Trans. Electron Devices* 2014, 61, 2454–2458. [CrossRef]
7. Fan, C.-L.; Chen, Y.-C.; Yang, C.-C.; Tsai, Y.-K.; Huang, B.-R. Novel LTPS-TFT Pixel Circuit with OLED Luminance Compensation for 3D AMOLED Displays. *J. Disp. Technol.* 2016, 12, 425–428. [CrossRef]
8. Lin, C.-S.; Chen, Y.-C.; Chang, T.-C.; Li, H.-W.; Chen, S.-C.; Jian, F.-Y.; Chuang, Y.-S.; Chen, T.-C.; Chen, Y.-C.; Tai, Y.-H. Analysis of Anomalous Capacitance Induced by TAGIDL in p-Channel LTPS TFTs. *J. Electrochem. Soc.* 2010, 157, H1003. [CrossRef]
9. Lin, C.-L.; Chang, J.-H.; Lai, P.-C.; Shih, L.-W.; Chen, S.-C.; Cheng, M.-H. Pixel Circuit With Leakage Prevention Scheme for Low-Frame-Rate AMOLED Displays. *IEEE J. Electron Devices Soc.* 2020, 8, 235–240. [CrossRef]
10. Im, C.; Kim, J.; Cho, N.-K.; Park, J.; Lee, E.G.; Lee, S.-E.; Na, H.-J.; Gong, Y.J.; Kim, Y.S. Analysis of interface phenomena for high-performance dual-stacked oxide thin-film transistors via equivalent circuit modeling. *ACS Appl. Mater. Interfaces* 2021, 13, 51266–51278. [CrossRef] [PubMed]
11. Lin, C.-L.; Lai, P.-C.; Chen, P.-S.; Wu, W.-L. Pixel Circuit With Parallel Driving Scheme for Compensating Luminance Variation Based on a-IGZO TFT for AMOLED Displays. *J. Disp. Technol.* 2016, 12, 1681–1687. [CrossRef]
12. Steudel, S.; van der Steen, J.-L.P.; Nag, M.; Ke, T.H.; Smout, S.; Bel, T.; van Diesen, K.; de Haas, G.; Maas, J.; de Riet, J.; et al. Power saving through state retention in IGZO-TFT AMOLED displays for wearable applications. *J. Soc. Inf. Disp.* 2017, 25, 222–228. [CrossRef]
13. Aman, M.; Takeda, Y.; Ito, K.; Yamamoto, K.; Tanaka, K.; Matsukizono, H.; Nakamura, W.; Makita, N. Reliability improvement of IGZO-TFT in hybrid process with LTPS. *J. SID.* 2021, 29, 416–427. [CrossRef]
14. Chang, T.-K.; Lin, C.-W.; Chang, S. 39-3: Invited Paper: LTOF TFT Technology for AMOLEDs. In SID Symposium Digest of Technical Papers; Wiley: Hoboken, NJ, USA, 2019; Volume 50, pp. 545–548.
15. Yonebayashi, R.; Tanaka, K.; Okada, K.; Yamamoto, K.; Yamamoto, K.; Uchida, S.; Nakamura, W. High refresh rate and low power consumption AMOLED panel using top-gate n-oxide and p-LTPS TFTs. *J. SID* 2020, 28, 350–359. [CrossRef]
16. Fu, J.; An, J.; Liao, C.; Liang, J.; Dai, C.; Zhang, X.; Zhang, S. P-17: Design of AMOLED Pixel Circuit Using LTPO TFTs with Enhanced Reliability. In *SID Symposium Digest of Technical Papers*; Wiley: Hoboken, NJ, USA, 2021; Volume 51, pp. 1116–1119.

17. Hsieh, H.H.; Tsai, T.T.; Chang, C.Y.; Hsu, S.F.; Chuang, C.S.; Lin, Y. Active-matrix organic light-emitting diode displays with indium gallium zinc-oxide thin-film transistors and normal, inverted, and transparent organic light-emitting diodes. *J. Soc. Inf. Disp.* 2011, 19, 323–328. [CrossRef]

18. Lai, P.-C.; Lin, C.-L.; Kanicki, J. Novel Top-Anode OLED/a-IGZO TFTs Pixel Circuit for 8K4K AM-OLEDs. *IEEE Trans. Electron Devices* 2018, 66, 436–444. [CrossRef]

19. Lin, C.-L.; Lai, P.-C.; Shih, L.-W.; Hung, C.-C.; Lin, T.-Y.; Liu, K.-H.; Wang, T.-H. Compensation Pixel Circuit to Improve Image Quality for Mobile AMOLED Displays. *IEEE J. Solid-State Circuits* 2018, 54, 489–500. [CrossRef]

20. Lin, C.-L.; Lai, P.-C.; Chang, J.-H.; Chen, S.-C.; Tsai, C.-L.; Koa, J.-L.; Cheng, M.-H.; Shih, L.-W.; Hsu, W.-C. Leakage-Prevention Mechanism to Maintain Driving Capability of Compensation Pixel Circuit for Low Frame Rate AMOLED Displays. *IEEE Trans. Electron Devices* 2021, 68, 2313–2319. [CrossRef]