AlGaN/GaN based high-electron mobility transistors (HEMTs) have been widely studied for microwave power applications, such as wireless base station and satellite communication owing to the high power handling capability at high frequencies for GaN devices.1-4 In modern wireless communication systems, multichannel transmissions are extensively used for signal transmission. During signal transmission, there are many operating frequencies and the neighboring frequencies are located closely to each other, hence the device used in this system will produce the intermodulation distortion and lead to the degradation of the system signal-to-noise ratio (SNR). Among all intermodulation distortions, third-order intermodulation distortion (IM3) dominates the linearity performance of the devices. Hence, IM3 performance is one of the most important criteria for evaluating device performance used in wireless communication systems.

Recently, improvement of linearity from the device level is attracting lots of attention. A nonlinearity transfer-function-based analysis method was used for the evaluation of device linearity.5 In order to reduce IM3, the transconductance needs to remain constant during all intermodulation distortions, and third order intercept point (IP3) suggests that the broader Gm distribution as a function of gate-bias, causes a lower IM3 level and higher IP3 values for the device. The improved device linearity demonstrates that dual-gate AlGaN/GaN HEMT design is a good approach for high-linearity RF device applications.

An effective method of improving the linearity of AlGaN/GaN HEMTs by using dual-gate technology is demonstrated. In this letter, we compare the DC characteristics and device linearity of the dual-gate AlGaN/GaN HEMTs with conventional single-gate AlGaN/GaN HEMTs. The correlation between the extrinsic transconductance (Gm) with third-order intermodulation distortion (IM3) and third order intercept point (IP3) suggests that the broader GaN distribution as a function of gate-bias, causes a lower IM3 level and higher IP3 values for the device. The improved device linearity demonstrates that dual-gate AlGaN/GaN HEMT design is a good approach for high-linearity RF device applications.

Experimental

The AlGaN/GaN HEMT heterostructure structure was grown by metal organic chemical vapor deposition (MOCVD) on SiC substrate. The epitaxial structure consisted of a AlN nucleation layer, 1.3 μm GaN buffer layer, 0.5 nm AlN spacer, and 22 nm undoped AlGaN barrier layer. The device fabrication began with mesa isolation of the active areas by inductively coupled plasma (ICP) etching using Cl2 based gas mixture. The ohmic contacts were formed by Ti/Al/Ni/Au metal stack which was deposited by electron beam evaporator and subsequently annealed by RTA at 800 °C for 1 min in N2 ambient. Then, the electron beam (EB) lithography with dual-layer photoresists was used for the fabrication of the single-gate and dual-gate devices. Ni/Au was deposited by electron beam evaporator as gate metal. Finally, the Si3N4 film was deposited by PECVD at 300 °C as passivation layer.

Fig. 1a shows the cross-sectional schematic of the conventional single-gate device structure. The gate-to-drain spacing LGD, gate-to-source spacing LGS, and gate length LG were 1.35 μm, 3.35 μm, and 0.3 μm, respectively. Fig. 1b shows the cross-sectional schematic of the dual-gate device structure. The gate-to-drain spacing LGD, gate-to-source spacing LGS, and gate length LG were 2.5 μm, 1.4 μm, 2.5 μm, and 0.3 μm, respectively. These two kinds of devices were fabricated by the same process and the single-gate device is referred as the control sample.

Results and Discussion

DC and RF measurements.—The output IDS–VDS characteristics of the single-gate and dual-gate devices are shown in Fig. 2. The IDS, (IDS = 0 V) for the 300 nm single-gate and 300 nm/300 nm dual-gate devices were 740 mA/mm and 620 mA/mm respectively. The relationship between the gate length and drain current has been reported.6 When the Schottky contact is deposited on the strained AlGaN/GaN heterostructures, the two-dimensional electron gas (2DEG) electrons under the Schottky contact are extracted to the empty surface donor states. It suggests that with the increased area of Schottky contact, more surface states of AlGaN barrier layer are affected by the electrons from the Schottky contact metal, and more 2DEG electrons are extracted to the empty surface donor states. Thus, the 2DEG sheet carrier concentration is decreased. Due to the larger schottky contact area of the dual-gate device, the 2DEG carrier concentration decreased, resulting in lower drain current for the dual-gate device.
Figure 1. (a) Schematic cross section of AlGaN/GaN HEMT with single-gate structure. (b) Schematic cross section of AlGaN/GaN HEMT with dual-gate structure.

Figure 2. I_Ds versus V_DS of single-gate and dual-gate GaN HEMTs.

Fig. 3 shows the I_Ds-V_GS curves of these two devices under study. It can be observed that the single-gate device has a higher pinch off voltage of −3.7 V and the dual-gate device has a lower pinch off voltage of −3.2 V, indicating the threshold voltage dependence on the gate length. As the device gate length reduced, the electron velocity overshoot effect becomes more significant because of there are more electrons travel ballistically. It can be observed that the slope of the I_Ds curve of single-gate device is higher than double-gate device at V_GS = −3 V to −2 V. This is due to the high electric field at the edge of gate, the high velocity electrons reduce the transit time and lead to higher drain current and transconductance. However, when increasing the gate bias to the positive voltage, the drain current of the dual-gate device increases in a stable rate owing to the fact that the second gate could effectively reduce the electric field, and thus suppress the electron overshoot effect. Therefore, the maximum currents of these two different types of devices reach almost the same value when biased at V_GS = 2 V and V_DS = 10 V.

The maximum extrinsic transconductance (G_m,max) of the single-gate and dual-gate GaN HEMTs were 174 mS/mm and 169 mS/mm, respectively, as shown in Fig. 4. The gate voltage swing (GVS) was defined as the 10% drop from the G_m,max. It can be observed that the dual-gate device has a larger GVS, suggesting a better linear behavior compared with the single-gate device. Fig. 5 shows the OFF-state drain leakage currents of the single-gate and dual-gate GaN HEMTs. There is an obvious reduction in the drain leakage current of the dual-gate device, indicating the electric field alleviated by the second gate.

The microwave small-signal performances were measured from 100 MHz to 50 GHz using an Agilent N5245A network analyzer. The S-parameter measurement system was calibrated using the standard LRRM calibration method. The single-gate device biased at V_GS = 10 V.
VGS = −3.3 V and VDS = 10 V. The current gain cutoff frequency (fT) and the maximum frequency of oscillation (fMAX) were 19.6 GHz and 64 GHz, respectively. The dual-gate device biased at VGS = −2 V and VDS = 10 V. The fT and fMAX were 18.4 GHz and 56 GHz, respectively.

**Linearity test.**—In order to investigate the device linearity performances, we used the polynomial curve fitting to the transfer characteristics of these devices. A polynomial equation was used to express device IDS-VGS transfer curves, as shown in the following:

\[
G_m(V_{GS}) = \frac{\partial I_{DS}(V_{GS})}{\partial V_{GS}} = a_1 + 2a_2V_{GS} + 3a_3V^2_{GS} + 4a_4V^3_{GS} + 5a_5V^4_{GS} + \ldots
\]

[1]

For a device with good linearity, IDS should increase linearly with VGS, therefore, \(a_1\) should be larger and the higher order constants should be minimized. The coefficients of these two kinds of devices extracted from the measurement data with VDS = 10 V are listed in Table I, and it is clearly observed that the dual-gate device has a larger \(a_1\) and smaller \(a_3/a_1\) and \(a_5/a_1\) values, indicating a better linearity for the dual-gate device.5,19

In addition, the relationships between IM3, IP3, and Gm, Gd are shown in Equation 2 and 3:

\[
IM3 \propto \left(\frac{G_m'}{G_m} \cdot R_L\right)^2 \cdot A^6
\]

[2]

\[
IP3 \propto \frac{(G_m)^3}{G_m' \cdot G_d \cdot R_L}
\]

[3]

where A is the signal amplitude, \(G_m'\) is the second derivative of the transconductance, and RL is the load impedance. It can be seen that the IM3 level is directly proportional to \((G_m'/G_m)^2\), while the IP3 value is inversely proportional to the \(G_m'\) and directly proportional to \((G_m)^3\). Therefore, a lower IM3 level can be achieved by increasing the flatness of the \(G_m\) distribution across the gate-bias region.5,6 As shown in Fig. 4, the dual-gate device has a flatter \(G_m\) curve, which leads to small absolute \(G_m'\) over a wide range of gate-source voltage shown in Fig. 6. As a result, the dual-gate device has lower IM3, indicating the device has a better linearity.7

To further evaluate the device linearity, the IM3 and IP3 measurements were performed by injecting two-tone signals at 6 GHz with an offset frequency of 1 MHz and VDS was set at 10 V. For the IP3 measurement, the load impedance was first tuned for maximum power for each individual device. Then, the IM3 was measured and plotted as a function of input power under given dc bias conditions. IP3 was determined by the intercept point of the Pout and IM3 curves after extrapolation. Fig. 7 shows the IP3 of these two kinds of devices with...
Table II. Comparison of the IP3 of single-gate and dual-gate GaN HEMTs.

| Device Type   | IDS bias point | P1dB(dBm) | IP3(dBm) | IP3- P1dB (dBm) | IP3/PDC |
|---------------|----------------|-----------|----------|-----------------|---------|
| Single-gate   | 50% IDSS       | 7.19      | 22.24    | 15.05           | 9.31    |
| Dual-gate     | 50% IDSS       | 11.05     | 26.56    | 15.51           | 14.37   |

Different bias currents. It can be observed that the dual-gate device has higher a IP3 value as compared to the single-gate device at a wide range of bias currents. The measured maximum IP3 values of single-gate and dual-gate device were 22.24 dBm and 26.56 dBm, respectively. In addition, the dual-gate device showed higher Δ/IP3-P1dB of 15.51 dB, and higher IP3 to DC power consumption ratio (IP3/PDC) of 14.37 as compared to the single-gate device (Table II).

Conclusions

In summary, the single-gate and dual-gate AlGaN/GaN HEMTs were fabricated, and the device DC performance and linearity were compared. Even though the single-gate device has higher IDSS and Gm,max, the dual-gate device shows much better device linearity with lower overall IM3 level and higher IP3 value. These results show the dual-gate GaN HEMTs have great potential to be used for future wireless communication systems.

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References

1. U. K. Mishra, P. Parikh, and Y.-F. Wu, Proc. IEEE, 90(6), 1022 (2002).
2. Y.-F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wissleder, U. K. Mishra, and P. Parikh, IEEE Electron Device Lett., 25(3), 117 (2004).
3. J. Khalil, A. Liero, M. Rudolph, R. Lossy, and W. Heinrich, IEEE Microw. Wireless Compon. Lett., 18(9), 605 (2008).
4. Y.-K. Lin, S. Noda, H.-C. Lo, S.-C. Liu, C.-H. Wu, Y.-Y. Wong, Q. H. Lac, P.-C. Chang, H.-T. Hsu, S. Samukawa, and E. Y. Chang, IEEE Electron Device Lett., 37(11), 1395 (2016).
5. Y.-C. Lin, E. Y. Chang, H. Yamaguchi, W.-C. Wu, and C.-Y. Chang, IEEE Trans. Electron Devices, 54(7), 1617 (2007).
6. J. Liu, Y. Zhou, R. Chu, Y. Cai, K. J. Chen, and K. M. Lau, IEEE Electron Device Lett., 26(3), 145 (2005).
7. J. Khalil, E. B. Treukel, F. Schneider, and J. Wierl, IEEE Trans. Electron Devices, 56(3), 361 (2009).
8. Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, and V. Sainnuganathan, IEEE Electron Device Lett., 31(8), 803 (2010).
9. C.-H. Hsu, W.-C. Shih, Y.-C. Lin, H.-T. Hsu, H.-H. Hsu, Y.-X. Huang, T.-W. Lin, C.-H. Wu, W.-H. Wu, J.-S. Maa, H. Iwai, K. Kakushima, and E. Y. Chang, Ipn. J. Appl. Phys., 55(4S), 04EG04 (2016).
10. T. Gao, R. Xu, Y. Kong, J. Zhou, C. Kong, X. Dong, and T. Chen, Appl. Phys. Lett., 2004(16).
11. J. S. Moon, R. Grabar, D. Brown, I. Alvarado-Rodriguez, D. Wong, A. Schmitz, H. Fung, P. Chen, J.-C. Kang, S. Kim, T. Oh, and C. Meguire, IEEE Electron Device Lett., 37(3), 272 (2016).
12. S.-E. Shih, W. R. Deal, D. M. Yamauchi, W. E. Sutton, W.-B. Luo, Y. Chen, I. P. Smorchkova, B. Heying, M. Wojtowicz, and M. Siddiqui, IEEE Trans. Microw. Theory Tech., 57(12), 3270 (2009).
13. Z. Lin and W. Lu, J. Appl. Phys., 99(1), 014504 (2006).
14. A. T. Ping, Q. Chen, J. W. Yang, M. A. Khan, and I. Adesida, IEEE Electron Device Lett., 19(2), 54 (1998).
15. T. Iide, M. Shimizu, A. Nakajima, M. Inada, S. Yagi, G. Piao, Y. Yano, N. Akutsu, H. Okumura, and K. Arai, Ipn. J. Appl. Phys., 46(4B), 2334 (2007).
16. Y. Awano, M. Koushi, K. Kosemura, T. Mimura, and M. Abe, IEEE Trans. Electron Devices, 36(10), 2260 (1989).
17. M. Singh, Y.-R. Wu, and J. Singh, IEEE Trans. Electron Devices, 52(3), 311 (2005).
18. C.-H. Chen, R. Cottif, K. Krishnamurthy, S. Keller, M. Rodwell, and U. K. Mishra, IEEE Electron Device Lett., 21(12), 549 (2000).
19. H.-C. Chiu, S.-C. Yang, F.-T. Chien, and Y.-J. Chan, IEEE Electron Device Lett., 23(1), 1 (2002).