Efficient CNOT Synthesis for NISQ Devices

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(Abstract—In the era of noisy intermediate-scale quantum (NISQ), executing quantum algorithms on actual quantum devices faces unique challenges. One such challenge is that quantum devices in this era have restricted connectivity: quantum gates are allowed to act only on specific pairs of physical qubits. For this reason, a quantum circuit needs to go through a compiling process called qubit routing before it can be executed on a quantum computer. In this study, we propose a CNOT synthesis method called the token reduction method to solve this problem. The token reduction method works for all quantum computers whose architecture is represented by connected graphs. A major difference between our method and the existing ones is that our method synthesizes a circuit to an output qubit mapping that might be different from the input qubit mapping. The final mapping for the synthesis is determined dynamically during the synthesis process. Results showed that our algorithm consistently outperforms the best publicly accessible algorithm for all of the tested quantum architectures.

Index Terms—quantum circuit, qubit routing, CNOT synthesis

I. INTRODUCTION

Compositions of CNOT gates on a n-qubit circuit can be represented as \( n \times n \) invertible matrices in \( \mathbb{F}_2 \). Under this representation, a single CNOT gate is simply an elementary matrix, an identity matrix with one off-diagonal entry set to 1. Based on this observation, any parity matrices can be decomposed into a sequence of CNOT gates through Gaussian elimination. Those techniques revealed a new approach for quantum circuit optimization, a task that is critical in the era of NISQ where the feasibility of quantum computing depends heavily on circuit complexity. Additionally, the current physical limits for quantum computers impose a further constraint. Although the theoretical mathematical model for quantum circuits allows interactions between any qubits, the currently available quantum computer architectures only allow specific pairs of qubits to interact. In this study, we present a heuristic method called the token reduction method for synthesis CNOT circuits for any connected architectures. This method not only outperforms the current testable benchmark, but also possess the desired characteristics for routing general quantum circuits.

A. Structure

In Section II, we introduce the background for the qubit routing problem, and show how CNOT synthesis can be used to solve this. In Section III, we first show how we can route a circuit to a different output mapping, then we propose a new representation called the row graph to work with qubit routing problems. Finally, in Section IV we introduce the token reduction methods.

II. BACKGROUND

A. The Quantum Circuit Model

The quantum circuit model is one of the most common ways to represent quantum computation. They are also widely used as models for all quantum processes such as quantum computation, quantum communication, and even quantum noise [2]. Like classical circuits, quantum circuits consist of wires and logic gates. However, a major departure from classical logic gates is that the quantum gates describe only unitary linear maps.

Quantum circuits are direct analogs to classical logical circuits, and this means we can interpret a quantum circuit as a “flow” of computation, with the gates acting as operations and the wires indicating the next steps. As a general understanding, a computation starts at the left end of the circuit with some input qubits, and produce the result at the right end of the circuit.

Example II.1. A Hadamard gate \( H = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \) is a linear map:

A CNOT (Controlled NOT) gate \( \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix} \) is a linear map:

1All graphs in this thesis are generated using TikZiT, available at https://tikzit.github.io/
the black dot is called the control, and the white dot with a cross inside is called the target. The following circuit computes the unitary linear map:

\[
U := (I \otimes H) \circ \text{CNOT} \circ (H \otimes I)
\]

![Fig. 1. A simple quantum circuit](image)

### B. NISQ

The theories around quantum information and quantum computing are relatively well established, but the quantum computers themselves are still far from ready. In order to run a quantum algorithm such as the Shor’s factoring algorithm, it requires a quantum computer that is fault-tolerant. Even though quantum technology has advanced rapidly in recent years, we still have a long way to go before achieving fault-tolerant quantum computing. Apart from the qubits needed for computing the algorithms, a fault-tolerant quantum computer also requires millions of qubits as overhead for error correction [3]. In comparison, the most recent quantum computer revealed by IBM only has 53 qubits.

Fault-tolerant quantum computers are still far away, but that is not to say the current or near-future quantum computers are not useful. In fact, some important milestones can potentially be reached by these devices such as the first demonstration of quantum computers solving a problem that is infeasible for classical computers \(^2\). Preskill [5] called these quantum computers, the noisy intermediate-scale quantum (NISQ) devices.

Other than the most noticeable issue of not having quantum error correction (i.e., not fault-tolerant), these NISQ devices also have other limitations. Firstly, the error rate for quantum gates are significantly high. The overall fidelity of computations on NISQ devices is directly affected by the depth of the circuits; the computations get noisier as the circuits get deeper [5].

Secondly, these devices have restricted connectivity such that any two-qubit quantum gate must satisfy certain topological restrictions; this usually means that a two-qubit gate can only be applied to a pair of adjacent qubits and with a certain direction.

Figure II-B shows the IBM QX5 architecture, which uses CNOT gates as the only allowed two-qubit gates; the edges indicate the connectivity between qubits, and the arrows indicate the allowed directions for CNOT gates. For example, the pair \((Q1, Q2)\) only allows CNOT gates whose control acts on \(Q1\) and whose target acts on \(Q2\).

\(^2A\) recent work claimed that this milestone had been achieved; however, whether the claim is true is still in debate [4]

### C. Qubit Routing

We mentioned that the NISQ devices have restricted connectivity:

1. A two-qubit gate can only be applied to adjacent qubits.
2. A two-qubit gate can only be applied to adjacent qubits with certain directions.

In this paper, however, we will only consider the first constraint. The second constraint is specific to CNOT gates, and it can usually be solved by the Equation (1) after the first constraint is met through compilation. Nevertheless, the gate direction constraint can still be an important factor to consider when we design methods to solve the first constraint; we will discuss this in Section VI-B. As a result, we will define quantum architectures as undirected graphs in Definition II.1, instead of the one shown in Figure II-B.

\[
\begin{align*}
\begin{array}{c}
IQX5\text{Architecture Graph}\\
\end{array}
\end{align*}
\]

Before we demonstrate why the restricted connectivity can be an issue, let’s explain how a quantum circuit can be applied to a quantum computer. Firstly, let’s define a quantum computer architecture in terms of graphs.

**Definition II.1 (Architecture Graph).** An architecture graph is an undirected connected graph \(G(V, E)\), such that each node represents a qubit, and each edge represents a connection.

**Remark II.1.** The usage of the term qubit is sometimes confusing. In this thesis, we use the term qubit or node for the physical nodes on quantum computers. We use logical qubit or wire for the wires in quantum circuits.

A quantum circuit must be mapped to a an architecture graph before it can be executed. Therefore, we define the following:

**Definition II.2 (Mapping).** Given a quantum circuit with \(n\) wires \(W = \{w_1, w_2 \cdots w_n\}\), and an architecture graph \(G(V, E)\) with \(|V| = n\), a mapping is a bijective function:

\[
f : W \rightarrow V
\]

In the following example, we illustrate how a quantum computer computes a circuit.

**Example II.2.** Consider the following architecture graph \(G\), the mapping \(M\) and circuit \(c\).

![Example II.2](image)
When given a set of inputs, the quantum device whose architecture is represented by $G$ computes $c$ with mapping $M$ as follows:

$$M = \begin{cases} w_1 \mapsto Q_1 \\ w_2 \mapsto Q_2 \\ w_3 \mapsto Q_3 \\ w_4 \mapsto Q_4 \end{cases}$$

When given a set of inputs, the quantum device whose architecture is represented by $G$ computes $c$ with mapping $M$ as follows:

$$|0\rangle \quad |1\rangle \quad |1\rangle \quad |1\rangle \quad$$

compute

is the Pauli X gate, whose matrix is $\begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$

In Example II.2, the architecture $G$ computes the circuit $c$ with mapping $M$ without any issue. However, $G$ cannot compute with the following mapping $M'$ as shown in Figure II-C. The first CNOT gate acts on the qubits $Q_1, Q_4$, which are not adjacent.

$$M' = \begin{cases} w_1 \mapsto Q_1 \\ w_2 \mapsto Q_4 \\ w_3 \mapsto Q_3 \\ w_4 \mapsto Q_2 \end{cases}$$

However, this circuit can still compile with mapping $M'$ by inserting SWAP gates. A SWAP gate is a linear map that swaps qubits between two wires.

$$SWAP = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix}$$ (2)

Remark II.2. The circuit $c$ shown in Example II.2 can always be compiled with architecture $G$ with an appropriate initial mapping without using any routing. However, this is not always possible as the circuit can get very large. Suppose another CNOT gate acting on $(w_1, w_4)$ is added to $c$, then one can verify that no initial mapping is sufficient for the circuit to compile with $G$ if no extra routing is performed. Nevertheless, selecting an optimal initial mapping that minimizes the number of SWAP gates is an NP-hard problem [6], and it is shown that the gate count in a routed circuit is very sensitive to the initial mapping. Hence optimizing initial mapping is often a very important task for any routing algorithms.

An important observation is that the circuit $c'$ and our original circuit $c$ do not compute the exact same function. In
fact, the SWAP gate only changed the mapping of the output, and the output mapping is:

\[
M'_1 = \begin{cases} 
    w_3 \mapsto Q1 \\
    w_2 \mapsto Q4 \\
    w_1 \mapsto Q3 \\
    w_4 \mapsto Q2 
\end{cases}
\]

This change of mapping can be understood as the computation result being output with a permutation that differs from the input’s permutation. This is a totally acceptable behavior because quantum gates are expensive, and we are better off re-ordering the results in a classical way after the quantum computation.

Since a routed circuit is still equivalent to the original circuit if only the output mappings are different, we define quantum circuit routing procedures as the following.

**Definition II.3.** A circuit routing procedure is defined as:

Given a \( n \)-wire quantum circuit \( c \), and a \( n \)-qubit architecture graph \( G \). Outputs a \( n \)-qubit circuit \( c' \), an initial mapping \( M_0 \) and a output mapping \( M_t \) satisfying:

1) \( c' \) complies with \( G \) with mapping \( M_0 \).
2) \( c' \) is equivalent to \( c \) with the results mapped by \( M_t \).

Since the fidelity of computation is critically affected by the depth of the circuits in the NISQ era, the most crucial goal for a routing procedure is to minimize the number of gates.

**D. CNOT Synthesis**

A universal gate set for quantum computing often contains one choice of two-qubit gates and some single-qubit gates. Usually, CNOT gates are used as the choice for primitive two-qubit gates. For example, in IBM Q devices, CNOT gates are the only allowed two-qubit gates; all other two-qubit gates need to be converted to CNOTs before applying. In particular, SWAP gates and CZ gates can be converted to CNOT gates by the following equations:

\[
\begin{align*}
\text{CZ} &= \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \\
\text{SWAP} &= \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}
\end{align*}
\]

(3)

(4)

Treating CNOT as the only two-qubit gates not only simplifies the qubit routing problem as we can partition the two-qubit gates into blocks of CNOT sub-circuits, but also opened a entirely new perspective. CNOT gates alone form a very important subclass of quantum circuits called the linear reversible classical circuits [1]. This type of circuits implements all linear reversible functions \( f : \mathbb{F}_2^n \rightarrow \mathbb{F}_2^n \), where \( n \) is the number of wires. In other words, all CNOT circuits with \( n \) wires can be represented as an invertible \( n \times n \) matrix in \( \mathbb{F}_2 \). This representation allows us to generate a CNOT circuit from a matrix using matrix decomposition methods such as Gaussian eliminations. We call this gate generation procedure **CNOT synthesis**.

A CNOT gate in classical circuits has the following truth table:

| Input | Output |
|-------|--------|
| control | target | control | target |
| 0 0 | 0 0 |
| 0 1 | 0 1 |
| 1 0 | 1 1 |
| 1 1 | 1 0 |

Fig. 6. CNOT Truth Table

Considering CNOT gates as classical linear reversible operators gives us a different matrix representation than the one shown in Example II.1. In this new representation, CNOT gates are surprisingly just **elementary matrices**. That is, an \( n \times n \) identity matrix with an additional off-diagonal entry set to 1. For example:

\[
\begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 1 \end{pmatrix} \sim 
\]

\[
\begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 1 \end{pmatrix} 
\]

**Theorem II.1.** Given an \( n \)-wire CNOT circuit with wires ordered by \([0, 1, \cdots, n-1]\), a CNOT gate whose control placed on the \( c_{th} \) wire and target placed on the \( t_{th} \) wire is represented by a \( n \times n \) identity matrix with an additional off-diagonal 1 in the \((t, c)\) entry, that is, the \( c_{th} \) column and \( t_{th} \) row.

Therefore, we can treat each CNOT gate as an elementary row operation.

**Theorem II.2.** The action of a CNOT gate, whose control is on the \( c_{th} \) wire and target is in the \( t_{th} \) wire, is an elementary row operation on a \( n \times n \) matrix on \( \mathbb{F}_2 \), which adds the \( c_{th} \) row to the \( t_{th} \) row.

The following two theorems serve as the foundation for the concept of CNOT synthesis.

**Theorem II.3.** Any classical linear reversible circuit can be synthesized by a sequence of CNOT gates.

**Proof.** For a classical linear reversible circuit with \( n \) wires, suppose it is represented by a \( n \times n \) matrix \( A \) in \( \mathbb{F}_2 \). Then by the fact that any invertible matrix can be reduced to an identity matrix by using row operations, \( E_k E_{k-1} \cdots E_1 A = I \) where \( \mathbb{F}_2 \) is the Galois field of two elements \( \{0,1\} \).
$E_j$ is an elementary matrix. Hence $A = E_1^{-1} \cdots E_{k-1}^{-1} E_k^{-1}$. But since these elementary matrices are self-inverse in $F_2$ (i.e. $E^{-1} = E$), we obtain $A = E_1 \cdots E_{k-1} E_k$.

That is, we construct a CNOT circuit from $A$ by adding the CNOT gates corresponding to $E_1 \cdots E_{k-1} E_k$ in reverse order.

**Remark II.3.** The fact that elementary matrices in $F_2$ are self-inverse is also an important aspect for quantum circuit optimization as gate cancellation is often the easiest way to reduce gate count. The reduction is achieved by the identity shown in Equation (5).

$$
\begin{array}{c}
\textbullet \\
\textbullet \\
\end{array} = 
\begin{array}{c}
\textbullet \\
\textbullet \\
\end{array}
\quad (5)
$$

**Theorem II.4.** The upper bound for the number of CNOTs needed to synthesize any $n$-wire classical linear reversible circuit is $\Omega(n^2 / \log(n))$ [11].

**Proof.** For a given linear reversible circuit with $n$ wires, let $d$ be the number of CNOT gates needed for synthesis the circuit. We know that there are $n(n-1)$ different placements for each CNOT, hence there are in total $(n^2-n)^d$ different CNOT circuits. Because there are $O(2^{n^2})$ different linear maps for the original circuit (i.e. $2^{n^2}$ different $n \times n$ matrices), we need $(n^2-n)^d \geq 2^{n^2}$. Take log for both sides we have $d \log(n^2-n) \geq n^2$, hence $d \geq n^2 / \log(n^2-n) = \Omega(n^2 / \log(n))$.

**Theorem II.3** demonstrates how we can synthesis a CNOT circuit from any classical linear reversible circuit. At this point, these theorems at least give us an idea of how a given CNOT circuit can be potentially optimized through synthesis. If a given CNOT circuit has a very large number of gates, there is a good chance that there is an equivalent but smaller circuit.

The methods for CNOT synthesis without connectivity constraints are well researched. Patel et al. [11] show that the upper bound in Theorem II.4 can be achieved through an optimized version of LU decomposition. A standard framework for how synthesis work is illustrated in Algorithm 1.

**Algorithm 1: Template for CNOT Synthesis**

**Input:** Classical reversible circuit $c$

1. Construct an empty circuit $c'$;
2. Construct a matrix $P$ from $c$ by composing the matrices representing the gates;
3. Perform matrix decomposition on $P$ using only row operations until an identity matrix is reached. Add the CNOT gates corresponding to each row operation to $c'$ in reverse order (i.e. from right to left);
4. **return** $c'$

Theorem II.2 states that composing a CNOT gate to a classical linear reversible circuit is equivalent to performing an elementary row operation to the matrix representation of the circuit. When connectivity is an issue, however, it poses a constraint on which row operations are allowed. We need to decompose a matrix to identity using only allowed row operations implied by an architecture graph (Definition II.1); otherwise, the resulting CNOT circuit may not be compatible with the architecture due to invalid connectivities.

**Definition II.4** (Constrained CNOT synthesis). A constraint CNOT synthesis procedure is defined as:

Given a $n$-wire CNOT circuit $c$, and a $n$-qubit architecture graph $G$. Outputs a $n$-qubit circuit $c'$, an initial mapping $M_0$ and a output mapping $M_t$ satisfying:

1) $c'$ complies with $G$ with mapping $M_0$,  
2) $c'$ is equivalent to $c$ with the results mapped by $M_t$.

Two recent independent works [7] [8] efficiently solve the constrained CNOT synthesis problem using a method called Steiner Gauss. Roughly speaking, they innovate to use Steiner trees (Definition II.5) to perform LU decomposition with only the row operations specified by a target architecture. Steiner Gauss achieves an $\Omega(n^2)$ upper bound for the number of CNOT gates generated and runs efficiently fast (i.e., $O(n^3)$). Noticeably, the work done by Kissinger and Van de Griend shows a significant improvement in gate count comparing to two SWAP insertion based techniques [9] [10], in some of the test circuits, the Steiner Gauss method results in more than 80% savings against the other two techniques. This discovery opens a new door for using CNOT synthesis as a way to solve the qubit routing problem.

**Example II.3.** The following circuit:

![Fig. 7. Original circuit](image)

has a synthesized circuit

![Fig. 8. Synthesized circuit](image)
**Definition II.5 (Unweighted Rooted Steiner Tree).** Let $G = (V, E)$ be an unweighted, undirected graph, and let $S \subseteq V$ be a subset of vertices containing a root node $u$, called the terminals. A Steiner tree is a tree $(V_T, E_T)$ in $G$ that spans $S$ with root $u$. We also call the set of vertices $V_T \setminus V$ the Steiner points.

**Remark II.4.** Finding the optimal Steiner Tree is an NP-complete problem, we give an simple heuristic algorithm that uses the Floyd-Warshall algorithm in Appendix A.

### III. Preliminaries

The Steiner Gauss method works great for CNOT only quantum circuit; however, it does not work very well if applied naively to a general circuit.

Let’s consider a circuit with only a single CNOT $g$. Inserting SWAP gates is essentially trying to compute $g$ to a different output mapping. However in many cases, a circuit synthesized using the Steiner Gauss method for $g$ resembles a circuit that firstly computes $g$ to a different output mapping and then reverts the output to the original mapping (see Example III.1). Therefore, if CNOT gates are sparse, which is common for quantum circuits, any synthesis methods whose result has the same input and output mapping could perform too many unnecessary mapping reversions hence increasing gate count.

CNOT synthesis has the potential benefit of computing an arbitrary function $f$ with a small set of CNOTs; this is why when a CNOT block is large, the Steiner Gauss method performs better even though it still has unnecessary mapping reversion. However, when the block is small, synthesis without change mappings is unlikely to generate a smaller set of CNOTs.

In this study, we introduce an efficient CNOT synthesis method that produces a routed circuit according to an architecture that is equivalent to the original circuit up to an output mapping.

**Example III.1.** Consider the following mapped circuit.

![Original circuit](image9.png)

Routing the circuit through SWAP insertion can give us the following (recall from (4), a SWAP gate can be converted to three consecutive CNOT gates.):

![Routing with SWAP](image10.png)

The CNOT synthesis method can give us the following:

![Routing with CNOT synthesis](image11.png)

but notice, this circuit is equivalent to the following based on the identity (5):

![Routing with CNOT synthesis (2)](image12.png)

### A. Matrix Decomposition to a Permutation Matrix

**Theorem III.1.** A CNOT circuit can be synthesized to a different mapping by left-multiply its associated matrix with the transpose of a permutation matrix and then perform the synthesis.

**Definition III.1 (Permutation Matrix).** A permutation matrix is a square matrix obtained by permuting the columns of an $n \times n$ identity matrix according to some permutation $\pi$.

**Example III.2.** Suppose there is a $n \times n$ matrix $P = \begin{pmatrix} p_{1,1} & p_{1,2} & \cdots & p_{1,n} \\ p_{2,1} & p_{2,2} & \cdots & p_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ p_{n,1} & p_{n,2} & \cdots & p_{n,n} \end{pmatrix}$. We want to transform $P$ to $P'$ such that:...
That is, we want to change the output permutation from
[1 2 3 ... n] to [2 n 3 ... 1]. This change of permutation is
represented uniquely by the following permutation matrix:

\[
m = \begin{pmatrix}
0 & 0 & \cdots & 1 \\
1 & 0 & \cdots & 0 \\
\vdots & \vdots & \ddots & \vdots \\
0 & 1 & \cdots & 0
\end{pmatrix}
\]

Notice that \(P' = m^T \cdot P\)

This utilization of permutation matrices leads to a more
general routing procedure shown as Algorithm 2.

### Algorithm 2: General Qubit Routing with CNOT Synthesis

**Input:** A quantum circuit \(c\)

**Output:** A quantum circuit \(c'\), an initial mapping \(M_0\),
and output mapping \(M_t\)

1. Optimize an initial mapping \(M_0\);
2. Initialize \(c'\) to an empty circuit;
3. Partition \(c'\) into blocks of gates such that each block
   contains only CNOT gates or one-qubit gates;
4. \(M_t \leftarrow M_0\);
5. while next block of gates \(B\) in \(c'\) do
   if \(B\) fits \(M_t\) then
     add \(B\) to \(c'\); continue
   else
     Find an optimal mapping \(M'\);
     Synthesize \(B\) to \(B'\) that has an output mapping
     \(M'\);
     \(M_t \leftarrow M'\) Add \(B'\) to \(c'\);
   end
6. return \(c', M_0, M_t\)

Finding such mapping has a \(n!\) search space. We want a
synthesis procedure to decide an output permutation on the fly. The following theorem shows that it is possible.

**Theorem III.2** (Decomposition to a permutation matrix).
Suppose \(P\) is the matrix representing a CNOT circuit
with respect to the original permutation. Let \(m\) be a permutation
matrix associated with some permutation \(\pi\). We can synthesize
\(P\) to the permutation \(\pi\) by decomposing \(P^T\) to \(m^T\).

**Proof.** If we synthesize \(P^T\) to \(m^T\) then,

\[
P^T = E_1 \cdot E_2 \cdot \cdots \cdot E_n \cdot m^T
\]

\[
\implies P^T \cdot m = E_1 \cdot E_2 \cdot \cdots \cdot E_n \cdot m^T
\]

That is, we effectively obtain a decomposition of \(m^T \cdot P\)
(see Theorem III.1) by decomposing \(P^T\) to \(m^T\). Then, we can
add the CNOT gates associated with \(E_1^T, E_2^T, \ldots, E_n^T\) one
by one to the circuit. Notice that the transpose of \(m\) to a CNOT
matrix represents a CNOT gate with the control and target
switched.

Next, we give an example of how above theorem works.

**Example III.3.** Consider the following circuit \(c\) with a mapping
\(M\) to an architecture \(G\)

\[
M = \begin{cases}
  w_0 \mapsto A \\
w_1 \mapsto B \\
w_2 \mapsto C \\
w_3 \mapsto D
\end{cases}
\]

\(G = \begin{array}{ccc}
A & B \\
\hline
C & D
\end{array}\)

Hence the circuit \(c\) corresponds to the following permuted matrix \(P\)

\[
P = \begin{pmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{pmatrix}
\]

And

\[
P^T = \begin{pmatrix}
1 & 0 & 1 & 1 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 1 \\
0 & 0 & 0 & 1
\end{pmatrix}
\]

The objective is to decompose \(P^T\) to some transposed per-
mutation matrix \(m^T\) with only row operations allowed by the
connectivity in $G$. In order to work on this task, it is visually easier if we represent $P^T$ and $G$ together such that each row of $P^T$ is placed on a node in $G$.

\[(P^T, G) \simeq \]

\[
\begin{pmatrix}
1 & 0 & 1 & 1 \\
0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 \\
0 & 0 & 1 & 1
\end{pmatrix}
\begin{pmatrix}
\begin{array}{cccc}
A & B & D & C
\end{array}
\end{pmatrix}
\]

*Recall a swap is simply three consecutive row operations in $\mathbb{F}_2$ (i.e. Equation (4)). Hence $P^T$ has the following decomposition:*

\[
P^T = \begin{pmatrix}
1 & 1 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{pmatrix}
\begin{pmatrix}
1 & 0 & 0 & 0 \\
1 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{pmatrix}
\begin{pmatrix}
1 & 1 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{pmatrix}
\begin{pmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 1 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{pmatrix}
\begin{pmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{pmatrix}
\]

Finally, we construct a new circuit $c'$ following the procedure in Theorem III.2.

\[
c' = w_0 \quad w_1 \quad w_2 \quad w_3
\]

Observe the the permutation of the output mapping is indicated by the permutation matrix $m$.

In the above example we assign each row vector in a matrix to its corresponding node to have a more visually intuitive model to work with. In the next section, we formally define this representation and replace row vectors by the sums of the standard basis vectors.

**B. Row Graph**

**Definition III.2** (Row Graph). A row graph is a triple $(G, P, f)$, where

1) $P$ is a $n \times n$ matrix
2) $G(V, E)$ is a connected undirected graph such that $|V| = n$.
3) $f : V \rightarrow P_{rows}$ is an assignment function, where $P_{rows}$ is the set of row vectors in matrix $P$.

Furthermore, each row vector is represented as a sum of the standard basis vectors. For example, $(1 \ 0 \ 1 \ 0)$ is represented as $e_0 + e_2$, where $e_i$ is the standard basis vector.
in $\mathbb{F}_2^n$ with $i_{th}$ entry set to 1 and 0 elsewhere. We also denote $size(f(u))$ to be the number of ones in a row vector $f(u)$.

Example III.4. The following is a row graph where $V = \{A, B, C, D\}, P = \begin{pmatrix} 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 \end{pmatrix}$.

Moreover, we rename the elementary row addition operation as the node addition operation to suit our new representation.

Definition III.3 (Node addition operation). Given two nodes $u, v$ on a node graph and an assignment function $f$, we define the node addition operation as $f(u) \leftarrow f(u) + f(v)$. Recall this is the addition in $\mathbb{F}_2$.

Remark III.1 (Swap on row graphs). A swap operation is also an very important operation on row graphs. For any two nodes $u, v$, $Swap(u, v)$ can be performed by $f(u) \leftarrow f(u) + f(v)$, $f(v) \leftarrow f(u) + f(v)$ and $f(u) \leftarrow f(u) + f(v)$. $swap(u, v)$ can be also performed by $f(v) \leftarrow f(u) + f(v)$, $f(u) \leftarrow f(u) + f(v)$ and $f(v) \leftarrow f(u) + f(v)$.

Additionally, we define a special class of row graphs.

Definition III.4 (Reversible Row Graph). A row graph $(G(V, E), P, f)$ is called reversible if and only if $P$ is invertible.

Finally, we define another class of row graphs called basic row graph. For instance, a permutation matrix is represented by a basic reversible row graph.

Definition III.5 (Basic form). A row graph $(G(V, E), P, f)$ is called basic if and only if $size(f(u)) = 1$ for all $u \in V$.

Example III.5. Example of a basic reversible row graph.

C. The Token Reduction Problem

When using the row graph representation, we can treat each standard basis vector as a token. Under this perspective, the task of decomposing a matrix in $\mathbb{F}_2$ can be visualized as reducing tokens on the row graph such that each node only has one token.

Definition III.6 (Token Reduction). We define the Token Reduction problem being the decision problem of whether a row graph can be reduced to a basic row graph only by the adjacent node addition operations.

Theorem III.3. If a row graph is reversible, then it can be reduced to a basic graph.

Proof (Sketch). This is equivalent to the constrained CNOT synthesis problem. The Steiner Gauss method can decompose any invertible $\mathbb{F}_2$ matrix given the architecture graph is connected. A row graph is a connected graph by Definition III.2.

Definition III.7 (Opt Token Reduction). We also define the optimization version of the Token Reduction problem as Opt Token Reduction, which asks for the smallest sequence of row operations on adjacent nodes that transforms a given row graph to a basic row graph.

Theorem III.4. Opt Token Reduction is NP-hard for reversible row graphs.

Proof (Sketch). It is known that the Swap Minimization Problem is NP-hard [6]. Token reduction for reversible row graph solves the Swap Minimization Problem.

Remark III.2. In this section, we proposed to reframe the constrained CNOT synthesis problem as token reduction on reversible row graphs. Although the two problems are equivalent, the token reduction representation provides us with a way to treat the constrained synthesis problem with more unity. In other words, instead of treating such problems as synthesis with graphical constraints, we should treat them as synthesis on graphs.

IV. Token Reduction Methods

We will spend the first two subsections to establish the theorems supporting the token reduction method and give an upper bound for the Opt Token Reduction problem for reversible row graphs. In Subsection IV-B, we present an
A. Tree Reduction

The primitive operation on a row graph is the node addition operation. We want to develop a strategy that only uses node additions to reduce a row graph. In this section, we construct an abstraction of row additions called tree reduction, which serves as the base operation for our task on hand.

Firstly, we prove a critical lemma, which states that any node on a reversible row graph can be reduced to a single standard basis vector by a linear combination with other nodes under node addition.

Lemma IV.1. For any \( u \in V \) in a reversible row graph \((G(V, E), P, f)\) where \( P \) is an \( n \times n \) matrix, there exists a standard basis vector \( y \in \mathbb{F}_2^n \) and a set of nodes \( V' \subseteq V \) containing \( u \), such that \( \sum_{v \in V'} f(v) = y \).

Proof. Suppose \( V = v_1, v_2, \ldots, v_n \), and \( r_0, \ldots, r_{n-1} \) are the row vectors in \( P \). Now, to prove our lemma for the case \( f(u) = r_k \) is equivalent to prove that there exists a standard basis vector \( y \) such that the following equation has a solution with \( x_k = 1 \). Let’s denote \( r_{i,j} \) as the \( j^{th} \) entry of \( r_i \).

\[
\begin{pmatrix}
  r_{0,0} & \cdots & r_{k,0} & \cdots & r_{n-1,0} \\
  \vdots & \cdots & \vdots & \cdots & \vdots \\
  r_{0,n-1} & \cdots & r_{k,n-1} & \cdots & r_{n-1,n-1}
\end{pmatrix}
\begin{pmatrix}
  x_0 \\
  x_1 \\
  \vdots \\
  x_k \\
  x_{n-1}
\end{pmatrix} =
\begin{pmatrix}
  y_0 \\
  y_1 \\
  \vdots \\
  y_k \\
  y_{n-1}
\end{pmatrix} \tag{7}
\]

Furthermore, equation (7) with the constraint \( x_k = 1 \) represents the following system.

\[
\begin{align*}
x_k & = 1 \\
r_{0,0}x_0 + \cdots + r_{k,0}x_k + \cdots + r_{n-1,0}x_{n-1} & = y_0 \\
\vdots & \\
r_{0,n-1}x_0 + \cdots + r_{k,n-1}x_k + \cdots + r_{n-1,n-1}x_{n-1} & = y_{n-1}
\end{align*} \tag{8}
\]

Let’s call all the expressions on the left side of the above equations except the first one \( Z_i \) (e.g. \( Z_0 = r_{0,0}x_0 + \cdots + r_{k,0}x_k + \cdots + r_{n-1,0}x_{n-1} \)). Notice that all \( Z_i \)'s are linearly independent because the columns in \( P \) are linearly independent. Therefore, \( x_k \) must be a linear combination of all these \( Z_i \)'s, let’s call this combination set \( Z' \). Since the system in (8) without \( x_k = 1 \) always have a solution regardless of \( y \), we can assign one of the expression in \( Z' \) to 1 and all others to 0 hence we will have a solution for the entire system (8).

Algorithm 3: TREE REDUCTION

Input: \( T = (root, S, K), G = (G(V, E), P, f) \)

1. Postorder Traversal \( T \) do
2. \( u \leftarrow \) current node;
3. if \( u == root \) then
4. \( \text{break}; \)
5. else if \( u.parent \in K \) then
6. \( \text{swap}(f(u), f(u.parent)); \)
7. \( K \leftarrow K \cup \{u\}; \)
8. \( K \leftarrow K \setminus u.parent; \)
9. else
10. \( f(u.parent) \leftarrow f(u.parent) + f(u) \)
11. end
12. end

Next, we give an example to show how tree reduction works.

Example IV.1. Consider the following reduction tree with assignment function \( f \), where the root is \( R \), the terminals are \( \{R, B, D, E\} \), and the Steiner Points are the light blue nodes \( \{A, C\} \).

First notice that \( f(R) + f(B) + F(D) + F(E) = e_4 \). Next,
we use the tree reduction procedure to reduce $f(R)$ to $e_4$.

![Diagram](https://example.com/diagram.png)

The arrow indicates the currently visited node during the tree traversal.

Next, we give a simple algorithm that reduce any reversible row graph with $O(n^2)$ node addition operations.

**Theorem IV.2.** Any reversible row graph with $|V| = n$ can be reduced to a basic row graph by $O(n^2)$ node addition operations.

**Proof.** We prove this theorem by constructing the Algorithm 4.

**Algorithm 4: SIMPLE TOKEN REDUCTION**

**Input:** $(G, P, f)$

1. for $u \in V, f(u) > 1$ do
2. Find a standard basis vector $e \in \mathbb{F}_2^n$ and a set of nodes $V' \subseteq V$ containing $u$, such that $\sum_{v \in V'} f(v) = \{e\}$. We do this by solving equation (7) for all $n$ standard basis vectors until we find a solution that contains $u$. Lemma IV.1 ensures such standard basis vector always exists;
3. Constructing a reduction tree $T$ with root as $u$ and terminals as $V'$;
4. Perform tree reduction on $T$;
5. Reversely perform all the reduction operations except the ones involve the root to make all non-root nodes back to their original vector assignments;
6. end

**Example IV.2.** Making all non-root nodes back to their original vector assignments.
The original row graph can have none of its nodes being standard basis vector. For each of these $n$ nodes, we construct a Steiner tree which can have size of at most $n$. Then for each of these trees, there can be at most $n - 2$ Steiner Points. Hence we need at most $3(n - 2) + 1$ addition operations to reduce $u$. Finally the reversal step will need at most $3(n - 2)$ addition operations. Hence the total operations required is at most $n(6(n - 2) + 1)$.

The construction in the proof of Theorem IV.2 provides us with a $O(n^2)$ upper bound for solutions in OPT TOKEN REDUCTION for reversible row graphs. That is, Algorithm 4 synthesizes a $n$-qubit CNOT circuit with $O(n^2)$ CNOT gates. In the next section, we improve this algorithm by introducing a heuristic and using partial reversal rather than reverting all non-root nodes.

B. Heuristic Reduction Method

Before we describe the algorithm, we define two heuristic functions.

**Definition IV.3** (Cost function). Given any node $v$ in a reversible row graph $(G(V, E), P, f)$, and a standard basis vector $e$ in $F_n^2$. If $v$ can be reduced to $e$ by a linear combination with other nodes (see Lemma IV.1), then let $T$ be the reduction tree that reduces the node $v$ to $e$. cost$(v,e)$ is defined as the number of node addition operations to reduce $v$ to $e$ on $T$, plus the number of operations required to recover any standard basis vector that were transformed to non-basis vector during the reduction. If $v$ cannot be reduced to $e$ by a linear combination with other nodes, then $\text{cost}(v,e) = \infty$.

To exactly compute the cost function, we define the following two algorithms. Algorithm 5 is identical to Algorithm 3 but with additional information indicating which nodes need to be recovered.

**Algorithm 5: TREE REDUCTION WITH TRACKING**

```plaintext
Input: $T = (root, S, K), G = (G(V, E), P, f)$
1 $R \leftarrow \{\}$;
2 operations $\leftarrow []$;
3 Preorder Traversal $T$ do
4 $u \leftarrow$ current node;
5 if $u == root$ then
6     break;
7 else if $u.parent \in K$ then
8     if $u \in R$ then
9         $R \cup \{u\}$;
10        $R \setminus \{u\}$;
11     end
12     swap$(f(u), f(u.parent))$;
13     $K \leftarrow K \cup \{u\}$;
14     $K \leftarrow K \setminus u.parent$;
15     operations.append("SWAP", u, u.parent);
16 else
17     if size$(f(u.parent)) == 1$ then
18         $R \cup \{u\}$;
19     end
20     $f(u.parent) \leftarrow f(u.parent) + f(u)$;
21     operations.append("ADD", u.parent, u);
22 end
23 end
24 return operations, $R$;
```

Algorithm 6 is similar to the operation reversal procedure described in Example IV.2, but only reversely performs operations that are necessary to recover those standard basis vectors that were transformed to non-basis vector during the reduction.

Consequently, the cost function can be computed directly by performing Algorithm 5 and Algorithm 6, then counting the total number of addition operations (a SWAP counts for 3 addition operations).

**Definition IV.4** (Loss function). For a reversible row graph $G = (G(V, E), P, f)$, we compute the loss function by the following steps:

1) Let $B$ be the set of standard basis vectors in $F_n^2$. For all $(u, e) \in V \times B$ construct the following table:

| $u_1$ | $e_1$ | $e_2$ | $e_3$ | ... | $e_n$ |
|-------|-------|-------|-------|-----|-------|
| $u_2$ | cost$(u_2, e_1)$ | cost$(u_2, e_2)$ | cost$(u_2, e_3)$ | ... | cost$(u_2, e_n)$ |
| $u_3$ | cost$(u_3, e_1)$ | cost$(u_3, e_2)$ | cost$(u_3, e_3)$ | ... | cost$(u_3, e_n)$ |
| ...  | ...   | ...   | ...   | ... | ...   |
| $u_n$ | cost$(u_n, e_1)$ | cost$(u_n, e_2)$ | cost$(u_n, e_3)$ | ... | cost$(u_n, e_n)$ |

**TABLE 1**

**COST TABLE**
Algorithm 6: Reduction Recovery

Input: operations, R, T = (root, S, k), G = (G(V, E), P, f)
1 recover_ops ← [];
2 for opType, node1, node2 ∈ reversed(operations) do
3   if opType == "ADD" and node1 ∈ R then
4     f(node1) ← f(node1) + f(node2);
5     recover_ops.append("ADD", node1, node2);
6   if size(f(node1)) == 1 then
7     R \ {node1};
8   end
9   else if opType == "SWAP" and node2 ∈ R then
10      swap(f(node1), f(node2));
11      R ∪ {node1};
12      R \ {node2};
13      recover_ops.append("SWAP", node1, node2);
14   end
15 return recover_ops

Algorithm 7: Heuristics Token Reduction

Input: G = (G, P, f)
1 while not in basic form do
2   We compute the cost table T 1;
3   Let S be the list of (u, e) pairs in T with the smallest cost;
4   (u_min, e_min) ← null;
5   loss_min ← ∞;
6   for (u, e) ∈ S do
7      Reduce u to e using Algorithm 5 and Algorithm 6;
8      if Loss(G) < loss_min then
9         loss_min ← Loss(G);
10        (u_min, e_min) ← (u, e);
11      end
12      Reverse all operations;
13      end
14 Reduce u_min to e_min by Algorithm 5;
15 Recover standard basis vectors by Algorithm 6;
16 end

The routed circuit is then subjected to the following post-processing procedure:
1) SWAP synthesis: for each SWAP gate, convert it to CNOT gates in an orientation (see Equation (4)) that can hopefully cancel some adjacent CNOT gates.
2) CNOT cancellation: for each CNOT gate, try to cancel it with other CNOT gates by Equation (5).5

Firstly, notice that we select u_min, e_min that have the smallest cost; this ensures that the algorithm reduces exactly one node for each iteration. This also helps to limit the number of times to compute the loss function. Secondly, minimizing the loss function helps the algorithm select a reduction that transforms the token graph such that the remaining iterations require few operations.

C. Complexity Analysis

In terms of the final circuits’ gate-count complexity, Algorithm 7 reduces one non-standard basis vector for each iteration. The reduction and recovery procedure cost O(n) node addition operations (n is the number of qubits). Therefore, the complexity is O(n^2).

Next, we analyze the computational complexity. First, notice that the approximation Steiner Tree algorithm we used has a complexity of O(n^3) (see Appendix A). Then for the cost table, we compute one Steiner tree for each standard basis vector e. Then we compute the cost for each (u, e) pair by selecting different nodes as the root. Hence the cost for constructing a cost table is of O(n^4).

Inside the while-loop, the computational bottleneck lies in the for-loop started at line 7. The set S can at most have n^2 elements; for each (u, e) pair, we have to compute a loss after

2) Let h be a bijective assignment function h : V → B, such that minimizes ∑_{u ∈ V} cost(u, h(u)). And the loss function is defined as

Loss(G) = ∑_{u ∈ V} cost(u, h(u))

3) The function h is solved by using the Hungarian algorithm 4.

Theorem IV.3. Given a reversible row graph G = (G(V, E), P, f). cost(u, h(u)) is finite for all u ∈ V, where h is defined in Definition IV.4.

Proof. This is equivalent to prove a perfect matching exists in a bipartite graph. Hall’s marriage theorem states that for a bipartite graph with vertex set V_1 and vertex set V_2, a perfect matching exists if and only if |neighbours(S)| ≥ |S| for all S ⊂ V_1 (Hall’s condition). That is, we want to prove for every set S ⊂ B, |neighbours(S)| ≥ |S|. We prove it by contradiction. Each standard basis vector in B is a linear combination of some of the row vectors on some nodes. Suppose |neighbours(S)| < |S| for some set S ⊂ B, this implies the system has more equations than variables (i.e. equations are of the form e_i = f(u_1) + f(u_2) + · · · + f(u_k) for some u_j ∈ V), hence there exists a linear combination of row vectors that gives two different results, which is clearly false.

Finally, we show a heuristic algorithm that outperforms the current benchmark when combined with a simple post-processing procedure.

4This project uses an open source implementation available at http://software.clapper.org/munkres/

5The procedure used in this project is the basic optimization method implemented in pyzx [11]
performing the reduction. The complexity of computing the loss function is dominated by the cost of constructing a cost table. Hence each iteration in the for-loop has a complexity of $O(n^4)$, and the complexity for the entire for-loop is $O(n^7)$.

Finally, in the worst case, we need to reduce $n$ nodes in total. Hence the total computational complexity for Algorithm 7 is $O(n^7)$.

D. Token Reduction for General Circuits

Recall that our goals for designing a CNOT synthesis method are: firstly, synthesize using as few operations as possible; and secondly, synthesize to an output mapping that benefits the rest of the circuit. In the previous section, we have addressed the first goal by introducing the heuristic token reduction algorithm. Here we discuss a possible direction to address the second goal.

One characteristic of the heuristic token reduction method is that we have some freedom for selecting a reduction tree in each iteration. For general circuits, the candidate evaluation process can also be adjusted to take into account the difficulty of synthesizing the next CNOT block in the circuit. We already have an approximation for measuring the difficulty of synthesizing a block of CNOT gates, the loss function defined in Definition IV.4. Therefore we only need a way to construct the next CNOT block as a row graph in order to compute the loss function. Constructing a row graph requires only an initial mapping. We can do this by guessing an output permutation that a reduction candidate would most likely lead to. This guessing can be facilitated by the cost table and the assignment function $h$ defined in Definition IV.4.

V. Result

A. Benchmark

A recent study demonstrated a constrained CNOT synthesis approach that relies on solving the syndrome decoding problem [12]. Their test results showed improvement against the Steiner Gauss method on 15 different architectures; hence their method can be considered the current state-of-the-art. However, a valid comparison with their method is not possible because their code is not accessible, and their test circuits are not published. Judging only by the available data shown in their paper, the token reduction method performs better for four of the five architectures tested in this project. Additionally, their method only works for architectures containing a Hamiltonian Path, whereas our approach works with all connected architectures.

As a result, we chose the Steiner Gauss method [7] as the benchmark in order to have a direct comparison. Their method has been considered the state-of-the-art until the work mentioned above was published; and more importantly, their code is publicly accessible.

B. Comparison Method

For each of the five architectures tested, we consider CNOT circuits with either 4, 8, 16, 32, 64, 128 or 256 gate counts. Then, for each of these gate counts, we generated 100 random CNOT circuits to perform synthesis and compared the results between the Steiner Gauss method and the token reduction method. For each random circuit, we used the same arbitrary initial mapping for both methods (See Appendix C). Moreover, after performing the token reduction method for each circuit, we verified the the output circuit was equivalent (up to a permutation) to the original circuit by direct matrix comparison. Our code is entirely written in Python; even though the implementation hasn’t been well optimized, the token reduction program still took less than 20 minutes to test all 3500 circuits on a consumer-grade laptop.

Table II shows a comparison between the Steiner Gauss method and the token reduction method for 5 different architectures. The first column shows the architectures tested in this comparison. The second column titled “#” shows the gate counts in the tested circuits. The third and fourth columns show the average of the output CNOT counts for the Steiner Gauss and the token reduction methods respectively. The fifth, sixth, and seventh columns show the average, minimum and maximum percent improvements in total CNOT count of our approach vs. the Steiner Gauss method. The last column shows the percentage of the tested circuits in which our approach outperformed the Steiner Gauss method. All of the 5 architecture graphs are listed in Appendix C.

VI. Discussion

A. Summary

In this study, we introduced a CNOT synthesis method for quantum computers with restricted connectivity. Our method utilizes the observation that a qubit routing procedure doesn’t require the routed circuit to have the same permutation for its output as for its input. As long as the permutation for the output is known, we can re-order the output after the quantum computation finishes. Our approach synthesizes a CNOT circuit to a permutation that is decided on the fly in order to find the best output permutation that is the easiest for the synthesis procedure. This approach consistently outperforms the benchmark method [7], which always synthesizes a CNOT circuit such that its input and output have the same permutation. Moreover, our approach works for all connected quantum computer architectures without any graphical assumptions.

Another important characteristic of our approach is that we have some control over the output’s permutation of a routed circuit. This property could prove beneficial when we extend our method for general quantum circuits. A general quantum circuit can be converted and partitioned into blocks of CNOT gates and blocks of one-qubit gates. Therefore, the output’s permutation for one CNOT sub-circuit will have a substantial effect on the difficulty to synthesize the remaining CNOT sub-circuits.

Furthermore, we also proposed a new representation for working with the constrained CNOT synthesis problem. This
## TABLE II
### METHODS COMPARISON

| Architecture      | #   | Steiner | TR  | Mean  | Max  | Min  | Positive |
|-------------------|-----|---------|-----|-------|------|------|----------|
|                   |     |         |     | Average output | CNOT count | Saving: TR against Steiner |          |
| 9-square          | 4   | 15.51   | 11.67 | 21.56% | 66.67% | -40.00% | 93.00%  |
|                   | 8   | 29.7    | 20.35 | 28.59% | 64.44% | -50.00% | 93.00%  |
|                   | 16  | 44.78   | 31.08 | 29.09% | 54.76% | -9.38% | 95.00%  |
|                   | 32  | 55.84   | 39.31 | 28.94% | 51.35% | -8.11% | 99.00%  |
|                   | 64  | 60.43   | 42    | 29.74% | 56.79% | 2.04%  | 100.00% |
|                   | 128 | 60.38   | 41.33 | 30.91% | 54.93% | 0.00%  | 100.00% |
|                   | 256 | 59.67   | 43.16 | 27.14% | 45.95% | -2.22% | 99.00%  |
| 16-square         | 4   | 28.24   | 21.29 | 20.88% | 63.41% | -32.43%| 90.00%  |
|                   | 8   | 56.93   | 40.11 | 27.40% | 58.06% | -15.09%| 97.00%  |
|                   | 16  | 98.95   | 64.08 | 33.46% | 64.78% | -11.67%| 98.00%  |
|                   | 32  | 154.93  | 109.69| 28.36% | 48.26% | 6.19%  | 100.00% |
|                   | 64  | 196.73  | 149.54| 23.85% | 42.20% | 8.65%  | 100.00% |
|                   | 128 | 205.41  | 165.08| 19.35% | 34.51% | -3.47% | 99.00%  |
|                   | 256 | 204.35  | 163.48| 19.78% | 37.13% | 5.76%  | 100.00% |
| ibmqx5            | 4   | 39.84   | 30.83 | 20.14% | 53.19% | -25.00%| 88.00%  |
|                   | 8   | 71.47   | 52.47 | 24.18% | 61.11% | -76.47%| 94.00%  |
|                   | 16  | 126.03  | 88.13 | 28.29% | 58.79% | -50.00%| 98.00%  |
|                   | 32  | 183.89  | 136.95| 24.60% | 50.24% | -7.95% | 100.00% |
|                   | 64  | 230.71  | 186.87| 18.65% | 39.07% | -4.69% | 97.00%  |
|                   | 128 | 242.24  | 199.79| 17.28% | 32.95% | 2.75%  | 100.00% |
|                   | 256 | 245.64  | 201.48| 17.83% | 31.01% | 2.18%  | 100.00% |
| rigetti-16q-aspen  | 4   | 59.37   | 30.32 | 43.60% | 81.44% | -24.00%| 98.00%  |
|                   | 8   | 101.24  | 56.5  | 41.72% | 66.22% | -22.45%| 98.00%  |
|                   | 16  | 166.03  | 96.81 | 40.61% | 60.11% | -17.53%| 99.00%  |
|                   | 32  | 223.05  | 156.91| 29.26% | 49.38% | 9.90%  | 100.00% |
|                   | 64  | 260.43  | 209.42| 19.34% | 34.73% | -5.38% | 99.00%  |
|                   | 128 | 271.12  | 226.81| 16.15% | 31.09% | 1.19%  | 100.00% |
|                   | 256 | 271.5   | 228.57| 15.62% | 29.24% | -4.47% | 98.00%  |
| ibm-q20-tokyo      | 4   | 23.75   | 17.72 | 22.87% | 52.17% | -16.67%| 97.00%  |
|                   | 8   | 50.89   | 33.25 | 32.11% | 62.50% | -12.00%| 96.00%  |
|                   | 16  | 99.57   | 64.88 | 31.93% | 59.15% | -3.17% | 97.00%  |
|                   | 32  | 177.28  | 116.83| 33.24% | 53.44% | 3.33%  | 100.00% |
|                   | 64  | 254.34  | 191.83| 24.24% | 48.44% | 3.90%  | 100.00% |
|                   | 128 | 290.99  | 233.66| 19.54% | 33.54% | 0.00%  | 100.00% |
|                   | 256 | 293.34  | 235.83| 19.46% | 33.87% | 6.94%  | 100.00% |
representation, which we call the row graph, is more visually appealing than the previously used matrix & graph representation. We expect more synthesis techniques to be inspired by this row graph representation.

B. Future Work

In Section II-C we mentioned that there a second issue associated with restricted connectivity for NISQ devices. This issue states that a CNOT gate can only be applied to adjacent qubits with certain directions. We briefly explained that this issue could be addressed by converting a CNOT with one direction to a CNOT with the opposite direction using Hadamard gates (Equation 1). However, future studies might want to take this issue into account while designing the synthesis algorithm. For example, when selecting a tree reduction, we might want to prefer a tree whose node addition operations mostly follow the architecture’s direction constraints.

In addition to designing a look-ahead mechanism to optimize the output’s permutation (see Section IV-D), we also need to find a suitable method for optimizing the initial mapping. The method in [7] uses a genetic algorithm to find an initial mapping. For each selection iteration, they run the entire synthesis algorithm for all populations to compute the fitness scores. However, our method has a larger run-time complexity; hence running the entire synthesis procedure to compute fitness score would require significantly more time. Therefore, we might want to design a fitness function that is easier to compute while accurately reflect the score for each mapping in the population.

Lastly, the approximate minimum Steiner Tree algorithm (see Appendix A) used in this project is not only inefficient but also not tailor-made for our tree reduction procedure. Two examples of this issue can be seen in Appendix B. Therefore, designing a better algorithm to construct Steiner trees would have a straightforward improvement to our algorithm. We expect that our algorithm will become more affected by a non-ideal Steiner Tree algorithm for larger architectures. Even though finding a minimum Steiner Tree is an NP-complete problem on general graphs, we can focus our efforts on designing a heuristic algorithm for each specific architecture.

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APPENDIX A

HEURISTIC ALGORITHM FOR STEINER TREES

Assume the input graph $G$ has its vertices labeled by $[0, 1, \cdots, n-1]$.
Algorithm 8: genSteiner

Input: A architecture graph \( G(V, E) \), set of vertices \( S \), root

Output: A Steiner tree \( T \)

1. # For each edge \((u, v)\) add an edge \((v, u)\);
2. newEdges = \{
3. foreach \((u, v) \in E_G\) do
4. newEdges.add((v, u));
5. end
6. \( E_G \).union(newEdges);
7. Dist, Successors = Floyd-WarshallWithPath\((G', (u, v) \mapsto 1)\);
8. # Find a pair of vertices in \( S \) with minimal distance;
9. \((u, v) = \text{NearestNeighbours}(S, S, Dist)\);
10. # The heuristic;
11. \( S2 = S.copy() \);
12. # Tree like graph;
13. \( T = \text{graph()} \);
14. path = PathFromSuccessors(Successors, u, v);
15. # Add the path to the tree and remove vertices from \( S \);
16. AddPathToGraph(T, path);
17. \( S2 = S2 \setminus V_T \);
18. while \( S2 . isNotEmpty() \) do
19. \((u, v) = \text{NearestNeighbours}(S2, V_T, Dist)\);
20. path = PathFromSuccessors(Successors, u, v);
21. AddPathToGraph(T, path);
22. \( S2 = S2 \setminus V_T \);
23. # Converted the tree like graph to a rooted tree by BFS;
24. RT = Treeify(T, root);
25. return RT

Algorithm 9: Floyd-WarshallWithPath

Input: A directed weighted graph \( G(V, E) \) where \( V = \{0, 1, 2, \ldots, |V| - 1\}\), a function weight()

Output: A \(|V| \times |V|\) distance matrix \( D \), a \(|V| \times |V|\) Successor matrix \( S \)

1. Construct a \(|V| \times |V|\) distance matrix \( D \) with \( 0 \) for every diagonal entry, and other entries has \( \infty \);
2. Construct a \(|V| \times |V|\) Successor matrix \( S \) with \( i.e \) \( i_{th} \) row for every diagonal entry, every other entry initialized null;
3. foreach \((u, v) \in E\) do
4. \( D[u][v] = \text{weight}((u, v)) \) \( S[u][v] = v \)
5. end
6. for \( k = 0; k < |V|; k = k + 1 \) do
7. for \( i = 0; i < |V|; i = i + 1 \) do
8. for \( j = 0; j < |V|; j = j + 1 \) do
9. if \( D[i][j] > D[i][k] + D[k][j] \) then
10. \( D[i][j] = D[i][k] + D[k][j] \);
11. \( S[i][j] = S[i][k] \)
12. end
13. end
14. end
15. return \( D, S \)

Algorithm 10: PathFromSuccessors

Input: Successor matrix \( S \), vertex \( u \), vertex \( v \)

Output: A path list object \( path \) contains the path from \( u \) to \( v \)

1. if \( S[u][v] == \text{null} \) then
2. return \( [] \)
3. end
4. path = \([u]\);
5. \( x = u \);
6. while \( x \neq v \) do
7. \( x = S[x][v] \);
8. path.append(x);
9. end
10. return path

APPENDIX B

EXAMPLES OF INEFFICIENT STEINER TREES

Example B.1. Given root \( Q2 \), terminals \( \{Q2, Q6, Q9, Q11\} \), the following tree requires 9 node addition operations to reduce.

Fig. 16. Inefficient Tree (1) on 16-square architecture

\[ \text{\{Q2, Q6, Q9, Q11\}} \]
while an efficient tree would be:

Fig. 17. Efficient Tree (1) on 16-square architecture

The efficient tree requires 6 node addition operations to reduce; hence a 33.33% improvement.

Example B.2. The following tree reduces $Q_2$ to $e_8$ with 7 node addition operations. However, except $Q_1$ and the root, all other terminal nodes will then have non-unit vectors after the reduction. Hence we have 6 nodes to be recovered.

$e_1 + e_2 + e_3 + e_4 + e_5 + e_6 + e_7 + e_8$

Fig. 18. Inefficient Tree (2) on 16-square architecture

The second tree also requires 7 node addition operations to reduce. However, we would only have to recover $Q_1, Q_3$ and $Q_4$ after the reduction.

• 9-square:

• 16-square:

Appendix C

Example Architectures

In this section we provide the architecture graphs for the 5 architectures tested in Chapter V-B. Notice that we ignore the directions of the edges in some architectures for the reason explained in Section II-C.

We also include the initial mappings for each architecture used in the comparison test. For each $n$-qubit circuit, we assume the wires are labeled as $w_1, w_2, \cdots, w_n$ from the top to the bottom.

- 9-square:

- 16-square:
• ibm-qx5:

See Figure 24.

\[
M_0 = \begin{cases} 
  w_1 \rightarrow Q_1, & w_2 \rightarrow Q_2 \\
  w_3 \rightarrow Q_3, & w_4 \rightarrow Q_4 \\
  w_5 \rightarrow Q_5, & w_6 \rightarrow Q_6 \\
  w_7 \rightarrow Q_7, & w_8 \rightarrow Q_8 \\
  w_9 \rightarrow Q_9, & w_{10} \rightarrow Q_{10} \\
  w_{11} \rightarrow Q_{11}, & w_{12} \rightarrow Q_{12} \\
  w_{13} \rightarrow Q_{13}, & w_{14} \rightarrow Q_{14} \\
  w_{15} \rightarrow Q_{15}, & w_{16} \rightarrow Q_{16}
\end{cases}
\]

• ibm-q20-tokyo:

\[
M_0 = \begin{cases} 
  w_1 \rightarrow Q_1, & w_2 \rightarrow Q_2 \\
  w_3 \rightarrow Q_3, & w_4 \rightarrow Q_4 \\
  w_5 \rightarrow Q_5, & w_6 \rightarrow Q_6 \\
  w_7 \rightarrow Q_7, & w_8 \rightarrow Q_8 \\
  w_9 \rightarrow Q_9, & w_{10} \rightarrow Q_{10} \\
  w_{11} \rightarrow Q_{11}, & w_{12} \rightarrow Q_{12} \\
  w_{13} \rightarrow Q_{13}, & w_{14} \rightarrow Q_{14} \\
  w_{15} \rightarrow Q_{15}, & w_{16} \rightarrow Q_{16}
\end{cases}
\]

• rigetti-16q-aspen:

\[
M_0 = \begin{cases} 
  w_1 \rightarrow Q_1, & w_2 \rightarrow Q_2 \\
  w_3 \rightarrow Q_3, & w_4 \rightarrow Q_4 \\
  w_5 \rightarrow Q_8, & w_6 \rightarrow Q_7 \\
  w_7 \rightarrow Q_6, & w_8 \rightarrow Q_5 \\
  w_9 \rightarrow Q_9, & w_{10} \rightarrow Q_{10} \\
  w_{11} \rightarrow Q_{11}, & w_{12} \rightarrow Q_{12} \\
  w_{13} \rightarrow Q_{16}, & w_{14} \rightarrow Q_{15} \\
  w_{15} \rightarrow Q_{14}, & w_{16} \rightarrow Q_{13}
\end{cases}
\]

• rigetti-16q-aspen:

Fig. 21. 16-square

Fig. 22. rigetti-16q-aspen

Fig. 23. ibm-q20-tokyo

Fig. 24. ibm-q20-tokyo
Fig. 24. ibm-qx5
This figure "fig1.png" is available in "png" format from:

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