Parallel wideband digital up-conversion architecture with efficiency

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Abstract: Owing to the limited processing speed of current digital signal processing devices, digital generated signal frequency and bandwidth based on digital up-conversion technique has long been a bottleneck. Interpolation on the baseband signal puts great pressure on the following filtering and mixing operation. In this study, an efficient parallel architecture is presented, which moves the interpolation behind the filtering and mixing, and adopts parallel numerically controlled oscillator (NCO) arrays and poly-phase low-pass filter arrays to achieve the anticipated orthogonal mixing signal and prototype filter. Parallel NCO decomposition principle and mathematical derivation are elaborated, and realisation of the poly-phase filter arrays is also discussed. The proposed post-interpolation architecture can effectively relieve the filtering and mixing pressure including operation rate and computational complexity, which will benefit the hardware implementation. In the end, verification test of signal up-conversion with 400 MHz bandwidth is launched to certify the architecture validity.

1 Introduction

Compared with digital down-conversion (DDC) technique (e.g. [1]), which tends to move the IF wideband signal to baseband and reduce data rate, digital up-conversion (DUC) technique operates in the reverse direction. DUC is a critical kind of technique in signal generation area, especially for advanced arbitrary waveform generation (e.g. [2]). The basic idea is to convert the baseband signal to a specific carrier and increase data rate.

Generally speaking, the common DUC processing always cascades the interpolation, low-pass filter, cascaded integrator comb (CIC) filter and tuning mixing (e.g. [3]), which will undoubtedly lead to high speed pressure and large resource consumption pressure for digital computation. Thus, it is difficult to implement high carrier and wide bandwidth DUC on hardware platforms such as ASIC, DSPs and FPGAs.

Take a comprehensive view of the above hardware platforms, the rapidly developed FPGA devices turn out to be more competent. As for the current situation, plenty of researches promote various parallel DDC structures (e.g. [4, 5]) in order to make it easy to realise, which pushes us to do the same work for the DUC technique. This paper mainly focuses on the research on parallel decomposition for several DUC units according to the classic conversion theory, and proposes an efficient parallel architecture that consists of numerical controller numerically controlled oscillator (NCO) arrays, poly-phase filter arrays and post-interpolator. On the basis of each branch signal that originates from the same input baseband signal, detailed convolution operation of the filtering is also elaborated. The decreased operation speed and reduced computational complexity make the presented DUC architecture much easier to be applied on hardware platforms.

2 Classic DUC system

For a given baseband signal, the classic block diagram of DUC system (e.g. [6]) is shown in Fig. 1. The baseband signal is modulated with a complex carrier signal to fit for the DAC conversion and complete RF transmission. The first level interpolation, designed according to the anticipated output signal frequency and bandwidth, tremendously increases the data rate and brings much computational pressure and complexity to the following low pass filter (LPF) and NCO. Therefore, the higher the output signal frequency and bandwidth is, the more difficult the system runs.

Suppose \( I(n) \) and \( Q(n) \) represent the baseband in-phase and quadrature signal, respectively, the output frequency of NCO is \( \omega_c \). Then, we can get the output signal expression of \( y(n) \) as

\[
y(n) = [(I(n), I) + K] \cdot \sin(\omega_c n) + [(Q(n), I) + K] \cdot \cos(\omega_c n)
\]

where all the LPF, NCO and DAC modules work at the same high speed of \( f_{DAC} \). Let the interpolation factor be \( K \), the baseband input signal should be limited to \( f_{DAC}/2K \) (e.g. [7]), which also gives instructions to the design rule of the low-pass filter \( h(n) \) in order to avoid spectrum overlapping.

3 Parallel DUC architecture

3.1 Parallel decomposition principle

Equivalent structure of the classic DUC architecture can be depicted as in Fig. 2. Given a baseband complex signal \( x(n) \) with

![Fig. 1 Block diagram of classic DUC system](Image)
mixing operation before the interpolation so long as we extract one flops (e.g. [11]) which is completely feasible and realisable.

In the context of digital signal processing, the inferred switch could be achieved only by D type flip signals under a certain rule, as charted in Fig. 7. Each path originates from the same input signal source, and goes through a pass filter data from every original mixing signal.

Fig. 4, where \( J. Eng. \) is depicted as Fig. 6 (e.g. [10]), which means we can put the model shown in Fig. 3.

Based on Figs. 3 and 4, allocate the tuning factor \( L(n) \) in Fig. 4 into each branch according to the distributive law of multiplication, we can get the equivalent structure of Fig. 4 shown in Fig. 5, where \( \lambda_k (n) = L(n + K - 1 - k) \).

What is more, there also exists one equivalent transformation model depicted as Fig. 6 (e.g. [10]), which means we can put the data from every K data of the mixing sequence.

Have a close-up view of Figs. 5 and 6, a new parallel K channel decomposition of DUC architecture occurs as shown in Fig. 7, where

\[
L_k(n) = L(nK + K - 1 - k)
\]

where \( L_k(n) \) and \( L_i(n) \) denote the cosine and sine parts of the sub-NCOs, respectively. Equation (5) also tells us that the subsequences vary as the relationship between \( f_0 \) and \( f_s \) changes. No matter what kind of situation, each branch tuning sequence operates at the same rate, which turns out to be \( f_s \) but not \( Kf_s \), leading to a tremendous relief on the hardware implementation difficulty.

Digging into the NCO decomposition process, a fixed phase \( n \) is found between \( f_s \) and \( Kf_s \) as it fetches data points sequentially from \( y_{k-1}(n) \) to \( y_k(n) \), which works like a switch. However, this operation could be executed on the I/O ports on hardware platform. As for FPGA devices, the inferred switch could be achieved only by D type flip flops (e.g. [11]) which is completely feasible and realisable.
According to the coefficient property of FIR (e.g. [14]) which states that
\[
\varphi(L_{Q,k}(n)) = 2\pi \cdot \frac{K - 1 - k}{K} \cdot \frac{f_0}{f_s}
\]
\[
\varphi(L_{I,k}(n)) = \pi - 2\pi \cdot \frac{K - 1 - k}{K} \cdot \frac{f_0}{f_s}
\]
From (6), a fixed phase deviation between every two adjacent branches can be calculated as
\[
\Delta \varphi(L_Q) = \Delta \varphi(L_I) = \left| \varphi(L_{Q,k+1}(n)) - \varphi(L_{Q,k}(n)) \right| = \left| \varphi(L_{I,k+1}(n)) - \varphi(L_{I,k}(n)) \right| = -2\pi f_s/f_s
\]
According to the previous deduction, the parallel DUC architecture in real mode could be easily depicted as Fig. 8.

Obviously, each branch poly-phase filter \(e_q(n)\) only has one-\(K\)th tap of the prototype filter \(h(n)\) and runs at data rate of \(f_s\) instead of \(Kf_s\). Correspondingly, we do not need to generate one NCO sequence with high data rate of \(Kf_s\), but \(K\) pairs of sine and cosine signals \([x_{Q,n}(n)\ x_{I,n}(n)], \ [x_{Q,n}(n)\ x_{Q,n}(n)], \ etc., \ [x_{Q,n}(n)\ x_{I,n}(n)], \) all operate at \(f_s\) to mix with the post-filtered \(I(n)\) and \(Q(n)\), respectively. Suppose the output of each branch after mixing is \(y_Q(n)\) and \(y_I(n)\), then we can get
\[
y_Q(nK + K - 1 - k) = y_Q(n) = \left\{ Q(n) \cdot e_q(n) \right\} \cdot x_{Q,n}(n)
\]
\[
y_I(nK + K - 1 - k) = y_I(n) = \left\{ I(n) \cdot e_q(n) \right\} \cdot x_{I,n}(n)
\]
Thus, the final output signal \(y(n)\) can be expressed as
\[
y(n) = y_Q(n) + y_I(n)
\]
\[\text{4 Poly-phase filter realisation}\]
As proposed above, the parallel DUC architecture involves \(K\) poly-phase filters on each signal path, which efficiently reduces the tap coefficient and data rate of these paths. Usually, we tend to adopt special interpolation filters to simplify the realisation, such as half-band filters (e.g. [12]), cascaded filters (e.g. [13]) and so on. However, we here discuss the general filter realisation without loss of generality.

Suppose the designed prototype filter \(h(n)\) holds \(N\)-tap coefficients, and \(N \mod K = 0\), then length of each poly-phase filter \(e_q(n)\) decreased to \(N/K\). Let \(r_q(n)\) represents the result that the original signal \(x(n)\) goes through each \(e_q(n)\) as shown in Fig. 7. We can get
\[
r_q(n) = \sum_{m=0}^{N/K-1} x(n-m)e_q(m)
\]
\[\text{(10)}\]
According to the coefficient property of FIR (e.g. [14]) which means
\[
h(n) = h(N - 1 - n), n \in [0, N - 1] \cap Z
\]
\[\text{(11)}\]
The \(r_{K-1,q}(n)\) expression can be derived as
\[
r_{K-1,q}(n) = \sum_{m=0}^{N/K-1} x(n-m)e_{K-1,q}(m)
\]
\[\text{(12)}\]
\[
= \sum_{m=0}^{N/K-1} x(n-m)h(mK + k)
\]
\[\text{(13)}\]
Let \(m = N/K - m - 1\), and replace \(m, m \in [0, N/K - 1] \cap Z\) with \(N/K - m - 1\), where \(N/K - m - 1\) also belongs to \([0, N/K - 1] \cap Z\), the \(r_{K-1,q}(n)\) expression can be rewritten as
\[
r_{K-1,q}(n) = \sum_{m=0}^{N/K-1} x(n + m - N/K + 1)h(mK + k - 1 - k)
\]
\[\text{(13)}\]
Compare (10) and (13), it is easy to find that the results of \(k\)th and \((K-1-k)\)th poly-phase filter path come from the same coefficient group of the original prototype filter with different delays that operate on the input signal, as shown in Fig. 9.

Fig. 9 shows that the input signal should execute delay operation first before multiplying with filter coefficients. If we apply the idea that Fig. 4 illustrates into the above structure, we succeed in putting the delay operation after the multiplication shown as Fig. 10, which achieves to reduce the multiplier accounts nearly to half.

\[\text{5 Verification}\]
In the following part, a verification test is launched to certify the efficiency and validity of the proposed parallel DUC technique. Given an input baseband chirp signal covers BW = 200 MHz with
The prototype low-pass filter could be designed according to the interpolation theory, whose pass-band should be 250 MHz @1000 MHz sample rate at most. Parameters such as attenuation and ripple and so on could be adjusted easily. Apply the four decomposed NCO signals and filter coefficients into parallel DUC architecture shown in Fig. 8, we can obtain the waveform and spectrum of the output signal as shown in Fig. 12.

The above results show that the proposed parallel DUC architecture can effectively complete the signal spectrum conversion and operates on relatively low speed which brings great benefit for hardware implementation.

6 Conclusion

DUC technique plays a key role in signal generation area. Although hardware processing speed is growing rapidly in current trend, the generated signal’s frequency and bandwidth are still subjected to the limited component speed such as FPGAs, DACs and so on. The proposed parallel DUC architecture with efficiency in this paper will break up this dilemma to some extent. For one hand, it reduces the system processing speed. For another, it makes the digital computation much easier, such as less filter tap coefficients, less multipliers and so on. Verification test certifies the feasibility and validity of the referred method.

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8 References

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