Low temperature and radiation resistant JFET differential amplifiers circuits synthesis with increased common-mode rejection ratio

N N Prokopenko1,2,3, I V Pakhomov1 and A A Zhuk1

1Don State Technical University, 1, Gagarin Sq., Rostov-on-Don, 344000, Russia
2Institute for Design Problems in Microelectronics of Russian Academy of Sciences, IPPM RAS, Zelenograd, 124681, Russia

3E-mail: ilyavpakhomov@gmail.com

Abstract. We have had limits for transfer ratios of adder $\Sigma 1$, when there are increased values of common-mode rejection ratio, for general function circuit of classic two stage JFET of differential amplifiers, including input differential stage and adder $\Sigma i$ output currents differential stage. We have considered three particular variants to synthesize differential amplifiers practical circuits based on current mirrors, folded cascodes and floating complementary differential stage. We have shown that differential amplifiers of floating complementary differential stage subclass is the most advanced to construct low noise analog circuits to process signals of sensors, operating in severe operating conditions (at low temperatures, initial radiation). Proposed circuit solutions are recommended for silicon and GaAs JFET technologies (including JFet, CJFet, CBiCJFet).

1. Introduction
The classical differential stages (DS) common-mode interference resistant significantly influences precision of differential amplifiers (DA), differential difference amplifiers (DDA) and instrumentation amplifiers (IA) [1-11]. A task to increase CMRR becomes complicated, when DA (DDA, IA) operate at low temperatures and initial radiation [12, 13]. So it is vital to find new architectures of DA, having increased CMRR, and to make something to increase CMRR coefficient in severe operating conditions.

The paper aim and novelty are the following:

- to have limits for transfer ratios K1, K2, K3, K4 of current adder $\Sigma 1$ with four current inputs in CJFet classic two stage DA, having input CJFet DS and output current adder $\Sigma 1$, when there is a minimum transconductance gem on DA’s output of input common-mode signal $v_c$, related to CJFet DS static mode set circuits influence. This DA’s topology is a base of modern operational amplifiers and other analog circuits [12, 14, 15];
- to consider new [16] and probable architectures of CJFet DA with increased CMRR for tasks of precision sensor interfaces construction.
2. Differential amplifier’s general functional circuit with current output
The differential stage (DS) output CJFet’s in the circuit of a classic DA on figure 1 differ by having commonly four current outputs Out.1÷Out.4 [13, 17-20]. The outputs Out.1 and Out.2 are matched with positive power source bus Vcc, the outputs Out.3, Out.4 are matched with the negative power source bus Vee. The current adder Σ1 provides addition (or subtraction) of DS’s outputs’ currents. Its current transfer ratios K1, K2, K3, K4 are close to 1 and may be 0, 1, -1, that is change or do not change signal phase.

\[
\text{sign}K_i = \text{sign}K_2, \text{sign}K_3 = \text{sign}K_4, \quad (1)
\]

where \(\text{sign}K\) is a sign function, which characterize DS’s current signal phase change when its transmission via adder Σ1. Moreover \(\text{sign}K_i = +1\), signal is in adder Σ1 on the input not inverted and \(\text{sign}K_i = -1\), if signal inverted.

An output current of adder Σ1 in the structure on figure 1 is defined by the following equation at influence of common-mode signal \(v_c\) on DS’s inputs:

\[
i_{\text{load}} = i_{\text{Out.1}}K_1 + i_{\text{Out.2}}K_2 + i_{\text{Out.3}}K_3 + i_{\text{Out.4}}K_4. \quad (2)
\]

Depending on phase relations of currents \(i_{\text{Out.1}}\), \(i_{\text{Out.4}}\) in DS and of the adder Σ1 transfer ratios \(K_1, K_2, K_3, K_4\), a significant quantity of individual circuit solutions for adder Σ1 and input DS [13, 17-20], in which, to suppress the common-mode signal, it is possible to obtain a current close to zero in the load \(i_{\text{load}} = 0\). It is possible to define \(K_1 = K_2 = K_3 = K_4 = -1\) for the first group of practical circuits, it corresponds an application of current mirrors in structure of adder Σ1 figure 1. In this case in order to provide current compensation on DA’s output, DS’s output currents, resulting from influence of \(v_c\), should have the following directions, which depend on DS’s circuitry:

![Figure 1. DA with CJFet’s general functional circuit for input common-mode signal (\(v_{c1} = v_{c2} = v_c\)).](image-url)
\[ I_{\text{Out.1}} + I_{\text{Out.2}} + I_{\text{Out.3}} + I_{\text{Out.4}} = 0. \]  

(3)

Defining \( i_{\text{Out.1}} = i_1 \), \( i_{\text{Out.2}} = i_2 \) as inputting into input stage DS’s multi-pole circuit, we have that \( i_{\text{Out.3}}, i_{\text{Out.4}} \) for to provide mutual compensation in unit \( \Sigma \) of errors from common-mode signal shall be outputted:

\[ i_3 = -i_{\text{Out.3}}; i_4 = -i_{\text{Out.4}}. \]  

(4)

For the second group of DA’s practical circuits, when non-inverting current amplifiers (for example, folded cascodes \( K_1 = K_2 = K_3 = K_4 = +1 \)) are used in adder \( \Sigma \), directions of DS’s output currents should meet the following conditions:

\[ i_1 = i_{\text{Out.1}}, i_2 = i_{\text{Out.2}}, i_3 = -i_{\text{Out.3}}; i_4 = -i_{\text{Out.4}}. \]  

(5)

The above limits of DS’s circuitry and characteristics of adder \( \Sigma \) is base for circuit synthesis DA’s with increased CMRR. In this case the following two variants of synthesis procedures are recommended.

In the first case ones defines a sign of transfer ratios \( K_1 : K_4 \), then synthesizes scheme DS according to the following principle: «required directions of output currents \( i_1 : i_4 \), which meet conditions (1) and (2). In this case we recommend to apply folded cascodes with \( K_1 = K_2 = K_3 = K_4 = +1 \) in adder \( \Sigma \) for CJFet microcircuits.

In the second variant of circuit synthesis directions of DS’s output currents of the input stage \( (i_1, i_2, i_3, i_4) \) may be known. Then it is necessary to identify circuit solutions for adder \( \Sigma \), which will provide mutual compensation of errors from DS’s input common-mode signal \( v_c \) in output node \( \Sigma \).

There are more than a hundred of DA constructions variants, which correspond to the architecture, specified on figure 1. There are known circuit solutions [21], and new topologies of DA [13, 17-20] among them.

3. Classical CJFet differential amplifiers based on current mirrors

It is acceptable to use inverting current mirrors (CM1) of different modifications, where current transfer ratio is equal (ideally) to minus 1 (\( K_i = -1 \)) in this DA’s class, for example in DA, specified on figure 2, corresponding to functional circuit on figure 1. The DA’s circuit, specified on figure 2, is quite popular in analog circuitry [21]. But it is necessary to note, that CJFet current mirrors’ circuitry significantly differs from classical variants of their construction, typical for CMOS and BJT processes and requires additional investigation.

![Figure 2. Classic CJFet DS with increased CMRR.](image-url)
In circuit on figure 2 the resistor $R_0$ simulates pedestal current source’s $I_1$ output resistance, the source defines static mode of input DS. Due to additional buffer amplifier’s connection to current output $\text{Out.}_\Sigma$ it is possible to implement CJFet operational amplifiers with classical architecture based on circuit figure 2 [21].

4. Classical CJFet differential amplifiers based on current mirrors

In analog microcircuits (AM) based on complementary field-effect transistors with a p-n junction control, instead of current mirrors, it is preferable to use CJFet “folded” cascodes [19, 20, 22, 23]. This simplifies the AM circuitry and also extends the frequency range. Examples of such successful circuitry solutions for DS with increased CMRR are shown in figures 3, 4 [16].

![Figure 3. CJFet DC based on symmetrical «folded cascodes».](image)

![Figure 4. CJFet DC with Increased CMRR based on asymmetrical «folded cascodes».](image)

5. CJFet differential amplifiers based on floating complementary differential stage

It is possible to implement this subclass of DA on base of CJFet of folded cascodes (figure 5) and CJFet current mirrors (figure 6). These circuits are peculiar by possibility to have extremely low values of common-mode signal error and minimum noise level.

The computer simulation of the circuit, specified on figure 6, at $t=-197^\circ\text{C}$ in LTspice simulation software on CJFet models [24] shows (figure 7), that the suggested circuitry solution provides decrease of $g_{cm}$ by more than 3 orders. As a result, CMRR is increased by the same amount.

The DA’s circuit figure 8 are peculiar by the fact that they operate in AB class mode for differential signal. It allows having not only increased CMRR, but also developing fast operational amplifiers [11].

6. Conclusion

We have formulated limits for input CJFet DS’s output current adder, when at which the increased attenuation coefficient of the input common-mode signal JFET of DA’s is provided. We have considered three particular variants of DA’s practical circuits synthesis: the one, based on current mirrors, folded cascodes and floating complementary differential stage with increased CMMR.

The computer simulation results have shown efficiency of floating complementary differential stage’s application in CJFet analog ICs.
The proposed circuitry solutions are focused on the use of silicon and GaAs technological processes that ensure the performance of integrated circuits at low temperatures and exposure to penetrating radiation.

**Figure 5.** CJFet DS with Increased CMRR based on symmetrical «folded cascodes» CA1, CA2.

**Figure 6.** CJFet DS with increased CMRR based on current mirrors CM1, CM2.

**Figure 7.** FDCS (figure 6) Input Common-Mode Signal Transconductance $g_{cm}$ Frequency Dependence at $R_1=12$ kOhm.

**Figure 8.** CJFet Differential Stage of AB Class with Increased CMRR.

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