GAROTA: Generalized Active Root-Of-Trust Architecture

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Abstract

Embedded (aka smart or IoT) devices are increasingly popular and becoming ubiquitous. Unsurprisingly, they are also attractive attack targets for exploits and malware. Low-end embedded devices, designed with strict cost, size, and energy limitations, are especially challenging to secure, given their lack of resources to implement sophisticated security services, available on higher-end computing devices. To this end, several tiny Roots-of-Trust (RoTs) were proposed to enable services, such as remote verification of device’s software state and runtime integrity. Such RoTs operate reactively: they can prove whether a desired action (e.g., software update, or execution of a program) was performed on a specific device. However, they can not guarantee that a desired action will be performed, since malware controlling the device can trivially block access to the RoT by ignoring/discarding received commands and other trigger events. This is a major and important problem because it allows malware to effectively “brick” or incapacitate a potentially huge number of (possibly mission-critical) devices.

Though recent work made progress in terms of incorporating more active behavior atop existing RoTs, it relies on extensive hardware support—Trusted Execution Environments (TEEs) which are too costly for low-end devices. In this paper, we set out to systematically design a minimal active RoT for tiny low-end MCU-s. We begin with the following questions: (1) What functions and hardware support are required to guarantee actions in the presence of malware?, (2) How to implement this efficiently?, and (3) What security benefits stem from such an active RoT architecture? We then design, implement, formally verify, and evaluate GAROTA: Generalized Active Root-Of-Trust Architecture. We believe that GAROTA is the first clean-slate design of an active RoT for low-end MCU-s. We show how GAROTA guarantees that even a fully software-compromised low-end MCU performs a desired action. We demonstrate its practicality by implementing GAROTA in the context of three types of applications where actions are triggered by: sensing hardware, network events and timers. We also formally specify and verify GAROTA functionality and properties.

1 Introduction

The importance of embedded systems is hard to overestimate and their use in critical settings is projected to rise sharply [1]. Such systems are increasingly inter-dependent and used in many settings, including household, office, factory, automotive, health and safety, as well as national defense and space exploration. Embedded devices are usually deployed in large quantities and for specific purposes. Due to cost, size and energy constraints, they typically cannot host complex security mechanisms. Thus, they are an easy and natural target for attackers that want to quickly and efficiently cause harm on an organizational, regional, national or even global, level. Fundamental trade-offs between security and other priorities, such as cost or performance are a recurring theme in the domain of embedded devices. Resolving these trade-offs, is challenging and very important.

Numerous architectures focused on securing low-end microcontroller units (MCU-s) by designing small and affordable trust anchors [2]. However, most such techniques operate passively. They can prove, to a trusted party, that certain property (or action) is satisfied (or was performed) by a remote and potentially compromised low-end MCU. Examples of such services include remote attestation [5,9,14,21,31,37], proofs of remote software execution [16], control-flow & data-flow attestation [3,17,18,39,46,49], as well as proofs of remote software update, memory erase, and system-wide reset [4,13]. These architectures are typically designed to provide proofs that are unforgeable, despite potential compromise of the MCU.

Aforementioned approaches are passive in nature. While they can detect integrity violations of remote devices, they cannot guarantee that a given security or safety-critical task will be performed. For example, consider a network comprised of a large number (of several types of) simple IoT devices, e.g., an industrial control system. Upon detecting a large-scale compromise, a trusted remote controller wants to fix the situation by requiring all compromised devices to reset, erase, or update themselves in order to expunge malware. Even if each device has an uncompromised, yet passive, RoT, malware (which is in full control of the device’s software state) can easily intercept, ignore, or discard any requests for the RoT, thus preventing its functionality from being triggered. Therefore, the only way to repair these compromised devices requires direct physical access (i.e., reprogramming by a human) to each device. Beyond the DoS damage caused by the multitude of essentially “bricked” devices, physical reprogramming itself is slow and disruptive, i.e., a logistical nightmare.

Motivated by the above, recent research [27,48] yielded trust anchors that exhibit a more active behavior. Xu et al. [48] propose the concept of Authenticated Watch-Dog Timers (WDT), which can enforce periodic execution of a secure component (an RoT task), unless explicit authorization (which can itself include a set of tasks) is received from a trusted controller. In [27] this concept is realized with the reliance on an exist-
being passive RoT (ARM TrustZone), as opposed to a dedicated co-processor as in the original approach from \cite{A48}. Both techniques are time-based, periodically and actively triggering RoT invocation, despite potential compromise of the host device. (We discuss them in more detail in Section \ref{5.4}).

In this paper, we take the next step and design a new general active RoT called \textit{GAROTA}: Generalized Active Root-Of-Trust Architecture. Our goal is an architecture capable of guaranteeing guaranteed execution of trusted and safety-critical tasks based on arbitrary events captured by hardware peripherals (e.g., timers, GPIO ports, and network interfaces) of an MCU the software state of which may be currently compromised. In principle, any hardware event that causes an interruption on the unmodified MCU can trigger guaranteed execution of trusted software in \textit{GAROTA} (assuming proper configuration). In that vein, our work can be viewed as a generalization of concepts proposed in \cite{27, A48}, enabling arbitrary events (interruption signals, as opposed to the timer-based approach from prior work) to trigger guaranteed execution of trusted functionalities. In comparison, prior work has the advantage of relying on pre-existing hardware, thus not requiring any hardware changes. On the other hand, our clean-slate approach, based on a minimal hardware design, enables new applications and is applicable to lower-end resource-constrained MCUs.

At a high level, \textit{GAROTA} is based on two main notions: “\textit{Guaranteed Triggering}” and “\textit{Re-Triggering on Failure}”. The term trigger is used to refer to an event that causes \textit{GAROTA} RoT to take over the execution in the MCU. The “guaranteed triggering” property ensures that a particular event of interest always triggers execution of \textit{GAROTA} RoT. Whereas, “re-triggering on failure” assures that, if RoT execution is illegally interrupted for any reason (e.g., attempts to violate execution’s integrity, power faults, or resets), the MCU resets and the RoT is guaranteed to be the first to execute after subsequent re-initialization. Figure \ref{fig:flow} illustrates this workflow.

We use \textit{GAROTA} to address three realistic and compelling use-cases for the active RoT:

- **GPIO-TCB**: A safety-critical sensor/actuator hybrid, which is guaranteed to sound an alarm if the sensed quantity (e.g., temperature, CO$_2$ level, etc) exceeds a certain threshold. This use-case exemplifies hardware-based triggering.
- **TimerTCB**: A real-time system where a predefined safety-critical task is guaranteed to execute periodically. This use-case exemplifies timer-based triggering, which is also attainable by \cite{27, A48}.
- **NetTCB**: A trusted component that is always guaranteed to process commands received over the network, thus preventing malware in the MCU from intercepting and/or discarding commands destined for the RoT. This use-case exemplifies network-based triggering.

In all these cases, the guarantees hold despite potential full compromise of the MCU software state, as long as the RoT itself is trusted.

In addition to designing and instantiating \textit{GAROTA} with three use-cases, we formally specify \textit{GAROTA} goals and requirements using Linear Temporal Logic (LTL). These formal specifications offer precise definitions for the security offered by \textit{GAROTA} and its corresponding assumptions expected from the underlying MCU, i.e., its machine model. This can serve as an unambiguous reference for future implementations and for other derived services. Finally, we use formal verification to prove that the implementation of \textit{GAROTA} hardware modules adheres to a set of sub-properties (also specified in LTL) that – when composed with the MCU machine model – are sufficient to achieve \textit{GAROTA} end-to-end goals. In doing so, we follow a similar verification approach that has been successfully applied in the context of passive RoT-s \cite{14, 16, A38}.

We implement and evaluate \textit{GAROTA} and make its verified implementation (atop the popular low-end MCU TI MSP430) available to the public along with respective computer proofs/formal verification publicly available in \cite{6}.

2 Scope

This work focuses on low-end embedded MCU-s and on design with minimal hardware requirements. A minimal design simplifies reasoning about \textit{GAROTA} and formally verifying its security properties. In terms of practicality and applicability, we believe that an architecture that is cost-effective enough for the lowest-end MCU-s can also be adapted (and potentially enriched) for implementations on higher-end devices with higher hardware budgets, while the other direction is usually more challenging. Thus, our design is applicable to the smallest and weakest devices based on low-power single-core platform with only a few KBytes of program and data memory (such as the aforementioned Atmel AVR ATmega and TI MSP430), with 8- and 16-bit CPUs, typically running at 1-16 MHz clock frequencies, with $\approx$ 64 KBytes of addressable memory. SRAM is used as data memory ranging in size between 4 and 16 KBytes, while the rest of address space is available for program memory. Such devices usually run software atop “bare metal”, execute instructions in place (physically from program memory), and have no memory management unit (MMU) to support virtual memory.

Our initial choice of implementing \textit{GAROTA} atop the well-known TI MSP430 low-energy MCU is motivated by availability of a well-maintained open-source MSP430 hardware design from OpenCores \cite{25}. Nevertheless, our design and its
The goal of GAROTA is to guarantee eventual execution of a pre-defined functionality \( \mathcal{F} \) implemented as a trusted software executable. We refer to this executable as GAROTA trusted computing base (TCB). GAROTA is agnostic to the particular functionality implemented by \( \mathcal{F} \), which allows guaranteed execution of arbitrary tasks, to be determined based on the application domain; see Section 5 for examples.

A trigger refers to a particular event that can be configured to cause the TCB to execute. Examples of possible triggers include hardware events from:

- **External (usually analog) inputs**, e.g., detection of a button press, motion, sound or certain temperature/CO\(_2\) threshold.
- **Expiring timers**, i.e., a periodic trigger.
- **Arrival of a packet from the network**, e.g., carrying a request to collect sensed data, perform sensing/actuation, or initiate a security task, such as code update or remote attestation.

If configured correctly, these events cause interruptions, which are used by GAROTA to guarantee execution of \( \mathcal{F} \). Since trigger and TCB implementation are configurable, we assume that these initial configurations are done securely, at or before initial deployment. Trigger configuration will include the types of interruptions and respective settings e.g., which GPIO port, what type of event, its time granularity, etc. At runtime, GAROTA protects the initial configuration from illegal modifications, i.e., ensures correct trigger behavior. This protection includes preserving interrupt configuration registers, interrupt handlers, and interrupt vectors. This way GAROTA guarantees that trigger always results in an invocation of the TCB.

However, guaranteed invocation of the TCB upon occurrence of a trigger is not sufficient to claim that \( \mathcal{F} \) is properly performed, since the TCB code (and execution thereof) could itself be tampered with. To this end, GAROTA provides runtime protections that prevent any unprivileged/untrusted program from modifying the TCB code, i.e., the program memory region reserved for storing that code. (Recall that instructions execute in place, from program memory). GAROTA also monitors the execution of the TCB code to ensure that:

1. **Atomicity**: Execution is atomic (i.e., uninterrupted), from the TCB’s first instruction (legal entry), to its last instruction (legal exit);

2. **Non-malleability**: During execution, DMEM cannot be modified, other than by the TCB code itself, e.g., no modifications by other software or DMA controllers.

These two properties ensure that any potential malware residing on the MCU (i.e., compromised software outside TCB or compromised DMA controllers) cannot tamper with TCB execution.

GAROTA monitors TCB execution and, if a violation of any property (not just atomicity and non-malleability) occurs, it triggers an immediate MCU reset to a default trusted state where TCB code is the first component to execute. Therefore, any attempt to interfere with the TCB functionality or execution only causes the TCB to recover and re-execute, this time with the guarantee that unprivileged/untrusted applications cannot interfere.

Both trigger configurations and the TCB implementation are updatable at run-time, as long as the updates are performed from within the TCB itself. While this feature is not strictly required for security, we believe it provides flexibility/updata ability, while ensuring that untrusted software is still unable to modify GAROTA trusted components and configuration thereof. In Section 4.7 we also discuss how GAROTA can enforce TCB confidentiality, which is applicable to cases where \( \mathcal{F} \) implements cryptographic or privacy sensitive tasks.

Each sub-property in GAROTA is implemented, and individually optimized, as a separate GAROTA sub-module. These sub-modules are then composed and shown secure (when applied to the MCU machine model) using a combination of model-checking-based formal verification and an LTL counterexample checking-based formal verification and an LTL computer-checked proof. GAROTA modular design enables verifiability and minimalism, resulting in low hardware overhead and significantly higher confidence about the security provided by its design and implementation.

As shown in Figure 2, GAROTA is implemented as a hardware component that monitors a set of CPU signals to detect violations to required security properties. As such it does not interfere with the CPU core implementation, e.g., by modifying its behavior or instruction set. In subsequent sections we describe these properties in more detail and discuss their implementation and verification. Finally, we use a commodity FPGA to implement GAROTA atop the low-end MCU MSP430 and report on its overhead.

### 4 GAROTA in Detail

We now get into the details of GAROTA. The next section provides some background on LTL and formal verification; given some familiarity with these notions, it can be skipped.
4.1 LTL & Verification Approach

Formal Verification refers to the computer-aided process of proving that a system (e.g., hardware, software, or protocol) adheres to its well-specified goals. Thus, it assures that the system does not exhibit any unintended behavior, especially, in corner cases (rarely encountered conditions and/or execution paths) that humans tend to overlook.

To verify GAROTA, we use a combination of Model Checking and Theorem Proving, summarized next. In Model Checking, designs are specified in a formal computation model (e.g., as Finite State Machines or FSMs) and verified to adhere to formal logic specifications. The proof is performed through automated and exhaustive enumeration of all possible system states. If the desired specification is found not to hold for specific states (or transitions among them), a trace of the model that leads to the erroneous state is provided, and the implementation can then be fixed accordingly. As a consequence of exhaustive enumeration, proofs for complex systems that involve complex properties often do not scale well due to so-called “state explosion”.

To cope with that problem, our verification approach (in line with prior work [14][16]) is to specify each sub-property in GAROTA using Linear Temporal Logic (LTL) and verify each respective sub-module for compliance. In this process, our verification pipeline automatically converts digital hardware, described at Register Transfer Level (RTL) using Verilog, to Symbolic Model Verifier (SMV) [36] FSMs using Verilog2SMV [29]. The SMV representation is then fed to the well-known NuSMV [12] model-checker for verification against the specified LTL sub-properties. Finally, the composition of the LTL sub-properties (verified in the model-checking phase) is proven to achieve GAROTA end-to-end goals using an LTL theorem prover [19]. Our verification strategy is depicted in Figure 3.

Regular propositional logic includes propositional connectives, such as: conjunction ∧, disjunction ∨, negation ¬, and implication →. LTL augments it with temporal quantifiers, thus enabling sequential reasoning. In this paper, we are interested in the following temporal quantifiers:

- \( X \phi \) – next \( \phi \): holds if \( \phi \) is true at the next system state.
- \( F \phi \) – Future \( \phi \): holds if there exists a future state where \( \phi \) is true.
- \( G \phi \) – Globally \( \phi \): holds if for all future states \( \phi \) is true.
- \( \phi \ U \psi \) – \( \phi \) until \( \psi \): holds if there is a future state where \( \psi \) holds and \( \phi \) holds for all states prior to that.
- \( \phi \ W \psi \) – \( \phi \) weak until \( \psi \): holds if, assuming a future state where \( \psi \) holds, \( \phi \) holds for all states prior to that.

If \( \psi \) never becomes true, \( \phi \) must hold forever. Or, more formally: \( \phi W \psi \equiv (\phi U \psi) \lor G(\phi) \)

Note that, since GAROTA TCB is programmable and its code depends on the exact functionality \( f \) for each application domain, verification and correctness of any specific TCB code is not within our goals. We assume that the user is responsible for assuring correctness of the trusted code to be loaded atop GAROTA active RoT. This assumption is consistent with other programmable (though passive) RoTs, including those targeting higher-end devices, such as Intel SGX [28], and ARM TrustZone [7]. In many cases, we expect the TCB code to be minimal (see examples in Section 5), and thus unlikely to have bugs.

4.2 Notation, Machine Model, & Assumptions

This section discusses our machine and adversarial models. We start by overviewing them informally in Sections 4.2.1 [4][2.2] and 4.2.3 [42.2]. Then, Section 4.2.5 formalizes the machine model using LTL. For quick-reference, Table 1 summarizes the notation used in the rest of the paper.

4.2.1 CPU Hardware Signals

GAROTA neither modifies nor verifies the underlying CPU core/instruction set. It is assumed that the underlying CPU adheres to its specification and GAROTA is implemented as a standalone hardware module that runs in parallel with the CPU, and enforcing necessary guarantees in hardware. The following CPU signals are relevant to GAROTA:

- **H1 – Program Counter (PC):** PC always contains the address of the instruction being executed in the current CPU cycle.
- **H2 – Memory Address:** Whenever memory is read or written by the CPU, the data-address signal \( D_{addr} \) contains the address of the corresponding memory location. For a read access, a data read-enable bit \( R_{en} \) must be set, while for a write access, a data write-enable bit \( W_{en} \) must be set.
- **H3 – DMA:** Whenever a DMA controller attempts to access the main system memory, a DMA-address signal \( D_{MA_{addr}} \) reflects the address of the memory location being accessed and a DMA-enable bit \( D_{MA_{en}} \) must be set. DMA can not access memory when \( D_{MA_{en}} \) is off (logical zero).
when the MCU initializes for the first time. An MCU
first software to execute following successful completion of
code, i.e., TCB: reset boots or after a
ment, i.e., the first software to be executed whenever the MCU
points to $\text{PC}$ for the following restarts.
Instructions are executed in place. Hence, at runtime, $\text{PC}$ points to
the PMEM address storing the instruction being executed.

$\text{PMEM}_{\text{min}}$ – Address to the
PMEM address space.

$\text{PMEM}_{\text{max}}$ – Address to the
PMEM address space.

$\text{PMEM}$ – Region corresponding to the entire
program memory of the MCU: $\text{PMEM} = [\text{PMEM}_{\text{min}}, \text{PMEM}_{\text{max}}]$.

$\text{TCB}$ – Memory region reserved for the TCB’s
executable implementing $\mathcal{F}$: $\text{TCB} = [\text{TCB}_{\text{min}}, \text{TCB}_{\text{max}}]$, $\text{TCB} \in \text{PMEM}$.

$\text{INIT}$ – Memory region containing the MCU’s default
initialization code. $\mathcal{F}$: $\text{INIT} = [\text{INIT}_{\text{min}}, \text{INIT}_{\text{max}}]$. $\text{INIT} \in \text{PMEM}$.

reset – A 1-bit signal that reboots/resets the MCU
when set to logical 1.

Table 1: Notation Summary

**H4 – MCU Reset:** At the end of a successful reset routine,
all registers (including $\text{PC}$) are set to zero before resuming
normal software execution flow. Resets are handled by
the MCU in hardware. Thus, the reset handling routine can not
be modified. Once execution re-starts, PC is set to point to
the first instruction in the boot section of program memory,
referred to as $\text{INIT}$ (see M2 below). When a reset happens,
the corresponding reset signal is set. The same signal is also set
when the MCU initializes for the first time. An MCU reset also
resets its DMA controller, and any prior configuration thereof.
(DMA) behavior is configured by user software at runtime. By
default (i.e., after a reset) DMA is inactive.

**H5 – Interrupts:** Whenever an interrupt occurs, the correspond-
ing $\text{irq}$ signal is set. Interrupts may be globally enabled or dis-
abled in software. The 1-bit signal $\text{gie}$ always reflects whether
or not they are currently enabled. The default $\text{gie}$ state (i.e., at
boot or after a reset) is disabled (logical zero).

### 4.2.2 Memory: Layout & Initial Configuration

As far as MCU initial memory layout and its initial software
configuration (set at, or prior to, its deployment), the following
are relevant to GAROTA:

**M1 – PMEM:** Corresponds to the entire $\text{PMEM}$ address space.
Instructions are executed in place. Hence, at runtime, $\text{PC}$ points to
the PMEM address storing the instruction being executed.

**M2 – INIT:** Section of $\text{PMEM}$ containing the MCU boot seg-
ment, i.e., the first software to be executed whenever the MCU
boots or after a reset. We assume $\text{INIT}$ code is finite.

**M3 – TCB:** Section of $\text{PMEM}$ reserved for GAROTA trusted
code, i.e., $\mathcal{F}$. TCB is located immediately after $\text{INIT}$; it is the
first software to execute following successful completion of
$\text{INIT}$.

**M4 – IRQ-Table and Handlers:** IRQ-Table is located in
$\text{PMEM}$ and contains pointers to the addresses of so-called
interrupt handlers. When an interrupt occurs, the MCU hard-
ware causes a jump to the corresponding handler routine. The
address of this routine is specified by the IRQ-Table fixed index
corresponding to that particular interrupt. Handler routines are
code segments (functions) also stored in $\text{PMEM}$.

**M5 – IRQ$\text{cfg}$:** Set of registers in $\text{DMEM}$ used to configure
specific behavior of individual interrupts at runtime, e.g., deadline
of a timer-based interrupt, or type of event on a hardware-based
interrupt.

Note that the initial memory configuration can be changed at
run-time (e.g., by malware that infects the device, as discussed in
Section 4.2.4), unless it is explicitly protected by GAROTA
verified hardware modules.

### 4.2.3 Initial Trigger Configuration

**T1 – trigger:** GAROTA trigger is configured, at MCU
(pre)deployment-time, by setting the corresponding entry in
IRQ-Table and respective handler to jump to the first instruction
in TCB ($\text{TCB}_{\text{min}}$) and by configuring the registers in $\text{IRQ}_{\text{cfg}}$
with desired interrupt parameters, reflecting the desired trigger
behavior; see Section 5 for examples. Thus, a trigger event
causes the TCB code to execute, as long as the initial configu-
ration is maintained.

Our initial configuration is not much different from a regular
interrupt configuration in a typical embedded system program.
It must correctly point to GAROTA TCB legal entry point, just
as regular interrupts must correctly point to their respective
handler entry points. For example, to initially configure a timer-
based trigger, the address in IRQ-Table corresponding to the
respective hardware timer is set to point to $\text{TCB}_{\text{min}}$ and the
correspondent registers in $\text{IRQ}_{\text{cfg}}$ are set to define the desired
interrupt period.

### 4.2.4 Adversarial Model

We consider an adversary $\mathcal{Adv}$ that controls $\mathcal{P}rv$’s entire
software state, including code, and data. $\mathcal{Adv}$ can read/
write from/to any memory that is not explicitly protected by
hardware-enforced access control rules. $\mathcal{Adv}$ might also have
full control over all Direct Memory Access (DMA) controllers of
$\mathcal{P}rv$. Recall that DMA allows a hardware controller to di-
rectly access main memory ($\text{PMEM}$ or $\text{DMEM}$) without going
through the CPU.

**Physical Attacks:** physical and hardware-focused attacks are
out of scope of GAROTA. Specifically, we assume that $\mathcal{Adv}$
can not modify induce hardware faults, or interfere with
GAROTA via physical presence attacks and/or side-channels.
Protection against such attacks is an orthogonal issue, which
can be addressed via physical security techniques [41].
Network DoS Attacks: we also consider out-of-scope all network DoS attacks whereby \(A_dv\) drops traffic to/from \(F_{rv}\), or floods \(F_{rv}\) with traffic, or simply jams communication. Note that this assumption is relevant only to network-triggered events, exemplified by the NetTCB instantiation of GAROTA, described in Section 5.3.

Correctness of TCB's Executable: we stress that the purpose of GAROTA is guaranteed execution of \(f\), as specified by the application developer and loaded onto GAROTA TCB at deployment time. Similar to existing RoTs (e.g., TEE-s in higher-end CPUs) GAROTA does not check correctness of, and absence of implementation bugs in, \(f\)'s implementation. In many applications, \(f\) code is minimal; see examples in Section 5. Moreover, correctness of \(f\) need not be assured. Since embedded applications are originally developed on more powerful devices (e.g., general-purpose computers), various vulnerability detection methods, e.g., fuzzing [11], static analysis [13], or formal verification, can be employed to avoid or detect implementation bugs in \(f\). All that can be performed off-line before loading \(f\) onto GAROTA TCB and the entire issue is orthogonal to GAROTA functionality.

4.2.5 Machine Model (Formally)

Based on the high-level properties discussed earlier in this section, we now formalize the subset (relevant to GAROTA) of the MCU machine model using LTL. Figure 4 presents our machine model as a set of LTL statements.

LTL statement (1) models the fact that modifications to a given memory address \(X\) can be done either via the CPU or DMA. Modifications by the CPU imply setting \(W_{en} = 1\) and \(D_{addr} = X\). If \(X\) is a memory region, rather than a single address, we denoted that a modification happened within the particular region by saying that \(D_{addr} \in X\), instead. Conversely, DMA modifications to region \(X\) require \(DMA_{en} = 1\) and \(DMA_{addr} \in X\). This models the MCU behaviors stated informally in H2 and H3.

In accordance with M4 and M5, a successful modification to a pre-configured trigger implies changing interrupt tables, interrupt handlers, or interrupt configuration registers (ICR-s). Since, per M4, the first two are located in PMEM, modifying them means writing to PMEM. The ICR is located in a DMEM location denoted \(IRQ_{cfg}\). Therefore, the LTL statement (2) models a successful misconfiguration of trigger as requiring a memory modification either within PMEM or within \(IRQ_{cfg}\), without causing an immediate system-wide reset (\(\neg reset\)). This is because an immediate reset prevents the modification attempt from taking effect (see H4).

LTL (3) models that attempts to disable interrupts are reflected by gie CPU signal (per H5). In order to successfully disable interrupts, \(A_dv\) must be able to switch interrupts from enabled \((gie = 1)\) to disabled \((\neg X(gie) \neg disabled)\) in the following cycle), without causing an MCU reset.

Recall that (from H1) \(PC\) reflects the address of the instruction currently executing. \(PC \in TCB\) implies that GAROTA TCB is currently executing. LTL (4) models T1. As long as the initial proper configuration of trigger is never modifiable by untrusted software \((G:\{\neg mod(\text{trigger}_{cfg}) \vee PC \in TCB}\)) and that untrusted software can never globally disable interrupts \((G:\{\neg \text{disable}(irq) \vee X(\text{PC} \in TCB)\})\), a trigger would always cause TCB execution \((G:\{\text{trigger} \rightarrow F(\text{PC} = TCB_{min})\})\). Recall that we assume that the TCB may update – though not misconfigure – trigger behavior, since the TCB is trusted. Similarly, LTL (5) states that, as long as \(PMEM\) is never modified by untrusted software, a \(reset\) will always trigger TCB execution (per H4, M2, and M3).

This concludes our formal model of the default behavior of low-end MCU-s considered in this work.

4.3 GAROTA End-To-End Goals Formally

Using the notation from Section 4.2, we proceed with the formal specification of GAROTA end-goals in LTL. Definition 2 specifies the “guaranteed trigger” property. It states in LTL that, whenever a trigger occurs, a TCB execution/invocation (starting at the legal entry point) will follow.

While Definition 2 guarantees that a particular interrupt of interest (trigger) will cause the TCB execution, it does not guarantee proper execution of the TCB code as a whole. The “re-trigger on failure” property (per Definition 3) stipulates that, whenever TCB starts execution (i.e., \(PC \in TCB\)), it must execute without interrupts or DMA interference \(\neg irq \neg dma_{en} \land PC \in TCB\). This condition must hold until:

1. \(PC = TCB_{max}\): the legal exit of TCB is reached, i.e., execution concluded successfully.
2. \(F(\text{PC} = TCB_{min})\): another TCB execution (from scratch) has been triggered to occur.

In other words, this specification reflects a cyclic requirement: either the security properties of the TCB proper execution are not violated, or TCB execution will re-start later.

Note that we use the quantifier Weak Until (W) instead regular Until (U), because, for some embedded applications, the TCB code may execute indefinitely; see Section 5.3 for one such example.

4.4 GAROTA Sub-Properties

Based on our machine model and GAROTA end-goals, we now postulate a set of necessary sub-properties to be implemented by GAROTA. Next, Section 4.3 shows that this minimal set of sub-properties suffices to achieve GAROTA end-to-end goals with a computer-checked proof. LTL specifications of the sub-properties are presented in Figure 6.

GAROTA enforces that only trusted updates are allowed to PMEM. GAROTA hardware issues a system-wide MCU reset.

\footnote{Since DMA could tamper with intermediate state/results in DMEM.}
Definition 1. Machine Model:
Memory Modifications:
\[ G: \{\text{modMem}(X) \rightarrow (\text{W}_{\text{en}} \land D_{\text{addr}} \in X) \lor (\text{DMA}_{\text{en}} \land D_{\text{addr}} \in X)\} \]

Successful Trigger Modification:
\[ G: \{\text{mod}(\text{trigger}_{X,fk}) \rightarrow [(\text{modMem}(\text{PMEM}) \lor \text{modMem}(\text{IRQ}_{X,fk})) \land \neg \text{reset}]\} \]

Successful Interrupt Disablement:
\[ G: \{\text{disable}(\text{irq}) \rightarrow \neg \text{reset} \land \neg \text{gie} \land \neg X(\text{gie}) \land \neg X(\text{reset})\} \]

Trigger/TCB Initialization [4] & [5]:
\[ G: \{\neg \text{mod}(\text{trigger}_{X,fk}) \lor PC \in TCB \} \land G: \{\neg \text{disable}(\text{irq}) \lor X(PC) \in TCB \} \rightarrow G: \{\text{trigger} \rightarrow F(PC = TCB_{\text{min}})\} \]

\[ G: \{\neg \text{modMem}(\text{PMEM}) \lor PC \in TCB \} \rightarrow G: \{\text{reset} \rightarrow F(PC = TCB_{\text{min}})\} \]

Figure 4: MCU machine model (subset) in LTL.

Definition 2. Guaranteed Trigger:
\[ G: \{\text{trigger} \rightarrow F(PC = TCB_{\text{min}})\} \]

Definition 3. Re-Trigger on Failure:
\[ G: \{PC \in TCB \rightarrow \{X(\text{irq} \land \neg \text{DMA}_{\text{en}} \land PC \in TCB) \} \lor (PC = TCB_{\text{max}} \land (PC = TCB_{\text{min}}))\} \]

Figure 5: Formal Specification of GAROTA end-to-end goals.

upon detecting any attempt to modify PMEM at runtime, unless this modification comes from the execution of the TCB code itself. This property is formalized in LTL [3]. It prevents any untrusted application software from misconfiguring IRQ-Table and interrupt handlers, as well as from modifying the INIT segment and the TCB code itself, because these sections are located within PMEM. As a side benefit, it also prevents attacks that attempt to physically wear off Flash (usually used to implement PMEM in low-end devices) by excessively and repeatedly overwriting it at runtime. Similarly, GAROTA prevents untrusted components from modifying IRQs to –DMEM registers controlling the trigger configuration. This is specified by LTL [7].

LTL [8] enforces that interrupts cannot be globally disabled by untrusted applications. Since, each trigger is based on interrupts, disablement of all interrupts would allow untrusted software to disable the trigger itself, and thus the active behavior of GAROTA. This requirement is specified by checking the relation between current and next values of gie, using the LTL neXt operator. In order to switch gie from logical 0 (current cycle) to 1 (next cycle), TCB must be executing when gie becomes 0 (X(PC) \in TCB), or the MCU will reset.

In order to assure that the TCB code is invoked and executed properly, GAROTA hardware implements LTL-s [9] and [11]. LTL [9] enforces that the only way for TCB’s execution to terminate, without causing a reset, is through its last instruction (its only legal exit): PC = TCB_{\text{max}}. This is specified by checking the relation between current and next PC values using LTL neXt operator. If the current PC value is within TCB, and next PC value is outside TCB, then either current PC value must be the address of TCB_{\text{max}}, or reset is set to 1 in the next cycle. Similarly, LTL [11] enforces that the only way for PC to enter TCB is through the very first instruction: TCB_{\text{min}}. This prevents TCB execution from starting at some point in the middle of TCB, thus making sure that TCB always executes in its entirety. Finally, LTL [10] enforces that reset is always set if interrupts or DMA modifications happen during TCB’s execution. Even though LTLs [9] and [11] already enforce that PC can not change to anywhere outside TCB, interrupts could be programmed to return to an arbitrary instruction within the TCB. Or, DMA could change DMEM values currently in use by TCB. Both of these events can alter TCB behavior and are treated as violations.

Next, Section 4.5 presents a computer-checked proof for the sufficiency of this set of sub-properties to imply GAROTA end-to-end goals. Then, Section 4.6 presents FSM-s from our Verilog implementation, that are formally verified to correctly implement each of these requirements.

4.5 GAROTA Composition Proof

GAROTA end-to-end sufficiency is stated in Theorems [4] and [5]. The complete computer-checked proofs (using Spot2.0 [19]) of Theorems [4] and [5] are publicly available at [6]. Below we present the intuition behind them.

Proof of Theorem [7] (Intuition). From machine model’s
Definition 4. LTL Sub-Properties implemented and enforced by GAROTA.

| Property                           | LTL Expression |
|-----------------------------------|----------------|
| Trusted PMEM Updates              | \( G : \{ \neg[PC \in TCB] \land W_{en} \land (D_{addr} \in PMEM) \lor [DMA_{en} \land (DMA_{addr} \in PMEM)] \rightarrow \text{reset} \} \) (6) |
| IRQ Configuration Protection      | \( G : \{ \neg[PC \in TCB] \land W_{en} \land (D_{addr} \in IRQ_{cfg}) \lor [DMA_{en} \land (DMA_{addr} \in IRQ_{cfg})] \rightarrow \text{reset} \} \) (7) |
| Interrupt Disablement Protection  | \( G : \{ \neg[PC \in TCB] \land W_{en} \land \lnot X(gie) \rightarrow X(PC \in TCB) \lor X(\text{reset}) \} \) (8) |
| TCB Execution Protection          | \( G : \{ \neg[PC \in TCB] \land (X(PC) \in TCB) \rightarrow (PC \in TCB_{max} \lor X(\text{reset})) \} \) (9) |
|                                    | \( G : \{ \neg[PC \in TCB] \land (X(PC) \in TCB) \rightarrow X(PC) = TCB_{min} \lor X(\text{reset}) \} \) (10) |
|                                    | \( G : \{(PC \in TCB) \land (irq \lor dma_{en}) \rightarrow \text{reset} \} \) (11) |

Figure 6: Formal specification of sub-properties verifiably implemented by GAROTA hardware module.

| Theorem 1. Definition 1 \( \land \) LTLs \( 6 \rightarrow \) Definition 2 |
| Theorem 2. Definition 1 \( \land \) LTLs \( 7-11 \rightarrow \) Definition 3 |

LTL 4, as long as the (1) initial trigger configuration is never modified outside the TCB; and (2) interrupts are never disabled from outside the TCB; it follows that a trigger will cause a proper invocation of the TCB code. Also, successful modifications to the trigger’s configuration imply writing to PMEM or IRQ_{cfg} without causing a reset (per LTL 2). Since GAROTA verified implementation guarantees that memory modifications (specified in LTL 1) to PMEM (LTL 6) or IRQ_{cfg} (LTL 7) always cause a reset, illegal modifications to trigger_{cfg} are never successful. Finally, LTL 8 assures that any illegal interrupt disablement always causes a reset, and is thus never successful). Therefore, GAROTA satisfies all necessary conditions to guarantee the goal in Definition 2.

Proof of Theorem 2 (Intuition). The fact that a reset always causes a later call to the TCB follows from the machine model’s LTL 5 and GAROTA guarantee in LTL 6. LTLs 8 and 9 ensure that the TCB executable is properly invoked and executes atomically, until its legal exit. Otherwise a reset flag is set, which (from the above argument) implies a new call to TCB. Finally, LTL 11 assures that any interrupt or DMA activity during TCB execution will cause a reset, thus triggering a future TCB call and satisfying Definition 3.

See 6 for the formal computer-checked proofs.

4.6 Sub-Module Implementation+Verification

Following the sufficiency proof in Section 4.5 for sub-properties in Definition 4, we proceed with the implementation and formal verification of GAROTA hardware using the NuSMV model-checker (see Section 4.7 for details).

GAROTA modules are implemented as Mealy FSMs (where outputs change with the current state and current inputs) in Verilog. Each FSM has one output: a local reset. GAROTA output reset is given by the disjunction (logic or) of local reset-s of all sub-modules. Thus, a violation detected by any sub-module causes GAROTA to trigger an immediate MCU reset. For the sake of easy presentation we do not explicitly represent the value of reset in the figures. Instead, we define the following implicit representation:

1. reset output is 1 whenever an FSM transitions to the RESET state (represented in red color);
2. reset output remains 1 until a transition leaving the RESET state is triggered;
3. reset output is 0 in all other states (represented in blue color).

Note that all FSM-s remain in the RESET state until PC = 0, which signals that the MCU reset routine finished.

Figure 7 illustrates GAROTA sub-module responsible for assuring that PMEM modifications are only allowed from within the TCB. This minimal 2-state machine works by monitoring PC, W_{en}, D_{addr}, DMA_{en}, and DMA_{addr} to detect illegal modification attempts by switching from RUN to RESET state, upon detection of any such action. It is verified to adhere to
LTL (6). A similar FSM is used to verifiably enforce LTL (7), with the only distinction of checking for writes within IRQ region instead, i.e., \( D_{addr} \in IRQ_{fg} \) and \( DMA_{addr} \in IRQ_{fg} \).

We omit the illustration of this FSM to conserve space, due to page limits.

Figure 8 presents an FSM implementing LTL[6]. It monitors the “global interrupt enable” (gie) signal to detect attempts to illegally disable interrupts. It consists of three states: (1) ON, representing execution periods where gie = 1; (2) OFF, for cases where gie = 0, and (3) RESET. To switch between ON and OFF states, this FSM requires \( PC \in TCB \), thus preventing misconfiguration by untrusted software.

Finally, the FSM in Figure 9 verifiably implements LTLs (8). This FSM has 5 states, one of which is RESET. Two basic states correspond to whenever: the TCB is executing (state “\( \in TCB \)”), and not executing (state “\( \notin TCB \)”). From \( \notin TCB \) the only reachable path to \( \in TCB \) is through state \( TCB_{entry} \), which requires \( PC = TCB_{min} \) – TCB only legal entry point. Similarly, from \( \in TCB \) the only reachable path to \( \notin TCB \) is through state \( TCB_{exit} \), which requires \( PC = TCB_{max} \) – TCB only legal exit. Also, in all states where \( PC \in TCB \) (including entry and exit transitions) this FSM requires DMA and interrupts to remain inactive. Any violation of these requirements, in any of the four regular states, causes the FSM transition to RESET, thus enforcing TCB execution protection.

### 4.7 TCB Confidentiality

One instance of GAROTA enables confidentiality of TCB data and code with respect to untrusted applications. This is of particular interest when \( f \) implements cryptographic functions or privacy-sensitive tasks.

This goal can be achieved by including and epilogue phase in the TCB executable, with the goal of performing a DMEM cleanup, erasing all traces of the TCB execution from the stack and heap. While the TCB execution may be interrupted before the execution of the epilogue phase, such an interruption will cause an MCU reset. The Re-Trigger on Failure property assures that TCB code will execute (as a whole) after any reset and will thus erase remaining execution traces from DMEM before subsequent execution of untrusted applications. In a similar vein, if confidentiality of the executable is desirable, it can be implemented following LTL (12), which formalizes read attempts based on \( R_{en} \) signal:

\[
G: \{ \{-(PC \in TCB) \land R_{en} \land (D_{addr} \in TCB) \lor \}
\quad \quad DMA_{en} \land (DMA_{addr} \in TCB) \Rightarrow reset \}
\]

An FSM implementing this property is shown in Figure 10. Note that, despite visual similarity with the FSM in Figure 7 the confidentiality FSM checks for reads (instead of writes) to the TCB (instead of entire PMEM).

This property prevents external reads to the TCB executable by monitoring \( R_{en} \), \( D_{addr} \), and DMA. When combined with the aforementioned erasure epilogue, it also enables secure storage of cryptographic secrets within the TCB binary (as in architectures such as [4],[5],[29]). This part of GAROTA design is optional, since some embedded applications do not require confidentiality, e.g., those discussed in Sections 5.1 and 5.2.

### 4.8 Resets & Availability

One important remaining issue is availability. For example, malware might interrupt (or tamper with) with INIT execution after a reset preventing the subsequent execution of TCB. Also,
malware could to interrupt the TCB execution, after each re-trigger, with the goal of resetting the MCU indefinitely, and thereby preventing TCB execution from ever completing its task.

We observe that such actions are not possible, since they would require either DMA activity or interrupts to: (1) hijack \texttt{INIT} control-flow; or (2) abuse \texttt{GAROTA} to successively \texttt{reset} the MCU during TCB execution after each re-trigger. Given \texttt{H5} interrupts are disabled by default at boot time. Additionally, \texttt{H4} states that any prior DMA configuration is cleared to the default disabled state after a \texttt{reset}. Hence, \texttt{INIT} and the first execution of TCB after a \texttt{reset} cannot be interrupted or tampered with by DMA.

Finally, we note that, despite preventing security violations by (and implementing re-trigger based on) resetting the MCU, \texttt{GAROTA} does not provide any advantage to malware that aims to simply disrupt execution of (non-TCB) applications by causing \texttt{resets}. Any software running on bare metal (including malware) can always intentionally reset the MCU. Resets are the default mechanism to recover from regular software faults on unmodified (off-the-shelf) low-end MCU-s, regardless of \texttt{GAROTA}.

5 Sample Applications

Many low-end MCU use-cases and applications can benefit from trigger-based active RoTs. To demonstrate generality of \texttt{GAROTA}, we prototyped three concrete examples, each with a different type of trigger-s. This section overviews these examples: (1) GPIO-TCB uses external analog events (Section 5.1), TimerTCB uses timers (Section 5.2), and NetTCB uses network events (Section 5.3). Finally, Section 5.4 discusses how \texttt{GAROTA} can match active security services proposed in [48] and [27].

5.1 GPIO-TCB: Critical Sensing+Actuation

The first example, GPIO-TCB, operates in the context of a safety-critical temperature sensor. We want to use \texttt{GAROTA} to assure that the sensor’s most safety-critical function – \textit{sounding an alarm} – is never prevented from executing due to software compromise of the underlying MCU. We use a standard built-in MCU interrupt, based on General Purpose Input/Output (GPIO) to implement trigger. Since this is our first example, we discuss GPIO-TCB in more detail than the other two.

As shown in Figure 11, MCU execution always starts by calling the TCB (at line 2). Therefore, after MCU initialization/reset, unprivileged (non-TCB) applications can only execute after the TCB; assuming, of course, that formal guarantees discussed in Section 4 hold. These applications are implemented inside \texttt{main\_loop} function (at line 3).

The correct trigger configuration in GPIO-TCB can be achieved in two ways. The first way is to set \texttt{IRQ\_cfg} to the desired parameters at MCU deployment time, by physically writing this configuration to \texttt{IRQ\_cfg}. The second option is to implement this configuration in software as a part of the TCB. Since the TCB is always the first to run after initialization/reset, it will configure \texttt{IRQ\_cfg} correctly, enabling subsequent trigger-s at runtime.

Figure 12 exemplifies \texttt{IRQ\_cfg} configuration, implemented as part of the TCB, i.e., called from within the TCB. This \texttt{setup} function is statically linked to be located inside the TCB memory region, thus respecting “TCB Execution Protection” LTL rules (see Definition 4). This \texttt{IRQ\_cfg} setup first configures the physical port \texttt{P1} as an input (line 2, “P1 direction” set to 0x00, whereas 0x01 would set it as an output). At line 3, \texttt{P1} is set as “interrupt-enabled” (P1IE = 0x01). A value of P1IES = 0x00 (line 4) indicates that, if the physical voltage input of P1 changes from logic 0 to 1 (“low-to-high” transition), a GPIO interrupt will be triggered and the respective handler will be called. Finally, P1IFG is cleared to indicate that the MCU is free to receive interrupts (as opposed to busy). We note that this initial trusted configuration of \texttt{IRQ\_cfg} cannot be modified afterwards by untrusted applications due to \texttt{GAROTA} guarantees (see Section 4). Based on this configuration, an analog temperature sensing circuit (i.e., a voltage divider implemented using a thermistor (i.e., a resistance thermometer – a resistor whose resistance varies with temperature) is connected to port P1. Resistances in this circuit are set to achieve 5V (logic 1) when temperature exceeds a fixed threshold, thus triggering a P1 interrupt.

P1 interrupt is handled by the function in Figure 13. This is configured using the \texttt{interrupt(PORT1\_VECTOR)} macro. This handler essentially calls \texttt{GAROTA} TCB. Parameter 1 in the TCB call distinguishes a regular TCB call from a TCB call following initialization/reset.

Figure 14 depicts the TCB implementation of f . Once triggered, TCB disables interrupts (\texttt{diis}), calls \texttt{setup} (if this is
the first TCB call after initialization/reset), and activates GPIO port P3 for a predefined number of cycles. P3 is connected to a buzzer (a high frequency oscillator circuit used for generating a buzzing sound), guaranteeing that the alarm will sound. Upon completion, TCB re-enables interrupts and returns control to the regular application(s).

Note that, as discussed in Section 4, executables corresponding to Figures 13 and 14 are also protected by GAROTA. Thus, their behavior cannot be modified by untrusted/compromised software.

5.2 TimerTCB: Secure Real-Time Scheduling

The second example of GAROTA, TimerTCB, is in the domain of real-time task scheduling. Without GAROTA (even in the presence of a passive RoT), a compromised MCU controlled by malware could ignore performing its periodic security- or safety-critical tasks. (Recall that targeted MCU-s typically run bare-metal software, with no OS support for preempting tasks). We show how GAROTA can ensure that a prescribed task, implemented within the TCB periodically executes.

Unlike our first example in Section 5.1, TimerTCB only requires modifying IRQcfg, as illustrated in Figure 15. This shows the relative ease of use of GAROTA. The setup function is modified to enable the MCU’s built-in timer to cause interrupts (at line 2). Interrupts are set to occur whenever the timer’s counter reaches a desired value (at line 3). The timer is set to increment the counter with edges of a particular MCU clock (MC1, at line 4). As in the first example, the corresponding interrupt handler is set to always call the TCB (Figure 16). In turn, the TCB can implement \( F \) as an arbitrary safety-critical periodic task.

5.3 NetTCB: Network Event-based trigger

The last example, NetTCB, uses network event-based trigger to ensure that the TCB quickly filters all received network packets to identify those that carry TCB-destined commands and take action. Incoming packets that do not contain such commands are ignored by the TCB and passed on to applications through the regular interface (i.e., reading from the UART buffer). In this example, we implement guaranteed receipt of external reset commands from some trusted remote entity. This functionality might be desirable after an MCU malfunction (e.g., due to a deadlock) is detected.

In NetTCB, trigger is configured to trap network events. IRQcfg is set such that each incoming UART message causes an interrupt, as shown in Figure 17. The TCB implementation, shown in Figure 18 filters messages based their initial character ‘r’ which is predefined as a command to reset the MCU. Note that: in practice such critical commands should be authenticated by the TCB. Although this authentication should be implemented within the TCB, we omit it from this discussion for the sake of simplicity, and refer to [22] for a discussion of authentication of external requests in this setting.

5.4 Comparison with [48] and [27]

Recent work proposed security services that can be interpreted as active RoT-s. However, these efforts aimed at higher-end embedded devices and require substantial hardware support: Authenticated Watchdog Timer (AWDT) implemented as a

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separate (stand-alone) microprocessor [48], or ARM TrustZone [27]. Each requirement is, by itself, far more expensive than the cost of a typical low-end MCU targeted in this paper (see Section 3). In terms of functionality, both [48] and [27] are based on timers. They use AWDT to force a reset of the device. As in GAROTA, in these designs, the TCB is the first code to execute; this property is referred to as “gated boot” in [48]. However, unlike GAROTA, [27, 48] do not consider active RoT behavior obtainable from other types of interrupts, e.g., as in GAROTA examples in Sections 5.1 and 5.3. We believe that this is partly because these designs were originally intended as an active means to enforce memory integrity, rather than a general approach to guaranteed execution of trusted tasks based on arbitrary trigger-s (as in GAROTA). Note that GAROTA design is general enough to realize an active means to enforce memory integrity. This can be achieved by incorporating an integrity-enforcing function (e.g., a suitable cryptographic keyed hash) into GAROTA TCB and using it to check PMEM state upon a timer-based trigger.

Finally, we emphasize that prior results involved neither formally specified designs nor formally verified open-source implementations. As discussed in Section 1 we believe these features to be important for eventual adoption of this type of architecture.

6 Implementation & Evaluation

We prototyped GAROTA (adhering to its architecture in Figure 2) using an open-source implementation of the popular MSP430 MCU – openMSP430 [25] from OpenCores. In addition to GAROTA module, we reserve, by default, 2 KBytes of PMEM for TCB functions. This size choice is configurable at manufacturing time and MCU-s manufactured for different purposes can choose different sizes. In our prototype, 2 KBytes is a reasonable choice, corresponding to 5 – 25% of the typical amount of PMEM in low-end MCU-s. The prototype supports one trigger of each type: timer-based, external hardware, and network. This support is achieved by implementing the IRQ_protection, as described in Section 4. The MCU already includes multiple timers and GPIO ports that can be selected to act as trigger-s. By default, one of each is used by our prototype. This enables the full set of types of applications discussed in Section 5.

As a proof-of-concept, we use Xilinx Vivado to synthesize our design and deploy it using the Basys3 Artix-7 FPGA board. Prototyping using FPGAs is common in both research and industry. Once a hardware design is synthesizable in an FPGA, the same design can be used to manufacture an Application-Specific Integrated Circuit (ASIC) at larger scale.

Hardware & Memory Overhead

Table 2 reports GAROTA hardware overhead as compared to unmodified OpenMSP430 [25]. Similar to the related work [3, 14, 16, 18, 37, 49], we consider hardware overhead in terms of additional Look-Up Tables (LUT-s) and registers. The increase in the number of LUT-s can be used as an estimate of the additional chip cost and size required for combinatorial logic, while the number of registers offers an estimate on the memory overhead required by the sequential logic in GAROTA FSMs.

GAROTA hardware overhead is small with respect to the unmodified MCU core – it requires 2.3% and 4.8% additional LUT-s and registers, respectively. In absolute numbers, GAROTA adds 33 registers and 42 LUT-s to the underlying MCU.

Runtime & Memory Overhead

We observed no discernible overhead for software execution time on the GAROTA-enabled MCU. This is expected, since GAROTA introduces no new instructions or modifications to the MSP430 ISA and to the application executables. GAROTA hardware runs in parallel with the original MSP430 CPU. Aside from the reserved PMEM space for storing the TCB code, GAROTA also does not incur any memory overhead. This behavior does not depend on the number of functions or triggers used inside the TCB.

Verification Cost

We verify GAROTA on an Ubuntu 18.04 machine running at 3.40GHz. Results are also shown in Table 2. GAROTA implementation verification requires checking 7 LTL statements. The overall verification pipeline (described in Section 5.1) is fast enough to run on a commodity desktop in quasi-real-time.

Comparison with Prior RoTs

To the best of our knowledge, GAROTA is the first active RoT targeting this lowest-end class of devices. Nonetheless, to provide a overhead point of reference and a comparison, we contrast GAROTA’s overhead with that of state-of-the-art passive RoTs in the same class. We note that the results from [27, 48] can not be compared to GAROTA quantitatively. As noted in Section 5.4 [48] relies on a standalone additional MCU and [27] on ARM TrustZone. Both of these are (by themselves) more expensive and sophisticated than the entire MSP430 MCU (and similar low-end MCUs in the same class). Our quantitative comparison focuses on VRASED [14], APEX [16], and SANCUS [37]; passive RoTs implemented on the same MCU and thus directly comparable (cost-wise). Table 5 provides a qualitative comparison between the aforementioned relevant designs. Figure 19 depicts the relative overhead (in %) of GAROTA, VRASED, APEX, and SANCUS with respect to the total hardware cost of the unmodified MSP430 MCU core.

In comparison with prior passive architectures, GAROTA presents lower hardware overhead. In part, this is due to the fact that it leverages interrupt hardware support already present in the underlying MCU to implement its triggers. SANCUS presents substantially higher cost as it implements task isolation and a cryptographic hash engine (for the purpose of verifying software integrity) in hardware. VRASED presents slightly higher cost than GAROTA. It also necessitates some properties that are similar to GAROTA’s (e.g., access control to particular

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Aside from closely related work in [48] and [27] (already discussed in Section 5.4), several efforts yielded passive RoT designs for resource-constrained low-end devices, along with formal specifications, formal verification and provable security. Low-end RoT-s fall into three general categories: software-based, hardware-based, or hybrid. Establishment of software-based RoT-s [23, 26, 30, 33, 43–45] relies on strong assumptions about precise timing and constant communication delays, which can be unrealistic in the IoT ecosystem. However, software-based RoT-s are the only viable choice for legacy devices that have no security-relevant hardware support. Hardware-based methods [32, 34, 35, 37, 40, 42–44] rely on security provided by dedicated hardware components (e.g., TPM [47] or ARM TrustZone [7]). However, the cost of such hardware is normally prohibitive for lower-end IoT devices. Hybrid RoT-s [9, 14, 16, 21, 31] aim to achieve security equivalent to hardware-based mechanisms, yet with lower hardware cost. They leverage minimal hardware support while relying on software to reduce the complexity of additional hardware.

In terms of functionality, such embedded RoT-s are passive. Upon receiving a request from an external trusted Verifier, they can generate unforgeable proofs for the state of the MCU or that certain actions were performed by the MCU. Security services implemented by passive RoT-s include: (1) memory integrity verification, i.e., remote attestation [5, 9, 14, 21, 31–37]; (2) verification of runtime properties, including control-flow and data-flow attestation [3–16, 18, 24, 35, 39, 46–49]; as well as (3) proofs of remote software updates, memory erasure, and system-wide resets [4, 8, 15]. As discussed in Section 1 and demonstrated in Section 5, several application domains and use-cases could greatly benefit from more active RoT-s. Therefore, the key motivation for GAROTA is to not only provide proofs that actions have been performed (if indeed they were), but also to assure that these actions will necessarily occur.

Formalization and formal verification of RoT-s for MCU-s is a topic that has recently attracted lots of attention due to the benefits discussed in Sections 1 and 5.1. VRASED [14] implemented the first formally verified hybrid remote attestation scheme. APEX [16] builds atop VRASED to implement and formally verify an architecture that enables proofs of remote execution of attested software. PURE [15] implements provably secure services for software updates, memory erasure, and system-wide resets atop VRASED’s RoT. Another recent result [10] formalized, and proved security of, a hardware-assisted mechanism to prevent leakage of secrets through time-based side-channel that can be abused by malware in control of the MCU interrupts. Inline with aforementioned work, GAROTA also formalizes its assumptions along with its goals and implements the first formally verified active RoT design.

### 7 Related Work

Aside from closely related work in [48] and [27] (already discussed in Section 5.4), several efforts yielded passive RoT designs for resource-constrained low-end devices, along with formal specifications, formal verification and provable security.

Low-end RoT-s fall into three general categories: software-based, hardware-based, or hybrid. Establishment of software-based RoT-s [23, 26, 30, 33, 43–45] relies on strong assumptions about precise timing and constant communication delays, which can be unrealistic in the IoT ecosystem. However, software-based RoT-s are the only viable choice for legacy devices that have no security-relevant hardware support. Hardware-based methods [32, 34, 35, 37, 40, 42–44] rely on security provided by dedicated hardware components (e.g., TPM [47] or ARM TrustZone [7]). However, the cost of such hardware is normally prohibitive for lower-end IoT devices. Hybrid RoT-s [9, 14, 16, 21, 31] aim to achieve security equivalent to hardware-based mechanisms, yet with lower hardware cost. They leverage minimal hardware support while relying on software to reduce the complexity of additional hardware.

In terms of functionality, such embedded RoT-s are passive. Upon receiving a request from an external trusted Verifier, they can generate unforgeable proofs for the state of the MCU or that certain actions were performed by the MCU. Security services implemented by passive RoT-s include: (1) memory integrity verification, i.e., remote attestation [5, 9, 14, 21, 31–37]; (2) verification of runtime properties, including control-flow and data-flow attestation [3–16, 18, 24, 35, 39, 46–49]; as well as (3) proofs of remote software updates, memory erasure, and system-wide resets [4, 8, 15]. As discussed in Section 1 and demonstrated in Section 5, several application domains and use-cases could greatly benefit from more active RoT-s. Therefore, the key motivation for GAROTA is to not only provide proofs that actions have been performed (if indeed they were), but also to assure that these actions will necessarily occur.

Formalization and formal verification of RoT-s for MCU-s is a topic that has recently attracted lots of attention due to the benefits discussed in Sections 1 and 5.1. VRASED [14] implemented the first formally verified hybrid remote attestation scheme. APEX [16] builds atop VRASED to implement and formally verify an architecture that enables proofs of remote execution of attested software. PURE [15] implements provably secure services for software updates, memory erasure, and system-wide resets atop VRASED’s RoT. Another recent result [10] formalized, and proved security of, a hardware-assisted mechanism to prevent leakage of secrets through time-based side-channel that can be abused by malware in control of the MCU interrupts. Inline with aforementioned work, GAROTA also formalizes its assumptions along with its goals and implements the first formally verified active RoT design.

### 8 Conclusions

This paper motivated and illustrated the design of GAROTA: an active RoT targeting low-end MCU-s used as platforms for embedded/IoT/CPS devices that perform safety-critical sens-
ing and actuation tasks. We believe that GAROTA is the first clean-slate design of a active RoT and the first one applicable to lowest-end MCU-s, which cannot host more sophisticated security components, such as ARM TrustZone, Intel SGX or TPM-s. We believe that this work is also the first formal treatment of the matter and the first active RoT to support a wide range of RoT trigger-s.

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