A Device Performance Data Acquisition System Based on Data Fusion Method

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Abstract. The data acquisition system is a system which collects the analog signal from the sensor, converts it into digital signal, then sends it to the computer for processing, and outputs the processing results in the form of demand. Based on the research of USB technology, this paper describes a data acquisition system based on data fusion technology, including hardware design, firmware design, device driver design and host application design. In the part of hardware design, this paper first describes the performance and characteristics of data acquisition chip, FPGA and USB2.0 interface chip, and then gives the specific hardware design scheme. In the part of firmware design, this paper first introduces the firmware architecture of FX2, and then introduces the firmware design of GPIF interface mode in detail. In the driver development part, this paper first introduces the WDM driver development model, and then completes the USB device driver design of the data acquisition system. Finally, the device performance data acquisition system based on data fusion method is completed with driver.

Keywords: Data Acquisition System, Bus Technology, Data Fusion, Performance Data Acquisition System

1. Introduction
Monitoring and control is an effective way to ensure the safety of train operation. The trains in service in China are basically equipped with a variety of monitoring and control equipment and systems (hereinafter referred to as train control equipment), among which the most representative are LKJ 2000 train operation monitoring and recording device, TAX2 locomotive safety information integrated monitoring device and train network control system (TCMS) [1]. At present, these on-board equipment are easy to form an information island in the process of train operation, and the monitoring and control information only circulates in the device or system [2-3]. It is difficult for train maintenance department, locomotive depot or information center of Railway Bureau to obtain real-time locomotive status information, safety information and monitoring information, which is not conducive to real-time train status monitoring and fault diagnosis. To solve this problem, Tang Guoping designed the LAIS train running status information system by using the existing wired and wireless networks of trains to realize the integration of LKJ2000, TAX2 and other equipment data [4]. On the basis of Tang Guoping's research [5], Zhang Qiping [6] integrated and improved the LAIS train operation status information system to make it more in line with the requirements of the Ministry of
Railways' informatization master plan. In view of the shortage of online train monitoring and control information sharing, the integration of locomotive safety information (data from LKJ and TAX), status information and monitoring information is realized by using vehicle-mounted information collection technology and communication technology [7].

The structure of the above system is complex, and there is no specific collection method and design scheme for train monitoring and control information collection. This paper analyzes the output data format of vehicle mounted TAX2 and TCMS equipment and the working principle of electrical interface, and improves UDP protocol to support congestion control method to improve the network utilization in the process of network transmission. From both hardware and software aspects, a multi-channel serial port train monitoring and control equipment data acquisition system based on Embedded Linux + ARM9 is designed, which aims at centralized data acquisition and processing of on-board TAX2 and TCMS equipment, and provides solutions for data acquisition of train control equipment for locomotive remote monitoring and fault diagnosis.

2. System principle analysis

2.1. Brief introduction of system principle
Combined with the electrical interface principle and data message format of train control equipment, the principle of data acquisition system of train control equipment is analyzed. The system schematic diagram is shown in Figure 1. In order to solve the difference of electrical characteristics of train control equipment interface and reduce the processing burden of data server, a data communication board is designed between the data acquisition end of train control equipment and the data server receiving end of data acquisition system, which plays a key role in the communication and interconnection between train control equipment and data server. As a special network node, the function of data communication board in the system is as follows:

(1) The data collected by the system for LKJ2000 is mainly TAX data, which adopts RS485 bus communication mode and baud rate is 28.8kb/s71. TAX data is converted from RS485 protocol to UDP/IP protocol by the data communication board, and sent to the on-board data server via Ethernet to complete a TAX data collection.

(2) To meet the complex and diverse requirements of TCMS system buses of different vehicle types, two types of data communication boards are designed to be connected with EI for collecting TCMS data: one communication interface based on HDLC (high-level data link control) protocol is used for collecting TCMS data of HXD3 locomotive. 1 RS422 communication interface is reserved for data acquisition of TCMS or other equipment of HXD2 locomotive. The collected TCMS data is processed by the data communication board and finally sent to the on-board data server via Ethernet.
2.2. UDP congestion control

The communication between the data communication board and the data server adopts UDP protocol, which is prone to packet loss and delay due to the lack of congestion control mechanism in the process of large amount of data transmission. This paper proposes an improved protocol based on UDP protocol, which realizes reliable congestion control of UDP through rate adjustment strategy. The following describes the specific implementation process of UDP congestion control.

(1) Detect network status

The congestion value $\text{diff}$ is defined as the ratio of the difference between the expected receiving time (ET) and the sending time (ST) and the sending time $[8-10]$:

$$\text{diff} = \frac{\text{abs}(ET - ST)}{ST} \times 100\% \quad (1)$$

The network congestion level divided by the network state is shown in Table 1, which is used to detect the network state. Where $\alpha$ is the upper limit of low network load, usually 2%. $\beta$ is the lower limit of mild congestion, usually 4%.

| Congestion level | 1  | 2 | 3     |
|------------------|----|---|-------|
| Network status   | Free | Good | Congestion |
| Diff interval    | $(0, \alpha)$ | $(\alpha, \beta)$ | $(\beta, 100\%)$ |

(2) Adjust the sending rate

At the end of the network state detection, the state of the network is determined, and the a-mad rate adjustment method is used to change the network state. In the network transmission of UDP protocol, the transmission rate changes in a certain range $[R_{\min}, R_{\max}]$, where $R_{\min}$ is the lower limit of the acceptable rate of UDP and $R_{\max}$ is the target rate. In the congestion avoidance phase, the transmission rate can be expressed as:

$$R = \begin{cases} 
\min(R + \alpha, R_{\max}), & 0 < \text{diff} < \alpha \\
R, & \alpha < \text{diff} < \beta \\
\max(R - \beta, R_{\min}), & \beta < \text{diff} < 100\% 
\end{cases} \quad (2)$$

3. System hardware and software design

3.1. Hardware design

The data communication board is the core component of the system. The hardware design principle is shown in Figure 2. According to the function, the hardware circuit can be divided into core processor module, Ethernet transmission module, data acquisition module, debugging module, power supply module, status indication module and other auxiliary modules.

![Figure 2](image-url)
The ARM926EJ-S core high performance processor based on Freescale i. MX287 series is adopted as the core processor, and its main frequency can reach 454 MHz. The 101100mb/s Ethernet MAC is integrated in the core board based on i. MX287 the Ethernet is accessed by extending the PHY Ethernet transceiver DP83848K and using HR60—1680 as the network isolator of Ethernet. According to the different electrical characteristics of the interface, the data acquisition module can be divided into one RS485 interface, one HDLC interface, one RS422 interface and one RS232 interface. The HDLC interface 13 circuit is connected with the enhanced serial communication controller Z85230 through the D0-D7 pins and control pins of the core processor, so that it can support the sending and receiving of HDLC protocol data in the data link layer. The power supply module is responsible for power supply. In order to ensure the normal operation of components and the stable operation of the system, measures such as adding zener diodes and overcurrent protection fuses have been taken. In addition, in order to improve the stability of Rs485 data acquisition module, a voltage stabilizing circuit based on DCR010505U power isolation chip is used to supply power to RSM3485Hr. In the status indication module, LED lights are added to indicate the working status of the communication board, i.e. power supply status, program running status, TAX2 communication status, TCMS communication status and Ethernet communication status.

3.2. Software framework design

According to the data acquisition requirements of TAX and TCMS, the data communication board adopts multi protocol data conversion design to meet the communication requirements between heterogeneous networks. The software framework is shown in Figure 3, including hardware layer, operating system layer and application layer. It can also be specifically divided into hardware layer, driver layer, core layer, interface layer, application layer and data layer.

The hardware layer mainly provides the electrical interface between the communication board and other devices, including one Ethernet connection 13 and four strings 13. Among them, the data bus D0 - D7 and control bus of i. MX287 core board are externally connected with Z85230 to realize the data receiving and transmitting operation based on HDLC protocol.

Figure 3 Communication board software framework

Operating system layer provides management and control schemes for the use and operation of hardware and software resources of communication board, mainly including Linux system boot file U-Boot, operating system kernel, root file system and device drivers, which include one Ethernet driver and four serial port drivers. After the Linux system is powered on, initialize the hardware, load the driver, and provide necessary services and corresponding interfaces for the application running.

The application layer provides the application program to realize the function of communication board, which mainly completes the data cache. The collected TAX data or TCMS data of LKJ2000 is cached in the data cache area, and finally the data is processed and forwarded according to the data type.
3.3. Software workflow design
In the network system, the communication events between the two layers of network are decomposed into two time-sharing asynchronous events for processing by using the data register mechanism. In the form, the communication protocol conversion between heterogeneous buses is completed, and the communication between heterogeneous networks is realized in essence. The data communication board of the system acts as UDP client-side talker in the Ethernet network layer, and the data server acts as UDP listener. In the process of data acquisition, the data communication board acts as Ethernet host, and uses UDP protocol to establish communication link with the vehicle data server. Its workflow is shown in Figure 4. The specific steps are as follows:

1. Read the configuration file and complete the interface mapping between serial port and Ethernet;
2. Initialize Socket for device IP, and establish UDP connection between data communication board and data server;
3. After the socket connection is successful, read the data packet in the data buffer, judge the data type, and call the corresponding data processing function
4. If the data is HDLC data, call the HDLCtoEthTask task function, process and encapsulate the HDLC data in the buffer into UDP/IP protocol data, and forward it to Ethernet.
5. If it is uART1 data, call the 485toEthTask function, first unpack RS485 data in the buffer, then pack it into Ethernet data message type conforming to UDP/IP protocol, and complete the subsequent queue data processing and forwarding.
6. The data processing of UART2 is similar to that of uart1.

![Figure 4 Work flow chart](image)

4. System test and analysis
In order to verify the functional integrity and reliability of the data acquisition system, TAX2 and TCMS data are simulated and tested. In this paper, a HXD3c in Nanning locomotive depot is taken as the test object, and the data waveform during TAX data acquisition is shown in fig. 5, and some results of TCMS data acquisition are shown in Table 2.

From Table 2, we can clearly see the state quantity and operation quantity on each network node of TCMS system, which can provide important factual basis for locomotive fault diagnosis. According to the data comparison, the accuracy of data acquisition is 100%. As shown in fig. 5, the oscillograph is used to monitor the transmission state data waveform in the process of TAX data acquisition, and the data packet waveform is stable and burr-free, which verifies the reliability of data communication board protocol conversion. Through TCMS data acquisition and analysis and TAX2 communication oscilloscope waveform capture test, it shows that the data acquisition system has complete functions, and the data acquisition is accurate, efficient and reliable.
Figure 5 Collect TAX data waveform

Table 2 Collect partial list of TCMS data

| Pantograph 1 raised | Pantograph 1 descending | Locomotive set speed / (km/h) | Actual speed of locomotive / (km/h) | Inlet pressure of cooling water for rack I / MPa | Outlet pressure of cooling water of rack I / MPa |
|---------------------|-------------------------|-------------------------------|-------------------------------------|-----------------------------------------------|-----------------------------------------------|
| 1                   | 0                       | 13                            | 0.1                                 | 2.22                                          | 0.47                                          |
| 1                   | 0                       | 13                            | 0.2                                 | 2.23                                          | 0.47                                          |
| 1                   | 0                       | 13                            | 0.3                                 | 2.19                                          | 0.48                                          |
| 1                   | 0                       | 13                            | 0.4                                 | 2.19                                          | 0.46                                          |
| 1                   | 0                       | 13                            | 0.5                                 | 2.21                                          | 0.46                                          |
| 1                   | 0                       | 13                            | 0.6                                 | 2.19                                          | 0.47                                          |
| 1                   | 0                       | 13                            | 0.8                                 | 2.21                                          | 0.47                                          |
| 1                   | 0                       | 13                            | 1                                   | 2.2                                           | 0.46                                          |
| 1                   | 0                       | 13                            | 1.1                                 | 2.2                                           | 0.46                                          |
| 1                   | 0                       | 13                            | 1.2                                 | 2.2                                           | 0.48                                          |

5. Conclusion
Based on the characteristics of train control equipment, an efficient and accurate data acquisition system for train control equipment is designed. The system solves the problems of independence and data concentration of various train control equipment. In the aspect of system design, it is lighter than the previous system, and easy to develop and maintain. In the experiment of data acquisition simulation test, it shows high data acquisition efficiency and accuracy, and meets the data acquisition requirements of train TAX2 and TCMS. The system has important reference value and wide application prospect in data acquisition of train control equipment.

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