TC: Throughput Centric Successive Cancellation Decoder Hardware Implementation for Polar Codes

Tiben Che, Jingwei Xu and Gwan Choi
Department of Electrical and Computer Engineering
Texas A&M University, College Station, Texas 77840
Email: \{ctb47321, xujw07, gchoi\}@tamu.edu

Abstract—This paper presents a hardware architecture of fast successive cancellation (SC) algorithm for polar codes, which significantly reduces the decoding latency and dramatically increases the throughput. Algorithmically, Fast SC algorithm suffers from the fact that its decoder scheduling and the consequent architecture depends on the code rate; this is a big challenge for rate-compatible system. However, by exploiting the homogeneous differences between the decoding processes of fast constituent polar codes and regular polar codes, the presented design is compatible with any rate. The scheduling plan and the intendedly designed process are also described. Results show that, compared with the 2b-SC-Precomputation decoder, known to be the fastest ASIC design of SC decoder, our proposed design can achieve at least 60% latency reduction for the codes with length $N = 1024$. For example, a latency reduction of 79.66% at the rate of 0.85 and 65.31% at the rate of 0.5. By using Nangate FreePDK 45nm process, proposed design can reach throughput up to 5.81 Gbps and 2.00 Gbps for (1024, 870) and (1024, 512) polar code, respectively.

I. INTRODUCTION

Recently, polar codes [1] have received significant attention due to its capability to achieve the capacity of binary-input memoryless symmetric channels with low-complexity encoding and decoding schemes. Successive cancellation (SC) [1], list successive cancellation (List-SC) [2] and belief propagation (BP) [3] are the three most common decoders proposed for polar codes. Among these, SC decoder is most promising for practical hardware implementation since its low $O(N \log N)$ complexity, where $N$ is the length of the code. Thus, many relevant hardware designs are proposed. The tree architecture and the line architecture of SC decoder are proposed in [4], with synthesis results using TMSC 65nm process. A more efficient semi-parallel SC decoder design is proposed for both tree architecture and line architecture [5]. An ASIC design of SC decoder in 180nm CMOS process is described in [6].

However, algorithmically, SC decoder suffers from high latency. Typically, for conventional SC decoder, its latency $(2N - 2)$ increases linearly with respect to the code length. This is a significant challenge for practical applications of SC decoder for real systems since polar codes work well only at very long code lengths. A lot of works have been done to reduce the latency of SC decoder from both hardware and algorithm aspects. In [7], a pre-computation method is used. This approach can reduce decoding latency from $2N - 2$ to $N - 1$ by updating the two outputs of basic channel polarizing kernel ($g$ node and $f$ node) at the same clock cycle. In [8], a 2-bit decoder for the last stage of SC decoding is used. This yields a $1.5N - 2$ latency. In [9] and [10], the simplified SC (SSC) decoder and maximum-likelihood SSC (ML-SSC) decoder are introduced. By observing the tree architecture of SC decoding, three constituent codes, called $N^0$, $N^1$ and $N^R$, are found. These three constituent codes can feed back the hard decision information immediately, without traversal, once they are activated. This can significantly reduce the latency of decoding some polar codes with a given architecture. Based on the concept of SSC and ML-SSC, two additional constituent codes, $N_{SPC}$ and $N_{REP}$, are found in [11]. These further reduce latency. This approach is refer to as fast SC decoder. Moreover, an array processing structure for FPGA implementation is also proposed in [11].

In this paper, a novel low latency hardware architecture of polar code decoding using fast SC algorithm is presented. Although fast SC algorithm naturally lacks flexibility for multiple rates, proposed design overcomes this disadvantage by utilizing the similarity between the decoding processes of fast constituent polar codes and regular polar codes. Corresponding scheduling plan is presented. We also provide the design details of the processing unit (PU) which is compatible with both regular polar code and constituent polar code. The comparison with other commonly discussed SC decoders is given. Compared with the 2b-SC-Precomputation decoder, the fastest ASIC design of SC decoder to best of our knowledge, the proposed design can achieve at least 60% latency reduction for polar code with length $N = 1024$. For example, a reduction of 79.66% at the rate of 0.85 and 65.31% at the rate of 0.5. The analysis of latency reduction with respect to code rates is also presented. It shows proposed architecture can yield a significant latency reduction especially at high code rate (code rate > 0.8). This is very promising for modern communication or data storage systems where high rate codes are desired. Synthesis results using Nangate FreePDK 45nm process shows the proposed design can reach throughput of up to 5.81 Gbps and 2.00 Gbps for (1024, 870) and (1024, 512) polar codes, respectively.

This paper is organized as follows. We start the paper by reviewing some necessary background including basic idea of polar code and SC decoder, the tree analysis method of polar code and the fast SC algorithm in section I. Then, the hardware implementation of proposed system is described in section III. After that, the synthesis results and relevant comparisons are discussed in section IV. Finally, the conclusion is in section V.

II. BACKGROUND

A. Polar Code

As described in [1], a polar code is constructed by exploiting channel polarization. Mathematically, polar codes are linear block codes of length $N = 2^n$. The transmitted codeword $x \triangleq (x_1, x_2, \cdots, x_N)$ is computed by

$$x = uG$$  \hspace{1cm} (1)
where \( G = F^\otimes m \), and \( F^\otimes m \) is the \( m \)-th Kronecker power of \( F = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} \). Each row of \( G \) is corresponding to an equivalent polarizing channel. For a \((N,k)\) polar code, \( k \) bits that carry source information in \( u \) are transmitted using the most reliable channels. These are refer to information bits. While the rest \( N-k \) bits, called frozen bits, are set to zeros and are placed at the least reliable channels. Determining the location of the information and frozen bits depends on the channel model and the channel quality is investigated in \cite{12}.

**B. Successive Cancellation Decoding**

Polar codes can be decoded using successive cancellation using a recursive approach. A length \( N \) polar code can be regarded as a concatenation of \((N \log_2 N)/2\) basic channel polarizing kernels. Decoding process begins with the channel output \( y \), then successively estimates the \( n \)-th bit at stage \( i \), say \( \hat{u}_i^0 \), in a recursive manner. Fig.1 shows a basic architecture of channel polarizing kernel, where \( \lambda \) stands for the log-likelihood ratio \( \text{LLR} \) defined as \( y \). The decoding direction is from right to left. The \( \lambda \) can be updated using the min-sum(MS) approximation according to the following rules:

\[
\begin{align*}
\lambda_0^{-1} &= f(\lambda_0^i, \lambda_1^i) = \text{sign}(\lambda_0^i)\text{sign}(\lambda_1^i)\min(|\lambda_0^i|, |\lambda_1^i|) \\
i &= 1, \quad \text{if } \lambda_0^i \geq 0 \\
i &= 1, \quad \text{otherwise} \\
\lambda_1^{-1} &= g(\hat{u}_0^{i-1}, \lambda_0^i, \lambda_1^i) = (1)\hat{u}_0^{i-1} \cdot \lambda_0^i + \lambda_1^i
\end{align*}
\]

When \( i = 1, \hat{u}_0^0 \) can be decided by:

\[
\hat{u}_0^0 = \begin{cases} 
0, & \text{if } \lambda_0^0 \geq 0 \\
1, & \text{otherwise}
\end{cases}
\]

The value of \( \hat{u} \) can be computed using following recursively way:

\[
\begin{align*}
\hat{u}_0^i &= \hat{u}_0^{i-1} \oplus \hat{u}_1^{i-1} \\
\hat{u}_1^i &= \hat{u}_1^{i-1} \oplus \hat{u}_1^{i-1}
\end{align*}
\]

**C. Tree Analysis of SC Decoding**

Since SC decoder works in a recursive manner, a binary tree is a natural representation for SC decoder where each node corresponds to a constituent code. The number of bits in one constituent node in stage \( i (i = 0, 1, 2, \ldots) \) is equal to \( \log_2 i \). Fig. 2a shows an example of 8 bits polar code. The inputs of root node are the LLRs of channel output. \( \alpha_v \) are the input LLRs from parent stage. \( \alpha_l \) and \( \alpha_r \) are the message passing from parent node to left child and right child, and can be computed according to Eq. (2) and Eq. (3), respectively. \( \beta_l \) and \( \beta_r \) are the hard decisions of each constituent code. \( \beta_v \) is the hard information needed to feedback to parent stage, and it can be computed by \( \beta_l \) and \( \beta_r \) via Eq. (5).

**D. Fast SC Algorithm**

The main idea of fast SC algorithm is illustrated in \cite{7, 9} and \cite{11}. By finding some certain pattern constituent polar codes, the hard decision of each leaf node and the feedback of the root node in the constituent code can be determined immediately, without traversing the entire tree, once the constituent polar code is activated. For a length \( N \) constituent code in non-systematic polar codes, \( \hat{u}_N \) is calculated by \( \hat{u}_N = \beta_N \cdot G_N \), where \( G_N \) is the generator matrix for length \( N \) polar code. We adopt 4 kinds of constituent polar code in our design. These are \( N^{01}, N^{11}, N^{SPC} \) and \( N^{REP} \), which are called fast constituent polar codes.

If all the leaf nodes in a constituent code are frozen, the parent node of such kind of constituent code is called \( N^{01} \) node. Since all the bits are frozen, there is no need to compute all the information inside recursively. We can set \( \beta_v \) to 0 immediately. If all the leaf nodes in a constituent code are information bits, the parent node of such kind of constituent code is called \( N^{11} \) node. \( \beta_v \) of \( N^{11} \) node can be directly decided via threshold detection which is similar to Eq. (4).

\( N^{SPC} \) and \( N^{REP} \) are two constituent codes containing both frozen bits and information bits. In a length \( N \) \( N^{SPC} \) codes, only the first leaf node is frozen. It renders the constituent codes as a rate \((N-1)/N\) single parity check (SPC) code. This code can be decoded by doing parity check with the least reliable bit which has the minimum absolute value of LLR. At the parent node, the hard decision \( HD_{vi} \) of each bit can be estimated via threshold detection which is similar to Eq. (4). The parity is calculated as

\[
\text{parity} = \sum_{i=1}^{N} HD_{vi}.
\]

Then, find the index of the least reliable bit via

\[
j = \arg \min_i |\alpha_{vi}|.
\]

Eventually, \( \beta_v \) is decided by

\[
\beta_v = \begin{cases}
HD_{vi} \oplus \text{parity}, & \text{when } i = j \\
HD_{vi}, & \text{otherwise}
\end{cases}
\]

In a length \( N \) \( N^{SPC} \) codes, only the last leaf node is information bit. In this case, all the \( \beta_v \) should be the same and are reflections of the information contained in the only one information bit. Thus, the decoding algorithm starts by summing all input LLRs and \( \beta_v \) is calculated as

\[
\beta_v = \begin{cases}
0, & \text{when } \sum_j \alpha_{vij} \geq 0; \\
1, & \text{otherwise}
\end{cases}
\]
Fig. 2b and Fig. 2c give examples of tree presentations of these four kinds constituting polar codes. Black circle and white circle stand for information bit and frozen bit, respectively. Actually, in [11], there is one more constituent polar code $N^r$ has been introduced. $N^r$ contains multiple frozen bits and information bits, and can be decoded by exhaustive-search maximum-likelihood (ML) algorithm. However, ML detection is not efficient in hardware, thus we do not adopt $N^r$ in our proposed design. $N^0$, $N^1$, $N^{SPC}$ and $N^{REP}$ constituent codes are prevalent in long length polar code [11], which allows us to gain a significant throughput improvement.

### III. Hardware Implementation

In this section, a novel hardware implementation of fast SC decoder is presented. For a polar code with a given length, different code rate yields different distribution of constituent polar codes. A thoughtfully-composed architecture should have the capability and flexibility to deal with different rates. By exploiting the homogeneity between the decoding processes of fast constituent polar codes and regular polar codes, our design supports a variety of rates. The scheduling scheme based on the proposed architecture is also discussed. Additionally, we develop an approach for sharing and reusing computational elements to achieve higher hardware efficiency. For instance, by sharing adder and comparator, the processing unit (PU) is compatible with both regular polar codes and fast constituent polar codes.

#### A. System Overview

As introduced in [5], tree architecture or line architecture for SC decoder is the most common. Line architecture has a higher hardware utilization but needs increased complexity in control module and memory access. Thus, we adopt tree architecture in our design. Fig. 3 shows an overview of proposed system when code length = 16. Processing unit (PU) performs the $f$ and $g$ functions in Eq. (2) and Eq. (3), respectively, and its arithmetic part is used to decode $N^{SPC}$ and $N^{REP}$ as well. Pre-computation technique is also used, which allows the left child node and right child node update in the same clock cycle. The PU used in stage 0 has a slight difference with ordinary PU. We denote it with PU0 in the figure. According to Eq. (7), the minimum LLR value needs to be found. The comparator tree is used to perform this since it inherently exists in the tree architecture of PUs. A judicious scheduling permits obtaining the minimum value at stage 0 and recording the choice of smaller input for each PU at each stage. After that, a backward operation implemented by a series of parity transmit unit (PTU) can help to locate the minimum one among the length $N$ $N^{SPC}$ constituent polar codes. Design details are illustrated in section III-C. The estimation of current bit in SC decoding is based on the information of previous decoded bits. This information is called partial sum. Thus, a partial sum generator (PSG) which can co-operate with decoding pipeline is also needed. We adopt the PSG introduced in [3] in our design, and it is compatible with our system. Thus, the design of PSG is not discussed in this paper.

#### B. Scheduling Scheme

In terms of tree presentation, SC decoder conventionally process one node in each clock cycle. Traversal of a subtree containing $N$ leaf nodes needs $2N - 2$ clock cycles. By using pre-computation as introduced in [7], which calculate all the possible value in Eq. (3) as the same clock cycle as Eq. (2) is calculated, the latency can be reduced to $N - 1$. Furthermore, if this subtree is belong to fast constituent polar codes, the latency can be further reduced.

For $N^0$, the feedback are all set to 0, and for $N^1$, the feedback is determined by hard decision of input LLRs. Both the two computations need only 1 clock cycle to generate feedback to previous stage after they are activated.

For $N^{SPC}$, according to Eq. (6), Eq. (7), and Eq. (8), we can tell that there are 3 operations needed. Finding the minimum LLR can be done by a comparator tree, which is naturally existed in SC decoder with tree architecture since every PU has a comparator for Eq. (2). For $N$ LLRs, finding the smallest one use $\log_2 N$ clock cycles. Meanwhile, we can obtain the parity bit when the minimum LLR is found, which is explained in the next subsection. After that, one more clock cycle is need for signal parity check which is done by a XOR gate. Thus, totally, decoding a length $N$ $N^{SPC}$ constituent polar code need $\log_2 N + 1$ clock cycles.

For $N^{REP}$, according to Eq. (9), an accumulation operation is needed. Similar to the comparator tree, an adder tree also exists in SC decoder within the tree architecture since every PU has an adder for Eq. (3). For a length $N$ $N^{REP}$ constituent polar code, it needs $\log_2 N$ clock cycles to decode.

Since we use the same PU for every stage except the last one, this architecture can deal with fast constituent polar code start from any stage. This property provides the flexibility for multiple rates, since polar codes with different rates do not have the uniform distribution of constituent polar codes.

Table I gives the summary of decoding latency for each
constituent polar code. $N^0$ and $N^1$ have time complexity $O(1)$ and $N^{SPC}$ and $N^{REP}$ have time complexity $O(\log_2 N)$. Compared with commonly discussed SC architecture in [3, 4] and [8], which all have linear time complexity $O(N)$, we can benefit significantly from proposed scheduling scheme in term of latency, especially with very large $N$. Fig. 3 shows the conventional tree presentation of 32-bit polar code and the simplified tree presentation of 32-bit polar code at rate 0.3125 and 0.6875. We can tell that both the number of nodes in these two simplified trees are significantly reduced. In the proposed design, we also adopt the pre-computation technique which allow us activate the left child node and right child node simultaneously. Table I lists the decoding scheduling schemes of 32-bit polar code using pre-computation SC decoder and proposed fast SC decoder at rate 0.3125 and 0.6875. Pre-computation SC decoder needs 31 clock cycles (CCs) to finish decoding, while fast SC decoder both only need 12 CCs at two different rates, which is much less than that of pre-computation SC decoder. Also note that the latency of two rates just happen to be the same in this example.

### C. Processing Unit Design

Fig. 5 shows design details of PU. A single PU can perform $f$ and $g$ functions in Eq. (2) and Eq. (3), respectively. Also a PU tree can help to find the minimum values or do accumulation for multiple inputs. In Fig. 5, $S$ stands for signed magnitude number and $C$ stands for 2’s complement number. Unlike the PU design in [8], in which data are initially stored as signed magnitude form, our design use 2’s complement as initial form. We do this for 2 reasons. 1) As Fig. 11 shows in [8], 4 number system convert modules are needed along the $g$ function path. However, according to synthesis result, we observe that the critical path of PU is along with the $g$ function path. By moving number system convert modules to the $f$ function path, which means using 2’s complement as initial data form, the critical path is still along with $g$ function path, but with significant reduction. 2) Number system convert modules are needed in $f$ function path if 2’s complement is used. $f$ function is a two input one output function, which means only three number system convert modules are needed. This is more hardware efficient. The benefits of this modification can be seen in section 4.

For each PU, two LLRs are fed simultaneously. Since we use the pre-computation technique, $f$ and $g$ functions are calculated at the same time, and which one needs to be output is determined by mode select 2. According to Eq. (5), there are only two types of possible results for $g$ function, sum or difference. Its final result depends on the corresponding partial sum. So two registers are used here to hold the most recently computed values until the corresponding partial sum is calculated. When it calculates the sum for decoding $N^{REP}$, only additions are needed. The datapath is decided by Mode select 1 signal. When $f$ function is performed, according to Eq. (2), both 2 inputs are divided into two parts: sign bit and unsigned number. Each part is processed separately first, and then results of two parts are combined together to obtain the updated value. $C$ to $S$ and $S$ to $C$ modules are needed before and after comparisons, respectively. When it deals with $N^{SPC}$, the result of comparison should be recorded using a register as the select signal for PTU. Since the processing of searching minimum value lasts several clock cycles, there should be a feedback of the register to hold this value for the later clock cycles. The input source is chosen by Mode select 3 signal. Since every PU does exclusive or operation to the sign bit of two inputs, according to Eq. (6), the sign bit of the final value in stage 0 should be equal to the parity. Eq. (8) can be performed using an XOR gate. The PU that contains the minimum LLR receives the parity check bit and the others receive 0s. The transmission
of parity check bit is done by the PTU which is a two input two output module. One input is the parity check bit (PCB) and the other is the select signal (SS). The parity check bit is transmitted via output 1 (O1) or output 2 (O2) bases on the values of SS. Table III shows the truth table of PTU. We can obtain the logic expression of O1 and O2 as:

\[ O1 = PCB \text{ and SS}, O2 = PCB \text{ and SS} \]

This can be done by two \textit{and} gates and one \textit{Inverter}. The current hard-decision is the partial sum.

**TABLE III. TRUTH TABLE OF PTU**

| PCB | SS | O1 | O2 |
|-----|----|----|----|
| 0   | 0  | 0  | 0  |
| 0   | 1  | 0  | 0  |
| 1   | 0  | 0  | 0  |

The PTU in \textit{stage0}, as denote PU0 in Fig. 3, has a simpler architecture. Fig. 5 shows the design details of PU0. Since only one more clock cycle need for single parity check, there is no feed back to this register. Furthermore, \( N^{SPC} \) cannot exist in \textit{stage0}. So top part in Fig. 5 which is relative to single parity check can be removed. For \( f \) function and \( N^{REP} \), the output of \( f \) function can be feed back to it immediately, and the sign bit of the result of adding is the partial sum for \( N^{REP} \).

### D. Quantization Analysis

Fig. 2 shows the effect of quantization on the (1024, 512) polar code. For channel outputs and inner LLRs, we use separate quantization schemes. The quantization schemes are shown in \((C, L, F)\) format. Where \( C \) is the total number of bits used for presenting channel output, \( L \) is the total number of bits used for inner LLRs and \( F \) is the total number of bits used for fraction parts of both channel output and LLRs. Since no division used in the algorithm, which means the length of fraction does not change, channel output or inner LLRs use the same fraction precision.

From Fig. 2, we can observe that there are only about 0.1dB performance lost with \((4, 5, 0)\) scheme, and increasing 1 bit fraction precision based on that, namely \((5, 6, 1)\), yields less than 0.1dB increased on performance. However, if we try to reduce the precision on the channel output or inner LLRs by 1 bit, namely \((3, 5, 0)\) or \((4, 4, 0)\), respectively, they cause 0.4dB and 0.3dB performance loss. From these results above, we can get the conclusion that \((4, 5, 0)\) is the most hardware efficient quantization scheme in term of gain loss. We use such scheme in our design.

### IV. HARDWARE ANALYSIS AND COMPARISON

In this section, the comparisons between proposed design and other state-of-the-art designs are given, and synthesis results using Nangate FreePDK 45nm process are also presented. Table IV shows the hardware comparison of different \((n, k)\) SC decoders with \(q\)-bit quantization for inner LLRs.
using tree architectures. All the throughputs are normalized to the SC decoder in [4]. From this table, we can see that our proposed design has a significant latency reduction. The exact latency depends on the code rate. Fig. 8 shows the latency reduction of the proposed design along with code rates from 0.05 to 0.95. The reduction is relative to the 2b-SC-Precomputation decoder which so far is known to be the fastest. The figure shows at least 60% latency reduction can be achieved by our proposed design. The worst point is at the rate of about 0.4. Beyond that, the reduction increases along with the code rate. This is very promising for many applications where high rate channel codes are needed, such as for data storage system. This latency reduction is achieved with minimum hardware overhead. In our proposed design, additional \( n \) registers and \( n/2 - 1 \) PTUs are needed. Since the PTU only consists of two AND gate and one Inverter, and only one more register which is for selecte signal is added to the original 3q registers for each PU, this overhead is negligible.

Additionally, we implemented the proposed design with Verilog for the polar code with length=1024 and synthesized it using NanGate FreePDK 45nm process with Synopsys Design Compiler. We calculated the throughput for (1024,870) and (1024,512) polar codes. Table IV shows the synthesis result for (1024,870) and (1024,512) polar codes. Notice that the maximum frequency is higher than that reported in [8] which use the same process as our design. Our design in theory should have a lower maximum frequency since we have one more Mux delay for regular and fast constituent polar codes. This performance improving is attributable to the modification we have done to PU as described in section III-C.

**TABLE IV. HARDWARE COMPARISON OF DIFFERENT \((n, k)\) SC DECODER WITH q-BIT QUANTIZATION FOR INNER LLRS USING TREE ARCHITECTURE**

| Hardware Type | SC-Precomputation [7] | SC [8] | 2b-SC-Precomputation [8] | Proposed Design |
|---------------|-----------------------|--------|--------------------------|-----------------|
| # of PE       | \( n - 1 \)           | \( n - 1 \) | \( n - 2\) and \( 1 + p \) node) | \( n - 1 \) |
| # of PTU      | 0                     | 0      | 0                        | \( 2/n - 1 \) |
| # of 1 bit KEQ| \( \leq 35p \)         | \( \leq 3q \) | \( \leq 35p \)              | \( \leq (3q + 1) \) |
| Latency (clock cycle) | \( \leq 2n - 2 \) | 0.76\( n - 1 \) | \( \leq 0.3 \sim 0.11n \) (rate between 0.05 and 0.95) |
| Throughput (Normalized) | 2                    | 1      | 2.6/7                    | \( \leq 0.69 \sim 22.26 \) (rate between 0.05 and 0.95) |

**V. CONCLUSION**

In this paper, we proposed a hardware architecture of fast successive cancellation (SC) algorithm for polar codes. By exploiting the similarity between the decoding processing of fast constituent polar codes and regular polar codes, proposed design overcomes the disadvantage of fast SC decoder that lacking decoding flexibility with respect to multiple code rates. Corresponding scheduling plan and the intendedly designed processing unit (PU) are also described. Result shows that proposed design significantly increase the decoding throughput of polar codes compared with other state-of-art SC decoders.

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