A novel common-ground switched-capacitor five-level inverter with adaptive hysteresis current control for grid-connected applications

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Abstract
The aim of this paper is to present a new topology of single-phase transformerless inverters, which can be tied to the local grid as a low-scaled ac module system. The proposed topology offers a common ground between the neutral point of the ac grid and the negative terminal of the dc supply, and can properly alleviate the concern of variable common mode voltage and leakage current problems. This promising feature is acquired by the aim of both the switched-capacitor and charge pumped circuit cells. In order to inject a tightly controlled ac current to the grid, an adaptive hysteresis current controller scheme is also presented, which can guarantee almost fixed switching frequency operation of the involved power switches. A complete theoretical analysis, comparative study, and the relevant experimental results are also given to confirm the superior performance of the proposed topology.

1 | INTRODUCTION

Owing to the massive shortage in the conventional fuel-based sources, environmental pollution, and power regulation incentives enacted by the governments, use of renewable energy (RE)-based resources like photovoltaic (PV) modules have been more popular in the modern energy conversion systems. In the low-scaled single-phase grid-tied utilities, a PV panel can be directly connected to a power electronic converter with a single or two energy conversion stages operation. Apparently, single-stage energy conversion platform is more preferred since additional power losses of multi power processing stages can be avoided [1–3].

Alternatively, to achieve an appropriate voltage gain from the low-scaled PV panels and to reach the peak voltage value of the local grid, transformerless structures are of important. The main challenge in designing a suitable transformerless grid-tied converter is the grounding issue viewpoint. Here, the parasitic capacitance provided by the negative terminal of the PV panel, which is around 100 nF per 1 kW, makes a resonant path with the output side filter inductor and therefore the leakage current can be circulated through the inverter side [4–7]. The value of such leakage current must be limited to under 20 mA based on the NEC 690 and VDE 0126-1-1 IEEE standards [8].

Since the main element in generating the leakage current is the variable high frequency common mode voltage (CMV), various efforts have been recently put forward in both the topological improvement aspect and modulation process [9]. The overall CMV can be constant during each switching instant by the means of bipolar pulse width modulation (PWM) scheme. However, such a bipolar two-level output voltage causes undesirable switching losses and affects thereby the injected grid current quality [10]. Decoupling the PV source from the ac grid during the freewheeling period in unipolar three-level (3L) PWM schemes is one of the well-known approaches to alleviate the leakage current value. H5 [11], HERIC [12], Optimized H5 (OH5) [13], Variant H8 five-level (5L) [14], different types of H6 family [15, 16] and Dual buck [17] inverters are able to clamp the overall CMV on a half value of the dc bus at each switching instant.

Connecting the mid-point of the dc bus to the neutral point of the grid is also capable of making a constant CMV [18–20]. In this case, half bridge (HB) or neutral point clamp
(NPC) inverters are usually utilised; therefore, to meet the grid voltage amplitude requirement, the PV voltage must be doubled through the front-end step-up converters. The up-graded version of such converters named as active boost NPC five-level (ABNPC5L) inverter and dual T-type (D2T)-5L inverter structure have been recently introduced as well [21, 22]; however, to meet the peak voltage of a standard grid with 311 V peak voltage, at least a 320 V DC power supply is still needed in this case [21]. Regarding all these types of inverters, the leakage current can be mitigated; however, owing to the junction parasitic capacitors of the involved power switches, the overall value of the leakage current is reduced but never totally suppressed.

Alternatively, the common-ground transformerless inverters (CGTLIs) can suppress the leakage current through bypassing the CMV [23, 34]. In this case, the input and output negative terminals are simultaneously connected to each other; therefore, the CMV is short-circuited and the leakage current value would be almost zero. Yet, the principle of positive and negative sequence inverter’s output voltage generation is different and a charge pumped circuit (CPC) theory is needed to make a true AC waveform. Regarding this concept, [23] presented a virtual dc-link concept as an CPC module, where five power switches are integrated to make a 3L output voltage waveform. Another scheme of CPC-based 3L-CGTLI has been proposed in [24]; yet, additional power diodes are needed to provide an indirect charging path for such a virtual dc-link capacitor. Following, three different structures of CGTLIs were reported in [25]. Again, the same virtual DC-link concept as the CPC is used here, but the maximum number of inverter output voltage levels is only three and there is not any boosting feature for such circuits.

Use of inductors in CPC-based CGTLIs have also been conceptualized in [26, 27]. However, although the number of semiconductor devices is low, the output voltage is bipolar, which results in adopting larger value of the output filter. An advance version of the presented CGTLI in [27], which offers a buck-boosting feature with a 3L output voltage was also recommended in [28, 29]. In both these cases, an additional inductor has been involved in the CPC cell; hence, it might bring additional losses. To further improve the quality of the injected current to the grid through such CGTLIs, some advanced versions of the 3L and 5L-based structures have been presented recently, where the flying-capacitor (FC) and switched-capacitor (SC) concepts have been put forward [30–34].

Here, the 5L FC-based topologies presented in [30, 31] need the additional charge balancing control procedures to maintain the balanced voltage for the FC cell, while it possesses again a buck-type feature. Using the SC concept integrated into the CPC cell can make a boosting feature for the inverter’s output, while the charging/discharging operation of the involved capacitors can be inherent [32–34]. The major drawback of such SC-based topologies is the inrush current problem, which causes an undesirable current stresses for those semiconductor devices integrating into the changing loop of the involved capacitors. However, by designing an appropriate resonant circuit with a very small size of the resonant/quasi resonant inductor, this huge current stresses can be notably alleviated [37, 38].

Considering the above-mentioned literature review, a new 5L SC-based CGTLI topology is presented in this study. Herein, the concept of CPC cell mentioned as for the CGTLIs is implemented by the means of an SC cell, which gives a voltage boosting feature within a single-stage to the overall configuration. 5L output voltage generation can also make sense since only a small single inductor-based (L) filter is used at the output. Therefore, some difficulties like active damping issues and resonant problems that are associated with the higher order LC or LCL filters can be removed. Since the ultimate goal of CGTLIs is to inject a high quality AC current into the grid, an adaptive hysteretic current controller (AHCC) approach is also used in this study. The proposed AHCC tends to control the sinusoidal shape of the injected grid current. In this case, not only the fast dynamic response/zero steady state error is achieved, but also a fixed switching frequency operation of the involved switches can be attained. Moreover, the reactive power support capability can be fulfilled by the proposed topology.

Rest of this paper is organised as follows: The working principles and the operating procedures of the proposed SC-based five-level CGTLI is presented in Section 2. Then to regulate the injected current of the grid, the proposed AHCC technique is explained in Section 3. Voltage and current stress analysis are given in Section 4. Also, a comprehensive comparison with other recently proposed CGTLIs is conducted in Section 5, and finally the relevant experimental results under various types of test-bench grid-connected condition are shown in Section 6 to verify the accurate performance of the proposed system.

2 DESCRIPTION OF THE PROPOSED CGTLI TOPOLOGY

The proposed grid-tied CGTLI topology is depicted in Figure 1. As can be seen, it requires a SC cell including two bi-directional switches triggering with the same switching pulse \( S_{1a}, S_{1b}, S_{2a}, \) and \( S_{2b} \), a single capacitor paralleled to the dc supply, which can be assumed as the PV string panel, and a unidirectional power switch. This prominent SC cell can provide a two-time voltage boosting feature with series-parallel switched operation and can generate two different voltage levels \( V_d \) and \( 2 V_d \) in turn. Alternatively, in order to make a proper CGTLI structure, a CPC-based cell including the defined SC cell, a single power diode and another capacitor indicated as \( C_2 \) are also needed.

Different operating modes and current flowing paths of the proposed 5L-CGTLI have been illustrated in Figures 2 and 3. Here, it is supposed that the inverter input voltage \( V_{inv} \) is fixed at \( V_d \). Also, the red and blue lines respectively denote as the active grid current and capacitors’ charging flowing paths. Throughout the circuit description, \( V_{C1} \) and \( V_{C2} \) denote the voltage across the integrated capacitor of the SC cell \( C_1 \) and the CPC cell’s capacitor \( C_2 \), respectively, while \( V_D \) represents the voltage drop across the diode in the CPC’s cell. Here, \( V_{inv} \) specifies the instant value of the inverter output voltage also,
As can be seen, both the paralleled switches of the SC cell (path, irrespective of the direction of through the forward biasing of the integrated diode. Here, whereas

\[ I_{Grid} \]

whereas \( I_{Grid} \) is the grid’s current injected through the inverter. The proposed topology is operated within six different instants as follows:

To make the zero-level of the output voltage in the positive half-cycle (zero-positive), Figure 2(a) should be considered. In this case, both the capacitors are disconnected from the supply and the grid, while \( S_5 \) and \( S_6 \) must be in ON state.

In order to make the first positive level of the inverter’s output voltage (+\( V_{dc} \)), Figure 2(b) should be taken into account. As can be seen, both the paralleled switches of the SC cell (\( S_1 \) and \( S_2 \)) are conducted with the same switching pulse. Therefore irrespective of the direction of \( I_{Grid} \), \( C_1 \) is charged to \( V_{dc} \) and then through triggering the switch \( S_6 \), this voltage level appears at the output.

Regarding Figure 2(c), the top positive level of \( V_{inv} (+2V_{dc}) \) is made by turning ON the series switch in the SC cell (\( S_1 \)) and also the power switch \( S_5 \). As is clear from the current flowing path, irrespective of the direction of \( I_{Grid} \), \( C_2 \) is charged to the sum of supply’s voltage and \( V_{C1} \) by forward biasing the CPC’s power diode during this operating mode, while \( C_1 \) is discharged (charged) in the positive (negative) direction of the grid’s current. Here, once the reactive power support mode is needed, the reverse current of the grid can be flown into the supply through the SC cell capacitor and the anti-parallel body diode of \( S_3 \).

Considering Figure 3(a) and as for the negative half-cycle of the grid voltage, the zero-level of the inverter’s output voltage (zero negative) can be generated through an alternative path when \( C_1 \) is discharged by the turned ON switch \( S_3 \).

In this case, since \( V_{C1} + V_{dc} > V_{C2} \), \( V_{D} \) will be positive and in turns the diode will be ON; so \( C_2 \) is charged again to \( 2V_{dc} \) through the forward biasing of the integrated diode. Here, \( V_{inv} \) will be zero once the switch \( S_1 \) is to be turned ON. In this case, by changing the direction of \( I_{Grid} \) when the reactive power is demanded, \( C_1 \) and \( C_2 \) can also be charged and discharged, respectively. So, similar to the top positive level of the output voltage, the reverse current of the grid can be flown into the supply through the SC cell capacitor and the anti-parallel body diode of \( S_3 \).

Considering Figure 3(b), the first negative level of the \( V_{inv} (-2V_{dc}) \) is generated once both the paralleled switches of the SC cell and the power switch \( S_4 \) are turned ON. Herein, \( V_{C1} \) is equal to \( V_{dc} \) in every condition of the power injection, whereas the charging and discharging operation of \( C_2 \) depend on the direction of \( I_{Grid} \).

Finally, the negative top level of the \( V_{inv} (-2V_{dc}) \) is created by considering the current flowing path shown in Figure 3(c). Hereby, none of the integrated series-paralleled switches of the SC cell is involved in the grid current path; therefore \( C_1 \) is disconnected from the grid. However, by turning ON the power switches \( S_4 \) and \( S_5 \), \( C_2 \) is in charge of delivering the power to the grid. It is clear that once \( I_{Grid} \) is to be positive, \( C_2 \) is charged and once it turns to the opposite direction, \( C_2 \) is discharged.

From the above-mentioned descriptions, the following remarks can be realised:

- It is revealed that both the capacitors are periodically charged and discharged by the proposed series-paralleled switching scheme and their voltage can be balanced at \( V_{dc} \) and \( 2V_{dc} \) at the end of the fundamental cycle of the grid’s frequency.
- It is also clear that switches \( S_4 \) and \( S_5 \) are respectively in ON state during the negative and positive half-cycle of the grid’s waveform, whereas other remaining switches are modulated on the basis of the switching frequency. Therefore, such two mentioned switches can be selected as the low frequency power switches like insulated gate bipolar transistor (IGBT), and other ones can be chosen as high frequency-low loss switches like Si-MOSFET or SiC-MOSFET.

Apart from the two times voltage boosting property of the proposed CGTLI, low number of ON state power switches in each operating mode is another interesting feature of the proposed topology since excluding the middle-level of the inverter’s output voltage in both half cycle (\( \pm V_{dc} \)), only two out of six involved power switches are in ON state at each instant. Such feature makes an appropriate condition from the overall conduction loss viewpoint.

- The charging inrush current of the involved capacitors is another important point that is common among all the SC-based structures and it is worth addressing [32–34]. Here, only a single power switch (\( S_1 \)) and the power diode D of the CPC cell is in the charging path of \( C_2 \) (See Figure 2(c)), while \( S_1 \) and \( S_2 \) are involved into the charging path of \( C_1 \) (See Figures 2(b) and 3(b)). Details of current stress analysis is discussed in Section 4.

3 | PROPOSED AHCC PRINCIPLES

Basically, the ultimate contribution of a grid-connected CGTLI system is to inject a tightly controlled current into the grid. Such type of the controlled current can be indirectly provided
through the voltage-oriented control (VOC)-based techniques and use of Proportional and Resonant (PR) or Proportional and Integrator (PI) controllers; however, in single-phase applications, an orthogonal signal generation (OSG) block is needed to transfer the measured data into the stationary or synchronous reference frame. Here, apart from the computational burden of such transformations, an unwanted dynamic caused by the second order effects like fluctuations in the dc-link or variations in the grid’s frequency and the supposed OSG system may be included in the switching process, which impact the stability and robustness of the system [35].

Alternatively, to have a fast dynamic response and to achieve an immunity to any uncertain condition in the system parameters, the desired tightly controlled current can be acquired through the current controlled-based techniques, like dead-beat controller (DBC), model predictive control (MPC) or hysteresis, methods. However, both the DBC and MPC methods highly depend on the prediction of the next behaviour of the injected grid current over each sampling/switching time. The conventional fixed-band or sine-bands hysteresis approaches are also suffering from variable switching frequency, which imposes additional difficulties in predicting the output harmonic spectrum and designing an appropriate filter [35, 36]. In this section, an effective AHCC method is presented to modulate the gate of switches and control the injected grid current waveform of the proposed 5L-CGTLI, which can resemble the conventional unipolar PWM schemes of the VOC-based system and it is able to track a desired reference current with a fixed switching frequency operation. The proposed AHCC method is applicable to any kinds of the grid-connected 5L-inverter including the proposed topology. Herein, as opposed to the MPC or DBC approaches, instead of predicting the next behaviour of the injected grid current and comparing the reference signal with such a predicted value, some adaptive variable bands based on the actual shape of the current are defined once the inverter is switching in different switching states. Therefore, the measured current is compared with such variable bands similar to the conventional hysterisis controller and the desired levels per each switching state are generated.

To develop the variable bands of the proposed AHCC and regarding these explanations, the following continuous-time domain dynamic relation can be written as:

\[ v_{inv}(t) = L_g \frac{dI_{grid}(t)}{dt} + v_g(t) \]  

(1)

where, \( v_g(t) \) is the instantaneous value of the grid voltage, and \( I_{grid}(t) \) is the inductance of the output filter. Since \( V_{inv} \) is a switched voltage, \( I_{grid}(t) \) possesses two different components as expressed in Equation (2). Here, \( I_C(t) \) and \( i_g(t) \) respectively denote the fundamental frequency and ripple switching frequency component of the injected grid current. Therefore, Equation (1) can be rewritten as Equation (3).

\[ I_{grid}(t) = I_C(t) + i_g(t) \]  

(2)
FIGURE 4  A typical waveforms of (a) the inverter's output voltage and the ripple component of injected current during each switching cycle. (b) The adaptive bands and the defined zones waveform based on the inverter’s output voltage of proposed five-level CGTLI along with their associated gate switching pulses

\[ v_{in}(t) = L_g \frac{dI_g(t)}{dt} + I_g \frac{dI_g(t)}{dt} + v_g(t) \]  \hspace{1cm} (3)

From Equation (3), it is deduced that the average value of \( v_{in}(t) \) at each instant indicated as \( v_{in}(t) \) depends on the ripple switching frequency component of the grid’s current. A typical waveform of \( v_{in}(t) \) and \( I_g(t) \) has been shown in Figure 4(a), where, \( T_s \) is the effective switching period and \( t_{rise} \) is named as the rising time to reach the peak value of \( i_g(t) \). As it is clear, \( v_{in}(t) \) is regularly switched between the upper \( (V_{up}^{inv}) \) and lower level \( (V_{low}^{inv}) \) of the inverter’s output voltage during each switching period. Therefore, regarding Figure 3(a), \( v_{in}(t) \) can be expressed as:

\[ v_{in}(t) = \frac{1}{T_s} \left( V_{up}^{inv} t_{rise} + V_{low}^{inv} (T_s - t_{rise}) \right) \]  \hspace{1cm} (4)

On the other hand, since \( v_g(t) \) can be assumed as a constant variable during each high frequency switching period; hence, an adaptive current band can be defined which is varied in respect to \( v_{in}(t) \). Considering the volt-second balanced principle for \( L_g \) and regarding Equation (3), such a variable adaptive band is taken by Equation (5).

\[ 2\Delta i(t) = \frac{1}{L_g} \left( V_{up}^{inv} - v_g(t) \right) t_{rise} \]  \hspace{1cm} (5)

By rearranging Equation (4) and finding \( t_{rise} \), Equation (5) can be further simplified as Equation (6), which makes a relationship between the supposed adaptive band and the instant value of the inverter’s output voltage in each switching period.

\[ \Delta i(t) = \frac{T_s}{2L_g} \left( V_{up}^{inv} - v_g(t) \right) \left( \frac{v_{in}(t)}{V_{up}^{inv}} - \frac{V_{low}^{inv}}{V_{up}^{inv}} \right) \]  \hspace{1cm} (6)

Hence, unlike the conventional approach of the fixed-band hysteresis current controller scheme, the current bands of the proposed AHCC technique are variable and conform the mentioned relation in Equation (6) and therefore a fixed switching frequency as \( \frac{1}{2T_s} \) for all the high frequency switches can be achieved. Such a valuable achievement makes the prediction of the output harmonic spectrum possible whilst preserving all the mentioned advantages of the conventional hysteresis techniques. In order to apply such an adaptive band into the modulation process of the proposed five-level CGTLI, four different zones depending on the inverter output voltage levels should be defined.

Taking the first zone (Zone I) into account, the output voltage of the proposed CGTLI is switched between \( V_{dc} \) and \( 2V_{dc} \). So, regarding Equation (6), the adaptive band can be obtained as Equation (7) during this switching period.

\[ \Delta i_{Zone I}(t) = \frac{T_s}{2L_g} \left( 2V_{dc} - v_g(t) \right) \left( \frac{v_{in}(t)}{V_{dc}} - \frac{V_{low}^{inv}}{V_{up}^{inv}} \right) \]  \hspace{1cm} (7)

Once the inverter is to be switched between \( 0 \) and \( V_{dc} \), the second zone (Zone II) is defined and the supposed adaptive band is taken as follows:

\[ \Delta i_{Zone II}(t) = \frac{T_s}{2L_g} \left( V_{dc} - v_g(t) \right) \left( \frac{v_{in}(t)}{V_{dc}} - \frac{V_{low}^{inv}}{V_{up}^{inv}} \right) \]  \hspace{1cm} (8)
The same procedure is applied once the polarity of the inverter is to be negative. Here, the third and fourth operating zones (Zone III and Zone IV) belong to the regions specified as \(-V_{dc} \leq v_{inv}(t) \leq 0\) and, \(-2V_{dc} \leq v_{inv}(t) < -V_{dc}\), respectively. As a result, the adaptive current bands for the third and fourth operating zones are defined as Equations (9) and (10), respectively.

\[
\Delta i_{Zone\; III\;}(t) = \frac{T_s}{2L_g} \left(\frac{V_{dc} + v_{g}(t)}{V_{dc}}\right) v_{inv}(t)
\]

\[
\Delta i_{Zone\; IV\;}(t) = \frac{T_s}{2L_g} \left(2V_{dc} + v_{g}(t)\right) \left(\frac{v_{inv}(t) + V_{dc}}{V_{dc}}\right)
\]

Contemporary, with an assumption of having a sinusoidal grid voltage and a desired reference current at the unity power factor (PF), a sinusoidal function of \(v_{inv}(t)\) can be defined as follows:

\[
v_{inv}(t) = V_X \sin (\omega t + \delta)
\]

where, \(V_X\) and \(\delta\) are expressed as Equations (12) and (13), respectively.

\[
V_X = \sqrt{(\omega L_g I_m)^2 + V_m^2}
\]

\[
\delta = \tan^{-1}\frac{\omega L_g I_m}{V_m}
\]

where, \(\omega\), \(I_m\), and \(V_m\) respectively denote the angular grid frequency term, the peak of reference current (\(i_{ref}\)), and the peak voltage of the grid.

Also, to have the reactive power support control in non-unity PF, the values of \(V_X\) and \(\delta\) will change to Equations (14) and (15), respectively.

\[
V_X = \sqrt{(\omega L_g I_m \cos \phi)^2 + (V_m + \omega L_g I_m \sin \phi)^2}
\]

\[
\delta = \tan^{-1}\frac{\omega L_g I_m \cos \phi}{V_m + \omega L_g I_m \sin \phi}
\]

Now, regarding the above-mentioned calculations, a typical low frequency zoomed waveform of these defined bands in four operating zones tracking a sinusoidal function of the reference current with the gate switching pulses of the involved switches are depicted in Figure 4(b). Considering this, the upper and lower current bands’ function in each of the operating zones indicated by the red and blue lines is obtained as the following equation:

\[
\left\{
\begin{array}{l}
i_{ref, Zone\; i}(t) = i_{ref}(t) + \Delta i_{Zone\; i}(t) \\
i_{ref, Zone\; i}(t) = i_{ref}(t) - \Delta i_{Zone\; i}(t)
\end{array}\right. \quad i = I, II, III, IV
\]

where, \(i_{ref}(t)\) represents the desired reference current. The details of modulation process based on the proposed AHCC technique is provided in Table 1. As it is clear here, the control operation of the proposed AHCC technique depends on the overall behaviour of \(i_{ref}(t)\) in respect to the reference current within these quadrant defined zones at each instant.

### 4 Voltage and Current Stress Analysis

To further explore the operating condition of the involved semiconductor devices from the peak inverse voltage (PIV) and the current stress viewpoints, some analysis are conducted in this section.

As for addressing the PIVs, Table 2 can be considered. From this table, it is clear that excluding the paralleled bi-directional switches in the SC cell with \(\pm V_{dc}\) as the PIV, all the involved switches and power diode must bear a uniform stress voltage of \(2V_{dc}\) at their OFF-state condition, which is a helpful characteristic for design consideration of the switches. Therefore, total standing voltage (TSV) of the power switches will be \(10V_{dc}\) which is equal to five in the per-unit scale.

Also, the proposed 5L CGTLI topology is constructed based on the SC cell with a CPC concept as earlier explained. Therefore, once the capacitors are to be paralleled by the supply, the charging current of the involved capacitors is of important for the design consideration. Having taken such a charging current that is a common feature among all the SC-based inverters, the current stresses of the involved power switches that are involved in the charging path of the capacitors can be extremely high in which its maximum value is beyond four times more than the
peak of injected grid current [34]. Herein, use of a small size resonant inductor into the charging loop of the capacitors has been recommended by [21, 37, 38] to make a soft/quasi soft charging operation. Thanks to this and by the aim of a proper design for such a resonant inductor, the current stress of the charging operation can be deduced that it can be written as:

\[
\frac{R_{Ch,eq}}{2} \sqrt{\frac{1}{L_r}} = \frac{1}{\sqrt{2}} \text{ as the damping factor of the RLC circuit,}
\]

the correct value of \(L_r\) for the under damp operation of the capacitors charging loop RLC circuit can be taken by:

\[
L_r = \frac{C_{eq} \left( R_{Ch,eq} \right)^2}{4} \quad (18)
\]

Considering the fact that excluding the SC cell switches, all the remaining power switches of the proposed CGTLI have to pass only the injected grid current waveform and regarding the maximum charging current of the capacitors that can be obtained by Equation (17), the following expression as for the maximum current stresses of all the involved power switches can be written as:

\[
I_{S4,\text{max}} = I_{S5,\text{max}} = I_{S6,\text{max}} = I_m \quad (19)
\]

\[
I_{S1,\text{max}} = I_{S2,\text{max}} = I_m + i_{Ch,\text{max}} C_1 \quad (20)
\]

\[
I_{S3,\text{max}} = I_m + i_{Ch,\text{max}} C_2 \quad (21)
\]

Having taken the above-mentioned descriptions, the typical current stress waveform of all the involved power switches and capacitors along with the injected grid current waveform within a cycle of the grid frequency (\(T\)) are illustrated in Figure 6. Here, the equivalent parasitic resistance of the charging loop of the CPC cell is supposed to be around 2 ohm, and as for a 600 W application, \(C_1\) and \(C_2\) are chosen as 470 \(\mu\)F and 1 mF, respectively. So, regarding Equation (18), the resonant inductor will be around 33 \(\mu\)H, which is a very small value for the quasi soft charging operation of \(C_2\).

Here, the charging operation of the \(C_1\) would be also affected; however, since the voltage across the \(C_2\) is charged up to the higher voltage level than \(C_1\); therefore, the resonant inductor is designed based on the charging loop of \(C_2\). Here in Figure 6, the earlier discussed zone definition of the proposed controlled system can also be observed in the injected grid current waveform. It is also seen that the current stress of \(C_2\) in Zone IV offers quite the same shape as the grid current, while by the aim of the soft charging operation, the maximum current stresses of the SC cell power switches is reduced to around 3\(I_m\). Regarding Figure 6, the current stress profile expression of all the involved switches as well as their average and RMS values over a full fundamental grid cycle is summarised as Table 3. Here, all the current stress values have been calculated in respect to the peak value of the injected grid current through the help of MATLAB and their expressed profile function

\[\text{TABLE 2} \quad \text{PIVs of semiconductor devices in the proposed CGTLI topology}\]

| Respective devices | \(S_1\) | \(S_2\) | \(S_3\) | \(S_4\) | \(S_5\) | \(S_6\) | \(D\) |
|--------------------|--------|--------|--------|--------|--------|--------|------|
| PIV                | \(\pm V_a\) | \(\pm V_a\) | \(2V_a\) | \(2V_a\) | \(2V_a\) | \(2V_a\) | \(2V_a\) |

\[\text{FIGURE 5} \quad (a) \text{The soft charging loop of the involved capacitors, (b) the equivalent resonant charging circuit}\]
per each working zone. Here in Table 3, \(d(t)\) represents the steady-state sinusoidal duty cycle of the switches and its general function over a fundamental grid cycle is expressed as follows:

\[
d'(t) = \frac{V_X}{2V_{dc}} \sin(\omega t)
\]  

(22)

With respect to Equation (22), the PWM duty cycle of switches is calculated in each of the specified quadrant zone [34].

Considering the maximum PIV and the maximum current stress values of the switches, the injected output power ratio \(P_{out}\) should be less than the maximum allowable volt-ampere rating of the semiconductors as the following relation:

\[
P_{out} \leq 9V_{dc}I_{sw}
\]  

(23)

5 | COMPARATIVE STUDY

In this section, a comprehensive comparative study is conducted in order to confirm the superiority and effectiveness of the proposed 5L SC-based CGTLI over some other recently proposed topologies. Here, the selected topologies are able to either remove or mitigate the value of the leakage current; hence, they can be suitable for the transformerless grid-tied applications. Some of the most important items of the presented comparative study are number of requiring accompanying components, for example, switches (\(S_i\), gate drivers (\(G_i\)), diodes (\(D_i\)), capacitors (\(C_i\)) and inductors (\(L_i\)), along with the maximum number of ON state switches, the boosting feature, and also the maximum possible number of inverter's output voltage levels. In this case, a PV application is target; so all the used components including the DC decoupling capacitor and/or passive \(I\), \(L\) or \(LC\) filtering devices are accounted.

Moreover, the feasibility of different structures from per unit scale of the TSV of the power switches, maximum number of power switches that are involved into the charging path of the capacitors, the reported leakage current value, charged balancing control requirement for the capacitors, reactive power support capability and reported rated efficiency are checked.

Here, the leakage current value is considered low and very low if its RMS value is to be less than 100 and 10 mA, respectively [30]. Also, the charge-balancing control procedure of the capacitors is inspected as "not needed" when the structure is not based on the FC or SC converters. It is also counted "needed" once at least a voltage sensor is to be recruited to change the charging current direction of the capacitors. And finally, it is seen as inherent if all the involved DC-link capacitors are charged/discharged based on the switching conversion without any need of additional voltage sensors. The overall result of such specifications can be realised by Table 4.

As can be understood, among the various types of topologies, the proposed CGTLI and those presented in [14, 16, 19, 21, 22, 30, 31, 34] have an ability to generate a 5L of the output voltage. Therefore, a much lower value of the output filter can be used since the inverter's output voltage waveform and in consequence the injected current possess higher quality in contrast to others. In this case, the presented topologies in [14, 16, 19], and [30, 31] do not have any voltage boosting property and common-grounded (CG) feature. So higher range of input voltage is needed when a low-scaled PV panel feeds the inverter. Such necessity makes the energy conversion of the system double and affects the losses, as well. Also, the overall value of the leakage current for the structures in [14, 16, 19], is minimized but never totally suppressed, while in spite of having a CG feature for [30, 31], they need a precise FC voltage balancing procedure. The structure in [21] also does not have the CG feature. Even though it offers an inherent FC voltage balancing, its minimum required value of the input voltage is still 320 V. Here also, although the D2T5L inverter presented in [22] has a two-time voltage boosting capability like the proposed one, it lacks in having CG feature and needs much more number of active power switches. By contrast, the converter presented in [34] is SC-based like the proposed topology, so it offers a CG feature with a two-time voltage boosting ability. However, although its number of power switches is less than the proposed one (it requires seven switches but the proposed topology needs eight switches), its per unit value of the overall TSV and number of power switches that are involved into the capacitors charging loop is higher than the proposed one. In additional, the maximum PIV across the switches in [34] is \(4V_{dc}\), while this value for the proposed structure is \(2V_{dc}\). The higher value of PIV per switch causes higher maximum Volt–Ampere rating of the semiconductors for the structure presented in [34]. Therefore,
| Type of converters | No. of components | Max no. of ON-state switches | Boosting feature/Minimum input voltage*** | No. of levels TSV (pu) | Max no. of charging path switches | Leakage current Value | Capacitor charge balancing behaviour | Reactive power support | Reported efficiency |
|-------------------|-------------------|-----------------------------|----------------------------------------|------------------------|-------------------------------|---------------------|-------------------------------------|---------------------|-------------------|
| H5 [11]           | 5 5 – 2 2 3       | NO/320 V                    | 3                                      | 5 –                    | Low                           | Not Needed         | Yes                                 | 96.5%               |
| HERIC [12]        | 6 6 – 2 2 3       | NO/320 V                    | 3                                      | 5 –                    | Low                           | Not Needed         | NO                                 | 97%                 |
| OHS [13]          | 6 6 – 2 2 3       | NO/320 V                    | 3                                      | 5 –                    | Low                           | Not Needed         | NO                                 | 96.6%               |
| Variant H8 [14]   | 8 8 1 3 1 4       | NO/320 V                    | 5                                      | 6 2                    | Very Low                      | Inherent           | Yes                                 | 96.8%               |
| H6 [15]           | 6 6 – 1 2 3       | NO/320 V                    | 3                                      | 5 –                    | Low                           | Not Needed         | Yes                                 | 97.4%               |
|                  | 6 6 2 2 2         | NO/320 V                    | 5                                      | 5 –                    | Very Low                      | Needed             | NO                                 | 97%                 |
| Dual Buck [17]    | 6 6 – 2 2 2       | NO/320 V                    | 3                                      | 6 –                    | Low                           | Not Needed         | Yes                                 | 97.5%               |
| ANPC [19]         | 6 6 2 2 1 3       | NO/640 V                    | 5                                      | 5 –                    | Very Low                      | Needed             | NO                                 | NA                  |
| ABNPC [21]        | 8 6 – 3 1 3       | Yes/320 V                    | 5                                      | 5 2                    | Very Low                      | Inherent           | Yes                                 | 97.3%               |
| D2T-SC based [22] | 10 8 – 3 1 3      | Yes/160 V                    | 5                                      | 5 2                    | Very Low                      | Inherent           | NO                                 | 99%                 |
| CGTLI [23]        | 5 5 – 2 1 3       | NO/320 V                    | 3                                      | 5 2                    | Zero                          | Inherent           | Yes                                 | 97.8%               |
| CG-SC based [24]  | 4 4 2 4 2 2       | NO/320 V                    | 3                                      | 4 2                    | Zero                          | Inherent           | Yes                                 | 96.9%               |
| CGTLI Type I&II [25] | 4 4 1 3 1 2 | NO/320 V 4 5 1 | Zero | Inherent | Yes | 98% |
| CGTLI Type III    | 6 4 – 3 1 2       | NO/320 V                    | 3                                      | 6 2                    | Zero                          | Inherent           | Yes                                 | 96.9%               |
| CGTLI [26]        | 4 4 – 3 3 2       | Yes/160 V                    | 2                                      | 6 2                    | Zero                          | Inherent           | Yes                                 | 96.1%               |
| CGTLI Type II     | 5 5 – 2 2 2       | Yes/160 V                    | 3                                      | 5 –                    | Zero                          | Inherent           | Yes                                 | 96.5%               |
| CGTLI [29]        | 5 5 2 2 3         | NO/320 V                    | 3                                      | 5 2                    | Zero                          | Inherent           | NO                                 | 96.3%               |
| CG-FC based [30]  | 6 6 1 3 1 3       | NO/320 V                    | 5                                      | 5 2                    | Zero                          | Needed             | Yes                                 | 95.8%               |
| CG-FC based [31]  | 6 6 – 3 1 3       | NO/320 V                    | 5                                      | 5 2                    | Zero                          | Needed             | Yes                                 | 97%                 |
| CG-SC based [32]  | 7 6 1 3 1 3       | Yes/160 V                    | 3                                      | 5 4                    | Zero                          | Inherent           | Yes                                 | 98%                 |
| CG-SC based [33]  | 6 6 2 3 1 3       | Yes/160 V                    | 3                                      | 5 3                    | Zero                          | Inherent           | Yes                                 | 98%                 |
| CG-SC based [34]  | 7 6 1 3 1 3       | Yes/160 V                    | 5                                      | 6 4                    | Zero                          | Inherent           | Yes                                 | 98%                 |
| Proposed Topology | 8 6 1 3 3         | Yes/160 V                    | 5                                      | 5 3                    | Zero                          | Inherent           | Yes                                 | 98.2%               |

*Including the dc decoupling and pre-assumed filter capacitors; 
**Including the pre-assumed filter’s inductor(s); 
***The input voltage must be matched with a given standard grid with 311 V as the peak voltage.
FIGURE 7   A laboratory built prototype of the proposed topology

TABLE 5 Parameters used in experimental setup

| Parameters     | Type               | Description     |
|----------------|--------------------|-----------------|
| Power switches | IXKH47N60C          | 600 V/47 A      |
| Capacitors     | SMM series         | 0.47 mF & 1 mF/530 V |
| Filter inductor| EE128 Ferrite core | 3 mH            |
| Power diode    | MUR1560            | 600 V/15 A      |
| Gate drivers   | TLP250             | IC Chip         |
| Current transceiver | LEM 50 A     | Hall effect     |
| Micro controller| LAUNCHXL-F28379D  | Texas instrument|

overall efficiency of the proposed topology in contrast to others.

6 | EXPERIMENTAL RESULTS

In order to further confirm the feasibility and accurate performance of the proposed CGTLI and its corresponding AHCC technique, some experimental results are given in this section. Here, as shown in Figure 7, a 590 W prototype was built in order to extract the experimental results in which its specifications have been compiled in Table 5.

As for the experimental results, a PV simulator with a fixed dc voltage equals to 180 V has been used as the input dc voltage supply. To digitally implement the proposed AHCC technique through the LAUNCHXL-F28379D Texas Instruments (TI) controller, three feedbacks from the PV emulator, the grid voltage and also the injected grid current are required. The information of such mentioned feedbacks are obtained by the appropriate voltage and current sensors and they must be filtered out to be in compatible range of the above-mentioned TI controller (zero to 3.3 V). Such values are incorporated into three different analogue to digital conversion (ADC) pins of the TI controller. By selecting a proper sampling time, which corresponds to the operating fixed switching frequency (40 kHz), the implementation of the proposed AHCC is possible by the following steps:

its maximum power injection capability is lower than the proposed one. Also, its control platform is on basis of the variable switching frequency, while all its involved switches must be switched with a high switching frequency modulation. In turn, two of the involved power switches in the proposed CGTLI topology is modulated based on the grid-frequency, while the remaining ones are switched with a fixed AHCC switching frequency technique. This valuable feature can also improve the
1. Through the information of ADCs from the measured input dc source and the grid voltage, the instant switching zone of the proposed 5L-CGTLI is obtained.

2. Regarding the first step and considering Equations (7)–(10), the adaptive current band related to the detected switching zone is calculated. Here, to calculate the steady state sinusoidal function of \( v_{ref}(t) \) mentioned in Equations (11)–(15), a phase locked loop PLL block is also required. This can be established by applying a simple second order generalized integrator (SOGI)-based PLL [35].

3. A desired reference current, \( i_{ref}(t) \), corresponding to the unity or non-unity PF condition of the injected grid current is defined through the Code-Composer Studio software in the above-mentioned TI controller.

4. Regarding the previous steps and taking Equation (16) into account, the required upper and lower bands of the injected
grid current per each switching zone is defined and accordingly written into the Code Composer Studio Software.

5. Considering Table 1 and step 4, and concerning the instant information of ADC related to the measured current, the PWM signals of all the involved switching devices are provided.

Taking such observations into account, Figure 8(a) shows the grid voltage and the injected grid current waveform under the unity PF, whereas the 5L proposed CGTLI’s output voltage and the injected current waveforms have been illustrated in Figure 8(b). Such 5L output voltage along with the grid’s voltage waveforms have also been demonstrated in Figure 8(c). Here the maximum value of the injected grid current is about 3.8 A, which results in 590 W injected active power to the grid. Also, the peak of 5L inverter output voltage is 360 V which reflects the two-time voltage boosting ability of the proposed CGTLI.

Also, in order to show the effectiveness of the proposed AHCC, a zoomed waveform of the injected grid current within a full cycle of the grid frequency is given in Figure 8(d). It is clear from the results that all the adaptive bands could be properly created and therefore a high quality of the 5L waveform for the inverter’s output voltage with a maximum value of 360 V can be realized. In this case, by measuring the input and output powers, the measured efficiency is about 98.2%. To address the loss breakdown results and show the overall efficiency behaviour of the proposed topology over a wide range of the injected active output power with the described AHCC technique, Figure 9(a,b) can be considered. The information of the loss distribution results have been derived from an industry standard-based PLECS software. Here, the parasitic internal resistance of all the semiconductors compiled in Table 4 have been considered, while the ambient temperature is selected at 40 °C. In following, the balanced voltage waveforms of the capacitors along with their ripple waveforms can also be seen in Figure 10(a).

As can be seen, with the proposed series/parallel operation, C1 and C2 could be balanced at 180 and 360 V, respectively, which is in agreement with the theory presented. Regarding the incorporated resonant inductor, the experimental current stress profile of such capacitors can be also seen in Figure 10(b). As can also be observed, the peak of the charging current is around 8 A that is twice of the peak of the grid current and it is in agreement with typical results presented in Figure 6. In addition, in order to attest the reactive power support capability of the proposed system, a lead and lag phase shift have been applied on the reference current of the proposed AHCC technique. Therefore, the grid voltage and the injected grid current waveforms under the non-unity PF can be observed from Figure 11(a) and 11(b), respectively.

In both the cases, high quality of the injected current with a peak value of 3.8 A and the reported total harmonic distortion (THD) of less than 3% can be confirmed. A dynamic response of the injected grid current waveform when the PF is suddenly changed from the unity to a non-unity value and from a non-unity PF to unity PF one can also be observed in Figure 11(c) and 11(d), respectively. Obviously, the proposed AHCC technique can properly support different operating modes of the converter without any significant delay. In case of dynamic results shown in Figure 11(c) and 11(d), the quality of injected grid current waveform is little affected once the injected power is changed from 100% of the maximum test-bench power ratio to 50% one. This may be because of the calibration of the used Hall Effect current sensor since the injected grid current information including both the ripple and fundamental frequency has been calibrated by the sensor based on a 100% of the power ratio.

Finally, using the Fast Fourier Transform (FFT) tool of the MATLAB/SIMULINK software, the harmonic content of both the inverter output voltage and the injected grid current have been analysed as shown in Figure 12(a) and 12(b), respectively. Herein, the input voltage is again fixed at 180 V. Regarding Figure 12(a), the reported THD of the inverter 5L output voltage up to 50th cycles of the grid fundamental frequency is around 35.38%, while the amplitudes of all the sub-harmonic orders are around 0.1% of the fundamental component.
FIGURE 11  Experimental results for the measured grid voltage (green trace) [100 V/div] and injected current (blue trace) [4 A/div], (a) at leading PF, (b) at lagging PF, (c) under a dynamic condition from the unity PF to a non-unity one, (d) under a dynamic condition from non-unity PF to the unity PF one.

FIGURE 12  FFT analysis. (a) The output voltage spectrum of the proposed CGTLI up to fifth main harmonic. (b) A comparative spectrum analysis of the injected grid current between the fixed and variable switching frequency control approaches.

Also, in Figure 12(b), a comparative FFT study for the injected grid current waveform of the proposed inverter has been conducted, while the peak of $i_{g1}(t)$ has been supposed to be 5 A at the unity PF condition. Here, the FFT results of both the conventional hysteresis-based modulation technique, which results in a variable PWM switching frequency, and the proposed AHCC technique at the same condition (the same size of the inductor filter and the same value of the sampling/switching time) have been addressed. It is clear that the
harmonic content of the conventional hysteresis approach covers a wide range of sub-harmonics frequency since its switching frequency is variable, whereas on the basis of the proposed AHCC technique and through the adaptive variable bands, the major harmonic content is around the fixed switching frequency (40 kHz) and therefore it can easily be filtered out. Here, the injected grid current THD of the proposed AHCC technique is around 2.20%, while with the same parameters (the filter inductor and maximum switching frequency), the conventional fixed-band approaches gives around 4% as the grid current THD.

7 | CONCLUSION

A new single-phase 5L grid-connected inverter named as common-grounded transformerless inverter (CGTLI) has been presented in this work. By integrating the series-parallel operation in a switched-capacitor (SC) cell and using the charged pumped circuit (CPC) technique, a two-time voltage boosting property within a single-stage operation can be facilitated which results in employing a lower value of the input voltage. Also, a common grounding feature can be provided; hence, all the concern of removing the leakage current concern in the conventional transformerless inverters are alleviated. The capability of 5L output voltage generation with a reasonable count of power electronic elements is another promising feature of the proposed CGTLI. In order to avoid the computational burden of the conventional controlled schemes as for a grid-tied AC module application of the proposed topology, a hysteresis-based current controller strategy has also been developed in this study. The controller can govern both the required active and reactive powers through adapting the variable bands. Based on such an adaptive hysteresis current controller technique, a fixed switching frequency for high frequency switches can be acquired, which can ease the analysis of power losses and output waveforms spectrum. A complete comparative study from different aspects could also highlight other merits of the proposed CGTLI. And finally, some experimental results have been given around 2.20%, while with the same parameters (the filter inductor and maximum switching frequency), the conventional fixed-band approaches gives around 4% as the grid current THD.

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