A Synchronous Trigger Method of Parallel Tasks Suitable for Semiconductor Testing

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Abstract. With the rapid development of semiconductor chip technology, the role of parallel testing in the semiconductor testing is increasing. Aiming at the uncontrollable trigger delay caused by the test task startup delay, this paper proposes a parallel task synchronization trigger method for semiconductor testing. The LabWindows/CVI integrated development environment is used to implement the design and development. The method achieves the test task starting delay time stable and not subject to parallel number affects, then ensure the efficiency and stability of parallel testing.

1. Introduction
With the continuous development of electronic information technology and manufacturing technology, the production scale of semiconductor chips has been greatly improved, and the demand for testing is increasing with the day by day[1-2]. The traditional serial sequence test can only deal with one of the unit under test (UUT) test tasks at the same time or at the same time interval, and the efficiency of testing and the utilization of resources are low. The parallel test technology can perform multiple UUT test tasks at the same time. It can effectively improve test throughput and the utilization of test resources, and shorten the test time. Therefore, it has been widely used in the field of semiconductor testing[3]. However, the existing parallel test system is still in serial execution at the bottom layer, and the test trigger process is asynchronous processing, which is very easy to affect the test efficiency. Therefore, it is necessary to introduce synchronous trigger technology[4] to eliminate or reduce the impact of asynchronous processing on the testing process, so as to ensure the stability and efficiency of the parallel test system.

2. Semiconductor parallel testing
There are two models for parallel testing: the batch process model and the parallel process model [5]. In the batch process model, multiple UUT test tasks are used as a group to ensure that multiple UUT test tasks in the group begin to execute at the same time and wait for the processing to end simultaneously. In the parallel process model, each UUT test task is completely independent and does not affect each other. In comparison, the UUT must wait for the slowest UUT test task to end the test in the parallel process model, and it is obvious that the test time in the idle state is longer.

At present, the mainstream semiconductor testing system usually uses a test fixture to load a batch of UUT once, and performs these UUT test tasks concurrently. Therefore, it belongs to the batch process model. Because the parallel test environment usually uses a single processor non real time operating system (such as Windows), it is difficult to implement multiple UUT test tasks at the same time in strict meaning. It is only a multi-thread/multi-process concurrent processing in a very short

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time interval. As shown in Figure 1, on the whole, the operator firstly starts each of the UUT test tasks by operating the task operation interface. Then each UUT test task is executed independently and concurrently. There is no impact on each other and they take up processor time and instrument resource in turn. Locally, a single UUT test task is in order to adjust the test basic information and perform the various predetermined test actions until all test actions are completed. Depending on the situation, the next UUT continues to process, and the cycle is repeated until all UUT batch tests are completed.

Summed up, it can be said as "synthetically parallel asynchronous concurrent execution and local serialization sequence processing".

![Figure 1 The regular batch process model](image)

Obviously, there are shortcomings in this execution process: the time delays between the UUT test tasks from start to execution are increasing uncertainty, and this delay becomes more apparent as the increase of the concurrent UUT test tasks number. It makes the test process suffer the double effects of the longest UUT test task and the uncertainty time delay, so the stability of test efficiency is seriously reduced.

3. Parallel task synchronization triggering method

Aiming at the above problems, this paper achieves the test process control mechanism by designing the synchronous trigger for each UUT test task. This method can realize the synchronous trigger of the parallel task.

3.1 The design method of synchronous trigger

The design of synchronous trigger for UUT test task is the core of this method. The design method is as follows: using the high precision clock generator inside the processor and the asynchronous timer or thread pool mechanism provided by the operating system, the synchronous trigger is designed. The attribute parameter and function API of the synchronous trigger are provided.

Among them, the attribute parameters include control handle ID, trigger type, trigger state and trigger action. The control handle ID is the only value, the Convention greater than 0 is a normal state of success, less than 0 is an abnormal state of failure, equal to 0 that the trigger has been released, a
single synchronous trigger corresponds to a UUT test task, and a resource application, parameter configuration, function call and resource release through the control handle ID; Types include immediate execution and delay execution, delay time can be set, and time control accuracy is equal to the time delay of concurrent task execution (limited by processor clock generator counting time precision limit); triggered state includes two kinds of activation and invalid. The trigger action is executed on the trigger type and does not allow the trigger action to be registered again; the trigger action of the trigger in the invalid state is in the loss of execution ability and allows the trigger action to be registered; the trigger action allows the specified sequence of current valid test movements, the executable test application or The dynamic library pattern test application media file, the trigger action is executed immediately in the triggering activation state and automatically changes the trigger state after the normal end. The trigger action optimization design is required, not only to trigger the rapid automatic execution of ignition but also to be registered as other UUT test task application; the trigger type default setting is immediately executed, the trigger state default setting is invalid, and the trigger action default is registered as the UUT test task sequence.

The function API includes creating triggers, triggering type settings, triggering state settings, triggering action registers and releasing triggers.

3.2 Parallel test flow

Parallel triggers can be used for parallel testing, which can be divided into two steps. Step 1: the trigger attribute parameter setting and function call are used to complete the preadjustment and setting of the test process control options; step 2: after the parameter setting is completed, the operating user can start, stop, or exit the UUT test tasks.

Step 1: the adjustable control option parameters include the number of concurrency of the test station (the number of triggers) and the UUT test task application (corresponding trigger action); after the control option parameters are adjusted, the trigger is created and the trigger property parameters are set up according to the number of triggers, in which the trigger type is set to the immediate execution and trigger state settings are invalid and trigger action is registered as the selected UUT test task application.

Step 2: the start, stop or exit process of the UUT test tasks are shown in Figure 2, which includes the following steps:

Step 2.1: respond to human-machine interface interaction in the UUT test task interface. If the operation is started, step 2.2 is performed; otherwise, idle wait is continued.

Step 2.2: the trigger state of each UUT test task trigger is activated.

Step 2.3: the trigger actions corresponding to the trigger of each UUT test task are automatically executed according to preset settings, and the functions of each test task are ready.

Step 2.4: the trigger action of a single UUT test task trigger is executed, that is, the UUT test task application that adjusts the basic information of the UUT test, executes the registered triggering action, and notifications the UUT test task operation interface to perform the test execution state display;

Step 2.5: respond to the manual intervention performed by the user through the UUT test task interface. If the operation is stopped, the step 2.7 is executed.

Step 2.6: after the execution of the trigger action of a single UUT test task, the trigger state of the current trigger is invalid, waiting for all UUT test tasks to end, prompting and guiding the user to determine whether to handle the next UUT test task. If we deal with the next batch of UUT test tasks, then execute step 2.2; otherwise, continue to step 2.7.

Step 2.7: update UUT test process status display and user operation log display;

Step 2.8: respond to human-machine interface interaction in the UUT test task interface. If the operation is started, step 2.2 is performed; if the exit operation is performed, each trigger resource is released successively, and the related resources of the UUT test task operation interface are released.
4. Realization effect
Using the LabWindows/CVI of NI company as the application development environment, the software is designed and implemented. By designing the synchronous trigger, the delay time of the test task is stable and not affected by the number of parallel. The main control interface of parallel testing is shown in Figure 3. The main control interface mainly provides device type, device list, test basic information, test attribute information, parameter attribute, history record, trigger setting and test process management (start, stop, storage) function button.

Figure 2 The operation flow of UUT test tasks

Figure 3 The main control interface of the parallel testing
RS232 bus data collection class application is selected as an example of test application, and 2, 4, 8 and 16 test stations are used for the parallel testing. The triggering time comparison between the method of this paper and the conventional method is shown in Figure 4. It can be seen from the table that the test task delay time of the method in this paper is more stable and less influenced by the parallel number. The test task delay time of the conventional method is greatly influenced by the effect of the execution order, and it is seriously affected by the parallel number. When the batch process model is used for parallel testing, the whole test process will be affected by the longest UUT test task and the time delay. Therefore, compared with the conventional method, the method in this paper has a great improvement on the stability of test efficiency.

![Figure 4 The contrast of the trigger time](image)

5. Conclusion
In the field of semiconductor testing, a parallel task synchronization trigger method for semiconductor testing is proposed to improve the conventional parallel testing, which is due to the uncontrollable trigger delay caused by the start delay of the test task. The experimental verification is carried out by using the LabWindows/CVI integrated development environment. It can be seen from the experimental results that the starting delay time of this method is greatly reduced compared with the conventional parallel test method, and it has the advantage of delay time stability and without the influence of parallel number. It can ensure the efficiency and stability of parallel testing.

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