ACIC: Admission-Controlled Instruction Cache

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Abstract—The front end bottleneck in datacenter workloads has come under increased scrutiny, with the growing code footprint, involvement of numerous libraries and OS services, and the unpredictability in the instruction stream. Our examination of these workloads points to burstiness in accesses to instruction blocks, which has also been observed in data accesses [61]. Such burstiness is largely due to spatial and short-duration temporal localities, that LRU fails to recognize and optimize for, when a single cache caters to both forms of locality. Instead, we incorporate a small i-Filter as in previous works [29], [49] to separate spatial from temporal accesses. However, a simple separation does not suffice, and we additionally need to predict whether the block will continue to have temporal locality, after the burst of spatial locality. This combination of i-Filter and temporal locality predictor constitutes our Admission-Controlled Instruction Cache (ACIC). ACIC outperforms a number of state-of-the-art pollution reduction techniques (replacement algorithms, bypassing mechanisms, victim caches), providing 1.0223 speedup on the average over a baseline LRU based conventional i-cache (bridging over half of the gap between LRU and OPT) across several datacenter workloads.

I. INTRODUCTION

The front-end stalls in datacenter applications have come under much scrutiny in recent years. These applications have complex and deep software stacks, executing millions of instructions even for a single user query [5]. The consequent unpredictability in their control flow, involvement of numerous software layers (libraries and OS) beyond the application, and the resulting large code footprint have been noted to cause higher instruction cache (referred henceforth as i-cache) misses compared to the more conventional scientific and desktop workloads, like SPEC [1]. One can attempt to prefetch instruction blocks, and/or predict branches, based on anticipated control flow, which can help reduce i-cache misses and branch mispredictions. Another important angle for attacking this problem is by being more discretionary in what to bring and retain (replacement algorithm) within the precious and limited i-cache space. Taking the latter approach, this paper draws insights from prior work [61] that proposes dead block predictors based on bursty accesses to a cache block, and finds that such bursty accesses are also widespread in datacenter workloads, due to distinct spatial and temporal localities in the instruction stream, that are often not well serviced by the conventional LRU replacement algorithm in a single i-cache. Instead, the paper adds a separate and small (16-entry) buffer, whose similar/variant forms have been proposed in prior works [29], [49], to meet spatial localities, and implements an admission control mechanism to determine whether the block will continue to have temporal locality to justify bringing it into the i-cache. This Admission-Controlled Instruction Cache (ACIC) delivers 1.0223 speedup on the average across 10 datacenter applications 18.14% reduction in i-cache misses), buying back 55.85% of the performance loss of the baseline LRU over the oracle-based optimal (OPT) replacement algorithm that is theoretically possible.

While one may question the motivation for reducing i-cache misses given that it typically results in single-digit percentage speedups, as pointed out in [82], achieving even these single-digit percentage speedups is important to provide significant performance-per-watt benefits in these workloads. Consequently, there have been numerous studies looking to reduce i-cache misses [3], [21], [22], [28], [40], [41], [50]. These techniques can be categorized into: (i) prefetching mechanisms (whether purely in hardware [4], [21], [22], [42], [43], [52], [53], [76] or through profile-guided [6], [46] and compilation [2], [65] techniques); (ii) code re-layout optimizations for better instruction locality [13], [57], [62], [67], [69], [74]; and (iii) better management of i-cache space by controlling what should be brought in/replaced (e.g. GHRP [64], Ripple [47]). This work falls in category (iii), and we will show that it can complement some of the recently proposed prefetching techniques of category (i) as well.

Conventionally, the L1 instruction caches (i-cache) have been considered with a relatively small (4 or 8) associativity and a LRU-based replacement algorithm within a set. To a large extent, this structure has served its purpose fairly well for the much smaller code footprints. However, with the larger footprints of datacenter workloads, it is not clear whether the traditional LRU would work as well. This has also been a reason for some of the recent efforts such as GHRP [64] and Ripple [47] which have tried to improve the replacement mechanism by predicting reuse distances and identifying problematic program fragments. LRU relies on the recent past to predict the future, and may not be suitable for some of the bursty scenarios that we observe in emerging datacenter applications [16], [20], [70].

In this paper, we draw insight from prior work [61] which uses cache burst history, instead of cache access history, to predict dead blocks. Unsurprisingly, such bursty accesses are also common in the instruction stream of these datacenter workloads: (a) a block that is referenced, continues to experi-

§This work was done while the author was at Intel Labs.
ence considerable spatial and short-term temporal locality, i.e. a burst. This is fairly intuitive since successive instructions of the stream would fall in the same block. There is also short-term temporal locality due to locality in the recent branch targets, as pointed out in [21]. (b) after this burst, it is not very clear whether the block is more important than another block which may already be present in the i-cache. It may happen that after this burst, the block may not be needed for a long time (its reuse distance is much longer) that it better not be brought into the i-cache to result in pollution. A single i-cache with LRU-based replacement policy, would not differentiate between the accesses within a burst and those between bursts. This is a reason why streaming buffers [29], [39], [49], [68], separate caches for the two forms of locality [25], [56], [86], and/or cache bypassing schemes [37], have been proposed to handle the two localities differently.

Based on this observation, we add an i-Filter (whose similar forms have been proposed and studied in prior works [29], [49]), which is a 16-slot buffer for instruction blocks to handle the spatial and short-term temporal accesses. However, when this buffer becomes full, the victim cannot be simply evicted (then i-cache serves no purpose) or simply inserted into i-cache (which cause pollution). Instead, we need a prediction mechanism to determine whether its reuse distance (i.e. to the next burst) is shorter than a block already in the i-cache that it will replace. If so, and only then, should we bring it into i-cache. This overall mechanism, termed Admission-Controlled Instruction Cache (ACIC), provides the necessary spatio-temporal separation to differentially meet the intra-burst and inter-burst accesses that LRU is not tuned for.

This paper makes the following contributions to reduce i-cache misses in datacenter workloads:

- We show that accesses to an instruction block are bursty, similar to the observation for data accesses in [61], with a large number of spatial and near-term temporal accesses, rather than spread out over the execution.
- At the same time, one cannot ignore the separation between the bursts. LRU, in such cases, presumes the block will continue to be needed soon, thus reaching a wrong decision in bringing it into i-cache.
- Further, we cannot throw away the block after its burst is done either. With several blocks being needed, we need to be very discretionary about what to retain and what to throw away from the i-cache.
- We present the design of ACIC which provisions (i) a 16-entry i-Filter to temporarily hold incoming blocks for accesses during a burst, and (ii) a prediction mechanism to determine whether its reuse distance after the burst is shorter than a contender block already in its i-cache set, and filtering it out otherwise.
- Using a number of datacenter applications we show that ACIC reduces i-cache misses by 18.14% (with a standard fetch-directed prefetcher [31]). This results in a 1.0223 speedup, bridging over half of the gap between conventional LRU and OPT (which is not implementable). The hardware takes 2.67KB (around 2/3rd of some other

recent proposals) space and saves 0.63% chip energy over the baseline system.

- We also show that ACIC provides better performance than other recently proposed cache replacement policies (GHRP [64], SRRIP [34], SHIP [90], Hawkeye [32]/Harmony [33]), cache bypassing policies (DSB [23] and OBM [58] which were initially proposed for d-caches), and alternate strategies such as victim caches (VVC [44] which were earlier proposed for d-caches).

II. MOTIVATION

Need for Spatio-Temporal Separation: Inspired by prior work [61] which observes bursty accesses to data blocks and proposes better cache management policies based on such burstiness, we explore similar optimizations for the instruction stream in datacenter workloads [16], [20], [70]. We first study the reuse distances of instruction blocks in server workloads, previously identified to have a front-end bottleneck. Figure 1a plots the distribution of reuse distances between current and previous accesses to the same instruction block. They are histogrammed into buckets on the x-axis for interesting reuse distance ranges (0 implies spatial locality to the same block, 1-16 for very short-term temporal locality, 16-512 captures the size of an i-cache, 512-1024 for distances just out-of-reach of i-cache, and much larger reuse distances (1024-10000).

In around 85% of the cases, an instruction block continues to be re-accessed, indicating strong spatial locality (due to successive instructions lying in the same block). This is typically followed by the [1-16] bucket, indicating high short-term temporal locality. While the log-scale in y-axis does indicate a significant drop as we move beyond reuse-distances that can be captured by today’s i-cache sizes (until 512), there is a non-negligible fraction (up to 6%) that falls beyond the reach of i-cache. While one would think these misses could be ignored, such misses can still amount to as much as 8.23% loss in speedup in some applications (due to the cost of servicing a miss). This is the region that this paper sets out to optimize. Incidentally, note that even an oracle-based Belady’s OPT replacement algorithm [9], tries to optimize for this region.

To further illustrate the spatial locality, in Figure 1b, we show the correlation between successive reuse distances as a Markov Chain in Media Streaming. Each state represents the range of reuse distances, and the transition from one to another indicates the probability of the next reuse distance from the current reuse distance. Again, the self-transitions/transitions into the smallest reuse distance states (particularly 0) dominate. This diagram indicates the “burstiness” of accesses to instruction blocks, i.e. once a block is referenced, it continues to get referenced for a while (largely due to spatial locality) as is illustrated in the diagram on top of Figure 1b. After this burst, its reuse distance can become long again. When this happens, LRU-like schemes which look at the past (rather than the future), try to retain rather than evict such blocks.

1In this work, the term reuse distance is defined similar to stack distance of LRU, i.e. the number of unique instruction cache blocks accessed between two successive accesses to the same instruction block.
These two sets of results point to the need to optimize for both spatial and temporal localities of instruction blocks. Currently, both these forms of locality are fulfilled by the single i-cache. However, as has been well known [55], [63], a single cache (with LRU replacement) is not well suited to meet both these forms of locality simultaneously. This is also one of the reasons why streaming buffers [29], [39], [49], [68], separate caches for the two forms of locality [25], [56], [86], and/or cache bypassing schemes [37], have been proposed to handle the two localities differently.

It is very likely that a block has already been evicted from and misses in i-cache when it is re-accessed again after the longer reuse distance from its last burst. Our proposed spatio-temporal separation for i-cache aims to eliminate such misses if the block turns out to be useful enough to be retained in i-cache after its burst. While a prefetcher can also try to reduce such misses by predictions, we should note (and will show experimentally) that the two techniques - ACIC and prefetching - are complementary. In fact, as we will show, ACIC can reduce such misses even when a state-of-the-art prefetcher (e.g. [31], [76]) falls short. This goes to show that there is headroom for replacement policies beyond what prefetchers can provide to further improve i-cache performance.

**Need for further admission control:** To provide spatio-temporal separation, we add a 16-slot fully associative buffer, called i-Filter, residing next to i-cache, similar to that in [29], [49]. As Figure 2 shows, upon a fetch, the requested address is searched concurrently in both i-Filter and i-cache. If found in either, the instruction block is sent to CPU, and is considered a hit. Otherwise, the missed block is fetched from deeper in the memory hierarchy and is then placed in i-cache only. If i-Filter is full, the LRU block in i-Filter is evicted in order to make space. Victim blocks that are evicted from i-Filter are always inserted into i-cache for now. This i-Filter can fulfill much of the spatial locality. Only when evicted from this structure and inserted into i-cache, will it be subject more to the temporal access patterns for subsequent replacement.

We evaluate such a spatio-temporal separation using this i-Filter + i-cache design for 10 widely used datacenter applications listed in Table III. The experimental setup and simulation parameters are described in Section IV. Figure 3a shows the speedup comparison between this scheme and the OPT replacement policy (for i-cache). While the OPT replacement policy provides a 1.0398 speedup over the LRU baseline on average, the i-Filter+i-cache scheme provides a measely 1.0057 average speedup, i.e. the spatio-temporal separation with i-Filter is not very effective. The reason behind this gap is that some of the i-Filter victims can cause i-cache pollution, and thus should not be placed in i-cache.

This suggests that a simple separation of spatial (using i-Filter) and temporal (using i-cache) localities with different structures will not suffice. We additionally need an admission control mechanism to determine whether the block evicted from i-Filter should replace some other block in the corresponding set of i-cache, or whether it should be thrown away, motivating our ACIC admission-controlled i-cache. We can also use Figure 1a as an indicator of when such admission control would really matter for an application. In applications such as Web search, Neo4J-analytics, Data caching, and Media streaming, we see the intermediary range (512-1024, which is just beyond i-cache’s reach), more prominent than even larger reuse distances. These are the cases when comparing reuse distances become more important, as opposed to applications such as TPC-C and Wikipedia which have much larger reuse distances.
distances.

A. Two-level Predictor-based Admission Control

Figure 4 illustrates our predictor for making this decision. Similar to the two-level branch predictor [93], our two-level i-cache admission predictor is comprised of two major data structures: a comparison History Register Table (HRT) and a Pattern Table (PT). The tag of an i-Filter victim block is first hashed to index HRT. Each HRT entry is a history register that shifts left with bits which represent the last few comparison results of an i-Filter victim block and its i-cache contender block. If the former is re-accessed sooner in the future\(^2\) than the latter, the history register that the i-Filter victim block is mapped to is shifted left and a 1 is inserted into the least significant bit (LSB). Else, it is shifted left and a 0 is inserted into the LSB. PT is indexed by the content of history register. Each PT entry contains a saturating counter that is incremented each time that the i-Filter victim is re-accessed sooner than the i-cache contender block, and is decremented otherwise. A simple threshold is then used to determine whether the i-Filter victim is to be inserted (in place of the contender) in i-cache, or simply thrown away.

B. Comparing next accesses of i-Filter victim and i-cache contender

To update HRT entries and the counters in PT, we must find out whether an i-Filter victim block will be re-accessed in the nearer future (shorter reuse distance) than its i-cache contender block. Inspired by the design of MSHR (Missing Status Holding Registers) that tracks outstanding misses [51], we use a similar structure called CSHR (Comparison Status Holding Registers) to keep track of pairs of i-Filter victim blocks and their i-cache contenders whose comparison results are not yet resolved as shown in Figure 5. When an i-Filter victim block is being evicted, its tag and the tag of its i-cache contender are inserted into a CSHR entry. As a result of this, the LRU entry in CSHR may need to be evicted since it has a finite size (discussed in Section III-C1).

When the pipeline front-end issues fetch requests to i-cache in order, the tag of the instruction block being fetched is searched in CSHR. If it matches the i-Filter victim block tag field in a CSHR entry, it means that the i-Filter victim block in the entry is re-accessed sooner than its i-cache contender block. Therefore, the HRT entry is left shifted with a 1 and the corresponding counter of this pattern in PT is incremented. On the other hand, if the tag of the instruction block being fetched matches the i-cache contender block tag in a CSHR entry, the PT counter of the HRT entry is decremented with the HRT entry left shifted with a 0. In either case, as long as the comparison result of a CSHR entry is resolved, this CSHR entry is marked as invalid and can be reused.

C. Discussion about CSHR

1) Storage overhead: A large CSHR that contains many entries can track more outstanding i-Filter and i-cache block pairs, but it incurs higher storage overhead. On the other hand, with a small CSHR, entries are more likely to be evicted

\(^2\)Section III-B will discuss how to track future accesses.
Always inserting i-Filter victims to i-cache provides 1.0057 geometric speedup over baseline. Bypassing with access count comparison provides 1.0102 geometric speedup. OPT replacement policy provides 1.0398 geometric speedup.

(b) Reuse distance of incoming block (from i-Filter into i-cache) — reuse distance of outgoing block (selected from the corresponding set of i-cache using OPT) in Media Streaming. In 38.38% of the cases, the incoming block has a larger reuse distance, showing that the last access of the burst (spatial locality) should not be used for projecting future temporal reuse.

To further reduce storage overhead, instead of full tags of i-Filter victim blocks and i-cache contenders, partial tags are stored in each CSHR entry. When HRT is accessed for either prediction or predictor updates, partial tag, rather than the full block address, of the i-Filter victim block is hashed to index HRT. We will show later in Section IV-G that a 12-bit tag suffices for our needs. Consequently the CSHR totally takes $256 \times (2 \times 12\text{-bit tags} + 1\text{-bit valid} + 5\text{-bit LRU}) = 0.9375$ KB of space.

2) Access cycles: Since fetching an instruction block from i-cache can proceed in parallel with searching the partial tag of the instruction block in CSHR, accessing CSHR and updating predictor tables are not in the critical path to accessing i-cache. However, it is not practical to finish searching all the 256 entries in CSHR within one CPU cycle. To solve this problem, we adopt a set associative design for CSHR, in which the 256 entries are divided into $k$ sets. Since the i-Filter block address and the i-cache contender block address in a CSHR entry are always mapped to the same i-cache set, we use the $m$ most significant bits in the i-cache set index to find out to which CSHR set this pair should be inserted. When the instruction block being fetched needs to be searched in CSHR, the $m$ most significant bits in its i-cache set index are used to index the CSHR set and parallel search is done within that set. We find that a $k$ value of 8 and a $m$ value of 3 to index the 8 CSHR sets, works quite well for our needs. Each CSHR set adopts LRU as the replacement policy. Figure 7 shows how the instruction block being fetched is simultaneously searched in the set-associative CSHR and how the predictor tables are updated when CSHR entries are matched.

Fig. 3: Need for additional filtering of blocks from entering L1i after the current burst of accesses in i-Filter

Fig. 4: Two-level i-cache admission predictor

Fig. 5: Insert a new CSHR entry upon i-Filter victim prediction before comparisons are resolved, leading to less accurate predictions. To study the balance between these two factors, we plot Figure 6 which shows the incremental percentage of comparisons performed as we increase CSHR entries for a fully associative CSHR design. Although around 23% of comparisons require a very large number of CSHR entries, we find that nearly 70% of the comparisons get done with just 256 CSHR entries. Consequently we simply use a 256 entry CSHR, and for those entries which get evicted before being resolved, we give the benefit of doubt to the i-Filter victim as if it was re-accessed earlier than its i-cache contender.

Fig. 6: Distribution of comparisons during the lifetime of CSHR entries in Data Caching

Fig. 7: Search incoming block in set-associative CSHR

When an instruction block is being searched for in a CSHR
set, it can match the i-Filter block field of at most one CSHR entry. This is because when a block becomes i-Filter victim again and is inserted into the CSHR set, it must have already been re-accessed for it to have got back into the i-Filter after the previous eviction. This re-access guarantees that the block’s previous comparison has been resolved and the corresponding CSHR entry is no longer valid, if we assume updating the predictor tables can finish before the block becomes i-Filter victim again (which does occur in most cases, as described in the next paragraph). However, the instruction block being searched can match the i-cache contender block field of multiple CSHR entries, because the i-cache contender block can be compared with different i-Filter victims and wins the competition each time to stay in i-cache. Therefore, one instruction block being searched can lead to multiple HRT and PT update requests. To address this, HRT is first indexed in parallel, and then the current history values in HRT are used to index and update PT in the next cycle. After the history values are passed to the PT updater, the current history registers in HRT are updated accordingly. Aliasing can occur when updating HRT and PT, and can cause conflicts when we update multiple entries in parallel. However, we find that aliasing in indexing HRT is so rare that we simply update each HRT entry for only one request and ignore the others. Since PT is much smaller than HRT, the probability of aliasing in PT is a little higher. To mitigate this problem, we add a 10-slot queue for each PT entry to accommodate the update requests. In each cycle, the heads of the PT update queues are popped and are used to update the PT entries. Figure 8 summarizes the datapath to update the predictor tables after matched CSHR entries are found.

Fig. 8: Updating predictor tables

There is a concern that due to the 2 cycles (or more if waiting in the PT entry update queue) spent in updating the predictor tables, a block X may become i-Filter victim again while there is already one unresolved CSHR entry whose i-Filter victim block field is X. This implies that the stale (older) information for block X in the predictor tables is used to make prediction this time. We illustrate this problem in Figure 9.

In the case with a prefetcher, where block X is prefetched before it is re-accessed, the predictor could be updated after block X becomes i-Filter victim again. As shown in the timeline, the prefetch request reduces the cycles between re-accessing block X and loading it into i-Filter from L2 cache. For a superscalar processor, it could take as few as 3 cycles for block X to move from the MRU position to LRU position in i-Filter. Therefore, it is possible that the CSHR entry could not be resolved in time with a prefetcher.

Fig. 9: CSHR entry could not be resolved in time with a prefetcher

in i-Filter. Therefore, it is possible that the CSHR entry could not be resolved in time with the presence of a prefetcher if N > 3. However, as discussed in Section IV-G, such cases have a negligible impact on the overall performance.

D. Additional Storage and Energy requirements for ACIC

Storage: Each i-Filter entry contains 58 tag bits, 1 valid bit, 4 LRU bits, which adds up to 63 metadata bits, and a 64B instruction block. We empirally determine the size of HRT to be 1024 entries, each of which consists of 4 history bits, leading to $2^4$ entries in PT. Each PT entry contains a 5-bit counter that indicates the prediction result. Each of the 10 slots in PT entry update queue contains a 4-bit PT index and 1 bit indicating whether the counter in the PT entry should be incremented or decremented.

CSHR contains 256 entries, and each entry consists of 12 tag bits for the i-Filter victim block, 12 tag bits for the i-cache contender block, 1 valid bit, and 5 LRU bits for the 32-way CSHR design. Table I summarizes the storage overhead of ACIC for a 32KB i-cache with 8-way associativity. Evaluation results of ACIC in Section IV are based on the ACIC parameters in Table I, and we provide sensitivity analysis of ACIC in Section IV-G.

We also list the storage overhead of the prior schemes that we compared with in Table IV. ACIC requires 2.67KB extra storage, which is roughly 2/3rd of the 4.06KB storage overhead of GHRP, the state-of-the-art i-cache replacement policy with hardware techniques.

TABLE I: Storage overhead of ACIC for a 32KB, 8-way i-cache

| Component          | Number of bits                        |
|--------------------|---------------------------------------|
| i-Filter           | 16 entries $\times$ (63 bit metadata + 64B instruction block) $= 1.123KB$ |
| HRT                | 1024 entries $\times$ 4 bit history $= 0.5KB$ |
| PT                 | $2^N$ entries $\times$ 5 bit counters $= 10B$ |
| PT entry update queue | 16 PT update queues $\times$ 10 slots $\times$ (4 bit PT idx + 1 bit update request) $= 100B$ |
| CSHR               | 256 entries $\times$ (24 bit tags + 1 bit valid + 5 bit LRU) $= 0.937KB$ |
| Total              | 2.67KB                                |

Energy: We use the power pack (of the simulation infrastructure described in Section IV-A) to measure the chip energy for a 22nm process technology. It uses the McPAT [59] model, and we calculate power for the i-Filter, HRT, PT, and CSHR with CACTI 7 [7] and add the estimated values to the McPAT power numbers. It includes the chip energy with total execution time, runtime dynamic power, and total leakage power. We find that ACIC saves 0.63% chip energy on average, despite the
additional power taken by the new structures. While this is only the chip energy, the higher speedup and higher i-cache hit rates of ACIC, will further decrease the overall system energy if we consider off-chip DRAM, interconnects and peripherals.

IV. EVALUATION

A. Simulation infrastructure

TABLE II: Simulation parameters

| Parameter                  | Value                                      |
|----------------------------|--------------------------------------------|
| CPU frequency              | 4GHz                                       |
| Fetch width                | 6-wide, 24-entry Fetch Target Queue        |
| Decode width               | 6-wide, 60-entry Decode Queue              |
| Out-of-order Core          | 352-entry Reorder Buffer                   |
| BTB                        | 8192-entry, 4-way                          |
| Branch predictor           | TAGE [79]                                  |
| L1 I-Cache                 | 32KB, 8-way, 16 MSHRs, 4-cycle             |
| L1 D-Cache                 | 48KB, 8-way, 16 MSHRs, 5-cycle             |
| L2 Unified Cache           | 512KB, 8-way, 32 MSHRs, 5-cycle            |
| L3 Unified Cache           | 2MB, 16-way, 64 MSHRs, 35-cycle            |
| DRAM                       | 1 channel, 3200MT/s (25.6GB/s)             |

We first collect the full system execution trace of each application with the Qemu [10] emulator. Specifically, a trace of 500 million or 1 billion instructions (depending on the execution time of the application) in the steady state is recorded. The traces are then fed to the Tejas [77] simulator, a detailed cycle accurate trace-driven simulator. In each simulation, the simulator is warmed up with the first 10% (i.e. 50-100 million) of the instructions. Our core model is similar to the Intel Sunny Cove, as shown in Table II.

TABLE III: Data center applications used in our evaluation

| Benchmark Suite | Description                        | MPKI |
|-----------------|------------------------------------|------|
| Media Streaming | CloudSuite [20] Darwin streaming server | 81.2 |
| Data Caching    | CloudSuite [20] Memcached for Twitter | 78.1 |
| Data Serving    | CloudSuite [20] YCSB data store server | 31.6 |
| Web Serving     | CloudSuite [20] cloud web services  | 65.8 |
| Web Search      | CloudSuite [20] Apache Solr search engine | 151.5 |
| TPC-C           | OLTP-Bench [16] OLTP workload        | 42.5 |
| Wikipedia       | OLTP-Bench [16] online encyclopedia  | 41.1 |
| SIBench         | OLTP-Bench [16] snapshot isolations in DBMSs | 35.0 |
| Finagle-HTTP    | Renaissance [70] Twitter’s HTTP server | 46.1 |
| Neo4J-Analytics | Renaissance [70] graph queries for a database | 58.7 |

B. Prior Works for Comparison

ACIC has similar motivations (avoiding and dealing with i-cache pollution) targeted by the following three broad strategies: cache replacement policies, cache bypassing policies, and victim cache. Consequently, we compare ACIC quantitatively with prior and recent proposals that fall in these three categories as shown in Table IV. The Cache Type column identifies the cache targeted by the original proposal. For each of these prior proposals, we also list their important parameters used in the simulations, along with the additional storage that they require. As Table IV shows, for the simulated system, ACIC imposes an additional storage requirement of 2.67KB, which is around 2/3rd of the recent GHRP [64] proposal.

Additionally, a prefetcher, which reduces i-cache misses, can complement or belittle the benefits of these prior/our proposals. Consequently, we consider a standard fetch-directed prefetcher (FDP) [31].

C. Workloads and Metrics

Table III lists the datacenter applications used in our evaluations. These applications have been noted to suffer from front-end bottlenecks in related studies [4], [47], [52] due to their large footprints, involvement of libraries and OS, as well as varying dynamism in their execution paths. Column MPKI quantifies the i-cache MPKI (misses per 1000 instructions) in these applications on our FDP baseline platform.

The most important metric for an application is the execution time, and speedup of any proposed enhancement over the baseline is the first metric that we consider. Equally important is the reduction in i-cache misses (MPKI) attained with the enhancements, since those are the key targets of optimization in these schemes. Consequently, we study both these metrics in our evaluation below.

D. Comparison with replacement policies (SRRIP, SHiP, Hawkeye/Harmony, GHRP)

From Figure 10, we can see that the recently proposed GHRP provides the highest speedup amongst these previously proposed replacement policies. Still, ACIC outperforms GHRP with FDP. In particular, ACIC provides 1.0223 speedup on average over the LRU replacement policy FDP baseline, which corresponds to 56.03% of the attainable speedups of the oracle-based OPT replacement policy.

GHRP uses instruction reuse to predict dead blocks in the i-cache and prioritizes such dead blocks for replacement. If we define replacement accuracy as the percentage of victims selected by a given policy (e.g. GHRP) that are identical to the victims selected by OPT, we find that the replacement accuracy of GHRP is 17.90% on average, resulting in 15.64% of the MPKI reduction provided by OPT. ACIC is much more accurate, reducing 55.85% of misses reduced by OPT, as shown in Figure 11.

As can be seen from Figure 11, Media streaming, Data caching, Web search, and Neo4J-analytics are applications that show higher MPKI reduction under ACIC and GHRP than the other applications. The potential of a replacement policy is determined by the performance/MPKI difference between the OPT replacement policy and the baseline LRU policy. With the larger headroom, these four applications, ACIC and GHRP can help them to a greater extent. These are also those applications which suffer more from the burstiness behavior identified earlier (Figure 1a), for which LRU cannot predict and optimize for the larger reuse distance after a recent burst. The relative benefits across applications with ACIC is further explained in Section IV-G.
TABLE IV: Schemes for comparison

| Optimization Strategy | Cache Type         | Important Parameters/Notes                           | Storage Overhead |
|-----------------------|--------------------|------------------------------------------------------|-----------------|
| SRRIP [34]            | replacement policy | LLC                                                 | 0.125KB         |
| SHIP [90]             | replacement policy | LLC                                                 | 2.88KB          |
| Hawkeye [32]/Harmony [33] | replacement policy | LLC                                                 | 4.69KB          |
| GHRP [68]             | replacement policy | L1 i-cache                                          | 4.06KB          |
| DSB [23]              | bypassing policy   | LLC                                                 | 0.48KB          |
| OBM [58]              | bypassing policy   | LLC                                                 | 1.41KB          |
| VVC [44]              | victim cache       | LLC                                                 | 9.06KB          |
| VC3K [39]             | victim cache       | L1 cache                                            | 8KB             |
| 40KB i-cache          | larger i-cache     | L1 i-cache                                          | 8KB             |
| OPT [9]               | replacement policy | all types                                           |                 |
| OPT bypass with i-Filter | bypassing policy | L1 i-cache                                          | 1.123KB         |
| ACIC                  | bypassing policy   | L1 i-cache                                          | 2.67KB          |

E. Comparison with bypassing policies (DSB and OBM)

Of these two prior bypassing policies, DSB performs slightly better, though providing only a limited 1.0006 speedup over the LRU baseline with FDP.

DSB bypasses newly allocated blocks from the cache with a probability tuned based on the effectiveness of past bypassing decisions. Though similar in goals, unlike ACIC, DSB does not provide spatio-temporal locality separation whose importance was pointed out in Section II. Even with a higher storage budget, DSB does not perform as well as ACIC due to this fundamental problem. DSB provides only 0.46% MPKI reduction over the LRU baseline on average. Moreover, the bypassing policy of DSB is not very effective, and when equipped with i-Filter, DSB still only provides 1.0010 speedup over baseline.

Interestingly, we see that the results for OPT bypassing and OPT replacement are similar/close, implying that combining the spatio-temporal separation provided by i-Filter and a good admission control mechanism, can be an effective way to improve i-cache performance.

F. Comparison with victim caches (VC3K, VVC) and larger i-cache

One could question whether the real-estate required for the filtering mechanism could have been better served with an appropriate victim cache (which temporarily retains evictions for another chance), or even a larger i-cache. Consequently, we compare ACIC with (i) a traditional 3KB fully-associative victim cache VC3K [39], (ii) a recent work on victim cache [44], VVC which better uses the existing space, and (iii) a larger 36KB, 9-way i-cache (i.e. adding 4KB over our baseline, which is more than the additional real-estate needed for ACIC and also has a higher associativity).

VVC turns out to actually slow down the execution as seen in Figure 10. VVC uses slots in the existing i-cache that are not both very large (if they are, they will both likely reuse distances than the predicted dead blocks in other sets, but they are still brought into other sets by VVC, leading to waste of cache capacity. While a traditional victim cache (VC3K) does much better than VVC, ACIC gives 1.018× the speedup provided by the 3KB victim cache on average.

Figure 10 shows that ACIC provides 1.09× the speedup provided by the 36KB i-cache on average. These results tend to reiterate the importance of being more discretionary in what comes into and goes out of i-cache, than blindly throwing more resources at it.

G. Insights into the working of ACIC

Discretionary Filtering: Figure 13 depicts the percentage of i-Filter victims that are inserted into i-cache based on the predictor in ACIC. The percentages vary significantly across applications (from 30-99%). As Figure 1a showed, Web search, Neo4J-analysts, Data caching, and Media streaming show a higher fraction of reuse distances which fall just beyond the i-cache’s reach, where it becomes more critical to decide whether or not to insert the victim from i-Filter into i-cache. This is confirmed by Figure 13, where we see these applications exhibiting a larger filtering effect. This reiterates the need for dynamic adaptation to application behavior as in ACIC, rather than a static way of determining whether to insert into i-cache after the current burst.

Accuracy of Filtering: It is even more important to examine whether ACIC made the correct filtering choice. To do this, we use oracle knowledge about reuse distances to compare the future reuse distances of the i-cache victim and the i-Filter victim, and compare that decision with ACIC’s prediction. The filter accuracy of ACIC is calculated as the percentage of the correct predictions over total predictions. Surprisingly, the average bypass accuracy of ACIC is only 60.89%, as shown in the first bar (corresponding to [0,InF]) of Figure 12a. However, the bypass accuracy matters only in cases when the reuse distances of the i-Filter victim and the i-cache contender block are not both very large (if they are, they will both likely
Fig. 10: ACIC’s speedup compared with state-of-the-art replacement, bypassing, and victim cache policies over an LRU baseline with fetch-directed prefetching.

Fig. 11: ACIC’s MPKI reduction compared with state-of-the-art replacement, bypassing, and victim cache policies over an LRU baseline with fetch-directed prefetching.

Fig. 12: ACIC bypass accuracy analysis

(a) Average ACIC bypass accuracy for various reuse distance ranges

(b) MPKI reduction comparison of random bypass with 60% accuracy and ACIC over fetch-directed prefetching baseline

Fig. 13: Percentage of i-Filter victims inserted into i-cache

get evicted before being accessed), and their reuse distances are not equal either. We consequently plot the ACIC bypass accuracy for varying ranges of reuse distances in Figure 12a.

To demonstrate that ACIC is reasonably accurate where it really matters, we also consider a “random” filtering mechanism to determine whether to insert the evicted i-Filter block into i-cache. In Figure 12b, we compare the i-cache MPKI reduction of ACIC and this random bypass scheme over the FDP baseline. Even though the random bypass scheme has 60% accuracy, similar to the overall bypass accuracy of ACIC, we can see that it provides only 7.65% MPKI reduction,
which is 42.17% of the MPKI reduction provided by ACIC. Figure 12a and Figure 12b provide a key insight: prediction accuracy matters only when at least either of the two (i-Filter victim or i-cache contender) has a reuse distance that is not very large, so that at least one of them is likely to be accessed again while in i-cache in the near future. Latency in updating predictor: Section III-C2 described the possibility that stale information is read from predictor due to the multiple cycles spent in updating the two tables, HRT and PT, with the existence of a prefetcher. To see whether this could cause a problem in performance, we compare the i-cache MPKI reduction with our parallel update scheme, in which at least 2 cycles are spent in updating HRT and PT, and an instant update scheme, in which the HRT and PT are updated immediately. From Figure 14, we can see that the MPKI reduction of the parallel update scheme is very close to that of the instant update scheme. The update latency of the predictor tables thus does not affect ACIC’s effectiveness, and does not need to come into the critical path. Sensitivity Analysis: Figure 15 shows the average speedup of ACIC with different configurations. Fig. 15: Sensitivity of ACIC to different configurations of ACIC when its key design parameters are varied. The leftmost bar default gives the average speedup of ACIC with parameters shown in Table I. Since the number of CSHR entries has been discussed in Section III-C1, here we only show sensitivity to HRT entries, length of each history register in HRT, length of counters in PT, number of i-Filter slots, and length of partial tags in CSHR. We can see that among all the parameters, increasing the i-Filter size gives the most benefit, while decreasing i-Filter size, length of PT counter and CSHR tags worsen performance the most. Increasing the history length from 4-bit to 10-bit does not show a big performance gain.

H. Discussion

1) Performance benefit due to bypass policy: While similar/variant forms of i-Filter are not necessarily modeled in current academic simulators, i-Filter-like small buffers are usually present in real processors to contain recently accessed instruction blocks. To show the benefit of ACIC more realistically, we present Figure 16 to show the speedup of ACIC over FDP baseline equipped with i-Filter. We can see that ACIC’s bypass policy itself gives 1.0165 geomean speedup over the LRU replacement policy baseline.

2) Necessity of each ACIC structure: While ACIC gives better performance and less storage overhead than the recently proposed GHRP, ACIC’s mechanism is more complex. CSHR is responsible for training the predictor, so it cannot exist on its own. To justify the necessity of the other two parts of ACIC (i-Filter and two-level predictor), we plot Figure 17 to show the geomean speedup of ACIC with simpler designs over FDP baseline: ACIC without i-Filter, ACIC with i-Filter only, ACIC with a global history two-level predictor, and ACIC with a bimodal predictor. We can see that turning off i-Filter/predictor or replacing two-level predictor with simpler ones does not give as good performance as our default ACIC.

3) Evaluation of ACIC with SPEC workloads: ACIC targets datacenter workloads, as these workloads suffer from higher i-cache misses than conventional workloads like SPEC [1]. For completeness, we evaluate how ACIC performs in SPEC workloads as well. We refer readers to Section IV-H3 in [87] for details.
4) With Entangling Prefetching baseline: Entangling prefetcher [76] is a more recent state-of-the-art instruction prefetcher than FDP. From Figure 18 and Figure 19, we can see that with the entangling prefetcher (with a 4K-entry entangled table) baseline, ACIC still outperforms GHRP and 36KB L1i, which are the two best prior policies shown in Figure 10 and Figure 11. ACIC provides 1.0102 geomean speedup and 6.71% MPKI reduction over the baseline. Entangling prefetcher improves the baseline L1i hit rate to be over 97% in our datacenter workloads, so it further complements ACIC’s benefits. However, considering that the entangling prefetcher incurs about 40KB storage overhead, which is larger than i-cache itself, ACIC is not redundant. As stated in Section II, ACIC and prefetching are complementary, and ACIC can improve i-cache performance beyond the benefits of prefetchers.

V. RELATED WORK

The cache pollution problem that ACIC addresses is most closely related to 3 broad categories - replacement policies, bypassing mechanisms and victim caches - that have similar goals, though most of the prior work in these have targeted d-caches as opposed to i-caches.

Replacement policies: There has been considerable work on replacement policies [11], [27], [34], [35], [45], [48], [55], [61], [66], [72], [75], [78], [81], [88], [89]. Since OPT is not implementable, heuristics include variations of LRU [35], [54], [66], [81], [89], frequency [55], [75], reuse prediction [17], [19], [34], [45], [48], [61], [64], [90], and others [11], [71], [73], [78], [83]. There have also been learning-based policies based on machine learning [36], [80], [85] and Belady’s optimal solution [32], [33], [60].

However, as our quantitative evaluation shows, many of these prior proposals for d-caches (e.g. [32]–[34], [90]) do not work as well for i-caches, compared to ACIC. On the other hand, recent techniques for i-caches such as Ripple [47] and GHRP [64] do not identify and leverage the burstiness of accesses to instruction blocks, making ACIC a better alternative as our evaluations have shown.

Bypassing policies: Cache bypassing policies use static approaches [14], [91] with a profile-guided compiler to identify lines for bypassing, and dynamic approaches [12], [17], [18], [23], [24], [26], [36]–[38], [48], [84], [92] which use run-time behavior to learn and predict bypassing opportunities.

DSB [23] and OBM [58] are two bypassing policies most similar to ACIC in that they also track the reuse behavior of newly allocated cache lines and their corresponding cache contender blocks to learn whether an incoming block should bypass the cache. DSB randomly bypasses newly allocated lines and the effectiveness of the past bypassing decisions is used to tune the bypassing probability. However, unlike the CSHR in ACIC, DSB only tracks one pair in a cache set at a time, and OBM tracks incoming-victim pairs with a low probability to reduce storage overhead. The selective tracking used by DSB and OBM turns out to be much less effective than our CSHR design. Moreover, DSB and OBM are further undermined since they are direct bypassing schemes without first separating spatial and temporal locality.

An early work [37] uses a small buffer, similar to ACIC, for short temporal/spatial locality. However, they use access counters to compare the utility of incoming and contender blocks, which does not work very well for the instruction stream that exhibits burstiness requiring a more extensive predictor as in ACIC.

Victim caches: Rather than regulate entry, an alternative is to retain the evicted victims temporarily in a victim cache to reduce pollution. Works on victim caches [39] include [8], [15], [30]. VVC [44] is a more recent work that predicts dead blocks and reuse the dead regions in the cache as a virtual victim cache. We have shown that ACIC can provide better performance for the instruction stream.

VI. CONCLUDING REMARKS & FUTURE WORK

We drew insight from the observation of bursty accesses in data stream [61], leveraged i-Filter proposed in [29], [49] to optimize “burstiness” in the instruction stream, and presented an admission control mechanism, ACIC, that regulates the entry of instruction blocks into the i-cache. Comparing with several (8 in all) prior approaches - replacement algorithms, bypassing mechanisms and victim caches - we have shown the benefits of ACIC over these prior approaches. We have also shown that it can complement previously proposed prefetching mechanisms.

The predictor in ACIC learns from on-demand instruction accesses, and tries to estimate reuse distances to implement a more practical version of Belady’s OPT algorithm (comparing reuse distances of i-Filter and i-cache victim). Prefetching could further reduce on-demand misses, but comes at a possible cost of higher memory traffic. As was pointed out in [33], Belady’s OPT may not be the best when prefetching is considered. Developing a prefetching-aware ACIC mechanism is part of our future work.

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