Hall and field-effect mobilities in few layered \( p \)-WSe\(_2\) field-effect transistors

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Here, we present a temperature (\( T \)) dependent comparison between field-effect and Hall mobilities in field-effect transistors based on few-layered WSe\(_2\) exfoliated onto SiO\(_2\). Without dielectric engineering and beyond a \( T \)-dependent threshold gate-voltage, we observe maximum hole mobilities approaching 350 cm\(^2\)/Vs at \( T = 300 \) K. The hole Hall mobility reaches a maximum value of 650 cm\(^2\)/Vs as \( T \) is lowered below ~150 K, indicating that insofar WSe\(_2\)-based field-effect transistors (FETs) display the largest Hall mobilities among the transition metal dichalcogenides. The gate capacitance, as extracted from the Hall-effect, reveals the presence of spurious charges in the channel, while the two-terminal sheet resistivity displays two-dimensional variable-range hopping behavior, indicating carrier localization induced by disorder at the interface between WSe\(_2\) and SiO\(_2\). We argue that improvements in the fabrication protocols as, for example, the use of a substrate free of dangling bonds are likely to produce WSe\(_2\)-based FETs displaying higher room temperature mobilities, i.e. approaching those of \( p \)-doped Si, which would make it a suitable candidate for high performance opto-electronics.

Field-effect transistors (FETs) based on exfoliated transition-metal dichalcogenides (TMDs)\(^1\)\(^–\)\(^4\) were shown to be promising as low-power switching devices and therefore as potential components for high-resolution liquid crystal and organic light-emitting diode displays, particularly in their multi-layered form\(^5\). Bulk transition metal dichalcogenides (TMD) crystallize in the “2H” or trigonal prismatic structure (space group \( P6_3/mmc \)), in which each transition metal is surrounded by six chalcogenide atoms defining two triangular prisms. Extended planes, which are weakly or van der Waals coupled, result from the tessellation of this basic unit. Contiguous planes are shifted with respect to one another (along both the \( a \)- and the \( b \)-axis), therefore the unit cell is composed of two planes with a transition metal dependent inter-layer distance \( c \). The covalently bonded layers are expected to display high crystallinity, although as in graphite/graphene, one can expect crystallographic mosaicity between planes stacked along the \( c \)-axis. Similarly to graphite, compounds such as MoS\(_2\), WS\(_2\), etc., are exfoliable layered materials characterized by a weak inter-planar van der Waals coupling\(^1\). In contrast to graphene, they exhibit indirect band gaps ranging from ~1 to ~2 eV which become direct in single atomic-layers, making them promising candidates for applications.

Early studies on field-effect transistors (FETs) based on bulk WSe\(_2\) single-crystals using parylene as the gate dielectric, revealed room temperature field-effect mobilities approaching those of \( p \)-Si\(^6\) but with a small current ON/OFF ratio. Subsequent investigations\(^7\) on mechanically exfoliated MoS\(_2\) flakes composed of tenths of atomic layers and SiO\(_2\) as the gate dielectrics, revealed considerably lower mobilities (10–50 cm\(^2\)/Vs), suggesting either a remarkable difference in mobilities between MoS\(_2\) and WSe\(_2\) or that an inadequate choice of gate dielectrics can hinder their performance. More recently\(^8\), it was suggested that field-effect carrier mobilities surpassing 1000 cm\(^2\)/Vs could be achieved in dual gated, single-layer MoS\(_2\) FETs through the use of a top gate composed of a high-\( k \) dielectric such as HfO\(_2\). Nevertheless, it was argued that this is an overestimated mobility value due to the capacitive coupling between both top and back gates\(^9\), a fact that is supported by subsequent reports of much smaller mobilities in similar devices when the gate capacitance is extracted from a Hall-effect study\(^10\). It was also recently argued that remote phonons from dielectric layers such as HfO\(_2\) can limit carrier mobility and would require the use of an interfacial layer to absorb most of the vibrational energy\(^11\). Nevertheless, these observations already led to the development of integrated circuits based on single-layered and on bi-layered MoS\(_2\). Recent studies in both single- and double-layered MoS\(_2\) revealed Hall mobilities which increase strongly with gate voltage, saturating at maximum values between ~200 and ~375 cm\(^2\)/Vs at low temperatures\(^12\). In multi-layered MoS\(_2\)
the Hall mobility has been found to increase from $\sim 175$ cm$^2$/Vs at 60 K to 311 cm$^2$/Vs at $T = 1$ K at back-gate voltages as large as 100 V.s. However, marked discrepancies were reported between the measured field-effect and the Hall mobilities, which at the light of Refs. 11–13 could be attributed to underestimated values for the gate capacitances.

Similarly to past research on graphene, much of the current effort on TMD-based FETs is focused on understanding the role played by the substrates, annealing conditions and the work functions of the metallic contacts. For example, it was recently argued that most of the above quoted mobilities are determined by the Schottky barriers at the level of the current contacts which limits the current-density that can be extracted from these transistors. The authors of Ref. 19 argue that small Schottky barriers, and therefore nearly Ohmic contacts in TMD based FETs, can only be achieved through the use of metals with small work functions such as Sc. Furthermore, due to the detrimental role played by the SiO$_2$ substrates, Ref. 19 finds that the highest mobilities ($\sim 175$ cm$^2$/Vs) can be achieved in FETs built on $\sim 10$ nm ($\sim 15$ layers) thick flakes. Thickness dependent mobilities were also recently reported for MoS$_2$ based transistors using poly(methyl methacrylate) (PMMA) as the gate dielectrics. High performance TMD-based FETs have been claimed to have the potential to make a major impact in low power optoelectronic applications.

Results and Discussion

Figures 1a and b show respectively, a micrograph of a typical device, whose experimental results will be discussed throughout this manuscript, and the sketch of a four-terminal configuration for conductance measurements. Current source $I$ and drain $I^*$ terminals, as well as the pairs of voltage contacts 1, 2 and 3, 4 are indicated. As shown below, this configuration of contacts allows us to compare electrical transport measurements performed when using a 2-contact configuration (e.g. $\mu_{FE}$) with a 4-terminal one (e.g. $R_{xy}$ or the Hall-effect). Figure 1b shows an atomic force microscopy profile and image (inset) from which we extract a flake thickness of 8 nm, or approximately 12 atomic layers. We chose to focus on multilayered FETs because our preliminary observations agree with those of Refs. 19, 20, indicating that the highest mobilities are observed in flakes with thicknesses between $\sim 10$ and 15 atomic layers as shown in Fig. 1d. In addition, as argued in Ref. 5 multilayered flakes should lead to thin film transistors yielding higher drive currents when compared to transistors based on single atomic layers, possibly making multilayered FETs more suitable for high-resolution liquid crystal and organic light-emitting diode displays. Our flakes were mechanically exfoliated and transferred onto a 270 nm thick SiO$_2$ layer grown on p-doped Si, which is used as a back gate. Throughout this study, we focus on devices with thicknesses ranging from 9 to 15 layers. Three of the devices were annealed at 150 °C, under high vacuum for 24 h, which as reported in Ref. 17, yields higher mobilities particularly at low temperatures. We found very similar overall
response among the non-annealed samples, as well as among the annealed ones.

Figure 2a shows the extracted field-effect current $I_{ds}$ as a function of the back gate voltage $V_{bg}$ for several fixed values of the voltage $V_{ds}$ across the current contacts, i.e. when using a 2-terminal configuration. From initial studies, but in contrast with Refs. 25, 26, WSe$_2$ is expected to show ambipolar behavior, i.e. a sizable current resulting from the accumulation of either electrons or holes at the WSe$_2$/SiO$_2$ interface due to the electric field-effect. Although we have previously observed such a behavior, all FETs studied here show a rather modest electron current (i.e. saturating at $SS \sim 250$ mV) for several values of $V_{ds}$. Notice, how all the curves collapse on a single curve, indicating linear dependence on $V_{ds}$. As argued below, this linear dependence most likely results from thermionic emission across the Schottky barrier at the level of the contacts. (c) Field effect mobility $\mu_{FE} = (1/c_e \Delta I/dV_{bg})$ as a function of $V_{bg}$, where $c_e = e_{bg}/d = 12.789 \times 10^{-7}$ F/cm$^2$ (for a $d = 270$ nm thick SiO$_2$ layer). (d) $I_{on}$ as a function of $V_{bg}$, when using an excitation voltage $V_{ds} = 5$ mV. Red line is a linear fit whose slope yields a field-effect mobility $\mu_{FE} = 300$ cm$^2$/Vs.

Figure 2 | (a) Current $I_{on}$ in a logarithmic scale as extracted from a WSe$_2$ FET at $T = 300$ K and as a function of the gate voltage $V_{bg}$ for several values of the voltage $V_{ds}$, i.e. respectively 5 (dark blue line), 26 (red), 47 (blue), 68 (magenta), and 90 mV (brown), between drain and source contacts. Notice that the ON/OFF ratio approaches $10^6$ and subthreshold swing $SS \sim 250$ mV per decade. We evaluated the resistance $R_s$ of the contacts by performing also 4 terminal measurements (see Fig. 7 a below) through $R_s = V_{ds}/I_{ds} - \rho_{xx}/w$, where $\rho_{xx}$ is the sheet resistivity of the channel measured in a four-terminal configuration. We found the ratio $R_s/\rho_{xx} \approx 20$ to remain nearly constant as a function of $V_{bg}$. (b) Conductivity $\sigma = S I_{ds}$, where the conductance $S = I_{ds}/V_{ds}$ (from (a)), as a function of $V_{bg}$ and for several values of $V_{ds}$. Notice, how all the curves collapse on a single curve, indicating linear dependence on $V_{ds}$. As argued below, this linear dependence most likely results from thermionic emission across the Schottky-barrier at the level of the contacts. (c) Field effect mobility $\mu_{FE} = (1/c_e \Delta I/dV_{bg})$ as a function of $V_{bg}$, where $c_e = e_{bg}/d = 12.789 \times 10^{-7}$ F/cm$^2$ (for a $d = 270$ nm thick SiO$_2$ layer). (d) $I_{on}$ as a function of $V_{bg}$, when using an excitation voltage $V_{ds} = 5$ mV. Red line is a linear fit whose slope yields a field-effect mobility $\mu_{FE} = 300$ cm$^2$/Vs.

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acetic Schottky energy barrier $\phi$, as seen for instance in Ref. 28. But according to Figs. 2b and 3b, $\phi$ is basically independent on $V_{bg}$ above a threshold gate voltage, even at lower temperatures.

Figure 4a shows $I_d$ as a function of $V_{bg}$ for several temperatures and for the crystal shown in Fig. 1a. Fig. 4b shows the resulting field-effect mobility $\mu_{FE}$ as a function of $T$ as extracted from the slopes of $I_d(V_{bg}, T)$. $\mu_{FE}$ is observed to increase, reaching a maximum of $\sim 650$ cm$^2$/Vs at $T \sim 100$ K, decreasing subsequently to values around $250$ cm$^2$/Vs at low temperatures. Orange markers depict $\mu_{FE}$ for a second, annealed sample whose Hall mobility is discussed below. This decrease is attributable to extrinsic factors, such as chemical residues from the lithographic process, since annealing the samples under high vacuum for at least 24 h considerably increases the mobility at low $T$s. As will be illustrated by the results shown below for a second sample annealed in this way. Figure 4c shows $\mu_{FE}$ as a function of $V_{bg}$ for several temperatures (as extracted from the curves in a). All curves show a maximum at a $V_{bg}$-dependent value. As seen, the main effect of lowering $T$ is to increase the threshold back-gate voltage $V^*_{bg}$ for carrier conduction. In WS$_2$, by using ambipolar ionic liquid gating, which heavily screens charged defects, the authors of Ref. 29 were able to estimate the size of its semiconducting gap, given roughly by the difference between the threshold voltages required for hole and electron conduction respectively, or $\sim 1.4$ V. The much larger $V^*_{bg}$ values observed by us in WSe$_2$ is attributable to intrinsic and extrinsic effects, such as vacancies and charge traps, which limit the carrier mobility becoming particularly relevant at low temperatures, see discussion below. At first glance, at low gate voltages, $\rho$ would seem to follow the activated behavior with a small activation gap. On the other hand at high temperatures and high gate voltages, $\rho$ displays metallic-like behavior, usually defined by $\rho(T) > 0$. Magenta line is a fit to a simple linear-dependence on temperature, suggesting either an unconventional metallic state or most likely, phonon scattering.

As observed in Figs. 4a and c, the threshold gate-voltage $V^*_{bg}$ required to observe a finite $\sigma$ increases from $\sim 5$ to $\sim 35$ V as $T$ is lowered from 300 to 5 K. In order to clarify the dependence of $V^*_{bg}$ on $T$, we assume that $V^*_{bg}$ is dominated by disorder at the interface between WSe$_2$ and SiO$_2$ which leads to charge localization. To illustrate this point, in Fig. 5 we plot $\sigma(T)$ as a function of $T^{-1/3}$ since from past experience on Si/SiO$_2$ MOSFETs, it is well known that spurious charges intrinsic to the SiO$_2$ layer$^{30-32}$, in addition to the roughness at the interface between the Si and the glassy SiO$_2$,$^{33}$ produces charge localization leading to variable-range hopping conductivity: $\sigma(T) = \sigma_0 \exp(-T_0/T)^{1/3}$ where $d$ is the dimensionality of the system, or $d = 2$ in our case$^{34}$. As seen in Fig. 5, one observes a crossover from metallic-like to a clear two-dimensional variable-range hopping (2DVRH) conductivity below a gate voltage dependent temperature; red lines are linear fits. At lower gate voltages, the 2DVRH regime is observed over the entire range of temperatures. Therefore, despite the linear transport regime and the relatively large mobilities observed in Figs. 1 through 4, this plot indicates very clearly, that below $V^*_{bg}$ the carriers in the channel are localized due to disorder. Notice that similar conclusions were also reported from measurements on MoS$_2$.$^{35}$ Although, at the moment we do not have a clear experimental understanding on the type and on the concomitant role of disorder in these systems (which would allow a deeper theoretical understanding on the origin of the localization), the above experimental plot is unambiguous in revealing the predominant conduction mechanism for gate-voltages below a threshold value.

Now, we are in position of qualitatively explaining the $T$-dependence of $V^*_{bg}$: thermal activated processes promote carriers across a mobility edge which defines the boundary between extended electronic states and a tail in the density of states composed of localized electronic states. At higher temperatures, more carriers are thermally excited across the mobility edge, or equivalently, can be excited across
Figure 4 | (a) $I_{ds}$ as a function of the gate voltage $V_{bg}$ for several temperatures $T$ and for an excitation voltage $V_{ds} = 5$ mV. From the slopes of the linear fit (red line) one extracts the respective values of the field-effect mobility $\mu_{FE}$ as a function of the temperature, shown in (b). Orange markers depicts $\mu_{FE}$ for a second, annealed sample. The field-effect mobility is seen to increase continuously as the temperature is lowered down to $T = 105$ K, beyond which it decreases sharply. (c) $\mu_{FE} = (1/\rho_{em}) \partial \rho_{em}/\partial V_{bg}$ as extracted from the curves in (a). Notice that $\mu_{FE}$ still saturates at a value of $\approx 300$ cm$^2$/Vs at $T = 5$ K. d Resistivity $\rho = 1/\sigma$ as a function of $T$ for 3 values of the gate voltage, i.e. $-20$, $-30$ and $-40$ V, respectively (as extracted from the data in (a) or (c)). Magenta line corresponds to a linear fit, describing the behavior of the metallic emission theory, defined by $\rho(T) > 0$, observed at higher temperatures when $V_{bg} = -40$ V.

the potential well(s) produced by disorder or charge traps, therefore one needs lower gate voltage(s) to untrap the carriers. Once these carriers have moved across the mobility edge, they become mobile and, as our results show, respond linearly as a function of the excitation voltage $V_{bg}$. Finally, as $V_{bg}$ increases with decreasing $T$ the number of carriers is expected to decrease continuously since they become progressively localized due to the suppression of thermally activated processes which can no longer contribute to carrier detrapping. This is clearly illustrated by Fig. 4b, where one sees an increase in mobility, due to the suppression of phonon scattering leading to a maximum in the mobility and to its subsequent suppression upon additional cooling. Therefore, at higher temperatures and for gate voltages above the threshold, where one observes a metallic-like state, one has two competing mechanisms at play upon cooling, i.e., the tendency to localization/suppression of carriers which is unfavorable to metallicity, and the suppression of phonon scattering. Suppression of phonon scattering is the only possible explanation for the observed metallic behavior. Hence, one must conclude that this metallic behavior ought to be intrinsic to the compound, but disorder-induced carrier localization dominates $\sigma$ at lower temperatures.

Although, as Figs. and 3 indicate, the conductivity $\sigma$ as measured through a two-terminal configuration, is linear on excitation voltage $V_{ds}$, when $V_{bg} > V_{bg}^{*}$ it was discussed at length that the electrical conduction through the drain and source contacts can by no means be ohmic. If, in effect, a Schottky barrier of $\sim 770$ meV is expected as the difference in energy between the work function of Ti, or 4.33 eV, and the ionization energy of WSe$\text{$_2$}$, or $\sim 5.1$ eV. The linear, or apparent ohmic regime presumably would result from thermionic emission or thermionic field emission processes. According to thermionic emission theory, the drain-source current $I_{ds}$ is related to the Schottky barrier height $\phi_{SB}$ through the expression:

$$I_{ds} = A A^* T^2 \exp \left( \frac{e \phi_{SB}}{k_B T} \right)$$

(1)

Where $A$ is the area of the Schottky junction, $A^*$ is $4\pi e m^* k_B^2 h^{-1}$ is the effective Richardson constant, $e$ is the elementary charge, $k_B$ is the Boltzmann constant, $m^*$ is the effective mass and $h$ is the Planck constant$^{19}$. In order to evaluate the Schottky barrier at the level of the contacts, in the top panel of Fig. 6 we plot $I_{ds}$ normalized by the square of the temperature $T^2$ as a function of $e k_B T$ and for several values of the gate voltage. Red lines are linear fits from which we extract the $\phi_{SB}(V_{bg})$. Notice that in the top panel of Fig. 6 the linear fits are limited to higher temperatures since at lower temperatures one observes pronounced, gate dependent, deviations from the thermionic emission theory. The bottom panel of Fig. 6 shows $\phi_{SB}(V_{bg})$ in a logarithmic scale as a function of $V_{bg}$. Red line is a linear fit from whose deviation we extract the size of the Schottky barrier$^{19}$, or $\Phi \sim 16$ meV, indicating a much better band alignment than originally expected. It is perhaps possible that the Eq. (1) might take a different form for layered two-dimensional materials, for example, in such compounds one might need a temperature pre-factor distinct from $T$. We attempted the use of different temperature pre-factors such as $T$ or $T^2$, but it does not improve the linearity of $\log(I_{ds}/T^2)$ over the entire range of temperatures when $V_{bg} = -20$ V, while in Fig. 6, thermionic emission can describe the behavior of $I_{ds}/T^2$ as a function of $T$ only when $T > 125$ K. Therefore the values of $\phi_{SB}(V_{bg})$ extracted here should be taken with caution.

In Figure 7, we compare the above field-effect mobilities with Hall mobility measurements on a second, vacuum annealed flake of similar thickness. Figure 7a shows the four-terminal sheet resistivity, i.e. $\rho_{xx} = \rho V_{ds}/I_{ds}$ as a function of $V_{bg}$. $\rho_{xx}$ was measured with a lock-in technique, for gate voltages where the voltages $V_{12}$ or $V_{34}$ were in phase with the excitation signal. We also checked that any pair of
voltage contacts produced nearly the same value for $\rho_{\text{ac}}$, indicating a nearly uniform current throughout the channel. $\rho_{\text{ac}}$ increases very rapidly, beyond $10^8 \Omega$ as $V_{bg} \to 0$ V. Also the out-of-phase component of the measured AC signal becomes very large as $V_{bg} \to 0$ limiting the $V_{bg}$ range for our measurements. Figure 7b displays the measured Hall signal $R_{xx}$ as a function of the magnetic field $H$ at $T = 50$ K and for several values of $V_{bg}$. Red lines are linear fits from which we extract the Hall constant $R_{xx}$ at different gate voltages. Notice that for $T = 50$ K and $V_{bg} = 70$ V one obtains, in this annealed sample, a $\mu_H$ value of $\sim 676$ cm$^2$/V s. Figure 7c shows the density of carriers $n_{\text{H}} = 1/eR_{xx}$ as a function of $V_{bg}$ for several $T$s. Red lines are linear fits from which we extract the slope $n_{\text{H}}/V_{bg} = e\sigma^*/c_e$, where $c_e$ is an effective back-gate capacitance: in the absence of extrinsic charged defects at the WSe$_2$/SiO$_2$ interface, $c_e$ should be equal to the previously quoted gate capacitance $c_{\text{fe}}$. Solid evidence for the existence of ionized impurities acting as hole traps at the interface is provided by the linear fits in Fig. 7c which intercepts the $n_{\text{H}} = 0$ axis at finite threshold gate voltages $V_{bg}$. This confirms that practically all holes generated by applying a gate voltage smaller than $V_{bg}$ remain localized at the interface. Figure 7d shows a comparison between $\mu_{\text{FE}}$ (magenta and blue lines) and $\mu_{\text{H}}$ (red markers) as extracted from the same device at room temperature. The blue line was measured after thermally cycling the FET device to low temperatures. Notice how $V_{bg}$ increases after thermally cycling the sample, thus suggesting that strain at the interface, resulting from the difference between the thermal expansion coefficients of SiO$_2$ and WSe$_2$, also contributes to $V_{bg}$. Therefore, strain would seem to be an additional factor contributing to the mobility edge. Notice also that both mobilities initially increase as a function $|V_{bg}|$, reaching a maximum at the same $V_{bg}$ value, decreasing subsequently as the back-gate voltage is further increased. Figure 7e shows $\mu_{\text{H}}$ as a function of $T$ for several values of $V_{bg}$. Notice how $\mu_{\text{H}}$ ($T \to 0$ K) is suppressed at low gate voltages due to the charge localization mechanism discussed above. $\mu_{\text{H}}$ is observed to increase as $T$ is lowered, requiring ever increasing values of $V_{bg}$ as $V_{bg}$ but decreases again below $T \sim 5$ K. A fit of $\mu_{\text{H}}(T, V_{bg} = -60$ V) to the $AT^{-\gamma}$ dependence yields $\gamma \sim (1 \pm 0.1)$. Finally Fig. 7f displays the $T$-dependence of the ratio between the measured and the ideal geometrical gate capacitance ($c_e^* = s e)/c_e$ where $s$ corresponds to the slopes extracted from the linear-fits in Fig. 7c. For a perfect FET this ratio should be equal to 1, i.e. the only charges in the conducting channel should be those resulting from the

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Figure 5 | Conductivity, i.e. $\sigma = 1/\rho$ (from the data in Fig. 4 d, acquired under $V_{bg} = 5$ mV) in a logarithmic scale as a function of $T^{-1/2}$. Red lines are linear fits, indicating that at lower $T$s and for gate voltages below a temperature dependent threshold value $V_{bg}(T)$ follows the dependence expected for two-dimensional variable-range hopping.

Figure 6 | Top panel: Drain to source current $I_{ds}$ as a function of ($k_B T/e)^{-1}$ for several values of the gate voltage $V_{bg}$ (from the data in Fig. 4a). Red lines are linear fits from which we extract the value of the Schottky energy barrier $\phi_{\text{SB}}$. Bottom panel: $\phi_{\text{SB}}$ in a logarithmic scale as a function of $V_{bg}$. Red line is a linear fit. The deviation from linearity indicates when the gate voltage matches the flat band condition$^{19}$ from which we extract the size of the Schottky barrier $\Phi = 16$ meV.

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**Conclusions**

In summary, field-effect transistors based on multi-layered p-doped WSe$_2$ can display peak hole mobilities in excess of 200 cm$^2$/Vs at room temperature. This value increases by a factor ~3.3 when the temperature decreases to ~100 K. The carrier density as a function of the gate voltage, as extracted from the Hall-effect, indicates larger effective gate capacitance. These spurious charges, in addition to disorder at the WSe$_2$/SiO$_2$ interface, leads to carrier localization and at a concomitant mobility edge. This manifests itself in an increasing threshold gate voltage for carrier conduction and, at a fixed gate voltage, in a concomitant decrease in carrier mobility upon cooling (resulting from an increase in the threshold gate voltage). When using Ti:Au for the electrical contacts one obtains a remarkably small value for the size of the Schottky barrier, although thermionic emission theory can only properly fit the transport data at higher temperatures.

We emphasize that our results indicate that WSe$_2$ displays what seems to be the highest Hall mobilities observed so far in TMDs, particularly among FETs based on few-layered TMDs exfoliated onto SiO$_2$ and remarkably, without the use of distinct or additional dielectric layers. The Hall mobility values observed here surpass, for example, the $\mu_{H}$ values in Ref. 17 for MoS$_2$ on HfO$_2$ or the field-effect mobilities of thicker multilayered MoS$_2$ flakes on Al$_2$O$_3$. This indicates that WSe$_2$ has the potential to display even higher carrier mobilities, particularly at room temperature, through the identification of suitable substrates (flatter interfaces, absence of impurities and dangling bonds, etc.), as well as contact materials. A major materials research effort must be undertaken to clarify the density of point defects (e.g. vacancies, intercalants) in the currently available materials and on how to decrease their density. However, our study reveals that WSe$_2$ has the potential to become as good if not a better material for optoelectronic applications than, for instance, multi-layered MoS$_2$. Recently, Ref. 44 reported the performance of multi-layered WSe$_2$ FETs, composed of WSe$_2$ atomic layers transferred onto a h-BN substrate using graphene for the electrical contacts as well as ionic liquid gating. Remarkably, despite the complexity of this architecture, originally intended to improve the overall performance of multi-layered WSe$_2$ FETs, the simpler devices reported here, still display considerably higher mobilities. We believe this is an import-
ant piece of information for those considering the development of electronic or optoelectronic applications based on transition metal dichalcogenides.

**Methods**

WS₂ single crystals were synthesized through a chemical vapor transport technique using iodine as the transport agent. Multi-layered flakes of WS₂ were exfoliated from these single crystals by using the “scotch-tape” micromechanical cleavage technique, and transferred onto p-doped Si wafers covered with a 270 nm thick layer of SiO₂. Prior to transferring the WS₂ crystals onto the SiO₂ layers, these were cleaned in the following way: SiO₂ was sonicated for 15 min in acetone, isopropanol and deionized water, respectively. It was subsequently dried by a nitrogen gas flow. For making the electrical contacts of Au was deposited onto a 4 nm layer of Ti via e-beam evaporation. Contacts were patterned using standard e-beam lithography techniques. After gold deposition, the devices were annealed at 200 °C for ~2 h in forming gas. Atomic force microscopy (AFM) imaging was performed using the Asylum Research MFP-3D AFM. Electrical characterization was performed by using a combination of sourcemeter (Keithley 2612 A), Lock-In amplifier (Signal Recovery 7265) and resistance bridges (Lakeshore 370) coupled to a Physical Property Measurement System. The Raman spectra were measured in a backscattering geometry using a 532 nm laser excitation. For additional details see the Supplementary Information.

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**Author contributions**

L.B. conceived the project in discussions with N.R.P., S.T., M.T. and P.M.A. D.R. wrote the manuscript with the input of all co-authors.

**Additional information**

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