CacheShield: Protecting Legacy Processes Against Cache Attacks

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ABSTRACT
Cache attacks pose a threat to any code whose execution flow or memory accesses depend on sensitive information. Especially in public clouds, where caches are shared across several tenants, cache attacks remain an unsolved problem. Cache attacks rely on evictions by the spy process, which alter the execution behavior of the victim process. We show that hardware performance events of cryptographic routines reveal the presence of cache attacks. Based on this observation, we propose CacheShield, a tool to protect legacy code by monitoring its execution and detecting the presence of cache attacks, thus providing the opportunity to take preventative measures. CacheShield can be run by users and does not require alteration of the OS or hypervisor, while previously proposed software-based countermeasures require cooperation from the hypervisor. Unlike methods that try to detect malicious processes, our approach is lean, as only a fraction of the system needs to be monitored. It also integrates well into today’s cloud infrastructure, as concerned users can opt to use CacheShield without support from the cloud service provider. Our results show that CacheShield detects cache attacks fast, with high reliability, and with few false positives, even in the presence of strong noise.

KEYWORDS
Cache attacks, Hardware performance counters, Change point detection

1 INTRODUCTION
Modern computing technologies like cloud computing build on shared hardware resources opaque to independent tenants, ensuring protection through sandboxing techniques. However, although this isolation is solid at the logical level, ensuring tenants cannot access each others memory, hypervisors cannot properly prevent information leakage stemming from the shared hardware resources such as caches. Compared to other resources like Branch Prediction Units or the DRAM, caches can be exploited to recover fine grain information from co-resident tenants in shared environments.

Cache attacks extract private information by setting up the cache memory, executing the victim process and observing effects related to sensitive data. Time-based cache attacks measure the effect on the victim process execution time [5] while access-based cache attacks measure the effect on the attacker [32]. Practical access-based cache attacks have been published for cloud environments with different variants: Prime+Probe [9, 17, 34, 47, 48], Flush+Reload [2, 13, 14, 43], and Flush+Reload [11]. All of them have demonstrated to recover cryptographic keys, break security protocols or infer privacy related information. They have shown that attacks can succeed in contemporary public cloud systems, with severe consequences to sensitive data of cloud customers.

To deter cache attacks, several techniques for detection and/or mitigation have been proposed. Most of the proposed mitigation techniques succeed in stopping cache based attacks, but are not being adopted by cloud service providers. Proposed hardware countermeasures require making modifications to the hardware that not only induce severe performance penalties but also take years to integrate and deploy into the infrastructure. Cloud hypervisors, on the contrary, can implement any of the proposed hypervisor based countermeasures [19, 21, 39] by just making small modifications to the kernel configuration. Despite the immediate fix that these countermeasures would provide, they are not being adopted by cloud providers, mainly due to the constant performance overhead that they add to their systems. Other feasible mitigation proposals consider periodic VM migration to avoid long-term co-location. VM migration, however, also introduces extra overhead whether there is an attack or not. Other proposals suggest that just as the attacker uses a side-channel to obtain information, the VM can defend itself by using a side-channel to detect co-resident tenants with possibly malicious intentions [46].

The current situation leaves tenants with little help from hardware and hypervisor designers or cloud service providers to protect themselves against cache attacks. Thus, we observe the necessity of giving those tenants that voluntarily want to protect against cache attacks, tools to defend themselves. So far, all known cache attacks have in common that they cause cache misses in the victim VM process. Thus, detecting an anomaly in the number of cache misses in the victim can indicate an ongoing cache attack and thus trigger VM migration or other actions to mitigate the attack.

Cache misses can be obtained by reading the hardware performance counters found in all modern processors. These hardware event counters track hardware events such as cache misses, and were originally intended to enable the detection of bottlenecks in executed software. Optimization is not the only application of these counters, it has also been demonstrated that the hardware performance counters are also useful to detect malware and security breaches [3, 8, 36, 40]. Libraries such as PAPI (Performance Application Programming Interface), facilitate the task of configuring and reading those hardware counters.

There have been several attempts to detect cache attacks using the hardware counters [7, 31, 45], but they have strong drawbacks.
Some works require the hypervisor to periodically monitor all existing processes, which introduces a great overhead in CPU usage and depends on how efficiently an attacker can hide from the monitoring tool [31, 45]. Other works offer solutions applicable to multi-process environments, but not feasible in cloud environments [7, 11].

We propose to use a monitoring service inside the VM that detects anomalies in the cache miss hardware performance counter only in the victim side. The monitoring service can be activated on demand inside the VM. The performance counters must be exposed to the VM in order to be feasible. Just changing the configuration of the hypervisor, it is possible to enable performance counters access inside the VM. This access can be enabled only in the VMs that request the service, and as the hypervisor is responsible for the virtualization of the counters that can be read inside a VM, they refer uniquely to this VM. That is, one VM can not read counters referring to another VM, even when they share the hardware. Right now, most cloud service providers only expose them if the customer is renting the whole machine, probably due to their fear of utilization as a side channel in hardware shared by various tenants. However, we believe they do not have much to worry about, as current attacking techniques exploiting shared hardware expose much more information than hardware counters would.

Our work demonstrates for the first time, that performance counter access for tenant VMs can indeed be utilized to improve security of the tenants. We offer tenant VMs a new monitoring service, CacheShield, to detect cache attacks. CacheShield can be activated before running sensitive processes. CacheShield detects attacks quickly and with high reliability and low CPU overhead, due to the use of Page’s cumulative sum method [30]. The CUSUM method is an unsupervised anomaly detection method, ensuring that even new attack techniques can be detected with high confidence. CacheShield automatically turns off if the monitored process is idle by detecting the lack of activity, resulting in a significant reduction in CPU processing overheads. In summary, our work presents a performance counter based monitoring service that users can voluntarily activate to detect when they are under attack.

- only monitors the victim process upon when active, i.e., the cloud service provider does not waste cycles continuously monitoring all processes.
- only requires the hypervisor to enable VM access to the performance counters, a feature commonly supported by all major hypervisor systems, including KVM, VMware and Xen. No other additional help from the underlying system is needed.
- implements an efficient algorithm that maximises fast and reliable attack detection, while minimizing false positives and keeping the performance overhead minimal and restricted to the victim VM.
- succeeds detecting all existing cache attacks, including stealthy attacks that are miss-detected by other solutions, e.g. Flush+Flush, since our detection uses attack characteristics that are independent of attack and victim behavior.

The rest of the paper is organized as follows. After discussing background and related work in Section 2, we show that monitoring performance events of a victim process is sufficient for reliable attack detection in Section 3. CacheShield is developed in Section 4. Section 5 presents the performance evaluation in several relevant scenarios and in section 6 we suggest different countermeasures. Finally, Section 7 discusses the conclusions of our work.

2 BACKGROUND AND RELATED WORK

2.1 Cache attacks

In the last years cache attacks have shown to pose a big threat in those systems in which the underlying hardware architecture is shared with a potential attacker. Cache attacks monitor the utilization of the cache to retrieve information about a co-resident victim. Indeed, if the utilization of such a hardware piece is directly correlated with a security-critical piece of information (e.g., a cryptographic key) the consequences of the attack can be as devastating as an impersonation of the victim.

Two main cache attack designs out-stand over the rest: the Flush+Reload and the Prime+Probe attacks. The first was first introduced in [13], and was later extended to target the LLC to retrieve cryptographic keys, TLS protocol session messages or keyboard keystrokes across VMs [12, 18, 43]. Further, Zhang et al. [48] showed that Flush+Reload is applicable in several commercial PaaS clouds. Despite its popularity and resistance to micro-architectural noise, the Flush+Reload presents a main drawback, as it can only be applied in systems in which memory deduplication mechanisms are in place, and further, can only recover information coming from statically allocated data.

The Prime+Probe attack design, contrary to the Flush+Reload attack, is agnostic to special OS features in the system, and therefore it can not only be applied in virtually every system, but further, it can additionally recover information from dynamically allocated data. This attack was first proposed for the L1 data cache in [29], while later was expanded to the L1 instruction cache [1]. Recently, it has been shown to also bypass several difficulties to target the LLC and recover cryptographic keys or keyboard typed keystrokes [9, 17, 22]. Even further, the Prime+Probe attack was used to retrieve a RSA key in the Amazon EC2 cloud [16].

Variations of both attacks have also been proposed to bypass specific difficulties found in some systems (e.g., lack of a flush instruction in the Instruction Set Architecture). Perhaps the one that most directly influences this work is the design of the Flush+Flush attack, as it was proposed to be stealthy and bypass attack monitoring systems [11]. This attack retrieves information by measuring the execution time of the flush instruction, thus avoiding direct cache accesses. As we will see, although this design might be effective against some of the proposed detection systems, ours correctly identifies when such an attack is being executed.

2.2 Performance counters

The performance counters are special purpose hardware registers that count a broad spectrum of low-level hardware events related to code execution. The selection of observable events is usually larger than the number of actual counters, hence, counters must be configured in advance. All events associated with a counter are recorded in parallel. As the PMU allows detailed insight into the state of the processor in real-time, it is a valuable tool for debugging applications and their performance. The list of available events consequently focuses on waiting periods (e.g., clock cycles
the processor is stalled), memory or bus accesses (e.g. cache misses or DRAM requests), and other performance-critical metrics like branch prediction or TLB events.

All main micro-processor architectures, i.e., Intel, AMD and ARM, include a bigger or a smaller number of these configurable registers. However, while monitoring of these hardware events in Intel and AMD processors is usually possible from user mode (when referring to an application also being run in user mode), ARM devices require root rights to enable them. Emulating the behavior in ARM devices, cloud providers might disable the utilization of performance counters from guest VMs. Indeed we find two main reasons why they would do this:

- Performance counters might be utilized with malicious purposes, similarly to the way the thermal sensor was used in [25], and retrieve information from co-resident user hardware utilization [6], which in theory should not be possible as the hypervisor only gives information to each VM about itself.
- As performance counters are hardware dependent, giving a guest VM access to benign utilization of performance counters might be problematic if guest VMs are migrated over different architectures, as customers would have to design code for different hardware architectures.

We do not believe that these facts should make cloud providers disable the usage of performance counters from guest VMs, specially when one can use them as a protection mechanism as we will see later in this work. In fact, attackers have already found alternative ways to retrieve the same information performance counters give. For instance, attackers can read the cycle counter or an incremental thread to know when TLB or cache misses occur. Thus, disabling the counters does not entirely prevent the leakage of hardware events information. As for the second claim, a possible solution could be to create clusters with the same hardware configuration, and migrate VMs within this cluster. Thus, we do not believe the above concerns are strong enough arguments against the guest VM performance counter usage. In this paper we will further show that such a usage can indeed offer more protection to cloud infrastructure customers.

2.3 Detection, mitigation and other countermeasures

HPCs have been used to detect generic malware [3, 35, 36] as well as microarchitectural attacks [7, 11, 31, 45]. Their success mostly depends on the ability to correctly identify cache (and other resource) attack patterns monitoring the associated event in the HPC. This approach is usually implemented at the OS or hypervisor level that has enough permissions to monitor what is running in the system. However, we observe two main problems with these detection-based approaches:

- Most of these detection approaches incur severe performance overheads that hypervisors or OSs do not seem willing to pay, as to the best of our knowledge no OS is implementing such a mechanism. This leaves the user of the system with few resources to know whether her code will be executed in a safe environment.
- As these detection countermeasures base their success on the monitoring of both the victim and the attacker processes, the attacker can vary patterns in a smart way to try to bypass the detection mechanisms.

These facts are observed, for instance in [7, 31, 45]. All three works incur significant overheads on all applications. CloudRadar, for example, requires three dedicated cores for its detection [45]. In addition, they usually assume the ability to monitor the attacking process [7, 11], which is not possible across VM boundaries (except for the hypervisor), and usually not even possible for user-level processes.

Detection-based countermeasures are not the only possibility shown to prevent cache timing attacks. Preemptive approaches can be taken at the hardware, software and application level. The first usually requires changes in the hardware pieces such that collisions in the cache can not happen, or if they do, they do not carry information [41]. The second involves the utilization of specific software features (e.g., page allocation) to prevent two processes from colliding in the cache [19]. Finally, the latter is achieved by utilizing specific tools to ensure a security sensitive binary does not leak information, even if it is under attack [44].

3 VICTIM-BASED ATTACK DETECTION

Our objective is to build an attack detection tool that detects any abuse of the LLC without any modifications to the hypervisor, OS, or the CPU hardware. Unlike previous approaches, we show that monitoring the behavior of a victim application is sufficient for the detection of cache attacks. To that end, we first analyze the behavior of these victim applications by monitoring several critical hardware performance counters. This behavior of critical applications is analyzed in the presence and absence of various cache attacks, and further analysis is performed to determine how well each counter serves as an indicator for ongoing attacks.

For the sake of simplicity, we base our analysis on cryptographic algorithms, which are the most popular target for cache attacks. Our approach can also detect attacks on other security-critical pieces of code like SSL/TLS protocol stacks. There are different types of cryptographic algorithms in use, which traditionally have been classified as symmetric cryptography an public-key cryptography.

**Symmetric cryptosystems** are sometimes also called private key algorithms, and include algorithms for encryption, authentication as well as hashing. Encryption and authentication schemes use single key for both the encryption/authentication and decryption/verification. Popular algorithms include AES and DES for encryption, SHA-2 and SHA-3 for hashing and HMAC or GCM for authentication or authenticated encryption. Symmetric primitives are usually heavily optimized for performance and feature constant execution flows. However, some implementations make use of table look-ups, which often result in exploitable cache leakage. One example is AES, the most widely used encryption algorithm. For AES, table look-ups are difficult to avoid, unless hardware support such as AES-NI is available.

**Public key cryptosystems** use a public key for encryption or verification and private key for decryption or signing. While public key cryptography can be used in more flexible ways, the used primitives are much more costly than for symmetric cryptography. As a result, public key cryptography is mainly
used for authentication and key exchange to establish a communication session, where payloads are protected using symmetric cryptography. Another important offered service are certificates, which require digital signatures for generation and verification of certificates. RSA, ECC and ElGamal are currently the prevailing schemes for public key cryptography.

As explained before, we only collect information about the victim processes, i.e. the processes operating on sensitive data. This approach avoids the need of monitoring other processes or VMs running in the same host. This approach also avoids relying on the information gathered from an attacker who might try to hide changes on its behavior to avoid triggering an alarm. Considering that each kind of algorithm presents different characteristics, we gather and analyze data of the execution of different algorithms in an initial scenario. Next, we show that the main results obtained in this scenario can be extended to others.

3.1 Analyzing Hardware Performance Events

Modern server CPUs make a large number hardware performance counters available, but only a limited number, typically 4 to 8, can be monitored in parallel. We use the Performance API (PAPI) [27] to access the performance counters. PAPI provides sufficient resolution to detect attacks while it also simplifies the task of collecting performance data. In this preliminary step, we collect data from 30 accessible hardware event counters on our test platform, for sample public and private key algorithms, in the presence and the absence of cache attacks. The PAPI interface provides instructions that allow us to read the counters for our process before and after each cryptographic operation, that is, we get detailed information about the variation of the counters for a single encryption or decryption execution. Since the number of counters that can be read at the same time is limited, we collect the data for different groups of counters at different times. We then join the data and compute the statistics. Once we get all this data, we carry further study to determine and quantify which counters provide meaningful information to detect the attacks.

As sample victim algorithms for this analysis, we chose the software AES T-Table implementation and the RSA sliding window implementation (with flag RSA_FLAG_NO_CONSTTIME set) of OpenSSL 1.0.1f, which give representative results for public key and symmetric key cryptography. As sample attacks we use the Flush+Reload against both implementations. Flush+Reload tries to gain information from the execution of certain instructions or from the accesses to certain data which depend on the key. For the used version of RSA, attacks target the instructions (depending on the implementation RSA can also be attacked considering accesses to data), while AES attacks are an example of cache attacks focused on the data.

Our experiments are performed on an Intel Core i7-4790 CPU 3.60 GHz machine with 8 MB of L3 cache and 8 GB of RAM, with Centos 7 OS. For each counter we collect samples for 1 million encryption or decryption operations. One noteworthy observation is that, whereas in the case of AES the values of the counters do not seem to depend on the key. For the analyzed vulnerable RSA implementation, however, some of the parameters depend on the value of the key. This behavior can be noticed, for example, in the number of instructions executed and in the decryption times. In fact, the number of operations performed depends on the distribution of zeros and ones in the key. However, while the number of instructions is not affected by the attacks, the decryption times are, as they include the extra times for cache misses.

We can select up to 5 or 6 counters which are representative of the attacks, as this is the maximum number of counters readable in parallel on our platform. The number of counters that can be read at the same time also varies depending on which counters are used and the combination of them. In order to decide which counters carry more information relative to the attacks, we use the WEKA tool [15]. This tool was designed with the aim of allowing researchers to easily access to state-of-the-art techniques in machine learning. WEKA implements several algorithms to perform attribute selection. As inputs for the tool, we select a subset among all the samples (otherwise the time it takes to perform the selection increases exponentially). We randomly select 50000 instances of each of the groups, that is for AES attack and non-attack and for RSA attack and non-attack, so we obtain 200000 samples with information about 30 counters, each labeled with ‘1’ for attacks and ‘0’ for non-attacks.

We first use the InfoGain function, which evaluates the worth of an attribute by measuring the information gain with respect to the class according with "$\text{InfoGain(Class,Attribute)} = H(\text{Class}) - H(\text{Class | Attribute})$, where H is the entropy. Note that our experiments are balanced between attack and non-attack "classes", that is $H(\text{Class})= 1$, thus an ideal attribute would gain 1 bit. Values around 0.5 may indicate the attribute carries meaningful information, but only for one of the algorithms or one of the attacks. Thus, L3 cache misses are not only the most meaningful predictions, but also work across the considered scenarios.

We have also evaluated the relief algorithm [20] for feature selection. Unlike the InfoGain, which only evaluates information gained from each attribute individually, the relief algorithm outputs a score of the predictive value of an attribute relative to other attributes. More positive weights indicate more predictability for this attribute. To calculate the weight of an attribute, it iteratively first identifies the nearest neighbors from the same and different classes. Then, weight increases if a change in the attribute leads to a change in the class and decreases when a change in the attribute value has no effect on the class.

Table 1 presents a summary of the attributes which give most relevant information for detection according to the selection algorithms, altogether with their mean values for the considered scenarios, and with the differences between attacks and the expected behavior. Both tests indicate that L3 cache misses are most meaningful. In fact, the relief algorithm scores all other attributes with very low scores, implying only little additional gain from using them.

3.2 Concurrent Signal Assessment

Tracking hardware performance events for each cryptographic operation showed that victim-based attack detection is feasible and helped identifying relevant counters. However, achieving fast detection with this approach, would require adding instructions in the middle of the code we want to protect. Hence, it requires alteration of the target code, which adds unnecessary burden on
Table 1: Overview of most relevant hardware performance counters in the presence and absence of attacks, over 1 million calls to RSA and AES, as well as their rankings according to the InfoGain and relieff metrics. Level 3 cache misses, PAPI_L3_TCM, clearly have the strongest information for cache attacks.

| Performance Counter | AES Normal µn | AES w/ Attack µa1 | AES w/ Attack µa1 - µn | AES Normal µa2 | AES w/ Attack µa2 - µn | RSA Normal µn | RSA Attack µa | Joint Evaluation Algorithms infoGain Relief |
|---------------------|---------------|-------------------|--------------------|----------------|----------------------|---------------|---------------|-------------------------------------------|
| PAPI_L3_TCM         | 0.0002        | 0.92              | 0.9189             | 3.56           | 3.5598               | 1.12          | 2601.4        | 2600.28        | 0.885 | 0.245 |
| Cycles (rdtsc)      | 612.33        | 828.60            | 216.27             | 1151.71        | 539.38               | 8.840e+07     | 8.956e+07     | 1.151e+06      | 0.714 | 0.014 |
| PAPI_REF_CYC        | 61.93         | 71.01             | 9.08               | 79.93          | 18                   | 2.453e+06     | 2.484e+06     | 3.1e+04         | 0.683 | 0.005 |
| PAPI_CA_SNPRINTF    | 21.95         | 28.77             | 6.82               | 30.35          | 8.4                  | 727.87        | 3417.5        | 2689.63        | 0.531 | 0.034 |
| PAPI_CA_INV         | 21.99         | 28.83             | 6.86               | 30.45          | 8.46                 | 727.88        | 3417.6        | 2689.72        | 0.530 | 0.033 |
| PAPI_L3_TCR         | 24.65         | 24.73             | 0.08               | 25.90          | 1.25                 | 490.47        | 3253.6        | 2763.13        | 0.528 | 0.029 |
| PAPI_L2_TCM         | 28.31         | 28.51             | 0.2                | 28.42          | 0.09                 | 559.27        | 3325.6        | 2766.33        | 0.513 | 0.028 |
| PAPI_L2_ICM         | 15.51         | 9.16              | -6.35              | 11.86          | -3.65                | 381.12        | 3149.2        | 2768.08        | 0.510 | 0.056 |

Figure 1: Mean LLC miss traces over time for AES and RSA executions in the presence and absence of cache attacks. The numbers next to flush indicate the number of lines flushed at a time. After the start up peaks, the misses go to zero in the absence of a cache attack, while under attack they remain high.

The initial transient state, the number of misses goes to zero in the absence of attacks (aes no attack and rsa no attack) for both crypto primitives. It can also be observed that the mean number of misses in the case of an attack varies with the number of lines flushed each time aes 1 flush, aes 2 flush, .... Thus, with concurrent monitoring, both algorithms behave similarly for the normal executions.

Switching to continuous monitoring of the counters implies that the information on total encryption times or reference cycles is no longer useful nor available. To ensure the information of the other counters mentioned in Table 1 is still optimal for attack detection, we performed a new analysis considering each sample collected at a period of 1 ms as an independent input to the selection attribute algorithms. The results show that for the LLC misses counter the infoGain increases up to 0.92, while values for the other counters decreases. Additionally, the relief algorithm output still gives better score for the L3 cache misses (0.18) and in this scenario, this value is still 5 times bigger than the weight of the next counter, indicating the L3_TCM is still the one counter of choice for cache attack detection.

We performed additional experiments to determine how well a cluster algorithm would distinguish between attacks and non-attacks with the periodically sampled data from several counters at once. WEKA also includes clustering algorithms. We tested EM and Self Organizing Maps, setting the number of clusters to two. The most interesting result of this experiments is that while these algorithms were able to classify in the same cluster respectively 84% and 91% of the attack samples when using only the LLC misses counter, this number decreases to around 50-60% when adding other counters. These results indicate that cache attacks can be detected, regardless of the algorithm the victim process runs, by only using information gathered from the L3 cache miss counter. The algorithms feature zero misses after the initial warm-up, except if an attacker is forcing misses. Additionally, as all known cache attacks, including Flush+Flush, cause cache misses on the victim process to obtain information, the results obtained here for the Flush+Reload attack are applicable for other attacks. Thus, we decided to only use this one attribute, as it provides most information and, also allows us to keep the detection tool simple.
4 CACHE SHIELD

So far, techniques proposed to detect cache attacks imply monitoring the victim VM, the attacker VM, and any other VM running in the same host [7, 45]. Monitoring all VMs at rates which vary from 1 us to 5 ms result in huge overheads, and increases with each new virtual machine allocated in the same host.

As a consequence, cloud providers may not want to implement such a tool, as it increases overall system cost, while the benefit of preventing cache attacks might be a benefit only few customers are willing to pay for. Yet, only the hypervisor, and thus the cloud service provider (CSP) has the ability to monitor all VMs on a system. Indeed, as of now, we are not aware of any CSPs employing VM monitoring for microarchitectural attacks.

As a difference with previous approaches, our goal is to design CacheShield in such a way that we avoid monitoring all the other processes or VMs running in the same host, i.e., we only focus on our own process. We assume that we have access to the performance counters within the VMs. Although most cloud providers currently do not allow access to the performance counters, hypervisor systems such as VMware and KVM can be easily configured to permit reading the counters inside the VM. Moreover, it is possible to decide which of the VMs allocated in a host would have access to the counters for their processes upon request. Even when our approach can be implemented at the hypervisor, we believe that for cloud providers would be easier just to enable the counters for the VMs that require it, leaving the responsibility on them, than to take care of these attacks.

By leaving the choice of deciding which processes should be monitored and when in the hands of the user, the impact in performance of such monitoring is reduced to a minimum, as we only watch a possible victim when it is executing the protected task. From the cloud provider’s point of view, this way of facing detection also means no waste, as it only affects the implied VM and only when it is necessary. Additionally, as the user decides when it is necessary to protect a process, we avoid the need to detect when a sensitive process is executed. As a consequence, we also reduce the risk of not detecting the execution of this sensitive process and then the probability of missing an attack.

Figure 2 presents a diagram of our proposed solution. Whenever a user wants protection, he informs the CacheShield module, which utilizes the information gathered from the performance counters to decide whether the user is being attacked. If CacheShield detects an attack, an appropriate response mechanism to prevent the information leakage is put in place. Although we mainly focus on the detection phase, we discuss in Section 6 some of the countermeasures that can be implemented to effectively prevent the attack from retrieving information, such as the utilization of a fake key or the addition of noise patterns in the cache.

4.1 Detection Algorithm

One of our goals is obtaining a technique for attack detection no matter which algorithm is being attacked. Additionally, we want to detect all types of cache attacks, even unknown attacks, for which the tool has not been trained to detect.

Supervised learning algorithms such as neural networks, have already been used to detect certain cache attacks. As any supervised algorithm they have to be "trained" to detect the attack. That is, they require a labeled data set including data from the different attacks we want to detect, so they can build models of them and identify their characteristic features. The drawback of supervised learning is precisely that we need to train the algorithm for each situation, for each algorithm and each attack. As a consequence new attacks, or attacks with different patterns would not be detected.

The alternative is using unsupervised techniques. An unsupervised algorithm does not receive labeled data, by itself tries to cluster the received data into different groups or to find relationships between different inputs in order to put any new sample in the appropriate cluster. We will briefly explore clustering techniques in the next section to select the counters which can identify an attack. Other kind of unsupervised techniques are anomaly-based detection algorithms, which in theory could detect "zero-day" attacks.

Change-point detection methods are designed to deal with the problem of detecting abrupt changes in distributions. Under the assumption that cache attacks have an effect in the performance of the protected algorithms, change-point detection algorithms stand as great candidates to detect LLC attacks. We propose an algorithm based on change point-detection techniques which is self-learning so it adapts itself to detect different attack patterns, which allows us to fix the attack detection delay, and which is computationally simple so it respects the constraint of minimum impact in performance and can be implemented online.

4.2 Cache Shield Design

CacheShield monitors the counters for LLC misses and for total cycles. The former gives information about the use of the LLC of the protected processes while the latter gives information about when it is running or when it has finished. Based on Figure 2, the CacheShield module needs the PID of the process we desire to protect and the process protected also needs to know the PID of the CacheShield process. The reason is both processes need to communicate with each other (one needs to inform the other when to watch and other needs to inform the one when there is an attack going on), and that the counters can be attached to gather the data from a single process given its PID.

On Unix systems, the easiest way to use CacheShield is to use the fork operation, and then to use the exec system call to run the module and to give it the PID of the parent process. The parent process then can execute the desired operation while being monitored. In case that the parent process stops or waits for something, CacheShield automatically stops after noticing the parent has not
been running for a while. This means that when the parent runs again, it needs to send a "SIGCONT" signal to the CacheShield tool. In a similar way, if the tool detects an attack, it can send a signal to inform the parent. On Windows Systems the mechanisms for inter-process communications are slightly different, but the tool can be also adapted.

**Change Point Detection:** In order to effectively assess the detection task, we made use of change point detection theory (CPD) [4]. This theory can be used to construct the commonly known as quick expression alarm, the mean time between false alarms will be given by the theory of change point detection leads to the development of efficient algorithms presenting certain optimality properties, in the sense that for a given false-alarm rate (FAR) they minimize the sense that for a given false-alarm rate (FAR) they minimize the detection time for the given threshold is

\[ s(t) = \ln \left( \frac{p_1(X(t), X(1), \ldots, X(t-1))}{p_0(X(t), X(1), \ldots, X(t-1))} \right) \]

The key property of this ratio is that a change in the parameter under study will also cause a change in the sign of the log-likelihood ratio. In other words, \( s(t) \) shows a negative drift before change and a positive drift after change. The relevant information for the detection task lies then in the difference between the value of \( s \) and a minimum value. The decision rule is based on a comparison with a threshold \( h \):

\[ g_k = S_k - m_k \geq h \]

where

\[ S_k = \sum_{i=1}^{k} s(t) \quad m_k = \min_{1 \leq j \leq k} S_j \]

This decision rule can be replaced by the following, which obeys the recursion and whose value for the initial observation is \( k = 0 \).

\[ g_k = \max \left\{ 0, g_{k-1} + \ln \frac{p_1(X(k))}{p_0(X(k))} \right\} \geq h \]

Then the detection time for the given threshold is

\[ \tau(h) = \min \left\{ k \geq 1 : g_k \geq h \right\} \]

Although this first approach considers that both distributions are known, this assumption is usually not true, and as a consequence this proposal has to be adapted for each situation. We may know one distribution in advance or none, so it may be necessary to estimate the parameters of the algorithm during the runtime. As long as the estimators for the distributions and the real observation meet certain convergence conditions, we will be able to fix for example the desired detection delay or the FAR.

**Change Point Detection in CacheShield:** While facing the cache attack detection, the attack may start from the very beginning or it may start after a few “normal” transactions. Both situations are efficiently managed by the proposed CUSUM algorithm. We assume that each new sample can be classified into one of two different groups or clusters, namely “attack” and “non-attack”. The "non-attack" cluster represents how we expect the protected process to behave under normal conditions. Based on the information we can gain from the counts, this assumption is that after a few samples corresponding to the initialization of the protected process, the number of L3 cache misses will be around 0, then \( \mu_{na} = 0 \). On the other hand, when there is an attack, we have observed that the mean number of misses is \( \mu_a \). Then each new sample belonging to the “attack” cluster will be around \( \mu_a \). The value of \( \mu_a \) is unknown and depends on the attack so it needs to be computed and recalculated with each new sample.

If we denote as \( miss_i \) each new sample that the CacheShield module gets referring to the protected process, we need to decide if
it belongs to one cluster or to the other. To do so, we compute the value of the "probability" that \( \text{miss}_i \) belongs to each one making use of the distance metric, this way we define the distance from \( \text{miss}_i \) to \( \mu_{na} \) as:

\[
d_{na}(i) = \text{miss}_i - \mu_{na} = \text{miss}_i
\]

Then, the distance with the "attack" cluster will be

\[
d_{a}(i) = |\text{miss}_i - \mu_a|
\]

As stated before the value of \( \mu_a \) is unknown when we start to monitor the process. We select an arbitrary initial value, and whenever a new sample \( \text{miss}_i \) is obtained, if \( \text{miss}_i \geq 0 \) we update the value of \( \mu_a \) as follows:

\[
\mu_a = (1 - \beta) * \mu_a + \beta * \text{miss}_i
\]

This method is known as exponentially weighted moving average, where the weight of the older datum decreases exponentially. This way of estimating the mean of the "attack cluster" makes the election of the initial arbitrary value irrelevant after collecting a few misses samples. If the initial value is chosen too low, we may trigger false positives. We recommend the election of an initial value higher than 10, in order to keep the rate of false positives low, while being able to detect the attack in a reasonable time. We will further discuss the noise tolerance of the proposed detection algorithm in the next section. In our experiments we set \( \beta = 0.05 \) and the initial value to 12.5.

Now we are in conditions to define the probability of belonging to each cluster:

\[
p_{na}(\text{miss}_i) = \frac{d_{a}(i) + 1}{[d_{na}(i)] + |d_{a}(i)|}, \quad p_{a}(\text{miss}_i) = \frac{d_{na}(i) + 1}{[d_{na}(i)] + |d_{a}(i)|}
\]

The value 1 has been added to avoid divisions by 0 in the LLR calculation that has to be performed as part of the detection algorithm. As a result, for every sample \( k, k \leq 1 \) we can express the detection rule as follows:

\[
g_k = \max \left\{ 0, g_{k-1} + \log \frac{d_{na}(k) + 1}{d_{a}(k)} \right\} \geq h
\]

As it can be easily derived from the previous equation and according to the properties of the LLR, when the number of misses is 0 or close to 0, the distance between the sample and the 'non-attack' cluster \( d_{na}(k) \) will be lower than the distance to the attack cluster \( d_{a}(k) \), so the value of the metric \( g_k \) decreases or stays at zero. On the other hand, readings from the LLC misses counter approaching to the attack cluster will increase the value \( g_k \). The properties of this approach let us choose the threshold based on a minimum detection time we want to achieve. Note that when the error in the estimation of the mean \( \epsilon \) approaches to zero, \( d_{a}(i) = \epsilon \) also tends to zero, then the increase in the value of \( g_k \) is also limited

\[
\log \frac{d_{na}(k) + 1}{d_{a}(k)} \leq \log(\mu_a + 1)
\]

As a consequence, the minimum expected detection time for the given threshold \( h \) is:

\[
\tau_e(h) \geq \frac{h}{\log(\mu_a + 1)}
\]

or reformulating this equation, the threshold \( h \), for a minimum expected delay \( \tau_e \)

\[
h \leq \tau_e * \log(\mu_a + 1)
\]

Figure 3: Relevant parameters for the detection task, prime+probe attack on AES

The unit of the \( \tau_e(h) \) is number of samples. Given that the most effective cache attacks can potentially extract most of the key with just one execution of the victim, the sampling rate must be chosen lower than the execution time of the victim. As the execution time of these algorithms is in the order of few milliseconds, a sampling rate of 100 \( \mu s \) seems sufficient to provide evidence of the attack. This frequency can be increased at additional load for the system. So, for an expected detection delay of 1 ms with a sampling rate of 100 \( \mu s \) we can define the threshold as \( h = 10 * \log(\mu_a + 1) \). As a result of this selection of \( h \), when the \( \mu_a \) is recalculated, the threshold should be recalculated too. The choice of the threshold \( h \) also determines the tolerance to noisy frames, and as a consequence the false positive rate. In practice, the false positive rate cannot be estimated and has to be measured.

Algorithm 1 summarizes CacheShield implementation and an example of the values of the parameters considered in the detection process is given in Figure 3.

Algorithm 1 CacheShield detection algorithm

**Input:** Process PID
**Output:** Attack detected

\[
\text{read_counters(misses,cpu_cycles);} \quad \text{wait};
\]

\[
\text{while victim_is_running} \quad \text{do}
\]

\[
\text{read_counters(misses,cpu_cycles);} \quad \text{if misses > 0} \quad \text{then}
\]

\[
\text{update \mu_a;} \quad \text{update \mu;}
\]

\[
\text{end if}
\]

\[
\text{calculate \( g_k \);} \quad \text{if \( g_k > h \) then}
\]

\[
\text{trigger_alarm;} \quad \text{end if}
\]

\[
\text{wait;}
\]

**return detected;**

5  EVALUATION OF CACHESHIELD

Once we have defined the relevant parameters of the detection algorithm and described it in detail, we evaluate its performance. To this end we ran several experiments in different environments and machines.

Native Environment The experiments for non-virtualized environments were performed in an Intel Core i7-4790 CPU 3.60GHz
machine with 8 MB of L3 cache and 8 GB of RAM, with Centos 7 OS.

**KVM-based Hypervisor** These experiments used the same hardware as above, but this time within a VM also with Centos 7 hosted in KVM as hypervisor.

**VMware-based Cloud Server** We have also executed experiments in a host managed with VMware, this machine is equipped with an Intel XeonE5-2670 v2 processor, 25Mb of L3 cache and 32GB of RAM. The OS in these VMs was Ubuntu 12.04.

When a user is executing the crypto algorithm in their own machine, they can get information about the utilization of such machine or other task running concurrently. However, when executing the crypto algorithms in cloud environments they cannot get any information about what their neighbors are doing. In such scenarios, it becomes mandatory to study how the execution of different applications running in parallel with the protected process affects the behavior of CacheShield. Note that as we use the "total cycles" counter (to determine if the victim is executing or not) and the LLC misses counter to decide if there is an attack going on, applications consuming high amount of memory resources are the most likely to cause the LLC misses indicator to rise, and as a consequence, to trigger false positives. For this reason, we have selected several worst-case scenario applications with high memory activity to run in parallel with the victim and CacheShield:

**Yahoo Cloud Serving Benchmark** This benchmark was originally designed as a tool that provides a common evaluation framework and a set of common workloads to test the performance of different serving stores as elastic search, Cassandra, MongoDB among others [33]. It allows different configurations for the workloads and provides a set of example workload scenarios, together with a workload generator, which generates the load to test storage systems. In our experiments, we use this benchmark with the Apache Cassandra database and the example workload named workloads.

**Video Streaming** Another kind of application that can generate cache misses is web-browsing or video streaming. The video streaming VM continuously streams and plays back youtube videos on the firefox browser.

**Randmem Benchmark** This benchmark was originally intended to test the impact of burst reading and writings [24]. Depending on the configuration, the benchmark accesses data stored in an array either sequentially or in random order. The tool also allows to configure the size of the memory it is going to use, by default it tries to use as much as possible, up to 2 GB. In our experiments, we launch each randmem instance with no memory limitation, which means 2 GB of RAM memory are used by each instance.

To show the applicability of CacheShield to a broad range of implementations that require protection against cache attacks, we chose from a range of crypto primitives and implementations, though focusing on vulnerable ones, since such legacy implementations actually require protection. The three crypto algorithms considered as victims are

**AES** as the most common symmetric encryption algorithm. We consider the T-Table implementation of AES from Openssl 1.0.1f, which is fast, but also leaky.

**RSA** is the probably most widely used signature and public key encryption algorithm. We analyzed the RSA implementation from Openssl 1.0.1f, with a 2048 bit key, and the RSA_FLAG_NO_CONSTTIME flag set.

**ElGamal** we chose the ElGamal implementation of libgcrypt 1.5.0 with a 4096 bits key. Unlike AES and RSA, ElGamal was not considered during the design of CacheShield, and hence shows how CacheShield can be expected to perform for other types of algorithms.

These algorithms differ quite significantly in their particular implementation and usage of cache. Many other potentially leaky codes might require protection, and we are confident that CacheShield will perform well.

To evaluate the effectiveness of CacheShield across different types of cache attacks, we implemented and performed three popular attacks, namely Flush+Reload, Flush+Flush and Prime+Probe. We collected data for the above-mentioned algorithms under attack as well as from normal executions, as baseline behavior. Under each configuration, we collect data for more than 1000 executions of the crypto primitives, and in the case of the AES attack we also consider different attack rates (number of lines flushed at a time), as the attacker may try to gain different amount of information from the T-tables per execution [10]. As stated in previous sections, the main characteristics defining the detection algorithm are the mean detection time, and the false positive rate. Table 2 presents the results for mean detection time under different configurations, for the different attacks and algorithms and table 3 shows the results related with false positives in noisy environments.

Note that the attack requirements for Flush+Reload, Flush+Flush and Prime+Probe differ significantly. While Flush+X attacks are faster and more precise, they require shared data, i.e. deduplication between attacker and victim. All the attacks performed in virtualized scenarios were across VMs so we enabled deduplication features (KSM and TPS for KVM and vmware respectively) to perform Flush+X attacks. Prime+Probe attacks work across VMs even without deduplication, so we disabled deduplication and enabled huge pages. Prime+Probe attacks require, prior to the information extraction, a profiling of the cache [9, 16, 17]. The profiling stage reveals the sets the victim process is accessing and that carry the necessary information to succeed in the attack. In this situation, the detection tool will trigger an alarm whenever the set being tested by the attacker was actually used by the victim. Fig. 4 visualizes the output of the detection algorithm, for the cache profiling stage of an 8 MB L3 cache when the target is the T-table implementation of AES. The x-axis represents each set of the cache being evicted during the Prime+Probe profiling step; a 1 on the the y-axis indicates that an alarm has been triggered. Thus, alarms are only triggered when the cache attack affects the target.

For all evaluated attacks, the detection rates are 100%. Note that the sampling rate is 100 μs and that we want to detect the attack before the end of each decryption (for public key cryptography). If we wished to detect attacks against algorithms whose duration is below 5 or 6 ms, we will need to increase the sampling rate, since mean number of samples required to detect the attack cannot be lowered arbitrarily without increasing the FAR too much. The duration of the decryption/encryption depends on frequency of
Table 2: Mean detection time (ms) per attack and scenario for the evaluated crypto algorithms. Note that in all cases CacheShield has the same configuration and that detection times are much lower than the ones required for the attack to succeed.

| Scenario | AES F+R (1) | AES F+R (4) | AES F+F (1) | RSA F+R | RSA F+F | RSA P+P | ElGamal F+R | ElGamal F+F | ElGamal P+P |
|----------|-------------|-------------|-------------|---------|---------|---------|-------------|-------------|-------------|
| Native   | 3.98        | 4.48        | 3.38        | 5.08    | 3.70    | 5.16    | 2.97        | 3.47        | 3.68        |
| KVM      | 7.38        | 7.05        | 6.64        | 9.53    | 4.08    | 3.92    | 4.93        | 3.76        | 3.45        | 3.98        |
| Vmware   | 8.75        | 5.98        | 10.74       | 13.42   | 4.43    | 3.87    | 4.51        | 4.83        | 5.06        | 7.08        |

Table 3: False positive rate for different scenarios and algorithms. (Instances: Y - Yahoo Cloud Serving, V - Video Streaming; R - Randmem)

| Scenario | Noise Instances | False Positives |
|----------|-----------------|-----------------|
| Y        | V               | R               | AES   | RSA   | ElGamal |
| KVM      | 1               | 0               | 0     | 1.2%  | 4.5%    | 2.8%    |
| KVM      | 0               | 1               | 0     | 1.1%  | 3.4%    | 0.6%    |
| KVM      | 0               | 0               | 1     | 12.2% | 21.4%   | 15.4%   |
| Native   | 1               | 0               | 0     | 1.2%  | 4.1%    | 2.4%    |
| Native   | 0               | 1               | 0     | 0.5%  | 1.3%    | 0.3%    |
| Native   | 0               | 0               | 1     | 11.1% | 19.2%   | 13.8%   |
| VMware   | 1               | 2               | 10    | 0.1%  | 5.9%    | 4.1%    |

Figure 4: Output of CacheShield when the cache is profiled accessing each set. ’1’ indicates a positive attack detection.

the processor, and as a consequence on the machine. For example, ElGamal encryption takes around 11 ms when being attacked on the i7 machine, while this time increases up to 24 ms on the Xeon machine. Thus, we are able to detect attacks against ElGamal when less than the 37% of the encryption has been performed for the i7 machine, and 30% for the second machine in the worst case. Regarding to RSA this mean execution times are around 18 ms for the i7 machine and around 37 ms for the other. Then, in the worst case, on average we detect the attacks with less than 50% of the decryption performed in the first case and with about 37% of decryption in the second one.

Regarding to the existing differences between false positive rates for AES and public crypto algorithms, these are easy to explain. While between AES encryptions exists some time in which the processor does nothing, the others execute uninterruptedly. This fact increases the probability of other processes accessing the cache during the same interval. For example, while the AES encryption in the period of 100 µs is only active during around 7000 cycles while the RSA process is active during about 30000 cycles for the VMware machine when there is no attack. Fig. 5 depicts the LLC misses for one noisy RSA encryption, besides the initialization steps, it can be observed a high amount of cache misses during the whole encryption. Similarly, Fig. 6 corresponds to one process performing AES encryptions.

The results also show that the tolerance to noise of the detection algorithm is more dependent on the hardware than on the virtualizing technology: While the results for the native and KVM scenarios are similar and the hardware is the same, the results are significantly better on the Xeon machine. The Xeon machine did not trigger any false positives when there were one or two VMs generating “noise” concurrently, until we launched several more instances. As this machine is more similar to the kind of machine cloud providers utilize, these results show that the tool is practical in these environments.

One approach to reduce the false positives in noisy environments could be considering the variance of the samples collected in the CUSUM algorithms proposed, as attacks present low variance compared with noise. However, we could fail to detect attacks masquerading as memory activity by generating different number of misses each time. Another consideration relative to memory utilization, and the false positives that are triggered when is high memory utilization is that Prime+Probe attacks need low memory activity to accurately locate the sets and to perform the attack, other way it renders much more difficult. On the other hand, Flush+Flush attacks are more tolerant to noise, but memory activity degrade its performance. So it is not likely that the attacker performs the attack in a situation where the memory is highly utilized. Additionally, the level of utilization of public clouds is low [23], so the assumption of high memory utilization in the considered cloud scenarios may not be realistic. As for using the tool in our controlled physical
One last consideration about our tool is the amount of CPU it utilizes to monitor the victim and compute the detection algorithm. Fig. 7 and 8 show the mean CPU utilization of CacheShield for different sampling rates and for different situations, namely when the victim is attacked and when is not, because the amount of operations it has to do changes, and again for both architectures, depending on the sampling rate. To obtain the CPU utilization we have measured the time it takes to read the counters and perform the calculations and the total time elapsed, then the utilization is given by its division. Note that sampling rates of 10 µs are not always achievable as sometimes (around 10% of the time) it takes more time to read the counters and perform the calculations. Note that in both cases total utilization of our tool is below 5% of CPU utilization.

6 CACHE ATTACK COUNTERMEASURES

Once an attack has been detected, CacheShield needs to react in some way. One way is to simply interrupt the monitored process and to purge used keys. While this approach ensures high security, it decreases the usability, as any false positives will result a total cryptosystem shutdown. An alternative is to continue execution, but to apply preventative measures to reduce or prevent the exploitability of the cache.

Adding Noise A simple method to hinder cache attacks is making the channel noisier, e.g. through frequently flushing cache lines used by the protected process, or by performing additional reads on data. This approach works particularly well if critical data is known, e.g. the tables of an AES implementation.

Dummy Operations An alternative approach is to perform dummy operations on meaningless secrets. In practice this can mean to run the protected process with a newly generated secret. The original process can either be paused, or be continued in parallel to the dummy process. Parallel processing obfuscates the true leakage. However, depending on the attack type, an attacker might still succeed with an increased number of observations. Pausing has the advantage that the attacker might actually extract the dummy key and discontinue the attack. The monitor can then restart the original process in the absence of the attack. Either way, the performance degradation is not negligible, but it only is incurred in the presence of an attack.

Protected Implementations The main reason why leakage is still observed in security solutions is the performance overhead that pure constant time implementations present. A way of avoiding such a scenario is to use protected implementations only when CacheShield detects an attack behavior. When no attack is detected, faster (less secure) implementations can be used.

Other more sophisticated solutions are also possible, but might not be as universally applicable. Since our focus is on the lightweight detectability of cache attacks at the user level, we do not explore these additional avenues of countermeasures.

7 CONCLUSION

In this work we have introduced CacheShield, a tool that is able to detect all known types of cache attacks targeting cryptographic applications. The analysis of various hardware performance counters revealed that the LLC miss counter by itself carries enough information to detect cache attacks. We take advantage of change point detection algorithms and adapt them to our objective of cache attack detection. CacheShield was designed to detect attacks based on the characteristics of two particular algorithms, AES and RSA. The evaluation revealed that CacheShield can also be used for other algorithms (as shown for ElGamal) without further modification. It is also effective against “unknown” attacks, as all known attacks force cache misses on the victim. This behavior can be easily detected, since the number of L3 cache misses of crypto algorithms approaches zero after a brief initial warm-up. In addition, we have shown that CacheShield tolerates considerably high amount of noise only triggering a few false positives in machines similar to the ones cloud providers use.

Previously proposed cache attack detection tools work at the hypervisor level and also need to continuously monitor all untrusted and concurrently running processes or VMs, resulting in huge performance overheads and often have questionable detection rates for novel attacks such as F1ush+F1ush. CacheShield only needs access to the protected victim process, and only during its execution,
greatly reducing the waste. All major hypervisor systems support transparent access to hardware performance counters for guest VMs while ensuring proper isolation between VMs. We urge Cloud Service Providers to enable these features in their systems and thus give their tenants finally the means to protect themselves against cache attacks with tools such as CacheShield.

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REFERENCES

[1] Onur Acımez and Werner Schindler. 2008. A Vulnerability in RSA Implementations Due to Instruction Cache Analysis and its Demonstration on OpenSSL. In Topics in Cryptology–CT-RSA 2008. Springer, 256–273.

[2] Gorka Irazoqui Apecechea, Mehmet Sinan Inci, Thomas Eisenbarth, and Berk Sunar. 2014. Wait a Minute! A fast, Cross-VM Attack on AES. In Advances in Cryptology, Intrusions and Defenses - 17th International Symposium, RAID 2014, Gothenburg, Sweden, September 17-19, 2014. Proceedings, 299–319. DOI: https://doi.org/10.1007/978-3-319-13379-1_15

[3] M. B. Bahador, M. Abadi, and A. Tajoddin. 2014. HPC MallHunter: Behavioral malware detection using hardware performance counters and singular value decomposition. In 4th International Conference on Computer and Knowledge Engineering (ICCKE). 703–708.

[4] Michele Bassivegge and Igor V. Nikiforov. 1993. Detection of Abrupt Changes: Theory and Application. Prentice-Hall, Inc., Upper Saddle River, NJ, USA.

[5] Daniel J. Bernstein. 2005. Cache-timing attacks on AES. Technical Report.

[6] Sarani Bhattacharya and Debdeep Mukhopadhyay. 2015. Who Watches the Watchmen?: Utilizing Performance Monitors for Compromising Keys of RSA on Intel Platforms. Springer Berlin Heidelberg, Berlin, Heidelberg, 248–266. DOI: https://doi.org/10.1007/978-3-662-48524-4_13

[7] Marco Chiappa, Eddy Savas, and Cemal Yilmaz. 2016. Real time detection of cache-based side-channel attacks using hardware performance counters. Applied Soft Computing 49 (2016), 1162 – 1174.

[8] John Demme, Matthew Maycock, Jared Schmitz, Adriang Tan, Adam Waksman, Simha Sethumadhavan, and Salvatore Stolfo. 2013. On the Feasibility of Online Malware Detection with Performance Counters. In Proceedings of the 40th Annual International Symposium on Computer Architecture (ISCA ’13). ACM, New York, NY, USA, 559–570.

[9] Fangfei Liu and Yuval Yarom and Qian Ge and Gernot Heiser and Ruby B. Lee. 2011. AES. In Constructive Side-Channel Analysis and Secure Design - 6th International Workshop, COSADE 2015, Berlin, Germany, April 13-14, 2015. Revised Selected Papers. 111–126. DOI: https://doi.org/10.1007/978-3-319-21476-4_8

[10] Mark Hall, Eibe Frank, Geoffrey Holmes, Bernhard Pfahringer, Peter Reutemann, and Ian H. Witten. 2009. The WEKA Data Mining Software: An Update. SIGKDD Explor. Newsl. 11, 1 (Nov. 2009), 10–18. DOI: https://doi.org/10.1145/1656274.1656278

[11] Mehmet Saninc Inci, Berk Gulmezoglu, Gorka Irazoqui, Thomas Eisenbarth, and Berk Sunar. 2016. Cache Attacks Enable Bulk Key Recovery on the Cloud. In Cryptographic Hardware and Embedded Systems – CHES 2016. 18th International Conference, Santa Barbara, CA, USA, August 17-19, 2016. Proceedings, Benedikt Gierlichs and Axel Y. Poschmann (Eds.).

[12] Gorka Irazoqui, Thomas Eisenbarth, and Berk Sunar. 2015. SBA: A Shared Cache Attack that Works Across Cores and Defies VM Sandboxing and its Application to AES. In 36th IEEE Symposium on Security and Privacy (S&P’15). 591–604.

[13] Gorka Irazoqui, Mehmet Saninc Inci, Thomas Eisenbarth, and Berk Sunar. 2015. Lucky 13 Strikes Back. In Proceedings of the 10th ACM Symposium on Information, Computer and Communications Security (ASIACCS ’15). ACM, New York, NY, USA, 85–96. DOI: https://doi.org/10.1145/2714576.2714625

[14] Taesoo Kim, Marcus Peinado, and Gloria Mainar-Ruiz. 2012. STEALTHMEM: System-Level Protection Against Cache-Based Side Channel Attacks in the Cloud. In Presented as part of the 21st USENIX Security Symposium (USENIX Security 12). USENIX, Bellevue, WA, 189–204. https://www.usenix.org/conference/usenixsecurity12/technical-sessions/presentation/kim

[15] Kenji Kira and Larry A. Rendell. 1992. The feature selection problem: Traditional methods and a new algorithm. In AIPN, Vol. 2. 129–134.

[16] Peng Li, Debin Gao, and Michael K. Reiter. 2014. Stopwatch: a cloud architecture for timing channel mitigation. ACM Transactions on Information and System Security (TISSEC) 17, 2 (2014), 8.

[17] militia, Leandro Rodrigues Lima, Andreas Zankl, Gorka Irazoqui, Johann Daniel Gruss, Clémentine Maurice, Klaus Wagner, and Stefan Mangard. 2016. ARMageddon: Cache Attacks on Mobile Devices. In 25th USENIX Security Symposium, USENIX Security 16, Austin, TX, USA, August 10-12, 2016. 549–564. https://www.usenix.org/conference/usenixsecurity16/technical-sessions/presentation/lipp

[18] H Liu. 2011. A Measurement Study of Server Utilization in Public Clouds. In 2011 IEEE Ninth International Conference on Dependable, Autonomic and Secure Computing. 435–442. DOI: https://doi.org/10.1109/DASC.2011.87

[19] Roy Longbottom. 2016. RandMem Benchmark. [Online; accessed 19-May-2017].

[20] Ramya Jayaram Masti, Devendra Rai, Aanjhan Ranganathan, Christian Müller, Lothar Thiele, and Srdjan Capkun. 2015. Thermal Covert Channels on Multi-core Platforms. In 24th USENIX Security Symposium (USENIX Security 15). USENIX Association, Washington, D.C., 865–880. https://www.usenix.org/conference/usenixsecurity15/technical-sessions/presentation/masti

[21] David McDonald. 1990. A casum procedure based on sequential ranks. Naval Research Logistics (NRL) 37, 5 (1990), 627–646. DOI: https://doi.org/10.1002/1097-0002(199010)37:5<627::AID-NAV3220370504>3.0.CO;2-F

[22] Philip J. Musci, Shirley Browne, Christine Deane, and George Ho. 1999. PAPI: A Portable Interface to Hardware Performance Counters. In In Proceedings of the Department of Defense HPCMP Users Group Conference. 7–10.

[23] Veronica Montes De Oca, Daniel R. Jeske, Qi Zhang, Charles Rendon, and Mazda Marvasti. 2010. A casum change-point detection algorithm for non-stationary sequences with application to data network surveillance. Journal of Systems and Software 83, 7 (2010), 1288 – 1297. DOI: https://doi.org/10.1016/j.jss.2010.02.006 [SPLC] 2008.

[24] Dag Arne Osvik, Adi Shamir, and Eran Tromer. 2006. Cache Attacks and Countermeasures: The Case of AES. In Topics in Cryptology – CT-RSA 2006: The Cryptographers’ Track at the RSA Conference 2006, San Jose, CA, USA, February 15–17, 2005. Proceedings, Springer Berlin Heidelberg, Berlin, Heidelberg, 1–20. DOI: https://doi.org/10.1007/11658058_1

[25] ES Page. 1954. Continuous inspection schemes. Biometrika 41, 1/2 (1954), 100–115.

[26] Mathias Payer. 2016. HexPADS: A Platform to Detect “Stealth” Attacks. In Engineering Secure Software and Systems: 8th International Symposium, ISSS 2016, London, UK, April 6–8, 2016. Proceedings, Juan Caballero, Eric Bodden, and Elias Athanasopoulos (Eds.). Springer International Publishing, Cham, 138–154.

[27] Colin Percival. 2006. Cache missing for fun and profit. In Proc. of BSDCan 2005.

[28] Yahoo research. 2010. Yahoo! Cloud System Benchmark (YCSB). https://github.com/brianfrankcooper/YCSB. (Online; accessed 19-May-2017).

[29] Thomas Ristenpart, Eran Tromer, Hovav Shacham, and Stefan Savage. 2009. Hey, you get off of my cloud: exploring information leakage in third-party compute clouds. In ACM Conference on Computer and Communications Security, CCS 2009, Chicago, Illinois, USA, November 9-13, 2009. 199–212. DOI: https://doi.org/10.1145/1653662.1653687

[30] Baljit Singh, Dmitry Evtyushkin, Jesse Elwell, Ryan Riley, and Biano Cervantes. 2017. On the Detection of Kernel-Level Rootkits Using Hardware Performance Counters. In Proceedings of the 2017 ACM on Asia Conference on Computer and Communications Security. ACM, 483–493.

[31] Adrian Tang, Simha Sethumadhavan, and Salvatore Stolfo. 2014. Unsupervised Anomaly-Based Malware Detection Using Hardware Features. In Research...
in Attacks, Intrusions and Defenses, Angelos Stavrou, Herbert Bos, and Georgios Portokalidis (Eds.). Lecture Notes in Computer Science, Vol. 8688. Springer International Publishing, 109–129.

[37] A. G. Tartakovsky, B. L. Rozovskii, R. B. Blazek, and Hongjoong Kim. 2006. A novel approach to detection of intrusions in computer networks via adaptive sequential and batch-sequential change-point detection methods. IEEE Transactions on Signal Processing 54, 9 (Sept 2006), 3372–3382. DOI: https://doi.org/10.1109/TSP.2006.879308

[38] Alexander G. Tartakovsky, Boris L. Rozovskii, Rudolf B. Blažek, and Hongjoong Kim. 2006. Detection of intrusions in information systems by sequential change-point methods. Statistical Methodology 3, 3 (2006), 252 – 293. DOI: https://doi.org/10.1016/j.stamet.2005.05.003

[39] Venkata Nathan Varadarajan, Thomas Ristenpart, and Michael Swift. 2014. Scheduler-based defenses against cross-VM side-channels. In 23rd USENIX Security Symposium (USENIX Security 14). USENIX Association, San Diego, CA, 687–702. https://www.usenix.org/conference/usenixsecurity14/technical-sessions/presentation/varadarajan

[40] X. Wang and R. Karri. 2013. NumiChecker: Detecting kernel control-flow modifying rootkits by using Hardware Performance Counters. In 2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC). 1–7.

[41] Zhenghong Wang and Ruby B. Lee. 2007. New cache designs for thwarting software cache-based side channel attacks. In 34th International Symposium on Computer Architecture (ISCA 2007), June 9–11, 2007, San Diego, California, USA, 494–505. DOI: https://doi.org/10.1145/1250662.1250723

[42] Yuval Yarom and Naomi Benger. 2014. Recovering OpenSSL ECDSA Nonces Using the FLUSH+RELOAD Cache Side-channel Attack. IACR Cryptology ePrint Archive 2014 (2014), 140.

[43] Yuval Yarom and Katrina Falkner. 2014. FLUSH+RELOAD: A High Resolution, Low Noise, L3 Cache Side-Channel Attack. In 23rd USENIX Security Symposium (USENIX Security 14). 719–732. https://www.usenix.org/conference/usenixsecurity14/technical-sessions/presentation/yarom

[44] Andreas Zankl, Johann Heyszl, and Georg Sigl. 2017. Automated Detection of Instruction Cache Leaks in Modular Exponentiation Software. In Smart Card Research and Advanced Applications: 15th International Conference, CARDIS 2016, Cannes, France, November 7–9, 2016, Revised Selected Papers, Kerstin Lemke-Baut and Michael Tunstall (Eds.). Springer International Publishing, Cham, 228–244. DOI: https://doi.org/10.1007/978-3-319-54669-8_14

[45] Tuan Wei Zhang, Yinqian Zhang, and Ruby B. Lee. 2016. CloudBadar: A Real-Time Side-Channel Attack Detection System in Clouds. Springer International Publishing, Cham, 118–140. DOI: https://doi.org/10.1007/978-3-319-45719-2_6

[46] Y. Zhang, A. Juels, A. Oprea, and M. K. Reiter. 2011. HomeAlone: Co-residency Detection in the Cloud via Side-Channel Analysis. In 2011 IEEE Symposium on Security and Privacy. 313–328. DOI: https://doi.org/10.1109/SP.2011.31

[47] Yinqian Zhang, Art Jueis, Michael K. Reiter, and Thomas Ristenpart. 2012. Cross-VM side channels and their use to extract private keys. In ACM Conference on Computer and Communications Security, CCS ’12, Raleigh, NC, USA, October 16-18, 2012. 305–316. DOI: https://doi.org/10.1145/2382196.2382200

[48] Yinqian Zhang, Art Jueis, Michael K. Reiter, and Thomas Ristenpart. 2014. Cross-Tenant Side-Channel Attacks in Paas Clouds. In Proceedings of the 2014 ACM SIGSAC Conference on Computer and Communications Security (CCS ’14). ACM, New York, NY, USA, 990–1003. DOI: https://doi.org/10.1145/2660267.2660356