Abstract: Neuromorphic engineering is a promising computing paradigm in next-generation information and communication technology. In particular, spiking neural networks are expected to reduce power consumption drastically owing to their event-driven operation. The spike-timing-dependent plasticity (STDP) rule, which learns from local spike-timing differences between spiking neurons, is a biologically plausible learning rule for spiking neural networks (SNNs). In this study, we designed and simulated an analog circuit that reproduces the multiplicative STDP rule, which is more flexible and adaptive to external signals. We also derived analytical expressions for the behavior of the proposed circuit. These results provide important insights for designing energy efficient neuromorphic devices for applications including edge computing.

Key Words: spike-timing-dependent plasticity, unsupervised learning, analog circuit, neuromorphic hardware, edge computing

1. Introduction
With the increasing demand for faster, safer, and more energy-efficient data processing, neuromorphic computing has attracted attention as a potential paradigm to support next-generation information and communication technology [1–3]. Hardware technology for the efficient implementation of artificial neural networks, particularly in the form of spiking neural networks (SNNs) [4–9], has also been studied intensively to decrease power consumption [10–19]. A central challenge in the development
of SNN hardware is the implementation of learning, or the tuning of synaptic connection strengths in response to training events, which is achieved mostly through software programming [3]. In contrast, biological neuronal networks autonomously adapt to external inputs and the environment through local interactions that plastically potentiate or depress the strength of individual synapses [6, 20–23].

The fundamental plasticity rule that governs weight tuning in biological neuronal networks is the spike-timing-dependent plasticity (STDP), which induces long-term potentiation or long-term depression depending on the time difference between pre-synaptic and post-synaptic spikes [24–27]. The STDP rule can be modeled in such a way that the amplitude of the weight update depends solely on the spike time difference (additive STDP) or in a way that depends on both the spike time difference and the current weight (multiplicative STDP). The multiplicative STDP is physiologically more plausible [24], and theoretical analysis has shown that it stabilizes synaptic dynamics and generates a unimodal, positively skewed distribution of weights [25]. A computational disadvantage of this multiplicative rule is that it makes obtaining input-specific weight distributions difficult [28]. To avoid this, a decay term can be introduced so that a value from the weight is constantly subtracted upon an activation of a post-neuron. Numerical simulations have shown that the decay term effectively prunes connections that do not undergo potentiation and enhances the performance of SNNs in image classification tasks [27].

The implementation of the STDP mechanism in CMOS neuromorphic circuits has been proposed by several groups [29–32] and has been reviewed in [33]. The circuit model and its prototype VLSI chip reported by Indiveri [29] is one of the earliest demonstrations of STDP in CMOS circuits. Despite the discrepancy in the precise shape of the STDP curve from physiology, in which the amount of weight change exponentially decays with spike time difference, the circuit model realized the STDP function with as few as 12 transistors. Subsequently, Bofill-i-Petit et al. [30] reported a CMOS circuit that reproduces the exponentially decaying and multiplicative STDP curve, although the number of transistors rose to 18. Unique circuit models that realized temporally symmetric and asymmetric STDP have been reported by Tanaka et al. [31]. More recently, Azghadi et al. [32] proposed a compact 15-transistor circuit for realizing an exponentially decaying STDP curve. The CMOS implementation of the exponentially decaying and multiplicative STDP with a constant decay term is desired using even fewer transistors, to realize a stable SNN system for applications such as edge computing.

This paper proposes an analog circuit that reproduces multiplicative STDP and decay, and reports the SPICE simulation results of its operation. In Section 2, in addition to the conventional STDP rule, an STDP rule considering weight dependence and decay is described. In Section 3, an analog circuit that reproduces the conventional STDP rule is described, and a circuit with weight dependence and decay is also discussed in terms of the STDP curve. Furthermore, an analytical derivation of the characteristics of the proposed analog circuit is presented. Finally, the conclusions are presented in Section 4.

2. STDP model

In the conventional (or additive) STDP rule, the synaptic weight \(w_{ij}\) between a pre-neuron \(i\) and a post-neuron \(j\) is updated as follows [24]:

\[
\Delta w_{ij} = \begin{cases} 
A_+ \exp(-|\Delta t|/\tau_+) & (\Delta t > 0), \\
-A_- \exp(-|\Delta t|/\tau_-) & (\Delta t < 0), 
\end{cases}
\]

\[
\Delta t = t_j - t_i, 
\]

where subscripts + and − represent the potentiation and depression of the synaptic weight, respectively. \(A\) is the amplitude of the weight change, and \(\tau\) is the time constant. The STDP rule with weight dependence and a constant decay is expressed as follows [27]:

\[
\Delta w_{ij} = \begin{cases} 
A_+ (w_{max} - w_{ij}(t)) \exp(-|\Delta t|/\tau_+) - A_{tar} & (\Delta t > 0), \\
-A_- (w_{ij}(t) - w_{min}) \exp(-|\Delta t|/\tau_-) - A_{tar} & (\Delta t < 0), 
\end{cases}
\]
where $w_{\text{max}}$ and $w_{\text{min}}$ represent the maximum and minimum values of $w_{ij}$, respectively. $A_{\text{tar}}$ is a constant target value that defines the decay amplitude.

Figure 1(a) shows the STDP curve. The black line represents the conventional STDP curve calculated using Eq. (1). The smaller the time difference $\Delta t$ between the spikes of the two neurons, the larger is the change in the weight value $\Delta w_{ij}$. This variation will decay in proportion to the exponent of $\Delta t$. If $\Delta t < 0$, the sign of the variation is reversed. The red line represents the STDP curve that considers the decay term. As the weight value always decays by $A_{\text{tar}}$ when an STDP event occurs, irrelevant connections are gradually pruned as learning progresses. Figures 1(b) and (c) show examples of timing diagrams based on the conventional STDP curve and the STDP curve that consider the decay term, respectively. $A_{\text{tar}}$ causes a decay of $w_{ij}$ in (c), even between spikes with large time differences that do not change in (b).

3. Results and discussion
3.1 STDP analog circuit
We designed an analog circuit for the hardware implementation of the proposed learning model based on the STDP circuit of a previous study [32], based on the correspondence with a low-power neuron circuit [18]. We first describe the operation of the additive STDP analog circuit with a reduced number of transistors using the TSMC 65 nm CMOS process, and verify the operation via SPICE simulation.

Figure 2(a) shows the proposed analog STDP circuit. In accordance with the circuit model proposed
by Azghadi et al. [32], the circuit consists of three main units. The depression unit generates a trace of post-synaptic spikes, $V_{dep}$. The potentiation unit generates a trace of pre-synaptic spikes, $V_{pot}$. The $\Delta t - V_W$ conversion unit detects the time difference between the spikes and calculates the voltage of the capacitor $C_W$, $V_W$, from the value of the trace $V_{dep}(t)$ or $V_{pot}(t)$ at time $t$. Here, $\Delta t = t_{post} - t_{pre}$ is the difference between the time $t_{pre}$, which is the timing of the pre-synaptic spike, and $t_{post}$, which is the timing of the post-synaptic spike. When $\Delta t < 0 (\Delta t > 0)$, $V_W$ is decreased (increased) by the depression (potentiation) circuit. The variation of $V_W$, $\Delta V_W$, corresponds to the change in the synaptic weight of the pre- and post-STDP operations.

Figure 2(b) shows the timing diagram of this circuit, in the weight-depression operation as an example. When the output spike $V_{post}$ of the post-synaptic neuron arrives at $t_{post}$, the transistor $M2$ is turned on, and the capacitor $C_{dep}$ is charged by the current source $I_{dep}$ for a duration of $\Delta t_p$. Then, the pre-synaptic spike $V_{pre}$ turns on $M6$ and the charge in the capacitor $C_W$ of the $\Delta t - V_W$ conversion unit is discharged, which depends on the potential of the capacitor $C_{dep}$ in the depression unit $V_{dep}$. $V_{dep}$ is linearly decayed by the drain current flowing through the transistor $M4$, which mirrors the current source $I_{td}$.

The circuit design of the potentiation unit is symmetric to the depression unit, and thus the weight-potentiation operation for $\Delta t > 0$ is performed based on the same mechanism as the weight-depression operation. When the output spike $\bar{V}_{pre}$ of the pre-synaptic neuron arrives at time $t_{pre}$, the transistor $M10$ is turned on, and the capacitor $C_{pot}$ is discharged by the current source $I_{pot}$ for a duration of $\Delta t_p$. Here, $\bar{V}_{pre}$ is inverted $V_{pre}$. After the $\bar{V}_{pre}$ pulse is turned off, $V_{pot}$ is linearly increased by the current flowing through the transistor $M9$, which depends on $I_{tp}$. The transistor $M7$ is then turned on by $\bar{V}_{post}$ (i.e., an inverted $V_{post}$), and the capacitor $C_W$ is charged with an amplitude that depends on $V_{pot}$.

The additive STDP circuit in [32] and the proposed STDP circuit were designed using the TSMC 65 nm CMOS process, and their operations were verified via SPICE simulation. The simulation conditions and STDP curves calculated from the STDP circuits are presented in Table I and Fig. 3, respectively. Both circuits reproduce the STDP characteristics with $\tau \sim 5 \mu$s. Although the number of transistors was reduced from the previous study, the proposed circuit reproduced almost the same STDP characteristics. Furthermore, the time constant of the STDP curve could be modulated by bias currents $I_{tp}$ and $I_{td}$.

### 3.2 Implementation of weight dependence and decay

Figure 4 shows the STDP circuit that includes the function of the weight dependence and decay expressed in Eq. (3). The circuit is based on the STDP circuit shown in Fig. 2(a). The decay term $A_{tar}$ is realized by the decay unit (highlighted in red), which consists of a current source $I_{tar}$ and a current mirror circuit. The post-synaptic spike $V_{post}$ turns on $M12$ and discharges the capacitor $C_W$ via $M13$. The amount of discharge is proportional to the product of the amplitude of the current

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**Table I.** Simulation conditions of the proposed circuit.

| parameter | value |
|-----------|-------|
| $V_{DD}$ [V] | 1.0 |
| $I_{dep}$ [nA] | 250 |
| $I_{pot}$ [nA] | 220 |
| $I_{tp}$ [nA] | 1, 3, 5 |
| $I_{td}$ [nA] | 1, 3, 5 |
| $C_W$ [fF] | 500 |
| $C_{dep}$, $C_{pot}$ [fF] | 100 |
| $\Delta t_p$ [ns] | 200 |
source $I_{tar}$ and the width of synaptic spikes, $\Delta t_p$.

The weight dependence circuit consists of a current mirror and a MOS transistor that controls the amount of current flowing in the current mirror. Assuming that the weight value can be referred to as a voltage $V_{W0}$, the amount of current in the current mirror is adjusted to realize the weight dependency by applying $V_{W0}$ to the gates of M1 and M21.

The STDP curve was evaluated by varying $V_{W0}$ to investigate the effect of weight dependence. Figure 5 shows the STDP curve of the proposed circuit with three conditions: $V_{W0} = 450, 500,$ and $550$ mV. The other experimental parameters are listed in Table II. The dashed line represents the theoretical value, which will be explained in detail in the following subsection. When the weight value is intermediate, i.e., $V_{W0} = 500$ mV, the STDP curve is positively and negatively symmetrical. When the weight value is greater than the intermediate value, i.e., $V_{W0} = 550$ mV, the amount of variation in potentiation is weakened, whereas that of depression is enhanced. When $V_{W0} = 450$ mV, the opposite change occurs.

Figure 6(a) shows the effect of the decay term. Here, only $I_{tar}$ was varied, the other parameters were set to be the same as those listed in Table II. $V_{W0}$ was set to 500 mV. The STDP curve shifted downwards in a linear proportion to the current $I_{tar}$. It was confirmed that the shape of the STDP curve was maintained for all $I_{tar}$. Figure 6(b) shows the relationship between $I_{tar}$ and $\Delta V_W$ at $\Delta t = −20 \mu s$ for different $V_{W0}$. The dashed lines represent the linear fit of each dataset. The slopes of the lines are $−0.3822, −0.3819,$ and $−0.3805$ mV/nA for $V_{W0} = 450, 500,$ and $550$ mV, respectively. Thus, the decay unit can control $\Delta V_W$ linearly, independent of the value of $V_{W0}$. The proposed configuration of the decay unit provided the expected linear characteristics.

We also estimated the power consumption of STDP operations with weight dependence and decay via SPICE simulation. The average power consumptions at the event frequency of 10 kHz were 0.748 and 0.775 $\mu$W at $I_{tar} = 0$ and 100 nA, respectively. From a practical application of the STDP circuit in edge devices, e.g., for an application in reservoir computing with $N_R$ reservoir neurons and $N_O$ output neurons, the total power consumption of STDP units sum up to be $N_R \times N_O \times 0.75 \mu$W. Assuming a network size of $N_R = 200$ and $N_O = 10$, a network size capable of classifying ten spoken digits [34], the power consumption is estimated to be 1.5 mW, a value of which is acceptable in edge devices.

Another concern for applications in edge devices is the chip area, which is primarily dominated by the area of the capacitors. Assuming a capacitance of $2 fF/\mu m^2$, the total area of 350 $\mu m^2$, and an additional wiring area of 20%, the total circuit area of the STDP unit is given by $350 \times 1.2 \times N_R \times N_O$. Therefore, for a reservoir network application with the abovementioned number of neurons, the total area amounts to be 0.84 mm$^2$, an area small enough for use in edge devices. Further reduction of the chip area requires the reduction of the area of the capacitors. Decreasing the area of the capacitor leads...
to a reduction in the amplitude of current required for charging the capacitor, which also contributes to reduction of power consumption. However, the holding time of $\Delta V_W$ is shortened due to the decrease in the maximum amount of charge in the capacitor, which requires fast readout of the weight change. Therefore, the size of the capacitor should be determined by considering the frequency at which the $V_W$ is readout.

### 3.3 Analytical modelling

Here, we derive the equation for $\Delta V_W$, which is the change in $V_W$ after the STDP operation, to understand the property of the proposed STDP circuit theoretically. The calculation of $\Delta V_W$ is divided into two parts: (1) the calculation of $V_{dep}$ after the charging operation of $C_{dep}$ when $M5$ opens, and (2) the calculation of the current $I_{stdp}(t)$ flowing through $M8$ when $M9$ opens.

We assume that the current $I_{M3}$ that flows through $M3$ is $I_{M3} \simeq I_{M2} = I_{M1}$, and $I_{M1}$ is controlled via the gate voltage of $M1$, $V_{W0}$. In our circuit configuration, $I_{M1}$ is almost linearly proportional to $V_{W0}$. The current $I_{dep}$ injected into $C_{dep}$ is $I_{dep}(t) = I_{M3} - I_{M4}$. As $M4$ is diode-connected, the current $I_{dep}(t)$ is expressed by the following equation:

$$I_{dep}(t) = I_{M3} - I_{0,M4} \exp \left( \frac{V_{dep}(t) - V_{th}}{\eta V_T} \right) \quad (V_{dep} < V_{th}),$$

where $I_0$ is the zero-bias current, $\eta$ is a slope factor that depends on the process, $V_{th}$ is the threshold voltage, and $V_T = k_B T/q$ is the thermal voltage at temperature $T$. We assume that $V_T \simeq 26 \text{ mV}$ at $T = 300 \text{ K}$. In the charging phase, $I_{td}$ was assumed to be zero because it was at least two orders of magnitude smaller than $I_{dep}(t)$. The value of $V_{dep}$ at the end of the charging phase, $V_{dep0}$, is expressed as follows:

$$V_{dep0} = V_{dep}(t_{post} + \Delta t_p) = \frac{1}{C_{dep}} \int_{t_{post}}^{t_{post} + \Delta t_p} I_{dep}(t) dt,$$

$$\Delta t_p [\text{ns}] \quad \begin{array}{c}
\lambda_1 \text{mV} \\
\lambda_2 \text{mV} \\
\lambda_3 \text{mV}
\end{array}
$$
where $\Delta t_p$ is the pulse width of the pre- or post-synaptic spike. Using Eq. (6), we can easily estimate the slope of $V_{\text{dep}}(t)$, which is equal to $-I_{\text{stdp}}/C_{\text{dep}}$. For example, when $I_{\text{stdp}} = 1 \text{nA}$ and $C_{\text{dep}} = 100 \text{ fF}$, $V_{\text{dep}}$ decays at a rate of $10 \mu\text{V/}\mu\text{s}$. Assuming that the on-resistance of M9 is negligible, the current $I_{\text{stdp}}(t)$ drawn from the capacitor $C_W$ when M9 is turned on is calculated as follows:

$$I_{\text{stdp}}(t) = I_{0\text{,M8}} \exp \left( \frac{V_{\text{dep}}(t) - V_{\text{th}}}{\eta V_T} \right).$$

Finally, $\Delta V_W$ is calculated as follows:

$$\Delta V_W \simeq \frac{1}{C_W} \int_{t_{\text{pre}}}^{t_{\text{pre}}+\Delta t_p} I_{\text{stdp}}(t) dt = \frac{I_{0\text{,M8}}}{C_W} \exp \left( \frac{V_{\text{dep}}(t_{\text{pre}}) - V_{\text{th}}}{\eta V_T} \right) \Delta t_p$$

$$= \frac{I_{0\text{,M8}}}{C_W} \exp \left( \frac{V_{\text{dep}} + I_{\text{stdp}}(\Delta t + \Delta t_p) - V_{\text{th}}}{\eta V_T} \right) \Delta t_p,$$

where we assume that $V_{\text{dep}}(t)$ is constant during $t_{\text{pre}} < t < t_{\text{pre}} + \Delta t_p$ because $\Delta t_p$ is sufficiently short. As the circuit structure is symmetrical, the same procedure can be used to derive the equation for potentiation. The values of $\Delta V_W$ calculated using the equations are shown in Fig. 5 with dashed lines. The results are consistent with the numerical values obtained from the SPICE simulations.

When $|V_{\text{dep0}} - V_{\text{th}}| \ll \eta V_T$, Eq. (8) can be further simplified as:

$$\Delta V_W \simeq \frac{I_{0\text{,M8}}}{C_W} \left( 1 + \frac{V_{\text{dep0}} - V_{\text{th}}}{\eta V_T} \right) \exp \left( \frac{I_{\text{stdp}}(\Delta t + \Delta t_p)}{C_{\text{dep}} \eta V_T} \right) \Delta t_p.\tag{9}$$

The equation indicates that $\Delta V_W$ varies linearly with $V_{W_0}$, and that the circuit approximates the weight dependence in Eq. (3).

### 3.4 Comparison with previous studies

The present STDP circuit model was designed based on the models proposed in [30] and [32]. The circuit model in the two previous works used identical configurations for the potentiation and depression units. This design is effective for use in synapses between neurons $i$ and $j$, which are bidirectionally connected because the potentiation and depression units in a single STDP circuit can be used for the modulation of both $w_{ij}$ and $w_{ji}$. However, this design comes at the cost of bearing an inverter circuit in the $\Delta t - V_W$ conversion unit, which consumes three transistors. For applications in unidirectionally coupled synapses, such as those present in connections between the reservoir and the output layer in reservoir computing models [35], bidirectionality need not be considered. In such cases, the STDP circuit can be further simplified, as shown in Fig. 2, where the number of transistors was reduced from 15 to 12. Although this reduction may appear minor, the approach is critical at the system level, as the number of synapses scales with $O(N_1 \times N_2)$, where $N_1$ and $N_2$ are the numbers of neurons in the first and second layers, respectively. Further reduction of the number of transistors can be achieved by replacing current sources $I_{\text{dep}}$ and $I_{\text{pot}}$ with voltage sources, which has been confirmed to be functional with additional SPICE simulations (data not shown).

In the present study, we added two functions to the classical STDP rule, that is, a constant decay and weight dependence. To the best of our knowledge, this study is the first to implement a constant decay unit in an analog STDP circuit, which has recently been shown to be effective in enhancing the performance of SNNs in classification tasks [27, 35]. We showed that this can simply be achieved by coupling a decay unit to the synapse element, $C_W$, which results in a linear control of the $\Delta V_W$ offset nearly independent of $V_{W_0}$. This linear controllability is important for the stable operation of the analog circuit, as it increases the predictability of the circuit response against parameter variations and improves the tractability of the circuit.

The weight-dependent tuning of the STDP curve has previously been implemented in the Bofill-i-Petit and Murray model [30]. In this model, the voltage $V_W$ of the capacitor $C_W$ was used as
the value for the synaptic weight, and four transistors were used to tune the value of $I_{pot}$ depending on the value of $V_W$. In contrast, we assumed that the synaptic weights were stored in an external non-volatile element. In such a case, the value of $V_{W0}$ can be used to tune the amplitude of the current source $I_{pot}$ and $I_{dep}$ directly. This allows the weight dependence function to be implemented without any increase in the number of transistors. When $V_{W0}$ is stored externally, e.g., in a non-volatile memory element, an additional circuit for converting $\Delta V_W$ to $V_{W0}$ is required. Since such circuit needs to be configured according to the specific characteristics of the memory element, the circuit was not implemented in the present model.

Finally, we confirmed that the STDP circuit can be designed and operated using a 65 nm CMOS process. This allows the circuit to be operated at a supply voltage of 1 V. This value is lower than the values used in previous studies, in which the circuits were designed using 0.6 $\mu$m [30] or 0.35 $\mu$m [32] processes, lowering the overall power consumption of the circuit. The use of a supply voltage of 1 V is also important from the perspective of designing mixed-signal circuits, as it enables the miniaturization of peripheral circuits. Energy efficiency and hardware efficiency are critical for the application of STDP circuits in edge computing devices.

4. Conclusions
We designed an analog circuit that reproduces the STDP rule to improve the efficiency of next-generation neuromorphic information processing systems, such as SNNs. The conventional STDP rule can be realized using 12 transistors. By operating transistors in the subthreshold region, the exponential decay of the biologically plausible STDP curve was reproduced. To increase the adaptability of the STDP learning, we studied the multiplicative STDP and decay term, and designed an analog circuit that reproduces these functions in hardware. Accordingly, 21 transistors were used to confirm the modulation of the STDP curve proportional to the weight and to reproduce the linear decay term. These findings will contribute to improve the energy efficiency of analog neuromorphic hardware.

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References
[1] S. Furber, “Large-scale neuromorphic computing systems,” Journal of Neural Engineering, vol. 13, no. 5, 051001, 2016.
[2] K. Roy, A. Jaiswal, and P. Panda, “Towards spike-based machine intelligence with neuromorphic computing,” Nature, vol. 575, no. 7784, pp. 607–617, 2019.
[3] H. Momose, T. Kaneko, and T. Asai, “Systems and circuits for AI chips and their trends,” Japanese Journal of Applied Physics, vol. 59, no. 5, 050502, 2020.
[4] Y. Katori, K. Sakamoto, N. Saito, J. Tanji, H. Mushiake, and K. Aihara, “Representational switching by dynamical reorganization of attractor structure in a network model of the prefrontal cortex,” PLoS Computational Biology, vol. 7, no. 11, e1002266, 2011.
[5] W. Nicola and C. Clopath, “Supervised learning in spiking neural networks with FORCE training,” Nature Communications, vol. 8, no. 1, pp. 1–15, 2017.
[6] G. Bellec, F. Scherr, A. Subramoney, E. Hajek, D. Salaj, R. Legenstein, and W. Maass, “A solution to the learning dilemma for recurrent networks of spiking neurons,” Nature Communications, vol. 11, no. 1, pp. 1–15, 2020.
[7] T. Sakaguchi and N. Wakamiya, “Consideration on liquid structure contributing to discrimination capability of liquid state machine,” NOLTA, vol. 11, no. 1, pp. 36–59, 2020.
[8] S. Moriya, H. Yamamoto, A. Hirano-Iwata, S. Kubota, and S. Sato, “Modular networks of spiking neurons for applications in time-series information processing,” NOLTA, vol. 11, no. 4, pp. 590–600, 2020.
[9] Y. Dai, H. Yamamoto, M. Sakuraba, and S. Sato, “Computational efficiency of a modular reservoir network for image recognition,” *Frontiers in Computational Neuroscience*, vol. 15, p. 1, 2021.

[10] S.B. Furber, F. Galluppi, S. Temple, and L.A. Plana, “The SpiNNaker project,” *Proceedings of the IEEE*, vol. 102, no. 5, pp. 652–665, 2014.

[11] F. Akopyan, J. Sawada, A. Cassidy, R. Alvarez-Icaza, J. Arthur, P. Merolla, N. Imam, Y. Nakamura, P. Datta, G.-J. Nam, et al., “TrueNorth: Design and tool flow of a 65 mW 1 million neuron programmable neurosynaptic chip,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 10, pp. 1537–1557, 2015.

[12] M. Davies, N. Srinivasa, T.-H. Lin, G. Chinya, Y. Cao, S.H. Choday, G. Dimou, P. Joshi, N. Imam, S. Jain, et al., “Loihi: A neuromorphic manycore processor with on-chip learning,” *IEEE Micro*, vol. 38, no. 1, pp. 82–99, 2018.

[13] A. Neckar, S. Fok, B.V. Benjamin, T.C. Stewart, N.N. Oza, A.R. Voelker, C. Eliasmith, R. Manohar, and K. Boahen, “Braindrop: A mixed-signal neuromorphic architecture with a dynamical systems-based programming model,” *Proceedings of the IEEE*, vol. 107, no. 1, pp. 144–164, 2018.

[14] B. Cramer, D. Stöckel, M. Kreft, M. Wibral, J. Schemmel, K. Meier, and V. Priesemann, “Control of criticality and computation in spiking neuromorphic networks with plasticity,” *Nature Communications*, vol. 11, no. 1, pp. 1–11, 2020.

[15] T. Kohno, J. Li, and K. Aihara, “Silicon neuronal networks towards brain-morphic computers,” *NOLTA*, vol. 5, no. 3, pp. 379–390, 2014.

[16] T. Kohno, M. Sekikawa, and K. Aihara, “A configurable qualitative-modeling-based silicon neuron circuit,” *NOLTA*, vol. 8, no. 1, pp. 25–37, 2017.

[17] S. Sato, H. Akima, K. Nakajima, and M. Sakuraba, “Izhikevich neuron circuit using stochastic logic,” *Electronics Letters*, vol. 50, no. 24, pp. 1795–1797, 2014.

[18] Y. Tamura, S. Moriya, T. Kato, M. Sakuraba, Y. Horio, and S. Sato, “An Izhikevich model neuron MOS circuit for low voltage operation,” in *International Conference on Artificial Neural Networks*, pp. 718–723, Springer, 2019.

[19] R. Hasani, G. Ferrari, H. Yamamoto, T. Tanii, and E. Prati, “Role of noise in spontaneous activity of networks of neurons on patterned silicon emulated by noise-activated CMOS neural nanoelectronic circuits.” (in press).

[20] Y. Katori, Y. Otsubo, M. Okada, and K. Aihara, “Stability analysis of associative memory network composed of stochastic neurons and dynamic synapses,” *Frontiers in Computational Neuroscience*, vol. 7, p. 6, 2013.

[21] G.M. Hoerzer, R. Legenstein, and W. Maass, “Emergence of complex computational structures from chaotic neural networks through reward-modulated Hebbian learning,” *Cerebral Cortex*, vol. 24, no. 3, pp. 677–690, 2014.

[22] J. Zierenberg, J. Wilting, and V. Priesemann, “Homeostatic plasticity and external input shape neural network dynamics,” *Physical Review X*, vol. 8, no. 3, 031018, 2018.

[23] D. Krotov and J.J. Hopfield, “Unsupervised learning by competing hidden units,” *Proceedings of the National Academy of Sciences*, vol. 116, no. 16, pp. 7723–7731, 2019.

[24] G.-q. Bi and M.-m. Poo, “Synaptic modifications in cultured hippocampal neurons: Dependence on spike timing, synaptic strength, and postsynaptic cell type,” *Journal of Neuroscience*, vol. 18, no. 24, pp. 10464–10472, 1998.

[25] M.C. van Rossum, G.Q. Bi, and G.G. Turrigiano, “Stable Hebbian learning from spike-timing-dependent plasticity,” *Journal of Neuroscience*, vol. 20, no. 23, pp. 8812–8821, 2000.

[26] T. Masquelier, R. Guyonneau, and S.J. Thorpe, “Competitive STDP-based spike pattern learning,” *Neural Computation*, vol. 21, no. 5, pp. 1259–1276, 2009.

[27] P.U. Diehl and M. Cook, “Unsupervised learning of digit recognition using spike-timing-dependent plasticity,” *Frontiers in Computational Neuroscience*, vol. 9, p. 99, 2015.

[28] J.-n. Teramae and T. Fukai, “Computational implications of lognormally distributed synaptic weights,” *Proceedings of the IEEE*, vol. 102, no. 4, pp. 500–512, 2014.
[29] G. Indiveri, “Neuromorphic bistable VLSI synapses with spike-timing-dependent plasticity,” in *Advances in Neural Information Processing Systems*, Citeseer, 2002.

[30] A. Bofill-i-Petit and A.F. Murray, “Synchrony detection and amplification by silicon neurons with STDP synapses,” *IEEE Transactions on Neural Networks*, vol. 15, no. 5, pp. 1296–1304, 2004.

[31] H. Tanaka, T. Morie, and K. Aihara, “A CMOS spiking neural network circuit with symmetric/asymmetric STDP function,” *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. 92, no. 7, pp. 1690–1698, 2009.

[32] M.R. Azghadi, S. Al-Sarawi, N. Iannella, and D. Abbott, “Efficient design of triplet based spike-timing dependent plasticity,” in *The 2012 International Joint Conference on Neural Networks (IJCNN)*, pp. 1–7, IEEE, 2012.

[33] M.R. Azghadi, N. Iannella, S.F. Al-Sarawi, G. Indiveri, and D. Abbott, “Spike-based synaptic plasticity in silicon: Design, implementation, application, and challenges,” *Proceedings of the IEEE*, vol. 102, no. 5, pp. 717–737, 2014.

[34] D. Verstraeten, B. Schrauwen, D. Stroobandt, and J. Van Campenhout, “Isolated word recognition with the liquid state machine: A case study,” *Information Processing Letters*, vol. 95, no. 6, pp. 521–528, 2005.

[35] T. Kato, S. Moriya, H. Yamamoto, M. Sakuraba, and S. Sato, “Unsupervised learning based on local interactions between reservoir and readout neurons,” in *IEICE Technical Report*, vol. NC2020-12, pp. 21–23, 2020.