Double gate operation of metal nanodot array based single electron device

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Multidot single-electron devices (SEDs) can enable new types of computing technologies, such as those that are reconfigurable and reservoir-computing. A self-assembled metal nanodot array film that is attached to multiple gates is a candidate for use in such SEDs for achieving high functionality. However, the single-electron properties of such a film have not yet been investigated in conjunction with optimally controlled multiple gates because of the structural complexity of incorporating many nanodots. In this study, Fe nanodot-array-based double-gate SEDs were fabricated by vacuum deposition, and their single-electron properties (modulated by the top- and bottom-gate voltages; $V_T$ and $V_B$, respectively) were investigated. The phase of the Coulomb blockade oscillation systematically shifted with $V_T$, indicating that the charge state of the single dot was controlled by both the gate voltages despite the metallic random multidot structure. This result demonstrates that the Coulomb blockade oscillation (originating from the dot in the multidot array) can be modulated by the two gates. The top and bottom gates affected the electronic state of the dot unevenly owing to the geometrical effect caused by the following: (1) vertically asymmetric dot shape and (2) variation of the dot size (including the surrounding dots). This is a characteristic feature of a nanodot array that uses self-assembled metal dots; for example, prepared by vacuum deposition. Such variations derived from a randomly distributed nanodot array will be useful in enhancing the functionality of multidot devices.

Recently, new types of computing technologies that use nanodot devices have been an active field of research; such as quantum1–4, reconfigurable5–7, and reservoir-computing8,9. A single-electron device (SED) can enable these technologies because of its high functionality and ultralow power consumption10–13. A SED exhibits a unique characteristic, known as the Coulomb blockade oscillation, with which the drain current ($I_D$) is periodically modulated by the gate voltage ($V_G$). This Coulomb blockade oscillation is caused by the charging effect of a nanodot (also known as the single-electron island) contained in the SED and is not observed in a conventional metal–oxide–semiconductor transistor. In previous studies, efforts were made to arrange a single dot between the SED electrodes, and the basic characteristics of the device14–18 were evaluated for applications associated with conventional logic circuits11,12,19–24. Using Si-based SEDs, the inverter operation20, half-sum and carry-out operation21, and multivalue memories22 have been demonstrated thus far.

Considering the single-nanodot SED known as the single-electron transistor (SET), which contains one nanodot between the source and drain electrodes, multiple SETs must be connected via wiring to form logic circuits. In this case, the one-by-one electron tunneling that occurs in SETs requires time for the wires to charge and the operation is slow. Additionally, the size variability of the nanodots induces the scattering of the SET characteristics. To overcome these difficulties, a nanodot-array-based SED that contains multiple nanodots without wiring was proposed, and its functionality was demonstrated under multigate operation25–27. For example, a flexible logic gate operation was enabled by using an Si nanodot array SED, indicating that nonuniform capacitive coupling between the dots and gate electrodes is a key factor for achieving logic operations26–27.

Besides nanodot fabrication methods that use lithography as reported in previous work, dispersion of chemically synthesized nanodots or self-assembled nanodot growth by thin-film deposition can be used to form nanodot array devices28–35. In these cases, the array comprises randomly distributed nanodots and numerous conduction paths with different properties must form. Although single-electron tunneling properties might be difficult to detect in such complex systems, Coulomb blockade properties are frequently detected29–30 and the modulation that is caused by the gate voltage is evident and straightforward in some cases31,33,37,38. To determine...
the potential of these complex array SEDs, further investigations using multigate operation are required. However, single-electron properties controlled by multiple gate voltages, which are important fundamentals for functional SEDs, have not been studied yet. In a randomly distributed nanodot array, nonuniform capacitive coupling between the dots and gate is expected due to the variation of the dot shape and size of the surrounding dots. In accordance with numerical simulations in Ref. 25, such variations of the gate capacitance are hypothesized to provide complex Coulomb blockade oscillations characteristics, which might enable a multidot SED to achieve logic operations.

In this study, an Fe nanodot single layer embedded in MgF₂ and sandwiched between two gate electrodes was used for SED fabrication; and modulation of \( I_D \) against the top- and back-gate voltages (\( V_T \) and \( V_B \), respectively) was systematically measured using SEDs with straightforward Coulomb blockade oscillation. It was demonstrated that the straightforward Coulomb blockade oscillations were controlled by \( V_T \) and \( V_B \), despite the metal and randomly distributed multidot structure. It was also found that the Coulomb blockade oscillations were unevenly responsive to both \( V_T \) and \( V_B \). These results indicate the application potential of a complex array SED in functional devices, including logic gates. The unevenness of the gate operations depends on the thickness of the gate insulators, the dot shape asymmetry (hemispheric rather than spheric), and the arrangement of the surrounding nanodots.

**Methods**

Figure 1 shows a schematic, and scanning electron microscopy images, of the fabricated Fe nanodot device. The source and drain electrodes (Au/Cr) with a gap length \( L \) of 50–400 nm were formed on a thermally oxidized SiO₂ (200 nm)/Si substrate. Afterward, an MgF₂ (45 nm)/Fe (film thickness \( t_{Fe} = 1.8–2.9 \text{ nm} \)) layer was formed between the electrodes at room temperature by using electron-beam deposition (base pressure < 10⁻⁷ Pa). In this \( t_{Fe} \) range, dispersed Fe nanodots were formed owing to surface migration and aggregation of Fe atoms on SiO₂. Finally, the gate-insulating SiO₂ (300 nm) layer was prepared on the MgF₂ layer via sputtering, followed by top-gate electrode (Au/Cr) formation. Details of the device fabrication were given in a previous study 37. The drain current between the source and drain electrodes (\( I_D \)) was measured using a semiconductor parameter analyzer (Agilent 4156C) by applying the voltages \( V_T \) and \( V_B \) to the Au/Cr top-gate and Si (substrate) back-gate electrodes, respectively, in a closed-cycle cryogenic probe station at a sample stage temperature \( T = 8 \text{ K} \).

**Results and discussion**

Almost all of the fabricated devices exhibited Coulomb blockade oscillations where highly reproducible back-and-forth \( I_D-V_B \) curves with the peak/valley ratio larger than ~ 1.1 were seen. About 95% of the fabricated devices were in this category. Some of them (ca. 10%) showed \( I_D-V_B \) oscillations that originated from a single dot as in our previous study 37. Typical current oscillation characteristics in this category are demonstrated in Fig. 2 as a function of \( V_B \) for two SEDs, termed Devices A and B in this report. The \( V_B \) value utilized here was sufficiently small such that the Coulomb blockade of the dot was not lifted. A brief discussion of \( I_D-V_D \) characteristics and
the charging energy of the dot can be seen in the supplementary information as well as our previous study. In both of the graphs shown in Fig. 2, three \(I_D-V_B\) curves at \(V_T = 1.8, 10,\) and \(20\) V are superposed. The observed oscillation curves are evident, and they originated from a single dot, as discussed in our previous study. The oscillation period was approximately 27 (Device A) or 37 V (Device B); corresponding to a back-gate capacitance \(C_B\) of 5.9 (Device A) or \(4.3 \times 10^{-3}\) aF (Device B), respectively. Device B has a smaller \(C_B\) compared with Device A, the dot that contributes the current oscillation in this device should be smaller than that of Device A.

In both devices, the current oscillations were added to the constant-background current components (\(\sim 520\) pA (Device A) and \(\sim 1.0\) nA (Device B)), which were attributable to the parallel conductive paths comprising the dots with the Coulomb blockade lifted. Such dots (attributable to the background current) are relatively large and/or exhibit higher tunneling conductance than the quantized value \((2e^2/h)\). By comparing the \(I_D-V_B\) curves with different \(V_T\), a systematic shift in the current peak was identified. With increasing \(V_T\), the peak ca. \(20\) V for Device A gradually shifted to \(14\) and \(3.3\) V (Fig. 2a). A similar tendency was evident for Device B (Fig. 2b), with a peak shift from \(22\) to \(16\) V, and then to \(9.3\) V. These peak shifts toward the negative \(V_B\) direction demonstrate that the current oscillation characteristics can be controlled by both the top and back gates, even in the metal multidot SED, where the change in the nanodot charging state by \(V_T\) can be compensated by \(V_B\) and vice versa.

To clearly understand the details of the peak shift as a function of the two gate voltages (i.e., \(V_T\) and \(V_B\)), a contour plot of the drain current was used. For this purpose, numerous \(I_D-V_B\) curves were measured using various \(V_T\) values from 0 to 30 V in 300-mV steps, where the \(V_B\) sweep was conducted in the sequences of 0–30, 30 to –30, and –30 to 0 V. The current oscillations were well-reproducible for the back-and-forth \(V_B\) sweeps. In addition, the current oscillations were stable over a few days against the peak shift due to the charge offset drift, similar to the findings of a previous study. Figure 3a and b show the data measured from \(V_B = 30\) to –30 V as two-dimensional (2D) contour maps of the drain current, corresponding to the stability diagrams of the device. The current peaks shown in bright contrast were systematically shifted. Thus, the phase of the current oscillation can be controlled by using \(V_T\) and \(V_B\). These contour maps were straightforward and periodic, as indicated by the yellow dotted lines, although there was an irregularity in Fig. 3b at \(V_B = 17\) V, which was caused by charge noise that might be attributable to the effect of satellite nanodots acting as single-electron traps. These characteristics

Figure 2. Current oscillations originating from a single dot measured as a function of the back-gate voltage \(V_B\) for the following: (a) Device A \((t_{Fe} = 2.4\) nm and \(L = 50\) nm) at drain voltage \(V_D = 20\) mV and (b) Device B \((t_{Fe} = 2.4\) nm and \(L = 400\) nm) at \(V_D = 5\) mV. The top-gate voltage \(V_T\) was constant at 1.8, 10, and 20 V.

Figure 3. Typical two-dimensional contour-line maps of drain current \(I_D\) as a function of \(V_B\) and \(V_T\). (a) Device A at \(V_D = 20\) mV and (b) Device B at \(V_D = 5\) mV. \(N\) is the number of electrons in a single dot.
confirm that the major current oscillation originated from a single dot. Controllability of the charge state of a single dot by a double-gate was confirmed despite the multidot structure. The results shown in Figs. 2 and 3 are well-known phenomena for multigate SETs with a single dot configuration. However, manifestation of such a phenomenon in metal nanodot arrays is unprecedented and important because of the corresponding suggestion that SEDs comprising randomly dispersed metal multi-dots can operate as, for example, two-input logic-gate devices. Via careful analysis of these data, characteristic features of the double-gate SED operation of the self-assembled nanodot system were clarified. For the devices investigated in this study, the top and back gates were capacitively coupled to the SED, and the current peak shift in accordance with the $V_B$ and $V_T$ follows Eq. (1):

$$C_B V_B + C_T V_T = \text{const},$$

where $C_B$ and $C_T$ are the capacitances between the single dot and back/top gates, respectively. When $V_T$ changes by $\Delta V_T$, the peak shift in the current oscillation ($\Delta V_B$) is given by Eq. (2):

$$\Delta V_B = -(C_T/C_B) \Delta V_T.$$  

Therefore, the gate capacitance ratio $C_B/C_T$ of the dot is $\Delta V_T/\Delta V_B$, which was evaluated using the slope of the observed current peak line in the contour map. Using Fig. 3a and b, the gate capacitance ratio $C_B/C_T$ between the single dot and back/top gates was $\sim 1.2$ (Device A) or $\sim 2.0$ (Device B). Therefore, using the $C_B$ previously described, $C_T$ was $\sim 4.9$ (Device A) or $\sim 2.2 \times 10^{-3}$ aF (Device B). Table 1 and Fig. 4 show these results along with data from two other devices. For the device structure investigated in this study, the back-gate insulator comprised 200-nm-thick SiO$_2$ and the top-gate insulator comprised 45-nm-thick MgF$_2$ and 300-nm-thick SiO$_2$. Assuming a parallel-plate capacitor structure and known bulk dielectric constants (3.8 for SiO$_2$ and 5.2 for MgF$_2$), the capacitance ratio $C_B/C_T$ was $\sim 1.7$ (Fig. 4). For a total set of devices, the evaluated $C_B/C_T$ followed this relationship. Furthermore, each $C_B/C_T$ ratio was between 1.2 and 2.7, indicating a clear discrepancy from this straightforward estimation by using the parallel-plane model ($\sim 1.7$). This discrepancy was not caused by measurement and/or estimation errors, but was an important characteristic of the self-assembled dot array. In the following paragraphs, this is discussed by using a simplified model.

| Device | $C_B/C_T$ | $C_B$ (10$^{-3}$ aF) | $C_T$ (10$^{-3}$ aF) |
|--------|-----------|----------------------|--------------------|
| A      | 1.2 ± 0.2 | 5.9 ± 0.6            | 4.9 ± 0.5          |
| B      | 2.0 ± 0.4 | 4.3 ± 0.3            | 2.2 ± 0.1          |
| C      | 1.5 ± 0.2 | 10 ± 0.4             | 6.7 ± 0.3          |
| D      | 2.7 ± 0.8 | 9.4 ± 0.9            | 3.5 ± 0.3          |

Table 1. Averaged values of $C_B/C_T$, $C_B$, and $C_T$ for four devices. $C_B/C_T$ and $C_B$ contains the reading error of the slope and period of the current peak line, respectively. $C_T$ was evaluated by using the values of $C_B/C_T$ and $C_B$.
The nanodot array SED comprised numerous dots with various sizes. Because dots were formed on the substrate plane, the planar arrangement of hemispheric nanodots can be assumed as a model for this discussion. In addition, for straightforward calculations, the model was simplified into parallel-arranged, half-columnar dots with an infinitive axis length. Here, a numerical fit to the experimental data is not the purpose of this simulation. Figure 5 shows an example of the cross-sectional schematic, where the column axis of the dot is perpendicular to the paper surface. The dot is half-circular in this diagram (gray), termed the half-circular dot in the following discussion. By adopting this model, only 2D electric field calculations were required, with few parameters. A compact software (EStat provided by Advanced Science Laboratory, Inc.) based on the finite-element method (with an optimized mesh size) was used to solve the Laplace equations for the following: (1) simulating the electric field and (2) evaluating the capacitances (per unit length along the column axis) between the dot and top/back-gate electrodes. Although the model was simplified, the simulation results provided the intrinsic features of the nanodot array. In the next paragraph, the simulation results are explained with details of the model.

Figure 5 shows a typical model for evaluation. Notably, the horizontal and vertical magnifications of this diagram are different from each other. The in-plane diameter of a metallic half-circular dot is 30, 20, or 14 nm; termed \( L \) (large), \( M \) (medium), or \( S \) (small), respectively, throughout this report. The dots were arranged horizontally to form a dot array. In Fig. 5, the dot arrangement is termed LSL in the central part and \( M \) in other regions. The distance between the adjacent dot edges was maintained at 10 nm. The dots were sandwiched between two 100-nm-thick SiO\(_2\) layers acting as the top- and back-gate insulators. On the surface of these SiO\(_2\) layers, two metallic gates (gray) were attached. For simulations, one of the gate electrodes was biased by 1 V, whereas the dots and another electrode were grounded. Figure 5 shows simulated potential distributions as color maps; the electric force lines are represented by white lines. As described next, a remarkable difference was observed between Fig. 5a for voltage application to the back gate and Fig. 5b for voltage application to the top gate. The electric force lines shown in Fig. 5a were almost parallel, similar to those in a parallel capacitor, except near the dot edges. Thus, \( C_0 \) of each dot must be almost proportional to the dot size. Conversely, in Fig. 5b, the electric force lines were strongly curved and those near the central \( S \) dot were attracted by the adjacent \( L \) dots. Some of the electric force lines were absorbed by the \( L \) dots; therefore, \( C_T \) of the central \( S \) dot became smaller in this dot arrangement, whereas \( C_T \) of the \( L \) dot became larger. This is because of the geometrical difference between the upper (roundish) and lower (flat) dot surfaces. A dot shape on the nanometer scale can modulate the electric field, changing the charge distribution on the dot surface and the capacitance with the gate electrode. This suggests that the Coulomb blockade oscillation characteristics in a multidot SED comprising a complex dot array can be modulated by the shape and distribution of the dots, including the surrounding dots.

These simulations were performed for various dot arrangements, and the gate capacitance ratios \( C_B/C_T \) of the central dots were evaluated. Figure 6 shows examples of the SSS, MSM, and LSL arrangements. To check the applicability of the calculations, simulation results of circular dots with the same arrangements were superposed in the graph. Because the dots were symmetric in this case, the \( C_B/C_T \) ratio should be 1.0 in all the cases, reflecting the thickness ratio of the top (100-nm-thick) and bottom (100-nm-thick) insulating layers. The simulation results fit well with this value (the error with the theoretical value was ca. 0.1%). This indicates that the simulation was performed with a sufficient accuracy (number of meshes) to evaluate the \( C_B/C_T \). Considering half-circular dots, the \( C_B/C_T \) value indicates a large change from 0.95 to 1.27, depending on the adjacent dot size. This is because of the nonuniform distribution of the electric field between the top and bottom gates, which was attributable to the geometrical shape effect of the central dot and surrounding dots (Fig. 5) as well as the vertical asymmetric structure of the dots. In the SSS arrangement, for example, the roundish shape of the surface that was facing the top gate gathered the electric force lines, rather than the flat surface that was facing the bottom electrode. Therefore, \( C_T \) became larger than \( C_0 \) and \( C_B/C_T \) was < 1. For the large adjacent dot, as in the MSM arrangement, some electric force lines were attracted by the \( M \) dots, decreasing the \( C_T \) value; ultimately resulting in \( C_B/C_T > 1 \).
Lager adjacent dots in LSL strongly attracted the electric force lines from the S dot, and the deviation of $C_B/C_T$ from 1 became large. Similar results were also identified for M or L as the central dot. Such fundamental discussions by using 2D simulations must also be valid for a three-dimensional dot shape and arrangement. The shape asymmetry of the dots and its positional arrangement resulted in a variation of the $C_B/C_T$ (and thus the device properties) during double-gate operation.

Conclusion
A double-gate, Fe nanodot-array-based SED comprising an SiO$_2$–Fe–MgF$_2$ system was fabricated by using vacuum deposition, and its electric characteristics were investigated. The fabricated Fe nanodot device exhibited current oscillations that originated from a single dot\(^37\). The charge state of a single dot was controlled by both the top and back gates, even in the multidot structure. This result demonstrates that Coulomb blockade oscillation characteristics that originate from a dot in randomly dispersed multidots can be modulated by two gates. Additionally, the variation of the gate capacitance ratio $C_B/C_T$ (derived from the randomly distributed and vertically asymmetric nanodot array) was demonstrated. This phenomenon might provide a complex response to the input (gate) voltage. It might be useful to produce flexible logic gates as indicated in previous reports\(^25–27\), although further comprehensive studies are required in the future. The on/off ratio of the Coulomb blockade oscillations was small because of the many conduction paths that provided the background current. Although this problem is unavoidable in multidot SEDs, the on/off ratio can be improved by using a cascode MOSFET\(^22,26,46\). The findings of this study will facilitate new applications of metal nanodot arrays.

Data availability
The data that support the findings of this study are available from the corresponding author upon reasonable request.

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References
1. Veldhorst, M. et al. An addressable quantum dot qubit with fault-tolerant control-fidelity. Nat. Nanotechnol. 9, 981 (2014).
2. Maurand, R. et al. A CMOS silicon spin qubit. Nat. Commun. 7, 13575 (2016).
3. Watson, T. F. et al. A programmable two-qubit quantum processor in silicon. Nature 555, 633 (2018).
4. Yoneuda, J. et al. Quantum non-demolition readout of an electron spin in silicon. Nat. Commun. 11, 1144 (2020).
5. Bose, S. K. et al. Evolution of a designless nanoparticle network into reconfigurable Boolean logic. Nat. Nanotechnol. 10, 1048 (2015).
6. Chen, T. et al. Classification with a disordered dopant-atom network in silicon. Nature 577, 341 (2020).
7. Ruiz Euler, H. C. et al. A deep-learning approach to realizing functionality in nanoelectronic devices. Nat. Nanotechnol. 15, 992 (2020).
8. Oya, T. Feasibility and advantage of reservoir computing on single-electron devices. Ipn. J. Appl. Phys. 59, 040602 (2020).
9. Ueno, M. & Oya, T. Design of a single-electron neural network circuit controlling weights for reservoir computing. Ipn. J. Appl. Phys. 60, SCCE02 (2021).
10. Kastner, M. A. The single-electron transistor. Rev. Mod. Phys. 64, 849 (1992).
11. Likharev, K. K. Single-electron devices and their applications. Proc. IEEE 87, 606 (1999).
12. Takahashi, Y., Ono, Y., Fujiwara, A. & Inokawa, H. Silicon single-electron devices. J. Phys. Condens. Matter 14, 995 (2002).
13. Cotofana, S., Lagedew, C. & Vassiliadis, S. Addition related arithmetic operations via controlled transport of charge. IEEE Trans. Comput. 54, 243 (2005).
14. Nakamura, Y., Chen, C. & Tsai, J.-S. 100-K operation of Al-based single-electron transistors. Ipn. J. Appl. Phys. 235, 1465 (1996).
Kobayashi, K., Aikawa, H., Sano, A., Katsumoto, S. & Iye, Y. Fano resonance in a quantum wire with a side-coupled quantum dot. *Phys. Rev. B* **87**, 035319 (2003).

17. Okabayashi, N. et al. Uniform charging energy of single-electron transistors by using size-controlled Au nanoparticles. *Appl. Phys. Lett.* **100**, 033101 (2012).

18. Makarenko, K. S. et al. Bottom-up single-electron transistors. *Adv. Mater.* **29**, 1702920 (2017).

19. Tucker, J. R. Complementary digital logic based on the “Coulomb blockade”. *J. Appl. Phys.* **72**, 4399 (1992).

20. Ono, Y. et al. Si complementary single-electron inverter with voltage gain. *Appl. Phys. Lett.* **76**, 3121 (2000).

21. Ono, Y. et al. Single-electron and quantum silicon SOI devices. *Microelectron. Eng.* **59**, 435 (2001).

22. Inokawa, H., Fujiwara, A. & Takahashi, Y. Multiphase negative-differential-resistance device by combining single-electron and metal–oxide–semiconductor transistors. *Appl. Phys. Lett.* **79**, 3618 (2001).

23. Ono, Y., Inokawa, H. & Takahashi, Y. Binary adders of multigate single-electron transistors: Specific design using pass-transistor logic. *IEEE Trans. Nanotechnol.* **1**, 93 (2002).

24. Mahapatra, S., Vaish, V., Wasshuber, C., Banerjee, K. & Ionescu, A. M. Analytical modeling of single electron transistor for hybrid CMOS-SET analog IC design. *IEEE Trans. Electron Devices* **51**, 1772 (2004).

25. Kaizawa, T. et al. Multifunctional device using nanodot array. *Ipn. J. Appl. Phys.* **45**, 5317 (2006).

26. Kaizawa, T., Oya, T., Arita, M., Takahashi, Y. & Choi, J.-B. Single-electron device with Si nanodot array and multiple input gates. *IEEE Trans. Nanotechnol.* **8**, 533 (2009).

27. Jo, M. et al. Effect of arrangement of input gates on logic switching characteristics of nanodot array device. *IEICE Trans. Electron.* **E95-C**, 865 (2012).

28. Kim, S. J. et al. One electron-based smallest flexible logic cell. *Appl. Phys. Lett.* **101**, 183101 (2012).

29. Han, X., Shinohara, M., Yoshikawa, N. & Sugahara, M. Observation of single-electron charging effect in BaSrCaCuO granular thin films. *Ipn. J. Appl. Phys.* **32**, 1516 (1993).

30. Ralph, D. C., Black, C. T. & Tinkham, M. Spectroscopic measurements of discrete electronic states in single metal particles. *Phys. Rev. Lett.* **74**, 3241 (1995).

31. Takahashi, Y., Arita, M. & Takahashi, Y. Binary adders of multigate single-electron transistors. *Jpn. J. Appl. Phys.* **91**, 7038 (2002).

32. Willing, S., Lehmann, H., Volkmann, M. & Klinke, C. Metal nanoparticle film-based room temperature Coulomb transistor. *Sci. Adv.* **3**, e1603191 (2017).

33. Bitton, O., Gutman, D. B., Berkovits, R. & Frydman, A. Multiple periodicity in a nanoparticle-based single-electron transistor. *Nat. Commun.* **8**, 402 (2017).

34. Mizugaki, Y. et al. One-dimensional array of small tunnel junctions fabricated using 30-nm-diameter gold nanoparticles placed in a 140-nm-wide resist groove. *Ipn. J. Appl. Phys.* **57**, 098006 (2018).

35. Iwata, Y., Nishimura, T., Singh, A., Satoh, H. & Inokawa, H. High-frequency rectifying characteristics of metallic single-electron transistor with niobium nanodots. *Ipn. J. Appl. Phys.* **61**, SC1063 (2021).

36. Hosoya, H. et al. Single-electron transistor properties of Fe–SrF2 granular films. *Material. Sci. Eng. B* **147**, 100 (2008).

37. Gyakushi, T., Asai, Y., Tsurumaki-Pukuchi, A., Arita, M. & Takahashi, Y. Periodic Coulomb blockade oscillations observed in single-layered Fe nanodot array. *Thin Solid Films* **704**, 138012 (2020).

38. Gyakushi, T. et al. Charge-offset stability of single-electron devices based on single-layered Fe nanodot array. *AIP Adv.* **11**, 035230 (2021).

39. Takahashi, Y., Fujiwara, A., Yamazaki, K., Namatsu, H. & Murase, K. Multigate single-electron transistors and their application to an exclusive-OR gate. *Appl. Phys. Lett.* **76**, 637 (2000).

40. Macaia, K. et al. Logic operations of chemically assembled single-electron transistor. *ACS Nano* **6**, 2792 (2012).

41. Lai, N. S. et al. Pauli spin blockade in a highly tunable silicon double quantum dot. *Sci. Rep.* **1**, 110 (2011).

42. Uchida, T., Arita, M., Fujiwara, A. & Takahashi, Y. Coupling capacitance between double quantum dots tunable by the number of electrons in Si quantum dots. *J. Appl. Phys.* **117**, 084316 (2015).

43. Uchida, T. et al. Fabrication and evaluation of series-triple quantum dots by thermal oxidation of silicon nanowire. *AIP Adv.* **5**, 117144 (2015).

44. Koch, M. et al. Spin read-out in atomic qubits in an all-epitaxial three-dimensional transistor. *Nat. Nanotechnol.* **14**, 137 (2019).

45. Fontanella, J., Andeen, C. & Schuele, D. Low-frequency dielectric constants of α-quartz, sapphire, MgF$_2$, and MgO. *J. Appl. Phys.* **145**, 2852 (1974).

46. Inokawa, H., Fujiwara, A. & Takahashi, Y. A merged single-electron transistor and metal–oxide–semiconductor transistor logic for interface and multiple-valued functions. *Ipn. J. Appl. Phys.* **41**, 2566 (2002).
