Time-Dependent Dielectric Breakdown under AC Stress in GaN MIS-HEMTs

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Abstract—We investigate time-dependent dielectric breakdown (TDBB) in AlGaN/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistors (MIS-HEMTs) under forward bias AC stress which better emulates real-world operational conditions. To this end, we have performed TDBB experiments across a wide range of frequencies, temperatures, and recovery voltage levels. We find that TDBB under AC stress shows longer breakdown times than under DC stress and that this increase is more prominent with higher frequency, lower temperature, and more negative recovery voltage. We hypothesize that this is due to the dynamics of the gate stack in GaN MIS-HEMTs biased with a high positive gate voltage. Under these conditions, a second electron channel forms at the dielectric/AlGaN interface. This process is relatively slow as these electrons come from the 2DEG at the AlGaN/GaN interface and must overcome the energy barrier presented by the AlGaN. At the same gate voltage then, the electric field across the gate oxide is lower in magnitude under AC stress at high enough frequency than under DC stress explaining the obtained results.

Keywords—dielectric reliability, TDBB, GaN, MIS-HEMT, AC Stress, power electronics

I. INTRODUCTION

GaN has emerged as a promising next generation candidate for high performance energy efficient electronics. In particular, the GaN Metal-Insulator-Semiconductor High Electron Mobility Transistor (MIS-HEMT) has recently been identified as a promising candidate for high-voltage and high-power applications due to high current drive while minimizing gate leakage. However, reliability concerns with this device type are hampering its widespread commercial deployment [1],[2].

A key reliability issue is time-dependent dielectric breakdown (TDBB) where prolonged electrical stress leads to catastrophic breakdown of the gate dielectric. There has recently been great progress in understanding TDBB in GaN FETS. Like in Si, TDBB in GaN has been shown to follow Weibull statistics and electric field scaling [3],[4]. In addition, it has also been shown that the percolation model, where TDBB is thought to happen when a conduction path is formed by an overlapping of defects generated at random in the dielectric, applies to the GaN MIS-HEMT system [5]. Furthermore, trapping has been shown to have profound effect on TDBB, particularly in the OFF-state [6].

Much of the work to date has been done under constant voltage stress conditions, mostly due to ease of instrumentation. Yet, power transistor operation typically involves rapid switching between an ON-state and an OFF-state. It is then imperative to characterize and understand TDBB under high frequency switching conditions. In fact, studies in Si MOS systems show improvements in time to breakdown under AC stress conditions [7],[8],[9], suggesting the intriguing possibility of similar enhanced reliability for GaN devices. Furthermore, as trapping is very prominent in GaN, understanding the impact of switching on TDBB is particularly important.

In this work, we investigate the impact of AC stress on GaN MIS-HEMT TDBB. We have performed experiments involving different frequencies, stress temperatures, and recovery voltage levels. We find that time-to-breakdown is enhanced under high frequency AC operation. We hypothesize a physical reason for this effect that is unique to the GaN MIS-HEMT system.

II. EXPERIMENTAL

The devices under study are industrially prototyped depletion-mode AlGaN/GaN MIS-HEMTs grown on Si substrate. Previous DC stress studies on these devices revealed a gate insulator breakdown behavior consistent with TDBB in both forward bias ($V_{GS,Stress} > 0$, $V_{DS} = 0$ V) and reverse bias ($V_{GS,Stress} < 0$, $V_{DS} > 0$ and large) [3],[5],[6].

In this work, we study TDBB under AC stress conditions in which the gate cycles between a forward voltage stress value and a recovery voltage value in a square wave fashion. For the stress portion we investigate $V_{GS,Stress} = 8.5$ V. For the recovery portion, the gate voltage is reduced to either $V_{GS,Recovery} = 0$ V (“unipolar”) or -8.5 V (“bipolar”). The drain and source are grounded across the entire experiment while the body is left floating. AC stress frequencies of 1 Hz, 1 kHz, 10 kHz, and 100 kHz are studied. All measurements are performed by Keysight B1500A Semiconductor Device Parameter Analyzer equipped with B1525 Pulse Generator Unit. The measurements are performed at -60, 25, and 200 °C. The duty cycle is fixed at 45%. To allow direct comparison with stress under DC, all AC stress times reported here refer to the aggregate time for which $V_{GS}=V_{GS,Stress}$.

Each die on the wafer contains 40 identical devices with gate width of 1 mm. As TDBB is a stochastic process, a large sample size at each stress condition is required for obtaining meaningful statistics. Here, at least 32 devices per each stress...
conditions were measured. To evaluate the impact of AC stress on TDBD under one set of conditions, DC stress experiments under identical conditions were performed as reference. A complication in studies of this kind is the unavoidable die-to-die variations present in an exploratory device technology. We have attempted to minimize their impact by performing the AC stress and the reference DC stress experiments on devices that are interspersed through the same set of dies. In total, 1200 devices were characterized as part of this study.

III. RESULTS

Fig. 1 shows a comparison of gate leakage current ($I_g$) during typical DC and 1 Hz AC TDBD experiments with $V_{GS,Recovery} = -8.5 \ \text{V}$ at the three temperatures. There are minimum differences between AC and DC stress experiments. In all cases, $I_g$ exhibits a slight initial drop due to trapping, followed by an increase known as stress-induced-leakage-current (SILC) [10]. Sharp jumps in the gate leakage current at the end of the experiment indicate dielectric hard breakdown. The role of temperature is also similar under AC and DC stress. As $T$ increases, $I_g$ increases as expected and the time to breakdown decreases [3].

![Figure 1](image1.png)

Weibull plots of the time to hard breakdown ($t_{HBD}$) for TDBD experiments at room temperature under DC and AC conditions with $V_{GS,Recovery} = -8.5 \ \text{V}$ for all the studied frequencies are plotted in fig. 2. In all cases, well-behaved Weibull statistics are demonstrated. We observe a clear increase in $t_{HBD}$ under AC with respect to DC conditions as the AC frequency increases beyond 1 kHz. Despite this shift, the nearly parallel Weibull statistics suggest the same underlying degradation mechanism under both conditions, most likely through the formation of a conduction path via defects that is known as the percolation model [11].

In Fig. 2, it is interesting to see how the DC reference data (red data points) which in all four panels is obtained under identical conditions differ to some extent from panel to panel. This reflects the underlying die-to-die variations that are present on the wafer. Note, however, that in spite of this, a clear behavior for AC vs. DC stress emerges from the study. This validates our protocols for device selection and for appropriate reference data.

The impact of temperature and frequency is shown in Figs. 3 and 4. Fig. 3 shows the impact of AC frequency on TDBD statistics at -60 °C. For all pairs of conditions, AC vs. DC, the distribution statistics are again consistently parallel, reinforcing that the same degradation mechanism prevails, albeit with

![Figure 2](image2.png)

![Figure 3](image3.png)
shifting $t_{\text{HBD}}$. At -60 °C, an enhancement in $t_{\text{HBD}}$ is observed all the way down to 1 Hz. On the other hand, Fig. 4 shows that no significant AC/DC difference appears at 200 °C throughout the entire frequency range.

Fig. 5 plots the TDDB distributions at room temperature (25 °C) and at 200 °C under DC stress versus AC stress with $V_{\text{GS,Recovery}} = 0$ V. Again, at room temperature, a frequency dependence of TDDB is shown. As before, as the frequency increases, TDDB under AC stress is shown to shift rightward compared to TDDB under DC stress. However, the shifts appear smaller than under identical bipolar stress conditions. At 200 °C, the AC breakdown distribution again shows no significant shift or difference compared to DC conditions.

IV. ACCELERATION PARAMETER

To extract a pattern from these large data sets, we define an acceleration parameter, $\alpha$, as

$$\alpha = \frac{t_{63,\text{AC}}}{t_{63,\text{DC}}} \quad (1)$$

where $t_{63,\text{AC}}$ and $t_{63,\text{DC}}$ are $t_{\text{HBD}}$ for which the value of the y-axis of the Weibull distribution plot is equal to 0 for AC and DC, respectively. $t_{63}$ corresponds to a 63% cumulative probability of breakdown and represents a typical time to failure for the population of devices. A ratio is taken for the acceleration parameter to allow for comparisons among different stress conditions.

Fig. 6 plots $\alpha$ versus AC stress frequency for $V_{\text{GS,Recovery}} = -8.5$ V at each temperature. At room temperature (black solid circles) and for low frequency, there is very little difference in TDDB between AC and DC stress. However, as the frequency increases, TDDB under AC begins to show average longer breakdown times than under DC stress with $\alpha$ reaching a factor of about 2.5 at 100 kHz. This represents a considerable improvement in breakdown time under AC stress compared to DC.
Increasing the temperature to 200 °C (solid red circles) results in a considerably different behavior. Across all frequencies, there is a much smaller change in TDBB between AC and DC as compared to room temperature. Furthermore, there is small frequency dependence.

Decreasing the temperature to -60 °C (solid blue circles) on the other hand again reveals a strong frequency dependence with larger enhancements than at RT. These enhancements extend all the way down to 1 Hz.

Fig. 7 plots α versus AC stress frequency for VGS,Recovery = 0 V and VGS,Recovery = -8.5 V at room temperature (25 °C) and 200 °C. TDDB shift under AC stress again shows frequency dependence for VGS,Recovery = 0 V at RT. However, at all frequencies, unipolar stress (VGS,Recovery = 0 V) results in a smaller α as compared to bipolar stress. At 200 °C, α is small at all frequencies with no discernible difference in bipolar vs. unipolar stress.

V. DISCUSSION

Our key finding in this work, that under high frequency AC stress the time to breakdown for the gate dielectric is enhanced when compared with DC stress, is important from a practical point of view. It suggests that the conventional dielectric lifetime extrapolation approach might be conservative, causing device designers to make unnecessary tradeoffs in performance.

Our findings are also intriguing from a device physics perspective. For Si n-MOSFETs with SiO2 dielectric, TDDB under bipolar AC conditions has been shown to result in longer breakdown times compared to DC or unipolar AC conditions [8]. The origin of this is believed to be hole detrapping near the gate when the gate bias is relaxed. Furthermore, even in high-κ dielectric/metal gate Si FETs, holes in the oxide are thought to be the reason behind the frequency dependence of TDBB [7].

The role of hole trapping in GaN MIS-HEMTs is improbable. With a wide bandgap and under forward gate voltage conditions, a negligible concentration of holes is expected across the structure. Instead, we focus on the so-called spillover effect of GaN MIS-HEMTs under positive gate bias [12]. To understand this, refer to the energy band diagrams of Fig. 8. For positive VG stress under DC conditions, the Fermi level is flat across the semiconductor, the edge of the conduction band at the AlGaN/dielectric interface is close to the Fermi level and an inversion layer of electrons appears at that location (Fig. 8, left). Evidence for this in our devices is clear from measurements of the gate C-V characteristics that show a hump at a VGS of about 4 V (Fig. 9). This has also been observed by many other authors [12],[13],[14]. A consequence of this band alignment is the appearance of a large electric field across the dielectric.

Fig. 8 Energy band diagrams across the gate stack of GaN MIS-HEMT under positive gate voltage. Left: under DC and after long enough wait following a gate pulse under AC. Right: immediately after the onset of a stress pulse.

Under fast-pulsed conditions, however, this inversion layer might not be able to respond sufficiently fast (Fig. 8, right). Electrons that accumulate at the dielectric/AlGaN interface must be supplied from the 2DEG at the AlGaN/dielectric interface, leading to a second increase in capacitance. Source and drain are shorted.
interface to the dielectric/AlGaN interface is likely to take place through a thermionic emission process over the AlGaN energy barrier. As a result, it will significantly slow down at low T, resulting in larger relative enhancements in $t_{\text{HBD}}$ at lower frequencies. In contrast, at high temperature we expect that electrons will readily respond to the AC drive, leading to little change in TDDB behavior between DC and AC.

The role of recovery voltage is less clear. A possible explanation for the effect that is observed is that with a 0 V recovery gate voltage under high-frequency conditions any electrons that made it to the dielectric/AlGaN interface during the stress phase might not be flushed out completely during the recovery phase. This is because the electric field across the AlGaN is likely to be small under $V_{\text{GS}} = 0 \, \text{V}$. In contrast, for a sufficiently large negative recovery voltage, the electrons across the dielectric/AlGaN interface will be flushed out in an efficient manner. Traps might also play a role in this behavior. Further experiments are required to clarify this.

VI. CONCLUSIONS

We show that in GaN MIS-HEMTs, time to breakdown in positive-gate TDDB experiments in significantly improve under AC stress when compared to DC stress. The increase is more significant at high frequency and low temperature. Furthermore, negative recovery voltage leads to a larger $t_{\text{HBD}}$ than recovery at zero volts at room temperature. The unique dynamics of the inversion layer at the dielectric/AlGaN interface are consistent with the observed behavior. A consequence of this study is that conventional dielectric lifetime extrapolation might be conservative, causing device designers to make unnecessary tradeoffs in performance.

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