A 120dB Programmable-Range On-Chip Pulse Generator for Characterizing Ferroelectric Devices

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Abstract—Novel non-volatile memory devices based on ferroelectric thin films represent a promising emerging technology that is ideally suited for neuromorphic applications. The physical switching mechanism in such films is the nucleation and growth of ferroelectric domains. Since this has a strong dependence on both pulse width and voltage amplitude, it is important to use precise pulsing schemes for a thorough characterization of their behavior. In this work, we present an on-chip 120 dB programmable range pulse generator, that can generate pulse widths ranging from 10 ns to 10 ms ±2.5% which eliminates the RLC bottleneck in the device characterisation setup. We describe the pulse generator design and show how the pulse width can be tuned with high accuracy, using Digital to Analog converters. Finally, we present experimental results measured from the circuit, fabricated using a standard 180 nm CMOS technology.

Index Terms—Pulse Generator, FTJ, FeFET, DAC, memory characterization

I. INTRODUCTION

Thanks to their ultra-low power operation, Complementary Metal-Oxide-Semiconductor (CMOS)-compatibility, and non-volatility, ferroelectric hafnium oxide-based devices such as ferroelectric capacitors (FeCAP) [1], ferroelectric field effect transistors (FeFET) [2], and ferroelectric tunneling junctions (FTJ) [3] are widely explored for digital storage conventional memory array architectures [1], [2] as well as in novel bio-inspired architectures [4]. Besides multi-bit storage in digital memories, the analog switching properties of these nano-scale devices are important for the realization of synaptic weight elements [5], [6] or artificial neurons [7] for adoption in neuromorphic applications [8]. In order to allow proper device optimization and defining the constraints for circuit design, a profound understanding of the switching kinetics in such nano-scale devices is needed [9].

Figure 1a depicts the results of such a switching kinetics measurement for a bilayer FTJ device featuring a 10 nm ferroelectric hafnium-zirconium-oxide (HZO) and a 2 nm aluminium oxide (Al$_2$O$_3$) layer sandwiched between two titanium nitride (TiN) electrodes [3]. The diagram depicts the portion of switched polarization upon application of different switching pulses. Extracting the respective switching voltage and time at 50% switched polarization results in the switching kinetics curve depicted in Fig. 1b. Extrapolation of this data yields both the data retention time of the respective device [11] as well as the required pulse voltages for ns-switching times. The switching kinetics of a given device will be material- and size-dependent [9], and as such, the characterization should be performed on individual devices. As an example, when looking at the voltage-time dependence in Fig. 1b and comparing to the data for an HZO-only sample (extracted from [10]), there is a shift to larger voltages due to the voltage drop over the Al$_2$O$_3$ layer, and an asymptotic saturation of switching time between 100 ns and 1 µs. This saturation is related to a RC-delay within the FTJ samples and measurement set-up that cannot be easily avoided. Similar issues occur for FeFET and FeCAP single devices, even though switching times down to just 14 ns to 20 ns have been demonstrated in integrated memory arrays [1], [2]. Obviously, the RC-delay has a strong impact on the extrapolation of switching kinetics, especially at shorter time scales, and consequently a pulse generator is required which is able to perform such a thorough characterization.
by applying pulses with varying amplitudes and timethroughs directly on-chip. Moreover, for the characterization of multi-bits and analogue storage a very precise control of the switching pulses is mandatory [12], especially for the steep switching gradients at shorter pulse times (see Fig. 1a). In order to tackle this issue, we developed an optimized on-chip pulse-generator circuit, enabling the application of well-controlled voltage pulses with timings that span over six orders of magnitude.

II. System Architecture

Figure 2 shows the architecture of the wide-range programmable on-chip pulse generator. On the arrival of the input pulses (shown as CLK), the programmable capacitor $C_{DAC}$ is abruptly charged to $V_{DD}$, and once the pulse is removed, it slowly discharges through the $I_{DAC}$ current. This results in a ramp voltage on node $V_{RAMP}$ which when compared to a reference voltage ($V_{REF}$), generates a pulse at the output ($V_{PULSE}$). The slope of the ramp voltage is determined by the magnitude of the current $I_{DAC}$ and the value of $C_{DAC}$. Therefore, the width of the pulse at the output of the comparator can be determined by the following equation:

$$I_{DAC} = C_{DAC} \cdot \frac{\Delta V_{REF}}{\Delta t}$$  \hspace{1cm} (1)

To have a precise control on the output pulse width ($\Delta t$), the circuit should be independent of the input pulse width, and employ a high-precision capacitor $C_{DAC}$, high-precision discharge current $I_{DAC}$, and a low-offset comparator. In this section we describe each of these blocks.

A. Edge detector

To decouple the $V_{PULSE}$ pulse-width from that of the CLK pulses, we implemented an Edge Detector block which detects the rising edge of the CLK signal and sends a fixed-width pulse to the transistor $M_{PD}$, independent of the CLK pulse width [13].

B. Wide-Range Current Digital to Analog Converter (IDAC)

The wide-range IDAC block of Fig. 2 represents a 7-bit current output binary weighted Digital to Analog Converter (DAC). It consists of identical modular unit cells, combined in a binary weighted fashion to work as p-type current sources.

The unit cells are sized appropriately to provide a precise value of current. Both p-type transistors where one being the current source and the other being the gating switch were sized to be of the same width but different lengths. The primary considerations for the sizing were the output resistance, matching, dynamic range and leakage depending on the function of each device. The DAC is biased by an external precise reference current which varies in three steps to cover the large operating range of the circuit as described in Table I.

One important consideration for the design of the current DAC is to ensure the current sources are accurate at large output currents, and that the current source transistors are not out of the saturation. The output impedance of the $I_{DAC}$ should be high to produce reliable output current with good accuracy. We decided to limit the systematic error $< 1\%$ to help the system deliver a highly accurate output current. This is especially important, because as shown in Figure 2, the $I_{DAC}$ output is injected to the $V_{RAMP}$ node whose voltage is changing over time, and the $I_{DAC}$ current should not be susceptible to this change through the drain-source voltage across the current sources of the $I_{DAC}$. We verified that the systematic error in the $I_{DAC}$ current is under 0.3% of the desired value, if the operating headroom is at least 400-450 mV. We simulated the functionality of the circuit with a wide range of currents, and verified with experimental measurements the correct functionality of the circuit down to the lowest current setting of 1 nA (see Section IV). Typically, the circuit’s systematic error is higher at lower currents, when p-type transistors operate in weak inversion. However, narrow pulses are needed to characterize the memristive devices. Therefore, in this application scenario to generate narrow pulses, the required $I_{DAC}$ current is in the order of magnitude where the IDAC operates in strong inversion saturation.

We performed a Monte Carlo simulation to quantify the expected accuracy and quality of this design, as we could not measure through a large set of silicon samples. In this analysis, we quantified the error for five different current settings ranging from the minimum to maximum of the 7-bit IDAC code across different range of operation as described in Table I. The deviation from the target value of the programmed current was calculated as:

$$I_{DAC,Error}[^\%] = \left( \frac{I_{DAC,Sim}}{I_{DAC,*}} - 1 \right) \cdot 100,$$

(2)

where $I_{DAC,Sim}$ is the actual simulated $I_{DAC}$ output current and $I_{DAC,*}$ is the desired output current programmed with the 7-bit code. The results are shown in Fig. 3. For this simulation, we limited the lower current setting of $I_{DAC}$ to 100 nA as the Monte Carlo simulation in this technology yields a very

![Fig. 2: Architecture of the Pulse Generator](image_url)
large systematic offset (probably arising from inaccurate sub-threshold mismatch models). It can be observed from Fig. 3 that the lower current setting of 100 nA shows the largest error, and the highest current setting of 1.28 mA (required for the narrowest pulse) shows the least error, indicative of its high accuracy. Overall, the combined 3σ error of $I_{DAC}$ is within ±6% for all the current ranges tested, without any calibration process. Extra tuning for higher accuracy is possible by adjusting the capacitance value (trimming).

C. $C_{DAC}$

The primary capacitor in this system is an 8-bit binary weighted capacitor DAC ($C_{DAC}$). The $C_{DAC}$ is constructed out of identical unit DAC cells, carefully laid out to provide a good level of matching among all the elements in the array. The resolution of the $C_{DAC}$ is 62.5 fF and the total capacitance we chose for our application is 10 pF. This enables us to adjust the DAC value and correct/trim out any non-idealities in the design with a precision of ±0.625%. As the desired value of 10 pF (maximum $C_{DAC}$ value = 16 pF) is not exactly at the centre of the DAC code range, we have non-uniform correction range centered around the desired value. However, one could potentially choose the exact center value of this DAC to be the capacitance required for pulse generation by either adjusting the $I_{DAC}$ current or the reference voltage $V_{REF}$ as described in Eq. 1.

D. Hysteretic Comparator

For this application, the primary considerations for a comparator was to have hysteresis to avoid false triggering due to fluctuations on the node the comparator monitors. In addition to this the other main considerations were to have low-offset and high-speed. For the comparator design, we chose a well-known architecture of a hysteretic comparator [14], [15] as shown in Fig. 4. Positive feedback is introduced in this circuit to have hysteresis.

III. IMPLEMENTATION AND SYSTEM LEVEL SIMULATION

The pulse generator was designed and fabricated in a standard 180 nm technology node. The final design excluding the probe pads occupy an area of 369 µm x 139 µm as shown in Fig. 5. The chip microphotograph is shown in Fig. 6.

The pulse generator can be programmed using internal Serial Peripheral Interface (SPI) registers. Both $I_{DAC}$ and $C_{DAC}$ are internally wired to their respective registers which are tightly integrated with rest of the analog circuitry as shown in Fig. 3. The I/Os are wired up to metal probe pads. They are powered and clocked externally through the wafer probing equipment. The FTJs will be fabricated on the same die with Back End Of Line (BEOL) post-processing integration steps. Therefore, the output of the pulse generator is directly connected to the FTJs with on-chip low parasitic interconnects and switches.

Table II compares the performance of this work against the implementations designed for similar application. This design can reliably cover a programmable range at least 4 orders of magnitude more than [16], the digital implementation on the same technology node. Although compared to [17], the area benefit of our work is explainable by the smaller technology node and the programming range is 1 order of magnitude less, the accuracy of the pulses in our design across the full programmable range is ±2.5% which is not reported in [16] and [17].
TABLE II: Performance comparison

| Parameters            | This work | [17] | [16] |
|-----------------------|-----------|------|------|
| Technology [nm]       | 180       | 350  | 180  |
| Implementation        | Analog    | Mixed| Digital |
| Silicon Area [mm²]   | 0.051     | 0.203| 0.015|
| Programmable Range [dB]| 120     | 150  | 42   |
| Output Pulse Accuracy [%] | ±2.5    | N.R. | N.R. |

* Not Reported

Fig. 7: Schematic of the electrical setup that provides the biases and signals to operate the pulse generator.

IV. HARDWARE SETUP AND ELECTRICAL CHARACTERIZATION

To measure data from the fabricated pulse generator circuit we used a probe-station and applied constant voltages and currents using a Semiconductor Parameter Analyzer (see Fig. 7). The SPI and CLK signals of Fig. 7 were generated using an Arbitrary Waveform Generator.

Fig. 9: Pre (red trace) and Post-calibrated (black dotted trace) pulse width measurements (a) 10 ms; (b) 100 µs; (c) 1 µs; (d) 336 ns

Initially, we biased the circuit using the same parameters used in the circuit simulations to produce pulses of desired widths. However, the fabricated circuits produced outputs that differ significantly from the circuit simulations (Fig. 8a). The option of precisely calibrating the capacitance value using the $C_{DAC}$ allows accurate pulse widths, with errors below ±2.5% (Fig. 8b). Here, only pulses down to 350 ns width could be measured, due to the RC parasitic load induced by the setup. This is confirmed in Fig. 9, showing a selection of waveforms generated by the pulse generator under different conditions. The trend shown in Fig. 8a proves that the pulse generator can work at shorter pulse widths. In normal operating conditions, the device to be tested is placed right next to the Pulse Generator, whose photograph, as well as a detail of the contacts for the BEOL-integration of ferroelectric devices, are shown in Fig. 6. In this configuration, the integrated Pulse Generator is no longer limited by the parasitic load, and the generated waveform are expected to be adequate to precisely investigate the switching kinetics of ferroelectric devices.

V. CONCLUSION

We presented an on-chip pulse-generator designed and fabricated in 180 nm technology. We demonstrated pulse generation across 6 orders of magnitude with an error of ±2.5%, while capable of driving relatively high parasitic capacitive loads present in the measurement setup. A low-parasitic on-chip interconnect between the pulse-generator and the FeFET/FTJ devices placed on the same silicon ensures a reliable delivery of programming pulses with high accuracy. Future work includes exploring performance of the two DACs and their effect on the output pulses. This work is a key enabler for thorough characterization of the FeFETs/FTJs, otherwise limited to the parasitics of the measurement set up.
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