Survey of Transient Execution Attacks

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ABSTRACT
Transient execution attacks, also called speculative execution attacks, have drawn much interest as they exploit the transient execution of instructions, e.g., during branch prediction, to leak data. Transient execution is fundamental to modern computer architectures, yet poses a security risk as has been demonstrated. Since the first disclosure of Spectre and Meltdown attacks in January 2018, a number of new attack types or variants of the attacks have been presented. These attacks have motivated computer architects to rethink the design of processors and propose hardware defenses. This paper summarizes the components and the phases of the transient execution attacks. Each of the components is further discussed and categorized. A set of metrics is proposed for each component to evaluate the feasibility of an attack. Moreover, the data that can be leaked in the attacks are summarized. Further, the existing attacks are compared, and the limitations of these attacks are discussed based on the proposed metrics. In the end, existing mitigations at the micro-architecture level from literature are discussed.

KEYWORDS
Transient Execution, Speculative Execution, Timing Channels, Covert Channels, Secure Processor Architectures

1 INTRODUCTION
In the past decades, computer architects have been working hard to improve the performance and power efficiency of computing systems. Different optimizations have been introduced in the various processor micro-architectures to improve the performance, including pipelining, out-of-order execution, and branch prediction [42]. Some of the optimizations require aggressive speculation of the executed instructions. For example, while waiting for a conditional branch to be resolved, branch prediction is used to predict the direction of the branch and the processor begins to execute code down the predicted control path before the outcome of the branch is known. Such speculative execution of instructions causes the micro-architectural state of the processor to be modified. The execution of the instructions down the speculated path is commonly called the transient execution – since the instructions execute transiently and should disappear with no side-effects if there was mis-speculation. When a mis-speculation is detected, the architectural and micro-architectural side effects should be cleaned up – but it is not done so today, leading to a number of recently publicized transient execution attacks [16, 53, 60, 70, 83, 95, 96, 102].

Besides focusing on pure performance optimization, many processors are designed to share hardware units in order to reduce area and improve power efficiency. For example, hyper-threading allows different programs to execute concurrently on the same processor pipeline by sharing the execution and other functional units among the hardware threads in the pipeline. Further, because supply voltage does not scale with the size of the transistors [72], modern processors use multi-core designs. In multi-core systems, caches, memory-related logic, and peripherals are shared among the different processor cores. Sharing of the resources has lead to numerous timing-based side and covert channels [41, 64, 91, 117] – the channels can occur independent of transient execution, or together with transient execution, which is the focus of this survey. The covert channels can be used to exfiltrate data from the transient states.

Today’s processor designs aim to ensure the execution of a program results in architectural states as if each instruction is executed in the program order. At the Instruction set architecture (ISA) level, today’s processors behave correctly. Unfortunately, the complicated underlying micro-architectural states, due to different optimizations, are modified during the transient execution, and the various transient execution attacks have shown how to make the modification visible so data can be leaked. For example, timing channels can lead to information leaks that can reveal some of the micro-architectural states which are not available at the ISA level [41, 64, 91, 117]. Especially, the micro-architectural states of a processor are not captured by the ISAs today, e.g., pipelining, the out-of-order execution, speculative execution, operation of the caches, sharing of units in hyper-threading, and the other sharing of resources in multi-core designs.

Transient execution combined with covert channels results in transient execution attacks which can compromise the confidentiality of the system, e.g., Spectre [1, 10, 20, 53, 54, 65, 86, 93], Meltdown [5, 16, 52, 60], Foreshadow [95, 102], LazyFP [89], or Micro-architectural Data Sampling (MDS) [70, 83, 96]. These transient execution attacks have been shown to break the security boundaries, e.g., privilege level, SGX enclave, sandbox, etc. These attacks have raised a lot of interests, and motivated computer architects to rethink the design of processors and propose a number of hardware defenses [8, 32, 50, 51, 85, 108] – this survey summarizes the attacks and hardware defenses, while software-based defenses are summarized in existing work [16].

This paper provides a survey of existing transient execution attacks. We start by analyzing each component of the transient execution attacks to show the root cause of these attacks. Then, we discuss the phases of the attacks and the data that can be leaked in these attacks. In the end, we discuss the mitigation strategies for each attack component and explain several existing hardware-based mitigations. The contributions are the following:

- We provide a taxonomy of the existing transient execution attacks by analyzing each component of the attack. We propose metrics to compare the attacks on different dimensions.
- We summarize and categorize the existing and potential timing-based covert channels in micro-architectures that...
can be used for transient execution attacks. We also propose metrics to compare the covert channels quantitively.
- We discuss the limitations of the existing attacks based on the metrics we proposed.
- We list and compare the different mitigation strategies in micro-architectural designs.

2 COMPONENTS AND PHASES OF TRANSIENT EXECUTION ATTACKS

Transient execution covert channel attacks are attacks that leak data from transient execution through a covert channel, where the secret or sensitive data is only available to the attacker when their code is executing transiently.

2.1 Components of the Attacks

The transient execution attacks contain two components: transient execution and a covert channel, as shown in Figure 1. Especially, the secret or sensitive data is only available to the attacker under transient execution – this differentiates the transient execution attacks from conventional covert channel attacks where the data is available, not just during transient execution.

After the secret data is accessed in transient execution and encoded into a covert channel, the secret data is extracted via the covert channel. Following the terminology in [94], we use the following terms:
- Speculation Primitive: The piece of code that causes transient execution to happen, e.g., prediction or an exception.
- Disclosure Gadget: The code to be executed transiently, which encodes the secret information into a covert channel.
- Disclosure Primitive: The covert channel used to make the secret observable by an attacker.

2.2 Attack Phases

As shown in Figure 1, there are three phases in the attacks:

Phase 1 – setup. The processor executes a set of instructions which modify the micro-architectural states such that it will later cause the transient execution of disclosure gadget to occur in a manner predictable to the attacker. An example is performing many branches at a specific address to “train” the branch predictor. The setup can be done by the attacker running some code or the attacker causing the victim to run in a predictable (to the attacker) manner so that the micro-architectural state is set up as the attacker expects.

Phase 2 – transient execution and encoding to the covert channel. The transient execution is actually triggered. The cause of transient execution is also known as speculation primitive. The disclosure gadget is executed transiently, to encode the secret into a covert channel. The instructions are eventually squashed, and the architectural states of the transient instructions are rolled back. Phase 2 can be either in the victim’s code or in the attacker’s code.

Phase 3 – decoding from the covert channel. The attacker is able to recover the data via the covert channel, called disclosure primitive of the attacker.

During an attack, Phase 1 and 2 cause the transient execution of disclosure gadget with the speculation primitive. Then, Phase 2 and 3 leverage the covert channel (a.k.a., disclosure primitive).

2.3 Where is Transient Execution Occurring?

Each phase can be performed by the attacker code or by the victim code, resulting in eight attack scenarios in Figure 2. When a phase is performed by the victim, the attacker should have the ability to trigger the victim to execute the code. We categorize the attacks based on who is execution transiently and encodes the secret to the covert channel in Phase 2.

2.3.1 Victim is Executing Transiently: If the victim is the one who executes transiently (Figure 2 (a-d)), the victim is caused to execute instructions that encode some secret into the covert channel during transient execution, and the attacker obtains the secret by decoding the signals from the covert channel. In this scenario, the attacker is assumed to be able to control or trigger the victim’s execution. The attacker can do this by calling some victim functions with certain parameters, e.g., in SGXpectre [20], the attacker can launch the target enclave program.

Different from the conventional side and covert channels, here, the victim encoding phase is executed transiently, and thus, the attack cannot be detected by simply analyzing the software semantics of the victim code. This attack vector leverages the difference between the expected semantics of software execution and the execution in hardware and is fundamental in current computer architectures.

To prepare for the transient execution (i.e., setup phase), there are also two options. First, sharing of hardware components that cause transient execution, e.g., the prediction unit, between the attacker and the victim, as shown in Figure 2 (c,d). So the attacker can be in control of the executed code. Second, the attacker triggers some of the setup code in the victim domain, as shown in Figure 2 (a,b). For the first option, the attacker needs to prepare some code to setup the hardware to lure the victim into desired transient execution. For the second option, the attacker needs to understand the victim’s code, and be able to trigger the code execution with a controlled input, e.g., call a function of the victim code.

To decode data from the covert channel, there are also two options: 1. the attacker using her code to observe the covert channel, as shown in Figure 2 (b,d); 2. the attacker use the victim code to observe the channel, as shown in Figure 2 (a,c). For the second case, the attacker may directly query some victim code, and the result of the victim code reveals information on the channel, or the attacker may trigger the execution of some piece of the victim code and measure the time or other side effect of the execution.

The attacker can use the victim code to complete both setup and decoding steps, as shown in Figure 2 (a), such as in [86]. In this case, the attacker can even launch the attack remotely. But most demonstration of transient execution attacks leverages scenarios (b,d) in Figure 2, because they use less code in the victim codebase and are easier for the attacker.

2.3.2 Attacker is Executing Transiently. As shown in Figure 2 (e-h), the attacker can directly obtain the secret in transient execution. The attacker will then encode the data into a covert channel and
decode it to obtain the secret in the architectural state, such as in her memory. The attacker can also launch different software threads for the setup or the decoding phases. The attacker’s code shown in Figure 2 (e-h) might be in different threads even on different cores.

During the attack, the attacker directly obtains the secret in transient execution, and thus, the attacker should be able to know the location of the victim data. There might be only the attacker code running, or the attacker and the victim running in parallel. When there is only the attacker code running, the victim’s protected data should be addressable to the attacker or the data is in some register in the hardware, i.e., the attacker should have a way to point to the data. In Meltdown [60], the attacker code first loads protected data by its virtual address to register and transfer the data through a covert channel. When the attacker and the victim are running concurrently, the attacker should be able to partially control the victim’s execution or synchronize with the victim execution. In MDS attacks [70, 83, 96], the attacker need to synchronize with the victim execution to extract useful information from the in-flight data of the victim.

The setup phases and decoding phases can also be done by the victim, resulting in four attack scenarios in Figure 2 (e-h). However, all the known attacks where the attacker executes transiently, i.e., Meltdown [60] and MDS [70, 83, 96], use exception (of the attacker) as the speculation primitive, and there is no need to train any predictor. Moreover, it is more practical for the attacker to decode from the covert channel rather than triggering the victim to decode. Thus, scenario (h) in Figure 2 is usually leveraged by the attacker in attacks where the attacker is executing transiently.
In micro-architectural implementations, transient execution allows the attacker to access more data than it is allowed in the architecture layer. Thus, this type of attacks is implementation-dependent and does not work on all the CPUs, e.g., meltdown [60], Foreshadow [95, 102], Micro-architectural Data Sampling (MDS) [70, 83, 96], are reported to work on Intel processors.

3 TRANSIENT EXECUTION

In this section, we focus on how to setup and trigger transient execution in Phase 1 and 2, respectively. Transient execution happens when the pipeline is squashed following a mis-speculation or detection of an exception and the all the architectural states are rolled back, but not all the micro-architectural side effects are cleaned up. We first discuss all possible causes of transient execution, discuss the features of transient execution that are required for an attack, and analyze under what condition the transient execution can be leveraged for attacks.

3.1 Causes of Transient Execution

The following is a list of possible causes of squashing the pipeline, which in turn are all the possible causes of transient execution.

Mis-prediction: The first possible cause for having to squash a pipeline is mis-prediction. Modern computer architectures make predictions to make full use of the pipeline to gain performance. When the prediction is correct, the execution continues and the results of the predicted execution will be used. In this way, predictions boost the performance by executing instructions earlier. If the prediction is wrong, the pipeline will be squashed, and the architectural states are rolled back as if the prediction never happened. There are three types of predictions: control flow prediction, address speculation, and value prediction.

1. Control Flow Prediction: Control Flow Prediction predicts the execution path that a program will follow. Branch prediction unit (BPU) stores the history of past branch directions and targets and leverages the locality in the program control flow to make predictions for future branches. BPU predicts whether the branch is to be taken or not (i.e., branch direction) by using pattern history table (PHT), and what is the target address (i.e., branch or indirect jump target) by branch target buffer (BTB) or return stack buffer (RSB).

2. Address Speculation: Address speculation is a prediction on whether two addresses are the same when the addresses are not fully available yet. It is used to improve performance in the memory system, e.g., store-to-load (STL) forwarding in the load-store queue, line-fill buffer (LFB) in the cache.

3. Value Prediction: To further improve the performance, while the pipeline is waiting for the data to be loaded from memory hierarchy, value prediction units have been designed to predict the data value and to continue the execution based on the prediction. While this is not known to be implemented in commercial architectures, value prediction had been proposed in literature [58, 59].

Exceptions: The second possible cause for having to squash a pipeline is exceptions. If an instruction causes an exception, the following instructions in the pipeline will be squashed when the instructing is to retire. And the OS will come to handle the exception.

3.1.1 Causes of Transient Execution in Existing Attacks

Not all transient execution can cause an attack, and Table 1 shows the speculation primitives leveraged in existing attacks. (Mis-)prediction is leveraged in Spectre-type attacks, e.g., [53]. Address speculation is leveraged in MDS attacks, e.g., [70, 83, 96]. Exceptions of loads or stores are leveraged in Meltdown-type attacks, e.g., [60, 95, 102]. Other types of exceptions, interrupts, and load-to-load reordering are not currently considered to be exploitable. Because the instructions that get squashed are in the execution path, the execution will be resumed later on, and no extra data is accessible to the attacker during the transient execution.

The sample codes of different variants are shown in Figure 3. The victim code should allow a potential mis-prediction or exception to happen. In Spectre V1, to leverage PHT, a conditional branch should exist in the victim code followed by the gadget. Similarly, in Spectre V2 and V5, the victim code should have an indirect jump (or a return from a function) that uses BTB (or RSB) for prediction of the execution path. In Spectre V4, to use STL, the victim code should have a store following a load having potential address speculation. In Meltdown, the attacker code should make an illegal load to cause an exception.

3.2 Metrics for Speculation Primitives

If the attacker wants to use a speculation primitive to launch a transient execution attack, the attacker should be able to cause transient execution of the disclosure gadget in a controlled manner. We use the following metrics to evaluate speculation primitives:

- Required Control of Victim Execution: This metric evaluates whether the attacker needs to control the execution of victim code – details will be discussed in Section 3.3.
- Level of Sharing: This metric evaluates how close the attacker should co-locate with the victim and whether the attacker should
The speculation primitive usually contains two parts: the code that needs prediction, e.g., conditional branch, direct or indirect jump, and the code that mis-trains the prediction units. In Phase 1, the prediction unit is mis-trained to direct future prediction to execute the disclosure gadget. In Phase 2, the transient execution of the disclosure gadget is triggered.

For the case of using mis-prediction as speculation primitive, the (mis-)training can be part of victim code, which is triggered by the attacker. In the example of Spectre V1, the attacker can first provide legal inputs to train the PHT to execute the gadget branch. Then, the training code will always share the same prediction unit as when the real attack happens. But in this case, the attacker should be able to control the execution of victim code. The (mis-)training code can also be a part of the attacker's code and run in parallel with the victim code, e.g., in Spectre V2. Then, it is required that the attacker’s training thread and the victim’s thread should be co-located to share the same prediction unit. Further, to share the same entry of the prediction unit, if the prediction unit is indexed by physical address, the attacker and the victim should also share the same memory space to share the entry. The required control of victim execution is summarized in Table 2.

For the speculation primitives that leverage exceptions, the instructions that follow the exception will be executed transiently, and thus, no mis-training (phase 1) is required, but the attacker needs to make sure the disclosure gadget is located in the code such that it is executed after the exception-causing instruction.

### 3.4 Level of Sharing in Mis-Training

The attacker can mis-train the prediction when running in parallel with the victim code. Then, it is required that the attacker’s training thread to share the same prediction unit with the victim. The following discusses different prediction mechanisms.

#### 3.4.1 Control Flow Prediction

To predict the branch direction, modern branch predictors use a hybrid mechanism [28, 47, 67, 69, 88]. One major component of the branch predictor is the PHT. Typically, a PHT entry is indexed based on some bits of the branch address, so a branch at a certain virtual address will always use the same entry in the PHT. In each entry of the PHT, a saturating counter stores the history of the prior branch results, which in turn is used to make future predictions.

To predict the branch targets, a BTB stores the previous target address of branches and jumps. Further, a return instruction is a special indirect branch that always jumps to the top of the stack. The BTB does not give a good prediction rate on return instructions, and thus, RSB has been introduced in commercial processors. The RSB stores $N$ most recent return addresses.

In Intel processors, the PHT and BTB are shared for all the processes running on the same physical core (same or different logical core in SMT). The RSB is dedicated to each logical core in the case of hyper-threading [65]. Table 3 shows whether the prediction unit can be trained when the training code and the

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**Table 1: Causes of Transient Execution and Existing Attacks Types.**

| Cause of Transient Execution | Attack Type |
|------------------------------|-------------|
| Prediction                   | Control Flow Prediction                     |
|                             | Address Speculation                          |
|                             | Value Prediction                              |
| Exception                   | Spectre (except V4)                           |
|                             | Spectre V4, MDS                               |
|                             | Not implemented in commercial architectures today |
| Load-to-load reordering      | Meltdown: no existing attacks today           |
|                             | Spectre V4, MDS                               |
|                             | Not implemented in commercial architectures today |

### 3.3 Required Control of Victim Execution

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**Figure 3:** Example code of transient execution attacks. Code highlighted in orange triggers transient execution. Code highlighted in yellow with dashed frame is the disclosure gadget.
victim are running in parallel in different settings. The results are implementation-dependent and Table 3 shows the result from Intel processors.

The prediction units sometimes have many entries, and the attacker and the victim should use the same entry for mis-training. The attacker and the victim will use the same entry only if they are using the same index. When the prediction unit is indexed by virtual address, such as the PHT and the BTB, the attacker can train the prediction unit from another address space using the same virtual address as the victim code, as shown in Table 3. If only part of the virtual address is used as the index, the attacker can train with an aliased virtual address, which maps to the same entry of the prediction unit as the victim address. The RSB does not index by the address, it overflows and has conflicts when there are more than N nested calls, and will cause mis-prediction.

3.4.2 Address Speculation: One of the uses of address speculation is in the memory disambiguation to resolve read-after-write hazards, which is the data dependency between instructions in out of order executions. In Intel processors, there are two uses of address speculation. First, loads are assumed not to conflict with earlier stores with unknown addresses, and speculatively store-to-load (STL) forwarding will not happen. When the address of a store is later resolved, the addresses of younger loads will be checked. And if store-to-load forwarding should have happened and data dependence has been violated, the loads will be flushed, and the new data is reloaded from the store, as shown in the attacks [1, 81]. Second, for performance, when the address of a load partially matches the address of a preceding store, the store buffer will forward the data of the store to the load speculatively, even though the full addresses of the two may not match [70]. In the end, if there is mis-prediction, the load will be marked as faulty, and flushed and reloaded again.

Another use of address speculation is in conjunction with the line-fill buffer (LFB), which is the buffer storing cache-lines to be filled to L1 cache. LFB may forward data speculatively without page-fill event, as in [96]. In an extreme case, the speculation can even be caused by a NULL pointer or an invalid address, and then the error is suppressed in the attacker code, as in attack [83]. In STL, the entries are indexed by a function of physical addresses. In this case, the training code needs to share memory space with the victim to achieve an attack.

3.5 Speculative Window Size

To let an attack happen, there should be a large enough speculative window for the disclosure gadget to finish executing transiently. The speculative window size is the window from the time the transient execution starts (instruction fetch) to the time the pipeline is squashed. In attacks leveraging predictions, the speculative window depends on the time the prediction is resolved. In a conditional branch, the time to resolve the branch depends on the time to solve the branch condition; in indirect jump, this depends on the time to obtain the target address; and in address speculation, this depends on the time to get the virtual and then the physical address. In

| Scenarios in Figure 2 | Phase 1 | Phase 2 | Required Control of Victim Execution |
|-----------------------|--------|--------|-------------------------------------|
| a,b                   | Victim | Victim | trigger desired victim execution   |
| c,d                   | Attacker | Victim | share prediction unit and address space to train |
| e,f                   | Attacker | Victim | trigger desired victim execution   |
| g,h                   | Attacker | Attacker | not required, all done by the attacker |

| Table 3: Level of Sharing and (Mis-)training the Prediction Unit on Intel processors. |
|-----------------|-----------------|-----------------|-----------------|-----------------|
| Prediction Unit | same thread     | same core, SMT  | same chip, different core | same motherboard |
| Branch          | (virtual addr)  | (virtual addr)  | –               | –               |
| PHT [31, 52]    | (virtual addr)  | (virtual addr)  | –               | –               |
| RSB [65]        | not by address  | –               | –               | –               |
| Address         | (physical addr) | –               | –               | –               |
| STL [46, 70]    | not by address  | not by address  | –               | –               |
| LFB [83, 96]    | –               | –               | –               | –               |
| Other*          | –               | –               | –               | –               |

*“-” indicates the prediction unit is not possible to be trained under the corresponding sharing setting; Otherwise, the prediction unit can be trained and "f(virtual addr)" indicates the prediction unit is indexed by a function of the virtual address, "f(physical addr)" indicates the prediction unit is indexed by a function of the physical address, and "not by address" indicates the prediction unit is not indexed by addresses. *Conflicting results are presented in different publications [30, 53]. *Most OSes overwrite RSBs on context switches. *STL is possible after context switch, but not on SGX enclave exit. *In [83], it is indicated that there could be other structures which forward data speculatively.
attacks leveraging exceptions, the speculative window depends on the implementation of exceptions. To make the speculative window large enough for the disclosure gadget, the attacker can delay the obtaining the result of the branch condition or the addresses by leveraging uncached loads from main memory, chains of dependent instructions, etc.

3.6 Exploitable Data

Table 4 lists the information that can be leaked by the current transient execution attacks, assuming the speculative window is large enough for the attack to happen.

In Table 4, we categorize the Spectre-type attacks by the type of prediction. We assume the victim is executing transiently and the disclosure gadget can only read from memory that the victim could access architecturally, as is assumed in [53]. In branch prediction, the disclosure gadget in victim code will execute transiently, and thus, any data then can be accessed by the victim legally can be leaked to the attacker. In address speculation, specifically STL, stale data or data depends on the stale data (e.g., data pointed by the stale data) can be accessed by the attacker. In addition, the Spectre-type attack can also access data transiently that is otherwise not permitted. So the attacker will execute transiently to access the secret. In Spectre V1 attack using SWAPGS instruction [12], kernel data can be accessed by the attacker running in user level.

Meltdown-type attacks allow the attacker to access illegal data directly in speculation. In some processor implementations, even if a load causes an exception due to permission violation, the data might still be propagated to the following instructions. For example, in Meltdown [60], privileged data is accessible transiently to an unprivileged user even if the privileged bit in the page table is set. In L1 terminal fault (L1TF) [102], secret data in L1 cache is accessible transiently even if the present bit in the page table is not set. In Table 4, Meltdown-type attacks are categorized by the cause of the exception and the related permission bit. [16] provides a systematic review of Meltdown-attacks, categorizing the cause of the exception and the related permission bit, the source of data leakage.

MDS-type attacks also allow the attacker to access data that is not permitted due to address speculation. Data present in the micro-architectural buffers can be accessed speculatively to the attacker. Different from Spectre-type and Meltdown-type attacks, address speculation is usually due to the address not being available yet, and thus, the data obtained is not related to the address used by the attacker, but could be any data in the buffer at the moment of the attack [70, 83, 96].

4 COVERT CHANNELS

Transient execution enables the attacker to access the secret data transiently, and for the attacker to eventually obtain the secret data in architectural states, a covert channel\(^\text{3}\) [91] is required. The disclosure gadget is the piece of code that encodes the data into the covert channel when executing transiently. There is a distinction between conventional channels where the encoding happens in software execution path, and transient execution channels where the encoding phase is executed transiently. Here, we focus on covert channels that can be used in transient attacks - these can also be used as conventional channels.

There are two parties in a covert channel: the sender and the receiver. In the covert channels, the sender execution will change some micro-architectural state and the receiver will observe the change to extract information.

4.1 Assumptions on Covert Channels as the Disclosure Primitive

This work focuses on covert channels that do not require physical presence and which only require attacker’s software (or software under the attacker’s control) to be executing on the same system as the victim. Thus, we do not consider physical channels, such as power [33], EM field [66], acoustic signals [6, 34], etc.; because the attacker needs to have physical access to the device and special sensors to get observations, which is hardly practical in remote software attacks. There are certain physical channels that can be accessed from software, such as temperature [105]. However, thermal conduction is slow and the bandwidth is limited.

Any sharing of hardware resources between users could lead to a covert channel between a sender and a receiver [98]. The receiver can observe the status of the hardware system with some metadata from the covert channel, such as the execution time, values of hardware performance counters (HPC), system behavior, etc.

The most commonly used observation by the receiver of the covert channels is the timing of execution. In today’s processors, components are designed to achieve a better performance, and thus, the execution time contains information about whether certain hardware unit is available during execution (e.g., port), whether the micro-architectural states are optimal for the code (e.g., cache hits or misses), etc. To observe the hardware states via timing, a timer is needed. In x86, rdtscp instruction can be used to read a high-resolution time stamp counter of the CPU, and thus, can be used to measure the latency of a chosen piece of code. When the rdtscp is not available, a counting thread can be used as a timer [84].

The receiver can also gain information from HPCs. HPCs have information about branch prediction, cache, TLB, etc., and are used in covert channel attacks [31]. However, HPCs must be configured in kernel mode [23], and thus, are not suitable for unprivileged attackers.

The receiver can further observe the state of the hardware by some system behaviors, e.g., abortion. In Prime+Abort attack [26], by exploiting TSX, an attacker receive an abort (call-back) if the victim process accesses a critical address.

In other cases, several covert channels are used in series. Here, for transient execution attacks, we only consider channels where the receiver can decode data architecturally. For example, in the Fetch+Bounce covert channel [81], first, the secret is encoded into the TLB states, which affect the STL forwarding, and then a cache Flush+Reload covert channel is used to observe the STL forwarding results. The first channel can only be observed by instructions in transient execution and the states will be removed when the instruction retires. We only consider the second covert channel to be critical for transient execution attack because the last channel allows the attacker to observe the secret architecturally.

\(^3\)The channel is considered a covert channel, not a side channel [53], because the attacker has control over the disclosure gadget, which encodes the secret.
We categorize the covert channels into volatile channels and persistent channels. In volatile channels, the sender and the receiver share the resource on the fly, no states are changed, e.g., sharing a port or some logic concurrently. The sender and the receiver have contention when communicating using this type of channel. In persistent channels, the sender changes the micro-architectural states, and the receiver can observe the state changes later, e.g., change of cache state. Although the states may be changed later, we call them persistent channels to differentiate from the volatile channels.

### 4.2 Categorization of Covert Channels

We categorize the covert channels into volatile channels and persistent channels. In volatile channels, the sender and the receiver share the resource on the fly, and thus the two should run concurrently, for example, as two hyper-threads in SMT processors or running concurrently on two different cores. As shown in Figure 4, the receiver first measures the baseline execution time when the sender is not using the shared resource. Then, the sender causes contention on the shared resource or not depending on the message to be sent, while the receiver continues to measure the execution time. If the execution time increases, the receiver knows the sender is using the shared resource at the moment.

Execution units, ports, and buses are shared between the hyper-threads running concurrently on the same physical core, and can be used for covert channels [3, 10]. L1 cache ports are also shared among hyper-threads. In Intel processors, L1 cache is divided into banks, and each cache bank can only handle a single (or a limit number of) requests at a time. CacheBleed [113] leverages the contention L1 cache bank to build a covert channel. Later, Intel resolved the cache bank conflicts issue with the Haswell generation. However, MemJam [71] attack demonstrates that there is still a false dependency of memory read-after-write requests when the addresses are of the same L1 cache set and offset for newer generations of Intel processors. This false dependency can be used for a covert channel. As shown in Table 5, the covert channel in execution ports and L1 cache ports can lead to covert channels between hyper-threads in SMT setting.

Memory bus serves memory requests to all the cores using the main memory. In [104], it is shown that the memory bus can act as a high-bandwidth covert channel medium, and covert channel attacks on various virtualized x86 systems are demonstrated.

#### 4.2.2 Persistent Covert Channels

In persistent channels, the sender and the receiver share the same micro-architectural states, e.g., registers, caches, etc. Different from volatile covert channels, the state will be memorized in the system for a while. And the sender and the receiver do not have to execute concurrently. Depending on whether the state has an ownership (i.e., can only be used by one party) or can be directly accessed by anyone, we further divide the persistent channels into occupancy-based and encode-based, as shown in Figure 5.

(1) **Occupancy-based Persistent Covert channels:**

- **Contention-based Persistent Channels:**

In this channel, the sender and the receiver will compete to occupy some states to store their data or metadata to (de-)accelerate their execution. One example of the contention-based channel is the Prime+Probe attack [38, 74, 75, 110]. The receiver first occupies a cache set (i.e., primes). Then, the sender may use the state for her data or not, depending on the message to be sent. And in the end, the receiver reads (i.e., probes) her data that were used to occupy the cache set in the first step to see whether those data are still in the cache by measuring the timing, as shown in the first row of Figure 5. Other examples of the contention-based channel are cache Evict+Time attack [9, 74], the covert channel in DRAM row buffer [76].

Another possible contention is that the sender needs to use the same piece of data (e.g., need exclusive access to the data for write), and thus, the receiver’s copy of data can be invalidated. Some state is used for tracking the relationship of data in different components, which can cause the data in one component to be invalidated and cause contention. For example, cache coherency policy can change the cache state of a cache line in a remote cache, and thus, it results in a covert channel between threads on different cores on the same processor chip [93, 111]. Cache directory keeps the tags and cache...
Figure 4: Steps for the sender and the receiver to transfer information through volatile covert channels. The yellow box shows the shared resource. The solid (dashed) arrow shows the shared resource is (not) requested or used by the corresponding party.

Figure 5: Steps for the sender and the receiver to transfer information through different types of persistent covert channels.

coherence state of cache lines in the lower levels of cache in a non-inclusive cache hierarchy and can cause eviction of a cache line in the lower cache level (a remote cache relative to the sender) to build a covert channel [110].

- **Reuse-based Persistent Channels:**
  In this channel, the sender and the receiver will share some data or metadata, and if the data is stored in the shared state, it could (de-)accelerate both of their execution. The cache Flush+Reload attack [37, 112] transfers information by reusing the same data in the cache. The receiver first clears the cache state. Then, the sender loads the shared data or not. And in the end, the receiver measures the execution time of loading the shared data, as in Figure 5. If the sender loads the shared data in the second step, the receiver will observer faster timing compared to the case when the sender does not load the shared data. There are other reuse-based attacks, such as Cache Collision attack [13] and the cache Flush+Flush attack [36]. BTB can also be used as such a covert channel, as shown in [101]. The sender and the receiver use the same indirect jump source, ensuring the same BTB entry is used. If the receiver has the same destination address as the sender, the BTB will make a correct prediction resulting in a faster jump.

(2) **Encode-based Persistent Channels:**
  Different from the contention-based and the reused-based covert channel, where the user needs to occupy the states (e.g., registers, cache, or some entries) or data to change the execution, in this type of channels, the sender and the receiver can both directly change and probe the shared state. One example of such a channel is the AVX channel [86]. There are two AVX2 unit states: power-off and power-on. To save power, the CPU can power down the upper half of the AVX2 unit by default. In step 2, if the sender then uses the AVX2 unit, it will be power-on the unit for at least 1 ms. In step 3, the receiver can measure whether the AVX2 unit is power-on by measuring the time of using AVX units. In this way, the sender encodes the message into the state of the AVX2 unit, as shown in Figure 5. Other examples are the covert channel using cache LRU states [15, 51, 106].

4.3 **Metrics for Covert Channels**
This section lists metrics to compare different covert channels:
- **Level of Sharing:** This metric indicates how the sender and the receiver should co-locate. As shown in Table 5, some of the covert channels only exists when the sender and the receiver share the same physical core. Other attacks exist when the sender and the receiver share the same chip or even the same motherboard.
- **Bandwidth:** This metric measures how fast the channel is. The faster the channel, the faster the attacker can transfer the secret. Table 5 compared the bandwidth of different covert channels. Usually, the bandwidth is measured in a real system considering the noise from activities by other software and the system.
- **Time Resolution of the Receiver:** As shown in Figures 4 and 5, the receiver needs to measure and differentiate different states. For a timing channel, the time resolution of the receiver’s clock decides whether the receiver can observe the difference between the sender sending 0 or 1. The last column of Table 5 shows the timing difference between states. Some channels, such as cache L1, require a very high-resolution clock to differentiate 5 cycles.
Table 5: Known Covert Channels in Micro-architecture.

| Covert Channel Type | Level of Sharing               | Bandwidth   |
|---------------------|--------------------------------|-------------|
|                     | same thread                     |             |
|                     | same core, SMT                  |             |
|                     | same chip, different core       |             |
|                     | same motherboard                |             |
| Volatile            | Execution Ports [3, 10, 98]     | not given   |
| Covert              | L1 Cache Ports [71, 113]        | not given   |
| Channels            | Memory Bus [104]                | ~700 B/s    |
| Persistent          | AVX2 unit [86]                  | >0.02 B/s   |
| Covert              | BTB [101]                       | not given   |
| Channels            | TLB [35, 44, 81]                | ~5 kB/s per set |
| Covert              | L1, L2 (tag, LRU) [51, 106, 107]| ~1 MB/s per cache entry |
| Channels            | LLC (tag, LRU) [15, 64]         | ~0.7 MB/s per set |
| Covert              | Cache Coherence [93, 111]       | ~1 MB/s per cache entry |
| Channels            | Cache Directory [110]           | ~0.2 MB/s per slice |
| Covert              | DRAM row buffer [76]            | ~2 MB/s per bank |

* indicates that the attack is possible to leak the protected data; □ indicates that the attack cannot leak the data.

Simulation results in GEM5. Depending on the setup, the required time resolution varies. The biggest one is shown. Shows the time resolution for covert channel use L1 cache. Depending on the level of TLB used, the required time resolution varies. The biggest one is shown.

 preservation of the secret. For covert channels in AVX and TLB, we have shown results in Table 5. For example, with Flush+Reload, the LLC leads to a covert channel sharing the same physical core. The Flush+Reload attack builds a covert channel when the sender and the receiver are on the same chip either on the same physical core (using L1/L2) or not (using LLC), i.e., the union of the sharing settings of L1/L2 and LLC in Table 5.

As shown in Table 5, the channels in caches have relatively high bandwidth (~1 MB/s), which allows the attacker to launch efficient attacks. Covert channels in AVX and TLB are slower but enough for practical attacks.

4.5 Disclosure Gadget

The covert channel is used in the disclosure gadget to transfer the secret to be accessible to the attacker architecturally. Disclosure gadget usually contains two steps: 1. load the secret to the register; 2 encode the secret into a covert channel. As shown in Figure 6, the disclosure gadget code depends on the covert channel used. For covert channels in the memory hierarchy (e.g., cache side channel), it will consist of memory access whose address depends on the

from 15 cycles, while the LLC covert channel only needs to differentiate 500 cycles from 800 cycles, and the receiver only needs a coarse-grained clock.

- **Retention Time:** This metric measures how long the channel can keep the secret. In some of the covert channels (volatile channels in Section 4.2.1), no state is changed, e.g., the channel leveraging port contention [3]. The retention time of such channels is zero, and the receiver must measure the channel concurrently when the sender is sending information. Other covert channels (persistent channels in Section 4.2.2) leverage state change in micro-architecture, the retention time depends on how long the state will stay, for example, AVX2 unit will be powered off after about 1ms. If the receiver does not measure the state in time, she will obtain no information. For other states, such as register, cache, etc., the retention time depends on the usage of the unit and when the unit will be used by another user.

4.4 Comparison of Covert Channels

Table 5 lists whether a covert channel exists in different sharing settings. Whether a covert channel exists depends on whether the unit is shared in that setting. For example, AVX2 units, TLB, and the L1/L2 caches are shared among programs using the same physical core. Therefore, a covert channel can be built among hyper-threads and threads sharing a logical core in a time-sliced setting. The LLC, cache coherence states, and DRAM are shared among different cores on the chip, and therefore, a covert channel can be built between different cores.

Some covert channels may use more than one component listed in Table 5. For example, in the cache hierarchy, there could be multiple levels of caches shared among the sender and the receiver. In Flush+Reload cache covert channel, the receiver can use the `clflush` instruction to flush a cache line from all the caches, and the sender may load the cache line into L1/L2 of that core or the shared LLC. If the sender and the receiver are in the same core, then the receiver will reload the data from L1. If the sender and the receiver are in different cores and only sharing the LLC, the receiver will reload the data from LLC. Therefore, even with the same covert channel code, the location of the covert channel depends on the actual setting of the sender and the receiver. On the other hand, for the same covert channel protocol, if it can establish a covert channel in different hardware components, the covert channel will exist in the settings that is the union of all the components shown in Table 5. For example, with Flush+Reload, the LLC leads to a covert channel among threads on different cores, L1/L2 leads to a covert channel sharing the same physical core. The Flush+Reload attack builds a covert channel when the sender and the receiver are on the same chip either on the same physical core (using L1/L2) or not (using LLC), i.e., the union of the sharing settings of L1/L2 and LLC in Table 5.

As shown in Table 5, the channels in caches have relatively high bandwidth (~1 MB/s), which allows the attacker to launch efficient attacks. Covert channels in AVX and TLB are slower but enough for practical attacks.
secret value. For AVX-based covert channels, the disclosure gadget encodes the secret by using AVX instruction.

5 EXISTING TRANSIENT EXECUTION ATTACKS

The transient execution attacks contain two parts: triggering transient execution to obtain data that is otherwise not accessible (discussed in Section 3) and transferring the data via a covert channel (discussed in Section 4).

Compared to conventional covert channel attacks, the transient execution attacks allow the attacker to access more secret data. In Spectre-type attacks, the victim will encode the secret into the channel, and the behavior cannot be analyzed from the software semantics without a hardware model of prediction. In Meltdown-type and MDS-type attacks, the micro-architecture propagates data that is not allowed to propagate at the ISA level (propagation is not visible at ISA level, but can be reconstructed through covert channels which observe the changes in micro-architecture). To formally model and detect the behavior, a new micro-architectural model, including the transient behavior, should be used [19, 39, 68].

5.1 Existing Transient Execution Attacks Types

To launch an attack, the attacker needs a way to cause transient execution of the victim or herself and a covert channel. Table 6 shows the attacks that are demonstrated in the publications. For demonstrating different speculation primitives, researchers usually use the covert channel in caches (row L1, L2 in Table 6). This is because the cache Flush+Reload covert channel is simple and efficient. For demonstrating different covert channels used in transient execution attacks, researchers usually use PHT (Spectre V1). This is because Spectre V1 is easy to demonstrate. Note that every entry in the table can become an attack. For mitigations, each entry of the table should be mitigated, either mitigate all the covert channels or prevent accessing the secret data in transient execution.

5.2 Limitations of Existing Attacks

5.2.1 Limited Controllability of the Speculative Primitive. Spectre-type attacks require the attacker to mis-train the prediction unit in the setup phase to let the victim execute gadget speculatively. To be able to mis-train, the attacker either needs to control part of the victim’s execution to generate the desired history for prediction or needs to co-locate with the victim on the same core. MDS-type attacks also require the attacker and the victim to share the same address speculation unit. As shown in Table 3, the prediction unit is shared only within a physical core, for some unit, not even share between each hyper-thread. In practice, it is not trivial to co-locate on the same core.

5.2.2 Limited Exploitable Data of the Speculative Primitive. Meltdown-type and MDS-type attacks both rely on the propagation of secret data during transient execution. Therefore, the attacks are implementation-dependent and are not applicable to all the processors [16]. Furthermore, there is a limit on the source of the data. For example, LITF attacks [95, 102] only pass data in L1 cache. MDS-type attacks only pass data in LFB [96] and STL [70]. If the critical data is not in the structure that is vulnerable or if the structure is isolated, the attack is mitigated. For example, to mitigate attacks in the time-sliced sharing setting, data can be flushed from the above-mentioned structure during a context switch.

5.2.3 Limitation of the Disclosure Primitive. For a covert channel to exist, the sharing of hardware is needed, which requires the co-location of the attacker and the victim. Furthermore, for a certain attack implementation, only one disclosure primitive is used, and the attack can be mitigated by blocking the covert channel.

6 MITIGATIONS OF SPECTRE-TYPE ATTACKS IN MICRO-ARCHITECTURE DESIGN

In this section, we focus on mitigations to Spectre-type attacks in micro-architecture designs. Spectre-type attacks are more fundamental in modern computer architectures. Meltdown-type and MDS-type attacks are implementation-dependent, and we consider them as implementation bugs. They can be fixed, although performance penalty is unknown now. We focus on possible future micro-architecture designs that are safe against Spectre. Thus, software mitigation schemes in current commercial computers, such as [17, 18, 73], are not discussed in detail.

6.1 Mitigating Transient Execution

The simplest mitigation is to stop any transient execution. However, it will come with huge performance overhead, e.g., adding fence after each branch to stop branch prediction causes 88% performance loss [108].

To mitigate Spectre-type attacks, one solution is to limit the attackers’ ability to mis-train the prediction units to prevent the disclosure gadget to be executed transiently (the first metric in Section 3.2). The prediction units (e.g., PHT, BTB, RSB, STL) should not be shared among different users. This can be achieved by static partition for concurrent users and flush the state during context switches. For example, there are ISA extensions for controlling and stopping indirect branch predictions [4, 45]. In [92], a decode-level branch predictor isolation technique is proposed. However, if the attacker can train the prediction unit by executing victim code with certain input (e.g., always provide valid input in Spectre V1), isolation is not enough.

There is also mitigation in software to stop speculation to make the potential secret data depends on the result of the branch condition by introducing data dependency, e.g., masking the data with the branch condition [17, 73], because current processors do not speculate on data. However, this solution requires to identify all control flow dependency and all disclosure gadgets, to figure out
## Table 6: Transient Execution Attacks Types.

| Covert Channel          | PHT | BTB | RSB | STL | LFB | Exception |
|-------------------------|-----|-----|-----|-----|-----|-----------|
| Execution Ports         | ![10] | ![□] | ![□] | ![□] | ![□] | ![□]       |
| L1 Cache Ports          | ![□] | ![□] | ![□] | ![□] | ![□] | ![□]       |
| Memory Bus              | ![□] | ![□] | ![□] | ![□] | ![□] | ![□]       |
| AVX2 unit               | ![86] | ![□] | ![□] | ![□] | ![□] | ![□]       |
| TLB                     | ![□] | ![□] | ![□] | ![□] | ![□] | ![□]       |
| L1, L2 (tag, LRU)       | ![20, 53] | ![53] | ![54, 65] | ![1, 70] | ![83, 96] | ![□]       |
| LLC (tag, LRU)          | ![□] | ![□] | ![□] | ![□] | ![□] | ![□]       |
| Cache Coherence         | ![93] | ![□] | ![□] | ![□] | ![□] | ![□]       |
| Cache Directory         | ![□] | ![□] | ![□] | ![□] | ![□] | ![□]       |
| DRAM row buffer         | ![□] | ![□] | ![□] | ![□] | ![□] | ![□]       |

□ shows attacks that are possible but not demonstrated yet.

all possible control flow that could lead to the execution of the disclosure gadgets, and to patch each of them. It is a challenge to identify all (current and future) disclosure gadgets, because disclosure gadgets may vary due to the encoding to different covert channels, and formal methods are required [39].

The windowing gadget creates a large enough speculative window to let the disclosure gadget execute transiently. The micro-architecture may be able to limit the time of speculation to prevent the encoding to the covert channel (the third metric in Section 3.2). However, the disclosure gadget can be very small that only contains two loads from L1 [106], which is only about 20 cycles in total. Detecting a malicious windowing gadget accurately can be challenging.

To mitigate leak of secret during the transient execution attacks, one way is to prevent the transient execution of disclosure gadget, i.e., to stop loading of secrets in transient execution or stop propagating the secret to younger instructions in the disclosure gadget transiently. For Meltdown-type and MDS-type attacks, it means to stop propagating secret data to the younger instructions. For Spectre-type attacks, however, the logic may not know which data is secret. To mitigate the attacks, secret data should be tagged with metadata as in secure architecture designs, which will be discussed in Section 6.1.1.

Another conservative solution is that any data cannot be propagated speculatively, which can potentially prevent transient execution attacks with any covert channel. Specifically, in NDA [101], a set of propagation policies are designed for defending the attacks leveraging different types of transient executions (for example, transient execution due to branch prediction or all transient execution), showing the trade-off between security and performance. Similarly, in SpecShield [7, 8], different propagation policies are designed and evaluated. In Conditional Speculation [56], the authors target at covert channels in the memory system, and proposed an architecture where data cannot be transiently propagated to instructions that lead to changes in memory system showing 13% performance overhead. They further optimized the design for Flush+Reload cache side channels resulting performance overhead of 7%. Furthermore, in STT [114], all possible covert channels are analyzed and a dynamic information flow tracking based micro-architecture is proposed to defend all covert channels, which improves the performance by wake up instructions as early as possible. The overhead to defend Spectre-like attacks is moderate, e.g., 21% reported in SpecShield [7], 20 ~ 51% (113% for defending all transient execution attacks) reported in NDA [101], and 8.5% in STT [114].

### 6.1.1 Mitigations in Secure Architectures.

Secure architectures are designed to protect the confidentiality (or integrity) of certain data or code. Thus, secure architectures usually come with ISA extensions to identify the data or code to be protected, e.g., secret data region, and micro-architecture designs to isolate the data and code to be protected [21, 57, 90].

With knowledge about the data to be protected, hardware can further stop propagate secret data speculatively. The hardware can identify data that is depended on secret with taint checking, as proposed in [32, 53, 85, 92], and fords tainted data to have micro-architectural side effects or flushes all the states on exits to defend permanent covert channel, and disable SMT to defend transient covert channel. The overhead of such mitigation depends on the size of secret data to be protected. For example, as reported in ConText [85], the overhead is 71.14% for security-critical applications, and less than 1% for real-world workloads. Similar overhead is reported in SpectreGuard [32]. Intel also proposed a new memory type, named speculative-access protected memory (SAPM) [48]. Any access to SAPM region will cause instruction-level serialization and speculative execution beyond the SAPM-accessing instruction will be stopped until the retirement of that instruction.

### 6.2 Mitigating Covert Channels.

To limit the disclosure primitive, one way is to isolate all the hardware across the sender and receiver of the channel, so the change cannot be observable to the receiver. However, this is not possible, e.g., in some attacks, the attacker is both the sender and the receiver of the channel.

Another mitigation is to eliminate the sender of the covert channel in transient execution. For volatile covert channels, the mitigation is challenging. For permanent covert channels, there should not be speculative change to any micro-architectural states, or any micro-architectural state changes should be rolled back when the pipeline is squashed. Covert channels in memory systems, such as caches and TLBs, are most commonly used. Hence, most of the existing mitigations focus on cache and TLB side channels.
Table 7: Comparison of Different Mitigation Schemes in Micro-architecture.

| Mitigation Schemes                                | Performance Overhead                  |
|---------------------------------------------------|---------------------------------------|
| Fence after each branch                           | 88% [108]                             |
| Stop propagating all data                         | 30 ~ 55% [8]; 21% [7]; 20 ~ 51% [101]; 8.5% [114] |
| Stop propagating all data to cache changes        | 13% [56]                              |
| Stop propagating all data to Flush+Reload channel | 7% [56]                               |
| Stop propagating all tagged secret data           | 71% for security-critical applications, < 1% for real-world workloads [32, 85] |
| Partitioned cache                                 | 1 ~ 15% [51]                          |
| Stop (Undo) speculative change in caches          | 22% [108], 11% [80], 5.1% [79]        |

InvisiSpec [108] proposed the concept of "visibility point" of a load, which indicates the time when a load is safe to cause micro-architecture state changes that are visible to attackers. Before the visibility point, a load may be squashed, and should not cause any micro-architecture state changes visible to the attackers. To reduce performance overhead, a "speculative buffer" is used to temporarily cache the load, without modifications in the local cache. After the "visibility point", the data will be fetched into the cache. For cache coherency, a new coherency policy is designed such that the data will be validated when stale data is potentially fetched.

The GEMS [11] simulation results show a 22% performance loss for SPEC 2006 benchmark [43]. Similarly, SafeSpec [50] proposed to add shadow buffers to caches and TLBs, so that transient changes in the caches and TLBs does not happen.

CleanupSpec [79] proposed to use a combination of undoing the speculative changes and secure cache designs. When mis-speculation is detected and the pipeline is squashed, the changes to the L1 cache is rolled back. For tracking the speculative changes in caches, iKbyte storage overhead is introduced. To prevent the cross-core or multi-thread covert channel, partitioned L1 with random replacement policy and randomized L2/LLC are used. Because only a small portion of transient executions results in mis-speculations, the method shows an average slowdown of 5.1%.

Moreover, accessing speculative loads that hit in L1 cache will not cause side effects (except LRU state updates) in the memory system. Therefore, only speculative L1 hits can mitigate transient execution attacks using covert channels (other than LRU) in the memory system. In Selective Delay [80], to improve performance, for a speculative load that miss in L1, value prediction is used. The load will fetch from deeper layers in the memory hierarchy until the load is not speculative. In their solution, 11% performance overhead is shown.

Meanwhile, many secure cache architectures are proposed to use randomization to mitigate the cache covert channels in general (not only the transient execution attacks). For example, Random Fill cache [62] decouples the load and the data that is filled into cache, and thus, the cache state will no longer reflect the sender’s memory access pattern. Random Permutation (RP) cache [99], New-cache cache [63, 100], CEASER cache [78] and ScatterCache [103] randomize memory-to-cache-set mapping to mitigate contention-based occupancy-based covert channels in cache. Non Deterministic cache [49] randomizes cache access delay and de-couple the relation between cache block access and cache access timing. Secure TLBs [25] are also proposed to mitigate covert channels in TLBs. But again, all the possible covert channels need to be mitigated to fully mitigate transient execution attacks. Further, Cyclone [40] proposed a micro-architecture to detect cache information leaks across security domains.

Another mitigation is to degrade the quality of the channel or even make the channel unusable for a practical attack. For example, many timing covert channels require the receiver to have a fine-grained clock to observe the channel (the second metric in Section 4.3). Limiting the receiver’s observation will reduce the bandwidth or even mitigate the covert channel [77, 82]. Noise can also be added to the channel to reduce the bandwidth (the third metric in Section 4.3).

However, the above mitigations only cover covert channels in memory systems. To mitigate other covert channels, there are the following challenges: 1. Identify all possible covert channels in micro-architecture, including future covert channels. Formal methods are required in this process. For example, information flow tracking, such as methods in [24, 115, 116], can be used to analyze the hardware components, where the data of transient execution could flow to. Then, analyze if each of the components could result in a permanent or transient covert channel. 2. Mitigate each of the possible covert channels.

6.2.1 Mitigations in Secure Architectures. With clearly defined security domain, isolation can be designed to mitigate not only transient covert channels and also conventional covert channels. For example, to defend cache covert channels, a number of partitioned caches to different security domains are proposed, either statically [14, 22, 41, 51, 55, 61, 99, 109, 115, 116] or dynamically [27, 97]. With partition, shared resource no longer exists between the sender and the receiver, and the receiver cannot observe secret dependent behavior to decode the secret.

The above proposal assumes the hardware is isolated for each security domains. However, there is also the scenario where software outside the security domain may use the same hardware after a context switch. In Mi6 processor [14], caches and ports partitioning are used to isolate software on different cores. Further, when there is a context switch, a security monitor flushes the architecture and micro-architecture states, which holds the information of in-flight speculation from the previously executing program. To protect the security monitor, speculation is not used in the execution of the security monitor.

7 CONCLUSION

This paper provided a survey of the transient execution attacks. This paper first presents the two components of the attacks – transient
execution and covert channel, and the three phases of the attack. It further analyzes each component by proposing a set of metrics and using the metrics to compare the primitives used in existing attacks. Especially, the paper enumerates all possible causes of transient execution and compares.

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