Verifying Random Quantum Circuits with Arbitrary Geometry Using Tensor Network States

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The ability to efficiently simulate random quantum circuits using a classical computer is increasingly important for developing Noisy Intermediate-Scale Quantum (NISQ) devices. Here we present a tensor network states based algorithm specifically designed to compute amplitudes for random quantum circuits with arbitrary geometry. Singular value decomposition based compression together with a two-sided circuit evolution algorithm are used to further compress the resulting tensor network. To further accelerate the simulation, we also propose a heuristic algorithm to compute the optimal tensor contraction path. We demonstrate that our algorithm is up to 2 orders of magnitudes faster than the Schödinger-Feynman algorithm for verifying random quantum circuits on the 53-qubit Sycamore processor, with circuit depths below 12. We also simulate larger random quantum circuits up to 104 qubits, showing that this algorithm is an ideal tool to verify relatively shallow quantum circuits on near-term quantum computers.

Recent progress of quantum computing hardware has achieved more than 50 qubits with gate operation fidelities higher than 99%, marking the entering of the Noisy Intermediate-Scale Quantum (NISQ) computing era [1–3]. Accompanying with the hardware progresses, there is a stimulated interest in exploring suitable near-term applications for such devices [4–12]. A central difficulty when building NISQ hardwares with even more qubits is to maintain the high qualities of the devices as to the quantum gate operations as well as the quantum measurements. Thus efficient ways to benchmark quantum hardwares become increasingly important since it enables researchers and engineers to rapidly evaluate the performance of the quantum processors and continuously improve them.

Randomized benchmarking has been a standard tool to benchmark quantum gate operations [13, 14]. However, it is difficult to be scaled up to quantum circuits with several tens of qubits due to the rapid growth of complexity. In Ref. [15], random quantum circuits (RQCs) were proposed to benchmark the performance of quantum computing devices. RQC possesses at least two important features which make it an ideal problem for NISQ hardwares to solve: 1) RQCs often consist of interlacing layers of single- and nearest-neighbour two-qubit gate operations which are extremely friendly for current quantum computing hardwares and 2) with a total of only several hundreds of two-qubit gate operations, RQCs could already generate highly entangled quantum states which are extremely hard to reproduce with even the best supercomputers [16–18]. For those reasons, RQCs have been employed to demonstrate quantum supremacy [1, 19, 20]. An important ingredient when using RQCs to benchmark NISQ hardwares is to simulate RQCs with the best classical algorithm, which can server as 1) a baseline for the classical complexity of the problem and 2) a verification tool for the outputs of the quantum devices. However, verifying the 53-qubit RQC reported in Ref. [1] has already used 1 million cores for 5 hours, which poses a huge challenge for the verification of RQCs on large-scale quantum computing hardwares in the next stage.

So far, various classical algorithms have been proposed to simulate RQCs. Depending on the way that the quantum state is represented, those algorithms can roughly be divided into three categories: 1) directly storing and evolving the quantum state [21–24]; 2) tensor network contraction based methods, where the quantum state and the quantum circuit are treated altogether as a large tensor network, and then amplitudes are obtained by contracting this tensor network with certain contraction path [25–31] and 3) tensor network states (TNS) based methods [32, 33], adapted from the tensor network states algorithm originally developed in quantum many-body physics [34–36]. The first category is limited by the memory, since current most powerful supercomputers can only store about 50 qubits. The major differences between the second and last categories are that in tensor network states based methods: i) the quantum states are directly stored as tensor networks and the gate operations are applied onto those tensor networks subsequently, as a result quantum measurements can be simulated straightforwardly in addition to computing the amplitudes, ii) there is in general a compression stage following each two-qubit gate operation.

TNS based methods are often designed for regular lattices, such as a one-dimensional lattice or a square lattice, which may not be easily adapted to the topology of current NISQ hardwares. Moreover, there may exist some bad qubits inside the lattice which are not used for the computation at all [1]. In
this work, we present a TNS based algorithm which would be suitable for arbitrary lattice geometry. For the specific task of computing a single amplitude, we use a two-sided circuit evolution technique which could maximum compress the size of the resulting tensor network, accompanied with a heuristic algorithm used to search for the optimal tensor contraction path. We demonstrate the efficiency of this method by applying it to simulate 53-qubit RQCs up to a depth of 11, and comparing its performance with the Schödinger-Feynman algorithm [37], which was used as the benchmarking baseline for demonstrating quantum supremacy [1]. We also apply our algorithm to study large quantum circuits, showing that it is an ideal tool for fast verification of relatively shallow RQCs running on NISQ hardwares.

State initialization and gate operations. We assume that the lattice geometry can be represented by a connected graph, where each node represents a qubit and each edge means that there is at least one two-qubit gate applied on the two qubits connected by this edge. We denotes the graph as $G = (\mathcal{V}, \mathcal{E})$, where $\mathcal{V}$ represents the nodes (qubits) and $\mathcal{E}$ represents the edges. We use $\mathcal{E}_j$ to denote all the edges connected to the $j$-th node $\mathcal{V}_j$. The quantum state on such a graph $G$ is initialized as a tensor network state as follows. For each node $\mathcal{V}_j$ with $\dim(\mathcal{E}_j)$ edges, we initialize a $\dim(\mathcal{E}_j) + 1$ dimensional tensor $A_{\mathcal{E}_j}^{a_{\mathcal{E}_j}^1 \cdots a_{\dim(\mathcal{E}_j)}}$ (we will simply denote it as $A^j$ for short if the details of the indexes are not important in the context) of size $2 \times 1 \times \cdots \times 1$, reshaped from the vector $[1, 0]$ ($[0, 1]$) corresponding to the single-qubit state $\ket{0}$ ($\ket{1}$). The first index is the physical index and the rest indexes are the auxiliary indexes. Moreover, if two nodes $\mathcal{V}_l$ and $\mathcal{V}_l$ are connected by an edge, then one of the auxiliary index of $A^k$, say $a_{l_m}^k$, should be contracted with one of the auxiliary index of $A^l$, say $a_{l_n}^l$, and we would simply say that those two auxiliary indexes $a_{l_m}^k$ and $a_{l_n}^l$ are connected. The initial $N$-qubit quantum state $\ket{0}^N$ is thus written as a tensor network

$$\ket{0}^N = \mathcal{F}(A_{\mathcal{E}_1}^{a_{\mathcal{E}_1}^1 \cdots a_{\dim(\mathcal{E}_1)}} \cdots A_{\mathcal{E}_N}^{a_{\mathcal{E}_N}^1 \cdots a_{\dim(\mathcal{E}_N)}}),$$

(1)

where we have written $\sigma_j = 0$ on the superscript of each tensor to explicitly indicate that $A_{\mathcal{E}_j}^{a_{\mathcal{E}_j}^1 \cdots a_{\dim(\mathcal{E}_j)}} = 1$ for $\sigma_j = 0$ and 0 otherwise. $\mathcal{F}$ means to contract all the pairs of connected auxiliary indexes. The central difference of Eq.(1) from a tensor network state on a regular lattice is that the number of auxiliary index increases after a two-qubit gate operation on $A^k$ and $A^l$ can be denoted as

$$A_{[a_1^k \cdots a_{\dim(\mathcal{E}_k)}]}^{a_{\mathcal{E}_k}^1 \cdots a_{\dim(\mathcal{E}_k)}^k} \leftarrow \sum_{\sigma_k} P_{\sigma_k} a_{\mathcal{E}_k} a_{\sigma_k} \otimes a_{\sigma_k}^l;$$

(3)

$$A_{[a_1^l \cdots a_{\dim(\mathcal{E}_l)}]}^{a_{\mathcal{E}_l}^1 \cdots a_{\dim(\mathcal{E}_l)}^l} \leftarrow \sum_{\sigma_l} Q_{\sigma_l} a_{\mathcal{E}_l} a_{\sigma_l},$$

(4)

where $[a_1^k \cdots a_{\dim(\mathcal{E}_k)}]$ is the size of the auxiliary dimensions $a_{\mathcal{E}_k}$ and $a_{\mathcal{E}_l}$, and $a_{\mathcal{E}_k}$ and $a_{\mathcal{E}_l}$ are increased by a factor of $\chi_o$. The procedure of a two-qubit gate operation is also shown in Fig. 1(b). Single-qubit gates are not considered since they can be absorbed into two-qubit gates using gate fusion.

Compression by SVD. As we have pointed out in the introduction, an important feature of TNS based algorithms is that the resulting tensors after each two-qubit gate operation will be compressed, which can be done as follows. First we perform SVD on one of the resulting tensors in Eqs.(3, 4), say

![FIG. 1. (a) Three examples of graph geometries: the Sycamore processor, a square lattice as well as an arbitrarily connected lattice from left to right. Each red circle stands for one qubit, and the black lines represent the connections between the qubits, which also correspond to the auxiliary indexes of the tensor network states. The orange lines represent the physical indexes. (b) Two-qubit gate operation. The left rectangle with four orange lines and a dashed cut in between represents the splitting of a two-qubit gate into two three dimensional tensors as in Eq.(2). The block on the right hand side of the black arrow shows the procedure of the two-qubit gate operation, which corresponds to Eqs.(3, 4). We have used a thicker green line to explicitly indicate that the size of the auxiliary index increases after the two-qubit gate operation. (c) SVD compression of the resulting tensors from two-qubit gate operation corresponding to Eqs.(5, 6).](image-url)
\[ A^\sigma_{[a_1^\sigma \ldots a_m^\sigma]} = \sum_{s^\sigma}^\sigma U^\sigma_{[a_1^\sigma \ldots a_m^\sigma]s^\sigma} S^\sigma_{s^\sigma} V^\sigma_{[a_1^\sigma \ldots a_m^\sigma]} , \]  

where only the nonzero singular values of \( S \) are kept. Then one absorbs the matrix \( V^\sigma_{[a_1^\sigma \ldots a_m^\sigma]} = \sum_{s^\prime}^\sigma S^\prime_{s^\prime} V^\sigma_{[a_1^\sigma \ldots a_m^\sigma]} \) into the other tensor \( A^\sigma_{[a_1^\sigma \ldots a_m^\sigma]} \) as

\[ A^\sigma_{[a_1^\sigma \ldots a_m^\sigma]} \leftarrow \sum_{a_m^\sigma} A^\sigma_{[a_1^\sigma \ldots a_m^\sigma]} V^\sigma_{[a_1^\sigma \ldots a_m^\sigma]} . \]  

Thus the size of the auxiliary index \( a_m^\sigma \) changes from \( \dim(a_m^\sigma) \chi_0 \) to \( \dim(s') \), satisfying \( \dim(s') \leq \dim(a_m^\sigma) \chi_0 \), and similarly for \( a_1^\sigma \). The SVD compression procedure is shown in Fig. 1(c).

In the follow we identify two situations that we could have \( \dim(s') < \dim(a_m^\sigma) \chi_0 \). First, when the \( k \)-th qubit is applied on by a two-qubit gate \( O^\sigma_{a_k a_l} \) with \( \chi_0 = 4 \) for the first time, we will have from Eq.(5) that

\[ \dim(s') \leq \min(2 \dim([a_1^\sigma \ldots a_m^\sigma]), \dim(a_m^\sigma)) = 2. \]  

Namely the size of the corresponding index can at most increase to 2. We note that it is pointed out in Ref. [1] that the FSim gate in the first two layers can be simplified into a controlled phase gate with \( \chi_0 = 2 \), since it can be decomposed into a controlled phase gate and an iSWAP gate. In contrast for our method the compression in Eq.(7) naturally results from Eqs.(5, 6) for any two-qubit gate satisfying \( \chi_0 > 2 \). Till now such compressions are only possible in the first few layers of gate operations. Now recalling that for the task of computing amplitudes, the quantum circuit starts from a separable quantum state corresponding to a bitstring \( 00 \ldots 0 \) and is finally projected onto another separable quantum state corresponding to a bitstring \( s_1 s_2 \ldots s_N \) with \( s_n = 0, 1 \). To make use of the compression in Eq.(7) also in the last layers of gate operations, we can divide the two-body gates into two groups and perform a two-sided circuit evolution, that is, the first group of gates are applied on the initial quantum state \( |0 \rangle^N \), while the second group of gates are applied inversely onto target quantum state \( |s_1 s_2 \ldots s_N \rangle \), then one obtains one amplitude by computing the overlap between two resulting TNS. This procedure is shown in Fig. 2(a).

In the second case, we consider the DCD pattern as described in Ref. [1], which means that there are three successive two-qubit gates acting on the qubit pairs \( (k, l), (l, r) \) and \((k, l)\). We look at the tensor \( A^k \) and assume that its auxiliary index \( a_m^k \) is connected to the tensor \( A^l \). \( A^k \) is applied on twice, therefore the size of \( a_m^k \) would increase to \( \dim(a_m^k) \chi_0^2 \), while the sizes of the rest auxiliary indexes of \( A^k \) remain unchanged. Moreover, DCD pattern often happens at the boundary, such that \( A^k \) only has very few auxiliary indexes. As a result it is very likely that \( \dim(a_m^k) \chi_0^2 > 2 \dim([a_1^k \ldots a_{\dim(E_1)}^k]_m) \), in which case the size of \( a_m^k \) will get compressed by Eq.(5) and thus grows slower than by a factor of \( \chi_0^2 \). The occurrence of this pattern as well as the compression of the resulting tensors are shown in Fig. 2(b). We note that this compression is done automatically by Eqs.(5, 6) without additional manual efforts.

**Overlap between two tensor network states.** As shown in Fig. 2(a), the two-sided circuit evolution will result in two TNS corresponding to two output quantum states \( |\phi \rangle \) and \( |\psi \rangle \) respectively. Writing \( |\phi \rangle = \mathcal{F}(A_{a_1^1 \ldots a_{\dim(E_1)}^1} \ldots A_{a_1^N \ldots a_{\dim(E_N)}^N}) \) and \( |\psi \rangle = \mathcal{F}(B_{b_1^1 \ldots b_{\dim(E_1)}^1} \ldots B_{b_1^N \ldots b_{\dim(E_N)}^N}) \), the overlap of \( |\phi \rangle \) and \( |\psi \rangle \) can be computed by contracting all the physical indexes between them, that is,

\[ \langle \psi | \phi \rangle = \mathcal{F}(C_{c_1^1 \ldots c_{\dim(E_1)}^1} \ldots C_{c_1^N \ldots c_{\dim(E_N)}^N}) , \]  

where \( C_{c_1^1 \ldots c_{\dim(E_1)}^1} = \sum_{a_1^1} A_{a_1^1 \ldots a_{\dim(E_1)}^1} B_{b_1^1 \ldots b_{\dim(E_1)}^1}^{c_1^1} \) for \( 1 \leq l \leq N \). Eq.(8) is a tensor network on graph \( \mathcal{G} \). Directly contracting this tensor network will generally result in high-dimensional intermediate tensors which have to be stored distributedly, leading to cross-node data communication costs [33]. To overcome this difficulty, one can cut a few legs in Eq.(8) as done in Ref. [30]. For example, cutting the auxiliary dimension \( c_m^k \) amounts to splitting the \( m \)-th leg of the tensor \( C^k \) into \( \dim(c_m^k) \) slices (the same for the tensor which connects to \( C^k \) via \( c_m^k \)), as a result the tensor network in Eq.(8) is split into \( \dim(c_m^k) \) sub tensor networks in which the auxiliary index \( c_m^k \) is removed. Each sub tensor network produces a single scalar. Summing over these scalars results in the final amplitude.

In addition, we propose a heuristic algorithm to search for the optimal tensor contraction path. Based on the observation that current NISQ hardwares have a (quasi)-regular two-
dimensional geometrical structure, we made three assumptions that an optimal tensor contraction path \( \mathcal{P}_{i_1, \ldots, i_N} \) needs to satisfy: 1) \( \mathcal{P}_{i_1, \ldots, i_N} \) starts from a qubit on the boundary; 2) the rank of the intermediate tensors appear along this path is bounded by a maximum value \( \mathcal{M} \); 3) For each \( m \), the subgraph formed by the qubits \( \{i_1, \ldots, i_m\} \) is almost connected. These assumptions allow us to neglect most of the paths. And we are able to come up with an efficient searching algorithm using state compression dynamical programming technique, which is detailed in the supplementary [38].

**Verification of RQCs.** We demonstrate the efficiency of our algorithm by applying it to simulate RQCs running on a 53-qubit Sycamore processor, and then comparing its performance to the Schrödinger-Feynman algorithm [37]. Our TNS based algorithm is a single-amplitude algorithm since the complexity of computing \( M \) amplitudes is equal to \( M \) times the complexity of computing a single amplitude. In contrast, the Schrödinger-Feynman algorithm is a full-amplitude algorithm since computing a single amplitude is almost as hard as computing a bunch of \( M \) amplitudes. Therefore for a fair comparison one needs to specify the smallest number of bitstrings \( N_S \) required, for example, for the verification task. \( N_S \) will in general increase as the fidelity \( \mathcal{F} \) of the quantum circuit decreases, which can be computed as

\[
\mathcal{F} = \prod_{g=G} (1 - e_g) \prod_{q=Q} (1 - e_q). \tag{9}
\]

Here \( G \) denotes the gate set, \( e_g \) denotes the gate error rate, \( Q \) denotes the qubit set and \( e_q \) denotes readout error rate. The Sycamore processor used in Ref. [1] has a single qubit error rate of \( e_1 = 0.16\% \), two-qubit gate error rate of \( e_2 = 0.62\% \), and readout error rate of \( e_q = 3.8\% \). To ensure that \( \mathcal{F} \) is larger than 0 with \( 3\sigma \), where \( \sigma = 1/\sqrt{N_s} \) denotes the statistical error, \( N_s \) needs to satisfy \( N_s \geq (3/\mathcal{F})^2 \). We plot \( N_s \) as a function of the circuit depth \( d \) in Fig. 3(a).

In Fig. 3(b), we plot the estimated total run time \( t \) for both algorithms as a function of \( d \), where the blue dashed line with square stands for the Schrödinger-Feynman algorithm while the red dashed line with circle stands for our tensor network based algorithm. For the Schrödinger-Feynman algorithm, we measure the time \( t_0 \) for a single path and then the total run time \( t \) can be computed as \( t = t_0 N_p \) where \( N_p \) is the total number of paths. For the TNS based algorithm, we compute the time \( t_s \) for a single amplitude and then the total run time \( t \) is simply \( t = t_s N_p \). Both simulations are done using a single thread of the Intel-Xeon-Gold-6254 CPU (3.1 GHz). We note that our native implementation of the Schrödinger-Feynman algorithm has a performance similar to the record in Ref. [1], which is however still 1 to 2 orders of magnitudes slower than our TNS based algorithm (see Table I).

![Fig. 3](https://via.placeholder.com/150)

**TABLE I.** Run time to compute a single amplitude using TNS based algorithm. RQCs on Sycamore-like structures of sizes 54, 60, 66, 72, 104 and depths from 6 to 10 are simulated using a single thread. The run time is shown in seconds. NA means that data is not available.

| Processor       | 6   | 7   | 8   | 9   | 10  |
|-----------------|-----|-----|-----|-----|-----|
| Sycamore-54     | 24  | 19  | 143 | 1370| 7260|
| Sycamore-60     | 24  | 30  | 337 | 4145| 53007|
| Sycamore-66     | 29  | 82  | 1525| 28968| 267802|
| Sycamore-72     | 41  | 465 | 21669| 278679| NA   |
| Sycamore-104    | 107 | 15177| 458576| NA   | NA   |

1 The increase in the number of simulated paths could also greatly increase the computational complexity of the Schrödinger-Feynman algorithm (see Ref. [39] for details), which is not discussed here.

2 Here we consider only the Schrödinger-Feynman algorithm with 2 patches. Using more patches can reduce the memory consumption, but the time consumption may increase dramatically (see Ref. [39] for details).
to compress the size of the resulting tensor network from computing a single amplitude, which is further split into many smaller sub tensor networks using the cut technique. We then propose a heuristic algorithm to find the optimal tensor contraction path. We demonstrate with numerical simulations that our algorithm is of 1 to 2 orders of magnitudes faster than the Schrödinger-Feynman algorithm when simulating random quantum circuits on the 53-qubit Sycamore processor for depths $6 \leq d \leq 11$, and show that for relatively shallow RQCs our algorithm has a much more preferable scaling than the Schrödinger-Feynman algorithm as the number of qubits increases. Therefore we expect that our algorithm could be the method of choice for the fast verification of NISQ hardwares.

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Supplemental Material:
Verifying Random Quantum Circuits with Arbitrary Geometry Using Tensor Network States
Algorithm
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1. HEURISTIC ALGORITHM TO SEARCH FOR THE OPTIMAL TENSOR CONTRACTION PATH

In this section we present the details of our algorithm used to search for the optimal tensor contraction path. We denote an unordered collection of qubit indexes \( i_1, i_2, \ldots, i_m \) as \( \{i_1, i_2, \ldots, i_m\} \). A contraction path is specified by an ordered list of integers representing the corresponding qubit indexes, denoted as

\[
P_{i_1i_2\ldots i_m} = i_1 \rightarrow i_2 \rightarrow \cdots \rightarrow i_m,
\]

where \( 1 \leq m \leq N \). When \( m < N \), \( P_{i_1 \ldots i_m} \) denotes a partial tensor contraction path. \( P_{i_1i_2\ldots i_m} \) is order-sensitive so that \( P_{i_1i_2} \) and \( P_{i_2i_1} \) represent different contraction paths. For each path \( P_{i_1i_2\ldots i_m} \), there is a corresponding group of tensors denoted as \( \{C^{i_1}, C^{i_2}, \ldots, C^{i_m}\} \). Contracting all the tensors in this group, we will get a resulting tensor denoted as

\[
C^{i_1i_2\ldots i_m} = \text{Contract}(C^{i_1}, C^{i_2}, \ldots, C^{i_m}),
\]

where the function \( \text{Contract}(A_1, A_2, \ldots, A_n) \) means to contract all the pairs of connected auxiliary indexes of the input tensors \( A_1, A_2, \ldots, A_n \). The rank of \( C^{i_1\ldots i_m} \) is equal to the number of unconnected auxiliary indexes. When \( m = N \), all the auxiliary indexes have been contracted with each other and \( C^{i_1\ldots i_N} \) is a scalar. We can see that \( C^{i_1\ldots i_N} \) is unique for a fixed group of qubit indexes, namely \( C^{i_1\ldots i_m} = C^{i_2\ldots i_m} \) as long as \( \{i_1, \ldots, i_m\} = \{i_1', \ldots, i_m'\} \).

For each \( P_{i_1 \ldots i_m} \), we associate a score \( S_{i_1 \ldots i_m} \) which is a scalar representing the computational complexity of this path. We set \( S_{i_1} = 0 \) when \( m = 1 \). When \( P_m \) absorbs a new qubit index \( i_{m+1} \), \( S \) grows correspondingly

\[
S_{i_1 \ldots i_m i_{m+1}} = S_{i_1 \ldots i_m} + \text{Cost}(C^{i_1i_2\ldots i_m}, C^{i_{m+1}}),
\]

where the function \( \text{Cost}(A, B) \) means the computational complexity of contracting the two input tensors \( A \) and \( B \). Therefore the goal is to find the optimal tensor contraction path reduces to finding the path \( P_{i_1 \ldots i_N} \) with the least score \( S_{i_1 \ldots i_N} \). In the following we denote the optimal tensor contraction path as \( P_{\text{opt}}^{i_1, \ldots, i_N} \), and the corresponding score as \( S_{\text{opt}}^{i_1, \ldots, i_N} \), which satisfy

\[
S_{\text{opt}}^{i_1, \ldots, i_N} = \min_{i_1, \ldots, i_N} \{ S_{i_1, \ldots, i_N} \}.
\]

Here we have used \( \{i_1, \ldots, i_N\} \) in the subscripts of \( P_{\text{opt}} \) and \( S_{\text{opt}} \) to explicitly indicate that they are independent of the order of the underlying qubit indexes, and the function \( \text{Permutations}(N) \) means the group of all the possible permutations of the list \( \{1, 2, \ldots, N\} \).

Directly searching for \( P_{\text{opt}}^{\{i_1, \ldots, i_N\}} \) by traversing over whole configuration space is apparently impossible due to the exponential growth of the number of possible contraction paths. For example, for the 53-qubit Sycamore lattice there are a total of \( 53! \) paths. However the geometrical configurations of real quantum hardwares are in general not arbitrary, but instead have (quasi)-regular two-dimensional structures, such as the square lattice [1], the Sycamore lattice [2]. As a result, \( P_{\text{opt}} \) is should grow continuously, that is, the successive qubit indexes \( i_n \) and \( i_{n+1} \) should be neighbours, since otherwise \( \text{Cost}(C^{i_1i_2\ldots i_n}, C^{i_{n+1}}) \) would be very large since no pairs of auxiliary indexes will be contracted in this step. Since each qubit only has a few neighbours (at most 4 for the above mentioned lattices), one may exclude a huge number of contraction paths. To be concrete, we make the following assumptions:

1. There are well-defined boundaries for the lattice configurations of real quantum hardwares which has a fewer number of neighbours, and paths starting from those boundary qubits have less scores;
2. The rank of the tensor \( C^{i_1\ldots i_m} \) appeared along the optimal path should be less than a maximal value \( M \) for all \( 1 \leq m \leq N \);
3. The partial contraction path \( P_{i_1 \ldots i_m} \) is itself either a connected graph, or a connected graph plus a single isolated qubit index. If the latter case happens, then \( i_{m+1} \) must be such that \( P_{i_1 \ldots i_m i_{m+1}} \) is connected;

Assumption. 1 eliminates the paths starting from interior qubits and Assumption. 2 prohibits the occurrence of very high-dimensional intermediate tensors. \( M \) could be chosen as the tree width of the underlying graph, for example. Assumption. 3 eliminates the cases that there are two or more disconnected paths with different starting points, which grow and finally join
each other. There is no guarantee that latter approach is more expensive than the case of a single main path. However in cases of quasi-regular lattices, one could often find a single main contraction path with a similar numerical complexity to the case of several disconnected contraction paths, especially if parallelization is not considered, which is indeed the case here since it is much more efficient and elegant to parallelize this program on the level of computing several amplitudes or contracting those sub tensor networks encountered when computing a single amplitude. We allow a single isolated qubit simply because for the current quantum computing hardwares there may exist qubits with a single neighbour, for such cases and for certain paths adding such an isolated qubit may be more beneficial in terms of the size of the resulting tensor. These three assumptions, especially the last one, allow us to filter out most of the tensor contraction paths.

In the following we present an efficient searching algorithm based on the state compression dynamical programming technique and then give a justification for it. We denote all the necessary information attached with a partial contraction path \( P_{1_i \ldots i_m} \) as a three-tuple \( T_{1_i \ldots i_m} = \{ P_{1_i \ldots i_m}, S_{1_i \ldots i_m}, c \} \), where \( c \) is an additional integer indicating the connectivity of \( P \). If \( P \) is connected then \( c = -1 \), otherwise \( c \) is a positive integer representing the index of the isolated qubit. We use the priority queue data structure to store all the possible \( T \)s, denoted as \( D = \{ T_{1_i \ldots i_m}, T_{1_j \ldots j_n}, \ldots \} \). \( D \) supports two operations PUSH and POP, where the function \( \text{PUSH}(D, T_{1_i \ldots i_m}) \) inserts a new item \( T_{1_i \ldots i_m} \) into \( D \), while the function \( \text{POP}(D) \) means to take the item \( T \) with the least score \( S \) out of \( D \). We use \( V^B \) to denote the collection of the indexes of the qubits on the boundaries.

The algorithm is shown in Algorithm 1. We have also made use of two more auxiliary functions Neighbours and Connectivity. The function \( \text{Neighbours}(P_{1_i \ldots i_m}) \) outputs all the possible new qubit indexes satisfying Assumptions. (2, 3). The function \( \text{Connectivity}(P_{1_i \ldots i_m}) \) outputs an integer \( c \) representing the connectivity of the path \( P_{1_i \ldots i_m} \), that is, \( c = -1 \) if there is at least one edge between \( i_{m+1} \) and any of \( i_1 \ldots i_m \) and \( c = i_{m+1} \) otherwise. Assumption 1 is used in the initialization stage, where we restrict ourself to start from the boundary qubits. Assumptions. (2, 3) are used when using the function Neighbours.

**Algorithm 1:** Algorithm to search for the optimal tensor contraction path.

**Result:** Optimal tensor contraction path \( P^\text{opt}_{1_{i_1} \ldots i_N} \)

Initialize \( I = \{ \} \), \( D = \{ T_{i_1}, T_{j_2}, \ldots \} \) with \( i_1, j_2, \ldots \in V^B \) and \( T_{i_1} = \{ P_{1_i}, 0, -1 \}, T_{j_2} = \{ P_{j_1}, 0, -1 \}, \ldots \)

while true do

| \( T_{i_1 \ldots i_m} = \text{POP}(D) \) |
|---|
| if \( \{ i_1, \ldots, i_m \} \in I \) then continue |
| end |
| \( \text{PUSH}(I, \{ i_1, \ldots, i_m \}) \) |
| if \( m == N \) then return \( P_{1_i \ldots i_m} \) |
| end |

for \( i_{m+1} \in \text{Neighbours}(P_{1_i \ldots i_m}) \) do

\( S_{1_i \ldots i_m i_{m+1}} = S_{1_i \ldots i_m} + \text{Cost}(P_{1_i \ldots i_m, i_{m+1}}) \)

\( c = \text{Connectivity}(P_{1_i \ldots i_m i_{m+1}}) \)

\( T_{1_i \ldots i_m i_{m+1}} = \{ P_{1_i \ldots i_m i_{m+1}}, S_{1_i \ldots i_m i_{m+1}}, c \} \)

end

end

Now we give a justification of Algorithm 1. An important observation is that if \( P_{1_i \ldots i_m} \) is the optimal contraction path among all the possible paths for a fixed set of qubit indexes \( \{ i_1, \ldots, i_{m-1}, i_m \} \), then \( P_{1_i \ldots i_m} \) must also be the optimal contraction path for the fixed set of qubit indexes \( \{ i_1, \ldots, i_{m-1} \} \). This can be proven straightforwardly as follows: for any \( P_{1_i' \ldots i_{m-1}'} \) with \( S_{1_i' \ldots i_{m-1}'} > S_{1_i \ldots i_{m-1}} \), where \( \{ i_1' \ldots i_{m-1}' \} \) is a permutation of \( \{ i_1 \ldots i_{m-1} \} \), we will have

\[
S_{1_i' \ldots i_{m-1}'} = S_{1_i \ldots i_{m-1}} + \text{Cost}(C_{i_1' \ldots i_{m-1}'}, C_{i_1 \ldots i_{m-1}}) > S_{1_i \ldots i_{m-1}} + \text{Cost}(C_{i_1' \ldots i_{m-1}'}, C_{i_1 \ldots i_{m-1}}) = S_{1_i \ldots i_{m-1}} + \text{Cost}(C_{i_1 \ldots i_{m-1}}, C_{i_1 \ldots i_{m-1}}) = S_{1_i \ldots i_{m-1} \ldots i_m}.
\]

where we have used the fact that \( C_{i_1 \ldots i_{m-1}} \) and \( C_{i_1' \ldots i_{m-1}'} \) are the same tensor. Then we have

\[
S^\text{opt}_{1_i \ldots i_m} = \min_{i_m' \in \{1_i \ldots i_{m-1}\}} \left( S^\text{opt}_{1_i' \ldots i_{m-1}'} + \text{Cost}(C_{i_1' \ldots i_{m-1}'}, C_{i_1' \ldots i_{m-1}'}) \right).
\]

Since \( S^\text{opt}_{1_i' \ldots i_{m-1}'} \) and \( C_{i_1' \ldots i_{m-1}'} \) are both independent of the order of \( \{ i_1' \ldots i_{m-1}' \} \), there are only \( m \) possible candidates on
the right hand side of Eq.(6). Eq.(6) means that to find $P_{\{i_1, \ldots, i_m\}}^{opt}$, one only needs to find all the $m$ possible $P_{\{i'_1, \ldots, i'_{m-1}\}}^{opt}$s.

Therefore without Assumptions.(1, 2, 3), namely in the initialization stage and the Neighbours function we allow the most generic case, then Algorithm. 1 is guaranteed to find the global optimal contraction path. In practice, we find that when these contrains are imposed, Algorithm. 1 returns a reasonably well contraction path at least for current quantum hardware geometries.

II. DETAILS FOR THE NUMERICAL SIMULATIONS

TABLE S1: Comparison between our native implementation of the Schödinger algorithm with the data in Ref. [2]. In our simulations we have used four CPUs (Intel-Xeon-Gold-6254, 3.1GHz) with 18 cores each, while in Ref. [2] they have used n1-ultramem-160, which has four CPUs (2.2 GHz) with 20 cores each. NA means that data is not available.

| Num. of qubits | run time in seconds (ours) | run time in seconds (Google) |
|----------------|---------------------------|------------------------------|
| 30             | 28                        | NA                           |
| 32             | 93                        | 111                          |
| 34             | 362                       | 473                          |
| 36             | 1357                      | 1954                         |

We use the Schödinger-Feynman algorithm as the benchmarking baseline for our numerical simulations. In the Schödinger-Feynman algorithm, the full 53-qubit circuit is split into two sub circuits of 26 and 27 qubits separately. Then those two sub circuits are evolved independently until a cross gate $O$ acting on both groups is met, in which case the evolution is split into $\chi_o$ independent paths weighted by the $\chi_o$ singular values if $O$ as defined in the main text. For detailed descriptions of this algorithm one can refer to Refs. [2, 3]. Therefore given a specific way of splitting the full circuit, the total number of paths is determined by the number of cross gates (denoted as $n_c$) as well as the rank $\chi_o$ of them, which is $\chi_{o,c}^n$.

In practice, one can make a checkpoint at a particular cross gate by saving a copy of the states corresponding to those two sub circuits, and then for rest evolution of each path could start from those copies instead of evolving from the initial states. The total number of gate operations could be significant reduced by this technique, the price to pay is an additional copy of each quantum state of the sub circuits, which is manageable at a scale of 26 to 27 qubits. With this technique, assuming there are $n_p$ cross gates before this checkpoint, then the total number of paths is counted as $N_p = \chi_{o,c}^{n_p}$ instead, as done in [2]. We implement the Schödinger-Feynman algorithm natively, in which the checkpoint $n_p$ is chosen such that the total number of gate operations is minimized. In particular, we have chosen $n_p = 3, 4, 7, 8, 11, 14$ for $d = 5, \ldots, 11$ respectively. Moreover, since the performance of the Schödinger-Feynman algorithm is ultimately determined by the performance of the Schödinger algorithm on each sub circuit, here we show the performance of our Schödinger algorithm based simulator in in TABLE S1, from which we are confident that our implementation of the Schödinger-Feynman algorithm has at least the same level of performance compared to Ref. [2].

For the tensor network states based algorithm, we have used the cut technique to further split the resulting tensor network from computing a single amplitude into many smaller sub tensor networks. After that, we compute the best tensor contraction path $P^{opt}$ for one of those sub tensor networks using Algorithm. 1, and then contract all those sub tensor networks along this path. The positions as well as the number of cuts are chosen empirically, which are shown in Fig. S1. As a rule of thumb, one should cut the edges where the lattice is the thinnest.

FIG. S1: Quantum processors of Sycamore-like structure with different sizes used in the main text for (a) 54-qubits, (b) 60-qubits, (c) 66-qubits, (d) 72-qubits, (e) 104-qubits. Each circle represents a qubit and the edges between the qubits represent the positions of the two-qubit gate operations. The vertical dashed line represents the positions of the cuts which have been used in the simulation results from our tensor network states based algorithm.
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