Variance Reduction during the Fabrication of Sub-20 nm Si Cylindrical Nanopillars for Vertical Gate-All-Around Metal-Oxide-Semiconductor Field-Effect Transistors

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ABSTRACT: The variance of sub-20 nm devices is a critical issue for large-scale integrated circuits. In this work, uniform sub-20 nm Si nanopillar (NP) arrays with a reduced diameter variance (to ±0.5 nm) and a cylindrical shape, which can be used for vertical gate-all-around metal-oxide-semiconductor field-effect transistors, were fabricated. For the fabrication process, an array of tapered Si NPs with a diameter of approximately 62.7 nm and a diameter variance of ±2.0 nm was initially fabricated by an argon fluoride lithography followed by dry etching. Then, the NPs were oxidized in a self-limiting region. After the oxide removal, a similar oxidation process was used again for the NPs. It is determined that by controlling oxidation in the self-limiting region, the diameter variance can be reduced in the height direction of Si NPs (as well as shape control) and between NPs, simultaneously with a controllable diameter decrease. This approach decreases the variance in size caused by conventional nanoprocessing and helps overcome the position-dependent variance for 300 mm ϕ wafers, which is caused by current semiconductor processing.

1. INTRODUCTION

Owing to their superior electrostatic control and higher integration, vertical gate-all-around (VGAA) metal-oxide-semiconductor field-effect transistors (MOSFETs) are expected to replace fin-structured MOSFETs in the near future. VGAA-MOSFET fabrication based on Si nanopillars (NPs) with diameters of several tens of nanometers has been reported by several groups.1–3 The further development of VGAA-MOSFETs requires the fabrication of sub-20 nm Si NP arrays with a fine-controlled size and shape and a decreased diameter variance. In addition to their potential use in VGAA-MOSFETs, Si NPs (and Si nanowires) can be utilized in battery anodes,4 solar cells,5 thermoelectric devices,6 and image sensors.7 For MOSFET applications, the cylindrical shape is important for channels when considering full depletion of the carrier and the effect of the NP sidewall/gate oxide interface on channel current.1–3,8 Furthermore, the diameter variance between NPs should be reduced as much as possible.

Oxidation is a key step for Si, both for producing gate oxide and for cleaning the surface of two-dimensional (2D) planar Si. Retarded oxidation for Si NPs (also “self-limiting”) has been widely reported.9–17 According to the traditional theory of oxidation of 2D planar surfaces,18–24 it is generally assumed that retarded oxidation occurs owing to the inhibition of oxygen diffusion in the oxide and/or the compressive stress caused by the oxide (i.e., volume expansion from Si to SiO2).9–17 However, we determined that the inhibition of oxidant diffusion in oxides is insufficient to explain the acceleration of oxidation after the cracking (broken) of the Si core at the bottom of Si NPs (Figure 1, ref 25) without any change in peripheral oxide for long oxidation durations.25 Recently, we determined that the oxide on the sidewalls of Si NPs has lower density compared to that formed on a 2D surface under the same conditions,26 which further proves that the diffusion inhibition contributes less to the self-limiting oxidation of Si NPs. Moreover, the compressive stress introduced into a new oxide by an old oxide is insufficient to explain the formation of cracks at 1050 °C, which is much higher than the glass-transition temperature of SiO2.16,25 Therefore, we proposed and confirmed that the breakage of Si bonds at the Si/SiO2 interface during oxidation causes stress in unreacted Si, which is intrinsically responsible for the self-limiting behavior of Si NP,25 whereas the inhibition of oxygen diffusion in oxide and/or the compressive stress induced by the formed oxide acts as external factors.

In this study, we controlled the oxidation of Si NPs by understanding the self-limiting oxidation mechanism of Si NPs and fabricated uniform sub-20 nm Si NP arrays for VGAA-MOSFET applications. In contrast to the sacrificial oxidation that is widely used in semiconductor processing, which aims to remove surface damage and metal pollution, we used oxidation
to control the shape and size of Si NPs and to reduce the diameter variance. Two-step oxidation was applied. In the first step, oxidation was followed by oxide etching using a hydrofluoric acid (HF) solution, which reduces the compressive stress from the formed oxide. Then, a second oxidation process was applied. Two-step oxidation has been previously used to reduce the size of Si NPs. However, oxidation in a self-limiting region for precise size/shape control and variance reduction are less reported.

2. RESULTS AND DISCUSSION

2.1. Fabrication Process. Figure 1a–c shows the scanning electron microscopy (SEM) images with different magnifications of Si NP arrays on a chip during focused ion beam (FIB) processing. Here, the white dot arrays in Figure 1b observed on the chip are the top view of Si NPs with a SiGe deposition layer (SiGe protects Si NPs) in the non-FIB processing region. For the FIB processing region, the longitudinal cross section (side view) of Si NPs is observed on a film produced by FIB. A ~0.4 μm conductive carbon layer deposited during FIB processing can be observed on the upper region of the film. Figure 1d shows the typical transmission electron microscopy (TEM) bright-field image of the longitudinal cross section of a Si NP. Figure 1b,c shows that numerous Si NPs can be simultaneously obtained by FIB processing, which can be used to evaluate variance.

Figure 2 shows TEM images of a 62.7 nm-diameter Si NP (a) after the fabrication by ArF lithography and dry etching, (b) after first oxidation at 900 °C for 3.5 h, (c) after etching with 5% HF, and (d) after second oxidation at 1000 °C for 10 min.
As indicated in our previous work, the control for the fabrication of Si NPs by the self-limiting mechanism of diameter variance reduction and shape/size further improvements.

MOSFETs, but the shape of the reported Si NPs required the fabrication of sub-20 nm Si NPs for VGAA-SiO2 interface for the subsequent oxidation and, thus, in a process, as discussed above. Based on the ratio of $\Delta D_A$ to $\Delta D_0$, $\Delta D_0$, $\Delta D_3$, and $\Delta D_4$ decrease as the oxidation continues, which further decreases the oxidation rate. Because Si oxidizes layer-by-layer, the direction of oxidation-induced stress is perpendicular to the oxidation surface. For a 2D planar surface, such as a wafer surface, the oxidation-induced stress can relax in the depth direction of the Si wafer. However, for oxidation at the sidewall of a Si NP, relaxation conflicts occur in the two diagonal directions in the transverse cross section of an NP. Figure 3 shows a schematic diagram of oxidation-induced stress in the transverse cross section [(001) surface] of Si NP for which the array of Si atoms and bonds of the (001) surface was simplified from an sp3 structure to a 2D structure, as described in a prior work. Because the circle transverse cross section (red dashed circles) can be considered to be composed of many adjacent surfaces with different crystal orientations (here, simplified to eight Si/SiO2 interfaces marked with dark dotted lines) and crystal Si has an sp3 structure, the crystalline orientation has less influence on oxidation of sidewalls of Si NPs with a circle transverse cross section. As oxidation continues, the interface changes as $x$ of $\Delta D_A$ increases, which is similar to the layer-by-layer oxidation of a 2D surface. The Si-Si bond shrinkage transfers from the outside circle to the inside circle, which relaxes the stress in Si that is induced by oxidation. The pink arrows named $F_x$ and $F_x'$ (here $x = 1, 2, 3, 4...$) indicates, which is similar to the layer-by-layer oxidation of a 2D surface. The Si-Si bond shrinkage transfers from the outside circle to the inside circle, which relaxes the stress in Si that is induced by oxidation. The pink arrows named $F_x$ and $F_x'$ (here $x = 1, 2, 3, 4...$) indicates, which is similar to the layer-by-layer oxidation of a 2D surface. The Si-Si bond shrinkage transfers from the outside circle to the inside circle, which relaxes the stress in Si that is induced by oxidation.

2.2. Variance Reduction Mechanism. Here, we explain the mechanism of diameter variance reduction and shape/size control for the fabrication of Si NPs by the self-limiting oxidation process. As indicated in our previous work, the oxidation of Si to form SiO2 first breaks Si–Si bonds at the Si interface, which shrinks the remaining Si–Si bonds. This shrinkage causes compressive stress in residual Si, which results in more energy needed to break Si–Si bonds at the Si/SiO2 interface for the subsequent oxidation and, thus, in a decrease in the oxidation rate. The stress increases as oxidation continues, which further decreases the oxidation rate. Because Si oxidizes layer-by-layer, the direction of oxidation-induced stress is perpendicular to the oxidation surface. For a 2D planar surface, such as a wafer surface, the oxidation-induced stress can relax in the depth direction of the Si wafer. However, for oxidation at the sidewall of a Si NP, relaxation conflicts occur in the two diagonal directions in the transverse cross section of an NP. Figure 3 shows a schematic diagram of oxidation-induced stress in the transverse cross section [(001) surface] of Si NP for which the array of Si atoms and bonds of the (001) surface was simplified from an sp3 structure to a 2D structure, as described in a prior work. Because the circle transverse cross section (red dashed circles) can be considered to be composed of many adjacent surfaces with different crystal orientations (here, simplified to eight Si/SiO2 interfaces marked with dark dotted lines) and crystal Si has an sp3 structure, the crystalline orientation has less influence on oxidation of sidewalls of Si NPs with a circle transverse cross section. As oxidation continues, the interface changes as $x$ of $\Delta D_A$ increases, which is similar to the layer-by-layer oxidation of a 2D surface. The Si-Si bond shrinkage transfers from the outside circle to the inside circle, which relaxes the stress in Si that is induced by oxidation. The pink arrows named $F_x$ and $F_x'$ (here $x = 1, 2, 3, 4...$) indicates, which is similar to the layer-by-layer oxidation of a 2D surface. The Si-Si bond shrinkage transfers from the outside circle to the inside circle, which relaxes the stress in Si that is induced by oxidation.

Figure 4 shows the diameters obtained for Si NPs with different initial diameters (e.g., 50.9, 62.7, 78, 95.8, and 152.5 nm) prepared under different oxidation conditions. Non-oxidation data are also shown as a dark dotted line for comparison. The line slopes for the initial diameters larger than 78 nm exhibit a slight change, whereas the line slope changes more for the samples with diameters smaller than 78 nm. The greater change in the slope for thinner NPs is observed because thinner NPs have a lower oxidation rate compared to thicker NPs during the self-limiting oxidation process.
between Si NPs can be reduced by applying a self-limiting process.

The abovementioned mechanism contributes to a decrease in the variance caused by conventional nanoprocessing and helps overcome the position-dependent variance for 300 mm $\varphi$ wafers caused by current semiconductor processing. Furthermore, Si NPs fabricated by conventional lithography and etching processes exhibit a tapered structure, as shown in Figure 2a, with different diameters at different heights, which can be considered as a diameter variance. Thus, this variance can be decreased by applying the abovementioned self-limiting oxidation process. Importantly, this variance-reducing oxidation process should be performed in a self-limiting region, as shown in Figure 4. Based on the abovementioned mechanisms, we performed oxidation at 900 °C for 3.5 h for the first step and fabricated cylindrical Si NPs, as shown in Figure 2b. The top and bottom regions of the Si NP shown in Figure 2b exhibit a slight oxidation delay, which is attributed to a large Si–Si bond energy near the edge (so-called edge effect),\textsuperscript{29} that can be adjusted by a further self-limiting oxidation, as described below. In addition, the abovementioned mechanism is also available for the lateral Si NPs.

### 2.3. Variance Reduction between Si Nanopillars

Figure 5a shows the TEM images of Si NP arrays after the two-step oxidation process described in Figure 2 (oxidation at 900 °C for 3.5 h, etching, and oxidation at 1000 °C for 10 min) described in Figure 2 and (3) 62.7 and (4) 50.9 nm Si nanopillars after a similar process (oxidation at 900 °C for 3.5 h, etching, and oxidation at 900 °C for 2.5 h). The insets show TEM images for each sample.

Figure 5. (a) TEM image of Si nanopillar arrays after the process described in Figure 2; (b, c) magnified TEM image of the (b) left and (c) right sides of (a); (d) TEM image of a Si nanopillar in (a); (e, f) high-resolution TEM bright-field image of the (e) top and (f) bottom regions of the Si nanopillar in (d).

Figure 6. Diameters at different heights for 16 Si nanopillars shown in Figure 5a.

Figure 7. Diameters at the heights of T:40, T:70, T:100, T:130, and T:160 nm for four samples: (1) 62.7 and (2) 50.9 nm Si nanopillars after the process (oxidation at 900 °C for 3.5 h, etching, and oxidation at 1000 °C for 10 min) described in Figure 2 and (3) 62.7 and (4) 50.9 nm Si nanopillars after a similar process (oxidation at 900 °C for 3.5 h, etching, and oxidation at 900 °C for 2.5 h). The insets show TEM images for each sample.
after the process as described in Figure 2. As discussed above, the white dot arrays observed in Figure 1a,b are the top view of Si NPs with deposited SiGe. More than 60,000 NPs of each diameter were fabricated on one chip. We confirmed that for the 62.7 nm-diameter and thicker NPs subjected to the processing described in Figure 2, all of the dots remained, which suggest that all NPs remain after the proposed process. Thus, this process is suitable for mass production. However, for the 50.9 nm-diameter NPs, not all NPs remained even after the lithography and etching processes. Therefore, in this study, we estimate the variance only for 62.7 nm-diameter Si NPs.

Figure 8 shows the diameters measured from TEM images at heights of T:40, T:100, and T:130 nm for 16 Si NPs, as shown in Figure 5a. The dashed lines show the average diameter at each height. The diameters measured for the 16 NPs are within ±0.5 nm of the average diameter [we believe that instead of the deviation from the average value, it is better to estimate the variance in semiconductor processing compared to the standard deviation, although the standard deviation here is small (~0.3)] at all heights, except for T:130 nm (within ±0.7 nm), which will not be used for VGAA-MOSFET channels. The variance for 62.7 nm-diameter Si NPs after lithography and etching, which is estimated for the same region of a 300 mm φ wafer, is ±2.0 nm, based on the investigations by both SEM observations and TEM images. Therefore, the diameter variance decreases by 75% after the process described in Figure 2 (oxidation at 900 °C for 3.5 h, 5% HF etching, and oxidation at 1000 °C for 10 min), which is close to the value obtained from Figure 4. Furthermore, the average diameters at the heights of T:40, T:100, and T:130 nm are 16.8, 17.9, and 20.9 nm, respectively. The Si NPs obtained prior to the two-step oxidation presented in this work have diameters of approximately 57.1, 62.7, and 69.0 nm at the corresponding heights (oxidation and etching change the NP height). In addition, the diameter difference (diameter variance) at the two higher points (T:40 and T:100) varies between 5.6 and 1.1 nm, which represents an 80.4% decrease in variance. This value also confirms the assumption in Figure 4. Importantly, for the heights from T:40 to T:100 nm, the diameter difference is approximately 1.1 nm for a length of 60 nm, which is suitable for the fabrication of VGAA-MOSFETs with channel lengths on the order of 10 nm or less. The diameter difference for the two lower points (T:100 and T:130) decreases from 6.3 to 3.0 nm, which can be further decreased by adjusting the experimental conditions, as discussed below.

2.4. Variance Reduction in the Height Direction of Si Nanopillar (Shape Control). Figure 7 shows the diameter measured from TEM images at the heights of T:40, T:70, T:100, T:130, and T:160 nm for the four samples: (1) 62.7 nm-diameter and (2) 50.9 nm-diameter Si NPs after the two-step oxidation process (oxidation at 900 °C for 3.5 h oxidation, etching, and oxidation at 1000 °C for 10 min) described in Figure 2 and (3) 62.7 nm-diameter and (4) 50.9 nm-diameter Si NPs, after a similar process (oxidation at 900 °C for 3.5 h, etching, and oxidation at 900 °C for 2.5 h). The inset is the TEM image for each sample. It was determined that both (3) and (4) have longer cylindrical shapes (diameter variance is lower at different heights) than those of (1) and (2). This result is obtained because more self-limiting oxidation occurs at 900 °C for 2.5 h during the second oxidation step compared to that at 1000 °C for 10 min.9−17,25 Thus, the diameter variance in the height direction of Si NP (also considered as shape control) can be reduced by self-limiting oxidation. Specifically, sample (3) has almost the same diameter (~14.8 nm) at all measured heights, which satisfies the requirement of the fabrication of VGAA-MOSFETs with any channel length. The diameter decreases to ~11 nm for sample (4), but the cracking of the Si core at the bottom of Si NPs was observed for some NPs under this condition. It is assumed that this cracking was produced during the second oxidation step (oxidation at 900 °C for 2.5 h) after the first oxidation at 900 °C for 3.5 h, because cracking was observed at the bottom of the 50.9 nm-diameter Si NP after the oxidation at 900 °C for 5 h.25 In addition, we previously determined that in the self-limiting region, the oxidation at the sidewall of Si NPs is initially retarded and eventually stops at a certain size depending on the initial size and oxidation conditions, and further oxidation produces cracks at the bottom of NPs.25 Therefore, it is expected that a designated diameter (even to sub-10 nm) of Si NP arrays with a reduced diameter variance for both the height direction of Si NP and between NPs can be achieved by the abovementioned mechanisms.

3. CONCLUSIONS

In summary, by understanding and controlling a self-limiting oxidation process of Si NPs, using a two-step oxidation after
the lithography and etching processes, we fabricated uniform sub-20 nm Si NP arrays with a decreased diameter variance and controllable shape/size, which overcome one of the most crucial issues in the mass production of VGAA-MOSFETs for large-scale integrated circuits.

4. EXPERIMENTAL SECTION

4.1. Sample Fabrication. Argon fluoride (ArF) lithography with a subsequent dry-etching process can produce NPs with a diameter of approximately 60–160 nm, with a controllable shape and mass production yield, as shown in Figure 8a. By applying ArF lithography with a subsequent dry-etching process in a two-step oxidation (Figure 8b), sub-20 nm Si NP arrays were fabricated as follows. (1) Si$_3$N$_4$-capped Si NP arrays with a height of approximately 200 nm were fabricated with different diameters (e.g., 50.9, 62.7, 78, 95.8, and 152.5 nm at the center of the NPs, and the NPs larger than 78 nm were used as references) on a 300-mm $q$ wafer (p-type, resistivity: 10.38 $\Omega$·cm) by ArF lithography and dry-etching processes. (2) A chip cut from the wafer was oxidized in a furnace in pure dry oxygen at 900 °C for 3.5 h as the first oxidation step. (3) Then, the oxidized chip was immersed in 5% HF to remove the oxide. (4) After the removal of the oxide, the samples were oxidized again as a second oxidation step, but the temperature and duration were varied. Further details were introduced in our previous work.25,29

4.2. Evaluation. The evaluation of oxide thickness and diameter was performed at longitudinal cross sections of the Si NPs using TEM. The TEM samples (with a thickness of less than 100 nm) were fabricated using an FIB. Because the height of NPs changes owing to the oxidation on the bottom surface, the measurements were carried out at 40, 70, 100 (middle of NP), 130, and 160 nm from the top surface, which were denoted as T:40, T:70, T:100, T:130, and T:160 nm, respectively.

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Notes

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