Quantum circuit optimizations for NISQ architectures

Beatrice Nash¹,²,³, Vlad Gheorghiu³,⁴,⁵ and Michele Mosca³,⁴,⁶,⁷

¹ Department of Physics, Massachusetts Institute of Technology, Cambridge, MA, United States of America
² Department of Computer Science, Harvard University, Cambridge, MA, United States of America
³ Institute for Quantum Computing, University of Waterloo, Waterloo, ON, N2L 3G1, Canada
⁴ Department of Combinatorics & Optimization, University of Waterloo, Waterloo, ON, N2L 3G1, Canada
⁵ softwareQ Inc., Kitchener, ON, Canada
⁶ Perimeter Institute for Theoretical Physics, Waterloo, ON, N2L 6B9, Canada
⁷ Canadian Institute for Advanced Research, Toronto, ON, M5G 1Z8, Canada

E-mail: beatricenash@fas.harvard.edu and vlad.gheorghiu@uwaterloo.ca

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Abstract
Currently available quantum computing hardware platforms have limited 2-qubit connectivity among their addressable qubits. In order to run a generic quantum algorithm on such a platform, one has to transform the initial logical quantum circuit describing the algorithm into an equivalent one that obeys the connectivity restrictions. In this work we construct a circuit synthesis scheme that takes as input the connectivity graph and a quantum circuit over the gate set generated by \( \{ R_{\text{CNOT}}, R_Z \} \) and outputs a circuit that respects the connectivity of the device. As a concrete application, we apply our techniques to Google’s Bristlecone 72-qubit quantum chip connectivity, IBM’s Tokyo 20-qubit quantum chip connectivity, and Rigetti’s Acorn 19-qubit quantum chip connectivity. In addition, we also compare the performance of our scheme as a function of sparseness of randomly generated quantum circuits, and discuss how to apply our techniques as a subroutine for the more general mapping problem over universal set of gates (Clifford + T).

1. Introduction
Near-term quantum devices, such as noisy intermediate scale quantum computers (NISQ) [1], are limited by sparse qubit connectivity, and many current compilers require that the input circuit takes into account the allowed connectivity of the hardware. In this paper we introduce a circuit synthesis method that takes as input the connectivity of the hardware and the desired transformation that can be produced using gates from the set \( \{ \text{CNOT}, R_Z \} \), where \( R_Z \) denotes an arbitrary rotation about the Z axis of the Bloch sphere and outputs a circuit that respects the connectivity of the device. Our results show a significant decrease in CNOT count compared to circuit synthesis methods currently in use and allows for efficient circuit synthesis given any arbitrary connectivity. The method we present is a heuristic: finding the exact optimal solution appears intractable [2].

The concept behind our approach is to take circuit synthesis methods that optimize the CNOT count of the output circuit that perform well under the assumption of full connectivity ([3] for CNOT circuits and [4] for CNOT+\( R_Z \) circuits) and modify them to take into account connectivity constraints. We compare the results to first synthesizing the circuit using the original methods and then accounting for the constraints and found that our approach of considering connectivity constraints and synthesizing the circuit simultaneously produced sizable reductions. These reductions depend on the sparseness of the connectivity and the complexity of the input transformation, as shown in our Results section.

Our method is effective and simple to implement, taking as input the desired transformation (the exact form of which is described in detail in the section 2—Methods) and the graph representing the connectivity of the device and outputting a circuit that respects the allowed connectivity.

The reminder of this paper is organized as follows. In section 2 we describe our methodology, followed by our results in section 3. In section 4 we show how to apply our techniques to arbitrary circuits composed of gates.
from a universal set, discuss the limitations and also compare with state-of-the-art methods of general compilers such as the one implemented in Qiskit [5]. In section 5 we conclude our manuscript and raise a series of open questions. A fully worked out example that illustrates our methods is depicted in appendix.

Note: Recently, the authors of [6] independently presented a similar optimization scheme. Our work is independent of [6], being a longer version of the seminar presented by Beatrice Nash at the Dagstuhl Seminar 18 381: Quantum Programming Languages, p 120, September 2018, Dagstuhl, Germany [7], slide deck available online at https://materials.dagstuhl.de/files/18/18381/18381.BeatriceNash.Slides.pdf.

2. Methods

In order to perform a CNOT operation between logical qubits mapped to non-adjacent qubits, a sequence of CNOT gates between adjacent qubits is required to indirectly perform the desired operation. If we have linear nearest-neighbor connectivity, then to perform a CNOT between $q_1$ and $q_4$ can be achieved using the example circuits shown in figure 1.

These general templates can be extended to work for any physical qubit connectivity graph. While performing a CNOT operation between any two qubits is possible, it is expensive. The circuit depicted in figure 1(b) requires $4(l - 1)$ CNOT gates to perform the operation, where $l$ is the distance between the two qubits. The naïve swap circuit in figure 1(c) requires $1 + 6(l - 1)$ gates. For circuits that dynamically reassign physical and logical qubits, the last two swap gates in figure 1(c) can be removed.

The best current circuit synthesis methods do not account for qubit connectivity when determining the output circuit. CNOT operations in the optimized output circuit must be replaced by templates such as those shown previously to account for the connectivity of the physical device. Given the sparsity of connectivity graphs of near-term quantum devices, this step increases the CNOT count drastically.

2.1. Linear reversible circuit synthesis

The first class of circuits we look at synthesizing are linear reversible circuits consisting of only CNOT gates. In the Clifford + T universal gate set, the only two-qubit gate needed to achieve universal quantum computation is
the CNOT gate, and therefore the efficient synthesis of CNOT circuits is useful for optimizing broader classes of circuits given restricted connectivity. Additionally, CNOT gates are far noisier than single qubit gates, and thus minimizing the number of CNOT gates in a circuit is helpful for reducing errors.

Patel et al. give in [3] an asymptotically optimal algorithm for synthesizing linear reversible circuits assuming full connectivity. The result is a $O(n \log n)$ size circuit in the worst case, where $n$ is the number of qubits. In [8] it is proven that, for $n$ qubits, there exists a linear transformation for which the optimal circuit producing that transformation (again, assuming full connectivity) is size $\Omega(\frac{n^2}{\log n})$; hence, the method in [3] is optimal in the worst case to within a multiplicative constant. However, each single CNOT gate in the output circuit using method [3] becomes $O(n)$ gates using the template in figure 1(b) to account for connectivity constraints. Thus, the resulting circuit increases to size $O\left(\frac{n^2}{\log n}\right)$ in the worst-case under connectivity constraints. The algorithm we propose in this section improves on this performance, achieving an $O(n^2)$ worst-case bound on the size of the resulting circuit, regardless of connectivity.

The algorithm in [3], which is the foundation for that proposed here, takes as input an arbitrary linear transformation represented by a $n \times n$ binary matrix and outputs a circuit that produces the desired transformation. The initial state of the $n$ qubits is represented by the $n \times n$ identity matrix and each CNOT applied produces a row operation. Specifically, a CNOT with target $i$ and control $j$ multiplies the matrix representation of the circuit by the elementary matrix $A_{ij}$, which is the matrix with all elements on the diagonal and $(i, j)$ equal to 1 and all others equal to 0. This results in the bitwise addition of row $i$ to row $j$. Hence, each row corresponds to the parity of the associated qubit. An example is given in figure 2.

The idea behind the process is to reverse engineer a circuit from the matrix representation of the transformation. The algorithm from [3] is an optimized version of the Gaussian elimination approach to synthesizing the circuit. The steps are as follows:

1. Reduce the matrix to upper-triangular form. Each row operation corresponds to a CNOT in the output circuit.
2. Transpose the resulting matrix and repeat, resulting in the identity matrix.
3. Construct the output circuit from the operations performed in the following order: first, the operations done in 2) with their control/targets flipped and in the same order in which they were performed, and second, the operations done 1), with their control/targets preserved but the order in which they were performed flipped.

The $O\left(\frac{n^2}{\log n}\right)$ upper bound on the number of operations required for this process, as opposed to the $O(n^2)$ operations required for row reduction via Gaussian elimination, is achieved by partitioning. The matrix is divided into $\frac{n}{\log n}$ sections of size $\log n \times n$. Starting with the first section—after placing a 1 on the diagonal, if necessary—eliminate duplicate sub-rows within that section before performing row reduction normally. Then move on to the next section and do the same for the rows below the first $\log_2 n$. Continue in this way until the matrix is in upper triangular form, then transpose and repeat.

The algorithm we propose does not make use of the partitioning (although it can be easily altered to do so), because it takes advantage of grouping multiple row operations to perform together. We found that while partitioning works well when physical qubits are fully or very nearly fully connected ($\geq 85\%$), for connectivity as

![Figure 2.](image). (a) Matrix operations corresponding to CNOTs in circuit in (b).
sparse as that of near-term devices our algorithm works best without the use of partitioning. Therefore, we do not go into more details of the process; for more information, see \cite{5}.

Now, we give the intuition for the motivation for our method, using an example of a linear transformation on 6 qubits and their connectivity given in figure 3 (see appendix for the fully worked-out example). To eliminate the ones in the first column below the first row, the method in \cite{3} uses row 1 as the control for each of the operations. Thus, using this example, the sequence of operations for the first column—represented as (control, target)—is (1, 3), (1, 4), (1, 5). Under the assumption of full connectivity, this makes no difference. However, with restricted connectivity, each operation requires 4(l - 1) CNOT gates when using the template in figure 1(b), where l > 1 is the length of the shortest path between the two physical qubits. Thus, this sequence of operations requires 4 + 8 + 4 = 16 CNOT gates. However, if we are to instead perform the row operations (4, 5), (3, 4), (1, 3), the ones below entry (1, 1) are still eliminated, and instead of 16 CNOT gates, only 1 + 1 + 4 = 6 are required.

Give a connectivity graph and a set of rows, our goal is to find the shortest set of paths through the graph that effectively hits each of the nodes associated with those rows. Then, we want to convert that path into a sequence of operations that effectively eliminates each of the rows, while leaving the rest unchanged.

### 2.2. Steiner tree problem reduction

This problem reduces to the Steiner tree problem on the connectivity graph $G$ with edge weights of 1 and the set $S$ equal to the nodes associated with the control and the set of rows to be eliminated. The Steiner tree problem is that of finding the minimum weight tree, $T$, that is a subgraph of $G$ and includes, but is not limited to including, all nodes in $S$. Nodes in $S$ are called terminals, and nodes in $T$ but not in $S$ are known as Steiner nodes. An example is shown in figure 4. The reason for this reduction, perhaps not instantly clear, will become so once shown how to transform a tree into a sequence of row operations.

We want to translate this tree, $T_{(c,S)}$, where $c$ is the control, into a sequence of operations that effectively eliminates each row in $S \setminus \{c\}$ using only operations between adjacent nodes. $S \setminus \{c\}$ is the set of rows in the linear transformation matrix with ones in their $c$th entry. We now describe in detail the process of converting a tree to a sequence of row operations. Note that the process differs between whether the row operations are performed before or after the transpose step.

In order to convert the tree into a sequence of row operations, we first separate it into a set of edge disjoint sub-trees $\{T_{(i,S)}\}$ with root $c \in S$ and leaves $S_i \setminus \{c\} \subset S$. The remaining nodes in each sub-tree are Steiner nodes. The first sub-tree, $T_{(c,S)}$, is rooted at $c$. Starting from $c$, grow the sub-tree by traversing $T_{(c,S)}$ in breadth first search order. When arriving at a non-leaf terminal $u$, add $u$ to $T_{(c,S)}$ as a leaf and create a new sub-tree containing a copy of $u$ as a root. Once the sub-tree rooted at $c$ is complete, build the sub-trees rooted at its leaves. Continue until all the edges in $T_{(c,S)}$ have been added to a sub-tree. The root of each sub-tree will be used as the control to eliminate each of its leaves.

Compute the sequence of row operations as follows. Starting with the last sub-tree constructed, traverse the tree in reverse depth first search order. When traversing an edge $(u, v)$, where $u$ is closer to the root than $v$, add a row operation to the sequence with $u$ as the control and $v$ the target. Once the top of the tree is reached, we have a sequence of operations $R$. Let $R' = \text{reverse}(R - R[j])$, where $R[j]$ is the last operation in $R$. Now, create $R'$ by

\begin{figure}[ht]
\centering
\includegraphics[width=\textwidth]{figure3.png}
\caption{(a) Matrix representation of linear transformation; (b) connectivity of physical qubits.}
\end{figure}
removing from $R + R'$ those operations with terminals as the targets. $R + R'$ applies the row eliminations, while $R^*$ undoes those performed on the Steiner nodes, leaving them unchanged. $R + R' + R^*$ gives the completed sequence of operations for that sub-tree. Add $R + R' + R^*$ to the overall sequence of operations and move on to the prior sub-tree until all have been traversed.

We give an example in figure 5 for the resulting sequence of operations for the tree in figure 4 (assuming before the transpose step), using node 1 as the overall control. Each CNOT in the circuit shown corresponds to a row operation with the same control and target; they are shown this way to help visualize the result. In the resulting circuit, just as in the original algorithm, if these eliminations are performed before the matrix is transposed, their order will be flipped in the resulting circuit. If they occur after, their control/targets will be flipped, but their order will be preserved.

Each edge will be traversed exactly once in this process. Thus, the total number of gates required will be approximately $4 \times (l - d)$, where $d$ is the number of terminals (excluding the control) and $l$ is the number of edges in the tree. It is clear that for minimum $l$, this is the optimal solution; hence the reduction to the Steiner tree problem.

The minimal Steiner tree problem, however, is NP-hard. There are approximation algorithms that come close to optimal: the best being within a factor of 1.39, given in [9], which improved on the previous bound of 1.55, given in [10]. However, their run-time is insufficient for our algorithm, which requires many iterations, two for each row. The algorithm we use, given in [11], is somewhat of a combination between the better-performing and more efficient approximation algorithms.

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**Figure 4.** A solution to the Steiner tree problem on this graph, with each edge having weight 1. The non-shaded nodes are the terminals. The bold edges are those included in the solution. Nodes 4, 5, and 8 are Steiner nodes.

**Figure 5.** Resulting sequence of operations from the tree in figure 4.
Given a set of terminals and a connectivity graph, the algorithm performs breadth-first search outwards from each of the terminals. When the paths collide, the nodes along that path consolidate into a single node and all the edges adjacent to the consolidated nodes are placed adjacent to this new node. The process is restarted with this node as a new terminal. The total time will therefore be \( O(d \times (|V| + |E|)) \), where \( d \) is the number of terminals. The resulting Steiner tree is within a factor of \( 2 - 1/2 \) times the size of the optimal tree, where \( l \) is the number of leaves in the optimal tree. From many trials, it seems that this approximation is sufficient to see a large reduction in the CNOT count of the output circuit. The choice of Steiner tree approximation algorithm for this purpose depends on the user’s efficiency and performance requirements; a survey is given in [12].

The algorithm thus far works as follows:

1. Start with column \( i = 1 \).
2. If entry \((i, i) = 0\), find all rows \( j \) such that \((j, i) = 1 \) and \( j > i \). Choose \( j \) with the shortest path in the connectivity graph to \( i \), and use this path to perform a series of allowed row operations that adds row \( j \) to row \( i \).
3. Find rows below row \( i \) with entry in column \( i \) equal to 1. Create set of terminals \( S \) from nodes associated with those rows in addition to node \( i \).
4. Find Steiner graph approximation with connectivity graph \( G \) and terminals \( S \).
5. Compute row operations using this graph that eliminate those rows with constraints on allowed row operations. Perform those operations and compute resulting matrix.
6. Repeat steps 2–5 on the next columns, until the matrix is in upper-triangular form.
7. Transpose the matrix and repeat.

After the matrix is transposed, we must alter step 5 in the process slightly. Now, say that a row operation is effectively performed between \((i,j)\), with \( i \) as the control, and \( j \) as the target. If \( i > j \), then the lower-triangular form of the matrix is ruined. Thus, we have to alter the algorithm so as to only allow effective row operations with a lower index row as the control and a higher index as the target.

To do this, perform the Steiner tree algorithm as before, except use the smallest node as the control for all of the operations. Figure 6 shows how to eliminate two rows on the same path, which is never necessary before the transpose step. From figure 6 it is clear that the maximum number of additional gates required to ensure this requirement is \( 4 \times d \).

Let the output sequence of operations before the transpose step be a list \( A \) and after the transpose step be a list \( B \). When adding each operation to the output sequence \( B \), flip the control and target. The output circuit will be: \( B \) + reverse\((A)\).

The Steiner tree approximations will always be size \( O(n) \). Since the number of operations is \( O(4 \times \text{size of tree}) \), then the operations required will be \( O(n) \). Since there are \( O(n) \) trees computed in total throughout the execution of the algorithm (\( O(1) \) per column), then the overall number of operations is \( O(n^2) \), regardless of connectivity.
2.3. CNOT + phase circuit synthesis

The other class of circuits we look at synthesizing given connectivity constraints are those consisting of CNOT gates and Z-basis rotations of arbitrary angles. Amy, Azimzadeh, and Mosca give in [4] a heuristic algorithm for the efficient synthesis of CNOT count optimized circuits in this class assuming full connectivity. The results in [4] show a 23% decrease in the CNOT count on average for a suite of Clifford + T benchmark circuits.

The \( \{\text{CNOT}, \text{RZ}\} \) circuit to be synthesized is described by its phase polynomial \( f \) and matrix \( A \) representing the overall linear transformation on the basis states. \( (f, A) \), known as the sum-over-paths form, fully defines the desired unitary transformation applied by the output circuit, \( U_C \). For a size \( n \)-qubit circuit:

\[
U_C = \sum_{x \in \mathcal{F}_n^2} e^{2\pi i f(x)} |Ax\rangle \langle x|,
\]

where \( \mathcal{F}_n^2 \) is the set of all length \( n \) bit strings, and \( f(x) \) is given by:

\[
f(x) = \sum_{y \in \mathcal{F}_n^2} \hat{f}(y)(x_1 \oplus x_2) y_2 \oplus \ldots \oplus x_n y_n.
\]

\( f(x) \) is the Fourier expansion of \( f \) with Fourier coefficients \( \hat{f}(y) \). Let the support of \( \hat{f} \), \( \text{supp}(\hat{f}) \), be the parities with nonzero Fourier coefficient. Since the application of a CNOT gate with control \( x_1 \) and target \( x_2 \) maps \( |x_1, x_2\rangle \) to \( |x_1 \oplus x_2, x_2\rangle \), the state of each qubit can be mapped to a bit string representing a parity. Each \( \text{RZ} \) gate is determined by the parity of the state of the qubit on which it is applied at that point in the circuit. The coefficients for each parity \( y \in \mathcal{F}_n^2 \), \( \hat{f}(y) \), are given by the sum of the \( \text{Z} \) rotation angles on that parity. Hence \( \text{RZ} \) gates acting on the same parity can be combined. For example, the phase polynomial \( f \) and basis state transformation \( A \) associated with the circuit shown in figure 7 is:

\[
f = a(x_1) + (b + c)(x_2) + d(x_3 \oplus x_4 \oplus x_1) + e(x_3 \oplus x_4) + f(x_3 \oplus x_2 \oplus x_4)
\]

\[
A = \begin{pmatrix}
0 & 1 & 0 & 0 \\
1 & 1 & 0 & 0 \\
1 & 1 & 1 & 0 \\
1 & 1 & 0 & 1
\end{pmatrix}.
\]

The method in [4] first synthesizes a circuit with the input phase polynomial \( f \), then uses the method in [3] to produce the basis state transformation given by input matrix \( A \). To do the former, the goal is to compute a minimal parity network. A parity network is a circuit in which every parity in a set \( S \) appears. In our case, \( S = \text{supp}(\hat{f}) \). By applying \( R_\theta(A) \), with \( \theta = \hat{f}(y) \), to each parity \( y \in S \), the resulting circuit will have the desired phase polynomial. To apply the linear transformation to the basis states given by \( A \), first compute the linear transformation \( CA^{-1} \) and append it to the end of the existing circuit.

To find the exact minimal parity network, however, is NP-hard; a heuristic for synthesizing an approximation is given in [4]. The algorithm works as follows:

1. Represent the set of parities as a matrix \( P \), where each column corresponds to a parity and each row to a qubit. For example, \( P \) associated with the circuit given in figure 7 is

\[
P = \begin{pmatrix}
1 & 0 & 1 & 0 \\
0 & 1 & 1 & 0 \\
0 & 0 & 1 & 1 \\
0 & 0 & 0 & 1
\end{pmatrix}.
\]

\[\text{Figure 7. CNOT + phase circuit example.}\]
where the first column corresponds to parity $x_1$, the second to parity $x_2$, the third to parity $x_1 \oplus x_2 \oplus x_3$, the fourth to parity $x_1 \oplus x_2 \oplus x_4$, and the last to parity $x_3 \oplus x_4$.

2. Find the row $j$ (of those not yet recursed on) such that:
   
   $$ j = \arg \max_{i \in \text{cols}} \max_{x \in \{0,1\}} \{|P_{j,i} = x|\} $$

3. Separate $P$ into $P_0$, the columns $i$ with $P_{j,i} = 0$, and $P_1$, those with $P_{j,i} = 1$.

4. Recurse on $P_0$.

5. For $P_1$, find row $i = j$ such that all elements in row $i$ of $P_1$ equal 1. Add a CNOT with control $i$ and target $j$ to our parity network. Set $P'_1 = P_1 + P_j$. Repeat until no more such rows are found.

6. Recurse on $P'_1$.

---

**Figure 8.** Results for the synthesis of CNOT circuits producing a randomly generated linear transformation on 20 qubits for connectivity of varying sparseness. We repeatedly generate random connected graphs of sparseness between 0.0 and 1.0, where sparseness is defined as the probability that an edge is placed between two qubits. Sparseness of 1.0 is a fully connected graph. The size of the output circuit is compared against the size of the circuit produced by first using the method in [3] (with partitioning) to synthesize a circuit assuming full connectivity and then taking into account connectivity constraints. The reason that our method performs worse than the method in [3] for nearly complete connectivity is due to partitioning, which our method does not use, but which achieves an improvement when the qubits are nearly fully connected. Since qubits in NISQ devices only have nearest-neighbor connectivity, their connectivity is very sparse.

**Figure 9.** Results for the synthesis of CNOT circuits producing randomly generated linear transformations of various size on Google’s Bristlecone 72-qubit topology. The performance is calculated as described in the caption of figure 8.
A detailed example of this process can be found in [4]. Our method performs the same series of steps, except step 5 is modified as follows:

1. Compute the approximate Steiner tree of the connectivity graph $G$ with $S$ equal to the set of rows $\{i\}$ such that each element in row $i$ of $P$ equals 1. Using row $j$ as the control, eliminate them all together in the same manner described in the previous section.

In this case, whether the control bit has greater index than the target is not relevant.

Each parity in $\text{supp}(\hat{f})$ will appear at least once in this circuit. For each $y \in \text{supp}(\hat{f})$, apply gate $R_Z(\hat{f}(y))$ to the qubit with incoming parity $y$. Lastly, append the circuit producing linear transformation $AC^{-1}$, taking into account connectivity constraints, using the algorithm described previously.
In this section we compare the size of the output circuits generated using the algorithm described in the previous sections to those generated by first synthesizing the circuit using the method in [3] (for linear reversible circuits) or [4] (for CNOT + T circuits) without taking into account connectivity constraints, then, once the circuit has been synthesized, using the template given in figure 1(b) to take into account the connectivity. In both cases, after the circuit has been synthesized, we further optimize the size of the resulting circuit by commuting operators and canceling where possible.

We investigate random circuits on 20 qubits with varying connectivity (results depicted in figures 8 and 10), the Google Bristlecone 72 qubit architecture (results depicted in figures 9 and 11), the IBM Tokyo 20 qubit architecture (results depicted in figure 12, and the Rigetti’s Acorn 19 qubit architecture (results depicted in figure 13).
4. Universal gate sets

We briefly discuss extending the applications of the method described in this paper to universal gate sets. Circuits consisting of CNOT and phase gates alone are not sufficient for universal quantum computing. Adding the Hadamard gate, \( H = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \), to the \( \{\text{CNOT}, \text{R}_z\} \) gate set makes it universal. Without compromising the universality of the set, we restrict to specific \( z \)-rotation gates:

\[
S = \begin{pmatrix} 1 & 0 \\ 0 & i \end{pmatrix}, \quad T = \begin{pmatrix} 1 & 0 \\ 0 & e^{\pi i} \end{pmatrix}
\]

and their conjugate transposes. Let \( U \) be the set of circuits composed solely of these gates.

We can apply the methods described here to this more powerful class of circuits as follows. Given a circuit \( C \) in \( U \), we can optimize for the number of \( H \) gates in the circuit using the ‘merge and delete’ method [13]. Then, partition \( C \) into \( 2 \cdot k \) segments \( S_{a,b}, 1 \leq a \leq k, b \in \{\text{CNOT}, H\} \), such that

\[
S_{L,\text{CNOT}}S_{L,H} \ldots S_{L,\text{CNOT}}S_{L,H} = C
\]

and each \( S_{L,H} \) contains only \( H \) gates while each \( S_{L,\text{CNOT}} \) contains only gates from \( \{\text{CNOT}, S, T, S^\dagger, T^\dagger\} \). Next, we can apply the methods discussed in previous sections to each of the \( S_{L,\text{CNOT}} \) segments in order to account for connectivity constraints. As discussed in the previous section, our method performs better as gate count increases, so, ideally, we want to partition the input circuit so that the \( S_{L,\text{CNOT}} \) segments are large.

To do so, we use a simple heuristic technique: first, naively partition the input circuit. Say that the size of \( C \), excluding \( H \) gates, is \( n \). Then, for \( i = n \) to 1, commute gate \( v_i \in \{\text{CNOT}, S, T, S^\dagger, T^\dagger\} \) forward through the circuit until reaching a gate with which it does not commute. Keep track of the largest segment \( S_{\text{max,\text{CNOT}}} \) that \( v_i \) can belong to. Once reaching the end of the circuit or a non-commuting gate, insert \( v_i \) into \( S_{\text{max,\text{CNOT}}} \). Once \( v_1 \) has been reached, repeat this process but in the opposite direction, from \( i = 1 \) to \( n \), this time commuting backwards instead of forwards.

The output circuit could then be further optimized using methods that preserve the allowed two-qubit gates, based on templates, for example, or those that dynamically re-allocate physical and logical qubits [14–16]. Of course, our method works best when the segments consisting of CNOT gates are large (many important circuits, such as quantum Fourier transform, fall under this category, increasingly so as the number of qubits increases [17]). The results are shown in figure 14 compared to IBM’s Qiskit transpiler and demonstrate that for input circuits with \( \leq 0.05–0.07 \) Hadamard to CNOT ratio, this method consistently outperforms the Qiskit compiler, while it does increasingly worse as the ratio grows larger. The input circuits have 1000 gates and do not take into account connectivity. To generate the initial circuit, each gate is chosen from the set \( \{\text{CNOT}, S, T, S^\dagger, T^\dagger, H\} \).

Figure 14. Using the method described in section 4, then by generating circuits from the set \( U \) with varied Hadamard to CNOT gate ratios, we can clearly see that while the method works well compared to IBM’s compiler for circuits that are mainly composed of CNOT gates, its performance decreases as the ratio of Hadamard to CNOT gates increases. Red solid circles represent data points in which our scheme over-performs Qiskit, whereas the blue solid circles represent data points in which our scheme performs worse than Qiskit. The ‘sweet-spot’ seem to be around 5%–7% Hadamard to CNOT ratio.
with respective probabilities $\{p_{\text{CNOT}}, p_{S}, p_{T}, p_{S^t}, p_{T^t}, p_{H}\}$. For this experiment, $p_S = p_T = p_{S^t} = p_{T^t} = 0.01$, $p_H \in [0, 0.2]$, and $p_{\text{CNOT}} = 1 - \sum_{i \in \{S,T,S^t,T^t,H\}} p_i$.

5. Conclusions and open questions

We constructed a circuit synthesis scheme that takes as input the qubit connectivity graph and a quantum circuit over the gate set generated by $\{\text{CNOT}, R_Z\}$ and outputs a circuit that respects the connectivity of the device. We applied our techniques to Google’s Bristlecone 72-qubit quantum chip connectivity, IBM’s Tokyo 20-qubit quantum chip connectivity, and Rigetti’s Acorn 19-qubit quantum chip connectivity. We also compared the performance of our methods as a function of sparseness of random quantum circuits of 20 qubits.

Since in practice different CNOT gates can be affected by different amount of noise, an idea for further work would be to weight the edges based on the error rate of the CNOT gate between the respective qubits. Techniques adapted from [4] could potentially be integrated into the methods given in this paper to produce circuits with lower error rates. In addition, we plan to improve on efficiency and quality of the results produced by our scheme.

We show how the method can be applied to broader classes of circuits comprising of universal set of gates, however our scheme performs (as expected) less optimally than compilers designed specifically for that task, while over-performing the latter for circuits comprising of $\{\text{CNOT}, R_Z\}$.

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Appendix. Example

Figure A1. Worked through example of circuit synthesis producing the linear transformation given figure 3(a) on connectivity given in figure 3(b). Fully synthesized circuit can be produced by putting together the gates from steps 8–11 and switching the controls and targets, then putting together the gates from steps 1–7 and reversing them, leaving the controls and targets as shown.
ORCID iDs

Vlad Gheorghiu @ https://orcid.org/0000-0002-4172-9186

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