Measuring the Capabilities of Quantum Computers

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A quantum computer has now solved a specialized problem believed to be intractable for supercomputers, suggesting that quantum processors may soon outperform supercomputers on scientifically important problems. But flaws in each quantum processor limit its capability by causing errors in quantum programs, and it is currently difficult to predict what programs a particular processor can successfully run. We introduce techniques that can efficiently test the capabilities of any programmable quantum computer, and we apply them to twelve processors. Our experiments show that current hardware suffers complex errors that cause structured programs to fail up to an order of magnitude earlier — as measured by program size — than disordered ones. As a result, standard error metrics inferred from random disordered program behavior do not accurately predict performance of useful programs. Our methods provide efficient, reliable, and scalable benchmarks that can be targeted to predict quantum computer performance on real-world problems.

Quantum processors are on the verge of realizing their promise to revolutionize computing. A quantum processor has now executed programs believed to defy classical simulation [1], and many hybrid quantum/classical algorithms have appeared that offer the possibility of near-term computational advantage [2]. Publicly available quantum processors continue to proliferate, and with them a widespread interest in running application-inspired quantum programs. But contemporary quantum processors are plagued by errors that will cause many of these programs to fail. Existing tools for characterization and benchmarking [1, 3–14] probe the magnitude and type of these errors. But none of them provide direct insight into a processor’s capability — the programs it can run successfully — and most are not practical on devices that are large enough to potentially demonstrate a quantum advantage. In this work we introduce the first scalable benchmark that is able to efficiently probe and summarize the capability of any gate-model quantum computer, and we present the first systematic study of the capabilities of publicly accessible quantum processors.

The errors suffered by multi-qubit quantum processors are complex and varied, often including effects such as crosstalk [15], coherent noise [16–18], and drift [19, 20]. Simple models for device performance that ignore this complexity offer inaccurate predictions, while complex models are generally intractable to learn or computationally taxing to use. Instead, we argue that the capability of a processor is best probed by running a set of representative test quantum programs whose measured output can be verified classically.

While several benchmarks have been proposed, few are efficiently verifiable. IBM’s quantum volume benchmark [5], like many application-derived benchmarks [10–12], becomes infeasible to verify by classical simulation as the number of qubits grows. Google leveraged the extreme difficulty of verifying the results of their cross-entropy benchmarking circuits to demonstrate “quantum supremacy” [1, 3, 4]. Other benchmarks present different problems. For example, Clifford randomized benchmarking [6–8] uses a class of programs that, while efficiently verifiable, require so many gates when compiled on more than 3-5 qubits that they almost never run correctly on today’s processors [9]. Moreover, all of these benchmarks rely strictly on randomized, disordered programs. This limits their sensitivity to coherent noise [17], and so they are unlikely to reflect the performance of structured programs that implement quantum algorithms.

We solve all of these problems by introducing a family of benchmarks that can probe the capability of any gate-model quantum processor — including large ones capable of quantum advantage. To build these benchmarks, we begin with quantum circuits of varied sizes and structures that constitute challenging tasks for a processor. Then we apply a procedure called “mirroring” [21] that transforms any circuit \(C\) into a related suite \(\{M_C\}\) of “mirror circuits” that are efficiently verifiable (see Fig. 1a). Mirroring concatenates the original circuit \(C\) with a quasi-inverse \(C^{-1}\) that reverses \(C\) up to a Pauli operation, and inserts special layers of operations before, after, and between \(C\) and \(C^{-1}\). Quasi-inversion, inspired by the Loschmidt echo [22] and early work on randomized benchmarking [7, 8], ensures that each \(M_C\) has a definite and easily verified target output, while the extra layers preserve the original circuit’s sensitivity to errors so that performance on \(\{M_C\}\) faithfully represents performance on \(C\). Unlike test circuits that yield high-entropy target distributions [4, 5], a mirror circuit’s performance is easily quantified by the probability \(S\) of observing the ideal outcome.

Mirror circuit benchmarks measure – and inform prospective programmers about — a processor’s capability to run specific programs (quantum circuits), rather than its ability to produce specific distributions [1] or unitary transformations [5]. The properties probed by such a benchmark are determined by the properties of the circuits in it. Mirror circuits can be efficiently constructed from circuits involving any number of qubits (circuit width, \(w\)) and logical cycles (circuit depth, \(d\)). They can have any structure, enabling construction of benchmarks that serve as proxies for any quantum program. We built benchmarks from disordered (Fig. 1b) and highly structured (Fig. 1c) circuits, using gates that respect each processor’s connectivity, to probe different aspects of performance.

We ran randomized mirror circuit benchmarks [23] on twelve publicly accessible quantum computers from IBM [24] and Rigetti Computing [25]. Their measured capabilities are displayed in Fig. 1d, using the framework of volumetric
A scalable method for benchmarking a quantum computer’s capability. (a) Mirror circuits — quantum circuits with a reflection structure — can be used to efficiently benchmark arbitrarily large quantum computers, because without errors they output a unique and easy-to-calculate bit string. Mirror circuits can be constructed from (b) random disordered logic gate sequences; (c) ordered, periodic sequences; or (not shown) quantum algorithm kernels. (d) The results of running randomized mirror circuits of varied shapes on twelve quantum computers from IBM and Rigetti Computing (schematics show device layouts, dates when the experiments were performed). Each circuit’s success probability $S$ is estimated from $\sim 1000$ circuit repetitions and rescaled to $P = (S - 1/2^w)/(1 - 1/2^w)$ where $w$ is the circuit’s width. The maximum, minimum and mean of $S$, over 40 circuits run at each width and depth, is shown for each device. Green, black, and red lines (respectively) show the frontiers at which these statistics drop below $1/e \approx 0.37$. The maximum and minimum frontiers are calculated so that any discrepancy between them is statistically significant at $p = 0.05$.

We probed each device at exponentially spaced ranges of circuit widths $w$ and benchmark depths $d$ [27], and for each width $w$ we tested several different embeddings of $w$ qubits into the available physical qubits. For each $d$, $w$, and embedding we ran 40 randomized mirror circuits. For each shape $(w,d)$, Fig. 1d shows the best, worst, and average case polarization $P = (S - 1/2^w)/(1 - 1/2^w)$ for the best-performing $w$-qubit embedding. The polarization $P$ is a rescaling of the success probability $S$ that corrects for few-qubit effects. For example, $S = 1/2$ is reasonably good performance for a width-10 circuit ($P \approx 1/2$) but represents total failure for a width-1 circuit ($P = 0$).

The volumetric benchmark plots [26] displayed in Fig. 1d provide an at-a-glance summary of these devices’ capabilities to run random disordered circuits. They also encode considerable detail about the nature of the errors that limit capability. The mean polarization at each shape indicates the expected performance of a random circuit of that shape, and it is closely related to the fidelity of the logic gates (a standard measure of gate quality). The maximum and minimum polarization, $P_{\text{max}}$ and $P_{\text{min}}$, provide estimates of best- and worst-case capability, and their difference captures the variability — how reliably do width and depth predict whether a random circuit will succeed? A large difference implies that whether a circuit can be successfully run on that processor depends not only on the circuit’s shape, but also on its exact arrangement of gates, i.e., its structure. Our experiments reveal that certain processors’ performance is strongly structure-dependent (e.g., Aspen 6) whereas other processors’ performance is nearly structure-invariant (e.g., Vigo). This is highlighted by comparing the dotted lines in Fig. 1d that show the frontiers beyond which $P_{\text{min}}$ (red) and $P_{\text{max}}$ (green) fall below $1/e$ [28]. When a processor’s performance is strongly structure-dependent, standard metrics derived from the average performance of random circuits [4–6] will not reliably predict whether it can successfully run any particular randomly sampled circuit.

The success probability of a quantum circuit is dictated by a complex interplay between the structure present in that circuit and the structure of the errors. If errors are completely structureless (i.e., global depolarization), all circuits of a given shape will have the same success probability. But structureless errors are rare in quantum hardware. Error rates vary across qubits and noise is often correlated in time or space. Our results for randomized circuits provide a glimpse of this interplay. But random circuits are inefficient probes of structured errors [17], because a typical randomized mirror circuit
is almost completely disordered in space and time (Fig. 1b). To study the effects of structure, we can incorporate explicit long-range order, such as periodic arrangements of gates, into mirror circuits (Fig. 1c). Periodic mirror circuits can be extremely sensitive to structured errors, supporting linear growth of coherent errors [29] just as ordered lattice systems support ballistic transport of excitations [30].

To investigate the interplay between circuit and error structures in real hardware, we benchmarked eight quantum processors using mirror circuits both with and without long-range order. We used periodic mirror circuits constructed by repeating a short unit cell of circuit layers (Fig. 1c) selected so that every circuit with \( w > 1 \) had a two-qubit gate density of \( \xi \approx 1/8 \). Concurrently, we ran similar but randomized mirror circuits, sampled so that \( \xi = 1/8 \) in expectation. All circuits have \( \xi \leq 1/2 \), and deviations from \( \xi = 1/8 \) are small circuit-size effects. We sampled and ran 40 circuits of each type at a range of widths and depths, using the best qubits according to the manufacturer’s published error rates [31]. Results for four representative devices [32] are summarized in Fig. 2.

We found that the worst-case performance \( (P_{\text{min}}) \) of periodic circuits was worse than that of disordered circuits for every processor, as shown in Fig. 2a. For some processors, the difference is dramatic — e.g., Aspen 4 ran every width-1 disordered circuit up to depth 128 successfully \( (P \geq 1/e) \), but failed on periodic circuits of depth 32. We conclude that testing a processor with disordered circuits cannot reliably predict whether that processor will be capable of running circuits with long-range order. Since circuits for quantum algorithms typically have long-range order, benchmarks like periodic mirror circuits are needed to predict the performance of algorithmic circuits [33].

We used our benchmarks to investigate one final question: can conventional error rates be used to predict a processor’s capability? IBM and Rigetti publish an error rate for each logic operation \( (\text{gates and readouts}) \) in each device, updated every day after recalibration [24, 25]. The presumption that these error rates can be used to accurately predict circuit success probabilities is the grounds for interpreting them as a measure of device quality. We recorded these error rates at the time of our experiments, and used them to predict the success probability for every circuit that we ran [34]. Fig. 2c shows a scatter plot comparing this prediction to experimental observations. In every case, the observed failure rates are dispersed widely around the prediction. This confirms the presence of unmodeled structure in the errors. The predictions are also biased towards over-optimism, suggesting the existence of significant error sources that are not captured by the error rates. Comparing Figs. 2a and 2b shows that, for every device, the observed worst-case performance is significantly worse than the performance predicted using published error rates. However, those error rates do not appear to be wrong — they correctly predict the average performance of one- and two-qubit disordered circuits in most cases. Instead, we conclude that these discrepancies stem from unmodeled structure. Structured errors affect structured and disordered circuits differently, and this cannot be captured by simple error rates.

The discrepancy between our observations and the predictions of the error rates reveals the types of structure present in the errors. All tested processors display performance that declines faster with circuit width than the error rates predict. This is a signature of crosstalk [26]. Similarly, the worst-case success rate of periodic circuits decays faster with depth than predicted, and than observed for disordered circuits. This is a signature of coherent errors [26, 29]. Mirror circuits with configurable structure are a simple tool for measuring the impact of these errors in large circuits like those needed for algorithms, so that they can be quantified and suppressed (e.g., with better calibrations) as necessary.

We have shown how to use mirror circuit benchmarks for detailed analysis of quantum processors’ performance. But our original goal was to capture performance in a simple and intuitive way. So, in Fig. 3, we concisely summarize the performance of all eight devices tested with both kinds of mirror circuits, by dividing the circuit width \( \times \) depth plane into

![Figure 2. Randomized benchmarks do not predict structured circuit performance.](image-url)
“success”, “indeterminate”, and “fail” regions. They correspond to the circuit shapes at which (respectively) all, some, and none of the test circuits succeeded ($P \geq 1/\xi$). These empirical capability regions allow potential users to predict what circuits a processor is likely to be capable of running. A circuit whose shape falls into a processor’s “success” or “fail” regions is likely to succeed or fail (respectively), because the test circuits probe both extremes of performance by including a variety of disordered and periodic circuits at each circuit shape. Conversely, a processor’s ability to successfully run a specific circuit whose shape falls within its “indeterminate” region depends unavoidably on that circuit’s structure. Capability regions depend on two-qubit gate density ($\xi \approx 1/\sqrt{s}$ in Fig. 3) and the threshold for success ($1/\xi$ in Fig. 3), and can be easily adapted to particular applications by setting these parameters.

Quantum computational power is a double-edged sword. The infeasibility of simulating quantum processors with 50+ qubits offers the possibility of computational speedups [1, 2], but simultaneously poses real problems for testing and assessing their capability. As processors grow, users and computer engineers will need scalable, efficient and flexible benchmarks that can measure and communicate device capabilities. Mirror circuit benchmarks demonstrate that this is possible, and highlight the scientific value of carefully designed benchmarks.

Figure 3. Empirical capability regions. The circuit shapes at which all (green), some (orange), and none (white) of the test circuits succeeded ($S \geq 1/\xi$). The test circuits have a two-qubit gate density of $\xi \approx 1/\sqrt{s}$. If a target circuit with $\xi \approx 1/\sqrt{s}$ lies in the green (white) region for a particular processor, then that processor will likely (not) execute the circuit successfully. Processor performance on circuits in the orange region is unpredictable.

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Our circuit mirroring technique is introduced in detail in Appendix IV.

The structure in algorithm circuits can be reduced using a variety of randomization techniques [35, 36], but it is not possible to remove all structure in algorithm circuits.

A complete definition of randomized mirror circuits and the sampling distributions used in this experiment are given in Appendix V. Experimental details are given in Appendix VIII.

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All circuits within a benchmark share a fixed O(1) number of overhead layers; a mirror circuit’s benchmark depth counts only its non-overhead layers, and it equals twice the depth of the original circuit. This is explained further in the appendices.

The $\frac{1}{2}$ threshold is arbitrary but convenient; under a simple, naive error model where each gate fails with probability $\epsilon < 1$, the frontier will include all circuits of size $\leq \frac{1}{2}$. The maximum and minimum frontiers are calculated so that any discrepancy between them is statistically significant at $p = 0.05$. The details of the statistical analysis are given in Appendix VIII.

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A complete definition of randomized mirror circuits, periodic mirror circuits, and the sampling distributions used in this experiment are given in Appendices V and VI. Experimental details are given in Appendix IX.

The results for all eight processors are included in Appendix IX.

The structure in algorithm circuits can be reduced using a variety of randomization techniques [35, 36], but it is not possible to remove all structure in algorithm circuits.

The method used to calculate these predictions is given in Appendix VII.

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I. OVERVIEW OF THE APPENDICES

In the main text, we used mirror circuit benchmarks to probe quantum computers’ capabilities. In these appendices:

1. We explain why mirror circuits constitute a good benchmark.

2. We detail our experiments and data analysis.

In this overview we explain what kind of benchmark we seek to construct, we list desiderata for such a benchmark, and we provide a guide for the remainder of these appendices.

A. The kind of benchmark we constructed

Benchmarking a device means commanding it to perform a set of tasks, and measuring its performance on them. The measured performance should be meaningful. Prospective users should be able to extrapolate straightforwardly, from benchmark results, approximately how well the device would perform on their use cases. But devices can be used in different ways, and for different tasks. Distinct use cases require distinct benchmarks. For example, a quantum computer can be commanded to (1) run a particular circuit, (2) apply a particular unitary, or (3) generate samples from a particular distribution. These task classes are categorically distinct, but each has real-world relevance. Google, in their demonstration of quantum supremacy [1], benchmarked their Sycamore chip (against a supercomputer) by its performance at sampling a distribution. IBM’s quantum volume benchmark [5] challenges quantum processors to perform specific unitaries, and cautions that it’s cheating to sample from the resultant distribution without performing the specified unitary. Randomized benchmarking [6, 9, 37] commands a processor to run specific circuits, each one of which produces a trivial unitary and a trivial distribution. These illustrate three different ways that a quantum processor’s task can be defined.

Here, we have adopted the third approach. We benchmark processors by specifying concrete circuits, not unitaries or distributions. Therefore, these benchmarks measure a processor’s ability to run circuits. Their results should enable users to predict how well that processor will run other circuits with similar properties. Relative to the other paradigms mentioned above, this approach emphasizes the reliability of the processor’s gates. Our paradigm isolates that aspect of performance from other properties, like qubit connectivity, gate set expressiveness, or the performance of a processor’s classical compilation software. Such benchmarks are and will be particularly useful to low-level quantum programmers who express their programs or algorithms as concrete circuits made of native gates, and then wish to predict how large a circuit can be run. Benchmarks rooted in the other paradigms mentioned above are complementary, emphasizing other aspects of performance. No single benchmark or paradigm is sufficient to capture all use cases.

B. Desiderata for benchmark circuits

The specific benchmarks we use in the main text are particular cases produced by a general process. This process is designed to generate a set of circuits suitable for benchmarking from one or more exemplar circuits C that represent a particular use case. A good question to ask is “If C is a representative circuit, why not simply run C itself as a benchmark?” Doing this presents two problems.

First, since the point of a benchmark is to measure performance, we must be able to evaluate how well or accurately a given processor has run our benchmark circuits. For many interesting and representative circuits, this is or will be impractical because good quantum algorithms can generate results that aren’t classically simulable, and/or solve problems outside of NP (i.e., the result is not efficiently verifiable).

Second, many circuits C are intrinsically subroutines, whose performance we wish to predict in contexts (i.e., within larger programs) that are a priori unknown or only partially known. A benchmark needs to run C in context — at a minimum, after state initialization and before measurement of all the qubits — and a good benchmark must place it in representative contexts, so that users can infer or predict how it is likely to perform in the specific context of their use cases. Even when C is not a subroutine, but a full algorithm that defines its own context, the transformations required to make it easy-to-verify (solving the first problem above) can change that context, requiring additional work to ensure that C’s performance is probed in contexts that are representative of its original function.

To solve these problems, we need a process that transforms a user-specified circuit C into a set of circuits or test suite $S(C)$, that can be run exhaustively or sampled from, and which satisfies the following key desiderata:

1. Even if C is a subroutine that needs to be embedded into a larger circuit, every circuit in $S(C)$ has a fully specified context including state initialization and measurement.
2. Each circuit in $\mathcal{S}(C)$ has a well-defined and easy to simulate target output, which it would produce if implemented without errors, so that the performance of an imperfect implementation can be measured straightforwardly.

3. The success probabilities of the circuits in $\mathcal{S}(C)$ are representative of how $C$ would perform in the context[s] where it might be used (which may be unknown).

C. Mirror circuit benchmarks

We have developed a set of circuit transformations, collectively called mirroring, that generate a set of benchmarking circuits from a user-specified circuit $C$, and that can be used to satisfy the above desiderata. These transformations generate mirror circuit benchmarks. In our experiments we ran two particular types of mirror circuit benchmark: randomized mirror circuits and periodic mirror circuits. Appendices II-VI are dedicated to introducing these benchmarking methods:

- In Appendix II we introduce our notation and definitions, and review the background material required to present both our benchmarking methods and the theory supporting them.

- In Appendix III we discuss the relative merits of defining benchmarking circuits over a standardized gate set versus over a gate set that is native to a particular processor, and we specify the approach that we take in our experiments.

- In Appendix IV we introducing our mirroring circuit transformations, and show how and why they satisfy the above desiderata.

- In Appendix V we introduce randomized mirror circuits, and the particular types of randomized mirror circuits used in our experiments.

- In Appendix VI we introduce periodic mirror circuits, and the particular type of periodic mirror circuits used in our experiments.

Although Appendices II-VI discuss certain aspects of our experiments, they are primarily focused on describing our benchmarking methods in a general way that is applicable to almost any quantum computer. The final three Appendices focus on our particular experiments and the corresponding data analysis:

- In Appendix VII we explain how we used each processor’s published error rates to predict the success probabilities of the mirror circuits that we ran.

- In Appendix VIII we detail the randomized mirror circuit experiment, and the corresponding data analysis, that is summarized in Fig. 1d of the main text. We will refer to this as experiment #1 throughout these appendices.

- In Appendix IX we detail the randomized and periodic mirror circuits experiment, and the corresponding data analysis, that is summarized in Figs. 2 and 3 of the main text. We will refer to this as experiment #2 throughout these appendices.

It is not necessary to read these appendices in chronological order. Each appendix has been written to be as self contained as possible.

II. DEFINITIONS

The purpose of this appendix is to define our notation and review the background material required throughout these appendices.

A. Quantum circuits

We use quantum circuits extensively in this paper, to define tasks and programs for quantum computers. Quantum circuits have been used so ubiquitously in the literature, for so many purposes, that it is difficult to define them in a simple yet universally valid way. Broadly speaking, a quantum circuit describes a (possibly complex) operation to be performed on a quantum computer, by specifying an arrangement of "elementary" operations (e.g., logic gates or subroutines) in sequence or in parallel, which if performed on the quantum computer will transform its state in a particular way. All the circuits that we consider in this paper can be represented, and implemented, as a series of layers.

1. Logic layers and unitaries

A $w$-qubit logic layer is an instruction to apply physical operations that implement a particular unitary evolution on $w$ qubits. We denote the unitary corresponding to $L$ by $U(L) \in \text{SU}(2^w)$. Here $\text{SU}(2^w)$ denotes the $2^w$-dimensional special unitary group represented as matrices acting on the $2^w$-dimensional complex vector space $\mathcal{H}_w$ of pure $w$-qubit quantum states. It will also often be convenient to use the superoperator representation of a unitary, so we define $\mathcal{U}(L)$ to be the linear map

$$\mathcal{U}(L)[\rho] := U(L)\rho U(L)^\dagger,$$

where $\rho$ is a $w$-qubit density operator (a unit-trace positive semi-definite operator on $\mathcal{H}_w$), representing a general $w$-qubit quantum state. We consider a logic layer $L$ to be entirely defined by the unitary $U(L)$, so — by definition — there is only one logic layer corresponding to each unitary. There will usually be many ways to implement a particular layer. Our methods are entirely agnostic as to how a layer is implemented, except that an attempt must be made to faithfully implement the unitary it defines. We use $L^{-1}$ to denote the logic layer satisfying

$$U(L^{-1}) = U(L)^{-1}.$$
There are two additional, special layers that can appear in our quantum circuits: an initialization or state preparation layer \( I \) that initializes all qubits in the \( |0\rangle \) state, and a readout or measurement layer \( R \) that reads out all qubits in the computational basis, producing a classical bit string and terminating the circuit. Initialization can only appear as the first layer in a circuit, and readout can only appear as the last layer. These layers are not unitary, and \( U(\cdot) \) is not defined for them.

2. Quantum circuits

A quantum circuit \( C \) over a \( w \)-qubit logic layer set \( \mathbb{L}_w \) is a sequence of \( d \geq 0 \) logic layers that are all elements from \( \mathbb{L}_w \). We will write this as

\[
C = L_dL_{d-1} \cdots L_2L_1,
\]

where each \( L_i \in \mathbb{L}_w \), and we use a convention where the circuit is read from right to left. The circuit \( C \) is an instruction to applying its constituent logic layers, \( L_1, L_2, \ldots, \) in sequence. For the benchmarking purposes that we are concerned with in this paper, operations across multiple layers must not be combined or compiled together by implementing a physical operation that enacts their composite unitary. This notion of strict “barriers” between circuit layers is required in many benchmarking and characterization methods [6, 29, 38], and we use it throughout this work.

We consider two categories of quantum circuits, which have significantly different roles. Quantum input / quantum output (QI/QO) circuits do not use the initialization or readout layers. Fixed input / classical output (FI/CO) circuits begin with an initialization layer, and end with a readout layer. There is a canonical mapping from QI/QO circuits to FI/CO circuits (by adding the initialization and readout layers) and back (by stripping them off).

QI/QO circuits generally appear as subroutines. A QI/QO circuit \( C \) encodes a unitary map \( U(C) \) on \( w \) qubits given by

\[
U(C) = U(L_d) \cdots U(L_2)U(L_1).
\]

FI/CO circuits represent complete, runnable programs. A FI/CO circuit \( C \) encodes a probability distribution

\[
\Pr(x | C) = | \langle x | U(L_d) \cdots U(L_2)U(L_1) | 0 \rangle |^2,
\]

over length-\( w \) classical bit-strings, \( x \).

3. Circuit width, depth, size and shape

The circuit \( C = L_dL_{d-1} \cdots L_2L_1 \) defined over the \( w \)-qubit layer set \( \mathbb{L}_w \) has

- a width of \( w \),
- a depth of \( d \),
- a size of \( wd \), and
- a shape of \((w,d)\).

The depth of a circuit is defined explicitly with respect to that circuit’s specific layer set \( \mathbb{L}_w \). Each specific quantum processor has a “native” layer set, generally corresponding to logic layers that can be implemented in a single unit of time. For most processors, each native layer is some combination of one- and two-qubit gates in parallel. We do not assume that every layer in the set \( \mathbb{L}_w \) is native, nor that it can even be implemented with a short sequence of the native logic layers. So implementing a circuit of depth \( d \) could require many more than \( d \) units of physical time.

Every (circuit paradigm) benchmark is defined by a set of circuits, and for every benchmark there is a set of “overhead” layers that are common to, and shared by, every circuit in the benchmark. At a minimum, this overhead includes initialization and readout layers. Therefore, in the context of a specific benchmark, we define three different depths for a circuit:

1. The full depth \( d_0 \) of a circuit is the total number of layers, including initialization and readout, as defined above.
2. The benchmark depth \( d \) of a circuit is the total number of non-overhead layers, \( d = d_0 - \text{const} \), where the constant is the same for every circuit in a benchmark.
3. The physical depth of a circuit is the total time taken to run a circuit assuming that every gate can be performed in single clock cycle (a single unit of time). Because this can depend strongly on hardware constraints, such as restrictions on parallelism, we do not use the physical depth in this work.

The circuit mirroring procedure that we discuss below typically adds overhead layers, and in our experiments there are five overhead layers (initialization, readout, and three extra logic layers). In the main text, we report the benchmark depth defined by \( d = d_0 - 5 \).

4. Pauli layers

The \( w \)-qubit Pauli layers \( \mathbb{P}_w \) are the \( 4^w \) logic layers that instruct the processor to implement \( w \)-fold tensor products of the four standard Pauli operators \( I, X, Y \) and \( Z \). For all \( Q_1, Q_2 \in \mathbb{P}_w \),

\[
U(Q_2Q_1) = U(Q_3)
\]

for some \( Q_3 \in \mathbb{P}_w \), i.e., \( U(\mathbb{P}_w) \) is a group, where \( U(\mathbb{L}) := \{U(L)\}_{L \in \mathbb{L}} \) for any layer set \( \mathbb{L} \). The Pauli operators induce bit flips and/or phase-flips on the qubits. So, if

\[
U(L_dL_{d-1} \cdots L_2L_1) = U(Q)
\]

for some Pauli layer \( Q \in \mathbb{P}_w \), then the circuit \( C = RL_dL_{d-1} \cdots L_2L_1I \) will deterministically output a \( w \)-bit string that is specified by \( Q \). This is a property that holds for all our benchmarking circuits. For any such circuit, its target bit string is the unique \( w \)-bit string that the circuit will output if it is implemented perfectly.
5. Clifford layers and circuits

All the benchmarking circuits in our experiments contain only Clifford layers. A \( w \)-qubit logic layer \( L \) is a Clifford layer if, for each \( Q \in \mathbb{P}_w \),

\[
\mathcal{U}(LQI^{-1}) = \mathcal{U}(Q')
\]

for some Pauli layer \( Q' \in \mathbb{P}_w \) [39]. Note that the Pauli layers are also Clifford layers, and \( \mathcal{U}(\mathbb{C}_w) \) is a group where \( \mathbb{C}_w \) denotes the set of all \( w \)-qubit Clifford layers. If a circuit contains only Clifford layers we refer to it as a Clifford circuit.

B. Modeling quantum processors

In these appendices we will show how a processor’s performance on our mirror circuit benchmarks depends on the magnitude and type of the imperfections in that processor. Here we introduce our notation for modeling errors in quantum processors, and review the relevant standard definitions.

1. The Markovian error model

We will use \( \Lambda(\cdot) \) to map from instructions — layers or circuits — to a mathematical object that models a processor’s implementation of that instruction. In particular:

- For a FI/CO circuit \( C \), \( \Lambda(C) \) is the distribution over \( w \)-bit strings that each run of \( C \) on that processor is sampling from.

- For a QI/QO circuit \( C \), \( \Lambda(C) \) denotes a map from \( w \)-qubit quantum states to \( w \)-qubit quantum states.

Our theory will use the Markovian error model [40] in which

- \( \Lambda(I) \) is a fixed \( w \)-qubit density operator.

- For any unitary logic layer \( L \), \( \Lambda(L) \) is a fixed completely positive and trace preserving (CPTP) linear map from \( w \)-qubit density operators to \( w \)-qubit density operators.

- \( \Lambda(R) \) is a positive-operator valued measure (POVM), i.e.,

\[
\Lambda(R) = \{ \Lambda(R)_b \}_{b \in \mathbb{B}_w},
\]

where \( \mathbb{B}_w \) is the set of \( w \)-bit strings, the \( \Lambda(R)_b \) are positive operators, and \( \sum_b \Lambda(R)_b = I \).

The map implemented by a QI/QO circuit \( C = L_d \cdots L_2 L_1 \) is then

\[
\Lambda(C) = \Lambda(L_d) \cdots \Lambda(L_2) \Lambda(L_1),
\]

where we have denoted composition of linear maps by multiplication (i.e., \( \Lambda(L') \Lambda(L) \) represents the composition of the two linear maps).

Similarly, for a FI/CO circuit \( C = RL_d \cdots L_2 L_1 I \), \( \Lambda(C) \) is a probability distribution over \( w \)-bit strings where the probability of the bit-string \( b \) is

\[
\Lambda(C)_b = \text{Tr} \left[ \Lambda(R)_b \Lambda(L_d) \cdots \Lambda(L_1) \Lambda(I) \right],
\]

This error model can describe many common error modes in quantum processors — including local coherent, stochastic and amplitude damping errors, as well as complex many-qubit errors like stochastic or coherent crosstalk [15, 40].

2. Stochastic Pauli channels

Stochastic Pauli channels, and the special case of depolarizing channels, will have an important role in our theory of mirror circuit benchmarks. A \( w \)-qubit stochastic Pauli channel is parameterized by a probability distribution over the \( 4^w \) Pauli operators: \( \{ \gamma_Q \}_{Q \in \mathbb{P}_w} \) with \( \sum_{Q \in \mathbb{P}_w} \gamma_Q = 1 \) and \( \gamma_Q \geq 0 \). The stochastic Pauli channel specified by \( \{ \gamma_Q \} \) has the action

\[
\mathcal{E}_{\text{pauli},\{\gamma_Q\}}[\rho] := \sum_{Q \in \mathbb{P}_w} \gamma_Q U(Q) \rho U(Q)^{-1}.
\]

A \( w \)-qubit depolarizing channel \( \mathcal{D}_{\text{w,\text{dep}}}(\rho) \) is a special case of a stochastic Pauli channel that is parameterized only by an error rate \( \epsilon \):

\[
\mathcal{D}_{\text{w,\text{dep}}}(\rho) := (1 - \epsilon) \rho + \frac{\epsilon}{4^w - 1} \sum_{Q \in \mathbb{P}_w} U(Q) \rho U(Q)^{-1},
\]

where \( \mathbb{P}_w,\text{err.} \) is the Pauli layers excluding the identity Pauli layer.

A \( w \)-qubit depolarizing channel is not the \( w \)-fold tensor product of one-qubit depolarizing channels, that is, \( \mathcal{D}_{\text{w,\text{dep}}} \neq \mathcal{D}_{\text{1,\text{dep}}}^{\otimes w} \) for any \( \epsilon' \) except for the special cases of the identity channel \( \epsilon = 0 \) and the maximally depolarizing channel \( \epsilon = (4^w - 1)/4^w \). A \( w \)-qubit depolarizing channel induces highly correlated errors, whereas the \( w \)-fold tensor product of one-qubit depolarizing channels induces independent errors.

3. Process fidelity

As we will show later, performance on our mirror circuit benchmarks have a relationship to the fidelity of the processor’s implementation of the circuit[s] from which that benchmark was constructed, via “mirroring.” There are two commonly used definitions for the “process fidelity” — the average fidelity and the entanglement fidelity. The average fidelity \( (F_{\text{av}}) \) of a \( w \)-qubit process \( \mathcal{E} \) to the identity process is defined by [41]

\[
F_{\text{av}}(\mathcal{E}) := \int d\psi \langle \psi | \mathcal{E}[\psi] | \psi \rangle | \psi \rangle | \psi \rangle,
\]

where the integral is over the unique SU(\( 2^w \))-invariant measure on pure states. The entanglement fidelity \( (F_{\text{e}}) \) is defined by [41]

\[
F_{\text{e}}(\mathcal{E}) := \langle \psi_e | (\mathcal{E} \otimes I)[| \psi_e \rangle \langle \psi_e |] | \psi_e \rangle,
\]

where \( \psi_e \) is the maximally entangled state of two \( w \)-qubit states.
where $I$ is the $w$-qubit identity superoperator (i.e., $I[\rho] = \rho$), and $|\psi_0\rangle$ is any maximally entangled state in $H_w \otimes H_w$. The entanglement and average fidelity are related via [41]:

$$F_{e}(\mathcal{E}) = (1 + 1/z^2) F_{a}(\mathcal{E}) - 1/z^2.$$ \hfill (16)

The average infidelity ($\epsilon_a$) and entanglement infidelity ($\epsilon_e$) are simply defined by

$$\epsilon_a(\mathcal{E}) := 1 - F_{a}(\mathcal{E}),$$ \hfill (17)

$$\epsilon_e(\mathcal{E}) := 1 - F_{e}(\mathcal{E}).$$ \hfill (18)

Although the average fidelity is more widely used in the literature, for our purposes the entanglement fidelity is more relevant. This is because $F_e$ accounts for errors that are only apparent when a circuit is used as a subroutine inside a circuit on more qubits, whereas $F_a$ does not (note that $F_e < F_a$, unless $F_a = F_e = 0$ or 1). Therefore, this is the definition that we use for ‘the process infidelity’. The entanglement infidelity of a stochastic Pauli channel has a simple and intuitive property: it is equal to the probability that the channel induces any Pauli error, i.e.,

$$\epsilon_e(\mathcal{D}_{\text{pauli}}, |\psi_0\rangle) = \sum_{Q \in \mathcal{D}_{\text{pauli}}} \gamma_Q.$$ \hfill (19)

In the special case of a depolarizing channel, $\epsilon_e(D_\text{w,1}) = \epsilon$.

**III. VOLUMETRIC CIRCUIT BENCHMARKS**

The benchmarks constructed and deployed in this paper are examples of volumetric benchmarks [26]. This means that each circuit in the benchmark has a well-defined width $w$ and depth $d$, that circuits with a range of $w$ and $d$ are selected, and that the data analysis sorts those circuits by $w$ and $d$. Therefore, it is essential that the nature of these circuits and the precise operational meaning of width and depth be stated clearly. A circuit’s width is the number of qubits required to run it, and its depth is the number of layers that appear in it. But both of these definitions are subject to non-obvious subtleties, especially depth. Depth is defined with respect to a particular set of logic operations (see Appendix II A 3). Therefore, the benchmarking analysis depends critically on which set of logic layers were used to define the benchmark circuits. The purpose of this appendix is to discuss several ways to choose layer sets, and then to describe the layer sets used in our experiments.

**A. Constructing layer sets from gate sets**

Layers are just instructions defining $w$-qubit unitary operations (see Appendix II A 1). Many diverse layer sets could be defined for circuit benchmarks. For example, it is possible to define layers that perform very complicated unitaries that have to be compiled into complex circuits of one- and two-qubit gates. Conversely, it is possible to define layers that can be performed in a single clock cycle (on a specified processor). The layer sets we use in this paper are composed of layers that are closer to the second example — their “physical depth” (the number of clock cycles required for implementation) is relatively small.

In the layer sets used for our benchmarks, every allowed $w$-qubit layer is constructed by combining one- and two-qubit gates, chosen from a small gate set, in parallel. Each of the $w$ qubits is acted on by at most one gate. The gate set contains an idle gate, and every qubit not targeted by a nontrivial gate is said to be acted on by that idle gate. By saying that individual gates are “combined in parallel”, we are not saying that the processor has to implement them simultaneously. Recall that a layer defines a unitary, not an implementation. We are defining layers that could in principle be implemented in parallel, within a single time step, by a processor that (1) can perform any gate in the gate set in a single time step, and (2) can perform them simultaneously. But real processors are not required to do so — the individual gates in a layer can be serialized and/or compiled into more elementary operations.

A precise description of how our layer sets are constructed from gate sets is as follows:

1. A $k$-qubit gate $G$ is an instruction to perform a specific unitary on $k$ qubits. We only consider $k = 1, 2$.
2. A gate set $\mathcal{G} = \{G_1, \ldots, G_n\}$ is a list of 1- and 2-qubit gates. Each gate could, in principle, be applied to any qubit (for 1-qubit gates) or any ordered pair of qubits (for 2-qubit gates). However, connectivity constraints (see below) can be specified, and they restrict the qubits and/or ordered pairs of qubits on which a given gate can be applied.
3. We consider only gate sets that contain (a) exactly one 2-qubit gate; (b) a 1-qubit “idle gate”; and (c) any number of additional 1-qubit gates.
4. A $w$-qubit layer is constructed by assigning gates from $\mathcal{G} = \{G\}$ to specific qubits. In each $w$-qubit layer, each of the $w$ qubits is acted on by exactly one gate, which may be the idle gate.

A $w$-qubit layer set $\mathcal{L}_w$ can be constructed, as above, by starting with a gate set and generating all possible $w$-qubit layers of this form. We define smaller layer sets by allowing all and only those layers that respect:

1. A connectivity constraint ($T_c$) that specifies which qubits, or ordered pairs of qubits, each gate can be assigned to. We call this a connectivity constraint because the most important type of assignment constraint is a limitation on which ordered pairs of qubits the two-qubit gate can be applied to. The connectivity constraint can be defined to respect a processor’s directed connectivity graph, so that a two-qubit gate only appears in layers if that processor can implement it natively. The (undirected) connectivity graphs for all twelve processors that we benchmarked are shown in Fig. 1d.
2. A parallelization constraint \((C_p)\) that specifies which assigned gates are allowed to appear together in a layer. This can be used to respect a processor’s limited ability to perform some gates in parallel, e.g., perhaps only a single two-qubit gate can be performed in a layer.

Enforcing these constraints can reduce (or eliminate) the need for additional circuit compilation at run time. This can simplify further analyses of the benchmark results, such as estimation of per-gate error rates.

B. Layer sets for benchmark circuits

The procedure given above defines a canonical layer set for each \((G, C_r, C_p)\), which contains all the layers that can be built from \(G\) and are consistent with the constraints \(C_r\) and \(C_p\). A benchmark’s layer set determines two of its properties:

- The circuits that can be constructed and included in the benchmark.
- How depth is defined and calculated for a given circuit.

The first property impacts what aspect of processor performance the benchmark measures, while the second impacts how that performance is quantified. So the choice of layer set — i.e., of \(G\), \(C_r\), and \(C_p\) — is significant.

A standardized, architecture-blind layer set can be defined by making the \(C_r\) and \(C_p\) constraints trivial — i.e., allowing all gate assignments and placing no restrictions on parallelization — and choosing a generic architecture-independent \(G\) such as CNOT plus all 24 single-qubit Clifford gates (or all single-qubit gates if non-Clifford gates are allowed.) At the other extreme, we can define an architecture-specific layer set by choosing \(G\), \(C_r\), and \(C_p\) to match the ‘native’ layer set of a specific processor that is to be benchmarked. Both are viable, useful options.

Benchmarking circuits defined over these two extreme layer sets, respectively, probe different properties of a processor. Performance on benchmarks defined over native layer sets will correlate directly with the error rate of the native gates, and will not capture how “useful” those native gates are, or how much the processor is limited by connectivity or lack of parallelism. Conversely, benchmarks defined over a standard layer set with no connectivity constraints will penalize processors with lower connectivity (relative to “native layer” benchmarks), because each two-qubit gate between qubits that are non-adjacent for a particular processor will have to be decomposed into a sequence of gates on adjacent qubits. In principle, this can be a desirable property, because it is expected to capture performance on realistic algorithm circuits. But it is also hard to calibrate. Exactly how a particular benchmark of this type penalizes lower connectivity will depend on the details of the benchmarking circuits. Different algorithmic circuits are expected to incur different amounts of overhead (penalty) when embedded into a particular connectivity [10, 42]. Capturing this behavior faithfully may require designing a different benchmark for each type of algorithm circuit.

C. The layer sets for experiments #1 and #2

In our experiments, we intentionally avoid the complexities of limited connectivity by using layer sets that respect a processor’s connectivity graph (in contrast to, e.g., Refs. [3, 10]). In particular, we choose a layer set constructed from:

1. A gate set consisting of a processor’s native two-qubit gate and a subset of the single-qubit Clifford group (see Appendix VIII A 2 and IX A 1 for details). The native two-qubit gate for IBM Q processors is CNOT [24], and for Rigetti processors it is CPHASE [25]. (Note that here “native” means the entangling gate exposed by the processor’s interface, which may or may not correspond to the “raw” two-qubit gate implemented in hardware.)

2. A connectivity constraint corresponding to the processor’s directed connectivity graph (see Fig. 1d for the undirected connectivity graphs for all twelve processors that we benchmarked.) Note that this means that specific width-\(w\) benchmarking circuits cannot be constructed until we have chosen a subset of \(w\) physical qubits on which to run them, because different subsets of qubits in a processor may have different connectivity graphs. We do not allow a disconnected subset of \(w\) qubits to be chosen.

3. No parallelization constraint. A layer can contain active (i.e., non-idle) gates on all the qubits, regardless of whether the processor actually implements all those gates at the same time. This does not mean that a processor necessarily actually runs the gates from a layer in parallel (for Rigetti’s processors, it is our understanding that only one active gate is implemented at a time, so every layer is serialized [25]). It merely means that we define circuit depth with respect to a layer set with parallel gates. On a processor that serializes every \(w\)-qubit layer, the compiled circuit’s physical depth (number of clock cycles required) may be up to a factor of \(w\) higher than the benchmark depth. (It may be less than \(w\) because some gates could take zero time when serialized, e.g., an idle gate can be skipped.)

It could be argued that our choice for the layer set of each processor does not provide a “fair” comparison between the processors. For example, a processor will typically perform better on our benchmarks if the connections in the connectivity graph corresponding to the worst performing two-qubit gates are removed. This is a direct consequence of our decision to benchmark the full set of native operations of a processor. But no single choice of layer set can provide an uniquely “fair” comparison of two processors. Processors are described by a complex set of performance characteristics, which can only be fully explored and compared by using multiple benchmarks. Some should capture the limitations stemming from restricted connectivity, while others should not. We anticipate that mirror circuit benchmarks will be easily adapted to explore aspects of performance related to device connectivity (as other benchmarks already do [3, 10]), but that is distinct and future work.
IV. CIRCUIT MIRRORING

The mirror circuit benchmarks used in the main text were constructed using a set of circuit transformation procedures that we call, collectively, mirroring. Mirroring transformations take arbitrary circuits, and create suites of benchmarking circuits that are closely related to the original circuit[s], but satisfy the benchmarking desiderata stated in Appendix 1B above. In this appendix, we introduce and motivate these transformations. First, we summarize the specific mirroring procedure used for the experiments we performed. Then, we present each of the transformations that make up mirroring separately, because their utility extends beyond the specific procedure we used in this paper.

A. Circuit mirroring as used in our experiments

We refer to the specific circuit transformation used to generate the mirror circuit benchmarks used in our experiments as subroutine Clifford circuit (SCC) mirroring. SCC mirroring is illustrated in Fig. 4. A Clifford subroutine is any QI/QO circuit composed entirely of Clifford layers. SCC mirroring maps any Clifford subroutine to an ensemble \( \mathcal{S}(C) \) of circuits that are suitable for benchmarking. SCC mirroring can be applied to FI/CO Clifford circuits, i.e., fully specified quantum programs composed of Clifford gates, by simply stripping away the program’s initialization and readout layers. But, as we discuss below, SCC mirroring is designed to probe the performance of \( C \) as a subroutine — i.e., with the expectation that it will not necessarily be applied to the \( |0\rangle_{\text{sys}} \) state, but to an arbitrary input state, generated in the context of a larger circuit that we do not know a priori. So SCC mirroring is not optimized to probe performance in the single FI/CO context, or any other specific context.

Given a Clifford QI/QO circuit \( C = L_d L_{d-1} \cdots L_2 L_1 \) defined over the layer set \( \mathbb{L}_w \), the circuits in \( \mathcal{S}(C) \) are defined as the following sequence of layers:

(a) The initialization layer \( I \) that initializes all \( w \) qubits to \( |0\rangle \).

(b) A layer \( L_0 \) drawn from from \( \mathbb{C}_1^w = \{ \text{all } 24^w \text{-fold tensor products of the } 24 \text{-qubit Clifford gates} \} \).

(c) The circuit \( C = L_d L_{d-1} \cdots L_2 L_1 \).

(d) A layer \( Q_0 \) drawn from \( \mathbb{P}_w = \{ \text{all } 4^w \text{-qubit Pauli layers} \} \).

(e) The quasi-inversion circuit

\[
\tilde{C}^{-1} = L_1^{-1} L_2^{-1} \cdots L_{d-1}^{-1} L_d^{-1},
\]

where each quasi-inversion layer \( L_i^{-1} \) is the unique circuit layer satisfying

\[
\mathcal{U}(L_i^{-1}) = \mathcal{U}(Q_i),
\]

where \( Q_i \) is a Pauli layer that is drawn from a user-specified distribution. (For example, this Pauli layer can

D. Self-inverse layer sets

A layer set \( \mathbb{L}_w \) is self-inverse if and only if \( L^{-1} \in \mathbb{L}_w \) for all \( L \in \mathbb{L}_w \). All the benchmarks and layer sets that we construct and use in this paper are self-inverse (in particular, note that CNOT and CPHASE are self-inverse gates). It is possible to construct layer sets \( \mathbb{L}_w \) that (1) are not self-inverse, and (2) include one or more layers whose inverse requires a very deep circuit (i.e., many layers in \( \mathbb{L}_w \)). But this has few or no practical consequences for applying the methods we present here — in all the commonly found native layer sets we are aware of, generating \( U^{-1} \) requires approximately (and often exactly) the same circuit depth as generating \( U \) for any unitary \( U \in SU(2^w) \). Throughout the rest of these appendices we assume a self-inverse layer set without further comment.

Figure 4. Transforming any Clifford circuit into mirror benchmarking circuits. This figure illustrates our algorithm for transforming (a) any Clifford circuit \( C \) into (b) a representative suite of benchmarking circuits \( \mathcal{S}(C) \). “Representative” means that a processor’s average performance on circuits sampled at random from \( \mathcal{S}(C) \) is representative of how well it could perform \( C \), in a randomly chosen context (see text for details). The quasi-inverse layer \( \tilde{L}^{-1} \) is the layer that inverts \( L \) up to a particular Pauli operator \( Q_i \) — i.e., \( \mathcal{U}(\tilde{L}^{-1} L) = \mathcal{U}(Q) \) — where each \( Q_i \) is drawn from a user-specified distribution (see text for details). The circuits used in our experiments were generated via this algorithm, which is a specific case of the more general circuit mirroring transformations that we discuss in Appendix IV. These more general transformations can convert any circuit (not just Clifford circuits) into a benchmarking suite.
be sampled from \( P_w \) uniformly and independently for each quasi-inversion layer. Alternatively, it can be set to the identity layer, so that each quasi-inversion layer is simply the inverse layer, i.e., \( L^{-1} = L^{-1} \). We detail the choices made in our experiments later.)

(f) The layer \( L_0^{-1} \in \mathbb{C}^{w}_1 \) that inverts the Clifford layer \( L_0 \) performed in step (b).

(g) The readout layer \( R \) that measures every qubit in the computational basis.

All circuits in \( \mathcal{S}(C) \) therefore have the form:

\[
\mathcal{S}(C) = \left\{ RL_0^{-1} \tilde{C}^{-1} Q_0 C L_0 I \right\} .
\]  

(22)

The circuits in \( \mathcal{S}(C) \) can be constructed by enumerating \( L_0 \) over the 24th Clifford layers, \( Q_0 \) over the 4th Pauli layers, and all other \( Q_i \) according to the user-specified distribution. More practically, they can be sampled by drawing \( L_0 \) and \( Q_0 \) uniformly at random from those layer sets, and drawing each \( Q_i \) from the given distribution.

Each circuit in \( \mathcal{S}(C) \) is defined over the layer set \( \mathcal{L}_w = \mathcal{L}_w \cup \mathbb{P}_w \cup \mathbb{C}^w_1 \) (where \( \mathcal{A} \cup \mathcal{B} \) denotes the union of sets \( \mathcal{A} \) and \( \mathcal{B} \)), and it has shape \( (w, 2d + 5) \). So if \( C \)'s original layer set \( \mathcal{L}_w \) does not contain \( \mathbb{P}_w \) and \( \mathbb{C}^w_1 \), then the circuits in \( \mathcal{S}(C) \) are defined over a larger layer set than \( C \). This generally has no meaningful consequences, because those single-qubit Pauli and Clifford layers can almost always be implemented with shallow circuits over native layers, with relatively low error rates (at least compared with layers containing 2-qubit gates). The generally negligible error rates of these “extra” layers motivate their exclusion from benchmark depth (see Appendix II A 3 above) — we define the benchmarking depth in SCC mirroring as \( d = d_0 - 5 \).

SCC mirroring is motivated by the benchmarking desiderata that we presented in Appendix I. So we will now demonstrate that it satisfies each of them.

The first requirement is that each circuit in \( \mathcal{S}(C) \) must have an entirely specified context — i.e., it must be a complete, runnable quantum program. SCC mirroring satisfies this by construction (because the \( I \) and \( R \) layers are explicitly included).

The second requirement is that each circuit in \( \mathcal{S}(C) \) must have a target output that is easy to compute on a conventional computer. SCC mirroring also satisfies this requirement, although the explanation is a bit longer. Any circuit \( C_{\text{scc}} \in \mathcal{S}(C) \) has the form \( C_{\text{scc}} = R C_{\text{scc}}^{(0)} I \) where

\[
C_{\text{scc}}^{(0)} = L_0^{-1} \tilde{L}_1^{-1} \tilde{L}_2^{-1} \cdots \tilde{L}_d^{-1} Q_0 L_d \cdots L_2 L_1
\]  

(23)

is the central (QI/QO) part of the circuit, which we now show implements an easily computed Pauli operation. For any \( w \)-qubit Pauli layer \( Q^{(1)} \in \mathbb{P}_w \) and any \( L_i \in \mathcal{L}_w \),

\[
U(L_i^{-1} Q^{(1)} L_i) = U(Q L_i^{-1} Q^{(1)} L_i) , \quad (24)
\]

\[
= U(Q Q^{(2)}) , \quad (25)
\]

\[
= U(Q^{(3)}), \quad (26)
\]

for some \( Q^{(2)}, Q^{(3)} \in \mathbb{P}_w \). The second equality holds because the Pauli group is closed under conjugation by Clifford operations, and the last because the Pauli group is closed under multiplication. Therefore

\[
U(C_{\text{scc}}^{(0)}) = U(Q') , \quad (27)
\]

for some Pauli layer \( Q' \in \mathbb{P}_w \). This Pauli layer can be calculated efficiently in the circuit’s size on a conventional computer using, e.g., the “CHP” code of Aaronson [39] (CHP can simulate large circuits over many thousands of qubits in less than a second on an ordinary laptop). Therefore, if performed without errors, each circuit in \( \mathcal{S}(C) \) always produces a unique and deterministic bit string specified by that circuit’s \( Q' \).

Since each circuit in \( \mathcal{S}(C) \) has a unique target output, how well a given processor ran that circuit is easily quantified by its success probability (\( S \)). \( S \) is just the probability of seeing the target bit string, and it can be estimated efficiently from data. In our data analysis we rescale \( S \) to the polarization \( P = (S - \frac{1}{2})/(1 - \frac{1}{2}) \), for the reasons discussed in the main text and in Appendix VIII B 1. But this is just a linear rescaling, which has no impact on the theory discussed here. So in the rest of this appendix we will analyze \( S \) instead of \( P \).

The third requirement (and the most subtle) is that the performance of the circuits in \( \mathcal{S}(C) \) must be representative of how \( C \) would perform in the context(s) where it might be used. This desideratum is what requires us to map \( C \) to an ensemble of circuits (rather than just a single circuit), and it therefore motivates each of the randomized elements in the procedure outlined above.

To show that SCC mirroring satisfies the third desideratum, we represent a processor’s imperfect implementation of the QI/QO circuit \( C \) by a \( w \)-qubit superoperator \( \Lambda(C) \) (see Appendix II). This superoperator can be written as

\[
\Lambda(C) = \mathcal{E}(C) \mathcal{U}(C) , \quad (28)
\]

where \( \mathcal{E}(C) \) is an error map. If the processor can run \( C \) perfectly, \( \mathcal{E}(C) \) would be the identity superoperator \( I \). As we will explain in the remainder of this appendix, SCC mirroring creates a test suite \( \mathcal{S}(C) \) with the following properties:

1. For any error superoperator \( \mathcal{E}(C) \neq I \) there is a circuit in \( \mathcal{S}(C) \) for which \( S < 1 \). That is, unless a processor can implement \( C \) perfectly in all contexts, there is at least one circuit in \( \mathcal{S}(C) \) that will bear witness to the error.

2. The expected value of \( S \) for a circuit sampled from \( \mathcal{S}(C) \) is closely related to the process fidelity of \( \mathcal{E}(C) \). Therefore, the expected value of \( S \) is approximately probing the performance of a processor on \( C \) in a uniformly random context. We make this statement more precise later in this appendix.

These two properties are a well-motivated sense in which a processor’s performance on a set of benchmarking circuits derived from \( C \) can be representative of the processor’s performance on \( C \). But it is not the only well-motivated interpretation of “representative performance”. SCC mirroring creates a benchmark whose average performance is closely related to...
the average fidelity with which the processor implements $C$. A benchmark that captured the processor’s worst-case performance on $C$ — i.e., the maximum probability, over all possible contexts, of getting the wrong output from running $C$ in that context — would arguably be even more desirable. But no benchmark can extract this information efficiently in $w$, because there are $e^{D(w)}$ possible contexts (e.g., input states). Capturing worst-case performance, without additional prior information, requires exhaustively exploring all of those contexts, which is infeasible. So the notion of “representative performance” achieved by SCC mirroring is not unique, but it is both natural and achievable.

The remainder of this appendix presents the collection of circuit transformations that, together, constitute mirroring. Combined in a specific way, they generate the SCC mirroring procedure explained above. Since all of the experiments we report in the main text use SCC mirroring exclusively, our primary aim is to prove that SCC mirroring satisfies the two properties stated above. But the mirroring transformations listed here are more powerful. They can also be used to generate (1) benchmarking circuits with different properties, and (2) benchmarks from non-Clifford circuits. So a secondary aim of this appendix is to explain the transformations independently, and illustrate this extensibility.

### B. Transformation 1: simple circuit mirroring

Many classical programs have a unique “right” answer, which makes it easy to detect (and benchmark) errors in classical computers. But interesting quantum circuits don’t generally produce definite outcomes (i.e., a unique bit string) even when run without errors. Instead, the post-measurement outcome of generic quantum programs is a high-entropy distribution over bit strings, and it can be extremely costly to verify that this distribution matches the target, i.e., that the right distribution is being produced. So to enable benchmarks derived from generic circuits, the first thing we need is a way of transforming interesting quantum circuits so that they do produce definite outcomes. The rather obvious solution is time reversal, and we call the particular transformation that we use simple circuit mirroring. This transformation turns any circuit into a definite-outcome circuit, satisfying our second requirement, at the cost of creating some new problems that we will address later.

Simple circuit mirroring is essentially a type of Loschmidt echo [22]. It maps any shape $(w, d)$ QI/QO circuit $C = L_d \cdots L_2 L_1$ over some self-inverse layer set $L_n$ into a single shape $(w, 2d + 2)$ FI/CO circuit $M(C)$ over $L_n$,

$$M(C) = R C^{-1} C I,$$  \hspace{1cm} (29)

consisting of:

(i) The initialization layer $I$ that initializes all $w$ qubits to $|0\rangle$.

(ii) The circuit $C = L_d L_{d-1} \cdots L_2 L_1$.

(iii) The inversion circuit

$$C^{-1} = L_1^{-1} L_2^{-1} \cdots L_{d-1}^{-1} L_d^{-1},$$  \hspace{1cm} (30)

consisting of the layers of $C$ in the reverse order and with each layer $L$ replaced with its inverse $L^{-1}$.

(iv) The readout layer $R$ that measures every qubit in the computational basis.

The inversion circuit $C^{-1}$ implements the inverse unitary to $C$, i.e.,

$$U(C)U(C^{-1}) = 1.$$  \hspace{1cm} (31)

Therefore, for any circuit $C$, if $M(C)$ is performed without error, it will deterministically return the all-zeros bit string. Simple circuit mirroring achieves the first two of our three desiderata for a circuit transformation (see above) for generating a benchmarking suite $\mathcal{S}(C)$ from a circuit $C$: the single-element set $\mathcal{S}_{sm}(C) = \{M(C)\}$ generated by simple circuit mirroring contains a single circuit with an entirely specified context (it is a complete program) and an efficiently simulable target output (it is the all-zeros bit string).

Simple circuit mirroring is a good starting point for satisfying the third desiderata, but, unaltered, it does not meet it. The circuit suite $\mathcal{S}_{sm}(C) = \{M(C)\}$ generated by simple circuit mirroring is not representative of $C$ in any meaningful sense. (Unless strong assumptions are made about the types of errors that a processor is subject to, $M(C)$ is only representative of $C$ in the trivial sense that a processor’s performance on $M(C)$ is representative of its performance on $C$ in the context of inserting $C$ into that simple circuit mirror circuit.) The limitations of simple circuit mirroring all stem from the fact that it involves running $C$ in a single context. Three specific effects that limit the usefulness of $\mathcal{S}_{sm}(C)$ are:

1. **Systematic error cancellation.** In simple circuit mirroring, the circuit $C$ is always followed by the circuit $C^{-1}$. This means that it is possible for systematic (coherent) errors in the implementation of $C$ to exactly cancel with systematic errors in the implementation of $C^{-1}$. For example, if $\Lambda(C) = \mathcal{V}$ and $\Lambda(C^{-1}) = \mathcal{V}^{-1}$ for some unitary superoperator $\mathcal{V}$ then $S = 1$, up to contributions from errors in qubit initialization and readout. This does not require that $\Lambda(C)$ is even close to the target evolution $\mathcal{U}(C)$. This is a well-known effect with the Loschmidt echo, which tests whether an evolution can be reversed, not whether a desired evolution can be implemented accurately.

2. A single input state. The state input into $C$ is always $|0\rangle^w$, so simple circuit mirroring is insensitive to any errors that do not impact $|0\rangle^w$.

3. A single measurement basis. The measurement is always in the computational basis, so simple circuit mirroring is insensitive to any errors that, once commuted through the circuit, manifest as errors that have no observable impact after projection onto $|0\rangle^w$ (such as dephasing or coherent $\hat{z}$-axis errors).
The three additional circuit transformations tools that we introduce below can be used to place $C$ in a wider range of contexts. They start from $\mathcal{S}_{\text{sm}}(C)$ and map it to an altered and (typically) enlarged benchmarking suite. It is convenient to think of these three tools as a set of three configurable circuit transformations that are applied in order.

C. Transformation 2: inserting a central subroutine

The first weakness of simple circuit mirroring, highlighted above, is that it can hide errors in $C$, because errors in $C^{-1}$ might systematically cancel out errors in $C$. To solve this problem, we introduce another transformation called central subroutine insertion, which we apply to the test suite $\mathcal{S}_{\text{sm}}(C) = \{M(C)\}$ obtained from simple circuit mirroring. It constitutes inserting each of a set $A$ of subroutines — i.e., QI/QO circuits — between $C$ and $C^{-1}$. This transformation acts on $\mathcal{S}_{\text{sm}}(C)$ as:

$$\{M(C) = RC^{-1}CI\} \rightarrow \{M_A(C) = RC^{-1}ACI\}_{A \in A}. \quad (32)$$

Central subroutine insertion generates a larger circuit suite,

$$\mathcal{S}_A(C) = \{M_A(C)\}_{A \in A}, \quad (33)$$

that can be run exhaustively or sampled from. The point of the central subroutine is to prevent systematic errors in $C$ and $C^{-1}$ from canceling each other. It only works if $A$ is chosen carefully, to satisfy three competing criteria:

1. The subroutines in $A$ should be sufficiently diverse that no possible error mode on $C^{-1}$ can systematically cancel out errors on $C$ in every circuit in $\mathcal{S}_A(C)$. As an obvious example, an $A$ containing only the trivial, depth-0 circuit would not be sufficiently diverse.

2. Each circuit in $\mathcal{S}_A(C)$, when run without error, should output a single, efficiently calculable bit string. In some scenarios, achieving this requirement will require an additional transformation, as explained in Transformation 3 below.

3. The subroutines in $A$ should be implementable with shallow circuits, so that running the circuits in $\mathcal{S}_A(C)$ is not much harder than running simple mirror circuits.

To make the “sufficiently diverse” condition above precise, we consider the linear map $\mathcal{L}_{CA}$ on $w$-qubit superoperators (a so-called super-duper-operator [43]) defined by:

$$\mathcal{L}_{CA}(S) = \Lambda(C^{-1})SA\Lambda(C). \quad (34)$$

This map is parameterized by (1) a circuit $C$, and (2) a processor’s $\Lambda(\cdot)$ map. We say that a processor implements a circuit $C$ perfectly if and only if $\Lambda(C) = \mathcal{U}(C)$. Therefore, a processor perfectly implements both $C$ and $C^{-1}$ if and only if, for every superoperator $S$,

$$\mathcal{L}_{CA}(S) = \mathcal{L}_{CA}(S). \quad (35)$$

Simple circuit mirroring cannot tell us whether this is the case. It only tells us about $\mathcal{L}_{CA}(I)$, where $I$ is the identity superoperator, because the processor’s implementation of the QI/QO component of the simple mirror circuit $M(C)$ is

$$\Lambda(C^{-1}C) = \mathcal{L}_{CA}(I). \quad (36)$$

So simple circuit mirroring cannot be sensitive to all possible errors in $\Lambda(C)$ and $\Lambda(C^{-1})$, because Eq. (35) might hold for $S = I$, but not for all $S$.

We can use $\mathcal{L}_{CA}$ to more precisely state the first of our criteria for $A$, introduced above. For any $\Lambda(C)$ and $\Lambda(C^{-1})$ superoperators for which $\Lambda(C) \neq \mathcal{U}(C)$ and/or $\Lambda(C^{-1}) \neq \mathcal{U}(C^{-1})$, there must exist an $A \in A$ such that

$$\mathcal{L}_{CA}(\mathcal{U}(A)) \neq \mathcal{L}_{CA}(\mathcal{U}(A)). \quad (37)$$

Without assumptions about the constituent superoperators, this holds if and only if $\mathcal{U}(A) = \{\mathcal{U}(A)\}_{A \in A}$ spans the vector space of $w$-qubit superoperators. (Because $\Lambda(C)$ and $\Lambda(C^{-1})$ must be completely positive and trace preserving maps there are interesting edge cases where we can learn everything about $\Lambda(C)$ and $\Lambda(C^{-1})$ with a smaller set $A$. Indeed, $\mathcal{U}(A)$ should span that space uniformly (as does, e.g., an orthonormal basis) to maximize sensitivity to all possible errors. However, constructing a set of circuits that span the superoperator space requires nontrivial circuits. So in SCC mirroring, we settle for a slightly weaker (but much simpler) construction that detects almost all errors.

We choose an $A$ containing all the $w$-qubit Pauli layers $\mathcal{P}_w$ (see Fig. 4). When $C$ is a Clifford circuit as in the main text (we address non-Clifford circuits briefly in the next subsection of this appendix), the Pauli layers are a particularly powerful choice for the following reasons.

1. Sensitivity to all small errors. The Pauli group $\mathcal{U}(\mathcal{P}_w)$ does not span superoperator space (there are only $4^w$ elements in $\mathcal{U}(\mathcal{P}_w)$, but superoperator space has dimension $4^w \times 4^w = 16^w$), but it has a property that is almost as good in this context. If $\mathcal{L}_{CA}(Q) = \mathcal{L}_{CA}(Q)$ for all $Q \in \mathcal{P}_w$ then this implies that $\Lambda(C) = \mathcal{U}(Q)$ and $\Lambda(C^{-1}) = \mathcal{U}(C^{-1}Q)$ for some Pauli layer $Q$ that is the same in both equations, i.e., the correct unitaries are implemented up to multiplication by some Pauli operator. So the only errors that go undetected by $A = \mathcal{P}_w$ are large, discrete, and unlikely except in an adversarial context.

2. Faithfulness in infidelity. More than merely making all small errors detectable, the Pauli group construction ensures that their average impact on the benchmark circuits faithfully reflects their impact in $C$ and $C^{-1}$. If we average uniformly over $A$, the effect of inserting a random Pauli layer between $C$ and $C^{-1}$ is to perform a Pauli twirl on the error maps for $C$ and $C^{-1}$, reducing them to stochastic Pauli channels [35, 44, 45]. For small errors, this ensures that the fidelity of the full benchmark circuit is very close to the product of the fidelities of $C$ and $C^{-1}$.
3. Efficiently calculable target outputs. For any Pauli layer \( Q, \mathcal{U}(C^{-1}QC) = \mathcal{U}(Q') \), for some Pauli layer \( Q' \). So \( M_Q(C) \) will always output a single, efficiently calculable bit string determined by \( Q' \), if implemented perfectly.

4. Unbiased target outputs. Uniform sampling from \( \mathbb{S}_P(C) \) ensures that the target bit string is uniformly random, so biased readout errors cannot artificially boost or suppress the success probabilities \( S \) of the circuits in \( \mathbb{S}_P(C) \) (again, on average).

5. Low-depth circuits. Any Pauli layer can be implemented with a low-depth circuit over the native layer-set of a typical processor.

In the remainder of this appendix we will consider only the case of \( \Lambda = \mathbb{P}_w \).

D. Transformation 3: replacing the inversion circuit with a suite of quasi-inversion circuits

The reason that errors can systematically cancel in simple circuit mirroring is that \( C \) is always followed by the same circuit, \( C^{-1} \). Inserting a central subroutine prevents this error cancellation, but we can also reduce the correlation between layers in a mirror circuit by replacing \( C^{-1} \) with a quasi-inversion circuit \( \tilde{C}^{-1} \). For a Clifford circuit \( C \), this transformation maps each \( M_Q(C) \) circuit to a set of circuits where the inverse circuit \( C^{-1} \) has been replaced by each of a set of quasi-inversion subroutines \( Q \). It is the map:

\[
M_Q(C) = R_C^{-1}QCI \to \{M_Q,\tilde{C}(C) = R_C^{-1}QCI\}_{\tilde{C} \in \mathbb{Q}}.
\] (38)

where \( \mathbb{Q}(C) \) consists of all circuits of the form

\[
\tilde{C}^{-1} = \tilde{L}_1^{-1}\tilde{L}_2^{-1}\cdots\tilde{L}_{d-1}^{-1}\tilde{L}_d^{-1}.
\] (39)

Here each \( \tilde{L}_i^{-1} \) runs over some set of \( L \)-dependent layers \( Q_1(L) \) that all implement unitaries that are equivalent to \( \mathcal{U}(L^{-1}) \) up to multiplication by a Pauli operator.

Different choices for \( Q_1 \) result in different transformations. In our benchmarking experiments we use two transformations: the trivial transformation given by \( Q_1(L) = \{L^{-1}\} \), and the transformation in which \( Q_1(L) \) consists of all \( 4^n \) layers \( L^{-1} \) that satisfy \( \mathcal{U}(L^{-1}) = \mathcal{U}(Q'L^{-1}) \) for some \( Q' \in \mathbb{P}_w \) (which is similar to Pauli frame randomization [35, 44, 45]).

A similar transformation can be used to create mirror circuits with a central Pauli subroutine from non-Clifford circuits: in that case we choose the quasi-inverse layers as a function of the central Pauli layer \( Q \), which allows us to construct quasi-inverse circuits for which the entire circuit implements a Pauli operator. As we do not use non-Clifford circuits in our experiments, we leave further details of this technique to future work.

E. Transformation 4: inserting preparation and measurement subroutines

The last of our circuit transformations is intended to address the last two limitations of simple circuit mirroring listed at the end of Appendix IV B: that only the \( |0\>^n \) state is input into \( C \), and that readout is always in the computational basis. These limitations mean that any errors in the implementation of \( C \) that do not affect the \( |0\>^n \) state do not contribute to the failure rate of a simple mirror circuit, nor to the failure rates of the circuits in the expanded suites obtained from Transformations 2 and 3. If the circuit \( C \) will only ever be applied to \( |0\>^n \), then this is not a flaw as it represents the desired context. But to capture any other contexts, we need to implement additional input states and measurement bases so that performance on the benchmarking suite is representative of ability to perform \( C \) in generic contexts. We do this by inserting “fiducial” [29] subroutines just after initialization and before readout, respectively.

This procedure is parameterized by a set of QI/QO circuits \( \mathbb{F} \) and it maps each circuit \( M_{Q,\tilde{C}}(C) = R_C^{-1}QCI \) to a test suite

\[
M_{Q,\tilde{C}}(C) \to \{M_{Q,\tilde{C},F}(C) = RF^{-1}\tilde{C}^{-1}QCFI\}_{F \in \mathbb{F}}.
\] (40)

Together, the four transformations generate the circuit suite

\[
\mathbb{S}_{P,F}(C) = \{M_{Q,\tilde{C},F}(C)\}_{Q \in \mathbb{P}_w, \tilde{C} \in \mathbb{Q}(C), F \in \mathbb{F}}.
\] (41)

which can be run exhaustively or sampled from. We need to choose \( \mathbb{F} \) to satisfy the four competing criteria:

1. Each circuit in \( \mathbb{S}_{P,F}(C) \) should still have an efficiently calculable target bit-string.

2. The fiducial subroutines should be implementable with shallow circuits over a typical processor’s native gate, so that errors in these subroutines do not dominate the failure rate of the circuits in \( \mathbb{S}_{P,F}(C) \), except perhaps for very shallow \( C \).

3. The fiducials should be sufficiently diverse that they reveal all errors that are visible in any of the contexts in which \( C \) will be used. In the case of a subroutine \( C \) that is to be used in an \textit{a priori} entirely unknown context, this means that if \( \Lambda(C^{-1}QC) \neq \mathcal{U}(C^{-1}QC) \) then there should be at least one \( F \in \mathbb{F} \) for which \( S < 1 \) for the corresponding circuit.

4. (Stretch goal) The fiducials should generate circuits that are \textit{uniformly sensitive} to all possible errors in \( \Lambda(C^{-1}QC) \), ensuring that the average performance over randomly sampled fiducials is closely related to the process fidelity of \( \Lambda(C^{-1}QC) \).

The first criterion is achieved by setting \( \mathbb{F} \) to any subset of the \( w \)-qubit Clifford layers \( \mathbb{C}_w \). The third criterion is satisfied if and only if \( \mathbb{F} \) is informationally complete (i.e., it’s element are sufficient for process tomography). The fourth criterion is achieved by a set \( \mathbb{F} \) that generates a 2-design, such as the \( w \)-qubit stabilizer states, which is achieved by the full \( w \)-qubit
Clifford layer set $C_w$ [46, 47]. But the elements of $C_w$ cannot be implemented with $O(1)$ depth circuits, so the full $w$-qubit Clifford group cannot satisfy our second criterion. In fact, no 2-design can be generated with $O(1)$ depth circuits over one- and two-qubit gates. We therefore choose to set $\mathbb{F} = C_1^w$, where $C_1^w$ denotes the $w$-fold tensor product of the single-qubit Clifford group.

Setting $\mathbb{F} = C_1^w$ satisfies criteria (1), (2), and (3). It does not directly satisfy criterion (4), as $C_1^w$ does not generate a 2-design. However, when combined with some simple and efficient data processing, $\mathbb{F} = C_1^w$ does satisfy the fourth criterion. To understand why, observe that averaging over these fiducials performs a type of group-twirl [15]. Fiducials from $C_1^w$ implement the twirling map $\mathcal{T}$ that acts on $w$-qubit super-operators as

$$\mathcal{T}(\mathcal{E}) = \frac{1}{24^w} \sum_{L \in C_1^w} \mathcal{U}(L) \mathcal{E} \mathcal{U}(L^{-1}).$$

This twirl projects any superoperator onto the space spanned by $w$-fold tensor products of one-qubit depolarizing channels [15] (in practice there will be errors in the fiducial subroutines, so they do not implement a perfect twirl. However, it is known that the effect of twirling is robust under weak error [48–50]). So averaging over the fiducials converts $\Lambda(\hat{C}^{-1} QC)$ into a stochastic Pauli channel with a distribution over Pauli errors that, for each of the $w$ qubits, has a uniform marginal distribution over the three Pauli errors, $X, Y$ and $Z$. This guarantees good (but not uniform) sensitivity to all errors, because, although the $Z$ errors cause no observable failure — i.e., the correct bit is output by the qubit on which the error occurs — both $X$ and $Y$ errors flip the output bit of that qubit. So the rate of unobserved $Z$ errors can be inferred from the observed rate of bit flips.

This implies that there is a simple function of data that is equal to $F_w(\Lambda(\hat{C}^{-1} QC))$, up to contributions from errors in the initialization, readout and fiducial subroutines. For $k = 0, 1, \ldots, w$, let $h_k$ denote the probability of the circuit producing a bit string whose Hamming distance from the target bit string is $k$ — so $h_0 = S$ and $\sum_{k=0}^w h_k = 1$. For $k = 0, 1, \ldots, w$, let $p_k$ denote the probability that $\mathcal{T}(\Lambda(\hat{C}^{-1} QC))$ induces any weight $k$ error — so $p_0$ is the probability of no error, meaning that

$$p_0 = F_w(\Lambda(\hat{C}^{-1} QC)), \quad (43)$$

and $\sum_{k=0}^w p_k = 1$. These distributions are related by

$$h = Mp,$$

where $M_{jk}$ is the probability that a weight-$k$ error causes $j$ bit flips on the target bit string. Now a weight-$k$ error causes $j$ bit flips if $j$ of the $k$ Pauli errors are not $Z$. Because the probability of all three Pauli errors is equal, this is simply given by

$$M_{jk} = \binom{k}{j} \frac{2^j}{3^k}.$$

for $j \leq k$, with $M_{jk} = 0$ for $j > k$. By inverting this equation we obtain:

$$p_0 = \sum_{k=0}^w \left(\frac{1}{3}\right)^k h_k. \quad (46)$$

The Hamming distance distribution can be efficiently estimated from data (it is a distribution over $w + 1$ elements). So we can use this relationship to efficiently estimate the process fidelity of $\Lambda(\hat{C}^{-1} QC)$ — up to contributions from errors in the initialization, readout and fiducial subroutines, which, if desired, could be estimated and removed using standard techniques [6]. It would therefore be well-motivated to use the right-hand-side of Eq. (46), in place of $S$ or $P$ (the polarization), as a quantifier of how successfully a mirror circuit with randomized single-qubit Clifford fiducials has run. We do not do so in this work, however, for two reasons. First, $S$ and $P$ are arguably more intuitive. Second, using $p_0$ instead of $S$ or $P$ makes little difference to our results, and no difference to our scientific conclusions. One of the reasons for this is that $p_0 \approx S$ when most of the observed incorrect bit strings are a large Hamming distance from the target bit string. This will typically occur when $C$ is a wide and deep circuit containing many two-qubit gates (which will spread errors).

V. RANDOMIZED MIRROR CIRCUITS

Our experiments used two kinds of mirror circuits: randomized mirror circuits and periodic mirror circuits. In this appendix we define randomized mirror circuits. Although the definitions in this appendix are self-contained, the mirroring transformations used to construct them were introduced and motivated in Appendix IV.

A. Definition

Our experiments used randomized mirror circuits built from alternating layers of randomized Pauli gates and Clifford gates chosen from a sampling distribution $\Omega$ over a Clifford layer set $\mathbb{C}_w$. In the second half of the circuit, each of the $\Omega$-random layers is inverted, but the Pauli layers are independently resampled randomly. The sampling distribution $\Omega$ is configurable, and is used to vary and fine-tune the properties of the benchmark. (A related construction plays a role in direct randomized benchmarking [9]).

A width-$w$ randomized mirror circuit with a benchmark depth of $d$ (see schematic in Fig. 5) consists of:

(a) An initialization layer that prepares all $w$ qubits in $|0\rangle$.

(b) A layer of uniformly random single-qubit Clifford gates on each qubit.

(c) A sequence of $d/4$ independently sampled pairs of layers, where each pair consists of

1. A layer of uniformly random Pauli gates on each qubit.
Figure 5. **Randomized mirror circuits.** This figure shows a schematic of the randomized mirror circuits used in our experiments. These circuits are sequences of \( w \)-qubit layers, of 5 distinct types: initialization, random Pauli, random local Clifford, general Clifford, and readout. Four of these layer types are completely standardized, but the set \( \Omega \) of general Clifford layers can be configured to generate different benchmark ensembles, by specifying a distribution \( \Omega \) over Clifford layers. A similar approach was used in direct randomized benchmarking [9], and this construction can be generalized to non-Clifford circuits (see text). A width \( w \) randomized mirror circuit with a *benchmark depth* of \( d \) consists of the following layers: (a) an initialization layer that prepares all \( w \) qubits in \(|0\rangle\); (b) a layer of uniformly random single-qubit Clifford gates on each qubit; (c) \( \frac{\pi}{4} \) independently sampled pairs of layers, each comprising a layer of uniformly random Pauli gates followed by a layer sampled from \( \Omega \); (d) a layer of uniformly random Pauli gates on each qubit; (e) the layers from step (c), but with their order reversed, each Pauli layer independently resampled, and each \( \Omega \)-random layer replaced with its inverse; (f) the inverse of the first layer of Clifford gates; and (g) a readout layer that measures each qubit in its computational basis. Randomized mirror circuits can have any width \( w \) (here \( w = 6 \)) and any benchmark depth \( d \) \(\geq 0\) that is an integer multiple of 4. Note that the full depth \( d_\text{f} \) of the circuit is \( d_\text{f} = d + 5 \) — the benchmark depth ignores the five constant layers from steps (a, b, d, f, g). Benchmark depth is reported in the main text.

2. A layer sampled from \( \Omega \).

   (d) A layer of uniformly random Pauli gates on each qubit.

   (e) The layers from step (c) in the reverse order with:

   1. Each \( \Omega \)-random layer replaced with its inverse.

   2. Each Pauli layer independently resampled.

   (f) The inverse of the Clifford layer from step (b).

   (g) A readout layer that measures each qubit in the computational basis.

Randomized mirror circuits can have any width \( w \), and any benchmark depth that is a multiple of four (i.e., \( d = 4k \) for some integer \( k \geq 0 \)). As with all our benchmark circuits, note that the full depth \( d_\text{f} \) of the circuit is \( d_\text{f} = d + 5 \) — the benchmark depth ignores the constant contribution of the five layers in steps (a), (b), (d), (f) and (g).

The bulk of a randomized mirror circuit is occupied by \( \Omega \)-random layers (which are the heart of the construction) and random Pauli layers. The random Pauli layers play a simple role: they maximize the disorder of each circuit (no matter what \( \Omega \) is used) and locally scramble errors. They impose local basis randomization, which ensures that systematic, coherent errors on the layers almost surely do not not align or anti-align, and therefore do not interfere constructively or destructively over many circuit layers. This has an effect somewhat similar to Pauli frame randomization [35, 44, 45]. However, in contrast to Pauli frame randomization, the Pauli layers in our circuits are not resampled each time the circuit is run. This is because our aim is not to convert all types of error into stochastic Pauli errors — instead we are aiming to benchmark a processor’s performance on disordered circuits. (Note, however, that a processor is free to implement our benchmarking circuits using randomized gate implementations. As discussed above, our construction is agnostic as to how the layers are implemented.)

The central random Pauli layer, which appears in *all* our mirror circuits (including the periodic ones shown in Fig. 6), plays a special role. It prevents cancellation of errors between a circuit \( C \) and the “quasi-inverse” circuit \( C^{-1} \) used to mirror \( C \). The alternating layers of randomized Pauli gates — which only appear in randomized mirror circuits — play a similar role for each layer. They limit the degree to which coherent errors can systematically add or cancel between layers, on average. The \( \Omega \)-random layers also prevent systematic addition and cancelation, but the addition of the uniformly random Pauli layers causes the rate that coherent errors systematically add or cancel to only weakly depend on \( \Omega \). This is convenient, because varying \( \Omega \) is useful for generating varied and interesting benchmarking circuit ensembles.

The theory of direct randomized benchmarking [9] can be used to show that the mean success probability of a randomized mirror circuit sampled according to \( \Omega \) is closely related to the process fidelity of a \( \Omega \)-random circuit layer. Similar relationships hold for other kinds of randomized circuit [4–6]. However, we do not use this relationship in this paper, so we do not pursue it further here.
B. Circuit samplers

Varying the distribution $\Omega$ over Clifford layers provides a way to tune and control important properties of the random mirror circuit benchmark. One of the most important properties is the density of two-qubit gates within the circuits, which we denote $\xi$. Each of our experiments used a distribution $\Omega$ over layers constructed from the following native gate set:

- a set of single-qubit Clifford gates, $\mathcal{G}_1$, each of which may be applied to any qubit, and
- a single two-qubit Clifford gate that may be applied to any pair of connected qubits.

We define $\Omega$ distributions constructively, by defining samplers that generate layers. Assigning two-qubit gates is the trickiest part of this sampling, and to do so we make use of an edge sampler that we denote $\chi$. An edge sampler $\chi$ takes as input the connectivity graph of the $w$ qubits being benchmarked, and (usually) a parameter to control the number of edges that will be sampled. It outputs a subset of edges that have no qubits (nodes) in common. This can be done in several ways, and we discuss the particular edge samplers we used in a moment. We can use this any such edge sampler $\chi$ to sample a $w$-qubit layer (which defines an $\Omega$) as follows:

1. Use $\chi$ to select a set of disjoint connected pairs of qubits from the $w$ available qubits.
2. Add a two-qubit gate on each edge selected in Step 1.
3. Assign a uniformly random single-qubit gate from $\mathcal{G}_1$ to each remaining qubit.

This sampling allows us to control the two-qubit gate density in the circuits, while guaranteeing that a typical circuit is always highly disordered. To specify a particular distribution $\Omega$, we only need to specify the edge sampler $\chi$. Below are the $\chi$ samplers used in our two experiments.

1. The circuit sampling of experiment #1

The randomized mirror circuits of experiment #1 were sampled using a particularly simple edge sampler ($\chi_1$). It returns either zero edges (with probability 1/2), or a single edge selected uniformly at random from the $w$-qubit connectivity subgraph (with probability 1/2). This sampling algorithm is not appropriate for arbitrarily large processors, because the expected two-qubit gate density of the circuits it generates $\bar{\xi}$ goes to zero as $w \to \infty$. However, it is simple and transparent, and in the 1-16 qubit regime of our experiments it generates a useful array of circuits. The low density of two-qubit gates ensures low enough error rates that we can actually probe how device performance varies with $d$ and $w$ (rather than seeing the success probability drop below measurable levels even for very small circuits).

2. The circuit sampling of experiment #2

The randomized mirror circuits of experiment #2 are sampled using an edge sampler ($\chi_2$) that we call the edge grab. It is parameterized by the expected two-qubit gate density of the sampled circuits, $\bar{\xi}$. This sampler is designed for generating randomized mirror circuit benchmarks on arbitrarily large processors.

Before we introduce the edge grab, we need to clarify our definition of two-qubit gate density ($\bar{\xi}$). The two-qubit gate density of a circuit $C$ with shape $(w, d)$ that contains $\alpha$ two-qubit gates is defined as $\xi = \frac{\alpha}{2w^d}$. If the circuit is thought of as a $w \times d$ lattice, this is the proportion of the lattice sites that are occupied by a two-qubit gate. In this work we use the benchmark depth to define $\bar{\xi}$.

The edge grab procedure $\chi_2$ is defined as follows:

1. Select a candidate set of edges $E$. Initialize $E$ to the empty set, and initialize $E_i$ to the set of all edges in the connected sub-graph of the $w$ qubits. Then, until $E_i$ is the empty set:
   1.1 Select an edge $v$ uniformly at random from $E_r$.
   1.2 Add $v$ to $E$ and remove all edges that have a qubit in common with $v$ from $E_r$.
2. Select a subset of the candidate edges. For each edge in $E$, include it in the final edge set with a probability of $\frac{wE}{|E|}$ where $|E|$ is the total number of edges in $E$.

The expected number of selected edges is $w\bar{\xi}$, so this sampler generates a $w$-qubit layer with an expected two-qubit gate density of $2\bar{\xi}$. Because only half of the layers in a randomized mirror circuit are sampled using $\chi$, randomized mirror circuits sampled according to the edge grab sampler have an expected two-qubit gate density of $\bar{\xi}$. Individual circuits’ two-qubit gate density will fluctuate around this value, but the ensemble variance of $\xi$ converges to zero as the circuit size increases. This sampling algorithm has another nice property: the probability of sampling a particular $w$-qubit layer $L$ is non-zero for every $L \in \Omega_w$ (except if $\bar{\xi} = 0$ or $\bar{\xi} = \frac{1}{2}$). The edge grab algorithm is invalid if $\frac{wE}{|E|} > 1$ for any possible candidate edge set $E$. For an even number of fully-connected qubits, $\xi$ can take any value between 0 and $\frac{1}{2}$ (note that $\frac{1}{2}$ is the maximum possible $\xi$ in a randomized mirror circuit, as half the layers in these circuits contain only single-qubit gates). But for any other connectivity the maximum achievable value of $\bar{\xi}$ is smaller. In our experiments, we set $\bar{\xi} = \frac{1}{8}$. This is an achievable value of $\bar{\xi}$ in the edge grab algorithm for all the processors that we benchmarked.

VI. PERIODIC MIRROR CIRCUITS

Our experiments consisted of running two types of mirror circuit benchmark: randomized mirror circuits and periodic mirror circuits. In this appendix we define the class of periodic mirror circuits, and the specific periodic mirror circuits that we ran in our experiments. These circuits are constructed
Figure 6. Periodic mirror circuits. A schematic of the periodic mirror circuits that we use in our experiments. A width \( w \) periodic mirror circuit with a benchmark depth of \( d \) consists of the following layers: (a) initialization of all \( w \) qubits in \( |0\rangle \); (b) a layer of uniformly random single-qubit Clifford gates on each qubit; (c) \( \lfloor w / d \rfloor \) repetitions of a "germ" circuit of depth \( d_c \); (d) a layer of uniformly random Pauli operators on each qubit; (e) the layers from step (c) in the reverse order and with each layer replaced with its inverse; (f) the inverse of the first layer of Clifford gates; (g) readout of each qubit in the computational basis. If \( \lfloor w / d \rfloor \) is not an integer then only some of the layers of the germ circuit are run in the last repetition of the germ in (c). In our experiments, the germ circuit is sampled at random, using an algorithm (detailed in the text) that generates a germ circuit with a two-qubit gate density \( \xi \leq 1/8 \). In the example shown here, the two-qubit density is exactly \( \xi = 1/8 \).

Periodic mirror circuits can have any width \( w \), any benchmark depth \( d \) that is an integer multiple of two. As with all our benchmark circuits, note that the full depth \( d_0 \) of the circuit is \( d_0 = d + 5 \), so we have removed the constant contribution of the five layers in (a), (b), (d), (f) and (g) from our definition of the benchmark depth. It is the benchmark depth that is reported in the main text.

A. Definition

Fig. 6 illustrates the form of our periodic mirror circuits. They are based on repetitions of a low-depth germ circuit \( C_g \), named following the terminology of gate set tomography [29]. For a given germ circuit \( C_g \) of shape \((w, d_c)\), a width-\( w \) periodic mirror circuit with a benchmark depth of \( d \) consists of:

(a) An initialization layer placing all \( w \) qubits in the \( |0\rangle \) state.

(b) A layer of uniformly random single-qubit Clifford gates on each qubit.

(c) A depth \( \lfloor w / d \rfloor \) circuit constructed by repeating \( C_g \) \( \lfloor w / d \rfloor \) times, and removing the final \( (\lfloor w / d \rfloor \mod d_c) \) layers.

(d) A layer of uniformly random Pauli operators on each qubit.

(e) The layers from step (c) in the reverse order and with each layer replaced with its inverse.

(f) The inverse of the first layer of Clifford gates in step (b).

(g) A layer reading out each qubit in the computational basis.

Using the mirroring circuit transformations introduced in Appendix IV, but note that the definitions in this appendix are self-contained.

B. Selecting the germ circuit

Defining a specific set of periodic mirror circuits — or a specific distribution over periodic mirror circuits — requires choosing a method for selecting germ circuits \( C_g \). Repeating a specific germ amplifies the effect of some errors, while suppressing others [29]. For example, a single-qubit germ circuit consisting of a single \( X \) gate amplifies coherent over/under-rotation errors in the \( X \) gate, but it suppresses the effect of "tilt" errors — i.e., \( Y \) or \( Z \) Hamiltonians that change the rotation axis of the \( X \) gate. (For example, if \( X \) is implemented perfectly except that it is followed by an erogenous small \( Z \)-axis coherent error, then a circuit consisting of an even number of \( X \) gates composes to an exact identity.) It is possible, in principle, to construct germ that, collectively, amplify all the parameters in a specific error model [29]. But a general model of Markovian errors on \( w \) qubits contains \( 16^w - 4^w \) parameters per layer, and amplifying all those parameters is infeasible. We could define a much smaller error model and construct germs that amplify all its parameters, but this is only well-motivated if that smaller model accurately describes the tested processors. We therefore take a different approach: we sample germs at random, using an algorithm that is biased towards amplifying parameters that are likely to be physically important.
1. The germ selection of experiment #2

We ran periodic mirror circuits in experiment #2. Here we describe the germ sampling algorithm that we used. It is composed of two steps. The first step constructs a germ circuit composed of only single-qubit gates, and the second step replaces some of these gates with two-qubit gates. This protocol is somewhat complicated, but was designed for investigating our specific scientific question — the effect of circuit order on circuit failure rates — and it is not intended as a general-purpose germ selection routine. We expect that different algorithms for generating periodic mirror circuits will be useful for, e.g., creating standardized benchmarks.

Step 1: The first step in our algorithm is to create a width-\( w \) germ circuit \( C_\xi \) that contains only single-qubit gates from some set \( G_1 \) (in our experiments, \( G_1 \) was the 24-element group of single-qubit Clifford gates). Our specific sampling algorithm was:

1. Select a germ depth \( d_\xi \). We do this by setting \( d_\xi = 2^x \) with probability \( 1/2^{x+1} \) for \( x = 0, 1, 2, \ldots \), and then truncating the depth to 8. That is, if \( d_\xi > 8 \) set \( d_\xi = 8 \). An exponentially decaying probability truncated at depth 8 is useful because a depth-\( d \) circuit constructed by repeating a germ of length \( d_\xi \) is only periodic if \( d > d_\xi \). Current processors cannot run very deep circuits without an error almost certainly occurring, so we can only study periodicity by repeating relatively shallow germ circuits.

2. Select a local germ for each qubit. For each of the \( w \) qubits, indexed by \( i \), we independently select a local germ \( C_{l,i} \) by:
   
   2.1 Setting \( d_{l,i} = 2^x \) with probability \( 1/2^{x+1} \) for \( x = 0, 1, 2, \ldots \), and, if the selected \( d_{l,i} \) is greater than \( d_\xi \), then setting \( d_{l,i} = d_\xi \).
   
   2.2 Setting \( C_{l,i} \) to a uniformly random depth-\( d_{l,i} \) sequence of single-qubit gates from \( G_1 \).

3. Combine the local germs. Construct a germ circuit \( C_\xi \) of depth \( d_\xi \) by combining the \( w \) independently selected local germs in parallel. To create a depth \( d_\xi \) circuit, the local germ for qubit \( q \) is repeated \( d_{l,q}/d_q \) times, where \( d_{l,q} \) is the depth of that local germ. By construction, this consists of an integer number of repetitions of each local germ.

We designed a sampling algorithm that has a strong bias towards shallow local germs — e.g., the marginal probability of a depth 1 local germ is \( \frac{1}{8} \) — because depth 1 germs amplify a particularly important class of errors that includes coherent over/under-rotations.

Step 2: The second step in our randomized germ selection algorithm is to replace some of the gates in \( C_\xi \) with two-qubit gates (unless \( w = 1 \), in which case this step is skipped). In order to test the hypothesis that periodic circuits perform worse than disordered circuits, we chose an algorithm that generates germs with a two-qubit density of \( \xi \leq \frac{1}{8} \), because \( \frac{1}{8} \) is the expected two-qubit gate density in the randomized mirror circuits that we ran alongside these periodic mirror circuits (see above, and note that these experiments are detailed further in Appendix IX). This then means that, if we observe worse performance on periodic mirror circuits, this cannot be explained by higher \( \xi \). The algorithm that we used, defined for \( w > 1 \), is as follows:

1. Set \( r \) to the minimum positive integer that satisfies \( 2/rd_\xi < 1/8 \), where \( d_\xi \) is the current germ’s depth, and then replace the germ circuit \( C_\xi \) with \( r \) repetitions of \( C_\xi \). This means that we can place at least one two-qubit gate within the germ and still obtain \( \xi \leq 1/8 \).

2. For each layer in the updated germ select a set of edges \( E_l \), with \( l = 1, 2, \ldots, rd_\xi \), using the first step of the “edge grab” sampling algorithm (see Appendix V). Then combine them into a single set \( E_\xi \) consisting of layer-index and edge pairs.

3. Place \( n = rd_\xi w/16 \) two-qubit gates into the germ, by

   (a) selecting \( n \) layer-index and edge pairs from \( E_\xi \), uniformly at random, and
   (b) replacing the one-qubit gates at each of these positions in the germ with a two-qubit gate.

Note that germs generated via this algorithm have a two-qubit gate density of \( \xi \leq \frac{1}{8} \). However, periodic mirror circuits generated from these germs can have a two-qubit gate slightly density above \( \xi \), because a germ is only partially repeated in a depth \( d \) periodic mirror circuit if the germ circuit’s depth is not a factor of \( d/2 \).

VII. PREDICTING MIRROR BENCHMARKS FROM A PROCESSOR’S ERROR RATES

Figure 2c of the main text compares the measured results of our benchmarks with the predicted performance based on the published error rates provided for each of the quantum processors. In this appendix we explain how we obtain these predictions.

The set of “error rates” \( \{ \epsilon \} \) provided for a given processor can consist of many different performance metrics estimated in many different ways. For example, the entire error rate set \( \{ \epsilon \} \) could consist of a single heuristic error rate for the entire processor. At the opposite extreme, \( \{ \epsilon \} \) could consist of all the parameters of a detailed process matrix error model fit using, e.g., gate set tomography [29]. For the processors in our experiments, the contents of the error rate sets lie between these two extremes. They include summary error rates for the native logic operations, with the gate error rates measured by randomized benchmarking. The error rate set represents a valuable description of a processor’s performance, but it does not immediately imply a detailed predictive model for the processor. In order to predict a circuit’s success probability from the provided error rates \( \{ \epsilon \} \), we need to construct a predictive
formula or model in which the only parameters are (1) these error rates, and (2) the circuit.

A. Standard error rates

The exact metrics that constitute the reported error rates, \( \epsilon \), display some minor variation across processors. But all of these can be straightforwardly transformed into a “standard form” capable of describing each of the processors we benchmarked. This standard form consists of:

- The estimated entanglement infidelity for each available single-qubit gate \( G \) on each possible target physical qubit \( i \), which we denote \( \epsilon(G_i) \).
- The estimated entanglement infidelity for each available two-qubit gate, indexed by the target physical qubits, \( i \) and \( j \), which we denote \( \epsilon(G_{i,j}) \).
- A readout error rate \( \epsilon(i) \) for each physical qubit \( i \) defined by
  \[
  \epsilon(i) = \frac{1}{2} \left( \Pr(1|0) + \Pr(0|1) \right),
  \]
where \( \Pr(x|y) \) is the probability of reading out \( x \) on qubit \( i \) after preparing that qubit in the state \( |y\rangle \).

Initialization errors are not reported separately, and are instead implicitly included in the readout error rate, so \( \epsilon(i) \) can be thought of as an average state preparation and measurement (SPAM) error. Further note that this standard form explicitly utilizes the entanglement infidelity, rather than the average gate infidelity that is the usual error metric associated with randomized benchmarking [6] (and which is the error metric used by IBM Q and Rigetti). The two infidelities are simply related to each other by the linear rescaling of Eq. (16).

B. Constructing a predictive model

This standard form given above for the error rate set \( \{\epsilon\} \) does not directly constitute a predictive model. Below we describe several increasingly detailed approaches for converting the descriptive error rates into predictive models of circuit success probabilities, and we highlight the method that we actually used.

1. A simple error accumulation formula

The simplest approach to predicting the success probability \( S \) of a circuit \( C \) is to compute the probability that no error happens over the course of the circuit. This is simply the product of one minus the error rates of all the operations in \( C \). In the small error and small circuit limit, the predicted failure rate \( 1 - S \) is then approximately the sum of the error rates of the constituent operations. So for the circuit \( C = RL_dL_{d-1} \cdots L_2L_1I \), we have:

\[
S = s(R)s(L_d) \cdots s(L_2)s(L_1)s(I),
\]
where \( s(L) \) is the success probability of layer \( L \) given by the product of one minus the error rates of the layer’s constituent operations:

- For the initialization layer \( I \), \( s(I) = 1 \). As discussed above, errors in the initialization are captured by the “readout” error rates.
- For a gate layer \( L \)
  \[
s(L) = \prod_{G \in L} (1 - \epsilon(G)),
  \]
where the product is over the particular one- and two-qubit gates (on particular qubits) from which \( L \) is constructed.
- For the readout layer \( R \)
  \[
s(R) = \prod_{i \in Q} (1 - \epsilon(i)),
  \]
where \( Q \) is the set of indices of the qubits on which \( C \) acts.

2. The global depolarization model

Equation (48) is simple and intuitive, but it is flawed. This is because it implicitly assumes that two or more errors cannot cancel, and so it predicts that \( S \to 0 \) as circuit depth \( d \to \infty \) rather than \( S \to \frac{1}{2^w} \). So, instead, we use a formula that corrects for this. We predict \( S \) using

\[
S = \frac{1}{2^w} + (s(R) - \frac{1}{2^w}) \lambda(L_d) \lambda(L_{d-1}) \cdots \lambda(L_1),
\]
where

\[
\lambda(L) = \frac{1}{1 - 4^w} \left( 1 - 4^w \prod_{G \in L} (1 - \epsilon(G)) \right).
\]

Although this formula might seem much more complex than Eq. (48), it follows simply from modeling the error in each gate layer as a global \( w \)-qubit depolarizing channel [see Eq. (13)] with an entanglement fidelity equal to the product of the entanglement fidelities of the constituent gates — which is how entanglement fidelity composes under tensor products. Moreover, note that this formula for \( S \) depends approximately only on the number of times each gate (and readout) appears in the circuit. This holds only approximately because errors compose differently when they occur in parallel or in serial (errors on different qubits that occur in the same layer cannot cancel, where errors on different layers can cancel).
3. The local depolarization model

An alternative model in which to embed the error rates is a local depolarizing model. In this model, each one-qubit gate $G_i$ is modeled as the perfect unitary followed by the one-qubit depolarizing channel $D_{1,\epsilon(G_i)}$ and each two-qubit gate $G_{i,j}$ is modeled as the perfect unitary followed by the two-qubit depolarizing channel $D_{2,\epsilon(G_{i,j})}$ [again, see Eq. (13) for the definition of a w-qubit depolarizing channel]. This is arguably more physically well-motivated than the global depolarizing model, because it is consistent with the characterization experiments from which the errors rates are extracted — that is, under this model, one- and two-qubit randomized benchmarking will return the error rates used in the model (up to scaling differences between average gate and entanglement fidelity). However, unlike the previous two models, the local depolarization model does not lend itself to a compact, analytical formula for the success probability. In order to make predictions from a local depolarizing model it is necessary to simulate the circuit.

Because our benchmarks use Clifford circuits, weak simulation (i.e., sampling from the circuit’s output distribution) under local depolarization is efficient in both circuit depth $d$ and width $w$. Strong simulation (i.e., computing the success probability exactly) is expensive, however, scaling exponentially in $d$. Somewhat surprisingly, the success probabilities predicted by this model are typically approximately the same as those predicted by a corresponding global depolarizing model. This is because, under either model, a circuit’s success probability is controlled only by (1) the rate that errors occur and (2) the rate that errors cancel. The error occurrence rate is equal in both models, and the error cancellation rate is almost equal in both models unless there is a large variance in the gate error rates on different qubits. For these reasons, we choose to use the global depolarizing model in this work.

VIII. EXPERIMENT #1

The purpose of this appendix is to describe the benchmarking experiments and data analysis summarized in Fig. 1d of the main text. Throughout these appendices we refer to these benchmarking experiments collectively as experiment #1. This appendix is not intended to be self-contained, and we make explicit references to earlier appendices when necessary. This appendix consists of two parts: in Appendix VIII A we detail the experiments, and in Appendix VIII B we detail the data analysis.

A. Experimental details

Experiment #1 used randomized mirror circuits to benchmark each of the twelve processors shown schematically in Fig. 1d. The benchmarking circuits were designed using a procedure we refer to as benchmark #1 that can be applied to any gate-model quantum information processor. Benchmark #1 has two notable properties: First, it was designed specifically for processors with fewer than \( \sim 20 \) qubits (in contrast to the benchmark of experiment #2, described in Appendix IX). Second, these benchmarking experiments took place over a period of time during which our methods were still under active development (the experiment dates range from July 2018 to November 2019), and so some minor aspects of the procedure changed over this time. We will note these changes explicitly as we introduce the benchmark. It was not possible to re-run all of the experiments with identical procedures, because not all of the processors were available for the full period of this research (in particular, IBM Q Rueschlikon, IBM Q Tenerife, Rigetti Agave and Rigetti Aspen-6 were no longer available in autumn 2019). This contrasts with experiment #2 (see Appendix IX) which is entirely standardized across the eight tested processors.

1. Circuit benchmarking algorithms

Benchmark #1 is an algorithmic approach for generating mirror circuit benchmarks to run on generic gate-model quantum information processors. It utilizes the following processor-specific information:

1. A single-qubit gate set $G_1$. We assume that all gates in $G_1$ can be applied to any qubit on the processor.

2. A two-qubit gate $G_2$. Without loss of generality, this gate is assumed to be asymmetric and may be applied to any adjacent qubits on the processor’s directed connectivity graph. (Fig. 1d displays the undirected connectivity graphs for each of the twelve processors we tested).

The algorithm then generates a suite of circuits to run on the target processor. The qubits in each circuit are explicitly assigned to specific physical qubits, and the circuits are composed of layers built from $G_1$ and $G_2$ gates allowed by the device’s connectivity. The motivation for choosing this sort of benchmarking circuits is covered in detail in Appendix III.

2. Gate set

The IBM Q and Rigetti processors use different native gate sets. For this reason, we chose different gate sets for IBM Q and Rigetti processors:

- IBM Q processors:
  
  \[ G_1 = \mathbb{C}_1, \text{ where } \mathbb{C}_1 \text{ is the set of all } 24 \text{ single-qubit Clifford gates}, \]
  
  \[ G_2 = \text{CNOT}. \]

- Rigetti processors:
  
  \[ G_1 \] comprises an idle gate, the three other single-qubit Pauli gates, and $\pm \pi/2$ rotations around $\hat{x}$ and $\hat{z}$. $G_1$ is a strict subset of $\mathbb{C}_1$.
  
  \[ G_2 = \text{CPHASE}. \]
In contrast, in experiment #2 we standarized the single-qubit gate set (to $G_1 = C_1$).

3. Circuit shapes

The first step in the benchmark #1 algorithm is to select the set of circuit shapes at which to construct benchmarking circuits. For an $n$-qubit processor, we chose the circuit shapes $(w, d) \in \mathcal{W}_n \times \mathcal{D}$, where:

$$\mathcal{W}_n = \{ 2^j \mid j \in [0..\lceil \log_2(n) \rceil] \} \cup \{n\} \quad (53)$$

$$\mathcal{D} = \{ 4, 14, \ldots, n \} \quad (54)$$

The circuit widths $w \in \mathcal{W}_n$ are powers of 2, with $w = n$ additionally included as the largest width (regardless of whether $n$ itself is a power of 2 or not). The benchmark depths $d \in \mathcal{D}$ are approximately exponentially spaced. We enforce that all depths are an integer multiple of 4, as this is a requirement of randomized mirror circuits (see Appendix V). For six of the twelve experiments (IBM Q Rueschlikon, IBM Q Melbourne, IBM Q Tenerife, Rigetti Agave, Rigetti Aspen 4 and Rigetti Aspen 6) we excluded depths $\{56, 112, 160, 224, 316\}$. For the other six experiments, which were all on 5-qubit IBM Q processors, we iteratively excluded the largest depth as the width was increased, i.e., shapes $(2, 316), (3, 316), (3, 224), (5, 316), (5, 224)$, and $(5, 160)$ where excluded. These choices were made in order to reduce the number of circuits required and/or due to limitations in what a particular processor could run.

4. Circuit embeddings

For any circuit width $w < n$ we must select a set (or several sets) of $w$ connected physical qubits before generating our benchmark circuits. This is because our benchmarks use layers of native gates, so we need to ensure that our circuits respect the connectivity constraints of the $w$ selected physical qubits. For most common connectivity graphs, as $n$ increases there is a rapidly increasing number of distinct connected sets of $w$ qubits for any non-extremal width (i.e., a width $w$ satisfying $1 \ll w \ll n$). For each width $w$ we select multiple width-$w$ sets $s_w$. We do so as follows:

- For a processor of $n \leq 5$ qubits, for each width we select each possible set of $w$ connected qubits.
- For a processor of $n > 5$ qubits, for each width $w$ we select $\lceil w/\text{width} \rceil$ sets of $w$ connected qubits whereby every qubit is in at least one set of each size (here $\lceil \cdot \rceil$ denotes the ceiling function, i.e., rounding up).

5. Circuit sampling

For each processor, each circuit shape $(w, d)$, and each chosen set of $w$ qubits ($s_w$) we sampled 40 shape-$(w, d)$ randomized mirror circuits acting on those $w$ qubits. These circuits were constructed using the $\chi_1$ sampler introduced in Appendix VB.1. The code that we used to perform this sampling has been incorporated into the open-source software package pyGSTi [51, 52].

6. Experimental details

We ran benchmark #1 on the twelve processors shown in Fig. 1d. The experiments were run using the online access services of IBM Q [24] and Rigetti [25]. Both IBM Q and Rigetti routinely recalibrate their processors; all of the circuits were run within a single calibration window. Each circuit was repeated 1024 times, except for the experiments on Rigetti Agave, where each circuit was repeated 1000 times. For our first six experiments (IBM Q Melbourne, IBM Q Rueschlikon, IBM Q Tenerife, Rigetti Agave, Rigetti Aspen 4 and Rigetti Aspen 6), equal-depth, single-qubit circuits on different qubits were implemented simultaneously [15]. That is, for each processor and each circuit depth $d$, the $40n$ width-$n$ circuits were combined into 40 width-$n$ circuits consisting of running one of the 40 depth-$d$ circuits for each qubit in parallel. For the circuit embedding strategy for processors of more than five qubits, this approximately halves the total number of circuits that need to be run. In an ideal processor, running these circuits in parallel has no effect on their outputs, but for real processors this is typically not the case, due to pulse spillover and other crosstalk effects [15, 40]. So, in our later six experiments (IBM Q Yorktown, IBM Q Ourense, IBM Q Essex, IBM Q London, IBM Q Vigo, and IBM Q Burlington), we ran the width-1 circuits separately. We did not parallelize any of the $w > 1$ circuits in any of our experiments, as two-qubit gate crosstalk is known to often be a significant effect in superconducting chips [9, 53, 54].

B. Data analysis

The results of experiment #1 are summarized in the volumetric benchmarking plots [26] of Fig. 1d. Here we explain the data analysis used to generate these plots. In this appendix we use notation that distinguishes between a circuit’s true success probability ($\delta$) and an observed success probability ($\hat{\delta}$) obtained from a finite number of repetitions of that circuit. As noted above, for some processors we left out depth 56 in order to reduce the total number of circuits. For these processors, in the plots in Fig. 1d the boxes (and frontiers) at depths 40 and 80 are stretched horizontally to meet at depth 56, so that there is no empty space in the plots.
1. Circuit polarization

For each circuit that we ran, we calculate the observed polarization

\[ \hat{P} = (\hat{S} - \frac{1}{2^e})/(1 - \frac{1}{2^e}), \]  

(57)

where \( \hat{S} \) is that circuit’s observed success probability and \( w \) is the circuit’s width. The polarization removes few-qubit effects. If a processor is subject only to depolarizing noise, then \( 1 \geq \hat{S} \geq \frac{1}{2^e} \), and as \( d \rightarrow \infty \) then \( \hat{S} \rightarrow \frac{1}{2^e} \) for any shape \((w, d)\) circuit. This is because a deep circuit will output \( w \) uniformly random bits. So, under this noise model, \( \hat{P} \rightarrow 0 \) as \( d \rightarrow \infty \) and \( 1 \geq \hat{P} \geq 0 \) for any width circuit. Note that \( \hat{P} \) can be negative, which can be caused by finite sampling or because \( P \) itself can be negative under more general error models.

2. Selecting the best qubits

For each benchmarked circuit shape \((w, d)\) and each benchmarked subset of \( w \) qubits \((s_w)\) we ran 40 distinct randomized mirror circuits and measured 40 corresponding observed polarizations \( \hat{P} \). These polarizations are collected into a set \( \hat{P}(w, d, s_w) \) for each circuit shape and qubit set. For each width \( w \), the first step in our analysis is to identify the single set of qubits \( b_w \) that we deem to have performed the best on our benchmarking circuits. We then discard the data for all other qubit sets, and generate volumetric benchmarking plots using only \( \hat{P}(w, d) \equiv \hat{P}(w, d, b_w) \).

We select \( b_w \) to be the \( w \) qubits with the largest \( d_{\text{mean}} \), where \( d_{\text{mean}} \) is the smallest depth at which the mean polarization drops below \( \frac{1}{e} \). When more than one of the benchmarked sets of \( w \) qubits have the same value for \( d_{\text{mean}} \) we choose the set of qubits with the largest mean polarization at that depth. This process means that we have selected the \( w \) qubit subsets that maximize the depth of the processor’s mean polarization \( \frac{1}{e} \) frontier, which is the solid black line in each panel of Fig. 1d (discussed below).

3. Maximum, minimum and mean polarization

In the volumetric benchmarking plot for each processor in Fig. 1d, we display the best, average, and worst case polarization versus circuit shape for the best-performing sets of qubits. That is, at each circuit shape \((w, d)\), we plot the maximum, mean, and minimum of \( \hat{P}(w, d) \). A circuit’s polarization can be negative, so we truncate each of our performance metrics to zero. In the case of the mean, this truncation occurs after averaging.

4. Performance frontiers

In each panel of Fig. 1d we plot three frontiers, corresponding to the circuit shapes at which the maximum, mean and minimum polarizations drop below \( \frac{1}{e} \). For performance frontiers it is often useful to account for finite sampling effects, i.e., to adjust for the finite number of repetitions of each circuit. Details of this statistical analysis are given below. For now, we assume a statistic-specific function \( f \) that takes \( \hat{P}(w, d) \), the set of observed polarizations, and returns “pass” or “fail” for that circuit shape.

It is convenient to enforce that the frontier be monotonic, in the sense that as width or depth is increased the boundary is guaranteed to only be crossed once. So, given an \( f \) function, the frontier is calculated as follows:

1. For each tested circuit shape \((w, d)\) use \( f(\hat{P}(w, d)) \) to designate that circuit shape as a “pass” or a “fail”.

2. Set the frontier to the border of the largest region \( R \) for which, if \((w', d') \in R, w \leq w', \) and \( d \leq d' \), then \( f(\hat{P}(w, d)) = \text{“pass”} \).

Of course, frontiers may be calculated for any threshold value. We choose \( \frac{1}{e} \) because circuit polarization will decay exponentially with the benchmark depth under the simplest error model — uniform, layer-independent depolarization (i.e., a global depolarizing channel with the same error rate for every circuit layer). When the decay is approximately exponential the frontier is a visual representation of the rate of this approximately exponential decay.

5. Accounting for finite sample fluctuations

The most appropriate method for accounting for the finite number of repetitions of each circuit \((N)\) when calculating a statistic’s frontier depends on the inferences that will be made from that frontier. In the case of the mean, we use the “raw” frontier that has no finite sampling adjustments. That is, for the mean, we use an \( f \) function that simply returns “pass” if the mean of \( \hat{P}(w, d) \) is above \( \frac{1}{e} \) and otherwise it returns “fail”. This is an unbiased estimate of whether the mean polarization is above or below the threshold value, and so it is a natural choice.

Different choices are possible of course, and statistical hypothesis testing [55] provides a rigorous framework for constructing broad classes of thresholding functions. For the case of the mean, for instance, one may desire a function \( f \) that hypothesizes the mean is above a threshold, returning “fail” if and only if there is statistically significant evidence that the mean is below the \( \frac{1}{e} \) threshold value. For the maximum and minimum frontiers, we will utilize this hypothesis testing framework exclusively.

In the main text we use the observation of a substantial discrepancy between the maximum and minimum frontiers as evidence that that processor is subject to highly structured errors. We therefore chose to calculate the maximum and minimum frontiers using a statistical hypothesis test that is designed so that the boundaries will be equal if there is no statistically significant evidence in the data to the contrary. This therefore guarantees that any observed discrepancy is not simply an artifact of finite \( N \).

At each circuit shape, we start from the null hypotheses \( H_0 \) that either \( H_1 \) is true or \( H_1 \) is true, where:

\[ H_0: \]}

```
• $H_1$ is the hypothesis that every circuit of this shape that we ran has a polarization that is above the $\frac{1}{e}$ threshold.

• $H_1$ is the hypothesis that every circuit of this shape that we ran has a polarization that is below the $\frac{1}{e}$ threshold.

Note that these hypotheses are about the circuits that we ran, not the distribution of circuits from which they were sampled. Starting from the $H_0$ hypothesis at each circuit shape encodes our aim of starting from the assumption that the maximum and minimum frontiers are equal. Only if we can reject $H_0$ at a given circuit shape, using a statistical hypothesis test with 5% significance, do we assign “pass” to the maximum polarization and “fail” to the minimum polarization. Otherwise we assign “pass” or we assign “fail” to both statistics (using the strategy outlined below).

To test the null hypothesis $H_0$ at a given circuit shape, we perform two statistical hypothesis tests at 5% significance — one that tests for evidence to reject $H_1$, and one that tests for evidence to reject $H_1$. Because we must reject both $H_1$ and $H_1$ to reject $H_0$, the significance of this type of test for $H_0$ is 5%.

The two tests that we use are equivalent, so we only describe the test of $H_1$. This test is more simply described in terms of each circuit’s observed success probability $\hat{S}$, rather than in terms of the polarizations.

The statistical hypothesis test of $H_1$ that we use consists of $K$ log-likelihood ratio tests [53], where $K$ is the number of circuits of that shape (here $K = 40$). We test whether each observed success probabilities $\hat{S}$ is consistent with the null hypothesis that it is the average of $N$ draws from a 0/1-valued “coin” with a probability $S$ to output 1 that is above $T_S = (1 + 1/e)1/e + 1/2^e$ ($T_S$ is the $1/e$ polarization threshold rescaled to the equivalent success probability threshold). There are $K$ hypothesis tests performed, and so to maintain the test significance to 5% we must account for this. We do so using the Benjamini-Hochberg procedure [56]. We then reject $H_1$ if any of the tests indicate that their circuit’s $S$ is below $T_S$. This is similar to rejecting $H_1$ if the smallest p-value in these $K$ tests is smaller than $0.05/K$, which is the well-known Bonferroni correction, but this testing procedure is more powerful. (The Benjamini-Hochberg procedure with $\alpha$ significance guarantees that, if all the tested null hypotheses are true, the probability of rejecting one or more null hypotheses is at most $\alpha$. This is known as weak control of the family-wise error rate. As we are using these 40 tests as a method for testing the composite null hypothesis $H_1$ that is true if and only if all of the individual null hypotheses are true, this is sufficient to maintain the test significance.)

There are four possible results of these two hypothesis test, corresponding to all combinations of rejecting or not rejecting $H_1$ and $H_1$. As we already noted, if we reject both hypotheses (and so we reject $H_0$) then we assign “pass” to the maximum polarization and “fail” to the minimum polarization. Otherwise, we assign the same output for both the maximum and minimum polarization as follows:

• If we reject $H_1$ but not $H_1$ then we designate both the maximum and minimum polarization as “pass.”

• If we reject $H_1$ but not $H_1$ then we designate both the maximum and minimum polarization as “fail.”

• If we reject neither $H_1$ or $H_1$ then we designate the maximum and minimum polarization as both “pass” (“fail”) if the maximum polarization (minimum polarization) is further from the $1/e$ threshold than the minimum polarization (maximum polarization).

Alternative techniques for generating frontiers from data may be preferable in other contexts.

IX. EXPERIMENT #2

The purpose of this appendix is to describe the experiments, and the corresponding data analysis, that are summarized in Figs. 2-3 of the main text. Throughout these appendices we refer to this as experiment #2. This appendix is not intended to be self-contained, and we make explicit references to earlier appendices when necessary. This appendix consists of two parts: in Appendix IXA we detail the experiments, and in Appendix IXB we detail the data analysis.

A. Experimental details

Experiment #2 used both randomized mirror circuits (see Appendix V) and periodic mirror circuits (see Appendix VI) to benchmark each of eight processors and to compare their performance on disordered and ordered circuits. The benchmarking circuits were designed using a procedure that we refer to as benchmark #2. As with benchmark #1 (see Appendix VIII), this procedure can be applied to any gate-model quantum information processor.

1. The gate set

As with benchmark #1 of experiment #1, benchmark #2 is an algorithmic approach for generating mirror circuit benchmarks to run on generic gate-model quantum information processors. It is parameterized by a processor’s two-qubit gate $G_2$ and the processor’s directed connectivity graph. Unlike benchmark #1, it uses a standardized single-qubit gate set $G_1$ consisting of all 24 single-qubit Clifford gates ($C_1$) for all processors. As in experiment #1, we used the native two-qubit gate for each processor, which is CNOT for IBM Q processors, and CPHASE for Rigetti processors.

2. The circuit shapes

The first step in the benchmark #2 algorithm is to select the set of circuit shapes at which to construct benchmarking circuits. For an $n$-qubit processor, we chose the circuit shapes
\((w, d) \in \mathbb{W}_n \times \mathbb{D}\), where:
\[
\mathbb{W}_n = \{1, 2, 3, 4, \ldots, n\}, \quad \mathbb{D} = \{0, 4, 8, 16, 32, 64, 128, 256, 512\}.
\]
Exponentially spaced widths would likely be preferable for larger processors, but for the processors we tested, running circuits at an exhaustive set of widths is feasible. For the larger widths we excluded the largest depths, as the processors’ error rates implied that all circuits of these shapes would almost certainly all fail. The exact combination of circuit shapes tested can be seen in Fig. 7. Circuits with depths of 1024 and above were not included only because the IBM Q interface did not allow these circuits to be run.

3. The circuit embeddings

For each processor, we ran width-\(w\) circuits on a single set of \(w\) qubits. We chose the \(w\) qubits predicted to perform the best on our benchmark, according to a simple heuristic based on the processor’s published error rates. As is the case for choosing the “best” performing qubits from data — which we did in the data analysis for experiment #1 (see Appendix VIII) — there are many reasonable ways to use the error rates to choose this qubit set. Using the standard form error rate set \(\{\epsilon\}\) introduced in Appendix VII A, we do so as follows:

1. We model the success probability for a shape \((w, d)\) benchmarking circuit on the qubit set \(q_w\) as
\[
S = (s(R) - 1/2^w) \lambda_1^{ld(w-\xi)} \lambda_2^{ld(1/2^w)} + 1/2^w, \quad (58)
\]
where
- \(s(R)\) is the success rate of the readout error layer for those qubits, defined in Eq. (50),
- \(\xi\) is the target two-qubit gate density of the benchmarking circuits (in these experiments, \(\xi = 0\) for \(w = 0\) and \(\xi = 1/8\) otherwise),
- \(\lambda_1 = 1 - \frac{\epsilon_1}{2^w}\) where \(\epsilon_1\) is the mean error rate of the one-qubit gates on the \(s_{\epsilon}\), and
- \(\lambda_2 = 1 - \frac{16\epsilon_2}{2^w}\) where \(\epsilon_2\) is the mean error rate of the two-qubit gates between the qubits in \(q_w\).

This formula is a heuristic for predicting the expected success probability of a shape \((w, d)\) randomized mirror circuit with a two-qubit density of \(\xi\).

2. For each connected qubit subset of size \(w\), we find the depth \(d\) for which Eq. (58) predicts that \(S = 1/2^w(1 - 1/2^w) + 1/2^w\). In terms of polarization \((P)\) this is the depth at which this equation predicts that \(P = 1/2\). Note that \(d\) is not restricted to being an integer, and it can be negative.

3. For each width \(w\), we select the connected qubit subset for which this depth is maximized.

This procedure is one reasonable method for selecting the “best” set of qubits using only a set of generic error rates for those qubits — but note that there are many possible alternative heuristics, and we do not claim our choice is optimal.

4. The circuit sampling

In this experiment we ran randomized mirror circuits and periodic mirror circuits. As the aim was to investigate the role of circuit order/disorder on circuit failure rates, they were designed to have similar properties.

- The randomized mirror circuits were sampled using the edge-grab sampler introduced in Appendix VB 2. The expected two-qubit gate density was set to \(1/8\).
- The periodic mirror circuits were sampled using the algorithm introduced in Appendix VI B 1. The two-qubit gate density of these circuits is approximately bounded by \(1/8\) (it is rigorously bounded by \(1/8\) except when a partial repetition of a germ is required — see Appendix VI B 1).

We sampled 40 randomized mirror circuits and 40 periodic mirror circuits for each circuit shape \((w, d)\). As with experiment #1, the circuits are constructed after identifying the expected best \(w\)-qubit set at each width \(w\). This allows us to ensure that the benchmark circuits respect connectivity constraints.

Because the periodic mirror circuits are also randomly sampled from a distribution (see Appendix VI B 1), for the remainder of this appendix we will refer to the randomized mirror circuits in this experiment as disordered mirror circuits. The code that we used to perform this sampling has been incorporated into the open-source software package pyGSTi [51, 52].

5. Experimental details

We ran benchmark #2 on eight of the twelve processors that we tested in experiment #1. The four devices benchmarked in experiment #1 but not in experiment #2 (IBM Q Reuselikon, IBM Q Tenerife, Rigetti Agave and Rigetti Aspen 6) were no longer available once we had designed this benchmark. At the time of these experiments, 8 of the 16 qubits in Rigetti Aspen 4 were not functioning, so it was tested as an 8-qubit processor (whereas all 16 qubits were available when we ran benchmark #1 on Aspen 4). The experiments were run using the online access services of IBM Q [24] and Rigetti [25]. We implemented two “passes” through the circuits [53]: the circuits were looped through with each circuit repeated 1024 times, and then we repeated this a second time (see Fig. 8 for more details). Both passes through all the circuits were run within the same calibration window. Unlike in experiment #1, none of the circuits were run in parallel.

B. Data analysis

The results of experiment #2 are summarized in Figs. 2 and 3 of the main text. For brevity, Fig. 2 shows the results for only four of the eight benchmarked processors, so in Fig. 7 we expand on Fig. 2 to show the results for all eight processors.
In the remainder of this appendix we explain the data analysis used to generate these plots. We use notation that explicitly distinguishes between a circuit’s true success probability ($S$) and the observed success probability ($\hat{S}$) obtained from a finite number of repetitions of that circuit. Because the data was taken in two passes, it is useful to further distinguish between a circuit’s true and observed success probability at the time of the first pass through the circuits ($S_1$ and $\hat{S}_1$, respectively) and a circuit’s true and observed success probability at the time of the second pass through the circuits ($S_2$ and $\hat{S}_2$, respectively). If the processor is stable then $S_1 = \hat{S}_1$ for every circuit, but this is not guaranteed to be true, as drift is a common problem in quantum processors [20, 53, 57].

1. Quantifying processor instability

The first step in our data analysis identifies instability in the processors by comparing the two passes through the benchmarking circuits using the statistically rigorous hypothesis testing technique of Ref. [53]. Although the results of this analysis are an informative performance benchmark in their own right, this analysis was primarily implemented so that the presence (or absence) of detectable instability could be used to inform other aspects of the data analysis. The formal aim of this analysis is to assess whether there is statistically significant evidence in the data that $S_1 \neq \hat{S}_2$ for any circuit. The analysis performs statistical hypothesis tests of the null hypothesis that $S_1 = \hat{S}_2$ for each circuit. Fig. 8 plots $(1 - \hat{S}_1)$ versus $(1 - \hat{S}_2)$ for every periodic (upper row) and disordered (lower row) mirror circuit that was run on each processor (the columns). Solid circles (transparent stars) denote the observed failure probabilities that are (are not) sufficiently different to constitute statistically significant evidence that $S_1 \neq \hat{S}_2$ for that circuit, according to the hypothesis tests of Ref. [53]. (The procedure of Ref. [53] is designed for strong control of the family-wise error rate. We implemented the hypothesis test at 5% significance. The test significance is not corrected to account for the fact that we are testing eight different processors.)

There is statistically significant evidence in the data that all eight processors are unstable between the two passes through the circuits, i.e., for every processor there is evidence that there is at least one circuit for which $S_1 \neq \hat{S}_2$. However, the magnitude of the instability varies dramatically between processors. For example, the difference between $\hat{S}_1$ and $\hat{S}_2$ is small for every circuit that was run on IBM Q Yorktown, whereas many circuits exhibit large differences between $\hat{S}_1$ and $\hat{S}_2$ for IBM Q Melbourne and Rigetti Aspen 4. We note that the experiment on IBM Q Melbourne took approximately 10 hours whereas all other experiments took under 3.5 hours, so the difference between the observed instability on IBM Q Melbourne and the other IBM Q devices should not be used to infer that IBM Q Melbourne suffered from worse instabilities than the other IBM Q devices. As we explain further below, because of the results of this instability analysis we discarded the data from the second pass through the circuits — i.e., we used only the data from the first pass in the remainder of the
Figure 8. **Quantifying temporal instability.** Experiment #2 consisted of both periodic and disordered mirror circuits. These circuits were run in four batches in the following order: all the periodic circuits (pass 1), all the disordered circuits (pass 1), all the periodic circuits (pass 2), all the disordered circuits (pass 2). We thus obtained observed success probabilities, $\hat{S}_1$ and $\hat{S}_2$, for each circuit in passes 1 and 2, respectively. For each processor, this figure plots each circuit’s observed failure rate in the first pass ($1 - \hat{S}_1$) versus the circuit’s observed failure rate in the second pass ($1 - \hat{S}_2$). The upper (lower) row shows data from the disordered (periodic) circuits. Solid circles (translucent stars) are data for which the difference between the failure rates in the two passes is (is not) 5% statistically significant as assessed using the technique of Ref. [53]. For further details, see Appendix IX B 1.

analysis.

### 2. Worst-case volumetric benchmarks

In Fig. 7a (and Fig. 2a) we summarized the difference between the success rates of periodic and disordered circuits in terms of worst-case performance. For each processor and each benchmarked shape ($w, d$), Fig. 7a (and Fig. 2a) shows the observed polarization versus circuit shape ($w, d$) for periodic (outer squares) and disordered (inner squares) circuits, minimized over all the test circuits of shape ($w^*, d^*$) where $w^* \leq w$ and $d^* \leq d$. This was calculated using only the data from the first pass through the circuits.

The observed minimum polarization is a biased estimate for the true minimum polarization over a circuit ensemble. If each circuit’s success probability was stable over time, this bias could be removed by using the data from the first pass through the circuits to select the worst-performing circuit for each circuit shape, and then using the data from the second pass to estimate these circuits’ polarizations. However, the validity of that strategy is based on the assumption of stability, and there are large instabilities between the two passes for some processors (see Fig. 8). As the purpose of Fig. 2a is to compare periodic and disordered circuits, and we ran the same number of periodic and mirror circuits of each shape and we ran every circuit the same number of times, we therefore chose to make no adjustment for finite sampling in the analysis for Fig. 2a.

3. **Comparing to the predictions of each processor’s error rates**

In Fig. 7b-c (and Fig. 2b-c) we compare our experimental results to predictions derived from each processor’s published error rates. The method used to predict the success probability for a specific circuit is explained in Appendix VII. Fig. 7c simply plots the predicted failure probability (i.e., one minus the predicted success probability) against the observed failure probability ($1 - \hat{S}$) for every circuit that we ran. This is arranged by processor (the rows) and is further split into periodic and disordered mirror circuits (the left and right columns, respectively). As with all of Fig. 7c, we include only the data from the first pass through the circuits.

In Fig. 7b we show volumetric benchmarking plots of the predicted worst-case performance implied by the processors’ error rates. As discussed above, the analysis resulting in Fig. 7a does not correct for finite sampling bias in the estimate of each of the minimum polarizations. To ensure that Fig. 7b may be fairly compared to Fig. 7a, we simulate this bias using a standard parametric bootstrap. For each processor:

1. We generated 1000 bootstrapped data sets, by sampling an “observed” success probability for each circuit that we ran, given by the average of 1024 draws from a 0/1 valued “coin” with the success probability set to the predicted success probability of the circuit.

2. For each bootstrapped data set, we implemented exactly the same analysis that was applied to the experimental data to generate Fig. 7a. This analysis computes a statistic $\lambda(w, d)$ at each circuit shape ($w, d$). This results in 1000 bootstrapped values for each $\lambda(w, d)$.

3. The predicted $\lambda(w, d)$ is then set to the mean of the 1000 bootstrapped values.
4. Empirical capability regions

In Fig. 3 of the main text, we summarize the performance of all eight processors on both periodic and disordered mirror circuits, by dividing the circuit width \( \times \) depth plane into “success”, “indeterminate”, and “fail” regions. These regions correspond to the circuit shapes at which all, some, and none of the 80 test circuits succeeded, respectively, where a circuit is considered to succeed if \( P \geq \frac{1}{e} \). To estimate these regions from the data we use statistically hypothesis testing. We start from the null hypothesis that, at shape \((w, d)\), every circuit succeeds \((P \geq \frac{1}{e})\) or every circuit fails \((P < \frac{1}{e})\), and we assign a circuit shape to “indeterminate” only if statistical hypothesis testing on the data allows us to reject this null hypothesis with 5% statistical significance.

The statistical hypothesis testing is performed using the same technique that we used to generate the performance frontiers from the data in experiment #1 (this is described in detail in Appendix VIII B 5), and the analysis uses only the data from the first pass through the circuits. The reason for using this hypothesis testing framework is that it addresses a bias towards including every circuit shape in the “indeterminate” region. To understand this, consider running \( K \) circuits of shape \((w, d)\) with each circuit repeated \( N \) times and with these \( K \) circuits sampled from some circuit ensemble in which every circuit has a success probability that is not exactly 1 or 0. Then, for fixed \( N \), the probability of the observed polarization being above \( \frac{1}{e} \) for at least one of these \( K \) sampled shape \((w, d)\) circuits and being below \( \frac{1}{e} \) for at least one of these \( K \) sampled shape \((w, d)\) circuits converges to 1 as \( K \) increases, even if every circuit in the ensemble has a success probability well above the threshold value.