FlexRay bus data fault diagnosis based on Zynq

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Abstract. CAN bus and LIN bus are widely used as communication bus in automobile industry. As a new type of automobile bus, FlexRay bus, with CAN bus and LIN bus do not have many advantages. FlexRay bus bandwidth is not limited by protocol mechanisms, and it use the synchronization-based access methods. And because of its unique dual-channel data transfer mode, which is especially suitable for the current automotive wire control system, it replaces the mechanical and hydraulic working mode of traditional automobile. And the FlexRay data transmission rate is fast, it can quickly transmit data to the car's electronic control unit. Zynq as an extensible platform combining ARM and FPGA, satisfying the programmability of the software, it also meets the programmability of hardware. Zynq chip functions can be divided into two working parts, A PS, another is PL. PS is the ARM part, mainly responsible for data storage and display module control and other functions; PL is the FPGA part, the main functions are data acquisition processing and time unification. Using based on Zynq data diagnosis FlexRay vehicle bus, can make data transmission more reliable and efficient, It can also effectively reduce the power consumption of the whole system.

1. Basic Principle and Characteristics of FlexRay bus

1.1. Basic principles of FlexRay bus

It can be seen as a train operating system in the image of how it works, and the train on the track is the information frame, people are the information, the time of the crowd received by the train station is fixed, the train is running according to the schedule, whether the next station has passengers on or off, the FlexRay works very similar. When sending data through the FlexRay bus, each time point is fixed, and whether the bus user has data to transmit.

FlexRay bus communication structure is shown in figure 1.
Communication cycle
(Synchronous clock drive)

| Static segment-MAC based on TDMA | Dynamic segment-MAC based on variable TDMA/Dedicated communications, dynamic bandwidth requirements |
|----------------------------------|--------------------------------------------------------------------------------------------------|
| Fixed delay, low delay jitter communication, requires fixed bandwidth |                                                                                                   |

Fig.1. FlexRay Bus Communication Cycle Structure

The FlexRay bus communication cycle can be divided into static segment and dynamic segment according to its application application. The static segment data transmission adopts time trigger mode, which can meet the needs of high reliable system application. Dynamic segment is mainly based on event trigger mode, allowing each node to occupy full broadband data transmission.

1.2. Characteristics of FlexRay bus
As a new generation of automobile bus technology, FlexRay bus has the following characteristics:

1. Communication bandwidth. FlexRay bandwidth is not limited by the protocol mechanism, and the channel can communicate at the fastest rate of 10 Mbps. When the dual channel redundant system is adopted, the rate of up to 20 Mbps is much higher than that of the CAN bus.

2. Time certainty. FlexRay bus adopts time-division multiplex data transmission mode, which is based on cyclic communication cycle. The data has a fixed position in the communication cycle to ensure the timeliness of message arrival.

3. Distributed clock synchronization. The FlexRay bus uses the access method based on synchronous time, and the synchronization is automatically established and synchronized by protocol, and the accuracy of time base reaches 1µs.

4. Fault tolerant data transmission. FlexRay bus has a special fault-tolerant protocol and supports multi-level fault-tolerant capability, including providing redundant and extensible system fault-tolerant mechanisms for transmission through single-channel or dual-channel mode, to ensure the reliability of data transmission.

5. Flexibility. FlexRay bus supports bus, star, cascade star and hybrid topology, supports time-triggered and time-triggered communication mode, has redundant message transmission or non-redundant transmission mode, and provides a large number of configuration parameters for users to flexibly adjust and expand the system.

2. System framework design
2.1. System design
This design combines FlexRay bus technology with Zynq development platform to collect, store and diagnose automobile data, and transmit the diagnosed information to users. On the basis of Zynq, combined with Flexray bus technology, five nodes are designed on the FlexRay bus, setting up the data of five nodes on the bus, and the data of five nodes are always reading and sending information through the bus driver module. The bus driver module is mainly composed of TJA1080. Since each node of the FlexRay will have different acquisition, control, and load-driven modules, each module under the node uses independent bus communication, therefore, the FlexRay bus communication board with single bus is required. The bus control module based on MC9S12XF512 single chip
microcomputer not only has the control function of bus, but also has the information processing ability of node function module to meet the communication cooperation within the whole system.

In order to feedback node data to users well, further processing of data is needed. Zynq is an extensible processing platform, PL (FPGA) and PS (ARM) components, the part of FPGA is mainly data reprocessing, and ARM is to store and upload data and other works. The interconnection between PL and PS through AXI interface protocols, because AXI have better performance and higher banding, and we can effectively improve the accuracy and rate of in-chip communication, it can also reduce the power of the system. The FlexRay control module will send the collected data to the FPGA chip, and the FPGA chip caches data through SDRAM. And through the time unified module to mark the data time information, after that, the processed data is passed to the ARM module through in-chip communication, The display screen and memory are controlled by the ARM and the final data is transmitted to the PC for feedback to the user.

The overall structure of the system is shown in figure 2:

Fig. 2. Structure of the System

2.2. FlexRay Principle of Independent Bus Communication Control Circuit

The bus control circuit is mainly a bridge connecting the controller chip and the FlexRay bus node. The controller chip mainly sends and receives the data transmission instruction to the FlexRay bus node through the FlexRay transceiver circuit. The transceiver chip is mainly designed by TJA1080 chip. The transceiver circuit adds filter isolation circuit before receiving the node. In order to increase the stability and anti-interference ability of FlexRay bus data transmission. The TJA1080 is connected with the MC9S12XF512 MCU, the DR serial port of the single chip microcomputer is connected with the TJA1080 UART serial port, and the other pins of the TJA1080 are connected with the general I/O port of the single chip microcomputer to realize the detection and control of various states of the single chip microcomputer. The bus control circuit schematic diagram is shown in Figure 3:
DSP uses the sampling clock inside the buffer serial port, the buffer serial port can be configured to receive and send data, and the 1-bit data of UART corresponds to the 16-bit data of the buffer serial port. DSP software must extend the 1-bit data to be sent to 16-bit data, and also compress every 16 bits of data received into 1-bit data. This requires setting the sampling rate generator to generate an internal serial clock, 16 times the serial baud rate. Since each UART word starts with a descent edge that can be used as frame synchronization input, both the data line and the frame synchronization signal are connected to the UART. This signal can be obtained on the output.

2.3. Design of Zynq-based Data Acquisition and Processing Module
The whole module consists of the CPU, memory, Flash, ADC acquisition chip etc, SoC’s memory is DDR3. Another piece of SRAM as a brush cache. Combined with A/D conversion chips, external the LCD screen, the data can be collected, stored and displayed. One analog input system, the AD chip is converted into a digital signal and stored in PL part of the SoC chip, DMA module is designed in PL section to match the data transfer rate to memory, Software processed to display data from memory, Writes PL part to the SRAM cache, under PL control LCD the data in the SRAM can be displayed.

3. Design of Time Unified Module Based on FPGA
The time unified module is the module that provides the unified standard time signal and the standard frequency signal for the data fault diagnosis system. In short, the time information is added to the data in the data processing, which makes the data more real-time. Because of the particularity of fault diagnosis system, the fault information obtained is very accurate, and after adding time information, the feedback information obtained by users is clearer.

3.1. Time-Unified Module Principle

3.1.1. IRIG-B Code Coding Principle
IRIG-B code is a common serial transmission mode time format code. Compared with parallel transmission mode, it has simple physical connection, large amount of information, high resolution, long transmission distance, strong anti-interference ability and standardized interface. IRIG-B code adopts two types according to the different requirements of time accuracy and the transmission distance of IRIG-B code: B (DC) code and B (AC) code. B (DC) code each symbol is a pulse signal, which can achieve high precision time synchronization, but the pulse signal spectrum is rich, narrowband channel can not be transmitted, suitable for short-distance cable transmission; B (AC) code can be transmitted using standard speech bandwidth (0.3 kHz~3.4 kHz) channel. B (AC) code can be obtained by amplitude modulation of standard sinusoidal carrier by B (DC) code. Different code types can be selected according to different requirements. In this system, both codes are used.

3.1.2. General Design Principle of Module
The overall schematic block diagram of the time unity module is shown in figure 4:
Switch
The equipment
B-code
signal
IRIG-B Terminal
Unified time
signal
Unified time card
NTP
Network
time
Switch
Timing signal
The equipment

Fig. 4. The overall principle block diagram of the time unified module

The hardware of the time system module includes the time card and the IRIG-B code terminal. IRIG-B the code terminal can realize the redundant reception of the dual system time signal of the GPS satellite system, as well as the direct reception of the foreign B code signal. Multiple DC or AC IRIG-B codes are generated and sent to the unified time card. The unified time card automatically acquires the standard time information by receiving the IRIG-B code directly and decoding the circuit, sends the information of unified time system to the server with the unified time card through the VPX bus. After receiving the information of unified time system, the server can monitor and output the signal strictly to the server itself, workstation and terminal.

3.2. Overall design of the time unified module
FPGA complete the decoding of B code to achieve accurate time information extraction and communication with the VPX interface. FPGA program can complete the extraction of time information, the automatic switching of B (DC) code and B (AC) code, and can also realize the interrupt signal at different time through the PPS second pulse generated by the decoding process of the B code. The VPX interface program completes the reception of time information and interrupt signals and transmits them to the VPX bus. The B code terminal is connected with the time card. Under the condition of access GPS signal, the upper computer is used to read the output signal of the unified time system card.

4. Data simulation experiment

4.1. Simulation of experimental data transmission
Through the joint simulation of Quartus II 13.1 and ModelSim-Altera 10.1d to verify the normal operation of the system data acquisition, The data simulation waveform is shown in figure 5:

Fig. 5. Data Simulation Waveform
Through the software simulation results diagram, the simulation set eight bits of data, when the reset signal set 1, the system works normally. The received data changes at any time, consistent with the input results.

4.2. Simulation and testing of experimental results
Programming FlexRay bus controllers through Codewarrior. The data test diagram is shown in figure 6:
Sent through queries, reading the data from the port of "COM3", set port bit baud rate set to "9600", the data bit is set to "8", check bit set to None", the stop bit is set to "1". In order to ensure that the whole system can accurately and timely diagnose the car body fault information, set here to read data all the time, and here the data is set to default to "1000", send PC analog data to the FlexRay bus controller, FlexRay bus will controller transfers data to the FPGA for processing and adds time data ,when it is 1000.

Serial data test diagram Zynq further processing the data received from the FlexRay controller to better transfer the data to the user, and transfer the data to the PC end through the USB interface and save it. The final results of the experiment are shown in figure 7.

5. Conclusion
The system takes FlexRay bus and Zynq-7035 chip as the core, it combines the FlexRay bus control module, data acquisition module and result processing module, and builds a system that can monitor and diagnose the body information in real time and feedback to the user in time. The system combines the high speed of the FlexRay bus and the low power consumption and real-time of the Zynq chip. It is faster than the data diagnosis of other systems. The addition of the time unified module makes the data real-time. Users can obtain car body fault information more accurately. According to the final experimental test, the obtained results achieve the desired results, and can obtain the information of the car body in real time and accurately.

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