Optogenetics in Silicon: A Neural Processor for Predicting Optically Active Neural Networks

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Abstract—We present a reconfigurable neural processor for real-time simulation and prediction of opto-neural behaviour. We combined a detailed Hodgkin–Huxley CA3 neuron integrated with a four-state Channelrhodopsin-2 (ChR2) model into reconfigurable silicon hardware. Our architecture consists of a Field Programmable Gated Array (FPGA) with a custom-built computing data-path, a separate data management system and a memory approach based router. Advancements over previous work include the incorporation of short and long-term calcium and light-dependent ion channels in reconfigurable hardware. Also, the developed processor is computationally efficient, requiring only 0.03 ms processing time per sub-frame for a single neuron and 9.7 ms for a fully connected network of 500 neurons with a given FPGA frequency of 56.7 MHz. It can therefore be utilized for exploration of closed loop processing and tuning of biologically realistic optogenetic circuitry.

Index Terms—ChR2, FPGA, Hodgkin–Huxley, neural processor, neuromorphic circuits, neuroprothesis, optogenetics.

I. INTRODUCTION

OPTOGENETICS involves a genetic modification of cells to make them sensitive to light by expressing light-gated cation channels such as Channelrhodopsin-2 (ChR2) [1] or anion channels in their cell membranes [2]. It has attracted interest from multiple disciplines, particularly due to its ability to genetically target neural sub-circuits, paving the way for high spatial and temporal resolution with perhaps better biocompatibility than with electrical approaches [1]. Some promising translational neuropsychiatric therapies to date include pacemakers for epilepsy [4], [5] and visual prostheses [6].

The kinetics of the molecule, were previously explored from an engineering viewpoint by ourselves (Nikolic et al. [7] and Grossman et al. [8]) using data from optogenetically transfected hippocampal cells. However there are still challenges to be addressed, such as how to physically stimulate large numbers of neurons. More importantly, how can therapeutic or scientific network stimulation protocols be translated into a particular three-dimensional light pattern? Such questions will be application-specific and can be answered either empirically or through modelling. The latter would require accurate software models. To explore further, bio-silicon hybrid networks could be used, with the potential for exploring both basic science and downstream translation.

A range of methodologies exist to simulate and predict the state of neural networks. These differ in their accuracy of mathematical representation as well as their scope and range of biological features. Abstract models such as integrate-and-fire [9], Izhikevich [10], and Hindemarsh-Rose [11] provide computational efficiency. This allows scaling to large network simulations (of many thousands of neurons) on commodity hardware. There is however a need for more moderate sizes of neural networks but with bio-realism and real-time operation. In particular, optogenetics can provide stimuli to relatively localized neuronal circuitry. This requires the combination of optogenetic models with spatially detailed Hodgkin–Huxley models of neurons [12]. Such a system could potentially interpret recordings and command stimulation equipment in real time (through closed loop control), and could be very useful to both the in vitro [13] and in vivo communities [14].

Previously, computer workstations have been used to achieve high speed simulation of moderately complex neural networks. This is particularly the case when Graphics Processing Units (GPU’s) are used for their parallel processing capability: Fidjeland used a GPU kernel to simulate 55 000 neurons with 1000 connections per neuron under bio-plausible conditions [15]; Wang implemented a network with 1 million HH based neurons on a commodity GPU, achieving a 28× speed-up over CPU implementations [16], and Tadashi applied a cerebellum gain and timing control algorithm on a GPU for real-time processing. However, with this technique it is difficult to achieve accurately timed output states for stimulation in real time using computational systems with operating systems. Therefore further digital logic is required to provide buffering and timing accuracy in the stimulus. This work is motivated by the benefit for timing accuracy in putting the neural network processing in this digital logic layer, and using the computer for updating variables associated with the neurons and network.
One of the most appealing solutions for creating such a digital implementation is via reconfigurable logic, and in particular with a Field Programmable Gated Array (FPGA). FPGA’s consist of arrays of logic and memory elements which can be defined as particular digital elements and connected in highly parallelized forms. These allow for rapid bespoke prototyping of digital circuits and their relative connectivity. As they are reprogrammable, they can be re-tuned to whatever neural network configuration is required. The downside of FPGA’s is that classically their relatively high power consumption means that their application is limited to the benchtop. This is still acceptable for in vitro applications however, and more recently non-volatile forms of FPGA’s provide low power operation suitable for battery-based applications.

FPGA systems have already been used to implement the Hodgkin–Huxley (HH) model, albeit with only voltage-dependent ion channels: Smaragdos implemented an olivocerebellar 92-neuron network using a three-compartment HH model [17]; Weinstein et al. developed a system level design flow for implementing voltage-dependent ion channels [18]; and Graas et al. presented a timing multiplexing technique to process multi-neuron activities sequentially [19].

In this work, we have developed an FPGA-based highly biologically plausible processor for real-time simulation of optogenetic neural networks. Fig. 1 depicts the opto-neural architecture.

The first key advancement of this work lies in how we implement a biologically realistic neuron model with our four-state ChR2 model [7]. In addition, we have incorporated calcium and calcium-dependent ion channel models from both Traub et al. [20] and Soto-Treviño et al. [21] Calcium is an important ion for neuronal adaptation (and also imaging).

Our model can be adapted to represent most forms of optogenetic channels (opsins) by modifying the time-constants, reversal potential and conductance to capture the dynamics of other variants. Therefore, compared to the other FPGA-based neural systems, the short- and long-term calcium- and light-dependent ion channels, allow the hardware to replicate more advanced neural characteristics (e.g., light-to-spike processes and calcium-related adaptation) in real-time.

The second key aspect of this system is its flexibility and computational efficiency. The data management system and configuration unit are separate to the computing data-path. Thus, the system application objectives can be easily updated by modifying corresponding model parameters (e.g., light irradiance, architecture, neural parameters and network sizes). For example, since each neuron’s stimulation level is calculated sequentially, from pre-stored tables of different light levels in the data generation system, the hardware is able to simulate the effects of spatially varying illumination levels over a population of neurons. This is especially useful for investigating multi-site light stimulation strategies for optogenetics, such as for shaping the illumination levels from arrays of LEDs.

Furthermore, our pipelined parallel processing requires only 0.03 ms for a single neuron and 9.7 ms for a fully connected 500-neuron network to calculate a simulation sub-frame. Thus the applicability of this system for either open or closed loop interaction with tissue is where the neuron count is in the hundreds of thousands rather than millions. Examples of this include active pixel sensor neural recording systems [22] and stimulation systems (e.g., Wang et al. [23] and ourselves [24]).

It is also possible to directly translate the FPGA design into an Application Specific Integrated Circuit (ASIC) chip. In this instance, the chip would be sufficiently small and low power for in vivo applications.

II. MODELLING THE LIGHT-TO-SPIKE PROCESS

The optogenetic-neuron mathematical model has been adapted from previous work [7]. It combines a detailed Hodgkin–Huxley neuron model with parameters for a CA3 neuron [20], and integrates an additional ChR2 channel [7]. The structure is shown in Fig. 1, which consists of four compartments: the synapses, axon, dendrites and soma. In order to ensure hardware translation, we do not attempt to increase the number of compartments to reflect long neuronal arbors. Nevertheless, it is still significantly more accurate than for abstract point-neuron models.

A. Cell Model: Soma and Dendrites

Our cell model is essentially a two-compartment neuron model: one compartment emulates the complete dendritic tree including synaptic inputs and the other compartment models the cell soma. Nominal there is a third compartment—the axon—but in our model it is treated as a simple communication contact, hence a separate compartment was not associated with it. The common ion channels for both the soma and dendrites are:

• The voltage-dependent ion channel: a sodium ion channel [Na\(^+\)], a calcium ion channel [Ca\(^{2+}\)], a delayed rectifier potassium ion channel [K\(^+\)(Dr)], and an A-type of transient potassium ion channel [K\(^+\)(A)].
The calcium-dependent ion channel: a long duration Calcium-dependent potassium ion channel [K+(AHP)], and a short duration Calcium-dependent potassium ion channel [K+(C)].

The light-dependent ion channel: [ChR2].

The light-dependent ion channels (ChR2) are assumed to be expressed only in the soma. We justify this as the surface area of the dendrites of any given cell is relatively small compared to the volume of tissue they inhabit, so optical stimulation is best targeted at the soma. We feel the computational cost is not justified by the small dendritic contribution of traditional ChR2, which has very low channel conductance. However, if a high conductance opsin were to be used, these effects could be incorporated.

Synapses are assumed to be only in the dendrites. Similarly, this is to simplify the model computationally, but again, this can be easily changed if required.

The neuronal model is based upon the traditional HH differential equations [12] which treat individual channels as having an individual conductance with a specific reversal potential. The traditional model contains potassium, sodium and leakage ion channel components. We have also incorporated calcium channels.

Equations (1) and (2) describe the time evolution of the membrane potential for the soma compartment and rhodopsin channels.

The current terms are described in Table I. The last term in Equations (1) and (2) describes the current between the compartments.

The mathematical equations for the current flow through the voltage-dependent ion channels [20] are given by

$$ I_L = g_L (V - E_L) $$

$$ \frac{dm(h)}{dt} = m(h)_\infty \times (1 - m(h)) - m(h)_r \times m(h). $$

where $I_L$ is the ion channel current, $g_L$ is the ion conductance, $m$ and $h$ are gate variables (where $h$ has the same form as $m$) and $m(h)_\infty$ and $m(h)_r$ are the gate-variable steady-state and time constant values respectively. Finally, $\nu$ is the reduced membrane potential ($\nu = V - V_{\text{rest}}$) and $E_L$ is the reduced reversal potential.

An empirical equation for intracellular calcium concentration [Ca$^{2+}$] was proposed by Traub et al. [20] and shown here in

$$ \frac{d[Ca^{2+}]}{dt} = -FI_{Ca} - [Ca^{2+}] / \tau_{Ca}. $$

Here, $F = 3$ is the scaling constant, and $\tau_{Ca} = 13.33$ ms is the time constant for the decay of intracellular calcium concentration, due to the rapid action of ion pumps which extrude calcium. The corresponding parameters are shown in Tables I and II.
The four-state model of Channelrhodopsin-2 was previously described by Nikolic et al. [7], which we believe to be optimal in terms of the balance between accuracy and simplicity. The model describes ChR2 as having four states; two closed states and two open (conducting) states, and is shown in Fig. 1(b).

The retinal molecular core of the ChR2 rhodopsin complex absorbs a photon to switch from all-trans to 13-cis-retinal. This induces the channel to switch from a dark-adapted OFF state [C1] to a dark-adapted ON state [O1]. If illuminated in this ON state there is a chance of further photon absorption. This would transition the ChR2 from a dark-adapted ON state [O1] to a less conductive, light-adapted ON state [O2]. From there it may thermally transition back to [O1] or decay to the light adapted OFF state [C2]. The [C2] state slowly reverts to the [C1] state (on the order of seconds) by thermal means.

These relations can be described as four coupled differential equations

\[
\frac{dC1}{dt} = G_{rd}C2 + G_{d1}O1 - G_{a1}(t)C1
\]

\[
\frac{dO1}{dt} = G_{a1}(t)C1 - (G_{d1} + e_{ct})O1 + e_{tc}O2
\]

\[
\frac{dO2}{dt} = G_{a2}(t)C2 - (G_{d2} + e_{tc})O2 + e_{ct}O1
\]

\[
\frac{dC2}{dt} = G_{d2}O2 - (G_{a2}(t) + G_{rd})C2
\]

where \(O1, O2, C1, \) and \(C2\) are the proportions of ChR2 complexes in the open states \((1 \) and \(2)\), and closed states \((1 \) and \(2)\), which are conserved to sum to one. \(G_{d1}\) and \(G_{d2}\) are the deactivation rates \(O1\rightarrow C1\) and \(O2\rightarrow C2\) respectively, and \(e_{tc}\) and \(e_{ct}\) are the rates of transition between \(O1\) and \(O2\) and vice versa and \(G_{rd}\) is the rate of thermal conversion of \(C2\) to \(C1\). \(G_{a1}\) and \(G_{a2}\) are the activation rates for \(C1\) to \(O1\) and \(C2\) to \(O2\) respectively [described in general terms in (10)]. \( \gamma = 0.05\) is the conductance ratio of \(O1\) and \(O2\). Light, \(F\) is flux in photons per ChR2 per millisecond and \(e\) is the quantum efficiency of the rhodopsin. \(V\) is the membrane potential of a neuron (in mV), \(v0\) and \(v1\) are empirical constants equal to 40 mV and 15 mV and \(E_{ChR2}\) is the channel reversal potential, equal to 0 mV. The ChR2 channel’s maximum conductance per unit area, \(g_{ChR2} = 2.5 \) pS/\(\mu\)m\(^2\) is multiplied by the ChR2 expression area \(A_{ChR2}\) to find the total channel conductance for the cell. The corresponding rate parameters are given by Table III.

### B. Synapses

The synapse model is described in

\[
I_{syn} = \sum_{j=1}^{n} \delta_{ij}(t - t'_{ij}) \times g_{i} \times \epsilon \times (v_{i} - E_{s})
\]

where \(I_{syn}\) indicates the total synaptic currents received by the neuron \(i\), \(n\) is the number of presynaptic neurons, indexed by \(j\), with their train of spike times represented by \(t'_{ij}\), \(g_{i}\) is the maximum synaptic conductance of each postsynaptic neuron, and \(\epsilon\) is the transmission efficiency. Spike events are represented by \(\delta_{ij}\), a Dirac-delta function, which is 1 at the time of a presynaptic spike (i.e., when \(t - t'_{ij} = 0\)) or 0 otherwise.

Our intention here is to explore the network dynamics rather than learning processes, however they could be included later using synaptic potentiation/depression models from [25].

### C. Axons

Cable theory such as described by Wilfrid [26] can be used to simulate axonal transmission. Its incorporation would allow for more detailed timing studies between synaptic connections, e.g., spike correlated timing. However, the partial derivative calculations would increase the required FPGA resources. In this instance we believe that the cost outweighs the benefits.

As with other neural network systems, we assume that the transmission channel efficiency is 100\%, i.e., no spike loss between soma and synapse. The transmission delay is one clock cycle which occurs at the end of each computing frame.

If transmission delays are important to study, e.g., for rank [27] or phase coding [28], then they are best introduced as direct network delays. Our system can be reconfigured to interpret this behaviour, but at the cost of additional memory blocks, which would reduce the maximum implementable network size.

### III. NEURAL PROCESSOR ARCHITECTURE

The neural processor mainly contains three components: the computing data-path, the data generation/reconfiguration units, and the router, which are shown in Fig. 2. The computing data-path is specifically designed for calculating the previously described mathematical equations (for details see Section II-A), the data generation system aims to deliver all the required neuronal fixed model parameters to the different data-paths at the corresponding time, the reconfiguration unit is to modify the computing data-path based on the models, and the router is for implementing the network’s synaptic connections.

The FPGA design utilizes 40-bit fixed-point precision, with 22 fractional bits. Therefore, the parameter’s dynamic range

| Parameter | Value |
|-----------|-------|
| \(\tau_{ChR1}\) | 1.3 ms |
| \(\tau_{ChR2}\) | 0.3 ms |
| \(G_{rd}\) | 3.3e-4 ms\(^{-1}\) |
| \(e_{ct}\) | 0.053 ms\(^{-1}\) |
| \(g_{ChR2}\) | 0.023 ms\(^{-1}\) |
| \(G_{d1}\) | 0.13 ms\(^{-1}\) |
| \(G_{d2}\) | 0.0025 ms\(^{-1}\) |
| \(A_{ChR2}\) | 5000 \(\mu\)m\(^2\) |
| \(v_{0}\) | 43 mV |
| \(v_{1}\) | 70 mV |
| \(g_{ChR2}\) | 0.0025 nS/\(\mu\)m\(^2\) |
| \(E_{ChR2}\) | 70 mV |
Fig. 2. A conceptual architecture of an FPGA based neural processor. It consists of three main parts: data generation system, reconfiguration unit, computing data-path and routing system.

Fig. 3. The computing data-path component. It contains three different algorithm logic units (ALUs), one ALU controller and memory data registers.

Fig. 4. The timing diagram of the developed neural processor. The algorithm logic units ALU1, ALU2 and ALU3 require 14, 3 and 3 clock cycles in each frame. The processes are integrated at the last clock cycle in each frame.

In this design, ALU1 calculates the voltage- and calcium-dependent ion channel activity in 14 clock cycles. When $I_{Ca}$ results are released at time-point $t_1$, ALU2 receives the values to calculate the calcium concentration, and the outputs at time-point $t_2$ are feedback to ALU1 for computing calcium-dependent ion channels. In parallel, ALU3 calculates the ChR2 current based on the current membrane potential and light stimulation. At the 15th clock cycle at time-point $t_3$, the integrator sums the outputs from ALU1 and ALU3 for the final output and the system performs the next frame calculation.

The ALU1 hardware architecture is shown at Fig. 5, which implements (3) and (4). During the process, the neural parameters (e.g., G, V) are released sequentially for calculation. A complete frame comprises of 14 clock cycles. There are also 3 switch control signals for the gate variable exponential (Sel1) and calcium calculation styles (Sel2 and Sel3). In the system the forward and backward slices are for calculating the activation and inactivation rate equations as shown in Table I. As described in Fig. 6, five different gate variable calculation styles can be selected in a system depending on the select signals. Particularly, styles d0, d1 and d3 share the common data-paths. Overall ALU1 has 4 configurations and 10 data stream signals. Specifically, when $I_{Ca}$ is calculated from the ALU1, the Sel signal in Fig. 3 will activate and send it to ALU2 for calcium computing. At the same time, the Sel signal will send ALU2 into an inactive state.

The data-path of ALU3 is shown at Fig. 7. The values $G_{a1}$ and $G_{a2}$ are pre-calculated and depend on the light irradiance. The three coupled differential equations (7)–(9) are implemented to simulate the ChR2 four-state model’s dynamic behaviour. The overall latency is optimized to 3 clock cycles, and the time-step for numerical integration is set to 50 $\mu$s. For each loop, the previous state values $O_1', O_2'$ and $C_2'$ are used with the current light stimulation levels to generate the ChR2 outputs. More importantly, ALU3 is only active for 1 clock cycle in a frame (14 clock cycles) due to the parallel implementation and computing pipeline.

B. Data Generation System

The data generation system is shown in Fig. 8. As can be seen, it contains $n$ individual units and a Finite State Machine (FSM). Each unit has one RAM cell and two program counters.
(PCs). The RAM is used for storing model parameters such as activation (inactivation) rate parameters (e.g., $a, b, \ldots, e$) and ion channel conductance. PC1 is an index of the different parameters of a neuron, and PC2 is an index of different neurons in a network. An FSM is employed as a control signal to select corresponding RAM states as output values. Specifically, the FSM decides frame and sub-frame control signals. In addition, memory address registers (MAR) are implemented based on the latency in the computing data-path. Since the system uses different sub-block RAM rather than an entire one, data management becomes more efficient and controllable. In a similar manner, the reconfiguration unit shares this technique with the data generation system.
Fig. 9. Routing system. It contains a ROM based Look-up Table for storing network connectivity, RAM for updating synaptic events, and two registers for data management. In the synaptic connection LUT, location \((1 \rightarrow 2), (1 \rightarrow 3)\) stores the maximum synaptic conductance of neuron index 1 to 2 and 1 to 3, and the RAM_networking LUT records the synaptic current values at time \(t\) for neuron index 1 to index 2 and index 3.

Using this approach we note that the simulator can handle biologically realistic situations which originate from uneven light distribution and/or ChR2 expression: different light intensities for different neurons can be stored in these units as well. The PCs at the address index are responsible for sending light-dependent variables at the correct times for modelling the spatial distribution of light, while the other PCs in the reconfiguration units turn on/off the ChR2 channels to implement different levels of opsin expression.

C. Routing System

The routing system is shown in Fig. 9. Spike events from three processors are sequentially sent into shift registers for processing, and the results are fed-back individually. The basic mechanism is as follows: when a neuron spike event (1 or 0) arrives, its corresponding post-synaptic neuron location (e.g., \(1 \rightarrow 1, 1 \rightarrow 2, \ldots, 1 \rightarrow n\)) will be addressed by the neuron index. By multiplying the synaptic strength pre-stored in the LUT and the spike event, the updated synaptic inputs are stored in the RAM block at the same location (e.g., \(1 \rightarrow 1_t, 1 \rightarrow 2_t, \ldots, 1 \rightarrow n_t\)). After calculating the states for all the neurons in the network, the accumulator adds all the received synaptic inputs per neuron for the next frame calculation (the process happens at the last sub-frame periods). For example, for neuron index 1, all the synaptic currents \((1 \rightarrow 1_t, 2 \rightarrow 1_t, \ldots, n \rightarrow 1_t)\) will be accumulated and represented by \((1)\). Two memory data registers are implemented for storing the accumulator results. One is for sending the previous frame’s synaptic inputs (e.g., \((1)\)) to the calculated neuron, the other one is for storing the currently summed synaptic inputs (e.g., \((1)\)) for computing in the next frame. The frame period is the product of the total number of neurons with the processing time per neuron.

Fig. 10. The hardware simulation results of ChR2. The results from the software model developed previously by Nikolic et al. [7] are shown in black together with the FPGA simulation results shown in red. The short light pulses are 1, 2, 3, 5, 8, 10 and 20 ms. The software fitting parameters used are \(\tau_{\text{ChR}} = 1.3\) ms, \(\gamma = 0.1\), \(e_{\text{ct}} = 0.01\), \(e_{\text{et}} = 0.02\), \(G_{d1} = 0.35\) ms\(^{-1}\), \(G_{d2} = 0.02\) ms\(^{-1}\), \(I_{\text{max}} = 0.2\) nA.

IV. Results

A. ChR2 Ion Channel

The individual silicon ChR2 channel simulation results are shown in Fig. 10. Light pulses of seven durations are used in this experiment: 1, 2, 3, 5, 8, 10 and 20 ms.

The FPGA simulations indicate that the developed silicon ChR2-HH neuron model behaves similarly to its biological counterpart, on which the software model is based (data not shown but can be seen in [7]). However, there are some slight differences between the model and the FPGA implementation, especially at 2 and 3 ms light pulses, which are due to the digital truncation errors and fixed-step integration.
B. Hippocampal CA3 Neurons

Voltage-dependent and [ChR2-expressing + voltage-dependent] hippocampal CA3 neurons have been simulated for comparison. Fig. 11(a) and (b), show oscilloscope readings of our neuron in response to constant and pulsed electrical stimulation (duty cycle = 50% with injected current 0.1 nA): the red line is the membrane potential and the blue line represents the electrical pulses. Fig. 11(c) and (d), show oscilloscope readings of our neuron’s response to constant and pulsed light stimulation (duty cycle = 50% with light irradiance 0.4 mW/mm²): the purple line is the membrane potential (showing action potentials) and the green line is the ChR2 current.

A comparison between software (simulated with Matlab) and hardware firing rates is shown in Fig. 12. For an electrical stimulus, as the stimulus strength increases, the firing rate increases accordingly. When the injected current exceeds 0.6 nA, the CA3 neuron approaches its saturation and the firing rate collapses. For the light-based stimulus, the firing rate increases with light intensity (from 0.01 to 10 mW/mm²) and duty cycle (from 10% to 80%). In both conditions software and hardware systems show identical and biologically realistic results.

In the simulations we used a relatively low light irradiance level (as an effective threshold) of 0.4 mW/mm². This value was experimentally found to be adequate to evoke opto-neuro activity for reasonably long pulses (≥50 ms), whereas the value of 1 mW/mm² tends to be used for short pulses (<5 ms).
In other experiments, even lower light intensities have been found to evoke a response (e.g., Mattis et al. [29] used 0.1 mW/mm²) so 0.4 mW/mm² was a compromise. This represents the power density reaching the neuron for in vitro experiments or simulations. However, in more complex experimental setups, i.e., in vivo studies, the light will be absorbed and scattered by other (non-transfected) brain tissue, reducing the effective power density at the target neurons. In that case, approximate calculations of the true power density just require a multiplicative correction factor, which would need to be determined by experimental measurements. Several studies have modelled these attenuating effects and produced software to simulate and calculate them [40], [41], and there is even an iPhone app called Optogenetics Pro for the purpose [42].

C. Optogenetically Transfected Neural Network

We simulated a 25-neuron opto-neural network. Each neuron receives different light stimulation as shown in Fig. 13(a). Each neuron randomly connects to 16–17 neurons on average with maximum synaptic conductance of 0.01 nS/μm². The unconnected neural responses (i.e., no network connectivity) are shown in Fig. 13(b). As expected, this is similar in response to that with the original irradiance patterns: only five neurons with light-stimulation above threshold (0.4 mW/mm²) had significantly elevated firing rates, while the others remained silent.

The network dominating condition is shown in Fig. 13(c). In this case, the synapses are all excitatory, i.e., no negative feedback. It can be seen that the average firing rate is 45 Hz and the light pattern can no longer be seen in the spatial distribution of neural responses. In this scenario, the irradiance pattern has an effect, but on the overall firing rate rather than a spatial pattern of activity, which is dominated by the synaptic connections.

Fig. 14 shows an interesting example of activity in Neuron (1, 1) where the two scenarios above are moderated such that the firing behaviour is determined by both surrounding network activity and the pattern of optical stimulation. That is, the optical stimulus on its own would not produce such significant neural activity.

V. DISCUSSION

A. System Scalability

We implemented different numbers of neuron on the FPGA processor to test the system’s scalability by measuring the wall-time required for the system to generate a single spike (sub-frame). As shown in Fig. 15, the processor wall-time increases linearly with the number of neurons (blue line). This is because the calculations are sequential. In contrast, the router processing time depends exponentially on the number of neurons due to the memory based approach (where all the connections are pre-stored in the LUTs). At cross point B, the routing computing
period exceeds that of the neural processing. At cross point C, the maximum number of neurons which can be implemented on the processor for real-time computing can be seen to be 500, for which the simulation time is 9.7 ms (assuming the fastest biologically-realistic firing frequency is 100 Hz).

Specifically, with fewer than 45 neurons, the network simulation time equals the processor time. This is because the processor and router compute in parallel in the hardware, and the routing period of a frame is less than a processor sub-frame period. However, with more than 45 neurons, indicated at cross point A, the system transitions from scaling linearly to non-linearly with the network size (neuron number). This is because the router requires more time for routing tasks compared to the processor’s sub-frame periods at this stage, meaning that the processor has to wait until the router finishes its current frame tasks. Therefore, the system simulation performance will mainly depend on the router itself. Overall, the system performance exhibits a linear relationship to network size when it is below 45 neurons, and displays a non-linear relationship for more than 45 neurons (shown by the black line).

### B. Comparison With Other Work

Comparisons between this work and previous FPGA neuron implementations are shown in Table IV. HH* indicates that a HH based model with three compartments, and HH+ represents our optogenetic-calcium enhanced model. Compared to the previous work, the major novelty of the presented work is that we include long- and short-term calcium- and light-dependent ion channels in the system. This enables our implementation to produce more biologically realistic behaviours when compared to other abstract models.

The neuron model itself exerts a major influence on the hardware architecture design. General models with strong biophysical meaning have smaller time steps than mathematically abstract models: Izhikevich [30] and LIF [31] models have 1 ms time step while HH [21], [22] based models have time- steps ranging from 0.001 to 0.05 ms. This is because complex neural models require higher integration step resolution to compute the detailed ionic dynamics. As a result, the number of hardware operations for 1 ms of biological time in bio-physical models is significantly larger than for the high-level phenomenological neuron models: LIF and Izhikevich hardware implementations take only 30 and 13 operations to simulate 1 ms of biological time, whereas the HH model with 3 compartments and our model require 22,200 and 11,880 operations respectively for the same period.

Another vital issue concerns the implementation of neural communication on the hardware. There are two major approaches for this: memory-based and routing-based. The memory-based approach uses on/off chip memory for pre-storing network connections. For each computing loop iteration, the neuron spike events will be sent to their postsynaptic-neuron targets according to their address packages (e.g., neuron and synaptic indices). Similarly to Cheung et al. [30], our design also follows this principle. It enjoys low latency and simple hardware design, but memory resource/bandwidth limits will be reached when the neuron number exceeds a certain threshold (dependent upon the resources of a particular FPGA). The other approach is to use a network-on-chip architecture; a tailor-made routing strategy implemented to deliver multi-core spike events in a system such as the SpiNNaker platform [32]. Our previous work [33], [34] employed this approach to implement cerebellum model [30] connections.
It shows excellent system scalability but has more complex hardware design to ensure low latency.

In addition, Randall et al. [18], Andrew et al. [31] and Smaragdos et al. [17] implemented an all-to-all connection through their custom-designed techniques.

In prior work, different designs have used different methods to assess their relative computing performances. It is therefore hard to directly compare system speed and efficiency: Graas et al. [19] proposed increasing the FPGA clock frequency and the step size for a speed up of $40 \times$ real-time; Cheung et al. [30] designed an event-driven and fully pipelined architecture for $2.48 \times$ real-time; Smaragdos et al. [17] optimized their HLS C-code for $12.5 \times$ real-time. Fully pipelining and shortening the critical path are employed in our system speed optimizations.

There are also several different hardware platforms such as Spinnaker [32], Neurogrid [36], IFAT [37], and GPU [16] for neural modelling. Each system has strengths and weaknesses in particular areas. For example, Neurogrid and IFAT are mixed-signal based architectures that are less reconfigurable but enjoy elegant design and efficient power consumption.

C. Applications

The developed hardware can serve as a multi-functional platform to investigate optogenetic related topics. Some of these potential applications are summarized in Table V.

| Applications                              | Hardware requirements                                      |
|-------------------------------------------|------------------------------------------------------------|
| Optogenetic actuators investigation       | Updating the parameters and configuration signals for ChR2 computational blocks |
| Verification of optical-neural interfaces | Updating all parameters in the data generation system and configuration signals in the control blocks |
| Multi-site light stimulation strategies investigation | Updating all parameters in spatially varying light stimulation profiles |

D. Future Work

One of the main areas for further development will be in developing new techniques for system optimization. For example, the natural communication in biological systems tends to be asynchronous and event driven. Therefore, an asynchronous communication protocol [43] coupled with an event driven approach [44] may potentially make the system more power efficient. Furthermore, sharing the common computing-path [45] (e.g., ALU1) and optimization of the neural network modularity [46], [47] will result in utilizing less hardware resources. Finally, multi-core architectures [48] represent a promising way to scale the number of implemented neurons towards brain-scale sizes with real-time computation.

VI. Conclusion

In this work we have designed and implemented an FPGA-based neural processor for real-time simulation of opto-neural behaviour. The developed neural processor can successfully reproduce the photo-kinetics of mammalian neurons expressing optically active ion channels [7] in a biologically realistic neural network model. It only requires 0.03 ms for a single neuron and 9.7 ms for a fully connected 500-neuron network to generate a spike. Therefore the system, with its real-time computing performance and highly biologically-realistic behaviour, can be applied in many ways as a powerful tool for multidisciplinary researchers in the field of optogenetics.

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