Design of a Time Discriminator in a Low-background, Anti-Compton Spectrometer

Xin-Chi Li, Guo-qiang Zeng, Lei Yan, Bin Bai, Li He*, Liang-Quan Ge, Chuan-Hao Hu, Yang Hou

Key Laboratory of Applied Nuclear Techniques in Geosciences of Sichuan Province, Chengdu University of Technology, Chengdu, Sichuan, 610059, China

*Corresponding author’s e-mail:1955783586@qq.com

Abstract. Compton scattering leads to the incomplete deposition of particle energy and produces a Compton scattering background, which decreases the measurement accuracy of low-energy rays. The low-background, anti-Compton spectrometer outputs 7-channel time signals through coincidence detector. The Compton events can be identified and reduced by the inverse coincidence of these time signals with the energy signals coming from the High Purity Germanium (HPGe) Detector. The precise-time measurement circuit can pulse shape the signal from the coincidence detector and accurately draw the arrival time of the signal. This is the key for a low-background, Compton-suppressed spectrometer to realize accurate anticoincidence measurements. In this study, a constant fraction discriminator (CFD) circuit was designed to replace the traditional leading-edge timer. A constant fraction discriminator-based all-pass filter without a delay line was used as the delay module. The advantages of the proposed method include the integration of circuits, low power consumption, and low cost. The simulation nuclear signals with different amplitudes, which were measured using the proposed CFD design, were outputted using the signal generator. The maximum deviation of the circuit triggering ratio was 2.5% and time jitter was 1.6 ns. The anti-Compton spectrometer with constant fraction discriminator has good Compton suppression effect. The peak-to-Compton ratio of the Compton-suppressed spectra is 1333:1 and the Compton-suppressed coefficient is 6.3.

1. Introduction

Interference from irrelevant counting must be reduced maximally in radiation measurements, especially in the conduct of low-level radiation measurements. The objectively existing Compton scattering and environmental background must be weakened during measurements. The low-background Compton-suppressed spectrometer identifies Compton events through anticoincidence, thereby decreasing the lower limit of detection (LLOD).

Designing a precise-time measurement circuit is the key for a low-background Compton-suppressed spectrometer to realize anticoincidence measurement. Such a design filters and shapes the output signals of the coincidence detector and outputs the arrival time of the signal. A well designed precise-time measurement circuit is not only significant in nuclear physics experiments, but can also be widely applied in many fields. These include the measurement of positive and negative electron annihilation lifetimes, anti-background Compton-suppressed measurement [1], duration test of an atomic nucleus in different excited states, electron annihilation and production of photon pairs in a
PET system, neutron-capture cross section measurement [2], laser ranging [3], neutron energy measurement [4] and pulse-shape discrimination [5].

This study emphasizes the design of a precise-time measurement circuit in the Compton-suppressed spectrometer, analyzes its working principles in detail, and discusses the further improvement and enlargement of the circuits. A two-stage all-pass filter was chosen as an analog delay circuit that can meet the ns-level delay of signals. Unlike the traditional delay line and digital plug-ins, the designed constant fraction discriminator (CFD) has a simpler structure and higher delay accuracy.

2. Low-background Compton-suppressed spectrometer system

Compton scattering induces γ-photon escape, an incomplete deposition of particle energy, and a relatively low full-energy peak; it also increases the Compton plateau counts, thereby making low-energy γ-ray difficult to detect. A low-background, Compton-suppressed spectrometer has a relatively low LLOD of energy, and this system is consists of the main, annular, and plug detectors. The annular and plug detectors constitute the coincidence detector. γ photons escape from the main detector and are recorded in the coincidence detector, and the coincident γ photon pairs are categorized according to time of arrival [6]. Each effective γ photon pair represents a Compton event. The 7-channel time information outputted by the coincidence detector is in anticoincidence with the energy signals outputted by the main detector, and such a circumstance can distinguish and shield the Compton scattering event and calibrate the environmental background.

Existing Compton-suppressed spectrometers block the output signals of the annular detector by using the output signals of the main detector. Similarly, these spectrometers also block the output signals of the main and annular detectors by using the output signals of the auxiliary detector. Although such spectrometers can realize anticoincidence in time, they cannot discriminate false coincidences from true ones when the background count is high. Hence, digital anticoincidence shall be set independently for statistical discrimination of coincidence information and extracting the characteristic information of nuclides effectively. Figure 1 shows the overall design framework.

Fig.1 Overall design framework of the low-background Compton-suppressed spectrometer

A detector array is composed of the NaI (Tl), HPGe, and PMT. A coincidence detector uses NaI (Tl) as a measurement crystal. Although NaI (Tl) has low energy resolutions, it has stable performances and relatively high detection efficiency and optical output. After the 7-channel time signals are outputted by the precise-time measurement circuit, the main detector uses HPGe with higher energy resolution to output single-channel energy signals after signal conditioning.

A complete time information acquisition circuit consists of a detector, amplifier, discriminator circuit, and time-to-digital converter. The detector outputs signals are then amplified and shaped. Timing logic pulses, which have known relations with time, are detected by the time discriminator. Finally, the digital time information is outputted by the time-to-digital converter, and then inversely matched with the energy information in the digital multichannel analyzer.

An ideal time discriminator can trigger signals that occur simultaneously. In fact, signals that appear at the same time are often recorded at different times for many reasons, such as the inherent jitter of the detector, noise superposition, and the time walking effect caused by amplitude and rise time fluctuation.
The time measurement circuit in the Compton-suppressed spectrometer is used to acquire the 7-channel time signals produced by the annular and plug detectors. These 7-channel time signals are outputted by the NaI detector. The rise time and signal amplitude of the NaI detector are approximately 230 ns and 600 mV, respectively. Compared with the output signals of the HPGe detector, the NaI detector output 7-channel time signals have a stable rise time variation trend; the accuracy of the timing measurement is more vulnerable to the fluctuation of the signal amplitude.

Three timing methods are used for reference, namely, leading edge timing, zero-crossing timing, and constant fraction timing. The first two cannot compensate for time walking brought by amplitude changes, whereas the last one achieves dual compensation for the time walking caused by the variations in amplitude and rise time. Constant fraction timing is a relatively precise timing method.

Existing constant fraction discriminators generally have similar structures but different delay modules and chip performances. The delay module is developing toward small sizes, low cost, and low power consumption from the delay line to the digital plug-ins and analog delay circuit. A digital filtering delay module [7] can realize ps-level precise delay and has a large delay range; however, it has the disadvantages of high-power consumption and difficult circuit integration. The analog delay circuit is characterized by a simple circuit structure, low cost, small size, and ease of integration. Analog delay performance is improving continuously with the development of electronic integrated chips.

To further increase timing accuracy, a constant fraction discriminator was chosen for the precise-time measurement circuit. A filtering shaping circuit was added in the front end, while the rear-end logic output applied the traditional TTL to connect digital multichannel analyzer, aiming to increase the signal to noise ratio (SNR); no additional circuit (such as logic conversion circuit) was required.

3. Theoretical principles

Primary nuclear signals are characterized by quick ascents and slow descents. The amplitude of a primary nuclear signal is believed to remain constant in a period after the peak, expressed as a straight line parallel to the horizontal axis. The slope of the rising edge is approximately a constant, that is, a linear straight line with constant slope (Fig. 2).

Two triggering situations in the first-half and second-half edges of the attenuation signals were analysed. The former is called the amplitude and rising time compensation (ARC) timing because it compensates for the effect of amplitude and rising time fluctuation, and the latter is called constant fraction discrimination (CFD) timing because of its constant fraction discrimination. The triggering point at the peak of the attenuation signal was used as the critical point. In Fig. 2, $T_d$ is delay time, $T_r$ is the rise time of signals, $P$ is the attenuation coefficient, and $A$ is the amplitude of the primary signals.

![Fig. 2 Principle of constant fraction timing](image)

Similar triangles indicate the following relationships:
\[ \frac{Tr - Td}{PA} = \frac{Tr}{A} \]  
(1)

\[ Td = (1 - P)Tr \]  
(2)

The critical value of the delay time is \((1 - P)\) times of the rise time. When the delay time is higher than or equal to this critical value, the triggering point occurs at CFD; otherwise, it occurs at ARC.

3.1. Constant fraction discrimination

When the delay time is higher than \((1 - P)\) times of rise time, the triggering point is at the second-half edge of the attenuation signals; thus, the delay time belongs to CFD timing. In this case, the triggering point is equivalent to the point of intersection between the straight line parallel to the horizontal axis and the straight line of the constant slope. This point can be solved by a linear equation. The x-axis of the triggering point denotes the triggering moment, and the y-axis denotes the timing threshold (Vt).

\[ \begin{align*}
  y &= \frac{A}{Tr} (x - Td) \\
  y &= PA
\end{align*} \]  
(3)

\[ \begin{align*}
  x &= PTr + Td \\
  y &= PA
\end{align*} \]  
(4)

As the triggering ratio is \(f\), the known signal amplitude is \(A\), and the timing threshold is \(y\). Then,

\[ f = \frac{y}{A} = P. \]  
(5)

Obviously, the timing moment \((x)\) is related to the rise time but is independent from the signal amplitude. In other words, this timing mode can compensate for the timing walking brought about by signal amplitude fluctuation but it cannot compensate for that caused by rise time fluctuation. CFD timing is more applicable to signals with great changes of amplitude but stable changes of rise time. The triggering ratio is constant and equal to the attenuation ratio. The triggering ratio can be controlled by changing the attenuation ratio. When the variation of the signal waveform is not obvious, the signal can be triggered at the maximum slope by adjusting the triggering ratio to an appropriate value, thereby enabling the weakening of the jitter caused by statistical fluctuations.

3.2. Amplitude- and rise time-compensated timing

When the delay time is smaller than \((1 - P)\) times of rise time, the signal is triggered at the first-half edge of the attenuation signals; thus, such delay time belongs to ARC timing. Under this circumstance, the triggering point is approximated as the point of intersection between two straight lines with different slopes. A linear equation is constructed to solve this triggering point. The x-axis of the triggering point denotes the triggering moment, and the y-axis denotes the timing threshold (Vt).

\[ \begin{align*}
  y &= \frac{A}{Tr} (x - Td) \\
  y &= \frac{PA}{Tr} x \\
  x &= \frac{1 - P}{Td} \\
  y &= \frac{P}{1 - P} Td A
\end{align*} \]  
(6)

\[ \begin{align*}
  x &= \frac{1 - P}{Td} \\
  y &= \frac{P}{1 - P} Td A
\end{align*} \]  
(7)

As \(x\) is the triggering moment \(T\), and \(y\) is the timing threshold \(Vt\), if the triggering ratio is \(f\), then the following equation applies:

\[ f = \frac{y}{A} = \frac{P}{1 - P} \frac{Td}{Tr}. \]  
(8)
Clearly, the timing moment is independent of the amplitude and rise time of signals. In other words, dual compensation for signal amplitude walking and rise time walking is realized. ARC timing is more applicable to signals with a large range of rise time (e.g., output signals of the HPGe detector). Moreover, the triggering ratio of the ARC timing is related to the rise time of the input signal.

4. Circuit design
The time pick-up circuit consists of two parts, namely, the front-end filter shaping circuit and the timing discriminator. The former is composed of differential, pole-zero cancellation and the Sallen and Key filter (SK filter) shaping, and the latter comprises the delay, attenuation, low-threshold pre-discrimination and a bias circuit.

The working principle of the design is shown in Fig. 3. After filtering, the signal is inputted to the attenuation circuit and the delay circuit. A bias level is added in the attenuation circuit to stabilize the baseline of the attenuation signal and prevent error-discrimination. The delay and attenuation signals were inputted into the two ends of the high-speed comparator in order to obtain a standard digital signal related to time. A low-threshold discrimination channel was added externally and noise interference was filtered. Two-channel time signals conform to the output.

![Fig. 3 Structure of the time pick-up circuit](image)

4.1. Circuit composition
The front-end shaping circuit included differential, pole-zero cancellation, and SK filtering shaping. The original nuclear signal was processed to a signal with a narrower pulse width and larger SNR, with an aim to increase the follow-up timing accuracy. Signals pass through the one-stage CR differential circuit to decrease the time constant of the input signal. The time constant of the pole-zero cancellation circuit is then adjusted to match that of the pulse signal, and the overshooting brought about by differential is reduced. Accordingly, the pulse signal returns to the baseline monotonously and the problems of pulse amplitude superposition and overloading of the counting rate are improved. The exponential pulse signal is shaped into a quasi-Gaussian waveform by the SK filter, and the signal-to-noise ratio is improved.

The constant fraction timing circuit is composed of an all-pass delay, attenuation circuit, bias circuit, high-speed comparator, low-threshold discriminator, and coincidence circuit. To realize accurate timing, the delay circuit maximally reduces attenuation distortion while realizing equilibrium delay. Previously, the delay line [2] and delay plug-in [8] were commonly used in delay modes. Due to the large size of the delay line, the delay line is inconvenient for packaging and cannot be used in a high-integrated circuit. In comparison, a digital plug-in can realize precise controllable delay and release the stored signal after the preset time to obtain an accurate delay and highly reduced waveform distortion. However, the digital plug-in has a high-power consumption and large size, as well as incompatibility to a low-power integrated circuit. Here, an all-pass filter was used as a precise delay
circuit structure. With its small size and low-power consumption, the all-pass filter can realize large-scaled group delay and decrease delay error of signals. Some people have replaced the original delay line and plug-in by an analog circuit, such as the delay circuit consisting of a first-order low-pass filter [9]. In this study, a two-stage, first-order, all-pass filter was used to replace the traditional delay line and digital delay module, such as the first-order, all-pass filter in Fig. 4.

![First-order all-pass filter diagram](image)

Fig. 4 First-order all-pass filter

Signal passing through the all-pass filter maintains the same amplitude but has different phase positions. This approach is often used to measure phase positions and has been applied in the modulator circuit of a single sideband suppressed carrier (SSB-SC). The delay of the first-order, all-pass filter in Fig. 4 is 2RC. In the design, a two-stage first-order, all-pass filter is applied and its total delay is 4RC. To prevent signal overshooting, this delay circuit requires enough slow ascents of the input signal and a rise time higher than or equal to 5RC.

The attenuation circuit applies the simple resistor divider, and the partial pressure accuracy is determined by the adjustable resistance accuracy. A bias circuit is installed in the attenuation circuit. A simple voltage division circuit and a small-capacitance filter were used to stabilize the signals of the attenuation channel, thereby preventing the spurious triggering of signals brought about by signal instability. First, the whole circuit requires two high-speed voltage comparators. The comparison speed of these two comparators directly influences the quality of the whole timing circuit. Comparators can be triggered well as long as the rotating speed is high enough. These two circuit voltage comparators employ the traditional TTL output, and the transmission delay is 4.5 ns. Compared with the high-speed level output of the ECL [10] and a transmission delay of 0.5 ns, this circuit voltage comparator has the advantage of outputting the standard NIM level signal without requiring additional transformation. Moreover, it has lower power consumption, is conducive to realizing a low-power integrated circuit, and each of its comparators only needs 5 mA current.

A low-threshold discriminator circuit is used to reduce the spurious triggering of noise signals. For the timing signal produced by a constant fraction discriminator, no fixed triggering threshold exists and such a discriminator may produce corresponding timing signals to all input signals, including the timing signal triggered by the low-amplitude noises. In order to prevent the influences of the timing signal produced by the low-amplitude noises on the final output timing signals, a low-threshold discriminator is employed. The fixed triggering threshold can be adjusted through the adjustable resistance. This triggering threshold is determined by the noise signal amplitude and triggering threshold of the actual constant fraction discriminator. That threshold shall be as high as possible as long as it is lower than the threshold of the constant fraction discriminator. A Gate coincidence circuit is utilized for identifying the coincidence of timing signals outputted by the low-threshold discriminator and the constant fraction discriminator. These two-pathway digital signals pass through the gate circuit and output the time of arrival of nuclear pulse signals accurately, thereby obtaining the corresponding timing square wave. Here, a high-speed gate integrated chip with four gates is chosen. The overall design of the timing discriminator is presented in Fig. 5 below.
5. Performance test

5.1. Changes of the triggering ratio caused by the signal amplitude fluctuation

With reference to the output signal of the NaI (Tl) detector, a gamma exponential signal in the signal generator is applied for the test. The rise time is 200 ns. After the signal passes through the front-end filtering shaping circuit, the rising and falling edges are 600 ns and 2 μs, respectively.

The initial signal was first processed by a differential. The time constant is lower and presents an exponential waveform. Signal undershooting brought about by the two-stage differential is reduced by pole-zero cancellation, and the signal becomes narrower. After SK filtering shaping, a quasi-Gaussian signal with higher SNR is gained. For signals after shaping and filtering, the time constant is small and SNR is high. The output signal enters the timing discriminator and is then inputted into two circuits separately. One circuit is the signal attenuation and the other is the signal delay. The resistance in the attenuation circuit is then adjusted. The actual attenuation multiple is 0.78. R and C in the delay circuit are adjusted according to the input signal and the actual circuit delay is 100 ns.

Signals in the attenuation and delay circuits pass through the positive and negative ends of a high-speed comparator, respectively. The logic pulse timing signals approximate to the rectangle are outputted. The rise time of the output signals is 20 ns and is determined by the response speed of the comparator. Variable resistance is adjusted to control the threshold of the low-threshold discriminator so that it is higher than the noise amplitude but lower than the threshold of the timing discriminator. Similarly, a logic pulse timing signal approximating a rectangle is gained. The signal of the low-threshold discriminator and the signal of the constant fraction discriminator pass through the gate coincidence circuit, thereby eliminating the identification of timing signals with low-threshold noises.

Here, the output timing signal is not produced at the actual triggering moment of the original signal. That signal also contains the inherent delay of comparators and the circuit transmission delay. In practical application for particle time discrimination, the delay of the coincidence detector shall be consistent with the delay of the main detector.

The measurement results were analyzed by changing the parameters of the simulation signal. Given the constant rise time and uniform increase of the amplitude of the input signal, measurements began from 24.8 mv. Data were collected every 100 mv and the upper limit was set at 2.09 v. A total of 16 groups of data were collected (average of multiple measurements). Meanwhile, the amplitude of the input signal and the corresponding amplitude ratio of the timing point (triggering ratio) were calculated.
The attenuation of the circuit and the delay time are 0.78 and 100 ns, respectively. The rise time of the signal after sk filtering and shaping is 600 ns. The triggering ratio is calculated according to the theoretically deduced formula:

\[ f = \frac{y}{A} = \frac{P}{1 - P} \frac{T_d}{T_{tr}} = \frac{0.78}{1 - 0.78} \frac{100}{600} \approx 0.59 \]  

(9)

The measurement data are shown in Fig. 6. The triggering ratio of this circuit is stabilized at approximately 0.59, which conforms to the theoretical value. The maximum error is 2.5%. This result suggests that this circuit can adequately realize the constant fraction triggering of signals and compensate for influences caused by amplitude fluctuation.

5.2. Jitter caused by signal amplitude fluctuation

Jitter caused by signal amplitude fluctuation was tested. To ensure measurement accuracy, double-exponential signals that are similar to the coincidence detector output were edited by using the Ultra Wave software. The amplitude of the output signal of the coincidence detector was set at 600 mv and the chosen simulation signals ranged between 75 mv and 1.3 v. Thus, the amplitude of the simulation signal was changed to test time difference between the signal zero-crossing moment and the discriminator timing moment. The fluctuation of this time difference can represent jitter.

By maintaining the rise time at 230 ns, 33 groups of signals with different amplitudes were measured. Each group of signals was measured 10 times. Therefore, a total of 330 groups of signals were measured. The statistical results are shown in Fig. 7.

![Fig. 6 Changes of trigger ratio with fluctuations of signal amplitude](image)

![Fig. 7 Statistical distribution of time difference](image)

Obviously, the time difference distribution conforms to a Gaussian distribution and the maximum probability occurs at 280.8 ns. According to the RMS equation, 330 groups of data are substituted into the following equation:

\[ \Delta X = \sqrt{\frac{\sum_{i=1}^{330} (X_i - 280.8)^2}{330 - 1}} = 1.6 \text{ns} \]  

(10)
The calculated jitter is 1.6 ns, and the results show that the design of CFD compensates for the time walking generated by amplitude fluctuation.

5.3. Actual Compton-suppressed measurement

In the actual measurement of a low-background, Compton-suppressed spectrometer, Cs137 source was applied and the measurement took 73 min. A total of 16,384 channels were involved. A nuclear signal with 230 ns rising edge and approximately 600 mv amplitude was outputted by the 7-channel photomultiplier tube. The arrival times of these signals were outputted by a precise-time measurement circuit. The time difference of the arrival time of particles was then calculated. Fig. 8 illustrates the probability distribution, in which the time difference is expressed by the number of clocks at a frequency of 200 MHz. The actually measured time difference of particles in the Compton-suppressed spectrometer system conforms to the Gaussian distribution, and the maximum probability was set at 120 ns. This outcome is mainly attributed to the statistical fluctuation in the transmission process of particles.

Digital signal processing after anticoincidence measurement and single-pathway energy signal ADC sample was accomplished in FPGA. All processed data were transmitted to the ARM controller through a parallel interface, data exchanges were realized, and spectrum storage was accomplished in the ARM. The original spectra and Compton-suppressed spectra were obtained (Fig.9). Full-energy peaks reached 21,326. The peak-to-Compton ratio of the original spectra is 211:1 and the peak-to-Compton ratio of the Compton-suppressed spectra is 1333:1. The Compton-suppressed coefficient is 6.3.

![Fig. 8 Statistical data on the time difference of particles in anti-Compton coincidence measurement](image)

![Fig. 9 Comparison between original spectra and Compton-suppressed spectra](image)

6. Conclusions

The low-background, Compton-suppressed spectrometer can shield from Compton scattering and environmental background by using anticoincidence based on time information. The said spectrometer has an extremely low LLOD. The constant fraction discriminator is the key factor in realizing time
coincidence measurement. The time information of the signal outputted by the coincidence detector is extracted and can be used to distinguish the Compton scattering event effectively. In this study, the problem of timing-error and constant fraction discriminator principle is analysed. A constant fraction discriminator is designed and two first-order, all-pass filters in cascade connection are used as the delay module of the circuit, an approach which has certain limitations. However, the resulting delay accuracy and signal distortion are satisfactory. Given the uneven amplitudes of the signals, the triggering ratio of this circuit is stabilized at 0.59, with a maximum error of 2.5% and a jitter of 1.6 ns. Moreover, the time difference of particles in the Compton-suppressed spectrometer system is 120 ns. The peak-to-Compton ratio of the Compton-suppressed spectra is 1333:1 and the Compton-suppressed coefficient is 6.3.

Acknowledgments
This work was supported by The National Key Research and Development Program of China (Grant No. 2017YFC0602100) and the National Natural Science Foundation of China (Grant No. 41474159)

References
[1] Feng Jiangping, Chen Yu, Yang Hualong. (2009) The Background Issue in the Measurement of Low-level Gamma-ray. Nuclear Electronics & Detection Technology, 29(03):652-657.
[2] Gao Weixiang, Ma Shulan. Rise time-amplitude Converter of FH4-017 (1981). Atomic Energy Science and Technology, 02:226-230.
[3] Li Xin, Tao Shiguang. Fast Discriminator Shaping Circuit (1986). Electronic Technological Application, 09:32-33.
[4] Deng Yunyue. Improving Laser Pulse Ranging Accuracy by Constant Fraction Timing Circuit and High-resolution Counter (1981). Laser & Infrared, 03 :43-46.
[5] Wei Lingfeng, Zhou Rong, Yang Chaowen. Design and realization of the ICF neutron time-of-flight measurement circuit (2015) . Nuclear Techniques, 38(07):53-58.
[6] Badran, H. M., & Sharshar, T. . (1999). An experimental method for the optimization of anti-compton spectrometer. Nuclear Instruments & Methods in Physics Research, Section A, (Accelerators, Spectrometers, Detectors and Associated Equipment), 435(3): 423-432.
[7] Wu Kai, Su Tao. Design and application of the allpass fractional delay filter (2015). Journal of Xidian University (Natural Science), 42(04):8-13.
[8] Chen Yu, Wang Ruiting, Sun Huibin. High Speed Constant-Fraction Discriminator with ARC Timing (2011). Nuclear Electronics & Detection Technology, 31(12):1350-1353.
[9] Yang Tao, Zhao Bo, Zhang Chi. A Constant Fraction Discriminator without Delay Line (2002) . Nuclear Electronics & Detection Technology, 03:244-246.
[10] Zhang Jun, Peng Chengzhi, Yang Tao. Development of a non-delay-line constant-fraction discriminator (2005) . Nuclear Electronics & Detection Technology, 06:191-194.