Run-to-Run Yield Evaluation of Improved Nb 9-layer Advanced Process using Single Flux Quantum Shift Register Chip with 68,990 Josephson Junctions

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Abstract. We have improved an Nb 9-layer advanced process (ADP2) using a plasma-enhanced chemical vapor deposition (PECVD) SiO$_2$ insulator. We could solve the problems due to the surface profile of the PECVD SiO$_2$ by adding an ion-milling process. The reliability of the ADP2 was evaluated by the operating yield of the SFQ shift registers (SRs). The SRs with six different bit sizes from 16 to 2560 were designed to evaluate the circuit size dependency of their yields. The total number of SRs is 16, and the total number of junctions per chip is 68,990. By introducing the PECVD SiO$_2$ insulator, we could obtain a high operating yield of more than 80% even for large-scale 2560-bit shift registers with more than 10,000 junctions. Moreover, we could obtain nine perfect chips (in which all the SRs in the chip functioned) out of 26 measured chips fabricated using the PECVD SiO$_2$. From these results, we believe that the fabrication yield of the ADP2 is at a level of 100,000 Josephson junction circuits.

1. Introduction
Superconducting digital devices are superior because they have lower power dissipation and higher speed operation compared to those of conventional semiconductor devices. However, the high performance of superconducting digital devices has not been achieved sufficiently since their integration level is still low. Fabrication technology that enables large-scale integration is required to realize the high performance of superconducting digital devices [1, 2].

We have been developing an Nb 9-layer advanced process (ADP2) for large-scale superconducting single flux quantum (SFQ) circuits [3]. In the ADP2, the bias-sputtered SiO$_2$ had been used for an inter-layer insulator, however we replaced the bias-sputtered SiO$_2$ with a plasma-enhanced chemical vapor deposition (PECVD) SiO$_2$, which has the advantages of good step coverage, low film stress, lower temperature process, and fewer particles. However, at first, there was a problem due to the surface profile of the PECVD film when applying it to the actual device structure.

Therefore, to improve the surface profile of the PECVD film, we introduced an ion-milling process. In this paper, we describe the inter-layer insulator forming methods using PECVD SiO$_2$ deposition and ion milling. Then, we describe the yield evaluation of the ADP2 by using shift registers (SRs).
2. Initial problem using PECVD and improved method

We introduced a PECVD system (Samco PD-270STL) in March 2014. The current process conditions of the PECVD SiO$_2$ are as follows: wafer temperature of 80ºC, TEOS/O$_2$ gas pressure of 30Pa, flow rate of 2.5/75 sccm, and RF power of 125W. Although PECVD SiO$_2$ films have the aforementioned advantages, there was an initial problem due to the surface profile. Figure 1 shows the difference of the surface profile between bias-sputtered SiO$_2$ and PECVD SiO$_2$ films. The bias-sputtered SiO$_2$ film has an appropriate angular slope on the step edges of the underlying Nb patterns (figure 1 (a)). On the other hand, the PECVD SiO$_2$ film has a surface profile with sharp step edges and narrow concaves (figure 1 (b)). After the upper Nb layer is formed, etching residues tend to be left in these regions. This was a serious problem since these etching residues led to intra-layer leaks of the upper Nb patterns.

Therefore, we improved the surface profile of the PECVD SiO$_2$ film by adding an ion-milling process after PECVD SiO$_2$ deposition. Figure 2 shows the process flow of the inter-layer insulator forming methods using the PECVD SiO$_2$ deposition and the ion milling. First, 400 nm SiO$_2$ film is deposited by PECVD over the Nb patterns with 400 nm thickness. Then, about half the thickness of the SiO$_2$ film is etched by Ar ion milling. The ion beam is accelerated with a voltage of 400 eV at an Ar pressure of $5 \times 10^{-2}$ Pa. The wafer is mounted on the plate that rotates during the milling operation, and the incident angle of the ion beam is 20 degrees to the rotation axis of the plate. By using this ion milling, we can eliminate sharp edges, and obtain a smooth surface profile. Then, additional PECVD SiO$_2$ is deposited to obtain the desired thickness. We could solve the problem of the intra-layer leaks by using this method.

3. Nb 9-layer advanced process using PECVD SiO$_2$ insulator

Figure 3 shows the device structure of the Nb 9-layer advanced process (ADP2) [3]. Every Nb layer for M1-M7 is planarized by the caldera planarization technology except for the upper 2-Nb layers. We simply replaced bias-sputtered SiO$_2$ with PECVD SiO$_2$ for planarized insulator layers between M1 (DCP) and M8 (BAS) since the above mentioned sharp step edges and narrow concaves of the PECVD SiO$_2$ are eliminated by the planarization before forming the upper Nb layer. However, for the insulator layer between M8 (BAS) and M9 (COU) which is not planarized, we introduced the technology described in section 2 to eliminate the problem of the intra-layer leaks. Moreover, to increase reliability,
we added a 2nd ion milling process to the process flow of figure 2, as shown in Table 1. This procedure, which uses PECVDs and ion millings is also used for our unplanarized standard processes (STP2, HSTP).

**Table 1. Process flow for interlayer insulation between M8 (BAS) and M9 (COU).**

| Step | Process       | Thickness |
|------|---------------|-----------|
| 1    | 1st PECVD     | 400 nm    |
| 2    | 1st Ar Milling| - 200 nm  |
| 3    | 2nd PECVD     | 400 nm    |
| 4    | 2nd Ar Milling| - 200 nm  |

**Figure 3.** Device structure of Nb 9-layer advanced process (ADP2). JJ: Nb/AlOx/Nb junction, M1-M9: Nb layers, M2, M4, M6, M7: Ground planes, RES: Mo resistor (thickness: 45 nm), C1-C6, GC, RC, BC, JC: Contacts between metal layers, SiO2: Interlayer insulator.

**4. Yield evaluations of ADP2 using shift registers**

Process evaluations have been performed for every fabrication by using both the diagnostic chips and shift register (SR) chips [3]. In this paper, we describe the yield evaluation using shift registers.

Figure 4 is a schematic of the shift register cell, and figure 5 is its device structure and layout design. The cell is composed of four junctions, inductors, and resistors. Since this shift register was designed to evaluate the reliability of the fabrication process (ADP2), most components were composed with minimum feature sizes (JJ: 1 μm square, line width: 1 μm, contact: 0.7 μm square) for ADP2. Since the DC bias is fed from the bottom DCP layer to the upper junction layer through the DCVIA, all layers are used. However, since this SR does not need PTL interconnections, dummy patterns composed of PTL1 and PTL2 layers are included in one of the two cells as shown in figure 5 (b).

Figure 6 (a) shows the layout of a shift register chip. SRs with six different bit sizes from 16 to

**Figure 4.** Schematic of shift register cell. J1 = 0.1mA, J2 = 0.12mA, J3 = 0.11mA, J4 = 0.1mA, L1 = 12 pH, L2 = 10 pH, L3 = 20 pH, L4 = 3.9 pH, DC bias = 0.172mA.
2560 were designed to evaluate the circuit size dependency of their yields. The specifications (the number of Josephson junctions, bias current values, and number of circuits) are listed in Table 2. The details of the SR design have been described in other papers [4, 5].

Figure 6 (b) shows the shot map of the ADP2. The shift register chips (C9) are included in these positions on the 3-inch wafers for every fabrication run of the ADP2.

Table 2. Shift register chip specifications. Total junctions per chip: 68,990.

| Bit capacity of SR | No. of JJ | SR_bias (mA) | No. of SRs |
|--------------------|-----------|--------------|------------|
| 16-bit             | 90        | 2.75         | 2          |
| 64-bit             | 282       | 11           | 2          |
| 160-bit            | 666       | 28           | 2          |
| 640-bit            | 2589      | 110          | 2          |
| 1280-bit           | 5153      | 220          | 4          |
| 2560-bit           | 10281     | 440          | 4          |

Figure 7 shows the run-to-run variations of the yields for the SRs. In this figure, to clarify differences in the circuit size dependency of the yield, only two kinds of SRs are shown: the smallest 16-bit SR in the blue bar graphs and the largest 2560-bit SR in the red bar graphs. For each fabrication run, since the number of measured circuits is different, the number of measured circuits and the number of correct operations for 2560-bit SRs are shown on each yield bar graph. For example, for ADP644 No. 2, sixteen 2560-bit SRs were measured, and correct operations were obtained for fifteen circuits of 2560-bit SRs, giving a yield of 93.8%. We replaced the bias-sputtered SiO2 with the PECVD SiO2 from ADP643 No. 1. Although the yields of the small-scale 16-bit SRs were so far relatively high, the yields of the large-scale 2560-bit SRs had a large run-to-run variation and were often very small or zero. However, we could obtain very high yields with a good run-to-run reproducibility for the fabrication runs after the implementation of the PECVD SiO2.
Figure 8 shows a summary of the measured operating yield depending on the circuit size for the fabrication runs before and after using the PECVD. The number of measured circuits, number of correct operating circuits, and operating yields depending on the circuit size are shown on the bar graph. These tables are summaries of 74 measured chips of the fabrications before using the PECVD, and 26 measured chips of the fabrications after using the PECVD. Before using the PECVD, the operating yields decrease drastically with increasing bit capacity, as shown in figure 8 (a). We obtained only 47 correct operation circuits out of the 296 measured circuits for the largest 2560-bit SRs, that is, a poor operating yield of 15.9%. On the other hand, after using the PECVD, the reduction of the operating yields is very small, as shown in figure 8 (b). We could obtain 85 correctly operating circuits out of the 104 measured circuits, that is, a high operating yield of 81.7% even for the large-scale 2560-bit SRs with more than 10,000 junctions.

Figure 7. Run-to-run variation of yields for 16-bit and 2560-bit SRs. Here, yield means ratio of number of correct operation circuits to number of measured circuits.
Figure 9 shows an example of measured bias margins for SRs in a perfect chip (ADP644 No.2 Chip E6). The perfect chip means that all SRs in the chip were correctly operated. In this figure, the bias margins of top-to-bottom SRs correspond to those of left-to-right SRs in the chip shown in figure 6 (a). The wide operating margins of more than ±20% were obtained for all SRs. The reduction of the bias margin is small for increasing the circuit size from 16bit to 2560-bit. This means that circuit parameter variations due to the fabrication process are very small. In this chip, all SR circuits were correctly operated, which means that the SFQ circuits including a total of 68,990 Josephson junctions were successfully operated.

![Figure 9. Measured bias margins for SRs in perfect chip (ADP644 No.2 Chip E6). Horizontal axis indicates ratio (%) for designed SR bias currents, as shown in Table 2.](image)

Figure 10 shows the yields of the SRs on individual chips for the two wafers before and after using the PECVD. In these figures, the yields are represented as percentages of the correctly operated SRs for all the 16 measured SRs, regardless of the differences in their bit capacities and measured bias margins. These are examples of good fabrication runs including perfect chips. Before using the PECVD SiO$_2$, there was a large difference of the yields as shown in figure 10 (a) even in the good fabrication run. However, after using the PECVD SiO$_2$, the uniformity of the yields in the wafer has substantially improved, as shown in figure 10 (b). We could obtain three perfect chips within the measured 6 chips in this wafer. Other three chips were also very high yields. In this wafer, the number of the malfunctioning SRs was just 4. The number of defects is also considered to be just 4 or so in the SRs including in total 413,940 Josephson junctions for the 6 chips since these malfunctions are considered to correspond to defects on a one-to-one basis. This defect number shows that the fabrication yield of our ADP2 is at a level of 100,000 Josephson junction circuits. Moreover, we could successfully obtain nine perfect chips out of the 26 measured chips fabricated recently using the PECVD SiO$_2$.

5. Discussion
From the above mentioned results, we consider that the reliability of the ADP2 has improved substantially by the interlayer insulator forming methods using the PECVD SiO$_2$ deposition and ion milling.

The run-to-run reproducibility of the fabrication using the bias-sputtered SiO$_2$ was not good. We think that this was mainly due to the number of adherent particles on the bias-sputtered SiO$_2$ films. Many particles often occurred during bias-sputtering depositions since SiO$_2$ films adhered inside the bias-sputtering chamber were easy to peel due to their high film stress. Most causes for the defects such as open or short circuits and degradation of the junction characteristics are considered to be in these particles [6].
On the other hand, since our PECVD system is kept in a good condition by scheduled cleanings for both the PECVD chamber using C$_2$F$_6$ gas plasma and the SiC substrate tray using buffered hydrofluoric acid (NH$_4$F and HF mixture), it is considered that the PECVD SiO$_2$ films with very few particles were formed with an excellent run-to-run reproducibility. We could replace the bias-sputtered SiO$_2$ with the PECVD SiO$_2$ to the actual device structure of the ADP2 by adding the ion milling process. We believe that this led to the substantial improvement of the yields and run-to-run reproducibility for the SRs.

![Figure 10](image1.png)

**Figure 10.** Examples of yields of shift registers depending on chip positions of wafer fabricated using (a) bias-sputtered SiO$_2$ (ADP623 No. 2) and (b) PECVD SiO$_2$ (ADP644 No. 3).

### 6. Conclusion

We replaced bias-sputtered SiO$_2$ with PECVD SiO$_2$ for the Nb 9-layer advanced process (ADP2). The surface profile of the PECVD SiO$_2$ film was improved by adding an ion-milling process after the PECVD SiO$_2$ deposition. We solved the problems of the PECVD by using the improved method. For the recent fabrication runs using PECVD SiO$_2$, we could obtain a high operating yield of more than 80% with an excellent run-to-run reproducibility even for the large scale 2560-bit SRs with more than 10,000 junctions. Moreover, we could successfully obtain nine perfect chips out of the 26 measured chips fabricated using the PECVD SiO$_2$. From these results, we believe that the reliability of the ADP2 has improved substantially by the inter-layer insulator forming methods using the PECVD SiO$_2$ deposition and ion milling, and the fabrication yield of our ADP2 is at a level of 100,000 Josephson junction circuits.

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