Logic Verification of Ultra-Deep Pipelined Beyond-CMOS Technologies

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Abstract—Traditional logical equivalence checking (LEC) which plays a major role in entire chip design process faces challenges of meeting the requirements demanded by the many emerging technologies that are based on logic models different from standard complementary metal oxide semiconductor (CMOS). In this paper, we propose a LEC framework to be employed in the verification process of beyond-CMOS circuits. Our LEC framework is compatible with existing CMOS technologies, but, also able to check features and capabilities that are unique to beyond-CMOS technologies. For instance, the performance of some emerging technologies benefits from ultra-deep pipelining and verification of such circuits requires new models and algorithms. We, therefore, present the Multi-Cycle Input Dependency (MCID) circuit model which is a novel model representation of design to explicitly capture the dependency of primary outputs of the circuit on sequences of internal signals and inputs. Embedding the proposed circuit model and several structural checking modules, the process of verification can be independent of the underlying technology and signaling. We benchmark the proposed framework on post-synthesis rapid single-flux-quantum (RSFQ) netlists. Results show a comparative verification time of RSFQ circuit benchmark including 32-bit Kogge-Stone adder, 16-bit integer divider, and ISCAS’85 circuits with respect to ABC tool for similar CMOS circuits.

Keywords—Formal Verification; Logical Equivalence Checking; Superconducting Circuits; Ultra-Deep Pipelining.

I. INTRODUCTION

The ongoing demand for energy-efficient and high-performance computing has driven the development of semiconductors since its early days, but with the conclusive end of Moore’s Law and rising challenges to the physical scaling of CMOS devices [1], there is a significant need for new device technologies to continue beyond end-of-scaling CMOS technology. The exploration and study of novel logic components has been a main research focus in the past decade [2], in pursuit of extending the semiconductor industry roadmap beyond the CMOS technology [2]. Beyond-CMOS device concepts include a wide variety of elements such as charged-based components like Quantum-dot Cellular Automata (QCA) [3]. Additionally, the research community has also focused on exploring non-charge-based solutions such as spin-based components like Spin Wave Devices (SWD) [4] and NanoMagnetic Logic (NML) [5],[6]. Superconducting technologies such as rapid single-flux-quantum (RSFQ) [7], the quantum flux parametron (QFP) [8], reciprocal quantum logic [9], energy-efficient RSFQ (eSFQ) [10], and Adiabatic QFP (AQFP) [9] are also very promising candidates, given their potential to be 1000x as energy efficient as the state-of-the-art CMOS technologies. Such high levels of energy efficiency are strongly required for high-performance computers having performances in exa-FLOPS. As an example power consumption of CMOS technologies could exceed 100 MW, which is equal to the power generated by a small power plant [11]. Beyond-CMOS technologies, however have several constraints that prevents them from supporting complex designs. One of the constraints in these technologies is that in order to cascade elementary devices, the complete circuits need to be clocked [9], [12], [13]. Therefore, state of computer-aided design (CAD) tools available to these technologies communities has been both outdated and not suitable for complex designs.

Logical equivalence check (LEC) is one of the most important checks during the entire chip design process [14]. Design passes through various steps like synthesis, ECOs (engineering change orders), and numerous optimizations, therefore it is vital to efficiently verify that the logical functionality remains intact and does not break because of any of the automated or manual changes. Hence, developing suitable, LEC techniques for beyond-CMOS devices will reduce verification time and ensure the correctness of the circuit functionality as the complexity of circuits grows [14]. In this paper we introduce a novel logical equivalence check (LEC) framework for beyond-CMOS circuits. The proposed LEC framework is technology independent, i.e., it is able to verify not only the CMOS technologies, but also various candidate technologies of future thanks to its independence to details of technology such as timing and signaling requirements.

We summarize our contributions as follows:

- We propose a novel graph representation of the beyond CMOS circuit, which we refer to as the multi-cycle input dependency (MCID) circuit model. MCID represents functional behavior model of a clock-synchronous pipelined netlist and explicitly captures the dependency of primary outputs of the circuit on sequences of internal signals and inputs which affect outputs. This representation model enables unifying timing and functionality pieces of
information of the given circuit into a unique functional model. Mitering a MCID model and golden model, correctness of functionality of the given circuit can be verified by a customized LEC which uses Boolean Satisfiability (SAT) as an underlying reasoning engine.

- We also present an input timing control logic (ITCL) which handles different arrival times of inputs at primary inputs since inputs can be applied at different clock periods.
- We propose two algorithms for structural checks on 1) pin count nets (e.g., typically two in SFQ technologies) and 2) equalization of path delay (to ensure coherent data wave propagation).
- We have also implemented a parameterized LEC tool to validate the correctness of our approach in verifying the beyond-CMOS circuit functionality independently of the underlying technology details including signaling and timing. Depending on technology, parameters are set to abstract the timing and signaling information. For example, our tool is able to perform LEC on SFQ vs CMOS, or SFQ vs AQFP. With respect to the LEC in ABC [15], as a baseline, our tool obtains comparative verification time on a set of benchmarks including 32-bit Kogge-Stone adder (KSA), 16-bit integer divider and ISCAS’85 circuits.

The remainder of this paper is organized as follows. In Section II, we introduce the central concepts used in this work. Section III presents the required algorithms and models for LEC of beyond-CMOS technologies. Section IV presents benchmarking results for our proposed LEC methodology, followed by conclusions in Section V.

II. BACKGROUND & MOTIVATION

Hereafter, we introduce the general operating principles of beyond-CMOS technologies.

A. Ultra-Deep Pipelining

Ordinary pipelined systems [16], [17] can process more than one instructions on a set of data simultaneously and are divided to several stages, isolated by registers. Each of these stages nominally performs its part an operation (i.e., instruction) separately from rest of the stages. The data flow through each stage is determined by the global clock signal which allows processing of a new set of data only once the previous set has propagated to the next stage.

In contrast, ultra-deep pipelining may utilize each logic cell (gate) as a stage. This is feasible since beyond-CMOS gates may need a clock signal to operate. For instance, SFQ gates (except for non-clocked gates such as confluence buffer, Splitter, I/O cells, and T-Flip-Flops) need a clock signal to function. As an example, Fig. 1 shows the circuit diagram of an SFQ OR gate and the corresponding waveform to show its functionality. After the arrival of an input pulse, the arrival of clock pulse, results in an output pulse. This is interpreted as logic 1. However, no input pulse, results in no output pulse and this would be interpreted as logic 0.

Similar operating principles may exist for the variety of beyond-CMOS technologies including SWD [4], QCA [3], and NML [5], [6]. In [18], the authors proposed an efficient synthesis framework for aforementioned technologies. Zografos et al. [18] suggested that to take advantage of the non-volatility property (which would eliminate the need for a constant supply voltage and reducing the standby power consumption), all gates in the circuit need to be clocked in order to cascade elementary devices [4], [12].

In order to make use of both logic and memory capabilities of these beyond-CMOS technologies, their framework tackles the physical constraints of the circuits based on these devices by equalization of path delay to ensure coherent data wave propagation which is equivalent to ultra-deep pipelining introduced here.

For a gate in such technologies to operate correctly, all of its fanin gates should have the same logic level. If there is a difference among logic levels of fanins of a gate, some D Flip-Flops (DFF, or buffer, dependent on the underlying technology) should be inserted into outputs of fanin gates with smaller logic levels. For example, as shown in Fig. 2 if the first fanin (in1) of an AND2 gate has a logic level of one and the second fanin (in2) has a logic level of zero, one DFF should be added to the input of in2. Without path-balancing, correct pulses on in2 will be consumed by this AND2 gate one clock before arrival of the corresponding pulses on the first input, hence, this gate will not be able to produce correct output values. One of the most important constraints which ultra-deep pipelining imposes is that all the propagation paths from the combinational circuit’s inputs to outputs have approximately the same logic level (i.e., number of gates from primary inputs), then each data flow propagates uniformly to the outputs without interfering with adjacent flow.

B. Fanout Restriction

Synthesis tools for beyond-CMOS implementation should normally limit the cascading of one component, ensuring feasibility, given that several emerging technologies have no

![Fig. 1. SFQ OR gate (a) equivalence circuit (b) corresponding signal waveform.](image-url)
intrinsic gains [9], [13], [18]. For instance, in SFQ logic family, if a gate needs to have more than one fanout, a special SFQ gate called Splitter should be added to the output of this gate. Splitter is an asynchronous gate that accepts an SFQ pulse and produces an output pulse on each of its fanouts after its intrinsic delay. One Splitter can produce only two fanouts. For additional fanouts, more Splitter cells should be added in a binary tree structure. To have n fanouts, n−1 Splitter cells are needed.

Similarly, Zografos et al. [18] confirmed that one of the physical constraints of the circuits based on SWD [4], QCA [3], NML [5], [6] is fanout restriction that needs to be addressed so that the resulting circuit can be efficiently implemented in the selected technologies. Fanout limitations for different technologies may vary. For instance, for AQFP, Splitter cells are clocked buffers that can have 1-to-2, 1-to-3, and even 1-to-4 fanouts [9].

III. OUR VERIFICATION FRAMEWORK

This section introduces our LEC framework (see Fig. 3) along with the specific assumptions for the selected technologies. Additionally, the MCID graph modeling of beyond-CMOS circuits is described. Our framework takes into account the fundamental differences between beyond-CMOS and CMOS circuits. It starts with structural checks and then builds the MCID model. Finally, it verifies the correctness functionality of the given netlist using customized LEC functions.

A. Structural Checkers

The proposed LEC framework extracts the circuit network of gates and wires from gate-level structural model and analyzes the network to ensure that the circuit satisfies the fanout restriction (e.g., single fanout in the case of SFQ gates except for Splitter cells which can have a fanout of two) and also meets the path-balanced requirements to needed for ultra-deep pipelining. To verify these properties, we utilize two checkers, a circuit fanout checker followed by a circuit path-balancing checker.

First, we use the following definitions provided in [18]:

- Distance \( D \) between two different components, is the set of lengths of any path going from the source to the destination.
- Base distance \( BD \) of a component, is the set of lengths of any path going from any netlist input to that component. The maximum length in this set represents the depth of the component.

The fanout checker ensures that the given netlist satisfies the fanout restriction. For instance, in case of SFQ technology, Splitter cells must have been inserted to adjust the SFQ gate fanout for any logic cell driving two gates or more. The fanout checker extracts the circuit’s wire adjacency lists and verify that the size of each list is not larger than 1 (or 2 for Splitter cells).

Objectives of the path balancing checker are as follows, (a) all paths from one component to another must be equal in length; (b) maximum base distance of all netlist outputs must be equal. Differently worded, for any two connected components the minimum distance must be equal to its maximum distance. If the first goal is also obtained, then the base distance of all outputs must be equal as this set will only contain one number (see

![Fig. 2. (a) A digital CMOS circuit (b) Counterpart SFQ circuit where DFFs and Splitter cells are added for path-balancing and Fanout limitation, respectively.

Theorem 1. If the base distance of all outputs is equal as this set will only contain one number, then all paths from one component to another must be equal length.

Proof. Proof by contrapositive. The contrapositive of the above statement is, if two paths \( P_1 \) and \( P_2 \) from one component \( comp_1 \) to another \( comp_2 \) are not equal in length, the base distance of at least one output \( PO_y \) contains at least two numbers. Since there is at least one path from one primary input \( PI_x \) to \( comp_1 \) (e.g., \( P_{PIx,1} \)) and similarly from \( comp_2 \) to one primary output \( PO_y \) which exist two unequal-length paths from \( PI_x \) to \( PO_y \) which are \( \{P_{PIx,1}, P_1, P_{2,PO_y}\} \) and \( \{P_{PIx,1}, P_1, P_{2,PO_y}\} \). So, Theorem 1 is proved.

B. MCID and ITCL

Equal propagation paths from inputs to outputs is a sufficient, but not necessary condition. More specifically, we have observed that an SFQ circuit may not be fully path-balanced yet

Algorithm 1. Path-Balancing Checker

| Input: \( P1 \) (circuit’s Primary input list), \( G \) (circuit’s DAG) |
| Output: Path balancing checker result |
| 1: For each element in P1 do |
| 2: BaseDistanceList = BaseDistanceList U PathDepthCounter() |
| 3: If BaseDistanceList values are not all one value then |
| 4: Return Fail |
| 5: Return Pass |
function correctly. A high-throughput Arithmetic Logic Unit (ALU) SFQ design with different arrival times of inputs [19], [20], custom design circuits with false paths [21], and synthesis methodology of area-efficient SFQ circuit [22]. Therefore, structural checkers are not sufficient to check specific properties of the new technologies. Hence, the following approaches are introduced and implemented as part of the proposed LEC.

1) MCID Graph

Functional error because of partially-balanced paths only can be captured by observing circuit behavior during several clock cycles. This is due to the fact that the output result of partially-balanced circuit depends on the inputs of multiple previous clock cycles not only one specific clock cycle which is the case in CMOS technology. In the following we introduce several definitions that will be used in this section.

- Each clocked gate generates a pulse at its output in the following clock cycle after receiving required pulses at its input(s). Hence, delay of each gate is assumed to be one clock cycle as also referred to as one time unit.
- Path delay is defined by the number of time units required by a signal to propagate on that path which is equal to number of clocked gates.

In a circuit where the shortest path delay from inputs is \( D_{P_s} \) time units, and the longest path delay is \( D_{P_l} \) time units, the current output \( O_t \) depends on the inputs of \( I_{t-D_{P_s}}, I_{t-D_{P_s}-1}, ..., I_{t-D_{P_l}} \) where indices denote the times of input with a step of one time unit. Each index is called a time step (i.e., time unit). Upper bound of number of time units to observe is circuit longest path. In simpler words, the older inputs (the inputs of the time units more distant from current time \( t \) ) influence the output through longer paths and the newer inputs (the inputs of the time units closer to the current time \( t \) ) affect the output through shorter paths. LEC tools for CMOS circuits check only the functionality of circuits over all possible input vectors at one specific time step which is meaningless in the case of beyond-CMOS circuits (see Fig. 4). Hence, we propose a clock-synchronous logical model of a circuit explicitly capturing multi-cycle input dependencies which helps to unify time and functional pieces of information into the functional domain.

Fig. 3. Flowchart of proposed LEC framework.

Fig. 4. An example of SFQ circuits with different path delays from inputs to outputs.

The MCID model represents the functional behavior model of a clock-synchronous pipelined netlist which explicitly captures the dependency of primary outputs of the circuit on sequences of inputs which affect outputs. This model enables analyzing the functional behavior of beyond-CMOS circuits using customized LEC functions. The underlying idea is that a signal \( s_t \) represents a signal \( s \) of the given circuit at time step \( t \). The process of constructing MCID graph is described in Algorithm 2. The input data of this algorithm is a circuit netlist. For each gate the algorithm creates as many copies of values of the gate at different time steps as necessary to determine the output. The algorithm starts from Primary Outputs (PO) and traverses the given circuit graph backward (line 2). Given the delay of one time unit to each clocked gate in the given circuit, the output of a gate depends on its corresponding inputs one time step before. These inputs are given by the predecessor node of the output in the given circuit graph (line 6). Given the output and its driving inputs, a new gate is created in which the output and the inputs have the timing difference of one time unit (lines 11 and 13). Note that non-clocked gates like Splitter cells must be treated differently. Such gates don’t receive any clock signal, so the output (e.g., pulse in RSQ technology) of them is generated at the same time step as input of them. We copied the non-clocked gate (except Splitter whose functionality is the same as buffer and we can skip it) and also find its predecessor node at the same time step (line 7-11). The inputs of gates at the current step are collected in the set \( SIG_temp \) to be used for the next backward traversal step (lines 14–16). If the input is a Primary Input (PI) or already exists in the set \( SIG_temp \) (fanout case), or if it will not be added to the set \( SIG_temp \) (line 15). This new circuit called the MCID circuit. MCID model generation has worst-case runtime complexity of \( O(|G|) \).
Theorem 2. Assuming MCID, as the MCID model for the the PO at time step \( (PO) \), it is guaranteed that MCID, models all time steps of internal signals and inputs which affect PO.

Proof. Proof by construction. The MCID model is constructed by traversing a given circuit one step time wise via Breadth-First Search (BFS) from the output PO towards PIs. Algorithm 2 visits every gate at least once. If a gate \( g \) is visited, three cases may occur as follows:

- Case 1: The gate \( g \) is visited only once. In this case, signal \( s \) the output of gate \( g \) never reconverges. Because if signal \( s \) reconverges, gate \( g \) is visited at least twice while traversing the circuit by the algorithm from the output PO backwards. Therefore, the value of signal \( s \) only at one time step affects the value of PO.
- Case 2: The gate \( g \) is visited through paths with the same path delays. In this case, only the value of signal \( s \) at one time step affects output \( o \) through multiple paths. Because the paths have the same path delays to output \( o \). Line 15 in Algorithm 2 checks whether a gate has been visited through paths with the same path delays. If a gate is visited for the first time through a path, the if-expression becomes true. But if a gate is visited for the second time through a path with the same path delay, the if-expression becomes false and the corresponding gate only once at one time step is copied.
- Case 3: Gate \( g \) is visited through paths with different path delays. In this case, the value of signal \( s \) at different time steps affects PO. In this case, the if-expression of line 15 in Algorithm 2 is false every time. Therefore, gate \( g \) is copied for all corresponding time steps.

Hence, the MCID, constructed by Algorithm 2 models all time steps which may affect PO. This proves Theorem 2.

Algorithm 2. MCID (Multi-Cycle Input Dependency) Constructor

**Input:** Circuit netlist, PI (circuit’s primary input set), PO (circuit’s primary output set), NCG (non-clocked gates set)

**Output:** MCID model

1: \( \text{Clock}\_\text{cycle} = 0 \)
2: \( \text{SIG} = \text{PO} \)
3: While \( \text{SIG} \neq \{\} \) do
4: \( \text{SIG} = \text{SIG} \cup \{\} \)
5: For each \( \text{sig} \in \text{SIG} \) do
6: \( \text{gate} = \text{predecessor(sig)} \)
7: If \( \text{gate} \in \text{NCG} \) then
8: \( \text{MCIDModel.copy} (\text{gate}, \text{ICl}=\text{clock}\_\text{cycle}, \text{oCl}=\text{clock}\_\text{cycle}) \)
9: \( \text{MCIDModel.copy} (\text{gate}, \text{ICl}=\text{clock}\_\text{cycle}, \text{oCl}=\text{clock}\_\text{cycle}) \)
10: Else
11: \( \text{MCIDModel.copy} (\text{gate}, \text{ICl}=\text{clock}\_\text{cycle}, \text{oCl}=\text{clock}\_\text{cycle}) \)
12: For each \( \text{input} \in \text{SIG} \) do
13: \( \text{MCIDModel.copy} (\text{gate}, \text{ICl}=\text{clock}\_\text{cycle}, \text{oCl}=\text{clock}\_\text{cycle}) \)
14: If \( \text{input} \in \text{SIG} \) and \( \text{input} \in \text{PI} \) then
15: \( \text{SIG} = \text{SIG} \cup \text{input} \)
16: \( \text{SIG} = \text{SIG} \cup \text{input} \)
17: \( \text{Clock}\_\text{cycle}++ \)
18: Return MCID

2) ITCL

Input timing control logic unit (ITCL) is added for controlling the inputs arrival time. Assume that a circuit is designed such that its inputs pulses must be applied in different clock cycles. To handle such cases, ITCL adds buffer(s) gate to MCID circuit inputs which receive input pulses later than other(s). For instance, the inputs arrival time given by designer is

\[ T(I): [t_{i_1}, t_{i_2}, ..., t_{i_n}] \]

where \( t_{i_1} \) represents the arrival time of input \( I_x \). ITCL finds \( \arg \min \{ t_{i_x} | I_x \in I \} \), i.e., \( \text{minI} \), and adds \( t_{i_x} - t_{\text{minI}} \) buffer(s) to input \( x \) of MCID circuit.

To generate the miter circuit of combining MCID model and golden model, the common inputs must be matched. Note that the main key in customized LEC functions is the use of structural similarities to reduce the size of SAT instance and hence to speed-up the LEC process. However, in the final MCID circuit, we may have several inputs in different clock cycle that can be matched to one primary input of golden model. So, to help customize the LEC function for finding structural similarities, it is crucial to find the largest subset of inputs arrived at same clock cycle of MCID circuit and match them to the primary inputs of golden model. Hence, there may be input(s) of MCID model that does not connected to any input of golden model. Overall, the final generated miter circuit is shown in Fig. 5. Following are the details of miter circuit,

\[ \phi_1 = C_1(l_1(t)) \]

\[ \phi_2 = C_2(l_2) \]

Fig. 6 shows an example of building MCID circuits and then applying ITCL. The SFQ circuit in Fig. 6 (a) is supposed implement \( \text{abcd} \) but it is not fully path-balanced. So, using the corresponding MCID circuit (see Fig. 6 (b)) an error trace can be found, i.e.,

\( l_1(t) = \{ [a = 0, b = 1, c = 1, d = 1]_{\text{clock cycle} = 0}, \]
\( [a = 0, b = 1, c = 1, d = 0]_{\text{clock cycle} = 1} \)

\( l_2 = [a = 0, b = 1, c = 1, d = 0] \)

Note that MCID model is in functional domain, so, only functionality of all gate is considered in customized LEC functions. That’s the reason for removing clock pin from each gate and replacing the DFF with buffers. However, if the designer makes the circuit partially-balanced on purpose since input \( d \) arrives one clock cycle later than other inputs, ITCL adds one buffer in front of that input pin as shown in Fig. 6 (c) and the circuit meets its specification.

IV. EXPERIMENTAL RESULTS

In this section, the efficacy of the proposed LEC is investigated. First, we introduce SFQ technology which we used for benchmarking our LEC framework. Next, the experimental setup and experimented combinational SFQ circuits are described. Two types of design errors, namely functional and structural errors are inserted to the netlist. Finally, the performance of MCID model in detecting these errors is presented.
A. Technology

Developed in the late 1980s, a very promising family of “beyond-CMOS” devices are single flux quantum (SFQ) circuits based on Josephson junction [7]. Similar to how CMOS circuits are built with transistors (3-terminal devices) as their active elements, SFQ circuits are built using Josephson junctions (JJ, 2-terminal devices) as their active components. When Josephson Junctions are operated at cryogenic temperatures, a phenomenon of a current called super-current that flows indefinitely long without any applied voltage. As a result, SFQ circuits benefit from Josephson junctions with high switching speeds on the order of picoseconds and low switching energy on the order of \(10^{-18}\) joules at 4.2 Kelvin [23]. The switching energy of Josephson junctions is two to three magnitudes lower than that of end-of-scaling CMOS devices [1]. Thus, SFQ circuits have demonstrated the potential to achieve the computing demands for energy-efficient and high-performance circuits [10], [24]. The rapid SFQ (RSFQ) technology is a new version of SFQ in which the parameter margins of the SFQ as well as operation speed to 300 GHz are increased [7]. (R)SFQ gates are pulsed-based and the presence and absence of a pulse are considered as “1” and “0”, respectively. A pulse is a single quantum of magnetic flux (\(\Phi_0 = h/2e = 2.07 m\text{V} \times ps\)) with a duration of a few ps and amplitude of a few mV.

B. Experimental Setup

The computer system used for the testing utilized an Intel Core i7-7700HQ CPU with nominal clock frequency of 2.8 gigahertz and 16 gigabytes of RAM. Among the available (open source) tools, ABC [15] was selected as the baseline verification tool. ABC is relatively fast and scalable compared to other open-source tools. The considered combinational SFQ circuits include Kogge-Stone adders (KSA), array multipliers, integer dividers, and ISCAS’85 combinational benchmark circuits [25]. Since our tool objective is to verify correct functionality of post-synthesis netlist, we used [13] as a synthesis tool to generate equivalent gate-level structural model from given a combinational circuit. Parameters including number of fanout constraints, non-clocked gates, and an indicator for ultra-deep pipelined circuits are set to abstract the timing and signaling information.

In order to evaluate the effectiveness of MCID model, two types of design errors were inserted to the netlist, functional and structural errors. Functional errors are those which change the functionality of circuit by swapping gates. As post synthesis SFQ circuits should be fully path-balanced and each gate should have limited fanout count, there exists two kinds of structural errors. One is to make the circuit partially-balanced by deleting a DFF. The other is to increase the number of fanouts of a gate by removing a Splitter.

C. LEC Results

With these inserted errors, the proposed LEC framework was evaluated under circuit designs to indicate the effectiveness of the proposed checkers and models, specifically in terms of verification scalability and runtime.

1) Performance of Proposed LEC

Each entry of runtime and number of gates after applying MCID model are average of ten runs of LEC framework for different type of errors. The functional errors were generated by swapping different kinds of gates. The Structural errors were created by randomly removing one or two DFFs near the primary outputs and by randomly removing one Splitter. Verification results are summarized in Table I. The results for 4-, 8-, 16-bit array multiplier as well as integer divider and KSA have been derived but are not included in this paper for brevity. One of the advantages of implemented tool is that it can generate the error trace similarly to conventional LEC tools. Furthermore, it also keeps track of the information about input vector arrival time. In other words, it has information about values of each input at different clock cycles that generate the wrong output. The results show that the proposed framework detects functional and structural errors in a very short runtime. Meanwhile, for partially-balanced circuits, it also shows the number of gates in the MCID model. We believe the following are the reasons for the short runtime of the proposed LEC, the used benchmark [25] consists of combinational logic circuits. The Verilog implementations of those circuits are almost all data-flow style. In data-flow style, the behavior of the logic is represented by Boolean operations and assignments. The corresponding networks of Verilog modules are therefore very similar to those of the synthesized netslits. As the proposed LEC utilizes the structural hashing (as the ABC does) of the internal nodes, the equivalence checking process of those similar (pre-synthesis and post-synthesis) structures would be fast. To validate this, we assess the implemented tool under different types of an 8-bit multiplier and report the results in section IV.C.3.
\[ \text{# of added gates} = 2^{D_{\text{Spli}}} - 1 \]

where \( D_{\text{Spli}} \) is the path delay of Splitter (i.e., the closest Splitter to removed DFF.) An Example is shown in Fig. 8 (a) where the number of added gates in MCID model is 7. Another factor in number of copied gates is reconvergent paths which is dependent on the number of Splitters. So, for the Splitter followed by a removed DFF which cause reconvergent paths with different base distance, the upper bound of number of copied gates can be calculated by summation over the Splitters (e.g., Fig. 8 (d)).

\[ \text{# of added gates} = \sum_{\text{Spli} \in \text{Splitter cells}} 2^{D_{\text{Spli}}} - 1 \]

Two examples are shown in Fig. 8 (b) and (c). Fig. 8 (b) shows two independent reconvergent path while the circuit of Fig. 8 (c) has two DFFs in one reconvergent path. Fig. 8 (d) depicts MCID circuit of Fig. 8 (c). As equation (4) shows, the upper bound of added gates is number of Splitters times number of gates before each Splitter (which is, in worst case, a binary tree by height of logical level of Splitter.) Therefore, the MCID model is linearly larger than the original circuit.

We calculate the upper bound for the largest circuit of each type which are 32-bit KSA, 16-bit integer divider and 16-bit array multiplier. We consider them as corner cases and further evaluate the effectiveness of MCID model using them. Table II lists the average verification runtime of ten experiments based on the corner cases, the original number of gates, as well as the upper bound of total number of gates in MCID circuit in different benchmark circuits. The upper bound for MCID circuits was generated according to Section IV.C.2. Results show even for the largest MCID circuits built from benchmark circuits, the proposed LEC still can detect structural errors in a reasonable time.

![Fig. 7](image1)

**Fig. 7.** An example of duplicating a gate within MCID model. (a) SFQ circuit, (b) corresponding MCID model.

![Fig. 8](image2)

**Fig. 8.** (a) A 5-level SFQ circuit with one reconvergent path where \( D_{\text{Spli}} \) is 4 and the number of added gates in MCID model is 7. (b) A 4-level SFQ circuit with two independent reconvergent path where \( D_{\text{Spli}} \) is 2 and the number of added gates is 2 in MCID model which is twice the number of added gates in each reconvergent path. (c) A 5-level SFQ circuit with two DFF in one reconvergent path, (d) Corresponding MCID circuit after removing 2 DFFs. The gates copied in MCID are highlighted by red and blue colors.

### 3) Scalability

In order to show the scalability of the proposed LEC, we compare its runtime to that of ABC which is a scalable verification tool. We used three different types of multipliers including an 8-bit Booth multiplier, an 8-bit Wallace multiplier, and an 8-bit Dadda multiplier as golden models and verified the correct functionality of an 8-bit array multiplier using these golden models. We choose multiplier circuit since it has been shown that checking arithmetic mites is still a challenge in hardware verification [26]. The experimental results are showed in Table III. Table III indicates scalability of our implemented
tool as our tool has comparable runtime with respect to ABC. Our results also show that in case of 16-bit multiplier, both ABC and our tool cannot finish verification process in limited time budget, e.g., 12 hours.

By adding the structural error(s), ABC still consider the circuits as equivalent but the proposed LEC can generate the error trace in less than 1 second. The main reason is that ABC only consider the functionality of each gate in its LEC functions. For instance, ABC treats DFFs that are inserted during the synthesis of RSFQ circuits to perform path balancing in beyond-CMOS are considered as simple buffers which is a non-clocked gate.

### TABLE II. EFFECTS OF MCID MODEL SIZE ON EFFICIENCY OF THE PROPOSED LEC.

| Benchmark | Type of Error | Run Time | Golden | # of Gates SFQ | MCID Circuit |
|-----------|---------------|----------|--------|----------------|--------------|
| KSA32     | Structural    | 0.01     | 449    | 1423           | 1914         |
| ArrMult16 | Structural    | 0.12     | 1872   | 5768           | 61409        |
| IntDiv16  | Structural    | 0.04     | 1325   | 19261          | 90870        |

### TABLE III. RUNTIME OF THE PROPOSED LEC AND ABC.

| Benchmark   | Golden Model | LEC Tool  | Runtime (s) |
|-------------|--------------|-----------|-------------|
| ArrMult8    | 8-bit Booth multiplier | proposed LEC | 11.736 ABC |
| ArrMult8    | 8-bit Wallace multiplier | proposed LEC | 21.603 ABC |
| ArrMult8    | 8-bit Dadda multiplier | proposed LEC | 20.980 ABC |

V. CONCLUSION

We presented a logical equivalence checking framework, based on a novel circuit model called MCID, which is able to perform logic verification of beyond-CMOS technologies independently from the underlying details of signaling and timing. The framework consists of several structural checkers of new technologies constraints satisfaction and build on top of conventional CMOS LEC tools. We additionally presented a multi-cycle input dependency circuit model to explicitly capture the dependence of primary outputs of the circuit on all possible sequences of primary inputs. We further proposed an input timing logic that effectively handled different arrival time of inputs and facilitated the miter circuit generation. We benchmarked the framework on post-synthesis netlists with an RSFQ technology. Results showed a comparative verification time of RSFQ circuit benchmark including ISCAS’85 circuits with respect to ABC tool for similar CMOS circuits. Results confirmed that proposed framework efficiently consider main technological constraints for emerging technologies.

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