PLL-Based Charge Control Scheme for SIMO Buck DC-DC Converter

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Abstract This paper presents a phase-locking-loop-based (PLL-based) charge control scheme to enhance the cross regulation (CR) performance of charge-controlled SIMO Buck DC-DC without freewheel period. By combining PLL structure with the traditional charge control scheme, each channel could be regulated by an independent charge control loop. Moreover, a gain-adapted charge pump (GACP) technique is applied for the stability in multi-load condition. The multi-loop stability and CR expressions are derived to improve their relative performance. Experimental results show that the proposed scheme can achieve worst-case CR of 0.052mV/mA in 384mA load transient, and 0.038mV/mA CR in 150mA load transient with at least 43.2% improvement above the existing charge control schemes.

Key words: SIMO Buck DC-DC, Charge control scheme, PLL, Cross regulation

Classification: Power devices and circuits

1. Introduction

Single-inductor multiple-output (SIMO) Buck DC-DC, using only one inductor to generate multiple DC outputs, shows many advantages of integration and flexibility in the low power management systems, and becomes a research hotspot. However, since SIMO Buck DC-DC has to face more load conditions than single output DC-DC, it has higher average inductor current and more complicated control scheme. Furthermore, an additional parameter called cross regulation (CR) is introduced to describe the decreased DC output performance. Ordered power-distributive control (OPDC) [1] is one of two main time sequences of inductor current distribution. It delivers charge to all DC outputs successively in one switching period, and can hold heavy inductor current while balancing output voltage ripple and efficiency. But OPDC still has difficulty analysing control scheme and performs bad CR.

CR represents the voltage variation of one channel’s DC output on the load transient of the other channels, and can be expressed as \( \frac{\Delta V_{oi}}{\Delta I_{oi}} \). To suppress CR of the OPDC SIMO, charge-balance control [1–21] was reported. Among them, charge control has already proven itself of good performance on CR suppression [2–8]. The typical charge control loop is exhibited in Fig. 1, acting as sub-converter for the corresponding channel. But because the end timing of a switching period in OPDC is determined by the beginning of next switching cycle, this charge control loop can not be applied to the last DC output. Therefore, the last output in [2, 3] has the worst CR performance. Freewheel period in [4] is set as an additional non-DC-output channel to balance accumulated error and buffer the worst CR of the last output. But freewheel period increases the inductor current, and will limit efficiency and application scene. This additional channel costs more chip area further. In order to control every channel equally without using freewheel period, phase locking loop (PLL) is introduced to lock switching frequency [22–24]. Unfortunately, additional PLL loop may cause multi-loop stability problems. Besides, existing switching-frequency-locked PLL-based SIMO without freewheel is only compatible with ripple-based control [22–29], in which the DC error of output voltage can be increased, and the switched inductor current introduces large interference to noise-sensitive controller when loads get heavier [30]. These make the CR measurement of ripple-based control difficult and limit the load range.

In this paper, a PLL-based charge control scheme is proposed to decrease CR. By applying charge control loops to all the outputs of SIMO Buck DC-DC, the CR to the last channel is obviously reduced. Utilizing paralleled charge control loops to constitute current controlled oscillator (CCO), the
The proposed SIMO Buck DC-DC could act as a PLL to make power stage’s switching frequency \( F_{sw} \) locked to its reference \( F_{ref} \). Besides, the gain-adapted charge pump (GACP) technique keeps this PLL structure stable when load changes sharply. A detailed small signal model is also given for CR and multi-loop stability analysis.

2. The Proposed PLL-based Charge Control Scheme

The architecture of PLL-based charge-controlled SIMO Buck DC-DC is illustrated in Fig. 2. The power stage contains \( n + 2 \) power switches \( MP, MN, M_{<1:n>} \), an inductor \( L \) and \( n \) output capacitors \( C_{o <1:n>} \). The \( V_g \) and \( I_o <1:n> \) (or \( R_o <1:n> \)) represent the voltage source and loads, respectively. The rest belongs to the controller, including \( n \) charge control loops, Logic cell, phase frequency detector (PFD), GACP\&low pass filter (LPF), proportion differentiation (PD), current loop and deadtime\&driver module. The deadtime\&driver module acts as an interface between controller and power stage, converting \( D, D_{<1:n>} \) into \( PS_P, PS_n, PN_{<1:n>} \) to drive the corresponding power switches \( MP, MN, M_{<1:n>} \).

There is an independent charge control loop in every DC output. It generates logic signal \( S_{<1:n>} \) according to inductor current sensing signal \( V_{cr} \) and the corresponding output error \( V_{c} \). The pulse of \( S_{<1:n>} \) indicates the boundary of duty ratio signal \( D_{<1:n>} \). The logic block then generates \( D_{<1:n>} \) from \( S_{<1:n>} \) on the basis of OPDC, and uses \( D_{1} \) as the real switching frequency signal \( F_{sw} \). Since every end timing of switching cycle is determined by the pulse of \( S_{n} \), \( F_{sw} \) is unknown and influenced by \( I_{o <1:n>}, V_{c <1:n>} \) and \( I_L \). The paralleled \( n \) charge control loops form a CCO.

In Fig. 2, PFD, GACP\&LPF, PD, current loop and CCO construct a full PLL structure. The role of current loop is to limit the inductor current \( I_L \) proportional to \( V_{c} \). GACP\&LPF compensates the variable gain of CCO’s transfer function, and PD compensates the closed PLL loop. PFD detects the difference of phase and frequency between \( F_{sw} \) and \( F_{ref} \).

The mentioned charge control loop, current loop and PLL loop, along with CR, will be analysed in the following part, where captain signal \( V_c \) represents its DC state, and has a relevant small signal \( \hat{V}_c \). The mathematic relationship between \( V_c \) and \( \hat{V}_c \) comes from perturbation and linearisation.

2.1 Charge Control Loop

The circuit of charge control loop is shown in both Fig. 1 and Fig. 2. The charging time of \( C_r \) can be written as:

\[
\frac{D_t}{F_{sw}} = \frac{A_{cr} C_{cr} V_{ci}}{I_L} \tag{1}
\]

considering perturbation and linearisation, small signals from Eq. (1) become as:

\[
\hat{d}_t = \frac{A_{cr} C_{cr} F_{sw}}{I_L} V_{ci} - \frac{D_t}{I_L} \hat{i}_L + \frac{A_{cr} C_{cr} V_{ci}}{I_L} \hat{f}_{sw} \tag{2}
\]

Then, the small signal model of charge control loop is shown in Fig. 3, where the \( G_{vcr}(s) \) is the transfer function of proportion integration (PI) \( PI \).

If the closed-loop gain of charge control loop \( T_{cri}(s) \) is defined:

\[
T_{cri}(s) = \frac{A_{cr} C_{cr} F_{sw} G_{vcr}(s)}{s R_{oi} C_{oi} + 1} \tag{3}
\]

Some expressions can be obtained:

\[
\hat{v}_{oi} = \frac{T_{cri}(s)}{T_{cri}(s) + 1} \hat{v}_{refi} + \frac{T_{cri}(s)}{T_{cri}(s) + 1} \frac{V_{ci}}{F_{sw}} F_{sw} G_{vcr}(s) \tag{4}
\]

\[
\hat{v}_{ci} = G_{vcr}(s) \hat{v}_{refi} - \frac{T_{cri}(s)}{A_{cr} C_{cr} F_{sw}} \hat{i}_{oi} \tag{5}
\]

\[
T_{cri}(s) = \frac{T_{cri}(s) V_{ci}}{T_{cri}(s) + 1} + \frac{1}{F_{sw}} F_{sw} \tag{6}
\]

From Eq. (4), closed charge control loop makes \( \hat{v}_{oi} \) only be affected by \( \hat{f}_{sw} \), which demonstrates that the frequency-lock capability of PLL loop has decisive effect on CR performance. And Eq. (5) indicates the relationship between load \( i_{oi} \) and error signal \( \hat{v}_{ci} \) in a charge control loop. If summing both sides of Eq. (1) with i from 1 to n, the \( F_{sw} \) will be function of \( V_c = \sum^n_{i=1} V_{ci} \) and \( I_L \):

\[
F_{sw} = \frac{I_L}{A_{cr} C_{cr} V_{ci}} \sum^n_{i=1} V_{ci} \tag{7}
\]
Equation (9) indicates that the frequency of paralleled charge control loops \( f_{sw} \) is the linear function of inductor current \( i_L \) with a variable argument \( V_{ct} \). And Eq. (9) is also the transfer function of CCO.

![Small Signal Model of PLL Loop with Current Loop Inside](image)

**Fig. 4.** Small Signal Model of PLL Loop with Current Loop Inside

### 2.2 PLL Loop

Including the CCO, the whole SIMO Buck DC-DC behaves a PLL. The small signal model of circuits in Fig. 2 is shown in Fig. 4, where the relationship between transfer functions and blocks is pointed out. GACP uses \( V_{ct} \) to generate charge pump current \( I_{cp} = \frac{V_{ct}}{nK_{cr}} \), which compensates the transfer function of CCO in multi-load condition. Because LPF diminishes the nonlinearity induced by switching of GACP, \( V_{ct} \) is not appeared in GACP&LPF module in Fig. 4. The inside current loop can be simplified since it is relatively independent. By defining the closed-loop gain of current loop:

\[
T_{cl}(s) = G_{vel}(s) \frac{1}{V_{peak}} \frac{V_{g}}{sL A_L} \tag{10}
\]

The expression from \( v_{cl}^* \) to \( i_L \) can be written as:

\[
i_L = \frac{T_{cl}(s)}{T_{cl}(s) + 1} R_f \frac{V_{cl}}{sL A_L} \tag{11}
\]

Therefore, the closed loop gain of the PLL loop \( T_{vl}(s) \) is obtained:

\[
T_{vl}(s) = \frac{T_{cl}(s) A_L G_{pd}(s)(T_{cr}(s) + 1)}{T_{cl}(s) + 1} \frac{1}{R_f} sLC_{zlpf} + \frac{1}{sC_{zlpf}} \tag{12}
\]

At the bandwidth nearby, the \( T_{vl}(s) \) has no variational argument, and \( G_{pd}(s) \) compensates the phase for two low frequency poles (one in \( T_{cr}(s) \)). It means that the PLL can keep well stable in multiple loads \( I_{r<1>m} \) condition. But since \( T_{vl}(s) \) is affected by \( T_{cr}(s) \) after closed loop compensation, the gain and bandwidth of \( T_{vl}(s) \) are limited, and change of the \( C_{pd}(s) \)'s phase-compensation-frequency \( F_{comp} \) will result in distinguishable CR performance.

### 2.3 CR Expression

To express CR using small signal model, assuming that load transient \( i_{aj} \) happens in \( s \) DC output. Then \( v_{cj} \) can be obtained from Eq. (5) and affects \( f_{sw} \) through Eq. (8), which eventually induces CR to \( v_{cj} \) in Eq. (4). There are two feedbacks to influence \( f_{sw} \) of Eq. (8). In the positive feedback, the \( v_{ct} \) of Eq. (6) increases change of \( f_{sw} \). While in the negative feedback, the \( i_L \) in PLL loop decreases change of \( f_{sw} \). The expression of \( \hat{i}_L \) is:

\[
\hat{i}_L = \frac{T_{cl}(s) A_L V_{ct} G_{pd}(s) (R_{cJ} + 1 + \frac{1}{sC_{zlpf}})}{T_{cl}(s) + 1} \tag{13}
\]

Substituting small signal \( \hat{i}_L, v_{cl}^* \) and \( v_{cj} \) of Eq. (13), (6) and (5) respectively into Eq. (8) can get:

\[
\hat{f}_{sw} = \frac{\frac{T_{cl}(s)}{T_{cl}(s) + 1} \frac{V_{cl}}{sL A_L} - \frac{T_{cl}(s) A_L G_{pd}(s)(T_{cr}(s) + 1)}{T_{cl}(s) + 1} \frac{1}{R_f} sL C_{zlpf} + \frac{1}{sC_{zlpf}}}{1 + \frac{T_{cl}(s)}{T_{cr}(s) + 1} \frac{V_{cr} - V_{cj}}{V_{cr}}} \tag{14}
\]

Concluding from Eq. (4) and (14), the CR expression can be simplified as:

\[
\frac{v_{ci}^*}{i_{aj}} = \frac{\frac{T_{cl}(s)}{T_{cl}(s) + 1} \frac{V_{cl}}{sL A_L} - \frac{T_{cl}(s) A_L G_{pd}(s)(T_{cr}(s) + 1)}{T_{cl}(s) + 1} \frac{1}{R_f} sL C_{zlpf} + \frac{1}{sC_{zlpf}}}{1 + \frac{T_{cl}(s)}{T_{cr}(s) + 1} \frac{V_{cr} - V_{cj}}{V_{cr}}} \tag{15}
\]

The Eq. (15) can optimize CR performance of proposed PLL-based charge control scheme. It declares that the CR of \( i \) DC output is related to uncontrollable load segments \( I_{oi} \), \( I_{oj} \) and \( I_L \) (sum of loads). Although increasing the gain of \( T_{vl}(s) \) among the whole bandwidth can be obviously effective to decrease the value of Eq. (15), the gain of \( T_{vl}(s) \) is limited from the above analysis of PLL loop. From the view of PLL structure, a larger bandwidth has advantage on locking speed but disadvantage on stability. Unfortunately, both loss of lock and low stability of PLL loop in Fig. 4 bring about large CR. Thus, an appropriate phase-compensation-frequency \( F_{comp} \) of PD and LPF is critical to the design with best CR performance.
3. Experimental Results

The proposed PLL-based charge control scheme is verified by simulation of one input four outputs SIMO Buck DC-DC on Matlab/Simulink. The parameters are listed in Table 1. The transfer functions of $G_{cr}(s)$, $G_{vcl}(s)$ and $G_{pd}(s)$ are nonideal and can be realized by circuits. The transfer functions of LPF and $G_{pd}(s)$ in the PLL loop have a tuning segment $F_{comp}$.

| Table 1. Experimental Parameters Value |
|----------------------------------------|
| Power Stage                            |
| $F_{ref}$                              | 1MHz                          |
| $V_{ref<14>}$                          | 0.9V, 1.2V, 1.5V, 1.8V        |
| $L$ with DCR                           | 4.7$\mu$H with 25m$\Omega$   |
| $C_{o<14>}$ with ESR                  | 10$\mu$F with 20m$\Omega$    |
| Charge Control Loop                    |
| $A_{cr}$                               | $5 \times 10^4$               |
| $C_{cr}$                               | $0.4pF$                       |
| $R_{cr}$                               | $1$M$\Omega$                  |
| $G_{vc}(s)$                            | $3 \times 10^{-1}s + 957.8$  |
| $2.543 \times 10^{-3} s + 1$          |
| Current Loop                           |
| $A_L$                                  | $2.5 \times 10^4$             |
| $V_{peak}$                             | $1.8V$                        |
| $R_f$                                  | $15k\Omega$                   |
| $G_{vc}(s)$                            | $3 \times 10^{-1}s + 957.8$  |
| $2.543 \times 10^{-3} s + 1$          |
| PLL Loop                               |
| $R_{clpf}$                             | $2k\Omega$                    |
| $C_{clpf}$                             | $7.938 \times 10^{-3}$        |
| $G_{pd}(s)$                            | $\frac{4.264 F_{comp}^2 + 8.930 F_{comp}}{s^2 + 207.3 F_{comp} + 555 F_{comp}}$ |

Based on the above parameters, the bode plots of $T_{cr}(s)$ and $T_{cl}(s)$ are shown in Fig. 5. It is known that heavy or light loads $R_{cr<14>}$ only cause small difference of $T_{cr}(s)$ at low frequency due to large $C_{o<14>}$. The bandwidths of charge control loop and current loop are designed to be 100kHz and 500kHz, respectively. Both of loops have roughly 90 degree phase margin at their bandwidth frequency. Therefore, no stability problem of four charge control loops and current loop can be observed in frequency domain model.

Fig. 5. Bode Plot of Charge Control Loop, Current Loop and PLL Loop with different $F_{comp}$

Fig. 5 and Fig. 6 respectively show the bode plots of $T_{cr}(s)$ and CR expression $\frac{V_{oi}}{I_{oi}}$ with different $F_{comp}$, whose values range from 0.167$F_{ref}$ to 0.25$F_{ref}$. For simplicity, $F_c$ is used to represent $F_{comp}$ in these figures. This range is chosen by time domain experimental results that the inductor current $I_L$ would be saturated when $F_{comp} \geq 0.333 F_{ref}$, and frequency $F_{sw}$ would be unlocked during load transient when $F_{comp} \leq 0.142 F_{ref}$. In Fig. 5, the bode plots of $T_{cr}(s)$ with different values of $F_{comp}$ are hardly separated, and all $T_{cr}(s)$ have almost the same 100kHz bandwidth. This is because the $T_{cr}(s)$ in Eq. (12) decreases the gain of $T_{cr}(s)$ with the increase of $F_{comp}$. Therefore, the stability of PLL loop can be ensured with $F_{comp}$ ranged from 0.167$F_{ref}$ to 0.25$F_{ref}$. And 7dB lower low-frequency magnitude of CR in Fig. 6 indicates smaller CR in time domain [9–11].

Some time domain CR measurement results are shown in Fig. 7 and Fig. 8. The values of CR and load regulation are captured by measuring relevant output ripple voltage. In Fig. 7, the CR and load regulation with different $F_{comp}$ are graphically compared. $L_{R_i}$ represents $i$ channel’s load regulation, and equals to $\frac{\Delta V_{oi,i}}{\Delta I_{oi,i}}$. While in contrast $CR_{ij}$ represents the CR appeared on $i$ channel when load transient happens in $j$ channel, and equals to $\frac{\Delta V_{ij}}{\Delta I_{oi,j}}$. When $F_{comp}$ is set to be 0.167$F_{ref}$ or 0.184$F_{ref}$, most test values of $L_{R_i}$ and $CR_{ij}$ are relatively low. But the real switching frequency $F_{sw}$ is unlock during the process of step-down of $I_{oa}$, resulting in that $V_{o<1>}$ suffers large CR, up to 0.117mV/mA. When $F_{comp}$ is set to be 0.2$F_{ref}$, 0.226$F_{ref}$ or 0.25$F_{ref}$, all $CR_{ij}$ are at very low level. Even the maximum value of $CR_{ij}$, which comes from $CR_{41}$ when $F_{comp} = 0.226F_{ref}$, is only 0.052mV/mA. Fig. 8 (a) shows the time sequence waveform of output voltages during steady and transient state with $F_{comp} = 0.2F_{ref}$. It is shown that the CR-induced shift voltages and DC error voltages in multiple loads are both negligible when compared to its output ripple voltages. And the stable inductor current $I_L$ and output voltage $V_{o<1>} \Delta v$ regulation in multi-load condition proves the good function and effectiveness of GACP. Fig. 8 (b) describes the real switching frequency $F_{sw}$ during load step-up. Before inductor current $I_L$ raises to the aim value, $F_{sw}$’s phase becomes slightly more laggard than $F_{ref}$’s, but its frequency still keep the same, which would not cause EMI problem to the DC outputs. The transient response time is about 22$\mu$s. It is seen that the states of $F_{sw}$ and values of CR also verify the accuracy of above small signal modelling.

The properties of proposed SIMO Buck DC-DC are concluded in Table 2. It is shown that the proposed PLL-based charge control scheme could achieve 0.038mV/mA CR, 43.2% smaller than that of [4] during the same 150mA
4. Conclusion

A PLL-based charge control scheme for SIMO Buck DC-DC is introduced in this paper. By utilizing charge control loop to each channel, the controller regulates all DC outputs independently to well suppress CR, and constructs a full PLL structure together with power stage. GACP compensates gain of PLL loop in multi-load condition. And small signal modelling of this control scheme is proven to be helpful to the analysis and design of multi-loop stability and CR performance.

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**Table II. The Properties of Proposed SIMO and Comparison**

| Platform | APEC 2008 [3] | ISSCC 2012 [4] | TPE 2018 [2] | This work |
|----------|---------------|----------------|---------------|-----------|
| Type     | FPGA          | 65nm           | 0.18µm        | Simulink  |
| Frequency| 0.5MHz        | 1.2MHz         | 1MHz          | 1MHz      |
| Outputs&Power Switches | 2&4           | 5&8            | 5&7           | 4&6       |
| Control Scheme | Charge        | Charge         | Charge        | Charge, PLL-based |
| Load Range | CCM/DCM accessible | CCM/DCM accessible | CCM accessible | CCM accessible |
| Freewheel | No            | Yes            | No            | No        |
| Worst CR and Transient Condition | 0.35mV/mA @1A in ch. 2 | 0.067mV/mA @150mA in ch. 1 | 0.133mV/mA @250mA in ch. 3 | 0.052mV/mA @384mA in ch. 1 | 0.038mV/mA @150mA in ch. 1 |

1 Continuous Conduction Mode/Discontinuous Conduction Mode
2 Through Measuring Ripple Voltage

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