SOL: Effortless Device Support for AI Frameworks without Source Code Changes

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Abstract—Modern high performance computing clusters heavily rely on accelerators to overcome the limited compute power of CPUs. These supercomputers run various applications from different domains such as simulations, numerical applications or artificial intelligence (AI). As a result, vendors need to be able to efficiently run a wide variety of workloads on their hardware.

In the AI domain this is in particular exacerbated by the existence of a number of popular frameworks (e.g., PyTorch, TensorFlow, etc.) that have no common code base, and can vary in functionality. The code of these frameworks evolves quickly, making it expensive to keep up with all changes and potentially forcing developers to go through constant rounds of upstreaming.

In this paper we explore how to provide hardware support in AI frameworks without changing the framework’s source code in order to minimize maintenance overhead. We introduce SOL, an AI acceleration middleware that provides a hardware abstraction layer that allows us to transparently support heterogenous hardware. As a proof of concept, we implemented SOL for PyTorch with three backends: CPUs, GPUs and vector processors.

Index Terms—artificial intelligence, middleware, high performance computing

I. INTRODUCTION

Artificial Intelligence (AI) has undoubtedly become one of the hottest fields in computer science today, with software and hardware vendors alike competing for a share of the big economic and scientific pie.

Within this domain, PyTorch and TensorFlow have surfaced as the most widely used AI frameworks today [1], to the point that hardware vendors are required to support at least one of these in order to get any kind of user adoption. These frameworks are open source projects with large communities, fastly evolving, requiring constant maintenance and code up-streaming. Because this is a tedious and time consuming task that needs to be repeated for every release of the framework, it has become common practise to branch the framework, add hardware device support for it, and then publish the result as a separate installation package [2]–[4]. This makes the life of the vendor much easier, but puts the maintenance burden on the user, who needs to maintain different installations or Docker images of the same framework for different devices. Worse, it prevents users from being able to mix devices from different vendors in their AI applications.

In this paper we introduce SOL, a middleware that provides a hardware abstraction layer that allows to simultaneously support different hardware devices on a range of standard AI frameworks without requiring changes to the frameworks themselves. In fact, data scientists need only to add a few lines of code to their scripts in order to enable SOL and its hardware support.

We explore two strategies to integrate new devices into AI frameworks using SOL as a middleware, to keep the original AI framework unchanged and still add support to new device types. The first strategy hides the entire offloading procedure from the framework, and the second only injects the necessary functionality into the framework to enable the execution, but does so without changing any PyTorch code.

In short, our contributions are:

- The design and implementation of SOL, a framework for transparently adding heterogenous hardware device support to popular AI frameworks.
- The implementation and evaluation of two methods to integrate device support into AI frameworks without changing the framework’s source code.
- An asynchronous execution design for device memory allocations.
- An evaluation of SOL on PyTorch using CPUs, GPUs and vector processor (NEC’s SX-Aurora Tsubasa).

We show that SOL enables to add device support to AI frameworks with at max 3.000 lines of code per device backend and 2.400 lines per AI framework. Further, because of the optimizing methods within SOL we achieve to accelerate workloads up to (Inference/Training) 7.79x/2.41x (CPU), 4.37x/1.22x (GPU) and 25.41x/4.18x (NEC SX-Aurora) compared to the reference implementations within the AI frameworks.

II. BACKGROUND ON NEURAL NETWORK PROCESSING

In this section we give an overview of existing AI frameworks, DNN optimization libraries, and optimizing compiler/middleware.

A. AI Frameworks

The landscape of AI frameworks is rather vast, with Torch [5] and Theano [6] being among the first popular frameworks. Facebook took over the principles of Torch and switched its interface from Lua to Python, introducing...
PyTorch [7] and making it to one of the most widely used frameworks today. PyTorch features a dynamic execution graph, making it very flexible and easy to program. Google’s TensorFlow [8] is the biggest competitor to PyTorch and uses a static execution graph (though it was recently extended to also allow for dynamic graphs). There are also other frameworks such as Chainer [9], MxNet [10], and CNTK [11], but their user base is considerably smaller than those of PyTorch and TensorFlow [1].

What these frameworks have in common is their design of their internal architecture (Fig. 1). All of these frameworks have a frontend API, usually written in, e.g., Python, C/C++ or Java, that maps onto a C-based core. This core handles all of the framework’s functionality. It manages the data on the devices and processes the computation graphs of the neural networks by issuing function calls to device specific backends. These backends either rely on hand optimized compute kernels, written specifically for the framework, or on vendor specific libraries, which we further explain in the next subsection.

The major problem for hardware vendors is, that there is no standard for these device backends, making it necessary to write separate code for each framework. DLPack [12] is an approach for sharing data between deep learning frameworks, but it did not get widely adopted. ONNX Runtime [13] and ONNXifi [14] aim to create device independent inference platforms by keeping the device layer outside the framework. Regarding training, to the best of our knowledge there is no existing work that abstracts the device layer from the frameworks.

B. Optimized DNN Libraries

As NNs are very compute intensive, hardware vendors provide hand optimized libraries to accelerate such workloads on their hardware: Intel provides DNNL [15] for their CPUs and GPUs, NVIDIA provides CUDNN [16], AMD provides ROCm MIOpen [17], ARM provides ARMCL [18] and NEC provides VEDNN [19]. These libraries all come with similar functionality, although ARMCL only supports functions for inference. Aside from this, NNPACK [20] provides functions for X86 and ARM64 CPUs, although its performance is no longer competitive with respect to DNNL or ARMCL. All AI frameworks usually rely on these libraries in order to leverage their superior compute performance. Although the hyper parameters of NN layers are well defined, the APIs of these libraries are not, making it necessary to write separate code for each of these libraries.

C. Optimizing Compilers and Middleware

TVM [21] is an optimizing compiler architecture with a large open source community and probably the highest number of supported hardware architectures. It features integration for TensorFlow and PyTorch, but so far only supports inference workloads (their high level IR “Relay” already supports training but not the lower level implementations). One disadvantage of TVM for now is the very long auto-tuning – which can be up to several days, depending on the NN structure and used hardware – needed to reach good performance. Resnet-18 – a rather small network – requires already 4h on an NVIDIA 1080 TI [22]. Intel’s OpenVino [23] is a similar tool, targeting mainly Intel CPUs, Movidius VPUs or Intel GPUs. NVIDIA provides TensorRT [24], which is a similar but closed source tool, to deploy NNs for NVIDIA hardware.

For PyTorch, AMD chose to write scripts that “hipify” (rewrite) the PyTorch source code, replacing all CUDA calls with HIP calls – as they are syntactically identical – and then having their devices pose as CUDA ones within PyTorch. However, this is only possible because they have spent considerable effort mimicking the CUDA API and all of its libraries (i.e., CUBLAS, CUSOLVER, etc.) [25].

PlaidML [26] and Tensor Comprehensions [27] are both compilers that use low level mathematical formulations rather than entire layers, and transform these into specialized implementations for multiple hardware architectures. These also require extensive auto-tuning to reach performance comparable to hand-optimized libraries.

Brainslug [28] was introduced by NEC as a framework to accelerate workloads within AI frameworks using the depth first parallelism method. It became the foundation of SOL’s code optimization (see Sec. III for more details). Aside from optimizing AI framework workloads, SOL also can extract NNs from the frameworks and deploy in minimalistic libraries, removing all framework dependencies, enabling to integrate these into user applications for inference workloads. NGRAPH [29] is a similar effort maintained by Intel. It is mainly based on PlaidML to provide support for Intel CPU+GPU, NVIDIA GPUs and AMD GPUs.

All of these approaches rely on similar optimizations ranging from high level graph transformations, mathematical and algorithmic optimizations, down to low level instruction optimizations that target specialized hardware through the use of hand-optimized libraries for work-intensive operations.

In all, we are not aware of any work able to add heterogenous device support to existing AI frameworks without changing their code base.

Beside these commonalities SOL targets some of the issues of modern AI frameworks brought up by Barham and Isard [30]. They criticize that depending on the pass of the model execution, different memory layouts could be optimal. SOL weights up if using the same layout in forward and backward pass is faster than using separate layouts, including the necessary data transformations. Further, SOL also allows to use different implementations for forward and backward pass, i.e., to use OpenBLAS for forward and DNNL for backward computations. Barham and Isard mention that AI frameworks address the dimensions of a tensor by its numeric value. SOL instead uses identifiers containing the purpose (None, Channel, Pixel) and a dimension. A tensor in NCHW format has the dimensions \([N, C, P, D]\) or \([N, P, C, D]\) in NHWC format. This enables SOL to make it easy to implement layers independent of the used memory layouts, i.e., by automatically selecting all channel dimensions for
Listing 1: Full code example for using SOL within PyTorch.

Line 5 optimizes the model, line 6 copies the parameters from `py_model` to `sol_model` and line 7 runs the optimized model.

```python
1 import torch
2 import sol.pytorch as sol
3 py_model = initPyTorchModel()
4 data = initInputData()
5 sol_model = sol.optimize(py_model, data.size())
6 sol_model.load_state_dict(py_model.state_dict())
7 output = sol_model(data)
```

The SOL runtime component connects the kernels with the framework’s memory allocation system; this makes it

dependent of how many there are. On top, SOL’s code generator automatically determines necessary
nested loops and how to map these onto the SIMD architecture of the hardware. More details about this can be found in the
following section.

III. SOL DESIGN AND IMPLEMENTATION

SOL is an optimizing middleware for inference and training that transparently integrates into existing AI frameworks (e.g.,
PyTorch or TensorFlow). It was designed to have a very small
programming footprint towards user; a data scientist only
needs to add a few lines of code to enable SOL (see Listing 1).

Beyond transparency, SOL was explicitly designed to sup-
port multiple AI frameworks (so called frontends) and hard-
ware devices (backends), including X86 and ARM64 CPUs,
NVIDIA GPUs and the NEC SX-Aurora vector processor. The
core of it targets SIMD architectures in order to leverage com-
mon features across all of these hardware architectures within
the same code base. This allows us to write and maintain very
small device backends (Figure 2 gives an overview of currently
implemented modules).

In short, SOL consists of two main components, the com-
piler and the runtime. We describe each of these in turn next.

A. SOL Compiler

The compiler is triggered by the call to
`sol.optimize(...)`, which extracts the computation
graph from the framework and translates it into SOL’s own
graph intermediate representation (IR). First, SOL analyzes
this graph and applies general mathematic optimizations,
i.e., a ReLU \( y = \max(x, 0) \) followed or proceeded by
a MaxPooling can be removed from the graph when the
minimum value of the Pooling gets set to 0. In other cases
the order of layers can be switched without changing the
mathematics, which can result in better data reuse.

After these initial high level optimizations, the IR gets
cloned for each device type in order to apply device-specific
optimizations. First, we determine which optimizing method
to apply to which layer. For now, we make this purely
heuristically, where all layers except Convolutions and Linears
get implemented using the Depth First Parallelism (DFP)
module [28]. The main idea of DFP is to process computa-
tion graphs in depth first order, to keep data as long as possible
in a processor’s registers and caches; to achieve this the
DFP modules applies loop-transformation and fusion methods.
The insight behind the DFP principle is to generate code
that minimizes the number of nested loops while efficiently
mapping these onto the SIMD architecture of the hardware.
The DFP module can handle arbitrary SIMD architectures
from very short AVX instructions to very long SX-Aurora
vectors, and it is also able to make use of features such as
Shared Memory and SIMD-groups (warps).

Convolution and Linear layers get implemented with the
Deep Neural Network (DNN) module, which maps these layers
onto external libraries, such as CUDNN or DNNL. There is
one exception: if the Convolution is grouped and has as many
groups as output channels (e.g., in MobileNet) they get also
implemented using the DFP module, as this boils down to a
WeightedPooling layer that can make use of the depth first
processing.

SOL further determines optimal memory layouts for the
given data (e.g., DNNL prefers blocked memory layouts) and
takes care that data are always given in the optimal layout
to the layers, while trying to minimize the number of reorder
operations. For example, it turns out that for the Linear layer
untransposed weights (Output/Input Channels) work best for
CPUs while (Input/Output Channels) is faster on the NEC SX-
Aurora.

In case we have multiple libraries or algorithms or lay-
outs available to implement one of these layers, we either
use heuristics or run a very short auto-tuning workload to
determine the best combination given the layer’s hyperpara-
eters. SOL can mix the usage of different implementations,

algorithms and layouts between forward and backward pass
to achieve higher performance.

After all layers have been assigned to an optimizing module,
SOL generates code for these and compiles it for the target
devices. This entire optimization procedure requires usually
less than 1 min (including the auto-tuning) and only needs to
be repeated if the input size of the network or its structure
change. After compilation, SOL injects a custom model into
the AI framework so that the user can use it the same way he
would use a native model, with the difference that the SOL
model internally calls the optimized implementation when
executed (see Listing 2).

B. SOL Runtime

The SOL runtime component connects the kernels with
the framework’s memory allocation system; this makes it
possible to directly read and write into the framework’s tensors without the need to copy between the framework’s and SOL’s memory space. Further, AI frameworks usually pre-allocate device memory to speed up allocations, which would limit the opportunity to maintain a separate memory space. Further, the runtime component is responsible for loading the optimized kernel functions, maintaining all communications between SOL, the framework and the devices’ APIs.

C. SOL Deployment

Deployment is a special mode of the SOL compiler, that extracts the neural network from AI frameworks to deploy it into a library that can be integrated into a user application, similar to TVM, TensorRT or OpenVino. This specialized NN library does not have any dependencies of the AI framework or SOL, only when specialized functions are used from libraries such as DNNL or CUDNN.

IV. SOL DEVICE BACKENDS

SOL device backends are very compact and easy to maintain. Each device relies on one or multiple functional-backends that implement the functionality for the DFP and DNN modules.

The DFP backends use a code generator that outputs standard C++ code. Only a few function calls need to be overwritten to add device-specific “flavours” to the generated code. Within the DFP generated code we use functions (i.e., sol_ispc_exp) that map onto device specific implementations. In most cases this is just a #define sol_ispc_exp(A) exp(A) but also can contain specialized implementations, in case the device does not have specific instructions for the given function. Listing 3 shows how an AveragePooling layer is described within the DFP module and how it is translated into code for the different device backends.

The DNN backends only provide minimal functionality to initialize the libraries descriptors and the ability to call the necessary library functions. The descriptors get initialized once when the neural network gets loaded and cached, to decrease time during model execution. Further, the backends can implement specialized auto-tuning functions to determine optimal algorithms or memory layouts at compile time.

On top of these modules, the device backend can determine if the main thread shall run on the host system or the device.

This can reduce communication overhead between host and device, if the devices supports this implementation.

In the rest of the section we describe the implementation of SOL’s backends for CPU, GPU and the SX-Aurora.

A. X86 and ARM64 Backend

The backends for X86 and ARM64 both rely on the ISPC [31] compiler for the DFP generated code, as it allows to write very efficient vectorizable code. As shown in Listing 3 the syntax of ISPC varies from standard C++ by keywords

Listing 2: Example of how SOL integrates its custom models into PyTorch.

```python
class SolModel(torch.nn.Module):
    def __init__(self):
        self.param_0 = ... # managed by framework
        self.param_1 = ... # managed by framework
    def forward(self, input):
        return sol.call(...) # executed by SOL
```

Listing 3: Example of an AveragePooling layer in DFP description and how it is translated to the different backends.

```c
// DFP: AveragePooling
auto I = layer(l=src()), O = layer(l);
auto K = kernel(l);
loop(); O += I[K];
loop(); O /= K.area(p->isCountPadding());

// Reference: standard C++
void kernel(const float* L0, float* L1) {
    for(int OC0x = 0; OC0x < 512; OC0x++)
        for(int OP1 = 0; OP1 < 128; OP1++)
            for(int OP0 = 0; OP0 < 128; OP0++)
                float L1_s = 0;
    for(int K1 = 0; K1 < 3; K1++)
        for(int K2 = 0; K2 < 3; K2++)
            L1_s += L0[OC0x * 16384 + (OP1 + K1) * 128 + (OP0 + K0)];
    L1[OC0x * 16384 + OP1 * 128 + OP0] = L1_s / 9;
}

// Backend-ISPC: X86 and ARM64
__global__ void kernel(const uniform float* L0, uniform float* L1) {
    uniform int OC0x = taskIndex;
    foreach(OP1 = 0 ... 128, OP0 = 0 ... 128) {
        float L1_s = 0;
    }
    for(uniform int K1 = 0; K1 < 3; K1++)
        for(uniform int K2 = 0; K2 < 3; K2++)
            L1_s += L0[OC0x * 16384 + (OP1 + K1) * 128 + (OP0 + K0)];
    L1[OC0x * 16384 + OP1 * 128 + OP0] = L1_s / 9;

// Backend-CUDA: NVIDIA
__global__ void kernel(const float* L0, float* L1) {
    int OC0x = blockIdx.x;
    foreach(OP0x = threadIdx.x; i < 16384; i += blockDim.x) {
        int OP0 = OP0x / 128, OP0 = OP0x % 128;
        float L1_s = 0;
    }
    for(int K1 = 0; K1 < 3; K1++)
        for(int K2 = 0; K2 < 3; K2++)
            L1_s += L0[OC0x * 16384 + (OP1 + K1) * 128 + (OP0 + K0)];
    L1[OC0x * 16384 + OP0x] = L1_s / 9;

// Backend-NCC: SX-Aurora
void kernel(const float* L0, float* L1) {
    #pragma omp parallel for collapse(2)
    for(int OC0x = 0; OC0x < 512; OC0x++)
        foreach(int OP0x = 0 ... 16384) {
            float L1_s = 0;
        }
        for(int K1 = 0; K1 < 3; K1++)
            for(int K2 = 0; K2 < 3; K2++)
                L1_s += L0[OC0x * 16384 + (OP1 + K1) * 128 + (OP0 + K0)];
    L1[OC0x * 16384 + OP0x] = L1_s / 9;
}
```
such as `uniform` (identifying a scalar variable) and `foreach` (identifying a vectorized loop), but most of the structure is identical to writing this in standard C++. For the DNN module, SOL’s CPU backends supports OpenBLAS, DNNL (only x86) and NNPACK.

B. NVIDIA Backend

The NVIDIA backend bears a close resemblance to the CPU one, except that it relies on CUDA for the DFP module and CUBLAS and CUDNN for the DNN module. Again Listing 3 shows the differences. On top of the CPU backend, it supports to use SIMD vector groups, which means that instead of using the full vector length and sharing data using shared memory between the different warp, SOL uses only the warp for vectorization. This allows to run multiple warps in parallel, on different parts of the data, which improves performance in situations where the available loops do not allow to leverage the combined SIMD processing of all warps. For DNN we use the NVIDIA provided libraries CUDNN and CUBLAS.

C. SX-Aurora Backend

The NEC SX-Aurora Tsubasa is a vector processor PCIe card. The SX-Aurora was not specifically designed for NN processing, but for more traditional high performance computing (HPC) applications, such as numerical simulations. As a result, it lacks AI-specific functionality such as tensor cores and float16 support. However, HPC clusters today need to run various kinds of workloads including AI. To solve this, we implement an SX-Aurora SOL device backend to transparently enable AI on this accelerator.

Developing the SX-Aurora backend for SOL was straightforward, as the accompanying NCC compiler supports the C++14 standard and only requires very few pragmas to be told which loop to vectorize. The DFP module is fairly slim, and uses knowledge of vector lengths to ensure that vector instructions are not underutilized.

For the DNN module we use the VEDNN library [19] that was originally implemented for the TensorFlow-VE [4] project. It contains optimized implementations for Convolution, Linear, MaxPooling, SoftMax and Activation layers, but we only use the Convolution and Linear implementations within SOL. Additionally we use the SX-Aurora BLAS library as a secondary implementation for Linear layers. For both libraries we use modified OpenMP implementations for task parallelism, as the default implementations weakly scale.

As SOL and the AI frameworks are running on the host system, we use the VEOoffload [32] library to launch our kernel functions on the Aurora. It features a CUDA API-like programming model to asynchronously offload kernels onto the device. However, it has latency issues because the execution queue is operated by the host system. To address this, we build a specialized asynchronous execution queue on top of the library specialized for the needs of SOL. Our design mainly mimics the principles of CUDA streams, but extends it with asynchronous malloc and free. As this does not directly allocate memory immediately, we instead return a 64-bit integer, where the first 32 bits contain a unique reference number and the second 32 bits can be used to offset the pointer. This allows us to use this virtual pointer with normal pointer arithmetics and removes the need to synchronize malloc and free operations, increasing the asynchrony of the processing.

As a final optimization, we gather multiple adjacent memcopies and group them together within our asynchronous execution queue. If only a small number of small tensors need to be transferred, we use the latency-optimized VEOoffload memcopy methods. Otherwise, we use the peak bandwidth optimized VEO-uda [33] library, which supports packed memcopies so that many small tensors can be packed into a big data segment to speed up transfers.

V. PyTorch Frontend

To integrate SOL into AI frameworks we use so called frontends. For the PyTorch frontend, we developed two strategies: transparent offloading, as it seamlessly integrates into the framework with only a minimal interaction between PyTorch and the device backends; and native offloading which requires much tighter integration with the framework, but yields higher performance during training.

A. Transparent Offloading

The idea behind transparent offloading is to add device support to the framework with as minimal effort as possible. We took TensorFlow’s Keras API as inspiration, as it exposes two functions `model.predict()` and `model.fit()` for prediction and training to the user, both of which consume Numpy arrays located on the host system as input so the user does not need to care about where the model is actually run.

Normally when a model is executed, SOL checks on which device the input data is located and executes all computations on that device. To enable transparent offloading computations the user just needs to call `sol.device.set(DEVICE, DEVICE_IDX) once prior executing the model. The next time a model gets executed SOL recognizes that the data is located on the host, but that the user requests to execute on another device. SOL then will ensure that the necessary data is copied to the device and will execute the model on it instead.

SOL injects its model into PyTorch’s execution environment as a custom layer (shown in Listing 2). This keeps the model parameters inside PyTorch, so that SOL can leverage all available learning methods without the need to implement these itself, and only execute the compute intensive calculations within SOL.

One problem are the model parameters. As these are needed on the device, it would be necessary to either copy them every time a model gets executed or to cache these on the device. We chose the latter. When the model gets run for the first time, we create a specialized offloading context that contains copies of all model parameters. As long as the model parameters do not get modified or the model gets destroyed, this context is kept alive to prevent continuous memcopies between the host and the device, limiting memcopies between host and device to just the input and output data.
While this works pretty well for inference, it is inefficient for training where the model changes in each epoch; this means that we not only need to retransfer the updated weights in each epoch but also to transfer all gradients from the device to the host after the backward pass, as the gradient upgrade is processed on the host system.

An obvious solution would be to implement the parameter management and learning methods also within SOL. However, these features have different implementations across AI frameworks, so portability is far from guaranteed. As a result, we decided to explore tighter integration with the framework.

B. Native Offloading

Support for X86, ARM64 and NVIDIA GPUs is already available in most AI frameworks, which allows SOL to directly connect to their public API to have access to all of the necessary framework functionality and to share the memory space on the device with the framework.

The SX-Aurora is not supported by these frameworks. AI frameworks such as PyTorch and TensorFlow are built for multi-device support in mind and, consequently, both of them support registering function callbacks for a specific device. As these frameworks target extensibility, these callback registrations are exposed to other libraries. We were interested to see if it would be possible to integrate all the necessary operations into PyTorch without even changing a single line of code, which would allow us to extend PyTorch without initializing a tedious upstreaming and maintenance process. In principle we want to be able to replace the entire lower device layer implementation of PyTorch for the SX-Aurora with SOL. In the following we will reference source code files which refer to the PyTorch source code located at github.com/pytorch/pytorch for version 1.4.0.

First we analyzed how PyTorch distinguishes devices. Unfortunately they use a fixed enum (c10/core/DeviceType.h), which cannot be extended from the outside, so we decided to just take one of the existing devices (OpenCL, XLA or HIP), as in the default installation package, only CPU and CUDA are used. The c10::RegisterOperators class enables us to register the necessary callbacks for devices within the device enum, as shown in Listing 4.

However, digging further through the source code reveals that some functions do not get registered in the c10::RegisterOperators registry, but rely on the class at::native::DispatchStub (ATen/native/DispatchSub.h) that only stores separate function pointers for CPU, CUDA and HIP (Listing 5 shows an excerpt of that class). As CPU and CUDA are already used within the default package, we chose to use HIP as our final device type.

Before the callbacks can be implemented, it is necessary to set up some basic functionality, i.e., implementing the at::HIPHooksInterface which contains methods to determine the number of available devices in the system, or the default device index. Further, it is necessary to implement

Listing 4: Example to register a method __and__ to PyTorch's callback registry.

```cpp
1 at::Tensor __and__(const at::Tensor& A, const at::Tensor& B) { ... 
2 static auto registry = c10::RegisterOperators()
3 .op(c10::RegisterOperators::options()
4 .schema("aten::__and__.Tensor(Tensor_self, Tensor_other)->Tensor")
5 .kernel(at::Tensor(const at::Tensor& A, const at::Tensor& B)>(TENSOR_TYPE_ID, &__and__)
6 .aliasAnalysis(c10::AliasAnalysisKind::FROM_SCHEMA))
```

Listing 5: PyTorch's DispatchStub that only supports CPU, CUDA and HIP functions.

```cpp
1 template <typename rT, typename T, typename... Args>
2 struct DispatchStub<rT (*)(Args...), T> {
3   FnPtr cpu_dispatch_ptr;
4   FnPtr cuda_dispatch_ptr;
5   FnPtr hip_dispatch_ptr;
6   // ...
7   
8   
9   
```

V. EVALUATION

We evaluate SOL under the aspect of how much effort it took to support the different processor architectures and how good performs SOL compared to the standard AI frameworks.

A. Programming effort

SOL was designed with extendibility and maintainability in mind. To add a new layer to SOL only the layer description needs to be added to the high level IR and to either implement it using the DFP or DNN module. All DFP layers are automatically available for all devices due to the code generation engine, while for the DNN module suitable glue code between SOL and the external libraries is required.

Our X86 backend requires about 3.000 lines of code. For ARM64 we only require 300 additional lines as it inherits most of its functionality from the X86 backend. The NVIDIA GPU backend requires about 2.400 lines of code, while the NEC SX-Aurora about 2.200 lines of code, plus 800 lines dedicated to the kernels required for the native tensor integration. We
TABLE I: Hardware devices used in our evaluation.

| Vendor | Model                  | Type | TFLOPs   | Bandwidth(GB/s) |
|--------|------------------------|------|----------|-----------------|
| Intel  | Xeon Gold 6126         | CPU  | 0.88     | 119.21          |
| NEC    | SX-Aurora VE10B        | VPU  | 4.30     | 1200.00         |
| NVIDIA | Quadro P4000           | GPU  | 5.30     | 243.30          |
| NVIDIA | Titan V                | GPU  | 14.90    | 651.30          |

conclude that adding a device to SOL requires at max 3,000 lines of code. In comparison, we identified 26,000 lines for CPU and over 47,000 lines of code solely dedicated to NVIDIA GPUs within PyTorch.

The frontend integration into PyTorch is about 1.200 lines of code for extracting the neural network, injecting the SOL optimized model and to hook up to the X86 and NVIDIA memory allocators to share the memory space with PyTorch. The native tensor integration of the SX-Aurora required another 1.200 lines. In total this is a rather small effort to do. It took a single programmer about 2 weeks to identify all entry points and implement the required callbacks and kernel functions.

B. Performance

To evaluate the performance of SOL we ran tests for inference and for training on an Intel Xeon 6126, an NEC SX-Aurora Tsubasa, an NVIDIA mid-range Quadro P4000 and high-end Titan V (see Table I for specs).

We used PyTorch 1.4.0 as baseline for the CPU and GPUs. As the SX-Aurora is not supported by PyTorch we used TensorFlow-VE 2.1 instead. The reference software was installed using the official unmodified pip packages. In the following we call the native execution model as SOL and the transparent offloading as SOL (TO).

As SOL currently supports CNN and MLP networks, we ran popular NN architectures from these domains. While SOL has been tested with all models from the TorchVision [34] package due to space reasons we only report results from Densenet, Resnet, SqueezeNet, VGG, ShuffleNet v2, and MNASNet (two versions each) and a 3-layer MLP with 8192 features and a ReLU activation functions. ShuffleNet is not supported by TensorFlow-VE 2.1 as it does not support 5D permutations. The CNN’s input data is a tensor with the dimensions $[B, 3, 224, 224]$ where $B$ stands for the batchsize. We repeated every experiment 100 times.

C. Inference

We start our performance evaluation with inference. The models are run with $B = 1$. For the CPU we can see that SOL is able to speed up the CNN models significantly compared to the reference within PyTorch. For the MLP there is no difference visible. MLPs do not provide optimization capabilities to SOL as it mainly relies on matrix multiplications. In the SX-Aurora chart we can see that TF-VE is always significantly slower than SOL. This is due to the VEDNN library, that only parallelizes over the batch elements, so that only 1 out of 8 SX-Aurora cores is active. SOL uses a modified version of VEDNN with a different, OpenMP-based parallelization to overcome these problems. Further there is no difference to be seen between the transparent and native offloading model, as the data needed to be copied in inference is too small to make an actual difference. In the GPU cases we can see, that SOL outperforms PyTorch especially in DenseNet, SqueezeNet and ShuffleNet. Overall SOL is always faster than the baseline implementations in the inference tests, on all devices.

D. Training

For evaluating the CNNs we use $B = 16$ and for the MLP $B = 64$. The results are shown in Fig. 3. As before, for the CPU SOL is always faster, especially in DenseNet where the execution time is more than halved. For the SX-Aurora we see that TF-VE is always slowest except for the MNASNet. We identified that SOL’s code generated for the grouped convolutions is slower than the implementation within VEDNN, which are used in TF-VE. For the other networks SOL outperforms TF-VE with both execution modes, while as expected, the native offloading always yields in higher performance, because of less memcpy between the host and the device. The GPU performance gain of SOL is not as high as for the inference cases, but still never slower than PyTorch.

VII. CONCLUSION

In this paper we introduced SOL, an AI workload middleware that makes it relatively easy to add support for a wide range of heterogenous hardware devices to existing AI frameworks such as PyTorch and TensorFlow. SOL’s device backends add such support without having to modify the actual framework’s code, avoiding any upstreaming and maintenance hassles. As a proof of concept, we implemented SOL along with a PyTorch frontend and backends for CPU, GPU and a vector processor, and showed an extensive evalation of SOL when running both inference and training workloads.

As future work we intend to add native tensor support for non-supported devices to our other frontends (i.e. TensorFlow). In addition, we are looking into supporting other kinds of networks such as transformers and RNNs.

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Fig. 3: Left: Inference (B = 1) performance for all tested NNs and processors. Right: training (B = 16 for CNNs and B = 64 for MLP) performance. Results are reported as execution time in milliseconds.

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