Optimizing the performance of streaming numerical kernels on the IBM Blue Gene/P PowerPC 450 processor

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Abstract
Several emerging petascale architectures use energy-efficient processors with vectorized computational units and in-order thread processing. On these architectures the sustained performance of streaming numerical kernels, ubiquitous in the solution of partial differential equations, represents a challenge despite the regularity of memory access. Sophisticated optimization techniques are required to fully utilize the CPU. We propose a new method for constructing streaming numerical kernels using a high-level assembly synthesis and optimization framework. We describe an implementation of this method in Python targeting the IBM Blue Gene/P supercomputer’s PowerPC 450 core. This paper details the high-level design, construction, simulation, verification, and analysis of these kernels utilizing a subset of the CPU’s instruction set. We demonstrate the effectiveness of our approach by implementing several three-dimensional stencil kernels over a variety of cached memory scenarios and analyzing the mechanically scheduled variants, including a 27-point stencil achieving a 1.7× speedup over the best previously published results.

Keywords
high-performance computing, performance optimization, code generation, SIMD, Blue Gene/P

1 Introduction
1.1 Motivation
As computational science soars past the petascale to exascale, a large number of applications continue to achieve disappointingly small fractions of the sustained performance capability of emerging architectures. In many cases this shortcoming in performance stems from issues at the single processor or thread level. The ‘many-core’ revolution brings simpler, slower, more power-efficient cores with vectorized floating point units in large numbers to a single processor. Performance improvements on such systems should be multiplicative with improvements derived from processor scaling.

The characteristics of Blue Gene/P that motivate this work will persist in the processor cores of exascale systems, as one of the fundamental challenges of the exascale relative to petascale is electrical power (Dongarra et al., 2011; Keyes, 2011). An optimistic benchmark (goal) for a petascale system is the continuous consumption of about a megawatt of electrical power, which represents the average continuous power consumption of roughly 1,000 people in an OECD country (1.4 kW per person). Power reductions relative to delivered flop/s of factors of one to two orders of magnitude are expected en route to the exascale, which means more threads instead of faster-executing threads, power growing roughly as the cube of the clock frequency (Kogge et al., 2008). It also means much less memory and memory bandwidth per thread because the movement of data over copper interconnects consumes much more power than the operations on data in registers. Mathematical formulations of problems and algorithms to implement them will be rewritten to increase arithmetic intensity in order to avoid data movement. Implementations in hardware will have to be made without some of today’s popular power-intensive performance optimizations.

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At each stage of such a design, tradeoffs are made that complicate performance optimization for the compiler and programmer in exchange for improved power and die efficiency from the hardware. For example, out-of-order execution logic allows a microprocessor to reorder instruction execution on the fly to avoid pipeline and data hazards. When out-of-order logic is removed to save silicon and power, the responsibility for avoiding these hazards is returned to the compiler and programmer. In the same vein, a wide vector processing unit can significantly augment the floating point performance capabilities of a processing core at the expense of the efficient single-element mappings between input and output in scalar algorithms. Such vector units also incur greater bandwidth demands for a given level of performance, as measured by percentage of theoretical peak. Graphics processing units (GPUs) provide a set of compute semantics similar to a traditional Single Instruction Multiple Data (SIMD) vector processing unit with Single Instruction Multiple Thread (SIMT), but still execute in-order and require vectorized instruction interlacing to achieve optimal performance. We observe a broad trend to improve efficiency of performance with wider vector units and in-order execution units in the architectures of the IBM Blue Gene/P PowerPC 450 (Sosa and International Business Machines Corporation, 2008), the Cell Broadband Engine Architecture (Pham et al., 2006), Intel’s MIC architecture (Seiler et al., 2008), and NVIDIA’s Tesla GPU (Lindholm et al., 2008).

In general terms, we may expect less memory per thread, less memory bandwidth per thread, and more threads per fixed data set size, creating an emphasis on strong scaling within a shared-memory unit. We also foresee larger grain sizes of SIMDization and high penalization of reads and writes from main memory as we move towards exascale.

### 1.2 Background

We define streaming numerical kernels as small, cycle-intensive regions of a program where, for a given $n$ bytes of data accessed in a sequential fashion, $O(n)$ computational operations are required. Streaming numerical kernels are generally considered to be memory-bandwidth bound on most common architectures due to their low arithmetic intensity. The actual performance picture is substantially more complicated on high-performance computing microprocessors, with constraints on computational performance stemming from such disparate sources as software limitations in the expressiveness of standard C and Fortran when targeting SIMD processors and a host of hardware bottlenecks and constraints, from the number of available floating point registers, to the available instructions for streaming memory into SIMD registers, to the latency and throughput of buses between the multiple levels of the memory hierarchy.

In this paper we focus upon stencil operators, a subset of streaming kernels that define computations performed over a local neighborhood of points in a spatial multi-dimensional grid. Stencil operators are commonly found in partial differential equation solver codes in the role of finite-difference discretizations of continuous differential operators. Perhaps the most well-known of these is the 7-point stencil, which usually arises as a finite difference discretization of the Laplace kernel on structured grids. Although adaptive numerical methods and discretization schemes have diminished this operator’s relevance for many problems as a full-fledged numerical solver, it is still a cycle-intensive subcomponent in several important scientific applications such as Krylov iterations of Poisson terms in pressure corrections, gravitation, electrostatics, and wave propagation on uniform grids, as well as blocks in adaptive mesh refinement methods (Berger and Oliger, 1984). We also target the 7-point stencil’s ‘boxier’ cousin, the 27-point stencil. The 27-point stencil arises when cross-terms are needed such as in the NASA Advanced Supercomputing (NAS) parallel Multi Grid (MG) benchmark, which solves a Poisson problem using a V-cycle multigrid method with the stencil operator (Bailey et al., 1991). Finally, we examine the 3-point stencil, the one-dimensional analogue to the 7-point stencil and an important sub-kernel in our analysis.

We concentrate on the Blue Gene/P architecture for a number of reasons. The forward-looking design of the Blue Gene series, with its power-saving and ultra-scaling properties, exemplifies some of the characteristics that will be common in exascale systems. Indeed, its successor Blue Gene/Q now tops the GREEN500 (Feng and Cameron, 2007) list. Blue Gene/P has SIMD registers, a slow clock rate (850 MHz), an in-order, narrow superscalar execution path, and is constructed to be highly reliable and power efficient, holding 15 of the top 25 slots of the GREEN500 list as recently as November 2009. Blue Gene continues to generate cutting-edge science, as evidenced by the continued presence of Blue Gene systems as winners and finalists in the Gordon Bell competition (Ananthanarayanan et al., 2009; Ghoting and Makarychev, 2009; Richards et al., 2009).

In the work presented here our simulations and performance enhancements focus on using code synthesis and scheduling to increase arithmetic intensity with unroll-and-jam, an optimization technique that creates tiling on multiply nested loops through a two-step procedure as in Callahan et al. (1988) and Carr and Kennedy (1994). Unroll-and-jam combines two well-known techniques, loop unrolling on the outer loops to create multiple inner loops, then loop fusion, or ‘jamming’, to combine the inner loops into a single loop. Figure 1 shows an example of unroll-and-jam applied to a copy operation between two three-dimensional arrays, where each of the two outer most loops is unrolled once. This technique can work well for three-dimensional local operators because it promotes register reuse and can increase effective arithmetic intensity, although it requires careful register management and instruction scheduling to work effectively.
for i = 1 to N step 2
for j = 1 to N step 2
for k = 1 to N
    A(i,j,k) = R(i,j,k)
endfor
endfor

Figure 1. Unroll-and-jam example for a three-dimensional array copy operation.

2 Related work

Several emerging frameworks are facilitating the development of efficient high-performance code without having to go down to the assembly level, at least not directly. These frameworks are largely motivated by the difficulties involved in utilizing vectorized Floating Point Unit (FPU) and other advanced features in the processor. CorePy (Mueller and Martin, 2007), a Python implementation similar to our approach, provides a code synthesis package with an API to develop high-performance applications by utilizing the low-level features of the processor that are usually hidden by the programming languages. Intel has introduced a new dynamic compilation framework, Array Building Blocks (ArBB) (Newburn et al., 2011), which represents/enables a high-level approach to automatically using the SIMD units on Intel processors. In addition, several techniques are developed in the literature to address the alignment problems in utilizing the SIMD capabilities of modern processors. Eichenberger et al. (2004) introduced an algorithm to reorganize the data in the registers to satisfy the alignment constraints of the processor. A compilation technique for data layout transformation is proposed by Henretty et al. (2011) that reorganizes the data statically in memory for minimal alignment conflicts.

As stencil operators in particular have been identified as an important component of many scientific computing applications, a good deal of effort has been spent attempting to improve their performance through optimization techniques. Christen et al. (2009) optimized a 7-point stencil in three-dimensional grids on the CELL BE processor and a GPU system. On CELL BE, they reduced bandwidth requirements through spatial and temporal blocking. To improve the computation performance, they utilized the SIMD unit with shuffling intrinsics to handle alignment issues. They utilized optimization techniques including preloading, loop unrolling, and instruction interleaving. Rivera and Tseng (2000) utilized tiling in space to improve spatial locality and performance of stencil computations. A domainspecific technique is time skewing (Li and Song, 2004; Krishnamoorthy et al., 2007). Unfortunately, time skewing is not generalizable because no other computations between time steps are allowed to occur. Recently, Nguyen et al. (2010) optimized the performance of a 7-point stencil and a Lattice Boltzmann stencil on Central Processing Unit (CPU)s and GPUs over three-dimensional grids by performing a combination of spatial and temporal blocking, which they dubbed 3.5D blocking, to decrease the memory bandwidth requirements of their memory bound problems. Wellein et al. (2009) performed temporal blocking on the thread level to improve the performance of stencil computations on multicore architectures with shared caches. Kamil et al. (2005) conducted a study on the impact of modern memory subsystems on three-dimensional stencils and proposed two cache optimization strategies for stencil computations in Kamil et al. (2006), namely cache-oblivious and cache-aware techniques. There have been several other recent studies in performance improvements in stencil operators, including multilevel optimization techniques (Dursun et al., 2009; Peng et al., 2009).

There are several approaches to obtaining performance improvements in stencil computations that are more automated, requiring less manual intervention and resulting in more generality: Christen et al. (2011) introduced a stencil code generation and auto-tuning framework, PATUS, targeting CPUs and GPUs. Williams et al. (2008) presented an auto-tuning framework. They performed their optimization work on a Lattice Boltzmann application over several architectures. Kamil et al. (2010) built an auto-tuning framework for code generation. Their framework accepts the stencil’s kernel in Fortran and then converts it into a tuned version in Fortran, C, or Compute Unified Device Architecture (CUDA). Solar-Lezama et al. (2007) proposed a software synthesis approach to generate optimized stencil code. Machine learning strategies were proposed by Ganapathi et al. (2009) to tune the parameters of the optimization techniques for the 7- and the 27-point stencil. Recently, Tang et al. (2011) introduced the Pochoir stencil compiler. Their framework aims to simplify programming efficient stencil codes, utilizing parallel cache-oblivious algorithms.

We call special attention to a comprehensive work by Datta (2009), who constructed an auto-tuning framework to optimize the 7- and the 27-point stencils and the Gauss–Seidel red–black Helmholtz kernel. Datta’s work
was performed on diverse multicore architectures modern at the time. Datta achieved impressive performance by employing a search over a variety of algorithmic and architecture-targeting techniques including common subexpression elimination and Non-Uniform Memory Access (NUMA)-aware allocations. It is interesting to note that aside from register blocking and common subexpression elimination, Datta’s techniques were ineffective in improving the performance of stencil operators on the Blue Gene/P platform. This was attributed in part to the difficulties in achieving good performance for the in-order-execution architecture of the PowerPC 450 processor.

3 Implementation considerations

3.1 Stencil operators

A three-dimensional stencil is a linear operator on $\mathbb{R}^{MNP}$, the space of scalar fields on a Cartesian grid of dimension $M \times N \times P$. Apart from some remarks in Section 6, we assume throughout this paper that the operator does not vary with the location in the grid, as is typical for problems with regular mesh spacing and space-invariant physical properties such as constant diffusion. The input, $A$, and output, $R$, are conventionally stored in a one-dimensional array using lexicographic ordering. We choose a C-style ordering convention so that an entry $a_{i,j,k}$ of $A$ has flattened index $(iN + j)P + k$, with zero-based indexing. Further, we assume that the arrays $A$ and $R$ are aligned to 16-byte memory boundaries.

Formally, the 3-point stencil operator defines a linear mapping from a weighted sum of three consecutive elements of $A$ to one element in $R$:

$$r_{i,j,k} = w_0 \cdot a_{i,j,k-1} + w_1 \cdot a_{i,j,k} + w_2 \cdot a_{i,j,k+1}.$$

We further assume certain symmetries in the stencils that are typical of self-adjoint problems, e.g. $w_0 = w_2$. The effect of this assumption is that fewer registers are required for storing the $w$ coefficients of the operator, allowing us to unroll the problem further. This assumption is not universally applicable to numerical schemes such as upwinding, where adaptive weights are used to capture the direction of flow.

The 7-point stencil (Figure 2) defines the result at $r_{i,j,k}$ as a linear combination of the input $a_{i,j,k}$ and its six three-dimensional neighbors with Manhattan distance one. The 27-point stencil uses a linear combination of the set of 26 neighbors with Chebyshev distance one. The boundary values $r_{i,j,k}$ with $i \in \{0, M - 1\}, j \in \{0, N - 1\}$, or $k \in \{0, P - 1\}$ are not written, as is standard for Dirichlet boundary conditions. Other boundary conditions would apply a different one-sided stencil at these locations, a computationally inexpensive consideration that we do not regard for our experiments.

The 27-point stencil (Figure 3) can be seen as the summation over nine independent 3-point stencil operators into a single result. We assume symmetry along but not between the three dimensions, leading to eight unique weight coefficients. The symmetric 7-point stencil operator has four unique weight coefficients.

3.2 PowerPC 450

Designed for delivering power-efficient floating point computations, the nodes in a Blue Gene/P system are four-way Symmetric Processors (SMPs) comprising PowerPC 450 processing cores (IBM Blue Gene Team, 2008). The processing cores possess a modest superscalar architecture capable of issuing a SIMD floating point instruction in parallel with various integer and load/store instructions. Each core has an independent register file containing 32 4-byte general purpose registers and 32 16-byte SIMD floating point registers which are operated on by a pair of fused floating point units. A multiplexing unit on
each end of this chained floating point pipeline enables a rich combination of parallel, copy, and cross semantics in the SIMD floating point operation set. This flexibility in the multiplexing unit can enhance computational efficiency by replacing the need for independent copy and swap operations on the floating point registers with fused operations. To provide backward compatibility as well as some additional functionality, these 16-byte SIMD floating point registers are divided into independently addressable, 8-byte primary and secondary registers wherein non-SIMD floating point instructions operate transparently on the primary half of each SIMD register.

An individual PowerPC 450 core has its own 64 kB L1 cache, divided evenly into a 32 kB instruction cache and a 32 kB data cache. The L1 data cache uses a round-robin (First In First Out (FIFO)) replacement policy in 16 sets, each with 64-way set-associativity. Each L1 cache line is 32 bytes in size.

Every core also has its own private prefetch unit, designated as the L2 cache, ‘between’ the L1 and the L3. In the default configuration, each PowerPC 450 core can support up to five ‘deep fetching’ streams or up to seven shallower streams. These values stem from the fact that the L2 prefetch cache has 15 128-byte entries. If the system is fetching two lines ahead (settings are configured on job startup), each stream occupies three positions, one current and two ‘future’, while a shallower prefetch lowers the occupancy to two per stream. The final level of cache is the 8 MB L3, shared among the four cores. The L3 features a Least Recently Used (LRU) replacement policy, with 8-way set associativity and a 128-byte line size.

On this architecture the desired scenario in high-performance numerical codes is the dispatch of a SIMD Floating point Multiply-Add (FMA), with any load or store involving one of the floating point registers issued in parallel, as inputs are streamed in and results are streamed out. Floating point instructions can be retired one per cycle, yielding a peak computational throughput of one (SIMD) FMA per cycle, leading to a theoretical peak of 3.4 GFlops/s per core. Blue Gene/P’s floating point load instructions, whether they be SIMD or non-SIMD, can be retired every other cycle, leading to an effective read band- width to the L1 of 8 bytes a cycle for aligned 16-byte SIMD loads (non-aligned loads result in a significant performance penalty) and 4 bytes a cycle otherwise. As a consequence of the instruction costs, no kernel can achieve peak floating point performance if it requires a ratio of load to SIMD floating point instructions greater than 0.5. It is important to ensure packed ‘quad-word’ SIMD loads occur on 16-byte aligned memory boundaries on the PowerPC 450 to avoid performance penalties that ensue from the hardware interrupt that results from misaligned loads or stores.

An important consideration for achieving high-throughput performance on modern floating point units is pipeline latency, the number of cycles that must transpire between accesses to an operand being written or loaded into in order to avoid pipeline hazards (and their consequent stalls). Floating point computations on the PowerPC 450 have a latency of five cycles, whereas double-precision loads from the L1 require at least 4 cycles and those from the L2 require approximately 15 cycles (Sosa and International Business Machines Corporation, 2008). Latency measurements when fulfilling a load request from the L3 or DDR memory banks are less precise: in our performance modeling we assume an additional 50 cycle average latency penalty for all loads outside the L1 that hit in the L3.

In the event of an L1 cache miss, up to three concurrent requests for memory beyond the L1 can execute (an L1 cache miss while three requests are ‘in-flight’ will cause a stall until one of the requests to the L1 has been fulfilled). Without assistance from the L2 cache, this leads to a return of 96 bytes (three 32-byte lines) every 56 cycles (50 cycles of memory latency + 6 cycles of instruction latency), for an effective bandwidth of approximately 1.7 bytes/cycle. This architectural characteristic is important in our work, as L3-confined kernels with a limited number of streams can effectively utilize the L2 prefetch cache and realize as much as 4.7 bytes/cycle bandwidth per core, while those not so constrained will pay the indicated bandwidth penalty.

The PowerPC 450 is an in-order unit with regards to floating point instruction execution. An important consequence is that a poorly implemented instruction stream featuring many non-interleaved load/store or floating point operations will suffer from frequent structural hazard stalls with utilization of only one of the units. Conversely, this in-order nature makes the result of efforts to schedule and bundle instructions easier to understand and extend.

### 3.3 Instruction scheduling optimization

We wish to minimize the required number of cycles to execute a given code block composed of PowerPC 450 assembly instructions. This requires scheduling (reordering) the instructions of the code block to avoid the structural and data hazards described in the previous section. Although we use greedy heuristics in the current implementation of the code synthesis framework to schedule instructions, we can formulate the scheduling problem as an Integer Linear Programming (ILP) optimization problem. We base our formulation on the work of Chang et al. (1997), which considers optimizations combining register allocation and instruction scheduling of architectures with multi-issue pipelines. To account for multi-cycle instructions, we include parts of the formulation of Wilken (2000). We consider two minor extensions to these approaches. First, we consider the two separate sets of registers of the PowerPC 450, the General Purpose Registers (GPR), and the Floating Point Registers (FPR). Second, we account for instructions that use the Load Store Unit (LSU) occupying the pipeline for a varying number of cycles.

We begin by considering a code block composed of \( N \) instructions initially ordered as \( I = \{I_1, I_2, I_3, \ldots, I_N\} \). A common approach to represent the data dependencies of these instructions is to use a Directed Acyclic Graph
Given a DAG $G(V, E)$, the nodes of the graph ($V$) represent the instructions and the directed edges ($E$) represent the dependencies between them. Figure 4 shows an example of a DAG representing a sequence of instructions with the edges representing data dependencies between instructions. Each read-after-write data dependency of an instruction $i$ on an instruction $j$ is represented by a weighted edge $e_{ij}$. This weighted edge corresponds to the number of cycles needed by instruction $i$ to produce the results required by instruction $j$. The weights associated with write-after-read and write-after-write data dependencies are set to one.

The PowerPC 450 processor has one LSU and one FPU. This allows the processor to execute a maximum of one floating point operation every cycle and one load/store operation every two cycles (each operation using the LSU consumes at least two cycles). We partition each instruction into one of two tuples, $I^{LSU}$ and $I^{FPU}$, based on the operation unit it occupies. A critical path, $C$, in the DAG is a path in the graph on which the sum of the edge weights attains the maximum. We can compute a lower bound ($L_{\text{bound}}$) of cycles necessary to run the instructions $I$ as follows:

$$L_{\text{bound}}(I) = \max\{C, 2 \cdot |I^{LSU}|, |I^{FPU}|\}. \quad (1)$$

At the DAG of Figure 4, for example, we have three critical paths of length 15, $\{I_1, I_2, I_3, I_7, I_8\}$, $\{I_1, I_2, I_3, I_5, I_6\}$, and $\{I_1, I_2, I_4, I_5, I_6\}$. The instructions of this example are partitioned into two tuples, $I^{FPU} : \{I_3, I_5, I_7\}$ and $I^{LSU} : \{I_1, I_2, I_4, I_6\}$.

We can compute an upper bound $U_{\text{bound}}(I)$ by simulating the number of cycles to execute the scheduled instructions. If $U_{\text{bound}}(I) = L_{\text{bound}}(I)$, the schedule is optimal.

We constrain the Boolean optimization variables $x_{ij}^k$ to take the value 1 when instruction $i$ is scheduled to execute at cycle $c_j$ and 0 otherwise. These variables are represented in the matrix shown in Figure 5, where $M$ represents the total number of the cycles.

The first constraint in our optimization is to force each instruction to be scheduled only once in the code block. Formally

$$\sum_{j=1}^{M} x_{ij}^k = 1, \forall i \in \{1, 2, \ldots, N\}. \quad (2)$$

The PowerPC 450 processor can execute a maximum of one floating point operation every cycle and one load operation every two cycles (store instructions are more complicated, but for this derivation we assume two cycles as well). This imposes the following constraints:

$$\sum_{i:j \in I^{FPU}} x_{ij}^k \leq 1, \forall j \in \{1, 2, \ldots, M\}, \quad (3)$$

$$\sum_{i:j \in I^{LSU}} (x_{ij}^k + x_{ij}^{k+1}) \leq 1, \forall j \in \{1, 2, \ldots, M - 1\}. \quad (4)$$

Finally, to maintain the correctness of the code’s results we enforce read-after-write data dependency constraints:

$$\sum_{k=1}^{M} (k \cdot x_{ij}^k) - \sum_{k=1}^{M} (k \cdot x_{ij}^k) + e_{ij} + 1 \leq 0, \forall i, j : e_{ij} \in E. \quad (5)$$

For a given data dependency $e_{ij}$, the first summation simplifies to the cycle number at which the instruction $i$ is scheduled. Similarly, the second summation emits the cycle number at which the instruction $j$ is scheduled. This equation enforces the restriction that instruction $i$ may only be scheduled after the results of instruction $j$ are available.

The instruction latency to write to a GPR is 1 cycle ($e_{ij} = 1$). The latency for writing to a FPR is 5 cycles for $I_j \in I^{FPU}$ and at least 4 cycles for $I_j \in I^{LSU}$. Load instructions have higher latency when the loaded data is present in the L3 cache or the RAM. This can be considered in future formulations to maximize the number of cycles between loading the data of an instruction $i$ and using it by maximizing $e_{ij}$ in the objective.

We also wish to constrain the maximum number of allocated registers in a given code block. All of the registers are assumed to be allocated and released within the code block. An instruction $i$ scheduled at a cycle $c_j$ allocates a register $r$ by writing on it. The register $r$ is released (deallocated) at a cycle $c_k$ by the last instruction reading from it. The life

![Figure 4. DAG representation of interdependent instructions.](image)

![Figure 5. The $N \times M$ Boolean matrix layout for scheduling variables.](image)
span of the register $r$ is defined to be from cycle $c^i$ to cycle $c^k$ inclusive.

We define two $N \times M$ matrices of Boolean variables, $g^i_j$ and $f^i_j$, to represent the usage of the GPR and the FPR files, respectively. The value of $g^i_j$ is set to 1 during the lifespan of a register in the GPR modified by the instruction $I_i$ scheduled at the cycle $c^i$ and last read by an instruction scheduled at the cycle $c^k$, that is $g^i_j = 1$ when $j \leq z \leq k$ and zero otherwise. The same applies to the variables $f^i_j$ to represent the FPR register allocation.

To compute the values of $g^i_j$ and $f^i_j$, we define the temporary variables $\tilde{g}^i_j$ and $\tilde{f}^i_j$:

$$\tilde{g}^i_j = K_i \sum_{z=1}^{p} x^i_z - \sum_{j \in \text{FPU}} \left( \sum_{z=1}^{p} x^i_z \right), \forall i : I_i \text{ writes on FPR}, \quad (6)$$

$$\tilde{g}^i_j = K_i \sum_{z=1}^{p} x^i_z - \sum_{j \in \text{GPR}} \left( \sum_{z=1}^{p} x^i_z \right), \forall i : I_i \text{ writes on GPR}, \quad (7)$$

where $K_i$ is the number of instructions reading from the registers allocated by the instruction $I_i$. Here $\tilde{g}^i_j$ and $\tilde{f}^i_j$ have positive value during the lifespan of a register modified by the instruction $I_i$ in the GPR registers and the FPR registers, respectively. The first summation is a unit step function, which is equal to one starting from the cycle $p$ at which the instruction $I_i$ is scheduled. This unit step function is scaled to the number of consumers, $K_i$, of the register modified by $I_i$. The summations in the second term accumulate the number of consumers scheduled up to the cycle number $p$. When all of the consumers are scheduled, the equation is reduced to zero again.

The optimization variables $g^i_j$ and $f^i_j$ should equal 1 only when $\tilde{g}^i_j > 0$ and $\tilde{f}^i_j > 0$, respectively. This can be formulated as follows:

$$f^i_j - \tilde{f}^i_j \leq 0$$

$$g^i_j - \tilde{g}^i_j \leq 0$$

$$K_i \cdot f^i_j - \tilde{f}^i_j \geq 0$$

$$K_i \cdot g^i_j - \tilde{g}^i_j \geq 0.$$  

Now we can constrain the maximum number of used registers $FPR_{\text{max}}$ and $GPR_{\text{max}}$ by the following:

$$\sum_{i=1}^{N} (g^i_j) - GPR_{\text{max}} \leq 0, \forall j \in \{1, 2, \ldots, M\}, \quad (12)$$

$$\sum_{i=1}^{N} (f^i_j) - FPR_{\text{max}} \leq 0, \forall j \in \{1, 2, \ldots, M\}. \quad (13)$$

The optimization objective is to minimize the required number of cycles to execute the code ($n_c$). The complete formulation of the instruction scheduling problem is

Minimize: $n_c$ \quad (14)
correspondence between intrinsics and instructions is not exact enough for our purposes. The use of intrinsics can aid programmer productivity, as this method relies upon the compiler for such tasks as register allocation and instruction scheduling. However, our methods require precise control of these aspects of the produced assembly code, making this path unsuitable for our needs.

Our code generation framework is shown in Figure 6. The framework requires two inputs, a Python code and a C code template, represented by the two frames on the left-hand side of the diagram. The high-level Python code produces the instruction sequence of each code block. First, registers are allocated by assigning them variable names. Next, a list of instruction objects is created that utilize the variables to address registers. The C code template contains the main C code skeleton of the kernel, mainly the for-loop header and some common variable definitions and initialization. The C code specifies the required locations where the generated code blocks will be filled, including the prologue, the main body, and the epilogue of the for-loop.

Enabling the greedy instruction scheduler allows the simulator to execute the instructions out of order; otherwise they will be executed in order. The instruction simulator uses virtual GPR, FPR, and memory to simulate the pipeline execution and to simulate the expected results of the given instruction sequence. A log is produced by the instruction simulator to provide the simulation details, showing the cycles at which the instructions are scheduled and any encountered data and structural hazards. Also, the log can contain the contents of the GPR, the FPR, and the memory, at any cycle, to debug the code for correctness. The C code generator takes the simulated instructions and generates their equivalent inline assembly code in the provided C code template using the inline assembly extension to the C standard provided by GCC. For added clarity, we associate each generated line with a comment showing the mapping between the used register numbers and their corresponding variable names in the Python code.

4.2 Kernel design

The challenges in writing fast kernels in C and Fortran motivate us to program at the assembly level, a (perhaps surprisingly) productive task when using our code synthesis framework: an experienced user was able to design, implement, and test several efficient kernels for a new stencil operator in one day using the framework. Much of our work is based on the design of two small and naively scheduled 3-point kernels, dubbed mutate-mutate (mm) and load-copy (lc), that we introduce in this section. The kernels distinguish themselves from each other by their relative balance between load/store and floating point cycles consumed per stencil.

We find that efficiently utilizing SIMD units in stencil computations is a challenging task. To fill the SIMD registers, we pack two consecutive data elements from the fastest moving dimension, \( k \), allowing us to compute two stencils simultaneously, as in Araya-Polo et al. (2009). Computing in this manner is semantically equivalent to an unrolling by 2 in the \( k \) direction. As a conventional notation, since \( i \) and \( j \) are static for any given stream, we denote the two values occupying the SIMD register for a given array by their \( k \) indices, e.g. SIMD register \( a_{34} \) contains \( A_{i,j,3} \) in its primary half and \( A_{i,j,4} \) in its secondary half.

Many stencil operators map a subset of adjacent \( A \) elements with odd cardinality to each \( R \) element, as is illustrated in the left half of Figure 7, which depicts the SIMD register contents and computations mid-stream of a 3-point kernel. The odd cardinality prevents a straightforward mapping from SIMD input registers to SIMD output registers. We note that aligned SIMD loads from \( A \) easily allow for the initialization of registers containing \( a_{23} \) and \( a_{45} \). Similarly, the results in \( r_{34} \) can be safely stored using a SIMD store. The register containing \( d_{34} \), unaligned elements common to the aligned registers containing adjacent data, requires a shuffle within the SIMD registers through the use of additional load or floating point move instructions.
We introduce two kernels, which we designate as mm and lc, as two different approaches to place the unaligned data into the packed SIMD registers while streaming through A in memory. A ‘mutate’ operation is defined as the replacement of one operand of a SIMD register by a value loaded from memory. A ‘load’ operation is defined as the replacement of both operands in a SIMD register by a SIMD load from memory. A ‘copy’ operation is the replacement of one operand of a SIMD register by an operand from another SIMD register. Mutates and loads utilize the LSU, copies utilize the FPU.

The mm kernel replaces the older half of the SIMD register with the next element of the stream. In our example in Figure 7 we start with $a_{23}$ loaded in the SIMD register, then after the first computation we load $a_4$ into the primary part of the SIMD register so that the full contents are $a_{43}$.

The lc kernel instead combines the unaligned values in a SIMD register from two consecutive aligned quad-words loaded in two SIMD registers by copying the primary element from the second register to the primary element of the first. In our example $a_{23}$ and $a_{45}$ are loaded in two SIMD registers. Then, after the needed computations involving $a_{23}$ have been dispatched, a floating point move instruction replaces $a_2$ with $a_4$ to form $a_{43}$.

The two kernels use an identical set of floating point instructions, visually depicted in the right half of Figure 7, to accumulate the computations into the result registers. The two needed weight coefficients are packed into one SIMD register. The first floating point operation is a cross copy–primary multiply instruction, multiplying two copies of the first weight coefficient by the two values in $a_{23}$, then placing the results in the SIMD register containing $r_{34}$ (Figure 7a). Then, the value of $a_{23}$ in the SIMD register is modified to become $a_{43}$, replacing one data element in the SIMD register either through mutate or copy. The second floating point operation is a cross complex multiply–add instruction, performing a cross operation to deal with the reversed values (Figure 7b). Finally, the value $a_{45}$, which has either been preloaded by lc or is created by a second mutation in mm, is used to perform the last computation (Figure 7c).

We list the resource requirements of the lc and the mm kernels in Table 1. The two kernels are at complementary ends of a spectrum. The mm kernel increases pressure exclusively on the load pipeline while the lc kernel incurs extra cycles on the floating point unit. The two strategies can be used in concert, using mm when the floating point unit is the bottleneck and the lc when it is not.

Figure 7. SIMD stencil computations on one-dimensional streams: (a) compute contributions from $a_{23}$; (b) compute contributions from $a_{43}$; (c) compute contributions from $a_{45}$.
Table 1. Resource usage per stencil of mutate-mutate and load-copy kernels.

| Kernel         | Operations | Cycles | Registers |
|----------------|------------|--------|-----------|
| mutate-mutate  | ld-st 2-1  | 3       | 6 FPU 3   |
|                |            |         | Input 1   |
|                |            |         | Output 1  |
| load-copy      | 1-1        | 4       | 4 FPU 4   |
|                |            |         | Input 2   |
|                |            |         | Output 1  |

4.3 Unroll-and-jam

The 3-point kernels are relatively easy to specify in assembly, but the floating point and load/store instruction latencies will cause pipeline stalls if they are not unrolled. Further unrolling in the \( k \)-direction beyond two is a possible solution that we do not explore in this paper. Although this solution would reduce the number of concurrent memory streams, it would also reduce data reuse for the other stencils studied in this paper.

Unrolling and jamming once in transverse directions provides independent arithmetic operations to hide instruction latency, but interleaving the instructions by hand produces large kernels that are difficult to understand and modify. To simplify the design process, we constructed a synthetic code generator and simulator with reordering capability to interleave the jammed FPU and load/store instructions to minimize pipeline stalls. The synthetic code generator also gives us the flexibility to implement many general stencil operators, including the 7-point and 27-point stencils, using the 3-point stencil as a building block.

Unroll-and-jam serves a second purpose for the 7-point and 27-point stencil operators due to the overlapped data usage among adjacent stencils. Unroll-and-jam eliminates redundant loads of common data elements among the jammed stencils, reducing pressure on the memory subsystem by increasing the effective arithmetic intensity of the kernel. This can be quantified by comparing the number of input streams, which we refer to as the ‘frame size’, with the number of output streams. For example, an unjammed 27-point stencil requires a frame size of 9 input streams for a single output stream. If we unroll once in \( i \) and \( j \), we generate a \( 2 \times 2 \) jam with 4 output streams using a frame size of 16, improving the effective arithmetic intensity by a factor of \( \frac{9}{16} \).

We used mm and lc kernels to construct 3-, 7-, and 27-point stencil kernels over several different unrolling configurations. Table 2 lists the register allocation requirements for these configurations and provides per-cycle computational requirements. In both the mm and lc kernels, the 27-point stencil is theoretically FPU-bound because of the high reuse of loaded input data elements across streams.

As can be seen in Table 1, the mm kernel allows more unrolling for the 27-point stencil than the lc kernel because it uses fewer registers per stencil. The number of allocated registers for input data streams at the mm kernel is equal to the number of the input data streams, while the lc kernel requires twice the number of registers for its input data streams.

4.4 PowerPC 450 scheduler

The high-level code synthesis technique generates as many as hundreds of assembly instructions to apply an unroll-and-jammed stencil. The PowerPC 450 scheduler attempts to minimize the expected cycles per stencil iteration by applying a greedy heuristic to the instruction scheduling problem defined in Equations (2)–(5) and (12)–(15) with the generated assembly instructions as data. We note that the scheduler does not guarantee global optimality of the resulting schedule and does not perform register allocation (it requires registers to be named by the input instructions). The PowerPC 450 scheduler simulates the execution of the instruction stream to solve the instruction scheduling problem. The simulator reflects an understanding of the constraints by modeling the instruction set, including semantics such as read and write dependencies, latency, and occupied execution unit. It functions as if it were a PowerPC 450 with an infinite-lookahead, greedy, out-of-order execution unit. On each cycle, it attempts to start an instruction on both the load/store and floating point execution units while observing instruction dependencies. If this is not possible, it provides diagnostics about the size of the stall and what dependencies prevented another instruction from being scheduled. The simulator both modifies internal registers that can be inspected for verification purposes and produces a log of the reordered instruction schedule. The log is then rendered as inline assembly code which can be compiled using the XL or GNU C compilers.

5 Performance

Code synthesis allows us to easily generate and verify the performance of 3-, 7-, and 27-point stencil operators against our predictive models over a range of unrolling-and-jamming and inner kernel options. We use individual MPI processes mapped to the four PowerPC 450 cores to provide 4-way parallelization and ascertain performance characteristics out to the shared L3 and DDR memory banks.

We conducted a number of simple tests to assess performance at various levels of the memory hierarchy. We determined the bandwidth to the DRAM to be 3.7 bytes/cycle, and 5.3 bytes/cycle write bandwidth. Also, we determined the read bandwidth to the L3 to be 4.7 bytes/cycle, and 5.3 bytes/cycle write bandwidth. The test codes utilized to perform these tests were all hand-written in assembly to utilize the SIMD load and store instructions available in the PowerPC 450 core. Because there are alignment restrictions related to the use of such SIMD instructions, we allocated the arrays so as not to incur alignment exceptions. It should also be noted that while it is sometimes possible, when one has exceeded the capacity of the L1 data cache, to achieve higher performance through the use of multiple data streams, each stream being carefully co-aligned, we did not employ that tactic in our tests. All of these tests employed a single data stream and, in fact, a single instruction type (e.g. we did not carefully...
interleave no-op instructions to provide what can sometimes be superior timing characteristics). Finally, these codes were constructed to have no data dependencies and we ensured that the number of static instructions was such that there could be no self-dependencies (i.e. a loop composed of a single load instruction will be hindered by the fact that there is a single target register).

We computed the bandwidth-limited throughput limit for each stencil kernel based on the read and write requirements for each stencil and the maximum read and write bandwidth of the hardware:

$$\text{throughput} = \frac{850 \text{ Mcycles/second}}{\text{cycles/stencil}}$$ \hspace{1cm} (16)

where

$$\text{cycles/stencil} = \frac{\text{read bytes/stencil}}{\text{HW read bytes/cycle}} + \frac{\text{write bytes/stencil}}{\text{HW write bytes/cycle}}$$ \hspace{1cm} (17)

We do not employ tiling strategies and therefore naively assume no data reuse within each cache level.

The generated assembly code, comprising the innermost loop, incurs a constant computational overhead from the prologue, epilogue, and registers saving/restoring. The relative significance of this overhead is reduced when larger computations are performed at the innermost loop. This motivated us to decompose the problem’s domain among the four cores along the outermost dimension for the 3- and 7-point stencils, resulting in better performance. However, the 27-point stencil has another important property, dominating the innermost loop overhead cost. Its computations exhibit relatively high input data sharing among neighbor stencils. Splitting the innermost dimension allows the shared input data points to be reused by consecutive middle dimension iterations, where the processor will likely have them in the L1 cache, resulting in faster computations. Conversely, if the computation is performed using a large innermost dimension, the shared input data points will no longer be in the L1 cache at the beginning of the next iteration of the middle loop.

All three studies were conducted over a range of cubic problems from size $14^3$ to $36^3$. The problem sizes were chosen such that all variations of the kernels could be evaluated naively without extra code for cleanup. We computed each sample in a nested loop to reduce noise from startup costs and timer resolution, then selected the highest performing average from the inner loop samples. There was almost no noticeable jitter in sample times after the first several measurements. All performance results are given per-core, although results were computed on an entire node with a shared L3 cache and no explicit ghost cell data exchange. Thus, a slightly optimistic limit on asynchronous full-node performance can be obtained by multiplying by four.

During the course of our experiments on the stencils, we noticed performance problems for many of the stencil variants when loading data from the L3 cache. The large number of concurrent hardware streams in the unroll-and-jam approach overwhelms the L2 streaming unit, degrading performance. This effect can be amplified in the default optimistic prefetch mode for the L2, causing wasted memory traffic from the L3. We made use of a boot option that disables optimistic prefetch from the L2 and compare against the default mode where applicable in our results. We distinguish between the two modes by using solid lines to indicate performance results obtained in the default mode and dashed lines to indicate results where the optimistic prefetch in L2 has been disabled.

### 5.1 3-point stencil computations

We begin our experiments with the 3-point stencil (Figure 8), the computational building block for the other experiments in our work.

| Kernel | Frame | Stencils/Iteration | Registers | Instructions |
|--------|-------|-------------------|------------|--------------|
|        |       |                   |            | Configurations | Count | Cycles | Utilization % |
|        |       |                   |            |              | Id-st FPU | Id-st FPU | Id-st FPU |
| 27-mm-1x1 | 9 2 | 9 | 1 | 4 | 18-1 27 | 36-2 27 | 100 71.1 80 |
| 27-mm-1x2 | 12 4 | 12 | 2 | 4 | 24-2 54 | 48-4 54 | 96.3 100 56 |
| 27-mm-1x3 | 15 6 | 15 | 3 | 4 | 30-3 81 | 60-6 81 | 81.5 100 48 |
| 27-mm-2x2 | 16 8 | 16 | 4 | 4 | 32-4 108 | 64-8 108 | 66.7 100 40 |
| 27-mm-2x3 | 20 12 | 20 | 6 | 4 | 40-6 162 | 80-12 162 | 56.8 100 34.7 |
| 7-mm-2x3 | 16 12 | 16 | 6 | 2 | 22-6 42 | 44-12 42 | 100 75 29.3 |
| 7-lc-2x3 | 16 12 | 22 | 6 | 2 | 16-6 48 | 32-12 48 | 91.7 100 29.3 |
| 3-lc-1x1 | 1 2 | 2 | 1 | 1 | 1-1 4 | 2-2 4 | 100 100 16 |
| 3-lc-2x1 | 2 4 | 4 | 2 | 1 | 2-2 8 | 4-4 8 | 100 100 16 |
| 3-lc-2x2 | 4 8 | 4 | 4 | 1 | 4-4 16 | 8-8 16 | 100 100 16 |
| 3-lc-2x3 | 6 12 | 12 | 6 | 1 | 6-6 24 | 12-12 24 | 100 100 16 |
| 3-lc-2x4 | 8 16 | 16 | 8 | 1 | 8-8 32 | 16-16 32 | 100 100 16 |
The 3-point stencil has the lowest arithmetic intensity of the three stencils studied, and unlike its 7-point and 27-point cousins, does not see an increase in effective arithmetic intensity when unroll-and-jam is employed. It is clear from Section 4.2 that the lc kernel is more efficient in bandwidth-bound situations, so we use it as the basis for our unroll-and-jam experiments. We see the strongest performance in the three problems that fit partially in the L1 cache (the peak of 224 Mstencil/s is observed at 263), with a drastic drop off as the problem inputs transition to the L3. The most robust kernel is the 2 × 1 jam, which reads and writes to two streams simultaneously, and can therefore engage the L2 prefetch unit most effectively. The larger unrolls (2 × 2, 2 × 3, and 2 × 4), enjoy greater performance in and near the L1, but then suffer drastic performance penalties as they exit the L1 and yet another performance dip near 2503. Disabling optimistic L2 prefetch does not seem to have any large effect on the 2 × 1 kernel, although it unreliably helps or hinders the other kernels.

The 3-point kernel seems to be an ideal target on the PowerPC 450 for standard unrolling in the fastest moving dimension, k, a technique we did not attempt due to its limited application to the larger problems we studied. Unroll-and-jam at sufficient sizes to properly cover pipeline hazards overwhelms the L2 streaming unit due to the large number of simultaneous streams to memory. Unrolling in k would cover these pipeline hazards without increasing the number of streams.

5.2 7-point stencil computations

Our next experiment focuses on the performance of the 7-point stencil operator (Figure 9). We compare the mm and lc kernels using the same unroll configurations. We note that the mm kernel can support a slightly more aggressive unroll-and-jam on this problem with a compressed usage of general purpose registers that was only implemented for the 27-point stencil.

Once again we note strong performance within the L1, then a dropoff as the loads start coming from the L3 instead of the L1. The performance drop near 2563 is caused when the 2 × 3 kernel’s frame size of (2 + 2)(3 + 2) − 4 = 16 multiplied by the length of the domain exceeds the size of L1. For smaller sizes, neighbors in the j direction can reside in L1 between consecutive passes so that only part of the input frame needs to be supplied by streams from memory. With up to 16 input streams and 2 · 3 = 6 output streams, there is no hope of effectively using the L2 prefetch unit. The lc kernel shows better performance than the mm kernel, as it is clear here that load/store cycles are more constrained than floating point cycles. We also note that performance of the lc kernel improves with the L2 optimistic prefetch disabled slightly within the L3, and drastically when going to the DDR banks. This is likely due to the kernel’s improved performance, and therefore increased sensitivity with regards to latency from the memory subsystem. It is likely that the 7-point stencil could attain better results by incorporating cache tiling strategies, though we note that without any attempts at cache tiling the performance of this result is commensurate with previously reported results for the PowerPC 450 that focused on cache tiling for performance tuning.

We compare our results with the findings of Datta (2009). Both results achieved perfect scaling from one to two and four cores. We achieved about 284 Mstencil/s and Datta achieved about 290 Mstencil/s on four cores. At this evaluated domain size, 2563, the problem becomes memory bound as the data is streamed from the main memory, resulting in the similarity of achieved performance.
Since performance within a core is often considerably easier to predict than when one must go beyond the core for memory access, we divide our comparisons into those on-core (L1) and those that go off the core, to L3 or main memory (streaming).

Our modeling of the 27-point stencils can be seen to be highly accurate in Table 3. Inside the L1 cache the disparity between predicted and actual performance is consistently less than 1%. Shifting our attention to the streaming predictions, our accuracy can be seen to be considerably degraded. This is not surprising, given that our simulator was largely targeted to model the L1 domain. However, the relative error is less than 15% in all cases; this appears to be sufficient for producing highly efficient code. This shortcoming appears to stem directly from the level of detail with which we model the shared L3 cache and main memory subsystem and we are working to address this in our simulator.

The match between predicted and witnessed performance for the 7-point stencil shows the same pattern. When modeling performance inside the L1 our relative error is less than 10%, but when extending our prediction to the components of the system shared by all four cores, our error is as great as 17.5%. Our greatest error in this instance is an under-prediction that is probably attributable to a fortuitous alignment of the continuous vectors in the k-direction, as staggering these carefully often result in bandwidth benefits of the order of 10–15%.

Finally, we assess our model for the 3-point stencil. Again we see good agreement between the model and observed performance within the L1, although prediction accuracy degrades for problem sizes requiring streaming. From some further experimentation, we are reasonably certain that the chief reason for our lack of accuracy in predicting performance outside of the L1 stems from the bandwidth that must be shared between the multiple write streams and our failure to account for this in our model. It is most apparent in the 3-point stencil predictions as the ratio of write streams to either read streams or floating point operations is highest in this case.

6 Concluding remarks

6.1 Conclusion

The main contribution of this work is effective register and instruction scheduling for constant coefficient linear operators on power-efficient processors. The loads of the input vector elements and stores of the output vector elements are minimized and the fraction of multiply–adds among all cycles is maximized. This is achieved by using two novel 3-point stream-computation sub-kernels designed for the PowerPC 450’s instruction set, mm and lc.

Recommendations for the research agenda for computational software libraries in the exascale domain include the fusion of library routine implementations as well as the creation of frameworks that enable the optimal instantiation of...
Table 3. Predictions versus observations for in-L1 and main memory streaming performance, in 𝑀stencil/s.

| Kernel     | Instruction limits | Bandwidth limits | In-L1 | Streaming |
|------------|--------------------|------------------|-------|-----------|
|            | Naive             | Simulated        | L1    | Streaming |
| 27-mm-1x1  | 44.74             | 11.93            | 80.88 | 40.54     |
| 27-mm-1x2  | 62.96             | 23.35            | 113.19| 58.69     |
| 27-mm-1x3  | 62.96             | 34.30            | 130.58| 68.99     |
| 27-mm-2x2  | 62.96             | 44.59            | 154.28| 83.68     |
| 27-mm-2x3  | 62.96             | 54.62            | 175.52| 97.51     |
| 7-mm-2x3   | 182.14            | 126.84           | 203.54| 116.84    |
| 7-1c-2x3   | 212.50            | 143.83           | 203.54| 116.84    |
| 3-1c-1x1   | 425.00            | 88.12            | 338.72| 231.51    |
| 3-1c-2x1   | 425.00            | 147.29           | 338.72| 231.51    |
| 3-1c-2x2   | 425.00            | 193.36           | 338.72| 231.51    |
| 3-1c-2x3   | 425.00            | 202.31           | 338.72| 231.51    |
| 3-1c-2x4   | 425.00            | 197.10           | 338.72| 231.51    |

The primary contribution of this work is a simulation model and code generation framework for the IBM PowerPC 450 CPU and its L1 cache. Further extensions to include a more comprehensive memory model specifically addressing cache sizes (Treibig and Hager, 2010), latency, and prefetch streams would enable coupled design of computational kernels and tiling strategies. For other multicore/simultaneous multithreading architectures such as Intel x86 and IBM Blue Gene/Q, a contention model for shared architectural components including the memory bus and caches will need to be introduced (Wittmann et al., 2010). The design and implementation of these extensions are left as future work.

While the three problems considered (3-point stencils in one dimension and 7-point and 27-point stencils in three dimensions, with constant coefficients and symmetry within each spatial dimension, but not across them) are heavily used in applications, there are numerous generalizations. The suitability of our approach can be characterized by the arithmetic intensity associated with each generalization. We elaborate on two that tend to increase the arithmetic intensity, higher-order stencils and chained iterative passes over the vectors, and two that tend to decrease arithmetic intensity, irregular stencils and spatial varying coefficients.

Higher-order stencils expand the number of adjacent input vector elements that enter into a single output vector element, in successive steps of semi-width one in each of the spatial dimensions 𝑖, 𝑗, and 𝑘, with an additional weight coefficient corresponding to each additional increment of semi-width in each dimension. This is a modest generalization. Higher-order discretization increases register pressure because of the larger number of inputs that combine in each output. Opportunities for reuse of input elements expand with the stencil width up to the ability to keep them resident. In a P-point regular stencil (regardless of number of spatial dimensions) each input element is operated upon with a pre-stored weight P times: once in the stencil centered upon it, and once in each neighboring stencil with which its own stencil overlaps. Floating point arithmetic intensity increases in proportion to P. That is, if there are 𝑁 elements in the input or output array, there are 𝑁 𝑃 floating point multiply–adds per 𝑁 floating reads and 𝑁 floating writes. Explicit methods for nonlinear systems, especially with high-order discretization techniques such as Weighted Essentially Non-Oscillatory (WENO) or discontinuous Galerkin (Shu, 2003), have similar properties, including a larger number of input streams, but with much higher arithmetic intensity.

S-stage chaining (as in the simultaneous accumulation of 𝑀 𝑋, 𝑀 𝑋, ...) allows the output vector to be fed back as input before being written. Per output vector of 𝑁 floating point writes, there are 𝑁/𝑆 reads and 𝑁 𝑃 floating point multiply–adds. Therefore, up to the ability to keep the additional operands cached, both higher-order operators and chained operations improve the potential for the transformations described here.

Irregular stencils require integer reads in addition to floating point reads to determine which elements of the input vector go with each row of the matrix. This further dilutes advantages that lead to the great break-throughs in stencils per second described here. Stencil operations with constant coefficients and sparse matrix–vector multiplies with general coefficients are similar when counting floating operations, but very different when it comes to data volume.

Spatially varying coefficients require the loading of additional weights, each of which is used only once, each of which is of the same floating precision of the input and
output vectors, $P$ of them in the production of each output vector element, with each input vector element being combined with $P$ different weights. While each input and output element can still be reused up to $P$ times in the execution of one pass through the overall vector-to-vector map, the dominant array in the workspace is the coefficient matrix of weights so the benefits of reusing the vectors are minimal. This situation is typical for nonlinear problems when using Newton–Krylov and linear multigrid methods. However, when ‘free flops’ are available, the weights can also be recomputed on the fly as a nonlinear function of a given state and/or scalar coefficients. In this case, the number of input streams is similar to the linear constant coefficient case (perhaps larger by a factor of 2 or 3), but the number of floating point results is several times higher and involves the problem-specific ‘physics’. Putting the physics inside the kernel like this suggests that there will be an emphasis on the ability to quickly develop high-performance kernels for new physics.

**Funding**

This research received no specific grant from any funding agency in the public, commercial, or not-for-profit sectors.

**Acknowledgments**

We are grateful to Andy Ray Terrel for his helpful commentary on an early draft of this paper. We are also indebted to Andrew Winfer for his support in conducting our numerical experiments on the Shaheen Blue Gene/P system at the KAUST Supercomputing Laboratory, and to Vernon Austel for his assistance in running experiments on the Blue Gene/P system at IBM’s Watson Research Center.

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