Successive Cancellation List Polar Decoder using Log-likelihood Ratios

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Abstract—Successive cancellation list (SCL) decoding algorithm is a powerful method that can help polar codes achieve excellent error-correcting performance. However, the current SCL algorithm and decoders are based on likelihood or log-likelihood forms, which render high hardware complexity. In this paper, we propose a log-likelihood-ratio (LLR)-based SCL (LLR-SCL) decoding algorithm, which only needs half the computation and storage complexity than the conventional one. Then, based on the proposed algorithm, we develop low-complexity VLSI architectures for LLR-SCL decoders. Analysis results show that the proposed LLR-SCL decoder achieves 50% reduction in hardware and 98% improvement in hardware efficiency.

Keywords—polar codes, successive cancellation list (SCL), log-likelihood ratio (LLR), VLSI, low-complexity

I. INTRODUCTION

Polar codes have become one of the most favorable forward error correction (FEC) codes since their discovery in 2008 [1]. Nowadays information theorists have shown that the capacity-achieving polar codes can achieve beyond-LDPC error-correcting performance with the use of successive cancellation list (SCL) algorithm [2]. Therefore, the SCL algorithm is viewed as the most promising approach for practical polar decoding.

To date, original SCL algorithm and its variants are based on likelihood [2] or log-likelihood (LL) forms [3-4][8]. Because most FEC-contained systems are based on log-likelihood ratio (LLR) form, the current non-LLR-based SCL decoders are incompatible for practical applications. Moreover, because two types of decoding messages (probability being 0 and 1) need to be processed and stored in non-LLR-based SCL decoders, the corresponding hardware complexity is very high.

This paper presents an LLR-based SCL (LLR-SCL) algorithm for polar code decoding. In the proposed algorithm, the ratio of probability being 0 and 1 is used to represent the decoding messages. As a result, the computation complexity and memory requirement of LLR-SCL algorithm is greatly reduced as compared to LL-SCL case. Then, based on this new algorithm, a VLSI architecture of the LLR-SCL decoder is presented. Analysis shows that the proposed LLR-SCL decoder achieves 50% reduction in hardware and 98% increase in hardware efficiency.

The rest of this paper is organized as follows. Section II reviews the polar codes. The proposed LLR-SCL algorithm is presented in Section III. Section IV develops the hardware architecture of LLR-SCL decoder. Hardware performance is analyzed in Section V. Section VI draws the conclusions.

II. REVIEW OF POLAR CODES

A. Polar Code

As shown in [1], the reliability of decoded bits over discrete binary memoryless symmetric channel (D-BMS) can be polarized according to their positions at the codeword. Therefore, by assigning k bits in the source data and (n-k) “0” bits over the reliable and unreliable positions, respectively, we can construct a length-n polar code with rate R=k/n. In general, these (n-k) “0” bits are called “frozen” bits while the k information bits are called “free” bits. For the details of polar encoding, the reader is referred to [1].

B. Successive Cancellation SC Algorithm

An SCL decoder can be viewed as multiple copies of successive cancellation (SC) decoder; therefore we first introduce SC decoder in this subsection.

Fig. 1 shows the decoding scheme of a likelihood-based SC decoder with n=4. Here the SC decoder consists of log2n=2 stages, where each stage consist of 4-input 2-output f and g units as the basic computation units. At the end of the last stage (stage2 in this example), a hard-decision unit (h) is used to determine the decoded bit u. Notice that in Fig. 1 each f or g unit is labeled with a number, which indicates the time index when the corresponding unit is activated.

The function of f and g units can be derived from the polar encoding procedure. Fig. 2(a) shows the basic computation unit of the polar encoder. It can be seen that the basic encoding computation is a left-to-right transformation as output=inn1 ⊕ inn2, and output2=inn2, where ⊕ is the exclusive-or operation.
Correspondingly, the functions of \( f \) and \( g \) units, as the basic computation unit of polar decoder, represent right-to-left estimations from \( out_1 \) and \( out_2 \) to \( \hat{n}_1 \) and \( \hat{n}_2 \), where \( \hat{n}_1 \), \( \hat{n}_2 \), \( out_1 \), \( out_2 \) denote the estimates of \( n_1 \), \( n_2 \), \( out_1 \), and \( out_2 \), respectively. If we assume previous decoded bits \( \hat{u}_1, \hat{u}_2 \ldots \hat{u}_{n-1} \) are \( z_1, z_2 \ldots z_{n-1} \), and denote this event as \( \hat{u}_n = z_{n-1} \), then we can derive the functions of \( f \) and \( g \) units as follows:

\[
c_0 = Pr(\hat{n}_1 = 0, u_1 = z_{i-1}^-) = a_0 h_0 + a_1 h_1
\]

\[
c_i = Pr(\hat{n}_1 = 1, u_1 = z_{i-1}^-) = a_0 h_1 + a_1 h_0
\]

\[
d_0 = Pr(\hat{n}_2 = 0, u_1 = z_{i-1}^-) = a_0 h_{out} + a_1 h_0
\]

\[
d_1 = Pr(\hat{n}_2 = 1, u_1 = z_{i-1}^-) = a_0 h_{out} + a_1 h_1
\]

where \( a_0 = Pr(out_2 = 0, u_1 = z_{i-1}^-), \ a_1 = Pr(out_2 = 1, u_1 = z_{i-1}^-), \ h_0 = Pr(out_1 = 0, u_1 = z_{i-1}^-), \) and \( h_1 = Pr(out_1 = 1, u_1 = z_{i-1}^-) \) are the 4 inputs of \( f \) and \( g \) units.

Besides, the function of hard-decision \( h \) unit is

\[
h_n = \begin{cases} 
0 & \text{if } a_n \geq a_i \text{ or } \hat{u}_i \text{ is frozen bit} \\
1 & \text{if } a_n < a_i \text{ and } \hat{u}_i \text{ is free bit} 
\end{cases}
\]

In general, (1)-(5) describe likelihood-based SC algorithm.

C. SC Algorithm over code tree

On the other hand, from the view of code tree, the SC algorithm can be viewed as the path searching process over \( n \)-level code tree. Fig. 3 shows an example searching procedure with \( n=4 \). Here level-\( i \) represents decoded bit \( \hat{u}_i \). In addition, the value associated with each node is the metric for the path from root node to the current node. For example, 0.09 is the path metric for length-3 path (1,0,1). Here (1,0,1) represents \( u_1 = 1, u_2 = 0 \) and \( u_3 = 1 \). Therefore, the path (1,0,1) with metric 0.09 indicates that \( Pr(\hat{u}_1 = 1, \hat{u}_2 = 0, \hat{u}_3 = 1) = 0.09 \).

\[\text{Fig. 2. (a) basic unit of polar encoding, (b) basic unit of polar SC decoding, cited from [8].}\]

Notice that for the \( f \) or \( g \) units in the last stage (for example stage2 in Fig. 1), \( \hat{n}_1 \) or \( \hat{n}_2 \) is \( \hat{u}_i \). In that case, according to (1)-(5), \( c_0, c_1, d_0 \) or \( d_1 \), as the output of \( f \) or \( g \) unit, represent the joint probabilities of \( u_1, u_2, \ldots, u_i \), which is just the metric of path \( (u_1, u_2, \ldots, u_i) \). Therefore, the path metric of SC algorithm is calculated by the \( f \) or \( g \) units in the last stage.

With the use of path metric, the SC decoder performs a locally optimal searching strategy to find the length-\( n \) path with largest metric. As shown in Fig. 3, in each level the SC decoder first visits two children nodes that are associated with the current survival path. By comparing the corresponding path metrics, the SC decoder selects the path with larger metrics as the updated survival path. The example survival path in Fig. 3 is marked as red arrows. It can be seen that the valid length-4 path with largest metric 0.19 can be found by the SC decoder.

D. SCL Decoding Algorithm

Due to the limit of locally optimal search, in many cases the SC decoder cannot find the correct decoding path. In [2] SCL algorithm was proposed to solve this problem. By using multiple SC decoders over the same code tree, the chance of finding the correct decoding path is significantly improved. Here the number of SC component decoders is referred as list size \( L \). Fig. 4 shows an example of \( n=4 \) SCL decoder with \( L=2 \). It can be seen that the SCL decoder can trace the correct path (1,0,0,0) with metric 0.23 while SC decoder cannot.
III. THE PROPOSED LLR-SCL ALGORITHM

A. Benefit of LLR-based Representation

In Section II we present the likelihood-based SC and SCL algorithms. However, in practical applications LLR-based representation, instead of likelihood-based form, is usually adopted for soft FEC decoder designs. This is because the LLR-based designs have much less hardware complexity than the non-LLR-based ones. Generally, in order to describe the joint probabilistic information of a bit \( v \) and event \( \Psi \), the likelihood-based decoders need to process and store two types of messages as \( \Pr(v=0, \Psi) \) and \( \Pr(v=1, \Psi) \), while LLR-based decoders only need to deal with one type of message as \( (\ln(\Pr(v=0, \Psi)/\Pr(v=1, \Psi))) \). As a result, the computation complexity and memory requirement of LLR-based decoders are much lower than their likelihood-based counterparts.

In [5], the LLR-based representation had been used in SC decoder design. The success of LLR-based scheme in SC algorithm is built on the property that the binary value of decoded bit \( \hat{u} \) can be directly determined from the sign of corresponding LLR messages. However, in SCL algorithm no such property exists. The \( \hat{u} \) in the SCL algorithm has to be determined by comparing the metrics of all the candidate paths, which are inherently based on likelihood form. As a result, the current SCL decoders are either based on likelihood or log-likelihood (LL) form, instead of LLR form.

B. The Proposed LLR-SCL Decoding Algorithm

In this subsection we present a LLR-based SCL (LLR-SCL) algorithm. First, we convert original likelihood-base messages in (1)-(4) to the LLR-based forms as follows:

\[
\begin{align*}
    c &= 2 \tanh^{-1}(\tanh(\frac{a}{2}) \tanh(\frac{b}{2})) = \text{sign}(a) \text{sign}(b) \min(|a|, |b|) \\
    d &= a(-1)^{|c|} + b
\end{align*}
\]

where \( c=\ln(c)/\ln(c) \), \( d=\ln(d)/\ln(d) \), \( a=\ln(a)/\ln(a) \) and \( b=\ln(b)/\ln(b) \).

After representing all the messages in the LLR form, the next step is to calculate path metrics, which is the key task for developing LLR-based SCL algorithm. For the likelihood-based SCL algorithm, this calculation is automatically performed by the likelihood-based \( f \) or \( g \) unit in the last stage of SC component decoders. However, for the LLR-SCL algorithm, after the LLR-based \( f \) or \( g \) unit outputs LLR messages \( c \) or \( d \), an extra metric computation unit (MCU) is needed to calculate path metrics. Next we derive the function of MCU.

First, notice that the metric for the length-1 path \( (\hat{u}_1, \hat{u}_2, \ldots, \hat{u}_i) \) is \( \Pr(\hat{u}_i = z_{i-1}, \hat{u}_{i-1} = z_{i-2}, \ldots, \hat{u}_0 = z) = \Pr(\hat{u}_i = z, \hat{u}_{i-1} = z_{i-1}) \).

Then with the log-domain representation, the metrics for length-1 paths are:

\[
\begin{align*}
    M_{i,0} &= \ln(\Pr(\hat{u}_i = 0, \hat{u}_{i-1} = z_{i-1})) \\
    M_{i,1} &= \ln(\Pr(\hat{u}_i = 1, \hat{u}_{i-1} = z_{i-1}))
\end{align*}
\]

where \( M_{i,0} \) and \( M_{i,1} \) represent the path metrics when \( \hat{u}_i = 0 \) and \( 1 \), respectively.

Then, recall the function of MCU is to calculate the path metrics \( M_{i,0} \) and \( M_{i,1} \) with the known \( c \) or \( d \) output from \( f \) or \( g \) unit in the last stage. Without loss of generality, we assume MCU uses \( c \) to calculate path metrics. As a result, for the \( f \) units in the last stage, we have:

\[
    c = \ln(\frac{\Psi_{0c}}{\Psi_1}) = \ln(\frac{\Pr(\hat{u}_i = 0, \hat{u}_{i-1} = z_{i-1})}{\Pr(\hat{u}_i = 1, \hat{u}_{i-1} = z_{i-1})}) = M_{i,0} - M_{i,1}
\]

(10)

In addition, similar to the case for length-1 path, the log-domain metric \( M_{i-k,i-k} \) for length-(\( i-1 \)) path \( (\hat{u}_i = z_i, \hat{u}_{i-1} = z_{i-1}, \ldots, \hat{u}_1 = z_2, \hat{u}_0 = z_1) \) can be represented as:

\[
\begin{align*}
    M_{i-k,i-k} &= \ln(\Pr(\hat{u}_{i-k} = z_{i-k}, \hat{u}_{i-1} = z_{i-1})) = \ln(\Pr(\hat{u}_i = 1, \hat{u}_{i-1} = z_{i-1})) \\
    &= \ln(\Pr(\hat{u}_i = 0, \hat{u}_{i-1} = z_{i-1}) + \Pr(\hat{u}_i = 1, \hat{u}_{i-1} = z_{i-1})) \\
    &= \ln(e^{M_{i-1,i-1}} + e^{M_{i-1,i-1}})
\end{align*}
\]

(11)

Consequently, based on (10)(11) we can calculate \( M_{i,0} \) and \( M_{i,1} \) as follows:

\[
\begin{align*}
    M_{i,0} &= M_{i-i,i-k} + c - \ln(1 + e^c) \\
    M_{i,1} &= M_{i-i,i-k} - \ln(1 + e^c)
\end{align*}
\]

(12)(13)

The above (12)(13) contains \( \ln(*) \) computation, which needs complex lookup table (LUT) for hardware design. Hence we need to simplify the calculations of \( M_{i,0} \) and \( M_{i,1} \).

Consider \( \ln(1 + e^c) \approx \begin{cases} x & \text{for large } x \\ 0 & \text{for small } x \end{cases} \), (12)(13) can be further approximated as follows:

\[
\begin{align*}
    M_{i,0} &\approx \begin{cases} M_{i-i,i-k} & \text{if } c \geq 0 \\ M_{i-i,i-k} + c & \text{if } c < 0 \end{cases} \\
    M_{i,1} &\approx \begin{cases} M_{i-i,i-k} - c & \text{if } c \geq 0 \\ M_{i-i,i-k} & \text{if } c < 0 \end{cases}
\end{align*}
\]

(14)(15)

Similarly, if MCU uses LLR messages \( d \) to calculate path metrics, then we have:

\[
\begin{align*}
    M_{i,0} &\approx \begin{cases} M_{i-i,i-k} + d & \text{if } d \geq 0 \\ M_{i-i,i-k} & \text{if } d < 0 \end{cases} \\
    M_{i,1} &\approx \begin{cases} M_{i-i,i-k} - d & \text{if } d \geq 0 \\ M_{i-i,i-k} & \text{if } d < 0 \end{cases}
\end{align*}
\]

(16)(17)

In general, (14)-(17) show how to calculate the metric of length-\( i \) path with LLR messages. After \( f \) or \( g \) unit in the last stage outputs the LLR message \( (c \text{ or } d) \), with the knowledge of length-(\( i-1 \)) path metric \( (M_{i-1,i-1}) \), we can calculate the metric of length-\( i \) path \( (M_{i,0} \text{ and } M_{i,1}) \). As a result, the LLR-SCL algorithm is summarized as follows:
C. Simulation Results

In subsection III-B, we perform approximation on the path metric calculation to avoid complex In(*) computation. Fig. 5 shows this approximation does not cause performance loss. In addition, it also seen that the approximated LLR-SCL algorithm has the same error-correcting performance with the original non-LLR-based SCL algorithm.

| Eb/No (dB) | SC | non-LLR SCL L=2 | LLR-SCL L=2 exact | LLR-SCL L=2 approx | non-LLR SCL L=4 | LLR-rSCL L=4 exact | LLR-rSCL L=4 approx |
|-----------|----|-----------------|-------------------|-------------------|-----------------|-------------------|-------------------|
| 1.2       | 10^0 | 10^0            | 10^0              | 10^0              | 10^0            | 10^0              | 10^0              |
| 1.4       | 10^0 | 10^0            | 10^0              | 10^0              | 10^0            | 10^0              | 10^0              |
| 1.6       | 10^0 | 10^0            | 10^0              | 10^0              | 10^0            | 10^0              | 10^0              |
| 1.8       | 10^0 | 10^0            | 10^0              | 10^0              | 10^0            | 10^0              | 10^0              |
| 2.0       | 10^0 | 10^0            | 10^0              | 10^0              | 10^0            | 10^0              | 10^0              |
| 2.2       | 10^0 | 10^0            | 10^0              | 10^0              | 10^0            | 10^0              | 10^0              |
| 2.4       | 10^0 | 10^0            | 10^0              | 10^0              | 10^0            | 10^0              | 10^0              |
| 2.6       | 10^0 | 10^0            | 10^0              | 10^0              | 10^0            | 10^0              | 10^0              |

D. Overall Architecture of LLR-SCL Decoder

A. Overall Architecture

In this section, based on the new LLR-SCL algorithm, we develop the corresponding hardware architecture. Fig. 6 shows the overall architecture of L-size LLR-SCL decoder. It can be seen that the LLR-SCL decoder consists of L LLR-SC component decoders, which had been discussed in our prior work [5]. After the last stages (f or g units) of the SC decoders calculate c or d, these LLR messages, together with previous path metrics, are input to L metric computation units (MCUs) to generate 2L path metric candidates. Then a sorting block is used to select L largest metrics among the 2L candidates. The L paths which are associated with the L selected metrics become the updated survival paths.

Besides the above mentioned computation blocks, the LLR-SCL decoder also contains three types of memory banks. The LLR messages memory bank stores and provides the LLR messages which are used in L LLR-SC decoders. Survival path memory bank and path memories memory bank store and update the L survival paths and the associated path metrics.

Considering the design of memory bank is straightforward, in this section we focus the discussion on f g units, MCU and sorting block.

![Overall Architecture of LLR-SCL Decoder](image)

**Fig. 6.** The overall architecture of LLR-SCL decoder.

B. Processing element (PE) for LLR-based f and g units

As shown in Fig. 6, the LLR-SC component decoder consists of multiple processing elements (PEs). Each PE contains an LLR-based f unit and an LLR-based g unit. Since the functions of these two units have been described in equations (6)(7), hence the architecture of a q-bit PE is developed as shown in Fig. 7. Here C2S and S2C represent the conversion blocks between 2’s complement and sign-magnitude forms. The detail of LLR-based PE can be referred to [5].

![Architecture of q-bit LLR-based PE](image)

**Fig. 7.** The architecture of q-bit LLR-based PE, cited from [5].

C. Metric Computation Unit (MCU)

(14)-(17) describe the function of MCU. Since for each decoded bit u_i, either c or d can be input to the MCU, we use inputLLR to represent these for convenience. Then, according to (14)-(17), the q-bit architecture of MCU is developed as shown in Fig. 8.
D. Sorting block

Recall that the sorting block is used to compare those metrics and select the $L$ paths with larger metrics. Here we use the batcher odd-even merge algorithm [6] to perform sorting function. Fig. 9 is an example architecture for 8-input sorting. Here C&S unit represents the compare and swap operation. It can be seen that for the example 8-input sorting block its critical path delay is $1+2+3=6 T_{CAS}$, where $T_{CAS}$ is the critical path delay of C&S unit. In general, for $2^i$-input sorting block, the critical path delay is $1+2+...+i=(i+1)i/2 T_{CAS}$, and it is also the critical path delay of the overall LLR-SCL decoder.

VI. CONCLUSION

This paper presents LLR-based SCL decoding algorithm and hardware architecture. Analysis results show that the proposed LLR-SCL decoder has very low hardware complexity and is suitable for current LLR-based systems.

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