Sub-kT/q Subthreshold-Slope Using Negative Capacitance in Low-Temperature Polycrystalline-Silicon Thin-Film Transistor

Jae Hyo Park1,2, Gil Su Jang1,2, Hyung Yoon Kim1,2, Ki Hwan Seok1,2, Hee Jae Chae1,2, Sol Kyu Lee1,2 & Seung Ki Joo1,2

Realizing a low-temperature polycrystalline-silicon (LTPS) thin-film transistor (TFT) with sub-kT/q subthreshold slope (SS) is significantly important to the development of next generation active-matrix organic-light emitting diode displays. This is the first time a sub-kT/q SS (31.44 mV/dec) incorporated with a LTPS-TFT with polycrystalline-Pb(Zr,Ti)O3 (PZT)/ZrTiO4 (ZTO) gate dielectrics has been demonstrated. The sub-kT/q SS was observed in the weak inversion region at −0.5 V showing ultra-low operating voltage with the highest mobility (250.5 cm2/Vsec) reported so far. In addition, the reliability of DC negative bias stress, hot carrier stress and self-heating stress in LTPS-TFT with negative capacitance was investigated for the first time. It was found that the self-heating stress showed accelerated SS degradation due to the PZT Curie temperature.

Almost 40 years have passed since several groups first demonstrated the amorphous-Si (a-Si) thin-film transistor (TFT) on a glass substrate1–4. It was successful in encouraging the mass-production of liquid crystal displays (LCDs) because of its simple and low-thermal budget. However, it is now limited for use in the active-matrix organic light-emitting diode (AMOLED) display, which is considered the next generation display. To address the poor electrical properties of the TFT, such as low current density, low field-effect mobility and high power dissipation, the low-temperature polycrystalline-Si (LTPS) TFT was introduced to continue the development of AMOLED displaysx4–9. However, the ongoing stringent performance and scaling of TFT will eventually be limited in the near future10,11. Although the LTPS-TFT shows a relatively higher electrical performance than the a-Si TFT, LTPS-TFT still has issues of unreliability and high voltage operation, which is believed to have originated from the grain boundary12–14. It was previously reported that the high power dissipation or high voltage operation can be significantly reduced if the high-k dielectric is incorporated with the LTPS-TFT15–17. In addition, the operation voltages are significantly related to the subthreshold slope (SS) which is an inverse of the drain current (Ids) variation that can be obtained for a unit gate voltage (Vgs) variation. According to Boltzmann thermodynamics, the SS of an ideal Si metal-oxide-semiconductor field-effect transistor (MOSFET) cannot be lower than 60 mV/dec (~2.3 kT) at room-temperature. For the development of a capable high-k dielectric, it is significantly important that SS can reach 60 mV/dec. Recent reports demonstrate a tunneling MOSFET18–21 using the band-to-band tunneling or impact ionization and ferroelectric-gate MOSFET22–26 using negative capacitance, where the carrier transports are independent of the Boltzmann thermodynamics. In the case of tunnel MOSFETs, the electrical properties are less sensitive to the gate dielectric than ferroelectric-gate MOSFET, but are strongly sensitive to the channel defect state which may not be suitable for the high defect-state LTPS27,28. On the other hand, the ferroelectric-gate MOSFET was not sensitive to the channel defect state, but was sensitive to the negative capacitance of the gate dielectric29,30. However, in the context of semiconductor manufacturing, integrating a single-crystal ferroelectric thin-film to Si is impossible. For example, perovskite-structured SrTiO3 is an excellent substrate for the growth of high qualified crystalline BaTiO3, but cannot be used as part of a Si-based gate.
dielectric because of its undesirable reaction and negligible band offset\textsuperscript{31–33}. In order to integrate a ferroelectric thin-film in LTPS or c-Si, polycrystalline-ferroelectric thin-film needs to be used.

In this work, we developed a LTPS-TFT with ZrTiO\textsubscript{4}(ZTO)/Pb(Zr,Ti)O\textsubscript{3}(PZT) gate stacks to realize an ultra-steep SS for the first time. Using the negative capacitance in PZT, the SS was 38.2 mV/dec, which is the best SS in LTPS-TFT reported so far. The concept of using negative capacitance is consistent with the Landau-Khalatnikov (L-K) equation. Moreover, the reliability was investigated under DC positive-bias stress, hot-carrier stress and self-heating stress.

**Results and Discussion**

According to an ideal Si-based MOSFET, the SS is defined as:\textsuperscript{34}

\[ SS = -\frac{\partial V_g}{\partial (log I_d)} = -\frac{\partial V_g}{\partial \psi_s} \cdot \frac{\partial \psi_s}{\partial (log I_d)} = m \times n = \left( 1 + \frac{C_s}{C_{inv}} \right) \frac{kT}{q} \ln 10 \]

where $\psi_s$ is the surface potential of Si, $C_s$ is the Si capacitance and $C_{inv}$ is the gate insulator capacitance. Note that $I_d$ is restricted to the $kT \ln 10/q$ term because the carrier transport diffusion is limited to the Boltzmann thermodynamics. If $C_s/C_{inv}$ reaches 0, the SS would be 60 mV/dec at room temperature. In order words, this minimum SS puts a fundamental lower limit on the operating voltage and power dissipation. In fact, it is impossible for $C_s/C_{inv}$ to reach 0 because the $C_{inv}$ cannot be infinite. $C_{inv}$ is a series of the multi-stack dielectrics where $C_{ZTO}$ and $C_{PZT}$ in our case are in equivalent circuits as shown in Fig. 1a:

\[ \frac{1}{C_{inv}} = \frac{1}{C_{ZTO}} + \frac{1}{C_{PZT}} \]

where $C_{ZTO}$ was 2.21 pF/m\textsuperscript{2} with 2-nm thickness and $C_{PZT}$ was 62.66 pF/m\textsuperscript{2} with 200-nm thickness. Thus, $C_{inv}$ was 2.13 pF/m\textsuperscript{2}, which is not infinite. This confirms that the ferroelectric-gate MOSFET is related to the m-factor determined by the $\psi_s$ and capacitance while, the tunneling MOSFET is related to the n-factor. Generally, the m-factor has a limited value in the range from 0 to 1, but this limited range is not considered when the capacitance is negatively expressed, as in the equation:
when the $C_{ZTO}$ becomes negative, equation (3) becomes:

$$0 < m \left(1 + \frac{C_{ZTO} + C_{PZT}}{C_{ZTO}C_{PZT}}\right) < 1$$

The $m$-factor eventually becomes a negative value ranging from $-1$ to $0$. Thus, the surface potential could be amplified to achieve SS less than 60 mV/dec. As shown in Fig. 1a, the LTPS-TFT with the PZT/ZTO gate stacks is well formed with a smooth interface with PZT/ZTO and ZTO/LTPS, as observed from high-resolution transmission microscopic images (HR-TEM). The PZT and ZTO were crystallized by rapid thermal annealing (RTA) for 30 sec at 600 °C in air ambient. The crystallized PZT and ZTO showed various crystal planes observed from the x-ray diffraction (XRD) 2-theta profile (Fig. 1b). The PZT showed perovskite-structured with (100), (111) and (200) orientated textures. When using crystallized PZT on top of Si, it is important to prevent the interdiffusion of Pb elements because of the undesirable reaction between PZT and Si. The role of thin ZTO is to block the Pb diffusion during the crystallization. Although the Pb element can be perfectly blocked in a thick-ZTO, a thick ZTO shows a large charge compensation loss which could easily depolarize the PZT. Unfortunately, a depolarization field ($D_{de}$) is always present when the PZT is used in a metal-ferroelectric-insulator-semiconductor (MFIS) structure. The depolarization field in the MFIS structure can be expressed as:

$$E_{de} = \frac{PC_{PZT}}{C_{ZTO} + C_{PZT}} = P\left(\frac{1}{\varepsilon(C_{ZTO}/C_{PZT})} + 1\right)$$

Here, $P$ is the polarization dipole moment and $\varepsilon$ is the PZT dielectric constant. It is found that the minimum thickness of ZTO with a maximum inter-diffusion barrier needs to be determined in order to reduce the $E_{de}$. The thickness of 2 nm is the optimized minimum ZTO. The atomic percentage measured by auger electron spectroscopy (AES) is shown in Fig. 1c. A large Pb element with high percentage was observed in the interface of ZTO, whereas it significantly dropped to 0% in the center of the ZTO thin-film. It is confirmed that even a 2.5-nm thick ZTO is sufficient for preventing the diffusion of Pb toward Si. This result is consistent with the energy-dispersive x-ray spectroscopy (EDS) images shown in the inset in Fig. 1a. To address these material characteristics, the buffer layer needs to be reduced to 1 nm to realize the full potential of the ferroelectric-gate MOSFET.

To understand the negative capacitance in PZT, the capacitance in terms of energy ($U$) is shown in Fig. 2. $U$ can be expressed in terms of a variation in $U$ as a function of a variation in stored charges ($Q_f$):

$$C = \left(\frac{\partial^2 U}{\partial Q_f^2}\right)^{-1}$$

From the equation, a quadratic relation occurs between $U$ and $Q_f$. Some materials, known as paraelectric materials, show a nonlinear $P$ as a function of the electric field, which implies that $U$ and $P$ have a slight possibility of having a single point corresponding to $P = 0$. In the case of the initial state $P$, the $U$ landscape is tilted and induces the polarized dipoles to move to the nearest minimum $U$ when a voltage is applied to the Pt gate (Fig. 2a). In this situation, it is difficult to observe a negative capacitance. After applying more voltage to the Pt gate, but
less than the PZT coercive voltage \( (E_c) \), the polarization dipole would move to the \( P = 0 \) point with balancing \( U \) (Fig. 2b). If the voltage is larger than the PZT \( E_c \), the polarization will move to the other side of the remaining minimum energy (Fig. 2c). This implies that the negative capacitance will descend when the PZT is more biased than the \( E_c \). Therefore, the PZT has a strong possibility of passing through the negative differential capacitance. In addition, the total capacitance (PZT + ZTO) should be stabilized in series with the paraelectric and ferroelectric capacitors. The negative capacitance of a single-layer of ferroelectric could not be observed.

Figure 3a shows the \( Q_{fe} - E_{eff} \) characteristics of \( Pt/PZT(100-nm)/ZTO(2-nm)/LTPS \) and \( Pt/ZTO(102-nm)/LTPS \). The capacitor with PZT showed a clear saturation remnant polarization \( (P_r) \) and large \( E_c \), while the capacitor without PZT showed no \( P_r \) or \( E_c \). The Landau-Khalatnikov (L-K) model is applied to the P-E data, giving the \( Q_{fe} - E_{eff} \) relation:

\[
\alpha \beta \gamma = + \begin{cases} \alpha & \beta & \gamma \\ E_p & P & P \end{cases} 24 6 (7) \]

where \( \alpha, \beta \) and \( \gamma \) are the material dependent constants. The \( \alpha, \beta \) and \( \gamma \) were obtained as \( 4.82 \times 10^{8} \ \text{m/F}, \ 4.1 \times 10^{8} \ \text{m/F/C}^2 \) and \( 4.8 \times 10^{8} \ \text{m/10/F/C}^4 \), respectively. This constant is consistent with the other epitaxial-PZT. These results are the proof of negative capacitance in PZT. As shown in Figs 2 and 3a, starting from the initial \( P \), as a voltage is applied across the ferroelectric capacitor, the energy landscape is tilted and the polarization will move to the nearest local minimum. During this mechanism, the negative capacitance spontaneously appears. This transition respect to the voltage appears when the applied voltage is smaller than coercive voltage \( (V_c) \). If the gate voltage is larger than \( V_c \), one of the minima energy potential disappears and \( Q_r \) moves to the remaining minimum of the energy. In other word, the negative capacitance is vanished when the gate voltage is larger than \( V_c \).

In our case, the \( V_c \) of PZT was \( -0.5 \) to \( 0.5 \) V indicating the negative capacitance range. Increasing the \( V_g \) above \( 0.5 \) V shows normally positive capacitance. Fortunately, the system of our PZT/ZTO/LTPS stacked TFT shows a subthreshold region and weak inversion. The general chemical formula for PZT-perovskite compounds is \( ABO_3 \), where 'A' and 'B' are two cations of different sizes and X is an anion that both to both A and B. Typically, the 'A' atoms are larger than the 'B' atoms. In the PZT system, 'A' corresponds to Pb atom, 'B' corresponds to Zr and Ti atoms and 'O' was oxygen atom. The ideal cubic-symmetry structure has B cation in 6-fold coordination, surrounded by an octahedron of anions and the A cation in 12-fold cub-octahedral coordination. According to the crystal structure of PZT, the Zr and Ti atoms move up-and-downward depending on the electrical field. These movements form polarization dipoles. As a result, it is possible to create a negative capacitor by tuning the polarization by Zr and Ti atoms. Moreover, the increasing voltage induces the opposite polarity to the Si channel.

Figure 3. (a) \( Q_{fe} - E_{eff} \) measurements of \( Pt/PZT(100-nm)/ZTO(2-nm)/LTPS \) and \( Pt/ZTO(102-nm)/LTPS \) and its Landau-Khalatnikov (L-K) fitting. (b) \( I_{ds} - V_{gs} \) measurements at \( V_{ds} = -0.1 \) V and \( W = L = 3.5/2 \) \( \mu \)m. The C-V characteristic is shown in inset figure. (c) Steep switching during turn on observed in weak inversion region. (d) \( I_{ds} - V_{ds} \) characteristics with 7 steps of \( V_{gs} \) from 0 to \( -15 \) V.
These polarizations behave nonlinearly, meaning that small increments in the voltage can lead to disproportionate changes in the PZT polarization. It is mainly reported that PZT have a spontaneous polarization that flips above a certain critical voltage which is \( V_p \), yielding an enormous and sudden accumulation of bound charge at the poly-Si surface\(^{44-46} \). Previously, Salahuddin et al. confirmed that PZT ferroelectric ‘negative-capacitance’ state maintains only for as long as the ferroelectric polarization is switching and remained unscreened\(^{47} \). To prevent the screening, an insulator (in our case ‘ZTO’) is inserted at the interface between the ferroelectric and poly-Si (Figure S1). There were already some experimental demonstration of negative capacitance based on the PZT\(^{48,49} \). Figure 3b shows the \( I_{ds}-V_{gs} \) characteristics of the Pt/PZT/ZTO/LTPS device at \( V_{ds} = 0.1 \) V to measure the SS. The SS of LTPS-TFT showed 31.44 mV/dec at the upper curve and 37.73 mV/dec at the lower curve. Both curves of SS are observed not at low \( V_{gs} \) but at high \( V_{gs} \), which is a weak inversion region (Fig. 3c). The off-current is observed at \( 10^{-8} \) A/\( \mu \)m with hysteresis of 0.26 V. The charges for strong inversion are formed at approximately 0.25 V, which is the lowest operation voltage of LTPS reported so far. In the inset figure, the negative capacitance having \( -0.5 \) pF/cm\(^2\) was observed in the weak inversion region near the \( V_{gs} = 0.25 \) V measured at 100 kHz. Moreover, we have measured the capacitance-frequency curves where the frequency was swept from 100 Hz to 1 MHz at\( V_{gs} = 0 \) and \( -0.5 \) V. It was confirmed that the negative capacitance values were observed in all frequency spectrum (Figure 2S).

The value of negative capacitance has started to decrease and almost showed saturation. We believe that the deep depletion originated from the high-frequency in the LTPS channel affects the total capacitance. This experiment confirms that the sub-\( kT/q \) SS is obtained when the \( V_{gs} \) ranges from \( 0.5 \) to 0 at the upper curve and from \( 0.3 \) to 0.5 at the lower curve. Both curves of SS are observed not at low \( V_{gs} \) but at high \( V_{gs} \), which is a weak inversion region (Fig. 3c). In addition, the \( I_{on}/I_{off} \) ratio was \( 1.1 \times 10^5 \) at \( V_{ds} = 0.1 \) and was increased to \( 1.0 \times 10^6 \) at \( V_{ds} = -1 \) V. The \( I_{ds}-V_{ds} \) characteristics are shown in Fig. 3d. The LTPS-TFT showed clear saturation even at a \( -1 \) V of low \( V_{ds} \) and a good ohmic contact was observed in the linear region. No kink or snap-back effect was observed in our LTPS-TFT, which is important to drive the AMOLED displays\(^{50,51} \). The saturation field-effect mobility (\( \mu_{fe} \)) that is independent of \( V_{ds} \) was obtained from the following expression:

\[
I_{ds,SAT} = \frac{W}{2L} \mu_{fe} C_{ox} \left( V_{gs} - V_{th} \right)^2
\]

The square root of the saturation current is linearly dependent on the \( V_{gs} \), and the \( \mu_{fe} \) can be extracted from the slope of \( I_{ds, SAT} \) vs \( V_{gs} \) curve. The \( \mu_{fe} \) was 250.5 cm\(^2\)/Vsec, which is the highest mobility in LTPS-TFT\(^{52-54} \). We can estimate that \( \mu_{fe} \) strongly depends on \( C_{ox} \). In the device, the \( C_{ox} \) with the use of PZT/ZTO is much higher than that of typical SiO\(_2\) due to the high dielectric constant of PZT (\( \varepsilon_r \sim 1050 \)).

One of the important characteristics of the LTPS-TFT is its reliability. It has been identified that the LTPS-TFT has three main degradation mechanisms under DC bias-stress, hot-carrier stress and self-heating stress. Figure 4a shows the degradation of LTPS-TFT with negative capacitance as a function of the DC negative bias-stress. The \( -10 \) V of the DC negative bias was applied at the Pt gate and grounding of the S/D. From our result, SS was slightly increased after stress for 100 sec, with a slight decrease to 90% of the on-current. Applying \( -10 \) V to the Pt-gate shows a strong inversion of hole carriers at the interface between ZTO and LTPS. These inversion carriers strongly influence the interface state, trap state generation and fixed charge formation originating from the depapsulation of the weak Si-H bonds located at the interface of the grain boundaries\(^{55-57} \). The increase in the number of interfacial traps and the increased depolarization field, which are generated by the broken hydrogen atoms, might...
are combined with two paraelectric capacitors. 

Thus, it is observed unless it is electrically biased to tilt the U at room-temperature (300 K). In Fig. 5b, the total capacitance of (PZT - PZT) remains. (b) At 300 K, PZT as a ferroelectric and ZTO as a paraelectric capacitor, where the total capacitance (PZT + ZTO) is dominated in the paraelectric capacitor. (c) At 500 K, both PZT and ZTO are combined with two paraelectric capacitors.

Figure 5. Energy density as a function of temperature in ZTO (green curve, 1), PZT+ZTO (red curve, 3) and PZT (yellow, 2). (a) At 100 K, PZT as a ferroelectric and ZTO as a paraelectric capacitor where the total capacitor (PZT+ZTO) remains. (b) At 300 K, PZT as a ferroelectric and ZTO as a paraelectric capacitor, where the total capacitance (PZT + ZTO) is dominated in the paraelectric capacitor. (c) At 500 K, both PZT and ZTO are combined with two paraelectric capacitors.

be the main source of SS degradation. Figure 4b shows the degradation in the hot-carrier (HC) stress. The Pt gate was biased at −1 V for the strong inversion without any damage to the interface and Vds was biased to −10 V. The carrier is exposed to a high electrical field in the near drain junction; it therefore gains enough energy to become HC, creating a defect and carrier injection in the PZT at the grain-boundary near the drain junction. This shows that the on-current decreased to 70% and the SS has slightly decreased to 40 mV/dec after stress for 10³ sec. Damaging the interface near the drain junction is significantly related to the on-current because of the pinch-off phenomenon, whereas the SS is not strongly affected because the injected charges are insufficient and could become trapped in the ZTO, thus diminishing the negative capacitance. In addition, for conventional LTPS-TFTs with SiO₂ gate dielectric, the shorter channel length induces larger HC degradation, which is attributed to the higher electric field for the shorter channel length. The degradation of self-heating stress is shown in Fig. 4c. The self-heating stress was performed at −0.5 V of Vgs and 70 μW/μm² (Vgs x Jds = −1 V x −7 × 10⁻⁷ A/μm²). In contrast to the DC negative-bias-stress, the self-heating stress combined with high electric field and high power could distort the strong Si-Si bonds located in the entire channel grain boundary [66-67]. It has been reported that grains with high angle-grain boundary and microtwins intensify the degradation. Unlike the conventional LTPS-TFT with SiO₂ dielectrics, the LTPS-TFT with ferroelectric dielectric is more seriously degraded because of its temperature-dependent polarization. Self-heating stress generates Joule heat and degrades the whole interface and grain boundaries. To alleviate the self-heating stress, an effective method is to dissipate the heat quickly in the substrate. Ferroelectric materials exhibit a spontaneous electric polarization below a critical temperature. However, the negative capacitance will be unstable or not observable and eventually PZT would be paraelectric in the high temperature caused by the self-heating stress. The Joule heat can increase to about 500 K in LTPS with 120 μW/μm². As shown in Fig. 5a, the total capacitance (PZT + ZTO) shows ferroelectric properties as indicated by the two negative minimum U points. It is found that the negative capacitance is unstable or not observed unless it is electrically biased to tilt the U at room-temperature (300 K). In Fig. 5b, the total capacitance (PZT + ZTO) shows a stable point in the negative capacitance U and ferroelectric properties. The roles of the two layers are ferroelectric in PZT and paraelectric in ZTO. However, the total capacitance of (PZT + ZTO) changed to the paraelectric capacitor because the temperature is above the Curie temperature of PZT (Fig. 5c). Thus, it is not possible to observe a negative capacitance.

For over a decade, several groups have attempted to improve the μfe and SS in LTPS. Starting from SiO₂ (εr = 3.9)[68], which is known as the most stable and perfect interface between Si among the other oxides, dielectrics with Si₃N₄, Al₂O₃, Y₂O₃, Eu₂O₃, ZrTiO₃ and HfO₂, etc. were developed and a steep SS was successfully realized, reaching up to 60 mV/dec (Fig. 6). However, a larger dielectric constant is needed to reach 60 mV/dec. Although some ultra-high-k dielectrics such as TiO₂ (80–100) [69], SrTiO₃ (200–300) [70], and BaSrTiO₃ (1000–1250) [71] have been attempted, they cannot be used with the LTPS-TFT because of its high gate current, poor thermal stability and rare-earth elements. Thus, using PZT with a ZTO buffer layer shows good gate stacks for realizing the high performance LTPS-TFT.

Conclusion

In summary, we successfully demonstrated for the first time a sub-kT/q SS (31.44 mV/dec) incorporating a negative capacitance in LTPS-TFT. The total structure of the proposed LTPS-TFT was Pt (200 nm)/PZT(100 nm)/ZTO(2 nm)/LTPS(50 nm) in a p-type channel. We systematically investigated the negative capacitor as a function of energy and stored charges to explain a way to achieve a sub-kT/q SS (<60 mV/dec). Moreover, the reliability of DC negative bias stress, hot-carrier stress and self-heating stress was measured. Unlike the conventional LTPS-TFT with SiO₂ gate dielectrics, the LTPS-TFT with PZT/ZTO showed a significant SS degradation on the self-heating stress because the PZT showed paraelectric properties rather than ferroelectric properties. It can be concluded that the performance of LTPS-TFT using negative capacitance can be realized by true low power LTPS-TFT for future AMOLED displays.
Methods

Fabrication. LTPS-TFT using negative capacitance structure was fabricated on glass substrate (Corning Eagle XG, 100 × 100 mm²). The total structure was Pt(200 nm)/PZT(100 nm)/ZTO(2 nm)/LTPS/(200 nm)SiO₂/glass as shown in Fig. 1a. The fabrication process begins with depositing a 50-nm-thick a-Si on a 200-nm-thick SiO₂ coated glass substrate. The a-Si was then crystallized with 5-nm thick Ni for metal-induced lateral crystallization (MILC) by annealing at 550 °C for 2 hrs in H₂ ambient. The detailed MILC conditions and mechanism have been reported elsewhere75,76. After the crystallization, the LTPS surface was subsequently cleaned with RCA1 (NH₄OH:H₂O₂:D.I=5:1:1), RCA2 (HCl:H₂O₂:D.I=6:1:1) and piranha solution (H₂SO₄:H₂O₂:D.I=3:2:1) to remove the Ni and residual defects. A 2-nm-thick ZrTiO₄ (ZTO) was deposited by RF reactive magnetron sputtering using a single composite target (99.999% purity) with O₂:Ar=10:1 at 200 °C. A 100-nm-thick Pb(Zr, Ti)O₃ (PZT) was subsequently deposited using a single composite target (PbZr₀.₅₂Ti₀.₄₈O₃, 99.9999% purity) with O₂:Ar=10:1 at 200 °C. After the deposition, the ZTO/PZT was crystallized using a 0.5-sec Xe-lamp pulse at 700°C in air ambient. The crystallization is confirmed by the XRD profile (Fig. 1b). Next, a 200-nm-thick Pt gate electrode was deposited by DC magnetron sputtering at room-temperature. The Pt/ZTO/ZTO was patterned for the self-aligned source and drain B₂H₆ doping. Boron dopants were implanted at accelerating voltages of 17 keV and RF power of 150 W. Finally, the dopant was electrically activated by annealing for 2 hr in H₂ ambient. The whole fabrication process was carried out in a 1000-class clean room (Eui-San Research Center, Seoul National University).

Measurement. The measurements for electrical properties and capacitance properties were carried out by E5270B semiconductor analyzer (Agilent Technologies) and 4284A precision LCR meter (Agilent Technologies, Inc.). In addition, the Qᵥ/Eᵥ measurements were performed by RT66A (Radiant Technologies, Inc.).

Characterization. The crystal orientations of PZT/ZTO were measured by XRD (PANalytical, X’pert Pro). The cross-sectional image was observed by high-resolution transmission electron microscopic image (JEOL, JEM-2100F).

References
1. A. J. Sneel et al. Application of amorphous silicon field effect transistors in addressable liquid crystal display panels. Appl. Phys. A 24, 357–362, doi: 10.1007/BF00899734 (1981).
2. K. D. Mackenzie et al. The characteristics and properties of optimized amorphous silicon field effect transistors. Appl. Phys. A 31, 87–92, doi: 10.1007/BF00616310 (1983).
3. J. M. Powell. The physics of amorphous-silicon thin-film transistor. IEEE Trans. Electron Devices 36, 2753–2763 doi: 10.1109/16.40933 (1989).
4. M. Shur, M. Hack & J. G. Shaw. A new analytic model for amorphous silicon thin-film transistors, J. Appl. Phys. 66, 3371 (1989).
5. M. K. Hatalis & D. W. Greve. Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited amorphous silicon films. J. Appl. Phys. 63, 2260 doi: 10.1063/1.341065 (1988).
6. S. Uchikoga. Low-temperature polycrystalline silicon thin-film transistor or technologies for system-on-glass displays. MRS Bull. 27, 881–886 doi: 10.1557/mrs2002.277 (2002).
7. G. Liu & S. J. Fonash. Polycrystalline silicon thin film transistors on corning 7059 glass substrate using short time, low-temperature processing. Appl. Phys. Lett. 62, 2254 doi: 10.1063/1.109294 (1993).
8. S.-W. Lee & S.-K. Joo. Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization. IEEE Electron Device Lett. 17, 160–162 doi: 10.1109/55.485160 (1996).
9. T. Serikawa, S. Shirai, A. Okamoto & S. Suyama. Low-temperature fabrication of high-mobility poly-Si TFTs for large-area LCDs. IEEE Trans. Electron Devices 36, 1929–1933 doi: 10.1109/16.34272 (1989).
10. A. Kumar, A. Nathan & G. E. Jabbour. Does TFT mobility impact pixel size in AMOLED backplanes? IEEE Trans. Electron Devices 52, 2386–2394 doi: 10.1109/TED.2005.857937 (2005).
11. Gu G & S. R. Forrest. Design of flat-panel displays based on organic light-emitting devices. **IEEE J. Sel. Top. Quantum Electron.** 4, 83–99 doi: 10.1109/29.669473 (1998).

12. C.-Y. Chen et al. Negative bias temperature instability in low-temperature polycrystalline silicon thin-film transistors. **IEEE Trans. Electron Devices** 53, 2993–3000 doi: 10.1109/TED.2006.885543 (2006).

13. C.-Y. Chen et al. A reliability model for low-temperature polycrystalline silicon thin-film transistors. **IEEE Electron Device Lett.** 28, 192–194 doi: 10.1109/LED.2007.895454 (2007).

14. M.-W. Ma et al. Characteristics of PBTI and hot carrier stress for LTPS-TFT with high-k gate dielectric. **IEEE Electron Device Lett.** 29, 171–173 doi: 10.1109/LED.2007.914091 (2008).

15. T.-M. Pan et al. High-performance poly-silicon TFTs using a high-k PtTiOx gate dielectric., **IEEE Electron Device Lett.** 30, 39–41 doi: 10.1109/LED.2008.280449 (2008).

16. L.-C. Yen et al. Electrical and reliability characteristics of polycrystalline silicon thin-film transistors with high-k Ea3Ox gate dielectrics. **Appl. Phys. Lett.** 100, 173509 doi: 10.1063/1.4705472 (2012).

17. M. J. Lee & W.-Y. Choi. Analytical model of single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs). **Solid-State Electron.** 63, 110–114 doi: 10.1016/j.sse.2011.05.008 (2011).

18. N. Ershov et al. Vertical Si-nanowire n-type tunneling FETs with low subthreshold swing (< 50 mV/decade) at room temperature. **IEEE Electron Device Lett.** 32, 437–439 doi: 10.1109/LED.2011.2106757 (2011).

19. M. T. Bjork et al. Silicon nanowire tunneling field-effect transistors, **Appl. Phys. Lett.** 19, 193504–193506 doi: 10.1063/1.3298227 (2008).

20. V. V. Zhirnov & R. V. Cavin. Nanoelectronics: negative capacitance to the rescue? **Nat. Nanotechnol.** 7, 77–78 doi: 10.1038/nnano.2008.18 (2008).

21. G. A. Salvatore et al. Experimental confirmation of temperature dependent negative capacitance in ferroelectric field effect transistor. **Appl. Phys. Lett.** 100, 163504 doi: 10.1063/1.4704179 (2012).

22. D. J. R. Appleby et al. Experimental observation of negative capacitance in ferroelectrics at room temperature. **Nano Lett.** 14, 3864–3868 doi: 10.1021/nl5037255 (2014).

23. C. M. Krowne et al. Examination of the possibility of negative capacitance using ferroelectric materials in solid-state electronic devices. **Nano Lett.** 11, 988–988 doi: 10.1021/nl1037215 (2011).

24. D. Jimenez, E. Miranda & A. Godoy. Potential and drain current in negative capacitance field-effect transistors. **IEEE Trans. Electron Devices** 57, 2405–2409 doi: 10.1109/TED.2010.2062188 (2010).

25. Y.-H. Chen et al. Low-temperature polycrystalline silicon tunneling thin-film transistor with MILC. **IEEE Electron Device Lett.** 34, 1017–1019 doi: 10.1109/LED.2013.2266331 (2014).

26. M.-H. Jaung, P.-S. Hu & S.-L. Jang. Formation of polycrystalline-Si thin-film transistors with tunneling field-effect structure. **Thin Solid Films** 518, 3978–3981 doi: 10.1016/j.tsf.2009.11.017 (2010).

27. G. Catalan et al. Ferroelectrics: negative capacitance detected. **Nat. Mater.** 14, 137–139 doi: 10.1038/nmat4195 (2015).

28. W. Gao et al. Room-temperature negative capacitance in a ferroelectric-dielectric superlattice heterostructure. **Nano Lett.** 14, 5814–5819 doi: 10.1021/nl502691u (2014).

29. K. Shimoyama et al. Room-temperature negative capacitance in a ferroelectric-dielectric superlattice heterostructure. **Nano Lett.** 14, 1017–1019 doi: 10.1021/nl304356j (2014).

30. A. I. Khan et al. Room-temperature negative capacitance in a ferroelectric-dielectric superlattice heterostructure. **Nano Lett.** 14, 1017–1019 doi: 10.1021/nl304356j (2014).

31. K. Shimoyama et al. Epitaxial growth of BaTiO3/SrTiO3 structure on SrTiO3 substrate with automatic feeding oxygen from the substrate. **J. Appl. Phys.** 92, 4625–4630 doi: 10.1063/1.1506196 (2002).

32. V. Visinioiu et al. Initial growth stages of epitaxial BaTiO3 films on vicinal SrTiO3 (001) substrate surfaces. **J. Appl. Phys.** 91, 1015–1017 doi: 10.1063/1.1478800 (2002).

33. B. D. Qu et al. Dielectric properties of BaTiO3/SrTiO3 multilayered thin-films prepared by pulsed laser deposition. **Appl. Phys. Lett.** 72, 1394 doi: 10.1063/1.1210666 (1998).

34. D. J. Wouters et al. Vertical-Si nanowire tunneling field-effect transistors. **IEEE Trans. Electron Devices** 37, 2022 doi: 10.1109/16.571665 (1990).

35. N. R. Parkh, J. T. Stephen, M. L. Swanson & E. R. Myers. Study of diffusion barrier for PZT deposited on Si for non-volatile random-access memory technology. **MRS Proc.** 200, 10 doi: 10.1557/PROC-200-193 (1990).

36. J. H. Park et al. Fabrication of metal/ferroelectric/insulator-semiconductor field effect transistor using Mo/Pb(Zr,Ti)O3/Pb(Zr,Ti)O3/poly Si thin film structure. **Integr. Ferroel.** 49, 13–20 doi: 10.1080/10584580290171720 (2002).

37. H.-T. Lue, C.-J. Wu & T.-Y. Tseng. Device modeling of ferroelectric field-effect transistor (FeFET). **IEEE Trans. Electron Devices** 49, 1799–1798 doi: 10.1109/TED.2002.803626 (2002).

38. J. Sun et al. Interface effects on the characteristics of metal-ferroelectric-insulator-semiconductor field-effect transistor. **J. Semi. Sci. Technol.** 26, 095027 doi: 10.1088/0268-1242/26/9/095027 (2011).

39. T. P. Ma & J.-P. Han. Why is nonvolatile ferroelectric memory field-effect transistor still elusive? **IEEE Electron Device Lett.** 23, 386–388 doi: 10.1109/LED.2002.1015020 (2002).

40. V. L. Chau et al. Nonvolatile, all-electrical nanoscale memory devices. **IEEE J. Explor. Solid-State Computat. Devices Circuits** 10, 43–48 doi: 10.1109/XSCDC.2015.2448414 (2015).

41. S. Inoue & T. Shimoda. Investigation of relationship between hot carrier degradation and kink effect in low temperature poly-Si TFETs. **SID Int. Symp. Dig. Tech.** 30, 452–455 doi: 10.1889/1.834054 (1999).

42. M.-K. Kang, K. Uhr & H. G. Kim. Invited paper: Advanced technologies based on a Si-oire PZT (low-temperature poly Si) TFT (thin film transistor) for high performance mobile display. **SID Int. Symp. Dig. Tech.** 38, 1262–1265 doi: 10.1889/1.2785541 (2007).
Temperature Polycrystalline-Silicon Thin-Film Transistor. Sub-kT/q Subthreshold-Slope Using Negative Capacitance in Low-

Author Contributions
J.H.P. and S.K.J. conceived and designed the experiments. J.H.P., G.S.J., K.H.S., H.J.C. and S.K.L. performed the fabrication. J.H.P. analyzed the performance and H.Y.K. analyzed the material characteristics. J.H.P. and S.K.J. interpreted the data and provided fruitful discussion all the coauthors.

Additional Information
Supplementary information accompanies this paper at http://www.nature.com/srep

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Park, J. H. et al. Sub-kT/q Subthreshold-Slope Using Negative Capacitance in Low-

Temperature Polycrystalline-Silicon Thin-Film Transistor. Sci. Rep. 6, 24734; doi: 10.1038/srep24734 (2016).

This work is licensed under a Creative Commons Attribution 4.0 International License. The images or other third party material in this article are included in the article’s Creative Commons license, unless indicated otherwise in the credit line; if the material is not included under the Creative Commons license, users will need to obtain permission from the license holder to reproduce the material. To view a copy of this license, visit http://creativecommons.org/licenses/by/4.0/.

Acknowledgements
The authors would like to thank Dr. Yoonsuk Yoon (LFoundary, Germany) for his valuable discussion. This work was supported by Seoul Nation University, Seoul, Republic of Korea, through the Eui-San Research Center and Research Institute of Advanced Materials (RIAM). In addition, this work was partially supported by Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (Grant 0417–20150112) and in part by BK21PLUS SNU Materials Division for Educating Creative Global Leaders under (Grant F15SN02D1702). The glass substrate (Eagle XG, 100 mm × 100 mm2) was provided by Corning Precision Materials Co., Ltd., Republic of Korea.

53. Y. Oana. Current and future technology of low-temperature poly-Si TFT-LCDs. SID Journal Soc. Inf. 9, 169–172 doi: 10.1889/1.1828784 (2001).
54. H. Ohshima & M. Führen. Invited paper: High-performance LTPS technologies for advanced mobile display applications. SID Int. Symp. Dig. Tech. 38, 1485–1487 (2007).
55. M.-W. Ma et al. Reliability mechanism of LTPS-TFT with HfO2 gate dielectric: PBTI, NBTI and hot-carrier stress. IEEE Trans. Electron Devices. 55, 1153–1160 doi: 10.1109/TED.2008.917910 (2009).
56. C.-Y. Chen et al. Bias temperature instabilities for low-temperature polycrystalline silicon complementary thin-film transistor. J. Electrochem. Soc. 154, H704–H707 doi: 10.1149/1.2742810 (2007).
57. D. K. Schroder. Negative bias temperature instability: What do we understand? Microelectron. Rel. 47, 841–852 doi: 10.1016/j. micrel.2006.10.006 (2007).
58. T. Grasser et al. The paradigm shift in understanding the bias temperature instability: from reaction-diffusion to switching oxide traps. IEEE Trans. Electron Devices 58, 3652–3666 doi: 10.1109/TED.2011.2164543 (2011).
59. R. A. Sporea, T. Burridge & S. R. P. Silva. Self-heating effects in polysilicon source gate transistors. Sci. Rep. 5, 1–11 doi: 10.1038/ srep14058 (2015).
60. S. Inoue, S. Takanaka & T. Shimoda. Study of degradation phenomenon due to a combination of contamination and self-heating in poly-Si thin film transistors fabricated by a low-temperature process. Ipn. J. Appl. Phys. 42, 4213–4217 doi: 10.1143/JJAP.42.4213 (2003).
61. K. Takechi et al. Dependence of self-heating effects on operation conditions and device structure for polycrystalline silicon TFTs. IEEE Trans. Electron Devices. 53, 251–257 doi: 10.1109/TED.2005.861729 (2006).
62. C. L. Wang, W. L. Zhong & P. L. Zhang. The curie temperature of ultra-thin ferroelectric films. J. Phys.: Condens. Matter. 3, 4743–4749 (1992).
63. S. C. Abrahams, S. K. Kurtz & P. B. Jamieson. Atomic displacement relationship to Curie temperature and spontaneous polarization in displace ferroelectric. Phys. Rev. Lett. 172, 551 doi: 10.1038/PhysRevLett.172.551 (1966).
64. B. Wang & C. H. Woo. Curie temperature and critical thickness of ferroelectric thin films. J. Appl. Phys. 97, 084109 doi: 10.1063/1.1861517 (2005).
65. E. H. Nicollian & A. Goetzberger. The Si-SiO2 interface–Electrical properties as determined by the metal-insulator-silicon conductance technique. Bell System Tech. J. 46, 1055–1133 doi: 10.1002/j.1538-7904.1967.tb01727.x (1967).
66. N. Lustig & J. Nanicki. Gate dielectric and contact effects in hydrogenated amorphous silicon-silicon nitride thin-film transistors. J. Appl. Phys. 65, 3951 doi: 10.1063/1.343361 (1989).
67. Z. Jin et al. High-performance polycrystalline SiGe thin-film transistors using Al2O3 gate insulators. IEEE Electron Device Lett. 19, 502–504 doi: 10.1109/55.735760 (1998).
68. T. M. Pan & C.-J. Chang High-performance polycrystalline silicon TFTs with high-k Y2O3 gate dielectrics. Semi. Sci. Technol. 26, 075004 doi: 10.1088/0268-1242/26/7/075004 (2011).
69. C.-P. Lin et al. High-performance polycrystalline-Si TFTs using HfO2 gate dielectric. IEEE Electron Device Lett. 27, 360–363 doi: 10.1109/ LED.2006.872832 (2006).
70. J. H. Park et al. High-performance poly-Si thin-film transistor with high-k ZrTiO4 gate dielectric. IEEE Electron Device Lett. 36, 920–922 doi: 10.1109/LED.2015.2462745 (2015).
71. H. Padmanabhan, N. Bhat & S. Mohan. High-performance metal-insulator-metal capacitors using europium oxide as dielectric. IEEE Trans. Electron Devices 59, 1364–1370 doi: 10.1109/TED.2012.2188329 (2012).
72. H.-S. Kim et al. Leakage current and electrical breakdown in metal-organic chemical vapor deposited TiO2 dielectrics on silicon substrate. Appl. Phys. Lett. 69, 3860 doi: 10.1063/1.117129 (1996).
73. G. W. Dietz et al. Electrode influence on the charge transport through SrTiO3 thin films. J. Appl. Phys. 78, 6113 doi: 10.1063/1.360553 (1995).
74. S. S. Kim & C. Park. Leakage current behaviors of acceptor- and donor-doped (Ba0.6Sr0.4)TiO3 thin films. Appl. Phys. Lett. 75, 2554 doi: 10.1063/1.1250755 (1999).
75. C. W. Byun et al. High-performance polycrystalline-Si thin-film transistor fabricated by novel and simple crystallization method using Ni-silicide seeds. J. Electrochem. Soc. 158, J354–J358 doi: 10.1149/2.04911jes (2012).
76. M. Miyasaka et al. In situ observation of nickel metal-induced lateral crystallization of amorphous silicon thin films. Appl. Phys. Lett. 80, 944 doi: 10.1063/1.1447014 (2002).
