TID-Effect Compensation and Sensor-Circuit Cross-Talk Suppression in Double-SOI Devices

SHUNSUKE HONDA\textsuperscript{A}, KAZUHIKO HARA\textsuperscript{A}, DAISUKE SEKIGAWA\textsuperscript{A}, BIPIN SUBEDI\textsuperscript{A}, MARI ASANO\textsuperscript{A}, NAOSHI TOBITA\textsuperscript{A}, WATARU AYAGI\textsuperscript{A}, YASUO ARAI\textsuperscript{B}, AKIMASA ISHIKAWA\textsuperscript{C}, YOSHIMASA ONO\textsuperscript{C}, ITARU USHIKI\textsuperscript{C}, SOI COLLABORATION

\textsuperscript{A}University of Tsukuba
\textsuperscript{B}High Energy Accelerator Research Organization (KEK)
\textsuperscript{C}Tohoku University

We are developing double silicon-on-insulator (DSOI) pixel sensors for various applications such as for high-energy experiments. The performance of DSOI devices has been evaluated including total ionization damage (TID) effect compensation in transistors using a test-element-group (TEG) up to 2 MGy and in integration-type sensors up to 100 kGy. In this article, successful TID compensation in a pixel-ASD-readout-circuit is shown up to 100 kGy for the application of DSOI to counting-type sensors. The cross-talk suppression in DSOI is being evaluated. These results encourage us that DSOI sensors are applicable to future high-energy experiments such as the BELLE-II experiment or the ILC experiment.

PRESENTED AT

International Workshop on SOI Pixel Detector (SOIPix2015), Tohoku University, Sendai, Japan, 3-6, June, 2015.
1 Introduction

Monolithic pixel devices utilizing a 0.2 µm fully depleted silicon-on-insulator (FD-SOI) technology have been intensively explored for various applications [1][2][3]. The main technological features in our development are use of ”bonded”-wafers fabricated by ”SmartCut™” technology by SOITEC Co.[4] and employment of commercially reliable 0.2-µm process by Lapis Semiconductor[5]. The monolithic feature is illustrated in Fig. 1 and technology characteristics of the Lapis SOI pixel process are summarized in Table 1.

Figure 1: Schematics of SOI monolithic pixel device. Two silicon substrates with different resistivities are bonded interleaved with 200-nm thick buried oxide layer (BOX) with each resistivity optimized depending on the sensor part or circuit part. The pixel implantation is made after removing the top silicon and BOX layers. The transistors are inter-connected via aluminum metal placed on top (five metal layers are available). The detector bias is applied between the backplane and the front contact (bias ring). The Buried P-Well (BPW) can suppress the back-gate effect on the front transistor circuits.

Double-SOI (DSOI) has been introduced as a solution to issues arising in application of SOI pixel sensors to high energy experiments. DSOI has an additional Si-layer (SOI2) in BOX, where the independent voltage can be applied. As the most main issue, the total ionization dose (TID) effects [6] are rather substantial in SOI since each SOI transistor is fully enclosed in oxide layers. With accumulating radiation, generated holes are trapped in BOX affecting the operation of SOI circuits [7][8][9]. The TID compensation in DSOI has been evaluated on transistor operation using test-element-group (TEG) chips up to 2 MGy and on integration-type sensors up to 100 kGy. These studies [10][11] conclude that the TID effects in SOI devices can be di-
minished sufficiently up to at least 100 kGy by compensation in DSOI, extending the radiation tolerance nearly two orders in the radiation dose. Recently we have shown the radiation tolerance can be improved further by adjusting the process parameters [12].

In this article, TID compensation in a DSOI pixel-ASD-readout-circuit is detailed, which is demonstrated successfully up to 100 kGy. The DSOI is also expected to be effective in suppression of cross-talk between sensor nodes and near-by SOI circuit, which is typical in devices with a thin BOX layer. The cross-talk suppression in DSOI is also being addressed.

2 TID Compensation in Pixel ASD-Readout

The previous studies shown in [11] demonstrated the TID compensation in overall functionality of an integration-type pixel sensor. In order to investigate further the detailed TID compensation, we evaluated TID compensation in a TEG device including amplifier-shaper-discriminator (ASD) readout circuit with the response from each stage monitored out. Such a device is for a counting-type detector applicable in high-energy experiments. The schematics of the TEG circuit is shown in Fig. 2. The circuit is designed with a readout frequency less than 1 MHz and applicable to high-energy physics experiments such as BELLE-II and ILC.

The ASD-TEG chips were irradiated up to 100 kGy with $^{60}$Co γ-rays at Takasaki Advanced Radiation Research Institute of JAEA. During the irradiation period of two days, all the chip terminals were grounded with irradiation made at room temperature. The samples were brought within four hours at room temperature, then kept at -20°C in a refrigerator except during the measurement.

At first, the functionality of each of the amplifier and the shaper, measured with
respect to VREF, is shown in Fig. 6 and Fig. 7. After the irradiation, the base-line of the output increased and exceeded beyond the dynamic range, disabling evaluation of the response curve at $V_{SOI2} = 0$ V. But similar to the case as reported in [11], applying a proper $V_{SOI2}$ can recover the lost functionality to VREF. Full recovery is not realized because a single common $V_{SOI2}$ is employed in the TEG chip where various types of transistors are having different preferred $V_{SOI2}$s depending on transistor parameters. Although much better recovery should be possible by employing multiple $V_{SOI2}$s, we determine here first appropriate ranges of $V_{SOI2}$ depending on the radiation dose to recover both the amplifier and shaper functionalities in wider dynamic range.

The ASD response to pulse-signal was evaluated by injecting step pulses into the TEG chip through a 1 pF capacitor. The response measured at pre-irradiation is shown in Fig. 8. The shaper and the discriminator outputs have FWHM time-widths of less than 1 $\mu$sec with the appropriate IIN_FB,AMP(SHP). After 100 kGy radiation, the response was also obtained with the optimized $V_{SOI2} = 12.2$ V (Fig. 9). For evaluating further dependence on the input current (IIN_FB,SHP), the FWHM time-widths of the output shaper signal are shown in Fig. 10. Even after 100 kGy, we can maintain the original 1 $\mu$sec FWHM although a larger input current (IIN_FB,SHP) is required.

Figure 2: Schematics of the ASD-TEG. The output signals from the shaper and the discriminator are measured individually. There are eight inputs (voltage or current) to tune the ASD performance. The four input currents are to generate six appropriate voltages through current mirror circuits (shown in square boxes). The total of ten voltages are explained in testing of each component of ASD (Figs. 3-5). In addition, there are other ASD circuits where individual components can be tested independently. The parameters are identical as those shown in the figure.
Figure 3: The schematics of the amplifier in ASD-TEG. The amplifier is based on a common source circuit with Krummenacher-scheme feedback and noise-suppression [13]. The input signal is injected through AIN. VREF voltage determines the input and output offsets. VB_CORE voltage generated from IIN_CORE_AMP adjusts the amplifier gain. VH_FB and VL_FB generated from IIN_FB_AMP determines the feedback current and adjusts the time-width of the output signal.

Figure 4: The schematics of the shaper in ASD-TEG. The output signal from the amplifier is sent to SIN through a 35 fF capacitor. VREF voltage determines the input and output offsets. VB_CORE (VH_FB and VL_FB) voltage(s) generated from IIN_CORE_SHP (IIN_FB_SHP) can adjust the gain (the time-width) of the shaper. The feedback current is larger in the shaper than in the amplifier.
Figure 5: The schematics of the discriminator in ASD-TEG. The discriminator has a hysteresis to avoid noise hits with two differential thresholds determined by a global threshold, VTH. The output signal is digital with 1.8 V for on-state and 0 V for off-state.

Figure 6: The response-curve to VREF in the amplifier after 100 kGy. Although the response is lost at $V_{SOI2} = 0$ V, the response is recovered by applying $V_{SOI2}$ in an appropriate range about from -5 V to -12 V.

Figure 7: The response-curve to VREF in the shaper after 100 kGy. Although the response is lost at $V_{SOI2} = 0$ V, the response is recovered by applying $V_{SOI2}$. The optimum $V_{SOI2}$ range is narrower in the shaper because larger drive currents are required and the control is more sensitive to $V_{SOI2}$. 
Figure 8: The time response of the shaper and the discriminator signals for a pre-irradiation sample. The ASD control currents and voltages are optimized. The discriminator threshold is 0.9 V.

Figure 9: The response signals from the shaper and the discriminator after 100 kGy radiation. \( V_{SOI2} = 12.2 \text{ V} \). The ASD control currents and voltages are optimized. The discriminator is 0.9 V, same as for pre-irradiation.
3 Sensor-Circuit Cross-Talk Suppression

Two TEGs named CAPTEG and XTALKTEG are being evaluated for verifying sensor-circuit cross-talk suppression in DSOI. The CAPTEG is designed for a direct measurement of capacitances between the sensor layer and the circuit layer. The design of the CAPTEG is shown in Fig. 11 with its cross section illustrated in Fig. 12. In CAPTEG, there are capacitances of three sizes made between the BPW layer as sensing-part and the SOI1 layer as the circuit-part (see Fig. 12). The measured capacitance values are shown in Fig. 14 where different $V_{SOI2}$ settings including floating are employed. The capacitance is reduced to about 50% in DSOI (floating) compared to single SOI because the SOI2 layer separates the BOX-SOI1 capacitor into two capacitors connected in serial. Fixing the SOI2 potential at lower voltages (GNDed, -1 V, ...) reduced the capacitance further. Precise modelling of this suppression mechanism requires further studies and more detailed evaluation of the phenomena.

For the case of XTALKTEG there are three capacitances arranged next to each other, where the SOI2 shielding effect of the cross-talk suppression can be evaluated taking into account of the finite resistance of the SOI2 layer. In Fig. 13, the cross section of the XTALKTEG is shown. Because of the finite SOI2 resistance, the magnitude of cross-talk varies depending on distance between the readout position and the SOI2 connection. The cross-talk magnitude is defined as the ratio of the

Figure 10: The FWHM time-widths of the shaper signal output as function of radiation dose with an optimized $V_{SOI2s}$. $V_{SOI2} = -6.0$ V at 10 kGy, -9.5 V at 50 kGy, and -12.2 V at 100 kGy.
amplitude of the BPW layer output divided by that injected into the SOI1 layer. The input signal was 0.2 V sine-wave with various frequencies. The result is shown in Fig. 15. The channel closer to the SOI2 connection has a better shielding performance as expected. The frequency dependence peaks at a certain frequency, and affects the sensor design in view of the cross-talk suppression. Therefore, although more detailed studies are needed, we can conclude that the suppression of the sensor-circuit cross-talk is effective in DSOI.

Figure 11: The design of the CAPTEG having six capacitors. Three blue boxes are capacitors made between the BPW layer and SOI1 layer with difference sizes, the largest one (CAP1) and second largest (CAP2) being three times and twice larger than the smallest one (CAP3). The size of CAP3 is 875 μm × 400 μm.

Figure 12: The cross section of the CAPTEG, illustrating the capacitors constructed between the BPW layer and the SOI1 layer. The results using different readout pairs connected to each layer are identical and are averaged.

Figure 13: The cross section of the XTALKTEG. Capacitances are named depending on the distance from the connection, S (=short), M (=medium), and L (=long).
Figure 14: The measured capacitances plotted for different SOI2 layer potential including floating. The values for w/o SOI2 are obtained for normal SOI device.

Figure 15: The cross-talks magnitude as function of the signal frequency. The data are shown for three distances from the signal input and readout contacts. $V_{SOI2} = -1 \text{ V}$. 
4 Summary

We are developing double-SOI pixel sensors. Successful TID compensation in a pixel ASD readout circuit has been demonstrated for radiation dose up to 100 kGy. The shaper width of less than 1 $\mu\text{sec}$ is maintained after 100 kGy. The discriminator also works properly after 100 kGy.

The cross-talk suppression in double-SOI is being evaluated. The double-SOI is effective in reduction of the capacitance between the sensor node and the circuit electronics. The capacitance is reduced in double-SOI at $V_{\text{SOI2}} = -1 \text{ V}$ to 40% compared to normal SOI. The cross-talk is substantially reduced if the distance from the SOI2 connection is shorter.

The obtained results further ensure that double-SOI sensors are applicable to future high-energy experiments such as at the BELLE-II experiment or at the ILC experiment.

ACKNOWLEDGEMENTS

The authors are grateful for fruitful collaboration with the Lapis Semiconductor Co. Ltd. The double SOI wafers have been realized through their excellence. This work was supported by JSPS KAKENHI Grand Number 25109006, by KEK Detector Technology Project and also by VLSI Design and Education Center (VDEC), The University of Tokyo, with the collaboration of the Cadence Corporation and Mentor Graphics Corporation.
References

[1] T. Miyoshi et al., gDevelopment of KEK SOI pixel sensorsh, presented at this symposium; S. Ono et al., gSOI pixel sensor for the ILC vertex detectorh, presented at this symposium; K. Hara et al., gDevelopment of FD-SOI Monolithic Pixel Devices for High-Energy Charged Particle Detectionh, IEEE NSS, 23 Oct-29 Oct 2011, Valencia, CR-N21-1.

[2] T. Tsuru et al., gKyoto’s X-ray Astronomical SOI pixel sensor - XRPIXh, presented at this symposium; A. Takeda et al., gImprovement of spectroscopic performance using a charge-sensitive amplifier circuit for an X-ray astronomical SOI pixel detectorh, 2015 JINST 10 C06005.

[3] T. Hatsui et al., gx-ray imaging detectors for X-ray Free-Electron Lasersh, presented at this symposium; T. Hatsui et al., gDevelopments of X-ray Imaging Detectors at SACLA/SPRing-8: Current Status and Future Outlookh, Synchrotron Radiation News, Volume 27, Issue 4, 2014.

[4] SOITEC: http://www.soitec.com/en/technologies/smart-cut/

[5] Lapis Semiconductor Co., Ltd.: http://www.lapis-semi.com/en/.

[6] J. R. Schwank, M. R Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, Radiation Effects in MOS Oxides, IEEE Trans. Nucl. Sci., vol. 55-4, p. 1833, 2008.

[7] K. Hara et al., gRadiation Resistance of SOI Pixel Devices fabricated with OKI 0.15 µm FD-SOI Technologyh, IEEE IEEE Trans. Nucl. Sci., vol. 56-5, October 2009, pp. 2896-2904.

[8] K. Hara et al., ”Development of INTPIX and CNTPIX Silicon-On-Insulator Monolithic Pixel Devices”, PoS (Vertex2010) 033.

[9] M. Kochiyama et al., gRadiation effects in silicon-on-insulator transistors with back-gate control method fabricated with OKI Semiconductor 0.20 um FD-SOI technologyh, Nucl. Instr Meth A636 (2011) S62.

[10] S. Honda, K. Hara et al., gTotal Ionization Damage Effects in Double Silicon-on-Insulator Devicesh, IEEE NSS Conf. Record, N41-2, 2013.

[11] S. Honda et al., gTotal Ionization Damage Compensations in Double Silicon-on-Insulator Pixel Sensorsh, Proceedings of Sciences (TIPP2014), 039, 2014.
[12] I. Kurachi et al., Analysis of Effective Gate Length Modulation by X-ray Irradiation for Fully Depleted SOI p-MOSFETs, accepted for publication in IEEE Trans. on Electron Devices.

[13] F. Krummenacher, Pixel Detectors with Local Intelligence: an IC Designer Point of View, Nuclear Instruments and Methods in Physics Research, A305, 1991, pp.527-532.