Modeling Interface Charge Traps in Junctionless FETs, Including Temperature Effects

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Abstract—In this paper, an analytical predictive model of interface charge traps in symmetric long channel double-gate junctionless transistors is proposed based on a charge-based model. Interface charge traps arising from the exposure to chemicals, high-energy ionizing radiation or aging mechanism could degrade the charge-voltage characteristics. The model is predictive in a range of temperature from 77K to 400K. The validity of the approach is confirmed by extensive comparisons with numerical TCAD simulations in all regions of operation from deep depletion to accumulation and linear to saturation.

Index Terms—Interface traps, charge-based model, double-gate junctionless FET, ionizing radiation, aging effects, biosensors, temperature.

I. INTRODUCTION

JUNCTIONLESS field-effect transistors (JLFET) were proposed as a promising device for the future of scaling. Actually, source/drain (S/D) junctions in conventional metal-oxide-semiconductor field-effect transistors (MOSFET) is a big challenge in the nanoscale dimension [1]. The main advantage of JLTs is that they overcome this step and still are fully compatible with CMOS technology. In addition, JLFET is a good option for label-free biosensors when shaped as nanowires [2].

Using JLFET as biosensors, called Nanowires (NWs), is an interesting option due to their proven high sensitivity to biological and chemical elements [3]. They share the same principle of operation with regular JLFETs, except that they do not have any solid-state gate over the insulator. Because of this feature, they are exposed to contaminants from the materials which they are in contact with. Hence, these devices are facing much more defects or interface charge traps than the state-of-the-art CMOS devices, a situation that may affect their electrical properties. Similarly, trap and defects can be generated by ionizing radiation just as in regular MOSFETs.

When a MOSFET is exposed to high-energy ionizing radiation, deep trap states are generated in the bulk oxide or near the Si/oxide interface. The process of traps generation depends on the temperature, the applied electric field, and the oxide thickness [4] and [5]. Aging mechanism in MOS technologies is also a common cause of traps creation at the Si/oxide interface [6] and [7]. These interface traps could degrade the performance of MOS devices.

Modeling the effect of radiation on inversion mode MOS-FETs has already addressed in [8], but that model is not appropriate for junctionless devices. Influence of interface charge traps on biosensor junctionless devices was discussed in [3].

Thus, in order to account for ionizing radiation, stress-induced defects as well as the effect of interface charge traps on JLFETs in a simple and compact model compatible approach, we propose analytical expressions for modeling the interface charge traps in Double-Gate JLFET (DG JLFET), and we also include the effect of temperature from 77 K to 400 K. This model relies on the charge-based approach in [9] where we derive an equivalent gate-source voltage (∆Vgs) to take into account the effect of interface charge traps. This is quite different from former developments [3]. We study the behavior of current-voltage characteristics and derive analytical solution for the subthreshold swing (SS). This approach will be validated with technology computer-aided design (TCAD) simulations, including temperature.

II. GATE VOLTAGE SHIFT IN PRESENCE OF INTERFACE TRAPS IN JLFETS

As mentioned, high-energy radiation and aging are responsible for ionization damage in the form of oxide charge traps (Qox) and interface charge traps (Qit). Traps close to the Si/oxide interface can be charged positively, negatively or neutral. These charge states depend on their energy level respect to the mid-gap energy and Fermi level. When the energy level of the trap is above the mid-gap, it behaves as an acceptor-like trap, and when below the mid-gap, it behaves like a donor-like trap [10] and [11]. A donor-like trap with an energy level above the Fermi level will be positively charged by emitting an electron, and neutral if its energy is below the Fermi level. Conversely, an acceptor-like trap with an energy level above the Fermi level is electrically neutral and will be negatively charged by trapping an electron if its energy is below the Fermi level [3] and [10]. Hence, Interface charge traps are amphoteric and their behavior as donors or acceptors depends on their energy in the band-gap [3], [8]. Fig. 1a shows the energy diagram of an n-type DG JLFET at flat band voltage. As explained, the donor-like traps are completely filled but the acceptor-like traps are partially filled. Hence, we have negative charges at the Si/oxide interface. Fig. 1b demonstrates the energy diagram of a p-type DG JLFET at flat band voltage. Acceptor-like traps are completely empty and donor-like traps are partially filled, resulting in positive charges at the interface.
The interface charge density \( Q_{it} \) is obtained by integrating the trap-state density \( D_{it}(E) \) times the trap occupation probability \( f(E) \) over the band-gap energy \([11]\),

\[
Q_{it} = -q \int_{E_V}^{E_G} D_{it}(E) \times f(E) dE. \tag{1}
\]

We consider an n-type long-channel symmetric double-gate JLFET (as shown in Fig. 1(c) with a doping density \( N_D \), a channel width \( W \) and a gate oxide thickness \( T_{ox} \).

The total charge in the semiconductor, \( Q_{sc} \), is related to the potential which drops across the gate capacitor

\[
Q_{sc} = -2C_{ox} \left( V_{GS} - \Delta \phi_{ms} + \psi_s + \frac{Q_{it}}{2C_{ox}} \right), \tag{2}
\]

where \( \Delta \phi_{ms} \) denotes the difference between the work function of metal and the work function of an intrinsic semiconductor, and \( Q_T \) represents the trap charge density includes interface charge traps and oxide charged traps i.e., \( Q_T = Q_{it} + Q_{ot} \).

We rewrite (2) as follows

\[
V_{GS} = \Delta \phi_{ms} + \psi_s - \frac{Q_{sc} + 2Q_T}{2C_{ox}}. \tag{3}
\]

The surface potential only depends on the charge density in the silicon channel (\( Q_{sc} \)). Hence, by imposing the same charge in the semiconductor, the gate potential in the case there is no trap i.e., \( Q_T = 0 \) will be

\[
V'_{GS} = \Delta \phi_{ms} + \psi_s - \frac{Q_{sc}}{2C_{ox}}. \tag{4}
\]

Therefore, according to (3) and (4), traps are responsible for a gate-source voltage shift (\( \Delta V_{GS} \)) equal to \(-Q_{T}/C_{ox}\). As expected, two contributions are evidenced

\[
\Delta V_{GS} = -\frac{Q_{it}}{C_{ox}} + \frac{Q_{ot}}{C_{ox}}. \tag{5}
\]

The oxide charge traps are supposed to have a fixed charge density (i.e. they are not affected by the potentials) meaning that they would merely shift the electrical characteristics by a constant value \(-Q_{ot}/C_{ox}\). Therefore, without loss of generality, we propose to focus on the effect of \( Q_{it} \) on the electrical characteristics.

Because the continuum nature of traps energy levels, \([11]\) has no analytical solution. Thus, we first investigate the single-level interface traps, then include the common exponential trap energy level distribution.

### III. SINGLE ENERGY LEVEL TRAPS

We assume an n-type DG JLFET and consider acceptor-like interface traps with a density \( N_{it} \) per unit area at \( E_{it} \) which is the energy of single interface charge trap. Hence, for a single trap \( E_{it} \), \( D_{it}(E_{it}) \) equals to \(-q \times N_{it} \) and \( Q_{it} \) is given by \( Q_{it} = -q \times N_{it} \times f(E_{it}) \). The occupation probability of an acceptor-like trap with an energy level \( E_{it} \) is determined by \([8]\)

\[
f(E_{it})^{-1} = 1 + \exp \left( \frac{E_{it} - E_F}{k_B T} \right). \tag{6}
\]

Here we assume the degeneracy factor equal to 1. By defining \( E_{i-1} = E_{it} - E_i \), where \( E_i \) is the intrinsic fermi level, \( Q_{it} \) is obtained by

\[
\frac{Q_{it}}{qN_{it}} = -\left[ 1 + \exp \left( \frac{E_{i-1} - E_F}{k_B T} \right) \exp \left( -\frac{\psi_s - V_{ch}}{U_T} \right) \right]^{-1}, \tag{7}
\]

where \( \psi_s = -(E_i - E_F)/q \) is the surface potential, \( V_{ch} \) is the quasi Fermi potential and \( U_T = k_B T/q \) is the thermal voltage.

Following the derivation of the charge-based model for double-gate JLFETs developed in \([9]\) and \([10]\), we have the two following relationships which link the surface potential \( \psi_s \) and the center potential \( \psi_0 \)

\[
E_s^2 = \frac{2qni_T U_T}{\epsilon_{si}} \left[ \exp \left( \frac{\psi_s - V_{ch}}{U_T} \right) - \exp \left( \frac{\psi_0 - V_{ch}}{U_T} \right) \right] - \frac{N_D}{n_i} \left( \frac{\psi_s - \psi_0}{U_T} \right), \tag{8}
\]

\[
\psi_s - \psi_0 = \frac{qni_T U_T^2}{8\epsilon_{sc}} \left[ \exp \left( \frac{\psi_s - V_{ch}}{U_T} \right) - \frac{N_D}{n_i} \right], \tag{9}
\]

where \( n_i \) is the intrinsic carrier concentration and \( \epsilon_{si} \) is the permittivity of silicon. \( E_s \) is the surface electric field which equals to \( Q_{sc}/2\epsilon_{si} \). Hence, \( Q_{sc} \), the semiconductor total charge density can be linked to the surface and center potential,
and we can write
\[
\left( \frac{Q_{sc}}{2\epsilon_{si}} \right)^2 = \frac{2qniU_T}{\epsilon_{si}} \left\{ \exp \left( \frac{\psi_0 - V_{ch}}{U_T} \right) \left[ \exp \left( \frac{\psi_s - \psi_0}{U_T} \right) - 1 \right] - \frac{N_D}{n_i} \left( \frac{\psi_s - \psi_0}{U_T} \right) \right\}.
\]

(10)

A. Depletion Mode

Under depletion mode, the potential at the center is larger than the potential at the surface which leads to a positive charge in the semiconductor \((Q_{sc} \geq 0)\). Hence, the exponential term in \([10]\) is much smaller than the second term and therefore relation \([10]\) can be approximated with
\[
\left( \frac{Q_{sc}}{2\epsilon_{si}} \right)^2 = \frac{2qN_D}{\epsilon_{si}} (\psi_0 - \psi_s).
\]

By substituting \([9]\) in \([11]\), the surface potential in the depletion mode is obtained with respect to the total charge density
\[
\psi_s - V_{ch} = U_T \ln \left( \alpha \theta \right), \quad (12)
\]

where \(\alpha\) and \(\theta\) are
\[
\alpha = \frac{N_D}{n_i} \exp \left( -\frac{Q_{sc}^2}{8U_T\epsilon_{si}C_{si}Q_f} \right), \quad (13)
\]
\[
\theta = 1 - \left( \frac{Q_{sc}}{Q_f} \right)^2, \quad (14)
\]

where \(Q_f = qN_D T_{si} \) and \(C_{si} = \epsilon_{si}/T_{sc}\).

Unlike oxide charge traps, interface charge traps can cause a gate-source voltage shift that depends on the total charge density. By introducing \([12]\) in \([14]\) and then in \([5]\) (with \(Q_{ot} = 0\)), the gate-source voltage shift is
\[
\Delta V_{GS} = \frac{qN_D}{C_{ox} \left( 1 + \eta \alpha^{-1} \theta^{-1} \right)}, \quad (15)
\]

where \(\eta = \exp(E_{it} - k_B T)\), the total charge density in the semiconductor becomes
\[
Q_{sc} = -2C_{ox} \left( V_{GS}^* - \Delta V_{GS} - V_{ch} - U_T \ln (\alpha \theta) \right), \quad (16)
\]

where we define the effective gate voltage as \(V_{GS}^* = V_{GS} - \Delta \phi_{gs}\). By solving relationships \([15]\) and \([16]\), total charge density in the semiconductor and the mobile charge density \(Q_m = Q_{sc} - Q_f\), are obtained. It is worth mentioning that, when there are not traps i.e., \(Q_T = 0\), \(\Delta V_{GS}\) is zero and relationship \([16]\) gives back the general relationship derived in \([9]\) and \([10]\).

B. Threshold Voltage Shift

Unlike inversion mode MOSFETs, the definition of threshold voltage \((V_{th})\) in junctionless transistors is not obvious. However, there are some definitions of threshold voltage for junctionless transistors. One of these defines the threshold voltage as the gate potential which cancels the mobile charge density \((Q_{sc} = Q_f)\) when the logarithmic term in \([16]\), i.e. \(\theta\) is neglected \([10]\). Hence, \(\alpha\) at threshold takes a simple form
\[
\alpha = \frac{N_D}{n_i} \exp \left( -\frac{Q_f}{8U_T C_{si}} \right). \quad (17)
\]

Under these assumptions, the threshold voltage shift is
\[
\Delta V_{th} = \frac{qN_D}{C_{ox} \left( 1 + \eta \alpha^{-1} \theta^{-1} \right)}, \quad (18)
\]

C. Accumulation Mode

In accumulation mode, the second term in \([5]\) is always smaller than the exponential term. Therefore, the second term in accumulation can be omitted. In addition, in accumulation the center potential remains close to the value it takes at the flat-band condition \([10]\)
\[
\psi_0 \approx \psi_{0,FB} = V_{ch} + U_T \ln \left( \frac{N_D}{n_i} \right). \quad (19)
\]

Thus, relation \([10]\) can be simplified to
\[
\left( \frac{Q_{sc}}{2\epsilon_{si}} \right)^2 = \frac{2qN_D}{\epsilon_{si}} \left[ \exp \left( \frac{\psi_s - V_{ch}}{U_T} \right) - \frac{N_D}{n_i} \right]. \quad (20)
\]

Hence, the surface potential in the accumulation mode is derived and is a function of the total charge density
\[
\psi_s - V_{ch} = U_T \ln (\beta), \quad (21)
\]

where \(\beta\) is defined as
\[
\beta = \frac{Q_{sc}^2}{8\epsilon_{si} qn_i U_T} + \frac{N_D}{n_i}. \quad (22)
\]

Introducing \([21]\) in \([4]\) and then in \([5]\) (with \(Q_{ot} = 0\)) results in the gate-source voltage shift in accumulation mode
\[
\Delta V_{GS} = \frac{qN_D}{C_{ox} \left( 1 + \eta \beta^{-1} \right)}, \quad (23)
\]

and the total charge density in the semiconductor in accumulation mode becomes
\[
Q_{sc} = -2C_{ox} (V_{GS}^* - \Delta V_{GS} - V_{ch} - U_T \ln (\beta)). \quad (24)
\]

Comparing \([15]\) with \([23]\), we notice that \(\Delta V_{GS}\) is given by the same relationship for both regions of operation, an unexpected but very interesting result which can be summarized as follows
\[
\Delta V_{GS} = \frac{qN_D}{C_{ox} \left( 1 + \eta \gamma^{-1} \right)}, \quad \gamma = \begin{cases} \alpha \theta, & \text{Depletion} \vspace{0.1cm} \\ \beta, & \text{Accumulation} \end{cases} \quad (25)
\]

This implies that the mobile charge density satisfies a generic relationship.
\[
Q_m = -Q_f - 2C_{ox} (V_{GS}^* - \Delta V_{GS} - V_{ch} - U_T \ln (\gamma)). \quad (26)
\]

To confirm the validity of this model, we performed simulations with SILVACO TCAD software assuming a double gate JLFET with \(1 \mu m\) channel length and \(10 \text{ nm}\) silicon thickness. The doping density and oxide thickness were set respectively to \(N_D = 5 \times 10^{16} \text{ cm}^{-3}\) and \(1.5 \text{ nm}\).

Here the single energy level has been activated for the traps. The interface trap density is set to \(N_{it} = 1 \times 10^{12} \text{ cm}^{-2}\). The mobile charge density versus effective gate voltage which is obtained from TCAD simulations and the model is depicted in Fig. 2.a. Lines and symbols have been used for the analytical model and TCAD simulations, respectively. Both linear and logarithmic representations of the analytical model demonstrate a full agreement with TCAD simulations.
D. Drain Current

Since we have analytical relationships for mobile charge density in depletion and accumulation modes, we can use both analytical charge-based model described in [9] and explicit relationships which are derived in [12] for obtaining drain current. To assess this model with TCAD simulations, we have used explicit relationships and we recall them here. Thus for the drain current in the depletion mode we have the following equation from [12]

\[ I_{Dep}(V_G^*, V_D, V_S) = \mu \frac{W}{L_G} \left[ \frac{1}{8C_{si}} - \frac{1}{4C_{ox}} \right] Q_{sc}^2 - \frac{Q_{sc}^3}{12Q_JC_{si}} \frac{Q_J}{2C_{ox}} + U_T Q_J \ln \left( 1 + \frac{Q_{sc}}{Q_J} \right)^2 \right]_S^D, \tag{27} \]

and for the accumulation mode [12]

\[ I_{Acc}(V_G^*, V_D, V_S) = \mu \frac{W}{L_G} \left[ \frac{Q_J}{2C_{ox}} + 2U_T \frac{Q_J}{4C_{ox}} \frac{Q_{sc}^2}{8Q_JC_{si}U_T} \right. \left. - U_T Q_J \ln \left( 1 + \frac{Q_{sc}^2}{8Q_JC_{si}U_T} \right) \right]_S^D, \tag{28} \]

where \( \mu \) is the free carrier mobility. If we define the hybrid channel when some part of the channel, near the source contact, is in accumulation and the other part, near the drain, is in depletion, we can write the drain current as follows [12]

\[ I_{hyb}(V_G^*, V_D, V_S) = I_{Acc}(V_G^*, V_D^* - V_{FB}, V_S) + I_{Dep}(V_G^*, V_D^* - V_{FB}). \tag{29} \]

In this work, \( \mu \) is assumed constant along the channel and the width of the device is set to 1 \( \mu \)m.

By solving (26) and introducing it in (27) to (29) the drain current is obtained. The drain current versus the effective gate voltage at \( V_{DS} = 10 \) mV and \( V_{DS} = 1 \) V for the trap energy levels \( E_{t-i} = 0 \) eV and \( E_{t-i} = 0.2 \) eV has been plotted in Fig. 2b and 2c. The results from the model are compared with TCAD simulations using the same parameters and indicate a good agreement in both linear and exponential representations.

The black dashed line in all the figures depicts the case which the density of traps is zero i.e. without traps. In order to make the effect of interface traps more clear, gate voltage shift due to the interface traps as a function of effective gate voltage for different values of energy levels has been shown in Fig. 3a. The agreement between the analytical model and TCAD simulations is excellent in both depletion and accumulation modes. It is observed from the plot that \( \Delta V_{GS} \) for above the flatband voltage doesn’t depend on the \( E_{t-i} \) and it can be simplified to \( \Delta V_{GS} = qN_{it}/C_{ox} \).

E. Subthreshold Swing

Subthreshold swing degradation is another important effect of interface charge traps since they implicitly change the
Thus, the subthreshold swing \( SS \) becomes
\[
SS = \left[ \frac{\partial}{\partial V_{GS}} \log (I_D) \right]^{-1} = Q_m \ln(10) \frac{\partial V_{GS}}{\partial Q_m},
\]
where \( \partial V_{GS}/\partial Q_m \) derived from (26):
\[
\frac{\partial V_{GS}}{\partial Q_m} = -\frac{1}{2C_{ox}} + \frac{\gamma'}{\gamma} \left( \frac{qN_{it} \eta \gamma}{C_{ox} (\eta + \gamma)} + U_T \right),
\]
where \( \gamma' = \partial \gamma/\partial Q_m \). Since the device operates in subthreshold, according to relation (25) \( \gamma \) is equal to \( \alpha \theta \) and \( \gamma'/\gamma \) becomes
\[
\gamma' = \frac{2Q_{sc}}{Q_m (Q_m + 2Q_f)} - \frac{Q_{sc}}{4U_T C_{ox} Q_f}.
\]
Next, introducing (33) in (32) then substituting in (31), the subthreshold swing becomes an explicit function of the mobile charge density:
\[
SS = \ln(10) \left[ -\frac{Q_m}{2C_{ox}} + \frac{Q_m \gamma'}{\gamma} \left( \frac{qN_{it} \eta \gamma}{C_{ox} (\eta + \gamma)} + U_T \right) \right].
\]
To extract the maximum subthreshold swing \( SS_{\text{max}} \), we propose to introduce some approximation in (34). Since \( Q_m \) is negligible in the subthreshold, we can ignore \( Q_m/(2C_{ox}) \) and assume that \( Q_m \gamma'/\gamma \) is close to unity:
\[
SS \approx \ln(10) \left[ \frac{qN_{it} \eta \gamma}{C_{ox} (\eta + \gamma)} + U_T \right].
\]
Thus, \( SS \) peaks when \( \gamma = \eta \)
\[
SS_{\text{max}} = \ln(10) \left( \frac{qN_{it}}{4C_{ox}} + U_T \right).
\]
Interestingly, the largest value of the subthreshold slope is closely related to the density of interface traps.

Subthreshold swing degradation induced by the presence of interface traps can be observed in Fig. 2. To make more clear this effect, subthreshold swing as a function of the effective gate potential for different values of \( E_{t-i} \) and \( N_{it} \) for both the analytical model and TCAD simulations, have been plotted in Fig. 3a and 3b. The agreement between the analytical solution and the TCAD simulations is evidenced.

IV. EXPONENTIAL TRAP ENERGY LEVEL DISTRIBUTION

So far only considered discrete energy trap levels have been discussed. Although these are instructive, they are not representative of real devices. Admittedly, real devices exhibit an exponential distribution of traps energy in the bandgap, commonly designed as U-shaped distribution [13].

Since we assume an n-type device, only interface traps which energies above the midgap are considered. In addition, according to the TCAD models, the maximum in the acceptor-like density lays at the conduction band edge. Hence, the charge density of traps can be written
\[
Q_{it} = -q \int_{E_i}^{E_C} N_{itc} \exp \left( \frac{E - E_C}{E_d} \right) \times f(E) dE, \quad (37)
\]
where \( N_{itc} \) is the density of acceptor-like states in the exponential distribution at the conduction band edge and \( E_d \) specifies the characteristic decay energy.

To calculate the trapped charge density, we rely on the same model discussed in section III valid for for single trap energy levels where we simply propose to replace \( N_{it} \) and \( E_{t-i} \) with averaged parameters \( N_{it}^* \) and \( E_{t-i}^* \):
\[
\frac{Q_{it}}{qN_{it}^*} = - \left[ 1 + \exp \left( \frac{E_{t-i}^*}{kT} \right) \right]^{-1}. \quad (38)
\]
The analytical approach is compared with TCAD simulations as shown in Fig. 4. Using \( N_{itc} = 4 \times 10^{13} \text{cm}^{-2} \) and \( E_d = 0.035 \text{eV} \) as reported in [3]. Then by adjusting the averaged parameters, \( N_{it}^* = 1.5 \times 10^{12} \text{cm}^{-2} \) and \( E_{t-i}^* = 0.592 \text{eV} \). These values fit quite well with TCAD results. Interestingly, these parameters which were ‘extracted’ at room temperature still give accurate results when changing the temperature. Fig. 4 illustrates the drain current versus the effective gate potential at \( V_{DS} = 10 \text{mV} \) and \( V_{DS} = 1 \text{V} \) for an exponential distribution of interface traps energy. Since the maximum density of interface traps happens close to the conduction band edge, their impact on the electrical characteristic is evidenced at relatively high gate potentials, otherwise traps remain unoccupied.

V. ASSESSMENT OF THE MODEL FROM 77K TO 400K

In some applications, low temperature operation is necessary and present many advantages such as a steeper subthreshold slope [14–16]. Having an analytical model covering a wide range of temperature operation is therefore a big advantage.

In this section, we assess the model for various temperatures ranging from 77 K to 400 K (note that we have used Boltzmann statistics only). For simplicity, we also assume a constant
mobility, given that this will mainly act as a scaling factor for the current, but will have almost no impact on the electrostatics, i.e. on the conclusions of this section [17]. According to [18] the mobility at low temperatures changes with respect to the mobile charge density. This effect could be introduced in the proposed model at the correction to the current, however, the conclusions on the trap charge distribution will remain the same. In addition, this would require introducing fitting parameters, which would weaken our physics-based analysis. The intrinsic carrier concentration for the temperatures used in this section are \( n_i = 4.39 \times 10^{-13} \text{ m}^{-3} \), \( 1.18 \times 10^{11} \text{ m}^{-3} \), and \( 6.16 \times 10^{18} \text{ m}^{-3} \) at \( T = 77 \text{ K} \), 200 K, and 400 K respectively.

Fig. 5 depicts the mobile charge density versus the effective gate voltage at \( T = 77 \text{ K} \), 200 K, and 400 K for single trap energy levels \( E_{t-i} = 0 \text{ eV} \) and \( E_{t-i} = 0.2 \text{ eV} \). For the range of mobile charge density considered, which is depicted in Fig. 5, different trap energy levels behave in the same way at 77 K. Indeed for those energy levels the traps do not change their charge states. The results confirm an excellent agreement between the analytical model and TCAD simulations.

Finally, we also assessed the validity of the model for the more realistic case of an exponential energy trap distribution at \( T = 77 \text{ K} \), 200 K, and 400 K. These are shown in Fig. 6 where the drain current versus the effective gate voltage is plotted at \( V_{DS} = 10 \text{ mV} \) and \( V_{DS} = 1 \text{ V} \). Interestingly, the averaged parameters, i.e., \( N^*_i \) and \( E^*_{t-i} \), do not need to be modified, meaning that the model that we have presented is quite predictive (note that we anticipate that for lower temperatures i.e. 4.2 K the roots of the model would have to be revised introducing Fermi-Dirac Statistics, and possibly 2D density of states).

VI. CONCLUSION

An analytical charge-based model for symmetric double-gate junctionless FETs with interface charge traps was developed. The model incorporates the impact of radiation and aging degradation on DC electrical characteristics of double-gate JLFETs by proposing an equivalent gate-source voltage. A detailed study of the interface charge traps and their influence on the device performance is carried out. Both single energy level and exponential distribution energy levels for interface traps have been investigated. In particular, the subthreshold swing degradation in the presence of single level interface charge traps has been modelled accurately. We also included the impact of the temperature from 77 K to 400 K, a very important aspect for cryogenic applications. The model has been compared to TCAD simulations with an excellent agreement in all regions of operation from deep depletion to accumulation and linear to saturation.

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