An anti-alias harmonic-reject phase modulation for digital outphasing transmitter

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Abstract: This paper proposes a sufficient anti-alias and harmonic-reject phase modulation (PM) technique for digital outphasing transmitter. Instead of using complicated spectrum shaping modulation or power-hungry digital-to-analog (DAC) and high-order filters, the proposed less-complex modulation employs cross point estimation (CPE) algorithm to improve the adjacent channel leakage ratio (ACLR) performance and adopts harmonic rejection algorithm to achieve out-of-band (OOB) noise attenuation. When evaluated with a 10 dB peak-to-average power ratio (PAPR) 16 QAM orthogonal-frequency-division-multiplexing (OFDM) signal with a 30 MHz intermediate frequency (IF) carrier, the proposed modulation achieves an ACLR of −65 dBc, providing 17 dB improvement compared with −48 dBc for conventional modulation. Moreover, 56 dB and 57 dB extra attenuations for the 2rd and 3rd images are achieved, respectively.

Keywords: ACLR, anti-alias, PM, harmonic-reject, outphasing transmitter

Classification: Integrated circuits

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1 Introduction

Benefiting from the lower circuit complexity and lower power consumption of digital circuits, the trend in transmitter systems is moving into digital domain by utilizing digital modulator and switch-mode power amplifier (SMPA) [1, 2, 3, 4, 5, 6]. Outphasing transmitter is an attractive structure to achieve all these objectives [2, 3, 4, 5]. However, digital outphasing transmitter suffers from ACLR degradation and OOB property deteriorated due to sampling images and harmonic components modulation, which are common problems for all kinds of digital transmitters [2, 5, 7, 8, 9, 10]. To address these issues, many authors presented alternative modulation options. SAW-less 33% duty-cycle LO is an efficient scheme to achieve harmonic suppression; however, 6xLO increases power consumption and 33% duty-cycle leads into even harmonics [7]. Sigma Delta (ΣΔ) modulation is another simple method to realize noise shaping for digital transmitters [5, 8]; however, the operating frequency should be a multiple of carrier frequency, which is limited by the reconfigurable hardware resources. As demonstrated in [5], to achieve three-level Sigma Delta modulation, 25 GHz digital sampling rate is used for 20M LTE signal, it is complex and power consumption. High-Q filters is also a straight solution for excellent ACLR and OOB performance, however this filter requires very sharp frequency response for alias signal and 3rd harmonic which is difficult to implement on chip and has limited tuning range. All these architectures increase cost and complexity and are generally not preferred for low power and low complexity communication systems, especially narrow-band systems, such as NB-IoT, LoRa and WPANs, which have drawn much attention from both academia and industry in recent years.

In this paper, we propose a less complicated anti-alias harmonic-reject phase modulation to overcome ACLR degradation and reduce OOB emission. Compared
with 33% duty-cycle based modulation and Sigma Delta modulation, the proposed modulation is always working at LO frequency without introduce extra harmonics, which means the power-hungry and complex multiple digital sampling rate is unnecessary. With on chip harmonic rejection, the transmitter system can be more flexible and avoid complicated high order filters. Furthermore, the high quality signal generated by the proposed modulation significantly relaxes the performance requirement for PA, the most power-consumption part in transmitter.

The proposed modulator is comprised of unwrap, cross point estimation (CPE), phase modulator (PM), and pulse width modulator (PWM), as depicted in Fig. 1. In the proposed approach, the phases are firstly unwrapped to limit the required phase steps. Then, the unwrapped phases pass through CPE to get zero cross points for suppressing the sampling images due to zero order hold (ZOH) operation. Two outputs of CPE are essential to describe the cross points, which are edge point (\(ep\)) and pulse width (\(pw\)) respectively. The \(ep\) is the control code for PM to realize basic phase modulation, and the \(pw\) controls PWM to achieve CPE based modulation. Four interrelated signals are generated from PWM to achieve low OOB emission. While simulating with a 16-QAM OFDM signal with 10-dB PAPR, the proposed modulation achieves an ACLR of \(-65\) dBc, 2rd image attenuation of \(-100\) dBc and 3rd image attenuation of \(-65\) dBc with 10-bit phase resolution in the LO frequency and without filter.

![Fig. 1. Overall structures of the proposed anti-alias phase modulator](image)

2 Low complexity CPE algorithm

Fig. 2 depicts a time domain illustration of ZOH and CPE processes. The linear interpolating based CPE [9, 10] can be regarded as a digitally approximation to the ideal analog phase signal, and the zero crossing points appear whenever \(\omega t + \phi(t)\) equals to \(\pi\) and multiples of it, as the circles depict in Fig. 2.

Moreover, the resulting outphasing signals with both sinusoidal carrier and square carrier are demonstrated in Fig. 2. The square waveform represents ideal sinusoidal waveform by reconstructing its zero crossing points. Therefore, the CPE based square carrier modulated signal can be expressed as

\[
Sig_{\text{cpe-square}}(t) = \text{sign}(\sin(\Phi(t))), \quad \text{where} \quad \Phi(t) = \omega t + \phi(t)
\]

where \(\omega = 2\pi/T\), and \(\phi(t)\) is given by

\[
\phi(t) = \phi(n) + \frac{\phi(n) - \phi(n - 1)}{T} \ast t \quad n = 1, 2, 3 \ldots .
\]

The contribution of the carrier \(\omega t\) is linearly increasing from 0 to \(2\pi\) within one period, and \(\phi(t)\) is a linear interpolation of the original sampled phase signal \(\phi(n)\). The zero crossing points then can be calculated by
\[
\omega t + \phi(t) = \frac{2\pi}{T} \ast t + \phi(n) + \frac{\phi(n) - \phi(n - 1)}{T} \ast t = k\pi, \quad k = 0, 1, 2, 3 \tag{3}
\]

where the range of \( k \) is decided by the maximum phase jump of \( \Phi(t) \), which is \( 3\pi \) when considering unwrapped phases [4]. Therefore, the \( ep \), as shown in Fig. 2, can be obtained by

\[
t_{ep,k} = \frac{(k\pi - \phi(n)) \ast T}{2\pi + \Delta\phi}, \quad \text{where} \quad \Delta\phi = \phi(n) - \phi(n - 1) \tag{4}
\]

For calculating (4), we propose another expression to avoid long-bit divisions:

\[
t_{ep,k} = \exp(\ln(k\pi - \phi(n)) + \ln(T) - \ln(2\pi + \Delta\phi)) \tag{5}
\]

Furthermore, taking into account the linear property of \( \Phi(t) \) in every period, the interval of the adjacent two zero crossing points, which means \( pw \) as Fig. 2 shows, is a constant for every period. Therefore, we calculate the desire values by the following steps:

\[
t_{pw} = \exp(\ln(\pi) + \ln(T) - \ln(2\pi + \Delta\phi)) \tag{6}
\]

\[
t_{ep-1} = \exp(\ln(\pi - \phi(n)) + \ln(T) - \ln(2\pi + \Delta\phi)) \tag{7}
\]

\[
t_{ep,k} = t_{ep,k-1} + t_{pw} \tag{8}
\]

where \( t_{ep,0} \) only appears when \( \phi(n) = 0 \), and \( t_{ep,k} \) should be smaller than \( T \).

![Fig. 2. Time domain illustrations of ZOH and CPE](image)

### 3 The proposed harmonic-reject modulation

The proposed harmonic-reject modulation consists of two mainly sub-blocks: the PM block for basic phase modulation and the PWM block to achieve negative edge correction due to CPE process.

Fig. 3 shows the architectures of the proposed lower-power glitch-free PM. The Phase detector (PD) [3] and DLL Controller are adopted together to lock the eight stages tapped delay line (TDL) [4] to one LO period. Therefore, each TDL Cell represents a 45° phase step. In addition, the two paths of outphasing transmitter share the TDL to save power. The TDL Controller is working as a glitch-free phase multiplexer for picking out the taps of TDL to achieve coarse phase modulation.
Moreover, further delay of the residual phase is implemented by the 7-bit digital-control-delay-line (DCDL) for accuracy. The TDL_Cell and DCDL have the similar structures as employed in [3]. The coarse stage uses power-of-two architecture, and the fine stage uses digital controlled varactors (DCVs).

The structures and timing diagram to describe the glitch-free implementation of TDL_Controller are illustrated in Fig. 4. The 3-bit MSB of the ep is transformed to eight enable control codes, which are detected by the negative edge of each tap signal (like tdl45) from TDL_Cell to provide glitch-free operation and achieve dynamical tap selections. As the timing diagram shows, the enable signals always change before the positive edge instead of transforming with the positive edge as conventional phase MUX, which generates glitches. The coarse modulated signal TDL_out is then further delayed by DCDL with the 7-bit LSB of ep to achieve residual phase modulation, as Fig. 3 shows. Finally, a 50% duty cycle modulated signal is obtained with rising edges representing the phase information.

The PWM stage is employed to achieve the negative edge locations correction for CPE based modulation. Fig. 5 shows the architectures and timing diagram of it. The CPE process contains pulse-extension mode and pulse-shortening mode to achieve time-varying pulse width. The conversion between them is determined by the comparison of pw and T/2. In the pulse-extension mode, the CPE uses OR logic for S1 and S1_d to keep much longer high logic, and in the pulse-shortening
mode, it employs an AND logic to narrow the original pulse. Meanwhile, besides the desired signal \( cpe \), an additional \( T/2 \) delayed signal \( cpe_{nc} \) is generated to remove even harmonics of \( cpe \). Moreover, the proposed PWM contains extra circuits for odd harmonics elimination, as Fig. 5 shows. In this approach, \( S1 \) is firstly delayed by \( pw/4 \) and \( 3 \times pw/4 \) \((pw/4 + pw/2)\) to obtain \( S1_S \) and \( S1_R \) respectively. Then, an SR-latch combines the rising edge and falling edge of the two delayed signals to generate \( cpe_{odd} \), as illustrated in Fig. 5. The \( cpe_{odd}_{nc} \) is used to remove even harmonics of \( cpe_{odd} \). The finally four output signals of PWM will be amplified with different gains. The \( cpe \) and \( cpe_{nc} \) have the same gain \( g \), while a larger gain \( \sqrt{2}g \) is used for the \( cpe_{odd} \) and \( cpe_{odd}_{nc} \).

4 Frequency-domain analysis of proposed modulation

4.1 Analysis of CPE

Fig. 6 shows the comparison of transfer function of ZOH and CPE operation. The frequency response of CPE is the square of ZOH, which means a much lower
magnitude-frequency property as depicted in Fig. 6. Therefore, the CPE process is capable of achieving sufficient images attenuation.

4.2 Analysis of harmonic-reject
Table I illustrates the harmonic components of each signal generated by PWM. The same factors ($1/k\pi$) of each harmonics have not taken into account. In addition, the magnitudes of $cpe_{\text{odd}}$ and $cpe_{\text{odd nc}}$ are $\sqrt{2}$ times larger than $cpe$ and $cpe_{\text{nc}}$. Consequently, with the proposed modulation, only the fundamental term and the 7th harmonic left, as the $tx_{\text{signal}}$ shows in Table I, which significantly improves the performance of ACLR and out-of-band emission.

![Table I: Harmonic components of each PWM signals](image)

5 Simulation results and discussion
The proposed anti-alias harmonic-reject modulation based digital outphasing transmitter was simulated by MATLAB with a 16 QAM 10 dB PAPR 802.15.4g OFDM signal. The proposed glitch-free PM and harmonic-reject PWM were modelled and simulated with Verilog code. The 30 MHz intermediate frequency carrier was chosen for the first stage of the two-stage up-conversion architectures for lower power consumption and adequate phase resolution.

The spectrum comparisons of ZOH based modulation and the proposed anti-alias harmonic-reject phase modulation are presented in Fig. 7. As Fig. 7(a) shows, the ACLR has been significantly suppressed from $-48$ dBc to $-60$ dBc in CPE approach, due to the sufficiently attenuation of sampling images compared to traditional sampled and hold process. Fig. 7(b) shows the spectrum of CPE process with proposed even harmonics reject algorithm. The emission in 2 fs is $-100$ dBc, which is 56 dB lower than the original modulated signal. This suppression is achieved by using $cpe$ and $cpe_{\text{nc}}$ signals together. The $cpe_{\text{nc}}$ is a negative polarity and T/2 delayed signal of $cpe$, which has the opposite even images to it, as Table I depicts. The proposed odd harmonics rejection is realized by combining the basic phase modulated signal $cpe$ with the extra same phase but half pulse width signal $cpe_{\text{odd}}$, as illustrated in Fig. 5. The performance is shown in Fig. 7(c). With the movement of majority of the odd harmonics, an 8 times higher suppression which is $-65$ dBc in 3 fs is achieved. Furthermore, benefiting from the elimination of odd harmonics, the ACLR performance is furtherly improved to $-65$ dBc. The final comparison of traditional modulation and the proposed anti-alias harmonic-reject modulation is depicted in Fig. 7(d).
Fig. 7. The spectrum comparison (a) ZOH and CPE operation (b) ZOH and CPE with even harmonics rejection (c) ZOH and CPE with odd harmonics rejection (d) ZOH and proposed modulation

Fig. 8. The spectrum of ideal sinusoidal carrier and proposed anti-alias modulation with square carrier
Fig. 8 illustrates the spectrum behavior of proposed modulated signal and the ideal sinusoidal carrier. Almost same performance of ACLR has been achieved, however, when considering wideband property, about 10 dBc noise degradation appears in the proposed modulation. This deviation is caused by the 6th image of the 7th harmonic component which has not been eliminated as mentioned before. Even though, the spectrum is still far away from the spectra mask in 802.15.4g standard.

A comparison of our work with other digital implementations transmitter is summarized in Table II.

| Table II. ACLR and OOB performance comparison |
|------------------------------------------------|
| Architecture | [6] | [7] | [9] | This work |
|---------------|-----|-----|-----|-----------|
| Bandwidth     | Digital polar | Digital Quadrature | CPE+DSM PWM | Digital Outphasing |
| Signal type   | 40 MHz 64QAM | 10 MHz N/A | 40 MHz N/A | 800 KHz 16QAM |
| Utilization of filter | Yes | Yes | No | No |
| Sampling rate (GHz) | 2.42 | N/A | 2.6 | 0.03 |
| Resolution    | 8 bit AM/PM | N/A | 11 bit PM | 10 bit PM |
| LO (Hz)/Fc (Hz) | 1 | 6 | 1 | 1 |
| ACLR (dBc)    | −40 | −54 | −75 | −48 | −65 |
| 2xLO Suppression (dBc/Hz) | −50 | −64* | N/A | −44 | −100 |
| 3xLO Suppression (dBc/Hz) | −36 | −58* | N/A | −8 | −65 |

*Signal with 20 samples

Our work demonstrates the best out-of-band noise performance without filter when compared with prior works. Meanwhile, with a lower oversampling rate and 10-bit phase resolution while without extra sigma-delta modulation, the proposed modulation achieves comparable ACLR performance as previous options. The algorithm in [9] is also simulated using a 20 KHz bandwidth signal at 1 MHz carrier frequency with 10-bit phase resolution, and the result shows the ACLR is −65 dBc, as same as our work. Compared with the implementation in [7], our work avoids using 6 times multiple LO to generated 33% duty carrier, which is complex and power consumption. In addition, with a much lower 3xLO suppression, a much better CIM3/CIM5 performance can be achieved.

6 Conclusion

An all digital and less complicated anti-alias harmonic-reject phase modulation is proposed for digital outphasing transmitter. The CPE algorithm is employed for suppressing sample images due to ZOH operation. And it uses look-up-table (LUT)
implementation to avoid long bit multiplications and divisions. To reduce power losses and prevent unpredictable spurs, we propose a TDL shared glitch-free PM for dynamical tap selection. For further attenuating the out-of-band emission cased by square waveform carrier, we propose harmonic-reject circuits which are realized by PWM. With the proposed modulation, aliasing problem has been significantly reduced and out-of-band performance is sufficiently improved. Moreover, the high performance signals sufficiently reduces the design challenges of PA and avoids high-Q and high-order filter requirements. As a consequence, the proposed sufficient and less complicated modulation is practical for the wireless communication systems, especially for narrow-band systems which is designed to operate in very large-scale low-power applications.

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