New Design of Reversible Full Adder/Subtractor using $R$ gate

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Abstract
Quantum computers require quantum processors. An important part of the processor of any computer is the arithmetic unit, which performs binary addition, subtraction, division and multiplication, however multiplication can be performed using repeated addition, while division can be performed using repeated subtraction. In this paper we present two designs using the reversible $R^3$ gate to perform the quantum half adder/subtractor and the quantum full adder/subtractor. The proposed half adder/subtractor design can be used to perform different logical operations, such as $AND$, $XOR$, $NAND$, $XNOR$, $NOT$ and copy of basis. The proposed design is compared with the other previous designs in terms of the number of gates used, the number of constant bits, the garbage bits,
the quantum cost and the delay. The proposed designs are implemented and tested using GAP software.

keywords: reversible gates; quantum processors; arithmetic unit; reversible adder; reversible subtractor.

1 Introduction

Quantum computers offer essential speedup over classical computers. Many researchers believe that, no amount of progress in classical computers, could overcome the power of a quantum computer [27]. More computer resources are required to solve computational problems; some problems are impossible to solve using classical computers, because they require ridiculous resources to solve the realistic case of the problem [28]. Quantum computers can efficiently solve computational problems, that have no efficient solution on classical computer, since Classical computers are built using irreversible gates [8, 27]. The main problem in using irreversible gates is the loss of data due to the problem of heat dissipation, since the amount of energy dissipated is proportional to the number of bits erased. To overcome this problem, reversible gates are used, as they do not cause heat dissipation, and thus there will be no loss of data [1, 2].

Reversible gates are the building block of reversible circuits. A reversible circuit maps each input vector to a unique output vector and vice versa [8]. Reversible circuits have many applications such as: building quantum computers, bioinformatics, nanotechnology based systems, low power CMOS systems, digital signals processing, optical computation, DNA computing and communications [8, 9, 11]. In reversible computing, the output values are sufficient to recover the input values, the number of inputs must be equal to the number of outputs, each input pattern maps to a unique output pattern. Thus fan-out, feed-back and loops are not allowed. When building a reversible circuit, the following criteria should be considered: minimum number of reversible gates, minimum number of garbage outputs, minimum number of constant inputs and minimum quantum cost. In reversible computers the main building blocks are: Multiplexer, Decoder, Arithmetic logical unit ...etc [1, 2, 4, 8].

Arithmetic adders and subtractors are the fundamental building blocks in many computational units. The expected paradigm shift logic that is compatible with quantum computation requires a compatible implementation of adder and subtractor. They can be used to perform other logical operations, such as multiplication and division [4, 8]. Thus many researchers focus on designing adders and subtractors. A method for constructing reversible full adder using two RG gates is introduced in [1]. A reversible full adder using two Peres gates, to minimize the quantum cost is designed in [4]. An efficient full adder circuit based on four Fredkin gates is introduced in [9]. A new reversible gate called NR gate is introduced in [7], then used to designed an optical reversible full
adder and subtractor, composed of two NR gates. A new 4 × 4 reversible gate called MOG gate, which can be used by itself as a full adder/subtractor, is introduced in [6]. The MOG gate is constructed from two C gates, one Fredkin gate and one Peres gate. Two designs using PRT gates are introduced in [8]. These designs are used to build reversible full adder using two PRT-2 gates, and reversible full subtractor using two PRT-1 gates. A new reversible gate called TR gate is introduced in [9], and then used to build a reversible full subtractor, then the quantum cost of the TR gate is optimized in [24]. The optimized model is used to redesigned the full subtractor. Three designs for one-bit full adder/subtractor is presented in [10], then used to build eight-bit parallel binary adder/subtractor. The first design is composed of five C gates, two Fredkin gates and one TR gate, the second design is composed of two TR gates and two C gates, and the third design is composed of two C gates and two Peres gates.

The aim of this paper is to introduce a new design of half and full Adder/Subtractor using the R gate introduced in [12]. In this paper, we are going to introduce two designs using the R₃ gate, which are: the half adder/subtractor and the full adder/subtractor. Three different R₃ gates (R₃₃₁₂, R₃₁₂₃ and R₃₂₃₁) are used in the two proposed designs. This new design is compared with the other full Adder/Subtractor introduced in [7, 6, 10]. The new design can be used as low quantum cost reversible ALU, it also has minimum number of garbage bits and minimum number of gates. These designs have advantage over the other designs, that they can be used as adder and/or subtractor using the same gate with minimal cost, in addition the proposed half adder/subtractor design can be used to perform different logical operations, which are: AND, XOR, NAND, XNOR, NOT and copy of basis, and the proposed full adder/subtractor design can be used to perform different logical operations, which are: AND, XOR, XNOR and NOT.

The organization of this paper is as follows: Section 2 gives a short introduction to the elementary quantum gates, and defines the terminologies used in this paper. Section 3 proposed the new designed half and full adder/subtractor. The results and discussion are presented in Section 4, where it compares the proposed designs with relevant designs proposed by others. Finally Section 6 concludes the paper.

2 Basic Definitions

This section introduces some basic symbols, definitions and terminologies, used in synthesizing of reversible circuits, to build reversible full adder/subtractor.

**Definition 2.1.** A Boolean function \( f : x \rightarrow y \) is said to be reversible, if and only if each input vector \( x \in X^n \) maps to a unique output vector \( y \in X^n \). For
- inputs/outputs function, there are \((2^n)!\) reversible functions, \(\forall X = \{0,1\}\) and \(n \in \mathbb{Z}\) [13].

**Definition 2.2.** The main reversible gate \(C^n\) NOT used to synthesize any reversible circuit, is defined as,

\[
(y_1, y_2, \ldots, y_{n-1}; f_{out}) = C^n\) NOT \((x_1, x_2, \ldots, x_{n-1}; f_{in}).
\] (1)

where \(y_i = x_i\) for \(1 \leq i \leq n - 1\) and \(f_{out} = f_{in} \oplus x_1x_2 \ldots x_{n-1}\). \(x_1, x_2, \ldots, x_{n-1}\) are called the control bits and \(f_{in}\) is called the target bit [13].

**Definition 2.3.** The cost of the circuit is the total cost of all the \(n\) gates used to synthesize the circuit [14].

**Definition 2.4.** The minimum cost \(\text{Minc}(g)\) defined for a reversible gate \(g\) means that, there exists a realization of \(g\) with cost equal to \(\text{Minc}(g)\), and there is no any other realization with cost less than \(\text{Minc}(g)\) [14].

**Definition 2.5.** Reversible gate \(g\) computes a reversible functions \(f\) and is bijective [13, 15].

**Definition 2.6.** A permutation \(\sigma: A \rightarrow A\) is said to be a bijection. It maps an input to an output, from a finite set \(A = \{1,2,\ldots,n\}\), can be written as follows,

\[
\sigma = \begin{pmatrix} 1 & 2 & 3 & \ldots & n \\ \sigma(1) & \sigma(2) & \sigma(3) & \ldots & \sigma(n) \end{pmatrix}; \quad (2)
\]

The top row can be eliminated and written as follows,

\[
\sigma = \begin{pmatrix} \sigma(1) & \sigma(2) & \sigma(3) & \ldots & \sigma(n) \end{pmatrix}; \quad (3)
\]

another notation having a permutation in the form of \(\begin{pmatrix} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 \\ 2 & 3 & 1 & 4 & 8 & 5 & 6 & 7 \end{pmatrix}\), it can be written as \((1,2,3)(5,8,7,6,5)\), this notation is called the product of disjoint cycles [13].

**Definition 2.7.** The constant bit is an input to the circuit used to compute some given logical operations [7].

**Definition 2.8.** Garbage bit is an additional output to the reversible logic gate, that is added to make the number of inputs equal to the number of outputs whenever necessary, in order to achieve reversibility. [7].

**Definition 2.9.** The quantum cost of any reversible circuit is the number of elementary gates (2-qubit gates) used to build the circuit [14] [15] [16]. There are two methods of calculating the quantum cost, which are: cost015 metric, which consider the quantum cost of any 1 \(\times\) 1 reversible gate as zero, the quantum cost of any 2 \(\times\) 2 reversible gate as one, and the quantum cost of the other reversible gates is calculated by counting the number of elementary gates used to build them [14] [7]. The cost115 metric, is similar to cost015 but it consider the quantum cost of the 1 \(\times\) 1 gates as one [7] [15] [16]. In this paper we are using cost015 metric.
2.1 Reversible Gates

There are many universal reversible gates, these gates are used to build any reversible circuits, this section introduces some of the popular important gates used to build adder and subtractor circuits.

The \textit{NOT} gate (\textit{N})

The \textit{N} gate is a 1-bit reversible gate, it flips the input bits unconditionally. For 1×1 reversible circuit, there is only one \textit{N} gate with quantum cost equals to zero \cite{19}. Eqn.\textbf{4} shows the functionality of the \textit{N} gate. The circuit representation of the \textit{N} gate is shown in Fig. \textbf{1} \cite{18}.

\begin{equation}
N_1 : y_1 = x_1 \oplus 1 = \overline{x}_1,
N_1 : (x_1) \rightarrow (1, 2),
\end{equation}

\textbf{The Feynman gate (\textit{CNOT})}

The \textit{CNOT} gate (also denoted as \textit{glsC} gate) is a 2-bits reversible gate. It takes as input 2-bits, a target bit and a controller bit, then flips the target bit, if the controller bit is set to 1. For 2×2 reversible circuit, there are two \textit{C} gates, having a quantum cost of one \cite{18}. Eqn.\textbf{5} shows the functionality of the \textit{C} gate. The circuit representation of the \textit{C} gate is shown in Fig. \textbf{2} \cite{18}.

\begin{equation}
C_{i,j}^2: y_i = x_i,
y_j = x_j \oplus x_i,
C_{1,2}^2: (x_1, x_2) \rightarrow (3, 4),
C_{2,1}^2: (x_1, x_2) \rightarrow (2, 4),
\end{equation}

where \(i\) and \(j\) ∈ \{1, 2\} in any order.

\textbf{The Square-root \textit{NOT} gates (\textit{V} and \textit{V}^\dagger)}

The square-root \textit{NOT} gate are the controlled-\textit{V} (\textit{v}) and the controlled-\textit{V}^\dagger (\textit{u}). They are 2-bits reversible gates, their quantum cost is \textit{one}. For 2×2 reversible
circuits, there are two \( V \) gates and two \( V^\dagger \) gates, Fig. 3 shows their circuit representation. They have the following properties [14, 18]:

- \( vv = uu = N \),
- \( uv = vu = I \),
- \( vN = Nv = u \),
- \( uN = Nu = v \),

where \( I \) is the identity gate [14, 18].

The Toffoli gate \( T^3 \)

The \( T^3 \) is a 3-bits reversible gate. It takes as input 2 controller bits and 1 target bit, then flips the target bit, if the control bits are set to 1. For a \( 3 \times 3 \) reversible circuit, there are three \( T^3 \) gates, having a quantum cost equals to \( five \). Eqn. 6 shows the functionality of the \( T^3 \) gate. The circuit representation of the \( T^3 \) gate is shown in Fig. 4 [19].
where \( j, k \) and \( l \in \{1, 2, 3\} \) in any order.

### The Peres gate \( P \)

The \( P \) gate is a 3-bits reversible gate. It combines the functions of \( T^3 \) gate and \( C \) gate in a single gate; and acts on an arbitrary 3-bits \( x_j, x_k \) and \( x_l \). It applies the \( C \) gate on one bit, taking the first bit as controller, and applies the \( T^3 \) gate on the other bit, taking the first and second bits as controller. For a \( 3 \times 3 \) bits circuit, there are six different \( P \) gates, having a quantum cost of four. Eqn.\( \ref{eqn:peres} \) shows the functionality of the \( P \) gate. The circuit representation of the \( P \) gate is shown in Fig. 5 \[20, 18\].

\[
P^3_{j,k,l} : \\
  y_j = x_j, \\
  y_k = x_j \oplus x_k, \\
  y_l = x_l \oplus x_j x_k, \\
\]

\[
P_{123} : (x_1, x_2, x_3) \rightarrow (5, 7, 6, 8), \\
P_{132} : (x_1, x_2, x_3) \rightarrow (5, 6, 7, 8), \\
P_{213} : (x_1, x_2, x_3) \rightarrow (3, 7, 4, 8), \\
P_{231} : (x_1, x_2, x_3) \rightarrow (3, 4, 7, 8), \\
P_{312} : (x_1, x_2, x_3) \rightarrow (2, 6, 4, 8), \\
P_{321} : (x_1, x_2, x_3) \rightarrow (2, 4, 6, 8). \\
\]

### The Fredkin gate \( F \)

The \( F \) gate is a 3-bits reversible gate. It is used to perform conditional swap on two of its inputs if the third input is set to 1. For a \( 3 \times 3 \) bits circuits, there are three different \( F \) gates, with quantum cost equals to five \[20\]. Eqn.\( \ref{eqn:fredkin} \) shows the functionality of the \( F \) gate. The circuit representation of the \( F \) gate is shown

\[
\begin{align*}
  &T^3_{1,2,3} \quad T^3_{1,3,2} \quad T^3_{2,3,1} \\
  &x_1 \quad y_1 \quad x_2 \quad y_2 \quad x_3 \quad y_3
\end{align*}
\]
Figure 5: The possible $P$ gates over 3-bits reversible circuit.

![Diagram of P gates]

Figure 6: The possible $F$ gates over 3-bits reversible circuit.

![Diagram of F gates]

in Fig. 6[18],

$$F_{j,k,l}^3: y_j = x_j,$$

$$x_j = \begin{cases} 1 & y_k = x_l, y_l = x_k \\ 0 & y_k = x_k, y_l = x_l \end{cases}$$

$$F_{1,2,3}^3: (x_1, x_2, x_3) \rightarrow (6, 7),$$

$$F_{2,1,3}^3: (x_1, x_2, x_3) \rightarrow (4, 7),$$

$$F_{3,2,1}^3: (x_1, x_2, x_3) \rightarrow (4, 6).$$

The $R$ gate

The $R^n$ gate is $n$-bits universal reversible gate. It is first introduced in [12]. It combines the functionality of the $N$ gate, the $C$ gate and the $T$ gate. The $R^1$ gate is a 1-bit gate, which inverts the input bit unconditionally, there is one $R^1$ gate, it's quantum cost is Zero. Eqn(9) shows the functionality of the $R^1$ gate[12].

$$R_1^1 : y_i = x_i \oplus 1,$$

$$R_1^1 : (x_1) \rightarrow (1, 2).$$

The $R^2$ gate is 2-bits gate, which makes one bit as a controller to flip the other bit, then it flips the controller bit is flipped unconditionally, there are two different $R^2$ gates, the quantum cost of the $R^2$ gate is one. Eqn(10) shows the
Figure 7: The six possible $R^3$ gates for 3-bits reversible circuit.

The $R^3$ gate is 3-bits reversible gate. The quantum cost for the $R^3$ gate is four. For 3-bits input/output circuit, there is six different $R^3$ gates as shown in Fig. 7. Eqn.11 shows the functionality of the six different $R^3$ gates [12].

$$R^3_{j,k,l} : y_j = x_j \oplus x_k \oplus x_l, \quad y_k = x_k \oplus x_j, \quad y_l = x_l \oplus x_j,$$

$$R^3_{1,2,3} : (x_1, x_2, x_3) \rightarrow (1, 7, 6, 5, 4, 2, 8, 3),$$
$$R^3_{1,2,1} : (x_1, x_2, x_3) \rightarrow (1, 4, 6, 2, 7, 5, 8, 3),$$
$$R^3_{1,3,1} : (x_1, x_2, x_3) \rightarrow (1, 4, 7, 3, 6, 5, 8, 2),$$
$$R^3_{1,3,2} : (x_1, x_2, x_3) \rightarrow (1, 6, 7, 5, 4, 3, 8, 2),$$
$$R^3_{1,2,2} : (x_1, x_2, x_3) \rightarrow (1, 6, 4, 2, 7, 3, 8, 5),$$
$$R^3_{2,1,3} : (x_1, x_2, x_3) \rightarrow (1, 7, 4, 3, 6, 2, 8, 5),$$

For $n \geq 3$ $R^n$ combines the functionality of $N, C, T^3, T^4, ..., T^n$, there are $n!$ different $R^n$ gates. In this paper we are going to build the proposed design using the $R^3$ gate.

3 The Proposed Design

This section introduces the two different proposed designs, which are half adder/subtractor and full adder/subtractor, designed using $R^3$ gate.
Table 1: The truth table for the proposed half Adder/subtractor.

| X | Y | S/D | B<sub>out</sub> | C<sub>out</sub> |
|---|---|-----|----------------|--------------|
| 0 | 0 | 1   | 0              | 0            |
| 0 | 1 | 1   | 1              | 0            |
| 1 | 0 | 1   | 0              | 0            |
| 1 | 1 | 1   | 0              | 1            |

3.1 The Proposed Design for half Adder/Subtractor

The half adder/subtractor is capable of adding or subtracting two bits X and Y, realizing the operation \( S = X + Y \), with \( C_{out} \) as the carry out bit, after performing addition, and realizing the operation \( D = X - Y \), with \( B_{out} \) as the borrow out bit, after performing subtraction. The \( R_{3,1,2}^3 \) gate can be used by itself as a reversible half adder/subtractor. It takes as input 3-bits, the first two input bits are the two bits required to be added or subtracted X and Y, the third bit is a constant bit of value one. It returns 3-bits as output, the first bit is the summation bit \( S \) or the difference bit \( D \), calculated by \( X \oplus Y \), the second bit is the borrowing bit \( B_{out} \), calculating \( \overline{XY} \) and the third bit is the carry out \( C_{out} \) bit, calculating \( XY \). Fig. 8 shows the circuit representation for half adder/subtractor, designed using \( R_{3,1,2}^3 \) gate.

The operation of the proposed half adder/subtractor can be expressed in the form of truth table, as shown in Table 1. The quantum cost of the proposed design is four.

\[
\begin{align*}
X \quad \quad \quad \quad \quad \quad \quad \quad X \oplus Y \ (S/D) \\
Y \quad R_{3,1,2}^3 \quad \quad \quad \quad \quad \quad XY \oplus Y (B_{out}) \\
1 \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad XY \ (C_{out})
\end{align*}
\]

Figure 8: The proposed design of the half adder/subtractor.

The half adder/subtractor can be extended to perform different logical operation, by changing the order of the input bits and the value of the constant bit. Setting the constant bit to 1, allows the design to perform bit-wise XOR and AND operations, while setting the constant bit to 0, allows it perform bit-wise XOR and NAND operation, as shown in Fig. 9 where \( G \) is the garbage bit. Setting the value of the input Y bit to 1, allows the design to perform bit-wise complement and copy of basis for the input bit X, as shown in Fig. 10. Changing
the order of the input bits, in which the first input bit is set to 1 as a constant bit, allows the design to perform XNOR operation as shown in Fig 11.

\[ X \oplus Y \]

(a) \hspace{1cm} (b)

Figure 9: Circuit representations for \( R_{2,3,1} \) gate as logical operator where: (a) the constant bit is set to 1 to calculate AND and XOR operations, and (b) the controller bit is set to 0 to calculate NAND and XOR operations.

\[ \overline{X} \]

\[ G \]

\[ X \]

\[ 1 \]

\[ R_{2,3}^3 \]

Figure 10: Circuit representations for \( R_{2,3,1} \) gate as logical operator where the constant bit is set to 1 and one of the other two bits is set to 1, to calculate NOT and copy of basis operations.

### 3.2 The Proposed Design for full Adder/Subtractor

A half adder/subtractor is not very useful on its own. In addition, a third bit is needed to add the carry-in to the two addend, while in subtraction, the borrow-in is required to be added to the subtrahend, thus a full adder/subtractor is required. It realizes the two operations \( S = X + Y + Z \) and \( D = X - Y - Z \), where \( X \) and \( Y \) are the two input bits required to be added or subtracted, and \( Z \) is either the carry-in bit during addition or the borrow-in bit during subtraction.

The proposed design of the full adder/subtractor consists of two \( R^3 \) gates, which are: \( R^3_{1,2,3} \) and \( R^3_{3,1,2} \). The two inputs \( X \) and \( Y \) with a constant bit is passed to \( R_{1,2,3}^3 \) gate. The first output is a garbage bit, the other two outputs are passed as input to \( R_{3,1,2}^3 \) with \( Z \) bit, which is either \( C_{in} \) during addition and \( B_{in} \) during subtraction. The output of this gate is 3-bits, which are: carry-out
Figure 11: Circuit representations for $R_{2,3,1}^3$ gate as logical operator, to calculate XNOR operations.

$(C_{out})$ at $y_2$, borrow-out $(B_{out})$ at $y_4$ and sum $(S)$ or difference $(D)$ at $y_3$, as shown in Fig. 12.

Figure 12: The proposed reversible Full Adder/subtractor using $R$ gate library.

The proposed design can work as a reversible full adder, if the value of the constant bit at $x_2$ is set to 0, while it can work as a reversible full subtractor, if the value of $Y$ is entered instead of the constant bit at $x_2$. Eqn. 12 shows the equations of the output bits. Table 2 shows the truth table of the proposed reversible full adder, and Table 3 shows the truth table of the proposed reversible full subtractor. The quantum cost of the proposed full adder/subtractor is eight. The following examples shows in steps how addition and subtraction are calculated using the proposed full adder/subtractor.

**Example 3.1.** Suppose we want to add the values (1+1+1=3) then $X = 1$, $Y = 1$ and $C_{in} = 1$, the inputs to $R_{123}$ are $x_1 = 1, x_2 = 0$ and $x_3 = 1$, giving outputs $y_1 = 0, 1$ and 0. 1 and 0 with $x_4 = 0$ are passed as input to $R_{312}$, giving outputs $y_2 = 1, y_3 = 0$ and $y_4 = 0$. Since $y_3$ is the Difference bit and $y_4$ is the $B_{out}$ bit, and they have the values 0, 0 respectively, then the output is 0.
Table 2: The truth table of the proposed full adder.

| X | Y | Z | S | C_{out} |
|---|---|---|---|--------|
| 0 | 0 | 0 | 0 | 0      |
| 0 | 0 | 1 | 1 | 0      |
| 0 | 1 | 0 | 1 | 0      |
| 0 | 1 | 1 | 0 | 1      |
| 1 | 0 | 0 | 1 | 0      |
| 1 | 0 | 1 | 0 | 1      |
| 1 | 1 | 0 | 0 | 1      |
| 1 | 1 | 1 | 1 | 1      |

Table 3: The truth table of the proposed full subtractor.

| X | Y | Z | D | B_{out} |
|---|---|---|---|--------|
| 0 | 0 | 0 | 0 | 0      |
| 0 | 0 | 1 | 1 | 1      |
| 0 | 1 | 0 | 1 | 1      |
| 0 | 1 | 1 | 0 | 1      |
| 1 | 0 | 0 | 1 | 0      |
| 1 | 0 | 1 | 0 | 0      |
| 1 | 1 | 0 | 0 | 0      |
| 1 | 1 | 1 | 1 | 1      |

**Example 3.2.** Suppose we want to subtract the values (1-1=0) then $X = 1$, $Y = 1$ and $B_{in} = 0$, the inputs to $R_{123}$ are $x_1 = 1$, $x_2 = 1$ and $x_3 = 1$, giving outputs $y_1 = 0$, $0$ and $0$. $0$ and $0$ with $x_4 = 1$ are passed as input to $R_{312}$, giving outputs $y_2 = 1$, $y_3 = 1$ and $y_4 = 0$. Since $y_2$ is the $C_{out}$ bit and $y_3$ is the summation bit, and they have the values 1,1 respectively, then the output is 3.

\[
S = X \oplus Y \oplus Z, \\
C_{out} = XY \oplus XZ \oplus YZ, \\
D = X \oplus Y \oplus Z, \\
B_{out} = \bar{X}(Y \oplus Z) \oplus YZ, \\
\]

(12)

where $X$ and $Y$ are the input bits, which are needed to be added or subtracted, $Z$ is either the carry-in bit, when addition is applied or the borrow-in bit, when subtraction is applied. $S$ is the summation bit, $D$ is the difference bit, $C_{out}$ is the carry out bit, $B_{out}$ is the borrow out bit.
Table 4: The effect of the constant inputs on the result of the 1-bit ALU proposed design based on Fig.12

| $x_1$ | $x_2$ | $x_3$ | $x_4$ | $y_1$ | $y_2$ | $y_3$ | $y_4$ | Result  |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| X     | 0     | Y     | $C_{in}$ | G     | $C_{out}$ | $Sum$ | G     | ADD     |
| X     | Y     | Y     | $B_{in}$ | G     | G     | $Diff$ | $B_{out}$ | SUB    |
| X     | 0     | Y     | -      | G     | $XY$    | G     | G     | AND     |
| X     | 0     | Y     | 0      | G     | G     | $X \oplus Y$ | G     | XOR     |
| X     | 0     | Y     | 1      | G     | G     | $X \oplus Y$ | G     | XNOR    |
| X     | 0     | 1     | 0      | G     | G     | $X$    | G     | NOT     |

3.3 Experimental Results

The proposed designs are compared with the designs proposed by others, according to the number of gates used to build the design, the number of constant bits, the number of garbage bits and the quantum cost of the design.

The comparison between the proposed half adder/subtractor design and the designs proposed by others, is shown in Table 5. It shows that the number of garbage bits achieved by the proposed design is 0, which is the best number of garbage bits achieved by the designs proposed by others. The number of gates used to build the proposed design is 1, which is similar to the best number of gates used to build designs proposed by others. The quantum cost of the proposed design is $four$, similar to the best quantum cost achieved by [24]. The number of constant bits is 1, similar to the smallest number of constant bits achieved by [24, 32]. As shown in Table 5, the proposed design shows the best results, compared with the other designs.

The comparison between the proposed design used to perform logical operations, and the designs proposed by others is shown in Table 6. The first design performs $AND$, $XOR$ and $NAND$ operations. The number of gates used to build the design is 1, similar to the best number of gates used to build the designs proposed by others. The number of garbage bits is 1, which is also similar to the best number of garbage bits achieved by [5, 23]. The number of constant bits used in the proposed design is 1, similar to the best number of constant bits used by the best designs proposed by others. The quantum cost of the proposed design is $four$, better than all the designs proposed by others.

The $NOT$ and copy of basis operations can be achieved by the second design.
Table 5: Comparing the different designs of half adders and subtractors.

| Proposed Design | Function | Gates used | No. Gates | No. Garbage bits | No. Constant bits | Quantum Cost |
|-----------------|----------|------------|-----------|------------------|-------------------|--------------|
| ADD/SUB         |          | One $R^2_{3,1.2}$ | 1         | 0                | 1                 | 4            |
| [25] ADD/SUB    |          | $2C$ gates+ $2Mux$ gates | 4         | 3                | 3                 | 8            |
| [7] ADD/SUB     |          | One $NR$ gate | 1         | 1                | 2                 | 7            |
| [9] ADD/SUB     |          | One $MOG$ gate | 1         | 2                | 2                 | 11           |
| [24] SUB        |          | One $TR$ gate | 1         | 1                | 1                 | 4            |
| [32] ADD        |          | One $T$ gate+ one controlled controlled $Z(-1)$ gate+ one $C$ gate | 3         | 1                | 1                 | 17           |

By comparing it with the other proposed designs, it is found that, the number of gates used to build the proposed design is 1, similar to the best number of gates used to build the designs proposed by others. The number of garbage bits in the proposed design is 1, similar to the best number of garbage bits achieved by [5, 23]. The quantum cost of the proposed design is four, better than the quantum cost of the other designs proposed by others.

The $XNOR$ and the $NOT$ operations can be obtained by the third proposed design. By comparing the four criteria points in the proposed design with the designs proposed by others, it is found that, the number of gates used to build the proposed design is 1, similar to the best number of gates used in the other designs. The number of garbage bits in the proposed design is 0, which is less than all the other designs proposed by others. The number of constant bits in the proposed design is 1, similar to the number of constant bits, used in the best designs proposed by others. The quantum cost of the proposed design is four, which is better than the quantum cost of the designs proposed by others.

The comparison between the proposed full adder/subtractor and the designs proposed by others is shown in Table 7. Some of the comparable designs in Table 7 are full adder/subtractor, such as: [6, 7, 10, 25, 30, 9, 33], other are full adders only, such as: [1, 3, 4, 5, 26, 31, 32], while in [24, 22] full subtractors are proposed.

The proposed full adder/subtractor is composed of two gates, which is the second best number of gates compared by the other designs, since in [6, 22] only one gate is used. The number of garbage bits in the proposed design is 1, similar to the number of garbage bits in [7], which is the best number of garbage bits
Table 6: Comparing the $R$ gate the other designs used to perform logical operation

| Logic operation  | Gates used     | No. Gates | No. Garbage bits | No. Conatant bits | Quantum Cost |
|------------------|----------------|-----------|------------------|-------------------|--------------|
| Proposed Design  | AND+ XOR + NAND | One $R_{3,1,2}$ | 1 | 1 | 1 | 4 |
| Proposed Design  | Copy + NOT     | One $R_{3,1,2}$ | 1 | 1 | 2 | 4 |
| Proposed Design  | XNOR+NOT       | One $R_{3,1,2}$ | 1 | 0 | 1 | 4 |
| [23] OR          | one $RG1$ gate | 1 | 2 | 1 | 5 |
| [23] AND         | One $RG1$ gate | 1 | 2 | 1 | 5 |
| [23] XNOR        | One $RG1$ gate | 1 | 2 | 1 | 5 |
| [23] NOT + copy  | One $RG1$ gate | 1 | 1 | 2 | 5 |
| [23] NOR         | One $RG2$ gate | 1 | 2 | 1 | 5 |
| [51] OR+AND      | One $F$ gate   | 1 | 1 | 1 | 5 |
| [51] XOR         | 2 $F$ gate     | 2 | 3 | 2 | 10 |
| [30] OR+XOR+NOR+XNOR | one $MRG$ gate | 1 | 2 | 2 | 6 |
| [29] NOT+XOR+NOR | one $TSG$ gate | 1 | 3 | 1 | 6 |
| [29] XOR+NAND+XNOR+OR | one $HNG$ gate | 1 | 2 | 2 | - |
| [29] NOR+AND+NOT | one $HNG$ gate | 1 | 3 | 2 | - |
achieved by the designs proposed by others. The number of constant bits in the proposed design is 1, similar to the second best number of constant bits used in the designs proposed by others, since the best number of constant bit is 0 proposed by [6]. The quantum cost of the proposed design is 8, which is similar to the best quantum cost achieved by the full adder/subtractor described in [4]. The quantum cost of the proposed design is greater than the best quantum cost of the full subtractor designed by [24]. The delay of the proposed design is 8, which is similar to the full adder/subtractor design in [7], much less than the delay of the full adder/subtractor design in [30]. The delay of the proposed design is higher than the delay of the designs in [24, 31], but these two designs are either full subtractor or full adder respectively.

The proposed design can be used as 1-bit ALU as it can perform Addition (ADD), Subtraction (SUB) and different logical operations such as: AND, XOR, XNOR and NOT, depending on the values of the constant bits, as shown in Table 4. By comparing the proposed design with the design described in [30], the proposed design has less quantum cost and less number of garbage bits.

Comparing the proposed design with the previously introduced designs, shows that the proposed design achieves better performance compared with the existing designs in terms of the number of gates used, the number of constant bits, the number of garbage bits and the quantum cost.
### Table 7: Comparing the different designs of full adders and subtractors.

| Proposed Design | Function | Gates used | No. gates | Garbage bits | Constant bits | Quantum cost | Delay |
|-----------------|----------|------------|-----------|--------------|---------------|--------------|-------|
| ADD/SUB         | 2 $R^3$ gates | 2 | 1 | 1 | 8 | 8 |
| [6]            | ADD/SUB | One MOG gate | 1 | 2 | 0 | 11 | - |
| [7]            | ADD/SUB | 2 $NR$ gate | 2 | 1 | 2 | 14 | 8 |
| [25]           | ADD/SUB | 2 $MUX$ gates + One $TR$ gate + 5 $F$ gates | 8 | 5 | 3 | 19 | - |
| [10] Design1   | ADD/SUB | 5 $C$ gates+ 2 $F$ gates + one $TR$ gate | 8 | 5 | 3 | 21 | - |
| [10] Design2   | ADD/SUB | 2 $TR$ gates+ 2 $C$ gates | 4 | 3 | 1 | 14 | - |
| [10] Design3   | ADD/SUB | 2 $P$ gates+ 2 $C$ gates | 4 | 3 | 1 | 10 | - |
| [30]           | ADD/SUB | 2 $C$ gates + one $HNG$ gate + 2$F$ gates + one $PAOG$ gate | 6 | 4 | 5 | 24 | 20 |
| [33]           | ADD/SUB | one $C$ gate + 2$QR$ gates+ one $NOT$ gate | 4 | 2 | 1 | - | - |
| [26]           | ADD     | One $NG$ gate+ One $T^3$ gate+ One $C$ | 3 | 2 | 1 | 10 | - |
| [11]           | ADD     | 2 $P$ gates | 2 | 2 | 2 | 8 | - |
| [14]           | ADD     | 4 $F$ gates | 4 | 4 | 2 | 20 | - |
| [13]           | ADD     | 2 $T^3$ + 2 $C$ | 4 | 2 | 2 | 12 | - |
| [11]           | ADD     | One $RG1_1$+ One $RG2_1$ | 2 | 2 | 1 | 10 | - |
| [31]           | ADD     | 2 $C$ gates+ 3 $u$ gates + one $v$ gate | 6 | 2 | 1 | 6 | 4 |
| [22]           | ADD     | one $DPG$ gate | 1 | 2 | 1 | 6 | - |
| [32]           | ADD     | 2 $T$ gate + 2$C$ gate + 2 controlled $Z(-1)$ gates | 6 | 2 | 1 | 34 | - |
| [24]           | SUB     | 2 $TR$ gates | 2 | 2 | 1 | 6 | 4 |
| [22]           | SUB     | one $F$ gate+ 2 $TSG$ gate | 3 | 6 | 2 | 9 | - |
4 Conclusion

The computer processor is the basic component of the computer. The most important part of the computer processor is the arithmetic logic unit. It performs binary addition, subtraction, multiplication and division. Addition and subtraction are the main operations in the arithmetic logical unit, since division and multiplication can be calculated using repeated subtraction and repeated division. Many applications uses the adder/subtractor, such as Arithmetic and logical unit (ALU), Program status word (PSW), Calculators, Embedded system, seven segment display etc.

In this paper, We proposed two new designs: quantum half adder/subtractor and quantum full Adder/ Subtractor using $R_3^3$ gate. we have shown that these two designs can be used to perform the logical operations, such as: AND, XOR, NAND, NOT and XNOR. The proposed designs are compared with the other previously proposed designs, according to the number of gates used to build the design, the quantum cost, the number of constant bits and the number of garbage bits.

The proposed half adder/subtractor is synthesized using $R_{231}^3$ gate and can be used to perform logical operations. It is compared with the other previous designs and it has the minimum number of gates, the minimum number of garbage bits, the minimum number of constant bits and the minimum quantum cost.

The proposed full adder/subtractor is synthesized using $R_{123}^3$ and $R_{312}^3$ gates, it can work as 1-bit ALU. It can also extend to work on any number of bits, by adding multiplexer to link each full adder/subtractor.

It is shown that the proposed full adder/subtractor is build using 2 gates which is the second minimum number of gates, it has one garbage bits which is equal to the minimum number of garbage bits, it has one constant bit, which is equal to the second minimum number of constant bits and it has the minimum quantum cost compared with the other full adder/subtractor. Consequently it will improve the efficiency of the arithmetic logical unit.

References

[1] Ni L., Guan Z., Zhu W.: A General Method of constructing the Reversible Full-adder. Third International Symposium on Information Technology and Security Informatics, IEEE, 109-113 (2010).

[2] Babu H., Islam M., Chowdhury A., Chowdhury S.: Reversible Logic Synthesis for Minimization of Full-Adder Circuit. The Euromicro Symposium on Digital System Design, IEEE, 1-5 (2003).
[3] Khlopotine A., Perkowski M., Kerntopf P.: Reversible Logic Synthesis by Iterative Compositions. IWLS, 1-5 (2002).

[4] Islam S., Islam R.: Minimization of Reversible Adder Circuits. Asian Journal of Information Technology, Medwell, 1146-1151 (2005).

[5] Bruce J., Thornton M., Shivakumaraiah L., Kokate P., Li X.: Efficient Adder Circuits Based on a Conservative Reversible Logic Gate. The IEEE Computer Society Annual Symposium on VLSI, IEEE, 1-6 (2002).

[6] Moghimi S., Reshadine M.: A Novel 4 × 4 Universal Reversible Gate as a Cost Efficient Full Adder/Subtractor in terms of reversible and Quantum Metrices. I.J. Modern Education and Computer Science, 28-34 (2015).

[7] Thersesal T., Sathish K., Aswinkumor R.: A new Design of Optical Reversible Adder and Subtractor using MZI. International Journal of Scientific and Research Publications, 5(4) 1-6 (2015).

[8] Fredkin H., Toffoli T.: Conservative logic. International J. Theor. Physics, v(21), 219-253 (1982).

[9] Thapliyal H., Ranganathan N.: Design of Efficient Reversible Binary Subtractors Based on a New Reversible Gate. IEEE Computer Society Annual Symposium on VLSI, IEEE, 229-234 (2009).

[10] Rangaraju H., Venugopal U., Muralidhara K., Raha K.: Design of Efficient Reversible Parallel Binary Adder/Subtractor. Computer Networks and Information Technologies, v(142), Springer, 83-37 (2011).

[11] Kamalakannan V., Shilpakala V., Ravi N.: Design of Adder/Subtractor Circuits Based on Reversible Gates. International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, 3796-3804 (2013).

[12] Montaser R., Younes A., Abdel-Aty M.: New Designs of Universal Reversible Gate Library. arXiv:1512.08991v1 [cs.ET], 1-17 (2015).

[13] Younes, A.: Tight bounds on the Synthesis of 3-bit reversible circuits: NF Fr library. Journal of Circuits, Systems and Computers, 23(3), 1-22 (2014).

[14] Yang, G., Song, X., Hung, W. N. N., Perkowski, M. A. and Seo, C.-J.: Synthesis of reversible circuits with minimal costs. CALCOLO, 45, 193–206 (2008).

[15] Shende, V. V., Prasad, A. K., Markov, I. L., and Hayes, J. P.: Synthesis of reversible logic circuits. IEEE T. Comput. Aid. D., 22(6), 710–722 (2003).

[16] Maslov, D., Miller, D.M.: Comparison of the cost metrics for reversible and quantum logic synthesis. IET Comput. Digit. Tec., 1(2), 98-104 (2008).
[17] Storme L., De Vos, A., Jacobs G.: Group theoretical aspects of reversible logic gates. J. Univers. Comput. Sci., 5(5), 307-321 (1999).

[18] Younes, A.: On the Universality of n-bit reversible gate libraries. Appl. Math. Inf. Sci., 9(5), 2579-2588 (2015).

[19] Montaser R., Younes A., Abdel-Aty M.: Improving the quantum cost of NCT-based reversible circuit. Quant. Inf. Process., Springer, 14(2), 325-351 (2013).

[20] Al Mamuni, S. and Menville, D.: Quantum cost optimization for reversible sequential circuit. Int. J. Adv. Comput. Sci. Appl., 4(12), 15-21 (2013).

[21] Khan, Md MH Azad.: Design of full-adder with reversible gates. International Conference on Computer and Information Technology, Dhaka, Bangladesh, 515-519 (2002).

[22] Saha R., Dalal S.: A Novel Reversible Combinational Circuit Design for Low Power Computation. Communication and Information Technology Conference (PCITC), IEEE 1-6 (2015).

[23] Lakshmi A., Sudha G.: Design of a reversible single precision floating point subtractor. Springer Open Journal, v(3), 1-20 (2014).

[24] Thapliyal H., Ranganathan N.: A New Design of the Reversible Subtractor Circuit. 11th IEEE International Conference on Nanotechnology, Portland Marriott, USA, 1430-1435 (2011).

[25] Gupta A., Singla P., Gupta J., Maheshwari N.: An Improved Structure of Reversible Adder and Subtractor. International Journal of Electronics and Computer Science Engineering, 2(2) 712-718 (2013).

[26] Hafez H., Islam M., Chowdhury S., Chowshury A.: Synthesis of Full-Adder Circuit using Reversible Logic. The 17th International Conference Conference on VLSI Design, IEEE, (2004).

[27] Nielsen M., Chuang I.: Quantum computation and Quantum Information. Cambridge University Press, 2000, (10),1-59 (2010).

[28] De Vos, A.: Reversible Computing Fundamentals. Quantum Computing and Applications, Wiley-VCH Verlag GmbH and Co.KGaA, 5-82, 131-166, 183-190 (2010).

[29] Islam, M.: A Novel Quantum Cost Efficient Reversible Full Adder Gate in Nanotechnology. CoRR, (abs/1008.3533), 1-7 (2010).

[30] Morrison, M., Ranganathan, N.: Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures. 2011 IEEE Computer Society Annual Symposium on VLSICoRR, IEEE, 126-131 (2011).
[31] Thapliyal, H.: *Mapping of Subtractor and Adder-Subtractor Circuits on Reversible Quantum Gates*. Trans. on Comput. Sci XXVII, Springer, LNCS 9570, 10-34 (2016).

[32] Monfared, A., haghparast, M.: *Design of Novel Quantum/Reversible Ternary Adder Circuits*. International Journal of Electronics Letters, Taylor and Francis, 1-14 (2016).

[33] Kianpour, M., Nadooshan, R.: *Novel 8-bit Reversible Full Adder/Subtractor using a QCA reversible Gate*. J Comput Electron, Springer, 459-472 (2017).