A CAD-Oriented Technique to Design an Optimum Load Impedance with Multi-Coupler Network for Class-F Power Amplifier

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Abstract

In this paper, a Load-pull technique to design a class-F power amplifier with multi-coupler network is presented. The fundamental load impedance and matching networks are separately integrated for class-F RF power amplifier high efficiency operation. The output used a transmitting type active integrated antenna. A Cree GaN FET CGH40006F transistor device at 3.50 GHz operating frequency was used in the design. The performance of the network has improved by 79.4% power added efficiency at 30.1dBm output power. This technique has been considered a useful for improving performance in mobile communication applications.

1 Introduction

Class-F power amplifier is well-known as the most efficient in the family of static nonlinear systems. It can achieve 100% efficiency by the way of harmonic resonators at the output network to wave shape the drain waveforms in a way the load appears to be a short at even harmonic and an open at odd harmonic. The drain voltage waveform can use one or multi-odd harmonics to estimate a square wave, while the drain current waveform accommodates one or more even harmonics to estimate a half a sine wave [1,2].

The class-F operation is not only a well-known technique in terms of improving the level of efficiency, but also easy to handle, compared to switching amplifiers [3]. The resonator power amplifiers use multiple resonators to control the harmonic frequencies in order to convert the drain voltage waveform to rectangular and the drain current waveform to half sinusoidal. Consequently, the efficiency improved with major reduction in power dissipation. For an active integrated system to perform optimally, optimization is required. An optimization allows fundamental frequency, achieve low impedance at even harmonics, and high impedance at odd harmonics. Furthermore, the use of simple approach to include a quarter wave lines at the drain output for drain load impedance ($Z_{VD}$) has illustrated a positive impact. The approach tolerates lowermost possible impedance at all harmonic frequencies outside the fundamental [4].

It is however weighty to apply load-pull technique with an active integrated antenna at the output of the active integrated system for shaping of harmonic frequencies by antenna resistivity. The optimal load impedance at fundamental frequency of the active integrated system can be conveyed to the load and cause resistances of the harmonic frequencies to be nearly flat, at the same time influence the active antenna to suppress the harmonic power from radiation. This shows that, the active integrated antenna impedance has matched with that of the active integrated system. Therefore, the active integrated system, which refers to the power amplifier with the optimum load impedance, accomplishes a high power added efficiency and output power. Furthermore, to consider the output matching circuit can increase the complexity of the active integrated power circuit and at the same time reducing the power losses. Finally, the active integrated antenna is considered to be responsible for converting the optimal load impedance for maximum efficiency [5].

This paper presents a design of class-F power amplifier using load pull approach to achieve high efficiency. Input and output matching circuits are designed with an active integrated antenna to obtain optimal fundamental load impedance. Couplers are used at the input and output of the active integrated system before the matching network. The 3.50 GHz operating frequency is used in this study to confirm the design principle of class-F operation with an alternative type of power transistor.

2 Power Amplifier Design and Optimization

The design and optimization class-F power amplifier was done with Agilent Technologies’ Advanced Design System (ADS) at 3.47 to 3.53 GHz, WiMAX frequency range. Subsequent choice of a suitable frequency of operation and output power, the transistor selected was the Cree 6 watt, GaN-HEMT large signal model. The large signal model is a multi-purpose device for variety of designs and applications. The input and output matching circuits are designed separately to avoid parasitic behavior of the transistor.

The Agilent Technologies’ Advanced Design System helps in optimizing the design. However, optimization of such design
is implemented according to the procedure of the design in one simulation. There is no defined separation technique for shaping a micro-strip antenna to acquire projected impedances at certain set of harmonic frequencies. However, this technique is feasible to use, where the impedance of the fundamental frequency can be kept rationally close to optimal point. In addition, the antenna input resistance can be reduced at the harmonic frequency by means of separating the higher resonance of micro-strip antenna from even and odd harmonic frequencies of the operating frequency. This may possibly be a realistic goal for controlling the 2nd to 7th harmonic frequencies, which are the main concern during optimization for higher efficiency [6]. These harmonic frequencies in the other hand cause the effect of feedback on input impedance, which makes the structure more complex. In optimizing the fundamental optimal load impedance of the input matching network, it is logical not to give so much attention to the feedback coming from harmonic frequencies. This simple technique can reduce the intense severity of the feedback [5]. Large signal transistor model provided by Cree was used in the simulation. In this research, third (3rd) and fifth (5th) harmonic frequencies are the main concern. So, in the design simulation, the harmonic are shaped to achieve higher efficiency. The drain source voltage (V<sub>ds</sub>) = 28V, gate bias voltage (V<sub>gs</sub>) = −3.0V. After the simulation, the DC drain current is achieved to be 41mA. The DC characteristics and quiescent bias point selection of the device has been illustrated in figure 1.

3 Load-pull Technique and 1-Tone Harmonic Balance Design and Simulation Consideration

After DC bias selection, load-pull in ADS using HB1Tone Load-Pull design guide with a nonlinear model of transistor is simulated. Figure 2 illustrates the load-pull design setup taken from the design guide. The circuit simulation results to output power and power added efficiency as shown in figure 3. The output power and power added efficiency contours responded as a function of load impedance. Each contour indicates the set of impedance corresponding to a constant output power or power added efficiency. It attempts to discover a standing solution for the nonlinear system in the frequency domain.

Figure 2: Circuit of design guide HB1Tone Load-Pull for 1-tone analysis.

Figure 3 has illustrated the outcome of the HB1Tone Load-Pull for 1-tone analysis. Maximum power added efficiency of 82.54% at 37.53dBm power delivered, was recorded as an estimated results expected in the final design. Nevertheless, this performance metric can be improved by the use of active integrated antenna at the output of the active integrated communication system, which can produce the perfect impedances for the load harmonics frequencies. The figure has also illustrated the input reflection coefficient and impedances of the active integrated class-F power amplifier load-pull simulation. The input reflection coefficient was produced as a function of the output impedance to exploit power added efficiency at a specified output power.

Figure 3: Source and Load reflection coefficients without matching.

Design of matching network is one of the most significant performance indicators in nonlinear power amplifiers. However, the response of the marching circuits can be seen in large signal s-parameters. The s-parameters measurement is not well clarified as predictable. As an alternative, a simple proxy method can be applied to derive reflection coefficients.
of the antenna, measuring the voltage of the incident and reflected wave. Both input and output reflection coefficients are taken into account, in this work. Hence, reflection coefficient can be acquire in many different ways, which one of these ways can be the application of a 2 x 2 simple coupler at the input and output phase of the active class-F power amplifier harmonic load-pull design circuit [7].

![Figure 4: Harmonic load-pull simulation circuit with a coupler.](image)

The simulation circuit was chosen from computer aided design software, an Agilent advanced design system’s (ADS) amplifier design guide. This can be used in determining the reflection coefficient of large signal S-parameters of the model. A load-pull simulation circuit with simple couplers for the input and output matching designs are illustrated in figure 4. At the input of the circuit, the coupler is connected between a signal generator and the transistor in order to examine the incident voltage from the source and reflected voltage reflected from the transistor. At the output of the amplifier, the output coupler is connected to oversee the signal at this section. It should be taken into account that these couplers are not proposed to be practicable hardware components, although are defined in ADS software as the operation of converting actual current and voltage into corresponding forward and reverse wave components [5]. The reflection coefficient of the transistor is derived in this equation as:

\[
\Gamma = \frac{V_{\text{ref}}}{V_{\text{in}}} \quad (1)
\]

The hypothesis behind designing a circuit for load-pull simulation is to optimally achieve high load impedance at the fundamental frequency of a power amplifier. Load-pull is important in class-F amplifiers. Load-pull approach is used in the class-F power amplifier with algorithm to improve the fundamental load impedances. The load impedances are controlled in a one-port device as S-parameter data. The S-parameter data are used in the class-F power amplifier biasing operation at fundamental frequency to increase efficiency and output power. These useful characteristics of the load-pull are essentially component of the Agilent Advanced Design System software package. However, the simulation procedure is to:

- Arbitrarily, position a middle point and radius for a circle on smith chart.
- Position the number of points in the circle of the Smith Chart. Each point of the circle presents a specific value of the load impedance.

- Change the position of the circle on the chart to produce the optimal load impedance. Moreover, the source and load impedances at given harmonic frequencies are set to be 50Ω.

Now, the aim of this work is to propose a simple design method that can make straightforward ways of designing a matching network for optimal load impedance. After comprehensive load-pull and optimization simulations, the input impedance and optimal load impedance can be obtained. The impedances are computed in magnitude and angle form as (1.04-j*29.13) Ω and (35.85+j*55.30) Ω. Furthermore, the impedances are also used in calculating and designing the input and output matching networks. The Harmonic load-pull simulation circuit is composed of input and output matching networks as illustrated in figure 5.

![Figure 5: Harmonic load-pull simulation circuit with input and output matching circuits.](image)

After the Harmonic load-pull simulation circuit design with the matching networks, results from simulation have been illustrated in figure 6. The results from large signal s-parameter have shown S11, S12, S21 and S22. The linear gain and return loss of the power amplifier have indicated a good performance levels. On the other hand, the optimal load impedance was still found to be (35.85+j*55.30) Ω with the same input signal. This method is projected to increase the level of efficiency with higher output power.

![Figure 6: Gain and return loss.](image)
The obtained optimal load impedance was used in the microstrip transmission lines to link the circuit components. An Ultralam 2000 substrate of $\varepsilon_r = 4.3$, thickness $h = 1.6$mm, metal thickness $T_m = 0.035$mm and $\tan\delta = 0.0023$ were used in the design.

The design method and implementation process have been well explained. To verify the design standard, a design example at 3.50 GHz, centre frequency was applied. Performance of the power amplifier could be better with an active integrated antenna. The final design of amplifier by wave shaping which controls the harmonic load impedances has been implemented. One intention is to try to design a novel harmonic suppression antenna, which will then be applied to the integrated active antenna design approach.

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