64QAM wireless link with 300GHz InP-CMOS hybrid transceiver

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Abstract This letter presents a 300GHz hybrid transceiver using CMOS and InP-HEMT, which achieves a maximum data rate of 56Gb/s. A 300GHz CMOS transceiver with a mixer-last transmitter mixer-first receiver is utilized to up- and down-convert the V-band IF signal to the 300GHz-band, while InP-HEMT is used for PA and LNA design. The transceiver also achieves wireless communication in ch.13–24 (1.76Gbaud), ch.39–44 (3.52Gbaud), ch.52–54 (7.04Gbaud) and ch.59 (10.56Gbaud) with lower than -16.7dB EVM. 64QAM modulation is also achieved for a 5Gbaud symbol rate. The CMOS transmitter and receiver consume 0.29W and 0.17W from a 1V supply, respectively, and the InP-HEMT PA and LNA consume 1.44W from a 1.2V supply.

key words: 300GHz-band, Wireless link, CMOS, 65nm, InP-HEMT

Classification: Integrated circuits (RF)

1. Introduction

Frequencies around 300GHz are attracting attention as candidates for beyond-5G wireless communication systems. The wide available bandwidth around these frequencies enables many future applications for ultra-high data rate links. To respond to such growing interest, new standards and regulations are being considered including the IEEE Std. 802.15.3d amendment [1, 2] and the new ITU regulations [3]. At these frequencies, designing reliable wideband amplifiers with acceptable gain and output power characteristics using the CMOS process is still a very difficult task as the transistor \( f_{\text{max}} \) is normally lower than 300GHz. Many works have utilized the 300GHz-band to achieve high data rates up to 120Gb/s using compound semiconductors as in [4, 5, 6, 7, 8, 9, 10, 11, 12, 13]. The high \( f_{\text{max}} \) makes it possible to design PAs and LNAs with high gain and good linearity resulting in an excellent EVM performance. However, the compound semiconductor process-based systems are costly, very difficult to integrate, and large-scale digital circuits are not feasible in most cases reducing the system’s overall feasibility.

Silicon-based processes such as SiGe also have an \( f_{\text{max}} \) that exceeds 300GHz, which means that it is still possible to realize good amplifier performance as in [14, 15, 16, 17, 18]. SiGe is also suitable for integration to some extent, even for digital processing circuits.

The CMOS process is still more desirable as the main system process due to its low cost, excellent area efficiency, and high integration ability. CMOS amplifiers operating around 300GHz were introduced in the literature despite the low \( f_{\text{max}} \) as in [19, 20], but a reliable wideband operation is yet to be demonstrated. Many works sacrificed the presence of an amplifier to realize the 300GHz wireless link using CMOS [21, 22, 23, 24, 25, 26, 27, 28, 29, 30]. The resulting mixer-last transmitter, mixer-first receiver system has very severe mixer linearity requirements, causing the overall system complexity to increase in order to get a reliable high data rate link.

In this work, a CMOS transceiver is used to up- and down-convert the IF signal to and from 300GHz, and InP-HEMT amplifiers are placed as PA and LNA, forming a hybrid transceiver that has the CMOS part which improves the integration between the transceiver front-end and the baseband circuitry, and the InP-HEMT part that provides the gain, linearity, and noise figure improvement at the transmitter output and the receiver input. One of the biggest challenges facing the hybrid system is the difficulty of the over the air (OTA) link evaluation before implementation. The direct implementation of the CMOS-InP connection on a board or in a module for link evaluation is not a practical choice at 300GHz-band due to the limited acceptable connection methods that can be used to avoid having huge losses. To tackle this issue, we here introduce the measurement setup...
for OTA measurement using one probe station with waveguide probes and horn antennas. Section 2 explains the system architecture used in realizing the wireless link with the link budget analysis. In Section 3, the measurement setup and results of the wireless link are given. Finally, section 4 concludes the letter with a comparison table of the transceivers that operate at the 300GHz-band.

2. System architecture and wireless link analysis

The transceiver system used to evaluate the wireless link is shown in Fig. 1. The RF frequency band from 278GHz to 304GHz is covered by up-converting the 50–70GHz IF band using a tripled LO signal that can be tuned between 38–39GHz. The subharmonic mixer utilizes the second harmonic of the 114–117GHz LO input. The CMOS part consists of the mentioned subharmonic mixer, V-band IF amplifier, tripler, and LO buffers [28]. The InP-HEMT amplifiers are designed using power combining to improve the overall linearity [31].

The CMOS subharmonic mixer schematic is illustrated in Fig. 2(a). The push-push architecture provides a good conversion version gain of around -16.5dB for both the transmitter and the receiver cases, but the linearity evaluated by the OP1dB shown in Fig. 2(b) is limited to -16dBm due to the small transistor sizes which are chosen to reduce the parasitic capacitance.

The improvement on the SNDR by adding the InP-HEMT amplifiers to the CMOS system is shown in Fig. 3. An 8cm distance is considered in this calculation with 26dBi antenna gain for both transmitter and receiver antennas. A 5Gbaud symbol rate is used to evaluate the SNDR here using the following equation:

$$\text{SNDR} = \frac{P_{RX(OUT)}}{N_{RX} + IM3}$$

where $P_{RX(OUT)}$ is the signal output power of the receiver, $N_{RX}$ is the noise floor at the receiver output. The parameters of each component are estimated using simulations and de-embedded measurement results. From this calculation, it can be observed that the 15dB InP amplifier gain increases the transmitter output power, and hence, the power at the receiver antenna. The receiver gain is increased by the amplifier gain and its noise figure gets reduced to an estimated...
value of 18.8dB compared to the 32.8dB of the CMOS-only receiver (including the external losses such as antenna-CMOS connection). The total TX-to-RX calculated SNDR improves from 8.6dB to 25.5dB at a 5Gbaud symbol rate enabling 64QAM communication by adding the InP amplifiers to the system as shown in Fig. 3(b) and (c). Assuming that a 2dB connection is realized for on-board implementation, the estimated SNDR improves to 27.9dB over twice the distance as shown in Fig. 3(c). This estimation indicates that a low-loss connection is crucial for hybrid transceivers.

### 3. Measurement results

The measurement setup used to evaluate the 300GHz wireless link is shown in Fig. 4. The data is generated using an arbitrary waveform generator and up-converted externally to the V-band. The 300GHz output signal is applied to the waveguide InP-HEMT amplifier module through a waveguide probe. Waveguide bends are used to align the antennas on the probe station. The 26dB waveguide horn antennas are directly connected to the amplifier modules. The receiver V-band output is directly evaluated by a 70GHz oscilloscope after external amplification to compensate for the CMOS-to-PCB connection loss. The equalizer function of the oscilloscope is used with 261 filter taps. The horn antennas are 5.6cm long, so the distance between the phase centers is estimated using the horn-to-horn measured propagation loss.

Fig. 5 shows the measured EVM for several symbol rates with an estimated distance of 2.5cm. 16QAM is achieved for symbol rates up to 14Gbaud resulting in a maximum data rate of 56Gb/s. 64QAM is also achieved at a maximum sym-
bol rate of 5Gb/s (30Gb/s). The measured 5Gb/s EVM with swept input power over the same distance is shown in Fig. 6. Fig. 7 summarizes the measured performance for the main IEEE 802.15.3d standard channels and the maximum data rate condition. 64QAM modulation is usable in several channels such as ch. 20 and ch. 42. The maximum data rate achieved using a standardized channel is 42.24Gb/s (ch. 59).

4. Conclusion

Table I shows a performance comparison with the other transceivers that operate at frequencies from 200GHz to 300GHz. The introduced hybrid transceiver achieves a relatively high data rate while keeping most of the system components in the CMOS chip. The achieved SNDR is also high enough to realize 64QAM communication. This demonstration shows that the digital-friendly CMOS process can be combined with the high-speed compound semiconductors to leverage the pros of the sub-THz band. Using the CMOS process makes it possible to integrate more complicated circuits as in SoCs where powerful processing circuitry can be directly connected to the transceiver on the same chip.

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