On Designing Computing Systems for Autonomous Vehicles: a PerceptIn Case Study

Bo Yu  
PerceptIn Inc.  
bo.yu@perceptin.io

Jie Tang*  
South China University of Technology  
cstangjie@scut.edu.cn

Shaoshan Liu  
PerceptIn Inc.  
shaoshan.liu@perceptin.io

ABSTRACT
PerceptIn develops and commercializes autonomous vehicles for micromobility around the globe. This paper makes a holistic summary of PerceptIn's development and operating experiences. This paper provides the business tale behind our product, and presents the development of the computing system for our vehicles. We illustrate the design decision made for the computing system, and show the advantage of offloading localization workloads onto an FPGA platform.

CCS CONCEPTS
• Computer systems organization → Robotics.

KEYWORDS
autonomous vehicle, FPGA, localization

1 INTRODUCTION
PerceptIn was established in 2016 to develop visual perception technologies for autonomous vehicles and robots. Since its inception, PerceptIn has successfully attracted over $10 million of venture capital funding, from Walden International, Matrix Partners, and Samsung Ventures [1]. PerceptIn is an international technology startup with operations in the U.S., Japan, Europe, and Asia. PerceptIn consists of over 30 researchers and engineers and 10 business professionals. The business professionals are responsible for business development in different markets and gather feedback for the company’s R&D efforts, whereas the engineers and researchers are responsible for developing cutting edge autonomous driving technologies. In the past three years, PerceptIn has generated over 20 U.S. patents and over 100 international patents, as well as numerous research papers.

*corresponding author
costs over $10,000. Besides the cost issue, these computing systems mostly accelerate only the perception function in autonomous driving, whereas PerceptIn require a system that optimizes the end-to-end performance. So we soon concluded that this option was not viable.

Option three, Development of proprietary autonomous driving computing systems: developing a proprietary computing system guarantees that PerceptIn have the most suitable system for PerceptIn’s customers and for its workloads, but also means that PerceptIn need to invest a significant amount of financial and personnel resources on this project. Also, the investment does not guarantee the success of this project. It is a huge and risky bet for a startup like PerceptIn.

After an unsuccessful exploration with option one, starting in early 2018, PerceptIn decided to move forward with option three and PerceptIn thus formed a team to develop the FPGA-based DragonFly computing system [8][9][10][11][12]. Option three was a huge success, today all autonomous vehicles shipped by PerceptIn are empowered by PerceptIn’s proprietary DragonFly computing system. In this paper, from a technical perspective we explained how we designed the PerceptIn’s DragonFly computing systems, and the design trade-offs that we faced.

For the rest of this paper, we first introduce the sensor suites of our vehicle (Sec. 2), and then present the end-to-end processing pipeline exercised by the on-vehicle computing systems (Sec. 3). Based on the processing pipeline, we then describe the on-vehicle computing system design (Sec. 4). To reduce the end-to-end computing latency, we offload the localization to an FPGA platform. Sec. 5 presents FPGA based vSLAM (visual simultaneous localization and mapping) front-end and back-end systems designed for our vehicle.

2 OUR VEHICLES AND SENSOR SUITE

We first briefly introduce our product and sensor suite deployed on our vehicle in order to provide contexts for the rest of the paper.

Our vehicles are electric cars that are powered by batteries. We provide two autonomous vehicles designs: 2-seater pods targeting private transportation experiences, and 8-seater shuttles targeting public autonomous driving transportation services. Both designs are capped at 20 mph to suit the unique needs of micromobility.

The unique scenarios of micromobility let us build affordable autonomous vehicles. We use cameras as the major sensor for the perception and localization, and develop the sensor suite, DragonFly, for our vehicle. DragonFly integrates two sets of stereo cameras, which cover forward and backward regions respectively, and an IMU (Inertial Measurement Unit) for pose estimation. Besides cameras, radars and sonars are used to cover the short range regions and to provide the 360 degree of perception coverage.

3 ALGORITHM PIPELINE

Processing pipeline. Fig. 2 shows the block diagram of the processing pipeline in our vehicle, which consists of three parts: sensing, perception and planning. The sensing module bridges sensors and the computing system. It synchronizes various sensor samples for the downstream perception module, which performs two fundamental tasks: 1) locating the vehicle itself in a global map and 2) understanding the surroundings through depth estimation and object detection. The planning module uses the perception results to devise a drivable route, and then converts the planned path into a sequence of control commands, which will drive the vehicle along the path. The control commands are sent to the vehicle’s Engine Control Unit (ECU) via the CAN bus interface.

Algorithm. Our localization module is based on Visual Inertial Odometry algorithms [13, 14], which fuses camera images, IMU and GPS samples to estimate the vehicle pose in the global map. The depth estimation employs traditional stereo vision algorithms, which calculates depths according to the principal of triangulation [15]. In particular, our method is based on the classic ELAS algorithm, which uses hand-crafted features [16]. While DNN models for depth estimation exist, they are orders of magnitude more compute-intensive than non-DNN algorithms[17] while providing only marginal accuracy improvements to our use-cases.

We detect objects using DNN models. Object detection is the only task in our current pipeline where the accuracy provided by deep learning justifies the overhead. An object, once detected, is tracked across time until the next set of detected objects are available. The DNN models are trained regularly using our field data. As the deployment environment can vary significantly, different models are specialized/trained using the deployment environment-specific training data. We use the Kernelized Correlation Filter (KCF) [18] to track detected objects. The planning algorithm we used is based on Model Predictive Control (MPC)[19].

Task-Level Parallelism. As shown in Fig. 2, sensing, perception and planning are serialized. They are all on the critical path of the end-to-end latency. We pipeline the three modules to improve the throughput. Different sensor processes (e.g., IMU vs. camera)
We will discuss later.

This section shows the hardware design space explored during our work.

Figure 3: Performance and energy comparison of four different platforms running three perception tasks.

are independent. Within perception, localization and scene understanding are independent and could execute in parallel.

While there are multiple tasks within scene understanding, they are mostly independent with the only exception that object tracking must be serialized with object detection. The task-level parallelisms influence how the tasks are mapped to the hardware platform as we will discuss later.

4 ON-VEHICLE COMPUTING SYSTEM

4.1 Hardware Design Space Exploration

This section shows the hardware design space explored during our development.

Mobile SoCs. Since our vehicles targets micromobility with low speed, which has much in common with mobile robots, high-end mobile SoCs that have been demonstrated on robots are initially explored. However, we found that mobile SoCs are ill-suited for autonomous driving as the main computing device. The major reason is that the compute capability of mobile SoCs is too low for realistic end-to-end autonomous driving workloads.

Fig. 3 shows the latency and energy consumption of three perception tasks—depth estimation, object detection, and localization—on an Intel Coffee Lake CPU (3.0 GHz, 9 MB LLC), Nvidia GTX 1060 GPU, and Nvidia TX2, which represents today’s high-end mobile SoCs. On TX2, we use the Pascal GPU for depth estimation and object detection, and use the ARM Cortex-A57 CPU (with SIMD capabilities) for localization, which is ill-suited for GPU due to the lack of massive parallelisms. Fig. 3a shows that TX2 is much slower than the GPU, leading to a cumulative latency of 844.2 ms for perception alone. Fig. 3b shows that TX2 has only marginal, sometimes even worse, energy reduction compared to the GPU due to the long latency.

On the other hand, although rich general IO ports are available on mobile SoCs, sensor processing supports in hardware, which is critical for multi-sensor fusion algorithm, are missed. For example, autonomous vehicles require very precise and clean sensor synchronization for accurate pose estimations, which mobile SoCs do not directly provide.

FPGA vs GPU. We implement depth estimation, YOLO [20] and ORB front-end on a Xilinx Zynq UltraScale+ FPGA and Nvidia GTX 1060. For FPGA design, we write RTL codes and use Xilinx Vivado for implementation. For GPU design, we implement depth and ORB front-end algorithm using CUDA.

Fig. 3b compares the latency of the perception tasks on the FPGA with the GPU. The GPU is faster than the FPGA on depth estimation and object detection mainly due to the highly parallel and regular operations in these image processing pipeline. The FPGA is faster than the GPU on localization, which inherently lacks massive parallelisms and is more lightweight than other tasks.

4.2 Hardware Architecture

The results from our hardware exploration motivate the on-vehicle computing system design. Fig. 4 illustrates an overview of the on-vehicle computing system. It includes sensors and a server+FPGA heterogeneous platform. Components that are not on the critical path, such as Radar and Sonar, are not shown here.

Considering the cost, compute requirements and power budget, our computing platform is composed of a Xilinx Zynq UltraScale+ FPGA and an on-vehicle PC equipped with an Intel Coffee Lake CPU and an Nvidia GTX 1060 GPU. The PC is the main computing platform, while the FPGA plays a critical role, which bridges sensors and the PC, and provides an acceleration platform.

Algorithm mapping. We map sensing to the Zynq FPGA platform, which essentially acts a sensor hub. It processes sensor data and transfers sensor data to the PC for subsequent processing. The Zynq FPGA hosts an ARM-based SoC and runs a full-fledged Linux OS, on which we develop sensor processing and data transfer pipelines.

We assign the planning tasks to the CPU of the on-vehicle server, for two reasons. First, the planning commands are sent to the vehicle through the CAN bus; the CAN bus interface is simply more mature on high-end servers than embedded FPGAs. Executing the planning module on the server greatly eases deployment. Second, we optimize our planning algorithm for micromobility, which leads to an extreme lightweight algorithm. We use a lane-level map instead of the grid high precision map. The search and optimization space of feasible trajectories is greatly reduced. On our computing system, the planning only contributes to about 1% of end-to-end latency.
Perception tasks include scene understanding (depth estimation and object detection/tracking) and localization, which are independent and, therefore, the slower one dictates the overall perception latency. Our design offloads localization onto the FPGA while leaving other perception tasks on the GPU. This partitioning also frees more GPU resources for depth estimation and object detection, further reducing latency.

When both scene understanding and localization execute on the GPU, they compete for resources and slow down each other. Scene understanding takes 120 ms and dictates the perception latency. When localization is offloaded to the FPGA, the localization and scene understanding are executed in parallel. Since scene understanding is more computationally intensive, scene understanding is still on the critical path, but its latency reduces to 77 ms. Overall, the perception latency improves by 1.6 ×.

5 FPGA BASED LOCALIZATION SYSTEM

This section presents an FPGA based localization front-end and back-end designed for our vehicles, which accelerates stereo ORB SLAM [21].

Modern FPGA platforms are built with rich and mature sensor interfaces and image processing IPs. As a result, our FPGA platform directly interfaces with the stereo cameras on DragonFly, of which image resolution is 1280 × 720 pixels. We designed FPGA circuits to synchronize two cameras by triggering cameras at the same time. Sensor synchronization is crucial to perception algorithms, which fuse multiple sensors. Out-of-sync sensor data is detrimental to perception. For stereo vision, even small temporal offsets will lead to large depth estimation error, which further compromise the accuracy of the localization algorithm.

5.1 Algorithm

Our SLAM system includes two components: the front-end and the back-end. The front-end extracts image features and associates features in consecutive frames to physical landmarks. It incrementally deduces the robot motion by applying geometry constraints on the associated sensory observations. The back-end tries to minimize errors introduced by the process and measurement noises by performing optimizations on a batch of observed landmarks and tracked poses.

5.1.1 Front-end. The front-end consists of two parts: ORB feature extraction and feature association.

- **Feature Extraction.** The front-end first extract key points on 2D images, which correspond to salient landmarks in the 3D world. The pipeline of ORB feature extraction is shown in Fig. 5. The input is a gray image. An n-level image pyramid is constructed to make the feature scale invariant. In our design, n is 2, which makes a trade-off between algorithm accuracy and computational intensity. Key points are detected using FAST feature on pyramid images. If a feature is detected, the orientation of the feature point is calculated to make the feature rotation invariant. Feature descriptors are computed on Gaussian blurred images using steered BRIEF descriptor. Lastly, feature descriptors of resized images are scaled back to the original image.

- **Feature Association.** This module compares features’ descriptor in two images and associates features that correspond to the same landmarks. We use 256 bits descriptors for features, and use Hamming distance between descriptors as the matching criteria. The pair of feature, of which Hamming distance is below a threshold, is considered as a matched pair. To improve matching accuracy, SAD (sum of absolute differences) rectification is applied. Comparing all the pairs of features in two images to find matched features is computationally expensive. The relative rotation and translation between two images provide geometry constraints on the corresponding features in the image pair, which limit the searching space on a band region on the image. We use IMU data to get the movement between two consecutive images, and get relative rotation and translation of stereo cameras from the sensors’ calibration process [22]. In the system, the relative rotation and translation between images pairs and its constraints are employed to find matched features.

5.1.2 Back-end. The front-end produces initial estimations of landmark positions and camera poses. The back-end further refines camera trajectories and 3D structures. We use bundle adjustment as the back-end method.

Bundle adjustment [23] is actually an optimization problem, which is formulated by Eq. (1). \( P(p_i, e_j) \) is the camera projection model that projects a 3D point in the world coordinate, \( p_i \), to a 2D point on the image plane. \( j \cdot e_j \) represents the parameters of the \( j \) - th camera pose. \( o_{ij} \) is the feature corresponding to the \( j \) - th point on the \( i \) - th image. \( e_{ij} \) is the discrepancy between the observation and the projection function.

In the equation, \( e_{ij} \) evaluates to 1 if the \( i \) - th 3D point is observed by the \( j \) - th camera, otherwise 0. This formulation shows that solving the bundle adjustment problem is to determine camera
parameters and 3D points’ positions such that observations are closely approximated by the corresponding re-projection points. Fig. 6 is an example of bundle adjustment. The initial estimations of the 3D point’s position and the camera’s extrinsic parameter are $\hat{p}_1$ and $\hat{c}_j$. After bundle adjustment, $p_i$ and $c_j$ are obtained.

$$\min_{p_i, c_j} \sum_{i=1}^{a} \sum_{j=1}^{b} \sigma_{ij} \|o_{ij} - P(p_i, c_j)\|$$  (1)

Figure 6: An example of bundle adjustment. The initial estimations of the 3D point’s position and the camera’s extrinsic parameter are $\hat{p}_1$ and $\hat{c}_j$. After bundle adjustment, $p_i$ and $c_j$ are obtained.

We use LM (Levenberg-Marquardt’s) algorithm [24], which is widely adopted by both industry and academia, to solve bundle adjustment. The LM algorithm includes five parts, which are Jacobian updates (JU), Schur elimination (SE), Cholesky factorization (CFS), cost function computation (CC) and gain ratio evaluation (GRE). To solve non-linear optimization problems, LM algorithm iteratively use Jacobian to linearize the problem and solve the linear equation at each iteration to obtain an update. Schur elimination is used to reduce the dimension of the linear equation, thus reduce the computational complexity. Cholesky factorization is employed to solve the linear equation to get an update of the solution. Cost function and ratio evaluation are used to determine if the update reduce the cost effectively. The update will add to the current solution if the update is effective.

### 5.2 Hardware Architecture

We implement the front-end and back-end algorithm on a Xilinx Zynq Ultrascale+ ZCU102, which integrates a quad-core ARM Cortex-A53 CPU with an FPGA on the same chip.

**Front-end Architecture.** Fig. 7 illustrates the front-end hardware architecture. The input (left and right) images are buffered on-chip. The two images go through feature extraction and data association. The left and right camera streams are time-multiplexed in the feature extraction block to save hardware resources. The feature extraction block implements the ORB feature extraction in Fig. 5, which consists of three tasks: oFAST feature point detection (fast feature detection and orientation calculation), image filtering, and descriptor calculation.

The feature extraction block is exercised by both the left and right images. Features and descriptors of a image pair are used by the data association block to get matched feature pairs. The depth of the landmark associated with the feature is calculated according to the disparity of the matched feature. Depths and associated features are then used to initialize a 3D feature map and poses, which are implemented on the embedded processor. Then, the estimated 3D features and camera poses are transferred to the back-end hardware.

**Back-end Implementation.** We profile the LM algorithm on data-sets[25]. Jacobian updates (JU), Schur elimination (SE), cost function computation (CC) are the top three time-consuming parts, of which computations account for 51%, 29.8% and 10.45% of total time.

We propose a hardware-software co-design [10] in which the time-consuming parts JU, SE and CC are accelerated by the hardware; Cholesky factorization (CFS) and gain ratio evaluation (GRE) are implemented by the software. DMA is used for data exchange between the hardware and software. The hardware optimizes camera poses and feature maps in a sliding window manner. The maximum window size, i.e. the number of camera poses, is 50.

### 5.3 Evaluation Results

We evaluate the front-end and back-end respectively on a Zynq Ultrascale+ ZCU102, which integrates a quad-core ARM Cortex-A53 CPU with an FPGA on the same chip.

**Resource consumption.** Table 1 summarizes the hardware resource consumption of the front-end and back-end. Front-end dominates the resource consumption. The front-end and back-end consume too much BRAM to be fitted together in one Zynq FPGA chip. To solve this problem, we take a holistic approach to optimize the on-chip memory and logic of the SLAM system (will appear in [26]).

**Performance.** Table 2 shows the performance comparison between front-end and back-end FPGA and Intel CPU. Compared with Intel CPU, front-end and back-end FPGA is 4.8 and 9.8 times faster, and reduce 96% and 92% power consumption.

### 6 SUMMARY AND DISCUSSION

This paper is a concise summary of PerceptIn’s efforts on designing the on-vehicle computing system for our commercial autonomous vehicles. By thoroughly characterize the workloads, we adopt a server+FPGA heterogeneous platform, in which localization front-end is offloaded to FPGA. By offloading, the perception latency
improves by 1.6×. In retrospective, PerceptIn shipped its products globally, but delayed by six months because PerceptIn took an R&D detour to explore using existing mobile SoCs for autonomous driving workloads. If PerceptIn had chosen to develop its proprietary computing system initially, PerceptIn would have greatly widened its moat, and enlarging its edge over competitions. The root cause behind this problem was that we didn’t have any good tools to help us quickly explore the design space, and to identify the right design decision. In general, we feel that the whole community of autonomous machine computing system development, regardless whether it is academia or industry, are exploring in an enormous design space, and we are limited by the tools available to us. As a next step of our research, we will focus on developing the necessary scenario simulators, benchmarks, data sets, and SoC simulators needed to accelerate the design flow for autonomous machine computing systems.

### REFERENCES

1. S. Liu, "Critical business decision making for technology startups: A perceptin case study," *IEEE Engineering Management Review*, 2020.
2. S. Liu and J.-L. Gaudiot, "Autonomous vehicles lite self-driving technologies should start small, go slow," *IEEE Spectrum*, vol. 57, no. 3, pp. 36–49, 2020.
3. A. Santos, N. McGuckin, H. Y. Nakamoto, D. Gray, S. Liss et al., "Summary of travel trends 2009 national household travel survey," United States. Federal Highway Administration, Tech. Rep., 2011.
4. S. Liu, *Engineering Autonomous Vehicles and Robots: The DragonFly Modular-based Approach*. John Wiley & Sons, 2020.
5. S. Liu, J. Tang, Z. Zhang, and J.-L. Gaudiot, "Computer architectures for autonomous driving," *Computer*, vol. 50, no. 8, pp. 18–25, 2017.
6. S. Liu, L. Liu, J. Tang, B. Yu, Y. Wang, and W. Shi, "Edge computing for autonomous driving: Opportunities and challenges," *Proceedings of the IEEE*, vol. 107, no. 8, pp. 1697–1714, 2019.
7. L. Liu, J. Tang, S. Liu, B. Yu, J.-L. Gaudiot, and Y. Xie, "π-architecture: A runtime framework to enable energy-efficient real-time robotic vision applications on heterogeneous architectures," *Computer*, vol. 54, 2021.
8. W. Fang, Y. Zhang, B. Yu, and S. Liu, "Dragonfly-+: Fpga-based quad-camera visual slam system for autonomous vehicles," *Proc. IEEE HotChips*, p. 1, 2018.
9. ——, "Fpga-based orb feature extraction for real-time visual slam," in *2017 International Conference on Field Programmable Technology (ICFPT)*. IEEE, 2017, pp. 275–278.
10. Q. Liu, S. Qin, B. Yu, J. Tang, and S. Liu, "π-b: Bundle adjustment hardware accelerator based on distribution of 3d-point observations," *IEEE Transactions on Computers*, 2020.
11. J. Tang, B. Yu, S. Liu, Z. Zhang, W. Fang, and Y. Zhang, "π-sc: Heterogeneous soc architecture for visual inertial slam applications," in *2018 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS)*. IEEE, 2018, pp. 8302–8307.
12. B. Yu, W. Hu, L. Xu, J. Tang, S. Liu, and Y. Zhu, "Building the computing system for autonomous micromobility vehicles: Design constraints and architectural optimizations," in *2020 53rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*. IEEE, 2020.
13. T. Qin, P. Li, and S. Shen, "Visor-mono: A robust and versatile monocular visual-inertial state estimator," *IEEE Transactions on Robotics*, vol. 34, no. 4, pp. 1004–1020, 2018.
14. K. Sun, K. Mohla, B. Pfommer, M. Wattersen, S. Liu, Y. Mulgaonkar, C. J. Taylor, and V. Kumar, "Robust stereo visual inertial odometry for fast autonomous flight," *IEEE Robotics and Automation Letters*, vol. 3, no. 2, pp. 965–972, 2018.
15. R. Szeliski, *Computer Vision: Algorithms and Applications*, ser. Texts in Computer Science. Springer London, 2010. [Online]. Available: https://books.google.com/books?id=bXzAlkODwa8C
16. A. Geiger, M. Roser, and R. Urtasun, "Efficient large-scale stereo matching," in *Proceedings of the 10th Asian Conference on Computer Vision*, 2010.
17. Y. Feng, P. Whatmough, and Y. Zhu, "Aeq: Accelerated stereo vision system," in *Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, ser. MICRO ’52, 2019, p. 643–656.
18. J. F. Henriques, R. Caseiro, P. Martins, and J. Batista, "High-speed tracking with kernelized correlation filters," *IEEE transactions on pattern analysis and machine intelligence*, vol. 37, no. 3, pp. 583–596, 2014.
19. A. Kelly, *Mobile robotics: mathematics, models, and methods*. Cambridge University Press, 2013.
20. J. Redmon and A. Farhadi, "Yolov3: An incremental improvement," 2018.
21. R. Mun-Artil and J. D. Tardós, "Orb-slam2: An open-source slam system for monocular, stereo, and rgb-d cameras," *IEEE Transactions on Robotics*, vol. 33, no. 5, pp. 1255–1262, 2017.
22. P. Furgale, J. Rehder, and R. Siegwart, "Unified temporal and spatial calibration for multi-sensor systems," in *2013 IEEE/RSJ International Conference on Intelligent Robots and Systems*, 2013, pp. 1280–1286.
23. B. Triggs, P. F. McLauchlan, R. I. Hartley, and A. W. Fitzgibbon, *Bundle adjustment—A modern synthesis*. Springer Berlin Heidelberg, 1999.
24. M. Lourakis and A. A. Argyros, "Is Levenberg-Marquardt the most efficient optimization algorithm for implementing bundle adjustment?" in *Computer Vision, 2009. CVPR 2009. IEEE Computer Society Conference on*, pp. 1526–1531.
25. S. Agarwal, N. Snavely, S. M. Seitz, and R. Szeliski, "Bundle adjustment in the large," in *European Conference on Computer Vision*, 2010, pp. 29–42.
26. Y. Gan, B. Yu, B. Tian, L. Xu, W. Hu, J. Tang, S. Liu, and Y. Zhu, "Eudoxus: Characterizing and accelerating localization in autonomous machines," (2020.

#### Table 2: Performance comparison between FPGA and Intel CPU.

|                | Front-end FPGA | Front-end CPU | Back-end FPGA | Back-end CPU |
|----------------|---------------|---------------|---------------|--------------|
| Latency (ms)   | 19.7          | 95            | 7.6           | 75           |
| Power (W)      | 2.3           | ~65           | 5.5           | ~65          |

a Back-end FPGA consists of JU, SE and CC.

![Figure 7: Front-end architecture, which consists of two parts: feature extraction and data association. On-chip memories are customized in different ways to suit different types of data reuse: line buffer (LB) supports sequential accesses, and scratchpad memory (SPM) supports irregular accesses.](image-url)