A Study of 4-level DC-DC Boost Inverter with Passive Component Reduction Consideration

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Abstract. This study is to analyze design principles of boost inductor and capacitor used in the 4-level DC-DC boost converter to realize size reduction of passive component referring to their attributes. The important feature of this circuit is that most of the boost-up energy is transferred from the capacitor-clamped to the output side which the small inductance can be used at the input side. The inductance of the boost inductor is designed by referring the inductor current ripple. On the other hand, the capacitance of the capacitor-clamped is designed by considering voltage stress on semiconductor devices and also the used switching frequency. Besides that, according to the design specifications, the required inductance in 4-level DC-DC boost converter is decreased compared to a conventional conventional DC-DC boost converter. Meanwhile, voltage stress on semiconductor device is depending on the maximum voltage ripple of the capacitor-clamped. A 50 W 4-level DC-DC boost converter prototype has been constructed. The results show that the inductor current ripple was 1.15 A when the inductors, 1 mH and 0.11 mH were used in the conventional and 4-level DC-DC boost converters, respectively. Thus, based on the experimental results, it shows that the reduction of passive components by referring to their attributes in 4-level DC-DC boost converter is achieved. Moreover, the decreasing of voltage stress on the semiconductor devices is an advantage for the selection of low ON-resistance of the devices which will contribute to the reduction of the semiconductor conduction loss. The integration result of boost converter and H-bridge inverter is also shown.

1. Introduction

Boost inverter is required in renewable energy (RE) systems in order to boost-up low input voltage from RE sources [1]–[3] due to difficulty to realize high input DC voltage. The bulky problem of passive components due to requirement of the component to boost-up the low input voltage is one of the major problem for a conventional structures [4][5]. A large inductor component is required in order to transfer energy from input to output sides. Multilevel structure offers interesting option to overcome the bulky of passive components used in conventional converter. Besides, interleaved structures have also an ability to reduce the bulky passive component [6][7]. However, for a single-phase operation and simplicity of the converter circuit, multilevel structure topology offers a good option [8][9]. The main advantage of multilevel structure topology is the inductors and capacitors will charge and discharge energies to the output side after it gets charged from input side. Due to the existence of capacitor-clamped, the inductor shares the transferred energy with the capacitor-clamped, thus the required inductance minimized [4][5][8][10]. Basically, the size and weight of the passive component can be reduced. The voltage stress on semiconductor devices is also reduced due to additional of semiconductor device in the multilevel DC-DC boost converter. This paper explains the
design principle of passive components which is inductors and capacitors in multilevel DC-DC boost converters. Conventional and 4-level DC-DC boost converters are considered for a boost inverter system in this study. The principles of conventional and 4-level boost DC-DC converters are defined. Then, the design of inductor and capacitor are discussed for both converters. The simulation and experimental results of the conventional and 4-level DC-DC converters are analyzed and discussed for the design parameters confirmation.

2. 4-level DC-DC Boost Inverter System

In the boost inverter system of this study, 4-level DC-DC boost converter is integrated with H-bridge inverter circuits as shown in Figure 1. The renewable energy source is considered constant where an open loop system is considered. The main interest of this study is 4-level DC-DC boost converter which has similar characteristics with conventional DC-DC boost converter. Even though, 4-level DC-DC boost inverter is known as a double stage system, the advantage of the multilevel structure topology is able to overcome the bulky problem of passive components.

![Figure 1. 4-level DC-DC boost inverter system.](image)

3. Principle of 4-level DC-DC Boost Converter

Basically, 4-level DC-DC boost converter consists of one boost inductor \( L \), two capacitor-clamped \( C_c \), one output capacitor \( C_{out} \) and six semiconductor devices, as shown in Figure 2(a). The output voltage \( V_{out} \) is expressed by (1), meanwhile the boost ratio \( \beta \) is expressed by (2). Thus the duty ratio \( D \) is controlled in order to varies the output voltage \( V_{out} \).

\[
V_{out} = \beta \times V_{in}
\]

(1)

\[
\beta = \frac{1}{1-D}
\]

(2)

Figure 2 (b) shows the operation modes of the 4-level DC-DC boost converter. Basically the 4-level DC-DC boost converter has six operation modes. In this study the boost ratio \( \beta \) is equal to 2 (\( D \) equal to 0.5) is considered.

4. Components Design Consideration

4.1. Inductor design principle

The inductor current ripple \( \Delta I_L \) is considered in order to design the boost inductor \( L \) \[4\] [11]. On the other hand, the current ripple \( \Delta I_L \) of the boost inductor \( L_B \) must be controlled in order to avoid discontinuous current mode (DCM) condition. Besides, when high switching frequency \( f_{sw} \) is used, \( \Delta I_L \) can be minimized. In Inductor current ripple \( \Delta I_L \) is expressed as follows,
\[
\Delta I_L = \frac{V_L}{L}T_L
\]  

(3)

where \(V_L\) is the inductor voltage and \(T_L\) is the charging time of the inductor.

Besides, in order to achieve maximum inductor current ripple \(\Delta I_L\), the maximum product of \(V_L\) and \(T_L\) must be achieved. Figure 3 shows the relationship between the product \((V_L \times T_L)\) against the duty ratio \(D\) for conventional and 4-level DC-DC boost converters. The maximum inductor current ripple is achieved at \(D\) equal to 1/2 \((V_L \times T_L\) is maximum). However, in the 4-level DC-DC boost converter it has three maximum current ripple when the duty ratios are 1/6, 3/6 and 5/6. Due to the lower value of maximum points of \(V_L \times T_L\), the inductance is reduced in 4-level DC-DC boost converter. Thus, the boost inductor in the conventional and 4-level boost converters are expressed as follows respectively,

\[
L_{2\text{-level}} = \frac{V_{\text{out}}}{2} \frac{T}{2} \frac{1}{\Delta I_{L(2\text{-level})}}
\]  

(4)

\[
L_{4\text{-level}} = \frac{V_{\text{out}}}{6} \frac{T}{6} \frac{1}{\Delta I_{L(4\text{-level})}}
\]  

(5)

If the inductance of the conventional DC-DC boost converter and in the 4-level DC-DC boost converter is compared with the same specifications, the ratio of between 4-level and conventional DC-DC boost converters is expressed in (5). The 4-level DC-DC boost converter required only 11.11% of the inductance.

\[
\frac{L_{4\text{-level}}}{L_{2\text{-level}}} = \frac{1}{9} = 0.1111 = 11.11\%
\]  

(6)

![Figure 2. 4-level DC-DC boost converter.](image-url)
4.2. Design of Capacitor-clamped principle

The voltage stress on switching devices can estimated by referring to the capacitor-clamped $C_C$ voltage. Switching frequency must be considered as well in estimating the capacitance. Basically, the voltage across capacitor-clamped are expressed follow,

$$V_{Cl(4-level)} = \frac{1}{3}V_{out}$$  \hspace{1cm} (7)

$$V_{C\text{c}(2\text{-level})} = \frac{2}{3}V_{out}$$  \hspace{1cm} (8)

The minimum capacitances $C_{Cc1}$ and $C_{Cc2}$ in the 4-level DC-DC boost converter are expressed as follow,

$$C_{Cc(4\text{-level})} = \frac{3P_D}{\left[6V_{\text{in}(4\text{-level})}\text{max} - 2V_{\text{out}}\right]} \frac{V_{\text{in}}}{f_{sw}}$$  \hspace{1cm} (9)

$$C_{Cc(2\text{-level})} = \frac{3P_D}{\left[6V_{\text{in}(2\text{-level})}\text{max} - 4V_{\text{out}}\right]} \frac{V_{\text{in}}}{f_{sw}}$$  \hspace{1cm} (10)

The maximum voltage stress on semiconductor device in 4-level DC-DC boost converter is expressed as follows,

$$V_{\text{max}(4\text{-level})} = \frac{1}{3}V_{out} + \frac{1}{2}V_{\text{in}}C_{Cc(4\text{-level})}\text{max} \frac{P_D}{f_{sw}}$$  \hspace{1cm} (11)

5. Results and analysis

In order to confirm the operation of the 4-level DC-DC boost converter, a prototypes is constructed. The specifications of the designed converter circuit are shown in Table 1.
Table 1. Specifications in the simulation and experiment for conventional and 4-level DC-DC boost converter.

| Specifications          | Value   |
|-------------------------|---------|
| Output power, $P$       | 50 W    |
| Inductor current, $I_{in}$ | 1.06 A |
| Input voltage, $V_{in}$ | 50 V    |
| Output voltage, $V_{out}$ | 100 V  |
| Switching frequency, $f_{sw}$ | 22 kHz|
| Duty ratio, $D$         | 0.5     |
| Boost inductance, $L_B$ | 1 mH    |
| Capacitor-clamped, $C_{Cc}$ | 470 μF |
| Output capacitor, $C_{out}$ | 470 μF |
| MOSFET                  | IRF840N |
| Diode                   | BYT79   |

5.1. Inductor current ripple, $\Delta I_L$

The inductor current ripple is observed by using the same boost inductance ($L = 1$ mH) for both converters. The inductor current ripple is designed at 127.42 mA for 4-level DC-DC boost converter meanwhile 1.15 A for the conventional boost converter. The simulation result shows a good agreement between design and simulation results as shown in Figure 4. It strengthened by the experimental result where the current ripple is approximately same with the simulation and design current ripple shown in Figure 5.

Figures 4 and 5 show the simulation and experimental results. Both results show a good agreement. The current ripple is approximately 127-128 mA ($D = 0.5$) from the simulation and experimental results in the 4-level DC-DC converter. Meanwhile, Figure 4(b) shows the current ripple is approximately 1.14-1.15 A from the simulation and experimental results in the conventional DC-DC converter. Thus the inductor current ripple is reduced in the 4-level DC-DC converter.

![Figure 4](image1.png)  
(a) 4-level DC-DC boost converter.  
(b) conventional DC-DC boost converter.  

Figure 4. Simulation results of the capacitor output voltage, capacitor-clamped voltage, input voltage and inductor current ripple ($C_{out} = 470 \mu F$, $C_{C} = 470 \mu F$, $L = 1$ mH).
5.2. Inductor voltage, $V_L$

In the conventional DC-DC converter, when $D$ is 0.5, charging time of the inductor is half of the switching period. This also occurred at the inductor voltage $V_L$ where the value becomes half of the output voltage $V_{out}$. However, in the 4-level DC-DC boost converter, the inductor voltage becomes $1/6$ of the output voltage and similar for the charging times of the inductor. Figure 6 shows the inductor voltage for 4-level DC-DC boost converter and conventional DC-DC boost converter and the results were confirmed with the designed values. The inductor voltage in the 4-level DC-DC boost converter needs only 33.3% of the conventional boost converter. Thus, the results of simulation and experimental show a good agreement.

5.3. Relationship between capacitance of the capacitor-clamped and output voltage ripple

The capacitances of the capacitor-clamped and output capacitor are considered in order to observe the relationship of the output voltage ripple and the capacitance used. To design the minimum capacitance of capacitor-clamped, the selection of semiconductor device voltage rating must be greater than the capacitor-clamped maximum operation voltage. Due to the explanation in [11], the capacitance of capacitor-clamped in 4-level DC-DC boost converter and the voltage ripple at the output is confirmed to be independent with each other. Thus, the capacitor-clamped can be design without affecting the voltage ripple at the output capacitor. Figure 7 shows the variation capacitances of the capacitor-clamped used in 4-level DC-DC boost converter.
5.4. Voltage stress on semiconductor device

In 4-level DC-DC boost converter, the voltage rating of the semiconductor device must greater than the maximum voltage of capacitor-clamped during operation. This is due to the charging condition of the capacitor-clamped where it reached the maximum value in certain mode operation. Thus, the voltage across on the semiconductor device can be based on the parallel connection with the capacitor-clamped. The switching frequency used is also influenced the design of the capacitor. When a high switching frequency is used, it will cause the time period become smaller, thus the time of charging and discharging of capacitor-clamped is reduced as well. It confirmed in the simulation results, when high switching frequency is used, the capacitor voltage ripple reduces and smaller capacitance can be used.

The conventional conventional DC-DC boost converter is suffered from high voltage stress on semiconductor devices due to parallel connection to output side. From the simulation result, it shows in Figure b(b), the MOSFET voltage is approximately same as the output voltage. Thus, the voltage rating of the semiconductor device use must be higher in order to withstand high voltage stress. However, the voltage stress on semiconductor device in 4-level DC-DC boost converter was greatly reduced. This is due to additional of semiconductor devices are used in 4-level DC-DC boost converter circuit. Figure 8(a) shows the voltage stress on the semiconductor devices is approximately same of the capacitor-clamped voltage, 33 V. The voltage stress on a semiconductor device in 4-level DC-DC boost converter is divided by three of the output voltage. In the experimental results, the input voltage is reduced by half due to the safety purposes. The output voltage was approximately 55 V. Figure 9 shows it is confirmed that the voltage stress on semiconductor devices are reduced greatly in 4-level DC-DC boost converter. The problems of improper charging and discharging of capacitor-clamped is reduced by considering a natural balancing circuit.
6. Integration

Figure 10 shows the results of the boost inverter system which the output of the boost inverter system is boosted in sinusoidal waveform as expected.

\[(V_{in} = 50 \text{ V}, L_B = 1 \text{ mH}, D = 0.5).\]

**Figure 9.** Experimental results of voltage stress on semiconductor device (MOSFET) in 4-level DC-DC boost converter circuit, \(V_{out} = 55 \text{ V} \).

**Figure 10.** Simulation result of 4-level DC-DC boost inverter system after integration.

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7. Conclusion

In this paper, the authors have discussed the design of passive components referring to their attributes in the 4-level DC-DC boost converter in order to solve the bulky problem of passive components which is suffered in conventional DC-DC boost converter. It confirmed that the inductance of the boost inductor can be reduced greatly in 4-level DC-DC boost converter. Besides, the simulation and experimental results show that the voltage stress on semiconductor devices in 4-level DC-DC boost converter circuit is reduced due to additional semiconductor devices and passive components. For the future works, closed loop control strategies may have applied to control power pulsation problem and unbalanced of the capacitor-clamped voltages.

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