How to Train Your Neural Network: A Comparative Evaluation

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Abstract—The field of deep learning has witnessed a remarkable shift towards extremely compute- and memory-intensive neural networks. These newer larger models have enabled researchers to advance state-of-the-art tools across a variety of fields. This phenomenon has spurred the development of algorithms for distributed training of neural networks over a larger number of hardware accelerators. In this paper, we discuss and compare current state-of-the-art frameworks for large scale distributed deep learning. First, we survey current practices in distributed learning and identify the different types of parallelism used. Then, we present empirical results comparing their performance on large image and language training tasks. Additionally, we address their statistical efficiency and memory consumption behavior. Based on our results, we discuss algorithmic and implementation portions of each framework which hinder performance.

Index Terms—neural networks, deep learning, distributed training, GPUs, performance, survey

I. INTRODUCTION

The previous decade witnessed an explosion in the development of machine learning algorithms. In particular, deep learning (DL), a subset of machine learning focused on using neural networks for function approximation, has gained widespread popularity. Deep neural networks (DNNs) have enabled the advancement of the state of the art in a plethora of research areas: ranging from visual recognition [1], [2], [3], [4], [5] and natural language processing [6], [7], [8], [9] to computational chemistry and computer systems [10], [11], [12], [13], [14], [15], [16], [17]. Their popularity stems from the DNN’s ability to automatically learn low-dimensional representations from high-dimensional unstructured data such as images, text and audio. Given enough data, the representations learned by these models are often superior to handcrafted features designed by domain experts.

The advances in accelerator technology, increased memory capacity per accelerator, and faster networks have encouraged users of deep learning to train neural networks with increasingly larger numbers of parameters. Figure 1 shows the increasing number of parameters in the largest networks since 2012. Often times, it is impossible to train such networks on a single accelerator either due to large execution time or insufficient memory capacity to fit these models. The latter problem is further exacerbated for contemporary neural architectures. For example, GPT-2, an extremely popular neural network used in NLP requires 84 GB of GPU DRAM for training. This has motivated recent works in parallelizing the task of deep learning: training large models using multiple GPUs on a single node [18], [19] or across multiple nodes connected by a network [20], [21], [22], [23], [24], [25], [26].

Different parallel frameworks offer different strengths and weaknesses in terms of performance (execution time for training), memory consumption, and statistical efficiency. Ben-Nun et al. [27] surveyed parallel DL frameworks and the different ways of exploiting the concurrency in neural networks in 2018. However, many new frameworks have emerged in the last three years, and the authors limited their discussion to a qualitative analysis. In this paper, we survey the most popular parallel DL frameworks available today and perform an empirical evaluation for the ones with open-source implementations to compare various metrics. This comparative evaluation can help users of deep learning select the best parallel framework for their training tasks.

We first present a comprehensive qualitative survey of the state of the art in parallel deep learning. We classify approaches for parallelization into three categories (defined in Section II): data parallelism, intra-layer parallelism (sometimes referred to as model parallelism), and inter-layer parallelism (sometimes referred to as pipelining.). We present the advantages and disadvantages of using each approach and discuss the capabilities of different frameworks that implement each type of parallelism.

An end user who needs a scalable DL framework for their training experiments needs to know which frameworks provide...
the best statistical efficiency in the shortest possible time. To the best of our knowledge, an empirical comparison of parallel DL frameworks has not been attempted before. We identify two popular training datasets and four neural networks to benchmark several open-source DL frameworks including DDP [22], PipeDream [23], ZeRO [20], Megatron [21], TorchGPipe [19], and LBANN [28]. We use metrics that matter the most to a deep learning researcher – epoch execution times, statistical efficiency, and memory consumption. We run our experiments on three different supercomputers and clusters that are built using different generations of NVIDIA GPUs (A100s, V100s, etc.). Through these experiments, we seek to develop a consensus on the suitability of parallel frameworks to different scenarios.

II. BACKGROUND

In this section, we first give a brief description of the terminology of deep learning. We then provide an outline of the three ways in which training of a deep neural network can be parallelized: data parallelism, intra-layer parallelism and inter-layer parallelism.

A. Definitions

Neural networks: In simple terms, neural networks are a class of parameterized function approximators. They can model very complex functions from extremely high dimensional data like images, audio, text and video. Unlike traditional ML algorithms that require manual feature engineering by domain experts, neural networks are able to automatically learn meaningful low dimensional representations from their input data.

Layers: Neural networks organize their computation into a sequence of layers. Each layer computes a non-linear transform of it’s input. Computation proceeds sequentially across the layers, with the output of a layer becoming the input of it’s successor layer. The first layer processes the input data. It is this hierarchical organization of layers that lends deep neural networks the power to generate useful high level representations in the latter layers.

Learning/Training and Loss: Learning or Training is defined as the task of selecting the weight values which can accurately compute the function that the neural network has to approximate. This is done by posing the problem as a parameterized optimization of a scalar proxy called the loss. The loss is designed in a way such that minimizing it leads to accurate function approximation. For training the input data is split into training and validation data. Training algorithms minimize the loss over the training data to find the optimum parameters for the neural network. In addition, the loss function is also calculated on the validation data at frequent intervals. This validation loss is not used for parameter optimization. Rather it is used to check the performance of the neural network on unseen data to make sure it is learning meaningful representations from the training data. A large disparity in the training loss and the validation loss is a sign that the neural network has memorized the training data and not learned anything meaningful.

Backpropagation: Backpropagation is the algorithm by which the gradients/derivatives of the loss w.r.t. the weights are calculated. Gradients are calculated in the reverse topological order starting from the final layer, i.e. if layer $i$ consumed the output of layer $j$, then layer $i$’s weight gradients are calculated first and used in the calculation of layer $j$’s weight gradients. This backward flow of gradients in the layers lends the name backpropagation to this process.

Gradient Descent and Learning Rate: Gradient Descent is the algorithm to find the optimal weights for the neural network. Given the dataset as input, the neural network calculates the scalar valued loss function. Gradients w.r.t the weights are calculated via backpropagation as described in the previous section. Weights are updated by subtracting from them the calculated gradient weighted by a positive scalar called the learning rate. This update ensures that the loss function is iteratively minimized with each update.

Mini-Batches, Epochs and Stochastic Gradient Descent: Using backpropagation to calculate weight gradients with the entire dataset as input can be expensive for large datasets. Hence, typically mutually exclusive and exhaustive subsets of the dataset are used iteratively for faster and more frequent weight updates. These subsets are called mini-batches and their cardinality is called the mini-batch size. Since a random subset of the dataset is used to approximate the gradient, the process is called stochastic gradient descent (SGD). An entire training iteration over the dataset by exhausting all the mini-batches is called an epoch.

Statistical Efficiency: A training algorithm is said to be statistically efficient if it requires a low number of epochs to converge to a target validation loss.

B. Parallel Deep Learning Methods

Data Parallelism: Data parallelism refers to an even division of training data among worker GPUs. Each GPU possesses a copy of the neural network along with it’s parameters. Gradient calculation via backpropagation proceeds independently on all GPUs. These gradients are then subject to a collective all-reduce operation before the weight update step of the optimizer. The all-reduce step can either take place synchronously after each mini-batch, or asynchronously using a central parameter server. Due to the simplicity of the idea, implementations of data parallelism are widely available in popular deep learning frameworks like PyTorch [22], and TensorFlow [29]. Figure 2 illustrates data parallelism across 4 GPUs.

Intra-layer Parallelism: Intra-layer parallelism distributes the work of a layer by dividing its computation across multiple GPUs. Parallelizing an entire neural network entails applying intra-layer parallelism to some or all of its constituent layers. Research in this area is focused on optimizing the multi-
C. Related Work

Pouyanfar et al. [33] and Ben-Nun et al. [27] comprehensively survey established techniques in sequential deep learning as well as distributed. Another survey [34] covers work in processing neural networks efficiently. Distributed training on big data software stacks (such as Spark and Hadoop) is explored by Lu et al. [35]. The network demands of parallel training are presented in [36] where typical communication workloads are profiled and characterized. Tang et al. [37] further character distributed training communication via analytical models and survey current practices. We also point the reader to the MLPerf benchmarks [1], which have become popular for comparing deep learning algorithms, frameworks, and hardware.

https://mlcommons.org/en/training-normal-07/

III. LITERATURE SURVEY

In this section we present a survey of current state-of-the-art techniques and implementations for each type of distributed learning. Table I provides an overview of each discussed framework.

| Framework       | Type of Parallelism | Largest Accelerator Count | Largest Trained Network (No. of Parameters) |
|-----------------|----------------------|---------------------------|---------------------------------------------|
| FlexFlow        | Hybrid               | 64 GPUs                   | 24M*                                        |
| PipeDream**     | Inter-Layer          | 16 GPUs                   | 138M                                        |
| DDP**           | Data                 | 256 GPUs                  | 155M                                        |
| GPipe           | Inter-Layer          | 8 GPUs                    | 557M                                        |
| MeshTensorFlow  | Intra-Layer          | 512-core TPUv2            | 4.9B                                        |
| Megatron        | Intra-Layer          | 512 GPUs                  | 8.3B                                        |
| TorchGPipe**    | Inter-Layer          | 8 GPUs                    | 15.3B                                       |
| KARMA           | Data                 | 2048 GPUs                 | 17B                                         |
| LBANN**         | Data                 | 3072 CPUs                 | 78.6B                                       |
| ZeRO**          | Data                 | 400 GPUs                  | 100B                                        |

*Note: FlexFlow does not provide a parameter size for the largest network it trains. We have defaulted to the largest network with a known network size cited in their paper.
**The following frameworks are compared quantitatively in Section IV

A. Data Parallelism

Data parallelism has been the go-to algorithm for parallelizing neural network training. Although it is a natural step in improving performance of deep learning models, it is not without its flaws.

1) Collective Communication Bottleneck: Data parallelism hinges on a synchronous all-reduce operation to gather the gradients across all GPUs. Naturally, this can become a bottleneck for contemporary neural networks having a large number of parameters. This problem is further exacerbated by the increasing computational capabilities of hardware accelerators.
The ensuing decrease in the computation to communication ratio increases the severity of this problem.

Initial attempts to reduce the communication overhead targeted introducing asynchrony in the stochastic gradient descent (SGD) algorithm [38], [39], [40]. However, Chen et al. [41] demonstrate that synchronous SGD and its variants converged faster with higher accuracy than their asynchronous counterparts.

Efforts to minimize communication bottlenecks continued. Zhang et al. [42] devise a strategy known as Wait-Free Back-propagation (WFBP) to interleave GPU and CPU computation and communication. WFBP reduces bursts in network traffic and lowers overall network strain. Using WFBP, Zhang et al. achieve speed-ups in training times in 16 and 32 single-GPU machines. WFBP has become the de-facto approach for data parallelism frameworks.

PyTorch DistributedDataParallel (DDP) [22], Horovod [43] and Livermore Big Artificial Neural Network (LBANN) [28] toolkit are three open source frameworks designed to assist in transitioning models into a distributed environment. Out of these frameworks PyTorch DDP has been extremely popular among the deep learning community due to its seamless integration with PyTorch [44]. Horovod is an implementation of WFBP for TensorFlow by Uber. LBANN accelerates parallelized deep learning by taking advantage of high performance computing hardware. These implementations share an uncanny similarity in the way they optimize WFBP. Instead of having an individual all-reduce call for each parameter tensor, they fuse parameter tensors into fixed size bins. All reduce calls are made at the granularity of these fused parameter bins. This increases network bandwidth utilization and thus the overall performance of these frameworks. Although the fused tensor bin-size is kept as a tunable hyperparameter, Li et al. [22] demonstrate that the default bucket size of PyTorch DDP i.e. 25MB is a reasonable choice for efficient scaling.

2) Memory Redundancy: Given the abundance of large training datasets, neural networks with increasingly larger number of parameters have led to tremendous gains in performance on a variety of training tasks. As models and datasets grow in size, GPU memory capacity becomes a major bottleneck. Data parallelism requires each GPU to store its own copy of the neural network. With larger models and datasets, the memory required to house the activations, gradients and parameters of these neural networks often exceed the capacity of a single GPU DRAM. Data parallelism is thus rendered infeasible for training large models without memory optimizations.

Zero Redundancy Optimizer (ZeRO) [20] is a framework built over PyTorch to reduce per-GPU memory consumption. The paper observes that most memory during training is occupied by optimizer states, gradients, and parameters. ZeRO partitions these model states across GPUs to remove memory redundancies. With ZeRO, memory reduction scales proportionally with the number of GPUs while communication overhead only increases by a constant factor of 1.5x. The paper finds improvements in model size, training performance, and scalability with 100 billion parameter models on up to 400 GPUs using Adam optimizer [45] and mixed precision. Researchers at Microsoft have used ZeRO to train one of the largest neural networks in language modeling literature: a 17B parameter neural network called the Turing-NLG.

Out-of-core training algorithms like NVIDIA’s vDNN [46] are often used to train neural networks on a single GPU with insufficient DRAM capacity. These algorithms move data back and forth between the CPU and the GPU to free up space on the GPU. KARMA [47] is a framework built over PyTorch that extends this out-of-core approach to data parallelism on multiple GPUs. They design an efficient algorithm for automatic offloading and prefetching of activations and parameters of the neural network to and from the CPU DRAM. These capabilities are further extended to support multi-GPU models by performing weight updates on the CPU. KARMA sees a 1.52x speed-up against other state-of-the-art out-of-core methods. It provides a way to utilize data parallelism for large models that would otherwise necessitate other frameworks.

3) Large Effective Mini-Batch Sizes: Data parallelism is most efficient with high per-GPU workloads. This is ensured by fixing the per-GPU mini-batch size. As an example, suppose a ResNet model with a per-GPU mini-batch size of 128 is trained over 64 GPUs. This is equivalent to an effective mini-batch size of 8192 on a single GPU. It has been empirically shown that an extremely large effective mini-batch size has an adverse effect on the statistical efficiency of neural network training [48].

The naive approach to compensate for this is to increase the learning rate (LR). Krizhevsky [49] proposes to scale LR linearly with mini-batch size. Problems emerge as more workers are added to accelerate training: large LR values result in accuracy losses and training instability.

Goyal et al. [48] propose a LR warmup scheme to combat accuracy loss. Training begins with a lower LR that slowly builds up to a target value following the linear scaling rule. The paper was able to train ResNet-50 with a mini-batch size of 8K and accuracy matching smaller mini-batch models.

You et al. [50], [24] devise Layer-wise Adaptive Rate Scaling (LARS) as an alternate approach to LR warmup. LARS adapts the global LR to create separate LRs per model layer based on the ratio between layer weights and gradient updates. The paper observes this ratio varies across layers and provides insight into the efficacy of a layer’s weight updates. You et al. utilize LARS to train AlexNet and ResNet-50 with a mini-batch size of 32K without accuracy loss.

LARS experiences inconsistent performance gains across different deep learning tasks. You et al. [51] propose a general strategy to adapt any iterative optimizer for large mini-batch training. They apply this strategy to create LAMB using the Adam optimizer as a base. Using LAMB, You et al. scale BERT training to a mini-batch size of 32K without performance degradation.
B. Intra-Layer Parallelism

State of the art training techniques in intra-layer parallelism span from fine-grained parallel implementations of numerical kernels to dividing the coarse-grained work of a single layer across processes. It is often used in conjunction with other parallelization strategies such as data or inter-layer parallelism.

1) Fine-Grained Parallelism: At the fine-grained level, many techniques draw from existing numerical methods and adapt them to deep learning. Matrix multiplication and convolutions are the most utilized kernels and have been the focus of much optimization from the ML and broader scientific community. Many accelerators and processors have paired software libraries which implement these kernels tuned to their hardware such as CuDNN [52], MIOpen [53], and OneDNN.

Accelerators have been at the core of fine-grained parallelism within a layer. Several works have introduced techniques, some ML based, for mapping layer computations to the hardware optimally [54], [55], [56]. Here a mapping is the tiling strategy, computation order, and parallelization strategy, hence, the search space for optimal mappings can be immense.

There has been recent interest in using hardware accelerators other than GPGPUs to train deep networks. FPGAs have emerged as a viable candidate in DNN acceleration due to their lower energy consumption compared to GPUs and the flexibility provided by their reconfigurability. Recent work has explored optimizing DNN operations on FPGA hardware [57]. More recently, novel architectures have been proposed to improve memory re-use and parallel performance [58], [59], [60].

2) Coarse-Grained Parallelism: Orthogonal to the fine-grained compute kernels there have been techniques developed to divide work inside a layer along coarser tensor dimensions. These typically involve using optimization algorithms and/or ML to identify optimal partitions of computation and data within a layer and then developing a parallel strategy for execution. Song et al. propose a method for finding communication optimal parallel strategies on accelerator arrays in linear time [61]. Similarly, Jia et al. introduce a novel Markov Chain Monte Carlo based search for finding optimal parallelization strategies, which encompasses intra-layer in its operator dimension [25].

MeshTensorFlow accomplishes a similar effect by mapping tensor dimensions to a n-dimensional processor array or "mesh" [32]. These tensors are split and/or replicated across the mesh, such that the computation can be done in parallel using the processor array. The framework itself provides an interface for users to define a layout. Any layout will produce the same results for the same problem, however, the memory footprint and performance can be greatly improved with an optimal layout.

Dryden et al [62] also propose several algorithms for partitioning convolution tensor dimensions with the goal of reducing all-reduce time during training. Their algorithms are available in the LBANN framework. Convolutions are also parallelized in [31] with a hybrid parallelism by extending data parallelism with parallelism in the spatial domain. For language-based models Megatron [21] achieves a similar parallelism by partitioning the blocks in transformer layers across processors. Megatron has been increasingly used as language models become more common and larger (see Figure 1). It has shown up to 74% weak scaling coefficient on 512 GPUs.

Dividing layer tensor dimensions across processors is, however, very sensitive to the layer type. For instance, fully connected layers involve an all-to-all computation and therefore all-to-all communication, which is more expensive the data parallelism’s all-reduce. Thus, to combat this some methods use strictly at compute graph operations and not model layers [25].

C. Inter-Layer Parallelism

True inter-layer parallelism can only be achieved by pipelining i.e. having multiple mini-batches active in the system at any given instance. There are two ways to achieve pipelining: with and without flushing. In this section, we discuss the pros and cons of both approaches. We also provide an overview of frameworks that implement these approaches.

1) Pipelining with Flushing: Pipelining with flushing divides a mini-batch into micro-batches of equal size. These micro-batches are injected one by one into the system. GPUs accumulate gradients from all the micro-batches in the system. A GPU updates it’s weights only after it has finished the backward pass of the last micro-batch. The next mini-batch and its corresponding micro-batches are injected after all the GPUs have finished updating their weights. This approach to pipelining is also called micro-batching. The number of micro-batches is usually kept to be much larger than the number of workers so that each worker can compute concurrently. Ensuring optimum hardware utilization requires having a large mini-batch size. To maintain statistical efficiency at large mini-batch sizes, the same set of solutions discussed in Section II-A3 can be used. Figure 5 shows pipelining with flushing in action. Worker GPUs incur idle time between the forward pass of the last micro-batch and the backward pass of the first micro-batch. These are called pipeline bubbles. They reduce the overall hardware utilization of the system. A load balanced mapping of layers to GPUs is absolutely critical to maximize performance. The load balancing algorithm must also be communication-aware. This is because activations and gradients exchanged at GPU boundaries can be in the magnitudes of GBs for large neural networks. An efficient implementation of pipelining with flushing must have load balancing support.

This idea was first introduced by Huang et al. in GPipe [18]. Using GPipe they trained a 557M parameter neural network - AmoebaNet-B [63] on the ImageNet [64] dataset and surpassed the state of the art in a number of downstream image classification tasks. TorchGPipe [19] is an unofficial open-source implementation of GPipe built on the PyTorch [44] backend. GEMS (GPU-Enabled Memory Aware Model-Parallelism System) [65] introduces a novel approach to increase hardware utilization. This framework proposes an
algorithm to train two neural networks concurrently using pipelining without flushing on multiple GPUs. They double the throughput of the system by overlapping the forward and backward passes of the two neural networks. We refer the reader to their paper for the details of their implementation. Recently ZeRO [20] and Megatron [21] also extended support for this approach towards inter-layer parallelism. TorchGPipe [19] provides a load balancing algorithm that seeks to balance the net execution time of the forward and backward pass of a micro-batch on each GPU. However, their algorithm ignores the communication overhead of exchanging tensors across GPU boundaries. Megatron divides the layers of a transformer across GPUs. This strategy is optimal because all the layers of a transformer are identical. ZeRO also provides an identical strategy that divides the layers equally across GPUs. Additionally they also support a load balancing algorithm that equalizes GPU memory consumption across GPUs. While Megatron and ZeRO support pipelining, it is not their preferred mode of execution for parallelizing neural networks.

2) Pipelining without Flushing: In this approach, the number of mini-batches active in the system is kept constant. As soon as a mini-batch finishes it’s backward pass on the first GPU, a new mini-batch is injected into the system to maintain full pipeline occupancy. Unlike pipelining with flushing, weight updates on a GPU take place as soon as it is done with the backward pass of a mini-batch. This method of pipelining seeks to increase hardware utilization by removing flushing induced bubbles in the pipeline. However, statistical efficiency of such a training algorithm falls drastically. This is due to a problem called weight staleness. Newer mini-batches in a pipeline encounter stale weights in forward passes which are yet to be updated with the backward pass of older mini-batches. This is one of the major reasons why pipelining without flushing has not seen widespread adoption. PipeDream [23] is a framework that implements pipelining without flushing. PipeDream employs an algorithm called weight stashing to counter weight staleness. We refer the reader to their paper for exact details of the implementation. Chen et al. [66] suggest predicting future weights from stale weights using a variant of SGD with momentum [67]. PipeDream also proposes a static load balancing algorithm that is communication aware. It instruments each layer and uses the profiling data in its load balancer. Their framework also has an additional provision to replicate compute-intensive layers across GPUs to increase their throughput. Replicated layers synchronize their gradients via all-reduce after each backward pass.

IV. EXPERIMENTAL SETUP AND DESIGN

In this section, we present a detailed overview of our empirical evaluation of a number of parallel deep learning frameworks.

A. Choice of Frameworks

We use DDP [22], ZeRO [20], Megatron [21], PipeDream [23], TorchGPipe [19], and LBANN [6] for our empirical analysis. This subset is representative of the three types of parallelism discussed in Section III. We select frameworks which have open-source implementations, are easy to setup, and have a relatively large user-base. We also tried to include MeshTensorFlow [32] and FlexFlow [25] in our set of frameworks. However, despite our best efforts we could not set them up successfully for experimentation on our machines.

B. System Hardware

Table II describes the systems and hardware used in our training. Lassen is an IBM machine at Lawrence Livermore National Laboratory with a Mellanox network. It currently sits at number 17 on the Top500 list. ThetaGPU is a GPU extension of the Cray XC40 Theta system. Vulcan is a heterogeneous GPU cluster at our institution. Each system was selected to be representative of typical machines used for DL training. Lassen is similar to other leadership HPC systems with GPU-dense nodes. The ThetaGPU extension of Theta with dense A100 nodes is more typical of current cutting edge AI machines. At the other end is Vulcan, which is representative of the machines used in smaller research groups for DL research.

1) Data Loading (I/O): The method of loading batches from storage into memory can have a significant impact on overall training performance. We mitigate this bottleneck on each machine by first copying the datasets into node-local SSDs before training. Data is loaded using PyTorch’s distributed data loader with several worker threads. MegatronLM implements their own data loaders, which we used with Megatron rather than PyTorch’s. In practice we found these to be much faster than the default PyTorch data loaders.

TABLE II: System information about the HPC platforms used for the experiments.

| System      | No. of Nodes | CPU        | Cores/node | GPU         | GPUs/node | CPU Mem. / Node (GB) | GPU Mem. / Node (GB) | GPU FP64 Peak (TFlop/s) |
|-------------|--------------|------------|------------|-------------|-----------|----------------------|----------------------|------------------------|
| Lassen      | 795          | IBM Power9 | 44         | NVIDIA V100 | 4         | 256                  | 64                   | 7.0                    |
| ThetaGPU    | 24           | AMD Rome   | 64         | NVIDIA A100 | 8         | 1024                 | 320                  | 9.7                    |
| Vulcan*     | 24           | Intel Xeon | 16         | NVIDIA GTX1080Ti | 4     | 128                  | 44/96                | 0.35/0.39              |

Quadro P6000

*Note: On Vulcan, VGG-16 jobs were run on GTX1080Ti’s. ResNet50 and GPT2 small/medium jobs were run on Quadro P6000’s.
2) **Mixed Precision:** Mixed precision training \[^{68}\] has recently gained a lot of traction as a tool to speedup the training of large neural networks. It essentially involves keeping two copies of the network parameters in single and half precision. All the computation, right up to the calculation of gradients is done using half precision to boost performance. However, the weight updates are applied to the single precision copy of the weight. Performing critical kernels with the lower precision leads to significant speed-ups with only minor changes necessary to preserve accuracy such as gradient scaling. Mixed precision computation can take advantage of the fast Tensor Cores present in modern hardware accelerators such as the NVIDIA V100 and A100 GPUs. For a fair performance evaluation of each framework we used mixed precision where available. That is on the V100 and A100 cards on Lassen and ThetaGPU. Of the frameworks we ran DDP, Megatron, LBANN, and ZeRO were the only ones that supported mixed precision with distributed training.

3) **Communication Libraries:** Similar to I/O implementations the communication libraries used can have significant impacts on overall performance. The implementation of collective routines and GPUDirect support are the most impactful parts of the communication library. Where available we use NVIDIA’s NCCL library for distributed communication. For PipeDream we used the Gloo \[^{69}\] backend as recommended by its original publication.

### C. Datasets and Neural Networks

We evaluate the aforementioned subset of frameworks on two popular deep learning tasks: image classification and language modeling. For the former task, we use The ImageNet Large Scale Visual Recognition Challenge (ILSVRC) 2012 dataset \[^{64}\]. This dataset has been widely used to train large state of the art image classification neural networks throughout the last decade. It consists of more than a million RGB images of dimension 224x224 evenly divided across 1000 image classes. We use this dataset to train the VGG-16 \[^{2}\] and ResNet50 \[^{70}\] architectures on our selected subset of frameworks. Language modeling is an unsupervised learning task wherein models are trained to predict the next word in a sentence, given all of the previously occurring words. We use the Wikitext-103 \[^{71}\] dataset for our language modeling training workloads. This dataset is comprised of more than 28000 articles from the English Wikipedia amounting to a total of 100 million English words. Language modeling has gained immense popularity recently in NLP for training extremely large neural networks. Researchers have achieved stellar performance with these models in a variety of downstream tasks like question answering, textual entailment, translation, reading comprehension etc. We train two variants of the GPT-2 architecture proposed by OpenAI in their paper \[^{7}\]: GPT2-small and GPT2-medium on the Wikitext-103 \[^{71}\] dataset. Table III provides an overview of the datasets used across our experiments.

| Dataset      | Training Split Size | Validation Split Size | Network       | Mini-Batch Size per GPU | Optimizer†† | Learning Rate | No. of Epochs | L2 Decay         |
|--------------|---------------------|-----------------------|---------------|-------------------------|-------------|---------------|---------------|-----------------|
| ImageNet     | 12,813,167 images   | 50,000 images         | VGG-16        | 64†                     | SGD†        | 0.01†         | 90†           | 0.0001†         |
|              |                     |                       | ResNet50      | 128**                   | LARS*       | 5*            | 90*           | 0.0001*         |
| Wikitext-103 | 103,227,021 words   | 217,646 words         | GPT2-small    | 32**                    | LAMB*       | 0.001*        | 100**         | 0.01*           |
|              |                     |                       | GPT2-medium   | 32**                    | LAMB*       | 0.001*        | 100**         | 0.01*           |

† Values directly taken from torchvision - https://github.com/pytorch/vision/tree/master/references/classification

†† Values defined as unconstrained in MLPerf

† For ZeRO, we use the Adam optimizer with 0.001 learning rate and 0.01 l2 decay as it’s memory optimizations only work with Adam

2) **Hyperparameters:** The epoch execution times and statistical efficiency of a training algorithm are very sensitive to the choice of hyperparameters. Learning rate schedules, optimizer choices and weight decay values can have a large impact on the statistical efficiency. Larger mini-batch sizes reduce epoch execution times at the expense of statistical efficiency.

Hyperparameters were chosen based on corresponding MLPerf \[^{72}\] benchmarks, which are a standard means of comparison for DL training. Because of this we keep the parameters fixed between frameworks. For parameters not included in the MLPerf description we choose them based on the values given in their respective papers. We ensure that training with our hyperparameters gives us reasonable performance on the validation set. Table III provides an overview of the hyperparameters applied to each model. It is possible further tuning could improve the performance and/or statistical efficiencies.

For efficient scaling to larger GPU counts, data parallel algorithms typically use a fixed mini-batch size per GPU to maintain a constant computational workload per GPU. Thus, to ensure a fair comparison of other frameworks with DDP and LBANN we do the following for each framework:

- Megatron - We linearly scale the mini-batch size with increasing number of GPUs.
- TorchGPipe - We fix the size of a micro-batch and set the number of micro-batches to 4 times that of the GPU count.
- PipeDream - We fix the size of a mini-batch. PipeDream ensures constant computational workload on each GPU by increasing it’s pipeline limit automatically.
D. Exceptions

We make the following exceptions to the experimental setups listed above. We only show results for PipeDream on a subset of the GPUs due to the framework deadlocking on higher GPU counts. We could not run PipeDream on ResNet50 as it did not support the batchnorm layer \[73\]. We only show results for TorchGPipe on 1, 2, and 4 GPUs as it is only applicable to a single node. We only show results for LBANN on Lassen as we had difficulties building the framework on both Vulcan and ThetaGPU.

Additional exceptions are made to the experiments conducted specifically on Vulcan due to training time constraint. On Vulcan, VGG-16 and ResNet50 are trained on a 100 class subset of the Imagenet dataset; GPT2-small and GPT-medium are trained on Wikitext-2; all VGG-16 performance runs are conducted on GTX1080Ti’s; ResNet50 and GPT2 performance runs are conducted on Quadro P6000’s. On Vulcan’s 4 GPU performance run of GPT2-medium using DDP, the mini-batch size hyperparameter is reduced to 16 due to out-of-memory errors. Similarly, Vulcan’s 4 GPU performance run of GPT2-small using TorchGPipe has its mini-batch size reduced due to 16 out-of-memory errors. The same mini-batch size adjustment is also made on Lassen for the language models to allow them to fit in memory.

E. Evaluation Metrics

For our analysis, we use metrics that matter the most to a deep learning researcher - epoch execution times, statistical efficiency and GPU memory consumption. Statistically efficient training algorithms or frameworks require less number of epochs to reach a certain target accuracy on the validation data. When comparing parallel DL frameworks, it is absolutely imperative to compare both the epoch execution times and statistical efficiency of the training runs. We have discussed the tradeoffs that parallel DL algorithms incur between these two metrics in Section \[11\].

We profile epoch execution times on 1, 2, 4, 8, 16, 32 and 64 GPUs for Lassen and ThetaGPU. For Vulcan we use 1, 2 and 4 GPUs only as the jobs on that system can only request single node allocations. While profiling the statistical efficiency for a particular framework, we use the GPU count where it has the minimum epoch execution times. For gathering memory utilization data we use 1, 2, 4, 8, 16, 32 and 64 GPUs on ThetaGPU. Table \[III\] and Table \[IV\] gives an overview of the neural networks and machines we used for evaluating these metrics.

To measure the statistical efficiency we record the accuracy and loss for the vision tasks and perplexity for the language tasks. Loss is the output of the loss function used for training. Its magnitude depends on its definition, but the training loss should decrease towards zero as the model improves in predictive capacity. Accuracy measures the ratio of samples accurately predicted to total samples. We use the validation accuracy, which is calculated based on samples exclusive to the training set. Perplexity is commonly used in NLP to measure how well a model predicts for a certain corpus based on the cross-entropy of the model. It is defined as the exponential of the cross entropy loss on the dataset.

V. COMPARATIVE EVALUATION

In this section we present and discuss the results from our experiments on epoch execution times, statistical efficiency, and memory utilization.

A. Execution Time Comparison

Figure 4 presents the sequential single GPU execution times for each framework on the four neural networks on ThetaGPU. PipeDream and TorchGPipe perform worse due to the lack of mixed precision support. The difference is exacerbated for extremely compute intensive neural networks like the GPT2-medium.

![Fig. 4: Comparison of single GPU performance on ThetaGPU for GPT2-medium.](image)

And while Megatron, DDP, and ZeRO employ mixed precision, Megatron is considerably faster as it uses its own optimized implementation of the transformer layer and Adam optimizer. Figure 4 exemplifies this, where we observe a 2x speedup on a single GPU over the native PyTorch kernel used by DDP and ZeRO. The PyTorch implementation performs worse due to its handling of the computationally intensive final softmax layer in GPT2-small and GPT2-medium. DDP’s and ZeRO’s mixed precision strategy computes this layer in full and half precision respectively, thus leading to the difference in performance between the two.

Out of all the frameworks TorchGPipe has the worst single GPU performance. This is because micro-batching provides no performance benefits on a single GPU. In fact it ends up degrading hardware utilization.

Figure 7 shows the time spent by each framework in the forward pass, backward pass and I/O for GPT2-medium on ThetaGPU. We observe a marked improvement in Megatron’s I/O performance. This is because it employs its custom data loaders which are much faster than the native PyTorch data loaders used by other frameworks. Single GPU profiles in the figure also highlight the difference in the computation time of the forward and backward passes for these frameworks. It lends further credence to our aforementioned reasoning for the sequential performance differences.
Fig. 5: Performance results on Lassen for VGG-16 and GPT2-medium.

Fig. 6: Performance results on ThetaGPU for VGG-16 and GPT2-medium.

Fig. 7: Breakdown of time spent in training on 1, 2, 4, and 8 GPUs of ThetaGPU for GPT2-medium. We use NVIDIA’s NVTX SDK for annotating events and Nsight Systems for instrumentation.

Figures 5, 6, and 8 detail the results from the performance tests on each machine. In this subsection we look at some interesting patterns that these experiments uncover and provide an explanation for them. Additionally, based on Figures 4 and 10, we see similar trends between Resnet-50 and VGG-16 in run time performance and likewise for the language models. Therefore, we will use VGG-16 and GPT2-medium to further discuss run time results.

As noted previously in Section III-A2, ZeRO reduces the per GPU memory footprint of data parallelism at the expense of added communication. We notice in Figures 5, 6, and 8 that ZeRO’s performance trends the same as DDP with only 10-15% difference in absolute run time. These variations can be attributed to the different mixed precision implementations and ZeRO’s memory optimizations.

Due to the lack of mixed precision support, PipeDream and TorchGPipe have the largest epoch execution times at all GPU counts across all machines. However, we note that PipeDream seems to scale erratically relative to its own single GPU execution. The poor scaling can be attributed to two factors. Firstly, PipeDream uses the relatively slow Gloo library as its communication backend. Secondly, erratic scaling is usually a sign of load imbalance. Our experiments show that their communication-aware load balancing algorithm doesn’t perform satisfactorily in practice.

While Megatron significantly outperforms the other frameworks for low GPU counts, its performance gradually plateaus out at higher GPU counts. We observed that the communication overhead of Megatron increases rapidly with increasing number of GPUs, ultimately reaching 52.5% of the total execution time on 16 GPUs. Based on our observations, we recommend that researchers who wish to train large transformer models on language modeling task use Megatron for their single GPU sequential implementations. If the model sur-
passes the memory capacity of a single GPU, we recommend employing Megatron’s layer parallelism to fit the model inside the GPUs of a single node. Scaling to large GPU counts should be done by integrating Megatron’s layer parallelism with data parallelism.

It is immediately apparent that the data parallel approaches used in DDP, ZeRO, and LBANN strongly outperform the other frameworks in scaling. This is notably due to the embarrassingly parallel workload in data parallelism when the entire model fits within GPU memory. We also see an expected slight reduction in speedup on Lassen and ThetaGPU (shown in Figure 10) for data parallelism as the number of GPUs surpassed that of a single node. This happens as the all-reduce communication now occurs outside the fast intra-node NVLink and has to use the system network.

B. Statistical Efficiency

Figure 9 illustrates the results of our statistical efficiency experiments. Following standard practice we measure the validation accuracy and perplexity at each epoch for the image classification and language modeling tasks respectively. On observing the performance of PipeDream on both the tasks, it is apparent that weight staleness is a huge roadblock in the path of algorithms that seek to implement pipelining without flushing. PipeDream’s proposed weight stashing approach does not mitigate this problem satisfactorily. ZeRO, DDP and LBANN exhibit near identical validation curves. The slight variations in the validation curves are likely due to differences in the mixed precision implementations in these frameworks. TorchGPipe and Megatron exhibit greater statistical efficiencies than the data parallel frameworks on the language modeling task. We attribute the fast convergence of these frameworks due to their training runs being carried out on a small GPU count. The data parallel frameworks being trained at 64 GPUs take
a slight hit in their convergence speeds due to the problem of increase effective mini-batch sizes that we highlighted in Section III-A3.

Figure 11 further details how the accuracies and perplexities behave over time rather than epoch. PipeDream is much slower to accuracies than the other frameworks. Such a figure presents a combined picture of the statistical efficiency and epoch execution times of a framework. We argue that plotting validation metrics against epoch times is the best way to evaluate the performance of any distributed deep learning framework. It also clearly demonstrates the superiority of data parallelism over other classes of parallel deep learning algorithms.

C. Memory Utilization

Figure 12 details the per GPU memory usage of each framework during the training tasks. ZeRO, while having similar performance and scaling to DDP, had between 42% and 66% of the memory footprint. We also see this improving as more GPUs are added similar to the layer parallel runs, while DDP clearly remains fixed as it simply duplicates the models across GPUs.

The pipelining implementations both experienced over 2x better memory usage with more resources. More of the models were able to be partitioned amongst the GPUs. However, the memory savings begin to plateau as more GPUs are added.

The U-shaped per GPU memory curve of Megatron can be attributed to the inner workings of their intra-layer parallelism implementation. While, the computation of a transformer layer is divided across multiple GPUs, the output of the last layer needs to be present in its entirety on every GPU. Since, the per GPU mini-batch size is fixed, the memory occupied by the input for any layer on each GPU increases linearly with an increase in GPU count. At lower GPU counts, this increase is offset by the decrease in parameter memory due to the division of the layer computation across GPUs. After a while however, the decrease is not enough to completely offset the increasing input activation memory.

VI. Conclusion

The increasing size of contemporary neural network architecture has necessitated the development of efficient algorithms for parallelizing neural networks. The performance of parallel training of neural networks is heavily dependent on the algorithm, implementation, hyperparameters, and hardware used. In this paper, we provide a comprehensive survey of parallel deep learning frameworks that have demonstrated scaling on parallel systems. We use four dataset-network combinations to study various properties of parallel deep learning frameworks such as scalability, memory requirements, and statistical efficiency as a function of performance.

Our benchmarking studies presents some interesting observations. When the entire model can fit within a single GPU, it is best to use data parallel approaches as they perform and scale well. In memory constrained environments, ZeRO can save us a decent amount of memory. Their memory optimizations only add substantial cost to the computation for non-transformer models. For saving more memory, we recommend using intra or inter-layer parallelism to deploy a model across a few number of GPUs and then scale it in a hybrid fashion with data parallelism.
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