A Clock Synchronization Algorithm for the Satellite System Based on MF-TDMA

Min Zhang, Linlin Duan, Kexian Gong*, Xiaoyan Liu and Qian Cheng
Electronics and Communication Engineering, College of Information Engineering, Zhengzhou University, Henan Prov, China

*Corresponding author email: ggkx@163.com

Abstract. In order to ensure microsecond slot scheduling, all terminals must maintain high precision of time synchronization in MF-TDMA(Multi-Frequency Time Division Multiple Access) satellite communication system. Due to the different frequency of crystal oscillator at the terminal, the absolute value of the clock deviation is constantly increasing, so a clock synchronization algorithm is required to keep the time synchronization of the satellite system. The traditional satellite clock synchronization algorithm minimizes the clock error through periodic synchronization, but it only considers the phase offset, not the crystal frequency offset, the synchronization accuracy is low and waste of bandwidth resources. Based on the traditional satellite clock synchronization, this paper proposes a gradient descent algorithm for the satellite system based on MF-TDMA(GDAS), adding clock frequency offset prediction and compensation mechanism to improve clock synchronization accuracy and bandwidth resource utilization rate. The simulation results of the proposed algorithm has optimized the precision performance of clock synchronization.

Keywords: Clock synchronization; Gradient descent; MF-TDMA; GDAS.

1. Introduction
MF-TDMA (Multi-Frequency Time Division Multiple Access) satellite communication system is a new type of broadband VAST network developed on the basis of the TDMA technical system. It is the mainstream system in the current broadband multimedia satellite communication system, and used maturely in the following systems: LinkWay, SkyWan, Hughes, etc[1]. The access method is a combination of FDMA and TDMA, that is, the frequency band of a transponder contains several different carriers, and each carrier works in the way of narrow-band TDMA. Clock synchronization is the key technology of the system satellite communication system which based on MF-TDMA.

In the satellite communication system, each terminal has a timer circuit based on a quartz crystal oscillator. The frequency error and the initial timing time of the crystal oscillator is different, which makes the clocks between the terminals not synchronized. Usually, the frequency of the ordinary crystal oscillator is offset in the range from 20 to 50 ppm[4], and the frequency offset may also be caused by changes of temperature, environment and etc. Usually, the indirect method is used to realize the clock synchronization of the system, that is, using the master station clock as the reference clock, all terminals are synchronized with the reference clock, so that the terminals are synchronized. Literature [1-3] introduce the DVB-RCS standard in detail of satellite interactive applications, explained in detail the clock synchronization technology of the satellite system. The clock synchronization between the terminal and the master station is realized by using the periodic broadcast clock signal, but the frequency offset of the terminal is not considered, the synchronization accuracy is low. In literature [5], it researches the accuracy of clock synchronization and the implementation of the
synchronization redundancy mechanism, and proposes the improvement solutions. Literature [6-7] respectively proposes the use of second-order polynomial, gray system and other models to predict satellite clock errors to improve the accuracy of clock synchronization. In Literature [8] uses the LS(least squares) method to fit polynomials on the basis of the two-way time comparison method to obtain the change curve and value of the clock difference caused by the relative motion of the MEO satellite and the ground, so as to realize the clock synchronization between the satellite and the ground, but its modeling requires a lot of data. When the amount of modeling data is small, the clock synchronization accuracy is affected.

Therefore, this paper proposes a MF-TDMA satellite time synchronization algorithm based on gradient descent (GDAS), which combines traditional clock synchronization algorithms and clock drift prediction and compensation mechanisms to correct phase and frequency offset synchronously, improve time synchronization accuracy.

2. Clock Synchronization Model of MF-TDMA Satellite

Define the local time \( t \) as the actual time, \( f_i(t) \) is the actual oscillation frequency of the clock source at time \( t \), \( f_i(t) \in [f_0 - f_{\text{max}}, f_0 + f_{\text{max}}] \), and \( f_0 \) is the ideal frequency, and \( \pm f_{\text{max}} \) are the upper and lower limits of the frequency offset. The clock dynamic offset is expressed as \( f_i(t) = f_0 + \Delta f(t) \), \( \Delta f(t) \) is the frequency offset, which is the uniform random variable in \( [-f_{\text{max}}, f_{\text{max}}] \), \( d_f \) is the frequency drift, and \( r_f \) is the random error. The definition of \( f_i(t) \) is expressed as the equation (1):

\[
f_i(t) = f_0 + \Delta f + d_f t + r_f(t)
\]  

(1)

Assuming that \( t=0 \) which is the initial reference time, the definition of \( C_i(t) \) is showed as equation (2):

\[
C_i(t) = C_i(0) + \frac{1}{f_0} \int_0^t f_i(t) dt
\]  

(2)

Substituting equation (1) into (2) formula can be obtained:

\[
C_i(t) = C_i(0) + \frac{1}{f_0} \left[ f_0 + \Delta f + d_f t + r_f(t) \right] dt
\]  

(3)

In order to obtain a simple linear model in a non-ideal state, assuming that \( d_f \) doesn’t exist and \( r_f = 0 \), then substituting equation (3) to obtain \( C_i(t) = C_i(0) + \left( \frac{\Delta f}{f_0} \right) t \). Carry out Taylor series expansion on formula (1) to get the local time representation:

\[
C_i(t) = a + bt
\]  

(4)

Where, \( i \) represents the \( i \)-th terminal, \( a \) is the clock offset between the local clock and the actual measured clock, and \( b \) is the clock frequency offset.

3. Traditional Clock Synchronization Principle and Implementation Process

According to the clock model equation (4), all clock deviations of terminals in MF-TDMA satellite communication system have differences in constant terms and clock frequency, that is, phase offset and frequency offset. Traditional time synchronization algorithms mainly use the characteristics of broadcast signals transmitted by wireless signals at the link layer to minimize clock synchronization errors through periodic synchronization.
Based on the EN 301790 standard [1], the reference clock (NCR) is used as the forward link signaling and is transmitted in the MPEG2 transport stream with a special PID. The NCR is derived from the NCC reference clock, which has an accuracy of 5ppm or better. The principle of synchronization between the terminal and the master station is shown in figure 1. The network management system detects the timestamp NCR_r made by the master station, sends the NCR information after coding, and broadcasts it to all terminals through the satellite broadcast channel. The receiving terminal detects the NCR information, extracts the NCR_r from the information and records the time NCR_s of the receiving time, calculates the clock difference \( \Delta t = NCR_r - NCR_s \) and adjusts the terminal clock to obtain synchronization, performs multiple measurements to improve accuracy.

![Figure 1. Synchronization principle between terminal and master station.](image)

The clock between terminals has a phase offset characterized by the difference in time value and a frequency offset characterized by the speed of time due to the characteristics of the crystal oscillator itself [12]. The research on clock synchronization between terminals needs to deal with the relative phase offset and relative frequency offset. If the crystal oscillator frequencies of all terminals are the same, and there is no accumulation of offset over time during use, a single synchronization can completely synchronize the local clock of the terminal. However, in fact, the slight difference in the crystal frequency at the factory, the terminal using a different frequency crystal or the external environment and etc can bring frequency offset. After a period of time, the terminal that has been synchronized with the clock will no longer be synchronized, the influence of the clock crystal frequency deviation is shown in figure 2.

The local clock difference between terminal A and terminal B are \( D_{t_1}^{A \rightarrow B} \) and \( D_{t_2}^{A \rightarrow B} \), which are corresponding to time \( t_1 \) and \( t_2 \) respectively, and \( D_{t_1}^{A \rightarrow B} = D_{t_2}^{A \rightarrow B} + RD_{t_1}^{A \rightarrow B} \), where \( RD_{t_1}^{A \rightarrow B} \) is caused by the difference of crystal vibration frequency from \( t_1 \) to \( t_2 \) of terminal A and terminal B. Therefore, the gradual increase of the clock deviation largely depends on the frequency offset between the clocks.

However, clock frequency offset compensation is not used in the traditional clock synchronization, this paper proposes a GDAS algorithm, which combine the traditional clock synchronization algorithm with the clock offset prediction and compensation mechanism. it improves the accuracy of clock synchronization, and improves the utilization of bandwidth resources while ensuring the accuracy of clock synchronization. It has greater adaptability and is suitable for the satellite communication system of MF-TDMA.
Local time of the terminal

Terminal A

Terminal B

Ideal clock

t_1
t_2

t_{NCC}

Figure 2. The influence of clock crystal deviation.

4. GDAS Algorithm Description

According to formula (2), the logic clock of the terminal $i$ can be expressed as

$$l_i(t) = l_i(t_0) + \hat{\theta}_i \left[ c_i(t) - c_i(t_0) \right]$$

(5)

Where $t_0$ is the initial time, and the frequency factor $\hat{\theta}_i$ is the estimated value of the relative frequency $f_i(t)/f_0$ in $[t_0, t]$. According to the clock model as shown in equation (4), clock synchronization can be regarded as a linear relationship, $l_i(t_0)$ and $\hat{\theta}_i$ are respectively used to adjust the initial clock deviation and relative frequency offset between the terminals and the master station. Therefore, the clock synchronization algorithm is a distributed algorithm for the terminal $i$ to update the logical clock $l_i(t_0)$ and $\hat{\theta}_i$ at the periodic synchronization time.

The master station $m$ transmits the reference broadcast information to the terminals at a period $T$, let $t_n = Tn (n = 0, 1, 2, \cdots)$ and $n$ represents the number of cycles in which the terminal receives the master station broadcast message. The time from the beginning of the transmission of the broadcast message to the terminal receives is called the transmission delay, which is a number of independent random processes. It is modeled as a Gaussian random variable, expressed as $\gamma \sim N\left(0, \sigma_d^2\right)$, where $\gamma_n$ represents the transmission delay, and then the receiving clock of the terminal at cycle $n$ is $l_m(t_n) = Tn + \gamma_n$. During the synchronization period, the error of the terminal relative to the reference clock of the master station can be expressed as

$$e_i(t_n) = l_i(t_n) - l_m(t_n) = l_i(t_n) - Tn - \gamma_n$$

(6)

After the synchronization error is used to compensate the clock offset of the terminal $i$, the logic clock of the terminal $i$ is:

$$l_i(t_n^+) = l_i(t_n) - e_i(t_n)$$

(7)

Where $t_n^+$ represents the time after the terminal $i$ adjusted the clock deviation at $t_n$. From equations (2) and (7), we get the equation (8)

$$e_i(t_{n+1}) = \hat{\theta}_i(t_n) \int_{t_n}^{t_{n+1}} f_i(t) dt - (T + \gamma_{n+1} - \gamma_n)$$

(8)
At the initial time, the synchronization error is \( e_i(t_0) = 0 \), and the relative frequency is \( \hat{\theta}_i(t_0) = 1 \).

The purpose of time synchronization is to minimize the synchronization error, which is the function \( e_i(\theta) \) of dynamic parameters \( \hat{\theta}_i \). It is updated iteratively to find the optimal value \( \hat{\theta}_i^* \) to minimize the synchronization error \( \left( e_i(\theta) \right)^2 \), proceed as follows:

\[
\ell_i(t_n^+) = t_n + \gamma_n \tag{9}
\]

Where \( t_n = Tn \) is the time of each synchronization cycle.

\[
\hat{\theta}_i(t_n^+) = \hat{\theta}_i(t_n) - \alpha \frac{d \left( e_i(t_n) \right)^2}{d \theta_i} \tag{10}
\]

\[
\frac{d \left( e_i(t_n) \right)^2}{d \theta_i} = 2e_i(t_n) \frac{de_i(\hat{\theta}_i)}{d \theta_i} \tag{11}
\]

According to the initial value of \( \hat{\theta}_i(t_n) \), gradient \( \alpha \) and convergence conditions, \( \hat{\theta}_i(t_n^+) \) is the updated value of \( \hat{\theta}_i(t_n) \) after each iteration, and the iteration continues until the difference between \( \hat{\theta}_i(t_n^+) \) and \( \hat{\theta}_i(t_n) \) less than the convergence value. Finally, \( \hat{\theta}_i(t_n) \) will be used as the estimated value of the relative clock frequency offset.

Substitute equations (9) into (11) to get (12)

\[
\frac{d \left( e_i(\hat{\theta}_i) \right)}{d \theta_i} = d \left( \frac{\hat{\theta}_i(t_n^+) f_i(t) dt}{T f_0} \right) = \frac{t_{n+1}^+}{t_n} f_i(t) dt \tag{12}
\]

Find the mean value of equation (12), \( E_{t_n}^{t_{n+1}} f_i(t) dt = T f_0 \), so

\[
\frac{de_i(\hat{\theta}_i)}{d \theta_i} = T f_0 \tag{13}
\]

\[
\frac{d \left( e_i(t_n) \right)^2}{d \theta_i} = 2T f_0 e_i(t_n) \tag{14}
\]

Then rewrite this equation, we get the formula (15).

\[
\hat{\theta}_i(t_n^+) := \hat{\theta}_i(t_n) - 2T f_0 \alpha e_i(t_n) \tag{15}
\]

The terminal \( i \) can correct the relative frequency difference between itself and the master station according to equation (15), and correct its own phase deviation according to the traditional time synchronization algorithm. It is the clock frequency deviation caused by environment, temperature and other factors that makes the time difference between the terminal and the master station larger and larger, the essence of clock synchronization is to correct the frequency offset of the terminal relative to the master.
station clock, that is, the relative frequency offset. Therefore, this improvement has great significance in terms of theoretical analysis and practical application.

5. Simulation and Analysis

5.1. Simulation Environment and Parameters
In order to verify the performance of the algorithm proposed in this paper, the proposed GDAS algorithm, the conventional LS algorithm and the traditional clock synchronization algorithm were carried out a series of simulations on the Matlab7.0 software platform. And the experiments were compared and analyzed the GDAS algorithm and the traditional clock synchronization algorithm, LS algorithm in synchronous precision performance metrics.

The master station is used as a reference, and each terminal in the satellite communication system uses the master station clock as a reference. A random function with a mean value of zero is added to the experiment to simulate the random error of the reference clock generated by the master station. Table 1 shows the simulation parameter values, the following tests are all carried out under this condition.

| Simulation parameter                  | Parameter value |
|--------------------------------------|-----------------|
| crystal oscillator                   | 40MHZ           |
| frequency offset                     | 30ppm           |
| synchronization period               | 600ms           |
| synchronization period number        | 50 rounds       |
| $\delta_d$                           | 50              |
| crystal temperature                  | 45°C            |

5.2. Analysis of Simulation Results
As shown in figure 3, the simulation has produced the clock value of the master station, the clock value of the terminal station and the clock difference between them. The second clock of crystal oscillator suffers from a large cumulative error due to its own frequency fluctuation. The data is based on equations (4) and (6):

![Figure 3. Unsynchronized clock offset curve.](image)

From the simulation results in figure 3, the variation trend of clock error generated by simulation is consistent with equation (4). The clock error between the terminal and the master station is increasing in a linear relationship, it is necessary to adopt a clock synchronization algorithm to synchronize the clocks of the entire network.
Figure 4. Different clock synchronizationalgorithms clock errors performance curve.

Figure 4 shows the performance comparison diagram of clock error between GDAS algorithm and traditional clock synchronization algorithm and LS. According to the simulation results, the clock error is about 18us when the traditional uncompensated clock frequency deviation, the clock synchronization accuracy is obviously improved after using the algorithm LS and GDAS, which can reach the ns level. This is because there is a clock frequency deviation, and the clock deviation between terminals will continue to increase over time.

The GDAS algorithm and the LS algorithm consider the clock frequency offset of the terminal, which effectively reduces the impact of the clock frequency offset. The window length is N1, which is the amount of data during modeling. The synchronization accuracy of the LS algorithm is affected by the amount of modeling data. From the figure 4, it can be seen that when the window length is N1=8, the synchronization accuracy of the GDAS algorithm is obviously improved, and the stability is enhanced.

Table 2. Different clock synchronizationalgorithms clock errors performance.

| Clock synchronization algorithm | Maximum clock error | Mean of clock error |
|---------------------------------|---------------------|---------------------|
| Traditional clock synchronization algorithm | 18.141 $\mu$s | 18.073 $\mu$s |
| LS algorithm | 110.875 ns | 66.280 ns |
| GDAS algorithm | 35.304 ns | 16.316 ns |

Table 2 shows the synchronization accuracy of different clock synchronization algorithms more intuitively, the maximum deviation is reduced from the LS algorithm 110.875ns to the current 35.304ns, and the average deviation is also reduced from 66.280ns to 16.316ns.

6. Conclusion

Based on the traditional clock synchronization, this paper proposes GDAS algorithm to synchronize the clock frequency and phase offsets of terminals. Combining the traditional clock synchronization algorithm with the gradient descent method, the clock offset of the terminal is corrected from two aspects: phase offset and frequency offset, which improves synchronization accuracy and improve resource utilization. Experimental results show that compared with traditional clock synchronization algorithms and LS synchronization algorithms, the GDAS algorithm can effectively improve synchronization accuracy and ensure the long-term effectiveness of synchronization.

Acknowledgments

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