Direct Heteroepitaxy and Selective Area Growth of GaP and GaAs on Si by Hydride Vapor Phase Epitaxy

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Direct heteroepitaxy and selective area growth (SAG) of GaP and GaAs on Si(110) and Si(111) are implemented by low-pressure hydride vapor phase epitaxy (LP-HVPE), which are facilitated by buffer layers grown at 410–490 °C with reactive gas mixing directly above Si substrates. High-density islands observed on GaP buffer layers on Si result in rough morphology and defect formation in the subsequent GaP layers grown at 715 °C. The impact of growth temperature of GaAs buffer layers on the crystal quality of GaAs/Si is studied. A decreased nucleation temperature significantly improves the morphology and crystalline quality of the overall GaAs growth on Si. It is observed that Si(111) substrates are favorable for both GaP and GaAs growths in comparison with Si(100). In SAGs of GaP/Si and GaAs/Si, the high selectivity innate to HVPE is maintained in the used unconventional growth regime. The spatially resolved photoluminescence mapping reveals the material quality of GaAs/Si is enhanced by defect filtering by SAG. The outcomes of this work will pave the way of III–V/Si integration realized by cost-effective HVPE for photonic device applications.

1. Introduction

The integration of III–V semiconductors on Si is promising for utilizing the superior optical and electronic properties of III–Vs while benefitting from the process maturity and cost effectiveness of Si-processing technology. Methods for integrating III–V semiconductors on Si are extensively researched and steady progress is being made.[1–3] Direct heteroepitaxy is a commonly used approach, where the main difficulties stem from the thermal and lattice mismatch between most of the III–V materials and Si. Numerous methods for overcoming these difficulties have been developed for achieving high-quality III–V films on Si using metal–organic vapor phase epitaxy (MOVPE) and molecular beam epitaxy (MBE).[4,5] Hydride vapor phase epitaxy (HVPE) is an economically viable technique for III–V/Si integration thanks to the comparatively low cost of its precursors compared with other epitaxial methods.[6] This is of particular importance for photovoltaics applications due to its sensitivity to fabrication costs because of the need for a market-competitive levelized cost of energy (LCOE). While direct heteroepitaxy of III–V on Si by HVPE poses additional challenges compared with other techniques, promising results have been reported by other groups utilizing a variation of HVPE called vapor mixing epitaxy (VME).[7–9] in which nucleation on Si is achieved through a low-temperature buffer layer followed by a second growth step at a higher temperature. These results indicate the feasibility of using this approach to exploit the beneficial properties of HVPE, including high growth rates and cheap precursors, while bypassing one of the major drawbacks of its near-equilibrium nature by allowing nucleation on Si. However, while some investigation of the properties and impact of the low-temperature buffer layer used for achieving nucleation during HVPE has been done,[10] more extensive studies are needed. Low-pressure HVPE is known to have several benefits compared with that at atmospheric pressure, including a higher growth rate,[31] improved uniformity,[12,13] and lower precursor flows required to maintain a high gas-velocity which increases the growth efficiency.[14] Several authors have studied the initial stages of growth during heteroepitaxy of III–V materials on Si substrates and their importance for the quality of the subsequent growth, both for two-step growths as described earlier and for growths made in a single step.[15,16] Applying this understanding to HVPE is crucial to achieve high-quality epitaxial growth on Si at the low cost afforded by the technique. One common approach for improving the material quality of the epitaxial III–V films on Si is using selective area growth (SAG), for which HVPE is uniquely suited because of its inherent selectivity and high growth rate.[17] SAG on complementary metal–oxide–semiconductor compatible Si(100) substrates is useful for reducing the impact of the lattice mismatch between Si and most of the III–V materials by defect filtering,[18] as well as for restricting the deposition to active regions on the Si substrate and preventing the formation of antiphase domains (APDs).[19] SAG on Si(111) substrates is useful for the precise control of the position and size of III–V/Si nanowire growth, and it has been suggested that using low-temperature buffer layers during SAG of nanowires on Si
would reduce the amount of unintentional doping from the Si substrate present during both high temperature SAG and vapor-liquid–solid method.[29] It is worth mentioning that HVPE has been investigated for nanowire growth previously.[21,22] SAG is also an important technique used for the growth of high crystalline quality GaN in the fashions of epitaxial lateral overgrowth (ELOG) and Pendeco-epitaxy.[23,24] Enabling SAG by HVPE on Si substrates without the need for other epitaxial techniques to grow the otherwise required nucleation layers would greatly increase the economic benefits of using HVPE for III–V/Si integration. Proper understanding and development of this technique will serve as a platform for cost-effective integration of III–V materials on Si for photonic devices.

This work investigates the growth of GaAs and GaP on both Si(100) and Si(111) utilizing the VME approach. Planar substrates are used to study the impact of the initial nucleation conditions and properties on the overall growth, and investigate the impact of Si (100) and (111) orientations on the crystalline quality of the III–V heteroepitaxial layers. Growth of GaP buffer layers is carried out and compared with GaP grown by the two-step process by characterizing the morphology and crystalline quality of the growths. GaAs is grown by the two-step process using different growth temperatures for the buffer layer to study the impact of the nucleation temperature on morphology and crystalline quality. SAG of GaP and GaAs is carried out on patterned Si(100) and (111) substrates to study the selectivity of HVPE in the unconventional growth regime used by VME and the beneficial effects of SAG for defect reduction in heteroepitaxy of III–V semiconductors on Si.

2. Experimental Section

In this work, on-axis Si(100) and Si(111) substrates were used for GaAs and GaP direct heteroepitaxy. SAG templates were also used, consisting of Si(100) and Si(111) substrates capped by a 400 nm dielectric mask with circular openings of 2–4 μm diameter. The low-temperature buffer layers and subsequent layers were grown in a horizontal commercial Aixtron low pressure HVPE reactor at 20 mbar with N₂ carrier gas. The reactor utilizes five separate heated zones, including a source, precursor mixing, and growth zone. The total flow of precursor and carrier gases was chosen to maintain a gas velocity of 5 cm s⁻¹ over the substrate. GaCl was used as the group III precursor, and AsH₃ and PH₃ were used as the group V precursors. GaCl was formed by flowing gaseous HCl over a quartz boat containing liquid gallium in a separately heated zone kept at 740 °C, which leads to an almost 100% efficient reaction between HCl and Ga. For the growth of the III–V layers at higher temperature, the precursors were mixed in a separately heated mixing zone kept at over 700 °C before reaching the growth zone with the substrates. For the low-temperature buffer layer growths, the V-element precursors were introduced through a different line located close to the substrates such that the precursors are not mixed before they reach the surface of Si substrates. This differs from how the VME experiments by Mori et al. were carried out, as the group V precursors were delivered from the cold side of the reactor and allowed to react with the GaCl without pyrolyzing. After growing the low temperature (LT) buffer layer, the growth was interrupted by removing the III-element precursor and keeping the substrates in an ambient of the V-element precursors to prevent thermal decomposition. The growth zone temperature was then increased to 660–710 °C for the subsequent layer growth. A total of six experiments were carried out (A–F) with multiple substrates grown in each experiment, where all but one (growth A) utilized the two-step growth method outlined earlier. Multiple, rectangular substrates were used in each growth, with areas of 1 cm² or larger. In growth A, a low-temperature GaP buffer layer was grown without a subsequent top-layer. After this growth, the samples in growth A were heated to 710 °C in a PH₃ ambient, effectively annealing the samples at this temperature for 3 min. This was done to mimic the conditions used for the two-step growth of GaP, ensuring that the buffer layer grown in A is as close to the ones used for subsequent top layer growth as possible. A two-step GaP growth was carried out in growth B, using the parameters from growth A for the LT buffer layer. GaAs was grown in runs C and D using the parameters except a slightly higher temperature for the buffer layer growth in run D. The choice of parameters used for growing the top layers was based on previously optimized homoepitaxy runs. The growth parameters used for each growth are shown in Table 1. GaP low-temperature buffer layers and subsequent top layers are denoted as GaP(1) and GaP(2), respectively, with GaAs layers following the same notation.

The morphology of the grown layers was characterized by Nomarski microscopy, scanning electron microscopy (SEM) and atomic force microscopy (AFM). Room temperature photoluminescence (PL), and Raman spectroscopy, both single scans and area mapping, as well as high-resolution X-ray diffraction (HRXRD) were used to characterize strain and crystalline quality of the grown layers. The PL and Raman scans were conducted with a 514 nm Ar⁺ laser and the mappings were carried out with 0.5 μm steps. The frequency resolution of the Raman scans was 0.6 cm⁻¹. Growthths B, C, and D included planar semi-insulating (SI) GaP and GaAs reference samples (Table 1), which were used to characterize the electrical properties of the grown material by Hall effect measurement. The layer thicknesses and growth rates were measured directly by cross-sectional SEM. While some of the growths were not entirely uniform, all characterization was carried out such that the results presented are representative of each overall growth.

3. Results and Analysis

It is challenging to achieve sufficient nucleation of III–V semiconductors on Si in the typically used growth regimes by HVPE due to its near-equilibrium nature. One way to overcome this is to perform the III–V semiconductor growth at a lower temperature, increasing the supersaturation far enough for nucleation on the Si substrate to occur. There is a problem with this approach, however, namely the occurrence of parasitic nucleation on the reactor walls which is a well-known and often addressed problem during HVPE, even at higher temperatures.[27] At the low temperatures required to achieve nucleation on Si, the excess nucleation on the reactor walls would be severe enough so that no precursors would reach the substrate, making growth impossible.[7] By mixing the precursors close to the substrate as per VME, the growth temperature can be kept low enough to readily
promote nucleation of III–V semiconductors on Si while preventing the consumption of precursors by parasitic nucleation on the reactor walls. At low growth temperature, the mobility of gas species on the substrate surface could be reduced and somehow move the process away from equilibrium, which may affect the nucleation and growth on Si surface. Such effect needs to be further investigated in the future. This low-temperature nucleation layer serves as a buffer for the consecutive III–V layer growth at higher temperatures.

3.1. Heteroepitaxy of GaP/Si

GaP buffer layers were grown on Si(100) and Si(111) substrates with an approximate rate of 40 nm min$^{-1}$. AFM and Raman scans were conducted to investigate the morphology and crystalline quality of the grown layers, with results shown in Figure 1. A homoepitaxially grown GaP(100) reference sample is included in the Raman scans (Figure 1d).

The AFM scans of sample A1 GaP/Si(100) and A2 GaP/Si(111) (Figure 1a,b) show the morphology of the GaP buffer layers grown at 410 °C. The resulting morphology on A1 and A2 are similar, but with larger features present on sample A2. The RMS roughness of the GaP buffer layer surfaces are 4 and 7 nm for 0.5 × 0.5 μm$^2$ scans on samples A1 and A2, respectively. As indicated by the AFM profiles (Figure 1c), the islands present on the GaP/Si(111) sample A2 generally have higher aspect ratio than the ones on the GaP/Si(100) sample A1. Both TO$_{GaP}$ and LO$_{GaP}$ phonon modes are observed in the Raman spectra of the GaP buffer layers, indicating the crystalline quality of the grown material. The prominent forbidden TO$_{GaP}$ peak visible in the spectrum of GaP/Si(100) sample A1 which is not present on the GaP(100) reference sample (Figure 1d) could be due to the morphology with high-density islands shown in the AFM scan (Figure 1a). No discernable crystalline planes are observed on the islands, as they appear rounded in the AFM profiles (Figure 1c). It is possible that the islands initially exhibit planes during the early stage of growth, as reported for growth of GaP on Si by MBE.$^{[16]}$

GaP/Si(100) sample B1 and GaP/Si(111) sample B2 prepared by two-step growth are characterized by SEM, AFM, and HRXRD omega-2theta scans, as shown in Figure 2. The crystalline quality of the GaP/Si layers is characterized by HRXRD omega scans, with full width at half maximum (FWHM) values shown in Table 2, which also shows the FWHM values for the GaAs/Si samples from growths C and D, as well as the Hall mobilities and carrier concentrations of the reference samples from growths B to D. The film thickness and growth rate for each growth on planar Si substrate are also presented.

The two-step GaP growth resulted in a rough morphology for both sample B1 on Si (100) and B2 on Si (111), as seen in the SEM and AFM images (Figure 2a–d). The irregularly shaped plateaus seen in SEM and AFM of the GaP/Si(100) sample B1 could be APDs, although they are larger than what is usually reported for direct epitaxy of GaP on Si.$^{[28–30]}$ Note that the presented AFM scans of the two-step GaP/Si samples are of different sizes, with a 20 × 20 μm$^2$ scan for GaP/Si(100) sample B1 and a 50 × 50 μm$^2$ scan for GaP/Si(111) sample B2. APDs, being charged defects, are detrimental to device performance and their density could be reduced through the use of offcut Si(100) substrates.$^{[12]}$ As shown in Figure 2e,f, the mismatch estimated by HRXRD omega-2theta scans are 0.27% and 0.28% for GaP/Si(100) sample B1 and GaP/Si(111) sample B2, respectively. These values are both lower than the lattice mismatch of 0.36% between unstrained GaP and Si. This discrepancy most likely stems from the mismatch of the thermal expansion coefficients between GaP and Si, resulting in tensile strain as the samples cool down after growth. The tensile strain will reduce the lattice constant along the growth direction and cause the reduction of Bragg angle separation seen in the HRXRD omega-2theta scans of GaP/Si (100) and GaP/Si (111). The crystalline quality of the GaP layers is evaluated by the FWHM of HRXRD omega-scans, which is 913 arcsec for GaP/Si(100) sample B1 and 419 arcsec for GaP/Si(111) sample B2, respectively (Table 2). These are significantly higher compared with previously reported direct heteroepitaxy of GaP on Si by VME, where a FWHM value of 93 arcsec was achieved on Si(100) substrates with 2° offcut toward [110].$^{[7]}$

Table 1. Growth parameters used for each sample.

| Sample | Substrates | Layer(s) | GaCl [sccm] | PH$_3$ [sccm] | AsH$_3$ [sccm] | T [°C] | Time [min] |
|--------|------------|----------|-------------|--------------|--------------|--------|------------|
| A1     | Si(100)    | GaP(1)   | 5           | 50           | 0            | 410-470| 2          |
| A2     | Si(111)    |          |             |              |              |        |            |
| B1     | Si(100)    | GaP(1)   | 5           | 50           | 0            | 410-470| 2          |
| B2     | Si(111)    | GaP(2)   | 5           | 100          | 0            | 715    | 15         |
| B3     | Si GaP     |          |             |              |              |        |            |
| C1     | Si(100)    | GaAs(1)  | 5           | 0            | 50           | 410-470| 2          |
| C2     | Si(111)    | GaAs(2)  | 5           | 0            | 100          | 660    | 15         |
| C3     | Si GaAs    |          |             |              |              |        |            |
| D1     | Si(100)    | GaAs(1)  | 5           | 0            | 50           | 440-490| 2          |
| D2     | Si GaAs    | GaAs(2)  | 5           | 0            | 100          | 660    | 15         |
| E1     | Patterned Si(100) | GaP(1) | 5           | 50           | 0            | 410-470| 2          |
| E2     | Patterned Si(111) | GaP(2) | 5           | 100          | 0            | 715    | 15         |
| F1     | Patterned Si(100) | GaAs(1) | 5           | 0            | 50           | 410-470| 2          |
| F2     | Patterned Si(111) | GaAs(2) | 5           | 0            | 100          | 660    | 15         |
indicating that some optimization of the growth parameters is needed. Contemporary direct epitaxial growth of GaP on Si by MBE and MOCVD routinely achieves substrate quality omega-scan FWHM values of the grown GaP layers (below 40 arcsec) for growth kept below the critical thickness.\[31–33\]

The GaP buffer layer growths on both Si (100) and (111) substrates appear to grow in separate 3D islands as opposed to the more favorable 2D Frank–Van der Merve growth mode. It has been suggested that growth of III–V materials on Si is of the Volmer–Weber mode due to incomplete surface wetting based on surface energy arguments, including for the quasilattice matched case of GaP on Si.\[16\] Furthermore, the precise conditions during the initial nucleation are important for the subsequent crystalline quality. Temperature has a large impact on this, as it influences the size of the initial 3D islands on the Si substrate and consequently how they coalesce into a continuous layer.\[34,35\] At lower temperatures, the critical size of the nucleus is reduced leading to a higher density of nuclei. Biegelsen et al. report that this, during MBE of GaAs on Si, results in a smoother morphology but higher defect density and suggest that this is caused by the generation of stacking faults during the coalescence of nuclei.\[35\] If a similar mechanism exists for HVPE growth, the growth temperature plays an important role in determining the surface topography of the low-temperature buffer layers. One possible way to improve the buffer layer growth could be to reduce the temperature to improve the morphology while compensating for the additional defect generation by annealing before the growth of the top layer. In fact, it has been described that the defects formed by coalescence of smaller islands are more mobile and are therefore more readily removed by annealing compared with defects that are allowed to form before the islands coalesce.\[36\] This would reduce the density of defect in the subsequently grown top layer, providing a possible way to reduce the high FWHM values obtained for the GaP/Si two-step growth (Table 2). Mori et al. have reported an improvement in crystalline quality of InP grown on Si by VME using a thermal cycle annealing and regrowth scheme.\[37\] The defect density reduction could also serve to reduce the mosaicity currently present in the buffer layer as indicated by the forbidden TO_{GaP} phonon peak in the Raman scan of the GaP/Si(100) buffer layer sample (Figure 1c).

The difference in morphology between samples A1 and A2 seen in AFM (Figure 1a,b), as well as the significantly lower crystalline quality of sample B1 compared with B2, as seen in the omega scan FWHM values (Table 2), could be explained by the different surface and interface energies associated with the GaP/Si(100) and GaP/Si(111) systems, which influence the surface wetting conditions.\[16\] Narayanan et al. have studied the initial stages of GaP growth on Si by pulsed chemical beam epitaxy, investigating the dependence of initial island nucleation and consequent defect formation on Si substrate orientation.\[38,39\] They report that the substrate orientation affects the shapes of the 3D islands that form in the initial stages of GaP growth on Si, including which facets that emerge.\[38\] This is a
of the different atomic structures and dangling bond density of the Si surfaces and in turn leads to differences in the amount and type of defects that form upon coalescence of the islands. The differences between the initial nucleation

Figure 2. Top-view SEM images showing a) GaP/Si(100) sample B1 and b) GaP/Si(111) sample B2; AFM scans of c) a 20 \( \mu \)m square on GaP/Si(100) sample B1 and d) a 50 \( \mu \)m square on GaP/Si(111) sample B2; HRXRD omega-2theta scans of e) the (004) reflection from the GaP/Si(100) sample and f) the (333) reflection from the GaP/Si(111) sample, indicating the nominal layer peak position and mismatch for a fully relaxed film and the mismatch for each peak.

Table 2. HRXRD omega-scan FWHM values, Hall measurement results, film thickness, and planar growth rate.

| Sample       | \( \omega \)-scan FWHM [arcsec] | Hall mobility [cm\(^2\)V\(^{-1}\)s\(^{-1}\)] | Carrier concentration \( [10^{16} \text{ cm}^{-3}] \) | Thickness [nm] | Growth rate [nm/min] |
|--------------|---------------------------------|---------------------------------|---------------------------------|----------------|---------------------|
| A1 GaP/Si(100) | –                                | –                               | –                               | 80             | 40                  |
| A2 GaP/Si(111) | –                                | –                               | –                               | 120            | 60                  |
| B1 GaP/Si(100) | 913                              | –                               | –                               | 4500           | 300                 |
| B2 GaP/Si(111) | 419                              | –                               | –                               | 3200           | 210                 |
| C1 GaAs/Si(100) | 659                              | –                               | –                               | 1000           | 70                  |
| C2 GaAs/Si(111) | 262                              | –                               | –                               | 750            | 50                  |
| D1 GaAs/Si(100) | 720                              | –                               | –                               | 1400           | 90                  |
| B3 GaP SI ref. | –                                | 34                              | 3.70                            | –              | –                   |
| C3 GaAs SI ref. | –                                | 1306                            | 29.91                           | –              | –                   |
| D2 GaAs SI ref. | –                                | 3507                            | 1.18                            | –              | –                   |
on different Si surfaces is attributed to the density of shallowly inclined, P-terminated facets. In the case of the chemical beam epitaxy reported in the study by Narayanan et al., growth of GaP on Si(111) was found to generate a higher density of planar defects, including stacking faults and microtwins, in the early stages of growth. This was caused by a higher density of P-terminated {111} surfaces present on the initially nucleated GaP islands for Si(111) compared to Si(100). However, the initial nucleation of GaP on Si(100) compared with Si(111) during VME could result in different densities of P-terminated facets emerging on the islands compared with that of chemical beam epitaxy. As such, a study of the initial stages of VME growth is required to fully explain the difference in both morphology and defect density between GaP grown on Si(100) and Si(111).

The Hall measurement results for the reference GaP/Si-GaP sample (B3) are shown in Table 2. Sample B3 has a Hall mobility of 34 cm² V⁻¹ s⁻¹ and a carrier concentration of 3.7 × 10¹⁶ cm⁻³. GaP with this carrier concentration is expected to have a Hall mobility of ≈150 cm² V⁻¹ s⁻¹. The addition of a low-temperature buffer layer appears to have a detrimental effect on the electronic properties of homoepitaxially grown GaP, in particular the Hall mobility. Further investigation is needed to determine the reason for this detrimental effect, and to what extent it impacts the electrical properties of homoepitaxially grown GaP on Si. The decrease in carrier mobility could be due to enhanced structural defects in the homoepitaxially grown GaP layer, originating from the buffer layer. The introduction of a low-temperature buffer layer might promote the formation of hillocks during the GaP growth, increasing their density. High hillock densities during homoepitaxial growth of GaP when on-axis GaP substrates are used have been attributed to the nucleation of hillocks from Ga droplets at the gas–liquid interface. The LT used during VME could result in a higher density of Ga droplets available for hillock nucleation, leading to a higher hillock density and lower Hall mobility.

3.2. Heteroepitaxy of GaAs/Si

The morphology of the GaAs/Si samples prepared by two-step growth is investigated by SEM and AFM, as shown in Figure 3.

The morphology of GaAs/Si(100) sample C1 has a few different features, each indicated in the SEM image (Figure 3a,b), namely plateau-like structures marked by a dotted line, small rectangular regions marked by arrows, and curved, thin lines marked with a dashed circle in Figure 3b. The plateaus, similar to GaP/Si(100) sample B1 (Figure 2a,c), are most likely APD. The AFM scans on GaAs/Si(100) sample C1 (Figure 3c,d) reveal the thin, curved lines to be steps with heights ranging from 2 to 8 nm. Similar curved lines have been reported as GaAs surface macrosteps. The rectangular features marked by arrows in the SEM image (Figure 3b), also seen in the high-resolution AFM scan (Figure 3d), could be associated with planar defects such as stacking faults or threading dislocations terminating at the GaAs surface. Moreover, they are aligned along both [110] and [−110] directions. Based on the close-up SEM image, the rectangular features have a density of 2 × 10⁶ cm⁻².

The GaAs/Si(111) sample C2 has a smoother surface compared with that of GaAs/Si(100) sample C1 with a high density of pits (Figure 3e,f). Growth of GaAs on Si(111) has been reported previously to result in a smoother morphology than that on Si(100), which was attributed to a greater tendency for layer-by-layer growth on Si(111). This is a result of prolonged island formation during the initial stages of growth due to the greater interface energy of GaAs/Si(111) compared with GaAs/Si(100). The lower growth rate for sample C2 (50 nm min⁻¹) compared with those of C1 and D1 (70 and 90 nm min⁻¹, respectively) can also be explained by this reasoning, as layer-by-layer growth is generally slower than island-like growth. The AFM scan (Figure 3f) reveals the pits on GaAs/Si(111) sample C2 to be up to 150 nm deep with a density of 9 × 10⁶ cm⁻². The fact that similar pits do not develop on the GaP/Si(111) sample B2 indicates that they stem from the lattice mismatch between GaAs and Si. Pits have been reported to arise from threading dislocations in heteroepitaxial layers, but a more detailed study is required to properly investigate the mechanisms behind the formation of these pits. Another important difference between sample C1 and C2 is the absence of APDs on sample C2, which is expected as the Si(111) surface has monoatomic steps which prevents their formation and leads to a smoother morphology compared with growth on Si(100). As such, the overall superior morphology of GaAs grown on Si(111) compared with Si(100) appears to mainly be the result of their different surface atomic structures, promoting layer by layer growth and preventing the formation of APDs.

The topography of the GaAs/Si(100) samples of growths C1 with buffer layer grown at 410 °C and D1 with buffer layer grown at 440 °C differ significantly, as seen in the SEM images (Figure 3a,d) and AFM images (Figure 3e,f,h,i), despite using almost identical growth conditions. An important difference is the absence of curved lines on D1 as well as generally larger aspect ratio (Figure 3h,i). One possible explanation is that the higher temperature for the buffer layer in sample D1 results in larger islands coalescing, leading to island-like growth for the consecutive top GaAs layer. Similar to the difference between the GaAs/Si(100) sample C1 and GaAs/Si(111) sample C2, this results in a slightly smoother morphology for sample C1 compared with D1.

HRXRD omega-2theta scans and PL measurements were carried out on GaAs layers grown on planar Si substrates from growths C and D to evaluate the as-grown crystalline quality, as shown in Figure 4. A PL scan was also carried out on a homoepitaxially grown GaAs/GaAs sample for reference.

The lower growth temperature used for the GaAs buffer layer in GaAs/Si(100) sample C1 (417–473 °C) compared with GaAs/Si(100) sample D1 (439–490 °C) resulted in a reduction of the HRXRD omega-scan FWHM from 720 to 659 arcsec (Table 2). As the same growth conditions are used for the top layers in growths C and D, this indicates that a lower buffer layer growth temperature is beneficial for the crystalline quality of GaAs grown on Si(100) by VME. It should be noted that the lower thickness of sample C1 compared with D1, as shown in Table 2 (1000 nm compared with 1400 nm) is expected to increase the omega-scan FWHM value of sample C1 compared with D1 as fewer threading dislocations are allowed to annihilate. As mentioned earlier, the buffer layer growth temperature is
expected to influence the growth significantly, both in resulting morphology and in defect formation. While the lower temperature is reported to lead to higher defect densities, this effect might have been compensated by the increase in temperature before the start of the top-layer growth, annealing out some of the formed defects. This is consistent with the description of how defects formed at lower nucleation temperatures are more mobile and easier to anneal out.

The HRXRD omega-2theta scans of GaAs/Si(100) samples C1 and D1 (Figure 4a) indicate that they both have some amount of residual thermal strain, as the measured mismatches of C1 and D1 (3.86% and 3.78%, respectively) are both smaller than the lattice mismatch of unstrained GaAs and Si (3.93%). The fact that the measured mismatches are also similar suggests that the growth temperature of the buffer layer does not influence relaxation of the grown layer during cooling. However, a more thorough investigation of buffer layer growth temperatures is required to fully determine its impact on the overall layer quality and growth. Direct heteroepitaxy of GaAs on epitaxial silicon surface (ESS) substrates by VME has been reported to reach omega-scan FWHM values as low as 220 arcsec after annealing at 800 °C, showing that further optimization of the GaAs growth parameters presented in this work is needed.

The comparatively high crystalline quality of GaAs/Si(111) sample C2 indicated by the low omega scan FWHM (262 arcsec) compared with that of GaAs/Si(100) samples C1 and D1 (659 and 720 arcsec) indicates that growing on Si(111) is favorable compared with growing on Si(100). This could be explained by the Si(111) substrate promoting layer-by-layer growth. Similar to the comparison of omega-scan FWHM values between GaAs/Si(100) samples C1 and D1, the FWHM value for GaAs/Si(111) sample C2 is lower than those for samples C1 and D1 despite sample C2 having a significantly lower thickness of 750 nm. This further demonstrates the benefits of growing on Si(111) compared to Si(100). For comparison, an omega-scan FWHM value of 165 arcsec has been reported for a GaAs/Si(111) film grown by MBE. Also worth noting is that the omega-scan FWHM of 262 arcsec for sample C2 is significantly lower than the values reported for VME growth on Si(100).
lower than the value of 419 arcsec for GaP/Si(111) sample B2, despite the significantly lower lattice mismatch and greater layer thickness of the latter.

The HRXRD omega–2theta scan of GaAs/Si(111) sample C2, in contrast to GaAs/Si(100) samples C1 and D1, measures a mismatch that is larger than the unstrained lattice mismatch of GaAs and Si, at 4.17% compared with 3.93% (Figure 4b). As such, sample C2 shows signs of an overall compressive strain, despite also being expected to display signs of tensile strain generated while cooling down after growth due to thermal mismatch. There appears to be some mechanism that compensates the tensile strain, the identification of which requires a more thorough investigation. Residual compressive strain attributed to lattice mismatch has been reported for GaAs/Si layers up to 2 μm thick, despite surpassing the critical thickness.[46]

The PL scans of GaAs/Si(100) samples C1 and D1 as well as GaAs/Si(111) sample C2 all show red-shifts compared with the reference GaAs sample with an emission wavelength of 871 nm. Such red shift in emission is indicative of tensile strain, stemming from the thermal mismatch between the GaAs layers and Si substrates during cooling.[47] The red shift seen in the PL emission seen for GaAs/Si(111) sample C2 (Figure 4c) appears to contradict the presence of residual compressive strain indicated by the HRXRD omega-2theta scan (Figure 4b). This could be due to the greater penetration depth associated with HRXRD compared with PL, indicating an increase in residual thermal strain further away from the GaAs/Si interface. The higher FWHM of 28 nm for both C1 and C2 along with the 29 nm for sample D1 compared with the FWHM value for the reference GaAs sample of 17 nm indicates a lower crystalline quality of the samples grown on Si.

The Hall measurements (Table 2) reveal that the mobility and carrier concentration of Si–GaAs reference sample C3 (1306 cm² V⁻¹ s⁻¹ and 29.91 × 10¹⁶ cm⁻³) is inferior to those of Si-GaAs reference sample D2 (3507 cm² V⁻¹ s⁻¹ and 1.18 × 10¹⁶ cm⁻³). This indicates that a lower nucleation temperature deteriorates the electrical properties homoepitaxial GaAs growth. In HVPE of GaAs, a high carrier concentration and subsequent low Hall mobility is usually due to unintentional doping with Si from the quartz walls of the reactor. The lower nucleation temperature seems to promote the incorporation of Si into the GaAs buffer layer.

The average thickness and growth rates for the GaP and GaAs samples grown on planar Si substrates are estimated by cross-sectional SEM and shown in Table 2. The growth rates of GaP/Si(100) sample A1 and GaP/Si(111) sample A2 are 40 and 60 nm min⁻¹, respectively, which are comparable to the 50 nm min⁻¹ that has been reported for VME-grown GaP at ≈400 °C.[7] The GaP growth rate for sample B1 on Si(100) is 300 nm min⁻¹ with an omega-scan FWHM of 913 arcsec, which
is higher than that of 210 nm min\(^{-1}\) on the Si(111) substrate with an omega-scan FWHM of 419 arcsec. Similar dependence of growth rate and crystalline quality on Si substrate orientation is observed on GaAs/Si(100) sample C1 (70 nm min\(^{-1}\), omega-scan FWHM of 659 arcsec) and GaAs/Si(111) sample C2 (50 nm min\(^{-1}\), omega-scan FWHM of 262 arcsec), respectively. The higher buffer layer growth temperature used for GaAs/Si(100) sample D1 compared with GaAs/Si(100) sample C1 resulted in an increase in growth rate from 70 to 90 nm min\(^{-1}\), along with a rougher morphology seen in AFM (Figure 3d,i) and an increase in omega-scan FWHM from 659 to 720 arcsec (Table 2). Such correlation between the growth rate and crystalline quality of GaP/Si and GaAs/Si could be explained by the enhanced growth rate due to higher dislocation density as predicted by the Burton– Cabrera–Frank (BCF) model.\(^{[48]}\) The growth rate is also expected to vary with the grown thickness as more and more precursors get depleted over time due to parasitic nucleation on the reactor walls, although for the short growths reported here this effect is not expected to be significant as these effects are typically observed for longer growths.\(^{[49]}\) Comparing the GaP/Si growths with the GaAs/Si growths, one unexpected difference is the consistently higher crystalline quality achieved for GaAs compared with GaP when the same substrate is used. Considering the higher lattice mismatch between GaAs and Si (3.93%) compared with the one between GaP and Si (0.36%), a significantly broader omega scan peak for the GaAs/Si case is expected due to the greater misfit strain causing an increased threading dislocation density. However, lower omega scan FWHM values (Table 2) for GaAs/Si(100) samples C1 and D1 (FWHM of 659 and 720 arcsec) are obtained as compared with GaP/Si(100) sample B1 (FWHM of 913 arcsec) as well as when comparing GaAs/Si(111) sample C2 (FWHM of 262 arcsec) to GaP/Si(111) sample B2 (FWHM of 419 arcsec). One possible explanation for the improved crystalline quality of the GaAs layer grown on Si is the fact that the Si substrate was preheated in an AsH\(_3\) ambient; this has been shown to improve the quality of heteroepitaxial growth on Si, including when used for GaP growth.\(^{[49,50]}\) This effect has been attributed to improved wetting of Si surfaces by GaP when the Si is terminated by As compared with P, promoting layer-by-layer growth.\(^{[51]}\) To summarize, the growth of a GaP buffer layer resulted in island-like growth with rough morphology on both Si(100) and Si(111) (Figure 1a,b). This resulted in poor morphology and crystalline quality for GaP growths using the 2-step process on both Si(100) and Si(111) (Figure 2a–d). While further investigation is needed, the difference between the growths on Si(100) and Si(111) could be attributed to the formation of P-terminated facets at the initial stages of growth. A lower temperature for the buffer layer growth resulted in a smoother morphology and improved crystalline quality for GaAs grown on Si(100). This is attributed to the coalescence of smaller islands in the first stages of growth resulting in more mobile defects that can be more effectively annealed out. Comparing GaAs growth on Si(100) and Si(111) revealed that Si(111) is favorable, both in terms of a smoother morphology and higher crystalline quality. This is attributed to the Si(111) substrate promoting layer-by-layer growth due to a lower GaAs/Si(111) interface energy compared with Si(100).

3.3. GaP and GaAs SAG on Si

The SAG templates consist of a \(\approx400\) nm SiO\(_2\) dielectric layer deposited on Si(100) and Si(111) with 2–4 \(\mu\)m circular mask openings. The lateral and vertical growth rates for the SAG samples vary across each sample. For the GaP/Si(100) sample E1 and GaP/Si(111) sample E2, the vertical growth rates were about 9 and 12 \(\mu\)m h\(^{-1}\), respectively. For GaAs/Si(100) sample F1 and GaAs/Si(111) sample F2, the vertical growth rates were about 4 and 11 \(\mu\)m h\(^{-1}\). The SAG samples from growth E and F were studied in SEM, with images shown in Figure 5.

All of the SAG samples had larger regions (not shown in Figure 5) without polycrystalline deposition on the dielectric mask, indicating that the characteristic selectivity of HVPE is maintained at lower temperatures. In the regions with openings shown in the SEM images, however, some areas have a lot of polycrystalline deposition on the mask as shown for GaP/Si(100) SAG sample E1 (Figure 5a) and GaAs/Si(100) SAG sample F1 (Figure 5c). Some areas were even completely coalesced with growth, as shown for GaP/Si(111) sample E2 (Figure 5b). The GaAs and GaP SAG samples demonstrate that, with some optimization of the growth conditions, a high selectivity between the Si substrate and dielectric mask can be maintained even while growing in the unconventional regimes required by VME. However, around the mask openings all samples showed various degrees of deposition on the mask. This variation in selectivity is unexpected, as the same processing was used to fabricate each SAG template and the dielectric mask should be homogenous both across each sample and between different samples. In MBE, being a far-from-equilibrium process, polycrystalline deposition on dielectric masks occurs when the adsorbed precursors on the mask are not able to diffuse sufficiently far to reach the mask opening.\(^{[52]}\) A similar effect could occur during VME, where the LT drives the process away from equilibrium. As such, the polycrystalline deposition seen between the mask openings on sample F1 (Figure 5c) could be due to roughness on the mask introduced during the SAG template processing or pregrowth cleaning, which might reduce the diffusion length of adsorbed precursors. This would explain why the selectivity is so much higher in other regions and on other samples, such as sample F2 grown alongside F1 (Figure 5d). The selectivity can be improved by introducing a flow of excess HCl, suppressing the nucleation on the masked areas. Improving the selectivity is important for the development of VME SAG and will be systematically investigated in future work, including reviewing the SAG template preparation process.

As seen in the SEM images (Figure 5), all samples have a rough morphology without any of the faceting that often characterizes SAG.\(^{[53]}\) GaP/Si(100) SAG sample E1 and GaP/Si(111) SAG sample E2 in particular were expected to exhibit faceting, both as the GaP/Si(111) sample B2 grown with the same conditions resulted in a faceted morphology (Figure 2b) and due to a well-pronounced faceting occurring on previously reported GaP grown on GaAs SAG templates using similar growth conditions.\(^{[44]}\) As faceting is usually caused by low surface energy planes emerging due to growth rate being anisotropic,\(^{[55]}\) this suggests that the growth is not solely kinetically controlled but...
that there instead are some mass-transport effects determining the shape of the growth.

Analysis of strain and crystalline quality of the SAG samples was carried out on GaP/Si(111) SAG sample E2 and GaAs/Si(111) SAG sample F2 using Raman mapping, as shown in Figure 6. The Raman mapping shows how the longitudinal optical (LO)-phonon frequency and FWHM vary over the scanned area, with the positions of SAG template mask openings indicated by dashed circles (Figure 6). The peak frequency and FWHM are determined by Lorentzian fitting, taking the position of the fitted curve as the phonon frequency. Both GaP and GaAs samples show a higher LO frequency and FWHM at and near the mask openings compared with regions outside the mask openings. The two hotspots in the center of the mask opening of GaAs/Si(111) SAG sample F2 are due to a particularly noisy signal. The maps presented of sample E2 (Figure 6a,b) are of a fully coalesced region similar to that shown in the SEM image (Figure 5b). The maps of F2 are of a region similar to the one shown in the SEM image (Figure 5d), but where growth from two adjacent mask openings have coalesced. In a disordered crystal, compared with an ordered one, LO phonon Raman peaks tend to get red-shifted and broadened, whereas compressive strain can introduce a blue-shift. This is consistent with the Raman maps of sample F2, as the linewidth decreases away from the mask opening by \(\approx 2\) cm\(^{-1}\) due to the filtering of defects from the GaAs/Si interface and the phonon frequency increases by \(\approx 1\) cm\(^{-1}\) around the mask opening due to the compressive strain caused by the lattice mismatch. For sample E2, there is a similar decrease in phonon linewidth away from the mask opening of \(\approx 0.5\) and a \(\approx 0.5\) cm\(^{-1}\) blue-shift in the phonon frequency at the mask opening. The decrease in linewidth is considerably lower than for sample F2, and since the lattice mismatch between GaP and Si is very small, the blue-shift in phonon frequency at the mask openings in sample E2 is probably due to a higher crystalline quality in those regions. This indicates that the growth in E2 shown in the SEM image (Figure 5b) did not only coalesce from the mask openings but also incorporated polycrystalline depositions on the mask, resulting in a continuous layer with a high degree of disorder.

The properties of GaAs/Si grown by SAG are also investigated by characterizing GaAs/Si(100) SAG sample F1 and GaAs/Si(111) SAG sample F2 using PL-mapping, as shown in Figure 7. The PL mapping shows how the PL emission wavelength and peak FWHM vary over the scanned area, with the positions of the SAG template mask openings indicated by dashed circles (Figure 7a–d). The maps of F1 were carried out on an area similar to the one shown in the SEM image (Figure 5c). As shown in Figure 4c, unstrained GaAs emits at 871 nm which corresponds to its bandgap of 1.424 eV at room temperature. It is interesting to note that the GaAs grown on the Si(100) SAG template emits at a lower energy, whereas the GaAs grown on the Si(111) SAG template emits at a higher energy. The lower emission energy indicates tensile strain, similar to what was seen for GaAs/Si(100) sample C1, which is probably due to the same thermal mismatch between the GaAs layer and Si substrate. The presence of the dielectric mask does not seem to significantly influence the strain generation or relaxation. The higher emission energy seen in the map of sample F2 (Figure 7c) conversely indicates the presence of some compressive strain. This could be explained by the GaAs layer relaxing its misfit strain to a lesser extent during growth due to the filtering of threading dislocations, leaving some residual compressive strain due to the lattice mismatch between the GaAs layer and Si substrate. This is further supported by the lower FWHM away from the SAG mask opening seen for sample F2 (Figure 7d). It is also worth noting that the FWHM away from the mask...
opening is generally lower than the FWHM of 28 nm seen for the GaAs/Si(111) sample C2 (Figure 4c), and also that the lowest FWHM is obtained at the point where the growths from the two adjacent mask openings have coalesced, indicated by a black arrow in the upper right corner of the sample F2 map (Figure 7d). This behavior is far less prominent for the GaAs/Si(100) SAG sample F1 (Figure 7b), which is most likely due to the incorporation of the polycrystalline deposition seen on the mask in the SEM image (Figure 5c). The areas at the edges of the map with significantly higher FWHM values (Figure 7b) are due to such polycrystalline depositions. Similar to what was observed in the Raman mapping of GaP/Si(111) SAG sample E2, the beneficial defect filtering is only observed when the selectivity is sufficiently high. Optimizing the growth conditions to improve the selectivity would lead to much improved film growth on Si SAG templates, which will be investigated in future works.

4. Conclusion

VME is a promising technique for taking advantage of the economic benefits of HVPE-based III–V/Si integration. To fully realize this, however, a deep understanding and thorough control of the initial nucleation and properties of the low-temperature buffer layer are required. The results presented in this work indicate a number of different possible investigations toward meeting these requirements. A low-temperature GaP buffer layer grown directly on Si(100) and Si(111) by VME has been studied and found to have a rough morphology in both cases. The parameters used for the buffer layer was also used during two-step growth of GaP on Si to investigate the relationship between the layer grown during the first and second steps of such a growth. Several improvements can be made by optimizing the temperature during the buffer layer growth and reducing defects by annealing. Two-step growth of GaAs on Si by VME is also presented, and it is demonstrated how a subtle change in buffer layer growth temperature significantly impacts the overall grown layer. It is found that growth on Si(111) is favorable to growth on Si(100) for both GaP and GaAs based on HRXRD crystalline quality analysis. Contrary to expectation, the crystalline quality of GaAs/Si was found to be generally higher than that of GaP/Si despite the higher lattice mismatch, which was attributed to the AsH₃ pretreatment of the Si substrates employed during GaAs growth. Finally, initial results of VME-enabled SAG of GaAs and GaP on masked Si templates have been presented. It is shown that it is possible to retain the characteristic high selectivity of HVPE during VME conditions and evidence of material improvement by defect filtering is presented. This
opens up a range of possibilities for future applications of the VME technique as it would bypass the need for nucleation layers grown by other epitaxial techniques during SAG by HVPE. This work lays the foundation for future investigation and optimization that will lead to a cost-effective platform for III–V/Si integration using the strengths of HVPE while bypassing its drawbacks, especially for photovoltaic applications where the economic benefits are particularly important.

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Conflict of Interest
The authors declare no conflict of interest.

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heteroepitaxy, hydride vapor phase epitaxy, III–V/Si integration, selective area growth, vapor mixing epitaxy
