A Ka-band TDD front-end chip with 24.7% bandwidth and temperature compensation technology

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Abstract: This paper presents a compact Ka-band TDD front-end chip with temperature compensation technology. The front-end chip is integrated with a passive switch, a low noise amplifier (LNA) and a power amplifier (PA). Temperature compensation bias network is used to reduce the gain ripple versus temperature, and co-design method between the amplifiers and the switch is used to enhance the bandwidth. The gain ripple is less than ±0.7 dB when the temperature ranges from −55°C to +85°C. The circuit works from 30.5 GHz to 39.1 GHz, with a 24.7% relative bandwidth. The chip is fabricated with GaAs pseudomorphic high electron mobility transistor (pHEMT) technology. The gain of the receiver (RX) link is 26.6 dB, and the noise figure of it is 2.95 dB at 36.5 GHz. The gain of the transmitter (TX) link is 26.0 dB, and the output 1 dB compression point of it is 16 dBm.

Keywords: switch, temperature compensation, GaAs, LNA, PA

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

Ka-band is one of the promising bands for many applications, such as phased array radar, back-haul networks and the future 5G communication, as broad bandwidth can be used [1, 2]. In the time division duplexing (TDD) mode transceiver systems, the front-end with TR switch is one of the key components and it is required to be able to work well under different temperature. However, the loss of passive switches and the gain of active amplifiers change considerably with the variation of the temperature, due to the change of the transistors’ parameters. This influences the performance of the systems. If the gain of the TX link or RX link decreases, the output power of the transmitter will decrease or the noise figure of the receiver will increase. As a result, the detection distance decreases if it is used in the phased array radar system or the communication distance decreases if it is used in the communication system. On the other hand, if the gain increases, the receiver will compress or even saturate, which will influence the short range detection or communication. Therefore, keeping the gain of the front-end stable is important to make the systems robust.

A front-end chip containing a TR switch, an LNA and a PA is presented in this paper. Amplifiers and passive switch are co-designed to compensate the gain variation and enhance the bandwidth. A bias network integrated with thermistors is used to control the gain of amplifiers versus temperature so that the gain of amplifiers and that of the switch change in the opposite direction. Then the gain variations are neutralized. The gain ripple of the proposed front-end chip is less than ±0.7 dB versus temperature from −55°C to +85°C. The Circuit works from 30.5 GHz~39.1 GHz, which achieves a 24.7% relative bandwidth. Additionally, interconnection bonding wires are modeled and taken into account in this design. The gain of RX link is 26.6 dB, and that of TX link is 26.0 dB. The noise figure of
RX link is 2.95 dB at 36.5 GHz and is less than 3.9 dB for the whole operating band. The OP1dB of TX link is more than 16 dBm, and the IP1dB of RX link is −14 dBm. The total current consumption is 95 mA with 5 V power supply and −5 V bias.

2 Circuit design

2.1 Switch module architecture

The architecture of the proposed front-end chip is shown in Fig. 1. A passive switch with high linearity is used for the antenna terminal. A PA and an LNA are set in the TX and RX links respectively. The amplifiers are biased by a temperature compensated bias network, which contains thermistors. The bias voltage of amplifiers changes versus temperature according to the resistance of the thermistor so that the gain of amplifiers changes correspondingly, which will compensate the variation of the passive switch loss. Additionally, bandwidth and stability are both enhanced by setting the peak gain point of each component different.

![Fig. 1. The architecture of the proposed switch module.](image)

2.2 Passive switch

![Fig. 2. The passive switch structure (a) based on series and parallel transistors (b) based on transmission lines.](image)

Two passive switch structures are usually used. One is based on series and parallel transistors as shown in Fig. 2a. This structure contains series transistors in the signal links, which increases the isolation of the turn-off link. It occupies a small area as no transmission lines or inductors are used. However, the impedance of transistors varies versus temperature because of the variation of the threshold voltage. Meanwhile, the series transistors increase the loss of the turn-on link, and the isolation of the turn-off link decreases fast when used in the millimeter-wave band because of the existence of the parasitic capacitors [3]. Structure in Fig. 2b is used in this design. Series χ/4 transmission lines are used instead of the series transistors [4, 5], for the reason that the loss of the χ/4 transmission lines is temperature independent, which reduces the gain variation of the switch module.
Consequently, only the turn-on resistors in the parallel branch influence the gain variation. Then the reduced gain variation is compensated by the amplifiers.

2.3 Current-reuse amplifiers and interconnection bonding wires

The schematic of the LNA is shown in Fig. 3. The LNA contains four stages, and the current-reuse structure [6, 7, 8] is used to minimize the power consumption. The stage 1 and 2 reuse the DC current and the same as the stage 3 and 4. The schematic of the PA is shown in Fig. 4. The stage 1 and 2 also reuse the DC current, while the stage 3 and 4 are common source structure to enhance the output power and efficiency performance. The bias terminals in both amplifiers are connected to the temperature compensated bias network. The gain of the LNA and PA can be controlled using this network, and then the gain variation caused by the passive switch can be compensated. Also, each stage in LNA or PA is designed in different frequency points to enhance the bandwidth and the stability.

![Fig. 3. The schematic of the LNA](image)

![Fig. 4. The schematic of the PA](image)

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![Fig. 5. The (a) structure and (b) model of bonding wire](image)

Besides, the bonding wires at the input of the PA and the output of the LNA are modeled and taken into account in this design. Typically, the bonding wire for the RF connection has a diameter of 25 µm and a length from 400–600 µm. Therefore, in this work, a bonding wire with the length of 500 µm is modeled as an inductor with a series resistor and parasitic capacitors firstly [9], as shown in Fig. 5. The model is used in the circuits to simplify the design process and simulation time. Then, the bonding wires and the whole layout are simulated using EM simulation software to include all of the parasitic components. Finally, the layout is optimized based on the EM simulation result.
2.4 Bias network

The schematic of the bias network is shown in Fig. 6. The T1~T2 are off-chip thermistors, and R1~R5 are fixed resistors. The resistance of the thermistors decreases linearly when the temperature goes up, and the bias voltage increases as shown in Fig. 7(a). To adjust the slope of the curve, resistors are put in parallel with the thermistors as shown in Fig. 7(b), which makes it suitable for the demand of temperature compensation. Meanwhile, the series cells of thermistors generate a proper bias point at the room temperature. The variable bias voltage makes the amplifiers have a proper gain on the condition of different temperature and compensates the loss variation of the passive switch [9, 10].

3 Simulation and measured results

The size of the whole chip is $2.76 \times 1.85 \text{mm}^2$ and the die photo is shown in Fig. 8. The simulated and measured S-parameters are shown in Fig. 9. As is show that the switch operates from 30.5 GHz to 39.1 GHz. The measured gain of RX link is 26.6 dB, and that of TX link is 26 dB. The gain variation versus temperature is shown in Fig. 10, which is $\pm 3 \text{ dB}$ for RX link and $\pm 1.6 \text{ dB}$ for TX link versus temperature from $-55 \degree C$ to $+85 \degree C$ without temperature compensation. While using the temperature compensation circuit, an attractive variation of $\pm 0.7 \text{ dB}$ for both links can be obtained. The noise figure of the RX link in different temperature is shown in Fig. 11. The minimum noise figure is 2.9 dB in 25°C and less than 3.9 dB for the whole operating band. Moreover, it is the less than 5.9 dB in all temperature. The IP1dB point of the RX link is larger than $-14 \text{ dBm}$, and the
OP1dB point of the TX link is larger than 16 dBm from 30 GHz to 40 GHz as shown in Fig. 12. The total current consumption is 95 mA with a 5 V power supply and −5 V bias.

4 Conclusion

This letter presents a TDD front-end chip with a 24.7% relative bandwidth using the temperature compensation technology. The gain variation is less than ±0.7 dB when temperature varies from −55°C to +85°C.