High-frequency pulse width modulation noise reduction for permanent magnet synchronous motors using hybrid asymmetrical regular sampled modified space-vector pulse width modulation

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1 INTRODUCTION

Permanent magnet synchronous motors (PMSMs) are gradually used in fields of domestic appliances and electric vehicles due to its high power density, torque density and high efficiency [1, 2], whose noise level directly influences the ear comfort. And space-vector pulse width modulation (SVPWM) is widely employed in voltage source inverters (VSIs) to achieve excellent static and dynamic performances for PMSM drive; however, unpleasant pulse width modulation vibration as well as audible noise are generated by undesirable high-frequency PWM voltage and current harmonics nearby carrier frequency and its multiples during intrinsic switching process [3–5]. Usually, the switching frequency is selected between 2–20 kHz(within the human hearing range) to reduce the switching losses; thus, it is necessary to address this problem.

From the perspective of power device, the emerging wide bandgap power devices including silicon carbide and gallium nitride takes advantages over conventional silicon such as higher breakdown voltage with lower on-resistance and faster switching speed [6, 7]. Nevertheless, the cost and current limitation are obstacles to prevent them from being widely applied. In view of control strategy, carrier phase-shift also called interleaving technique and improved SVPWM have been proposed to reduce PWM harmonics.

Parallel interleaving topologies can replace each phase-leg with multiple ones to increase the power level with carrier phase shift [8]. Symmetrically interleaving N voltage source converter modules cancels all harmonics in both the output voltage and the dc-link current except for the N-multiples of the carrier harmonic and their sideband components, but the large inductors used to suppress circulating current are obstacles to be widely applied [9, 10]. And coupled inductors...
are proposed to substitute inductors for its small volume [11, 12]. For two paralleled inverters driving a three-phase load, symmetrically interleaving \( \pi \) can eliminate the odd-order carrier frequency harmonics, however, without impact on twice carrier frequency harmonics, but two three-phase VSIs are employed.

Random PWM (RPWM)-based methods spread power of noise over a wide range of frequency domain, and the peak of PWM noise in phase voltage is decreased by 9–10 dB [13–17]. Random switching frequency PWM (RSF-PWM) as one of the RPWM techniques has good performance of voltage and current harmonics elimination at both low and high speed [14]. However, incomplete reduction of PWM harmonic noise and elevation of frequency band still need further study. Similarly, periodic carrier frequency modulation technique changes the switching frequency according to the periodic function, such as sinusoidal wave, sawtooth wave and triangular wave [18], whereas this technique has little influence on the elevation of frequency band with comparison with RSF-PWM method. Modified SVPWM (MSVPWM) introduced in [19] exchanges the active vector in the next half of the PWM period and reduces the odd-order carrier frequency harmonics at the cost of slightly increasing the switching losses. Combining the MSVPWM and RPWM can also further reduce the harmonic peak through the spread of harmonic energy [20]. However, the whole frequency band is elevated and system resonance may be induced since the harmonic energy moves to the low and medium frequency.

This paper extends the study of [19] and further eliminates the odd-order PWM noise on the three-phase PMSM driven by three-phase VSIs by changing the phase voltage waveform. The periodical switching frequency can reduce the even-order PWM harmonics with the merits of avoiding the elevation of the frequency band and system resonance. With the proposed strategy, the acoustic noise under 20.0 kHz can be reduced to a great extent when the switching frequency is selected 4.0 kHz. Although the proposed method is implemented on the PMSM, it can also be used in other drive systems using SVPWM.

The rest of this paper is organised as follows. Section 2 introduces the HARSM-SVPWM, discusses its characteristics and illustrates the implementation process. The elimination principle of PWM harmonics is elaborated in Section 3. Experiments are carried out on the three-phase PMSM using digital signal processor control unit in Section 4. Finally, conclusions are presented in Section 5.

## 2 | INTRODUCTION OF THE PROPOSED METHOD

### 2.1 | HARSM-SVPWM

SVPWM commonly used in digital processors is actually symmetrical regular sampled SVPWM, whose generation process in sector I is illustrated in Figure 1(a). \( f_a(t), f_b(t), f_c(t) \) are three-phase reference waves; \( S_a, S_b, S_c \) are three-phase switching states of upper arm; \( T_c \) is carrier period; \( u_a(t) \) is phase voltage waveform, which can be expressed as (1)

\[
u_{aN} = \frac{1}{3} (2S_a - S_b - S_c) V_{dc}.
\]

Focusing on the switching state and the phase voltage waveform, the waveforms are symmetrical about the time moment \( T_c/2 \). Since the phase voltage waveform has the period of \( T_c \), thus the harmonics exists in carrier frequency and its multiples.
Based on the conventional symmetrical regular sampled SVPWM in Figure 1(a), MSVPWM shown in Figure 1(b) exchanges the active vector during the next half carrier period from 111-110-100-000 to 111-100-110-000. Therefore, the phase voltage waveform are not symmetrical against the medium moment. Note that although the period of voltage waveform has been changed into half, the corresponding harmonic frequency does not directly start from twice carrier frequency, as the waveform in former and the latter half period are identical. According to Flourier transform, the carrier frequency and its odd multiples harmonics still exist.

As a consequence, the HARS-SVPWM is proposed in order to change the waveform period of phase voltage for further reducing the remaining odd and even multiples of carrier frequency harmonics. The PWM generation process with the proposed method in sector I during one carrier period is illustrated in Figure 1(c). The active vectors are also altered the sequence in the latter half carrier period. More importantly, the reference waveforms are calculated twice in one period by asymmetrical regular sample, and hence the phase voltage waveform becomes different in the former and the latter half carrier period, which therefore removes the odd multiples carrier frequency component of phase voltage harmonics.

Apart from the waveform change of phase voltage, the carrier period of HARS-SVPWM also varies according to the periodical function, such as sawtooth function, whereas MSVPWM maintains the same carrier period. Researchers in [21] investigates the effect of noise reduction for different periodic function, verifying sawtooth function and its period equal to the fundamental wave. Moreover, it should be noted that wider variation range $\left(f_{max} - f_{min}\right)$ of switching frequency can remove further harmonics according to application requirement.

With the proposed strategy, all odd multiples of carrier frequency harmonics of phase voltage can be removed and all even multiples of carrier frequency harmonics of phase voltage can be reduced. The proposed HARS-SVPWM achieves the good performance of the PWM harmonics of VSI.

### 2.2 Discussion of HARS-SVPWM

#### 2.2.1 Switching loss

Since the switching states have been changed in the proposed HARS-SVPWM, it is necessary to compare the switching loss between the conventional fixed switching frequency SVPWM and the proposed method. Since the switching loss difference of using varying carrier frequency or not is relatively small [22], hence we investigate HARS-SVPWM with fixed carrier frequency for the influence on the switching loss.

Different from the conventional SVPWM, the proposed strategy eliminates the odd multiples of carrier frequency harmonics. To achieve the similar effects, twice carrier frequency should be set for the conventional SVPWM. For example, similar high-frequency performance requires the carrier frequency to set 6 kHz for conventional SVPWM but 3 kHz for the proposed method, whose the average switching frequency is 4 kHz. In other words, the proposed HARS-SVPWM with actual switching frequency 4 kHz can accomplish almost the same high-frequency harmonic performance against conventional SVPWM with actual switching frequency 6 kHz.

Note that the switching loss is not equivalent to the switching frequency and is actually dependent on the power factor, namely the phase angle between the phase voltage modulation wave and the phase current, due to the uneven distribution of switching frequency in a fundamental phase voltage for the proposed strategy. The average switching loss of the proposed HARS-SVPWM and the conventional SVPWM can be evaluated and written as [23]

$$
P_{avg\text{-switching-loss}} = \frac{1}{2\pi} \int (E_{on} + E_{off}) |i| f_c \text{d}\theta
$$

where $E_{on}$ and $E_{off}$ represents turn-on switching energy coefficient and turn-off switching energy coefficient, respectively. $i_c$ means the phase current and $f_c$ is the switching frequency.

Figure 3 shows $f_c$ distribution in the six sectors for the phase reference wave A and phase A current waveform when the phase angle is 0° and 90°. Due to the HARS-SVPWM, the switching frequency in sector II and V is 2$f_c$ for phase A. According to (2) and Figure 3, when the phase angle changes from 0° and 90°, the reduction ratio of switching loss of the proposed method with carrier frequency $f_c$ and the conventional SVPWM with carrier frequency 2$f_c$ can be calculated by integral. Note that the maximum and minimum reduction ratio can be calculated as 43.3% and 25% when phase angle is 0° and 90°, respectively. Therefore, the proposed HARS-SVPWM has the advantage of the switching loss reduction against the conventional SVPWM when considering similar harmonic spectrum. Because the PWM current harmonics is reduced, the power loss of the motor such as stator iron loss, rotor eddy current loss as well as copper loss will also be improved.

![FIGURE 2 Switching frequency varying function of the proposed strategy](image-url)
2.2.2 Dynamic response

The dynamic response of the drive system is decided by the control loop composed of hardware and the software program. The hardware work procedure is shown in Figure 4. The phase currents and rotor position are sampled by the current transducer and the position encoder, respectively. Then the signal regulation circuits usually composed of analogue-digital amplifiers spend time handling the information. After transmitting to micro-control unit (MCU), MCU gives the pulse command to drive circuits. Finally, the power devices turn on and off. During the control loop, hardware delay should be considered in the design process. More importantly, the inertia of the motor as a key factor should be seriously considered.

In the view of software, MCU acquires the phase current from the transducer and the position information at time \( t = k \). Then within \( t = k \) and \( t = k+1 \), in the interrupt program, the MCU adopts the algorithm and calculates the PWM duty cycle. And then, when \( t = k+1 \), the calculated compare value are loaded in the register. Thus, the smaller calculation step is, the better dynamic performance of the drive system will have.

As shown in Figure 1(c), the calculation step of the proposed HARSM-SVPWM is \( T_c/2 \) but \( T_c \) for the conventional SVPWM and MSVPWM. Although the proposed strategy varies its carrier period, sometimes larger than the center carrier period and sometimes smaller, the calculation step is always smaller than the other two techniques. Therefore, the drive system has better dynamic performance with the proposed method in view of software algorithm. Note that the dynamic response of the whole drive system is dependent on many links in Figure 4, including hardware and software. The improvement of the whole drive system using the proposed strategy may be unobvious.

2.3 Implementation of the proposed method

The proposed HARSM-SVPWM demonstrates good performance as mentioned above. Here gives the implementation method of the proposed strategy. Considering the twice more action for the PWM waveform in one carrier period, control law accelerator (CLA) in MCU TMS320F28075 in this paper is conducted to help us capture the action moment. Figure 5 illustrates the MCU implementation process in a sequential way after judging the sector I. The detailed actions are shown as follows.

1. When the counter reaches peak, the central processing unit (CPU) executes interrupt program: loading the \( T_{a1}, T_{b1}, T_{c1} \) calculated in the last half period into active compare register A, then calculating the compare value \( T_{a2}, T_{b2}, T_{c2} \) of the next half period and loading them to shadow compare register A. Besides, compare value \( T_{a2}+T_{c2}-T_{b2} \) is calculated and loaded into the shadow compare register B.

2. When the counter becomes zero, interrupt is received by CPU and the calculated compare value \( T_{a2}, T_{b2}, T_{c2} \) are loaded in the active compare register A. Compare value \( T_{a3}, T_{b3}, T_{c3} \) are gotten and loaded in shadow compare register A. Additionally, compare value \( T_{a2}+T_{c2}-T_{b2} \) is loaded into the active compare register B.

3. At the counter value \( T_{c2} \), interrupt happens and is received by the CLA. CLA forces low action on \( S_b \) sets the compare register B to act and disables the compare register A.

4. At the counter value \( T_{a2}+T_{c2}-T_{b2} \), the \( S_b \) is set high according to configuration of compare register B.

5. When counter value is equal to \( T_{a2} \), interrupt happens and is received by the CLA. CLA forces low action on \( S_b \) sets the
TABLE 1  Compare value of the modified switch in six sectors

| Sector | S | Moment (°) | Moment (°) | Moment (°) |
|--------|---|------------|------------|------------|
| I      | Sb | Tc         | Tc+Tb-Tb   | Ta         |
| II     | Sb | Tb         | Tb+Ta-Ta   | Tb         |
| III    | Sb | Ta         | Ta+Tc-Tc   | Tb         |
| IV     | Sb | Tb         | Tb+Tc-Ta   | Tb         |
| V      | Sb | Tb         | Tb+Ta-Ta   | Tb         |
| VI     | Sb | Tb         | Tb+Ta-Ta   | Tb         |

compare register A to act and disables the compare register B.

New carrier period \(T_c\) is loaded into the active period register to change the carrier period in a confined range. Similar steps can be executed in the following waves.

Table 1 gives the action compare value of the medium moment in all the sectors. For example, in sector II, switch \(S_b\) should be modified, actions should be taken on \(S_b\) at counter moment \(T_c+T_b-T_b\) at counter moment \(T_c\).

3 | PRINCIPLE OF NOISE ELIMINATION

Focusing on the phase voltage waveform with HARSM-SVPWM, it is equivalent to the generation process using sawtooth carrier with carrier frequency \(2f_c\). As a consequence, the output PWM voltage of the HARSM-SVPWM without carrier frequency variation is equivalent to single-edge sawtooth carrier regular sampled modulation, and using double Fourier integral in a unit cell [24], it can be expressed as

\[
E_h(t) = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \left[ A_{mn} \cos \left( 2m \omega_c t + \theta_n \right) + n \left[ \omega_c t + \theta_n \right] \right] + B_{mn} \sin \left( 2m \omega_c t + \theta_n \right) + n \left[ \omega_c t + \theta_n \right] \]

(3)

where the carrier index variable \(m\) and the baseband index variable \(n\) define the angular frequency of each harmonic component groups as \(m\omega_c + n\omega_0\). \(\omega_c\) and \(\omega_0\) are the carrier frequency and fundamental wave frequency, respectively. \(\theta_n\) and \(\theta_0\) are the phase offset angle for carrier wave and fundamental wave, respectively. The magnitudes of the harmonic components defined in (3) are the \(A_{mn}\) and \(B_{mn}\) coefficients, which are very complicated. It can be seen from formula (3) that the high-frequency harmonics concentrate on the \(2m\omega_c + n\omega_0\) groups, which verifies the elimination of the odd multiples of carrier harmonics. Note that the varying switching frequency are distributed the concentrated energy, and thus the amplitude of high-frequency even-order carrier harmonics are also reduced.

Figure 6 shows the equivalent circuits for the high-frequency carrier harmonics. By equivalent circuit, it can be seen that the harmonic phase voltage and impedance determine the amplitude of the current harmonics. Based on the equivalent circuits, the simulation results of phase voltage and current harmonics near 4 kHz and 8 kHz are shown in Tables 2 and 3 when the dc voltage is 30 V and the modulation ratio is selected 0.2, 0.5 and 0.8. \(L_s\) is equal to 0.5 mH. \(R_s\) is equal to 10Ω. The carrier frequency varies between 3.8 kHz to 4.2 kHz. It can be seen that the fixed switching frequency SVPWM has the highest amplitude phase voltage harmonics, thus producing the highest current harmonics. With the increase of modulation ratio, the harmonics get larger with the three-method. Carrier frequency harmonics will be curbed with the MSVPWM. However, twice carrier frequency harmonics is not impacted. The proposed method HARSM-SVPWM can further reduce the carrier frequency harmonics but also decrease the twice carrier frequency harmonics against SVPWM.

| Harmonics amplitude/\(\text{dBV}\) | Modulation index | SVPWM | MSVPWM | HARSM-SVPWM |
|---------------------------------|------------------|-------|--------|-------------|
| 4 kHz                           | 0.2              | -19.67| -25.45 | -32.64      |
| 0.5                             | -3.02            | -24.35| -32.89 |
| 0.8                             | 4.83             | -24.26| -32.92 |
| 0.2                             | 7.27             | 7.33  | 2.17   |
| 8 kHz                           | 0.5              | 12.59 | 12.30  | 7.78        |
| 0.8                             | 9.73             | 9.57  | 6.36   |

TABLE 2  Phase voltage harmonics amplitude of SVPWM, MSVPWM and HARSM-SVPWM for different modulation index.

| Harmonics amplitude/\(\text{dB}\) | Modulation index | SVPWM | MSVPWM | HARSM-SVPWM |
|---------------------------------|------------------|-------|--------|-------------|
| 4 kHz                           | 0.2              | -44.59| -50.68 | -59.35      |
| 0.5                             | -27.38           | -49.44| -59.82 |
| 0.8                             | -19.76           | -49.24| -59.90 |
| 0.2                             | -21.37           | -21.27| -26.43 |
| 8 kHz                           | 0.5              | -16.38| -16.31 | -20.98      |
| 0.8                             | -18.93           | -19.18| -22.48 |
4 | EXPERIMENTAL VALIDATION

A PMSM drive system has been set up to verify the capability of PWM noise reduction with the proposed HARSMS-SVPWM practically. The experiment platform is based on MCU C2000 TMS320F28075 from Texas Instrument to validate the above analysis and the test bench is shown in Figure 7. Voltage differential probe measures the phase voltage of the PMSM. The Bruel & Kjær® 2250S noise analyser is used to measure acoustic noise from motor at distance of 10 cm. Hysteresis dynamometer loads the motor. The specification and parameters of the drive system are listed in Table 4. The PWM phase voltage harmonics, phase current and acoustic noise are compared with the method of fixed-frequency SVPWM, MSVPWM, and the proposed strategy to show the advantages in removing PWM noise.

In the following results, the sampling point of the fast Fourier transform (FFT) for signals in oscilloscope is 125 k and the frequency resolution is 10 Hz. The varying range of switching frequency is 3.8–4.2 kHz. Note that harmonics spectrum can reflect the current ripple. Once the corresponding harmonics is reduced, the current ripple will be curbed. Therefore we only give the FFT results in the experimental results.

4.1 | Results for reduction of PWM voltage noise

Figure 8 shows the comparison results of phase voltage for three methods. When traditional method—namely, fixed switching frequency SVPWM, is implemented, as seen in Figure 8(a), the phase voltage harmonics at 4.0 kHz and 8.0 kHz is 5.17 dBV and 11.80 dBV, respectively, and their amplitudes are greater than the other methods. It also can be seen that MSVPWM decreases the carrier frequency harmonics by 17.68 dBV, and has almost no effect on the twice carrier frequency harmonics. Whereas the proposed HARSMS-SVPWM in Figure 8(c) not only reduces the first carrier harmonics to -29.86 dBV but also decreases the second carrier harmonics by 4.32 dBV. By horizontal comparison, obviously, in Figure 8(c), the third carrier harmonics near 12 kHz are eliminated to a relative low level like first carrier harmonics and the magnitude of fourth carrier harmonics near 16 kHz in FFT window are reduced in terms of the amplitude. Some harmonics in Figure 8(c) still left near 4.0 kHz and 12.0 kHz due to the non-ideality of the algorithm, but the residual harmonics can still be suppressed by periodical switching frequency modulation.

4.2 | Results for reduction of PWM current noise

The FFT spectrum of phase current with three methods when motor runs at rated condition can be seen in Figure 9. MSVPWM reduces the carrier frequency harmonics by 17.25 dBA in Figure 9(b), compared with fixed-frequency SVPWM, which is not enough for noise reduction. The proposed strategy is able to reduce the carrier frequency harmonics and twice carrier frequency harmonics by 26.72 dBA and 5.48 dBA, respectively in Figure 9(c). Besides, the triple carrier frequency harmonics near 12.0 kHz is also reduced almost at frequency band. The quadruple carrier frequency harmonics near 16 kHz is also reduced by cutting the peak value as seen in FFT window of Figure 9(c). Note that the frequency band near 4 kHz and 12 kHz is not elevated obviously with the HARSM-SVPWM compared with the conventional SVPWM while the whole frequency band is lifted with the method in [20] using random switching frequency.

4.3 | Results for reduction of PWM acoustic noise

When motor runs at rated speed and under rated load, the spectrum of noise signal are shown in Figure 10, in which the PWM noise is in accordance with PWM current noise spectrum in Figure 9. Actually, the motor was driven on a test bench; the noise caused by mechanical vibration was also received by the noise analyser. Therefore, the low-frequency noise are large and the amplitude of noise has not been reduced obviously. Figure 10(c) shows the harmonic peak at 4.0 kHz is reduced to background noise level about −95.75 dBV. At the same time, the FFT results near 8 kHz also demonstrate that the magnitude of harmonics reduce 1.33 dBV. Moreover, the FFT results of acoustic noise signal obviously demonstrates no peak near 12 kHz in Figure 10(c). The magnitude of harmonics near 16 kHz in Figure 10(c) are reduced to background noise level compared with Figure 10(a) and (b). Comparing the figures in part 4.1, 4.2 and 4.3, it can be found that results of the phase voltage, current,
noise are consistent to validate the effectiveness of HARSM-SVPWM for the PWM noise elimination.

4.4 Results for different variation range

Different variation range of switching frequency also has influence on the even-order carrier frequency harmonics. The switching frequency range in this part is 3.5–4.5 kHz. Figure 11 shows the phase voltage, current and noise signal and their FFT analysis results. Comparing Figure 11(a) and 8(c), it can be seen that twice carrier frequency harmonics in phase voltage is further reduced by 3.26 dBV. Similar results can be found in Figures 11(b) and 9(c). When focusing on the noise signal in Figures 11(c) and 10(c), 0.9 dBV harmonics in twice carrier frequency harmonics is removed. Besides, carrier frequency harmonics near 4 kHz in phase voltage, current and noise are almost eliminated completely in Figure 11, which verifies the effectiveness of the proposed strategy.

4.5 Summary of the experimental results

In the last four parts, phase voltage, phase current and acoustic noise are investigated. In order to clearly show the reduction effect of the proposed strategy, Figure 12 demonstrates the acoustic noise reduction effect of the two methods, including MSVPWM and HARSM-SVPWM, compared with the
FIGURE 11  FFT results of (a) phase voltage, (b) phase current, (c) acoustic signal for different varying range of switching frequency with the proposed strategy

FIGURE 12  Results comparison of carrier frequency and twice carrier frequency acoustic noise

traditional fixed switching frequency SVPWM. HARSM-SVPWM1 means the switching frequency ranges from 3.8 to 4.2 kHz, while it is 3.5–4.5 kHz for HARSM-SVPWM2. It can be explicitly seen from Figure 12 that the proposed HARSM-SVPWM has better reduction performance against the other two methods.

5  CONCLUSION

This paper presents an effective strategy HARSM-SVPWM, which makes use of asymmetrical regular sampled SVPWM and adjusts the active vector of the half period of PWM to change the waveform of the phase voltage, therefore eliminating the odd-order carrier frequency harmonics. Moreover, the even-order carrier frequency harmonics are reduced by the periodical varying switching frequency.

The switching loss of the proposed HARSM-SVPWM can save at least 25% compared with the conventional SVPWM when achieving similar PWM harmonics spectrum. The dynamic performance using the proposed strategy can also be improved by decreasing the calculation step.

The experimental results further verify the analysis of the noise elimination principle and effectiveness of the proposed HARSM-SVPWM. Moreover, the frequency band is not elevated obviously compared with the existing methods. At last, the influence of different switching frequency varying range on the elimination of even-order carrier frequency is also discussed. And the experimental results demonstrate the wider varying range leads to lower harmonic peak.

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