A 36 Gb/s Wireline Receiver with Adaptive CTLE and 1-Tap Speculative DFE in 0.13 μm BiCMOS Technology

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Abstract This paper presents a 36 Gb/s receiver equalizer including an adaptive continuous time linear equalizer (CTLE), which is based on slope detection and a half-rate speculative decision feedback equalizer (DFE) in 0.13 μm BiCMOS technology for high speed serial link. The CTLE with middle frequency compensation can not only adjust the ratio of high frequency and low frequency components adaptively, but also provide a small amount of equalization to middle frequency range. A half-rate speculative DFE, which is connected to the back of the CTLE, can satisfy the time constraints and eliminate the residual inter-symbol interference. The chip area including pads is about 1.2 mm² and the power consumption is about 750 mW under 3.3 V power supply. Measurement results show that the receiver chip can effectively equalize 24 dB loss at Nyquist frequency and a clear eye diagram can be captured at 36 Gb/s.

key words: CTLE, slope detection, speculative, inter-symbol interference, eye diagram

Classification: Integrated circuits

1. Introduction

With the rapid progress of new internet services such as cloud computing and internet of things (IoT), the development of traditional parallel communication has encountered bottlenecks and the serial link communication has become the mainstream. When the data rate of serial link is above 5 Gb/s, it is difficult to maintain good signal integrity due to limited bandwidth, insertion loss, crosstalk and reflection [1, 2].

The CTLE can improve the signal integrity by raising the high-frequency component of the signal [3, 4, 5]. However, while the CTLE amplifies the high-frequency component of the signal, noise and crosstalk are potentially amplified. DFE can effectively eliminate inter-symbol interference caused by finite band, crosstalk, and reflection, but it is effective to eliminate the precursor [6, 7, 8, 9]. Therefore, the combination of CTLE and DFE is widely used to eliminate inter-symbol interference at the receiver [10, 11, 12, 13, 14]. Because of temperature variation, material properties, length and bends, it is very important for equalizer to automatically detect and critically compensate for the high frequency loss of channel. Continuous time adaptive equalizer can adapt its response to both the possible variations of the characteristics of the backplane [15, 16, 17, 18, 19]. Ref. [20] introduced that there are two loops in the adaptive continuous time equalizer for detecting high frequency and low frequency components, respectively. However, there is interference between the two loops. Adaptive CTLE with spectrum balancing method was adopted in Ref. [21]. Power-detection and V/I converter consumes large power, and some digital circuits result in a slow adaptive speed. Traditional adaptive CTLE based on slope detection has the issue that the middle frequency band can not be compensated, leading to a large number of tail-offs in impulse response and finally seriously increasing the burden of DFE [22].

In order to solve the issue that traditional adaptive CTLE manifests a depression in middle frequency section, this paper proposes an adaptive CTLE with middle frequency compensation. In addition, when the data rate reaches above 25 Gb/s, it is difficult to realize that the feedback path delay of the first tap is less than a UI for full-rate DFE, multiplexed full-rate DFE, half-rate DFE and multiplexed half-rate DFE, a half-rate DFE architecture with speculative first tap is adopted.

2. Architecture

2.1 Adaptive CTLE

In order to compensate for the high frequency loss of serial links at 36 Gb/s, a combination structure of adaptive CTLE with middle frequency amplifier as depicted in Fig.1 and half-rate DFE with speculative Ci tap described in Fig.2 is adopted in this paper. The received signal is divided in two paths. One path comprises a high frequency amplifier to amplify high frequency component. The other path is a low frequency amplifier to match the time delay of first path. The following middle amplifier compensates the loss in middle frequency band by adding a pair of zeros and poles. The compensation range of high frequency and low frequency is adjusted by the adaptive loop. Slicer
restores the output signal of the slicer to fixed swing. The three amplifiers of the forward path make the transfer function of the forward path more matched with the transmission of the channel so as to eliminate the inter-symbol interference as much as possible.

The adaptation of CTE is realized by feedback path, which mainly includes: 1) two slope detectors: detecting the slope of slicer input and slicer output respectively; 2) integrator: converting the slope (energy) of output signal of the two slope detectors into feedback control voltage $V_{ctrl}$ and $V_{ctrl}$. According to the difference of slope, the weight relationship between the high frequency amplifier and the unit gain amplifier is adjusted. If the slope of slicer input is lower than that of the slicer output, the $V_{ctrl}$ should be increased to improve the high frequency component. On the contrary, the low frequency component of the signal is not enough, the low frequency component should be adjusted by increasing the $V_{ctrl}$. By dynamically adjusting the high frequency and low frequency components of the signal, the inter-symbol interference is minimized.

2.2 Half-rate DFE with speculative tap

The half-rate DFE employing one speculative tap behind CTE is mainly used to eliminate residual inter-symbol interference. Fig. 2 shows half-rate DFE with speculative $C_1$ tap, in which the upper DFE (above the dotted line) deals with odd data and lower DFE (below the dotted line) deals with even data [24, 25]. Firstly, the adding and subtracting of tap coefficient $C_1$ is performed in advance, and then the output signal of MUX is selected by the previous output. That is, the even data is selected by odd data and vice versa. The feedback loop delay of $C_1$ is easier to be less than one UI, and the feedback loop of $C_2$ becomes the critical path, whose delay must be lower than 2 UI. Finally, the full rate data is recovered through a MUX. Compared with the half-rate structure, $t_{FB}$ is replaced by $t_{MUX}$, and the delay constraints is easier to be satisfied.

3 Circuit Design

3.1 Linear equalizer

Fig. 3 illustrates the main circuit of linear equalizer that is designed in this paper, which includes high frequency gain amplifier (high-pass path) and unit gain amplifier (all-pass path) [26, 27]. It can achieve the best effect through adjusting the tail current of the high frequency amplifier and the unit gain amplifier, i.e. adjusting the compensation range of the high frequency components and low frequency components of the linear equalizer. The passive peaking inductance $L$ is used to expand bandwidth of high frequency amplifier and a simply resistively-degenerated trans-conductor is used to expand bandwidth of unit gain amplifier. The transfer function of a linear equalizer can be expressed as:

$$H(s) = \frac{g_{m2,2}}{1 + g_{m2,2} \left( \frac{R_{L} \| R_c}{2} \right) \left( \frac{1}{2sC_L} \right)}$$

$$+ \frac{g_{m3,4}}{1 + g_{m3,4} \left( \frac{R_{E2}}{2} \right) \left( \frac{1}{2sC_L} \right)}$$

(1)

where $g_{m2,2}$ and $g_{m3,4}$ are trans-conductors of transistors $Q_1$ ($Q_2$) and $Q_3$($Q_4$) respectively. $R_L$ is load resistance, $R_{E1}$ and $C_k$ are negative feedback resistance and capacitance respectively, $R_{E2}$ is negative feedback resistance producing zero.
3.2 Middle frequency amplifier
In adaptive CTLE, the middle frequency amplifier designed is given in Fig. 4. The forward path is constituted by Q1, Q2 and load resistance R1, R2, and the feedback loop is composed of Q3-Q8, and low-pass filters consisted of C1 and R1[17, 28]. Fig.5 (a) and (b) display the output eye diagrams of linear equalizer without middle frequency compensation and with middle frequency compensation respectively. It follows that the latter effectively eliminates the tailing of impulse response and improves eye diagram opening.

Fig. 4. Middle frequency amplifier

Fig. 5. Comparison of simulation results: (a) Eye diagram with only linear equalizer (b) Eye diagram with linear equalizer and middle frequency amplifier

3.3 Slope detector and integrator
Fig. 6 depicts the detailed circuit of slope detector and integrator as described in Fig.1. The drain current of differential pairs M1 and M2 can be expressed as:

$$I_{out} = I_{d1} + I_{d2} = \frac{\mu C_w}{2} \left( \frac{W}{L} \right) \left( 2(V_{in,cm} - V_o) + V_{in,dm}^2 \right)$$  (2)

where $I_{d1}$ and $I_{d2}$ are drain currents of NMOS M1 and M2 respectively, $V_{in,cm}$ and $V_{in,dm}$ are corresponding common mode voltage and differential mode voltage respectively. The square term in the Eq. (2) indicates that the output is related to the energy of the input signal $V_{in}$. When the slope of the input signal increases, the output $I_{out}$ increases; conversely, when the slope of the input signal decreases, the output $I_{out}$ decreases [17, 28]. Similarly, the drain current $I_{out}$ of the NMOS M1 and M2 is used to detect the slope (energy) of the input signal $V_{in}$. 

3.4 Slicer
The slicer depicted in Fig.7 is consisted of two cascaded CML buffers [22]. The first stage has fast conversion time and can correct signal amplitude. In order to obtain fixed conversion time, the load of the second stage is capacitive load.

Fig. 7. Slicer

3.5 SCFL based D Flip-Flop
D Flip-Flop (DFF) plays an important role in speculative half-rate DFE. In order to implement a high-speed DFF, an architecture based on SCFL [26] is used, as shown in Fig. 8. It is consisted of two stages latch, one is called master latch, the other is called slaver. Each latch has three pairs of differential transistors. Take the master latch as an example, $Q_1(Q_2)$ is the input clock transistor, $Q_3(Q_4)$ is the sampling one and $Q_5(Q_6)$ is latch one. The current is converted into output voltage by load $R_l$. For SCFL latch, the clock signal must be large enough to ensure that $Q_1(Q_2)$ can be completely shut down. It has been known that the ratio of the latch transistor size and the sampling one has an effect on the working speed and capability of date retention. Considering retention capability, working speed and high bandwidth, the ratio is set as 0.8.

3.6 Summer
The summer is used to eliminate the post-cursors in speculative half-rate DFE. A two-tap summer based on current mode logic (CML) with common load resistors is shown in Fig. 9. The sum operation is achieved by the current flowing through the load resistor [26, 29]. The current of the $i^{th}$ tail current source can be expressed as:

$$I_i = C_i I_0$$  (3)

where $I_i$ is the current of $i^{th}$ tail, $I_0$ is main tap, $C_i$ is the tap coefficient and can be adjusted by the gate bias.
voltage of the tail current source. The effect of equalization is seriously influenced by $C_i$ which should be calculated by the impulse response of the channel.

![Fig. 8. SCFL based DFF](image)

**Fig. 8. SCFL based DFF**

![Fig. 9. Summer](image)

**Fig. 9. Summer**

4. Measurement Results

The receiver chip shown in Fig. 10 is fabricated in a 0.13 μm BiCMOS process and occupies an area of $1.01 \times 1.11 \text{mm}^2$ including all the test circuits and dissipates a total of power of 750 mW. As shown in Fig. 11, a 12 cm Rogers backplane is used as tested channel. The insertion loss and echo loss of Rogers backplane shown in Fig. 12 is 24 dB and 10 dB respectively at 18 GHz which is the Nyquist frequency.

![Fig. 10. Micrograph of receiver chip](image)

**Fig. 10. Micrograph of receiver chip**

Fig. 13 depicts the eye-diagram of a 25 Gb/s PRBS31 signal passed through tested backplane, it has been completely closed. The eye-diagram equalized by adaptive CTLE with middle frequency compensation is shown in Fig. 14. Obviously, the adaptive CTLE can effectively eliminates the inter-symbol interference and significantly improve the eye opening. Fig. 15 shows the eye-diagram after DFE equalization. The eye height is increased to 45.95 mV and the noise points in the center of eye diagram are less, which indicates that the DFE eliminates most post-cursors. In order to validate the performance of receiver chip, the data rate is increased to 36 Gb/s. Fig. 16 describes eye diagram of received 36 Gb/s with adaptive CTLE and DFE equalization. It can be seen that a better opening can still be obtained.

![Fig. 11. Rogers backplane](image)

**Fig. 11. Rogers backplane**

![Fig. 12. Measured channel insertion loss and echo loss](image)

**Fig. 12. Measured channel insertion loss and echo loss**

![Fig. 13. Measured eye diagram of received 25 Gb/s after the Rogers backplane](image)

**Fig. 13. Measured eye diagram of received 25 Gb/s after the Rogers backplane**
Fig. 14. Measured eye diagram of received 25 Gb/s with adaptive CTLE equalization

Fig. 15. Measured eye diagram of received 25 Gb/s with adaptive CTLE and DFE equalization

Fig. 16. Measured eye diagram of received 36 Gb/s with adaptive CTLE and DFE equalization

Table I. Performance summary and comparison

| Design | This work | [33] | [34] |
|--------|-----------|------|------|
| Technology           | 130nm (BiCMOS) | 28nm (CMOS) | 40nm (CMOS) |
| Date rate(Gb/s)     | 36         | 32   | 28   |
| Power supply(V)      | 3.3        | 0.9  | 0.9  |
| Structure            | Adaptive CTLE DFE | Adaptive CTLE DFE | Adaptive CTLE DFE |
| Channel loss         | 24         | 37   | 20   |
| (dB@Nyquist)         |            |      |      |
| Clocking             | Half-rate  | Half-rate | Half-rate |
| Area(µm²)            | 1.2        | 0.33 | 0.6  |
| Power(mW)            | 750        | 240  | 780  |

5 Conclusion

This paper designs a 36 Gb/s receiver chip over 12 cm Rogers backplane using a 0.13 µm BiCMOS process. The proposed adaptive CTLE with middle frequency compensation improves the flatness of frequency response in the whole frequency band and raises eye opening. Half-rate DFE architecture with speculative first tap can meet the timing constraint and remove most post-cursors at 36 Gb/s.

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