Quantum Approximate Optimization Algorithm (QAOA) is studied primarily to find approximate solutions to combinatorial optimization problems. For a graph with \( n \) vertices and \( m \) edges, a depth \( p \) QAOA for the Max-cut problem requires \( 2 \cdot m \cdot p \) CNOT gates. CNOT is one of the primary sources of error in modern quantum computers. In this paper, we propose two hardware independent methods to reduce the number of CNOT gates in the circuit. First, we present a method based on Edge Coloring of the input graph that minimizes the number of cycles (termed as depth of the circuit), and reduces up to \( \lfloor \frac{n^2}{2} \rfloor \) CNOT gates. Next, we depict another method based on Depth First Search (DFS) on the input graph that reduces \( n - 1 \) CNOT gates, but increases depth of the circuit moderately. We analytically derive the condition for which the reduction in CNOT gates overshadows this increase in depth, and the error probability of the circuit is still lowered. We show that all IBM Quantum Hardware satisfy this condition. We simulate these two methods for graphs of various sparsity with the ibmq_manhattan noise model, and show that the DFS based method outperforms the edge coloring based method, which in turn, outperforms the traditional QAOA circuit in terms of reduction in the number of CNOT gates, and hence the probability of error of the circuit.

1 Introduction

Near term quantum devices have a small number of noisy qubits that can support execution of shallow depth circuits (i.e., those with few operational cycles) only. Variational Quantum Algorithms (VQA) aim to leverage the power as well as the limitations imposed by these devices to solve problems of interest such as combinatorial optimization [2, 3, 4, 5], quantum chemistry [6, 7], and quantum machine learning [8, 9, 10]. VQA divides the entire computation into functional modules, and outsources some of these modules to classical computers. The general framework of VQA can be divided into four steps: (i) encode the problem into a parameterized quantum state \( |\psi(\theta)\rangle \) (called the ansatz), where \( \theta = \{\theta_1, \theta_2, \ldots, \theta_k\} \) are \( k \) parameters; (ii) prepare and measure the ansatz in a quantum computer, and determine the value of some objective function \( C(\theta) \) (which depends on the problem at hand) from the measurement outcome; (iii) in a classical computer, optimize the set of parameters to find a better set \( \theta' = \{\theta'_1, \theta'_2, \ldots, \theta'_k\} \) such that it minimizes (or maximizes) the objective function; (iv) repeat steps (ii) and (iii) with the new set of parameters until convergence.

Quantum Approximate Optimization Algorithm (QAOA) is a type of VQA that focuses on finding good approximate solutions to combinatorial optimization problems. It has been studied most widely for finding the maximum cut of a (weighted or unweighted) graph (called the Max-Cut problem) [2]. For this problem, given a graph \( G = (V, E) \) where \( V \) is the set of vertices and \( E \) is the set of edges, the objective is to partition \( V = V_1 \cup V_2 \), such that \( V_1 \cap V_2 = \phi \), and the number of edges crossing the partition is maximized. Throughout this paper, we shall consider connected graphs with \( |V| = n \) and \( |E| = m \), but
the results can be easily extended to disconnected graphs as well.

In the initial algorithm proposed by Farhi [2] for the Max-Cut problem, a depth-$p$ QAOA consists of $p \geq 1$ layers of alternating operators on the initial state $|\psi_0\rangle$

$$|\psi(\gamma, \beta)\rangle = (\prod_{l=1}^{p} e^{(-i\beta_l H_M)} e^{(-i\gamma_l H_P)}) |\psi_0\rangle$$  \hspace{1cm} (1)

where $H_P$ and $H_M$ are called the Problem and Mixer Hamiltonian respectively, and $\gamma = \{\gamma_1, \gamma_2, \ldots, \gamma_p\}$ and $\beta = \{\beta_1, \beta_2, \ldots, \beta_p\}$ are the parameters. It is to be noted that the depth $p$ of the QAOA is not related to the depth of the quantum circuit realizing the algorithm. The problem Hamiltonian describing the Max-Cut can be represented as in Eq. (2), where $w_{jk}$ is the weight associated with the edge $(j, k)$.

$$H_P = \frac{1}{2} \sum_{(j,k) \in E} w_{jk}(I - Z_j Z_k)$$  \hspace{1cm} (2)

Furthermore, the mixer Hamiltonian should be an operator that does not commute with the Problem Hamiltonian. In the traditional QAOA, the mixer Hamiltonian is $H_M = \sum_i X_i$.

Variations to this have been studied to improve the performance of the algorithm — such as using other mixers [11, 12, ?], training the parameters to reduce the classical optimization cost [13], and modifying the cost function for faster convergence [14]. In this paper we stick to the original problem and mixer Hamiltonians proposed in the algorithm by Farhi et al. [2]. The applicability and effectiveness of our proposed method on the modifications of this algorithm can be looked at as a follow-up work. However, our proposed methods optimize the circuit corresponding to the problem Hamiltonian. Since most of the modifications suggested in the literature aim to design more efficient mixers, our proposed optimization should be applicable on those as well.

The realization of the QAOA circuit for Max-cut requires two CNOT gates for each edge (details given in Sec. 2). Hardware realization of a CNOT gate is, in general, significantly more erroneous than a single qubit gate. Even in the higher end devices of IBM Quantum, such as ibmq_montreal, ibmq_manhattan, the probability of error for a single qubit gate and a CNOT gate are $O(10^{-4})$ and $O(10^{-2})$, respectively [1]. In other words, CNOT gates are 100 times more likely to be erroneous than single qubit gates. Therefore, we focus primarily on reducing the number of CNOT gates in the design of QAOA ansatz for Max-cut.

Contributions of this paper

In this paper, we

(i) propose two optimization methods for reducing the number of CNOT gates in the first layer of the QAOA ansatz based on (1) an Edge Coloring that can reduce upto $\left\lfloor \frac{n}{2} \right\rfloor$ CNOT gates, and (2) a Depth First Search (DFS) that can reduce $n - 1$ CNOT gates.

(ii) prove that there exists no method that can reduce more than $n - 1$ CNOT gates while still maintaining a fidelity of 1 with the original QAOA ansatz [2].

(iii) show that while the Edge Coloring based optimization reduces the depth of the circuit, the DFS based method may increase the depth. We further analytically derive the criteria (involving the increase in the depth and the reduction in the number of CNOT gates) for which the DFS based optimization method still leads to a lower probability of error in the circuit, and show that the IBM Quantum Hardwares [1] conform to that criteria.

(iv) simulate our proposed optimization methods in Qiskit [15] with the ibmq_manhattan noise model and show that for graphs of different sparsity (Erdos-Renyi graphs with the probability of edge varying from 0.4 - 1)

(a) the proposed reduction in the CNOT gate is still retained post transpilation

(b) the DFS based method has lower error probability than the Edge Coloring method, which in its turn has lower error probability than the traditional QAOA ansatz.

Therefore, for any graph $G = (V, E)$, our proposed method provides reduction in the number of CNOT gates, and hence lowers the error probability of the circuit. Although the DFS method provably surpasses the Edge Coloring method, both in terms of reduction in CNOT gates and
In QAOA, the circuit is implemented. Note that the gates acting simultaneously on all the qubits.

Each layer of QAOA contains the operator \( \exp \{ -i \gamma P \} \) that prepares an equal superposition of states. The initial state \(| \psi_0 \rangle\) is usually the equal superposition of \(n\) qubits, where \(n = |V|\). The circuit of the QAOA ansatz has a fixed form as described in Eq. (1). The initial state \(| \psi_0 \rangle\) is prepared by applying Hadamard gates acting simultaneously on all the qubits.

The objective function of a depth-\(p\) QAOA for Max-Cut [2] can be expressed as

\[
\max_{\psi(\gamma, \beta)} \langle \psi(\gamma, \beta) | H_P | \psi(\gamma, \beta) \rangle
\]

where \(\gamma = \{ \gamma_1, \gamma_2, \ldots, \gamma_p \}\) and \(\beta = \{ \beta_1, \beta_2, \ldots, \beta_p \}\) are the parameters. The trial wavefunction \(| \psi(\gamma, \beta) \rangle\) is called the ansatz.

The QAOA ansatz has a fixed form as described in Eq. (1). The initial state \(| \psi_0 \rangle\) is usually the equal superposition of \(n\) qubits, where \(n = |V|\). Note that the depth of the circuit required to prepare \(| \psi_0 \rangle\) is \(1\) (Hadamard gates acting simultaneously on all the qubits). Similarly, for each layer of QAOA, the operator \(\exp(-i \beta_l H_M)\) can be realized by a depth one circuit of \(R_z(\beta_l)\) gates acting simultaneously on all the qubits.

The operator \(\exp(-i \gamma H_P)\) has a more costly implementation. Note that

\[
\exp(-i \gamma H_P) = \prod_{(i,j) \in E} \exp \left( -i \gamma l \left( \frac{I - Z_j Z_k}{2} \right) \right).
\]

The operator \(\exp \left( -i \gamma l \left( \frac{I - Z_j Z_k}{2} \right) \right)\) acts on each edge \((j, k)\), and is realized as shown below:

Here, \(q_j\) and \(q_k\) represent qubit indices \(j\) and \(k\), respectively. Note that Max-Cut is a symmetric problem, and therefore, the selection of control and target from qubits \(q_j\) and \(q_k\) for the CNOT gate corresponding to the edge \((j, k)\) is irrelevant, i.e. the operator \(\exp \left( -i \gamma l \left( \frac{I - Z_j Z_k}{2} \right) \right)\) can be equivalently realized as \(CNOT_{kj} (I_k \otimes R_z(2\gamma l)_{j})\) \(CNOT_{kj}\). In Fig. 1(a) and (b), we show a 2-regular graph with four vertices and its corresponding QAOA circuit for \(p = 1\) respectively.

![Figure 1: The Max-Cut QAOA circuit for \(p = 1\) corresponding to the graph](image)

Figure 1: The Max-Cut QAOA circuit for \(p = 1\) corresponding to the 2-regular graph with four vertices; the values of \(\gamma\) and \(\beta\) can be arbitrary but those in this figure are the optimum values for this graph when \(p = 1\).

### 3 Methods for Optimized ansatz design

Some recent studies have proposed optimization methods for the circuit of the QAOA ansatz with respect to the underlying hardware architecture [17]. In this paper we propose two hardware independent methods to reduce the number of CNOT gates in the traditional QAOA ansatz. The intuition is that in the circuit realization of the operator \(\exp \left( -i \gamma l \left( \frac{I - Z_j Z_k}{2} \right) \right)\) as \(CNOT_{jk} (I_j \otimes \ldots \otimes \ldots)\).
\[ R_z(2\gamma_k) \text{ CNOT}_{jk}, \] the first CNOT gate can be removed whenever it does not make any contribution to the overall effect of the operator. Our proposed method reduces the number of CNOT gates in the circuit irrespective of the hardware architecture, and hence is applicable for any quantum device.

In Theorem 1 we prescribe the condition where the first CNOT gate is irrelevant to the effect of the said operator, and hence may be removed.

**Theorem 1.** Let \( |\psi\rangle \) be an \( n \)-qubit state prepared in a uniform superposition (upto relative phase) over all basis states \( |x_1, \ldots, x_n\rangle \) such that the relative phase on each basis state is a function of a subset \( S \subset \{1, 2, \ldots, n\} \) of the \( n \) qubits (and independent of remaining qubits) i.e.

\[
|\psi\rangle = \frac{1}{\sqrt{2^n}} \sum_{x_1, \ldots, x_n} e^{i\phi(x_S)} |x_1, \ldots, x_n\rangle
\]

where \( x_S = \{x_i : i \in S\} \) and \( \phi(x_S) \) depicts the relative phase of each superposition state. For any two qubits \( |j\rangle \) and \( |k\rangle \), where \( |k\rangle \notin S \) and for the two operators \( U_1 = \text{CNOT}_{jk} (I_j \otimes R_z(2\gamma_k)) \text{ CNOT}_{jk} \) and \( U_2 = (I_j \otimes R_z(2\gamma_k)) \text{ CNOT}_{jk} \), we have

\[
U_1 |\psi\rangle = U_2 |\psi\rangle.
\]

**Proof.** Let us consider the action of the operators \( U_1 \) and \( U_2 \) on any edge \( (j, k) \).

\[
U_1 |\psi\rangle = \text{CNOT}_{jk} (I_j \otimes R_z(2\gamma_k)) (\text{CNOT}_{jk}) |\psi\rangle
\]

\[
= \sum_{x_1, \ldots, x_n} \text{CNOT}_{jk} (I_j \otimes R_z(2\gamma_k)) (\text{CNOT}_{jk}) e^{i\phi(x_S)} |x_1, \ldots, x_n\rangle
\]

\[
= \sum_{x_1, \ldots, x_n} \text{CNOT}_{jk} (I_j \otimes R_z(2\gamma_k)) e^{i\phi(x_S)} |x_1, x'_k = x_j \oplus x_k, \ldots, x_n\rangle
\]

\[
= \sum_{x_1, \ldots, x_n} e^{i\phi(x_S) - \gamma(x_j \oplus x_k)} \text{CNOT}_{jk} |x_1, \ldots, x_n\rangle
\]

where \( e^{i\phi(x_S)} \) is the cumulative effect of operators acting on previous edges (= 0 if \( (j, k) \) is the first).

We have dropped the normalization constant for brevity.

Similarly,

\[
U_2 |\psi\rangle = \text{CNOT}_{jk} (I_j \otimes R_z(2\gamma_k)) |\psi\rangle
\]

\[
= \text{CNOT}_{jk} \sum_{x_1, \ldots, x_n} e^{i((\phi(x_S)) - \gamma x_k)} |x_1, \ldots, x_n\rangle
\]

\[
= \sum_{x_1, \ldots, x_n} e^{i((\phi(x_S)) - \gamma x_k)} |x_1, \ldots, x_j \oplus x_k, \ldots, x_n\rangle
\]

where the qubit in \( k^{th} \) position changes to \( x_j \oplus x_k \) due to the \( \text{CNOT}_{jk} \) operation. Now, substituting \( x'_k = x_j \oplus x_k \) in the above equation, we get

\[
U_2 |\psi\rangle = \sum_{x_1, \ldots, x_n} e^{i((\phi(x_S)) - \gamma x_k)} |x_1, \ldots, x_j \oplus x_k, \ldots, x_n\rangle
\]

\[
= \sum_{x_1, \ldots, x'_k, \ldots, x_n} e^{i((\phi(x_S)) - \gamma (x_j \oplus x'_k))} |x_1, \ldots, x'_k, \ldots, x_n\rangle
\]

\[
= \sum_{x_1, \ldots, x_k, \ldots, x_n} e^{i((\phi(x_S)) - \gamma (x_j \oplus x_k))} |x_1, \ldots, x_k, \ldots, x_n\rangle
\]

(9)

Here since \( k \notin S \), the substitution in second last step, does not change the phase \( e^{i\phi(x_S)} \). The last step is valid since \( x'_k \) is a running index and hence can be changed to \( x_k \). Thus Eq. (7) and Eq. (9) are identical.

**Corollary 1.1.** For a graph \( G \), we can optimize the circuit for the operator \( \exp (-i \gamma \left( \frac{1-Z_j Z_k}{2} \right)) \) corresponding to an edge \( (j, k) \) replacing \( U_1 \) by \( U_2 \), provided that the target vertex does not occur in any of the edge operators run earlier. In other words, the following conditions are sufficient to optimize an edge:-

1. if the vertex \( j \) is being operated on for the first time, then it acts either as a control or a target for the \( \text{CNOT} \) gate corresponding to the operator;

2. the vertex \( j \) does not act as a target of the \( \text{CNOT} \) gate if it occurs as a part of any other edge operators run earlier.

**Proof.** The first time we consider an edge adjacent to a vertex \( j \), where \( j \notin S \), (see Theorem 1) the relative phase \( \phi(x_S) \) does not depend on \( j \). Thus it satisfies the condition of Theorem 1 and allows optimization of the operator.

On the other hand, if the vertex \( j \) occurs as part of an edge operator already run, the phase on the basis state \( \phi \) can potentially depend on \( S \), i.e. \( j \in S \). By not allowing it to act as target, we satisfy the conditions of Theorem 1.
From the above discussion, it follows that if we arbitrarily choose edges for applying the operator $$\exp \left( -i\gamma \left( \frac{1-Z_uZ_v}{2} \right) \right)$$, then it cannot be guaranteed that a large number of edges will conform to Corollary 1.1. The requirement, in fact, imposes a precedence ordering among the edges. In Section 4 and 5, we provide two algorithmic procedures for maximizing the number of edges that satisfy the requirement in order to reduce the number of CNOT gates in the ansatz.

For the rest of the paper, we say that an edge is optimized if the operator $$U_2$$ can be operated on that edge instead of $$U_1$$.

4 Edge Coloring based Ansatz Optimization

The total error one incurs in a circuit depends on the number of operators (since a larger number of operators tend to incur more error) and the depth of the circuit (corresponding to relaxation error). In this section, we discuss how one can minimize the depth of the circuit. We also discuss the possibility of reduction in CNOT gates in the depth optimized circuit.

The operators $$H_M$$ act on distinct qubits and hence can be run in parallel contributing to a depth of 1 (for each step of the QAOA). On the other hand, the operators in $$H_P$$ can potentially contribute a lot to depth since the edge operators do not act on disjoint vertices. At a given level of the circuit, we can only apply edge operators corresponding to a vertex disjoint set of edges. Thus the minimum depth of the circuit will correspond to the minimum value $$k$$ such that we can partition the set of edges $$E$$ as a disjoint union $$\cup_i E_i$$ where each subset $$E_i$$ consists of a vertex disjoint collection of edges. This in turn corresponds to the edge coloring problem in a graph.

Given a graph $$G = (V, E)$$ and a set of colors $$\chi' = \{\chi'_1, \chi'_2, \ldots, \chi'_{\chi'}\}$$, an edge coloring [18] assigns a color to each edge $$e \in E$$, such that any two adjacent edges (i.e., edges incident on a common vertex) must be assigned distinct colors. The edge coloring problem comprises of coloring the edges using the minimum number of colors $$k$$. Note that the operators corresponding to edges having the same color can be executed in parallel. Moreover,

1. the number of colors in optimal coloring, called the chromatic index, corresponds to the minimum depth of the circuit;
2. edges having the same color corresponds to the operators $$\exp \left( -i\gamma \left( \frac{1-Z_vZ_u}{2} \right) \right)$$ that can be executed simultaneously.

Optimal edge coloring is an NP-complete problem [18]. But it is not practical to allocate exponential time to find the optimal edge-coloring as a pre-processing step for QAOA. Vizing’s Theorem states that every simple undirected graph can be edge-colored using at most $$\Delta + 1$$ colors, where $$\Delta$$ is the maximum degree of the graph [19]. This is within an additive factor of 1 since any edge-coloring must use at least $$\Delta$$ colors. Misra and Gries algorithm [20] achieves the above bound constructively in $$O(n \cdot m)$$ time. Therefore, we use the Misra and Gries edge coloring algorithm. Algorithm 1 below computes the sets of edges having the same color using Misra and Gries algorithm as a subroutine. It returns the largest set $$S_{\text{max}}$$ of edges having the same color in the coloring computed by Misra and Gries algorithm.

**Algorithm 1 Edge Coloring based Ansatz Optimization**

**Input:** A graph $$G = (V, E)$$.  
**Output:** Largest set $$S_{\text{max}}$$ of edges having the same color.

1. Use the Misra and Gries algorithm to color the edges of the graph $$G$$.
2. $$S_i \leftarrow$$ set of edges having the same color $$i, 1 \leq i \leq \chi'$$.
3. $$S_{\text{max}} \leftarrow \max \{S_1, S_2, \ldots, S_{\chi'}\}$$.
4. Return $$S_{\text{max}}$$.

This edge coloring approach provides the minimum depth achievable for QAOA ansatz using a polynomial time pre-processing. After reducing the depth, we now try to further reduce errors by decreasing the number of CNOT gates. Recall that the operators corresponding to edges with the same color can be executed in parallel. We use the operators corresponding to the edges of $$S_{\text{max}}$$ as the first layer of operators. The other layers can be used in any order.

**Lemma 2.** Every edge in the first layer can be optimized according to Corollary 1.1.

**Proof.** For every edge $$(u, v)$$ in the first layer, both the vertices are adjacent to an edge for the
first time, i.e., both \( u, v \notin S \). Therefore, it satisfies the criteria of Corollary 1.1, and hence can be optimized. In fact, any one of the qubits corresponding to the two vertices can be selected as the control for the CNOT operation.

Some edges in the corresponding layers may be optimized as well. Nevertheless, it is trivial to come up with examples where this is not the case (e.g., a complete graph of 4-vertices). Therefore, in the worst case scenario, only the edges in the first layer can be optimized. However, since this method does not increase the depth of the circuit, it always leads to a more efficient circuit design than the traditional QAOA circuit with lower depth (by 1 since the first layer of CNOT is absent) and fewer CNOT gates.

For general graphs, the worst case scenario is, therefore, that only the edges in the first layer can be optimized. In the following subsection we provide an analysis on the number of optimized edges using this method.

4.1 Lower and upper bound on the number of optimized edges

Let us assume that the chromatic index of a graph \( G = (V, E) \) is \( \chi' \). Using the Misra and Gries Theorem [20] we can find a polynomial time coloring using at most \( \Delta + 1 \) colors, where \( \Delta \) is the maximum degree of the graph. Therefore, on an average, \( \left\lceil \frac{m}{\Delta+1} \right\rceil \) edges have the same color.

More precisely, two extreme cases arise: (i) the colors may be uniformly distributed, and the maximum number of edges having the same color is \( \left\lceil \frac{m}{\Delta+1} \right\rceil \); or (ii) one of the colors is used dominantly for most of the edges. Nevertheless, note that for all the edges adjacent to the same vertex, a particular color can be assigned to one of the edges only. Therefore, the dominant color can be used at most on \( \left\lceil \frac{n}{2} \right\rceil \) edges, where \( n = |V| \). Therefore, the possible number of optimized edges that can be obtained via the Edge Coloring method is as shown in Eq. (10).

\[
\left\lceil \frac{m}{\Delta+1} \right\rceil \leq \# \text{Optimized Edges} \leq \left\lceil \frac{n}{2} \right\rceil. \tag{10}
\]

5 Depth First Search based Ansatz Optimization

As the edge coloring based algorithm can optimize at most \( \left\lceil \frac{n}{2} \right\rceil \) edges, in this section, we present a Depth First Search (DFS) based optimization procedure which can optimize \( n - 1 \) edges. Algorithm 2, for obtaining the optimized QAOA ansatz, uses the standard DFS algorithm [21], by returning the tree edges or discovery edges forming the DFS tree.

In this method, we start from the first vertex of the DFS tree. For every edge \( e = (u, v) \) in the DFS tree, the vertex \( u \) is made the control and \( v \) is made the target for the CNOT gate corresponding to that edge. The edges are operated on sequentially one after another, as in the set \( E_{dfs} \) (the tree edges). Once every edge in the DFS tree has been operated on, the remaining edges can be executed in any order. In fact, one may opt to use the Edge Coloring method on the remaining edges to obtain the minimum depth of the circuit corresponding to these edges, although CNOT gates cannot be reduced any further.

**Algorithm 2 DFS based Ansatz Optimization**

**Input:** A graph \( G = (V, E) \).

**Output:** A list \( E_{dfs} \) of \( n - 1 \) edges.

1: \( E_{dfs} = \{\} \)
2: \( u \leftarrow \) randomly selected vertex from \( V \).
3: Start DFS from the vertex \( u \). For every vertex \( v \) discovered from its predecessor \( v' \),

\[ E_{dfs} = E_{dfs} \cup (v', v). \]
4: Return \( E_{dfs} \).

**Theorem 3.** Each edge in the DFS tree can be optimized according to Corollary 1.1.

**Proof.** We prove this by the method of induction. Let \( u \) be the vertex from which the DFS tree starts. Then \( u \) is being operated on for the first time, and, hence, can act both as a control/target for the CNOT operation corresponding to the first edge (Corollary 1.1). Choose \( u \) to be the control.

**Base case:** If \( v \) is the vertex that is discovered from \( u \) via the edge \((u, v)\), then choosing \( u \) as the control and \( v \) as the target satisfies Corollary 1.1. Therefore, the edge \((u, v)\) can be optimized.

**Induction hypothesis:** Let the DFS tree has been constructed upto some vertex \( j \), and every edge \((e_1, e_2)\) in this DFS tree so far can be optimized, i.e. \( e_1 \) acts as the control and \( e_2 \) as the target.

**Induction step:** Let the next vertex in the DFS tree, that is discovered from some vertex \( i \), is \( k \). From DFS algorithm, the vertex \( i \) must have
been discovered in some previous step. Since vertex \( k \) was not previously discovered, so \( k \notin x_S \) and hence the edge \((i,k)\) can be optimized if we select \( i \) to be the control and \( k \) as the target. ■

Therefore, the DFS based optimization method provides \( n - 1 \) optimized edges, \( i.e. \), a reduction in the number of CNOT gates by \( n - 1 \). We now show in Theorem 4 that this is the maximum number of edges that can be optimized.

Therefore, the DFS method is optimal in the number of optimized edges. However, we note that the DFS based method associates an ordering of the edges, \( i.e. \), some of the edges which could have been operated on simultaneously, cannot be done so now. This, in turn, can lead to an increase in the depth of the circuit. Hence, a penalty for this method producing optimal reduction in CNOT gates, is that it increases the depth of the circuit.

![Figure 2: Depth of the ansatz circuit when using (a) Edge Coloring and (b) DFS based method; edges having same color can be executed simultaneously. The depth of the spanning tree in the DFS based method is 4, compared to depth 2 for the Edge Coloring based method. However, the number of optimized edges in the Edge Coloring based method is 2, while that by the DFS based method is 3.](image)

**Theorem 4.** Optimization of ansatz for Max-Cut QAOA with \( p=1 \), by deletion of the CNOT gate in the first level for an edge of the graph, can be done for no more than \( n - 1 \) edges.

**Proof.** Let us assume that there is some method by which at least \( n \) edges can be optimized. Now, the connected subgraph which contains all the \( n \) vertices and at least \( n \) optimized edges must contain a cycle. Let \((u,v)\) be an edge of this cycle, \( i.e. \), if \((u,v)\) is removed then the residual graph is a tree (in case there are \( > n \) edges, the removal of edges can be performed recursively till such an edge \((u,v)\) is obtained whose removal makes the residual graph a tree). For this edge \((u,v)\), both the vertices \( u \) and \( v \) must act as the control for the CNOT gate corresponding to the edge \((u,v)\) in order for this edge to be optimized, which is not possible. Therefore, it is not possible to optimize more than \( n - 1 \) edges. ■

![Figure 3: Max-Cut QAOA ansatz with \( p = 1 \) corresponding to (a) Edge Coloring and (b) DFS based optimization. In (a), the first CNOT gates of the operators have been deleted. The operators corresponding to \((q_1,q_2)\) and \((q_3,q_4)\) act in parallel. In (b), the first CNOT gates of three operators have been deleted, but the depth has increased.](image)

In Fig. 2, we show a 2-regular graph with four vertices. In Fig. 2(a), the depth of the circuit corresponding to the operator \( \exp(-i\gamma L P) \) is 2; the edges of the same color can be operated on simultaneously. If the red (or blue) edges form the first layer, then those two edges are optimized. However, if we use the DFS method, with the DFS tree starting from, say, vertex 1, then...
the edges (1, 2), (2, 3) and (3, 4) can be optimized (Fig. 2(b)). Now these three edges must be operated on one after another, followed by the fourth edge. Thus the depth of the circuit corresponding to the operator $\exp(-i\gamma H_F)$ becomes 4. The circuits corresponding to these two scenarios are depicted in Fig 3(a) and (b) respectively.

The question, therefore, is whether this increase in depth is always acceptable, even with the increased reduction in the number of CNOT gates as, with increased depth, the circuit becomes more prone to relaxation error. Numerical analysis and simulation (Section 6) establishes that although the depth of the circuit is increased, the overall error probability of the circuit is reduced further.

5.1 When is the DFS based method useful?

In this subsection, we formulate a relation for which the increase in the depth still leads to a lower probability of error for the reduction in the number of CNOT gates. For this analysis, we make an assumption that the error in the circuit arises only from noisy CNOT gates and the depth of the circuit (i.e., the $T_1$ time). Although this assumption is idealistic, the ansatz primarily consists of layers of CNOT gates. Furthermore, in superconductors, $R_z$ gates are executed virtually [?], and hence does not lead to any gate error. Therefore, CNOT is the primary source of gate error and with increasing depth, the qubits become more prone to relaxation error. Therefore, this assumption allows for a simple but powerful model for analyzing the query at hand.

Let us assume that the time duration and the error probability of each CNOT gate is $t_{cx}$ and $p_{cx}$ respectively. Let there be $N$ layers of CNOT operations. Note that although there can be multiple CNOT gates in each layer, the time duration of each layer is $t_{cx}$ only. Therefore, the probability of no error (i.e., the probability that the circuit remains error free) after $N$ layers of operations, considering only relaxation error, is $\exp(-\frac{N t_{cx}}{T_1})$.

Let there be $k$ CNOT gates in the original circuit. Therefore, the probability of no error after the operation of the CNOT gates, considering only CNOT gate error, is $(1 - p_{cx})^k$.

Combining both the sources of the errors, Eq. (11) gives the probability of success (i.e., the probability of no error) after a single cycle of computation of the QAOA ansatz.

$$P_{\text{success}} = (1 - p_{cx})^k \cdot \exp\left(-\frac{N t_{cx}}{T_1}\right) \quad (11)$$

Henceforth, $P_{\text{success}}$ will refer to the probability of success (i.e., how close the noisy outcome is to the noise-free ideal outcome) of the ansatz circuit execution for a single run of the algorithm. Note that in QAOA, the ansatz is computed multiple times for multiple cycles, and the objective is to maximize the expectation value of the outcome.

We further assume that after the optimization using DFS-based method, $k_1$ CNOT gates have been reduced leading to an increase in $N_1$ layers of operations. The probability that this optimized circuit remains error-free is given in Eq. (12).

$$P_{\text{success}}^{\text{opt}} = (1 - p_{cx})^{(k-k_1)} \cdot \exp\left(-\frac{(N + N_1) t_{cx}}{T_1}\right) \quad (12)$$

The optimization is fruitful only when $P_{\text{success}}^{\text{opt}} \geq P_{\text{success}}$. Note that $P_{\text{success}}^{\text{opt}} = P_{\text{success}} \cdot \exp\left(-\frac{N t_{cx}}{T_1}\right) / (1 - p_{cx})^{k_1}$.

Since both $P_{\text{success}}^{\text{opt}}$ and $P_{\text{success}} \leq 1$, the required inequality holds only if $\exp\left(-\frac{N_1 t_{cx}}{T_1}\right) / (1 - p_{cx})^{k_1} \geq 1$. In other words,

$$\exp\left(-\frac{N t_{cx}}{T_1}\right) \geq (1 - p_{cx})^{k_1}$$

$$\Rightarrow N_1 \leq \lambda \times k_1,$$

**where**

$$\lambda = \frac{-\ln(1 - p_{cx}) \cdot T_1}{t_{cx}}. \quad (13)$$

The constant $\lambda$ is defined in terms of parameters specific to the quantum device.

5.1.1 Effect of varying $\lambda$ Given that $\lambda = f(t_{cx}, p_{cx}, T_1)$, we expect the $T_1$ value to increase, and the $t_{cx}$ and $p_{cx}$ values to decrease as technology improves. The value of $\lambda$ increases for increasing $T_1$ and/or decreasing $t_{cx}$, whereas it decreases for decreasing $p_{cx}$. Therefore,

- If $p_{cx}$, the probability of error for CNOT gates decreases, the optimization becomes less useful since we are increasing the probability of relaxation error, but the reduction in error probability becomes less. According to this observation, for smaller $\lambda$, Eq. (13) is satisfied when the increase in depth is reduced as well.
Similarly, if (i) $T_1$ increases, then the qubit can retain its coherence for a longer period of time, or (ii) $t_{cx}$ decreases, then the overall computation time of the circuit decreases as well, and the circuit can allow some relaxation in the depth even if $T_1$ remains unchanged. We observe that for both of these cases, by Eq. (13), $\lambda$ increases, thus allowing more increase in depth for a given reduction in the number of CNOT gates.

5.2 Trade-off between depth and reduction in CNOT gates

If the DFS based method is not applied, then the number of layers of CNOT gates is equal to the number of color classes (as in Edge Coloring method). The maximum number of color classes is $\Delta + 1$ (as discussed in the previous section), and hence the maximum depth of the circuit is $\Delta + 1$ as well. Now, when the DFS based method is applied, the circuit can be divided into two disjoint sets of edges:

1. The set of edges belonging to the DFS tree which can be optimized. The depth of this portion of the circuit is at most $n-1$ (i.e., the depth of the DFS tree). Each of the operators corresponding to these edges contains a single CNOT gate only, and hence the number of CNOT gate layers is $n-1$ as well.

2. The set of edges that do not belong to the DFS tree and hence are not optimized. The operators corresponding to these edges can be applied in any order, but after all the optimized edges. When removing the edges of the DFS tree, the degree of each vertex is reduced by at least 1. Therefore, the maximum degree of the remaining subgraph is at most $\Delta - 1$. Therefore, the depth of this portion of the circuit will be at most $\Delta$ (From Misra and Gries Algorithm). Each of the layer in this portion contains 2 CNOT gates, and hence the number of CNOT gate layers is $2\Delta$.

Therefore, the maximum depth of the circuit after applying the DFS based optimization is $n - 1 + \Delta$. In other words, the increase in depth due to this method is given by Eq. (14).

$$n - 1 + \Delta - (\Delta + 1) = n - 2 \quad (14)$$

Recall that the number of CNOT gates reduced due to the DFS method is always $n-1$. Therefore, from Eq. (13) and (14), we get

$$n - 2 \leq \lambda \cdot (n - 1)$$

$$\Rightarrow \lambda \geq \frac{n - 2}{n - 1} \quad (15)$$

In Table 1 we show the average value of $\lambda$ for some IBM Quantum [1] devices, ranging from the comparatively more noisy ibmq_melbourne to the comparatively less noisy ibmq_manhattan.

Table 1: Average value of $\lambda$ for four IBM Quantum machines [1]

| IBM Quantum devices | Avg value of $\lambda$ |
|---------------------|------------------------|
| ibmq_manhattan      | 3.6                    |
| ibmq_montreal       | 2.47                   |
| ibmq_sydney         | 3.35                   |
| ibmq_melbourne      | 2.03                   |

Note that the lower bound on $\lambda$, $\frac{n - 2}{n - 1}$ (Eq. (15), is always less than 1 for all $n$. In the asymptotic limit, $\frac{n - 2}{n - 1} \rightarrow 1$. Thus, the proposed DFS based optimization method leads to a lower error probability on any quantum device for which $\lambda \geq 1$. Table 1 readily shows that the IBM Quantum hardwares conform to this requirement.

6 Results of simulation

In this section we show the effect of our optimization methods on reducing the probability of error and the CNOT count of QAOA for MaxCut. We first show that our proposed reduction is retained in the post transpilation circuit, which is executed on the quantum hardware. Next, we run our simulation with the noise model for ibmq_manhattan from IBM Quantum; this noise model corresponds to the actual noise in the IBM Quantum Manhattan device which has 65 qubits and a Quantum Volume of 32 [1]. For our simulation purpose, we have considered Erdos-Renyi graphs, where the probability that an edge exists between two vertices, $p_{\text{edge}}$, varies respectively from 0.4 to 1 (complete graph). The choice of Erdos-Renyi graph allows us to study the performance of these proposed methods for various sparsity of graphs.

The circuit that we construct is usually not executed as it is in the IBM Quantum hardware. It undergoes a process called transpilation in which
The gates of the circuit are replaced with one, or a sequence of, basis gates which are actually executed in the quantum hardware. The basis gates of the IBM Quantum devices are \{CNOT, SX, X, R_z and Identity\} [1], (ii) the circuit is mapped to the underlying connectivity (called the coupling map) of the hardware [22], (iii) the number of gates in the circuit is reduced using logical equivalence [23].

A natural question, therefore, is whether the reduction in CNOT gates is retained post transpilation. In Table 2 we show the number of CNOT gates in the post transpilation circuit for the ibmq_manhattan device as the number of vertices is varied from 10 – 60 for each of the graph family considered. Our results readily show that the proposed optimization in the number of CNOT gates still hold good even in the transpiled circuit. Since the ibmq_manhattan device is a 65-qubits device, we show the results upto 60 qubits, but the results show that the trend will continue for higher qubit devices as well, when they become available.

Let \( |\psi\rangle \) be the state obtained from the noise-free (ideal) computation of the QAOA circuit, and the state obtained from noisy computation be \( |\psi_e\rangle \). The probability of success of the noisy computation, then, is defined as

\[
P_{\text{succ}} = |\langle \psi | \psi_e \rangle|^2 \tag{16}
\]

In Fig. 4(a) - (d) we plot \( P_{\text{succ}} \) of the traditional QAOA ansatz, Edge Coloring based and
the DFS based optimization method for Erdos-Renyi graphs, where $p_{\text{edge}}$, the probability that an edge exists between two vertices, varies from 0.4 to 1 (complete graph). The choice of Erdos-Renyi graph allows us to study the performance of these proposed methods for various sparsity of graphs. For each case we vary the number of vertices $n$ from 4 to 12. For each value of $n$ and $p_{\text{edge}}$, the results are averaged over 20 input graph instances, and each instance is an average of 100 randomly generated noisy circuits by the simulator model for ibmq_manhattan with noise. Our results readily show that the DFS based optimization outperforms both the Edge Coloring based method and the traditional QAOA in terms of lower error probability.

From Table 2, and our simulation results in Fig. 4(a)-(d), we can infer that the DFS based optimization outperforms the Edge Coloring based optimization, which again, outperforms the traditional QAOA in the reduction in CNOT count, and the probability of error in the circuit in (i) the actual transpiled circuit that is executed on the quantum devices, as well as (ii) in realistic noisy scenario of quantum devices.

7 Conclusion

In this paper we have proposed two methods to reduce the number of CNOT gates in the traditional QAOA ansatz. The Edge Coloring based method can reduce up to $\lfloor \frac{n}{2} \rfloor$ CNOT gates whereas the DFS based method can reduce $n - 1$ CNOT gates. While the former method provides a depth-optimized circuit, the latter method can increase the depth of the circuit. We analytically derive the constraint for which a particular increase in depth is acceptable given the number of CNOT gates reduced, and show that every
graph satisfies this constraint. Therefore, these methods can reduce the number of CNOT gates in the QAOA ansatz for any graph. Finally, we show via simulation, with the ibmq_manhattan noise model, that the DFS based method outperforms the Edge Coloring based method, which in its turn, outperforms the traditional QAOA in terms of lower error probability in the circuit. The transpiler procedure of Qiskit maps a circuit to the underlying hardware connectivity graph, and some gates are reduced in this process. This transpiled circuit is executed on the real hardware. We show, with the ibmq_manhattan coupling map, that the reduction in the number of CNOT gates still holds post transpilation. Therefore, our proposed methods provide a universal way to an improved QAOA ansatz design. On a final note, all the calculations in this paper considers connected graph, but these carry over easily to disconnected graphs as well.

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Code Availability

A notebook providing the code to generate the plots of Fig. 4(a)-(d) is available open source at https://github.com/RitajitMajumdar/Optimizing-Ansatza-Design-in-QAOA-for-Max-cut.

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