Memristive control of mutual SHNO synchronization for neuromorphic computing

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Synchronization of large spin Hall nano-oscillators (SHNO) arrays is an appealing approach toward ultra-fast non-conventional computing based on nanoscale coupled oscillator networks. However, for large arrays, interfacing to the network, tuning its individual oscillators, their coupling, and providing built-in memory units for training purposes, remain substantial challenges. Here, we address all these challenges using memristive gating of W/CoFeB/MgO/AlO$_x$ based SHNOs. In its high resistance state (HRS), the memristor modulates the perpendicular magnetic anisotropy (PMA) at the CoFeB/MgO interface purely by the applied electric field. In its low resistance state (LRS), and depending on the voltage polarity, the memristor adds/subtracts current to/from the SHNO drive. The operation in both the HRS and LRS affects the SHNO auto-oscillation mode and frequency, which can be tuned up to 28 MHz/V. This tuning allows us to reversibly turn on/off mutual synchronization in chains of four SHNOs. We also demonstrate two individually controlled memristors to tailor both the coupling strength and the frequency of the synchronized state. Memristor gating is therefore an efficient approach to input, tune, and store the state of the SHNO array for any non-conventional computing paradigm, all in one platform.

Introduction

The demand for compact communication systems and faster processing hardware is booming as we approach the era of the Internet of Things (IoT). However, with the approaching end of Moore’s law and the increasing demand for mobile applications, it seems unlikely that state-of-the-art CMOS technologies can live up to all IoT expectations. Emerging paradigms—such as machine vision
and cognitive tasks for connected objects—have severely challenged the existing technologies in terms of power consumption and processing speed, tasks that the human brain, thanks to its massive neuronal connectivity, performs extremely fast using negligible power compared to conventional processors.² Although there have been efforts to imitate the neuronal connectivity by involving many transistors representing individual neurons, Von–Neumann computing inherently does not include connected and interactive computing elements.³ Numerous types of unconventional computing hardware have been proposed by different research communities to address such von–Neumann shortcomings, each outperforming CMOS processors in some aspects: Memristive computing⁴⁵, optical computing⁶–⁸, spintronic computing⁹¹², and quantum computing¹³¹⁴ are only a few examples of such hardware.

Using coupled networks of oscillators as an alternative computing paradigm has been proposed since many different technologies can explore this route, ranging from mechanical oscillators¹⁵¹⁶ through memristive¹⁷¹⁸ and superconducting oscillators⁶¹⁹²⁰ to optical²¹ and spintronic¹⁰²²–²⁴ oscillators. Among these, the spintronic oscillator is a promising candidate meeting all technical requirements, such as room–temperature operation, true miniaturization, CMOS integration, high-speed, and low power consumption. In a recent study, a short chain of four weakly coupled spin transfer torque nano–oscillators (STNOs) was used to perform vowel recognition²². Through tuning of the individual STNO currents, and their injection phase–locking to two external microwave sources, a recognition rate comparable to state-of-the-art CMOS processors was achieved. However, more complex tasks will require many more oscillators, and the demonstrated STNOs do not offer an attractive scaling path to much larger networks. We have recently demonstrated two–
dimensional (2D) synchronization in large arrays of an alternative emerging class of nanoscale spin-based oscillators—so-called spin Hall nano–oscillators (SHNOs). Arrays accommodating up to 64 strongly coupled SHNOs, operating at 10 GHz, achieved robust synchronization and a corresponding record-high quality factor of 170,000. We also demonstrated that the 2D–SHNO arrays were capable of performing the same type of computation as STNO chains while they operate at a 25 times higher frequency. Adding the potential to control individual SHNOs using direct voltage control, such SHNO arrays offer a viable scaling path to very large nano-oscillator networks of SHNOs that can be scaled down to 20 nm.

In addition, most oscillator network computation proposals require not only interacting oscillators but also on-chip memory for training purposes. There is hence both a practical and computational need for non-volatile storage of individual oscillator properties, a challenge that remains unsolved for nanoscale arrays.

In this work we present an ultra-low-power path to controlling the magnetization dynamics in W/(Co$_{0.75}$Fe$_{0.25}$)$_{75}$B$_{25}$/MgO based SHNOs by applying an electric field via gating. The use of electric field (voltage) to control magnetism has been extensively studied in the literature, e.g. using voltage controlled magnetic anisotropy (VCMA) to achieve low power switching in magnetic tunnel junction (MTJ) memory cells by controlling/modulating the perpendicular magnetic anisotropy (PMA). As PMA can have a significant impact on the operating frequency and the auto-oscillation (AO) mode profile of W/CoFeB/MgO based SHNOs, our voltage control of the CoFeB/MgO interface tunes the local magnetodynamical properties, resulting in a change in
the precessional angle and the mode volume\textsuperscript{26,44} that define the SHNO frequency and the coupling between SHNOs. In addition to the direct voltage control, we also show that the gates can exhibit a pronounced memristive behavior, which we then use to control both the individual oscillators and their mutual coupling to make them either operate in synchrony or break their synchronization. Synchronization control can be achieved in both the high resistance state (HRS) and the low resistance state (LRS) of the memristor, albeit through different mechanisms: electric field-driven in the HRS, and current-driven in the LRS. The memristors also add embedded memory functionality that can be used to recall the past input values each oscillator was exposed to. The demonstrated locally embedded memristive tuning capability of individual SHNOs and their coupling in large arrays provides tremendous added functionality and a direct scaling path towards the realization of large nano-scale coupled oscillatory networks for a range of different non-conventional computing paradigms.

Results and discussion

Gated SHNO and memristor geometries. After defining nano-constriction based SHNOs, to apply an electric field to the SHNO, we covered the entire W(5 nm)/(Co\textsubscript{0.75}Fe\textsubscript{0.25})\textsubscript{75}B\textsubscript{25} (1.7 nm)/MgO (2 nm)/AlO\textsubscript{x} (2 nm) based SHNO (see e.g. Ref. \textsuperscript{26,42,43}) with 15 nm SiN\textsubscript{x} and placed a 100 nm wide Ti/Cu gate on top of the 120 nm wide nano–constriction region. Fig. 1a and b show the schematic of the fabricated SHNO and the memristor in two operating regimes, HRS and LRS. The memristor shares its bottom electrode with the ground contact of the SHNO. The multilevel resistance states obtained by reversible
Figure 1: **Device schematic and multi-level resistive switching of the memristor gate.** Schematic of a SHNO with a memristive gate fabricated on top of the nanconstriction sharing a common ground contact when operating in (a) HRS and (b) LRS. A W(5)/(Co_{0.75}Fe_{0.25})_{75}B_{25}(1.7)/MgO (2)/AlO_x(2) multilayer (numbers in parentheses indicate thickness in nm) is buried in SiN_x(15) with a Ti(2)/Cu(40) top electrode as gate contact. The coordinate system shows the magnetic field vector $\mu_0H$ applied at an out–of–plane angle $\theta$ and an in–plane angle $\phi$. Upon sweeping $V_M$, an electric field driven reversible conductive bridge is formed and retracted through the insulating multilayer and the memristor current $I_M$ is added/subtracted from $I_{SHNO}$ depending on the $V_M$ polarity. (c) multi-level resistive switching of the memristive gate, controlled by the current compliance of the power supply.
memristive switching pinched at the origin is shown in Fig. 1c. The different low resistance states (LRS) of the memristor were achieved by sweeping the gate voltage while keeping the current compliance (CC) of the voltage source to different values; this controls the size of the conducting path formed inside the insulating multilayer (MgO(2 nm)/AlO$_x$(2 nm)/SiN$_x$(15 nm)). In practice, setting the memristor into various resistance states is done by programming the width of voltage pulses applied to the memristor. The (negligible) memristor current $I_M$ in the high resistance state (HRS) is defined by the leakage current of the insulating multilayer. $I_M$ in both the HRS and the LRS is added/subtracted to/from the drive current applied to the SHNO ($I_{SHNO}$) depending on the memristor voltage polarity. Because of the presence of the metal oxide layers and active upper electrode metals, MgO, AlO$_x$ and Ti/Cu, the memristive switching mechanism is believed to be governed by either oxygen or metal ion migration forming a filamentary conduction bridge (CB) inside the insulating multilayer as shown in Fig. 1a and b.

Fig. 2 shows the memristive control of the power spectral density (PSD) for a 120 nm SHNO operating at $I_{SHNO} = 1.27$ mA while a magnetic field of $\mu_0 H = 0.3$ T was applied at an out–of–plane (OOP) angle of $\theta = 65^\circ$ and an in–plane (IP) angle of $\phi = 22^\circ$ (see methods and supplementary figure 4 for detailed description of electrical measurements). The memristor is in the HRS when $V_M$ is swept in the forward direction from -2 V to 4 V as Fig. 2c shows a negligible value for $I_M$. In the HRS the conductive path is not yet formed in the memristor, so the applied voltage induces a strong electric field across the insulating multilayer changing the PMA field ($H_k^\perp$) and consequently the effective magnetization described by $M_{eff} = M_s - H_k^\perp$. The change in $M_{eff}$ directly translates into a change in the precession angle of the magnetization, resulting in an overall
Figure 2: Memristive control of SHNO auto-oscillations (AO). $I_{\text{SHNO}} = 1.27$ mA in all plots. $\mu_0 H = 0.3$ T was applied at $\theta = 65^\circ$ and $\phi = 22^\circ$. (a) SHNO frequency tuned by forward sweep of the memristor voltage from its HRS, modifying the PMA by electric field until $V_M = V_{\text{set}}$ where the AO is instead controlled by $I_M$ in the LRS. Inset: SEM image of the gate on top of the SHNO. (b) AO for the reverse $V_M$ sweep. The memristor returns to its HRS at $V_M = V_{\text{reset}}$ and the electric field regains control of the AO. (c) and (d) show the memristor current, $I_M$, for both forward and reverse sweep.
60 MHz (10 MHz/V) AO frequency change as shown in Fig.2a. When the memristor switches to one of its LRSs, in this case defined by \( CC = 100 \ \mu A \), at \( V_M = V_{set} = 4 \ \text{V} \), a non-negligible \( I_M \) is added to \( I_{SHNO} \) which in turn sharply increases the magnitude of spin current. The increase of spin current reflects in operating frequency of the SHNO as it is experimentally observed by a jump in the SHNO frequency. The frequency jump is associated with the memristor resistance state and each LRS defines a new frequency state. In the reverse sweep shown in Fig.2b and d, the AO frequency linearly follows \( I_M \) until \( V_M \) reaches \( V_{reset} \) and \( I_M \) again becomes negligible. When the SHNO chain is biased, the memristor \( I - V \) plot is no longer pinched at 0 V since the bottom electrode is at a non-zero potential. From \( V_{reset} \), the memristor is back to its HRS where the AO frequency is controlled by the electric field. One fundamental importance of the memristive gating hence lies in the fact that the memristive mechanism provides two qualitatively very different regimes with their respective tuning knobs for the frequency of the SHNO—an electric field and a memristor current.

To study the potential for using both the electric field and the memristor current to tune individual nano-constrictions in SHNO arrays, we fabricated a chain accommodating two SHNOs and placed two memristive gates, \( M_1 \) and \( M_2 \), on top of the nano-constriction regions as shown in the inset in Fig.3a. When both gates are floating, \( i.e. \) no voltage applied to either \( M_1 \) and \( M_2 \), sweeping \( I_{SHNO} \) brings the two SHNOs into synchronization at about \( I_{SHNO} = 0.8 \ \text{mA} \) as shown in Fig.3a. The SHNOs stay synchronized until \( I_{SHNO} \) reaches 0.9 mA. As our initial state, we therefore fix \( I_{SHNO} \) to 0.85 mA corresponding to a stable synchronized state.
Fig. 3b shows the memristive switching of $M_1$ as a function of the applied gate voltage, $V_{M_1}$. Starting from $V_{M_1} = -2$ V, $M_1$ stays in its HRS until it switches to its LRS at $V_{\text{set}} = 2.4$ V (blue solid data points and arrow). Upon reversing the voltage sweep direction, $M_1$ stays in its LRS until it is reset at about $-0.2$ V (green hollow data points and arrow). The corresponding response

Figure 3: A chain of two SHNOs with two memristive gates. (a) PSD vs. $I_{\text{SHNO}}$ in a field of $\mu_0 H = 0.25$ T applied at $\theta = 65^\circ$ and $\phi = 22^\circ$. The AO shows a synchronized region for a small $I_{\text{SHNO}}$ range around $0.85$ mA. The inset shows an SEM image of the two nano-constrictions with their respective memristor gates, $M_1$ and $M_2$. (b) $I_{M_1}$ vs. $V_{M_1}$ showing reversible switching between HRS and LRS defined by $CC = 100$ $\mu$A for a constant $I_{\text{SHNO}} = 0.85$ mA. (c) PSD vs. $V_{M_1}$ for the forward sweep. The electric field induced by $V_{M_1}$ in the HRS breaks the synchronized state and recovers it again as $M_1$ approaches $V_{M_1} = V_{\text{set}}$. In the LRS, an $I_{M_1} = +100$ $\mu$A adds to the $I_{\text{SHNO}}$ increasing the AO to a non-synchronized frequency in (a). (d) Extracted peak power and linewidth values vs. $V_{M_1}$ for the forward sweep in (c). (e) PSD vs. $V_{M_1}$ for reverse sweep. The AO frequency linearly follows $I_{M_1}$ recovering the synchronized state until $M_1$ switches back to its HRS and synchronization breaks apart again.
of the SHNO chain is shown in Fig. 3c. We first note that applying a negative voltage to \( M_1 \) breaks the synchronized state into two distinct frequency branches, \( f_1 \) and \( f_2 \), with lower peak power (PP) and larger linewidth (\( \Delta f \)) values as shown by the red and blue solid data points in Fig. 3d. As \( V_{M_1} \) approaches zero, the synchronized state is retrieved and appears to grow more robust since both PP and \( \Delta f \) continues to improve. However, once \( M_1 \) switches to its LRS, a substantial \( I_{M_1} = 100 \mu A \) (\( I_{M_1} > 0 \)) is sharply injected into the entire chain causing a jump in the operating frequency, as shown by the white arrow in Fig. 3a. At this operating point, the chain is no longer robustly synchronized and both PP and \( \Delta f \) deteriorate, as shown by hollow green data points in Fig. 3d. However, as Fig. 3b depicts, when \( I_{M_1} \) is reduced during the reverse sweep, the synchronized state is once again recovered even when \( I_{M_1} \) eventually changes its sign (\( I_{M_1} < 0 \)) and opposes \( I_{SHNO} \) while \( V_{M_1} \) crosses the pinch off voltage. Finally, the synchronization again breaks when \( M_1 \) is back to the HRS at \( V_{M_1} = V_{reset} \). A very similar behavior was observed when \( V_{M_2} \) forward and reversed sweeps were performed on \( M_2 \) (see Supplementary Figure 1).

We then studied the electric field and memristive tuning on the coupling within a chain accommodating four SHNOs in series. Two memristive gates, \( M_1 \) and \( M_2 \), were again fabricated but this time placed on top of the bridges connecting the SHNOs 2 & 3 and 3 & 4 as shown in the inset in Fig. 4a. As the connecting bridges are the regions where the AO modes can overlap and interact, we intend to modify the synchronization properties also this way. The PSD profile of the chain vs. \( I_{SHNO} \) (both gates floating), shown in Fig. 4a, indicates that the four oscillators start in a synchronized state and later break apart into two frequency branches for larger \( I_{SHNO} \). A value of \( I_{SHNO} = 0.712 \) mA (dotted white arrow in Fig. 4a), at which the synchronization is broken, was
chosen as the operating point to conduct the subsequent gating operation. In the HRS (indicated by the small $I_{M_1}$ Fig. 4b), sweeping $V_{M_1}$ forward (while $M_2$ is floating) brings the upper frequency branch down towards the lower frequency branch as shown in Fig. 4c. At $V_{M_1} = V_{\text{sync}}$ (white arrow in Fig. 4c) and until $V_{M_1} = 4.2$ V, the two frequency branches continue to operate in unison as also indicated by the 50% drop of the linewidth and the significant increase in the peak power (see Supplementary Figure 2). As the VCMA induced by $V_{M_1}$ increases the weak coupling to recover the broken synchronization, the chain remains synchronized even when $M_1$ switches to the LRS and $I_{M_1} = 100$ µA adds to SHNO 3 & 4. In the HRS, when $V_{M_1}$ is swept from −3 to +4.2 V, an overall frequency change of 203 MHz is achieved, corresponding to a tunability of 28 MHz/V. For the reverse sweep direction presented in Fig. 4d, the synchronization state is extended for a larger range of $V_{M_1}$ down to $V_{\text{un-syn}}$ (white arrow in Fig. 4d) as the oscillators tend to pull each other’s frequencies when they are synchronized. Therefore, $M_1$ operating in the HRS is capable of either bringing multiple oscillators to a synchronized state or break their synchronization apart. The maximum power consumption of the tuning provided by $I_{M_1}$ in the HRS is only 0.4 µW, which can be further suppressed by material engineering for the insulating multilayer. The memristive switching of $M_2$ is shown in Fig. 4e. Again, both the VCMA mechanism in the HRS and the effect of the additional current in the LRS, as well as their respective impact on the synchronization, can be clearly observed in Fig. 4f and g.
Figure 4: VCMA dominant control of synchronization in a chain of four SHNOs with two memristive gates. (a) PSD vs. $I_{\text{SHNO}}$ in a field of $\mu_0 H = 0.25 \text{ T}$ applied at $\theta = 65^\circ$ and $\phi = 22^\circ$. The AO starts in a synchronized state, then splits into two branches at higher $I_{\text{SHNO}}$. The inset shows an SEM image of the SHNO with two memristor gates, $M_1$ and $M_2$, placed mid-way between the nano-constrictions and the bridges connecting the SHNOs. For $I_{\text{SHNO}} = 0.712 \text{ mA}$, (b) $I_{\text{M}_1}$ vs. $V_{\text{M}_1}$ shows the memristive switching of $M_1$. (c) PSD vs. $V_{\text{M}_1}$ in the forward sweep where the two frequency branches synchronize by VCMA in the HRS. The chain remains synchronized even when $M_1$ switches to the LRS. (d) PSD response for reverse sweep of $V_{\text{M}_1}$. The chain stays in syncrony until $M_1$ toggles to the HRS again. (e) $I_{\text{M}_1}$ vs. $V_{\text{M}_2}$ and the memristive switching of $M_2$ having very weak impact on recovering the broken synchronized state neither in (f) forward nor in (g) reverse sweep of $V_{\text{M}_2}$. 

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Finally, we show how the memristor current itself can dominate over the VCMA effect and hence promote synchronization, or break it reversibly, when the VCMA fails to provide enough coupling to achieve synchronization. Since we have found that we can provide stronger memristor currents in the forward current direction than in the negative, we now operate the same chain as in Fig. 4 but with the direction of the applied field and current reversed. As a consequence, the growing frequency separation vs. increasing memristor current in Fig. 4g is now replaced by a decreasing frequency separation in Fig. 5e, which will be used to control the mutual synchronization. The positive direction of $I_{\text{SHNO}}$ is shown by white solid arrows in the inset of Fig. 5a. Similar to Fig. 4a, the chain starts in synchrony but fails to hold its state and splits into two frequency branches, $f_{3,4}$ and $f_{1,2}$, at more negative $I_{\text{SHNO}}$. Having fixed $I_{\text{SHNO}}$ at $-0.757$ mA, we swept $V_{M_1}$ in both the forward and reverse directions and obtained a robust memristive switching as shown in Fig. 5b. Note that due to the negative sign of $I_{\text{SHNO}}$, the memristor $I-V$ is now pinched at a negative $V_{M_1}$ value. Fig. 5c shows that during the forward sweep, while $V_{M_1}$ bends the upper frequency branch down, it fails to place it within the synchronization bandwidth with the lower frequency branch. However, when $M_1$ toggles to its LRS state at $V_{M_1} = V_{\text{set}} = V_{\text{synch}}$, a noticeable $I_{M_1}$ flows to the common ground contact through SHNO 3 & 4, this time opposing $I_{\text{SHNO}}$. Therefore, the operating current for SHNO 3 & 4 sharply drops, which is reflected as a sharp decline in the upper frequency branch. Since $I_{M_1}$ only affects SHNO 3 & 4, we can associate the operating frequency of SHNO 3 & 4 with the jump in the upper frequency branch, now indicated as $f_{3,4}$. The lower frequency branch then represents SHNO 1 & 2 and is indicated as $f_{1,2}$. As a result of the sharp frequency jump, the $f_{3,4}$ branch jumps down to a frequency value near $f_{1,2}$ where they
Figure 5: Memristive dominant control of synchronization in a chain of four SHNOs with two memristive gates. (a) PSD vs. $I_{\text{SHNO}}$ in a reversed field of $\mu_0 H = -0.25$ T applied at $\theta = 65^\circ$ and $\phi = 22^\circ$. The AO starts in a weak synchronized state, then again splits into two branches at more negative $I_{\text{SHNO}}$. The arrows in the inset define the positive direction of $I_{\text{SHNO}}$. (b) $I_{M_1}$ vs. $V_{M_1}$ showing the memristive switching of $M_1$. (c) PSD vs. increasing $V_{M_1}$ at $I_{\text{SHNO}} = -0.757$ mA. While the VCMA in the HRS is insufficient to synchronize the SHNOs, the substantial $I_{M_1}$ added when $M_1$ switches to its LRS, sharply pulls the $f_{3,4}$ branch towards $f_{1,2}$ and synchronizes the entire chain. (d) shows how the corresponding extracted linewidth and peak power values improvement when $M_1$ switches. (e) PSD vs. decreasing $V_{M_1}$. The synchronized state is first tuned by the decreasing $|I_{M_1}|$ and then breaks apart when $V_{M_1}$ switches at $V_{\text{reset}}$.

synchronize as shown in Fig. 5d indicating significant improvement in the peak power and linewidth values (hollow green data points). Reversibly, in Fig. 5e, when $|I_{M_1}|$ is too small at
\[ V_{M_1} = V_{\text{un-syn}} \] the synchronized state breaks although \( M_1 \) is still in the LRS. The two frequency branches keep increasing their distance when \( V_{\text{reset}} \) is met and electric field takes the control back. Again, memristive switching of \( M_2 \) shows to have no significant impact on bringing the chain to a synchronized state (see Supplementary Figure 3).

**Prospect for non-conventional computing.** Apart from the potential of using ultra lower power gating to control and improve the coherency and output power of SHNO arrays as microwave sources, they also hold great potential as emerging computing systems. All coupled oscillatory network-based computing schemes, irrespective of their topology and hardware implementation require a certain input interface, *e.g.* to provide a bus to feed the data in pattern recognition\[47,48\], map the problem to hardware\[28,49\], and adjust the weights for training purposes in reservoir computing. The latter happens to be a missing piece in recent reservoir computing proposals\[25,50\] for large nanoscale oscillator arrays.

Memristive control of SHNOs provides a scalable approach to both direct input and non-volatile reversible fine-tuning of the individual oscillators and their connections at any location within the network. The memristive approach not only offers such tunability at extremely low power but also opens up a wide range of opportunities to use application-specific memristors from the entire family of memristors\[46,51\] depending on the computing paradigm for which the oscillator array is designed. More importantly, the memristive gating approach inherently addresses the memory bottleneck from which conventional von–Neumann processors suffer. In memristor controlled arrays, each processing unit, *i.e.* each SHNO, has its own memory element and there
is hence no need to store and retrieve their states in any external memory limited by data transfer bandwidth. This in turn makes such oscillatory networks with intrinsic memory an appealing candidate for edge computing paradigms that aim to bring computation and data storage closer to the location where it is needed.

**Methods**

**Fabrication of memristive controlled SHNO.** A trilayer stack of $\text{W}(5)/\text{Co}_{0.75}\text{Fe}_{0.25}\text{B}_{25}(1.7)/\text{MgO}(2)$ (thicknesses in nm) was grown at room temperature on an intrinsic high resistivity Si substrate ($\rho_{\text{Si}} > 10 \text{ k}\Omega\cdot\text{cm}$) using an ultra-high vacuum sputtering system. DC and RF sputtering were sequentially employed for the depositions of metallic and insulating layers, respectively. The stack was covered with 2 nm thin layer of sputtered $\text{AlO}_x$ at room temperature to protect the MgO layer from degradation due to exposure to the ambient conditions. The stack was subsequently annealed at 300 °C for 1 hour to induce PMA. The stack was then patterned into an array of $4\times14 \mu\text{m}^2$ rectangular mesas and the nano-constriction SHNO devices with different widths were defined at the center of these mesas by a combination of electron beam lithography and Argon ion beam etching (IBE) using negative electron beam resist as the etching mask. After removing the electron resist, the sample was covered with 15 nm stoichiometric room--temperature sputtered SiN$_x$ to isolate the gate contacts from the nano--constriction metallic sidewalls. The gates were defined by sputtering a bilayer of Ti(2 nm)/Cu(40 nm) followed by EBL lithography using negative electron resist to fabricate 100 nm wide gate pattern on top of nano--constriction. The pattern was then transferred to the Ti/Cu bilayer using IBE technique.
After removing the remaining negative resist, the sample went through optical lithography using positive resist to define vias in SiN$_x$, giving access to the SHNO metal layers for the contact pads. Finally, the electrical contacts, including two SG-CPWs for microwave and dc measurements were defined by optical lithography and lift-off for a bilayer of Cu(700 nm)/Pt(20 nm).

**Memristor characterization and Microwave measurements.** All microwave electrical measurements were carried out at room temperature using a custom built probe station with the sample mounted at a fixed in-plane angle on an out-of-plane rotatable sample holder between the pole pieces of an electromagnet capable of producing a uniform magnetic field. Using a 6220 Keithley current source, a direct positive electric current, $I_{SHNO}$, was made to inject through the dc port of a high frequency bias-T and the resulting auto-oscillating signal was then amplified by a low-noise amplifier with a gain of +46 dB and subsequently recorded using a spectrum analyzer from Rhode & Schwarz (10 Hz-40 GHz) comprising a resolution bandwidth of 1 MHz. Two 2400 Keithley source meter were used to sweep the voltage in order to perform the voltage sweeps on the memristors. The output current of the source meter was complied by setting different values for the current compliance on the instrument. Also, the source meter measured the current of the memristive gates for any applied voltage confirm the proper switching between HRS and LRSs (see supplementary Figure 4 for schematic of the measurement setup).

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**Author contributions** S.F. and S.K. and H.O. developed the material stacks. M.Z. designed and fabricated the devices, and carried out all measurements and data analysis. All authors contributed to the interpretation of the results and co-wrote the manuscript.

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Figure S1: **Supplementary Fig.1.** A chain of two SHNOs with two memristive gates. (a) $I_{M_2}$ vs. $V_{M_2}$ showing reversible switching between HRS and LRS defined by $CC = 100 \mu A$ for a constant $I_{SHNO} = 0.85 \text{ mA}$. PSD vs. $V_{M_2}$ for (b) the forward and and (c) the reverse sweeps. Similar to sweeping $V_{M_1}$ in Fig.[2], $M_2$ in forward sweep provides a strong VCMA tunability to break and restore the synchronized state.
Supplementary Fig. 2. Impact of VCMA dominant control on linewidth and peak power values in a chain of four SHNOs. (a) Extracted linewidth and peak power values vs. $V_{M_1}$ for the forward sweep in Fig. 4c. Both linewidth and peak power substantially improve when $f_{1,2}$ and $f_{3,4}$ (solid blue and red data points) synchronize at $V_{M_1} = V_{\text{sync}}$ while $M_1$ is in the HRS (solid green data points). The chain remains synchronized even after $M_1$ switches to the LRS (hallow green data points). (b) Extracted linewidth and peak power values vs. $V_{M_1}$ for the reverse sweep in Fig. 4d. $I_{M_1}$ keep the SHNOs in synchrony until $M_1$ switches back to the HRS at $V_{\text{un-sync}}$ where the VCMA is too weak to keep the chain synchronized.
Supplementary Fig.3. Memristive dominant control of synchronization in a chain of four SHNOs with two memristive gates. (a) $I_{M2}$ vs. $V_{M2}$ showing the memristive switching of $M_2$. (b) PSD vs. increasing $V_{M2}$ at $I_{SHNO} = -0.757$ mA. Neither VCMA in the HRS nor the substantial $I_{M1}$ when switching to the LRS are sufficient to synchronize the chain. (c) PSD vs. decreasing $V_{M2}$. The chain remains non-synchronized for the entire $V_{M2}$ reverse sweep.
Supplementary Fig. 4. Schematic of electrical setup for characterizing memristors and microwave measurement of SHNOs.