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Large Area 1.2 kV GaN Vertical Power FinFETs with a Record Switching Figure-of-Merit

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Abstract—This work presents the first experimental study on capacitances, charges and power-switching figure-of-merits (FOMs) for a large-area vertical GaN power transistor. A 1.2 kV, 5 A GaN vertical power FinFET was demonstrated in a chip area of 0.45 mm², with a specific on-resistance of 2.1 mΩ·cm² and a threshold voltage of 1.3 V. Device junction capacitances were characterized and their main components were identified. This was used to calculate the switching charges and practical switching frequencies. Device FOMs were then derived that take into account the trade-offs between conduction and switching power losses. Our GaN vertical FinFETs exhibit high frequency (~MHz) switching capabilities and superior switching FOMs when compared to commercial 0.9-1.2 kV Si and SiC power transistors. This work shows the great potential of GaN vertical FinFETs for next-generation medium-voltage power electronics.

Index Terms— gallium nitride, vertical power transistors, FinFETs, power switching, junction capacitances, switching charges, switching frequency, power switching figure of merits.

I. INTRODUCTION

GaN devices are excellent candidates for next-generation power electronics. Vertical GaN transistors have several potential advantages over lateral GaN transistors: 1) higher breakdown voltage (BV) and current for a given chip area; 2) superior reliability and 3) easier thermal management [1]. Until now, several structures have been demonstrated for vertical GaN power transistors, such as current-aperture vertical electron transistors (CAVETs) [2]–[4] and trench MOSFETs [5]–[7]. However, the fabrication of these devices requires either the epitaxial regrowth or p-type GaN layers, which either greatly increases the fabrication complexity and cost, or limits the channel carrier mobility.

Recently, the GaN vertical power FinFET [8]–[10] (Fig. 1 (a)) was demonstrated. This transistor overcomes most of the challenges of CAVETs and trench MOSFETs as it only needs n-GaN layers and does not require epitaxial regrowth. The current in this device is controlled through the fin-shaped n-GaN channels with all-around gate stacks. In narrow fin channels, all electrons can be depleted at zero gate bias due to the work function difference between the gate metal and GaN, enabling normally-off operation. A BV of 1.2 kV and a specific on-resistance (Ron,sp) of 1 mΩ·cm² have been demonstrated [8] on small devices with tens of fins. 10 A transistors have also been fabricated but their BV was limited to 800 V [8]. To advance the device applications in power converters, large-current 1.2 kV devices are typically required. Critical device parameters for switching considerations, such as capacitance and charges, also need to be characterized.

In this work, we demonstrate a 1.2 kV, 5 A GaN vertical power FinFET by incorporating edge termination structures. Besides BV and Ron,sp, device capacitance and charges were
characterized for power switching considerations. Switching
FOMs were derived and then used to benchmark these devices
with other existing 0.9-1.2 kV power transistors.

II. DEVICE FABRICATION & STATIC PERFORMANCE

The epitaxial structure in this work consists of a 0.3 μm-thick
n⁺-GaN cap layer (Si: -2x10¹⁹ cm⁻³) and 9.5 μm-thick n⁻-GaN
drift layer (N₀=4x10¹⁵ cm⁻³), grown by MOCVD on 2-inch
n⁺-GaN substrates. As shown in Fig. 1(c), the large-area device
consists of 498 fins with 350-μm fin length and 183 fins with
200-μm fin length. The fin width, fin spacing and height are
0.18 μm, ~0.92 μm and ~1 μm, respectively. The area of active
device regions is 0.23 mm². The total device area, including
the source/gate pad areas, is ~0.45 mm². Device fabrication started
with the fin etch and corner rounding [9][11]. Edge termination
was then formed, for the first time in vertical GaN FinFETs,
below the gate pad edges by argon implantation [12][13]. The
details of edge termination will be elaborated in a future paper.
After edge termination, the remaining fabrication steps for
spacer oxides and gate, source and drain contacts were similar
to our previous report [8]. Fig. 1(b) shows a cross-section scanning
electron microscopy (SEM) image of the fin region.

Fig. 2 (a) shows the device output characteristics. The extracted
threshold voltage (Vth) is 1.3 V (at Ids=2 mA) with almost
no hysteresis. A high drain current over 5 A and a Ron of
0.9 Ω (a Ron.off of 2.1 mΩ cm² normalized with the active
device area) were obtained. Fig. 2 (b) shows the reverse
conduction characteristics, revealing a reverse turn-on voltage (Von(reverse)) of
0.8 V, which is much smaller than the one in SiC/GaN
MOSFETs (typically 2–3 V) as no pn junctions are present in
our FinFETs. This low Von(reverse) can reduce the power loss and
eliminate the need for paralleling a freewheeling diode in many
switching applications. Fig. 2 (c) shows the off-state characteristics,
revealing a destructive BV over 1.2 kV
(occurring at edge termination regions) with a μA-level leakage
current at BV. The leakage current at high bias exhibits a
ln(I) ∝ V relation, indicating the variable-range-hopping
trough dislocations as the dominant leakage mechanism [14].

Device junction capacitances Cds, Cgs and Cgd were measured as a function of VDS (Fig. 3 (a)). Cgs and Cgd dominate the device capacitance, while Cds is very small as the fin region is fully depleted at zero gate bias. Fig. 3 (b) illustrates the main components of Cgs and Cgd in in both device active regions and pad/edge regions. The Cgs in device active regions

III. SWITCHING CHARGES & FOMS

In general, device power loss under switching operations
consists of the conduction losses, switching losses and the
losses related to device/diode reverse conduction [15][17]:

\[
P = P_{cond} + (P_{gate} + P_{OSS}) + P_{rr}
\]

\[
= I^2R_{on}D + Q_{g}V_{fsw}\quad (Q_{g}V_{fsw}) + P_{rr} \quad \text{(Hard SW)}
\]

\[
= I^2R_{on}D + Q_{g}V_{fsw} + Q_{oss}V_{fsw} + I_{ds} + P_{rr} \quad \text{(Soft SW)}
\]

where D is the duty cycle and fsw is the switching frequency.

Based on the dominant switching loss in specific switching
applications, different FOMs have been proposed to benchmark
the performance of power devices, such as the Ron·Qg for
high-voltage hard-switching [16] and the Ron·(Qoss + Qg) for
resonant and soft-switching [17]. In these FOMs, the Ron
accounts for conduction losses and the charges account for

Fig. 3. (a) Device junction capacitances Cgs, Cds and Cgd measured by using the Agilent B1505A power device analyzer and a custom-built RC
circuit. (b) Schematics of different Cgs and Cgd components in the active
and pad/edge regions of a GaN vertical FinFET. (c) Calculated
components break-out for the measured Cgs and Cgd.
switching losses. To evaluate the performance of our new GaN vertical FinFETs in a broad range of power switching applications, the following power switching FOM is used considering all possible conduction and switching losses:

\[ FOM_{SW} = R_{on} (Q_G + Q_{gd} + Q_{rr}) \]  

(2)

This FOM is independent of device area or current ratings, and is suitable for evaluating our devices for both hard and soft switching (as \( Q_{oss} \approx Q_{gd} \) for our devices). As only majority carriers are involved in our devices, \( Q_{rr} \approx 0 \). \( Q_G \) is the amount of charge provided by the gate driver circuit to charge/discharge the \( C_{igs} \) during the device switching. As \( C_{igs} \) changes very little with junction biases, \( Q_G \approx C_{igs} V_G \cdot \) where \( V_G \) is the gate bias for device on-state operation. \( Q_{gd} \) is the amount of charge depleted in the drift region in the off-state. As the drift layer is designed to be fully depleted at 1.2 kV for our device (punch-through model), \( Q_{gd} = qN_D t_D A \). Then the FOM of our GaN vertical FinFETs is given by:

\[ FOM_{FINFETS}^{SW} = \frac{R_{on} (C_{igs} V_G + q N_D t_D A)}{3.3 \text{ nC} \cdot \mathcal{C}} = 3.3 \text{ nC} \cdot \mathcal{C} \]  

(3)

where \( V_G \) of 5 V is used; \( N_D \) (~4×10^{15} cm\(^{-3}\)) and \( t_D \) (8.5 µm) is the net donor concentration and thickness of the drift region between the gate and drain, respectively; and \( A \) is the total device area (~0.45 mm\(^2\)).

Switching frequency of power devices is a compromise between the conduction and switching losses. Sound design typically requires these two losses to be about the same [18]. Given this design approach, from Eqn. (1), a practical \( f_{sw} \) of ~3.5 MHz is calculated for our 1.2 kV GaN vertical FinFETs, which is much higher than 1.2 kV Si IGBTs (10-20 kHz).

Table I summarizes the key device metrics of our 1.2 kV GaN vertical FinFETs, including the chip area, \( R_{on} \), BV, \( V_{th} \), capacitances, switching charges and FOMs, benchmarked against state-of-the-art commercial 0.9-1.2 kV Si and SiC [19] power transistors. Other large-area 0.9-1.2 kV GaN devices at the R&D level [2][5][20] are also included, although, to the best of our knowledge, there is no complete experimental data reported so far for the capacitance and charges of these devices.

As shown, our device exhibited the best power switching FOMs among all 0.9-1.2 kV power transistors. This is attributable to the combination of the superior physical properties of GaN (high critical electric field and high mobility) and the merits of our vertical FinFET (small capacitances, low \( V_G \) and no \( Q_{rr} \)).

Despite the excellent performance, there is still much room for improvement in our GaN vertical FinFETs. For example, if the pad capacitances can be minimized, the FOM could be reduced to \(~2 \text{ nC} \cdot \mathcal{C}\). On the other hand, the fin spacing currently used in our devices (0.92 µm) is relatively large compared to the fin width (0.18 µm). This indicates large room for improvement in \( R_{on} \)-junction capacitances and charges by shrinking the fin spacing. From the fabrication point of view, the fin spacing could be well reduced to below 0.3 µm, while the derivation of the optimum fin spacing requires a more comprehensive consideration of spreading resistance, capacitances and heat dissipation. We will do this derivation in the future work.

### IV. SUMMARY

This work demonstrates a large-area 1.2 kV, 5 A GaN vertical power FinFET. Systematic device characterization of \( R_{on} \), \( BV \), \( V_{th} \) and capacitances is presented, followed by the charge analysis and FOM derivation for power switching applications. Our device shows superior power switching FOMs when compared to commercial 0.9-1.2 kV Si and SiC power transistors. This performance demonstrates the great potential of GaN vertical FinFETs for next-generation medium-voltage and high-frequency power applications.
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