Ultra-Low Power Poly-Si TFTs with 10 nm Stacked Gate Oxide Fabricated by Nitric Acid Oxidation of Silicon (NAOS) Method

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Abstract

We have fabricated poly-silicon-based thin film transistors (TFTs) on glass substrates, and achieved ultra-low power consumption by driving at 1 V. The gate oxide layer has a 10 nm thick stacked structure with a 1.4 nm interfacial SiO2 layer formed by the nitric acid oxidation of silicon (NAOS) method and a 8.6 nm SiO2 layer formed by a plasma-enhanced chemical vapor deposition (PECVD) method. The dynamic power consumption ratio of the NAOS-TFTs is 1/144 of that for the currently commercial TFTs with the driving voltage of 12 V and 80 nm gate oxide. The off-current decreases by ~2 orders of magnitude by insertion of the ultrathin NAOS SiO2 layer. The current decrease is attributed to i) blocking of the gate leakage current by the NAOS SiO2 layer, and ii) improvement of the quality of the deposited oxide on the NAOS SiO2 layer because of better nucleation, and consequently, the high on/off ration exceeding 1010 is achieved.

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Low power consumption is one of the most important issues for mobile products with batteries. System liquid crystal displays (LCDs) are widely used for popular mobile electronic products such as smart phones, e-books, and personal digital assistance (PDAs) because of their low power consumption.

The dynamic power consumption of a TFT, \( P \), is expressed as

\[ P = f C V^2 \]

where \( f \) is a signal frequency, \( C \) is a charging and discharging capacitance, and \( V \) is a driving voltage. Therefore, the consumed power can be decreased most effectively by reducing the driving voltage, which is approximately proportional to a gate oxide thickness. The decrease in the gate insulator thickness makes it possible not only to decrease the consumed power but also to miniaturize TFTs, which greatly improves electrical characteristics of TFTs.

Thermal oxidation is unavailable for TFT production because of the use of glass substrates with low softening temperature of ~1000 °C. Consequently, a gate oxide layer in poly-crystalline Si (poly-Si)-based TFTs is usually formed by the plasma-enhanced chemical vapor deposition (PECVD) method using tetraethyl orthosilicate (TEOS). However, deposition methods have following demerits: i) interface state densities are high due to incomplete interfacial chemical bonds and presence of contaminants before deposition, ii) bulk characteristics are poor due to interface defects, iii) particles which were originally formed in the gas phase and C and OH contaminants, and iv) due to poor nucleation of an SiO2 layer on poly-Si surfaces compared to that on oxide surfaces.

Oxide layer thickness is not uniform on rough poly-Si surfaces due to formation of ridge structure arising from laser annealing of amorphous-Si (a-Si) films to crystallize.

Extensive studies have been performed for developing direct Si oxidation methods at low temperatures including plasma oxidation, photo-oxidation, ozone oxidation, metal-promoted oxidation, etc. We have developed a low temperature direct Si oxidation method, i.e., the chemical oxidation method called nitric acid oxidation of Si (NAOS) method. This method simply involves immersion of Si in high concentration (i.e., 68–98 wt%) nitric acid (HNO3) aqueous solutions at temperatures below 120 °C. We have observed that a 1.4 nm-NAOS SiO2 layer formed on Si(100) possesses approximately one order of magnitude lower leakage current density than that of a 1.5 nm-thermal oxide layer. TFTs with a gate oxide of 20 and 40 nm thickness with a NAOS SiO2 layer have decreased the dynamic consumption to 1/16 and 1/64 (1/V2 reduction) of that for the current commercial TFTs with 12 V driving voltage, respectively.

In the present study, we have demonstrated that the driving voltage of 1 V is realized by a decrease in the gate oxide thickness to 10 nm (cf. 80 nm for commercial TFTs). The ultrathin 1.4 nm NAOS interfacial SiO2 layer greatly decreases the leakage current density, which makes it possible to decrease the gate oxide thickness to 10 nm. Consequently, the dynamic power consumption ratio of 1/144 (1/V2 reduction) of that for the current commercial TFTs with 12 V driving voltage has been achieved.

Experimental

Fig. 1 shows the TFT fabrication process flows. The schematic structure of the fabricated TFTs with the NAOS method is shown in Fig. 2. The TFTs were fabricated on non-alkali metal glass substrates. A 100 nm thick silicon nitride layer was deposited on the glass substrates to prevent diffusion of contaminants from the glass substrates. Then, 50 nm thick a-Si films were deposited by use of the PECVD method. The a-Si films were irradiated using an excimer laser in order to crystallize. Si patterns were formed with lithography, followed by etching in a diluted HF aqueous solution to remove native oxide.

For the TFTs with a NAOS SiO2 layer, a 1.4 nm thick SiO2 layer was formed by immersion in 68 wt% HNO3 aqueous solutions (i.e., azetotropic mixture of HNO3 and water) at 120 °C for 10 min. A 8.6 nm thick SiO2 layer was deposited on the NAOS SiO2 layer using the PECVD method. For the TFTs without a NAOS SiO2 layer, 10, 20 or 30 nm thick SiO2 layer was deposited on the poly-Si surface using the PECVD method. These TFTs were fabricated in a foundry for industrial production of TFTs with a 80 nm PECVD SiO2 gate oxide and no NAOS layer. Therefore, TFTs represent the actual technological level used at the poly-Si TFTs industrial production.

Tungsten gate electrodes were fabricated, and single drain and source regions were defined by ion implantation with phosphorous and boron for n-channel (N-ch) and p-channel (P-ch) TFTs, respectively, followed by activation annealing at 500 °C for 1 h in nitrogen atmosphere. Then, a dielectric interlayer was deposited using the PECVD method, and contact holes and aluminum (Al) wires were fabricated. For current-voltage (I-V) measurements, an ultrathin NAOS SiO2 layer was formed on p-Si(100) wafers of ~10 Ωcm resistivity. Al dots of 0.15 mm diameter were formed by the vacuum evaporation method, resulting in (Al/NAOS SiO2/Si(100)) MOS structure. Post-metalization annealing (PMA) was performed at 200 °C in 5 vol% hydrogen for 20 min. I-V measurements were performed using an HP 4140B picoamperemeter.
X-ray photoelectron spectroscopy (XPS) spectra were measured using an ESCALAB 220i-XL spectrometer with a monochromatic Al Kα radiation source. Photoelectrons were collected in the surface-normal direction.

TEM micrographs were observed using a JEOL JEM-3000F microscope at an incident electron energy of 300 keV.

Surface metal concentrations were determined by total X-ray reflection fluorescence (TXRF) measurements using a Technos TRENEX 610 spectrometer.

Electrical characteristics of the fabricated TFTs were measured using an Agilent B1500A semiconductor device analyzer. The field-effect mobility was calculated from the maximum transconductance at $|V_{ds}| = 0.1$ V. The on-current ($I_{on}$) and off-current ($I_{off}$) were measured by use of an auto-prober for 25 TFTs.

Results and Discussion

TEM micrographs of the NAOS SiO₂/Si(100) structure are shown in Fig. 3. It is clearly seen that a uniform SiO₂ layer was formed on the Si substrate. From the magnified view (Fig. 3b), the thickness of the NAOS SiO₂/Si(100) was found to be 1.39 nm. Figs. 3a and 3b verify the formation of a flat SiO₂/Si(100) interface in a wide region. Fig. 3b demonstrates that step edge formation is limited to bilayer steps as indicated by the arrow. Bilayer steps most probably result from misorientation from the (100) direction. This indicates that the NAOS oxidation proceeds with a layer-by-layer oxidation mechanism.

TEM micrographs of a NAOS layer formed on a poly-Si surface are shown in Fig. 4. A NAOS SiO₂ layer of a uniform thickness with a smooth interface is clearly seen on the poly-Si surface. This corresponds to the result that a NAOS SiO₂ layer of the same thickness was formed on the Si(100) and Si(111) surfaces.

Fig. 5 shows the XPS spectrum in the Si 2p region for the NAOS SiO₂/Si structure. The SiO₂ thickness was also estimated to be 1.4 nm from the ratio in the area intensity between SiO₂ and Si peaks. No XPS peaks for suboxides were observed between the Si and SiO₂ peaks. The concentrations of metal contaminants after the NAOS method obtained from TXRF measurements were always below the lower detection limit of $\sim 3 \times 10^9$ atoms/cm². This result indicates that the NAOS method can effectively remove metal contaminants.

Transmission electron micrographs (TEM) of the fabricated TFT are shown in Fig. 6. Source, drain and gate electrodes were clearly seen in Fig. 6a. The magnified view (Fig. 6b) clearly shows the layered structures consisting of glass, back coat, poly-Si, ultra-thin gate oxide, and gate electrode. The high resolution TEM micrograph (Fig. 6c)
showed the formation of a uniform gate oxide layer with the 10 nm thickness on a rough poly-Si surface. The threshold voltage was defined as a voltage where the drain current at source-drain voltage $|V_{ds}|$ of 3 V was equal to $(W/L) \times 10^{-7}$ A ($W$: gate width, $L$: gate length). The threshold voltage ($V_{th}$) was $0.2 \sim 0.4$ V for the N-ch TFTs and $-0.4 \sim -0.5$ V for the P-ch TFTs as shown in Fig. 7. Due to the low $V_{th}$, the driving voltage could be as low as 1 V as described below. Sub-micrometer TFTs could also be fabricated with the ultrathin gate oxide. It was found that the ultra-thin NAOS SiO$_2$ layer on poly-Si effectively blocks the gate leakage current.

Fig. 8 shows the drain current vs. drain-source voltage ($I_d-V_{ds}$) curves for the TFTs with the 1.4 nm NAOS SiO$_2$/8.6 nm CVD SiO$_2$ stacked gate oxide structure. The gate length and width are 0.9 and 10 $\mu$m, respectively. The $I_d-V_{ds}$ curves were measured with the 0.5 V step in the gate-source voltage ($V_{gs}$) region between 0.5 and 3.0 V. The $I_d-V_{ds}$ curves showed good saturation feature, and the saturation current was sufficiently high even at the supply voltage of 1 V, demonstrating that the TFTs could be operated at 1 V. Eq. 1 indicates that consumed power was reduced to $(1/12)^2 = 1/144$, i.e. $1/V^2$ reduction that of commercial TFTs with 12 V driving voltage.

Fig. 9 shows the $I_d-V_{gs}$ curves at $|V_{ds}|=0.1$ V for the TFTs with a NAOS SiO$_2$ layer. $I_d$ rapidly changed with $V_{gs}$ in the region between 0 and 1 V for the N-ch TFTs and between $-1$ and 0 V for the P-ch TFTs. The sharp feature of these curves indicates that these TFTs possess low sub-threshold swings (S-values) because of low interface state densities and the thin gate oxide thickness (i.e., 10 nm).

Figs. 10 and 11 show scatter diagrams of $I_{on}$ vs. $I_{off}$ for the N-ch and P-ch TFTs, respectively. $I_{on}$ was measured at $|V_{gs}|=3$ V, while $I_{off}$ was measured at $I_{off}$ $|V_{gs}|=1$ V ($|V_{ds}|$ was set at 3 V for both cases). In Figs. 10 and 11, $I_{on}$ and $I_{off}$ increase with decreasing gate oxide thickness due to increases in a channel carrier density and a gate leakage current, respectively. It should be noted that $I_{off}$ for the N-ch and P-ch TFTs with the NAOS SiO$_2$ layer was lower by $\sim 2$ orders of magnitude than those without it. $I_{off}$ for the NAOS-TFTs with the 10 nm gate oxide was nearly the same as that for TFTs with the 20 nm CVD SiO$_2$ layer, indicating that the ultra-thin NAOS SiO$_2$...
layer effectively blocks the gate leakage current. $I_{\text{off}}$ at $|V_{gs}| < 1.5$ V could not be determined because it was lower than the lower detection limit of the semiconductor analyzer. A reduction of the gate leakage current by the NAOS SiO$_2$ layer formed at 120 °C is ascribed to (i) low density interface states by direct oxidation of poly-Si surfaces, (ii) uniform thickness of the NAOS SiO$_2$ layer, and (iii) high atomic density of the NAOS SiO$_2$ layer, resulting in a high band discontinuity energy at the Si/SiO$_2$ interface, and thus in a low tunneling probability of charge carriers through SiO$_2$.\[^{20,27}\] Moreover, the characteristics of the CVD SiO$_2$ overlayer are thought to be improved by the NAOS interfacial layer with a better CVD SiO$_2$ nucleation on a NAOS layer compared to a poly-Si surface. This is because the NAOS treatment greatly decreased the concentrations of metal contaminants (e.g., Fe contaminant before and after the NAOS treatment: ~4 × 10$^{10}$ and ~1 × 10$^{10}$ atoms/cm$^2$, respectively) and formed considerably flat SiO$_2$ surfaces (cf. Fig. 3) due to the layer-by-layer oxidation mechanism.\[^{28}\] $I_{\text{off}}$ for N-ch and P-ch TFTs with the 0.9 μm gate length was decreased to 1/100 by insertion of the ultra-thin NAOS SiO$_2$ layer.

Fig. 12 shows the S-values of the TFTs at $|V_{ds}| = 0.1$ V. The S values were between 70 and 80 mV/decade which was close to the theoretical limit of 60 mV/decade at room temperature (RT).\[^{30}\] These low S-values resulted from the thin gate insulator and the high quality Si/NAOS SiO$_2$ interface with a low interface state density. From the S values, the interface state density $D_{it}$ is roughly estimated to be $6 × 10^{11}$/cm$^2$ eV for N-ch TFTs and $4 × 10^{11}$/cm$^2$ eV for P-ch TFTs by use of the following equation:\[^{31}\]

$$D_{it} = \frac{C_{it}}{q} = \frac{(n - 1)C_{ox} - C_d}{q} = \frac{(S \log e)C_{ox} - C_d}{q}$$  \[2\]

where $C_{it}$, $C_{ox}$ and $C_d$ are capacitances of interface states, gate oxide and a depletion layer ($C_d \sim 10^{-8}$ F/cm$^2$ $< (n - 1)C_{ox} \sim 3 \times 10^3$ F/cm$^2$), respectively, $q$ is the unit electronic charge, $k$ is the Boltzmann’s constant, and $T$ is the temperature, and $n$ is given by:\[^{31}\]

$$n = \frac{S q \log e}{kT}$$  \[3\]

The interface state densities have been reported to be $1.4 \times 10^{12} \sim 1.1 \times 10^{13}$/cm$^2$ for poly-Si-based TFTs with a PECVD-SiO$_2$ gate oxide.\[^{32-35}\] The interface state density at the NAOS-SiO$_2$/poly-Si interface was much lower than those values.

The channel mobilities were 100–200 cm$^2$/V$\cdot$s for the N-ch TFT and 80–120 cm$^2$/V$\cdot$s for the P-ch TFT as shown in Fig. 13. These channel mobilities were higher than those for poly-Si-based TFTs\[^{35}\] and InGaZnO-based TFTs\[^{36}\] reported in previous literature. The high mobilities result from the high quality Si/NAOS SiO$_2$ interface (i.e., low interface state density), and hence, they depend only on the poly-Si quality without degradation by the interface.

**Conclusions**

In the present research, we have succeeded in the fabrication of TFTs with 10 nm (1.4 nm NAOS SiO$_2$/8.6 nm CVD SiO$_2$) stacked gate dielectric structure. Due to the thin gate insulators, the sub-micrometer TFTs driven at 1 V were achieved. The dynamic TFT power consumption could be reduced to 1/100 of that for conventional TFTs with the 12 V driving voltage. The excellent electrical characteristics of the NAOS SiO$_2$ layer led to remarkably low S values of 70–80 mV/decade and high on/off ratio of 10$^6$. The stand-by power consumption could also be decreased to 1/100 of that for a TFT without a NAOS SiO$_2$ interfacial layer. The present study demonstrates that the NAOS method is promising for mass production of TFTs for the following reasons: i) a high quality ultra-thin SiO$_2$ layer with a low leakage current and a low interface state density formed at low temperature; ii) non-time consuming and low cost method which simply involves immersion in azeotropic (i.e., 68 wt%) HNO$_3$ solutions for several minutes.

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References

1. G. Palumbo and M. Pennisi, *Integration, VLSI J.*, 41, 439 (2008).
2. R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Basset, and A. R. Le Blanc, *IEEE J. Solid State Circuit*, SC-9, 256 (1974).
3. Y. Z. Wang, O. O. Awadelkarim, J. G. Couillard, and D. G. Ast, *Solid-State Electron.*, 42, 1689 (1998).
4. B. Stanislawski, J. K. Rath, and R. E. O. Schropp, *Thin Solid Films*, 430, 220 (2003).
5. Y. Chen, K. Pangal, J. C. Sturm, and S. Wagner, *J. Non-Crystal. Solids*, 266–269, 1274 (2000).
6. A. Saboundji, N. Coulon, A. Gorin, H. Lhermite, T. Mohammed-Brahim, M. Fonrodona, J. Bertomeu, and J. Andreu, *Thin Solid Films*, 87, 227 (2005).
7. S. V. Nguyen, D. Dobuzinsky, D. Dopp, R. Gleason, M. Gibson, and S. Fridmann, *Thin Solid Films*, 193/194, 595 (1990).
8. O. Maida, H. Yamamoto, N. Okada, T. Kanashima, and M. Okuyama, *Appl. Surf. Sci.*, 130–132, 214 (1998).
9. H. Kinoshita, T. Murakami, and F. Fukushima, *Vacuum*, 76, 19 (2004).
10. V. E. Vamvakas and D. Davaazoglu, *Microelectron. Reliab.*, 38, 265 (1998).
11. S. Uchikoga and N. Ibaraki, *Thin Solid Films*, 383, 19 (2001).
12. H. Niimi, K. Koh, and G. Lucovsky, *Nucl. Instrum. Methods Phys. Res. B*, 127/128, 364 (1997).
13. H. Kakiuchi, H. Ohtma, M. Harada, H. Watanabe, and K. Yasutake, *Sci. Technol. Adv. Mater.*, 8, 137 (2007).
14. J.-Y. Zhang and I. W. Boyd, *Appl. Surf. Sci.*, 186, 64 (2002).
15. N. Kalish, J.-Y. Zhang, and I. W. Boyd, *Appl. Surf. Sci.*, 168, 288 (2000).
16. S. Ichimura, A. Kurokawa, K. Nakamura, H. Itoh, H. Nonaka, and K. Koike, *Thin Solid Films*, 577–578, 518 (2000).
17. K. Koike, K. Izumi, S. Nakamura, G. Inoue, A. Kurokawa, and S. Ichimura, *J. Electron. Mater.*, 34, 240 (2005).
18. H. Kobayashi, T. Yuasa, Y. Nakato, K. Yonedo, and Y. Todokoro, *J. Appl. Phys.*, 80, 4124 (1996).
19. H. Kobayashi, T. Yuasa, K. Yamanoaka, K. Yonedo, and Y. Todokoro, *J. Chem. Phys.*, 109, 4997 (1998).
20. H. Asuha, Y. Yuasa, O. Maida, and H. Kobayashi, *Appl. Phys. Lett.*, 80, 4175 (2002).
21. H. Kobayashi, H. Asuha, O. Maida, M. Takahashi, and H. Iwasa, *J. Appl. Phys.*, 94, 7328 (2003).
22. H. Asuha, T. Kobayashi, M. Takahashi, and H. Kobayashi, *Surf. Sci.*, 547, 275 (2003).
23. H. Asuha, Y.-L. Liu, O. Maida, M. Takahashi, and H. Kobayashi, *J. Electrochem. Soc.*, 151, G824 (2004).
24. W.-B. Kim, T. Matsumoto, and H. Kobayashi, *J. Appl. Phys.*, 105, 103709 (2009).
25. Y. Fukaya, T. Yanase, Y. Kubota, S. Imai, T. Matsumoto, and H. Kobayashi, *Appl. Surf. Sci.*, 256, 5610 (2010).
26. T. Matsumoto, Y. Kubota, M. Yamada, H. Tsuji, T. Shimatani, Y. Hirayama, S. Terakawa, S. Imai, and H. Kobayashi, *IEEE Electron Device Lett.*, 31, 821 (2010).
27. Y. Kubota, T. Matsumoto, S. Imai, M. Yamada, H. Tsuji, K. Taniguchi, S. Terakawa, and H. Kobayashi, *IEEE Trans. Electron Devices*, 58, 1134 (2011).
28. H. Asuha, T. Kobayashi, O. Maida, M. Inoue, M. Takahashi, Y. Todokoro, and H. Kobayashi, *Appl. Phys. Lett.*, 81, 3410 (2002).
29. W.-B. Kim, W.-B. Asuha, T. Matsumoto, and H. Kobayashi, *Appl. Phys. Lett.*, 93, 072101 (2008).
30. H.-C. Lin, C.-H. Kao, G.-J. Li, C.-J. Su, and T.-Y. Huang, *IEEE Electron Device Lett.*, 31, 384 (2010).
31. D. K. Shroder, “Semiconductor material and device characterization”, 3rd ed., John-Wiley & Sons, Inc., New Jersey, 2006, pp. 359.
32. M.-W. Ma, T.-Y. Chiang, C.-R. Chao, and T.-F. Lei, *Electrochem. Solid-State Lett.*, 12, H361 (2009).
33. Z. Meng, M. Wang, and M. Wong, *IEEE Electron Device Lett.*, 47, 404 (2000).
34. M.-J. Yang, C.-H. Chien, Y.-H. Lu, C.-Y. Shen, and T.-Y. Huang, *IEEE Electron Device Lett.*, 29, 1027 (2008).
35. S. B. Brotherton, C. Glasse, C. Glaister, P. Green, F. Rohlfing, and J. R. Ayres, *Appl. Phys. Lett.*, 84, 293 (2004).
36. T. Kamiya, K. Nornura, and H. Hosono, *Sci. Technol. Adv. Mater.*, 11, 044305 (2010).