Quantum scaling in nano-transistors

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Abstract

In our previous papers on ballistic quantum transport in nano-transistors [J. Appl. Phys. 98, 84308 (2005)] it was demonstrated that under certain conditions it is possible to reduce the three-dimensional transport problem to an effectively one-dimensional one. We show that such an effectively one-dimensional description can be cast in a scale-invariant form. We obtain dimensionless variables for the characteristic channel length $l$ and width of the transistor which determine the scale-invariant output characteristic. For $l \gtrsim 10$, in the strong barrier regime, the output characteristics are similar to that of a conventional MOSFET assuming an ideal form for $l \to \infty$. In the weak barrier regime, $l \lesssim 10$, strong source-drain currents lead to i-v characteristics that differ qualitatively from that of a conventional transistor. Comparing with experimental data we find qualitative agreement.

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Recently, a number of extremely small nano-transistors with physical gate lengths of fifteen nanometers or less have been fabricated[1, 2, 3]. A rather simple but particularly illuminating approach to describe the electron dynamics in such small structures is to assume ballistic quantum transport (for a recent review see Ref. [4]). It is found for a long enough electron channel that the output characteristic is similar to that of a conventional transistor. However, in this quantum ballistic transistor (QBT) regime source-drain tunneling currents cause residual slopes in the ON-state and the development of only a quasi-OFF-state. In Refs. [5, 6] it was shown that separating the ON-state of classically allowed transport and the quasi OFF-state of tunneling transport there is a threshold characteristic (TH) which exhibits a close-to-linear dependence of the current on the drain voltage. Above the TH, in the ON-state, the I-V curves are characterized by a negative bending and below the TH by a positive bending. In Refs. [5, 6] it was furthermore demonstrated that for a narrow electron channel the complete three-dimensional quantum problem can be approximated by an effectively one-dimensional one (Fig. 1).

In the present paper we recast our effectively one-dimensional description of quantum transport in a nano-transistor in a scale-invariant form. The scaled output characteristics of a transistor are governed by its dimensionless characteristic length \( l = L/L_0 \) and the width \( w = W/(\pi L_0) \), which are given by its physical length \( L \) and width \( W \) in units of the scaling length \( L_0 = \hbar/(2m^*\epsilon_F)^{1/2} \). Here \( \epsilon_F \) is the Fermi energy in the source contact and \( m^* \) is the effective mass in the electron channel in transport direction. The characteristic length permits a classification of source-drain barriers in terms of their strength. In the strong barrier regime, \( l \gtrsim 10 \), typical output characteristics in the QBT regime occur. As \( l \to \infty \), ideal output characteristics (IOC) are assumed with a vanishing residual slope in the ON-state and a clear OFF-state exhibiting negligible leakage currents. In the weak barrier regime, \( l \lesssim 10 \), strong source-drain currents lead to I-V characteristics which differ strongly from that of a conventional transistor. In the limit of large \( w \) we relate our scaling theory to the experiments and find qualitative agreement.

In Fig. 1 our effective potential \( V^{eff} \) is illustrated. Though simple, it allows us to define the essential parameters: because of good screening it is constant in the source contact with \( V^{eff}(y \leq 0) = 0 \) and in the drain contact with \( V^{eff}(y \geq L) = -eU_D \), where \( U_D \) is the applied drain voltage. The source-drain barrier is taken as a constant potential offset \( V_0 \) for \( 0 \leq y \leq L \). In the latter interval there is an additional contribution due to the applied
FIG. 1: a) Generic n-channel FET in three dimensions: narrow electron channel (blue) with abrupt transition to source and drain contact (red). b.) Effective one-dimensional potential in the ON-state: \( V_g \equiv \epsilon_F - V_0 > 0 \).

The drain voltage which is assumed to fall off linearly so that \( V_{\text{eff}}(0 \leq y \leq L) = V_0 - eU_D y / L \). Such a piecewise linear potential or more complex potentials with the same qualitative behavior have been used in the literature.

We calculate the drain current through

\[
i = \dot{\epsilon}_F^{-1} \int_0^\infty d\dot{\epsilon} \left[ F(\dot{\epsilon}_F - \dot{\epsilon}) - F(\dot{\epsilon}_F - \hat{v}_D - \dot{\epsilon}) \right] T_{\beta \hat{v}_D}(\dot{\epsilon}),
\]

with the normalized drain current \( i = I/I_0 \), \( I_0 = 2e\epsilon_F/h \), and \( \dot{\epsilon}_F = \epsilon_F/V_0 \), and \( \hat{v}_D = eU_D/V_0 \). The current transmission \( T_{\beta \hat{v}_D}(\dot{\epsilon}) = k_{\text{s eff}}^s(\dot{\epsilon})|t^S(\dot{\epsilon})|^2[k_{\text{s eff}}^s(\dot{\epsilon})]^{-1} \) results from the transmission coefficient \( t^S(\dot{\epsilon}) \) of a source-incident scattering function in a one-dimensional scattering problem associated with the effective Schrödinger equation

\[
\left[-\frac{1}{\beta} \frac{d^2}{dy^2} + \hat{v}_{\text{eff}}^s(\dot{y}) - \dot{\epsilon}\right] \psi(\dot{y}, \dot{\epsilon}) = 0.
\]

Here we have \( \dot{y} = y/L \), \( \beta = 2m^*V_0 L^2/h^2 \), \( \hat{v}_{\text{eff}}^s(\dot{y}) = V_{\text{eff}}^s(y)/V_0 \), \( k_{\text{s eff}}^s = \sqrt{\beta(\dot{\epsilon} + \hat{v}_s)} \), \( s = S/D \), and \( v_S = 0 \). The three-dimensional geometry of the transistor determines the choice of the supply function \( F \). For a narrow transistor (small \( W \)) it was shown in Ref. [6] that at \( T = 0 \) it is given by \( F(x) = \Theta(x) \). In a straightforward way one can generalize this result to a wide transistor yielding \( F(x) = \hat{w} \sqrt{x} \Theta(x) \), with the normalized transistor width \( \hat{w} = \sqrt{2m^*W^2V_0/(\hbar \pi)} \) [8].

To consider an I-V chart \( I(U_G, U_S) \) we represent the gate potential \( U_G \) by the parameter \( V_g = \epsilon_F - V_0 \), which is the deviation of the Fermi energy in the source contact from the maximum of the source-drain barrier (see Fig. 1(b)). Normalized to \( V_0 \) one has \( \dot{\epsilon}_F = \hat{v}_g + 1 \),
allowing us to eliminate $\hat{\epsilon}_F$ in Eq. (1). Furthermore, we define new variables $v_D = eU_D/\epsilon_F$ and $v_g = V_g/\epsilon_F$. These are normalized to $\epsilon_F$, which is independent of the gate voltage. To cast $\hat{v}_D$ and $\hat{v}_g$ in terms of $v_D$ and $v_g$ in Eq. (1) one exploits the identities $\hat{v}_g = v_g/(1 - v_g)$ and $\hat{v}_D = v_D/(1 - v_g)$. Furthermore, the parameter $\beta$ is replaced by $\beta = l^2(1 - v_g)$, where we introduce the dimensionless characteristic length of the transistor as $l = L/L_0$ with the scaling length

$$L_0 = \frac{\hbar}{\sqrt{2m^*\epsilon_F}}.$$

(3)

FIG. 2: i-v-traces in wide transistor limit, $v_g$ starting from 0.5 with decrements of 0.1 (solid lines, blue for $v_g = 0$). a) $l = 500$ and b) $l = 10$ in strong barrier regime. Best straight line fit for $v_g = 0$ in red dashed line, in a) coinciding with the x-axis. c) $l = 5$ in weak barrier regime.
Likewise $\hat{w} = w(1 - v_g)$, where we introduce the characteristic width of the transistor as $w = W/(\pi L_0)$.

The calculated $I - V$ traces in Figs. 2 (a) and (b) exemplify the QBT regime at $l \gtrsim 10$. For positive $v_g$, i.e. in the ON-state, an initial linear dependence of the drain current for small drain voltages turns into a quasi-saturation regime for larger drain voltages. The turnover between linear and quasi-saturation regime becomes more and more abrupt, which is seen in the experimental transistors in Fig. 3 (a) and (b) as well. The essentially linear THs at $v_g = 0$ allow us to define a threshold conductivity through $i/w = \sigma_{th} v_D$. Upon analysis of the numerical data it can be seen that in the range of interest $10 \leq l \leq 500$ one can approximate with an error of less than 10 percent $\sigma_{th} \sim 0.94 l^{-1.25}$. This weak power law decrease indicates that the IOC are assumed slowly with growing $l$ and that there is no critical characteristic length to define a hypothetical ‘ideal transistor regime. As shown in Fig. 2 (c) in the weak barrier limit, $l \lesssim 10$, I-V traces differ strongly from that of a conventional field effect transistor because of strong source-drain tunneling and no TH is observed.

For a rough estimate of the characteristic lengths in the experimental nano-transistors in Fig. 3 we approximate $\epsilon_F$ by the well-known expression for a three-dimensional non-interacting electron gas. Assuming a high level of source-doping of $N_D \sim 5 \times 10^{20} cm^{-3}$ yields $\epsilon_F = 0.2 eV$. Inserting in Eq. 3 furthermore the silicon light mass, $m^* = 0.19 m_0$, one obtains $L_0 \sim 1 nm$. The experimental channel lengths of 5nm to 15nm then correspond to characteristic lengths of five, ten, and fifteen. As expected we find for $l \gtrsim 10$ a close-to linear TH with an experimental threshold slope $\Sigma_{th} = I/(WU_D) = 75 \mu A/(\mu m A)$ for $L = 15 nm$ and $\Sigma_{th} = 270 \mu A/(\mu m A)$ for $L = 10 nm$. Writing $\Sigma_{th} = 2 \sigma_{th} e^2/(h\pi L_0)$ one obtains for $l = 15$ a theoretical value for $\Sigma_{th}$ of 750$\mu A/(\mu m A)$ and for $l = 10$ a theoretical value of 1250$\mu A/(\mu m A)$. While the decrease in the threshold conductivity results theoretically and experimentally, there is a considerable quantitative discrepancy which is to be expected because in our model essential effects like heating of the transistor and microscopic Coulomb interaction are not included. Consistent with Fig. 2 (c) the I-V characteristics of the experimental transistor with 5nm gate length in Fig. 3 (c) seem to deviate considerably from the output characteristic of conventional transistor. However, for a characterization of the breakdown of the QBT-regime for weak barriers further research is needed. Finally, we note that in the range of the experimental $L$ the barrier strength could be increased using metal
FIG. 3: Experimental output characteristics: a) 15nm gate length (taken from Ref. [3]) b) 10nm gate length (taken from Ref. [2]), We locate the position of the TH in the strong barrier limit as marked by a blue arrow. c) 5nm gate length (taken from Ref. [1]).

contacts like in a Schottky barrier transistor[9]. Here larger $\epsilon_F$ are possible which according to Eq. (3) lead to smaller $L_0$ and larger $l$.

In summary, we present a scaling theory for quantum transport in nano-transistors. The scaled i-v characteristics depend on the dimensionless characteristic length of the transistor channel which allows for a classification of a given source-drain barrier in terms of its strength. In the strong barrier regime, $l \gtrsim 10$, the output characteristics are similar to that of a conventional MOSFET assuming an ideal form for $l \to \infty$. In the weak barrier regime strong source-drain currents occur and the i-v characteristics differ strongly from that of a conventional transistor.
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