A Novel Loadless 6T-SRAM Cell with Isolated Read Port

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Abstract: Conventional 6T SRAM cell parameters have degraded with scaling to newer technologies and reduced power supply voltages. This has led to numerous tradeoffs with respect to cell stability, performance, power, and area. In this paper, a novel Dual Port SRAM design has been introduced that aims at improving the read and write ability of the standard 6T SRAM cell. The simulations for the proposed structure have been performed on HSpice using PTM 32nm Technology node. The comparison of results with the standard cell showed an increase of 84.76% in read margins and 40.81% in the write stability. Also, the proposed design was found to be capable of writing at high frequencies as the minimum pulse width of WWL for a successful write operation was determined to be 25ps. Further, the design also improves in the areas of WTV, SVNM, WTP, SPNM

1. INTRODUCTION

Static Random Access Memory forms a major part of system-on-chip (SoC) and has become a significant area of interest due to a wide variety of microelectronic applications. From memory hierarchy in computer systems to high-performance multimedia products, there has been a crucial need for high speed and robust SRAMs. The need to improve performance and robustness has led to rapid scaling of the CMOS technology. However, with this scaling of dimensions both the read and write stabilities of the standard 6T cell get affected. For the correct working of the SRAM cells [1], the memory cell is expected to be stable for both the read and write cycles. While maintaining the static read and write margins, the selected transistor sizing present with conflicting constraints. During the read cycle, it is essential for read stability to increase the holding potential of the memory cell by strengthening the inverter pair and weakening the access transistors. While the opposite is required for a stable write cycle. Therefore, while designing the 6T SRAM cell, a delicate balance must be maintained with the cell ratios of the pull-down, pull-up, and access transistors. This inevitable design conflict gave rise to the development of several new SRAM designs and techniques to overcome the same.

The use of disassociation of the read and write ports to improve the noise margin during the read cycle led to development of designs such as the 7T [2],[3] and 8T SRAM [4],[5] cells. These have been important approaches to improve noise margins. Apart from isolation of ports for separate read and write cycles, several other concepts and techniques have been developed. These read and write assist techniques are applicable for improvement in the standard 6T cell, as well as can be applied on the isolated port structures to further improve the read and write stabilities. The techniques of Negative VSS [6], which decreases the GND potential even beyond zero volts, and Cell VDD boost [7], wherein the supply voltage is shot up above the normal limit of the cell greatly improves the read stability. Other possible methods are Lowered word line Voltage [8],[9], and Word-line under-drive (WLUD) [10], [11] that improve the read margins by reducing the strength of the access transistor.
Apart from such read assist techniques, various write assist techniques have also been proposed over the years. A few of them include the Transient Voltage Collapse (TVC) Write assist technique [10], the negative transient voltage technique [12], and the Asymmetrical floating cell virtual ground method [13].

Therefore, in this paper, a novel SRAM structure employing six transistors has been proposed that incorporates several of these concepts to improve upon the read and write abilities of the standard 6T cell. The paper has been divided as follows. The proposed architecture has been described in detail in Section II. Section II also covers the read, hold operation, and write operation of the presented architecture. The simulation results and discussions along with comparisons have been shown in Section III of the paper. Section IV concludes the paper with a summary of improvements over the conventional 6T cell.

2. PROPOSED DUAL PORT 6T SRAM ARCHITECTURE

The cell structure of the presented 6T SRAM architecture has been shown in Figure 1. The cell includes the pull-down nMOS pair (M1, M2), that act as the storage/drive transistors. The pair of pull-ups pMOS transistors (M3, M4) is used to access the memory for the write operation(dual-ended) as well as for the hold operation. The nMOS pair (M5, M6) is used to perform the single-ended read operation. The write wordline (WWL) and the bit-lines (BL and BL’) are used to perform the write operation. The separate read word line (RWL) and read bit-line (RBL) are used during the read operation. The detailed read, write and hold operations of the cell have been explained in the following sections.

![Fig. 1. Proposed Dual Port 6T SRAM Architecture.](image)

2.1. Hold and Read Ability of the proposed structure

The proposed architecture introduces a separate read stack (M5-M6), along with a separate read word line (RWL) and read bit-line (RBL). Therefore, the original word line structure is now reserved for the operation during the write cycle only. Hence, this new arrangement effectively eliminates any disturbance or noise during the read cycle. During the read cycle, RBL is precharged to $V_{DD}$, and RWL is asserted a logic value high. Assuming the cell stores a logic low i.e., $Q$ is at low and $Q'$ is charged to $V_{DD}$, the transistor M5 is activated, and switching of RWL activates the transistor M6 pulling down the RBL to zero reflecting the value stored in the cell as shown in Figure 2(a). Similarly, when a logic high is stored the node $Q'$ is at zero potential, the transistor M5 is operating in the cut-off mode and therefore, is unable to pull down the RBL keeping it steady at the precharged value and reflecting the logic high value stored in the cell shown in Figure 2(b). Next, the hold operation of the proposed structure, the concept of Word line under-drive has been introduced. In the proposed technique, pMOS access transistors (M3-M4) act as weak pull-ups by asserting WWL as $V_{DD} - |V_{TP}|$, instead of $V_{DD}$ during the hold operation. The weak pull-up pMOS access transistors substitute as loads during the hold state of the cell.
2.2. Write Ability of the proposed structure

The proposed structure performs a Dual-ended write operation without explicit load elements. For the write operation, assuming the case of writing logic high in the cell, initially, the internal nodes $Q$ and $Q'$ will be logic low & high, respectively. The transistors $M_1$ is in on state and $M_2$ is in cut-off state as seen in Figure 3 and WWL will be $V_{DD} - |V_{TP}|$. To write logic high, the bitline is charged to $V_{DD}$ and complementary Bit-line is discharged to zero. The WWL is asserted to a low value, turning the access transistors on, which allows $M_3$ to pull the node $Q'$ down to zero and $M_4$ to charge the node $Q$ to a logic high. The absence of load in the proposed structure makes it easier for $Q'$ to be pulled down to GND due to the lack of any opposing pull-up action.

Next, to write a zero-logic value, the transistor $M_1$ is in the cut-off state and $M_2$ is in the on state with internal nodes $Q$ and $Q'$ at logic high & low, respectively. Like the previous case, the bitline and Complementary Bitline are discharged and charged to write in the cell. The WWL is given logic low, allowing access transistor $M_3$ to pull down the node $Q$ down to zero and $M_4$ to pull up the node $Q'$ to a logic high. The absence of load in the proposed structure makes it easier for $Q$' to be pulled down to GND due to the lack of any opposing pull-up action.

3. RESULTS AND DISCUSSIONS

The Different SRAM Characteristics [14] of the proposed design and the conventional 6T SRAM Cell for comparison have been presented in this section. Initially, the butterfly curves for both the standard and proposed structure have been simulated to compare the stability metrics. Further, the variation of these metrics has been observed as a variation in threshold voltages and cell ratios. Apart from the stability metrics, N-Curve Analysis has been performed to determine several other parameters such as
Write Trip Voltage, Current Metrics, and Power Metrics. Finally, the transient simulation for verification of operation of the structure has also been presented. These simulations were carried out using Predictive Technology Model (PTM) 32nm file on HSpice.

3.1. Hold, Read and Write Static Noise Margin
In the proposed 6T structure, since the read operation is performed using a separate read stack and has no effect on the storage cross-coupled inverter pair, therefore the Hold and Read Static Noise margins are equivalent to each other. The Read SNM of the proposed structure comes out to be 0.388V, whereas it is 0.21V for the conventional 6T cell. The Hold SNM comes out to be 0.388V and 0.41V for the proposed and conventional 6T cells, respectively. Therefore, the proposed structure provides 84.76% improvement in read stability in contrast to the standard cell because of the disassociation of read and write ports, while maintaining a respectable hold noise margin as seen in Figure 4 and Figure 5. This eliminates the problem of the complex sizing of the conventional cell for optimal read and write operations.

The cross-coupled transistors can now be sized solely to improve the write margins without worrying about the implications on the read operation. The results for the write operation are shown in Figure 6. As discussed for the case of proposed structure since the storage cell is load less, therefore, the side writing logic low is experiencing no opposite force from the cross-coupled pair. Hence for the inverter side flipping from high to low the characteristics are completely at the zero-level indicating high stability of write operation in the cell. This is confirmed with the results obtained as 0.69V for the proposed cell showing an improvement of 40.81% compared to the 0.49V obtained for the conventional cell.

![Fig 4. Butterfly Curves for Hold Noise Margin Measurement](image1)

![Fig 5. Butterfly Curves for Read Noise Margin Measurement](image2)

3.2. Hold, Read and Write Static Noise Margin Variation with Threshold Voltage and Cell Ratio
The hold and read noise margins of the proposed structure have high dependency on the threshold voltages of the nMOS and pMOS due to the application of the concept of WLUD for the hold Operation. Therefore, it becomes imperative to check how the read and hold SNM vary with respect to the difference in threshold voltages(\(|V_{TN}| - |V_{TP}|\)). For the analysis, the threshold voltage of nMOS (M1, M2) was fixed at the default value as in the PTM model file and varied for pMOS (M3, M4) such that the difference in threshold voltages(\(|V_{TN}| - |V_{TP}|\)) varied from 0V to 0.3V. Also, to understand the effect of sizing in the proposed structure the analysis includes variation in size of nMOS Transistors (M1, M2).
Figure 7 shows the HSNM variation with respect to the difference in threshold voltages (|V_{TN}| - |V_{TP}|) for the conventional and proposed 6T structures. Initially for the proposed 6T cell, with an increase in the difference in threshold voltages the most optimized point was found at 0.05V where both pMOS and nMOS of the inverter became equally strong giving a sharper transition in the characteristics. On further increasing the difference in threshold, since the pMOS grows stronger the characteristics become asymmetric causing a decrease in SNM value. The conventional 6T cell has a similar variation curve as the proposed 6T cell as seen in Figure 7.

Similarly, Figure 8 shows the RSNM variation with respect to the difference in threshold voltages. The RSNM trend for the proposed 6T cell is the same as that of its HSNM. As it can be seen there is a major improvement in the RSNM value of the presented 6T cell in contrast to the standard 6T cell at all threshold voltages presented in the result. As discussed earlier, for the proposed structure the RSNM decreases when the difference in threshold voltage grows beyond 0.05V value. While, in the standard 6T cell, the RSNM value increases with the increase in difference in threshold voltages, however, the major improvement in the RSNM values still exists. Finally, the effect of different cell ratios for the conventional and the proposed structure shows that as the nMOS transistor size increases, the SNM plots shift upwards indicating an overall increase in the parameters at all threshold voltages analyzed.
3.3. N-Curve Stability Metrics
Along with the Static noise margins, the N-curves further provide several different parameters to study various aspects of the cell like power metrics, current metrics and Write Trip Voltage. The setup for extraction of N-Curve has been shown in Figure 9. The source $V_{IN}$ is swept from GND to $V_{DD}$ and the current $I_{IN}$ is observed as a variation in $V_{IN}$.

![N-Curves](image)

**Fig 10. N-Curves with variation in Cell Ratio (a) Proposed 6T Cell (b) Standard 6T Cell.**

The N-Curve intersects the voltage axis three times— A, B & C (in order of intersection) which are determined by the ratios of various transistors. In the case of the conventional architecture, the first point (A) is determined by the Bit cell ratio, similarly, the second point (B) is dependent on both the pull-up and bit cell ratio and the third point (C) solely dependent on the pull-up ratio. However, in the case of the proposed cell, due to absence of the pull-up load transistors, the first point is dependent on the ratio of $M1(M2)$ to $M4(M3)$ and the same for the second point. However, the third point is only dependent on the pass transistor sizing. The current and voltage noise margins and write trip points are defined using these points. To characterize read stability, the Static Voltage Noise Margin (SVNM) and Static Current Noise Margin (SINM) metrics are used. The SVNM and SINM are defined as the maximum tolerable DC voltage and current noise at the internal nodes before the contents flip. The SVNM is computed as the potential difference between the points B and point A. SINM measured as a peak current located between points B and A. Similarly, for write operation, the Write Trip Voltage (WTV) i.e., the minimum voltage to flip the cell contents, is calculated as the voltage difference between points C and B. Write Trip Voltage (WTI), being the minimum current required to flip cell contents, is measured as the negative current peak between point B and C.

Initially, as the $V_{IN}$ is swept from GND to $V_{DD}$, the access and pull-down transistors of the proposed structure are active in the saturation and linear mode respectively, like the conventional 6T cell. However, as the first peak is crossed, the pull-up transistors of standard 6T cell get activated thus reducing the current $I_{IN}$ and all the pass, pull-down, and pull-up transistors go to saturation. But in the proposed scheme due to the absence of pull-up transistors, the $I_{IN}$ decreases at a slower rate pushing the point further away, thereby, increasing the SVNM and decreasing the WTV, and improving the parameters. Similarly, after crossing the negative peak, in the standard 6T, the pull-up and access transistors operate in linear modes and the pull-down transistor in the cut-off region. Whereas, in the proposed structure, $M4$ is the only transistor in linear mode. Thus, it draws current and slowly decreases it to zero with an increase in $V_{IN}$; therefore, explaining the results as in Figure 10(a) & 10(b).

Additionally, parameters derived from the N-Curves have been plotted in Figure 11 to map out the comparison with the standard scheme. The SVNM and SINM are desired to be as high as possible while the WTV and WTI are desired to be as small as possible. Therefore, as shown, the Voltage metrics for the presented structure are much better than the standard one with SVNM being...
significantly higher and WTV being significantly lower. While the current metrics do not show much improvement compared to the standard 6T Cell, they remain as good as the standard 6T Cell. The trends however mostly remain the same i.e., with an increase in the sizing of nMOS transistors for both cases the SVNM, SINM, WTV, and WTI show the same variations. Along with these the power stability metrics were extracted using area under the N-Curves. For better power stability SPNM is desired to have a larger value and WTP a smaller Value. Therefore, the introduced structure shows improvement in both as can be seen in Figure 11(c).

![Fig 11. Parameters Extracted from N-Curve (a) Voltage Metrics: SVNM, WTV (b) Current Metrics: SINM, WTI (c) Power Metrics: SPNM, WTP.](image)

### 3.4 Transient Operation and Dynamic Stability

During the write cycle, the pMOS pass transistors also act like load for the storage unit, hence a misconception may arise if the newly written value can be held on while the pMOS transistor switches from access to hold mode. Therefore, the transient operation for the write cycle followed by the hold cycle has been shown in Figure 12. It can be seen initially the storage nodes are holding an ambiguous value. In the first write, the BL is lowered to GND and simultaneously WWL is asserted a low to activate the pass transistors. Immediately the internal storage nodes Q and QB flip to the respective values and as WWL is disserted the cell holds the contents of the storage nodes. Similar can be seen when WWL is asserted and a write ‘1’ operation is performed.

Next, the dynamic stability for write operation is presented in Figure 13 to determine the minimum pulse width of WWL for a fast and successful operation. The pulse width at which the write operation may fail has also been calculated using the same. As shown in the results, for a pulse width less than 8.5ps, the write operation is not successful and 25ps is the minimum pulse width before which the storage nodes Q and QB flip just before WWL is disserted. Therefore, the critical time for write
operation is defined in the range of 8.5ps and 25ps. However, if the pulse width is chosen less than 25ps for the proposed structure since the pull-up is very weak, the charging time for Q and QB becomes very high. Hence, it is recommended that the cell contents are written with a WWL signal pulse width of at least 25ps for a stable write operation.

![Fig 12. Transient Operation of the Proposed 6T Cell](image1)

![Fig 13. Dynamic Stability of Write Operation](image2)

4. CONCLUSION

In this paper, a novel dual-port 6T SRAM Cell was presented that shows improvement in read and write abilities from the standard cell. The structure uses four transistors for the storage and access of the cell. The other two transistors comprise the read stack for improved read abilities. The technique of word line underdrive for improved hold operation has also been used in the presented design.

To verify the efficacy of the presented design, the characteristics were simulated on the 32 nm PTM CMOS technology node and the results were compared with the standard 6T SRAM cell. Different metrics such as the HSNM, RSNM, WNM, WTV, SVNM, SINM, WTI, SPNM, WTP and write dynamic stabilities were measured. The proposed design proves to give an 84.76% improvement in the read stability and a 40.81% improvement in the write ability over the conventional SRAM cell. The proposed design is capable of writing at a very high frequency as the minimum pulse width of WWL for a successful write operation was determined to be 25ps. However, the design does lose out slightly in the hold margins by 5.67%. Although the simulations have been performed on 32nm CMOS technology node, it is expected that the advantages of the proposed 6T design will also be present in smaller technology nodes.

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