An Exhaustive Approach to Detecting Transient Execution Side Channels in RTL Designs of Processors

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Abstract—Hardware (HW) security issues have been emerging at an alarming rate in recent years. Transient execution attacks, such as Spectre and Meltdown, in particular, pose a genuine threat to the security of modern computing systems. Despite recent advances, understanding the intricate implications of microarchitectural design decisions on processor security remains a great challenge and has caused a number of update cycles in the past.

This paper addresses the need for a new approach to HW sign-off verification which guarantees the security of processors at the Register Transfer Level (RTL). To this end, we introduce a formal definition of security with respect to transient execution attacks, formulated as a HW property. We present a formal proof methodology based on Unique Program Execution Checking (UPEC) which can be used to systematically detect all vulnerabilities to transient execution attacks in RTL designs. UPEC does not exploit any a priori knowledge on known attacks and can therefore detect also vulnerabilities based on new, so far unknown, types of channels. This is demonstrated by two new attack scenarios discovered in our experiments with UPEC.

UPEC scales to a wide range of HW designs, including in-order processors (RocketChip), pipelines with out-of-order writeback (Ariane), and processors with deep out-of-order speculative execution (BOOM). To the best of our knowledge, UPEC is the first RTL verification technique that exhaustively covers transient execution side channels in processors of realistic complexity.

Index Terms—Hardware security, formal verification, transient execution attacks, timing side channels, microarchitecture.

I. INTRODUCTION

The discovery of Spectre [1] and Meltdown [2] has led to a number of recent product updates in industry, targeting both the hardware (HW) and the software (SW) of computing systems. The variety of attacks discovered in the past years, from MDS attacks (e.g., [3]) to Speculative Interference [4], with many of them attacking a previously patched system (e.g., Fallout attack [3]), proves that transient execution side channel (TES) attacks can pose a substantial security challenge. TES attacks exploit side effects of transient instruction execution, a phenomenon which is not visible in the sequential execution semantics of the ISA. While transient instructions are not part of the correct flow of the program, the processor still executes them but later discards their result, e.g., due to a mispredicted branch.

Software-level patches, such as in [5], are crucial for fixing legacy systems, but they are not a panacea. Lack of concrete knowledge about the root cause of the problem can lead to SW being patched based on the known attacks, potentially rendering systems vulnerable to future attacks (see, e.g., the case of speculative store bypass attack [6]). Alternatively, SW may be fixed conservatively, preventing also future attacks, however, at the cost of possibly prohibitive performance overhead (up to 200% [7]).

Compared to SW-only patches, enhancing security also at the HW level is the more favorable protection against TES attacks in the long run. Besides improving the performance overhead [8], microarchitectural countermeasures can relieve the SW developer from having to consider HW details in security analysis.

A variety of microarchitectural security patches have been proposed by the research community. Although the achieved protection and the performance of these techniques can be easily evaluated on abstract models (e.g., using the gem5 simulator [9]), the security guarantee can, eventually, only be delivered at the Register Transfer (RT) level. As observed in the Speculative Interference [4] and Spectre-STC attacks (cf. Sec. II-B), certain vulnerabilities are introduced into the system due to specific Register Transfer Level (RTL) details. In addition, the performance requirement for the microarchitectural security patches leads to more and more complex design techniques making the design prone to new vulnerabilities at the RTL.

A. Contributions

We propose a formal security verification approach for HW, called Unique Program Execution Checking (UPEC), which fully covers the class of TES attacks. UPEC is applicable to RTL designs in a wide range of complexity, from simple processors with in-order pipelines to deep out-of-order speculative execution processors. Given a confidentiality requirement, UPEC either certifies the security of the design w.r.t. this requirement, or it automatically generates a counterexample.
pointing to possible vulnerabilities. The outline of the paper and its key contributions are as follows:

(I) We provide new insights into TES attacks (Sec. III). Through experimental evidence, we show that TESs are possible not only in high-end processors with advanced features, such as out-of-order (OOO) and speculative execution. They can also exist in simple in-order processors and can be introduced by low-level design decisions.

(II) We propose formal definitions for microarchitectural vulnerabilities causing confidentiality violation in HW through explicit or implicit information flows (Sec. IV). The definitions, unlike previous works, consider a concrete microarchitecture on the RTL and do not restrict the leakage to known side channels such as cache footprint. As a result, they also cover so far unknown TES attacks.

(III) This paper proposes UPEC as a structured and systematic formal methodology for HW security verification targeting all TES attacks in RTL processor designs (Secs. V and VI). The proposed method is exhaustive and provides security guarantees without requiring a radically different design methodology or expert knowledge about different classes of microarchitectural attacks. UPEC therefore can be easily integrated into existing design flows and can serve as a basis for HW security verification sign-off at the RT level.

(IV) The paper introduces the notion of microequivalence which is key in making UPEC scalable to processors with out-of-order and speculative execution features (Sec. VII).

(V) The effectiveness of the UPEC approach is shown by verifying various RTL designs with different levels of complexity (Sec. VIII). In our experiments, by merit of the exhaustiveness of our approach, previously unknown vulnerabilities have been found in RocketChip [10], Ariane [11] and BOOM [12]. The reported runtime of UPEC confirms the scalability of the approach to processors of realistic size.

(VI) A sophisticated re-design of the BOOM processor is beyond the scope of this paper. However, we developed a fully verified secure variant of the BOOM processor based on conservative fixes, which is published as an open source design on GitHub [13]. Although the design does not deliver competitive performance, it serves well as a demonstration that RTL sign-off verification regarding TES attacks is doable for large processors. To the best of our knowledge, this is the first example of a deep OOO processor with a well-defined security guarantee against transient execution side channel attacks.

New HW/SW contracts have also been developed in [20] as a framework to reason more precisely about what information HW leaks and what consequences this has for SW security requirements. This provides a useful framework to reason about security at the SW level, without leaving a gap due to certain microarchitectural features. However, it has not yet been examined how the HW side of the high-level contracts can be mapped to the RTL implementation by RTL properties and whether these properties scale for state-of-the-art commercial property checking.

Cabodi et al. [21] present one of the first HW security verification approaches targeting speculative attacks. It extends over their previous work [22] and the work of [23], pioneering the adoption of taint analysis in the HW domain. Hu et al. [24] also proposed a model for precise taint propagation and taint property verification. It is, however, in the nature of taint analysis that it requires assumptions on the paths to be analyzed. As a result, such approaches can be effective in checking a design for known variants of Spectre, but face their limitations with respect to unknown variants. Furthermore, proving taint properties for paths of unknown temporal length can be prohibitively complex, and restricting the proof to a feasible temporal upper-bound limits the detection capability of the method.

The formal approaches known as InSpectre [25], CheckMate [26] and the verification techniques based on UCLID5 [27] evaluate the security of HW designs on abstract models. InSpectre [25] proposes an abstract execution semantics to formalize security against TES attacks. This abstract formalization is different from the TES properties formulated in this paper, because it lacks the RTL semantics of the processor model. Design verification based on high-level models can provide important insights into the design. However, it cannot provide the final sign-off verification which always uses cycle-accurate RTL as the point of reference.

Also techniques based on HW fuzzing bear promise, such as IntroSpectre [28] and HyperFuzzing [29]. Their non-exhaustive nature, however, does not allow them to deliver formal guarantees when signing off a design.

III. NEW TES ATTACKS

A. ORC Attack

For reasons of performance, many cache designs employ a pipelined structure which allows the cache to receive new requests while still processing previous ones. However, this can create a Read-After-Write (RAW) Hazard in the cache pipeline, if a load instruction tries to access an address for which there is a pending write.

A straightforward HW solution employs a hazard detection unit which checks for every read request whether or not there is a pending write request to the same cache line. If so, all read requests are removed until the pending write has completed. The processor pipeline is stalled, repeating to send read requests until the cache interface accepts them.

In the following, we show an example how such a cache structure can create a security vulnerability allowing an attacker to open a TES. Let’s assume we have a computing

II. RELATED WORK

Cheang et al. [14] formally defined Secure Speculation as an observational determinism property over four traces. A related approach was proposed by [15], who formalized Speculative Non-Interference as the requirement for security against speculative execution attacks. These techniques can be effective in verifying software by extending the ISA semantics to a speculative semantics. However, these and related works, such as [17], [18], do not take the microarchitecture into account and are not meant to verify the security of HW. Adopting SW security concepts to HW verification is not trivial, as shown for the example of constant time execution by [19].
system with an in-order core pipeline, a cache with write-back/write-allocate policy and the RAW hazard resolution just described. In the system, some confidential data (secret data) is stored in a certain protected location (protected address). We assume that the cache holds a valid copy of the secret data (from an earlier execution of privileged code). We also make the simplifying assumption that each cache line holds a single byte, and that a cache line is selected based on the lower 8 bits of the address of the cached location. Hence, in our example, there are a total of $2^8 = 256$ cache lines.

The basic mechanism for the Orc attack is the following. Every address in the computing system’s address space is mapped to some cache line. If we use the secret data as an address, then the secret data also points to some cache line. The attacker program “guesses” which cache line the secret data points to. It sets the conditions for a RAW hazard in the pipelined cache interface by writing to the guessed cache line. If the guess was correct then the RAW hazard occurs, leading to a slightly longer execution time of the instruction sequence than if the guess was not correct. Instead of guessing, of course, the attacker program iteratively tries all 256 possible cache locations until successful.

Fig. 1 shows the instruction sequence for one such iteration. The sequence attempts an illegal memory access in instruction #5 by trying to load the secret data from the protected address into register x4. The processor correctly intercepts this attempt and raises an exception. However, before control is actually transferred, instruction #6 has already entered the pipeline and has initiated a cache transaction. The cache transaction has no effect on the architectural state of the processor. But the execution time of the instruction sequence depends on the state of the cache. When probing all values of #test_value, the case will occur where the read request affects the same cache line as the pending write request of instruction #4, thus creating a RAW hazard and a stall in the pipeline. It is this difference in timing that can be exploited as a side channel.

This new covert channel can be illustrated at the example of the RISC-V Rocketchip [10]. The original Rocketchip design is not vulnerable to the Orc attack. However, with only a slight modification (17 lines of code (LoC) in an RTL design of $\sim 250,000$ LoC) and without corrupting the functionality, it is possible to insert the vulnerability. The modification actually optimizes the performance of the design by bypassing a buffer in the cache such that an additional stall between consecutive load instructions with data dependency is removed.

The Orc attack presented above is based on the interface between the core (a simple in-order core in this case) and the cache. This provides the insight that the orchestration of component communication in an SoC, such as RAW hazard handling in the core-to-cache interface, may also open or close covert channels.

The described vulnerability is a very subtle one, and unlike Meltdown and Spectre, it is feasible in an in-order non-speculative pipeline.

B. Spectre-STC

Spectre-STC is a new speculative transient execution attack which demonstrates that single-threaded processors can be vulnerable to contention-based Spectre attacks.

In BOOM, the ALU, the multiplier and the division unit use the same write port to access the register file. In case of contention, there is a fixed-priority arbitration, in which the ALU has the highest and the division unit the lowest priority, regardless of the program order. This means that a division instruction can be delayed by a younger multiply or add instruction due to port contention, which is exploited by Spectre-STC.

Fig. 2 shows a hypothetical gadget for the Spectre-STC attack. The basic idea is to start a division before the transient execution, and then, in the transient time window, using a secret-dependent branch, perform multiplications and additions (and create port contention) if the secret is equal to a probing value. The attacker can probe the secret (line 4) by measuring how long it takes to execute the gadget code.

This TES demonstrates that seemingly innocuous choices on RTL implementation details, in this case on how to resolve the port contention between two functional units, can introduce a vulnerability to a Spectre-style attack.

Similarly as Spectre-STC, the research works on Speculative Interference [4] and SpectreRewind [30] discovered independently that a secret-dependent branch instruction within the transient sequence can be exploited as TES. In those attacks, the vulnerability is created by high-level architectural features based on multi-cycle operations in non-pipelined functional units. Spectre-STC, discovered automatically by analyzing the RTL description of BOOM, reveals that such vulnerabilities can have root causes other than non-pipelined functional units.

IV. UNIQUE PROGRAM EXECUTION CHECKING (UPEC)

In this section, we propose a mathematical definition for Unique Program Execution and refine the formulation such that it exclusively targets the class of TES attacks. Since UPEC shall be applicable to design implementations at the RTL, all elements of the following definitions directly relate to components of a CPU’s microarchitecture.

The contents of the program-visible registers and data memory (including cache) are assumed to be partitioned into two
sets: a set of public information, \( X_p \), and a set of confidential information, \( X_c \). A program \( P \) is the content of instruction memory together with a start address and an end address. It receives \( X_c \) and \( X_p \) as its inputs. In the microarchitectural implementation of our system, we consider a microarchitectural state \( S \), which is defined for all state bits other than those holding the inputs, \( X_p \) and \( X_c \), to the program. \( S_0 \) is the initial (starting) state for executing a program \( P \). We distinguish the following notions:

**Definition 1** (Architectural Observation). The architectural observation \( O(P, X_p, X_c) \) of a program \( P \) is the (time-abstract) sequence of valuations to the program-visible (architectural) registers, as they are produced by committing instructions according to the ISA specification. 

The architectural observation is independent of any hardware implementation of the ISA and does not relate to any microarchitectural features such as cache or pipelining. It can be seen as the result of simulating the program by an ISA simulator.

**Definition 2** (Microarchitectural Execution). The microarchitectural execution \( \xi(S_0, P, X_p, X_c) \) of a program \( P \) is the (clock-cycle-accurate) sequence of valuations to the program-visible (architectural) registers, as they are produced during execution of \( P \) on a specific hardware implementation/microarchitecture.

The microarchitectural execution can be seen as the clock-cycle-accurate result of simulating the program on the HW design using an RTL simulator.

**Definition 3** (Microarchitectural Observation). The microarchitectural observation \( \mu(S_0, P, X_p, X_c) \) of a program \( P \) is the (time-abstract) sequence of valuations to the program-visible (architectural) registers, as they are produced by committing instructions on a specific hardware implementation/microarchitecture.

In this definition, committing instructions are those instructions that finish their execution and leave the pipeline, i.e., they have written to the program-visible registers. The microarchitectural observation can be obtained from the microarchitectural execution by keeping in the sequence all valuations to the architectural registers at the time points they are written (due to instruction commitment) and discarding all other “intermediate” valuations. For a functionally correct microarchitecture, for any tuple \((P, X_p, X_c)\), the microarchitectural and architectural observation are the same.

Using these notions we can now formulate **Unique Program Execution** which is the security requirement for an SoC to provide the root of trust for confidentiality.

**Definition 4** (Unique Program Execution). A program executes uniquely w.r.t. a set of confidential information \( X_c \) if and only if the sequence of valuations to the set of architectural state variables is independent of \( X_c \), in every clock cycle of program execution.

We can use this notion to formulate the requirement for confidentiality as a trace property:

\[
\forall P, S_0, X_p, X_c, X_c' : \\
O(P, X_p, X_c) = O(P, X_p, X_c') \\
\Rightarrow \xi(S_0, P, X_p, X_c) = \xi(S_0, P, X_p, X_c') \quad (1)
\]

The property is a “non-interference property” which considers an arbitrary program running for different sets of secret data, \( X_c \) and \( X_c' \). It states that if differences in the secret data do not change the results of the program, as defined by the ISA level specification, then its cycle-accurate execution for the program-visible registers of the microarchitectural implementation must not depend on the secret either.

It is helpful to distinguish between confidentiality violations caused by transient execution side channels (TESs) and functional leakages. The latter are not caused by timing side channels but by conventional design bugs violating the functional (ISA) specification of the system such that confidentiality is compromised. UPEC covers both types of confidentiality violations. A functional leakage is a counterexample not only to the property of Eq. 1 but also to the following, weaker property:

\[
\forall P, S_0, X_p, X_c, X_c' : \\
O(P, X_p, X_c) = O(P, X_p, X_c') \\
\Rightarrow \mu(S_0, P, X_p, X_c) = \mu(S_0, P, X_p, X_c') \quad (2)
\]

This means, when targeting functional leakages, we do not consider the detailed timing behavior of the HW implementation. We only need to check if the actual content of the program-visible registers can be influenced by secret data. Functional leakages, in principle, can be identified by any functional verification technique, such as conventional property checking or functional simulation. Unfortunately, conventional verification techniques are not always effective for this purpose. This motivates the work in [31] where the potential of UPEC in detecting functional confidentiality violations is examined further. This paper, however, is dedicated to TES-based confidentiality violations.

A TES attack is a counterexample to the following trace property. It results from Eq. 1 by excluding functional leakages from consideration:

\[
\forall P, S_0, X_p, X_c, X_c' : \\
\left[ O(P, X_p, X_c) = O(P, X_p, X_c') \land \\
O(P, X_p, X_c) = \mu(S_0, P, X_p, X_c) \land \\
O(P, X_p, X_c') = \mu(S_0, P, X_p, X_c') \right] \\
\Rightarrow \xi(S_0, P, X_p, X_c) = \xi(S_0, P, X_p, X_c') \quad (3)
\]

It should be noted that this property verifies a concrete HW considering any possible SW for both the attacker process and the underlying operating system. This is different from SW verification approaches (e.g., [14, 16, 17, 18]) which always consider a concrete kernel SW that must be verified to be secure against TES attacks.

Consider a transient execution attack, given as a counterexample \((S_0, P, X_p)\) to the trace property of Eq. 1 executing a
concrete instruction sequence $A$ on the processor. The attack is called a Spectre attack if there exists a sub-sequence of $A$ called $A_{\text{victim}}$ such that $A_{\text{victim}}$ is executed under an execution context with the proper privilege to access some confidential program input $X_c$, without an exception being raised. Otherwise, if no such $A_{\text{victim}}$ exists, the attack is called a Meltdown attack.

The counterexample to the above trace property is not necessarily the complete attack vector, but rather can be the critical part of the attack exfiltrating the secret and creating the covert channel. For example, the part of the Spectre attack which poisons the branch prediction unit (by bad training) can be excluded from $P$ and can be implicitly represented by $S_0$.

Remember, $S_0$ defines the valuation to all state bits other than those holding $X_p$ and $X_c$. The use of the same $S_0$ in both traces excludes classical timing side channels from consideration, i.e., side channels which are not based on transient executions. Those rely on exploiting a specific victim SW, such as an encryption SW, whose footprint would need to be represented by a difference between initial states of the two traces.

For the remainder of this paper, it is helpful to observe that any valid counterexample to the property in Eq. 3 fulfills the following condition:

$$\mu(S_0, P, X_P, X_c) = \mu(S_0, P, X_P, X'_c)$$

This condition is referred to as microequivalence in the following sections.

V. UPEC ON A BOUNDED MODEL

Proving the property of Eq. 1 by generic unbounded model checking is infeasible for SoCs of realistic size. Therefore, we develop a SAT-based approach which is tailored towards the properties considered in UPEC. Our approach is based on "any-state proofs" in a bounded circuit model. It is related to a variant of Bounded Model Checking (BMC) called Interval Property Checking (IPC) which is applied to the UPEC problem in a similar way as in [35] for functional processor verification.

The property of Eq. 1 relates two separate execution traces for a given program and initial microarchitectural state to each other. Consequently, in our IPC-based approach, we use a computational model that consists of two identical instances of the SoC under verification, $SoC_1$ and $SoC_2$, that each run an execution trace. In the terminology of SW verification, UPEC pursues an approach based on 2-safety hyperproperties. A 2-safety formulation provides similar benefits for UPEC as for information flow and taint property verification. In HW equivalence checking the underlying self-compositional model is widely referred to as “miter” [38], [39]. Owing to the resemblance of UPEC with HW equivalence checking we refer to the UPEC computational model as “miter for side channel detection”.

In the rest of the paper, without loss of generality, we assume that $X_c$ resides in the data memory, unless otherwise noted. Verifying the SoC for confidentiality of information in the register file is analogous.

Assume:

at $t$: $micro\_soc\_state_1 = micro\_soc\_state_2$;

at $t$: $public\_mem_1 = public\_mem_2$;

during $t..t+k$: $secret\_load\_speculative()$;

Prove:

at $t+k$: $soc\_state_1 = soc\_state_2$;

Fig. 4. Unrolled miter for side channel detection.

A. UPEC Interval Property

Fig. 3 shows the UPEC property formulated as an interval property. It is proven on the unrolled miter model depicted in Fig. 4. In this property, $micro\_soc\_state$ is the vector of all state variables inside the SoC, excluding those parts of memory that hold the public information $X_P$ and the confidential information $X_c$. The state variables of memory and cache holding $X_P$ are denoted with $public\_mem$ in the UPEC property.

Similar to Eq. 1, the first two assumptions of the property guarantee that both SoC instances execute the same, arbitrary, program and that the only difference between the two execution traces at the start state is the set of secret data. Since microarchitectural behavior at the RTL is deterministic, including that of cache eviction and branch prediction, any discrepancy between the state of $SoC_1$ and $SoC_2$ that may occur in later clock cycles is due to the propagation of the secret.

For a productive verification methodology, we need to avoid formulating the property with reference to the architectural observation of a program, since this would require formalizing the ISA. Instead, we formulate two constraints $secret\_data\_protected$ and $secret\_load\_speculative$. They are expressed in terms of the considered execution traces, and serve the purpose of taking into account only traces with the same architectural observation, without actually specifying the ISA.
The macro `secret_data_protected` states that a HW protection mechanism is enabled to protect the memory locations holding $X_c$. This means that, provided that the protection mechanism is implemented correctly, any access to the secret within a user-level process is blocked by an exception. This allows for considering Meltdown-style attacks (according to Sec. [IV]). The macro `secret_load_speculative` assumes that any access to $X_e$ within an OS-level process happens transiently and is discarded before it commits. This allows for considering Spectre-style attacks (according to Sec. [IV]). These macros can be easily refined for any given microarchitecture based on the memory protection logic and pipeline signals controlling the speculation level. More detail on their implementation for the example of the BOOM processor can be found in [13]. With the help of the macros `secret_data_protected` and `secret_load_speculative`, only execution traces are considered in which any access to $X_e$ is either blocked by an exception or discarded due to an earlier exception or misprediction. Since all other sources of instruction operands are the same between the two instances, the two execution traces considered by the property always yield the same architectural observation.

Although the macros guarantee a secret-independent architectural observation, it is important to understand that the described macros do not over-constrain the interval property compared to the property of Eq. 1. In any execution trace that violates `secret_data_protected` or `secret_load_speculative`, the system executes a load instruction targeting the secret that becomes visible as part of the architectural observation, since the instruction is neither misspeculated nor blocked by an exception. Consequently, the architectural observation is secret-dependent which is a violation of the assumption in Eq. 1. It should also be noted that `secret_data_protected` and `secret_load_speculative` macros do not provide a global constraint on the system, but rather constrain program execution within the property time window between $t$ and $t + k$. The system is still free to execute any program, even the ones violating the macros, in the clock cycles before $t$. This is taken into account by considering any microarchitectural state as the starting state of the program execution for the trace property of Eq. 1 and the interval property of Fig. 3.

As in any IPC proof, UPEC may return spurious counterexamples due to considering unreachable starting states at the beginning of the interval. This is addressed in the usual way by strengthening the property using invariants. Since program execution is unique also in most unreachable states, only little effort is caused in UPEC to create the needed invariants, detailed in [40].

In the `prove` part of the property, `soc_state` is a vector of state variables which includes all architectural (program-visible) state variables, as required by Eq. 1, but additionally it can also include some or all other microarchitectural state variables. Observing also non-architectural registers is a key concept in UPEC which serves to obtaining an unbounded and scalable proof method. This will be further developed in the following subsections.

### B. Counterexamples to the UPEC Property

For a full proof of the UPEC property on the bounded computational model of Fig. 4 in principle, we need to consider a time window as large as the sequential depth, $d_{soc}$, of the examined SoC. This is infeasible in most practical cases. Fortunately, employing a symbolic initial state allows the solver to often capture hard-to-detect vulnerabilities within much smaller time windows.

Any information leakage starts with the propagation of confidential information into some microarchitectural register. As a result, if we include every microarchitectural state variable in `soc_state`, the any-state proof on our bounded model guarantees detection of any violation of this UPEC property in only a single clock cycle. This is due to the fact that the symbolic initial state of the proof includes, as a subset, all possible reachable states.

However, unique program execution only requires that the secret data must not be observable through the architectural state variables. Therefore, proving that the secret data cannot propagate to any state variable in a superset of the architectural state variables represents a sufficient but not a necessary condition for certifying confidentiality.

We therefore distinguish two kinds of “alerts” to the UPEC property. In the following discussion, an alert $a_k$ is a counterexample of length $k$ to the UPEC property where `soc_state1` $\neq$ `soc_state2` in the ending state, i.e., at time $k$.

#### Definition 5 (L-alert).
An alert, $a_k$, is called a leakage alert (L-alert) iff the differing state variables of `soc_state1` and `soc_state2` include architectural state variables.

L-alerts demonstrate how secret data can affect the sequence of architectural states. Two cases can be distinguished. In the first case, secret data propagates directly into an architectural register, i.e., the microarchitectural observation is changed. If this happens the design contains a functional bug. In the second case, the problem is more subtle. The secret changes the timing and/or the values of the sequence without violating the functional design correctness and without leaking the secret directly. In other words, it changes the microarchitectural execution without affecting the microarchitectural observation. UPEC detects the HW vulnerability in both cases.

#### Definition 6 (P-alert).
An alert, $a_k$, is called a propagation alert (P-alert) iff the differing state variables of `soc_state1` and `soc_state2` are not architectural state variables.

P-alerts show possible propagation paths of secret data from the cache or memory to program-invisible, internal state variables of the system, such as pipeline buffers. Hence, no secret data is leaked. However, a P-alert can be a precursor to an L-alert, because the secret often traverses internal, program-invisible buffers before it is propagated to an architectural state variable like a register in the register file. In fact, any L-alert that is not (yet) visible within the time window of the unrolled model has one or more shorter precursor P-alerts that are. Based on this observation, we realize that proving the absence of P-alerts and L-alerts within one clock cycle in an any-state proof is sufficient for verifying confidentiality. In
the following section, we present the UPEC methodology for verifying systems that do not fulfill this sufficient condition for confidentiality.

VI. UPEC VERIFICATION METHODOLOGY

A. Modeling the Propagation of Secrets

In the UPEC verification methodology, P-alerts provide valuable information on the “locations” to which secret information can propagate.

Definition 7 (P-location). For a P-alert $a_k$ the P-location, $Ploc(a_k)$, is the set of all microarchitectural state variables of the SoC whose values in the ending state of $a_k$ (at time point $k$) depend on the secret, i.e., whose valuations differ between the SoC instances 1 and 2.

In the following, we use P-locations to distinguish different scenarios of secret information flows. In our proof method, the P-locations are represented by Boolean state predicates.

Definition 8 (P-location Predicate). A P-location predicate, $\Lambda_P$, for a set of microarchitectural state variables, $P$, is a state predicate over all microarchitectural variables of the miter, given as a conjunction of equalities and inequalities of corresponding variables in the SoC instances 1 and 2:

$$\Lambda_P = \prod_i(v_{i,1} \neq v_{i,2}) \cdot \prod_j(w_{j,1} = w_{j,2})$$

specifies

- inequality for every variable $v_i \in P$, and
- equality for every other variable $w_j \notin P$.

A P-alert $a_k$ satisfies its P-location predicate $\Lambda_P$ with $P = Ploc(a_k)$ at time point $k$, i.e., in its ending state.

Using these notions, we can collect and enumerate all possible locations in the SoC to which secret information can propagate in $k$ clock cycles. Similar to an all-SAT enumeration, after finding a P-alert $a_k$, a blocking clause is added to the property preventing the solver from generating another counterexample fulfilling the same $\Lambda_P$, i.e., reaching the same P-location.

In the following, we will use the complete set of P-locations to decompose the UPEC proof problem into scalable subproblems. Before this idea is elaborated, we introduce a cone-of-influence reduction for UPEC, as an additional optimization for the proof procedures to be presented.

B. Cone-of-Influence Reduction

Cone-of-influence reduction is a well-known technique for reducing the complexity of proof tasks in formal verification by structurally removing parts from the computational model that are irrelevant for the proof at hand. In the original UPEC interval property of Fig. 3, however, the prove part includes every state variable in the design; as a result, the unrolled model cannot be simplified by the solver through cone-of-influence reduction.

Fortunately, this changes when we decompose the problem, as presented in the following subsection. In the decomposed UPEC proof on a bounded model we are interested in finding P-alerts and L-alerts of a specific length $k$ while the precursor

UPEC_Base ($P$, $k$, blocking_clause):

assume:

- at $t$: $micro\_soc\_state_1 = micro\_soc\_state_2$;
- at $t$: $public\_mem_1 = public\_mem_2$;
- at $t$: $secret\_data\_protected();$
- during $t..t+k$: $secret\_load\_speculative();$
- at $t+k-1$: $\Lambda = true$;
- at $t+k$: $blocking\_clause = true$;

prove:

- at $t+k$: $Alert\_candidate_{P_1} = Alert\_candidate_{P_2}$;

Fig. 5. UPEC property for induction base procedure

P-alerts and their P-locations $Ploc(a_{k-1})$ are known. Therefore, only the subset of next-state variables that lie in the fanout of the given locations need to be considered as the possible candidates for a new alert.

Definition 9 (Alert Candidate). $Alert\_candidate_{P}$ is the set of state variables of the SoC which are in the immediate fanout cone of $P = Ploc(a_{k-1})$.

We can use the set $Alert\_candidate_{P}$ to simplify the proof obligation for the property of Fig. 5. Assuming $a_{k-1}$ is a P-alert of length $k-1$, for the UPEC proof of length $k$, we can replace $soc\_state$ in the prove part of the property with $Alert\_candidate_{P}$. This helps the solver in many cases to conduct an effective cone-of-influence reduction.

C. Iterative UPEC Proof Procedure

The any-state proof of UPEC guarantees to find all P-alerts of a given temporal length, if the model is unrolled for the corresponding number of clock cycles. As already observed in Sec. V-B, any P-alert $a_k$ with $k > 1$ has a pre-cursor P-alert $a_{k-1}$, which explains how the secret propagates to SoC variables in the immediate fanin variables of $Ploc(a_k)$. This information can be used to guide the solver towards the next counterexamples and mitigate the computational complexity of the proof by decomposing the UPEC proof into simpler steps.

In our general procedure, we enumerate P-alerts by starting with the ones for $k = 1$, and then incrementing $k$ until no new alerts are found. We decompose each UPEC proof for a particular $k$ along the different precursors for P-alerts, by enumerating all P-locations reached within $k-1$ clock cycles. The proposed decomposition does not violate the completeness of the proof, since the any-state proof on the $k-1$ clock cycle time window guarantees finding all possible P-alerts of that length and, hence, every counterexample to the UPEC property is covered by a P-location computed by the proof procedure.

Fig. 3 shows the UPEC property used in our iterative procedure. The property receives a P-location $P$, as reached by a precursor P-alert, and verifies whether the secret can propagate further and produce a new alert. The property also receives a blocking clause which prevents the solver from generating the same counterexamples again when calling the proof procedure repeatedly.
Algorithm 1 UPEC_Induction_Base

1: procedure UPEC_INDUCTION_BASE
2: \( k \leftarrow 1 \)
3: \( A_k \leftarrow \emptyset \)
4: \( bc \leftarrow true \)
5: \( a_k \leftarrow IPC\_Solver(UPEC\_Base(\emptyset, 1, bc)) \)
6: while \( a_k \neq \emptyset \) do
7: if \( a_k \) is L-alert then return \( a_k \)
8: \( P = Ploc(a_k) \)
9: \( A_k \leftarrow A_k \cup \{P\} \)
10: \( bc \leftarrow bc \land \neg \Lambda_P \)
11: \( a_k \leftarrow IPC\_Solver(UPEC\_Base(\emptyset, 1, bc)) \)
12: while \( A_k \neq \emptyset \) do
13: \( k \leftarrow k + 1 \)
14: \( A_k \leftarrow \emptyset \)
15: for \( P' \) in \( A_{k-1} \) do
16: \( a_k \leftarrow IPC\_Solver(UPEC\_Base(P', k, bc)) \)
17: while \( a_k \neq \emptyset \) do
18: if \( a_k \) is L-alert then return \( a_k \)
19: \( P = Ploc(a_k) \)
20: if \( P \notin \bigcup_{i=1}^{k} A_i \) then
21: \( A_k \leftarrow A_k \cup \{P\} \)
22: \( bc \leftarrow bc \land \neg \Lambda_P \)
23: \( a_k \leftarrow IPC\_Solver(UPEC\_Base(P', k, bc)) \)
24: return \( \bigcup_{i=1}^{k} A_i \)

The UPEC verification methodology is based on proof by induction, which consists of an induction base and an induction step. Alg. 1 shows the base proof. It iteratively verifies the design against the property of Fig. 5, collecting all possible P-locations, and searches for any L-alert. The “IPC Solver” is an interval property checker which returns a counterexample if the given property fails or, otherwise, returns \( \emptyset \).

The first step (lines 2 to 11) is to compute the initial set of P-locations, \( A_1 \), which can be reached in one clock cycle. “UPEC Base(\( \emptyset, 1, bc \))” is a special case of the UPEC property where \( k = 1 \) and there is no predecessor P-alert. Therefore, Alert_candidate needs to be determined based on the initial location of the secret (e.g., data memory/data cache). The design is repeatedly verified using the property. Every time, after finding a counterexample, the blocking clause is updated to search for new P-alerts. The loop is terminated as soon as the solver returns \( \emptyset \), which means there is no new P-location that is reachable within one clock cycle.

Once \( A_1 \) is computed, the procedure continues to find more alerts with longer time windows, until it reaches a time window in which it determines no new P-alert or L-alert (lines 12 to 24). The for loop (line 16) iterates through all P-locations determined in the previous iteration for \( k - 1 \), and, for each one of them, computes all successor alerts of length \( k \). In line 21, for the newly found alert \( a_k \), we check whether the same P-location has been detected by a shorter P-alert. This avoids generating the same P-location twice and makes sure that circular propagation of the secret between a set of state variables will not cause the algorithm to become stuck in an infinite loop.

Every time “IPC Solver” returns a counterexample, it is also checked if it is an L-alert. If this happens, a true security violation has been detected. The L-alert is returned immediately to the designer for debugging and repair. If no L-alert is detected, the algorithm returns all the P-locations found in the iterations.

Once the design successfully passes the UPEC induction base proof, it is guaranteed that, starting from any possible initial state, there is no information leakage possible within \( k \) clock cycles. The any-state proof within UPEC_Induction_Base implicitly considers any possible pipeline context and system state that is required for initiating secret propagation. As a result, for any information leakage possible within a time window larger than \( k \) clock cycles, UPEC_Induction_Base is guaranteed to find at least one precursor P-alert. This ensures exhaustive coverage of yet undiscovered P-alerts and L-alerts by the following algorithm for the induction step.

The goal of the induction step is to prove that, if the secret propagates to some non-observable microarchitectural state variables, it will not leak to architectural state variables at any time in the future. In other words, we need to prove that a P-alert cannot be extended further to reach a new P-location or to an L-alert. Therefore, in contrast to the induction base, the induction step property does not assume equality of all microarchitectural state variables at time \( t \) but instead assumes that the secret has already propagated to some of these variables, represented by a P-location \( P' \).

Algorithm 2 UPEC_Induction_Step

1: procedure UPEC_Induction_Step
2: for \( P' \) in \( A \) do
3: \( bc \leftarrow true \)
4: \( a_2 \leftarrow IPC\_Solver(UPEC\_Step(P', bc)) \)
5: while \( a_2 \neq \emptyset \) do
6: if \( a_2 \) is L-alert then return \( a_2 \)
7: \( P = Ploc(a_2) \)
8: if \( P \notin A \) then
9: \( A \leftarrow A \cup \{P\} \)
10: \( bc \leftarrow bc \land \Lambda_P \)
11: \( a_2 \leftarrow IPC\_Solver(UPEC\_Step(P', bc)) \)
12: return \( \emptyset \)

Fig. 6 shows the property which is the heart of...
**UPEC_Induction_Step** (Alg. 2). In this property, the starting state (at time point $t$) is the ending state of some P-alert found within the base proof. The property proves that any P-alert (of any length) that reaches $P$ and that does not reach a new P-location in the subsequent clock cycle, will also (inductively) not reach a new P-location thereafter. Note that a counterexample to the step property is always of length 2.

The procedure over-approximates the history prior to the ending state of a considered P-alert and, thus, includes all reachable behaviors of the design, including possible L-alerts. The over-approximation may lead to unreachable counterexamples. This is a standard problem and can be addressed by extending the proof to a $k$-step induction [41], or by strengthening the initial state of the proof by invariants. In our experiments, only for one of the designs (RocketChip), due to several uninitialized state variables, a few simple invariants had to be added manually.

Alg. 2 describes the procedure for the UPEC induction step. It receives the set of P-locations determined by the induction base computation of Alg. 1. For each P-location in this set, it computes all subsequent P-alerts using the “UPEC_Step” property. If the property holds, it is guaranteed that there is no subsequent P-alert. If the property fails, it checks whether the counterexample is an L-alert. If it is not an L-alert and also yields a new P-location, the new P-location is added to the set (lines 8 and 9) and used in another “UPEC_Step” proof.

The latter situation reflects that the induction base computation of Alg. 1 terminates as soon as incrementing $k$ does not yield any new P-location. The bounded model of **UPEC_Induction_Base** misses a P-location in case it is reached only at a later time point, after having been propagated through already known P-locations. However, such a P-location is detected afterwards, in **UPEC_Induction_Step**, by iteratively computing all successor P-locations of already known ones. Alg. 2, therefore, always completes the set of P-locations. If Alg. 2 terminates without an L-alert, it means there cannot be any information leakage and the procedure returns $\emptyset$, certifying the security of the design.

In most practical cases, already Alg. 1 determines all P-locations that exist. This implies that **UPEC_Induction_Step** mostly serves as a check for proof completeness and usually does not incur additional debugging effort. The possible P-locations typically comprise only a small fraction of the microarchitectural state variables, entailing only a small number of iterations in Alg. 1 and Alg. 2. Although the above procedures are fully automated, there can be a benefit in manually inspecting the counterexamples for every generated P-alert that points to a new P-location. This helps the user to understand the security implications of microarchitectural optimizations, detect undesired information flows and, even more importantly, capture security violations early if the security compromise is already obvious from the given P-alert.

**D. Blackboxing in the UPEC Flow**

The computational model of UPEC provides a good opportunity for automatic blackboxing, without the risks associated with under- or over-approximating the design behavior. In UPEC a component can be blackboxed soundly using only a simple constraint. It states that the component outputs are equal between SoC instance 1 and 2 in every clock cycle of the proof as long as the component’s inputs are equal between SoC instance 1 and 2 in every clock cycle of the proof. If a P-alert occurs during the verification procedure of Sec [VI.C] which violates this condition, i.e., if the secret propagates to the inputs of the blackboxed component, then this component must be unblackboxed. Otherwise, it is proven that the blackbox is sound and no leakage can be missed.

This blackboxing technique can, for example, be applied effectively to system components containing large memory arrays, like the tag array in a cache. It should be noted that in the design examples we have considered so far, such components have a state-dependent timing behavior. Consequently, secret propagation to their internal state can alter the timing of instruction execution. Therefore, a P-alert which shows a propagation of the secret to the inputs of such a component can be seen as an early security alarm.

**VII. UPEC for Advanced Processors**

**A. UPEC for OOO processors**

For processors of medium complexity with in-order pipelining, the miter construction of Fig. 4, as discussed in Sec. V-A, entails that only little effort is required for manually creating invariants to eliminate unreachable counterexamples [42]. However, this changes when out-of-order processors are considered. The symbolic initial state can then include starting states, for example, with inconsistent instruction tags or IDs in different bookkeeping structures, so that invalid execution orders are considered.

The key idea to tackle this problem is to constrain the UPEC proof by microequivalence (Eq. 4). This means that, instead of verifying the trace property of Eq. 1, we propose to target Eq. 3 when dealing with OOO-processors. This simplifies the proof procedure significantly. Note that excluding functional correctness violations from consideration is legitimate since functional verification, i.e., checking compliance of the microarchitectural implementation with the functional ISA specification, is a separate and mandatory step in standard design flows, regardless of the security requirements.

In the following, we provide an exemplary description of how to specify microequivalence. A general template for microequivalence and a concrete example of its refinement for the BOOM processor is made available at [13].

The symbolic initial state models the reservation stations of the pipeline with arbitrary instructions having arbitrary operands, IDs and other bookkeeping information. The information about how this is linked by the renaming mechanism to the original instructions, as they were processed by the previous decode stage, is lost. For example, in our computational model, an older, non-speculative ADD instruction may receive an operand from the destination register of a younger speculative LOAD instruction. Obviously, this can lead to false alarms.

Invariants for microequivalence can be created that remove such spurious behavior by relating the entries of the reservation
stations to the relevant operand and bookkeeping information of the reorder buffer (ROB) such that only feasible orders and operand dependencies are taken into consideration. These invariants must be formulated, however, for each pair of pending instructions in the pipeline. This, unfortunately, can be quite laborious.

A better understanding of transient instruction execution in OOO processors helps us to to reduce this manual effort drastically. Fig. 7 shows a general model of how instructions execute in a transient execution attack. The main sequence of instructions reaches a branch instruction, initiating the transient sequence that is executed speculatively and discarded eventually. Since the program must have a secret-independent architectural observation, there must be no instruction in the main sequence that depends on the secret. However, instructions in the transient sequence (in a Spectre-style attack these typically belong to a privileged process called by the attacker) can access the secret but cannot commit.

In the following, we assume that the transient instructions are discarded due to a misprediction event. For the case that the transient instructions are discarded due to an exception (Meltdown-style attacks) or for the case that other kinds of speculations (e.g., load to store dependency prediction) are the cause of misprediction, the approach is analogous.

For an information leakage to happen, the transient sequence must affect the behavior of the main sequence, i.e., it must affect the microarchitectural execution of the program. For example, in a Spectre-STC attack, the instructions in the transient sequence affect the timing when instructions commit in the first block of the main sequence. As another example, for the original Spectre attack, the instructions in the transient sequence create a secret-dependent cache footprint which induces timing variations in the second block of the main sequence.

We observe that a spurious behavior, such as the one described above, can only lead to a false counterexample to the UPEC proof if it creates a false interrelation between instructions of the transient and the main sequence (e.g., a secret value being forwarded from the transient sequence to the main sequence). Due to the UPEC miter structure and the fact that the only difference between the two instances is the value of the secret, any spurious behavior within each block is irrelevant for the proof and cannot produce a false L-alert. The reason is that within the main sequence, no execution order can create a secret-dependent result and within the transient sequence, none of the results can be committed.

This means that the bookkeeping mechanisms must be constrained to ensure the program order and corresponding operand dependencies only between the three code blocks in Fig. 7 but not necessarily within each block. This can be achieved by enforcing that the instructions in the main sequence do not use the result of transient instructions as an operand. Note that this is a valid constraint because the main sequence block before the branch never reads an operand from instructions after the branch instruction, and the main sequence block after the branch never reads a result from a transient (and as such always discarded) instruction.

This observation is key and allows us to approximate microequivalence effectively by using the branch instruction to split the ROB into the slots of the main sequence and the slots of the transient sequence.

Using this partitioning, false operand dependencies between the blocks can be avoided without formulating complex invariants for source and destination registers of each in-flight instruction. For example, to avoid the false operand dependence for the ADD instruction of the above example, the proof must be constrained such that if an ADD instruction from the main sequence (based on its ROB slot) is being executed by the ALU in both SoC instances, its operands must be independent of the secret. This element of the microequivalence specification is expressed in Eq. 5 using a pseudo-code notation. The approach is similar for other functional units.

\[(\text{ALU}_1.\text{instr}_\text{ID} = \text{ALU}_2.\text{instr}_\text{ID}) \land \text{ALU}_1.\text{instr}_\text{ID} \text{ is assigned to main sequence ROB slot} \rightarrow (\text{ALU}_1.\text{instr}_\text{operands} = \text{ALU}_2.\text{instr}_\text{operands})\]

A more detailed description on how to specify microequivalence for any processor with a reorder buffer, as well as how to deal with more advanced features such as nested speculation and load-store dependency speculation, is available in [43], [13].

B. UPEC for Processors with Dynamic Register Mapping

ISAs usually define a set of logical registers (or general-purpose registers) which are used as source and destination of different instructions. In in-order pipelines, these logical registers are statically mapped to a set of physical registers. They are the architectural (program-visible) registers of the design. However, in order to gain performance improvement by register renaming, some OOO microarchitectures (e.g., BOOM [12]) feature dynamic register mapping. The microarchitecture implements a physical register file, which usually has more registers than specified in the ISA, as well as a map table, which holds, at each time point of program execution, the mapping between logical ISA registers and physical registers. This allows for storing both speculative and committed values in the same register file. Such an architecture creates an additional challenge for the UPEC approach since the proof methodology relies on making the distinction between L-alerts and P-alerts. This means that UPEC must know the architectural state of the system which relies on the state of the ROB and the map tables.

Fortunately, there is an efficient solution to this problem. In our proof methodology for OOO processors, microequivalence constrains the search to only transient execution attacks, i.e., UPEC analyzes windows of the execution where the
microarchitectural observation is independent of the secret. This means that the same sequence of values is committed to the architectural registers in both SoC instances and only the timing (but not the values) of instruction commit can be secret-dependent. This allows us to modify the definition of an L-alert to be used in Alg. \[1\] (lines 7, 19) and Alg. \[2\] (line 6). Instead of comparing values of architectural registers, as in Def. \[5\] we check, as given by Eq. \[6\], whether or not the instructions in the two SoC instances reach the head of the ROBs simultaneously.

\[ \text{soc1.core.rob.head} = \text{soc2.core.rob.head} \quad (6) \]

VIII. Experiments

The proposed UPEC approach has been evaluated by verifying three different SoC designs: RocketChip (v1.2.0) \[10\], the Berkeley Out-Of-Order Machine (BOOM v2.0.1) \[12\] and Ariane (v4.1.2) \[11\]. All results were obtained using the commercial property checker OneSpin 360 DV running on an Intel Core i7 at 3.4 GHz, with 32 GB of RAM.

A. UPEC for In-order Pipelines

We evaluated the effectiveness of UPEC for capturing vulnerabilities in in-order pipelines by targeting different design variants of RocketChip and the Ariane design. The considered RocketChip design variants included the original design as well as two modified design variants vulnerable to two different versions of the Orc attack. In the first modified variant, we conditionally bypassed one buffer in the cache-to-core interface pipeline to make the design vulnerable to the attack described in Sec. \[III-A\]. For the second vulnerable design, RocketChip was modified such that a cache line refill is not canceled in case of an invalid access. While the illegal access itself is not successful but raises an exception, the cache content is modified and can be analyzed by an attacker.

It should be noted that these design modifications are minor (compared to the overall design size) and they represent a realistic design optimization. The modified designs successfully pass all tests in the suite provided by the RISC-V framework.

In the following experiments, the secret data is assumed to be in a protected location, \(A\), in the main memory, possibly with a copy in the data/instruction cache. In our RocketChip experiments, memory protection was implemented using the Physical Memory Protection (PMP) scheme of the RISC-V ISA by configuring the memory region holding the location \(A\) of the secret data as inaccessible in user mode. In our Ariane experiment, secret protection is achieved through virtual address translation, i.e., the memory page holding the location \(A\) is marked as unreadable and unexecuteable by the page table. In our experiments, we assumed correctness of the page table walking mechanism, i.e., the content of the Translation Lookaside Buffer (TLB) is always correct w.r.t. the page table.

For RocketChip and Ariane the proof methodology is based on the properties of Figures \[5\] and \[6\] and does not employ microequivalence. Consequently, these experiments target information leakage through both functional bugs and transient execution attacks. UPEC successfully captured all vulnerabilities to Orc Attacks in the RocketChip design variants. In addition, UPEC found a design bug introducing an ISA incompliance in the locking mechanism of the Physical Memory Protection (PMP) unit of the original RocketChip design. The bug allowed modification of PMP configurations even when the lock bit is set. This can compromise security \[31\] and is therefore forbidden by the RISC-V ISA. The vulnerability is removed in the current version of the design.

UPEC proved the Ariane design to be free of vulnerabilities to transient execution attacks. However, UPEC found an invalid information flow which has relevant security implications. (This was reported to the Ariane development team.) The instruction cache, in a certain scenario, allows a user-level process to refill a cache line with an inaccessible address. This may further expand the ability of the attacker to launch classical side channel attacks, even in cases where there is no page sharing between attacker and victim. We patched the design and re-verified with UPEC.

In an additional experiment for Ariane we verified the confidentiality of the page table. Protecting physical addresses that are stored in the page table is important to limit the impact of attack scenarios such as RowHammer \[44\]. We verified the absence of any vulnerability that reveals the physical address to a user-level process using a modified experimental setup in which the confidential information of the miter model is an arbitrary physical page number stored in the TLB.

Tab. \[I\] shows the proof complexity of the experiments. The designs are verified using the iterative UPEC methodology, described in Sec. \[VI-C\]. In case of the detected vulnerabilities, the CPU time, memory consumption and property time window \((k)\) of the proof that returned the corresponding L-alert is reported. All vulnerabilities were found within the UPEC_InitInduction_Base algorithm, before proceeding to UPEC_InitInduction_Step. In case of the designs verified to be secure, the reported CPU time, memory consumption and property time window \((k)\) corresponds to the most complex proof in terms of run time within the UPEC_InitInduction_Base and UPEC_InitInduction_Step algorithms. It should be noted that in all these experiments, the most complex proof was always within the last iteration of UPEC_InitInduction_Base. For the secure designs, the last column in Tab. \[I\] shows the number of P-locations that have to be proven secure in UPEC_InitInduction_Step.

In these experiments, it took approximately 10 person-days of manual work to verify each design, which was predominantly spent in analyzing the provided counterexamples and debugging the design. Considering the complexity of the designs, the incurred manual effort is small compared...
to the efforts required for the functional verification of these processors.

Tab. II evaluates the effect of different factors on the proof complexity, based on the UPEC experiment on RocketChip. Both 32-bit and 64-bit versions of the design are verified and the highest proof runtime is reported, which shows the robustness of our approach w.r.t. datapath complexity. The table also shows the significant improvements that can be achieved by simplifying the prove part of the property based on cone-of-influence reduction (cf. Sec VII-B).

B. UPEC for OOO Pipelines

The BOOM processor is of particular interest in our experiments since it is known to be vulnerable to Spectre-style attacks while deemed secure with respect to Meltdown. It is a full-grown SoC with an OOO-core which features a branch prediction unit with support for nested branches, virtual memory translation with a TLB, a non-blocking data cache with miss status handling registers (MSHR), a page table walker, a physical register file with dynamic register mapping and other features typically employed with OOO-cores. BOOM’s performance is comparable to ARM cores between Cortex A9 and A15, depending on its configuration. The verified Boom design (single core and peripherals) consists of more than 650 k state bits. The only difference with the previous experiments is that the UPEC proofs were constrained using the concept of microequivalence (Sec. VII).

As a demonstration that we can focus separately on different classes of attacks, in our experiments, we decomposed the proofs into checks for Meltdown versus Spectre, i.e., as defined in Sec. IV. We assume that the instruction accessing the secret either has the proper privilege to do so (Spectre class) or not (Meltdown class). Furthermore, the secret is assumed to reside in the main memory, with the possibility of a copy in the data cache.

Tab. III has three sections, describing our experiments with the checks for the Spectre and Meltdown classes, as well as for page table confidentiality. Similar to Tab. II it shows the computational effort for the most complex proofs within UPEC_Induction_Base and UPEC_Induction_STEP for our patch-and-verify flow, as described below. It should be noted that the vulnerabilities were detected by L-alerts in UPEC_Induction_Base. For the secure designs, the last column in the table shows the number of P-locations that had to be proven secure in UPEC_Induction_STEP.

Tab. IV shows the amount of manual work required to develop and prove the UPEC property for BOOM.

For the class of Spectre attacks, our approach generated counterexamples to the UPEC property in terms of L-alerts (cf. Sec. VI) demonstrating that the considered BOOM design is vulnerable to Spectre-STC, a so far unknown variant of Spectre, described in Sec. III-B. We employed an iterative design procedure where we iteratively patch the vulnerability detected in a selected UPEC counterexample, and then re-verify the design using UPEC. After fixing the Spectre-STC vulnerability through a minor fix in the first iteration, UPEC identified (by L-alert) a second version of the Spectre-STC vulnerability. This version is similar to the first one except that port contention now happens on the TLB rather than on the write port to the register file. The patch-and-verify flow can be repeated until all the vulnerabilities have been removed.

In the third iteration of our flow, we picked a UPEC counterexample pointing to the original Spectre attack, which uses the cache as side channel [1]. We applied a simple and rather conservative patch for this vulnerability. Our fix for Spectre prevents speculative load instructions to execute before all preceding branch instructions are resolved. The patched design coming out of this third iteration (“secure design variant” in Tab. III) was then formally verified to be secure with respect to transient execution attacks. Although the fix incurs performance penalties, it still allows for speculative execution of the majority of instructions.

In a separate experiment, we also examined the original design for the class of Meltdown attacks, as defined in Sec. IV. The computational effort for this experiment, which proves security of the original BOOM v2.0.1 w.r.t. Meltdown, is also listed in Tab. III.

To the best of our knowledge, presently no other method is capable of solving the above RTL verification tasks. As a result of our experiments, the patched BOOM design is the first formally proven RTL model of a secure speculative execution processor.

IX. Conclusion

The paper has shown that transient execution side channels can occur also in simple processors. They do not only result from certain architectural features, such as out-of-order execution and speculative execution, but can also be inserted by low-level RTL design modifications. Such vulnerabilities may
be introduced inadvertently by seemingly innocuous design decisions and, even worse, they may also be deliberately created by a malicious SW/HW provider to create an invisible “backdoor”. Such a new kind of Trojan can be extremely hard to find, since it does not conform to the conventional Trojan models (trigger and payload), and, more importantly, it neither corrupts the functionality of the design nor does it add any redundant logic. With the increasing role of shared HW and SW infrastructures involving components from numerous providers as well as open-source domains, such a risk must be given appropriate attention.

We have demonstrated that UPEC is capable of detecting TESs in an exhaustive, scalable and highly automated way. This is a significant improvement over the state of the art, especially since also vulnerabilities can be detected which are based on so far unknown exfiltration channels.

The required manual work in UPEC is small compared to the total SoC design and verification effort at the RTL. The bulk of this effort is spent on analyzing the provided counterexamples and security violations.

The proposed approach, due to its exhaustiveness, has promise for an efficient solution regarding legacy HW. By analyzing the RTL design of legacy systems the UPEC user can collect all possible attack scenarios feasible in the design. The collected information can be passed on to the SW domain to enforce SW fixes only for the necessary cases and relevant gadgets. Future work will explore how UPEC can support methodologies employing contracts between HW and SW such that a sound compositionality can be achieved between measures at the SW level and the RTL.

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