Sampling and Comparator Speed-Enhancement Techniques for Near-Threshold SAR ADCs

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ABSTRACT This paper presents the sampling and comparator speed-enhancement techniques for SAR ADCs under near-threshold supply voltages. The proposed level-shifted boosting circuit generates sharp falling edges for the sampling clock, which is found a key factor limiting the sample speed under ultra-low voltages. Delayed cross-coupling comparator is introduced in this work, which enhances the comparator regeneration while keeping the noise comparable. A 0.35V 8b 12MS/s SAR ADC is designed in a 65nm CMOS technology to prove the proposed techniques. The post-layout simulated SAR ADC consumes only 6.71 $\mu$W and achieves SNDR of 48.8dB at Nyquist input, resulting in a figure-of-merit (FoM) of 2.47 fJ/convertion-step. Simulation results show the proposed speed-enhancement techniques improve the sampling rate of SAR ADC significantly under near-threshold supply voltages.

INDEX TERMS Sampling rate, SAR ADCs, comparators, ultra-low voltage, near-threshold.

I. INTRODUCTION

WITH the scaling down of feature sizes in advanced CMOS technologies, the standard supply voltages are getting lower. In order to achieve high speed under low voltages, pipeline [1] and flash [2] analog-to-digital converters (ADC) are designed to achieve tens of MHz sampling rate under 0.5V. But their figure-of-merits (FoMs) are not competitive as compared to successive approximation register (SAR) based ADCs due to the simple architecture with no need for power hungry modules. Working at low power supply voltage, SAR ADCs have a wide range of applications in wireless sensor network, biomedical (EEG, ECG, EMG), environmental monitoring (temperature, humidity, pressure) and other fields. However, the working principle of SAR ADCs normally limits the sampling rate at hundreds of kS/s with supply voltages lower than 0.5V.

Conventional SAR ADC is composed of two boosted sampling switches, a differential binary-weighted capacitive DAC, a comparator and control logics. For an asynchronous SAR ADC, the total time for each conversion cycle is

$$T_{\text{tot}} = T_{\text{samp}} + \sum_{i=1}^{N} (T_{\text{DAC}[i]} + T_{\text{comp}[i]} + T_{\text{logic}[i]}),$$

where $T_{\text{samp}}$ is the sampling time of the ADC. DAC settling time ($T_{\text{DAC}[i]}$), comparison time ($T_{\text{comp}[i]}$) and propagation delay time for digital control logics ($T_{\text{logic}[i]}$) consume the time budget of each successive approximate (SA) cycle. $N$ SA cycles are needed for an $N$-bit SAR ADC with 1b-per-cycle architecture.

Constant-$V_{\text{GS}}$ bootstrapping technique is commonly used for sampling switches, which keeps the on-resistance the same over the rail-to-rail input voltage range. The overdrive voltage of the sampling switch with constant-$V_{\text{GS}}$ bootstrapping technique is $V_{\text{DD}}-V_{\text{TH}}$. However, under near-threshold supplies, the overdrive voltages become too low for MHz sampling. A cascade of clock boosting circuits [3] is employed to achieve higher switch-on voltage, but the
falling edge of the boosted signal becomes slower, resulting in a slow turn-off of the sampling switch.

Comparator is the key analog block in a SAR ADC. The working speed of the comparator affects the comparison time \( T_{\text{comp}}(i) \) in each SA cycle, and the noise performance of the comparator affects the resolution of the ADC directly. Speeding up a comparator with large input transistors leads to large kick-back noise to the capacitor array, which is more severe for small arrays under ultra-low voltages. Another approach is to enhance the positive feedback of the cross-coupling transistors. However, because the amplification time is shortened, the comparator noise is enlarged [4].

Two speed-enhancement techniques for near-threshold SAR ADCs are introduced in this work. The level-shifted boosting circuit is proposed to achieve sharp-edged sampling clock for megahertz rail-to-rail sampling. Delayed cross-coupling comparator is exploited to improve the comparison speed and, at the same time, keep the comparator noise low. In order to demonstrate the proposed techniques, a 0.35V 8b 12MS/s SAR ADC is designed, achieving 7.82b ENOB and 2.47 fJ/conv.-step FoM.

The rest of this paper is organized as follows. Section II introduces the level-shifted boosting circuit. Delayed cross-coupling comparator is presented in Section III. Section IV shows the architecture of the SAR ADC with the proposed speed-enhancement techniques. Post-layout simulation and comparison with recent design are carried out in this section. Section V concludes this paper.

II. LEVEL-SHIFTED BOOSTING CIRCUIT

The performance of sampling circuits limits both the speed and linearity of the whole ADC. High switch-on voltage is generally preferred for linear sampling of a rail-to-rail input. Clock boosting technique is often employed to boost the switch-on voltage. Constant-\( V_{GS} \) bootstrapping technique is widely used for sampling switches, since the overdrive voltage of the sampling switch remains the same with different input voltages, which doesn’t introduce extra nonlinearity to the system. Since the overdrive voltage of the sampling switch with constant-\( V_{GS} \) bootstrapping technique is \( V_{DD} - V_{TH} \), the overdrive voltage is close to zero under a near-threshold supply voltage, which increases the switch-on resistance by several orders of magnitude. Hence, the sampling speed with constant-\( V_{GS} \) bootstrapping is limited under ultra-low voltages. A cascade of clock boosters [3] was introduced to boost the switch-on voltage several times, which ensures a sampling with 8-bit linearity.

Nevertheless, we found switch-off speed, or the falling time of the sampling clock, is the main limitation for sampling rate under low supply voltages. The relationship between the falling time of the sampling clock and SFDR & SNDR is analyzed in Fig. 1, where the sampling rate and switch-on voltage of the sampling clock are fixed at 12MS/s and 1V, respectively, and a 0.35V, 5.86MHz sine wave is used as the input signal. The simulation result in Fig. 1 indicates that SFDR and SNDR degrade when the falling time of sampling clock increases. And a falling time less than 4ns is needed to achieve over 60-dB SFDR.

Fig. 2(a) presents the schematic of a single stage of conventional clock boosting circuit [5]. When \( \text{clk\_in} \) gets high, \( V_y \) is set to \( \text{clk\_in} + \text{VDD} \) and \( \text{clk\_out} \) is connected to \( V_y \) through \( M_1 \). When \( \text{clk\_in} \) is low, \( V_x \) is set high to switch on \( M_2 \), which pulls \( \text{clk\_out} \) to low. Since \( V_x \) is limited by \( \text{VDD} \), the voltage of \( \text{clk\_out} \) in Fig. 2(a) falls slowly under near-threshold supply. Fig. 2(b) shows the schematic of the proposed level-shifted boosting circuit. A level shifter is utilized to replace the inverter in the dotted box in Fig. 2(a). Signal \( \text{clk\_in} \) in Fig. 2(b) is used to pre-charge \( V_z \) to \( \text{clk\_in} + \text{VDD} \). When \( \text{clk\_samp} \) is high, \( V_p \) goes low and \( \text{clk\_out} \) is connected to \( V_z \) through \( M_7 \). When \( \text{clk\_samp} \) is
low, \( V_p \) and \( V_z \) are connected together through M5 and M3. Hence, \( V_p = V_z - V_{TH} = \text{clk}_\text{in} + VDD - V_{TH} \). If \( \text{clk}_\text{in} \) is a high voltage signal, \( V_p \) is higher than VDD. So M8 pulls \( \text{clk}_\text{out} \) to zero much faster than M2. The connection of the PMOS substrate in the Fig. 2(a) and Fig. 2(b) is indicated with dotted lines. The purpose of this connection is to prevent the substrate leakage.

Since the maximum output voltage of a single stage of Fig. 2(a) and Fig. 2(b) is \( \text{clk}_\text{in} + VDD \), the switch-on resistance of the sampling switch is limited under near-threshold supply. Therefore, cascade of boosting circuits is needed. Fig. 2(c) shows the block diagram of a popular solution with three cascaded conventional clock boosting stages. When \( \text{clk}_\text{samp} \) gets high, the output of the conventional clock boosting circuit goes high stage by stage. After three-boost-stage delay, signal \( \text{samp}_1 \) rises to a boosted voltage. Similarly, when \( \text{clk}_\text{samp} \) gets low, the output of the conventional clock boosting circuit goes low stage by stage.

Fig. 2(d) proposes the proposed circuit with two conventional clock boosting stages cascaded with a level-shifted boosting stage. Fig. 3 shows the timing diagram together with simulation results. Signal \( \text{pre}_\text{samp} \) is employed to pre-charge the capacitors to high voltage in the boosting circuits. When \( \text{pre}_\text{samp} \) gets high, the output of the two conventional clock boosting stages goes high stage by stage. Then \( \text{clk}_\text{samp} \) is set high to pull the output, \( \text{samp}_2 \), to the boosted voltage only after two-stage gate transmission delay. When \( \text{clk}_\text{samp} \) goes low, \( V_p \) is pushed to a voltage higher than supply. Large overdrive voltage of M8 pulls the output voltage to zero in a very short time. Then signal \( \text{pre}_\text{samp} \) goes low after \( \text{samp}_2 \) gets to zero.

From Fig. 3, the switch-on voltages of \( \text{samp}_1 \) and \( \text{samp}_2 \) are over 1 V, which ensures a small switch-on resistance. The falling time of \( \text{samp}_1 \) is more than 10 ns. The falling time of \( \text{samp}_2 \) from 0.9 maximum voltage to 0.1 maximum voltage is 1.8 ns, which is sufficient for a 0.35V 8b 12MS/s ADC according to Fig. 1. Fig. 4 shows the simulated spectrum of a 0.35V sampling circuit with the proposed clock boosting technique shown in Fig. 2(d). The performance with the conventional clock boosting circuit of Fig. 2(c) is also given as reference. The simulated sampling circuit is the same with the one in Fig. 1. With a 5.86MHz Nyquist input sampled at 12MS/s, 58.71dB SNDR and 64.24dB SFDR are achieved with the proposed clock boosting technique. As shown in Fig. 4, 10.76dB improvement on SFDR is obtained.

### III. DELAYED CROSS-COUPLING COMPARATOR

Speed and noise are the key considerations for ultra-low voltage comparators. The comparison consumes the time of each SA cycle, and the input referred noise of the comparator affects the resolution of the ADC directly. In addition, there are tradeoffs between the speed and noise of the comparators.

Fig. 5(a) shows the schematic of a typical P-latch comparator. M1, M6 and M7 are used as switches to enable and reset the comparator. M2 and M3 are input differential transistors. M4 and M5 are cross-coupled for positive feedback. The process of comparison can be viewed as four phases [4], [6], i.e., reset, amplification, regeneration and decision, as shown in Fig. 6. When \( \text{clk} \) is low, M1 is turned off, M6 and M7 are turned on. The comparator is in reset phase, \( \text{Vop} \) and \( \text{Von} \) are reset to high. Sampling phase starts after the rising edge of \( \text{clk} \), where the voltage difference of \( \text{Vop} \) and \( \text{Von} \) is sampled and amplified to trigger the following regeneration phase. The speed of the comparison can be improved with larger pull-down current by increasing the size of the M1, and increasing the size of M2 & M3 in the same proportion to achieve greater transconductance. However, increasing the size of the input transistors results in higher kick-back noise to the capacitor array, which degrades the linearity.

As a direct approach, an additional cross-coupled pair, M8 and M9, can be introduced to enhance the positive feedback, as shown in Fig. 5(b). Right after reset, the NMOS cross coupled pair is in on-state and starts regeneration, which greatly reduced the duration of amplification phase. To show the influence of the changing part, the transistors marked with the same name in Fig. 5 are also sized the same for the simulation in Fig. 7. The result shows NP-latch comparator is much faster than the P-latch one. However, the extra cross-coupling circuit decreases the sampling time as well. Since the input signal is sampled and amplified in amplification phase, the input referred noise of the comparator is inversely proportional to the time of amplification phase [4]. Hence, the noise performance of NP-latch comparator is degraded. The simulation result proves the root-mean-square (RMS)
FIGURE 5. Schematics of (a) a P-latch comparator, (b) a NP-latch comparator, (c) the proposed delayed cross-coupling comparator.

FIGURE 6. Four phases of conventional comparator.

FIGURE 7. Simulated timing diagram and noise performance of the three kinds of comparators under the situation of “same name sized the same”. The noise of NP-latch comparator is 1490 \( \mu V \), whereas the noise of P-latch comparator is 350 \( \mu V \).

The delayed cross-coupling comparator is proposed to decrease the comparison time without degrading the noise performance, as depicted in Fig. 5(c). Since M8 & M9 in Fig. 5(b) decrease the time for amplification phase and increase the comparator noise, the additional cross-coupling pair is delayed to work until the amplification phase ends. The timing of the comparator is given together with the simulation results in Fig. 7. The comparator is enabled when \( clk \) gets high, while \( clk2 \) is kept low during the amplification phase, disconnecting the extra cross-coupling pair from the comparator. Therefore, the equivalent circuit of Fig. 5(c) in amplification phase is the same with Fig. 5(a). \( clk2 \) gets high after amplification phase, then M8 & M9 are added into the circuit to enhance the regeneration. So the delayed cross-coupling comparator improves the speed of comparator without degrading the noise performance. In order not to degrade the noise performance, the rising edge of \( clk2 \) should be later than the amplification phase. While if \( clk2 \) is too late, the comparison speed would be affected. Hence, \( clk2 \) is generated by a voltage-controlled delay circuit from \( clk \). The control signal can be adjusted manually in the simulation. When this value is set larger, the delay time is shorter, and the comparator is faster but noise performance gets worse. When this value is set small, the rising edge of \( clk2 \) arrives later, and the comparator’s noise is reduced but the speed is limited. After a lot of simulations and comparisons, when the control voltage is set to 185mV, the optimal delay time on \( clk2 \) is 1.86ns, and the speed and noise performance of delayed cross-coupling comparator are optimized. From Fig. 7, the RMS noise of the proposed comparator is 400 \( \mu V \), which is similar to the noise performance of the traditional P-latch comparator. It shows the proposed comparator can enhance the working speed while remaining the noise performance.

In order to show the improvement of the proposed delayed cross-coupling comparator, the sizes of M8 & M9 in the NP-latch comparator are tuned to achieve the same delay of the proposed comparator. The simulated noise and power are listed in Table 1. The average current is achieved under 125 MHz speed. Simulation results show the proposed comparator achieves similar power with NP-latch comparator, but the noise of the proposed one is much lower.

### TABLE 1. Simulated noise and power with same delay.

| Comparator Type                  | RMS Noise | Average Current |
|----------------------------------|-----------|-----------------|
| NP-latch comparator              | 767 \( \mu V \) | 2.35 \( \mu A \) |
| Delayed cross-coupling comparator| 400 \( \mu V \) | 2.41 \( \mu A \) |

IV. ADC ARCHITECTURE AND SIMULATION

Sections II and III introduce two speed-enhancement techniques for near-threshold SAR ADCs. A 0.35V SAR ADC with these techniques has been designed with post-layout simulations. Fig. 8 presents the system architecture of the
TABLE 2. Performance summary and comparison.

|                  | This work* | ESSCIRC’12 [8] | ISSCC’13 [9] | TCAS-II’15 [10] | TCAS-II’16 [11] | JSSC’16 [12] | JSSC’17 [13] | JSSC’19 [14] |
|------------------|------------|----------------|--------------|----------------|----------------|---------------|---------------|---------------|
| Resolution (bit) | 8          | 8              | 10           | 11             | 10             | 10            | 9             | 10            |
| Tech. (nm)       | 65         | 40             | 90           | 130            | 90             | 90            | 28            | 40            |
| Area (mm²)       | 0.018      | 0.0153         | 0.0418       | 0.868          | 0.0125         | 0.0408        | 0.00312       | 0.00975       |
| Voltage (V)      | 0.35       | 0.35           | 0.4          | 0.5            | 0.4            | 0.5           | 0.3           | 0.5           |
| Sampl. rate (MS/s) | 12        | 0.512          | 1.3          | 6.144          | 0.5            | 1.25          | 0.5           | 0.5           |
| ENOB (bit)       | 7.82       | 6.79           | 7.08         | 7.07           | 8.72           | 8.94          | 9.6           | 10.03         |
| Power (µW)       | 6.71       | 0.4            | 1.06         | 6.43           | 0.5            | 1.8           | 26.1          | 39.9          |
| FoM (J/conv.-step) | 2.47     | 6.8            | 5.9          | 7.7            | 2.37           | 2.93          | 67.3          | 76.3          |

* Post-layout simulation results

Fig. 8: System architecture of the proposed SAR ADC.

Fig. 9: Layout of the proposed SAR ADC.

The proposed SAR ADC. It is composed of a split capacitor array [7], two sampling switches with the proposed level-shifted clock boosting circuits, the proposed delayed cross-coupling comparator and control logics. The split capacitor array is employed to avoid the common-mode reference voltage $V_{cm}$ (0.5*$V_{DD}$), because the low overdrive voltage for switching on $V_{cm}$ affects the DAC settling time under ultra-low supply voltages.

The 0.35V ADC has been post-layout simulated in a 65-nm CMOS technology. Fig. 9 shows the layout of the proposed ADC. The unit capacitance of the CDAC is 1 fF. Fig. 10 shows the 4096-points fast Fourier transform (FFT) spectrum result with a 5.86 MHz input sampled at 12 MS/s. The SNDR and SFDR are 48.8 dB (7.82 ENOB) and 67.39 dB, respectively. The simulated results of SFDR and
SNDR versus input frequency are also presented in Fig. 10. The whole ADC consumes only 6.71 $\mu$W with DAC of 0.7 $\mu$W, comparator of 0.78 $\mu$W, clock boosting of 0.71 $\mu$W, and logic of 4.52 $\mu$W. With the Walden FoM definition, 

$$FoM = \frac{\text{power}}{[2^{ENOB} \cdot fs]},$$

a FoM of 2.47 $\text{fJ/conv.-step}$ has been achieved. Table 2 summarizes the simulated performance and compares the proposed work with previously reported sub-0.5V SAR ADCs with 8-11 bits of resolution. Fig. 11 plots the speed-enhancement techniques have significantly increased the potential sampling rate of near-threshold SAR ADCs.

**V. CONCLUSION**

Sampling and comparator speed-enhancement techniques for SAR ADC under near-threshold supply voltages have been introduced in this work. Sharp-edged sampling signal with 1.8-ns falling time has been generated by the proposed level-shifted boosting circuit. The proposed delayed cross-coupling comparator improves the comparator speed without degrading the noise performance. The proposed speed-enhancement techniques have been post-layout simulated in a 0.35V 8b 12MS/s SAR ADC. The results has proved the proposed sampling technique and comparator design with significantly enhanced speed as compared to reported near-threshold ADCs.

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**VOLUME 2, 2021 309**
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