Analog VLSI Circuits for Short-Term Dynamic Synapses

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Short-term dynamical synapses increase the computational power of neuronal networks. These synapses act as additional filters to the inputs of a neuron before the subsequent integration of these signals at its cell body. In this work, we describe a model of depressing and facilitating synapses derived from a hardware circuit implementation. This model is equivalent to theoretical models of short-term synaptic dynamics in network simulations. These circuits have been added to a network of leaky integrate-and-fire neurons. A cortical model of direction-selectivity that uses short-term dynamic synapses has been implemented with this network.

Keywords and phrases: short-term synaptic dynamics, depression, facilitation, silicon synapse, cortical models.

1. INTRODUCTION

Cortical neurons show a wide variety of neuronal and synaptic responses to their input signals. Networks with simplified models of spiking neurons and synapses and consisting of one or two time constants already exhibit a large number of possible operating regimes [1, 2]. Simulations of these spiking networks can take a long time on a serial computer.

In most network simulations, synapses are assumed to be static. Recent physiological data, however, show that synapses frequently show activity-dependent plasticity which vary on a time scale of milliseconds to seconds. In particular, short-term dynamical synapses [3, 4, 5, 6, 7] with time constants of hundreds of milliseconds are seen in many parts of the visual cortex. When these synapses are stimulated with a train of input spikes, the amplitude of the membrane potential of the neuron or the excitatory postsynaptic potential (EPSP) decreases (depressing synapse) or increases (facilitating synapse) with each subsequent spike. The recovery time of the maximum synaptic amplitude is in the order of hundreds of milliseconds. These synapses encode the history of their inputs and can be treated as time-invariant filters with fading memory [8].

These activity-dependent synapses, when added to the network, allow for different forms of dynamical networks that can process time-varying patterns [9, 10]. Examples of how these synapses could contribute to visual cortical responses include direction selectivity [11] and automatic gain control [12]. The simulation time of spiking networks with different types of activity-dependent synapses consisting of different time constants will increase significantly. This simulation time can be shortened by using a hardware implementation of a network with spiking neurons and these activity-dependent synapses.

Here, we describe a circuit model of short-term synaptic dynamics based on the silicon implementation of synaptic depression and facilitation in [13]. The dynamics of this circuit model is qualitatively comparable to the dynamics of two theoretical models [14]: the phenomenological model from [6, 9, 15] and the model from [5, 12]. Measurements from these circuits on a fabricated chip show how these synapses filter the inputs to a leaky integrate-and-fire neuron under transient and steady-state conditions.

The dynamics of short-term plastic synapses are dependent on the frequency of the presynaptic input. In the case of a neuron which is stimulated through a depressing synapse by a regular input spike train, the firing rate of the neuron decreases over time due to the decrease in synaptic input with each presynaptic spike. Interestingly, a class of neurons in the cortex also adapt their firing rate over time in response to a regular spike input through a normal synapse. This output adaptation mechanism is non-input specific whereas the first mechanism involves the filtering of specific inputs.

The inclusion of these short-term synapses into networks of neurons allow processing of time-varying inputs. However, the simulation time of such networks on a computer increases substantially as more different types of time constants are added to the circuits. The previous constructions of neuron circuits ranging from Hodgkin-Huxley models of neurons [16, 17] to integrate-and-fire neurons [18, 19, 20, 21, 22], together with long-time constant learning synapses [23, 24] and short-term dynamic synapses [13] can be used to develop realistic, real-time, low-power, and spike-based networks.
2. SYNAPSES

Synaptic circuits have been implemented using very few transistors [13, 25]. However, their dynamics are usually different from the exponential dynamics of synaptic models used in simulations. To implement the exponential dynamics, we would have to use a linear resistor to obtain the exponential dynamics. A transistor can act as a linear resistor as long as the terminal voltages satisfy certain criteria. Additional circuitry would be needed to satisfy these criteria, thus increasing the final size of the circuit. One alternative is to replace the linear-resistor dynamics with diode dynamics which is easily obtained with one diode-connected transistor. We will discuss the difference between the diode-connected transistor dynamics and the exponential dynamics for the different types of synapses.

2.1. Normal synapses

In simulations, the synaptic current \( i(t) \) is either treated as a point current source at the time of the spike \( t_{sp} \):

\[
i(t) = I_f \delta(t - t_{sp}),
\]

where \( I_f \) is a fixed current, or as a current source with a finite decay time:

\[
i(t) = I_f \frac{t}{\tau_g} (1 - e^{-t/\tau_g}),
\]

where \( \tau_g \) is the time constant of the decay and \( t \) is measured right after a spike.

The point current source can be implemented by two transistors (e.g., \( M_2 \) and \( M_3 \) in Figure 1a). If we need a synaptic current with a finite decay time, we include the current-mirror circuit \( M_1, M_4 \), and \( C \). Unlike the dynamics in (4), the synaptic current \( I_d \) has a 1/t decay dynamics [25] rather than exponential dynamics. The decay of \( I_d \) is described by

\[
I_d(t) = \frac{I_{d0}}{1 + (AI_{d0}/Q_T)},
\]

where \( Q_T = CU_T, A = e^{(\kappa V_{dd} - V_{gain})/U_T}, U_T \) is the thermal voltage, and \( I_{d0} \) is the value of \( I_d \) at the time of the spike \( t = t_{sp} \).

2.2. Short-term synaptic dynamics

Dynamical synapses can be depressing, facilitating, or a combination of both. In a depressing synapse, the synaptic strength decreases after each spike and recovers towards its maximal value with a time constant \( \tau_d \). In facilitating synapses, the strength increases after each spike and recovers towards its minimum value with a time constant \( \tau_f \). Two prevalent models that are used in network simulations and also for fitting physiological data are the phenomenological model in [6, 9, 15] and the model from [5, 12]. We only consider the dynamics of the model from Abbott et al. [12] in this work.

2.2.1 Simulation model of short-term dynamic synapses

The dynamics of the depressing synapse is similar to the adaptation dynamics of the photoreceptor. Both elements code primarily changes in the input rather than the absolute level of the input. The photoreceptor amplifies the contrast of the visual signal and has a low gain to background illumination. The output of the depressing synapse codes primarily changes in the presynaptic frequency. The synaptic strength adapts to a steady-state value that is approximately inversely dependent on the input frequency.

Thus, the depressing synapse acts like a band-pass filter to spike rates, much like the photoreceptor has a band-pass response to illumination. The facilitating synapse, on the other hand, acts like a low-pass filter to changes in spike rates. A step increase in presynaptic firing rate leads to an increase in the synaptic strength. Both types of synapses can be treated as time-invariant fading memory filters [8].

In the theoretical model from Abbott et al. [12], the depression in the synaptic strength is defined by a variable \( D \) varying between 0 and 1. The synaptic strength is given by
$gD(t)$ where $g$ is the maximum synaptic strength. The recovery dynamics of $D$ is described by

$$
\tau_d \frac{dD}{dt} = 1 - D,
$$

where $\tau_d$ is the recovery time constant of the depression, and the update dynamics is

$$
D(t_+^\ast) = dD(t_-^\ast),
$$

where $d$ ($d < 1$) is the amount by which $D$ is decreased right after the spike. In the case of a regular spike train, the average steady-state value of $D$ is

$$
\langle D \rangle = \frac{1 - e^{-1/\tau_d}}{1 - de^{-1/\tau_d}}.
$$

In the facilitating case, the facilitation is defined by a variable $F \geq 1$. The synaptic strength is $g_F F(t)$, where $g_F$ is the maximum synaptic strength. The recovery dynamics of $F$ is

$$
\tau_f \frac{dF}{dt} = 1 - F,
$$

where $\tau_f$ is the time constant in which $F$ recovers exponentially back to 1.

The update dynamics is now additive instead of subtractive:

$$
F(t_+^\ast) = F(t_-^\ast) + f,
$$

where $f$ ($f < 1$) is the amount by which $F$ is increased right after the spike. The variable $F$ is updated additively because multiplicative facilitation can lead to increases of synaptic strength without bounds, especially at high frequencies, for the recovery dynamics in (7).

### 2.2.2 Circuit model of short-term dynamic synapses

As before, we replace the exponential dynamics in (4) with the diode-connected transistor dynamics. This replacement gives rise to the synaptic depressing circuit in Figure 1b which was proposed in [13]. The new circuit gives rise to the following recovery dynamics for the depressing variable $D$:

$$
\frac{dD}{dt} = M(1 - D^{1/\kappa}),
$$

where $M$ is the equivalent of $1/\tau_d$ and $\kappa$ is a transistor parameter which is less than 1 in subthreshold operation. The update dynamics are similar to (5):

$$
D(t_+^\ast) = dD(t_-^\ast).
$$

### 2.2.3 Depressing circuit

The detailed analysis leading to (9) and (10) for $D$ is described in [14]. The voltage $V_x$ determines the maximum synaptic strength $g$ while the synaptic strength $gD$ or $I_{syn}$ is exponential in the voltage $V_x$. The subcircuit consisting of transistors $M_1$, $M_2$, and $M_3$ controls the dynamics of $I_{syn}$.

The presynaptic input goes to the terminal of $M_3$ which acts like a switch. During a presynaptic spike, a quantity of charge (determined by $V_d$) is removed from the node $V_x$. In between spikes, $V_x$ recovers towards $V_a$ through the diode-connected transistor $M_1$. Also during the presynaptic spike, transistor $M_4$ turns on and the synaptic current $I_{syn}$ flows into the membrane potential of the neuron. We can convert the $I_{syn}$ current source into an equivalent current $I_f$ with some gain and a “time constant” through the current-mirror circuit consisting of $M_a$, $M_b$, and the capacitor $C_2$, and by adjusting the voltage $V_{gain}$.

The synaptic strength is given by

$$
I_{syn}(t) = I_{syn} e^{V_x/U_t} = gD(t),
$$

where $g = I_{syn} e^{V_x/U_t}$, and

$$
D(t) = \left( e^{(V_{dd} - V_x)/U_t} I_{op} \right) / I_{f}(t),
$$

where $I_f := I_{op} e^{(V_{dd} - V_x)/U_t}$. The recovery time constant (1/M) of $D$ is set by $V_a$ ($M = (I_{op}/Q)t e^{-(1/\kappa)(V_{dd} - V_x)/U_t}$).

Because it is difficult to compute a closed-form solution for (9) for any value of $\kappa$, we look at a simple case where $\kappa = 0.5$ and solve for $D(t)$ after a spike has occurred at $t = t_0$.

The actual value of $\kappa$ changes for different operating conditions and also depends on fabrication parameters. The recovery equation in (13) includes the current dynamics of the diode-connected transistor ($M_1$ in Figure 1b) in the region when $D$ is close to the maximum value. The equation for $D(t)$ is then

$$
\frac{dD}{dt} = M(1 - D^{1/2}),
$$

which simplifies to

$$
\Rightarrow D(t) = \frac{D(t_0) + D(t_0) e^{2Mt} - 1 + e^{2Mt}}{D(t_0) + D(t_0) e^{2Mt} + 1 + e^{2Mt}}
$$

$$
= \frac{D(t_0) \cosh(Mt) + \sinh(Mt)}{\cosh(Mt) + D(t_0) \sinh(Mt)}.
$$

If $D$ is not close to its maximum value of 1, we can approximate the dynamics to $dD/dt = M$ (regardless of $\kappa$) and solve for $D(t)$:

$$
D(t) = Mt + D(t_0).
$$

In this regime, $D(t)$ follows a linear trajectory. Note that the same is true for (4) when $t \ll \tau_d$.

### 2.2.4 Model of facilitating synapse

The schematic for the facilitating synapse is shown in Figure 2. The difference in this circuit from the depressing synaptic circuit is that the node $V_x$ goes to the gate of a pFET instead of an nFET. The synaptic strength is now

$$
I_{syn}(t) = I_{op} e^{(V_{dd} - V_x)/U_t} \text{ and is directly proportional to the current variable } I_{f} = I_{op} e^{(V_{dd} - V_x)/U_t},
$$

so

$$
I_{syn}(t) = g_f F(t),
$$

where $g_f = I_{op} e^{(V_{dd} - V_x)/U_t}$ and $F(t) = 1/D(t)$.

Note that if $\kappa = 1$, then the equation reduces to (4).
3. NEURON CIRCUIT

The dynamics of the neuron circuit are similar to that of a leaky integrate-and-fire neuron with a constant leak (Figure 3). The circuit is described in detail in [26, 27]. It is a modified version of previous designs [18, 22] and also includes the circuitry which models firing-rate adaptation [21, 25] frequently seen in pyramidal cells. The equation for the depolarization of the soma is as follows:

$$C_m \frac{dV_m(t)}{dt} = i(t) - I_{\text{leak}} - I_{\text{ahp}}, \quad V_m(t) < V_{\text{thresh}}, \quad (20)$$

where $i(t)$ is the synaptic current to the soma, $I_{\text{leak}}$ is the leakage current, and $I_{\text{ahp}}$ is the after-hyperpolarization potassium ($K$) current which causes the adaptation in the firing rate of the cells.

When $V_m(t)$ increases above $V_{\text{thresh}}$ at $t = t_h$ (the time of spike), it increases by a step increment determined by the capacitive coupling $C_1$ and $C_m$. The output $V_o$ becomes active at this time and turns on the discharging current path through transistors $M_3$ and $M_6$. The time during which $V_o$ remains high, $T_p$, depends on the time taken for $V_m$ to discharge below $V_{\text{thresh}}$. In this design, the pulse width $T_p$ is determined by the rate at which $V_m$ is discharged which in turn depends on the difference between the input current $I_d$, the leak current $I_{\text{leak}}$, and the current $I_{\text{refr}}$. In other designs, $V_m$ is reset immediately below $V_{\text{thresh}}$ when $V_o$ becomes active because either the input current is blocked from charging the membrane or the current $I_{\text{refr}}$ is much larger than the input current. The refractory period $T_R$ is determined by $V_{\text{refr}}$ which keeps $V_o$ high so that $I_d$ cannot charge up the membrane. The spike output is taken from the node $V_o$.

The time taken for the neuron to charge up to threshold is

$$T_l = (C_m + C_1) \frac{V_{\text{thresh}}}{i - I_{\text{leak}}}, \quad (21)$$

and, in the case of a constant input current $I_d$, the spike rate is

$$r = \frac{1}{T_l + T_p + T_R}. \quad (22)$$

**Spike adaptation**

Transistors $M_1$ to $M_5$ and the capacitor $C_a$ in Figure 3 implement the spike adaptation mechanism. The data in Figure 8b show the adaptation of the output spike rate when the neuron was driven by a 100 Hz regular input spike train through a nonplastic synapse. The amount of charge dumped on $C_a$ is determined by $V_{\text{cs}}$. The dynamics of the current mirror circuit ($M_{3}, M_{4},$ and $C_a$) are used to set the dynamics of the $I_{\text{ahp}}$ current. The adapted spike rate is reduced from the initial rate by a factor $y = (1 + A_e Q_d/Q_{th})$ [21], where $Q_d$ is the charge that is dumped onto the capacitor $C_a$ during each postsynaptic spike (i.e., when $V_o$ is high), $Q_{th}$ is the amount of charge needed for $V_m$ to reach threshold, and $A_e = e^{eV_i}$.

4. TRANSIENT RESPONSE

The data in the figures in the remainder of the paper are obtained from a multineuron circuit with depressing and
facilitating synapses fabricated in a 0.8 μm CMOS process. To show the effect of synaptic depression, we measured $V_o$ over time as the input was driven by a regular spike train as shown in Figure 4. Remember that the synaptic strength $gD$ is exponential in $V_x$. When there are no spikes, $V_x$ is approximately equal to $V_d$. During a spike, $V_x$ is decreased by an amount dependent on $V_d$. This node recovers in-between spikes at a rate that depends on the difference in voltage between $V_x$ and $V_d$. The recovery rate is faster when $V_x$ is far from $V_d$. The dependence of the recovery rate on this difference is due to the current-mirror circuit dynamics. The parameter $V_d$ controls both the synaptic strength and the recovery time constant. For a fixed $V_d$, the dynamics and the steady-state value of $D$ can be set by changing $V_d$ (or $d$) as shown in Figure 4b.

The subsequent effect on the neuron is seen by measuring the EPSP response when a presynaptic spike occurs. The EPSPs recorded when the neuron was stimulated by a regular spiking input through these synapses are shown in Figure 5. The parameters of the synapse and the neuron have been tuned so that the EPSPs do not add up with each incoming spike. In Figure 5a, the EPSP amplitude decreases with each incoming spike, while in Figure 5b the amplitude increases instead. The EPSPs in response to the first few spikes in Figure 5b are not observable because the leak current is larger than the synaptic current. The amplitude reaches a steady-state value after a finite number of spikes. The number of spikes needed to reach a steady state can be tuned by the parameters $V_a$ and $V_d$. Different $V_d$ and $V_f$ values lead to different amounts of depression and facilitation as shown in Figure 6. The fits between the circuit model and the simulation model are described in [14].

### 4.1. Depression and facilitation

We can obtain a combination of facilitation and depression dynamics in $I_d$ from the depressing synaptic circuit in Figure 1b by choosing certain circuit parameters. The output of the current-mirror synaptic circuit in Figure 1a can produce paired-pulse facilitation [25]. The equation for $I_d$ is the same as (15) for $I_{syn}$ in the facilitating synapse circuit $I_d = g_{ff}F_d(t)$, where $g_{ff} = I_{op}e^{\xi(V_{dd}-V_{low})/U_T}$.

\[ F_d(t) = \frac{I_{f,df}(t)}{e^{\xi(V_{dd}-V_{low})/U_T}I_{sp}}, \tag{23} \]

and $I_{f,df} := I_{op}e^{\xi(V_{dd}-V_{low})/U_T}$. This equation also applies to $I_d$ in Figure 1b. The difference between both circuits is that the factor $f_d$ that determines the change in $F_d$ right after a spike is constant in one circuit and varies for the other circuit ($f_d = e^{\xi(V_{dd}-V_{low})/U_T}$). In the depressing synaptic circuit, $I_{ff}$ is not constant and depends on the input spike activity, whereas in the current-mirror synaptic circuit, $I_{ff} (= I_f)$ is constant. So, for certain parameter settings in the depressing circuit, the EPSPs show initial facilitation before depressing in response to a step input of a regular 100 Hz spike train as shown in Figure 7.

### 4.2. Depression or adaptation

Both the synaptic depression and spike adaptation mechanisms lead to adaptation in the neuron’s firing rate to a step increase in the input rate as shown in Figure 8. In fact, the transient response to a step increase in the rate of a regular spiking input is almost indistinguishable using either mechanism. Although both mechanisms lead to gain control in the neuron, the individual mechanisms are sensitive to different signals. Synaptic depression gives rise to sensitivity in input rate changes whereas spike adaptation makes the neuron sensitive to changes in the neuron's output rate. For example, if one of the inputs to the neuron is highly active, the spike adaptation mechanism of the neuron reduces its sensitivity to the continuous large input current regardless of the origin of the large input. On the other hand, the synaptic depressor mechanism only turns down the sensitivity of that particular active input so the neuron is still selective to all other inputs. The role of depression and facilitation in implementing gain control has been described in [12, 28, 29].

### 5. STEADY-STATE RESPONSE

The dependence of the steady-state values of $D$ and $F$ on the presynaptic frequency can be determined easily in the case of a regular spiking input. In the case of depression, we use (10) and (13) to compute the steady-state value of $D$.
Analog VLSI Circuits for Short-Term Dynamic Synapses

Figure 4: Response of $V_x$ to a regular spiking input of 20 Hz with different values of $V_d$. (a) Change of $V_x$ over time. It is decreased when an input spike arrives and it recovers back to the quiescent value at different rates dependent on its distance from the resting value of about 0.33 V. (b) The steady-state value and dynamics of $V_x$ can be tuned by changing $V_d$.

\[ D_{ss} = \frac{(-1+d)(1+e^{2M/r}) + \sqrt{4d(-1+e^{2M/r})^2 + (1-d)^2(1+e^{2M/r})^2}}{2d(-1+e^{2M/r})}. \]  
(24)

For the simpler dynamics of $dD/dt = M$, we use (14) instead of (13) and obtain a simpler expression for $D_{ss}$:

\[ D_{ss} = \frac{M}{(1-d)r}. \]  
(25)

Thus the steady-state EPSP amplitude is inversely dependent on the presynaptic rate $r$ as shown in Figure 9. The form of the curve is similar to the results obtained in the work of Abbott et al. [12] where the data can be fitted with (6).

In the case of facilitation, we use (16) and (18) to compute the steady-state value, $F_{ss}$:

\[ F_{ss} = \frac{(-1+f)(1+e^{2M/r}) + \sqrt{4f(1-e^{2M/r})^2 + (1-f)^2(1+e^{2M/r})^2}}{2f(-1+e^{2M/r})}. \]  
(26)

In the simpler case, where $dF/dt = -MF(t)^2$,

\[ F_{ss} = \frac{(f - 1)r}{fM}. \]  
(27)

Figure 5: Transient response of a neuron (by measuring its membrane potential, $V_m$) when stimulated by a regular spiking input through a depressing synapse (a) and a facilitating synapse (b). The leak current of the neuron has been adjusted so that the neuron does not reach threshold. (a) The EPSP decreases with each incoming input spike for a depressing synapse. (b) The EPSP increases with each incoming input spike for a facilitating synapse. The initial EPSPs are not seen because the leak current of the neuron is larger than the synaptic current.
which shows that the steady-state value of $F$ is linear in the presynaptic rate and it does not increase without bounds as in the case of the exponential dynamics model for $F$.

### 6. DIRECTION SELECTIVITY USING SHORT-TERM SYNAPTIC DEPRESSION

Depressing synapses have been implicated in the appearance of certain visual cortical cell responses, for example, direction-selectivity. Because these synapses act like a high-pass filter in the frequency domain, the response of the neuron shows a phase advance over its response if stimulated through a nonplastic synapse. This feature was exploited in a model that described the direction-selective responses of visual cortical neurons [11]. In this model, the neuron was driven by the outputs of a set of cells in the lateral geniculate nucleus (LGN) through depressing synapses and the outputs of a spatially shifted set of LGN cells through nondepressing synapses. We have attempted the same experiment by driving a “cortical neuron” on our chip with spikes recorded from an LGN cell in the cat visual cortex during stimulation with a drifting sinusoidal grating (courtesy of K. Martin) and a temporally shifted version of these spikes. An example of the direction-selective response is shown in Figure 10 [30]. The direction-selective results were qualitatively similar to the data in [11]. This chip has been used for exploring other spike-based cortical models, for example, orientation selectivity [27].
7. CONCLUSION

The addition of short-term dynamical synapses to neuronal networks increases the computational power of such networks, especially in processing time-varying inputs. Because of the similarity of the dynamics of the silicon models to the theoretical models, a silicon network of leaky integrate-and-fire neurons which incorporate these synapses can provide an alternative to network simulations on the computer.

This type of spike-based network runs in real-time and the computational time does not scale with the size of the network. This chip is a basic module in a reconfigurable, rewireable, and spike-based system that provides ease for prototyping computational models. The system can also be useful for possible applications, for example, in interfacing with neural wetware.
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REFERENCES

[1] C. van Vreeswijk and H. Sompolinsky, “Chaotic balanced state in a model of cortical circuits,” Neural Computation, vol. 10, no. 6, pp. 1321–1371, 1998.

[2] N. Brunel, “Dynamics of sparsely connected networks of excitatory and inhibitory spiking neurons,” Journal of Computational Neuroscience, vol. 8, no. 3, pp. 183–208, 2000.

[3] K. Tárczy-Hornoch, K. A. Martin, J. J. Jack, and K. J. Stratford, “Synaptic interactions between smooth and spiny neurones in layer 4 of cat visual cortex in vitro,” Journal of Physiology, vol. 508, no. Pt 2, pp. 351–363, 1998.

[4] K. Tárczy-Hornoch, K. A. Martin, K. J. Stratford, and J. J. Jack, “Intracortical excitation of spiny neurones in layer 4 of cat striate cortex in vitro,” Cerebral Cortex, vol. 9, no. 8, pp. 833–843, 1999.

[5] J. A. Varela, K. Sen, J. Gibson, J. Fost, L. F. Abbott, and S. B. Nelson, “A quantitative description of short-term plasticity at excitatory synapses in layer 2/3 of rat primary visual cortex,” J. Neurosci., vol. 17, no. 20, pp. 7926–7940, 1997.

[6] H. Markram, Y. Wang, and M. Tsodyks, “Differential signaling via the same axon of neocortical pyramidal neurones,” Proc. Natl. Acad. Sci. USA, vol. 95, no. 9, pp. 5323–5328, 1998.

[7] A. Reyes, R. Lujan, A. Rozov, N. Burnashev, P. Somogyi, and B. Sakmann, “Target-cell-specific facilitation and depression in neocortical circuits,” Nat. Neurosci., vol. 1, no. 4, pp. 279–285, 1998.

[8] W. Maass and E. D. Sontag, “Neural systems as nonlinear filters,” Neural Computation, vol. 12, no. 8, pp. 1743–1772, 2000.

[9] M. Tsodyks, K. Pawelzik, and H. Markram, “Neural networks with dynamic synapses,” Neural Computation, vol. 10, no. 4, pp. 821–835, 1998.

[10] W. Maass and A. Zador, “Computing and learning with dynamic synapses,” in Pulsed Neural Networks, W. Maass and C. Bishop, Eds., chapter 6, pp. 521–536, MIT Press, Cambridge, Mass, USA, 1999.

[11] F. S. Chance, S. B. Nelson, and L. F. Abbott, “Synaptic depression and the temporal response characteristics of v1 cells,” The Journal of Neuroscience, vol. 18, no. 12, pp. 4785–4799, 1998.

[12] L. F. Abbott, J. A. Varela, K. Sen, and S. B. Nelson, “Synaptic depression and cortical gain control,” Science, vol. 275, no. 5297, pp. 220–224, 1997.

[13] C. Rasche and R. Hahnloser, “Silicon synaptic depression,” Biological Cybernetics, vol. 84, no. 1, pp. 57–62, 2001.

[14] M. Boegerhausen, P. Suter, and S.-C. Liu, “Modeling short-term synaptic depression in silicon,” Neural Computation, vol. 15, no. 2, pp. 331–348, 2003.

[15] M. V. Tsodyks and H. Markram, “The neural code between neocortical pyramidal neurones depends on neurotransmitter release probability,” Proc. Natl. Acad. Sci. USA, vol. 94, no. 2, pp. 719–723, 1997, erratum in Proc. Natl. Acad. Sci. USA, vol. 94, no. 10, pp. 54–59, May 13.

[16] M. Mahowald and R. Douglas, “A silicon neuron,” Nature, vol. 354, no. 6354, pp. 515–518, 1991.

[17] G. N. Patel and S. P. DeWeerth, “Analog VLSI Morris-Lecar neuron,” Electronics letters, vol. 33, no. 12, pp. 997–998, 1997.

[18] C. Mead, Analog VLSI and Neural Systems, Addison-Wesley, Reading, Mass, USA, 1989.

[19] R. Sarapeshkar, L. Watts, and C. Mead, “Refractory neuron circuits,” Tech. Rep. CNS-TR-92-08, California Institute of Technology, Pasadena, Calif, USA, 1992.

[20] J. F. Lazzaro and J. Wawrzynek, “Low-power silicon axons, neurons, and synapses,” in Silicon Implementations of Pulse Coded Neural Networks, M. E. Zaghoul, J. L. Meador, and R. W. Newcomb, Eds., pp. 153–164, Kluwer Academic Press, Norwell, Mass, USA, 1994.

[21] K. A. Boahen, “The retinomorphic approach: Pixel-parallel adaptive amplification, filtering, and quantization,” Analog Integrated Circuits and Signal Processing, vol. 13, no. 1–2, pp. 53–68, 1997.

[22] A. van Schaik, “Building blocks for electronic spiking neural networks,” Neural Networks, vol. 14, no. 6/7, pp. 617–628, 2001, Special Issue on Spiking Neurons in Neuroscience and Technology.

[23] P. Hadser, C. Diorio, B. A. Minch, and C. Mead, “Single transistor learning synapses,” in Advances in Neural Information Processing Systems, vol. 7, pp. 817–824, MIT Press, Cambridge, Mass, USA, 1995.

[24] P. Häfliiger and M. Mahowald, “Spike based normalizing Hebbian learning in an analog VLSI artificial neuron,” in Learning on Silicon, G. Cauwenberghs and M. A. Bayoumi, Eds., pp. 131–142, Kluwer Academic Press, Norwell, Mass, USA, 1999.

[25] K. A. Boahen, Retinomorphic Vision Systems: Reverse Engineering the Vertebrate Retina, Ph.D. thesis, California Institute of Technology, Pasadena, Calif, USA, 1997.

[26] G. Indiveri, “Modeling selective attention using a neuromorphic analog VLSI device,” Neural Computation, vol. 12, no. 2, pp. 2857–2880, 2000.

[27] S.-C. Liu, J. Kramer, G. Indiveri, T. Delbrück, T. Burg, and R. Douglas, “Orientation-selective aVLSI spiking neurons,” Neural Networks, vol. 14, no. 6–7, pp. 629–643, 2001, Special Issue on Spiking Neurons in Neuroscience and Technology.

[28] W. Senn, I. Segev, and M. Tsodyks, “Reading neuronal synchrony with depressing synapses,” Neural Computation, vol. 10, no. 4, pp. 815–819, 1998.

[29] V. Matveev and X. Wang, “Differential short-term synaptic plasticity and transmission of complex spike trains: to depress or to facilitate?,” Cerebral Cortex, vol. 10, no. 11, pp. 1143–1153, 2000.

[30] S.-C. Liu, “Simple cortical modeling with aVLSI spiking neurons and dynamic synapses,” in ZNZ Symposium, University of Zurich, Zurich, 2001.

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