Designing elements of MOS circuits resistant to destabilizing factors

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Abstract. Some reliability limitations are the result of increasing electric field strength in MOS devices where the supply voltage does not decline in proportion to the decrease in the size of components. Degradation of devices occurs due to the action of hot carriers and breakdown of very thin films of the gate insulating oxide. The problems of decreasing reliability associated with the exposure to hot carriers and with degradation of circuit characteristics under the influence of these carriers are aggravated with a decline in the geometric dimensions of elements in CMOS integrated circuits. The parameters of the degradation process of field-effect n-MOS transistors are carried out. They are caused by the tunneling injection of carriers which differ in the oxide type: standard, grown by thermal oxidation, thermally nitrided, which has a number of advantages over the previous one, in particular, higher resistance to the action of hot electrons, and reoxidized thermally nitrided, characterized by a smaller number of electron traps formed during nitriding, as well as generated surface states. The modes of oxide production have a significant effect on its dielectric properties including the density of charged traps and surface states and resistance to the generation of the latter at high fields which should lead to noticeable differences between MOS-FET, and gate oxide dielectrics of various types.

1. Introduction

In recent decades, the miniaturization of microelectronic devices obeying Moore’s law has led to a decrease in the size of contemporary microelectronic devices (MED) [1]. Besides the reduction in physical size, the miniaturization process has led to a decrease in MED parameters such as operating voltage (supply voltage), power consumption, as well as a rise in the degree of integration, speed and MED output characteristics. However, despite the decrease in supply voltage and power consumption in modern MEDs, the problem of hot media effects still occupies one of the crucial positions in the degradation of device performance and, as a consequence, in determining the reliability of MEDs. Studies show that one of the basic reasons for the onset of parametric failure of field-effect transistors is the degradation of appliance characteristics caused by the formation of surface states at the semiconductor/dielectric interface [2–4].
2. Problem statement and experiment
A natural limiting factor for the gate oxide thickness in MOS GSI is a magnification in the tunneling current through the oxide film. Although the gate tunneling current increases exponentially with decreasing gate oxide thickness, the ratio of this current to the drain current is not so high. Changes in the drain current and electron tunneling current $I_{Ga}$ with a change in the gate oxide thickness for two different channel lengths, obtained as a result of modeling, show that the ratio of the tunneling current to the drain current decreases in proportion to the square of the channel length which can only confirm the trend towards miniaturization of GSI components.

Figure 1 shows the dependence of the minimum channel length on the gate oxide thickness for a transition depth of 0.35 μm at various degrees of substrate doping.

![Graph showing the dependence of the minimum channel length on the gate oxide thickness for a transition depth of 0.35 μm at various substrate doping levels.]

**Figure 1.** Dependence of the minimum channel length on the gate oxide thickness for a transition depth of 0.35 μm at a substrate doping level: 1 – $10^{17}$ cm$^{-2}$; 2 – $4 \times 10^{16}$ cm$^{-2}$; 3 – $10^{16}$ cm$^{-2}$; 4 – $4 \times 10^{15}$ cm$^{-2}$

The main factor that makes it possible to reduce the generation of hot carriers is a decrease in the electric field strength and separation of the current maximum path and the position of the maximum electric field strength. The source of hot carriers can be hot channel electrons and electron-hole pairs arising during impact ionization [5, 6]. Avalanche injection of hot electrons under conditions when the gate voltage is less than the channel voltage leads to intense degradation of devices [7]. The total number of hot carriers in impact ionization is the integration of results determined by current density and impact ionization intensity. Impact ionization depends exponentially on the reciprocal of the electric field strength.

A decrease in the field strength reduces the electron energy, and therefore there is a lower probability of injection of hot carriers and damage to the Si-SiO$_2$ interface. Another significant factor in suppressing the injection of hot carriers is the region depth in which impact ionization occurs. The shallower the depth becomes, the greater the possibility of reaching the boundary between silicon and silicon dioxide and hot carriers takes place.

The injection probability can be represented by the ratio:

$$\exp\left(-\frac{\Phi_i}{k \star T_c}\right) \star \left(-\frac{x}{\mathcal{A}}\right),$$
where $\Phi$ – is the energy required to overcome the barrier and damage the silicon-silicon dioxide interface, $T_c$ – electron temperature and $x$ – distance to the silicon-silicon dioxide interface, $\lambda$ – average free energy-dependent path.

The second exponential component describes the probability that electrons will reach the silicon-silicon dioxide interface without collisions at x distance. Limiting the position of the injected hot carriers with respect to the gate edge reduces the effect of series resistance especially in devices with a lightly doped channel.

The capture mechanism of hot carriers includes the capture in the bulk of the oxide and the generation of traps by the silicon-silicon dioxide boundary region, traps of hot holes and hot electrons. The generation of traps is the basic reason for the degradation of device characteristics caused by the trapping of holes and electrons. The hot media capture mechanism can be divided into three components:

- capture of positive charges by hole capture centers;
- neutralized capture centers;
- capture of slow electrons.

Charge trapping in the oxide and the silicon-silicon dioxide interface leads to a shift in the threshold voltage, a change in the slope of the subthreshold characteristic, and a decrease in conductivity and the linear region current. Possibilities of regulating characteristics exist by changing the energy of holes and electrons in the region of the silicon surface at the gate edges. Hot channel electrons are the main source of hot carriers at high gate biases. Most of the hot channel electrons move parallel to the silicon surface. These hot channel electrons are reoriented relative to the silicon surface using a scattering process, and then they are injected into the silicon dioxide.

The injection of hot electrons and holes into the gate dielectric of short-channel MOS field-effect transistors is inhomogeneous along the channel and is maximally near the diffusion region of the drain and beyond. As a result, the properties of the Si/SiO$_2$ interface change unevenly due to the build-in of a charge into the dielectric and the creation of fast surface states which leads to a change in the electrical parameters of transistors and a decrease in their reliability. However, due to the changes locality, such a defect is hard to evaluate from the device electrical characteristics [8].

Long-channel MOS structures with adjacent injection diodes which are the source of charge carrier injection into the dielectric, were used to study the effect of injection inhomogeneity. Both symmetric and asymmetric electron injection configurations can be realized in such structures.

An injection diode located parallel to the channel length of the transistors in the array of n-channel devices provides symmetric injection along the transistor length since the distance between the active region of the transistor and the diode edge is constant. Injection from a diode adjacent to the drain/source diffusion regions is asymmetric with a maximum flux in the transistor region that is closest to the diode.

The injected carriers that enter the gate oxide area are accelerated towards the interface. Most of them have energy preventing from overcoming the barrier and getting into the dielectric, and make up the source/drain current. Besides, carriers from the depletion regions surrounding the drain and source junctions are added to it. The carriers trapped in a dielectric can interact with it, be captured by traps, or create surface states. The carriers that have passed through the dielectric without being captured form the gate current. The gate current can be considered equal to the number of carriers arriving at the silicon-oxide interface since only an insignificant fraction of the carriers injected into the dielectric is captured or returned.

The obtained values of the gate current as a density function of injected electrons are shown in Figure 2.
Ion implantation processes are used in the formation of MOS-field-effect transistors. In this regard, the study of the defect effects on the threshold voltage of MOS-FET, formed in the processes of ion implantation and sputtering, was carried out. The n-channel MOS-FET was used as test appliances. The gate length and channel width were 2 and 10 μm, respectively, and the gate oxide thickness was 50 nm. Figure 3 shows the structure of the test appliance. Its peculiarity lies in the connection of polysilicon tracks with the source and drain. The appliance characteristics were measured before and after ion bombardment processes, and after high-temperature annealing.

As ions with \(5 \times 10^{15} \text{ cm}^{-2}\) dose were implanted at 25 keV energy. The ion energy did not exceed 100 eV during the sputtering of Al. The shift in the threshold voltage due to both the direct effect of the process and subsequent injection of hot electrons was determined before and after each process. The injection of hot electrons was measured at a field strength in the gate oxide layer of 1.17 MV/cm, a current density of 5 μA/cm² in the oxide, and a total number of injected electrons \(3.1 \times 10^{16} \text{ cm}^{-2}\).

Figure 4 demonstrates the process of changing the threshold voltage due to ion implantation and post-implantation annealing.
Figure 4. Process of changing the threshold voltage due to ion implantation and post-implantation annealing (abscissa 1 – initial value without ion implantation; 2 – As implantation; 3 – 3 h in N₂; 4 – 30 min in H₂/N₂; 5 – 6 h in N₂)

A large negative shift in the threshold voltage takes place after ion implantation. The injection of hot electrons is accompanied by a positive shift in the threshold voltage. The shift is 0.07 V before implantation, and after implantation its value reaches 2.7 V. A strong effect of hot electrons on the threshold voltage of the test MOS-FETs is observed after annealing at 450° C. The negative shift in the threshold voltage after implantation is explained by the positive charge appeared in the gate oxide.

Neutral traps are formed in the oxide during implantation [9]. The traps are capable of capturing the injected hot electrons after which a negative charge, leading to a positive shift in the MOS-FET threshold voltage, is formed in the oxide. Ion implantation is accompanied by the formation of states at the semiconductor-dielectric interface bringing a change in the S factor of the subthreshold characteristics of appliances.

The influence of hot electrons on the change magnitude in the threshold voltage due to injection of hot electrons is relatively weak in samples with a grounded gate during ion implantation. In the case when implantation is carried out at a floating potential at the gate, the injection of hot electrons is accompanied by a significant change in the threshold voltage. Therefore, the degradation of the MOS-FET performance is due to the appearance of a charge on the gate electrode, rather than the effects associated with ion bombardment.

The injection influence of hot electrons on the threshold voltage of MOS-FET at external gate bias was determined to study this effect. Hot electrons were injected at electric field strength of 1.17 MV/cm. The obtained results are shown in Figure 5.
Figure 5. Changes in the threshold voltage due to injection of hot electrons at various electric field strengths

The negative shift of the threshold voltage at strong electric fields in the gate oxide, caused by the gate electrode charge during ion implantation (Fig. 5), is associated with the trapping of holes released during the ionization of lattice atoms by a strong electric field. Subsequent partial compensation of this shift occurs due to the capture of electrons. The large positive shift of the threshold voltage at low fields in the gate oxide can be explained by the presence of neutral electron traps formed during the experiments [10].

It should be noted that the degradation degree of characteristics in the case of hot electrons injection does not depend on the energy of ions bombarding the substrate surface. Since the described degradation is brought about the gate electrode charge, it can be eliminated by grounding the gate during ion bombardment.

Investigations of the degradation process parameters of field-effect n-MOS transistors (MOS-FET) were carried out. Degradation is caused by the tunneling injection of carriers differed in the oxide type: standard grown by thermal oxidation, thermally nitried which has a number of advantages over the previous one, in particular, higher resistance to hot electrons, and reoxidized thermally nitried (NO₂) which has a smaller number of electron traps formed during nitriding, as well as generated surface states. The oxide production modes have a significant effect on its dielectric properties including the density of charged traps and surface states, resistance to the generation of the latter at high fields, which should lead to noticeable differences between MOS-FET and gate oxide dielectrics of various types.

The threshold voltage ($U_{th}$) was used as degradation parameters, as well as the gate subthreshold voltage of (S) swing, the electron field mobility ($\mu_{FE}$), and the maximum slope (GM) in the MOS-FET inverse channel. HS and quasi-static measurements of capacitance-voltage (C-V) characteristics were conducted on condensers with different oxides. Dry oxidation of trichlorethylene at a temperature of 1000 °C and atmospheric pressure for 30 min was applied to obtain a gate oxide; nitriding modes – 1200 °C for 100 seconds; NO₂ – 1000 °C for 60 minutes, and reoxidation of NO₂ – 1000 °C for 30 minutes. The required threshold voltage was achieved by implanting boron ions into the channel. The source and drain areas were formed by As+ ion implantation (80 keV, $4 \times 10^{15}$ cm$^{-2}$). Phosphorus-doped polysilicon gate is of 400 nm thick. The experiments were carried out on appliances of large
geometric sizes to exclude the effect of small dimensions and to ensure the uniformity of the Fowler-Nordheim injection: the length and width of the MOS-FET channel was 50 μm, the capacitor area was 100x200 μm².

The change nature in the threshold voltage with the value of the injected charge (Fig. 6) indicates that the charge captured in the oxide varies from positive to negative, and NO₂-appliances have the greatest stability of Uₜᵣ value.

They are also characterized by the most insignificant degree of S value change (Fig. 7), hence, by the smallest degree of density change of surface states.

Figure 6. Changes in the threshold voltage from the injected charge value: 1 – standard grown thermal oxide; 2 – thermally nitrided; 3 – reoxidized thermally nitrided

Figure 7. Changes in S value from the injected charge: 1 – standard grown thermal oxide; 2 – thermally nitrided; 3 – reoxidized thermally nitrided

The nitriding influence on the values stability of the maximum slope normalized to the capacitance of C1 dielectric is especially noticeable (Fig. 8).
Figure 8. Values stability of the maximum slope normalized to the dielectric capacitance from the injected charge value: 1 – standard grown thermal oxide; 2 – thermally nitrided; 3 – reoxidized thermally nitrided

An additional increase in the mobility upon reoxidation may be associated with the removal of bulk electron traps [11].

Figure 9. Voltage shift magnitude of flat zones from the injected charge value: 1 – standard grown thermal oxide; 2 – thermally nitrided; 3 – reoxidized thermally nitrided

Analysis of quasi-static C-V curves for MOS capacitors confirmed that appliances with standard grown thermal oxide are most susceptible to degradation [12–13]. The magnitude of the voltage shift of flat zones (Fig. 9) is less than the threshold voltage (Fig. 6) which indicates a different amount of charge captured by the surface states.

It is obvious that the supplementary amount of charge is associated with the surface states of the acceptor type. Data comparison in Fig. 7 and Fig. 9 makes it possible to verify that the generation of
such states in capacitors with standard grown thermal oxide occurs faster than in capacitors of the other two types.

3. Conclusion
The conducted studies have shown that the initial positive shift in $U_t$ and $V_{FB}$ values is mainly associated with the trapping of holes in the oxide, while the negative shift – with captured electrons in surface states of the acceptor type, rather than in the oxide. Light nitriding of the oxide causes a sharp negative shift in $U_t$, while deep nitriding can suppress it followed by significant oxidation. It can be possible to reduce the density of surface states in the same way, and thus $U_t$ shift will deposite in the positive direction and in the value of $S$. The use of nitriding, especially combined with reoxidation, is also an efficient way to decrease appliance degradation in terms of parameters such as $GM$ and $\mu_{FE}$.

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