Design of Adaptive Camouflage System Based on SOPC

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Abstract. With the development of electrochromic devices, the requirements for the accuracy and real-time performance of control devices are constantly increasing. For the reliability problems of single-chip microcomputer control technology, through the SOPC development platform, based on the Cydone IV core chip, the hardware design is completed by itself. The Quartus II integrated development environment is used to tailor the NIOSII real-time operating system, to achieve data collection and control. The signal is filtered using an FIR filter. The designed system has the characteristics of real-time, stability, scalability, low power consumption, etc., and can adaptively control the MOFs-based flexible electrochromic device.

1. Introduction

Materials and devices that can change color according to their environment have broad application prospects in the field of visible stealth and artificial intelligence. However, the current color-changing response devices are usually based on stimuli or control means such as gas, light, heat, etc., the color change effect is not obvious, the coordination is poor, and it is difficult to adapt to the changing environment[1][2]. The flexible electrochromic device based on Metal organic Frameworks (MOFs) has the dual function of photoelectric response[3]. By connecting external logic control, the adaptive change of photoelectric characteristics can be realized, so that the optical characteristic parameters of the camouflage body and the environmental optical characteristics can be highly matched and integrated. Commonly used control devices have non-linearity and parameter inconsistency. When replacing the device, the amplifier needs to be re-commissioned due to zero drift of the amplifier. In the signal acquisition and output control technology, the control system is mainly based on CPU or single chip microcomputer. The system speed of controlling operation and operation by software is much lower than that of pure hardware system, and the reliability is not high. System-on-a-Programmable-Chip (SOPC) is a special embedded system: first, it is a system-on-a-chip, which is the main logic function of the entire system by a single chip; second, it is a programmable system with a flexible design that can be reduced, scalable, upgradeable, and has hardware and software programmable functions in the system[4]. This paper aims to develop the system hardware design based on Cydone IV E as the core chip SOPC system development platform. On the hardware platform, the data acquisition and control system is realized through the transplantation and tailoring of the Quartus II integrated development environment and the NIOSII real-time operating system, and the MOFs-based flexible electrochromic device is adaptively controlled.
2. System design
The system adopts MOFs electrochromic materials. The excellent electrochemical stability and porous structure of MOFs meet the requirements of electrochromic materials. After solvothermal reaction, a layer of MOFs film is attached to the conductive glass substrate. These films have good electrochemical stability and excellent electrochromic properties. When different colors of light are irradiated on the material, the material will produce corresponding small current signals. The signal is collected, amplified and filtered by the front-end adjustment circuit, and A/D analog-to-digital conversion is performed on it. The system performs real-time processing on the collected data, and completes the output control of the voltage according to the collected data. By controlling data acquisition, processing and feedback output, high quality acquisition, coordination and feedback of MOFs device signal are realized.

The overall structure design of the system is shown in Figure 1. It consists of front-end adjustment circuit, data acquisition module, data processing module, data transmission control module and embedded software system based on SOPC.

3. Function Module Design
A complete adaptive camouflage system needs to include sensing, analysis, control and discoloration mechanism. The key technology lies in the performance of sensing and discoloration materials and the adaptability of logical control system.

3.1 Data Acquisition Module Design
Since the current range of the input signal is between 0 and 0.5 μA, the measured signal cannot be directly collected and processed. First, the circuit amplifies the signal by AD620 amplifier. The AD620 features high accuracy, low offset voltage and low offset drift[5].And meets the system's requirements for small size, low voltage, and low power consumption.

The system designs a signal conditioning circuit to amplify and filter the analog signal of the input system. The circuit realizes low-pass filtering by programmable amplifier AD620, and filters the analog current signal input from the front end. The analog current signal is converted into analog voltage signal by using MAX4081 chip.

Then low power ADC128S022 chip is used to realize analog-to-digital conversion. ADC128S022 chip communicates with the controller through SPI interface. The communication sequence diagram is shown in the Figure 2.
3.2 Data Processing Module Design

The electrical signals generated by MOFs electrochromic materials under illumination have low noise, low drift and low common mode rejection ratio after passing through preamplifier circuit [6][7]. At this time, the electrical signal is mainly disturbed by power frequency, EMG and other signals. The system customizes the convolution operation unit with the DSP (Digital Signal Processor) multiplier module integrated by FGPA to generate FIR filter with pulsating array structure [8]. The filter adopts full pipeline structure, which can realize real-time signal processing at high speed and without delay.

The transition process of FIR filter has a finite interval, and its system function is equation (1):

\[ H(Z) = \sum_{n=0}^{N-1} h(n)z^{-n} \] (1)

N-1 is the delay period of FIR filter, it can also be expressed by equation (2):

\[ y(n) = \sum_{m=0}^{N-1} h(m)x(n-m) \] (2)

\( x(n) \) is the input sampling sequence, \( h(m) \) is the filter coefficient, N-1 is the delay period of FIR filter, and \( y(n) \) represents the output sequence of the filter. Direct FIR filtering is used as shown in Figure 3.

![Figure 2. ADC128S022 operational timing diagram](image)

![Figure 3. Direct form FIR filter](image)

The FIR filter designed in this system is a low-pass filter, and the difference equation is equation (3):

\[ y(n) = h(0)x(n) + h(1)x(n-1) + \cdots + h(13)x(n-13) \] (3)

The sampling frequency is \( F_s \), the CUT-OFF frequency of the filter is \( F_{co} \), and the length of the filter is \( N_{fir} \), as shown in the following Figure 4:
That Nfir = 128, Nco = 13 notes: Fco = Fs* (Nco / Nfir), h(t) is calculated as Figure 5:

```csharp
CSp[0].real()=1.0;
CSp[0].imag()=0.0;

for (i=0;i<=Nco;i++) { //pass-band
    CSp[i].real()=1.0; //Left page(Gain=1.0)
    CSp[i].imag()=0.0;
    CSp[Nfir-i].real()=1.0; //Right page(Gain=1.0)
    CSp[Nfir-i].imag()=0.0;
}

for(i=Nco+1;i<=(Nfir-Nco-1);i++) { //Rejection band
    CSp[i].real()=0.0; //Gain=0.0
    CSp[i].imag()=0.0;
}
```

Figure 4. Filter length and frequency relationship

Figure 5. Program of h(t) calculation

In this FIR filter, 13 delay units and 14 multiplication units are needed. If this system uses ordinary digital signal processors, delay, multiplication and addition operations can be only performed sequentially in a serial manner. It needs a few instruction cycles to complete this process. By using the parallel structure of FPGA, the output of a FIR filter can be obtained in one clock cycle.

4. System acquisition Test

The system collects and processes the current signals produced by the material irradiated by red and blue light respectively. In this paper, Quartus II and ModelSim software are used to compile and simulate, and the simulation waveform is shown in the Figure 6. The working frequency of Clk is 50MHz, Div_PARM is the clock frequency division setting, SCLK is the clock signal of ADC serial data interface, Channel is the channel selection, Data is the result of ADC. The processed signal meets the design expectation.

(a)Simulation data under red light
(b) Simulation data under blue light

Figure 6. Data acquisition simulation diagram

As the Figure 7 shows, the controller outputs the corresponding voltage. When the chromotropic device loads 2.5V voltage, the device turns red and the current changes from 2.5mA to 0.1mA. It indicates that the resistance of the device changes from 1000Ω to 25000Ω. When 3 V voltage is applied, the device becomes blue and the current changes from 8 mA to 0.2 mA, which indicates that the resistance changes from 400Ω to 15000Ω.

Figure 7. Device current varies with applied voltage

5. Conclusion

According to the application requirement of wearable material control system, FPGA is used as hardware platform and SOPC technology is used to carry NIOS II soft core in the design. The hardware and soft core are flexibly tailored according to the actual control requirements. Materials will produce different current signals under different colors of light. The system collects and analyses them, controls the output of the corresponding rated voltage and feeds back to the material, so that the material can be converted from transparent to red, green and blue. SOPC technology can be used to improve the real-time and accuracy of system data acquisition and control. At the same time, the system has the characteristics of flexible design space, simple debugging and small hardware volume. Reserve more space for subsequent system upgrades.

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