Update the Root of Integrity Tree in Secure Non-Volatile Memory Systems with Low Overhead

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Abstract—Data integrity is important for non-volatile memory (NVM) systems that maintain data even without power. The data integrity in NVM is possibly compromised by integrity attacks, which can be defended against by integrity verification via integrity trees. After NVM system failures and reboots, the integrity tree root is responsible for providing a trusted execution environment. However, the root often becomes a performance bottleneck, since updating the root requires high latency on the write critical path to propagate the modifications from leaf nodes to the root. The root and leaf nodes have to ensure the crash consistency between each other to avoid any update failures that potentially result in misreporting the attacks after system reboots.

In this paper, we propose an efficient and low-latency scheme, called SCUE, to directly update the root on the SGX integrity tree (SIT) by overlooking the updates upon the intermediate tree nodes. The idea behind SCUE explores and exploits the observation that only the persistent leaf nodes and root are useful to ensure the integrity after system failures and reboots, due to the loss of the cached intermediate tree nodes. To achieve the crash consistency between root and leaf nodes, we accurately predict the updates upon the root and pre-update the root before the leaf nodes are modified. Moreover, the SIT root is difficult to be reconstructed from the leaf nodes since updating one tree node needs its parent node as input. We use a counter-summing approach to reconstructing the SIT from leaf nodes. Our evaluation results show that compared with the state-of-the-art integrity tree update schemes, our SCUE scheme delivers high performance while ensuring the system integrity.

I. INTRODUCTION

Non-Volatile Memory (NVM) has demonstrated the salient features of non-volatility, low power consumption and high performance. To guarantee the data security and confidentiality, we need to encrypt the data in NVM. Moreover, the data integrity is also important, which is interpreted that the data can’t be illegally tampered with. The encrypted data need to be further verified to ensure the integrity, which requires security metadata, i.e., counter blocks in counter mode encryption and tree nodes in integrity tree verification. However, due to the persistence of NVM, these security metadata need to be crash consistent and recoverable, to guarantee the NVM systems continue to run safely and efficiently after system failures and reboots.

To ensure data confidentiality, existing works use the counter mode encryption (CME) to encrypt the data in NVM. CME uses counters to generate the one-time padding (OTP) and XORs the OTP with the plaintext/encrypted data to generate the encrypted/plaintext data. CME fetches the counter blocks in the metadata cache in the memory controller in advance. The generation of OTP is in parallel with reading the data from NVM. Therefore, the latency of decryption is hidden by that of reading data. The data integrity is verified by the integrity trees, such as merkle tree (MT), bonsai merkle tree (BMT) [22] and SGX integrity tree (SIT) [8]. In the MT, the user data are iteratively hashed to generate the Keyed-Hash Message Authentication Codes (HMACs) in the intermediate tree nodes and the root. When the user data are modified, the root of MT changes to reflect the modifications of the user data. The data read from NVM also needs to be verified by the cached intermediate tree nodes and the root.

However, MT fails to efficiently support the encryption in NVM. To combine the counter mode encryption with integrity verification, the bonsai merkle tree (BMT) is used. BMT treats the counter blocks as leaf nodes, and the intermediate nodes and root are generated by iteratively hashing the counter blocks. The counters increase to encrypt the new data when being persisted. Moreover, the modifications of the counter blocks in BMT are further propagated to the root. BMT elaborately combines the counter mode encryption and integrity tree by organizing all security metadata (i.e., counter blocks and integrity tree nodes) in the integrity tree. SIT also organizes the counter blocks as leaf nodes in the integrity tree. Unlike BMT, the intermediate tree node in SIT contains eight counters and one HMAC. To exhibit the changes of leaf nodes, the root in SIT needs to be updated in time while the modified leaf nodes are persisted.

The root in the integrity tree is the only trusted base to verify the integrity of data. Since the root is stored in the non-volatile register on chip, the root can’t be attacked. Other tree nodes will be flushed into NVM and tampered by the attackers, and thus the tree nodes in NVM are not trusted. When running the system, the cached intermediate tree nodes can be regarded as the trusted bases since they are directly/indirectly verified by the root. However, when the system failures occur, the cached intermediate nodes are lost, and only the root is trusted. For verifying the leaf nodes after system reboots, we need to timely update the root during the running time.

However, updating root in the integrity tree needs to address two problems: ① the long root update latency: the long latency of propagating the modifications from leaf nodes to root on the critical path, and ② the root crash inconsistency: the crash inconsistency between root and leaf nodes when the system failures occur. Moreover, SIT can’t be reconstructed from leaf nodes since constructing one SIT node requires the counter in the parent node as input.
When the leaf nodes are modified, the modifications need to be propagated to the root for the verification after system failures and reboots. However, propagating the modifications in MT/BMT, i.e., iteratively hashing the data, incurs a long latency. One hash computation needs 80–160 cycles \cite{10,18,25}. Due to the large capacity of NVM, the height of the integrity tree is high, e.g., tens of levels in the integrity tree for the 16GB NVM. Propagating the modifications needs tens of hash computations incurring a long latency of the systems. SIT has the ability to compute the HMACs in parallel. However, SIT needs multiple hash circuits to compute multiple HMACs while the integrity verification is performed in the memory controller with limited computational resources \cite{38}, which consumes the expensive on-chip space and incurs energy consumption. Since NVM can provide TB-scale capacity and the integrity trees in the large NVM are much high \cite{14}, it is important to decouple the latency of updating SIT root from the number of hash circuits.

Existing schemes overlook the system performance slowdown incurred by the root update latency of integrity tree. In secure NVM systems \cite{4,33,36}, the writes to user data are considered to be completed if the write requests arrive at the write queue, which is persistent domain due to the support of Intel Asynchronous DRAM Refresh (ADR) technique \cite{1}. Propagating the modifications to update the integrity tree root is executed by the backend threads. Therefore, the update latency doesn’t impact the system performance. However, due to the recoverability of the NVM systems, the root of the integrity tree must be updated in time before system failures to ensure the data integrity verification after system reboots. The write requests of user data are actually completed when the modifications propagate to the integrity tree root. The operation of updating root exists on the critical path and significantly reduces the system performance \cite{18}.

Like the counter and user data described in SCA \cite{17}, there exist crash inconsistency problems between the root and leaf nodes. System failures may occur at any time. If the failures occur after persisting leaf nodes but before updating the root, the old root can’t verify the new leaf nodes after system failures, which possibly causes the misreport of attacks. Similarly, if the failures occur after updating root but before persisting leaf nodes, the attacks are also misreported after system reboots. We call it root crash inconsistency problem, i.e., after system failures, the root needs to be consistent with the leaf nodes.

After system failures, we use the root as the trusted base to verify other data. However, since the SIT can’t be recovered from the leaf nodes, the root of SIT can’t play its role after system reboots. The generation of one SIT node needs its parent node as input. Due to the loss of the intermediate nodes during failures, the nodes in the SIT can’t be reconstructed from leaf nodes \cite{36}. After reboots, the system doesn’t know whether the leaf nodes are attacked or not via verifying the SIT root. This drawback limits the usage of SIT. In existing SIT-based NVM systems \cite{2,36}, one MT constructed in cache or NVM is added outside the SIT, and the root of the MT is used as the trusted base to verify the integrity of data. Some other integrity-tree works \cite{4,9} can’t be leveraged by the SIT since SIT fails to be reconstructed from leaf nodes.

We observe that in SIT, increasing the child counter causes the increment of the parent counter, and thus the parent counter is the sum of the corresponding child counters. Moreover, the counter in root is the sum of all corresponding leaf counters. Based on the observation, to reduce the long latency of updating root, we propose the ShortCut Update scheme (SCUE) to correctly update the root of SIT with low overheads, and leverage a counter-summing recovery approach to reconstructing the SIT from the leaf nodes. When propagating the modifications of leaf nodes, we directly update the root of SIT by overlooking the intermediate nodes, called SCUE scheme. In SCUE, the leaf nodes and root are guaranteed to be consistent, excluding the intermediate nodes. After system reboots, we reconstruct the whole SIT by the same observation that the parent counter is the sum of the corresponding child counters. The reconstructed root detects the attacks on the leaf nodes by comparing with the stored one.

SCUE decreases the latency of updating root, and however, the failures also occur between persisting leaf nodes and updating the root. To ensure the root crash consistency, we observe that the root of SIT can be predicted. Thus we pre-update the root in SCUE to prepare the root in the ADR region.

To evaluate the performance of our proposed scheme, we use Gem5 \cite{5} with NVMain \cite{20} to implement SCUE. We evaluate 5 persistent workloads that have been widely used in the community \cite{7,15,17,21,37} and 8 macro-benchmarks from the SPEC2006 \cite{13}. Our experimental results show that SCUE significantly reduces the write latency by 1.81x on average and provides 1.59x system speed up (up to 2.28x) compared with existing tree update schemes.

In summary, this paper makes the following contributions:

- **Shortcut update scheme for reducing write latency.** We propose a new update scheme to directly update the root of the integrity tree without propagating the modifications on the intermediate tree nodes.

- **Ensuring the root crash consistency.** We analyze the root crash inconsistency problem and pre-update the root in the ADR to address the problem.

- **Reconstructing the SIT from the leaf nodes.** We use counter-summing approach to recovering the SIT from the consistent leaf nodes without the aid of the MT. This work compensates for the shortcomings of SIT compared with the BMT.

- **Extensive experiments.** We have implemented and evaluated SCUE via micro- and macro-benchmarks. The experimental results show that our proposed scheme delivers high performance while ensuring the system integrity.
A. Threat Model

Existing works \[3, 4, 17, 22, 32, 34, 36\] assume that only the on-chip domain in the computer system is safe, including the processor, cache and memory controller, which we follow in our threat model. The NVM can be attacked to reveal the data, such as stolen DIMM and bus snooping attacks. The data confidentiality attacks can be defended by encryption \[\{\}\]. The memory tampering attacks modify the data in NVM to compromise the data integrity, including data replay attacks \[26\]. These integrity attacks can be detected by the integrity trees. Other types of attacks are beyond the scope of this paper. In this paper, we mainly focus on the integrity trees to improve the performance of SIT.

B. Counter Mode Encryption

The counter mode encryption (CME) has been widely used in state-of-the-art security systems \[3, 27, 35, 38\]. In general, to encrypt the data, direct AES encryption is used, which however places the decryption latency on the read critical path. Moreover, due to the unchanged secret key, the AES can be broken via the dictionary attacks. To deliver high performance and improve the security of the systems, the counter mode encryption is used as shown in Fig. 1. CME uses the counter and line address to generate the one-time-padding (OTP). When writing data, the ciphertext is generated by XORing the plaintext and OTP. When reading data, since the counter blocks are cached in the memory controller, systems generate the OTP and read the encrypted data in parallel. The encrypted data is decrypted by XORing the ciphertext and OTP. Therefore, the decryption latency is masked by the data read latency.

For security considerations, the OTP should never be reused. CME uses the line address as OTP generation input to ensure that different data lines have different OTPs. When one modified data is persisted into NVM, the corresponding minor counter increases by 1. For the same data, the OTP is not reused in each write since the counters are different. One counter block contains one 64-bit major counter and 64 7-bit minor counters. When the minor counter overflows, the major counter increases by one, all minor counters in the counter block are reset to 0, and 64 corresponding user data blocks need to be re-encrypted.

C. Integrity Verification

Data integrity verification is important for system security. An attacker tampers with the user data without authorization, which becomes even worse once the tampered data are used by CPU. Normally, systems use Keyed-Hash Message Authentication Codes (HMACs) to verify the integrity of data. HMACs are generated by hashing the data, address and secret keys. When reading data, systems verify the data integrity via comparing the stored and recomputed HMACs. If the two HMACs are different, systems detect the unauthorized modifications. Due to the lack of secret keys, the attackers fail to construct the matched HMACs of the modified data and can’t pass the integrity checking.

However, HMACs can’t detect the data replay attacks that break the data integrity. Attackers record the old data and HMAC, and use the old tuple to replace the new data and HMAC. By only using HMAC, systems can’t detect replay attacks, since the old HMAC matches the old data. To defend against the replay attacks, an integrity tree is used, including the Merkle Tree (MT), Bonsai Merkle Tree (BMT) and SGX Integrity Tree (SIT) \[8, 11, 22, 29\], to protect data via the on-chip root that can’t be tampered by attackers.

D. Merkle Tree

Merkle trees (MT) are used to protect the data integrity by constructing the whole tree from the user data which are leaf nodes in the MT. In an 8-ary MT, 8 data are hashed to generate the upper-level node that consists of 8 HMACs, called parent node of the hashed data. The upper-level nodes are also hashed to generate the higher-level nodes, and finally, the root is generated by iteratively hashing the leaf nodes. As shown in Fig. 3, the leaf nodes are in Level 0, i.e., leaf level, and they are iteratively hashed to construct the Level 1 and higher-level nodes. Systems store the root on the chip so that the root can’t be tampered by attackers in our threat model.

Modifying one user data causes the change of its parent node in the MT, and the modification will propagate to the root by iteratively modifying the intermediate nodes. If attackers
The high overhead of updating root in an

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integrity tree. To correctly verify the leaf nodes after system failures, the modifications of leaf nodes need to be propagated into the root before system failures. However, propagating the modifications incurs long latency on the write critical path. To update the root, all nodes in the branch are read from NVM (if they are not in cache), which consumes some latency, called read latency. Since updating one node uses its child nodes as inputs, updating the root consumes a long latency to serially hash all nodes in the branch, called hash latency. Hashing the inputs to generate one HMAC needs 80–160 cycles [10], [18], [25]. To propagate the modifications from leaf nodes to root, we serially hash tens of HMACs, which incurs a long latency.

2. The inconsistency between root and leaf nodes. Since the write queue in the memory controller is supported by ADR, the write queue is a persistent domain. Updating the on-chip root and persisting the leaf nodes into the write queue are two atomic operations. As shown in Fig. 5 if a system failure occurs after updating root but before persisting leaf node, the new root can’t correctly verify the old leaf nodes. On the other hand, if a system failure occurs after persisting leaf node but before updating root, the new leaf node also can’t match with the un-updated root, thus causing root crash inconsistency problem. When updating root and persisting a leaf node are executed in an atomic manner, the leaf nodes can be verified by the root after the system failures. After verifying the leaf nodes, i.e., counter blocks in BMT and SIT, the user data can be further verified via the HMAC.

SIT is a parallelizable integrity tree to significantly reduce the propagating latency. The HMACs in SIT nodes are computed in parallel once the counters are ready. However, parallel generating the HMACs in nodes requires multiple hash circuits, and consumes computing resources. Security schemes, including encryption and integrity verification, are executed in the memory controller with limited resources. Moreover, the capacity of NVM can be up to 6TB [19], which means tens of nodes exist in a branch. To generate HMACs in all nodes in a branch, tens of hash circuits in the memory controller become necessary, while incurring the consumption of on-chip space and energy. To decouple the root update latency from the number of hash circuits, it is important to consume low computing resources and reduce the latency of updating root in SIT.

Moreover, even if the root in SIT is correctly updated in time, the root can’t verify the data integrity after system reboots. The root fails to be reconstructed from the leaf nodes [36] to be compared with the stored one to detect the leaf nodes. Without the correct counters in the target node and its parent node, the target node can’t be reconstructed. To make the SIT root play its role after system reboots, it is important to recover the SIT from persistent leaf nodes.

As shown in Fig. 5 the lazy and eager schemes in SIT exhibit an approximate number of metadata cache misses (the experimental configurations are shown in Section IV). However, since the lazy scheme doesn’t update the root [36], we focus on the eager scheme to reduce the root update latency.

In this paper, in order to improve the system performance, we propose SCUE, a low-overhead shortcut update scheme, to immediately update the root, ensure the root crash consistency and provide the ability to reconstruct the SIT from leaf nodes for verification after system reboots.

III. System Design and Implementations

A. Overview

In the secure NVM systems, the encryption and integrity verification are performed in the memory controller and transparent to applications. As shown in Fig. 7 a processor sends a write request to the memory controller. The written data is encrypted by the CME and updates the SIT. The data then enters the write queue supported by ADR. To ensure the consistency of data, counter and tree node, existing schemes offer different approaches to flushing the counters
Fig. 8. The eager and SCUE schemes in SIT. (a) Eager update scheme modifies the intermediate nodes. (b) SCUE overlooks the intermediate nodes, and tree nodes into the write queue [17], [33], [36], which unfortunately fail to offer efficient update upon the root in SIT. To support the verification after system reboots, the systems also need to ensure the consistency between the root and the leaf nodes.

We propose the SCUE to significantly reduce the latency of updating tree root and ensure the root crash consistency. As shown in Fig. 7 modifying the counter blocks in CME causes the changes in the entire SIT, and we overlook the intermediate nodes to directly update the root of SIT via SCUE since the updates in the intermediate tree nodes are unnecessary. The tags are appended on the write queue and used to store the updated roots. The counter crash consistency [17], [34], [37] is beyond the scope of this paper, and we use Osiris [34] to ensure the counter blocks are up-to-date and consistent. The encrypted user data contain the updates of the counter blocks as the leaf nodes in the SIT. Due to the use of ADR, the encrypted data are flushed into the NVM while the corresponding roots are flushed into the non-volatile register on chip to ensure the root crash consistency.

B. Update the Root in a Shortcut Manner

To reduce the latency of updating the root of SIT eager scheme and improve system performance, we propose a low-overhead shortcut update (SCUE) scheme. The basic idea of SCUE is to remove the computation of HMACs and reads of intermediate tree nodes from the write critical path.

1) Lazy computing in SCUE: We observed that in SIT nodes, the HMACs are used to verify the node itself, and the counters are used to verify the child nodes. When reading data from NVM into cache, the counters in the cached tree nodes and HMACs in the read data are used to verify the integrity of the read data. Since the on-chip data are invulnerable to attackers in our threat model, the integrity of the cached tree nodes needn’t be verified, and the HMACs are not used. To verify the integrity of the data next time they are read, the counters in cached tree nodes need to increase when the data are persisted, but updating HMACs is unnecessary. Only the HMACs in the persisted data need to be updated to defend against attacks that occur in NVM.

We propose lazy computing in SCUE to remove the long hash latency in the propagation path from leaf nodes to root. When one user data is persisted, the HMAC in the user data is computed to facilitate the verification of the following read. The counters in the ancestor tree nodes increase, but their HMACs are only computed when the nodes are flushed into NVM via the cache replacement policy.

2) Remove the reads of tree nodes: Propagating the modifications from leaf nodes to root needs to read the ancestor nodes with long read latency, if the ancestor nodes are not in cache. In SIT, the root consists of eight counters, and the counter values are related to the leaf nodes. As shown in Fig. 8(a), in the eager update scheme, when one modified leaf node is persisted, its ancestor nodes are updated. Specifically, all corresponding counters increase by one, including the counter in root. In summary, if one modified leaf node is persisted into NVM, the corresponding counter in root increases by one. To improve the system performance, as shown in Fig. 8(b), we propose the SCUE to directly increase the counter in root without reading the intermediate tree nodes.

However, the root update by overlooking intermediate nodes needs to carefully handle the system execution. When the intermediate nodes are read, they should be iteratively verified by the cached tree nodes and root. However, the updated root can’t match the un-updated intermediate nodes since we overlook the intermediate nodes to update the root. Therefore, the attacks are misreported even if the intermediate nodes are un-attacked. To verify the data integrity on running time, we read and update the intermediate tree nodes via lazy computing in the backend threads without computing HMACs after the root is updated. In SCUE, after updating the root counters, the write operations are completed. The latencies of reading the intermediate tree nodes are removed from the write critical path.

Moreover, when the cached tree nodes are flushed into NVM due to cache replacement policy, their parent nodes need to be read to compute the HMACs of the persisted nodes, which possibly incurs iterative reads of ancestor nodes to execute the integrity verification. To reduce these reads, SCUE proposes the dummy counter as shown in Fig. 9. A dummy counter is generated by summing all counters in the tree node being flushed. In the eager scheme, when any counter in one node increases by one, the corresponding counter in the parent node (called parent counter) also increases by one. Therefore, the dummy counter becomes the parent counter of the persisted node to compute the HAMC. Since the cached node is safe in our threat model, the generated dummy counter is the same as the parent counter. The iterative reads of the ancestor nodes are hence removed.

3) Benefits of the proposed optimizations: Persisting user data causes the modifications of the counter blocks, which are the leaf nodes of the SIT. SCUE propagates the modifications by directly updating the root without reading and updating intermediate nodes. The reads and updates of the intermediate tree nodes are removed from the write critical path. Shortcuts are generated for the root counter by summing all root counter in the tree instead of reading the intermediate tree nodes.
nodes are executed via lazy computing by the backend threads. When the cached tree nodes are flushed into NVM, the dummy counters are generated to compute the HMACs if the parent nodes of the flushed nodes are not in cache. Even compared with lazy scheme which doesn’t update the root, SCUE also delivers better performance, since lazy scheme needs to compute the HMACs in the written data and parent node and iteratively read the ancestor nodes when one data is persisted.

In summary, for writing data, SCUE removes all reads of integrity tree nodes from the write critical path and only needs to generate one HMAC in the persisted data.

C. Reconstruct the SIT

SIT fails to be reconstructed from the leaf nodes [2], [9], [36] since reconstructing one SIT node requires its parent node as input. We leverage a counter-summing approach to reconstructing the SIT from leaf nodes up and analyze the security of the proposed scheme.

1) Counter-summing approach to reconstructing tree: In SIT, even if the root is timely updated via SCUE, due to failing to reconstruct the integrity tree from the leaf nodes, the up-to-date root in SIT fails to verify the leaf nodes after system reboots. In existing integrity tree schemes, only the eager updated BMT and MT, which can be reconstructed from leaves and contain up-to-date root, offer integrity verification after system failures with a long root update latency during running time. To provide efficient integrity verification for SCUE, we use the counter-summing recovery approach to reconstructing the SIT.

In SIT, each node contains eight counters and has eight child nodes. We observed that when one child node is modified, i.e., any counter increases by one, the corresponding counters in the parent and ancestor nodes also increases by one. As shown in Fig. 9, the dummy counter is generated according to the observation. After the system reboots, we reconstruct the tree from the bottom up via the dummy counter.

We first reconstruct the Level-1 nodes from the consistent leaf nodes. Reconstructing one SIT node requires correct counters and HMAC in the node. For reconstructing counters, we generate the dummy counters from the leaf nodes, and each $8K$th to $8K + 7$th ($K$ is a natural number) dummy counters are combined to form one Level-1 node. The dummy counters become counters in the reconstructed nodes. We then use the HMACs in the persistent leaf nodes to verify the correctness of the reconstructed counters in Level-1 nodes. The HMAC is recomputed by hashing the reconstructed counter in the Level-1 node and all counters in the corresponding leaf node. The mismatches of recomputed HMACs and stored HMACs in the leaf nodes indicate attacks occurring during system recovery. All counters in the Level-1 nodes can be recovered via summing the corresponding counters in the leaf nodes.

For recomputing HMACs, the counters in Level-2 nodes need to be reconstructed by generating the dummy counters from Level-1 nodes. The HMACs in the Level-1 nodes are recomputed by hashing the corresponding counters in the Level-2 nodes and all counters in the Level-1 nodes. Therefore, the counters and HMACs in the Level-1 nodes are reconstructed. We use the same way to reconstruct the whole tree from the bottom up. Finally, the dummy root counters are generated. If the dummy root counters are different from the stored root counters, the SIT reconstruction fails, and attacks occur during recovery. Otherwise, the SIT is successfully reconstructed.

2) Security analysis: We analyze the security of the proposed counter-summing recovery approach of SIT. We focus on the root and leaf nodes since the intermediate tree nodes are lost when failures occur, which need to be reconstructed from the persistent leaf nodes. Moreover, since the root is on chip, attackers can’t tamper with the root. When recovering the SIT, only the leaf nodes in NVM are attacked.

We use the HMACs in the leaf nodes and the on-chip root to detect the attacks that occur during system recovery. All attacks in the leaf nodes can be divided into two types: roll-forward and roll-back attacks. Specifically, the roll-forward attacks tamper with the counter value in the leaf nodes to a larger value. On the contrary, the roll-back attacks tamper with the counter value in the leaf nodes to a smaller value. The replay attack is a typical roll-back attack that replaces the counters and HMACs using the old tuple.

As shown in Table I, the roll-forward attacks are detected by the HMACs in the leaf nodes. The parent counters are reconstructed from the leaf nodes, and the HMACs of the leaf nodes are recomputed. Without the secret key, attackers can’t calculate the correct HMACs using new counters. The mismatches between the recomputed HMACs and stored HMACs in leaf nodes indicate the attacks.

The normal roll-back attacks are also detected by HMAC since the HMAC doesn’t match the tampered counters. We discuss how to detect the replay attacks, which pass the verification of HMAC since the old HMAC matches the old counters. Since increasing counters in leaf nodes causes the increment of counters in root, one root counter is equal to the sum of all counters in the corresponding leaf nodes. For example, the value of first counter in the root is the sum of counters’ values in the leading one eighth of the nodes in the leaf level since the root contains eight counters. Rolling back counters in leaf nodes causes the reconstructed root to mismatch the stored root. Therefore, the attacks are detected.

Moreover, attackers may roll back and roll forward some counters at the same time to deceive the root, but rolling forward counters is detected by the HMACs as shown in Table I. The detection process is similar to that of BMT, i.e., the attacks are detected after reconstructing the whole integrity tree and comparing the reconstructed root with the stored one.

The counter-summing recovery approach allows to recon-
struct the SIT from consistent leaf nodes. Therefore, the SIT root can be used to verify data after system failures. The related tree works [4], [9] for better system performance can be used by SIT.

D. Ensure Root Crash Consistency

Like SCA [17], we slightly modify the write queue to ensure the crash consistency between root and leaf nodes. However, the intuitive design fails to be used in a modern multi-thread platform. We pre-update the root before leaf nodes are modified to address the problem of root crash inconsistency.

1) Intuitive hardware design: SCUE updates the root of SIT with negligible latency. However, persisting the leaf nodes and updating the root are still two atomic operations. When system failures occur between these two operations, the root is inconsistent with the leaf nodes and can’t be used to verify the leaf nodes after system reboots. To ensure the root crash consistency, we slightly modify the hardware architecture like the SCA [17]. As shown in Fig. 10(a), the write queue is supported by ADR. Once power off, the data in the write queue can be flushed into NVM with the support of the backup battery. To persist the root, we extend the write queue in the memory controller, i.e., each entry in the write queue has a tag, in which we store the corresponding root. Since we use Osiris [34] to ensure the counter crash consistency, the user data contain the updates of the counter blocks. Persisting user data means that the counter blocks are persisted, which are the leaf nodes in the SIT. When the user data enter the write queue (1), we fill the tags using the roots (2), which are updated by increasing the corresponding counter via SCUE. When the tags become ready (3), the user data in the write queue are allowed to flush into NVM, and the roots in tags are also flushed into the on-chip root register.

We analyze the root crash consistency in the intuitive design. If the system failures occur before the tags are prepared, the new user data are not allowed to be flushed into NVM. The old root can match the old and consistent leaf nodes in NVM when the leaf nodes are recovered from user data via Osiris. If the system failures occur after the tags are prepared, the user data in the write queue are flushed into NVM due to the ADR support, and the updated root in the tag is also flushed into the on-chip root register. Thus both the root and leaf nodes become new states.

2) Pre-update approach: The intuitive hardware design is inspired by SCA [17] and can work well on the single-thread architectures. However, in the modern multi-thread architectures, the root fails to be correctly updated. When user data concurrently enter the write queue, multiple threads read the root and increase the corresponding counter value by one to fill the tags. The multiple tags are incorrectly updated to the same values since the same root is read and root counters increase by one by the threads.

To correctly update the roots in tags, we observe that the updates of root counters are predictable, i.e., the counters of roots in consecutive tags are incremented in most cases. Since one counter in root covers 1/8 memory space, persisting two data may cause the same counter in root modified, i.e., the two data share the same root counter. Assume one counter in root is n, persisting one user data changes the counter to \( n + 1 \) in the root. Following user data persistence also increases this counter to \( n + 2 \) if the user data shares the same root counter with the previous data. Based on this observation, we propose a Pre-update approach to filling the tags in advance. As shown in Fig. 10(b), the background thread writes Root to the 1st tag and Root + 1 to the 2nd tag. The remaining tags are also prepared by increasing the value in the previous tag(8). The write queue concurrently receives user data(9) as filling the tags.

When pre-updating the tags in the write queue, we need to determine which counter in root needs to increase by one. The root contains eight counters, and the memory is equally divided into eight parts. According to the location of the user data, persisting the data increases one corresponding counter in the root. If the user data entering the write queue makes another counter, which is not the counter prepared in advance, in the root modified, the prepared tags need to be cleared and a new root fills the tag. The write queue is blocked until the new tags are prepared for the root crash consistency.

In general, applications have high spatial locality and one counter in root covers 1/8 memory space. It is a high probability that the following persisted user data share the same root counter as the previous persisted user data. Thus we wait for the root counter to be modified and increase the same root counter in the consecutive tags in advance. If persisting one data needs to increase another root counter in the tag, we re-update this tag and remaining tags.

The tags in the write queue are used to store the counterparts of the 64-byte root. An entry in the write queue is also 64 bytes. Thus the write queue needs to extend 1x space to store the tags, which consumes the expensive ADR space. However, only one counter in root increases when one user data enters the write queue. To reduce the space overhead, we store the modified 64-bit counter in the tag, instead of the full root.

When system failures occur, due to the support of ADR, the data in the write queue are flushed into NVM. If the root counters in tags have corresponding data in the queue, the root counters are flushed into the on-chip non-volatile register to
update the root. As shown in Fig. 10(b), the blue root counters are flushed into the register since their corresponding user data are flushed into NVM, while the red root counters can’t be flushed. Flushing the root counters is simple. Due to the first-in-first-out feature of the write queue, the old root counter is first flushed. The latest root counter finally covers the old root counter in the register, so that the root becomes the latest to match the leaf nodes that are recovered from the persistent user data.

Persisting tree nodes doesn’t impact the root in SCUE. However, when entering the write queue, the tree nodes have the corresponding tags. After system failures, the root is incorrectly updated via ADR. Data writes contain security metadata and user data writes. Fig. 11 shows the breakdown of data writes. On average, the amount of metadata writes is 13.6% of all data writes. For the 64-entry write queue, we add another 10 entries without tags to handle metadata writes like SCA [17]. Persisting tree nodes thus doesn’t incorrectly increase counters in the root.

E. Comparisons of Integrity Tree Update Schemes

We compare existing schemes of updating integrity trees with our proposed SCUE. As shown in Table II, the eager BMT requires long latency to update the root. The eager SIT also needs to propagate the modifications, and however, the eager SIT uses multiple hash circuits to update the intermediate nodes in parallel with high computation overhead in the memory controller. Thus the latency of updating eager SIT root is shorter than that of eager BMT root. Our SCUE needs a negligible latency to update root, since the scheme overlooks the intermediate nodes and directly updates the root. The lazy BMT/SIT doesn’t update the tree roots. They can’t recover after failure due to the loss of the latest root. Moreover, the eager SIT can’t be reconstructed from leaf nodes due to the unique dependency between the counters in parent nodes and HMACs in the child nodes.

In existing works, we only reconstruct the eager BMT from the leaf nodes during recovery. However, the long root update latency and root crash inconsistency problems are not considered by existing integrity tree update schemes. Our proposed SCUE is able to immediately update the root of SIT, recover the SIT from the leaf nodes and ensure the root crash consistency.

IV. PERFORMANCE EVALUATION

A. Evaluation Methodology

To evaluate the performance of SCUE, we model the system in the Gem5 [5] and NVMain [20]. NVMain is a cycle-accurate main memory simulator for emerging NVM technologies. Main parameters are shown in Table III. The metadata cache in the memory controller is 256KB, storing counter blocks and integrity tree nodes. We model the PCM technologies with 16GB capacity. The PCM latency is modeled like existing works [31], [37]. In general, the hash latency to generate the HMAC is 80 cycles [10]. In our sensitive study, we vary the hash latencies (from 80 to 160 cycles [18], [25]) to analyze the impacts on performance. We use 8 representative applications from CPU SPEC2006 benchmarks [13], simulating 5 billion instructions for each application, and 5 persistent workloads to evaluate the systems. The persistent workloads, i.e., array, btree, hash, queue and rbtree, are widely used in existing works of persistent memory [7], [15]–[17], [21], [37].

To comprehensively examine the performance of our proposed SCUE, we evaluate and compare the following schemes.

- **Eager scheme (Eager).** An eager update scheme propagates the modifications from the modified leaf nodes to the root with a large overhead. The BMT-eager scheme verifies the leaf nodes after system failures since the integrity tree can be reconstructed from the persistent leaf nodes.
- **Lazy scheme (Lazy).** The lazy scheme updates the parent nodes of the written data in the integrity tree but doesn’t propagate the modifications to the root. It also needs to

## TABLE II

| Schemes          | Latency of updating root | Recoverability | Root crash consistency |
|------------------|--------------------------|----------------|------------------------|
| Lazy BMT         | /                        | N              | N                      |
| Eager BMT        | high                     | Y              | Y                      |
| Lazy SIT         | /                        | N              | N                      |
| Eager SIT        | normal                   | N              | Y                      |

## TABLE III

| The Configurations of the Evaluated NVM System. |
|-----------------------------------------------|
| Processor                                      |
| CPU                                           |
| 8 cores, X86-64 processor, 2 GHz               |
| Private L1 cache                              |
| 64KB, 2-way, LRU, 64B Block                    |
| Private L2 cache                              |
| 512KB, 8-way, LRU, 64B Block                   |
| Shared L3 cache                               |
| 4MB, 8-way, LRU, 64B Block                     |
| DDR-based PCM Main Memory                      |
| Capacity                                      |
| 16GB                                          |
| PCM latency model                             |
| 8KC2(13) CL(W1/TAHW/THA) = 48/15/10/7.5/300 ns |
| Write queue                                   |
| 64 entries with 64-bit tags for user data, 10 entries without tags for security metadata |
| Secure Parameters                             |
| Security metadata cache                       |
| 256KB, 3-way, 64B Block, in MC                 |
| SIT                                           |
| 9 levels, 8-ary, 64B Block                     |
| Hash latency                                  |
| 80 cycles [10]                                |

Fig. 11. The breakdown of data writes in SCUE.
read the ancestor nodes to verify the parent node when writing data. The lazy scheme doesn’t offer integrity verification after system failures and reboots.

- Our proposed lazy computing (LC). LC increases the counters of the tree nodes in the propagation path. Only the HMACs in the persisted data are computed.
- Shortcut update scheme (SCUE). SCUE directly updates the root without propagating the modifications from leaf nodes to root. In SCUE, the HMACs are calculated via LC, and the intermediate tree nodes are not read on the write critical path.

B. Results and Analysis

Propagating the modifications from leaf nodes to the root incurs a long latency on the write critical path. We evaluate the write latency and execution time on different schemes.

Fig. 12 shows the write latencies on different schemes. Due to performing multiple hash calculations before persisting data, on average, the write latency in the Eager scheme is 1.81x than that in SCUE. Moreover, the Lazy scheme needs to read the parent and ancestor nodes of the evicted user data and metadata, and calculate the HMACs in the evicted data and parent nodes on the write critical path. Our SCUE needn’t read any nodes and only compute the HMAC once when writing data. Therefore, SCUE has a lower write latency than the Lazy scheme. On average, the write latency in Lazy scheme is 1.21x than that in SCUE.

We also compare LC with the SCUE. SCUE contains the LC approach but removes the data reads of the ancestor nodes. Compared with the LC approach, the performance improvement of SCUE is related with the number of metadata reads from NVM when writing data. Since many metadata are cached during the data read process, Fig. 13 shows that the metadata cache hit ratio is high during the write process. Many ancestor nodes already exist in cache and needn’t be read from NVM. Therefore, SCUE shows a light improvement (5% on average) on write latency than the LC approach. However, for the workloads with low metadata cache hit ratios, such as mcf and cactusADM, SCUE shows much lower write latency than the LC approach when using the high hit ratio workloads, such as lbm, btree and queue.

As shown in Fig. 14, SCUE shows a lower execution time than the Eager and Lazy schemes. Specifically, the Eager scheme leads to a 1.59x slowdown than SCUE. On the write-intensive workloads, such as mcf, the slowdown of the Eager scheme is up to 2.28x. SCUE delivers a higher performance than the Lazy scheme in terms of execution time. The average execution time in the Lazy scheme is 1.14x than that in SCUE, while SCUE is able to verify the integrity after system reboots and the Lazy scheme fails. Moreover, SCUE achieves less execution time than LC as shown in Fig. 14. Like the write latency in Fig. 12 compared with LC, SCUE shows higher performance improvement when using lower hit ratio workloads.

C. The Sensitivity to the Hash Latency

In our simulated configuration, the hash latency to generate the HMACs is 80 cycles. However, the hash latency can be
higher in existing works \cite{18, 25}, i.e., 160 cycles. We adjust the hash latency from 80 cycles to 160 cycles to evaluate the performance of SCUE.

As shown in Fig. 15, doubling the hash latency incurs up to 1.19x write latency in SCUE. On average, once the hash latency becomes 160 cycles, the write latency is 1.10x than that of 80-cycle hash latency configuration. Fig. 16 shows the execution time when adjusting the hash latency. The execution time increases by 1.05x when the hash latency is 160 cycles. Since we only calculate the HMAC once when writing data, doubling the hash latency results in the slight decrease in the performance of SCUE. This result motivates us to use more secure hash algorithms with higher computation latency to protect systems \cite{12} while providing high performance.

D. Recovery Scheme

After system failures, a system needs to recover the integrity tree for the following verification. We use Osiris \cite{34} to recover the counter blocks. For integrity tree nodes, existing works \cite{4, 36} offer different approaches to recovering the BMT and SIT with different overheads, since SIT can’t be reconstructed from the leaf nodes. In our SCUE, since the SIT is reconstructed from the leaf nodes via our proposed counter-summing recovery approach, all existing recovery schemes, no matter whether they are designed for BMT or SIT, can be used in the shortcut updated SIT. For better recovery performance, we use the AGIT in the Anubis \cite{36}, which is designed for BMT, to recover the shortcut updated SIT. In fact, any recovery schemes designed for BMT and SIT can be used.

V. RELATED WORK

Security metadata recovery. Security metadata include counter blocks and integrity tree nodes. For improving performance, security metadata are cached in a volatile on-chip buffer in the memory controller. After system failures, some updates of security metadata are lost due to not being persisted into NVM in time. To recover the counter blocks, Osiris \cite{34} relaxes the persistence of counter blocks, and retrieves the counters from the stale state in NVM. Supermem \cite{37} uses write-through scheme to ensure the consistency of counter blocks. When the counter blocks are modified, they are directly flushed into NVM. SCA \cite{17} consistently persists the counter and encrypted data via the support of ADR. To recover the BMT, Triad-NVM \cite{4} persists low-level tree nodes with user data. After failures, the systems can reconstruct the BMT from the persistent low-level nodes. Anubis \cite{36} records the address and content of the modified cached metadata in the shadow table in NVM. According to the shadow table, Anubis has the ability to recover both BMT and SIT. Phoenix \cite{2} observed that Anubis needs 2x writes to recover SIT. To reduce the write overhead of recovering SIT, Phoenix relaxes the persistences of counter blocks via Osiris, and recovers the intermediate tree nodes via Anubis.

Security metadata organization. The security metadata are organized in multiple ways to improve the performance of accessing metadata. To reduce the access latency and space overhead of integrity trees, existing schemes propose multiple variants of SIT. VAULT \cite{29} reduces the height and space overhead of SIT by storing more than 8 counters in one node, e.g., 64 counters in the leaf node, 32 counters in the Level-1 node and 16 counters in Level-2 and upper-level nodes. Based on VAULT, Morphable Counters \cite{23} observed that when one counter overflows, either less than a quarter of counters or all the counters are used. The Morphable Counters scheme provides a scalable solution to store 128 counters in one node and further reduces the height of the tree. Synergy \cite{24} places the MAC inside the ECC chip in a 9-chip ECC-DIMMs and demonstrates that MAC can be used to detect not only data tamper but also memory errors. ITESP \cite{28} uses small counters to save space in the tree node. The ECCs of the child nodes are XORed, and the XORed ECC is embedded in the parent node in ITESP.

The overheads of updating the integrity tree. Updating the integrity tree incurs large latency and consumes computation overheads. To reduce the overhead of integrity verification, Janus \cite{18} executes the integrity tree updates with backend operations (e.g., encryption and deduplication) in parallel. Janus also pre-executes the tree updates before the write requests arriving at the memory controller. Freij et al. \cite{9} observed that updating the BMT with correct order needs a large overhead. They propose the pipelining BMT update scheme to reduce the latency of updating BMT.

Unlike existing schemes, our SCUE directly updates the root to exhibit the changes of leaf nodes by looking over updating the intermediate tree nodes. Therefore, SCUE delivers high performance on NVM systems while ensuring the integrity.

VI. CONCLUSION

In order to correctly update the root of the integrity tree with low overheads, this paper proposes the low-latency and shortcut updated scheme SCUE. The idea behind SCUE is that only the updates in persistent leaf nodes and on-chip root are necessary. Ensuring the consistency between the root and the leaf nodes causes most overhead to persist the security metadata. Since the updates in cached intermediate tree nodes are not used, it is unnecessary to update the root in a step-by-step manner via modifying the intermediate tree nodes. We directly update the root in the SIT to significantly reduce the update overheads. To consistently update the tree root, we...
pre-update the root in the ADR. A counter-summing recovery approach is used to reconstruct the SIT from the consistent leaf nodes after system reboots. Compared with the eager update scheme, the SCUE shows 1.59x performance improvements in terms of system execution time while offering integrity verification after system failures and reboots.

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