CHECKMATE: BREAKING THE MEMORY WALL WITH OPTIMAL TENSOR REMATERIALIZATION

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ABSTRACT

Modern neural networks are increasingly bottlenecked by the limited capacity of on-device GPU memory. Prior work explores dropping activations as a strategy to scale to larger neural networks under memory constraints. However, these heuristics assume uniform per-layer costs and are limited to simple architectures with linear graphs, limiting their usability. In this paper, we formalize the problem of trading-off DNN training time and memory requirements as the tensor rematerialization optimization problem, a generalization of prior checkpointing strategies. We introduce Checkmate, a system that solves for optimal schedules in reasonable times (under an hour) using off-the-shelf MILP solvers, then uses these schedules to accelerate millions of training iterations. Our method scales to complex, realistic architectures and is hardware-aware through the use of accelerator-specific, profile-based cost models. In addition to reducing training cost, Checkmate enables real-world networks to be trained with up to 5.1× larger input sizes.

1 INTRODUCTION

Deep learning is rapidly pushing the limits of memory capacity on neural network accelerators as researchers train neural networks on high-resolution images [15, 32, 55], 3D point-clouds [10, 59], and long Natural Language Processing (NLP) sequence data [11, 14, 56]. In these applications, GPU memory usage is dominated by the intermediate activation tensors (see Figure 1) needed for backpropagation.

The limited availability of high bandwidth on-device memory creates a memory wall that stifles exploration of novel architectures. Authors of state-of-the-art models cite memory as a limiting factor in image classification [20, 25, 34], semantic segmentation [8, 45], and long Natural Language Processing (NLP) [11, 13, 36].

Given there is insufficient RAM to cache all activation tensors for backpropagation, some select tensors can be discarded during forward evaluation. When a discarded tensor is necessary as a dependency for gradient calculation, the tensor can be rematerialized. As illustrated in Figure 2, rematerializing a node allows a large DNN to fit within memory at the expense of additional computation.

Chen et al. [9] and Griewank and Walther [22] present heuristics for rematerialization, referring to the problem as checkpointing. However, their approaches cannot be generally applied to nonlinear DNN structures such as residual connections. Furthermore, they force a very strong assumption that the graph has uniform compute across all nodes.

Prior work also assumes that gradients may never be rematerialized. These assumptions limit the efficiency and generality of prior approaches.

Our work formalizes tensor rematerialization as a constrained optimization problem. Using off-the-shelf numerical solvers, we are able to discover optimal rematerialization strategies for arbitrary deep neural networks in Tensorflow with non-uniform computation and memory costs. We demonstrate that optimal rematerialization allows larger batch sizes and substantially reduced memory usage with minimal computational overhead across a range of image classification and semantic segmentation architectures. As a consequence, our approach allows researchers to easily explore larger models, at larger batch sizes, on more complex signals with minimal computation overhead.

In particular, the contributions of this work include:

- a formalization of the rematerialization problem as a mixed integer linear program with a substantially more flexible search space than prior work, in Section 4.5.
- an algorithm to translate a feasible solution into a concrete execution plan and a static training graph.
- an implementation of optimal tensor rematerialization in Tensorflow at runtime.
- Checkmate, a system that enables training models with up to 5.1× larger input sizes and with up to 2.6× larger batch sizes than prior art at minimal overhead.
2 Optimal Rematerialization

Tensor rematerialization enables training neural networks with activation memory requirements larger than the capacity of current hardware.

In Figure 2, we examine a three-layer neural network that exceeds device memory (OOMs) with the current practice of caching every dependency. We represent the corresponding gradient nodes in red. Our proposed policy discards the activations for node B at $t = 3$, thereby freeing memory. However, B’s gradient operation $\nabla B$ depends on the value of $B$. At $t = 5$, B is rematerialized in time for $\nabla B$.

Prior art assumes networks are linear graphs, or path graphs, where node $v_i$ solely depends on $v_{i-1}$ and edge set $E = \{(v_1, v_2), (v_2, v_3), \ldots, (v_{n-1}, v_n)\}$. For example, Chen et al. [9] propose a strategy where the graph is divided into $\sqrt{n}$ segments each with $\sqrt{n}$ nodes. During the forward pass, the strategy retains the activation of the endpoint of each segment. During backpropagation, each segment is recomputed from the activation of the endpoint of the previous segment. This results in an $O(\sqrt{n}\sqrt{n}) = O(n)$ rematerialization overhead. As Chen assumes networks are linear graphs, node B cannot be rematerialized independently.

Linear graph assumptions dramatically limit applicability of prior work to popular DNN architectures. For example, the popular ResNet50 [25] requires treating each residual block as a single node which leads to inefficient solutions. For other networks with larger skip connection (e.g., U-Net [47]), the vast majority of the graph is incompatible.

Prior work also makes similar assumptions about the cost model for DNN graphs, namely that all nodes require an equivalent number of operations to evaluate. In the VGG19 [49] architecture, the largest layer is seven orders of magnitude more expensive than the smallest layer. This leads to suboptimal solutions.

Our work makes few assumptions on neural network graphs. We explore a solution space that allows for (a) arbitrary graphs with several inputs and outputs for each node, (b) variable memory costs across layers and (c) variable computation costs for each layer (such as FLOPs or profiled runtimes). We constrain solutions to simply be correct (a node’s dependencies must be materialized before it can be evaluated) and within the RAM budget (at any point during execution, resident tensors must fit into RAM).

To find solutions to this generalized problem, we find solutions that minimize the amount of time it takes to perform a single training iteration, subject to the correctness and memory constraints outlined above. To efficiently solve this optimization problem, we project schedules into space and time. Modeling schedules this way allows us to cast the objective as a linear expression. This problem can then be solved using off-the-shelf mixed integer linear program solvers such as GLPK [19] or COIN-OR Branch-and-Cut [17]. An optimal solution to the linear program will be optimal for arbitrary graphs with variable memory and variable compute profiles, factors that are neglected by prior work.
3 RELATED WORK

We categorize the large body of related work into activation compression, rematerialization and checkpointing, reversible architectures, and distributed computation.

Activation compression In some DNN applications, it is possible to process compressed representations with minimal accuracy loss. Guéguen et al. [24] develop a DNN that classifies ImageNet images given discrete cosine transform codes from partially decoded JPEG images, accelerating network evaluation, and possibly requiring less memory. Jain et al. [29] observe that feature maps, or activations, dominate memory usage during training, and halve memory usage on average by reducing the precision of activations. Still, compression only reduces memory usage by a constant factor and reduces accuracy at higher compression rates. In contrast, deleting and recomputing values maintains the same accuracy at a range of memory budgets. Also, as our solver operates on arbitrary computation graphs, compression operations may be included.

Checkpointing and rematerialization Prior work has addressed checkpointing and rematerialization in linear graphs. In work from the differential equation community that inspired later work in reverse-mode automatic differentiation, Griewank and Walther [22] develop a procedure for checkpointing in idealized linear computation graphs with $O(\log n)$ memory usage, where $n$ denotes the number of computation nodes. Griewank proves that their proposed logarithmic checkpointing strategy is optimal with respect to linear graphs with unit cost and memory per node. Chen et al. [9] propose a heuristic for rematerialization in similarly idealized unit cost, unit memory usage linear graphs with $O(\sqrt{n})$ memory usage at an $O(n)$ computational overhead, intended for DNN training. However, the approach is far from optimal in practice as DNN layers vary significantly in memory usage and computational cost [53]. Chen et al. [9] also develop a greedy algorithm that checkpoints layers of a network in roughly memory equal segments, with a hyperparameter $b$ for the size of such segments. Still, neither procedure is cost aware nor deallocates checkpoints when possible. Gruslys et al. [23] develop a dynamic programming algorithm for checkpoint selection in unrolled recurrent neural network training, exploiting their linear forward graphs. To extend checkpointing to branching networks, Feng and Huang [16] provide a dynamic program to select checkpoints that partition a nonlinear computation graph, but ignore layer costs and memory usage. Siskind and Pearlmutter [50] develop a divide-and-conquer strategy in programs. Beaumont et al. [2] give a dynamic program for checkpoint selection in join networks where multiple linear graphs merge at the loss node.

Intermediate value recomputation is also common in register allocation. Compiler backends lower an intermediate representation of code to an architecture-specific executable binary. During lowering, an abstract static single assignment (SSA) graph of values and operations [12, 48] is concretized by mapping values to a finite number of registers. If insufficient registers are available for an SSA form computation graph, values are spilled to main memory by storing and later loading the value. Register allocation has been formulated as graph coloring problem [7], integer program [21, 38], and network flow [33].

As an optimization, register allocators can rematerialize, or recompute, constants and values with register-resident dependencies if the cost of doing so is less than the cost of a spill [3, 7, 46]. While similar to our setup, register rematerialization is limited to exceptional values that can be recomputed in a single instruction with dependencies already in registers. For example, memory offset computations can be cheaply recomputed, and loads of constants can be statically resolved. In contrast, Checkmate can recompute entire subgraphs of the program’s data-flow.

During the evaluation of a single kernel, GPUs spill per-thread registers to a thread-local region of global memory (i.e. local memory) [41, 42]. NN training executes DAGs of kernels and stores intermediate values in shared global memory. This produces a high range of value sizes, from 4 byte floats to gigabyte tensors, whereas CPU and GPU registers range from 1 to 64 bytes. Our problem of interkernel memory scheduling thus differs in scale from the classical problem of register allocation within a kernel or program. Rematerialization is more appropriate than copying values out of core as the cost of spilling values from global GPU memory to main memory (RAM) is substantial [29, 41], though possible [40].

Reversible Networks Gomez et al. [20] propose a reversible (approximately invertible) residual DNN architecture, where intermediate temporary values can be recomputed from values derived later in the standard forward computation. Reversibility allows forward pass activations to be recomputed during the backward pass rather than stored, similar to gradient checkpointing. Bulo et al. [5] replace only ReLU and batch normalization layers with invertible variants, reconstructing their inputs during the backward pass, reducing memory usage up to 50%. However, this approach has a limit to memory savings, and does not support a range of budgets. Reversibility is not yet widely used to save memory, but is a promising complementary approach.

Distributed computation An orthogonal approach to address the limited memory problem is distributed-memory computations and gradient accumulation. However, model parallelism requires access to additional expensive compute accelerators, fast networks, and non-trivial partitioning of model state to balance communication and computation [18, 31, 39]. Gradient accumulation enables larger
batch sizes by computing the gradients in sub-batches across a mini-batch. However, gradient accumulation often degrades performance as batch normalization performs poorly on small minibatch sizes [28, 57].

4 OPTIMAL REMATERIALIZATION WITH INTEGER LINEAR PROGRAMMING

In this section, we develop an optimal solver that schedules computation, memory allocation and garbage collection during the evaluation of general data-flow graphs including those used in neural network training. Our proposed scheduler minimizes computation or execution time while guaranteeing that the schedule will not exceed device memory limitations. The rematerialization problem is formulated as a mixed integer linear program (MILP) that can be solved with standard commercial or open-source solvers.

4.1 Problem definition

A computation or data-flow graph \( G = (V, E) \) has \( n \) nodes \( V = \{v_1, \ldots, v_n\} \) that represent operations yielding values (e.g. tensors). These operations depend on the results of other operations, with dependencies specified by \( m \) edges \( E \). Operations are neural network layers such as convolutions, fully connected layers, and activation functions, and values include activations and gradients stored in memory. Operations may also depend on parameters, or weights, which are stored in memory.

In this work, we impose a topological order over the nodes, such that operation \( j \) may only depend on the results of operations \( i < j \). This topological ordering specifies an execution order for the graph, and is given by user code in eager-execution frameworks such as PyTorch [44]. For convenience, we refer to nodes by their index in the ordering. Separating ordering and allocation is common in compiler design, and both GCC [43] and LLVM [35] have separate instruction scheduling and register allocation passes.

We wish to find a feasible schedule specifying the order of memory allocations, evaluations, and garbage collections such that the total computational cost is minimized, subject to a global memory budget \( M_{\text{budget}} \) in bytes. This schedule will be optimal with respect to the topological order and a cost model for the computational expense of operations.

4.2 Partitioning the schedule

Any schedule that evaluates all nodes in the computation graph can be partitioned into \( n \) frontier-advancing stages, where in stage \( t \in [n] \), operation \( t \) is evaluated for the first time. Each operation in the graph can be evaluated once per stage if needed to advance the frontier. The partitioned schedule is represented by binary decision variables \( R \) and \( S \) that indicate whether a node is to be computed and whether it is to be checkpointed at each point in evaluation.

Let \( R_{t,i} \in \{0, 1\} \) be a binary variable, where \( R_{t,i} = 1 \) indicates that operation \( i \) should evaluated in stage \( t \). This computation has cost \( C_i \geq 0 \) in FLOPs or latency, and the result of the operation consumes memory \( M_i \geq 0 \) in bytes.

Further, let \( S_{t,i} \in \{0, 1\} \) indicate that the result of operation \( i \) should be retained in memory at stage \( t - 1 \) until stage \( t \), such that the result is available for use during stage \( t \). This generalizes checkpointing [9, 16, 22, 23, 51], as values can be retained and deallocated many times in our schedules.

The decision variables are instantiated as binary lower triangular matrices. Coupled with an aggressive memory deallocation policy that frees memory as soon as possible (4.4), \( R \) and \( S \) are sufficient to express the evaluation schedule.

4.3 Scheduling with ample memory

First, consider neural network evaluation on a processor with ample memory. Even without a memory constraint, our solver must ensure that checkpointed and computed operations have dependencies resident in memory. Minimizing the total cost of computation across stages with dependency constraints yields objective (1a):

\[
\begin{align*}
\arg \min_{R, S} & \quad \sum_{t=1}^{T} \sum_{i=1}^{N} C_i R_{t,i} \\
\text{subject to} & \quad R_{t,j} \leq R_{t,i} + S_{t,i} \quad \forall t \forall (i,j) \in E, \\
& \quad S_{t,i} \leq R_{t-1,i} + S_{t-1,i} \quad \forall t \forall i, \\
& \quad R_{t,t} = 1 \quad \forall t, \\
& \quad R_{t,i}, S_{t,i} \in \{0, 1\} \quad \forall t \forall i 
\end{align*}
\]

Constraints encode boolean logical formulas for feasibility via arithmetic operations.

Dependencies must be resident Constraint (1b) ensures that an operation is computed in stage \( t \) only if all dependencies are resident in memory. Dependencies can either be recomputed or retained from the previous stage. That is, \( R_{t,j} \implies R_{t,i} \lor S_{t,i} \) if operation \( j \) depends on operation \( i \). Similarly, Constraint (1c) encodes \( S_{t,i} \implies R_{t-1,i} \lor S_{t-1,i} \): retaining a value requires it to either be computed or already be checkpointed.

Frontier advancement Constraint (1d) partitions the schedule into stages and imposes a topological ordering over operations, requiring exactly one new operation to be evaluated per stage. For connected computation graphs with a single leaf node, we could replace (1d) with \( R_{n,n} = 1 \). The ILP solver would then need to choose an evaluation order in conjunction with the rematerialization and check-
pointing pattern. However, imposing an execution order substantially accelerates solving in practice. Analogously, production compilers such as LLVM [35, 43] and GCC separately allocate registers and schedule instructions.

The infinite memory ILP has $O(|V|^2)$ binary decision variables and $O(|V||E|)$ constraints.

### 4.4 Constraining memory utilization

For a schedule specified by $R$ and $S$ to be feasible, the memory used at all points of evaluation must be less than $M_{\text{budget}}$. To constrain memory usage, we introduce memory accounting variables $U_{t,k} \in \mathbb{R}$ into the ILP. Let $U_{t,k}$ denote the memory used while computing node $v_k$ in stage $t$. $U_{t,k}$ is defined recursively in terms of auxiliary binary variables $\text{FREE}_{t,i,k}$ for $(i,k) \in E$, which specify whether node $v_i$ may be deallocated in stage $t$ after evaluating node $v_k$.

We assume that (1) network inputs and parameters are always resident in memory and (2) enough space is allocated for gradients of the loss with respect to parameters. Parameter gradients are typically small, the same size as the parameters themselves. Additionally, at the beginning of a stage, all checkpointed values are resident in memory. Hence, we initialize the recurrence as

$$U_{t,0} = \frac{M_{\text{input}}}{\text{Constant overhead}} + \frac{2M_{\text{param}}}{\text{Checkpoint}} + \sum_{i=1}^{n} M_{i} S_{t,i}$$

Suppose $U_{t,k}$ bytes of memory are utilized after possibly evaluating operation $k$. Before evaluating operation $k+1$, $v_k$ and dependencies of $v_k$ may be deallocated if no longer used. Then, an output tensor for the result of operation $k+1$ is allocated, consuming memory $M_{k+1}$. This yields recurrence (3), depicted in Figure 3:

$$U_{t,k+1} = U_{t,k} - \text{mem\_freed}(v_k) + R_{t,k+1} M_{k+1}$$

where $\text{mem\_freed}(v_k)$ expresses the amount of memory that can be freed by deallocating $v_k$ and its dependencies.

$R$ and $S$ as booleans, where $1[\cdot]$ is the indicator function,

$$\text{mem\_freed}(v_k) = \sum_{i \in \text{DEPS}[k] \cup \{k\}} M_i \ast \text{FREE}_{t,i,k}$$

and $\text{FREE}_{t,i,k} = 1 \left[ R_{t,k} \land \neg S_{t+1,i} \land \bigwedge_{j \in \text{USERS}[i]} \neg R_{t,j} \right]$.

Logically, $M_i$ bytes are deallocated if dependency $v_i$ is not checkpointed for the next stage nor used for later computation within the stage. That is, $\text{FREE}_{t,i,k} = 1$ if and only if $v_i$ can be deallocated in stage $t$ after evaluating $v_k$. Predicating on $R_{t,k}$ in (5) ensures values are only freed once. To express $\text{FREE}$ in our ILP, (5) must be defined arithmetically with linear constraints. Applying De Morgan’s law for union and intersection interchange,

$$\text{FREE}_{t,i,k} = \neg \left( R_{t,k} \lor S_{t+1,i} \lor \bigvee_{j \in \text{USERS}[i]} R_{t,j} \right)$$

$$= \left( 1 - R_{t,k} + S_{t+1,i} + \sum_{j \in \text{USERS}[i], j > k} R_{t,j} \right)$$

$$\triangleq \text{num\_hazards}(t, i, k) = 0$$

where $\text{num\_hazards}(t, i, k)$ is introduced simply for notational convenience. Relation (6) is implemented with linear cast-to-boolean constraints. Relation (7) is implemented with linear constraints.

$$\text{FREE}_{t,i,k} \in \{0, 1\}$$

$$1 - \text{FREE}_{t,i,k} \leq \text{num\_hazards}(t, i, k)$$

$$\kappa(1 - \text{FREE}_{t,i,k}) \geq \text{num\_hazards}(t, i, k)$$
4.5 Complete Integer Linear Program formulation

The complete memory constrained MILP follows in (8), with $O(|V||E|)$ variables and constraints.

$$\arg\min_{R, S, U, \text{FREE}} \sum_{t=1}^{n} \sum_{i=1}^{t} C_i R_{t,i}$$

subject to

(1b), (1c), (1d), (1e),
(2), (3), (7a), (7b), (7c),
$U_{i,k} \leq M_{\text{budget}}$

4.6 Constraints implied by optimality

Problem 8 can be simplified by removing constraints implied by optimality of a solution. In (2), all values with $S_{t,i} = 1$ are allocated space, even if they are unused. If such a value is unused, the checkpoint is spurious and the solver can set $S_{t,i} = 0$ to reduce memory usage if needed.

Further, $\text{FREE}_{t,k,k} = 1$ only if operation $k$ is spuriously evaluated with no uses of the result. Hence, the solver can set $R_{t,k} = 0$ to reduce cost. When constructing the MILP, we eliminate $|V|^2$ variables $\text{FREE}_{t,k,k}$, assumed to be 0, by modifying (4) to only sum over $i \in \text{DEPS}[k]$. Note that the eliminated variables can be computed inexpensively from $R$ and $S$ after solving.

4.7 Generating an execution plan

Given a feasible solution to (8), $(R, S, \text{FREE})$, we generate a concrete execution plan that evaluates the computation graph with bounded memory usage. This execution plan, or schedule, is constructed via a row major scan of the solution matrices, detailed in Algorithm 1.

A concrete execution plan is a program consisting of $k$ statements $P = \{s_1, \ldots, s_k\}$, where $s_i \in \{\text{allocate, compute, deallocate}\}$. Statement $\%r = \text{allocate } v$ defines a virtual register for the result of the operation corresponding to $v$, used to track memory usage during execution. Such a register must be allocated for $v$ before an instance of statement $\text{compute } v$, $\%r$ in the plan, which invokes the operation and generates an output value which is tracked by the register $\%r$. Finally, statement $\text{deallocate } \%r$ deletes the virtual register, marks the output value for garbage collection, and updates the tracked memory usage.

The execution plan generated by Algorithm 1 is further optimized by moving deallocations earlier in the plan if possible. For example, spurious checkpoints that are unused in a stage can be deallocated at the start of the stage rather than during the stage. Note that this code motion is unnecessary for feasibility as the solver guarantees that the unoptimized schedule will not exceed the desired memory budget.

4.8 Generating static computation graph

For implementation, the concrete execution plan can either be interpreted, or encoded as a static computation graph. In this work, we generate a static graph $G' = (V', E')$ from the plan, which is executed by a numerical machine learning framework. See Section 5.2 for implementation details.

4.9 Cost model

To estimate the runtime of a training iteration under a rematerialization plan, we apply an additive cost model (1a), incurring cost $C_i$ when node $v_i$ is evaluated. Costs are determined prior to MILP construction by profiling network layers on target hardware with random inputs across a range of batch sizes and input shapes, and exclude static graph construction and input generation time.

As neural network operations consist of dense numerical kernels such as matrix multiplication, these runtimes are low variance and largely independent of the specific input data [30, 52]. However, forward pass time per batch item decreases with increasing batch size due to improved data parallelism [6], so it is important to compute costs with appropriate input dimensions.

We statically determine the memory consumption of each value in the data-flow graph as input sizes are known. Values are multi-dimensional tensors stored at 4 byte floating point precision. The consumption $M_i$ is used to construct memory constraints (2-3).

Algorithm 1 Generate execution plan

Input: graph $G = (V, E)$, feasible $(R, S, \text{FREE})$
Output: execution plan $s_1, \ldots, s_k$
Initialize $\text{REGS}[1 \ldots |V|] = -1, r = 0$
for $t = 1$ to $|V|$ do
for $k = 1$ to $|V|$ do
if $R_{t,k}$ then
  // Materialize $v_k$
  emit $\%r = \text{allocate } v_k$
  emit compute $v_k$, $\%r$
  $\text{REGS}[k] = r$
  $r = r + 1$
end if
// Free $v_k$ and dependencies
for $i \in \text{DEPS}[k] \cup \{k\}$ do
  if $\text{FREE}_{t,i,k}$ then
    emit deallocate $\%\text{REGS}[i]$
  end if
end for
end for
work is largely limited to simplified computation graphs, we
The nominal evaluation strategy stores all features generated
Table 1 summarizes baseline rematerialization strategies.
Checkpoint all (Ideal) No rematerialization. Default in deep learning frameworks.
Griewank et al. log n Griewank and Walther [22] REVOLVE procedure
Chen et al. \sqrt{n} Chen et al. [9] checkpointing heuristic
Chen et al. greedy Chen et al. [9], with search over parameter \( b \)
AP \sqrt{n} Chen et al. \sqrt{n} on articulation points + optimal R solve
AP greedy Chen et al. greedy on articulation points + optimal R solve
Linearized \sqrt{n} Chen et al. \sqrt{n} on topological sort + optimal R solve
Linearized greedy Chen et al. greedy on topological sort + optimal R solve
Optimal MILP MILP as formulated in Section 4

4.10 Extension: Recomputing nodes within a stage
In Section 4.2, we allowed each operation in a computation graph to be evaluated in multiple stages, though a given operation could only be evaluated once per stage. Results are cached if needed later within a stage. This allows certain nodes to be evaluated up to \( n \) times, a substantially more flexible search space than prior work. However, the schedule could be partitioned into any number of stages to allow more evaluations of a given node, which may be useful for highly connected graphs. For example, one frontier-advancing stage in our formulation could be split into \( k \) stages, allowing up to \( n \times k \) re-evaluations. In Section 5, we evaluate without splitting stages, so \( k = 1 \).

5 Evaluation
In this section, we demonstrate that optimal rematerialization with Checkmate significantly decreases DNN training memory usage at minimal overhead (Figure 4). Furthermore, by allowing at most a single extra forward pass, we can increase state-of-the-art network batch sizes up to \( 5.1 \times \) over frameworks which store all intermediate values, and up to \( 2.6 \times \) over the best rematerialization baseline (Figure 6). We compare our proposed solver against eight baseline rematerialization heuristics on representative image classification and high resolution semantic segmentation models. As prior work is largely limited to simplified computation graphs, we propose novel extensions where necessary for comparison.

5.1 Rematerialization baselines and generalizations
Table 1 summarizes baseline rematerialization strategies. The nominal evaluation strategy stores all features generated during the forward pass for use during the backward pass – this is the default in frameworks such as Tensorflow. Hence, every layer is computed once. We refer to this baseline as Checkpoint all, an ideal approach given ample memory.

On the linear architectures, such as VGG16 and MobileNet (v1), we directly apply prior work from Griewank and Walther [22] and Chen et al. [9], baselines referred to as Griewank and Walther log \( n \), Chen et al. \sqrt{n} and Chen et al. greedy. To build a tradeoff curve for computation versus memory budget, we search over the segment size hyperparameter \( b \) in Chen’s greedy strategy. However, these baselines cannot be used for modern architectures with simple residual connections. For a fair comparison, we extend Chen’s \( \sqrt{n} \) and greedy algorithms to apply to general computation graphs with residual connections or branching structure (e.g. ResNet50 and U-Net).

Chen et al. [9] suggests manually annotating good checkpointing candidates in a computation graph. For the first extensions, denoted by AP \sqrt{n} and AP greedy, we automatically identify articulation points, or cut vertices, vertices that disconnect the forward pass DAG, and use these as candidates. The heuristics then select a subset of these candidates, and we work backwards from the checkpoints to identify which nodes require recomputation.

Still, some networks have few articulation points, including U-Net. We also extend Chen’s heuristics by treating the original graph as a linear network, with nodes connected in topological order, again backing out the minimal recomputations from the selected checkpoints. These extensions are referred to as Linearized \sqrt{n} and Linearized greedy.

Sections 5.1.1 and 5.1.2 provide more details on our generalizations. Note that all proposed generalizations exactly reproduce the original heuristics on linear networks.

5.1.1 AP \sqrt{n} and AP greedy
We identify Articulation Points (AP) in the undirected form of the forward pass data-flow graph as candidates for checkpointing. Articulation points are vertices that increase the number of connected components (e.g. disconnect) the
graph if removed, and can be identified in time $O(V + E)$ via a modified DFS traversal [26]. An articulation point $v_{at}$ is a good candidate for checkpointing as subsequent vertices in the topological order have no dependencies on vertices before $v_{at}$ in the order. DNN computation graphs are connected, so each intermediate tensor can be reconstructed from a single articulation point earlier in the topological order, or the input if there is no such AP. APs include the input and output nodes of residual blocks in ResNet, but not vertices inside blocks. We apply Chen’s heuristics to checkpoint a subset of these candidates, then solve for the optimal recomputation plan $R$ to restore correctness. Solving for $R$ ensures that the dependencies of a node are in memory when it is computed.

We could find $R$ by solving the optimization (8) with additional constraints on $S$ that encode the heuristically selected checkpoints. However, as $S$ is given, the optimization is solvable in $O(|V||E|)$ via a graph traversal per row of $R$ that fills in entries when a needed value is not in memory.

5.1.2 Linearized $\sqrt{n}$ and Linearized greedy

The data-flow graph $G = (V, E)$ can be treated as a linear graph $G_{lin} = (V, E_{lin})$ with edges connecting consecutive vertices in a topological order:

$$E_{lin} = \{(v_1, v_2), (v_2, v_3), \ldots, (v_{n-1}, v_n)\}$$

While $G_{lin}$ does not properly encode data dependencies, it is a linear graph that baselines can analyze. To extend a baseline, we apply it to $G_{lin}$ to generate checkpoint matrix $S$ from the resulting checkpoint set, and solve for the optimal $R$ with respect to $G$ as in the AP baselines.

5.2 Evaluation Setup

The feasible set of our optimal MILP formulation includes all possible schedules produced by the baselines. This allows us to leverage the same execution planning, static graph generation, and testing infrastructure across the rematerialization strategies. Together, these components form the Checkmate system, illustrated in Figure 5.

Our framework is implemented in Tensorflow 2.0 [1], accepting user-defined models expressed via the high-level Keras interface. We extract the forward and backward computation graph, then construct optimization problem (8) with the Gurobi mathematical programming library as a mixed integer linear program. To accelerate problem construction, decision variables $R$ and $S$ are expressed as lower triangular matrices, as are the memory accounting variables $U$. FREE

**Figure 4.** Computational overhead versus memory budget for (a) VGG16 image classification NN [49], (b) MobileNet image classification NN, and (c) the U-Net semantic segmentation NN [47]. Overhead is measured with respect to the best possible strategy without a memory restriction based on a profile-based cost model of a single NVIDIA Tesla V100 GPU. For U-Net (c), at the V100 memory budget of 16 GB, we achieve a $1.20 \times$ speedup over the best baseline—linearized greedy—and a $1.38 \times$ speedup over the next best—linearized $\sqrt{n}$.

**Takeaway:** our model- and hardware-aware solver produces in-budget solutions with the lowest overhead on linear networks (a-b), and dramatically lowers memory consumption and overhead when residual connections are used (c).
Figure 6. Maximum batch size possible on a single NVIDIA Tesla V100 GPU when using different generalized rematerialization strategies with at most a single extra forward pass. We enable increasing batch size by up to 5.1× over the current practice of caching all activations (on U-Net), and up to 2.6× over the best checkpointing scheme (on MobileNet).

is represented via a $V \times E$ binary matrix. Solutions are generated with a user-configurable time limit of 3600 seconds, though the large majority of problems solve within minutes. Problems with exceptionally large batch sizes or heavily constrained memory budgets may reach this time limit if the solver cannot prove the optimization to be infeasible. Finally, solutions are translated into concrete execution plans and are used to construct a new static training graph.

5.3 Results

Figure 4 compares rematerialization strategies on VGG-16, MobileNet, and U-Net. The y-axis shows the computational overhead of checkpointing in terms of time as compared to baseline. The time is computed by profiling each individual layer of the network. The x-axis shows the total memory budget required to run each model with the specified batch size, computed for single precision training. Except for the $\sqrt{n}$ heuristics, each rematerialization algorithm has a knob to trade-off the amount of recomputation and memory usage (a smaller memory budget leads to higher overhead).

Takeaways: For all three DNNs, our optimal Checkmate formulation produces clearly faster execution plans as compared to algorithms proposed by Chen et al. [9] and Griewank and Walther [22] – over 1.2× faster than the next best on U-Net at the NVIDIA V100 memory budget. Our framework allows training a U-Net at a batch size of 32 images per GPU with less than 10% higher overhead. This would require 23 GB of memory without rematerialization, or with the original baselines without our extensions. In fact, we can increase the batch size even further to 57.

It is interesting to compute the largest batch size that we can use when training these models on a single GPU. The maximum batch size enabled by different rematerialization strategies is shown in Figure 6. The y-axis shows the theoretical maximum batch size we could feasibly train with bounded compute cost. This is calculated by enforcing that the total cost must be less than the cost of performing just one additional forward pass. That is, in Figure 6 the cost is at most an additional forward pass higher, if the specified batch size would have fit in GPU memory. We reformulate Problem (8) to maximize a batch size variable $B \in \mathbb{N}$ subject to modified memory constraints that use $B \times M_i$ in place of $M_i$ and subject to an additional cost constraint (9).

$$
\sum_{i=1}^{n} \sum_{t=1}^{T} C_{i,t,i} \leq 2 \sum_{v_i \in G_{\text{fwd}}} C_i + \sum_{v_i \in G_{\text{bwd}}} C_i
$$

The modified integer program has quadratic constraints, and is difficult to solve. We set a time limit of one day for the experiment, but Gurobi may be unable to reach optimality within that limit. Figure 6 then provides a lower bound on the maximum batch size that Checkmate can achieve.

For fair comparison on the non-linear graphs used in U-Net and ResNet, we use the AP $\sqrt{n}$ and AP greedy generalizations of Chen’s algorithms described in Section 5.1.1. For U-Net, the baselines perform slightly worse than the checkpoint all strategy due to the constrained search space. Let $M_{\text{fixed}} = 2M_{\text{param}}$, as in (2) and let $M_{\text{bwd}}$ be the memory a baseline strategy uses at batch size 1. The maximum baseline batch size is estimated with (10), where the minimization is taken with respect to hyperparameters, if any.

$$
\max B = \left\lceil \frac{16 \text{ GB} - M_{\text{fixed}}}{\min M_{\text{bwd}} - M_{\text{fixed}}} \right\rceil
$$

Costs are measured in FLOPs, determined statically. U-Net, FCN8 and SegNet semantic segmentation networks use a resolution of $416 \times 608$, and classification networks ResNet50, VGG19 and MobileNet use resolution $224 \times 224$. 

Checkmate: Breaking the Memory Wall with Optimal Tensor Rematerialization
Takeaways: We can increase the batch size of U-Net to 57 at a high resolution, an unprecedented result. For many tasks such as semantic segmentation, where U-Net is commonly used, it is not possible to use batch sizes greater than $8-16$, depending on resolution. This is sub-optimal for batch normalization layers, and being able to increase the batch size by $2.6 \times$ (57 vs 22 for a representative resolution) is quite significant. Orthogonal approaches to achieve this include model parallelism and distributed memory batch normalization which can be significantly more difficult to implement and have high communication costs. Furthermore, for MobileNet, Checkmate allows a batch size of 1105 which is $2.19 \times$ higher than the best baseline solution, Chen's greedy heuristic, and $5.1 \times$ common practice, checkpointing all activations.

6 CONCLUSIONS

One of the main challenges when training large neural networks is the limited capacity of high-bandwidth memory on accelerators such as GPUs and TPUs. This has created a memory wall that limits the size of the models that can be trained. Critically, the bottleneck for state-of-the-art model development is now memory rather than data and compute availability, and we expect this trend to worsen in the near future. To address this challenge, we proposed a novel checkpointing and rematerialization algorithm which allows large models to be trained with limited available memory. Our method does not make the strong assumptions required in prior work. In particular, our proposed approach supports general non-linear computation graphs such as residual networks and captures the impact of non-uniform memory usage and computation cost throughout the graph with a hardware-aware, profile-guided cost model.

We presented a MILP formulation for the problem, implemented the Checkmate system for optimal checkpointing and rematerialization in Tensorflow, and tested the proposed system on a range of neural network models including VGG16, VGG19, ResNet50, MobileNet, U-Net, FCN, and SegNet. Furthermore, we showed that Checkmate enables practitioners to train a high resolution U-Net on a single V100 GPU with an unprecedented batch size of 57, as well as batch size of 1105 for MobileNet. The former is $2.6 \times$ larger than the maximum batch size with prior art.

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