Dynamic partial reconfiguration scheme for fault-tolerant FFT processor based on FPGA

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Abstract: The fast Fourier transform FFT processor is an important part of the space real-time signal processing system based on field programmable gate array (FPGA). Since occupying a large amount of logical resources and storage resources, FFT processor is more vulnerable to high-energy particles in space, resulting in single event upset (SEU). This paper presents a novel FPGA scrubbing framework base on dynamic partial reconfiguration technique for a FFT processor to mitigate SEU. The proposed scheme is compared with the blind scrubbing, the reconfiguration time is reduced by 78%. Then, the resource utilisation is 61.5% less than triple modular redundancy scheme. This paper also presents a DPR controller for FFT processor, which is evaluated in terms of hardware resources and reconfiguration time. A comparison to the Xilinx PRC IP shows that multipath delay feedback FFT controller saves 38.6% resources.

1 Introduction

Fast Fourier Transform (FFT) is a basic algorithm in signal processing field. FFT processor is widely used in application, such as communication, image processing, and radar signal processing. Some of proposed applications work in a space radiation environment. With low overhead and fast prototyping, the FPGAs are used as implementation platform in space. However, the strike of high-energy particles on a semiconductor node in the space radiation environment might cause SEU that will lead to an incorrect functionality of the application or a system failure. Thus, effective anti-radiation protection measures should be seriously considered by designer.

Several anti-radiation mechanisms are used to protect FPGAs with different characters in space. Although anti-fuse FPGAs have radiation hardened characteristics, the high cost and limited hardware resources make them unsuitable for the FFT processor [1]. The reconfigurable feature of flash-based FPGAs makes scrubbing technology as a fault tolerant method, but flash-based FPGAs are inappropriate for long missions, as they suffer from high total ionising dose [1]. With high performance and enough resources, SRAM FPGAs are appropriate platform for FFT processor. However, the configuration memory of SRAM FPGAs is sensitive to SEU leading to a bit-flip. When the bit-flip occurred in the configuration memory, the mapped design changes permanently, which may cause incorrect result of FFT processor on the circuit until the device is reconfigured [2]. Therefore, effective SEU mitigation methods should be considered.

Scrubbing technique is to rewrite the configuration memory with an error-free bitstream, which are generally used as error correction. Blind Scrubbing Technique proposed in [3] is the quickest error correction method, where, configuration memory is rewritten with the golden copy continuously, whether an error happened or not. However, lack of error detection mechanism, the scrubber might not immediately react to the SEU, which might cause in non-work status for a long time. Since the large bitstream needs long time to configure, the technique is inappropriate for the large scale FPGA.

On-demand scrubbing technique is proposed to solve the above problem, using scrubbing in conjunction with error detection mechanisms. Two duplication with comparison (DWC) and triple modular redundancy (TMR) are able to provide high fault coverage. The scheme proposed in [4], used three identical modules operating in parallel with a comparator checking outputs for discrepancies to detect faults and a partial reconfiguration controller to reconfigure the module where the bit-flip occurred only. However, DMR and TMR require two or three times hardware resources consumption compared to the original design. In [5], the frame-level redundancy check (CRC) and error correcting codes (ECC) are used instead of module-level redundancy. In [6], an external scrubber is used to read back the configuration memory contexts though select map interface and compares with the golden copy stored in protected external memory. This scheme has high performance in error correction, but the complexity and cost of the system also increase with additional radiation hardened devices and storage resources. However, high availability resources and reliability are demanded simultaneously in space FPGA application.

This paper proposes a novel SEU mitigation scheme for FFT processor, using DPR technique to decrease the failure recovery time. A custom dynamic partial reconfiguration (DPR) controller and Xilinx SEM IP are used to involve a trade-off between extra resources consumption and the fault tolerance on Xilinx KC705 platform.

2 Methodology

2.1 MDF-FFT processor

The N-point discrete Fourier transform (DFT) is defined as:

\[
X(k) = \sum_{n=0}^{N-1} x(n)W_N^{nk} \tag{1}
\]

The Cooley-Tukey algorithm [7] calculates a long sequence DFT of size \( N = M \times L \) by dividing it into several smaller sequences DFT of size \( M \) and \( L \):

\[
\begin{align*}
\left\{ n = L \times m + l \mid m = 0, \ldots, M - 1; l = 0, \ldots, L - 1 \right\} \\
\left\{ k = M \times i + j \mid i = 0, \ldots, M - 1; j = 0, 1, \ldots, L - 1 \right\}
\end{align*}
\]

Then, the DFT can be defined as:

\[
X(i + M \times j) = \sum_{l=0}^{L-1} [X_l(i)W_N^l]W_M^j \tag{2}
\]
where $W_L^m$ is the twiddle factor and $X_L(i)$ is defined as

$$X_L(i) = \sum_{m=0}^{M-1} x(L \times m + i)W_L^m$$  \hspace{1cm} (3)$$

Based on the Cooley–Tukey algorithm, [8] proposed a mixed-radix multipath delay feedback (MDF) FFT processor, where the FFT module is divided into multiple SDF modules and the complete result is calculated from the way of coupling. In Fig. 1, the green block diagram shows the architecture of MDF-FFT processor.

After reproducing the proposed processor design, a data path is implemented to data transfer between the host computer and FPGA, where the Uart-Rx module and two BRAMs are used to receive the time domain sequence $x(n)$ while the four BRAMs and the Uart-Tx module are used to store and transmit the frequency sequence of FFT results $X_L(i)$. The function of the RAM-to-FFT and the FFT-to-RAM module is to send the data in specific length and parallel mode, as the MDF-FFT processor can calculate FFT of twelve different sizes.

2.2 Critical bits

In configuration memory of Xilinx FPGAs, a bit-flip in any of bits mapped to the circuit will change the implementation [9]. However, the bit-flip may not affect the function, as only a percentage of the critical bits influence the performance of the circuit. Compared with other modules, the SDF modules are the main parts, they occupy most logic and storage resources. Since the strike of high-energy particles is a random event, and the position obeys uniform distribution, the most configuration memory bits mapped to SDF modules are more prone to bit-flip, leading to an incorrect computation.

In this paper, the bits mapped to SDF modules are regarded as critical bits. Conversely, non-critical bits are those mapped to other modules. If the SDF modules are implemented as a whole, once a bit-flip occurs, all the SDF modules will be scrubbed simultaneously, which will increase the reconfiguration time and unnecessary external data transfer. Four Pblocks were drawn to divide the SDF modules into four independent reconfiguration modules and divide all critical bits into four parts. The address range of each reconfiguration module bits can be found in the logic location file generated by Vivado, which will be used in the error detection mechanism.

2.3 Proposed scrubbing scheme

This paper proposes a novel partial reconfiguration scheme for fault-tolerant FFT design on Xilinx Kintex-7 FPGA platform. The proposed scheme is based on configuration frame CRC and ECC for detecting errors using SEM IP and uses the partial reconfiguration property of modern FPGA devices to remove the error. Two different protection patterns are used in proposed scheme, where the non-critical part is protected by the SEM controller IP using ECC check while the critical part is protected by the MDF controller using partial scrubbing technique. In Fig. 1, the architecture of reconfiguration is shown in the block marked with red dashed lines.

Once the SEU is detected, SEM controller will report the linear frame address (LFA) of the error to the error detector module. As discussed in the previous section, only the simple frame address can be found in logic location file. Figs. 2 and 3 show the structure of LFA and simple frame address. LFA can be calculated by the follow formula

$$Frame = (offset - frame_offset)/101/32$$
$$Word = frame_offset/32 - 1$$
$$Bit = frame_offset \mod 32 - 1$$

Receiving the LFA, the detector module compares with the border address of each reconfigurable module stored in internal register to find out whether the error is critical one or not. If the error occurred in the non-critical part, SEM controller will repair it immediately using ECC check, while if the error occurred in critical parts, the detector will send the trigger vector to MDF controller to indicate which SDF module need to be scrubbed.

The example design with the structure, where external memory controller (EMC) and partial reconfiguration controller (PRC) connect with each other through the AXI bus, is described in Xilinx Partial Reconfiguration Tutorial [10]. As the Xilinx’s example brings more resource costs, the proposed scheme replaces the structure with the MDF controller. A block diagram of MDF...
controller is shown in Fig. 4. The controller is connected to a micron linear BPI Flash through external memory interface and to configuration memory through ICAP interface. The controller has a set of 32-bit registers. The error detector can monitor the controller status by reading the Status register. Triggers register can be written by the error detector to send the message of fault reconfiguration module. Once receiving the trigger, the controller will fetch the ID, based on address and length of reconfiguration module from the register sets. Then, specified critical bits stored in external BPI flash will be transmitted through the fetch path to reconfigure the SDF module with error with starting the timer. When processing the previous scrubbing, the controller will hold the new trigger and react later.

Fig. 5 shows the storage structure of the bit stream in the BPI Flash. After power up, the BPI flash memory can synchronously configure the FPGA in master BPI mode by full bit stream information from the zero position at the 33 MHz. When scrubbing, the partial bitstreams are transmitted into configuration memory at 30 MHz.

3 Results
As shown in Table 1, the FPGA hardware resource usage in terms of flip-flops (FFs), look-up tables (LUTs), and BRAMs for proposed scheme and comparison with TMR scheme. The FFs, LUTs, and BRAMs are reduced by 61.5, 59.5, and 55.6%, respectively. The comparison of FFs utilisation is shown in Table 2. The comparison result indicates that the MDF controller is 38.8% less than PRC in the use of FFs, while LUTs utilisation is 26.3% than PRC. As shown in Table 3, the reconfiguration time of proposed scheme is only 22% of blind scrubbing scheme.

4 Conclusion
This paper presented a DPR scheme with error detection for fault-tolerance FFT processor in Radiation environment. The proposed scheme consumes less hardware resources than the redundancy scheme and improves the scrubbing speed compared to the blind scrubbing scheme. The MDF controller is used to replace the structure that combines EMC IP and PRC IP, which is considerably smaller than the PRC. The experiment and comparison results indicate that the proposed scheme further improves the availability of system resources.

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6 References
[1] Felix, S., Tanya, V., Jrgen, I., et al.: ‘Mitigation of radiation effects in SRAM-based FPGAs for space applications’, ACM Comput. Surv., 2015, 47, (2), pp. 27–34
[2] Asadi, G.H., Tahoori, M.B.: ‘Soft error mitigation for SRAM based FPGAs’. Proc. 23rd IEEE VLSI Test Symp., 2005, pp. 207–212
[3] Ahmed, A.: ‘New FPGA blind scrubbing technique’. IEEE Aerospace Conf., 2016, pp. 1–9
[4] Tanoue, S., Ishida, T., Ichinomiya, Y., et al.: ‘A novel states recovery technique for the TMR softcore processor’. IEEE Int. Conf. on Field Programmable Logic and Applications, 2009, pp. 543–546
[5] Brosser, F., Milh, E., Geijer, V., et al.: ‘Assessing scrubbing techniques for Xilinx SRAM-based FPGAs in space applications’. Int. Conf. Field-Programmable Technology (FPT), China, Shanghai, 2014, pp. 296–299
[6] Carmichael, C., Caffrey, M., Salazar, A.: ‘Correcting single-event upsets through virtual partial configuration’, Encyclopedia of Genetics Genomics Proteomics & Informatics, 2008
[7] Cooley, J.W., Tukey, J.W.: ‘An algorithm for the machine calculation of complex Fourier series’, Math. Comput., 1965, 19
[8] Yang, C., Wei, C., Xie, Y., et al.: ‘Area-efficient mixed-radix variable-length FFT processor’, IEICE Electron. Express, 2017, 14, (10)
[9] Le, R.: ‘Soft error mitigation using prioritized essential bits’, XAPP538, Xilinx, San Jose, CA, 2012
[10] Xilinx: ‘Vivado design suite tutorial partial reconfiguration’, UG947, 2017
Table 1  Hardware resources of proposed scheme and comparison with TMR

| Scrubbing, scheme | Hardware resource |
|------------------|------------------|
|                  | FF      | LUT      | BRAM   |
| our scheme       | 21,302  | 25,857   | 83     |
| TMR              | 55,272  | 63,792   | 187    |

Table 2  Hardware resources of MDF controller and PRC

| DPR, controller | Target, FPGA | Hardware resource |
|-----------------|--------------|------------------|
| MDF controller  | Kintex-7     | FF 1021, LUT 885 |
| PRC             | Kintex-7     | FF 1667, LUT 1161 |

Table 3  Reconfiguration time of proposed scheme and comparison with blind scrubbing

| Scrubbing scheme | Reconfiguration time, ms |
|------------------|--------------------------|
| proposed scheme  | 1.917                    |
| blind scrubbing  | 8.699                    |