Voltage Quality Enrichment using Transformerless Dynamic Voltage Compensator based on Asymmetrical Multilevel Inverter

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Highlights

• VQ enrichment with lesser filter size with low switching frequency.
• Asymmetrical MLI based Transformerless Dynamic Voltage Compensator.
• P-HIL testing method carried out for dynamic performance analysis.

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Abstract

In this article, Asymmetrical voltage source Multilevel Inverter based Transformerless Dynamic Voltage Compensator (ASMLI-TDVC) for load Voltage Quality (VQ) enrichment is proposed. The ASMLI-TDVC is controlled such that it compensates different levels of VQ problems with lesser Total Harmonic Distortion (THD). Synchronized voltage injection achieved through series transformer from traditional DVC leads to rise in the size of DVC and make system cumbersome. ASMLI based on less switch count topology is utilized for TDVC to overcome these aforementioned issues. Simulation studies of ASMLI-TDVC are carried out using Matlab Simulink software. Further, an experimental model is developed and tested in real-time using OP4500. Results prove that dynamic compensation for VQ improvement is achieved by ASMLI-TDVC.

1. INTRODUCTION

The modern power distribution system is interconnected with various adjustable speed drives, power electronics converters and appliances. This interconnection causes power supply polluted and sometimes intermittent supply for the loads connected at the point of common coupling (PCC) [1]. This polluted power supply becomes Power Quality (PQ) problems for the loads associated with the same system [2]. For a critical load, these PQ problems should be eliminated before supply damages the load. Some common voltage related PQ problems facing by customers are voltage sag, swell, unbalance and interruption [3,4]. To restore PQ from these aforementioned problems, installing of Dynamic Voltage Restorer (DVR) as a compensator is the better solution [5,6]. A series transformer connected in a conventional DVR with the line makes system cumbersome and expensive. Transformerless DVC (TDVC) was introduced by connecting a transformer less inverter in series with the supply line to overcome these transformer issues.

1.1. Comparison of existing TDVC.

Existing topologies of TDVC are categorized and shown in Figure 1. TDVC based on DC to AC converters and AC to AC converters are the two main classifications of TDVC topology. Single H-Bridge inverter and MLI based TDVC are the two divisions of DC to AC based TDVC. Full bridge and half bridge converter based TDVC requires less switches count and less complexity in control. However, when switching frequency increases aiming to filter size decrease with respect to switching loss will increase [7-10]. Hence to reduce filter size along with switching frequency, Multilevel Inverter (MLI)s
are used instead of three level bridge inverter for TDVCs [11,12]. Multilevel inverters are used in power systems for its better quality of output waveform. Cascaded H-Bridge MLI and MLI with reduced number of switches based TDVC are the two categories of MLI based TDVCs [13,14]. MLI with lesser components count is also an important factor for considering the size and losses in the inverter [15]. AC to AC converter based TDVC requires no energy storage devices during compensation, which gives an advantage of less size and weight of the converter. However, it draws more current during compensation which is not feasible for the weak grid [16,17]. The other application of TDVC is used in Transformerless Unified Power Quality Conditioner (TUPQC), which consist of half bridge inverter based TDVC and Distribution Static Compensator (D-STATCOM) with no common DC link capacitor [10,18]. Comparison of existing TDVC is given in Table 1.

![Figure 1. Existing topologies of TDVC](image)

**Table 1. Comparison of existing TDVC**

| Types of converters used for TDVC | Advantages | Disadvantages |
|----------------------------------|------------|---------------|
| Half bridge inverter [8-10]      | Less switch count and easy to control | Requires high switching frequency to reduce filter size, capacitor voltage balance, Low power applications. |
| Full bridge inverter [7]         | Less switch count, easy to control and high power applications. | Requires high switching frequency to reduce filter size. |
| AC to AC direct converter [16]   | Requires no energy storage devices. | Requires more number of switches, high switching frequency. |
| AC to AC indirect converter [17] | Requires no energy storage devices, reduced switch count. | High switching frequency required. |
| Cascaded H-Bridge MLI [5]        | Requires less filter size, High power Applications. | Requires more number of switches, more switching loss. |
| MLI with reduced number of switches (SMLI) [11] | Reduced filter size and less number of switches. | Less number of levels hence more THD. |
| Proposed ASMLI -TDVC             | Reduced filter size, less THD and less switch count even for high levels. | Required more isolated DC sources as levels increases. |

Hence, Asymmetrical Multi Level Inverter (ASMLI) with lesser component count topology is chosen for this presented ASMLI-TDVC. Performance of ASMLI-TDVC is tested by utilizing OP4500 as a real-time controller [19]. Establishment of real world communication between the test device (ASMLI) and
OP4500 are done through analog and digital input output ports. Section 2 gives Configuration of ASMLI-TDVC, followed by ASMLI configuration is presented in section 2.1. Error signal generation for ASMLI-TDVC is given in section 3. Section 3.1, 3.2, and 3.3 gives Generation of error signal, ASMLDC pulse generation and VSI pulse generation method respectively. Section 4 presents simulation results of ASMLI-TDVC followed by hardware testing of ASMLI-TDVC in section 5 and section 6 presents comparison of ASMLI-TDVC results with existing TDVCs. Section 7 presents the conclusion of this work.

2. CONFIGURATION OF ASMLI-TDVC

Figure 2 shows configuration of ASMLI-TDVC for VQ improvement. Power grid supply voltage denoted as $V_s$ is supplied with line impedance $R_s$ and $L_s$ connected respectively to a PCC, where critical load and other loads are interconnected. ASMLI-TDVC is installed confines between PCC and critical load through a series capacitor with the line to protect sensitive load from VQ problems. ASMLI-TDVC comprises of ASMLI, inductive filter $L_f$, capacitive filter $C_f$ and a controller. ASMLI is made up of Asymmetrical Multi Level DC (ASMLDC) converter connected as a source for full bridge single phase Voltage Source Inverter (VSI). Input DC voltage sources $V_{dcs}$, $V_{dc1}$, $V_{dc2}$ and $V_{dc3}$ are connected with three IGBT switches $S_1$, $S_2$ and $S_3$ on the positive side of DC supply. Four reverse bias diodes $D_1$, $D_2$, $D_3$ and $D_4$ are parallel connected to each DC source which acts as a bypass diode when any DC supply disconnect from the circuit. Switching pulses to these switches are generated from ASMLDC pulse generation unit. ASMLDC output voltage $V_{mldc}$ is the input source for VSI. VSI consist of four switches $S_4$, $S_5$, $S_6$ and $S_7$ which are operated such that filtered ASMLI-TDVC output voltage $V_{inj}$ synchronous with PCC voltage $V_{pcp}$ through $L_f$ and $C_f$ to make $V_{inj}$ as sinusoidal. Injected $V_{inj}$ should synchronous with $V_{pcp}$ such that load voltage $V_{load}$ should maintain constant magnitude as 1p.u as given by Equation (1)

$$V_{load} = V_{pcp} + V_{inj}.$$  

(1)

![Figure 2. ASMLI-TDVC for load voltage compensation](image-url)

2.1. Asymmetrical Multilevel inverter (ASMLI) configuration

ASMLI input DC voltages vary from $V_{dcs}$ to $V_{dc3}$. Input DC voltage $V_{dcs}$ is integrated with the circuit such that ASMLDC output level and magnitude will increase by a $V_{dc}$ without increasing in switch count. VSI switching pattern with respect to the VQ conditions controls the supply of $V_{dcs}$. Input DC voltages
from \(V_{dc1}\) to \(V_{dc3}\) are in the ratio of 1:2:4. Equation (2) gives \(i^{th}\) DC voltage value of ASMLDC and input DC voltage of \(V_{dcs}\) is given by Equation (3)

\[
V_{dc i} = \left(2^{i-1}\right) V_{dc} + V_{dcs}
\]  
(2)

where \(V_{dc}\) is denoted as base input DC source voltage and \(V_{dci}\) is the \(i^{th}\) value of DC voltage ranges from 1,2,3…n. Maximum voltage level of Asymmetrical MLDC (ASMLDC) \(N_{dcn}\) is given by Equation (4)

\[
N_{dcn} = (\sum_{i=1}^{n} V_{dc i})
\]  
(3)

Output voltage level of ASMLI \(N_{acn}\) is given by following Equation (5)

\[
N_{acn} = 2(N_{dcn}) + l.
\]  
(4)

Switches present in ASMLDC \(S_{dcn}\) is equal to number of dc voltage source available in AMLDC, as given by following Equation (6)

\[
S_{dcn} = N_{dcn} - 1.
\]  
(5)

Equation (7) gives total number of switches available in ASMLI \(S_{acn}\), where \(S_{acn}\) is the sum of total number of switches available in ASMLDC and in VSI

\[
S_{acn} = S_{dcn} + 4.
\]  
(6)

3. CONTROLLER

Figure 2 shows three controlling sections of ASMLI-TDVC. Section A shows error signal generation for ASMLI-TDVC compensation voltage \(V_{inj}\) during VQ problems occurring. Section B and C shows switching pulse generation for VSI and ASMLDC switches respectively.

3.1. Error signal generation for TDVC compensation.

Clark and Park reference frame theories [20-22] are utilized for error signal generation. Sensed three phase PCC voltage \(V_{pcc}\), as per Equations (8-10) are converted into alpha voltage \(v_{pcc,a}\) and beta voltage \(v_{pcc,b}\) quantities using Clark transformation as per Equations (11-13)

\[
v_a = v_m \sin(2\pi f t)
\]  
(8)

\[
v_b = v_m \sin(2\pi f t - \frac{2\pi}{3})
\]  
(9)

\[
v_c = v_m \sin(2\pi f t + \frac{2\pi}{3})
\]  
(10)

where, \(v_a, v_b, v_c\) are the three phase voltages with 120 degree phase shifted, \(v_m\) is the \(V_{pcc}\) voltage magnitude and \(f_f\) is the fundamental frequency

\[
\begin{pmatrix}
    v_{pcc,a} \\
    v_{pcc,b}
\end{pmatrix} = \frac{1}{\sqrt{3}} \begin{pmatrix}
    1 & -\frac{1}{2} & -\frac{1}{2} \\
    \frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} \\
    \frac{1}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2}
\end{pmatrix} \begin{pmatrix}
    v_a \\
    v_b \\
    v_c
\end{pmatrix}
\]  
(11)

hence,

\[
v_{pcc,a} = \frac{1}{\sqrt{3}} v_a - \frac{v_b}{\sqrt{6}} - \frac{v_c}{\sqrt{6}}
\]  
(12)

\[
v_{pcc,b} = \frac{1}{\sqrt{2}} v_b - \frac{1}{\sqrt{2}} v_c.
\]  
(13)
Phase Lock Loop (PLL) connected to $V_{pcc}$ generates $\omega t$. Matrix Equation (14) gives Park transformation through which voltage direct axis $v_{pcc,d}$ and quadrature axis $v_{pcc,q}$ are determined as per Equations (15-16). By the same Clark and Park transformation method, the reference three phase voltages $v_{ref}$ is converted into reference direct and quadrature voltage axis $v_{ref,d}$ and $v_{ref,q}$ respectively. The Error voltage signals $v_{error,d}$ and $v_{error,q}$ is generated by comparing $v_{pcc,d}$ and $v_{pcc,q}$ as per Equations (20-21). PLL connected with $v_{ref}$ generates $\omega t$, which is used for $V_{inj}$ synchronize with $V_{pcc}$ to make $V_{load}$ constant magnitude

$$
\begin{bmatrix}
v_{pcc,d} \\
v_{pcc,q}
\end{bmatrix} = 
\begin{bmatrix}
\cos \omega t_1 & \sin \omega t_1 \\
-\sin \omega t_1 & \cos \omega t_1
\end{bmatrix}
\begin{bmatrix}
v_{pcc,a} \\
v_{pcc,b}
\end{bmatrix}
$$

(14)

hence

$$
v_{pcc,d} = (v_{pcc,a} \cos \omega t_1 + v_{pcc,b} \sin \omega t_1)
$$

(15)

$$
v_{pcc,q} = (-v_{pcc,a} \sin \omega t_1 + v_{pcc,b} \cos \omega t_1)
$$

(16)

$$
v_{error,d} = v_{ref,d} - v_{pcc,d}
$$

(17)

$$
v_{error,q} = v_{ref,q} - v_{pcc,q}.
$$

(18)

Error voltage D and Q axis as per Equations (17-18) is converted to $\alpha$ and $\beta$ quantities Equations (20-21) by following inverse Park transformation matrix Equation (19)

$$
\begin{bmatrix}
v_{error,\alpha} \\
v_{error,\beta}
\end{bmatrix} = 
\begin{bmatrix}
\cos \omega t_2 & -\sin \omega t_2 \\
\sin \omega t_2 & \cos \omega t_2
\end{bmatrix}
\begin{bmatrix}
v_{error,d} \\
v_{error,q}
\end{bmatrix}
$$

(19)

hence,

$$
v_{error,\alpha} = (v_{error,d} \cos \omega t_2 - v_{error,q} \sin \omega t_2)
$$

(20)

$$
v_{error,\beta} = (v_{error,d} \sin \omega t_2 + v_{error,q} \cos \omega t_2)
$$

(21)

where $v_{error,\alpha}$ and $v_{error,\beta}$ are the error alpha and beta voltage signals. Inverse Clark transformation matrix Equation (22) is utilized for conversion of Equations (20-21) into three phase voltage error signal, which is to be injected by TDVC as given below

$$
\begin{bmatrix}
v_{error,a} \\
v_{error,b} \\
v_{error,c}
\end{bmatrix} = \frac{1}{\sqrt{3}}
\begin{bmatrix}
1 & -1 & 0 \\
\frac{1}{2} & \frac{1}{2} & \frac{\sqrt{3}}{2} \\
\frac{1}{2} & \frac{1}{2} & -\frac{\sqrt{3}}{2}
\end{bmatrix}
\begin{bmatrix}
v_{error,\alpha} \\
v_{error,\beta}
\end{bmatrix}
$$

(22)

hence,

$$
v_{error,a} = \frac{1}{\sqrt{3}} v_{error,\alpha}
$$

(23)

$$
v_{error,b} = -\frac{v_{error,a} + \sqrt{3}v_{error,\beta}}{\sqrt{6}}
$$

(24)

$$
v_{error,c} = -\frac{v_{error,a} - \sqrt{3}v_{error,\beta}}{\sqrt{6}}
$$

(25)

where Equations (23-25) are the three phase error signals used as reference waveform for generation of PWM to the switches of ASMLDC and VSI.

3.2. Asymmetrical Multilevel DC (ASMLDC) Pulse Generation

Error signal generation for ASMLDC is shown in Figure 2, section C. For single phase Equation (23) is compared with dc offsets of seven triangular carrier signals of 2.5 kHz frequency for generation of gating
signals. Figure 3 (a) shows generation of gating signals $g1 - g7$. Gate signals are used for generating of switching pulses of ASMLDC switches as given in Equations (26-28). Figure 3 (b) shows switching pulses of ASMLDC switches [13]

\[ P_1 = (g1 \oplus g2) + (g3 \oplus g4) + (g5 \oplus g6) + g7 \]  
\[ P_2 = (g2 \oplus g4) + g6 \]  
\[ P_3 = g4 \]  

where ‘\( \oplus \)’ symbol denotes XOR gate and ‘+’ sign denotes OR gate. $P_1$, $P_2$ and $P_3$ are the switching pulses for the switches $S_1$, $S_2$ and $S_3$ respectively. ASMLDC switching states are given in Table 2.

![Figure 3. a) ASMLDC pulse generation method b) ASMLDC and ASMLI switching pulse](image)

### Table 2. ASMLDC switching states

| Output levels | ASMLDC Switching states | Voltage levels |
|---------------|--------------------------|----------------|
| 1             | off off off              | $V_{dc1}$      |
| 2             | on off off               | $V_{dc1} + V_{dcx}$ |
| 3             | off on off               | $V_{dcx} + V_{dc1}$ |
| 4             | on on off                | $V_{dcx} + V_{dc2} + V_{dcx}$ |
| 5             | off off on              | $V_{dcx} + V_{dc2}$ |
| 6             | on off on               | $V_{dcx} + V_{dc1} + V_{dcx}$ |
| 7             | off on on               | $V_{dc1} + V_{dc2} + V_{dcx}$ |
| 8             | on on on               | $V_{dcx} + V_{dc2} + V_{dc1} + V_{dcx}$ |

### 3.3. Pulse Generation for VSI

Pulses $P_4, P_5, P_6$ and $P_7$ are the switching pulses for the VSI switches $S_4, S_5, S_6$ and $S_7$ respectively. For single phase, Equation (23) is compared with single carrier signal for generation of $P_4$ and $P_5$ switching pulses. 180 degree phase shift of Equation (23) is compared with the same single carrier signal for generation of $P_6$ and $P_7$ switching pulses. These switching pulses operate at fundamental frequency 50Hz. During normal operation when there is no event occurring, no switching pulse supplied for VSI switches. VSI operates in phase with $V_{pcc}$ during Voltage sag and 180 degree out of phase during voltage swell compensation [8,11]. VSI switching states during conditions such as when there is no disturbance, voltage sag and swell are given in Table 3.
Table 3. switching sequence of VSI switches

| Conditions       | $S_4$ | $S_5$ | $S_6$ | $S_7$ |
|------------------|-------|-------|-------|-------|
| No disturbances  | off   | off   | off   | off   |
| Voltage sag      | on    | on    | off   | off   |
| Voltage swell    | off   | off   | on    | on    |

4. ASMLI-TDVC SIMULATION RESULTS AND DISCUSSION

Figure 4. ASMLI-TDVC during normal condition, voltage sag, swell and unbalance

Figure 5. ASMLDC voltage, ASMLI voltage before and after filter during compensation
The voltage magnitudes of the waveforms are given in per unit (pu) system. The base voltage for each \( V_{dc} \) is supplied as 24\( V_{dc} \). Maximum levels of ASMLDC and ASMLI are calculated by Equation (4) and Equation (5) respectively. ASMLI-TDVC injects zero voltage when controller not sensing any abnormal condition at PCC. Figure 4 shows voltage at PCC \( V_{pcc} \). ASMLI-TDVC injected voltage \( V_{inj} \) and load voltage \( V_{load} \). The time duration of voltage sag is from 0.05s to 0.1s, voltage swell is from 0.15s to 0.2s and voltage magnitude unbalance is from 0.25s to 0.3s respectively. During voltage sag \( V_{pcc} \) reduced to 0.4pu from the supply voltage 1pu, at this time ASMLI produce 17 level output voltage is filtered and inject \( V_{inj} \) of 0.6 pu synchronous with \( V_{pcc} \) to make \( V_{load} \) magmitude constant 1pu. During voltage swell \( V_{pcc} \) increases to 1.3 pu of supply voltage, at this time ASMLI produce 9 level output voltage in 180 degree phase shift of \( V_{pcc} \) is filtered and injected. During voltage unbalance two phases reduced to 0.8 pu hence \( V_{inj} \) injects 0.2 pu voltage such that \( V_{load} \) made constant nominal voltage. Table 4 gives THD comparision of ASMLI before and after filter, number of voltage levels and THD of \( V_{load} \) after compensation. Figure 5 shows ASMLDC output voltage, ASMLI-TDVC output voltage and filtered ASMLI-TDVC voltage during compensation.

5. HARDWARE RESULTS AND DISCUSSION

5.1. Standalone ASMLI working Results

DSO waveform of \( P_1, P_2, P_3 \) and 17 level ASMLI output voltage waveform without filter, working standalone condition with switching frequency of 2.5kHz is shown in Figure 6(a). DC sources of ASMLDC are supplied as per Equation (4) and base voltage \( V_{dc} \) is fixed as 20V. Figure 6(b) shows ASMLI with filter output voltage and current waveform taken using Fluke 43B. The value of connected filter inductor \( L_f \) and filter capacitor \( C_f \) are 4mH and 5\( \mu \)F respectively. THD of output voltage and current are shown in Figure 6(c) and Figure 6(d) respectively. It is seen that both the THDs are within the range of IEEE standards [3,4]. Power converter supplied to 260W load consists of 96.3V and 2.6A.

![Figure 6. ASMLI standalone output results; a) ASMLI output voltage without filter and switching pulses b) Filtered ASMLI output voltage and current waveform c) Filtered ASMLI output voltage THD d) Filtered ASMLI output current THD](image-url)
Total power loss can be calculated by Equation (29). Power losses of each IGBT switch is calculated by Equation (30) and power losses of each anti parallel diode is calculated by Equation (31). Switch conduction loss $P_{s,con}$ is calculated from the Equation (32)

$$P_{loss} = P_s + P_d + P_{fd}$$  \hspace{1cm} (29)

where total power loss is denoted as $P_{loss}$, switch loss is denoted as $P_s$, diode loss is denoted as $P_d$ and freewheeling diode loss is denoted as $P_{fd}$

$$P_s = P_{s,con} + P_{s,sw}$$  \hspace{1cm} (30)

$$P_d = P_{d,con} + P_{d,sw}$$  \hspace{1cm} (31)

$$P_{s,con} = (V_{ce} \cdot I_{s,av}) + R_{s,on} \cdot I_{s,rms}^2$$  \hspace{1cm} (32)

where $V_{ce}$ denoted as IGBT collector-emitter voltage, $I_{s,av}$ denoted as average switch current, $R_{s,on}$ denoted as on state switch resistance and $I_{s,rms}$ denoted as output rms current. Diode conduction loss denoted as $P_{d,con}$ is calculated from Equation (33)

$$P_{d,con} = (V_{d,con} \cdot I_{d,av}) + R_{d,con} \cdot I_{d,rms}^2$$  \hspace{1cm} (33)

where $V_{d,con}$ denoted as diode on state voltage, $I_{d,con}$ denoted as average diode current, $R_{d,con}$ denoted as on state diode resistance and $I_{d,rms}$ denoted as diode output rms current. IGBT switching loss denoted as $P_{s,sw}$ is calculated as per following Equation (34)

$$P_{s,sw} = (E_{s,con} + E_{s,off}) \cdot f_{sw}$$  \hspace{1cm} (34)

where $E_{s,con}$ is the energy loss during turn on transient, $E_{s,off}$ is the energy loss during turn off transient and $f_{sw}$ is denoted as switching frequency. $E_{s,con}$ and $E_{s,off}$ can be calculated by following Equation (35) and (36) respectively. Switch diode can be calculated by Equation (37)

$$E_{s,con} = V_{ce} \cdot I_{s,con} \cdot \frac{t_{rr}+t_{rf}}{2}$$  \hspace{1cm} (35)

$$E_{s,off} = V_{ce} \cdot I_{s,off} \cdot \frac{t_{rr}+t_{rf}}{2}$$  \hspace{1cm} (36)

$$P_{d,sw} = E_{d,con} \cdot f_{sw}$$  \hspace{1cm} (37)

where $t_{rr}$ and $t_{rf}$ denoted as voltage rise time and fall time respectively. $t_{rr}$ and $t_{rf}$ denoted as current rise time and fall time respectively. $P_{d,sw}$ denoted as diode loss, $E_{d,con}$ denoted as energy loss during diode turn on transient. Power loss in freewheeling diode can be calculated by Equation (38)

$$P_{fd} = P_{d,con} + P_{fw}$$  \hspace{1cm} (38)

$$P_{fw} = V_d \cdot I_d$$  \hspace{1cm} (39)

where $P_{fw}$ is the power loss occur during freewheel operation of the diode. Total power loss for the presented converter is calculated by following Equation (40)

$$P_{loss} = 7(P_s + P_d) + 4P_{fd}$$  \hspace{1cm} (40)

where total number of switches are counted as 7 for the presented 17 level inverter output and 4 free wheeling diodes.

A low pass LC filter is used to eliminate higher order harmonic content generated by ASMLI to make $v_{inj}$ as sinusoidal waveform. Filter values are selected by considering equation along with switching
frequency and fundamental frequency [23]. Value of filter inductor \( l_f \) is selected as per Equations (41, 42) and filter capacitor \( c_f \) value is selected as per Equation (43)

\[
l_f = \frac{v_{\text{mldc}}}{24f_s\Delta u_{p-p}} \tag{41}
\]

where \( l_f \) is denoted as filter inductor, \( v_{\text{mldc}} \) is the peak value of asmldc voltage, \( f_s \) is the switching frequency and \( \Delta u_{p-p} \) is the filter inductor peak to peak ripple current

\[
\Delta i_{p-p} < 25\% \frac{P_{\text{rated}}}{v_{\text{inj,max}}} \tag{42}
\]

where \( P_{\text{rated}} \) is the rated power of the converter and \( v_{\text{inj,max}} \) is the maximum compensation voltage of ASMLI-TDVC

\[
c_f = 5\% \frac{P_{\text{rated}}}{2\pi f_f(v_{\text{inj,max}})} \tag{43}
\]

Where \( c_f \) is the filter capacitor and \( f_f \) is the fundamental frequency of the power system.

5.2. Real Time testing method.

Configuration of ASMLI-TDVC testing using Power-Hardware In Loop (P-HIL) method is shown in Figure 7 and experimental setup is shown in Figure 8 [24-26].

![Figure 7. Testing method of ASMLI-TDVC.](image)

![Figure 8. P-HIL Experimental setup of ASMLI-TDVC](image)
Testing of ASMLI-TDVC consist of a PC with Real time interfacing software RT lab is installed and connected to OP4500 through a common server communication. Real time computer modeled power system consists of voltage sag, swell, unbalance and real time controller is made virtually built in OP4500 using Matlab Simulink. Amplifier circuit amplifies digital signal from OP4500 to the switches of ASMLI. Analog signal of test system is given as input signal to OP4500 through analog I/O channels for closed loop operation of ASMLI-TDVC. Thus dynamic performance of ASMLI-TDVC is validated in real time.

5.3. Single phase ASMLI based TDVC Results

Figure 9 (a), (b) shows single phase DSO waveform of \( V_{pcc}, V_{amli}, V_{inj}, \) and \( V_{load} \) during 60% voltage sag occurrence. ASMLI-TDVC injects zero voltage when controller not sensing any abnormal condition at PCC. During voltage sag \( V_{pcc} \) reduced to 0.4pu from the supply voltage 1pu, at this time ASMLI produce 17 level output voltage is filtered and inject \( V_{inj} \) of 0.6 pu synchronous with \( V_{pcc} \) to make \( V_{load} \) magmitude constant 1pu. Figure 9(b) shows magnified view of Figure 9(a) having 5ms/div timing. Figure 9(c) and Figure 9(e) shows \( V_{amli} \) and \( V_{inj} \) having 138.2Vrms and 136.2Vrms respectively during 60% voltage sag taken by Fluke 43B. Figure 9(d) and Figure 9(f) shows THD of \( V_{amli} \) and \( V_{inj} \) during voltage sag having 5.9% and 2.5% respectively. Figure 10 shows the performance of ASMLI-TDVC during 20% voltage sag. During this time \( V_{pcc} \) reduced to 0.8pu from the supply voltage 1pu, at this time ASMLI produce 7 level output voltage is filtered and inject \( V_{inj} \) of 0.2 pu synchronous with \( V_{pcc} \) to make \( V_{load} \) magnitude constant 1pu. Figure 10(b) shows magnified view of Figure 10(a) having 5ms/div. Figure 10(c) and Figure 10(e) shows \( V_{amli} \) and \( V_{inj} \) having 47.7Vrms and 45.3Vrms respectively during 20% voltage sag taken by Fluke 43B. Figure 10(d) and Figure 10(f) shows THD of \( V_{amli} \) and \( V_{inj} \) during voltage sag having 21.5% and 11.7% respectively. Figure 11 shows 30% of voltage swell compensation.

![Figure 9. ASMLI-TDVC experimental results during 60% voltage sag; a) DSO waveform with 10ms time scaling b) DSO waveform with 5ms time scaling c) ASMLI output voltage d) ASMLI voltage THD e) ASMLI-TDVC voltage waveform f) ASMLI-TDVC voltage THD](image-url)
Mohanasundaram RAVI, Chendur Kumaran R/GU J Sci, 33( ): x-x (2020)

Figure 10. ASMLI-TDVC experimental results during 20% voltage sag: a) DSO waveform with 10ms time scaling b) DSO waveform with 5ms time scaling c) ASMLI output voltage d) ASMLI output voltage THD e) ASMLI-TDVC voltage waveform f) ASMLI-TDVC voltage THD

Figure 11. ASMLI-TDVC experimental results during 30% voltage swell: a) DSO waveform with 10ms time scaling b) ASMLI output voltage c) ASMLI output voltage THD d) ASMLI-TDVC voltage waveform e) ASMLI-TDVC voltage THD
Figure 11 (a) shows $V_{pcc}$ increases to 1.3 pu of supply voltage, at this time ASMLI produce 9 level output voltage in 180 degree phase shift with $V_{pcc}$ is filtered and injected. Figure 11(b) and Figure 11(d) shows $V_{asmli}$ and $V_{inj}$ having 69.5Vrms and 67.5Vrms respectively. Figure 11(c) and Figure 11(e) shows THD of $V_{asmli}$ and $V_{inj}$ during voltage swell having 14.7% and 7.2% respectively. Table 4 shows comparison of hardware results of ASMLI-TDVC and THD during compensation. Output results of ASMLI-TDVC are compared with existing systems is shown in Table 5.

5.4. Three phase ASMLI based TDVC Results

Three isolated single phase ASMLI-TDVC connected in series with each phase of supply is controlled by the controller as discussed in section 3 for VQ enhancement. Operation of three phase ASMLI-TDVC is similar to single phase ASMLI-TDVC. Figure 12(a) shows three phase voltage sag occurs at PCC as per Equations (8-10).
6. COMPARISON OF ASMLI-TDVC RESULTS WITH EXISTING TDVC

Proposed ASMLI-TDVC results are compared with existing TDVC on the basis of load voltage THD, filter size, overall all size of the converter, switching frequency required and voltage compensation level. It is observed that proposed ASMLI-TDVC works effectively and results are improved compared with existing TDVC. Load voltage THD, filter size and overall converter size is reduced with increased compensation level. Comparison of presented ASMLI-TDVC with existing TDVC is given in Table 7.

Table 7. Comparison of existing work with presented ASMLI-TDVC

| Category                  | Reference [9] | Reference [8] | Reference [11] | Proposed   |
|---------------------------|---------------|---------------|----------------|------------|
|                           |               |               | LSPWM          | RCPWM      | ASMLI-TDVC |
| Load voltage THD          | 1.2%          | 0.9%          | 0.8%           | 4.86%      | 2.77%      | 1.1%        |
| Overall size of the       | small         | small         | small          | very small | very small |
| converter                 |               |               |               |            |            |
| Filter size               | $L_f$:10mH,  | $L_f$:0.6867mH,| $L_f$:2mH,     | $L_f$:4mH, |           |
|                           | $C_f$:20µf    | $C_f$:50µf    | $C_f$:1100µf   | $C_f$:5µf  |            |
| Compensation level        | 30%           | 30%           | 50%            | 60%        |
| Switching frequency       | 4.2kHz        | 12kHz         | variable       | 2kHz       | 2.5kHz     |

7. CONCLUSION

Dynamic performance of single phase and three phase ASMLI-TDVC during VQ problems compensation is analyzed and verified in real time. P-HIL testing method carried out using OP4500 as a real-time controller. Utilizing reduced components count topology leads to power loss reduction due to less number of components are used. ASMLI produced 17 levels in the output waveform which effect harmonic reduction leads to filter size reduction along with switching frequency of 2.5 kHz. Experimental results prove that ASMLI-TDVC is capable of compensating VQ problems to make load voltage magnitude constant with lesser filter size. Hence further this ASMLI-TDVC can be used significantly in applications such as interline transformerless dynamic voltage restorer and renewable energy integration with different level DC bus voltages.

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

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