Investigation of parameters of Schottky diodes based on chromium silicides

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Abstract. In this work, the parameters of Schottky diodes obtained by sputtering chromium on silicon and annealed at 900÷1100°C were investigated. Experimental studies of Schottky contacts based on silicides have an all-microscopic analysis of the physical and chemical properties of the layers and an analysis of the electrical behavior of the system. The Schottky model assumes that surface states are located on the border between the transition layer and silicon. Using measurements of direct and inverse volt-amperage characteristics (VAC), values of the height of the effective Schottky barrier, the rate of change in the height of the barrier, as well as the value of the density of surface states, the thickness of the transition layer were obtained and the tunneling process was considered. The temperature dependencies of electrical conductivity are given and the course of the curve is analyzed. The obtained VAC is explained by the model of thermionic emission of the Schottky theory. Height of a barrier to contact chrome-silicon silicide which is equal to 0.65 eV is determined, and the factor of ideality was close to unit. The number of steps required by the charge carriers to overcome the potential barrier is determined. It is described that the current transfer mechanism is associated with the presence of surface states at the interface, as well as the occurrence of lattice mismatch and the difference in thermal coefficients. Diode illumination by LED confirms the effect of surface states on VAC. An increase in the surface states of photogenerated holes is shown. It has been shown that the existence of surface states affects the change in the height of the potential barrier, the amount of bending of the zones, and also determines that the predominant transfer mechanism is a tunneling multistage mechanism.

The Schottky of the diode based on the contact of chromium-silicon silicides were made using ingots of n-type silicon single crystal grown by the Chohralsky method with an impurity concentration (2÷9)·10^{15} cm^{-3}. From the ingots of silicon monocrystal, samples were cut with a diamond disk in the form of a rectangular parallelepiped with a size of (1÷2) x (2÷3) x (2÷4) mm^3. After mechanical and chemical treatments, 1200÷2000Å thick chromium was applied to the pure silicon surface at a high vacuum (not lower than 10^{-7} mm.Hg) and annealed in quartz vials.

Temperature dependencies of electrical conductivity for chromium silicides were measured (figure 1). Three sites have been identified in this relationship for CrSi and CrSi2. The first section is the temperature region 150-200°C, where the electrical conductivity decreases linearly as the temperature increases. The second section is the temperature region 150-250 °C, where electrical conductivity increases linearly with increasing temperature. In the first section, chromium silicide behaves metallic. In the third section, the temperature dependence of chromium silicides as in a semiconductor. The
The electrical conductivity of chromium monosilicide is 6-7 times greater than that of disilicide, which is explained by the difference in the number of charge carriers.

The decrease in electrical conductivity in the first region is due to an increase in electron scattering on the phonons of the lattice, on the boundaries of crystalline grains, on crystal imperfections, on impurity ions, etc. It should be noted that in different temperature areas the role of collisions of various kinds is different. In our crystals, the main role is played by scattering at the oscillations of lattice atoms and at the boundaries of crystalline grains.

**Figure 1.** Temperature dependence of electrical conductivity for chromium silicides: 1 - CrSi, for, 2 – CrSi₂.

Direct volt-ampere characteristics after 20 minute heat treatments at temperatures were measured 300°C, 400°C, 500°C (figure 2). As can be seen from the figure, VAC has a linear appearance. The measurement of the inclination angle of the lines with an increase in annealing temperature is explained by the Schottky theory thermionic emission model, according to which VAC is described by the equation

$$I_s = I_s \left[ \exp \left( \frac{e \varphi_{bn}}{nkT} \right) - 1 \right],$$

(1)

where $I_s = SAT^2 \exp \left( -\frac{\varphi_{bn}}{kT} \right)$, $S$ - Schottky area of the diode, $A$ - Richardson constant, $\varphi_{bn}$ - height of the barrier, $n$ - is the ideality factor. The barrier height $\varphi_{bn}$ is derived from the saturation current $I_s = f(V_s)$ density curve using the least squares method. Barrier heights $\varphi_{bn} = 0.5$ eV at a temperature of 300°C, and the ideality factor is 1.3

**Figure 2.** Volt is an ampere characteristic of the Schottky diode based on chromium silicide: 1 – 300°C, 2 – 400°C, 3 – 500°C.
Studies have shown that with an increase in temperature, the height of the barrier decreases, and the ideality factor increases, which can explain the decrease in the inclination angle of straight BAX with an increase in temperature.

In the works of Brezeanu G., Dan P. [1], chromium silicide diodes - n-Si, made according to planar-epitaxial technology, were investigated. The height of the barrier determined by him is 0.62 eV, and factor \( n \) is close to unity. They propose a model based on a heterogeneous distribution of surface state density. The most reproducible and real Schottky diodes are obtained on the basis of contacts from silicides [2, 3]. Experimental studies of Schottky contacts based on silicides have an all-microscopic analysis of the physical and chemical properties of the layers and an analysis of the electrical behavior of the system. The Schottky model assumes that surface states are located on the border between the transition layer and the semiconductor. The model results in a ratio for barrier height:

\[
\varphi_{bn} = \varphi_{bn}^0 - \alpha E_s
\]

where \( \varphi_{bn} \) – height of effective Schottky barrier, \( \varphi_{bn}^0 \) – Schottky barrier height at zero field on the surface, \( \alpha \) – rate of change of barrier height relative to surface electric field, \( E_s \) – electric field on the surface. In this work, using measurements \( I_F-V_F \) (figure 3) and \( I_R-V_R \) (figure 4) VAC values, \( \varphi_{bn}^0, \alpha \), as well as the density value of surface states, the thickness of the transition layer were obtained and a multistage tunneling process was considered.

![Figure 3](image3.png)

**Figure 3.** Direct VAC of the diode CrSi - n-Si. The 1-300 K, 2-77 K.

In theoretical consideration, the model assumes the presence of an interfacial layer between silicon and silicide, having the structure and properties of a glass membrane. This region may be amorphous and metastable. The transition region of the structure differs from silicon and chromium silicide, and determines the electrical properties of Schottky contacts. The zone diagram at thermodynamic equilibrium silicide - transition layer n-Si is shown in figure 4.

![Figure 4](image4.png)

**Figure 4.** The inverse VAC of the diode CrSi - n-Si. 1 - 300K, 2 - 77K.
It is assumed that the transition layer of thickness $d$ is charge free and with properties as for a structure with energy zones varying gradually from metal to the corresponding properties of a semiconductor.

For our model, we assume that the dielectric constant obeys the law:

$$\varepsilon(x) = \varepsilon_m + (\varepsilon_s - \varepsilon_m) \frac{x}{d}, \quad 0 \leq x \leq d \quad (3)$$

The electric field in the transition layer is:

$$\varepsilon(x) = -\frac{(\Delta\varphi)_M}{\lambda} \frac{1}{1 + \left(\frac{e_x}{\varepsilon_m} - 1\right) \frac{x}{d}}, \quad (4)$$

The electric field in the transition layer is: (4)

$$\varphi(x) = -\int_0^x \varepsilon(x) dx = (\Delta\varphi)_M \cdot \left\{1 + \frac{d}{\lambda (\varepsilon_s - \varepsilon_m)} \cdot \ln \left[1 + \left(\frac{e_x}{\varepsilon_m} - 1\right) \frac{x}{d}\right]\right\} \quad (5)$$

At the interface between the transition layer and the semiconductor, the electric field and the electric potential have values from equations (4) and (5):

$$\varepsilon(d) = -\frac{\varepsilon_m}{\varepsilon_s} \frac{(\Delta\varphi)_M}{\lambda} \quad , \quad (6)$$

$$\varphi(d) = \beta(\Delta\varphi)_M + (\Delta\varphi)_M \quad (7)$$

At the interface between the transition layer and the semiconductor, the electric field and the electric potential have values from equations (4) and (5).

Using Gauss's theorem at $x = d$, you can obtain an electric field on the surface of a semiconductor:

$$\varepsilon_s \varepsilon_s = Q_{ss} + \varepsilon_s \varepsilon(d)$$

where - $Q_{ss}$ charge density of surface states.

If the dielectric layer is very thin, as in a good Schottky diode, then the state at the interface well interacts by tunneling with the states in the metal conduction zone and their filling is determined by the Fermi level of the metal. At the same time, with a good approximation, the Fermi-Dirac distribution can be used at an absolute temperature of zero, that is, it can be assumed that all states below $\alpha F$ are filled, and above are empty.

We receive:

$$Q_{ss} = -q \int_{E_F}^{E_F - q(\Delta\varphi)_0} D_S \frac{dE}{1 + \exp \left[\frac{E - E_F}{(kT)}\right]} \quad (9)$$

The value $q(\Delta\varphi)_0$ can be obtained from figure 5 as the energy gap between the Fermi level in the metal and the neutral level. The neutrality level is characterized by the distribution of surface states and when $Q_{ss} = 0$ the neutrality level coincides with the Fermi level. From figure 5:

**Figure 5.** Zone diagram under conditions of thermodynamic equilibrium of metal-transition layer structure -n - semiconductor type.
\( (\Delta \varphi)_0 = E_g - \varphi_{bn} - \varphi_0 \), \hspace{1cm} (10)

where \( E_g \) is the gap width.

By integrating equation (8) and taking into account equation (9) we get:

\[ Q_s = -q^2 D_s (E_g - \varphi_{bn} - \varphi_0 - v_t ln 2), \]

\( \) where \( v_t = \frac{kT}{q} \).

The height of the silicide \( q\varphi_{bn} \)-side barrier is the Schottky barrier. From figure 4 you can define:

\[ \varphi_{bn} = \varphi_M - \frac{\chi}{q} (\Delta \varphi)_M (1 + \beta), \]

\( \) (12)

Where \( \varphi_M \) - operation of metal output, \( \chi \) - semiconductor electronic affinity.

By introducing into equation (8) the expressions (7) and (11) for \( \varepsilon(d) \) and \( Q_s \), respectively, an expression for the definition can be obtained \( \varphi_M \).

Using this expression and substituting in the expression (12), and instead \( \varphi_{bn} \) of equation (2), we get:

\[ \varphi_{bn}^0 = \gamma (\varphi_M - \frac{\chi}{q}) + (1 - \gamma) (E_g - \varphi_0 - v_t ln 2), \]

\( \) (13)

and

\[ \alpha = \gamma(1 + \beta) \frac{\varepsilon_s}{\varepsilon_M} \lambda, \]

\( \) (14)

\( \beta \) – has the form of equation (7), and \( \gamma \) is:

\[ \gamma^{-1} = 1 + q^2 \lambda / \varepsilon_M (1 + \beta) D_s \]

Based on photosonde studies on the conductivity profile, it was determined that our samples could be considered as a Schottky-barrier silicide-semiconductor model. Direct volt-ampere characteristics of \( I_F - U_F \) at temperatures 77 K and 300 K (figure 3) and inverse \( VAC \) \( I_R - U_R \) (figure 4) for the same temperatures were obtained. \( VAC \) in the forward direction is described by the modified equation:

\[ j_F = j_0 \exp \left( \frac{V_F}{n kTq} \right) [1 - \exp \left( \frac{-V_F}{kTq} \right)] \]

where \( n \) is the ideality factor.

Saturation current density depends on \( \varphi_{bn}^0 \):

\[ j_0 = A^{**}_n T^2 \exp(- \frac{\varphi_{bn}^0}{kTq}), \]

\( \) (17)

where \( A^{**}_n \) – constant Richardson for electrons, \( A^{**}_n \approx 120 \frac{A}{K^2 cm^2} \).

The values \( \varphi_{bn}^0 \) and \( n \) were obtained from comparing the real curve with the ratio (16) using the least squares method. The results are shown in table 1.

| Table 1. Results of values of barrier height, ideality factor and \( \alpha \)-parameter. |
|---------------------------------|--------|--------|
| \( I_F - U_F \) | \( \varphi_{bn}^0(B) \) | 0.657 | 0.516 |
| \( n \) | 1.0024 | 1.065 |
| \( I_R - U_R \) | \( \varphi_{bn}^0(B) \) | 0.667 | 0.503 |
| \( \alpha(\AA) \) | 61.0 | 78.0 |
Barrier height $\varphi_{bn}^0 = 0.65 \pm 0.18$ V chromium-cream silicide is characteristic of contact, and the ideality factor is close to unity, which is confirmation of the "almost ideal" behavior of the device.

Figure 4 shows the inverse characteristic of the diode - the dependence of $I_R$ on $\sqrt{V_R + V_D}$ ($V_D$ - diffusion potential).

The reverse branch of the VAC is subject to the law:

$$j_R = j_0 \exp\left(\frac{\varphi_{bs}}{kT}\right) = j_0 \exp\left(\frac{\alpha}{q}\right) \sqrt{(V_R + V_D) \frac{2qN_D}{\varepsilon_s}}$$

(18)

where $\alpha$-is a parameter defined by properties of the boundary layer.

Comparing the experimental curve with equation (18) leads to the definition $j_0$, $\varphi_{bn}$ and $\alpha$. Table 2 shows the results for the reverse VAC branch.

**Table 2.** Results of values of physical quantities: work function of metal, electronic affinity of semiconductor, depth of field penetration, dielectric constants of metal and semiconductor.

| Physical constants | $\varphi_M$ (V) | $\chi$ (eV) | $\lambda$ (Å) | $\varepsilon_M$ (F/cm) | $\varepsilon_s$ (F/cm) |
|-------------------|-----------------|-------------|---------------|-------------------------|-------------------------|
| Sizes             | 4.64            | 4.05        | 2.2           | 8.856·10$^{-14}$        | 9.65·10$^{-13}$         |

The barrier value is close to that obtained from straight VAC. The coincidence between the two results confirms the possibility of using equation (18) to simulate the inverse characteristics.

Using the ratios 7.13.14 and 15 and the found values $\varphi_{bn}^0$ and $\alpha$ from table 1, as well as the constants of table 2, values for the thickness of the transition layer and the density of surface states were obtained, which are presented in table 3.

**Table 3.** Results of the values of the thickness of the transition layer and the density of surface states.

| T(K)  | d(Å) | $D_s$ (eV$^{-1}$ cm$^{-2}$) |
|-------|------|----------------------------|
| 77    | 11.5 | 4.0·10$^{12}$              |
| 300   | 11.5 | 9.8·10$^{12}$              |

The temperature dependence of the band gap was taken as:

$$E_g(T) = 1.785 - 9.025 \cdot 10^{-5} T - 3.05 \cdot 10^{-7} T^2$$

(19)

The obtained temperature dependence of density of surface states is shown in figure 6.

**Figure 6.** Temperature dependence of density of surface states of the diode is chromium-silicon silicide.
From the results obtained, it can be seen that as the temperature increases, the ideality coefficient decreases - this shows that the tunnel mechanism is the predominant current transfer mechanism. In this regard, according to the theory of Franz [4], the direct branch of VAC can be described by the equation:

\[ j_F = j_0 \exp[AV], \]  
where \( A \) is a constant, is determined by the formula:

\[ A = \frac{d(\ln j_F)}{dV} = \frac{q}{kT} \cdot \frac{1}{n} \]

On the other hand:

\[ A = \left( \frac{8}{3h} \right) \sqrt{\frac{m^* \varepsilon}{R N_D}}, \]  
where \( m^* \) — effective electron mass, \( \varepsilon \) — dielectric constant, \( h \) — constant determined by temperature dependence of diffusion potential, \( N_D \) — concentration of donors, \( R \) — number of steps required for charge carriers to overcome potential barrier. Consequently, the following was obtained from BAH:

\[ T = 77 \text{ K} \quad A = 14V^{-1} \quad R = 238 \text{ step} \]
\[ T = 300 \text{ K} \quad A = 39V^{-1} \quad R = 824 \text{ steps}. \]

The reverse branch of the BAX also confirms the multistage tunnel transfer mechanism and it can be represented by (at \( V > 0.1V \)):

\[ I_R V^{-1} \exp \left[ -\lambda (V_D - V)^{-\frac{1}{2}} \right] = q^2 a D_s h^{-1} \]

at \( a \) — lattice constant, \( D_s \) — density of surface states,

\[ \lambda = A(RE)^{3/2} q^{-3/2}. \]

By building a constraint \( \ln(I_R/V) \) from \( (V_D - V)^{-\frac{1}{2}} \) from the experimental straight line, the slope angle was determined \( \lambda \) (figure 7.)

![Figure 7. Inverse VAC of I/V dependence on (V_R-V_D)^{1/2} 1-300K; 2-77K.](image)

\[ T = 77 \text{ K} \quad \lambda = 2.72 \]
\[ T = 300 \text{ K} \quad \lambda = 2.8 \]

Then, values of barriers between steps were found:
$T = 77\text{ K } E_t = 4.02 \cdot 10^{-4} \text{ eV}$

$T = 300\text{ K } E_t = 7.22 \cdot 10^{-4} \text{ eV}$

The effect of lighting on BAC is shown in figure 8, where 1-dark VAC, and 2-VAC during illumination arsenide with gallium light-emitting diode. ($A_{\text{dark}} = 14, A_{\text{lgyt}} = 14.2$)

![Figure 8. Direct VAC silicide-silicon. 1 - in the dark; 2 - at illumination.](image)

A chromium-silicon silicide contact that meets the requirements of the Schottky diode was obtained by shallow chromium diffusion chasing and heat treatment. The Schottky diode model was applied taking into account the intermediate layer between the silicidal nanofilm and silicon to determine the height of the barrier $\phi_{bn}$, the ideality factor $n$, the thickness of the layer $d$ and the density of surface states.

The results show that the height of the barrier decreases as the temperature decreases. Similar results were obtained by Hakama and Harop [5]. This phenomenon can be explained by the following reasons:

- The conditions of the experiment;
- Inhomogeneity of surface layer doping;
- Change of barrier height due to temperature dependence of surface electronic state density.
- Due to the tunnel passage of charges through the barrier.

Evidence of this is the reduction of the ideality coefficient with an increase in temperature, showing that the predominant mechanism of carrier transport through the barrier is the tunneling mechanism, due to the permitted levels of SESSE (surface electronic state of silicon electron) within the band gap.

In addition, Riben's work [6] shows that since direct current exponentially increases with increasing temperature, the tunneling mechanism is multi-stage. This current transfer mechanism is associated with the presence of SESSE at the interface, as well as the occurrence of lattice mismatch and the difference in thermal coefficients. Therefore, the direct current according to [4]

$$ j_F = j_0 \exp(A \cdot V), $$

where the $A$ constant is proportional to the number of steps an electron needs to overcome a potential barrier. It was determined that the number of steps increases with a decrease in temperature. This is due to the fact that at a higher temperature, charge carriers (electrons) have greater kinetic energy and therefore can quickly overcome the potential barrier in fewer steps. And as shown, the energy barrier between steps decreases with decreasing temperature. This was determined from the reverse branch of
VAC, which also confirms the multistage tunnel transfer mechanism. The effect of SESSE on the volt-ampere characteristic of the diode is also confirmed by LED lighting. Lighting increases the current without changing the A parameter. This confirms that photogenerated holes are captured by surface states and increase the tunneling current of electrons. In general, it can be said that at the chromium-silicon silicide interface there is always a SESSE and their effect is great. They affect the change in height of the potential barrier, the amount of bending of the zones, and also determine that the predominant transfer mechanism is a tunneling multistage mechanism.

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