A channel-emulating high-speed transmitter with pseudo-logarithmic and low-bandwidth amplifiers

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Abstract This paper describes a transmitter that can emulate a wide variety of frequency-dependent loss characteristics of high-speed dynamic random-access memory (DRAM) channels, with an aim to facilitate an automated test procedure for a DRAM interface, which does not require physical reconfiguration of channels. Specifically, the proposed transmitter can generate the waveform of an NRZ data stream that has experienced adjustable amounts of skin-effect loss and dielectric loss in electrical channels. To save the hardware cost of implementing a high-speed, high-resolution digital-to-analog converter, the transmitter constructs the waveform using a set of logarithmic and exponential basis functions, each of which is implemented using a pseudo-logarithmic amplifier and low-bandwidth amplifier with adjustable gain and bandwidth, respectively. The prototype chip, fabricated in a 65-nm CMOS process, occupies an area of 5200 µm² and operates over 1.4–7 Gbps while dissipating 38 mW at 7 Gbps. It is demonstrated that the implemented transmitter can emulate 10–40 µm long microstrip lines on an FR4 grade material with a peak error less than 12.5% in the pulse response.

Keywords: high-speed link, transmitter, built-in self-test, channel emu-

1. Introduction

The diversity of high-speed I/O standards for DRAM requires an automated way of doing production tests over a variety of channels [1, 2, 3, 4, 5, 6, 7]. DRAM standards, such as DDR4, LPDDR4, GDDR5, and HBM address different application-specific needs in PCs, mobile devices, graphics processors, and artificial intelligence (AI) accelerators, respectively [8, 9, 10, 11], and use different I/O channels whose loss characteristics span a wide variety, as shown in Fig. 1. However, most types of automated test equipment (ATE) in use for DRAM production tests use fixed, low-loss channels only, in order to share a common command bus between multiple devices under test and reduce the test time [12, 13, 14, 15, 16]. The discrepancies between the ATE test channels and actual memory channels may result in insufficient test coverages, allowing critical defects related to the I/O transceivers to escape.

To address this problem, this work describes a transmitter with a built-in self-test circuit (BIST) that can emulate variable amounts of channel attenuation while transmitting NRZ data streams. With such a transmitter, one can automate production tests for multiple DRAM standards while closing the gap in the channel characteristics.

The proposed channel-emulating transmitter can also help test the margins of high-speed I/O systems whose channels have limited accessibility, as shown Fig. 2. For instance, package-over-package (PoP) of mobile DRAMs and silicon interposers of HBMs integrate dense interconnects within small volumes for high aggregate bandwidths [17, 18, 19, 20], which makes it very difficult to probe individual channels for loss characterization. A BIST transmitter that can electronically emulate variable amount of channel loss without physically swapping in and out of different packages or interposers is essential for measuring additional losses that can be tolerated by these systems.

The rest of the paper is organized as follows. Section 2 examines the loss characteristics of typical high-speed I/O channels and proposes a canonical model. Section 3 then describes the architecture and circuit implementation of a transmitter that realizes the proposed model. Section 4 demonstrates the experimental results obtained from the prototype chip fabricated in a 65-nm CMOS process.

2. Channel attenuation modeling

The loss in high-speed I/O channels can be largely attributed to skin-effect loss or dielectric loss, as shown in Fig. 3(a) [21, 22]. The skin-effect loss is due to the current crowding near the surfaces of conductors at high frequencies, which increases the effective series resistance of the conductor material as a square-root function of the frequency f. On the other hand, the dielectric loss is due to the imaginary permittivity component of the insulating materi-
al, which increases its shunt conductance proportionally with the frequency. The difference in their frequency dependencies makes the skin-effect loss prominent at low-range frequencies and dielectric loss prominent at high-range frequencies. In time domain step responses shown in Fig. 3(b), the skin-effect loss has the prominent effects on the settling tails of the step response, while the dielectric loss has the prominent effects on the initial transition time of the step response [22, 23].

As this work aims to emulate individually-adjustable amounts of skin-effect loss and dielectric loss, a channel is modeled as a cascade combination of a skin-effect-loss-only sub-channel and a dielectric-loss-only sub-channel. Then, the frequency-domain transfer function $H(f)$ of the overall channel can be expressed as the product of the two sub-channel transfer functions, $H_{\text{skin}}(f)$ and $H_{\text{dielectric}}(f)$, which is equivalent to expressing the time-domain impulse response $h(t)$ of the channel as a convolution of two sub-channel impulse responses, $h_{\text{skin}}(t)$ and $h_{\text{dielectric}}(t)$:

$$H(f) = H_{\text{skin}}(f) \cdot H_{\text{dielectric}}(f),$$

$$h(t) = h_{\text{skin}}(t) \otimes h_{\text{dielectric}}(t).$$

For the purpose of implementing a low-cost channel-emulating transmitter, we claim that the sub-channel impulse responses $h_{\text{skin}}(t)$ and $h_{\text{dielectric}}(t)$ can be approximated as a rational function and an exponential function, respectively:

$$h_{\text{skin}}(t) = \frac{c_1}{a_1 t + 1},$$

$$h_{\text{dielectric}}(t) = c_2 \cdot e^{-a_2 t}. \tag{2}$$

Since a step response is equal to the time-integral of the impulse response from time 0, the above claim implies that the step response of the overall channel $s(t)$ can be modeled as a convolution between a logarithmic function and an exponential function:

$$s(t) = a_0 \log(a_1 t + 1) \otimes e^{-a_2 t}. \tag{3}$$

The step response of the overall channel $s(t)$ can be approximated as a convolution of two sub-channel impulse responses, $h_{\text{skin}}(t)$ and $h_{\text{dielectric}}(t)$, respectively:

$$s(t) = \int h_{\text{skin}}(\tau) h_{\text{dielectric}}(t-\tau) d\tau.$$
For two different channels that achieved from IEEE802.3 task group web page [24], the proposed model shows the closer agreements with the S-parameter-based step responses than the two-pole system model. This is mainly due to the fact that the logarithmic function \( \log(a + 1) \) is the better representation of the skin-effect-loss-induced step responses.

3. Architecture and circuit implementation

Fig. 6(a) shows the proposed architecture of the channel-emulating transmitter, which implements the logarithmic step response and exponential step response in (3). The digital input data stream first goes through a skin-effect loss emulator with a logarithmic step response, and its output then goes through a dielectric loss emulator with an exponential step response, basically, a single-pole low-pass filter (LPF). The amount of loss in each emulator stage is adjustable, so that the proposed transmitter can generate an NRZ data stream that has experienced various amounts of skin-effect and dielectric losses.

The skin-effect loss emulator consists of a set of linear amplifiers, delay units, and LPF stages, as shown in Fig. 6(a). The architecture is a modified version of the one in [25], which approximates the logarithmic response in a piecewise manner. That is, the overall logarithmic response is divided into time intervals and the different linear gain of each time interval is modeled by a dedicated amplifier branch. As illustrated in Fig. 6(b), adjusting the time intervals and gains can realize the logarithmic step responses with programmable amount of skin-effect loss. It is noteworthy that the variable time intervals, controlled by the programmable delay units, are instrumental in emulating a wide range of skin-effect loss with a small number of adjustable circuits.

On the other hand, the dielectric loss emulator is implemented as an RC-type LPF to emulate the exponential decay step response. Adjustable amount of dielectric loss can be realized by programming the pole location of the LPF.

Fig. 7 shows the block diagram of the prototype channel-emulating transmitter implemented. It consists of the aforementioned transmitter stage as well as a pattern generator, serializer, and clock generator that feed the data and clock. As shown in Fig. 7(a), the skin-effect loss emulator consists of five amplifier branches, where each amplifier is implemented as a differential, current-mode logic (CML) driver. The gain of each amplifier stage is controlled by its bias current level without altering the output impedance [26, 27]. The bias current level of each amplifier stage is set by a dedicated current-steering digital-to-analog converter (DAC), which receives two control codes: one that is shared among all the amplifier stages and one that is dedicated for each amplifier stage. On the other hand, the delay separation between the amplifier stages is controlled by a set of fine and coarse delay units, as shown in Fig. 7(b). The first delay unit, between the first and second amplifier stages, has the finest resolution of 30 ps and is implemented as a digitally-controlled delay line (DCDL) controlled by a 4-bit thermometer code [28]. The other delay units have the coarser resolutions ranging from 1 to 4 UI and are implemented as flip-flop-based shifters that control the synchronous delay of the data streams feeding the amplifier stages.

The pole frequency of the dielectric loss emulator is adjusted by a capacitor array connected across the differential outputs of the transmitter, via a set of MOS switches controlled by a 7-bit binary code. The cut-off frequencies of the LPFs smoothing the piecewise logarithmic response of the skin-effect loss emulator are also adjustable using the similar programmable switched capacitor array.

The prototype chip also contains a pattern generator and programmable shift register with an additional serializer for testing the channel-emulating transmitter. The pattern generator is capable of generating the pseudo random bit sequence (PRBS) pattern and any user-defined pattern of 256-bit length.

4. Experimental results

The proposed prototype chip was fabricated based on a 65-nm process and its die photograph is shown in Fig. 8. The channel-emulating transmitter occupies a total active area of 5200 \( \mu \text{m}^2 \) and operates with a 1 V supply. When operating at 7 Gbps, the transmitter consumes 38 mW, of which 7 mW is due to the channel-emulating parts. Table I summarizes the prototype chip characteristics and performance.

The proposed channel-emulating transmitter requires three steps to find the set of coefficient values that emulate given channel’s characteristics. The first step is to obtain a step response of the channel to be emulated, either by measuring it directly or by simulating it with an S-parameter model. The second step is to perform a regression analysis that finds the optimal coefficients achieving the best fit to the channel’s step response. The final step is to convert the coefficients to the circuit parameters, such as the bias current levels, delays, and LPF pole frequency.
To validate the operation of the channel-emulating transmitter, a set of FR4 channels with different lengths (10, 20, and 40") are fabricated and emulated, as shown in Fig. 9. The first column shows the measured responses from the channel-emulating transmitter, and the second column shows measured responses from the real FR4 channels. The last column compares the responses of the former two columns and plots the magnified difference between the two. The error is maintained at less than 25 mV (6.25%) at a swing level of 400 mV for all channel lengths. Fig. 9(b) compares the emulated eye diagram and measured eye diagram of the data transmitter across the 10" FR4 channel at 5 Gbps. The results demonstrate good agreement between the emulated responses and measured responses with real channels, confirming the validity of the proposed channel-emulating transmitter.

Fig. 10 shows the additional results emulating the FR408 and Nelco 4000-13SI channels based on the S-parameter models [29, 30]. These channels have 25–50% lower loss tangent than FR4, but have almost the same level of skin-effect loss. The emulation errors are at 12.5%, slightly greater than those with the FR4 channels, due to the fact that the simulated responses with the S-parameter models did not include the additional channel components such as vias and connectors, which were present for the channel-emulating transmitter.

5. Conclusion

A channel-emulating transmitter is proposed to facilitate an automated production test on high-speed memory interfaces with a wide variety of frequency-dependent loss characteristics. To emulate a channel with skin-effect and dielectric losses, this work proposed a model equation that describes the step response of the channel as a convolution of a logarithmic function and an exponential function, each of which characteristics is represented by a very small number of parameters. The proposed channel model is then realized by a set of adjustable-gain CML amplifiers, variable delay units, and adjustable LPF stages, which can effectively emulate variable amounts of skin-effect loss and dielectric loss with low overheads in area and power consumptions. The prototype channel-emulating transmitter implemented in 65-nm CMOS operates up to 7 Gbps and emulate the responses of 10–40" FR4 channels with less than 6.25% errors, demonstrating the viability of the automated production tests with the proposed channel-emulating transmitter.

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