A bulk-driven quasi-floating gate regulated cascode current mirror and its application in squarer circuit

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ABSTRACT A regulated cascode current mirror (RGC) and its improved version with bulk driven quasi floating gate technique (BD-QFG) are presented in this paper. The proposed BD-QFG RGC current mirror (CM) is compared with the conventional (GD) RGC CM to show the performance improvement. The conventional and unconventional CM are implemented in Candace Virtuoso using 90 nm CMOS technology. For input current (I_{in}) varied from 0 to 200 μA and for 0.8 V supply voltage, the simulation results present that the proposed BD-QFG RGC CM has less variation in current transfer error (0.2%) as compared to the GD RGC CM (12%). The output voltage requirement for 200 μA input current is respectively 0.7 V and 0.17 V for the GD RGC CM and the BD-QFG RGC CM. The power consumption of the proposed circuit is 22.71 μW which is 0.15 μW higher than the GD RGC (22.56 μW). The total harmonic distortion (THD) of the proposed circuit is 0.4% which is 1.1% less than the conventional circuit (1.5%). All these improvements in the proposed BD-QFG RGC CM are attained at a cost of 0.05 GHz reduction in frequency (2.31 GHz). The minimum supply voltage of BD-QFG RGC CM and GD RGC CM is 0.4 V and 0.8 V respectively. The designed chip of the proposed BD-QFG RGC CM occupies an area of 29.4 μm². To show the workability of the proposed circuit, a new squarer circuit has been presented.

INDEX TERMS BD-QFG – GD – Current mirror – Squarer

1. INTRODUCTION

Low voltage and low power circuit is demanded in portable electronics to extend the battery lifetime. For analog circuits, higher threshold voltage CMOS technology imposes a serious degrading circuit performance [1].

In the literature, diverse techniques unconventional have been developed to construct the low supply voltage and the low consumption CMOS circuits. The important techniques are the floating-gate (FG) [2], the quasi-floating-gate (QFG) [3] and the bulk-driven (BD) [4]. These techniques have many advantages and disadvantages. The disadvantages of the unconventional techniques (FG, QFG) in comparison to the conventional technique (GD) are the reduction of the effective transconductance, the high occupied chip area and the lower output impedance. Although, these techniques (FG, QFG) offer the possibility of multiple inputs. Moreover, the threshold voltage can be reduced in the FG and QFG techniques [5]. For the BD technique, the threshold voltage is removed, and it can process DC signals. The disadvantage of the BD MOST is the lower transconductance than the FG, QFG and GD MOST. A two new MOS techniques Bulk-Driven Floating-Gate (BD-FG) and Bulk-Driven Quasi-Floating-Gate (BD-QFG) are firstly presented in 2014 [6], experimentally verified and published in the literature [7].

The BD-QFG technique has revealed all the advantages of BD and QFG techniques and suppress their limitations. The symbol of the BD-QFG MOST is shown in Fig. 1.a, and their equivalent circuit is exposed in Fig. 1.b[14]. In this technique, the input signal (V_{in}) is applied to the quasi-floating gate and to the bulk terminal through the capacitance C_{in}. The quasi-floating-gate terminal of the BD-QFG MOST is connected by a very high value resistor (R_{a}) to an appropriate bias voltage (V_{bias}). Practically, this resistance (R_a) is implemented via transistor M_a operating in the cutoff region. The current mirror (CM) structure is an important circuit in many applications, such as the conveyors, the multiplier, the comparator [1], the OTA, the ADC [8], [9] and the DAC. Various researches have been reported to attain the perfect performance of the CM circuit. The characteristic of the CM has a direct impact on the efficiency of the integrated circuits [10]–[12]. The CM presented in [13] is characterized by a low input impedance and a high output impedance. These types of CM are needed to minimize the loading effect. But it has a very high supply voltage and power operation. In [14], using the unconventional technique (BD), a CM circuit is introduced to surmount the limitation of the high supply voltage of the technique GD. This circuit presented an amelioration in terms of power consumption and supply voltage, but it has low bandwidth. High bandwidth in a CM is an important characteristic of increasing the speed of devices. In [15], the CM employs the BD-QFG technique. It presents amelioration in terms of low supply voltage and low input impedance, but it suffers from lowered output impedance and a high number of transistors. Based on the advantages of the unconventional technique (BD-QFG), a new regulated cascode CM circuit is proposed. The interesting performances of the proposed circuit are low voltage supply, high bandwidth, low consumption, and high output impedance. The proposed circuit is employed to realize a high-performance squarer circuit. This paper is arranged as follows. Section 2 presents the proposed BD-QFG RGC CM and calculates its significant performances.
Simulation results are presented in Section 3. Section 4 presents the application of the proposed CM. Finally, Section 5 concludes the paper.

2. Proposed current mirror

2.1. Circuit description

In this part, the operation and implementation of the conventional and unconventional CM are discussed. The conventional RGC CM proposed in [16] is shown in Fig. 2.a. This circuit is composed of a simple CM (M_1, M_2) and an amplification stage. The amplification stage consists of a transistor M_4, a current source I_{B1}, and a cascode transistor M_3. This structure provides a high output impedance owing to the negative feedback offered by the transistor M_4 and the bias current I_{B}.

This circuit performs a low supply voltage and high output impedance. Due to the augmented demand for smaller electronic devices, reducing the supply voltage, removing the threshold voltage, reducing the input impedance and lowering the power consumption becomes necessary.

Fig. 2.b shows the proposed RGC CM. It consists of modified the two transistors (M_1, M_2) based on the GD technique by two transistors M_1 and M_2 based on the BD-QFG technique and to replace the bias source I_{B1} with an active current source M_5.

2.2. Small signal analysis

2.2.1. Output impedance

The small signal analysis for calculating the output impedance of the proposed circuit, is presented in Fig. 3.

At node2:

\[ V_2 = i_{out} r_{02} \]

\[ V_2 = \frac{V_{out} r_{02} + r_{02} g_{m3} V_{32}}{r_{02} + r_{03}} \]  

(4)

At node 3:

\[ V_3 = -g_{m4} \left( \frac{I_{f05}}{r_{04} + r_{05}} \right) V_2 \]  

(5)

Based on these three expressions, the equation for the output resistance is given by:

\[ r_{out} = \frac{V_{out}}{i_{out}} = r_{02} + r_{03} + r_{02} g_{m3} r_{03} \left( 1 + \frac{g_{m4} r_{04} r_{f05}}{r_{04} + r_{05}} \right) \]  

(6)

\[ r_{out} \approx r_{02} \left( g_{m3} r_{03} \right) \frac{g_{m4} r_{04} r_{f05}}{r_{04} + r_{05}} \]  

(7)

From Eq. (1) and (8), it can be noticed that the output impedance of the BD-QFG RGC circuit is near to the conventional GD RGC circuit.

2.2.2. Bandwidth

For calculating the bandwidth, the small signal analysis is presented in Fig. 4.

Assume:

\[ C_z = C_1 + C_{g1} \], \[ C_z = C_{m1} + C_{g1} \], \[ C_z = C_2 + C_{g2} + C_{g1} \], \[ C_A = C_4 + C_3 + C_m \], \[ g_{mBD-QFG} = g_{m eff} + g_{mb1} \]  

and

\[ g_{mBD-QFG} = g_{m eff} + g_{mb2} \]  

At node1:

\[ g_{mBD-QFG} = g_{m eff} + g_{mb1} \]  

(1)

\[ g_{mBD-QFG} = g_{m eff} + g_{mb2} \]  

(2)

Fig. 1. Transistor NMOS BD-QFG: (a) symbol, (b) equivalent circuit

Fig. 2. RGC CM: (a): the GD circuit, (b): the proposed BD-QFG circuit

\[ g_{mBD-QFG} = g_{m eff} + g_{mb1} \]  

(1)

\[ g_{mBD-QFG} = g_{m eff} + g_{mb2} \]  

(2)

Fig. 3. Small signal analysis for calculating the output impedance of the proposed circuit, is presented in Fig. 3.
\[ i_{in} = \left( g_{mBD-QFG1} + sC_A \right) V_i \]  
(8)

At node 2:

\[ V_2 = \left( g_{m3} + sC_{g3} \right) V_i - \frac{g_{mBD-QFG2} V_i}{s(C_{g3} + C_{g4})} \]  
(9)

At node 3:

\[ \frac{i_{out}}{i_{in}} = \frac{g_{mBD-QFG2} \left( g_{m4} + sC_{g3} \right)}{g_{mBD-QFG1} \left( 1 + \frac{2g_{m3} + \omega^2}{\omega^2} \right)} \]  
\[ \frac{L_{out}}{L_{in}} = \frac{g_{mBD-QFG2}}{g_{mBD-QFG1}} \left( 1 + \frac{sC_{g4}}{g_{m4}} \right) \]  
\[ \frac{1}{\omega_{g3}} = \frac{\sqrt{g_{m3} g_{m4}}}{\sqrt{C_{g3} C_{g4} + C_{g3} C_{g5} C_{g4} C_{g5}}} \]  
(12)

\[ \frac{i_{out}}{i_{in}} = \frac{g_{mBD-QFG2}}{g_{mBD-QFG1}} \left( 1 + \frac{j \omega}{\omega_\text{c}} \right) \]  
(13)

\[ \omega_\text{c} = \frac{1}{2\pi} \frac{g_{mBD-QFG}}{C_A} \]  
(14)

3. Simulation Results

The performance of the GD RGC and the proposed BD-QFG RGC is verified through cadence simulator based on 90 nm CMOS parameters under a 0.8 V supply voltage.
conventional and unconventional RGC CM shown in Fig. 2 have been simulated in the same environment to provide an appropriate comparison. The dimensions of transistors and element values of the GD RGC and the BD-QFG RGC CM are identical. For the conventional RGC CM, the current source $I_{B1}$ has been designed by using a transistor $M_s$.

Fig. 5 shows the current transfer characteristic of the conventional GD RGC CM and the proposed BD-QFG RGC for different values of $V_{DD}$ (0.4 V, 0.6 V, and 0.8 V) and $I_{in}$ ranging from 0 to 200 $\mu$A. As it is seen, the proposed circuit exhibits excellent current tracking between input and output currents. The maximum current transfer error for the conventional and unconventional CM circuits for 0.8 V is respectively 12% and 0.2%.

It can be remarked that the BD-QFG RGC CM shows an acceptable current pursuit between the input and the output. In Fig.6, the output current of the GD RGC and of the BD-QFG RGC is plotted for different input current values from 0 $\mu$A to 200 $\mu$A in steps of 50 $\mu$A and for the output voltage ranging from 0 to 0.8 V. The output voltage requirement for the conventional and the unconventional CM circuits is respectively 0.7 V and 0.17 V.

The frequency responses of the RGC CM based on different techniques are compared in Fig. 7. The maximum bandwidth for the GD RGC and the BD-QFG RGC CM is respectively 2.36 GHz and 2.31 GHz, and the power consumption is respectively 22.56 $\mu$W and 22.71 $\mu$W. The bandwidth value of the proposed circuit is very near to the bandwidth value of the GD-MOST.

Fig. 5. Current transfer characteristics of the GD RGC and the BD-QFG RGC CM for different supply voltage

![Current transfer characteristics](image1)

![Frequency response](image2)

![Output voltage characteristic](image3)

Fig. 6. Output voltage characteristic of GD RGC and BD-QFG RGC CM

Fig. 7. Frequency response of the conventional and unconventional RGC CM

To demonstrate the maximum frequency, the transfer function shown in Eq. (20) is calculated by MATLAB and presented in the Fig. 8. It is clear that the simulated and the calculated results are in good agreement. Fig. 9 shows the output impedance, where their value is very near. The output impedance values achieved by the conventional and the unconventional CM are respectively 14.75 G$\Omega$ and 15 G$\Omega$. 

Fig. 8. The simulated and the calculated results of the frequency response of the proposed CM

![Frequency response](image4)

![Output impedance](image5)
Fig. 10 present the resulted output current of the conventional and unconventional RGC CM for a sinusoidal input current signal with a frequency of 10 KHz and a peak-to-peak value of 100 µA, the total harmonic distortion (THD) is respectively 1.5% and 0.4%. The Monte-Carlo analysis is presented of 500 runs for an input current 200 µA for some important specifications including the bandwidth, the current transfer error, and the output impedance. From Fig. 11, it is seen that the proposed CM does not present an important degradation within the mentioned specifications.

The layout of the proposed BD-QFG RGC CM has been done by using 90 nm process technology with cadence virtuoso. The total chip area was 4.2 µm × 7 µm (29.4 µm²). The layout simulation is shown in Fig. 12. The BD-QFG technique shows the best performance in the current mirror design in terms of low supply voltage, low current transfer error, low output voltage and low THD value. While the other parameters (frequency, output impedance, and consumption) are close for both techniques. The comparative study between the BD-QFG RGC CM and GD RGC CM is summarized in Table 1.

The validity of the layout is confirmed by using the post-layout simulation. Table. 2 present a comparison between the post-layout and the pre-layout simulations. From this table, it is clear that the variations between the pre-layout and the post-layout simulations are very weak. The simulation results of the proposed BD-QFG RGC CM are presented with other works in Table. 3.
Table 2. Difference between the pre-layout and the post-layout simulations of the proposed BD-QFG RGC CM

| Parameter                      | Pre-layout | Post-Layout | Percentage variation |
|-------------------------------|------------|-------------|----------------------|
| Bandwidth (G Hz)              | 2.31       | 2.29        | 0.86%                |
| THD                           | 0.4%       | 0.4%        | 0%                   |
| Output impedance (G Ω)        | 15         | 14.92       | 0.53%                |
| Power Consumption (µW)        | 22.79      | 22.79       | 0%                   |

Fig. 12. Layout of the proposed BD-QFG RGC CM

Table 3. Comparative analysis of proposed BD-QFG RGC CM

|                        | [17] | [18] | [19] | [20] | BD-QFG CM |
|------------------------|------|------|------|------|-----------|
| Technology (m)         | 0.13 | 0.18 | 0.18 | 0.18 | 90 n      |
| Supply Voltage (V)     | ±0.5 | ±0.2 | 1    | 0.9  | 0.8       |
| Power Consumption (W)  | 0.83 | 0.34 | 9 m  | -    | 154 μ     |
| Bandwidth (Hz)         | 1.52 G| 285 | 402  | 181  | 2.31 G    |
| Current range (µA)     | 500  | 250  | 100  | 100  | 200       |
| Current transfer error (%) | 3.6 | -    | 0.28 | 0.6  | 0.2       |
| Output impedance (Ω)   | 117 K | 19.5 G| 10.5 G| 1 M | 15 G      |
| Area (m²)              | -    | -    | -    | -    | 29.4 μ    |

4. Application of the CM

4.1. BD-QFG squarer circuit

The squarer circuit is an important circuit in the design of many integrated circuits. It is can be used in many applications such as the current multipliers, the automatic gain controlling, the frequency doublers and the modulator circuit.

The implementation of the conventional and unconventional squarer circuit is discussed in this part. The conventional squarer circuit presented in [21] is shown in Fig. 13.a. This structure is composed of simple current mirrors based on the conventional (GD) technique. According to the above-mentioned advantage of the proposed BD-QFG RGC CM, a new squarer circuit is proposed. Fig. 13.b shows the proposed BD-QFG squarer circuit.

The transconductance of the BD-QFG MOST operating in the saturation region is determined by [6]:

\[ g_{mBD-QFG} = g_{mb} + g_{meff} \]  

\[ g_{m,eff} = \frac{C_{in}}{C_{total}} g_m \]  

\[ g_{mb} = \frac{C_{GC}^2}{C_{BS}} g_m \]  

Where \( C_{Total} \) is the capacitance seen from the QFG, \( C_{in} \) is the input capacitance between the QFG and the input-terminal, \( C_{GC} \) is the gate channel capacitance, and \( C_{BS} \) is the bulk channel capacitance. Using Eq. (21) to Eqs. (23) the transconductance of the BD-QFG MOST can be written as:

\[ g_{mBD-QFG} = C_L g_m \]  

Assume that \( g_{meff} C_{Total} = C_{GC}^2 + C_{in} C_{BS} \), the equation of the transconductance can be expressed as:

\[ g_{mBD-QFG} = \sqrt{2} \beta I_D \]  

Where \( \beta = \mu_0 C_{ox} \left( \frac{W}{L} \right) \) present the transconductance parameter, \( W/L \) present the transistor dimension, \( C_{ox} \) present the oxide gate capacitance and \( \mu_0 \) present the electron mobility.

Using the Eq. (25) and the Eq. (24), the drain current of BD-QFG MOS is given by:

\[ I_D = C_L^2 \frac{\beta}{2} \left( V_{GS} - V_{TH} \right)^2 \]  

\[ V_{GS} = \frac{2I_D}{\beta C_L} \]  

The threshold voltage \( V_{TH} \) is removed in BD-QFG technique [6]. The equation of \( V_{GS} \) can be presented as:
Using Eq. (26), Eq. (27) can be written as
\[
\frac{2I_{D8}}{\beta_8 C_L} + \frac{2I_{D15}}{\beta_{15} C_{L15}} = \frac{2I_{D9}}{\beta_9 C_L} + \frac{2I_{D1}}{\beta_1 C_L}
\]  
(28)

From the circuit schematic show in Fig. 13.b. We have
\[
I_B = I_{D8} = I_{D15}
\]
(30)
\[
I_D = I_{D4} + I_{in}
\]
(31)

Using Eqs. (30) to (32), the Eq. (29) can be expressed by
\[
2 \sqrt{I_B \beta C_L^2} = \sqrt{2I_{D9}} + \frac{2(I_{D4} + I_{in})}{\beta C_L^2}
\]
(32)

Squaring Eq. (33) two times we get
\[
32 I_B I_{D8} = 16 I_B^2 + 4 I_{in}^2 - 16 I_B I_{in}
\]
(33)

Writing the Kirchhoff current law at node A results
\[
I_{out} + I_B = I_{D2} + I_{D9}
\]
(34)

Using Eq. (35) and Eq. (36), the output current of the proposed squarer circuit is expressed by
\[
I_{out} = \frac{I_{in}^2}{4I_B}
\]
(35)

4.2. Simulation results

The simulation results of the conventional and the proposed squarer circuit are simulated through Cadence simulator using 90 nm CMOS technology parameters with 0.8 V supply voltage. The conventional and the proposed square circuit have been verified in the same environment to provide a proper comparison.

Fig. 13: Squarer circuit, (a): Conventional, (b): Proposed

Fig. 14: The DC analysis of the squarer circuit
The bias current ($I_B$) is 20 μA, the input current ($I_{in}$) is varied from 0 μA to 100 μA. The DC analysis of the conventional and the proposed squarer circuit is presented in Fig. 14 and the transient analysis is shown in Fig. 15 with an input signal triangular for 1 MHz frequency and for 100 μA amplitude. The Nonlinearity Errors analysis of the conventional and the proposed squarer circuit are respectively 41% and 0.5%. The simulations of frequency show in Fig. 16 a -3 dB are 320 MHz and 1.2 GHz respectively of the GD and the proposed BD-QFG squarer circuit.

Monte Carlo analysis of the proposed squarer circuit of the bandwidth has been presented in Fig. 17. The simulation results of the proposed BD-QFG squarer circuit are presented with other works in Table. 4.

![Fig. 15. The transient response of the squarer circuit](image)

![Fig. 16. Frequency characteristics of the squarer circuit](image)

**5. Conclusion**

In this paper, a new low voltage low power BD-QFG RGC CM circuit is presented. It is the modified version of the conventional GD RGC CM. This proposed BD-QFG RGC presents a better linearity performance than the GD RGC. The proposed BD-QFG RGC has a 0.2% error current which 11.8% better than the GD RGC (12%), a high output impedance (15 GΩ) and a low power consumption (22.71 µW). The proposed circuit enjoys a higher frequency value (2.31 GHz) near to the frequency value of the GD-MOST (2.36 GHz). The THD value of the proposed RGC CM is 0.4% which is 1.1% less than the conventional circuit (1.5%). The mismatch variation of the proposed RGC is presented using Monte Carlo analysis and this layout simulation is also presented. An application of the proposed BD-QFG RGC CM is presented in the form of squarer circuit to ensure the workability of the proposed CM.

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