A simple and continuous on-state current model of polysilicon thin-film transistors for circuit simulation

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Abstract. A simple and continuous model for the on-state current of polysilicon thin-film transistors, suitable for implementation in circuit simulators, is presented. The model includes the potential barrier at the grain boundaries, the channel length modulation and the excess current due to impact ionization. Comparison between measured output characteristics and the model shows excellent agreement over wide range of bias voltages and for devices with different gate lengths.

1. Introduction

Polycrystalline silicon thin-film transistors (polysilicon TFTs) are important for applications in active-matrix liquid-crystal displays and three-dimensional integrated circuits. For the successful design of circuits, a proper analytical TFT device model is required operating in both linear and saturation regimes. In recent years, several polysilicon TFT models have been developed by adopting an effective medium approach, which treats the nonuniform polysilicon sample as a uniform medium with some effective material properties [1], [2]. The drawback of these models is that the extracted parameters are not directly related to the material properties. Janunski et al. [3] have proposed a semi-empirical short-channel dc SPICE model for polysilicon TFTs operating in all regimes. In this model, the semi-empirical approach results in a physically based model with parameters that are related to the device structure and fabrication process. In other models, a physical model has been proposed in which the effect of the grain boundaries on the I-V characteristics has been considered using the thermionic-diffusion conduction mechanism [4]. The anomalous current increase at high drain voltages, has been explained by the drain induced grain barrier lowering.

Recently, we have developed an analytical on-state drain current model of large-grain polysilicon TFTs, based on the carrier transport through latitudinal and longitudinal grain boundaries [5]. In this model, the material is considered as an array of square grains in the channel, with the current flowing along the longitudinal grain boundaries or through the grains and across the latitudinal grain boundaries. The basic equation is a simple expression for the drain current valid above the charge inversion voltage, which appears to be lower than the current threshold voltage. In the present work, this equation is used to simulate the output characteristics of polysilicon TFTs over wide range of bias voltages and for devices with different gate lengths, by including the channel length modulation and the excess current due to impact ionization.
2. Theoretical model

For a polysilicon TFT of channel width \( W \) and channel length \( L \), the drain current in the linear region of operation of a large grain polysilicon TFT can be adequately described by the relation [5]

\[
I_{ds} = \frac{W}{L} \mu_{\text{eff}} C_{\text{ox}} (V_{gs} - V_{\text{inv}}) V_{ds}
\]

(1)

where \( V_{ds} \) is the drain voltage, \( C_{\text{ox}} \) is the gate oxide capacitance per unit area, \( \mu_{\text{eff}} \) is the effective carrier mobility and \( V_{\text{inv}} \) is the charge inversion voltage which appears to be much lower than the current threshold voltage \( V_T \). In solid phase crystallized (SPC) polysilicon TFTs, due to the columnar structure of the grains, the polysilicon is considered to be composed of an array of square grains, with the drain current following the path either along the grain boundaries or through the grains and across the grain boundaries. In this polysilicon structure, the effective carrier mobility is affected by the barrier height \( V_b \) through the relationship [5]:

\[
\mu_{\text{eff}} = \frac{\mu_{gi}}{1 + \frac{w}{L_g} \exp \left( \frac{qV_b}{kT} \right)} + \frac{L_g}{L_g - w} \mu_{gb/1}
\]

(2)

where \( \mu_{gi} \) and \( \mu_{gb/1} \) is the mobility for a carrier passing through the interior region of the grain and across the grain boundary respectively, \( w \) is the width of the depletion region at the grain boundary which depends on \( V_b \) and the gate-induced carrier concentration in the inversion channel and \( L_g \) is the average grain size. It has been demonstrated that the dependence of \( V_b \) on \( V_{gs} \) can be modelled according to [5]

\[
qV_b = \frac{E_o}{1 + \left( \frac{q(V_{gs} - V_{\text{inv}})}{E_t} \right)}
\]

(3)

where \( E_o \) is the maximum potential barrier which is approximately equal to the half of the silicon bandgap and the parameter \( E_t \) is related to the filling of the traps and thus to the quality of the polysilicon material. Fit of the experimental \( I_{ds} \) versus \( V_{gs} \) data with Eqs. (1) - (3) enables the determination of the parameters \( V_{\text{inv}}, E_o, \mu_{gb/1} \) and \( \mu_{gi} \).

For high drain bias, considering the voltage drop across the channel, the drain current obtained by integrating (1) from the source to the drain can be expressed as

\[
I_{ds} = \frac{W}{L} \mu_{\text{eff}} C_{\text{ox}} \left( V_{\text{inv}} V_{ds} - \frac{V_{ds}^2}{2 \alpha_{\text{sat}}} \right)
\]

(4)

where \( V_{\text{inv}} = V_{gs} - V_{\text{inv}} \) and \( \alpha_{\text{sat}} \) accounts for the depletion charge variation across the channel. By taking into account the channel length modulation, the impact ionization near the drain and the effective gate and drain voltages \( V_{\text{inv,e}} \) and \( V_{ds,e} \) respectively for a smooth transition from the linear to the saturation region, Eq. (4) can be written as

\[
I_{ds} = \frac{W}{L} \mu_{\text{eff}} C_{\text{ox}} \left( V_{\text{inv}} V_{ds,e} - \frac{V_{ds,e}^2}{2 \alpha_{\text{sat}}} \right) 1 + \frac{\Delta V_{ds}}{1 - I_{ds}}
\]

(5)

where

\[
V_{ds,e} = \frac{V_{ds}}{\alpha_{\text{sat}} V_{\text{inv,e}}} \left[ 1 + \left( \frac{V_{ds}}{\alpha_{\text{sat}} V_{\text{inv,e}}} \right)^{m_{\text{eff}}} \right]^{-m_{\text{eff}}}
\]

(6)
$V_{ds,e}$ is approximately equal to $V_{ds}$ for $V_{ds} < \alpha_{sat}V_{ginv}$ and remains constant at $\alpha_{sat}V_{ginv}$ in saturation, and $m_1$ is a parameter that fits the transition. The factor $(1+\lambda V_{ds})$ describes the current increase caused by channel length modulation and $\Delta I$ is the excess drain current related to impact ionization. It has been demonstrated experimentally that the normalized excess current $\Delta I/I_{ds}$ is a second order polynomial function of $(V_{ds} - V_{kink})$ [6]

$$\frac{\Delta I}{I_{ds}} = A_1 (V_{ds} - V_{kink}) + A_2 (V_{ds} - V_{kink})^2$$

(7)

where $A_1$ and $A_2$ are fitting parameters and $V_{kink}$ is the $V_{ds}$-value for the onset of the kink effect which corresponds to the maximum of the device output resistance. Experimental measurements have shown that $V_{kink}$ is a linear function of $V_{gs}$ and only few output characteristics are needed to establish the relationship between $V_{kink}$ and $V_{gs}$ [6]. Equations (5) - (7) can be used to reproduce the experimental output characteristics with six fitting parameters $\alpha_{sat}$, $\lambda$, $\delta$, $m_1$, $A_1$ and $A_2$.

3. Comparison with experimental results

The proposed on-state current model is applied in polysilicon TFTs fabricated on fused quartz glass substrates. First, amorphous silicon film (50 nm thick) was deposited on the oxidized glass substrates by low pressure chemical vapor deposition at 425 °C and pressure 1.1 Torr and then crystallized by furnace annealing at 600 °C for 24 h in nitrogen ambient. Then, the crystallized specimens were irradiated at room temperature by KrF excimer laser ($\lambda = 248$ nm) with energy density varying from 280 mJ/cm$^2$ in air ambient. A standard n-channel metal-oxide-semiconductor (NMOS) self-aligned process was used to fabricate devices of gate width $W = 10$ µm and gate lengths $L = 4$ and 10 µm. As gate insulator, a 120 nm thick SiO$_2$ was deposited by ECR-PECVD at 100 °C.

Figure 1 shows the experimental transfer characteristics of two typical polysilicon TFTs and the simulated characteristics based on Eqs. (1) - (3) using the fitting parameters: $V_{inv} = 0.485$ V, $\mu_{gb} = 1.32$ cm$^2$/Vs, $\mu_{gi} = 38.95$ cm$^2$/Vs and $E_t = 2.51$ eV for the TFT with gate length $L = 4$ µm and $V_{inv} = 1.43$ V, $\mu_{gb} = 0.225$ cm$^2$/Vs, $\mu_{gi} = 37.53$ cm$^2$/Vs and $E_t = 3.06$ eV for the TFT with gate length $L = 10$ µm.

To evaluate the excess current $\Delta I$ related to impact ionization, we determined the kink voltage at different gate voltages from the maximum of the output resistance [6]. A plot of $V_{kink}$ versus $V_{gs}$ is presented in Fig. 2, showing that $V_{kink}$ increases linearly with increasing $V_{gs}$ following the relation $V_{kink} = 3.26 \times 10^{-3} + 0.554 V_{gs}$ for the TFT with gate length $L = 4$ µm and $V_{kink} = 1.18 + 0.418 V_{gs}$ for the TFT with gate length $L = 10$ µm. This linear relationship can be derived by analyzing a reduced set of experimental data so that the kink voltage can be easily predicted for any bias condition. The parameter $V_{inv}$ and the variations of $\mu_{eff}$ and $V_{kink}$ with $V_{gs}$ are used for simulation of the output characteristics.

Figures 3 and 4 show the output characteristics $I_{ds}$ -$V_{ds}$ of the polysilicon TFTs with gate lengths $L = 4$ and 10 µm, respectively, for various gate voltages. The model describes adequately the measured results over wide ranges of gate and drain voltages, using the parameters $\alpha_{sat} = 0.424$, $\lambda = 0$, $m_1 = 2.02$, $A_1 = 0.0103$ and $A_2 = 0.0276$ for the TFT with gate length $L = 4$ µm and $\alpha_{sat} = 0.1$, $\lambda = 4.86$, $m_1 = 0.7$, $A_1 = 0.0053$ and $A_2 = 0.003$ for the TFT with gate length $L = 10$ µm. It is interesting to note that the parameter $\lambda$ is zero for the TFT with $L = 4$ µm, whereas the excess current due to impact ionization is much larger in the device with the shorter channel length. These findings indicate that the appearance of the channel length modulation effect is prevented in short channel devices due to the fact that the kink effect is strong occurring at lower $V_{ds}$.

4. Conclusion

The on-state current model of polysilicon TFTs is based on a simple expression for the drain current, valid above the charge inversion voltage which is much lower than the current threshold voltage. The model includes the potential barrier height at the grain boundaries, the channel length modulation and the excess current due to impact ionization, and provides accurate description of the transfer
characteristic in the linear regime and of the output characteristics of polysilicon TFTs over a wide range of bias voltages and for devices with different gate lengths. The model parameters can be extracted straightforwardly and it can be implemented without difficulty into circuit simulation.

![Figure 1](image1.png)  
**Figure 1.** Experimental (symbols) and simulated (lines) transfer characteristics of polysilicon TFTs with different gate lengths.

![Figure 2](image2.png)  
**Figure 2.** $V_{\text{kink}}$ vs $V_{\text{gs}}$ of the TFTs of Figure 1.

![Figure 3](image3.png)  
**Figure 3.** Experimental (symbols) and simulated (lines) output characteristics of the TFT with gate length $L=4 \mu m$.

![Figure 4](image4.png)  
**Figure 4.** Experimental (symbols) and simulated (lines) output characteristics of the TFT with gate length $L=10 \mu m$.

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