INTRODUCTION

An exponential increase in the performance of silicon microelectronics and the demand to manufacture in great volumes has created an ecosystem that requires increasingly complex tools to fabricate and characterize the next generation of chips. However, the cost to develop and produce the next generation of these tools has also risen exponentially, to the point where the risk associated with progressing to smaller feature sizes has created pain points throughout the ecosystem. The present challenge includes shrinking the smallest features from nanometers to atoms (10 nm corresponds to 30 silicon atoms). Relaxing the requirement for achieving scalable manufacturing creates the opportunity to evaluate ideas not one or two generations into the future, but at the absolute physical limit of atoms themselves. This article describes recent advances in atomic precision advanced manufacturing (APAM) that open the possibility of exploring opportunities in digital electronics. Doing so will require advancing the complexity of APAM devices and integrating APAM with CMOS.

APAM

The era of atomic manipulation, the ability to place or move single atoms with the spatial precision of single atomic sites in some host material, began in 1989 when Don Eigler used a scanning tunneling microscope (STM) to position 35 Xenon atoms on the surface of nickel to spell out the IBM logo. Similar positioning precision has since been achieved using a broad range of atoms and materials, and different manipulation approaches. However, to date, only one pathway, which we refer to as APAM, has been used to produce functioning atomic precision electronic devices in silicon.

APAM places dopants into silicon using surface chemistry, a mechanism not typically used in microfabrication. Examining the process, shown in Fig. 1, reveals some key contrasts with standard processing. The Si (100) surface common to microelectronics has one reactive bond per atom, which can be made unreactive by attaching a hydrogen atom. Starting with a surface fully passivated by hydrogen, which serves as a monatomic resist, an STM can remove hydrogen atoms from silicon atoms site-by-site at high bias, and image the surface at low bias. The hydrogen atom is either present or absent at each site. As a result, the resist cannot be overexposed, in contrast to the resists used in next-generation extreme ultraviolet (EUV) photolithography. The depassivated pattern is transferred into the silicon using surface chemistry. Importantly, APAM has shown the atomically precise placement of dopants and semiconductors, but pathways for oxides...
and metals have yet to be discovered. Phosphine, a dopant precursor, only attaches to silicon surface sites that have an unsatisfied bond, and not to those sites that remain passivated with hydrogen. Phosphine only produces an electrically active phosphorus donor in windows that are at least six atomic sites in size, which has the effect of error-correcting imperfections in the resist.\[10\]

Lastly, capping the surface with a few nm of silicon at moderate temperatures (300°C) satisfies all the bonding to the phosphorus dopant, donating an electron to silicon. The low temperatures enable APAM to achieve higher densities than any other approach—typically 1.7 x 10^{14} cm^{-2} (or over 1 x 10^{21} cm^{-3} in a single atomic plane).\[11\] Other approaches, such as selective area growth and ion implantation, are limited by the equilibrium concentration of phosphorus in silicon because they require higher temperatures.

Currently, two outstanding challenges inhibit using APAM to develop microelectronics: the need to (1) evolve the complexity of APAM devices relative to the simple devices that have been fabricated so far and (2) integrate with existing CMOS processing (Fig. 2). For both challenges, we will describe the state-of-the-art, the key limitations, and paths forward.

**ADVANCING DEVICE COMPLEXITY**

Figure 3 shows a schematic, image, and electrical transport data of an APAM device. This device probes the electronic structure of the two islands between the source and drain leads, each containing only a handful (two to four) of phosphorus donors. The basic characteristics of this device—that it only contains donors, demonstrates basic physics principles, and operates only at cryogenic temperatures (< 4 K)—are common to nearly all state-of-the-art APAM devices.\[5\] In contrast, digital
microelectronics require significantly more complicated device structures, containing both donors and acceptors, with material stacks that permit extensive engineering of the switching performance, all operating at room temperature. Each of these presents a significant challenge.

Acceptor doping is needed to make complementary transistors (Fig. 4a). While the semiconductor industry employs a number of precursor molecules that are acceptor analogues of phosphine—diborane, boron trifluoride, and trimethyl aluminum, for example—it is unclear whether any can be used with the chemical contrast created by hydrogen-terminated and unterminated silicon. Even if an acceptor can be used, whether they produce a high density of electrically active dopants at temperatures where the hydrogen mask is stable, below 430°C, has not been shown. Early work from IBM-Zurich indicates that diborane satisfies the first of these requirements, with the electrical quality of the material remaining an open question. Another reason for optimism is the development of halogen-based resists, which may provide a different kind of chemical contrast from hydrogen.

Digital electronics rely on the ratio of on and off currents in a transistor to be very large. This requires surface gates with higher gain than the dopant-based structures used historically for this purpose in APAM devices (Fig. 4b). Adding a high-gain surface gate to an APAM device is complicated because phosphorus dopants diffuse above 500°C, destroying the atomic precision of the device. This prevents the use of common dielectrics, like silicon dioxide, which require high growth temperatures. It does leave open low-leakage high-k/metal gates, although these require complicated multi-layer material stacks (Fig. 4b). In an encouraging recent development, the first fab-compatible surface gate has recently been implemented atop an APAM device.

Another obstacle is realizing device operation at room temperature, which again requires advancing APAM device complexity. At cryogenic temperatures, the density of donors produced by APAM is so high that it provides significant confinement of the electrons, and leakage paths around the dopant layer are frozen out. Room temperature operation requires adding features that confine current to the transistor channel and block unintentional leakage paths (Fig. 4c). For the channel of the transistor itself, confinement can be enhanced by adding acceptors to create a local electric field. Here, the standard preparation method for APAM samples—Joule heating of the silicon—destroys heavily acceptor-doped substrates, so alternative sample preparation techniques are being explored.

CMOS INTEGRATION

The second outstanding challenge in applying APAM to digital microelectronics is interfacing APAM and CMOS on the same die (Fig. 5). While the thermal budget to incorporate activated dopants using APAM is modest, the temperature necessary to prepare the atomically clean surfaces required for APAM has typically been 1200°C. Should APAM come after CMOS fabrication, this temperature would destroy the products of high-temperature steps in a CMOS workflow, the so-called front end of line (FEOL). Similarly, the APAM device only survives up to 500°C, which is insufficient to execute FEOL CMOS manufacturing after APAM. Recently a sample cleaning method operating at 850°C has been demonstrated. This means APAM can fit into a split CMOS fabrication process, wherein high temperature steps such as ion implantation and initial oxidation precede APAM, which is followed by low temperature steps such as oxide deposition and metallization.
The reduced temperature APAM clean should leave the FEOL CMOS fabrication steps undisturbed, although this has yet to be proven out on real parts. Similarly, back end of line (BEOL) CMOS fabrication steps require low enough temperatures that they should leave the APAM device undisturbed, although that too has yet to be proven out.

An opportunity exists to add APAM features to CMOS circuits even later in fabrication, at the cost of reduced precision (Fig. 6). The temperature required to clean silicon can be reduced to just 100°C by leveraging exotic chemical preparations\[^{17,20}\]. This temperature is less than the operating temperature for most CMOS parts, and opens the door to adding APAM features inside APAM target windows designed into these parts. Wet chemical routes to cleaning silicon do not produce atomically perfect surfaces, but the surface appears clean enough to execute a reduced resolution APAM process. The other steps of the APAM process, from hydrogen termination to dopant incorporation and silicon capping, work with slightly reduced effectiveness at ambient temperatures when starting with atomically perfect surfaces. Patterning the resist becomes a few times less efficient, dopant activation falls from nearly 100% to 75%, and conductivity goes down by a factor of three. These steps have yet to be combined into a single process flow, and the effect of APAM on the functionality of the CMOS host remains unknown, but this approach remains promising.

PROSPECTUS

Existing data on APAM devices indicates that the work detailed above may well be justified due to the high performance enabled by APAM fabrication. Figure 7 shows that an APAM nanowire can support a current density of up to 2 mA/µm, at 4K, which exceeds modern CMOS, at room temperature. This extremely high current density is likely the result of the high density of carriers, and a sizable confinement potential, both courtesy of the high dopant density. There are reasons to expect much of this performance to be preserved on warming to room temperature. Related quantities such as the carrier density and mobility, as measured by infrared ellipsometry at room temperature, agree with cryogenic Hall measurements to within a factor of two. The current density may be further enhanced by adopting modern approaches, including three-dimensional geometries\[^{21}\] and engineering channel strain through alloying.\[^{22}\] Overall, there is every reason to believe that APAM devices can be interfaced directly with CMOS, without any transduction.

Modeling and simulation of APAM devices requires the development of new numerical tools.\[^{23}\] Most approaches for modeling silicon devices cannot readily accommodate such a high density of dopants with a sharp dopant profile due to limitations of the discretization schemes used for the underlying equations. Moreover, much of the processing relevant for APAM devices
occurs outside of the useful parameter space of most TCAD (technology computer aided design) process simulators, necessitating extending the applicability of those simulators. Lastly, at the small size-scales, strong confinement, and high current densities that APAM permits access to, quantum effects can no longer be handled semi-classically, even at room temperature. The ability to treat classical and quantum electrical transport on equal footing remains an outstanding problem, and one broadly useful outside of APAM itself.

CONCLUSION

Advancing the complexity of APAM devices and integrating APAM with CMOS will lead to a powerful tool for advancing microelectronics. At the simplest level, it creates the opportunity to explore the physical limitations of CMOS far into the future. Aside from the ramifications for device function, APAM also provides a platform for studying basic physics such as quantum effects that emerge at small size scales, and statistical number fluctuations that will dominate the behavior of few-atom systems. At a subtler level, it introduces the possibility of changing CMOS processing itself by integrating a higher density of dopants than has been created using any other approach, and at relatively late points of the workflow.

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