The motivation of this paper is to introduce a new Hebbian least mean square control algorithm for two level self-supported voltage source converter based distributed static compensator. The Hebbian least mean square controller is employed on the various aspects such as, weight updating, direct and quadrature unit voltage template, active and reactive part of reference supply currents and switching signal generation. Firstly, a set up equations using Hebbian least mean square are premeditated to compute both active and reactive weight updating. Secondly, DC and AC proportional integral controller outputs are involved with the updating weight to generate the reference supply current. The error signal obtained from both reference and actual source current is processed through the hysteresis current controller for the gate signal firing. The MATLAB/Simulink results as well as experimental results prove that the proposed algorithm is competent to afford the better voltage regulation, voltage balancing, source current harmonic reduction and power factor correction. Finally, performance obtained from the proposed controller reveals the applicability for various loading condition in the distribution grid..

1 | INTRODUCTION

In recent years, modern controlling equipments and loads are widespread due to advancement in the power distribution sector [1, 2]. The several end users like residential, commercial, industrial, irrigation, traction system, electric vehicle charging station and integration of distributed generation are the major reasons for the degradation of the grid current. The above said reasons can cause significant increase in line losses, communication interference, poor power factor, capacitor blowing, overheating and insulation failure. These causes aim to modify the power quality to end-users. Hence, a promising distributed flexible AC transmission system device distributed static compensator (DSTATCOM) is only the right solution [3, 4].

Recently, two level voltage source converter (VSC) based converters are very well-known for the three phase three wire (3P3W) distribution system. It is preferred for the sake of several advantages like lower output voltage and lower output current ripples and reduced number of power switching devices etc. [4, 5]. Several new control algorithms are designed and also, existing controllers are restructured during the last few decades [6, 7]. These are leaky least mean square, adaptive neuro-fuzzy inference system LMS algorithm, artificial neural network-based discrete-fuzzy logic, Type-1 and Type-2 fuzzy logic [8–12]. Besides these, other algorithms are LMS based NN [13], Kernel Hebbian LMS [14], LMS–LMF [15] etc. These controller algorithms show promising results for the power quality (PQ) improvement [16–19]. But the problems involved in the NN based algorithm are selection of proper size, noisy weight, inadequate number of hidden neurons and unsuitable topology of the networks. This problem becomes more complex in case of training to very small error signal.

In this paper, a new learning based Hebbian least mean square (HLMS) control algorithm is proposed and implemented by its own learning principle using mathematical equation rather than embedded systems toolbox. This suggested controller consists of six subnets. Three subnets for active and other three for reactive weight components are used to extract the fundamental component of the load current. Each subnet is constructed on the concept of biological features like input neuron, target neuron, weight correction and more attractive due to its parallel computing, learning capability behaviour. Several
factors like previous weight, normalizing weight and learning rate are involved in the HLMS weight updating rule to have better dynamic performance, less computational burden and better estimation speed.

This technique is selected for the following purposes: Such as (i) Selection of proper layer size is not required, (ii) tracking of input neurons and online learning mechanism is achieved smoothly, (iii) fast convergence characteristics and better optimized weight are obtained. The different parameters like unit voltage template, learning rate, step size, load current, previous weight are associated with weight updating equations. The weight updating equation is modelled by mathematical equation for single step size, fulfilling weight updating and normalization attributes. It provides better dynamic response to control the DSTATCOM for any variable choice of supplying and loading condition in real-time applications.

In recent years, the application of HLMS is diversified in the direction of image processing, renewable power generation, medical sciences, industrial processes etc. [20–22]. Some of the other applications of the DSTATCOM include ship power system, smart grid, micro-grid, renewable energy sources and distributed generation etc. Emulating the principle of DSTATCOM, the algorithm is proposed by interpreting weight updating rules using suitable mathematical analysis. As a result, the following objectives are attained such as: 1) voltage regulation, used to set the voltage magnitude across the DC side of the inverter; 2) voltage balancing, yield to control the PCC voltage, 3) source current harmonic reduction, provide to control the supply current, 4) power factor correction, supports to improve the power factor in between supply voltage and corresponding current.

The present section covers the overview of the case studies. The mathematical description of both ALMS and HLMS regarding the design and implementation is formulated in Section 2, whereas Section 3 explains results and discussion. In Section 4, experimental results are included to support the feasibility in the real time. An effectiveness of the proposed control strategy is summarized in Section 5. The detailed structure of distribution supply system (DSS) using mathematical developments is demonstrated in the subsequent section.

## 2 DISTRIBUTED STATIC COMPENSATOR WITH DISTRIBUTION SUPPLY SYSTEM

In this section, a typical DSTATCOM with DSS is shown in Figure 1. It contains supply system, compensator and nonlinear load. The supply and PCC voltage are represented by $v_s$ and $v_t$, respectively. Here, three phase AC supply is feeding to load comprising of 3-phase diode full bridge rectifier load containing $R_l = 10 \, \Omega$ and $L_l = 20 \, mH$. The source, load and compensator current are represented by $i_s$, $i_l$ and $i_c$, respectively. The self-supported capacitor voltage and current are represented as $v_{dc}$ and $i_{dc}$, respectively. The DSTATCOM is treated as composed of six insulated-gate bipolar transistors (IGBT) switching devices and single DC link capacitor. Simulation results are carried out in this DSS show the desired behaviour. Also, validation using experimental results is presented by considering same parameters used in simulation.

### 2.1 Topology of distributed static compensator

The DSTATCOM topology is shown in Figure 2. Here, three phase two level based VSC topology is served as DSTATCOM. Here, VSC is interfaced through the compensating impedances ($z_{ca}$, $z_{cb}$, $z_{cc}$) in parallel to the load. The dc-side voltage is kept constant and allows the VSC to feed the ac side with the adequate compensating three-phase currents ($i_{ca}$, $i_{cb}$, $i_{cc}$). Thus, the primary objective is chosen for controlling the dc-side voltage whereas secondary objective is chosen for correction of other PQ issues.
2.2 Procedures for design of control algorithm

The procedures followed in both the ALMS and proposed HLMS techniques are listed below:

a. The fundamental components of both active and reactive parts of the load current are extracted using Discrete Fourier successfully.

b. Both active and reactive updating weight of the fundamental component of the load currents are achieved using ALMS/HLMS principle.

c. Calculations of active component of reference source currents are performed.

d. Calculations of reactive component of reference source currents are done.

e. Calculation of switching signal generation obtained.

f. Besides this, one proportional integral (PI) controller to regulate the DC bus voltage and another PI controller to regulate the AC bus voltage are involved separately.

2.2.1 ALMS learning principle

The training process for the updating weighting values of fundamental active component of load current is extracted using ALMS algorithm as follows:

\[ w_{pa(n+1)} = \alpha \times \gamma \{ i_{a(n)} - w_{pa(n)}u_{pa(n)} \} a_{pa(n)} + w_{pa(n)}. \]  

(1)

\[ w_{pb(n+1)} = \alpha \times \gamma \{ i_{b(n)} - w_{pb(n)}u_{pb(n)} \} b_{pb(n)} + w_{pb(n)}. \]  

(2)

\[ w_{pc(n+1)} = \alpha \times \gamma \{ i_{c(n)} - w_{pc(n)}u_{pc(n)} \} c_{pc(n)} + w_{pc(n)}. \]  

(3)

Similarly, the updated weighting values of fundamental reactive component of load current are extracted as follows:

\[ w_{qa(n+1)} = \alpha \times \gamma \{ i_{a(n)} - w_{qa(n)}u_{qa(n)} \} a_{qa(n)} + w_{qa(n)}. \]  

(4)

\[ w_{qb(n+1)} = \alpha \times \gamma \{ i_{b(n)} - w_{qb(n)}u_{qb(n)} \} b_{qb(n)} + w_{qb(n)}. \]  

(5)

\[ w_{qc(n+1)} = \alpha \times \gamma \{ i_{c(n)} - w_{qc(n)}u_{qc(n)} \} c_{qc(n)} + w_{qc(n)}. \]  

(6)

2.2.2 Hebbian least mean square learning principle

HLMS control technique is introduced by Donald O. Hebb. It offers bootstrap training patterns for getting stable equilibrium point. The weight updation pattern that occurs in the “fire together wire together” of the network modifies the initial weight elements to a standard LMS pattern. Hebbian learning is unsupervised. LMS learning is supervised. However, a form of LMS can be constructed to perform unsupervised learning and, as such, LMS can be used in a natural way to implement Hebbian learning. This algorithm has practical engineering applications and provides insight into learning in living neural networks.

- Both the concept of LMS and Hebbian learning are utilized to perform unsupervised learning. Because of this, the precise duration between presynaptic and postsynaptic firing causes to change the synaptic weight.

- HLMS learning rule is also quite simple and intuitive. In this algorithm, each input and output pattern vector are processed the weight vector to slight change for inappropriate timing which sticks at the clustered value.

- The sigmoidal (SGM) neuron is incorporated to train the weight with bootstrap learning.

When the number of training patterns is greater than capacity, the ALMS algorithm will cause the pattern responses to cluster some near the positive stable equilibrium point and some near the negative stable equilibrium point. The error corresponding to each input pattern will be generally small but not zero. The mean square of the errors averaged over the training patterns will be minimized by HLMS. The HLMS maintains stable control and prevents saturation of the SGM weights. This HLMS is a new neuroscience based adaptive algorithm. It can be used for solution of shunt related power quality problems followed by its proper learning mechanism [21, 22]. Here, \( \alpha \) is the normalized adaptation rate, \( \gamma \) is the somatic gain, \( w_{pa(n+1)} \) and \( w_{qb(n+1)} \) are the updated active and reactive synaptive weight of phase ‘a’ respectively, \( w_{pa(n)} \) and \( w_{qa(n)} \) are the previous active and reactive synaptive weight. Similarly \( w_{pa(n)} \), \( a_{qa(n)} \) and \( i_{a(n)} \) are the independent input neurons of phase ‘a’.

The training process for the updating weighting values of fundamental active component of load current is extracted using HLMS algorithm as follows:

\[ u_{pa(n+1)} = \alpha \{ i_{a(n)} - a_{pa(n)}u_{pa(n)} \} \{ SGM (h_{pa(n)}w_{pa(n)}) \} - \gamma h_{pa(n)}u_{pa(n)} \} a_{pa(n)} + w_{pa(n)}. \]  

(7)

where

\[ h_{pa(n)}^T \] : Transpose of \( h_{pa(n)} \) and SGM = sigmoid function.

The SGM function is considered as an activation function. It is a bounded non-decreasing nonlinear and differentiable function like the logistic function or the hyperbolic tangent function. The logistic function is appropriate for response variables since it maps the output of each neuron to the interval \([-1, 1]\). If

\[ h_{pa(n)}^T \rightarrow +ve \infty, \quad SGM (h_{pa(n)}^T w_{pa(n)}) - \gamma h_{pa(n)}^T w_{pa(n)} = 1. \]  

(8)

and

\[ h_{pa(n)}^T \rightarrow -ve \infty, \quad SGM (h_{pa(n)}^T w_{pa(n)}) - \gamma h_{pa(n)}^T w_{pa(n)} = -1. \]  

(9)
So it can be regarded as activation function whose limit lies in between −1 to 1.

\[ w_{pb}(n+1) = \alpha \{ i_{pb}(n) - u_{pb}(n)w_{pb}(n) \} \{ \text{SGM} (u_{pb}^T w_{pb}(n)) - \gamma u_{pb}^T w_{pb}(n) \} u_{pb}(n) + w_{pb}(n). \]  

(10)

\[ w_{pc}(n+1) = \alpha \{ i_{pc}(n) - u_{pc}(n)w_{pc}(n) \} \{ \text{SGM} (u_{pc}^T w_{pc}(n)) - \gamma u_{pc}^T w_{pc}(n) \} u_{pc}(n) + w_{pc}(n). \]  

(11)

Similarly, the updated weighting values of fundamental reactive component of load current are extracted as follows:

\[ w_{qa}(n+1) = \alpha \{ i_{qa}(n) - u_{qa}(n)w_{qa}(n) \} \{ \text{SGM} (u_{qa}^T w_{qa}(n)) - \gamma u_{qa}^T w_{qa}(n) \} u_{qa}(n) + w_{qa}(n). \]  

(12)

\[ w_{qb}(n+1) = \alpha \{ i_{qb}(n) - u_{qb}(n)w_{qb}(n) \} \{ \text{SGM} (u_{qb}^T w_{qb}(n)) - \gamma u_{qb}^T w_{qb}(n) \} u_{qb}(n) + w_{qb}(n). \]  

(13)

\[ w_{qc}(n+1) = \alpha \{ i_{qc}(n) - u_{qc}(n)w_{qc}(n) \} \{ \text{SGM} (u_{qc}^T w_{qc}(n)) - \gamma u_{qc}^T w_{qc}(n) \} u_{qc}(n) + w_{qc}(n). \]  

(14)

The mean values of weighting values \((w_r)\) of a, b and c-phase is calculated as follows:

\[ w_p = \frac{w_{pa}(n+1) + w_{pb}(n+1) + w_{pc}(n+1)}{3}. \]  

(15)

Similarly, the mean values of weighting values \((w_q)\) of a, b and c-phase is calculated as follows

\[ w_q = \frac{w_{qa}(n+1) + w_{qb}(n+1) + w_{qc}(n+1)}{3}. \]  

(16)

### 2.3 Computation of in-phase and quadrature unit voltage template

The in-phase unit voltage templates \((u_{pa}, u_{pb}, u_{pc})\) are the relation of phase voltages & amplitude of PCC voltage \((v_t)\) estimated as follows

\[ u_{pa} = \frac{v_{pa}}{v_t}, \quad u_{pb} = \frac{v_{pb}}{v_t}, \quad u_{pc} = \frac{v_{pc}}{v_t}. \]  

(17)

The quadrature unit voltage templates \((u_{qa}, u_{qb}, u_{qc})\) are the relation of phase voltages as follows

\[ u_{qa} = \frac{u_{pb} + u_{pc}}{\sqrt{3}}, \quad u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}, \quad u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}. \]  

(18)

where \(r_i\) can be expressed as

\[ r_i = \sqrt{2 \left( r_{a_i}^2 + r_{b_i}^2 + r_{c_i}^2 \right)}. \]  

(19)

### 2.4 Calculation of active part of reference source currents

The error in dc voltage \((r_{dc})\) is calculated by subtracting sensed dc voltage from reference dc voltage and it is expressed as

\[ r_{dc} = r_{dc\ (ref)} - r_{dc}. \]  

(20)

This difference is processed through the proportional-integral (PI) controller to control the constant dc bus voltage. The output of PI controller can be expressed as

\[ w_{cp} = k_{pa} r_{dc} + k_{ia} \int r_{dc} dt. \]  

(21)

The total active component of the reference source current is calculated by adding the PI controller output with the average magnitude of active component of load currents. It is expressed as

\[ w_{cp} = w_p + w_{cp}. \]  

(22)

### 2.5 Determination of reactive component of reference source currents

The difference in between reference ac voltage and sensed amplitude of ac bus voltage is the error in ac voltage \((r_{ac})\) can be expressed as

\[ r_{ac} = r_{ac\ (ref)} - r_{ac}. \]  

(23)

This difference is processed through the PI controller to maintain the constant ac bus voltage. The output of PI controller can be expressed as

\[ w_{cq} = k_{pr} r_{ac} + k_{ir} \int r_{ac} dt. \]  

(24)

The difference between output of PI controller and the average magnitude of reactive component of load currents is the total reactive components of the reference source current can be expressed as;

\[ w_{eq} = w_q - w_{eq}. \]  

(25)

### 2.6 Estimation of switching signal generation

Three phase instantaneous reference source active component are estimated by multiplying in phase unit voltage template
and active power current component and these are obtained as

$$i_{aa} = w_{sp} u_{pa}, \quad i_{ab} = w_{sp} u_{pb}, \quad i_{ac} = w_{sp} u_{pc}. \quad (26)$$

Similarly, three phase instantaneous reference source reactive component are estimated by multiplying quadrature unit voltage template and reactive current component and these are obtained as

$$i_{ra} = w_{sq} u_{qa}, \quad i_{rb} = w_{sq} u_{qb}, \quad i_{rc} = w_{sq} u_{qc}. \quad (27)$$

The summation of active and reactive components of current is called as reference source currents and these are obtained as

$$i_{sa}^* = i_{aa} + i_{ra}, \quad i_{sb}^* = i_{ab} + i_{rb}, \quad i_{sc}^* = i_{ac} + i_{rc}. \quad (28)$$

Both the actual source currents ($i_{sa}, i_{sb}, i_{sc}$) and the reference source currents ($i_{sa}^*, i_{sb}^*, i_{sc}^*$) of the respective phases are compared then current error signals are fed to a hysteresis current controllers. Their outputs are used to feed the IGBTs $T_1$ to $T_6$ of the VSC served as a DSTATCOM.

Using mathematical analysis, the simulation results obtained from both the controllers under the different event of loading are presented in Section 3.

### 3 | SIMULATION RESULTS AND DISCUSSION

This section describes the comparative results between ALMS and HLMS algorithm in terms of various PQ issues. The performance of both algorithms is simulated using MATLAB/Simulink and sim power system toolboxes in discrete time are discussed below.

#### 3.1 | Performance of ALMS algorithm

The system performance including DSTATCOM using ALMS technique is presented in this section. The different aspects related to power quality improvement are presented separately like (i) voltage regulation, (ii) voltage balancing, (iii) harmonic reduction, (iv) power factor improvement, (v) reactive power exchange and (vi) reduction in sizing of VSC etc.

#### 3.1.1 | Constant loading

The study under the constant loading throughout the time of simulation is considered for the balanced loading.

The subplots like supply voltage ($v_s$), load current ($i_l$), source current ($i_s$), compensator current ($i_{ca}, i_{cb}, i_{cc}$) and respective input voltage ($v_{dc}$) are arranged on the common plot, as shown in the Figure 2(i).

It is noted that this control algorithm provides the input power factor (p.f) 0.96 causing p.f corrections as shown in the Figure 2(ii), whereas the load side p.f between phase 'a' voltage and corresponding current is 0.87. The magnitude of the source current is 55.88 A and THD of the source current is 4.62%. The magnitude of the load current is 53.54A, and THD of the load current is 26.84%. The desired dc-link voltage of 600 V is maintained as constant by injecting the satisfactory compensating currents satisfying the voltage regulation. It is also observed that the magnitude of PCC voltage is regulated at the reference value of 318 V under constant loading, satisfying the voltage balancing.

#### 3.1.2 | Variable loading

The variable loading is considered between 0.6 and 0.7 s. At the same instant of time, phase ‘a’ load is released. The subplots like supply voltage ($v_s$), load current ($i_l$), source current ($i_s$), compensator current ($i_{ca}, i_{cb}, i_{cc}$) and respective input voltage ($v_{dc}$) are arranged on the common plot, which is presented in the Figure 3(i).

It is noted, this control algorithm provides the input p.f 0.897 causing p.f correction, as shown in the Figure 3(ii),
whereas the load side p.f between of phase ‘a’ voltage and corresponding current is 0.86. The magnitude of the source current is 50.58 A and THD of source current is 4.9%. The magnitude of the load current is 42.96 A and THD of load current is 26.34%.

The desired dc-link voltage of 670 V is maintained as constant by injecting the satisfactory compensating currents satisfying the voltage regulation. It is also observed that the magnitude of PCC voltage is regulated at the reference value of 317 V even if subjected to the load variation, satisfying the voltage balancing.

3.2 | Performance of Hebbian least mean square algorithm

3.2.1 | Constant loading

The subplots like supply voltage (v_s), load current (i_l), source current (i_s), compensator current (i_ca, i_cb, i_cc) and respective input voltage (v_dc) are arranged on the common plot, which is presented in the Figure 4(i). It is noted that the control algorithm delivers excellent result and the input p.f is found to be 0.98 causing a significant improvement in power factor correction which is shown in the Figure 4(ii) whereas the load side p.f between of phase ‘a’ voltage and corresponding current is 0.91. The magnitude of the source current is 54.06 A and THD of source current is 4.06%. The magnitude of the load current is 53.96 A and THD of load current is 26.04%. The desired dc-link voltage of 535 V is maintained constant by injecting the satisfactory compensating currents satisfying the voltage regulation. It is also observed that the magnitude of PCC voltage is regulated at the reference value of 320 V under constant loading, satisfying the voltage balancing.

3.2.2 | Variable loading

The subplots like supply voltage (v_s), load current (i_l), source current (i_s), compensator current (i_ca, i_cb, i_cc) and respective input voltage (v_dc) are arranged on the common plot, which is illustrated in the Figure 5(i).

It is noted that the control algorithm delivers excellent result and the input p.f is found to be 0.96 causing significant improvement in p.f corrections. The magnitude of the source current is 51.2 A and THD of the source current is 4.87%. The magnitude of the load current is 43.64 A and THD of the load current is 25.02%. The input p.f is found to be 0.94, proved that the control algorithm performs satisfactorily and it is shown in the Figure 5(ii), whereas the load side p.f between of phase ‘a’ voltage and corresponding current is 0.89. The desired dc-link voltage of 586 V is maintained constant by injecting the
TABLE 1  Performance comparison of ALMS and HLMS

| Algorithm | i/p power factor (p. f) | THD (%) of $i_s$, Case-i | THD (%) of $i_s$, Case-ii | THD (%) of $i_l$, Case-i | THD (%) of $i_l$, Case-ii |
|-----------|-------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| ALMS      | 0.96                    | 55.88, 4.62              | 50.5, 4.91               | 53.54, 26.84             | 42.96, 26.34             |
| HLMS      | 0.98                    | 54.62, 4.06              | 51.2, 4.87               | 53.40, 25.82             | 43.64, 25.02             |

FIGURE 6  DC-link voltage using both ALMS and Hebbian least mean square controller under (i) constant loading and (ii) variable loading

satisfactory compensating currents satisfying the voltage regulation. It is also observed that the magnitude of PCC voltage is regulated at the reference value of 320 V even if subjected to the load variation, satisfying the voltage balancing. With these observations, this algorithm can be regarded as the comparatively better solution for this present scenario.

Apart from the above analysis, an important comparison is made in between the two algorithms to show dc-link voltage under various loading conditions. In the proposed method, comparative results like input p.f, THD% of both the source current, as well as, load current are presented in the Table 1. The dc link voltage should be greater than or equal to $\sqrt{6}$ times the phase voltage of the system for distortion free compensation. Hence the range of the dc link voltage for a phase voltage of 230 V is $\sqrt{6} \times 230 \pm 10\% = 507.05V < v_{dc} < 619.71$ V. The dc-link voltage oscillation during unbalanced condition is found to be between 535 and 586 V whereas it is 600–660 V in the ALMS control technique and is shown in the Figure 6(i),(ii). The other benefits such as less capacitor stress, reduced rating of VSC and low power consumption is the major contribution of the proposed control method are presented in the Table 2. From the comparison, it can be observed that the HLMS control technique provides a less harmonic content in the source current with a significant reduction in the dc-link voltage.

As, the power rating of DSTATCOM is calculated by

$$kVA = \frac{\sqrt{3} v_{dc} i_l}{\sqrt{2}}$$  \hspace{1cm} (29)

So reduced rating of VSC, less capacitor stress and less stored energy can be obtained using the proposed method. The choice of reduced dc-link voltage is considered and helps in choosing the reduction of VSC sizing. Furthermore, less stress across the semiconductor switching devices, lower switching power loss due to low switching frequency, lower costs, better performance and higher efficiency can be achieved. Apart from these, this suggested algorithm is capable enough for the detection, measurement and monitoring of the signal attributes like amplitude, power factor and frequency and performs smooth operation among analog components and digital signal processor simultaneously in the real time application. This technique is selected in view of better speed processing, less memory requirement, accuracy and power quality, responsive and easier to implement in the practical application due to parallel computing nature and adapted to system dynamic features. In order to validate the effectiveness of the controllers, the experimental results are presented in Section 4.

4  | EXPERIMENTAL RESULTS AND DISCUSSION

A 3P3W prototype DSTATCOM is developed in the laboratory to verify the practicability of both ALMS as well as HLMS controller and shown in Figure 7. The parameters used in experimental setup are the same as that described in Table 3 for simulations. The DSTATCOM involves an IGBT based SEMIKRON (MD B6I 600/415-30F) inverter assembled with required DC-supply and other accessories. Voltages and currents from various parts of the system are sensed using hall-effect voltage transducer LEM LV25-P, current transducer LA55-P, current probes (A622) and voltage probes (RP1050D). The dSPACE module DS1104 used along
TABLE 2  Comparative study of VSC rating

| Algorithm | $v_{dc} \text{ \text{V}}$ | $p_{loss} \text{ \text{W}}$ | Rating of VSC $\text{kVA}$ |
|----------|----------------|----------------|----------------|
| ALMS     | Case-i: 600 | Case-i: 119.82 | Case-i: 9.288 |
|          | Case-ii: 670 | Case-ii: 125.5827 | Case-ii: 10.372 |
| HLMS     | Case-i: 535 | Case-i: 106.56 | Case-i: 7.810 |
|          | Case-ii: 586 | Case-ii: 109.80 | Case-ii: 8.648 |

TABLE 3  Simulation and experimental parameter

| Grid     | Load                                      | Controller                      | VSC                        |
|----------|-------------------------------------------|---------------------------------|----------------------------|
| $r_s = 230 \text{ V (L-N)}$ | $3\Phi$ diode bridge  | $\alpha = 0.4$ | $C_{dc} = 2000 \text{ \mu F}$ |
| $f_s = 50 \text{ Hz}$     | rectifier with RL  | $\gamma = 0.01$ | $R_s = 0.25 \Omega$ |
| $R_s = 0.04 \Omega$      | load:                      | $v_{dc(\text{ref})} = 600 \text{ V}$ | $I_s = 1.5 \text{ mA}$ |
| $L_s = 2 \text{ mH}$     | $R_l = 10 \Omega$          | $v_{i(\text{ref})} = 325 \text{ V}$ | $f_{sw} = 10 \text{ kHz}$ |
| $L_{dc} = 20 \text{ mH}$ | $I_{l} = 10 \Omega$        | $k_p = 0.7$               |

with MATLAB2014a/Simulink and connector panel module CP1104 for analog feedback signal are used to implement the proposed control algorithm. Power analyzer Yokogawa (WT 500) is used for capturing and recording of the waveforms. The supply voltage and load current are tracked through the dSPACE 1104 panel via DAC (digital to Analog converter) channel. The use of all 14 ADC channels at a time may be problematic because of high acquisition delays of the processor’s core. Here, sampling time of 20 $\mu$s is chosen to achieve due to simple and efficient algorithm. The voltage balancing, source current harmonic reduction, p.f improvement, voltage regulation and reduced rating of the VSC are analysed by dSPACE 1104 real-time controller. The load current, source current and compensating current for ALMS & HLMS controller under both the constant and diversity loading conditions depicted in Figure 8(i),(ii), respectively. From these figures, it is observed that input p.f is 0.94 and 0.87, respectively. Similarly, the load current, source current and compensating current are also analysed using HLMS technique based DSTATCOM which are presented in Figure 9(i),(ii), respectively. It is found that input p.f is 0.96 and 0.93 for both the constant and diversity, respectively.

The comparative study of voltage across the capacitor is presented in Figure 10(i),(ii), respectively. The DC bus voltage is regulated at 600 and 670 V balanced and unbalanced conditions respectively under ALMS technique whereas the DC bus voltage is regulated at 535 and 586 V balanced and unbalanced conditions under HLMS techniq. The source current harmonics is reduced to 4.62% and 4.91% using ALMS whereas the source current harmonics is reduced to 4.06% and 4.87% using HLMS technique correspond to balanced and unbalanced condition as shown in the Table 4. The experimental results are in close agreement with the simulation results and so confirm the better performance of the HLMS technique for DSTATCOM. It can be expected that the proposed controller will perform better under any possibility loading condition. Moreover, this feasible solution can be selected for the integrated operation in the distribution system as per IEEE519 standards. Finally, the achieved goals are possessed the better impact on selection of the proposed control algorithm, which are summarized in the Section 5.

TABLE 4  Experimental performance comparison of ALMS and Hebbian least mean square

| Algorithm | i/p power factor (p.f) | Mag (A), THD (%) of $i_s$ | Mag (A), THD (%) of $i_l$ |
|----------|----------------|----------------|----------------|
|          | Case-i | Case-ii | Case-i | Case-ii | Case-i | Case-ii |
| ALMS     | 0.94   | 0.87   | 55.88, 4.62 | 50.5, 4.91 | 53.54, 26.84 | 42.96, 26.34 |
| HLMS     | 0.96   | 0.93   | 54.62, 4.06 | 51.2, 4.87 | 53.40, 25.82 | 43.64, 25.02 |
FIGURE 8  Load current, source current and compensator current using ALMS controller under (i) constant loading and (ii) variable loading

FIGURE 9  Load current, source current and compensator current using Hebbian least mean square controller under (i) constant loading and (ii) variable loading

5  CONCLUSION

A comparative assessment of DSTATCOM using both ALMS and HLMS control techniques for 3P3W distribution system is presented in this paper. The proposed algorithm provides better remedial solutions, which are listed below:

- Harmonic reduction of source current is maintained less than 5% as per the benchmark value of IEEE-519 grid code.
- Balancing of three-phase source voltage and current are accomplished successfully.
- Reduced dc-link voltage of VSC is retained.
- DSTATCOM rating is reduced from 9.288 to 7.810 kVA (nearly 81.08%) using proposed control technique.

With these presented design scenarios, the proposed controller can be implemented by the industry for the distribution system are the major requirements.

REFERENCES

1. Luo, A., et al.: Distribution static compensator based on an improved direct power control strategy. IET Power Electron. 7(4), 957–964 (2014)
2. Herman, L., Papic, I., Blazic, B.: A proportional-resonant current controller for selective harmonic compensation in a hybrid active power filter. IEEE Trans. Power Delivery. 29(5), 2055–2065 (2014)
3. Manoj Kumar, M.V., Mishra, M.K.: Three-leg inverter based distribution static compensator topology for compensating unbalanced and non-linear loads. IET Power Electron. 8(11), 2076–2084 (2015)
4. Luo, A., Xiao, H., Shuai, Z.: Double deadbeat-loop control method for distribution static compensator. IET Power Electron. 8(7), 1104–1110 (2015)
5. Venkatraman, K., Selvan, M.P., Moorthi, S.: Predictive current control of distribution static compensator for load compensation in distribution system. IET Generation. Transmission & Distribution. 10(10), 2410–2423 (2016)
6. Singh, B., et al.: Comprehensive study of DSTATCOM configurations. IEEE Trans. Ind. Inf. 10(2), 854–870 (2014)
7. Barghi Latran, M., Teke, A., Yoldas, Y.: Mitigation of power quality problems using distribution static synchronous compensator: A comprehensive review. IET Power Electron. 8(7), 1312–1328 (2015)
8. Arya, S.R., Singh, B.: Performance of DSTATCOM using leaky LMS control algorithm. IEEE Journal of Emerging and Selected Topics in Power Electronics. 1(2), 104–113 (2013)
9. Badoni, M., Singh, A., Singh, B.: Adaptive neurofuzzy inference system least-mean-square-based control algorithm for DSTATCOM. IEEE Trans. Ind. Inf. 12(2), 483–492 (2016)
10. Juang, J.G., Chien, L.H., Lin, F.: Automatic landing control system design using adaptive neural network and its hardware realization. IEEE Syst. Journal. 5(2), 266–277 (2011)
11. Saribulut, L., Teke, A., Tumay, M.: Artificial neural network-based discrete-fuzzy logic controlled active power filter. IET Power Electron. 7(6), 1536–1546 (2014)
12. Mangaraj, M., et al.: An adaptive LMBP training based control technique for DSTATCOM. IET Generation. Transmission and Distribution. 14(5), 516–524 (2020)
13. Agarwal, R.K., Hussain, I., Singh, B.: Application of LMS-based NN structure for power quality enhancement in a distribution network under abnormal conditions. IEEE Trans. Neural Networks and Learning Systems. 29(5), 1598–1607 (2018)
14. Mangaraj, M., Panda, A.K.: Modeling and simulation of KHLMS algorithm-based DSTATCOM. IET Power Electron. 12(9), 2304–2311 (2019)
15. Srinivas, M., Hassain, I., Singh, B.: Combined LMS–LMF based control algorithm of DSTATCOM for power quality enhancement in distribution system. IEEE Trans. Ind. Electron. 63(7), 4160–4168 (2016)
16. Mangaraj, M., Panda, A.K.: NBP-based icos control strategy for DSTATCOM. IET Power Electron. 10(12), 1617–1625 (2017)
17. Kumar, P., Mahajan, A.: Soft computing techniques for the control of an active power filter. IEEE Trans. Power Delivery. 24(1), 452–461 (2009)
18. Mangaraj, M., Panda, A.K., Penthia, T.: Investigating the performance of DSTATCOM using ADALINE based LMS algorithm. 2016 IEEE 6th International Conference on Power Systems (ICPS), New Delhi, pp. 1–5 (2016)
19. Mangaraj, M., Panda, A.K.: Performance analysis of DSTATCOM employing various control algorithms. IET Generation. Transmission & Distribution. 11(10), 2643–2653 (2017)
20. Widrow, B., Kim, Y., Park, D.: The Hebbian-LMS learning algorithm. IEEE Comput. Intell. Magazine. 10(4), 37–53 (2015)
21. Siri, B., et al.: A mathematical analysis of the effects of Hebbian learning rules on the dynamics and structure of discrete-time random recurrent neural networks. International Journal of Neural Comput. 20(12), 2937–2966 (2008)
22. Pehlevan, C., Hu, T., Chklovskii, D.B.: A Hebbian/anti-Hebbian neural network for linear subspace learning: A derivation from multidimensional scaling of streaming data. International Journal of Neural Comput. 27(7), 1461–1495 (2015)

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