A low power and glitch-free circular rotation phase modulator for outphasing transmitter

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Abstract: This paper proposes an energy-efficient and glitch-free digital phase modulator for outphasing transmitter. The proposed modulator uses a path-shared tapped delay line (TDL) and a dynamical pseudo clock-gating control technique. These approaches lead a 64\% lower power consumption compared conventional digital control delay lines (DCDLs). Moreover, the proposed modulator achieves circular rotational phase modulation, resulting a system EVM of \(-36.93\) dB and ACLR of \(-50.96\) dBc without extra shaping circuits or analog filters. The prototype modulator was fabricated in 130 nm CMOS process with an active area of 0.134 mm\(^2\). Operating under 40 MHz frequency with 1.2 V power supply, the proposed modulator consumes total power of 450 \(\mu\)W. In addition, this chip achieves an 80 ps coarse resolution with 4.7 ps RMS error and a minimum phase resolution of 0.96 ps.

Keywords: lower power, glitch-free, PM, digital transmitter

Classification: Integrated circuits

References

[1] E. Roverato, et al.: “All-digital LTE SAW-less transmitter with DSP-based programming of RX-band noise,” IEEE J. Solid-State Circuits 52 (2017) 3434 (DOI: 10.1109/JSSC.2017.2761781).

[2] M. Kosunen, et al.: “A 0.35-to-2.6 GHz multilevel outphasing transmitter with a digital interpolating phase modulator enabling up to 400 MHz instantaneous bandwidth,” ISSCC Dig. Tech. Papers (2017) 224 (DOI: 10.1109/ISSCC.2017.7870342).

[3] T. W. Chen, et al.: “A sub-mW all-digital signal component separator with branch mismatch compensation for OFDM LINC transmitters,” IEEE J. Solid-State Circuits 46 (2011) 2514 (DOI: 10.1109/JSSC.2011.2164133).

[4] A. Ravi, et al.: “A 2.4-GHz 20–40-MHz channel WLAN digital outphasing transmitter utilizing a delay-based wideband phase modulator in 32-nm CMOS,” IEEE J. Solid-State Circuits 47 (2012) 3184 (DOI: 10.1109/JSSC.2011.2164133).
1 Introduction

Digital outphasing transmitter with switch-mode power amplifier (SMPA) [1, 2, 3] have recently become a focus of research and development activity due to its less circuit complexity and lower power consumption [2, 3, 4, 5, 6]. Phase modulator (PM), as an essential part of outphasing transmitters, has been widely discussed by many researchers [2, 3, 4, 5, 6, 7, 8, 9, 10]. The author in [2] propose a sub-mW achievement with simple power-of-two structure. However, unnecessary inverse leads into power dissipation and the asynchronous control causes pulse-shortening problem. To reduce power overhead, implementation in [10] employs a continuous locking scheme. Although this approach minimize power consumption by gating the un-working path, it still suffers from glitch and pulse-shortening problems. To address these issues, authors in [4, 5, 7, 11] present alternative options. Infinite delay modulation proposed in [4, 5, 7] is an efficient scheme. Unfortunately, in this implementation, the modulated square signal cannot reconstruct the zero crossing points of ideal modulated sinusoidal signal [2]. This deviation would result severe adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM) degradation. NAND-based topology presented in [11] is another fascinating way to remove glitches without intricate circuits design. However, in this structure, six NAND gates compose one delay element with a $2T_{\text{NAND}}$ resolution, which is too large to satisfy communication requirements. To achieve desirable performances, interpolating phase modulator is presented in [2]. However, four DTCs are needed to achieve one phase, that is complex and power consumption. The disadvantages mentioned before have limited their application on all-digital transmitter systems.
especially lower power systems such as NB-IoT, LoRa and WPANs, which have drawn much attention from both academia and industry in recent years.

In this paper, we propose a simple lower power and glitch-free phase modulator with circular rotation phase shift. The proposed modulator employs shared TDL to achieve coarse phase modulation for saving power, and it adopts a stage-by-stage clock-gating topology to address glitch issue. In addition, digital-control varactors (DCVs) are used to realize ps-level resolution to meet communication requirement. Moreover, different from conventional infinite delay modulations [4, 5, 7], this design has ability of rotation phase shift, which is the key to a desirable system performance. The proposed modulator is realized in a 130 nm CMOS process, achieving a 450 µw total power consumption and 0.96 ps phase resolution under 1.2 V power supply. The proposed modulator shows potential on both lower power narrow-band and wide-band systems.

2 Proposed phase modulator

Fig. 1 shows the architectures of the proposed energy-efficient glitch-free PM. It consists of six major blocks: TDL.cell, TDL.controller, phase detector (PD), DLL.controller, digitally-control delay line (DCDL) and CDC circuits.

The PD [3] and DLL.Controller are adopted together to constitute all digital delay lock loop (ADDLL) for locking the eight stages TDL [4] to half of one LO period. Therefore, each TDL.Cell represents a 22.5° phase step. In addition, two paths of outphasing transmitter share the TDL stage, which is much more power saving than conventional implementations. The TDL.Controller is working as a glitch-free phase multiplexer for picking out the taps of TDL to achieve coarse phase modulation. Then, further delay of the residual phase is implemented by the 15-bit digital-control-delay-line (DCDL) for accuracy. The TDL.Cell and DCDL have the similar structures as employed in [3]. The coarse stage uses power-of-two architecture, and the fine stage uses digital controlled varactors (DCVs). The CDC circuits is a copy the constant delay of TDL and DCDL, which is used for circular rotation phase modulation.

Fig. 1. Overall structures of the proposed phase modulator
The proposed modulator achieves circular phase shift instead of infinite delay modulation as traditional implementation. To demonstrate the difference, a timing diagram comparison between them is shown in Fig. 2. In infinite delay process, phase information is corresponding to the duration of low logic. In this way, each time the phase greater than π, there will be distortions in the current period and the next period, as period3 and period4 show in Fig. 2(a) [2]. Period3 has a smaller duty-cycle than 50% while period4 has a greater one larger than 50%. In this way, the square carrier cannot ideally reconstruct zero crossing points of a modulated sinusoidal waveform [2]. That leads serious signal distortion, to address this issue, extra technique such as sigma delta modulation or high-order filter have to be used, which is complex and power consumption. While for the proposed modulation, as illustrated in Fig. 2(b), modulated square signal exhibits ideal zeros crossing points. That results excellent signal quality, which significantly relaxes the performance requirement of other complex analog circuits.

![Fig. 2. Timing diagrams comparison](image)

3 Implementation of key building blocks

3.1 DCDL and CDC

The TDL_Cell and DCDL have same structures as Fig. 3 shows. The coarse stage is implemented by a power-of-two based architecture, which is simple and power saving. But unlike conventional methods, in the presented architecture, additional AND gates are adopted in each stage to close inactive path to minimize dynamical inversion power, as shown in Fig. 3(a). However, due to asynchronous control property, the AND-gates will produce unpredictable glitches. In addition, it suffer pulse-shortening issue [4]. To solve these problems, a clock-gating topology is proposed. As illustrated in Fig. 3(a), a data flip-flop (DFF) is added in each stage to conform the control code changes before positive edges instead of with them. This determine-before-break operation has effectively avoided glitches and maintained duty-cycle. The fine stage and extra stage employs DCV to achieve required phase resolution. In this approach, each delay stage consists of an inverter driving a 5-bit
binary weighted bank of small switched capacitors. The proposed DCV adopts a 5-bit extra code in the final stage to achieve admirable resolution while using same control code in the first four stages to keep linearity. System simulations show that the resulting DCV resolution and INL are sufficient small to satisfy any current communication standard requirements.

Due to the constant delay caused by MUX cells in the power-of-two schemes [3, 10, 11], the 0° phase is always indicated by the constant delayed signal instead of the original input signal. Therefore, a CDC circuit is proposed to get relative 0° phase for determining the changing time of the enable signals, which is essential for the circular phase shift.

The structure of the proposed CDC is shown in Fig. 4, which is a copy of the constant parts of delay line (TDL.Cells and DCDL). However, even though the same gates in delay line have already copied the major delay, the minute deviation between them caused by placement and route cannot be copied accurately. In order to ensure the accuracy, the CDC circuit is configurable. The clk.cdc and clk.out, as shown in Fig. 3, would be locked by ADDLL to generate constant control codes for CDC or the delay line.

3.2 TDL_Controller for glitch-free process

The structures and timing diagram to describe the glitch-free implementation of TDL_Controller are illustrated in Fig. 5. The 3-bit MSB is firstly transformed to eight enable control codes, which are self-retimed by the negative edge of each tap.
signal (like \( tdl0 \)) from TDL.Cells to provide glitch-free operations and achieve dynamical tap selections. As the timing diagram shows, the enable signals always change before the positive edge, which sufficiently avoids glitches.

3.3 Circular rotation phase modulation

Fig. 6 shows a detailed timing scheme of proposed circular phase shift modulation. When the modulating phase is belong to \([0, \pi]\), as the left trace shows in Fig. 6, the enable signal \( en \) keeps high. As a result, \( clk_{out} \) is as same as \( clk_{mod} \). When the phase \( \phi \) greater than \( \pi (5 \times \pi/4) \), the input signal firstly delay by phase \( \phi-\pi (\pi/4) \), as \( clk_{mod} \) shows in Fig. 6. Then, the residue phase \( \pi \) will be achieved by inverting \( clk_{mod} \) with the control signal \( en \), which is controlled by \( clk_{cdc} \). Thereby, the rotational modulated signal is achieved. A prospective benefit from this process is coverage reduction. As the modulating phase is always mapped to \([0, \pi]\), only half LO coverage is required in the proposed modulator. That is the reason why each tap only with 22.5° phase step instead 45° as traditional implementation dose [4].

The proposed circular rotation phase modulator was simulated in 130nm CMOS technology with 8-bit control codes (not including DCVs). Note that, with circular rotation phase shift, the 8-bit delay line can achieve maximum control code of 512. In addition, for fair comparisons, conventional structure in [3] and the AND-gated architecture in [10] were also designed and simulated in the same condition. As shown in Fig. 7(a), both the conventional and the AND-gated structures suffer from pulse-shortening issues, moreover, AND-gated modulator generates glitches when control code trenchantly switches. For the proposed modulation, the shorter pulse is reappeared and unanticipated glitches are eliminated. Fig. 7(b) shows the power consumption comparisons of all these modulators. The proposed modulator shows slight inferiority during the former half of control codes compared with the AND-gated only structure due to extra DFFs and
CDC circuits. However, it shows a prominent superiority when the control code is greater than 256, profiting from circular rotation modulation. The propose modulator achieves a maximum power of 136 µW and average power consumption of 86 µW, 64% improvement compare with 240 µW in traditional implementation [3].

4 Measurement results

The proposed phase modulator was fabricated in a 130 nm CMOS process. The die microphotograph of the chip is shown in Fig. 8. The active area is 670 µm × 210 µm. The designed phase modulator was tested with a 1.2 V supply voltage and a 40 MHz frequency. Under this condition, this chip consumes total power of 450 µW, including digital logic and SPI test circuits.
To verify linearity of the proposed modulator, the output was captured with a 100 GS/s oscilloscope with sweeping control code. Fig. 9(a) shows the measured transfer function of coarse stage. Operating at 40 MHz, the coarse-tune provide an additional maximum delay of 40.98 ns with a constant delay of 4.26 ns. Fig. 9(b) shows the differential nonlinearity (DNL) of the coarse-tune. The maximum DNL is $13/−8.8\text{ps}$ ($+0.187°/−0.127°$), and is sufficient to drive no matter narrow band or wide-band (40 MHz) signals [4]. Fig. 10 shows output delay with different codes of fine stage and the extra stage. The average resolutions of each stage were 5.98 ps and 0.96 ps, respectively. The minimum resolution provide by extra stage implied a 0.83° phase adjustment capability for even 2.4 GHz signal, which is competent to meet wide-band system requirements, such as WIFI specifications [4].

![Fig. 9. Measured results of coarse stage (a) Delay transfer function (b) DNL errors](image)

![Fig. 10. Output delay of fine stage and extra stage](image)

Fig. 11 shows the measured output waveform example when the control code represents a 180° phase. The average delay difference of original and the delayed signal is 12.51 ns, which is close enough to the ideal value 12.5 ns. Fig. 12 shows the output waveforms of the delay line with 0 control codes (only constant delay) and the CDC circuits. They have almost synchronized rising edge with assistant of phase detector.

Moreover, to validate the performances of the outphasing behaviors with the proposed modulator, the characteristics of the measured output waveform was fed
back to MATLAB. With an 802.15.4g 16 QAM OFDM signal, the proposed phase modulator achieves $-36.93$ dB EVM and $-50.96$ dBc ACLR. The realization in [4], which is infinite delay modulation, was also simulated with same characteristics. The EVM and ACLR were $-27.17$ dB and $-36.92$ dBc, respectively.

Table I compares the performance of the proposed phase modulator with prior implementations. Our work is the most energy-efficient when compared with other works, benefiting from the path-shared and clock-gating structures. The power consumptions of [2] and [7] shown in Table I only contain the modulator and digital logic instead of total power for fair comparisons. Meanwhile, with 40.98 ns phase coverage and 0.96 ps phase resolution, the proposed modulator has ability to handle carrier frequency from 25 MHz to 2.4 GHz, which is sufficient for current communication specifications. Different from conventional infinite delay phase modulation, the proposed circular rotation modulation achieves comparable EVM and ACLR of $-36.93$ dB and $-50.96$ dBc respectively, without extra sigma-delta modulation or complex filters. This high performance signals sufficiently reduces the design challenges of PA and avoids high-Q and high-order filter requirements.
5 Conclusion

This paper presents a delay-based lower power and glitch-free rotation shift phase modulator for digital outphasing transmitters. The proposed modulator employs a path-shared structure and AND-gated control scheme to avoid unnecessary power consumption. And it uses the self-retimed technique to achieve glitch-free phase selection. In addition, the proposed modulator has ability of circular phase shift, achieving complete LO range with only half coverage. This leads into 64% power consumption reduction compared with previous works. Meanwhile, the proposed modulator achieves 0.96 ps phase resolution, making it capable to process RF signals. Moreover, with circular rotation phase modulation and an admirable phase resolution, the proposed modulation achieves an EVM of $-36.93$ dB and ACLR of $-50.96$ dBc, easily to satisfy current communication standard requirements. As a consequense, the proposed lower power phase modulator shows a prospectively potential for current digital transmitters.

Acknowledgments

This work was supported in part by National Natural Science Foundation of China (Grant No.: 61474135) and Youth Innovation Promotion Association of the Chinese Academy of Sciences (Member No.: 2015102).