Area-optimized design of SOT-MRAM

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Abstract In this letter, we present a new structure of spin-orbit torque magnetic random access memory (SOT-MRAM) for area optimization. Based on the observation of SOT-MRAM layout that the metal line can be added in the horizontal direction without increasing the cell area, the proposed design optimizes the metal line routing direction as well as biasing conditions for read and write operations. Implemented with a 45-nm CMOS technology, the proposed design achieves cell area reduction of 42\% (23\%) compared with the conventional SOT-MRAM (STT-MRAM). The proposed design achieves 6.26x lower write power than STT-MRAM by taking advantage of high spin current injection efficiency. Also, owing to separate read and write current paths, the proposed design can optimize each path independently, resulting in 7.69x lower read power and 1.88x higher read-disturb margin in comparison to STT-MRAM that has a common path for read and write operations.

Keywords: MRAM, spin-orbit torque, area optimization

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

Spin-transfer torque magnetic RAM (STT-MRAM) has attracted great attention for on-chip caches and embedded applications due to its desirable attributes like non-volatility, high density, and compatibility with CMOS process [1, 2, 3, 4, 5, 6, 7]. STT-MRAM, however, is designed with the common access path through a magnetic tunnel junction for both read and write operations, which negatively impacts its reliability such as (i) causing a bit flip during a read and (ii) exerting a high stress on the tunnel junction during a write [8, 9, 10]. Recently, spin-orbit torque magnetic RAM (SOT-MRAM) was proposed as another candidate for non-volatile on-chip memories with the enhanced reliability [11, 12, 13]. Since three terminal structure of SOT-MRAM separates a read path from a write path, each path can be independently optimized without disturbing the other. Also, a write of SOT-MRAM does not require a high stress condition across the tunnel junction as SOT-induced switching is performed by spin injection from a heavy metal [14, 15, 16]. These advantages make SOT-MRAM a promising alternative for STT-MRAM.

However, the main disadvantage of SOT-MRAM is that each cell requires two access transistors [17, 18]. This results in bit-cell area larger than that of STT-MRAM using a single access transistor. In this work, we propose a new structure of SOT-MRAM to improve integration density while maintaining advantages of SOT-MRAM. As will be shown, a layout of conventional SOT-MRAM cell includes two metal layers for bit-line (BL) and source-line (SL) routed in the same direction, which dominate a bit-cell area. The key idea of our proposal is to route the SL layer in the direction perpendicular to the BL layer, which can relax the minimum pitch of a cell. Our simulation result shows that the proposed structure is denser than the conventional SOT-MRAM and STT-MRAM by 42\% and 23\%, respectively, when each bit-cell is designed for 7ns switching time, 20\% write margin, and >50\% of read disturb margin.

2. SOT-MRAM fundamentals

A three terminal SOT device consists of magnetic tunnel junction (MTJ), heavy metal (HM), and spin-sink layer (SSL) as shown in Fig. 1. The MTJ comprises a pinned layer (FL) and a free layer (FL) sandwiching an oxide barrier. The magnetization of FL is bi-stable: either parallel (P state) or antiparallel (AP state) with respect to the fixed magnetization of FL. Since the resistance of MTJ in the P state is relatively lower than that in the AP state, the MTJ can function as the storage element whose bit information can be retrieved by passing a read current through a terminal \(T_1\) and sensing the MTJ resistance.

In order to switch the FL magnetization, charge current is applied to the HM in direct contact with FL. It leads to the spin-orbit interaction in HM, creating spin current transverse to the charge current as shown in Fig. 1(b). The spin current injected into the top surface of HM exerts a spin-transfer torque, causing the FL magnetization to be switched. This SOT-induced switching eliminates the reliability concern associated with the oxide barrier of MTJ because the oxide barrier is not stressed by high voltage drop [7]. Also, note that the spin current \((I_S)\) can be larger than the charge current

\[ I_S > I_C \]

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(\(I_C\)), i.e., the spin current injection efficiency can be >100%, because a single electron flowing through the HM transfers multiple units of angular momentum [11, 12]. The SSL is attached to the bottom of HM to enhance the spin current injection efficiency further by reducing the backflow of spin current due to spin-polarized electrons at the bottom surface of HM [19, 20].

The bit-cell of a conventional SOT-MRAM requires two transistors as shown in Fig. 2: (1) a read access transistor connected to the terminal \(T_1\) and (2) a write access transistor connected to a terminal \(T_2\) of HM. Because the read path is separated from the write path, each path can be optimized independently. To write a logical value 1 in the bit-cell, BL is set to a positive value \((V_W)\), SL to a ground \((G_{ND})\), and a write word-line (WWL) is asserted high, resulting in a write current \((I_W)\) flowing from BL to SL through HM. Similarly, a logical value 0 can be written by applying opposite voltages, i.e., \(V_W\) to SL and \(G_{ND}\) to BL. For a read operation, SL is set to \(G_{ND}\), BL is connected to the current source, and a read word-line (RWL) is asserted high such that read current \((I_R)\) flows from BL to SL. Then, sense amplifier compares a reference voltage \((V_{REF})\) from a reference BL with a cell voltage \((V_{READ})\) from BL.

3. Proposed cell design

We first analyze the layout of conventional SOT-MRAM using \(J\)-based rules where \(J\) refers to half the minimum feature size [21]. In this work, the minimum pitch between metal lines is assumed to be 6 \(\mu\)m [22, 23]. The other parameters for layout design rules are defined in Fig. 3(a). Note, if the width of access transistors is sized small, the horizontal dimension is not determined by the transistor width \((W_{FET})\). Rather, it is limited by the metal pitch as shown in Fig. 3(b). In particular, to share BL and SL among cells in the same column, the conventional SOT-MRAM needs two metal lines routed in the vertical direction, resulting in 12 \(\mu\)m in x-dimension. By contrast, if \(W_{FET}\) increases beyond 9 \(\mu\)m, the horizontal dimension also increases proportionally to \(W_{FET}\), as shown in Fig. 3(c). We will assume that \(W_{FET}\) for the conventional SOT-MRAM is 9 \(\mu\)m that is the maximum value desired for high density of memory. This assumption is justified by the fact that SOT-MRAM can achieve sub-10ns write operation even with a small write current thanks to >100% spin current injection efficiency.

The vertical layout dimension typically grows as the number of access transistors increases. As in Fig. 3, the y-dimension of conventional SOT-MRAM using two single-finger transistors is obtained as follows:

\[
W_C + 4W_{G2C} + 2W_G + 2W_C + 2W_{C2A} + W_{A2A} = 23\mu m
\]

Note that the value 23 \(\mu\)m in the above equation is twice the y-dimension of STT-MRAM that uses a single-finger access transistor [22]. Due to this, the conventional SOT-MRAM, even with a small \(W_{FET}\), may lead to the larger bit-cell area when compared to the STTT-MRAM.

In order to improve integration density, we propose a modified SOT-MRAM bit-cell structure based on the observation that the metal line can be added in the horizontal direction without increasing the cell area. To route the SL metal layer in the horizontal direction (rather than the vertical direction), the proposed structure always sets SL to \(G_{ND}\) as shown in Fig. 4(a). Read and write operations are performed with biasing conditions shown in Fig. 4(b). Note, for writing a value 0, BL is biased at the negative voltage \((V_{\text{MINUS}})\) such that the current flows from SL to BL through HM.

Application of a negative voltage to BL needs careful transistor biasing for reliable and energy-efficient operations. First, gate-source voltage \((V_{GS})\) of write access transistor selected for writing a value 0 may exceed \(V_{DD}\) if WWL is biased same as in the conventional cell (See a write access transistor in the cell A in Fig. 5). Because the excessive \(V_{GS}\) causes the reliability issue of transistor such as bias-temperature instability [24], the proposed structure applies \(V_{WWL}\) that is positive, yet lower than nominal \(V_{DD}\), to assert WWL. We note that \(V_{WWL}\) lower than \(V_{DD}\) can reduce the...
current driving strength for writing a value 1 (See a cell B in Fig. 5). However, as will be discussed in simulation section, it is still viable to achieve sub-10ns write operation owing to high spin current injection efficiency. Second, RWL or WWL in the proposed scheme is biased at the negative voltage $V_{\text{MINUS}}$ if its associated transistor is not selected for access. This prevents an unselected transistor from passing the leakage current by ensuring that $V_{\text{GS}}$ is 0V even if the associated BL voltage is negative (See read access transistors in Fig. 5). Third, body-source voltage ($V_{\text{BS}}$) can be positive if a body of the transistor is set to GND as in the conventional design. Since the positive $V_{\text{BS}}$ leads to the forward-biased PN junction between the body and the source, and thus, the unnecessary leakage current from unselected cells, the body voltage in this work is set to $V_{\text{MINUS}}$.

4. Simulation

For comparison of our proposed cell to the conventional STT-/SOT-MRAM cells, we use the simulation framework [25] comprising three components as follows:

1. Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation solver to model the magnetization dynamics [26],
2. Non-Equilibrium Green’s Function (NEGF) formalism to obtain the MTJ resistance, and
3. SPICE simulations to model the circuit of MRAM bit-cells.

The LLGS equation solver determines the critical switching current of each cell based on magnetic device parameters in Table I [27]. The spin current injection efficiency for SOT-MRAM cells, i.e., the ratio of $I_S$ to $I_C$ can be calculated as follows [20]:

$$\frac{I_S}{I_C} = \frac{A_{\text{MTJ}}}{A_{\text{HM}}} \cdot \theta_{\text{SH}}$$

where $A_{\text{MTJ}}$ ($A_{\text{HM}}$) is the cross-sectional area of the MTJ (HM) and $\theta_{\text{SH}}$ is a spin Hall angle that is assumed to be 0.3 in this work [12]. Note from Table I that $A_{\text{HM}} (= \text{HM} \times W_{\text{HM}})$ is designed smaller than $A_{\text{MTJ}} (= \pi/4 \times W_{\text{MTJ}} \times L_{\text{MTJ}})$, resulting in high spin current injection efficiency of 471%.

For SPICE circuit simulations [28], the resistances of MTJ and HM need to be determined [29]. The voltage dependent resistance of MTJ in AP and P states is calculated by the NEGF based electron transport simulation [25, 30], whereas the resistance of HM is estimated by using the experimental resistivity value in [12] and the device dimension in Table I. Further, a commercial 45nm transistor model is used to form the complete memory cell structure and evaluate read and write operations. The comparison is carried out between three different cell structures designed under identical conditions of 7ns switching time, 20% write margin defined as $(I_W - I_C) / I_C$, and >50% of read-disturb margin defined as $(I_C - I_R) / I_C$.

Simulation results are summarized in Table II. STT-MRAM requires a transistor width of 20l (= 400nm) to achieve 7ns switching time with $V_{\text{WRITE}}$ not exceeding the nominal $V_{\text{DD}}$ (1V). By contrast, the conventional SOT-MRAM is designed with 9l (= 180nm) width as mentioned earlier. Even with the relatively small transistor width, the SOT-MRAM requires the low value of $V_{\text{WRITE}}$ for the same 7ns switching specification, leading to the low write power as well. Note, however, the SOT-MRAM cell area is larger than the STT-MRAM cell area because of two-transistor requirement as shown in Fig. 6.

In order to address the disadvantage of SOT-MRAM cell area, the proposed cell routes the SL metal line in the horizontal direction as shown in Fig. 6(c), which relaxes the minimum x-dimension while maintaining the y-dimension. The proposed cell with the transistor sized at 80nm can meet the requirement of 7ns switching time by using biasing conditions in Table II. Compared with STT-MRAM, the proposed cell shows 23% smaller bit-cell area (due to the relaxed minimum x-dimension) and 6.26x lower write power (due to high spin injection efficiency). Also, unlike the STT device whose oxide thickness (1.15nm) trade-offs readability and writability, the SOT device can optimize the oxide thickness (1.45nm) for read operation only. Because the

| Table I | Parameters of the spin devices. |
|---------|---------------------------------|
| STT device | SOT device |
| Gilbert damping, $\alpha$ | 0.007 | 0.0122 |
| Sat. magnetization, $M_s$ | $900 \times 10^3$A/m | $900 \times 10^3$A/m |
| Dimension of free layer ($W_{\text{Lx}}\times L_{\text{x}} \times t_{\text{SL}}$) | 120nm $\times$ 40nm $\times$ 2nm | 120nm $\times$ 40nm $\times$ 2nm |
| Dimension of HM ($W_{\text{HM}}\times L_{\text{HM}} \times t_{\text{HM}}$) | - | 120nm $\times$ 80nm $\times$ 2nm |
| HM resistivity | - | 200$\mu\Omega$ cm |
| Spin Hall angle, $\theta_{\text{SH}}$ | - | 0.3 |
| Oxide thickness, $t_{\text{OX}}$ | 1.15nm | 1.45nm |
| Critical current (7ns) | 130$\mu$A | 42$\mu$A |

$^{12}$MTJ FL has an elliptical shape

| Table II | Comparison of STT-/SOT-MRAMs. |
|----------|---------------------------------|
| Transistor width (nm) | STT- MRAM | SOT- MRAM | Proposed MRAM |
| Bit-cell area ($\mu$m$^2$) | 0.0832 | 0.1104 | 0.0644 |
| $V_{\text{WRITE}}$ (V) | +0.98 | +0.13 | +0.95 |
| $V_{\text{MINUS}}$ (V) | - | - | -0.24 |
| $V_{\text{WRITE}}$ (V) | -1 | +1 | +0.76 |
| Write power ($\mu$W) | 190.82 | 6.86 | 30.47 |
| Read power ($\mu$W) | 69.79 | 9.26 | 9.08 |
| Read-disturb margin (%) | 51 | 96 | 96 |
Fig. 6 Cell layouts of (a) conventional STT-MRAM (b) conventional SOT-MRAM (c) proposed SOT-MRAM. Each cell area is optimized under identical conditions of 7ns switching time, 20% write margin, and > 50% read-disturb margin.

thicker oxide layer translates into the higher resistance that requires the smaller current to develop the same BL voltage during a read, the proposed cell achieves 7.69x lower read power and 1.88x higher read-disturb margin in comparison with STT-MRAM.

5. Conclusion

In this letter, we propose a new structure of SOT-MRAM design that improves integration density while maintaining inherent advantages such as reliability associated with MTJ and energy efficiency during a write. Based on the observation of SOT-MRAM layout that the metal line can be added in the horizontal direction without increasing the cell area, the proposed structure is designed to route the SL metal line, whose direction was conventionally vertical, in the horizontal direction. Compared to the conventional SOT- and STT-MRAMs, the proposed design achieves the cell area improvement by 42% and 23%, respectively. The proposed design also takes advantage of high spin injection efficiency, resulting in 6.26x lower write power than STT-MRAM. The separate read and write current paths of the SOT device enable the MTJ parameter optimization only for read operation, leading to 7.69x lower read power and 1.88x higher read-disturb margin in comparison with STT-MRAM.

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