Effect of NBTI Aging and Process Variations on Write Failures in CMOS and FinFET Flip-Flops

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Abstract— The assessment of noise margins and the related probability of failure in digital cells has growingly become essential, as nano-scale CMOS and FinFET technologies are confronting reliability issues caused by aging mechanisms, such as NBTI, and variability in process parameters. The influence of such phenomena is particularly associated to the Write Noise Margins (WNM) in memory elements, since a wrong stored logic value can result in an upset of the system state. In this work, we calculated and compared the effect of process variations and NBTI aging over the years on the actual WNM of various CMOS and FinFET based flip-flop cells. The massive transistor-level Monte Carlo simulations produced both nominal (i.e. mean) values and associated standard deviations of the WNM of the chosen flip-flops. This allowed calculating the consequent write failure probability as a function of an input voltage shift on the flip-flop cells, and assessing a comparison for robustness among different circuit topologies and technologies.

Index Terms—Digital VLSI; CMOS; FinFETs; noise margins; NBTI aging; process variations; setup time slack;

I. INTRODUCTION

Invasive uninterrupted scaling of CMOS and FinFET technologies to nano-scale level leads to various fallouts such as variability of process parameters and aging due to Negative Bias Temperature Instability (NBTI). While the effects of such issues on performance figures like leakage power and delay modeling have been profoundly inquired [1][2][16][18], their influence on the reliability of digital designs over the years is being modelled and quantified [4][11][13][12] and there is a general correspondence that reliability be a key topic of future digital integrated circuits [14].

Digital operation reliability is hinged upon noise margins, which have been a prime concept since the foundation of logic circuits [8], as they ascertain the robustness of circuit operation to voltage noise in the circuit nodes. The investigation of noise margin behavior impacted by process variability and aging mechanisms is a prerequisite towards the assessment of circuit-level and system-level design reliability.

In this work, we focus our attention on memory elements (registers) in semi-custom digital design. A transient voltage deviation on a register input during a write operation can result in a wrong stored value, i.e. a permanent upset of the system state, and ultimately in a system operation deviance [8]. Therefore, a remarkable role in digital system reliability is played by the Write Noise Margins (WNM) of registers. WNM are defined as the maximum tolerance to input dc voltage noise during a write operation to avoid the memory element by capturing a wrong logic value and storing it permanently (write failure). The concept of WNM differs from the static noise margin of memory cells, the latter being the maximum internal dc voltage noise tolerance to avoid a memory cell state being flipped during idle mode or read mode, thus measuring the memory cell stability [26].

In this work, we address the occurrence of write failures. The occurrence of timing errors, i.e. the possibility that the stored value – albeit correct – becomes valid too late at a register output, is a different failure condition which is not in the scope of this work.

Our work proposes at evaluating and comparing the effect of process variations and NBTI aging over the years on the WNM and the consequent statistical occurrence of write failures in seven types of flip-flop cells. The analysis proceeds from the statistical characterization of WNM, performed by means of Monte Carlo transistor-level simulations, in order to calculate the probability of write failure as a function of an input voltage shift on the flip-flop cells. The seven analyzed flip-flop cells span from dynamic to pseudo-static and static implementations, based on transmission gates, C²MOS gates, and TSPC gates; the analysis is carried out for two distinct CMOS and FinFET technologies.

The presentation of the work is organized as follows: Section II reports related research and highlights the novel contributions of the work, Section III presents the exact definitions and methodology, Section IV discusses the resulting collection of data on noise margins statistics, usable as the basis for higher level analyses, and calculates the statistical distribution of the occurrences of write failures for each flip-flop as a function of an input voltage shift.

II. BACKGROUND AND RELATED WORKS

Process parameter variations has caused several concerns as for digital circuit speed and power consumption. In fact, extensive work has been explored on the impact of variability on propagation delay and leakage power [3][2][17][20][21]. In this work, we

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address the impact of statistical process variations and NBTI aging on the WNMs and consequently on the probability of write failures in register cells (flip-flops) used in semi-custom digital design.

Our focus is on local cell-level variations in equivalent oxide thickness \(t_{oxe}\), channel width \((W)\) and length \((L)\) for CMOS cells, and equivalent oxide thickness \(t_{oxe}^2\), channel length \(L\), fin height \(h_f\) and fin thickness \(t_f\) for FinFET cells. The selected parameter variations have become an integral part of degradation of reliability, specifically while catering with NBTI mechanism [22][23][24].

NBTI is a state-of-the-art degradation factor for the operation of digital circuits. The raising electric field through the oxide thickness generates interface traps in P-type devices and results in unwanted increase in threshold voltage \((V_{th})\) which ultimately affects propagation delay and noise margins. In [5] and [18], investigations have been done on propagation delay for various flip-flops subject to NBTI aging.

A crucial datum obtained by device level research is that NBTI actually depends on process parameters including \(t_{oxe}, L, W\) in MOSFETs, and \(t_{oxe}, L, h_f, t_f\) in FinFETs, so that process variations actually interfere with the aging statistical impact [7][10][25]. In [9], for CMOS gates, \(L, W\) and \(t_{oxe}\) are taken into account in estimating the gate aging effects, to conclude that NBTI circuit aging can be severely affected by the magnitude of the process variations. In the FinFET case, [10] shows a variability analysis on \(t_{oxe}, L, h_f, t_f\) which result to influence the NBTI reliability degradation effect.

In our work, the following established NBTI equations are used within the simulation tools [22][23]:

\[
\Delta V_{th,IT} \approx e^{\left(-\frac{E_{TITF}}{e}\right)^{\frac{L}{L^*}}},
\]

\[
\Delta V_{th,OT} \approx e^{\left(-\frac{E_{TOTFD}}{e}\right)^{\frac{L}{L^*}}},
\]

Eq. 1 and 2 show the physical effect of NBTI in terms of voltage threshold change in interface trapped charges \((\Delta V_{th,IT})\) and oxide trapped charges \((\Delta V_{th,OT})\), involving process parameters along with fitting parameters such as TITTD (Temperature dependent component of interface-trap-inducing threshold voltage degradation), TITCE (Inversion charge exponent for interface-trap-inducing threshold voltage degradation), TITFD (Oxide electric field dependence for interface trap inducing threshold voltage degradation), TOTFD (Oxide electric field dependent component for oxide-trap-inducing threshold voltage degradation) and TOTTD (Temperature dependent component for oxide-trap-inducing threshold voltage degradation). The interested reader should refer to [22][23].

The issue of the reliability of logic memory elements has been always related to the definition of noise margins. In SRAM cells, the criterion of maximum squares in the mirrored VTCs [15] has been applied to quantify nominal static noise margins [19], which express the stability of the memory element to internal voltage noise during idle mode, read access and write access. SRAM cell stability has been studied in terms of such static noise margins with respect to process variations [26] and to NBTI aging [6]. In [31], the authors present a voltage control technique for improving BTI-degraded SRAM cell stability. In [32], the authors report on optimizing the energy-delay product in flip-flops affected by NBTI aging. In [4], a work is reported on estimating the probability of read failure induced by process variations in SRAM cells. A preliminary subset of results of the proposed work has been presented in [35]. To the best of our knowledge no previous work exists on the characterization and study of write failure probability in flip-flops with respect to variability and aging.

III. METHODOLOGY

A. Flip-flop cells under analysis

Fig. 1 – 7 show the schematic circuit design of the flip-flop cells considered in this work. In our analysis, all the circuits are based on a master-slave double latch structure and are established topologies in VLSI design. Other more sophisticated topologies have been proposed in the past, featuring automatic clock-gating, implicit pulsed, explicit pulsed, and differential operating mode [28][29][30][33][34], which are out of the scope of this work. The list of the flip-flops in Fig. 1 – 7, which we also use as reference in the presentation of results, follows:

A) Transmission Gate based static FF;
B) Transmission Gate based pseudo-static FF;
C) Bootstrap Transmission Gate based pseudo-static FF;
D) C²MOS based pseudo-static FF;
E) Bootstrap C²MOS based pseudo-static FF;
F) C²MOS based dynamic FF;
G) TSPC N²MOS-P²MOS based dynamic FF.

The static cells store a bit value permanently, the pseudo-static ones store the value permanently provided that the clock signal is maintained above a certain frequency, and the dynamic implementations need a refresh of the stored value at each clock cycle.

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2 Equivalent oxide thickness \(t_{oxe}\) is mentioned as \(e_r\) in FinFET PTM, however we used \(t_{oxe}\) as a common naming convention throughout the paper.
Cells C and E include “bootstrap” circuits, in which a direct input-output transmission gate path in each latch is used to speed-up the propagation delay of the cell.

B. Write noise margin definition and characterization

For the purpose of WNM assessment, we identify an invalid input voltage, as one that actually results in a write failure, in the flip-flop under analysis. The methodology to characterize the noise margins therefore consists of presenting a voltage value on the flip-flop input pin \( D \) and then checking the actual data recorded by the cell, by examining the output pin \( Q \) after the clock edge has occurred. Once we find the input voltage thresholds for correct write operation, \( V_{\text{writeL}} \) and \( V_{\text{writeH}} \), for ‘1’ and ‘0’ logic input respectively, the high and low noise margins are represented by the widely known relations:

\[
\begin{align*}
\text{WNM}_{\text{H}} &= V_{\text{DD}} - V_{\text{writeH}} \quad \text{WNM}_{\text{L}} = V_{\text{writeL}} \\
\end{align*}
\]

where we have recalled that output nominal voltage values in CMOS and FinFET cell are \( V_{\text{OH}} = V_{\text{DD}} \) and \( V_{\text{OL}} = 0 \text{V} \).

Fig. 8 reproduces SPICE simulation results (for 16 nm CMOS, Flip-Flop A) that exemplify the procedure to measure \( V_{\text{writeL}} \) and \( V_{\text{writeH}} \). For different values of actual input voltage \( V(D) \) on the clock edge, the output voltage either switches to the correct value or remains practically unchanged.

In the actual \( V_{\text{writeL}} \) (\( V_{\text{writeH}} \)) characterization procedure, voltage values on node \( D \) ranging from 0 \text{V} to \( V_{\text{DD}} \) are iterated by a bisection search, until the highest (lowest) voltage on \( D \) producing a low (high) logic output \( Q \) is found. The stop criterion of the bisection search algorithms for determining the target \( V_{\text{writeL}} \) and \( V_{\text{writeH}} \) values is set to an accuracy of 0.001 \(-\cdot\) \( V_{\text{DD}} \). The following pseudo code shows the procedure of estimation of \( V_{\text{writeL}} \) and one can compute \( V_{\text{writeH}} \) in the same manner.

**Pseudo code: VwriteL estimation**

1. **Input:** Transistor-level Flip Flop Netlist with Y, Tox, L, W, Vd parameters
2. **For** each NBTI_Aging_year Y in [0, 1, 2,…. 10]
3. \hspace{1em} **For** each I in \([0...10E4]\]
4. \hspace{2em} Random_value_selection(Tox, L, W);
5. \hspace{2em} **do**
6. \hspace{3em} Update input Vd according to bisection search;
7. \hspace{2em} **Create Netlist(Tox, L, W, Vd);**
8. \hspace{2em} **Simulate SPICE Netlist;**
9. \hspace{3em} Extract output VQ value;
10. \hspace{2em} **While** (VQ is not correct); \hspace{2em} **end For**
11. **Output:** Save VwriteL = Vd value for Tox, L, W, value;
12. **end For**

C. Impact of slack time and clock frequency

The setup time of input \( D \) with respect to the clock edge assumed in the characterization procedure has an impact of the resulting \( V_{\text{writeL}} \) and \( V_{\text{writeH}} \). In general, a large setup slack favors wider noise margins, while a slack time close to zero leads to narrower actual noise margins. Therefore, our analysis has been divided into two operating cases:

- long setup slack times, reflecting design cases where the registers (flip-flops) are not on the critical path of the architecture, or the architecture is clocked at low speed, resulting in a large slack. The long setup slack time was fixed at 2 \text{ns} for all flip-flops types. We verified that longer slack times do not produce any relevant change.
- zero setup slack time, reflecting the case of registers on the critical path of a high-clock-speed architecture design. Zero slack time models a timing critical situation at the input of the flip-flop, possibly producing a logic error in the stored data; it does not refer to a timing error on the output of the flip-flop. In the noise margin analysis at zero setup slack time, the interval between the rising/falling edge of \( D \) and the rising clock edge was set equal to the minimum setup time for each of the flip-flops.

A potentially important point was the influence of the clock period duration. In fact, in the simulation script to identify \( V_{\text{writeL}} \) and \( V_{\text{writeH}} \), we considered the output \( Q \) correct if the voltage value at node \( Q \) stably reached the correct nominal value (0 \text{V} or \( V_{\text{DD}} \)) within the current clock cycle. Our simulations always showed that, in this respect, the outcome and the consequently extracted noise margins are not impacted by the clock period duration for clock frequencies ranging from 10 \text{MHz} up to 1 \text{GHz} and above, i.e. in a range typically used in semi-custom designs in the target technologies. All the presented results have been obtained at the reference clock frequency of 1 \text{GHz}.

D. Aging effect and process variation effect evaluation

For the case of CMOS technology, we can formally express the \( V_{\text{writeL}} \) and \( V_{\text{writeH}} \) values of a generic flip-flop instance as a pair of functions:
where $T_{ox}, L, W$ are to be considered random variables, characterized by technology-dependent nominal value (mean) and standard deviation, and $Y$ is the circuit life in years.

For the case of a generic FinFET-based flip-flop instance, we can similarly write:

\[ V_{\text{write}L} = V_{\text{writeL}}(Y, t_{\text{ox}}, L, W) \]
\[ V_{\text{write}H} = V_{\text{writeH}}(Y, t_{\text{ox}}, L, W) \]

where $t_{\text{ox}}, L, h_{\text{fin}}, t_{\text{fin}}$ are random variables and $Y$ is the year count.

We implemented the characterization in two phases. First, we targeted the impact of aging $Y$ on the noise margins in nominal process conditions by NBTI simulation analysis. Secondly, we targeted the analysis of NBTI aging together with process variation effects, implemented by Monte Carlo simulations with random variations in the technology model parameters, at each aging step $Y$.

### E. Characterization setup

All the circuits include an inverter load cell sized 4 times the minimum size (FO4 load). The target technology models are a bulk FinFET 16 nm LSTP process, at nominal 0.85V supply $V_{DD}$, and a bulk CMOS 16 nm HP process, the latter with scaled-up supply $V_{DD}$ from nominal 0.7V to 0.85V in order to compare the resulting noise margins at same supply voltage.

The NBTI aging analysis was performed on the built-in HSPICE tool MOSFET Model Reliability Analysis (MOSRA). According to the typical usage, the simulation was divided into pre-stress analysis (fresh simulations or at zero time) and post-stress analysis (in long time periods) [23]. We chose the post-stress analysis for 10 years with 2 years’ time period.

For the zero setup slack time case, we had to a priori identify the minimum setup time of each flip-flop type. The state of the art practical definition of minimum setup time has been extensively reported in literature as the setup time causing an increase of 10% of Clock-to-Q nominal propagation delay\(^3\) [9]. Table I reports the characterization obtained for the timing performance of each flip-flop cell in nominal process conditions, obtained by SPICE simulations with MOSRA aging models [23] for different aging times. Note that the minimum setup time degrades (i.e. increases) with aging, so that to provide for 10 years’ circuit operating life we assumed the setup time slack at 10 years aging as design reference.

For statistical variability analysis, according to a typical setup in the literature [17], we implemented HSPICE Monte Carlo simulations with normal distributions of the selected process parameters, assuming $3\sigma/\mu = 10\%$. Other statistical distributions obtained from industrial process development kits (PDK) can be applied without any modification to the methodology. The nominal (mean) values and standard deviation values are reported in Table II. Note that for CMOS $L$ and $W$, the nominal values are of $L_{\text{int}}$ (AL) and $W_{\text{int}}$ ($\Delta W$) respectively; however, the standard deviation value 0.26 nm is according to $L$ and $W$ actual value i.e. 16 nm. The relationship between $L$, $W$ with $L_{\text{int}}, W_{\text{int}}$ is according to BSIM equation i.e. $L_{\text{eff}} = L_{\text{drawn}} + X_{L} - 2 L_{\text{int}}$ and $W_{\text{eff}} = (W_{\text{drawn}}/NF) + X_{W} - 2 W_{\text{int}}$ respectively [27].

### V. Results

#### A. Noise margin distributions

The statistical distributions of all the noise margins samples obtained by MC simulation showed a good matching with normal distributions. In all cases the substantial matching between nominal values and statistical mean values confirm the correctness of the Monte Carlo simulations. In all cases the substantial matching between nominal values and statistical mean values confirm the correctness of the Monte Carlo simulations.

![Image](image.png)

For the calculation of the cumulative normal distribution, based on the obtained values of mean and standard deviation of the WNM, allows us to obtain a picture of the probability of an actual write failure caused by a voltage shift $\Delta V$ at the register input.

\(^3\) Technical documents report 5% as well as 10%, depending on the target degree of tolerance assumed for the cell library.
The voltage shift $\Delta v$ can also be seen as the minimum needed noise margin in given application [4]. In fact, the probability that a register stores a wrong bit is the probability that the voltage noise margin is smaller than the input voltage shift $\Delta v$, i.e. formally:

- Logic value ‘0’ at register input:
  \[ \Pr\{\text{failure}\} = \Pr\{WNM_L < \Delta v\} = \Pr\{V_{\text{write}L} < \Delta v\} = \int_{-\infty}^{\Delta v} N(x, \mu_{V_{\text{write}L}}, \sigma_{V_{\text{write}L}}) \, dx ; \]

- Logic value ‘1’ at register input:
  \[ \Pr\{\text{failure}\} = \Pr\{WNM_H < \Delta v\} = \Pr\{V_{\text{write}H} > V_{DD} - \Delta v\} = \int_{V_{DD} - \Delta v}^{+\infty} N(x, \mu_{V_{\text{write}H}}, \sigma_{V_{\text{write}H}}) \, dx. \]

Here, $\Delta v$ is a positive quantity and $N(x, \mu, \sigma)$ is the normal probability density function with mean $\mu$ and standard deviation $\sigma$.

Fig. 16 shows the results of the above calculation for the zero slack time case, allowing a direct comparison of the flip-flop cells with respect to their robustness to a certain amount of input voltage drop/rise $\Delta v$ during a write operation, as impacted by process variations and NBTI aging.

From our results, while in nominal conditions the CMOS cells outperform FinFET ones as for robustness to input voltage shift (even at 10 years’ aging), when considering process variations the outcome is reversed: the larger standard deviations of noise margins in CMOS cells lead to a smoother behavior of the failure probability curves (Fig. 16) and ultimately reduce the yield associated to a certain input noise tolerance more than it happens in FinFET cells. It must be considered, however, that this result only refers to the case $3\sigma/\mu = 10\%$ assumed in both technologies for the selected geometric process parameters.

In general, we observe an asymmetrical performance for low and high logic input values, depending on the cell. This effect is evidenced for both technologies, and suggests that a proper transistor sizing could balance robustness between ‘1’ and ‘0’ logic write operations.

A final most important outcome of the reported analysis, is the identification of the best performing flip-flop circuit topologies with respect to write failures subject to process variations and NBTI aging. In this respect, the validity of the results is enforced by the fact that in both technologies we have the same outcomes. First, bootstrap transmission gate results to enhance robustness to process variations and also to aging, as shown by Fig. 16 for flip-flops (C) and (E). Secondly, flip-flops (G), (F) and (D) appears to be more impacted by NBTI aging than others. Somehow surprisingly, the fully static flip-flop (A) shows a poor performance especially referring to the 10-year aging condition, not very differently from fully dynamic implementations (F) and (G) which in fact were expected to be weak. Overall, the best performance is attained by flip-flop (E), which may be considered for reliability-oriented libraries of semi-custom cells.

V. CONCLUSIONS

The characterization of $WNMs$ of different flip-flop cells have been quantified with respect to the combined effect of NBTI aging and process variations, in a CMOS and a FinFET technology, according to state of the art technology models; the distribution of write failure probability has been also calculated accordingly.

The results show that the NBTI aging affects the noise margins differently in large slack time and zero-slack time conditions. Also, for large slack time an evident asymmetry exists between the aging effects on the logic high noise margin and the logic low noise margin.

The evidently smaller standard deviation in FinFET cells with respect to CMOS, results in better performance as for write failure probability at a given input voltage noise.

As for the cell topology comparison, fully static cells results to perform poorly with respect to pseudo-static ones, and bootstrap transmission gates result to improve the noise margins. Overall, the best performing flip-flop for reliability results to be the bootstrapped C$^{2}$MOS pseudo-static cell.

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### Table I – Characterized propagation delay and minimum setup time for different types of flip-flops at different aging times

| MOSFET 16 nm | FinFET 16 nm |
|--------------|--------------|
| Q edge       |              |
|              | 0 years      | 10 years    |
|              | 0 years      | 10 years    |
|              | t_{CKQ} (ps) | t_{setup} MIN (ps) | t_{CKQ} (ps) | t_{setup} MIN (ps) | t_{CKQ} (ps) | t_{setup} MIN (ps) | t_{CKQ} (ps) | t_{setup} MIN (ps) |
| flip flop A  | 0.0-1        | 05.70        | 10.00       | 06.59        | 12.62        | 06.78        | 06.83        | 08.05        | 07.68 |
| flip flop B  | 0.0-1        | 05.48        | 13.16       | 06.44        | 15.98        | 06.09        | 06.19        | 06.17        | 08.08 |
| flip flop C  | 0.0-1        | 11.09        | 10.59       | 15.05        | 10.68        | 06.03        | 06.36        | 08.03        | 06.84 |
| flip flop D  | 0.0-1        | 08.63        | 17.41       | 09.84        | 21.37        | 08.46        | 11.20        | 09.41        | 12.11 |
| flip flop E  | 0.0-1        | 08.58        | 19.79       | 10.04        | 22.17        | 08.70        | 10.22        | 08.80        | 11.58 |
| flip flop F  | 0.0-1        | 05.98        | 21.77       | 06.66        | 29.00        | 04.68        | 13.47        | 05.55        | 15.45 |
| flip flop G  | 0.0-1        | 01.59        | 09.00       | 02.79        | 12.00        | 00.82        | 08.00        | 02.32        | 11.00 |

### Table II – Process parameters with their mean and standard deviation values

| Parameters | MOSFET 16 nm | FinFET 16 nm |
|------------|--------------|--------------|
|            | t_{OX} [nm] | L [nm] | W [nm] | t_{OX} [nm] | L [nm] |
| N-Type     | 0.95 0.0317 1.45 0.26 5 0.26 | 1 0.0334 26 0.867 12 0.40 20 0.667 |
| P-Type     | 1 0.0334 1.45 0.26 5 0.26 | 1 0.0334 26 0.867 12 0.40 20 0.667 |
Fig. 1. Transmission Gate based static flip-flop A

Fig. 2. Transmission Gate based pseudo-static flip-flop B

Fig. 3. Bootstrap transmission gate based pseudo-static flip-flop C

Fig. 4. C$^2$MOS based pseudo-static flip-flop D

Fig. 5. Bootstrap C$^2$MOS based pseudo-static flip-flop E
Fig. 6. C²MOS based dynamic flip-flop F

Fig. 7. TSPC N²MOS-P²MOS based dynamic flip-flop G

Fig. 8. Sample of SPICE simulations (16 nm CMOS, FF-A). Top: Clock, Mid: $V_{\text{writeH}}$ characterization, Bottom: $V_{\text{writeL}}$ characterization
Fig. 9 $V_{\text{write}H}$, $V_{\text{write}L}$ nominal values and standard deviations for flip-flop-A

Fig. 10 $V_{\text{write}H}$, $V_{\text{write}L}$ nominal values and standard deviations for flip-flop-B
| FF-C | Nominal | MC Standard Deviations |
|------|---------|------------------------|
| Large Slack | ![Graph](image1) | ![Graph](image2) |
| Zero Slack | ![Graph](image3) | ![Graph](image4) |

Fig. 11 $V_{\text{writeH}}$, $V_{\text{writeL}}$ nominal values and standard deviations for flip-flop-C

| FF-D | Nominal | MC Standard Deviations |
|------|---------|------------------------|
| Large Slack | ![Graph](image5) | ![Graph](image6) |
| Zero Slack | ![Graph](image7) | ![Graph](image8) |

Fig. 12 $V_{\text{writeH}}$, $V_{\text{writeL}}$ nominal values and standard deviations for flip-flop-D
Fig. 13 $V_{writeH}$, $V_{writeL}$, nominal values and standard deviations for flip-flop-E

Fig. 14 $V_{writeH}$, $V_{writeL}$, nominal values and standard deviations for flip-flop-F
Fig. 15 $V_{\text{writeH}}$, $V_{\text{writeL}}$ nominal values and standard deviations for flip-flop-G
Fig. 16. Write Failure Probability of the Flip-Flop cells vs input voltage shift $\Delta v$ (on the x axis).