A Shunt DC Electric Spring-Based Control Strategy for Real-Time Critical and Noncritical Load Management in DC Microgrid

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Deployment of DC Electric Spring (DCES) technology is an innovative demand side management (DSM) program that helps to mitigate voltage interruptions. Conventional control strategy uses proportional-integral controllers to regulate DC spring parameters. As PI controllers have a trade-off between settling time and peak overshoot, they may not be able to achieve the desired dynamic performance under varying DC microgrid (DCMG) conditions. In this regard, this paper proposes an inverted zero compensator for the control of shunt DCES (ShDCES) in DCMG. This controller regulates the ShDCES current and terminal voltage under all operating conditions with reduced settling time and peak overshoot. A power management algorithm is also proposed to optimize the operation of ShDCES under the presence of varying PV generation and critical and noncritical loads. A detailed mathematical analysis of ShDCES and inverted zero compensator design are furthermore incorporated to validate the strategy. The simulation of the proposed method is performed in MATLAB/Simulink environment. The comparison analysis with the conventional controller proves the effectiveness of the new controller. The results are also validated using real-time simulator OP4510RTS.

1. Introduction

As India holds the third rank in the emission of greenhouse gas, transformation towards a cleaner energy sector is the utmost necessity to reduce fossil fuel consumption and thereby tackle the drastic climatic changes [1–4]. The technological advancements in power electronics have promoted the desegregation of renewable energy sources (RES) into the electric power system leading to reduced carbon footprints. However, the integration of a higher percentage of RES has led to grid instability and poor power quality. The use of microgrids is a promising solution to get rid of these aforementioned shortcomings of RES integration. Among different types of microgrids, standalone DC microgrids (DCMG) have come up with a ray of hope for reliable and quality power supply especially to remote rural areas having no access to grid [5–7]. Despite these advantages, DCMG is prone to voltage flickers and instability [8, 9]. Since contemporary electronic loads are intolerant to voltage changes, the primary challenge facing the DCMG is the need to maintain dynamic voltage control as stability of DCMG is indicative of constancy in bus voltage [10]. The stability of all electrical systems depends on the balance between generation and demand. The traditional power system follows a strategy based on power generation rather than load demand [11–13]. Though it is impractical to determine real-time generation due to the intermittent nature of the RESs, it is advisable to switch to Demand Oriented Power Control Strategy [14]. Battery energy
storage systems (BESS) are usually used to attain real-time energy balance by buffering the intermittencies of PV power [15, 16]. However, reducing the size of BESS and increasing the battery life are major challenges due to the high cost and environmental threats arising from dumping of obsolete batteries [17].

Electric Spring (ES) is a new concept in demand side management (DSM) initially introduced to stabilize the bus voltage in AC power systems with nondispatchable RESs having intermittent characteristics by the adaptive manipulation of loads [18, 19]. In spring concept, the loads are grouped as critical loads (CL) and noncritical loads (NCL) based on their tolerance limits to voltage fluctuations [20]. The main advantages of this DSM approach are its on-site voltage support utilizing the flexibility of loads in the system and independency of information and communication technology (ICT) [20]. The inclusion of storage components into the ES configuration increased its functionalities like storage reduction [13], three-phase balancing [18], frequency stabilization [21], and so on in AC systems. This concept of ES is extended to DCMG systems for voltage stabilization and size reduction of energy storage devices [22, 23]. Similar to ACES, DCES can also be incorporated into DCMG via two major configurations based on how the ES connects to the NCL, namely, the series DCES (SDCES) and the ShDCES [24, 25]. In [26], different topologies of DCES are compared. A PV-embedded DCES is discussed in [27] for reducing energy storage requirements. In all the above-discussed papers, SDCES is used for critical load voltage stabilization by real-time manipulation of NCL. As the NCL is connected in series with DCES, SDCES offers a slower dynamic response leading to a larger settling time and overshoot of DC bus voltage than its shunt rival [23]. In addition, the boundary of voltage tolerance limit for NCL needs to be predefined [26] in SDCES, which may also limit its operation within a band. As a result, practical implementation of the SDCES configuration which ensures both steady-state and dynamic performance is difficult. In [28], parallel connection of NCL has been implemented for DCES using a three-port converter, but the circuit is costlier and complicated in construction. Hence, this paper focuses on a simple ShDCES configuration with a proper power management scheme which ensures better transient and steady-state performances by the real-time manipulation of NCL.

In the literature, both single-loop and two-loop control strategies with conventional PI controllers are adopted for controlling the DCES. Conventional PI controllers are able to improve steady-state performance but do not contribute much to transient performance [29]. Further PI controller leads to additional overshoots over the transient period due to high gain at crossover frequency. Therefore, this work utilizes an inverted zero lag compensator for reducing the gain introduced by the conventional PI controller at high frequencies, which in turn improves the steady-state and transient performance of DCMG. The proposed control strategy thus ensures improved dc bus voltage stabilization and enhanced ShDCES performance under different operating scenarios. Additionally, a power management strategy is proposed to control the coordinate operation of CL, NCL, PV, and ShDCES, which further reduces the battery’s charge/discharge cycle and improves the battery’s cycle life. The major key contributions of this work include the following:

1. An inverted zero-based lag compensator control scheme is analyzed and implemented for ShDCES in isolated DCMG. The proposed control scheme ensures the fast dynamic and steady-state performance for DC bus voltage.
2. A detailed mathematical modeling of ShDCES and inverted zero compensator design procedure are derived to regulate the operation of DCMG. Further, the stability of controller parameters is validated using frequency domain analysis.
3. An optimized energy management strategy for ShDCES-integrated DCMG is proposed to ensure minimal usage of battery energy and extended battery cycle life.
4. A comparative analysis of the proposed controller and conventional controller is carried out.
5. A prototype of the proposed ShDCES-integrated DCMG is developed and validated with inverted zero compensator realized through the OPALRT platform.

The remaining sections are structured as follows. Section 2 deals with the system configuration and modeling, which comprises the basic concept, design, and operating modes of DCES, PV design, and system loads. Section 3 covers the controller design and stability analysis of the SPV-fed ShDCES-integrated DCMG test system. Section 4 and Section 5 discuss the simulation studies and comparative analysis. Finally, Section 6 and Section 7 deal with experimental validation and conclusions.

2. System Configuration and Modeling

Figure 1(a) portrays the generalized configuration of the test system. The main components comprise an MPPT controlled SPV system, ShDCES, and loads. The converters are used for interfacing the loads and sources with the DC bus. For meeting the demand during shortfall in PV generation, battery-incorporated ShDCES is shunted with the loads. A power management strategy with a new control procedure is suggested to ensure DC bus voltage stabilization of DCMG.
under varying disturbances. As per system requirements, ES can be used to boost or buck voltage like mechanical springs, which stores and releases equivalent energy to create a force by changing the displacement [8, 9]. The term ES has been coined from the force-voltage analogy in control system engineering [8]. The DCES basically encompasses a battery and a bidirectional DC-DC converter operating in buck and boost mode as depicted in Figure 1(b). The variation in bus voltage triggers the DCES into action for regulating a constant voltage across CL by controlling the voltage across ES, thus establishing power balance automatically. The literature reviews reveal that DCES could play a major role in reducing battery storage, and the charge/discharge cycles of batteries can be reduced in future grids.

Depending on the operating principle, there are two categories of DCES, namely, SDCES and ShDCES [8, 9, 23]. Both SDCES and ShDCES are DC-DC converters with storage devices operating in synchronization with voltage controller circuits for accomplishing stabilized DC bus voltage. The SDCES plays the role of a controllable voltage source to form a smart load when cascaded with NCL [8, 9, 23]. When the bus voltage is above the desired value, the NCL voltage is raised by the absorption of current, while buck operation is initiated to release the current if there is a decrease in bus voltage compared to the desired value. The ShDCES acts as a controllable current source shunted with the DC bus [8, 9, 23]. When the bus voltage surpasses its desired value, the ShDCES draws current from the bus, whereas it releases current to the bus when the bus voltage gets below the desired value. ShDCES maintains a consistent voltage across all the loads attached to the bus [8, 9, 23] as opposed to SDCES, which regulates bus voltage by relinquishing the voltage quality of NCL. Hence, this work has proceeded with a shunt-type configuration as represented in Figure 2(a).

2.1. Modes of Operation of DCES. The modes of operation of DCES are grouped into four categories [9]:

1. Boosting Discharge Mode (BDM): when there is a drastic decrease in DC bus voltage, the DCES operates in BDM. In this mode, the battery-powered DCES begins to discharge, thereby increasing the bus voltage, which in turn helps to restore system stability.

2. Boosting Charge Mode (BCM): in this mode, DCES boosts up the bus voltage while the surplus power is utilized for charging the battery.

3. Suppressing Discharge Mode (SDM): the DCES acts as a controllable current source shunted with the DC bus [8, 9, 23]. When the bus voltage surpasses its desired value, the ShDCES draws current from the bus, whereas it releases current to the bus when the bus voltage gets below the desired value. ShDCES maintains a consistent voltage across all the loads attached to the bus [8, 9, 23] as opposed to SDCES, which regulates bus voltage by relinquishing the voltage quality of NCL. Hence, this work has proceeded with a shunt-type configuration as represented in Figure 2(a).

2.2. Design of ShDCES. The bidirectional converter consists of inductance and load side capacitance with two switches as depicted in Figure 1(b) [29–32]. In the buck mode (battery charging) of operation, only $S_1$ will be ON and power flows from the DC bus side to the battery. In boost mode (battery discharging mode), $S_2$ will be ON and power will flow from

![Figure 1: (a) Generalized block diagram of ShDCES-integrated DCMG and (b) basic configuration of DCES.](image-url)
the battery to the DC bus. Equation (1) found in [29] is used in the design of the passive components of ShDCES, which assume a continuous conduction boost mode of operation where \( L_d, C_d, V_{dc}, f_{dces}, f_{sw}, \) and \( D \) represent inductance, capacitance, output voltage, current, switching frequency, and duty ratio of DCES, respectively.

\[
\begin{align*}
I_d &= \frac{V_{dc}D}{\Delta t_{dces}f_{sw}} \\
C_d &= \frac{I_{dces}D}{\Delta V_{dc}f_{sw}} \\
D &= \frac{V_{dc} - V_{dces}}{V_{dc}}
\end{align*}
\]  

Equation (1)

2.3. PV Design. Several pieces of literature focused on the modeling of PV arrays [33]. To obtain desired voltage and current, the PV arrays are connected in cascade and/or in shunt. Temperature and irradiance fluctuations strongly affect the properties of PV array’s characteristic curves. Figures 3(a) and 3(b) represent the I-V and P-V curves of the PV array used for the simulation. Figure 3(c) illustrates the flowchart of the popular Perturb and Observe (P & O) algorithm used for the MPPT controller [34, 35]. PV specifications are listed in Table 1, and equation (2) represents the characteristic equation of the single diode model of the PV array [33].

\[
i_{pv} = N_p i_{ph} - N_p i_{ns} \left( e^{(N_p/N_s)} - 1 \right)
\]

\[
- \frac{N_p V_{pv}/N_s}{R_{sh}} + i_{pv}R_s
\]

where \( V_{pv} \) is the PV array voltage, \( I_{pv} \) is the PV array current, \( I_{ph} \) is the total photocurrent generated from the PV array, \( I_{ns} \) is the reverse saturation current of PV cell, \( R_s \) and \( R_{sh} \) are the series and parallel resistances, \( A \) is the diode ideal factor, \( T \) is the PV cell’s working temperature, \( K \) is Boltzmann’s constant \((1.38 \times 10^{-23} J/K)\), \( N_p \) is the number of Parallel PV cells, and \( N_s \) is the number of series PV cells.

2.4. System Loads. In the ES concept, based on the voltage tolerance range, loads fall under two classes, namely, critical loads (CL) and noncritical loads (NCL) [9]. CL comprises appliance requiring a steady DC voltage such as data servers and computers, while NCL comprise washing machines, electric water heaters, and air conditioners capable of withstanding wide voltage deviations but within allowable limits [9, 23]. Figure 2(a) shows the basic circuit of ShDCES, where RCL represents the critical load and RNCL represents the noncritical load. As ShDCES configuration is considered for analysis, \( R_s \) represents the parallel combination of \( R_{CL} \) and \( RNCL \).

3. ShDCES Controller Design and Stability Analysis

A single bus ShDCES-integrated DCMG as depicted in Figure 2(b) is proposed. An advanced control strategy is needed to optimize the performance of ShDCES in DCMG. The traditional method uses the PI controller to control the ShDCES parameters in the DCMG [27]. However, the PI controller cannot provide the optimum steady-state and transient performance simultaneously [29]. Therefore, a new control strategy with an inverted zero compensator is proposed in this work to control the performance of ShDCES. The proposed controller uses two loops to control the DC bus voltage and the ShDCES current. In Sections 3.1 and 3.2, detailed modeling and analysis of the proposed method are described.

3.1. ShDCES Inner Current Control Loop Design. A bidirectional DC/DC converter is used to interface the ShDCES module with the DC bus. Due to the presence of right half side zero in the boost mode of operation of the bidirectional converter, boost mode is regarded for the current controller loop design. The ShDCES current of the bidirectional converter is fed back to the error detector with a gain of \( H_{ES} \). The triggering pulses to the switches \( S_1 \) and \( S_2 \) are created by modulating the pulse width. Figure 4 is the SSM of DCMG. The prime equations used in the design of the ShDCES current control loop are represented using equations (3)–(6), and all relevant equations used for calculating the controller parameters are also tabulated in Table 2. The feedback factor \( H \) of the battery current control loop is taken as unity [36]. The duty ratio \( d \) to ShDCES current \( i_{dces} \) transfer function \( G_{id} (s) \) is represented in equation (3), and the parameters for computing \( G_{id0} \) are tabulated in Table 2.
\[ G_{id} = \frac{1}{s} \left( \frac{1}{T_h} \right) \]

where \( \hat{D} \) is the duty ratio, \( D \) is the ShDCES duty ratio, \( \hat{D} = 1-D \), and \( \omega_0 \) and \( \omega_{zid} \) are the ShDCES angular frequency and angular corner frequency. The designed values of \( D \), \( G_{id0} \), \( \omega_{zid} \), \( Q_d \), and \( \omega_0 \) are 0.5, 38.4000, 869.5652, 1.6167, and 702.9019 rad/s.

The Bode plot of the uncompensated \( T_{ud} \) current control loop of the ShDCES converter is marked in Figure 5(a). The GM and PM are \( \infty \) and 88.9° at a crossover frequency of 3.48 kHz. Even though the closed-loop system is stable, an inverted zero lag compensator \( G_{ci} \) is incorporated to further enhance the transient as well as steady-state conditions. The compensated loop gain of the ShDCES current control loop is designed with a desired crossover frequency \( f_c \) of 4 kHz. The inverted zero of the compensator is selected to provide high gain at low frequencies to reduce steady-state error, and a pole is added at high frequencies to nullify the gain introduced by the inverted zero. The implementation of an inverted zero pole compensator is simple compared to a PID controller, which also ensures

\[ T_{ud}(s) = H_{ES} G_{id}(s). \]  

\[ G_{id}(s) = \frac{i_{dces}}{d} = G_{id0} \frac{1 + (s/\omega_{zid})}{1 + (s/Q_d \omega_0) + (s^2 / \omega_0^2)}. \]  

**Figure 3:** (a) I-V characteristics. (b) P-V characteristics of PV panel with varying irradiance. (c) P & O MPPT algorithm flowchart.

**Table 1:** The system parameters for simulation.

| S. no | Parameters | Values |
|-------|------------|--------|
| 1     | PV parameters |         |
|       | Open circuit voltage \( (V_{pv}) \) | 38.6 V |
|       | Short circuit current \( (I_{pv}) \) | 8.93 A |
|       | Voltage at MPP \( (V_{mp}) \) | 31.6 V |
|       | Current at MPP \( (I_{mp}) \) | 8.21 A |
|       | Power at MPP \( (P_{mp}) \) | 259.4 W |
| 2     | DCES parameters |         |
|       | DCES voltage \( (V_{dces}) \) | 24 V |
|       | DCES Ah capacity | 17 Ah |
|       | DCES inductance \( (L_d) \) | 2.2 mH |
|       | DCES capacitance \( (C_d) \) | 230 \( \mu \)F |
|       | Switching frequency \( (f_{sw}) \) | 20 kHz |
| 3     | Load parameters |         |
|       | Critical load resistance \( (R_{CCL}) \) | 20 \( \Omega \) |
|       | No critical load resistance \( (R_{NCL}) \) | 20 \( \Omega \) |
|       | Nominal load power | 0.5 kW |
|       | Bus \( (V_{bus}) \) | 48 V |
superior performance at steady-state and transient situations. The ShDCES current control loop controller transfer function $G_{ci}(s)$ is as shown in Table 2, where $\omega_{pcid}$ and $\omega_{zcid}$ are the pole and zero of the compensator. The zero and pole are set as 10 times ahead and after the ShDCES crossover frequency, and the obtained values are 2513.27 rad/s and 251327.41 rad/s. The ShDCES current control loop compensator is calculated using equation (5). The obtained $G_{ci0}$ value is 1.1519 [36]. The compensated loop gain is obtained from equation (6).

\[
G_{ci}(s) = G_{ci0} \frac{\omega_{zcid}/s}{1 + (\omega_{pcid}/s)}
\]

(5)

\[
T_{cd}(s) = G_{ci}(s)G_{id}(s).
\]

(6)
The GM and PM of the compensated loop are $\infty$ and $75.6^\circ$ at a crossover frequency of 4 kHz as obtained from Bode analysis and depicted in Figure 5(a), which ensures stability.

3.2. ShDCES Outer Voltage Control Loop Design. The DC bus voltage must be stabilized to attain power balance in DCMG. The PV and ShDCES converters are designed with a proper controller for ensuring the stability of the inner current control loop. As the outer voltage control loop also plays a significant role in stabilization, the next step is to design the parameters of the voltage controller properly to ensure the stability of the overall system, and the prime equations used in the design of the outer voltage loop are represented using equations (7)–(10). The ShDCES current to DC bus voltage transfer function $G_{v\ell}(s)$ is obtained from equation (7), where the computed values of $G_{\mathrm{c}\ell}$, $\omega_{p\ell}$ and $\omega_{s\ell}$ are 11.25, 23011, and 869.5652 rad/s, respectively.

$$G_{v\ell}(s) = \frac{\dot{V}_{dc}}{i_{dces}} = G_{v\ell} \left( 1 - \frac{s/\omega_{p\ell}}{1 + s/\omega_{s\ell}} \right). \quad (7)$$

The uncompensated loop gain of the DC bus voltage control loop with the ShDCES controller is obtained from equation (8). The Bode plot of the uncompensated loop gain is shown in Figure 5(b). In order to improve the gain at low frequencies and make the system more stable, a DC bus voltage controller $G_{cv}(s)$ is computed using equation (9).

$$T_{av}(s) = H_{V} \left[ \frac{G_{av}(s)}{H_{ES}} \right], \quad (8)$$

$$G_{cv}(s) = G_{v\ell} \left( 1 + \frac{\omega_{s\ell}}{s} \right), \quad (9)$$

$$T_{cv}(s) = T_{av}(s)G_{cv}(s). \quad (10)$$

As the ShDCES converter right half side zero is resting at 3.6624 kHz, the bandwidth of the voltage management loop $f_{s\ell}$ is picked out to be 366.624 Hz, which is $f_{s\ell}/10$ for reducing the effect of $\omega_{p\ell}$. The compensated loop gain of the DC bus voltage control loop with the ShDCES controller is obtained from equation (10).

The Bode plot of the compensated voltage control loop is also marked in Figure 5(b), and the obtained BW 366.6 Hz and PM 85.2° of the compensated outer voltage control loop ensure stable operation of DCMG. The obtained BW of the outer voltage loop, 366.624 Hz, is lesser compared to the BW of the inner current loop. It validates that the inner current loop is faster compared to the outer voltage loop making the operation of the current control loop independent, which in turn also simplifies the design of the voltage control loop. From the Bode plot shown in Figure 5(b), it is also inferred that the system has high gain at low frequencies and low gain at high frequencies, ensuring enhanced steady-state and transient responses.

3.3. Power Management Strategy. The proposed power management strategy (PMS) aims to ensure the efficient operation of ShDCES by combining load power demand and the SoC DCES range. The unified controller of ShDCES operates in accordance with power availability in the DC bus. However, a PMS is inevitable to regulate the charge and discharge cycles of ShDCES, leading to increased battery life. The proposed PMS also controls the power flow in NCL and CL. The flowchart of the proposed PMS is illustrated in Figure 6. The upper and lower limit of ShDCES power demand are represented by $P_{dcesU}$ and $P_{dcesL}$. When the ShDCES power demand exceeds $P_{dcesU}$, the NCL is manipulated to meet the CL power demand, whereas the lower limit enables the reverse power flow from the DC bus. When the power demand range lies between the lower and upper limits, the operation of ShDCES depends on PV power availability. This helps to extend the operating hours and lifespan of the battery in ShDCES. The DCES operation is designed based on available SoC ($SoC_{dces}$) and load demand. The modes are explained as follows:

(i) $SoC_{dces} > 80\%$: this mode corresponds to the maximum allowable limit of stored energy in ShDCES. In this mode, charging is limited, and supplying to the load is preferred. Hence, both NCL and CL are active, and PV shifts to load regulation mode to supply the load demand. If the PV generation is less than load demand, the ShDCES supplies the deficit power of CL.

(ii) $50\% < SoC_{dces} < 80\%$: depending on the load demand, the ShDCES supplies or absorbs energy in this mode. In this SoC$_{dces}$ range, the ShDCES would have enough power to meet the total load demand. This mode is divided into two submodes so as to control the operation of NCL and CL. If the power demand to the ShDCES is greater than $P_{dcesU}$, then NCL is disconnected to support the power demand of CL. On the other hand, if the power demand is less than the upper limit allowed, the ShDCES operates to supply or absorb power from the DC bus.

(iii) $20\% < SoC_{dces} < 50\%$: in this mode, the SoC$_{dces}$ of ShDCES lies in between 20% and 50%. Hence, the NCL is disconnected to fully utilize the ShDCES for CL power demand. Also, the PV operates in MPPT mode.

(iv) $SoC_{dces} < 20\%$: if the SoC$_{dces}$ is less than 20%, the NCL is disconnected, and the operation of CL and DCES is determined by the PV power availability. If there exists excess PV generation after meeting CL demand, the DCES absorbs the excess power to regain its SoC. If the PV power is not enough to meet the CL demand, PV control shifts to load regulation mode. Load regulation is not discussed as the focus of the work is on ShDCES. Preference of this mode is to charge the ShDCES and helps in restoring the normal operation of the system.

4. Simulation Results

The general schematic of the ShDCES-integrated DCMG setup depicted in Figure 1(a) is simulated in MATLAB/ Simulink. Simulation studies have been carried out to
examine the coordinated operation of PV, ShDCES, non-critical loads, and critical loads under different conditions. The PV panel used in the test system is 1Soltech 15TH-215-P. The ShDCES battery rating is 24 V and 17 Ah. CL and NCL are represented by resistive loads. The parameters selected for the simulation study are detailed in Table 1. Two cases are considered for performance analysis of the proposed method through the control of CL and NCL when exposed to various disturbances.

4.1. Performance Analysis of CL. Voltage regulation of the CL is important to preserve the power balance and stability of the DCMG. Hence, source and load side disturbances are applied to evaluate the performance of the proposed method. The simulation results of DCMG under different disturbances are shown in Figure 7. Initially, the DC bus voltage is regulated at 48 V, the CL power is 400 W, and the NCL power is 0 W. The PV output is 265 W, and the system operates in a power deficit mode activated by ShDCES to supply the remaining power to preserve the power balance as shown in Figures 7(a) and 7(b). To validate the stability of the DC bus voltage and the power balance in the system corresponding to load disturbances, at \( t = 1 \) sec, CL decreases to 200 W. PV generation is sufficient to meet load demand in this mode, forcing ShDCES power to 0 W and thus ensuring power balance. At \( t = 2 \) sec, the disconnected CL is reinstalled, and the ShDCES works in boost mode to maintain the bus voltage constant. At \( t = 3 \) sec, the PV generation increases from 265 W to 415 W. In this mode, the total load demand is met by the coordinate operation of PV and ShDCES. As the PV power output increases, the power supplied by ShDCES decreases to stabilize the DC bus voltage. At \( t = 4 \) sec, the PV power is increased to 500 W. In this mode, the system operates in surplus power mode, forcing ShDCES to absorb excess power to maintain the power balance in the system. In short, CL power is accurately supplied by the coordinate operation of PV and ShDCES.

4.2. System Response towards NCL. Since NCL comprises a load of less priority, its performance depends entirely on the

![Flowchart of power management strategy of ShDCES.](image-url)
power availability of the system. In the proposed PMS, the maximum power limit allowed by the NCL is 20% of the rated power. According to PMS, the NCL can only be activated when the PV generation is ample to meet the total load demand. From the simulation results shown in Figure 7(b), the NCL is activated from $t = 1$ sec to $2$ sec and $t = 3$ sec to $4.5$ sec. The NCL has been activated at $t = 1$ sec as the CL demand was lower than the PV generation.

In summary, the simulation study reveals that the NCL is deactivated during excess power demand to assure the smooth performance of the CL. Whenever the CL power demand exceeds PV power, the NCL connects or
disconnects based on the available power of ShDCES. Hence, a reduction in PV power generation will ensure reduced battery storage requirement as the NCL disconnects to meet CL load demand. Disconnection of the NCL reduces the charge/discharge cycle of the ShDCES and thereby increases the battery life.

5. Comparison with Conventional Control Strategy

This section deals with a comparative performance analysis of the proposed controller with the traditional PI controller. The DC bus voltage waveform for the conventional and proposed controller is depicted in Figure 8. The DC bus shows a peak overshoot of 25–27% with a conventional control strategy during load disturbances, while the peak overshoot is reduced to 10–13% using the proposed method. With the change in PV irradiance, the DC bus shows a peak overshoot of 2.5–4.5%, while the peak overshoot decreases to 2-3% with the proposed control strategy. The settling time of DCMG with the conventional controller is 70–100 m·sec and 60–70 m·sec, respectively. For the proposed controller, the settling time is reduced by 50% compared to the conventional controller. In all cases, the settling time for the proposed controller is within the range of 30–40 m·sec, thus ensuring the effective operation of the ShDCES with DCMG.

6. Experimental Study and Discussions

Real-time simulation study is experimentally validated using the OP4510 RTS simulator. The control method is included in the control block of MATLAB/Simulink®, and real-time simulations were performed using the FPGA-based real-time simulator as shown in Figure 9. System parameters considered for experimental evaluation are similar to those for simulation studies and are shown in Table 1. Different cases are considered for testing CL voltage control using real-time manipulation of the NCL, including the ShDCES function. Due to the rapid and efficient working of the proposed PMS and ShDCES controller strategy, the DC bus voltage of DCMG has been found to stabilize and ensure power balance in the system. This study examines the performance of CL by applying PV and load disturbances. In each case, the NCL manages to accommodate the power balance according to the proposed PMS. Hence, this paper presents the system operation with PV variations and load disturbances to validate the performance of CL and NCL. The simulation study is experimentally validated in real-time using OP4510 RTS simulator.

6.1. Performance under CL Variation. Experimental results of DC bus voltage and ShDCES current, CL current, NCL current, ShDCES power, PV power, NCL power, and CL power are depicted in Figure 10. As presented in the simulation study, PV power, CL power, and ShDCES power are 265 W, 400 W, and 135 W, respectively. According to the PMS, the NCL remains inactive. CL power is reduced to 200 W at t₁ to analyze DCMG performance. According to the PMS, the NCL is activated because the load demand is less than 20% of the rated load as depicted in Figure 10(b). CL power at t₂ reinstates to 400 W. In this case, the NCL is deactivated according to the PMS, and ShDCES begins to supply the power difference to maintain critical load voltage stability. In all of the above cases, the DC bus voltage is regulated at 48 V as depicted in Figure 10(a).

6.2. Performance under PV Irradiance Variation. PV irradiance was increased at t₃ and t₄ to check PMS. PV power increased from 265 W to 420 W as depicted in Figure 10(c).
CL and NCL work simultaneously as the NCL demand is less than 20%, and ShDCES provides additional current to the NCL as depicted in Figure 10(a). The battery life of the battery improves as the charge/discharge power of the ShDCES battery decreases. At t₄, PV generation again increased from 420 W to 500 W, and PV power meets CL and NCL requirements as depicted in Figure 10(d). In all the aforementioned scenarios, the CL voltage is kept constant, and the ShDCES balances the maximum power generated by PV and load demand. The real-time manipulation of the NCL reduces the battery’s charge/discharge rate and thereby increases battery cycle life.

7. Conclusions

The rapid increase in electronic loads, renewable generation power units, and electric vehicles has created a galaxy of opportunities for the DCMG to play a critical role in future power supply. The combination of nonlinear loads and renewable sources contributes to the power quality and stability issues in DCMG. The proposed controller design and PMS presented in this paper ensure DC bus voltage stability, regardless of source fluctuations and load disturbances with a better dynamic response compared to the conventional controller. The proposed PMS aids in extending the cycle life of the battery by decreasing its charge/discharge rate, thereby reducing the environmental concerns in DCMG to a certain extent. Improved DC bus voltage stability is also achieved with the new controller design. Both simulation and real-time validation of results using the OP4510 RTS simulator prove the credibility of the suggested controller and PMS.

Data Availability

There are no new data generated in this work. Data used are available openly and cited properly. Moreover, the new findings in this work are kept open.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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