On Fault-Tolerant Design of Exclusive-OR Gates in QCA

Dharmendra Kumar, Debasis Mitra
Department of Information Technology
National Institute of Technology, Durgapur-713209, India

Bhargab B. Bhattacharya
Advanced Computing and Microelectronics Unit
Indian Statistical Institute, Kolkata-700108, India

Abstract
Design paradigms of logic circuits with Quantum-dot Cellular Automata (QCA) have been extensively studied in the recent past. Unfortunately, due to the lack of mature fabrication support, QCA-based circuits often suffer from various types of manufacturing defects and variations, and therefore, are unreliable and error-prone. QCA-based Exclusive-OR (XOR) gates are frequently used in the construction of several computing subsystems such as adders, linear feedback shift registers, parity generators and checkers. However, none of the existing designs for QCA XOR gates have considered the issue of ensuring fault-tolerance. Simulation results also show that these designs can hardly tolerate any fault. We investigate the applicability of various existing fault-tolerant schemes such as triple modular redundancy (TMR), NAND multiplexing, and majority multiplexing in the context of practical realization of QCA XOR gate. Our investigations reveal that these techniques incur prohibitively large area and delay and hence, they are unsuitable for practical scenarios. We propose here realistic designs of QCA XOR gates (in terms of area and delay) with significantly high fault-tolerance against all types of cell misplacement defects such as cell omission, cell displacement, cell misalignment and extra/additional cell deposition. Furthermore, the absence of any crossing in the proposed designs facilitates low-cost fabrication of such systems.

Keywords: Quantum-dot cellular automata, fault-tolerance, Exclusive-OR (XOR Gate)

1. Introduction
Having matured over around six decades, CMOS technology is now expected to reach its physical limit in the near future [1]. The never-ending quest for smaller computing devices has driven the research on alternative nanotechnologies. Quantum-dot Cellular Automata (QCA) [2] has emerged as a possible option in recent years. In QCA, information flows through basic elements (referred to as cells) not by actual flow of current, as in conventional CMOS based designs, but by coulombic interactions between electrons present in neighboring cells resulting in very low power dissipation [2]. Other promising features of QCA technology include high device packing density, high speed (in order of THz), inherent pipelining [3]. Implementations of basic logic devices in QCA have been demonstrated [3]. Design and simulation of common digital modules (both combinational and sequential) have been studied extensively [1, 3, 4, 5, 6, 7, 8, 9, 10].

As in other nanotechnologies, QCA-based circuits often suffer from various types of manufacturing defects [10]. Experimental studies revealed that cell misplacement defects are the most common among all such defects [12]. Several types of cell misplacement defects viz. cell displacement, cell misalignment, cell omission have been reported in the literature so far [12]. Hence, low-cost fault-tolerant designs for such defects are needed. Fault-tolerance and thermal characteristics of fundamental QCA logic devices have been analysed by Anduwan et al. [13]. Errors due to random clock shifts in QCA circuits have been studied by Karim et al. [14]. Ma et al. [10] presented a comparative study on the applicability of a few generic fault-tolerant schemes such as triple modular redundancy (TMR) [15], NAND multiplexing [16], and majority multiplexing [17] in the context of reliable realization of QCA systems. A few new fault-tolerant QCA designs of majority gates and adders have been reported in the literature [12, 13, 14, 15, 16, 17, 18, 19].

An Exclusive-OR (XOR) gate is a digital logic gate that results a true output (logic 1) if one, and only one, of the two inputs of the gate is true. The associative nature of the exclusive-OR function implies the possibility of using exclusive-OR gates with three or more inputs. The exclusive-OR operation with three or more variables can be defined as an odd function where the output assumes logic value 1 if an odd number of variables be equal to 1
XOR gates are often considered as important modules in digital circuit design due to their frequent use in the construction of several computing subsystems such as adders, linear feedback shift registers, parity generators, parity checkers, decoders for error correction and channel codes [23]. An XOR gate with three or more inputs is usually constructed by appropriately connecting two or more 2-input XOR gates only. However, as described in [24]. XOR gates with four or higher inputs can be efficiently constructed with the help of 2-input and 3-input XOR gates.

Several designs for 2-input QCA XOR gates have been presented in recent past [25, 26, 27, 28, 29, 30]. A multilayer 2-input XOR design is also given as sample file in QCADesigner version 2.0.3 [31]. A few 3-input XOR gate designs have also been presented recently [32, 33]. But, both of them have used 2-input XORs and hence shows very poor performance in terms of design parameters such as latency and area. Most importantly, to the best of our knowledge, none of the XOR designs (both 2-input and 3-input) considered fault-tolerance. Again, wire crossing (coplanar or multi-layer), inherent to some of these designs, make them difficult to realize in practice [34].

In this paper, we investigate the applicability of various existing fault-tolerant schemes such as TMR, NAND multiplexing, and majority multiplexing in the context of practical realization of QCA XOR gate. Our investigations reveal that the XOR-function realized under these fault-tolerant schemes requires a large number of cells thereby showing a very poor fault-tolerance vs. area trade-off. Additionally, these designs demand a large number of clock zones leading to higher delay, which is unacceptable for practical realizations. For example, best existing design of 2-input QCA XOR gate [25] requires 249 to 529 cells and 6 to 8 clock zones when the above mentioned fault-tolerant schemes are applied on it. In order to overcome the above shortcomings, we propose new designs of 2-input and 3-input XOR gates in QCA that attain significantly high fault-tolerance with respect to all types of cell misplacement defects. The proposed XOR designs requires 85 and 124 QCA cells for 2-input and 3-input respectively and hence show significantly better fault-tolerance vs. area trade-off than all the existing designs of QCA XOR gates. Furthermore, the absence of any wire crossing (coplanar or multi-layer) in the proposed designs facilitates low cost fabrication. Simulation results are presented based on semiconductor implementation of QCA with an intermediate dot size of about 5nm.

The rest of the paper is organized as follows. Background and related prior work is discussed in Section 2. Section 3 demonstrates the applicability of TMR, NAND-multiplexing and majority-multiplexing on existing QCA XOR gates. Design and simulation of the proposed fault-tolerant 2-input and 3-input XOR gates are presented in Section 4. Detailed comparative study between the proposed XOR gates and the existing ones against various cell misplacement defects is presented in Section 5. Conclusions are drawn in Section 6.

2. Background and Related Prior Work

The basic element in QCA technology is referred to as cell. A QCA cell consists of four potential wells or dots located at the four corners of a square. There are two extra electrons which can tunnel quantum mechanically from one dot to another. Due to coulombic repulsion between these two electrons, they always occupy diagonally opposite corner dots. This results in two possible orientations, referred to as polarizations \( p \). Fig. 1(a) and Fig. 1(b) show QCA cells with \( p = +1 \) and \( p = -1 \) respectively. These two polarization states are used to represent binary information 1 and 0 respectively.

![Figure 1: QCA cell with (a) \( p = +1 \) and (b) \( p = -1 \)](image)

Majority voter (MV) and inverter gates are considered as the two most fundamental building blocks of QCA. A variety of MVs and inverter gates have been reported in the literature [3, 20, 21]. Typical designs of MV and inverter are shown in Fig. 2(a) and Fig. 2(b) respectively. Two types of QCA wires namely binary wire and inverter chain are shown in Fig. 3(a) and Fig. 3(b) respectively.

![Figure 2: Fundamental Gates in QCA (a) Majority Gate (b) Inverter](image)

![Figure 3: Wires in QCA (a) Binary Wire (b) Inverter Chain](image)

To apply input to a logic device, input cell(s) are forced to assume a particular state by applying external electric field. The input cell(s) then interact with its neighboring cells and change their polarization states accordingly. The process continues and finally the output cell assumes the desired state. Note that the magnitude of the Coulomb force decreases with respect to distance and time. A four-phase clocking scheme [22] is used to synchronize and control the information flow.
For the last two decades, a major part of the research on QCA has focused on the design and simulation of various digital modules. Designing different types of adders \[^{4, 6, 20}\] have received considerable interest due to their importance in a computing system. A conceptual design of QCA XOR gate was first presented in \[^{3}\]. Note that a straightforward realization of the design is not possible since it does not consider clocking. A number of QCA implementations of 2-input XOR gate have been presented so far \[^{25, 26, 27, 28, 29, 30, 31}\]. A few 3-input QCA XOR gate designs have also appeared in the recent literature \[^{32, 33}\]. The designers have used a number of metrics such as area, latency, number of cells, and the type of crossovers. The summary of a comparative study considering these metrics is presented in Section 4 (Table 2 and Table 3). It is apparent that all the existing designs of 2-input XOR gates show more or less similar performances in terms of number of cells, area and latency with the design proposed by Ahmad and Bhat \[^{25}\] seems to be the best. For 3-input XOR, the design presented in \[^{32}\] outperforms both the designs presented in \[^{32, 33}\]. Interestingly, none of these XOR designs has considered fault-tolerance. Considering the importance of XOR module in digital circuit design, we analyse the degree of fault-tolerance of these designs. Simulation results (Section 5) show that all of them perform very poorly against most of the cell misplacement defects. This fact motivate us to investigate the applicability of various existing fault-tolerant schemes in the context of practical realization of QCA XOR gate.

### 3. Applicability of Generic fault-tolerant Schemes on Existing QCA XOR Gates

Fault-tolerance of digital circuits is often achieved by adding redundancy into the original design. Triple modular redundancy (TMR) \[^{15}\] and NAND multiplexing \[^{16}\] are the two most popular classical generic fault-tolerance schemes that are often employed to increase the reliability of a circuit module. Recently, a new adaptation of NAND multiplexing referred to as majority multiplexing \[^{17}\] has appeared to be a better alternative for nanotechnologies. In this section, we investigate the applicability of TMR, NAND multiplexing, and majority multiplexing in the context of practical realization of fault-tolerant QCA XOR gate.

In a TMR system, the original circuit module is triplicated where the three copies perform the same task in parallel with corresponding outputs being compared through a majority voter circuit. Fig. 4 shows the block diagram of a TMR system for a 2-input XOR gate. TMRs can be cascaded to further improve the system’s reliability at the cost of higher redundancy. The basic idea behind NAND multiplexing is to replace the original module by a multiplexing unit, which has N copies of every input and output of the original unit. The multiplexing unit randomly permutes the input signals producing N outputs in parallel.

![Block diagram of a TMR system for an XOR gate](image1.png)

Fig. 4: Block diagram of a TMR system for an XOR gate

Although, the generic fault-tolerant techniques discussed above can tolerate a variety of faults (including cell misplacements), the degree of redundancy is unacceptably high. For example, a single stage TMR system for the
best 2-input XOR gate identified in Section 4 requires minimum 249 QCA cells. Moreover, the fault-tolerance of the TMR system strongly depends on the fault-tolerance capability of the majority gate. Use of a fault-tolerant majority gate may add up more overhead (22 more cells). The situation become even worse in the case of NAND multiplexing and majority multiplexing. Construction of a NAND multiplexing system (Fig. 5) for the same XOR gate requires minimum 529 cells. Similarly, a majority multiplexing system (Fig. 6) requires minimum 523 cells. High degree of redundancy involved in all the three systems makes them impractical to realize from both the point of views of area and latency. The above observations (summarized in Table 1) motivate us to design two new practically realizable (in terms of area and delay) fault-tolerant XOR gates which are presented in the next section.

Table 1: Area and latency incurred by generic fault-tolerant techniques applied on a 2-input QCA XOR gate.

| Technique   | Min. #cells | Min. Area ($\mu m^2$) | Latency (clock phases) | Crossover |
|-------------|-------------|-----------------------|------------------------|-----------|
| TMR         | 249         | 0.30                  | 6                      | Yes       |
| NAND-MUX    | 529         | 0.53                  | 8                      | Yes       |
| MAJ-MUX     | 523         | 0.40                  | 8                      | Yes       |

4. Proposed Fault-tolerant XOR Gate Designs

As mentioned in Section 1, exclusive-OR operation with two or more variables act as key elements in designing many digital computing subsystems such as adders, linear feedback shift registers, parity generators and checkers etc. In general, an $n$-variable exclusive-OR function is an odd function defined as the logical sum of the $2^n$ minterms whose binary numerical values have an odd number of 1s. In conventional CMOS based designs, an XOR gate with three or more inputs is usually constructed by appropriating connecting two or more 2-input XOR gates only. However, a closer look reveals that this approach, especially for QCA based design, may lead to larger area and delay. Feinstein and Thornton have shown how XOR gates with four or higher inputs can be efficiently constructed with the help of 2-input and 3-input XOR gates only. Fig. 7 shows few examples demonstrating the idea. This motivates us to propose fault-tolerant designs of 2-input and 3-input XOR gates in QCA.

The logical expression representing 2-input XOR function $(A\bar{B} + \bar{A}B)$ can be rewritten equivalently as $(\bar{A} + \bar{B}) + AB$ using simple Boolean algebra. As mentioned in Section 2, majority gate and inverter pair are commonly used as the basic building blocks in QCA circuits. Note that a majority gate acts as an AND gate when one of its input cell polarization is set to -1 (logic 0). Similarly, it acts as an OR gate when one of its input cell polarization is set to +1 (logic 1). A NOR gate may be implemented by adding an inverter gate in front of an OR gate. Hence, considering Majority voter and inverter based synthesis (which suits QCA based implementation), the above expression may also be rewritten as $M[M(A, B, 1), M(A, B, 0), 1]$, where $M(a, b, c)$ represents the majority function defined as $M(a, b, c) = ab + bc + ac$. Figure 8 shows the gate level implementation of the expression.

Following a similar approach, the logical expression representing 3-input XOR function $(\bar{A}\bar{B}C + \bar{A}BC + AB\bar{C} + ABC)$ may be rewritten as $M[M(A, B, C), C, M(A, B, C)]$. Figure 9 shows the corresponding gate level implementation.

The logical expression representing 2-input XOR function $(A\bar{B} + \bar{A}B)$ can be rewritten equivalently as $(\bar{A} + \bar{B}) + AB$ using simple Boolean algebra. As mentioned in Section 2, majority gate and inverter pair are commonly used as the basic building blocks in QCA circuits. Note that a majority gate acts as an AND gate when one of its input cell polarization is set to -1 (logic 0). Similarly, it acts as an OR gate when one of its input cell polarization is set to +1 (logic 1). A NOR gate may be implemented by adding an inverter gate in front of an OR gate. Hence, considering Majority voter and inverter based synthesis (which suits QCA based implementation), the above expression may also be rewritten as $M[M(A, B, 1), M(A, B, 0), 1]$, where $M(a, b, c)$ represents the majority function defined as $M(a, b, c) = ab + bc + ac$. Figure 8 shows the gate level implementation of the expression.

Figure 8: Gate level implementation of the proposed 2-input XOR gate

Figure 9: Gate level implementation of the proposed 3-input XOR gate

Figure 10: Layout of the proposed 2-input XOR gate

Figure 11: Layout of the proposed 3-input XOR gate

As apparent from the figures, the proposed designs consist of 85 QCA cells and 124 cells respectively. Assuming QCA cell size of $18\times 18\, nm$ with a gap of $2\, nm$ between two consecutive cells, the layouts consume area $0.08\, \mu m^2$ and $0.10\, \mu m^2$.
respectively. Moreover, both the designs use 5 phases (1.25 clock cycles) of clock latency and have no crossover. Note that a number of redundant cells have been used in the basic building blocks (majority gates, inverters, and connecting wires) of both the designs to improve the fault-tolerance potential of the designs against various types of cell omission and cell misplacement defects.

To verify the functional behavior of the proposed XOR gates, we carried out simulations with bistable simulation engine of QCADesigner [31] (version 2.0.3) with the following parameters: (i) Cell size: 18nm × 18nm with a gap of 2nm between two consecutive cells, (ii) Radius of effect: 65nm, (iii) Relative permittivity: 12.9, (iv) Convergence tolerance: 0.001000, (v) Number of samples: 50000, (vi) Intermediate dot size: 5nm. The bistable simulation engine of QCADesigner uses intercellular Hartree approximation (ICHA) assuming a simple two-state system to represent each QCA cell. A little compromise in accuracy as compared to full-basis computation is often compensated by the significantly better scalability [36]. ICHA is found to be valid and sufficient for verifying the functionality of large QCA circuits. The simulation output of QCADesigner is shown in Figure 12 and Figure 13 for 2-input and 3-input XOR gates respectively. Note that the maximum polarization at the 2-input XOR output ($P_{max} = 0.984$) and at the 3-input XOR output ($P_{max} = 0.985$) are significantly strong. To verify the robustness of the proposed XOR gates further, we have also simulated it for various values of radius of effect (for example, 40nm or 75nm). The behavior of the proposed XORs is found to remain unaltered. The maximum polarization at the output remains almost same.
comparative study with existing designs. The summary of the comparative study separately for 2-input and 3-input QCA XOR designs are shown in Table 2 and Table 3 respectively. It is interesting to note that the proposed 3-input XOR gate outperforms all the existing 3-input XOR designs in terms of the above metrics. Although, the proposed 2-input XOR design cannot outperform the existing designs in terms of these metrics but it does not compromise much too for most of them. The number of cells used (and hence the area) by the proposed 2-input XOR gate is higher than the most of the existing 2-input XOR designs. However, as described in the next section, the degree of fault-tolerance achieved by the proposed design leads to a significantly better fault-tolerance vs area trade-off as compared to other designs. In fact, fault-tolerance of the proposed designs against cell misplacements is achieved at the cost of redundancy (increased number of cells).

Table 2: Comparisons of various 2-input QCA XOR gates in terms of common design metrics

| XOR Structures | No. of #cells | Area (µm^2) | Latency (clock phases) | Crossover |
|---------------|--------------|------------|-----------------------|-----------|
| 27            | 58           | 0.062      | 3                     | None      |
| 26            | 42           | 0.036      | 3                     | None      |
| 29            | 41           | 0.044      | 4                     | None      |
| 30            | 62           | 0.090      | 6                     | None      |
| 28            | 35           | 0.040      | 3                     | None      |
| 25            | 32           | 0.030      | 3                     | Multilayer |
| 31            | 85           | 0.078      | 4                     | Multilayer |
| Proposed      | 85           | 0.078      | 5                     | None      |

Table 3: Comparisons of various 3-input QCA XOR gates in terms of common design metrics

| XOR Structures | No. of #cells | Area (µm^2) | Latency (clock phases) | Crossover |
|---------------|--------------|------------|-----------------------|-----------|
| 32            | 98           | 0.12       | 8                     | Coplanar  |
| 33            | 164          | 0.22       | 10                    | Coplanar  |
| 34            | 136          | 0.18       | 9                     | Coplanar  |
| Proposed      | 124          | 0.10       | 5                     | None      |

5. Comparison of proposed XOR gates with existing XORs in terms of fault-tolerance

In this section, we demonstrate the degree of fault-tolerance achieved by our proposed XOR gates against different cell misplacement defects and also present a detailed comparative study with the existing XOR designs in this regard. Although none of the existing XOR designs consider fault-tolerance, we reproduce them [25, 26, 27, 28, 29, 30, 31, 32, 33], and simulate them with bistable simulation engine of QCADesigner [31] (version 2.0.3) to perform the above mentioned comparative study. Note that Shin et al. have proposed two 3-input XOR gates in [33]. In this comparative study, we have included the best one (in terms of common design metrics identified in the previous section).

First, we simulate all the XOR gates including the proposed ones for single-cell omission defects at all the device cells (excluding the input/output cells and the cells with fixed polarization). For the proposed 2-input XOR gates, out of 79 device cells omission of 73 of them produce correct output, thereby achieving 92.41% (73/79 x 100%) fault-tolerance. For the proposed 3-input XOR gates, out of 120 possible instances of single-cell omissions, correct output is produced for 112 cases, thereby achieving 93.33% fault-tolerance. The summary of comparison is illustrated in Figure 14 and Figure 15 with the help of bar charts. It is apparent that both the proposed XOR designs outperform their existing counterparts.

We also inspect the effect of double-cell omissions on the functional behavior of the proposed XOR gates. The output of the proposed 2-input XOR gate...
achieved 95% fault-tolerance via 111 possible instances of extra cell depositions, thereby achieving 96% fault-tolerance.

Input XOR gates against single-cell omission defect

Figure 14: Comparison of fault-tolerance of various 2-input XOR gates against single-cell omission defect

Figure 15: Comparison of fault-tolerance of various 3-input XOR gates against single-cell omission defect

Figure 16: Comparison of fault-tolerance of various 2-input XOR gates against double-cell omission defect

Figure 17: Comparison of fault-tolerance of various 3-input XOR gates against double-cell omission defect

is found to produce correct output for 107 cases out of total 111 possible instances of extra cell depositions, thereby achieving 96.40% fault-tolerance. Similarly, the output of the proposed 3-input XOR gate is found to produce correct output for 125 cases out of total 131 possible instances of extra-cell depositions, thereby achieving 95.42% fault-tolerance. The comparison of fault-tolerance achieved by various XOR gates (existing and proposed) against extra-cell deposition defects is illustrated in Figure 18 and Figure 19.

Finally, we explore the effect of cell displacement and cell misalignment defects on the functional behavior of the proposed XOR gates and all other existing XOR gates. Displacement or misalignment larger than a critical value (referred to as permissible displacement) of a cell in a particular direction causes the circuit to malfunction [20].

Figure 18: Comparison of fault-tolerance of various 2-input XOR gates against extra-cell deposition defect
Larger is the value of permissible displacement associated with a cell displacement/misalignment defect, the circuit is expected to have better fault-tolerance against that defect. The percentage of defects having permissible displacements more than a certain value could be a measure of fault-tolerance of the design against such defects. We simulate all the XOR designs to find out the percentage of such defects having permissible displacements greater than certain values. Table 4 and Table 5 show the percentage of defects having permissible displacements greater than 10nm (i.e., more than half the width of a QCA cell), 20nm (i.e., more than the width of a QCA cell) and 500nm for various 2-input and 3-input XOR gates. For better illustration, we have also included bar charts to present the comparison (Figures 20 and 21). It is apparent that the proposed XOR gates completely outperform all the existing ones in terms of fault-tolerance against cell displacement and cell misalignment defects as well. A significant percentage (88.54% and 34.78% respectively) having permissible displacements more than 500nm for the cell displacement/misalignment defects in the proposed 2-input and 3-input XOR gates indicates that the complete removal of the corresponding cell from the design area does not have any effect on the functional behavior of the circuit. In other words, the proposed design contains a large number of redundant cells. In fact, the presence of redundant cells play a major role in achieving higher degree of fault-tolerance against cell omission defects.

A consolidated summary of our comparative study on fault-tolerance of various 2-input and 3-input XOR gates (including the proposed XOR gates) against various cell misplacement defects is shown in Table 6 and Table 7.

6. Conclusions

Design of effective fault-tolerant schemes are desirable for reliable realization of various digital modules in QCA.
XOR gates are found to be one of the important components used in the construction of several computing subsystems. The applicability of popular fault-tolerant schemes such as TMR, NAND multiplexing, and majority multiplexing in the context of practical realization of QCA XOR gate has been investigated and is observed to perform poorly. In order to bridge the gap a new fault-tolerant design of QCA XOR gates have been presented. Simulation results show that the proposed designs achieve significantly high fault-tolerance against various cell misplacement defects and completely outperform existing counterparts in this regard. Absence of any crossover in the physical layout of the proposed gates further enhances practical realizability of the designs.

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