Gate current degradation in W-band InAlN/AlN/GaN HEMTs under Gate Stress

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Abstract—Schottky gate degradation of W-band InAlN/AlN/GaN high-electron-mobility transistors (HEMTs) has been studied under prolonged positive gate stress. Two different degradation mechanisms have been identified. In an early stage, a gate leakage current increase takes place without any observable drain current nor source and drain resistance degradation. We propose electric field induced trap generation in the AlN barrier layer as the cause. Under harsher gate stress, a second degradation mechanism kicks in where gate leakage current, as well as drain current and the source and drain resistances degrade significantly. We attribute this to Schottky barrier degradation due to severe local self-heating.

Index Terms—InAlN/AlN/GaN, trap generation, self-heating, Schottky gate breakdown.

I. INTRODUCTION

Ever since GaN High-Electron-Mobility-Transistors (HEMTs) became commercially available about a decade ago, the market for GaN RF power amplifiers has grown rapidly. Recently, there has been strong interest in InAlN/AlN HEMTs fabricated on SiC substrates for millimeter-wave applications. This is a result of their excellent gate length scaling potential which stems from the high spontaneous polarization of InAlN and yields a large two-dimensional electron gas (2DEG) density at the InAlN/GaN interface even with a very thin barrier layer [1].

Recent technology improvements have enabled ultrascaled InAlN/GaN HEMTs with $f_T$ of 400 GHz by minimizing parasitic effects as reported in [1]. In addition, InAlN/AlN HEMTs with high drain current (more than 1.2 A/mm), high breakdown voltage (73 V), and simultaneous high $f_T$ (113 GHz) and $f_{\text{max}}$ (230 GHz) have been reported [2]. Furthermore, InAlN/GaN HEMTs with a low ohmic contact resistance of 0.36 $\Omega \cdot \text{mm}$ have also been realized [3]. All these results demonstrate the potential of InAlN as a barrier material for ultra-high-frequency power amplifier applications.

However, in nanometer-scale InAlN/GaN HEMTs, the use of a very thin barrier layer also brings leakage current and reliability concerns to the fore. In typical designs, the absence of a dielectric in the gate stack implies that gate leakage current is relatively large. In addition, the high dislocation density of GaN heterostructures grown on Si or SiC means that defect-related charge transport mechanisms such as Poole-Frenkel emission and trap-assisted-tunneling can become dominant in the gate leakage current [4]–[6]. Research focusing on suppressing the thermionic emission portion of the gate leakage by improving material properties as well as using metals with large work functions has been going on for some time. However, up till now, there has been no single good solution. This is partly due to the fact that charge transport mechanisms as well as gate stack degradation mechanisms are not well understood.

It has been reported that in AlGaN/GaN HEMTs, under OFF-state stress, time-dependent defect generation in the AlGaN barrier layer can result in increase of gate leakage [7]. Recently, under forward gate stress, time-dependent defect generation in the gate stack of p-GaN gate AlGaN/GaN HEMTs has also been observed [8]. Despite progress in understanding leakage current issues in the AlGaN/GaN system, so far, to our knowledge, there are no studies that have focused on the degradation mechanisms related to the gate region of InAlN/GaN HEMTs under positive gate stress. Developing an understanding of these issues is the motivation for our work.

This manuscript presents a study of reliability of InAlN/AlN/GaN HEMTs with emphasis on positive gate stress conditions. Under prolonged mild forward gate stress, we have observed the creation of a gate leakage path which we believe to be a result of defect generation in the AlN layer. Under harsh forward gate stress, on the other hand, we observe not only gate leakage path creation but also source resistance ($R_S$) and drain resistance ($R_D$) increases as well as drain current degradation. We attribute this to significant local self-heating-induced Schottky barrier degradation.

II. DEVICES AND STEP-STRESS EXPERIMENTS

The devices studied here are industrially prototyped InAlN/AlN/GaN HEMTs with $L_G = 40$ nm fabricated on a SiC wafer. Enhancement-mode is achieved through gate recessing of the entire InAlN layer leaving only a 1 nm AlN barrier between the GaN channel and the gate metal.

Previously we have shown that under high-$V_{DS}$-high-$I_D$ stress, significant degradation of the gate current takes place during the first few tens of seconds [2]. Additionally, we found that, unlike in conventional AlGaN/GaN devices where the barrier is relatively thick, the stress-induced leakage path appears on the source side [9]. This is unexpected particularly in light of conventional AlGaN/GaN HEMTs with a thicker barrier layer for which drain-side degradation dominates under
similar stress conditions [10]–[12]. After analyzing the difference in terms of stress conditions on the source and drain sides, we postulated a defect formation degradation mechanism caused by high electric field across the 1 nm AlN layer on the source side together with high \( I_{G_{stress}} \) (through the source side) coupled with significant self-heating [9].

To further our understanding of this degradation mode, in this work we have conducted several gate stress experiments under \( V_{DS} = 0 \) V bias. This ensures a simpler symmetric stress condition.

In a first assessment, we have carried out a step-stress-recovery experiment with \( V_{DS_{stress}} = 0 \) V and \( V_{GS_{stress}} \) increasing from 0.1 to 2.5 V in 0.1 V steps at room temperature (RT). The stress and recovery times corresponding to each stress step are both 5 minutes.

Shown in Fig. 1 is the time evolution of drain resistance \( R_D \) (a), gate current during stress \( I_{G_{stress}} \) (a inset), and OFF-state gate current \( I_{Goff} \) (at \( V_{GS} = -2 \) V and \( V_{DS} = 0.1 \) V). \( R_S \) behaves similarly to \( R_D \) and is not shown here. From Fig. 1(a) inset, we noticed that as \( V_{GS_{stress}} \) reaches 2.3 V, there is visible degradation of the stress bias current \( I_{G_{stress}} \) under constant voltage conditions. \( R_D \) (Fig. 1(a)) starts to degrade at a similar critical stress voltage, that is when \( V_{GS_{stress}} \) exceeds 2.3 V. \( I_{Goff} \) on the other hand, starts to increase at an earlier stage when \( V_{GS_{stress}} \) exceeds about 1.7 V (Fig. 1(b)). An acceleration in \( I_{Goff} \) degradation occurs later at \( V_{GS_{stress}} = 2.3 \) V. The saturation drain current \( I_{D_{max}} \) (at \( V_{GS} = 2 \) V, \( V_{DS} = 4 \) V) also exhibits fast degradation as \( V_{GS_{stress}} \) exceeds 2.3 V (not shown), in agreement with \( R_D \) degradation.

For \( V_{GS_{stress}} \) less than 2.3 V during recovery (pink points in Fig. 1), \( R_D \) almost recovers completely during each recovery period following stress. \( I_{Goff} \) on the other hand, recovers largely but not fully especially for \( V_{GS_{stress}} \) higher than about 2 V. This is also an indication of trap generation. As \( V_{GS_{stress}} \) exceeds 2.3 V, both \( R_D \) and \( I_{Goff} \) show only partial recovery. These results suggest the existence of two mechanisms: a first one causing the initial increase in \( I_{Goff} \) and a second one leading to further rapid \( I_{Goff} \) increase, \( I_{D_{max}} \) decrease, as well as \( R_D \), and \( I_{G_{stress}} \) increases.

At the end of the experiment, in order to separate permanent and recoverable degradation, we conducted a thermal detrapping step designed to detrap all electrons and reveal permanent degradation [9]. The red dots in Fig. 1 (a) and (b) represent measured values after thermal detrapping. Both \( R_D \) and \( I_{Goff} \) recovered by a considerable amount though not completely, indicating the coexistence of trapping related degradation and permanent degradation. Fig. 2 shows the transfer characteristics before and after the experiment with the device fully detrapped. In this figure we see that in addition to severe \( I_{Goff} \) degradation, there is significant permanent degradation of \( I_{D_{max}} \) in the ON regime, as well as a permanent positive \( V_T \) shift.

To understand the role of temperature, we then conducted a high temperature (\( T_{stress} = 150^\circ C \)) step-stress experiment, again with \( V_{DS_{stress}} = 0 \) V and \( V_{GS_{stress}} \) increasing from 0.1 to 2.5 V in 0.1 V steps. The stress time during each step is 1 minute.

![Figure 1. Degradation of (a) \( R_D \) (measured with gate current injection method [5] with \( I_{inj} = 20 \) mA/mm) and \( I_{G_{stress}} \) (inset) (b) \( |I_{Goff}| \) (at \( V_{GS} = -2 \) V, \( V_{DS} = 0.1 \) V) as a function of stress time in a step-stress-recovery experiment with \( V_{GS_{stress}} > 0 \) and \( V_{DS_{stress}} = 0 \). \( I_{Goff} \) starts to degrade at \( V_{GS_{stress}} = 1.7 \) V. Enhanced \( I_{Goff} \) degradation as well as \( R_D \) and \( I_{G_{stress}} \) degradation happen as \( V_{GS_{stress}} \) reaches 2.3 V.](image)

![Figure 2. \( I_{D_{max}} \) transfers characteristics before and after stress experiment shown in Fig. 1. The device is fully detrapped in both cases. \( V_T \) shifts positive. \( I_{D_{max}} \) drops and OFF-state \( I_D \) increases after stress.](image)

Fig. 3 shows the time evolution of \( R_D, I_{G_{stress}}, \) and \( I_{Goff} \) in a format similar to Fig. 1. This time, under high \( T_{stress}, R_D, R_S \) (not shown), and \( I_{G_{stress}} \) start to degrade at a lower \( V_{GS_{stress}} \) level of about 2 V. \( I_{Goff} \) starts to increase significantly at \( V_{GS_{stress}} \) around 1.4 V. Both critical voltages are lower than
under RT stress, suggesting that both mechanisms are thermally enhanced. At the end of the experiment after thermal detrapping, this device also shows significant permanent ID drop (not shown). VT extraction, however, is no longer meaningful for this device due to excessive leakage current increase under the harsh stress.

Previous studies in AlGaN/GaN HEMTs have shown TDDB-like gate current degradation under OFF-state stress [7], which is believed to be caused by trap generation in the AlGaN barrier under high electric field and high temperature. Moreover, recently, under forward gate stress, time-dependent defect generation in the gate stack of AlGaN/GaN HEMTs with a p-GaN gate has also been observed [8]. In our gate stress experiments, the mechanism associated with the initial IGoff increase is likely due to similar trap generation in the AlN layer. This layer is only 1 nm thick, and at a VGS of around 1.7 V (1.4 V in the high temperature stress experiment), the electric field across it can be very large. Such a condition would favor defect generation in the AlN layer. Also, a lower critical voltage at higher stress temperature is consistent with typical TDDB behavior in Si MOSFETs. In the AlGaN/GaN HEMT system, similar temperature dependence under OFF-state stress has also been reported [13].

The second mechanism, which takes place at higher VGSstress and IGstress values (and thus entails significant local self-heating), might be related to thermally-induced Schottky gate degradation. This is consistent with our previous study on similar devices [14].

### III. CONSTANT GATE STRESS EXPERIMENT

To further our understanding and separate the effects and corresponding signatures of the two degradation mechanisms proposed above, we have designed a RT constant gate stress experiment at a relatively low VGSstress level (2 V) for an extended period of time such that only trap generation in the AlN layer (the first degradation mechanism) is to be expected. Fig. 4 shows the change of RD, IGstress, and IGoff during the experiment.

![Figure 4](image)

**Figure 4.** Degradation of (a) RD and IGstress (inset), (b) IGoff (at VGS = -2 V, VDS = 0.1 V) as a function of stress time in a RT constant gate stress experiment with VGSstress = 2 V and VDSstress = 0 V. IGoff starts to become noisy and degrade at around 500 s. RD and IGstress, on the other hand, do not show significant degradation.

From Fig. 4(a) inset, we notice that unlike the previous two experiments (Figs. 1(a) and 3(a)), where the stress conditions are harsher, IGstress keeps decreasing, possibly due to electron trapping. This is also an indication of the absence of Schottky gate degradation (the second degradation mechanism observed in the previous two experiments). RD throughout the experiment does not change much, which further indicates the lack of the second degradation mechanism under this
relatively low gate stress. In Fig. 4(b), \( I_{G\text{off}} \) becomes noisy close to \( t_{\text{stress}} \) around 500 s and that is also the point beyond which \( I_{G\text{off}} \) starts to increase. This strongly suggests the onset of trap generation.

To see the overall permanent degradation of this device, we again performed thermal detrapping and then characterized the device. Fig. 5 shows that under this stress condition, there is significant increase in the OFF-state drain current which is consistent with the observed \( I_{G\text{off}} \) increase shown in Fig. 4(b). However, there is negligible permanent \( I_{\text{Dmax}} \) and \( V_T \) degradation. This indicates the absence of the second degradation mechanism, as expected.

### IV. THERMAL STRESS

In Section II, we noted an enhancement of the second degradation mechanism under high \( T_{\text{stress}} \). In order to verify the correlation between high junction temperature and the second degradation mechanism, we carried out pure thermal stress experiments on a virgin device.

![Figure 5. \( I_D-V_{GS} \) transfer characteristics before and after stress. OFF-state \( I_D \) increased due to an increased gate leakage. Neither \( I_{\text{Dmax}} \) nor \( V_T \) show significant degradation.](image1)

A virgin device was sequentially annealed at 400 °C and 500 °C for 1 minute each in an \( N_2 \) environment. RT device characterization was carried out before and after stress as well as in between the two thermal stress steps. Fig. 6 shows \( I_D-V_{GS} \) curves of the device before and after thermal stress. Thermal stress results in a reduction in saturation drain current \( I_{\text{Dmax}} \) and a positive shift in \( V_T \). There is only minor degradation of the off-state current. These observations are consistent with the second mechanism identified in the experiments of Figs. 1 and 3. This supports the hypothesis of self-heating induced Schottky gate degradation under strong forward bias gate stress.

### V. GATE CURRENT: DOMINANT CHARGE TRANSPORT MECHANISMS

To understand the dominant charge transport mechanisms related to the gate current, we conducted \( I_G-V_{GS} \) measurements before and after stress in a temperature range from -50 °C to 200 °C in virgin and stressed devices. For the virgin devices, we found that thermionic field emission (TFE) explains well the gate current in the low forward regime (before series resistance effects become important). This is shown in Fig. 7. Here we show a fit of the \( I_G-V_{GS} \) characteristics between -50 °C and 200 °C with an I-V relationship given by

\[
I_{\text{TFE}} = I_s \exp \left( \frac{qV_{GS}}{E_0} \right),
\]

where \( I_s \) is approximated as [15]

\[
I_s = \frac{A \sqrt{\pi E_{00} q (\phi_b - V_{GS})}}{kT \cosh \left( \frac{E_{00}}{kT} \right)} \exp \left[ -\frac{q \phi_b}{E_0} \right],
\]

and

\[
E_0 = E_{00} \coth \left( \frac{E_{00}}{kT} \right),
\]

In these equations, \( \phi_b \) is the effective Schottky Barrier Height (SBH), \( A \) is the classical Richardson constant and the rest of the symbols have their usual meaning. This formulation assumes that the penetration of the Fermi level inside the conduction band is much smaller than \( \phi_b \) which is valid for the low gate bias range studied here.

Experimentally, \( E_0 \) for each temperature can be obtained from the slope of \( \ln(I) \) vs. \( V \) plots (Fig. 7). The obtained values of \( E_0 \) are graphed in Fig. 8 against \( kT \). The full collection of values is well described by (3) with a single value of \( E_{00} = 23 \text{ meV} \), as indicated by the red line. This gives us confidence in the extraction procedure. \( \phi_b \) can then be estimated from the saturation value of \( I_G \), that is, the extrapolation of \( I_G \) to \( V_{GS} = 0 \). By rearranging (2) and taking the natural log on both sides of the equation, we obtain:

\[
\ln \left( I_s kT \cosh \left( \frac{E_{00}}{kT} \right) \right) = \ln(X) - \frac{q \phi_b}{E_0},
\]

with
Here, $X$ is independent of $T$. Using (4), $\phi_b$ can be extracted from the slope of a plot $\ln \left( I_s kT \cosh \left( E_{\infty} / kT \right) \right)$ vs. $1/E_0$, as shown in the inset of Fig. 7. The extracted value of $\phi_b$ is 0.95 eV.

Similar fittings have been performed on several virgin devices. In all cases, the $I_G$-$V_{GS}$ fits are excellent and the extracted SBHs were all around 1 eV.

After a mild constant $V_{GS} = 2$ V stress (device in Fig. 4), we found that the I-V characteristics changed significantly and can no longer be well described by the TFE model. Considering our hypothesis of defect generation in the AlN layer under this mild gate stress, we used a Poole-Frenkel (P-F) emission model [6] which turns out to fit the gate current reasonably well. According to [6],

\[
I_{PF} = CE \exp \left[ -q \left( \phi_f - \sqrt{qE / \varepsilon} \right) / kT \right],
\]

where $C$ is a constant, $E$ is the electric field across the barrier layer, $\varepsilon$ is the permittivity of the barrier at high frequency, and $\phi_f$ is the barrier height for electron emission from the trap state to a continuum of states (conduction band edge or dislocations).

According to (6), by taking the natural log on both sides of the equation, we obtain

\[
\ln \left( I_{PF} / E \right) = m(T) + n(T)\sqrt{E},
\]

where

\[
m(T) = \ln(C) - q\phi_f / kT,
\]

and

\[
n(T) = 1 / kT \sqrt{q / \varepsilon},
\]

From (7), for each temperature, a plot of $\ln \left( I_{PF} / E \right)$ vs. $\sqrt{E}$ should be a straight line from which the intercept to $E = 0$, $m(T)$ can be extracted.

This is indeed the case as illustrate by Fig. 9. Here, we use $V_G$ instead of $E$ since we expect a linear correlation between the two and the threshold voltage is close to 0. From the extracted values of $m(T)$, (8) suggests that a graph of $m(T)$ vs. $1/kT$ should be a straight line with slope -$\phi_f$.

As Fig. 9 (inset) shows, this is indeed the case and a trap energy level $\phi_f$ of around 0.36 eV is derived. This is close to the donor level of N vacancy in AlN of 0.5 eV as reported in the literature [16].

Similar TFE fittings before and after stress were carried out on the $I_G$-$V_{GS}$ characteristics of the device with a severely degraded Schottky junction (device shown in Fig. 1). After stress, as shown in Fig. 10, the temperature and gate bias dependence of the device changed significantly. A similar $I_G$-$V_{GS}$ shape regardless of $T$ indicates a different charge transport mechanism than TFE. Again, in this case, the P-F model reasonably describes the $I_G$-$V_{GS}$ characteristics and yields a trap energy level of about 0.11 eV (Fig. 11) which is much smaller than the previously obtained value of 0.34 eV for the device stressed under mild gate voltage (Fig. 9). This is consistent with a different degradation mechanism dominating the gate current, as postulated above. This extremely shallow energy level also suggests a significantly degraded Schottky junction.
VI. CONCLUSIONS

In summary, we have investigated Schottky gate-related degradation of InAlN/AlN/GaN HEMTs with a very thin barrier layer under forward gate stress. We have identified two degradation modes that are thermally enhanced. A first mechanism leads to an increase of $I_{\text{off}}$ but does not affect saturation drain current (and thus output power). We attribute this to trap generation in the AlN layer similar to dielectric degradation under both positive and negative gate stresses in a Si MOSFET. The second degradation mechanism also results in an increase of $I_{\text{off}}$, and additionally in a drop in saturation drain current, a positive $V_T$ shift, and $R_D$ and $R_S$ increases. We postulate that this is due to Schottky gate degradation as a result of high junction temperature. Our findings are consistent with a source-side degradation mechanism postulated under harsh ON-state stress conditions.

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