Airborne Communication Computer Based on PowerPC+ SRIO Architecture

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Abstract. In order to break through the transmission capacity limitation of airborne computers, an airborne communication computer based on PowerPC+ SRIO Architecture is designed according to the wide application of the SRIO bus and the high performance of the PowerPC processor. In terms of optimization design, the computer adopts a redundant fault-tolerant system and improves the SRIO register initialization and address mapping method. The experimental results show that the transmission speed of the airborne communication computer based on PowerPC+ SRIO architecture reaches 81% of the theoretical value, and 16KBytes data can be transmitted in real time within 1μs.

1. Introduction

With the rapid development of electronic information technology, airborne systems have entered the era of digitalization. Digital computers have gradually replaced analog computers, and their reliability and processing performance have greatly improved the information processing capabilities of the entire aircraft. In recent years, with the rapid development of high-performance processors, to improve the comprehensive processing capabilities of the system, parallel processing of multiple processors has become an effective way. However, real-time processing systems place very high demands on internal data transmission capabilities, and the transmission capability between modules becomes a shortcoming that limits overall performance. Therefore, in addition to focusing on the overall performance and computing power of the processor in the airborne system design [1-2], it is extremely important to study and solve the efficient transmission of data between processors.

At present, the airborne computer information processing system mainly uses the ARM processor architecture [3], and the data transmission between the boards uses the PCM bus interface, which not only fails to meet the requirements of high-performance processing, but also cannot solve the problem of data transmission speed due to bandwidth limitation. The DSP processor uses a single-threaded operation and cannot be well adapted to the real-time operating system [4]. On this basis, some computer information processing systems began to adopt PowerPC computer architecture [5-7], which has significantly improved performance and stability compared with ARM architecture. However, when data is transmitted, the Local bus cannot meet the requirements of high-speed data exchange. Even with the use of PCIe technology, the requirements for high-speed data multi-point switching between boards can not be achieved due to the limitations of the bus architecture. At the same time, the requirements for aircraft are getting higher and higher, and the airborne computer needs to be perfected. Miniaturization, high reliability and high-speed transmission have become essential points in the design process.

Therefore, the article studies the integrated design of airborne communication computer. Firstly, a dual redundant operating system is adopted in the system architecture. [8-10] Secondly, the SRIO
register initialization and address mapping method is improved. Finally, an airborne information processing system based on SRIO [11-13] switching technology is proposed. Based on the PowerPC computing architecture, the system makes full use of the high-speed serial interface SRIO (Serial RapidIO) to achieve efficient data transmission.

2. System architecture of airborne communication computer

As the core part of the airborne electronic system, the airborne communication computer has the characteristics of high real-time performance and large data volume. PowerPC processor with wide application in the military field and good architecture scalability is used in this article. The article selects the P2040 processor which operates in harsh environments from -40 °C to 125 °C. The P2040 single-board ruggedized computer module uses a highly integrated SOC processor with two high-performance Power Architecture e500 cores, DDR3 memory controllers, five MAC controllers, and 10 high-speed SerDes and other common interfaces. In the design of the module, the SerDes interface is configured as one PCIe x1 and one SRIO x4 which is directly exported to the VPX interface as an external high-speed communication port. PCIe x1 is extended to the 32-bit PCI bus used to expand the 1553B avionics port. The three MACs are converted to 1000BASE-T through the PHY for external high-speed communication interface which is led to the VPX connector. Besides, the board has its hardware monitoring function. The hardware monitoring chip is connected through the I2C interface to realize the collection and reporting of the voltage and temperature of the motherboard.

After solving the information processing capability of the system, how to realize high-speed data transmission between P2040 and other boards becomes a key issue that breaks through the system bottleneck. The SRIO bus is based on packet-switched point-to-point transmission interconnect serial architecture with high bandwidth, low latency and low pin count. Since SRIO uses point-to-point technology, a switch is required in the system that requires more than two RapidIO interfaces processing or bridging portions. The system uses Tundra's third-generation switch TSI578 which supports version 1.3 of the RapidIO protocol. It can flexibly supports 16 1X ports or 8 4X ports. The ports are independent of each other with optional baud rates including 1.25Gbit/s, 2.5 Gbit/s and 3.125 Gbit/s. The system uses five ports of TSI578, namely port 2, port 4, port 6, port 8, and port 10. All five ports are configured in 4X mode, and the baud rate is configured to 3.125 Gb/s. In the system Port 2, port 4, port 6, port 8 and port 10 are connected BCU, MCU, IO device 1, IO device 2, and IO device 3 respectively. Before the switch forwards the data packet, the route of the TSI578 should be configured first, the address of the peripheral equipment is shown in Table 1.

| Port | Address | Device               |
|------|---------|----------------------|
| 2    | 0x01    | BCU                  |
| 4    | 0x02    | MCU                  |
| 6    | 0x03    | Function interface board 1 |
| 8    | 0x04    | Function interface board 2 |
| 10   | 0x05    | Function interface board 3 |
To adapt to the application requirements of different models, the airborne communication computer adopts the design idea of combining modularization with building blocks, and divides the internal module of the computer into three parts: computer main module, switching module and interface module. For the miniaturized airborne computer with a simple function, only the main computer module can be used, and the computer with complex functions can make from different number and different types of interface modules. To improve the reliability of the airborne computer, the dual-redundant hot standby mode is used to set two internal motherboard systems of the computer as the MCU system and the BCU system. During the system operation and communication process, the two boards receive data tasks together, and carry out signal transmission. By default, the MCU controls the entire system and is responsible for communicating with the external interface. When there is a problem in the operation of the MCU system, the system is mutually aware through the heartbeat mechanism (through RS422), and the BCU actively takes over the entire system and completes the work of external interface communication and internal computing. The overall architecture of the airborne communication computer is shown in Figure 1.

3. Design and implementation of integrated optimization
In order to solve the limitations of traditional interconnection and meet the needs of embedded systems, the SRIO standard came into being. The standard simplifies the protocol and flow control mechanism, and has significant improvements in packaging efficiency, transmission delay, and scalability. Compared with the PCIe technology adopted at this stage, PCIe unable to meet the requirements of high-speed data multi-point exchange between boards and the establishment of complex high-speed data exchange networks when performing high-speed transmission of data between boards with multiple devices. The system uses SRIO to realize the data transmission of P2040 and other boards by direct point-to-point connection, table 2 compares the overall performance of two high-speed serial buses.
Table 2  Comparison of SRIO and PCIe parameters.

| Feature   | Topology Format | Direct Point to Point | Maximum Payload | Transmission Distance | Transmission Efficiency (<1KB) | Hardware Error Correction | Flow Control | Embedded Link Control Package |
|-----------|-----------------|-----------------------|-----------------|-----------------------|-------------------------------|---------------------------|--------------|-------------------------------|
| SRIO      | Arbitrarily     | yes                   | 256B            | Long                  | High                          | Strong                    | Credit, Retry | yes                           |
| PCI-Express | PCI Tree       | no                    | 4096B           | Medium                | Medium                        | Medium                    | Credit       | no                            |

The SRIO bus uses the format of the packet for data transfer. During the transfer process, the packet exchange technology divides the transmitted information into a series of data packets, including routing, sequence information and data, and then transfers the packets from the source host to the target one by one. This switching strategy can make better use of network resources, and improve the efficiency of data exchange. However, before reading and writing RapidIO information, the hardware configuration for the P2040 and TSI578 is necessary at power-on. This system uses five ports of TSI578, namely port 2, port 4, port 6, port 8, port 10, and all 5 ports are configured in 4X mode, and the baud rate is configured to 3.125Gb/s. After that, the internal register of the TSI578 needs to be further initialized to determine the mapping relationship between the internal SRIO and the external agent address space. Finally, the address space can be directly manipulated by accessing the external memory to complete the read operation and the write operation to each SRIO sub-device. The process is shown in Figure 2.

![Diagram of SRIO Initialization Process](image-url)
In the process of initializing SRIO, the local processor including the entry register, the internal area register, and the three registers of the RapidIO Outbound window is configured firstly. At the same time, the link connection information is obtained by reading the ESCSR register to determine the connection status. Then obtain the device ID of the switch TSI578 through Maintenance read, configure the switch port and routing information, and then search for the SRIO slaves in the system to read the device ID; then enable the external SRIO configuration space, configure the ROKBAR starting address to 0x00C1100, and set the attribute value of the ROWAR window to NWRITE and NREAD. Finally, enable memory reading and writing, after configuring the three registers of the host outbound window, you need to configure the three registers of each slave inbound window, including the RIWBAR setting from the base address of the device, and the RIWTAR setting from the device output. The starting position, RIWAR settings window properties.

4. Test Results
This design is designed for the transmission and communication of real-time data of airborne computers, requiring 5-6Kbytes of data to be transmitted every few microseconds. The computer system uses the SRIO 4X mode to perform data transmission experiments at a rate of 3.125 Gbit/s, the block diagram used in the experiment is shown in Figure 3.

The configuration of the switch TSI578 is implemented by using PowerPC. Three slave SRIO devices are searched through the switch, and initialized respectively. It includes configuration of the Device ID, Outbound registers, SRIO Inbound, and read and write mapping space. After the SRIO configuration is completed, the data is sent to the PowerPC by the host computer network, and the received data is directly transmitted to the three slave devices of the SRIO through memory read and write operations. Data transmission and reception are completed after receiving data from the device. Then the system read the data received by the three devices separately and compare the data. Experiments show that 16KBytes data can be transmitted correctly and in real-time within 1μs using SRIO protocol communication at 3.125Gbit/s.

![Figure 3 Connection Diagram of SRIO Experiment](image)

To test the impact of different size data on the transmission efficiency, perform multiple reciprocating transmission tests on 32B, 512B, 2048B, 32768B, and 65536B data respectively. The test results are shown in Table 3. When the amount of data transmitted is small, the ratio of the transmission rate to the theoretical value is low. In the transmission test, the working efficiency of the interface is set to 3.125 Gbit/s. After the physical layer 8B/10B encoding, the transmission efficiency of the packet is only 2.5 Gbit/s. The theoretical transmission rate is 10 Gbit/s in the 4X transmission mode. When transmitting 32 bytes of data, the ratio of the transmission rate to the theoretical transmission rate is only 1.2%. Most of the time is spent on packing and unpacking the data. As the amount of data continues to increase, the transmission rate of SRIO also increases. When transmitting 65536 bytes of data, the transmission rate reaches 8320 Mbit/s.
Table 3  SRIO Transmission Rate Test for Different Size Data.

| Amount of Data Transferred (B) | Number of Transmission Cycles | Transmission Rate (Mbit/s) | Ratio to Theoretical Value (%) |
|-------------------------------|-------------------------------|---------------------------|-------------------------------|
| 32                            | 24                            | 124                       | 1.2                           |
| 512                           | 725                           | 672                       | 6.6                           |
| 2048                          | 4480                          | 3726                      | 36.4                          |
| 32768                         | 33747                         | 7868                      | 76.8                          |
| 65536                         | 66358                         | 8320                      | 81.2                          |

5. Conclusion
This paper analyzes the design requirements of airborne communication computer and introduces a design method of airborne communication computer based on PowerPC+SRIO architecture. The system adopts the operation mode of dual redundant hot backup and completes the system switching automatically when problems occur. The improvements to the initialization and address mapping of the SRIO registers have been completed. Through the application of PowerPC processor and SRIO switching technology, using SRIO protocol communication at 3.125 Gbit/s, the data transmission speed can reach 81% of the theoretical value, and 16KBytes data can be transmitted correctly in real time within 1μs. SRIO interconnection represents the future development direction of embedded system bus technology. Due to the wide application scenarios of airborne equipment, how to further realize the general design of airborne communication computer still needs more in-depth research.

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