Large-Scale and Robust Multifunctional Vertically Aligned MoS$_2$ Photo-Memristors

Kamalakannan Ranganathan, Mor Fiegenbaum-Raz, and Ariel Ismach*

Memristive devices have drawn considerable research attention due to their potential applications in non-volatile memory and neuromorphic computing. The combination of resistive switching devices with light-responsive materials is considered a novel way to integrate optical information with electrical circuitry. On the other hand, 2D materials have attracted substantial consideration, thanks to their unique crystal structure, as reflected in their chemical and physical properties. Although not the major focus, van der Waals solids are proven to be potential candidates in memristive devices. In this scheme, the majority of the resistive switching devices are implemented on planar flakes, obtained by mechanical exfoliation. Here a facile and robust methodology is utilized to grow large-scale vertically aligned MoS$_2$ (VA-MoS$_2$) films on standard silicon substrates. Memristive devices with the structure silver/VA-MoS$_2$/Si are shown to have low set-ON voltages (~0.5 V), large retention times (~2 $\times$ 10$^5$ s), and high thermal stability (up to 350 $^\circ$C). The proposed memristive device also exhibits long term potentiation/depression (LTP/LTD) and photo-active memory states. The large-scale fabrication, together with the low operating voltages, high thermal stability, light-responsive behavior, and LTP/LTD, make this approach very appealing for real-life non-volatile memory applications.

1. Introduction

The search of materials for robust memory storage has been a prime focus for developing future computing capabilities.[1] Among non-volatile memory storage techniques, the memristor is one of the leading potential candidates for replacing or complementing complementary metal oxide semiconductor technologies.[2] Memristors were found to exhibit multiple analogue states for information processing as well.[3] These makes the memristors a potential candidate for solving the long standing problem known as “memory wall” of the von-Neumann architecture by using data storage and data processing from the same device.[3,4] The standard memristor configuration complies a metal oxide thin film sandwiched between two metal contacts.[2b,5] The resistive switching mechanism in these type of devices depends on the metal contact type and they are classified in two main groups, active, and non-active metal contacts. When the later type of contacts is used (such as gold), the low-resistance mode is achieved by the formation of a conductive path by the migration, and accumulation of oxygen anions.[2a,6] When an “active” metal is used as one of the contacts, such as copper and silver, the high conductance state is reached by the diffusion of Cu or Ag ions to form a conductive filament.[6b] or to reduce locally the resistance across the solid electrolyte, without necessarily forming a continuous metallic wire.[10,20] Both processes are highly stochastic.

Atomic-thin semiconductors, such as the transition metal dichalcogenide (TMDC) family have attracted great scientific, and technological attention due to their interesting physical and chemical properties, which make them promising candidates in a wide range of applications, such as nano-electronics,[7] opto-electronics,[8] catalysis,[9] and energy storage.[9c-e,10] Such atomic crystals were also suggested as solid electrolytes in resistive switching devices.[1a,11] To our knowledge, only planar single- and few-layer 2D materials were implemented into memristor devices with top and bottom metal contacts. Therefore, the conductive path in these cases is formed perpendicular to the basal plane, along defects present in the layers, such as sulfur vacancies. Despite these promising device prototyping, mostly based on mechanically exfoliated flakes, the large-scale single- and few-layer TMDCs formation with the desired homogeneity, as required for the fabrication of such memory devices, is still a great challenge.[12] In addition, making a vertical device with the structure metal–2D material–metal, is prone to malfunction due to electrical leaks caused by intrinsic defects, and the atomic size of such layers. Vertically aligned (VA) TMDCs were shown to be formed by the calchogenization of transition metal thin films or foils.[9a,13] Thin films of VA-MoS$_2$,[9a,10,13a,b] MoSe$_2$,[11b] and WSe$_2$[13c] were reported and their electronic and catalytic properties tested. These films therefore, offer some interesting features, not available on planar few-layer TMDCs. First, the sulfurization/selenization process is scalable, and large-area thin films of VA-TMDCs can be realized in a consistent manner. Second, the VA-TMDC configuration can be advantageous in a vertical memristive device due to the enhanced ionic/cationic diffusion in between vdW layers.[9a,d,e,10] Furthermore, such
VA-TMDCs can in principle be doped/alloyed in situ during the sulfurization process, therefore, adding functionality to the films.[9a,14]

Conventional memristor devices based on a metal oxide thin film as the active layer, are not expected to be light sensitive due to their wide band-gap, and disordered nature (amorphous) of such layers. Therefore, the integration of metal-oxide memristors into light sensitive devices is not feasible. The integration of optical sensing with electrical circuitry is very interesting for future energy-efficient electronic systems.[15] TMDCs-based photodetectors have shown fast response and high sensitivities,[8,15] therefore, allowing to integrate optical sensing, and data storage. Indeed, photo-sensitive memory devices were demonstrated with TMDC-based planar configuration.[15,16] However, as stated above, the vast majority of such reports were performed on exfoliated flakes as proof of concept studies.[15,16] Moving forward to real life applications requires a highly consistent and robust synthetic methodology.

An additional interesting functionality is the ability of electrical components to operate at high temperatures, often defined as higher than 150 °C, as is considered to be the temperature in which electrical performance is highly degraded.[17] To our knowledge, research on high temperature memristor performance is very scarce. For example, the performance at temperatures up to ≈180 °C, and ≈860 °C were tested in resistive switching devices based on SiCN[18] and HfO.[19] thin films, respectively. Graphene/MoS 2–xO x/graphene layered devices were shown to operate up to ≈340 °C.[116] Hence, the development of memristive devices at high operation temperatures are desirable to expand their functionality, and be used in harsh conditions.

In this study we demonstrate the successful fabrication of large-scale VA-MoS2 based memristors with an active metal contact (top contact-Ag) and a heavily doped Si wafer as the bottom electrode. Such resistive switching devices exhibit low SET voltages (<0.5 V) and good stability at high temperatures (up to 350 °C), to our knowledge, the higher measured so far. The Ag/VA-MoS2/Si devices are shown to be light sensitive, thus allowing for future integration between light-stimulation, and data storage. The memristive device also exhibits long term potentiation/depression (LTP/LTD), as needed for neuromorphic computing applications. The work presented here may allow for the large-scale fabrication of functional (photo) resistive switching devices based on VA-TMDCs, with high stability in high temperatures.

2. Result and Discussion

The VA-MoS2 thin films were prepared by the sulfurization of a pre-deposited 15 nm-thick Mo film on Si substrates (see Figure S1, Supporting Information and Experimental Section for details). Here, heavily doped Si wafer was chosen to serve as the growth substrate and the bottom contact without any additional metal fabrication. Prior to the Mo film deposit, the native oxide Si wafer is treated with an HF solution in order to assure no SiO2 is present at the metal evaporation step. Figure 1 shows the film characterization. The in-plane TEM image, Figure 1a, was taken after transferring the MoS2 film to a standard holey carbon TEM grid. The MoS2 standing layered structure is clearly seen. The measured interlayer distance of ≈0.6 nm is consistent with the MoS2 bulk crystal structure.[11a] To visualize the interface between the MoS2 and the Si substrate, as well to further corroborate the vertical alignment of the layers, cross section samples were prepared using focused ion beam (FIB)-related methods, as specified in the Experimental Section. Figure 1b shows the TEM image of such samples, in which the VA-MoS2 is noticed.[11a,15] The final thickness of the film is ≈35 nm, exhibiting a volume expansion of around ≈2.2 from the initial 15 nm Mo film thickness, which is consistent with previous reports.[11a] A thin layer (3–5 nm thick) of SiO2 is also present at the interface between the MoS2 and the Si. The oxygen initially present at the surface of the Mo film and as residual species in the reactor chamber, must diffuse through the metal film, and react with Si, due to its higher oxygen affinity, in the Ellingham diagram comparing between the free energy of formation for the SiO2 and Mo–O phases. Figure S2, Supporting Information. Nevertheless, this oxide layer is expected to have low density and porous structure, since the sulfurization temperature and gas composition does not fit the conditions required for a high quality dielectric layer formation.[20] Hence, the thin, and porous SiO2 interfacial layer is not expected to have a big influence on the memristor behavior. HRTEM (high resolution transmission electron microscopy) analysis in various spots indeed indicates a porous and amorphous with a thickness of less than 5 nm (Figure 1b and Figure S3, Supporting Information). Previous reports on similar VA-MoS2 films confirmed the presence of a layer at the interface as well,[11a,20] Raman spectroscopy, Figure 1c, shows the characteristic MoS2 modes, the in-plane ($E_{2g}^{1}$), and out of plane (A$^{2g}_{g}$) phonon modes were assigned. [9b,22]

The chemical analysis was carried out by X-rays photoemission spectroscopy (XPS). The survey spectrum (Figure S4a, Supporting Information) of the as grown MoS2 shows the coexistence of Mo, S, and O species on the surface of the film. High resolution XPS spectrum (Figure 1d) of Mo 3d was resolved into three peaks. The peaks at 236.2 eV for Mo6+$^{3}d_{3/2}$, 232.5 eV for Mo6+$^{3}d_{5/2}$, and 226.6 eV for Mo4+$^{3}d_{3/2}$ and 226.6 eV for Mo4+$^{3}d_{5/2}$ were assigned.[9b,22] The survey spectrum of an Au+ ion gun sputter cleaned surface (Figure S4b, Supporting Information) indicates a drastic reduction of oxygen on the surface. Moreover, the Mo6+$^{3}d_{3/2}$ peak also vanished (Figure S4c, Supporting Information) after surface cleaning, indicating that the oxide species such as MoO3 is mainly at the surface, and are a result of processing the samples in atmospheric conditions. The S2− 2p (Figure 1e) has been resolved into two peaks at 163.5 and 162.2 eV for 2p1/2 and 2p3/2, respectively. Further, XPS depth profile has been carried out to study the chemical, and phase composition throughout the film. Figure 1f shows the result of such profiling. The system consists of a multi-layer structure of MoS2 on top of a thin coated Si substrate. The high resolution XPS
at the interface between Si and MoS$_2$ is referred to a thin layer of SiO$_2$ without any other phases, such as molybdenum silicide (Figure S5, Supporting Information).

Figure 2 shows the electrical characterization of the VA-MoS$_2$ based memristor. A schematic representation of the measurement set-up is depicted in Figure 2a. Figure 2b,c show the results obtained on a device made with a vertical structure of Au/MoS$_2$/Si. The current–voltage curve in Figure 2b,c exhibit the typical switching characteristics of such device, in which some hysteresis can be observed. On the other hand, a thin layer (30 nm) of Ag deposited in between the Au top contact, and the VA-MoS$_2$ film, changed dramatically the device behavior.
First, a clear electroforming step, at 2.2 V, can be observed, Figure 2d,e, which is a common feature in a memristive device, where the conductive path across the solid electrolyte, the VA-MoS₂, is formed for the first time. The device shows a switching behavior from high-resistance state (HRS, i.e., OFF state) to the low resistance state (LRS, i.e., ON state). Following the electroforming cycle, the device requires lower voltages to sweep (−0.5 to 0.5 V) for the repeated switching form HRS to LRS, and vice versa. While sweeping voltage from 0 to 0.5, the current increased drastically around ≈0.45 V, thus considered as the set voltage. Similarly, in the negative bias regime, the device current started a significant reduction around −0.3 V, hence showing the resetting capability of the memory state. The reliability and robustness of the device was tested for more than 100 switching cycles, Figure S5, Supporting Information, in which a low standard deviation for the SET voltage (0.4 ± 0.03 V) is obtained, Figure S5b, Supporting Information. The I_{ON}/I_{OFF} ratio for this device type was found to be 10². The volatility of the memory has been studied from the retention time of the devices. The SET and RESET states were read with a sequential voltage pulse of 0.1 V, with one second interval. The memory written in the Au top contact device was found to be volatile, with short retention times of ≈500 s, Figure 2f. The addition of the Ag thin layer in between the Au and the VA-MoS₂ exhibit a memory retention of more than 20 ks, Figure 2g. The low ON state voltage (<0.5 V) and high retention time in the Ag/VA-MoS₂/Si devices, demonstrate its robustness toward memristive applications.

High-angle annular dark-field (HAADF) STEM and elemental mapping were used to study and compare between the pristine and the turned “ON” devices. To this end, cross-sectional samples were prepared via FIB methodologies (see experimental section) on both types of samples. STEM and EDS characterization of the pristine and ON-device are shown in Figure 3a,b, respectively. No significant difference is observed in the HAADF STEM images, the top left in (a) and (b), for the pristine, and set ON device, respectively. On the other hand, EDS of both samples show the presence of Ag in within the VA-MoS₂ film, only for the set-ON device (bottom right in (b)). This indicates that Ag ions/atoms diffused or intercalated between layers, though it may not necessarily be a continuous filament, forming the conducting path, as measured at the LRS.

These observations are well correlated with the I−V profiles in the switching cycles. The I−V sweep of Ag/VA-MoS₂/Si devices exhibit bipolar characteristics with a close to linear characteristic at low voltages, Figure 2c and Figure S6, Supporting Information. Figure 4a shows the I versus V profile for HRS and LRS states in a positive cycle. The HRS follows a space charge limited current (SCLC) model with an Ohmic region (slope ≈ 1) at low voltages. Further voltage increase leads to a field driven I = V² (slope = 2: Child’s law) region for transition from HRS to LRS. Here, the positive bias drives the electron/Ag ion between the electrodes through the MoS₂ film, forming a conducting filament that drives the HRS to LRS transition. The Ohmic behavior (slope = 1.2) in LRS further approves such filament formation through the silver diffusion, creating conduction path for the low resistive “on” state. A schematic representation of the proposed Ag-enriched VA-MoS₂ film—assisted conduction path formation mechanism is shown in Figure 4b. In this scheme, the diffusion of the Ag ions/atoms (with ionic/atomic radii of ≈0.129–0.160 nm) through the channels created by the vertically aligned MoS₂ layers, with a vdW gap of ≈0.314 nm. First principle calculations also demonstrate that the electrochemical intercalation of Ag in vdW gap of the 2H-MoS₂ is energetically favorable with low activation energies. The application of a positive bias to the Ag electrode leads to its oxidation into Ag⁺ ions, facilitating their diffusion toward the bottom contact, the Si++ substrate, for the reduction to take place. This phenomenon is the reason for the conducting Ag-based filament-like in between the VA-MoS₂ layers, turning the device into the LRS. When the device polarity is reversed, the continuity of the Ag filament is disrupted due to reverse migration of the intercalated Ag atoms. Hence, the conduction properties seen in the sweeping cycles arise from the complex hybrid structure of Ag intercalated MoS₂.

The stability and robustness of the VA-MoS₂ memristor was tested as a function of temperature. In this scheme, the device is first turned ON to its LRS at room temperature (RT-SET), and then heated to 350 °C with a heating rate of 5 °C min⁻¹. The device retained the LRS state, while current increases with temperature. The I−T curve of this RT-SET state was well fitted with a linear equation with a positive slope. Figure 5a. In a complimentary experiment the device was switched ON at 350 °C (HT-SET) and then cooled down to RT, exhibiting a negative linear slope in the I−T curve, Figure S7a, Supporting Information, that is, the current decreases while cooling. The direct relationship of the current with respect to temperature indicates a non-metallic behavior in the LRS of the memristor. This means that the diffusion/intercalation of Ag ions/atoms throughout the VA-MoS₂ film increases with the temperature, and accordingly, the current. Therefore, the LRS is achieved when the amount of Ag ions/atoms is enough to allow for the charges to hop efficiently through the silver-enriched VA-MoS₂. Figure 5b shows the Arrhenius plot, ln(I)−1/T, for the heating, Figure 5a, and cooling, Figure S7a, Supporting Information, measurements. Interestingly, the activation energies, E_a, extracted from such plots in the heating set of measurements, (0.6 eV), was found to be larger than for the cooling process (0.35 eV). Such activation energies, imply the presence of shallow traps, suggesting the LRS is reached by trap-assisted charge transport, rather than the formation of a continuous metallic filament. The difference in the E_a can be understood according to the working mechanism principle mentioned above, in which the temperature enhances the diffusion of silver ions/atoms into the MoS₂ film, thus creating conductive centers that facilitate charge hopping, and hence the lower E_a for the cooling set of measurements.

The memristor shows bipolar switching characteristics in all tested temperatures. It is found that the set voltages significantly decrease with the temperature raise. For 100, 200, 300, and 350 °C the set voltages are 0.5, 0.35, 0.27, and 0.2 V, respectively, Figure 5c. It reveals that along with applied potential between electrodes the temperature also assists to switch on the device. The comparison between pre- and post-heating testing cycles, Figure 5d show the permanent changes in the resistance of a device in both LRS and HRS states. It is also noted that cooling–heating cycle (Figure S7b, Supporting Information) does not yield changes in the initial resistance of the tested
state of the memristor. Hence, low voltages (∼10 mV) used for “reading” the state does not have an impact on the current. On the other hand, writing a memory (larger SET-V, ≈0.4 V) at particular temperature yield a permanent change in the resistance. In a memory cell the disruption occurs locally at the weakest part of the filament.\[27\] According to the temperature-dependent memristive results, the increased intercalation of Ag in between vdW gaps may not be entirely reversible.\[28\] Therefore, once the device set at a high temperature, the resistance of the Ag-MoS$_2$ ($R_1$, see Supporting Information for details) reduced permanently. Retention time is almost not affected by the operation temperature, as shown in Figure 5e, and the switching endurance of the device tested for more than 100 cycles (at room temperature, RT, and 350 °C), is presented in Figure 5f and Figure S8, Supporting Information. Here, the endurance of the device was extracted from the current measured at 0.2 V in HRS, and LRS of the continuous sweeping cycle.

The VA-MoS$_2$-based memristive devices were tested for emulating synaptic behavior to be applied in neuromorphic computing. The $I$–$V$ behavior of ten continuous positive voltage sweeping cycles were tested, Figure 6a, in the HRS regime (low voltages, <SET V). A hysteresis loop for each cycle is clearly seen, Figure 6a. Moreover, the consecutive sweeping cycles increases the conductance of the device. This behavior indicates the possibility of monotonous and sequential modulation of the intrinsic conductance of the memristive devices to simulate synaptic behavior.\[3b,4,29\] We further investigate their weighted synaptic behavior by applying voltage pulses. Here, the stress,
and depress of the neural synapsis were analyzed by continuous positive and negative pulses, respectively. The voltage pulse train consists of 200 positive (100 mV) and 200 negative (−100 mV) pulses, Figure 6b. The consecutive positive pulses stress the device for long term potentiation which are observed through the increases in current, Figure 6c. Similarly, long-term depression are seen from exponentially reduced current through successive negative pulses. It is important to note that this modulation was observed for currents lower than 120 nA and a low power consumption of 7 nW ($P = V_{\text{read}} \times I$). This current is significantly lower than the ones reported in multilayer and polycrystalline VdW materials.[11c,e,30] Further the presence of the voltage amplitude dependent potentiation also demonstrated by comparing 100, 150, and 200 mV voltage training

Figure 4. a) In(I) versus In (V) show the SCLC characteristics in HRS with Ohmic and $I \alpha V^2$ (Child’s law) regions. The LRS shown the slope of 1.2 while fitted with linear equation. b) Schematic representation of the different states along the I-V cycle, while applying positive bias the HRS was transitioned to LRS with the diffusion of Ag ions. The continuity of the Ag ion disrupted and the device switched back to HRS during resetting process. Note, in the reset state, part of the intercalated Ag ions/atoms stays throughout the VA-MoS$_2$ film.

Figure 5. Thermal stability of the memristive devices at elevated temperature: a) The device was set-ON at RT (RT-SET). The stored memory (set state) was tested up to 350 °C. The current increases with the temperature and fitted with linear equation. b) Arrhenius plot, ln(I)/1/T, from the measurements in (a) and Figure S7a, Supporting Information, showing the extracted $E_g$ (heating) = 0.6 eV, for the heating and cooling measurements, respectively. c) Switching characteristics at different temperatures. d) RT and High temperature cycle operation showing the permanent reduction in the resistance of the device. e) Retention time as a function of operation temperature. f) Switching endurance at room temperature and at 350 °C.
pulses (Figure S9, Supporting Information). These are required for multi-level memory devices which are used in simulating a weighted synaptic behavior. The non-linear relation between the current and the pulse number is believed to arise from non-uniform conductance changes in response to identical pulses. Such changes could be related to the different conductive path or filament formation stages and has been observed in metal-oxide based memristors.\[31\] This phenomenon is unwanted because in order to keep a linear current modulation with the pulse number, as desired in neuromorphic computing,\[31\] the pulse amplitude/width must be changed accordingly, increasing the complexity of the whole circuit. The reason for the non-linearity behavior in the above devices is not clear at this point and further work needs to be done on this topic. With a proper material (VA-TMDC) engineering, for example by creating vertical heterostructures or a gradient of alloying/doping elements (like a functional gradient material, FGM), the kinetics of the conducting path could be tuned, and thus, the LTP and LTD behavior.

Along with the electronic properties, MoS$_2$ is also well known to be photosensitive,\[8a\] which has potential for integration with memristive applications,\[16a\] therefore, presenting an advantage over the more traditional metal-oxide based memristors.\[31\] This phenomenon is unwanted because in order to keep a linear current modulation with the pulse number, as desired in neuromorphic computing,\[31\] the pulse amplitude/width must be changed accordingly, increasing the complexity of the whole circuit. The reason for the non-linearity behavior in the above devices is not clear at this point and further work needs to be done on this topic. With a proper material (VA-TMDC) engineering, for example by creating vertical heterostructures or a gradient of alloying/doping elements (like a functional gradient material, FGM), the kinetics of the conducting path could be tuned, and thus, the LTP and LTD behavior.

Figure 6. Weighted synaptic behavior: a) Continuous positive $I-V$ ($V < V_{set}$) sweep showing the monotonous conductance increment for each sweeping cycle. b) Applied positive (100 mV) and negative (-100 mV) continuous pulses with respect to output current results in exponential current increase and decrease, manifesting long-term potentiation (LTP), and long-term depression (LTD) process, respectively.

In summary, a facile and robust approach is presented for the synthesis and assembly of Ag/VA-MoS$_2$/Si two-terminal memristor devices. The VA-MoS$_2$ film is grown by the sulfurization of pre-deposited Mo thin films and therefore, suitable for large-scale applications on various target substrates. The memristive device shows large retention times with low-SET voltages. Such devices exhibit reproducible and non-volatile behavior at high operating temperatures, up to 350 °C, which, to our knowledge, is the highest reported so far (for 2D materials-based memristors). Weighted synaptic behavior with LTP and LTD were demonstrated as well. Finally, the Ag/VA-MoS$_2$/Si devices exhibit photoresponse, and hence, light-sensitive used for illumination. The $I-t$ curve shows that in both states, HRS and LRS, the current output increases upon illumination, Figure 7c. The responsibility was calculated using the formula, 

$$\text{Responsivity} = \frac{I_L - I_D}{P_{\text{laser}}}.$$  

Here, $I_L$ and $I_D$ are the current measured under light and dark condition and $P_{\text{laser}}$ the incident laser power. The responsivity was found to be higher for the LRS comparing to HRS (Figure S10, Supporting Information). In LRS the photoactivated charges might reach the bottom electrode due to the enhanced charge transport in the “ON” state of the device. In both states, the photoresponse of the device was linear within the studied regime, Figure S10, Supporting Information. Figure 7d shows an example in which six discrete states of the device were programmed, using three different laser power intensities, Figure 7d. The photo-responsivity calculated for the LRS is found to be higher (>30 times) than for the HRS (Figure S10, Supporting Information). The conduction path is formed by the diffusion of Ag ions/atoms into the VA-MoS$_2$, and thus, the LRS is achieved when higher amounts of silver are embedded in the film. The enhanced photoresponse in the LRS may indicate that the Ag contribute by enhancing the absorption\[33\] and/or facilitating the charge separation of the excited electron–hole pair upon illumination.\[34\] The light induced photo-memristive behavior has high potential to be implemented in high speed resistive switching devices,\[19\] as required for various applications.

3. Conclusions

In summary, a facile and robust approach is presented for the synthesis and assembly of Ag/VA-MoS$_2$/Si two-terminal memristor devices. The VA-MoS$_2$ film is grown by the sulfurization of pre-deposited Mo thin films and therefore, suitable for large-scale applications on various target substrates. The memristive device shows large retention times with low-SET voltages. Such devices exhibit reproducible and non-volatile behavior at high operating temperatures, up to 350 °C, which, to our knowledge, is the highest reported so far (for 2D materials-based memristors). Weighted synaptic behavior with LTP and LTD were demonstrated as well. Finally, the Ag/VA-MoS$_2$/Si devices exhibit photoresponse, and hence, light-sensitive
memristive behavior is shown and, by changing the laser power used for the light stimulation, different memory states programmed. The facile and high scalability of the synthetic process used to make the VA-MoS₂, together with the high performance at RT and high temperatures, the synaptic behavior, and photo-sensitivity, may allow for the integration of large-scale multi-functional memristive devices. The same methodology shown here is suitable to be applied to other TMDCs and their heterostructures. Moreover, doping and alloying strategies can be easily implemented in this approach,[9a,14] therefore, opening a large window for property tunability.

4. Experimental Section

Synthesis of VA-MoS₂: A heavily doped Si wafer (p++) was treated with HF (30%) for 5s to etch native SiO₂ on Si. Immediately after etching the Si was loaded into e-beam evaporator (VINCI) for a coating of 15 nm Mo thin film. The Mo/Si were used for growing MoS₂ through sulfurization process in atmospheric chemical vapor deposition (CVD) system (Figure S7, Supporting Information). The three step CVD process starts with annealing under 100 sccm of Ar and 5sccm H₂ at 200 °C for 1hr. In next step, the gas flow was changed in to 60sccm Ar, and 5sccm H₂. The furnace was ramped to 800 °C with the rate of 6 °C min⁻¹ and the sulfur powder was heated to 180 °C by external heater. During this 2 h of VA-MoS₂ growth time, the sulfur vapor (above its melting point, which is 120 °C) was carried downstream into the reaction zone by the carrier gas. At the end of this process the furnace cools down naturally to room temperature and the sulfur heater is turned off when the furnace cools to the temperature of 600 °C.

Structural and Chemical Characterization: The TEM lamellas were prepared by the lift-out method in a dual-beam FIB (FEI Helios NanoLab Dual Beam G3 UC). Samples were thinned to 50 nm using a Ga⁺ ion beam at 30 kV with beam currents ranging from 0.43 nA down to 24 pA. Amorphization layer removal was carried at 5 and 9 pA, respectively. The HRTEM with a probe corrected FEI/ThermoFisher Titan Cubed Themis G2 60–300 operated at 200keV acceleration voltage were used to acquire the microgram. The EDS maps were acquired using a Bruker Dual-X detector (Bruker Corp., Billerica, USA) and processed using the Thermo Fisher Velox software. The Raman spectra were collected with a green laser (532 nm) by HORIBA LabRAM HR Evolution Raman spectrometer. A 100× Olympus objective focuses the laser beam to a spot of <1 µm diameter with 1800 gr mm⁻¹ grating. XPS measurements were performed in UHV (2.5 × 10⁻¹⁰ Torr base pressure) using a 5600 Multi-Technique System (PHI, USA). The sample was irradiated with an Al Kα monochromated source (1486.6 eV) and the outcome electrons were analyzed by a Spherical Capacitor Analyzer using the slit aperture of 0.8 mm. Depth Profiling was done by means of Ar⁺ Ion Gun sputtering (sputter rate was ≈17 Å min⁻¹ on/Si reference).

Device Fabrication and Testing: To fabricate metal-insulator-metal structure for a memristor the existing Si substrate was served as a bottom contact. The metal stacks Ag/Au and Ag/ITO for top contact was coated by using e-beam evaporator and RF magnetron sputtering (PENTA sputter), respectively. While coating, a shadow mask was used to define the device area. The current–voltage (I–V) characteristics of fabricated Si/MoS₂/Au structures were investigated in the dark and under laser excitation (532 nm) using a Keysight B1500A semiconductor device parameter analyzer. A Linkam probe stage (HFS350EV-PB4) was used to control temperature during I–V measurements.
Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors gratefully acknowledge the very generous support from the Israel Science Foundation, projects # 2171/17 (K.R.), 2549/17 (M.F.) and 1784/15 (A.I.).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

electrochemical metallization, memory states, memristors, photomemristors, potentiation, vertically aligned MoS₂

Published online: September 18, 2020
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