RELOAD+REFRESH: Abusing Cache Replacement Policies to Perform Stealthy Cache Attacks

Samira Briongos\textsuperscript{1}, Pedro Malagón\textsuperscript{1}, José M. Moya\textsuperscript{1} and Thomas Eisenbarth\textsuperscript{2,3}

\textsuperscript{1}Integrated Systems Laboratory, Universidad Politécnica de Madrid, Madrid, Spain  
\textsuperscript{2}University of Lübeck, Lübeck, Germany  
\textsuperscript{3}Worcester Polytechnic Institute, Worcester, MA, USA

\textbf{Abstract}

Caches have become the prime method for unintended information extraction across logical isolation boundaries. Even Spectre and Meltdown rely on the cache side channel, as it provides great resolution and is widely available on all major CPU platforms. As a consequence, several methods to stop cache attacks by detecting them have been proposed. Detection is strongly aided by the fact that observing cache activity of co-resident processes is not possible without altering the cache state and thereby forcing evictions on the observed processes. In this work we show that this widely held assumption is incorrect. Through clever usage of the cache replacement policy it is possible to track a victims process cache accesses \textit{without forcing evictions} on the victim’s data. Hence, online detection mechanisms that rely on these evictions can be circumvented as they do not detect be the introduced RELOAD+REFRESH attack. The attack requires a profound understanding of the cache replacement policy. We present a methodology to recover the replacement policy and apply it to the last five generations of Intel processors. We further show empirically that the performance of RELOAD+REFRESH on cryptographic implementations is comparable to that of other widely used cache attacks, while its detectability becomes extremely difficult, due to the negligible effect on the victims cache access pattern.

\section{Introduction}

The microarchitecture of modern CPUs shares resources among concurrent processes. This sharing may result in unintended information flows between concurrent processes. Microarchitectural attacks, which exploit these information flows, have received a lot of attention in academia, industry and, with Spectre and Meltdown [32, 37], even in the public news. The OS or the hypervisor in virtual environments provide strict logical isolation among processes to enable secure multithreading. Yet, a malicious process can intentionally create contention to gain information about co-resident processes. Exploitable hardware resources include the branch prediction unit [2–4], the DRAM [31, 47, 51] and the cache [6, 13, 20, 44, 45, 57]. Last level caches (LLC) provide very high temporal and spatial resolution to observe and track memory access patterns. As a consequence, any code that generates cache utilization patterns dependent on secret data is vulnerable. Cache attacks can trespass VM boundaries to infer secret keys from neighboring processes or VMs [21, 49], break security protocols [26, 50] or compromise the end users privacy [44], but they can leak information from within a victims memory address space [32] when combined with other techniques.

Different techniques have been proposed for detection and/or mitigation of cache and other microarchitectural attacks due to the great threat they pose. On the one hand, hardware countermeasures take years to integrate and deploy, may induce performance penalties and currently, are not implemented. On the other hand, other proposals that are meant for cloud hypervisors [30, 35, 53] and only require making small modifications to the kernel configuration are neither implemented presumably due to the overhead they entail.

The only solution that seems practical for users that want to protect themselves against these kind of attacks, is to detect ongoing attacks and then react in some way. To this end, different proposals [9, 11, 34, 46, 60] use hardware performance counters (HPCs), which are special registers available in all modern CPUs, that monitor hardware events such as cache misses. The most recent proposals are able to detect even attacks specially designed to bypass previous countermeasures [18]. The common assumption in these works is that the attacker induces measurable effects on the victim. We, on the contrary, demonstrate that it is possible to obtain information from the victim while keeping its data in the cache and, consequently, not significantly altering its behavior, thus making attack detection difficult.

\textbf{Our Contribution: } We analyze the replacement policy of current Intel CPUs and identify a new strategy which allows an attacker to monitor cache set accesses without forcing evictions of the victim’s data, thereby creating a new and
stealthy cache-based microarchitectural attack. To achieve this goal, we perform the first full reverse engineering of different replacement policies present in various generations of Intel Core processors. We propose a technique that can be extended to study replacement policies of other processors. Using this technique, we demonstrate that it is possible to accurately predict which element of the set will be replaced in case of a cache miss. Then, we show that it is possible to exploit these deterministic cache replacement policies to derive a sophisticated cache attack: RELOAD+REFRESH, which is able to monitor the memory accesses of the desired victim without generating cache misses. As a proof of concept, we demonstrate the feasibility and quantify the performance of RELOAD+REFRESH by retrieving the key of a T-Table implementation of AES and attacking the square and multiply version of RSA. We prove that our approach is at least as accurate as other state-of-the-art cache attacks. Even when adding extra steps to recover the information, the attack has still enough resolution (similar to PRIME+PROBE) to trace the victim memory accesses with high accuracy. Thus, our work reveals the need for new detection mechanisms or countermeasures. To sum up, this work:

- introduces a methodology to test different replacement policies in modern caches.
- uncovers the replacement policy currently implemented in modern Intel Core processor generations, from fourth to eighth generation.
- expands the understanding of modern caches and lays the basis for improving traditional cache attacks.
- presents RELOAD+REFRESH, a new attack that exploits Intel cache replacement policies to extract information referring to a victim memory accesses.
- shows that the proposed attack causes negligible cache misses on the victim, which renders it undetectable by state of the art countermeasures.

2 Background and related work

2.1 Cache architecture

CPU caches are small banks of fast memory located between the CPU cores and the RAM. As they are placed on the CPU die and close to the cores, they have low access latencies and thus reduce memory access times observed by the processor, improving the overall performance. Modern processors include cache memories that are hierarchically organized; low level caches (L1 and L2) are core private, smaller and closer to the processor, whereas the last level cache (LLC or L3) is bigger and shared among all the cores.

Intel processors traditionally have included L3 inclusive caches: all the data which is present in the private lower caches has to be in the shared L3 cache. This approach makes cache coherence much easier to implement. However, due to cache attacks, the newest Intel Skylake Server microarchitecture considers using a non-inclusive Last Level Cache [22].

In most modern processors caches are W-way set-associative. The cache is organized into multiple sets (S), each of them containing W lines of usually 64 bytes of data. The set in which each line is placed is derived from its address. The address bits are divided into offset (lowest-order bits used to locate data within a line), index \((\log_2(S))\) consecutive bits starting from the offset bits that address the set) and tag (remaining bits which identify if the data is cached).

2.2 Cache replacement policies

When the processor requests some data, it first tries to retrieve this data from the cache (it starts looking in the lowest levels up to the last level). In the event of a cache hit the data is loaded from the cache. On the contrary, in the event of a cache miss, the data is retrieved from the main memory and it is also placed in the cache assuming that it will be reused in the near future. If there is no free room in the cache set, the memory controller has to decide which element in the cache has to be evicted. Since the processor is stalled for several cycles whenever there is a cache miss, the decision of which data is evicted and which data stays is crucial for the performance.

Many replacement policies are possible including, for example, FIFO (first in first out), LRU (least recently used) or its approximations such as NRU [52] (not recently used), LFU (least frequently used), CLOCK [27](keeps a circular list of the elements) or even pseudo-random replacement policies. Modern high performance processors implement approximations to LRU, because LRU is hard to implement (it requires complex hardware to track each access). LRU or pseudo LRU policies have demonstrated to perform well in most situations. Nevertheless, LRU policy behaves poorly for memory-intensive workloads whose working set is bigger than the available cache size or for scans (bursts of one-time access requests). As a result, adaptive algorithms, which are capable to adapt themselves to changes in the workloads, came up. In 2003, Megiddo el al. [42] proposed ARC (Adaptive Replacement Cache) a hybrid of LRU and LFU. One year later, Bansal et al. [8] presented their solution based on LFU and CLOCK, which they named CAR (Clock with Adaptive Replacement).

In 2007 Qureshi et al. [48] suggested that performance could be improved by changing the insertion policy while maintaining the eviction policy. LIP (LRU Insertion Policy) consists in inserting each new piece of data in the LRU position whereas BIP (Bimodal Insertion Policy) most of the times places the new data in the MRU position and sometimes inserts it in the LRU position. In order to decide which of the two policies behaves better, they proposed a dynamic
insertion policy (DIP). DIP chooses between LIP and BIP depending on which one incurs fewer misses.

In 2010, Jaleel et al. [29] proposed a cache replacement algorithm that makes use of Re-reference Interval Prediction (RRIP). By using 2 bits per cache line, RRIP predicts if a cache line is going to be re-referenced in the near future. In case of eviction, the line with the longest interval prediction will be selected. Analogously to Qureshi et al, they presented two different approaches: Static RRIP (SRRIP) which inserts each new block with an intermediate re-reference, and Bimodal RRIP (BRRIP) which inserts most blocks with a distant re-reference interval and sometimes with an intermediate re-reference interval. They also proposed using set auditing to decide which policy fits better for the running application (Dynamic RRIP or DRRIP).

Regarding to Intel processors, their replacement policy is undocumented and consequently unknown. All that is officially known is the name of the policy: "Quad-Age LRU" [28]. The first serious attempt to reveal the cache replacement policy of different processors was made by Abel et al. [1]. In their work, they were able to uncover the replacement policy of an Intel Atom D525 processor and to infer a pseudo-LRU policy in an Intel Core 2 Duo E6300 processor. However, they could not determine the eviction policy in the other machines (Intel Core 2 Duo E6750 and E8400) they used for the experiments. Later on, Henry [56] showed that Intel processors seem to implement a dynamic insertion or eviction policy, but he did not provide further details about the replacement policy.

Gruss et al. [17] studied cache eviction strategies on recent Intel CPUs in order to replace the clflush instruction and build a remote Rowhammer attack. As they mention, their work is not strictly a reverse engineering of the replacement policy, rather they test access patterns to find the best eviction strategy. To the best of our knowledge, our work is the first one that provides a comprehensive description of the replacement policies implemented on modern Intel processors.

### 2.3 Cache attacks

Cache attacks monitor the utilization of the cache (the sequence of cache hits and misses) to retrieve information about a co-resident victim. Whenever the pattern of memory accesses of a security-critical piece of software depends on the actual value of sensible data, such as a secret key, this sensitive data can be deduced by an attacker and will no longer be private. Traditionally cache attacks have been grouped into three categories [14]: FLUSH+RELOAD, PRIME+PROBE and EVICT+TIME. From those, the FLUSH+RELOAD and the PRIME+PROBE attacks (and their variants) out-stand over the rest due to their higher resolution.

Both attacks target the LLC, selecting one memory location that is expected to be accessed by the victim process. They consist of three stages: initialization (the attacker prepares the cache somehow), waiting (the attacker waits while the victim executes) and recovering (the attacker checks the state of the cache to retrieve information about the victim).

#### 2.3.1 FLUSH+RELOAD

This attack relies on the existence of shared memory. Thus, it requires memory deduplication to be enabled. Deduplication is an optimization technique designed to improve memory utilization by merging duplicate memory pages. Using the clflush instruction the attacker removes the target lines from the cache, then waits for the victim process to execute (or an equivalent estimated time) and finally measures the time it takes to reload the previously flushed data. Low reload times mean the victim has used the data.

It was first introduced in [20], and was later extended to target the LLC to retrieve cryptographic keys, TLS protocol session messages or keyboard keystrokes across VMs [19, 26, 57]. Further, Zhang et al. [61] showed that it was applicable in several commercial PaaS clouds.

Relying on the clflush instruction and with the same requirements as FLUSH+RELOAD, Gruss et al. [18] proposed the FLUSH+FLUSH attack. It was intended to be stealthy and bypass existing monitoring systems. This variant recovers the information by measuring the execution time of the clflush instruction instead of the reload time, thus avoiding direct cache accesses and, as a consequence, detection. However, recent works have demonstrated that it is detectable [9, 34].

#### 2.3.2 PRIME+PROBE

Contrary to the FLUSH+RELOAD attack, PRIME+PROBE is agnostic to special OS features in the system. Therefore, it can be applied in virtually every system. Moreover, it can recover information from dynamically allocated data. To do so, the attacker first fills or primes the cache set in which the victim data will be placed (initialization stage). Then, he waits and finally probes the desired set looking for time variations that carry information about the victim activity.

This attack was first proposed for the L1 data cache in [45] and later was expanded to the L1 instruction cache [5]. These approaches required both victim and attacker to share the same core, which diminishes practicality. However, it has been recently shown to be applicable to LLC. Researchers have bypassed several difficulties to target the LLC, as retrieving its complex address mapping [23, 41, 58], and recovered cryptographic keys or keyboard typed keystrokes [13, 24, 36]. Even further, the PRIME+PROBE attack was used to retrieve a RSA key in the Amazon EC2 cloud [21].

In case a defense system tries to either restrict access to the timers [33, 40] or to generate noise that could hide tim-
ing information, cache attacks are less likely to succeed. The PRIME+ABORT attack [12] overcomes this difficulty. It exploits Intel’s implementation of Hardware Transactional Memory (TSX) to retrieve the information about cache accesses. It first starts a transaction to prime the targeted set, waits and finally it may or may not receive and abort depending on whether the victim has or has not accessed this set.

2.4 Countermeasures

Researchers have tackled the problem of mitigating cache attacks from different perspectives. Several proposals suggest limiting the access to the shared resources that can be exploited to infer information about a victim by modifying the underlying hardware [39,54]. While effective, these hardware countermeasures take years to deploy and it is not likely that any CPU manufacturer will deploy them.

System-level software approaches, on the other hand, require modification of the current cloud infrastructure or the Linux kernel. STEALTHMEM [30] uses private virtual pages that ensure the data located in them is not evicted from the cache and avoid mapping any other page with these private virtual pages. CATalyst [38] uses Intel Cache Allocation Technology (CAT), which is a technology that enables system administrators to control how cores allocate data into the LLC, to mitigate cache attacks. CACHEBAR [62] designs a memory management subsystem that dynamically changes the amount or lines per cache set that a security domain can access that data and force a miss when desired to observe details about the data.

These countermeasures are more plausible than the previous ones, however no cloud provider or OS is implementing them, probably because of the performance penalties they incur.

For these reasons, we believe that the only countermeasures that an attacker may have to face when trying to retrieve information from a victim, are detection based countermeasures which can be implemented at user level. Cache attacks exploit the side effects of running a program in certain hardware to gain information from it, and similarly, these countermeasures employ monitoring mechanisms to detect such attacks. Detection systems can use time measurements [10], hardware performance counters [9,11,34,60] or place data in transactional regions [16] defined with the Intel TSX instructions. All of them measure the effect of the last level cache misses on the victim or on both the victim and the attacker. As a consequence, an attack that does not generate cache misses on the victim side would be undetectable by these systems.

A different approach to protect sensitive applications is to specifically design them to be secure against side-channels (no memory accesses depend on private information). Then, developers can use specific tools to ensure the binary of such applications does not leak information, even if it is under attack [55,59]. There are other tools, such as MASCAT [25], which use code analysis techniques to detect potential attacks before running a program, as most anti-viruses do. This kind of tools is effective before malware distribution or execution. Their effectiveness is reduced in cloud environments where the attacker does not need to infect the victim.

3 Retrieval of Intel cache eviction policies

This work focuses on the LLC. Since it is shared across cores, the attacks targeting the LLC are not limited to the situation in which the victim and the attacker share the same core. It is also possible to extract fine-grained information from it and many researchers are concerned about the attacks targeting the LLC. Attacks that assume a pseudo LRU eviction policy such as PRIME+PROBE or EVICT+RELOAD can benefit from the detailed knowledge of the eviction policy, as can benefit one attacker wishing to carry out a stealthy attack that does not cause cache misses on the victim.

In order to be able to study the eviction policy, we have to ensure we can fill one set of the cache with our own data, access that data and force a miss when desired to observe which element of the set is evicted. For this reason, we have constructed an eviction set (a group of $w$ different addresses that map to one specific set in $w$-way set-associative caches) and what we call a conflicting set (a second eviction set that maps to exactly the same set and is composed of disjoint addresses). Previous works have shown how to statically recover the complex addressing function [23,41,58]. However, we have decided to create both the eviction and conflicting sets dynamically [13]. This approach is faster and general for all the processors involved in this work.

Algorithm 1 Obtaining the conflicting set

| Input: Eviction_set, Conflicting set candidates |
| Output: Conflicting_set |

function $\text{GET\_CONFLICTING\_SET}(\text{eviction\_set, candidates})$

$\text{conflicting\_set} \leftarrow \{\}$;

for all $e \in \text{candidates}$ do

read_all($\text{eviction\_set}$);

flush_all($\text{eviction\_set}$);

read($e$);

read_all($\text{eviction\_set}$);

measure $\text{time}$ to read $e$;

if $\text{time} > \text{threshold}$ then

$\text{conflicting\_set} \leftarrow e$;

if $\text{sizeof}(\text{conflicting\_set}) == w$ then

break;

return $\text{conflicting\_set}$

The eviction set was constructed following the procedure proposed by Liu et al. in [13] (Algorithm 1). The procedure for obtaining the conflicting set follows the same principles.
and uses the eviction set that has just been constructed. This procedure is summarized in algorithm 1. First, we remove all the data from one set by accessing the eviction set and then, once the data is in the cache set, flushing the whole eviction set. When the set is completely empty, we select one address among all the possible candidates (memory lines whose set index bits are equal to the eviction set index bits) for the conflicting set. Finally, we access the candidate address, the whole eviction set, and re-access the candidate again. If the reload time is higher than a threshold, we can conclude that the candidate address maps to the same set as the eviction set. Thus, it can be included in our conflicting set. We repeat the same procedure until the conflicting set has w lines.

For all the experiments, we have enabled the use of hugepages in our systems. Note that the order of the accesses is important to deduce the eviction policy. We enforce this order using mfence instructions, which act as barriers that ensure all preceding load and store instructions have finished before any load or store instruction that follows mfence.

3.1 Design of the experiments

We have performed experiments in five different machines, each of them including an Intel processor from a different generation. Table 1 presents a summary of the machines employed in this work. It includes the processor name, its number of cores, the associativity of the cache and the OS running on each machine. We have started by studying the processor of the fourth generation, which has been a common victim of published PRIME+PROBE attacks. We have finally covered from fourth to eighth generations.

Before conducting the experiments to disclose the eviction policy implemented in each of the used machines, we have performed some experiments intended to verify that no cached data is evicted in the event of a cache miss if there is free room in the set. The procedure is quite straightforward: for each of the sets, we first completely fill it with the data on its corresponding eviction set. Next, we randomly flush one of these lines to ensure there is free room in the set, and we access one of the lines in the conflicting set to ensure there is going to be a cache miss. Finally, we check, by measuring times when re-accessing them, that all the lines in the eviction set (except for the one evicted) still reside in the cache. As expected, in all cases the incoming data was loaded in replacement of the flushed line.

Note that in a machine fully controlled by us, we can compare the actual evolution of the data in each of the sets with its theoretical evolution defined by an eviction policy during the runtime. This is the main idea of the procedure we propose to retrieve the replacement policy. Algorithm 2 summarizes this procedure. Each of the policies that has been tested had to be manually defined. We have evaluated true LRU, Tree PLRU, CLOCK, NRU, Static and Bimodal RRIP, self-defined policies using four control bits, etc. among many other possible cache eviction policies. After multiple experiments, we can conclude that the implemented policy is the defined policy which best matches the experimental observations.

Algorithm 2 tries to emulate by software the behavior of the hardware (of the cache). For this purpose, it uses two arrays of size w. On the one hand, address_array mimics the studied set, storing the memory addresses whose data is in the cache set. On the other hand, control_array contains the control bits used for deciding which address will be evicted in case of conflict. Additionally, we need to manually define one function that updates the content of the address_array, one function that updates the control_array and another one that provides the eviction candidate i.e. it returns the address of the element that will be evicted in case of conflict. These functions are defined based on the replacement policy.

As an example, we assume we want to test the NRU policy [52], which turns out to match the policy implemented in an Intel Xeon E5620 according to our experiments. According to its specification, NRU uses one bit per cache line, this bit is set whenever a cache line is accessed. If setting one bit implies that all the bits of a cache set will be equal to one, then all the bits (except for the one that has just being accessed) will be cleared. In case of conflict, NRU will remove from the cache one element whose control bit is equal to zero. Thus in our procedure, the control bits would be -1 (line empty), 0 (line not recently used), and 1 (line recently used). When a memory line is accessed, the update function first checks if its address is already included in the address_array. If it is not, our function will add it to the address_array and set the corresponding bit in the control_array. On the contrary, the function only updates the control_array. The getEvictionCandidate function will return one array position whose control bit value is -1, or, if no control bit is equal to -1, one whose control bit is equal to 0. In case multiple addresses have control bits equal to -1 or to 0, the function will return the first address whose control bits are -1 or 0, that it encounters when traversing the control_array from the beginning. Finally, after forcing a cache miss, the testDataEvicted() returns the element truly evicted that we then compare with the predicted by the NRU policy (the output of getEvictionCandidate).

We have noticed that only accesses to the LLC update the values of the control bits of the accessed element. That is, if the data is located in L1 or L2 caches when requested (reload time lower than ll_threshold), we do not update the values in the control_array. Figure 1 shows the distinction between accesses to low and last level caches based on reload times.

3.2 Results

The outcomes of our experiments highlight some differences in the cache architecture of the machines, as also noticed in [12]. Traditionally, the cache is divided into slices, each of them containing N sets. The number of slices used to be
equal to the number of physical cores a machine has. This is true for the 4th and 5th generation processors. Per contra, the newest ones have as many slices as virtual cores; that is, two times the number of physical cores. Cache sizes are similar, so they also differ in the number of sets per slice.

Since several policies suggest that different sets can perform differently, we have repeated the experiment in Algorithm 2 for each of the sets in the last level cache. As a result, we have found out that only the i7-4790 and the i3-5010U machines (4th and 5th generation) implement set dueling to dynamically select the eviction policy with better performance between two candidate policies. We conducted several further experiments intended for determining which sets implement a fixed policy and which others change their policy based on the number of hits and misses. Locating the sets with a fixed policy is interesting for several reasons: these sets will allow to accurately determine the two different replacement policies and they will allow to favor one policy over the other depending on our interests. This also means that we could monitor one set belonging to the group of followers to determine which policy is currently operating.

The strategies for locating the sets included different access patterns that we believed would lead to different number of misses. For example, if we access the eviction set in an ordered way, then we access the whole conflicting set, and finally re-access again the eviction set, we will observe different number of misses depending on the policy. Pseudo LRU policies will probably evict all the data in the eviction set after accessing the elements in the conflicting set. Whereas other policies intended for good performance in these situations (burst accesses to memory) will probably incur fewer misses. As a result, we have located two regions composed of 64 cache sets in each slice that control each policy. Figure 3 represents all the sets of a cache slice with the control regions. The region coloured in blue controls the policy 1, and the region coloured in red controls the policy 2.

However, not all the sets within the aforementioned regions implement a fixed policy. Particularly, only one of the sets in each slice implements a fixed policy, the corresponding sets in the remaining slices will have a varying policy. This fact was discovered after multiple experiments with different patterns. The sets with fixed policy for each of the slices are depicted in figure 4. To obtain the actual control sets within the slice, it is important to test the sets without order, as it may seem that some sets have a fixed policy and they do not.

The policy we will uncover is the one implemented in the L3 cache. The policies implemented in the L1 and L2 caches can be different. We have been able to uncover a policy that seems to explain the observed evictions. In fact, over 98% of the evictions have been correctly predicted in all cases \(^1\), and it is likely that the errors were due to noise.

\(^1\)These results refer to the sets with fixed policy in the machines that

Table 1: Details of the machines used in this work to retrieve their Replacement Policies

| Processor   | Cores | L3 cache accesses | Core Memory |
|-------------|-------|-------------------|-------------|
| i7-4790    | 4     | 1                | Ubuntu 14   |
| i3-5010U   | 2     | 2                | Ubuntu 16   |
| i7-6700K   | 4     | 4                | Centos 7.0  |
| i5-7600K   | 4     | 4                | Centos 7.0  |
| i7-8650U   | 4     | 4                | Debian 9.5  |

Algorithm 2 Test of the desired eviction policy

Input: Eviction_set, Conflicting_set
Output: Accuracy of the policy

| Function | Description |
|----------|-------------|
| TEST    | function    |

if time ≥ 1l_threshold then
    Force miss candidate=getEvictionCandidate();

if testDataEvicted() == candidate then
    hits++;
Figure 2: Diagram that represents the process of data (D) retrieval whenever the processor makes a request. The blocks with green background represent a cache hit, whereas the blocks with red background represent a cache miss.

Figure 3: Location of the sets controlling the eviction policy within a slice of 2048 sets. Mode 1 (blue) and mode 2 (red).

Figure 4: Detailed representation of the sets with fixed policy within each of the slices for the i7-4790 machine.

Although we have observed differences between generations and some machines implement set dueling, the decision of which data is going to be evicted is the same in all cases. The replacement policy is always the same and what changes is the insertion policy. Due to space limitations and to avoid creating confusion, we only include here the description of the policies revealed by our experiments as the ones implemented in the Intel processors. Assuming that the policy is named Quad-Age LRU, in the following we refer to ages instead of control bits. Figure 2 represents the two possible situations whenever the processor requests a piece of data in our processors. If the data is in the LLC, the controller decreases the age of the requested element when giving it to the processor. If there is a cache miss and one element has to be evicted, the replacement policy will select the oldest one.

Intel processors use two bits to represent the age of the elements in the cache. Consequently, the maximum age is three. In case the reader wonders which block will be replaced in the case there are multiple blocks whose age is three, the answer is the first one it finds. The cache behaves somehow like an array of data, and when searching for a block of data placed on it, the controller always starts from the same location, which would be the equivalent to the index 0 in an array.

As we have already stated, the machines used in our experiments only differ in the insertion age; that is, the value that gets a cache line as age when first loaded in the set or when reloaded after a cache miss. Particularly, the i7-4790 and the i3-5010U machines (4th and 5th generation) that implement set dueling insert the elements with age 2 in one of the cases and with age 3 in the other. We denote each of these situations or working modes as mode 1 and mode 2 respectively. The i7-6700K, the i5-7600K and the i7-8650U machines (6th, 7th and 8th generations) always insert the blocks with age 2, which is equivalent to the mode 1 in the oldest machines.

In order to help the reader to understand how the cache works, figure 5 shows an example of how the contents of a cache set are updated with each access according to each policy. When the processor requests the line “d”, there is an empty block in the set, so “d” is located in that set and it gets age 2 (Mode 1) or age 3 (Mode 2). In mode 1, the eviction candidate is now “a” because it is the only one with age 3, whereas in mode 2 the eviction candidate is “d” as it has age 3 and is on the left of “a”. The processor then requests “b” so its age decreases from 2 to 1 in both cases. Accessing “g” causes a miss. The aforementioned eviction candidates will be replaced with “g”, and its age will be set to 2 or 3 respectively. Eventually, when the processor requests “a”, it will cause a miss in mode 1 (it was evicted on the previous step) and a hit in mode 2, so it will decrease its age.

4 RELOAD+REFRESH

If any kind of sharing mechanism is implemented, an attacker knowing the eviction policy can place some data that the victim is likely to use in the cache (the target) and in the desired position among the set. Since the position of the blocks and their ages (which in turn depend on the sequence of mem-
The number of ways in low level caches is lower than the without any cache misses (no attack trace). This is the main environments where multiple VMs are likely to place the same victim uses the as this address. Section he also needs to find an eviction set that maps to the same set target victim uses the target address. W e follow the procedure in algorithm Merging (KSM) in Linux [7] that improve memory utiliza- tion by merging multiple copies of identical memory pages into one. This feature was originally designed for virtual en-vironments where multiple VMs are likely to place the same data in memory, and was later included in the OSs. Although most cloud providers have disabled it, it is still enabled in multiple OSs. Although most cloud providers have disabled it, it is still enabled in multiple OSs. When enabled, the attacker needs some reverse engineering to retrieve the address he wants to monitor and he also needs to find an eviction set that maps to the same set as this address. Section 3 shows how to construct the eviction sets in order to find the one which creates a “conflict” with the target address. We follow the procedure in algorithm 1 replacing the conflicting set candidates with the target address.

We use figure 6 to depict the stages of the attack and the possible “states” of the cache set. The attacker first inserts into the cache the target address and then all the elements in the eviction set except one, which will be used to force an eviction. By the time the attacker has finished filling the cache with data, the target address will be in level 3 cache. The number of ways in low level caches is lower than the number of ways in the L3 cache, and since the L3 cache is inclusive it will remove the target address from the low level caches when loading the last elements of the eviction set. Even if the victim and the attacker are located in the same core, an access of the victim to the target address will update its age, so the attacker would be able to retrieve this information.

The data is placed in such a way that the target becomes the eviction candidate. The attacker then waits for the victim to access the target. If it does the eviction candidate changes and is now the element inserted in the second place. If it does not, the eviction candidate is still the target address. The attacker reads then the remaining element of the eviction set (ev_{w-1}), forcing this way a conflict in the cache set, and the eviction of the candidate. As a consequence, when reading (RELOAD) the target address again, the attacker will know if the victim has used the data (low reload time) or not (high reload time). The state of the cache has to be reverted to the initial one, so all the elements get the same age again (REFRESH). The element ev_{w-1} is forced out of the cache, so it could be used to create a new conflict on the next iteration.

When the cache policy is working in mode 2, each element is inserted with age 3. In this case, steps 1 to 5 are equivalent. However step 6 changes depending on whether the victim is allocated in the same core as the attacker or not. When not, the other elements have age 3 and the target is the eviction candidate, so there is no need to refresh the data for the attack. On the other hand, when they are on the same core, the attacker needs to remove the target from the low level cache by refreshing the other elements in the cache. Moreover, the

Figure 5: Sequence of data accesses in a cache set updating their content and their associated ages for the two observed policies. Mode 1 of the 4th and 5th generations behaves exactly the same as the 6th 7th and 8th generations. The red arrow points the eviction candidate, that is, the data that would be evicted in case of cache miss.
1) The attacker fills the set with the Target address and all the elements of the eviction set except one.

```
Target 2 ev0 2 ev1 2 ev2 2 evW−2 2
```

2) The attacker waits. The next state of the cache depends on whether the victim accesses (a) or not (b) the target address.

```
\begin{itemize}
  \item a) Target 1 ev0 2 ev1 2 ev2 2 evW−2 2
  \item b) Target 2 ev0 2 ev1 2 ev2 2 evW−2 2
\end{itemize}
```

3) The attacker forces a miss by reading evW−1. The evicted element depends on whether the victim had accessed (a) or not (b) the Target.

```
\begin{itemize}
  \item a) Target 2 evW−1 2 ev1 3 ev2 3 evW−2 3
  \item b) evW−1 2 ev0 3 ev1 3 ev2 3 evW−2 3
\end{itemize}
```

4) The attacker now reloads the Target address, it will be placed in different positions depending on the previous accesses.

```
\begin{itemize}
  \item a) Target 1 evW−1 2 ev1 3 ev2 3 evW−2 3
  \item b) evW−1 2 Target 2 ev1 3 ev2 3 evW−2 3
\end{itemize}
```

5) The attacker has to revert the changes. To ensure the Target gets age 2 and its placed in the "first" position, evW−1 has to be flushed, as it has to be the Target, then the Target is reloaded and finally ev0 is loaded.

```
\begin{itemize}
  \item a) Target 2 ev0 2 ev1 3 ev2 3 evW−2 3
  \item b) Target 2 ev0 3 ev1 3 ev2 3 evW−2 3
\end{itemize}
```

6) Accessing the remaining elements of the set will allow the attacker to get the cache as it was on the beginning.

```
\begin{itemize}
  \item a) Target 2 ev0 2 ev1 2 ev2 2 evW−2 2
  \item b) Target 2 ev0 2 ev1 2 ev2 2 evW−2 2
\end{itemize}
```

Figure 6: Sequence of possible cache set states during the attack for the mode 1 or the newest generations, starting with all elements in the set with age 2.

The mode 2 policy enables a detectable fast cross core cache attack that does not require shared memory. Once the cache set is filled with the attacker’s data, the eviction candidate is now the first element inserted by the attacker. If the victim uses the expected data, the eviction candidate will be replaced. Even if the victim uses the data multiple times, its age will not change, since it will be fetched from the low level caches. Then, after forcing a miss, the attacker only has to access the first element (eviction candidate) to check whether the victim has or has not accessed the target data. Note that with this access the attacker replaces the victim’s data (because it became the eviction candidate when loaded) so it is equivalent to the REFRESH. If, on the contrary, the victim does not use the data, the attacker’s data will still be in the cache. The attacker will then flush and reload this data to ensure it gets age 3 again.

Algorithms 3 and 4 summarize the steps of the RELOAD+REFRESH attack when the insertion age is two (newest Intel generations or mode 1 in oldest generations). The cache set is filled with the target address plus W − 1 elements of the eviction set during initialization. Then, the attacker waits for the victim to run the code. Later, he performs the RELOAD and REFRESH steps. The RELOAD step gives information about the victim accesses and the REFRESH step gets the set ready to retrieve information from the victim. When initializing the set, we first fill the set, then flush the whole set and finally reload the data again to ensure the insertion order.

In the RELOAD function it is not necessary to flush the Target_address unless it has not been used by the victim. The same assumption is true for the conflicting address or the element w − 1 of the eviction set, which would have to be flushed only in that situation. However, to avoid if conditions in the code, we have chosen to implement the RELOAD function this way. Low reload times mean the data was used by the victim, whereas high reload times mean it was not.

**Algorithm 3 Reload function**

**Input:** Eviction_set, Target_address

**Output:** Reload time

```
function RELOAD(Target_address,eviction_set)
  "rdsc";
  "mfence";
  read(eviction_set[w−1]); ▷ Forces a miss
  "mfence";
  flush(eviction_set[w−1]);
  "mfence";
  read(Target_address);
  flush(Target_address);
  "mfence";
  read(Target_address); ▷ Reload on first position
  "rdsc";
  read(eviction_set[0]);
  return time_reload;
```

The REFRESH function presented is meant for a 12 way set. Since the target and the first element of the eviction set have been loaded in the RELOAD step, the REFRESH function only has to access the remaining 10 elements of the set. To avoid out of order execution and ensure the order, the elements of the eviction set have to be provided as a linked list (one element contains the address of the following one). Additionally the refresh time can be used to detect if any other process is also using that set.

### 4.1 Noise tolerance

The proposed attack relies on the order in which the elements are inserted into the cache set to both avoid misses on the victim side and to learn information about the data that has been accessed. If other processes are running and using data that maps to the same cache slice (introducing noise), the efficiency of the attack can be lessened and also some detection...
Algorithm 4 Refresh function

Input: Eviction_set
Output: Refresh time

function REFRESH(Eviction_set)
    volatile unsigned int time;
    asm __volatile__(
        " mfence \n"
        " rdtsc \n"
        " movl %eax, %esi \n"
        " movq 8(%1), %rdi \n" ▶ Eviction_set[1]
        " movq (%rdi), %rdi \n"
        " movq (%rdi), %rdi \n"
        " movq (%rdi), %rdi \n"
        " movq (%rdi), %rdi \n"
        " movq (%rdi), %rdi \n"
        " movq (%rdi), %rdi \n"
        " movq (%rdi), %rdi \n" ▶ Eviction_set[w-2]
        " mfence \n"
        " rdtsvc \n"
        " subl %esi, %eax \n" ▶ Time value on %eax
    )
    return time_refresh;

mechanisms can be triggered.

As mentioned before, the refresh step can reveal such situations. Then, the attacker can slightly change the approach. Assuming that only one address is being used by the noise generating process, the attacker can easily handle noise, avoid detection and still gain information about the victim. The trick to deal with noise is placing the target on a different place within the set (the second place in this example). In case somebody else uses any data mapping to that set, the replaced data belongs to the attacker; specifically it is the data placed in first place in the set. When the attacker forces a miss, the eviction candidate will be either the target address (if the victim did not use it) or the element inserted in third place (the victim did use the target data). The attacker can gain information about the victim by reloading the target address and he must begin by refreshing the third element of the eviction set and finish with the first one which will evict the “noise” from the cache, so the age of all the blocks is 2 again.

5 Results

To show the applicability of RELOAD+REFRESH, we have replicated two published attacks: one against the T-Table implementation of AES and one against the square and multiply exponentiation implementation included in RSA. Although both implementations have been replaced by new ones, we use them for comparison. All the experiments presented in this section have been performed in the intel i5-7600K machine.

5.1 Attacking AES

The T-Table implementation used to be a popular software implementation of AES. While still available, this implementation is not the default option when compiling the OpenSSL library due to its susceptibility to micro architectural attacks. This implementation replaces the SubBytes, ShiftRows and MixColumns operations with table lookups (memory accesses) and XOR operations. Since the accesses to the T-Tables depend on the secret key, an attacker monitoring just one line of each T-Table is able to recover the full AES key.

Our scenario is similar to the one described by Irazoqui et al. in [6]. They focused in retrieving information about the last round of the AES encryption process, where the ciphertext is obtained by performing one XOR operation between an element contained in the tables and the secret key. As the content of the tables is publicly available from the source code, they obtained the secret key xoring it with the ciphertext.

Besides performing the attack against the AES T-Table implementation (OpenSSL 1.0.1f) using the RELOAD+REFRESH (R+R) technique, we have performed the same attack using the FLUSH+RELOAD (F+R) and PRIME+PROBE (P+P) techniques, to provide a fair comparison regarding the number of traces required to obtain the key. In order to retrieve the whole key, the attacker has to monitor at least one line of each T-Table. The attacker can monitor from one up to four lines at a time. For this comparison we monitor one table at a time.

Table 2 shows the results for each of the approaches. In this scenario the attacker performs one operation, then the victim performs the encryption, and finally the attacker retrieves the information about the victim. That is, victim and attacker do not interfere with each other while doing the different operations. As it can be inferred from the table, our approach performs almost as good as FLUSH+RELOAD, and clearly outperforms PRIME+PROBE.

Table 2: Mean number of samples required to retrieve each four byte group of the whole AES key when monitoring one line per encryption.

| Attack | R+R | F+R | P+P |
|--------|-----|-----|-----|
| Samples | 110000 | 108000 | 220000 |

5.1.1 Detection evaluation

RELOAD+REFRESH is able to retrieve an AES key with a negligible impact on the victim process. We compare the
shows the distribution of the number of misses the victim process by the different attacks, and with no attack. Each includes 1 million samples.

Figure 7: Distribution of the number of misses induced in the victim process by the different attacks, and with no attack. Each includes 1 million samples.

Figure 8: Distribution of the encryption times in different situations. Each distribution includes 1 million samples.

number of cache misses the victim suffers per encryption performed, for all the attacks and for normal executions. We use the PAPI software interface [43] to read the counters referred to the victim. PAPI allows us to insert one instruction just before and another one just after the encryption process to read the L3 cache misses counter, which is mainly the information used for cache attack detection [9,11,34,60]. As a result, figure 7 shows the distribution of the number of misses the victim sees for each attack and for the normal execution of the encryption.

As figure 7 shows, our attack can not be distinguished from the normal performance of the AES encryption process by measuring the number of misses. Note that, when performing the PRIME+PROBE attack against AES, around 20% of the times the attacker does not cause misses on the victim. When retrieving the information about the victim using this approach, we first perform a PRIME, then wait for the victim to perform an encryption and finally perform a PROBE. During the PRIME stage the elements in the eviction set are accessed from 0 to 11, whereas in the PROBE step they are accessed the opposite way, in a zig-zag pattern. Due to the eviction policy and to the zig-zag pattern some of the elements still reside in low level caches and their ages are not updated. As a consequence, the attack is not able to evict the victim’s data from the cache, so the victim does not see any miss and it is likely that the attacker sees a false positive.

Additionally, we use the rdtsck instruction to measure the time it takes to complete each encryption and show the results in figure 8. The differences observed in figure 8 between the normal encryption and the RELOAD+REFRESH approach are not significant if we compare them with the other attacks. The mean encryption time when there is no attack is 595 cycles, whereas it increases up to 623 cycles when attacked with the RELOAD+REFRESH technique. This time difference exists because, when suffering the RELOAD+REFRESH attack, the victim has to load the data from the L3 cache instead of loading it from the L1 or L2 caches.

5.2 Attacking RSA

RSA is the most widely used public key crypto system used for data encryption as well as for digital signatures. Its security is based on the practical difficulty of the factorization of the product of two large prime numbers. RSA involves a public key (used for encryption) and a private key (used for decryption). There are many algorithms suitable for computing the modular exponentiation required for both encryption and decryption. In this work we focus in the square and multiply exponentiation algorithm [15] as Yarom et al. did in [57].

Square and multiply computes \( x = b^e \mod m \) as a sequence of Square and Multiply operations (followed by a Modulo Reduce) that depend on the bits of the exponent \( e \). If the bit happens to be a 1, then the Square-Multiply-Reduce sequence of operations is executed. On the other hand, if the bit is a 0, only the Square-Reduce operations are executed. As a consequence, retrieving the sequence of operations executed means recovering the exponent; that is, the key.

As a difference with the attack against AES, we monitor instructions instead of data. Additionally, an attack against RSA needs to have enough time resolution to correctly retrieve the sequence of operations. As we did with AES, we performed the attack using our stealthy technique as well as the FLUSH+RELOAD and PRIME+PROBE techniques.

In this work we use the libgcrypt version 1.5.0, which includes the aforementioned square and multiply implementation. The key length in our experiments is 2048 bits. When attacking RSA it is possible to monitor all the functions implied in the exponentiation or just one. When monitoring all the instructions the attacker is able to reconstruct the sequence of observations, when monitoring only one instruction the attacker has to use the differences of times between occurrences of the monitored event to retrieve the key. Since our purpose is to compare the ability of our approach to obtain information about the victim, we only monitor the multiply operation. All the attacks were configured to obtain a sample with the same time resolution (3000 cycles), to ensure the differences in accuracy are due to the attack technique.

Figure 9 shows an example of part of a retrieved trace using the RELOAD+REFRESH approach. The trace corre-
sponding to the real sequence of squares and multiplies is represented as blue bars with different values, 800 means a square was executed and 700 it was a multiply. Since the timestamp is collected after each exponentiation operation has finished, and the timestamp of the attack samples after the reload operation, it may seem that there is some misalignment between traces.

The results of our experiments are summarized in Table 3. The accuracy is given as the number of multiplies correctly detected divided by the number of multiplies really executed during the RSA decryption. The percentage of false positives is obtained as the total number a multiply was detected minus the number of correctly detected operations, divided by the total number of detected multiplies:

\[ FP = \frac{\text{Mul}_{\text{detected}} - \text{Mul}_{\text{correct}}}{\text{Mul}_{\text{detected}}} \]

Again, the RELOAD+REFRESH performance is similar to FLUSH+RELOAD. The increase in the number of false positives for the PRIME+PROBE approach is most likely due to the way each sample is obtained. In this case, we measure the prime time, then wait for around 3000 cycles, and then measure the probe time, and so on and so forth. Each prime or probe operation gives the time measurement required for detecting the accesses. Taking into the account the eviction policy, it is expected that sometimes the victim data still resides in the cache after a prime or probe step.

Table 3: Percentage of samples correctly retrieved and false positives generated by each approach when attacking RSA.

| Attack   | R+R   | F+R   | P+P   |
|----------|-------|-------|-------|
| True positives | 94.9% | 97.25% | 96.16% |
| False positives | 38.75% | 38.86% | 57.25% |

5.2.1 Detection evaluation

We have monitored the number of cache misses detected when executing a RSA decryption. Figure 10 includes the resulting distributions for 1000 samples without attack and applying the considered attacks. The number of total misses increases compared to the no-attack case for the FLUSH+RELOAD attack. However, it decreases for both the RELOAD+REFRESH and PRIME+PROBE attacks, being RELOAD+REFRESH the approach causing the minimum amount of misses. This result is explained due to the monitoring process, to the PRIME+PROBE attack that does not evict the data from the cache, and to the fact that in the RSA decryption most misses happen at the beginning of the process. These results prove that the total amount of misses per decryption is not indicative of an attack going on for RSA.

For this reason we have also monitored the victim LLC misses periodically, with a sampling rate of 100 µs. The results obtained in this case confirm that the main differences between RELOAD+REFRESH and the normal operation of the decryption process occur during the initialization steps. During this initialization, the number of misses caused by RELOAD+REFRESH and PRIME+PROBE is lower than in the normal execution. Later, when the number of misses of the normal operation tends to zero, the number of misses for the RELOAD+REFRESH is also close to zero. On the contrary, both FLUSH+RELOAD and PRIME+PROBE cause a noticeable amount of misses. Since detection mechanisms such as CacheShield [9], define a region in with some misses are tolerated to avoid false positives, our attack will not trigger an alarm. Figure 11 shows the section of the decryption process in which the number of misses has become stable.

For each sample we get with the RELOAD+REFRESH approach, we have to perform both operations and then wait for 3000 cycles. The RSA decryption process runs in parallel, which means both victim and attacker can try to access the memory simultaneously. If the victim tries to execute the multiply operation when the attacker is flushing and reloading the mentioned line, the victim may get a miss. Therefore, a few misses can be observed in figure 11 for our approach.

6 Discussion of the results

The absence of randomness in the replacement algorithm makes it possible to accurately determine which of the elements located in a cache set will be evicted in case of conflict. Also, the accurate timers included in Intel processors altogether with the cflush instruction allow to trace accesses to the different caches and to force the cache lines to have the desired ages, we exploit these facts to run undetectable attacks.

RELOAD+REFRESH is just one way to exploit the eviction policy assuming some kind of memory sharing mechanism enabled. In the case that the victim and the attacker do not share memory, our proposal can be adapted so the attacker can track his own data. The attacker has to prepare the data in the set, in such a way that once the victim places his data in the cache, the eviction candidate is one of the elements the attacker controls. The target address will only be evicted if not used by the victim, who will see a cache miss the next time that tries to use it. If there is an encryption process going on, the most likely situation is that the victim will evict the data. As a result, the number of misses will be limited. This is a new idea, that would lead to different results and a new attack, that we leave for future work.

The knowledge of the eviction policy, enables the usage of a different access pattern to gain the information about the victim and to ensure its data is really evicted from the cache, reducing the amount of false positives. Thus, PRIME+PROBE attacks, EVICT+RELOAD attacks or any attack requiring to evict some data from the cache can benefit from our results. Moreover, the PROBE step can, in some cases, be reduced to just one access to the eviction candidate.
Figure 9: Example of a retrieved trace referred to an execution of a RSA decryption. The blue bars represent the real execution of squares (points equal to 800) and multiplies (700). The yellow line represents the information retrieved, low reload times mean detection of the multiply execution.

Figure 10: Distribution of the number of misses induced in the victim process by the different attacks, and with no attack.

Figure 11: Detail of a trace of misses measured each 100 μs for each of the approaches.

6.1 Performance of Reload+Refresh

As a difference with traditional cache attacks, one of our main objectives is to be stealthy. This involves we should cause as few cache misses and as low delay as possible on the victim process. Consequently, our sampling rate has to be at least the same as the rate at which the victim using its own data. We have already showed that it is possible to extract information referring to a RSA decryption, however in this section we discuss the performance of our approach and the resolution penalty paid as the price for stealthiness. Compared with traditional attacks such as PRIME+PROBE or FLUSH+RELOAD, our proposal is more sophisticated and involves extra steps in order to retrieve the same information.

RELOAD+REFRESH includes an access to one address not located in the working set (the conflicting address) plus some others accesses focused in checking if the data has been replaced and in re-allocating the data in the desired places within the cache set. As a consequence, it induces some misses on the attacker side and the corresponding delays. In our test machine we have measured the time in cycles it takes to perform both the RELOAD (1012) and the REFRESH (447) operations as well as the mean time resulting of performing the two operations sequentially, that is, the maximum sampling rate (1520). When the number of ways per set increases, we do not expect variations in the RELOAD time, however there will be a proportional increase in the REFRESH time as it would be for a PRIME+PROBE attack.

Regarding to the capability of the channel to extract information, FLUSH+RELOAD attacks are the fastest and most accurate. RELOAD+REFRESH attacks do not lose accuracy, nevertheless, their performance is degraded due to the extra accesses. The mean times between samples that we have measured for the FLUSH+RELOAD attack is about 260 cycles, whereas this time is 810 cycles for PRIME+PROBE. Note that in the PRIME+PROBE approach the time varies between 280 and 1950, which is a great variation and makes it harder to accurately obtain samples with resolutions below 1950.

To provide more insights into the resolution required to obtain data from algorithms such as RSA, we have gathered time measurements between calls to square and multiply. This time is approximately 1400 cycles for keys with 1024 bits and 3100 cycles for keys with 2048 bits. When the key length of RSA is 1024 bits, both PRIME+PROBE and RELOAD+REFRESH may have trouble getting the proper number of samples. However, we have been able to accurately retrieve 93% of the multiply executions gathering the information at maximum speed with the RELOAD+REFRESH attack.
7 Conclusion

This work presented a thorough analysis of cache replacement policies implemented in Intel processors covering from 4th to 8th generations. To this end, we have developed a methodology that allows us to test the accuracy of each policy by comparing the data that such policy selects as the eviction candidate with the data truly evicted after forcing a miss.

The RELOAD+REFRESH attack builds on this deep understanding of the platforms replacement policy to stealthily exploit cache accesses to extract information about a victim. We have demonstrated the feasibility of our approach by targeting AES and RSA and retrieving as much information as we can retrieve with other state of the art cache attacks. Additionally, we have monitored the victim while running these attacks to confirm that our attack causes a negligible amount of last level cache misses, rendering it impossible to detect with current countermeasures.

These results are not only useful for broadening the understanding of modern CPU caches and their performance but also for improving previous attacks and eviction strategies. Our work also demonstrates that new detection countermeasures have to be designed to protect against RELOAD+REFRESH.

Acknowledgment

Visit of Samira Briongos to Lübeck has been supported by a grant from the Universidad Politécnica de Madrid. This work was in part supported by the National Science Foundation under Grant No. CNS-1618837 and by the EU (FEDER), under contract RTC-2016-6090-3, the Centre for the Development of Industrial Technology (CDTI), under contracts IDI-20171183 and IDI-20171194.

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