A Common-Gate, $g_m$-boosting LNA Using Active Inductor-Based Input Matching for 3.1–10.6 GHz UWB Applications

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ABSTRACT

This paper presents the circuit of a low-noise amplifier (LNA) using active inductor (AI) input matching with common gate (CG) current-reused technique. This configuration is implemented in 90 nm CMOS and enables to achieve high power-gain ($S_{21}$) with ultra-wideband (UWB) input matching at low power levels. Utilization of modified high-Q AI at the input side of the proposed LNA reduces the number of inductors and achieves UWB from only two inductors. Proposed LNA dissipates 10.4 mW from 1.0 V supply and exhibits an $S_{21}$ response of 18.0 $\pm$ 0.8 dB for 3.1–10.6 GHz with a maximum and average $S_{21}$ of 18.8 dB and 18.22 dB, respectively. The proposed LNA has noise-figure (NF) equal to 3.36–4.68 dB, with input ($S_{11}$) and output ($S_{22}$) reflection coefficients of less than $-9.3$ dB and $-11.35$ dB, respectively across the entire UWB range.

Index Terms—Active-inductor, common-gate, current-reuse, low noise amplifier, UWB

I. INTRODUCTION

Due to the demand for high data rates in wireless communication, ultra-wideband (UWB) technology has attracted great attention. Demand for a high data rate can be achieved using UWB technology as it consumes very less power and requires less complex receiver architectures [1,2]. Not only this, nowadays, every communication media ranging from TV receiver to telephone receiver has changed from wired to wireless and every wireless communication system needs one or other form of transceiver circuit which consists of a low-noise amplifier (LNA) as a first active key component [3-7]. The signal which an LNA receives from antenna needs to be amplified by the LNA without adding much noise to it. The overall performance of a receiver circuit depends upon the sensitivity of the LNA circuit and it has to satisfy various parameters such as low-noise figure (NF), high power gain ($S_{21}$), wideband input ($S_{11}$) and output ($S_{22}$) matching, high linearity, and unconditional stability.

In order to accomplish all these objectives, different LNA topologies have been proposed by many researchers and each of these topologies have a trade-off between various performance parameters. Based upon complementary metal-oxide semiconductor (CMOS) configurations, common source (CS) [4,5,8-12] and common gate (CG) [6,7,13-18] are the two broad categories in which these LNAs can be classified. These topologies are shown in Fig. 1. Common source resistive termination (CS-RT) LNA can be used for wideband impedance matching but at the cost of high NF, as a resistor at the input of the transistor adds thermal noise to the signal [5]. Feedback LNA achieves wideband impedance matching but at the cost of high NF, as a resistor at the input of the transistor adds thermal noise to the signal [5]. Feedback LNA achieves wideband impedance matching with an NF better than CS-RT as the signal is not attenuated with the noisy resistor before amplification [4]. For example, LNA presented in [8] achieves 12.4 dB $S_{21}$ with NF of 2.7–3.7 dB. Common source inductive degeneration (CS-ID) topology provides high $S_{21}$ with low NF and good input matching for narrowband applications [19,20]. Distributed LNA employs several parallel transistors to achieve extreme wideband input matching and provides small additive gain and high NF as reported in [21,22].

Common gate LNA renders a fairly higher NF as compared to CS amplifiers and a large area is occupied by the inductors used. However, it shows wideband behavior due to its simple and easy achieve input impedance matching by maintaining the transconductance of input
CG transistor close to 20 mS [14]. Common gate followed by CS (CG-CS) noise-canceling technique shown in Fig. 1(f) utilized in [23-25] is still unable to resolve the problem of large chip area. Several methods have been utilized to decouple the trade-off between NF and impedance matching, but the trade-off has not been fully decoupled.

For the matching network, most of the LNAs use bulky passive inductors requiring several hundred micrometers of interconnects. These passive inductors also possess fixed inductance values and poor quality factors [26]. Thus, to reduce the chip area, active inductor LNA topologies have been used in [27-29]. The active inductors are advantageous in the sense that they have tunable inductance value, less cost and high-quality factor, and smaller chip area. An LNA architecture employing active inductor for the input matching is presented in this paper.

The rest of this manuscript is organized as follows: In Section II, the $g_m$-boosting mechanism and active inductor are discussed. Section III discusses the proposed LNA circuit and its operation. Input impedance, output impedance, and stability of the proposed LNA are also analyzed in Section III. The results for the proposed LNA are discussed in Section IV. Finally, Section V concludes this manuscript.

II. METHODOLOGY ADOPTED

A. $g_m$-Boosting Mechanism in LNA

Common gate configuration with $g_m$-boosting technique is implemented to design an LNA with high gain over the entire UWB besides dissipating very less power. There is a tight coupling between NF characteristics and input impedance matching of CG-LNA. To enhance the performance and to overcome its drawbacks, $g_m$-boosting technique is a decent choice. The NF of CG-LNA is restricted by $1/g_m$, and thus can be decreased by increasing the transconductance ($g_m$). At the other aspect, for input matching $R_i$ ($\approx 1/g_m$) is set to 50 Ω. Because of the input matching condition, $g_mR_i = 1$, it is not favorable to increase the transconductance randomly in order to reduce the noise factor as the noise factor has an inseparable link with input matching condition. However, by employing the $g_m$-boosting technique, the NF performance can still be improved by decoupling the input matching and noise figure.

Fig. 2, shows a CG-LNA with $g_m$-boosting. An amplifier with negative gain ($-A$), when inserted between the source and gate terminal of the input CG-stage, will increase the overall transconductance. The input signal is applied to the gate of transistor $M_1$ after being amplified by $-A$ by the inverting gain block; hence, the transconductance of the CG amplifier is increased by $(1 + A)$ times.

The input matching condition becomes $(1 + A) g_mR_i = 1$, thereby reducing the NF by a factor of $(1 + A)$, relaxing the stringent requirements on the noise factor. The channel noise of input transistor in $g_m$-boosted CG-LNA is less because it requires a lower bias current. In Fig. 2, the inverting gain is achieved by using a CS amplifier.

B. Active-Inductor (AI)

Although passive spiral inductors have a wide variety of applications, they suffer from a number of disadvantages as well. The major disadvantages of passive inductors are limited inductance value and simultaneously have low self-resonance frequency which is non-tunable. Low-quality factor ($Q$) and large silicon area are another disadvantages of passive inductors. Contrarily, active inductors possess many important advantages such as reduced chip area requirement, high resonance frequencies with high tunable $Q$, and inductance value.
The block diagram of a gyrator-based AL with its schematic as shown in Fig. 3 is utilized in the proposed LNA circuit and it consists of a positive and a negative transconductance amplifiers connected back to back [26].

In this active inductor, after biasing through the current sources $I_{b1}$ and $I_{b2}$, the transistor $M_{1}$ provides negative transconductance, whereas the transistor $M_{2}$ provides positive transconductance. This circuit converts capacitance $C_{g}$ which includes gate-drain parasitic capacitance of $M_{1}$ and other parasitic capacitances into its equivalent active inductor as shown in Fig. 3(c). The input admittance ($Y_{in,act,ind}$) can be expressed as

$$Y_{a,act,ind} = \frac{1}{Z_{in,act,ind}} = sC_{p} + \frac{1}{R_{p}} + \frac{1}{R_{s} + sL_{eq}} \quad (1)$$

where

$$C_{p} = C_{g1}; \quad R_{p} = (g_{ds1} + g_{m2})^{-1}; \quad R_{s} = g_{ds2}(g_{m3}g_{m2})^{-1}; \quad L_{eq} = C_{g2}(g_{m3}g_{m2})^{-1} \quad (2)$$

The diagonal-source output conductances at node 1 and 2 are given by $g_{ds1}$ and $g_{ds2}$, respectively. Solving for the small-resonating frequency ($\omega_{0}$) and quality factor ($Q$) of the active-inductor in (3) and (4) as

$$\omega_{0} = \frac{1}{\sqrt{C_{p}L_{eq}}} \left( \frac{R_{p}}{2} \right) \quad (for \ small \ R_{s}) \quad (3)$$

and

$$Q = \frac{R_{s}}{R_{p}} \left( \frac{1}{\omega L_{eq} - \omega C_{p}(R_{s}^{2} + \omega^{2}L_{eq}^{2})} \right) = \frac{R_{p}}{\omega L_{eq}}, \quad for \ R_{s} \gg \ R_{s} \quad (4)$$

For achieving good quality, high $Q$ in high value of $R_{s}$ and small value of $R_{s}$ are always expected from the active inductor. The active inductor circuit utilized at the input of the proposed LNA is shown in Fig. 4a, where $C_{p}$ here includes gate-drain parasitic capacitance of $M_{1}$ and $M_{2}$ respectively. The ideal current sources $I_{b1}$, $I_{b2}$, and $I_{b3}$ are always expected from the active inductor. The active inductor shown in Fig. 4a can be expressed as

$$\omega_{0} = \sqrt{\frac{g_{m}g_{m2}}{C_{g1}C_{g2}}}, \quad Q = \sqrt{\frac{g_{m}g_{m2}g_{m3}C_{g1}}{g_{m}g_{m2}C_{g1}}} \quad (6)$$

It is clear from equation (6) that the resonant frequency of the active inductor shown in Fig. 4 is directly proportional to $g_{m1}$ and $g_{m2}$ whereas its $Q$-factor is directly proportional to $g_{m1}$, $g_{m2}$, and $g_{m3}$. The variation in $Q$-factor with frequency for the active inductor used in this LNA is shown in Fig. 4(c) and it achieves a minimum $Q$-factor of 7.3 for 3.1–10.6 GHz frequency range.

III. PROPOSED ACTIVE INDUCTOR-BASED LNA

The proposed $g_{m}$-boosted active inductor-based LNA with CG as input stage is shown in Fig. 5. The active inductor topology here is used for input-impedance matching whereas the CG topology with $g_{m}$-boosting is employed here for achieving high gain and low NF over the UWB frequency range.

The input matching network is designed using a gyrator-C-based AL realized by transistors $M_{1}$, $M_{3}$ forming positive transconductance and biased using current sources $I_{b1}$ and $I_{b3}$ whereas $M_{1}$ is forming negative transconductance and biased using $I_{b2}$. The active inductor is connected in conjunction with the CG stage to achieve the matching condition. The transistor $M_{4}$ is in CG mode and the inverting gain block is realized using CS transistor $M_{5}$. The transistor $M_{4}$ is connected between the gate-to-source terminal of CG transistor $M_{5}$, thus boosting its transconductance by a factor of $A = g_{m1}/R_{s}$ without increasing the bias current. Increasing the transconductance by $A$ times, the noise factor is reduced by the same amount thus decoupling the noise factor and input matching characteristics. The effect of adding $g_{m}$-boosting transistor $M_{4}$ on $S_{21}$ and NF is shown in Fig. 6. Also, the CG configuration reduces the Miller effect and provides a better isolation to the output signal and a noise factor relatively independent of frequency. The bias network of $M_{4}$ comprises of gate biasing resistor $R_{g}$ and the coupling capacitor $C_{g}$. Similarly, the resistor $R_{s}$ and capacitor $C_{g}$ form the bias network of $M_{5}$.

The output of $M_{4}$ is loaded by LC tank in which inductor $L_{1}$ is tuned with gate-drain capacitance of $M_{5}$. Signal matching from stage-1 to stage-2 is achieved by another serially tuned LC tank formed by inductor $L_{2}$ and gate-source parasitic capacitance $C_{gs}$ of successive gain-stage formed by transistor $M_{5}$.
Transistor M₇ acts as the buffer stage with the current source load being modeled by M₈ and the biasing resistance R₇. The individual elements used in the proposed LNA with their values are listed in Table I.

A. Circuit Analysis of Proposed

1) Input Matching Analysis

As is well known, the input impedance of the LNA should be matched with the source impedance Rₛ for maximum power transfer and least reflections, where Rₛ is the receiver’s antenna resistance. The simplified small-signal equivalent circuit of the input stage for calculating input impedance of the proposed LNA is shown in Fig. 7. For small-signal analysis, the biasing capacitors C₁ and C₃ are considered as short-circuited. The resistance Rₑq shown in Fig. 7 is parallel combination of 1/g₄, R₂ and R₃ (i.e., Rₑq = (1/g₄)||R₂||R₃).

The input impedance of the proposed LNA can be approximated as:

\[ Z_{in,LNA} \approx Z_s \left( \left| \frac{1}{j \omega C_{gs4}} \right| \right) \tag{7} \]

where Zₕ,LNA is the total impedance of the active inductor, Cₕₛ₄ is the gate-to-source capacitance of M₄, and impedance Zₛ is given by:

\[ Z_s = \frac{V_s}{I_s} = \frac{1 + Z_{load} g_{ds5}}{g_{m5} + g_{ds5}} \tag{8} \]

where gₘ₅ is the transconductance of M₅ and Zₕₕₕₕ is the load impedance. The input reflection coefficient (S₁₁), which is a function of input impedance Zₕₕₕₕ and source resistance Rₛ, is given by:
The major portion of wideband input matching is provided by the $1/g_{m5}$, whereas the rest is contributed by the input impedance of active inductor and the $g_{m}$-boosting stage. The input impedance matching ($S_{11}$) for different values of $g_{m1}$, $g_{m4}$, and $g_{m5}$ is shown in Fig. 8 from which it is depicted that transistor M1 of AI and transistor M4 of input CG-stage are playing an important role in achieving UWB input matching.

2) Output Matching Analysis

Another issue responsible for achieving a good LNA circuit design is output impedance matching which can be defined using output reflection coefficient ($S_{22}$). The ac equivalent of the output buffer stage is shown in Fig. 9.

Exploiting the ac analysis of output stage, the output impedance ($Z_{\text{out,LNA}}$) is given by:

$$Z_{\text{out,LNA}} = \frac{V_{\text{out}}}{I_{\text{out}}} = \frac{r_{d7}}{1 + g_{m7} \cdot r_{d8}} \frac{g_{m7} \cdot r_{d8}}{1 + g_{m7} \cdot r_{d8} \cdot (j \omega C_{g7})^{-1}}$$

(10)

where $r_{d7} = (g_{ds7})^{-1}$, $r_{d8} = (g_{ds8})^{-1}$, $g_{m7}$ and $C_{g7}$ are transconductance and gate-to-source parasitic capacitance of $M_7$ and $M_8$, respectively and then $S_{22}$ can be expressed as:

$$S_{22} = \frac{Z_{\text{out,LNA}} - R_s}{Z_{\text{out,LNA}} + R_s}$$

(11)

C) Noise Analysis

For the NF analysis, the small-signal noise equivalent circuit of the proposed LNA is shown in Fig. 10, where the drain-induced channel thermal noise is considered as the main source of noise in transistors used in active inductor and the CG current reused.

Absolutely, the noise added by the active inductor at node1 cannot be ignored; therefore, the total root-mean-square (rms) noise voltage due to active inductor circuit at node 1 can be represented as:

$$V_{n,\text{out,act.ind}}^2 = \frac{V_{n,\text{out,act.ind}}^2}{R_s} + \frac{V_{n,\text{out,act.ind}}^2}{R_s}$$

(12)

where, $V_{n,\text{out,act.ind}}^2$ represents noise voltage due to $M_7$, $M_5$, and $M_4$ respectively. If $V_{n,\text{out,Rs}}^2$ is the output noise due to source resistance $R_s$, then Eq. (12) can be expressed as:

$$V_{n,\text{out,act.ind}}^2 = R_s \left[ \frac{g_{m7} \cdot g_{m3}}{g_{m3} + g_{m7}} \right] \frac{1}{\alpha} \left[ C_{g7} + g_{ds7} \right] + \frac{g_{m7} \cdot g_{m3}}{\alpha} V_{n,\text{out,Rs}}^2$$

(13)
The output noise due $i_{n,3}$ and $i_{n,4}$ can be expressed as:

$$V_{n,4}^2 = \frac{K}{P^2} \gamma g_{m4} V_{n,4}^2$$

and

$$V_{n,5}^2 = \frac{K}{P^2} \gamma g_{m5} V_{n,5}^2$$

respectively. Whereas the noise due to $V_{n,3}$ is given by:

$$V_{n,3}^2 = K R_2 \frac{g_{m3}}{P^2 R_s} V_{n,R_1}^2$$

where,

$$V_{n,R_1}^2 = \frac{P^2}{K} V_{n,R_1}^2$$

$$K = \left[ R_2 \left( \frac{1}{R_s g_{m5}} \left( \frac{1}{Z_{in,act,ind}} + \frac{1}{Z_{in,act,ind}} \right) + g_{m4} \left( \frac{1}{R_s} + \frac{1}{Z_{in,act,ind}} \right) \right) \right]^{-1}$$

**Fig. 8.** Input reflection coefficient ($S_{11}$): (a) effect of $g_{m1}$, (b) effect of $g_{m2}$ boosting, and (c) effect of input common-gate stage.

**Fig. 9.** AC equivalent of the buffer stage.
Fig. 10. Small-signal noise equivalent circuit of AI-based LNA.

Fig. 11. Variation in NF: (a) with $g_{m1}$, (b) $g_{m5}$ of input common gate stage.
Fig. 12. LNA characteristics: (a) noise-figure and (b) S-parameters.

Fig. 13. (a) NF, (b) $S_{21}$, and (c) $S_{11}$, at various $V_{dd}$ supply.
Therefore, the NF of the proposed LNA can be expressed as:

\[
NF \approx 1 + \frac{g_{m5}(1 + A)}{R_s} \left( 1 + \frac{1}{Z_{\text{act,ind}}} + g_{m5}(1 + A) \right)
\]

Equation (17) and Fig. 11 reveals that NF can be reduced by considering small-sized transistor for M1 and large size for M5. Antenna source resistance matching simultaneously with low NF can be achieved by a parallel combination of impedance due to feedback loop of M4 and M5, and input impedance of the active inductor (i.e., \(Z_{\text{act,ind}}\)).

**IV. RESULTS AND DISCUSSION**

The proposed \(g_m\)-boosting AI-based CG LNA was simulated using Cadence Spectre RF at a \(V_{dd}\) supply of 1.0 V. Fig. 12 shows the results of NF and S-parameters. It is observed that NF has a span of 3.36–4.68 dB with a power gain in the range of 17.22–18.79 dB over the UWB frequency range of 3.1–10.6 GHz. The achieved values for \(S_{11}\) and \(S_{22}\) are less than \(-9.31\) dB and less than \(-11.35\) dB, respectively. The proposed LNA is a suitable option for wireless local area network (WLAN) receivers as a flat gain response of 18.0 ± 0.8 dB with a minimum NF of 3.362 dB and excellent matching is achieved for the entire UWB frequency range. The NF of the proposed circuit is slightly higher due to the use of active inductor for input matching but it reduces the chip area. As the input RF signal is applied at the source terminal of input CG configuration, it results in a good reverse isolation of better than \(-64.36\) dB for the entire bandwidth.

Fig. 13 shows the characteristics of the proposed AI-based LNA at 0.8 V, 1.0 V, and 1.2 V of \(V_{dd}\) supply. It has been observed that as supply voltage increases from 0.8 V to 1.2 V, the power gain increases, which decreases the value of NF but the input matching deteriorates. The value to NF varies from a minimum of 3.215 dB at \(V_{dd}\) equal to 1.2 V.

![Fig. 14. (a) NF, (b) S21, and (c) S11, at different temperatures.](image-url)
to a maximum of 4.958 dB at $V_{dd}$ equal to 0.8 V, whereas $S_{11}$ varies from 14.70 to 20.34 dB, with a standard deviation of 1.55 dB from its average value of 18.096 dB. The minimum value of $S_{11}$ varies from less than $-8.193$ dB to less than $-9.688$ dB.

Further, it is always desired from a designed LNA that, with the change in operating temperature, the performance parameters should remain in the acceptable range. The stability of the system parameters $NF$, $S_{21}$, and $S_{11}$ against temperature variation at different temperatures of $-25°C$, $0°C$, $25°C$, and $50°C$ is shown in Fig. 14. This LNA achieves $NF$ of 3.24 dB at $25°C$ to 5.05 dB at $50°C$ and $S_{21}$ greater than $15.90$ dB and $S_{11}$ less than $-6.90$ dB at different temperatures. The extremes of the parameter variations within which a circuit must function properly can be represented by process corners. Fig. 15 shows $NF$, $S_{21}$, and $S_{11}$ at different process parameters with a comparison with LNA discussed in this paper. Due to process variation, $NF$ varies from 3.35 to 5.52 dB, minimum $S_{21}$ varies from 13.28 dB to 18.22 dB, and $S_{11}$ of less than $-7.3$ dB.

The linearity performance of the proposed LNA is observed in terms of 1-dB compression point ($P_{1dB}$), the power gain and the output signal power at $P_{1dB}$, third-order intercept point ($IIP_3$), and the second-order intercept point ($IIP_2$). The linearity performance plots for the proposed LNA are shown in Fig. 16. The simulated 1-dB compression point of the proposed LNA is approximately $-32.3$ dBm with a flat gain of approximately 17.1–18.1 dB. The proposed LNA provides an output signal power ($P_{out}$) of $-15.3$ dBm at $P_{1dB}$ as shown in Fig. 16(c). Two-tone test is performed at center frequency of 6 GHz with $f_1 = 5.995$ GHz and $f_2 = 6.005$ GHz spaced at 10 MHz in order to analyze $IIP_3$. The simulated $IIP_3$ for the proposed LNA was found to be $-22.8$ dBm as can be seen from Fig. 16(d). For a UWB LNA, it is also important to analyze second-order linearity in case of direct-conversion type receiver architectures. The simulated $IIP_2$ of the proposed LNA is $-16.8$ dBm as shown in Fig. 16(e).

The phase linearity of the proposed LNA is observed in terms of group-delay variations. Due to the presence of two large-sized inductor, the proposed LNA achieves a group delay of $85.60 \pm 25.2$ ps for 3.1–10.6 GHz frequency range and is found comparable with the other LNAs reported in [16,20] as shown in Fig. 17.

The oscillations occur at the output of the LNA if the system is not stable. So stability is an important performance parameter. The LNA should be unconditionally stable over the entire bandwidth which can be analyzed by using Rollett’s stability factor ($K$). For a system to be stable, it should satisfy the conditions expressed by equations (18) and (19):
The stability-factor plots for this LNA is shown in Fig. 18, and the value of $K$ is much greater than 1 and $|\Delta|$ has a value less than 1 over the entire bandwidth.

The figure-of-merit (FOM) of the proposed LNA can be expressed by

$$K = \frac{1 - |S_{11}|^2 - |S_{21}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$
where \(|S_{21}|_{abs}\) and \(F\) are the absolute values of \(S_{21}\) and \(NF\), respectively. The LNA has a very good \(FOM\) equal to 38.89.

Layout of the proposed low-noise amplifier with its post-layout simulation results are shown in Fig. 19. It has been depicted from the results that post-layout NF is varying from 3.99 to 5.7 dB, whereas \(S_{21}\) is varying from 15.21 dB at 3.0 GHz to 16.98 dB at 9.46 GHz. The input reflection coefficient (\(S_{11}\)) remains less than \(-8.452\) dB, whereas output reflection coefficient (\(S_{22}\)) remains less than \(-10.13\) dB. Table II presents the state-of-art and performance comparison with the existing works. It is depicted that the bandwidth of the inductor noise-canceling LNA proposed in [18] is only 0.1–1.4 GHz. Further, LNA proposed in this work consumes less power as compared to the LNAs proposed in [7,15,18,20,23,25]. Also NF of the LNA proposed in [16] is far greater than NF of the proposed work, whereas it is comparable to the NF of LNAs proposed in [7,13,24]. The \(IIP3\) of the proposed LNA is low but is still acceptable and comparable with the LNA proposed in [16]. It highlights the fact that the proposed AI-based LNA exhibits high \(S_{21}\) while dissipating very less power.

### IV. CONCLUSION

This paper presents a CG LNA design using the \(g_{m}\)-boosting technique. The main contribution of this paper is its active inductor-based input matching technique for UWB LNA design utilizing only two inductors that will benefit in terms of reduced chip area. Proposed LNA consists of \(g_{m}\)-boosting common gate stage, gain stage, and output buffer stage. \(g_{m}\)-boosting technique has been used to obtain high gain and dissipate less power as it decouples the existing trade-off between NF and input impedance. An active inductor was implemented for input impedance matching, thereby reducing the chip area. Proposed 90 nm CMOS LNA was designed using Cadence software. Proposed LNA demonstrates a flat power gain of \(18 \pm 0.8\) dB, a minimum NF of \(3.36\) dB, and an input return loss less than \(-9.3\) dB across the entire bandwidth. Proposed LNA circuit design operates in the frequency range of 3.1–10.6 GHz and dissipates 10.4 mW from 1.0 V supply. This makes the proposed LNA circuit suitable for most of the UWB wireless applications.

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| Ref.  | [18] | [7]| [23]| [13]| [25]| [24]| [15]| [16]| [20]| TW |
|------|------|----|------|------|------|------|------|------|------|----|
| Year | 2018 | 2021 | 2018 | 2012 | 2020 | 2019 | 2016 | 2015 | 2018 | 2021 |
| Topology | Inductor less NC | CCG with current reuse | CS-ID + NC | CG | CS-CG NC | CS-CD current-reuse | $g_m$-boosted CG | CG | CS-ID with self-cascode current reused | CG-AI |
| Tech. (nm) | 180 | 45 | 180 | 180 | 180 | 180 | 90 | 90 | 90 | 90 |
| BW (GHz) | 0.1–1.4 | 26–34 | 3–12 | 2.0–14 | 3–10.6 | 2–11 | 1–103 | 3.1–10.6 | 3.1–10.6 | 3.1–10.6 |
| $V_{dd}$ (V) | 1.8 | 1.0 | 1.8 | 1.5 | 1 | 1.8 | 0.6 | 1 | 1 | 1 |
| $S_{21}$ (dB) | 16.1$^\text{max}$ | 13.1$^\text{max}$ | 19.24–20.24 | 9$^\text{avg}$ | 12.1–13.4 | 12.35 ± 0.85 | 6 | 20.17 ± 0.39 | 2010 ± 1.65 | 18.22$^\text{max}$ |
| $S_{11}$ (dB) | $<-10$ | $<-9.58$ | $<-10$ | $<-10$ | $<-10$ | $<-10$ | $<-10$ | $<-10^a$ | $<-10^a$ | $<-9$ |
| NF (dB) | 2.8–3.4 | 3.08$^\text{min}$ | 1.72–1.99 | 2.7–6.2 | 1.7–2.3 | 3.35 ± 0.8 | 4.1–4.7$^\text{min}$ | 1.11–1.41 | 1.2$^a$ | 3.36–4.68 |
| $IIP_1$ (dBm) | 13–18.9 | NA | 5.5 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| $IIP_3$ (dBm) | 24–40 | NA | NA | NA | NA | NA | NA | NA | NA | NA |
| Power (mW) | 19 | 16 | 23.23 | 9 | 11.56 | 9.52 | 10.9 | 4.33 | 11.52 | 10.4 |

FOM (GHz/mW):

\[
\text{FOM} = \frac{S_{21}(\text{dB})}{P_{\text{in}}^{0.6}} \quad \text{\text{FOM} =} \quad \frac{S_{21\text{max}}(\text{dB}) \times BW_{\text{in}}}{(F-1) \times P_{\text{in}}} \quad \text{\text{FOM} =} \quad \frac{S_{21\text{max}}(\text{dB})}{(F-1) \times P_{\text{in}}} \quad \text{\text{FOM} =} \quad \frac{S_{21\text{max}}(\text{dB}) \times BW_{\text{in}} \times IIP_3\text{max}}{(F-1) \times P_{\text{in}}^{0.6}}
\]

$^a$Simulation results; $^b$post-layout simulation results; CS, common source; ID, inductive degeneration; CG, common gate; NC, noise cancelling; CCG, complementary common gate.

$^a$NF$^\text{min}$; $^\text{avg}$average; $^\text{max}$maximum; $^\text{for}$ 3.1–9.7 GHz; $^\text{Excluding buffer}; ^\text{min}$minimum; $^\text{FOM in dB.}$
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