Energy-Efficient Deflection-based On-chip Networks: Topology, Routing, Flow Control

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Abstract

As the number of cores scales to tens and hundreds, the energy consumption of routers across various types of on-chip networks in chip multiprocessors (CMPs) increases significantly. A major source of this energy consumption comes from the input buffers inside Network-on-Chip (NoC) routers, which are traditionally designed to maximize performance. To mitigate this high energy cost, many works propose bufferless router designs that utilize deflection routing to resolve port contention. While this approach is able to maintain high performance relative to its buffered counterparts at low network traffic, the bufferless router design suffers performance degradation under high network load.

In order to maintain high performance and energy efficiency under both low and high network loads, this chapter discusses critical drawbacks of traditional bufferless designs and describes recent research works focusing on two major modifications to improve the overall performance of the traditional bufferless network-on-chip design. The first modification is a minimally-buffered design that introduces limited buffering inside critical parts of the on-chip network in order to reduce the number of deflections. The second modification is a hierarchical bufferless interconnect design that aims to further improve performance by limiting the number of hops each packet needs to travel while in the network. In both approaches, we discuss design tradeoffs and provide evaluation results based on common CMP configurations with various network topologies to show the effectiveness of each proposal.

Keywords: network-on-chip, deflection routing, topology, bufferless router, energy efficiency, high-performance computing, computer architecture, emerging technologies, latency, low-latency computing
1. Introduction

As commercial processors incorporate more cores, scalability and energy efficiency demand better interconnection substrates. Different interconnect designs such as a 2D mesh [1,17] or a flattened butterfly [18] have become increasingly popular as scalable, high-performance on-chip networks for chip multiprocessors (CMPs) as the number of core grows to hundreds. Unfortunately, these high-performance Network-on-Chip (NoC) designs are projected to consume significant amount of power. For example, 28% of the chip power is consumed by the NoC in the Intel Terascale 80-core chip [19], 36% in MIT RAW [20], and 36% in Intel 48-core SCC [21]. To reduce the overall power consumption of modern processors, NoC energy efficiency is a critically important design goal [2,4,22,25].

Previous on-chip interconnection network designs commonly assume that each router in the network needs to contain buffers to buffer the packets (or flits) transmitted within the network. Indeed, buffering within each router improves the bandwidth efficiency in the network because buffering reduces the number of dropped or “misrouted” packets [1], i.e. packets that are sent to a less desirable destination port. On the other hand, buffering has several disadvantages. First, buffers consume significant energy/power: dynamic energy when read/written and static energy even when they are not occupied. Second, having buffers increases the complexity of the network design because logic needs to be implemented to place packets into and out of buffers. Third, buffers can consume significant chip area: even with a small number (16) of total buffer entries per node where each entry can store 64 bytes of data, a network with 64 nodes requires 64KB of buffer storage. In fact, in the TRIPS prototype chip, input buffers of the routers were shown to occupy 75% of the total on-chip network area [26]. Energy consumption and hardware storage cost of buffers increases as future many-core chips incorporate more network nodes.

Mechanisms have been proposed to make conventional input-buffered NoC routers more energy-efficient (i.e., use less energy per unit of performance). For example, bypassing empty input buffers [27,28] reduces some dynamic buffer power, but static power remains. Such bypassing is also less effective when buffers are not frequently empty. Bufferless deflection routers [2] remove router input buffers completely (thereby eliminating their static and dynamic power) to reduce router power. In a conventional bufferless deflection network, flits (several of which make up one packet) are independently routed, unlike most buffered networks, where a packet is the smallest independently-routed unit of traffic. When two flits contend for a single router output, one must be deflected [29] to another output. Thus, a flit never requires a buffer in a router. By controlling which flits are deflected, a bufferless deflection router can ensure that all traffic is eventually delivered. Removing buffers yields simpler and more energy-efficient NoC designs: for example, CHIPPER [4] reduces average network power by 54.9% in a 64-node system compared to a conventional buffered router.

Unfortunately, at high network load, deflection routing reduces performance and efficiency. This is because deflections occur more frequently when many flits contend in the network. Each deflection sends a flit further from its destination, causing unnecessary link and router traversals. Relative to a buffered network, a bufferless network with a high deflection rate wastes energy, and suffers from worse congestion, because of these unproductive network hops. In contrast, a buffered router is able to hold flits (or packets) in its input buffers until the required output port is available, incurring no unnecessary hops. Thus, a buffered network can sustain higher performance at peak load [2], but at the cost of large buffers, which can consume significant power and die area.

The best interconnect design would obtain the energy efficiency of the bufferless approach with the high performance of the buffered approach. To obtain the best of both worlds, a router would contain only a small amount of buffering for flits that actually require it, and the network topology would allow flits to reach their destination using the fewest number of hops.

On top of the bufferless approach, to achieve scalability to many (tens, hundreds, or thousands) of cores, mesh or other higher-radix topologies are used. Both the Intel SCC [30] and Terascale [31] CMPs, and several other many-core CMPs (e.g., the MIT RAW [20] prototype, the UT-Austin TRIPS chip [32], several Tilera products [33,34]), and more recently, the Intel Skylake [35], Intel Cascade Lake [36], and Intel Ice Lake [37] server processors exchange packets on a mesh. A mesh topology has good scalability because there is no central structure which needs to scale (unlike a central bus or crossbar-based design), and bisection bandwidth increases as the network grows. However, routers in a 2D mesh can consume significant energy and die area due to overheads in buffering, in routing and flow control, and in the switching elements (crossbars) that connect multiple inputs with multiple outputs.

Mainstream commercial CMPs today most commonly use ring-based interconnects. Rings are a well-known network topology [1], and the idea behind a ring topol-
ogy is very simple: all routers (also called “ring stops”) are connected by a loop that carries network traffic. At each router, new traffic can be injected into the ring, and traffic in the ring can be removed from the ring when it reaches its destination. When traffic is traveling on the ring, it continues uninterrupted until it reaches its destination. A ring router thus needs no in-ring buffering or flow control because it prioritizes on-ring traffic. In addition, the router’s datapath is very simple compared to a mesh router, because the router has fewer inputs and requires no large, power-inefficient crossbars; typically it consists only of several MUXes to allow traffic to enter and leave, and one pipeline register. Its latency is typically only one clock cycle, because no routing decisions or output port allocations are necessary (other than removing traffic from the ring when it arrives). Because of these advantages, several prototype and commercial multicore processors have utilized ring interconnects. Examples of these processors include the Intel Larrabee [38], IBM Cell [39], Intel Sandy Bridge [40], Intel Skylake [35], Intel Coffee Lake [41] and more recently, the Intel Ice Lake [42] and the three interwiring rings in the NVIDIA DGX-1 NVLink [42].

Past work has shown that rings are competitive with meshes up to tens of nodes [43,45]. Unfortunately, rings suffer from a fundamental scaling problem because a ring’s bisection bandwidth does not scale with the number of nodes in the network. Building more rings, or a wider ring, serves as a stopgap measure but increases the cost of every router on the ring in proportion to the bandwidth increase. As commercial CMPs incorporate more cores, a new network design will be needed that balances the simplicity and low overhead of rings with the scalability of more complex topologies.

A hybrid design is possible. In this chapter, we introduce an approach to construct rings in a hierarchy such that groups of nodes share a simple ring interconnect, and these “local” rings are joined by one or more “global” rings. Figure 1 shows an example of such a hierarchical ring design [23,24,44,49,51]. Past works [44,49,49,51] propose hierarchical rings as a scalable alternative to single ring and mesh networks. These proposals join rings with bridge routers, which reside on multiple rings and transfer traffic between rings. This design was shown to yield good performance and scalability [46]. A state-of-the-art design [46] requires flow control and buffering at every node router (ring stop), because a ring transfer can cause one ring to back up and stall when another ring is congested. While this previously proposed hierarchical ring is much more scalable than a single ring [46], the reintroduction of in-ring buffering and flow control nullifies one of the primary advantages of using ring networks in the first place (i.e., the lack of buffering and buffered flow control within each ring).

![Figure 1: A traditional hierarchical ring design [46,50] allows “local rings” with simple node routers to scale by connecting to a “global ring” via bridge routers. Reproduced from [52].](image)

To combine the concept of a minimally-buffered router with a hierarchical ring, previous work allows a bridge router with a full buffer to deflect packets, called HiRD (i.e., Hierarchical Rings with Deflection [23,24,52]). Rather than requiring buffering and flow control in the ring, packets simply cycle through the network and try again. While deflection-based, bufferless networks have been proposed and evaluated in the past [2–4,6,19,23,24,27,53,55], this minimally-buffered hierarchical ring approach is effectively an elegant hybridization of bufferless (rings) and buffered (bridge routers) styles. To prevent packets from potentially deflecting around a ring arbitrarily many times (i.e., to prevent livelock), we introduce two new mechanisms, the injection guarantee and the transfer guarantee, that ensure packet delivery even for adversarial/pathological conditions (as discussed in [23,24,52] and evaluated with worst-case traffic in Section 5.10). This simple hierarchical ring design provides a more scalable network architecture while retaining the key simplicities of ring networks (no buffering or flow control within each ring). Section 5.10 show in our evaluations that HiRD provides better performance, lower power, and better energy efficiency with respect to various buffered hierarchical ring designs [46] as well as other NoC designs.

2. Bufferless Routing

2.1. Why Bufferless? (and When?)

Bufferless¹ NoC design has recently been evaluated as an alternative to traditional virtual-channel buffered

¹More precisely, a “bufferless” NoC has no in-router (e.g., virtual channel) buffers, only pipeline latches. Baseline bufferless designs, such as BLESS, still require reassembly buffers and injection queues. Another subsequent work CHIPPER eliminates these buffers as well.
routers [2,4,6,19,23,24,27,53,65]. It is appealing mainly for two reasons: reduced power consumption, and simplicity in design. As core count in modern CMPs continues to increase, the interconnect becomes a more significant component of system power consumption. Several prototype manycore systems point toward this trend: in MIT RAW, interconnect consumes 40% of system power; in the Intel Terascale chip, 30%. Buffers consume a significant portion of this power. A recent work [2], described in Section 2.2, reduces network energy by 40% by eliminating buffers. Furthermore, the complexity reduction of the design at the high level could be substantial: a bufferless router requires only pipeline registers, a crossbar, and arbitration logic. This can translate into reduced system design and verification cost.

Bufferless NoCs present a tradeoff: by eliminating buffers, the peak network throughput is reduced, potentially degrading performance. However, network power is often significantly reduced. For this tradeoff to be effective, the power reduction must outweigh the slowdown’s effect on total energy. Moscibroda and Mutlu [2] reported minimal performance reduction with bufferless when NoC is lightly loaded, which constitutes many of the applications they evaluated. Bufferless NoC design thus represents a compelling design point for many systems with low-to-medium network load, eliminating unnecessary capacity for significant savings.

2.2. BLESS: Baseline Bufferless Deflection Routing

Here we briefly introduce bufferless deflection routing in the context of BLESS [2]. BLESS routes flits, the minimal routable units of packets, between nodes in a mesh interconnect. Each flit in a packet contains header bits and can travel independently, although in the best case, all of a packet’s flits remain contiguous in the network. Each node contains an injection buffer and a reassembly buffer; there are no buffers within the network, aside from the router pipeline itself. Every cycle, flits that arrive at the input ports contend for the output ports. When two flits contend for one output port, BLESS avoids the need to buffer by misrouting one flit to another port. The flits continue through the network until ejected at their destinations, possibly out of order, where they are reassembled into packets and delivered. Deflection routing is not new: it was first proposed in [29], and is used in optical networks because of the cost of optical buffering [60]. It works because a router has as many output links as input links (in a 2D mesh, 4 for neighbors and 1 for local access). Thus, the flits that arrive in a given cycle can always leave exactly \( N \) cycles later, for an \( N \)-stage router pipeline. If all flits request unique output links, then a deflection router can grant every flit’s requested output. However, if more than one flit contends for the same output, all but one must be deflected to another output that is free.

2.2.1. Livelock Freedom

Whenever a flit is deflected, it moves further from its destination. If a flit is deflected continually, it may never reach its destination. Thus, a routing algorithm must explicitly avoid livelock. It is possible to probabilistically bound network latency in a deflection network [66, 67]. However, a deterministic bound is more desirable. BLESS [2] uses an Oldest-First prioritization rule to give a deterministic bound on network latency. Flits arbitrate based on packet timestamps. Prioritizing the oldest traffic creates a consistent total order and allows this traffic to make forward progress. Once the oldest packet arrives, another packet becomes oldest. Thus livelock freedom is guaranteed inductively. However, this age-based priority mechanism is expensive [27, 55] both in header information and in arbitration critical path. Alternatively, some bufferless routing proposals do not provide or explicitly show deterministic livelock-freedom guarantees [55,57]. This can lead to faster arbitration if it allows for simpler priority schemes. However, a provable guarantee of livelock freedom is necessary to show system correctness in all cases. CHIPPER [4], described in Section 2.3, provides strong livelock freedom guarantees in a bufferless design.

2.2.2. Injection

BLESS guarantees that all flits entering a router can leave it, because there are at least as many output links as input links. However, this does not guarantee that new traffic from the local node (e.g., core or shared cache) can always enter the network. A BLESS router can inject a flit whenever an input link is empty in a given cycle. In other words, BLESS requires a “free slot” in the network in order to insert new traffic. When a flit is injected, it contends for output ports with the other flits in that cycle. Note that the injection decision is purely local: that is, a router can decide whether to inject without coordinating with other routers.

2.2.3. Ejection and Packet Reassembly

A BLESS router can eject one flit per cycle when that flit reaches its destination. In any bufferless deflection network, flits can arrive in random order; therefore, a packet reassembly buffer is necessary. Once all flits in a packet arrive, the packet can be delivered to the local node. Importantly, this buffer must be managed so that it does not overflow, and in such a way that maintains
correctness. BLESS [2] does not consider this problem in detail. Instead, it assumes an infinite reassembly buffer, and reports maximum occupancies for the evaluated workloads.

2.3. Deflection Routing Complexities

While bufferless deflection routing is conceptually and algorithmically simple, a straightforward hardware implementation leads to numerous complexities. In particular, two types of problem plague baseline bufferless deflection routing: high hardware cost, and unaddressed correctness issues. The hardware cost of a direct implementation of bufferless deflection routing is nontrivial, due to expensive control logic. Just as importantly, correctness issues arise in the reassembly buffers when they have practical (non-worst-case) sizes, and this fundamental problem is unaddressed by current work. Here, we describe the major difficulties: output port allocation, expensive priority arbitration, and reassembly buffer cost and correctness. Prior work cites these weaknesses [2].

To address these drawbacks, CHIPPER [4] proposes a new bufferless router architecture, CHIPPER, that solves these problems through three key insights. First, CHIPPER eliminates the expensive port allocator and the crossbar, and replace both with a permutation network; deflection routing maps naturally to this arrangement, reducing critical path length and power/area cost. Second, CHIPPER provides a strong livelock guarantee through an implicit token passing scheme, eliminating the cost of a traditional priority scheme. Finally, CHIPPER proposes a simple flow control mechanism for correctness with reasonable reassembly buffer sizes, and propose using cache miss buffers (MSHRs [68–70]) as reassembly buffers. CHIPPER [4] shows that at low-to-medium load, the reduced-complexity CHIPPER design performs competitively to a traditional buffered router (in terms of application performance and operational frequency) with significantly reduced network power, and very close to baseline bufferless (BLESS [2]) with a reduced critical path.

For low-to-medium network load, CHIPPER delivers performance close to a conventional buffered network as shown in Figure 2, because the deflection rate is low: thus, most flits take productive network hops in every cycle, just as in the buffered network. In addition, the bufferless router has significantly reduced power (hence improved energy efficiency), because the buffers in a conventional router consume significant power. However, as network load increases, the deflection rate in a bufferless deflection network also rises, because flits contend with each other more frequently. With a higher deflection rate, the dynamic power of a bufferless deflection network rises more quickly with load than dynamic power in an equivalent buffered network, because each deflection incurs some extra work. Hence, bufferless deflection networks lose their energy efficiency advantage at high load. Just as important, the high deflection rate causes each flit to take a longer path to its destination, and this increased latency reduces the network throughput and system performance.

Overall, neither design obtains both good performance and good energy efficiency at all loads. If the system usually experiences low-to-medium network load, then the bufferless design provides adequate performance with low power (hence high energy efficiency). But, if we use a conventional buffered design to obtain high performance, then energy efficiency is poor in the low-load case, and even buffer bypassing does not remove this overhead because buffers consume static power regardless of use. Finally, simply switching between these two extremes at a per-router granularity, as previously proposed [71], does not address the fundamental inefficiencies in the bufferless routing mode, but rather, uses input buffers for all incoming flits at a router when load is too high for the bufferless mode (hence retains the energy-inefficiency of buffer operation at high load).

This chapter (in Section 4) describes MinBD [3,72,73], a minimally-buffered deflection router that combines bufferless and buffered routing in a new way to reduce this overhead.

Figure 2: System performance and energy efficiency (performance per watt) of bufferless deflection routing, relative to conventional input-buffered routing (4 VCs, 4 flits/VC) that employs buffer bypassing, in a 4x4 2D mesh. Injection rate (X axis) for each workload is measured in the baseline buffered network. Reproduced from [3].
3. Scalability in Mesh-Based Interconnects

Despite the simplicity advantage of a ring-based network, rings have a fundamental scalability limit: as compared to a mesh, a ring stops scaling at fewer nodes because its bisection bandwidth is constant (proportional only to link width) and the average hop count (which translates to latency for a packet) increases linearly with the number of nodes. (Intuitively, a packet visits half the network on its way to the destination, in the worst case, and a quarter in the average case, for a bidirectional ring.) In contrast, a mesh has bisection bandwidth proportional to one dimension of the layout (e.g., the square-root of the node count for a 2D mesh) and also has an average hop count that scales only with one dimension. The higher radix, and thus higher connectivity, of the mesh allows for more path diversity and lower hop counts which increases performance.

To demonstrate this problem quantitatively, Figure 3 shows application performance averaged over a representative set of network-intensive workloads on (i) a single ring network and (ii) a conventional 2D-mesh buffered interconnect. As the plot shows, although the single ring is able to match the mesh’s performance at the 16-node design point, it degrades when node count increases to 64. Note that in this case, the ring’s bisection bandwidth is kept equivalent to the mesh, so the performance degradation is solely due to higher hop count; considerations of practical ring width might reduce performance further.

Figure 3: Performance as mesh and ring networks to 64 nodes.

3.1. Simplicity in Ring-Based Interconnects

Ring interconnects are attractive in current small-to-medium-scale commercial CMPs because ring routers (ring stops) are simple, which leads to smaller die area and energy overhead. In its simplest form, a ring router needs to perform only two functions: injecting new traffic into the ring, and removing traffic from the ring when it has arrived at its destination. Figure 4(a) depicts the router datapath and control logic (at a high level) necessary to implement this functionality. For every incoming flit (unit of data transfer as wide as one link), the router only needs to determine whether the flit stays on the ring or exits at this node. Then, if a flit is waiting to inject, the router checks whether a flit is already present on the ring in this timeslot, and if not, injects the new flit using the in-ring MUX.

Rings achieve very good energy efficiency at low-to-medium core counts [43]. However, the simplicity advantage of a ring-based network, rings have a fundamental scalability limit: a ring stops scaling at fewer nodes because its bisection bandwidth is constant (proportional only to link width) and the average hop count (which translates to latency for a packet) increases linearly with the number of nodes. (In the worst case for a bidirectional ring, a packet visits half the network on its way to its destination, and a quarter on average.)

3.2. Hierarchical Rings for Scalability

Fortunately, past work has observed that hierarchy allows for additional scalability in many interconnects: ring-based designs [46–50], with hierarchical buses [74], and with hierarchical meshes [75]. The state-of-the-art hierarchical ring design [46] in particular reports promising results by combining local rings with one or more levels of higher-level rings, which we refer to as global rings, that connect lower level rings together. Rings of different levels are joined by Inter-Ring Interfaces (IRIs), which we call “bridge routers” in this work. Figure 4(b) graphically depicts the details of one bridge router in the previously proposed buffered hierarchical ring network.

Unfortunately, connecting multiple rings via bridge routers introduces a new problem. Recall that injecting new traffic into a ring requires an open slot in that ring. If the ring is completely full with flits (i.e., a router attempting to inject a new flit must instead pass through a flit already on the ring every cycle), then no new traffic will be injected. But, a bridge router must inject transferring flits into those flits’ destination ring in exactly the same manner as if they were newly entering the network. If the ring on one end of the bridge router is completely full (cannot accept any new flits), and the transfer FIFO into that ring is also full, then any other flit requiring a transfer must block its current ring. In other words, ring transfers create new dependences between adjacent rings, which creates the need for end-to-end flow control. This flow control forces every node router (ring stop) to have an in-ring FIFO and flow control logic, which increases energy and die area overhead and significantly reduces the appeal of a simple ring-based design. Table 1 compares the power consumption for a previously proposed hierarchical ring design (Buffered HRing) and a bufferless hierarchical ring design on a system with 16 nodes using DSENT 0.91 [76] and a 45nm technology commercial design library. In the examined idealized bufferless design, each ring has no in-ring buffers, but
there are buffers between the hierarchy levels. When a packet needs a buffer that is full, it gets deflected and circles its local ring to try again. Clearly, eliminating in-ring buffers in a hierarchical ring network can reduce power and area significantly.

| Metric               | Buffered HRing | Bufferless HRing |
|----------------------|----------------|------------------|
| Normalized power     | 1              | 0.355            |
| Normalized area      | 1              | 0.495            |

Table 1: Power and area comparison (16-node network). Reproduced from [52].

However, simply removing in-ring buffers can introduce livelock, as a deflected packet may circle its local ring indefnitely. Our goal in this work is to introduce a hierarchical ring design that maintains simplicity and low cost, while ensuring livelock and deadlock freedom for packets.

4. MinBD: Minimally-Buffered Deflection Router Design

The MinBD (minimally-buffered deflection) router [3, 72, 73] is a new router design that combines bufferless deflection routing with a small buffer, which we call the side buffer. We start by outlining the key principles we follow to reduce deflection caused inefficiency by using buffering:

1. When a flit would be deflected by a router, it is often better to buffer the flit and arbitrate again in a later cycle. Some buffering can avoid many deflections.
2. However, buffering every flit leads to unnecessary power overhead and buffer requirements, because many flits will be routed productively on the first try. The router should buffer a flit only if necessary.
3. Finally, when a flit arrives at its destination, it should be removed from the network (ejected) quickly, so that it does not continue to contend with other flits.

Basic High-Level Operation. The MinBD router does not use input buffers, unlike conventional buffered routers. Instead, a flit that arrives at the router proceeds directly to the routing and arbitration logic. This logic performs deflection routing, so that when two flits contend for an output port, one of the flits is sent to another output instead. However, unlike a bufferless deflection router, the MinBD router can also buffer up to one flit per cycle in a single FIFO-queue side buffer. The router examines all flits at the output of the deflection routing logic, and if any are deflected, one of the deflected flits is removed from the router pipeline and buffered (as long as the buffer is not full). From the side buffer, flits are reinjected into the network by the router, in the same way that new traffic is injected. Thus, some flits that would have been deflected in a bufferless deflection router are removed from the network temporarily into this side buffer, and given a second chance to arbitrate for a productive router output when re-injected. This reduces the network’s deflection rate (hence improves performance and energy efficiency) while buffering only a fraction of traffic.

We will describe the operation of the MinBD router in stages. First, Section 4.1 describes the deflection routing logic that computes an initial routing decision for the flits that arrive in every cycle. Then, Section 4.2 describes how the router chooses to buffer some (but not all) flits in the side buffer. Section 4.3 describes how buffered flits and newly-generated flits are injected into the network, and how a flit that arrives at its destination is ejected. Finally, Section 4.4 discusses correctness issues, and describes how MinBD ensures that all flits are eventually delivered.

4.1. Deflection Routing

The MinBD router pipeline is shown in Figure 5. Flits travel through the pipeline from the inputs (on the left) to outputs (on the right). We first discuss the deflection routing logic, located in the Permute stage on the right. This
logic implements deflection routing: it sends each input flit to its preferred output when possible, deflecting to another output otherwise. MinBD uses the deflection logic organization first proposed in CHIPPER [4]. The permutation network in the Permute stage consists of two-input blocks arranged into two stages of two blocks each. This arrangement can send a flit on any input to any output. (Note that it cannot perform all possible permutations of inputs to outputs, but as we will see, it is sufficient for correct operation that at least one flit obtains its preferred output.) In each two-input block, arbitration logic determines which flit has a higher priority, and sends that flit in the direction of its preferred output. The other flit at the two-input block, if any, must take the block’s other output. By combining two stages of this arbitration and routing, deflection arises as a distributed decision: a flit might be deflected in the first stage, or the second stage. Restricting the arbitration and routing to two-flit subproblems reduces complexity and allows for a shorter critical path, as demonstrated in CHIPPER [4]. In order to ensure correct operation, the router must arbitrate between flits so that every flit is eventually delivered, despite deflections. We adapt a modified version of the Golden Packet priority scheme [4], which solves this livelock-freedom problem. This priority scheme is summarized in RuleSet 1. The basic idea of the Golden Packet priority scheme is that at any given time, at most one packet in the system is golden. The flits of this golden packet, called “golden flits,” are prioritized above all other flits in the system and contention between golden flits is resolved by the flit sequence number. While prioritized, golden flits are never deflected by non-golden flits. The packet is prioritized for a period long enough to guarantee its delivery. Finally, this “golden” status is assigned to one globally-unique packet ID (e.g., source node address concatenated with a request ID), and this assignment rotates through all possible packet IDs such that any packet that is “stuck” will eventually become golden. In this way, all packets will eventually be delivered, and the network is livelock-free. (See CHIPPER [4] for the precise way in which the Golden Packet is determined; we use the same rotation schedule.) However, although Golden Packet arbitration provides correctness, a performance issue occurs with this priority scheme. Consider that most flits are not golden: the elevated priority status provides worst-case correctness, but does not impact common-case performance (prior work reported over 99% of flits are delivered without becoming golden [4]). However, when no flits are golden and ties are broken randomly, the arbitration decisions in the two permutation network stages are not coordinated. Hence, a flit might win arbitration in the first stage, and cause another flit to be deflected, but then lose arbitration in the second stage, and also be deflected. Thus, unnecessary deflections occur when the two permutation network stages are uncoordinated.

In order to resolve this performance issue, we observe that it is enough to ensure that in every router, at least one flit is prioritized above the others in every cycle. In this way, at least one flit will certainly not be deflected. To ensure this when no golden flits are present, we add a “silver” priority level, which wins arbitration over common-case flits but loses to the golden flits. One silver flit is designated randomly among the set of flits that enter a router at every cycle (this designation is local to the router, and not propagated to other routers). This modification helps to reduce deflection rate. Prioritizing a silver flit at every router does not impact correctness, because it does not deflect a golden flit if one is present, but it ensures that at least one flit will consistently win arbitration at both stages. Hence, deflection rate is reduced, improving performance.

4.2. Using a Small Buffer to Reduce Deflections

The key problem addressed by MinBD is deflection inefficiency at high load. In other words, when the network
is highly utilized, contention between flits occurs often. This results in many deflected flits. We observe that adding a small buffer to a deflection router can reduce deflection rate, because the router can choose to buffer rather than deflect a flit when its output port is taken by another flit. Then, at a later time when output ports may be available, the buffered flit can re-try arbitration.

Thus, to reduce deflection rate, MinBD adds a “side buffer” that buffers only some flits that otherwise would be deflected. This buffer is shown in Figure 5 above the permutation network. In order to make use of this buffer, a “buffer eject” block is placed in the pipeline after the permutation network. At this point, the arbitration and routing logic has determined which flits to deflect. The buffer eject block recognizes flits that have been deflected, and picks up to one such deflected flit per cycle. It removes a deflected flit from the router pipeline, and places this flit in the side buffer, as long as the side buffer is not full. (If the side buffer is full, no flits are removed from the pipeline into the buffer until space is created.)

This flit is chosen randomly among deflected flits (except that a golden flit is never chosen: see Section 4.4). In this way, some deflections are avoided. The flits placed in the buffer will later be re-injected into the pipeline, and will re-try arbitration at that time. This re-injection occurs in the same way that new traffic is injected into the network, which we discuss below.

4.3 Injection and Ejection

So far, we have considered the flow of flits from router input ports (i.e., arriving from neighbor routers) to router output ports (i.e., to other neighbor routers). A flit must enter and leave the network at some point. To allow traffic to enter (inject) and leave (eject), the MinBD router contains inject and eject blocks in its first pipeline stage (see Figure 5). When a set of flits arrive on router inputs, these flits first pass through the ejection logic. This logic examines the destination of each flit, and if a flit is addressed to the local router, it is removed from the router pipeline and sent to the local network node.

If more than one locally-addressed flit is present, the ejector picks one, according to the same priority scheme used by routing arbitration.

However, ejecting a single flit per cycle can produce a bottleneck and cause unnecessary deflections for flits that could not be ejected. In the workloads we evaluate, at least one flit is eligible to eject 42.8% of the time. Of those cycles, 20.4% of the time, at least two flits are eligible to eject. Hence, in 8.5% of all cycles, a locally-addressed flit would be deflected rather than ejected if only one flit could be ejected per cycle. To avoid this significant deflection-rate penalty, we double the ejection bandwidth. To implement this, a MinBD router contains two ejector blocks. Each of these blocks is identical, and can eject up to one flit per cycle. Duplicating the ejection logic allows two flits to leave the network per cycle at every node. After locally-addressed flits are removed from the pipeline, new flits are allowed to enter. There are two injector blocks in the router pipeline shown in Figure 5: (i) re-injection of flits from the side buffer, and (ii) injection of new flits from the local node. (The “Redirection” block prior to the injector blocks will be discussed in the next section.) Each block operates in the same way. A flit can be injected into the router pipeline whenever one of the four inputs does not have a flit present in a given cycle, i.e., whenever there is an “empty slot” in the network. Each injection block pulls up to one flit per cycle from an injection queue (the side buffer, or the local node’s injection queue), and places a new flit in the pipeline when a slot is available. Flits from the side buffer are re-injected before new traffic is injected into the network. However, note that there is no guarantee that a free slot will be available for an injection in any given cycle. We now address this starvation problem for side buffer re-injection.

4.4 Ensuring Side Buffered Flits Make Progress

When a flit enters the side buffer, it leaves the router pipeline, and must later be re-injected. As we described above, flit re-injection must wait for an empty slot on an input link. It is possible that such a slot will not appear for a long time. In this case, the flits in the side buffer are delayed unfairly while other flits make forward progress.

To avoid this situation, we implement buffer redirection. The key idea of buffer redirection is that when this side buffer starvation problem is detected, one flit from a randomly-chosen router input is forced to enter the side buffer. Simultaneously, the flit at the head of the side buffer is allowed to inject into the slot created by the forced flit buffering. In other words, one router input is “redirected” into the FIFO buffer for one cycle, in order to allow the buffer to make forward progress. This redirection is enabled for one cycle whenever the side buffer injection is starved (i.e., has a flit to inject, but no free slot allows the injection) for more than some threshold \( C_{\text{threshold}} \) cycles (in our evaluations, \( C_{\text{threshold}} = 2 \)). Finally, note that if a golden flit is present, it is never

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2 Note that flits are reassembled into packets after ejection. To implement this reassembly, we use the Retransmit-Once scheme, as used by CHIPPER [1], which uses MSHRs (Miss-Status Handling Registers [2]), or existing buffers in the cache system to reassemble packets in place.
redirected to the buffer, because this would break the delivery guarantee.

4.5. Liveloop and Deadlock-free Operation

MinBD provides liveloop-free delivery of flits using Golden Packet and buffer redirection. If no flit is ever buffered, then Golden Packet\footnote{All operations in the network happen in a flit level similar to previous works \cite{4,17,65,75}.} ensures liveloop freedom (the “silver flit” priority never deflects any golden flit, hence does not break the guarantee). Now, we argue that adding side buffers does not cause liveloop. First, the buffering logic never places a golden flit in the side buffer. However, a flit could enter a buffer and then become golden while waiting. Redirection ensures correctness in this case: it provides an upper bound on residence time in a buffer (because the flit at the head of the buffer will leave after a certain threshold time in the worst case). If a flit in a buffer becomes golden, it only needs to remain golden long enough to leave the buffer in the worst case, then progress to its destination. We choose the threshold parameter ($C_{\text{threshold}}$) and golden epoch length so that this is always possible. More details can be found in our extended technical report \cite{22}.

MinBD achieves deadlock-free operation by using Retransmit-Once\cite{4}, which ensures that every node always consumes flits delivered to it by dropping flits when no reassembly/request buffer is available. This avoids packet reassembly deadlock (as described in \cite{4}), as well as protocol level deadlock, because message-class dependencies \cite{78} no longer exist.

5. HiRD: Simple Hierarchical Rings with Deflection

With the design of a minimally-buffered deflection router, minBD \cite{3,72,73}, we now describe how a similar concept can be integrated to a deflection-based hierarchical ring interconnect called HiRD \cite{23,24} in order to further improve performance, energy efficiency and scalability of NoCs. HiRD is built on several basic operation principles:

1. Every node (e.g., CPU, cache slice, or memory controller) resides on one local ring, and connects to one node router on that ring.
2. Node routers operate exactly like routers (ring stops) in a single-ring interconnect: locally destined flits are removed from the ring, other flits are passed through, and new flits can inject whenever there is a free slot (no flit present in a given cycle). There is no buffering or flow control within any local ring; flits are buffered only in ring pipeline registers. Node routers have a single-cycle latency.
3. Local rings are connected to one or more levels of global rings to form a tree hierarchy.
4. Rings are joined via bridge routers. A bridge router has a node-router-like interface on each of the two rings it connects, and has a set of transfer FIFOs (one in each direction) between the rings.
5. Bridge routers consume flits that require a transfer whenever the respective transfer FIFO has available space. The head flit in a transfer FIFO can inject into its new ring whenever there is a free slot (exactly as with new flit injections). When a flit requires a transfer but the respective transfer FIFO is full, the flit remains in its current ring. It will circle the ring and try again next time it encounters the correct bridge router (this is a deflection).

By using deflections rather than buffering and blocking flow control to manage ring transfers, HiRD retains node router simplicity, unlike past hierarchical ring network designs. This change comes at the cost of potential liveloop (if flits are forced to deflect forever). We introduce two mechanisms to provide a deterministic guarantee of liveloop-free operation in \cite{23,24}.

While deflection-based bufferless routing has been previously proposed and evaluated for a variety of off-chip and on-chip interconnection networks (e.g., \cite{24,8,9,29,65}), deflections are trivially implementable in a ring: if deflection occurs, the flit continues circulating in the ring. Contrast this to past deflection-based schemes that operated on mesh networks where multiple incoming flits may need to be deflected among a multitude of possible out-bound ports, leading to much more circuit complexity in the router microarchitecture, as shown by \cite{4,27,55}. Our application of deflection to rings leads to a simple and elegant embodiment of bufferless routing.

5.1. Node Router Operation

At each node on a local ring, we place a single node router, shown in Figure\cite{6}. A node router is very simple: it passes through circulating traffic, allows new traffic to enter the ring through a MUX, and allows traffic to leave the ring when it arrives at its destination. Each router contains one pipeline register for the router stage, and one pipeline register for link traversal, so the router latency is exactly one cycle and the per-hop latency is two cycles. Such a design is very common in ring-based and ring-like designs (e.g., \cite{29}).
As flits enter the router on the ring, they first travel to the ejector. Because we use bidirectional rings, each node router has two ejectors, one per direction. Note that the flits constituting a packet may arrive out-of-order and at widely separated times. Re-assembly into packets is thus necessary. Packets are re-assembled and reassembly buffers are managed using the Retransmit-Once scheme, borrowed from the CHIPPER bufferless router design. With this scheme, receivers reassemble packets in-place in MSHRs (Miss-Status Handling Registers), eliminating the need for separate reassembly buffers. The key idea in Retransmit-Once is to avoid ejection backpressure-induced deadlocks by ensuring that all arriving flits are consumed immediately at their receiver nodes. When a flit from a new packet arrives, it allocates a new reassembly buffer slot if available. If no slot is available, the receiver drops the flit and sets a bit in a retransmit queue which corresponds to the sender and transaction ID of the dropped flit. Eventually, when a buffer slot becomes available at the receiver, the receiver reserves the slot for a sender/transaction ID in its retransmit queue and requests a retransmit from the sender. Thus, all traffic arriving at a node is consumed (or dropped) immediately, so ejection never places back-pressure on the ring. Retransmit-Once hence avoids protocol-level deadlock. Furthermore, it ensures that a ring full of flits always drains, thus ensuring forward progress (as we will describe more fully in §5.3). It also allows for a flit to be egressed from the ring, and will eventually come back to the bridge router, at which point there may be an open slot available in the transfer FIFO. This is analogous to a deflection in hot-potato routing, also known as deflection routing, and has been used in recent on-chip mesh interconnect designs to resolve contention. Note that to ensure that flits are eventually delivered, despite any deflections that may occur, we introduce two guarantee mechanisms in §5.2. Finally, note that deflections may cause flits to arrive out-of-order (this is fundamental to any non-minimal adaptively-routed network). Because we use Retransmit-Once, packet reassembly works despite out-of-order arrival.

The bridge router uses crossbars to allow a flit ejecting from either ring direction in a bidirectional ring to enqueue for injection in either direction in the adjoining ring. When a flit transfers, it picks the ring direction that gives a shorter distance, as in a node router. However, these crossbars actually allow for a more general case: the bridge router can actually join several rings together for simplicity, we assume that up to two ejected flits can be accepted by the processor or reassembly buffers in a single cycle. For a fair comparison, we also implement two-flit-per-cycle ejection in our baselines.
by using larger crossbars. For our network topology, we use hierarchical rings. We use wider global rings than local rings (analogous to a fat tree [53]) for performance reasons. These wider rings perform logically as separate rings as wide as one flit. Although not shown in the figure for simplicity, the bridge router in such a case uses a larger crossbar and has one ring interface (including transfer FIFO) per ring-lane in the wide global ring. The bridge router then load-balances flits between rings when multiple lanes are available. (The crossbar and transfer FIFOs are fully modeled in our evaluations.)

When building a two-level design, there are many different arrangements of global rings and bridge routers that can efficiently link the local rings together. Figure 8a shows three designs denoted by the number of bridge routers in total: 4-bridge, 8-bridge, and 16-bridge. We assume an 8-bridge design for the remainder of this paper. Also, note that the hierarchical structure that we propose can be extended to more than two levels. We use a 3-level hierarchy, illustrated in Figure 8b to build a 64-node network.

Finally, in order to address a potential deadlock case (which will be explained more in [23, 24, 52]), bridge routers implement a special Swap Rule. The Swap Rule states that when the flit that just arrived on each ring requires a transfer to the other ring, the flits can be swapped, bypassing the transfer FIFOs altogether. This requires a bypass datapath (which is fully modeled in our hardware evaluations). It ensures correct operation in the case when transfer FIFOs in both directions are full. Only one swap needs to occur in any given cycle, even when the bridge router connects to a wide global ring. Note that because the swap rule requires this bypass path, the behavior is always active (it would be more difficult to definitively identify a deadlock and enable the behavior only in that special case). The Swap Rule may cause flits to arrive out-of-order when some are bypassed in this way, but the network already delivers flits out-of-order, so correctness is not compromised.

5.3. Routing

Finally, we briefly address routing. Because a hierarchical ring design is fundamentally a tree, routing is very simple: when a flit is destined for a node in another part of the hierarchy, it first travels up the tree (to more global levels) until it reaches a common ancestor of its source and its destination, and then it travels down the tree to its destination. Concretely, each node’s address can be written as a series of parts, or digits, corresponding to each level of the hierarchy (these trivially could be bitfields in a node ID). A ring can be identified by the common prefix of all routers on that ring; the root global ring has a null (empty) prefix, and local rings have prefixes consisting of all digits but the last one. If a flit’s destination does not match the prefix of the ring it is on, it takes any bridge router to a more global ring. If a flit’s destination does match the prefix of the ring it is on (meaning that it is traveling down to more local levels), it takes any bridge router which connects to the next level, until it finally reaches the local ring of its destination and ejects at the node with a full address match.

5.4. Guaranteed Delivery: Correctness in Hierarchical Ring Interconnects

In order for the system to operate correctly, the interconnect must guarantee that every flit is eventually delivered to its destination. HiRD ensures correct operation through two mechanisms that provide two guarantees: the injection guarantee and the transfer guarantee. The injection guarantee ensures that any flit waiting to inject into a ring will eventually be able to enter that ring. The transfer guarantee ensures that any flit waiting to enter a bridge router’s transfer queue will eventually be granted a slot in that queue.
To understand the need for each guarantee, let us consider an example, shown in Figure 9. A flit is enqueued for network injection at node N1 on the leftmost local ring. This flit is destined for node N2 on the rightmost local ring; hence, it must traverse the leftmost local ring, then the global ring in the center of the figure, followed by the rightmost local ring. The flit transfers rings twice, at the two bridge routers B1 and B2 shown in the figure. The figure also indicates the six points (labeled as 1 to 6) at which the flit moves from a queue to a ring or vice-versa: the flit first enters N1’s injection queue, transfers to the leftmost local ring 1, the bridge router B1 2, the global ring 3, the bridge router B2 4, the rightmost local ring 5, and finally the destination node N2 6.

Figure 9: The need for the injection and transfer guarantees: contention experienced by a flit during its journey. Reproduced from 52.

In the worst case, when the network is heavily contended, the flit could wait for an unbounded amount of time at 1 to 5. First, recall that to enter any ring, a flit must wait for an empty slot on that ring (because the traffic on the ring continues along the ring once it has entered, and thus has higher priority than any new traffic). Because of this, the flit traveling from node N1 to N2 could wait for an arbitrarily long time at 1, 3, and 5 if no other mechanism intercedes. This first problem is one of injection starvation, and we address it with the injection guarantee mechanism described below. Second, recall that a flit that needs to transfer from one ring to another via a bridge router enters that bridge router’s queue, but if the bridge router’s queue is full, then the transferring flit must make another trip around its current ring and try again when it next encounters a bridge router. Because of this rule, the flit traveling from N1 to N2 could be deflected an arbitrarily large number of times at 2 and 4 (at entry to bridge routers B1 and B2) if no other mechanism intercedes. This second problem is one of transfer starvation, and we address it with the transfer guarantee mechanism described below.

Our goal in this section is to demonstrate that HiRD provides both the injection guarantee (5.5) and the transfer guarantee (5.5.1) mechanisms. We show correctness in 5.5.2 and quantitatively evaluate both mechanisms in 5.10 and in 52.

5.5. Preventing Injection Starvation: Injection Guarantee

The injection guarantee ensures that every router on a ring can eventually inject a flit. This guarantee is provided by a very simple throttling-based mechanism: when any node is starved (cannot inject a flit) past a threshold number of cycles, it asserts a signal to a global controller, which then throttles injection from every other node. No new traffic will enter the network while this throttling state is active. All existing flits in the network will eventually drain, and the starved node will be able to finally inject its new flit. At that time, the starved node de-asserts its throttling request signal to the global controller, and the global controller subsequently allows all other nodes to resume normal operation.

Note that this injection guarantee can be implemented in a hierarchical manner to improve scalability. In the hierarchical implementation, each individual local ring in the network monitors only its own injection and throttles injection locally if any node in it is starved. After a threshold number of cycles, 3 if any node in the ring still cannot inject, the bridge routers connected to that ring start sending throttling signals to any other ring in the next level of the ring hierarchy they are connected to. In the worst case, every local ring stops accepting flits and all the flits in the network drain and eliminate any potential livelock or deadlock. Designing the delivery guarantee this way requires two wires in each ring and small design overhead at the bridge router to propagate the throttling signal across hierarchy levels. In our evaluation, we faithfully model this hierarchical design.

5.5.1. Ensuring Ring Transfers: Transfer Guarantee

The transfer guarantee ensures that any flit waiting to transfer from its current ring to another ring via a bridge router will eventually be able to enter that bridge router’s queue. Such a guarantee is non-trivial because the bridge router’s queue is finite, and when the destination ring is congested, a slot may become available in the queue only infrequently. In the worst case, a flit in one ring may circulate indefinitely, finding a bridge router to its destination ring with a completely full queue each time it arrives at the bridge router. The transfer guarantee ensures that any such circulating flit will eventually be granted an open slot in the bridge router’s transfer queue. Note in particular that this guarantee is separate from the injection guarantee: while the injection guarantee ensures that the bridge router will be able to inject flits from its transfer queue into the destination ring (and

3In our evaluation, we set this threshold to be 100 cycles.
hence, have open slots in its transfer queue eventually), these open transfer slots may not be distributed fairly to flits circulating on a ring waiting to transfer through the bridge router. In other words, some flit may always be “unlucky” and never enter the bridge router if slots open at the wrong time. The transfer guarantee addresses this problem.

In order to ensure that any flit waiting to transfer out of a ring eventually enters its required bridge router, each bridge router observes a particular slot on its source ring and monitors for flits that are “stuck” for more than a threshold number of retries. (To observe one “slot,” the bridge router simply examines the flit in its ring pipeline register once every N cycles, where N is the latency for a flit to travel around the ring once.) If any flit circulates in its ring more than this threshold number of times, the bridge router reserves the next open available entry in its transfer queue for this flit (in other words, it will refuse to accept other flits for transfer until the “stuck” flit enters the queue). Because of the injection guarantee, the head of the transfer queue must inject into the destination ring eventually, hence an entry must become available eventually, and the stuck flit will then take the entry in the transfer queue the next time it arrives at the bridge router. Finally, the slot which the bridge router observes rotates around its source ring: whenever the bridge router observes a slot the second time, if the flit that occupied the slot on first observation is no longer present (i.e., successfully transferred out of the ring or ejected at its destination), then the bridge router begins to observe the next slot (the slot that arrives in the next cycle). In this way, every slot in the ring is observed eventually, and any stuck flit will thus eventually be granted a transfer.

5.5.2. Putting it Together: Guaranteed Delivery

Before we prove the correctness of these mechanisms in detail, it is helpful to summarize the basic operation of the network once more. A flit can inject into a ring whenever a free slot is present in the ring at the injecting router (except when the injecting router is throttled by the injection guarantee mechanism). A flit can eject at its destination whenever it arrives, and destinations always consume flits as soon as they arrive (which is ensured despite finite reassembly buffers using the Retransmit-Once mechanism [4], as already described in §5.1). A flit transfers between rings via a transfer queue in a bridge router, first leaving its source ring to wait in the queue and then injecting into its destination ring when at the head of the queue, and can enter a transfer queue whenever there is a free entry in that transfer queue (except when the entry is reserved for another flit by the transfer guarantee mechanism). Finally, when two flits at opposite ends of a bridge router each desire to transfer through the bridge router, the Swap Rule allows these flits to exchange places directly, bypassing the queues (and ensuring forward progress).

Our proof is structured as follows: we first argue that if no new flits enter the network, then the network will drain in finite time. The injection guarantee ensures that any flit can enter the network. Then, using the injection guarantee, transfer guarantee, the swap rule, and the fact that the network is hierarchical, any flit in the network can eventually reach any ring in the network (and hence, its final destination ring). Because all flits in a ring must consume any flits that are destined for that node, final delivery is ensured once a flit reaches its final destination ring.

Network drains in finite time. Assume no new flits enter the network (for now). A flit could only be stuck in the network indefinitely if transferring flits create a cyclic dependence between completely full rings. Otherwise, if there are no dependence cycles, then if one ring is full and cannot accept new flits because other rings will not accept its flits, then eventually there must be some ring which depends on no other ring (e.g., a local ring with all locally-destined flits), and this ring will drain first, followed by the others feeding into it. However, because the network is hierarchical (i.e., a tree), the only cyclic dependencies possible are between rings that are immediate parent and child (e.g., global ring and local ring, in a two-level hierarchy). The Swap Rule ensures that when a parent and child ring are each full of flits that require transfer to the other ring, then transfer is always possible, and forward progress will be ensured. Note in particular that we do not require the injection or transfer guarantee for the network to drain. Only the Swap Rule is necessary to ensure that no deadlock will occur.

Any node can inject. Now that we have shown that the network will drain if no new flits are injected, it is easy to see that the injection guarantee ensures that any node can eventually inject a flit: if any node is starved, then all nodes are throttled, no new flits enters the network, and the network must eventually drain (as we just showed), at which point the starved node will encounter a completely empty network into which to inject its flit. (It likely will be able to inject before the network is completely empty, but in the worst case, the guarantee is ensured in this way.)

All flits can transfer rings and reach their destination rings. With the injection guarantee in place, the transfer guarantee can be shown to provide its stated guarantee as follows: because of the injection guarantee, a transfer queue in a bridge router will always inject its head flit
in finite time, hence will have an open entry to accept a new transferring flit in finite time. All that is necessary to ensure that all transferring flits eventually succeed in their transfers is that any flit stuck for long enough gets an available entry in the transfer queue. The transfer guarantee does exactly this by observing ring slots in sequence and reserving a transfer queue entry when a flit becomes stuck in a ring. Because the mechanism will eventually observe every slot in the ring, all flits will be allowed to make their transfers eventually. Hence, all flits can continue to transfer rings until reaching their destination rings (and thus, their final destinations).

5.5.3. Hardware Cost

Our injection and transfer guarantee mechanisms have low hardware overhead. To implement the injection guarantee, one counter is required for each injection point. This counter tracks how many cycles have elapsed while injection is starved, and is reset whenever a flit is successfully injected. Routers communicate with the throttling arbitration logic with only two wires, one to signal blocked injection and one control line that throttles the router. The wiring is done hierarchically instead of globally to minimize the wiring cost (§5.5). Because the correctness of the algorithm does not depend on the delay of these wires, and the injection guarantee mechanism is activated only rarely (in fact, never for our evaluated realistic workloads), the signaling and central coordinator need not be optimized for speed. To provide the transfer guarantee, each bridge router implements “observer” functionality for each of the two rings it sits on, and the observer consists only of three small counters (to track the current timeslot being observed, the current timeslot at the ring pipeline register in this router, and the number of times the observed flit has circled the ring) and a small amount of control logic. Importantly, note that neither mechanism impacts the router critical path nor affects the router datapath (which dominates energy and area).

5.6. HiRD: Evaluation Methodology

We perform our evaluations using a cycle-accurate simulator of a CMP system with 1.6GHz interconnect to provide application-level performance results [82]. Our simulator is publicly available and includes the source code of all mechanisms we evaluated [82]. Tables 2 and 3 provide the configuration parameters of our simulated systems.

Our methodology ensures a rigorous and isolated evaluation of NoC capacity for especially cache-resident workloads, and has also been used in other studies [2–4, 8, 9]. Instruction traces for the simulator are taken using a Pintool [83] on representative portions of SPEC CPU2006 workloads.

We mainly compare to a single bidirectional ring and a state-of-the-art buffered hierarchical ring [56]. Also,
note that while there are many possible ways to optimize each baseline (such as congestion control [5, 8, 9], adaptive routing schemes, and careful parameter tuning), we assume a fairly typical aggressive configuration for each.

**Data Mapping.** We map data in a cache-block-interleaved way to different shared L2 cache slices. This mapping is agnostic to the underlying locality. As a result, it does not exploit the low-latency data access in the local ring. One can design systematically better mapping in order to keep frequently used data in the local ring as in [84, 85]. However, such a mapping mechanism is orthogonal to our proposal and can be applied in all ring-based network designs.

**Application & Synthetic Workloads.** The system is run with a set of 60 multiprogrammed workloads. Each workload consists of one single-threaded instance of a SPEC CPU2006 benchmark on each core, for a total of either 16 (4x4) or 64 (8x8) benchmark instances per workload. Multiprogrammed workloads such as these are representative of many common workloads for large CMPs. Workloads are constructed at varying network intensities as follows: first, benchmarks are split into three classes (Low, Medium and High) by L1 cache miss intensity (which correlates directly with network injection rate), such that benchmarks with less than 5 misses per thousand instructions (MPKI) are “Low-intensity,” between 5 and 50 are “Medium-intensity,” and above 50 MPKI are “High-intensity.” Workloads are then constructed by randomly selecting a certain number of benchmarks from each category. We form workload sets with four intensity mixes: High (H), Medium (M), Medium-Low (ML), and Low (L), with 15 workloads in each (the average network injection rates for each category are 0.47, 0.32, 0.18, and 0.03 flits/node/cycle, respectively).

**Multithreaded Workloads.** We use the GraphChi implementation of the GraphLab framework [86, 87]. The implementation we use is designed to run efficiently on multi-core systems. The workload consists of Twitter Community Detection (CD), Twitter Page Rank (PR), Twitter Connected Components (CC), Twitter Triangle Counting (TC) [88], and Graph500 Breadth First Search (BFS). We simulated the representative portion of each workload and each workload has a working set size of greater than 151.3 MB. On every simulation of these multithreaded workloads, we warm up the cache with the first 5 million instructions, then we run the remaining code of the representative portion.

**Energy & Area.** We measure the energy and area of routers and links by individually modeling the crossbar, pipeline registers, buffers, control logic, and other datapath components. For links, buffers and datapath elements, we use DSENT 0.91 [76]. Control logic is modeled in Verilog RTL. Both energy and area are calculated based on a 45nm technology. The link lengths we assume are based on the floorplan of our designs, which we describe in the next paragraph.

We assume the area of each core to be 2.5 mm x 2.5 mm. We assume a 2.5 mm link length for single-ring designs. For the hierarchical ring design, we assume 1 mm links between local-ring routers, because the four routers on a local ring can be placed at four corners that meet in a tiled design. Global-ring links are assumed to be 5.0 mm (i.e., five times as long as local links), because they span across two tiles on average if local rings are placed in the center of each four-tile quadrant. Third-level global ring links are assumed to be 10mm (i.e., ten times as long as local links) in the 8x8 evaluations. This floorplan is illustrated in more detail in Figure 10 for the 3-level (64-node) HiRD network. Note that one quadrant
of the floorplan of Figure 10 corresponds to the floorplan of the 2-level (16-node) HiRD network. We faithfully take into account all link lengths in our energy and area estimates for all designs.

**Application Evaluation Metrics.** For multiprogrammed workloads, we present application performance results using the commonly-used Weighted Speedup metric [89, 90]. We use the maximum slowdown metric to measure unfairness [15–17, 91–103].

5.7. Performance, Energy Efficiency and Scalability of HiRD

We provide a comprehensive evaluation of our proposed mechanism against other ring baselines. Since our goal is to provide a better ring design, our main comparisons are to ring networks. However, we also provide sensitivity analyses and comparisons to other network designs as well.

5.8. Ring-based Network Designs

5.8.1. Multiprogrammed workloads

Figure 11 shows performance (weighted speedup normalized per node), power (total network power normalized per node), and energy-efficiency (perf./power) for 16-node and 64-node HiRD and buffered hierarchical rings in [46], using identical topologies, as well as a single ring (with different bisection bandwidths).

1. A hierarchical topology yields significant performance advantages over a single ring (i) when network load is high and/or (ii) when the network scales to many nodes. As shown, the buffered hierarchical ring improves performance by 7% (and HiRD by 10%) in high-load workloads at 16 nodes compared to a single ring with 128-bit links. The hierarchical design also reduces power because hop count is reduced. Therefore, link power reduces significantly with respect to a single ring. On average, in the 8x8 configuration, the buffered hierarchical ring network obtains 15.6% better application performance than the single ring with 256-bit links, while HiRD attains 18.2% higher performance.

2. Compared to the buffered hierarchical ring, HiRD has significantly lower network power and better performance. On average, HiRD reduces total network power (links and routers) by 46.5% (4x4) and 14.7% (8x8) relative to this baseline. This reduction in turn yields significantly better energy efficiency (lower energy consumption for buffers and slightly higher for links). Overall, HiRD is the most energy-efficient of the ring-based designs evaluated in this paper for both 4x4 and 8x8 network sizes. HiRD also performs better than Buffered HRing due to the reasons explained in the next section (5.9).

Note that the low intensity workloads in the 8x8 network is an exception. HiRD reduces energy efficiency for these as the static link power becomes dominant for them.
3. While scaling the link bandwidth increases the performance of a single ring network, the network power increases 25.9% when the link bandwidth increases from 64-bit to 128-bit and 15.7% when the link bandwidth increases from 128-bit to 256-bit because of higher dynamic energy due to wider links. In addition, scaling the link bandwidth is not a scalable solution as a single ring network performs worse than the buffered hierarchical ring baseline even when a 256-bit link is used. 

We conclude that HiRD is effective in simplifying the design of the hierarchical ring and making it more energy efficient, as we intended to as our design goal. We show that HiRD provides competitive performance compared to the baseline buffered hierarchical ring design with equal or better energy efficiency.

5.8.2. Multithreaded workloads

Figure 12 shows the performance and power of HiRD on multithreaded applications compared to a buffered hierarchical ring and a single-ring network for both 16-node and 64-node systems. On average, HiRD performs 0.1% (4x4) and 0.73% (8x8) worse than the buffered hierarchical ring. However, on average, HiRD consumes 43.8% (4x4) and 3.1% (8x8) less power, leading to higher energy efficiency. This large reduction in energy comes from the elimination of most buffers in HiRD.

Both the buffered hierarchical ring and HiRD outperform single ring networks, and the performance improvement increases as we scale the size of the network.

Even though HiRD performs competitively with a buffered hierarchical ring network in most cases, HiRD performs poorly on the Page Ranking application. We observe that Page Ranking generates more non-local network traffic than other applications. As HiRD is beneficial mainly at lowering the local-ring latency, it is unable to speed up such non-local traffic, and is thus unable to help Page Ranking. In addition, Page Ranking also has higher network traffic, causing more congestion in the network (we observe 17.3% higher average network latency for HiRD in an 8x8 network), and resulting in a performance drop for HiRD. However, it is possible to use a different number of bridge routers as illustrated in Figure 8a, to improve the performance of HiRD, which we will analyze in Section 5.15. Additionally, it is possible to apply a locality-aware cache mapping technique [84, 85] in order to take advantage of lower local-ring latency in HiRD.

We conclude that HiRD is effective in improving energy efficiency significantly for both multiprogrammed and multithreaded applications.
5.9. Synthetic-Traffic Network Behavior

Figure 13 shows the average packet latency as a function of injection rate for buffered and bufferless mesh routers, a single-ring design, the buffered hierarchical ring, and HiRD in 16 and 64-node systems. We show uniform random, transpose and bit complement traffic patterns. Sweeps on injection rate terminate at network saturation. The buffered hierarchical ring saturates at a similar point to HiRD but maintains a slightly lower average latency because it avoids transfer deflections. In contrast to these high-capacity designs, the 256-bit single ring saturates at a lower injection rate.

As network size scales to 8x8, HiRD performs significantly better than the 256-bit single ring, because the hierarchy reduces the cross-chip latency while preserving bisection bandwidth. HiRD also performs better than Buffered HRing because of two reasons. First, HiRD is able to allow higher peak utilization (91%) than Buffered HRing (71%) on the global rings. We observed that when flits have equal distance in a clock-wise and counter clock-wise direction, Buffered HRing has to send flits to one direction in order to avoid deadlock while deflections in HiRD allow flits to travel in both directions, leading to better overall network utilization. Second, at high injection rates, the transfer guarantee [23] starts throttling the network, disallowing future flits to be injected into the network until the existing flits arrive at their destinations. This reduces congestion in the network and allows HiRD to saturate at a higher injection rate than the buffered hierarchical ring design.

5.10. Injection and Transfer Guarantees

In this subsection, we study HiRD’s behavior under a worst-case synthetic traffic pattern that triggers the injection and transfer guarantees and demonstrates that they are necessary for correct operation, and that they work as designed.

Traffic Pattern. In the worst-case traffic pattern, all nodes on three rings in a two-level (16-node) hierarchy inject traffic (we call these rings Ring A, Ring B, and Ring C). Rings A, B, and C have bridge routers adjacent to each other, in that order, on the single global ring. All nodes in Ring A continuously inject flits to nodes in Ring C, and all nodes in Ring C likewise inject flits to nodes in Ring A. This creates heavy traffic on the global ring across the point at which Ring B’s bridge router connects. All nodes on Ring B continuously inject flits (whenever they are able) addressed to another ring elsewhere in the network. However, because Rings A and C continuously inject flits, Ring B’s bridge router will not be able to transfer any flits to the global ring in the steady state (unless another mechanism such as the throttling mechanism in [23] intercedes).

Results. Table 4 shows three pertinent metrics on the network running the described traffic pattern: average network throughput (flits/node/cycle) for nodes on Rings A, B, and C, the maximum time (in cycles) spent by any one flit at the head of a transfer FIFO, and the maximum number of times any flit is deflected and has to circle a ring to try again. These metrics are reported with the injection and transfer guarantee mechanisms disabled and enabled. The experiment is run with the synthetic traffic pattern for 300K cycles.

The results show that without the injection and transfer guarantees, Ring B is completely starved and cannot transfer any flits onto the global ring. This is confirmed by the maximum transfer FIFO wait time, which is almost the entire length of the simulation. In other words, once steady state is reached, no flit ever transfers out of Ring B. Once the transfer FIFO in Ring B’s bridge router fills, the local ring fills with more flits awaiting a transfer, and these flits are continuously deflected. Hence, the maximum deflection count is very high. Without the injection or transfer guarantees, the network does not ensure forward progress for these flits. In contrast, when the injection and transfer guarantees are enabled, (i) Ring B’s bridge router is able to inject flits into the global ring and (ii) Ring B’s bridge router fairly picks flits from its
local ring to place into its transfer FIFO. The maximum transfer FIFO wait time and maximum deflection count are now bounded, and nodes on all rings receive network throughput. Thus, the guarantees are both necessary and sufficient to ensure deterministic forward progress for all flits in the network.

**Real Applications.** Table 5 shows the effect of the transfer guarantee mechanism on real applications in a 4x4 network. Average transfer FIFO wait time shows the average number of cycles that a flit waits in the transfer FIFO across all 60 workloads. Maximum transfer FIFO wait time shows the maximum observed flit wait time in the same FIFO across all workloads. As illustrated in Table 5, some number of flits can experience very high wait times when there is no transfer guarantee. Our transfer guarantee mechanism reduces both average and maximum FIFO wait time.\(^7\) In addition, we observe that our transfer guarantee mechanism not only provides livelock- and deadlock-freedom but also provides lower maximum wait time in the transfer FIFO for each flit because the guarantee provides a form of throttling when the network is congested. A similar observation has been made in many previous network-on-chip works that use source throttling to improve the performance of the network.\(^5\)\(^,\)\(^6\)\(^,\)\(^104\)\(^,\)\(^105\).

We conclude that our transfer guarantee mechanism is effective in eliminating livelock and deadlock as well as reducing packet queuing delays in real workloads.

### 5.11. Network Latency and Latency Distribution

Figure 14 shows average network latency for our three evaluated configurations: 256-bit single ring, buffered hierarchical ring and HiRD. This plot shows that our proposal can reduce the network latency by having a faster local-ring hop latency compared to other ring-based designs. Additionally, we found that, for all real workloads, the number of deflections we observed is always less than 3% of the total number of flits. Therefore, the benefit of our deflection based router design outweighs the extra cost of deflections compared to other ring-based router designs. Finally, in the case of small networks such as a 4x4 network, a 1-cycle hop latency of a single ring provides significant latency reduction compared to the buffered hierarchical design. However, a faster local-ring hop latency in HiRD helps to reduce the network latency of a hierarchical design and provides a competitive network latency compared to a single ring design in small networks.

In addition, Figure 15 shows the maximum latency and Figure 16 shows the 95th percentile latency for each network design. The 95th percentile latency shows the behavior of the network without extreme outliers. These two figures provide quantitative evidence that the network is deadlock-free and livelock-free. Several observations are in order:

1. HiRD provides lower latency at the 95th percentile and the lowest average latency observed in the network. This lower latency comes from our transfer guarantee mechanism, which is triggered when flits spend more than 100 cycles in each local ring, draining all flits in the network to their destination. This also means that HiRD improves the worst-case latency that a flit can experience because none of the flits are severely delayed.

2. While both HiRD and the buffered hierarchical ring have higher 95th percentile and maximum flit latency compared to a 64-bit single ring network, both hierarchical designs have 60.1% (buffered hierarchical ring) and 53.9% (HiRD) lower average network latency in an 8x8

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\(^7\) As the network scales to 64 nodes, we observe that the average wait time in the transfer FIFO does not affect the overall performance significantly (adding 1.5 cycles per flit).

| Configuration   | Transfer FIFO Wait time (cycles) | Deflections/Retries |
|-----------------|----------------------------------|---------------------|
|                 | (avg/max)                        | (avg/max)           |
| Without guarantees | 3.3 / 169                        | 3.7 / 19            |
| With guarantees  | 0.76 / 72                        | 0.7 / 8             |

Table 5: Effect of transfer guarantee mechanism on real workloads. Data reproduced from \[52\].
network because a hierarchical design provides better scalability on average.

3. Maximum latency in the single ring is low because contention happens only at injection and ejection, as opposed to hierarchical designs where contention can also happen when flits travel through different levels of the hierarchy.

4. The transfer guarantee in HiRD also helps to significantly reduce the maximum latency observed by some flits compared to a buffered design because the guarantee enables the throttling of the network, thereby alleviating congestion. Reduced congestion leads to reduced maximum latency. This observation is confirmed by our synthetic traffic results shown in Section 5.9.  

5.12. Fairness

Figure 17 shows the fairness, measured by the maximum slowdown metric, for our three evaluated configurations. Compared to a buffered hierarchical ring design HiRD, is 8.3% (5.1%) more fair on a 4x4 (8x8) network. Compared to a single ring design, HiRD is 40.0% (296.4%) more fair on a 4x4 (8x8) network. In addition, we provide several observations:

1. HiRD is the most fair design compared to the buffered hierarchical ring and the single ring designs. Compared to a single ring design, hierarchical designs are more fair because the global ring in the hierarchical designs allows flits to arrive at the destination faster. Compared to the buffered hierarchical ring design, HiRD is more fair because HiRD has lower average network latency. HiRD is much more fair for medium and high intensity workloads, where the throttling mechanism in HiRD lowers average network latency.

2. Global rings allow both hierarchical designs to provide better fairness compared to the single ring design as the size of the network gets bigger from 4x4 to 8x8.

3. We conclude that HiRD is the most fair ring design among all evaluated designs due to its overall lower packet latencies and reduced congestion across all applications.
5.13. Router Area and Timing

We show both critical path length and normalized die area for single-ring, buffered hierarchical ring, and HiRD, in Table 6. Area results are normalized to the buffered hierarchical ring baseline, and are reported for all routers required by a 16-node network (e.g., for HiRD, 16 node routers and 8 bridge routers).

| Metric          | Single-Ring | Buffered HRing | HiRD |
|-----------------|-------------|----------------|------|
| Critical path (ns) | 0.33        | 0.87           | 0.61 |
| Normalized area  | 0.281       | 1              | 0.497|

Table 6: Total router area (16-node network) and critical path. Data reproduced from [52].

Two observations are in order. First, HiRD reduces area relative to the buffered hierarchical ring routers, because the node router required at each network node is much simpler and does not require complex flow control logic. HiRD reduces total router area by 50.3% vs. the buffered hierarchical ring. Its area is higher than a single ring router because it contains buffers in bridge routers.

However, the energy efficiency of HiRD and its performance at high load make up for this shortcoming. Second, the buffered hierarchical ring router’s critical path is 42.6% longer than HiRD because its control logic must also handle flow control (it must check whether credits are available for a downstream buffer). The single-ring network has a higher operating frequency than HiRD because it does not need to accommodate ring transfers (but recall that this simplicity comes at the cost of poor performance at high load for the single ring).

5.14. Sensitivity to Link Bandwidth

The bandwidth of each link also has an effect on the performance of different network designs. We evaluate the effect of different link bandwidths on several ring-based networks by using 32-, 64- and 128-bit links on all network designs. Figure 18 shows the performance and power consumption of each network design. As links get wider, the performance of each design increases. According to the evaluation results, HiRD performs slightly
better than a buffered hierarchical ring design for almost all link bandwidths while maintaining much lower power consumption on a 4x4 network, and slightly lower power consumption on an 8x8 network.

Additionally, we observe that increasing link bandwidth can decrease the network power in a hierarchical design because lower link bandwidth causes more congestion in the network and leads to more dynamic buffer, crossbar and link power consumption due to additional deflections at the buffers. As the link bandwidth increases, congestion reduces, lowering dynamic power. However, we observe that past a certain link bandwidth (e.g., 128 bits for buffered hierarchical ring and HiRD), congestion no longer reduces, because deflections at the buffers become the bottleneck instead. This leads to diminishing returns in performance yet increased dynamic power.

### 5.15. Sensitivity to Configuration Parameters

**Bridge Router Organization.** The number of bridge routers connecting the global ring(s) to the local rings has an important effect on system performance because the connection between local and global rings can limit bisection bandwidth. In Figure 19a, we showed three alternative arrangements for a 16-node network, with 4, 8, and 16 bridge routers. So far, we have assumed an 8-bridge design in 4x4-node systems, and a system with 8 bridge routers at each level in 8x8-node networks (Figure 19b). In Figure 19b, we show average performance across all workloads for a 4x4-node system with 4, 8, and 16 bridge routers. Buffer capacity is held constant. As shown, significant performance is lost if only 4 bridge routers are used (10.4% on average). However, doubling from 8 to 16 bridge routers gains only 1.4% performance on average. Thus, the 8-bridge design provides the best tradeoff of performance and network cost (power and area) overall in our evaluations.

**Bridge Router Buffer Size.** The size of the FIFO queues used to transfer flits between local and global rings can have an impact on performance if they are too small (and hence are often full, leading them to deflect transferring flits) or too large (and hence increase bridge router power and die area). We show the effect of local-to-global and global-to-local FIFO sizes in Figures 19b and 19c, respectively, for the 8-bridge 4x4-node design. In both cases, increased buffer size leads to increased performance. However, performance is more sensitive to global-to-local buffer size (20.7% gain from 1-flit to 16-flit buffer size) than to local-to-global size (10.7% performance gain from 1 to 16 flits), because in the 8-bridge configuration, the whole-loop latency around the global ring is slightly higher than the loop latency in each of the local ring, making a global-to-local transfer retry more expensive than a local-to-global one.

For our evaluations, we use a 4-flit global-to-local and 1-flit local-to-global buffer per bridge router, which results in transfer deflection rates of 28.2% (global-to-local) and 34% (local-to-global) on average for multi-programmed workloads. These deflection rates are less than 1% for all of our multithreaded workloads. The deflection rate is much lower in multithreaded workloads because these workloads are less memory-intensive and hence the contention in the on-chip interconnect is low for them.

**Global Ring Bandwidth.** Previous work on hierarchical ring designs does not examine the impact of global ring bandwidth on performance but instead assume equal bandwidth in local and global rings [59]. In Figure 19d, we examine the sensitivity of system performance to global ring bandwidth relative to local ring bandwidth, for the all-High category of workloads (in order to stress check bisection bandwidth). Each point in the plot is described by this global-to-local ring bandwidth ratio. The local ring design is held constant while the width of the global ring is adjusted. If a ratio of 1:1 is assumed (leftmost bar), performance is significantly worse than the best possible design. Our main evaluations in 4x4 networks use a ratio of 2:1 (global:local) in order to provide equivalent bisection bandwidth to a 4x4 mesh baseline. Performance increases by 81.3% from a 1:1 ratio to the 2:1 ratio that we use. After a certain point, the global ring becomes less of a bottleneck, and further
global-ring bandwidth increases have massively smaller effects.

**Delivery Guarantee Parameters.** We introduced injection guarantee and ejection guarantee mechanisms to ensure every flit is eventually delivered to its destination. These guarantees are clearly described in detail in our original work [23]. The injection guarantee mechanism takes a threshold parameter that specifies how long an injection can be blocked before action is taken. Setting this parameter too low can have an adverse impact on performance, because the system throttles nodes too aggressively and thus underutilizes the network. Our main evaluations use a 100-cycle threshold. For high-intensity workloads, performance drops by 21.3% when using an aggressive threshold of only 1 cycle. From 10 cycles upward, variation in performance is at most 0.6%: the mechanism is invoked rarely enough that the exact threshold does not matter, only that it is finite (is required for correctness guarantees). In fact, for a 100-cycle threshold, the injection guarantee mechanism is never triggered in our real applications. Hence, the mechanism is necessary only for corner-case correctness. In addition, we evaluate the impact of communication latency between routers and the coordinator. We find less than 0.1% variation in performance for latencies ranging from 1 to 30 cycles (when parameters are set so that the mechanism becomes active); thus, slow, low-cost wires may be used for this mechanism.

The ejection guarantee takes a single threshold parameter: the number of times a flit is allowed to circle around a ring before action is taken. We find less than 0.4% variation in performance when sweeping the threshold from 1 to 16. Thus, the mechanism provides correctness in corner cases but is unimportant for performance in the common case.

**5.16. Comparison Against Other Ring Configurations**

Figure [20] highlights the energy-efficiency comparison of different ring-based design configurations by showing weighted speedup (Y axis) against power (X axis) for all evaluated 4x4 networks. HiRD is shown with the three different bridge-router configurations (described in §5.2). Every ring design is evaluated at various link bandwidths (32-, 64-, 128- and 256-bit links). The top-left is the ideal corner (high performance, low power). As the results show, at the same link bandwidth, all three configurations of HiRD are more energy efficient than the evaluated buffered hierarchical ring baseline designs at this network size.

We also observe that increasing link bandwidth can sometimes decrease router power as it reduces deflections in HiRD or lowers contention at the buffers in a buffered hierarchical ring design. However, once links are wide enough, this benefit diminishes for two reasons: 1) links and crossbars consume more energy, 2) packets arrive at the destination faster, leading to higher power as more energy is consumed in less time.

**5.17. Comparison Against Other Network Designs**

For completeness, Table [7] compares HiRD against several other network designs on 4x4 and 8x8 networks using the multiprogrammed workloads described in Section 5.6.
We compare our mechanism against a buffered mesh design with buffer bypassing [27] [28]. We configure the buffered mesh to have 4 virtual channels (VCs) per port with 8 buffers per VC. We also compare our mechanism against CHIPPER [4], a low-complexity bufferless mesh network. We use 128-bit links for both designs. Additionally, we compare our mechanism against a flattened butterfly [18] with 4 VCs per output port, 8 buffers per VC, and 64-bit links. Our main conclusions are as follows:

1. Against designs using the mesh topology, we observe that HiRD performs very closely to the buffered mesh design both for 4x4 and 8x8 network sizes, while a buffered hierarchical ring design performs slightly worse compared to HiRD and buffered mesh designs. Additionally, HiRD performs better than CHIPPER in both 4x4 and 8x8 networks, though CHIPPER consumes less power in an 8x8 design as there is no buffer in CHIPPER.

2. Compared to a flattened butterfly design, we observe that HiRD performs competitively with a flattened butterfly in a 4x4 network, but consumes lower router power. In an 8x8 network, HiRD does not scale as well as a flattened butterfly network and performs 11% worse than a flattened butterfly network; however, HiRD consumes 59% less power than the flattened butterfly design.

3. Overall, we conclude that HiRD is competitive in performance with the highest performing designs while having much lower power consumption.

6. Other Methods to Improve NoC Scalability

In this Section, we now discuss other approaches that are designed to improve scalability of NoCs.

**Ring-based NoCs.** Hierarchical ring-based interconnect was proposed in a previous line of work [44],[44],[51],[106]. We have already extensively compared to past hierarchical ring proposals qualitatively and quantitatively. The major difference between HiRD and these previous approaches is that HiRD uses deflection-based bridge routers with minimal buffering, and node routers with no buffering. In contrast, all of these previous works use routers with in-ring buffering, wormhole switching and flow control. Kim et al. propose tNoCs, hybrid packet-flit credit-based flow control [106] and Clumsy Flow Control (CFC) [64]. However, these two designs add additional complexity because tNoCs requires an additional credit network to guarantee forward progress while CFC requires coordination between cores and memory controllers. Flow control in HiRD is different from that in these works due to HiRD’s simplicity (with deflection based flow control, the Retransmit-Once mechanism, and simpler local-to-global and global-to-local buffers). Additionally, throttling decisions in HiRD can be made locally in each local ring as opposed to global decisions in CFC [64] and tNoCs [106].

Udipi et al. propose a hierarchical topology using global and local buses [74]. Using buses limits scalability in favor of simplicity. In contrast, HiRD design has more favorable scaling, in exchange for using more complex flit-switching routers. Das et al. [75] examine several hierarchical designs, including a concentrated mesh (one mesh router shared by several nearby nodes).

A previous system, SCI (Scalable Coherent Interface) [107], also uses rings, and can be configured in many topologies (including hierarchical rings). However, to handle buffer-full conditions, SCI NACKs and subsequently retransmits packets, whereas HiRD deflects only single flits (within a ring), and does not require the sender to retransmit its flits. SCI was designed for off-chip interconnect, where tradeoffs in power and performance are very different from those in on-chip interconnects. The KSR (Kendall Square Research) machine [108] uses a hierarchical ring design that resembles HiRD, yet these techniques are not disclosed in detail and, to our knowledge, have not been publicly evaluated in terms of energy efficiency.

**Scalable Topology Design.** While low-radix topologies (e.g., ring, tori [109], meshes [110], Express Cubes [10] and Kilo-NoC [12],[13],[111]) offers low area and power consumption, high-radix topologies [113],[112] provide scalable alternatives to large scale systems. A flat-
tended butterfly topology provides a scalable design that allows routers to send flits using two hops [18]. A HyperX network [12] extends the hypercube [61] design to minimize cost and lowering the latency. A SlimNoC [22] network provides a low-diameter, high-radix that further reduces the power and area through a SlimFly topology [113].

Low Cost Router Designs. Kim [79] proposes a low-cost router design that is superficially similar to HiRD’s node router design where routers convey traffic along rows and columns in a mesh without making use of crossbars, only pipeline registers and MUXes. Once traffic enters a row or column, it continues until it reaches its destination, as in a ring. Traffic also transfers from a row to a column analogously to a ring transfer in our design, using a “turn buffer.” However, because a turn is possible at any node in a mesh, every router requires such a buffer [114, 115]: in contrast, HiRD require similar transfer buffers only at bridge routers, and their cost is paid for by all nodes. Additionally, this design does not use deflections when there is contention.

Mullins et al. [116] propose a buffered mesh router with single-cycle arbitration. Abad et al. [117] propose the Rotary Router that consists of two independent rings that join the router’s ports and perform packet arbitration similar to standalone ring-based networks. Both the Rotary Router and HiRD allow a packet to circle a ring again in a “deflection” if an ejection (ring transfer or router exit) is unsuccessful. Nicopoulos et al. [14] propose a buffer structure that allows the network to dynamically regulate the number of virtual channels. Kodi et al. [118] propose an orthogonal mechanism that reduces buffering by using links as buffer space when necessary. Multidrop Express Channels [10] also provides a low cost mechanism to connect multiple nodes using a multidrop bus without expensive router changes.

7. Conclusion and Future Outlook

Scalability and energy are two major concerns as core counts increase in commercial processors. To provide a design that is area-efficient and energy efficient without sacrificing performance, this chapter first presents MinBD [3, 72, 73]. MinBD is a minimally-buffered deflection router design. It combines deflection routing with a small buffer, such that some network traffic that would have been deflected is placed in the buffer instead. By using the buffer for only a fraction of network traffic, MinBD makes more efficient use of a given buffer size than a conventional input-buffered router. Its average network power is also greatly reduced: relative to an input-buffered router, buffer power is much lower, because buffers are smaller. Relative to a bufferless deflection router, dynamic power is lower, because deflection rate is reduced with the use of a small energy-conscious buffer.

To further improve scalability, this chapter discusses HiRD [23, 24, 52], a simple hierarchical ring-based NoC design that employs deflection routing. Past work has shown that a hierarchical ring design yields good performance and scalability relative to both a single ring and a mesh. HiRD has two new contributions: (1) a simple router design that enables ring transfers without in-ring buffering or flow control, instead using limited deflections (retries) when a flit cannot transfer to another ring, and (2) two guarantee mechanisms that ensure deterministically-guaranteed forward progress despite deflections. The evaluations show that HiRD enables a simple and low-cost implementation of a hierarchical ring network. Our HiRD evaluations also show that HiRD is more energy-efficient than several other topologies while providing competitive performance.

Despite the extensive design space for low-power NoC we considered so far, a number of key challenges remain to enable truly scalable and energy-efficient interconnection networks for modern systems and workloads. We believe that low-cost, energy-efficient network-on-chip design is an important challenge in scaling modern architectures beyond traditional CMPs. For example, heterogeneous architectures in modern SoCs can stress the interconnect through their imbalanced loads that are a consequence of largely different demands across many different types of applications and accelerators. Relatively new technology such as chiplets [119, 120] or new types of memory [121, 125] can create demands for efficient interconnection network designs that connect multiple memory nodes together. Especially processing-in-memory systems [124, 179] can require well-connected memory arrays via efficient interconnects to tightly couple computation and communication. A fundamentally low-cost and energy-efficient interconnection network can further push the boundaries of computing systems, leading to significant improvements in performance and energy, and potentially enabling new applications and computing platforms.

Acknowledgments

This chapter incorporates revised material from another earlier article published in Parallel Computing in 2016 [25], the proceedings of the International Symposium on Computer Architecture and High Performance
Computing in 2014 [23], the proceedings of the International Symposium on Networks-on-Chip in 2012 [3] and the proceedings of the International Symposium on High Performance Computer Architecture in 2011 [4].

This article is based on research done over the course of the past 13 years in the SAFARI Research Group on the topic of Network-on-Chips (NoC). We thank all of the members of the SAFARI Research Group, and our collaborators at Carnegie Mellon, ETH-Zurich, and other universities, who have contributed to the various works we describe in this paper. Thanks also goes to our research group’s industrial sponsors over the past 13 years, especially Alibaba, AMD, ASML, Google, Huawei, Intel, Microsoft, NVIDIA, Samsung, Seagate, and VMware. This work was also partially supported by the Intel Science and Technology Center for Cloud Computing, the Semiconductor Research Corporation, the Data Storage Systems Center at Carnegie Mellon University, various NSF and NIH grants, and various awards, including the NSF CAREER Award, the Intel Faculty Honor Program Award, a number of Google and IBM Faculty Research Awards to Onur Mutlu, and the Royal Thai Scholarship to Rachata Ausavarungnirun.

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