Design and characterization of high-speed CMOS pseudo-LVDS transceivers

S V Kondratenko
National Research Nuclear University MEPhI (Moscow Engineering Physics Institute), Kashirskoe highway 31, Moscow, 115409, Russia

E-mail: utakser@mail.ru

Abstract. High-speed transceiver for on-board systems of data collection and processing need to meet additional requirements, such as low power consumption and increased radiation hardness. It is therefore necessary to compare and search for alternative variants of transceivers on the physical layer, where high transfer speed is not achieved at the cost of a significant increase in power consumption or a limitation of transmission distance by the size of a printed circuit board. For on-board applications, it is also necessary to solve the problem of increasing the radiation hardness without going to expensive types of technology. In this paper, we studied some variants of implementation of pseudo-LVDS transceivers and analyzed their achievable quantitative characteristics. According to the results of calculations and analysis of the literature, specialized transceivers of this type, intended for the manufacture or manufactured according to the bulk CMOS technology processes in the range of 250–80 nm, can provide data speeds up to 6 Gbps at a specific power consumption of less than 4 mW/Gbps.

1. Introduction
On-board systems for data collection and processing obtained in the course of physical experiments can be highly specialized for data collection only and use the land powerful computing resources or based on close cooperation with the productive onboard computer network. Accordingly, these systems can use very different traffic connections and apply a variety of technical implementation – from the low-speed serial interfaces such as CAN to Gigabit Ethernet, and different transmission media – from classic cabling and wireless channels to fiber optics. Large amounts of data have to be processed in the shortest possible time. This leads to the need for the physical layer represented by a new generation of high-speed transceivers with speeds up to several Gbps. Even if this speed is not required directly in a physical experiment, it is useful to have appropriate margin for two reasons. First, this margin may be considered as the foundation for the future. Secondly, it is a mean of ensuring the operation of such transceivers in comfort, far from limiting speeds conditions in view of an adequate margin for the impact of external factors (including radiation) and the natural degradation of the technical characteristics of the onboard equipment operated by a long time. This logic is true, of course, if the speed margin is provided not at the cost of substantial and continuous increase in power consumption, as is typical, for example, for CML interface transceivers. Due to its low power consumption combined with a number of other advantages the transceivers with LVDS interface are currently widely used in the on-board systems [1,2]. LVDS-transceivers’ disadvantage is the relatively low speed of transmission (typically – from 0.2 to 0.4 Gbps, the maximum standard – about 2 Gbps). It makes sense to analyze the features and specifications of transceivers with pseudo-LVDS interface that may provide speed higher 6 Gbps (according to the published data [3-6]).
2. Properties of pseudo-LVDS transmitters and receivers

Analysis of the literature [3-6] shows that there is currently no clear definition of pseudo-LVDS interface, although the term is often used by different authors. This situation is obviously connected with various deviations from LVDS-standard [7], which often aim to increase the allowable speed in comparison with the one specified in the standard. The above-mentioned restriction (2 Gbps) is connected, in turn, with a built-in LVDS-standard restriction on slew-rate of the signals from the driver outputs, which limits radiated emissions. Important advantages of LVDS-interface are follows:

1. The insensitivity of the transmission quality to the impedance mismatch between the transmitter (driver) output and the transmission line characteristic impedance. In fact, a pair of LVDS transmitter – LVDS receiver in the classic version implements a transmit mode type of current loop ensuring impedance matching conditions at the receiver input.
2. Small swing of the output signals of the driver (typically ±350 mV), thereby reducing power consumption and achieving high performance due to the reduction of parasitic capacitance recharge problems.
3. The relatively low slew rate of signal change at the driver output (~ 0.3V / 0.3ns = 1 V / ns) and the differential nature of processed and transmitted signals, which leads, as mentioned, to the reduction in the level of noise generated primarily by the driver in general purpose circuits (bus power and ground).
4. The lack of binding of the driver’s output signal levels to the supply voltage and active maintenance of their common (in-phase) level near 1.2 V (or 1.25V at the formation of a reference voltage by division of the supply voltage 2.5V). At the direct communication with the receiver this provides maximum available symmetrical value range ±1V for common-mode noise on the transmission line.

The question is whether we can preserve these benefits during the transition to a non-standard pseudo-LVDS interface with increased speed without violating the basic properties of LVDS and pseudo-LVDS transceivers compatibility on the electric level? Possible and known solution is to construct a pseudo-LVDS driver with impedance matching at the output to the transmission line characteristic impedance due to the built-in resistor 100 Ohms, and increased in two times output current to restore the value of the standard scope of output signals. Figure 1 shows the structure of the described pseudo-LVDS transmitter. For standard LVDS transmitter is no built-in resistor R, and the nominal output current I = 3.5 mA (instead of 2×I). In the transition to such a pseudo-LVDS transmitter listed above LVDS interface advantages (except claim 3 and partly to claim 2) are reserved, and the following additional advantages are provided:

- It may be used as a direct communication with the receiver and communication through coupling capacitors, that is important when there is a relatively large distance between the transmitter and receiver due to a possible difference of ground potential.
- Output impedance nominally equal to the characteristic impedance of the transmission line, thereby reducing reflections and allows operation at higher speeds and, at the same speed, the ability to work on a long line.
- Improved performance due to the reduction of influence of the stray parasitic capacitors at the transmitter output / receiver inputs and increased current in the output stage of the LVDS driver, which recharges these capacitors.

The disadvantage of a such pseudo-LVDS driver is the increased current consumption, which makes up a significant portion of the total current consumption of the transmitter and receiver.
Figure 1. The variant of pseudo-LVDS transceiver (LT – Level Translator).

In comparison with the LVDS-transmitters LVDS-receivers do not have such pronounced features as operate overall function of comparison of differential input signal, coming from the transmission line, to zero regardless of the absolute levels of these signals, as well as receivers that implement other interface types.

3. The characteristics of pseudo-LVDS transceivers

Table 1 shows the characteristics of a number of pseudo-LVDS devices taken from published sources and based on the results obtained by the design within this work.

| № | Pseudo-LVDS device | Main deviations from LVDS standard | Speed, bps | Relative power consumption, mW/Gbps | Technology | Ref. |
|---|--------------------|-----------------------------------|------------|-----------------------------------|------------|-----|
| 1 | Transmitter (driver) | Amplitude of output differential signal is 0.2 V, voltage of power source is 1.2 V, voltage-mode of transmission | 3G         | 3.8                               | CMOS       | [3] |
| 2 | Transmitter         | Amplitude of output differential signal is 0.196 V, voltage of power source is 1.2 V | 6G         | 4.2                               | CMOS       | [4] |
| 3 | Driver³             | Pseudo-differential output, voltage of power sources are 1 V and 1.4 V | 105M       | N/A                               | N/A        | [5] |

Table 1. The characteristics of pseudo-LVDS devices.
| №  | Pseudo-LVDS device | Main deviations from LVDS standard | Speed, bps | Relative power consumption, mW/Gbps | Technology | Ref. |
|----|-------------------|-----------------------------------|-----------|-------------------------------------|------------|-----|
| 4  | Driver\(^2\)      | Pair of CMOS buffers with resistive divider at the outputs | 622M      | 34                                  | CMOS 0.18 \(\mu m\)\(^3\) | [6] |
| 5  | Transmitter true-LVDS | -                                  | 1.25G     | 12                                  | CMOS 90 nm\(^3\) | -   |
| 6  | Transmitter       | Matching 100 Ohm resistor at the outputs, increased driver output current | 2.5+G     | 14                                  |            |     |
| 7  | Transmitter       | Voltage of power source is 1.2V, capacitive decoupling with the receiver | 5+G       | 3.4                                 |            |     |

\(^1\) configurable output buffer composed of ADC type of LTC2284  
\(^2\) emulation of LVDS driver composed of FPGA Virtex-E series  
\(^3\) also 0.25 \(\mu m\) peripherals used

From the analysis of the table 1 it follows that a significant reduction in power consumption can be achieved when using LVDS-drivers based on a reduced compare with peripheral core voltage. Calculations have shown that receivers, designed as a pair to LVDS or pseudo-LVDS transmitters, do not reduce the overall speed and consume significantly less power.

**4. Conclusion**

LVDS transceivers, commonly used in on-board systems of data collection and processing, may be modified to substantially increase the transmission speed while maintaining their main advantages in comparison with the high-speed transceivers that implement other types of interfaces at the physical layer. Three variants of pseudo-LVDS transmitters carried by bulk CMOS 90nm technology were analyzed. It is shown, that for these transmitters operating in a tandem with designed receivers there is the possibility to reach speed more than 5 Gbit/s at a comparable or lower (relative to published data [3-6]) specific power consumption.

**Acknowledgments**

Author acknowledge partial support by MEPhi Academic Excellence Project (contract № 02.a03.21.0005, 27.08.2013).

**References**

[1] Parkes S 2012 *SpaceWire User’s Guide* (STAR-Dundee Limited) p 115  
[2] Kondratenko S V et al. 2010 *Proceedings of the 3rd International SpaceWire Conference (SpaceWire-2010)* p 239  
[3] Bae J-H et al. 2010 *IEICE Transactions on Electronics* 1 132  
[4] Kim S, Kong B S and Lee C G 2006 *Solid-state circuits conference (ESSCIRC 2006)* 9 484  
[5] 2007 *High Speed ADC Products. High Performance Analog ICs* (Linear Technology Corporation) p 12  
[6] 2000 *LVDS Comparison. APEX 20KE vs. Virtex-E Devices* PIB29 (Altera Corporation) p 24  
[7] TIA/EIA STANDARD 2001 *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* ANSI/TIA/EIA-644-A-2001 (Arlington: Telecommunications Industry Association)