Design of Wideband Communication Waveform for Swarm UAV Warfare

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Abstract. In order to improve the battlefield survivability and information reliability of swarm UAV (unmanned aerial vehicle) data link network, the signal waveform was redesigned in signal time domain and frequency, combining with symbol interleave and LDPC encoding. The physical layer design of the terminal machine was optimized, the collision probability of the signal was reduced, and the transmission time delay of time-sensitive information was reduced.

1 Introduction

With the continuous improvement of the combat technology performance of UAV, its application fields continue to expand. Currently, military UAV have been widely used in battlefield surveillance and reconnaissance, electronic countermeasures, target indication, war result evaluation, and communication relay[1-3]. It has been difficult to meet the operational requirements, and it has gradually evolved from a stand-alone combat mode to a swarm combat mode. In order to meet the future unmanned and intelligent battle needs, it is urgent to research and develop our army's swarm UAV network technology to achieve the swarm. The fast and dynamic self-organizing network between UAVs and the low-latency transmission of sensitive information enable the network to have self-organizing, self-healing capabilities, and the advantages of efficient and fast networking to meet the complex coordinated combat needs of UAV platforms[4-6]. Research on coordinated networking technology for drone measurement and control and information transmission, focusing on breaking through its key technologies, so as to achieve a no center, fast, and dynamic self-organizing network of swarm UAV, and greatly enhance the cooperative operations of UAV in complex combat environments Capabilities lay the foundation for the development of China's UAV combat distributed ad hoc network[7].

2 Technical designed

In order to improve the battlefield survivability and information transmission reliability of the swarm UAV data link networking in a complex electronic countermeasure environment, it is necessary to jointly design the signal waveform in the time and frequency domains to improve the bandwidth utilization and reduce the signal interception probability. Improve the anti-interference ability and improve the effective signal-to-noise ratio, combined with symbol interleaving and LDPC encoding and decoding, further improve the system's anti-interference and signal transmission reliability. Through the above-mentioned technical
methods, the physical layer design of the terminal is optimized to reduce the collision probability of the signal and reduce the time. Delay in transmitting sensitive information\cite{4,7}.

The signal waveform design of the unmanned combat platform ad hoc network data transmission end and the corresponding demodulation principle block diagram are shown in Fig. 1.

![Diagram of the sender and receiver of the ad hoc network.](image)

**Figure 1.** Block diagram of the sender and receiver of the ad hoc network.

The message from the upper layer is divided into multiple data groups, scrambled after error correction coding and symbol interleaving, and then frequency-hopping and time-hopping processing to improve the high anti-interference ability and enhance the low interception performance of the signal. The purpose of interleaving is to improve the anti-pulse interference ability of the message, so as to reduce the serious degradation of the transmission performance of the communication medium due to the sudden interference of the message symbol. The receiver only needs to do the opposite to restore the message. In order to ensure the SPMA protocol, Before sending data, channel busy and busy detection and prediction technology are needed.

### 1.1 Channel busyness detection and prediction technology

The channel load condition is the basis for the MAC protocol to determine the packet access channel or random back-off, which largely determines the performance of the MAC protocol. UAV measurement and control and information transmission collaborative networking High priority services use SPMA based on statistical priority access control protocol. The network internally determines which nodes are currently allowed to transmit signals based on the busyness of the channel and the priority of service transmission\cite{8}.

The traditional method uses carrier sensing to determine whether the channel is busy or not, but in the collaborative network of UAV measurement and control and information transmission, each node is widely distributed, the communication distance is long, the network topology changes rapidly, and the carrier sensing results are inaccurate, and the transmission delay caused by listening is large\cite{2}.

This design uses a channel busyness detection and prediction algorithm based on time-frequency analysis to provide a basis for judging channel access based on the busyness of the channel and distinguishing business priorities. Nodes count the number of bursts received by the channel over the past period to predict the number of bursts received in the current time frame, and use the predicted number of bursts to determine the current level of busyness, avoiding the delay consumed by the listening channel before each packet is sent, and grouping for different priorities at the same time. Sending or back-off provides a more accurate basis to prevent packet congestion and slow latency caused by packet access to the channel too quickly\cite{9}.
When LDPC decoding is implemented on FPGA, the top-level modules and sub-modules are divided using a layered idea. The implementation of LDPC coding is mainly composed of four modules, namely the top-level module, the coding module, the input buffer, and the output buffer. Among them, the top-level module calls other three modules. The relationship between each module is shown in Fig.2.

LDPC input buffer module, Double-buffered RAM is used when inputting data. Calling the Xilinx IP core can implement RAM instantiation with inconsistent read and write bit widths. Inbuff_wea is the writing signal that controls the RAM. When the highest bit of the address signal is 0, it means the first bit. When the highest bit is 1, it means the second bit. The highest bit of the address of the write data part is controlled by the BCH module, and the highest bit of the address of the read data part is controlled by the LDPC module. The system design guarantees that the control signal is sent by the ctrl module At ldpc_start, the next pending bit frame has been filled.[10]

LDPC encoding module, implements error correction encoding of transmitted data, which contains a total of 4 states, idle state, clear state, sub-matrix calculation state, and iterative calculation state.

LDPC output module, In the output module, dual-buffer RAM is also used, and outbuff_rd is the read signal of the sending RAM. When the highest bit of the address signal is 0, the corresponding data of the highest address of the output RAM is 0, the highest bit of the address is 1, it corresponds to the data with the highest address of the data RAM being 1. The change of the highest bit of the address is completed when the last one of the frame of data is stored.

### 1.3 GMSK modulation

![GMSK modulation process](image)
Compared with the MSK modulation used by the Link16 data link, GMSK uses a Gaussian filter for pre-modulation filtering before modulation, which reduces the jump energy of the carrier when switching frequency points, which can maximize the channel throughput and effectively reduce bit errors. The GMSK modulation process is shown in Fig. 3.

1.4 Symbol interleaving

The purpose of symbol interleaving is to discretize a long burst error in a time-division high-speed data chain into random errors, and then use random coding to correct random errors to eliminate random errors. The greater the interleaving depth, the greater the dispersion and the resistance to burst errors. The stronger the ability is. In the actual design, the interleaver takes the form of row-by-row input and column-by-column output, starting from the upper left corner and writing from the lower right corner.

1.5 Frequency hopping and time hopping synchronization

The primary condition of the demodulation signal at the receiving end is to obtain frequency hopping and time synchronization. The corresponding schematic block diagram is shown in Fig. 4.

![Figure 4](image_url)

Figure 4. Schematic diagram of parallel acquisition of frequency-hopping system.

Because the receiving end knows the frequency hopping and time hopping rules of the transmitting end in advance, the receiver uses the sequence matching filter to capture in parallel at all frequency hopping points according to the same frequency hopping and time hopping rules. After the input signal passes the sequence matching filter, through the adder, if the addition result is greater than the threshold, it indicates that the input signal meets the requirements of the sequence matching filter, then the synchronization indication is output, and the receiving end obtains the same frequency-hopping pattern as the transmitting end.

1.6 Frame synchronization

The premise of the receiver demodulating data is frame synchronization. The frame header position of each frame of data is an extended training sequence with a length of 64, which has good autocorrelation characteristics. The receiver uses a pre-stored local reference signal to correlate with the received signal. Operation, you can get very obvious peak characteristics, and use the time position of the peak to achieve frame synchronization.
1.7 GMSK demodulation

The GMSK demodulation process is shown in Fig. 5. After the modulated signal is filtered out by the IF filter to remove high-frequency components, it is divided into two channels for processing, one of which passes the delay of $t$, and the other does not change. The two signals are multiplied and then low. After the pass filter is processed, the demodulated information is obtained by the decision gate.

![GMSK demodulation process](image)

Figure 5. GMSK demodulation process.

The demodulated data is descrambled, deinterleaved, and LDPC error-corrected and decoded to output demodulated message data.

3 Summary

This design is aimed at the information transmission between swarm UAV with fast topology changes, high real-time signal transmission requirements, and crowded channel transmission. The channel busyness detection and prediction algorithm through time-frequency analysis reduces channel delay and channel congestion, use GMSK modulation to reduce signal hopping energy, improve channel signal transmission capacity, and reduce bit error rate, use symbol interleaving to disrupt the order of data signals, reduce correlation, become random signals, and eliminate the danger of sudden errors, send and receive. The terminal adopts a structure of one transmission and four receptions, which optimizes the physical layer waveform design of the swarm drone, and proposes a feasible solution for swarm drone information transmission.

The bee colony drone operation has the huge advantages of fast response speed, zero casualty rate, and huge development potential in local and asymmetric warfare, but there are still many technical difficulties to be overcome before practical application.

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