Profile-Guided Parallel Task Extraction and Execution for Domain Specific Heterogeneous SoC

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Abstract—In this study, we introduce a methodology for automatically transforming user applications in the radar and communication domain written in C/C++ based on dynamic profiling to a parallel representation targeted for a heterogeneous SoC. We present our approach for instrumenting the user application binary during the compilation process with barrier synchronization primitives that enable runtime system schedule and execute independent tasks concurrently over the available compute resources. We demonstrate the capabilities of our integrated compile time and runtime flow through task-level parallel and functionally correct execution of real-life applications. We perform validation of our integrated system by executing four distinct applications each carrying various degrees of task level parallelism over the Xeon-based multi-core homogeneous processor. We use the proposed compilation and code transformation methodology to re-target each application for execution on a heterogeneous SoC composed of three ARM cores and one FFT accelerator that is emulated on the Xilinx Zynq UltraScale+ platform. We demonstrate our runtime’s ability to process application binary, dispatch independent tasks over the available compute resources of the emulated SoC on the Zynq FPGA based on three different scheduling heuristics. Finally, we demonstrate execution of each application individually with task level parallelism on the Zynq FPGA and execution of workload scenarios composed of multiple instances of the same application as well as mixture of two distinct applications to demonstrate ability to realize both application and task level parallel execution. Our integrated approach offers a path forward for application developers to take full advantage of the target SoC without requiring users to become hardware and parallel programming experts.

Index Terms—Task-level parallelism, dynamic profiling, heterogeneous SoC and runtime, parallelism detection

I. INTRODUCTION

SoCs composed of a pool of heterogeneous processing elements offer performance gains over their homogeneous counterparts as they allow pairing each task or execution phase of application with a suitable processing element (PE) from a pool of heterogeneous processing elements.

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TABLE I: Related work on program analysis and workload parallelization

| Framework | Static | Dynamic | Multithreaded | Heterogeneous | End-to-End |
|-----------|--------|---------|---------------|---------------|-----------|
| Tensorflow [1] | ✔️ | ✔️ | | | ✔️ |
| Hadoop [2] | ✔️ | | ✔️ | | ✔️ |
| HPVM [3] | ✔️ | ✔️ | | | ✔️ |
| Cilk et al. [4] | ✔️ | | ✔️ | | ✔️ |
| Parx [5] | ✔️ | ✔️ | | ✔️ | ✔️ |
| SD3 [6] | ✔️ | | ✔️ | | ✔️ |
| Wang et al. [7] | ✔️ | | ✔️ | | ✔️ |
| Kernels [8] | ✔️ | | ✔️ | | ✔️ |
| Chir | | | ✔️ | | ✔️ |

Based on the state of the system resources. To harness this flexibility, programming models have been introduced where application developers or domain experts guide the compilation process by making task to PE mapping decisions based on offline profiling. For example, in CUDA-based programming, programmers have to understand the application, partition it into independent tasks, and manually map them to threads and blocks in GPU. This model of computation results in a static execution flow and a hand-crafted schedule that is greedily tuned for a single application. In this study, we introduce an integrated compile time and runtime environment that automatically detects parallelism in the user application, transforms the program to parallel representation, and provides the runtime system with a flexible binary structure. This allows the runtime system to dynamically schedule and launch these tasks in parallel to heterogeneous resources based on the system state rather than rely on a hand-crafted static schedule.

Programming models such as OpenMP [9] and Pthread [10] offer interfaces like pragma labels and thread bindings where users specify the parallelism in their applications explicitly. Program analysis tools have been introduced to enable transforming a user application to a parallel representation based on static [1]–[4] or dynamic [5]–[8] analysis as listed in Table I. These tools also vary in terms of their approach to parallelism detection from instruction level granularity targeted for multi-core architectures to task level granularity for heterogeneous architectures. Static parallelization methods require the user to express the application in an explicit data flow style either using a domain-specific language (DSL) or a dedicated framework. Among the dynamic methods, our approach is the only one that targets both homogeneous multi-core architectures and heterogeneous SoCs in an end-to-end integrated compile and run time flow.
Our approach employs a profile-guided dynamic analysis of memory access patterns using a combination of memory tuples, loop-access patterns and function pointers for inferring the required runtime control states that are necessary for task-level dependence analysis. It offers the ability to retarget user applications with coarse-grained computation tasks for heterogeneous architectures through code transformations that enable parallel task execution in one unified compile time and runtime framework. The key technical contributions of this study are as follows:

- We introduce a novel profile-guided memory analysis approach to detect the data dependencies among coarse-grained tasks in a given application and expose the parallelism among those tasks.
- We present a methodology that partitions the user application into serial and parallel tasks following a fork-join programming model and compiles into an application binary representation with embedded parallelism and instrumentation such that the runtime system can issue and execute all independent tasks concurrently.
- We integrate the profile-guided parallel program generation tool flow with an open-source runtime and demonstrate an end-to-end system that is able to compile and execute real-life applications on off-the-shelf platforms.
- We demonstrate the ability to identify task-level parallelism for real life applications, transform user-application for parallel execution, and successfully execute those tasks in parallel first using an event-driven simulation environment DS3 [11]. After validating the ability to extract parallelism, we demonstrate functionally correct task-level parallelism in our runtime for those parallelized applications on a homogeneous 8-core Xeon processor. Finally, we demonstrate functionally correct parallel execution on an emulated heterogeneous SoC composed of 3 ARM CPUs and an FPGA-based accelerator. This emulation platform illustrates not only our ability to process single application with parallel execution flow but also our ability to execute multiple dynamically arriving applications supporting both task-level and application level parallel execution across heterogeneous set of resources.

II. PROFILE GUIDED PARALLEL PROGRAM GENERATION

A. Overview

The overall flow of the profile guided parallel program generation as illustrated in Figure 1, involves the Preprocessing (Step-1) and Application Data DAG Generation (Step-2) followed by Parallel Code Generation (Step-3). In this design flow, we leverage TraceAtlas [12] for profile-based program analysis and update Compiler Integrated Extensible DSSoC Runtime (CEDR) [13] for runtime task scheduling. TraceAtlas [12] offers flexible interfaces to support dynamic profiling and trace analysis of LLVM IR [14] rapidly with lower resource requirements compared to other frameworks [15]–[17]. We use TraceAtlas to collect memory address ranges accessed by each basic block in the IR along with the runtime control states of those blocks. We then use this information to identify tasks that can be executed in parallel during a task-level memory analysis of the user application. The CEDR ecosystem allows integrating compile-time application analysis with a Linux-based runtime system. We choose CEDR over other runtime frameworks [18]–[24] as it enables compilation and development of user applications for heterogeneous SoCs, evaluating the performance of pre-silicon heterogeneous hardware configurations based on dynamically arriving workload scenarios through distinct plug-and-play integration points in a unified workflow.

B. Program Model

Our system partitions the user application into two types of tasks to represent the execution flow as Type-1 Task and Type-2 Task regions as described below.

1) Type-1 Task: These tasks represent code segments that have low computation complexity, function as auxiliary, and are suitable for executing on the CPU core in a single thread.

2) Type-2 Task: These tasks represent compute-intensive segments of the execution at the task level such as FFT and matrix multiplication. We assume that there is accelerator support for Type-2 Tasks and they can be executed in parallel using multi-threading on CPU or on the accelerator depending on the state of the system resources. Users are required to register Type-2 tasks with C-models and interface functions to invoke the driver of any supported accelerators. Here the C-model is flexible enough that users can either use third-party libraries or just manually implement them.

C. Running Example

We utilize a running example that consists of commonly used program structures with a representative computation task in our problem domain, namely, FFT (Fast Fourier Transform). Figure 2 presents the workings of our tool flow for the user application. Figure 2a is crafted in such a way that it includes features where static analysis is not feasible for detecting data dependence such as the use of pointers for passing variables (lines 2 and 8), function pointers for tasks (lines 6 and 11), different function spaces while calling the tasks (lines 18 and 20), and loop iteration counter that is not known at compile time (line 19). Pre-processing step re-factors the user application through inlining functions dynamically, redirecting function pointers and flattening loops that iterate over Type-2 Tasks. This prepares the application for data DAG generation that captures concurrent execution paths over Type-2 Tasks through dynamic memory analysis followed by control and data flow analysis. Finally refactored code is instrumented with pthread insertion for runtime system to be able to schedule the detected parallel Type-2 Tasks concurrently. In the following subsections, we present the details of our approach by walking through the steps of transforming a user application written in C/C++ into a representation that allows the runtime system to execute tasks without dependencies in parallel.

D. Step 1: Pre-processing

In this step, we implement a profile-guided method to flatten the loops and inline the functions that interface with Type-
2 Tasks. The pre-processing stage parses the user application and automatically instruments it with functions as illustrated in Figure 2b (lines 3, 15, 18 and 20) to be able to trace each Type-2 Task and loop identifier. The instrumented application is compiled and executed to collect profiling data for passing variables and unknown loop iteration count; (b) Instrumented user application for tracing during pre-processing; (c) Flattened user application in Figure 2b (lines 3, 15, 18 and 20) to be able to trace

E. Step 2: Data DAG Generation

Implementation flow for this step is illustrated in Figure 1b where we start with compiling the preprocessed application using Clang to generate the LLVM IR. Recall that a user application is represented with a Control DAG, where each node represents either Type-1 or Type-2 tasks and the edges between the nodes represent the flow of the execution. Here a task can contain multiple basic blocks. We trace basic block control related flags such as BasicBlockEnter, BasicBlockExit along with task control related flags such as TaskEnter and TaskExit using TraceAtlas in Dynamic Profiling stage. We generate the Control DAG structure of the application based on the above four control flags. In our running example, the serial flow of program execution (ReadData(a0), FFT(a0, b0, ...), WriteData(b0), ReadData(a1), FFT(a1, b1, ...), WriteData(b1)) illustrated in Figure 2c corresponds to the Control DAG with six nodes (0 → 1 → 2 → 3 → 4 → 5) shown in Figure 1b. The entry and exit points collected at the task level allow for segmenting the program into Type-1 and Type-2 tasks. Each time TaskEnter or TaskExit is seen, a new node is pushed into the Control DAG, and the basic blocks that appear between TaskEnter and TaskExit are recorded as the basic block elements of the node. The traced memory instructions in TraceAtlas include LoadAddress, StoreAddress, along with a set of LLVM intrinsic memory instructions such as MemCopy, MemSet, and MemMove. The addresses of memory instructions, control flags, and Control DAG are used during Memory Analysis stage to detect data dependencies and expose parallelism among the tasks.

The Memory Analysis parses the Control DAG and uses the trace information collected from TraceAtlas to generate the load/store memory tuple sets for each node. We define a load memory tuple set and a store memory tuple set for each task of the Control DAG to represent the continuously accessed memory space for read and write activities, respectively. Each tuple for a task is composed of start address, end address, number of memory accesses, number of bytes accessed, and task label. The memory tuples are stored in a red-black tree structure with the start address as the key to reducing the indexing time.

The visual representation of memory analysis is shown in Figure 3, where the y-axis shows an index of each node in the Control DAG, x-axis shows the address range accessed (load or store) by each node through labeled rectangles in
a normalized form. For example, node index one is the first FFT task in the user application with 2048 samples and 16,384 bytes of memory footprint starting with the load address range followed by the store address range corresponding to read and write operations respectively. The read after write dependence is identified by checking if the load tuple set of the successor node overlaps with the store tuple set of the predecessor node. A data dependency between predecessor and successor nodes exists only if the predecessor node is the last node to write into the load address space of the successor node. Based on the order of execution, the true dependency is between Nodes 3 and 4 (second FFT task). The second FFT task (Node 4) has a load address space that does not overlap with the store address space of the first FFT task (Node 1). Finally, we implement the LastWriterMap data structure as illustrated in Figure 4 to keep track of the address spaces modified by each node and utilize this representation to identify Type 2 Tasks that can be executed in parallel.

The Data DAG stage in this phase detects Type-2 Tasks that can be executed in parallel and generates the corresponding Data DAG structure, with each edge representing the data dependencies between the tasks.

Figure 4 shows state of the LastWriterMap and Data DAG generation in three steps (t1 to t3) for a simple scenario composed of independent Tasks A and B feeding their data to Task C with a Control DAG of A → B → C. Each time a new node is visited in the Control DAG, its store memory tuple set is written into the LastWriterMap. We overwrite the existing memory tuples and change the pointed value to the new node’s index if the store memory tuple set of the new node overlaps with the store memory tuple set maintained in the current LastWriterMap. At the end of the second step, the Data DAG with two independent nodes are generated as load address space of Task B (B.ld) is not overlapping with the store address space in the LastWriterMap. On the other hand, in step 3, edges from Task A and Task B to Task C are generated due to the load-store overlap between C.ld and store memory tuple in the LastWriterMap that points to both Task A and Task B.

F. Step 3: Parallel Code Generation

We define the group of Type-1 tasks that can be scheduled for execution before a Type-2 task as the Type-1 Region and the group of Type-2 tasks that can be scheduled before a Type-1 task as the Type-2 Region. After identifying the Type-2 tasks that can be executed in parallel, we transform the user application to be represented as a series of code sections composed of Type-1 and Type-2 regions successively in Task
Reordering stage. We implement the Schedule Generation algorithm for this transformation and generate a Schedule DAG that follows the fork-and-join parallel model as illustrated in Figure 5 for our running example shown in Figure 2. The Schedule Generation algorithm is realized through seven steps as illustrated in Figure 6 using Data DAG and Control DAG as its inputs. We define a task as a ready task if all of its parent tasks in the Data DAG have been scheduled. Steps 1-3 generate Schedule DAG for Type-1 Tasks (Nodes 0 and 3) and mark these nodes as visited. Steps 4-6 update Schedule DAG with Type-2 Tasks (Nodes 1 and 4) and mark these nodes as visited. All steps are repeated by visiting Type-1 Tasks followed by visiting Type-2 Tasks that remain in the DAG until all DAG nodes have been visited. While our running example in Figure 2c involves two parallel Type-2 Tasks, the Schedule Generation algorithm implements a generalized solution that is capable of clustering $N$ parallel Type-2 Tasks into a single region to realize $N$-way parallelism.

Referring to the user application shown in Figure 2c, during the application refactoring process of Pthread Insertion, all Type-2 Tasks (FFTs) are swapped with the enqueue kernel as shown in the tool-generated code with Figure 2d. This representation is our interface for the Type-2 tasks to be scheduled by the runtime resource manager. CEDR operates as a background Daemon Process in the Linux user space and applications are submitted through inter-process communication (IPC). The CEDR Management Thread parses the dynamically arriving application binaries and through the enqueue kernel function places Type-2 Tasks, whose dependencies are resolved, into the ready queue. The scheduler makes task-to-PE mapping decisions for those tasks that are in the ready queue. Then CEDR launches a worker thread for each Type-2 Task to execute on the selected PE and monitors the state of execution through PE Tracker.

The trace-based analysis and Data DAG representation enable specifying that the user application in Figure 2c can be refactored from the original structure shown in Figure 7a into Type-1 and Type-2 regions as illustrated in Figure 7b. Along with this transformation, the run time environment needs to know the number of independent Type 2 Tasks grouped together into a single region. For this, during Pthread Insertion stage, code refactoring also involves automatically inserting pthread initialization and conditional wait statements into the transformed application. In this final code representation, two enqueue kernels are placed one after another without barrier synchronization but there is a while loop waiting for those two FFT functions to be completed. At run time, the OS thread initializes the counter value to 0 and waits for the counter to meet the condition. For our running example, the conditional wait value is set to two. We updated CEDR to support the execution of parallel Type-2 Tasks in Type-2 Region. Given that the data initializations are completed by the OS thread, CEDR places both FFTs into the ready queue as there is no barrier between the two FFTs. The scheduler then picks up both FFTs from the ready queue and makes the task to PE mapping decisions. For each FFT, a worker thread is launched and both functions get executed in parallel. Through the PE Tracker, the CEDR management thread monitors the execution of each FFT. As soon as an FFT task gets completed, the CEDR worker thread increments the counter value by one and passes this information back to the OS thread. When the counter reaches to two, the OS thread resumes its Type-1 region possibly to the next phase that needs outputs of the two FFTs. The runtime system supports executing $N$-way parallelism as the counter value is a parameter that is generated during the Pthread Insertion stage.

### III. Experimental Setup

#### A. Applications

For our analysis, we use Pulse Doppler, WiFi-TX, Radar Correlator and Temporal Mitigation as real-world applications from the domain of software defined radio. These applications have varying levels of parallelization and help illustrate the generalizability of our approach.

**Pulse Doppler** determines both the distance of an object and its velocity based on a series of short radar pulses emitted, and the user application observes the shift in the frequencies of the return pulses with respect to the input pulse.

**WiFi TX** implements a WiFi transmit chain, generating a single packet with 64 bits of input data and scrambling, encoding, modulating, followed by forward error correction.

**Radar Correlator** models the use of a radar pulse to determine
distance to an object by looking at the time delay in the received pulse compared to the input pulse. Temporal Interference Mitigation receives a signal consisting of low-energy radar signals combined with high-energy communications data and applies a technique known as successive interference cancellation to cancel out the communications data and extract the radar signals for further processing.

Figure 8 shows the execution phases as a data flow graph (DFG) for each application generated by our tool chain, where a phase is defined as a distinct Type-2 Region. For the sake of simplicity, we show DFG for the 4-Pulse Doppler version which has three execution phases, but in our evaluations, we also use the full scale implementation with 256-Pulses. In Table II we summarize the type of task, the number of execution phases, and the degree of task-level parallelism observed during each execution phase.

B. Evaluation Platforms

For our evaluations, we utilize three diverse platforms, namely, DS3 [11], an event-driven simulator, a homogeneous architecture based on Intel(R) Xeon(R) CPU E5-2650 v3 multicore processor, and Xilinx Zynq Ultrascale+ ZCU102 MPSoC development board.

DS3 simulates the execution of an application represented as a DAG over a user specified heterogeneous SoC configuration where the task to processing element mapping decisions are handled through its built-in Earliest Finish Time (EFT) scheduler. This environment serves as a suitable platform to estimate performance gains of the task-level parallelism extracted through our tool chain.

On the Xeon(R) CPU, each application is processed through our compiler tool chain and then executed through the CEDR environment over 8-cores. This setup allows us to validate the end-to-end integrated compiler and runtime flow over a homogeneous architecture and evaluate the performance gain with respect to serial execution.

The Xilinx Zynq Ultrascale+ ZCU102 MPSoC development board is used to emulate a heterogeneous SoC with 3 ARM CPU cores and 1 FFT accelerator. This setup serves three purposes. First, it allows validating our ability to compile a user application for execution on a heterogeneous SoC. Second, we demonstrate our ability to execute parallel FFT tasks in a single application across a pool of heterogeneous resources concurrently. Third, we demonstrate our ability to manage workload scenarios where multiple independent user applications arrive dynamically and parallel execution at both application and task levels are realized through our integrated compile and runtime flow. To facilitate data transfer to and from accelerators, we use direct memory access (DMA) blocks to move data between the host ARM core and the FFT accelerator via the AXI4-Stream protocol. On the host side, we utilize udmabuf to enable contiguous userspace-accessible buffers for transferring data to and from the hardware accelerators. A user application communicates with the accelerators by writing the data into a udmabuf buffer and a DMA engine is then configured to move data from this buffer into an accelerator for processing. This setup, while allowing experimentation on a heterogeneous hardware configuration, does not offer a realistic SoC representation since we are not emulating a dedicated NoC. Therefore we strictly use it for functional verification purpose rather than conducting realistic performance evaluations.

For the FPGA evaluation we use the Radar Correlator and WiFi-TX. We process them through our compiler tool chain and submit them as single or 100 instance jobs where the CEDR management thread parses application binary, monitors system resources, schedules tasks based on Minimum Execution Time (MET), Round Robin (RR) and Earliest Finish Time (EFT) schedulers. We measure application execution time as the difference between the end of the last task and the start of the first task of an application, including the overhead of all scheduling decisions and data transfers to and from the accelerator in between.

IV. RESULTS AND ANALYSIS

A. Functional Verification and Performance Analysis

Pulse Doppler shows higher degree of parallelism relative to the other applications we use in this study. Therefore, we start with functional verification based on the Pulse Doppler execution through DS3 based simulation over an SoC with 4 and 8 FFT accelerators as shown in Figure 9a and Figure 9b, respectively. Since the 4-pulse version has 8 FFTs during the first stage (Figure 9a), an SoC with 4 FFT accelerators takes two rounds to complete the first stage, whereas on the 8 FFT configuration it takes one round. These two figures together illustrate ability to launch FFT tasks in parallel. Figure 9c shows the 256-Pulse Doppler execution over the 8 FFT SoC configuration where first stage of the execution takes 64 rounds to complete and subsequent two phases take 32 rounds each. Overall, the plots in Figure 9 show that our tool flow is able to extract parallelism in each stage of the execution and distribute the parallel tasks over the available compute resources.

We demonstrate the execution of the real 256-Pulse Doppler implementation that is compiled for execution over the 8-core Xeon processor configuration using Figure 10, where execution of the parallelized application is managed by the CEDR. This plot shows same flow as Figure 9c with three stage execution where first stage takes 64 rounds and subsequent two stages take 32 rounds each. This plot validates the runtime’s ability to distribute FFT tasks as expected. Here we note that the DS3 based execution shows faster execution time than the Xeon processor based execution. There are two key factors to this observation. First the DS3 uses a model based execution where the FFT compute time is based on its actual execution over the Xilinx FFT IP Core synthesized for the ZCU102 FPGA. The compute time for the FFT accelerator is 128 ns whereas the execution time for the FFT task on the Xeon processor is 25,000 ns. Furthermore, overhead associated with the CEDR environment in terms of parsing application binary and dispatching task to the compute resources contribute to the increased overall execution time. Such runtime overhead is not modeled in DS3.
Finally, Table III shows reduction in execution time with respect to the serial single Xeon core-based execution covering the end-to-end execution of the whole application and the time spent only over the FFT or GEMM tasks.

| Application        | Whole Application | Only Tasks |
|--------------------|-------------------|------------|
| Radar Correlator   | 9.6               | 14.8       |
| Pulse Doppler      | 59.0              | 67.3       |
| Temporal Mitigation| 5.9               | 15.8       |
| WiFi-TX            | 17.0              | 21.2       |
| Average            | 22.8              | 29.7       |

Table III: Execution time reduction (%) with respect to the serial single Xeon core-based execution covering the end-to-end execution of the whole application and the time spent only over the FFT or GEMM tasks.

V. CONCLUSIONS

In order to make heterogeneous SoCs accessible, there is the need for integrating the application development, compilation and runtime processes vertically towards a unified ecosystem that enables productive application deployment without requiring users to become hardware experts in the process. Towards this goal, in this study, we present an integrated flow where we expose parallelism in a user application through dynamic profiling and memory analysis, and design a flexible binary structure where an application task can be invoked on any of its supported processing elements in the target SoC. We pass the parallelized binary to the runtime system that enables productive application deployment without requiring users to become hardware experts in the process. Towards this goal, in this study, we present an integrated flow where we expose parallelism in a user application through dynamic profiling and memory analysis, and design a flexible binary structure where an application task can be invoked on any of its supported processing elements in the target SoC.

B. FPGA-based Emulation and Analysis

In Figure 11, we show timing analysis for the Radar Correlator that is refactored into parallel execution form through our compiler tool chain. The three plots illustrate the makespan for completing a workload composed of 100 instances of Radar Correlator executed based on the MET, RR, and EFT schedulers. This experiment shows that making a greedy choice favoring the accelerator (common in hand-crafted code) only results in FFT tasks starving for the accelerator to become available. MET enforces serial execution on the accelerator and also serves as a baseline for total execution time. The RR and EFT schedulers allow for utilizing the parallelism embedded into the application binary, and each one completes the workload in 41.61ms (1.48x faster) and 40.66ms (1.51x faster), respectively.

Figure 12 illustrates the runtime system’s ability to execute FFT tasks from two applications as well as the independent FFTs within an application concurrently. In Figure 12a, we show execution for two instances of Radar Correlator arriving concurrently where a total of four FFT tasks are dispatched to all PEs concurrently. Finally in Figure 12b, we show the PE utilization based on the concurrent execution of WiFi TX and Radar Correlator applications. The EFT in this case favors the FFT accelerator to be used by the WiFi TX as it has higher latency than the Radar Correlator. It splits the use of ARM cores among the two applications and assigns Cores 2 and 3 to WiFi TX after the completion of the Radar Correlator.
the Control DAG for different inputs and setting up a back-up control flow to recover the program execution and resolve unpredictable application behavior.

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