ICSML: Industrial Control Systems Machine Learning inference framework natively executing on IEC 61131-3 languages

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Abstract

Industrial Control Systems (ICS) have played a catalytic role in enabling the 4th Industrial Revolution. ICS devices like Programmable Logic Controllers (PLCs), automate, monitor and control critical processes in industrial, energy and commercial environments. The convergence of traditional Operational Technology (OT) with Information Technology (IT) has opened a new and unique threat landscape. This has inspired defense research that focuses heavily on Machine Learning (ML) based anomaly detection methods that run on external IT hardware which means an increase in costs and the further expansion of the threat landscape. To remove this requirement, we introduce the ICS Machine Learning inference framework (ICSML) which enables the execution of ML models natively on the PLC. ICSML is implemented in IEC 61131-3 code and works around the limitations imposed by the domain-specific languages, providing a complete set of components for the creation of fully fledged ML models in a way similar to established ML frameworks. We then demonstrate a complete end-to-end methodology for creating ICS ML models using an external framework for training and ICSML for the PLC implementation. To evaluate our contributions we run a series of benchmarks studying memory and performance and compare our solution to the TFLite inference framework. Finally, to demonstrate the abilities of ICSML and to verify its non-intrusive nature, we develop and evaluate a case study of a real defense for process aware attacks against a Multi Stage Flash (MSF) desalination plant.

1 Introduction

As a term, Industrial Control Systems (ICS) encompasses all the devices that enable automation of the industrial process, including control systems and their instrumentation, network, and other systems. These ICS devices are frequently utilized in Critical Infrastructure to control critical physical processes. It ensures the smooth and reliable operation of industrial, energy and commercial environments such as assembly lines, water desalination plants, smart energy grids, chemical processing stations, and mining infrastructure. According to a 2021 report by Research and Markets [37], the global market value for Industrial Controls is expected to grow to reach 49.6 billion US dollars by 2025.

With the advent of Industry 4.0, industries have started leveraging Information Technology (IT) devices in the Operational Technology (OT) sector, enabling real-time yield optimization, remote monitoring and control, predictive maintenance, increasing automation, and much more. However, Industry 4.0 has blurred the boundaries between IT and the OT sector, which was once considered secure due to the air-gapped network being now susceptible to network-based remote attacks. For instance, the recent Log4j vulnerability (CVE-2021-44228), considered by many to be a vulnerability impacting the IT domain, has, in fact, even impacted ICS vendors. It has impacted more than 100 products for Siemens, 8 devices for Rockwell such as Plex IIoT and more, the Smart Script labeling software for WAGO, and many other manufacturers [21]. As a result, adversaries can utilize vulnerabilities in the IT infrastructure to propagate onto the OT network and launch attacks on critical infrastructure that can lead to devastating impacts.

With the increase of internet-exposed OT devices and incentives such as rising payouts and a potential for severe damage due to abundant vulnerabilities, OT is becoming an increasingly attractive attack target. According to Packetlabs, globally, a total of 33.8% of ICS computers were attacked in the first half of 2021. Moreover, the vulnerabilities for ICS grew by 41%, with 71% of these vulnerabilities being remotely exploitable compared to the last half of 2020 [31].

There have been many high-profile attacks in the ICS domain: Stuxnet infected over 200,000 computers and...
damaged a significant amount of centrifuges used for uranium enrichment [22]. The Ukraine power grid attack in December 2015, beginning with stolen VPN credentials in which adversaries opened up breakers, took various substations offline, and overwrote legitimate firmware to disable remote commands, leading to a blackout affecting around 230,000 people [6]. Other attacks have been thwarted, for instance, the attack on a water treatment plant in Oldsmar, Florida, where the adversaries attempted to boost the level of sodium hydroxide in the water supply to 100x its regular quantity [5].

Attacks on ICS have been explored in literature, for instance, attacking the Programmable Logic Controller (PLC) to change the control logic or its parameters process [19] [25] [17], modifying the firmware [11] or the sensors with false data injection (FDI) attacks that gather and relay data to the PLC [24] [28] [9] [34] for attacking the controlled physical process. Proactively uncovering vulnerabilities in PLC programming [40] and detecting the presence of malware [35] are also topics of interest to the ICS community. Defenses for attacks on ICS hardware have also been studied extensively, among others these include protecting the PLC using control invariants (correlation between sensor readings and PLC commands) [44], extracting control logic rules [16] and detecting safety violations [26]. Similarly, Machine Learning-based (ML) solutions [20] [4] [27] [30] [43] have been employed for detecting FDI attacks.

However, these ML-based solutions for detecting FDI attacks are often built with high level languages such as Python [42], and can only be executed on PLCs that employ an operating system (OS) supporting the execution of general-purpose binaries. Many of these PLCs are bare-metal or utilize proprietary OS, forbidding such operations. Furthermore, these solutions operate out-of-the-device either in online or offline data collection mode. Therefore, such approaches cannot be realistically deployed because they require an additional device for each PID loop running the ML-based solution with the sensor inputs. Fig. 1a shows the current (proposed) state-of-the-art: Any ML-based solution has to receive the process inputs (typically analog) separately from the PLC, perform inference and potentially detect an anomaly. This external device (typically a regular computer) needs to connect to the OT network to transmit its inference outcome. Apparently, a traditional IT device in the OT network can expand the attack surface and damage capabilities.

In order to remove the requirement of including and integrating a regular computer for ML-based security defenses, in this work we present ICSML, an ML inference framework implemented natively in Structured Text (ST), thus compatible with all IEC 61131-3 languages. Since the framework is built in ST, it integrates with any IEC project and enables on-the-device implementation of ML-based defenses. Such a solution can work on the PLC without requiring additional external devices and remains tightly coupled with the sensor inputs relayed to the PLC. ICSML, displayed in Fig. 1b, allows inference within the PLC without 1) sacrificing inference accuracy, and 2) affecting the PLC regular operation. Our contributions can be summarized as follows:

- We formulate the problem of efficiently performing inference on PLCs using IEC 61131-3 languages by studying the expressivity limitations of the available languages, taking into consideration PLC hardware limitations and factoring in the real time constraints imposed by ICS operation environments.
- We develop a Machine Learning inference framework that works around the IEC 61131-3 domain-specific language limitations and offers a complete set of Machine Learning components to the ML process engineer for building and running ML models directly on the PLC.
- We present an end-to-end methodology for performing ML inference on PLCs that includes dataset formation, model building and training on established Machine Learning frameworks (e.g: TensorFlow, Pytorch etc.), model porting to ICSML and execution on the PLC.
- We evaluate the performance of the ICSML framework through a series of benchmarks that highlight memory requirements and performance scaling with respect to model size.
- We demonstrate the usefulness and ability of the framework via a case study that implements a real on-PLC defense for a Multi Stage Flash (MSF) desalination plant. We also use the case study to show that ML models built on ICSML hold the property of non-intrusiveness with respect to the primary tasks of the PLCs that they run on.

2 Preliminaries

2.1 Industrial Control Systems

Architecture. An ICS encompasses control systems and associated instrumentation that monitor, manage, control, and automate physical industrial processes, often employed in critical infrastructure. The typical architecture of an ICS consists of three layers:

1. Field Instrument Control Layer. It consists of sensors and actuators that implement input/output to the process control layer.
2. **Process Control Layer.** It consists of control systems that control real-time processes responsible for regulating a physical industrial process. These devices sample sensor reading and operate actuators based on the implemented control logic based on the scan cycle.

3. **Supervisory Control Layer.** This layer provides monitoring and control capabilities for the devices in the control layer. For instance, the IDE for programming and debugging the control application or the Human-Machine Interface (HMI) monitoring the currently executing process.

According to the nature of the processes they control, ICS configurations can be categorized into Distributed Control Systems (DCS), where the system is decentralized, and each subsystem independently controls a part of the overall control process. Next, the Supervisory Control and Data Acquisition (SCADA) topologies, where the system relies on a central node that collects data and controls all subsystems. ICS systems of both configurations rely on PLCs: integrated devices with ruggedized packaging designed for reliable operation in harsh industrial environments. PLCs work under a cyclical model of operation in which they read sensor inputs, perform computations based on the control logic, and regulate the actuators. Programming the control logic of PLC devices is done by process engineers using a family of domain-specific programming languages defined by the IEC 61131-3 standard [4].

### 2.2 IEC 61131-3 Languages

IEC 61131-3 is a programming standard in the automation industry with support for various programming languages [36]:

1. **Ladder Diagram (LD).** It is a low-level graphical language representing a ladder-like structure, consisting of vertical lines the rails, connected by horizontal circuits. Here, input and outputs are represented by contact and coil symbols, respectively. LD is more suitable for maintenance technicians lacking familiarity with programming languages.

2. **Function Block Diagram (FBD).** A graphical language consisting of function blocks, written any IEC 61131-3 language, connected by horizontal lines known as the signal flow lines.

3. **Sequential Function Chart (SFC).** It is a high-level graphical language specifying sequential behavior capable of integrating with other IEC languages. Rectangular blocks specify the phases of the control process and connect through flow lines.

4. **Structured Text (ST).** A high-level textual language that looks similar to C. It allows complex functionalities to meet the growing sophistication of PLCs. Each program incorporates a network of functions (subprogram without internal memory) and function blocks (segments of reusable code with internal memory). These software blocks are called Program Organization Units (POU) that make up the PLC project.

### 3 Problem Formulation

In this work we aim to explore the ability of PLCs to efficiently perform inference using IEC 61131-3 languages, in order to reap the benefits of ML inference natively on the PLC. ML inference natively in the PLC is challenging, since:

1. PLC applications are coded using limited expressivity domain-specific programming languages that are compiled to non-standard binaries. These languages have limitations (e.g. no dynamic memory management, recursion is not supported, etc.) that require novel approaches to properly support ML inference. This is discussed in Section 5.1.
2. PLCs come at a variety of computational capability configurations, with the majority incorporating limited amount of memory and embedded microprocessors, as further elaborated in Section 3.2. Therefore, developed methods have to both be lightweight and not interfere with the primary computational objective of the PLC.

3. Industrial processes typically have real-time requirements, with the scan cycle (sense-compute-actuate loop) potentially having periods in the order of milliseconds. Therefore, inference has to be carefully developed with respect to the scan cycle, as further discussed in Section 3.3.

3.1 IEC 61131-3 Languages Limitations

Implementing ICS machine learning solutions and all related functionality in the PLC vendor stack using IEC 61131-3 languages brings forward challenges that stem from the limitations of the chosen language. Initially, Structured Text (ST) seems to be by far the most well suited language to be used for developing Machine Learning applications as it resembles traditional imperative programming languages and looks like the most versatile of the languages defined in the IEC 61131-3 standard. However, in theory, all IEC 61131-3 languages examined in Section 2.2 are interchangeable and as such the use of ST for analysis can be done without loss of generality. Being a domain specific language, ST features a number of nuances and limitations that must be kept under consideration during the development of an ML application. Some important limitations are the following:

**Lack of Dynamic Memory Management:** ST, like the rest of IEC 61131-3 languages, lacks the ability to dynamically manage memory during run time. Among other things, this prevents the allocation of variable length arrays and requires that the programmer manually precomputes all array sizes or statically preallocates large memory scratch pads. To understand the amount of manual memory allocation required when creating a densely connected neural network in ST, consider that each dense layer requires memory buffers for its weights, biases and outputs. Thus, even a simple 3-layer dense NN requires manually precomputing the dimensions of and statically preallocating 9 memory areas.

Beyond simple model instantiation, the lack of dynamic memory management and the ability to dynamically allocate temporary memory in a function call can also hinder the efficient implementation of algorithms desired in a Machine Learning context (e.g: Convolution algorithms, BLAS operations, Divide and Conquer style algorithms, the Strassen algorithm etc.).

**Inputs are “Call-by-Value”:** Inputs to POUs defined under VAR_INPUT are passed by value to the called function, meaning copies of the input data are automatically created specifically for every POU call. In the context of an ICS Machine Learning application where multiplying large matrices might be done on memory limited hardware, programming with side effects and avoiding unnecessary data duplication is key to reducing the memory footprint of the application. To illustrate the need for working around call-by-value POU calls, consider the example of multiplying an input vector of 512 LREAL numbers (64-bit precision floating point numbers) with a 512x512 LREAL weights matrix. This vector and matrix require a combined total of 512 * 8 bytes + 512 * 512 * 8 bytes ≈ 2 MB of memory. Making a function call to a call-by-value vector-matrix multiplication function would mean that the amount of allocated memory would be doubled to reach 4 MB. While this might seem like a small number, it is an important percentage of available memory for PLCs like the Festo CECC-D that is equipped with just 16 MB of RAM.

**Functions cannot call Function Blocks:** ST allows passing Function Blocks as arguments to Functions but this is only for the purpose of accessing them as data structures and not calling their methods. This prevents certain simple ML routines from being implemented. For example, consider an environment where Neural Network layers like those found in Keras [7] are represented by Function Blocks that encapsulate data and functionality. Performing inference could be as simple as implementing a generic stateless inference function that is passed an ordered array of FBs which are then evaluated in the function’s body as illustrated in the following code example. However due to Functions not being able to call FBs, this is not possible since Inference_Function(), a Function, cannot call the evaluate() FB method.

```
PROGRAM Main_Program
Model: ARRAY[0..2] OF Layers := [input, dense_1, dense_2];
Inference_Function(Model);

FUNCTION Inference_Function
FOR index:=0 TO UPPER_BOUND(Model_Arg, 1) DO
    Model_Arg[index].evaluate();
END_FOR
```

Listing 1: Example ST program that cannot be compiled due to Functions not being able to call Function Blocks.

**No Recursion:** Recursive calls of POUs, direct or indirect, in IEC 61131-3 languages is strictly forbidden. This limitation expands on instances of Function Blocks of the same type calling each other. Consequently it is hard to implement a layer based Machine Learning application in a way that ML model layers directly link to each other through layer references or chained function calls during inference. While there exist workarounds to bypass static
compiler checks, these cause crashes during runtime. To illustrate this, consider the following code example, that cannot be compiled, in which layer_2’s evaluate() is not allowed to recursively call layer_1’s evaluate() for inference because they are of the same type:

```plaintext
input_layer : Input := (size:=32);
layer_1 : Dense := (input:=input_layer, neurons=128);
layer_2 : Dense := (input:=layer_1, neurons=256);
inference_result := layer_2.evaluate();
```

Listing 2: Example of Linked Layers model that is infeasible due to the Recursion limitation in ST.

**No First-Class Functions:** Functions in ST are not considered first-class citizens and as such cannot be passed as arguments to POU’s. This limitation prevents the employment of functional programming paradigms when programming in ST. For example, under this restriction, it is impossible to precisely reimplement one of Keras’ Core Layers, the Lambda Layer, which expects a lambda expression as an argument and enables the hassle free implementation of custom activation functions and even arbitrary expressions as Layers. As such, even simple functional programming concepts cannot be implemented as Functions in ST. To illustrate this, consider the following code example where Map, a Function that performs mapping, cannot be implemented in ST because ST does not support passing Square Function(), a Function, as an argument to Map.

```plaintext
squared_integers_array := Map(integers_array, ADR(Square_Function));
```

Listing 3: Mapping Function Example that is infeasible because ST does not support passing Functions as arguments to other Functions.

### 3.2 PLC Hardware Limitations

Given that PLCs are often deployed in interconnected harsh industrial environments, their design usually prioritizes robustness, efficiency, connectivity and ruggedness over the inclusion of high performance computational hardware.

As can be seen in Table 1 computationally entry-level PLCs like Allen Bradley’s Micro 810, use low power CPUs and feature a fairly limited amount of memory (just 2 KB). On the other hand, mid-tier performance-wise PLCs, like the Schneider Electric Modicon M241, come equipped with faster multi-core processors and upgraded RAM around 64 MB. Finally, on the higher end of the performance spectrum, sit PLCs like WAGO’s PFC 200 which houses ARM’s Cortex A8 CPU clocked at 1GHz paired with 512 MB of RAM.

Considering the limited resources available on PLCs, ICS Machine Learning applications must be coded in a way that makes efficient use of I/O, CPU time and memory so as to seamlessly operate and achieve the desired performance metrics without resource starving other ICS tasks running on the PLC.

### 3.3 Real Time Constraints

ICS processes typically involve tasks that run in a cyclical fashion, such as PID feedback loops. As such, PLCs are designed to operate by following a periodic model that is based on the scan-cycle sequence. At the beginning of the scan cycle the PLC captures the values from its inputs, that are usually sensor readings, and loads them into memory for computations to take place. After the PLC executes the instruction sequence that it was programmed to do using IEC 61131-3 languages. Finally, based on the results of the previous step, the PLC’s outputs are updated. These outputs can be used for purposes like actuator activation and control, data collection etc.

The desired length of the scan cycle can vary depending on the ICS environment. For example PLCs used to control robots in industrial manufacturing might be required to respond within microseconds, especially when human safety is involved. On the other hand, slower petrochemical processes can even be controlled using second-long PLC scan cycles.

The number of calculations that can be made within a single PLC scan cycle is limited by the length of the scan cycle and the computational power of the PLC being used. Violation of ICS process real-time constraints, as set by the PLC scan cycle, can prove to have disastrous ramifications.

### 4 ICSML Framework

ICSML is a Machine Learning Inference Framework for ICS environments. It is built using Structured Text and is compatible with all IEC 61131-3 standard languages. Its goal is to provide the ML application engineer with a code base and structured approach for effortlessly building and deploying cross-compatible, real-time, and efficient ML solutions on PLC hardware.

This section presents an overview of the framework’s design, structure, and usage workflow. Initially, various design challenges, including the limitations outlined in Section 3.1 are examined and addressed through the framework design process. Then, the framework structural hierarchy and its components are presented. Finally, a complete end-to-end high level methodology for developing and deploying Machine Learning applications on PLCs using ICSML is discussed.
OUT, which would pass variables.

No Recursion: If ST supported recursion, ICSML could directly in the body of the PLC Program POU. Alternatively, the programmer can define a scheduler array of Layer type FBs for evaluation during inference.

of a Model Function Block which is passed an ordered as stateless Functions. To overcome this, ICSML Mction does not allow defining inference layer schedulers with side effects can take place on the data directly. However this approach has the important limitation of not being able to access these variables using the Function Block dot accessor.

Functions cannot call Function Blocks: This limitation does not allow defining inference layer schedulers as stateless Functions. To overcome this, ICSML Machine Learning Model schedulers are integrated as part of a Model Function Block which is passed an ordered array of Layer type FBs for evaluation during inference. Alternatively, the programmer can define a scheduler directly in the body of the PLC Program POU.

No Recursion: If ST supported recursion, ICSML could be built in a way where Layers were directly linked to each other through Function Block references and inference worked using backwards recursive calls to previous Layers. The solution to this limitation is the same one employed for the above limitation: ICSML represents ML Models using a FB which contains an array of ordered Layers to be evaluated by an integrated scheduler function.

No First-Class Functions: The ability to pass Functions as arguments would have allowed the easier implementation of functionality equivalent to Keras’ Lambda layer or mapping and reduction operations. While this cannot be done using Functions in ST, this style of programming can be emulated using Function Blocks if they are to be considered as closures. However, this emulation tactic provides no real benefit for the development of ICSML. To illustrate this consider the example of activation functions. Closure support by the language would have allowed passing an activation function as an argument directly to the Dense Layer. To work around ST’s limitations, the Function would have to be wrapped as a stateful Function Block which would then be passed to the Dense Layer Function Block. But at this point the amount of additional code and programming effort is the same as implementing the function as a Layer Function Block, with the additional confusion of the existence of an Activation Function Interface. Instead of employing this emulation tactic, ICSML provides the programmer with ST Interfaces for implementing custom functionality as dedicated Layers.

External Libraries: Another design dilemma that needs to be addressed when designing an ICS Machine Learning framework is the use of external libraries versus the implementation of their functionality as part of the framework. For example Machine Learning frameworks rely extensively on computationally intense mathematical calculations like matrix multiplication. Many PLC manufacturers provide optimized libraries for their

Table 1: PLC hardware specifications grouped by manufacturer. Time per instruction is measured by manufacturers for Steps, which differ in definition by manufacturer to manufacturer.

| Manufacturer | Models | Average Time/Instruction (µs) | Memory / RAM |
|--------------|--------|------------------------------|--------------|
| Allen Bradley | Micro | 2.5/0.3/0.3/0.3/0.3 | 128-512KB/512KB/1MB/2-4MB/16MB/256KB-1MB/128-512KB |
| Eaton | XCI152, XC300 | 1.6, 0.02 LD | N/A, 2/20/20/40KB, 600KB-10MB, 3/40/32/32/32MB |
| Emerson | Micro CPU/E5001, RX3i CPE400/CPL410 | 0.8 Bool/1.8, N/A | N/A, 123KB-4MB |
| Fatek | B1, B1r | 0.33, 0.33 | 64/34KB, 64/2MB |
| Festo | CEC-D3/RS | N/A | N/A, 512MB |
| Fuji Electric | SP/H00/IH/HIV3/300/300/200/200 | FP: 0.025/0.066/0.08/0.08/0.08/0.08/0.08/0.27/5600 | 4/4/2/2MB/128KB |
| Hitachi | Micro EH++,HX,EHVP+ | N/A, 0.006 FP, 0.08 | 1MB, 16MB, 2MB |
| Honeywell | ControlLogix 1786 PLC | N/A | 256MB ECC |
| Mitsubishi Electric | MELSEC IQ-RQ/LQ | 0.0098 FP/0.0016 LD/0.0065 LD | 4MB/64-896KB/64KB Steps |
| Panasonic | FP/7/8/9/10/11/12/13 | 0.011/0.030/0.05/0.08-0.08/0.08/0.08/0.08/0.08 | 1MB/20KB/64KB/16KB/64KB Steps |
| Rexroth (Bosch) | XM21/22/42, VPB | FP/0.026/0.01/0.02/0.02 | 0.5/5/2/10GB |
| Schneider Electric | MDS/21/21/24/25/26 | 0.3/0.3/0.029/0.028/0.028/0.028 | 256KB/64/4MB/4MB/32MB |
| Siemens | SIMATIC S7-1200/1500 | 2.3/0.006-0.384 | 150KB/150KB-4MB |
| WAGO | PFC100/200 | N/A, N/A | 256/512MB |

4.1 IEC 61131-3 Expressivity Challenges

Designing a ML inference framework that runs inside the vendor software stack requires using IEC 61131-3 languages. As such the design process involves making choices that address and work around the various limitations imposed by the use of the language. ICSML addresses these as follows:

Lack of Dynamic Memory Management: ICSML overcomes this limitation by using statically preallocated memory. The proposed methodology for using ICSML involves declaring layer sizes via constants and using them to precompute the size of the memory areas that are to be statically preallocated. Memory spaces are then associated with metadata regarding their size and data dimensions through specially defined data structures (dataMems) which are used internally by ICSML.

Inputs are “Call-by-Value”: The framework works around the potential memory duplication issue caused by declaring POUs argument variables as VAR_INPUT, by using the dataMem structure to pass arrays as arguments to POUs. The dataMem structure contains a pointer to the memory space and related metadata. This way operations with side effects can take place on the data directly. An alternative to this approach would be to declare arguments under VAR_IN_OUT, which would pass variables by reference. However this approach has the important limitation of not being able to access these variables using the Function Block dot accessor.

Datasets and Batch Processing: In ML frameworks, working with batches is critical. However, ST does not support arrays, so the only way to handle this is by hardcoding the batch size in the code. This is a limitation that needs to be addressed in future versions of ST.

Limited Recursion: ST does not support recursive functions, which can be a limitation when implementing certain types of algorithms, such as depth-first search. ICSML addresses this limitation by using external libraries to implement recursive functions.

No First-Class Functions: The ability to pass Functions as arguments would have allowed the easier implementation of functionality equivalent to Keras’ Lambda layer or mapping and reduction operations. While this cannot be done using Functions in ST, this style of programming can be emulated using Function Blocks if they are to be considered as closures. However, this emulation tactic provides no real benefit for the development of ICSML. To illustrate this consider the example of activation functions. Closure support by the language would have allowed passing an activation function as an argument directly to the Dense Layer. To work around ST’s limitations, the Function would have to be wrapped as a stateful Function Block which would then be passed to the Dense Layer Function Block. But at this point the amount of additional code and programming effort is the same as implementing the function as a Layer Function Block, with the additional confusion of the existence of an Activation Function Interface. Instead of employing this emulation tactic, ICSML provides the programmer with ST Interfaces for implementing custom functionality as dedicated Layers.

External Libraries: Another design dilemma that needs to be addressed when designing an ICS Machine Learning framework is the use of external libraries versus the implementation of their functionality as part of the framework. For example Machine Learning frameworks rely extensively on computationally intense mathematical calculations like matrix multiplication. Many PLC manufacturers provide optimized libraries for their...
icsml components

f(x)

activation functions

layers & data structures

math & utility functions

models

f(x)

• ... tanh

• dataMem

• input

• dense

• concatenation

• activation

• sequential

• binarr

• arribin

• dot product

4.2 framework architecture

As shown in figure 2, architecturally icsml is comprised of activation functions, math and utility functions, data structures, layers and models. These components have been modeled in a way similar to that encountered in popular machine learning frameworks to ensure compatibility and enable users to easily port their models to icsml.

activation functions: one of the fundamental components of an artificial neural network (ann) neuron is its activation function which is applied to the weighted sum of the neuron’s inputs to calculate the output. Activation functions are used to introduce non-linearity that enables ANNs to achieve more complicated goals using fewer neurons. ICSML provides parameterizable implementations for the binary step, exponential linear unit, rectified linear unit (relu), leaky relu, sigmoid, softmax, swish and hyperbolic tangent (tanh) activation functions.

math & utility functions: during machine learning inference, weighted sums of neuron inputs are calculated. These calculations are essentially matrix and vector multiplications that rely on the dot product operation which is implemented as a function in icsml. Beyond this, ICSML provides utility functions binarr and arribin that provide abstractions to load and save array data from and to binary files. Among other things, these can be used to form datasets, load network weights and biases and log inference results.

layers & data structures: like in other ML frameworks, layers are the fundamental building blocks of ML models in icsml. Each layer type offers its own unique functionality. Dense layers feature a number of neurons and their corresponding weights and biases that are used to calculate the layer’s outputs. Concatenation layers combine the outputs of their inputs and can be used to build ML models with parallel sections that branch out and merge. Activation layers apply an activation function to their inputs. As also mentioned earlier, as a means to work around the lack of dynamic memory management, and to offer a convenient way to manage layer memory, ICSML provides the user with the dataMem structure which associates memory areas with their metadata.

models: following the example set by other frameworks, ML models in icsml are built by wiring together layers. ICSML models contain an array of layers and a evaluation function that is called to perform inference. For building traditional densely connected feedforward ANNs, ICSML offers the sequential model, however using icsml to build more sophisticated models like Recurrent Neural Networks is also possible.
4.3 Methodology for Porting a ML Model to ICSML

The ICSML framework was designed to enable Machine Learning application engineers to effortlessly design and train their models on popular ML frameworks and run them on ICS platforms. This section discusses the steps involved in building and porting a Machine Learning model to ICSML. An overview of the process is depicted in Figure 3.

Data collection is an important step in creating ICS ML models, as the quality of the formed dataset directly impacts the quality of the end model. Data collection can be done by recording the PLC’s inputs using an external setup with an ADC, however, it is recommended that it is done directly on the PLC in order to account for potential effects from the integrated ADC (e.g: quantization noise and accuracy) and to ensure that the collected samples are as true as possible to what is encountered by the PLC. ICSML provides the ARRBIN abstraction function that allows recording PLC inputs to binary files.

```
ICSML.ARRBIN('PLC_Inputs.bin', Inputs_size * SIZEOF (REAL), ADR (Inputs));
```

Designing the model’s architecture and training can be done using established high-level ML frameworks like TensorFlow [1], Pytorch [33] and Caffe [13]. Designing, training and exporting the ML model with the purpose of then porting it to ICSML do not differ from standard procedure.

Weights and biases extraction from the exported ML model is necessary for reconstruction of the trained model in ICSML. During this step the exported model file is read and its weights and biases are saved into binary files which are then loaded onto the PLC.

Given the knowledge of the trained model’s architecture and its extracted weights and biases, the model can be reconstructed in ICSML. Reconstruction is done in a structured approach in which first layer sizes are defined as constant variables.

```
L1_size := UINT := 512;
```

Then, arrays for weights, biases, output memory buffers and dimensions of each layer are defined as variables.

```
L1_weights : ARRAY[0.. L1_size * input_size -1] OF REAL;
L1_biases : ARRAY[0.. L1_size -1] OF REAL;
L1_buff : ARRAY[0.. L1_size -1] OF REAL;
L1_dimensions : ARRAY[0..0 ] OF UINT := [ L1_size];
```

After, memory buffers and size metadata are used to construct each layer’s dataMem structures.

```
L1_dataMem : ICSML.dataMem := (address:=ADR( L1_buff), length:=L1_size, dimensions:= ADR(L1_dimensions), dimensions_num:=1);
```

Subsequently, Layers are instantiated and placed into an array which is used to construct the Model.

```
L1_layer : ICSML.Dense := (input:=input_layer output, output:=L1_dataMem , weights:= ADR(L1_weights), biases:=ADR(L1_biases),
activation:=ICSML.activationType.ReLU);
Model : ICSML.Sequential := (layers:=L1_layer, layers_num:=UPPER_BOUND(layers_array, 1)+1);
```

Finally, in the dynamic part of the code, weights and biases are loaded using BINARR and the Model is ready to be used for inference.

```
ICSML.BINARR('L1_biases.bin', L1_size * SIZEOF(REAL), ADR(L1_biases));
Model.evaluate();
```

For a full example of a model ported to ICSML, refer to the MNIST classification model in Appendix A.

5 Benchmarking

Performance and efficiency are key for running ML applications on PLCs since they are devices with limited memory and CPU resources that are bound by real-time constraints. To better understand the proposed framework’s performance when deployed on PLC hardware, the Codesys Profiler is used with a Wago PFC100 (600MHz ARM Cortex-A8, 256MB RAM) and a BeagleBone Black (1GHz ARM Cortex-A8, 512MB RAM) configured to run the Codesys Runtime. To investigate the framework’s scalability, various configurations of ICSML components and their memory usage and CPU time are studied. To draw comparison with a state-of-the-art solution running outside the vendor stack, TensorFlow Lite is considered running on a Raspberry Pi 2 (900 MHz ARM Cortex-A7, 1GB RAM).

5.1 Memory Limitations

To study the memory limitations that PLC ML applications face, a test ICSML application is instantiated with various configurations for the Model and its Layers. Using the Codesys Memory Tools, a linear relation is observed between Layer sizes and memory usage since each Layer on the PLC occupies memory equal to the sum of its weights matrix, biases vector and output memory buffer. To put the size of PLC memory into perspective with the size of ML models in number of parameters and size occupied on disk, consider Figure 4. The figure places popular Deep Learning models from the Keras Application library next to various PLCs according to model size and memory availability respectively. As can be observed from Table 1, PLCs typically come with limited size memory, making it imperative that ML models deployed on ICS hardware use memory efficiently.
Figure 4: Deep Learning models from the Keras Application library with respect to their size on disk in megabytes and number of parameters in millions. The memory of various PLCs is noted in green. Acronyms used: DN - DenseNet, EN - EfficientNet, MN - MobileNet, NN - NASNet, RN - ResNet.

5.2 Layer Stacking Scaling

To study the performance implications of adding additional Dense layers to an ICSML model, a dense model with a 64 feature input vector is used. The Input layer performs a simple copy operation and its evaluation function takes 3µs to return. Loading and storing the input and output vectors (64 32-bit floating point numbers) is done using the BINARR and ARRBIN functions which take approximately 396µs and 530µs of CPU time per call respectively. The Dense layers used in the model have 64 neurons and use a ReLU activation function. Initially a single Dense layer is instantiated, and in every iteration of the experiment an additional layer is added to the model.

As can be observed by the results presented in Figure CPU time for the Dot Product operation, Activation Function application and the model as a whole, scales linearly. In the case of the BeagleBone Black, each additional layer in the test model adds approximately 455.186µs, 181.81µs and 741.863µs to each of the aforementioned execution times respectively, while for the Wago PFC100 these numbers increase to 696.435µs, 248.347µs and 1093.565µs.

Comparing the total inference time of the ICSML benchmark model to that of an equivalent model running on the Raspberry Pi 2 with the TensorFlow Lite inference framework, shows that inference in TFLite is on average 29.99x and 45.67x faster than inference using ICSML running on the BeagleBone Black and the Wago PFC100 respectively.

Figure 5: Scaling of Activation Function, Dot Product and model inference CPU times with respect to the number of the model’s layers on a WAGO PFC100 and a BeagleBone Black running ICSML and a Raspberry Pi 2 running TensorFlow Lite.

5.3 Layer Size Scaling

To gain an understanding of how the width of a layer impacts the performance of an ICSML model, a simple model is instantiated with an Input layer for 32 features and a single Dense layer that also applies the ReLU activation function. On each iteration of the experiment, the number of neurons of the Dense layer is doubled. From the results in Figure CPU time for the Dot Product operation, Activation Function application and the model as a whole scales almost linearly with respect to the number of neurons. On average, a single neuron adds approximately 9.3256µs to
Figure 6: Scaling of Activation Function, Dot Product and model inference CPU times with respect to the number of the size of the model’s layer on a WAGO PFC100 and a BeagleBone Black running ICSML and a Raspberry Pi 2 running TensorFlow Lite.

Figure 7: Experimental setup for detecting false data injection attacks in MSF desalination plant HITL model.

the total model inference time on the BeagleBone Black and 13.722µs on the Wago PFC100. Comparison of execution time between an equivalent benchmarking model and the ICSML model running on the BeagleBone Black and the Wago PFC100, shows that TFLite is faster by 23.87x and 35.29x respectively.

6 Case Study

This section presents a real on-PLC Machine Learning application that was built using ICSML. The case study implements an ML-based defense mechanism against Process Aware Cyber Attacks targeting a Multi Stage Flash (MSF) Desalination process.

MSF Desalination is a widely used process that converts high salinity sea water into potable water. As shown in Figure 8, a typical MSF plant is composed by three sections: a Heat Rejection section, a Heat Recovery section and a Heating section. As Seawater intake passes through the Heat Rejection section, its temperature increases due to latent heat brought in by the brine flowing in from the Heat Recovery Stage. The intake is then mixed into a pool from which a Recycle Brine flow leaves and goes through the Heat Recovery section. In the Heat Recovery section the Recycle Brine flow temperature is further increased through the absorption of latent heat from the vapors in the flashing chamber. The Heating Section further heats the brine flow creating the vapors which are released into the flashing chamber. Through heat recovery these flashed vapors form the distillate product which is then collected by special distillate trays.

A Process Aware attack on the MSF Desalination plant assumes that the attacker has compromised the plant ICS system and has knowledge of the process which can be exploited to inflict damages. Such attacks usually aim to cause mechanical failures or inflict financial losses to plant operators. They can be carried out by intelligently manipulating sensor readings, directly controlling actuators (e.g: valves) or even by modifying the PID parameters of the controllers that govern the operation of the desalination process.

Such attacks directly impact the controlled process and as such can be detected by observing variables associated with the ICS system state. These variables are also used by PLCs to control the dynamic process and include sensor readings and actuator states. As such it is possible to formulate process aware attack detection as an anomaly detection problem that can be solved by employing Machine Learning methods running directly on PLC hardware.

Since experimenting on an active MSF Desalination plant is not a feasible solution, a simulated model validated against real data from Saudi Arabia’s Khubar II MSF and used to research Process Aware attacks on MSF plants is used. For added realism the model is expanded to include a Hardware-In-The-Loop (HITL) setup so that the core process is simulated using MATLAB Simulink, but the controller regulating the Steam
Flow Rate (Ws) is implemented on actual PLC hardware. As illustrated in Figure [7] in this setup the PLC interfaces with the rest of the simulation by receiving Initial Brine Temperature (TB0) and Distillate Product Flow Rate (Wd) as inputs and outputs the Steam Flow Rate control signal which is calculated by a cascading PID setup.

Using the simulated setup, a dataset is built that includes data collected under normal plant operation conditions and under a series of various simulated attacks that have been shown to inflic palpable damages [4]. The dataset contains about 22 hours and 45 minutes of MSF plant operation data, out of which about 11 hours and 6 minutes are data collected under 7 different process aware attacks each aiming to influence different performance metrics. Data points are collected at a 100ms interval to match the PLC’s scan cycle and contain measurements for TB0 and Wd that are observed by the PLC during operation, along with a label for the attack.

For defending against process aware attacks, the PLC is considered to have access to windows of ordered TB0 and Wd readings from the past 20 seconds. Given that the PLC scan cycle is 100ms, a Densely connected classifier with 400 inputs (= 2 feature readings · 10 readings per second · 20 seconds) is designed. The dataset is split into three subsets for Training (72.25%), Validation (12.75%) and Testing (15%). The model consists of 4 hidden layers with 64, 32, 16 and 2 units, the first three of which use the ReLU activation function. The model is instantiated and trained in TensorFlow Keras using Sparse Categorical Cross Entropy as the Loss Function and Adam as the Optimizer with the Learning Rate parameter set to 0.00001. During training the checkpoint weight saving mechanism is used so that the top model’s weights are saved on every epoch that overall Validation Accuracy is increased. The maximum number of training epochs is set to 600 and early stopping is configured to 64 epoch patience. The final model is trained for 175 epochs. The trained model’s point classification accuracy on whether an attack is underway or not, is 93.68%.

Finally, the model’s weights and biases are extracted and the model is ported to ICSML using the methodology demonstrated in Section 4.3. The PLC is then placed again into the HITL setup for testing.

As shown in Figure [9] a series of attacks is simulated using previously unseen attack parameters to test the effectiveness of the ICSML model running on the PLC. The continuous light blue line shows the Wd and TB0 inputs to the PLC as recorded by Simulink, while the plotted points show the same inputs as recorded by the PLC. These points are colored according to their classification as benign samples or attacked. As can be understood by studying the figure, due to the defense model employing a sliding window strategy response might be slightly delayed in recognising an attack.

A desired property for the defense model to have is that of non-intrusiveness, i.e executing the ML model on the PLC should not in any way affect the outcome of the primary task. To show that the ICSML defense model does not interfere with the output of the cascading PID controller setup running on the PLC, the PLC’s inputs and outputs are recorded in controlled condition scenarios without the defense running on the PLC and with it enabled. By analyzing the recorded input and output data, like that shown in Figure [10] and Figure [11] it can be understood that the execution of the ICSML model does not affect the output of the cascading PID controllers. The variation between the compared data can be attributed to the artificial additive noise included in the simulation for added realism and to the noise introduced by the use of the HITL setup.

7 Discussion & Future Work

7.1 Performance

As expected, and as shown through the series of performed benchmarks in Section 5, ICSML performance and memory requirements scale linearly with the size of the ML model. The ability of a specific ML model to be deployed on a specific PLC in an ICS environment depends on the required memory by the model and the
one offered by the PLC. It also depends on the architecture of the model, the processing power of the PLC and the nature of the controlled process, since the PLC has to operate within the real-time restrictions imposed by the scan cycle selected for the governing the given ICS process.

Through the MSF Desalination case study it was demonstrated that running an ICSML model on the PLC does not interfere with the primary task of the PLC. Additionally, using a series of tests it was shown that there was no unintended loss in accuracy by performing inference on the PLC as compared to running the same model on traditional IT hardware. These observations are of great importance since errors or failures in ICS can have catastrophic consequences including environmental disasters, risk of human safety and major financial losses.

In Section 5 it is shown that the total inference time of the TensorFlow Lite inference framework running on a Raspberry Pi 2 is on average between 23.87-29.99x and 35.29-45.67x faster than ICSML running on the BeagleBone Black and Wago PFC100 respectively. This significant difference in performance can be attributed to a number of factors. These include the fact that TensorFlow Lite is built for high performance native execution and employs advanced compilers that perform various high-level and platform specific optimizations during the compilation process. On the other hand IEC applications and ICSML by extension, are programmed in a mostly platform agnostic way with little room for platform optimizations by the programmer and then compiled to specialty binaries that are executed using the vendor’s runtime stack. This process involves applying little to no optimizations in order to ensure greater stability and predictability of code execution which are desired properties in ICS environments.

Performance is an important aspect of ML inference on ICS hardware as it defines the types of models that can run within the scan cycle time dictated by the controlled ICS project. ICSML can be further optimized for performance by exploring a number of avenues including lowering the precision of neuron operations and looking into Integer Quantization \[^{12}\] that could speed up inference time. Additionally, non-linear functions in ICSML, like the Exponential Linear Unit activation function, can be rewritten in Taylor series format to improve performance. Furthermore, copy operations used during inference can be reimplemented on a case-by-case basis using vendor-specific low-level memory manipulation functions to ensure optimal performance. Finally, investigating the use of platform-specific libraries for optimized vector and matrix multiplications can potentially further decrease inference time.

### 7.2 Features

In its initial release state, ICSML provides a complete set of components that allow the ML engineer to build and port densely connected Neural Networks to PLC software stacks. The existence of the Concatenation Layer allows building networks that branch out and merge and also enables building Recurrent Neural Networks.

Future expansion of ICSML can be inspired by the features found in established Machine Learning frameworks. Integrating Convolution and Pooling layers into the framework will enable building CNN networks. Another useful addition to the ICSML feature set, given that PLCs often observe timeseries data as inputs, would be Long-Short Term Memory (LSTM) and Gated Recurrent Units (GRUs) which can be used to build more complex

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**Figure 10:** Timeseries of Distillate Product Flow Rate (Wd) recorded in HITL setups where the ICSML defense was not and was present.

**Figure 11:** PLC Cascading PID output recorded in HITL setups where the ICSML defense was not and was present.
RNN models.

Beyond expanding the functionality of the framework itself, its usability can be extended through the development of external tools. As outlined in Section 4.3, IC-SML code for ported ML models can be built in a structured process that follows well defined steps. This potentially allows the complete automation of the porting process by employing Model-To-Model Transformation techniques [8] that perform weight extraction and IC-SML code generation using saved ML models exported directly from high-level ML frameworks. Additionally, this intermediate transformation tool can be further enhanced to offer and automatically apply suggestions for performance optimizations for a given ML model while taking into consideration the specific PLC hardware and the scan cycle parameters of the target ICS environment.

7.3 Applications & Related Work

As discussed earlier in the paper, Machine Learning in ICS environments has been extensively explored for security purposes. In their work [3], Alves et al. use an open source PLC platform to embed an ML based intrusion prevention system onto the device that thwarts network flood attacks like Denial of Service. Teixera et al. [39] craft Machine Learning defenses for a water treatment and distribution testbed complete with a Supervisory Control and Data Acquisition (SCADA) system. Junejo et al. [15] use unsupervised ML algorithms to create a behaviour-based defense for a water treatment facility testbed with PLCs. In their paper Yau et al. [45] employ a semi-supervised One-class Support Vector Machine ML algorithm to detect anomalous PLC events and aid forensics investigations. Meleshko et al. [27] propose a method for detecting anomalous sensor data in cyber-physical systems and apply it on an example of a water supply system.

Apart from security systems, ICSML can be used to implement other ancillary applications that are of interest in ICS environments, such as Predictive Maintenance. In their paper Kanawaday and Sane [18] utilize Machine Learning and Internet of Things (IoT) sensor data collected from an environment that includes PLCs, to predict possible failures and quality defects in a manufacturing process. Strauß et al. [38] leverage ML and data from an Industrial IoT environment with PLCs to enable predictive maintenance for an Electric Monorail System. In their work Paolanti et al. [32] propose an ML system for Predictive Maintenance using the Random Forest method and data collected from sensors and PLCs.

Beyond enabling auxiliary and passive functionality running side-by-side with primary tasks, ICSML can support ML applications created to directly control the underlying physical processes. As advancements in Machine Learning popularize its applications in an ever growing number of specialty areas, it is no surprise that the use of ML techniques is actively considered in fields such as manufacturing [10] and process systems engineering [41] and energy systems [23]. This growing trend of ML adoption in areas where ICS hardware is present foreshadows further use of ML techniques in PLC control logic.

7.4 Compatibility

One of the most important objectives when developing the ICSML framework, was for it to be cross-compatible with PLCs from different vendors. This is done by leveraging the standardized programming environment and languages established by the IEC 61131-3 standard. ICSML code is built purely on IEC 61131-3 languages and, besides its binary data loading and storing functions, does not depend on vendor-specific code for its operation. Consequently ICSML applications can be deployed on virtually any PLC compliant with the IEC 61131-3 standard. The framework has already been ported and tested on the Codesys V3 ecosystem and on Beckhoff’s TwinCAT 3 platform. Porting the framework in the future to the software stacks of other vendors like SIEMENS’ STEP 7, WAGO’s e!Cockpit and Schneider Electric’s Control Expert, should be a trivial task.

8 Conclusion

In this work we studied the need for performing Machine Learning Inference on PLCs. We explored the requirements and limitations for ICS Machine Learning applications running on PLCs and based on this we developed a ML framework using IEC 61131-3 languages. We then presented an end-to-end methodology for building and porting ML models to the developed framework. Afterwards we explored the framework’s performance using a series of benchmarks, and compared it to the Tensor-Flow Lite inference framework. Finally, we showcased the abilities of the proposed framework and confirmed its non-intrusive nature by developing a real-life case study of an ML based defense for the MSF desalination process.

Resources

ICSML will be made available on Github in the following repository: https://github.com/momalab/ICSML
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A MNIST Classification Model ported to ICSML

Listing 4: MNIST classification model recreated in ST using ICSML.