Bipolar resistive switching in metal-insulator-semiconductor nanostructures based on silicon nitride and silicon oxide

M N Koryazhkina¹, S V Tikhov¹, A N Mikhaylov¹, A I Belov¹, D S Korolev¹, I N Antonov¹, V V Karzanov¹, O N Gorshkov¹, D I Tetelbaum¹, P Karakolis², and P Dimitrakis³

¹ Lobachevsky University, 23/3 Gagarin prospect, 603950 Nizhny Novgorod, Russia
² Institute of Nanoscience and Nanotechnology, NCSR “Demokritos”, Agia Paraskevi 15341, Greece
³ Department of Physics, University of Patras, GR 26500 Patras, Greece

E-mail: mahavenok@mail.ru

Abstract. Bipolar resistive switching in metal-insulator-semiconductor (MIS) capacitor-like structures with an inert Au top electrode and a Si₃N₄ insulator nanolayer (6 nm thick) has been observed. The effect of a highly doped n⁺-Si substrate and a SiO₂ interlayer (2 nm) is revealed in the changes in the semiconductor space charge region and small-signal parameters of parallel and serial equivalent circuit models measured in the high- and low-resistive capacitor states, as well as under laser illumination. The increase in conductivity of the semiconductor capacitor plate significantly reduces the charging and discharging times of capacitor-like structures.

1. Introduction

Memristors [1] or memristive nanomaterials (devices) are the basis for new-generation non-volatile memory devices (Resistive Random Access Memory), the operation of which relies on switching between at least two stable states of a material at different applied voltages: High Resistance State (HRS) and Low Resistance State (LRS) [2]. Memristive devices are usually implemented on the basis of a metal-insulator-metal (MIM) and (rarely) a metal-insulator-semiconductor (MIS) capacitor-like structure. The latter configuration is the most compatible with the traditional CMOS process, especially if the “native” Si-based insulators (SiO₂ and Si₃N₄) are used. In order to make resistive switching (RS) possible in a metal-insulator structure, the electroforming process is usually required, which consists of applying a voltage greater than a certain value (the forming voltage) and results in irreversible changes in electrical properties of a capacitor due to the local rearrangement of the insulator atomic structure. The MIS configuration with a relatively high-resistance semiconductor substrate (capacitor plate) makes it possible to efficiently investigate the mechanisms of ionic and electronic phenomena occurring in the insulator during electroforming and RS [3], as well as to get the resistive memory effect manipulated by light due to a possible change in resistance of the semiconductor substrate [4]. Usually, heavily doped silicon substrates with negligible resistance, which are similar to metal capacitor plates, are used for the fabrication of memristive MIS capacitors, including capacitors with silicon nitride layers [5-9]. The memristive devices based on Si₃N₄ are
characterized by both unipolar and bipolar RS, and active metal electrodes like Ni or Cu are most commonly used, as their material is responsible for the electrochemical RS mechanism.

In the present work, the bipolar RS in the MIS capacitors on the basis of Si$_3$N$_4$ with a chemically inert top electrode (Au) has been investigated in relation to the intrinsic phenomena in a “metal-free” insulator-semiconductor nanostructure. The measurements of small-signal parameters of equivalent circuit models showed [10-12] that the resistance of a semiconductor capacitor plate has a great impact on the memristor characteristics when the thickness of an insulator nanolayer is comparable with the thickness of the space charge region in a Si substrate.

2. Material and methods
Memristive capacitor-like devices were deposited on a $n^+$-Si substrate with an equilibrium density of electrons $n_0 \approx 3 \cdot 10^{19}$ cm$^{-3}$ and an area of $15 \times 15$ mm$^2$. Figure 1 shows the schematic cross-section of these devices. A Si$_3$N$_4$ layer with a thickness of 6 nm was deposited on a substrate by the LPCVD method at a temperature of 800 °C. In some of the devices, a 2-nm-thick SiO$_2$ layer was preliminarily formed on a Si substrate by thermal oxidation of Si in dry oxygen at 900 °C. The top Au electrodes (40 nm) with an area of $10^2$ or $10^3$ cm$^2$ were deposited through a shadow mask by the method of DC-magnetron sputtering at a substrate temperature of 200 °C. On the back-side of a Si substrate, the Al contact was deposited using an e-gun evaporator.

Current-voltage ($I-V$) characteristics were measured by using an Agilent B1500A semiconductor device analyzer at room temperature with voltage sweep amplitudes up to 10 V and a sweep rate of 0.3 V/s. The sign of bias on the device corresponds to the potential of the top electrode (Au). Different current compliance (CC) was used for negative voltage sweeps. The temperature dependencies of current ($I-T$) were measured in a range of 300 ÷ 500 K for the devices biased at $V = 0.5$ V. Small-signal characteristics of the capacitors were measured at a test voltage $V = 20$ mV in a frequency range of $10^3$ ÷ $10^7$ Hz in parallel and serial equivalent circuit models: parallel capacitance ($C_p$), parallel conductivity reduced to a circular frequency ($G_p/\omega$), parallel resistance ($R_p$), serial resistance ($R_s$) and insulator losses ($\tan \delta$), which do not depend on the type of equivalent circuit. Capacitors with an area of $\approx 10^{-2}$ cm$^2$ were used in measurements. Before electroforming, some capacitors were also measured under illumination with a blue MASTER-PRO LSB462 laser at a wavelength of 462 nm and a power density of $\approx 1$ W/mm$^2$.

![Figure 1. Schematic cross-section of the Au/Si$_3$N$_4$/SiO$_2$/n$^+$-Si capacitor and its equivalent RC circuits used for the determination of small-signal parameters (serial capacitance $C_s$ and resistance $R_s$, parallel capacitance $C_p$ and resistance $R_p$).](image)

3. Result and discussion
Let us first consider the experimental results obtained for the Au/Si$_3$N$_4$/n$^+$-Si capacitors without a SiO$_2$ interlayer. Before electroforming, the Si$_3$N$_4$ layers were characterized by relatively good insulator properties: an electrical resistivity of $\approx 3 \cdot 10^{15}$ Ω·cm and a breakdown field density of $\approx 7 \cdot 10^6$ V/cm. The value of the relative permittivity at 1 kHz was $\approx 5$, and the values of $\tan \delta$ were $\approx 0.01$ at the same frequency. The current transport mechanism at room temperature in the initial state (IS) can be
explained by the Pool-Frenkel effect [13], as the \( I - V \) characteristics are quite symmetric with respect to the voltage polarity (figure 2) and are linearized in the \( \ln I - V^{1/2} \) plot with a slope corresponding to the Pool-Frenkel emission (figure 3). The depth of deep traps in Si\(_3\)N\(_4\) responsible for the observed Pool-Frenkel effect was calculated from \( I-V \) characteristics and amounted to \( \sim 1 \) eV from the bottom of the conduction band.

![Figure 2. Typical \( I-V \) characteristics of the Au/Si\(_3\)N\(_4\)/\( n^+\)-Si capacitor, measured in the processes of electroforming and RS and plotted in semi-logarithmic (a) or double-logarithmic (b) scales.](image)

Typical \( I-V \) characteristics of a Au/Si\(_3\)N\(_4\)/\( n^+\)-Si capacitor-like device (figure 2) demonstrate the electroforming process, during which the capacitor state is changed from the IS to LRS, and the bipolar RS is changed from LRS to HRS (RESET transition) at a positive bias and back from HRS to LRS (SET transition) at a negative bias. The electroforming manifests itself in the form of a current jump at around –5 V during the first negative voltage sweep. The \( I-V \) curve in the LRS after a complete SET transition (with no CC or a low CC at 30 mA) is described by the Ohm's law (figure 2). The corresponding temperature dependence in the range of 300 ÷ 500 K (figure 4) is typical of electron scattering on impurity ions in semiconductors (\( I \sim T^{3/2} \)). When the SET transition is not complete (with a high CC at 10 mA), the linear \( I-V \) relation in LRS becomes quadratic with an increase in voltage. In this regard, the resistance of a silicon capacitor plate mainly provides the resistance in LRS after a complete SET transition, whereas after an incomplete SET transition the resistance of an insulator is included in the total resistance.

![Figure 3. The \( \ln I - V^{1/2} \) plots for different polarities in IS.](image)
After the RESET transition, the current in HRS is three orders of magnitude smaller than the current in LRS, but more than 2 orders of magnitude higher than the current in IS prior to electroforming. The latter result indicates the irreversible change of insulator properties after electroforming due to the occurrence of filaments (conductive channels shorting the capacitor [10]). In the low-conductive state, the $I - V$ curve is also characterized by a linear law at low voltages, which transforms to a quadratic law at higher voltages. Such a quadratic $I - V$ dependence is typical of the space charge limited current mechanism [13, 14] but it is hard to rigorously confirm this for memristive nanostructures because it is impossible to vary the thickness in the location of filament rupture.

The temperature dependence of a current in HRS (as well as in LRS obtained with CC at 10 mA) shown in figure 4 reveals the power growth with a rate close to 1, which probably corresponds to tunnel electron jumps through barriers arising in completely or partially broken filaments (the tunneling process in MIM structures is usually described by the quadratic $I - T$ dependence [15]).

The observed bipolar nature of RS is typical of the valence-change oxide materials, in which the growth and rupture of filaments are related to the oxidation-reduction (redox) phenomena with the participation of oxygen vacancies (ions) [16]. At the same time, it is known that Si$_3$N$_4$ films are used to prevent the ion drift of impurities in insulator layers of MIS transistors [17], so the question of the relationship between the filament growth in Si$_3$N$_4$ and ion migration induced by the electric field requires special consideration. In particular, it is necessary to simulate the stochastic processes of breaking Si-N bonds and the formation of nitrogen vacancies or ions by the Monte-Carlo approach, as has already been done for SiO$_2$-based memristive devices [18]. In any case, the mechanism of the filament formation in Si$_3$N$_4$ can be associated with a high concentration of defects in these layers (up to $10^{19}$ cm$^{-3}$ [19]). These defects can be ionized in the regions of electric field concentrators (e.g. represented by the roughness of an Au electrode) and form filaments between capacitor plates. When the high defect density in a filament is achieved, the electronic conductivity becomes possible through a filament due to the charge injection from electrodes and subsequent hopping between the defect sites.

![Figure 4](image_url)

**Figure 4.** Typical $I - T$ dependencies for the Au/Si$_3$N$_4$/n$^+$-Si capacitor, measured at $V = 0.5$ V in HRS (blue, multiplied by a factor of 100) and LRS (red) with different CC during the proceeding SET transition: no CC (■), CC = 10 mA (●), CC = 30 mA (▲).

Important information about the origin of resistive states can be obtained from the analysis of the results of small-signal measurements. In figure 5, the frequency dependencies of the parameters of equivalent circuits in IS, HRS and LRS are plotted. In the case of IS, the data are also obtained under illumination of the capacitor by laser emission at a wavelength of 462 nm.
Figure 5. The frequency dependencies of $C_p$ (solid line) and $G_p/\omega$ (dashed line) (a); $R_s$ (solid line) and $R_p$ (dashed line) (b) for the Au/Si$_3$N$_4$/$n^+$-Si capacitor (zero voltage bias; AC test signal amplitude is 20 mV). Curves 1, 2 (blue) are measured in HRS and IS; 3, 4 (red) are measured in LRS; 5, 6 (black) are measured in IS under laser illumination.

The frequency dispersion of capacitance and conductivity (figure 5(a)) is related to the finite charging time of the capacitor due to the presence of the serial resistance of capacitor plates. It is known that charging of a capacitor is described by the expression:

$$V = E \left(1 - e^{-\frac{t}{R}}\right),$$

where $V$ is the voltage on the capacitor plates during charging, $E$ is the charging voltage of a capacitor, $t$ is the charging time, and $R$ is the serial resistance. In our case, $R = R_{\infty}$ at a high frequency of $2 \cdot 10^6$ Hz (figure 5(b)). The dependencies of $G_p/\omega$ on $C_p$ (Cole-Cole plots), not shown here, have demonstrated [11] that such curves are close to semicircles, thus the process of capacitance relaxation is characterized by a single time $\tau = R_{\infty}C_{p0}$, where $C_{p0}$ is the low-frequency capacitance in the saturation region ($C_p = C_s$ at low frequencies). This time value can be estimated from the capacitance frequency dependence at a level of $0.7$-$C_{p0}$ or in the maximum of the $G_p/\omega$ frequency dependence as $1/2\pi f$ (figure 5(a), curves 1, 2), and the estimations give $\tau \approx 10^{-6}$ s for IS and HRS. The $\tau$ value actually determines the performance of a memristor when reading its state in IS and HRS. Of course, this performance can be increased proportionally with a decrease in capacitance, i.e. in the capacitor area, and a decrease in $R_{\infty}$. After switching to LRS (curves 3 and 4 in figure 5), as well as under laser illumination (curves 5 and 6 in figure 5), the value of $\tau$ decreases proportionally with a decrease in the serial resistance $R_{\infty}$ (4 and 10 times decrease, respectively), since the $C_{p0}$ value practically does not change. Also, the ohmic losses in LRS and under illumination grow in the range of low frequencies. In the first case, these losses are related to partial shorting of a capacitor by filaments and, in the second case, with the emergence of constant capacitor leakage due to the external photoelectric effect that originated from the emission of electrons from the Au electrode. In both cases, the value of parallel resistance is decreased at low frequency ($10^3$ Hz) (figure 5(b), curves 4 and 6) that characterizes the insulator properties. The magnitude of this resistance change in HRS and LRS is equivalent to the difference of currents in HRS and LRS.

The change in $R_{\infty}$ can be associated with the changes in a semiconductor capacitor plate. The initial state of the semiconductor surface before electroforming apparently corresponds to a depleted layer on a semiconductor surface, which is formed as a result of a contact potential difference equal to a difference of electron work functions of gold and silicon. The work function of silicon for the given doping level is almost equal to its electron affinity energy (~ 4 eV) [20]. The average work function of Au is ~ 5.2 eV [21]. Thus, in the space charge region of a semiconductor (SCR), which is serially
connected to the insulator, the potential difference $V_c$ of up to 1 V can drop in the absence of external voltage. Then, one can estimate the SCR thickness $d$ in Si by using the following formula [22]:

$$d = \sqrt{\frac{2 \varepsilon_0 \varepsilon_s V_c}{q n_0}},$$

where $\varepsilon_0$ is the absolute insulator permittivity of vacuum, $\varepsilon_s$ is the relative permittivity of Si, and $q$ is the charge of electron. The estimation gives $d \approx 10$ nm. Thus, the SCR thickness in a semiconductor substrate is comparable with the thickness of an insulator layer, and the SCR resistance can affect the characteristics of a memristive device. Light illumination increases the SCR conductivity due to a decrease in its thickness induced by photogenerated carriers. After the SET transition ($V < 0$), the positive charge can be accumulated near the insulator-semiconductor interface due to the capture of holes from a semiconductor, which increases the SCR conductivity and reduces its thickness, resulting in a reduced contribution of the serial resistance to the total resistance of capacitor plates. Moreover, the accumulation of positive charge favors the shorting of a capacitor by forming filaments. The back RESET transition ($V > 0$) leads to the accumulation of negative charge due to the capture of electrons in the defect states in an insulator, which increases the serial resistance due to the formation of a potential barrier for electrons.

Au/Si₃N₄/SiO₂/n⁺-Si capacitors also demonstrate bipolar RS and similar regularities. However, the presence of a SiO₂ interlayer affects the total serial resistance and thus modifies the character of $\tau$ change. The estimation gives $\tau \approx 2.6 \cdot 10^{-5}$ s for IS and $10^{-7}$ s for HRS. These changes are also proportional to the changes in $R_{ser}$. After switching to HRS, the negative charge from Si is captured at the Si₃N₄/SiO₂ interface, leading to an increase in conductivity of a SiO₂ layer, and an increase in the capacitor performance. In addition, the capacitors with a double-layer insulator do not withstand prolonged cyclic switching, unlike Au/Si₃N₄/n⁺-Si capacitors, for which the number of cycles in the continuous switching mode is at least 100.

The degradation of RS is revealed in the form of a nonreversible transition of the Si₃N₄-based capacitor to LRS, the origin of which should be a subject of further investigation. One of the most probable mechanisms can be related to hard thermal breakdown of a thin dielectric layer (permanent material change) due to high current and local heating.

4. Conclusions
Bipolar resistive switching has been observed in Au/Si₃N₄/n⁺-Si and Au/Si₃N₄/SiO₂/n⁺-Si capacitor-like MIS structures with insulator nanolayers represented by thin Si₃N₄ (6 nm) and SiO₂ (2 nm) films. The origin of the memristive behavior is related to the formation and rupture of conductive filaments in insulator layers. It is established that electronic processes are responsible for the effect of a highly doped $n^+$-Si ($3 \cdot 10^{19}$ cm$^{-3}$) semiconductor plate of a capacitor and a SiO₂ interlayer on the small-signal parameters of parallel and serial equivalent circuit models after electroforming and subsequent switching between the low-resistance and high-resistance states, as well as at illumination of a capacitor by blue laser emission. The corresponding change in the parameters of the semiconductor space charge region and the charge capture at the Si₃N₄/SiO₂ interface can affect the resistive state and should be taken into account in the interpretation of resistive switching. The observed increase in conductivity of a semiconductor plate and a SiO₂ interlayer significantly lowers the capacitor charging and discharging time, which determines the capacitor reading performance (response time of a memristive device).

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