Low-power-consumption CMOS inverter array based on CVD-grown $p$-MoTe$_2$ and $n$-MoS$_2$

Wanying Du, Xionghui Jia, Zhixuan Cheng, Wanjing Xu, Yanping Li, Lun Dai

lunds@pku.edu.cn

Highlights

A practical approach to fabricate large-scale CMOS inverter arrays is demonstrated

A method to balance the current characteristics of the channel materials is developed

Complete logic swing and clear dynamic switching behavior are observed

Ultra-low power consumption of $\sim 0.37$ nW is achieved
Low-power-consumption CMOS inverter array based on CVD-grown p-MoTe₂ and n-MoS₂

Wanying Du,¹,² Xionghui Jia,¹,² Zhixuan Cheng,¹,² Wanjing Xu,¹ Yanping Li,¹ and Lun Dai¹,²,³,⁴,*

SUMMARY

Two-dimensional (2D) semi-conductive transition metal dichalcogenides (TMDCs) have shown advantages for logic application. Complementary metal-oxide-semiconductor (CMOS) inverter is an important component in integrated circuits in view of low power consumption. So far, the performance of the reported TMDCs-based CMOS inverters is not satisfactory. Besides, most of the inverters were made of mechanically exfoliated materials, which hinders their reproducible production and large-scale integration in practical application. In this study, we demonstrate a practical approach to fabricate CMOS inverter arrays using large-area p-MoTe₂ and n-MoS₂, which are grown via chemical vapor deposition method. The current characteristics of the channel materials are balanced by atomic layer depositing Al₂O₃. Complete logic swing and clear dynamic switching behavior are observed in the inverters. Especially, ultra-low power consumption of ~0.37 nW is achieved. Our work paves the way for the application of 2D TMDCs materials in large-scale low-power-consumption logic circuits.

INTRODUCTION

Over the years, two-dimensional (2D) materials such as graphene and transition metal dichalcogenides (TMDCs) have stimulated great research enthusiasm, owing to their unique electronic and optoelectronic properties and ultrathin geometry (Akinwande et al., 2019; Fiori et al., 2014; Liu et al., 2021). Graphene, with high conductivity and high carrier mobility, has been extensively studied (Castro Neto et al., 2009; Flory et al., 2020; Novoselov et al., 2005; Yu et al., 2013). However, because of its gapless nature, graphene is not a good channel material for field-effect transistor (FET), which requires efficient electrostatic control. Semi-conductive TMDCs, with larger bandgaps, surpass graphene in this aspect. Recently, n-channel metal-oxide-semiconductor inverters (Wang et al., 2019) and p-channel metal-oxide-semiconductor inverters (Zhang et al., 2019) based on TMDCs have been reported. Complementary metal-oxide-semiconductor (CMOS) inverter, composed of an n-channel and a p-channel FET, has advantage in reducing power consumption and therefore is an important component in integrated circuits. However, so far, the performance of the reported TMDCs-based CMOS inverters is not satisfactory. They suffered from high power consumption (Liu et al., 2019; Pu et al., 2016) or large leakage current (Lin et al., 2014). Besides, most of the CMOS inverters were made of mechanically exfoliated TMDCs (Cho et al., 2019; Jeon et al., 2015; Pezeshki et al., 2016), which hinders their reproducible production and large-scale integration in practical application. Recently, large-area growth in a cost-effective way has been realized for several TMDCs via chemical vapor deposition (CVD) method (Pu et al., 2016; Wang et al., 2019; Xu et al., 2019a). The as-grown MoTe₂ (Xu et al., 2019b) and MoS₂ (Wang et al., 2019) are p- and n-type, respectively. Moreover, it is demonstrated that atomic layer deposition (ALD) of Al₂O₃ under certain conditions can cause n-type doping to 2D materials, including graphene (Zheng et al., 2015), MoS₂ (Li et al., 2017), and MoTe₂ (Lim et al., 2017; Park et al., 2019).

In this study, we fabricate CMOS inverter arrays using large-area CVD-grown p-MoTe₂ and n-MoS₂. We have developed a method to balance the current characteristics of the channel materials. Complete logic swing is obtained in our inverters. High voltage gain (~23, much larger than 1) and noise margins close to ideal values are obtained. Especially, ultra-low peak power consumption of ~0.37 nW is achieved, which is among the lowest power consumption values reported so far for TMDCs-based CMOS inverters under similar measurement conditions (Cho et al., 2019; Jeon et al., 2015; Pezeshki et al., 2016). We also investigate the dynamic switching behavior of the CMOS inverters and observe satisfying rising time tᵣ (several
RESULTS AND DISCUSSIONS

Figures 1A–1E are the corresponding optical images after each fabrication step, illustrating the fabrication process of our CMOS inverter array and demonstrating the feasibility of the large-scale fabrication method. First, arrayed Ti/Au (10/50 nm) electrodes were fabricated on a SiO2/Si substrate as buried gates for both of MoTe2 and MoS2 FETs. Then a 20-nm-thick Al2O3 dielectric layer was deposited on the substrate via ALD.

(A) Arrayed Ti/Au (10/50 nm) electrodes were fabricated on a SiO2/Si substrate as buried gates for both of MoTe2 and MoS2 FETs. Then a 20-nm-thick Al2O3 dielectric layer was deposited on the whole substrate to protect MoTe2 from subsequent steps.

(B) A CVD-grown MoTe2 film was transferred onto the Al2O3 layer and patterned into rectangular sheets (outlined by the red dashed lines) over the buried gates. After that, a 3-nm-thick Al2O3 layer was deposited on the whole substrate, which caused an n-type doping effect on MoS2.

(C) Pairs of Pd/Au (10/50 nm) source and drain electrodes (Electrodes 1 and 2 in (F)) were fabricated on the ends of each MoTe2 sheet. After that, a 3-nm-thick Al2O3 layer was deposited on the whole substrate to protect MoTe2 from subsequent steps.

(D) Pairs of Pd/Au (10/50 nm) source and drain electrodes (Electrodes 3 and 4 in (F)) were fabricated on the Al2O3 layer. Herein, Electrode 3 and Electrode 2 have an overlapping area in the vertical direction (outlined by the black dashed lines) for measurement purpose.

(E) The MoS2 channels (outlined by the blue dashed lines) were fabricated by transferring and patterning a CVD-grown MoS2 film. Finally, a 5-nm-thick Al2O3 layer was deposited on the whole substrate, which caused an n-type doping effect on MoS2.

(F) The optical image of a single inverter in the CMOS inverter array. The red, blue, and black dashed lines outline the MoTe2 sheet, the MoS2 sheet, and the overlapping area of Electrodes 2 and 3, respectively. To construct a complete CMOS circuit, the buried Gate Electrode and Electrode 1 were connected to $V_{in}$ and $V_{dd}$, respectively. Electrodes 2 and 3 were connected to a digital oscilloscope by a tungsten needle for $V_{out}$ extraction. Electrode 4 was grounded.

(G) The cross-sectional schematic of the device structure depicted in (F).

Our work paves the way for the application of 2D TMDCs materials in large-scale low-power-consumption logic circuits.
substrate via ALD method (Figure 1A). Second, a CVD-grown MoTe2 film (see Method details) was transferred onto the Al2O3 layer from the growth substrate with the help of polymethyl methacrylate (PMMA) and deionized water, which avoids the common use of hydrofluoric acid (Pu et al., 2016; Xu et al., 2019b). The transferred MoTe2 film was patterned (see Method details) into rectangular sheets (outlined by the red dashed lines) over the buried gates (Figure 1B). Third, pairs of Pd/Au (10/50 nm) source and drain electrodes (Electrodes 1 and 2) were fabricated on the ends of each MoTe2 sheet. After that, a 3-nm-thick Al2O3 layer was deposited on the MoTe2 FET array to protect MoTe2 from subsequent steps (Figure 1C). For fabricating the MoS2 FET array, pairs of Pd/Au (10/50 nm) source and drain electrodes (Electrodes 3 and 4) were fabricated on the Al2O3 layer (Figure 1D). Herein, Electrode 3 and Electrode 2 have an overlapping area in the vertical direction (outlined by the black dashed lines) for measurement purpose. Similarly, MoS2 channels (outlined by the blue dashed lines) were fabricated by transferring and patterning a CVD-grown MoS2 film (see Method details). Finally, a 5-nm-thick Al2O3 layer was deposited on the whole substrate (Figure 1E), which caused an n-type doping effect on MoS2. Figure 1F is the optical image of a single inverter in the CMOS inverter array. To construct a complete CMOS circuit, the buried Gate Electrode and Electrode 1 were connected to the input voltage (V_in) and supply voltage (V_dd), respectively. Electrodes 2 and 3 were connected to a digital oscilloscope by a tungsten needle for output voltage (V_out) extraction. Electrode 4 was grounded. The cross-sectional schematic of the device structure depicted in Figure 1F is shown in Figure 1G. The CMOS circuit diagram is shown in the inset of Figure 3C. Notably, in this work, we fixed the MoS2 FETs’ channel length (15 μm) and changed the MoTe2 FETs’ channel lengths to make their current characteristics balanced. The optical image of the CMOS inverter array is presented in Figure S1C.

The MoTe2 films (Figure S1A) used in our devices are formed by seamlessly stitched single crystal MoTe2 domains (Xu et al., 2019a). Figure 2A shows the Raman spectrum of an as-grown MoTe2 film, which presents the Raman characteristic peak of 2H-MoTe2 at ~235 cm\(^{-1}\) (Yamamoto et al., 2014). Figure 2B shows the atomic force microscope (AFM) image of the MoTe2 and the surface height profile along the white dashed line. The MoTe2 is about 6 nm thick, corresponding to 9-layer MoTe2 (Lin et al., 2014). The MoS2 films (Figure S1B) used in our devices are formed by single crystal MoS2 domains (see the inset of Figure 2C). Figure 2C shows the Raman spectrum of an as-grown MoS2 film, which presents Raman characteristic peaks of MoS2 at ~386 and ~404 cm\(^{-1}\) (Li et al., 2012). The peak distance is ~18 cm\(^{-1}\), demonstrating the monolayer nature of the MoS2. Inset: the optical image of the MoS2 film. The MoS2 film is formed by single crystal MoS2 domains.

Figures 3A and 3B show the transfer curves and output curves of the MoTe2 FET (with 15 μm channel length) and MoS2 FET in an inverter, respectively. The transfer curves are approximately symmetrical about their intersection. Note that the two ALD steps in the device fabrication process balanced the carrier
concentrations of the MoTe$_2$ and MoS$_2$, enabling the realization of high-performance CMOS inverters (Figure S2). It is worth noting that, in order to avoid the ALD-caused n-type doping effect on the p-MoTe$_2$, we also fabricated a CMOS inverter array with another device structure, where the MoTe$_2$ is free from Al$_2$O$_3$ coverage (Figure S4). The overall device performance did not improve (Figure S5). Figure 3C shows the voltage transfer characteristics (VTCs) and voltage gain ($-\frac{dV_{out}}{dV_{in}}$) plots of the inverter at various $V_{dd}$. The solid and dashed lines correspond to the output voltage and gain, respectively. Inset: the CMOS circuit diagram. For each $V_{dd}$ applied (from 1 to 4 V), the VTC presents complete logic swing, and the maximum voltage gain is bigger than 1. At $V_{dd}$ of 4 V, a maximum voltage gain of ~23 and good noise margins (NM$_{IH}$ = 0.40 $V_{dd}$, NM$_{IL}$ = 0.44 $V_{dd}$, total noise margin = 0.84 $V_{dd}$) are obtained.

Figure 3D shows the power consumption ($V_{dd} \times I_{dd}$) characteristics of the inverter at various $V_{dd}$. At $V_{dd}$ of 1 V, peak power consumption of as low as ~2.3 nW is achieved.

(F) The power consumption characteristics of the inverter corresponding to (E) at various $V_{dd}$. At $V_{dd}$ of 1 V, ultra-low peak power consumption of ~0.37 nW is achieved.
also presents complete logic swing. At $V_{dd}$ of 4 V, a voltage gain of $9.5$ and good noise margins (NM $0.36$ $V_{dd}$, $0.40$ $V_{dd}$, total noise margin $0.76$ $V_{dd}$) are obtained. Especially, ultra-low peak power consumption of $0.37$ nW is achieved at $V_{dd}$ of 1 V. The statistical gain and power consumption data of the CMOS inverter array are presented in Figures S3A and S3B. It is worth noting that the peak power consumption ($0.37$–$2.3$ nW) of our inverters at $V_{dd}$ of 1 V is lower compared with previously reported CMOS inverters based on p-MoTe2 and n-MoS2 and among the lowest peak power consumption values reported so far for TMDCs-based CMOS inverters (see Table 1). Besides, all the inverters exhibit maximum voltage gains of >1 at each $V_{dd}$ applied.

We also investigated the dynamic switching behavior of the CMOS inverters. Figures 4A–4C show the time-dependent $V_{out}$ of an inverter (with MoTe2 channel length of 10 µm) at $V_{dd}$ of 3 V, driven by square wave $V_{in}$ with various frequencies. The high and low levels of the input square wave were 0 and $-6$ V, respectively. Logic switching behavior is clear at 100 Hz and remains to be observed at a critical logic switching frequency of 1 kHz. The $t_i$ and $t_f$ are about 340 and 308 µs, respectively, at 1 kHz, calculated at 10% and 90% (marked by the red dashed lines in Figure 4B) of $V_{out}$ amplitude. The RC delays mainly result from the overlap capacitance in the CMOS circuit (Pezeshki et al., 2016; Wang et al., 2020). At 1.4 kHz, the amplitude of $V_{out}$ decreased to half ($-1.5$ V) of $V_{dd}$ with $t_i$ ($t_f$) of about 275 µs (290 µs). The statistical dynamic switching frequency data of the CMOS inverter array are presented in Figure S3C.

Conclusions
We have fabricated CMOS inverter arrays using large-area CVD-grown p-MoTe2 and n-MoS2. The current characteristics of the channel materials were balanced by atomic layer depositing Al2O3 under proper conditions. Complete logic swing and clear dynamic switching behavior are observed in the inverters. The inverters have overall high performance such as maximum voltage gains of >1 at each $V_{dd}$ applied, low and even ultra-low peak power consumption ($0.37$–$2.3$ nW), and satisfying $t_i$ ($t_f$) and working frequencies. Our low-power-consumption CMOS inverters, with the merits of reproducibility and large-scale integration, have promising applications in future 2D microelectronic systems.

Limitation of the study
In order to further improve the device performance, developing new methods to increase the grain size of the monolayer MoS2 is needed.
STAR METHODS

Detailed methods are provided in the online version of this paper and include the following:

- KEY RESOURCES TABLE
- RESOURCE AVAILABILITY
  - Lead contact
  - Materials availability
  - Data and code availability
- METHOD DETAILS
  - CVD growth of large-area MoTe₂ and MoS₂
  - Fabrication of the CMOS inverter arrays
  - Characterizations

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.isci.2021.103491.

ACKNOWLEDGMENTS

This work was supported by National Natural Science Foundation of China (Nos. 61521004, 61874003, and 62174005).

AUTHOR CONTRIBUTIONS

L.D. and W.Y.D. conceived the project. W.Y.D. grew the MoS₂ and MoTe₂ films, fabricated the devices, and conducted the measurement. L.D. and W.Y.D. performed data analysis. X.H.J. helped with the drawing of the cross-sectional schematics of the devices. Z.X.C. and X.H.J. helped with the design of the device structure. W.J.X. prepared the Mo films for MoTe₂ growth. Y.P.L. helped with the deposition of the metal electrodes. L.D. supervised this research. W.Y.D. and L.D. wrote the manuscript. All authors contributed to discussions.

DECLARATION OF INTERESTS

The authors declare no competing interests.

Received: August 2, 2021
Revised: October 6, 2021
Accepted: November 19, 2021
Published: December 17, 2021
STAR METHODS

KEY RESOURCES TABLE

| REAGENT or RESOURCE | SOURCE | IDENTIFIER |
|---------------------|--------|------------|
| Chemicals, peptides, and recombinant proteins |         |            |
| Tellurium           | Zhongnuoxincai | CAS: 13494-80-9 |
| Solid PTAS          | 2D Semiconductors | N/A |
| Molybdenum(VI) oxide | Ourchem | CAS: 1313-27-5 |
| Sulfur              | Aladdin | CAS: 7704-34-9 |
| PMMA                | AllRESIST | CAS: 9011-14-7 |

RESOURCE AVAILABILITY

Lead contact
Further information and requests for resources should be directed to and will be fulfilled by the lead contact, Lun Dai (lundai@pku.edu.cn).

Materials availability
This study did not generate new unique reagents.

Data and code availability
All data reported in this paper will be shared by the lead contact upon request.

This paper does not report original code.

Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

METHOD DETAILS

CVD growth of large-area MoTe2 and MoS2
Large-area MoTe2 and MoS2 films were grown via CVD method. For MoTe2 growth, Mo films were deposited on SiO2 (285 nm)/p+-Si substrates via magnetron sputtering. Then, the substrates were placed in a quartz boat containing Te powder. Molecular sieves were placed in the quartz boat between the substrates and the Te powder. After that, the quartz boat was pushed into the center heating zone of a quartz tube furnace with a tube diameter of 1 inch. After evacuating the quartz tube to an air pressure of less than 1 mTorr, high-purity Ar was let in at the maximum flow rate until the pressure reached atmospheric pressure. Next, the furnace was heated to 650°C in 30 min and kept there for 180 min. High-purity H2 and Ar were used as carrier gases, whose flow rates were 7 and 5 standard cubic centimeters per minute (sccm), respectively. After the growth, the furnace cooled to room temperature naturally.

For MoS2 growth, SiO2 (285 nm)/p+-Si substrates were processed with O2 plasma. Then, PTAS was spun-coated on the substrates as seeding promoter. The substrates were placed in a quartz boat containing MoO3 powder. Another quartz boat with S powder was pushed into the upstream heating zone of a 3-temperature-zone quartz tube furnace with a tube diameter of 2 inch. Then the quartz boat with growth substrates was pushed into the downstream heating zone of the furnace. The growth was performed at atmospheric pressure. High-purity Ar (15 sccm) was used as carrier gas. The upstream and downstream heating zones of the furnace were heated to 200°C and 650°C, respectively, in 40 min, and kept there for 5 min. Finally, the furnace cooled to room temperature naturally.

Fabrication of the CMOS inverter arrays
Both the CVD-grown MoTe2 and MoS2 films were transferred with the help of PMMA and deionized water (Kim et al., 2019), and patterned into rectangular sheets through ultra-violet (UV) lithography and reactive
ion etching. The Ti/Au and Pd/Au electrodes were fabricated via UV lithography, electron beam evaporation, and lift-off process. The Al₂O₃ layers were deposited using an ALD system (Cambridge NanoTech Inc., Savannah-100). The patterned Al₂O₃ layer (see Figure S4F) was fabricated via UV lithography, ALD, and lift-off process. In the ALD process, trimethylaluminum and deionized water served as precursors and high-purity N₂ served as carrier gas. The reaction temperatures were 200°C for Al₂O₃ films covering the whole substrate and 80°C for the patterned Al₂O₃ layer (because the photoresist could not endure the temperature of 200°C). The Al₂O₃ thickness was controlled by deposition time.

Characterizations
The optical images of the devices were taken by an optical microscope (ZEISS, Axio Imager A2m). The Raman spectra were collected by a micro-zone confocal Raman system (WITec alpha 300R) under 532 nm laser illumination. The thickness of the MoTe₂ film was measured by an atomic force microscope (Asylum Research, Cypher S). All the electrical measurement was conducted in the dark with a semiconductor characterization system (Keithley 4200-SCS) that was connected to a probe station. For the dynamic switching performance measurement, a function generator (Tektronix AFG 3102) and a digital oscilloscope (Tektronix DPO 2024) were employed to generate the V_in and record the V_out, respectively. Both the function generator and the digital oscilloscope had common ground with the semiconductor characterization system, which provided the V_ddd. All the characterizations were performed in ambient condition.