Design and Construction of a Low Cost All-Digital Phase Locked Loop Based on Field Programmable Gate Array

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Abstract. The phase-locked loop (PLL) is a key element to capture the voltage phase of the grid in power systems with high permeability of new energy sources. An accurate phase information catcher which can be applied in the field can provide a strong support for the control process of the system. This paper constructs a low-cost all-digital PLL (ADPLL) on an embedded field-programmable gate array (FPGA) for real-time (RT) digital simulation. Compared with offline simulation, RT digital simulation can realize hardware-in-loop (HIL) testing of utility connected devices to validate their performance in every working condition, which would not be possible using only experimental tests. Meanwhile, an improved simulation architecture construction method based on Algorithm Architecture Adequation (A-A-A) is presented in this paper. This method further saves the internal hardware resources on the basis of making full use of the parallel computing capability of FPGA. Analysis and experimental results made based on an FPGA ALTERA Stratix V show that the proposed modeling algorithm can achieve both efficiency and accuracy.

1. Introduction

Recently, the growing concerns about environmental pollution and energy crisis have helped boost the development of clean energy[1]. Most types of clean energy use converters and/or inverters and as grid-connected interfaces (e.g., wind power, solar photovoltaics and energy storage systems). The phase-locked loop (PLL) is a vital element of the control loop of the flexible utility connected devices[2], which can track the voltage phase of the grid for the controllers[3][4]. Moreover, with the rapid development of high flexible power grid, the requirement of modularization and integration of network equipment is more and more urgent. A real-time all-digital simulator of PLL runs in natural time and reproduces the dynamic behavior of the system in real time.

So far, there are two main commercial tools of PLL simulation[5][6]: 1) offline simulation program (e.g., Matlab/Simulink, PSCAD-EMTDC and ATP-EMTP, etc.); 2) online simulation platform (e.g., RT-LAD, RTDS, etc.). Compared with them, the field-programmable gate array (FPGA) platform has strong parallel computing performance and can achieve the RT digital simulation of PLL in a more low-cost and low-voltage way[7][8][9], which meet the simulation requirements of control loop in modern power grid[10].

This paper constructs a low-cost all-digital PLL (ADPLL) on an embedded FPGA platform for real-time (RT) digital simulation. Meanwhile, an improved simulation architecture construction method based on Algorithm Architecture Adequation (A-A-A) is presented. This method makes full
use of timing sequence to find the optimal balance between saving internal hardware resources and
making full use of the parallel computing ability of FPGA.

2. Modeling

The block diagram of ADPLL is shown in Figure 1. As describe in Figure 1, there are three
components in the ADPLL loop: phase detector (PD), loop filter (LPF) and voltage-controlled
oscillator (VCO). The input of the PLL is the voltage of the grid, which can be represented as:

\[
\begin{bmatrix}
U_a \\
U_b \\
U_c
\end{bmatrix} =
\begin{bmatrix}
V_m \sin(\theta_0) \\
V_m \sin(\theta_0 + \frac{2\pi}{3}) \\
V_m \sin(\theta_0 - \frac{2\pi}{3})
\end{bmatrix}.
\]

The component of PD is the “abc-dq” transformation, and the output can be represented as:

\[U_d = \sin(\theta_0 - \theta).\]  

The output phase (\(\theta\)) can track the input phase by setting the reference value (\(U_d^*\)) to “0”. The PI
controller is chosen as the LPF, which can be represented in a form of transfer function as:

\[L(s) = K_p + \frac{K_i}{s}.\]

In order to facilitate digital implementation, it is discretized by trapezoidal difference method. A
general expression of LPF after discretization can be written as:

\[u_{LPF}(k) = A_1 e_{LPF}(k) + A_2 e_{LPF}(k-1) + A_3 u_{LPF}(k-1).\]

Where \(A_1 = K_p + \frac{\Delta t}{2} K_i\), \(A_2 = \frac{\Delta t}{2} K_i - K_p\), \(A_3 = 1\), \(e_{LPF}(*)\) and \(u_{LPF}(*)\) are the input
and output of LPF at instant *, respectively, and \(\Delta t\) is the simulation step of the simulator. Similarly, the
discrete expression of VCO element can be obtained. Furthermore, for digital realization, the output of
ADPLL at each instant is stored in the embedded FIFO memory for the next step calculation.
3. RT Simulation Architecture

In A-A-A methodology, the execution of each operation by an operator consists in reading the operation’s input data from the operator memory, then in combining them to compute the output data which are finally written into the operator memory[11]. The hardware architecture diagram of transformation abc – αβ and LPF are shown in Figure 2. As shown in Figure 2 and Figure 3, the controllable registers have been inserted among the operators. The data transfers are regulated by a sequencer, which is a finite-state machine that synchronizes with the system clock. Moreover, in order to save the internal hardware resources (such as multipliers and adders), a time-division multiplexing (TDM) data path has been defined. The data that is not used by the operator is stored in a register and read out for parallel operation at the next step. As a result, the calculation can be done in a low-cost way without compromising the efficiency of the calculation.

Figure 2: Block diagram of abc – αβ.

Figure 3: Block diagram of LPF.

The block diagram of the overall system is shown in Figure 4. As shown in Figure 4, The large task has been broken down into small modules and calculated separately, and each small module is
configured with a sequencer. At the same time, the sequencer equipped in the top module is responsible for managing the execution sequence of the lower level sequencer.

4. Experimental results

The ADPLL system is constructed based on an embedded FPGA ALTERA Stratix V. The values of parameters are: \( K_p = 2.85, K_i = 445, V_m = 120V, \omega_n = 314\text{rad/s} \) and the sample interval is \( 2\mu\text{s} \) (with a 50-MHz system clock). The PLL has also been constructed on Simulink for comparison, and the result is shown in Figure 5. In the proposed manner, the simulator has the same precision as Simulink. The signal source in flexible power system inevitably contain high harmonics. As shown in Figure 6, the tracking performance of the ADPLL is also strong.
5. Conclusions
In this paper, a low-cost ADPLL based on FPGA has been constructed for RT digital simulation. The phase information catcher can be applied in the field to provide a strong support for the control process of the power system in real time. Meanwhile, an improved economic simulation architecture construction method is presented for making full use of the parallel computing capability of FPGA. Analysis and experimental results show that the proposed modeling approach can achieve the same precision as the offline simulation software. Moreover, the ADPLL also has the strong tracking performance in the case of adding higher harmonics. In addition, the parallel computing performance of FPGA can be further developed to be applied in the field of large-scale power system simulation.

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