An ultra-low leakage energy efficient level shifter with wide conversion range

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Abstract An ultra-low leakage energy efficient level shifter that can convert extremely low input voltage into the supply voltage level is presented in this paper. In order to reduce the leakage power dissipation, the super-cut-off mechanism and MTCMOS technique are utilized in the proposed structure. At the same time, a positive feedback circuit is inserted to avoid the loss of performance. Post-layout simulation results in a 55-nm MTCMOS process demonstrate that for the voltage level conversion from 0.3V to 1.2V, the proposed level shifter exhibits a propagation delay of 70.77ns and an energy per transition of 89.55fJ for input frequency of 1MHz. Meanwhile, the static power of the proposed level shifter is as low as 27.82pW. The proposed level shifter only occupies 7.79um\textsuperscript{2}, which demonstrates prominent area efficiency.

key words: level shifter, leakage power reduction, wide conversion range, sub-threshold operation, MTCMOS.

Classification: Integrated circuits (logic)

1. Introduction

In recent years, power consumption becomes the critical limitation in an increasing number of applications [1 - 3], and one of the most effective ways to reduce power consumption is lowering the power supply voltage [4 - 7]. Hence, voltage scaling technique has been widely adopted in low-power design [8 - 11]. Aggressive voltage scaling into the sub-threshold region would provide better energy efficiency. But when the voltage scaling technique is utilized for sub/near-threshold operation, the sub-to-supra threshold level conversion is usually unavoidable. Therefore, a wide range energy efficient level shifter is highly demanded for voltage scaling systems. Once the system operates at a low speed such as battery-less processors [12, 13], the leakage power becomes the major concern. Fig. 1(a) shows one of the conventional level shifters which uses cross-coupled PMOS devices to achieve low-to-high voltage conversion. The cross-coupled based level shifter consists of a half latch structure and consumes near-zero leakage current owing to its complementary pull-up and pull-down networks. The major drawback of this kind of level shifter is the strong contention between pull-up and pull-down networks. Once the VDDL drops to sub-threshold region, the pull-down transistors would be too weak to overcome the strength of the pull-up transistors. Although upsizing the pull-down transistors could increase the pull-down strength, previous works [14 - 16] show that the required NMOS-to-PMOS ratio grows exponentially in the sub-threshold region, which is unacceptable. Fig. 1(b) shows the other conventional level shifter based on current-mirror PMOS devices. It utilizes a current-mirror instead of the cross-coupled architecture to avoid the contention between pull-up and pull-down networks. Unfortunately, when the voltage of IN is high, the large standby current passing through MP1 and MN1 would result in large standby power.

To realize robust conversions between large supply voltage differences, several level shifters have been proposed [15 - 32]. In order to balance the strength of the pull-up and pull-down networks in cross-coupled based level shifter, in [18, 26], diode current limiters are inserted in the pull-up networks to reduce the pull-up strength. Another way to reduce the strength of pull-up networks is to insert current generators in pull-up networks shown in [23]. As for the large standby power of the current-mirror based level shifter, feedback circuits are usually inserted to cut-off the static on-current [16, 21, 22, 25, 28, 31].

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The above-mentioned level shifters could provide robust conversions in sub-threshold regions, but the static power is still hundreds or thousands pW, which is a huge expense in battery-less systems. In this paper, an ultra-low leakage level shifter with wide conversion range is presented. With the employment of super-cut-off mechanism and MTCMOS, the static power decreases to 27.82pW for a 0.3V to 1.2V voltage conversion.

The rest of the paper is organized as follows: Section 2 describes the structure of the proposed level shifter. Section 3 displays the simulation results and comparisons with other state-of-the-art level shifters. Finally, Section 4 draws a conclusion.

2. Proposed level shifter

The proposed level shifter is shown in Fig. 2. The main voltage conversion stage is cross-coupled based. Two PMOS-diode current limiters (MP3, MP4) are inserted to reduce the strength of the pull-up networks. As shown in Fig.3, if the PMOS-diode current limiters are not applied, the pull-down networks are too weak to overcome the strength of the pull-up transistors at VDDL = 0.4V. On the contrary, the level shifter could work correctly even if the VDDL is as low as 100mV once the current limiters are applied. To optimize the leakage and the delay of the proposed level shifter, several strategies have been applied to the proposed design.

In order to realize a wide conversion range, the pull-down networks need to employ relatively large low threshold NMOS transistors. As is well known that low threshold transistors usually lead to significant leakage power. Fig. 4 exhibits the leakage current of the minimum size low threshold NMOS as a function of V_{GS} at V_{Drain} = 1.2V. From the leakage current result, it is obvious that the transistor would be placed in a super-cut-off state and consumes much less leakage power once the V_{GS} is reduced to below -100mV. In our design, the input inverter is split to two asymmetric inverters to drive MN1 and MN2 independently, respectively, to improve the speed of the level shifter. When the voltage of IN is VSS, the weak PMOS MP5 will charge the node N5 to VDDL, and the transistor MN1 will be placed in super-cut-off state. Similarly, when the voltage of IN is VDDL, the node N6 will be discharged to VSS through the weak NMOS MN5, and the transistor MN2 will be placed in super-cut-off state. As a result, the leakage power is greatly reduced. To remedy the loss of speed due to the stack structure (MN1 and MN4), a small feedback transistor MN3 is inserted, when the voltage of IN is VDDL, the pull-down network will discharge the node N2 to below VDDH, and the voltage of node N4 will gradually rise to supra-threshold, then the feedback transistor MN3 will significantly improve the strength of the pull-down network, which will greatly speed up the conversion. As shown in Fig.5, the voltage of N2 can drop faster when the feedback transistor MN3 is applied. As a result, the Low to High conversion is speeded up.

The proposed level shifter is further optimized through
the MTCMOS technique and sub-threshold device sizing. To decrease the leakage power, the cross-coupled PMOS MP1 and MP2 are implemented with HVT transistors. The PMOS-diode current limiters are implemented with LVT transistors because the voltage difference between node N2/N4 and VDDH will significantly influence the leakage power of MP2/MP1. With the employment of LVT transistors, the voltage difference could be greatly eliminated. With the employment of PMOS current limiters, the node N1 could charge to VDDH, but could not discharge to VSS. Similarly, the node N2 could discharge to VSS but could not charge to VDDH. To optimize leakage power of the output inverter, the input of the inverter is split to two node N1 and N2 so that the inverter could cut-off no matter the output is VDDH or VSS, meanwhile, HVT transistors are employed.

The level shifter operates as follows: When the input IN changes from Low to High (VSS to VDDL), MN4 and MN1 are switched on and MN2 is switched off. The voltage of N2 begins to drop and MP2 is switched on. Then the voltage of N3 and N4 begins to rise and MP1 is switched off gradually. As MP1 is switched off, the voltage of N1 and N2 is further reduced until the voltage of N2 falls to VSS. As the voltage of node N4 could rise to supra-threshold quickly, the feedback transistor MN3 could speed up the falling transition of N1 and N2. Finally, MP7 is switched on and MN6 is switched off, the voltage of OUT is charged to VDDH quickly. When IN changes from High to Low (VDDL to VSS), MN2 is switched on and MN1 is switched off. The voltage of N4 begins to drop and MP1 is switched on. Then the voltage of N1 and N2 begins to rise and MP2 is switched off gradually. The voltage of N1 could rise to VDDH as MN1 is off. Finally, MN6 is switched on and MP7 is switched off, the voltage of OUT falls to VSS quickly. Since MN1 and MN2 are switched on with different inputs, the connections of MN1 and MN2 are different. MN2 adopts a pass-transistor structure to speed up the falling transition. Fig.6 shows the transient waveform of the proposed level shifter in the detail.

In order to verify the performance of the proposed level shifter, the proposed level shifter has been simulated in a SMIC 55nm MTCMOS technology. Fig. 7 shows the layout of the proposed level shifter with the core area as compact as 7.79um² (4.96um * 1.57um). The following simulation results are based on post-layout analysis. Three PVT corners should be determined with care for sub-threshold level shifters. The typical case in our design includes typical NMOS, typical PMOS, a VDDH supply voltage of 1.2V and a temperature of 25°C. As discussed in previous sections, the pull-down networks need to overcome the strength of the PMOS transistors, thus, the slow-NMOS fast-PMOS is the worst corner of the sub-to-supa threshold level shifter. Moreover, a 10% VDDH supply voltage increase (1.32V) and a temperature of -40°C are selected to further weaken the conversion. Correspondingly, the best case includes fast-NMOS, slow-PMOS, a 10% VDDH supply voltage reduction (1.08V) and a temperature of 125°C.

3.1 Conversion range
To investigate the conversion range of the proposed level shifter, several 500-iteration Monte Carlo simulations have been performed at a 10% VDDH supply voltage increase (1.32V), a temperature of -40°C. The VDDL supply voltage is set to be between 0.1V and 0.2V with a step size of 0.01V. The result shown in Fig. 8 illustrates that the proposed level shifter could operate at VDDL as low as 0.12V under extreme PVT corners.
3.2 Static power
The static power dissipation against VDDL is illustrated in Fig. 9. When the VDDL scales down, the static power decreases as expected. But the static power increases when the VDDL scales down to 0.1V, which is mainly due to the fact that the super-cut-off mechanism is weakened while the $V_{GS}$ is only -100mV. The proposed level shifter consumes 27.82pW of static power for the voltage level conversion from 0.3V to 1.2V at the typical case. This is attributed to the employment of the super-cut-off mechanism, the MTCMOS technique and the split output inverter as discussed in Section 2. Both MTCMOS technique and split inverter are mainly used to decrease the voltage drop of the internal node. The super-cut-off mechanism is used to suppress leakage current of the LVT pull-down networks. To evaluate the effect of each optimization strategy, Table I shows the static power consumption of cross-coupled based level shifters with different optimization strategies. The static power could be reduced to several hundred pW with MTCMOS technique and split inverter. When the super-cut-off mechanism is applied, the static power is further reduced to as low as 27.82pW.

### Table I. Static power of cross-coupled based level shifters with different strategies. (0.3V to 1.2V voltage conversion)

| Strategy | No | HVT-diode CL | LVT-diode CL | LVT-diode CL + SI | Super cut-off CL + SI |
|----------|----|--------------|--------------|------------------|---------------------|
| Static power (pW) | fail | 1997.63 | 603.75 | 570.99 | 27.82 |
| Norm. | --- | 71.8 | 21.7 | 20.52 | 1 |

*: CL = current limiter, SI = split inverter.

![Fig. 9 Static power at typical case as a function of VDDL.](image9.png)

![Fig. 10 Propagation delay as a function of VDDL.](image10.png)

3.3 Delay and energy per transition
The post-layout simulations have been performed for three PVT corners. The input signal frequency is 1MHz with a transition time of 10 ns. In addition, the output capacitance is fixed at 0.1 pF.

The propagation delay of the proposed level shifter against the low supply voltage (VDDL) is shown in Fig. 10. The propagation delay grows exponentially with VDDL scales into the sub-threshold regions. The observed phenomenon is more severe at the worst case. This is mainly because when transistors work in the weak inversion region, the operating current is dominated by the leakage current, which is significantly affected by the temperature. At 300mV, the worst case delay is 63 times higher than the best case delay, and at 200mV, the factor increases to 461. While the VDDL drops to 100mV, the worst case delay becomes 1168 times higher than the best case delay. Still, the proposed level shifter operates accurately across the simulated PVT corners. In addition, the delay of the proposed level shifter is 70.77ns when VDDL is 0.3V, which is comparable to other state-of-the-art level shifters.

Fig. 11 shows the energy per transition as a function of VDDL at the typical case. The energy per transition decreases relatively slowly while the VDDL scales down. But as the VDDL scales into the deep sub-threshold regions, the energy per transition appears to rise. This is due to the exponentially increasing propagation delay, which introduces enormous internal short-circuit power. The optimized energy consumption is obtained between 0.5V and 0.7V. For a low supply voltage of 0.3V, the proposed level shifter achieves 89.55fJ energy per transition in the typical case.

3.4 Comparison
In order to validate the benefits of the proposed level shifter, a comparative analysis of the proposed level shifter and some other state-of-the-art level shifters has been performed. It can be seen in Table II that the proposed level shifter has the smallest static power among recently published designs. With the employment of the super-cut-off mechanism and the MTCMOS technique, the proposed level shifter consumes only...
27.82pW of static power, far less than other level shifters. The energy per transition of the proposed level shifter is similar to other level shifters while the input signal frequency is 1MHz. If the speed is decreased to sub-KHz, which is widely used in battery-less systems, the proposed level shifter could provide a much smaller energy per transition than other level shifters due to the ultra-low static power. As for the propagation delay, to remedy the loss of speed due to the stack structure, a small feedback transistor is inserted. As a result, the propagation delay of the proposed level shifter is still comparable to other level shifters.

| Table II. Performance summary and comparison. |
| Tech. | Min. VDDL | Delay (ns) | Energy/transition (pJ) | $P_{\text{static}}$ (pW) | Area (um$^2$) |
|-------|-----------|----------|------------------------|----------------------|------------|
| TCAS-II 2010 [16]$^*$ | 65nm | 0.1 | 17.5 @ 0.3~1.2 | 552 @ 0.3V | 20400 | 9.94 |
| TCAS-1 2014 [24] | 65nm | 0.2 | 162 @ 0.3~1.2 | 136 @ 0.3V | 4056 | 16.8 |
| VLSI 2015 [32] | 90nm | 0.1 | 16.6 @ 0.2~1.2 | 77 @ 0.2V | 8700 | 37.3 |
| VLSI 2017 [19] | 40nm | 0.2 | 66.48 @ 0.3~1.1 | 72.3 @ 0.3V | 88.4 | 11.92 |
| TCAS-II 2018 [25] | 65nm | 0.1 | 7.5 @ 0.3~1.2 | 123.8 @ 0.3V | 2840 | 7.45 |
| This work | 55nm | 0.12 | 70.77 @ 0.3~1.2 | 89.55 @ 0.3V | 27.82 | 7.79 |

$^*$: re-implemented in [25].

4. Conclusion

In this paper, an ultra-low leakage energy efficient level shifter that can convert extremely low input voltage into the supply voltage level is presented. To get a wide conversion range, two PMOS-diode current limiters are inserted to reduce the strength of the pull-up networks. With the employment of the super-cut-off mechanism and the MTCMOS technique, the leakage power of the proposed level shifter is greatly reduced. At the same time, a positive feedback circuit is inserted to avoid the loss of performance. Post-layout simulation results using a 55nm MTCMOS demonstrate that the proposed level shifter could convert an extremely low input voltage of 0.12V to the supply voltage of 1.2V. For the voltage level conversion from 0.3V to 1.2V, the proposed level shifter exhibits a propagation delay of 70.77ns and an energy per transition of 89.55fJ for input frequency of 1MHz. Meanwhile, the static power of the proposed level shifter is 27.82pW. In addition, the proposed level shifter occupies only 7.79um$^2$, which demonstrates prominent area efficiency. Therefore, the proposed level shifter is appropriate for digital systems where multiple aggressively scaled voltage domains are employed, especially for these systems where the leakage power is the major concern.

Acknowledgments

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