Increasing integration scale of superconductor electronics beyond one million Josephson junctions

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Abstract. We review the existing fabrication processes for superconductor digital electronics and describe approaches to increasing the scale of integration of superconducting digital circuits from the current level of about one million Josephson junctions (JJs) on a 1-cm\textsuperscript{2} chip toward ten million JJs per chip. We present designs of ac-clocked Single Flux Quantum (SFQ) shift registers, convenient benchmarking circuits, in a 250-nm-linewidth superconductor electronics fabrication process developed recently at MIT Lincoln Laboratory (MIT LL). For shift registers using resistively shunted JJs with Josephson critical current density, \(J_c\) of 100 \(\mu\text{A}/\mu\text{m}^2\), we achieved a record-high circuit density of \(4.2 \times 10^6\) JJs per \(\text{cm}^2\), a factor of three higher than the previous record obtained in the MIT LL 350-nm-linewidth SFQ5ee process. Using self-shunted JJs with \(J_c\) of 600 \(\mu\text{A}/\mu\text{m}^2\), we increased this record circuit density to \(7.4 \times 10^6\) JJs per \(\text{cm}^2\).

1. Introduction
Superconductor electronics could become a technology of choice for energy efficient high performance computing, quantum information processing, advanced sensing and imaging, etc., if a very large scale of integration (VLSI) can be achieved in order to deliver the required functionality and performance. Recent progress in fabrication technology at MIT Lincoln Laboratory (MIT LL) \cite{1}-\cite{4} enabled demonstration of circuits with about one million Josephson junctions (JJs) \cite{5}, \cite{6}, a device count usually viewed as VLSI threshold. For increasing the integration scale, two new processes have been recently demonstrated \cite{7}-\cite{9}. The first one is the PSE2 process with two layers of Nb/Al/AlO\textsubscript{x}/Nb junctions and two layers of resistors, a layer of Mo\textsubscript{2}N kinetic inductors, and six Nb wiring layers \cite{7}. A special node of this process integrates magnetic \(\pi\)-junctions of the SFS-type on one JJ layer with Nb/Al/AlO\textsubscript{x}/Nb JJs on another layer. The second is the SC1 process \cite{8} with 250-nm linewidth \cite{9}. This process can also utilize self-shunted Nb/Al/AlO\textsubscript{x}/Nb JJs with high critical current density, \(J_c\), and kinetic inductors \cite{3}, \cite{4}.

In \cite{5}, \cite{6} we introduced scalable ac-biased shift registers and demonstrated their use to benchmark the progress in integration scale and fabrication technology. These shift registers contain four Josephson junctions per unit cell (bit), and operating margins of each individual bit can be tested independently, providing information on the process uniformity and yield, statistics of JJs and inductors. The shift registers were demonstrated in several process nodes of the SFQ*ee fabrication process developed at MIT-LL, which differ mainly by the minimum linewidth of inductors and shunt resistors, and the Josephson critical current density of Nb/Al/AlO\textsubscript{x}/Nb Josephson junctions (JJs). With...
the progress in fabrication technology, the size of a 4-junction unit cell (circuit pitch) of the shift registers was decreased from 17 µm x 40 µm in the SFQ4ee process with 0.5-µm linewidth to 15 µm x 20 µm in the SFQ5ee process with 0.35-µm linewidth, and to 10 µm x 15 µm in the SFQ5ee process with self-shunted junctions (also known as the SFQ5hs process) [6]. The largest shift register circuit demonstrated in the SFQ5ee process had about $8.1 \times 10^5$ JJs and the circuit density of $1.33 \times 10^6$ JJs per cm².

Random access memory (RAM) is another type of benchmark circuits for assessing the progress in superconductor electronics fabrication technology. Recently, using the SFQ5hs process with self-shunted JJs and 0.35-µm inductor linewidth, we demonstrated 72-bit arrays of vortex transitional (VT) memory cells with the record density of about $4 \times 10^6$ JJs per cm² [10].

In order to investigate relationships between the integration scale and the minimum feature size and other process features in superconductor electronics, we redesigned the ac-biased shift register used in [5], [6] in the new SC1 process [7] that offers 250-nm minimum linewidth for inductors and 400-nm minimum linewidth for shunt resistors. We also designed the same shift register using high-$J_c$ self-shunted junctions eliminating the need for shunt resistors.

2. Results

2.1. Shift register unit cell with resistively shunted junctions

The circuit diagram of a unit cell (single bit) of an ac-clocked (ac-biased) shift register is shown in Figure 1 and is similar to the previously described ac-biased shift registers; see Fig. 5 in [5] and Fig. 1a in [6]. The shift register operates as follows. A positive current (flowing to the right in Figure 1) in the primary of the clock transformer, $M$ induces a current flowing to the left in the secondary of the transformer and positively biases junctions $J_1$ and $J_2$, causing a single flux quantum encoding “1” to shift from the first loop of the cell formed by JJs $J_1$, $J_2$ and inductors $L_2$–$L_3$ to the second loop formed by $J_3$, $J_4$, $L_5$ and $L_6$. On the negative half-period of the ac clock, the current in the secondary of the transformer flows to the right and positively biases junctions $J_3$ and $J_4$, shifting the flux out of the second loop to the next cell of the shift register. For the new SC1 process, we re-optimized parameters of all components of the unit cell.

The layout of the ac-clocked shift register unit cell (shift register bit) in the SC1 process is shown in Figure 2 below. The cell dimensions setting a multi-bit shift register pitch are 12 µm x 8 µm. This is a factor of three reduction in the cell area in comparison to the SFQ5ee process [5], [6].

2.1.1. Circuit density. With the unit cell area of 96 µm² (including ground plane moats for flux trapping mitigation), as shown in Figure 2, the shift register circuit density is $4.2 \times 10^6$ JJs per cm². This slightly exceeds the circuit density we recently demonstrated in RAM circuits with self-shunted JJs [10] and sets a new record. At this density, the junction count in a shift register circuit occupying the entire 1-cm² chip (including a periphery array of 200 contact pads and input/output circuitry) exceeds three million, a device count in Intel’s Pentium II processor. It was necessary to use meandered inductors, e.g., $L_2$, $L_5$, $L_8$, and transformer $M$ in order to provide the proper inductance and mutual inductance values of the inductors connecting closely spaced junctions in the shift register. Although necessary, this generally increases the cell area. As can be seen in Figure 2, the total area of the inductors and the transformer is noticeably larger than the area of the Josephson junctions. This indicates that the process node used is inductor-limited, in the terminology of [11]. Ideally, to
maximize the circuit density, we would like to balance the densities of JJs and inductors because, on average, one JJ requires one inductor.

Figure 2. Layout of the shift register cell shown in Figure 1 in the SC1 process. Shunt resistors damping junctions $J_1$–$J_4$ are labeled R1–R4, respectively. The layout closely follows the circuit diagram. The latter does not show the external shunt resistors explicitly to be applicable also to the case of self-shunted, high-$J_c$ junctions. The cell dimensions are 12 µm by 8 µm.

2.2. Shift register unit cell with self-shunted junctions

Implementation of self-shunted junctions allows for a significant increase in the circuit density by eliminating external shunt resistors. As was demonstrated in [3], [9], a sufficient self-shunting in Nb/Al/AlO$_x$/Nb junctions is reached at $J_c=600$ µA/µm$^2$ giving junctions with the Stewart-McCumber damping parameter $\beta_c \approx 2$. Previously, we have successfully implemented junctions with this $J_c$ in RAM circuits [10]. The 100-µA/µm$^2$ JJs can be simply replaced by 600-µA/µm$^2$ junctions in a way preserving all values of junction critical currents, $I_c$, and circuit inductors. The junction diameter would need to be reduced by a factor of $\sqrt{6}$, from 1.32 µm used in the circuit in Sec. 2.1 to 0.54 µm. The latter is possible in the current technology, but using somewhat larger JJs with higher critical currents permits reducing values of the cell inductors and of their area. Also, high-$J_c$ junctions have a larger specific capacitance than 100-µA/µm$^2$ JJs [3]. Therefore, we increased $I_c$ of the junctions $J_1$–$J_4$ to 250 µA and completely re-optimized the shift register for the SC1 process with $J_c=600$ µA/µm$^2$.

Figure 3. Layouts of the shift register unit cell using self-shunted JJs with $J_c=600$ µA/µm$^2$ (a) and resistively shunted junctions with $J_c=100$ µA/µm$^2$ (b). Both layouts use the same inductor linewidth and are given in the same scale. Parameters of the cell (a) with self-shunted junctions are: $J_1=J_2=J_3=J_4=250$ µA, $L_1=0.82$ pH, $L_2=3.80$ pH, $L_3=0.08$ pH, $L_4=2.09$ pH, $L_5=4.17$ pH, $L_6=0.08$ pH, $L_7=0.77$ pH, $L_8=8.45$ pH, $M=1.27$ pH. Only inductors $L_2$ and $L_5$ are marked in (a) for clarity. White bars show the scale.
The cell layout with self-shunted junctions is shown in Figure 3. For a comparison, the cell using resistive shunted junctions is also shown in the same scale. The new cell dimensions are 9 µm by 6 µm, giving a factor of two reduction in the cell area with respect to the cell for $J_c = 100 \, \mu\text{A}/\mu\text{m}^2$. The unit cell area of 54 µm$^2$ translates in the shift register circuit density of $7.4 \times 10^6$ JJs per cm$^2$. This record-high density is a factor of two higher than our previous record obtained on Josephson random access memory circuits [10].

3. Conclusion
This work has shown that the circuit density and the device count in superconductor digital circuits can be tripled in comparison with the current state-of-the-art by utilizing the 250-nm-linewidth SC1 process with $J_c = 100 \, \mu\text{A}/\mu\text{m}^2$ [7], a process similar to the widely-used SFQ5ee process but offering smaller feature sizes for inductors and shunt resistors. With resistively shunted junctions with $J_c = 100 \, \mu\text{A}/\mu\text{m}^2$, the SC1 process enables superconducting circuits with junction count over four million JJs per cm$^2$. Implementation of the self-shunted Nb/Al/AlOx/Nb JJs with $J_c = 600 \, \mu\text{A}/\mu\text{m}^2$ instead of resistively shunted JJs allows to increase circuit density typically by a factor of two for the same type circuits, e.g., up to $7.4 \times 10^6$ JJs per cm$^2$ for the ac-clocked shift registers. The results of our designs agree with the estimates in [9] and [11] on the maximum circuit density and device count achievable in various nodes of superconductor electronics fabrication processes.

Even higher circuit densities can be achieved by reducing further the area of inductors. This requires inductors with higher inductance per unit area and can be achieved by increasing kinetic inductance contribution to the total inductance, e.g., by reducing Nb inductor linewidth further and/or thickness below the current 200-nm film thickness. A process for 200 nm and 180 nm inductors is currently under development using 193-nm photolithography.

As the next step in demonstrating functioning circuits with a few millions of Josephson junctions, we have designed multibit ac-clocked shift registers on 5 mm x 5 mm chips for both $J_c = 100 \, \mu\text{A}/\mu\text{m}^2$ and 600 µA/µm² using the cells presented above. These initial circuits have over 361600 Josephson junctions and are currently in fabrication.

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