Low-Latency VLSI Architectures for Modular Polynomial Multiplication via Fast Filtering and Applications to Lattice-Based Cryptography

Weihang Tan, Student Member, IEEE; Antian Wang, Student Member, IEEE; Yingjie Lao, Member, IEEE; Xinmiao Zhang, Senior Member, IEEE; and Keshab K. Parhi, Fellow, IEEE

Abstract—This paper presents a low-latency hardware accelerator for modular polynomial multiplication for lattice-based post-quantum cryptography and homomorphic encryption applications. The proposed novel modular polynomial multiplier exploits the fast finite impulse response (FIR) filter architecture to reduce the computational complexity for the schoolbook modular polynomial multiplication. We also extend this structure to fast $M$-parallel architectures while achieving low-latency, high-speed, and full hardware utilization. We comprehensively evaluate the performance of the proposed architectures under various polynomial settings as well as in the Saber scheme for post-quantum cryptography as a case study. The experimental results show that our design reduces the computational time and area-time product by 61% and 32%, respectively, compared to the state-of-the-art designs.

Index Terms—Parallel Modular Polynomial Multiplication, Low-Latency, Fast Filtering, VLSI Architecture, Polyphase Decomposition, Homomorphic Encryption, Post-Quantum Cryptography, Lattice-Based Cryptography.

1 INTRODUCTION

MODULAR polynomial multiplication is commonly used in lattice-based post-quantum cryptography (PQC) and homomorphic encryption applications. While homomorphic encryption aims at allowing computations to be directly carried out in the encrypted domain without decryption, lattice-based cryptographic algorithms are also designed to be resistant against attacks from both traditional and quantum computers and are thus well suited for PQC. Three out of the four finalists for the ongoing NIST PQC standard in round-3 fall into this category of lattice-based cryptography. Specifically, the lattice-based schemes can be classified as either NTRU-based (e.g., NTRU), and learning with errors-based (LWE) (e.g., Crystals-Kyber and Saber). In prior works, the modular polynomial multiplication for the lattice-based cryptography scheme has mostly been implemented by schoolbook polynomial multiplication, number theoretic transform (NTT) or the Katsuha multiplication. Different from the prior works, this paper proposes a novel low-latency architecture by exploiting the fast finite impulse response (FIR) parallel filter architecture. The paper also proposes a novel weight-stationary systolic array for modular polynomial multiplication; these are used as building blocks for the fast parallel architecture. The proposed architecture is feed-forward and can be pipelined at arbitrary levels to achieve desired speed. To the best of our knowledge, this is the first paper to utilize the fast parallel filter architecture to accelerate the modular polynomial multiplication for the lattice-based schemes.

Exploiting the fast parallel filter approach to modular polynomial multiplication is neither straightforward nor trivial. Since the fast parallel filters contain several subfilters and merging operations, the modular operations must be incorporated at the subfilter level and at the merging level. No prior work has addressed these design aspects. The subfilters should correspond to single-input single-output architectures that should integrate the modular operation and should operate in real-time with no hardware under-utilization. These should also require simpler control circuits. Such designs have not been presented before.

The contributions of this paper are four-fold. First, using systolic mapping methodology, we derive a sequential weight-stationary systolic array for modular polynomial operation. This structure is partly similar to the transpose-form FIR digital filter and is the main building block of the proposed architecture. The low-latency systolic array achieves full hardware utilization. Second, we propose a low-latency fast modular polynomial multiplication architecture that integrates the modular reduction at the merging level, achieves full hardware utilization, and minimizes latency. Third, using iterated fast parallel filter design approach, we propose highly parallel architectures where the level of parallelism is the product of short lengths. The modular operation is also carried out at the merging step of each iteration to reduce overall latency and achieve full hardware utilization. Fourth, the advantages of the proposed architecture are demonstrated using the Saber scheme as a PQC benchmark.

Compared to prior parallel architectures in [6], the proposed fast $M$-parallel architecture has 50% less overhead under the same degree of latency reduction. As most lattice-based PQC schemes involve a relatively large number of polynomial multiplications, the proposed architecture can significantly accelerate the over-
all computation. This architecture requires fewer post-processing operations than the Karatsuba algorithm \[16\]. The experimental result shows that the proposed fast 4-parallel architecture has the lowest actual latency compared with prior works \[6\], \[17\], \[18\].

The rest of the paper is organized as follows: Section 2 reviews the mathematical background and the prior works on the modular polynomial multiplication. Section 3 and Section 4 present the details of the proposed hardware architecture, including the modular polynomial multiplier, and fast M-parallel architecture. Section 5 describes the experimental results and comparisons with the state-of-the-art designs. Finally, Section 6 concludes the paper.

2 BACKGROUND AND RELATED WORK

Since this paper targets the schoolbook polynomial multiplication, we briefly review the essential notations, mathematical background, and related works of the schoolbook polynomial multiplication.

2.1 Lattice-based cryptography

Lattice-based cryptography relies on the NP-hard lattice problems that even quantum computers cannot solve efficiently. One example of the lattice problems is the shortest vector problem (SVP), whose security relies on the hardness of approximating SVP in the Euclidean norm \[1\]. Modular polynomial multiplication is a fundamental and yet the most computationally intensive operation of lattice-based cryptography. For the lattice-based PQC, modular polynomial multiplication dominates the computations across key-generation, encryption, and decryption steps. Similarly, the most expensive operation for homomorphic encryption schemes is also the modular polynomial multiplication. Therefore, improving the efficiency of modular polynomial multiplication is critical to the practical deployments of lattice-based cryptosystems and homomorphic encryption.

2.2 Modular polynomial multiplication

For the product \( P(x) \) of two polynomials
\[
A(x) = a[0] + a[1]x + a[2]x^2 + \ldots + a[n-1]x^{n-1},
\]
\[
B(x) = b[0] + b[1]x + b[2]x^2 + \ldots + b[n-1]x^{n-1},
\]
over \( R_q \), all the coefficients of \( P(x) \) need to be less than \( q \) but non-negative integers, while the degree of \( P(x) \) should be less than \( n \), where \( R_q = \mathbb{Z}_q/(x^n + 1) \) is the ring of the polynomial, and \( \mathbb{Z}_q \) is the ring of integers modulo a power-of-two integer \( q \). The schoolbook polynomial multiplication between \( A(x) \) and \( B(x) \) modulo \( (x^n + 1, q) \) can be described as
\[
A(x) \cdot B(x) = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} a[i]b[j]x^{i+j} \mod (x^n + 1, q)
\]
\[
= \sum_{i=0}^{n-1} \left( \sum_{j=0}^{n-1} (-1)^{(i+j)/n} a[i]b[j] \mod q \right) \cdot x^{(i+j) \mod n}.
\]

For the schoolbook modular polynomial multiplication, the moduli are not required to be prime, which is different from the NTT-based polynomial multiplication. Consequently, the polynomial multiplication used in the module-learning with rounding (M-LWR) problem \[19\] and ring-learning with errors (R-LWE) problem \[20\] can benefit from these moduli. In this case, since all the moduli can be selected as power-of-two integers, the modular reduction for the coefficients on the schoolbook polynomial multiplication can be simply performed by keeping the least significant \( \epsilon \) bits (\( \epsilon \) is the bit-length of the modulus \( q \), i.e., \( \epsilon = \lceil \log_2(q) \rceil \)) instead of using the expensive Barrett reduction \[21\] or Montgomery modular multiplication \[22\]. Meanwhile, schemes based on the M-LWR problem (such as the Saber scheme) obtain the error term by rounding, while naturally aligning with the power-of-two modulus. Besides, recent work shows that a power-of-two modulus can simplify and improve the polynomial multiplication for the R-LWE based homomorphic encryption schemes without affecting the computational hardness \[23\]. The modulus in this format has been applied in some popular schemes such as BFV scheme \[24\]. Based on this advantage, shortening the bit-length of the operand and eliminating the modular reduction for the coefficients can increase the resource available which can then enable the designer to increase the level of parallelism to achieve a low-latency modular polynomial multiplier.

However, using the power-of-two moduli cannot leverage the acceleration from the NTT-based polynomial multiplication without further expensive transformation. NTT-based polynomial multiplication has been widely applied in many lattice-based cryptography schemes \[7, 25, 26, 27, 28, 29, 30\]. The concept of NTT is to convert all the coefficients of the polynomials into the NTT-domain, which will then go through a direct coefficient-wise multiplication, and followed by an inverse NTT transform to recover the produced coefficients in the original algebraic domain polynomial. As a result, it can reduce the quadratic complexity \( \mathcal{O}(n^2) \) from the schoolbook polynomial multiplication to \( \mathcal{O}(n \log n) \). Thus, there is a trade-off between utilizing the low-cost PEs based on the power-of-two moduli and the low computational complexity from using the NTT algorithm for the modular polynomial multiplication. The goal of this paper is to leverage the low resource consumption with power-of-two modulus to increase the parallelism for achieving a competitive timing performance without using an \( \mathcal{O}(n \log n) \) computational complexity algorithm.

2.3 Karatsuba polynomial multiplication

To improve the efficiency and reduce the complexity of schoolbook polynomial multiplication, methods based on the divide-and-conquer strategy to increase the parallelism are of great interest. One of the examples is the Karatsuba algorithm \[16\]. The 2-level Karatsuba polynomial multiplication first decomposes the input polynomials into higher-degree and lower-degree parts as \( A(x) = A_0(x) + A_1(x) \cdot x^{n/2} \) and \( B(x) = B_0(x) + B_1(x) \cdot x^{n/2} \) and computes
\[
C_0(x) = A_0(x) \cdot B_0(x)
\]
\[
C_1(x) = (A_0(x) + A_1(x)) \cdot (B_0(x) + B_1(x))
\]
\[
C_2(x) = A_1(x) \cdot B_1(x).
\]

Then the above products are summed up and polynomial modular reduction is carried out to derive the product \( P(x) \) over the ring as
\[
P(x) = C_0(x) + C_3(x) \cdot x^{n/2} + C_2(x) \cdot x^n \mod (x^n + 1),
\]
where
\[
C_3(x) = (C_1(x) - C_0(x) - C_2(x)).
\]
Note that the degrees of $C_3(x) \cdot x^{n/2}$ and $C_2(x) \cdot x^n$ are $3n$ and $2n$, respectively. Hence polynomial subtractions are needed to perform the modular reduction by $x^n + 1$. Based on this divide-and-conquer strategy of the Karatsuba algorithm, the number of coefficient multiplications is reduced from $n^2$ to $3(n/2)^2$.

2.4 Prior hardware implementations

Several hardware accelerators for the lattice-based cryptography without using the NTT algorithm have been proposed recently [6, 7, 18, 31, 32, 33, 34, 35, 38]. As expected, optimizing the polynomial multiplier is the main focus of these works, since it is the bottleneck. The hardware/software co-design for the modular polynomial multiplication accelerator in [31] shows a significant acceleration compared with the software implementation. Subsequently, the work in [18] introduced the compact hardware/software interfacing design, which applies a hybrid method of Toom-Cook multiplication [36] (a variant of Karatsuba algorithm) and a degree-64 schoolbook polynomial multiplier to optimize the modular polynomial multiplication. A full hardware implementation is proposed in [6], which utilizes a memory-based schoolbook polynomial multiplier. This design achieves a higher speed where each degree-256 polynomial multiplication only consumes 256 clock cycles. Furthermore, an 8-level recursive split hierarchical Karatsuba algorithm-based implementation is introduced in [17], which reduces a degree-256 polynomial multiplication to only 81 clock cycles without considering the pipelining startup time. Besides, several architectures of modular polynomial multipliers for the R-LWE schemes are introduced in [8, 34, 37]. The works in [34, 37] investigate the low-area design for the schoolbook modular polynomial multiplication, which only consumes a small amount of LUTs and DSPs. Meanwhile, the design in [8] proposes a modular polynomial multiplier using the Karatsuba algorithm and reduces the complexity by merging the polynomial modular reduction on the post-processing stage of the Karatsuba algorithm.

However, these designs do not consider an architecture using the fast filtering technique to reduce the latency. Also, the architectures based on Karatsuba algorithm generally consider the polynomial modular reduction after the multiplication. These designs do not reduce the number of addition operations. Therefore, it is possible to further reduce the number of additions/subtractions at the post-processing stage thereby reducing the total number of addition/subtraction operations. Since our objective is to improve the speed under a given hardware budget, we define the following two metrics in evaluating the performance from the speed perspective:

- Response time: clock cycles between the first input and first output sample.
- Total latency: clock cycles between the first input and last output sample.

2.5 Case study: modular polynomial multiplication for Saber PQC scheme

We also evaluate and compare the performance of our proposed architectures used in the Saber scheme [5] (one of the finalist PQC candidates), as a case study. Saber is an indistinguishability under chosen-ciphertext attack secure Key Encapsulation Mechanism (KEM), which consists of three algorithms: key generation, encapsulation, and decapsulation [5]. More specifically, the primitive of the Saber scheme is based on the hardness of the M-LWR problem and the use of the Fujisaki-Okamoto transform [38].

Among all the steps in the Saber scheme, the most heavily used functions are the matrix and vector multiplication and inner product of two vectors whose core operation is the entry-entry multiplication, i.e., degree-256 modular polynomial multiplication. For the standard security level Saber, there are 9, 12, and 15 polynomial multiplications in the key generation, encapsulation, and decapsulation, respectively.

3 Modular Polynomial Multiplier based on Weight-Stationary Systolic Array

Consider the design for a degree-$n$ modular polynomial multiplier described by Equation (3). In this section, we use $n = 4$ as an example to illustrate our proposed novel modular polynomial multiplier. The modular polynomial multiplication is described by:

$$
P(x) = A(x) \cdot B(x) \mod (x^4 + 1, q) \tag{7}
$$

where

$$
A(x) = a[0] + a[1]x + a[2]x^2 + a[3]x^3,
B(x) = b[0] + b[1]x + b[2]x^2 + b[3]x^3.
$$

The polynomial multiplication of $A(x)$ and $B(x)$ leads to

$$
P'(x) = p'[0] + p'[1]x + p'[2]x^2 + p'[3]x^3 + p'[4]x^4 + p'[5]x^5 + p'[6]x^6. \tag{8}
$$

Since the polynomial multiplication has a degree higher than three, the terms $x^4$, $x^5$, and $x^6$ are replaced by $-1$, $-x$, and $-x^2$, respectively, to perform the modular reduction. Thus, the coefficients of the modular polynomial multiplication are:

$$
p[3] = a[3]b[0] + a[2]b[1] + a[1]b[2] + a[0]b[3],
p[2] = a[2]b[0] + a[1]b[1] + a[0]b[2] - a[3]b[3],
p[1] = a[1]b[0] + a[0]b[1] - a[3]b[2] - a[2]b[3],
p[0] = a[0]b[0] - a[3]b[1] - a[2]b[2] - a[1]b[3]. \tag{9}
$$

A dependence graph (DG) of the modular polynomial multiplication for the $n = 4$ example is shown in Fig. 1.

![Fig. 1. DG of the modular polynomial multiplication when $n = 4$](image)
3.1 Architecture of modular polynomial multiplier using transpose-form FIR filter

Given the similarity between modular polynomial multiplication and FIR filter, it is useful to consider three common types of FIR filter structures [9], i.e., direct-form, transpose-form, and hybrid-form, respectively, as shown in Fig. 2.

The direct-form FIR filter shown in Fig. 2(a) leads to a long critical path, which consists of one multiplier and $n$ adders. It can also be observed from Fig. 2(c) that the hybrid-form architecture generates its first output immediately after loading the first input, and requires additional registers to store the intermediate results; however the architecture is not feed-forward and has a slightly longer critical path than the transpose-form. Thus, the best choice for implementing polynomial multiplication in lattice-based schemes is the transpose-form as shown in Fig. 2(b) as it has the least critical path and a feed-forward datapath. Fortunately, the DG in Fig. 1 can be mapped to a weight-stationary systolic array using the projection vector shown in blue in the figure. Alternatively, the systolic array can also be derived using the folding algorithm [39]. Note that all multiplications with coefficient $b_j$ are mapped to the same hardware multiplier.

![Diagram](image)

**Fig. 2.** Three different forms of FIR filter architecture when $n = 4$.

3.2 Scheduling for the modular polynomial multiplier

The scheduling and control logic in the proposed architecture are very simple and efficient. The coefficients of polynomial $A(x)$ are loaded sequentially from the most significant (highest degree) coefficient to the least significant (lowest degree) coefficient while the coefficients of polynomial $B(x)$ are stored starting with the least significant coefficient to the most significant coefficient from left to right. Finally, the result coefficients are output in the same order as $A(x)$ (i.e., from most significant coefficient to the least significant coefficient). Each switch is controlled by a one-bit

in each tap (node) are illustrated in Fig. 3(b). The systolic array contains additional switches and a shift register of size-$n$ (see the top of Fig. 3(a)) for continuous processing of input polynomials and polynomial modular reduction. Note that using a conventional transpose-form like structure to perform the polynomial multiplication would require padding zeros until the entire operation finishes; otherwise, it will lead to conflicts and produce wrong results. Furthermore, to perform polynomial modular reduction, the shift register as well as the switches can control the signals (coefficients of polynomial $A(x)$) properly based on the expression in Equation (9). Specifically, the coefficients of polynomial $A(x)$ with the negative signs are extracted from the shift register in its inverse form. Then, the switches select either the inverse form or the normal form coefficients from polynomial $A(x)$ in different clock cycles. As shown in Fig. 3, the proposed degree-$4$ modular polynomial multiplier consists of four modular multipliers, three modular adders, three delay elements, three switches, and one shift register. Specifically, the shift register consists of four delay elements, and the switches are constructed using multiplexers (MUXs). The design in Fig. 3 can be easily extended to degree-$n$. A degree-$n$ modular polynomial multiplier requires $n$ modular multipliers, $(n - 1)$ modular adders, $(n - 1)$ delay elements, $(n - 1)$ switches at the lower data paths and one shift register (consists of $n$ delay elements). For one modular polynomial multiplication, the response time is $n$ clock cycles, while the total latency is $(2n - 1)$ clock cycles. For $L$ polynomial multiplications, the response time remains the same, while the total latency in clock cycles is given by:

$$T_{lat} = n \cdot (L + 1) - 1. \quad (10)$$

The modular reduction can be performed by simply keeping the least $\epsilon$ bits for a $2^\epsilon$ modulus. For the lattice-based cryptography schemes, the degrees of the polynomial are relatively large, i.e., $n$ can be up to hundreds or thousands, which could cause a high fan-out issue on the output of the shift register and the input node. To overcome this, buffers (registers) are inserted after the switches, as shown as the green dashed line in Fig. 3(a). As a result, the critical path is one modular multiplier and one modular adder.

![Diagram](image)

**Fig. 3.** A degree-$4$ weight-stationary systolic modular polynomial multiplier.

- **(a)** Top-level architecture with transpose-form like structure. $4l + \{0,1,2,3\}$ represent the switching instances in a clock period of 4 respectively.
- **(b)** Details of each tap.
signal from the \((n - 1)\)-bit controller \(ctrl_{lsu}\): if this bit is equal to 1, the operand from polynomial \(A(x)\) of the modular multiplier is loaded from the input node; otherwise, it is loaded from the shift register. These control signals \(ctrl_{lsu}\) can be simply generated by a counter (ranging from 0 to \((n - 1)\)), as:

\[
ctrl_{lsu} = \begin{cases} 
0, \ldots, 0, & \text{if counter = 0,} \\
\{ctrl_{lsu}[n-2 : 1] \} & \text{otherwise.}
\end{cases}
\]  

(11)

After resetting the counter, all \((n - 1)\)-bit control signals \(ctrl_{lsu}\) are zeros. Then, in every subsequent clock cycles, \(ctrl_{lsu}\) shifts left by padding a “1” to the least significant bit (LSB).

4 Fast Polynomial Multiplier Using Fast M-Parallel Filter Architecture

In this section, we derive a highly parallel hardware architecture for the polynomial multiplication based on the fast parallel filter algorithm [9], [10], [11], [12]. The proposed algorithm is similar to the Karatsuba algorithm but has a significantly lower addition cost in the post-processing stage. Furthermore, this design requires less resource overhead than prior schoolbook polynomial multipliers. Parallel structures for modular polynomial multiplication for small lengths are first derived. These can then be iterated to obtain multiplier architectures for larger levels of parallelism. For example, a fast 2-parallel (i.e., \(M = 2\)) modular polynomial multiplier can be iterated twice (or thrice) to design a 4-parallel (or 8-parallel) multiplier.

4.1 Fast 2-parallel architecture

The fast 2-parallel modular polynomial multiplication, referred to as Fast.2.PolyMult, is described in Algorithm 1 which mainly consists of three stages: pre-processing (Step 1), intermediate polynomial multiplication (Step 2), and post-processing (Steps 3 and 4).

We first decompose the polynomials \(A(x)\) and \(B(x)\) based on the even and odd indices, as shown in Step 1, also called polyphase decomposition [2]. We denote \(y = x^2\), and the polynomial \(A(x)\) is expressed as:

\[A(x) = A_0(x^2) + A_1(x^2) \cdot x = A_0(y) + A_1(y) \cdot x,\]

(12)

where the even indexed polynomial \(A_0(y)\) and the odd indexed polynomial \(A_1(y)\) are expressed as:

\[A_0(y) = a[0] + a[2]y + a[4]y^2 + \ldots + a[n - 2]y^{n/2 - 1} \mod (y^{n/2} + 1),\]

(13)

\[A_1(y) = a[1] + a[3]y + a[5]y^2 + \ldots + a[n - 1]y^{n/2 - 1} \mod (y^{n/2} + 1).\]

(14)

Similar decomposition is applied to \(B(x)\) to obtain its even and odd polynomials \(B_0(y)\) and \(B_1(y)\). The product \(P(x)\) can be computed as:

\[P(x) = P_0(y) + P_1(y) \cdot x = (A_0(y) + A_1(y) \cdot x) \cdot (B_0(y) + B_1(y) \cdot x) = A_0(y)B_0(y) + [A_0(y)B_1(y) + A_1(y)B_0(y)] \cdot x + [A_1(y)B_1(y)] \cdot y.
\]

(15)

The polyphase decomposition describes one polynomial multiplication of length-\(n\) in terms of four polynomial multiplications of length-\(n/2\). While this step in itself does not reduce the computation complexity, it is an essential first step. In Step 2, the fast filter algorithm describes the modular polynomial multiplication in terms of three polynomial multiplications of half length; this reduces the complexity by 25%. Denote the three intermediate modular polynomial multiplication outputs as \(U(y)\), \(V(y)\), and \(W(y)\). In the fast algorithm, \(P_1(y)\) is computed as:

\[P_1(y) = A_0(y)B_1(y) + A_1(y)B_0(y),\]

\[= (A_0(y) + A_1(y))(B_0(y) + B_1(y)) - A_0(y)B_0(y) - A_1(y)B_1(y)\]

\[= W(y) - (U(y) + V(y)),\]

(16)

(17)

where

\[U(y) = A_0(y)B_0(y),\]

(18)

\[V(y) = A_1(y)B_1(y),\]

(19)

\[W(y) = (A_0(y) + A_1(y))(B_0(y) + B_1(y)).\]

(20)

Note that unlike \(P_1(y)\), \(P_0(y) = U(y) + V(y) \cdot y \mod (y^{n/2} + 1)\) requires further modular polynomial reduction, which is achieved in the post-processing step. Since \(V(y)\) needs to be multiplied by \(y\) before adding the coefficients of \(U(y)\), the highest degree of coefficient exceeds the range of the ring \((y^{n/2} + 1)\), i.e., \(U(y) + V(y) \cdot y = u[0] + p_0[1]y + p_0[2]y^2 + \ldots + v[n/2 - 1]y^{n/2 - 1}\). As a result, the even polynomial \(P_0(y)\) requires an additional subtraction and is computed as:

\[P_0(y) = (u[0] - v[n/2 - 1]) + p_0[1]y + p_0[2]y^2 + \ldots + p_0[n/2 - 1]y^{n/2 - 1}.\]

(21)

The data-flow of the proposed fast parallel architecture is shown in Fig. 4.
While the fast modular polynomial multiplier structure is similar to the fast parallel filter, there is one fundamental difference. Unlike the fast parallel filter where all computations are causal, the computation $V(y) \cdot y$ is inherently a non-causal operation. This is transformed to a causal operation by introducing a latency of one clock cycle; this can be achieved by placing delays at one feed-forward cutset in the post-processing step. The proposed novel approach of computing $V(y) \cdot y$ does not increase the latency beyond one clock cycle, and preserves the feed-forward property of the architecture and continuous data-flow property.

### 4.2 Fast 4-parallel architecture

A fast 4-parallel architecture can be derived by iterating the 2-parallel filter twice [9, 10, 11, 12]. The fast 4-parallel schoolbook modular polynomial multiplication algorithm (also denoted as Fast.4.PolyMult) is presented in Algorithm 2 while Fig. 7 shows the corresponding architecture.

**Algorithm 2 Fast.4.PolyMult($A(x), B(x)$)**

Input: $A(x)$ and $B(x) \in \mathbb{F}_q$

Output: $P(x) = (P_0(x^4), P_1(x^4), P_2(x^4), P_3(x^4))$, 

\[
\text{//} P(x) = A(x) \cdot B(x) \mod (x^n + 1, q)
\]

1: $A(x) = A_0(x^2) + A_1(x^2) \cdot x^2$

//split $A(x)$ as two parts based odd and even indices

\[
B(x) = B_0(x^2) + B_1(x^2) \cdot x^2
\]

//split $B(x)$ as two parts based odd and even indices

2: $(C_0(y), C_1(y)) = \text{Fast.2.PolyMult}(A_0(x^2), B_0(x^2))$

where $y = x^4$

\[
(C_2(y), C_3(y)) = \text{Fast.2.PolyMult}\left((A_0(x^2) + A_1(x^2)), (B_0(x^2) + B_1(x^2))\right)
\]

$(C_4(y), C_5(y)) = \text{Fast.2.PolyMult}(A_1(x^2), B_1(x^2))$

3: $P_0(y) = C_0(y) + C_5(y) \cdot y \mod (y^{n/4} + 1, q)$

\[
P_1(y) = C_2(y) - C_1(y) - C_4(y) \mod (y^{n/4} + 1, q)
\]

\[
P_2(y) = C_1(y) + C_4(y) \mod (y^{n/4} + 1, q)
\]

\[
P_3(y) = C_3(y) - C_0(y) - C_5(y) \mod (y^{n/4} + 1, q)
\]

4: $P(x) = P_0(x^4) + P_1(x^4) \cdot x + P_2(x^4) \cdot x^2 + P_3(x^4) \cdot x^3$

where $y = x^4$

5: return $P(x)$

The Fast.4.PolyMult algorithm has three steps. In Step 1 of Algorithm 2, $A(x)$ is split as two parts based on the odd and even indices. Then, $A_0(x^2)$, $A_1(x^2)$, and their sum $(A_0(x^2) + A_1(x^2))$ are further split based on Step 1 in Fast.2.PolyMult (Algorithm 1). $A_0(x^2)$ and $A_1(x^2)$ are decomposed as four polynomials $(A_{00}(x^4), A_{01}(x^4), A_{10}(x^4), A_{11}(x^4))$ which are fed to upper
and lower fast 2-parallel modular polynomial multipliers (denoted Fast-2 PolyMult. in Fig. 7), respectively. Meanwhile, as the fast 2-parallel modular polynomial multiplier has two inputs in parallel, \((A_0(x^2) + A_1(x^2))\) in Step 2 is simply implemented as two adders in the middle fast 2-parallel modular polynomial multiplier, i.e., \((A_{00}(x^4) + A_{10}(x^4))\) and \((A_{01}(x^4) + A_{11}(x^4))\). Let \(y\) represents \(x^4\), hence the four polynomials decomposed from \(A_0(x^2)\) and \(A_1(x^2)\) can be expressed as

\[
A_{00}(y) = a[0] + a[4]y + [8]y^2 + ... + a[n - 4]y^{n/4 - 1} \mod (y^{n/4} + 1),
\]

\[
A_{10}(y) = a[1] + a[5]y + [9]y^2 + ... + a[n - 3]y^{n/4 - 1} \mod (y^{n/4} + 1), \tag{22}
\]

\[
A_{01}(y) = a[2] + a[6]y + a[10]y^2 + ... + a[n - 2]y^{n/4 - 1} \mod (y^{n/4} + 1), \tag{23}
\]

\[
A_{11}(y) = a[3] + a[7]y + a[11]y^2 + ... + a[n - 1]y^{n/4 - 1} \mod (y^{n/4} + 1), \tag{24}
\]

where

\[
A(x) = A_{00}(x^4) + A_{10}(x^4) \cdot x + A_{01}(x^4) \cdot x^2 + A_{11}(x^4) \cdot x^3. \tag{26}
\]

\(B(x)\) can be decomposed in a similar manner.

In the intermediate polynomial multiplication stage, three degree-\(\frac{n}{2}\) fast 2-parallel modular polynomial multipliers (Fig. 5) generate six degree-\(\frac{n}{4}\) polynomials, \(C_0(y), C_1(y), ..., C_5(y)\). As shown in Fig. 6, \(\frac{n}{2}\) additions/subtractions operated are carried out by six adders/subtractors, where each adder/subtractor performs \(\frac{n}{4}\) additions/subtractions. Finally, polynomial modular reduction for \(C_5(y)\) and \(C_0(y)\) are performed in a manner similar to the fast 2-parallel architecture (Fig. 5).

### 4.3 Fast 3-parallel architecture

We also present the design for a fast 3-parallel schoolbook modular polynomial multiplication algorithm (denoted as Fast.3.PolyMult), allowing \(M\) to be a multiple of 3, enabling various levels of parallelism. Fast.3.PolyMult algorithm also consists of three stages, which is illustrated in Algorithm 3. During the polyphase decomposition (pre-processing stage), polynomial \(A(x)\) is decomposed as

\[
A(x) = A_0(x^3) + A_1(x^3) \cdot x + A_2(x^3) \cdot x^2. \tag{27}
\]

The modular multiplication result \(P(x)\) can be defined as:

\[
P(x) = P_0(y) + P_1(y) \cdot x + P_2(y) \cdot x^2, \tag{28}
\]

where \(y = x^3\), and these three sub-polynomials are presented in Step 4 in Algorithm 3. The derivation of the fast 3-parallel modular multiplier is similar to the fast parallel filter derivation; the reader is referred to [9, 10, 12].

The architecture for the Fast.3.PolyMult algorithm is shown in Fig. 8, which consists of six degree-\(\frac{n}{6}\) modular polynomial multipliers, thirteen modular adders/subtractors with additional delay elements. These six degree-\(\frac{n}{6}\) modular multipliers compute the intermediate polynomials \(C_0(y)\) to \(C_5(y)\) with an additional pipelining stage at the end of the modular multipliers’ output.

In the post-processing stage, six intermediate polynomials are used to generate four new intermediate polynomials \(D_0(y)\) to \(D_3(y)\) before computing the outputs \(P_0(y)\), \(P_1(y)\), and \(P_2(y)\) using less number of additions/subtractions.

### 4.4 Fast M-parallel architecture

Using iterated approach, we can use fast 2-parallel architecture and/or fast 3-parallel architecture to achieve higher levels of parallelism. Therefore, we can implement various fast \(M\)-parallel architectures, where the level of parallelism \(M\) can be a power-of-two integer, power-of-three integer, or product of any power-of-two and power-of-three. Note that the coefficients from all the sub-polynomials of \(P(x)\) should be aligned after all operations. This is similar to inserting a pipelining cutset to transform non-causal operations to causal operations, at the expense of an increase in latency by one cycle.

The timing performance can be theoretically derived as follows. The fast \(M\)-parallel design can reduce the response time to approximately \(n/M\) clock cycles. In general, the total latency of an \(M\)-parallel modular polynomial multiplier for \(L\) polynomial multiplications can be expressed as:

\[
T_{\text{lat}} = n(1 + L)/M + \lceil \log_2(M) \rceil. \tag{29}
\]
TABLE 1. Performance of modular polynomial multiplier when \( n = 256 \).

| Design       | Device      | LUTs | FFs | DSPs | BRAM | Freq. [MHz] |
|--------------|-------------|------|-----|------|------|-------------|
| Roy [6]      | Ultrascale+ | 17406| 5083| 0    | 0    | 250         |
| Roy (2 Mults.) [6] | Ultrascale+ | 31853| 8844| 0    | 0    | 250         |
| Zhu [17]     | Ultrascale+ | 13954| 3943| 85   | 6    | 100         |
| FIR.PolyMult | Ultrascale+ | 16971| 8755| 0    | 0    | 250         |
| Fast.2.PolyMult | Ultrascale+ | 25831| 12850| 0    | 0    | 250         |
| Fast.4.PolyMult | Ultrascale+ | 35306| 19143| 64   | 0    | 250         |
| Mera [18]    | Artix-7     | 7400 | 7331| 38   | 2    | 125         |
| FIR.PolyMult | Artix-7     | 16902| 8755| 0    | 0    | 133         |
| Fast.2.PolyMult | Artix-7     | 25854| 12850| 0    | 0    | 133         |
| Fast.4.PolyMult | Artix-7     | 35396| 19143| 64   | 0    | 133         |

TABLE 2. Timing performance (total latency (unit: clock cycle)/actual latency (unit: \( \mu s \))) of modular polynomial multiplier when \( n = 256 \).

| Design       | Device      | PolyMult. | KeyGen | Enc | Dec |
|--------------|-------------|-----------|--------|-----|-----|
| Roy [6]      | Ultrascale+ | 256/1.02  | 2685/10.74 | 3592/14.37 | 4484/17.94 |
| Roy (2 Mults.) [6] | Ultrascale+ | 128/0.51 | 1552/6.21 | 2205/8.82 | 2911/11.64 |
| Zhu [17]     | Ultrascale+ | 81/0.81   | (Not Reported) | 978/9.78 | 1227/12.27 |
| FIR.PolyMult | Ultrascale+ | 51/2.04   | 2560/10.24 | 3328/13.31 | 4096/16.38 |
| Fast.2.PolyMult | Ultrascale+ | 255/10.20 | 1281/5.12 | 1665/6.66 | 2049/8.20 |
| Fast.4.PolyMult | Ultrascale+ | 127/5.08  | 642/2.57  | 834/3.34  | 1026/4.10 |
| Mera [18]    | Artix-7     | 1299/10.30| 11592/92.74 | 15456/123.65 | 19320/154.56 |
| FIR.PolyMult | Artix-7     | 511/3.83  | 2560/19.20 | 3328/24.96 | 4096/30.72 |
| Fast.2.PolyMult | Artix-7     | 255/1.91  | 1281/9.61  | 1665/12.48 | 2049/15.36 |
| Fast.4.PolyMult | Artix-7     | 127/0.95  | 642/4.82  | 834/6.26  | 1026/7.70 |

5 Experimental Results

The performance of the proposed modular polynomial multiplication is demonstrated for the Saber scheme using Verilog HDL implementation. Several changes are adopted specifically for the Saber scheme. Due to the Saber scheme’s advantages, the basic components do not consume a large amount of hardware resources. In particular, the modular multiplier discussed in Section 3 can be replaced by general adders since the random elements are small (since the coefficients of polynomial \( B(x) \) are in \([-4, 4])\). As the moduli are power-of-two integers, the modular reduction can again be performed by simply keeping the lower bits. Note that, the coefficients in both polynomials \( A(x) \) and \( B(x) \) are represented in the sign-magnitude form, and the word-lengths of the magnitudes of these two polynomials are 13-bit and 3-bit, respectively. The modular adder calculates the 13-bit sum (\( \text{sum} \)) by adding the product \( \text{prod} \) of the corresponding \( a[i] \) and \( b[j] \), and the output from the register \( \text{acc} \) as shown in Fig. 3b, which can also be mathematically expressed as:

\[
\text{sum} = \begin{cases} 
\text{acc} - \text{prod}, & \text{if } a_{\text{sign}} \oplus b_{\text{sign}} = 1, \\
\text{acc} + \text{prod}, & \text{otherwise}, 
\end{cases}
\]

(30)

where \( a_{\text{sign}} \) and \( b_{\text{sign}} \) are the sign bits of the two operands \( a[i] \) and \( b[j] \), respectively.

The experiment is performed on the Xilinx Artix-7 AC701 FPGA board which is recommended by NIST for PQC hardware implementation. In addition, since several prior works also used the high-performance Xilinx UltraScale+ FPGA board, we also demonstrate the performance of our architecture on this board for more comparisons. The communication and data transmission between FPGA and PC use the universal asynchronous receiver-transmitter (UART) module provided by AC701 device for functionality verification.

5.1 Evaluation of modular polynomial multiplier

We first examine the performance of our proposed modular polynomial multipliers, including the FIR filter-based (Fig. 3), fast 2-parallel architecture, and fast 4-parallel architecture in key generation, encapsulation, and decapsulation steps of Saber scheme with the standard security level. The experimental results and comparison with prior works [6], [17], [18] are summarized in Table 1. A further comparison of the timing performance is presented in Table 2. The clock frequencies are set as 250MHz and 133MHz for UltraScale+ and Artix-7, respectively. It can be seen from Table 1 that our design has a shorter critical path than those of the designs in [17], [18] and the same as the work in [6].

For a fair comparison, we focus on the evaluation against the architecture [6], since both designs use the same clock frequency while the implementation of the design in [17] has a much lower clock frequency. Compared to [6], our proposed FIR filter based modular polynomial multiplier has slightly less number of LUTs and less total latency while requiring a larger number of flip-flops (FFs) due to the additional shift registers. Our design achieves 18% and 25% reductions on the LUTs and the clock cycles for all the polynomial multiplications in the Saber scheme. Even though our design requires more FFs in the data-path and shift registers, we argue that it makes a smaller influence on the overall performance on UltraScale+ and Artix-7 FPGA boards, since both devices have a much higher resource budget for FFs than LUTs.

Furthermore, both the polynomial multiplier in LWRpro [17] and the compact polynomial multiplier in [17], [18] use the Karatsuba algorithm with 8-level and 4-level, respectively. For instance, the compact polynomial multiplier has a long critical path of five adders/subtractors and two multipliers in the interpolation part, which requires two pipelining stages to reduce the critical path for maintaining a high frequency. This design targets the low-
area performance, which only requires limited numbers of LUTs, FFs, and only 38 DSP units, as shown in Tables 1. While this design has a lower LUT usage than our architecture, it suffers from a low speed since their degree-64 polynomial multipliers require 1168 clock cycles for each computation, which causes the actual latency in such a compact design to be around 19 times of the latency in our fast 4-parallel architecture as presented in Table 2. If we consider the area-time product (ATP) [LUTs × μs] as the performance metric, our proposed fast 4-parallel architecture and the prior low-area design yield an ATP of 1.71 × 10^5 and 6.86 × 10^5, respectively, for the key generation. In other words, our design achieves a 75.07% reduction on the ATP. Besides, the modular polynomial multiplier in [17] has the lowest clock cycles among all the prior works, while having a lower clock frequency as illustrated in Table 3. In comparison, our fast 4-parallel architecture requires 14.72% less number of clock cycles and achieves a 65.85% reduction in the actual latency for the encryption. Besides, our design achieves a 13.24% lower ATP than that of their design (1.36 × 10^5 in their design versus 1.18 × 10^5 in ours). Moreover, the design in [17] requires 24.71% more DSPs than our fast 4-parallel architecture. Thus, we can conclude that our design achieves significant reduction on the latency or the delay (critical path) which leads to reductions on ATP, when comparing to the two prior works that employ the Karatsuba polynomial multiplication.

5.3 Comparison with Saber and other related PQC scheme implementations

For the implementation of the entire Saber scheme, the modular polynomial multiplication is implemented by the proposed fast 4-parallel architecture, while other simple functional blocks are modified from the open-source codes provided in [5] and [6].

Table 4 presents the comparison of the FPGA performance with recent hardware implementations for the PQC schemes, including Saber as well as some other schemes for a more comprehensive comparison. The latency in our design is 52% less than the latency in [6], where the reduction is mainly from the optimized low-latency modular polynomial multiplier and the hash function block. For example, the total latency of SHA3-256 (needs to process 32-byte, 64-byte, 992-byte, and 1088-byte seeds) operating in the hash function block is reduced from 585 clock cycles to 526 clock cycles in the Saber encapsulation. The rationale behind this latency reduction is as follows. Most open-source packages add stages of pipelining to achieve a high frequency (low critical path) design in order to adapt to general applications [41]. However, the critical path among the prior works are under the NTT-based or schoolbook modular polynomial multiplier that requires addition or multiplication, which is much higher than Keccak core provided in the open-source packages, thus implying that some pipelines are redundant. Different from the prior works, we implement our own hash function block as we aim to reduce the total latency for computing the hash functions by eliminating unnecessary pipelining stages.

For the area performance, although we have increased hardware costs, both Artix-7 and UltraScale+ FPGA boards still have sufficient resources to accommodate our 4-parallel design. In other words, our proposed 4-parallel architecture is under the constraint of hardware complexity specified by NIST (Artix-7). LWPro [17] exhibits less latency, even though our fast 4-parallel architecture for the polynomial multiplication achieves a better timing performance as discussed in Section 5.1. The rationale behind is that their hash function module runs 24 rounds of permutation in only 12 clock cycles, which doubles the hardware resource, while our hash function block utilizes the similar structure as in prior works that employ one Keccak core [6], [26]. It is possible to adapt their hash module [17] in our proposed architecture to further reduce the latency, but with a cost of increased hardware overhead. The designs in [18], [31] are also implemented as software/hardware co-design, which however require large computational time. Specifically, our accelerator achieves reductions of about 77.5% and 99.4% compared to the designs in [31] and [18], respectively. We note that the relatively large latency of compact modular polynomial multiplier design is mainly due to the hash function computation in software, and communication cost in [18].

Furthermore, the proposed architecture also achieves a lower latency than recent implementations for other PQC schemes. Note that the results only include implementations for KEM schemes and these three designs [7], [26], [40] consider low-area (compact) design as the primary objective. Compared with the Crystals-

---

Table 3. Performance of modular polynomial multiplier using fast M-parallel architecture when \( n = 180 \).

| Design       | Device | LUTs  | FFs  | DSPs | Freq. [MHz] | 1 PolyMult.* | 9 PolyMult.* |
|--------------|--------|-------|------|------|-------------|--------------|--------------|
| Fast.2.PolyMult | Artix-7 | 17902 | 9096 | 0    | 133         | 181/1.36     | 901/6.77     |
| Fast.3.PolyMult | Artix-7 | 21279 | 11996| 60   | 133         | 122/0.91     | 602/4.53     |
| Fast.4.PolyMult | Artix-7 | 25110 | 13633| 45   | 133         | 92/0.69      | 452/3.40     |

*: Total latency (unit: clock cycle)/actual latency (unit: μs)
**TABLE 4. Comparisons with recent PQC implementations**

| Platform     | Time in (μs): KeyGen/Encaps/Decaps | Freq. [MHz] | Area: LUTs/FFs/DSPs/BRAM | Scheme       |
|--------------|-----------------------------------|-------------|--------------------------|--------------|
| Roy [6]      | 21.8/26.5/32.1                    | 250         | 23.6k/9.8k/0/2           | Saber        |
| Zhu [17]     | (Not Reported)/11.6/4.1           | 100         | 34.8k/9.9k/85/6          | Saber        |
| Mera [18]    | 3.2k/4.1k/3.8k                    | 100         | 7.4k/7.3k/2/8/2          | Saber        |
| Dang [31]    | (Not Reported)/60/65             | 322         | 12.5k/1.6k/256/4         | Saber        |
| Xing [26]    | 39.2/47.6/62.3                   | 161         | 7.4k/6.6k/2/3           | Kyber        |
| Zhang [17]   | 40/62.5/24                       | 200         | 6.7k/4.1k/2/8           | NewHope      |
| Howe [40]    | 45k/45k/47k                      | 167         | 7.7k/3.5k/1/24          | Frodo        |
| Ours         | 19.2/23.6/29.2                   | 133         | 41.5k/22.3k/6/4/2       | Saber        |
| Ours         | 10.2/12.6/15.6                   | 250         | 41.5k/22.3k/6/4/2       | Saber        |

Kyber processor [26], our design reduces the actual latency by 59.2%. We also compare the implementations of NewHope and Frodo, which are not the finalist schemes in current round of NIST standardization. The NewHope accelerator in [7] does not involve any SHA-3 functions since it only considers the IND-CPA security application. However, our IND-CCA secure sabre design still shows a better timing performance. On the other hand, the design in [40] is constrained by the expensive computation of the scheme [42], which leads to a long computational time.

6 CONCLUSION

This paper presented a novel modular polynomial multiplier for lattice-based cryptography. The proposed hardware design exploits the fast filtering technique to achieve low latency, high scalability, and full hardware utilization. We proposed efficient parallel architectures with much lower hardware overhead and latency than prior works. Our design can be easily generalized across different levels of parallelism. Comprehensive experimental results are presented. We show our design achieves superior performance than the state-of-the-art modular polynomial multipliers based on schoolbook polynomial multiplication or the Karatsuba algorithm. A case study of instantiating Saber scheme is also presented, which shows that our proposed design can accelerate the computation and reduce the actual latency of the cryptosystem compared with the prior works.

REFERENCES

[1] C. Gentry and D. Boneh, *A fully homomorphic encryption scheme*. Stanford University Stanford, 2009, vol. 20, no. 09.

[2] National Institute of Standards and Technology (NIST), “Post-quantum cryptography standardization.” https://csrc.nist.gov/project/post-quantum-cryptography, 2020.

[3] C. Chen, O. Danba, J. Hoffstein, A. Hulsing, J. Rijneveld, J. M. Schanck, T. Saito, P. Schwabe, W. Whyte, K. Xagawa, T. Yamakawa, and Z. Zhang, “Algorithm specifications and supporting documentation,” 2020.

[4] J. Bos, L. Ducas, E. Kiltz, T. Lepoint, V. Lyubashevsky, J. M. Schanck, P. Schwabe, G. Seiler, and D. Stehlé, “CRYSTALS-Kyber: a CCA-secure module-lattice-based KEM,” in *2018 IEEE European Symposium on Security and Privacy (EuroS&P)*. IEEE, 2018, pp. 353–367.

[5] J.-P. D’Anvers, A. Karmakar, S. S. Roy, and F. Vercauteren, “Saber: Module-LWR based key exchange, CPA-secure encryption and CCA-secure KEM,” in *International Conference on Cryptology in Africa*. Springer, 2018, pp. 282–305.

[6] S. S. Roy and A. Basso, “High-speed instruction-set coprocessor for lattice-based key encapsulation mechanism: Saber in hardware,” *IACR Transactions on Cryptographic Hardware and Embedded Systems*, pp. 443–466, 2020.

[7] N. Zhang, B. Yang, C. Chen, S. Yin, S. Wei, and L. Liu, “Highly efficient architecture of NewHope-NIST on FPGA using low-complexity NTT/INTT,” *IACR Transactions on Cryptographic Hardware and Embedded Systems*, pp. 49–72, 2020.

[8] X. Zhang and K. K. Parhi, “Reduced-complexity modular polynomial multiplication for R-LWE cryptosystems,” in *ICASSP 2021–2021 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*. IEEE, 2021, pp. 7853–7857.

[9] K. K. Parhi, *VLSI digital signal processing systems: design and implementation*. John Wiley & Sons, 2007.

[10] D. A. Parker and K. K. Parhi, “Low-area/power parallel FIR digital filter implementations,” *Journal of VLSI signal processing systems for signal, image and video technology*, vol. 17, no. 1, pp. 75–92, 1997.

[11] C. Cheng and K. K. Parhi, “Hardware efficient fast parallel FIR filter structures based on iterated short convolution,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 8, pp. 1492–1500, 2004.

[12] D. A. Parker and K. K. Parhi, “Area-efficient parallel FIR digital filter implementations,” in *Proceedings of International Conference on Application Specific Systems, Architectures and Processors: ASAP’96*. IEEE, 1996, pp. 93–111.

[13] H.-T. Kung, “Why systolic architectures?” *Computer*, vol. 15, no. 01, pp. 37–46, 1982.

[14] S. Y. Kung, “VLSI array processors,” *Englewood Cliffs, 1988*.

[15] H. V. Jagadish, S. K. Rao, and T. Kailath, “Array architectures for iterative algorithms,” *Proceedings of the IEEE*, vol. 75, no. 9, pp. 1304–1321, 1987.

[16] A. Karatsuba, “Multiplication of multidigit numbers on automata,” in *Soviet physics doklady*, vol. 7, 1963, pp. 595–596.

[17] Y. Zhu, M. Zhu, B. Yang, W. Zhu, C. Deng, C. Chen, S. Wei, and L. Liu, “LWRpro: An energy-efficient configurable crypto-processor for Module-LWR,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 3, pp. 1146–1159, 2021.

[18] J. M. B. Mera, F. Turan, A. Karmakar, S. S. Roy, and I. Verbauwheide, “Compact domain-specific co-processor for accelerating module lattice-based KEM,” in *2020 57th ACM/IEEE Design Automation Conference (DAC)*. IEEE, 2020, pp. 1–6.

[19] J. Alwen, S. Krenn, K. Pietrzak, and D. Wichs, “Learning with rounding, revisited,” in *Annual Cryptology Conference*. Springer, 2013, pp. 57–74.

[20] V. Lyubashevsky, C. Peikert, and O. Regev, “On ideal lattices and learning with errors over rings,” in *Annual International Conference on the Theory and Applications of Cryptographic Techniques*. Springer, 2010, pp. 1–23.

[21] P. Barrett, “Implementing the Rivest Shamir and Adleman public key encryption algorithm on a standard digital signal processor,” in *Conference on the Theory and Application of Cryptographic Techniques*. Springer, 1986, pp. 311–323.

[22] P. L. Montgomery, “Modular multiplication without trial division,” *Mathematics of computation*, vol. 44, no. 170, pp. 591–592, 1985.

[23] Z. Brakerski, A. Langlois, C. Peikert, O. Regev, and D. Stehlé, “Classical hardness of learning with errors,” in *Proceedings of the forty-fifth annual ACM symposium on Theory of computing*, 2013, pp. 575–584.

[24] J. Fan and F. Vercauteren, “Somewhat practical fully homomorphic encryption,” *IACR Cryptology ePrint Archive*, vol. 2012, p. 144, 2012.

[25] G. Xin, J. Han, T. Yin, Y. Zhou, J. Yang, X. Cheng, and X. Zeng, “VPQC: A domain-specific vector processor for post-quantum cryptography based on RISC-V architecture,” *ACM symposium on Theory of computing*, 2013, pp. 575–584.

[26] Y. Xing and S. Li, “A compact hardware implementation of CCA-secure key exchange mechanism CRYSTALS-KYBER on FPGA,” *IACR Transactions on Cryptographic Hardware and Embedded Systems*, pp. 328–356, 2021.

[27] D. T. Nguyen, V. B. Dang, and K. Gaj, “A high-level synthesis approach to the software/hardware codesign of ntt-based post-quantum...
cryptography algorithms,” in 2019 International Conference on Field-Programmable Technology (ICFPPT). IEEE, 2019, pp. 371–374.

[28] U. Banerjee, T. S. Ukyab, and A. P. Chandarakas, “Sapphire: A configurable crypto-processor for post-quantum lattice-based protocols,” IACR Transactions on Cryptographic Hardware and Embedded Systems, pp. 17–61, 2019.

[29] D. T. Nguyen, V. B. Dang, and K. Gaj, “High-level synthesis in implementing and benchmarking number theoretic transform in lattice-based post-quantum cryptography using software/hardware codesign.” in ARC, 2020, pp. 247–257.

[30] S. S. Roy, F. Vercauteren, J. Vliegen, and J. Verbauwhede, “Hardware assisted fully homomorphic function evaluation and encrypted search,” IEEE Transactions on Computers, vol. 66, no. 9, pp. 1562–1572, 2017.

[31] V. B. Dang, F. Farahmand, M. Andrezejczak, and K. Gaj, “Implementing and benchmarking three lattice-based post-quantum cryptography algorithms using software/hardware codesign,” in 2019 International Conference on Field-Programmable Technology (ICFPPT). IEEE, 2019, pp. 206–214.

[32] W. Liu, S. Fan, A. Khalid, C. Rafferty, and M. O’Neill, “Optimized schoolbook polynomial multiplication for compact lattice-based cryptography on FPGA,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 10, pp. 2459–2463, 2019.

[33] S. Fan, W. Liu, J. Howe, A. Khalid, and M. O’Neill, “Lightweight hardware implementation of r-lwe lattice-based cryptography,” in 2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS). IEEE, 2018, pp. 403–406.

[34] T. Poppelmann and T. Güneysu, “Area optimization of lightweight lattice-based encryption on reconfigurable hardware,” in 2014 IEEE international symposium on circuits and systems (ISCAS). IEEE, 2014, pp. 2796–2799.

[35] V. Migliore, M. M. Real, V. Lapotre, A. Tisserand, C. Fontaine, and G. Gogniat, “Hardware/software co-design of an accelerator forfv homomorphic encryption scheme using karatsuba algorithm,” IEEE Transactions on Computers, vol. 67, no. 3, pp. 335–347, 2016.

[36] A. L. Toom, “The complexity of a scheme of functional elements realizing the multiplication of integers,” in Soviet Mathematics Doklady, vol. 3, no. 4, 1963, pp. 714–716.

[37] Y. Zhang, C. Wang, D. E. S. Kundi, A. Khalid, M. O’Neill, and W. Liu, “An efficient and parallel R-LWE cryptoprocessor,” IEEE Transactions on Circuits and Systems II, vol. 67, no. 5, pp. 886–890, 2020.

[38] E. Fujisaki and T. Okamoto, “Secure integration of asymmetric and symmetric encryption schemes,” in Annual international cryptology conference. Springer, 1999, pp. 537–554.

[39] K. K. Pathi, C.-Y. Wang, and A. P. Brown, “Synthesis of control circuits in folded pipelined DSP architectures,” IEEE Journal of Solid-State Circuits, vol. 27, no. 1, pp. 29–43, 1992.

[40] J. Howe, T. Oder, M. Krausz, and T. Güneysu, “Standard lattice-based key encapsulation on embedded devices,” IACR Transactions on Cryptographic Hardware and Embedded Systems, pp. 372–393, 2018.

[41] M. Sandler and R. Chaves, “Efficient FPGA implementation of the SHA-3 hash function,” in 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI). IEEE, 2017, pp. 86–91.

[42] E. Alkim, J. W. Bos, L. Ducas, P. Longa, I. Mironov, M. Naehrig, V. Nikolaenko, C. Peikert, A. Raghunathan, and D. Stebila, “FrodoKEM learning with errors key encapsulation,” NIST, 2021.

Keshab K. Parhi (Fellow, IEEE) is Distinguished McKnight University Professor and Edgar F. Johnson Professor in the Department of Electrical and Computer Engineering. He completed his Ph.D. in EECS at the University of California, Berkeley in 1988. He has published over 650 papers, is the inventor of 32 patents, and has authored the textbook VLSI Digital Signal Processing Systems (Wiley, 1999). His current research addresses VLSI architectures for machine learning, hardware security, data-driven neuroscience and molecular/DNA computing. Dr. Parhi is the recipient of numerous awards including the 2003 IEEE Kiyo Tomiyasu Technical Field Award, and the 2017 Mac Van Valkenburg award and the 2012 Charles A. Desoer Technical Achievement award from the IEEE Circuits and Systems Society. He served as the Editor-in-Chief of the IEEE Trans. Circuits and Systems, Part-I during 2004 and 2005. He is a Fellow of the ACM, AAAS, and NAI.

Weihang Tan (Student Member, IEEE) received his B.S. (2018) and M.S. (2020) degrees in Electrical Engineering from Clemson University, where he is currently pursuing a Ph.D. degree. His research interests include hardware security and VLSI architecture design for fully homomorphic encryption, post-quantum cryptography, and digital signal processing systems.

Antian Wang (Student Member, IEEE) received his B.E. (2017) in Communication Engineering from Shanghai Maritime University. He is currently pursuing a Ph.D. degree in Clemson University. His research interests include hardware security and VLSI architecture design, and design automation.

Yingjie Lao (Member, IEEE) is currently an assistant professor in the Department of Electrical and Computer Engineering at Clemson University. He received the B.S. degree from Zhejiang University, China, in 2009, and the Ph.D. degree from the Department of Electrical and Computer Engineering at University of Minnesota, Twin Cities in 2015. He is the recipient of an NSF CAREER Award, a Best Paper Award at the International Symposium on Low Power Electronics and Design (ISLPED), and an IEEE Circuits and Systems Society Very Large Scale Integration Systems Best Paper Award.

Xinmiao Zhang (Senior Member, IEEE) received her Ph.D. degree from the University of Minnesota. She joined The Ohio State University as an Associate Professor in 2017. Prior to that, she was a Senior Technologist at Western Digital, an Associate Professor at Case Western Reserve University. Her research interests include VLSI architecture design, digital storage and communications, security, and signal processing. She published more than 100 papers and authored the book “VLSI Architectures for Modern Error-Correcting Codes” (CRC Press, 2015). Dr. Zhang is a recipient of the NSF CAREER Award in 2009 and the Best Paper Award at 2004 ACM Great Lakes Symposium on VLSI. She was elected to serve on the BoG (2019-2021) of the IEEE CASS. She is also the Chair (2021-2022) of the Data Storage Technical Committee. She served on the committees of many conferences, including ISCAS, SIPS, ICC, and GLOBECOM.