Next Generation Digital Backends for the GMRT

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Abstract : The GMRT Backend Group is in the process of developing wide-band digital backends as part of a major upgrade of the GMRT. The main requirements are for processing 400 MHz bandwidth signals from 30 antennas for interferometry and array mode operations, along with additional features like narrow band modes and RFI cancellation schemes. Both FPGA and GPU based designs have been explored and this paper presents the design and implementation details along with results from testing of prototype units. A comparison of the resources needed and performance achieved on FPGA and GPU based designs is presented, along with an extrapolation of these designs to a 30 station backend for the final GMRT system.

1. Introduction

The Giant Metrewave Radio Telescope (GMRT) is a large, fully steerable telescope array of thirty 45 m diameter antennas, built for studying the astrophysical phenomena at low radio frequencies [1]. Located near Khodad, at a distance of about 80 kms north of Pune city in India, the GMRT array spread over a 30 km region, consists of a compact central area of 1 km by 1 km having 12 dishes, and the remaining 18 are distributed in 3 arms of a “Y” shaped array, that extends 15 km from the centre. Astronomical observations are currently possible at 5 different RF bands – 150, 235, 325, 610, 1420 MHz – with an instantaneous bandwidth of 32 MHz from each of two polarisation channels. The present digital backend that processes these signals to implement a 30 antenna, full polar correlator (for interferometry requirements) and incoherent / coherent beamformer (for array mode requirements) is the GMRT software backend (GSB) that utilizes a network of CPUs to carry out the tasks in real-time, achieving a peak performance of about 400 GFlops [2]. The GMRT observatory is undergoing a major upgrade to provide seamless frequency coverage for observations between 50 to 1500 MHz with instantaneous bandwidth of 400 MHz. New digital backends are being developed for processing the signals from antennas with 400 MHz bandwidth to produce interferometry and array outputs. The compute requirement for this is estimated to be about 6 TFlops.

2. Digital Backend – Implementation Options

The main specifications for the new backend system being developed for the upgraded GMRT are as follows : 30 inputs, dual polarisation, 400 MHz processing bandwidth, 8-bit sampling, up to 8192 spectral channels, delay correction range of +/- 128 microsec, fringe correction up to 5 Hz, correlator dump times 1 sec or better, full Stokes capability, array mode with incoherent and coherent beamformer options for pulsar processing, narrow band modes and RFI excision capabilities, raw
voltage recording and playback options. Two possible options for implementing the system have been tried out and are described in this paper.

2.1. Field Programmable Logic Array (FPGA) based design
This design is based on the packetised design approach of CASPER (Centre for Radio Astronomy Signal Processing and Electronic Research) of which the GMRT backend team is a member [3]. An 8-antenna, dual polarisation FPGA based digital correlator has been implemented and tested at GMRT in collaboration with the SKA-SA team from South Africa.

2.2. Graphical Processing Unit (GPU) based design
This is a hybrid design where the FPGA does the data capture and sends it on a 10GbE link to a host computer with a high performance GPU that does the bulk of the compute intensive data processing. An 8-antenna dual polarisation design of such a correlator has been developed in collaboration with Swinburne University of Technology, Australia and nVidia India, and has been tested at the GMRT.

Both options use the hardware boards from the CASPER collaboration [3] : iADC which uses Atmel make dual 8-bit ADC chips and a generic FPGA board called ROACH (Reconfigurable Open Architecture Computing Hardware) which uses one Virtex-5 chip for signal processing.

3. FPGA based design
The basic block schematic of the FPGA implementation of the digital correlator is shown in figure 1. The main components are dual channel ADCs for digitising both polarisation channels from each antenna, and ROACH boards for the processing – one set called F-engines which do the coarse delay correction, FFT, fine delay (FSTC) and fringe corrections, and the second set called X-engines which carry out the multiply and accumulate (MAC) operations and send the outputs to a host computer for storage. A 10 GbE switch is used to transfer the data from the F-engines to the X-engines such that each X-engine processes a pre-defined slice of the complete frequency spectrum from all the antennas.

![Figure 1: Schematic block diagram for a FPGA based backend](image)

An 8-antenna dual polarisation correlator based on this FPGA design has been implemented using 8 ADC boards, 8 F-engine and 8 X-engine ROACH boards, and tested with GMRT antenna signals. A typical self and cross spectrum of 110 MHz bandwidth signal at L-band from two antennas (E02, E06 in the eastern arm of the GMRT) while tracking the astronomical source 3C286, with an accumulation time of 2 sec, is shown in figure 2. Detailed tests and comparison with the existing 32 MHz GMRT Software Backend, show matching results (figure 3) which validates the basic performance of this new broadband backend design. By extrapolating this design, a version meeting the specs for the 30
antenna GMRT has been outlined. The estimated cost of this design is USD 469,400 and the net power dissipation is estimated to be about 5830 W.

4. GPU based design

GPUs consist of thousands of small efficient cores optimised for parallel performance. A CPU+GPU node is a powerful combination where the compute intense portion of the code is offloaded to GPU for processing while the CPU host handles the remaining portions, including i/o operations. At the GMRT we have implemented a GPU based 8-antenna dual polarisation correlator and tested it using GMRT signals. In our implementation we have used C2050 GPU cards of nVidia [4] with Dell T7500 machines as host. The ADC + FPGA board combination is used for digitizing and packetizing the input voltage signals from 2 channels, which are then sent to one host PC via a 10GbE connection. Such data from 8 host PCs are then shared over a 10GbE switch to provide each PC with a small time-slice of the full data block, from all the antennas (figure 4). The time slices are transferred to the GPU, where all the F-Engine and X-engine processing happens, and the final integrated results are passed on to the host and from there to a single machine for storage after stitching together the different time slices. For efficient handling of the tasks, the host machine employs multiple threads and MPI synchronization.

![Figure 4: Schematic block diagram for a GPU based backend](image-url)
Test data acquired with the GPU correlator has been used to generate radio maps of sources in the sky and these have been found to compare favorably with maps from GSB data (figure 5). By extrapolation, the estimated cost of this design for a 30 antenna system is expected to be USD 491600 and power consumption is expected to be 20,800 W.

5. Summary and Conclusion
The GMRT team has successfully developed 2 kinds of prototype designs for 400 MHz bandwidth backend systems. Based on our experience with these FPGA and GPU based correlator prototypes, it can be concluded that for a full GMRT backend, cost implications are similar in both FPGA and GPU approaches, but the total power consumption in GPU based designs is expected to be about 4 times higher. At the same time GPU designs are more flexible and the parameter set can be changed and new features added easily without major redesign effort, and they also benefit from full floating point arithmetic.

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