Quantum Circuit Designs of Integer Division
Optimizing T-count and T-depth

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Abstract—Quantum circuits for mathematical functions such as division are necessary to use quantum computers for scientific computing. Quantum circuits based on Clifford+T gates can easily be made fault-tolerant but the T gate is very costly to implement. The small number of qubits available in existing quantum computers adds another constraint on quantum circuits. As a result, reducing T-count and qubit cost have become important optimization goals. The design of quantum circuits for integer division has caught the attention of researchers and designs have been proposed in the literature. However, these designs suffer from excessive T gate and qubit costs. Many of these designs also produce significant garbage output resulting in additional qubit and T gate costs to eliminate these outputs. In this work, we propose two quantum integer division circuits. The first proposed quantum integer division circuit is based on the restoring division algorithm and the second proposed design implements the non-restoring division algorithm. Both proposed designs are optimized in terms of T-count, T-depth and qubits. Both proposed quantum circuit designs are based on (i) a quantum subtractor, (ii) a quantum adder-subtractor circuit, and (iii) a novel quantum conditional addition circuit. Our proposed restoring division circuit achieves average T-count savings from 79.03% to 91.69% compared to the existing works. Our proposed non-restoring division circuit achieves average T-count savings from 49.75% to 90.37% compared to the existing works. Further, both our proposed designs have linear T-depth.

I. INTRODUCTION

Among the emerging computing paradigms, quantum computing appears promising due to its applicability in number theory, encryption, search and scientific computation [1] [2]. Quantum circuits for integer arithmetic operations such as addition, subtraction, multiplication and division are required in the quantum circuit implementations of many quantum algorithms in these areas. Quantum arithmetic circuits for division can be used in the circuit implementation of quantum algorithms such as those for computing shifted quadratic character problems, principal ideal problems and hidden shift problems [2] [3] [4]. Quantum division circuits also reduce the resources needed in the circuit implementations of higher level functions such as calculating the greatest common divisor via the Euclidean algorithm. An efficient quantum circuit for the Euclidean algorithm has use in quantum algorithms such as those for solving the shifted multiplicative character problem [4]. Thus, researchers have included dedicated libraries of basic quantum integer arithmetic functions such as division in quantum programming languages such as Quipper and LIQUi| and in quantum computing design tools [1] [5].

Quantum computation can be performed on quantum circuits built from quantum gates. Any constant inputs in the quantum circuit are called ancillae. Garbage outputs are any outputs which exist in the quantum circuit to preserve one-to-one mapping but are neither one of the primary inputs nor a useful output. The inputs regenerated at the outputs are not considered garbage outputs [6]. Ancillae and garbage outputs are circuit overhead that need to be minimized.

The fault-tolerant implementation of quantum circuits is gaining the attention of researchers because physical quantum computers are prone to noise errors [7]. Fault-tolerant implementations of quantum gates and quantum error correcting codes can be used to overcome the limits imposed by noise errors in implementing quantum computing [8] [9]. Recently, researchers have implemented quantum logic gates such as the Toffoli gate, Fredkin gate and quantum full adder with fault-tolerant implementations of the Clifford+T gates due to their demonstrated tolerance to noise errors [8]. However, the increased tolerance to noise errors comes with the increased implementation overhead associated with the quantum T gate [10] [8] [9]. Because of the increased cost to realize the T gate, T-count and T-depth are important performance measures for fault-tolerant quantum circuit design.

The design of quantum circuits for integer division is an active area of research. Designs such as those proposed in [11], [12] and [13] present dividers that can be used in quantum computation. The design in [11] implements the restoring division algorithm and the designs in [12] are based on the non-restoring division algorithm. The design presented in the recent work in [13] uses a novel division algorithm. The design in [11] has a significant overhead in terms of T gates because it depends on quantum gates that cannot be exactly constructed using Clifford+T gates. The Clifford+T gate approximations for these gates are costly in terms of T-count [14]. Further, the T-count increases as the accuracy of the approximation of these gates is improved [13]. In contrast the dividers in [12] depend on quantum gates that can be exactly realized with Clifford+T gates. At most 7 T gates are required to implement each logic gate in [12]. Thus, the designs in [12] require significantly fewer T gates than the design presented in [11]. However, the designs in [12] produce significant garbage output. Thus, the dividers in [12] will have additional ancillae and T gate overhead from removing these garbage outputs. A recent design presented in [13] also depends on quantum gates that can be exactly realized with Clifford+T gates. However,

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the design methodology presented in [13] generates a quantum circuit that suffers from significant T gate and qubit cost overhead. In addition, the design in [13] produces significant garbage output. Thus, the divider in [13] will have additional ancillae and T gate overhead from removing these garbage outputs.

To address the shortcomings of the existing work this paper presents two designs for quantum circuit integer division based on Clifford+T gates. The first proposed quantum circuit is based on the restoring division algorithm and the second proposed quantum circuit is based on the non-restoring division algorithm. Both proposed quantum integer division circuits are based on: (i) a quantum subtractor, (ii) a quantum adder-subtractor circuit, and (iii) a novel quantum conditional addition circuit. The preliminary version of this paper is available in [15], [16]. The proposed quantum restoring division circuit has quadratic T-count, linear T-depth and requires $3 \cdot n$ qubits (where $n$ is the size of the inputs). The proposed non-restoring division circuit has quadratic T-count, linear T-depth and requires $3 \cdot n - 1$ qubits (where $n$ is the size of the inputs).

This paper is organized as follows: Section III discusses the background on resource cost measures, the quantum subtractor, quantum adder-subtractor circuit and the novel quantum conditional addition circuit. The proposed quantum restoring integer division circuit is presented in Section III while the comparison with the existing works is discussed and Section VI illustrates comparison with the existing works.

II. BACKGROUND

A. Quantum Gates

CLIFFORD+T GATE SET

| Gate          | Matrix Representation |
|---------------|-----------------------|
| Hadamard Gate | $\frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$ |
| T Gate        | $\begin{bmatrix} 1 & 0 \\ 0 & e^{i \frac{\pi}{2}} \end{bmatrix}$ |
| Hermitian of T Gate | $\begin{bmatrix} 1 & 0 \\ 0 & e^{-i \frac{\pi}{2}} \end{bmatrix}$ |
| Phase Gate    | $\begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix}$ |
| Hermitian of Phase Gate | $\begin{bmatrix} 1 & 0 \\ 0 & -i \end{bmatrix}$ |
| NOT Gate      | $\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$ |
| Feynman Gate  | $\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix}$ |

Fig. 1: The quantum gate set used in this work.

Fault-tolerant implementation of quantum circuits is gaining the attention of researchers because physical quantum computers are prone to noise errors [27]. Recently, researchers have implemented quantum logic gates and circuits with fault-tolerant implementations of the Clifford+T gate set due to its demonstrated tolerance to noise errors [8]. Figure 1 presents the gates that make up the Clifford+T quantum gate family. Evaluating quantum circuit performance in terms of T-count and T-depth is of interest to researchers because the fault-tolerant implementation of the T gate is significantly more costly than the fault-tolerant implementation costs of the other Clifford+T gates [10]. The number of qubits in a quantum circuit is a resource measure of interest because of the limited number of qubits available on existing quantum computers [17] [18]. We now define the T-count, T-depth and qubit cost resource measures.

- T-count: T-count is the total number of T gates used in the quantum circuit.
- T-depth: T-depth is the number of T gate layers in the circuit, where a layer consists of quantum operations that can be performed simultaneously.
- Qubit cost: Qubit cost is the total number of qubits required to design the quantum circuit.

B. Design of Quantum Subtractor

The subtractor circuit takes two $n$ bit inputs $a$ and $b$. At the end of computation, the input $a$ emerges unchanged and the input $b$ is transformed to the difference of $b$ from $a$. The quantum subtractor calculates $(b + a)$ which is equivalent to $b - a$ [19]. A quantum ripple carry adder is used to realize the quantum subtractor circuit. We use the quantum ripple carry adder proposed in [20] for developing the quantum subtractor circuit. We chose the ripple carry adder proposed in [20] because this adder has been shown in the literature to be efficient in terms of gates and has a T-depth that is constant and independent of the circuit size $n$. We determined that this quantum subtractor will have a T-count of $14 \cdot n - 14$ and a T-depth of 10. Thus, the quantum subtraction circuit used in our proposed dividers will have a T-count of order $O(n)$ and a T-depth of order $O(1)$.

C. Design of Quantum Adder-Subtractor (Add-Sub) Circuit

The quantum adder-subtractor (Add-Sub) circuit takes two $n$ bit inputs $a$ and $b$ and a single one bit input $ctrl$. Operation of the quantum Add-Sub circuit is conditioned on the value of $ctrl$. When $ctrl$ is high, the circuit calculates $b - a$. When the $ctrl$ input is low, the circuit calculates $b + a$. Quantum Add-Sub calculates $(b + a)$ when $ctrl$ is high. The expression $(b + a)$ is equivalent to $b - a$. The quantum Add-Sub circuit is based on the design presented in [19] and uses the ripple carry adder in [20]. We determined that this quantum Add-Sub circuit will have a T-count of $14 \cdot n - 14$ and a T-depth of 10. Thus, the quantum Add-Sub circuit used in our proposed dividers will have a T-count of order $O(n)$ and a T-depth of order $O(1)$.

D. Design of Quantum Conditional Addition Ctrl-Add Circuit

The quantum Ctrl-Add circuit in this work is a modified version of the Ctrl-Add circuit proposed in [27]. Operation of
the quantum Ctrl-Add circuit is conditioned on the value of \( ctrl \). When \( ctrl \) is high, the circuit calculates \( b + a \). When \( ctrl \) is low, the circuit performs no computation. An illustrative example is shown in Figure 2 for two 4 qubit operands \( a_0 \ldots a_3 \) and \( b_0 \ldots b_3 \). We are able to reduce the amount of qubits and quantum gates required because we do not need the carry out qubit in the proposed integer dividers.

We determined that our quantum Ctrl-Add circuit will have a T-count of \( 21 \cdot n - 14 \) and a T-depth of \( 2 \cdot n \). Thus, the quantum Ctrl-Add circuit used in our proposed dividers will have a T-count of order \( O(n) \) and a T-depth of order \( O(n) \).

III. PROPOSED DESIGN OF RESTORING QUANTUM INTEGER DIVISION CIRCUIT

We now present our proposed restoring quantum integer division circuit. The proposed design produces no garbage output and has lower T-count and qubit costs compared to the existing works. The quantum circuits used in our proposed quantum restoring division circuit are (i) the quantum subtractor and (ii) the quantum Ctrl-Add circuit. Our proposed quantum restoring divider saves T gates by not doing computation in the QFT domain. We also base our design on the T gate efficient quantum subtractor and the novel quantum Ctrl-Add circuit presented in Section II. The modules used in our quantum circuit do not produce garbage outputs and restore inputs to their original values. Thus, we are able to save qubits and T gates by placing these quantum circuits such that our proposed quantum restoring division circuit will produce no garbage outputs.

This proposed quantum integer division circuit calculates division by implementing the restoring division algorithm. The restoring division algorithm is illustrated in Figure 3. Prior research has demonstrated the correctness of the restoring division algorithm through functionally correct circuit implementations such as those in [11].

Consider the division of two \( n \) bit 2’s complement positive binary numbers \( a \) and \( b \). Let \( |B\rangle \) be a \( n \) bit quantum register that is initialized to the value \( b \), let \( |Q\rangle \) be a \( n \) bit quantum register that is initialized with the value \( a \) and let \( |R\rangle \) be a \( n \) bit quantum register initialized to 0. At the end of computation, the quantum register \( |B\rangle \) will be restored to the value \( b \) while the quantum register \( |R\rangle \) will have the remainder of the division of \( a \) by \( b \). At the end of computation, the quantum register \( |Q\rangle \) will have the quotient of the division of \( a \) by \( b \).

The proposed methodology is generic in nature and can design a quantum restoring integer division circuit of any size. The steps of the proposed methodology are presented along with an illustrative example of the proposed quantum restoring integer division circuit for the division of two 4 bit numbers \( a_0 \ldots a_3 \) and \( b_0 \ldots b_3 \) shown in Figure 4. The proposed methodology is repeated \( n \) times. A quantum circuit is generated for each step of the design.

A. Steps of the Proposed Design Methodology

The following steps of the proposed methodology are repeated \( n \) times. Starting with the first \( n - 1 \) iterations.

For \( i = 1 : 1 : n - 1 \):

1. Step 1: This step executes line 6 and line 8 of Algorithm 1 in quantum hardware. Step 1 is shown for a 4 bit restoring divider in Figure 4(a). This step has the following two substeps:
   1. Sub-step 1: Treat the locations \( |R_{n-1-i}\rangle \) through \( |R_0\rangle \) of quantum register \( |R\rangle \) and locations \( |Q_{n-1}\rangle \) through \( |Q_{n-i}\rangle \) of quantum register \( |Q\rangle \) as one \( n \) qubit combined quantum register \( |Y\rangle \) such that
Sub-step 1: Apply quantum register location \(|R_{n-i}\rangle\) to the quantum Ctrl-Add circuit such that the operation of the Ctrl-Add circuit will be conditioned on the value at location \(|R_{n-i}\rangle\). Quantum register location \(|R_{n-i}\rangle\) is unchanged.

After this step,

- Step 4: This step completes the execution of line 12 of Algorithm 1. Step 4 is shown for a 4 bit restoring divider in Figure 4d. At quantum register location \(|R_{n-i}\rangle\) apply a quantum NOT gate. Quantum register location \(|R_{n-i}\rangle\) now has the remainder bit \(r_{n-i}\) of the division of \(a\) by \(b\).

After this step, quantum register \(|Q\rangle\) will have the quotient of the division of \(a\) and \(b\).

Step 4: This step completes the execution of line 19 of Algorithm 1. Step 4 is shown for a 4 bit restoring divider in Figure 4e. At quantum register locations \(|R_0\rangle\) and \(|Q_{n-1}\rangle\), apply a CNOT gate such that quantum register location \(|Q_{n-1}\rangle\) is unchanged and quantum register location \(|R_0\rangle\) shall be transformed to the value \(|R_0 \oplus Q_{n-1}\rangle\).

Step 3: Steps 3 implements lines 16 through 18 of Algorithm 1 in quantum hardware. Step 3 is shown for a 4 bit restoring divider in Figure 4e. Step 3 has the following two sub-steps:

- Sub-step 1: Apply the quantum registers \(|B\rangle\) and \(|Y\rangle\) to the quantum Ctrl-Add circuit such that the quantum register \(|B\rangle\) will be unchanged and quantum register \(|Y\rangle\) will contain the result of computation.

- Sub-step 2: Apply quantum register location \(|R_{n-i}\rangle\) to the quantum Ctrl-Add circuit such that the operation of the Ctrl-Add circuit will be conditioned on the value at location \(|R_{n-i}\rangle\). Quantum register location \(|R_{n-i}\rangle\) is unchanged.

The final iteration has the following steps:

- Step 1: This step executes line 15 of Algorithm 1 in quantum hardware. Step 1 is shown for a 4 bit restoring divider in Figure 4a. Apply quantum register \(|B\rangle\) and quantum register \(|Q\rangle\) to the quantum subtraction circuit so that, at the end of computation, \(|B\rangle\) is unchanged and \(|Q\rangle\) has the result of computation.

- Step 2: This step prepares register location \(|R_0\rangle\) for use in subsequent steps and partially completes the execution of line 19 of Algorithm 1. Step 2 is shown for a 4 bit restoring divider in Figure 4a. At quantum register locations \(|R_0\rangle\) and \(|Q_{n-1}\rangle\), apply a CNOT gate such that quantum register location \(|Q_{n-1}\rangle\) is unchanged and quantum register location \(|R_0\rangle\) shall be transformed to the value \(|R_0 \oplus Q_{n-1}\rangle\).

- Step 3: Steps 3 implements lines 16 through 18 of Algorithm 1 in quantum hardware. Step 3 is shown for a 4 bit restoring divider in Figure 4e. Step 3 has the following two sub-steps:

The values at locations \(|Q_{n-1}\rangle\) through \(|Q_{n-i}\rangle\) will occupy locations \(|Y_{n-1}\rangle\) through \(|Y_0\rangle\) and locations \(|R_{n-i}\rangle\) through \(|R_0\rangle\) will occupy locations \(|Y_{n-1}\rangle\) through \(|Y_0\rangle\).

- Sub-step 2: Apply quantum register \(|B\rangle\) and quantum register \(|Y\rangle\) to the quantum subtraction circuit so that, at the end of computation, \(|B\rangle\) is unchanged and \(|Y\rangle\) has the result of computation.

Figure 5 shows the complete proposed quantum restoring division circuit for the division of two 4 bit numbers \(a_0 \ldots a_3\) and \(b_0 \ldots b_4\).
circuit is illustrated shortly for each step of the proposed design methodology.

A. T-Count Analysis

The T-count of the proposed quantum integer division circuit is illustrated shortly for each step of the proposed design methodology. The steps are iterated \( n \) times.

- The T-count for Step 1 is \( 14 \cdot n - 14 \). We use a quantum subtraction circuit of T-count \( 14 \cdot n - 14 \) in this step.
- Steps 2 does not require T gates.
- The T-count for Step 3 is \( 21 \cdot n - 14 \). We use a quantum Ctrl-Add circuit of T-count \( 21 \cdot n - 14 \) in this step.
- Steps 4 does not require T gates.

We determine the T-count for a single iteration of the proposed design by summing the T-count for each step in the methodology as shown below:

\[
14 \cdot n - 14 + 21 \cdot n - 14
\]

This expression can be simplified to the following:

\[
35 \cdot n - 28
\]

The steps in the proposed methodology are iterated \( n \) times. Thus the T-count for the proposed restoring division circuit is \( n \cdot (35 \cdot n - 18) \) which simplifies to the expression shown below:

\[
35 \cdot n^2 - 28 \cdot n
\]

B. T-Depth Analysis

The T-depth of the proposed quantum integer division circuit is illustrated shortly for each step of the proposed design methodology. Our proposed design is based on T-depth efficient designs of quantum subtraction circuits and quantum Ctrl-Add circuits. We determined that garbageless and T gate optimized quantum subtraction circuits in the literature such as the design in [19] have a T-depth that is constant and independent of the circuit size \( n \). Thus, these subtraction circuits have T-depth of order \( O(1) \). We determined as well that Ctrl-Add circuits in the literature such as the design in [21] scale as a function of circuit size \( n \). Thus, these Ctrl-Add circuits have a T-depth of order \( O(n) \).

The T-depth of the proposed quantum integer division circuit is illustrated shortly for each step of the proposed design methodology. The steps are iterated \( n \) times.

- Step 1 has a constant T-depth of 10. This T-depth is seen by locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) of quantum register \(|B\rangle\). We use a quantum subtraction circuit of constant T-depth 10 in this step (where T-depth is independent of circuit size \( n \)).
- Step 2 does not require T gates.
- Step 3 has a T-depth of \( 2 \cdot n \). This T-depth is seen by location \(|R_{n-1}\rangle\) of quantum register \(|R\rangle\) (where \( 0 \leq i \leq n-1 \)). We use a quantum Ctrl-Add circuit of T-depth \( 2 \cdot n \) in this step.
- Step 4 does not require T gates.

We now illustrate the steps we use to determine the total T-depth for the proposed quantum restoring integer division circuit.

- Step 1: Calculate the total T-depth for quantum register \(|B\rangle\). We determine the T-depth for quantum register \(|B\rangle\) for each step of the proposed methodology.
  - Step 1: Locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) of quantum register \(|B\rangle\) see 10 T gate layers.
  - Step 2 does not require T gates
  - Step 3: Locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) of quantum register \(|B\rangle\) see 13 T gate layers.
  - Step 4 does not require T gates.

Thus, quantum register \(|B\rangle\) has a T-depth of \( 23 \cdot n \).

- Step 2: Calculate the total T-depth for quantum register \(|R\rangle\). We first consider iterations 1 through \( n-1 \). For iteration \( i \) (where \( 1 \leq i \leq n-1 \)), we determine the T-depth for quantum register \(|R_i\rangle\) for each step of the proposed methodology.
  - Step 1: Locations \(|R_{n-2-i}\rangle\) through \(|R_0\rangle\) of quantum register \(|R\rangle\) see 4 T gate layers. After iteration \( n-2 \), only location \(|R_0\rangle\) of quantum register \(|R\rangle\) will see T gate layers. In iteration \( n-1 \), \(|R\rangle\) will not see any T gate layers.
  - Step 2 does not require T gates
  - Step 3: Locations \(|R_{n-i}\rangle\) sees \( 2 \cdot n \) T gate layers while \(|R_{n-2-i}\rangle\) through \(|R_0\rangle\) of quantum register \(|R\rangle\) see 6 T gate layers. After iteration \( n-2 \), only locations \(|R_2\rangle\) and \(|R_0\rangle\) of quantum register \(|R\rangle\) will see T gate layers. In iteration \( n-1 \), only location \(|R_1\rangle\) will see any T gate layers.
  - Step 4 does not require T gates.

Thus, a single iteration of the proposed design see a T-depth of \( 2 \cdot n \) on quantum register location \(|R_{n-1}\rangle\). We now consider the final iteration of the proposed design:

- Step 1: No locations of quantum register \(|R\rangle\) see T gate layers.
- Step 2 does not require T gates
- Step 3: Location \(|R_0\rangle\) sees \( 2 \cdot n \) T gate layers.
- Step 4 does not require T gates.
Thus, the final iteration of the proposed design sees a T-depth of $2 \cdot n$ on quantum register location $|R_0\rangle$. We calculate the total T-depth seen by each location in register $|R\rangle$ and determined that location $|R_0\rangle$ sees the most T gate layers, a total of $12 \cdot n - 18$ T gate layers.

- **Step 3:** Calculate the total T-depth for quantum register $|Q\rangle$. We first consider iterations 1 through $n - 1$. For iteration $i$ (where $1 \leq i \leq n - 1$), we determine the T-depth for quantum register $|Q\rangle$ for each step of the proposed methodology:
  - **Step 1:** Locations $|Q_{n-1}\rangle$ through $|Q_{n-i}\rangle$ of quantum register $|Q\rangle$ see 4 T gate layers.
  - **Step 2** does not require T gates
  - **Step 3:** Locations $|Q_{n-1}\rangle$ through $|Q_{n-i}\rangle$ of quantum register $|Q\rangle$ see 6 T gate layers.
  - **Step 4** does not require T gates.

Thus, a single iteration of the proposed design sees a T-depth of 10 on quantum register location $|Q_{n-1}\rangle$ through $|Q_{n-i}\rangle$. We now consider the final iteration of the proposed design:

- **Step 1:** Locations $|Q_{n-2}\rangle$ through $|Q_0\rangle$ of quantum register $|Q\rangle$ see 4 T gate layers.
- **Step 2** does not require T gates
- **Step 3:** Locations $|Q_{n-2}\rangle$ through $|Q_0\rangle$ of quantum register $|Q\rangle$ see 6 T gate layers.
- **Step 4** does not require T gates.

Thus, the final iteration of the proposed design sees a T-depth of 10 on quantum register locations $|Q_{n-2}\rangle$ through $|Q_0\rangle$. We calculate the total T-depth seen by each location in register $|Q\rangle$ and determined that location $|Q_{n-1}\rangle$ sees the most T gate layers. Location $|Q_{n-1}\rangle$ sees $10 \cdot n - 8$ T gate layers.

- **Step 4:** Determine which quantum register sees the most T gate layers. In our proposed design the T-depth for each quantum register is given as:
  - Quantum register $|Q\rangle$ has a T-depth of $10 \cdot n - 8$.
  - Quantum register $|R\rangle$ has a T-depth of $12 \cdot n - 18$.
  - Quantum register $|B\rangle$ has a T-depth of $23 \cdot n$.

Quantum register $|B\rangle$ sees the most T gate layers because $23 \cdot n > 12 \cdot n - 18$ and $23 \cdot n > 10 \cdot n - 8$. Thus, the T-depth for our proposed quantum restoring integer division circuit is $23 \cdot n$. This T-depth is seen by location $|B_1\rangle$ through $|B_{n-2}\rangle$ of quantum register $|B\rangle$.

### TABLE I: Comparison of Resource Count Between Proposed and Existing Work

|      | Proposed | 1 | 2 | % Improvement w.r.t. 1 | % Improvement w.r.t. 2 |
|------|----------|---|---|------------------------|------------------------|
| $n$  | $1$      | $2$ | $\text{Proposed}$ | $\text{% Improvement \, w.r.t. \, 1}$ | $\text{% Improvement \, w.r.t. \, 2}$ |
| $4$  | $16$     | $48$ | $12$ | $25.00$ | $75.00$ |
| $8$  | $32$     | $288$ | $24$ | $25.00$ | $91.67$ |
| $16$ | $64$     | $2112$ | $48$ | $25.00$ | $97.73$ |
| $32$ | $128$    | $16512$ | $96$ | $25.00$ | $99.42$ |
| $64$ | $256$    | $131328$ | $192$ | $25.00$ | $99.85$ |
| $128$| $512$    | $1049088$ | $384$ | $25.00$ | $99.96$ |
| $256$| $1024$   | $8308632$ | $768$ | $25.00$ | $99.99$ |
| $512$| $2048$   | $6710912$ | $1536$ | $25.00$ | $99.99$ |

Average: $25.00 \approx 93.94$

1 is the design by Khosropour et al. [11]
2 is the design by Dibbo et al. [13] modified to remove garbage output.

### TABLE II: T-count Comparison of Quantum Integer Division Circuits

|      | $1$ | $2$ | Proposed | % Improvement w.r.t. 1 | % Improvement w.r.t. 2 |
|------|-----|-----|----------|------------------------|------------------------|
| $n$  | $1$ | $2$ | $\text{Proposed}$ | $\text{% Improvement \, w.r.t. \, 1}$ | $\text{% Improvement \, w.r.t. \, 2}$ |
| $4$  | $16$ | $48$ | $12$ | $25.00$ | $75.00$ |
| $8$  | $32$ | $288$ | $24$ | $25.00$ | $91.67$ |
| $16$ | $64$ | $2112$ | $48$ | $25.00$ | $97.73$ |
| $32$ | $128$ | $16512$ | $96$ | $25.00$ | $99.42$ |
| $64$ | $256$ | $131328$ | $192$ | $25.00$ | $99.85$ |
| $128$| $512$ | $1049088$ | $384$ | $25.00$ | $99.96$ |
| $256$| $1024$ | $8308632$ | $768$ | $25.00$ | $99.99$ |
| $512$| $2048$ | $6710912$ | $1536$ | $25.00$ | $99.99$ |

Average: $25.00 \approx 93.94$

1 is the design by Khosropour et al. [11]
2 is the design by Dibbo et al. [13] modified to remove garbage output.

### TABLE III: Qubit Cost Comparison of Quantum Integer Division Circuits

|      | $1$ | $2$ | Proposed | % Improvement w.r.t. 1 | % Improvement w.r.t. 2 |
|------|-----|-----|----------|------------------------|------------------------|
| $n$  | $1$ | $2$ | $\text{Proposed}$ | $\text{% Improvement \, w.r.t. \, 1}$ | $\text{% Improvement \, w.r.t. \, 2}$ |
| $4$  | $16$ | $48$ | $12$ | $25.00$ | $75.00$ |
| $8$  | $32$ | $288$ | $24$ | $25.00$ | $91.67$ |
| $16$ | $64$ | $2112$ | $48$ | $25.00$ | $97.73$ |
| $32$ | $128$ | $16512$ | $96$ | $25.00$ | $99.42$ |
| $64$ | $256$ | $131328$ | $192$ | $25.00$ | $99.85$ |
| $128$| $512$ | $1049088$ | $384$ | $25.00$ | $99.96$ |
| $256$| $1024$ | $8308632$ | $768$ | $25.00$ | $99.99$ |
| $512$| $2048$ | $6710912$ | $1536$ | $25.00$ | $99.99$ |

Average: $25.00 \approx 93.94$

1 is the design by Khosropour et al. [11]
2 is the design by Dibbo et al. [13] modified to remove garbage output.
that our proposed design methodology achieves improvement ratios ranging from 91.26% to 93.00% and 22.22% to 99.24% compared to the designs by Khosropour et al. and the design by Dibbo et al. in terms of T-count.

2) Cost Comparison in Terms of Qubits: Table II shows that our proposed design and the design by Khosropour et al. have qubit costs of order $O(n)$ while the qubit cost for the design by Dibbo et al. is of order $O(n^3)$. We also compared the qubit cost of our proposed design methodology to the designs presented by Khosropour et al. and Dibbo et al. for values of $n$ ranging from 4 to 512 in Table II. We calculated that our proposed design methodology achieves an improvement ratio of 25.00% compared to the design by Khosropour et al. We determined that our proposed design achieves improvement ratios ranging from 75.00% to 99.99% compared to the design by Dibbo et al.

3) Cost Comparison in Terms of T-depth: The T-depth cost of the proposed design and designs by Khosropour et al. and the proposed design are $O(n)$. A closed-form T-depth expression is not available for the design by Dibbo et al. We calculated that the design by Khosropour et al. has a T-depth that is 5.6 times higher than the T-depth of the proposed work.

V. PROPOSED DESIGN OF NON-RESTORING QUANTUM INTEGER DIVISION CIRCUIT

We now present our proposed non-restoring quantum integer division circuit. The proposed design produces no garbage output and has lower T-count and qubit costs compared to the existing work. The quantum circuits required to build our proposed quantum non-restoring division circuit are (i) the quantum subtractor, (ii) the quantum Add-Sub circuit and (iii) the quantum Ctrl-Add circuit. Our proposed quantum non-restoring divider saves T gates by not doing computation in the QFT domain. We also base our design on the T gate efficient quantum subtractor, quantum Add-Sub circuit and the novel quantum Ctrl-Add circuit presented in Section II. The modules used in our proposed quantum circuit do not produce garbage outputs and restore inputs to their original values. Thus, we are able to save qubits and T gates by placing these quantum circuits such that our proposed quantum restoring division circuit will produce no garbage outputs. We are able to save additional qubits and T gates because the remainder will be at most $n - 1$ bits wide when we divide two $n$ bit numbers with our proposed divider.

This proposed quantum integer division circuit calculates division by implementing the non-restoring division algorithm. The non-restoring division algorithm is illustrated in Figure 6. Existing research has demonstrated the correctness of the non-restoring division algorithm through functionally correct circuit implementations such as those in [23] [16].

Consider the division of two $n$ bit 2’s complement positive binary numbers $a$ and $b$. Let $|B\rangle$ be a $n$ bit quantum register where that is initialized to the value $b$, let $|R\rangle$ be a $n - 1$ quantum register where each register location is initialized with the value $a_i$ for $0 \leq i \leq n - 2$ and let $|Q\rangle$ be a $n$ bit quantum register where register location $|Q_0\rangle$ is initialized with the value $a_{n-1}$ and the remaining $n - 1$ locations in $|Q\rangle$ are initialized to 0. At the end of computation, the quantum register $|B\rangle$ will be restored to the value $b$ while the quantum register $|R\rangle$ will have the remainder of the division of $a$ by $b$. At the end of computation, the quantum register $|Q\rangle$ will have the quotient of the division of $a$ by $b$.

The proposed methodology is generic in nature and can design a quantum non-restoring integer division circuit of any size. The steps of the proposed methodology are presented along with an illustrative example of the proposed quantum non-restoring integer division circuit for the division of two 6 bit numbers $a_0 \ldots a_5$ and $b_0 \ldots b_5$ shown in Figure 7. The proposed methodology has three steps. A quantum circuit is generated for each step of the design.

### Algorithm 2: Non-restoring division algorithm

**Function Non-Restoring($a$, $b$)**

Requirements: $a$ and $b$ are positive and 2’s complement.

- Takes $2$ $n$ bit values $a$ and $b$ as input.
- Returns the quotient as an $n$ bit number $Q$ and the remainder from the division as an $n - 1$ bit number $R$.

```plaintext
R = 0^{n-1}; // Where 0^{n-1} are n - 1 zeros.
Q = 0^{n-1}a_{n-1}; // Where 0^{n-1} are n - 1 zeros.
// Q’s least significant bit has the value $a_{n-1}$
// $a_{n-1}$ is the most significant bit of $a$.
Q = Q - b

For $i = 1$ to $n - 1$
    $Q_{n-i} = Q_{n-i-1}$
    $Y = Q_{n-i-1} \cdots Q_0 R_{n-2} \cdots R_{n-1-i}$
    // Where $Q_{n-1-i}$ is the most significant bit of $Y$.
    // significant bit of $Y$.
    If $(Q_{n-i} = 0)$
        $Y = Y + b$
    Else
        $Y = Y - b$
End
End
End
If $(R < 0)$
    $R = R + b$
End
Q_0 = Q_0

Return $Q, R$
```

Fig. 6: The non-restoring division algorithm.

- Step 1: This step executes line 5 of Algorithm 2 in quantum hardware. Step 1 is shown for a 6 bit restoring divider in Figure 6. Apply the quantum registers $|Q\rangle$ and $|B\rangle$ to a quantum subtraction circuit such that, at the end of computation, the quantum register $|B\rangle$ is
The final Iteration of Step 2 is shown for a 6 bit restoring divider in Figure 7d. This step has the following sub-steps:

- **Sub-step 1:** Apply locations \(|B_{n-2}\rangle\) through \(|B_0\rangle\) of quantum register \(|B\rangle\) and quantum register \(|R\rangle\) to a quantum Ctrl-Add circuit such that the operation of the circuit is conditioned on the value at register \(|Q_{n-1}\rangle\). Location \(|Q_{n-1}\rangle\) is unchanged. If \(|Q_{n-1}\rangle = 0\), this step executes line 13 of Algorithm 2. If \(|Q_{n-1}\rangle = 1\), this step executes line 15 of Algorithm 2.

- **Step 3:** This step executes lines 19 through 22 of Algorithm 2 in quantum hardware. Step 3 is shown for a 6 bit restoring divider in Figure 7e. We show the steps for iteration \(i\) where 1 ≤ \(i \leq n - 1\).

  - **Sub-step 1:** This sub-step executes line 9 of Algorithm 2 in quantum hardware. Treat the locations \(|R_{n-2}\rangle\) through \(|R_{n-1-i}\rangle\) of quantum register \(|R\rangle\) and locations \(|Q_{n-1-i}\rangle\) through \(|Q_0\rangle\) of register \(|Q\rangle\) as a combined quantum register \(|Y\rangle\). The values at locations \(|R_{n-2}\rangle\) through \(|R_{n-1-i}\rangle\) will occupy locations \(|Y_{n-1}\rangle\) through \(|Y_0\rangle\) and the values at locations \(|Q_{n-1-i}\rangle\) to \(|Q_0\rangle\) will occupy locations \(|Y_{n-1}\rangle\) through \(|Y_i\rangle\).

- **Sub-step 2:** This sub-step executes line 8 of Algorithm 2 in quantum hardware and prepares location \(|Q_{n-1-i}\rangle\) for use in subsequent sub-steps. At quantum register location \(|Q_{n-1}\rangle\) apply a quantum NOT gate. Location \(|Q_{n-1}\rangle\) now has the quotient bit \(q_{n-i}\) of the division of \(a\) by \(b\).

- **Sub-step 3:** Apply the quantum registers \(|B\rangle\) and \(|Y\rangle\) to a quantum Add-Sub circuit such that \(|B\rangle\) is unchanged while \(|Y\rangle\) will hold the result of computation.

- **Sub-step 4:** Apply the quantum register location \(|Q_{n-1}\rangle\) to the quantum Add-Sub circuit such that the operation of the circuit is conditioned on the value at location \(|Q_{n-1}\rangle\). Location \(|Q_{n-1}\rangle\) is unchanged. If \(|Q_{n-1}\rangle = 0\), this step executes line 13 of Algorithm 2. If \(|Q_{n-1}\rangle = 1\), this step executes line 15 of Algorithm 2.

**VI. Cost Analysis of the Proposed Non-Restoring Division Circuit**

**A. T-Count Analysis**

The T-count of the proposed quantum integer division circuit is illustrated shortly for each step of the proposed design methodology:

- The T-count for Step 1 is \(14 \cdot n - 14\). We use a quantum subtraction circuit of T-count \(14 \cdot n - 14\) in this step.
- Step 2 is repeated \(n - 1\) times. The T-count for each iteration of Step 2 is \(14 \cdot n - 14\). We use a quantum Add-Sub circuit of T-count \(14 \cdot n - 14\) in this step.
- The T-count for Step 3 is \(21 \cdot n - 21\). We use a quantum Ctrl-Add circuit of size \(n - 1\) in this step. We use a quantum Ctrl-Add circuit of T-count \(21 \cdot n - 14\) in this step.
We determine the total T-count by summing the T-count for each step in the design as shown below:

\[ 14 \cdot n - 14 + (14 \cdot n - 14) \cdot (n - 1) + 21 \cdot n - 21 \]

This expression can be simplified to the following:

\[ 14 \cdot n^2 + 7 \cdot n - 35 \] (4)

B. T-depth Cost

The T-depth of the proposed quantum integer division circuit is illustrated shortly for each step of the design methodology. Our proposed design is based on T-depth efficient designs of quantum subtractors, quantum Add-Sub circuits and quantum Ctrl-Add circuits. We determined that garbageless and T gate optimized quantum subtractor and quantum Add-Sub circuits in the literature such as the designs in [19] have a T-depth that is constant and independent of the circuit size \( n \). Thus, these quantum circuits have T-depth of order \( O(1) \). We determined as well that Ctrl-Add circuits in the literature such as the design in [21] scale as a function of circuit size \( n \).

Thus, these Ctrl-Add circuits have a T-depth of order \( O(n) \).

- Step 1 has a constant T-depth of 10. This T-depth is seen by locations \( |B_1\rangle \) through \( |B_{n-2}\rangle \) of quantum register \( |B\rangle \). We use a quantum subtraction circuit of constant T-depth 10 in this step (where T-depth is independent of circuit size \( n \)).
- Step 2 is repeated \( n - 1 \) times. The \( i \)th iteration of Step 2 (where \( 1 \leq i \leq n - 1 \)) has a constant T-depth of 10. This T-depth is seen by locations \( |B_i\rangle \) through \( |B_{n-2}\rangle \) of quantum register \( |B\rangle \). We use a quantum Add-Sub circuit of constant T-depth 10 in this step (where T-depth is independent of circuit size \( n \)).
- Step 3 has a T-depth of \( 2 \cdot n \). This T-depth is seen by location \( |Q_0\rangle \) of quantum register \( |Q\rangle \). We use a quantum Ctrl-Add circuit of T-depth \( 2 \cdot n \) in this Step.

We now illustrate the steps to determine the total T-depth for the proposed quantum integer division circuit:

1) Calculate the T-depth for Step 1. Step 1 has a T-depth of 10. This T-depth is seen by locations \( |B_1\rangle \) through

\[ \approx 9 \cdot n^3 + 7 \cdot n + 7 \]

\[ 2 \cdot n^2 + 5 \cdot n - 1 \]

\[ 3 \cdot n^2 + 14 \cdot n \]

\[ \approx \frac{1}{3} n^3 + 4 \cdot n \]

\[ 3 \cdot n - 1 \]

1 and 2 are the designs by Jamal et al. [23] modified to remove garbage output.
3 is the design by Dibbo et al. [13] modified to remove garbage output.

Table entries are marked NA where a closed-form expression is not available for the designs by Jamal et al. and Dibbo et al.

### Table IV: Comparison of Quantum Integer Division Circuits

|          | 1         | 2         | 3         | Proposed |
|----------|-----------|-----------|-----------|----------|
| T count  | 28 \cdot n^2 | 42 \cdot n^2 + 28 \cdot n | \approx 9 \cdot n^3 | 14 \cdot n^2 + 7 \cdot n + 7 |
| T-depth  | NA        | NA        | NA        | 10 \cdot n + 13 |
| qubits  | 2 \cdot n^2 + 5 \cdot n - 1 | 3 \cdot n^2 + 14 \cdot n | \approx \frac{1}{3} n^3 + 4 \cdot n | 3 \cdot n - 1 |

1 and 2 are the designs by Jamal et al. [23] modified to remove garbage output.
3 is the design by Dibbo et al. [13] modified to remove garbage output.

### Table V: T-count Comparison of Quantum Integer Division Circuits

| \( n \) | 1      | 2      | 3      | Proposed |
|--------|--------|--------|--------|----------|
|        | % Impr. w.r.t. 1 | % Impr. w.r.t. 2 | % Impr. w.r.t. 3 |
| 4      | 51.56  | 72.32  | \approx 62.33 |
| 8      | 48.83  | 68.51  | \approx 80.10 |
| 16     | 48.93  | 67.31  | \approx 90.07 |
| 32     | 49.34  | 66.92  | \approx 95.07 |
| 64     | 49.64  | 66.77  | \approx 97.55 |
| 128    | 49.81  | 66.71  | \approx 98.78 |
| 256    | 49.90  | 66.69  | \approx 99.39 |
| 512    | 49.95  | 66.68  | \approx 99.70 |

Average: 49.75 67.74 90.37

### Table VI: Qubit Cost Comparison of Quantum Integer Division Circuits

| \( n \) | 1      | 2      | 3      | Proposed |
|--------|--------|--------|--------|----------|
|        | % Impr. w.r.t. 1 | % Impr. w.r.t. 2 | % Impr. w.r.t. 3 |
| 4      | 78.43  | 89.42  | \approx 77.08 |
| 8      | 86.23  | 92.43  | \approx 92.01 |
| 16     | 92.05  | 95.26  | \approx 97.77 |
| 32     | 95.70  | 97.30  | \approx 99.42 |
| 64     | 97.76  | 98.55  | \approx 99.85 |
| 128    | 98.85  | 99.25  | \approx 99.96 |
| 256    | 99.42  | 99.62  | \approx 99.99 |
| 512    | 99.71  | 99.81  | \approx 99.99 |

Average: 93.52 96.46 95.76

1 and 2 are the two designs from Jamal et al. [23] modified to remove garbage output.
3 is the design by Dibbo et al. [13] modified to remove garbage output.
2) Calculate the T-depth for all iterations of Step 2. The total T-depth for all iteration of Step 2 has a T-depth of \(10 \cdot (n - 1)\) because each iteration of Step 2 requires a quantum Add-Sub circuit. The total T-depth \(10 \cdot (n - 1)\) simplifies to \(10n - 10\). This T-depth is seen by locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) of quantum register \(|B\rangle\).

3) Calculate the T-depth for Step 3. Step 3 has a T-depth of \(2 \cdot n\). This T-depth is seen by location \(|Q_0\rangle\) of quantum register \(|Q\rangle\).

4) Determine which qubits see the most T gate layers. We find after comparing all the qubits in our proposed design, quantum register location \(|Q_0\rangle\) of quantum register \(|Q\rangle\) and quantum register locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) of quantum register \(|B\rangle\) are the most T gate layers.

5) Determine the total number of T gate layers seen by quantum register location \(|Q_0\rangle\) in the proposed design. Quantum register \(|Q_0\rangle\) will see a total of \(6 \cdot n - 4\) T gate layers because in Step 1 location \(|Q_0\rangle\) sees 4 T gate layers, in Step 2 location \(|Q_0\rangle\) sees \(4 \cdot (n - 2)\) T gate layers and in Step 2 location \(|Q_0\rangle\) sees \(2 \cdot n\) T gate layers. The total number of T gate layers seen by location \(|Q_0\rangle\) is \(4 + 4 \cdot (n - 2) + 2 \cdot n\) which simplifies to \(6 \cdot n - 4\).

6) Determine the total number of T gate layers seen by quantum register locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) in the proposed design. Quantum register locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) will see a total of \(10 \cdot n + 13\) T gate layers because in Step 1 locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) see 10 T gate layers, in Step 2 locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) sees \(10 \cdot (n - 1)\) T gate layers and in Step 3 locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) see 13 T gate layers. The total number of T gate layers seen by locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) is \(10 + 10 \cdot (n - 1) + 13\) which simplifies to \(10 \cdot n + 13\).

7) Determine which qubits see the most T gate layers. We determined that locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) see more T gate layers than register location \(|Q_0\rangle\) because \(10 \cdot n + 13 > 6 \cdot n - 4\).

Thus, our proposed design has a T-depth of \(10 \cdot n + 13\) and this T-depth is seen by locations \(|B_1\rangle\) through \(|B_{n-2}\rangle\) of quantum register \(|B\rangle\).

C. Cost Comparison

Comparison of the proposed design with the current state of the art are presented in Tables IV and VII. We compare our proposed design to the existing quantum non-restoring division circuits by Jamal et al. [23] and the alternative design methodology presented in Dibbo et al. [13]. To perform the comparison we implemented each design with Clifford+T gates. To realize reversible gates such as the Toffoli gate, we use the Clifford+T implementations presented in [8]. As shown in [8], the Toffoli gate has a T-count of 7 and a T-depth of 3. We also apply the Bennett’s garbage removal scheme illustrated in [22] to remove the garbage outputs from each design presented by Jamal et al. and Dibbo et. al. We determined the qubit cost for each design in Jamal et. al. by summing the qubits required for the quotient, remainder, garbage outputs, and primary inputs. We estimated the qubit cost for each design by summing the qubits required for the quotient, remainder, garbage outputs, and primary inputs.

1) Cost Comparison in Terms of T-count: Table VII illustrates that the T-count cost of the proposed design and the designs by Jamal et al. are \(O(n^2)\). The design by Dibbo et. al. has a T-count cost of order \(O(n^3)\). Table VII shows that our proposed design methodology achieves improvement ratios ranging from 49.95% to 51.56%, 66.68% to 72.92% and 62.33% to 99.70% compared to the designs by Jamal et al. and the design by Dibbo et. al. in terms of T-count.

2) Cost Comparison in Terms of Qubits: Table VII shows that our proposed design has a qubit cost of order \(O(n)\) while the qubit cost for the designs by Jamal et al. are of order \(O(n^2)\). Table VII also illustrates that the design by Dibbo et. al. has a qubit cost of order \(O(n^3)\). Table VII shows the comparison of our proposed design methodology to the designs presented by Jamal et al. and Dibbo et. al. for values of \(n\) ranging from 4 to 512 in terms of qubit cost. We calculated that our proposed design methodology achieves improvement ratios ranging from 78.43% to 99.71%, 89.42% to 99.81% and 77.08% to 99.99% compared to the designs by Jamal et al. and the design by Dibbo et al.

3) Cost Comparison in Terms of T-depth: The T-depth cost of the proposed design is \(O(n)\). A closed-form expression is not available for the designs by Jamal et al. and the design by Dibbo et. al. for the T-depth.

VII. Conclusion

In this work, we have proposed two designs for quantum circuit integer division based on Clifford+T gates. The first quantum integer division circuit proposed is based on the restoring division algorithm and the second is based on the non-restoring division algorithm. We also show the design of components used in our proposed quantum integer division circuits such as the quantum subtraction circuit, quantum Add-Sub circuit and quantum Ctrl-Add circuit. The proposed quantum restoring division circuit is shown to be superior to existing designs in terms of T-depth, T-count and qubits. Likewise, the proposed quantum non-restoring division circuit is shown to be superior to existing designs in terms of T-count and qubits. We conclude that the proposed restoring division circuit or proposed non-restoring division circuit can be integrated in a larger quantum data path system design where T-count and T-depth are of primary concern.

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