Reduction in Circulating Current with Improved Secondary Side Modulation in Isolated Current-Fed Half Bridge AC-DC Converter

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Abstract—Current-fed half bridge converter with bidirectional switches on ac side and a full bridge converter on dc side of a high frequency transformer is an optimal topology for single stage galvanically isolated ac-dc converter for onboard vehicle charging application. AC side switches are actively commutated to achieve zero current switching (ZCS) using single phase shift modulation (SPSM) and discontinuous current phase shift modulation (DCPSM). Furthermore, zero voltage turn-on (ZVS) is achieved for dc side switches. Compared to SPSM, DCPSM maintains a constant peak current in the converter throughout the grid cycle of ac mains voltage. However, constant peak current contributes to a high circulating current near the zero crossings of ac mains voltage and also at light load conditions. This paper proposes an improved discontinuous current phase shift modulation (IDCPSM) to increase the efficiency of the converter across different loading conditions. A dual control variable is adopted to actively reduce the circulating current while maintaining soft switching of both ac and dc side switches across the grid cycle of ac mains voltage. A 1.5 kW laboratory prototype has been developed to experimentally validate the analysis, design and improvement in performance for different loading conditions.

Index Terms—Current-fed half bridge, ac-dc converter, single stage, improved discontinuous current phase shift modulation (IDCPSM)

I. INTRODUCTION

Electric vehicles (EVs) have gained tremendous popularity against their internal combustion engine (ICE) counterparts over the past decade. As EVs are becoming more common, ac-dc power converters are being explored for onboard charging applications (OBCs). OBCs provide the user with the convenience of using an ac utility outlet to charge the EVs battery. The design of an OBC is mainly driven by electrical and volumetric efficiency [1]. These ac-dc power converters should meet power quality standards on the grid side as per IEEE 519 [2]. Such converters should also have galvanic isolation between the ac side (grid) and the dc side (vehicle battery) as per Underwriters Laboratories (UL) 2202 safety standard [3].

The most general approach to attain the above requirements is a two-stage solution. An active power factor correction circuit as the first stage followed by an isolated dc-dc converter as second stage [4], [5]. The isolated DC-DC converter is realized by a dual active bridge (DAB) in [4] and series resonant converter in [5]. However, the two-stage approach increases device count and losses, contributing to lower efficiency, along with increase in control complexity and volume. To overcome the disadvantages of the two-stage solution, several single-stage approaches, which could be either voltage-fed or current-fed, have been reported in the literature [6]–[9].

Current-fed isolated converters have some distinct advantages over the voltage-fed isolated converters, such as lower input current ripple, inherent short circuit protection, wide soft-switching operating range and ease of current control [10], [11]. Work presented in [12] exhaustively compared the various isolated current-fed (ICF) topologies in terms of electrical and volumetric efficiency and reported that the L-L type isolated current-fed half-bridge (ICFHB) is an optimal topology among the different ICF topologies. Thus, an L-L type single stage single phase ICFHB ac-dc converter using bidirectional switches proposed in [13] is the focus of this paper. This converter shown in Fig. 1 is conceptually derived from an L-L type ICFHB dc-dc converter [14].

However, one major drawback of such converters is that a huge voltage spike appears at the switching node caused by an abrupt change in the current through the high frequency transformer (HFT) winding. It occurs at the instant when the boost inductor current finds a path through the HFT windings. A common technique to mitigate the problem of voltage spike is to use an additional active clamp circuit. An active clamp circuit consisting of two active switches and a clamping capacitor was proposed in [15] for L-L type ICFHB. This clamp circuit assisted in zero voltage switching (ZVS) of all the switches. Another active clamp circuit consisting of a single switch, two diodes, a clamping capacitor and a resonant inductor was proposed in [16] that ensures zero current switching (ZCS) of the main primary side switches. This increased component count in the auxiliary clamp circuit attributes to higher losses.

Another technique is the modulation based approach also known as secondary side modulation (SSM) [14], [17]–[20]. The secondary side voltage-fed full bridge (VFFB) is used for active current commutation at the primary side current-fed half bridge (CFHB). This is achieved by using the reflected output voltage to completely transfer the boost inductor current from the commutating leg to the non-commutating leg through the HFT. The reflected output voltage is applied across the primary side of the HFT for a sufficiently long duration to force the current through the commutating leg in the reverse direction, through the body diode. When the body diode current naturally reaches zero, the switch is turned-off achieving ZCS. Also, body diode conduction in the secondary side ensures ZVS...
A single phase shift modulation (SPSM) for an L-L type ICFHB is proposed in [4]. The phase shift $\phi$ is between the primary and secondary side bridge gating signals. Soft switching is achieved in both bridge switches for a wide operating range. However, when implemented in the case of the converter shown in Fig. 1 with ac input, the circulating current flowing through the switches and the HFT is substantially high near the zero crossing of the ac mains voltage and at light load conditions, attributing to poor efficiency of the converter.

A discontinuous current single phase shift modulation (DCPSM) is proposed in [17] where the current through the HFT drops to zero and a resonance occurs between the output capacitance of the dc side switches and the leakage inductance of the transformer. The circulating current flowing through the devices is still relatively large near the zero crossing of the ac mains voltage. A discontinuous current dual phase shift modulation (DCDPSM) for an L-L type ICFHB dc-dc converter is proposed in [18], where unsymmetrical switching pattern is applied to dc side switches to avoid resonance. However, a five control variable were adopted to reduce the circulating current value at light load conditions making the control architecture complex.

This paper proposes an improved discontinuous current single phase shift modulation (IDCPSM) with a simpler unsymmetrical switching pattern. The objective is to minimize the circulating current, flowing through the switches and the HFT across the grid cycle of ac mains voltage and also at different loading conditions. This is achieved by modulating the duty of the dc side VFFB in every switching interval. The duty of ac side CFHB is modulated to maintain unity power factor (UPF). This dual control variable approach keeps the control architecture simple and easy to implement. ZCS turn-off for ac side switches and ZVS turn-on for dc side switches is maintained across the grid cycle. Reduced RMS current through ac and dc side switches as well as through the HFT is achieved contributing to lower conduction losses with significant improvement in the efficiency of the converter.

This paper is organized as follows. Section II provides a detailed description of the schematic of ICFHB ac-dc converter. Operational stages with the proposed IDCPSM are described and compared with the conventional SSM in Section III. Section IV shows the experimental results of the implemented IDCPSM on the developed laboratory prototype and the comparative performance evaluation among the different SSM. Lastly, Section V concludes this paper.

II. ICFHB AC-DC CONVERTER DESCRIPTION

The schematic of a single phase single stage galvanically isolated current-fed half bridge ac-dc converter is shown in Fig. 1. It consists of a current-fed half bridge converter with bidirectional switches on the ac side and a full bridge converter on the dc side, connected through a high frequency transformer (HFT). $L_1$ and $L_2$ are the two boost inductors. $L_{lk}$ is the leakage inductance of the HFT. An external series inductor $L_s$ is connected on the dc side to achieve the required total series inductance $L_t = L_{lk} + L_s/n^2$. $C_o$ is the output filter capacitor.

The ac side switches are annotated as $S_{xyg}$, where $x$ denotes leg number and $y = a$ or $b$. $S_{xyg}$ are switched at high frequency in the positive half cycle of grid voltage and remains continuously on in the negative half cycle. While $S_{xyb}$ are switched at high frequency in the negative half cycle of grid voltage and remains continuously on in the positive half cycle. The gate signals between ac side leg 1 and leg 2 are phase-shifted by 180°. $S_{xyg}$ is switched at a duty ratio $d_1$ always greater than 0.5, ensuring conduction overlap between the legs. Battery side switches are annotated as $S_p$, where $p = A, B, C$ or $D$. $S_A$ and $S_B$ are switched at a fixed duty of 0.5. $S_C$ and $S_D$ are switched at a duty ratio of $d_2$. $S_p$ turn-off is synchronised with the turn-off of $S_{xyg}$ in the following way. In the positive half cycle of the grid voltage, $S_{C,D}$ and $S_{A,B}$ turn off is synchronised with $S_{1ag}$ and $S_{2ag}$ respectively. In the negative half cycle, $S_{C,D}$ and $S_{A,B}$ turn off is synchronised with $S_{2bg}$ and $S_{1bg}$ respectively. During the turn-off duration of ac side switches, a resonance occurs between its output device capacitance and the total series inductance, $L_t$.

In order to suppress this parasitic ringing, HFT is designed to have very minimum leakage inductance $L_{lk}$. Diode clamps $D_{c1}$ and $D_{c2}$ are connected between the HFT terminals and external series inductor at dc side, thereby clamping the ac side switch voltage to $V_o/n$. These diode clamps incur lower losses than the damping resistor used in [13].

III. OPERATION STAGES WITH IDCPSM

To simplify analysis, it has been assumed that the converter is operating at unity power factor (UPF). Further, input ac mains voltage $v_g^{(k)}(t)$ is assumed constant in a switching interval $k$. Variable with superscript $k$ is changing every next switching interval and variable without the superscript $k$ is assumed constant throughout the converter operation.

\begin{align*}
  v_g^{(k)}(t) &= V_m \sin(\omega t) \\
  i_g^{(k)}(t) &= \frac{2P_o}{V_m} \sin(\omega t)
\end{align*}

AC side duty cycle is given by

\begin{equation}
  d_1^{(k)} = \frac{V_o - n|v_g^{(k)}(t)|}{V_o}
\end{equation}

where, $\tau = k * T_s$ and $T_s$ is the time period of a switching cycle, $\omega = 2\pi/t_g$, $t_g$ is the time period of a grid cycle, $P_o$
is the output power and $V_o$ is the output voltage. Fig. 2a and Fig. 2b shows the operating waveform of the converter at the peak and near the zero crossing in the positive half cycle of ac mains voltage respectively. Fig. 2c shows the ac side switch current and dc side switch current during this stage is given by (7) and (8) respectively.

$$i_{k}^{(k)}(t) = \begin{cases} 
\frac{1}{2}(i_g^{(k)} - \frac{v_{rs}^{(k)}}{L_1} T_s) + \frac{v_{rs}^{(k)}}{L_1} t - (k-1)T_s, & (k-1)T_s < t \leq (k-1 + d_1^{(k)})T_s \\
\frac{1}{2}(i_g^{(k)} + \frac{v_{rs}^{(k)}}{L_1} T_s) + \frac{v_{rs}^{(k)}}{L_1} [t - (k-1 + d_1^{(k)})T_s] - \frac{V_o}{nL_1} [t - (k-1 + d_1^{(k)})T_s], & (k-1 + d_1^{(k)})T_s < t < kT_s \\
\frac{1}{2}(i_g^{(k+1)} + \frac{v_{rs}^{(k+1)}}{L_1} d_1^{(k+1)}T_s), & t = kT_s
\end{cases}$$  

(4)

Stage 1 ($t_0$, $t_1$): Fig. 3a shows the equivalent circuit during this stage. At $t_0$, the HFT ac side winding current $i_{1k}^{(k)}(t)$ equals boost inductor current $i_{L2}^{(k)}(t)$. The current through $S_{2ag}$ body diode reaches zero and naturally turns off achieving ZCS. The output parasitic capacitance of $S_{2ag}$ charges to $V_o/n$, therefore $v_{pq}^{(k)} = -V_o/n$. $S_{1ag}$ is on in this stage. $S_C$ and $S_D$ are turned on at $t_0$ and their respective body diode current transfers to the channel of the devices thereby achieving ZVS. $S_A$ and $S_B$ are off during this stage and their respective device output capacitance are charged to $V_o$. The equation of $i_{1k}^{(k)}(t)$ during stage 1 is given by (5) and at $t_0$ is given by (6). The equation of ac side switch current and dc side switch current during this stage is given by (7) and (8) respectively.

$$i_{1k}^{(k)}(t) = \frac{V_o}{nL_1} (t - t_1) + i_{1k}^{(k)}(t_1)$$  

(9)

$$i_{1k}^{(k)}(t_1) = \frac{1}{2}(i_g^{(k)} - v_{rs}^{(k)}) d_1^{(k)} T_s$$  

(10)

$$i_{2ag}^{(k)}(t) = -i_{1k}^{(k)}(t)$$  

(11)

The duration of this stage is denoted as $\alpha^{(k)} T_s$ as shown in...
Fig. 3. Equivalent circuits of ICFHB ac–dc converter in a switching interval at various stages (a) Stage 1 \((t_0, t_1)\), (b) Stage 2 \((t_1, t_2)\), (c) Stage 3 \((t_2, t_3)\), (d) Stage 4 \((t_3, t_4)\), (e) Stage 5 \((t_4, t_5)\), (f) Stage 6 \((t_5, t_6)\).

From Fig. 2a it can be noted that the duration of this stage is the secondary side duty \(d_s^{(k)}T_s\) and is given by

\[
d_s^{(k)}T_s = \frac{nL_{\text{L}}|i_{\text{L}}^{(k)}(t_1)|}{V_o}\tag{12}
\]

Stage 3 \((t_2, t_3)\): At \(t_2\), HFT winding current \(i_{lk}\) reaches zero as the line inductor current \(i_{L2}\) gets completely transferred to switch \(S_{2ag}\). Since both \(S_{1ag}\) and \(S_{2ag}\) is on, \(v_{pq}^{(k)} = 0\). \(S_D\) is kept on and gate pulse to \(S_C\) is removed. Since \(v_{rs}^{(k)} = -V_o\) at \(t_2\), this voltage is kept across the winding of HFT for a short duration even after \(t_2\). This rises the HFT winding current to a minimum value which in turn discharges the output device capacitance of \(S_D\) and charges the \(S_C\) device capacitance of \(S_C\). The body diode of \(S_D\) gets forward biased and the HFT winding current is maintained at that minimum value as \(v_{rs}^{(k)} = 0\). This minimum current value is very small compared to the total load current and hence it is assumed to be zero. Fig. 3c shows the circuit condition during this stage.

Stage 4 \((t_3, t_4)\): Fig. 3d shows the equivalent circuit during this stage. \(S_{1ag}\) and \(S_{2ag}\) is kept on and \(v_{pq}^{(k)} = 0\). At \(t_3\), \(S_C\) is turned on and its output device capacitance discharges and at the same time output device capacitance of \(S_D\) charges to \(V_o\). Thus, \(v_{rs}^{(k)} = -V_o\) and is applied across the dc side winding of HFT, rising the current through it at a constant slope. The current through \(S_{1ag}\) falls at the same constant slope and through \(S_{2ag}\) rises at the same constant slope. This duration is kept sufficiently long enough for the current to go negative through \(S_{1ag}\) as shown in Fig. 2c. The negative current flowing through the loop of ac side switches and the HFT is the circulating current \(i_{\text{cir}}^{(k)}\) as shown in Fig. 3c. The equation of \(i_{\text{cir}}^{(k)}(t)\) during this stage is given by \[13\]. AC side leg 1 switch current and leg 2 switch current is as per \[14\] and \[15\] respectively. DC side switch current equation in stage 4 is same as in stage 1.

\[
i_{\text{LK}}^{(k)}(t) = \frac{V_o}{nL_{\text{L}}} (t - t_3)\tag{13}
\]

\[
i_{\text{SI}}^{(k)}(t) = \frac{v_{pq}^{(k)}}{L_{\text{L}}} (t - t_3) - i_{\text{LK}}^{(k)}(t)\tag{14}
\]

\[
i_{\text{SI}}^{(k)} (t) = i_{\text{L2}}^{(k)} (t) + i_{\text{LK}}^{(k)} (t)\tag{15}
\]

It is clear from \[16\] that the peak value of ac side HFT winding current \(i_{lk,pk}\) is dependent on \(d_s^{(k)}\). In the existing modulation scheme, the value of \(d_s^{(k)}\) was decided for the maximum output power and was kept constant irrespective of the operating conditions \[17\]. Thus, \(i_{lk,pk} = I_{\text{max}}\) remained constant across the entire grid cycle of ac mains voltage and in different load conditions. This can be observed from Fig. 2a that at the peak of ac mains voltage i.e at \(\omega t = 90^\circ\), the winding current reaches \(I_{\text{max}}\) during \(d_s^{(k)}T_s\). For this fixed value of \(d_s^{(k)}\), the peak current value remains constant near the zero crossing of ac mains voltage i.e at \(\omega t = 90^\circ\) as shown by dotted lines \((t_2' - t_3')\). From \[16\], Fig. 2c shows the current through the ac side and dc side switches near the zero crossing. It can be observed in the figure, as shown by dotted lines, that the peak current through the switches remains constant across the grid cycle. From \[17\] it is evident that for a fixed value of \(i_{lk,pk} = I_{\text{max}}\), the circulating current flowing through the converter is substantially high near the zero crossing of ac mains voltage. This high circulating current attributes to increased conduction losses in both ac and dc side switches and in the HFT.

\[
i_{\text{cir}}^{(k)} = i_{lk,pk} - \frac{1}{2} i_{\text{L2}}^{(k)}\tag{17}
\]

In the proposed IDCPSM, the ratio between \(i_{y}^{(k)}\) and \(i_{lk,pk}\) is kept fixed in the entire grid cycle of ac mains voltage i.e \(i_{lk,pk}\) follows the grid current sinusoidal envelope. This is achieved by varying \(d_s^{(k)}\) in every switching interval. This can be observed from Fig. 2a that near the zero crossing of ac mains voltage, \(d_s^{(k)}\), is adjusted as per the fixed ratio between \(i_{y}^{(k)}\) and \(i_{lk,pk}\). This substantially reduces the peak current value through the HFT winding as shown by bold lines. The merits of the proposed IDCPSM can also be seen in Fig. 2c. The peak current through the ac and dc side switches has also reduced.
Proposed IDCPSM

| Parameters | SPSM [14] | DCPSM [17] | Proposed IDCPSM |
|------------|-----------|-------------|-----------------|
| \(i_{ik, rms}^{(k)}\) | \(\frac{i_g^{(k)}}{2} \sqrt{\frac{5}{3}} \frac{4d_{ik}^{(k)}}{3} + \frac{i_{ik, pk}^{(k)}}{6} + \frac{2\beta^{(k)}}{3}\) | \(\frac{i_g^{(k)}}{2} \sqrt{\frac{1}{3}} \left(1 - d_{ik}^{(k)} + \frac{\alpha^{(k)}}{3} + \frac{\beta^{(k)}}{3}\right)\) | \(\frac{i_g^{(k)}}{2} \sqrt{\frac{1}{3}} \left(1 - d_{ik}^{(k)} + \frac{4d_{ik}^{(k)}}{3} + \frac{\alpha^{(k)}}{3} + \frac{7\beta^{(k)}}{3}\right)\) |
| \(I_{S_{ayg, rms}}^{(k)}\) | \(\frac{i_g^{(k)}}{2} \sqrt{\frac{5}{3}} \frac{4d_{ik}^{(k)}}{3} + \frac{i_{ik, pk}^{(k)}}{6} + \frac{\beta^{(k)}}{3}\) | \(\frac{i_g^{(k)}}{2} \sqrt{\frac{11}{3}} \left(1 - d_{ik}^{(k)} + \frac{10d_{ik}^{(k)}}{3} + \frac{4d_{ik}^{(k)}}{3} + \frac{7\alpha^{(k)}}{3} + \frac{5\beta^{(k)}}{3}\right)\) | \(\frac{i_g^{(k)}}{2} \sqrt{\frac{11}{3}} \left(1 - d_{ik}^{(k)} + \frac{10d_{ik}^{(k)}}{3} + \frac{4d_{ik}^{(k)}}{3} + \frac{7\alpha^{(k)}}{3} + \frac{17\beta^{(k)}}{3}\right)\) |
| \(I_{D_{ayg, avg}}^{(k)}\) | \(\frac{i_g^{(k)}}{2} \frac{\alpha^{(k)}}{2}\) | \(\frac{i_g^{(k)}}{2} \frac{\alpha^{(k)}}{2}\) | \(\frac{i_g^{(k)}}{2} \frac{\alpha^{(k)}}{2}\) |
| \(I_{S_{p, rms}}^{(k)}\) | \(\frac{i_g^{(k)}}{2n} \left(\frac{5}{6} \frac{2d_{ik}^{(k)}}{3} + \frac{i_{ik, pk}^{(k)}}{6} + \frac{\beta^{(k)}}{3}\right)\) | \(\frac{i_g^{(k)}}{2n} \left(\frac{1}{12} \frac{d_{ik}^{(k)}}{3} + \frac{i_{ik, pk}^{(k)}}{6} + \frac{\beta^{(k)}}{3}\right)\) | \(\frac{i_g^{(k)}}{2n} \left(\frac{1}{12} \frac{d_{ik}^{(k)}}{3} + \frac{i_{ik, pk}^{(k)}}{6} + \frac{\beta^{(k)}}{3}\right)\) |
| \(I_{D_{p, avg}}^{(k)}\) | 0 | 0 | 0 |

**TABLE I**

CURRENT Expressions

substantially as shown by bold lines near the zero crossing of ac mains voltage. As per \([17]\) the circulating current will also follow the sinusoidal envelope across the grid cycle. This reduced peak and circulating currents through the switches and the HFT contributes to lower conduction losses, significantly improving the efficiency of the converter.

**Stage 5** \((t_4, t_5)\): At \(t_4\), \(S_{1ag}\) is turned off and the negative current flowing through it shifts to its body diode. \(S_{2ag}\) continues to stay on from the previous stage therefore \(v_{pq} = 0\). \(S_C\) and \(S_D\) are turned off and its output parasitic capacitance charges to \(V_o\) and at the same time output parasitic capacitance of \(S_A\) and \(S_{yg}\) discharges and their body diode starts conducting. Thus, \(v_{rs} = V_o\) and applied across the dc side winding of HFT and current through it falls at a constant slope. The equation of \(i_{ik}^{(k)}(t)\) during this stage is given by \([18]\) at \(t_4\) is given by \([19]\). AC side switch current follows the same equation as per stage 4. DC side body diode current equation is given by \([20]\).

\[
i_{ik}^{(k)}(t) = \frac{V_o}{nL_t}(t - t_4) + i_{ik}^{(k)}(t_4) \quad (18)
\]

\[
i_{ik}^{(k)}(t_4) = \frac{V_o d_2^{(k)} T_S}{nL_t} = i_{ik, pk}^{(k)} \quad (19)
\]

\[
i_{D_{A}}^{(k)}(t) = i_{D_{A}}^{(k)}(t) = \frac{i_{ik}^{(k)}(t)}{n} \quad (20)
\]

As represented in Fig. 2a this duration is \(\beta T_s\) and is given by

\[
\beta^{(k)} T_s = \frac{nL_t (i_{ik}^{(k)}(t_5) - i_{ik}^{(k)}(t_4))}{V_o} \quad (21)
\]

**Stage 6** \((t_5, t_6)\): At \(t_5\), the current flowing through the body diode of \(S_{1ag}\) goes to zero, naturally turning off the device.

![Graphs showing variations](image-url)
and achieving ZCS. $S_{2a,g}$ continues to stay on therefore $i_{lk}^{(k)} = V_o / n$. $S_A$ and $S_B$ are turned on and the current through their body diode shifts to channel undergoing ZVS. $v_{rs}^{(k)} = V_o$. The equation of $i_{lk}^{(k)}(t)$ during this stage is given by (22) and at $t_5$ is given by (25). AC side leg 2 switch current equation in given by (24) and dc side switch current equation is given by (25).

Fig. 4a shows that the ac side HFT winding rms current near the zero crossing of ac mains voltage, attributing value of the winding current is 10.2 A. This higher circulating current near the zero crossing of ac mains voltage, attributing to higher conduction losses with considerable reduction can also be seen in rms current through ac and dc side switch $i_{lk}^{(k)}$, ac side HFT winding current $i_{S_{2a,g}}^{(k)}$, and dc side switch $i_{S_A}^{(k)}$. Fig. 4b shows the zoomed waveform at the peak and near the zero crossing of the ac mains voltage respectively. The peak value of the winding current is 10.2 A. This higher circulating current near the zero crossing of ac mains voltage, attributing to higher conduction losses and deteriorating efficiency.

Stage 1 to stage 5 describes the converter operation in a half switching interval. The other half is symmetrical to the above described stages as evident from stage 6.

Table I lists the expressions of rms current through ac side HFT winding $i_{lk, rms}$, rms current through ac side switch $i_{S_{2a,g}, rms}$, and dc side switch $i_{S_A, rms}$, average current through the body diode of ac side switch $i_{D_{S_{2a,g}}}$, and dc side switch $i_{D_{S_A}}$ in a switching interval $k$ and Fig. 4 shows their variation in a half grid cycle for SPSM, DCPSM and proposed IDCPSM. Fig. 4c shows that the ac side HFT winding rms current is maximum in switching intervals near the zero crossing of ac mains voltage for SPSM and is substantially low for DCPSM. In the proposed IDCPSM, this value is further reduced as the peak current through the windings of HFT is significantly reduced by modulating $d_{lk}^{(k)}$ across the grid cycle. Reduction can also be seen in rms current through ac and dc side switches for the proposed IDCPSM as depicted in Fig. 4d. This amounts to lower conduction losses with considerable improvement in the efficiency of the converter.

IV. EXPERIMENTAL RESULTS

A 1.5 kW laboratory prototype was developed and is shown in Fig. 5. The performance of the converter with proposed modulation scheme is validated at different loading conditions. Table II lists the parameters of the implemented prototype. The control scheme is implemented in a TI TMS320F28397D launchpad and the combinational logic of gate pulses is generated using Xilinx XC6SLX4 based FPGA board.

A. Experimental Waveform

Fig. 6a shows the measured ac grid voltage $v_g$ along with the input grid current $i_g$, ac side HFT winding current $i_{lk}$ and output voltage $V_o$ for DCPSM [17]. It can be observed that the peak value of the winding current is constant in the entire grid cycle of ac mains voltage. This is further depicted in Fig. 6b and 6c showing the zoomed waveform at the peak and near the zero crossing of the ac mains voltage respectively. The peak value of the winding current is 10.2 A. This higher circulating current near the zero crossing of ac mains voltage, attributing to higher conduction losses and deteriorating efficiency.

Table II

| Parameter                          | Value                  |
|------------------------------------|------------------------|
| AC mains voltage $V_g$             | 230 V rms              |
| AC mains frequency $f_g$           | 50 Hz                  |
| Output Voltage $v_o$               | 300 V ... 400 V        |
| Output Power $P_o$                 | 1.5 kW                 |
| Switching Frequency $f_{sw}$       | 100 kHz                |
| Transformer ratio                  | 0.38                   |
| Transformer Prim                    | 26 turns, 135 wires, #40 SWG |
| Transformer Sec                     | 10 turns, 260 wires, #40 SWG |
| Transformer Core                    | Ferrite EE80/20 (2 stacked) |
| $L_{ih}$                            | 600 nH                 |
| Boost Inductor $L_1$, $L_2$        | 82 turns, 135 wires, #40 SWG |
|                                    | Core: Kool Mµ 77620    |
| Series Inductor $L_s$               | 10 turns, 260 wires, #40 SWG |
|                                    | Core: Kool Mµ 77071    |
| Output Capacitor $C_o$              | 940 µF                 |
|                                    | 4 parallel leg         |
|                                    | Each leg: 2 series connected 470 µF (Electrolytic 400 V) |
| AC side SiC Mosfets $S_{xyg}$      | Cree C2M0080170P       |
| DC side SiC Mosfets $S_p$           | UnitedSiC UF3C065030K4S |

Fig. 7a shows the measured ac grid voltage $v_g$, grid current $i_{g}$, ac side HFT winding current $i_{lk}$ and output voltage $V_o$ for proposed IDCPSM. It is clear from the figure that converter is operating at 0.999 power factor. The total series inductor current now has a sinusoidal envelope with twice the ac mains voltage frequency. Its peak current value has reduced by almost 55% from the peak Fig. 7b to near the zero crossing Fig. 7c of the ac mains voltage.

Fig. 8 shows the zoomed waveform of gate source voltage...
Fig. 6. Measured grid voltage $v_g$, grid current $i_g$, output voltage $V_o$ and ac side HFT winding current $i_{lk}$ for DCPSM in (a) grid cycle, (b) zoomed near zero crossing of ac mains voltage. ($P_o = 1.5 \text{ kW}, v_g = 230 \text{ V}_{\text{rms}}$ and $V_o = 345 \text{ V}$)

Fig. 7. Measured grid voltage $v_g$, grid current $i_g$, output voltage $V_o$ and ac side HFT winding current $i_{lk}$ for IDCPSM in (a) grid cycle, (b) zoomed near peak of ac mains voltage, (c) zoomed near zero crossing of ac mains voltage. ($P_o = 1.5 \text{ kW}, v_g = 230 \text{ V}_{\text{rms}}$ and $V_o = 345 \text{ V}$)

Fig. 8. Zoomed-in measured gate source voltage $v_{gs-S_{1ag}}$, drain source voltage $v_{ds-S_{1ag}}$ and the ac side HFT voltage $V_{pq}$

$v_{gs-S_{1ag}}$ and drain source voltage $v_{ds-S_{1ag}}$ of ac side switch $S_{1ag}$, along with the ac side HFT voltage $V_{pq}$. It can be observed that (dotted region) even though the gate voltage is at $-5\text{V}$, the switch voltage is zero, indicating that its body diode is conducting as discussed in section II. The switch naturally turns-off as the current through its body diode goes to zero achieving ZCS.

**B. Efficiency**

Fig. 9 shows the efficiency curve for different SSM at nominal output voltage $V_o = 345\text{V}$. Power analyser module of Tektronix MDO3104 DSO is used for measuring power. From the figure it can be concluded that the proposed IDCPSM has the best performance with peak efficiency of 94.4%. Furthermore, the efficiency curve for IDCPSM remains nearly flat across different loading conditions. An improvement of around 3% is seen at lighter loading condition $P_o = 1 \text{ kW}$ and 1.5% at full load $P_o = 1.5 \text{ kW}$ from DCPSM. This improvement in performance is due to active control of the peak circulating across the grid cycle of the ac mains voltage and at different loading conditions. The SPSM is the least efficient among the three SSM. Fig. 10 shows the loss distributions among the components. The sum of switching and conduction loss is depicted as ac or dc side switch loss. HFT loss shows the total loss occurred in the HFT and the series inductor. The reduction in peak value of circulating current with the proposed IDCPSM reduces the conduction losses in ac side switch as depicted in the Fig. 10. The total loss in the dc side switch is reduced by almost 42% from DCPSM. This is because both switching and conduction loss are reduced in the dc side switch. Furthermore, the total loss in the HFT is reduced by almost 20% with the proposed IDCPSM as both core loss and copper loss reduces in the HFT and the series...
inductor.

![Graph showing Power Loss distribution among the components of L-L type ICFHB ac-dc inductor.](image)

**Fig. 10.** Loss distribution among the components of L-L type ICFHB ac-dc inductor.

V. CONCLUSION

This paper proposed a IDCPSM for an L-L type ICFHB ac-dc converter. A dual control variable approach has been developed where in ac side CFHB duty is modulated to maintain UPF and dc side VFFB duty is modulated to reduce the peak circulating current in a grid cycle of ac mains voltage and also at light load conditions. ZCS turn-off of ac side switches and ZVS turn-on of dc side switches are maintained throughout the operating condition. This has significantly reduced the conduction and switching losses in both ac and dc side switches. A comparative performance analysis with different SSM reported in literature is also presented. The proposed IDCPSM provides the best performance with peak efficiency of 94.4% and almost a flat efficiency profile across different loading conditions.

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