1. Introduction

Printed and solution-processed polymer field-effect transistors (FETs) are considered among key enablers of flexible, wearable, and portable electronics, and they hold the promise of low-cost access to many novel mass applications. This promise stemmed from the prospect of utilizing printing tools derived from well-established graphical arts technologies to deposit a variety of functional materials, which exhibit a suitable combination of mechanical and electronic properties. Such vision has begun to show concrete potential through a variety of proof-of-concept demonstrations, among which are programmable logic circuitry for flexible displays, transferrable electronics for pharmaceutics, healthcare sensors for brainwave detection, or pulse oximetry, fully printed washable electronics on fabrics, and imperceptible logic circuitry on ultrathin substrates for intelligent electronic skin.

Nonetheless, several among the most desirable applications, such as radio-frequency (RF) tags and smart labels, driving circuitry for large-area high-resolution flexible displays, and real-time sensor arrays, along with wireless sensors and sensors networks, require high-speed and low-voltage operation of the basic components of the circuits, in particular the transistor. Given the limited carrier mobility and the coarse resolution of printing tools, printed organic electronics has struggled to deliver the challenging performances required to enable wireless capabilities. Alternative flexible electronics technologies with higher carrier mobilities are being developed to achieve high-frequency circuits, such as metal-oxide semiconductors, carbon nanotubes, and 2D materials, reaching in some cases very high “transition frequency” $f_t$, the highest operational frequency of a transistor, in the order of the GHz or tens of GHz. However, such high performances are either achieved by resorting to conventional micro and nanofabrication techniques (i.e., e-beam lithography, chemical vapor deposition, sputtering, and thermal evaporation), or pose scaling and processing issues (placing of high-quality monolayers of 2D materials, alignment of carbon nanotubes, and process temperatures compatible with cheap plastic substrates for high-quality metal-oxide layers).

It is therefore highly desirable to further develop printed and flexible organic electronics in order to achieve high-frequency operation. While the possibility to obtain GHz organic transistors has only recently become argument of discussion, progresses are being made in the range of near-field wireless communication. Several research groups in fact have proven the feasibility of operating organic transistors at frequencies in excess of 10 MHz, but only a few works have achieved such frequencies by adopting printing techniques, which are more easily upscaleable and compatible with large-area processing. The maximum frequency drastically decreases for organic transistors on flexible substrates. Moreover, since $f_t$ is proportional to the bias voltage, the requirement of low-voltage operation, at least below 10 V as necessary for portable, self-powered wireless electronics, further complicates the achievement of high operational frequency. Examples of $f_t$ beyond the MHZ threshold have been shown through the adoption of conventional thermally grown silicon dioxide dielectrics (20 MHz at a bias voltage of 10 V), alumina deposited via atomic layer deposition (19 MHz at 10 V), or hybrid metal-oxide/self-assembled ultrathin dielectrics.
(3.7 MHz at a bias of 3 V\cite{38} and 1.5 MHz at 4 V\cite{39}). There are instead scarce examples of fast devices where low-voltage is achieved through solution-processing. In this respect, ionic gating schemes through electrolyte dielectrics,\cite{40,41} which allow to achieve 1 V, or even lower, operational voltages, are not suitable because of their slow switching speed, in the tens of kHz range for the best reported cases.\cite{42,43} because of the slow movement of ions. Polymer dielectrics, in particular if based on low-k materials, are a suitable choice to attain ideal high-frequency operation of FETs, but the achievement of the high capacitance necessary for low-voltage operation is challenging. Demonstrations of MHz operation in FETs integrating low-k polymers are rare,\cite{16} and high $f_t$ values at a voltage below 10 V of transistors of this kind on flexible substrate are yet to be shown.

In this work, we demonstrate that fully solution-processed, low-voltage polymer FETs, operating at MHz range, can be realized on flexible substrates with a combination of printing and direct-writing techniques. In particular, $f_t$ in excess of 1 MHz can be reached at an extremely low bias voltage of 2 V, a voltage comparable to electrolyte-gated devices. 14 MHz operation can be attained already at 7 V, therefore enabling near-field wireless communication, which we exemplify here with a voltage rectifier, one of the most relevant building blocks for 13.56 MHz RF tags. The combination of these performances, obtained through scalable processes on cheap flexible substrates, represents a step forward in the realization of mass-produced, distributed electronics with RF communication functionalities.

2. Results

To realize low-voltage, high-frequency polymer FETs we adopted a combination of femtosecond-laser sintering of high-resolution metal electrodes on plastic, a fast coating of uniaxially aligned polymer semiconductor, and a solution-processed high capacitance dielectric stack. We have previously adopted femtosecond-laser sintering for the realization of high-resolution electrodes and high-frequency polymer transistors on glass.\cite{37} The same technique was also previously demonstrated to be compatible with plastic substrates for the fabrication of electrodes,\cite{44,45} semi-transparent grids,\cite{46} and transistors,\cite{47–49} while it has not yet been adopted yet for high-frequency, printed electronics on plastic. Here we show that femtosecond-laser sintering, thanks to highly controlled deposition of energy, allows the conversion of silver inks on plastic and the high spatial resolution patterning of electrodes suitable for high-performance fully solution-processed polymer transistors. Our simple two-step fabrication process is sketched in Figure 1a: we first deposit via spin-coating a uniform thin film of an ink of silver nanoparticles, then a near-infrared femtosecond-pulsed laser beam ($\lambda = 1030$ nm, 67 MHz repetition rate) induces the local sintering of the nanoparticles, directly writing conductive patterns. Finally, the unprocessed areas are washed out with an organic solvent. In future implementations aiming at reducing the amount of waste materials, spin-coating may be replaced with a suitable printing technique (e.g., bar-coating or inkjet) and the washed material can be recollected and recycled.

This approach allows to reach a maximum resolution of 1.5 $\mu$m for the patterning of conductive features at a scanning speed of 1 mm s$^{-1}$ (current limit of our setup), with an impinging laser beam intensity of 1.9 mW $\mu$m$^{-2}$. With this method, we patterned silver source and drain electrodes with a width $L_{ov}$ of 1.7 $\mu$m on polyethylene naphthalate (PEN) to be used in FETs with a bottom-contact, top-gate architecture (Figure 1b). We realized an interdigitated structure in which the central finger is used as the source electrode, while the two

\[ \text{Figure 1. a) Laser sintering processing steps for the fabrication of conductive electrodes on plastic; b) optical micrograph of a single device comprising active area and contact pads (magnification: layout of the source and drain electrodes); c) picture of the final realized devices on plastic PEN substrate.} \]
external fingers are used as the drain. A photograph of the realized devices on a flexible PEN substrate is shown in Figure 1c.

To proceed with the fabrication of organic field-effect transistors (OFETs), we followed the process illustrated in Figure 2a. We first modified the sintered Ag electrodes with a self-assembled monolayer of dimethylamino(benzenethiol) (DABT), which has been shown to improve electrons injection in organic semiconductors.[50] Then, we adopted the widely studied semiconducting good electron transporting co-polymer poly[N,Nʹ-bis(2-octyldodecyl)-Naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5ʹ-(2,2ʹ-bithiophene) (P(NDI2OD-T2)) and deposited a thin layer of such material via bar-coating, which is a simple and fast method to induce the directional alignment of the polymer chains along the coating direction,[51] yielding a film with optimized charge mobility over large area.[54] We then deposited via spin-coating a 150 nm thick multilayered polymer dielectric stack, composed of an ultrathin crossed-linked low-k polymer and a top high-k polymer, achieving an areal capacitance $C_{\text{areal}}$ of 39 nF cm$^{-2}$. We finally inkjet-printed poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) gate electrodes on top of the dielectric. We fabricated FETs (Figure 2b) with a varying channel length $L$, ranging from 1 to 17.5 µm, with constant channel width $W$ of 800 µm.

The transfer curve for an FET with the shortest channel length of 1 µm (Figure 2c) highlights the correct operation and turn-on of the device at a gate voltage as low as 5 V, both in the linear ($V_d = 1$ V) and in the saturation ($V_d = 5$ V) regime, with no appreciable hysteresis. In addition, we highlight the extremely low gate leakage current that is more than four orders of magnitude lower than the device ON current in both operation regimes. Similarly, analogous electrical performance and low gate leakage current are achieved in the devices with longer channel length (Figure S1a–c, Supporting Information). The drain current scales correctly with the channel length (Figure 2e and Figure S2a–c, Supporting Information), while the output curve, although not achieving clear saturation differentely from the longer channel devices (Figure S3a–c, Supporting Information) and likely owing to the onset of short-channel effects,[52] both confirms the correct operation of our downscaled device and suggests that a good charge injection performance is achieved in our architecture (Figure 2d).

We calculated the apparent electron mobility ($\mu_{\text{app}}$) for our devices as a function of gate voltage from the derivative of the transfer curves according to the gradual channel approximation model. In the device with $L = 1$ µm (Figure 2f), $\mu_{\text{app}}$ peaks at a low $V_g$ of 1.8 V (2.2 V) in the linear (saturation) regime, and then slightly rolls off with $V_g$, an effect related to the influence of charge injection limitations. For our case, we simply report in Table 1 the calculated value for the mobility in the saturation regime at maximum $V_g$, being one of the relevant bias

![Figure 2. a) Process flow for the fabrication of polymer FETs on plastic with solution-based techniques; b) 3D view of the final device stack; c) transfer curve and d) output curve for a realized FET with $L = 1$ µm; e) drain current at $V_g = 5$ V for the FETs and for the realized channel lengths; and f) calculated apparent charge mobility for the device with $L = 1$ µm.](image-url)
Table 1. Measured effective charge mobility and corresponding reliability factor for the realized FETs for the different channel lengths.

| Channel length [µm] | Apparent mobility at $V_g = 5$ V [cm² V⁻¹ s⁻¹] | Reliability factor $r$ [%] |
|---------------------|-----------------------------------------------|--------------------------|
| 1                   | 0.30                                          | 107                      |
| 1.5                 | 0.29                                          | 109                      |
| 5.5                 | 0.16                                          | 128                      |
| 17.5                | 0.14                                          | 134                      |

points for the FET and for the rectifier circuit presented later in the text. At this bias point, $\mu_{pp}$ ranges in the interval from 0.15 to 0.3 cm² V⁻¹ s⁻¹ when $L$ is shortened from 17.5 to 1 µm. Such an increasing trend as the channel length is reduced is an effect stemming from the increase of the lateral electric field across the channel region, which affects charge injection and/or charge transport in organic FETs.[53–55] In Table 1, alongside with the calculated mobility, we report the “measurement reliability factor” $r$ as suggested in Choi et al.[56] which in our cases is always above 100%, highlighting the presence of a very mild “kink effect.”

We extracted the contact resistance of the shortest channel device ($L = 1$ µm) with the differential method,[57] which yielded a width-normalized contact resistance $R_C W = 1015$ Ωcm at $V_g = 5$ V in the linear regime. The latter is a very small value in the context of printed polymer FETs, has rarely been achieved with the sole use of solution-based approaches and with low-voltage operation,[58,59] and has a paramount role in the achievement of good electrical behavior of our downscaled FETs. In particular, $R_C W$ is below the value of the width-normalized channel resistance $R_{ch} W = V_g W / I_d = R_C W = 1369$ Ωcm at the highest gate bias of $V_g = 5$ V (and $V_d = 1$ V). Despite $R_C W$ values below 1000 Ωcm have been demonstrated for organic transistors,[60–66] these examples either adopted evaporation of dopants/electrodes, or device biasing in excess of 10 V, or the use of electrolyte-gating schemes, which are not desirable for high-frequency, low-voltage, all-solution-processed devices.

We show in Figure S4a,b (Supporting Information) the superimposed transfer curves of five different devices each for $L = 1$ µm and $L = 1.5$ µm cases, and in Figure S5 (Supporting Information) we plot the superimposed trends of the extracted mobility versus gate voltage for the devices with the shortest channel ($L = 1$ µm), highlighting that our results are reproducible even at these challengingly short, micrometer-sized channel lengths. In Table S1 (Supporting Information) we plot the superimposed trends of the extracted mobility versus gate voltage for the devices with the shortest channel ($L = 1$ µm), highlighting that our results are reproducible even at these challengingly short, micrometer-sized channel lengths. In Table S1 (Supporting Information) we report the “measurement reliability factor” $r$ as suggested in Choi et al.[56] which in our cases is always above 100%, highlighting the presence of a very mild “kink effect.”

We also measured the transfer curve of a device ($L = 1$ µm) after 7 months from fabrication and storage in nitrogen atmosphere, highlighting how only a small loss in performance is detected (Figure S6b, Supporting Information), detecting a good stability of the device upon operational stress.

In order to evidence the benefit of downscaled features on the frequency response of the fabricated FETs, we characterized the AC performance of our devices in terms of transition frequency $f_t$, which depends on the electrical parameters of the transistor according to[60]

$$f_t = \frac{g_m}{2 \pi (C_{gs} + C_{gd})}$$

(1)

where $g_m$ is the device transconductance and $C_{gs}$, $C_{gd}$ are the gate/source and gate/drain capacitances, respectively. Additional details on the measurement method can be found in ref. [37]. In Figure 3a we show the measured $C_{gs}$ and $C_{gd}$ versus bias voltage in the saturation regime ($V_{gs} = V_{ds}$ and compared them to the theoretically expected values for our layout, according to[67]

$$C_{gs} = C_{del} \left( \frac{W}{2} \frac{L + W_{ov} L_m}{L_m} \left( 1 + \alpha_{g,s} \right) \right)$$

(2)

$$C_{gd} = 2 C_{del} W_{ov} L_m \left( 1 + \alpha_{g,d} \right)$$

(3)

where $W_{ov} = 500$ µm is the total width of the overlap between gate and bottom electrodes, which exceeds the actual channel width $W$ (see the scheme reported in Figure S7, Supporting Information), while the correction factors $\alpha_{g,s}$ and $\alpha_{g,d}$ are introduced to account for the fringing capacitance between the source/drain electrodes and the wide top gate. We calculated such factors using a formula proposed by Elmasry,[68] yielding $\alpha_{g,s} = 12.4\%$ and $\alpha_{g,d} = 21.1\%$, which is in perfect agreement with our measured data. In the case of $C_{gd}$, the measured values are correctly constant at ≈0.8 pF up to a bias voltage of 5 V, while $C_{gs}$ exhibits a slightly increasing trend with the bias voltage, which we attribute to parasitic accumulation of additional charge outside the channel active area. This effect has already been explained for structures of this kind,[69] and originates from the fact that the semiconductor layer is not patterned, covering the whole substrate. At bias voltages $>5$ V, the higher electric fields are producing a further increase in capacitance and a relatively small deviation from the predicted values.

The measured $g_m$ per unit width versus bias voltage is shown in Figure 3b. We correctly identify a linear increase of $g_m$ from $V_{gs} = 1$ V to $V_{gs} = 5$ V, where the transconductance varies from 0.081 to 0.58 mS cm⁻¹. The latter value is very close to the theoretical one extracted from the slope of the transfer curves, which yields $g_m = \frac{e L_m}{W_m^2} (V_{gs} - V_T) + 0.51 \frac{m A}{V_m}$. For bias voltages in excess of 5 V, $g_m$ exhibits a superlinear increase with $V_{gs}$, an effect that we attribute to the high lateral electric field insulating across the channel region. The measurements for $g_m$, $C_{gs}$, and $C_{gd}$ can be combined to identify $f_t$ as in Figure 3c, where we show such measurement for a device with $L = 1$ µm and a bias voltage of 7 V (top panel) and 2 V (bottom panel). The measurement is limited at a frequency of 2 MHz due to setup constraints. Remarkably, we can measure an $f_t = 1.6$ MHz for a bias voltage of only 2 V. In Figure 3d we show the trend of the measured $f_t$ for the same device versus bias voltage, highlighting how this
figure of merit essentially follows the behavior of $g_m$. In the case of a bias voltage of 7 V, we can extrapolate a high transition frequency of 10.4 MHz.

To assess the relevance of the performance achieved by our devices and also to favor the identification of effective strategies to improve even further $f_t$, we have calculated the maximum achievable transition frequency with respect to the variation of our FET parameters, using the modeling recently proposed by Klauk.\cite{30} With an $R_C W$ of a value equal to the one we measured, neither a further reduction of $L$ nor an increase of $\mu_0$ would yield a very significant increase in $f_t$ (Figure S8a, Supporting Information). At such fixed contact resistance, an increase in $f_t$ would only be obtainable with the reduction of $L_{ov}$. However, even in the extreme and unrealistic case of $L_{ov} = 0$, $f_t$ would be limited to a value below 100 MHz at best (Figure S8b, Supporting Information). These calculations underline that we have already obtained, with the physical parameters characterizing our devices, an AC performance that is close to the highest possible. The reduction of the contact resistance thus constitutes the main route for accessing higher $f_t$ in the future, as it is the key point in order to achieve a regime where the modification of the other parameters is effective (Figure S8c, Supporting Information).

We have also measured the reproducibility of our devices in terms of transition frequency after 7 months from fabrication. In Figure S9 (Supporting Information) we show the measured curves for four devices with $L = 1 \mu$m at a bias voltage of 5 V, which highlight good reproducibility for $f_t$ with a mean value of 6.65 MHz and a standard deviation of 2.12 MHz. Overall, our best $f_t$ in the measurement set yielded a value of 14.4 MHz at a bias voltage of 7 V (Figure S10, Supporting Information).

We have also compared our achieved performance to the previous literature for organic high-frequency transistors on plastic, for which the transition frequency was explicitly measured and reported. Since $f_t$ is directly proportional to the applied bias voltage, in our comparison we decouple such effect by defining the voltage-normalized transition frequency $f_t/V_{bias}$, where $V_{bias}$ is the maximum voltage applied to the transistor electrodes during $f_t$ measurement. In this way the voltage-normalized transition frequency encompasses the achieved performance exclusively in terms of effective charge transport properties and geometrical resolution. We report in Table 2 the calculated $f_t/V_{bias}$ of our FETs in comparison with other representative examples of high-frequency ($f_t > 1$ MHz) organic devices on flexible substrate.

Our FETs achieve the best performance in terms of $f_t/V_{bias}$ in the field of organic transistors on plastic, with a tenfold improvement compared to previous demonstrations.

While $f_t$ is the relevant figure of merit for the assessment of the FET maximum operational speed for integration in analog circuitry (e.g., amplifiers), we additionally assessed the performance of our FETs upon large-signal operation, which is relevant for the implementation of RF applications such as wireless data communication. To this goal, we realized a...
simple rectifying circuit (Figure 4b, inset) and operated it up to 15 MHz, above the frequencies of interest for near-field communication (NFC). In Figure 4a we show the rectified output (red line) on an oscilloscope corresponding to an oscillating input signal with an amplitude of 8 V (black line). We measure a $-3 \, \text{dB}$ frequency of 8.7 MHz, with respect to the amplitude recorded at 100 kHz (Figure S11, Supporting Information). For a reduced signal amplitude of 5 V, the $-3 \, \text{dB}$ frequency is as high as 6.4 MHz already (Figure 4b), and 1 V can still be read in DC at 15 MHz (Figure S12, Supporting Information) proving the applicability of our approach for the implementation of RF tags.

We also verified the stability of the output of our rectifier upon constant operation for 150 min at an input voltage amplitude of 5 V and at an input frequency of 15 MHz (Figure S13, Supporting Information). The device was measured after 7 months from fabrication. Our rectifier shows stable performance over 2.5 h of continuous operation even at the high operational frequency of 15 MHz.

To better understand the measured performance of our rectifier we developed a simple model, based on the charge balance of the smoothing capacitor (see Figure 4b, inset), for the behavior of the output voltage versus input voltage frequency (see the Supporting Information). We are able to predict with good approximation the frequency behavior of the output voltage (Figure 4b, solid line), correctly identifying the frequency cutoff. Moreover, the model allows us to identify the main factors determining the output/input voltage ratio without affecting the rectifier cutoff frequency: in order to achieve a high ratio, it is critical to limit the OFF current in the transistor and to adopt a channel width large enough to feed the load resistance. The cutoff frequency is instead determined by the same parameters as the $f_t$ (i.e., $L$, $\mu$, and $V_{\text{bias}}$) and can be set independently.

3. Conclusions

We have demonstrated the realization of high-frequency, low-voltage polymer FETs on flexible substrates using only printing techniques and digital laser patterning. The proposed FETs feature a transition frequency in excess of 1 MHz at a bias voltage as low as 2 V, and can operate at a frequency in excess of 10 MHz at a bias voltage of 7 V, which is, to the best of our knowledge, the highest for the case of printed polymers integrating direct-written electrodes, on flexible substrates. Such performance allows the reported devices to operate at supply voltages comparable to electrolyte gated organic transistors, while they can be modulated at two to three orders of magnitude higher frequencies. Moreover, such operational bias voltage enables the implementation of stand-alone electronic devices, being fully compatible with thin film batteries or energy harvesters, such as plastic photovoltaic modules. In addition, these devices achieve the best figure to date, by an order of magnitude, in terms of voltage-normalized transition frequency (2.06 MHz V$^{-1}$). Finally, we have integrated these devices into a rectifying circuit that can provide voltage rectification up to 15 MHz, thus being compatible with NFC wireless communication at 13.56 MHz. The demonstration of such performance and its achievement with the sole use of solution-based processing, printing techniques, and laser patterning identify a feasible route toward low-cost, mass-scale production of organic devices for RF applications.

| $f_t$ [MHz] | $V_{\text{bias}}$ [V] | $f_t/V_{\text{bias}}$ (MHz V$^{-1}$) | Fabrication techniques | Ref. |
|------------|----------------|-----------------------------|-------------------------|-----|
| 14.4       | 7              | 2.06                        | Laser sintering, bar-coating, spin-coating, inkjet | This work |
| 1.6        | 2              | 0.80                        | Laser sintering, bar-coating, spin-coating, inkjet | This work |
| 1.6        | 8              | 0.20                        | Inkjet, spin-coating     | [16]|
| 4.9        | 30             | 0.16                        | Laser ablation, spin-coating, inkjet | [18]|
| 1.92       | 15             | 0.13                        | Gravure, inkjet          | [15]|
| 3.3        | 30             | 0.11                        | NIL, evaporation, inkjet, gravure | [17]|

NIL: Nanoimprint lithography.

Figure 4. a) Input and output voltage waveforms for a rectifier based on a realized FET with $L = 1$ $\mu$m at an input voltage frequency of 100 kHz (top panel) and of 10 MHz (bottom panel). b) Measured and simulated output voltage of the same rectifier versus frequency at an input voltage amplitude of 5 V (inset: rectifier circuit).
4. Experimental Section

General: The Ag-nanoparticles ink (NPS-JL) was purchased from Harima Chemicals, 4-(dimethylamino)benzenethiol (DABT) was purchased from TCI Chemicals, P(NDI2OD-T2) was purchased from Polyera (Mw = 35.3 kDa; PDI = 1.8 (GPC); elemental analysis: C: 75.21, H: 8.73, N: 2.87 (theoretical: C: 75.26, H: 8.96, N: 2.83)), and PEDOT:PSS (Clevios PJ700) was purchased from Heraeus. The substrates consisted of 125 µm thick polyethylene naphthalate foils (Teonex Q65FA) of 125 µm thick polyethylene naphthalate foils (Teonex Q65FA) purchased from DuPont TeijinFilms.

Femtosecond Laser Sintering Setup: The laser setup consisted of a commercial laser source (LightConversion PHAROS, based on Yb:KGW as active medium), which generated ∼80 fs long laser pulses with a repetition rate of 67 MHz, λ = 1030 nm, and a maximum output power of 2 W. Before reaching the sample, the beam was conditioned through an optical path that includes a software-controlled attenuator and a focalizing objective (Mitutoyo) lens whose magnifying power could be selected between 20X, 50X, and 100X. The sample was positioned on a software-controlled moving stage (Aerotech ALB1000) capable of a maximum resolution of 0.5 nm and a maximum speed of 300 mm s⁻¹.

Organic FET Fabrication: The samples with the desired laser-sintered patterns for the FET bottom electrodes were Ar-plasma etched with a power of 100 W for 4 min. A solution of 17°L of DABT in 12 mL of isopropanol was prepared, and the samples were immersed in it for the linear regime.

Contacts Fabrication: The PEN substrates were used as-is on the pristine side (without adhesion-promoting treatment) and a 4 nm thick AlOx layer was deposited via thermal evaporation of Al and exposure to atmosphere. The Ag-nanoparticles ink was spun at 7000 rpm for 5 min, yielding a 70 nm thick layer. The laser-sintering step was then performed using 1.9 mW µm⁻² beam power, 50X optics, and 0.1 mm s⁻¹ scanning speed. After laser processing, the samples were thoroughly washed with o-Xylene and isopropanol and finally dried with a nitrogen flux.

Organic FET Fabrication: The samples with the desired laser-sintered patterns for the FET bottom electrodes were Ar-plasma etched with a power of 100 W for 4 min. A solution of 17°L of DAET in 12 mL of isopropanol was prepared, and the samples were immersed in it for 15 min and then rinsed with abundant isopropanol. A solution of P(NDI2OD-T2) in toluene (5 g L⁻¹) was then deposited via bar-coating on the samples as described in ref. [14] using a bar designed to yield an 8 µm thick wet layer. The samples were then annealed in a nitrogen atmosphere for 20 min at 120 °C. The dielectric was a double layer stack composed of a very thin layer of a low-k polymer, for a total thickness of about 200 nm and an areal capacitance of 39 nF cm⁻². Finally, PEDOT:PSS was inkjet-printed with a Fujifilm Dimatix DMP-2831 to pattern the gate electrodes and the samples were annealed for 8 h in nitrogen atmosphere before measurement.

Rectifier Fabrication: The rectifier circuit was realized by connecting one of the realized transistors, biased in a transdiode configuration, to a discrete capacitor of 0.15 µF and to an oscilloscope with an input resistance of 1 MΩ using external point-contact probes.

Electrical Characterization: The devices were measured in nitrogen atmosphere. Static characterization was performed via a Keysight B1500A Semiconductor Parameter Analyzer. Frequency performance was measured using a custom setup that includes a Keysight ENA E5061B Vector Network Analyzer and an Agilent B2912A Sourcec o m e r t. The apparent mobility \( \mu_{\text{app}} \) was extracted from the transfer characteristic according to \( \mu_{\text{app}} = \frac{V}{I_D} \frac{W}{L} \) for the saturation regime and according to \( \mu_{\text{app}} = \frac{I_D}{V} \frac{W}{L} \) for the linear regime.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

flexible organic transistors, laser sintering, printed electronics, radio frequency, rectifiers

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