Multi-island single-electron devices from self-assembled colloidal nanocrystal chains

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We report the fabrication of multi-island single-electron devices made by lithographic contacting of self-assembled alkanethiol-coated gold nanocrystals. The advantages of this method, which bridges the dimensional gap between lithographic and NC sizes, are (1) that all tunnel junctions are defined by self-assembly rather than lithography and (2) that the ratio of gate capacitance to total capacitance is high. The rich electronic behavior of a double-island device, measured at 4.2 K, is predicted in detail by combining finite element and Monte Carlo simulations with the standard theory of Coulomb blockade with very few adjustable parameters.

The confinement of electrons to small metallic islands leads to the quantization of charge because of the energy barrier associated with adding an extra electron to a small capacitance.\textsuperscript{1} As a result, when multiple islands are connected in series, electrons pass through them one at a time, making it possible to create current standards, potentially useful for metrology.\textsuperscript{2-4} Although they are usually made by lithography, single-electron transistors (SETs), consisting of individual islands between metallic leads, have also been produced using colloidal nanocrystals (NCs). In principle, the latter could have much smaller capacitances than lithographic islands, resulting in larger Coulomb charging energies, larger operating voltages, higher operating temperatures and more accurate current standards. However, the fabrication of devices with NC islands has been limited to the fortuitous trapping of single or multiple NCs between pre-fabricated electrode gaps.\textsuperscript{5-7} In addition, the capacitances between the lithographically-defined electrodes and the NCs are relatively large, eliminating the advantages of the small NC size.

Here we demonstrate a fabrication scheme which bridges the dimensional gap between lithographic and NC sizes, by lithographic contacting of previously self-assembled NC chains. Because one or more NCs are incorporated into the edge of the large electrode, all of the important tunnel junctions are defined by self-assembly rather than lithography. This method allows the fabrication of one-dimensional island arrays, similar to those used for metrology, with predictable electronic characteristics. Specifically, we show that the electronic behaviour of a double-island device can be fully explained using the standard theory of Coulomb blockade with very few adjustable parameters.

Our fabrication consisted of three steps: (1) The 50-nm diameter commercially obtained gold NCs were coated with alkanethiol spacer molecules; the NCs were supplied with charged citrate on their surfaces to keep them suspended in solution. (2) The NCs self assembled into a variety of structures and were deposited on a substrate consisting of SiO\textsubscript{2} thermally grown on a degenerate Si crystal; the Si substrate is used as a gate electrode. (3) After locating the self-assembled structure of interest, electron-beam lithography was used to contact the structure with gold source and drain electrodes.

After coating the NCs with octanethiol,\textsuperscript{8} degenerately doped Si substrates with 300 nm thermal oxide and alignment markers were placed into the NC solution and left for 15 min, during which NCs precipitated on the substrate. The substrate was then removed and rinsed for 1 min with ethanol and blow-dried with nitrogen. Samples for TEM were produced in the same way on carbon-coated Cu grids. The deposited NCs were imaged with SEM and self-assembled chains were contacted using the following steps: Electron-beam lithography [950,000 molecular weight poly(methylmethacrylate), single resist layer]; development of the exposed resist; brief oxygen-plasma etching to remove organic residues; thermal evaporation of 40 nm Au; and liftoff.

The deposition process results in a variety of structures. In addition to chains [Fig. 1(a)] and branched structures, both indicative of diffusion-limited aggregation,\textsuperscript{9} we also observe two- and three-dimensional NC aggregates. Aggregation likely occurs in solution after addition of the thiols in step 1, as indicated by a color change from red to purple.\textsuperscript{10} Similar to pyridine, described in previous work,\textsuperscript{11} thiols displace the charged citrate molecules from the NC surface, thereby lowering the repulsive force between crystals and inducing agglomeration. The local structure of the chains is often characterized by parallel NC facets [Fig. 1(a) arrows]. The gaps between NCs are 1 nm wide, as seen in TEM. Fig. 1(b) shows a double-NC device with lithographic source and drain electrodes attached. We emphasize that the self-assembled chains can be robust enough to survive all of the steps required for e-beam lithography of the leads. Two NCs framing the two island NCs become part of the electrodes. With this method, devices with N islands generally consist of chains of at least N + 2 NCs. We have measured a low contact resistance for 50-nm wide Au thin-film test stripes on the same
substrate contacted with the same method, and infer that the resistance between the electrodes and the incorporated NCs is small. Therefore, the tunnel junctions that determine the device characteristics are all defined by self-assembly.

The samples were held in liquid He and a small (870 µV) AC voltage at frequency 13 Hz was applied between source and drain, together with a DC drain-source voltage. The AC current was measured with a current amplifier and lock-in amplifier. Twenty percent of the devices had resistances of 0.1 – 20 GΩ at room temperature; the remaining 80% were either shorted (probably due to the sintering of NCs during plasma etching) or had infinite resistance. Fifty percent of the conductive devices exhibited Coulomb-blockade at 4.2 K.

Fig. 2(a) shows the differential conductance dI/dV_{DS} as a function of drain-source V_{DS} and gate V_G voltages, of the double-island structure whose micrograph is shown in Fig. 1(b). Near V_{DS}=0, the conductance is suppressed because of the energy cost to add an electron to one of the islands. This is called Coulomb blockade. Two Coulomb blockade regions (large and small white diamonds near V_{DS}=0) are seen. One also observes four peaks in dI/dV_{DS} (diagonal dark lines) per gate period. The Coulomb charging energy, based on the size of the diamonds is ~20 meV, which is why such well-resolved structure can be seen in dI/dV_{DS} at liquid He temperature.

These data are compared to a simulation of the conductivity plot expected for a double-island device made of four 50-nm diameter spheres with 1 nm dielectric cap layers, separated by 1 nm, connected in series with the outer two incorporated into the electrodes [Fig. 2(b)]. The simulation consists of two parts. First, a finite element calculation is made of the capacitance matrix of the model structure in Fig. 2(b). Second, a semiclassical Monte Carlo simulation is made of the tunneling rate as a function of V_{DS} and V_G. In the Monte Carlo simulation, the double island is modeled as a purely classical network of resistors and capacitances [Fig. 2(c)], but charge quantization is imposed. The interdot thiol spacing layers are considered as tunneling barriers that couple each of the two outermost islands to the leads with capacitance C_L and the two centre islands together with capacitance C_M. The capacitance between each of the islands and the degenerate silicon substrate is C_G.

As seen in Fig. 2(d), and as discussed further below, our simulations predict the experimental behaviour quite well. Specifically, the simulation reproduces the two diamonds and the four peaks per gate period. The resistances of the tunnel junctions are adjusted to describe the experimental data. One resistance has to be much smaller than other two in order to give the prominent peaks in dI/dV_{DS}, the sum of the resistances is determined directly from the observed average conductance above the threshold for Coulomb blockade. It is remarkable...
that the simulation provides an excellent description of the data with only the resistances as adjustable parameters.

Deeper understanding of the pattern of the differential conductance is obtained by considering the charge states of the double-island system. These states are labeled by the number of extra electrons in the first and second islands, m and n, respectively. At zero V_{DS} the current is zero unless the chemical potentials of the two islands \( \mu_1 \) and \( \mu_2 \) are the same, which is very unlikely at any value of \( V_G \). However, at finite V_{DS} \( \mu_1 \) and \( \mu_2 \) can both fall between the chemical potentials of drain and source. In particular, electrons can pass through the device by means of a cycle such as \((m,n) \rightarrow (m+1,n) \rightarrow (m,n+1) \rightarrow (m,n)\), and holes can pass by means of a cycle such as \((m+1,n+1) \rightarrow (m+1,n) \rightarrow (m,n+1) \rightarrow (m+1,n+1)\).

A step-like increase in the current occurs whenever a new channel of this kind enters the window \(-eV<\mu<\mu_{C\text{G}}\). From this one can determine the number of accessible current-carrying channels, and the results are shown in Fig. 3(a). There is a peak in d\(I/dV_{\text{DS}}\) at the voltages at which a new channel is added, giving the set of lines in Fig. 3(b). The fitted capacitance values from Fig. 3(b), \(C_L=8.2\pm0.2\ aF\), \(C_M=4.5\pm0.1\ aF\) and \(C_G=0.785\pm0.015\ aF\), agree reasonably well with the results of our finite-element analysis, \(C_L=4.9\ aF\), \(C_M=3.7\ aF\) and \(C_G=0.84\ aF\). The model underestimates \(C_L\) and \(C_M\) to some extent, probably because we omitted parallel NC facets, whereas the agreement with experiment is much better for \(C_G\), for which the exact crystal shape is less significant.

A remarkable property of this device is the high ratio of gate capacitance to total capacitance, which is an order of magnitude larger than for previous NC devices.\(^5\) This is obviously the result of incorporating a NC into the edge of each electrode, reducing the capacitance between the outermost island and the electrode. This makes it possible to access multiple charge states with moderate gate voltages, an important requirement for nanoelectronic devices. Another valuable feature is the high stability of the electronic properties of our devices, whereas previous authors reported multiple “switching” events due to changes in background charges.\(^3,5\) This property, the origin of which is not yet fully understood, will be of practical importance for a future implementation of NC-based electronic devices.

In summary, we have demonstrated a new fabrication route for making one-dimensional metal-island arrays based on a combination of self-assembly of surfactant-coated NCs and lithography. The electronic properties of a double-island device at 4.2 K are successfully predicted with combined finite element and Monte Carlo modeling. Furthermore, all features in the differential conductance are explained by the conventional Coulomb blockade model. This fabrication method may be useful for studying other nano-electronic devices.

The double-diamond structure at small V_{DS} clearly identifies the Coulomb blockade region of the device; the values of \((m,n)\) for the successive diamonds is indicated. At higher V_{DS}, the differential conductance shows evidence of the two charge transfer processes, for electrons or holes (or both) sequentially tunneling through the device [Fig. 3(a)]. Comparing the data in Fig. 3(b) to the diagram in Fig. 3(a), one can determine the number of tunneling channels at any values of V_{DS} and V_G.

The fitted capacitance values from Fig. 3(b), \(C_L=8.2\pm0.2\ aF\), \(C_M=4.5\pm0.1\ aF\) and \(C_G=0.785\pm0.015\ aF\). The model underestimates \(C_L\) and \(C_M\) to some extent, probably because we omitted parallel NC facets, whereas the agreement with experiment is much better for \(C_G\), for which the exact crystal shape is less significant.

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