Capacitor Technologies: Characterization, Selection, and Packaging for Next-Generation Power Electronics Applications

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Abstract—DC-bus capacitors take up substantial space in an electric vehicle (EV) traction inverter, limiting the traction drive’s volumetric power density. Film capacitors are typically used, but other capacitor technologies with higher energy densities can help reduce the overall size. In this article, several commercial capacitor technologies are considered for use as dc-bus capacitors for EV traction inverters. They are characterized, evaluated, and compared for optimized design for volume reduction. This article also proposes a novel capacitor packaging technique that utilizes symmetrically distant parallel capacitor branches from termination, which improves electrical and thermal performance compared to a traditional flat-printed circuit board-based design. The proposed design was prototyped for a 100-kW traction inverter, and then, the thermal and electrical characteristics were evaluated under various operating conditions. Results show that the proposed symmetrical design has 40% lower layout inductance and 80% lower temperature difference than a traditional package among the parallel capacitor branches.

Index Terms—Capacitor characterization, electric traction drive, high-energy-density capacitor, lead lanthanum zirconate titanate (PLZT) capacitor, low-inductance capacitor packaging.

NOMENCLATURE

- α: Dielectric material constant.
- Δt: Switching time.
- ΔV: Voltage oscillation.
- ω: Operating frequency in rad/s.
- ψm: Magnet flux.
- C: Capacitance.
- ESL: Equivalent series inductance.
- ESR: Equivalent series resistance.

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dielectric leakage current are modeled with $R_{dc}$, which is also parallel to the total capacitance $C$. The circuit is then simplified and shown on the right of Fig. 1. In the figure, ESL represents the total inductance that contributes to the inverter’s commutation-loop inductance, thus deteriorating the switching performance. According to [6] and [7], total losses can be modeled using an ESR; the transformation is shown in the following equation:

$$\text{ESR} = R_e + \frac{1}{\omega} \left( \frac{\alpha 2\pi}{1 + (\alpha 2\pi C)^2} \right)$$  \hspace{1cm} (1)

where

$$R_d = \frac{\alpha 2\pi}{\omega}.$$  \hspace{1cm} (2)

In the equations, $\alpha$ is the dielectric material constant and $\omega$ is the operating frequency in rad/s. In the simplified model, ESR is in series with ESL and total capacitance, which generates all the losses in the capacitor. The parameters shown in Fig. 1 are highly dependent on operating temperature ($T$), bias voltage ($V_{dc}$), and operating frequency ($f$). Thus, it is necessary to extract the parameters of a capacitor accurately for volume optimization in motor drive applications.

Volume optimization of a dc-bus capacitor for three-phase motor drive applications has been studied in several papers. In [2] and [8], the process of identifying the rms current stress on the dc-link capacitor, along with the required capacitance for a three-phase inverter, is presented for the optimal selection of the capacitor bank. A new modulation technique is proposed in [9] to reduce the dc-link capacitor’s rms current stress for a dual three-phase motor. In this method, two three-phase inverters are utilized instead of a single inverter; thus, overall inverter volume may not be optimized. In [10], an additional current source inverter is used to control the dc-link voltage in the low-speed region, thus reducing the rms current stress of the dc-link capacitor. This method will increase the capacitor lifetime by reducing capacitor losses but will adversely affect the overall inverter volume. Other papers discuss different capacitor technologies and their advantages and disadvantages for motor drive applications [11], [12]. Although dc-link capacitor volume optimization topics for three-phase motor drive applications are widely discussed in the literature, few references compare different capacitor technologies for the inverter volume optimization.

Moreover, a small number of papers show high-frequency characterization of a capacitor for dc-bus applications [7], [13]–[16]. In [7], Class II MLCC and PLZT capacitors are compared at 120 Hz operation, showing that MLCCs are better in terms of losses up to 90 °C operating temperature. A calorimetric method is presented to identify the ESR of the capacitor in [13], where ESR is modeled with respect to bias voltage and rms current. Still, no results addressed temperature variation. In this article, three capacitor technologies are characterized at various bias voltages, frequencies, and temperatures (up to 150 °C) for a fair comparison.

Furthermore, there has not been much discussion of the challenges of capacitor packaging techniques where ceramic or discrete capacitors are used. For high-power systems, a large number of capacitors are paralleled to achieve the required current conduction capability and high capacitance. Placing this large number of capacitors in a single package will introduce additional layout inductance and asymmetrical current distribution among parallel capacitor branches, which can adversely affect semiconductor device-switching performance and the capacitor’s lifetime.

With the introduction of wide bandgap devices (e.g., silicon carbide metal–oxide–semiconductor field-effect transistors and gallium nitride (GaN) high-electron-mobility transistors), an increasing amount of applications demand capacitors with high-current capability at high frequencies. Applications requiring high-power density, such as dc–dc converters for aerospace electrification, utilize switching frequencies at megahertz range to reduce passive components’ volume [17], [18]. Another emerging application is high-power wireless charging, where the power level increases from several kilowatts to several hundred kilowatts with an operating frequency up to 85 kHz [19], [20]. A similar trend can be seen in traction inverters, where challenges have arisen with high-speed, low-inductance motors. The low-inductance windings introduce high-current distortion, which increases motor and inverter losses. One way that this challenge can be eliminated without introducing a large sine filter at the output of the inverter is to increase switching frequency, which increases the fundamental frequency of the dc-link capacitor current. Other topologies proposed in the literature increase the fundamental frequency of the capacitor current by interleaving segmented phase legs [21]. This high-current, high-frequency operation is possible only if the capacitor bank has low inductance. Otherwise, the capacitors will operate at a nonideal inductive region. The traditional packaging approach using flat, rectangular PCBs is discussed in [22]. It can be seen that a flat-design layout could introduce large inductance compared to a similarly sized film capacitor and may not be suitable for high-performance applications. Thus, this article also presents a novel circular capacitor packaging technique to overcome the challenges mentioned above.

The first part of this article discusses emerging capacitor technologies based on experimental characterization; the detailed results can be found in [23]. The second part of this article discusses the challenges of the ceramic capacitor packaging technique and will introduce a novel symmetrical package to improve thermal and electrical performance. The proposed package performance is then validated with experimental results.

II. EMERGING AND EXISTING CAPACITOR TECHNOLOGIES

The most commonly used dc-bus capacitors available in the market are electrolytic capacitors, ceramic capacitors, and film capacitors. Electrolytic capacitors have the lowest cost and
the highest energy density. Although these capacitors are the most popular choice for conventional motor drive applications, their short lifespan, limited current conduction capability, and low-frequency operation [11], [24] make them untenable for use as dc-bus capacitors in EV traction inverters. Thus, electrolytic capacitors are not considered in the comparison presented in this article.

In contrast, film capacitors show high-current conduction capability, high-frequency operation, and lower ESR compared to electrolytic capacitors [14]. Moreover, it shows self-healing properties [25], [26], which increases reliability and makes it a popular choice for industry. Film capacitors use plastic/polymer as the dielectric and have very low-temperature dependence; thus, the change in the dielectric characteristic is minimal. The relative permittivity of these dielectrics is low (i.e., 2–3); therefore, film capacitors are bulkier in comparison to electrolytic capacitors. Furthermore, the operating temperature of commercially available film capacitors is also low (∼105 °C), thus necessitating an active-cooling strategy [27]. Due to these factors, film capacitors may not be the optimal choice for the next generation of power-dense inverters.

Another promising candidate for use as a dc-bus capacitor is the ceramic capacitor, which uses ceramic dielectric with a very high dielectric constant. These capacitors can be constructed using a single-layer structure for small capacitance or by stacking multiple layers to achieve higher capacitance; the latter is commonly known as MLCC. MLCC capacitors have a much higher rms current rating, can withstand higher temperatures, and have much higher energy density than film capacitors [14], [23]. The most common dielectric used in MLCCs is barium titanate (BaTiO₃), which is a Class II ferroelectric dielectric material, and the parameters are highly temperature-dependent [28]. Tables I and II present the properties of common dielectric materials in high-power capacitors. Moreover, the capacitance of the Class II ceramic capacitor decreases rapidly with the dc bias voltage. Thus, a higher number of capacitors are required for a given energy density compared to film capacitors; this introduces an additional challenge in the capacitor layout for equal current distribution. There are also reliability issues associated with ceramic capacitors; the ceramic dielectric material is rigid and can crack due to mechanical and thermal stress, thus creating a short-circuit between dc terminals [28]. For these reasons, ceramic capacitors have not gained popularity for safety-critical applications such as EV traction inverters.

Another emerging ceramic capacitor technology available in the market is the PLZT-based capacitor. PLZT is an antiferroelectric dielectric material that can withstand higher currents and temperatures [32]. Unlike ferroelectric material, antiferroelectric material exhibits an incremental capacitance with respect to the bias voltage. Furthermore, the market-available PLZT capacitor is more reliable than MLCCs. Its reliability is achieved by utilizing the series connection of two MLCC geometries in one component, meaning that the capacitor will be operational in the event of a crack in the dielectric. The copper electrodes on these capacitors improve the electrical and thermal performance and can withstand a higher operating temperature (150 °C); thus, these capacitors may enable the development of high-power-density traction inverters.

### Table I

| Material            | Class 1 Ceramic | Class 2 Ceramic | PLZT | Plastic/Polymer |
|---------------------|-----------------|-----------------|------|-----------------|
| BaTiO₃              | –               | 300–7000        | –    | –               |
| Ba₂Ti₃O₇            | 40              | –               | –    | –               |
| (ZrSn)TiO₄          | 37              | –               | –    | –               |
| ZnTaO₆              | 37              | –               | –    | –               |
| PLZT                | –               | –               | 500–1500 | –               |
| Polypropylene       | –               | –               | 2.2  | –               |
| Polyethylene        | –               | –               | 2.3  | –               |

### Table II

| Material        | Temperature Dependence | Capacitance with Bias | Operating Temperature |
|-----------------|------------------------|-----------------------|-----------------------|
| BaTiO₃          | High                   | Decrease              | 85 °C–150 °C          |
| Ba₂Ti₃O₇        | Stable                 | No change             | –                     |
| (ZrSn)TiO₄      | Stable                 | No change             | 125 °C–150 °C         |
| ZnTaO₆          | Stable                 | No change             | –                     |
| PLZT            | High                   | Increase              | 150 °C                |
| Polypropylene   | Stable                 | No change             | –                     |
| Polyethylene    | Stable                 | No change             | 85 °C–125 °C          |

*Temperature are based on the available packaged capacitors.

### III. Capacitor Selection

To optimize the dc-bus capacitor volume, three capacitor technologies—film, MLCC, and PLZT—were selected for detailed experimental characterization [23]. The objective was to identify the equivalent circuit parameters (shown in Fig. 1) of the selected capacitors for various temperatures, bias voltages, and frequencies so that the volume of each capacitor technology would be comparable to a BMW-i3’s capacitor bank.

An experimental test bed was developed to characterize the individual capacitor technologies [23]; some of the significant results are shown in Fig. 2(a)–(d). It can be seen that the film capacitor parameters do not vary with respect to operating conditions.

In contrast, the capacitance of the Class II MLCC capacitor decreases by 70% with dc bias voltage [Fig. 2(a)] but increases with higher operating temperatures [Fig. 2(b)]. An increase of capacitance with temperature will decrease impedance; thus, the capacitor operating under higher temperatures will take more current and may experience thermal runaway, resulting in premature failure. The PLZT capacitor demonstrates slightly different characteristics: the capacitance of the PLZT capacitor increases with the bias voltage (up to 400 V) and with temperature (up to 75 °C), but, unlike MLCCs, the capacitance value decreases with incremental changes to the operating temperature [Fig. 2(b)]. The decrease in capacitance increases.
TABLE III
IDENTIFIED PARAMETERS ALONG WITH THE ADVANTAGES AND DISADVANTAGES OF THE SELECTED CAPACITORS [23], [33]–[35]

| Parameter                        | Film          | MLCC          | PLZT          |
|----------------------------------|---------------|---------------|---------------|
| Energy density                   | 80 J/dm³      | 350 J/dm³     | 172 J/dm³     |
| Capacitance density              | 0.47 mF/dm³   | 4.37 mF/dm³   | 2.25 mF/dm³   |
| Thermal runaway                  | Immune        | Prone         | Immune        |
| Reliability                      | High          | Low           | Medium        |
| Inductance, ESL                  |              | Low           | Medium        |
| Current carrying capability      | 4 Amps @ 50 kHz, 85 °C | 5 Amps @ 50 kHz, 85 °C | 8 Amps @ 50 kHz, 85 °C |
| Actual ESL                       | 13 nH @ 10 MHz | 4.58 nH @ 10 MHz | 3.57 nH @ 10 MHz |
| ESR                              | Low           | Medium        | Medium        |
| BMW-13 capacitor (0.644 L)       | 0.612 L       | 0.123 L       | 0.155 L       |

Fig. 2. (a) Change in capacitance with respect to bias voltage showing bias-dependent capacitance value of MLCC and PLZT. (b) Change in capacitance with operating temperature. (c) Effect of bias voltage on ESR, especially on PLZT capacitor. (d) Change in ESR with operating temperature; showing that PLZT ESR is identical to film and MLCC at high-temperature operation.

the capacitor impedance after 75 °C, meaning that the hottest capacitor will conduct the lowest current (i.e., positive temperature coefficient), ensuring natural current balancing through parallel capacitor branches and thus increasing the PLZT capacitors’ reliability by avoiding thermal runaway.

Although PLZT capacitors show high-temperature operation and higher reliability, they have challenges associated with the losses at higher bias voltage. The change in ESR of PLZT capacitors with bias voltage is plotted in Fig. 2(c), where the base ESR value is at 0 V bias with 25 °C operating temperature. It can be seen that the ESR (i.e., capacitor losses) may increase more than 300% for PLZT capacitors at full bias voltage. The change in ESR with the operating temperature at 400 V bias voltage shows promising results [Fig. 2(d)]. The ESR value of PLZT decreases with higher operating temperatures, and the value for all three capacitors becomes similar at 100 °C, suggesting that the PLZT capacitor will provide better performance at higher operating temperatures. Experimentally identified parameters along with advantages and disadvantages of the three selected capacitors are shown in Table III. It is evident from the table that the ceramic-based capacitor has a much higher energy density than the widely used film capacitor. Furthermore, the ceramic capacitor has high-current and high-temperature operation and shows ≈65% lower ESL compared to film capacitors, thus making it suitable for next-generation power electronics. Finally, the volume of the capacitors is compared with the 2016 BMW-i3’s capacitor volume, which indicates more than 70% volume reduction using ceramic capacitor technologies.

The comparison shows clear advantages of using ceramic capacitors: MLCC (barium titanate-based Class II) and PLZT ceramic capacitors. The Class I ceramic has a much lower energy density and is not included in this study. Among the two candidates, PLZT has a higher temperature operation capability, low ESL, higher reliability (i.e., series–parallel structure and avoiding thermal runaway), and high-current operation. These advantages make PLZT capacitors suitable for next-generation power-dense applications and thus were selected for the rest of the study.

IV. CAPACITOR SIZING

In this section, a capacitor bank is sized based on a 100 kW traction drive system with 30 kHz switching frequency using an interleaved inverter topology named segmented inverter. This inverter can reduce the capacitor rms current stress by 50% compared to well-known two-level, three-phase inverters using a specific modulation technique [9], [36]. A circuit diagram of the segmented inverter is shown in Fig. 3.

Capacitors’ rms stress is first estimated to identify the required current-handling capacity based on a 100 kW motor. The motor and power electronics parameters are shown in Table IV. A simulation model is created using these parameters to evaluate the motor current at various operating points, and then, the current values are used to evaluate the capacitor current stress. The selected motor’s torque–speed characteristics along with peak-phase current are presented in the surface plot in Figs. 4 and 5. The motor current values are used to evaluate the capacitor rms current at maximum power over all modulation ranges. Three different modulation techniques were used to evaluate capacitor current: 1) carrier-based triangular modulation with 180° phase shift; 2) sawtooth with 90° phase shift; and 3) discontinuous space vector modulation.

It can be seen that the maximum rms current (Fig. 6) is the same for all three modulation techniques and occurs at the
TABLE IV
MOTOR AND INVERTER PARAMETERS

| Parameter                  | Value |
|----------------------------|-------|
| Permanent magnet motor     |       |
| Number of phases           | P 6   |
| Stator resistance          | R_s  6.25 mΩ |
| Stator inductance          | L_{d,q} 22 μH |
| Magnet flux                | ψ_m 0.0256 Wb |
| Poles/Phase pairs          | P_p  8  |
| Maximum speed              | S 20 kRPM |
| Inverter                   |       |
| Switching frequency        | f_{sw} 30 kHz |
| DC voltage                 | V_{dc} 800 V |
| Dead time                  | t_{dt} 500 ns |

Fig. 3. Circuit diagram of segmented inverter feeding two three-phase motors.

Fig. 4. Torque–speed characteristics of the motor.

Fig. 5. Motor-phase current for all operating conditions.

The results suggest that the capacitor bank is required to handle 120 A rms current.

The next step in capacitor sizing is to estimate the required capacitance to keep the voltage fluctuation within 5% of the rated voltage [37]. This voltage fluctuation is inversely proportional to the frequency of the capacitor current; thus, increasing the frequency will decrease the capacitance value for the given fluctuation voltage. A fast Fourier transform (FFT) is performed over all three capacitor currents to identify the frequency components, and the currents are plotted in Fig. 7. It can be seen that the triangular modulation technique will introduce much higher frequency components and, thus, will require a smaller capacitance value for the same voltage oscillation. A simulation-based approach is used to identify the required capacitance value, where the capacitor current is integrated and then divided by the required voltage oscillation, which is 40 V (5% of 800 V bus) as shown in the following equations:

\[ i_c = C \frac{\Delta V}{\Delta t} \]  \hspace{1cm} (3)

\[ C = \frac{\int i_c \Delta t}{\Delta V} \]  \hspace{1cm} (4)

where \( i_c \) is the capacitor current, \( C \) is the capacitance, \( \Delta t \) is the switching time, and \( \Delta V \) is the voltage oscillation. The capacitance values for different modulation schemes are tabulated in Table V. The results show that the capacitor bank must handle \( \approx 120 \)-A rms current with only 15 \( \mu \)F capacitance.
for the triangular technique and 25 μF for the sawtooth modulation technique. Although 15 μF is enough capacitance to keep the voltage oscillation within limits, a 25 μF package is developed to test all modulation techniques in a laboratory environment.

In summary, Sections II–IV describe the capacitor selection and sizing process for a traction inverter. Various capacitor technologies were reviewed for dc-link energy storage, and three promising technologies were investigated. Samples from identified capacitor technologies (i.e., film, ceramic, and PLZT) were selected for detailed characterization to identify equivalent circuit parameter values at various operation points (i.e., operating voltage, temperature, and frequency). After the capacitor characterization, the permanent magnet synchronous motor model was developed to represent the load; inverter topologies and modulation techniques were identified to evaluate the maximum rms current and frequency of the capacitor current. Based on the values, capacitor banks with each technology were sized, and ceramic-based capacitors were found to provide the best possible solution in terms of power density. A flowchart showing the capacitor selection and sizing process is shown in the Appendix (Fig. 23).

V. CAPACITOR PACKAGING AND ASSEMBLY

It is clear from previous discussions that PLZT-based capacitors can be utilized to optimize dc-bus capacitor volume for traction inverters due to their higher energy density, high-current conduction capability, and high-temperature operation. These capacitors use antiferroelectric ceramic dielectric material, which is brittle and thus produced in a small package; therefore, hundreds of discrete capacitors would be required to develop a high-current, high-capacitance package for the 100 kW electric-drive application.

Paralleling a large number of capacitors is challenging, as the asymmetrical layout will increase overall inductance and introduce current asymmetry among the parallel capacitor branches. Thus, this section proposes a novel circular packaging technique to optimize the electrical performance of a capacitor bank; an exploded diagram of the proposed capacitor package is shown in Fig. 8. The package is developed by sandwiching capacitors between two PCBs to improve the capacitor fill factor. In the top board, capacitors are placed in the outer periphery of the circle. The bottom board is designed to fill in the hollow space on the top PCB, and the remaining areas are reserved for connectors. A cross section of the board is shown in Fig. 9, where the current loops are shown. It can be seen that all the capacitors maintain a symmetrical distance from the termination. Moreover, the current return path has no obstruction and, thus, will overlap with the input current path, reducing layout inductance. On the other hand, a traditional flat capacitor board will have an asymmetrical distance from each capacitor to the termination. The current return path will be obstructed by the PCB vias, thus introducing additional layout inductance, as shown in Fig. 10.

Another challenge with this type of flat design is the asymmetrical current distribution at high frequency. The capacitors closer to the termination will take a higher current due to the low-impedance path than the capacitors further away from terminations. At the same time, the circular capacitor package will allow symmetrical current distribution and increase the capacitor’s lifetime due to the symmetrical path. The boards mentioned above were designed for each phase leg of the inverter using a 1 mm-thick PCB with 70 μm copper tracks to handle 20 A rms current (one-sixth of 120 A).

An 800 V PLZT capacitor package was selected [37], which contains three parallel capacitors. The packages were designed for each phase leg of a segmented inverter to achieve 4.2 μF capacitance (for a total 25 μF for six phase legs). PLZT capacitors can handle much higher current than film capacitors; thus, they are sized using the capacitance value. The design considered the experimentally evaluated parameter values (i.e., single capacitor in Section VI) and paralleled 15 capacitors in each package; the assembled top and bottom boards are shown in Fig. 11(a) and (b), respectively. A special connector was designed to take out the terminations from one end of the package, as shown in Fig. 8. Finally, all the boards and connectors were assembled to form the circular capacitor package shown in Fig. 11(c) and (d). Traditional PCB-based flat capacitor boards were also designed using 15 parallel capacitors; two different boards were designed with 5 × 3
Fig. 11. (a) Top PCB with five parallel capacitors, (b) bottom PCB with ten parallel capacitors, (c) assembled capacitor package’s top view, and (d) bottom view showing the four pin connectors of the assembled capacitor package.

Fig. 12. Two flat capacitor boards were designed and assembled showing (a) capacitor board containing 15 capacitors in a $5 \times 3$ configuration and (b) capacitor board designed in $3 \times 5$ configuration.

and $3 \times 5$ arrangements to compare the electrical and thermal performance, as shown in Fig. 12(a) and (b), respectively.

VI. EXPERIMENTAL CHARACTERIZATION

A. Electrical Characterization

Capacitors were characterized individually and in different packages to evaluate equivalent circuit parameters at various frequencies, temperatures, and bias voltages. First, the selected discrete PLZT capacitor was characterized, followed by the packaged capacitor boards. The experiment discussed in this section was conducted by connecting two similar capacitors or capacitor packages in series. One was connected to a dc source (for biasing purposes), and the other acted as a dc block. The voltage across the two series capacitors will be zero; thus, any network or component analyzers can be used for small-signal analysis. A PCB was designed to characterize the capacitors containing two series capacitors, charging–discharging resistors, and a dc supply to vary the bias voltage from 0 to 800 V. An environmental chamber was used to evaluate the parameters at various operating temperatures ($-25^\circ C$–$150^\circ C$). A network analyzer was used to inject a small signal and measure the phase and impedance of the two series-connected capacitors. Then, the results were postprocessed to identify the equivalent circuit parameters of a single capacitor package. The setup is shown in Fig. 13.

The test results of a single capacitor are plotted in Fig. 14(a)–(d), where capacitance and ESR values in Fig. 14(a) and (c) are taken at room temperature ($25^\circ C$) with an injection frequency of 100 kHz.

The results in Fig. 14(b) and (d) are taken at full bias voltage (800 V) with 100 kHz injection frequency. It can be seen that the capacitance of the PLZT capacitor increases with bias voltage up to 800 V, which is an antiferroelectric behavior. The capacitance value showed a different character when the operating temperature was varied; it increased when the temperature varied from $-25^\circ C$ to $75^\circ C$ and then decreased beyond $75^\circ C$. This capacitance behavior with temperature ensures current balancing among the parallel capacitor branches and avoids thermal runaway. Another challenge with PLZT capacitors is the increase in ESR with bias voltage [Fig. 14(c)], which is much higher than the similarly sized film or ceramic capacitors [23]. On the other hand, the ESR reduces drastically with operating temperature and reaches a steady state at around 100 $^\circ C$ [Fig. 14(d)], suggesting that this type of capacitor will perform best if operated at or more than 100 $^\circ C$. Similar tests were carried out with the circular package; the results are shown in Fig. 14(e)–(h). Results show the same trend as the single capacitor; the parameters of the circular capacitor are presented in Table VI. It can be seen that the designed circular capacitor has a minimum of 4.2 $\mu F$ capacitance at $-25^\circ C$.  

![Network analyzer](image)

![Thermal chamber](image)

![Charging & discharging resistors](image)

![Capacitors](image)

![DC supply](image)

Fig. 13. Circuit diagram of capacitor characterization setup showing the network analyzer, environmental chamber, and single capacitor characterization board.
The inductance of these capacitors is independent of bias voltage and operating temperature and, thus, measured at zero bias voltage at room temperature (25 °C). An OMICRON Bode 100 network analyzer with two-port shunt through measurement was used to capture a low-inductance value. The analyzers can measure down to 1 nH [38] with the measurement technique described in [39]. According to the measurement, the circular capacitor has a 3 nH input inductance measured from the termination points, which is ≈40% less than the flat capacitor boards. This reduction will not only reduce the voltage overshoot but will also improve device-switching performance; the comparison is shown in Table VI.

B. Thermal Characterization

This section evaluates the thermal performance of the designed circular capacitor board and compares it with the traditional flat capacitor board. The performance of the capacitor was assessed by injecting a high-frequency triangular current. A GaN-based half-bridge power module was utilized as a synchronous buck converter to transfer energy between the input and output capacitor bank, as shown in Fig. 15. An inductor was used in series with the test capacitor, and the inductance value was varied to keep the rms current constant at 40 A at different operating frequencies; the results at 60 kHz are shown in Fig. 16. According to the datasheet, these capacitor packages can handle more than 100 A current at 85 kHz frequency. In this case, however, the maximum rms current is limited to 40 A to keep the GaN device temperature below 130 °C.

All the assembled capacitor packages were painted black, and a thermal camera was used to capture the results at various switching frequencies. Images captured by the thermal camera are shown in Fig. 17(a)–(c) for flat and circular designs. The temperature distribution results (Figs. 17(a) and 18–20) show the asymmetric temperature distribution of flat capacitor boards. It is also evident from the figures that the connector was cooling down the capacitors close to the terminations. This phenomenon can also be seen in an actual inverter
Fig. 17. Packaged capacitor temperature distribution in °C: (a) asymmetric temperature distribution of the 3 × 5 flat capacitor board at 60-kHz frequency, (b) asymmetric temperature distribution of the 5 × 3 flat capacitor board at 60-kHz frequency, and (c) symmetric temperature distribution of the circular capacitor board at 60-kHz frequency.

Fig. 18. Capacitor temperature for 3 × 5 flat capacitor board at various injection frequencies.

Fig. 19. Capacitor temperature for 5 × 3 flat capacitor board at various injection frequencies.

Fig. 20. Capacitor temperature for the proposed circular capacitor board at various injection frequencies.

Fig. 21. Average temperature variation for different packages.

Fig. 22. Temperature variations among the capacitors for different packages.

system where the busbar may be at a lower temperature than the capacitor board and will act as a heat sink for some capacitors. Also, heat from semiconductor devices can propagate to capacitor boards via busbars, which will increase the temperature of the capacitors close to the terminations. This asymmetrical temperature distribution will decrease the operating lifetime of the flat capacitor board.

On the other hand, the circular capacitor board shows a more symmetrical temperature distribution within the inner and outer circle capacitors. There are mainly two reasons for the temperature difference between the inner and outer circles.

1) The top PCB covers the inner capacitor circle; thus, the heat generated in the inner circle will be trapped.

2) The inner circle has a lower copper trace area, which can be easily modified to decrease the difference.

The maximum, minimum, and average temperatures of the capacitor packages are shown in Figs. 18–20 and are compared in Figs. 21 and 22. The flat capacitor temperatures shown in these figures are the average temperature measured from the top surface of the capacitor. First, the individual capacitor’s average surface temperature is measured to identify the minimum and maximum temperatures. Then, the total average is calculated based on the average temperature of
all 15 capacitors. Bottom capacitors were exposed in the circular capacitor board for thermal measurement; thus, average surface temperature values were used. The capacitors soldered to the top boards are buried inside; thus, small holes were created to take the thermal measurement from the bottom surface of the capacitor [Fig. 17(c)]. It can be seen from the results that the circular capacitor has a lower temperature difference (ΔT) among the parallel capacitor branches, and the change with frequency is minimal. The results suggest that the symmetrical distribution of discrete capacitors improves electrical performance by improving layout inductance and thermal distribution, thus improving the overall inverters' performance and lifetime.

VII. CONCLUSION

In this article, different capacitor technologies were reviewed to optimize traction inverter volume. Three promising capacitor technologies have been identified and their advantages and disadvantages summarized. Based on the outcome, PLZT capacitors are selected and sized for a 100-kW traction drive system. An optimized circular packaging technique has been proposed, and a package was prototyped. The developed package was then experimentally evaluated to identify electrical and thermal performance. The results show that the designed circular package has 40% less layout inductance and 80% lower ΔT at 120 kHz frequency than traditional flat capacitor boards. It can be concluded from the results that ceramic capacitors with segmented inverter topology can decrease the capacitor volume by 70%. Moreover, advanced capacitor packaging techniques can improve electrical and thermal performances, which leads to enhanced semiconductor device performance and capacitor lifetime.

APPENDIX

CAPACITOR SELECTION AND SIZING PROCESS

Design a package to improve electro-thermal performance

Select a capacitor technology and estimate required number of capacitance

Select the topology and modulation which gives lowest RMS current and higher frequency

Estimate maximum RMS capacitor current and frequency

Select modulation scheme: Carrier based, SV PWM, harmonic injection....

Select inverter topology: 2-level, 3-level, segmented....

Determine load model

Select capacitor technology: Film, ceramic, electrolytic...

Determine current conduction capability at the rated voltage and frequency

Determine capacitance at rated voltage

Estimate number of parallel capacitors to handle required current

Does the capacitance meet voltage oscillation requirement?

Yes

No

Add more capacitors in parallel until it meets the voltage oscillation requirement

Select capacitor technology with minimum volume

Table showing steps in selecting and sizing capacitors:

- Determine load model
- Select inverter topology: 2-level, 3-level, segmented...
- Select modulation scheme: Carrier based, SV PWM, harmonic injection....
- Estimate maximum RMS capacitor current and frequency
- Select the topology and modulation which gives lowest RMS current and higher frequency
- Select a capacitor technology and estimate required number of capacitance
- Design a package to improve electro-thermal performance
- Select capacitor technology: Film, ceramic, electrolytic...
- Determine current conduction capability at the rated voltage and frequency
- Determine capacitance at rated voltage
- Estimate number of parallel capacitors to handle required current
- Does the capacitance meet voltage oscillation requirement?
- Yes
- No
- Add more capacitors in parallel until it meets the voltage oscillation requirement
- Select capacitor technology with minimum volume

Fig. 23. Capacitor selection and sizing process used in this article.

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