A self-testing method of large analog circuits in electronic embedded systems

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Abstract. A new self-testing method of high-order filters consisting of a chain of first- or second-order filter units of mixed-signal electronic embedded systems controlled by microcontrollers or DSPs is presented in the paper. The main idea of the method bases on the fact that the signal response of the given filter unit is treated as the signal stimulation of the next filter unit. Thanks to this, a simple reconfigurable BIST consisting of only internal devices of the microcontroller controlling the system was obtained.

1. Introduction

In recent times, almost all electronic devices, even simple ones, are equipped with electronic embedded systems which are characterized by an embedded intelligent unit often accessible in the form of a controlling microcontroller. Mixed-signal embedded systems serving controlling functions of devices or working as intelligent sensors predominate on the market, because information about a controlled object and work environment is often obtained through analog sensors. They convert physical values to electrical analog signals, which are transmitted and initially converted in analog parts of these systems. Next, these signals are digitized by ADCs and processed by microprocessors or microcontrollers.

Hence, on each stage of signal conversion the embedded system has to work properly, because an incorrectly measured or converted or processed signal can lead to a wrong decision of the control unit, that e.g. in extreme cases can cause damage of the device controlled by the system. Thus, self-testing procedures dealing with functional testing of whole systems [1], the software testing [2,3] and testing of particular blocks of the system [4] are elaborated. One of the important blocks of the embedded systems is an analog part usually working as an anti-aliasing filter for ADCs.

For these circuits the following testing methods are used:

• based on sigma-delta modulators [5,6],
• using the oscillation-test methodology [7-11],
• based on test strategy using power spectral analysis [12]
• and based on using internal measurement devices of the microcontrollers controlling embedded system [13-16].

An advantage of the last class of the self-testing methods elaborated by the author is the fact that to test analog circuits we use already existing resources of embedded electronic systems, what simplifies the structure of built-in-testers (BISTs). It allows to minimize the test cost and guarantees the reliability of
products. These methods were elaborated for fault detection and localization of moderately complex analog circuits.

In this paper a new approach extending these methods for testing and especially self-testing of large analog circuits is proposed.

2. Principle of the approach

This approach was elaborated for all types of anti-aliasing filters (low-, high-, band-pass and band-rejection) consisting of a chain of units without feedback paths between them (figure 1). Each unit can base on a first-order filter, a Salen-Key topology or a multiple feedback topology. It can seem that this solution regards to a narrow class of analog circuits, but preferably chosen in engineering practice. It follows from the fact that recently engineers like to design simple analog circuits without feedbacks (because inappropriately designed feedbacks can influence on unstable work of the circuits), and each second-order filter unit consists of a minimum number of elements (only one operational amplifier and four passive elements) what reduces costs. Additionally, a cascade connection of these filter units allows to create any characteristic in a simple way.

It needs underlining that typically first- or second-order filters are used as anti-aliasing filters. The remaining signal filtering is realized digitally by microprocessors. But we can observe a new trend in electronic embedded system design, especially for battery systems, where possibly all signal filtering process is moved to analog parts. It shortens the activity time of the microprocessor, what finally reduces power consumption. Obviously, it causes an increase of the filter order (usually maximally to sixth- or eighth-order).

Hence, it was needed to elaborate a self-testing method for this type of high-order filters implemented in electronic embedded systems controlled by microcontrollers or DSPs. Thus, a new self-testing method for these circuits is proposed in the paper.

2.1. The idea of the self-testing method

The method allows to find which \( n \)-th unit in the chain of \( N \) filter units of the \( 2N \)-order filter is faulty. The novelty of the method and also its main idea is that we treat the signal response of the \( n \)-th unit as the signal stimulation of the \((n+1)\)-th unit. Thanks to this, the structure of the BIST is still simple in comparison to self-testing methods for simple circuits [13-16]. For the proposed method, the square impulse stimulation is applied only to the input of the first unit of the \( 2N \)-order filter (Figure 1). The ADC measures \( K \) voltage samples at the output of each unit. Thus, the self-testing method needs only one output pin of the microcontroller and its \( N \) input pins connected to the internal analog multiplexer (where typically \( N = 3,4 \), and the analog multiplexer usually has got 8 or 16 channels).

![Figure 1. Example of the electronic embedded system in mode of self-testing of the analog part, where the analog part consists of cascade of \( N \) 2\(^{nd}\)-order filters.](image)

Generally, the method consists of two stages. In the first pre-testing stage the fault dictionary for given tested analog part is created and entered to the microcontroller program memory. The second stage is self-testing of the analog part by the microcontroller. It is divided into two parts realized by the measurement procedure and by the fault detection procedure adequately.
The self-testing method will be illustrated on the example of a 6th-order low pass Butterworth filter consisting of three 2nd-order filter units (figure 2).

![Diagram](image)

**Figure 2.** The 6th-order low pass Butterworth filter, where $R_1 = R_2 = R_3 = 10 \, \text{k} \Omega$, $R_4 = R_5 = R_6 = 10 \, \text{k} \Omega$, $C_1 = 15.33 \, \text{nF}$, $C_2 = 16.5 \, \text{nF}$, $C_3 = 11 \, \text{nF}$, $C_4 = 22.5 \, \text{nF}$, $C_5 = 4.3 \, \text{nF}$, $C_6 = 62 \, \text{nF}$.

2.2. The fault dictionary

Each output signal $u_n$ is sampled two times ($K = 2$) as shown in figure 3. For the first unit the first sample $U_{1,1}$ is determined during the duration of the stimulant signal $u_{in}$ and the second one $U_{1,2}$ after the stimulation in the same way as described in [13]. However, for next units the first sample $U_{n,1}$ is taken during rising of the stimulation $u_{n-1}$ (the response of the previous unit), and the second one $U_{n,2}$ during falling of this signal.

We can make an assumption that the first sample $U_{n,1}$ is the first coordinate, and second one is the second $U_{n,2}$ coordinate of the measurement space for $n$-th unit output of the 6th-order filter (figure 4).

![Diagram](image)

**Figure 3.** Time responses of the 6th-order low pass filter (figure 2) at its unit outputs.

![Diagram](image)

**Figure 4.** Nominal areas of the low pass filter (figure 2) for respective units for 0.1% resistor tolerances and 1% capacitor tolerances.
It is assumed that tolerances of non-faulty elements are 0.1% for resistors and 1% for capacitors. For these tolerance values the nominal areas representing the nominal state of the 6th-order filter (figure 2) were drawn on the measurement spaces based on the Monte Carlo method (figure 4). Hence, if a measurement point plotted in the n-th measurement space is outside the nominal area, it means that the n-th filter unit is faulty.

The nominal areas are approximated by an ellipse \([16]\) with coordinates of its foci \((u_{n,1}^{F1}, u_{n,2}^{F1})\) and \((u_{n,1}^{F2}, u_{n,2}^{F2})\) and the length \(e_n\) of the major axis. Thus, the fault dictionary has the form: \(\{(u_{n,1}^{F1}, u_{n,2}^{F1}), (u_{n,1}^{F2}, u_{n,2}^{F2}), e_n\}_{n=1,2,N}\). The values stored in the fault dictionary are presented in the form of the code which is compatible with the ADC conversion result contained in the 8-bit data register of the ADC (left adjustment result mode). Thanks to this, the ADC conversion results can be directly compared with the fault dictionary.

### 2.3. Determination of the sample moments

The fault detection resolution (the shape of nominal areas) depends exclusively on the duration time \(T\) of the stimulation (the amplitude \(U_{in}'\) is set \textit{a priori} to \(V_{cc}\)) and on voltage sample moments \(t_{nk}\). The way of determination of these parameters for the first filter unit, for which we obtain the best detection resolution, was described in [13].

To determine the voltage sample moments \(t_{n1}\) and \(t_{n2}\) for the n-th filter unit (in this case \(n = 2,3,...,N\)), we divide the stimulation \(u_{n,1}\) of the n-th unit (the response of the previous unit, that is the (n-1)-th unit) into two parts: rise of this signal \(u_{n,1,rising}\) and its fall \(u_{n,1,falling}\). This division is marked by \(t_{n,\text{max}}\) (figure 3). Next we introduce a coefficient of the detection resolution \(\lambda_{n,i}\) of the component \(p_{i,n}\) of the tested circuit \((i=1,...,I, I = \text{the number of components of the n-th unit})\). For each n-th filter unit output signal, it is defined in the same way as in [13]:

\[
\lambda_{n,i}(t_{n,j}) = \max_{l=1,...,L} \{u_n(p_{i,n}^l,t_{n,j})\} - \min_{l=1,...,L} \{u_n(p_{i,n}^l,t_{n,j})\}
\]

(1)

where \(L\) – the number of discrete values of the component \(p_{i,n}\) in the assumed range from \(0.1p_{i,n}\) nom to \(10p_{i,n}\) nom, where \(p_{i,n}\) nom – the nominal value of the \(i\)-th component of the n-th unit, \(t_{nj}\) – the moment of the \(j\)-th sample of the signal on the output of the n-th unit, \(j = 1,..,J, J = \text{the number of samples in an analyzed time interval of the time response signal. Division (digitizing) of the signal onto J samples follows from the fact that simulation programs use only discrete values for signal analysis and simulation.}

Thank to this definition, the \(\lambda_{n,i}\) coefficient is an equivalent of a large-signal sensitivity of the circuit.

In the next step we define the coefficient \(\lambda_n\):

\[
\lambda_n(t_{n,j}) = \frac{1}{I} \sum_{j=1,...,J} \frac{\lambda_{n,i}(t_{n,j})}{\max_{j=1,...,J} \{\lambda_{n,i}(t_{n,j})\}}
\]

(2)

Timings of these coefficients for all units are shown in figure 5. The maximum value of \(\lambda_n\) represents the optimum sensitivity of the circuit voltage response measured in the n–th unit output to changes of values of all n–th unit components. Thus, we can define:

\[
\lambda_{n,\text{max}1} = \max_{j=1,...,J, t_{nj} \in (0,t_{n,\text{max}})} \{\lambda_n(t_{n,j})\}
\]

(3a)

\[
\lambda_{n,\text{max}2} = \max_{j=J, t_{nj} \in (t_{n,\text{max}}, \nu T)} \{\lambda_n(t_{n,j})\}
\]

(3b)

where \(t_{n,\text{max}}\) – the index of the sample at the moment \(t_{n,\text{max}}\), \(\nu T\) – the analyzed time interval of the time response signal, \(\nu = 1,2,...\)
In (3) the max function realizes an extremum maximum operation, what allows to improve the detection resolution.

Hence, the solution of (3) determines two moments of voltage samples for each unit response signal:

\[ \lambda_{n,\text{max}1} \rightarrow t_{n,1} \quad \text{and} \quad \lambda_{n,\text{max}2} \rightarrow t_{n,2} \]  \hspace{1cm} (4)

For these moments were determined voltage samples \( U_{n,1} \) and \( U_{n,2} \) and drawn nominal areas in figure 4.

![Figure 5. Coefficient \( \lambda \) charts of the low pass filter (figure 2) for individual units.](image)

2.4. The self-testing procedure

The self-testing procedure entirely realized by the microcontroller consists of two subsequent parts, as shown in figure 6. The first part is responsible for stimulation of tested analog part and measurements of two voltage samples \( U_{n,1} \) and \( U_{n,2} \) at \( N \) unit outputs.

Hence, in this part the following steps [13] are run \( N \) times by the microcontroller (figure 6):

- the \((n-1)\)-th channel of its analog multiplexer is set (channels are numbered from 0 to \( N-1 \)),
- the tested anti-aliasing filter is stimulated by a square impulse with programmable duration time \( T \) determined by its internal timer,
- and in the same time its internal ADC measures two samples \( U_{n,1} \), \( U_{n,2} \) of voltages of the time response on the output of the \( n \)-th filter unit at precise moments \( t_{n,1} \), \( t_{n,2} \) established by its internal timer.
In the second part the detection condition (5) for the next measurement result is tested sequentially, until it localizes the faulty filter unit or it tests all $N$ conditions (figure 5). In the first case we know which unit is faulty (the variable $s$ contains the number of the faulty unit), in the second case the filter is fault-free ($s = 0$). Obviously, the presented approach allows to find only one and only the first faulty unit in the investigated unit chain of the filter. It seems that this can be a disadvantage of the detection algorithm, but single faults constitute the majority (over ninety several percent) of all faults. Hence, this solution simplifies and accelerates the detection algorithm.

The detection condition is represented by the following inequality (basing on the taxi norm):

$$\sum_{k=1}^{2} \left( |U_{n,k}^{F_1} - U_{n,k}^{F_2}| + |U_{n,k}^{F_1} - U_{n,k}^{F_2}| \right) \leq e_n$$  \hspace{1cm} (5)

If the inequality (5) is fulfilled (the measurement point is placed inside the $n$-th ellipse), the $n$-th filter unit is fault-free.

This inequality does not need complex calculations, thus the presented detection algorithm is computationally simple, thus it can be boldly implemented in control units, especially in microcontrollers which do not have great computing power.

3. Conclusion

A novelty of the proposed approach is the extension of self-testing methods of soft fault diagnosis of passive elements in simple analog circuits elaborated by the author to new self-testing methods for high-order filters consisting of a chain of first- or second-order filter units. The main idea of the methods is that we treat the signal response of the given filter unit as the stimulation signal of the next filter unit. Thanks to this approach, the structure of the BIST used to test the high-order filter is simple, what
decreases test costs. The BIST is created only with internal devices of the microcontroller (two timers, an analog multiplexer and an ADC) and it takes only one output pin and as many input pins of the microcontroller as the filter has got units.

Nominal areas representing the nominal state of the tested circuit with component tolerances were approximated by ellipses. Thanks to this, we obtained a small size of the fault dictionary, what simultaneously allows to elaborate the simple detection algorithm.

Hence, the self-testing method can be implemented in mixed-signal embedded electronic systems where the control unit has not great computing power or the calculation time (activity of the control unit) have to limited to minimum, e.g. in wireless intelligent sensors.

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