1kW Bidirectional 48V-12V DCDC Converter Design Based on Full Bridge CLLC Topology and FDP Controlling Method for Electric Vehicles Application

Hai Liu\textsuperscript{1,2}, Lenian He\textsuperscript{1,3}

\textsuperscript{1} VLSI Department, School of Micro-nano Electronics, Zhejiang University, 733 Jianshe3 Road, Hangzhou, Zhejiang, China
\textsuperscript{2} EngD in electronic information
\textsuperscript{3} Professor

Email: liuhai@zju.edu.cn, 375641282@qq.com, helenian@zju.edu.cn

Abstract. Present electric vehicles market calls for 1kW bidirectional 48V-12V DCDC converters with high performances. The requirements that isolation and soft switching determine the power stage topology choosing range. Based on previous research results and actual requirements of this application, full-bridge CLLC topology is chosen for further analyses and designs. By properly choosing resonant devices, operating frequency (F), phase shift (P) between power side and load side, and duty (D) of power side, the power system achieves high efficiency with soft switching. Soft switching comes from a small extra time per period with no power transfer. The FPD has respective influences on the performances of the power system. For each one of FDP, there is a balance and two important performances that are conversion efficiency and output voltage accuracy which are listed for illustrating influences of FPD and choosing a best FPD for the whole system. The whole system includes power stage design on PCB and controlling stage design on integrated circuits. FPD can be designed self-adapting respectively and a simple control loop is proposed with adjustable D and settled F. A proper FPD can achieve over 98.9% efficiency and control loop can be verified workable for load variation.

1. Introduction

In recent years, fossil fuels are consuming faster and faster which causes serious energy and environment problems. To alleviate this trend, some renewable and clean energy sources such as water energy, wind energy and solar energy are entering markets. However in most applications, these energy sources cannot be used directly. They are usually changed into electric energy and then saved in a whole system that redistribute energy for different functional modules.

As for transportation field, electric vehicle is gradually replacing traditional fossil fuel vehicle. Present electric vehicle has a universal battery voltage class 48V and early electric vehicles use 48V for supplying all modules in the whole vehicle system. But limited to low energy storage, low mileage per charge and high energy consumption of intelligent devices under high voltage class, early electric vehicle must be upgraded to multi-voltage class power supply. Contemporary electric vehicle drive engine using 48V DC power supply, drive control module, gauge unit, lamps, etc using 12V DC power supply, drive on-board USB charging port using 5V DC power supply and drive CPU of on-board intelligent devices using 1V DC power supply. Among these functions, engine and some 12V applications consume most of the power and on-board batteries are configured as 48V and 12V for...
most high power functions leaving other low voltage low power functions achieved by affiliated low voltage low power converters such as 12V-5V DCDC and 5V-1V DCDC converters without corresponding voltage class batteries. [1] To increase mileage per charge, all batteries with 48V and 12V voltages class should be full charged. While being charged, electric vehicles need 48V-to-12V energy transfer; while driving, electric vehicles need both directions energy transfer and the specific energy transfer direction depends on the conditions of batteries and load. Typical maximum power of electric vehicles is 3kW to 4kW. For such a high power requirement, input-series-output-parallel structure is applied for restricting the power of single converter to around 1kW which almost reaches the extremity due to present components' properties with 3-4 same converters placed parallel. Therefore a 1kW bidirectional converter between 48V DC and 12V DC is necessary for this system. [2]

On-board converter requires isolation while high efficiency requires soft switching. To satisfy these two requirements, there are 2 types (4 kinds) typical topologies published on previous papers: full-bridge CLLC, half-bridge CLLC, full-bridge DAB(Dual Active Bridge), and half-bridge DAB. Among these 4 topologies, previous researches show that full-bridge CLLC has highest efficiency and highest stability; CLLC has wider soft switching adjusting range than DAB but CLLC has high level design and control complexity due to the nonlinearity between system gain and load; full-bridge has more components and lower power density than half-bridge but higher efficiency and higher power transfer capacity. [3] For on-board converters, safety, stability and efficiency are important factors while power density, size, complexity are relatively unimportant because there is no strong need for small volume, which is significant different from converters in some portable devices. Based on researches, analyses and verification, full-bridge CLLC is chosen for this application.

The output of the the full-bridge CLLC converter is mainly influenced by the FDP(frequency, duty, and phase shift) of driving signals when given a certain converter. All these 3 factors can be designed self-adapting or one-time setting for input, load, and resonant condition variation. A universal control loop and a specific control analysis based on self-adapting D and one-time setting F P will be presented in this paper.

### 2. Operating principle of full-bridge CLLC

Figure 1 shows the structure of a full-bridge CLLC converter operating in buck mode. In figure 1, Vin corresponds to 48V DC power supply and Io corresponds to load with output DC voltage Vo that is expected to be 12V DC. Therefore when power transfer is 1kW, the output current Io is around 83.33A. Co is a filter capacitor for reducing the ripple of Vo. Q1~Q8 are power MOSFETs driven by V1~V8 respectively. By adjusting the on and off states of these power MOSFETs reasonably, some meaningful resonants will occur in resonant components including C1, L1, L2, and C2, and this is why this structure is called CLLC. Between high side(48V side) and low side(12V side) is a transformer that is used for high side and low side isolation including high side winding LH and low side winding LL with turns ratio n(nLH:nLL) and a leakage inductance Lm that is parallel to LH operating as magnetic inductance. In fact, Vin and Io are both batteries essentially and when the converter operates in boost mode, Vin and Io can be interchanged because there is also a filter capacitor parallel to Vin which is reserved for boost mode. When introducing the operating principle based on buck mode, this capacitor parallel to a DC voltage source can be neglected.

![Figure 1](image1.png)

**Figure 1.** Full-bridge CLLC power system(buck mode).

![Figure 2](image2.png)

**Figure 2.** Resonant waves of full-bridge CLLC.
Figure 2 shows the waveforms of some important signals simulated on LTspice for illustrating the operating principle. In a half period, Q1 and Q2 are turned on and turned off at the same time which is a little later than Q5 and Q6 and they are all turned on with the same duty that is a little less than 50%. In this half, the high side current flows through Q1, L1, LH(Lm), C1, Q2 from Vin+ to Vin-(ground). The current through LH induces current in LL and generates low side current through Q5, C2, LL, L2, Q6 from Io-(ground) to Io+ which means the load is charged in this half period. In this half, L1 and C1 generate LC resonant in high side, resonant current shunts at LH and Lm. When Lm is set much larger than L1, I(Lm) increases almost linearly and I(LL) is induced by the difference between I(L1) and I(Lm). When operating frequency is a little lower than inherent frequency (determined by L1, C1, L2, and C2), there will be extra time per period for zero power transfer (load side current is kept around zero) between each half period. The dead time zone lies in this extra time range to realize ZCS (Zero Current Switching) off for load side and ZVS (Zero Voltage Switching) on for power side, which is helpful to reduce switching loss and improve efficiency. In the other half, the circuit converts to another bridge with the same current direction on load and opposite current direction on resonant components due to the full-bridge topology.

Previous researches calculate and finally provide some important parameters and experiences for devices choosing of this topology: There is a simple topology design experience that choosing L1 equals to equivalent L2 on power side, choosing C1 equals to equivalent C2 on power side, and Lm 4 times of L1; Based on the simple design, inherent frequency is equal to the reciprocal of square root of L1 times C1 and this determines the operating frequency range; Quality factor equals to square root of L1 over C1 over power side equivalent load and this determines the frequency selectivity (high quality factor correspond to better selectivity) and monotony (low quality factor corresponds to better monotony and then wide soft switching range) of gain (normalized to 1/n)-frequency (normalized to inherent frequency) curve where is a tradeoff; To realize soft switching, dead time should be enough to charge and discharge the parasitic output capacitors of power MOSFETs Q1-Q8, which put an upper limit to Lm. [4] In this paper, inherent frequency is set as 350kHz and quality factor is set as 0.4 for a normal operating range of about 340kHz-350kHz which requires L1=339.69nH, L2=21.23nH, C1=608.72nF, C2=9.73952μF, Lm=1.35876μH, and choosing rather large filter capacitor for high side of 220μF and low side of 2.2mF as shown in figure 3. [5] For further analysis, the MOSFETs are choosing as IPT004N03L with very low Ron=0.4mΩ for low conduction loss.

Figure 4 shows the input current and output voltage wave of figure 3 with typical FPD that are F=348kHz, P=0, D=48%. By measuring the output and calculation we get some performances that are Vo(ave)=11.941V, Vo(ripple)=5.8mV, Pin(ave)=1005.6W, efficiency=98.95. Figure 5 shows the Vds8, Ids8, and V8 to illustrate soft switching condition of load side MOSFET. From figure 5, it can be found that when Vds8 begins to increase from 0, Ids8 has already crossed 0 which corresponds to ZCS off.

![Figure 3. Power system schematic for simulation.](image-url)
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Figure 4. Output voltage $V(n002)$ and input current $I(V9)$ of the power system.

Figure 5. ZCS off condition of a load side MOSFET $Q8$ -- $V_{ds8}:V(n007)$ $V_{gs8}:V(n015)$ $I_{ds8}:I(d(M8))$.

3. Influence factors on full-bridge CLLC

The whole system for this application includes 2 parts: power stage is designed to be achieved by discrete devices on PCB; 8 driving signals are designed to be generated by IC controller. A complete control stage takes output condition (feedback for load variation), input condition (feedforward for input variation), soft switching condition and resonant condition (feedback for devices variation), and arm voltage (for float driving) as inputs and outputs 8 MOSFET gate driving signals.

The output driving signals mainly includes 3 meaningful parameters that are frequency, duty of power side, and phase shift between two sides due to the analysis of operating principle. Followings are analyses for each one based on simulation results.

3.1. The influence of $F$

Some operating frequencies are simulated with results in figure 6.

![Resonant waves at different F](image)

(a) (b) (c)

Figure 6. Resonant waves at different $F$ (a)340kHz (b)348kHz (c)350kHz.

From figure 6, some points can be concluded as follows:

If operating frequency is higher than inherent frequency, high side resonant inductor and leakage inductor will not resonant together, and there is no time interval for zero-current transformer and finally there is no time space for soft-switching.

If operating frequency is much less than inherent frequency, too much time for resonant together raises the peak resonant current to a very high value which will cause large conduction loss and even abnormal resonant waveform in a period (in one half period, resonant current may not change direction due to very high initial value (the end of last half period)).

If operating frequency is a little smaller than inherent frequency, soft switching can achieve and related conduction loss will be affordable when considering the reduction of switching loss.

Within a proper range, lower operating frequency brings about more time for zero-current transformer and then larger design margin for D and P to achieve soft-switching. However lower operating frequency brings out higher conduction loss. Here is a balance.

3.2. The influence of $P$

Some phase shift are simulated with results in figure 7.
Figure 7. Soft switching condition at different P (a)0.0% (b)0.5% (c)1%.

From figure 7, some points can be concluded as follows:

When operating in buck mode, advancing the phase of low side a little (about 0.1%-1% of period) can achieve soft switching which rationally utilizes the design margin left by F. When P=0, soft-switching can theoretically achieve at the design edge, but due to the parasitic influences of real devices, soft-switching can not achieve. When P is too large, the output voltage will increase to a very high voltage which is not desired.

Higher P causes significant increasement of output voltage while no P can not fully achieve soft switching. Here is a balance.

3.3. The influence of D

After simulated different duties on power side and check the results, some points can be concluded as follows:

A lower D (on time is not enough for resonant together) will cause less energy transferred in a period which will cause lower output power and will perform a lower output voltage.

A higher D will damage soft-switching seriously due to deadtime is not enough for current changing between bridges and a short will occur in a bridge which will cause large loss and will perform a very low output voltage.

Lower D makes the system works in a relatively safe environment (enough deadtime for soft switching) but lower D will decrease output voltage which is not suit for high output power at the same load condition(same current source as load). Here is a balance.

3.4. Simulated influences of FPD

To obtain a set of proper parameters, some basic performances are measured and recorded in table 1. From table 1 and further subtle sweep, we can find a proper point for the power system by balancing the efficiency and output voltage accuracy.

Table 1. The influences of F P and D.

| Variation from typical FPD | Efficiency (%) | Vo(ave) (V) | Variation from typical FPD | Efficiency (%) | Vo(ave) (V) |
|---------------------------|----------------|-------------|---------------------------|----------------|-------------|
| F=340kHz                  | 98.488         | 11.883      | P=0.7%                    | 98.432         | 11.893      |
| F=345kHz                  | 98.908         | 11.975      | P=1.0%                    | 97.988         | 11.875      |
| F=350kHz                  | 98.947         | 11.907      | D=40%                     | 97.792         | 11.860      |
| P=0.1%                    | 98.941         | 11.939      | D=45%                     | 98.609         | 11.927      |
| P=0.2%                    | 98.917         | 11.935      | D=47%                     | 98.849         | 11.938      |
| P=0.5%                    | 98.640         | 11.907      | D=49%                     | 98.759         | 11.940      |

When typical FPD with no variation F=348kHz, P=0, D=48% applied, efficiency=98.947% Vo(ave)=11.941V

4. FDP controlling method and verification

As analyzed before, F D P and be designed self-adapting respectively or combined based on different variation features. A simple control of adjustable D for load variation with F P settled is proposed here to illustrate a possible method for achieving the whole system.
Figure 8 shows a whole system schematic in Cadence. In figure 8, most of power stage still remain but 8 ideal gate drivers are replaced by the output of control stage. The main loop of the control stage is detecting Vo and control driving signals to make Vo keeps around desired value. When controlling D, the internal control concept is similar to PWM that comparing carrying wave and modulated wave to get switching driving signals. Here the control loop includes error amplifier(EA), EA window, threshold regulator for comparator, comparator for modulating, delay block, and analog adder for driving in sequence. The key point of this loop is the comparator for modulating that takes carrying wave from voltage controlled oscillator (VCO) that desired for adjusting F when required as input and adjusted EA wave as threshold, and this comparator outputs fundamental driving signals reserved for next delay and driving block. [6] Here inherent frequency=350kHz F=34kHz and P=0.35% and self-adapting D are applied, the simulated results are shown in figure 9. From figure 9, it can be observed that when load varies in a wide range, Vo can be adjusting to around 12V automatically.

![Figure 8. The whole system structure.](image)

All analyses above are based on buck mode for simple illustration. For such a bidirectional converter, there are two same but opposite direction control loop in controller IC design actually. When converted to boost mode by external indicating signal, opposite direction control loop will be activated and this loop deactivated. The simulated results of boost mode are shown in figure 10 that also verifies the whole system.

![Figure 9. Simulated Vo(cc_Vout) and load current set(I343/PLUS).](image)  
![Figure 10. Simulated Vo(do_Vout) and load current set(I346/PLUS) in boost mode.](image)

5. Conclusion
This paper introduces the background and prospect of high power bidirectional 48V-12V DCDC converter in electric vehicles. To satisfy the requirements of this application, CLLC and DAB with full bridge and half bridge are existing alternatives for this project and full-bridge CLLC is finally chosen. Full-bridge CLLC transfers energy from power side to load side with different arms in two halves of one period. Based on requirements of the converter and the working principle, proper devices can be chosen. Then resonant devices L1, L2, C1, and C2 determine the inherent frequency and quality factor.
When operating frequency is a little less than inherent frequency, there will be a small extra time with no power transfer for achieving soft switching. Besides, quality factor that is related to resonant components and output impedance and minimum dead time that is related to output capacitors of power MOSFETs should be properly chosen for normal working and soft switching.

FDP have influences on two important performances of power system that are output voltage accuracy and conversion efficiency respectively. For F, there is a balance between soft switching margin and conduction loss; For P, there is a balance between switching loss and output voltage accuracy; For D, there is a balance between output voltage accuracy and system safety that is induced by deadtime. FPD in a proper range achieves almost over 98% efficiency (highest 98.947%) and over 98.83% output voltage accuracy (highest 99.79%).

FDP can be designed self-adapting or adjustable respectively. A simple control loop for settled F P and adjustable D is organized similar to traditional PWM structure and is verified workable under load variation from 0 to full load 1kW. The whole system is also verified workable at boost mode (the other power transfer direction).

6. References

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