Effect of CNTs Parameter Variation on the Performance of Analog Device

Shailendra K. Tripathi

Abstract: Carbon nanotubes (CNTs) have emerged as a prominent material for present day nano-scale systems design. In spite of their widespread use in biology, and nano-electro mechanical systems (NEMS), CNTs have encroached upon conventional MOSFETs for the design of low power and high speed circuits. Because CNT possesses higher current carrying capability, higher transconductance and near ballistic transport of charge carrier, they are added because of carbon nanotube (CNT). The diameter of the CNTs used in the CNFETs. HSPICE simulations performed on a 0.9V; 32nm CNFET-based ICC-II are included to exemplify the dependencies studied.

Keywords: Analog Circuits, Nano-electronics, CNFET, CMOS

I. INTRODUCTION

The present trends and overall needs for ICs are low power supply, high packaging density, and low power consumption. The accuracy for signal processing is another requirement in various applications [1-2]. From the last thirty years, the electronic industry has achieved a notable scaling of transistor sizes with the number of devices (transistors) on an integrated circuit approximately raising double in every 18–24 months [3]. Moreover, it is being projected that processing technology based on Silicon will reach to its capacity with channel length of MOSFETs around sub-10 nm. As the channel length lines sub-10 nm regime, secondary effects and tunneling occur, which stop further scaling of MOSFET device [4]. On account of this, the electronic industry is putting efforts for alternate materials and technology to amalgamate with current MOSFET-based fabrication techniques. The technologies beyond-CMOS like as CNFET [5], Tunnel-FET and Single Electron Transistor (SET) [6], are came into the picture. Among above technologies, the CNFET is the most protuberant due to its superior features which are added because of carbon nanotube (CNT). The CNTs have near ballistic transport of charge carrier and alterable band gap, which make them a superior channel material for low power and high-speed futuristic electronics [7].

II. THEORETICAL BACKGROUND OF CNFET

A carbon nanotube contains two arrangements, (i) Single-walled carbon nanotube (SWCNT) and (ii) Multi-walled carbon nanotube (MWCNT) as presented in Figure 2. SWCNTs are basically the rolled sheets of Graphene. The diameter of SWCNTs is 1 nm - 2 nm and length around 0.2 μm – 5 μm. The MWCNTs look like as a coaxial cable with the assemblage of SWCNTs. The diameter of MWCNTs fluctuates from 2-25 nm, and inter-layer space is around 0.36 nm [10], [11].

Further, as chiral vector m ≠ n and chiral angle lies between 0 and 30 °, CNT is known chiral, as illustrated in Figure 3.

Revised Manuscript Received on October 20, 2020.

* Correspondence Author
Shailendra K. Tripathi*, Department of ECE, Sharda University, Greater Noida, India. Email: Shailendra.tripathi@sharda.ac.in

International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-9 Issue-4, November 2020

doi:10.35940/ijrte.F7990038620

Retrieval Number: 100.1/ijrte.F7990.119420

237 Published By: Blue Eyes Intelligence Engineering and Sciences Publication
The circuits based on CNTs possess fewer leakages current and improved switching. The construction of a CNFET is alike to MOS transistor excluding the SWNTs play as the device channel region. The metal contacts fabricated on either end of the SWNTs work for the source and drain. CNFET shows merits over conventional MOSFET, such as decrease in carrier tunneling and short-channel effects improved current density, greater carrier velocity and decreased leakage currents. Moreover, the drain current of transistor is shown by (1) and it is contingent upon charge mobile densities (ξS & ξD) which are represented in (2) and (3).

\[ I_D = \frac{4qkT}{h} \left[ \ln(1 + \exp(\xi_S)) \ln(1 + \exp(\xi_D)) \right] \]  
(1)

\[ \xi_S = \frac{(\Phi_S - \delta_1)}{V_T} \]  
(2)

\[ \xi_D = \frac{(\Phi_S - \delta_1 - V_{DS})}{V_T} \]  
(3)

Further, the mobile charge densities of CNFET are connected to surface potential (\(\Phi_S\)) and thermal voltage (\(V_T\)) as illustrated in (4). Additionally, the CNT diameter (d), thickness of oxide (t_OX), and capacitance of oxide (C_OX) of CNFET are related by (6) with some constants parameters [12]. The relation of threshold voltage is given in (6). Moreover, \(\delta_1\) is known as equilibrium sub-band minima of first sub-band (E_G = 2). The terms q, k, T and h represent electron charge, Boltzmann’s constant, absolute temperature and Planck’s constant accordingly [13].

\[ \Phi_S = \frac{V_{GS} - qN_{mobile}}{C_{OX}} \]  
(4)

\[ C_{OX} = \frac{2\pi \varepsilon_0 \varepsilon_{OX}}{\ln(2t_{OX}/d) + 1} \]  
(5)

\[ V_T = \frac{kT}{q} \]  
(6)

III. CNFET-BASED INVERTING CURRENT CONVENER-II

The circuits with current-mode (CM) approach have gained noteworthy consideration because of their aids weighed against voltage-mode (VM) circuits in terms of wider bandwidth, higher linearity, enhanced dynamic range and reduced power consumption [14-17]. Further, CM circuits are appropriate for integration with CMOS process technology [17], [18]. The ICC-II was presented by Soliman et.al, to implement the CM circuits from the VM circuits [19], [20]. The block diagram of ICC-II is given in Figure 4. The port equations of inverting current conveyor are shown in (7). This is very versatile active device and also implemented with CNFET [24].

![Symbol of ICC-II](image)

**Fig. 4: Symbol of ICC-II**

The CMOS technology has many performance concerns which can be answered by recently emerging CNFET technology [5], [12], [13]. The CMOS realization of ICC-II has been presented in the literature [23], [25]. Transistor level implementation of Current Conveyor based on CNFET is presented in Figure 5. The design uses HSPICE 32 nm parameters, developed by Stanford [21]. The important model parameters are illustrated in Table 1.

![Implementation of ICC-II with one Z+ and one Z- output](image)

**Fig. 5: Implementation of ICC-II with one Z+ and one Z- output [15]**
In subsequent section, the effects of diameter alteration on the performance of device have been tested taking some other parameters in the design. The results would discover the various favorable effects for the CNT-based circuit design in coming future.

\[
\begin{bmatrix}
I_y \\
V_x \\
I_{zz}
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 \\
-1 & 0 & 0 \\
0 & \pm 1 & 0
\end{bmatrix}
\begin{bmatrix}
V_y \\
I_x \\
V_z
\end{bmatrix}
\]  (7)

\[W = (N-1)*S + D_{CNT} \]  (11)

The diameter of the carbon nanotube is a physical property that closely depends on the indices of Graphene lattice (n, m) given in (8). The single-walled CNT is obtained from the Graphene layer and its diameter has the great impact on the threshold voltage and band gap of the device as shown in (9) and (10). It is important to know that the modification of band gap in MOS transistor is critical but in CNFET, it can be easily controlled by diameter of the nanotube. The width of transistor also depends on the diameter of CNT [22]. The extensive simulations have been carried out to test the properties of current conveyor block.

(i) Variation in the Number of Tubes

The diameter of CNT affects various parameters of CNFET, and it is considered further the effect of the change in the diameter of CNT on the performance of CNFET-based inverting current conveyor. Results show that frequency response of the device is improved by increasing the diameter as illustrated in Figure 7. It is also attempted to see the effect of variation in the number of tubes with the 3-dB bandwidth of the device.

\[D_{CNT} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \]  (8)

\[\sum g = \frac{0.84eV}{D_{CNT}} \]  (9)

\[V_{th} = \frac{aV_x}{qD_{CNT} \sqrt{3}} \]  (10)

TABLE 1: CNFET DESIGN PARAMETERS

| S.N. | Parameters          | Value |
|------|---------------------|-------|
| 1    | Oxide Thickness (Tox)| 4 nm  |
| 2    | Dielectric Constant (Kox) | 16 |
| 3    | Power Supply        | ±0.9 V|
| 4    | CNT’s Chirality (n, m)| 19, 0 |
| 5    | Physical channel length (Lch) | 32 nm |
| 6    | No. of tubes in the device | 6 |
| 7    | Pitch (S)           | 14 nm |

IV. OPTIMIZATION OF CNT DIAMETER

The CNT parameters like diameter (D_{CNT}), threshold voltage (V_{th}) etc. have been measured in the design of CNFET-based devices. The useful relations are illustrated in equations (8), (9), (11).

Also, CNFET’s width (W), number tubes (N), pitch (S) are given in (11) and presented in Figure 6. The n and m are the indices’s of Graphene lattice and a = 2.49 Å (constant). Additionally, electronic charge is represented by q and V = 3.033 eV, is the Carbon’s π- π bond energy.
Effect of CNTs Parameter Variation on the Performance of Analog Device

(ii) Variation in Power Supply

An attractive feature of CNFET that it can operate at much scaled power supply voltages. The effect of power supply variation in the performance of ICC-II is explored in the proposed work. The scaled supply voltages have more effect of parasitics and so on the performance [25]. Figure 10 depicts that 3-dB voltage bandwidth reducing with scaled power supply voltages. Although, the scaled voltages have the pessimistic effect on frequency response yet it reduces the average power of the device that is needed for present low power circuit design. The similar effort has been repeated for current-mode design.

Fig. 8: CNT Diameter versus 3-dB Current Bandwidth with the Number of CNT

Fig. 9: CNT Diameter versus Average Power with the Number of CNT

Fig. 10: CNT Diameter versus 3-dB Voltage Bandwidth

Fig. 11: CNT Diameter versus 3-dB Current Bandwidth

Figure 12 represents the effect of power supply scaling on the average power requirement of the device (CNFET). The other design parameters like inter-CNT pitch (S), number of CNT (N), oxide thickness (T_{OX}), dielectric constant (K_{OX}) have been referred from Table 1. Finally, it is important to discuss the advantages of current-mode circuits over voltage-mode counterparts. They have inherently wide bandwidth, greater linearity, wide dynamic range and simple circuitry.

V. CONCLUDING REMARKS

In this paper, the advantages of carbon nanotube and transistor based on CNT have been discussed. This work investigated the effect of CNT diameter variation in the performance of analog building block. The bandwidth of above 100 GHz is achieved with the CNFET-based design which is far away from CMOS design. In this paper optimization of the number of tubes and power supply voltages express a wide significance for the CNFET-based low power circuit design which can solve the challenges of current nano-electronics. In addition to this, features of CM circuits are emphasized over VM circuits in the design. The results included in the paper are expected to act as guidelines for practicing electronics designers to decide the most optimum value of the diameter of CNTs for a particular design. The performance depicts that CNFET can be a suitable alternate option for present MOSFET technology.
REFERENCES

1. Maheshwari, Sudhanshu. "Analogue signal processing applications using a new circuit topology." IET circuits, devices & systems 3, no. 3 (2009): 106-115.

2. Kuhn, K. J. "Considerations for ultimate CMOS scaling." IEEE Trans. Electron Devices 59, no. 7 (2012): 1813-1828.

3. Patil, Nishant, Albert Lin, Edward R. Myers, Koungmin Ryu, Alexander Badmaev, Chongwu Zhou, H-S. Philip Wong, and Subhasish Mitra. "Wafer-scale growth and transfer of aligned single-walled carbon nanotubes." IEEE Transactions on Nanotechnology 4, no. 4 (2005): 498-504.

4. Kuhn, Kiel J. "CMOS scaling for the 22nm node and beyond: Device physics and technology." In Proceedings of 2011 International Symposium on VLSI Technology, Systems and Applications. (2011).

5. Deng, Jie, and H-S. Philip Wong. "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region." IEEE Transactions on Electron Devices 54, no. 12 (2007): 3186-3194.

6. Asra, Ram, Mayank Shrivastava, Kota VRM Murali, Rajan K. Pandey, Harald Gossner, and V. Ramgopal Rao. "A tunnel fet for scaling below 0.6 V with a cmos-comparable performance." IEEE Transactions on Electron Devices 58, no. 7 (2011): 1855-1863.

7. Low, Chong Guan, and Qing Zhang. "From Bulk TFETs to CNT-TFETs: Status and Trends." Carbon Nanotubes and Their Applications (2012): 221.

8. Zhuang, Hao, Frank He, Xinmin Lin, Lining Zhang, Jian Zhang, Xufang Zhang, and Mansun Chan. "A Web-Based Platform for Nanoscale Non-Classical Device Modeling and Circuit Performance Simulation." In Web Information Systems and Mining, 2009. WISM'09. International Conference on, IEEE, (2009): pp. 371-375.

9. Patil, Nishant, Jie Deng, Subhasish Mitra, and H-S. Philip Wong. "Circuit-level performance benchmarking and scalability analysis of carbon nanotube transistor circuits." IEEE Transactions on Nanotechnology 8, no. 1 (2009): 37-45.

10. Javey, Ali, Jing Guo, Qian Wang, Mark Lundstrom, and Hongjie Dai. "Ballistic carbon nanotube field-effect transistors," nature 424, no. 6949 (2003): 654-657.

11. Kang, Seong Jun, Coskun Kocabas, Taner Ozel, Moonsub Shim, Nainad Pimparkar, Muhammad A. Alam, Slava V. Rotkin, and John A. Rogers. "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes." Nature nanotechnology 2, no. 4 (2007): 230-236.

12. Fedawy, Mostafa, Wael Fikry, Adel Alhenawy, and Hazem Hassan. "IV characteristics model for ballistic Single Wall Carbon Nanotube Field Effect Transistors(SW-CNTFET)." In Electronics Design, Systems and Applications (ICEDSA), IEEE International Conference on, (2012): pp. 10-13.

13. Imam, Ale, Mohd Hasan, Aminul Islam, and Shuja Ahmed Abbasi. "Optimized design of a 32-nm CNFET-based low-power ultra wideband CCII." IEEE Transactions on Nanotechnology 11, no. 6 (2012): 1100-1109.

14. Sedra, A. S., Gordon W. Roberts, and F. Gohh. "The current conveyor: history, progress and new results." In IEE proceedings, vol. 137, no. 2 Pt. G, pp. (1990): 78-87.

15. Maheshwari, Sudhanshu, Jitendra Mohan, and Durg Singh Chauhan. "High input impedance voltage-mode universal filter and quadrature oscillator." Journal of Circuits, Systems, and Computers 19, no. 07 (2010): 1597-1607.

16. Yamacli, Serhan, Sadri Ozcan, and Hakan Kuntman. "A novel active circuit building block: Electronically tunable differential difference current conveyor (edcc) and its application to ken filter design." In 2006 International Conference on Applied Electronics. (2006) Minaei, Shahram, and Erkan Yuce. "A new full-wave rectifier circuit employing single dual-X current conveyor." International Journal of Electronics 95, no. 8 (2008): 777-784.

17. Laxminidhi, Tonse, and Shanthi Pavan. "Efficient design centering of high-frequency integrated continuous-time filters." IEEE Transactions on Circuits and Systems I: Regular Papers 54, no. 7 (2007): 1481-1488.

18. Sohby, Ehab Ahmed, and Ahmed M. Soliman. "Novel CMOS realizations of the inverting second-generation current conveyor and applications." Analog Integrated Circuits and Signal Processing 52, no. 1-2 (2007): 57-64.

19. Sohby, Ehab A., and Ahmed M. Soliman. "Realizations of fully differential voltage second generation current conveyor with an application." International Journal of Circuit Theory and Applications 38, no. 5 (2010): 441-452.

20. Deng, Jie, and H-S. Philip Wong. "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region." IEEE Transactions on Electron Devices 54, no. 12 (2007): 3186-3194.

21. Marani, Roberto, Gennaro Gelaio, and Anna Gina Perri. "Modelling of Carbon Nanotube Field Effect Transistors oriented to SPICE software for A/D circuit design." Microelectronics Journal 44, no. 1 (2013): 33-38.

22. Usmani, Fahad Ali, and Mohammad Hasan. "Carbon nanotube field effect transistors for high performance analog applications: An optimum design approach." Microelectronics Journal 41, no. 7 (2010): 395-402.

23. Bandaru, Prabhakar R. "Electrical properties and applications of carbon nanotube structures." Journal of nanoscience and nanotechnology 7, no. 4-5 (2007): 1239-1267.

24. Tan, Michael Loong Peng, and Georgios Lentaris. "Device and circuit-level performance of carbon nanotube field-effect transistor with "benchmarking against a nano-MOSFET." Nanoscale research letters 7, no. 1 (2012): 1-10.

25. Hayat, Khizar, Hammad M. Cheema, and Atif Shamim. "Potential of carbon nanotube field effect transistors for analogue circuits." The Journal of Engineering (2013).

26. Tripathi, S. K., and Mohd Samar Ansari. "Tunable Active Biquad Filter in±0.9 V 32 nm CNFET." In Electronic System Design (ISED), 2014 Fifth International Symposium on, pp. 63-67. IEEE, 2014.

27. Kanoun, Olfa, Christian Müller, Abderrahmane Benchirouf, Abdulkadir Sanli, Trong Nghia Dinh, Ammar Al-Hamry, Lei Bu, Carina Gerlach, and Ayda Bouhamed. "Flexible carbon nanotube films for high performance strain sensors." Sensors 14, no. 6 (2014): 10042-10071. https://nanotechnologieblog.wordpress.com/carbon-nanotubes/

28. http://yzhang.sjtu.edu.cn/en/research.asp?id=7

AUTHORS PROFILE

Dr. Shailendra Kumar Tripathi has completed M.Tech., in Electronics Engineering from Aligarh Muslim University, Aligarh, India, in 2008. He has completed Ph.D from the Department of Electronics & Communication Engineering, Malaviya National Institute of Technology, Jaipur, India in 2019. Presently, he is working as Assistant Professor in the department of Electronics & Communication Engineering, Sharda University, Gautam Buddha Nagar, India. His research interests are analog signal processing, nanoelectronic circuits and VLSI Design. He has published ten research papers in reputed national/international journals and conferences. He has contributed one book & two book chapters.