GE-SpMM: General-purpose Sparse Matrix-Matrix Multiplication on GPUs for Graph Neural Networks

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Abstract—Graph Neural Networks (GNNs) based graph learning algorithms have achieved significant improvements in various domains. Sparse Matrix-Matrix multiplication (SpMM) is a fundamental operator in GNNs, which performs a multiplication operation between a sparse matrix and a dense matrix. Accelerating SpMM on parallel hardware like GPUs can face the following challenges: From the GNN application perspective, the compatibility needs to be considered. General GNN algorithms require SpMM-like operations (e.g., pooling) between matrices, which are not supported in current high-performance GPU libraries (e.g., Nvidia cuSPARSE [1]). Moreover, the sophisticated preprocessing in previous implementations will lead to heavy data format conversion overheads in GNN frameworks. From the GPU hardware perspective, optimizations in SpMV (Sparse Matrix-Vector) designs on GPUs do not apply well to SpMM. SpMM exposes the column-wise parallelism in the dense output matrix, but straightforward generalization from SpMV leads to inefficient, uncoalesced access to the GPU global memory. Moreover, the sparse row data can be reused among GPU threads, which is neither possible in SpMM designs inherited from SpMV.

To tackle these challenges, we propose GE-SpMM: GE-SpMM performs SpMM-like operation on sparse matrices represented in the most common Compressed Sparse Row (CSR) format. Thus, GE-SpMM can be efficiently embedded in GNN frameworks with no preprocessing overheads and support general GNN algorithms. We introduce the Coalesced Row Caching method to process columns in parallel and ensure efficient coalesced access to the GPU global memory. We also present the Coarse-grained Warp Merging method to reduce redundant data loading among GPU warps. Experiments on a real-world graph dataset show that GE-SpMM achieves up to 1.41× speedup over Nvidia cuSPARSE [1] and up to 1.81× over GraphBLAST [2]. We also embed GE-SpMM in GNN frameworks and get up to 3.67× speedup over popular GNN models like GCN [3] and GraphSAGE [4].

I. INTRODUCTION

Machine learning algorithms on graphs, especially the recently proposed Graph Neural Networks (GNNs), have been successfully applied to tasks such as link prediction and node classification [3]–[8]. Acceleration of GNN systems is crucial to solving real-world problems because of days of execution time (e.g., it takes up to 78 hours to train a GNN model with 7.5 billion edges on 16 GPUs [9]). In GNN algorithms, data are organized in the graph structure composed of vertices (nodes) and edges (links). Each vertex in the graph is associated with a feature vector, and these feature vectors are propagated through edges to perform GNN algorithms. Thus, aggregating the feature vectors of neighbor vertices is a fundamental operation in GNNs, which can be expressed with Equation (1).

$$\vec{f}_u = \text{reduce}_\text{op}(\{\vec{f}_v\}, \exists \text{edge}_v \rightarrow u) \quad (1)$$

In Equation (1), $\vec{f}_u$ represents the feature vector of a vertex $u$ in the graph, while $\{\vec{f}_v\}$ denotes the collection of feature vectors of $u$’s in-edge neighbors. The $\text{reduce}_\text{op}$ is the aggregation operation to generate a new feature vector of $u$, which varies in different GNN algorithms [3], [4]. The edges between vertices in natural graphs are usually sparse, and the graph structure can be represented using a sparse adjacency matrix. Fig. [1] shows that the aggregation operation on the graph can be treated as a customized multiplication between the sparse adjacency matrix (representing the graph) and dense feature matrix (representing feature vectors of vertices). When the $\text{reduce}_\text{op}$ in Equation (1) is taking sum, the operation between the adjacency matrix and the feature matrix is a standard Sparse Matrix-Matrix Multiplication (SpMM). When a customized $\text{reduce}_\text{op}$ is adopted (e.g., pooling), we call it a general SpMM-like operation.

Being a primary operation in GNN models, SpMM is also a time-consuming step even on parallel hardware like GPUs. We profile the percentage of SpMM operation during a GCN training procedure. In GCN training, the forward and backward of graph convolution layers both involve SpMM. As listed in Table [1] SpMM operations take $\sim 30\%$ of the total time in the example code provided by DGL [11] with default settings. Dense matrix multiplications take $\sim 10\%$, and the rest of the operators all take less than 10%. Thus,

1 The project is open-sourced at https://github.com/hgyhungry/ge-spmm

2 Percentage of CUDA time, reported by PyTorch [10] autograd profiler.
accelerating SpMM operations in GNN frameworks is significant for improving performance. However, current SpMM acceleration solutions on GPUs still face challenges from 1) meeting GNN application requirements, and 2) full utilization of global memory bandwidth of the GPU hardware.

From the GNN application perspective, embedding SpMM designs in GNN frameworks has at least two requirements: support for general SpMM-like operators (rather than the standard SpMM), and no (or very low) data format conversion overhead in the whole framework. In terms of general SpMM-like operators, existing GNN frameworks cannot achieve as good performance as using standard SpMM in cuSPARSE library. Current SpMM researches claiming better performance than cuSPARSE rely on preprocessing sparse matrix and cannot be conveniently adopted. Existing GNN systems like DGL relies on Nvidia cuSPARSE to perform standard SpMM, but falls back to its own implementation for SpMM-like operations because they are not provided in cuSPARSE. Table I shows the comparison of the same aggregation step in two models: GraphSAGE-GCN, which internally calls SpMM, and GraphSAGE-pool, which internally calls SpMM-like. We again use example codes provided by DGL with default parameters. The results show that current implementation of SpMM-like in DGL cannot compete with the performance of cuSPARSE. On the other hand, although recent studies on SpMM in high-performance computing fields achieve even better performance than cuSPARSE, they cannot be directly adopted by GNN frameworks. These implementations require preprocessing on input sparse matrix, which is hard to be integrated into GNN frameworks. Also, the extra time spent on preprocessing cannot be compensated by SpMM performance gain if SpMM is performed only a few times in GNNs, as is the case in GNN direct inference or batched training.

From the GPU hardware perspective, SpMM exposes column-wise parallelism in output dense matrix, which does not exist in the widely-studied Sparse Matrix-Vector Product (SpMV). A straightforward generalization by adding parallel threads along the column dimension can result in uncoalesced access patterns to sparse matrix data, as shown in Fig. 2. Uncoalesced access pattern has been proved to be inefficient on GPUs. Thereby, SpMM kernel needs to be carefully designed to enable a coalesced access pattern for data loading. On the other hand, reusing sparse matrix data is crucial for SpMM, while this issue does not rise for SpMV. In real applications, the column dimension of the dense matrix can be up to 512, in which case the amount of memory transactions is substantial. Fig. 3 shows the profiling of SpMM kernel in cuSPARSE. We use as input sparse matrix a synthetic random matrix of 65K rows and 650K non-zeros, detailed in Section IV-B, and test a range of column numbers (\(N\) in Table III) in the dense matrix. The two metrics are 1) number of global load transactions (in the unit of 32bytes), and 2) global load throughput (in the unit of GB/s), both reported by Nvidia nvprof. The GPU we use has a maximum global bandwidth of 484GB/s. Fig. 3 shows that the total number of memory transactions linearly grows with \(N\), but the kernel reaches near maximum bandwidth throughput after \(N\) reaches 32. From the test we can observe that, unlike SpMV which is typically bounded by low bandwidth utilization, SpMM can easily achieve a high utilization but suffers from too much data movement. Thereby, SpMM design requires a data-reuse mechanism to reduce redundant data transactions.

In this paper, we present GE-SpMM (an acronym for General-purpose SpMM), a customized CSR-based (Compressed Sparse Row) SpMM design that tackles all these challenges. We summarize our contributions as follows:

- We present GE-SpMM, an efficient CSR-based SpMM-like kernel on GPUs to accelerate GNN workloads. GE-SpMM can be integrated into existing GNN frameworks with no data conversion overhead for various GNN algorithms.
- We introduce the Coalesced Row Caching (CRC) method for SpMM, which uses GPU shared memory to cache sparse matrix rows. This method enables coalesced memory access to both sparse and dense matrix, leading to a more efficient utilization of bandwidth. The average

### Table I

| Graph  | SpMM percentage |
|--------|-----------------|
| Cora   | 33.1%           |
| Citeseer | 29.3%      |
| Pubmed | 29.8%           |

### Table II

| Graph   | SpMM-like perf. loss against SpMM in GraphSAGE |
|---------|-----------------------------------------------|
| Cora    | 8.8%                                          |
| Citeseer| 89.2%                                         |
| Pubmed  | 139.1%                                        |

Fig. 2. Differences in data loading in SpMV and its straightforward generalization to SpMM. SpMM exposes more redundant data loading and uncoalesced access pattern.

Fig. 3. Profiling of csrmm2 in cuSPARSE. The loading throughput approaches upper bound when \(N\) ≥ 32 but memory transactions keep growing linearly.
improvement by adopting this method can be up to 1.25×.

- We introduce the Coarse-grained Warp Merging (CWM) method for SpMM, which reuses loaded sparse matrix by merging the workload of different warps. This technique reduces the amount of memory transactions and improves instruction-level parallelism. The average speedup by adopting this method can be up to 1.51×.

- We conduct extensive experiments on GE-SpMM on real-world graphs [18], [19]. GE-SpMM achieves up to 1.41× speedup over Nvidia cuSPARSE [1] and up to 1.81× over GraphBLAST [2]. We also embed GE-SpMM in GNN frameworks and get up to 3.67× CUDA time reduction on popular GNN models like GCN [3] and GraphSAGE [4].

The rest of this paper is organized as follows. Background information is introduced in Section II. The designs and optimizations of GE-SpMM will then be detailed in Section III, followed by the method to embed GE-SpMM in GNN frameworks. Our experimental setup and results will be presented in Section IV. The paper is concluded in Section VI.

II. BACKGROUNDS AND RELATED WORKS

In this section, we introduce background information about both SpMM and GNNs on GPUs. The notations used in this paper are shown in Table III.

| Notation | Description |
|----------|-------------|
| A        | Sparse input matrix with dimension $M \times K$ |
| B        | Dense input matrix with dimension $K \times N$ |
| C        | Dense output matrix with dimension $M \times N$ |
| M        | Number of rows in A. |
| K        | Number of columns in A, equal to M in graph problems. |
| N        | Number of columns in B. |
| nnz      | Number of non-zero elements in A. |

A. GPU Preliminaries

We use Nvidia GPUs with CUDA [12] as the programming interface in this paper. GPU is a highly parallel architecture composed of many streaming multiprocessors (SMs). An SM executes threads in a SIMT (Single Instruction Multiple Threads) fashion, and a bunch of 32 threads called a warp run simultaneously. The warp is transparent in CUDA programming model. Instead, users define a bunch of parallel blocks and assign each block with a certain number of threads. In CUDA programming model, each block owns a shared memory, which is more efficient to access than the global memory (accessible to all blocks). Shared memory can be used for data reusing for different threads in order to reduce data transactions from the global memory.

Organizing threads into warps also have effects on the memory access pattern. GPU always try to merge the memory request from a warp into as few transactions as possible. From the program perspective, it is recommended in technical materials [12], [15] to make a warp of threads access consecutive, aligned memory in one SIMT instruction. This technique is called coalesced memory access.

B. SpMM on GPUs

Because the dense matrix in the SpMM problem can be treated as a vector of vectors, a straight forward SpMM implementation is simply to perform SpMV for multiple times sequentially, as can be done in [20]. This method clearly does not exploit parallelism along the output column dimension. SpMV design in [17] uses a GPU warp to process a row in the sparse matrix, and previous SpMM design in GraphBLAST [2] inherits this method so that multiple threads can work on one output row in parallel. For intra-warp data reuse, it uses a warp-level intrinsic (___shfl) to broadcast fetched data to other threads within the same warp. However, GraphBLAST fails to consider reusing the sparse row data among different warps and still has room for improvement. Nvidia cuSPARSE library [1] also provides a high-performance (not open-source) SpMM kernel (csrmv2), but general SpMM-like operations in GNN applications are not supported in cuSPARSE.

There are also other researches on high-performance SpMM kernels that perform better than cuSPARSE. Unlike GraphBLAST [2] which takes Compressed Sparse Row (CSR) format as input, these works require preprocess on input sparse matrix to form a new sparse format specially for SpMM, such as ELLPACK-R in FastSpmm [21], and sparse formats used by RS-SpMM [13] and ASPM [14]. But they are not practical for GNN frameworks to adopt. These non-standard formats lead to extra memory space and difficulties in software maintenance. Moreover, preprocess time can be up to 5× actual SpMM computation time [13], [14]. Although this cost can be tolerated in iterative algorithms, GNN applications sometimes demand running SpMM only a few times for one matrix. One example scenario is GNN inference, where trained models are directly used on new graphs to make predictions, such as predicting properties on new protein graphs [4]. Another is sampled batch training [4], [22], where the sampled subgraphs are different for each batch. For these applications, preprocess cannot be amortized in GNN frameworks since the benefit cannot make up to overhead.

C. Graph Neural Network Frameworks

Many existing systems aim to provide high performance and easy programming abstractions for GNN algorithm developers. Projects like DGL [11] and Pytorch-Geometric (PyG) [23] provide graph APIs on top of deep learning frameworks (e.g., Pytorch [10]). Other systems in the industry [24], [25] and academia [16], [20] also provide programming interfaces and optimizations for GNNs.

As SpMM is a critical operation in many GNN models, DGL and PyG both implement custom SpMM kernel instead of using sparse matrix operators provided by Pytorch.

- DGL internally calls the function, csrmm2 in cuSPARSE [1], to perform SpMM. However, for SpMM-like operations cuSPARSE does not provide corresponding functions, so DGL falls back to its own kernels.
Besides limited support for SpMM-like operations, csrmm2 produces a column-major output. Since in GNNs both input and output of feature matrix need to be row-major, DGL calls a matrix transpose from cuBLAS\cite{26} to transform the layout.

PyG uses another abstraction called MessagePassing to represent graph propagation in GNN models. Message-passing first generates message on all edges explicitly and then reduce them, while SpMM can fuse these two stages into one kernel. The consideration of MessagePassing is to allow more flexible user-defined operation, but with generality it loses the room for improving the performance of specific operations like SpMM.

Some aforementioned researches on fast SpMM design require preprocessing\cite{3}.\cite{14}. CuSPARSE\cite{1} has limited support for SpMM-like operation\cite{1}. Other SpMM designs inherited from SpMV fail to consider the column-wise parallelism or sparse matrix data reuse, which may lead to inefficiency when implemented on GPUs. These will further hinder the performance of both SpMM and GNNs.

### III. GE-SPMM DESIGN

In Section\cite{1} we observe from experiments that SpMM can be memory-bounded, so it is crucial to load data in a more efficient way and reduce total memory transactions. In this section, we propose Coalesced Row Caching (CRC) and Coarse-grained Warp Merging (CWM) methods to achieve these goals.

#### A. Data Organization in GE-SpMM

In order to meet the requirement of compatibility to GNN frameworks with low preprocess overheads, an universal data format for both SpMM and other sparse matrix operations is required. The Compress Sparse Row (CSR) format is a widely-used format in vendor libraries (e.g., Nvidia cuSPARSE\cite{1}), data science toolkit (e.g., SciPy\cite{27}), and GNN frameworks\cite{1},\cite{20}. As shown in Fig. 4, a sparse matrix is stored by three arrays using the CSR format: rowPtr, colInd, val. The column indices and values of non-zeros are first packed along the column and then stored in the order of their row indices. rowPtr stores the offset of first element of each row in colInd.

The data structure of CSR format determines the procedure of SpMM. The computation of each output $C[i,j]$, which is dot-product of sparse row $i$ of $A$ and dense column $j$ of $B$, begins with accessing $A.rowPtr$ for the offset of row $i$. Then the program needs to traverse a segment of $A.colInd$ and $A.val$ array to acquire the non-zeros in sparse row $i$. For each non-zero element, the program needs to use the column index got from $A.colInd$ to locate a specific row in dense matrix $B$. If the column index gives $k$, the program then loads $B[k,j]$, multiply it with the sparse element value from $A.val$ and add to final result. When all non-zeros in sparse row $i$ is consumed, the final result of $C[i,j]$ is returned. Algorithm\cite{1} shows this procedure with pseudo code.

#### B. Coalesced Row Caching

When trying to map Algorithms\cite{1} on parallel architectures like GPU, a simple way is to parallelize for-loop in line 1 and 2 since there exists no dependency among each iteration of the loop. For-loop at line 4 in Algorithm\cite{1} has variable loop bound decided at runtime and involves adding to one same

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**Algorithm 1** A simple parallel CSR-based SpMM

Input: A.rowPtr[], A.colInd[], A.val[], B[]
Output: C[]

1: for i = 0 to $M-1$ in parallel do
2: for j = 0 to $N-1$ in parallel do
3: result = 0
4: for ptr = A.rowPtr[i] to A.rowPtr[i+1] do
5: k = A.colInd[ptr]
6: result += A.val[ptr] * B[k,j]
7: end for
8: C[i,j] = result
9: end for
10: end for

**Algorithm 2** SpMM with CRC

Input: A.rowPtr[], A.colInd[], A.val[], B[]
Output: C[]

1: i = tb_id
2: j = tid
3: lane_id = tid % warp_size
4: sm_base = tid - lane_id
5: row_start = A.rowPtr[i]
6: row_end = A.rowPtr[i+1]
7: result = 0
8: for ptr = row_start to row_end-1 step warp_size do
9: /*load A.colInd and A.val with tile warp size*/
10: if ptr+lane_id<row_end then
11: sm_k[tid]=A.colInd[ptr+lane_id]
12: sm_v[tid]=A.val[ptr+lane_id]
13: end if
14: __syncwarp()
15: /*consume the loaded elements*/
16: for kk = 0 to warp_size do
17: if ptr+kk<row_end then
18: k = sm_k[sm_base+kk]
19: result += sm_v[sm_base+kk] * B[k,j]
20: end if
21: end for
22: end for
23: C[i,j] = result
variable, so it cannot be parallelized. As introduced in section II-A, coalesced memory access can improve bandwidth efficiency, and it requires a warp of threads to access consecutive elements in one instruction.

In Algorithm 1, it is easy to ensure coalesced access to dense matrix $B$ (the instruction at line 9). When we parallelize loop at line 1 and 2 among threads, we just need to ensure that threads within a warp have same $i$ and contiguous $j$. However, the current algorithm does not present coalesced memory access to any part of the sparse matrix. Since threads within a warp share same $i$, we cannot enable coalesced access to $A.rowPtr$. As to $A.colInd$ and $A.val$, in the current algorithm, the sequential execution of for-loop at line 4 forces threads in the same warp to access the same address (instructions at line 5-6), leading to the broadcast-like pattern in Fig 2. Compared with ideal coalesced access to sparse rows (referring to a segment of $A.colInd$ and $A.val$), the current algorithm is not making full use of data in one memory transaction and issues too many transactions.

Our solution is to partially unroll this sequential for-loop, by a factor of $warp\_size$ (number of threads within a warp, 32 on Nvidia GPUs). During each iteration, a warp of threads first loads a tile of the sparse row $i$ into GPU shared memory. The size of a tile is the same as $warp\_size$, meaning that each thread loads a different element. For now, we assume that the total number of non-zeros in row $i$ is multiples of $warp\_size$, but we will generalize to arbitrary sparse row length later. After loading a tile to shared memory, threads enter an inner for-loop and compute on the loaded data one-by-one, but this time the sparse row data are loaded from shared memory instead of global memory.

A pseudo-code of our method is listed in Algorithm 2. Basically, our method uses a two-phase strategy to load and compute on sparse rows, as shown in Fig. 5. In the first phase, a warp loads a tile of a sparse row into shared memory to enable coalesced loading of a sparse row. In the second phase, a warp sequentially consumes the previously loaded elements. This is to ensure that a warp always accesses the same row in the dense matrix. When the number of non-zeros in sparse row exceeds a tile, the two-phase procedure continues until all non-zeros are consumed. It is not hard to deal with arbitrary row length. Each thread has a copy of row length, and always checks if the bound is exceeded before loading from a sparse row in the first phase (if-condition at line 10). In the second phase, since elements stored in shared memory are consumed sequentially, we simply check with loop bound in every iteration (condition at line 17).

The improvement of this algorithm over Algorithm 1 lies in more efficient global memory loading of sparse rows. Ideally, the total number of load requests to these two arrays can be reduced by a factor of $warp\_size$, because a tile of sparse row is loaded in one coalesced request. In reality, sparse rows are often not perfectly aligned, leading to more than one transaction for a tile. Moreover, many sparse rows have fewer non-zeros than a tile, and the number of load transactions in the Algorithm 1 equals to number of non-zeros. Thus the reduction in load transactions for these short rows is strictly less than $warp\_size$. Despite all these factors, the improved algorithm still achieves an obvious reduction of load transactions and improves the efficiency of global bandwidth, as shown in Section V-B.

C. Coarse-grained Warp Merging

With CRC, we can convert the uncoalesced access to sparse matrix into a more efficient, coalesced way. From the data reuse perspective, the benefit of CRC is to share loaded sparse matrix via GPU shared memory. Although each non-zero element in the sparse matrix can be used to compute an entire row in the output, our CRC method only makes loaded elements shared by threads within the same warp. The consideration behind is to reduce synchronization overhead. To safely use the shared memory, synchronization needs to be called to avoid read-write races (between line 12 and line 18 in Algorithm 2). If we allow different warps to use the same piece of data in shared memory, we need to insert synchronization in the entire thread block which brings significant overhead. Since CUDA provides warp-level fine-grained synchronization, which is much less expensive than block-level synchronization, we only make loaded data to be shared within a warp. The drawback is that different warps still perform redundant loading of sparse rows.

Our technique to address redundant data loading is Coarse-grained Warp Merging (CWM). It is similar to thread coarsening in dense matrix multiplication, which can improve bandwidth throughput with instruction-level parallelism (ILP) [28], and reduce the amount of memory transactions [29]. The basic idea is to merge the workload of different warps that
Algorithm 3 SpMM with CRC and CWM (CF=2)

Input: A.rowPtr[], A.colInd[], A.val[], B[]
Output: C[]

1: /* initialization (line 1-6 of Algorithm 2) */
2: result_1 = 0, result_2 = 0
3: for ptr = row_start to row_end-1 step warp_size do
4: /* load A.colInd, A.val (line 10-14 of Algorithm 2) */
5: for kk = 0 to warp_size do
6: k = sm_k[sm_base+kk]
7: result_1 += sm_v[sm_base+kk] * B[k,j]
8: result_2 += sm_v[sm_base+kk] * B[k,j+warp_size]
9: end for
10: end for
11: C[i,j] = result_1
12: C[i,j+warp_size] = result_2

has redundant data loading. In SpMM, merging workloads means to make each thread produce more output. We illustrate CWM by an example in Fig. 6. In Fig. 6, the suffix of \( t \) (short for thread) indicates both the indices to this thread and the indices of output it produces. Observe that \( \text{thread}_0 \) and \( \text{thread}_{0,32} \) both load data from row 0 of \( A \), but they belong to different warps and cannot share data under Algorithm 2. To dismiss this redundant load, we merge these two threads’ workloads, making \( \text{thread}_0 \) compute both \( C[0,0] \) and \( C[0,32] \). \( \text{thread}_0 \) will have two partial sum variables locally, and with every non-zero element in \( A \), it will load two values from matrix \( B \) and update two partial results. In Algorithm 3, we give a pseudo code with CWM adopted.

In Fig. 6 we merge the workloads of two warps and cut the number of threads by half. Intuitively this process can continue and we can cut down more threads. We call the factor of thread number reduction coarsening factor (CF). For example, CF is 2 in Fig. 6 which means each thread is assigned to produce 2 output values. In general, the load transactions of sparse rows can be reduced by CF through this technique. Another benefit of introducing thread coarsening is to improve bandwidth utility via ILP [28]. Line 7-8 in Algorithm 3 is independent memory loading instructions and GPU architecture can serve these two requests simultaneously, potentially increasing the usage of global bandwidth. Increasing CF can further reduce memory load, but there will be fewer threads on the fly. Large CF also causes each thread to hold more local variables for partial results, and this increment in resource usage may hurt performance. GPUs use massive parallel threads to hide all types of stalls, mostly the latency of memory load. When using CWM, it is significant to balance between data reuse and parallelism. Analytical models for choosing CF could be difficult due to the entangled effects of hardware parameters and sparse matrix properties. We turn to an empirical method and experimented on our dataset of real-world graphs with \( N = 512 \) to find a general best choice of CF, detailed in Section V-B.

IV. ACCELERATE GNN FRAMEWORKS WITH GE-SPMM

GE-SPMM is developed to accelerate GNN applications. The CSR format and SpMM-like operation support make it easy to be embedded in existing frameworks. This section briefly discusses how we use GE-SPMM to enhance the performance of existing GNN frameworks.

A. GE-SPMM for Different Matrix Sizes

To accelerate real applications, we make a few enhancement to support arbitrary input size (\( N \)). CRC and CWM apply well to problems with large \( N \), where the kernel needs to load a large amount of data from dense matrix and is bottle-necked by bandwidth efficiency. Fig. 7(c) shows the overall benefit of our two techniques when \( N = 16 \) and \( N = 64 \), with average performance on the test dataset (detailed in Section V-A) normalized to Algorithm 1. When \( N > 32 \) we apply both CRC and CWM in the kernel. CWM is not necessary for \( N \leq 32 \), since warp_size is 32, and we should directly call Algorithm 2 to dismiss the overhead of unnecessary instructions.

To address the need for SpMM-like operation in GNN models, we modify the basic GE-SPMM to allow user-defined operation. To define an SpMM-like operation, the user needs to provide an initialization function and a reduce function, both will be inlined at compile time. The parallel execution requires the reduction function to be associative and commutative, but common operations like taking sum or maximum are naturally valid.

B. GNN Acceleration Based on GE-SPMM

Current GNN frameworks like DGL [11] and PyG [23] are often based on other deep learning (DL) frameworks (e.g. PyTorch [10]), but add new APIs for graph operations. Although it is possible to express graph operations with sparse tensor operations provided by DL frameworks, the performance of sparse tensor operations is not satisfactory, so DGL implements all graph-related operations in C++/CUDA and exposes to DL frameworks as shared lib. We also follow this method to accelerate GNN application with a high-performance CUDA kernel.
To be more specific, we wrap our kernel inside a custom autograd function, which is an atomic operator with gradient definition in PyTorch. This function represents an aggregation step on the graph, and can be used to build GNN layers and modules. Since DGL already implements SpMM-like in CUDA, we simply substitute their kernel with ours and rebuild the project. PyG is another popular Python library for GNN built on PyTorch. It abstracts GNN as MessagePassing procedure and implements MessagePassing as a versatile module that allows user-defined message and aggregation functions. MessagePassing is a more general interface than SpMM-like, so we cannot use SpMM-like to replace MessagePassing. We instead implement an SpMM-like operator and replace the MessagePassing function calls in training code with ours. An overview of how we integrate GE-SpMM to GNN frameworks is shown in Fig. 2.

V. EXPERIMENT EVALUATIONS

We conduct extensive experiments on our GE-SpMM design, and the performance comparison against various SpMM kernels and GNN frameworks is shown in this section.

A. Experiment Setup

1) Graph Benchmarks: In order to test the proposed GE-SpMM for GNN workloads, we run experiments on three graphs [19] used for node-classification tasks in many GNN models [3], [4]. Cora, Citeseer, and Pubmed, whose properties are listed in Table IV. We also test the performance on SNAP dataset collected in SuiteSparse Matrix Collection [30], a sparse matrix benchmark. SNAP group in SuiteSparse contains 66 valid graphs from various domains. The original SNAP dataset maintained in [18] also contains metadata of some graphs which are not collected in SuiteSparse, but we limit our test to graphs in SuiteSparse to save the effort of converting metadata to standard input. We omit two graphs (FriendSter and Twitter) due to out-of-memory. Some items in SuiteSparse contains more than one matrices. We only run tests on one matrix in each item. This set of 64 sparse matrices has size \( M \) from 1005 to 4847571 with \( nnz/row \) from 1.58 to 32.53. [16] experiments on models with feature size up to 512 and presents the best performance on SNAP dataset collected in SuiteSparse Matrix Collection.

2) SpMM Baselines: We compare our GE-SpMM with the following baselines in our experiments.

- SpMM kernel by vendor: \texttt{csrmm2}. It is a function in cuSPARSE [1] for SpMM. cuSPARSE has two functions for multiplication of sparse and dense matrices. The \texttt{csrmm2} assumes a row-major input dense matrix, while the other one, \texttt{csrmm}, assumes a column-major input dense matrix. The \texttt{csrmm2} consistently outperforms \texttt{csrmm}, and here we show a comparison to \texttt{csrmm2}. Note that, the output dense matrix of \texttt{csrmm2} is column-major, which is a convention in many Nvidia libraries. As explained in Section II-C, GNN applications require row-major output, so existing solution is forced to perform matrix transpose upon \texttt{csrmm2} output. We do not add this to baseline when comparing kernel performance. However, this overhead of cuSPARSE cannot be ignored in real applications.

- Open-source SpMM kernel: \texttt{rowsplit} in GraphBLAST [2]. It is a most-recent CSR-based SpMM implementation in literature.

- Graph processing engine on GPUs: GunRock [20]. Because the SpMM can be executed from a graph perspective by assigning each vertex with a feature vector, we also compare our GE-SpMM with the state-of-the-art graph processing system on GPUs.

3) Environments: We conduct experiments on the following two machines:

- Machine 1. GPU: Nvidia GTX 1080Ti, Compute Capability 6.1 (28 Pascal SMs at 1.481 GHz, 11 GB GDDR5X with 484 GB/s bandwidth). Host CPU: Intel(R) Xeon(R) CPU E5-2643 v4 (24 cores).

- Machine 2. GPU: Nvidia RTX 2080, Compute Capability 7.5 (46 Turing SMs at 1.515 GHz, 8 GB GDDR6 with 448 GB/s bandwidth). Host CPU: Intel(R) Core(TM) i7-9700K (8 cores).

In kernel performance tests, all codes are compiled using NVCC (CUDA compiler provided by Nvidia) in CUDA 10.1 with -O3 flag. Execution time is measured from average of 200 kernel runs. Throughput is calculated from theoretical float-operation \((2 \times nnz \times N)\) over measured execution time. For application speedup, all reported items (kernel and model time) refer to CUDA time reported in PyTorch profiler.

B. Benefits of GE-SpMM Design

1) Benefits of Coalesced Row Caching: The aim of CRC is to enable coalesced access to sparse matrix and improve bandwidth efficiency. To evaluate the effectiveness of CRC, we use Nvidia’s nvprof to profile two metrics [12]: gld_transactions (GLT), the number of global load transactions; gld_efficiency (GLT_eff), ratio of requested global memory load throughput to required global memory load throughput. One issued memory transaction loads a fixed size of data, but the program may only require a part of it. This metric can reflect how efficiently the program uses global bandwidth.

### Table IV

**Graphs Used in GNN for Classification [19]**

| Graph   | # Vertices | # Edges | # Classes |
|---------|------------|---------|-----------|
| Cora    | 2708       | 5429    | 7         |
| Citeseer| 3327       | 4732    | 6         |
| Pubmed  | 19717      | 44338   | 3         |

*The matrix which has the same filename as this item is considered the default one.*
The tests run on three synthetic random graphs with $N = 512$. We only have profiling results on Machine 1 since nvpprof in CUDA 10.1 does not support GPU over 7.2 capability [12]. The results in Table V show that using CRC can significantly reduce the total number of load transactions, as well as improve the memory load efficiency due to coalesced memory access.

### Table V

| Matrix | Method       | GLT ($\times$ 32 bytes) | GLT effi |
|--------|--------------|--------------------------|----------|
| $M=16K$ | w/o CRC      | 1.34e+8                  | 68.95%   |
| $nnz=160K$ | w/ CRC      | 0.53e+8                  | 92.40%   |
| $M=65K$ | w/o CRC      | 5.36e+8                  | 68.95%   |
| $nnz=650K$ | w/ CRC     | 2.18e+8                  | 92.40%   |
| $M=262K$ | w/o CRC      | 2.14e+8                  | 68.95%   |
| $nnz=2.6M$ | w/ CRC      | 8.75e+8                  | 92.39%   |

Fig. 8 shows the relative improvement of applying CRC (Algorithm 2) against Algorithm 1. On GTX 1080Ti, CRC brings an average of 1.246× performance gain. On RTX 2080, simply applying CRC does not bring significant performance gain (average of 1.011×). However, CRC is the foundation of our second technique CWM. One benefit of CWM is a high throughput of loading dense matrix with ILP, but without CRC, the bandwidth is spent on a large amount of inefficient access to the sparse matrix, and leaves little room for loading the dense matrix. In the next part, we will show that combined with CWM, GE-SpMM still achieved significant improvement over simple SpMM on RTX 2080.

2) Benefits of Coarse-grained Warp Merging: CWM is introduced in order to reuse loaded data and reduce global transactions. However, it reduces the total number of warps and may harm parallelism. We also use nvpprof to test the effects brought by CWM. We profile three metrics: gld_transactions (GLT), as previously mentioned it indicates the amount of data loading; gld_throughput, the throughput of the global load; achieved_occupancy (Occ), the ratio of the average active warps to the maximum supported on a multiprocessor, which can be a reflection of achieved parallelism.

The results in Table VI are tested on one of the random graphs ($M = 65K, nnz = 650K, N = 512$). It shows that CWM can reduce global data loading. When the coarsening factor (CF) gets larger, gld_transactions keep decreasing, but the benefit becomes smaller because loading dense matrix takes up most of the transactions. When increasing CF, the occupancy also decreases, indicating parallelism loss. The combination of CRC and CWM brings an average of 1.65× and 1.53× speedup on GTX 1080Ti and RTX 2080 respectively over non-optimized version (Algorithm 1).

### Table VI

| Method       | GLT ($\times$ 32 bytes) | gld_throughput (GB/s) | Occ |
|--------------|--------------------------|-----------------------|-----|
| w/o CWM      | 2.18e+8                  | 479.54                | 0.75 |
| CWM (CF=2)   | 1.93e+8                  | 567.82                | 0.75 |
| CWM (CF=4)   | 1.80e+8                  | 479.23                | 0.75 |
| CWM (CF=8)   | 1.74e+8                  | 395.22                | 0.75 |

In practice, tuning for optimal CF requires a balance between data reuse and parallelism, which are related to properties of the input matrix. In Fig. 9, we plot the relative performance when taking different CF. Each bar represents a test on one graph in SNAP dataset. The relative performance means speedup over not using CWM. It can be observed that CF = 2 works well for most matrices, while CF > 4 shows obvious performance drop. For rare cases (4 and 1 out of 64 on two GPUs), choosing CF = 2 causes over 15% performance loss compared to optimal CF. Since our goal is to provide a runtime SpMM kernel, we avoid any parameter tuning and

Fig. 10 shows the relative improvement of applying CRC (Algorithm 2) against Algorithm 1. On GTX 1080Ti, CRC brings an average of 1.246× performance gain. On RTX 2080, simply applying CRC does not bring significant performance gain (average of 1.011×). However, CRC is the foundation of our second technique CWM. One benefit of CWM is a high throughput of loading dense matrix with ILP, but without CRC, the bandwidth is spent on a large amount of inefficient access to the sparse matrix, and leaves little room for loading the dense matrix. In the next part, we will show that combined with CWM, GE-SpMM still achieved significant improvement over simple SpMM on RTX 2080.

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use $CF = 2$ because it provides the best overall effect. The kernel performance reported in the following experiments is all the results of $CF = 2$. Moreover, our previous tests show that on RTX 2080, CRC cannot bring large performance gain, but a combination of CRC and CWM can bring significant improvement (an average of $1.51 \times$) with $CF = 2$.

C. Overall Performance of SpMM Kernel

In this part, we present overall performance compared to kernels in cuSPARSE [1] and GraphBLAST [2]. All matrices in tests are single-precision, as is the case in GNN models. For kernel performance, we test $N$ from 128 up to 512.

1) Graphs for GNNs: We test GE-SpMM on three graphs used in GNN models, and results are shown in Fig. [10]. Benefit from our two techniques, GE-SpMM can outperform cuSPARSE by at most $1.62 \times$. Tests on these three graphs show that GE-SpMM can potentially accelerate real GNN models if applied in GNN frameworks.

2) Graphs from SNAP: The performance comparison of GE-SpMM and baselines on SNAP dataset is shown in Fig. [11]. To summarize, the average performance gain is listed in Table VII. GE-SpMM achieves up to $1.43 \times$ and $1.81 \times$ speedup compared with cuSPARSE [1] and GraphBLAST [2]. Although the arbitrary performance is related to graph characteristics, Fig. [11] can demonstrate that for any specific graph, our kernel becomes more competitive over baseline when $N$ gets larger. In other words, our techniques are crucial for applications with large $N$.

D. Comparison with Graph Engines on GPUs

It is also possible to build SpMM with graph engines from a graph processing perspective. GunRock [20] provides many APIs and built-in kernels that allow users to write graph algorithms. We use GunRock’s API advance to write an SpMM program. However, GunRock does not provide any options to parallelize along feature dimension, because in traditional graph algorithms like PageRank, the feature of a vertex is an undividable scalar. GunRock fails to provide feature-dimension parallelism, which significantly harms SpMM performance. Fig. [12] shows the kernel execution time of GE-SpMM compared to the program written with GunRock. GE-SpMM outperforms GunRock-based implementation by $18.27 \times$ on average for all test cases, indicating that SpMM and GNN workloads require new primitives in graph processing frameworks rather than SpMV.

E. Comparison with preprocess-based approaches

Some previous researches propose specialized sparse formats for SpMM problem that exploit regular memory access [21] or data reuse [13], [14]. As far as we know, ASpT [14] is the best SpMM implementation publicly avail-

| Machine   | Baseline | N=128 | N=256 | N=512 |
|-----------|----------|-------|-------|-------|
| GTX 1080Ti| cuSPARSE | 1.18  | 1.30  | 1.37  |
|           | GraphBLAST | 1.42  | 1.44  | 1.61  |
| RTX 2080  | cuSPARSE | 1.20  | 1.34  | 1.43  |
|           | GraphBLAST | 1.57  | 1.73  | 1.81  |

Fig. 11. Overall performance on 64 graphs in SNAP dataset. The omitted bars are due to out-of-memory. The matrix_id corresponds to the alphabetical order of matrix name.
able. ASpT [14] exploits reusing dense matrix data with tiling. It requires a special sparse format composed of CSR and additive arrays to mark the positions of locally-dense blocks explicitly. Our optimizations in this paper to reuse sparse matrix data is orthogonal to their techniques.

We test their source code on our machines on the SNAP dataset and results are listed in VIII. Our GE-SpMM achieves average of 0.93X, 0.97X, 1.00X for N=128, 256, 512 on GTX1080Ti GPU, and average 0.85X, 0.93X, 0.98X on RTX2080, against ASpT (without preprocess time).

The preprocess overhead varies significantly on different sparse matrices, from 0.01× to 64.53× of actual SpMM execution time, and average overhead is 0.47× execution time on GTX1080Ti and 0.34× on RTX2080. With preprocess time added (one preprocess + one run), our kernel is average 1.43×~2.06× against ASpT.

| Machine      | Baseline | N=128 | N=256 | N=512 |
|--------------|----------|-------|-------|-------|
| GTX 1080Ti   | ASpT [1] | 0.93  | 0.97  | 1.00  |
|              | ASpT w/ preproc [2] | 1.88  | 1.97  | 2.06  |
| RTX 2080     | ASpT [1] | 0.85  | 0.93  | 0.98  |
|              | ASpT w/ preproc [2] | 1.43  | 1.57  | 1.69  |

Fig. 12. Speedup of GE-SpMM over GunRock-based SpMM.

Fig. 13. Accelerating GNNs using GE-SpMM in DGL [11], (x, y) represents the number of layers (x) and the length of features (y) in a GNN model, which is the input parameter for GNNs.

Fig. 14. Accelerating GNNs using GE-SpMM in PyG [23], (x, y) represents the number of layers (x) and the length of features (y) in a GNN model, which is the input parameter for GNNs.

TABLE VIII

GE-SpMM AVERAGE SPEED AGAINST ASpT [14]

F. End-to-End Performance for GNNs

Our kernel is developed to accelerate GNN applications, and the CSR-based property makes it easy to be embedded in existing frameworks. As introduced in Section IV we embed GE-SpMM in DGL [11] and PyG [23]. We test application speedup on GCN, GraphSAGE, and other popular GNN models that involve SpMM or SpMM-like operations.

1) GNNs based on SpMM Operators: Comparison with DGL. SpMM is a very common operator in GNN, and GE-SpMM can benefit many GNN models. We test the benefit of integrating GE-SpMM in DGL with two models: GCN [3] and GraphSAGE-gcn [4]. For both models, we use example codes provided by DGL, and run tests on different model settings (number of layers and length of feature vectors in each layer). We use PyTorch profiler to monitor the entire training process and record total CUDA time from the report. The results are shown in Fig. 13. GE-SpMM brings speedup in most of these applications. However, in 4 tests on GTX 1080Ti, GE-SpMM does not bring acceleration over original DGL. This is because the feature length of the last layer in GNN models usually equals the number of classes in the classification problem. Therefore, the output layer involves SpMM with a small N, when GE-SpMM is not very competitive.

2) GNNs based on SpMM-like Operators: GE-SpMM is intended to accelerate a class of SpMM-like operators that is not yet supported by cuSPARSE. One good example is the pooling operation in GraphSAGE-pool [4], where each vertex aggregates the features of its neighbors by taking maximum. cuSPARSE does not provide this operation. Future GNN models may also use customized reduction functions for pooling, and relying on cuSPARSE is not flexible to these user-defined operations. It is not hard to generalize GE-SpMM to support SpMM-like operations, since these operations follow similar memory access patterns and the code is almost the same. We implement a GE-SpMM kernel for the aggregation step in GraphSAGE-pool. Our kernel brings up to 1.14× acceleration on the CUDA time of GraphSAGE-pool training on Pubmed graph. Note that for SpMM-like operation only, GE-SpMM can achieve 2.39× to 6.15× speedup over DGL's
SpMM-like kernel. This shows the value of this work in supporting flexible, user-defined SpMM-like operation in new GNN models, which are not covered by the vendor library, and achieve even better performance.

| (#layer, #feature) | GTX 1080Ti | RTX 2080 |
|------------------|------------|----------|
| SpMM-like        | Total      | SpMM-like total | Total      | SpMM-like total |
| (1,16)           | 2.89       | 1.10      | 3.24       | 1.11 |
| (1,64)           | 3.92       | 1.14      | 3.44       | 1.11 |
| (1,256)          | 4.04       | 1.14      | 3.46       | 1.09 |
| (2,16)           | 2.39       | 1.11      | 3.03       | 1.09 |
| (2,64)           | 3.09       | 1.09      | 3.37       | 1.11 |
| (2,256)          | 6.15       | 1.12      | 3.51       | 1.09 |

VI. CONCLUSION

In this paper, we propose an efficient CSR-based SpMM design, GE-SpMM, for Graph Neural Network applications on GPUs. GE-SpMM considers requirements by GNN applications, including no preprocessing and SpMM-like operation requirements. GE-SpMM introduces two techniques: Coalesced Row Caching and Coarse-grained Warp Merging, to improve the efficiency of global data access, leading to 1.25 × and 1.51 × speedup, respectively. By adopting these optimizations, GE-SpMM achieves up to 1.41 × speedup over Nvidia cuSPARSE [1] and up to 1.81 × over GraphBLAST [2]. We also embed GE-SpMM in GNN frameworks (e.g., DGL, PyG) and achieve significant CUDA time reduction.

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