Operads of Wiring Diagrams

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**ABSTRACT.** Wiring diagrams and undirected wiring diagrams are graphical languages for describing interconnected processes and their compositions. These objects have enormous potentials for applications in many different disciplines, including computer science, cognitive neuroscience, dynamical systems, network theory, and circuit diagrams. It is known that the collection of wiring diagrams is an operad and likewise for undirected wiring diagrams.

This monograph is a comprehensive study of the combinatorial structure of various operads of wiring diagrams and undirected wiring diagrams. Our first main objective is to prove a finite presentation theorem for each operad of wiring diagrams, describing each one in terms of just a few operadic generators and a small number of generating relations. For example, the operad of wiring diagrams has 8 generators and 28 generating relations, while the operad of undirected wiring diagrams has 6 generators and 17 generating relations.

Our second main objective is to prove a corresponding finite presentation theorem for algebras over each operad of wiring diagrams. As applications we provide finite presentations for the propagator algebra, the algebra of discrete systems, the algebra of open dynamical systems, and the (typed) relational algebra. We also provide a partial verification of Spivak’s conjecture regarding the quotient-freeness of the relational algebra.

Our third main objective is to construct explicit operad maps among these several operads of wiring diagrams. In particular, there is a surjective operad map from the operad of all wiring diagrams, including delay nodes, to the operad of undirected wiring diagrams.

This monograph is intended for graduate students, mathematicians, scientists, and engineers interested in operads and wiring diagrams. Assuming no prior knowledge of categories, operads, and wiring diagrams, this monograph is self-contained and can be used as a supplement in a graduate course and for independent study. There are over 100 graphical illustrations and a chapter with a list of problems.
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# List of Notations

| Notation                  | Page | Description                                           |
|--------------------------|------|-------------------------------------------------------|
| \( S \)                  | 13   | a class                                               |
| \( \text{Prof}(S) \)     | 14   | the collection of \( S \)-profiles                   |
| \( s = (s_1, \ldots, s_n) \) | 14   | an \( S \)-profile of length \( n \)                 |
| \( \text{Prof}^n(S) \)   | 14   | \( S \)-profiles of length at least \( n \)           |
| \( \Sigma_n \)          | 15   | the symmetric group on \( n \) letters                |
| \( (O, \mathbb{1}, \gamma) \) | 15   | an \( S \)-colored operad                            |
| \( O(\sigma) \)         | 15   | the \( (\sigma) \)-entry of \( O \)                  |
| \( c \sigma \)          | 15   | the right permutation of \( c \) by \( \sigma \)      |
| \( \mathbb{1}_c \)      | 15   | the \( c \)-colored unit                              |
| \( \gamma \)            | 15   | operadic composition                                  |
| \( \sigma(k_1, \ldots, k_m) \) | 17   | block permutation                                     |
| \( \tau_1 \oplus \cdots \oplus \tau_n \) | 17   | block sum                                             |
| \( \text{End}(X) \)     | 17   | endomorphism operad of \( X \)                       |
| \( \text{As} \)         | 18   | associative operad                                    |
| \( \text{Com} \)        | 18   | commutative operad                                    |
| \( \text{GrOp} \)       | 18   | operad of graph operations                            |
| \( (O, \mathbb{1}, \circ) \) | 20   | an \( S \)-colored operad                            |
| \( \circ_i \)          | 20   | \( \circ_i \)-composition in an operad               |
| \( \sigma \circ \tau \) | 22   | \( \circ \)-composition of permutations              |
| \( \text{Fin} \)        | 25   | the category of finite sets and functions             |
| \( \text{Fin}_S \)      | 25   | the category of \( S \)-finite sets                  |
| \( (X^{\text{in}}, X^{\text{out}}) \) | 25   | an \( S \)-box                                        |
| \( X^{\text{in}} \)     | 25   | the set of inputs of an \( S \)-box \( X \)          |
| \( X^{\text{out}} \)    | 25   | the set of outputs of an \( S \)-box \( X \)         |
| \( \text{Box}_S \)      | 25   | the collection of \( S \)-boxes                      |
| Notation          | Page | Description                                                                 |
|-------------------|------|-----------------------------------------------------------------------------|
| \( v \)          | 25   | value assignment                                                            |
| \( \emptyset \)   | 25   | the empty S-box                                                              |
| \( \text{DN} \)   | 27   | the set of delay nodes                                                       |
| \( \text{Dm} \)   | 27   | the set of demand wires                                                      |
| \( \text{Sp} \)   | 27   | the set of supply wires                                                      |
| \( s : \text{Dm} \rightarrow \text{Sp} \) | 28   | the supplier assignment                                                      |
| \( \varphi \)     | 28   | the set of external wasted wires of \( \varphi \)                           |
| \( \varphi w \)   | 28   | the set of internal wasted wires of \( \varphi \)                           |
| \( \text{WD}(\vec{\lambda}) \) | 29   | the \( (\vec{\lambda}) \)-entry of \( \text{WD} \)                        |
| \( \text{WD} \)   | 29   | the collection of wiring diagrams                                           |
| \( \text{I}_Y \)  | 30   | the \( Y \)-colored unit in \( \text{WD} \)                                 |
| \( \epsilon \)    | 40   | the empty wiring diagram                                                    |
| \( \delta_d \)    | 40   | a 1-delay node                                                               |
| \( \tau_{x,y} \)  | 41   | a name change                                                               |
| \( \theta_{x,y} \) | 41   | a 2-cell                                                                    |
| \( \lambda_{x,x} \) | 41   | a 1-loop                                                                    |
| \( \sigma_{x_1,x_2} \) | 42   | an in-split                                                                 |
| \( \sigma_{y_1,y_2} \) | 43   | an out-split                                                                 |
| \( \omega_{y_1,y_2} \) | 44   | a 1-wasted wire                                                             |
| \( \omega^x_{x,x} \) | 45   | a 1-internal wasted wire                                                    |
| \( \varphi_1 \circ \cdots \circ \varphi_k \) | 46   | (iterated) \( \circ_1 \)                                                   |
| \(|T|\)            | 47   | the cardinality of a finite set                                             |
| \( \pi^{lp} \)    | 69   | the set of loop elements in \( \pi \)                                       |
| \( \pi^{sp}_x \)  | 69   | the set of internally supplied elements in \( \pi \)                        |
| \( \pi^{sp}_x \)  | 69   | the set of externally supplied elements in \( \pi \)                        |
| \( |\Psi|\)         | 88   | the composition of a simplex \( \Psi \)                                     |
| \( (\psi_1, \ldots, \psi_n) \) | 89   | an \( n \)-simplex in \( \text{WD} \)                                     |
| \( \text{WD}_n \) | 99   | the collection of normal wiring diagrams                                     |
| \( \text{WD}_0 \) | 101  | the collection of strict wiring diagrams                                     |
| \( A_c \)         | 106  | the \( c \)-colored entry of an algebra \( A \)                             |
| \( \mu \)         | 106  | the structure map of an algebra                                             |
| \( \mu \circ_1 \mu \xi \) | 108  | \( \circ_1 \)-composition of structure maps                                |
| \( \partial \)    | 119  | truncation                                                                  |
| \( \text{Hist}^k \) | 119  | the set of \( k \)-historical propagators                                  |
| \( D_k \)         | 120  | \( k \)-moment delay function                                               |
| \( P_X \)         | 120  | the set of 1-historical propagators of type \( X \)                         |
| \( \langle-\rangle_{x_+} \) | 122  | take only the \( \nu(x_+) \)-entry                                         |
| \( \langle-\rangle_{\backslash x_+} \) | 122  | remove the \( \nu(x_+) \)-entry                                           |
### List of Notations

| Notation | Page | Description |
|----------|------|-------------|
| DS($X$) | 137  | the collection of $X$-discrete systems |
| $x_I$   | 145  | take only the entries indexed by $I$ |
| $X_{\sim I}$ | 145  | remove the entries indexed by $I$ |
| $G_X$   | 145  | the $X$-colored entry of the algebra of open dynamical systems |
| Ch. 7   | 155  | a cospan |
| UWD     | 156  | the collection of undirected wiring diagrams |
| $X_{[i,j]}$ | 161  | $X_i \cup \cdots \cup X_j$ or $\emptyset$ |
| $C_\varphi$ | 161  | the set of cables in $\varphi$ |
| Ch. 8   | 170  | the empty cell |
| $e$     | 170  | a 1-output wire |
| $\omega_+$ | 170  | an undirected name change |
| $\tau_f$ | 170  | an undirected 2-cell |
| $\theta_{(X,Y)}$ | 171  | a loop |
| $\lambda_{(X,x_+)}$ | 171  | a split |
| Ch. 9   | 186  | the set of $(m,n)$-cables |
| $C_\varphi^{(m,n)}$ | 186  | the set of wasted cables |
| $C_\varphi^{(0,0)}$ | 186  | the set of $(\geq m,n)$-cables |
| $C_\varphi^{(m,\geq n)}$ | 186  | the set of $(m,\geq n)$-cables |
| $C_\varphi^{(\geq m,\geq n)}$ | 186  | the set of $(\geq m,\geq n)$-cables |
| Ch. 10  | 204  | an $n$-simplex in UWD |
| $(\psi_1, \ldots, \psi_n)$ | 204  | an $n$-simplex in UWD |
| Ch. 11  | 221  | the set of functions $X \rightarrow A$ |
| $A^X$   | 221  | the power set of $X$ |
| $\mathcal{P}(X)$ | 221  | $\mathcal{P}(A^X)$ |
| $\text{Rel}_A(X)$ | 221  | the relational algebra of $A$ |
| $\text{Rel}_A$ | 222  | the typed relational algebra |
| Ch. 12  | 241  | $Y_{\text{in}} \cup Y_{\text{out}}$ |
| $\chi$  | 242  | the operad map $\text{WD}_\bullet \rightarrow \text{UWD}$ |
| $\chi^0$ | 254  | the operad map $\text{WD}_0 \rightarrow \text{UWD}$ |
| Ch. 13  | 262  | the operad map $\text{WD} \rightarrow \text{UWD}$ |
Chapter 1

Introduction

1.1. What are Wiring Diagrams?

Wiring diagrams form a kind of graphical language that describes operations or processes with multiple inputs and multiple outputs and how such operations are wired together to form a larger and more complicated operation. Some visual examples of wiring diagrams are in (2.2.18.1), Chapter 3 and Example 4.2.3. The first type of wiring diagrams that we are going to study in this monograph was first introduced in [RS13], with variants studied in [Spi15, Spi15b, VSL15]. In [Spi15, Spi15b] wiring diagrams without delay nodes (Def. 5.3.1), which we call normal wiring diagrams, were used to study mode-dependent networks, discrete systems, and dynamical systems. In [VSL15] wiring diagrams without delay nodes and whose supplier assignments are bijections (Def. 5.4.1), which we call strict wiring diagrams, were used to study open dynamical systems.

Wiring diagrams are by nature directed, in the sense that every operation has a finite set of inputs and a finite set of outputs, each element of which is allowed to carry a value of some kind. There is also an undirected version of wiring diagrams [Spi13, Spi14]. Unlike a wiring diagram, in an undirected wiring diagram, each operation is a finite set, each element of which is again allowed to carry a value. Some visual examples of undirected wiring diagrams are in (7.4.7.1), Example 7.3.8 and Chapters 8 and 9. For those familiar with operad theory, the distinction between wiring diagrams and undirected wiring diagrams is similar to that between operads and cyclic operads. Just as cyclic operads are not simpler than operads, undirected wiring diagrams are not really simpler than wiring diagrams and have their own subtlety.
The main reason that wiring diagrams and undirected wiring diagrams are important is that they have enormous potential for applications in many different disciplines. Wiring diagrams and undirected wiring diagrams allow one to consider a finite collection of related operations, wired together in some way, as an operation itself. Such an operation can then be considered as a single operation within a yet larger collection of operations, and so forth. For instance, a finite collection of related operations may be a group of neurons in a certain region of the brain, a collection of codes within a large computer program, or a few related agents within a large supply-chain. In fact, the authors of [RS13] cited both computer science and cognitive neuroscience as potential applications of wiring diagrams. Furthermore, in [Spi15b, VSL15] wiring diagrams were used to study dynamical systems and to model certain kinds of differential equations. Many potential fields of applications are mentioned in the introduction of [VSL15]. In [Spi13] undirected wiring diagrams were used to study database relational queries, plug-and-play devices, recursion, and circuit diagrams.

The substitution process involving wiring diagrams and undirected wiring diagrams described in the previous paragraph can be captured precisely using the notion of colored operads. A colored operad, or just an operad, is a mathematical object that describes operations with multiple inputs and one output and their compositions. A colored operad in which there are only unary operations is exactly a category. If one restricts even further to just the 1-colored case in which the unary operations form a set, then one has exactly a monoid, such as the set of integers under addition. Therefore, a colored operad is a multiple-input generalization of a category, and in fact colored operads are also called symmetric multicategories. Multicategories without symmetric group actions were introduced by Lambek [Lam69]. One-colored operads, together with the name operad, were introduced by May [May72] in the topological setting. See [May97] for the definition of a one-colored operad in a symmetric monoidal category. The book [Yau16] is an elementary introduction to colored operads in symmetric monoidal categories. The book [YJ15] has more in-depth discussion of colored operads and related objects.

In [RS13] Rupel and Spivak observed that the collection of wiring diagrams is a colored operad $\mathcal{WD}$, in which the operadic composition corresponds precisely to the substitution process described above. Each colored operad has associated algebras, on which the colored operad acts. The operadic action is similar to the action of an associative algebra on a left module. The authors of [RS13] defined a $\mathcal{WD}$-algebra, called the propagator algebra, that models a certain kind of input-output process.

Closely related colored operads of sub-classes of wiring diagrams were introduced in [Spi15, Spi15b, VSL15]. We will denote by $\mathcal{WD}_\bullet$ (Def. 5.3.1) the operad of normal wiring diagrams, meaning those without delay nodes. In [Spi15b] Spivak introduced a $\mathcal{WD}_\bullet$-algebra, called the algebra of discrete systems, that is closely
1.2. Purposes of this Monograph

This monograph is a comprehensive study of the combinatorial structure of the operads $WD$, $WD_\bullet$, $WD_0$, and $UWD$ of (normal/strict/undirected) wiring diagrams, their algebras, and the relationships between these operads. Specifically, our main results are of the following three types.

**Finite Presentation for Operads:** For each of the operads $WD$, $WD_\bullet$, $WD_0$, and $UWD$, we prove a finite presentation theorem that describes the operad in terms of just a few operadic generators and a small number of generating relations. For the operad of wiring diagrams $WD$, there are 8 generating wiring diagrams and 28 generating relations. For the smaller operads $WD_\bullet$ and $WD_0$ of normal and strict wiring diagrams, the numbers of operadic generators and of generating relations are $(7, 28)$ and $(4, 8)$, respectively. For the operad of undirected wiring diagrams $UWD$, there are 6 operadic generators and 17 generating relations.

**Finite Presentation for Algebras:** For each of the operads $WD$, $WD_\bullet$, $WD_0$, and $UWD$, we prove a corresponding finite presentation theorem for their algebras. To be more precise, we describe $WD$-algebras using 8 generating structure maps and 28 generating axioms. So finite presentation refers to the $WD$-algebra structure maps, not the elements in the underlying set. Similar finite presentations are also obtained for the algebras over the operads $WD_\bullet$ of normal wiring diagrams, $WD_0$ of strict wiring diagrams, and $UWD$ of undirected wiring diagrams. As applications we provide finite presentations for the propagator algebra over $WD$, the algebra of discrete systems over $WD_\bullet$, the algebra of open dynamical systems over $WD_0$, and the (typed) relational algebra over $UWD$. Along the way, we provide a partial verification of Spivak’s conjecture regarding the quotient-freeness of the relational algebra.
Maps Between Operads: We construct a commutative diagram

\[
\begin{array}{ccc}
WD_0 & \longrightarrow & WD \\
\downarrow^{\chi_0} & & \downarrow^{\chi} \\
\downarrow^\rho & & \downarrow^\rho \\
UWD & \longrightarrow & UWD
\end{array}
\]

of operad maps, in which the horizontal maps are operad inclusions. For each of the operad maps $\chi_0$, $\chi$, and $\rho$, we compute precisely the image in $UWD$. In particular, the operad map $\rho : WD \longrightarrow UWD$ is surjective. The existence of the operad map $\rho$ answers a question raised in [RS13].

The end of this chapter contains several tables that summarize the main results and contain some key references.

The finite presentation theorems for the operads $WD$, $WD_\bullet$, $WD_0$, and $UWD$ reduce the structure of these operads and their algebras to just a few generators and relations. For example, our finite presentation theorem for the operad $WD$ reduces the understanding of this operad to just 8 simple wiring diagrams and 28 simple relations among them. Likewise, the structure map of a general $WD$-algebra can be quite involved, as can be seen in the propagator algebra [RS13]. Our finite presentation theorem for $WD$-algebras reduces the definition and understanding of $WD$-algebras to just 8 simple generating structure maps and 28 generating axioms, almost all of which are trivial to check in practice. We will further illuminate this point when we discuss the finite presentations for the propagator algebra over $WD$, the algebra of discrete systems over $WD_\bullet$, the algebra of open dynamical systems over $WD_0$, and the (typed) relational algebra over $UWD$.

To give our finite presentation theorems for the operads $WD$, $WD_\bullet$, $WD_0$, and $UWD$, and for their algebras an even more familiar feel, let us recall a few other places where various kinds of finite presentations occur. Each type of finite presentation is a way to reduce a large, usually infinite, collection of conditions to a finite, or at least smaller, collection of conditions, thereby making the relevant structure more manageable.

1. In basic group theory and commutative ring theory [AT69, Rot02], it is quite common to consider finite presentation of groups and modules. For example, over a commutative Noetherian ring, every finitely generated module is also finitely presented [Rot02] (Prop. 7.59).

2. A cornerstone in category theory, Mac Lane’s Coherence Theorem [Mac63, Mac98] can be regarded as a finite presentation theorem for monoidal categories. Roughly speaking, this theorem says that, in any monoidal category, the infinite collection of commutative formal diagrams has a finite presentation. The generators are the associativity isomorphism, the left
and the right units, and their inverses. The generating relations are the
Pentagon Axiom for 4-fold iterated tensor products and two unity axioms.

3. In the linear setting, the operads for associative algebras, commutative al-
gebras, Lie algebras, Leibniz algebras, Poisson algebras, and many others,
are finitely presented [GK94]. For example, the associative operad has
one generator, which in its algebras corresponds to the usual multiplica-
tion $A \otimes A \to A$ of an associative algebra. The associative operad has one
generating relation, which in its algebras corresponds to the usual associ-
avity axiom, $(ab)c = a(bc)$, of an associative algebra.

4. In [BE14, BSZ14] a finite presentation is given for the symmetric monoidal
category of signal-flow graphs. In applications signal-flow graphs form
another kind of graphical language that describes processes with inputs
and outputs and relations between them. One main difference between
(undirected) wiring diagrams and signal-flow graphs is that the composi-
tion of signal-flow graphs is done by grafting. This means that the outputs
of one signal-flow graph are connected to the inputs of another signal-flow
graph. This is similar to the situation in string diagrams [JSV96, SSR15]
On the other hand, the operadic composition of (undirected) wiring dia-
grams is done by substitution, which is pictorially depicted in (2.3.3.1) for
wiring diagrams and in (7.3.3.1) for undirected wiring diagrams. In more
conceptual terms, the collection of signal-flow graphs is a prop, hence an
algebra over the operad for props [YJ15] (Theorem 14.1). On the other
hand, the collection of (undirected) wiring diagrams is an operad.

5. Closer to the topic of this monograph is [YJ15] (Ch.7), where finite pre-
sentations are given for various graph groupoids including those for col-
ored operads, colored props, and colored wheeled props. In fact, the way
we phrase and verify our finite presentation theorems for the operads of
(undirected) wiring diagrams and for their algebras is conceptually simi-
lar to the presentation in [YJ15] (Ch.7). One way to explain this conceptual
similarity is that, for both (undirected) wiring diagrams and the graphs
for, say, colored wheeled props, the composition is done by substitution.
However, wiring diagrams are in several ways more complicated than the
graphs in [YJ15]. In fact, the graphs in [YJ15] do not have delay nodes, in-
ternal and external wasted wires, and split wires, all of which can happen
in a wiring diagram. See, for example, the wiring diagram in (2.2.18.1).

1.3. Audience and Features

The main results in this monograph—namely, the finite presentation theorems for
the various operads of (undirected) wiring diagrams and for their algebras as well
as operad maps between them—are new. So this monograph should be useful to
1. Introduction

mathematicians with an interest in operads and (undirected) wiring diagrams. Furthermore, due to the wide variety of potential applications, we also intend to make this monograph and this subject accessible to scientists and engineers.

With such a large audience in mind, the prerequisite for this monograph has been kept to an absolute minimum. In particular, we assume the reader is comfortable with basic concepts of sets, functions, and mathematical induction. No prior knowledge of categories, operads, and (undirected) wiring diagrams is assumed. The presentation of the material proceeds at a fairly leisurely pace and is roughly at the advanced undergraduate to beginning graduate level. To motivate various constructions and concepts, we have many examples and a lot of discussion that explains the intuition behind the scene. Furthermore, there are over 100 pictures throughout this monograph that help the reader visualize (undirected) wiring diagrams. Finally, to solidify one’s understanding of the subject, the reader may work through the problems in Chapter 14. There are enough problems there to keep one busy for a few days.

1.4. Chapter Summaries

This monograph is divided into three parts.

**Part 1:** Wiring Diagrams (Chapters 2–6)
This part contains the finite presentation theorems for the operad $\mathcal{WD}$ of wiring diagrams, the operad $\mathcal{WD}_*$ of normal wiring diagrams, the operad $\mathcal{WD}_0$ of strict wiring diagrams, and their algebras.

**Part 2:** Undirected Wiring Diagrams (Chapters 7–11)
This part contains the finite presentation theorems for the operad $\mathcal{UWD}$ and for their algebras.

**Part 3:** Maps Between Operads of Wiring Diagrams (Chapters 12–15)
This part contains the construction and description of various operad maps between the operads $\mathcal{WD}$, $\mathcal{WD}_*$, $\mathcal{WD}_0$, and $\mathcal{UWD}$. It also contains a chapter with a list of problems and a chapter with references for further reading.

Each part begins with a brief introduction and a reading guide. Below is a brief description of each chapter.

In Chapter 2, to keep this document self-contained, we first recall two equivalent definitions of a colored operad. The first definition is in terms of May’s operad structure map $\gamma$, and the other one is in terms of the $\circ_i$-compositions. After recalling the definition of a wiring diagram, we provide a proof of the fact from [RS13] that the collection of wiring diagrams $\mathcal{WD}$ is a colored operad. The main difference here is that we use the definition of a colored operad based on the $\circ_i$-compositions. In this monograph, we prefer to work with the $\circ_i$-compositions rather than May’s
operad structure map $\gamma$ because the $\circ_i$-compositions are more convenient in phrasing and verifying our finite presentation theorems.

In Chapter 3 we introduce 8 generating wiring diagrams and 28 elementary relations among them. On the one hand, one may regard this chapter as a long list of concrete examples of wiring diagrams and their operadic compositions. On the other hand, in later chapters we will see that these finite collections of generating wiring diagrams and elementary relations are sufficient to describe the operad $\mathcal{W}D$ of wiring diagrams, its variants $\mathcal{W}D_\bullet$ and $\mathcal{W}D_0$, and their algebras.

For the finite presentation theorems for the operad $\mathcal{W}D$ of wiring diagrams and its variants $\mathcal{W}D_\bullet$ and $\mathcal{W}D_0$, we will need to be able to decompose every wiring diagram in terms of the 8 generating wiring diagrams in a highly structured way. The purpose of Chapter 4 is to supply all the steps needed to establish such a decomposition.

The finite presentation theorems for the operad $\mathcal{W}D$ of wiring diagrams as well as its two variants $\mathcal{W}D_\bullet$ and $\mathcal{W}D_0$ are given in Chapter 5; see Theorems 5.2.11, 5.3.7, and 5.4.8. Since we are not working in the linear setting (e.g., of modules) where we can take quotients, we need to be extra careful in phrasing our finite presentations for the operads $\mathcal{W}D$, $\mathcal{W}D_\bullet$, and $\mathcal{W}D_0$. For this purpose, a crucial concept is that of a stratified presentation, which is the highly structured decomposition mentioned in the previous paragraph. The results in Chapter 4 guarantees the existence of a stratified presentation for each wiring diagram. This implies the finite generation parts of our finite presentation theorems for $\mathcal{W}D$, $\mathcal{W}D_\bullet$, and $\mathcal{W}D_0$. The relation parts of the finite presentation theorems are phrased in terms of our concept of an elementary equivalence. Roughly speaking, an elementary equivalence means replacing one side of either (i) an elementary relation in Chapter 3 or (ii) an operad associativity/unity axiom for the generating wiring diagrams, by the other side.

In Chapter 6 we discuss finite presentations for algebras over the operads $\mathcal{W}D$, $\mathcal{W}D_\bullet$, and $\mathcal{W}D_0$. In each case, the finite presentation for algebras is a consequence of the finite presentation theorem for the corresponding operad of wiring diagrams. To illustrate the finite presentation for $\mathcal{W}D$-algebras, we will describe the propagator algebra in terms of 8 generating structure maps and 28 generating axioms. To illustrate our finite presentation for $\mathcal{W}D_\bullet$-algebras, we will describe the algebra of discrete systems in terms of 7 generating structure maps and 28 generating axioms. To illustrate our finite presentation for $\mathcal{W}D_0$-algebras, we will similarly describe the algebra of open dynamical systems in terms of 4 generating structure maps and 8 generating axioms. This finishes Part 1 on wiring diagrams.

Part 2 begins with Chapter 7, where we first recall the notion of an undirected wiring diagram. Then we give a proof of the fact that the collection of undirected wiring diagrams forms an operad $\mathcal{U}W\mathcal{D}$. As in Chapter 2, the operad structure on $\mathcal{U}W\mathcal{D}$ as well as its proof are both given in terms of the $\circ_i$-compositions because
the finite presentation theorems are easier to phrase this way. One subtlety about
the operad UWD is that undirected wiring diagrams may have wasted cables (Def.
7.1.2), which are cables that are not soldered to any wires. As opposed to what
was stated in [Spi14] (Example 7.4.2.10), wasted cables cannot be excluded from
the definition of undirected wiring diagrams. In fact, wasted cables can actually be
created from operadic composition of undirected wiring diagrams without wasted
cables. We will make this point precise in Example 7.3.8.

Chapter 8 is the undirected analogue of Chapter 3. In this chapter, we describe
6 generating undirected wiring diagrams and 17 elementary relations among them. On
the one hand, one may regard this chapter as a long list of concrete examples of
undirected wiring diagrams and their operadic compositions. On the other hand,
in later chapters we will see that these finite collections of generating undirected
wiring diagrams and elementary relations are sufficient to describe the operad
UWD of undirected wiring diagrams.

Chapter 9 is the undirected analogue of Chapter 4. In this chapter, we show
that each undirected wiring diagram can be decomposed in terms of the generating
undirected wiring diagrams in a highly structured way. Such a decomposition is
needed to establish the finite presentation theorem for the operad UWD.

Chapter 10 is the undirected analogue of Chapter 5. In this chapter, we establish
the finite presentation theorem for the operad UWD of undirected wiring diagrams;
see Theorem 10.2.7. This result is phrased in terms of the generating undirected
wiring diagrams and an undirected version of an elementary equivalence.

Chapter 11 contains the finite presentation theorem for UWD-algebras. This
result is a consequence of the finite presentation theorem for the operad UWD.
It describes each UWD-algebra in terms of 6 generating structure maps and 17
generating axioms, almost all of which are trivial to check in practice. We will
illustrate this point with the relation algebra and the typed relational algebra from
[Spi13]. We will also provide a partial verification of Spivak’s conjecture regarding
the quotient-freeness of the relational algebra. This finishes Part 2 on undirected
wiring diagrams.

Part 3 begins with Chapter 12 in which we first construct the operad inclusions
WD_0 \rightarrow WD_\bullet \rightarrow WD. Recall that WD_\bullet is the operad of normal wiring diagrams–
i.e., those without delay nodes–and that WD_0 is the operad of strict wiring diagrams–
i.e., those without delay nodes and whose supplier assignments are bijections.
Then we construct an operad map \chi : WD_\bullet \rightarrow UWD, essentially by forgetting di-
rections, and its restriction \chi^0 : WD_0 \rightarrow UWD. For each of the operad maps \chi
and \chi^0, we compute precisely the image in UWD. In the terminology of Notation
9.1.1 the image of the operad map \chi consists of precisely the undirected wiring
diagrams without wasted cables and (0, \geq 2)-cables. The image of the operad map
\( \chi^0 \) consists of precisely the undirected wiring diagrams with only \((1, 1)\)-cables and \((2, 0)\)-cables.

In Chapter 13 we extend the operad map \( \chi : \text{WD} \rightarrow \text{UWD} \) to an operad map \( \rho : \text{WD} \rightarrow \text{UWD} \) that is defined for all wiring diagrams. We prove that the operad map \( \rho \) is surjective, so every undirected wiring diagram is the image of some wiring diagram. The operad map \( \rho \) is slightly subtle because wiring diagrams may have delay nodes, while undirected wiring diagrams do not seem to have an exact analogue of delay nodes. In fact, for this reason Rupel and Spivak [RS13] (Section 4.1) expressed doubt about the possibility that there be an operad map \( \text{WD} \rightarrow \text{UWD} \). We will see that delay nodes, far from being an obstruction, play a critical role in the surjectivity of the operad map \( \rho \).

Chapter 14 contains some problems about operads and (undirected) wiring diagrams arising from the earlier chapters. Chapter 15 contains some relevant references on categories, operads, props, and their applications in the sciences. This finishes Part 3.

### 1.5. References for the Main Results and Examples

The following table summarizes the key references for the various operads of (undirected) wiring diagrams and their finite presentation theorems.

| Operad of | Finite Presentation | Generators | Relations |
|-----------|---------------------|------------|-----------|
| WD        | wiring diagrams     | Theorem 2.3.11 | 8         | 28        |
| WD_       | normal wiring       | Theorem 5.2.11 | 7 (Def. 5.1.9) | 28 (Def. 5.3.30) |
|           | diagrams (Prop. 5.3.8) | Theorem 5.3.7 | 4 (Def. 5.3.6(1)) | 8 (Def. 5.4.7(5)) |
| WD_0      | strict wiring       | Theorem 5.4.8 | 4 (Def. 5.4.7(1)) | 8 (Def. 5.4.7(5)) |
|           | diagrams (Prop. 5.4.6) | Theorem 5.4.8 | 4 (Def. 5.4.7(1)) | 8 (Def. 5.4.7(5)) |
| UWD       | undirected wiring   | Theorem 10.2.7 | 6 (Def. 8.1.7) | 17 (Def. 8.2.18) |
|           | diagrams (Theorem 7.3.14) | Theorem 10.2.7 | 6 (Def. 8.1.7) | 17 (Def. 8.2.18) |

The following table summarizes the key references for the finite presentation theorems for algebras over the various operads of (undirected) wiring diagrams.
### 1. Introduction

| Algebras over Finite Presentation (Generators, Relations) | Key Example |
|----------------------------------------------------------|-------------|
| WD \[ (8, 28) \] (Def. 6.2.1) | propagator algebra (Theorem 6.3.16) |
| WD* \[ (7, 28) \] (Def. 6.4.1) | discrete systems (Theorem 6.5.12) |
| WD\(_0\) \[ (4, 8) \] (Def. 6.6.1) | open dynamical systems (Theorem 6.7.9) |
| UWD \[ (6, 17) \] (Def. 11.1.1) | (typed) relational algebra (Theorems 11.2.5 and 11.4.7) |

The following table summarizes the key references for the operad maps between the various operads of (undirected) wiring diagrams.

| Operad Map | Reference | Note/Image |
|-----------|-----------|------------|
| WD\(_0\) \[ ➔ \] WD* \[ ➔ \] WD | Prop. 12.1.7 | inclusions |
| WD* \[ ➔ \] \(\chi\) UWD | Theorem 12.2.4 | no (0,0)- and (0,\(\geq\)2)-cables (Theorem 12.4.1) |
| WD\(_0\) \[ ➔ \] \(\chi^o\) UWD | Theorem 12.5.1 | only (1,1)- and (2,0)-cables |
| WD \[ ➔ \] \(\rho\) UWD | Theorem 13.1.4 | surjective (Theorem 13.3.3) |
Part 1

Wiring Diagrams
The main purpose of this part is to describe the combinatorial structure of

(1) the operad $\text{WD}$ of wiring diagrams,

(2) the operad $\text{WD}_\bullet$ of normal wiring diagrams, and

(3) the operad $\text{WD}_0$ of strict wiring diagrams.

A normal wiring diagram is a wiring diagram without delay nodes. A strict wiring diagram is a normal wiring diagram whose supplier assignment is a bijection. For each of these three operads, we prove a finite presentation theorem that describes the operad in terms of a few operadic generators and a small number of generating relations.

Operads and wiring diagrams are recalled in Chapter 2. Operadic generators and generating relations for the operad $\text{WD}$ of wiring diagrams are presented in Chapter 3. Various decompositions of wiring diagrams are given in Chapter 4. Using the results in Chapters 3 and 4, the finite presentation theorems for the operads $\text{WD}$, $\text{WD}_\bullet$, and $\text{WD}_0$ are proved in Chapter 5. In Chapter 6, we prove the corresponding finite presentation theorems for $\text{WD}$-algebras, $\text{WD}_\bullet$-algebras, and $\text{WD}_0$-algebras and discuss the main examples of the propagator algebra, the algebra of discrete systems, and the algebra of open dynamical systems. Each finite presentation theorem for algebras describes the algebras in terms of finitely many generating structure maps and relations among these maps.

**Reading Guide:** In this reading guide we describe what can be safely skipped in Part 1 during the first reading. The purpose is to help the reader get to the main results and examples quicker without getting bogged down by all the technical details.

In Chapter 2, the reader who already knows about colored operads and categories may skip Section 2.1 and start reading about wiring diagrams from Def. 2.2.6. In Section 2.3 about the operad structure on $\text{WD}$, the reader may wish to skip the proofs of the Lemmas and just study the pictures. Section 3.2 about internal wasted wires may be skipped during the first reading.

In Chapter 4, the various decompositions of wiring diagrams are outlined in the introduction. The reader may read that introduction, followed by Motivation 4.1.4 and 4.1.9 and Examples 4.2.3 and 4.3.2 which provide pictures that illustrate the decompositions.

In Section 5.2, after the initial definitions and examples, the reader may wish to skip the proofs of Lemmas 5.2.8, 5.2.9, and 5.2.10 and go straight to Theorem 5.2.11, the finite presentation theorem for wiring diagrams.

The reader who already knows about operad algebras may skip Section 6.1.
This purpose of this chapter is to recall the definitions of colored operads and wiring diagrams. In Section 2.1 we recall two equivalent definitions of a colored operad, one in terms of the structure map $\gamma$ (2.1.3.2) and the other in terms of the $\circ_i$-compositions (2.1.10.1).

Wiring diagrams are defined in Section 2.2. The main difference between our definition of a wiring diagram and the original one in [RS13] is that we allow the wires to carry values in an arbitrary class $S$ instead of just the class of pointed sets. This added flexibility will be important in later chapters when we discuss operad algebras. Indeed, in Section 6.3 when we discuss the propagator algebra, we will take $S$ to be the class of pointed sets. On the other hand, in Section 6.7 when we discuss the algebra of open dynamical systems, we will take $S$ to be a set of representatives of isomorphism classes of second-countable smooth manifolds.

In Section 2.3 we define the operad structure on wiring diagrams in terms of $\circ_i$-compositions. Although we could also have defined this operad structure in terms of $\gamma$ as in [RS13], we chose to use $\circ_i$-compositions because the finite presentation theorems in Chapter 5 can be phrased and proved more easily using the latter.

2.1. Colored Operads

For brief discussion about classes in the set-theoretic sense, the reader is referred to [Hal74, Pin04]. In this monograph, the reader can safely take the word class to just mean a collection of objects, such as sets, pointed sets, and real functions. First we introduce some notations for the colors in a colored operad.

Definition 2.1.1. Suppose $S$ is a class.
(1) Denote by $\text{Prof}(S)$ the class of finite ordered sequences of elements in $S$. An element in $\text{Prof}(S)$ is called an $S$-profile or just a profile if $S$ is clear from the context.

(2) A typical $S$-profile of length $n$ is denoted by $\underline{s} = (s_1, \ldots, s_n)$ with $|\underline{s}|$ denoting its length.

(3) The empty $S$-profile is denoted by $\emptyset$.

(4) For $n \geq 0$ denote by $\text{Prof}^{\geq n}(S) \subseteq \text{Prof}(S)$ the sub-class of $S$-profiles of length at least $n$.

Motivation 2.1.2. Before we define an operad, let us first motivate its definition with a simple but important example. Suppose $X$ is a set and $\text{Map}(X^n, X)$ is the set of functions from $X^n = X \times \cdots \times X$, with $n \geq 0$ factors of $X$, to $X$. If $f \in \text{Map}(X^n, X)$ with $n \geq 1$ and $g_i \in \text{Map}(X^{m_i}, X)$ for each $1 \leq i \leq n$, then one can form the new function

$$f \circ (g_1, \ldots, g_n) \in \text{Map}(X^{m_1 + \cdots + m_n}, X)$$

by first applying the $g_i$'s simultaneously and then applying $f$. Moreover, we may even allow the inputs and the output of each function to be from different sets, i.e., functions $X_{c_1} \times \cdots \times X_{c_n} \to X_d$. In this case, the above composition is defined if and only if the outputs of the $g_i$'s match with the inputs of $f$.

A function $f \in \text{Map}(X_{c_1} \times \cdots \times X_{c_n}, X_d)$ may be depicted as follows.

When $n \geq 1$, the composition $f \circ (g_1, \ldots, g_n)$ corresponds to the 2-level tree:

Here each $g_i \in \text{Map}(X_{b_i^1} \times \cdots \times X_{b_{m_i}}, X_{c_i})$, $n \geq 1$, and each $m_i \geq 0$. Together with permutations of the inputs, the above collection of functions satisfies some associativity, unity, and equivariance conditions. An operad is an abstraction of this example that allows one to encode operations with multiple, possibly zero, inputs and one output and their compositions.
With the above motivation in mind, next we define colored operads. See, for example, \textit{Yau16} for more in-depth discussion of colored operads. For each integer \(n \geq 0\), the symmetric group on \(n\) letters is denoted by \(\Sigma_n\).

**Definition 2.1.3.** Suppose \(S\) is a class. An \textit{\(S\)-colored operad} \((O, 1, \gamma)\) consists of the following data.

1. For any \(d \in S\) and \(\underline{c} \in \text{Prof}(S)\) with length \(n \geq 0\), \(O\) is equipped with a class
   \[O(d^{\underline{c}}) = O_{(c_1, \ldots, c_n)}^{d}\]
   called the \textit{entry} of \(O\) with \textit{input profile} \(\underline{c}\) and \textit{output color} \(d\). An element in \(O(d^{\underline{c}})\) is called an \textit{n-ary element} in \(O\).

2. For \(\underline{c} \in \text{Prof}(S)\) as above and a permutation \(\sigma \in \Sigma_n\), \(O\) is equipped with a bijection
   \[
   O(d^{\underline{c}}) \xrightarrow{\gamma^\sigma} O(d^{\underline{c}\sigma})
   \]
   called the \textit{right action} or the \textit{symmetric group action}, in which
   \[
   \underline{c}\sigma = (c_{\sigma(1)}, \ldots, c_{\sigma(n)})
   \]
   is the right permutation of \(\underline{c}\) by \(\sigma\).

3. For each \(c \in S\), \(O\) is equipped with a specific element \(1_c \in O(c)\), called the \textit{c-colored unit}.

4. For \((\underline{d}, \underline{c}) \in \text{Prof}(S) \times S\) as above with \(n \geq 1\), suppose \(b_1, \ldots, b_n \in \text{Prof}(S)\) and \(\underline{b} = (b_1, \ldots, b_n) \in \text{Prof}(S)\) is their concatenation. Then \(O\) is equipped with a map
   \[
   O(\underline{d}^{\underline{c}}) \times \prod_{i=1}^{n} O(b_i^{c_i}) \xrightarrow{\gamma} O(\underline{d}^{\underline{c}})
   \]
   called the \textit{operadic composition}. For \(y \in O(\underline{d}^{\underline{c}})\) and \(x_i \in O(b_i^{c_i})\) for \(1 \leq i \leq n\), the image of the operadic composition is written as
   \[
   \gamma(y; x_1, \ldots, x_n) \in O(\underline{d}^{\underline{c}}).
   \]

This data is required to satisfy the following associativity, unity, and equivariance axioms.

**Associativity Axiom:** Suppose that:

- in (2.1.3.2),
  \[
  \underline{b}_j = (b_{j,1}^{\underline{b}_j}, \ldots, b_{j,k_j}^{\underline{b}_j}) \in \text{Prof}(S)
  \]
  has length \(k_j \geq 0\) for each \(1 \leq j \leq n\) such that at least one \(k_j > 0\);
- \(d_i^{\underline{c}} \in \text{Prof}(S)\) for each \(1 \leq j \leq n\) and \(1 \leq i \leq k_j\);
2. Wiring Diagrams

- for each $1 \leq j \leq n$,
  \[
  a_j = \begin{cases} \{a^j_1, \ldots, a^j_{k_j}\} & \text{if } k_j > 0, \\ \emptyset & \text{if } k_j = 0; \end{cases}
  \] (2.1.3.3)

- $a = (a_1, \ldots, a_n)$ is their concatenation.

Then the associativity diagram

\[
\begin{array}{ccc}
\mathrm{O}_2^{(d)} \times \left[ \prod_{j=1}^{n} \mathrm{O}_2^{(c_j)} \right] \times \prod_{j=1}^{n} \left[ \prod_{i=1}^{k_j} \mathrm{O}_2^{(a^j_i)} \right] \\ \downarrow \text{permute} \\ \mathrm{O}_2^{(d)} \times \prod_{j=1}^{n} \left[ \mathrm{O}_2^{(c_j)} \times \prod_{i=1}^{k_j} \mathrm{O}_2^{(a^j_i)} \right] \\

\end{array} \xrightarrow{\gamma} \begin{array}{ccc}
\mathrm{O}_2^{(d)} \times \prod_{j=1}^{n} \mathrm{O}_2^{(a^j)} \\
\end{array}
\] (2.1.3.4)

is commutative.

Unity Axioms: Suppose $d \in S$.

1. If $\mathfrak{c} = (c_1, \ldots, c_n) \in \text{Prof}(S)$ has length $n \geq 1$, then the right unity diagram

\[
\begin{array}{ccc}
\mathrm{O}_2^{(d)} \times \{\ast\}^n \\ \downarrow \text{(Id,n1c)} \\
\mathrm{O}_2^{(d)} \times \prod_{j=1}^{n} \mathrm{O}_2^{(c_j)} \\
\end{array} \xrightarrow{\gamma} \begin{array}{ccc}
\mathrm{O}_2^{(d)} \\
\end{array}
\] (2.1.3.5)

is commutative. Here $\{\ast\}$ is the one-point set, and $\{\ast\}^n$ is its $n$-fold product.

2. If $\mathfrak{b} \in \text{Prof}(S)$, then the left unity diagram

\[
\begin{array}{ccc}
\{\ast\} \times \mathrm{O}_2^{(d)} \\ \downarrow \text{(I_b,Id)} \\
\mathrm{O}_2^{(d)} \times \mathrm{O}_2^{(d)} \\
\end{array} \xrightarrow{\gamma} \begin{array}{ccc}
\mathrm{O}_2^{(d)} \\
\end{array}
\] (2.1.3.6)

is commutative.

Equivariance Axioms: Suppose that in (2.1.3.2) $|b_j| = k_j \geq 0$. 

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(1) For each permutation \( \sigma \in \Sigma_n \), the top equivariance diagram

\[
\begin{array}{c}
O^{(d)} \times \prod_{j=1}^{n} O^{(d)} \xrightarrow{(\sigma, \sigma^{-1})} O^{(d)} \\
\gamma \downarrow \hspace{1cm} \downarrow \gamma \\
O^{(d)} \xrightarrow{\sigma(k_1, \ldots, k_n)} O^{(d)}
\end{array}
\]

is commutative. Here \( \sigma(h, \ldots, k_n) \in \Sigma_{k_1 + \cdots + k_n} \) is the block permutation induced by \( \sigma \) that permutes the \( n \) consecutive blocks of lengths \( k_1, \ldots, k_n \), leaving the relative order within each block unchanged.

(2) Given permutations \( \tau_j \in \Sigma_{k_j} \) for \( 1 \leq j \leq n \), the bottom equivariance diagram

\[
\begin{array}{c}
O^{(d)} \times \prod_{j=1}^{n} O^{(d)} \xrightarrow{(\text{Id, } \tau_1)} O^{(d)} \\
\gamma \downarrow \hspace{1cm} \downarrow \gamma \\
O^{(d)} \xrightarrow{\tau_1 \oplus \cdots \tau_n} O^{(d)}
\end{array}
\]

is commutative. Here the block sum \( \tau_1 \oplus \cdots \oplus \tau_n \in \Sigma_{k_1 + \cdots + k_n} \) is the image of \( (\tau_1, \ldots, \tau_n) \) under the inclusion \( \Sigma_{k_1} \times \cdots \times \Sigma_{k_n} \rightarrow \Sigma_{k_1 + \cdots + k_n} \).

A colored operad is a \( C \)-colored operad for some class \( C \). We will also call a colored operad simply as an operad.

**Remark 2.1.4.** A 1-colored operad \([\text{Kel05], [MSS02], [May72], [May97]}\), with \( S = \{ * \} \), is usually called an operad or a symmetric operad. The underline notation for \( \underline{\bullet} \in \text{Prof}(S) \) and the vertical notation for \( (\underline{\bullet}) \in \text{Prof}(S) \times S \) originated in \([\text{JY09}]\). See \([\text{Yau16}]\) (section 9.6) for more discussion of these notations. In a 1-colored operad \( O \), the entry of \( O \) whose input profile has length \( n \) is denoted \( O(n) \).

**Example 2.1.5 (Endomorphism Operads).**

(1) Each set \( X \) yields a 1-colored operad \( \text{End}(X) \), called the endomorphism operad, whose \( n \)th entry is the set \( \text{Map}(X^n, X) \) of functions with the operad structure in Motivation 2.1.2.

(2) More generally, for a non-empty class \( C \), suppose \( X = \{ X_c \}_{c \in C} \) is a \( C \)-indexed class of sets. Then there is a \( C \)-colored endomorphism operad whose \( (\underline{\bullet}) \)-entry is the set of functions \( \text{Map}(X_{c_1} \times \cdots \times X_{c_n}, X_d) \) with the operad structure in Motivation 2.1.2.

**Example 2.1.6 (Monoids as Operads).** Recall that a monoid is a triple \((A, \mu, 1)\) consisting of a set \( A \), a binary operation \( \mu : A \times A \rightarrow A \), and an element \( 1 \in A \) such that the following two conditions are satisfied.

**Associativity:** \( \mu(\mu(a, b), c) = \mu(a, \mu(b, c)) \) for all \( a, b, c \in A \).
Unity: \( \mu(1, a) = a = \mu(a, 1) \).

A monoid is uniquely determined by the operad \( O \) with \( O(1) = A, O(n) = \emptyset \) for all \( n \neq 1 \), \( \mu \) as the only non-trivial operadic composition, and \( 1 \in A \) as the unit.

**Example 2.1.7 (Associative and Commutative Operads).**

1. There is a 1-colored operad \( A_n \), called the *associative operad*, whose \( n \)th entry is the symmetric group \( \Sigma_n \) for each \( n \geq 0 \) with group multiplication as the symmetric group action and the identity \( e \in \Sigma_1 \) as the unit. Given permutations \( \sigma, \tau_i \in \Sigma_n \) with \( n \geq 1 \) and \( \tau_i \in \Sigma_{k_i} \) for each \( 1 \leq i \leq n \), the operadic composition is given by

\[
\gamma(\sigma; \tau_1, \ldots, \tau_n) = \sigma(k_1, \ldots, k_n) \circ (\tau_1 \oplus \cdots \oplus \tau_n) \in \Sigma_{k_1 + \cdots + k_n}.
\]

Here \( \sigma(k_1, \ldots, k_n) \in \Sigma_{k_1 + \cdots + k_n} \) is the block permutation in \( \Sigma_{k_1 + \cdots + k_n} \), and \( \tau_1 \oplus \cdots \oplus \tau_n \in \Sigma_{k_1 + \cdots + k_n} \) is the block sum in \( \Sigma_{k_1 + \cdots + k_n} \). The algebras of the operad \( A_n \), in the sense of Def. 6.1.2, are precisely monoids.

2. There is a 1-colored operad \( \text{Com} \), called the *commutative operad*, whose \( n \)th entry is a single point \( * \) for each \( n \geq 0 \). Its operad structure maps are all trivial maps, and its algebras, in the sense of Def. 6.1.2, are precisely commutative monoids, i.e., monoids whose multiplication maps are commutative.

**Example 2.1.8 (Operad of Graph Operations).**

We now discuss an operad from non-commutative probability theory [Ma16]. By a *finite directed graph*, or just a graph, we mean a pair of finite sets \((V, E)\) with \( V \) non-empty such that an element in \( E \) is an ordered pair \((u, v)\) in \( V^2 \), where each such ordered pair may appear in \( E \) more than once. Elements in \( V \) and \( E \) are called vertices and edges, respectively, and an edge \( e = (u, v) \) is said to have initial vertex \( u \) and terminal vertex \( v \), denoted \( e : u \rightarrow v \). An edge of the form \((v, v)\) is called a loop at \( v \). An edge of the form \((u, v)\) or \((v, u)\) is said to connect \( u \) and \( v \). We say that a graph \((V, E)\) is connected if for each pair of distinct vertices \( u \) and \( v \), there exist edges \( e_i \) for \( 1 \leq i \leq n \) for some \( n \geq 1 \) such that each \( e_i \) connects \( v_{i-1} \) and \( v_i \) with \( v_0 = u \) and \( v_n = v \).

A graph operation is a connected graph \((V, E)\) equipped with

1. an ordering \( \sigma \) of the set \( E \) of edges and
2. two possibly equal vertices in and out, called the input and the output.

An isomorphism of graph operations is a pair of bijections \((V, E) \rightarrow (V', E')\) on vertices and edges that preserves the initial and the terminal vertices of each edge, the ordering on edges, and the input and the output. We only consider graph operations up to isomorphisms. That is, if there is an isomorphism

\[(V, E, \sigma, \text{in}, \text{out}) \rightarrow (V', E', \sigma', \text{in}', \text{out}')\]

of graph operations, then we consider them to be the same. For each \( n \geq 0 \), denote by \( \text{GrOp}_n \) the set of graph operations with \( n \) edges. So \( \text{GrOp}_0 \) contains only the
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Graph with one vertex, which is both the input and the output, and no edges. Here is a graph operation with two vertices and four edges, two of which are loops:

There is an operad structure on graph operations given by edge substitution as follows. Suppose \( G \in \text{GrOp}_n \) with \( n \geq 1 \) and \( G_i \in \text{GrOp}_{m_i} \) for \( 1 \leq i \leq n \). Then the operadic composition

\[
G(G_1, \ldots, G_n) \in \text{GrOp}_{m_1 + \cdots + m_n}
\]
is obtained from \( G \) by replacing the \( i \)th edge \( e_i \) in \( G \) by \( G_i \) and by identifying the initial (resp., terminal) vertex of \( e_i \) with the input (resp., output) of \( G_i \). The edge ordering of the operadic composition is induced by those of \( G \) and of the \( G_i \)'s. The input and the output are inherited from \( G \). The symmetric group action on \( \text{GrOp}_n \) is given by permutation of the edge ordering. The operadic unit is the graph operation in \( \text{in} \rightarrow \text{out} \) with two vertices and one edge from the input to the output.

For example, suppose \( G, H, \) and \( K \) are the following graph operations in \( \text{GrOp}_2 \):

Then the operadic composition \( G(H, K) \) is the graph operation with four edges above. The algebras of the operad \( \text{GrOp} \) are closely related to traffic spaces and non-commutative probability, as we will discuss in Example 6.1.8 below.

Due to the presence of the colored units, a colored operad can also be defined in terms of a binary product, called the \( \circ_i \)-composition, which leads to axioms that are sometimes easier to check in practice and that we will use in most of the rest of this monograph. In the one-colored linear setting, this alternative formulation of an operad was first made explicit in [Mar96].

Motivation 2.1.9. Using functions as in Motivation 2.1.2, the operadic \( \circ_i \)-compositions can be visualized as follows. Suppose

\[
f \in \text{Map}(X_{c_1} \times \cdots \times X_{c_n}, X_d) \quad \text{and} \quad g \in \text{Map}(X_{b_1} \times \cdots \times X_{b_i}, X_{c_j})
\]
are functions for some \( 1 \leq i \leq n \), pictorially depicted as follows.
Then their $o_i$-composition

$$f \circ_i g = f \circ (\text{Id}^{i-1}, g, \text{Id}^{n-i})$$

is the picture

in which the output of $g$ is used as the $i$th input of $f$. The operadic $o_i$-composition is an abstraction of this $f \circ_i g$ of functions.

With the above motivation in mind, we now recall this alternative formulation of an operad. The elementary relations in Section 3.3 are almost all stated in terms of the $o_i$-compositions in the following definition.

**Definition 2.1.10.** Suppose $S$ is a class. An $S$-colored operad $(O, 1, \circ)$ consists of the following data.

1. It has the same data as in (1)–(3) in Def. 2.1.3.
2. For each $d \in S$, $\mathcal{C} = (c_1, \ldots, c_n) \in \text{Prof}(S)$ with length $n \geq 1$, $b \in \text{Prof}(S)$, and $1 \leq i \leq n$, it is equipped with a map

$$O(d) \times O(c_i) \xrightarrow{o_i} O(d)$$

(2.1.10.1)

called the $o_i$-composition, where

$$\mathcal{C} \circ_i b = \left(c_1, \ldots, c_{i-1}, b, c_{i+1}, \ldots, c_n\right).$$

(2.1.10.2)

This data is required to satisfy the following associativity, unity, and equivariance axioms. Suppose $d \in S$, $\mathcal{C} = (c_1, \ldots, c_n) \in \text{Prof}(S)$, $b \in \text{Prof}(S)$ with length $|b| = m$, and $g \in \text{Prof}(S)$ with length $|g| = l$.

**Associativity Axioms:** There are two associativity axioms.
2.1. Colored Operads

(1) Suppose \( n \geq 2 \) and \( 1 \leq i < j \leq n \). Then the horizontal associativity diagram

\[
\begin{array}{c}
\xymatrix{
O(\underline{d}) \times O(\underline{c}_i) \times O(\underline{c}_j) \ar[r]^{(\circ, \text{Id})} \ar[d]^\cong & O(\underline{d}) \times O(\underline{c}_j) \\
O(\underline{d}) \times O(\underline{c}_i) \times O(\underline{c}_j) \ar[r]^{\circ_{j-1+i}} & O(\underline{d}) \times O(\underline{c}_j)
}
\end{array}
\]

is commutative.

(2) Suppose \( n, m \geq 1 \), \( 1 \leq i \leq n \), and \( 1 \leq j \leq m \). Then the vertical associativity diagram

\[
\begin{array}{c}
\xymatrix{
O(\underline{d}) \times O(\underline{c}_i) \times O(\underline{c}_j) \ar[r]^{(\text{Id}, \circ)} \ar[d]^{\cong} & O(\underline{d}) \times O(\underline{c}_j) \\
O(\underline{d}) \times O(\underline{c}_i) \times O(\underline{c}_j) \ar[r]^{\circ_{j-1+i}} & O(\underline{d}) \times O(\underline{c}_j)
}
\end{array}
\]

is commutative.

**Unity Axioms:** There are two unity axioms.

(1) The left unity diagram

\[
\begin{array}{c}
\xymatrix{
\{ \ast \} \times O(\underline{d}) \ar[r]^{(\text{Id}, \text{Id})} \ar[d]^\cong & O(\underline{d}) \times O(\underline{d}) \\
\{ \ast \} \times O(\underline{d}) \ar[r]^{\circ_1} & O(\underline{d})
}
\end{array}
\]

is commutative.

(2) If \( n \geq 1 \) and \( 1 \leq i \leq n \), then the right unity diagram

\[
\begin{array}{c}
\xymatrix{
O(\underline{d}) \times \{ \ast \} \ar[r]^{(\text{Id}, 1_i)} \ar[d]^\cong & O(\underline{d}) \times O(\underline{c}_i) \\
O(\underline{d}) \ar[r]^{\circ_i} & O(\underline{d})
}
\end{array}
\]

is commutative.
Equivariance Axiom: Suppose $|\underline{c}| = n \geq 1$, $1 \leq i \leq n$, $\sigma \in \Sigma_n$, and $\tau \in \Sigma_m$. Then the equivariance diagram

$$O^{(d)}(\underline{c}; L) \times O^{(c_{\sigma(i)}; L)} \xrightarrow{\sigma; \tau} O^{(d)}(\underline{c}; L)$$ (2.1.10.7)

is commutative, where

$$\sigma \circ_i \tau = \sigma(1^{i-1}, m, 1^{n-i})(1^{i-1} \oplus \tau \oplus 1^{n-i}) \in \Sigma_{n+m-1}.$$

On the right side, the block sum permutes the interval $[i, i + m - 1]$ via $\tau$. The block sum permutation induced by $\sigma$ regards the interval $[i, i + m - 1]$ as a single block, within which the relative order is unchanged.

Each $\circ_i$-composition is also called an operadic composition or just a composition.

Remark 2.1.11. Without the symmetric group action (2.1.3.1) and the equivariance axiom (2.1.10.7), a non-symmetric colored operad as in Def. 2.1.10 is exactly a multicategory as defined by Lambek [Lam69] (p.103-105). In [Lam69]:

1. The elements in an entry $O^{(d)}(\underline{c})$ of a colored operad $O$ are called multimaps.
2. The $\circ_i$-composition (2.1.10.1) is called a substitution or a cut.
3. The horizontal associativity axiom (2.1.10.3) is called the commutative law.
4. The vertical associativity axiom (2.1.10.4) is called the associative law.

The reader is cautioned that there are several typographical errors in [Lam69] (p.104-105) in the definition of a multicategory.

Due to the presence of the colored units, the two definitions of a colored operad are in fact equivalent.

Proposition 2.1.12. Definitions 2.1.3 and 2.1.10 of an $S$-colored operad are equivalent.

Proof. In the 1-colored case, a proof can be found in [Mar08] (Prop. 13). For the general colored case, the proof is similar and can be found in, e.g., [Yau16] (Section 16.4). The correspondence goes as follows. Given the operadic composition $\gamma$ (2.1.3.2), $y \in O^{(d)}(\underline{c})$ with $|\underline{c}| = n \geq 1$, and $x \in O^{(d)}(\underline{c})$ with $1 \leq i \leq n$, one defines the $\circ_i$-composition as

$$y \circ_i x = \gamma\left(y, \underbrace{1_{c_1}, \ldots, 1}_{\emptyset \text{ if } i = 1}, x, \underbrace{1_{c_{i+1}}, \ldots, 1}_{\emptyset \text{ if } i = n}\right).$$
2.2. Defining Wiring Diagrams

Conversely, given the $\circ_i$-compositions \([2.1.10.1]\), $y \in \mathcal{O}(\underline{\gamma})$ with $|\underline{\gamma}| = n \geq 1$, and $x_i \in \mathcal{O}(\underline{\gamma})$ for $1 \leq i \leq n$ with $k_i = |\underline{h}_i|$, one defines the operadic composition $\gamma$ as

$$\gamma(y; x_1, \ldots, x_n) = \left( (y \circ_1 x_1) \circ_{k_1+1} x_2 \cdots \right) \circ_{k_1+\cdots+k_{n-1}+1} x_n.$$ (2.1.12.1)

On the right side, every pair of parentheses starts on the left. □

2.2. Defining Wiring Diagrams

The operad of wiring diagrams $\mathcal{WD}$ has Box$\Sigma$ as its class of colors. So before we define wiring diagrams, we first define Box$\Sigma$. We begin by recalling the basic definition of a category. The reader may consult [Awo10, Lei14, Mac98] for more in-depth discussion of category theory. In this monograph, we do not need anything fancy from category theory. All that the reader needs to know is that a category consists of a collection of objects, such as sets, or finite sets, and maps between them that can be composed and that satisfy some natural unity and associativity axioms with respect to compositions.

Motivation 2.2.1. To motivate the definition of a category, consider the collection of groups and group homomorphisms. Given group homomorphisms $f : G_1 \rightarrow G_2$ and $g : G_2 \rightarrow G_3$, there is a composition $g \circ f : G_1 \rightarrow G_3$. The identity map of each group serves as the identity for composition. Furthermore, composition of group homomorphisms is associative, in the sense that given a group homomorphism $h : G_3 \rightarrow G_4$, there is an equality

$$(h \circ g) \circ f = h \circ (g \circ f)$$

of group homomorphisms. One can think of a category as an abstraction of the collection of groups, group homomorphisms, their composition, and the unity and the associativity axioms governing composition.

Definition 2.2.2. A category $\mathcal{C}$ consists of the following data.

- **Objects**: It is equipped with a collection $\text{Ob}(\mathcal{C})$ of objects. For an object $a$ in $\mathcal{C}$, we will write either $a \in \text{Ob}(\mathcal{C})$ or simply $a \in \mathcal{C}$.

- **Morphisms**: For any objects $a, b \in \text{Ob}(\mathcal{C})$, it is equipped with a collection $\mathcal{C}(a, b)$ of morphisms with domain $a$ and codomain $b$. A morphism $f$ in $\mathcal{C}(a, b)$ is usually denoted by $f : a \rightarrow b$ and is also called a map from $a$ to $b$.

- **Composition**: For any objects $a, b, c \in \text{Ob}(\mathcal{C})$ and morphisms $f : a \rightarrow b$ and $g : b \rightarrow c$, it is equipped with a morphism $g \circ f : a \rightarrow c$, called the composition of $f$ and $g$.

- **Identities**: Each object $a \in \text{Ob}(\mathcal{C})$ is equipped with a morphism $1_a : a \rightarrow a$, called the identity morphism of $a$. 
The above data is required to satisfy the following axioms.

**Unity:** For any objects \(a, b, c \in \text{Ob}(C)\) and morphisms \(g : a \rightarrow b\) and \(h : c \rightarrow a\), there are equalities of morphisms

\[
g \circ 1_a = g \in C(a, b) \quad \text{and} \quad 1_a \circ h = h \in C(c, a).
\]

**Associativity:** For any objects \(a, b, c, d \in \text{Ob}(C)\) and morphisms \(f : a \rightarrow b\), \(g : b \rightarrow c\), and \(h : c \rightarrow d\), there is an equality of morphisms

\[
(h \circ g) \circ f = h \circ (g \circ f)
\]

in \(C(a, d)\).

**Example 2.2.3.** Here are some basic examples of categories. In each case, the identity morphisms and the composition are the obvious ones.

1. There is an empty category with no objects and no morphisms.
2. There is a category \(*\) with only one object \(*\) and only the identity morphism of \(*\).
3. There is a category \(\text{Set}\) whose objects are sets and whose morphisms are functions between sets.
4. There is a category \(\text{Fin}\) whose objects are finite sets and whose morphisms are functions between finite sets. Given any disjoint finite sets \(X_1, \ldots, X_n\), their coproduct \(\bigsqcup_{i=1}^n X_i\) is the finite set given by their disjoint union. If the \(X_i\)'s are not disjoint, we can still define their coproduct, but we must first replace each \(X_i\) (or just the ones with \(i \geq 2\)) by an \(X'_i\) equipped with a bijection to \(X_i\) such that the resulting \(X'_1, \ldots, X'_n\) are disjoint. Then the coproduct \(\bigsqcup_{i=1}^n X_i\) is defined as the disjoint union of the \(X'_i\) for \(1 \leq i \leq n\), and it is well-defined up to isomorphism. If \(n = 0\) then the coproduct is defined as the empty set \(\emptyset\).

In what follows, if the identity morphisms and the composition are obvious, then we will omit mentioning them.

**Example 2.2.4.** A monoid \((A, \mu, 1)\) (Example 2.1.6) is a category with one object, whose only morphism set is \(A\). Composition and identity are those of \(A\), i.e., the multiplication \(\mu\) and the unit element \(1\). Therefore, one can think of a category as a monoid with multiple objects.

**Example 2.2.5.** Suppose \(O\) is an \(S\)-colored operad (Def. 2.1.3). Then \(O\) determines a category \(C\) whose objects are the elements in \(S\). For \(c, d \in S\) the morphism object \(C(c, d)\) is \(O(^d_c)\), and the identity morphism of \(c\) is the \(c\)-colored unit of \(O\). Composition in \(C\) is the restriction of the operadic composition in \(O\). Therefore, one can think of a colored operad as a generalization of a category in which the domain of each morphism is a finite sequence of objects.
For wiring diagrams, we will usually consider finite sets in which each element is allowed to carry a value of some kind. The precise notion is given in the following definition.

**Definition 2.2.6.** Suppose $S$ is a non-empty class, and $\text{Fin}$ is the category of finite sets and functions between them.

1. Denote by $\text{Fin}_S$ the category in which:
   - an object is a pair $(X, v)$ with $X \in \text{Fin}$ and $v : X \to S$ a function;
   - a map $(X, v_X) \to (Y, v_Y)$ is a function $X \to Y$ such that the diagram
     \[
     \begin{array}{ccc}
     X & \xrightarrow{v_X} & Y \\
     v_X \downarrow & & \downarrow v_Y \\
     S & & S
     \end{array}
     \]
     (2.2.6.1)

     is commutative.

2. An object $(X, v) \in \text{Fin}_S$ is called an $S$-finite set.

3. For $(X, v) \in \text{Fin}_S$, we call $v$ the value assignment for $X$. For each $x \in X$, $v(x) \in S$ is called the value of $x$.

4. If $(X_i, v_i) \in \text{Fin}_S$ for $1 \leq i \leq n$, then their coproduct $X = \bigsqcup_{i=1}^n X_i \in \text{Fin}_S$ has value assignment $\bigsqcup_{i=1}^n v_i$.

5. The empty $S$-finite set is denoted by $\emptyset$.

**Definition 2.2.7.** Suppose $S$ is a non-empty class.

1. An $S$-box is a pair $X = (X^{\text{in}}, X^{\text{out}}) \in \text{Fin}_S \times \text{Fin}_S$. If $S$ is clear from the context, then we will drop $S$ and call $X$ a box.
   - An element of $X^{\text{in}}$ is called an input of $X$.
   - An element of $X^{\text{out}}$ is called an output of $X$.
   - We write $v = v_X : X^{\text{in}} \cup X^{\text{out}} \to S$ for the value assignment for $X$.

2. The class of $S$-boxes is denoted by $\text{Box}_S$.

3. The empty $S$-box, denoted by $\emptyset$, is the $S$-box with $\emptyset^{\text{in}} = \emptyset^{\text{out}}$ the empty set.

**Convention 2.2.8.** From now on, whenever $\text{Fin}_S$ or $\text{Box}_S$ is used, we always assume that the class $S$ is non-empty.

**Remark 2.2.9.** In [Spi15] (Def. 3.1) an $S$-box is called a signed finite set. It is a slight generalization of what appears in [RS13, VSL15]. In [RS13] $S$ is the class of pointed sets, where an $S$-box is called a black box. In [VSL15] $S$ is a set of representatives of isomorphism classes of second-countable smooth manifolds and smooth maps, or more generally the class of objects in a category with finite products.
Convention 2.2.10. For the purpose of visualization, an S-box $X$ will be drawn as follows.

\begin{align}
\begin{array}{c}
\text{X}^{\text{in}} \\
\text{or} \\
\text{X}^{\text{out}}
\end{array}
\end{align}

On the left, the inputs of $X$ are depicted as arrows going into the box, and the outputs of $X$ are depicted as arrows leaving the box. Alternatively, if we do not need to specify the sizes of $X^{\text{in}}$ and $X^{\text{out}}$, then we depict them using a generic arrow $\Rightarrow$, as in the picture on the right. The value of each $x \in X^{\text{in}} \cup X^{\text{out}}$ is either not depicted in the picture for simplicity, or it is written near the corresponding arrow.

Definition 2.2.11. Suppose $X_1, \ldots, X_n$ are S-boxes for some $n \geq 0$. Define the S-box $X = \coprod_{i=1}^n X_i$, called the coproduct, as follows.

1. If $n = 0$, then $X = \emptyset$, the empty S-box.
2. If $n \geq 1$, then:

\begin{align}
X^{\text{in}} &= \prod_{i=1}^n X_i^{\text{in}}, \\
X^{\text{out}} &= \prod_{i=1}^n X_i^{\text{out}}, \quad \text{and} \\
v_X &= \prod_{i=1}^n v_{X_i}.
\end{align}

Motivation 2.2.12. Before we define wiring diagrams, let us first provide a motivating example. A typical wiring diagram looks like this:

There is an output box $Y$ (the outermost box in the picture), a finite number of input boxes $X$ (which the above picture only has one), and a finite number of delay nodes (which the above picture again only has one). To make sense of such a picture, first of all, for each output $y^i$ of $Y$ we need to specify where the arrow is coming from. In the example above, $y^1$ comes from $x^1$, and both $y^2$ and $y^3$ come from the delay node $d$. We will say that each $y^i$ is a demand wire, and $y^1$ (resp., $y^2$ and $y^3$) is supplied by the supply wire $x^1$ (resp., $d$).

Similarly, for each input $x_i$ of $X$ and the delay node $d$, we again need to specify where the arrow is coming from. So $d$ is also a demand wire, and by tracing the arrow ending at $d$ backward, we see that it is supplied by the supply wire $y_1$. Starting at the input $x_1$ (resp., $x_2$ and $x_3$) and tracing the arrow backward, we see that it
is supplied by \(x^1\) (resp., \(y_1\) and \(d\)). We will come back to this example precisely in Example 2.2.18.1 below.

The above exercise tells us that the outputs of \(Y\), the inputs of \(X\), and the delay nodes are demand wires, in the sense that each of their elements demands a supply wire. The supply wires consist of the inputs of \(Y\), the outputs of \(X\), and the delay nodes. Each supply wire may supply multiple demand wires or none at all. For instance, in the above example, the supply wire \(x^1\) supplies both the demand wires \(x_1\) and \(y_1^1\). On the other hand, the supply wires \(y_2\) and \(x^2\) do not supply to any demand wires at all. We will call them wasted wires.

To avoid pathological situations, one requirement of a wiring diagram is that a demand wire in the outputs of \(Y\) should not be supplied by a supply wire in the inputs of \(Y\). In other words, we exclude pictures like this

![Bad Wiring Diagram]

in which the demand wire \(y'\) is directly supplied by the supply wire \(y\). So we insist that an output of \(Y\) be supplied by either an output of an input box \(X\) or a delay node \(d\). We will call this the non-instantaneity requirement.

Wiring diagrams will be defined as equivalence classes of prewiring diagrams, as defined below.

**Definition 2.2.13.** Suppose \(S\) is a class. An \(S\)-prewiring diagram is a tuple

\[
\varphi = (\mathbf{X}, \mathbf{Y}, \mathbf{DN}, v, s)
\]

consisting of the following data.

1. \(\mathbf{Y} = (Y^{\text{in}}, Y^{\text{out}}) \in \text{Box}_S\), called the output box of \(\varphi\).
   - An element in \(Y^{\text{in}}\) is called a global input for \(\varphi\).
   - An element in \(Y^{\text{out}}\) is called a global output for \(\varphi\).
2. \(\mathbf{X} = (X_1, \ldots, X_n)\) is a Box\(_S\)-profile for some \(n \geq 0\); i.e., each \(X_i \in \text{Box}_S\).
   - We call \(X_i\) the \(i\)th input box of \(\varphi\).
   - Denote by \(X = \bigsqcup_{i=1}^n X_i \in \text{Box}_S\) the coproduct.
3. \((\mathbf{DN}, v) \in \text{Fin}_S\) is an \(S\)-finite set. An element of \(\mathbf{DN}\) is called a delay node. Define:
   - \(\text{Dm} = Y^{\text{out}} \sqcup X^{\text{in}} \sqcup \mathbf{DN} \in \text{Fin}_S\). An element of \(\text{Dm}\) is called a demand wire in \(\varphi\).
   - \(\text{Sp} = Y^{\text{in}} \sqcup X^{\text{out}} \sqcup \mathbf{DN} \in \text{Fin}_S\). An element of \(\text{Sp}\) is called a supply wire in \(\varphi\).

Furthermore:
• When DN is regarded as a subset of Dm, an element in \( X^{in} \cup DN \) is called an *internal input* for \( \varphi \).
• When DN is regarded as a subset of \( Sp \), an element in \( X^{out} \cup DN \) is called an *internal output* for \( \varphi \).

(4) With a slight abuse of notation, we write

\[
\begin{array}{c}
\text{Dm} \sqcup_{\text{DN}} \text{Sp} = Y^{in} \sqcup X^{out} \sqcup X^{in} \sqcup X^{out} \sqcup DN \xrightarrow{v} S
\end{array}
\]

for the coproduct of the value assignments for \( X, Y, \) and DN.

(5) \( s : Dm \rightarrow Sp \in \text{Fin}_S \) is a map, called the *supplier assignment* for \( \varphi \), such that

\[
y \in Y^{out} \subseteq Dm \quad \text{implies} \quad s(y) \in Sp \setminus Y^{in} = X^{out} \cup DN.
\]

- The condition (2.2.13.2) is called the *non-instantaneity requirement*.
- For \( w \in Dm \), we call \( s(w) \in Sp \) the supplier or the supply wire of \( w \). So non-instantaneity says that the supply wire of a global output cannot be a global input.
- A supply wire \( w \in Y^{in} \) that does not belong to the image of the supplier assignment \( s \) is called an *external wasted wire*. The set of external wasted wires in \( \varphi \) is denoted by \( \varphi_{w}^{-} \).
- A supply wire \( w \in X^{out} \cup DN \) that does not belong to the image of the supplier assignment \( s \) is called an *internal wasted wire*. The set of internal wasted wires in \( \varphi \) is denoted by \( \varphi_{w}^{+} \).

If \( S \) is clear from the context, then we will drop \( S \) and call \( \varphi \) a *prewiring diagram*. If we need to emphasize \( \varphi \), then we will use subscripts such as \( Dm_{\varphi}, Sp_{\varphi}, \) and \( s_{\varphi} \).

**Remark 2.2.14.** In the constructions that follow, the compatibility of the value assignments with the various supplier assignments are usually immediate because, in each prewiring diagram, the supplier assignment \( s : Dm \rightarrow Sp \in \text{Fin}_S \). Therefore, we will omit checking such compatibility.

**Definition 2.2.15.** Suppose \( S \) is a class, \( \varphi = (X, Y, DN, v, s) \) is an \( S \)-prewiring diagram as in (2.2.13.1), and \( \varphi' = (X, Y, DN', v', s') \) is another \( S \)-prewiring diagram with the same input boxes \( X \) and output box \( Y \).

(1) An *equivalence* \( f : \varphi \rightarrow \varphi' \) is an isomorphism \( f_0 : (DN, v) \rightarrow (DN', v') \in \text{Fin}_S \) such that the diagram

\[
\begin{array}{ccc}
Y^{out} \sqcup X^{in} \sqcup DN = Dm_{\varphi} & \xrightarrow{id \sqcup id \sqcup f_0} & Dm_{\varphi'} = Y^{out} \sqcup X^{in} \sqcup DN' \\
\downarrow s_{\varphi} & & \downarrow s_{\varphi'} \\
Y^{in} \sqcup X^{out} \sqcup DN = Sp_{\varphi} & \xrightarrow{id \sqcup id \sqcup f_0} & Sp_{\varphi'} = Y^{in} \sqcup X^{out} \sqcup DN'
\end{array}
\]

in \( \text{Fin}_S \) is commutative.
2.2. Defining Wiring Diagrams

(2) We say that $\varphi$ and $\varphi'$ are equivalent if there exists an equivalence $\varphi \longrightarrow \varphi'$.

(3) An $S$-wiring diagram is an equivalence class of $S$-prewiring diagrams. If $S$ is clear from the context, we will drop $S$ and just say wiring diagram.

(4) The class of $S$-wiring diagrams with input boxes $X = (X_1, \ldots, X_n)$ and output box $Y$ is denoted by

$$\text{WD}^{(1)}_X \quad \text{or} \quad \text{WD}(X_{i_1 \ldots i_n})$$

The class of all $S$-wiring diagrams is denoted by $\text{WD}$. If we want to emphasize $S$, then we will write $\text{WD}^S$.

Convention 2.2.16. To simplify the presentation, we usually suppress the difference between a prewiring diagram and a wiring diagram. In any given wiring diagram, $\text{DN}$ is a finite set in which each element $d$ is equipped with a value $v(d) \in S$.

Unless otherwise specified, in the rest of this book, we will always use this representative of a wiring diagram. For a wiring diagram $\varphi \in \text{WD}^{(1)}_X$, we will sometimes draw it as

$$\begin{array}{c}
Y_{\text{in}} \xrightarrow{\varphi} Y_{\text{out}} \\
\text{or}
\end{array}$$

without drawing the input boxes $X$, the delay nodes, and the supplier assignment.

Remark 2.2.17. Def. 2.2.15 of an $S$-wiring diagram is a slight generalization of the one given in [RS13], where $S$ was taken to be the class of pointed sets. Note that when $S$ is a proper class (e.g., the class of pointed sets), the collection $\text{WD}^{(1)}_X$ (2.2.15.1) is also a proper class, not a set. This is the reason why in Def. 2.1.3 we allow $O^{(1)}_S$ to be a class, in contrast to what was stated in [RS13] (Def. 2.1.2B).

Example 2.2.18. Suppose $S$ is a non-empty class and:

- $X_{\text{in}} = \{x_1, x_1, x_3\}$, $X_{\text{out}} = \{x^1, x^2\}$, $Y_{\text{in}} = \{y_1, y_2\}$, $Y_{\text{out}} = \{y^1, y^2, y^3\}$, and $\text{DN} = \{d\}$;
- $v(x_2) = v(x_3) = v(y_1) = v(y^2) = v(y^3) = v(d) \in S$;
- $v(x_1) = v(x^1) = v(y^1) \in S$, and $v(x^2)$ and $v(y_2)$ in $S$ are arbitrary;
- $s(x_1) = s(y^1) = x^1$, $s(x_2) = s(d) = y_1$, and $s(x_3) = s(y^2) = s(y^3) = d$. 

Then the above data defines a wiring diagram \( \varphi \in WD(\mathcal{Y}) \) with one input box \( X \) and output box \( Y \), which can be depicted as follows:

![Wiring Diagram](image)

The output box \( Y \) is drawn as the outermost box. The single input box \( X \) is the smaller box. The delay node \( d \) is drawn as a circle, which will be our convention from now on. The supply wires \( y_2 \in Y^{in} \) and \( x_2 \in X^{out} \) are not in the image of the supplier assignment \( s : Dm \to Sp \), so \( y_2 \) (resp., \( x_2 \)) is an external (resp., internal) wasted wire.

### 2.3. Operad Structure

Throughout this section, \( S \) denotes a class. In this section, using Def. 2.1.10 of a colored operad, we define the colored operad structure on the collection \( WD \) of \( S \)-wiring diagrams (Def. 2.2.15).

The equivariant structure is given by permuting the labels of the input boxes.

**Definition 2.3.1** (Equivariance in \( WD \)). Suppose \( Y \in \text{Box}_S \), \( X \) is a \( \text{Box}_S \)-profile of length \( n \), and \( \sigma \in \Sigma_n \) is a permutation. Define the function

\[
WD(x_1, \ldots, x_n) = WD(X) \xrightarrow{\sigma} WD(X_{\sigma}) = WD(x_{\sigma(1)}, \ldots, x_{\sigma(n)})
\]

by sending \( \varphi = (DN, v, s) \in WD(X) \) to \( \varphi = (DN, v, s) \in WD(X_{\sigma}) \), using the fact that \( \bigsqcup_{i=1}^n X_i = \bigsqcup_{i=1}^n X_{\sigma(i)} \in \text{Box}_S \).

Next we define the colored units. For a box \( Y \), the \( Y \)-colored unit can be depicted as follows.

![Unit](image)

**Definition 2.3.2** (Units in \( WD \)). For each \( Y \in \text{Box}_S \), the \( Y \)-colored unit is defined as the wiring diagram

\[
1_Y = \left( DN = \emptyset, s = \text{Id} \right) \in WD(Y)
\]

(2.3.2.1)
with:

- no delay nodes and trivial $v : \text{DN} \rightarrow S$;
- supplier assignment

$$Dm = Y^{\text{out}} \sqcup Y^{\text{in}} \xrightarrow{\text{Id}} Y^{\text{in}} \sqcup Y^{\text{out}} = \text{Sp}$$

the identity function.

**Motivation 2.3.3.** Before we define the $o_i$ composition (2.1.10.1) in WD, let us first describe the intuition behind the definition. Pictorially, the $o_i$ composition $\varphi \circ_i \psi$ in WD replaces the $i$th input box $X_i$ in $\varphi$ with the wiring diagram $\psi$, using $X_i^{\text{in}}$ and $X_i^{\text{out}}$ for the necessary wire connections. Here is a picture to keep in mind for $\varphi \circ_i \psi$.

For simplicity we did not draw any delay nodes. In the actual definition below, we will take the coproduct of the sets of delay nodes in $\varphi$ and $\psi$.

**Definition 2.3.4** ($o_i$-Composition in WD). Suppose:

- $\varphi = (\text{DN}_\varphi, v_\varphi, s_\varphi) \in \text{WD}(X)$ with $X = (X_1, \ldots, X_n)$, $n \geq 1$, and $1 \leq i \leq n$;
- $\psi = (\text{DN}_\psi, v_\psi, s_\psi) \in \text{WD}(Y)$ with $|W| = r \geq 0$.

Define the wiring diagram $\varphi \circ_i \psi \in \text{WD}(Y)$ as follows, where the Box$_S$-profile

$$X \circ_i W = (X_1, \ldots, X_{i-1}, W, X_{i+1}, \ldots, X_n)$$
is as in (2.1.10.2).

(1) \(DN_{\varphi,\psi} = DN_{\varphi} \sqcup DN_{\psi} \in \text{Fin}_{S}\), so \(v_{\varphi,\psi} = v_{\varphi} \cup v_{\psi}\).

(2) The supplier assignment for \(\varphi \circ_{i} \psi\),

\[
\begin{align*}
\text{Dm}_{\varphi,\psi} & = Y^{\text{out}} \sqcup \bigsqcup_{j \neq i} X^{\text{in}}_{j} \sqcup \prod_{k=1}^{r} W^{\text{in}}_{k} \sqcup DN_{\varphi} \sqcup DN_{\psi} \\
\text{Sp}_{\varphi,\psi} & = Y^{\text{in}} \sqcup \bigsqcup_{j \neq i} X^{\text{out}}_{j} \sqcup \prod_{k=1}^{r} W^{\text{out}}_{k} \sqcup DN_{\varphi} \sqcup DN_{\psi}
\end{align*}
\]

in which the coproduct \(\bigsqcup_{j \neq i}\) is indexed by all \(j \in \{1, \ldots, i-1, i+1, \ldots, n\}\), is defined as follows. Suppose \(z \in \text{Dm}_{\varphi,\psi}\).

(a) If \(z \in Y^{\text{out}} \sqcup \bigsqcup_{j \neq i} X^{\text{in}}_{j} \sqcup DN_{\varphi} \subseteq \text{Dm}_{\varphi}\), then

\[
s_{\varphi,\psi}(z) = \begin{cases} s_{\varphi}(z) & \text{if } s_{\varphi}(z) \notin X^{\text{out}}_{i} \\ s_{\psi}s_{\varphi}(z) & \text{if } s_{\varphi}(z) \in X^{\text{out}}_{i} \end{cases}
\]

(b) If \(z \in \bigsqcup_{k=1}^{r} W^{\text{in}}_{k} \sqcup DN_{\psi} \subseteq \text{Dm}_{\psi}\), then

\[
s_{\varphi,\psi}(z) = \begin{cases} s_{\varphi}(z) & \text{if } s_{\varphi}(z) \notin X^{\text{in}}_{i} \\ s_{\psi}s_{\varphi}(z) & \text{if } s_{\varphi}(z) \in X^{\text{in}}_{i} \text{ and } s_{\varphi}s_{\psi}(z) \notin X^{\text{out}}_{i} \\ s_{\psi}s_{\varphi}s_{\psi}(z) & \text{if } s_{\varphi}(z) \in X^{\text{in}}_{i} \text{ and } s_{\varphi}s_{\psi}(z) \in X^{\text{out}}_{i} \end{cases}
\]

This finishes the definition of \(\varphi \circ_{i} \psi\).

**Lemma 2.3.5.** Def. 2.3.4 indeed defines a wiring diagram \(\varphi \circ_{i} \psi\) in \(WD(\frac{Y}{X}_{W})\).

**Proof.** We need to check that the supplier assignment for \(\varphi \circ_{i} \psi\) satisfies the non-instantaneity requirement (2.2.13.2). So suppose \(y \in Y^{\text{out}}\). We must show that \(s_{\varphi,\psi}(y) \notin Y^{\text{in}}\). By (2.3.4.2) we have

\[
s_{\varphi,\psi}(y) = \begin{cases} s_{\varphi}(y) \in \bigsqcup_{j \neq i} X^{\text{out}}_{j} \sqcup DN_{\varphi} & \text{if } s_{\varphi}(y) \notin X^{\text{out}}_{i} \\ s_{\psi}s_{\varphi}(y) \in \prod_{k=1}^{r} W^{\text{out}}_{k} \sqcup DN_{\psi} & \text{if } s_{\varphi}(y) \in X^{\text{out}}_{i} \end{cases}
\]

Here we have used the non-instantaneity requirement for both \(\varphi\) and \(\psi\). So in either case we have that \(s_{\varphi,\psi}(y) \notin Y^{\text{in}}\). \(\square\)

Many examples of the \(\circ_{i}\)-composition in WD will be given in Chapter 3. We now prove that, equipped with the structure above, WD is a colored operad.

**Lemma 2.3.6.** The \(\circ_{i}\)-composition in Def. 2.3.4 satisfies the left unity axiom (2.1.10.5), the right unity axiom (2.1.10.6), and the equivariance axiom (2.1.10.7).
2.3. Operad Structure

**Proof.** This follows from a direct inspection of the definitions of the equivariant structure (2.3.1.1) and the colored units in WD (2.3.2.1).

Next we show that WD satisfies the associativity axioms (2.1.10.3) and (2.1.10.4). The reader may wish to skip the proofs of the following two Lemmas and simply look at the pictures during the first reading.

**Motivation 2.3.7.** For the horizontal associativity axiom (2.1.10.3), one should keep in mind the following picture for the iterated operadic composition \((\varphi \circ_j \zeta) \circ_i \psi\).

\[
\begin{align*}
\psi &\Rightarrow Y_i \\
\zeta &\Rightarrow Y_j \\
\varphi &\Rightarrow Y_k \Rightarrow Y_{i} \Rightarrow Y_{j} \Rightarrow Y_{l} \Rightarrow Z_{i} \Rightarrow Z_{j} \Rightarrow Z_{l} \\
(\varphi \circ_j \zeta) \circ_i \psi &\Rightarrow Y_k \Rightarrow Y_{i} \Rightarrow Y_{j} \Rightarrow Y_{l} \Rightarrow Z_{i} \Rightarrow Z_{j} \Rightarrow Z_{l}
\end{align*}
\]

(2.3.7.1)

Note that on the right side, \(\psi\) and \(\zeta\) are depicted as gray boxes because their output boxes—namely \(Y_i\) and \(Y_j\)—are no longer input boxes in \((\varphi \circ_j \zeta) \circ_i \psi\). Furthermore, for simplicity the delay nodes are not drawn.

**Lemma 2.3.8.** The \(\circ_i\)-composition in Def. 2.3.4 satisfies the horizontal associativity axiom (2.1.10.3).

**Proof.** Suppose:

- \(\varphi \in WD(Y_k)\) with \(|Y| = n \geq 2\) and \(1 \leq i < j \leq n\);
- \(\psi \in WD(Y_j)\) with \(|W| = l\);
- \(\zeta \in WD(Y_i)\) with \(|X| = m\).

We must show that

\[(\varphi \circ_j \zeta) \circ_i \psi = (\varphi \circ_i \psi) \circ_{i-1+j} \zeta \in WD(Y_k)\]  

(2.3.8.1)

By Lemma 2.3.5 we already know that both sides are well-defined wiring diagrams in the indicated entry of WD. Moreover, both sides have \(\text{DN}_\varphi \cup \text{DN}_\psi \cup \text{DN}_\zeta \in \text{Fin}_S\) as the set of delay nodes. So it remains to show that their supplier assignments are equal.
Note that both sides in (2.3.8.1) have demand wires

$$Dm = Z^\text{out} \cup \bigsqcup_{p \neq i,j} Y^\text{in}_p \cup \bigsqcup_{q=1}^l W^\text{in}_q \cup \bigsqcup_{r=1}^m X^\text{in}_r \cup \text{DN}_\varphi \cup \text{DN}_\psi \cup \text{DN}_\zeta,$$

in which the coproduct $\bigsqcup_{p \neq i,j}$ is indexed by all $1 \leq p \leq n$ such that $p \neq i, j$. Similarly, both sides in (2.3.8.1) have supply wires

$$Sp = Z^\text{in} \cup \bigsqcup_{p \neq i,j} Y^\text{out}_p \cup \bigsqcup_{q=1}^l W^\text{out}_q \cup \bigsqcup_{r=1}^m X^\text{out}_r \cup \text{DN}_\varphi \cup \text{DN}_\psi \cup \text{DN}_\zeta.$$

Using the definitions (2.3.4.2) and (2.3.4.3), it follows from direct inspection that both sides in (2.3.8.1) have the following supplier assignment $s : Dm \rightarrow Sp$.

1. If $v \in Z^\text{out} \cup \bigsqcup_{p \neq i,j} Y^\text{in}_p \cup \text{DN}_\varphi \subseteq Dm$, then

$$s(v) = \begin{cases} 
  s_\varphi(v) & \text{if } s_\varphi(v) \notin Y^\text{out}_i \cup Y^\text{out}_j; \\
  s_\psi s_\varphi(v) & \text{if } s_\psi(s_\varphi(v)) \notin Y^\text{out}_i \cup Y^\text{out}_j; \\
  s_\zeta s_\varphi(v) & \text{if } s_\zeta(s_\varphi(v)) \notin Y^\text{out}_i \cup Y^\text{out}_j.
\end{cases}$$

2. If $v \in \bigsqcup_{q=1}^l W^\text{in}_q \cup \text{DN}_\psi \subseteq Dm$, then

$$s(v) = \begin{cases} 
  s_\psi(v) & \text{if } s_\psi(v) \notin Y^\text{in}_i; \\
  s_\psi s_\varphi(v) & \text{if } s_\psi(s_\varphi(v)) \notin Y^\text{in}_i \cup Y^\text{out}_j; \\
  s_\psi s_\zeta s_\varphi(v) & \text{if } s_\psi(s_\varphi(v)) \notin Y^\text{in}_i \cup Y^\text{out}_j; \\
  s_\zeta s_\varphi v & \text{if } s_\zeta(s_\varphi(v)) \notin Y^\text{in}_i \cup Y^\text{out}_j.
\end{cases}$$

3. Finally, if $v \in \bigsqcup_{r=1}^m X^\text{in}_r \cup \text{DN}_\zeta \subseteq Dm$, then

$$s(v) = \begin{cases} 
  s_\zeta(v) & \text{if } s_\zeta(v) \notin Y^\text{in}_i; \\
  s_\psi s_\zeta(v) & \text{if } s_\psi(s_\zeta(v)) \notin Y^\text{in}_i \cup Y^\text{out}_j; \\
  s_\psi s_\zeta s_\varphi(v) & \text{if } s_\psi(s_\zeta(s_\varphi(v))) \notin Y^\text{in}_i \cup Y^\text{out}_j; \\
  s_\zeta s_\psi s_\zeta(v) & \text{if } s_\zeta(s_\psi(s_\zeta(v))) \notin Y^\text{in}_i \cup Y^\text{out}_j.
\end{cases}$$

This finishes the proof of the desired equality (2.3.8.1). $\square$
**Motivation 2.3.9.** For the vertical associativity axiom, one should keep the following picture of $\phi \circ_i (\psi \circ_j \zeta)$ in mind.

\[
\begin{array}{c}
X^\text{in}_j \quad \rightarrow \quad \zeta \quad \rightarrow \quad X^\text{out}_j \\
Y^\text{in}_j \quad \rightarrow \quad X_j \quad \rightarrow \quad X_k \quad \rightarrow \quad \psi \quad \rightarrow \quad Y^\text{out}_l \\
Z^\text{in}_l \quad \rightarrow \quad Y_l \quad \rightarrow \quad Y_l \quad \rightarrow \quad \zeta \quad \rightarrow \quad Z^\text{out}_l
\end{array}
\]

\[
\phi \circ_i (\psi \circ_j \zeta)
\]

Once again on the right side, $\zeta$ is depicted as a gray box because its output box $X_j$ is no longer an input box in $\phi \circ_i (\psi \circ_j \zeta)$. Furthermore, for simplicity the delay nodes are not drawn.

**Lemma 2.3.10.** The $\circ_i$-composition in Def. 2.3.4 satisfies the vertical associativity axiom (2.3.10.4).

**Proof.** Suppose:

- $\phi \in WD(\overline{Z})$ with $|Y| = n \geq 1$ and $1 \leq i \leq n$;
- $\psi \in WD(\overline{X})$ with $|X| = m \geq 1$ and $1 \leq j \leq m$;
- $\zeta \in WD(\overline{W})$ with $|W| = l$.

We must show that

\[
(\phi \circ_i \psi) \circ_{i-1+j} \zeta = \phi \circ_i (\psi \circ_j \zeta) \in WD(\overline{X_Y(X^Z)}_{i-1+j}).
\]

By Lemma 2.3.5 we already know that both sides are well-defined wiring diagrams in the indicated entry of WD. Moreover, both sides have $\text{DN}_{\phi} \cup \text{DN}_{\psi} \cup \text{DN}_{\zeta} \in \text{Fin}_5$ as the set of delay nodes. So it remains to show that their supplier assignments are equal.

Note that both sides in (2.3.10.1) have demand wires

\[
D_m = Z^\text{out}_m \cup \bigcup_{p \neq i} Y^\text{in}_p \cup \bigcup_{q \neq j} X^\text{in}_q \cup \bigcup_{r=1}^l W^\text{in}_r \cup \text{DN}_{\phi} \cup \text{DN}_{\psi} \cup \text{DN}_{\zeta}
\]
in which $\bigsqcup_{p \neq i}^{\mbox{out}}$ is indexed by all $1 \leq p \leq n$ such that $p \neq i$, and $\bigsqcup_{q \neq j}^{\mbox{out}}$ is indexed by all $1 \leq q \leq m$ such that $q \neq j$. Similarly, both sides in (2.3.10.1) have supply wires

$$Sp = Z^\mbox{in} \cup \bigsqcup_{p \neq i}^{\mbox{out}} Y_p^\mbox{out} \cup \bigsqcup_{q \neq j}^{\mbox{out}} X_q^\mbox{out} \cup \bigsqcup_{r=1}^{l} W_r^\mbox{out} \cup \mbox{DN}_p \cup \mbox{DN}_q \cup \mbox{DN}_c.$$  

Using the definitions (2.3.4.2) and (2.3.4.3), it follows from direct inspection that both sides in (2.3.10.1) have the following supplier assignment $s : Dm \rightarrow Sp$.

1. If $v \in Z^\mbox{out} \cup \bigsqcup_{p \neq i}^{\mbox{in}} Y_p^\mbox{in} \cup \mbox{DN}_p \subseteq Dm_p$, then

$$s(v) = \begin{cases} s_q(v) & \text{if } s_q(v) \notin Y_i^\mbox{out} \cup Y_i^\mbox{in}; \\ s_q s_p(v) & \text{if } s_q(v) \in Y_i^\mbox{out}; \\ s_p s_q(v) & \text{if } s_p(v) \in Y_i^\mbox{in} \text{ and } s_p s_q(v) \notin Y_i^\mbox{out}; \\ s_q s_p s_q(v) & \text{if } s_q(v) \in Y_i^\mbox{in}, s_p s_q(v) \in Y_i^\mbox{out}, \text{ and } s_p s_q s_q(v) \notin X_i^\mbox{out}; \\ s_p s_q s_p s_q(v) & \text{if } s_p(v) \in Y_i^\mbox{in}, s_p s_q(v) \in Y_i^\mbox{out}, \text{ and } s_p s_q s_p s_q(v) \in X_i^\mbox{out}. \\ \end{cases}$$

2. If $v \in \bigsqcup_{q \neq j}^{\mbox{out}} X_q^\mbox{in} \cup \mbox{DN}_q \subseteq Dm_q$, then

$$s(v) = \begin{cases} s_q(v) & \text{if } s_q(v) \notin X_j^\mbox{out} \cup X_j^\mbox{in}; \\ s_q s_q(v) & \text{if } s_q(v) \in X_j^\mbox{out}; \\ s_q s_p s_q(v) & \text{if } s_q(v) \in X_j^\mbox{in} \text{ and } s_q s_p s_q(v) \notin X_j^\mbox{out}; \\ s_p s_q s_p s_q(v) & \text{if } s_p(v) \in X_j^\mbox{in}, s_q s_p s_q(v) \in Y_j^\mbox{in}, \text{ and } s_p s_q s_p s_q(v) \notin X_j^\mbox{out}. \\ \end{cases}$$

3. If $v \in \bigsqcup_{r=1}^{l} W_r^\mbox{in} \cup \mbox{DN}_c \subseteq Dm_c$, then

$$s(v) = \begin{cases} s_c(v) & \text{if } s_c(v) \notin X_i^\mbox{out}; \\ s_p s_c(v) & \text{if } s_c(v) \in X_i^\mbox{in} \text{ and } s_p s_c(v) \notin X_i^\mbox{out} \cup Y_i^\mbox{in}; \\ s_q s_p s_c(v) & \text{if } s_p(v) \in X_i^\mbox{in} \text{ and } s_p s_c(v) \notin Y_i^\mbox{out}; \\ s_p s_q s_p s_c(v) & \text{if } s_q(v) \in X_i^\mbox{in}, s_q s_p s_c(v) \in Y_i^\mbox{in}, \text{ and } s_p s_q s_p s_c(v) \notin X_i^\mbox{out}; \\ s_p s_q s_p s_q s_c(v) & \text{if } s_p(v) \in X_i^\mbox{in}, s_q s_p s_c(v) \in Y_i^\mbox{in}, s_p s_q s_p s_q s_c(v) \in X_i^\mbox{out}; \\ \end{cases}$$

This finishes the proof of the desired equality (2.3.10.1). \hfill \square

**Theorem 2.3.11.** For any class $S$, when equipped with the structure in Def. 2.3.3–2.3.4, WD in Def. 2.2.13 is a $\boxS$-colored operad, called the operad of wiring diagrams.

**Proof.** In view of Def. 2.1.10, this follows from Lemmas 2.3.6, 2.3.8 and 2.3.10. \hfill \square

**Remark 2.3.12.** When $S$ is the class of pointed sets, Theorem 2.3.11 is proved in [RS13] (section 2). The proof in [RS13] is somewhat different than ours because it uses Def. 2.1.3 of a colored operad instead of Def. 2.1.10.
2.4. Summary of Chapter 2

(1) An $S$-colored operad consists of a class $O(d, c_1, \ldots, c_n)$ for each $d, c_1, \ldots, c_n \in S$ and $n \geq 0$ together with symmetric group actions, an operadic composition, and colored units that satisfy the associativity, unity, and equivariance axioms.

(2) Every operad is determined by the $\circ_i$-compositions.

(3) An $S$-wiring diagram has a finite number of input boxes, an output box, an $S$-finite set of delay nodes, and a supplier assignment that satisfies the non-instantaneity requirement.

(4) For each class $S$, the collection of $S$-wiring diagrams $WD$ is a $\Box_S$-colored operad.
Chapter 3

Generators and Relations

Fix a class $S$. The purpose of this chapter is to describe a finite number of wiring diagrams that we will later show to be sufficient to describe the entire operad $\mathcal{WD}$ of wiring diagrams (Theorems 5.2.11) as well as its variants $\mathcal{WD}_\bullet$ (Theorem 5.3.7) and $\mathcal{WD}_0$ (Theorem 5.4.8). One may also regard this chapter as consisting of a long list of examples of wiring diagrams.

In Section 3.1 we describe eight wiring diagrams, called the generating wiring diagrams. In Theorem 5.1.11 we will show that they generate the operad $\mathcal{WD}$ of wiring diagrams. This means that every wiring diagram can be obtained from finitely many generating wiring diagrams via iterated operadic compositions. For now one may think of the generating wiring diagrams as examples of wiring diagrams.

In Section 3.2 we explain why a wiring diagram with an internal wasted wire is not among the generating wiring diagrams. More concretely, we will observe in Prop. 3.2.3 that an internal wasted wire can be generated using two generating wiring diagrams.

In Section 3.3 we describe 28 elementary relations among the generating wiring diagrams. In Theorem 5.2.11 we will show that these elementary relations together with the operad associativity and unity axioms—(2.1.10.3), (2.1.10.4), (2.1.10.5), and (2.1.10.6)—for the generating wiring diagrams generate all the relations in the operad $\mathcal{WD}$ of wiring diagrams. In other words, suppose an arbitrary wiring diagram can be built in two ways using the generating wiring diagrams. Then there exists a finite sequence of steps connecting them in which each step is given by one of the 28 elementary relations or an operad associativity/unity axiom for the generating wiring diagrams. For now one may think of the elementary relations as examples of the operadic composition in the operad $\mathcal{WD}$. 

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3. Generators and Relations

3.1. Generating Wiring Diagrams

Recall the definition of a wiring diagram (Def. 2.2.15). In this section, we introduce 8 wiring diagrams, called the generating wiring diagrams. They will be used in later chapters to give a finite presentation for the operad $\mathcal{WD}$ of wiring diagrams.

**Definition 3.1.1.** Define the empty wiring diagram $\varepsilon \in \mathcal{WD}^\emptyset$ with:

1. no input boxes;
2. the empty box $\emptyset$ (Def. 2.2.7) as the output box;
3. no delay nodes (i.e., $\text{DN} = \emptyset$);
4. supplier assignment $s : \text{Dm} = \emptyset \rightarrow \emptyset = \text{Sp}$ the trivial function.

The next wiring diagram has a delay node as depicted in the following picture, where we use the convention that delay nodes are drawn as circles as in (2.2.18.1).

![Delay Node Diagram]

**Definition 3.1.2.** Suppose $d \in S$. Denote also by $d \in \text{Box}_S$ the box with one input and one output, both also denoted by $d$ and have values $d \in S$. Define the 1-delay node $\delta_d \in \mathcal{WD}^\emptyset$ as the wiring diagram with:

1. no input boxes;
2. the output box $d = (\{d\}, \{d\})$, in which both $d$’s have values $d \in S$;
3. $\text{DN} = \{d\}$, in which $d$ has value $d \in S$;
4. supplier assignment $Dm = Y^{\text{out}} \sqcup \text{DN} = \{d\} \sqcup \{d\} \xrightarrow{s} \{d\} \sqcup \{d\} = Y^{\text{in}} \sqcup \text{DN} = \text{Sp}$ the identity function that takes $d \in Y^{\text{out}}$ to $d \in \text{DN}$ and $d \in \text{DN}$ to $d \in Y^{\text{in}}$.

Next we define the wiring diagram:

![1-Delay Node Diagram]

**Definition 3.1.3.** Suppose $X, Y \in \text{Box}_S$ together with isomorphisms $f^{\text{in}} : X^{\text{in}} \cong Y^{\text{in}}$ and $f^{\text{out}} : Y^{\text{out}} \cong X^{\text{out}}$ in $\text{Fin}_S$. Define the wiring diagram $\tau_f \in \mathcal{WD}(X,Y)$ with:

1. one input box $X$ and output box $Y$;
(2) no delay nodes;
(3) supplier assignment

\[ Dm = Y^{out} \cup X^{in} \xrightarrow{s = f^{out} \cup f^{in}} Y^{in} \cup X^{out} = Sp \]

the coproduct of the given isomorphisms.

We will often suppress the given isomorphisms and simply write \( \tau_{X,Y} \) or even \( \tau \), which will be called a *name change*.

Next we define the wiring diagram:

---

**Definition 3.1.4.** Suppose \( X, Y \in \text{Box}_S \). Define the wiring diagram \( \theta_{X,Y} \in \text{WD}(X, Y) \) with:

1. two input boxes \( (X, Y) \) and output box \( X \cup Y \);
2. no delay nodes;
3. supplier assignment

\[
Dm = \left[ X^{out} \cup Y^{out} \right] \cup \left[ X^{in} \cup Y^{in} \right] \xrightarrow{s} \left[ X^{in} \cup Y^{in} \right] \cup \left[ X^{out} \cup Y^{out} \right] = Sp
\]

the identity map.

We will call \( \theta_{X,Y} \) a 2-cell.

Next we define the wiring diagram:

---

**Definition 3.1.5.** Suppose:

- \( X \in \text{Box}_S \), and \( (x_+, x_-) \in X^{out} \times X^{in} \) such that \( v(x_+) = v(x_-) \in S \).
- \( X \setminus x \in \text{Box}_S \) is obtained from \( X \) by removing \( x_+ \), so \( (X \setminus x)^{in} = X^{in} \setminus \{x_-\} \) and \( (X \setminus x)^{out} = X^{out} \setminus \{x_+\} \).

Define the wiring diagram \( \lambda_{X,X} \in \text{WD}(X, Y) \) with:
(1) one input box $X$ and output box $X \setminus x$;
(2) no delay nodes;
(3) supplier assignment

$$
\begin{align*}
Dm &= \left[ X^{\text{out}} \setminus \{x_+\} \cup \{x_-\} \right] \cup X^{\text{in}} \setminus \{x_+\} \cup \{x_-\} \\
Sp &= \left[ X^{\text{in}} \setminus \{x_-\} \cup X^{\text{out}} \setminus \{x_+\} \right] \cup \{x_+\}
\end{align*}
$$

given by $s(x_-) = x_+$ and the identity function everywhere else.

We will call the wiring diagram $\lambda_{X,x}$ a 1-loop.

Next we define the wiring diagram:

$$
\sigma_{X,x_1,x_2}
$$

\begin{align*}
Y^{\text{in}} &\xrightarrow{x_{12}} X \\
X &\xrightarrow{x_1} Y^{\text{out}} \\
X &\xrightarrow{x_2} Y^{\text{out}}
\end{align*}

**Definition 3.1.6.** Suppose:

- $X \in \text{Box}_S$, and $x_1, x_2 \in X^{\text{in}}$ are distinct elements such that $v(x_1) = v(x_2) \in S$.
- $Y = X/\langle x_1 = x_2 \rangle \in \text{Box}_S$ is obtained from $X$ by identifying $x_1$ and $x_2$, so $Y^{\text{in}} = X^{\text{in}}/(x_1 = x_2)$ and $Y^{\text{out}} = X^{\text{out}}$. The identified element of $x_1$ and $x_2$ in $Y^{\text{in}}$ will be denoted by $x_{12}$.

Define the wiring diagram $\sigma_{X,x_1,x_2} \in \text{WD}^{(\lambda)}$ with:

(1) one input box $X$ and output box $Y$;
(2) no delay nodes;
(3) supplier assignment

$$
\begin{align*}
Dm &= Y^{\text{out}} \cup X^{\text{in}} = X^{\text{out}} \cup X^{\text{in}} \\
Sp &= Y^{\text{in}} \cup X^{\text{out}} = \frac{X^{\text{in}}}{\langle x_1 = x_2 \rangle} \cup X^{\text{out}}
\end{align*}
$$

that sends both $x_1, x_2 \in X^{\text{in}}$ to $x_{12} \in Y^{\text{in}}$ and is the identity function everywhere else.
We will call the wiring diagram $\sigma_{X,x_1,x_2}$ an \textit{in-split}.

Next we define the wiring diagram:

\[
\begin{array}{c}
\text{Y}^{\text{in}} \xrightarrow{y_1} X \xrightarrow{x_1} Y^{\text{out}} \\
\text{Y}^{\text{in}} \xrightarrow{y_2} X \xrightarrow{x_2} Y^{\text{out}}
\end{array}
\]

\textbf{Definition 3.1.7.} Suppose:

- $Y \in \text{Box}_S$, and $y_1, y_2 \in Y^{\text{out}}$ are distinct elements such that $v(y_1) = v(y_2) \in S$.
- $X = Y/(y_1 = y_2) \in \text{Box}_S$ is obtained from $Y$ by identifying $y_1$ and $y_2$, so $X^{\text{in}} = Y^{\text{in}}$ and $X^{\text{out}} = Y^{\text{out}}/(y_1 = y_2)$. The identified element of $y_1$ and $y_2$ in $X^{\text{out}}$ will be denoted by $y_{12}$.

Define the wiring diagram $\sigma_{Y,y_1,y_2} \in \text{WD}(X)$ with:

1. one input box $X$ and output box $Y$;
2. no delay nodes;
3. supplier assignment

\[
\begin{array}{c}
\text{Dm} = Y^{\text{out}} \cup X^{\text{in}} = Y^{\text{out}} \cup Y^{\text{in}} \\
\text{Sp} = Y^{\text{in}} \cup X^{\text{out}} = Y^{\text{in}} \cup Y^{\text{out}}/(y_1 = y_2)
\end{array}
\]

that sends both $y_1, y_2 \in Y^{\text{out}}$ to $y_{12} \in X^{\text{out}}$ and is the identity function everywhere else.

We will call the wiring diagram $\sigma_{Y,y_1,y_2}$ an \textit{out-split}.

Next we define the following wiring diagram with an external wasted wire:

\[
\begin{array}{c}
\text{Y}^{\text{in}} \xrightarrow{y} X \xrightarrow{\omega_{Y,y}} Y^{\text{out}}
\end{array}
\]

\textbf{Definition 3.1.8.} Suppose:

- $Y \in \text{Box}_S$, and $y \in Y^{\text{in}}$.
- $X \in \text{Box}_S$ is obtained from $Y$ by removing $y$, so $X^{\text{in}} = Y^{\text{in}} \setminus \{y\}$ and $X^{\text{out}} = Y^{\text{out}}$. 
Define the wiring diagram \( \omega_{Y,y} \in \text{WD}(X) \) with:

1. one input box \( X \) and output box \( Y \);
2. no delay nodes;
3. supplier assignment

\[
D_m = Y^\text{out} \uplus X^\text{in} = Y^\text{in} \uplus \left[ Y^\text{in} \setminus \{ y \} \right]
\]

\[
S_p = Y^\text{in} \uplus X^\text{out} = Y^\text{in} \uplus Y^\text{out}
\]

the inclusion.

We will call the wiring diagram \( \omega_{Y,y} \) a 1-wasted wire.

**Definition 3.1.9.** The eight wiring diagrams in Def. 3.1.1–3.1.8 will be referred to as generating wiring diagrams.

**Remark 3.1.10.** Among the generating wiring diagrams:

1. A 1-delay node \( \delta_d \) (Def. 3.1.2) is the only wiring diagram that has a delay node.
2. A 1-wasted wire \( \omega_{Y,y} \) (Def. 3.1.8) is the only wiring diagram that has an external wasted wire, namely \( y \in Y^\text{in} \).
3. None has an internal wasted wire (Def. 2.2.13). As we will see in Prop. 3.2.3 below, an internal wasted wire can be generated using a 1-loop and a 1-wasted wire, hence is not needed as a generator.
4. The empty wiring diagram \( \varepsilon \) (Def. 3.1.1) and a 1-delay node \( \delta_d \) are 0-ary elements in \( \text{WD} \).
5. A name change \( \tau \) (Def. 3.1.3), a 1-loop \( \lambda_{X,X} \) (Def. 3.1.5), an in-split \( \sigma_{X,x_1,x_2} \) (Def. 3.1.6), an out-split \( \sigma^{Y,y_1,y_2} \) (Def. 3.1.7), and a 1-wasted wire \( \omega_{Y,y} \) are unary elements in \( \text{WD} \).
6. A 2-cell \( \theta_{X,Y} \) (Def. 3.1.4) is a binary element in \( \text{WD} \).

### 3.2. Internal Wasted Wires

Recall from Def. 2.2.13 that an internal wasted wire is an internal output, hence a supply wire, that does not belong to the image of the supplier assignment. The purpose of this section is to explain why the wiring diagram
that has an internal wasted wire \( x \) is not needed as a generating wiring diagram. First we define this wiring diagram.

**Definition 3.2.1.** Suppose:
- \( X \in \text{Box}_S \), and \( x \in X^{\text{out}} \).
- \( Y = X \setminus \{ x \} \in \text{Box}_S \) is obtained from \( X \) by removing \( x \).

Define the wiring diagram \( \omega^{X,x} \in \text{WD}(\chi) \) with:
1. one input box \( X \) and output box \( Y \);
2. no delay nodes;
3. supplier assignment

\[
\begin{align*}
D_m &= Y^{\text{out}} \cup X^{\text{in}} = [X^{\text{out}} \setminus \{ x \}] \cup X^{\text{in}} \\
S_p &= Y^{\text{in}} \cup X^{\text{out}} = X^{\text{in}} \cup X^{\text{out}}
\end{align*}
\]

the inclusion.

We will call the wiring diagram \( \omega^{X,x} \) a **1-internal wasted wire**.

**Motivation 3.2.2.** The following observation says that a 1-internal wasted wire can be obtained as the substitution of a 1-wasted wire into a 1-loop, both of which are generating wiring diagrams. This is expressed in the following picture

\[
X^{\text{in}} = Y^{\text{in}} \rightarrow X \rightarrow Y^{\text{out}} = X^{\text{out}} \setminus \{ x \}
\]

in which the intermediate gray box will be called \( W \) below.

**Proposition 3.2.3.** Suppose:
- \( \omega^{X,x} \in \text{WD}(\chi) \) is a 1-internal wasted wire (Def. 3.2.1).
- \( W = X \cup \{ w \} \in \text{Box}_S \) such that \( w \in W^{\text{in}} \) satisfies \( v(w) = v(x) \in S \).
- \( \lambda_{W,\{w,x\}} \in \text{WD}(\gamma) \) is the 1-loop (Def. 3.1.5) in which \( x \in X^{\text{out}} = W^{\text{out}} \) is the supply wire of \( w \in W^{\text{in}} \).
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- \( \omega_{W,n} \in \text{WD}(\chi) \) is a 1-wasted wire (Def. 3.1.8).

Then

\[
(\lambda_{W, (w, x)}) \circ_1 (\omega_{W,n}) = \omega_{X,x} \in \text{WD}(\gamma)
\]

(3.2.3.1)

Proof. By definition both sides of (3.2.3.1) belong to \( \text{WD}(\gamma) \) and have no delay nodes. It remains to check that their supplier assignments are equal. By the definitions of \( \circ_1 \) (Def. 2.3.4), 1-loop, and 1-wasted wire, the supplier assignment of the left side \( (\lambda_{W, (w, x)}) \circ_1 (\omega_{X,x}) \), namely

\[
\begin{align*}
D_m &= Y^{\text{out}} \cup X^{\text{in}} = [X^{\text{out}} \setminus \{x\}] \cup X^{\text{in}} \\
S_p &= Y^{\text{in}} \cup X^{\text{out}} = X^{\text{in}} \cup X^{\text{out}}
\end{align*}
\]

is the inclusion. By Def. 3.2.1 this is also the supplier assignment of the 1-internal wasted wire \( \omega_{X,x} \).

As a consequence of (3.2.3.1), the 1-internal wasted wire \( \omega_{X,x} \) is not needed as a generating wiring diagram.

3.3. Elementary Relations

The purpose of this section is to introduce 28 elementary relations among the generating wiring diagrams (Def. 3.1.9). Each elementary relation is proved by a simple inspection of the relevant definitions of the generating wiring diagrams and operadic compositions, similar to the proofs of Lemma 2.3.8, Lemma 2.3.10, and Prop. 3.2.3 above. Therefore, we will prove only the first one and omit the proofs for the rest, providing a picture instead in most cases. We will frequently use the \( \circ_i \)-composition (2.1.10.1) in describing these elementary relations.

Notation 3.3.1. Suppose \( O \) is an S-colored operad (Def. 2.1.10), and \( T \) is a set.

1. If \( \varphi \in O(c) \) where the input profile \( (c) \) has length 1 and if \( \phi \in O(\chi) \), then we write

\[
\varphi \circ \phi = \varphi \circ_1 \phi.
\]

(3.3.1.1)

2. Suppose \( \varphi_1, \ldots, \varphi_k \in O \) such that each of \( \varphi_1, \ldots, \varphi_{k-1} \) belongs to an entry of \( O \) whose input profile has length 1. Then we write

\[
\varphi_1 \circ \cdots \circ \varphi_k = \left( \cdots (\varphi_1 \circ_1 \varphi_2) \circ_1 \cdots \right) \circ_1 \varphi_k
\]

(3.3.1.2)
whenever the right side is defined, in which each pair of parentheses starts on the left. For example, we have

\[
\varphi_1 \circ \varphi_2 \circ \varphi_3 = (\varphi_1 \circ \varphi_2) \circ \varphi_3,
\]

\[
\varphi_1 \circ \varphi_2 \circ \varphi_3 \circ \varphi_4 = \left((\varphi_1 \circ \varphi_2) \circ \varphi_3\right) \circ \varphi_4.
\]

(3) Write \(|T|\) for the cardinality of \(T\).

The first six relations are about the name change wiring diagrams (Def. 3.1.3). The first relation says that two consecutive name changes can be composed into one name change.

**Proposition 3.3.2.** Suppose:

- \(\tau_{Y,Z} \in \text{WD}(\subseteq \mathcal{X})\) and \(\tau_{X,Y} \in \text{WD}(\subseteq \mathcal{Y})\) are name changes.

- \(\tau_{X,Z} \in \text{WD}(\subseteq \mathcal{Z})\) is the name change given by composing the isomorphisms that define \(\tau_{Y,Z}\) and \(\tau_{X,Y}\).

Then

\[
(\tau_{Y,Z}) \circ (\tau_{X,Y}) = \tau_{X,Z} \in \text{WD}(\subseteq \mathcal{Z}).
\]

**Proof.** We are given isomorphisms \(f^{\text{in}} : X^{\text{in}} \cong Y^{\text{in}}\) and \(f^{\text{out}} : Y^{\text{out}} \cong X^{\text{out}}\) for \(\tau_{X,Y}\) and isomorphisms \(g^{\text{in}} : Y^{\text{in}} \cong Z^{\text{in}}\) and \(g^{\text{out}} : Z^{\text{out}} \cong Y^{\text{out}}\) for \(\tau_{Y,Z}\). The name change \(\tau_{X,Z}\) given by composing these isomorphisms is defined by the isomorphisms

\[
g^{\text{in}} \circ f^{\text{in}} : X^{\text{in}} \cong Z^{\text{in}} \quad \text{and} \quad f^{\text{out}} \circ g^{\text{out}} : Z^{\text{out}} \cong X^{\text{out}}.
\]

On the other hand, by Def. 2.3.4 the composition \(\tau_{Y,Z} \circ \tau_{X,Y}\) has no delay nodes, since neither \(\tau_{X,Y}\) nor \(\tau_{Y,Z}\) has a delay node. Its supplier assignment is the function

\[
\text{Dm} = Z^{\text{out}} \amalg X^{\text{in}} \xrightarrow{s} Z^{\text{in}} \amalg X^{\text{out}} = \text{Sp}
\]

given by

\[
s(z) = s_{\tau_{X,Y}} s_{\tau_{Y,Z}}(z) = f^{\text{out}}(g^{\text{out}}(z)) \quad \text{for} \quad z \in Z^{\text{out}};
\]

\[
s(x) = s_{\tau_{X,Y}} s_{\tau_{Y,Z}}(x) = g^{\text{in}}(f^{\text{in}}(x)) \quad \text{for} \quad x \in X^{\text{in}}.
\]

This is the same supplier assignment as that of the name change \(\tau_{X,Z}\) above. \(\square\)

The next relation says that name changes inside a 2-cell (Def. 3.1.4) can be rewritten as a name change outside of a 2-cell.

**Proposition 3.3.3.** Suppose:

- \(\tau_{X,X'} \in \text{WD}(\subseteq \mathcal{X})\) and \(\tau_{Y,Y'} \in \text{WD}(\subseteq \mathcal{Y})\) are name changes.

- \(\tau_{X,Y,X',Y'} \in \text{WD}(\subseteq \mathcal{X}'\mathcal{Y})\) is the name change induced by \(\tau_{X,X'}\) and \(\tau_{Y,Y'}\).

- \(\theta_{X',Y'} \in \text{WD}(\subseteq \mathcal{X}')\) and \(\theta_{X,Y} \in \text{WD}(\subseteq \mathcal{X})\) are 2-cells.
Then
\[
(\theta_{X',Y} \circ \tau_{X,X'}) \circ_2 \tau_{Y,Y'} = (\tau_{X,Y,X',Y'}) \circ (\theta_{X,Y}) \in \text{WD}(X,Y). \tag{3.3.3.1}
\]

The next relation says that a name change inside a 1-loop (Def. 3.1.5) can be rewritten as a name change of a 1-loop.

**Proposition 3.3.4.** Suppose:

- \( X \in \text{Box}_S, (x_+, x_-) \in X^{\text{out}} \times X^{\text{in}} \) such that \( \nu(x_+) = \nu(x_-) \in S. \)
- \( X \setminus x \in \text{Box}_S \) is obtained from \( X \) by removing \( x_+ \).
- \( \lambda_{X,x} \in \text{WD}(\gamma_X) \) is the corresponding 1-loop.
- \( \tau_{X,Y} \in \text{WD}(\gamma_Y) \) is a name change such that \((y_+, y_-) \in Y^{\text{out}} \times Y^{\text{in}} \) corresponds to \((x_+, x_-) \).
- \( \lambda_{Y,y} \in \text{WD}(\gamma_Y) \) is the corresponding 1-loop.
- \( \tau_{X \setminus x, Y \setminus y} \in \text{WD}(\gamma_{X,Y}) \) is the name change induced by \( \tau_{X,Y} \).

Then
\[
(\lambda_{Y,y}) \circ (\tau_{X,Y}) = (\tau_{X \setminus x, Y \setminus y}) \circ (\lambda_{X,x}) \in \text{WD}(\gamma_{X,Y}). \tag{3.3.4.1}
\]

The next relation says that a name change inside an in-split (Def. 3.1.6) can be rewritten as a name change of an in-split.

**Proposition 3.3.5.** Suppose:

- \( X \in \text{Box}_S, \) and \( x_1, x_2 \in X^{\text{in}} \) are distinct elements such that \( \nu(x_1) = \nu(x_2) \in S. \)
- \( X' = X/(x_1 = x_2) \in \text{Box}_S \) is obtained from \( X \) by identifying \( x_1 \) and \( x_2 \).
- \( \sigma_{X,x_1,x_2} \in \text{WD}(\gamma_X) \) is the corresponding in-split.
- \( \tau_{X,Y} \in \text{WD}(\gamma_Y) \) is a name change with \( y_1, y_2 \in Y^{\text{in}} \) corresponding to \( x_1, x_2 \in X^{\text{in}} \).
- \( Y' = Y/(y_1 = y_2) \in \text{Box}_S \) is obtained from \( Y \) by identifying \( y_1 \) and \( y_2 \).
- \( \sigma_{Y,y_1,y_2} \in \text{WD}(\gamma_Y) \) is the corresponding in-split.
- \( \tau_{X',Y'} \in \text{WD}(\gamma_{X,Y}) \) is the name change induced by \( \tau_{X,Y} \).

Then
\[
(\sigma_{Y,y_1,y_2}) \circ (\tau_{X,Y}) = (\tau_{X',Y'}) \circ (\sigma_{X,x_1,x_2}) \in \text{WD}(\gamma_{X,Y}). \tag{3.3.5.1}
\]

The next relation is the out-split (Def. 3.1.7) analogue of (3.3.5.1).

**Proposition 3.3.6.** Suppose:

- \( Y \in \text{Box}_S, \) and \( y_1, y_2 \in Y^{\text{out}} \) are distinct elements such that \( \nu(y_1) = \nu(y_2) \in S. \)
- \( Y' = Y/(y_1 = y_2) \in \text{Box}_S \) is obtained from \( Y \) by identifying \( y_1 \) and \( y_2 \).
3.3. Elementary Relations

- $\sigma^{Y,y_1,y_2} \in WD(Y)\text{'s} \text{ is an out-split.}$
- $\tau_{X,Y} \in WD(X)$ is a name change with $x_1,x_2 \in X^{\text{out}}$ corresponding to $y_1,y_2 \in Y^{\text{out}}$.
- $X' = X/(x_1 = x_2) \in \Box_S$ is obtained from $X$ by identifying $x_1$ and $x_2$.
- $\sigma^{X,x_1,x_2} \in WD(X)$ is the corresponding out-split.
- $\tau_{X',Y'} \in WD(Y)$ is the name change induced by $\tau_{X,Y}$.

Then

$$\left(\sigma^{Y,y_1,y_2} \circ (\tau_{X',Y'})\right) = (\tau_{X,Y} \circ (\sigma^{X,x_1,x_2})) \in WD(Y)\text{'s}. \quad (3.3.6.1)$$

The next relation says that a name change inside a 1-wasted wire (Def. 3.1.8) can be rewritten as a name change of a 1-wasted wire.

**Proposition 3.3.7.** Suppose:

- $Y \in \Box_S$, $y \in Y^{\text{in}}$, and $Y' = Y \setminus \{y\} \in \Box_S$ is obtained from $Y$ by removing $y$.
- $\omega_{Y,y} \in WD_Y$ is the corresponding 1-wasted wire.
- $\tau_{X,Y} \in WD(X)$ is a name change with $x \in X^{\text{in}}$ corresponding to $y \in Y^{\text{in}}$.
- $X' \in \Box_S$ is obtained from $X$ by removing $x$.
- $\omega_{X,x} \in WD_X$ is the corresponding 1-wasted wire.
- $\tau_{X',Y'} \in WD(Y)$ is the name change induced by $\tau_{X,Y}$.

Then

$$\left(\omega_{Y,y} \circ (\tau_{X',Y'})\right) = (\tau_{X,Y} \circ (\omega_{X,x})) \in WD(X). \quad (3.3.7.1)$$

The next seven relations are about 2-cells (Def. 3.1.4). The following relation says that substituting the empty wiring diagram (Def. 3.1.1) into a 2-cell yields a colored unit (2.3.2.1).

**Proposition 3.3.8.** Suppose:

- $X \in \Box_S$ with $X$-colored unit $1_X \in WD(X)$.
- $\epsilon \in WD(O)$ is the empty wiring diagram.
- $\theta_{X,\emptyset} \in WD(X,\emptyset)$ is the 2-cell with input boxes $(X,\emptyset)$ and output box $X$.

Then

$$\theta_{X,\emptyset} \circ (\epsilon) = 1_X \in WD(X). \quad (3.3.8.1)$$

The next relation is the associativity property of 2-cells. It says that, in the picture below, the wiring diagram in the middle can be constructed using two 2-cells, either as the operadic composition on the left or the one on the right.
Proposition 3.3.9. Suppose:

- $\theta_{X,Y,Z} \in \text{WD}(X^0Y^0Z^0)_{X,Y,Z}$ and $\theta_{X,Y} \in \text{WD}(X^0Y^0)_{X,Y}$ are 2-cells.
- $\theta_{X,Y,Z} \in \text{WD}(X^0Y^0Z^0)_{X,Y,Z}$ and $\theta_{Y,Z} \in \text{WD}(Y^0Z^0)_{Y,Z}$ are 2-cells.

Then

$$\theta_{X,Y,Z} \circ_1 (\theta_{X,Y}) = (\theta_{X,Y,Z} \circ_2 (\theta_{Y,Z}) \in \text{WD}(X^0Y^0Z^0). \quad (3.3.9.1)$$

The next relation is the commutativity property of 2-cells and uses the equivariant structure in WD (2.3.1.1).

Proposition 3.3.10. Suppose:

- $\theta_{X,Y} \in \text{WD}(X^0Y^0)_{X,Y}$ is a 2-cell.
- $(1 \ 2) \in \Sigma_2$ is the non-trivial permutation.

Then

$$\theta_{X,Y}(1 \ 2) = \theta_{Y,X} \in \text{WD}(Y^0X^0). \quad (3.3.10.1)$$

The next relation says that substituting a 1-loop inside a 2-cell can be rewritten as substituting a 2-cell inside a 1-loop. It gives two different ways to construct the wiring diagram in the middle in the picture below using a 1-loop and a 2-cell, either as the operadic composition on the left or the one on the right.

Proposition 3.3.11. Suppose:

- $X \in \text{Box}_S$, and $(x_+, x_-) \in X^{\text{out}} \times X^{\text{in}}$ such that $v(x_+) = v(x_-) \in S$.
- $X \setminus x \in \text{Box}_S$ is obtained from $X$ by removing $x_+$.
- $\theta_{X \setminus x,Y} \in \text{WD}(X^{\text{out}}(x)_{X \setminus x,Y})$ and $\theta_{X,Y} \in \text{WD}(X^0Y^0)_{X,Y}$ are 2-cells.
3.3. Elementary Relations

- \( \lambda_{X,x} \in WD^{(X,x)}_{X} \) and \( \lambda_{X,Y,x} \in WD^{(X,Y)\setminus(x)}_{X \times Y} \) are the corresponding 1-loops.

Then

\[
(\theta_{X,x,Y}) \circ (\lambda_{X,x}) = (\lambda_{X,Y,x}) \circ (\theta_{X,Y}) \in WD^{(X,Y)\setminus(x)}_{X \times Y}.
\] (3.3.11.1)

All the relations in the rest of this section can be illustrated with pictures similar to the two previous pictures, each one showing how a wiring diagram can be built in two different ways using operadic compositions. So we will mostly just draw the picture of the wiring diagram being built without the accompanying pictures of the operadic compositions.

The next relation says that substituting an in-split inside a 2-cell can be rewritten as substituting a 2-cell inside an in-split. It gives two different ways to construct the following wiring diagram using an in-split and a 2-cell:

\[
\begin{align*}
X^{\text{in}} \quad & \quad (\text{in split}) \\
\text{case } (x_1 = x_2) & \quad \text{case } (x_1 \neq x_2)
\end{align*}
\]

Proposition 3.3.12. Suppose:

- \( X \in \Box_S \), and \( x_1, x_2 \in X^{\text{in}} \) are distinct elements such that \( v(x_1) = v(x_2) \in S \).
- \( X' = X/(x_1 = x_2) \in \Box_S \) is obtained from \( X \) by identifying \( x_1 \) and \( x_2 \).
- \( \theta_{X',Y} \in WD^{(X',Y)}_{X,Y} \) and \( \theta_{X,Y} \in WD^{(X,Y)}_{X,Y} \) are 2-cells.
- \( \sigma_{X,x_1,x_2} \in WD^{(X)}_{X} \) and \( \sigma_{X,Y,x_1,x_2} \in WD^{(X,Y)}_{X \times Y} \) are in-splits.

Then

\[
(\theta_{X',Y}) \circ (\sigma_{X,x_1,x_2}) = (\sigma_{X,Y,x_1,x_2}) \circ (\theta_{X,Y}) \in WD^{(X,Y)}_{X \times Y} \quad \text{.} \] (3.3.12.1)

The next relation says that substituting an out-split inside a 2-cell can be rewritten as substituting a 2-cell inside an out-split. It gives two different ways to construct the following wiring diagram using an out-split and a 2-cell:

Proposition 3.3.13. Suppose:

- \( X \in \Box_S \), and \( x_1, x_2 \in X^{\text{out}} \) are distinct elements such that \( v(x_1) = v(x_2) \in S \).
Proposition 3.3.14. Suppose:

- $X \in \text{Box}_S$, $x_0 \in X^{\text{in}}$, and $X' = X \setminus \{x_0\} \in \text{Box}_S$ is obtained from $X$ by removing $x_0$.
- $\theta_{X,Y} \in \text{WD}(X_{X,Y}^Y)$ and $\theta_{X',Y} \in \text{WD}(X_{X',Y}^Y)$ are 2-cells.
- $\omega_{X,x_0} \in \text{WD}(X_{X,x_0}^X)$ and $\omega_{X,x_0} \in \text{WD}(X_{X,x_0}^X)$ are 1-wasted wires.

Then

$$(\theta_{X,Y} \circ (\omega_{X,x_0} = (\omega_{X,Y,x_0} \circ (\theta_{X',Y}) \in \text{WD}(X_{X',Y}^Y)).$$

(3.3.14.1)

The following six relations are about 1-loops. The next relation is the commutativity property of 1-loops. It gives two different ways to construct the following wiring diagram using a 1-wasted wire and a 2-cell:

![Wiring Diagram](image)

**Proposition 3.3.15.** Suppose:

- $X \in \text{Box}_S$, $x_1 \neq x_2 \in X^{\text{in}}$, and $x_1 \neq x_2 \in X^{\text{out}}$ such that $v(x_1) = v(x_2) \in S$ and $v(x_1) = v(x_2) \in S$.
- $X \setminus x_1 \setminus x_2$, and $X \setminus x \in \text{Box}_S$ are obtained from $X$ by removing $x_1$, $x_2$, and $\{x_1, x_2\}$, respectively.
Proposition 3.3.16. Suppose:

- \( X \in \Box S, x_-, x_1, x_2 \in X^{in} \) are distinct, and \( x_+ \in X^{out} \) such that \( v(x_+) = v(x_-) \in S \) and \( v(x_1) = v(x_2) \in S \).
- \( X \setminus x \in \Box S \) is obtained from \( X \) by removing \( x_+ \).
- \( X' = X/(x_1 = x_2) \in \Box S \) is obtained from \( X \) by identifying \( x_1 \) and \( x_2 \).
- \( X' \setminus x \in \Box S \) is obtained from \( X' \) by removing \( x_+ \).
- \( \lambda_{X', x} \in WD(X', x)\) and \( \lambda_{X, x} \in WD(X, x)\) are 1-loops.
- \( \sigma_{X, x_1, x_2} \in WD(X, x) \) and \( \sigma_{X \setminus x_1, x_2} \in WD(X \setminus x, x) \) are in-splits.

Then
\[
(\lambda_{X', x}) \circ (\sigma_{X, x_1, x_2}) = (\sigma_{X \setminus x_1, x_2}) \circ (\lambda_{X, x}) \in WD(X, x).
\] (3.3.16.1)

The next relation is the commutativity property between 1-loops and out-splits. It gives two different ways to construct the following wiring diagram using one 1-loop and one out-split:

Proposition 3.3.17. Suppose:

- \( X \in \Box S, (x_+, x_-) \in X^{out} \times X^{in} \) such that \( v(x_+) = v(x_-) \in S \).
- \( x_1 \neq x_2 \in X^{out} \setminus \{x_+\} \) such that \( v(x_1) = v(x_2) \in S \).
- \( X' = X/(x_1 = x_2) \in \Box S \) is obtained from \( X \) by identifying \( x_1 \) and \( x_2 \).
3. Generators and Relations

- \( X \setminus x \in \text{Box}_S \) is obtained from \( X \) by removing \( x \).
- \( X' \setminus x \in \text{Box}_S \) is obtained from \( X' \) by removing \( x \).
- \( \lambda_{X',x} \in \text{WD}(X'_X) \) and \( \lambda_{X,x} \in \text{WD}(X_X) \) are 1-loops.
- \( \sigma^{X,X_1,X_2} \in \text{WD}(X_X) \) and \( \sigma^{X_1,X_2} \in \text{WD}(X'_X) \) are out-splits.

Then
\[
\left( \sigma^{X,X_1,X_2} \right) \circ (\lambda_{X',x}) = (\lambda_{X,x}) \circ \left( \sigma^{X_1,X_2} \right) \in \text{WD}(X'_X). \tag{3.3.17.1}
\]

The next relation is the commutativity property between 1-loops and 1-wasted wires. It gives two different ways to construct the following wiring diagram using one 1-loop and one 1-wasted wire:

Proposition 3.3.18. Suppose:
- \( X \in \text{Box}_S, (x_+, x_-) \in X_{\text{out}} \times X_{\text{in}} \) such that \( v(x_+) = v(x_-) \in S \), and \( x_0 \in X_{\text{in}} \setminus \{x_+\} \).
- \( X' = X \setminus \{x_0\} \in \text{Box}_S \) is obtained from \( X \) by removing \( x_0 \).
- \( X' \setminus x \in \text{Box}_S \) is obtained from \( X' \) by removing \( x_- \).
- \( X \setminus x \in \text{Box}_S \) is obtained from \( X \) by removing \( x_+ \).
- \( \lambda_{X',x} \in \text{WD}(X'_X) \) and \( \lambda_{X,x} \in \text{WD}(X_X) \) are 1-loops.
- \( \omega_{X,X_0} \in \text{WD}(X_X) \) and \( \omega_{X',x_0} \in \text{WD}(X'_X) \) are 1-wasted wires.

Then
\[
(\omega_{X,X_0} \circ (\lambda_{X',x})) = (\lambda_{X,x} \circ (\omega_{X',x_0})) \in \text{WD}(X'_X). \tag{3.3.18.1}
\]

The next relation involves 1-loops, in-splits, and out-splits. It says that the following two wiring diagrams are equal:
The wiring diagram on the left, in which the gray box is called $X'$ below, is created by substituting an in-split into a 1-loop. The wiring diagram on the right is created by substituting an out-split into a 1-loop, which is then substituted into another 1-loop. The inner gray box is called $Y$, and the outer gray box is called $Y \setminus x(1)$ below. In both wiring diagrams, the outermost box is called $X^*$.

**Proposition 3.3.19.** Suppose:

- $Y \in \text{Box}_S$, and $x_1 \neq x_2 \in Y_{\text{out}}$ such that $v(x_1) = v(x_2) \in S$.
- $X = Y/(x_1 = x_2) \in \text{Box}_S$ is obtained from $Y$ by identifying $x_1$ and $x_2$, called $x_{12} \in X_{\text{out}}$.
- $x_1 \neq x_2 \in X_{\text{in}} = Y_{\text{in}}$ such that $v(x_{12}) = v(x_1) = v(x_2) \in S$.
- $X' = X/(x_1 = x_2) \in \text{Box}_S$ is obtained from $X$ by identifying $x_1$ and $x_2$, called $x_{12}$ in $X'$.
- $\sigma_{X,x_1,x_2} \in \text{WD}^{(Y)}(X)$ is an in-split.
- $X^* = X \setminus \{x_{12}, x_1, x_2\} \in \text{Box}_S$ is obtained from $X$ by removing $x_{12}, x_1, \text{ and } x_2$.
- $\lambda_{X',x} \in \text{WD}^{(Y)}(X')$ is the 1-loop in which $x_{12}$ is the supply wire of $x_{12}$.
- $\sigma_{Y,x_1,x_2} \in \text{WD}(Y)$ is an out-split.
- $\lambda_{Y \setminus x(1),x(2)} \in \text{WD}^{(Y \setminus x(1))}(Y)$ is a 1-loop, where $Y \setminus x(1) \in \text{Box}_S$ is obtained from $Y$ by removing $\{x_1, x^1\}$.
- $\lambda_{Y \setminus x(1),x(2)} \in \text{WD}^{(Y \setminus x(1))}(Y)$ is a 1-loop, in which $x_2$ is the supply wire of $x_2$.

Then

$$\lambda_{X',x} \circ (\sigma_{X,x_1,x_2}) = (\lambda_{Y \setminus x(1),x(2)}) \circ (\lambda_{Y \setminus x(1)}) \circ (\sigma_{Y,x_1,x_2}) \in \text{WD}(Y).$$  (3.3.19.1)

The next relation says that the colored unit of a box can be rewritten as the substitution of an out-split into a 1-wasted wire and then into a 1-loop. This is depicted in the picture

in which the outer gray box is called $Z$ and the inner gray box is called $Y$ below.

**Proposition 3.3.20.** Suppose:

- $Z \in \text{Box}_S$, and $(x_1, x^1) \in Z_{\text{in}} \times Z_{\text{out}}$ such that $v(x_1) = v(x^1) \in S$. 

The next relation says that the colored unit of a box can be rewritten as the substitution of an out-split into a 1-wasted wire and then into a 1-loop. This is depicted in the picture

in which the outer gray box is called $Z$ and the inner gray box is called $Y$ below.
3. Generators and Relations

- \( Y = Z \setminus \{ x_1 \} \in \text{Box}_S \) is obtained from \( Z \) by removing \( x_1 \in Z_{\text{in}} \).
- \( x^1 \neq x^2 \in Y_{\text{out}} = Z_{\text{out}} \) such that \( v(x^1) = v(x^2) \in S \).
- \( X = Z \setminus \{ x_1, x^1 \} \in \text{Box}_S \) is obtained from \( Z \) by removing \( \{ x_1, x^1 \} \).
- \( \sigma_{Y, x^1, x^2} \in \text{WD}(X) \) is an out-split in which both \( x_1, x^2 \in Y_{\text{out}} \) have supply wire \( x^2 \in X_{\text{out}} \).
- \( \omega_{Z, x_1} \in \text{WD}(Y) \) is a 1-wasted wire.
- \( \lambda_{Z, x} \in \text{WD}(X) \) is a 1-loop in which \( x_1 \in Z_{\text{out}} \) is the supply wire of \( x_1 \in Z_{\text{in}} \).

Then

\[
(\lambda_{Z, x} \circ (\omega_{Z, x_1}) \circ (\sigma_{Y, x^1, x^2}) = 1_X \in \text{WD}(X). \quad (3.3.20.1)
\]

The following five relations are about in-splits. The next one is the associativity property of in-splits. It gives two different ways to construct the following wiring diagram using two in-splits:

\[
\begin{array}{ccc}
Y_{\text{in}} & \xrightarrow{X} & Y_{\text{out}} \\
\end{array}
\]

**Proposition 3.3.21.** Suppose:

- \( X \in \text{Box}_S \), and \( x_1, x_2, x_3 \in X_{\text{in}} \) are distinct elements such that \( v(x_1) = v(x_2) = v(x_3) \in S \).
- \( X_{12} = X/(x_1 = x_2) \in \text{Box}_S \) is obtained from \( X \) by identifying \( x_1 \) and \( x_2 \), called \( x_{12} \in X_{12}^* \).
- \( X_{23} = X/(x_2 = x_3) \in \text{Box}_S \) is obtained from \( X \) by identifying \( x_2 \) and \( x_3 \), called \( x_{23} \in X_{23}^* \).
- \( Y = X/(x_1 = x_2 = x_3) \in \text{Box}_S \) is obtained from \( X \) by identifying \( x_1, x_2, \) and \( x_3 \).
- \( \sigma_{X_{12}, x_1, x_2} \in \text{WD}(Y) \) and \( \sigma_{X, x_1, x_2} \in \text{WD}(X) \) are in-splits.
- \( \sigma_{X_{23}, x_2, x_3} \in \text{WD}(Y) \) and \( \sigma_{X, x_2, x_3} \in \text{WD}(X) \) are in-splits.

Then

\[
(\sigma_{X_{12}, x_1, x_2}) \circ (\sigma_{X, x_1, x_2}) = (\sigma_{X_{23}, x_1, x_2}) \circ (\sigma_{X, x_1, x_3}) \in \text{WD}(Y). \quad (3.3.21.1)
\]

The next relation is the commutativity property of in-splits. It gives two different ways to construct the following wiring diagram using two in-splits:
Proposition 3.3.22. Suppose:

- $X \in \text{Box}_S$, and $x_1, x_2, x_3, x_4 \in X^{in}$ are distinct elements such that $v(x_1) = v(x_2)$ and $v(x_3) = v(x_4) \in S$.
- $X_{12} = X/(x_1 = x_2) \in \text{Box}_S$ is obtained from $X$ by identifying $x_1$ and $x_2$, called $x_{12} \in X^{in}_{12}$.
- $X_{34} = X/(x_3 = x_4) \in \text{Box}_S$ is obtained from $X$ by identifying $x_3$ and $x_4$, called $x_{34} \in X^{in}_{34}$.
- $Y = X/(x_1 = x_2; x_3 = x_4) \in \text{Box}_S$ is obtained from $X$ by (i) identifying $x_1$ and $x_2$ and (ii) identifying $x_3$ and $x_4$.
- $\sigma_{X_{12},x_3,x_4} \in \text{WD}(Y_{X_{12}})$ and $\sigma_{X,x_1,x_2} \in \text{WD}(X_{x_1})$ are in-splits.
- $\sigma_{X_{34},x_1,x_2} \in \text{WD}(Y_{X_{34}})$ and $\sigma_{X,x_3,x_4} \in \text{WD}(X_{x_3})$ are in-splits.

Then
\[
(\sigma_{X_{12},x_3,x_4} \circ \sigma_{X,x_1,x_2}) = (\sigma_{X_{34},x_1,x_2} \circ \sigma_{X,x_3,x_4}) \in \text{WD}(Y_{X}).
\] (3.3.22.1)

The next relation is the commutativity property between an in-split and an out-split. It gives two different ways to construct the following wiring diagram using one in-split and one out-split:

Proposition 3.3.23. Suppose:

- $Z \in \text{Box}_S$, and $z^1 \neq z^2 \in Z^{out}$ such that $v(z^1) = v(z^2) \in S$.
- $X = Z/(z^1 = z^2) \in \text{Box}_S$ is obtained from $Z$ by identifying $z^1$ and $z^2$.
- $z_1 \neq z_2 \in Z^{in}$ such that $v(z_1) = v(z_2) \in S$.
- $Y = Z/(z_1 = z_2) \in \text{Box}_S$ is obtained from $Z$ by identifying $z_1$ and $z_2$.
- $W = Z/(z_1 = z_2; z^1 = z^2) \in \text{Box}_S$ is obtained from $Z$ by (i) identifying $z_1$ and $z_2$ and (ii) identifying $z^1$ and $z^2$.
- $\sigma_{Y,z^1,z^2} \in \text{WD}(Y_{W})$ is an out-split, and $\sigma_{X,z_1,z_2} \in \text{WD}(X_{Y})$ is an in-split.
- $\sigma_{Z,z_1,z_2} \in \text{WD}(Z_{Y})$ is an in-split, and $\sigma_{Z,z^1,z^2} \in \text{WD}(Z_{X})$ is an out-split.
Then
\[(\sigma_{Y,z_1,z_2}^{\text{in}}) \circ (\sigma_{X,z_1,z_2}^{\text{out}}) = (\sigma_{Z,z_1,z_2}^{\text{in}}) \circ (\sigma_{Z,z_1,z_2}^{\text{out}}) \in \text{WD}(X^Y). \quad (3.3.23.1)\]

The next relation is the commutativity property between an in-split and a 1-wasted wire. It gives two different ways to construct the following wiring diagram using one in-split and one 1-wasted wire:

**Proposition 3.3.24.** Suppose:
- \(Z \in \text{Box}_S\), and \(z_1, z_2 \in Z^{\text{in}}\) are distinct elements such that \(v(z_1) = v(z_2) \in S\).
- \(Y = Z/(z_1 = z_2) \in \text{Box}_S\) is obtained from \(Z\) by identifying \(z_1\) and \(z_2\).
- \(X = Z \setminus \{z\} \in \text{Box}_S\) is obtained from \(Z\) by removing \(z \in Z^{\text{in}}\).
- \(W = X/(z_1 = z_2) \in \text{Box}_S\) is obtained from \(X\) by identifying \(z_1\) and \(z_2\).
- \(\sigma_{X,z_1,z_2} \in \text{WD}(X^W)\) and \(\sigma_{Z,z_1,z_2} \in \text{WD}(X^Y)\) are in-splits.
- \(\omega_{Y,z} \in \text{WD}(Y^W)\) and \(\omega_{Z,z} \in \text{WD}(Y^X)\) are 1-wasted wires.

Then
\[(\omega_{Y,z}) \circ (\sigma_{X,z_1,z_2}) = (\sigma_{Z,z_1,z_2}) \circ (\omega_{Z,z}) \in \text{WD}(X^Y). \quad (3.3.24.1)\]

The next relation says that the colored unit of a box \(X\) can be rewritten as the substitution of a 1-wasted wire into an in-split. This is depicted in the picture:

**Proposition 3.3.25.** Suppose:
- \(Y \in \text{Box}_S\), and \(x, y \in Y^{\text{in}}\) are distinct elements such that \(v(x) = v(y) \in S\).
- \(X = Y/(x = y) \in \text{Box}_S\) is obtained from \(Y\) by identifying \(x\) and \(y\).
- \(\omega_{Y,z} \in \text{WD}(X^Y)\) is a 1-wasted wire.
- \(\sigma_{Y,x,y} \in \text{WD}(X^Y)\) is an in-split.

Then
\[(\sigma_{Y,x,y}) \circ (\omega_{Y,z}) = 1_X \in \text{WD}(X^Y). \quad (3.3.25.1)\]
The following three relations are about out-splits. The next one is the associativity property of out-splits. It gives two different ways to construct the following wiring diagram using two out-splits:

![Wiring Diagram](image)

**Proposition 3.3.26.** Suppose:

- $Y \in \text{Box}_S$, and $y^1, y^2, y^3 \in Y_{\text{out}}$ are distinct elements such that $\nu(y^1) = \nu(y^2) = \nu(y^3) \in S$.
- $Y^{12} = Y/(y^1 = y^2) \in \text{Box}_S$ is obtained from $Y$ by identifying $y^1$ and $y^2$, called $y^{12}$ in $Y^{12}$.
- $Y^{23} = Y/(y^2 = y^3) \in \text{Box}_S$ is obtained from $Y$ by identifying $y^2$ and $y^3$, called $y^{23}$ in $Y^{23}$.
- $X = Y/(y^1 = y^2 = y^3) \in \text{Box}_S$ is obtained from $Y$ by identifying $y^1$, $y^2$, and $y^3$.
- $\sigma^{Y,y^1,y^2} \in \text{WD}(Y_{\text{in}},X)$ and $\sigma^{Y^{12},y^{12},y^3} \in \text{WD}(Y^{12},X)$ are out-splits.
- $\sigma^{Y,y^2,y^3} \in \text{WD}(Y_{\text{in}},X)$ and $\sigma^{Y^{23},y^{23},y^1} \in \text{WD}(X,Y)$ are out-splits.

Then

$$\left(\sigma^{Y,y^1,y^2}\right) \circ \left(\sigma^{Y^{12},y^{12},y^3}\right) = \left(\sigma^{Y,y^2,y^3}\right) \circ \left(\sigma^{Y^{23},y^{23},y^1}\right) \in \text{WD}(Y_{\text{in}},X).$$

**Proposition 3.3.27.** Suppose:

- $Y \in \text{Box}_S$, and $y^1, y^2, y^3, y^4 \in Y_{\text{out}}$ are distinct elements such that $\nu(y^1) = \nu(y^2)$ and $\nu(y^3) = \nu(y^4) \in S$.
- $Y^{12} = Y/(y^1 = y^2) \in \text{Box}_S$ is obtained from $Y$ by identifying $y^1$ and $y^2$.
- $Y^{34} = Y/(y^3 = y^4) \in \text{Box}_S$ is obtained from $Y$ by identifying $y^3$ and $y^4$.
- $X = Y/(y^1 = y^2; y^3 = y^4) \in \text{Box}_S$ is obtained from $Y$ by (i) identifying $y^1$ and $y^2$ and (ii) identifying $y^3$ and $y^4$.
- $\sigma^{Y,y^1,y^2} \in \text{WD}(Y_{\text{in}},Y)$ and $\sigma^{Y^{12},y^{12},y^3} \in \text{WD}(Y^{12},X)$ are out-splits.
Generators and Relations

\[ \sigma_{Y,Y^3,Y^4} \in \text{WD}(Y) \text{ and } \sigma_{Y^3,Y^1,Y^2} \in \text{WD}(Y) \text{ are out-splits.} \]

Then
\[ (\sigma_{Y,Y^3,Y^4}) \circ (\sigma_{Y^3,Y^1,Y^2}) = (\sigma_{Y,Y^3,Y^4}) \circ (\sigma_{Y^3,Y^1,Y^2}) \in \text{WD}(X). \] (3.3.27.1)

The next relation is the commutativity property between an out-split and a 1-wasted wire. It gives two different ways to construct the following wiring diagram using one out-split and one 1-wasted wire:

![Wiring Diagram](image)

**Proposition 3.3.28.** Suppose:

- \( Y \in \text{Box}_S \), \( y \in Y^\text{in} \), and \( y^1, y^2 \in Y^\text{out} \) such that \( v(y^1) = v(y^2) \in S \).
- \( W = Y \setminus \{y\} \in \text{Box}_S \) is obtained from \( Y \) by identifying \( y^1 \) and \( y^2 \).
- \( Z = Y \setminus \{y\} \in \text{Box}_S \) is obtained from \( Y \) by removing \( y \in Y^\text{in} \).
- \( X = Z \setminus \{y^1, y^2\} \in \text{Box}_S \) is obtained from \( Y \) by identifying \( y^1 \) and \( y^2 \).
- \( \sigma_{Z,Y^1,Y^2} \in \text{WD}(Z) \) and \( \sigma_{Y,Y^1,Y^2} \in \text{WD}(Y) \) are out-splits.
- \( \omega_{Y,y} \in \text{WD}(Y) \) and \( \omega_{W,y} \in \text{WD}(W) \) are 1-wasted wires.

Then
\[ (\omega_{Y,y}) \circ (\sigma_{Z,Y^1,Y^2}) = (\sigma_{Y,Y^1,Y^2}) \circ (\omega_{W,y}) \in \text{WD}(X). \] (3.3.28.1)

The final relation is the commutativity property of 1-wasted wires. It gives two different ways to construct the following wiring diagram using two 1-wasted wires:

![Wiring Diagram](image)

**Proposition 3.3.29.** Suppose:

- \( Y \in \text{Box}_S \), and \( y_1, y_2 \in Y^\text{in} \) are distinct elements.
- \( Y_1 = Y \setminus \{y_1\} \in \text{Box}_S \) is obtained from \( Y \) by removing \( y_1 \).
- \( Y_2 = Y \setminus \{y_2\} \in \text{Box}_S \) is obtained from \( Y \) by removing \( y_2 \).
- \( X = Y \setminus \{y_1, y_2\} \in \text{Box}_S \) is obtained from \( Y \) by removing \( y_1 \) and \( y_2 \).
- \( \omega_{Y,y_1} \in \text{WD}(Y) \) and \( \omega_{Y_1,y_2} \in \text{WD}(Y) \) are 1-wasted wires.
• $\omega_{Y,y_2} \in WD(\mathcal{Y}_1)$ and $\omega_{Y_2,y_1} \in WD(\mathcal{Y}_2)$ are 1-wasted wires.

Then
\[
(\omega_{Y,y_1} \circ \omega_{Y_2,y_2}) = (\omega_{Y,y_2} \circ \omega_{Y_2,y_1}) \in WD(\mathcal{Y}_1).
\]

(3.3.29.1)

Definition 3.3.30. The 28 relations (3.3.2.1)–(3.3.29.1) are called elementary relations.

3.4. Summary of Chapter

(1) There are eight generating wiring diagrams in $WD$.

(2) Each internal wasted wire can be generated using a 1-wasted wire and a 1-loop.

(3) There are twenty-eight elementary relations in $WD$. 

Chapter 4

Decomposition of Wiring Diagrams

As part of the finite presentation theorem for the operad WD of wiring diagrams (Theorem 5.2.11), in Theorem 5.1.11 we will observe that each wiring diagram has a highly structured decomposition into generating wiring diagrams (Def. 3.1.9), called a stratified presentation. Stratified presentations are also needed to establish the second part of the finite presentation theorem for WD regarding relations. The purpose of this chapter is to provide all the steps needed to establish the existence of a stratified presentation for each wiring diagram. We remind the reader about Notation 3.3.1 for (iterated) operadic compositions.

In Section 4.1 we show that each wiring diagram \( \psi \) has a specific operadic decomposition (4.1.7.1)

\[
\psi = \alpha \circ \varphi.
\]

An explanation of this decomposition is given just before Def. 4.1.5. The idea of this decomposition is that we are breaking the complexity of a general wiring diagram into two simpler parts. On the one hand, the inner wiring diagram \( \varphi \) contains all the input boxes and the delay nodes of \( \psi \), but its supplier assignment is as simple as possible, namely the identity map. See Lemmas 4.1.8 and 4.1.10. On the other hand, the outer wiring diagram \( \alpha \) has only one input box and no delay nodes, but its supplier assignment is equal to that of \( \psi \).

In Section 4.2 we observe that the outer wiring diagram \( \alpha \) in the previous decomposition of \( \psi \) can be decomposed as (4.2.6.1)

\[
\alpha = \pi_1 \circ \pi_2.
\]
Example 4.2.3 has a concrete wiring diagram that illustrates this decomposition. The idea of this decomposition is that in a wiring diagram there are usually wires that go backward (i.e., "point to the left"), as in (2.2.18.1), in a 1-loop (Def. 3.1.5), and in the pictures just before Prop. 3.3.11 and Prop. 3.3.15. This decomposition breaks the complexity of the wiring diagram $\alpha$ into two simpler parts. On the one hand, the outer wiring diagram $\pi_1$ contains all the backward-going wires in $\alpha$ but no wasted wires or split wires (Lemma 4.2.7). On the other hand, the inner wiring diagram $\pi_2$ contains no backward-going wires, but it has all the wasted wires and split wires in $\alpha$.

In Section 4.3, we observe that the wiring diagram $\pi_2$ in the previous decomposition of $\alpha$ can be decomposed further as 

$$\pi_2 = \beta_1 \circ \beta_2 \circ \beta_3.$$ 

Example 4.3.2 has a concrete wiring diagram that illustrates this decomposition. In this decomposition:

- The outermost wiring diagram $\beta_1$ is an iterated operadic composition of 1-wasted wires (Lemma 4.3.6).
- The middle wiring diagram $\beta_2$ is an iterated operadic composition of in-splits (Lemma 4.3.9).
- The innermost wiring diagram $\beta_3$ is an iterated operadic composition of out-splits (Lemma 4.3.12).

By convention an empty operadic composition means a colored unit. In summary, for a wiring diagram $\psi$, we will decompose it as

$$\psi = \pi_1 \circ \beta_1 \circ \beta_2 \circ \beta_3 \circ \varphi.$$ 

### 4.1. Factoring Wiring Diagrams

**Assumption 4.1.1.** Throughout this chapter, fix a class $S$. Suppose

$$\psi = (D\psi, v_\psi, s_\psi) \in WD(\frac{1}{2})$$

is a wiring diagram with:

- output box $Y \in Box_S$ and input boxes $X = (X_1, \ldots, X_N)$ for some $N \geq 0$;
- $r$ delay nodes $D\psi = \{d_1, \ldots, d_r\}$ for some $r \geq 0$;
- value assignment $v_\psi : Y^{\text{in}} \cup X^{\text{out}} \cup X^{\text{in}} \cup X^{\text{out}} \cup D\psi \longrightarrow S$, where $X^{\text{in}} = \bigsqcup_{i=1}^{N} X_i^{\text{in}}$ and $X^{\text{out}} = \bigsqcup_{i=1}^{N} X_i^{\text{out}}$;
- supplier assignment $s_\psi : Dm_\psi \longrightarrow Sp_\psi$.

Since $N = 0$ and $r = 0$ are both allowed, $\psi$ is a general wiring diagram. Furthermore:
4.1. Factoring Wiring Diagrams

(1) To simplify notation, we will write \( v_\psi(d_i) \in S \) simply as \( d_i \), so each \( \delta_{d_i} \in WD^{(i)} \) is a 1-delay node (Def. 3.1.2).

(2) \( X = \bigsqcup_{i=1}^N X_i \in \Box S \) is the coproduct of the \( X_i \)'s.

(3) Define \( X' \in \Box S \) as

\[
X'^{\text{in}} = X^{\text{in}} \cup DN_\psi \quad \text{and} \quad X'^{\text{out}} = X^{\text{out}} \cup DN_\psi. \tag{4.1.1.2}
\]

Motivation 4.1.2. The first observation is about the marginal case where \( \psi \) has no input boxes and no delay nodes. So it looks like this

with finitely many, possibly zero, external wasted wires. In any case, it can be written in terms of the empty wiring diagram and finitely many 1-wasted wires.

Lemma 4.1.3. Suppose \( N = r = 0 \) in \( \psi \); i.e., \( \psi \in WD^{(i)} \) has no input boxes and no delay nodes. Then one of the following two statements is true.

1. \( \psi = \epsilon \in WD^{(i)} \), the empty wiring diagram (Def. 3.1.1).

2. There exist 1-wasted wires (Def. 3.1.8) \( \omega_1, \ldots, \omega_m \), where \( m = |Y^{\text{in}}| > 0 \), such that

\[
\psi = \omega_1 \circ \cdots \circ \omega_m \circ \epsilon. \tag{4.1.3.1}
\]

Proof. Since \( X^{\text{in}} = X^{\text{out}} = DN_\psi = \emptyset \), the supplier assignment of \( \psi \) is a function

\[
Dm_\psi = Y^{\text{out}} \xrightarrow{s} Y^{\text{in}} = Sp_\psi.
\]

The non-instantaneity requirement (2.2.13.2) then implies \( Y^{\text{out}} = \emptyset \). If \( m = |Y^{\text{in}}| = 0 \), then \( Y \) is the empty box and \( \psi = \epsilon \), the empty wiring diagram, by definition.

If \( m > 0 \), then every global input \( y \in Y^{\text{in}} = \{y_1, \ldots, y_m\} \) is an external wasted wire, and the supplier assignment \( s : Y^{\text{out}} = \emptyset \longrightarrow Y^{\text{in}} \) is the trivial map. For each \( 1 \leq j \leq m \), define the box

\[
Y_j = \begin{cases} 
Y & \text{if } j = 1; \\
Y \setminus \{y_1, \ldots, y_{j-1}\} & \text{if } 2 \leq j \leq m; \\
\emptyset & \text{if } j = m + 1.
\end{cases}
\]

Each \( \omega_{Y_j} \in WD^{(Y_j)} \) is a 1-wasted wire. Using the notation (3.3.1.2), the iterated composition

\[
\omega_{Y_1} \circ \cdots \circ \omega_{Y_m} \circ \epsilon \in WD^{(i)}
\]
is then a wiring diagram with output box \( Y_1 = Y \), no input boxes and no delay nodes, and supplier assignment \( \emptyset = Y^{\text{out}} \rightarrow Y^{\text{in}} \) the trivial map. This is the same as \( \psi \).

Next, for wiring diagrams \( \psi \) not necessarily covered by Lemma 4.1.3 we define two relatively simple wiring diagrams that will be shown to provide a decomposition for \( \psi \). Each of these two simpler wiring diagrams will then be analyzed further.

**Motivation 4.1.4.** This decomposition for \( \psi \) is depicted in the following picture:

![Diagram](image)

Here the intermediate gray box is \( X' \) \(^{4.1.1.2}\). In this decomposition, the inside wiring diagram \( \varphi \) has all the input boxes and the delay nodes of \( \psi \), but its supplier assignment is the identity function. The outside wiring diagram \( \alpha \) has a single input box \( X' \) and no delay nodes, but it has the same supplier assignment as \( \psi \).

**Definition 4.1.5.** Suppose \( \psi \) is as in Assumption 4.1.1. Define the wiring diagram

\[
\varphi = (\text{DN}_\varphi, v_\varphi, s_\varphi) \in \text{WD}(X')
\]

with:

- output box \( X' \) \(^{4.1.1.2}\) and input boxes \( X = (X_1, \ldots, X_N) \);
- delay nodes \( \text{DN}_\varphi = \text{DN}_\psi = \{d_1, \ldots, d_r\} \);
- supplier assignment

\[
\begin{align*}
\text{Dm}_\varphi &= X'^{\text{out}} \cup X^{\text{in}} \cup \text{DN}_\varphi = (X'^{\text{out}} \cup \text{DN}_\varphi) \cup (X^{\text{in}} \cup \text{DN}_\varphi) \\
\text{Sp}_\varphi &= X^{\text{in}} \cup X'^{\text{out}} \cup \text{DN}_\varphi = (X^{\text{in}} \cup \text{DN}_\varphi) \cup (X'^{\text{out}} \cup \text{DN}_\varphi)
\end{align*}
\]
the identity function that sends $X'\text{out}$ to $(X'\text{out} \cup DN_\psi)$ and $(X'\text{in} \cup DN_\psi)$ to $X'\text{in}$. 

**Definition 4.1.6.** Suppose $\psi$ is as in Assumption 4.1.1. Define the wiring diagram

$$\alpha = (DN_\alpha, v_\alpha, s_\alpha) \in WD^{(Y)}_{(X')}(4.1.6.1)$$

with:

- one input box $X'$ (4.1.2) and output box $Y$;
- no delay nodes;
- supplier assignment

$$Dm_\alpha = Y'\text{out} \cup X'\text{in} = Y'\text{out} \cup X'\text{in} \cup DN_\psi = Dm_\psi$$

$$Sp_\alpha = Y'\text{in} \cup X'\text{out} = Y'\text{in} \cup X'\text{out} \cup DN_\psi = Sp_\psi$$

equal to $s_\psi$.

**Lemma 4.1.7.** Given a wiring diagram $\psi$ (4.1.1), there is a decomposition

$$\psi = \alpha \circ \varphi \in WD^{(Y)}_{(X)}(4.1.7.1)$$

in which $\alpha \in WD^{(Y)}_{(X)}$ is as in (4.1.6.1) and $\varphi \in WD^{(Y)}_{(X)}$ is as in (4.1.5.1).

**Proof.** By the definition of $\circ$ (Def. 2.3.4), $\alpha \circ \varphi = \alpha \circ_1 \varphi$ belongs to $WD^{(Y)}_{(X)}$ and has $DN_\varphi = DN_\psi$ as its set of delay nodes. It remains to check that its supplier assignment is equal to that of $\psi$. This follows from a direct inspection because $s_\varphi$ is the identity function, while $s_\alpha = s_\psi$. □

To obtain the desired stratified presentation of $\psi$, we now begin to analyze the wiring diagram $\varphi$.

**Lemma 4.1.8.** Consider the wiring diagram $\varphi$ (4.1.5.1).

1. If $N = r = 0$, then $\varphi = \epsilon$, the empty wiring diagram (Def. 3.1.1).
2. If $(N, r) = (1, 0)$, then $\varphi = 1_{X_1}$, the colored unit of $X_1$ (Def. 2.3.2).
3. If $(N, r) = (0, 1)$, then $\varphi = \delta_{d_1}$, a 1-delay node (Def. 3.1.2).

**Proof.** All three cases are checked by direct inspection. □

**Motivation 4.1.9.** Next we observe that, for higher values of $N + r$, the wiring diagram $\varphi$ is generated by 2-cells (Def. 3.1.4) and 1-delay nodes via iterated operadic compositions, as depicted in the following picture.
The operadic composition $\gamma$ is used in the following observation.

**Lemma 4.1.10.** Suppose $N + r \geq 2$ in the wiring diagram $\varphi \in \text{WD}(\mathcal{C})$. Then it admits a decomposition

$$\varphi = \gamma \left( \theta \left( \{1_{X_i}\}_{i=1}^{N}, \{\delta_{d_j}\}_{j=1}^{r} \right) \right).$$

(4.1.10.1)

Here

$$\theta = \begin{cases} \theta_1 & \text{if } N + r = 2, \\ \theta_1 \circ_2 \left( \cdots \circ_2 \left( \theta_{N+r-2} \circ_2 \theta_{N+r-1} \right) \right) & \text{if } N + r > 2 \end{cases}$$

(4.1.10.2)

with each $\theta_k$ a 2-cell, and each $\delta_{d_j} \in \text{WD}(d_j)$ is a 1-delay node as in Assumption 4.1.1.

**Proof.** Recall that $X = (X_1, \ldots, X_N)$ and $\text{DN}_\varphi = \text{DN}_\psi = \{d_1, \ldots, d_r\}$. For $N + 1 \leq j \leq N + r$ define the box $X_j = d_j \in \text{Box}_S$ as

$$X_j^\text{in} = \{d_j\} = X_j^\text{out}.$$  

For $1 \leq i \leq N + r$ define the box

$$X^{\text{2d}} = \prod_{p=i}^{N+r} X_p \in \text{Box}_S.$$  

Note that $X^{\text{2d}} = X'$. Next, for $1 \leq k \leq N + r - 1$, define the 2-cell

$$\theta_k = \theta_{X_{k}X_{k+1}} \in \text{WD}(\mathcal{C}_{X_{k}X_{k+1}}).$$

Then we have a wiring diagram

$$\theta \in \text{WD}(\mathcal{C}_{X_1X_N})$$

in which $\theta^*$ is defined as in (4.1.10.2). Since $1_{X_i} \in \text{WD}(X_i)$ and $\delta_{d_j} \in \text{WD}(d_j)$, the operadic composition on the right side of (4.1.10.1) is defined and belongs to $\text{WD}(\mathcal{C})$.

Since the two sides of (4.1.10.1) both have delay nodes $\{d_1, \ldots, d_r\}$, it remains to check that the supplier assignment of the right side is equal to $s_\varphi = \text{Id}$. This follows from a direct inspection because (i) colored units (Def. 2.3.2), 1-delay nodes (Def.
and 2-cells (Def. 3.1.4) all have identity supplier assignments and because
(ii) \(\gamma_{(2.1.12.1)}\) is an iteration of various \(\circ\) (Def. 2.3.4).

## 4.2. Unary Wiring Diagrams

In this section, we analyze wiring diagrams with exactly one input box and no delay nodes, such as \(\alpha_{(4.1.6.1)}\). We will show that such a wiring diagram can be generated by the generating wiring diagrams (Def. 3.1.9) of name changes (Def. 3.1.3), 1-loops (Def. 3.1.5), 1-wasted wires (Def. 3.1.8), in-splits (Def. 3.1.6), and out-splits (Def. 3.1.7), in this order. We remind the reader of Notation 3.3.1 for (iterated) \(\circ\).

We will need a few definitions and notations.

**Definition 4.2.1.** Suppose \(\pi \in \text{WD}(\_x)\) is a wiring diagram with one input box \(X\) and no delay nodes.

1. A **loop element** in \(\pi\) is an element \(x \in X^{\text{out}}\) such that there exists \(x' \in X^{\text{in}}\) with \(x\) as its supply wire. The set of loop elements in \(\pi\) is denoted by \(\pi^{lp}\).
2. An element \(x' \in X^{\text{in}}\) is said to be **internally supplied** if \(s_{\pi}(x') \in X^{\text{out}}\). The set of such elements in \(\pi\) is denoted by \(\pi^{sp}_{+}\).
3. An element \(x' \in X^{\text{in}}\) is said to be **externally supplied** if \(s_{\pi}(x') \in Y^{\text{in}}\). The set of such elements in \(\pi\) is denoted by \(\pi^{sp}_{-}\).

Recall from Definition 2.2.13 the concepts of external wasted wires \(\pi^{w}_{-}\) and of internal wasted wires \(\pi^{w}_{+}\) of a wiring diagram \(\pi\).

**Lemma 4.2.2.** Suppose \(\pi \in \text{WD}(\_x)\) is a wiring diagram with one input box \(X\) and no delay nodes. Then:

1. \(\pi^{sp}_{+} \cup \pi^{sp}_{-} = X^{\text{in}}\).
2. \(\pi^{w}_{+} \cup \pi^{lp} \subseteq X^{\text{out}}\).
3. \(s_{\pi}(\pi^{sp}_{+}) = \pi^{lp}\).
4. \(s_{\pi}(\pi^{sp}_{+}) \cup \pi^{w}_{-} = Y^{\text{in}}\).
5. \(s_{\pi}(Y^{\text{out}}) \subseteq X^{\text{out}} \setminus \pi^{w}_{+}\).

**Proof.** All the statements are immediate from the definitions.

**Example 4.2.3.** Consider the wiring diagram \(\pi \in \text{WD}(\_x)\) as depicted in the picture
Decomposition of Wiring Diagrams

\[ \pi \]

with

- \( X^{in} = \{x_1, x_2, x_3, x_4\} \), \( X^{out} = \{x^1, x^2, x^3\} \), \( Y^{in} = \{y_1, y_2\} \), and \( Y^{out} = \{y^1, y^2\} \);
- \( \pi^{lp} = \{x^1\} \), \( \pi^{sp}_{+} = \{x_1, x_2\} \), \( \pi^{sp}_{-} = \{x_3, x_4\} \), \( \pi^{w}_{+} = \{x^3\} \), and \( \pi^{w}_{-} = \{y_1\} \).

Note that we may operadically decompose \( \pi \) as follows.

\[ \pi = \pi_1 \circ \pi_2 \]

The point of this decomposition is that the inner wiring diagram \( \pi_2 \) is generated by:

- two 1-wasted wires, one for the external wasted wire \( y_1 \) and the other for the internal wasted wire \( x^3 \);
- two in-splits, one for \( \{x_1, x_2\} \) and the other for \( \{x_3, x_4\} \);
- one out-split for \( x^1 \), which is the supply wire of \( y^1, x_1 \), and \( x_2 \).

At the same time, the outer wiring diagram \( \pi_1 \) is generated by two 1-loops, one for the loop element \( x^1 \) and the other for the internal wasted wire \( x^3 \).

With this example as a guide, next we will factor a general wiring diagram with one input box and no delay nodes into two wiring diagrams. The outer wiring diagram will be generated by name changes and 1-loops. The inner wiring diagram will be generated by 1-wasted wires, in-splits, and out-splits. The intermediate gray box in (4.2.3.1) will be called \( Z \) below.

Convention 4.2.4. Using the five elementary relations (3.3.3.1), (3.3.4.1), (3.3.5.1), (3.3.6.1), and (3.3.7.1), name changes can always be rewritten on the outside (i.e., left side) of an iterated operadic composition in WD. Moreover, using the elementary relation (3.3.2.1), an iteration of name changes can be composed down into just one name change. To simplify the presentation, in what follows these elementary relations regarding name changes are automatically applied wherever necessary. With this in mind, we will mostly not mention name changes.
For a wiring diagram with one input box and no delay nodes, we will decompose it using the wiring diagrams in the next definition.

**Definition 4.2.5.** Suppose \( \pi \in \text{WD}(Y_X) \) is a wiring diagram with one input box \( X \) and no delay nodes.

1. Define the box \( Z \in \text{Box}_S \) as
   \[
   Z^\text{in} = Y^\text{in} \cup \pi^w_+ \cup \pi^l_p;
   \]
   \[
   Z^\text{out} = Y^\text{out} \cup \pi^w_+ \cup \pi^l_p.
   \]

2. Define the wiring diagram \( \pi_1 \in \text{WD}(Y_Z) \) with:
   - one input box \( Z \), output box \( Y \), and no delay nodes;
   - supplier assignment
   \[
   Dm_{\pi_1} = Y^\text{out} \cup Z^\text{in} = Y^\text{out} \cup [Y^\text{in} \cup \pi^w_+ \cup \pi^l_p] \]
   \[
   s_{\pi_1} \downarrow
   \]
   \[
   Sp_{\pi_1} = Y^\text{in} \cup Z^\text{out} = Y^\text{in} \cup [Y^\text{out} \cup \pi^w_+ \cup \pi^l_p]
   \]
   the identity function.

3. Define the wiring diagram \( \pi_2 \in \text{WD}(Z_X) \) with:
   - one input box \( X \), output \( Z \), and no delay nodes;
   - supplier assignment
   \[
   Dm_{\pi_2} = Z^\text{out} \cup X^\text{in} = [Y^\text{out} \cup \pi^w_+ \cup \pi^l_p] \cup [\pi^s_p \cup \pi^{sp}_p] \]
   \[
   s_{\pi_2} \downarrow
   \]
   \[
   Sp_{\pi_2} = Z^\text{in} \cup X^\text{out} = [Y^\text{in} \cup \pi^w_+ \cup \pi^l_p] \cup X^\text{out}
   \]
   whose restriction to:
   - \( Y^\text{out} \) is \( s_\pi : Y^\text{out} \rightarrow X^\text{out} \);
   - \( \pi^w_+ \cup \pi^l_p \) is the subset inclusion into \( X^\text{out} \);
   - \( \pi^s_p \) is \( s_\pi : \pi^{sp}_p \rightarrow \pi^l_p \);
   - \( \pi^{sp}_p \) is \( s_\pi : \pi^{sp}_p \rightarrow Y^\text{in} \).

This is well-defined by the non-instantaneity requirement (2.2.13.2) for \( \pi \) and Lemma 4.2.2.

An example of the following decomposition is the picture (4.2.3.1) above.

**Lemma 4.2.6.** Suppose \( \pi \in \text{WD}(Y_X) \) is a wiring diagram with one input box \( X \) and no delay nodes. Then it admits a decomposition
\[
\pi = \pi_1 \circ \pi_2
\]
(4.2.6.1)
in which \( \pi_1 \in \text{WD}(Y_Z) \) and \( \pi_2 \in \text{WD}(Z_X) \) are as in Def. 4.2.5.
Proof. Both sides of (4.2.6.1) belong to WD(Y) and have no delay nodes. So it remains to check that the supplier assignment s of π₁ ∘ π₂ is equal to sₚ. Note that
\[ Dm_{π₁ ∘ π₂} = Y^{out} ⊔ X^{in} = Y^{out} ⊔ [π₁^{sp} ⊔ π₂^{sp}] . \]
By the definitions of ∘ = o₁ (Def. 2.3.4), sₚ₁ (4.2.5.1), and sₚ₂ (4.2.5.2):
- on \( Y^{out} \) the supplier assignment s is \( s_{π₂} s_{π₁} = s_π \),
- on \( π₁^{sp} ⊔ π₂^{sp} \) the supplier assignment s is \( s_{π₂} s_{π₁} = \text{Id} s_π = s_π \).

So the supplier assignment of \( π₁ ∘ π₂ \) is equal to \( s_π \). □

To obtain the desired stratified presentation of \( π_1 \), next we observe that \( π_1 \) in Def. 4.2.5 is either a colored unit (2.3.2.1) or an iterated operadic composition of 1-loops (Def. 3.1.5). An example of \( π_1 \) is the outer wiring diagram in the example (4.3.1).

Lemma 4.2.7. Suppose:
- \( Y, Z \in \text{Box}_S \) such that \( Z^{in} = Y^{in} \sqcup T \) and \( Z^{out} = Y^{out} \sqcup T \) for some \( T \in \text{Fin}_S \),
- \( ζ \in WD(Y) \) is a wiring diagram with no delay nodes and with supplier assignment
  \[ Dm_ζ = Y^{out} \sqcup Z^{in} = Y^{out} \sqcup [Y^{in} \sqcup T] \]
  \[ S_ζ = Y^{in} \sqcup Z^{out} = Y^{in} \sqcup [Y^{out} \sqcup T] \]

the identity function.

Then the following statements hold.

1. \( ζ = 1_Y \) if \( T = \emptyset \).
2. If \( p = |T| > 0 \), then there exist 1-loops \( λ_1, \ldots, λ_p \) such that
   \[ ζ = λ_1 ∘ \cdots ∘ λ_p . \]  

Proof. If \( T = \emptyset \), then \( ζ \in WD(Y) \) has no delay nodes and has supplier assignment \( s_ζ = \text{Id} \). So \( ζ \) is the \( Y \)-colored unit.

Next suppose \( T = \{t₁, \ldots, t_p\} \) with \( p > 0 \). For the definitions below, it is convenient to keep in mind the following picture of \( ζ \):
For $0 \leq j \leq p$ define the box $Y_j \in \text{Box}_S$ as

$$Y_j = \begin{cases} Y & \text{if } j = 0; \\ Y \cup \{t_1, \ldots, t_j\} & \text{if } 1 \leq j \leq p. \end{cases}$$

Here $Y \cup \{t_1, \ldots, t_j\}$ means a copy of $t_i$ for $1 \leq i \leq j$ is added to each of $Y^\text{in}$ and $Y^\text{out}$. In particular, we have $Y_p = Z$. For $1 \leq j \leq p$ define the 1-loop

$$\lambda_j = \lambda_{Y_j, t_j} \in \text{WD}(Y_j)$$

in which $t_j \in Y_j^\text{in}$ has supply wire $t_j \in Y_j^\text{out}$.

The iterated operadic composition

$$\lambda_1 \circ \cdots \circ \lambda_p \in \text{WD}(Y_p) = \text{WD}(Z)$$

has no delay nodes. To see that it is equal to $\zeta$, it remains to check that its supplier assignment is equal to $s_\zeta = \text{Id}$. This holds because each 1-loop $\lambda_j$ has identity supplier assignment.

Observe that Lemma 4.2.7 applies to $\pi_1 \in \text{WD}(Z)$ in Def. 4.2.5 with $T = \pi^w_+ \cup \pi^p$. So $\pi_1$ is either the $Y$-colored unit or an iterated operadic composition of 1-loops.

### 4.3. Unary Wiring Diagrams with No Loop Elements

In order to show that the wiring diagram $\pi_2 \in \text{WD}(Z)$ in Def. 4.2.5 is generated by 1-wasted wires, in-splits, and out-splits, first we identify its external wasted wires, internal wasted wires, and loop elements.

**Lemma 4.3.1.** Consider the wiring diagram $\pi_2 \in \text{WD}(Z)$ in Def. 4.2.5.

1. The set of external wasted wires in $\pi_2$ is $\pi^w_2^- = \pi^w_+ \cup \pi^w$.  
2. The set of internal wasted wires in $\pi_2$ is $\pi^w_2^+ = \emptyset$.  
3. The set of loop elements in $\pi_2$ is $\pi^p_2 = \emptyset$.  
4. $s_{\pi_2}(Z^\text{out}) = X^\text{out}$.  
5. $Z^\text{in} = \pi^w_+ \cup \pi^w \cup s_{\pi_2}(X^\text{in})$.

**Proof.**

1. By definition an external wasted wire in $\pi_2$ is an element in $Z^\text{in}$ that is not in the image of $s_{\pi_2} \ (\ref{def:4.2.5})$. By the definition of $s_{\pi_2}$, this is the subset

$$\pi^w_+ \cup [Y^\text{in} \setminus s_{\pi}(\pi^\text{sp}^p)] \subseteq Z^\text{in}.$$

It follows from the non-instantaneity requirement (\ref{def:2.2.13}) for $\pi$ that

$$Y^\text{in} \setminus s_{\pi}(\pi^\text{sp}^p) = \pi^w_-. $$
(2) By definition an internal wasted wire in \( \pi_2 \) is an element in \( X^{\text{out}} \) that is not in the image of \( s_{\pi_2} \). An element of \( X^{\text{out}} \) is either an internal wasted wire in \( \pi \), or else it is the \( s_{\pi} \)-image of an element in \( \pi^{\text{sp}} \cup Y^{\text{out}} \). Since
\[
X^{\text{out}} = \pi^w_+ \cup s_{\pi} \left( \pi^{\text{sp}}_+ \cup Y^{\text{out}} \right) \\
= \pi^w_+ \cup \left[ \pi^l_+ \cup s_{\pi}(Y^{\text{out}}) \right],
\]
an inspection of the definition of \( s_{\pi_2} \) reveals that all of \( X^{\text{out}} \) is in the image of \( s_{\pi_2} \). So \( \pi_2 \) has no internal wasted wires.

(3) By definition a loop element in \( \pi_2 \) is an element in \( X^{\text{out}} \) that is the supply wire, under \( s_{\pi_2} \), of some element in \( X^{\text{in}} \). Since \( X^{\text{in}} = \pi^{\text{sp}}_+ \cup \pi^{\text{sp}}_- \), the definition of \( s_{\pi_2} \) yields
\[
s_{\pi_2} \left( \pi^{\text{sp}}_+ \cup \pi^{\text{sp}}_- \right) = s_{\pi} \left( \pi^{\text{sp}}_+ \right) \cup s_{\pi} \left( \pi^{\text{sp}}_- \right) \subseteq \pi^l_+ \cup Y^{\text{in}} \subseteq Z^{\text{in}} = \text{Sp}_{\pi_2} \setminus X^{\text{out}}.
\]
So \( \pi_2 \) has no loop elements.

(4) By (2) \( \pi_2 \) has no internal wasted wires, so \( X^{\text{out}} = s_{\pi_2} \left( Z^{\text{out}} \cup \pi^{\text{sp}}_+ \right) \). But by (3) \( \pi_2 \) has no loop elements, so \( \pi^{\text{sp}}_+ = \emptyset \) and \( X^{\text{out}} = s_{\pi_2} \left( Z^{\text{out}} \right) \).

(5) Since \( \pi_2 \) has no loop elements by (3), \( s_{\pi_2} \left( X^{\text{in}} \right) \subseteq Z^{\text{in}} \). An element in \( Z^{\text{in}} \) that is not in \( s_{\pi_2} \left( X^{\text{in}} \right) \) is precisely an external wasted wire in \( \pi_2 \). By (1) the set of external wasted wires in \( \pi_2 \) is \( \pi^w_+ \cup \pi^w_- \).

\[\square\]

Continuing our analysis of wiring diagrams with one input box and no delay nodes, our next goal is to construct a decomposition for \( \pi_2 \) (Def. 4.2.5) involving 1-wasted wires, in-splits, and out-splits.

**Example 4.3.2.** Consider the inner wiring diagram \( \pi_2 \in \text{WD}(\chi^e) \) in the example 4.2.3.1, which is depicted in the following picture.

For this wiring diagram, the desired decomposition is depicted in the picture:
4.3. Unary Wiring Diagrams with No Loop Elements

The inner gray box will be called $V$, and the outer gray box will be called $W$ below. Note that:

- The outermost wiring diagram $\beta_1 \in WD(\tilde{\beta})$ is generated by two 1-wasted wires.
- The middle wiring diagram $\beta_2 \in WD(\tilde{\nu})$ is generated by two in-splits.
- The innermost wiring diagram $\beta_3 \in WD(\tilde{\nu})$ is an out-split.

For a general wiring diagram with one input box, no delay nodes, no loop elements, and no internal wasted wires, such a decomposition uses the following definitions.

**Definition 4.3.3.** Suppose $X, Z \in \text{Box}_S$ and $\beta \in WD(\tilde{\nu})$ is a wiring diagram with no delay nodes and no loop elements.

1. Suppose the box $W = Z \setminus \beta_w \in \text{Box}_S$ is obtained from $Z \in \text{Box}_S$ by removing the external wasted wires of $\beta$, so $W^{\text{in}} = Z^{\text{in}} \setminus \beta_w$ and $W^{\text{out}} = Z^{\text{out}}$.

2. Define the wiring diagram $\beta_1 \in WD(\tilde{\nu})$ as having:
   - no delay nodes;
   - supplier assignment
     \[
     \begin{align*}
     &D_m \beta_1 = Z^{\text{out}} \uplus W^{\text{in}} = Z^{\text{out}} \uplus [Z^{\text{in}} \setminus \beta_w] \\
     \quad s_{\beta_1} \downarrow \\
     &S_p \beta_1 = Z^{\text{in}} \uplus W^{\text{out}} = Z^{\text{in}} \uplus Z^{\text{out}}
     \end{align*}
     \]
   the identity function on $Z^{\text{out}}$ and the subset inclusion on $Z^{\text{in}} \setminus \beta_w \subseteq Z^{\text{in}}$.

3. Define the box $V \in \text{Box}_S$ as $V^{\text{in}} = X^{\text{in}}$ and $V^{\text{out}} = Z^{\text{out}} = W^{\text{out}}$.

4. Define the wiring diagram $\beta_2 \in WD(\tilde{\nu})$ as having:
   - no delay nodes;
   - supplier assignment
     \[
     \begin{align*}
     &D_m \beta_2 = W^{\text{out}} \uplus V^{\text{in}} = W^{\text{out}} \uplus X^{\text{in}} \\
     \quad s_{\beta_2} \downarrow \\
     &S_p \beta_2 = W^{\text{in}} \uplus V^{\text{out}} = [Z^{\text{in}} \setminus \beta_w] \uplus W^{\text{out}}
     \end{align*}
     \]
   the coproduct of the identity function on $W^{\text{out}}$ and the restriction of the supplier assignment $s_{\beta} : X^{\text{in}} \rightarrow Z^{\text{in}} \setminus \beta_w$.
   This is well-defined because $\beta$ has no delay nodes and no loop elements.

5. Define the wiring diagram $\beta_3 \in WD(\tilde{\nu})$ as having:
   - no delay nodes;
• supplier assignment

\[
\begin{align*}
\text{Dm}_{\beta_3} &= V^\text{out} \cup X^\text{in} = Z^\text{out} \cup X^\text{in} \\
\text{Sp}_{\beta_3} &= V^\text{in} \cup X^\text{out} = X^\text{in} \cup X^\text{out}
\end{align*}
\]

(4.3.3.3)

\[
\begin{array}{c}
\text{s}_{\beta_3} \\
\downarrow \\
\text{Sp}_{\beta_3} = V^\text{in} \cup X^\text{out} = X^\text{in} \cup X^\text{out}
\end{array}
\]

the coproduct of the identity function on \(X^\text{in}\) and \(s_\beta : Z^\text{out} \rightarrow X^\text{out}\).

This is well-defined because \(\beta\) has no delay nodes and because of the non-instantaneity requirement (2.2.13.2) for \(\beta\).

Lemma 4.3.4. In the context of Def. 4.3.3

(1) The map \(s_\beta : X^\text{in} \rightarrow Z^\text{in} \setminus \beta^\text{out}\), which is part of \(s_{\beta_3}\), is surjective.

(2) If \(\beta\) has no internal wasted wires (such as \(\pi_2\) in Def. 4.2.5), then the map \(s_\beta : Z^\text{out} \rightarrow X^\text{out}\), which is part of \(s_{\beta_3}\), is surjective.

Proof. The first assertion is true because \(\beta\) has no delay nodes and because of the non-instantaneity requirement (2.2.13.2). The second assertion is true because \(\beta\) has no delay nodes and no loop elements. \(\square\)

Lemma 4.3.5. In the context of Def. 4.3.3, there is a decomposition

\[
\beta = \beta_1 \circ \beta_2 \circ \beta_3 \in \text{WD}(\mathcal{X}).
\]

(4.3.5.1)

Proof. By construction the iterated operadic composition \(\beta_1 \circ \beta_2 \circ \beta_3\) also belongs to \(\text{WD}(\mathcal{X})\) and has no delay nodes. So it remains to check that its supplier assignment \(s\) is equal to \(s_\beta\). A direct inspection of (4.3.3.1), (4.3.3.2), and (4.3.3.3) reveals that:

• on \(X^\text{in} \subseteq \text{Dm}_{\beta_3}\) the supplier assignment \(s\) is given by \(\text{Id}_{\beta_3} \text{Id}_{X^\text{in}} = s_{\beta_3}\);

• on \(Z^\text{out} \subseteq \text{Dm}_{\beta_1}\) the supplier assignment \(s\) is given by \(s_{\beta_3} \text{Id}_{Z^\text{out}} \text{Id}_{Z^\text{out}} = s_{\beta_3}\).

So the supplier assignment of \(\beta_1 \circ \beta_2 \circ \beta_3\) is equal to \(s_\beta\). \(\square\)

Note that the decomposition in Lemma 4.3.5 applies to \(\pi_2\) because \(\pi_2\) has one input box, no delay nodes, and no loop elements (by Lemma 4.3.1).

Next we show that in the decomposition 4.3.5.1

(1) \(\beta_1\) is either a colored unit (Def. 2.3.2) or an iterated operadic composition of 1-wasted wires (Def. 3.1.8). See Lemma 4.3.6

(2) \(\beta_2\) is either a colored unit or an iterated operadic composition of in-splits (Def. 3.1.6). See Lemma 4.3.9
(3) If $\beta$ has no internal wasted wires, such as $\pi_2$ by Lemma 4.3.1, then $\beta_3$ is either a colored unit or an iterated operadic composition of out-splits (Def. 3.1.7). See Lemma 4.3.12.

During the first reading, the reader may wish to skip the proofs of the following Lemmas and simply look at the pictures. The following observation deals with the first statement.

**Lemma 4.3.6.** Consider the wiring diagram $\beta_1 \in WD(Z)$ in Def. 4.3.3.

1. If $\beta_w = \emptyset$ (i.e., $\beta$ has no external wasted wires), then $\beta_1 = 1_Z$, the $Z$-colored unit.
2. If $q = |\beta_w^w| > 0$, then there exist 1-wasted wires $\omega_1, \ldots, \omega_q$ such that
   \[
   \beta_1 = \omega_1 \circ \cdots \circ \omega_q. \tag{4.3.6.1}
   \]

**Proof.** Recall that $\beta_1$ has no delay nodes and has supplier assignment (4.3.3.1)
\[
\begin{align*}
Dm_{\beta_1} &= Z^{\text{out}} \cup W^{\text{in}} = Z^{\text{out}} \cup \left[ Z^{\text{in}} \setminus \beta_w^w \right] \\
Sp_{\beta_1} &= Z^{\text{in}} \cup W^{\text{out}} = Z^{\text{in}} \cup Z^{\text{out}}
\end{align*}
\]
that is the identity function on $Z^{\text{out}}$ and the subset inclusion on $Z^{\text{in}} \setminus \beta_w^w$. If $\beta_w^w = \emptyset$, then $s_{\beta_1} = \text{Id}$ and, therefore, $\beta_1$ is the colored unit.

Next suppose $\beta_w^w = \{w_1, \ldots, w_q\} \subseteq Z^{\text{in}}$ with $q > 0$. Recall that $W = Z \setminus \beta_w^w$. For $0 \leq j \leq q$ define the box
\[
Z_j = \begin{cases} 
Z & \text{if } j = 0 \\
Z \setminus \{w_1, \ldots, w_j\} & \text{if } 1 \leq j \leq q.
\end{cases}
\]
So in particular $Z_q = W$. The iterated operadic composition on the right side of (4.3.6.1) is represented in the following picture.

Here the outermost box is $Z$, the outermost gray box is $Z_1$, and the innermost gray box is $Z_{q-1}$.

For $1 \leq j \leq q$ define the 1-wasted wires (Def. 3.1.8)
\[
\omega_j = \omega_{Z_{j-1}, w_j} \in WD(Z_j).
\]
The iterated operadic composition
\[ \omega_1 \circ \cdots \circ \omega_q \in \text{WD}\left(\frac{Z}{n}\right) = \text{WD}\left(\frac{W}{n}\right) \]
has no delay nodes. So to prove (4.3.6.1), it remains to check that its supplier assignment \( s \) is equal to \( s_{\beta_1} \).

- On \( Z^{\text{out}} \subseteq Dm_{\omega_1} \) the supplier assignment \( s \) is the composition of \( q \) copies of the identity function, hence is the identity function.
- On \( W^{\text{in}} \subseteq Dm_{\omega_q} \) the supplier assignment \( s \) is the composition of the inclusions \( Z_j^{\text{in}} \rightarrow Z_{j-1}^{\text{in}} \) for \( 1 \leq j \leq q \), which is the inclusion \( W^{\text{in}} \rightarrow Z^{\text{in}} \).

\[ \square \]

**Motivation 4.3.7.** To show that \( \beta_2 \) is either a colored unit or an iterated composition of in-splits, we first need a lemma that says that the following wiring diagram is generated by in-splits.

![Wiring Diagram](image)

**Lemma 4.3.8.** Suppose:

- \( X, Y \in \text{Box}_S \) such that \( X^{\text{out}} = Y^{\text{out}} \).
- There exist \( y \in Y^{\text{in}} \) and distinct elements \( x_1, \ldots, x_k \in X^{\text{in}} \) with \( k \geq 1 \) such that
  \[ X^{\text{in}} = \left[ Y^{\text{in}} \setminus \{y\} \right] \cup \{x_1, \ldots, x_k\} \]
  and \( v(y) = v(x_i) \in S \) for all \( i \).
- \( \sigma \in \text{WD}(X) \) is a wiring diagram with no delay nodes and with supplier assignment
  \[ \text{Dm}_\sigma = Y^{\text{out}} \uplus X^{\text{in}} = Y^{\text{out}} \uplus \left[ Y^{\text{in}} \setminus \{y\} \right] \cup \{x_1, \ldots, x_k\} \]
  \[ \text{Sp}_\sigma = Y^{\text{in}} \uplus X^{\text{out}} = Y^{\text{in}} \uplus Y^{\text{out}} \]
  given by
  \[ s_\sigma(z) = \begin{cases} 
  y & \text{if } z = x_1, \ldots, x_k; \\
  z & \text{if } z \in Y^{\text{out}} \uplus \left[ Y^{\text{in}} \setminus \{y\} \right].
  \end{cases} \]

Then:

1. \( \sigma \) is the \( Y \)-colored unit if \( k = 1 \);
2. \( \sigma \) is an iterated operadic composition of \((k - 1)\) in-splits if \( k \geq 2 \).
Proof. Since \( \sigma \) has no delay nodes, if \( k = 1 \), then \( s_\sigma = \text{Id} \). So \( \sigma \) is a colored unit.

Suppose \( k \geq 2 \). We will prove that \( \sigma \) is an iterated operadic composition of \((k - 1)\) in-splits by induction on \( k \). If \( k = 2 \), then by definition \( \sigma \) is the in-split \( \sigma_{X,x_1,x_2} \) (Def. 3.1.6).

Suppose \( k \geq 3 \). We will factor \( \sigma \) into two wiring diagrams as depicted in the picture

in which the intermediate gray box will be called \( W \) below. The outer wiring diagram \( \sigma_1 \) will be an in-split, and the inner wiring diagram \( \sigma_2 \) will be an iterated operadic composition of \((k - 2)\) in-splits. To define such a decomposition, we will need the following definitions.

1. Suppose \( W \in \text{Box}_S \) such that \( W^\text{out} = Y^\text{out} = X^\text{out} \) and

\[
W^\text{in} = [Y^\text{in} \setminus \{y\}] \cup \{x',x_k\}
\]

for some \( x_k \neq x' \) such that \( v(x') = v(x_k) \in S \). In particular, we have

\[
X^\text{in} = [W^\text{in} \setminus \{x'\}] \cup \{x_1, \ldots, x_{k-1}\}.
\]  
(4.3.8.1)

2. Define the wiring diagram \( \sigma_1 \in \text{WD}(W) \) with no delay nodes and with supplier assignment

\[
\begin{align*}
\text{Dm}_{\sigma_1} &= Y^\text{out} \sqcup W^\text{in} = Y^\text{out} \sqcup [Y^\text{in} \setminus \{y\}] \cup \{x',x_k\} \\
\text{Sp}_{\sigma_1} &= Y^\text{in} \sqcup W^\text{out} = [Y^\text{in} \setminus \{y\}] \cup \{y\} \sqcup Y^\text{out}
\end{align*}
\]

given by

\[
s_{\sigma_1}(z) = \begin{cases} 
  y & \text{if } z = x', x_k; \\
  z & \text{otherwise}.
\end{cases}
\]
(3) Define the wiring diagram \( \sigma_2 \in WD(X) \) with no delay nodes and with supplier assignment

\[
D_{\sigma_2} = W^{\text{out}} \sqcup X^{\text{in}} = W^{\text{out}} \sqcup \left[ Y^{\text{in}} \setminus \{y\} \right] \sqcup \{x_1, \ldots, x_{k-1}\} \sqcup \{x_k\}
\]

\[
S_{\sigma_2} = W^{\text{in}} \sqcup X^{\text{out}} = \left[ Y^{\text{in}} \setminus \{y\} \right] \sqcup \{x', x_k\} \sqcup W^{\text{out}}
\]

given by

\[
s_{\sigma_2}(z) = \begin{cases} 
  x' & \text{if } z = x_1, \ldots, x_{k-1}; \\
  z & \text{otherwise}.
\end{cases}
\]

Then \( \sigma_1 \circ \sigma_2 \in WD(Y) \) is a wiring diagram with no delay nodes. To see that it is equal to \( \sigma \), it suffices to check that the supplier assignment of \( \sigma_1 \circ \sigma_2 \) is equal to \( s_{\sigma} \). This is true by a direct inspection of \( s_{\sigma_1} \) and \( s_{\sigma_2} \).

By definition \( \sigma_1 \) is the in-split \( \sigma_{W,x',x_k} \). By (4.3.8.1) the induction hypothesis applies to \( \sigma_2 \), which says that it is an iterated operadic composition of \((k-2)\) in-splits. Combined with the previous paragraph, it follows that \( \sigma = \sigma_1 \circ \sigma_2 \) is the iterated operadic composition of \((k-1)\) in-splits, finishing the induction. \( \Box \)

Next we consider \( \beta_2 \).

**Lemma 4.3.9.** The wiring diagram \( \beta_2 \in WD(Y) \) in Def. 4.3.3 is either a colored unit or an iterated operadic composition of in-splits.

**Proof.** Recall that \( W^{\text{in}} = Z^{\text{in}} \setminus \beta^w \), \( V^{\text{in}} = X^{\text{in}} \), and \( V^{\text{out}} = Z^{\text{out}} = W^{\text{out}} \). The wiring diagram \( \beta_2 \in WD(Y) \) has no delay nodes and has supplier assignment \( [4.3.3.2] \)

\[
D_{\beta_2} = W^{\text{out}} \sqcup V^{\text{in}} = Z^{\text{out}} \sqcup X^{\text{in}}
\]

\[
S_{\beta_2} = W^{\text{in}} \sqcup V^{\text{out}} = [Z^{\text{in}} \setminus \beta^w] \sqcup Z^{\text{out}}
\]

the coproduct of the identity function on \( Z^{\text{out}} \) and \( s_\beta : X^{\text{in}} \rightarrow Z^{\text{in}} \setminus \beta^w \). Write \( W^{\text{in}} = Z^{\text{in}} \setminus \beta^w = \{z_1, \ldots, z_p\} \), so each \( s^{-1}_\beta(z_i) \) is non-empty by Lemma [4.3.4]

If \( p = 0 \), then \( Z^{\text{in}} \setminus \beta^w = \emptyset = X^{\text{in}} \), and \( \beta_2 \) is the \( W \)-colored unit.

Suppose \( p > 0 \). We will write \( \beta_2 \) as an iterated composition as in the following picture.
4.3. Unary Wiring Diagrams with No Loop Elements

There are $p - 1$ gray boxes. The outermost gray box will be called $W_1$, and the innermost gray box will be called $W_{p-1}$ below. To define such a decomposition, we will need the following definitions.

(1) For $0 \leq j \leq p$ define the box $W_j \in \text{Box}_S$ with $W_j^{\text{out}} = W^{\text{out}}$ and

$$W_j^{\text{in}} = \begin{cases} \bigcup_{i=1}^{j} s^{-1}_\beta(z_i) \cup \{z_{j+1}, \ldots, z_p\} & \text{if } j \neq 0, p \\ \emptyset & \text{if } j = 0, p \end{cases}$$

Note that $W_0^{\text{in}} = W^{\text{in}}$ by definition, while $W_p^{\text{in}} = X^{\text{in}} = V^{\text{in}}$ by Lemma 4.3.4. So $W_0 = W$ and $W_p = V$.

(2) For $1 \leq j \leq p$ define the wiring diagram $\sigma_j \in \text{WD}(W_j^{\text{in}}, W_j^{\text{out}})$ with no delay nodes and with supplier assignment

$$\text{Dm}_{\sigma_j} = W_{j-1}^{\text{out}} \cup W_j^{\text{in}} = W^{\text{out}} \sqcup \bigcup_{i=1}^{j-1} s^{-1}_\beta(z_i) \cup \{z_{j+1}, \ldots, z_p\}$$

and

$$\text{Sp}_{\sigma_j} = W_{j-1}^{\text{in}} \cup W_j^{\text{out}} = \bigcup_{i=1}^{j-1} s^{-1}_\beta(z_i) \cup \{z_{j+1}, \ldots, z_p\} \cup W^{\text{out}}$$

given by

$$s_{\sigma_j}(x) = \begin{cases} z_j & \text{if } x \in s^{-1}_\beta(z_j) \\ x & \text{otherwise.} \end{cases}$$

Since

$$W_j^{\text{in}} = \left[ W_{j-1}^{\text{in}} \setminus \{z_j\} \right] \cup s^{-1}_\beta(z_j),$$

by Lemma 4.3.8 $\sigma_j$ is:

- a colored unit if $|s^{-1}_\beta(z_j)| = 1$;
- an iterated operadic composition of $(|s^{-1}_\beta(z_j)| - 1)$ in-splits if $|s^{-1}_\beta(z_j)| \geq 2$. 

Therefore, to show that $\beta_2$ is either a colored unit or an iterated operadic composition of in-splits, it is enough to check that there is a decomposition

$$\beta_2 = \sigma_1 \circ \cdots \circ \sigma_p \in \text{WD}^{\text{W}}(Y).$$

Since the iterated operadic composition on the right has no delay nodes, it remains to check that its supplier assignment $s$ is equal to $s_{\beta_2}$ \((4.3.3.2)\).

On $W^{\text{out}} = Z^{\text{out}} \subseteq Dm_{\sigma}$, the supplier assignment $s$ is the composition of $p$ identity functions, hence the identity function. On

$$V^{\text{in}} = X^{\text{in}} = \prod_{i=1}^{p} s_{\beta_2}^{-1}(z_i) \subseteq Dm_{\sigma},$$

the supplier assignment $s$ sends elements in each $s_{\beta_2}^{-1}(z_i)$ to $z_i \in W^{\text{in}}$, so it is equal to $s_{\beta_2}$. □

**Motivation 4.3.10.** Next, to show that $\beta_3$ is either a colored unit or an iterated operadic composition of out-splits, we first need a lemma that says that the following wiring diagram is generated by out-splits.

![Wiring Diagram]

The following observation is the out-split analogue of Lemma \((4.3.8)\).

**Lemma 4.3.11.** Suppose:

- $X, Y \in \text{Box}_S$ such that $X^{\text{in}} = Y^{\text{in}}$.
- There exist $x \in X^{\text{out}}$ and distinct elements $y_1, \ldots, y_k \in Y^{\text{out}}$ with $k \geq 1$ such that $Y^{\text{out}} = [X^{\text{out}} \setminus \{x\}] \cup \{y_1, \ldots, y_k\}$

and $v(x) = v(y_i) \in S$ for $1 \leq i \leq k$.

- $\sigma \in \text{WD}(X)$ is a wiring diagram with no delay nodes and with supplier assignment

$$Dm_{\sigma} = Y^{\text{out}} \cup X^{\text{in}} = [X^{\text{out}} \setminus \{x\}] \cup \{y_1, \ldots, y_k\} \cup X^{\text{in}}$$

$$s_{\sigma} : X^{\text{out}} \rightarrow X^{\text{in}}$$

given by

$$s_{\sigma}(z) = \begin{cases} x & \text{if } z = y_1, \ldots, y_k; \\ z & \text{if } z \in [X^{\text{out}} \setminus \{x\}] \cup X^{\text{in}}. \end{cases}$$

Then:
4.3. Unary Wiring Diagrams with No Loop Elements

(1) \( \sigma \) is the \( Y \)-colored unit if \( k = 1 \);

(2) \( \sigma \) is an iterated operadic composition of \((k - 1)\) out-splits if \( k \geq 2 \).

**Proof.** If \( k = 1 \), then \( s_\sigma \) is the identity function, so \( \sigma \) is a colored unit.

The assertion for \( k \geq 2 \) is proved by induction. If \( k = 2 \), then \( \sigma \) is by definition the out-split \( \sigma^{Y,y_1,y_2} \) (Def. 3.1.7).

Suppose \( k \geq 3 \). We will factor \( \sigma \) into two wiring diagrams as depicted in the picture

![Wiring Diagram](image)

in which the intermediate gray box will be called \( W \) below. The inner wiring diagram \( \sigma^2 \) will be an out-split, and the outer wiring diagram \( \sigma^1 \) will be an iterated operadic composition of \((k - 2)\) out-splits. To define such a decomposition, we will need the following definitions.

(1) Define the box \( W \in \text{Box}_S \) with \( W^{in} = X^{in} = Y^{in} \) and

\[
W^{out} = [X^{out} \setminus \{x\}] \cup \{w, y_k\}
\]

for some \( w \neq y_k \) such that \( v(w) = v(y_k) \in S \). In particular, we have

\[
Y^{out} = [W^{out} \setminus \{w\}] \cup \{y_1, \ldots, y_{k-1}\}.
\] (4.3.11.1)

(2) Define the wiring diagram \( \sigma^1 \in \text{WD}^Y(W) \) with no delay nodes and with supplier assignment

\[
\begin{align*}
\text{Dm}_{\sigma^1} &= Y^{out} \cup W^{in} = [X^{out} \setminus \{x\}] \cup \{y_1, \ldots, y_k\} \cup Y^{in} \\
\text{Sp}_{\sigma^1} &= Y^{in} \cup W^{out} = Y^{in} \cup [X^{out} \setminus \{x\}] \cup \{w, y_k\}
\end{align*}
\]

given by

\[
s_{\sigma^1}(z) = \begin{cases} 
    w & \text{if } z = y_1, \ldots, y_{k-1}; \\
    z & \text{otherwise.}
\end{cases}
\]
(3) Define the wiring diagram $\sigma^2 \in WD_{\lambda}^{(V)}$ with no delay nodes and with supplier assignment

$$
\begin{align*}
\text{Dm}_{\sigma^2} &= W^{\text{out}} \sqcup X^{\text{in}} = [X^{\text{out}} \setminus \{x\}] \sqcup \{w, y_k\} \sqcup W^{\text{in}} \\
\text{Sp}_{\sigma^2} &= W^{\text{in}} \sqcup X^{\text{out}}
\end{align*}
$$

given by

$$
\begin{align*}
\sigma^2(z) = \begin{cases} 
  x & \text{if } z = w, y_k; \\
  z & \text{otherwise.}
\end{cases}
\end{align*}
$$

Then $\sigma \circ \sigma^2 \in WD^{(V)}_{\lambda}$ is a wiring diagram with no delay nodes. To see that it is equal to $\sigma$, it suffices to check that the supplier assignment of $\sigma^1 \circ \sigma^2$ is equal to $s_{\sigma}$. This is true by a direct inspection of $s_{\sigma^1}$ and $s_{\sigma^2}$.

By (4.3.11.1) the induction hypothesis applies to $\sigma^1$, which says that it is an iterated operadic composition of $(k - 2)$ out-splits. By definition $\sigma^2$ is the out-split $\sigma^{W, w, y_k}$. Combined with the previous paragraph, it follows that $\sigma = \sigma^1 \circ \sigma^2$ is the iterated operadic composition of $(k - 1)$ out-splits, finishing the induction. □

Finally, we consider $\beta_3$.

**Lemma 4.3.12.** In the context of Def. 4.3.3, suppose $\beta$ has no internal wasted wires (such as $\pi_2$ by Lemma 4.3.7). Then $\beta^3 \in WD_{\lambda}^{(V)}$ is either a colored unit or an iterated operadic composition of out-splits.

**Proof.** Recall that the wiring diagram $\beta^3 \in WD_{\lambda}^{(V)}$ has no delay nodes and has supplier assignment

$$
\begin{align*}
\text{Dm}_{\beta^3} &= V^{\text{out}} \sqcup X^{\text{in}} = Z^{\text{out}} \sqcup X^{\text{in}} \\
\text{Sp}_{\beta^3} &= V^{\text{in}} \sqcup X^{\text{out}} = X^{\text{in}} \sqcup X^{\text{out}}
\end{align*}
$$

the coproduct of the identity function on $X^{\text{in}}$ and $s_{\beta} : Z^{\text{out}} \longrightarrow X^{\text{out}}$. Since $\beta$ has no internal wasted wires, by Lemma 4.3.4 the map $s_{\beta} : Z^{\text{out}} \longrightarrow X^{\text{out}}$ is surjective.

Write $X^{\text{out}} = \{x_1, \ldots, x_r\}$, so $Z^{\text{out}} = \bigsqcup_{i=1}^{r} s_{\beta}^{-1}(x_i)$ with each $s_{\beta}^{-1}(x_i)$ non-empty. If $r = 0$, then $X^{\text{out}} = \emptyset = Z^{\text{out}}$, and $\beta_3$ is a colored unit.

Suppose $r > 0$. We will decompose $\beta_3$ as in the picture:
4.3. Unary Wiring Diagrams with No Loop Elements

The outermost gray box will be called $V_1$, and the innermost gray box will be called $V_{r-1}$ below. To define such a decomposition, we first need some definitions.

1. For $0 \leq j \leq r$ define the box $V_j \in \text{Box}_S$ with $V_j^{\text{in}} = V_1$ and $V_j^{\text{out}} = \{x_1, \ldots, x_j\}$.

$$V_j^{\text{out}} = \begin{cases} \emptyset & \text{if } j = 0 \\ \bigcup_{i=j+1}^{r} s_{\beta}^{-1}(x_i) & \text{if } j = r \\ \bigcup_{i=j+1}^{r} s_{\beta}^{-1}(x_i) \cup X_1 & \text{otherwise} \\ \end{cases}$$

Note that $V_0^{\text{out}} = Z^{\text{out}} = V^{\text{out}}$, so $V_0 = V$. Also, $V_r^{\text{out}} = X^{\text{out}}$, so $V_r = X$.

2. For $1 \leq j \leq r$ define the wiring diagram $\sigma^j \in \text{WD}(V_j)$ with no delay nodes and with supplier assignment

$$\text{Dm}_{\sigma^j} = V_j^{\text{in}} \cup V_j^{\text{out}} = \{x_1, \ldots, x_{j-1}\} \cup \bigcup_{i=j+1}^{r} s_{\beta}^{-1}(x_i) \cup X_1$$

$$\text{Sp}_{\sigma^j} = \begin{cases} x_i & \text{if } z \in s_{\beta}^{-1}(x_i); \\ z & \text{otherwise} \\ \end{cases}$$

The iterated operadic composition

$$\sigma^1 \circ \cdots \circ \sigma^r \in \text{WD}^{(V_0)} = \text{WD}^{(V)}$$

has no delay nodes. To see that it is equal to $\beta_3$, it remains to check that the former’s supplier assignment $s$ is equal to $s_{\beta_3}$.

- On $X^{\text{in}} \subseteq \text{Dm}_{\sigma^r}$ the supplier assignment $s$ is the composition of $r$ identity functions, hence the identity function.

- On $V^{\text{out}} = Z^{\text{out}} \subseteq \text{Dm}_{\sigma^1}$ the supplier assignment $s$ sends elements in each $s_{\beta}^{-1}(x_i)$ to $x_i$. 

4. Decomposition of Wiring Diagrams

So $s$ is equal to $s_{\beta_3}$.

By Lemma [4.3.11] each $\sigma^j$ for $1 \leq j \leq r$ is either a colored unit or an iterated operadic composition of out-splits. Therefore, $\beta_3 = \sigma^1 \circ \cdots \circ \sigma^r$ is either a colored unit or an iterated operadic composition of out-splits. □

4.4. Summary of Chapter 4

(1) A wiring diagram with no input boxes and no delay nodes is generated by the empty wiring diagram and a finite number of 1-wasted wires.

(2) Every wiring diagram $\psi$ has a decomposition

$$\psi = \pi_1 \circ \beta_1 \circ \beta_2 \circ \beta_3 \circ \varphi$$

in which:

- $\pi_1$ is generated by 1-loops;
- $\beta_1$ is generated by 1-wasted wires;
- $\beta_2$ is generated by in-splits;
- $\beta_3$ is generated by out-splits;
- $\varphi$ is either the empty wiring diagram or is generated by 2-cells and 1-delay nodes.
Fix a class $S$, with respect to which the Box$_S$-colored operad $WD$ of wiring diagrams is defined (Theorem 2.3.11). The main purpose of this chapter is to establish finite presentations for the operad $WD$ of wiring diagrams and its variants $WD_{\bullet}$ and $WD_0$. For the operad $WD$, our finite presentation means the following two statements.

(1) The 8 generating wiring diagrams (Def. 3.1.9) generate the operad $WD$. This means that every wiring diagram can be expressed as a finite iterated operadic composition involving only generating wiring diagrams.

(2) If a wiring diagram can be operadically generated by the generating wiring diagrams in two different ways, then there exists a finite sequence of elementary equivalences from the first iterated operadic composition to the other one. An elementary equivalence is induced by either an elementary relation (Def. 3.3.30) or an operad associativity/unity axiom for the generating wiring diagrams.

In Chapter 6 we will use these finite presentations to describe algebras over the operads $WD$, $WD_{\bullet}$, and $WD_0$ in terms of finitely many generating structure maps and generating axioms corresponding to the generating wiring diagrams and elementary relations. In Section 6.3 we will use the finite presentation for WD-algebras to study the propagator algebra. In Section 6.7 we will use the finite presentation for $WD_0$-algebras to study the algebra of open dynamical systems.

In Section 5.1 we establish the first part of the finite presentation theorem for $WD$ by showing that every wiring diagram has a stratified presentation (Theorem 5.1.11). A stratified presentation (Def. 5.1.9) is a highly structured iterated operadic composition of the generating wiring diagrams. The proof of the second part of the finite presentation theorem also requires the use of stratified presentations.
In Section 5.2 we establish the second part of the finite presentation theorem for WD. We show that any two presentations of the same wiring diagram in terms of generating wiring diagrams are connected by a finite sequence of elementary equivalences (Theorem 5.2.11).

In Section 5.3 we establish a finite presentation for the operad WD$_*$ of wiring diagrams without delay nodes, which we call normal wiring diagrams. Normal wiring diagrams appeared in Spivak’s study of mode-dependent networks and dynamical systems [Spi15][Spi15b].

In Section 5.4 we restrict further and establish a finite presentation for the operad WD$_0$ of wiring diagrams without delay nodes and whose supplier assignments are bijections. We call them strict wiring diagrams. They appeared in [VSL15]. We will use strict wiring diagrams in Section 6.7 to study the algebra of open dynamical systems.

5.1. Stratified Presentation

In this section, we define a stratified presentation and show that every wiring diagram has a stratified presentation (Theorem 5.1.11). We also need the concept of a simplex to discuss generators and relations in the operad WD of wiring diagrams.

**Motivation 5.1.1.** In plain language, a simplex is a finite parenthesized word whose alphabets are generating wiring diagrams, in which each pair of parentheses has a well defined associated operadic composition. In particular, a simplex has a well defined operadic composition. As we have seen in Chapter 3, it is often possible to express a wiring diagram as an operadic composition of generating wiring diagrams in multiple ways. In other words, a wiring diagram can have many different simplex presentations. We now start to develop the necessary language to say precisely that any two such simplex presentations of the same wiring diagram are equivalent in some way.

**Definition 5.1.2.** Suppose $n \geq 1$. An $n$-simplex $\Psi$ and its composition $|\Psi| \in WD$ are defined inductively as follows.

1. A 1-simplex is a generating wiring diagram (Def. 3.1.9) $\psi$. Its composition $|\psi|$ is defined as $\psi$ itself.

2. Suppose $n \geq 2$ and that $k$-simplices for $1 \leq k \leq n - 1$ and their compositions in WD are already defined. An $n$-simplex is a tuple $\Psi = (\psi, i, \phi)$ consisting of
   - an integer $i \geq 1$,
   - a $p$-simplex $\psi$ for some $p \geq 1$, and
   - a $q$-simplex $\phi$ for some $q \geq 1$

   such that:
   - (i) $p + q = n$;
5.1. Stratified Presentation

(ii) the operadic composition

\[
|\Psi| \overset{\text{def}}{=} |\psi| \circ_i |\phi|
\]

(5.1.2.1)

is defined in WD (Def. 2.3.4).

The wiring diagram \(|\Psi|\) in (5.1.2.1) is the composition of \(\Psi\).

A simplex in WD is an \(m\)-simplex in WD for some \(m \geq 1\). We say that a simplex \(\Psi\) is a presentation of the wiring diagram \(|\Psi|\).

**Notation 5.1.3.** To simplify notations, we will sometimes use the right side of (5.1.2.1) to denote a simplex. To simplify notations even further, we may even just list the generating wiring diagrams \((\psi_1, \ldots, \psi_n)\) in a simplex in the order in which they appear in the composition (5.1.2.1), omitting all the pairs of parentheses and the operadic compositions from the notations.

**Remark 5.1.4.** In Def. 5.1.2 we could have made the definition for a general operad \(O\) other than WD, using a specified collection of elements in \(O\) in place of the generating wiring diagrams. Such a definition would be useful in discussing generators and relations in a general operad \(O\).

In the next three Examples, every \(\psi_i\) denotes a generating wiring diagram, and we will use Notation 5.1.3.

**Example 5.1.5.** A 2-simplex has the form \((\psi_1, i, \psi_2)\), which we abbreviate to \(\psi_1 \circ_i \psi_2\), for some integer \(i \geq 1\). For instance, suppose \(d \in S\), and \(X\) is the box with \(X^{\text{in}} = \{d\} = X^{\text{out}}\). Suppose \(Y\) is an arbitrary box. Then there is a 2-simplex

\[(\theta_{X,Y}, 1, \delta_d)\]

in which \(\theta_{X,Y}\) is a 2-cell (Def. 3.1.4) and \(\delta_d\) is a 1-delay node (Def. 3.1.2). Its composition \(\theta_{X,Y} \circ_1 \delta_d\) is the wiring diagram

![Diagram](image)

in WD\((X,Y)\) with one delay node.

**Example 5.1.6.** A 3-simplex is an iterated operadic composition in WD of the form

\[(\psi_1 \circ_i \psi_2) \circ_j \psi_3 \quad \text{or} \quad \psi_1 \circ_i (\psi_2 \circ_j \psi_3)\]

for some integers \(i, j \geq 1\). Once again these are really abbreviations for the 3-simplices

\[((\psi_1, i, \psi_2), j, \psi_3) \quad \text{or} \quad (\psi_1, i, (\psi_2, j, \psi_3)).\]
For instance, continuing the example above, suppose $\lambda_{X,Y,Y,d} \in WD(Y)$ is a 1-loop (Def. 3.1.5). Then there is a 3-simplex

$$\left(\lambda_{X,Y,Y,d}, 1, (\theta_{X,Y}, 1, \delta_d)\right)$$

whose composition $\lambda_{X,Y,Y,d} \circ_1 (\theta_{X,Y} \circ_1 \delta_d)$ is the wiring diagram

![Wiring Diagram](attachment:diagram.png)

in $WD(Y)$ with one delay node.

**Example 5.1.7.** A 4-simplex is an iterated operadic composition in $WD$ of the form

$$\left(\left(\psi_1 \circ_{i} \psi_2 \circ_{j} \psi_3\right) \circ_{k} \psi_4, \left(\psi_1 \circ_{i} \left(\psi_2 \circ_{j} \psi_3\right) \circ_{k} \psi_4\right), \left(\psi_1 \circ_{i} \left(\psi_2 \circ_{j} \psi_3\right) \circ_{k} \psi_4\right)\right)$$

for some integers $i, j, k \geq 1$. For instance, continuing the previous example, suppose $Y^{\text{out}} = \{y\}$ and $Z$ is a box such that $Z^{\text{out}} = \{z, z'\}$ with $v(z) = v(z') = v(y)$ and that $Z/(z = z') = Y$. Suppose $\sigma_{Z, z, z'} \in WD(Y)$ is an out-split (Def. 3.1.7). Then there is a 4-simplex

$$\left(\sigma_{Z, z, z'}, 1, \left(\lambda_{X,Y,Y,d}, 1, (\theta_{X,Y}, 1, \delta_d)\right)\right)$$

whose composition

$$\sigma_{Z, z, z'} \circ_1 \left(\lambda_{X,Y,Y,d} \circ_1 (\theta_{X,Y} \circ_1 \delta_d)\right)$$

is the wiring diagram

![Wiring Diagram](attachment:diagram.png)

in $WD(Y)$ with one delay node.

In Section 5.2 we will show that any two presentations of the same wiring diagram are equivalent in a certain way. For this purpose, we will need a more structured kind of presentation.

**Motivation 5.1.8.** If we think of a simplex as a parenthesized word whose alphabets are generating wiring diagrams, then the stratified simplex in the next definition is a word where the same alphabets must occur in a consecutive string. For example, all the 1-loops must occur together as a string $(\lambda_1, \ldots, \lambda_n)$. Furthermore,
we can even insist that these strings for different types of generating wiring diagrams occur in a specific order, with name changes and 1-loops at the top and with 1-delay nodes and 2-cells at the bottom.

**Definition 5.1.9.** A \( \text{stratified simplex} \) in \( WD \) is a simplex in \( WD \) (Def. 5.1.2) of one of the following two forms, where Notation 5.1.3 is used:

1. \( (\omega, \epsilon) \), where:
   - \( \omega \) is a possibly empty string of 1-wasted wires (Def. 3.1.8);
   - \( \epsilon \) is the empty wiring diagram (Def. 3.1.1).

2. \( (\tau, \lambda, \omega, \sigma^*, \sigma^*, \theta, \delta) \), where:
   - \( \tau \) is a name change (Def. 3.1.3);
   - \( \lambda \) is a possibly empty string of 1-loops (Def. 3.1.5);
   - \( \omega \) is a possibly empty string of 1-wasted wires;
   - \( \sigma^* \) is a possibly empty string of in-splits (Def. 3.1.6);
   - \( \sigma^* \) is a possibly empty string of out-splits (Def. 3.1.7);
   - \( \theta \) is a possibly empty string of 2-cells (Def. 3.1.4);
   - \( \delta \) is a possibly empty string of 1-delay nodes (Def. 3.1.2).

We call these stratified simplices of type (1) and of type (2), respectively. If \( \Psi \) is a stratified simplex, then we call it a **stratified presentation** of the wiring diagram \( \Psi \).

**Remark 5.1.10.** Stratified simplices of type (1) and of type (2) are mutually exclusive. Indeed, the composition of a stratified simplex of type (1) has no input boxes and no delay nodes. On the other hand, the composition of a stratified simplex of type (2) either has at least one input box or at least one delay node or both.

Using the decompositions in the previous Chapter, we now observe that the generating wiring diagrams generate the operad \( WD \) of wiring diagrams in a highly structured way.

**Theorem 5.1.11.** Every wiring diagram has a stratified presentation (Def. 5.1.9).

**Proof.** Suppose \( \psi \in WD(Y) \) is a general wiring diagram as in Assumption 4.1.1 with input boxes \( X = (X_1, \ldots, X_N) \) and delay nodes \( D\psi = \{d_1, \ldots, d_r\} \). Recall Notation 3.3.1 for (iterated) \( \circ_1 \).

If \( N = r = 0 \), then \( \psi \) has a stratified presentation of type (1) by Lemma 4.1.3.

Next suppose \( N + r \geq 1 \). We use the decomposition \( \psi = \alpha \circ \varphi \) (4.1.7.1) and show that \( \psi \) has a stratified presentation of type (2) using the following observations.

1. If \( N + r = 1 \), then \( \varphi \) is either a colored unit, which can be ignored in a simplex by Lemma 2.3.6 or a 1-delay node by Lemma 4.1.8.
(2) If $N + r \geq 2$, then $\varphi$ has a stratified presentation $(\theta, \dot{\theta})$ consisting of 2-cells and 1-delay nodes by Lemma 4.1.10 and by the equivalence between $\gamma$ and the $\circ_i$-compositions (2.1.12.1).

(3) By definition $\alpha$ (4.1.6.1) has one input box and no delay nodes. There is a decomposition $\alpha = \pi_1 \circ \pi_2$ by Lemma 4.2.6. The outer wiring diagram $\pi_1$ is either a colored unit or has a stratified presentation $(\lambda)$ consisting of 1-loops by Lemma 4.2.7.

(4) Furthermore, by Lemma 4.3.5 there is a decomposition $\pi_2 = \beta_1 \circ \beta_2 \circ \beta_3$ in which:
   - $\beta_1$ is a colored unit or has a stratified presentation $(\omega)$ consisting of 1-wasted wires by Lemma 4.3.6
   - $\beta_2$ is a colored unit or has a stratified presentation $(\sigma^*)$ consisting of in-splits by Lemma 4.3.9
   - $\beta_3$ is a colored unit or has a stratified presentation $(\sigma^*)$ consisting of out-splits by Lemma 4.3.12

Using the decomposition

$$\psi = \pi_1 \circ \beta_1 \circ \beta_2 \circ \beta_3 \circ \varphi$$

together with Convention 4.2.4, we obtain the desired stratified presentation of type (2) for $\psi$ when $N + r \geq 1$. \hfill \square

5.2. Finite Presentation for Wiring Diagrams

The purpose of this section is to establish the second part of the finite presentation theorem for the operad $\text{WD}$. First we define precisely what it means for two presentations of the same wiring diagram to be related to each other. Recall the 28 elementary relations (Def. 3.3.30) and the definition of a colored operad (Def. 2.1.10). In what follows, we will regard each operad associativity or unity axiom as an equality. We remind the reader of Notation 5.1.3 regarding simplices in $\text{WD}$.

Motivation 5.2.1. Recall that a simplex is essentially a parenthesized word whose alphabets are generating wiring diagrams. In the next definition, we develop the precise concept through which one simplex presentation of a wiring diagram may be replaced by another. We only allow replacement of strings within a simplex corresponding to either one of the 28 elementary relations or an operad associativity/unity axiom. When such a replacement within a simplex is possible, we say that the two simplices are elementarily equivalent.

Definition 5.2.2. Suppose $\Psi$ is an $n$-simplex in $\text{WD}$ as in Def. 5.1.2

(1) A subsimplex of $\Psi$ is a simplex in $\text{WD}$ defined inductively as follows.
   - If $\Psi$ is a 1-simplex, then a subsimplex of $\Psi$ is $\Psi$ itself.
5.2. Finite Presentation for Wiring Diagrams

- Suppose \( n \geq 2 \) and \( \Psi = (\psi, i, \phi) \) for some \( i \geq 1 \), \( p \)-simplex \( \psi \), and \( q \)-simplex \( \phi \) with \( p + q = n \). Then a subsimplex of \( \Psi \) is
  - a subsimplex of \( \psi \),
  - a subsimplex of \( \phi \), or
  - \( \Psi \) itself.
If \( \Psi' \) is a subsimplex of \( \Psi \), then we write \( \Psi' \subseteq \Psi \).

(2) An elementary subsimplex \( \Psi' \) of \( \Psi \) is a subsimplex of one of two forms:
  (i) \( \Psi' \) is one side (either left or right) of a specified elementary relation (Def. 3.3.30).
  (ii) \( \Psi' \) is one side (either left or right) of a specified operad associativity or unity axiom, or (2.1.10.3), (2.1.10.4), (2.1.10.5), or (2.1.10.6)–involving only the generating wiring diagrams (Def. 3.3.9).

(3) Suppose \( \Phi \) is another simplex in WD. Then \( \Psi \) and \( \Phi \) are said to be equivalent if their compositions are equal; i.e., \( |\Psi| = |\Phi| \in WD \).

(4) Suppose:
  - \( \Psi' \subseteq \Psi \) is an elementary subsimplex corresponding to one side of \( R \), which is either an elementary relation or an operad associativity/unity axiom for the generating wiring diagrams.
  - \( \Psi'' \) is the simplex given by the other side of \( R \).
  - \( \Psi^1 \) is the simplex obtained from \( \Psi \) by replacing the subsimplex \( \Psi' \) by \( \Psi'' \).
We say that \( \Psi \) and \( \Psi^1 \) are elementarily equivalent. Note that elementarily equivalent simplices are also equivalent.

(5) If \( \Psi \) and \( \Phi \) are elementarily equivalent, we write \( \Psi \sim \Phi \) and call this an elementary equivalence.

(6) Suppose \( \Psi_0, \ldots, \Psi_r \) are simplices for some \( r \geq 1 \) and that there exist elementary equivalences
\[
\Psi_0 \sim \Psi_1 \sim \cdots \sim \Psi_r.
\]
Then we say that \( \Psi_0 \) and \( \Psi_r \) are connected by a finite sequence of elementary equivalences. Note that in this case \( \Psi_0 \) and \( \Psi_r \) are equivalent.

**Remark 5.2.3.** In the definition of an elementary subsimplex and an elementary equivalence, we did not use the operad equivariance axiom (2.1.10.7). The reason is that the associativity and commutativity properties of 2-cells–namely, the elementary relations (3.3.9.1) and (3.3.10.1)–are enough to guarantee the operad equivariance axiom involving only the generating wiring diagrams.

**Example 5.2.4.** In a 3-simplex \((\psi_1 \circ \psi_2) \circ \psi_3\), both
\[
(\psi_1, \psi_2) = \psi_1 \circ \psi_2 \quad \text{and} \quad (\psi_1, \psi_2, \psi_3) = (\psi_1 \circ \psi_2) \circ \psi_3
\]
are subsimplices. However, \((\psi_2, \psi_3)\) is not a subsimplex.
Example 5.2.5. A given wiring diagram may have many different equivalent presentations. For example, suppose $X \in \text{Box}_S$. Then the 1-simplex consisting of the $X$-colored unit $1_X$ (2.3.2.1) is elementarily equivalent to:

1. the 2-simplex $\theta_{X,\emptyset} \circ 2 \in \text{Box}_S$ by (3.3.8.1);
2. the 3-simplex $(\lambda_Z, x) \circ (\omega_{Z, X})$ by (3.3.2.1);
3. the 2-simplex $\sigma_{T, t_1, t_2} \circ (\omega_{Y, y})$ by (3.3.25.1).

Any two of these three simplices are connected by a finite sequence of elementary equivalences. Note that elementarily equivalent simplices may have different lengths.

Example 5.2.6. Suppose:

- $\theta_{X, Y} \in \text{WD}(X_{X, Y})$ is a 2-cell (Def. 3.1.4).
- $\theta_{V, W} \in \text{WD}(V_{V, W})$ is a 2-cell with $X = V \sqcup W \in \text{Box}_S$.
- $\sigma_{T, t_1, t_2} \in \text{WD}(T)$ is an in-split (Def. 3.1.6).

Then the 3-simplices

$$\left(\theta_{X, Y} \circ_1 \theta_{V, W}\right) \circ_3 \sigma_{T, t_1, t_2} \quad \text{and} \quad \left(\theta_{X, Y} \circ_2 \sigma_{T, t_1, t_2}\right) \circ_1 \theta_{V, W}$$

are elementarily equivalent by the horizontal associativity axiom (2.1.10.3). This elementary equivalence expresses the fact that the wiring diagram

![Wiring Diagram](image)

can be created from $\theta_{X, Y}$ by substituting in the two gray boxes in either order.

Convention 5.2.7. In what follows, to simplify the presentation, elementary equivalences corresponding to an operad associativity/unity axiom—(2.1.10.3), (2.1.10.4), (2.1.10.5), or (2.1.10.6)—for the generating wiring diagrams will often be applied tacitly wherever necessary. For instance, an elementary equivalence given by replacing one of the 3-simplices in Example 5.2.6 by the other one will often not be mentioned explicitly.

Our next goal is to show that any two equivalent simplices are connected by a finite sequence of elementary equivalences. In other words, with respect to the
generating wiring diagrams, the 28 elementary relations and the operad associativity/unity axioms—\((\text{2.1.10.3}, \text{2.1.10.4}, \text{2.1.10.5}),\) and \((\text{2.1.10.6})\)—for the generating wiring diagrams generate all the relations in WD. During the first reading, the reader may wish to skip the proofs of the following three Lemmas.

The first step is to show that every simplex is connected to a stratified simplex in the following sense.

**Lemma 5.2.8.** Every simplex is either a stratified simplex or is connected to an equivalent stratified simplex by a finite sequence of elementary equivalences (Def. 5.2.2).

**Proof.** Using Notation [5.1.3] suppose \(\Psi = (\psi_1, \ldots, \psi_n)\) is a simplex with composition \(|\Psi| = \psi \in \text{WD}(\_\_\_)\) as in Assumption 4.1.1. So \(\psi\) has input boxes \(X = (X_1, \ldots, X_N)\) and delay nodes \(\text{DN}_\psi = \{d_1, \ldots, d_r\}\). Suppose \(\Psi\) is not a stratified simplex. We will show that \(\Psi\) is connected to an equivalent stratified simplex by a finite sequence of elementary equivalences.

Using the five elementary relations (3.3.3.1)–(3.3.7.1), first we move all the name changes (Def. 3.1.3) in \(\Psi\), if there are any, to the left. Then we use the elementary relation (3.3.2.1) repeatedly to compose them down into one name change. Therefore, after a finite sequence of elementary equivalences, we may assume that there is at most one name change in \(\Psi\), which is the left-most entry. If there are further elementary equivalences later that create name changes, we will perform the same procedure without explicitly mentioning it.

The empty wiring diagram \(\epsilon \in \text{WD}(\_\_)\) (Def. 3.1.1) and the 1-delay nodes \(\delta_d \in \text{WD}(\_\_)\) (Def. 3.1.2) have no input boxes, so no operadic composition of the forms \(\epsilon \circ_i \) or \(\delta_d \circ_i \) can be defined. Therefore, after a finite sequence of elementary equivalences corresponding to the horizontal associativity axiom (2.1.10.3), we may assume that \(\Psi\) has the form

\[
(\tau, \Psi^1, \underline{\epsilon}, \underline{\delta})
\]

in which:

- \(\tau\) is a name change;
- all the 1-delay nodes \(\underline{\delta}\) are at the right-most entries;
- all the empty wiring diagrams \(\underline{\epsilon}\) are just to their left;
- \(\Psi^1\) is either empty or is a subsimplex involving 2-cells (Def. 3.1.4), 1-loops (Def. 3.1.5), in-splits (Def. 3.1.6), out-splits (Def. 3.1.7), and 1-wasted wires (Def. 3.1.8).

Next we use the elementary relations (3.3.11.1)–(3.3.14.1) to move all the 2-cells in \(\Psi\) to just the left of \(\underline{\epsilon}\). Then we use the elementary relations (3.3.16.1)–(3.3.18.1) to move all the remaining 1-loops to just the right of the name change \(\tau\). After that, we use the elementary relations (3.3.24.1) and (3.3.28.1) to move all the 1-wasted
wires to just the right of the 1-loops. Then we use the elementary relation \((3.3.23.1)\) to move all the in-splits to just the right of the 1-wasted wires. So after a finite sequence of elementary equivalences, we may assume that the simplex \(\Psi\) has the form

\[
\left( \tau, \lambda, \omega, \gamma^*, \theta, \epsilon, \delta \right).
\]  
(5.2.8.1)

If the string \(\epsilon\) of empty wiring diagrams is empty, then we are done because this is now a stratified simplex of type (2).

So suppose the string \(\epsilon\) in (5.2.8.1) is non-empty. Using finitely many elementary equivalences corresponding to the elementary relations \((3.3.8.1)\)–\((3.3.10.1)\), we may cancel all the unnecessary empty wiring diagrams in (5.2.8.1). If there are no empty wiring diagrams left after the cancellation, then we have a stratified simplex of type (2).

Suppose that, after the cancellation in the previous paragraph, the resulting string \(\epsilon\) is still non-empty. Then it must contain a single empty wiring diagram \(\epsilon\), and there are no 2-cells \(\theta\) and no 1-delay nodes \(\delta\) in the resulting simplex \(\Psi\). Since the output box of \(\epsilon\) is the empty box, the current simplex \(\Psi\) cannot have any 1-loops \(\lambda\), in-splits \(\sigma^*\), or out-splits \(\sigma^*\). Therefore, in this case the simplex (5.2.8.1) has the form

\[
\left( \tau, \omega, \epsilon \right).
\]  
(5.2.8.2)

There are now two cases. First suppose the string \(\omega\) in (5.2.8.2) is empty. Since the output box of \(\epsilon\) is the empty box, in the simplex \((\tau, \epsilon)\) the name change \(\tau\) must be the colored unit of the empty box. So by the left unity axiom \((2.1.10.5)\), the simplex \((1_{\emptyset}, \epsilon)\) is elementarily equivalent to the simplex \((\epsilon)\), which is a stratified simplex of type (1).

Next suppose the string \(\omega\) in (5.2.8.2) is non-empty. Using finitely many elementary equivalences corresponding to the elementary relation \((3.3.7.1)\), the simplex (5.2.8.2) is connected to a simplex of the form

\[
(\omega, \tau, \epsilon)
\]  
(5.2.8.3)

with \(\tau \circ \epsilon\) as one of the operadic compositions. As in the previous case, the composition \(\tau \circ \epsilon\) forces \(\tau\) to be the colored unit of the empty box. So the simplex \((\omega, 1_{\emptyset}, \epsilon)\) in (5.2.8.3) is elementarily equivalent to the simplex \((\omega, \epsilon)\), which is a stratified simplex of type (1). \(\square\)

The next step is to show that equivalent stratified simplices are connected. We begin with stratified simplices of type (1).

**Lemma 5.2.9.** Any two equivalent stratified simplices of type (1) are either equal or are connected by a finite sequence of elementary equivalences (Def. 5.2.2).
Proof. Suppose \( \Psi^1 = (\omega^1, \epsilon) \) and \( \Psi^2 = (\omega^2, \epsilon) \) are equivalent stratified simplices of type (1) with common composition \( \psi \). Then \( \psi \) has no input boxes and no delay nodes, and its output box contains only external wasted wires as in Lemma 4.1.3. Each 1-wasted wire in each \( \Psi^i \) creates one external wasted wire in \( \psi \). So the 1-wasted wire strings \( \omega^1 \) and \( \omega^2 \) have the same length. It follows that the simplices \( \Psi^1 \) and \( \Psi^2 \) are connected by a finite sequence of elementary equivalences corresponding to the elementary relation \( (3.3.29.1) \) and the vertical associativity axiom \( (2.1.10.4) \). □

Lemma 5.2.10. Any two equivalent stratified simplices of type (2) are either equal or are connected by a finite sequence of elementary equivalences (Def. 5.2.2).

Proof. The proof consists of a series of reductions. Suppose \( \Psi^1 \) and \( \Psi^2 \) are distinct but equivalent stratified simplices of type (2) with common composition \( \psi \in WD_{(\lambda, \Sigma)} \). Using elementary equivalences corresponding to

- the operad unity axioms \( (2.1.10.5) \) and \( (2.1.10.6) \),
- the elementary relations \( (3.3.8.1), (3.3.20.1), \) and \( (3.3.25.1) \) regarding colored units, and
- other elementary relations that move the generating wiring diagrams around the simplices,

we may assume that there are no unnecessary generating wiring diagrams in these stratified simplices. Here unnecessary refers to either a colored unit or generating wiring diagrams whose (iterated) operadic composition is a colored unit.

The name change \( \tau^1 \) in \( \Psi^1 \) has output box \( Y \) and input box uniquely determined by \( \psi \), and the same is true for the name change \( \tau^2 \) in \( \Psi^2 \). It follows that \( \tau^1 \) is equal to \( \tau^2 \). So we may assume that there are no name changes in the two stratified simplices \( \Psi^i \).

The string of delay nodes \( \delta^i \) in each simplex \( \Psi^i \) represents the set of delay nodes in \( \psi \). Therefore, the two \( \Psi^i \) without their strings of delay nodes are also equivalent. Moreover, if these simplices without delay nodes are connected by a finite sequence of elementary equivalences, then so are the two \( \Psi^i \) themselves by the horizontal associativity axiom \( (2.1.10.3) \). So we may assume that the wiring diagram \( \psi \) and the two simplices \( \Psi^i \) have no delay nodes. At this stage, each stratified simplex \( \Psi^i \) has the form

\[
(\lambda^i, \omega^i, \sigma^i, \sigma^*i, \theta^i).
\]

The composition of the string of 2-cells \( |\theta^i| \) in each simplex \( \Psi^i \) has the same input boxes as \( \psi \). So using finitely many elementary equivalences corresponding to the elementary relations \( (3.3.9.1) \) and \( (3.3.10.1) \), we may assume that the wiring diagram \( \psi \) has only one input box and that the simplices \( \Psi^i \) have no 2-cells. At this
stage, each stratified simplex $\Psi^i$ has the form

$$\left( \lambda^i, \omega^i, \sigma^i, \sigma^* \right).$$

Observe that for each $i \in \{1, 2\}$, the string of 1-wasted wires $\omega^i$ in the simplex $\Psi^i$ corresponds to precisely the set $\psi^{\omega^i} \cup \psi^{\sigma^i}$ of external and internal wasted wires in the wiring diagram $\psi$ (Def. 2.2.13). Here an internal wasted wire in $\psi$ is created by applying a 1-loop to a 1-wasted wire as in (3.2.3.1). Therefore, using finitely many elementary equivalences corresponding to the elementary relations (3.3.15.1) and (3.3.18.1), we may assume that the wiring diagram $\psi$ and the two simplices $\Psi^i$ have no 1-wasted wires. At this stage, each stratified simplex $\Psi^i$ has the form

$$\left( \lambda^i, \sigma^i, \sigma^* \right).$$

Using finitely many elementary equivalences corresponding to the elementary relation (3.3.19.1), we may assume that each loop element in the wiring diagram $\psi$ (Def. 4.2.1) corresponds to precisely one 1-loop $\lambda$ in each simplex $\Psi^i$. At this stage, the 1-loops in each simplex $\Psi^i$ are in bijection with the loop elements in $\psi$. Moreover, the two stratified subsimplices $\left( \sigma^1, \sigma^{*1} \right) \subseteq \Psi^1$ and $\left( \sigma^2, \sigma^{*2} \right) \subseteq \Psi^2$ are equivalent. Therefore, using finitely many elementary equivalences corresponding to the elementary relation (3.3.15.1), we may assume that the wiring diagram $\psi$ has no loop elements and that the simplices $\Psi^i$ have no 1-loops. So each stratified simplex $\Psi^i$ now has the form

$$\left( \sigma^i, \sigma^* \right).$$

The two stratified subsimplices $\left( \sigma^i \right) \subseteq \Psi^i$ of in-splits for $i \in \{1, 2\}$ are also equivalent. They are connected by a finite sequence of elementary equivalences corresponding to the elementary relations (3.3.21.1) and (3.3.22.1). Likewise, the stratified subsimplices $\left( \sigma^* \right) \subseteq \Psi^i$ of out-splits for $i \in \{1, 2\}$ are connected by a finite sequence of elementary equivalences corresponding to the elementary relations (3.3.26.1) and (3.3.27.1). So the two simplices $\Psi^i$ are also connected by a finite sequence of elementary equivalences. \hfill \Box

We are now ready for the finite presentation theorem for wiring diagrams. It describes the wiring diagram operad $\operatorname{WD}$ (Theorem 2.3.11) in terms of finitely many generators and finitely many relations.

**Theorem 5.2.11.** Consider the operad $\operatorname{WD}$ of wiring diagrams.

1. Every wiring diagram can be obtained from finitely many generating wiring diagrams (Def. 3.1.9) via iterated operadic compositions (Def. 2.1.10).

2. Any two equivalent simplices are either equal or are connected by a finite sequence of elementary equivalences (Def. 5.2.2).
5.3. Finite Presentation for Normal Wiring Diagrams

Proof. The first statement is a special case of Theorem 5.1.11. The second statement is a combination of Remark 5.1.10, Lemma 5.2.8 twice, Lemma 5.2.9, and Lemma 5.2.10. □

5.3. Finite Presentation for Normal Wiring Diagrams

In this section, we establish a finite presentation theorem for the operad of wiring diagrams without delay nodes. Such wiring diagrams are used in [Spi15, Spi15b] to study mode-dependent networks and dynamical systems. Recall Def. 2.2.13, Def. 2.2.15, and Convention 2.2.16 regarding wiring diagrams.

Definition 5.3.1. Fix a class $S$.

(1) A wiring diagram is said to be normal if its set of delay nodes is empty.

(2) The collection of normal wiring diagrams is denoted by $\text{WD}^\bullet$. If we want to emphasize $S$, then we will write $\text{WD}^S$. 

Example 5.3.2. Among the 8 generating wiring diagrams (section 3.1):

(1) A 1-delay node $\delta_d$ (Def. 3.1.2) is not normal.

(2) The empty wiring diagram $\epsilon$ (Def. 3.1.1), a name change $\tau_{X,Y}$ (Def. 3.1.3), a 2-cell $\theta_{X,Y}$ (Def. 3.1.4), a 1-loop $\lambda_{X,x}$ (Def. 3.1.5), an in-split $\sigma_{X,x_1,x_2}$ (Def. 3.1.6), an out-split $\sigma^{Y,y_1,y_2}$ (Def. 3.1.7), and a 1-wasted wire $\omega_{Y,y}$ (Def. 3.1.8) are normal.

In particular, there is a proper inclusion $\text{WD}^\bullet \subsetneq \text{WD}$. Furthermore, the 1-internal wasted wire $\omega^{X,x}$ (Def. 3.2.1) is normal.

Example 5.3.3. All the wiring diagrams that appear in the 28 elementary relations (section 3.3) are normal.

Example 5.3.4. Among the wiring diagrams in Chapter 4:

(1) $\varphi$ (4.1.5.1) is not normal, unless $r = 0$.

(2) $\psi$ in (4.1.3.1), $\alpha$ (4.1.6.1), $\pi_1$ (4.2.5.1), $\pi_2$ (4.2.5.2), $\beta_1$ (4.3.3.1), $\beta_2$ (4.3.3.2), and $\beta_3$ (4.3.3.3) are normal.

Proposition 5.3.5. With respect to

- the equivariant structure in Def. 2.3.1
- the colored units in Def. 2.3.2
- the $\circ_i$-compositions in Def. 2.3.4

$\text{WD}^\bullet$ is a Box$^S$-colored operad, called the operad of normal wiring diagrams.
Proof. We can reuse the proof of Theorem 2.3.11—that WD is a Box-colored operad—as long as we know that the relevant structure is well-defined in WD•.

The collection WD• is closed under the equivariant structure map (2.3.1.1). Furthermore, each colored unit 1γ (2.3.2.1) is in WD•.

Suppose both ϕ and ψ are normal wiring diagrams such that ϕ ○ iψ ∈ WD is defined. Then ϕ ○ iψ is also normal because

\[ \text{DN}_{ϕ ○ iψ} = \text{DN}_ϕ \cup \text{DN}_ψ = \emptyset. \]

Therefore, Lemmas 2.3.6, 2.3.8, and 2.3.10 all apply to WD• to show that it is an operad.

Our next objective is to obtain a version of the finite presentation theorem for WD•. For this purpose, we will use the following definitions.

Definition 5.3.6. Consider the operad WD• of normal wiring diagrams.

1. A normal generating wiring diagram is a generating wiring diagram (Def. 3.1.9) except for 1-delay nodes δd (Def. 3.1.2).
2. A normal simplex is defined as in Def. 5.1.2 using normal generating wiring diagrams and WD• in place of WD.
3. A normal stratified simplex and a normal stratified presentation are defined as in Def. 5.1.9 with WD• in place of WD, except that a normal stratified simplex of type (2) has the form \( [τ, Λ, ω, σ, σ^+, θ] \).
4. All of Def. 5.2.2 is repeated with normal generating wiring diagrams and WD• in place of WD.

The following result is the finite presentation theorem for normal wiring diagrams.

Theorem 5.3.7. Consider the operad WD• of normal wiring diagrams.

1. Every normal wiring diagram has a normal stratified presentation.
2. Every normal wiring diagram can be obtained from finitely many normal generating wiring diagrams via iterated operadic compositions (Def. 2.1.10).
3. Any two equivalent normal simplices are connected by a finite sequence of elementary equivalences (Def. 5.2.2).

Proof. For statement (1), we reuse the proof of Theorem 5.1.11 while assuming r = 0. Statement (2) is a special case of statement (1).

For statement (3) we reuse the proof of Theorem 5.2.11(2). In other words, we simply reuse the proofs of Lemma 5.2.8, Lemma 5.2.9, and Lemma 5.2.10 while...
5.4. Finite Presentation for Strict Wiring Diagrams

In this section, we establish a finite presentation theorem for the operad of strict wiring diagrams. Such wiring diagrams are used in [VSL15] to study open dynamical systems.

**Definition 5.4.1.** Fix a class $S$.

1. A wiring diagram (Def. 2.2.15) is said to be *strict* if
   - it is normal (Def. 5.3.1) and
   - its supplier assignment is a bijection.

2. The collection of strict wiring diagrams is denoted by $\text{WD}_0$. If we want to emphasize $S$, then we will write $\text{WD}_0^S$.

**Remark 5.4.2.** What we call a strict wiring diagram is simply called a wiring diagram in [VSL15] (Def. 3.5). In [VSL15] (Remark 2.7) $S$ is a set of representatives of isomorphism classes of second-countable smooth manifolds. The non-instantaneity requirement (2.2.13.2) in this case is called the no passing wires requirement in [VSL15]. As noted in [VSL15] (Remark 3.6), strictness implies the non-existence of external wasted wires, internal wasted wires (Def. 2.2.13), and split wires, i.e., multiple (at least two) demand wires having the same supply wire. So strict wiring diagrams are much simpler than a general wiring diagram.

**Example 5.4.3.** Among the 8 generating wiring diagrams (section 3.1):

1. A 1-delay node $\delta_d$ (Def. 3.1.2) is not normal (Def. 5.3.1), hence also not strict.

2. The empty wiring diagram $\epsilon$ (Def. 3.1.1), a name change $\tau_{X,Y}$ (Def. 3.1.3), a 2-cell $\theta_{X,Y}$ (Def. 3.1.4), and a 1-loop $\lambda_{X,x}$ (Def. 3.1.5) are strict.

3. An in-split $\sigma_{X,x_1,x_2}$ (Def. 3.1.6), an out-split $\sigma^{Y,y_1,y_2}$ (Def. 3.1.7), and a 1-wasted wire $\omega_{Y,y}$ (Def. 3.1.8) are normal but not strict.

In particular, there are proper inclusions $\text{WD}_0 \subsetneq \text{WD}_* \subsetneq \text{WD}$. Furthermore, the 1-internal wasted wire $\omega_{X,x}$ (Def. 3.2.1) is normal but not strict.
Example 5.4.4. Among the wiring diagrams that appear in the 28 elementary relations (section 3.3):

1. (3.3.2.1), (3.3.3.1), (3.3.4.1), (3.3.8.1), (3.3.9.1), (3.3.10.1), (3.3.11.1), (3.3.15.1), (3.3.20.1), and (3.3.25.1) are strict wiring diagrams.

2. The other 18 are normal but not strict.

3. Only (3.3.2.1), (3.3.3.1), (3.3.4.1), (3.3.8.1), (3.3.9.1), (3.3.10.1), (3.3.11.1), and (3.3.15.1) involve only strict wiring diagrams on both sides. Indeed, both (3.3.20.1) and (3.3.25.1) involve a 1-wasted wire, which is not strict.

Example 5.4.5. Among the wiring diagrams in Chapter 4:

1. $\psi$ in (4.1.3.1) is normal but not strict.

2. $\alpha$, $\pi_2$, $\beta_1$, $\beta_2$, $\beta_3$ are normal but not strict in general.

3. $\pi_1$ (4.2.5.1) is a strict wiring diagram by Lemma 4.2.7.

Proposition 5.4.6. With respect to

- the equivariant structure in Def. 2.3.1,
- the colored units in Def. 2.3.2, and
- the $\circ_i$-compositions in Def. 2.3.4,

$WD_0$ is a $Box_S$-colored operad, called the operad of strict wiring diagrams.

Proof. The argument is essentially identical to the proof of Prop. 5.3.5 with a minor modification. Suppose both $\varphi$ and $\psi$ are strict wiring diagrams such that $\varphi \circ_i \psi \in WD$ is defined. Then $\varphi \circ_i \psi$ is also strict. Indeed, we already know that it is normal. Next, one can check directly from the definition of the supplier assignment $s_{\varphi \circ_i \psi}$ (2.3.4.1) that it is a bijection because, in all cases, it is defined as a composition of the bijections $s_\varphi$ and $s_\psi$. Therefore, Lemmas 2.3.6, 2.3.8, and 2.3.10 all apply to $WD_0$ to show that it is an operad.

Our next objective is to obtain a version of the finite presentation theorem for $WD_0$. For this purpose, we will use the following definitions.

Definition 5.4.7. Consider the operad $WD_0$ of strict wiring diagrams.

1. A strict generating wiring diagram means the empty wiring diagram $e$ (Def. 3.1.1), a name change $\tau_{X,Y}$ (Def. 3.1.3), a 2-cell $\theta_{X,Y}$ (Def. 3.1.4), or a 1-loop $\lambda_{X,x}$ (Def. 3.1.5).

2. A strict simplex is defined as in Def. 5.1.2 using strict generating wiring diagrams and $WD_0$ in place of $WD$. 

(3) A strict stratified simplex is a stratified simplex (Def. 5.1.9) of the form \((\varepsilon)\) or \((\tau, \lambda, \theta)\).

(4) If \(\Psi\) is a strict stratified simplex, then we call it a strict stratified presentation of the strict wiring diagram \(|\Psi|\).

(5) A strict elementary relation means one of the 8 elementary relations that involve only strict wiring diagrams on both sides, namely, \((3.3.2.1)\), \((3.3.3.1)\), \((3.3.4.1)\), \((3.3.8.1)\), \((3.3.9.1)\), \((3.3.10.1)\), \((3.3.11.1)\), and \((3.3.15.1)\). See Example 5.4.4.

(6) All of Def. 5.2.2 is repeated with \(\text{WD}_0\) in place of \(\text{WD}\) using strict generating wiring diagrams, strict simplices, and strict elementary relations. The resulting notions are called strict elementary equivalences, and so forth.

The following result is the finite presentation theorem for strict wiring diagrams.

**Theorem 5.4.8.** Consider the operad \(\text{WD}_0\) of strict wiring diagrams.

(1) Every strict wiring diagram has a strict stratified presentation.

(2) Every strict wiring diagram can be obtained from finitely many strict generating wiring diagrams via iterated operadic compositions (Def. 2.1.10).

(3) Any two equivalent strict simplices are connected by a finite sequence of strict elementary equivalences.

**Proof.** As in the proof of Theorem 5.3.7 for statement (1), we reuse the proof of Theorem 5.1.11 while assuming the wiring diagram \(\psi\) is strict. In this case, \(\psi\) is either the empty wiring diagram \(\varepsilon\) or has a decomposition (using \((4.1.7.1)\) and \((4.2.6.1)\))

\[
\psi = \pi_1 \circ \pi_2 \circ \varphi
\]

in which \(\pi_2\) is a name change. The desired strict stratified presentation follows from Convention 4.2.4 and the facts that:

- \(\pi_1\) is either a colored unit or has a stratified presentation \((\lambda)\) by Lemma 4.2.7.
- \(\varphi\) is either a colored unit or has a stratified presentation \((\theta)\) by Lemma 4.1.10.

Statement (2) is a special case of statement (1).

For statement (3) we use the strict versions of the proofs of Lemma 5.2.8, Lemma 5.2.9, and Lemma 5.2.10. The key observation is that, in this case, only strict generating wiring diagrams and strict elementary equivalences are used in these proofs. \(\square\)
5.5. Summary of Chapter 5

(1) A simplex in WD is a finite non-empty parenthesized word of generating wiring diagrams in which each pair of parentheses is equipped with an operadic \( o_i \)-composition.

(2) A stratified simplex in WD is a simplex of one of the following two forms.
   - \( (\omega, \varepsilon) \)
   - \( (\tau, \lambda, \omega, \sigma, \sigma^*, \theta, \delta) \)

(3) Every wiring diagram has a stratified presentation.

(4) Two simplices are elementarily equivalent if one can be obtained from the other by replacing a subsimplex \( \Psi' \) by an equivalent simplex \( \Psi'' \) such that \( |\Psi'| = |\Psi''| \) is either one of the twenty-eight elementary relations in WD or an operad associativity/unity axiom involving only the eight generating wiring diagrams.

(5) Any two simplex presentations of a given wiring diagram are connected by a finite sequence of elementary equivalences.

(6) A normal wiring diagram is a wiring diagram with no delay nodes.

(7) The operad WD\( _\bullet \) of normal wiring diagrams satisfies a finite presentation theorem involving the seven normal generating wiring diagrams and the twenty-eight elementary relations.

(8) A strict wiring diagram is a wiring diagram with no delay nodes and whose supplier assignment is a bijection.

(9) The operad WD\( _0 \) of strict wiring diagrams satisfies a finite presentation theorem involving the four strict generating wiring diagrams and the eight strict elementary relations.
Chapter 6

Finite Presentation for Algebras over Wiring Diagrams

The main purpose of this chapter is to provide finite presentations for algebras over the operads $\text{WD}$ (Theorem 2.3.11), $\text{WD}_\bullet$ (Prop. 5.3.5), and $\text{WD}_0$ (Prop. 5.4.6). The advantage of such a finite presentation is that sometimes the general structure map of an operad algebra can be a bit difficult to write down and understand. On the other hand, our generating structure maps and generating axioms are all fairly easy to write down and understand, as we will illustrate with examples in Sections 6.3, 6.5, and 6.7.

In Section 6.1 we recall the basics of algebras over an operad.

In Section 6.2 we first define a $\text{WD}$-algebra in terms of 8 generating structure maps and 28 generating axioms corresponding to the generating wiring diagrams (Def. 3.1.9) and the elementary relations (Def. 3.3.30), respectively. Then we observe that this finite presentation for a $\text{WD}$-algebra is in fact equivalent to the general definition of a $\text{WD}$-algebra (Theorem 6.2.2). This is an application of the finite presentation theorem for the operad $\text{WD}$ (Theorem 5.2.11).

In Section 6.3 we provide a finite presentation for the $\text{WD}$-algebra called the propagator algebra. In its original form, the propagator algebra was the main example in [RS13].

In Section 6.4 we observe that algebras over the operad $\text{WD}_\bullet$ of normal wiring diagrams have a similar finite presentation with 7 generating structure maps and
28 generating axioms. In Section 6.5 we provide a finite presentation for the \( \text{WD}_* \)-algebra called the algebra of discrete systems. In its original form, this algebra was one of the main examples in \cite{Spi15b}.

In Section 6.6 we observe that algebras over the operad \( \text{WD}_0 \) of strict wiring diagrams admit a finite presentation with 4 generating structure maps and 8 generating axioms. In Section 6.7 we provide a finite presentation for the \( \text{WD}_0 \)-algebra called the algebra of open dynamical systems. In its original form, this algebra was one of the main examples in \cite{VSL15}.

### 6.1. Operad Algebras

Let us first recall the definition of an algebra over an operad. The following definition can be found in \cite{Yau16} (Def. 13.2.3). In its original 1-colored topological form, it was first given in \cite{May72}. Fix a class \( S \) as before.

**Motivation 6.1.1.** One can think of an algebra over an operad as a generalization of a module over a ring. Given a ring \( R \), a left \( R \)-module \( M \) is equipped with structure maps \( r : M \rightarrow M \) for each element \( r \in R \) that satisfy some axioms. In particular, these structure maps are associative in the sense that

\[
(r_1 r_2)(m) = r_1(r_2 m)
\]

for \( r_1, r_2 \in R \) and \( m \in M \). Furthermore, the multiplicative unit \( 1_R \) of \( R \) acts as the identity map, so \( 1_R(m) = m \). For algebras over an operad, there is also an equivariance axiom because operads can model operations with multiple inputs.

**Definition 6.1.2.** Suppose \((O, \mathbb{1}, \gamma)\) is an \( S \)-colored operad as in Def. 2.1.3 An \( O \)-algebra is a pair \((A, \mu)\) consisting of the following data.

1. For each \( c \in S \), \( A \) is equipped with a class \( A_c \) called the \( c \)-colored entry of \( A \).
2. For each \( d \in S, \underline{c} = (c_1, \ldots, c_n) \in \text{Prof}(S) \), and \( \zeta \in O^{(\underline{c})}_d \), \( A \) is equipped with a structure map

\[
A_{\underline{c}} \overset{\text{def}}{=} \prod_{i=1}^{n} A_{c_i} \xrightarrow{\mu_i} A_d
\]

in which an empty product, for the case \( n = 0 \), means the one-point set \( \{\ast\} \).

This data is required to satisfy the following associativity, unity, and equivariance axioms.

**Associativity:** Suppose \( \underline{c} \in \text{Prof}(S) \times S \) is as above with \( n \geq 1 \), \( \zeta_0 \in O^{(\underline{c})}_d \), \( \zeta_i \in O^{(c_i)}_{\underline{c}} \) for each \( 1 \leq i \leq n \) with \( \underline{b} \in \text{Prof}(S) \), and \( \underline{b} = (b_1, \ldots, b_n) \) as in

\[
(\prod_{i=1}^{n} A_{c_i}) \xrightarrow{\mu} A_d
\]
6.1. Operad Algebras

\((2.1.3.2)\). Write \(\zeta = \gamma(\bar{\zeta}, \zeta_1, \ldots, \zeta_n) \in O(d)\). Then the diagram

\[
\begin{array}{ccc}
A_b & \xrightarrow{\mu_\zeta} & A_d \\
\downarrow & & \uparrow \mu_\zeta \\
\prod A_{b_i} & \xrightarrow{\Pi \mu_\zeta_i} & A_{c_1} \times \cdots \times A_{c_n} = A_c
\end{array}
\]

is commutative.

**Unity:** For each \(c \in S\), the structure map

\[
A_c \xrightarrow{\mu_1_c} A_c
\]

is the identity map, where \(1_c \in O(c)\) is the \(c\)-colored unit of \(O\).

**Equivariance:** Suppose \(\zeta \in O(d)\) as in \((6.1.2.1)\), \(\sigma \in \Sigma_n\), and \(\bar{\zeta}^\sigma \in O(d^\sigma)\) is the image of \(\zeta\) under the right action \((2.1.3.1)\). Then the diagram

\[
\begin{array}{ccc}
A_c & \xrightarrow{\sigma^{-1}} & A_{\bar{\zeta}^\sigma} \\
\downarrow \mu_i & & \uparrow \mu_\bar{\zeta}^\sigma \\
A_d & = & A_d
\end{array}
\]

is commutative. Here the top \(\sigma^{-1}\) permutes the factors of \(A_c\) from the left, and \(\bar{\zeta}^\sigma = (c_\sigma(1), \ldots, c_\sigma(n))\).

To simplify the notations, we will sometimes denote an \(O\)-algebra by just \(A\) and denote the structure map \(\mu_\zeta\) by \(\zeta\).

Just as operads can be equivalently expressed in terms of the \(\circ_i\)-compositions (Prop. 2.1.12), so can operad algebras.

**Definition 6.1.3.** Suppose \((O, 1, \circ)\) is an \(S\)-colored operad as in Def. 2.1.10. An \(O\)-algebra \((A, \mu)\) is defined exactly as in Def. 6.1.2 except that the associativity axiom \((6.1.2.2)\) is replaced by the following axiom.

**Associativity:** Suppose:

- \(d \in S\), \(\bar{\zeta} = (c_1, \ldots, c_n) \in \text{Prof}(S)\) with \(n \geq 1\), and \(1 \leq i \leq n\);
- \(b \in \text{Prof}(S)\) and \(\bar{\zeta} \circ_i b\) as in \((2.1.10.2)\);  
- \(\bar{\zeta}^i \in O(\bar{\zeta})\), \(\zeta \in O(\bar{\zeta})\), and \(\zeta \circ_i \bar{\zeta} \in O(\bar{\zeta}^i)\).

Then the diagram

\[
\begin{array}{ccc}
A_{\bar{\zeta} \circ_i b} & \xrightarrow{\mu_{\bar{\zeta} \circ_i b}} & A_d \\
\downarrow & & \uparrow \mu_{\zeta} \\
A(c_1, \ldots, c_{i-1}) \times A_{b_i} \times A(c_{i+1}, \ldots, c_n) & \xrightarrow{(\text{Id}, \mu_\zeta, \text{Id})} & A(c_1, \ldots, c_{i-1}) \times A_{c_i} \times A(c_{i+1}, \ldots, c_n) = A_{\bar{\zeta}}
\end{array}
\]

is commutative.
is commutative.

**Notation 6.1.4.** To simplify the notations, we will sometimes denote the structure map \( \mu_\zeta \) by \( \zeta \). We will also write the composition in the diagram (6.1.3.1) as \( \mu_\zeta \circ_i \mu_\xi \), called the \( \circ_i \)-composition of \( \mu_\zeta \) and \( \mu_\xi \). So this associativity axiom states that

\[ \mu_{\zeta \circ_i \xi} = \mu_\zeta \circ_i \mu_\xi. \]

In other words, the structure map of the \( \circ_i \)-composition \( \zeta \circ_i \xi \) is the \( \circ_i \)-composition of the structure maps corresponding to \( \zeta \) and \( \xi \).

Using the associativity and the unity axioms in Def. 2.1.3 and Def. 2.1.10, it is not hard to check that Def. 6.1.2 and Def. 6.1.3 are in fact equivalent. A proof of this equivalence can be found in [Yau16] (Prop. 16.7.8 and Exercises 10 and 11 in Chapter 16).

**Remark 6.1.5.** In Def. 6.1.2 and Def. 6.1.3, each entry of an operad algebra has no structure beyond being a class. We could have just as easily defined operad algebras in a symmetric monoidal category, which is in fact the setting in [Yau16] (Def. 13.2.3). One simply replaces the product with the symmetric monoidal product and the one-point set with the monoidal unit. However, to keep the presentation simple, we chose to define operad algebras whose entries are just classes. This is sufficient for the main examples in Sections 6.3, 6.5, and 6.7.

**Example 6.1.6 (Monoid Modules).** Suppose \((A, \mu, 1)\) is a monoid (Example 2.1.6). Recall that a left \(A\)-module is a set \(M\) equipped with a structure map \(a : M \rightarrow M\) for each \(a \in A\) that is associative and unital. Associativity means \((ab)m = a(bm)\) for \(a, b \in A\) and \(m \in M\). Unity means \(1m = m\) for \(m \in M\). If we regard \(A\) as a 1-colored operad \(O\) concentrated in arity 1 as in Example 2.1.6, then left \(A\)-modules yield \(O\)-algebras in the sense of Def. 6.1.2. The only slight difference between a left \(A\)-module and an \(O\)-algebra is that the former has an underlying set, while the latter is allowed to have an underlying class.

**Example 6.1.7 (Associative and Commutative Monoids).** This is a continuation of Example 2.1.7.

1. For the associative operad \(A_s\), an \(A_s\)-algebra with an underlying set is exactly a monoid.

2. For the commutative operad \(\text{Com}\), a \(\text{Com}\)-algebra with an underlying set is exactly a monoid whose multiplication is commutative.

**Example 6.1.8 (Traffic Spaces and Probability Spaces).** This is a continuation of Example 2.1.8 where we discussed the graph operation operad \(\text{GrOp}\). Here we consider \(\text{GrOp}\)-algebras in the category of complex vector spaces; see Remark 6.1.5. In particular, a \(\text{GrOp}\)-algebra \(A\) has an underlying complex vector space, and all the structure maps are linear maps, with tensor products playing the roles of products. The graph operation \(\bullet \in \text{GrOp}_0\), consisting of a single vertex and no edges, yields
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an element in \( A \), also denoted by \( \bullet \). For a general graph operation \( G \in \text{GrOp}_n \), the corresponding structure map \( A^\otimes n \to A \) is also denoted by \( G \). We will write \( \delta \in \text{GrOp}_1 \) for the graph operation consisting of a single vertex and a loop.

A traffic space \([\text{Mal16}]\) is a pair \((A, \varphi)\) in which \( A \) is a GrOp-algebra and \( \varphi : A \to C \) is a linear functional such that the following two conditions are satisfied.

**Unity and Diagonality:** \( \varphi(\bullet) = 1 \) and \( \varphi = \varphi \circ \delta \).

**Input-Independence:** For each graph operation \( G \in \text{GrOp}_n \), the graph operation \( \delta(G) \in \text{GrOp}_n \) is obtained from \( G \) by identifying its input and output. Suppose \( G' \) is a graph operation obtained from \( \delta(G) \) by choosing a different vertex as the input/output. Then \( \varphi \circ \delta(G) = \varphi \circ G' \).

For example, suppose \( G \in \text{GrOp}_4 \) is the graph operation on the left:

Then \( \delta(G) \) is the graph operation in the middle, and the graph operation on the right is an example of a \( G' \).

Traffic spaces play an important role in (non-commutative) probability theory. Indeed, a non-commutative probability space, also known as a quantum probability space, is a pair \((A, \varphi)\) in which:

1. \( A \) is a unital \( C \)-algebra.
2. \( \varphi : A \to C \) is a unital linear functional.

A *-probability space is a non-commutative probability space \((A, \varphi)\) in which:

1. \( A \) is equipped with an anti-linear involution * such that \((ab)^* = b^*a^* \) for all \( a, b \in A \).
2. \( \varphi \) satisfies the positivity condition that \( \varphi(a^*a) \geq 0 \) for all \( a \in A \).

Then a commutative *-probability space is an example of a traffic space, since the product of \( n \) elements in \( A \) is well-defined and is independent of the order of those elements. It is, furthermore, a *-algebra in the following sense. For each graph operation \( G \in \text{GrOp}_n \), its transpose \( G^t \) is the graph operation obtained from \( G \) by
for all $a_1, \ldots, a_n \in A$.

### 6.2. Algebras over the Operad of Wiring Diagrams

The purpose of this section is to provide a finite presentation for WD-algebras. We begin by defining a WD-algebra in terms of the generating wiring diagrams and the elementary relations. Immediately afterwards we will establish its equivalence with Def. 6.1.3 when $O = \text{WD}$. Recall that WD is a $\text{Box}_S$-colored operad (Theorem 2.3.11).

**Definition 6.2.1.** A WD-algebra $A$ consists of the following data. For each $X \in \text{Box}_S$, $A$ is equipped with a class $A_X$ called the $X$-colored entry of $A$. It is equipped with the following 8 generating structure maps corresponding to the generating wiring diagrams (Def. 3.1.9).

1. Corresponding to the empty wiring diagram $\varepsilon \in \text{WD}(\emptyset)$ (Def. 3.1.1), it has a structure map
   \[ \ast \xrightarrow{\varepsilon} A_{\emptyset} \]  
   i.e., a chosen element in $A_{\emptyset}$.

2. Corresponding to each 1-delay node $\delta_d \in \text{WD}(d)$ (Def. 3.1.2), it has a structure map
   \[ \ast \xrightarrow{\delta_d} A_{d} \]  
   i.e., a chosen element in $A_d$.

3. Corresponding to each name change $\tau_{X,Y} \in \text{WD}(\tau_{X,Y})$ (Def. 3.1.3), it has a structure map
   \[ A_X \xrightarrow{\tau_{X,Y}} A_Y \]  
   that is, furthermore, the identity map if $\tau_{X,X}$ is the colored unit $1_X$ (2.3.2.1).

4. Corresponding to each 2-cell $\theta_{X,Y} \in \text{WD}(\theta_{X,Y})$ (Def. 3.1.4), it has a structure map
   \[ A_X \times A_Y \xrightarrow{\theta_{X,Y}} A_{X\cup Y} \]  

5. Corresponding to each 1-loop $\lambda_{X,X} \in \text{WD}(\lambda_{X,X})$ (Def. 3.1.5), it has a structure map
   \[ A_X \xrightarrow{\lambda_{X,X}} A_{X\times X} \]
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(6) Corresponding to each in-split \( \sigma_{x_1, x_2} \in \text{WD}_X^{(1)} \) (Def. 3.1.6), it has a structure map
\[
A_X \xrightarrow{\sigma_{x_1, x_2}} A_Y.
\] (6.2.1.6)

(7) Corresponding to each out-split \( \sigma_{y_1, y_2} \in \text{WD}_X^{(1)} \) (Def. 3.1.7), it has a structure map
\[
A_X \xrightarrow{\sigma_{y_1, y_2}} A_Y.
\] (6.2.1.7)

(8) Corresponding to each 1-wasted wire \( \omega_{y} \in \text{WD}_X^{(1)} \) (Def. 3.1.8), it has a structure map
\[
A_X \xrightarrow{\omega_y} A_Y.
\] (6.2.1.8)

The following 28 diagrams, called the generating axioms, which correspond to the elementary relations (Def. 3.3.30), are required to be commutative.

(1) In the setting of (3.3.2.1), the diagram
\[
A_X \xrightarrow{\tau_{x,y}} A_Y \\
\xrightarrow{\tau_{x,z}} A_Z \\
\xrightarrow{\tau_{y,z}} A_Z
\] is commutative.

(2) In the setting of (3.3.3.1), the diagram
\[
A_X \times A_Y \xrightarrow{\theta_{x,y}} A_{X \cup Y} \\
\xrightarrow{\tau_{x,y}} A_{X \cup Y} \\
\xrightarrow{\tau_{y,y}'} A_{X' \cup Y'}
\] is commutative.

(3) In the setting of (3.3.4.1), the diagram
\[
A_X \xrightarrow{\lambda_{x,y}} A_{X \setminus x} \\
\xrightarrow{\tau_{x,y}} A_{X \setminus x} \\
\xrightarrow{\tau_{y,y}} A_{Y \setminus y}
\] is commutative.
(4) In the setting of (3.3.5.1), the diagram

\[
\begin{array}{c}
A_X \\ \sigma_{x_1, x_2} \\
\downarrow \tau_{X,Y} \\
A_Y \\ \sigma_{y_1, y_2}
\end{array}
\quad \begin{array}{c}
A_X' \\ \tau_{X',Y'} \\
\downarrow \tau_{X,Y} \\
A_Y' \\
\end{array}
\]

is commutative.

(5) In the setting of (3.3.6.1), the diagram

\[
\begin{array}{c}
A_X' \\ \sigma_{X_1, x_2} \\
\downarrow \tau_{X',Y'} \\
A_Y' \\ \sigma_{y_1, y_2}
\end{array}
\quad \begin{array}{c}
A_X \\ \tau_{X,Y} \\
\downarrow \tau_{X,Y} \\
A_Y \\
\end{array}
\]

is commutative.

(6) In the setting of (3.3.7.1), the diagram

\[
\begin{array}{c}
A_X' \\ \omega_{x,Y} \\
\downarrow \tau_{X',Y'} \\
A_Y' \\
\end{array}
\quad \begin{array}{c}
A_X \\ \tau_{X,Y} \\
\downarrow \omega_{y,Y} \\
A_Y \\
\end{array}
\]

is commutative.

(7) In the setting of (3.3.8.1), the diagram

\[
A_X \times \ast \quad \begin{array}{c}
\ast \\
\downarrow \theta_{X, \ast}
\end{array}
\quad \begin{array}{c}
A_X \times \ast \ast \\
\downarrow \theta_{X, \ast}
\end{array}
\]

is commutative.

(8) In the setting of (3.3.9.1), the diagram

\[
\begin{array}{c}
A_X \times A_Y \times A_Z \\ (\ast, \ast, \ast) \\
\downarrow \theta_{X,Y,Z} \\
A_X \times A_Y \times A_Z \\
\downarrow \theta_{X,Y,Z} \\
A_X \times A_Y \times A_Z \\
\downarrow \theta_{X,Y,Z}
\end{array}
\]

is commutative.
(9) In the setting of (3.3.10.1), the diagram

\[
\begin{array}{ccc}
A_Y \times A_X & \xrightarrow{\text{permute}} & A_X \times A_Y \\
\downarrow \theta_{Y,X} & & \downarrow \theta_{X,Y} \\
A_{Y \cup X} & \xrightarrow{\approx} & A_{X \cup Y}
\end{array}
\]  

(6.2.1.14)

is commutative.

(10) In the setting of (3.3.11.1), the diagram

\[
\begin{array}{ccc}
A_X \times A_Y & \xrightarrow{\theta_{X,Y}} & A_{X \cup Y} \\
(\lambda_{X,x,\text{Id}}) & & \downarrow \lambda_{X \cup Y,x} \\
A_{X \setminus x} \times A_Y & \xrightarrow{\theta_{X \setminus x,Y}} & A_{(X \cup Y) \setminus \{x\}}
\end{array}
\]  

(6.2.1.15)

is commutative.

(11) In the setting of (3.3.12.1), the diagram

\[
\begin{array}{ccc}
A_X \times A_Y & \xrightarrow{\theta_{X,Y}} & A_{X \cup Y} \\
(\sigma_{X,x_1,x_2,\text{Id}}) & & \downarrow \sigma_{X \cup Y,x_1,x_2} \\
A_{X' \setminus x} \times A_Y & \xrightarrow{\theta_{X' \setminus x,Y}} & A_{X' \cup Y}
\end{array}
\]  

is commutative.

(12) In the setting of (3.3.13.1), the diagram

\[
\begin{array}{ccc}
A_{X'} \times A_Y & \xrightarrow{\theta_{X',Y}} & A_{X' \cup Y} \\
(\rho_{X',x_1,x_2,\text{Id}}) & & \downarrow \rho_{X \cup Y,x_1,x_2} \\
A_X \times A_Y & \xrightarrow{\theta_{X,Y}} & A_{X \cup Y}
\end{array}
\]

is commutative.

(13) In the setting of (3.3.14.1), the diagram

\[
\begin{array}{ccc}
A_{X'} \times A_Y & \xrightarrow{\theta_{X',Y}} & A_{X' \cup Y} \\
(\omega_{X,x_0,\text{Id}}) & & \downarrow \omega_{X \cup Y,x_0} \\
A_X \times A_Y & \xrightarrow{\theta_{X,Y}} & A_{X \cup Y}
\end{array}
\]

is commutative.
(14) In the setting of (3.3.15.1), the diagram
\[
\begin{array}{ccc}
A_X & \xrightarrow{\lambda_{x,2}} & A_{X \setminus x^2} \\
\downarrow{\lambda_{x,1}} & & \downarrow{\lambda_{x,1}x^2, a^1} \\
A_{X \setminus x} & \xrightarrow{\lambda_{x,1}x^2} & A_{X \setminus x}
\end{array}
\]
(6.2.1.16)
is commutative.

(15) In the setting of (3.3.16.1), the diagram
\[
\begin{array}{ccc}
A_X & \xrightarrow{\lambda_{x,2}} & A_{X \setminus x} \\
\downarrow{\sigma_{x,y_{1,2}}} & & \downarrow{\sigma_{x,y_{1,2}}x, y^1} \\
A_{X'} & \xrightarrow{\lambda_{x,2}} & A_{X' \setminus x}
\end{array}
\]
is commutative.

(16) In the setting of (3.3.17.1), the diagram
\[
\begin{array}{ccc}
A_X & \xrightarrow{\sigma_{x,y_{1,2}}} & A_X \\
\downarrow{\lambda_{x,2}} & & \downarrow{\lambda_{x,2}} \\
A_{X' \setminus x} & \xrightarrow{\sigma_{x,y_{1,2}}} & A_{X' \setminus x}
\end{array}
\]
is commutative.

(17) In the setting of (3.3.18.1), the diagram
\[
\begin{array}{ccc}
A_X & \xrightarrow{\omega_{x,y_0}} & A_X \\
\downarrow{\lambda_{x,2}} & & \downarrow{\lambda_{x,2}} \\
A_{X' \setminus x} & \xrightarrow{\omega_{x,y,0}} & A_{X' \setminus x}
\end{array}
\]
is commutative.

(18) In the setting of (3.3.19.1), the diagram
\[
\begin{array}{ccc}
A_X & \xrightarrow{\sigma_{x,y_{1,2}}} & A_Y \xrightarrow{\lambda_{y,x}(1)} A_{Y \setminus x(1)} \\
\downarrow{\sigma_{x,y_{1,2}}} & & \downarrow{\lambda_{y,x}(1), x(2)} \\
A_{X'} & \xrightarrow{\lambda_{x,2}} & A_{X'}
\end{array}
\]
(6.2.1.17)
is commutative.
(19) In the setting of (3.3.20.1), the diagram
\[
\begin{align*}
A_X & \xrightarrow{\sigma_{Y,x_1,x_2}} A_Y \\
& \xrightarrow{\omega_{Z,x_1}} A_Z \\
& \xrightarrow{\lambda_{Z,z}} A_W \\
\end{align*}
\] is commutative.

(20) In the setting of (3.3.21.1), the diagram
\[
\begin{align*}
A_X & \xrightarrow{\sigma_{X,x_2,x_3}} A_{X_{23}} \\
& \xrightarrow{\phi_{X_{12},x_3}} A_{X_{12}} \\
& \xrightarrow{\phi_{X_{12},x_3}} A_Y \\
\end{align*}
\] is commutative.

(21) In the setting of (3.3.22.1), the diagram
\[
\begin{align*}
A_X & \xrightarrow{\sigma_{X,x_3,x_4}} A_{X_{34}} \\
& \xrightarrow{\phi_{X_{12},x_3}} A_{X_{12}} \\
& \xrightarrow{\phi_{X_{12},x_3}} A_Y \\
\end{align*}
\] is commutative.

(22) In the setting of (3.3.23.1), the diagram
\[
\begin{align*}
A_X & \xrightarrow{\sigma_{X,x_1,x_2}} A_Z \\
& \xrightarrow{\phi_{Z,x_1}} A_W \\
& \xrightarrow{\phi_{Z,x_1}} A_Y \\
\end{align*}
\] is commutative.

(23) In the setting of (3.3.24.1), the diagram
\[
\begin{align*}
A_X & \xrightarrow{\omega_{Z,z}} A_Z \\
& \xrightarrow{\lambda_{Z,z}} A_W \\
& \xrightarrow{\lambda_{Z,z}} A_Y \\
\end{align*}
\] is commutative.
(24) In the setting of (3.3.25.1), the diagram

$$AX \xrightarrow{\omega y} AY$$

$$\Downarrow \sigma_{y,x,y}$$

$$AX$$

is commutative.

(25) In the setting of (3.3.26.1), the diagram

$$AX \xrightarrow{\sigma_{12,y}^{-1},y_{23}} A_{Y_{12}}$$

$$\xrightarrow{\sigma_{y,y}^{2},y_{3}} A_{Y}$$

is commutative.

(26) In the setting of (3.3.27.1), the diagram

$$AX \xrightarrow{\sigma_{24,1},y_{2}} A_{Y_{24}}$$

$$\Downarrow \sigma_{y,y}^{4}$$

$$AX_{12} \xrightarrow{\sigma_{y,y}^{4}} A_{Y}$$

is commutative.

(27) In the setting of (3.3.28.1), the diagram

$$AX \xrightarrow{\omega_{W,1}} A_{W}$$

$$\Downarrow \omega_{y,y}^{2}$$

$$AZ \xrightarrow{\omega_{y,y}} A_{Y}$$

is commutative.

(28) In the setting of (3.3.29.1), the diagram

$$AX \xrightarrow{\omega_{2y_{1},y_{2}}} A_{Y_{1}}$$

$$\Downarrow \omega_{y_{1},y_{2}}$$

$$A_{Y_{1}} \xrightarrow{\omega_{y_{1},y}} A_{Y}$$

is commutative.

This finishes the definition of a WD-algebra.

At this moment we have two definitions of a WD-algebra.
6.2. Algebras over the Operad of Wiring Diagrams

(1) On the one hand, in Def. 6.1.3 with \( O = WD \), a \( WD \)-algebra has a structure map \( \mu_\zeta \) \((6.1.2.1)\) for each wiring diagram \( \zeta \). This structure map satisfies the associativity axiom \((6.1.3.1)\) for a general operadic composition in \( WD \), together with the unity and the equivariance axioms in Def. 6.1.2.

(2) On the other hand, in Def. 6.2.1 a \( WD \)-algebra has 8 generating structure maps and satisfies 28 generating axioms.

We now observe that these two definitions are equivalent, so \( WD \)-algebras indeed have a finite presentation as in Def. 6.2.1.

**Theorem 6.2.2.** For the operad of wiring diagrams \( WD \) (Theorem 2.3.11), Def. 6.1.3 with \( O = WD \) and Def. 6.2.1 of a \( WD \)-algebra are equivalent.

**Proof.** First suppose \((A, \mu)\) is a \( WD \)-algebra in the sense of Def. 6.1.3. To see that it is also a \( WD \)-algebra in the sense of Def. 6.2.1 first note that the structure map \( \mu_\zeta \) \((6.1.2.1)\) gives the eight generating structure maps \((6.2.1.1)-(6.2.1.8)\). Moreover, the generating structure map \( \mu_{1_X} \) \((6.2.1.3)\) is the identity map by the unity axiom \((6.1.2.3)\).

The generating axiom \((6.2.1.14)\) is a special case of the equivariance diagram \((6.1.2.4)\), so it is commutative. Each of the other 27 generating axioms corresponds to an elementary relation that describes two different ways to construct the same wiring diagram as an iterated operadic composition of generating wiring diagrams. Each such generating axiom asserts that the two corresponding compositions of generating structure maps—defined using the composition in the diagram \((6.1.3.1)\)—are equal. The associativity axiom \((6.1.3.1)\) of \((A, \mu)\) applied twice guarantees that two such compositions are indeed equal.

Conversely, suppose \( A \) is a \( WD \)-algebra in the sense of Def. 6.2.1, so it has eight generating structure maps that satisfy 28 generating axioms. We must show that it is a \( WD \)-algebra in the sense of Def. 6.1.3. For a wiring diagram \( \psi \in WD \) with a presentation \( \Psi \) (Def. 5.1.2), we define its structure map \( \mu_\psi \) \((6.2.1.1)\) inductively as follows.

(1) If \( \Psi \) is a 1-simplex, then \( \Psi = (\psi) \), and \( \psi \) is a generating wiring diagram by the definition of a simplex. In this case, we define \( \mu_\psi \) as the corresponding generating structure map \((6.2.1.1)-(6.2.1.8)\) of \( A \).

(2) Inductively, suppose \( \Psi \) is an \( n \)-simplex for some \( n \geq 2 \), so \( \Psi = (\Phi, i, \Theta) \) for some \( i \geq 1 \), \( p \)-simplex \( \Phi \), and \( q \)-simplex \( \Theta \) with \( p + q = n \). Since \( 1 \leq p, q < n \), by the induction hypothesis, the structure maps \( \mu_{|\Phi|} \) and \( \mu_{|\Theta|} \) are already defined. Then we define the structure map

\[
\mu_\psi = \mu_{|\Phi|} \circ \mu_{|\Theta|}
\]

as in Notation 6.1.4.
By Theorem 5.1.11 every wiring diagram has a stratified presentation, hence a presentation. To see that the structure map \( \mu_\psi \) as above is well-defined, we need to show that the map \( \mu_\psi \) is independent of the choice of a presentation \( \Psi \). Any two presentations of a wiring diagram are by definition equivalent simplices. By Theorem 5.2.11(2) (= the relations part of the finite presentation theorem for WD), any two equivalent simplices are either equal or are connected by a finite sequence of elementary equivalences. Therefore, it suffices to show that every elementary equivalence in WD yields a commutative diagram involving the generating structure maps of \( A \), where \( \circ_i \) is interpreted as in Notation 6.1.4. Recall from Def. 5.2.2 that an elementary equivalence comes from either an elementary relation or an operad associativity/unity axiom for the generating wiring diagrams.

It follows from a direct inspection that the operad associativity and unity axioms—(2.1.10.3), (2.1.10.4), (2.1.10.5), and (2.1.10.6)—for the generating wiring diagrams yield commutative diagrams involving the generating structure maps of \( A \). In fact, the diagrams involving the horizontal and the vertical associativity axioms (2.1.10.3) and (2.1.10.4) are commutative because composition of functions is associative. The diagrams for the two unity axioms (2.1.10.5) and (2.1.10.6) are commutative because the generating structure map for a colored unit (6.2.1.3) is required to be the identity map.

By definition each of the 28 generating axioms of \( A \) corresponds to an elementary relation (Def. 3.3.30) and is a commutative diagram. Therefore, the structure map \( \mu_\psi \) for each wiring diagram \( \psi \) is well-defined.

It remains to check that the structure map \( \mu \) satisfies the required unity, equivariance, and associativity axioms. The unity axiom (6.1.2.3) holds because it is part of the assumption on the generating structure map corresponding to a name change (6.2.1.3).

The associativity axiom (6.1.3.1) holds because the structure map \( \mu_\psi \) is defined above (6.2.2.1) by requiring that the diagram (6.1.3.1) be commutative.

For the equivariance axiom (6.1.2.4), first note that it is enough to check it when the wiring diagram in questioned is an iterated operadic composition of 2-cells. This is because 2-cells are the only binary generating wiring diagrams (Remark 3.1.10). All other generating wiring diagrams are either 0-ary or unary, for which equivariance is trivial.

So now suppose \( \zeta \) in the equivariance axiom (6.1.2.4) is an iterated operadic composition of 2-cells. If \( \zeta \) is a 2-cell and the permutation \( \sigma \) is the transposition \( (12) \in \Sigma_2 \), then the equivariance axiom (6.1.2.4) is true by the generating axiom (6.2.1.14). The general case now follows from this special case using:

- the generating axiom (6.2.1.13) corresponding to the associativity property of 2-cells (3.3.9.1);
6.3. Finite Presentation for the Propagator Algebra

As an illustration of Theorem 6.2.2, in this section we provide a finite presentation for the WD-algebra called the propagator algebra that was first introduced in [RS13] (Section 3). This finite presentation is about the structure maps, not the underlying sets. As explained in [RS13] (Section 3.4), the propagator algebra can be used, for example, to provide an iterative description of the Fibonacci sequence. In contrast to the original definition in [RS13], we will define the propagator algebra using finitely many generating structure maps and axioms—8 generating structure maps and 28 generating axioms to be exact. Since our generating structure maps are rather simple, our description of the propagator algebra is less involved than the original definition and verification in [RS13]. The equivalence between the two definitions of the propagator algebra is explained in Remark 6.3.23.

Assumption 6.3.1. Throughout this section, $S$ denotes the class of pointed sets, with respect to which $S$-boxes (Def. 2.2.7) and the operad WD are defined (Theorem 2.3.11). In a pointed set, the base point is denoted by $\ast$.

Recall the concept and notations regarding profiles from Def. 2.1.1. Let us first recall a few definitions from [RS13] (section 3).

Definition 6.3.2. Suppose $T$ and $U$ are pointed sets and $k \geq 0$.

(1) Define the truncation $\partial_T : \text{Prof}^{\geq 1}(T) \rightarrow \text{Prof}(T)$ as the function

$$\partial_T(t_1, \ldots, t_n) = (t_1, \ldots, t_{n-1}).$$

(6.3.2.1)

We will often omit the subscript and just write $\partial$.

(2) A $k$-historical propagator from $T$ to $U$ is a function $f : \text{Prof}(T) \rightarrow \text{Prof}(U)$ such that:

(i) $|f(T)| = |T| + k$ for all $T \in \text{Prof}(T)$;

(ii) If $T \in \text{Prof}(T)$ has length $|T| \geq 1$, then

$$\partial_U f(T) = f(\partial_T T).$$

(6.3.2.2)

The condition (6.3.2.2) is called historicity.

(3) The set of $k$-historical propagators from $T$ to $U$ is denoted by $\text{Hist}^k(T, U)$.

(4) A historical propagator from $T$ to $U$ is an $m$-historical propagator from $T$ to $U$ for some $m \geq 0$. 

- the operad associativity axioms (2.1.10.3) and (2.1.10.4) when applied to 2-cells;
- the fact that the transpositions $(i, i+1)$ for $1 \leq i \leq n-1$ generate the symmetric group $\Sigma_n$.

So $(A, \mu)$ is a WD-algebra in the sense of Def. 6.1.3. □
Example 6.3.3. Given a pointed set $T$ and an integer $k \geq 0$, the function $D_k : \text{Prof}(T) \rightarrow \text{Prof}(T)$ defined as

$$D_k(t_1, \ldots, t_n) = (\ast, \ldots, \ast, t_1, \ldots, t_n),$$

in which the right side starts with $k$ entries of the base point $\ast$, is a $k$-historical propagator, called the $k$-moment delay function in [RS13].

Before we can define the propagator algebra, we first need to define its entries.

Definition 6.3.4. Suppose $X = (X^{\text{in}}, X^{\text{out}}) \in \text{Box}_S$ (Def. 2.2.7).

1. Define the pointed sets

$$X_{v}^{\text{in}} = \prod_{x \in X^{\text{in}}} v(x) \quad \text{and} \quad X_{v}^{\text{out}} = \prod_{x \in X^{\text{out}}} v(x) \quad (6.3.4.1)$$

in which each $v(x)$, a pointed set, is the value of $x$ (Def. 2.2.6) and an empty product means the one-point set.

2. Define the set

$$P_X = \text{Hist}^1(X_{v}^{\text{in}}, X_{v}^{\text{out}}) \quad (6.3.4.2)$$

of 1-historical propagators of type $X$.

So a 1-historical propagator of type $X$ is a function that takes each $X_{v}^{\text{in}}$-profile to an $X_{v}^{\text{out}}$-profile whose length is one higher than before and that satisfies historicity 6.3.2.2.

Example 6.3.5. Suppose $(\mathbb{N}, 1)$ is the pointed set of non-negative integers with base point 1. Consider the box $X$ with $X^{\text{in}}$ and $X^{\text{out}}$ both equal to the one-point set $\ast$ with value $v(\ast) = (\mathbb{N}, 1)$.

A 1-historical propagator of type $X$ is a function that takes each finite sequence of non-negative integers to a sequence of non-negative integers whose length is one higher than before and that satisfies historicity. For example:

1. The 1-moment delay function in Example 6.3.3 given by

$$D_1(m_1, \ldots, m_n) = (1, m_1, \ldots, m_n)$$

for $m_i \in \mathbb{N}$, is a 1-historical propagator of type $X$. For instance, we have $D_1(1, 5, 6) = (1, 1, 5, 6)$.

2. The function $f : \text{Prof}(\mathbb{N}) \rightarrow \text{Prof}(\mathbb{N})$ defined as

$$f(m_1, \ldots, m_n) = \left(0, m_1, m_1 + m_2, \ldots, \sum_{i=1}^{n} m_i \right)$$
6.3. Finite Presentation for the Propagator Algebra

is a 1-historical propagator of type $X$, denoted "$\Sigma$" in [RS13]. This 1-historical propagator takes a sequence of non-negative integers to the sequence whose $i$th entry is the sum of the first $i - 1$ entries of the given sequence. For instance, we have $f(1, 5, 6) = (0, 1, 6, 12)$.

(3) The function $g: \text{Prof}(\mathbb{N}) \rightarrow \text{Prof}(\mathbb{N})$ defined as

$$g(m_1, \ldots, m_n) = \left(1, m_1 m_1, m_2, \ldots, \prod_{i=1}^{n} m_i \right)$$

is a 1-historical propagator of type $X$. This 1-historical propagator takes a sequence of non-negative integers to the sequence whose $i$th entry is the product of the first $i - 1$ entries of the given sequence. For instance, we have $g(1, 5, 6) = (1, 1, 5, 30)$.

**Example 6.3.6.** Consider the box $Y$ with $Y^\text{in} = \{y_1, y_2\}$, $Y^\text{out} = \{y\}$, and values $v(y_1) = v(y_2) = v(y) = (\mathbb{N}, 1)$.

A 1-historical propagator of type $Y$ is a function that takes each finite sequence of ordered pairs of non-negative integers to a sequence of non-negative integers whose length is one higher than before and that satisfies historicity. For example:

(1) The function $h: \text{Prof}(\mathbb{N} \times \mathbb{N}) \rightarrow \text{Prof}(\mathbb{N})$ given by

$$h((m_1, m'_1), \ldots, (m_n, m'_n)) = (1, m_1 + m'_1, \ldots, m_n + m'_n)$$

is a 1-historical propagator of type $Y$, denoted "$+$" in [RS13]. For instance, we have $h((1, 4), (5, 2), (6, 8)) = (1, 5, 7, 14)$.

(2) The function $j: \text{Prof}(\mathbb{N} \times \mathbb{N}) \rightarrow \text{Prof}(\mathbb{N})$ given by

$$j((m_1, m'_1), \ldots, (m_n, m'_n)) = (1, m_1 m'_1, \ldots, m_n m'_n)$$

is a 1-historical propagator of type $Y$. For instance, we have

$$j((1, 4), (5, 2), (6, 8)) = (1, 4, 10, 48).$$

**Example 6.3.7.** Consider the box $Z$ with $Z^\text{in} = \{z_1, z_2, z_3\}$, $Z^\text{out} = \{z^1, z^2\}$, and all $v(-) = (\mathbb{N}, 1)$.
6. Finite Presentation for Algebras over Wiring Diagrams

A 1-historical propagator of type $Z$ is a function that takes each finite sequence of ordered triples of non-negative integers to a sequence of ordered pairs of non-negative integers whose length is one higher than before and that satisfies historicity. For example, the function
\[ \ell : \text{Prof}(\mathbb{N} \times \mathbb{N} \times \mathbb{N}) \rightarrow \text{Prof}(\mathbb{N} \times \mathbb{N}) \]
given by
\[ \ell((m_1, m'_1, m''_1), \ldots, (m_n, m'_n, m''_n)) = ((1,1), (m_1, m'_1 + m''_1), \ldots, (m_n, m'_n + m''_n)) \]
is a 1-historical propagator of type $Z$. For instance, we have
\[ \ell((3, 1, 4), (7, 2, 9), (8, 5, 10)) = ((1,1), (3,5), (7,11), (8,15)) \].
We will come back to this example several times below.

The generating structure map of the propagator algebra associated to a 1-loop requires a few notations in its definition. So here we define this map first. The reader should keep in mind that the following definition as well as all the proofs in this section involve simple inductions on the length of some profiles.

**Definition 6.3.8.** Suppose $X \in \text{Box}_S$, $x_- \in X^\text{in}$, and $x_+ \in X^\text{out}$ such that $\nu(x_-) = \nu(x_+)$ as pointed sets. The box $X \setminus x \in \text{Box}_S$ is obtained from $X$ by removing $x = \{x_+\}$. For $\ell \in \text{Prof}(X^\text{out}_\nu)$, we will write:

(i) $\ell_{x_-} \in \text{Prof}(\nu(x_+))$ for the profile obtained from $\ell$ by taking only the $\nu(x_+)$-entry;
(ii) $\ell_{\setminus x_+} \in \text{Prof}(\nu(x_-))$ for the profile obtained from $\ell$ by removing the $\nu(x_+)$-entry.

Suppose $g \in \text{P}_X$ (6.3.4.2). Define two functions
\[ \text{Prof}(\nu(x_-)^\text{in}) \xrightarrow{\lambda g} \text{Prof}(\nu(x_+)^\text{out}) \] (6.3.8.1)
and
\[ \text{Prof}(\nu(x_-)^\text{in}) \xrightarrow{G g} \text{Prof}(\nu(x_+)) \] (6.3.8.2)
with the properties
\[ |(\lambda g)(?)| = |?| + 1 = |G g(?)| \] (6.3.8.3)
inductively as follows.

(i) For the empty profile, define
\[ (\lambda g)(\emptyset) = g(\emptyset)_{\setminus x_+} \in \text{Prof}(\nu(x_+)^\text{out}) \]
\[ G g(\emptyset) = g(\emptyset)_{x_+} \in \text{Prof}(\nu(x_+)) \] (6.3.8.4)

In each definition in (6.3.8.4), the first $\emptyset$ is the empty $(X \setminus x)^\text{in}_\nu$-profile, and the second $\emptyset$, to which $g$ applies, is the empty $X^\text{in}_\nu$-profile. The profile $g(\emptyset)$ has
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length 1 because \( g \in \text{Hist}^1 \left( X_{\text{in}}^v, X_{\text{out}}^v \right) \). So both \((\lambda g)(\emptyset)\) and \(G_{\hat{g}}(\emptyset)\) have length 1.

(ii) Inductively, suppose \( w \in \text{Prof}\left( (X \setminus x)^{\text{in}}_v \right) \) has length \( n \geq 1 \). Define

\[
(\lambda g)(w) = g(w, G_{\hat{g}}(\partial w)) \in \text{Prof}\left( (X \setminus x)^{\text{out}}_v \right)
\]

\[
G_{\hat{g}}(w) = g(w, G_{\hat{g}}(\partial w)) \in \text{Prof}(v(x_+)).
\]

(6.3.8.5)

Here \( \partial \) is the truncation \( (6.3.2.1) \), so the profile

\[
G_{\hat{g}}(\partial w) \in \text{Prof}(v(x_+)) = \text{Prof}(v(x_-))
\]

is already defined and has length \( n \) by the induction hypothesis. In each definition in \( (6.3.8.5) \),

\[
(w, G_{\hat{g}}(\partial w)) \in \text{Prof}(X_{\text{in}}^v)
\]

has length \( n \), so its image under \( g \) has length \( n + 1 \). Therefore, both \((\lambda g)(w)\) and \(G_{\hat{g}}(w)\) have length \( n + 1 \).

We say that \( \lambda g \) and \( G_{\hat{g}} \) are defined with respect to \( x = \{ x_+ \} \).

**Example 6.3.9.** This is a continuation of Example \( 6.3.7 \), where the box \( Z \) has \( Z^{\text{in}} = \{ z_1, z_2, z_3 \} \), \( Z^{\text{out}} = \{ z^1, z^2 \} \), and all \( v(-) = (\mathbb{N}, 1) \). For \( z_1 \in Z^{\text{in}} \) and \( z^1 \in Z^{\text{out}} \), suppose \( Z \setminus z \) is the box obtained from \( Z \) by removing \( z \in \{ z_1, z^1 \} \). So we have

\[
(Z \setminus z)^{\text{in}} = v(z_2) \times v(z_3) = \mathbb{N} \times \mathbb{N};
\]

\[
(Z \setminus z)^{\text{out}} = v(z^2) = \mathbb{N}.
\]

For the 1-historical propagator \( \ell \) of type \( Z \) defined as

\[
\ell((m_1, m'_1, m''_1), \ldots, (m_n, m'_n, m''_n)) = ((1, 1), (m_1, m'_1 + m''_1), \ldots, (m_n, m'_n + m''_n)),
\]

the functions

\[
\text{Prof}(\mathbb{N} \times \mathbb{N}) \xrightarrow{\lambda \ell} \text{Prof}(\mathbb{N}) \quad \text{and} \quad \text{Prof}(\mathbb{N} \times \mathbb{N}) \xrightarrow{G_{\ell}} \text{Prof}(\mathbb{N})
\]

in \( (6.3.8.1) \) and \( (6.3.8.2) \) are given as follows. Suppose

\[
m = ((m_1, m'_1), \ldots, (m_n, m'_n)) \in \text{Prof}(\mathbb{N} \times \mathbb{N})
\]

is an \( (\mathbb{N} \times \mathbb{N}) \)-profile of length \( n \geq 0 \). Then a simple induction shows that

\[
(\lambda \ell)(m) = (1, m_1 + m'_1, \ldots, m_n + m'_n),
\]

\[
G_{\ell}(m) = (1, 1, \ldots, 1),
\]
in which on the right side of $G(\bar{w})$ there are $n + 1$ copies of 1. In particular, $\lambda^\ell = h$, the 1-historical propagator of type $Y$ in Example 6.3.6. In this example, both $\lambda^\ell$ and $G^\ell$ are 1-historical propagators. This is not an accident, as we show in the next result.

The following observation will use Def. 6.3.2 about historical propagators.

**Lemma 6.3.10.** In the context of Def. 6.3.8 with $g \in P_X$, the following statements hold.

1. $Gg \in \text{Hist}^1((X \setminus x)_v, v(x_+))$.
2. $\lambda g \in \text{Hist}^1((X \setminus x)_v, (X \setminus x^\text{out})_v) = P_{X \setminus x}$.

**Proof.** In this proof, we will abbreviate $Gg$ to $G$. For statement (1), we are trying to show that $G$ is a 1-historical propagator from $(X \setminus x)_v$ to $v(x_+)$. In view of the property (6.3.8.3), it remains to check historicity (6.3.2.2) for $G$, which we will do by induction. Suppose $\bar{w} \in \text{Prof}((X \setminus x)^\text{in})_v$ has length $\geq 1$.

If $|\bar{w}| = 1$, then $\partial \bar{w} = \emptyset$. Using the definitions (6.3.8.4) and (6.3.8.5) we have:

$$\partial G(\bar{w}) = \partial g(\bar{w}, G(\emptyset))_{x_+} = g(\partial (\bar{w}, g(\emptyset)_{x_+}))_{x_+} \text{ by historicity of } g = g(\emptyset)_{x_+} = G(\emptyset).$$

Inductively, suppose $|\bar{w}| \geq 2$. Using the definition (6.3.8.5), we have:

$$\partial G(\bar{w}) = \partial g(\bar{w}, G(\partial \bar{w}))_{x_+} = g(\partial \bar{w}, \partial G(\partial \bar{w}))_{x_+} \text{ by historicity of } g = g(\partial \bar{w}, G(\partial \bar{w}))_{x_+} \text{ by the induction hypothesis on } G = G(\partial \bar{w}).$$

This finishes the proof of statement (1).

Statement (2) is proved by essentially the same argument as above, except that, in view of the definitions (6.3.8.4) and (6.3.8.5), the various right-most subscripts $x_+$ are replaced by $\setminus x_+$.

We are now ready to define the propagator algebra in terms of finitely many generating structure maps and generating axioms as in Def. 6.2.1. Most of the generating structure maps below are easily seen to be well-defined. The only exception is the generating structure map associated to a 1-loop, which we dealt with in Lemma 6.3.10 above.

**Definition 6.3.11.** Define the propagator algebra $P$ as the WD-algebra, in the sense of Def. 6.2.1 with $X$-colored entry

$$P_X = \text{Hist}^1(X^\text{in}_v, X^\text{out}_v)$$
as in (6.3.4.2) for each $X \in \text{Box}_S$. Its 8 generating structure maps are defined as follows.

1. Corresponding to the empty wiring diagram $\varepsilon \in \text{WD}^{(0)}$ (Def. 3.1.1), the structure map 

$$\varepsilon \vdash \text{ Hist}^1\{\ast\}, \{\ast\} = \{\ast\} \quad (6.3.11.1)$$

sends $\ast$ to the unique function

$$(\varepsilon \ast) \left( \ast, \ldots, \ast \right) = \left( \ast, \ldots, \ast \right).$$

2. Corresponding to each 1-delay node $\delta_d \in \text{WD}^{(1)}$ (Def. 3.1.2) with $d$ a pointed set, the structure map

$$\delta_d \vdash \text{ Hist}^1(d, d) \quad (6.3.11.2)$$

sends $\ast$ to the function

$$(\delta_d \ast)(\lambda) = (\ast, \lambda)$$

for each $\lambda \in \text{Prof}(d)$. Here the $\ast$ on the right is the base point in $d$. In other words, $\delta_d \ast$ is the 1-moment delay function in Example 6.3.3.

3. Corresponding to each name change $\tau_{X,Y} \in \text{WD}^{(1)}$ (Def. 3.1.3), the structure map

$$\text{Hist}^1(X_{\text{in}}^{\lambda_Y}, X_{\text{out}}^{\lambda_Y}) = \text{Hist}^1(Y_{\text{in}}^\tau, Y_{\text{out}}^\tau)$$

is the identity map. Here we are using the fact that, if $x \in X_{\text{in}} \cup X_{\text{out}}$ and $y \in Y_{\text{in}} \cup Y_{\text{out}}$ corresponds to $x$ under $\tau_{X,Y}$, then $\nu(x) = \nu(y)$ as pointed sets.

4. Corresponding to each 2-cell $\theta_{X,Y} \in \text{WD}^{(2)}$ (Def. 3.1.4), the structure map

$$\text{Hist}^1(X_{\text{in}}^{\lambda_Y}, X_{\text{out}}^{\lambda_Y}) \times \text{Hist}^1(Y_{\text{in}}^\tau, Y_{\text{out}}^\tau)$$

is given by

$$\theta_{X,Y}(f_X, f_Y) = f_X \times f_Y$$

for $f_X \in \text{Hist}^1(X_{\text{in}}^{\lambda_Y}, X_{\text{out}}^{\lambda_Y})$ and $f_Y \in \text{Hist}^1(Y_{\text{in}}^\tau, Y_{\text{out}}^\tau)$.

5. Corresponding to each 1-loop $\lambda_{X,x} \in \text{WD}^{(1)}$ (Def. 3.1.5), the structure map

$$\lambda_{X,x} \vdash \text{ Hist}^1(X_{\text{in}}^{\lambda_{X,x}}, X_{\text{out}}^{\lambda_{X,x}})$$

is the identity map. Here we are using the fact that, if $x \in X_{\text{in}} \cup X_{\text{out}}$ and $y \in Y_{\text{in}} \cup Y_{\text{out}}$ corresponds to $x$ under $\lambda_{X,x}$, then $\nu(x) = \nu(y)$ as pointed sets.
sends each \( g \in P_X \) to \( \lambda g \in P_{X \times X} \) (6.3.8.1), which is well-defined by Lemma 6.3.10.

(6) Corresponding to each in-split \( \sigma_{X,x_1,x_2} \in WD(\lambda) \) (Def. 3.1.6), the structure map

\[
P_X \xrightarrow{\sigma_{X,x_1,x_2}} P_Y
\]

(6.3.11.6)

is given by

\[
(\sigma_{X,x_1,x_2} g)(y) = g(\pi y)
\]

for \( g \in P_X \) and \( y \in \text{Prof}(Y^\text{in}_v) \). Here \( \pi y \in \text{Prof}(X^\text{in}_v) \) is the same as \( y \) except that its \( v(x_1) \)-entry and \( v(x_2) \)-entry are both given by the \( v(x_{12}) \)-entry of \( y \).

(7) Corresponding to each out-split \( \rho_{Y,y_1,y_2} \in WD(\lambda) \) (Def. 3.1.7), the structure map

\[
P_X \xrightarrow{\rho_{Y,y_1,y_2}} P_Y
\]

(6.3.11.7)

is given by

\[
(\rho_{Y,y_1,y_2} g)(y) = \pi g(y)
\]

for \( g \in P_X \) and \( y \in \text{Prof}(Y^\text{in}_v) = \text{Prof}(X^\text{in}_v) \). Here \( \pi g(y) \in \text{Prof}(Y^\text{out}_v) \) is the same as \( g(y) \in \text{Prof}(X^\text{out}_v) \) except that its \( v(y_1) \)-entry and \( v(y_2) \)-entry are both given by the \( v(y_{12}) \)-entry of \( g(y) \).

(8) Corresponding to each 1-wasted wire \( \omega_{Y,y} \in WD(\lambda) \) (Def. 3.1.8), the structure map

\[
P_X \xrightarrow{\omega_{Y,y}} P_Y
\]

(6.3.11.8)

is given by

\[
(\omega_{Y,y} g)(\underline{l}) = g(\underline{l}_{,y})
\]

for \( g \in P_X \) and \( \underline{l} \in \text{Prof}(Y^\text{in}_v) \). Here \( \underline{l}_{,y} \in \text{Prof}(X^\text{in}_v) \) is obtained from \( \underline{l} \) by removing the \( v(y) \)-entry.

This finishes the definition of the propagator algebra \( P \).

The following four examples continue Examples 6.3.7 and 6.3.9, where \( Z \) is the box with \( Z^\text{in} = \{z_1,z_2,z_3\} \), \( Z^\text{out} = \{z^1,z^2\} \), and all \( v(-) = (N,1) \). The 1-historical propagator \( \ell \in P_Z = \text{Hist}^1(N^3,N^2) \) is defined as

\[
\ell((m_1,m'_1,n_1'''),\ldots,(m_n,m'_n,n_n''')) = ((1,1),(m_1,m'_1 + m''_1),\ldots,(m_n,m'_n + m''_n))
\]

Let us consider the image of \( \ell \) under some of the structure maps of \( P \).

**Example 6.3.12.** Suppose \( Y \) is the box obtained from \( Z \) by removing \( z = \{z_1,z^1\} \). Consider the 1-loop (Def. 3.1.5)
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in WD(\(W\)), the structure map

\[ P_Z = \text{Hist}^1(\mathbb{N}^3, \mathbb{N}^2) \xrightarrow{\lambda_{Z,z}} \text{Hist}^1(\mathbb{N}^2, \mathbb{N}) = P_Y \]

in (6.3.11.5), and \(m = ((m_1, m'_1), \ldots, (m_n, m'_n)) \in \text{Prof}(Y^\text{in}) = \text{Prof}(\mathbb{N}^2)\). As observed in Example 6.3.9 we have

\[ (\lambda_{Z,z})(m) = h(m) = (1, m_1 + m'_1, \ldots, m_n + m'_n) \]

in \(\text{Prof}(Y^\text{out}) = \text{Prof}(\mathbb{N})\), where \(h \in P_Y\) is the 1-historical propagator in Example 6.3.6. For instance, we have

\[ (\lambda_{Z,z})(2, 5, (4, 9), (3, 7)) = (1, 7, 13, 10). \]

**Example 6.3.13.** Suppose \(W\) is the box with \(W^\text{in} = Z^\text{in}/(z_1 = z_2) = \{w, z_3\}\), and \(W^\text{out} = Z^\text{out}\). For the in-split (Def. 3.1.6)

in WD(\(W\)), the structure map

\[ P_Z = \text{Hist}^1(\mathbb{N}^3, \mathbb{N}^2) \xrightarrow{\sigma_{Z,z_1,z_2}} \text{Hist}^1(\mathbb{N}^2, \mathbb{N}^2) = P_W \]

in (6.3.11.6) applied to the 1-historical propagator \(\ell \in P_Z\) is given as follows. For \(m = ((m_1, m'_1), \ldots, (m_n, m'_n)) \in \text{Prof}(W^\text{in}) = \text{Prof}(\mathbb{N}^2)\), we have

\[ (\sigma_{Z,z_1,z_2}\ell)(m) = \ell(\pi m) = \ell((m_1, m_1, m'_1), \ldots, (m_n, m_n, m'_n)) = ((1, 1), (m_1, m_1 + m'_1), \ldots, (m_n, m_n + m'_n)) \]

in \(\text{Prof}(W^\text{out}) = \text{Prof}(\mathbb{N}^2)\). For instance, we have

\[ (\sigma_{Z,z_1,z_2}\ell)(2, 5, (4, 9), (3, 7)) = ((1, 1), (2, 7), (4, 13), (3, 10)). \]

**Example 6.3.14.** Suppose \(V\) is a box with \(V^\text{out} = \{v, v', z^2\}\) such that \(V^\text{out}/(v = v') = Z^\text{out}\), and \(V^\text{in} = Z^\text{in}\). For the out-split (Def. 3.1.7)
Suppose Example 6.3.15. in Prof applied to \( \ell \) in (6.3.11.8) applied to the 1-historical propagator \( \ell \) in (6.3.11.7) applied to the 1-historical propagator.

\[
\begin{aligned}
\sigma^{V,v,v'}(m) &= \pi \ell(m) \\
&= \pi((1,1),(m_1,m_1'+m_1''),\ldots,(m_n,m_n'+m_n'')) \\
&= ((1,1,1),(m_1,m_1,m_1'+m_1''),\ldots,(m_n,m_n,m_n'+m_n''))
\end{aligned}
\]

in Prof applied to the 1-historical propagator \( \ell \in P_Z \) given as follows. For \( m = ((m_1, m_1', m_1''), \ldots, (m_n, m_n', m_n'')) \in \text{Prof}(V^m) = \text{Prof}(N^3) \), we have

\[
\sigma^{V,v,v'}((2,5,1),(4,9,10),(3,7,6)) = ((1,1,1),(2,2,6),(4,4,19),(3,3,13)).
\]

**Example 6.3.15.** Suppose \( U \) is a box such that \( U \times u = Z \) for some \( u \in U^\text{in} \) with \( \nu(u) = (N,1) \). For the 1-wasted wire (Def. 3.1.8)

\[
\begin{aligned}
\omega_{U,u} &
\end{aligned}
\]

in WD applied to \( \ell \in P_Z \) given as follows. For

\[
\begin{aligned}
m &= \{(m_i^1, m_i^2, m_i^3, m_i^4)\}_{i=1}^n \\
&\in \text{Prof}(U^m) = \text{Prof}(\nu(u) \times \nu(z_1) \times \nu(z_2) \times \nu(z_3)) = \text{Prof}(N^4),
\end{aligned}
\]

we have

\[
\omega_{U,u}(m) = \ell(m) = \ell(\{(m_i^2, m_i^3, m_i^4)\}_{i=1}^n) \\
= ((1,1),(m_1^2, m_1^3 + m_1^4),\ldots,(m_n^2, m_n^3 + m_n^4))
\]

in Prof. For instance, we have

\[
\omega_{U,u}((2,5,1,7),(4,9,10,2),(3,7,6,5)) = ((1,1),(5,8),(9,12),(7,11)).
\]
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The following observation is the finite presentation theorem for the propagator algebra.

**Theorem 6.3.16.** The propagator algebra in Def. 6.3.11 is actually a WD-algebra in the sense of Def. 6.2.1, hence also in the sense of Def. 6.1.3 by Theorem 6.2.2.

**Proof.** We need to check the 28 generating axioms in Def. 6.2.1. The 8 generating structure maps are all rather simple functions except for \( \lambda_{x,x} \) (6.3.11.5). The only generating axioms that are not obvious are the ones that involve a composition of two such generating structure maps, namely (6.2.1.16) and (6.2.1.17). These two generating axioms are verified in Lemma 6.3.20 and Lemma 6.3.22 below. □

In preparation for Lemma 6.3.20, we will need a few definitions and notations. Recall that the generating axiom (6.2.1.16) is really the WD-algebra manifestation of Prop. 3.3.15. The next definition is essentially the double-loop version of Def. 6.3.8.

**Definition 6.3.17.** Suppose:

1. \( X \in Box_S, x_1 \neq x_2 \in X^{in} \), and \( x_1^+ \neq x_2^+ \in X^{out} \) such that \( v(x_i^+) = v(x_i^-) \) as pointed sets for each \( i \in \{1,2\} \).
2. \( X \setminus x_1, X \setminus x_2, \) and \( X \setminus x \in Box_S \) are obtained from \( X \) by removing \( x_1 = \{x_1^+\}, x_2 = \{x_2^+\}, \) and \( x = \{x_1^+, x_2^+\} \), respectively.

Suppose \( \mathfrak{I} \in \text{Prof}(X^\mathfrak{I}) \).

(i) Write \( v(x_+) = v(x_1^+) \times v(x_2^+) \) and \( v(x_-) = v(x_1^-) \times v(x_2^-) \).

(ii) Write \( \mathfrak{I}_{v_+} \in \text{Prof}(v(x_+)) \) for the profile obtained from \( \mathfrak{I} \) by taking only the \( v(x_+)-\)entries.

(iii) For \( i \in \{1,2\} \), write \( \mathfrak{I}_{v_i} \in \text{Prof}(v(x_i^+)) \) for the profile obtained from \( \mathfrak{I} \) by taking only the \( v(x_i^+)-\)entry.

(iv) The profile \( \mathfrak{I}_{v_i} \) is also defined as long as \( \mathfrak{I} \) \( \in \text{Prof}(X^\mathfrak{I}) \)

\[
\mathfrak{I}_{v_1} \in \text{Prof}
\left( \prod_{u \in T} v(u) \right)
\]

for some subset \( \{x_1^+, x_2^+\} \subseteq T \subseteq X^{out} \).

(v) Write \( \mathfrak{I}_{x_+} \in \text{Prof}(X \setminus x)^{out} \) for the profile obtained from \( \mathfrak{I} \) by removing the \( v(x_+)-\)entries.

(vi) For \( i \in \{1,2\} \), write \( \mathfrak{I}_{x_i} \in \text{Prof}(X \setminus x_i)^{out} \) for the profile obtained from \( \mathfrak{I} \) by removing the \( v(x_i^+)-\)entry.
Suppose $g \in P_X$. Define two functions

$$\text{Prof}((X \setminus x)^{\text{in}}_v) \xrightarrow{\lambda^2 g} \text{Prof}((X \setminus x)^{\text{out}}_v)$$

(6.3.17.1)

and

$$\text{Prof}((X \setminus x)^{\text{in}}_v) \xrightarrow{G^2_S} \text{Prof}(v(x_+))$$

(6.3.17.2)

with the properties

$$|\lambda^2 g(x)| = |x| + 1 = |G^2_S(x)|$$

(6.3.17.3)

inductively as follows.

(i) For the empty profile, define

$$\lambda^2 g(\emptyset) = g(\emptyset)_{\setminus x_+} \in \text{Prof}((X \setminus x)^{\text{out}}_v)$$
$$G^2_S(\emptyset) = g(\emptyset)_{\setminus x_+} \in \text{Prof}(v(x_+)).$$

(6.3.17.4)

In each definition in (6.3.17.4), the first $\emptyset$ is the empty $(X \setminus x)^{\text{in}}_v$-profile, and the second $\emptyset$, to which $g$ applies, is the empty $X_v^{\text{in}}$-profile. The profile $g(\emptyset)$ has length 1 because $g \in \text{Hist}^1(X_v^{\text{in}}, X_v^{\text{out}})$. So both $(\lambda^2 g)(\emptyset)$ and $G^2_S(\emptyset)$ have length 1.

(ii) Inductively, suppose $w \in \text{Prof}((X \setminus x)^{\text{in}}_v)$ has length $n \geq 1$. Define

$$\lambda^2 g(w) = g(w, G^2_S(\partial w))_{\setminus x_+} \in \text{Prof}((X \setminus x)^{\text{out}}_v)$$
$$G^2_S(w) = g(w, G^2_S(\partial w))_{\setminus x_+} \in \text{Prof}(v(x_+)).$$

(6.3.17.5)

Here $\partial$ is the truncation (6.3.21), so the profile

$$G^2_S(\partial w) \in \text{Prof}(v(x_+)) = \text{Prof}(v(x_-))$$

is already defined and has length $n$ by the induction hypothesis. In each definition in (6.3.17.5),

$$\lambda^2 g(w, G^2_S(\partial w)) \in \text{Prof}(X_v^{\text{in}})$$

has length $n$, so its image under $g$ has length $n + 1$. Therefore, both $(\lambda^2 g)(w)$ and $G^2_S(w)$ have length $n + 1$.

Example 6.3.18. This is a continuation of Examples 6.3.7 and 6.3.9, where $Z$ is the box with $Z^{\text{in}} = \{z_1, z_2, z_3\}$, $Z^{\text{out}} = \{z^1, z^2\}$, and all $v(-) = (N, 1)$. The 1-historical propagator $\ell \in P_Z = \text{Hist}^1(N^3, N^2)$ is defined as

$$\ell((m_1, m'_1, m''_1), \ldots, (m_n, m'_n, m''_n)) = ((1, 1), (m_1, m'_1 + m''_1), \ldots, (m_n, m'_n + m''_n)).$$

With $w^1 = \{z^1, z^1\}$ and $w^2 = \{z_2, z^2\}$, suppose $Z \setminus w$ is the box obtained from $Z$ by removing $\{z_1, z_2, z^1, z^2\}$. Then

$$(Z \setminus w)^{\text{in}}_v = v(z_3) = N \quad \text{and} \quad (Z \setminus w)^{\text{out}}_v = \star,$$

where $\star$ here is the one-point set (= empty product).
The functions

\[\text{Prof}(\mathbb{N}) \xrightarrow{\lambda^2} \text{Prof}(\ast) \quad \text{and} \quad \text{Prof}(\mathbb{N}) \xrightarrow{G^2_\ell} \text{Prof}(\mathbb{N} \times \mathbb{N})\]

in (6.3.17.1) and (6.3.17.2) are given as follows. For \(m = (m_1, \ldots, m_n) \in \text{Prof}(\mathbb{N})\), a simple induction shows that

\[(\lambda^2 \ell)(m) = (\ast, \ldots, \ast),\]

\[(G^2_\ell)(m) = ((1, 1), (1, 1 + m_1), (1, 1 + m_1 + m_2), \ldots, (1, 1 + m_1 + \ldots + m_n)),\]

where on the right side of \((\lambda^2 \ell)(m)\) there are \(n + 1\) copies of \(\ast\). For instance, we have

\[(G^2_\ell)(6, 3, 2, 9) = ((1, 1), (1, 7), (1, 10), (1, 12), (1, 21)).\]

The generating axiom (6.2.1.16) for the propagator algebra \(P\) claims that the diagram

\[
\begin{array}{ccc}
P_X & \xrightarrow{\lambda_{X,x^2}} & P_{X \times x^2} \\
\lambda_{X,x^1} & & \lambda_{X,x^2,x^1} \\
\downarrow & & \downarrow \\
P_{X \times x^1} & \xrightarrow{\lambda_{X \times x^1,x^2}} & P_{X \times x} &
\end{array}
\]

is commutative. We will consider the top-right composition, so let us use the abbreviations

\[\lambda_2 = \lambda_{X,x^2} \quad \text{and} \quad \lambda_1 = \lambda_{X \times x^1,x^1}.\]

For the proof of Lemma 6.3.20, we will need the following observation. It provides an explicit formula for the function \(G^2_\ell (6.3.17.2)\) in terms of \(G_\ell (6.3.8.2)\) (defined with respect to \(x_2\)) and \(G_{\lambda_2 \ell} (6.3.8.2)\) (defined with respect to \(x_1\)) for each \(g \in P_X\).

**Lemma 6.3.19.** In the context of Def. 6.3.17, suppose \(g \in P_X\) and \(w \in \text{Prof}((X \times x)^{\text{in}})\) with length at least 1. Then the following equalities hold.

\[
\begin{align*}
G^2_\ell (\partial w)(x^1) & = G_{\lambda_2 \ell}(\partial w) \in \text{Prof}(v(x^1)) \\
G^2_\ell (\partial w)(x_2) & = G_\ell (\partial w \partial G_{\lambda_2 \ell}(\partial w)) \in \text{Prof}(v(x_2))
\end{align*}
\]

In the above equalities:

1. \(\partial\) is the truncation (6.3.2.1).
(2) $\lambda_2 \varepsilon \in P_{X, x^2}$ by Lemma 6.3.10(2).

(3) The function

$$\Prof((X \setminus x_i)_{\text{in}}) \xrightarrow{G_{\lambda_2^g}} \Prof(\nu(x_i^1))$$

is defined with respect to $x^1 = \{x_i^1, x_i^1\}$ (6.3.8.2).

(4) The function

$$\Prof((X \setminus x^2)_{\text{in}}) \xrightarrow{G_\lambda} \Prof(\nu(x^2_i))$$

is defined with respect to $x^2 = \{x_i^2, x_i^2\}$.

**Proof.** The proof of (6.3.19.1) is by induction on $|w| \geq 1$. If $|w| = 1$, then $\partial w = \emptyset$. So by (6.3.8.4) and (6.3.17.4) we have

$$G_{\lambda_2 g}(\emptyset) = (\lambda_2 g)(\emptyset)_{x_i^1} = [g(\emptyset)_{x_i^1}]_{x_i^1} = g(\emptyset)_{x_i^1} = G_\lambda(\emptyset)_{x_i^1}.$$  

Likewise, we have

$$G_\lambda(\emptyset) = G_\lambda^2(\emptyset)_{x_i^2}.$$  

This proves the initial case $|w| = 1$.

For the induction step, suppose $|w| \geq 2$. For the first equality in (6.3.19.1) we have:

$$G_{\lambda_2 g}(\partial w) = (\lambda_2 g)(\partial w, G_{\lambda_2 g}(\partial^2 w))_{x_i^1} \text{ by } (6.3.8.5)$$

$$= g(\partial w, G_{\lambda_2 g}(\partial^2 w), G_\lambda(G_\lambda(\partial^2 w, \partial G_\lambda(\partial^2 w)))_{x_i^1} \text{ by } (6.3.8.5)$$

$$= g(\partial w, G_\lambda^2(\partial^2 w)_{x_i^1}, G_\lambda^2(\partial^2 w)_{x_i^1})_{x_i^1} \text{ by induction hypothesis}$$

$$= G_\lambda^2(\partial w)_{x_i^1} \text{ by } (6.3.17.5).$$

In the second equality above, we used the fact that

$$\left\{g(\ldots)_{x_i^1}\right\}_{x_i^1} = g(\ldots)_{x_i^1}.$$  

For the second equality in (6.3.19.1) we have:

$$G_\lambda(\partial^2 w, \partial G_{\lambda_2 g}(\partial^2 w))$$

$$= G_\lambda(\partial^2 w, G_{\lambda_2 g}(\partial^2 w)) \text{ by Lemma } 6.3.10(1)$$

$$= g(\partial^2 w, G_{\lambda_2 g}(\partial^2 w), G_\lambda(G_\lambda(\partial^2 w, \partial G_\lambda(\partial^2 w)))_{x_i^2} \text{ by } (6.3.8.5)$$

$$= g(\partial^2 w, G_\lambda^2(\partial^2 w)_{x_i^1}, G_\lambda^2(\partial^2 w)_{x_i^1})_{x_i^2} \text{ by induction hypothesis}$$

$$= G_\lambda^2(\partial w)_{x_i^2} \text{ by } (6.3.17.5).$$
This finishes the induction. □

**Lemma 6.3.20.** The propagator algebra $P$ in Def. 6.3.11 satisfies the generating axiom (6.2.1.16), i.e., the diagram (6.3.18.1) is commutative.

**Proof.** We will use the abbreviations (6.3.18.2). By the symmetry between $x^1 = \{x^1_+\}$ and $x^2 = \{x^2_+\}$, it suffices to show that

$$(\lambda_1 \lambda_2 g)(\underline{w}) = (\lambda_2^2 g)(\underline{w})$$

(6.3.20.1)

for $g \in P_{x}$ and $\underline{w} \in \text{Prof}(\langle X \setminus x^1 \rangle^{\mathrm{in}})$, where $\lambda_2^2 g$ is defined in (6.3.17.1). We prove (6.3.20.1) by induction on the length $|\underline{w}|$.

If $|\underline{w}| = 0$, then by (6.3.8.4) and (6.3.17.4) the left side of (6.3.20.1) is:

$$(\lambda_2 g)(\emptyset)_{\setminus x^1_1} = g(\emptyset)_{\setminus x^1_1} = (\lambda_2^2 g)(\emptyset).$$

For the induction step, suppose $|\underline{w}| \geq 1$. Then the left side of (6.3.20.1) is:

$$(\lambda_2 g)(\underline{w}, \partial \underline{w})_{\setminus x^1_1} = (\lambda_2^2 g)(\underline{w}, \partial \underline{w})$$

(6.3.20.1)

by (6.3.19.1)

This finishes the induction. □

The proof of the generating axiom (6.2.1.17) in Lemma 6.3.22 below will use the following observation. Recall that the generating axiom (6.2.1.17) is really a WD-algebra manifestation of the generating relation (3.3.19.1).

**Lemma 6.3.21.** In the context of Prop. 3.3.19 recall that

$$X = \frac{Y}{(x^1 = x^2)}, \quad X' = \frac{X}{(x_1 = x_2)}, \quad \text{and} \quad X^* = X \setminus \{x^{12}, x_1, x_2\}.$$ 

Consider the maps:

$$\sigma^* = \sigma_{x^1 = x^2}$$

$$P_X \xrightarrow{\sigma^* = \sigma_{x^1 = x^2}} P_Y$$

Then for $g \in P_X$ and $\underline{w} \in \text{Prof}(X^*_v^{\mathrm{in}})$ with length $\geq 1$, the equality

$$G^2_{\sigma^* g}(\partial \underline{w}) = \left(G_{\sigma^* g}(\partial \underline{w}), G_{\sigma^* g}(\partial \underline{w})\right)$$

(6.3.21.1)

holds. Here:

(1) $\sigma^* g \in P_Y$ and $\sigma^* g \in P_{X^*}$.
(2) The function

\[
\text{Prof}\left( X^\text{in}_v \right) \xrightarrow{G \circ \sigma^*} \text{Prof}\left( v(x^1) \times v(x^2) \right)
\]

is defined as in (6.3.17.2), starting with the box \( Y \) and the wires \( x^1 \neq x^2 \in Y^\text{out} \) and \( x_1 \neq x_2 \in Y^\text{in} \).

(3) The function

\[
\text{Prof}\left( X^\text{in}_v \right) \xrightarrow{G \circ \sigma^*} \text{Prof}\left( v(x_{12}) \right)
\]

is defined as in (6.3.8.2), starting with the box \( X' \) and the wires \( x_{12} \in X'^\text{in} \) and \( x_{12} \in X'^\text{out} \).

**Proof.** The proof is by induction on the length of \( w \). If \( |w| = 1 \), the \( \partial w = \emptyset \). So we have:

\[
G^2_{\sigma^* g}(\emptyset) = (\sigma^* g)(\emptyset)_{x^1, x^2} \quad \text{by (6.3.17.4)}
\]

\[
= (g(\emptyset)_{x^{12}}, g(\emptyset)_{x^{12}}) \quad \text{by (6.3.11.7)}
\]

\[
= \left( (\sigma^* g)(\emptyset)_{x^{12}}, (\sigma^* g)(\emptyset)_{x^{12}} \right) \quad \text{by (6.3.11.6)}
\]

\[
= \left( G_{\sigma^* g}(\emptyset), G_{\sigma^* g}(\emptyset) \right) \quad \text{by (6.3.8.4)}
\]

For the induction step, suppose \( |w| \geq 2 \). Then we have:

\[
G^2_{\sigma^* g}(\partial w) = (\sigma^* g)(\partial w, G^2_{\sigma^* g}(\partial^2 w))_{x^1, x^2} \quad \text{by (6.3.17.5)}
\]

\[
= (\sigma^* g)(\partial w, G_{\sigma^* g}(\partial^2 w), G_{\sigma^* g}(\partial^2 w))_{x^1, x^2} \quad \text{by induction hypothesis}
\]

\[
= \left( g(\partial w, G_{\sigma^* g}(\partial^2 w), G_{\sigma^* g}(\partial^2 w))_{x^{12}}, \text{same} \right) \quad \text{by (6.3.11.7)}
\]

\[
= \left( (\sigma^* g)(\partial w, G_{\sigma^* g}(\partial^2 w))_{x^{12}}, \text{same} \right) \quad \text{by (6.3.11.6)}
\]

\[
= \left( G_{\sigma^* g}(\partial w), G_{\sigma^* g}(\partial w) \right) \quad \text{by (6.3.8.5)}
\]

This finishes the induction. \( \square \)

**Lemma 6.3.22.** The propagator algebra \( P \) in Def. 6.3.11 satisfies the generating axiom (6.2.1.17), i.e., the diagram

\[
\begin{array}{ccc}
P_X & \xrightarrow{\sigma^* = \sigma_{Y, x^1, x^2}} & P_Y \\
\downarrow{\sigma^* = \sigma_{X, x_1, x_2}} & & \downarrow{\lambda = \lambda_{Y, x}} \\
P_X & \xrightarrow{\lambda(1) = \lambda_{Y, x(1)}} & P_{Y, x(1)} \\
\downarrow{\lambda = \lambda_{Y, x}} & & \downarrow{\lambda(2) = \lambda_{Y, x(2)}} \\
P_X & \xrightarrow{\lambda(1) = \lambda_{Y, x(1)}} & P_{X, x(1)}
\end{array}
\]

is commutative.
Proof. For \( g \in P_X \) and \( w \in \text{Prof}(X_v^{\text{out}}) \), we will prove the desired equality
\[
(\lambda \sigma \ast g)(w) = (\lambda_{(2)} \lambda_{(1)} \sigma \ast g)(w) \in \text{Prof}(X_v^{\text{out}})
\]  
(6.3.22.1)

by induction on the length of \( w \). If \(|w| = 0\), then both sides of (6.3.22.1) are equal to \( g(\emptyset) \).

For the induction step, suppose \(|w| \geq 1\). Then we have:
\[
(\lambda \sigma \ast g)(w) = (\sigma \ast g)\left( w, G_{\sigma \ast g}(\partial w) \right)_{x^{12}} \text{ by } (6.3.8.5)
\]
\[
= g\left( w, G_{\sigma \ast g}(\partial w) \right)_{x^{12}} \text{ by } (6.3.11.6)
\]
\[
= g\left( w, G_{\sigma \ast g}^2(\partial w) \right)_{x^{12}} \text{ by } (6.3.21.1)
\]
\[
= (\sigma \ast g)\left( w, G_{\sigma \ast g}^2(\partial w) \right)_{\{x^1, x^2\}} \text{ by } (6.3.11.7)
\]
\[
= (\lambda_{(2)} \lambda_{(1)} \sigma \ast g)(w) \text{ by } (6.3.17.5) \text{ and } (6.3.20.1)
\]

This finishes the induction. \( \Box \)

Remark 6.3.23. To see that our definition of the propagator algebra \( P \) in Def. 6.3.11 agrees with the one in \( \text{[RS13]} \) (Section 3), recall that our version of the propagator algebra is based on Def. 6.2.1. On the other hand, the propagator algebra in \( \text{[RS13]} \) is based on Def. 6.1.2, which is equivalent to Def. 6.1.3. A direct inspection of \( \text{[RS13]} \) (Announcement 3.3.3 and Eq. (17)) reveals that their structure map of \( P \), when applied to the generating wiring diagrams (section 3.1), reduces to our 8 generating structure maps in Def. 6.3.11. Theorem 6.2.2 then guarantees that the two definitions are equivalent.

6.4. Algebras over the Operad of Normal Wiring Diagrams

The purpose of this section is to provide a finite presentation for algebras over the \( \text{Box}_S \)-colored operad \( WD \) of normal wiring diagrams (Prop. 5.3.5). We begin by defining these algebras in terms of finitely many generators and relations. Recall from Def. 5.3.6 that a normal generating wiring diagram is a generating wiring diagram that is not a 1-delay node \( \delta_d \).

Definition 6.4.1. A \( WD \)-algebra \( A \) consists of the following data.

1. For each \( X \in \text{Box}_S \), \( A \) is equipped with a class \( A_X \) called the \( X \)-colored entry of \( A \).

2. It is equipped with the 7 generating structure maps in Def. 6.2.1 corresponding to the normal generating wiring diagrams.

This data is required to satisfy the same 28 generating axioms in Def. 6.2.1.
The next observation is the WDₜ version of Theorem 6.2.2. It guarantees that the two existing definitions of a WDₜ-algebra are equivalent. The first one (Def. 6.1.3) is in terms of a general structure map satisfying an associativity axiom for a general operadic composition. The other one (Def. 6.4.1) is in terms of 7 generating structure maps and 28 generating axioms regarding the normal generating wiring diagram. Therefore, algebras over WDₜ have a finite presentation.

**Theorem 6.4.2.** For the operad WDₜ of normal wiring diagrams (Prop. 5.3.5), Def. 6.1.3 with \( O = \text{WD} \) and Def. 6.4.1 of a WDₜ-algebra are equivalent.

**Proof.** Simply restrict the proof of Theorem 6.2.2 to normal (generating) wiring diagrams. Instead of Theorem 5.1.11 here we use Theorem 5.3.7 for the existence of a presentation involving only normal generating wiring diagrams. □

**Remark 6.4.3.** In [Spi15b] (Def. 4.1–4.4) several closely related WDₜ-algebras were defined, although they appeared in the language of symmetric monoidal categories. By Theorem 6.4.2 each of these WDₜ-algebras has a finite presentation with 7 generating structure maps and 28 generating axioms as in Def. 6.4.1. In Section 6.5 we will discuss one of these WDₜ-algebras and its finite presentation. In Section 6.7 we will discuss a similar algebra of open dynamical systems over the operad WD₀ of strict wiring diagrams. Essentially the same formalism applies to the other WDₜ-algebras in [Spi15b].

### 6.5. Finite Presentation for the Algebra of Discrete Systems

The purpose of this section is to provide a finite presentation for the algebra of discrete systems introduced in [Spi15b] (Definition 4.9). Let us first recall some definitions from [Spi15b] (Sections 2.1 and 4.1).

**Assumption 6.5.1.** Throughout this section, \( S \) denotes the class of sets. So \( \text{Box}_S = \text{Box}_{\text{Set}} \), and WDₜ is the \( \text{Box}_{\text{Set}} \)-colored operad of normal wiring diagrams (Prop. 5.3.5).

**Definition 6.5.2.** Suppose \( A \) and \( B \) are sets. An \((A,B)\)-discrete system is a triple \((T,f^{\text{rd}},f^{\text{up}})\) consisting of:

1. a set \( T \), called the state set;
2. a function \( f^{\text{rd}} : T \to B \), called the readout function;
3. a function \( f^{\text{up}} : A \times T \to T \), called the update function.

**Definition 6.5.3.** Suppose \( X = (X^{\text{in}},X^{\text{out}}) \in \text{Box}_S \) is a box. An \( X \)-discrete system is an \((X^{\text{in}},X^{\text{out}})\)-discrete system, where

\[
X^{\text{in}} = \prod_{x \in X^{\text{in}}} v(x) \quad \text{and} \quad X^{\text{out}} = \prod_{x \in X^{\text{out}}} v(x) \in \text{Set}
\]
as in \((6.3.4.1)\) (but with sets instead of pointed sets). In other words, an \(X\)-discrete system is a triple \((T, f^{rd}, f^{up})\) such that \(T\) is a set and that

\[
T \xrightarrow{f^{rd}} X^{\text{out}} \quad \text{and} \quad X^{\text{in}} \times T \xrightarrow{f^{up}} T
\]

are functions. The collection of all \(X\)-discrete systems is denoted by \(\text{DS}(X)\).

Example 6.5.4. If \(X = \emptyset \in \text{Box}_S\) is the empty box, then \(X^{\text{in}}_{\emptyset} = X^{\text{out}}_{\emptyset} = \ast\) by convention. A readout function \(f^{rd} : T \rightarrow \ast\) gives no information, and \(\ast \times T \cong T\). So

\[
\text{DS}(\emptyset) = \{(T, f^{up}) : T \in \text{Set}, f^{up} : T \rightarrow T \text{ a function}\}. \quad (6.5.4.1)
\]

In particular, the collection \(\text{DS}(\emptyset)\) is not a set but a proper class. This example explains why in Def. 6.1.2 we defined an entry of an operad algebra to be a class and not a set.

Example 6.5.5. Suppose \(X\) is the box with \(X^{\text{in}} = \{x_1, x_2\}\), \(X^{\text{out}} = \{x^1, x^2\}\), and values

\[
v(x_1) = \{a_1, b_1\}, \quad v(x_2) = \{a_2, b_2\}, \quad v(x^1) = \{a^1, b^1\}, \quad \text{and} \quad v(x^2) = \{a^2, b^2\}.
\]

An \(X\)-discrete system is an \((X^{\text{in}}_{\emptyset}, X^{\text{out}}_{\emptyset})\)-discrete system, where

\[
X^{\text{in}}_{\emptyset} = v(x_1) \times v(x_2) = \{a_1, b_1\} \times \{a_2, b_2\}; \\
X^{\text{out}}_{\emptyset} = v(x^1) \times v(x^2) = \{a^1, b^1\} \times \{a^2, b^2\}.
\]

Suppose \(T = \{1, 2\}\) is the state set. There is an \(X\)-discrete system \((T, f^{rd}, f^{up})\) with the readout function \(f^{rd} : T \rightarrow X^{\text{out}}\) and update function \(f^{up} : X^{\text{in}}_{\emptyset} \times T \rightarrow T\) defined as follows.

\[
\begin{align*}
f^{rd}(1) &= (a^1, a^2) \\
f^{rd}(2) &= (b^1, a^2)
\end{align*}
\]

\[
\begin{align*}
f^{up}((a_1, a_2), 1) &= 1 \\
f^{up}((a_1, a_2), 2) &= 1 \\
f^{up}((a_1, b_2), 1) &= 2 \\
f^{up}((a_1, b_2), 2) &= 1 \\
f^{up}((b_1, a_2), 1) &= 2 \\
f^{up}((b_1, a_2), 2) &= 2 \\
f^{up}((b_1, b_2), 1) &= 1 \\
f^{up}((b_1, b_2), 2) &= 2
\end{align*}
\]

Visually it can also be represented by the transition diagram:
For example, the arrow labeled \((b_1, a_2)\) from the box for state 1 to the box for state 2 represents the value \(f^{\uparrow}(b_1, a_2, 1) = 2\), and likewise for the other arrows.

We now define the algebra of discrete systems in terms of 7 very simple generating structure maps.

**Definition 6.5.6.** The algebra of discrete systems is the \(WD\)-algebra \(DS\) in the sense of Def. 6.4.1 defined as follows. For each \(X \in Box_S\), the \(X\)-colored entry is the class \(DS(X)\) of \(X\)-discrete systems in Def. 6.5.3

The 7 generating structure maps— as in Def. 6.2.1 but without \(\delta_d\)—are defined as follows.

1. Corresponding to the empty wiring diagram \(\varepsilon \in WD/\emptyset\) (Def. 3.1.1), the chosen element in \(DS(\emptyset)\) (6.5.4.1) is the pair \((\ast, \text{Id})\) with:
   - the one-point set \(\ast\) as its state set;
   - the identity map as its update function.

2. Corresponding to each name change \(\tau_{X,Y} \in WD_{/X}^\downarrow\) (Def. 3.1.3), the structure map
   \[ DS(X) \xrightarrow{\tau_{X,Y}} DS(Y) \]
   is the identity map, using the fact that \(X^\text{in}_v = Y^\text{in}_v\) and \(X^\text{out}_v = Y^\text{out}_v\).

3. Corresponding to a 2-cell \(\theta_{X,Y} \in WD_{/X Y}^\downarrow\) (Def. 3.1.4), it has the structure map
   \[
   DS(X) \times DS(Y) \xrightarrow{\theta_{X,Y}} \left( (T_X, f_X^{\text{rd}}, f_X^{\uparrow}), (T_Y, f_Y^{\text{rd}}, f_Y^{\uparrow}) \right)
   \]
   using the fact that
   \[
   (X \cup Y)^\text{in}_v = X^\text{in}_v \times Y^\text{in}_v \quad \text{and} \quad (X \cup Y)^\text{out}_v = X^\text{out}_v \times Y^\text{out}_v.
   \]

4. Corresponding to a 1-loop \(\lambda_{X,x} \in WD_{/X}^\downarrow\) (Def. 3.1.5) with \(x = (x_-, x_+) \in X^\text{in} \times X^\text{out}\) (so \(v(x_+) = v(x_-)\)), it has the structure map
   \[
   DS(X) \xrightarrow{\lambda_{X,x}} DS(X \setminus x) \quad \left( T, f_X^{\text{rd}}, f_X^{\uparrow} \right) \rightarrow \left( T, f_X^{\text{rd}}, f_X^{\uparrow} \right)
   \]
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in which, for \((y, t) \in (X \setminus X)^n \times T:\)

\[ f_{\up}(t) = \left( f_{\up}(t) \setminus x_i, f_{\up}(t)_{x_i} \right) \in (X \setminus x)^{out}_v \times \nu(x_+); \]

\[ f_{\down}(t) = f_{\down}(t) \setminus x_i \in (X \setminus x)^{out}_v; \]

\[ f_{\text{up}}(y, t) = f_{\text{up}}\left( \left( y, f_{\down}(t)_{x_i} \right), t \right). \]

(5) Corresponding to an in-split \(\sigma_{X,x_1,x_2} \in \text{WD}_*(X)\) (Def. 3.1.6) with \(\nu(x_1) = \nu(x_2) \) and \(Y = X/(x_1 = x_2)\), it has the structure map

\[ DS(X) \xrightarrow{\sigma_{X,x_1,x_2}} DS(Y) \quad (T, f_{\down}, f_{\up}) \longrightarrow (T, f_{\down}, \sigma_{\text{up}}f_{\up}) \]

in which the update function is

\[ (\sigma_{\text{up}}f_{\up})(y, t) = f_{\up}(\sigma_{\text{up}}y, t) \]

for \((y, t) \in Y^{in}_v \times T\). Here \(\sigma_{\text{up}}y \in X^{in}_v\) is obtained from \(y\) by using the \(\nu(x_1)\)-entry of \(y\) in both the \(\nu(x_1)\)-entry and the \(\nu(x_2)\)-entry, where \(x_1, x_2 \in Y^{in}\) is the identified element of \(x_1\) and \(x_2\).

(6) Corresponding to an out-split \(\sigma_{Y,y_1,y_2} \in \text{WD}_*(Y)\) (Def. 3.1.7) with \(\nu(y_1) = \nu(y_2)\) and \(X = Y/(y_1 = y_2)\), it has the structure map

\[ DS(X) \xrightarrow{\sigma_{Y,y_1,y_2}} DS(Y) \quad (T, f_{\down}, f_{\up}) \longrightarrow (T, f_{\down}, \sigma_{\text{down}}f_{\up}) \]

in which the readout function is

\[ (\sigma_{\text{down}}f_{\up})(t) = \sigma_{\text{down}}(f_{\down}(t)) \in Y^{out}_v \]

for \(t \in T\). Here \(\sigma_{\text{down}}(f_{\down}(t))\) is obtained from \(f_{\down}(t) \in X^{out}_v\) by using its \(\nu(y_2)\)-entry in both the \(\nu(y_1)\)-entry and the \(\nu(y_2)\)-entry, where \(y_1, y_2 \in X^{out}\) is the identified element of \(y_1\) and \(y_2\).

(7) Corresponding to a 1-wasted wire \(\omega_{Y,y} \in \text{WD}_*(Y)\) (Def. 3.1.8) with \(y \in Y^{in}\) and \(X = Y \setminus y\), it has the structure map

\[ DS(X) \xrightarrow{\omega_{Y,y}} DS(Y) \quad (T, f_{\down}, f_{\up}) \longrightarrow (T, f_{\down}, \omega f_{\up}) \]

in which the update function is

\[ (\omega f_{\up})(z, t) = f_{\up}(z, y, t) \]

for \((z, t) \in Y^{in}_v \times T\). Here \(z, y \in X^{in}_v\) is obtained from \(z\) by removing the \(\nu(y)\)-entry.

This finishes the definition of the WD*-algebra of discrete systems.
Remark 6.5.7. In [Spi15b] (Example 2.7) the image of $\theta_{X,Y}$ is called the **parallel composition**. The structure map $\lambda_{X,x}$ corresponding to a 1-loop was discussed in [Spi15b] (Example 2.9). The structure maps $\sigma_{X,x_1,x_2}$ and $\sigma^{T,y_1,y_2}$ corresponding to an in-split and an out-split were discussed in [Spi15b] (Example 2.8).

The following four examples refer to the $X$-discrete system $(T, f^{rd}, f^{up})$ in Example 6.5.5, where $X^{in} = \{x_1, x_2\}$, $X^{out} = \{x^1, x^2\}$, $v(x_i) = \{a_i, b_i\}$, and $v(x') = \{a', b'\}$ for $i = 1, 2$. Let us consider the effects of some of the structure maps in Def. 6.5.6 on $(T, f^{rd}, f^{up}) \in DS(X)$.

**Example 6.5.8.** Suppose $a_1 = a^1$ and $b_1 = b^1$, so $v(x_1) = \{a_1, b_1\} = v(x^1)$. Suppose $X \setminus x$ is the box obtained from $X$ by removing $x = \{x_1, x^1\}$, so $(X \setminus x)^{in} = v(x_2)$ and $(X \setminus x)^{out} = v(x^2)$. Consider the 1-loop (Def. 3.1.6)

$$
\lambda_{X,x}
$$

in $WD_*(X)$. Then

$$
\lambda_{X,x}(T, f^{rd}, f^{up}) = (T, f^{rd}_{X,x}, f^{up}_{X,x}) \in DS(X \setminus x)
$$

is the $(X \setminus x)$-discrete system with update and readout functions

$$
(X \setminus x)^{in} \times T = \{a_2, b_2\} \times T \xrightarrow{f^{up}_{X,x}} T \xrightarrow{f^{rd}_{X,x}} \{a^2, b^2\} = (X \setminus x)^{out}.
$$

Its transition diagram is:

For instance, we have

$$
f^{up}_{X,x}(a_2, 1) = f^{up}_{X,x}((a_2, f^{rd_{X,x}}(1), 1) = f^{up}_{X,x}((a_1, a_2), 1) = 1,
$$

which explains the loop at state 1 labeled $a_2$. Similar calculation yields the rest of the update function and the readout function.

**Example 6.5.9.** Suppose $a_1 = a_2$ and $b_1 = b_2$, so $v(x_1) = \{a_1, b_1\} = v(x_2)$. Suppose $Y$ is the box $X/(x_1 = x_2)$, so $Y^{in} = v(x_1)$ and $Y^{out} = X^{out}$. Consider the in-split (Def. 3.1.6)
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\[ \sigma_{X,x_1,x_2}(T, f^{rd}, f^{up}) = (T, f^{rd}, \sigma_\star f^{up}) \in \text{DS}(Y) \]

is the \( Y \)-discrete system with update and readout functions
\[ \gamma^{\text{in}}_v \times T = \{a_1, b_1\} \times T \xrightarrow{\sigma_\star f^{up}} T \xrightarrow{f^{rd}} \gamma^{\text{out}}_v = \{a^1, b^1\} \times \{a^2, b^2\} \]

Its transition diagram is:

For instance, we have
\[ (\sigma_\star f^{up})(a_1, 2) = f^{up}(a_1, a_2, 2) = 1, \]
which explains the arrow from state 2 to state 1 labeled \( a_1 \). Similar calculation yields the rest of the update function.

**Example 6.5.10.** Suppose \( Z \) is a box with \( z \neq z' \) in \( Z^{\text{out}} \) such that \( v(z) = v(z') = v(x_1) \) and that \( Z/(z = z') = X \). So \( Z^{\text{in}}_v = X^{\text{in}}_v \) and \( Z^{\text{out}}_v = v(x_1) \times v(x_1) \times v(x_2) \). Consider the out-split (Def. 3.1.7)

\[ \sigma^{Z,z,z'}(T, f^{rd}, f^{up}) = (T, \sigma^\star f^{rd}, f^{up}) \in \text{DS}(Z) \]

is the \( Z \)-discrete system with update and readout functions
\[ Z^{\text{in}}_v \times T = X^{\text{in}}_v \times T \xrightarrow{f^{up}} T \xrightarrow{\sigma^\star f^{rd}} Z^{\text{out}}_v. \]

Its transition diagram is:
This transition diagram is the same as that of \((T, f^{rd}, f^{up})\), except for the values of the readout function at states 1 and 2.

**Example 6.5.11.** Suppose \(W\) is a box such that \(W \setminus w = X\) for some \(w \in W_{\text{in}}\). So \(W_{\text{in}}^{w} = v(w) \times X_{\text{in}}^{w}\) and \(W_{\text{out}} = X_{\text{out}}^{w}\). Consider the 1-wasted wire (Def. 3.1.8)

\[
\omega^{w}_{W, w}, W_{\text{in}}^{w} \xrightarrow{w} W_{\text{out}}^{w}
\]

in \(WD_{\ast}(W)\). Then

\[
\omega^{w}_{W, w}(T, f^{rd}, f^{up}) = (T, f^{rd}, \omega^{w} f^{up}) \in DS(W)
\]

is the \(W\)-discrete system with update and readout functions

\[
W_{\text{in}}^{w} \times T = v(w) \times X_{\text{in}}^{w} \xrightarrow{\omega^{w} f^{up}} T \xrightarrow{f^{rd}} W_{\text{out}}^{w}.
\]

Its transition diagram is:

Here each double arrow \(\Rightarrow\) represents the set of arrows as \(s\) runs through \(v(w)\). For instance, for each \(s \in v(w)\) we have

\[
(\omega^{w} f^{up})(s, a_{1}, b_{2}) = f^{up}(a_{1}, b_{2}) = 2,
\]

which explains the double arrow from state 1 to state 2 labeled \((s, a_{1}, b_{2})\). Similar calculation yields the rest of the update function.

The following observation ensures that \(DS\) is a well-defined \(WD_{\ast}\)-algebra, i.e., that it satisfies the generating axioms.
**Theorem 6.5.12.** The algebra of discrete systems $DS$ in Def. 6.5.6 is actually a $WD_\bullet$-algebra in the sense of Def. 6.4.1 hence also in the sense of Def. 6.1.3 by Theorem 6.4.2.

**Proof.** We must check that $DS$ satisfies the 28 generating axioms in Def. 6.2.1, which are all trivial to check. For example, the generating axiom (6.2.1.17) says that, in the setting of (3.3.19.1) with $X^* = X \setminus \{x^{12}, x_1, x_2\}$ and $v(x^{12}) = v(x_1) = v(x_2)$, the diagram

$$
\begin{array}{c}
DS(X) \xrightarrow{\sigma_{X,Y}^{x_1,x_2}} DS(Y) \xrightarrow{\lambda_{Y,x}(1)} DS(Y \setminus x(1)) \\
\downarrow \quad \downarrow \\
DS(X') \xrightarrow{\lambda_{X',x}} DS(X^*)
\end{array}
$$

is commutative. When applied to a typical element $(T, f^{rd}, f^{up}) \in DS(X)$, a simple direct inspection reveals that both compositions in the above diagram yield $(T, g^{rd}, g^{up}) \in DS(X^*)$, in which

$$
\begin{align*}
g^{rd}(t) &= f^{rd}(t) \setminus x^{12}; \\
g^{up}(y, t) &= f^{up}(y, f^{rd}(t)_{x^{12}}, f^{rd}(t)_{x^{12}}, t)
\end{align*}
$$

Here for $(y, t) \in X^{in}_v \times T$, we have

$$
\begin{align*}
f^{rd}(t) &= \left(f^{rd}(t) \setminus x^{12}, f^{rd}(t)_{x^{12}}\right) \in X^{out}_v = X^{out}_v \times v(x^{12}); \\
(y, f^{rd}(t)_{x^{12}}, f^{rd}(t)_{x^{12}}) &\in X^{in}_v \times v(x_1) \times v(x_2) = X^{in}_v.
\end{align*}
$$

The other generating axioms are checked similarly. \qed

**Remark 6.5.13.** Our definition of the algebra of discrete systems $DS$ actually agrees with the one in [Spi15b] (Example 2.7 and Def. 4.9). To see this, note that Spivak’s definition is essentially based on Def. 6.1.2 except that it is stated in terms of symmetric monoidal categories. Spivak’s structure map of $DS$, when applied to the 7 normal generating wiring diagrams (Def. 5.3.6(1)), agrees with ours in Def. 6.5.6. So Theorems 6.4.2 and 6.5.12 imply that the two definitions of $DS$—namely, the one in [Spi15b] and our Def. 6.5.6—are equivalent.

### 6.6. Algebras over the Operad of Strict Wiring Diagrams

The purpose of this section is to provide a finite presentation for algebras over the $Box_\mathcal{S}$-colored operad $WD_0$ of strict wiring diagrams (Prop. 5.4.6). We begin by defining these algebras in terms of finitely many generators and relations. Recall from Def. 5.4.7 that:

1. The strict generating wiring diagrams are the empty wiring diagram $\varepsilon$, a name change $\tau_{X,Y}$, a 2-cell $\theta_{X,Y}$, and a 1-loop $\lambda_{X,x}.$
2. The *strict elementary relations* are the 8 elementary relations that involve only strict generating wiring diagrams on both sides.

**Definition 6.6.1.** A WD₀-algebra A consists of the following data.

1. For each X ∈ Box_S, A is equipped with a class A_X called the X-colored entry of A.
2. It is equipped with the 4 generating structure maps in Def. 6.2.1 corresponding to the strict generating wiring diagrams.

This data is required to satisfy the 8 generating axioms in Def. 6.2.1 corresponding to the strict elementary relations, namely, (6.2.1.9), (6.2.1.10), (6.2.1.11), (6.2.1.12), (6.2.1.13), (6.2.1.14), (6.2.1.15), and (6.2.1.16).

The next observation is the WD₀ version of Theorems 6.2.2 and 6.4.2. It gives a finite presentation for WD₀-algebras.

**Theorem 6.6.2.** For the operad WD₀ of strict wiring diagrams (Prop. 5.4.6), Def. 6.1.3 with O = WD₀ and Def. 6.6.1 of a WD₀-algebra are equivalent.

**Proof.** Simply restrict the proof of Theorem 6.2.2 to strict (generating) wiring diagrams. Instead of Theorem 5.1.11, here we use Theorem 5.4.8 for the existence of a presentation involving only strict generating wiring diagrams. ■

6.7. Finite Presentation for the Algebra of Open Dynamical Systems

The purpose of this section is to provide a finite presentation for the algebra of open dynamical systems introduced in [VSL15]. In [VSL15] the algebra of open dynamical systems G was defined and verified using essentially Def. 6.1.2 but in the form of symmetric monoidal categories and monoidal functors. Our definition of G in Def. 6.7.7 is based on Def. 6.6.1 which involves four relatively simple generating structure maps. Our verification that G is actually a WD₀-algebra in Theorem 6.7.9 boils down to verifying the generating axiom (6.2.1.16) for a double-loop. This is a simple exercise involving the definition of the generating structure map corresponding to a 1-loop (6.7.7.4). The equivalence between the two definitions of the algebra of open dynamical systems is explained in Remark 6.7.10.

Let us first recall the setting of [VSL15]. For the definitions of the basic objects in differential geometry that appear below, the reader may consult, for example, [Hel78] (Ch.1).

**Assumption 6.7.1.** Throughout this section:

1. S is a chosen set of representatives of isomorphism classes of second-countable smooth manifolds, henceforth called manifolds.
(2) The operad of strict wiring diagrams $\text{WD}_0$ (Prop. 5.4.6) is defined using this choice of $S$.

(3) All the maps between manifolds are smooth maps.

(4) For a manifold $M$, denote by $\pi : TM \to M$ the projection map of the tangent bundle.

**Definition 6.7.2.** Suppose $(M, v) \in \text{Fin}_S$ is an $S$-finite set (Def. 2.2.6).

1. Define $M_v = \prod_{m \in M} v(m) \in S$. \hfill (6.7.2.1)

2. For a subset $I \subseteq M$ and $x = (x_m)_{m \in M} \in M_v$, define $x_I = (x_m)_{m \in I} \in I_v = \prod_{m \in I} v(m)$ \hfill (6.7.2.2)

$x_{\setminus I} = (x_m)_{m \in M \setminus I} \in (M \setminus I)_v = \prod_{m \in M \setminus I} v(m)$.

**Definition 6.7.3.** An open dynamical system, or ods for short, is a tuple $(M, U^{\text{in}}, U^{\text{out}}, f)$ consisting of:

1. manifolds $M$, $U^{\text{in}}$, and $U^{\text{out}}$,

2. a pair of maps $f = (f^{\text{in}}, f^{\text{out}})$,

\[
\begin{array}{ccc}
M \times U^{\text{in}} & \xrightarrow{f^{\text{in}}} & TM \\
\downarrow \text{project} & & \downarrow \pi \\
M & & M \\
\end{array}
\]

\[
\begin{array}{ccc}
& & \downarrow f^{\text{out}} \\
M & \xrightarrow{\text{project}} & M^{\text{out}} \\
\end{array}
\]

such that the left diagram is commutative.

Next is [VSL15] (Def. 4.2).

**Definition 6.7.4.** For each $X = (X^{\text{in}}, X^{\text{out}}) \in \text{Box}_S$, define the class

$$G_X = \left\{(M, f) : M \in \text{Fin}_S, (M_v, X^{\text{in}}_v, X^{\text{out}}_v, f) \text{ is an ods}\right\}$$ \hfill (6.7.4.1)

in which $M_v$, $X^{\text{in}}_v$, and $X^{\text{out}}_v$ are as in (6.7.2.1).

**Example 6.7.5.** For the empty box $\emptyset = (\emptyset, \emptyset) \in \text{Box}_S$ and an $S$-finite set $M$, to say that $(M_v, \emptyset_v = \{\ast\}, \emptyset_v = \{\ast\}, f)$ is an open dynamical system means that $f$ is a pair of maps $f = (f^{\text{in}}, f^{\text{out}})$,

\[
\begin{array}{ccc}
M_v = M_v \times \{\ast\} & \xrightarrow{f^{\text{in}}} & TM_v \\
\downarrow \text{Id} & & \downarrow \pi \\
M_v & & M_v \\
\end{array}
\]

\[
\begin{array}{ccc}
& & \downarrow f^{\text{out}} \\
M_v & \xrightarrow{\text{project}} & \{\ast\} \\
\end{array}
\]
such that the left diagram is commutative. Since $f^{\text{out}}$ gives no information, $f = f^{\text{in}}$ is equivalent to a vector field on $M_v$. So

$$G_{\emptyset} = \{(M, f) : M \in \text{Fin}_S, f \text{ is a vector field on } M_v\}.$$  \hfill (6.7.5.1)

**Example 6.7.6.** Suppose $W$ is the box with $W^{\text{in}} = \{w_1, w_2\}$, $W^{\text{out}} = \{w^1, w^2\}$, and all $v(-) = \mathbb{R}$, so $W^{\text{in}}_v = W^{\text{out}}_v = \mathbb{R}^2$. Suppose $M$ is the one-point set with value $\mathbb{R}$. There is an element $(M, f) \in G_W$ whose structure maps

$$\mathbb{R} \times \mathbb{R}^2 \xrightarrow{f^{\text{in}}} TM = \mathbb{R}^2 \xrightarrow{\pi_1} \mathbb{R} \xrightarrow{f^{\text{out}}} \mathbb{R}^2$$

are given by

$$f^{\text{in}}(x, y, z) = (x, ax + by + cz) \quad \text{and} \quad f^{\text{out}}(x) = (dx, e^x)$$

for any choice of fixed parameters $a, b, c, d \in \mathbb{R}$.

We now define the algebra of open dynamical systems in terms of 4 generating structure maps.

**Definition 6.7.7.** The *algebra of open dynamical systems* is the $\text{WD}_0$-algebra $G$ in the sense of Def. 6.6.1 defined as follows. For each box $X \in \text{Box}_S$, the $X$-colored entry is $G_X$ in (6.7.4.1).

The 4 generating structure maps (Def. 6.2.1) are defined as follows.

1. Corresponding to the empty wiring diagram $\varepsilon \in \text{WD}_0(\emptyset)$ (Def. 3.1.1), the structure map

$$\xymatrix{\ast \ar[r]^-{\varepsilon} & G_{\emptyset}}$$

sends $\ast$ to $(\emptyset, \ast) \in G_{\emptyset}$ (6.7.5.1). Here $\emptyset \in \text{Fin}_S$ is the empty set, in which $\emptyset_v = \{\ast\}$, and in the second entry $\ast$ is the trivial vector field.

2. Corresponding to a name change $\tau_{X,Y} \in \text{WD}_0(\emptyset)$ (Def. 3.1.3), the structure map

$$G_X \xrightarrow{\tau_{X,Y}} G_Y$$

is the identity map, using the fact that $X^{\text{in}}_v = Y^{\text{in}}_v$ and $X^{\text{out}}_v = Y^{\text{out}}_v$. 
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(3) Corresponding to a 2-cell \( \theta_{X,Y} \in WD_0(X, Y) \) (Def. 3.1.4), it has the structure map

\[
\begin{array}{ccc}
G_X \times G_Y & \longrightarrow & (M_X, f_X, (M_Y, f_Y)) \\
\theta_{X,Y} & \downarrow & \downarrow \\
G_{X\sqcup Y} & & (M_X \sqcup M_Y, f_X \times f_Y)
\end{array}
\]  

(6.7.7.3)
in which \( M_X \sqcup M_Y \) is the coproduct in \( \text{Fin} \) (Def. 2.2.6).

(4) Corresponding to a 1-loop \( \lambda_{X,x} \in WD_0(X) \) (Def. 3.1.5) with \( x = (x_-, x_+) \in X^{\text{in}} \times X^{\text{out}} \), it has the structure map

\[
G_X \xrightarrow{\lambda_{X,x}} G_{X\setminus x} (M, f) \longmapsto (M, f_{\setminus x}).
\]  

(6.7.7.4)
The maps \( f_{\setminus x} = (f_{\setminus x}^{\text{in}}, f_{\setminus x}^{\text{out}}) \) are defined as

\[
\begin{align*}
f_{\setminus x}^{\text{in}}(m, y) &= f_{\setminus x}^{\text{in}}(m, (f_{\text{out}}(m)_{x_+}, v(x_+)) \in TM_{\text{in}}, \\
f_{\setminus x}^{\text{out}}(m) &= f_{\text{out}}(m)_{x_+} \in (X \setminus x)^{\text{out}}
\end{align*}
\]

for \( m \in M \) and \( y \in (X \setminus x)^{\text{in}} \). Recalling that \( f_{\text{out}}(m) \in X^{\text{out}} \), the elements \( f_{\text{out}}(m)_{x_+} \in v(x) \) and \( f_{\text{out}}(m)_{x_+} \in (X \setminus x)^{\text{out}} \) are as in (6.7.2.2).

This finishes the definition of the \( WD_0 \)-algebra of open dynamical systems.

**Example 6.7.8.** This is a continuation of Example 6.7.6, where \( W \) is the box with \( W^{\text{in}} = \{ w_1, w_2 \} \) and \( W^{\text{out}} = \{ w^1, w^2 \} \) and \( M \) is the one-point set, all with \( v(\cdot) = \mathbb{R} \). Suppose \( W \setminus w \) is the box obtained from \( W \) by removing \( w = \{ w_1, w^1 \} \), so \( (W \setminus w)^{\text{in}} = (W \setminus w)^{\text{out}} = \mathbb{R} \).

Consider the 1-loop (Def. 3.1.5)

\[
\begin{array}{ccc}
W & \xrightarrow{\lambda_{W,w}} & (W \setminus w)^{\text{in}} \\
W & \xrightarrow{\lambda_{W,w}} & (W \setminus w)^{\text{out}}
\end{array}
\]
in \( WD_0(W \setminus w) \). Then \( \lambda_{W,w}(M, f) = (M, f_{\setminus w}) \in G_{W \setminus w} \) has structure maps

\[
\begin{array}{ccc}
\mathbb{R} \times \mathbb{R} & \longrightarrow & TM = \mathbb{R}^2 \\
\pi_1 & \downarrow & \pi_1 \\
\mathbb{R} & \xrightarrow{f_{\setminus w}} & \mathbb{R}
\end{array}
\]
given by
\[ f^{\text{out}}_{\mathcal{W}}(x) = f^{\text{out}}_{\mathcal{W}}(x)_\mathcal{W}^1 = (dx, e^x)_\mathcal{W}^1 = e^x; \]
\[ f^{\text{in}}_{\mathcal{W}}(x, y) = f^{\text{in}}(x, (f^{\text{out}}_{\mathcal{W}}(x)_\mathcal{W}^1, y)) = f^{\text{in}}(x, dx, y) = (x, (a + bd)x + cy). \]

The following observation ensures that \( G \) is a well-defined \( \mathcal{W}D_0 \)-algebra, i.e.,
that it satisfies the generating axioms.

**Theorem 6.7.9.** The algebra of open dynamical systems \( G \) in Def. 6.7.7 is actually a \( \mathcal{W}D_0 \)-algebra in the sense of Def. 6.6.1, hence also in the sense of Def. 6.1.3 by Theorem 6.6.2.

**Proof.** We must check the 8 generating axioms corresponding to the strict elementary relations listed in Def. 6.6.1. All of them follow from a quick inspection of the definitions except for (6.2.1.16). This generating axiom says that, in the setting of the elementary relation (3.3.15.1) corresponding to a double-loop, the diagram

\[ \begin{array}{ccc}
G_{X \setminus x^1} & \xrightarrow{\lambda_{x^2, x^3}} & G_{X \setminus x^2} \\
\lambda_{x^2} & & \lambda_{x^3} \\
G_{X \setminus x^2} & \xrightarrow{\lambda_{x^1, x^3}} & G_{X \setminus x^1}
\end{array} \]  

(6.7.9.1)
is commutative.

To prove (6.7.9.1), suppose \((M, f) \in G_X\). First define the element \((M, f_{\setminus x}) \in G_{X \setminus x}\) with the maps \(f_{\setminus x} = (f^{\text{in}}_{\setminus x}, f^{\text{out}}_{\setminus x})\),

\[
\begin{array}{ccc}
M \times (X \setminus x)_{x} & \xrightarrow{f^{\text{in}}_{\setminus x}} & TM_v \\
\text{project} & & \pi \\
M & \xrightarrow{\pi} & (X \setminus x)_{x}^{\text{out}}
\end{array}
\]

defined as follows. Given \(m \in M_v\) and

\[
y \in (X \setminus x)_{x} = \prod_{y \in X \setminus \{x^1, x^2\}} v(y)
\]
we define

\[
\begin{align*}
f^{\text{in}}_{\setminus x}(m, y) &= f^{\text{in}}(m; (f^{\text{out}}(m)_{x^1, x^2}, y)) \in TM_v \\
f^{\text{out}}_{\setminus x}(m) &= f^{\text{out}}(m)_{x^1, x^2} \in (X \setminus x)_{x}^{\text{out}}.
\end{align*}
\]

Recalling that \(f^{\text{out}}(m) \in X_v^{\text{out}}\), the elements

\[
f^{\text{out}}(m)_{x^1, x^2} \in v(x^1_+) \times v(x^2_+) = v(x^1_-) \times v(x^2_-)
\]

and \(f^{\text{out}}(m)_{x^1, x^2} \) are as in (6.7.2.2).
6.8. Summary of Chapter 6

Now it follows from a direct inspection using the definition (6.7.7.4) that both composites in (6.7.9.1), when applied to $(M, f)$, yields $(M, f \setminus x) \in G_{X \setminus x}$. This proves the generating axiom (6.7.9.1) for $G$. □

Remark 6.7.10. Our definition of the algebra of open dynamical systems $G$ actually agrees with the one in [VSL15] (Def. 4.4 and 4.5). To see this, note that among the four generating structure maps in Def. 6.7.7:

- $\varepsilon$ (6.7.7.1), $\tau_{X,Y}$ (6.7.7.2), and $\lambda_{X,x}$ (6.7.7.4) agree with [VSL15] (Def. 4.4);

- $\theta_{X,Y}$ (6.7.7.3) agrees with [VSL15] (Def. 4.5).

Theorem 6.6.2 then implies that the two definitions of $G$—namely, the one in [VSL15] and our Def. 6.7.7—are equivalent.

6.8. Summary of Chapter 6

(1) For an $S$-colored operad $O$, an $O$-algebra $A$ consists of a class $A_c$ for each $c \in S$ and a structure map

$$A_{c_1} \times \cdots \times A_{c_n} \xrightarrow{\zeta} A_d$$

for each $\zeta \in O(\langle c_1, \ldots, c_n \rangle)$ that satisfies the associativity, unity, and equivariance axioms.

(2) Each WD-algebra can be described using eight generating structure maps that satisfy twenty-eight generating axioms.

(3) The propagator algebra is a WD-algebra.

(4) Each WD$_*$-algebra can be described using seven generating structure maps that satisfy twenty-eight generating axioms.

(5) The algebra of discrete systems is a WD$_*$-algebra.

(6) Each WD$_0$-algebra can be described using four generating structure maps that satisfy eight generating axioms.

(7) The algebra of open dynamical systems is a WD$_0$-algebra.
Part 2

Undirected Wiring Diagrams
The main purpose of this part is to describe the combinatorial structure of the operad UWD of undirected wiring diagrams. The main result is a finite presentation theorem that describes the operad UWD in terms of 6 operadic generators and 17 generating relations.

The operad UWD of undirected wiring diagrams is recalled in Chapter 7. Operadic generators and generating relations for the operad UWD are presented in Chapter 8. Various decompositions of undirected wiring diagrams are given in Chapter 9. Using the results in Chapters 8 and 9, the finite presentation theorem for the operad UWD is proved in Chapter 10. In Chapter 11 we prove the corresponding finite presentation theorem for UWD-algebras and discuss the main example of the relational algebra. This finite presentation theorem for algebras describes each UWD-algebra in terms of finitely many generating structure maps and relations among these maps. Also given in this Chapter is a partial verification of a conjecture of Spivak about the rigidity of the relational algebra.

Reading Guide. The reader who already knows about pushouts of finite sets may skip Section 7.2. In Section 7.3, where we define the operad structure on undirected wiring diagrams, the reader may wish to skip the proofs of Lemmas 7.3.11 and 7.3.13 and just study the accompanying pictures.

Section 8.3 is not technically needed in later sections. However, it contains several illuminating examples about how wasted cables can be created from undirected wiring diagrams without wasted cables. So we urge the reader not to skip these examples.

The decompositions in Chapter 9 are illustrated with a detailed example in Section 9.1. The reader may read that section and skip the rest of the Chapter during the first reading.

In Section 10.2, after the initial definitions and examples, the reader may skip the proofs of Lemmas 10.2.5 and 10.2.6 and go straight to Theorem 10.2.7, the finite presentation theorem for undirected wiring diagrams.
Chapter 7

Undirected Wiring Diagrams

The purposes of this chapter are

1. to recall the definition of an undirected wiring diagram (Def. 7.1.4) from [Spi13];

2. to give a proof that the collection of undirected wiring diagrams forms an operad (Theorem 7.3.14).

There is a subtlety regarding the definition and the operadic composition of undirected wiring diagrams; see Remark 7.1.5(4) and Example 7.3.8. Many more examples of undirected wiring diagrams and their operadic composition will be given in the next chapter.

Fix a class $S$ for this chapter.

7.1. Defining Undirected Wiring Diagrams

In this section, we recall the definition of an undirected wiring diagram. Recall from Def. 2.2.6 that an $S$-finite set is a pair $(X, v)$ with $X$ a finite set and $v : X \to S$ a function, called the value assignment. Maps between $S$-finite sets are functions compatible with the value assignments. The category of $S$-finite sets is denoted by $\text{Fin}_S$. As in earlier chapters, if there is no danger of confusion, then we write an $S$-finite set $(X, v)$ simply as $X$. The number of elements in a finite set $T$ is denoted by $|T|$. As in Section 2.2 we first define undirected prewiring diagrams. Undirected wiring diagrams are then defined as the appropriate equivalence classes.
Motivation 7.1.1. Before we define an undirected wiring diagram precisely, let us first provide some motivation for it. An undirected wiring diagram is a picture similar to this:

There are two input boxes \( X_1 = \{x_1, \ldots, x_6\} \) and \( X_2 = \{x^1, x^2\} \), an output box \( Y = \{y_1, \ldots, y_6\} \), and seven cables \( \{c_1, \ldots, c_7\} \). In general, there can be any finite numbers of input boxes and cables, and each input/output box is a finite set. For each element \( z \) in the input boxes and the output box, we need to specify a cable \( c \) to which \( z \) is connected. For instance, \( x_4, x_5, \) and \( x^2 \) are connected to the cable \( c_6 \).

Depending on the given undirected wiring diagrams, there are four possible kinds of cables. First, a cable may only be connected to elements in the inside boxes, such as \( c_6 \) and \( c_7 \) in the picture above. Second, a cable may only be connected to elements in the outside box, such as \( c_1 \) and \( c_5 \) above. Third, a cable may be connected to elements in both the inside boxes and the outside box, such as \( c_2 \) and \( c_3 \) above. Finally, there may be standalone cables that are not connected to anything in the inside and the outside boxes, such as \( c_4 \) above. Such distinction among the set of cables will be important later when we discuss the finite presentation for the operad of undirected wiring diagrams. We will come back to this picture in Example 7.1.7 below.

The following definition is a slight generalization of [Spi13] (Examples 2.1.7 and 4.1.1); see Remark 7.1.5.

Definition 7.1.2. Suppose \( S \) is a class. An undirected \( S \)-prewiring diagram is a tuple

\[
\varphi = (X, Y, C, f, g)
\]

consisting of the following data.

1. \( Y \in \text{Fin}_S \), called the output box of \( \varphi \). An element in \( Y \) is called an output wire for \( \varphi \).
2. \( X = (X_1, \ldots, X_n) \) is a \( \text{Fin}_S \)-profile for some \( n \geq 0 \) (Def. 2.1.1); i.e., each \( X_i \in \text{Fin}_S \).
   - We call \( X_i \) the \( i \)th input box of \( \varphi \).
   - An element in each \( X_i \) is called an input wire for \( \varphi \).
   - Denote by \( X = \bigsqcup_{i=1}^n X_i \in \text{Fin}_S \) the coproduct.
7.1. Defining Undirected Wiring Diagrams

- Each element in \(X \uplus Y\) is called a wire.

(3) \(C \in \text{Fin}_S\), called the set of cables of \(\varphi\). Each element in \(C\) is called a cable.

(4) \(f\) and \(g\) are maps in the diagram, called a cospan

\[
\begin{array}{ccc}
X_1 \uplus \cdots \uplus X_n = X & \xrightarrow{f} & C & \xleftarrow{g} & Y \\
\end{array}
\]

in \(\text{Fin}_S\).

- \(f\) is called the input soldering function and \(g\) the output soldering function.

- If \(f(x) = c\), then we say that \(x\) is soldered to \(c\) and that \(c\) is soldered to \(x\) via \(f\). If \(g(y) = c\), then we say that \(y\) is soldered to \(c\) and that \(c\) is soldered to \(y\) via \(g\).

- If \(c \in C\) is a cable and if \(m = |f^{-1}(c)|\) and \(n = |g^{-1}(c)|\), then \(c\) is called an \((m,n)\)-cable.

- A \((0,0)\)-cable is also called a wasted cable. In other words, a wasted cable is a cable that is in neither the image of \(f\) nor the image of \(g\).

Given \(Y\) and \(X\), we will denote \(\varphi\) as either the tuple \((C, f, g)\) or the cospan \((7.1.2.2)\).

**Remark 7.1.3.** In Def. \([2.2.7]\) an \(S\)-box is an element in \(\text{Fin}_S \times \text{Fin}_S\). In the context of undirected (pre)wiring diagrams, the name box refers to an element in \(\text{Fin}_S\), such as the output box or one of the input boxes. The context itself should make it clear what box means.

The cables tell us how to wire the input wires and the output wires together. So the names of the cables should not matter. This is made precise in the following definition.

**Definition 7.1.4.** Suppose \(\varphi = (X, Y, C, f, g)\) and \(\varphi' = (X, Y, C', f', g')\) are two undirected \(S\)-prewiring diagrams with the same output box \(Y\) and input boxes \(X\).

(1) An equivalence \(h : \varphi \rightarrow \varphi'\) is an isomorphism \(h : C \rightarrow C' \in \text{Fin}_S\) such that the diagram

\[
\begin{array}{ccc}
X & \xrightarrow{f} & C & \xleftarrow{g} & Y \\
\downarrow{f'} & \uparrow{\cong} & \downarrow{h} & \downarrow{g'} \\
C' & \xleftarrow{h} & & \xrightarrow{g'} \\
\end{array}
\]

in \(\text{Fin}_S\) is commutative.

(2) We say that \(\varphi\) and \(\varphi'\) are equivalent if there exists an equivalence \(\varphi \rightarrow \varphi'\).

(3) An undirected \(S\)-wiring diagram is an equivalence class of undirected \(S\)-prewiring diagrams. If \(S\) is clear from the context, we will drop \(S\) and just say undirected wiring diagram.
(4) The class of undirected $S$-wiring diagrams with output box $Y$ and input boxes $\underline{X} = (X_1, \ldots, X_n)$ is denoted by

$$UWD(\underline{X}) \quad \text{or} \quad UWD(Y_{X_1, \ldots, X_n}).$$

(7.1.4.1)

The class of all undirected $S$-wiring diagrams is denoted by $UWD$. If we want to emphasize the class $S$, we will write $UWD_S$.

**Remark 7.1.5.** Consider Def. 7.1.2 and 7.1.4

1. If $S = \{\ast\}$, a one-point set, then what we call an undirected $\{\ast\}$-wiring diagram is called a *singly-typed wiring diagram* in [Spi13] (Example 2.1.7).

2. If $S = \text{Set}$, the collection of sets, then what we call an undirected Set-wiring diagram is called a *typed wiring diagram* in [Spi13] (Example 4.1.1).

3. Cospans (7.1.2.2) are also used in other work about processes and networks. For example, cospans in a category, rather than just $\text{Fin}_S$, are used in [Fon13]. That setting is then used in [BF15, BFP16] to study passive linear networks and Markov processes.

4. In the book [Spi14] p.464 (but not in [Spi13] Example 2.1.7), Spivak’s definition of an undirected $\{\ast\}$-wiring diagram is slightly different from ours. More precisely, Spivak insisted that the maps $(f, g)$ in the cospan (7.1.2.2) be *jointly surjective*, meaning that there are no wasted cables. However, undirected wiring diagrams whose structure maps $(f, g)$ are jointly surjective are not closed under the operad structure in $UWD$, to be defined in Section 7.3. In Example 7.3.8 and Section 8.3 we will illustrate that the operadic composition of undirected wiring diagrams without wasted cables can have wasted cables. In other words, while individual undirected wiring diagrams may have no wasted cables, the operadic composition can actually create wasted cables. So there is no such thing as the operad of undirected wiring diagrams without wasted cables. In [Fon15] (Def. 3.1) Fong also used cospans, but did not insist that they be jointly surjective in any way.

**Convention 7.1.6.** To simplify the presentation, we usually suppress the difference between an undirected prewiring diagram and an undirected wiring diagram. Each undirected wiring diagram $\varphi = (X, Y, C, f, g)$ has a unique representative in which:

- each cable is an element in $S$;
- the value assignment $v : C \to S$ sends each cable to itself.

Unless otherwise specified, we will always use this representative of an undirected wiring diagram.
Example 7.1.7. Suppose $S$ is any class. Consider the undirected wiring diagram $\varphi \in \text{UWD}_{X_1, X_2}$ defined as follows.

- The input boxes are $X_1 = \{x_1, x_2, x_3, x_4, x_5, x_6\}$ and $X_2 = \{x^1, x^2\} \in \text{Fin}_S$.
- The output box is $Y = \{y_1, y_2, y_3, y_4, y_5, y_6\} \in \text{Fin}_S$.
- The set of cables is $C = \{c_1, c_2, c_3, c_4, c_5, c_6, c_7\} \in \text{Fin}_S$.

Their value assignments satisfied the following conditions:

- $v(c_1) = v(y_1) = v(y_2) \in S$.
- $v(c_2) = v(x_1) = v(y_3) \in S$.
- $v(c_3) = v(x_2) = v(x_3) = v(x^1) = v(y_4) = v(y_5) \in S$.
- $v(c_4) \in S$ is arbitrary.
- $v(c_5) = v(y_6) \in S$.
- $v(c_6) = v(x_4) = v(x_5) = v(x^2) \in S$.
- $v(c_7) = v(x_6) \in S$.

The input and the output soldering functions

$$X_1 \cup X_2 \xrightarrow{f} C \xleftarrow{g} Y$$

are defined as follows:

- $c_1 = g(y_1) = g(y_2)$ is a $(0, 2)$-cable.
- $c_2 = f(x_1) = g(y_3)$ is a $(1, 1)$-cable.
- $c_3 = f(x_2) = f(x_3) = f(x^1) = g(y_4) = g(y_5)$ is a $(3, 2)$-cable.
- $c_4$ is a $(0, 0)$-cable, i.e., a wasted cable.
- $c_5 = g(y_6)$ is a $(0, 1)$-cable.
- $c_6 = f(x_4) = f(x_5) = f(x^2)$ is a $(3, 0)$-cable.
- $c_7 = f(x_6)$ is a $(1, 0)$-cable.
Graphically we represent this undirected wiring diagram \( \varphi \in \text{UWD}(x_1, x_2) \) as follows.

The input boxes \( X_1 = \{x_1, \ldots, x_6\} \) and \( X_2 = \{x^1, x^2\} \) are drawn as the smaller boxes inside. The output box \( Y = \{y_1, \ldots, y_6\} \) is drawn as the outer rectangle. Each element within each box is drawn along the boundary, either just inside (as in \( X_1 \) and \( X_2 \)) or just outside (as in \( Y \)). Note that no orientation is attached to the sides of these squares and rectangles. For example, we could have drawn \( y_6 \in Y \) on the bottom side of the outer rectangle. Each cable \( c_i \in C \) is drawn as a small gray disk, which is not to be confused with a delay node in a wiring diagram (such as \( d \) in \( (2.2.18.1) \)). The soldering functions \( f \) and \( g \) tell us how to connect the wires in \( X = X_1 \sqcup X_2 \) and \( Y \) to the cables. We will revisit this example in Example 9.1.2 below.

### 7.2. Pushouts

The operadic composition on the collection of undirected wiring diagrams \( \text{UWD} \) (Def. 7.1.4) involves the basic categorical concept of a pushout, which we recall in this section. The reader may consult [Awodey 2010] (5.6) and [MacLane 1998] (p.65-66) for more discussion of pushouts. Roughly speaking, a pushout is a way of summing two objects with some identification. We will only use the following definition when the category is \( \text{Fin}_5 \) (Def. 2.2.6), so the reader may simply take the category \( C \) below to be \( \text{Fin}_5 \) and objects and maps to be those in \( \text{Fin}_5 \).

**Definition 7.2.1.** Suppose \( C \) is a category (Def. 2.2.2), and

\[
\begin{array}{c}
Y \xleftarrow{f} X \xrightarrow{g} Z
\end{array}
\]

is a diagram in \( C \). Then a **pushout** of this diagram is a tuple \((W, \alpha, \beta)\) consisting of an object \( W \in C \) and maps \( \alpha : Y \rightarrow W \) and \( \beta : Z \rightarrow W \) in \( C \) such that the following two conditions hold.

1. The square

\[
\begin{array}{c}
\begin{array}{ccc}
X & \xrightarrow{g} & Z \\
\downarrow{f} & & \downarrow{\beta} \\
Y & \xrightarrow{\alpha} & W
\end{array}
\end{array}
\]

in \( C \) is commutative, i.e., \( \alpha f = \beta g \).
(2) Suppose \((W', \alpha', \beta')\) is another such tuple, i.e., \(\alpha' f = \beta' g\). Then there exists a unique map \(h : W \rightarrow W'\) in \(C\) such that the diagram

\[
\begin{array}{ccc}
X & \xrightarrow{g} & Z \\
\downarrow{f} & & \downarrow{\beta} \\
Y & \xrightarrow{a} & W \\
\downarrow{\alpha'} & & \downarrow{h} \\
W' & & W'
\end{array}
\]

in \(C\) is commutative, i.e., \(\alpha' = h \alpha\) and \(\beta' = h \beta\).

If a pushout exists, then by definition it is unique up to unique isomorphisms. In a general category, a pushout may not exist for a diagram of the form \((\ref{eq:7.2.1.1})\). Even if it exists, it may be difficult to describe. Luckily, for \(S\)-finite sets (Def. \(\ref{def:2.2.6}\)), pushouts always exist and are easy to describe, as the following observation shows.

**Proposition 7.2.2.** In the category \(\text{Fin}_S\) of \(S\)-finite sets, each diagram of the form \((\ref{eq:7.2.1.1})\) has a pushout given by the quotient

\[
W = \frac{Y \sqcup Z}{\{f(x) = g(x) : x \in X\}} \quad \text{(7.2.2.1)}
\]

taken in \(\text{Fin}_S\).

**Proof.** The maps \(\alpha : Y \rightarrow W\) and \(\beta : Z \rightarrow W\) are the obvious maps, each being the inclusion into \(Y \sqcup Z\) followed by the quotient map to \(W\). Then the tuple \((W, \alpha, \beta)\) has the required universal property of a pushout in \(\text{Fin}_S\). \(\square\)

**Example 7.2.3.** A commutative square with opposite identity maps is a pushout square. In other words, a pushout of the diagram

\[
\begin{array}{ccc}
X & \xrightarrow{=} & X \\
\downarrow{g} & & \downarrow{g} \\
Z & & Z
\end{array}
\]

in any category is given by the commutative square

\[
\begin{array}{ccc}
X & \xrightarrow{g} & Z \\
\downarrow{=} & & \downarrow{=} \\
X & \xrightarrow{g} & Z
\end{array}
\]

as can be checked by a direct inspection.
7.3. Operad Structure

Fix a class $S$. In this section we define the $\text{Fin}_S$-colored operad structure (Def. 7.1.10) on the collection of undirected wiring diagrams $\text{UWD}$ (Def. 7.1.4). When $S$ is either $\{\ast\}$ or the collection of sets, this operad structure on $\text{UWD}$ was first introduced in [Spi13] using the structure map $\gamma$ (2.1.3.2).

**Definition 7.3.1 (Equivariance in $\text{UWD}$).** Suppose $Y \in \text{Fin}_S$, $X = (X_1, \ldots, X_n)$ is a $\text{Fin}_S$-profile of length $n$, and $\sigma \in \Sigma_n$ is a permutation. Define the function

$$UWD(Y_{X_1, \ldots, X_n}) \cong UWD(Y_{X_{\sigma(1)}, \ldots, X_{\sigma(n)}})$$

by sending $\phi = (C, f, g) \in UWD(Y_{X_1, \ldots, X_n})$ to $\phi = (C, f, g) \in UWD(Y_{X_{\sigma(1)}, \ldots, X_{\sigma(n)}})$, using the fact that $\prod_{i=1}^n X_i = \prod_{i=1}^n X_{\sigma(i)}$.

In other words, the equivariant structure in $\text{UWD}$ simply relabels the input boxes.

Next we define the colored units in $\text{UWD}$. The $Y$-colored unit in $\text{UWD}$, for $Y \in \text{Fin}_S$, may be depicted as follows.

![Diagram](image)

**Definition 7.3.2 (Units in $\text{UWD}$).** For each $Y \in \text{Fin}_S$, the $Y$-colored unit is defined as the undirected wiring diagram

$$1_Y = \left( Y \xrightarrow{=+} Y \xleftarrow{=} Y \right) \in UWD(Y).$$

**Motivation 7.3.3.** Next we define the $\circ_i$-composition in $\text{UWD}$. The operadic composition $\phi \circ_i \psi$ can be visualized in the following picture.

![Diagram](image)

Intuitively, to form the operadic composition $\phi \circ_i \psi$ in $\text{UWD}$, we replace the $i$th input box $X_i$ in $\phi$ by the input boxes in $\psi$. The set of cables in $\psi$ is added to the
set of cables in $\varphi$, with appropriate identification from the input and the output soldering functions in $\varphi$ and $\psi$.

The following notation will be useful in the definition of the $\circ_i$-composition.

**Notation 7.3.4.** Suppose $X = (X_1, \ldots, X_n)$ is a Fin$_S$-profile.

1. Write $X = X_1 \cup \cdots \cup X_n \in$ Fin$_S$.
2. For integers $i$ and $j$, define
   
   $$X_{[i,j]} = \begin{cases} 
   X_{i} \cup \cdots \cup X_{j} & \text{if } 1 \leq i \leq j \leq n; \\
   \emptyset & \text{otherwise.} 
   \end{cases}$$

**Definition 7.3.5** ($\circ_i$-Composition in UWD). Suppose:

- $\varphi = \{ X \xrightarrow{f_\varphi} C_\varphi \xleftarrow{g_\varphi} Y \} \in$ UWD$^{(X)}_{(Y)}$ with $X = (X_1, \ldots, X_n)$, $n \geq 1$, and $1 \leq i \leq n$;
- $\psi = \{ W \xrightarrow{f_\psi} C_\psi \xleftarrow{g_\psi} X_i \} \in$ UWD$^{(X)}_{(W)}$ with $|W| = m \geq 0$.

Define the undirected wiring diagram

$$\varphi \circ_i \psi = (C, f, g) \in$ UWD$^{(X)}_{(Y)}$$

as the cospan

$$\begin{array}{c}
X_1 \cup \cdots \cup X_n \\
\downarrow f_\varphi \\
C_\varphi \\
\downarrow g_\psi \\
Y
\end{array} \xleftarrow{(\text{Id}, f_\psi, \text{Id})} \xrightarrow{(\text{Id}, g_\varphi, \text{Id})}

\begin{array}{c}
\uparrow \text{pushout} \\
X_{[1,i-1]} \cup W \cup X_{[i+1,n]} \\
\downarrow f
\end{array} \xrightarrow{(\text{Id}, f_\psi, \text{Id})} \xleftarrow{(\text{Id}, g_\varphi, \text{Id})}

\begin{array}{c}
X_{[1,i-1]} \cup C_\psi \cup X_{[i+1,n]} \\
\downarrow f
\end{array}$$

in Fin$_S$. Here:

- The square is a pushout in Fin$_S$, which always exists by Prop. **7.2.2**
- The $S$-finite sets $W$, $X_{[1,i-1]}$, and $X_{[i+1,n]}$ are as in Notation **7.3.4**
- The Fin$_S$-profile

$$X \circ_i W = (X_1, \ldots, X_{i-1}, W, X_{i+1}, \ldots, X_n)$$

is as in **2.1.10.2**.
The map $f$ is the bottom horizontal composition, and the map $g$ is the right vertical composition.

In the following observation, we describe the undirected wiring diagram $\varphi \circ_i \psi$ more explicitly.

**Proposition 7.3.6.** Consider the diagram (7.3.5.1).

1. A choice of a pushout $C$ is the quotient
   \[
   C = \frac{C_\varphi \sqcup C_\psi}{\{f_\varphi(x) = g_\psi(x) : x \in X_i\}}
   \] (7.3.6.1)
   in $\text{Fin}_S$. The following statements use this choice of $C$.

2. The maps $C_\varphi \to C$ and $C_\psi \to C$ are the obvious maps, each being the inclusion into $C_\varphi \sqcup C_\psi$ followed by the quotient map to $C$.

3. In the map $f$ and in the horizontal unnamed map, for $j \neq i$, the map $X_j \to C$ is the composition
   \[
   X_j \xrightarrow{f_\varphi} C_\varphi \xrightarrow{\gamma} C.
   \]

4. On $W$ the map $f$ is the composition
   \[
   W \xrightarrow{f_\varphi} C_\psi \xrightarrow{\gamma} C.
   \]

**Proof.** A direct inspection shows that the first three statements indeed describe a pushout of the square in the diagram (7.3.5.1). The last assertion follows from the definition of $f$ as the bottom horizontal composition. \qed

**Remark 7.3.7.** Consider Def. 7.3.5.

1. Pushouts are unique up to unique isomorphisms. Since undirected wiring diagrams are defined as equivalence classes of undirected preswiring diagrams (Def. 7.1.4), the undirected wiring diagram $\varphi \circ_i \psi$ is well-defined.

2. In [Spi13] $S$ was taken to be either the one-point set or the collection of sets. The operadic composition in $\text{UWD}$ was defined in terms of the operadic composition $\gamma$ (2.1.3.2). By Prop. 2.1.12 the two descriptions—i.e., the one in [Spi13] and Def. 7.3.5—are equivalent.

Recall from Def. 7.1.2 that a wasted cable in an undirected wiring diagram is a cable that is not in the image of the input and the output soldering functions.

**Example 7.3.8.** In this example, we observe that wasted cables can be created by the $\circ_i$-composition, even if the original undirected wiring diagrams have no wasted cables. Suppose:
7.3. Operad Structure

* S = \{∗\} and X = \{x_1, x_2\} ∈ Fin is a two-element set.
* \(\varphi = \{ X \rightarrow \{∗\} \leftarrow \emptyset \} \in \text{UWD}(^S_X)\).
* \(\psi = \{ \emptyset \rightarrow X \leftarrow X \} \in \text{UWD}(^X_\emptyset)\).

Note that neither \(\varphi\) nor \(\psi\) has a wasted cable. On the other hand, the undirected wiring diagram \(\varphi \circ_1 \psi \in \text{UWD}(^S_\emptyset)\) is the cospan

\[
\begin{array}{c}
\emptyset \\
\downarrow
\end{array}
\begin{array}{c}
X \\
\downarrow
\end{array}
\begin{array}{c}
\{∗\} \\
\downarrow
\end{array}
\]

in Fin, in which the square is a pushout by Example 7.2.3. The following picture gives a visualization of this \(\circ_1\)-composition.

In particular, the unique cable in \(\varphi \circ_1 \psi\) is a wasted cable. This example illustrates that the \(\circ_i\)-composition of two undirected wiring diagrams without wasted cables may have wasted cables, which we mentioned in Remark 7.1.5. We will revisit this example in Section 8.3 and Example 10.1.5 below.

We now prove that the collection UWD of undirected wiring diagrams is a \(\text{Fin}_S\)-colored operad in the sense of Def. 2.1.10.

**Lemma 7.3.9.** The \(\circ_i\)-composition in Def. 7.3.5 satisfies the left unity axiom (2.1.10.5), the right unity axiom (2.1.10.6), and the equivariance axiom (2.1.10.7).

**Proof.** The equivariance axiom holds because the equivariant structure (7.3.1) simply relabels the input boxes. The unity axioms follow from the definitions of the colored units in UWD (7.3.2.1) and Example 72.3 \(\square\)

**Motivation 7.3.10.** The horizontal associativity axiom in UWD may be visualized as follows.
To keep the picture simple, we omitted drawing the wires and the cables. Note that this is basically the undirected version of the picture (2.3.7.1).

**Lemma 7.3.11.** The $\circ_i$-composition in Def. 7.3.5 satisfies the horizontal associativity axiom (2.1.10.3).

**Proof.** Suppose:

- $\varphi = (\mathcal{C}_\varphi, f_\varphi, g_\varphi) \in \text{UWD}(Y) \text{ with } |Y| = n \geq 2 \text{ and } 1 \leq i < j \leq n$;
- $\psi = (\mathcal{C}_\psi, f_\psi, g_\psi) \in \text{UWD}(Y) \text{ with } |Y| = l$;
- $\zeta = (\mathcal{C}_\zeta, f_\zeta, g_\zeta) \in \text{UWD}(Y) \text{ with } |X| = m$.

We must show that

$$((\varphi \circ_j \zeta) \circ_i \psi) = (\varphi \circ_i \psi) \circ_{i+1} \zeta \in \text{UWD}(Y, Z, W). \quad (7.3.11.1)$$

Consider the undirected wiring diagram

$$(\mathcal{C}, f, g) \in \text{UWD}(Y, Z, W)$$

given by the cospan

$$Y_{[1, i-1]} \sqcup W \sqcup Y_{[i+1, j-1]} \sqcup X \sqcup Y_{[j+1, n]} \xrightarrow{f} C \xleftarrow{g} Z$$

in $\text{Fin}_S$, where Notation 7.3.4 was used. In this cospan:

- The set of cables is the quotient
  $$C = \frac{C_\varphi \sqcup C_\psi \sqcup C_\zeta}{\{f_\varphi(y_i) = g_\varphi(y_i), f_\varphi(y_j) = g_\zeta(y_j) : y_i \in Y_i, y_j \in Y_j\}}.$$
- The output soldering function $g$ is the composition $Z \xrightarrow{g_\varphi} C_\varphi \xrightarrow{C_\varphi} C$.
- For the input soldering function $f$: 

7.3. Operad Structure

- The restriction to $Y_k$ is the composition $Y_k \xrightarrow{f \varphi} C \xrightarrow{\varphi} C$ for $k \neq i, j$.
- The restriction to $W$ is the composition $W \xrightarrow{f \psi} C \xrightarrow{\psi} C$.
- The restriction to $X$ is the composition $X \xrightarrow{f \zeta} C \xrightarrow{\zeta} C$.

Using the description of $\circ_i$ in Prop. 7.3.6, a direct inspection reveals that both sides of (7.3.11.1) are equal to $(C, f, g)$.

**Motivation 7.3.12.** The vertical associativity axiom in UWD may be visualized as follows.

As before, to keep the picture simple, we did not draw the wires and the cables. Note that this is basically the undirected version of the picture (2.3.9.1).

**Lemma 7.3.13.** The $\circ_i$-composition in Def. 7.3.5 satisfies the vertical associativity axiom (2.1.10.4).

**Proof.** Suppose:

- $\varphi = (C, f, g) \in \text{UWD}(Z)$ with $|Y| = n \geq 1$ and $1 \leq i \leq n$;
- $\psi = (C, f, g) \in \text{UWD}(Z)$ with $|X| = m \geq 1$ and $1 \leq j \leq m$;
- $\zeta = (C, f, g) \in \text{UWD}(Z)$ with $|W| = l$.

We must show that

$$(\varphi \circ_i \psi) \circ_{i-1+j} \zeta = \varphi \circ_i (\psi \circ_j \zeta) \in \text{UWD}(Z),$$

(7.3.13.1)

Consider the undirected wiring diagram

$$(C, f, g) \in \text{UWD}(Z).$$
given by the cospan

\[
Y_{[i-1, j-1]} \sqcup X_{[j+1, m]} \sqcup W X_{(i+1, n]} \xrightarrow{f} C \leftarrow \xrightarrow{g} Z
\]

in \( \text{Fin}_S \), where Notation [7.3.4] was used. In this cospan:

- The set of cables is the quotient

\[
C = \frac{C_\varphi \sqcup C_\psi \sqcup C_\zeta}{\{ f_\varphi(y) = g_\psi(y), f_\psi(x) = g_\zeta(x) : y \in Y_i, x \in X_j \}}.
\]

- The output soldering function \( g \) is the composition \( Z \xrightarrow{g_\varphi} C_\varphi \longrightarrow C \).

- For the input soldering function \( f \):
  - The restriction to \( Y_l \) is the composition \( Y_l \xrightarrow{f_\varphi} C_\varphi \longrightarrow C \) for \( l \neq i \).
  - The restriction to \( X_k \) is the composition \( X_k \xrightarrow{f_\psi} C_\psi \longrightarrow C \) for \( k \neq j \).
  - The restriction to \( W \) is the composition \( W \xrightarrow{f_\zeta} C_\zeta \longrightarrow C \).

Using the description of \( o_i \) in Prop. [7.3.6] a direct inspection reveals that both sides of (7.3.13.1) are equal to \((C, f, g)\). \( \square \)

**Theorem 7.3.14.** For any class \( S \), when equipped with the structure in Def. [7.3.1–7.3.5], UWD in Def. [7.1.4] is a \( \text{Fin}_S \)-colored operad, called the operad of undirected wiring diagrams.

**Proof.** In view of Def. [2.1.10], this follows from Lemmas [7.3.9, 7.3.11] and [7.3.13] \( \square \)

**Example 7.3.15.** Consider Theorem 7.3.14.

1. If \( S = \{ \ast \} \), a one-point set, then our \( \text{Fin} \)-colored operad UWD is called the operad of singly-typed wiring diagrams in \( \text{S pla}_1 \) (Example 2.1.7).

2. If \( S = \text{Set} \), the collection of sets, then our \( \text{Fin}_{\text{Set}} \)-colored operad UWD is called the operad of typed wiring diagrams in \( \text{S pla}_1 \) (Example 4.1.1).

We defined the operad UWD in terms of the \( o_i \)-compositions (Def. [7.3.5]). The following observation expresses the operad UWD in terms of the operadic composition \( \gamma \) (2.1.3.2). In \( \text{S pla}_1 \) the operad structure on undirected wiring diagrams was actually defined in terms of \( \gamma \).

**Proposition 7.3.16.** Suppose:

- \( \varphi = (C_\varphi, f_\varphi, g_\varphi) \in \text{UWD}(\underline{Y}) \) with \( \underline{X} = (X_1, \ldots, X_n) \) for some \( n \geq 1 \) and \( X = X_1 \sqcup \cdots \sqcup X_n \).
For each $1 \leq i \leq n$, $\psi_i = (C_i, f_i, g_i) \in UWD(\gamma_W)$ with $W_i = (W_{i,1}, \ldots, W_{i,k_i})$ for some $k_i \geq 0$.

$W = (W_1, \ldots, W_n)$, $W_i = W_{i,1} \cup \cdots \cup W_{i,k_i}$, and $W = \bigcup_{1 \leq i \leq n} W_i$.

Then $\gamma(\varphi; \psi_1, \ldots, \psi_n) = (C, f, g) \in UWD(\gamma_W)$ is given by the cospan

![Diagram](7.3.16.1)

in $\text{Fin}_S$, in which the square is a pushout. In this diagram:

1. $C$ is the quotient $C = \frac{C_\varphi \sqcup C_1 \sqcup \cdots \sqcup C_n}{\{f_\varphi(x) = g_i(x) : x \in X_i, 1 \leq i \leq n\}}$ in $\text{Fin}_S$.

2. The maps $C_\varphi \longrightarrow C$ and $C_i \longrightarrow C$ are the obvious maps, each being an inclusion followed by a quotient map to $C$.

3. The restriction of $f$ to $W_i$ is the composition of $f_i : W_i \longrightarrow C_i$ and $C_i \longrightarrow C$.

**Proof.** This follows from (i) the correspondence (2.1.12.1) between $\gamma$ and the $\circ_i$-compositions and (ii) the description of $\circ_i$ given in Proposition 7.3.6.

7.4. Summary of Chapter

1. An undirected $S$-wiring diagram has a finite number of input boxes, an output box, an $S$-finite set of cables, an input soldering function, and an output soldering function.

2. For each class $S$, the collection of $S$-wiring diagrams $UWD$ is a $\text{Fin}_S$-colored operad.
Generators and Relations

Fix a class $S$, and consider the $\text{Fin}_5$-colored operad $UWD$ of undirected wiring diagrams (Theorem 7.3.14). The purpose of this chapter is to describe a finite number of undirected wiring diagrams that we will later show to be sufficient to describe the entire operad $UWD$. One may also regard this chapter as consisting of a long list of examples of undirected wiring diagrams.

In Section 8.1 we describe 6 undirected wiring diagrams, called the generating undirected wiring diagrams. Later we will show that they generate the operad $UWD$ of undirected wiring diagrams. This means that every undirected wiring diagram can be obtained from finitely many generating undirected wiring diagrams via iterated operadic compositions. For now one may think of the generating undirected wiring diagrams as examples of undirected wiring diagrams.

In Section 8.2 we describe 17 elementary relations among the generating undirected wiring diagrams. Later we will show that these elementary relations together with the operad associativity and unity axioms—(2.1.10.3), (2.1.10.4), (2.1.10.5), and (2.1.10.6)—for the generating undirected wiring diagrams generate all the relations in the operad $UWD$ of undirected wiring diagrams. In other words, suppose an arbitrary undirected wiring diagram can be built in two ways using the generating undirected wiring diagrams. Then there exists a finite sequence of steps connecting them in which each step is given by one of the 17 elementary relations or an operad associativity/unity axiom for the generating undirected wiring diagrams. For now one may think of the elementary relations as examples of the operadic composition in the operad $UWD$. 

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8.1. Generating Undirected Wiring Diagrams

Recall the definition of an undirected wiring diagram (Def. 7.1.4). In this section, we introduce 6 undirected wiring diagrams, called the generating undirected wiring diagrams. They will be used in later chapters to give a finite presentation for the operad UWD of undirected wiring diagrams. The undirected wiring diagrams in this section all have directed analogues in Section 3.1.

The following undirected wiring diagram is an undirected analogue of the empty wiring diagram (Def. 3.1.1).

Definition 8.1.1. Define the empty cell

\[ e = \left( \emptyset \longrightarrow \emptyset \leftarrow \emptyset \right) \in \text{UWD}(\emptyset), \]

where \( \emptyset \) is the empty \( S \)-finite set. Note that the empty cell is a 0-ary element in \( \text{UWD} \).

Next we define the undirected wiring diagram

with no input boxes and whose unique cable is a \((0,1)\)-cable. This is an undirected analogue of a 1-wasted wire (Def. 3.1.8). To simplify the typography, we will often write \( x \) for the one-point set \( \{x\} \).

Definition 8.1.2. Suppose \( * \in \text{Fin}_S \) is a one-element \( S \)-finite set. Define the 1-output wire

\[ \omega_* = \left( \emptyset \longrightarrow * \leftarrow * \right) \in \text{UWD}(\{\} \).

Note that a 1-output wire is a 0-ary element in \( \text{UWD} \).

Next we define the undirected wiring diagram

with 1 input box and whose cables are all \((1,1)\)-cables. This is an undirected analogue of a name change (Def. 3.1.3).

Definition 8.1.3. Suppose \( f : X \longrightarrow Y \in \text{Fin}_S \) is a bijection. Define the undirected name change

\[ \tau_f = \left( X \xrightarrow{f} Y \xleftarrow{=} Y \right) \in \text{UWD}(\{\}). \]
If the bijection \( f \) is clear from the context, then we write \( \tau_f \) as \( \tau_{X,Y} \) or just \( \tau \). If there is no danger of confusion, then we will call \( \tau_f \) a name change.

Next we define the undirected wiring diagram

![Diagram](https://via.placeholder.com/150)

with 2 input boxes and whose cables are all \((1,1)\)-cables. This is an undirected analogue of a 2-cell (Def. 8.1.4).

**Definition 8.1.4.** Suppose \( X, Y \in \text{Fin}_S \) and \( X \uplus Y \) is their coproduct. Define the undirected 2-cell

\[
\theta_{(X,Y)} = \left( \begin{array}{c}
X \uplus Y \\
\rightarrow
\end{array} \right) \in \text{UWD}(X \uplus Y).
\]

If there is no danger of confusion, then we will call it a 2-cell.

Next we define the undirected wiring diagram

![Diagram](https://via.placeholder.com/150)

with a \((2,0)\)-cable, all other cables being \((1,1)\)-cables. This is an undirected analogue of a 1-loop (Def. 8.1.5).

**Definition 8.1.5.** Suppose:

- \( X \in \text{Fin}_S \), and \( x_+, x_- \in X \) are two distinct elements with \( v(x_+) = v(x_-) \in S \).
- \( X \setminus x_+ \in \text{Fin}_S \) is obtained from \( X \) by removing \( x_+ \) and \( x_- \).
- \( X/(x_+ = x_-) \in \text{Fin}_S \) is the quotient of \( X \) with \( x_+ \) and \( x_- \) identified.

Define the loop

\[
\lambda_{(X,x_+)} = \left( \begin{array}{c}
X \xrightarrow{\text{projection}} X \\
\xrightarrow{(x_+ = x_-)} \includegraphics{inclusion} X \setminus x_+ \\
\end{array} \right) \in \text{UWD}(X/(x_+ = x_-)).
\]

Next we define the undirected wiring diagram

![Diagram](https://via.placeholder.com/150)
with a (1,2)-cable, all other cables being (1,1)-cables. This is an undirected analogue of an out-split (Def. 3.1.7).

Definition 8.1.6. Suppose:
- \( X \in \text{Fin}_S \), and \( x_1, x_2 \) are two distinct elements in \( X \) with \( v(x_1) = v(x_2) \in S \).
- \( X' \in \text{Fin}_S \), and \( x \in X' \) such that \( v(x) = v(x_1) \) and that \( X' \setminus \{x\} = X \setminus \{x_1, x_2\} \).

Define the split
\[
\sigma^{(X,x_1,x_2)} = \left( \begin{array}{c}
\xymatrix{X' \ar[r] & X'} \\
X \ar@{->}[l]
\end{array} \right) \in \text{UWD}(\frac{X}{X'})
\]
in which the output soldering function \( X \rightarrow X' \) sends \( x_1, x_2 \in X \) to \( x \in X' \) and is the identity function on \( X \setminus \{x_1, x_2\} \).

Definition 8.1.7. The 6 undirected wiring diagrams in Def. 8.1.1–8.1.6 will be referred to as generating undirected wiring diagrams. If the context is clear, we will simply call them generators.

Remark 8.1.8. Among the generating undirected wiring diagrams:

1. None has a wasted cable (Def. 8.1.2). As we will see in Section 8.3, wasted cables can be created by the generators.

2. The empty cell \( \epsilon \) (Def. 8.1.1) and a 1-output wire \( \omega_\ast \) (Def. 8.1.2) are 0-ary elements in UWD.

3. A name change \( \tau \) (Def. 8.1.3), a loop \( \lambda^{(x,x)} \) (Def. 8.1.5), and a split \( \sigma^{(X,x_1^\pm,x_2^\pm)} \) (Def. 8.1.6) are unary elements in UWD.

4. A 2-cell \( \theta^{(X,Y)} \) (Def. 8.1.4) is a binary element in UWD.

8.2. Elementary Relations

The purpose of this section is to introduce 17 elementary relations among the generating undirected wiring diagrams (Def. 8.1.7). Each elementary relation is proved using Prop. 7.3.6 and Example 7.2.3 and by a simple inspection of the relevant definitions of the generating undirected wiring diagrams and operadic compositions. Each proof is similar to Example 7.3.8 and the proofs of Lemma 7.3.11 and Lemma 7.3.13. Therefore, we will omit the proofs, providing a picture instead in most cases. Some, but not all, of the following relations have directed analogues in Section 3.3.

Recall the operadic composition in the \( \text{Fin}_S \)-colored operad UWD (Def. 7.3.5) and Notation 3.3.1 for (iterated) \( \circ \). The first five relations are about name changes (Def. 8.1.3). The first one says that two consecutive name changes can be composed down into one name change.

Proposition 8.2.1. Suppose:
8.2. Elementary Relations

- \( f : X \longrightarrow Y \) and \( g : Y \longrightarrow Z \in \text{Fin}_S \) are bijections.
- \( \tau_f \in \text{UWD}(X) \), \( \tau_g \in \text{UWD}(Y) \), and \( \tau_{gf} \in \text{UWD}(Z) \) are the corresponding name changes.

Then

\[ \tau_g \circ \tau_f = \tau_{gf} \in \text{UWD}(Z). \] (8.2.1.1)

The next relation says that a name change of a 1-output wire (Def. 8.1.2) is again a 1-output wire.

**Proposition 8.2.2.** Suppose:

- \( X = \{ x \} \) and \( Y = \{ y \} \) are two 1-element \( S \)-finite sets with \( v(x) = v(y) \in S \).
- \( \omega_x \in \text{UWD}(X) \) and \( \omega_y \in \text{UWD}(Y) \) are the corresponding 1-output wires.
- \( \tau_{X,Y} \in \text{UWD}(Y) \) is the name change corresponding to the bijection \( X \longrightarrow Y \in \text{Fin}_S \).

Then

\[ \tau_{X,Y} \circ \omega_x = \omega_y \in \text{UWD}(Y). \] (8.2.2.1)

The next relation says that name changes inside a 2-cell (Def. 8.1.3) can be rewritten as a name change of a 2-cell.

**Proposition 8.2.3.** Suppose:

- \( f_1 : X_1 \longrightarrow Y_1 \) and \( f_2 : X_2 \longrightarrow Y_2 \in \text{Fin}_S \) are bijections.
- \( f_1 \cup f_2 : X_1 \cup X_2 \longrightarrow Y_1 \cup Y_2 \in \text{Fin}_S \) is their coproduct.
- \( \tau_{f_1} \in \text{UWD}(X_1), \tau_{f_2} \in \text{UWD}(Y_2), \) and \( \tau_{f_1 \cup f_2} \in \text{UWD}(X_1 \cup X_2) \) are the corresponding name changes.
- \( \theta_{(X_1,x_2)} \in \text{UWD}(X_1, X_2) \) and \( \theta_{(Y_1,y_2)} \in \text{UWD}(Y_1, Y_2) \) are 2-cells.

Then

\[ \left( \theta_{(Y_1,y_2)} \circ_1 \tau_{f_1} \right) \circ_2 \tau_{f_2} = \tau_{f_1 \cup f_2} \circ \theta_{(X_1,x_2)} \in \text{UWD}(X_1, X_2). \] (8.2.3.1)

The next relation says that a name change inside a loop (Def. 8.1.5) can be rewritten as a name change of a loop.

**Proposition 8.2.4.** Suppose:

- \( X \in \text{Fin}_S \), and \( x_+, x_- \in X \) are two distinct elements with \( v(x_+) = v(x_-) \in S \).
- \( f : X \longrightarrow Y \in \text{Fin}_S \) is a bijection with \( y_+ = f(x_+) \) and \( y_- = f(x_-) \).
- \( X \setminus x_\pm \in \text{Fin}_S \) and \( Y \setminus y_\pm \in \text{Fin}_S \) are obtained from \( X \) and \( Y \) by removing the indicated elements.
- \( f' : X \setminus x_\pm \longrightarrow Y \setminus y_\pm \) is the corresponding bijection.
• \( \tau_f \in \text{UWD}(\text{\( Y \to X \)}}) \) and \( \tau_{f'} \in \text{UWD}(\text{\( Y' \to X' \)}}) \) are name changes.

• \( \lambda_{(X,x_a)} \in \text{UWD}(\text{\( X' \to X \)}}) \) and \( \lambda_{(Y,y_a)} \in \text{UWD}(\text{\( Y' \to Y \)}}) \) are loops.

Then

\[
\lambda_{(Y,y_a)} \circ \tau_f = \tau_{f'} \circ \lambda_{(X,x_a)} \in \text{UWD}(\text{\( Y' \to X' \)}}). \tag{8.2.4.1}
\]

The next relation says that a name change inside a split (Def. 8.1.6) can be rewritten as a name change of a split.

**Proposition 8.2.5.** Suppose:

• \( X \in \text{Fin}_S \), and \( x_1, x_2 \) are two distinct elements in \( X \) with \( v(x_1) = v(x_2) \in S \).

• \( X' \in \text{Fin}_S \), and \( x \in X' \) such that \( v(x) = v(x_1) \) and that \( X' \setminus \{x\} = X \setminus \{x_1, x_2\} \).

• \( f : X \to Y \in \text{Fin}_S \) is a bijection with \( y_1 = f(x_1) \) and \( y_2 = f(x_2) \).

• \( Y' \in \text{Fin}_S \), and \( y \in Y' \) such that \( v(y) = v(y_1) \in S \) and that \( Y' \setminus \{y\} = Y \setminus \{y_1, y_2\} \).

• \( f' : X' \to Y' \in \text{Fin}_S \) is a bijection such that \( f'(x) = y \) and that its restriction to \( X' \setminus \{x\} = X \setminus \{x_1, x_2\} \) is equal to that of \( f \).

• \( \tau_f \in \text{UWD}(\text{\( X \)}}) \) and \( \tau_{f'} \in \text{UWD}(\text{\( X' \)}}) \) are name changes.

• \( \sigma_{(X,x_1,x_2)} \in \text{UWD}(\text{\( X \)}}) \) and \( \sigma_{(Y,y_1,y_2)} \in \text{UWD}(\text{\( Y \)}}) \) are splits.

Then

\[
\sigma_{(Y,y_1,y_2)} \circ \tau_{f'} = \tau_f \circ \sigma_{(X,x_1,x_2)} \in \text{UWD}(\text{\( Y \)}}). \tag{8.2.5.1}
\]

The following two relations involve 1-output wires in somewhat subtle ways. The next relation says that the undirected wiring diagram

![Diagram](image1)

with a \((1,0)\)-cable, all other cables being \((1,1)\)-cables, can be obtained from the generators as either one of the following two (iterated) operadic compositions.

![Diagram](image2)

As in Section 7.3, the gray boxes here indicate an operadic composition.
• On the left, a 1-output wire \( \omega_y \) is substituted into a 2-cell \( \theta_{(X,y)} \), which is then substituted into a loop \( \lambda_{(Y,x,y)} \).

• On the right, a split \( \sigma^{(Y,x,y)} \) is substituted into a loop \( \lambda_{(Y,x,y)} \).

**Proposition 8.2.6.** Suppose:

• \( Y \in \text{Fin}_S \), and \( x, y \in Y \) are distinct elements with \( v(x) = v(y) \in S \).

• \( X = Y \setminus y \in \text{Fin}_S \) is obtained from \( Y \) by removing \( y \).

• \( \omega_y \in \text{UWD}(Y) \) is the 1-output wire for \( y \).

• \( \theta_{(X,y)} \in \text{UWD}(X) \) is a 2-cell.

• \( \lambda_{(Y,x,y)} \in \text{UWD}(W) \) is a loop, where \( W = Y \setminus \{x, y\} = X \setminus x \).

• \( \sigma^{(Y,x,y)} \in \text{UWD}(Y) \) is a split.

Then

\[
\lambda_{(Y,x,y)} \circ \left( \theta_{(X,y)} \circ \omega_y \right) = \lambda_{(Y,x,y)} \circ \sigma^{(Y,x,y)} \in \text{UWD}(W).
\] (8.2.6.1)

The next relation says that the \( X \)-colored unit (Def. 7.3.2) can be obtained from the generators as the following iterated operadic composition.

More precisely, it says that the \( X \)-colored unit \( 1_X \) can be obtained by substituting a 1-output wire \( \omega_y \) into a 2-cell \( \theta_{(X,y)} \), then into a split \( \sigma^{(W,x,y)} \), and then into a loop \( \lambda_{(W,w,y)} \).

**Proposition 8.2.7.** Suppose:

• \( W \in \text{Fin}_S \), and \( w, x, y \) are distinct elements in \( W \) with \( v(w) = v(x) = v(y) \in S \).

• \( Y = W \setminus w \in \text{Fin}_S \) is obtained from \( W \) by removing \( w \).

• \( X = Y \setminus y \in \text{Fin}_S \) is obtained from \( Y \) by removing \( y \).

• \( \omega_y \in \text{UWD}(Y) \) is the 1-output wire for \( y \).

• \( \theta_{(X,y)} \in \text{UWD}(X) \) is a 2-cell.

• \( \sigma^{(W,x,y)} \in \text{UWD}(Y) \) is a split.

• \( \lambda_{(W,w,y)} \in \text{UWD}(X) \) is a loop.
Then
\[
\lambda_{(W, w, y)} \circ \sigma^{(W, x, w)} \circ \left( \theta_{(X, y)} \circ \omega_y \right) = \mathbbm{1}_X \in \text{UWD}^{(X)}_X,
\]
(8.2.7.1)
in which \( \mathbbm{1}_X \) is the \( X \)-colored unit (Def. 7.3.2).

The next five relations are about 2-cells (Def. 8.1.4). The following relation is the unity property of 2-cells.

**Proposition 8.2.8.** Suppose:

- \( \theta_{(X, \emptyset)} \in \text{UWD}^{(X)}_{(X, \emptyset)} \) is a 2-cell.
- \( \epsilon \in \text{UWD}^{(\emptyset)} \) is the empty cell (Def. 8.1.1).

Then
\[
\theta_{(X, \emptyset)} \circ_2 \epsilon = \mathbbm{1}_X \in \text{UWD}^{(X)}_X.
\]
(8.2.8.1)

The next relation is the associativity property of 2-cells. It gives two different ways to construct the following undirected wiring diagram using two 2-cells.

**Proposition 8.2.9.** Suppose:

- \( \theta_{(X_u Y, Z)} \in \text{UWD}^{(X_u Y, \emptyset)}_{(X_u Y, Z)} \) and \( \theta_{(X, Y)} \in \text{UWD}^{(X_u Y)}_{(X, Y)} \) are 2-cells.
- \( \theta_{(X_u Y, \emptyset)} \in \text{UWD}^{(X_u Y)}_{(X_u Y, \emptyset)} \) and \( \theta_{(Y, Z)} \in \text{UWD}^{(Y)}_{(Y, Z)} \) are 2-cells.

Then
\[
\theta_{(X_u Y, Z)} \circ_1 \theta_{(X, Y)} = \theta_{(X_u Y, \emptyset)} \circ_2 \theta_{(Y, Z)} \in \text{UWD}^{(X_u Y, \emptyset, Z)}_{(X_u Y, \emptyset, Z)}.
\]
(8.2.9.1)

The next relation is the commutativity property of 2-cells. It uses the equivariant structure (7.3.1) in UWD.

**Proposition 8.2.10.** Suppose:

- \( \theta_{X, Y} \in \text{UWD}^{(X_u Y)}_{(X, Y)} \) is a 2-cell.
- \( (1 \ 2) \in \Sigma_2 \) is the non-trivial permutation.

Then
\[
\theta_{(X, Y)} (1 \ 2) = \theta_{(Y, X)} \in \text{UWD}^{(Y_u X)}_{(Y, X)}.
\]
(8.2.10.1)

The next relation is the commutativity property between a 2-cell and a loop. It gives two different ways to construct the following undirected wiring diagram.
Proposition 8.2.11. Suppose:

- \( Y \in \text{Fin}_S \), and \( y_+ \), \( y_- \) are distinct elements in \( Y \) with \( v(y_+) = v(y_-) \in S \).
- \( Y' = Y \setminus y \pm \in \text{Fin}_S \) is obtained from \( Y \) by removing \( y_+ \) and \( y_- \).
- \( \lambda_{(Y,y \pm)} \in \text{UWD}(Y') \) is a loop.
- \( \theta_{(X,Y)} \in \text{UWD}(X,Y') \) and \( \theta_{(X,Y')} \in \text{UWD}(X,Y) \) are 2-cells for some \( X \in \text{Fin}_S \).
- \( \lambda_{(X \cup Y,y \pm)} \in \text{UWD}(X,Y') \) is a loop.

Then
\[
\theta_{(X,Y') \circ_2 \lambda_{(Y,y \pm)}} = \lambda_{(X \cup Y,y \pm)} \circ \theta_{(X,Y')} \in \text{UWD}(X,Y').
\] (8.2.11.1)

The next relation is the commutativity between a 2-cell and a split. It gives two different ways to construct the following undirected wiring diagram.

Proposition 8.2.12. Suppose:

- \( Y \in \text{Fin}_S \), and \( y_1 \), \( y_2 \) are distinct elements in \( Y \) with \( v(y_1) = v(y_2) \in S \).
- \( Y' \in \text{Fin}_S \), and \( y \in Y' \) such that \( v(y) = v(y_1) \) and that \( Y' \setminus \{y\} = Y \setminus \{y_1,y_2\} \).
- \( \sigma^{(Y,y_1,y_2)} \in \text{UWD}(Y') \) is a split.
- \( \theta_{(X,Y)} \in \text{UWD}(X,Y') \) and \( \theta_{(X,Y')} \in \text{UWD}(X,Y) \) are 2-cells for some \( X \in \text{Fin}_S \).
- \( \sigma^{(X \cup Y,y_1,y_2)} \in \text{UWD}(X,y_1,y_2) \) is a split.

Then
\[
\theta_{(X,Y)} \circ_2 \sigma^{(Y,y_1,y_2)} = \sigma^{(X \cup Y,y_1,y_2)} \circ \theta_{(X,Y')} \in \text{UWD}(X,Y').
\] (8.2.12.1)

The following four relations are about splits. The next relation is the commutativity property of splits. It gives two different ways to construct the following undirected wiring diagram using two splits.
Proposition 8.2.13. Suppose:

- \( X \in \text{Fin}_S \), and \( y_1, y_2, z_1, z_2 \) are distinct elements such that \( v(y_1) = v(y_2) \) and \( v(z_1) = v(z_2) \in S \).
- \( X' \in \text{Fin}_S \), and \( y \) and \( z \) are distinct elements in \( X' \) such that
  - \( v(y) = v(y_1) \) and \( v(z) = v(z_1) \);
  - \( X' \setminus \{y, z\} = X \setminus \{y_1, y_2, z_1, z_2\} \).
- \( Y = \left[ X' \setminus \{y\} \right] \cup \{y_1, y_2\} \) and \( Z = \left[ X' \setminus \{z\} \right] \cup \{z_1, z_2\} \in \text{Fin}_S \).
- \( \sigma^{(X,y_1,y_2)} \in \text{UWD}(Y) \) and \( \sigma^{(Z,z_1,z_2)} \in \text{UWD}(Z) \) are splits.
- \( \sigma^{(X,z_1,z_2)} \in \text{UWD}(X) \) and \( \sigma^{(Y,y_1,y_2)} \in \text{UWD}(Y) \) are splits.

Then

\[
\sigma^{(X,y_1,y_2)} \circ \sigma^{(Z,z_1,z_2)} = \sigma^{(X,z_1,z_2)} \circ \sigma^{(Y,y_1,y_2)} \in \text{UWD}(X).
\] (8.2.13.1)

The next relation is the associativity property of splits. It gives two different ways to construct the following undirected wiring diagram using two splits.

Proposition 8.2.14. Suppose:

- \( Y \in \text{Fin}_S \), and \( y_1, y_2, y_3 \) are distinct elements in \( Y \) with \( v(y_1) = v(y_2) = v(y_3) \in S \).
- \( X \in \text{Fin}_S \), and \( x \in X \) such that
  - \( v(x) = v(y_1) \);
  - \( X \setminus \{x\} = Y \setminus \{y_1, y_2, y_3\} \).
- \( Y_1 = Y/(y_1 = y_2) \in \text{Fin}_S \) is the quotient of \( Y \) with \( y_1 \) and \( y_2 \) identified, called \( y_{12} \in Y_1 \).
- \( Y_2 = Y/(y_2 = y_3) \in \text{Fin}_S \) is the quotient of \( Y \) with \( y_2 \) and \( y_3 \) identified, called \( y_{23} \in Y_2 \).
- \( \sigma^{(Y,y_1,y_2)} \in \text{UWD}(Y) \) and \( \sigma^{(Y_1,y_{12},y_3)} \in \text{UWD}(Y_1) \) are splits.
- \( \sigma^{(Y,y_2,y_3)} \in \text{UWD}(Y) \) and \( \sigma^{(Y_2,y_{23},y_1)} \in \text{UWD}(Y_2) \) are splits.
Then
\[
\sigma(Y,y_1,y_2) \circ \sigma(Y_1,y_{12},y_3) = \sigma(Y_2,y_{13}) \circ \sigma(Y_2,y_{23}) \in \text{UWD}^{(Y)}_X. \tag{8.2.14.1}
\]

The next relation is the commutativity property between a split and a loop. It gives two different ways to construct the following undirected wiring diagram using a split and a loop.

**Proposition 8.2.15.** Suppose:

- \( Y \in \text{Fin}_S \), and \( y_1 \) and \( y_2 \) are distinct elements in \( Y \) with \( v(y_1) = v(y_2) \in S \).
- \( X \in \text{Fin}_S \), and \( x, x_+, x_- \) are distinct elements in \( X \) such that
  - \( v(x) = v(y_1) \);
  - \( v(x_+) = v(x_-) \);
  - \( X \setminus \{x, x_+, x_-\} = Y \setminus \{y_1, y_2\} \).
- \( Y' = [X \setminus \{x\}] \cup \{y_1, y_2\} \) and \( X' = X \setminus \{x_+, x_-\} \).
- \( \sigma(Y',y_1,y_2) \in \text{UWD}^{(Y')}_X \) and \( \sigma(Y,y_1,y_2) \in \text{UWD}^{(Y)}_X \) are splits.
- \( \lambda(Y',x_+) \in \text{UWD}^{(Y')}_X \) and \( \lambda(X,x_+) \in \text{UWD}^{(Y)}_X \) are loops.

Then
\[
\lambda(Y',x_+) \circ \sigma(Y',y_1,y_2) = \sigma(Y,y_1,y_2) \circ \lambda(X,x_+) \in \text{UWD}^{(Y)}_X. \tag{8.2.15.1}
\]

The next relation says that the undirected wiring diagram

![Diagram](image1)

can be obtained by substituting a split inside a loop as in the picture

![Diagram](image2)
or in the counterpart in which \( x_+ \) and \( x_- \) are switched. In (8.2.16.1) below, this picture corresponds to the left side, and its counterpart corresponds to the right side.

**Proposition 8.2.16.** Suppose:

- \( X \in \text{Fin}_S \), and \( x_+ \) and \( x_- \) are distinct elements in \( X \) with \( v(x_+) = v(x_-) \in S \).
- \( Y \in \text{Fin}_S \), and \( y \in Y \) such that \( v(y) = v(x_+) \) and that \( X \setminus x_\pm = Y \setminus y \).
- \( W = X \sqcup y = Y \sqcup x_\pm \in \text{Fin}_S \).
- \( \sigma(W,y,x_+) \in \text{UWD}(W^/) \) and \( \sigma(W,y,x_-) \in \text{UWD}(W^-) \) are splits.
- \( \lambda(W,x_+) \in \text{UWD}(W^-) \) is a loop.

Then

\[
\lambda(W,x_+) \circ \sigma(W,y,x+) = \lambda(W,x_+) \circ \sigma(W,y,x-) \in \text{UWD}(W^-). \tag{8.2.16.1}
\]

The final relation is the commutativity property of loops. It gives two different ways to construct the following undirected wiring diagram using two loops.

![Undirected Wiring Diagram](image)

**Proposition 8.2.17.** Suppose:

- \( X \in \text{Fin}_S \), and \( x_1, x_2, x_3, x_4 \) are distinct elements in \( X \) with \( v(x_1) = v(x_2) \) and \( v(x_3) = v(x_4) \in S \).
- \( W = X \setminus \{x_1, x_2\}, Z = X \setminus \{x_3, x_4\}, and Y = X \setminus \{x_1, x_2, x_3, x_4\} \in \text{Fin}_S \).
- \( \lambda(W,x_3,x_4) \in \text{UWD}(W^/) \) and \( \lambda(X,x_1,x_2) \in \text{UWD}(W^-) \) are loops.
- \( \lambda(Z,x_1,x_2) \in \text{UWD}(Z^/) \) and \( \lambda(X,x_3,x_4) \in \text{UWD}(Z^-) \) are loops.

Then

\[
\lambda(Z,x_1,x_2) \circ \lambda(X,x_1,x_2) = \lambda(Z,x_1,x_2) \circ \lambda(X,x_3,x_4) \in \text{UWD}(Z^-). \tag{8.2.17.1}
\]

**Definition 8.2.18.** The 17 relations (8.2.1.1)–(8.2.17.1) are called elementary relations in \( \text{UWD} \). If there is no danger of confusion, we will call them elementary relations.

### 8.3. Wasted Cables

The purpose of this section is to consider several examples of how the generators in the operad \( \text{UWD} \) can create wasted cables (Def. 7.1.2). Example 8.3.4 provides an illustration of some of the elementary relations in \( \text{UWD} \). The examples in this
section provide a good warm-up exercise for the discussion in Chapter 10 about stratified presentations and elementary equivalences.

Recall from Remark 8.1.7 that none of the generators has a wasted cable.

**Example 8.3.1.** In the context of Example 7.3.8 with $X = \{x_1, x_2\}$:

1. $\varphi = \{ X \longrightarrow \ast \longrightarrow \varnothing \} \in \text{UWD}(\varnothing)_X$ is the loop $\lambda_{(X,x_1,x_2)}$.

2. $\psi = \{ \varnothing \longleftarrow X \longleftarrow \ast \longrightarrow \varnothing \} \in \text{UWD}(\varnothing)_X$ is the iterated operadic composition

   \[
   \psi = \left[ \left( \theta_{(\varnothing,X)} \circ \theta_{(x_1,x_2)} \right) \circ \omega_{x_1} \circ \omega_{x_2} \right]
   \]

   involving two 2-cells and two 1-output wires.

So the composition

\[
\varphi \circ \psi = \left( \varnothing \longrightarrow \ast \longrightarrow \varnothing \right) \in \text{UWD}(\varnothing)_X,
\]

which is depicted as

\[
\begin{array}{c}
\text{Inclusion} \\
\text{Inclusion} \\
\end{array}
\]

and has one wasted cable, is the iterated operadic composition

\[
\lambda_{(X,x_1,x_2)} \circ \left[ \left( \theta_{(\varnothing,X)} \circ \theta_{(x_1,x_2)} \right) \circ \omega_{x_1} \circ \omega_{x_2} \right]
\]

(8.3.1.1) involving 5 generators.

**Example 8.3.2.** As a variation of the previous example, consider any box $Y \in \text{Fin}_S$ and the undirected wiring diagram with one wasted cable

\[
\zeta_Y = \left( Y \underbrace{\text{inclusion}}_{\varnothing} Y \sqcup \underbrace{\text{inclusion}}_{\varnothing} Y \right) \in \text{UWD}(\varnothing)_Y.
\]

It is depicted as follows.

\[
\begin{array}{c}
\text{Y} \\
\text{inclusion} \\
\end{array}
\]

This undirected wiring diagram can be created by replacing the empty box $\varnothing$ in the 2-cell $\theta_{(\varnothing,X)}$ by $Y$ and the loop $\lambda_{(X,x_1,x_2)}$ by the loop $\lambda_{(Y \sqcup X,x_1,x_2)}$ in (8.3.1.1) above. The resulting operadic composition

\[
\zeta_Y = \lambda_{(Y \sqcup X,x_1,x_2)} \circ \left[ \left( \theta_{(Y,X)} \circ \theta_{(x_1,x_2)} \right) \circ \omega_{x_1} \circ \omega_{x_2} \right] \in \text{UWD}(\varnothing)_Y
\]

(8.3.2.1)
involves 5 generators: one loop, two 2-cells, and two 1-output wires. It corresponds to the following picture.

```
```

The intermediate gray box is $Y \sqcup X = Y \sqcup \{x_1, x_2\}$. Roughly speaking, the operadic composition (8.3.2.1) says that a wasted cable can be created by applying a loop to two 1-output wires. Additional wasted cables can similarly be created using more 2-cells, 1-output wires, and loops.

**Example 8.3.3.** The undirected wiring diagram $\zeta_Y$ in Example 8.3.2 can also be created as in the following picture.

```
```

The inner gray box is $Y \sqcup x_1$, and the outer gray box is $Y \sqcup X$. In terms of the generators, the above picture is realized as the operadic composition

$$
\zeta_Y = \left[ \lambda_{(Y \sqcup X, x_1, x_2)} \circ \sigma(Y \sqcup X, x_1, x_2) \right] \circ \left[ \theta_{(Y, x_1)} \circ_2 \omega_{x_1} \right] \in \text{UWD}(^Y_1). \quad (8.3.3.1)
$$

It involves one loop, one split, one 2-cell, and one 1-output wire. Roughly speaking, the operadic composition (8.3.3.1) says that a wasted cable can be created by applying a loop to a split that is attached to a 1-output wire.

**Example 8.3.4.** As an illustration of using the elementary relations in UWD, recall the undirected wiring diagram $\zeta_Y \in \text{UWD}(^Y_1)$ in Examples 8.3.2 and 8.3.3. It can be generated by the generators as either one of the two iterated operadic compositions (8.3.2.1) and (8.3.3.1). These two decompositions of $\zeta_Y$ are actually connected as
8.4. Summary of Chapter 8

(1) There are six generating undirected wiring diagrams.

(2) There are seventeen elementary relations in UWD.

(3) Wasted cables can arise from operadic composition of undirected wiring diagrams with no wasted cables.
Decomposition of Undirected Wiring Diagrams

This chapter is the undirected analogue of Chapter 4. As part of the finite presentation theorem for the operad $UWD$ of undirected wiring diagrams (Theorem 7.3.14), in Theorem 10.1.12 we will observe that each undirected wiring diagram has a highly structured decomposition in terms of generators (Def. 8.1.7), called a stratified presentation (Def. 10.1.8). Stratified presentations are also needed to establish the second part of the finite presentation theorem for the operad $UWD$ regarding relations (Theorem 10.2.7). The purpose of this chapter is to provide all the steps needed to establish the existence of a stratified presentation for each undirected wiring diagram. We remind the reader about Notation 3.3.1 for (iterated) operadic compositions.

Fix a class $S$, with respect to which the operad $UWD$ of undirected wiring diagrams (Def. 7.3.14) is defined.

9.1. A Motivating Example

Before we establish the desired decomposition of a general undirected wiring diagram, in this section we consider an elaborate example that will serve as a guide and motivation for the construction later in this chapter for the general case. The point of this decomposition is to break the complexity of a general undirected wiring diagram into several stratified pieces, each of which is easy to understand and visualize.
The following notations regarding subsets of cables will be used frequently in this chapter. Recall that an \((m,n)\)-cable is a cable to which exactly \(m\) input wires and exactly \(n\) output wires are soldered (Def. 7.1.2).

**Notation 9.1.1.** Suppose \(\psi = (C_\psi, f_\psi, g_\psi)\) is an undirected wiring diagram and \(m, n \geq 0\). Define:

- \(C_{\psi}^{(m,n)} \subseteq C_\psi\) as the subset of \((m,n)\)-cables. In particular, \(C_\psi^{(0,0)}\) is the set of wasted cables.
- \(C_{\psi}^{(\geq m,n)} \subseteq C_\psi\) as the subset of \((l,n)\)-cables with \(l \geq m\).
- \(C_{\psi}^{(m,\geq n)} \subseteq C_\psi\) as the subset of \((m,k)\)-cables with \(k \geq n\).
- \(C_{\psi}^{(\geq m,\geq n)} \subseteq C_\psi\) as the subset of \((j,k)\)-cables with \(j \geq m\) and \(k \geq n\).
- \(C_{\psi}^{\geq 3} \subseteq C_\psi\) as the subset of \((k,l)\)-cables with \(k,l \geq 1\) and \(k+l \geq 3\).

A cable in \(C_{\psi}^{(\geq m,n)}\) is called an \((\geq m,n)\)-cable, and similarly for cables in the other subsets defined above.

As in the case of wiring diagrams (see Convention 4.2.4), name changes (Def. 8.1.3) are easy to deal with. Therefore, in the following example, to keep the presentation simple, we will ignore name changes.

**Example 9.1.2.** Consider \(\varphi = (C_\varphi, f_\varphi, g_\varphi) \in \text{UWD}(X_1, X_2)\) in (7.1.7.1), which is visualized as

```
with \(X_1 = \{x_1, \ldots, x_6\}\) and \(X_2 = \{x^1, x^2\}\). We can decompose it as
\[
\varphi = \varphi_1 \circ \varphi_2
\] (9.1.2.1)
```

as indicated in the following picture.
As before the intermediate gray box $Z$ indicates that an operadic composition occurs along it. The box $Z$ is defined as

$$Z = X \sqcup \{c_{4+}, c_{4-}\} \sqcup \{c_1, c_5\} \sqcup \{c_7\} \in \text{Fin}_S$$

in which:

- $X = X_1 \sqcup X_2$.
- $c_{4+}$ and $c_{4-}$ are two copies of the wasted cable $c_4$ in $\varphi$, so $\{c_{4+}, c_{4-}\} = C^{(0,0)}_{\varphi} \sqcup C^{(0,0)}_{\varphi}$.
- $\{c_1, c_5\} = C^{(0,\geq 1)}_{\varphi}$.
- $\{c_7\} = C^{(1,0)}_{\varphi}$.

So we may also write $Z$ as

$$Z = X \sqcup C^{(0,0)}_{\varphi, \pm} \sqcup C^{(0,\geq 1)}_{\varphi} \sqcup C^{(1,0)}_{\varphi}$$

in which $C^{(0,0)}_{\varphi, \pm} = C^{(0,0)}_{\varphi} \sqcup C^{(0,0)}_{\varphi}$ is the coproduct of two copies of the set of wasted cables $C^{(0,0)}_{\varphi}$ in $\varphi$.

In the decomposition [9.1.2.1] of $\varphi$, the inside undirected wiring diagram is the cospan

$$\varphi_2 = \left( \begin{array}{c} X \xrightarrow{\text{inclusion}} Z \\ \xrightarrow{=} Z \end{array} \right) \in \text{UWD}(x_1, x_2).$$

Note that in $\varphi_2$:

- All the input wires—i.e., those in $X$—are soldered to $(1, 1)$-cables.
- All other cables—i.e., those in $C^{(0,0)}_{\varphi, \pm} \sqcup C^{(0,\geq 1)}_{\varphi} \sqcup C^{(1,0)}_{\varphi}$—are $(0, 1)$-cables.
- There are no wasted cables.
As we will see later in (9.3.8.1), such an undirected wiring diagram can be decomposed into 2-cells (Def. 8.1.4) and 1-output wires (Def. 8.1.2). For example, this \( \varphi_2 \) needs:

- five 1-output wires, exactly as many as the number of \((0,1)\)-cables;
- six 2-cells, where 6 is the number of input boxes plus the number of \((0,1)\)-cables minus 1.

The outside undirected wiring diagram in the decomposition \( \varphi = \varphi_1 \circ \varphi_2 \) is the cospan

\[
\varphi_1 = \left( Z \xrightarrow{(f_\varphi, \iota)} C_\varphi \xleftarrow{g_\varphi} Y \right) \in \text{UWD}(U).
\]

Here:

- \( f_\varphi : X \to C_\varphi \) is the input soldering function of \( \varphi \).
- \( \iota : C^{(0,0)}_{\varphi, \pm} \cup C^{(0,1)}_{\varphi, \leq} \cup C^{(1,0)}_{\varphi, \leq} \to C_\varphi \) is the inclusion map on each coproduct summand.
- \( g_\varphi : Y \to C_\varphi \) is the output soldering function of \( \varphi \).
- Every cable is an \((m,n)\)-cable with \( m \geq 1 \) and \( n \geq 0 \). In other words, every cable in \( \varphi_1 \) is soldered to some input wires, so in particular there are no wasted cables in \( \varphi_1 \).
- There are also no \((1,0)\)-cables, but there are \((\geq 2,0)\)-cables.

As we will see later, such an undirected wiring diagram can be decomposed into loops (Def. 8.1.5) and splits (Def. 8.1.6). In the case of \( \varphi_1 \), which is the undirected wiring diagram

\[
\varphi_1 = \varphi_1 \circ \varphi_2
\]

this further decomposition

\[
\varphi_1 = \varphi_1 \circ \varphi_2
\]

(9.1.2.3)
9.1. A Motivating Example

can be visualized as follows.

![Diagram of a wiring diagram]

In this decomposition \( \phi_1 = \phi_1 \circ \phi_2 \), the inner undirected wiring diagram is the cospan

\[
\phi_2 = \left( \begin{array}{c} Z \\ \xrightarrow{g_{\phi_2}} \\ W \end{array} \right) \in \text{UWD}(W)
\]

with \( g_{\phi_2} \) surjective. So every cable in \( \phi_2 \) is a \((1, n)\)-cable for some \( n \geq 1 \). As we will see later, such an undirected wiring diagram is generated by splits (Def. 8.1.6). For example, this \( \phi_2 \) is the iterated operadic composition of 5 splits—one for the cable soldered to \( c_1 \), one for the cable soldered to \( x_5 \), and three for the cable soldered to \( x_2 \).

The outer undirected wiring diagram in the decomposition (9.1.2.3) is the cospan

\[
\phi_1 = \left( \begin{array}{c} W \\ \xleftarrow{\text{C}_{\phi_1}} \\ Y \end{array} \right) \in \text{UWD}(Y)
\]

in which every cable is either a \((1, 1)\)-cable or a \((2, 0)\)-cable. We will show later that such an undirected wiring diagram is generated by loops (Def. 8.1.5). For example, this \( \phi_1 \) is the iterated operadic composition of 6 loops, where 6 is the number of \((2, 0)\)-cables in \( \phi_1 \).

In summary, we decompose \( \varphi \in \text{UWD}(X_{1, X_0}) \) as the iterated operadic composition

\[
\varphi = \varphi_1 \circ \varphi_2 = \varphi_1 \circ \varphi_2 \circ \varphi_2
= \left( \lambda_1, \ldots, \lambda_6, \sigma_5, \ldots, \sigma_5, \theta_6, \ldots, \theta_6, \omega_5, \ldots, \omega_5 \right).
\]

Here \( \lambda, \sigma, \theta, \) and \( \omega \) denote a loop, a split, a 2-cell, and a 1-output wire, respectively. This decomposition in terms of the generators is called a stratified presentation (Def. 10.1.8). In the next few sections, we will establish all the steps needed to obtain a stratified presentation for a general undirected wiring diagram.
9.2. Factoring Undirected Wiring Diagrams

In this section, using Example 9.1.2 as a guide and motivation, we establish a decomposition of a general undirected wiring diagram into two simpler undirected wiring diagrams (Theorem 9.2.3). This is the general version of the decomposition (9.1.2.1) above. Each undirected wiring diagram in this decomposition will be decomposed further, eventually leading to the desired stratified presentation.

**Assumption 9.2.1.** Suppose 
\[
\psi = \left( X \xrightarrow{f_\psi} C_\psi \xleftarrow{g_\psi} Y \right) \in \text{UWD}(\Sigma) 
\] (9.2.1.1)
is a general undirected wiring diagram with:
- output box \(Y \in \text{Fin}_S\) and input boxes \(X = (X_1, \ldots, X_N)\) for some \(N \geq 0\);
- \(X = X_1 \cup \cdots \cup X_N \in \text{Fin}_S\).

Recall Notation 9.1.1 for certain subsets of cables. The undirected wiring diagrams \(\psi_1\) and \(\psi_2\) in the next definition are the general versions of \(\varphi_1\) and \(\varphi_2\) in the decomposition (9.1.2.1) above.

**Definition 9.2.2.** Suppose \(\psi = \left( C_\psi, f_\psi, g_\psi \right) \in \text{UWD}(\Sigma)\) is a general undirected wiring diagram as in (9.2.1.1) with \(X = (X_1, \ldots, X_N)\).

1. Define 
\[
Z = X \cup C_{\psi, ±}^{(0,0)} \cup C_{\psi}^{(0,1)} \cup C_{\psi}^{(1,0)} \in \text{Fin}_S \quad \text{(9.2.2.1)}
\]
in which 
\[
C_{\psi, ±}^{(0,0)} = C_{\psi}^{(0,0)} \cup C_{\psi}^{(0,0)}
\]
is the coproduct of two copies of the set of wasted cables \(C_{\psi}^{(0,0)}\) in \(\psi\).

2. Define the undirected wiring diagram 
\[
\psi_1 = \left( Z \xrightarrow{(f_\psi, \iota)} C_\psi \xleftarrow{g_\psi} Y \right) \in \text{UWD}(\Sigma) \quad \text{(9.2.2.2)}
\]
in which 
\[
C_{\psi, ±}^{(0,0)} \cup C_{\psi}^{(0,1)} \cup C_{\psi}^{(1,0)} \xrightarrow{\iota} C_\psi
\]
is the inclusion map on each coproduct summand.

3. Define the undirected wiring diagram 
\[
\psi_2 = \left( X \xrightarrow{\text{inclusion}} Z \xleftarrow{=} Z \right) \in \text{UWD}(\Sigma). \quad \text{(9.2.2.3)}
\]

**Theorem 9.2.3.** In the context of Def. 9.2.2, there is a decomposition 
\[
\psi = \psi_1 \circ \psi_2 \in \text{UWD}(\Sigma). \quad \text{(9.2.3.1)}
\]
Proof. By the definition of $\circ = \circ_1$ (Def. 7.3.5), the operadic composition $\psi_1 \circ \psi_2$ is given by the cospan

$$
\begin{array}{c}
\xymatrix{ & Y \ar[dl]_{g_\psi} \ar[dr]^{g_\psi} & \\
Z \ar[d]^{(f_{\psi,i})} & C_\psi \ar[d]_{=} & Z \ar[d]_{(f_{\psi,i})} \\
X & \ar@{=}[r] & C_\psi \ar@{=}^{f_\psi}
}
\end{array}
$$

in $\text{Fin}_S$. The square is a pushout by Example 7.2.3. This cospan is equal to $\psi$. \hfill $\Box$

Example 9.2.4. If $\psi = \epsilon$ is the empty cell (Def. 8.1.1), then:

- $\psi_1 = 1_{\emptyset}$, the $\emptyset$-colored unit (Def. 7.3.2) with $\emptyset \in \text{Fin}_S$ the empty box;
- $\psi_2 = \epsilon$.

So in this case the decomposition (9.2.3.1) simply says $\epsilon = 1_{\emptyset} \circ \epsilon$.

Remark 9.2.5. In the decomposition (9.2.3.1), both $\psi_1$ and $\psi_2$ are simpler than $\psi$ for the following reasons.

1. $\psi_1$ has the same set of cables $C_\psi$ and the same output soldering function $g_\psi$ as $\psi$. Furthermore, its input soldering function $(f_{\psi,i})$ includes the input soldering function $f_\psi$ of $\psi$. However, every cable in $\psi_1$ is soldered to at least one input wire (i.e., $C_{\psi_1}^{(0,\geq 0)} = \emptyset$), whereas $C_{\psi}^{(0,\geq 0)}$ may be non-empty. In particular, $\psi_1$ has no wasted cables, even though $\psi$ may have some. Furthermore, $\psi_1$ has only one input box $Z$, while $\psi$ has $N \geq 0$ input boxes.

2. $\psi_2$ has the same input boxes $X$ as $\psi$. However, it is, in general, much simpler than $\psi$ and $\psi_1$ because its cables are either $(1,1)$-cables or $(0,1)$-cables. In particular, $\psi_2$ also has no wasted cables.

3. Neither $\psi_1$ nor $\psi_2$ has any $(1,0)$-cables, even though $\psi$ may have some.

9.3. The Inner Undirected Wiring Diagram

The purpose of this section is to analyze the undirected wiring diagram $\psi_2$ in the decomposition (9.2.3.1). The undirected wiring diagram $\psi_1$ will be studied in the next few sections. We begin with the following observation regarding iterated operadic compositions of 2-cells (Def. 8.1.4).

Motivation 9.3.1. The following result says that an undirected wiring diagram of the form
can be generated by 2-cells.

**Proposition 9.3.2.** Suppose \( n \geq 2 \), \( X_i \in \text{Fin}_S \) for \( 1 \leq i \leq n \), and \( X = \bigsqcup_{i=1}^{n} X_i \). Then the undirected wiring diagram

\[
\Theta = \left( \begin{array}{c}
X \\
\cdots
\end{array} \begin{array}{c}
X \\
\cdots
\end{array} \begin{array}{c}
X
\end{array} \right) \in \text{UWD}(X_{X_i \cdots X_n})
\]

is:

- a 2-cell if \( n = 2 \);
- an iterated operadic composition

\[\Theta = \left( (\theta_1 \circ_2 \theta_2) \circ_3 \cdots \circ_{n-1} \theta_{n-1} \right)\]

with each \( \theta_j \) a 2-cell if \( n \geq 3 \).

**Proof.** This is proved by induction on \( n \geq 2 \). The initial case simply says that \( \Theta \) is the 2-cell \( \theta_{(X_1,X_2)} \) by Def. [8.1.4]

Suppose \( n \geq 3 \). By the definition of \( \circ_{n-1} \) (Def. [7.3.5] and Example [7.2.3]) we may decompose \( \Theta \) as

\[\Theta = \Theta_1 \circ_{n-1} \theta_{(X_{n-1},X_n)}\]

in which

\[\Theta_1 = \left( \begin{array}{c}
X \\
\cdots
\end{array} \begin{array}{c}
X \\
\cdots
\end{array} \begin{array}{c}
X
\end{array} \right) \in \text{UWD}(X_{X_{i=2}X_n})\]

and

\[\theta_{(X_{n-1},X_n)} \in \text{UWD}(X_{X_{n-1}X_n})\]

is a 2-cell. Since the induction hypothesis applies to \( \Theta_1 \), the proof is finished. \( \Box \)

**Example 9.3.3.** In the previous Proposition:

1. If \( n = 3 \), then \( \Theta \) decomposes as

\[\Theta = \theta_{(X_1,X_2 \sqcup X_3)} \circ_2 \theta_{(X_2,X_3)}\]

into two 2-cells.

2. If \( n = 4 \), then \( \Theta \) decomposes as

\[\Theta = \left( \theta_{(X_1,X_2 \sqcup X_3 \sqcup X_4)} \circ_2 \theta_{(X_2,X_3 \sqcup X_4)} \circ_3 \theta_{(X_3,X_4)} \right)\]

into three 2-cells.

**Notation 9.3.4.** In the context of [9.2.2.1], write:
9.3. The Inner Undirected Wiring Diagram

\[ C'_{\psi} = C_{\psi, +}^{(0, 0)} \cup C_{\psi, -}^{(0, \geq 1)} \cup C_{\psi}^{(1, 0)} \in \text{Fin}_S, \text{ so } Z = X \cup C'_{\psi}. \]

\[ p = \left| C'_{\psi} \right|. \]

The following observation covers the marginal cases for \( \psi_2 \).

**Lemma 9.3.5.** For \( \psi_2 = \left( X \xrightarrow{\text{inclusion}} Z \right) \in \text{UWD}(\mathcal{Z}) \) in (9.2.2.3):

1. If \( N = p = 0 \), then \( \psi_2 \) is the empty cell \( \epsilon \) (Def. 8.1.1).
2. If \( N = 0 \) and \( p = 1 \), then \( \psi_2 \) is a 1-output wire (Def. 8.1.2).
3. If \( N = 1 \) and \( p = 0 \), then \( \psi_2 \) is the \( X_1 \)-colored unit (Def. 7.3.2).

**Proof.** Since \( X = (X_1, \ldots, X_N) \) and \( X = X_1 \cup \cdots \cup X_N \), all three statements follow immediately from the definition of \( \psi_2 \). \( \square \)

The next observation covers the other cases for \( \psi_2 \). Recall \( C'_{\psi} \) in Notation 9.3.4.

**Motivation 9.3.6.** The following result says that an undirected wiring diagram of the form

\[ \cdots \quad X_1 \quad \cdots \quad X_N \quad \cdots \]

can be generated by 2-cells and 1-output wires.

**Proposition 9.3.7.** For \( \psi_2 = \left( X \xrightarrow{\text{inclusion}} Z \right) \in \text{UWD}(\mathcal{Z}) \) in (9.2.2.3), suppose:

- \( N, p \geq 1 \), and \( C'_{\psi} = \{c_1, \ldots, c_p\} \);
- \( \omega_j = \left( \varnothing \xrightarrow{=} c_j \xrightarrow{=} c_j \right) \in \text{UWD}(\gamma) \) is the 1-output wire for \( c_j \) (Def. 8.1.2) for \( 1 \leq j \leq p \).

Then there is a decomposition

\[ \psi_2 = \left( (\Theta \circ_{N+1} \omega_1) \cdots \circ_{N+1} \omega_p \right) \in \text{UWD}(\mathcal{Z}) \quad (9.3.7.1) \]

in which every pair of parentheses starts on the left and

\[ \Theta = \left( \xrightarrow{=} Z \xleftarrow{=} Z \right) \in \text{UWD}(X_1, \ldots, X_N, c_1, \ldots, c_p). \]

**Proof.** The right side of (9.3.7.1) is a well-defined element in (\( \mathcal{Z} \)). By the correspondence between the \( \circ_i \)-compositions and \( \gamma \) (2.1.12.1) in the operad UWD, the right
9. Decomposition of Undirected Wiring Diagrams

side of (9.3.7.1) can be rewritten as

\[ \psi'_2 = \gamma \left( \Theta; \mathbb{1}_{X_1}, \ldots, \mathbb{1}_{X_N}, \omega_1, \ldots, \omega_p \right). \]

Since \( Z = X \cup \{ c_1, \ldots, c_p \} \), by Prop. 7.3.16 the cospan for \( \psi'_2 \) is

\[ \begin{array}{ccc}
Z & \rightarrow & Z \\
\downarrow & & \downarrow \\
X & \hookrightarrow & Z
\end{array} \]

in \( \text{Fin}_5 \). This is equal to the cospan that defines \( \psi_2 \). \( \square \)

The following observation says that, if \( N, p \geq 1 \), then \( \psi_2 \) is generated by 2-cells and 1-output wires.

**Corollary 9.3.8.** Suppose \( \psi_2 \in \text{UWD}(\mathcal{A}) \) in (9.2.2.3) has \( N = |X|, p = |C'_\psi| \geq 1 \). Then there is a decomposition

\[ \psi_2 = [ \left( (\theta_1 \circ_2 \theta_2) \circ_3 \cdots \circ_{N+p-1} \theta_{N+p-1} \right) \circ_{N+1} \omega_1 ] \cdots \circ_{N+1} \omega_p \]  

(9.3.8.1)

with:

- each \( \theta_i \) a 2-cell;
- each \( \omega_j \) a 1-output wire;
- each pair of parentheses starting on the left.

**Proof.** This is true by the decomposition (9.3.7.1) above and Prop. 9.3.2 with \( n = N + p \geq 2 \), applied to \( \Theta \). \( \square \)

### 9.4. The Outer Undirected Wiring Diagram

The purpose of this section is to establish a decomposition for the undirected wiring diagram \( \psi_1 \) (9.2.2.2) that appeared in (9.2.3.1). This is the general version of the decomposition (9.1.2.3), so the reader may wish to refer back there for specific examples of the constructions below. Each of the constituent undirected wiring diagrams in this decomposition will be studied further in later sections. The goal is to decompose \( \psi_1 \) into two undirected wiring diagrams in which the outer one, called \( \phi_1 \) below, is generated by loops (Def. 8.1.5), while the inner one, called \( \phi_2 \) below, is generated by splits (Def. 8.1.6).

Recall Notation 9.1.1 for certain subsets of cables. Also recall from Remark 9.2.5 that \( \psi_1 \in \text{UWD}(\mathcal{A}) \) has neither \((0, \geq 0)\)-cables nor \((1, 0)\)-cables. So \( \psi_1 \) satisfies the hypotheses of the next definition.
9.4. The Outer Undirected Wiring Diagram

Definition 9.4.1. Suppose \( \varphi = (C_\varphi, f_\varphi, g_\varphi) \in \text{UWD}_{(B, A)} \) is an undirected wiring diagram with

- one input box \( A \) and
- \( C_\varphi^{(0, \geq 0)} = \emptyset = C_\varphi^{(1, 0)} \).

We will write \( f_\varphi \) and \( g_\varphi \) as \( f \) and \( g \), respectively.

(1) For each cable \( c \in C_\varphi^{(\geq 3, 0)} \cup C_\varphi^{\geq 3} \), choose a wire \( a_c \in f^{-1}c \subseteq A \), where \( f^{-1}c = f^{-1}\{c\} \) is the set of \( f \)-preimages of \( c \).

(2) Define
\[
W = B \cup f^{-1}C_\varphi^{(2, 0)} \cup \coprod_{c \in C_\varphi^{(\geq 3, 0)} \cup C_\varphi^{3}} \left[ f^{-1}c \setminus a_c \right] \in \text{Fin}_S
\] (9.4.1.1)
in which
\[
\left[ f^{-1}c \setminus a_c \right]_+ = \left[ f^{-1}c \setminus a_c \right]_+ \cup \left[ f^{-1}c \setminus a_c \right]_-
\]
is the coproduct of two copies of \( f^{-1}c \setminus a_c \). This \( W \) is the general version of the \( W \) in the example (9.1.2.4).

(3) Define
\[
V = B \cup C_\varphi^{(2, 0)} \cup \coprod_{c \in C_\varphi^{(\geq 3, 0)} \cup C_\varphi^{3}} \left[ f^{-1}c \setminus a_c \right] \in \text{Fin}_S.
\] (9.4.1.2)
This \( V \) is the general version of the set of cables between \( W \) and \( Y \) in the example (9.1.2.4).

(4) Define
\[
\phi_1 = \left( W \xrightarrow{f_1} V \xleftarrow{g_1} B \right) \in \text{UWD}_{(B, A)}
\] (9.4.1.3)
in which the restrictions of \( f_1 \) to the coproduct summands of \( W \) are defined as follows.

- \( f_1 : B \rightarrow B \) is the identity map.
- \( f_1 : f^{-1}C_\varphi^{(2, 0)} \rightarrow C_\varphi^{(2, 0)} \) is the map \( f \).
- \( f_1 : \left[ f^{-1}c \setminus a_c \right]_+ \rightarrow \left[ f^{-1}c \setminus a_c \right]_+ \) is the fold map for each \( c \in C_\varphi^{(\geq 3, 0)} \cup C_\varphi^{\geq 3} \).

That is, the restriction of \( f_1 \) to each of \( \left[ f^{-1}c \setminus a_c \right]_+ \) and \( \left[ f^{-1}c \setminus a_c \right]_- \) is the identity map.

This \( \phi_1 \) is the general version of that in the example (9.1.2.4).

(5) Define
\[
\phi_2 = \left( A \xrightarrow{f_2} A \xleftarrow{g_2} W \right) \in \text{UWD}_{(A, W)}
\] (9.4.1.4)
as follows. We will use the equality
\[ B = g^{-1}C^{(1,2)}_q \sqcup \tilde{g}^{-1}C^{(2,1)}_q \]
which is true because \( C^{(0,2)}_q = \emptyset = C^{(1,0)}_q \). For
\[ w \in W = g^{-1}C^{(1,2)}_q \sqcup \tilde{g}^{-1}C^{(2,1)}_q \sqcup f^{-1}C^{(2,0)}_q \sqcup \bigcup_{c \in C^{(2,1)}_q \cup C^{(3)}_q} \left[ f^{-1}c \setminus a_c \right] \in \text{Fin}_S \quad (9.4.1.5) \]
define
\[
g_2(w) = \begin{cases} 
    \left\{ \begin{array}{l}
    f^{-1}g(w) \in A \\
    a_g(w) \in f^{-1}g(w) \subseteq A \\
    w \end{array} \right. & \text{if } w \in g^{-1}C^{(1,2)}_q; \\
    \left\{ \begin{array}{l}
    a_g(w) \in f^{-1}g(w) \subseteq A \\
    w \end{array} \right. & \text{if } w \in \tilde{g}^{-1}C^{(2,1)}_q; \\
    \left\{ \begin{array}{l}
    f^{-1}c \in A \\
    a_c \end{array} \right. & \text{if } w \in f^{-1}C^{(2,0)}_q \text{ or } w \notin \left[ f^{-1}c \setminus a_c \right]_+. 
\end{cases}
\]

In the first line of this definition, we used the fact that each cable in \( C^{(1,2)}_q \) has a unique \( f \)-preimage in \( A \). In the second line, \( a_2 \) was defined earlier in the current definition, using the fact \( C^{(2,1)}_q \subseteq C^{(3)}_q \). This \( \phi_2 \) is the general version of that in the example (9.1.2.4).

**Remark 9.4.2.** Consider the previous definition.

1. The input soldering function \( f_1 \) of \( \phi_1 \) is surjective. Furthermore, all the cables in \( \phi_1 \) are either \((1,1)\)-cables (namely, those cables in \( B \subseteq V \)) or \((2,0)\)-cables (namely, those in \( V \setminus B \)).

2. The output soldering function \( g_2 \) of \( \phi_2 \) is surjective because of the assumption \( C^{(0,2)}_q = \emptyset = C^{(1,0)}_q \).

**Theorem 9.4.3.** In the context of Def. 9.4.1, there is a decomposition
\[ \emptyset = \phi_1 \circ \phi_2. \quad (9.4.3.1) \]

**Proof.** It suffices to check that the operadic composition \( \phi_1 \circ \phi_2 \in \text{UWD}^{(3)}_{(A,B)} \) is given by the cospan
in $\text{Fin}_S$. Here the two coproducts $\coprod$ are both indexed by all $c \in C^{(2,0)}$ $\cup C^{2,0}$. By the definition of $\circ = \circ_1$ (7.3.5.1), we just need to check that the rectangle is a pushout (Def. 7.2.1) in $\text{Fin}_S$. It follows from direct inspection of each coproduct summand of $W$ in (9.4.1.5) that the rectangle is commutative.

Next, suppose given a solid-arrow commutative diagram

\[
\begin{array}{ccc}
W & \xrightarrow{f_1} & V \\
\downarrow g_2 & & \downarrow g_3 \\
A & \xrightarrow{f} & C_\phi \\
\downarrow a & & \downarrow \beta \\
U & & \\
\end{array}
\]

in $\text{Fin}_S$. We must show that there exists a unique map $h$ that makes the diagram commutative. Recall that

\[C_\phi = C^{(1,1)}_\phi \cup C^{(2,0)}_\phi \cup C^{(2,3)}_\phi \cup C^{2,3}_\phi\]

because $C^{(2,0)} = \emptyset = C^{(1,0)}$. Define $h : C_\phi \rightarrow U$ as

\[h(c) = \begin{cases} 
\alpha f^{-1}(c) & \text{if } c \in C^{(1,1)}_\phi; \\
\beta(c) & \text{if } c \in C^{(2,0)}_\phi \subseteq V; \\
\alpha(a_c) & \text{if } c \in C^{(2,3)}_\phi \cup C^{2,3}_\phi.
\end{cases}\]

One checks by direct inspection that (i) $hf = \alpha$ and $hg_3 = \beta$ and that (ii) $h$ is the only such map. \qed

As we mentioned just before Def. 9.4.1 the decomposition (9.4.3.1) applies to $\psi_1 \in \text{UWD}^{(1)}$ defined in (9.2.2.2). In the next two sections, we will show that, up to name changes, $\phi_1$ is generated by loops (Prop. 9.6.2), and $\phi_2$ is generated by splits (Prop. 9.5.3).

### 9.5. Iterated Splits

The purpose of this section is to show that $\phi_2$ (9.4.1.4) is either a name change or is generated by splits. First let us adopt the following convention, which is the undirected version of Convention 4.2.4.

**Convention 9.5.1.** Using the three elementary relations (8.2.3.1), (8.2.4.1), and (8.2.5.1), name changes (Def. 8.1.3) can always be rewritten on the outside (i.e., left side) of an iterated operadic composition in UWD. Moreover, using the elementary relation (8.2.1.1), an iteration of name changes can be composed down into just one name change. To simplify the presentation, in what follows these elementary relations...
regarding name changes are automatically applied wherever necessary. With this in mind, in the sequel we will mostly not mention name changes.

Recall from Remark 9.4.2 that in $\phi_2 \ (9.4.1.4)$, the input soldering function is the identity function and the output soldering function is surjective. So the following Proposition applies to $\phi_2$.

**Motivation 9.5.2.** The following result says that an undirected wiring diagram of the form

\[
\begin{array}{c}
\vdots \\
A \\
\vdots \\
\vdots \\
g^{-1}a_i
\end{array}
\]

\[
\begin{array}{c}
\vdots \\
\vdots \\
\vdots \\
g^{-1}a_n
\end{array}
\]

can be generated by splits.

**Proposition 9.5.3.** Suppose $A, B \in \text{Fin}_S$, and

\[
\rho = \left( \begin{array}{c}
A & f_\rho \\
\downarrow & \downarrow \\
A & g_\rho \\
\downarrow & \downarrow \\
B \end{array} \right) \in \text{UWD}(B_A) \quad (9.5.3.1)
\]

with $f_\rho = \text{Id}_A$ and $g_\rho$ surjective.

1. If $A = \emptyset$, then $\rho = 1_\emptyset \in \text{UWD}(\emptyset)$ (Def. 7.3.2).
2. Suppose $A \neq \emptyset$.
   
   (i) If $g_\rho$ is a bijection, then $\rho$ is a name change $\tau_{A,B}$.
   
   (ii) Otherwise, $\rho$ is an iterated operadic composition of splits (Def. 8.1.6).

**Proof.** We will write $f_\rho$ and $g_\rho$ as $f$ and $g$, respectively. If $A = \emptyset$, then $\rho$ is the cospan $(\emptyset \rightarrow \emptyset \leftarrow \emptyset)$, which is the $\emptyset$-colored unit in UWD. Suppose $A \neq \emptyset$. If $g$ is a bijection, then by definition $g$ is the name change $\tau_{g^{-1}}$.

So suppose $g$ is surjective but is not a bijection. We must show that $\rho$ is an iterated operadic composition of splits. The first step is to decompose $\rho$ in such a way that each constituent undirected wiring diagram creates one group of output wires $g^{-1}a_i$. Decompose $A$ as $A = A_1 \sqcup A_2 \in \text{Fin}_S$ in which

- $A_1 = \{a \in A : |g^{-1}a| = 1\}$;
- $A_2 = \{a \in A : |g^{-1}a| \geq 2\} = \{a_1, \ldots, a_n\}$.

By assumption $A_2 \neq \emptyset$. To decompose $\rho$ we will use the following intermediate boxes. For each $1 \leq i \leq n + 1$, define

\[
D_i = A_1 \sqcup \bigoplus_{1 \leq k < i} g^{-1}a_k \sqcup \{a_{i+1}, \ldots, a_n\} \in \text{Fin}_S.
\]
Note that $D_1 = A$ and $D_{n+1} \cong B$.

For $1 \leq i \leq n$ define

$$\rho_i = \left( D_i \xrightarrow{f_i} D_i \xleftarrow{g_i} D_{i+1} \right) \in \text{UWD}(D_{i+1}) \tag{9.5.3.2}$$

in which, for $d \in D_{i+1}$,

$$g_i(d) = \begin{cases} a_i & \text{if } d \in g^{-1}a_i, \\ d & \text{otherwise}. \end{cases}$$

A direct inspection using Example 7.2.3 and Prop. 7.3.6 shows that, up to a name change, there is a decomposition

$$\rho = \rho_n \circ \cdots \circ \rho_1 \in \text{UWD}(B_A). \tag{9.5.3.3}$$

When $n = 2$, this decomposition is depicted in the following picture.

To finish the proof, it suffices to show that each $\rho_i$ is an iterated operadic composition of splits. We will prove this assertion in the next result. \hfill \Box

**Motivation 9.5.4.** The following result says that an undirected wiring diagram of the form

\begin{center}
\begin{tikzpicture}
\node (A) at (0,0) {$A$};
\node (b1) at (-2,-2) {$b_1$};
\node (bp) at (-2,-4) {$b_p$};
\node (a1) at (-3,-3) {$a_1$};
\node (a2) at (-3,-4) {$a_2$};
\node (A1) at (-1,-2.5) {};\node (B) at (-1,2.5) {};
\draw (A) -- (B);
\draw (A) -- (A1) node [midway, above] {$g^{-1}a_1$};
\draw (A) -- (B) node [midway, above] {$g^{-1}a_2$};
\draw (A) -- (b1);\draw (A) -- (bp);
\end{tikzpicture}
\end{center}

\text{can be generated by splits.}

**Proposition 9.5.5.** Suppose $D \in \text{Fin}_S$, $D \not\ni b \in S$, and

$$\pi = \left( D \cup b \xrightarrow{=} D \cup b \xrightarrow{g} D \cup g^{-1}b \right) \in \text{UWD}(D_{g^{-1}b}) \tag{9.5.5.1}$$

such that

- $g|_D = \text{Id}_D$ and
- $p = |g^{-1}b| \geq 2.$

Then $\pi$ is an iterated operadic composition of $p - 1$ splits.
Proof. Write $g^{-1}b = \{b_1, \ldots, b_p\}$. If $p = 2$ then $\pi$ is the split $\sigma^{(D_\cup\{b_1, b_2\}, b_1, b_2)}$ by definition.

Suppose $p \geq 3$. Then there is a decomposition of $\pi$ into $p - 1$ splits as

$$\pi = \sigma^{(D_\cup\{b_1, \ldots, b_p\}, b_{p-1}, b_p)} \circ \ldots \circ \sigma^{(D_\cup\{b_1, b_{[2:p]}\}, b_{[1:p]} \circ b_p)}.$$  \hfill (9.5.5.2)

Here each $b_{[j:p]}$ means the wires $b_j$ for $j \leq l \leq p$ are identified into one element. Starting from the right, the $j$th split in the above decomposition of $\pi$, namely

$$\sigma^{(D_\cup\{b_1, \ldots, b_j, b_{[j+1:p]}\}, b_{[j+1:p]})} \in \text{UWD}^{(D_\cup\{b_1, \ldots, b_j, b_{[j+1:p]}\})},$$

is the cospan

$$D \cup \{b_1, \ldots, b_j, b_{[j+1:p]}\} \xrightarrow{\pi} D \cup \{b_1, \ldots, b_j, b_{[j:p]}\}$$

in $\text{Fin}_S$. Here the output soldering function sends $b_j$ and $b_{[j+1:p]}$ to $b_{[j:p]}$ and is the identity function everywhere else. \hfill \Box

Example 9.5.6. For each $1 \leq i \leq n$ the undirected wiring diagram $\rho_i \in \text{UWD}^{(D_{\delta_i})}$ in (9.5.3.2) is of the form $\pi$ (9.5.5.1) with

$$D = A_1 \cup \bigcup_{1 \leq k < i} g^{-1}a_k \cup \{a_{i+1}, \ldots, a_n\} \quad \text{and} \quad b = a_i.$$

Therefore, $\rho$ in (9.5.3.3) is an iterated operadic composition of splits.

Example 9.5.7. In (9.5.5.2) above:

1. If $p = 3$, then $\pi$ decomposes into two splits as

$$\pi = \sigma^{(D_\cup\{b_1, b_2, b_3\}, b_2, b_3)} \circ \sigma^{(D_\cup\{b_1, b_{[2:3]}\}, b_1, b_{[2:3]})}.$$  \hfill (9.5.5.1)

2. If $p = 4$, then $\pi$ decomposes into three splits as

$$\pi = \sigma^{(D_\cup\{b_1, b_2, b_3, b_4\}, b_3, b_4)} \circ \sigma^{(D_\cup\{b_1, b_{[2:3]}, b_4\}, b_2, b_{[3:4]} \circ b_4)} \circ \sigma^{(D_\cup\{b_1, b_{[2:4]}\}, b_1, b_{[2:4]})}.$$  \hfill (9.5.5.3)

9.6. Iterated Loops

The purpose of this section is to show that $\phi_1$ (9.4.1.3) is either a name change or is generated by loops (Def. 8.1.5). Recall Convention 9.5.1 regarding name changes. Also recall from Remark 9.4.2 that in $\phi_1$ (9.4.1.3) each cable is either a $(1, 1)$-cable or a $(2, 0)$-cable. Therefore, the following result applies to $\phi_1$.

Motivation 9.6.1. The following result says that an undirected wiring diagram of the form
9.6. Iterated Loops

Proposition 9.6.2. Suppose $A, B, C \in \text{Fin}_S$ and

$$
\xi = \left( A \xrightarrow{f} C \xleftarrow{\text{inclusion}} B \right) \in \text{UWD}^{(\ell)}
$$

in which each cable is either a (1,1)-cable or a (2,0)-cable. Suppose $\xi$ has $q$ (2,0)-cables. Then:

1. $\xi$ is a name change if $q = 0$.
2. $\xi$ is the iterated operadic composition of $q$ loops (Def. 8.1.5) if $q \geq 1$.

Proof. Since $\xi$ only has (1,1)-cables and (2,0)-cables, up to a name change we may write it as the cospan

$$
\xi = \left( B \sqcup T_\pm \xrightarrow{f} B \sqcup T \xleftarrow{\text{inclusion}} B \right)
$$

with:

- $T$ the set of (2,0)-cables in $\xi$;
- $f^{-1}T = T_\pm = T_+ \sqcup T_-$ the coproduct of two copies of $T$.

If $q = 0$ (i.e., $T = \emptyset$), then $\xi$ is the $B$-colored unit (Def. 7.3.2).

If $q = 1$ with $T = \{t\}$ and $T_\pm = \{t_\pm\}$, then $\xi$ is the loop $\lambda_{\{Bt(t_\pm)\}}$ by definition.

Suppose $q \geq 2$. We may write $T = \{t^1, \ldots, t^q\}$ and $T_\pm = \{t^1_\pm, \ldots, t^q_\pm\}$. The picture

\hspace{1cm}

depicts a decomposition of $\xi$ into two loops when $q = 2$. A direct inspection shows that there is a decomposition of $\xi$ into $q$ loops as

$$
\xi = \lambda_{\{Bt_\pm(t^1_\pm)\}} \circ \cdots \circ \lambda_{\{Bt_\pm(t^q_\pm)\}}.
$$

(9.6.2.1)
Starting from the right, the \( j \)th loop in the above decomposition of \( \xi \), namely

\[
\lambda \left( B_{U \cup \{ t_{1}^{j}, \ldots, t_{q}^{j} \}} \right) \in \text{UWD}(B_{U \cup \{ t_{1}^{j}, \ldots, t_{q}^{j} \}}),
\]

is the cospan

\[
\begin{array}{c}
B \uplus \{ t_{1}^{j+1}, \ldots, t_{q}^{j} \} \\
\downarrow \text{inclusion} \\
B \uplus \{ t_{1}^{j+1}, \ldots, t_{q}^{j} \} \uplus t_{j}
\end{array}
\]

in \( \text{Fin}_{S} \). Here the input soldering function sends \( t_{j}^{l} \) to \( t_{j} \) and is the identity function everywhere else. \( \Box \)

**Example 9.6.3.** In (9.6.2.1) above:

1. If \( q = 2 \), then \( \xi \) decomposes into two loops as

\[
\xi = \lambda \left( B_{U \cup \{ t_{1}^{j}, t_{2}^{j} \}} \right) \circ \lambda \left( B_{U \cup \{ t_{1}^{j}, t_{2}^{j} \}} \right).
\]

2. If \( q = 3 \), then \( \xi \) decomposes into three loops as

\[
\xi = \lambda \left( B_{U \cup \{ t_{1}^{j}, t_{2}^{j}, t_{3}^{j} \}} \right) \circ \lambda \left( B_{U \cup \{ t_{1}^{j}, t_{2}^{j}, t_{3}^{j} \}} \right) \circ \lambda \left( B_{U \cup \{ t_{1}^{j}, t_{2}^{j}, t_{3}^{j} \}} \right).
\]

### 9.7. Summary of Chapter 9

Every undirected wiring diagram \( \varphi \) has a decomposition

\[
\varphi = \phi_{1} \circ \phi_{2} \circ \varphi_{2}
\]

in which:

- \( \phi_{1} \) is generated by loops;
- \( \phi_{2} \) is generated by splits;
- \( \varphi_{2} \) is generated by 2-cells and 1-output wires.
Finite Presentation for Undirected Wiring Diagrams

Fix a class $S$, with respect to which the $\text{Fin}_S$-colored operad $UWD$ of undirected wiring diagrams is defined (Theorem 7.3.14). The main purpose of this chapter is to establish a finite presentation for the operad $UWD$; see Theorem 10.2.7. This means the following two statements.

1. The 6 generating undirected wiring diagrams (Def. 8.1.7) generate the operad $UWD$. This means that every undirected wiring diagram can be expressed as a finite iterated operadic composition involving only the 6 generators. See Theorem 10.1.12.

2. If an undirected wiring diagram can be operadically generated by the generators in two different ways, then there exists a finite sequence of elementary equivalences (Def. 10.2.1) from the first iterated operadic composition to the other one. See Theorem 10.2.7. An elementary equivalence is induced by either an elementary relation in $UWD$ (Def. 8.2.18) or an operad associativity/unity axiom for the generators.

This finite presentation theorem for $UWD$ is the undirected analogue of the finite presentation theorem for $WD$ (Theorem 5.2.11). As in the directed case, this result leads to a finite presentation theorem for $UWD$-algebras, which we will discuss in Chapter 11.

We will continue to use Notation 3.3.1 for (iterated) operadic compositions.
10.1. Stratified Presentation

In this section, we define a stratified presentation in UWD and show that every undirected wiring diagram has a stratified presentation (Theorem 10.1.12). The following definition is the undirected analogue of Def. 5.1.2.

Motivation 10.1.1. A simplex below is a finite parenthesized word whose alphabets are generating undirected wiring diagrams, in which each pair of parentheses has a well defined associated $\circ_i$-composition. In particular, a simplex has a well defined operadic composition. As we have seen in Chapter 8, it is often possible to express an undirected wiring diagram as an operadic composition of generating undirected wiring diagrams in multiple ways. In other words, an undirected wiring diagram can have many different simplex presentations. We now start to develop the necessary language to say precisely that any two such simplex presentations of the same undirected wiring diagram are equivalent in some way.

Definition 10.1.2. Suppose $n \geq 1$. An $n$-simplex $\Psi$ and its composition $|\Psi| \in UWD$ are defined inductively as follows.

1. A 1-simplex is a generator (Def. 8.1.7) $\psi$. Its composition $|\psi|$ is defined as $\psi$ itself.

2. Suppose $n \geq 2$ and that $k$-simplices for $1 \leq k \leq n-1$ and their compositions in UWD are already defined. An $n$-simplex in UWD is a tuple $\Psi = (\psi_i, i, \phi)$ consisting of
   - an integer $i \geq 1$,
   - a $p$-simplex $\psi_p$ for some $p \geq 1$, and
   - a $q$-simplex $\phi_q$ for some $q \geq 1$
   such that:
     i. $p + q = n$;
     ii. the operadic composition

$$|\Psi| \overset{\text{def}}{=} |\psi| \circ_i |\phi|$$

is defined in UWD (Def. 7.3.5).

The undirected wiring diagram $|\Psi|$ in (10.1.2.1) is the composition of $\Psi$.

A simplex in UWD is an $m$-simplex in UWD for some $m \geq 1$. We say that a simplex $\Psi$ is a presentation of the undirected wiring diagram $|\Psi|$.

Remark 10.1.3. To simplify the presentation, as in Notation 5.1.3 we will sometimes use either

- the right side of (10.1.2.1) or
- even just the list of generators $(\psi_1, \ldots, \psi_n)$ in a simplex in the order in which they appear in (10.1.2.1)
10.1. Stratified Presentation

Example 10.1.4. Elementary relations in UWD (Def. 8.2.18) provide a large source of simplices in UWD. In fact, each side, either left or right, of each elementary relation in UWD is a simplex. For example:

1. The elementary relation (8.2.6.1) says that the 3-simplex
   \[ \lambda_{(Y,x,y)} \circ \left( \theta_{(X,y)} \circ_2 \omega_y \right) \]
   and the 2-simplex
   \[ \lambda_{(Y,x,y)} \circ \sigma^{(Y,x,y)} \]
   have the same composition.

2. The elementary relation (8.2.7.1) says that the 4-simplex
   \[ \lambda_{(W,w,y)} \circ \sigma^{(W,w,x)} \circ \left( \theta_{(X,y)} \circ_2 \omega_y \right) \]
   and the 1-simplex \( 1_X \) have the same composition. In other words, the former has composition \( 1_X \).

Example 10.1.5. In (8.3.1.1) we considered the 5-simplex
\[ \lambda_{(X,x_1,x_2)} \circ \left[ \left( \theta_{(\emptyset,X)} \circ_2 \theta_{(x_1,x_2)} \right) \circ_2 \omega_{x_1} \right] \circ_2 \omega_{x_2}, \]
whose composition has a wasted cable.

Example 10.1.6. In (8.3.2.1) we considered the 5-simplex
\[ \lambda_{(Y\cup X,x_1,x_2)} \circ \left[ \left( \theta_{(Y,X)} \circ_2 \theta_{(x_1,x_2)} \right) \circ_2 \omega_{x_1} \right] \circ_2 \omega_{x_2}, \]
whose composition also has a wasted cable.

Motivation 10.1.7. If we think of a simplex as a parenthesized word whose alphabets are generating undirected wiring diagrams, then the stratified simplex in the next definition is a word where the same alphabets must occur in a consecutive string. For example, all the loops must occur together as a string \( (\lambda_1, \ldots, \lambda_n) \). Furthermore, we can even insist that these strings for different types of generating undirected wiring diagrams occur in a specific order, with name changes and loops at the top, followed by splits, 2-cells, and 1-output wires at the bottom.

Definition 10.1.8. A stratified simplex in UWD is a simplex in UWD (Def. 10.1.2) of one of the following two forms:

1. \((\varepsilon)\), where \( \varepsilon \in \text{UWD}^{(\emptyset)} \) is the empty cell (Def. 8.1.1).
2. \((\tau, \lambda, \sigma, \theta, \omega)\), where:
   - \(\tau\) is a name change (Def. 8.1.3);
   - \(\lambda\) is a possibly empty string of loops (Def. 8.1.5);
   - \(\sigma\) is a possibly empty string of splits (Def. 8.1.6);
10. Finite Presentation for Undirected Wiring Diagrams

- $\theta$ is a possibly empty string of 2-cells (Def. 8.1.4);
- $\omega$ is a possibly empty string of 1-output wires (Def. 8.1.2).

We call these stratified simplices of type (1) and of type (2), respectively. If $\Psi$ is a stratified simplex in UWD, then we call it a stratified presentation of the undirected wiring diagram $[\Psi]$.

**Remark 10.1.9.** The composition of a stratified simplex of type (2) cannot be the empty cell $\epsilon$. Indeed, if the composition of a stratified simplex of type (2) is in $\text{UWD}^\emptyset$, then 1-output wires must be involved. So the composition must have at least one cable, and it cannot be the empty cell.

**Example 10.1.10.** In (8.3.2.1) and (8.3.3.1) we gave two stratified presentations of the undirected wiring diagram $\zeta_\varepsilon \in \text{UWD}(\varepsilon)$ in Example 8.3.2.

**Example 10.1.11.** In (9.1.2.5) we gave a stratified presentation of the undirected wiring diagram $\varphi \in \text{UWD}(X_1, X_2)$.

We now observe that the generators generate the operad UWD of undirected wiring diagrams in a highly structured way.

**Theorem 10.1.12.** Every undirected wiring diagram admits a stratified presentation.

**Proof.** Suppose $\psi$ is an undirected wiring diagram. If $\psi$ is the empty cell $\epsilon$ (Def. 8.1.1), then $(\epsilon)$ is a stratified presentation of $\psi$. So let us now assume that $\psi$ is not the empty cell. We will show that it admits a stratified presentation of type (2). We remind the reader of Convention 9.5.1.

Combining (9.2.3.1) and (9.4.3.1), there is a decomposition

$$\psi = \phi_1 \circ \phi_2 \circ \psi_2.$$}

In this decomposition:

- The undirected wiring diagram $\psi_2$ either is a colored unit or has a stratified presentation $(\theta, \omega)$ by Lemma 9.3.5 and Corollary 9.3.8.
- The undirected wiring diagram $\phi_2$ either is a name change or has a stratified presentation $(\sigma)$ by Prop. 9.5.3.
- The undirected wiring diagram $\phi_1$ either is a name change or has a stratified presentation $(\Lambda)$ by Prop. 9.6.2.

By the above three statements, $\psi$ has a stratified presentation of type (2). \qed

**10.2. Elementary Equivalences**

The purpose of this section is to establish the second part of the finite presentation theorem for the operad UWD of undirected wiring diagrams. Recall the 17
elementary relations in UWD (Def. 8.2.18). In what follows, we will regard each operad associativity or unity axiom as an equality. The following definition is the undirected analogue of Def. 5.2.2.

**Definition 10.2.1.** Suppose Ψ is an n-simplex in UWD as in Def. 10.1.2.

1. A *subsimplex* of Ψ is a simplex in UWD defined inductively as follows.
   - If Ψ is a 1-simplex, then a subsimplex of Ψ is Ψ itself.
   - Suppose n ≥ 2 and Ψ = (ψ, i, φ) for some i ≥ 1, p-simplex ψ, and q-simplex φ with p + q = n. Then a subsimplex of Ψ is
     - a subsimplex of ψ,
     - a subsimplex of φ, or
     - Ψ itself.

   If Ψ′ is a subsimplex of Ψ, then we write Ψ′ ⊆ Ψ.

2. An *elementary subsimplex* Ψ′ of Ψ is a subsimplex of one of two forms:
   - Ψ′ is one side (either left or right) of a specified elementary relation in UWD (Def. 8.2.18).
   - Ψ′ is one side (either left or right) of a specified operad associativity or unity axiom—(2.1.10.3), (2.1.10.4), (2.1.10.5), or (2.1.10.6)—involving only the generators in UWD (Def. 8.1.7).

3. Suppose Φ is another simplex in UWD. Then Ψ and Φ are said to be *equivalent* if their compositions are equal; i.e., |Ψ| = |Φ| ∈ UWD.

4. Suppose:
   - Ψ′ ⊆ Ψ is an elementary subsimplex corresponding to one side of R, which is either an elementary relation or an operad associativity/unity axiom for the generators in UWD.
   - Ψ″ is the simplex given by the other side of R.
   - Ψ¹ is the simplex obtained from Ψ by replacing the subsimplex Ψ′ by Ψ″.

   We say that Ψ and Ψ¹ are *elementarily equivalent*. Note that elementarily equivalent simplices are also equivalent.

5. If Ψ and Φ are elementarily equivalent, we write Ψ ~ Φ and call this an *elementary equivalence*.

6. Suppose Ψ₀, ..., Ψ_r are simplices in UWD for some r ≥ 1 and that there exist elementary equivalences

   Ψ₀ ~ Ψ₁ ~ ... ~ Ψ_r.

Then we say that Ψ₀ and Ψ_r are *connected by a finite sequence of elementary equivalences*. Note that in this case Ψ₀ and Ψ_r are equivalent.

**Example 10.2.2.** By definition, for each elementary relation in UWD (Def. 8.2.18), the simplices given by its two sides are elementarily equivalent. For example:
(1) By the elementary relation (8.2.6.1), replacing an elementary subsimplex of the form
\[ \lambda(Y, x, y) \circ (\theta(x, y) \circ_2 \omega_y) \]
by one of the form
\[ \lambda(Y, x, y) \circ \sigma'(Y, x, y) \]
yields an elementary equivalence.

(2) By the elementary relation (8.2.7.1), replacing an elementary subsimplex of the form
\[ \lambda(W, w, y) \circ \sigma(W, x, w) \circ(\theta(x, y) \circ_2 \omega_y) \]
by the colored unit \(1_X\) yields an elementary equivalence.

**Example 10.2.3.** In Example 8.3.4, we observed that for the undirected wiring diagram \(\zeta_Y \in \text{UWD}(\ell)\) in Example 8.3.2, the stratified presentations (8.3.2.1) and (8.3.3.1) are connected by a finite sequence of elementary equivalences.

**Convention 10.2.4.** As in Convention 5.2.7, to simplify the presentation, elementary equivalences corresponding to an operad associativity/unity axiom–(2.1.10.3), (2.1.10.4), (2.1.10.5), or (2.1.10.6)–for the generators in \(\text{UWD}\) (Def. 8.1.7) will often be applied tacitly wherever necessary.

The goal of this section is to show that any two equivalent simplices in \(\text{UWD}\) are connected by a finite sequence of elementary equivalences. The first step is to show that every simplex in \(\text{UWD}\) is connected to a stratified simplex (Def. 10.1.8) in the following sense. The following observation is the undirected analogue of Lemma 5.2.8.

**Lemma 10.2.5.** Every simplex in \(\text{UWD}\) is either a stratified simplex (Def. 10.1.8) or is connected to an equivalent stratified simplex by a finite sequence of elementary equivalences (Def. 10.2.1).

**Proof.** Suppose \(\Psi\) is a simplex in \(\text{UWD}\) that is not a stratified simplex. Using the three elementary relations (8.2.3.1–8.2.5.1), first we move all the name changes (Def. 3.1.3) in \(\Psi\), if there are any, to the left. Then we use the elementary relation (8.2.1.1) repeatedly to compose them down into one name change. Therefore, after a finite sequence of elementary equivalences, we may assume that there is at most one name change in \(\Psi\), which is the left-most entry. If there are further elementary equivalences later that create name changes, we will perform the same procedure without explicitly mentioning it.

The empty cell \(\epsilon \in \text{UWD}(\emptyset)\) (Def. 8.1.1) and a 1-output wire \(\omega_* \in \text{UWD}(\ast)\) (Def. 8.1.2) have no input boxes, so no operadic composition of the forms \(\epsilon \circ_i \) or \(\omega_* \circ_i \) can be defined. Therefore, after a finite sequence of elementary equivalences corresponding to the operad horizontal associativity axiom (2.1.10.3), we may assume
that $\Psi$ has the form

$$\left(\tau, \Psi^1, \varepsilon, \omega\right).$$

Here:

- $\tau$ is a name change;
- all the 1-output wires $\omega$ are at the right-most entries;
- all the empty cells $\varepsilon$ are just to their left;
- $\Psi^1$ is either empty or is a subsimplex involving 2-cells (Def. 8.1.4), loops (Def. 8.1.5), and splits (Def. 8.1.6).

Next we use the elementary relations (8.2.9.1)–(8.2.12.1) to move all the 2-cells in $\Psi$ to just the left of $\varepsilon$. Then we use the elementary relations (8.2.15.1) and (8.2.17.1) to move all the remaining loops to just the right of the name change $\tau$. So after a finite sequence of elementary equivalences, we may assume that the simplex $\Psi$ has the form

$$\left(\tau, \lambda, \sigma, \theta, \varepsilon, \omega\right). \quad (10.2.5.1)$$

If the string $\varepsilon$ of empty cells is empty, then we are done because this is now a stratified simplex of type (2).

So suppose the string $\varepsilon$ of empty cells in (10.2.5.1) is non-empty. Using finitely many elementary equivalences corresponding to the elementary relations (8.2.8.1)–(8.2.10.1), we may cancel all the unnecessary empty cells in (10.2.5.1). If there are no empty cells left after the cancellation, then we have a stratified simplex of type (2).

Suppose that, after the cancellation in the previous paragraph, the resulting string $\varepsilon$ of empty cells is still non-empty. Then it must contain a single empty cell $\varepsilon$, and there are no 2-cells $\theta$ and no 1-output wires $\omega$ in the resulting simplex $\Psi$. Since the output box of $\varepsilon$ is the empty box, the current simplex $\Psi$ cannot have any loops $\lambda$ or splits $\sigma$. Therefore, in this case the simplex (10.2.5.1) has the form

$$\left(\tau, \varepsilon\right).$$

Since the output box of $\varepsilon$ is the empty box $\emptyset$, this name change $\tau$ must be the colored unit $\mathbb{1}_\emptyset$. So by the operad left unity axiom (2.1.10.5), the simplex $\left(\mathbb{1}_\emptyset, \varepsilon\right)$ is elementarily equivalent to $(\varepsilon)$, which is a stratified simplex of type (1). \qed

The next step is to show that equivalent stratified simplices are connected. The following observation is the undirected analogue of Lemmas 5.2.9 and 5.2.10.

**Lemma 10.2.6.** Any two equivalent stratified simplices (Def. 10.1.8) in UWD are either equal or are connected by a finite sequence of elementary equivalences (Def. 10.2.1).

**Proof.** Suppose $\Psi^1$ and $\Psi^2$ are equivalent stratified simplices in UWD. By Remark 10.1.9 $\Psi^1$ and $\Psi^2$ are both of type (1) or both of type (2). If they are both of type (1),
then they are both equal to $(e)$ by definition. So let us now assume that $\Psi^1$ and $\Psi^2$ are distinct but equivalent stratified simplices of type (2) in UWD. The rest of the proof is similar to that of Lemma 5.2.10 and consists of a series of reductions.

Write $\psi \in \text{UWD}(\Lambda_X)$ for the common composition of $\Psi^1$ and $\Psi^2$. Using elementary equivalences corresponding to

- the operad unity axioms (2.1.10.5) and (2.1.10.6),
- the elementary relations (8.2.7.1) and (8.2.8.1) regarding colored units, and
- other elementary relations in UWD that move the generators around the stratified simplices,

we may assume that there are no unnecessary generators in these stratified simplices. Here unnecessary refers to either a colored unit or generators whose (iterated) operadic composition is a colored unit. If $\psi$ itself is a name change $\tau$, then at this stage both $\Psi^1$ and $\Psi^2$ are equal to the 1-simplex $(\tau)$. So let us now assume that $\psi$ is not a name change.

The name change $\tau^1$ in $\Psi^1$ has output box $Y$, and the same is true for the name change $\tau^2$ in $\Psi^2$. We may actually assume that the input boxes of $\tau^1$ and of $\tau^2$ are also equal, provided that we change the output boxes of other generators in $\Psi^2$ accordingly by a name change if necessary. Such changes correspond to elementary equivalences coming from the operad unity and associativity axioms and the elementary relation (8.2.1.1). Using finitely many elementary equivalences, we may therefore assume that $\tau^1$ is equal to $\tau^2$. So we may as well assume that there are no name changes in the two stratified simplices $\Psi^i$. At this stage, each stratified simplex $\Psi^i$ has the form

$$(\lambda^i, \omega^i, \theta^i, \omega^i).$$

Using finitely many elementary equivalences corresponding to the elementary relation (8.2.6.1) and other elementary relations that move the generators around, we may assume that in the simplices $\Psi^1$ and $\Psi^2$ all the $(1,0)$-cables in $\psi$ are created as in the left side of (8.2.6.1), i.e., as $(\lambda, \theta, \omega)$ rather than as $(\lambda, \sigma)$. In plain language, this means that every $(1,0)$-cable in $\psi$ is created in both $\Psi^i$ by applying a loop to a 1-output wire and some other wire, rather than by applying a loop to a split.

Similarly, using Example 8.3.4 and finitely many elementary equivalences, we may further assume that every wasted cable in $\psi$ is created in both simplices $\Psi^i$ as $(\lambda, \theta, \omega, \omega)$ as in (8.3.2.1), rather than as $(\lambda, \sigma, \theta, \omega)$ as in (8.3.3.1). In plain language, this means that every wasted cable in $\psi$ is created in both $\Psi^i$ by applying a loop to two 1-output wires, as in the first picture after (8.3.2.1).

Recall that each 1-output wire $\omega$ is a 0-ary element in UWD, while loops and splits are unary. Therefore, by the operad associativity axioms (2.1.10.3) and (2.1.10.4),
we may assume that in each simplex $\Psi^i$, the right portion $(\theta^i, \omega^i)$ is a subsimplex. By the above reductions, at this stage the two simplices $(\theta^1, \omega^1)$ and $(\theta^2, \omega^2)$ are uniquely determined by $\psi$ and have the same composition. In fact, each simplex $(\theta^i, \omega^i)$ has composition $\psi_2$ (9.2.2.3). Using finitely many elementary equivalences corresponding to the elementary relations (8.2.9.1) and (8.2.10.1) and the operad associativity axioms, we may now assume that the simplices $(\theta^1, \omega^1)$ and $(\theta^2, \omega^2)$ are equal.

Similarly, at this stage the simplices $(\lambda^1, \sigma^1)$ and $(\lambda^2, \sigma^2)$ both have composition $\psi_1$ (9.2.2.2). Using finitely many elementary equivalences corresponding to the elementary relations (8.2.13.1)–(8.2.17.1) and the operad vertical associativity axiom (2.1.10.4), we may now assume that the simplices $(\lambda^1, \sigma^1)$ and $(\lambda^2, \sigma^2)$ are equal. □

We are now ready for the finite presentation theorem for undirected wiring diagrams. It describes the operad UWD of undirected wiring diagrams (Theorem 7.3.14) in terms of finitely many generators and finitely many relations.

**Theorem 10.2.7.** Consider the operad UWD of undirected wiring diagrams.

1. Every undirected wiring diagram can be obtained from finitely many generators (Def. 8.1.7) via iterated operadic compositions (Def. 2.1.10).

2. Any two equivalent simplices in UWD are either equal or are connected by a finite sequence of elementary equivalences (Def. 10.2.1).

**Proof.** The first statement is a special case of Theorem 10.1.12. The second statement is a combination of Lemma 10.2.5 twice and Lemma 10.2.6 □

10.3. Summary of Chapter

1. A simplex in UWD is a finite non-empty parenthesized word of generating undirected wiring diagrams in which each pair of parentheses is equipped with an operadic $\circ_i$-composition.

2. A stratified simplex in UWD is a simplex of one of the following two forms.
   - $(\epsilon)$
   - $(\tau, \lambda, \sigma, \theta, \omega)$

3. Every undirected wiring diagram has a stratified presentation.

4. Two simplices in UWD are elementarily equivalent if one can be obtained from the other by replacing a subsimplex $\Psi'$ by an equivalent simplex $\Psi''$ such that $|\Psi'| = |\Psi''|$ is either one of the seventeen elementary relations in UWD or an operad associativity/unity axiom involving only the six generating undirected wiring diagrams.
(5) Any two simplex presentations of a given undirected wiring diagram are connected by a finite sequence of elementary equivalences.
Chapter 11

Algebras of Undirected Wiring Diagrams

The main purpose of this chapter is to provide a finite presentation theorem for algebras over the operad $UWD$ of undirected wiring diagrams (Theorem 7.3.14). As in the case of wiring diagrams (Theorem 6.2.2), this finite presentation for $UWD$-algebras is a consequence of the finite presentation for the operad $UWD$ (Theorem 10.2.7). This finite presentation allows us to reduce the understanding of a $UWD$-algebra to just a few basic structure maps and a small number of easy-to-check axioms. We will illustrate this point further with the relational algebra of a set and the typed relational algebra.

In Section 11.1 we first define a $UWD$-algebra in terms of 6 generating structure maps and 17 generating axioms corresponding to the generators (Def. 8.1.7) and the elementary relations (Def. 8.2.18) in $UWD$. Then we observe that this finite presentation for a $UWD$-algebra is in fact equivalent to the general definition (Def. 6.1.3) of a $UWD$-algebra (Theorem 11.1.2). This is an application of the finite presentation theorem for the operad $UWD$ (Theorem 10.2.7).

In Section 11.2 we provide, for each set $A$, a finite presentation for the $UWD$-algebra called the relational algebra of $A$ (Theorem 11.2.5). In its original form, the relational algebra was the main algebra example in [Spi13]. In [Spi13] Spivak pointed out that the relational algebra of a set and its variant called the typed relational algebra, to be discussed in Section 11.4, have applications in digital circuits, machine learning, and database theory.

In Section 11.3 we prove a rigidity property of the relational algebra of a set (Theorem 11.3.3). It says that a given map of sets is a bijection precisely when it
induces a map between the two relational algebras. The motivation for this rigid-
ity property comes from [Spi13] Section 3, where several examples suggest that
there are very few interesting maps out of the relational algebra of a set. In fact, in
[Spi13] Conjecture 3.1.6, Spivak conjectured that the relational algebra of any set
is quotient-free. Although our rigidity result does not prove Spivak’s conjecture in
its full generality, it adds further evidence that the conjecture should be true.

In Section 11.4 we consider a generalization of the relational algebra of a set,
called the typed relational algebra. We observe that, similar to the relational algebra
of a set, the typed relational algebra has a finite presentation (Theorem 11.4.7). In
its original form, the typed relational algebra was first defined in [Spi13] Section 4.

11.1. Finite Presentation for Algebras

The main purpose of this section is to prove a finite presentation theorem for UWD-
algebras. We first define a UWD-algebra in terms of a finite number of generators
and relations. Immediately afterwards we will show that this definition agrees
with the general definition of an operad algebra (Def. 6.1.3) when the operad is
UWD.

Fix a class $S$, with respect to which the $\text{Fin}_S$-colored operad $\text{UWD}$ of undirected
wiring diagrams is defined (Theorem 7.3.14).

Definition 11.1.1. A UWD-algebra $A$ consists of the following data. For each
$X \in \text{Fin}_S$, $A$ is equipped with a set $A_X$ called the $X$-colored entry of $A$. Moreover, it
is equipped with the following 6 generating structure maps corresponding to the
generators in UWD (Def. 8.1.7).

(1) Corresponding to the empty cell $\epsilon \in \text{UWD}(\emptyset)$ (Def. 8.1.1), it has a structure
map
\[ * \xrightarrow{\epsilon} A_{\emptyset}, \]

i.e., a chosen element in $A_{\emptyset}$.

(2) Corresponding to each 1-output wire $\omega_* \in \text{UWD}(\ast)$ (Def. 8.1.2), it has a
structure map
\[ * \xrightarrow{\omega_*} A_* , \]

i.e., a chosen element in $A_*$.

(3) Corresponding to each name change $\tau_f \in \text{UWD}(\underline{X})$ (Def. 8.1.3), it has a
structure map
\[ A_X \xrightarrow{\tau_f} A_Y \]

that is, furthermore, the identity map if $f$ is the identity map on $X$. 
(4) Corresponding to each 2-cell $\theta_{(X,Y)} \in \text{UWD}^{(X,Y)}$ (Def. 8.1.4), it has a structure map

$$A_X \times A_Y \xrightarrow{\theta_{(X,Y)}} A_{X \cup Y}.$$  \hspace{1cm} \text{(11.1.1.4)}

(5) Corresponding to each loop $\lambda_{(X,x)} \in \text{UWD}^{(X,x)}$ (Def. 8.1.5), it has a structure map

$$A_X \xrightarrow{\lambda_{(X,x)}} A_{X \setminus x}.$$  \hspace{1cm} \text{(11.1.1.5)}

(6) Corresponding to each split $\sigma^{(X,x_1,x_2)} \in \text{UWD}^{(X)}$ (Def. 8.1.6), it has a structure map

$$A_{X'} \xrightarrow{\sigma^{(X,x_1,x_2)}} A_X.$$  \hspace{1cm} \text{(11.1.1.6)}

The following 17 diagrams, called the *generating axioms*, which correspond to the elementary relations in UWD (Def. 8.2.18), are required to be commutative.

1. In the setting of (8.2.1.1), the diagram

$$
\begin{array}{ccc}
A_X & \xrightarrow{\tau_f} & A_Y \\
\downarrow{\tau_g} & & \downarrow{\tau_g} \\
A_Z
\end{array}
$$

is commutative.

2. In the setting of (8.2.2.1), the diagram

$$
\begin{array}{ccc}
* & \xrightarrow{\omega_x} & A_X \\
\downarrow{\omega_y} & & \downarrow{\tau_{x,y}} \\
A_y
\end{array}
$$

is commutative.

3. In the setting of (8.2.3.1), the diagram

$$
\begin{array}{ccc}
A_{X_1} \times A_{X_2} & \xrightarrow{\theta_{(X_1,X_2)}} & A_{X_1 \cup X_2} \\
\downarrow{(\tau_{f_1},\tau_{f_2})} & & \downarrow{\tau_{f_1 \cup f_2}} \\
A_{Y_1} \times A_{Y_2} & \xrightarrow{\theta_{(Y_1,Y_2)}} & A_{Y_1 \cup Y_2}
\end{array}
$$

is commutative.
In the setting of (8.2.4.1), the diagram

\[
\begin{array}{ccc}
A_X & \xrightarrow{\lambda_{(X,x)}} & A_{X \setminus x} \\
\downarrow \tau_f & & \downarrow \tau_f' \\
A_Y & \xrightarrow{\lambda_{(Y,y)}} & A_{Y \setminus y}
\end{array}
\]

is commutative.

In the setting of (8.2.5.1), the diagram

\[
\begin{array}{ccc}
A_{X'} & \xrightarrow{\rho(X,x_1,x_2)} & A_X \\
\downarrow \tau_f' & & \downarrow \tau_f \\
A_{Y'} & \xrightarrow{\rho(Y,y_1,y_2)} & A_Y
\end{array}
\]

is commutative.

In the setting of (8.2.6.1), the diagram

\[
\begin{array}{ccc}
A_X \times * & \xrightarrow{\mu(X,y)} & A_Y \\
\downarrow (Id,\omega_y) & & \downarrow \lambda_{(Y,x,y)} \\
A_X \times A_y & \xrightarrow{\theta_{(X,y)}} & A_Y \lambda_{(Y,x,y)}
\end{array}
\]

is commutative.

In the setting of (8.2.7.1), the diagram

\[
\begin{array}{ccc}
A_X & \xrightarrow{\theta_{(X,y)}} & A_Y \\
\downarrow Id & & \downarrow \rho(y,x,w) \\
A_X & \xrightarrow{\lambda_{(W,w,y)}} & A_W
\end{array}
\]

is commutative.

In the setting of (8.2.8.1), the diagram

\[
\begin{array}{ccc}
A_X & \xrightarrow{=} & A_X \times * \\
\downarrow Id & & \downarrow (Id,\epsilon) \\
A_X & \xrightarrow{\theta_{(X,\emptyset)}} & A_X \times A_{\emptyset}
\end{array}
\]

is commutative.
(9) In the setting of (8.2.9.1), the diagram

\[
\begin{array}{c}
A_X \times A_Y \times A_Z \\
(\theta_{(X,Y)}, \text{Id}) \\
A_{XuY} \times A_Z \\
\end{array} \xrightarrow{(\text{Id}, \theta_{(Y,Z)})} \begin{array}{c}
A_X \times A_{YuZ} \\
\theta_{(X,YuZ)} \\
A_{XuYuZ} \\
\end{array}
\]

is commutative.

(10) In the setting of (8.2.10.1), the diagram

\[
\begin{array}{c}
A_Y \times A_X \xrightarrow{\text{permute}} A_X \times A_Y \\
\theta_{(Y,X)} \\
A_{YuX} \\
\end{array} \xrightarrow{=} \begin{array}{c}
A_{XuY} \\
\theta_{(X,Y)} \\
A_{XuY} \\
\end{array}
\]

is commutative.

(11) In the setting of (8.2.11.1), the diagram

\[
\begin{array}{c}
A_X \times A_Y \\
(\text{Id}, \lambda_{(Y,z)}) \\
A_X \times A_{Y'} \\
\theta_{(X,Y')} \\
A_{XuY'} \\
\end{array} \xrightarrow{\lambda_{(X,Y',y)}} \begin{array}{c}
A_{XuY} \\
\theta_{(X,Y)} \\
A_{XuY} \\
\end{array}
\]

is commutative.

(12) In the setting of (8.2.12.1), the diagram

\[
\begin{array}{c}
A_X \times A_{Y'} \\
(\text{Id}, \sigma^{(Y,y_1,y_2)}) \\
A_X \times A_Y \\
\theta_{(X,Y)} \\
A_{XuY} \\
\end{array} \xrightarrow{\sigma^{(X,Y,y_1,y_2)}} \begin{array}{c}
A_{XuY'} \\
\sigma^{(X,Y,y_1,y_2)} \\
A_{XuY'} \\
\end{array}
\]

is commutative.

(13) In the setting of (8.2.13.1), the diagram

\[
\begin{array}{c}
A_X \\
\sigma^{(Y,y_1,y_2)} \\
A_{Y'} \\
\end{array} \xrightarrow{\sigma^{(Z,z_1,z_2)}} \begin{array}{c}
A_Y \\
\sigma^{(X,Y,y_1,y_2)} \\
A_{XuY} \\
\end{array} \xrightarrow{\sigma^{(X,Y,y_1,y_2)}} \begin{array}{c}
A_{YuZ} \\
\sigma^{(X,Y,y_1,y_2)} \\
A_{XuYuZ} \\
\end{array}
\]

is commutative.
(14) In the setting of (8.2.14.1), the diagram

\[
\begin{array}{c}
A_X \xrightarrow{\sigma(Y_1, y_{12})} A_Y \\
\downarrow_{\sigma(Y_1, y_{12})} \quad \downarrow_{\sigma(Y_2, y_{23})} \\
A_{Y_1} \xrightarrow{\sigma(Y_2, y_{23})} A_Y
\end{array}
\]

is commutative.

(15) In the setting of (8.2.15.1), the diagram

\[
\begin{array}{c}
A_X \xrightarrow{\lambda(X, x_+)} A_{X'} \\
\downarrow_{\lambda(Y', x_+)} \quad \downarrow_{\lambda(Y, x_+)} \\
A_{Y'} \xrightarrow{\lambda(Y', x_+)} A_Y
\end{array}
\]

is commutative.

(16) In the setting of (8.2.16.1), the diagram

\[
\begin{array}{c}
A_X \xrightarrow{\sigma(W, y, x_+)} A_W \\
\downarrow_{\sigma(W, y, x_+)} \quad \downarrow_{\sigma(W, x_+)} \\
A_W \xrightarrow{\lambda(W, x_+)} A_Y
\end{array}
\]

is commutative.

(17) In the setting of (8.2.17.1), the diagram

\[
\begin{array}{c}
A_X \xrightarrow{\lambda(X, x_1, x_2)} A_Z \\
\downarrow_{\lambda(X, x_1, x_2)} \quad \downarrow_{\lambda(Z, x_1, x_2)} \\
A_W \xrightarrow{\lambda(W, x_3, x_4)} A_Y
\end{array}
\]

is commutative.

This finishes the definition of a UWD-algebra.

At this moment we have two definitions of a UWD-algebra.

- On the one hand, in Def. [6.1.3] with \( O = \text{UWD} \), a UWD-algebra has a structure map \( \mu_\zeta \) for each undirected wiring diagram \( \zeta \in \text{UWD} \). This structure map satisfies the associativity axiom \( (6.1.2.1) \) for a general operadic composition in UWD, together with the unity and the equivariance axioms in Def. [6.1.2].

- On the other hand, in Def. [11.1.1] a UWD-algebra has 6 generating structure maps and satisfies 17 generating axioms.
11.1. Finite Presentation for Algebras

We now observe that these two definitions are equivalent, so UWD-algebras indeed have a finite presentation as in Def. 11.1.1.

**Theorem 11.1.2.** For the operad UWD of undirected wiring diagrams (Theorem 7.3.14), Def. 6.1.3 with \( O = \text{UWD} \) and Def. 11.1.1 of a UWD-algebra are equivalent.

**Proof.** This proof proceeds as in the proof of Theorem 6.2.2. First suppose \((A, \mu)\) is a UWD-algebra in the sense of Def. 6.1.3. To see that it is also a UWD-algebra in the sense of Def. 11.1.1, first note that the structure map \( \mu \) (11.1.2.1) gives the 6 generating structure maps (11.1.1.1)–(11.1.1.6). Moreover, the generating structure map \( \mu_1 \) (11.1.1.3) is the identity map by the unity axiom (6.1.2.3).

The generating axiom (11.1.1.9) is a special case of the equivariance diagram (6.1.2.4), so it is commutative. Each of the other 16 generating axioms corresponds to an elementary relation in UWD that describes two different ways to construct the same undirected wiring diagram as an iterated operadic composition of generators in UWD. Each such generating axiom asserts that the two corresponding compositions of generating structure maps—defined using the composition in the diagram (6.1.3.1)—are equal. The associativity axiom (6.1.3.1) of \((A, \mu)\) applied twice guarantees that two such compositions are indeed equal.

Conversely, suppose \( A \) is a UWD-algebra in the sense of Def. 11.1.1, so it has 6 generating structure maps that satisfy 17 generating axioms. We must show that it is a UWD-algebra in the sense of Def. 6.1.3. For an undirected wiring diagram \( \psi \in \text{UWD} \) with a presentation \( \Psi \) (Def. 10.1.2), we define its structure map \( \mu_\psi \) (6.1.2.1) inductively as follows.

1. If \( \Psi \) is a 1-simplex, then \( \Psi = (\psi) \), and \( \psi \) is a generator in UWD by definition. In this case, we define \( \mu_\psi \) as the corresponding generating structure map (11.1.1.1)–(11.1.1.6) of \( A \).

2. Inductively, suppose \( \Psi \) is an \( n \)-simplex for some \( n \geq 2 \), so \( \Psi = (\Phi, i, \Theta) \) for some \( i \geq 1 \), \( p \)-simplex \( \Phi \), and \( q \)-simplex \( \Theta \) with \( p + q = n \). Since \( 1 \leq p, q < n \), by the induction hypothesis, the structure maps \( \mu_{|\Phi|} \) and \( \mu_{|\Theta|} \) are already defined. Then we define the structure map

\[
\mu_\psi = \mu_{|\Phi|} \circ i \mu_{|\Theta|}
\]

(11.1.2.1) as in Notation 6.1.4

By Theorem 10.1.12 every undirected wiring diagram has a stratified presentation, hence a presentation. To see that the structure map \( \mu_\psi \) as above is well-defined, we need to show that the map \( \mu_\psi \) is independent of the choice of a presentation \( \Psi \). Any two presentations of an undirected wiring diagram are by definition equivalent simplices. By Theorem 10.2.7 (2) (= the relations part of the finite presentation theorem for UWD), any two equivalent simplices in UWD are either equal or are connected by a finite sequence of elementary equivalences. Therefore, it
suffices to show that every elementary equivalence in UWD yields a commutative diagram involving the generating structure maps of $A$, where $\circ_i$ is interpreted as in Notation 6.1.4. Recall from Def. 10.2.1 that an elementary equivalence comes from either an elementary relation in UWD or an operad associativity/unity axiom for the generators in UWD.

It follows from a direct inspection that the operad associativity and unity axioms—(2.1.10.3), (2.1.10.4), (2.1.10.5), and (2.1.10.6)—for the generators yield commutative diagrams involving the generating structure maps of $A$. In fact, the diagrams involving the horizontal and the vertical associativity axioms (2.1.10.3) and (2.1.10.4) are commutative because composition of functions is associative. The diagrams for the two unity axioms (2.1.10.5) and (2.1.10.6) are commutative because the generating structure map for a colored unit (11.1.1.3) is required to be the identity map.

By definition each of the 17 generating axioms of $A$ corresponds to an elementary relation (Def. 8.2.18) and is a commutative diagram. Therefore, the structure map $\mu_\psi$ for each wiring diagram $\psi$ is well-defined.

It remains to check that the structure map $\mu$ satisfies the required unity, equivariance, and associativity axioms. The unity axiom (6.1.2.3) holds because it is part of the assumption on the generating structure map corresponding to a name change (11.1.1.3).

The associativity axiom (6.1.3.1) holds because the structure map $\mu_\psi$ is defined above (11.1.2.1) by requiring that the diagram (6.1.3.1) be commutative.

For the equivariance axiom (6.1.2.4), first note that it is enough to check it when the undirected wiring diagram in question is an iterated operadic composition of 2-cells. This is because 2-cells are the only binary generators in UWD (Remark 8.1.8). All other generators are either 0-ary or unary, for which equivariance is trivial.

So now suppose $\zeta$ in the equivariance axiom (6.1.2.4) is an iterated operadic composition of 2-cells. If $\zeta$ is a 2-cell and the permutation $\sigma$ is the transposition $(1 2) \in \Sigma_2$, then the equivariance axiom (6.1.2.4) is true by the generating axiom (11.1.1.9). The general case now follows from this special case using:

- the generating axiom (11.1.1.8) corresponding to the associativity property of 2-cells (8.2.9.1);
- the operad associativity axioms (2.1.10.3) and (2.1.10.4) when applied to 2-cells;
- the fact that the transpositions $(i, i+1)$ for $1 \leq i \leq n - 1$ generate the symmetric group $\Sigma_n$.

So $(A, \mu)$ is a UWD-algebra in the sense of Def. 6.1.3. □
Remark 11.1.3. The proofs of the finite presentation theorems [11.1.2 and 6.2.2] for UWD-algebras and WD-algebras are almost identical. In fact, it is not difficult to formulate and prove a more general result that has both of these finite presentation theorems as special cases. Such a result would say that, if an operad $O$ has a finite presentation (i.e., specific finite sets of generators and generating relations expressed in terms of simplices and elementary equivalences similar to Def. 10.1.2 and 10.2.1), then $O$-algebras have a corresponding finite presentation. We purposely chose not to present the material this way in order to avoid the higher level of abstraction that is unnecessary for actual applications of (undirected) wiring diagrams. Although the context is slightly different, the formulation and proof of such a finite presentation theorem for $O$-algebras can be extracted from the Strong Biased Definition Theorem in \cite{YJ15} page 193.

11.2. Finite Presentation for the Relational Algebra

The purpose of this section is to provide an illustration of Theorem 11.1.2, the finite presentation theorem of UWD-algebras, using the relational algebra. This algebra was originally introduced as the main algebra example in \cite{Spi13} using Def. 6.1.2. We will describe the relational algebra in terms of 6 generating structure maps and 17 generating axioms. First we need some notations.

**Definition 11.2.1.** Suppose $A$ and $X$ are sets.

1. $A^X = \text{Set}(X, A)$ is the set of functions $X \rightarrow A$.
2. An element $u \in A^X$ is called an $X$-vector in $A$, and $u(x) \in A$ is called the $x$-entry of $u$ for $x \in X$.
3. $\mathcal{P}(X) = \{T \subseteq X\}$ is the set of subsets of $X$, called the power set of $X$.
4. $\text{Rel}_A(X) = \mathcal{P}(A^X)$ is the power set of the set $A^X$ of $X$-vectors in $A$.

**Example 11.2.2.** Suppose $A, B, X, Y$ are sets and $*$ is a one-element set.

1. Since $A^\varnothing = \ast$, it follows that
   \[ \text{Rel}_A(\varnothing) = \mathcal{P}(\ast) = \{\varnothing, \ast\}. \] \hspace{1cm} (11.2.2.1)
2. Since $A^\ast = A$, it follows that
   \[ \text{Rel}_A(\ast) = \mathcal{P}(A), \] \hspace{1cm} (11.2.2.2)
   the power set of $A$.
3. There is a canonical bijection
   \[ A^X \times A^Y \cong A^{X \times Y}. \] \hspace{1cm} (11.2.2.3)
4. Suppose $h : X \rightarrow Y$ is a function.
(i) There is an induced map \( h^* : A^Y \to A^X \) sending each map \( Y \to A \) to the composition of \( X \to Y \to A \); i.e., \( h^* \) is pre-composition with \( h \).

(ii) Likewise, there is an induced map

\[
\begin{array}{c}
\text{Rel}_A(Y) \\
\xrightarrow{h^*}
\end{array}
\begin{array}{c}
\text{Rel}_A(X)
\end{array}
\]

given by pre-composition with \( h \).

(5) Suppose \( p : A \to B \) is a function.

(i) There is an induced map \( p_* : A^X \to B^X \) sending each map \( X \to A \) to the composition \( X \to A \to B \); i.e., \( p_* \) is post-composition with \( p \).

(ii) Likewise, there is an induced map

\[
\begin{array}{c}
\text{Rel}_A(X) \\
\xrightarrow{p_*}
\end{array}
\begin{array}{c}
\text{Rel}_B(Y)
\end{array}
\]

given by post-composition with \( p \).

**Assumption 11.2.3.** Throughout this section, \( S \) is the one-element set. So \( \text{Fin}_S = \text{Fin} \) is the collection of finite sets, and \( \text{UWD} \) is a \( \text{Fin} \)-colored operad (Theorem 7.3.14).

We now define the relational algebra in terms of finitely many generating structure maps and generating axioms.

**Definition 11.2.4.** Suppose \( A \) is a set. The relational algebra of \( A \), denoted \( \text{Rel}_A \), is the \( \text{UWD} \)-algebra in the sense of Def. 11.1.1 defined as follows. For each finite set \( X \), the \( X \)-colored entry is

\[
\text{Rel}_A(X) = \{ \varnothing, * \}
\]

as in Def. 11.2.1. Its 6 generating structure maps are defined as follows.

1. For the empty cell \( \epsilon \in \text{UWD}(\varnothing) \) (Def. 8.1.1), the chosen element in \( \text{Rel}_A(\varnothing) = \{ \varnothing, * \} \) is \( * \).

2. For a 1-output wire \( \omega_* \in \text{UWD}(\cdot) \) (Def. 8.1.2), the chosen element in \( \text{Rel}_A(\cdot) = \emptyset(A) \) is \( A \).

3. For a bijection \( f : X \to Y \in \text{Fin} \) and the name change \( \tau_f \in \text{UWD}(\cdot) \) (Def. 8.1.3), the generating structure map is the pre-composition map (11.2.2.4)

\[
\begin{array}{c}
\text{Rel}_A(X) \\
\xrightarrow{\tau_f = (f^{-1})^*}
\end{array}
\begin{array}{c}
\text{Rel}_A(Y)
\end{array}
\]

In other words, each \( X \)-vector in \( A \) is reindexed as a \( Y \)-vector in \( A \) using the bijection \( f \).
(4) For a 2-cell \( \theta_{(X,Y)} \in \text{UWD}(\frac{X \times Y}{X,Y}) \) (Def. 8.1.4), the generating structure map is defined using the bijection (11.2.2.3) as follows.

\[
\begin{array}{ccc}
\text{Rel}_A(X) \times \text{Rel}_A(Y) & (U \subseteq A^X, V \subseteq A^Y) & \\
\downarrow \theta_{(X,Y)} & & \\
\text{Rel}_A(X \cup Y) & (U \times V \subseteq A^X \times A^Y \cong A^{X \cup Y}) & \\
\end{array}
\]

In other words, concatenate every given \( X \)-vector with every given \( Y \)-vector to form an \( (X \cup Y) \)-vector.

(5) For a loop \( \lambda_{(X,x)} \in \text{UWD}(\frac{X,x}{X}) \) (Def. 8.1.5), the generating structure map is defined as

\[
\begin{array}{ccc}
\text{Rel}_A(X) & (U \subseteq A^X) & \\
\downarrow \lambda_{(X,x)} & & \\
\text{Rel}_A(X \setminus x) & \{u \setminus x : u \in U, u(x_+) = u(x_-)\} \subseteq A^{X \setminus x} & \\
\end{array}
\]

in which \( u \setminus x \) is the composition

\[
X \setminus x \xrightarrow{\text{inclusion}} X \xrightarrow{u} A.
\]

In other words, for a given subset of \( X \)-vectors in \( A \), look for those whose \( x_+ \)-entry and \( x_- \)-entry are equal, and then delete these two entries to form a subset of \( (X \setminus x) \)-vectors.

(6) For a split \( \sigma_{(X,x_1,x_2)} \in \text{UWD}(\frac{X}{X}) \) (Def. 8.1.6), denote by \( p : X \rightarrow X' \) the projection map that sends both \( x_1, x_2 \in X \) to \( x \in X' \) and is the identity function everywhere else. The generating structure map is defined as the pre-composition map (11.2.2.4)

\[
\begin{array}{ccc}
\text{Rel}_A(X') & \sigma_{(X,x_1,x_2)} = p^* & \\
\downarrow & & \\
\text{Rel}_A(X) & & \\
\end{array}
\]

In other words, for a given subset of \( X' \)-vectors in \( A \), use the \( x \)-entry for both the \( x_1 \)-entry and the \( x_2 \)-entry to form a subset of \( X \)-vectors.

The following observation is the finite presentation theorem for the relational algebra of a set.

**Theorem 11.2.5.** For each set \( A \), the relational algebra \( \text{Rel}_A \) in Def. 11.2.4 is actually a UWD-algebra in the sense of Def. 11.1.1 hence also in the sense of Def. 6.1.3 by Theorem 11.1.2.

**Proof.** We need to check that \( \text{Rel}_A \) satisfies the 17 generating axioms in Def. 11.1.1. Due to the simplicity of the 6 generating structure maps, all the generating axioms
can be checked by a direct inspection. For example, the generating axiom (11.1.1.7), which corresponds to the elementary relation (8.2.6.1), is the assertion that the diagram

\[
\begin{array}{ccc}
\text{Rel}_A(X) \times \ast & \cong & \text{Rel}_A(Y) \\
\downarrow \text{(Id,ω)} & & \downarrow \sigma(\lambda,\lambda) \\
\text{Rel}_A(X) \times \text{Rel}_A(Y) & \xrightarrow{\theta_{(\lambda,\lambda)}} & \text{Rel}_A(Y) \\
\downarrow \lambda_{(\lambda,\lambda)} & & \downarrow \lambda_{(\lambda,\lambda)} \\
\text{Rel}_A(W) & & \text{Rel}_A(W)
\end{array}
\]

is commutative, where \( X = Y \setminus y \) and \( W = Y \setminus \{x, y\} = X \setminus x \). For each element \( U \subseteq A^X \) \( \in \text{Rel}_A(X) \), one can check that both compositions in the above diagram send \( U \) to the element

\[
\left\{ W \xrightarrow{\text{inclusion}} X \xrightarrow{u} A : u \in U \right\} \subseteq A^W
\]

in \( \text{Rel}_A(W) \). The other 16 generating axioms are checked similarly. \( \square \)

**Remark 11.2.6.** To see that our relational algebra \( \text{Rel}_A \) in Def. 11.2.4 agrees with the one in \([Spi13]\) Example 2.2.10, note that the latter is based on Def. 6.1.2, which is equivalent to Def. 6.1.3. A direct inspection of \([Spi13]\) Eq. (11) reveals that Spivak’s structure map of \( \text{Rel}_A \), when applied to the 6 generators in UWD (Def. 8.1.7), reduces to our generating structure maps in Def. 11.2.4. Theorem 11.2.5 then guarantees that the two definitions of the relational algebra \( \text{Rel}_A \)–i.e., our Def. 11.2.4 and \([Spi13]\) Example 2.2.10–are equivalent.

### 11.3. Spivak’s Conjecture: Rigidity of the Relational Algebra

The purpose of this section is to partially verify a conjecture in \([Spi13]\) (Conjecture 3.1.6) that states that the relational algebra \( \text{Rel}_A \) in Def. 11.2.4 is quotient-free. To state this conjecture, we first need the definition of a map between operad algebras. Recall from Section 6.1 the definition of an operad algebra.

**Definition 11.3.1.** Suppose \( O \) is an \( S \)-colored operad, and \( (A, \mu^A) \) and \( (B, \mu^B) \) are \( O \)-algebras. A **map of \( O \)-algebras** \( f : A \longrightarrow B \) consists of a collection of maps

\[
\left\{ A_c \xrightarrow{f_c} B_c : c \in S \right\}
\]

that is compatible with the structure maps in the following sense.
Compatibility with Structure Maps: For each \( d \in S, \zeta = (c_1, \ldots, c_n) \in \text{Prof}(S) \), and \( \zeta \in \mathcal{O}^{d} \), the diagram

\[
\begin{array}{ccc}
\prod_{i=1}^{n} A_{c_i} & \xrightarrow{\prod f_i} & \prod_{i=1}^{n} B_{c_i} \\
\mu_{\zeta}^A & \downarrow & \mu_{\zeta}^B \\
A_{d} & \xrightarrow{f_d} & B_{d}
\end{array}
\]

is commutative.

Furthermore, we call \( f \) an isomorphism if there exists a map of \( \mathcal{O} \)-algebras \( g : B \rightarrow A \) such that \( gf = \text{Id}_A \) and \( fg = \text{Id}_B \). If such a map \( g \) exists, then it is necessarily unique.

The following conjecture regarding the relational algebra is [Spi13] Conjecture 3.1.6. Since we are talking about the relational algebra, here \( S \) is a one-element set, and \( \text{UWD} \) is a Fin-colored operad.

**Conjecture 11.3.2.** Suppose:

- \( A \) is a set, and \( \text{Rel}_A \) is the relational algebra of \( A \) in Def. 11.2.4.
- \( f : \text{Rel}_A \rightarrow B \) is a map of \( \text{UWD} \)-algebras.

Then at least one of the following two statements holds.

1. \( f \) is an isomorphism.
2. \( B_X \) is a one-element set for each finite set \( X \).

Roughly speaking this conjecture states that there are no interesting maps out of any relational algebra. In the following observation, we will verify Conjecture 11.3.2 in the special case when the map \( \text{Rel}_A \rightarrow B \) is induced by a map of sets out of \( A \).

**Theorem 11.3.3.** Suppose \( f : A \rightarrow B \) is a map of sets. Then the following statements are equivalent.

1. \( f \) is a bijection of sets.
2. The post-composition maps \( f_* : \text{Rel}_A(X) \rightarrow \text{Rel}_B(X) \) (11.2.2.5), with \( X \) running through all the finite sets, form an isomorphism of \( \text{UWD} \)-algebras.
3. The post-composition maps \( f_* : \text{Rel}_A(X) \rightarrow \text{Rel}_B(X) \), with \( X \) running through all the finite sets, form a map of \( \text{UWD} \)-algebras.

**Proof.** The implications (1) \( \Rightarrow \) (2) \( \Rightarrow \) (3) are both immediate from the definitions. It remains to check the implication (3) \( \Rightarrow \) (1). So let us now assume that
$f_* : \text{Rel}_A \longrightarrow \text{Rel}_B$ is a map of UWD-algebras. This means that the diagram

$$
\begin{array}{c}
\prod_{i=1}^{n} \text{Rel}_A(X_i) \\
\downarrow \mu_\zeta^A \\
\text{Rel}_A(Y) \\
\end{array} \xrightarrow{f_Y} 
\begin{array}{c}
\prod_{i=1}^{n} \text{Rel}_B(X_i) \\
\downarrow \mu_\zeta^B \\
\text{Rel}_B(Y) \\
\end{array}
$$

(11.3.3.1)
is commutative for each $\zeta \in \text{UWD}(Y)$ with $X = (X_1, \ldots, X_n)$. We will consider two special cases, which will show that $f$ is surjective and injective.

1. To show that $f$ is surjective, consider a 1-output wire $\omega_* \in \text{UWD}(*)$ (Def. 8.1.2). In this case, the commutative diagram (11.3.3.1) becomes the diagram

$$
\begin{array}{c}
* \\
\downarrow \omega_*^A \\
\text{Rel}_A(*) = \mathcal{P}(A) \\
\end{array} \xrightarrow{f_*} 
\begin{array}{c}
* \\
\downarrow \omega_*^B \\
\text{Rel}_B(*) = \mathcal{P}(B) \\
\end{array}
$$
in which

$$\omega_*^A(*) = A \in \mathcal{P}(A) \quad \text{and} \quad \omega_*^B(*) = B \in \mathcal{P}(B)$$

by Def. 11.2.4 The bottom horizontal map $f_*$ is post-composition with $f$, so it sends each subset $U \subseteq A$ to its image $f(U) \subseteq B$. Therefore, the commutativity of the above diagram forces

$$f(A) = f_*(A) = B,$$

so $f$ is surjective.

2. To show that $f$ is injective, we argue by contradiction. So suppose there exist distinct elements $a_+, a_- \in A$ such that $f(a_+) = f(a_-) \in B$. We will show that this assumption leads to a contradiction. Consider the loop $\lambda_{(A,a_+)} \in \text{UWD}(A,a_+)$ (Def. 8.1.5). In this case, the commutative diagram (11.3.3.1) becomes the diagram

$$
\begin{array}{c}
\text{Rel}_A(A) \\
\downarrow \lambda_{(A,a_+)} \\
\text{Rel}_A(A \setminus a_+) \\
\end{array} \xrightarrow{f_*} 
\begin{array}{c}
\text{Rel}_B(A) \\
\downarrow \lambda_{(A,a_+)} \\
\text{Rel}_B(A \setminus a_+) \\
\end{array}
$$
in which both horizontal maps $f_*$ are post-composition with $f$. Consider the element

$$U = \{ A \overset{=} \longrightarrow A \} \in \text{Rel}_A(A) = \mathcal{P}(A^A),$$

which is the single-element set consisting of the identity map of $A$. We will show that the two compositions in (11.3.3.2) do not agree at $U$. 
On the one hand, since $a_+ \neq a_-$, applying the left vertical map to $U$ yields

$$\lambda_{(A,a_+)}(U) = \emptyset \subseteq A^{A \setminus a_+}$$

by the definition of the generating structure map for a loop (11.2.4.1). Applying the bottom horizontal map $f_*$ in (11.3.3.2) yields

$$f_*\lambda_{(A,a_+)}(U) = \emptyset \subseteq B^{A \setminus a_+}.$$ 

On the other hand, applying the top horizontal map $f_*$ to $U$ yields

$$f_*(U) = \left\{ A \xrightarrow{f} B \right\} \in \mathcal{R}_B(A) = \mathcal{P}(B^A),$$

which is the single-element set consisting of the map $f$. Since $f(a_+) = f(a_-)$, applying the right vertical map now yields the single-element set

$$\lambda_{(A,a_+)}f_*(U) = \left\{ A \setminus a_+ \xrightarrow{\text{inclusion}} A \xrightarrow{f} B \right\} \subseteq B^{A \setminus a_+}$$

by (11.2.4.1). Since this is not empty, the two compositions in the commutative diagram (11.3.3.2) do not agree at the element $U$. This is a contradiction, so the map $f$ is injective.

□

Example 11.3.4. Let us provide a simple illustration of the non-commutativity of the diagram (11.3.3.2) for the non-injective function $f : A = \{0,1\} \rightarrow \{\ast\} = B$ that sends both 0 and 1 to $\ast$. Consider the singleton $U = \{\text{Id}_A\} \in \mathcal{P}(A^A) = \mathcal{R}_A(A)$. Since $0 \neq 1$, we have

$$f_*\lambda_{(A,0,1)}U = f_*(\emptyset) = \emptyset \in \mathcal{P}(B^\emptyset) = \mathcal{R}_B(\emptyset).$$

On the other hand, $f_*U$ is the singleton $\{f\} \in \mathcal{P}(B^A) = \mathcal{R}_B(A)$ with $f(0) = f(1)$. So

$$\lambda_{(A,0,1)}f_*U = \lambda_{(A,0,1)}\{f\} = \left\{ \emptyset \rightarrow B \right\} \in \mathcal{P}(B^\emptyset) = \mathcal{R}_B(\emptyset),$$

which contains one element. So $\lambda_{(A,0,1)}f_* \neq f_*\lambda_{(A,0,1)}$, and the diagram (11.3.3.2) in this case is not commutative. In particular, this non-injective function $f$ does not induce a map of UWD-algebras $\mathcal{R}_A \rightarrow \mathcal{R}_B$.

11.4. Finite Presentation for the Typed Relational Algebra

The relational algebra $\mathcal{R}_A$ in Def. 11.2.4 has a fixed set $A$ as the set of potential values in each coordinate in an $X$-vector (Def. 11.2.1). There is a more general version of the relational algebra, called the typed relational algebra, in which each coordinate in an $X$-vector has its own set of potential values. The typed relational algebra was first introduced in [Spi13] (Section 4) using Def. 6.1.2. In this section, we observe that the typed relational algebra also has a finite presentation, similar to the one for the relational algebra in Theorem 11.2.5.
Assumption 11.4.1. Throughout this section, \( S \) is the collection of sets, so \( \text{UWD} \) is the \( \text{Fin}_{\text{Set}} \)-colored operad of undirected wiring diagrams (Theorem 7.3.14).

Definition 11.4.2. Suppose \((X, v) \in \text{Fin}_{\text{Set}}\) (Def. 2.2.6), so \( X \) is a finite set and \( v : X \rightarrow \text{Set} \) assigns to each \( x \in X \) a set \( v(x) \).

1. Define the set
   \[ X_v = \prod_{x \in X} v(x) \quad (11.4.2.1) \]
   in which an empty product, for the case \( X = \emptyset \), means the one-point set.

2. An element in \( X_v \) is also called an \( X \)-vector.

3. For \( x \in X \), the \( x \)-entry of an \( X \)-vector \( u \) is denoted by \( u_x \).

As before, we will omit writing \( v \) in \((X, v)\) if there is no danger of confusion.

Example 11.4.3. Suppose \( A \) is a set and \((X, v) \in \text{Fin}_{\text{Set}}\) such that \( v(x) = A \) for all \( x \in X \). Then

\[ X_v = \prod_{x \in X} A = A^X \]

as in Def. 11.2.1.

Example 11.4.4. Each map \( f : (X, v) \rightarrow (Y, v) \in \text{Fin}_{\text{Set}} \) induces a map

\[ Y_v = \prod_{y \in Y} v(y) \xrightarrow{f_v} \prod_{x \in X} v(x) = X_v. \quad (11.4.4.1) \]

For \((a_y)_{y \in Y} \in Y_v\) with each \( a_y \in v(y)\), its image is defined as

\[ f_v((a_y)_{y \in Y}) = (a_{f(x)})_{x \in X} \]

using the fact that \( a_{f(x)} \in v(f(x)) = v(x) \). If \( A \) is a set and \( v(y) = v(x) = A \) for all \( y \in Y \) and \( x \in X \), then \( f_v \) is the pre-composition map in Example 11.2.2. In what follows, a map induced by the map \( f_v \) will often be denoted by \( f_v \) as well.

We now define the typed relational algebra in terms of finitely many generating structure maps and generating axioms.

Definition 11.4.5. The typed relational algebra \( \text{Rel} \) is the \( \text{UWD} \)-algebra in the sense of Def. 11.1.1 defined as follows. For each \((X, v) \in \text{Fin}_{\text{Set}}\), the \( X \)-colored entry is

\[ \text{Rel}(X) = \wp(X_v) \]

with \( X_v \) as in (11.4.2.1) and \( \wp(\cdot) \) the power set (Def. 11.2.1). Its 6 generating structure maps are defined as follows.

1. For the empty cell \( \varepsilon \in \text{UWD}(\emptyset) \) (Def. 8.1.1), the chosen element in
   \[ \text{Rel}(\emptyset) = \wp(\emptyset_v) = \wp(*) = \{\emptyset, *\} \]
   is \(*\).
(2) For a 1-output wire \( \omega_1 \in UWD(X) \) (Def. 8.1.2), the chosen element in \( \text{Rel}(x) = \mathcal{V}(v(x)) \) is \( v(x) \).

(3) For a bijection \( f : X \rightarrow Y \in \text{Fin}_{\text{Set}} \) and the name change \( \tau_f \in UWD(Y) \) (Def. 8.1.3), the generating structure map is the bijection

\[
\text{Rel}(X) = \mathcal{V}(X_v) \xrightarrow{\tau_f = f_v^{-1}} \mathcal{V}(Y_v) = \text{Rel}(Y)
\]

induced by \( f_v^{-1} \) as in (11.4.4.1).

(4) For a 2-cell \( \theta: X \rightarrow Y \subseteq UWD(X) \) (Def. 8.1.4), the generating structure map is defined as follows.

\[
\begin{array}{ccc}
\text{Rel}(X) \times \text{Rel}(Y) & \xrightarrow{\theta(X,Y)} & \text{Rel}(X \cup Y) \\
(U \subseteq X_v, V \subseteq Y_v) & & (U \times V \subseteq X_v \times Y_v = (X \cup Y)_v)
\end{array}
\]

(5) For a loop \( \lambda_{(X,x_\pm)} \in UWD(X \times X) \) (Def. 8.1.5), the generating structure map is defined as

\[
\begin{array}{ccc}
\text{Rel}(X) & \xrightarrow{\lambda_{(X,x_\pm)}} & \text{Rel}(X \setminus x_\pm) \\
(U \subseteq X_v) & & \{ u_{\setminus x_\pm} : u \in U, u_{x_\pm} = u_{x_{\pm}} \} \subseteq (X \setminus x_\pm)_v
\end{array}
\]

in which \( u_{\setminus x_\pm} \) is obtained from \( u \) by deleting the \( x_\pm \)-entries. In other words, if \( i : (X \setminus x_\pm) \rightarrow X \) is the inclusion map, then

\[
u_{\setminus x_\pm} = i_v(u)
\]

provided \( u_{x_\pm} = u_{x_{\pm}} \), where \( i_v \) is as in (11.4.4.1).

(6) For a split \( \sigma^{(X,x_1,x_2)} \in UWD(X) \) (Def. 8.1.6), denote by \( p: X \rightarrow X' \) the projection map that sends both \( x_1, x_2 \in X \) to \( x \in X' \) and is the identity function everywhere else. The generating structure map is the map

\[
\text{Rel}(X') \xrightarrow{\sigma^{(X,x_1,x_2)} = p_v} \text{Rel}(X)
\]

induced by \( p_v \) in (11.4.4.1). In other words, \( \sigma^{(X,x_1,x_2)} \) takes each \( X' \)-vector \( u \) in any given subset of \( X' \)-vectors to the \( X \)-vector whose \( x_1 \)-entry and \( x_2 \)-entry are both equal to the \( x \)-entry of \( u \), and all other entries remain the same.

**Example 11.4.6.** Suppose \( A \) is a set and \( (X,v) \in \text{Fin}_{\text{Set}} \) such that \( v(x) = A \) for all \( x \in X \). Then

\[
\text{Rel}(X) = \mathcal{V}(X_v) = \mathcal{V}(A^X) = \text{Rel}_A(X),
\]
the X-colored entry of the relational algebra of $A$ (Def. 11.2.4). Furthermore, if in Def. 11.4.5 all the value assignments $v$ take the constant value $A$, then the 6 generating structure maps of Rel reduce to those of $\text{Rel}_A$ in Def. 11.2.4.

The following observation is the finite presentation theorem for the typed relational algebra.

**Theorem 11.4.7.** The typed relational algebra $\text{Rel}$ in Def. 11.4.5 is actually a UWD-algebra in the sense of Def. 11.1.1, hence also in the sense of Def. 6.1.3 by Theorem 11.1.2.

**Proof.** As in the proof of Theorem 11.2.5 for the relational algebra of $A$, we just need to check that $\text{Rel}$ satisfies the 17 generating axioms in Def. 11.1.1. Due to the simplicity of the 6 generating structure maps, all the generating axioms can be checked by a direct inspection. For example, the generating axiom (11.1.1.7), which corresponds to the elementary relation (8.2.6.1), is the assertion that the diagram

$$
\begin{array}{ccc}
\text{Rel}(X) \times \ast & \cong & \text{Rel}(X) \\
\downarrow & & \downarrow \\
\text{Rel}(X) \times \text{Rel}(y) & \rightarrow & \lambda_{Y,x,y} \downarrow \\
\text{Rel}(Y) & \rightarrow & \text{Rel}(W) \\
\end{array}
$$

is commutative, where $X = Y \setminus y$ and $W = Y \setminus \{x, y\} = X \setminus x$. For each element $U \subseteq X_v = \prod v(x) \in \text{Rel}(X)$, one can check that both compositions in the above diagram send $U$ to the element

$$\{\iota_U(u) : u \in U\} \subseteq W_v$$

in $\text{Rel}(W)$, where $\iota : W \rightarrow X$ is the inclusion map and $\iota_U$ as in (11.4.4.1). The other 16 generating axioms are checked similarly. $\square$

**Remark 11.4.8.** To see that our relational algebra $\text{Rel}$ in Def. 11.4.5 agrees with the one in [Spi13] Section 4, note that the latter is based on Def. 6.1.2, which is equivalent to Def. 6.1.3. A direct inspection of [Spi13] Lemma 4.1.2 reveals that Spivak’s structure map of $\text{Rel}$, when applied to the 6 generators in UWD (Def. 8.1.7), reduces to our generating structure maps in Def. 11.4.5. Theorem 11.4.7 then guarantees that the two definitions of the relational algebra $\text{Rel}$—i.e., our Def. 11.4.5 and [Spi13] Section 4—are equivalent.

### 11.5. Summary of Chapter 11

1. Each UWD-algebra can be described using six generating structure maps and seventeen generating axioms.

2. The (typed) relational algebra is a UWD-algebra.

3. Spivak’s Conjecture holds when restricted to relational algebras.
Part 3

Maps Between Operads of Wiring Diagrams
So far we have considered four operads constructed from wiring diagrams and undirected wiring diagrams:

1. the $\text{Box}_S$-colored operad of wiring diagrams $\text{WD}$ (Theorem 2.3.11);
2. the $\text{Box}_S$-colored operad of normal wiring diagrams $\text{WD}_\bullet$ (Prop. 5.3.5);
3. the $\text{Box}_S$-colored operad of strict wiring diagrams $\text{WD}_0$ (Prop. 5.4.6);
4. the $\text{Fin}_S$-colored operad of undirected wiring diagrams $\text{UWD}$ (Theorem 7.3.14).

The purpose of this part is to study maps between these operads. We will show that there is a commutative diagram

\[
\begin{array}{ccc}
\text{WD}_0 & \longrightarrow & \text{WD}_\bullet \\
\downarrow_{\chi^0} & & \downarrow_{\chi} \\
\text{UWD} & \longrightarrow & \text{WD} \\
\uparrow_{\rho} & & \\
\end{array}
\]

of operad maps, in which the horizontal maps are operad inclusions. All the operad maps in this diagram except $\rho$ are discussed in Chapter 12. The operad map $\rho$ is discussed in Chapter 13. The existence of such operad maps implies that:

- Every $\text{UWD}$-algebra induces a $\text{WD}$-algebra along $\rho$.
- Every $\text{WD}$-algebra restricts to a $\text{WD}_\bullet$-algebra.
- Every $\text{WD}_\bullet$-algebra restricts to a $\text{WD}_0$-algebra.

For each of the three operad maps that end at $\text{UWD}$, we will compute precisely the image. An undirected wiring diagram is in the image of

- $\chi^0$ if and only if its cables are either $(1, 1)$-cables or $(2, 0)$-cables;
- $\chi$ if and only if it has no $(0, 0)$-cables and no $(0, \geq 2)$-cables.

Furthermore, the operad map $\rho : \text{WD} \rightarrow \text{UWD}$ is surjective, so every undirected wiring diagram is the $\rho$-image of some wiring diagram. Delay nodes play a crucial role in the surjectivity of the operad map $\rho$.

Reading Guide. The reader who already knows about operad maps may skip most of Section 12.1 and go straight to Propositions 12.1.7 and 12.1.9. Instead of the proof of Theorem 12.2.4 about the existence of the operad map $\chi$, the reader may wish to concentrate on the motivating Example 12.2.1. Likewise, the proofs of Theorems 12.4.1 and 12.5.1 about the images of the operad maps $\chi$ and $\chi^0$ may be skipped during the first reading.

Instead of the proof of Theorem 13.1.4 on the existence of the operad map $\rho$, the reader may wish to concentrate on the motivating Example 13.1.1. Likewise, before
reading the proof of Theorem 13.3.3 on the surjectivity of the map \( \rho \), the reader may wish to first read the illustrating Example 13.3.4.
Chapter 12

Map from Normal to Undirected Wiring Diagrams

This chapter has three main purposes.

1. We show that there exists an operad map $\chi : WD_* \to UWD$ from the operad $WD_*$ of normal wiring diagrams to the operad $UWD$ of undirected wiring diagrams. See Theorem 12.2.4. Recall that a normal wiring diagram is a wiring diagram with no delay nodes. Intuitively, the map $\chi$ is given by forgetting directions.

2. We compute precisely the image of the operad map $\chi : WD_* \to UWD$ in Theorem 12.4.1. An undirected wiring diagram is in the image of $\chi$ if and only if it has no wasted cables and no $(0, \geq 2)$-cables.

3. We consider the restriction $\chi^0 : WD_0 \to UWD$ of the operad map $\chi : WD_* \to UWD$ to the operad $WD_0$ of strict wiring diagrams and compute precisely its image in Theorem 12.5.1. An undirected wiring diagram is in the image of $\chi^0$ if and only if its cables are either $(1, 1)$-cables or $(2, 0)$-cables.

In Theorem 13.1.4 we will extend the operad map $\chi : WD_* \to UWD$ to an operad map $\rho : WD \to UWD$ defined for all wiring diagrams. Furthermore, we will show in Theorem 13.3.3 that the operad map $\rho : WD \to UWD$ is surjective.

In Section 12.1 we define a map of operads and observe that there are inclusions of operads $WD_0 \to WD_* \to WD$. Furthermore, if the underlying class $S$ changes,
then there are corresponding maps of operads for each of the four operads of (un-der-rected) wiring diagrams.

Section 12.2 contains the first main result Theorem 12.2.4 of this chapter. It says that there is a map of operads \( \chi : WD_\bullet \to UWD \) defined by forgetting directions.

In Section 12.3 we provide a series of examples to illustrate the operad map \( \chi \).

Section 12.4 contains the second main result Theorem 12.4.1 of this chapter. This result identifies precisely the image of the operad map \( \chi : WD_\bullet \to UWD \) consisting of the undirected wiring diagrams with no wasted cables and no \((0, \geq 2)\)-cables.

In Section 12.5 we consider the restriction of the operad map \( \chi \) to the operad \( WD_0 \) of strict wiring diagrams. Recall that a strict wiring diagram is a wiring diagram with no delay nodes and whose supplier assignment is a bijection. In Theorem 12.5.1 we will show that the image of the operad map \( WD_0 \to UWD \) consists of precisely the undirected wiring diagrams with only \((1, 1)\)-cables and \((2, 0)\)-cables.

12.1. Operad Maps

In this section, we define an operad map and record some obvious maps among the various operads of (undirected) wiring diagrams (Prop. 12.1.7 and 12.1.9). Recall from Def. 2.1.10 the definition of an \( S \)-colored operad.

Definition 12.1.1. Suppose \( O \) is an \( S \)-colored operad and \( P \) is a \( T \)-colored operad. A map of operads, also called an operad map, \( f : O \to P \) consists of a pair of maps \((f_0, f_1)\) as follows.

1. \( f_0 : S \to T \), called the color map.
2. For each \( d \in S \) and \( \underline{c} = (c_1, \ldots, c_n) \in \text{Prof}(S) \) with \( n \geq 0 \), it has a map, called an entry map,

\[
O^{(\underline{c})}(d) \xrightarrow{f_1} P^{(f_0\underline{c})}
\]

in which \( fd = f_0d \in T \) and \( f\underline{c} = (f_0c_1, \ldots, f_0c_n) \in \text{Prof}(T) \).

We will usually write both \( f_0 \) and \( f_1 \) as \( f \). These maps are required to preserve the operad structure in the sense that the following three conditions hold.
12.1. Operad Maps

**Preservation of Equivariance:** For each \((d, c) \in \text{Prof}(S) \times S\) as above and permutation \(\sigma \in \Sigma_n\), the diagram

\[
\begin{array}{c}
\text{O}(d, c) \xrightarrow{f} P(f^d, f^c) \\
\downarrow \cong \downarrow \cong \\
\text{O}(d, c) \xrightarrow{f} P(f^d, f^c)
\end{array}
\]

is commutative, in which \(f \sigma = (f c_{\sigma(1)}, \ldots, f c_{\sigma(n)})\).

**Preservation of Colored Units:** For each \(c \in S\),

\[ f 1_c = 1_{f c} \]

in which \(1_c \in \text{O}(c)\) is the \(c\)-colored unit in \(O\) and \(1_{f c} \in P(f^c)\) is the \((f c)\)-colored unit in \(P\).

**Preservation of Operadic Composition:** For each \((d, c) \in \text{Prof}(S) \times S\) with \(|c| \geq 1\), \(b \in \text{Prof}(S)\), and \(1 \leq i \leq |c|\), the diagram

\[
\begin{array}{c}
\text{O}(d, c) \times \text{O}(c) \xrightarrow{(f, f)} P(f^d, f^c) \times P(f^c) \\
\downarrow o_i \downarrow o_i \\
\text{O}(d, c) \xrightarrow{f} P(f^d, f^c)
\end{array}
\]

is commutative.

**Definition 12.1.2.** Suppose \(O\) is an \(S\)-colored operad and \(P\) is a \(T\)-colored operad.

1. A map of operads \(f : O \to P\) is called an operad inclusion if the color map \(f_0 : S \to T\) and all the entry maps \(f_1\) are inclusions.

2. If there exists an operad inclusion \(O \to P\), then we call \(O\) a sub-operad of \(P\).

**Example 12.1.3.** With the one-point set \(*\) as the set of color, there is an operad \(T\) in which every entry \(T(*, *, \ldots, *) = *\). Then for each colored operad \(O\), there exists a unique map of operads \(O \to T\). In category theoretical terms, \(T\) is a terminal object in the category of all colored operads.

**Example 12.1.4.** There is an operad \(I\) with the empty set as its set of color, and \(I\) has no entries because it has no colors. Then for each colored operad \(O\), there exists a unique operad inclusion \(I \to O\). In category theoretical terms, \(I\) is an initial object in the category of all colored operads.

**Example 12.1.5.** Suppose \(f : O \to P\) and \(g : P \to Q\) are maps of operads. Composing the color maps and the entry maps, there is a composition map of operads \(gf : O \to Q\).
Example 12.1.6. Suppose $f : O \to P$ is an operad map as in Def. 12.1.1 and $A = \{ A_t \}_{t \in T}$ is a $P$-algebra as in Def. 6.1.2 or Def. 6.1.3. Then there is an induced $O$-algebra $A^f$ defined by the following data.

1. For each $c \in S$, $A^f_c$ is equipped with the $c$-colored entry $A^f_c = A_{fc}$.
2. For each $(c_1, \ldots, c_n) \in \text{Prof}(S) \times S$ and $\zeta \in O(c_1, \ldots, c_n)$, $A^f$ is equipped with the structure map

$$A^f_{c_1} \times \cdots \times A^f_{c_n} = A_{fc_1} \times \cdots \times A_{fc_n} \xrightarrow{\mu^f_\zeta = \mu_f \zeta} A_{fd} = A^f_d.$$ 

Here $\mu_f$ is the $P$-algebra structure map of $A$, and $f \zeta \in P(f(c_1, \ldots, c_n))$. Since an operad map is assumed to preserve all the operad structure, a direct inspection reveals that $A^f$ is indeed an $O$-algebra.

We say that the $O$-algebra $A^f$ is induced along $f$.

In the next two observations, we record some obvious operad maps among the various operads of (undirected) wiring diagrams.

Recall the $\text{Box}_S$-colored operad $WD$ of wiring diagrams (Theorem 2.3.11), the $\text{Box}_S$-colored operad $WD_\bullet$ of normal wiring diagrams (Prop. 5.3.5), and the $\text{Box}_S$-colored operad $WD_0$ of strict wiring diagrams (Prop. 5.4.6). Remember that a normal wiring diagram is a wiring diagram without delay nodes, and a strict wiring diagram is a normal wiring diagram whose supplier assignment is a bijection. Also recall that $WD^S$ means the operad of $S$-wiring diagrams, and the symbol $S$ is suppressed from the notation $WD^S$ unless we need to emphasize it. Similar remarks apply to $WD_0^S$ and $WD_\bullet^S$.

**Proposition 12.1.7.** Given a map $f : S \to T$ of classes, there exists an induced commutative diagram

$$
\begin{array}{ccc}
WD_0^S & \xrightarrow{f_*} & WD_\bullet^S \\
\downarrow{f_*} & & \downarrow{f_*} \\
WD_T^T & \xrightarrow{f_*} & WD_T^T
\end{array}
$$

(12.1.7.1)

of maps of operads in which:

- the horizontal maps are operad inclusions;
- the vertical maps are induced by $f$ on value assignments.

**Proof.** In each row of the diagram (12.1.7.1), the maps on colors (i.e., either $\text{Box}_S$ or $\text{Box}_T$) are the identity map. For a fixed class, a strict wiring diagram is by definition also a normal wiring diagram, which by definition is also a wiring diagram. In each of $WD_0$ and $WD_\bullet$, the operad structure—i.e., the equivariant structure, the colored
12.2. Normal to Undirected Wiring Diagrams

Fix a class $S$ for the rest of this chapter, with respect to which the operad $\mathcal{WD}_\bullet$ of normal wiring diagrams (Prop. 5.3.5) and the operad $\mathcal{UWD}$ of undirected wiring diagrams (Theorem 7.3.14) are defined. Recall that a normal wiring diagram is a wiring diagram without delay nodes. The purpose of this section is to construct a map of operads $\mathcal{WD}_\bullet \rightarrow \mathcal{UWD}$ given by forgetting directions (Theorem 12.2.4). The existence of such a map of operads was hinted at in the discussion in [RS13] Section 4.1.

Example 12.2.1. To motivate the definition of the map of operads $\mathcal{WD}_\bullet \rightarrow \mathcal{UWD}$ to be defined below, consider the following normal wiring diagram.

units, and the operad composition—i s defined as that in $\mathcal{WD}$ (Def. 2.3.1–2.3.4). So the horizontal entrywise inclusions actually define operad inclusions.

For the vertical maps in the diagram (12.1.7.1), first note that $f$ induces maps $\text{Fin}_S \rightarrow \text{Fin}_T$ and $\text{Box}_S \rightarrow \text{Box}_T$ that are the identity map on the underlying finite sets. On value assignments, these maps are post-composition with $f$. A direct inspection reveals that, using these two maps, every (strict/normal) $S$-wiring diagram is sent to a (strict/normal) $T$-wiring diagram. Moreover, all the operad structure (Def. 2.3.1–2.3.4) is preserved by these maps. So the vertical entrywise defined maps in the diagram (12.1.7.1) are maps of operads. The commutativity of the diagram is immediate from the definitions of the operad maps.

Example 12.1.8. By Example [12.1.6] and Prop. [12.1.7] every $\mathcal{WD}$-algebra (Def. 6.2.1) restricts to a $\mathcal{WD}_\bullet$-algebra (Def. 6.4.1), and every $\mathcal{WD}_\bullet$-algebra restricts to a $\mathcal{WD}_0$-algebra (Def. 6.6.1). For example, the propagator algebra (Def. 6.3.11), which is a $\mathcal{WD}$-algebra, restricts to a $\mathcal{WD}_\bullet$-algebra and also to a $\mathcal{WD}_0$-algebra.

Recall that $\mathcal{UWD}^S$ is the $\text{Fin}_S$-colored operad of undirected $S$-wiring diagrams (Theorem 7.3.14), and the symbol $S$ in $\mathcal{UWD}^S$ is dropped unless we need to emphasize $S$. Essentially the same as in Prop. [12.1.7] we have the following operad maps for undirected wiring diagrams.

Proposition 12.1.9. Given a map $f : S \rightarrow T$ of classes, there exists an induced map of operads

$$\mathcal{UWD}^S \longrightarrow \mathcal{UWD}^T.$$

Example 12.1.10. Suppose $S = \ast$, a one-point set, and $T = \text{Set}$, the collection of sets. Then the inclusion $\ast \rightarrow \text{Set}$ induces an operad inclusion $\mathcal{UWD}_\ast \rightarrow \mathcal{UWD}^{\ast\text{Set}}$. In [Spi13] Example 2.1.7, $\mathcal{UWD}_\ast$ is denoted by $S$ and is called the operad of singly-typed wiring diagrams. In [Spi13] Example 4.1.1, $\mathcal{UWD}^{\ast\text{Set}}$ is denoted by $T$ and is called the operad of typed wiring diagrams.

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Example 12.1.8. By Example [12.1.6] and Prop. [12.1.7] every $\mathcal{WD}$-algebra (Def. 6.2.1) restricts to a $\mathcal{WD}_\bullet$-algebra (Def. 6.4.1), and every $\mathcal{WD}_\bullet$-algebra restricts to a $\mathcal{WD}_0$-algebra (Def. 6.6.1). For example, the propagator algebra (Def. 6.3.11), which is a $\mathcal{WD}$-algebra, restricts to a $\mathcal{WD}_\bullet$-algebra and also to a $\mathcal{WD}_0$-algebra.
Here

\[ X_1^{\text{in}} = \{x_{11}^{\text{in}}, x_{12}^{\text{in}}, x_{13}^{\text{in}}\}, \quad X_1^{\text{out}} = \{x_{11}^{\text{out}}, x_{12}^{\text{out}}\}, \quad X_2^{\text{in}} = \{x_2^{\text{in}}\}, \quad \text{and} \quad X_2^{\text{out}} = \{x_2^{\text{out}}\}. \]

The supplier assignment of \( \varphi \) (Def. 2.2.13), \( s : \text{Dm}_\varphi \rightarrow \text{Sp}_\varphi \), is given by

- \( y_1 = s(x_{12}) = s(x_2^{\text{in}}); \)
- \( x_{11}^{\text{out}} = s(x_{11}^{\text{in}}) = s(y_1); \)
- \( x_2^{\text{out}} = s(y_2) = s(x_{13}^{\text{in}}). \)

Note that \( y_2 \in Y^{\text{in}} \) is an external wasted wire, and \( x_{12}^{\text{out}} \in X_1^{\text{out}} \) is an internal wasted wire.

A natural way to make \( \varphi \) into an undirected wiring diagram is to forget the directions of all the arrows. For instance, we send

\[ Y = (Y^{\text{in}}, Y^{\text{out}}) = (\{y_1, y_2\}, \{y_1, y_2, y_3\}) \in \text{Box}_S \]

to

\[ \overline{Y} = Y^{\text{in}} \uplus Y^{\text{out}} = \{y_1, y_2, y_1, y_2, y_3\} \in \text{Fin}_S, \]

and similarly we send \( X_i \in \text{Box}_S \) to \( \overline{X_i} = X_i^{\text{in}} \uplus X_i^{\text{out}} \in \text{Fin}_S \) for \( i = 1, 2 \). So we have

\[ \overline{X_1} = \{x_{11}^{\text{in}}, x_{12}^{\text{in}}, x_{13}^{\text{in}}, x_{11}^{\text{out}}, x_{12}^{\text{out}}\} \quad \text{and} \quad \overline{X_2} = \{x_2^{\text{in}}, x_2^{\text{out}}\}. \]

Inserting cables at appropriate places, we obtain the following undirected wiring diagram.
Call the two cables on the left, from top to bottom, \(c_1\) and \(c_2\) and the three cables on the right, also from top to bottom, \(c_3\), \(c_4\), and \(c_5\). Then on the left side \(c_1\) is a \((2, 1)\)-cable, and \(c_2\) is a \((0, 1)\)-cable. On the right side, \(c_3\), \(c_4\), and \(c_5\) are a \((2, 1)\)-cable, a \((1, 0)\)-cable, and a \((2, 2)\)-cable (Def. 7.1.2), respectively.

Note that the set of cables \(\{c_1, \ldots, c_5\}\) in \(\phi\) is in canonical bijection with the set of supply wires in \(\phi\) (Def. 2.2.13), namely

\[
\text{Sp}_\psi = Y^\text{in} \cup X_1^\text{out} \cup X_2^\text{out} \in \text{Fin}_S.
\]

With this identification, the input and output soldering functions of \(\phi\) are completely determined by the identity map on \(\text{Sp}_\psi\) and the supplier assignment of \(\phi\). We will make this precise in (12.2.2.3) below.

With the previous example as motivation, we now define the map of operads \(\text{WD}_* \rightarrow \text{UWD}\). Recall the definitions of normal wiring diagrams (Def. 2.2.13 and 5.3.1) and of undirected wiring diagrams (Def. 7.1.2 and 7.1.4).

**Definition 12.2.2.** Fix a class \(S\).

1. Define the map \(\chi_0 : \text{Box}_S \rightarrow \text{Fin}_S\) by

\[
\chi_0 Y = Y = Y^\text{in} \cup Y^\text{out} \in \text{Fin}_S
\]

for each \(Y = (Y^\text{in}, Y^\text{out}) \in \text{Box}_S\).

2. For each \((X_{x, \ldots, x_n}) \in \text{Prof} (\text{Box}_S) \times \text{Box}_S\) with \(n \geq 0\), define the map

\[
\text{WD}_* (X_{x, \ldots, x_n}) \rightarrow \text{UWD}(X_{x, \ldots, x_n})
\]

as follows. For \(\psi \in \text{WD}_* (X_{x, \ldots, x_n})\) (so \(\text{DN}_\psi = \emptyset\)), its image

\[
\chi_1 \psi = \overline{\psi} \in \text{UWD}(X_{x, \ldots, x_n})
\]

is the cospan

\[
\overline{Y} = Y^\text{in} \cup Y^\text{out}
\]

in \(\text{Fin}_S\). Here:

- \(X^\text{out} = \bigsqcup_{i=1}^n X_i^\text{out}\) and \(X^\text{in} = \bigsqcup_{i=1}^n X_i^\text{in}\).
- \(\text{Sp}_\psi\) is the set of supply wires of \(\psi\).
- The map

\[
\text{Dm}_\psi = Y^\text{out} \cup X^\text{in} \rightarrow Y^\text{in} \cup X^\text{out} = \text{Sp}_\psi
\]

is the supplier assignment for \(\psi\) (Def. 2.2.13).
Remark 12.2.3. Consider the output soldering function of $\overline{\psi}$ in (12.2.2.3). Due to the non-instantaneity requirement (2.2.13.2), the restriction of the supplier assignment $s_\psi$ to $Y^{\text{out}}$ is a map $Y^{\text{out}} \rightarrow X^{\text{out}}$.

Theorem 12.2.4. The maps $\chi_0$ (12.2.2.1) and $\chi_1$ (12.2.2.2) define a map of operads

\[ WD_* \xrightarrow{\chi} UWD. \tag{12.2.4.1} \]

Proof. As before we will write both $\chi_0$ and $\chi_1$ as $\chi$. We must check that $\chi$ preserves the operad structure in the sense of Def. 12.1.1. In both $WD_*$ (2.3.1.1) and $UWD$ (7.3.1.1), the equivariant structure is given by permuting the labels of the input boxes. So $\chi$ preserves equivariance in the sense of (12.1.1.1). Likewise, it follows immediately from the definitions of the colored units in $WD_*$ (2.3.2.1) and $UWD$ (7.3.2.1) that they are preserved by $\chi$ in the sense of (12.1.1.2).

To check that $\chi$ preserves operadic composition in the sense of (12.1.1.3), suppose $\varphi \in WD_*(x_{i_0} \ldots x_{i_n})$ with $n \geq 1$, $1 \leq i \leq n$, and $\psi \in WD_*(w_{i_1} \ldots w_{i_m})$ with $m \geq 0$. We must show that

\[ \chi(\varphi \circ_i \psi) = (\chi \varphi) \circ_i (\chi \psi) \in UWD(\overline{Z}) \tag{12.2.4.2} \]

in which

\[ \overline{Z} = (\chi \circ_0 W) = (X_{i_1}, \ldots, X_{i_{n-1}}, W_{i_1}, \ldots, W_{i_m}, X_{i_{n+1}}, \ldots, X_n) \in \text{Prof}(\text{Fin}_S) \]

as in (2.1.10.2), $X = (X_1, \ldots, X_n)$, and $W = (W_1, \ldots, W_m)$.

To prove (12.2.4.2), on the one hand, by Def. 2.3.4, $\varphi \circ_i \psi \in WD_*(x_{i_0}^\gamma \ldots x_{i_n}^\gamma)$ has supplier assignment

\[ Dm_{\varphi \circ_i \psi} = Y^{\text{out}} \sqcup \bigcup_{j \neq i} X^\text{in}_j \sqcup W^\text{in} \xrightarrow{s_{\varphi \circ_i \psi}} Y^\text{in} \sqcup \bigcup_{j \neq i} X^\text{out}_j \sqcup W^{\text{out}} = \text{Sp}_{\varphi \circ_i \psi} \]

that is given by $s_\varphi, s_\psi s_\varphi, s_\psi s_\psi$, or $s_\varphi s_\psi s_\psi$ according to (2.3.4.2) and (2.3.4.3). Here

\[ W^\text{in} = \prod_{k=1}^m W^\text{in}_k \quad \text{and} \quad W^{\text{out}} = \prod_{k=1}^m W^{\text{out}}_k \in \text{Fin}_S. \]

So by (12.2.2.3), $\chi(\varphi \circ_i \psi) \in UWD(\overline{Z})$ is the cospan

\[ \overline{Y} = \frac{Y^\text{in} \sqcup Y^{\text{out}}}{\text{Id} \sqcup s_{\varphi \circ_i \psi}} \tag{12.2.4.3} \]

\[ \bigcup_{j \neq i} X^\text{in}_j \sqcup \bigcup_{k} W^\text{in}_k \xrightarrow{(s_{\varphi \circ_i \psi}, \text{Id})} \text{Sp}_{\varphi \circ_i \psi} = \frac{Y^\text{in} \sqcup \bigcup_{j \neq i} X^\text{out}_j \sqcup W^{\text{out}}}{\text{Id} \sqcup s_{\varphi \circ_i \psi}} \]

in $\text{Fin}_S$. Here:

- The input soldering function is made up of
  - the identity map on $\bigcup_{j \neq i} X^\text{out}_j \sqcup W^{\text{out}}$,
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- the supplier assignment $s_{\varphi \circ i \psi} : \bigsqcup_{j \neq i} X^i_j \sqcup W^i_j \rightarrow S p_{\varphi \circ i \psi}$.

- The output soldering function is the coproduct of
  - the identity map on $Y^i_j$;
  - the supplier assignment $s_{\varphi \circ i \psi} : Y^\text{out} \rightarrow \bigsqcup_{j \neq i} X^\text{out}_j \sqcup W^\text{out}$.

On the other hand, by (12.2.2.3) and Def. 7.3.5 the $\circ_i$-composition

$$(\chi \varphi) \circ_i (\chi \psi) \in \text{UWD}(\Xi)$$

is the cospan

\[
\begin{array}{ccc}
\bigsqcup_{j \neq i} X^i_j \sqcup \bigsqcup_k W^i_k & \xrightarrow{(s_{\varphi} \mid_{\bigsqcup_k W^i_k}, \text{Id}_{\bigsqcup_k W^i_k})} & S p_{\varphi} = Y^\text{in} \sqcup Y^\text{out} \\
\text{pushout} & & \downarrow \\
\bigsqcup_{j \neq i} X^\text{out}_j \sqcup \bigsqcup_{k \neq i} W^\text{out}_k & \xrightarrow{(s_{\psi} \mid_{\bigsqcup_{k \neq i} W^\text{out}_k}, \text{Id}_{\bigsqcup_{k \neq i} W^\text{out}_k})} & S p_{\psi} \\
\end{array}
\]

in $\text{Fin}_S$, in which the square is defined as a pushout. In this diagram:

- In the middle vertical map, the restriction to
  - $X^\text{out}_i$ is the supplier assignment $s_{\varphi} : X^\text{out}_i \rightarrow W^\text{out}_i$;
  - all other coproduct summands is the identity map.

- In the bottom left horizontal map, the restriction to
  - $W^\text{in}$ is the supplier assignment $s_{\varphi} : W^\text{in} \rightarrow S p_{\varphi}$;
  - all other coproduct summands is the identity map.
Therefore, to check the condition (12.2.4.2), it suffices to show that the cospans (12.2.4.3) and (12.2.4.4) are the same. So it is enough to show that the square

\[
\begin{array}{ccc}
X_{\text{in}} \sqcup \bigcup_{j \neq i} X_{j} \sqcup X_{i}^{\text{out}} &=& X_{\text{in}} \sqcup X_{\text{out}} \\
\downarrow & & \downarrow \\
Y_{\text{in}} \sqcup \bigcup_{j \neq i} X_{j}^{\text{out}} \sqcup X_{i}^{\text{out}} &=& Y_{\text{in}} \sqcup X_{\text{out}}
\end{array}
\]

(12.2.4.5)

in \text{Fin}_{S} is a pushout (Def. 7.2.1). Here the restriction of the map \(h\) to

- \(\bigcup_{j \neq i} X_{j}^{\text{out}} \sqcup W_{\text{out}}\) is the identity map;
- \(X_{\text{in}}\) is the composition

\[
X_{\text{in}} \xrightarrow{s_{\psi}} Y_{\text{in}} \sqcup \bigcup_{j \neq i} X_{j}^{\text{out}} \sqcup X_{i}^{\text{out}} \xrightarrow{\operatorname{Id} \cup s_{\psi}^{\text{out}} \cup X_{i}^{\text{out}}} Y_{\text{in}} \sqcup \bigcup_{j \neq i} X_{j}^{\text{out}} \sqcup W_{\text{out}}.
\]

To see that the square (12.2.4.5) is commutative, observe that both compositions when restricted to

- \(X_{\text{in}}\) is \((\operatorname{Id} \cup s_{\psi}^{\text{out}}) \circ s_{\psi};\)
- \(\bigcup_{j \neq i} X_{j}^{\text{out}}\) is the identity map;
- \(X_{i}^{\text{out}}\) is \(s_{\psi}\).

It remains to check the condition (7.2.1.2) of a pushout. So suppose given a solid-arrow commutative diagram

\[
\begin{array}{ccc}
X_{\text{in}} \sqcup \bigcup_{j \neq i} X_{j} \sqcup X_{i}^{\text{out}} &=& Y_{\text{in}} \sqcup X_{\text{out}} \\
\downarrow & & \downarrow \\
Y_{\text{in}} \sqcup \bigcup_{j \neq i} X_{j}^{\text{out}} \sqcup W_{\text{out}} &=& Y_{\text{in}} \sqcup \bigcup_{j \neq i} X_{j}^{\text{out}} \sqcup W_{\text{out}}
\end{array}
\]

(12.2.4.5)
in \( \text{Fin}_S \). We must show that there exists a unique dotted map \( \eta \) that makes the diagram commutative. By a direct inspection the only possible candidate for \( \eta \) is given by the restrictions

\[
\gamma^{\text{in}} \amalg \bigcup_{j \neq i} X^{\text{out}}_j \xrightarrow{\eta = \beta} V \quad \text{and} \quad W^{\text{out}} \xrightarrow{\eta = \alpha} V.
\]

With this definition of \( \eta \), it remains to check the equalities

\[
\eta \left( \text{Id} \uplus \psi \big|_{X^{\text{out}}} \right) = \beta \quad \text{and} \quad \eta h = \alpha. \quad (12.2.4.6)
\]

Both of these equalities can be checked by a direct inspection. This finishes the proof that the square \((12.2.4.5)\) is a pushout and, therefore, that \( \chi \) preserves operadic composition \((12.2.4.2)\). \(\square\)

**Example 12.2.5.** By Example \(12.1.6\) and Theorem \(12.2.4\), every UWD-algebra (Def. \(11.1.1\)) induces a WD\(_*\)-algebra (Def. \(6.4.1\)) along the operad map \( \chi : \text{WD}\(_*\) \longrightarrow \text{UWD} \).

For example:

- The relational algebra of a set \( A \) (Def. \(11.2.4\) with \( S = * \)) induces a WD\(_*\)-algebra along the operad map \( \chi \).
- The typed relational algebra (Def. \(11.4.5\) with \( S = \text{Set} \)) also induces a WD\(_*\)-algebra along the operad map \( \chi \).

### 12.3. Examples of the Operad Map

The purpose of this section is to provide concrete examples of the map of operads \( \chi : \text{WD}\(_*\) \longrightarrow \text{UWD} \) in Theorem \(12.2.4\). Recall that the map \( \chi \) was defined in Def. \(12.2.2\). Similar to Section \(8.2\) all the assertions in this section are checked by a direct inspection of the normal and undirected wiring diagrams involved. So we will omit the proofs.

First we consider the normal generating wiring diagrams (Def. \(5.3.6\)) that are sent by \( \chi \) to generators in \( \text{UWD} \) (Def. \(8.1.7\)).

**Example 12.3.1.** For the empty wiring diagram \( \varepsilon \in \text{WD}\(_*\)(\(^{\text{in}}\)) \) (Def. \(3.1.1\)), the image

\[
\chi \varepsilon \in \text{UWD}(\^{\text{in}})
\]

is the empty cell (Def. \(8.1.1\)).

**Example 12.3.2.** For a name change \( \tau_f \in \text{WD}\(_*\)(\(^{\text{in}}\)) \) (Def. \(3.1.3\)), the image

\[
\chi \tau_f \in \text{UWD}(\^{\text{in}})
\]

is the name change \( \tau_f \) (Def. \(8.1.3\)) corresponding to the bijection

\[
\begin{align*}
\chi X &= X^{\text{in}} \amalg X^{\text{out}} \xrightarrow{f^{\text{in}} \amalg (f^{\text{out}})^{-1}} Y^{\text{in}} \amalg Y^{\text{out}} = \chi Y \in \text{Fin}_S
\end{align*}
\]

induced by \( f \).
Example 12.3.3. For a 2-cell $\theta_{X,Y} \in \text{WD}_{\bullet}(\frac{X}{Y})$ (Def. 3.1.4), the image
\[ \chi\theta_{X,Y} \in \text{UWD}(\frac{X}{Y}) \]
is the 2-cell $\theta(\frac{X}{Y})$ (Def. 8.1.4).

Example 12.3.4. For a 1-loop $\lambda_{X,x} \in \text{WD}_{\bullet}(\frac{X}{x})$ (Def. 3.1.5), the image
\[ \chi\lambda_{X,x} \in \text{UWD}(\frac{X}{x}) \]
is the loop $\lambda(\frac{X}{x})$ (Def. 8.1.5).

Example 12.3.5. For an out-split $\sigma_{Y,y_1,y_2} \in \text{WD}_{\bullet}(\frac{Y}{X})$ (Def. 3.1.7), the image
\[ \chi\sigma_{Y,y_1,y_2} \in \text{UWD}(\frac{Y}{X}) \]
is the split $\sigma(\frac{Y}{X})$ (Def. 8.1.6).

Next we consider an in-split and a 1-wasted wire. They are not sent by the map of operads $\chi$ to generators in $\text{UWD}$. So we will express their $\chi$-images as operadic compositions of the generators in $\text{UWD}$. By Theorem 10.1.12 this is always possible.

Example 12.3.6. For an in-split $\sigma_{X,x_1,x_2} \in \text{WD}_{\bullet}(\frac{X}{Y})$ (Def. 3.1.6) with $Y = \frac{X}{(x_1 = x_2)}$, suppose
\[ Z = \emptyset \cup \{x_1^+, x_1^-, x_2^+, x_2^-, x_1, x_2\} \in \text{Fin}_S \]
in which $v(x_1^+) = v(x_1^-) = v(x_1) \in S$. Identify
\[ \frac{Z}{(x_1^+ = x_1^-)} = \frac{\emptyset \cup \{x_1^+, x_2^+, x_2^-, x_1, x_2\}}{(x_1 = x_2 = x_1^+)} = \frac{X}{(x_1 = x_2)} \]
via $x_1^+ \mapsto x_1$ and $x_1^- \mapsto x_2$. Then we have
\[ \chi\sigma_{X,x_1,x_2} = \lambda(\frac{Z}{x_1}) \circ \sigma(\frac{Z}{x_1^+}) \in \text{UWD}(\frac{X}{Y}) \]  
(12.3.6.1)
in which:
- $\lambda(\frac{Z}{x_1}) \in \text{UWD}(\frac{Z}{X})$ is a loop (Def. 8.1.5);
- $\sigma(\frac{Z}{x_1^+}) \in \text{UWD}(\frac{Z}{X})$ is a split (Def. 8.1.6).

Observe that the right side of (12.3.6.1) also appeared in the elementary relation (8.2.16.1) in $\text{UWD}$. The equality (12.3.6.1) may be visualized as the following picture.
On the right side, the intermediate gray box is \( X \). In \( \chi_{\sigma_{X,x_1,x_2}} \) we drew all of \( X \setminus \{x_1, x_2\} \) on the right side of the box to make the picture easier to read. It has a \((2,1)\)-cable, and all other cables are \((1,1)\)-cables.

Next we consider the \( \chi \)-image of a 1-wasted wire.

**Example 12.3.7.** For a 1-wasted wire \( \omega_{Y,y} \in \text{WD}_\bullet(Y) \) (Def. 3.1.8) with \( X = Y \setminus y \), we have

\[
\chi \omega_{Y,y} = \theta_{(X,y)} \circ_2 \omega_y \in \text{UWD}(X)
\]  

(12.3.7.1)

in which:

- \( \theta_{(X,y)} \in \text{UWD}(X) \) is a 2-cell (Def. 8.1.4);
- \( \omega_y \in \text{UWD}(\emptyset) \) is a 1-output wire (Def. 8.1.2).

Observe that the right side of (12.3.7.1) also appeared in the elementary relations (8.2.6.1) and (8.2.7.1) and the example (8.3.3.1). The equality (12.3.7.1) may be visualized as the following picture.

\[
\begin{array}{c}
\omega_{Y,y} \\
\downarrow \quad X \quad \downarrow \chi \\
Y \quad X \quad y \\
\end{array}
\]  

(12.3.7.2)

In \( \chi \omega_{Y,y} \) we drew all of \( X \) on the right side to make the picture easier to read. It has a \((0,1)\)-cable, and all other cables are \((1,1)\)-cables.

**Example 12.3.8.** Each 1-output wire is in the image of \( \chi \). Indeed, for a 1-output wire \( \omega_y \in \text{UWD}(\emptyset) \) (Def. 8.1.2), we have

\[
\omega_y = \left[ \theta_{(\emptyset,y)} \circ_2 \omega_y \right] \circ \epsilon \\
= (\chi \omega_{y,y}) \circ (\chi \epsilon) \quad \text{by Examples (12.3.7) and (12.3.1)} \\
= \chi(\omega_{y,y} \circ \epsilon).
\]

(12.3.8.1)

Here:

- \( \theta_{(\emptyset,y)} \in \text{UWD}(\emptyset) \) is a 2-cell (Def. 8.1.4).
- \( \epsilon \in \text{UWD}(\emptyset) \) is the empty cell (Def. 8.1.1).
- \( \omega_{y,y} \in \text{WD}_\bullet(\emptyset) \) is the 1-wasted wire \( \omega_{Y,y} \) (Def. 3.1.8) with \( Y^{\text{out}} = \emptyset \) and \( Y^{\text{in}} = y \).
- \( \epsilon \in \text{WD}_\bullet(\emptyset) \) is the empty wiring diagram (Def. 3.1.1).

Note that in the first two lines of (12.3.8.1), the operadic compositions are in the operad UWD. On the other hand, in the last line of (12.3.8.1) the operadic composition is in the operad WD._
Example 12.3.9. By Examples 12.3.1–12.3.5 and 12.3.8, all 6 types of generators in $UWD$ (Def. 8.1.7) are in the image of the operad map $\chi : WD \to UWD$. However, one must be careful that this does not imply that every undirected wiring diagram is in the image of $\chi$. We will make precise the image of the operad map $\chi$ in Theorem 12.4.1 below.

Next we consider a 1-internal wasted wire, which by Prop. 3.2.3 can be generated by a 1-loop and a 1-wasted wire.

Example 12.3.10. For a 1-internal wasted wire $\omega^{X,x} \in WD_*$ (Def. 3.2.1) with $Y = X \setminus x$, we have
\[
\chi \omega^{X,x} = \lambda_{(Z,x_s)} \circ \sigma_{(Z,x_s)} \in UWD(\overline{X})
\] (12.3.10.1)
in which:
- $Z = \overline{Y} \cup x_s \in \text{Fin}_S$ with $v(x_+) = v(x-) = v(x) \in S$;
- $\lambda_{(Z,x_s)} \in UWD(\overline{Y})$ is a loop (Def. 8.1.5);
- $\sigma_{(Z,x_s)} \in UWD(\overline{Z})$ is a split (Def. 8.1.6).

Observe that the right side of (12.3.10.1) also appeared in the elementary relation (8.2.6.1). The equality (12.3.10.1) may be visualized as the following picture.

On the right side, the gray box is $Z$. In $\chi \omega^{X,x}$, all of $\overline{X} \setminus x = \overline{Y}$ is drawn on the left side. It has a $(1,0)$-cable, and all other cables are $(1,1)$-cables.

Example 12.3.11. Consider the wiring diagram $\pi \in WD_*$ in Example 4.2.3. Then $\chi \pi \in UWD(\overline{Y})$ is the right side of the following picture.

So $\chi \pi$ has a $(0,1)$-cable, a $(2,1)$-cable, a $(3,1)$-cable, a $(1,1)$-cable, and a $(1,0)$-cable.
Example 12.3.12. Consider the wiring diagram \( \pi_2 \in WD_\bullet(\mathcal{X}) \) in Example 4.3.2. Then \( \chi \pi_2 \in UWD(\mathcal{X}) \) is the right side of the following picture.

![Diagram](Image)

So \( \chi \pi_2 \) has two \((2,1)\)-cables, two \((0,1)\)-cables, a \((1,2)\)-cable, and two \((1,1)\)-cables.

12.4. Image of the Operad Map

The purpose of this section is to give an explicit description of the image of the map of operads \( \chi : WD_\bullet \longrightarrow UWD \) in Theorem 12.2.4. Recall that the map \( \chi \) was defined in Def. 12.2.2. Also recall the notations and terminology in Notation 9.1.1 regarding subsets of cables.

Theorem 12.4.1. Consider the operad map \( \chi : WD_\bullet \longrightarrow UWD \) in Theorem 12.2.4. Then:

1. The color map \( \chi_0 : Box_S \longrightarrow Fin_S \) \((12.2.2.1)\) is surjective.

2. The image of the entry map \( \chi_1 : WD_\bullet \longrightarrow UWD \) \((12.2.2.2)\) consists of precisely the undirected wiring diagrams with no wasted cables and no \((0, \geq 2)\)-cables.

Proof. The color map \( \chi_0 \) is surjective because, for each \( X \in Fin_S \), we have \((\emptyset, X) \in Box_S \) and \( \chi(\emptyset, X) = X \).

For the second assertion, we will prove the required inclusions in both directions. First suppose \( \psi \in WD_\bullet(\mathcal{X}_{i_1, \ldots, i_n}) \) for some \( n \geq 0 \). Recall that \( \chi \psi = \overrightarrow{\psi} \in UWD(\mathcal{X}_{i_1, \ldots, i_n}) \) is the cospan \((12.2.2.3)\)

\[
\overrightarrow{Y} = Y^{in} \uplus Y^{out}
\]

\[
\biguplus_{i=1}^n \overrightarrow{X_i} = X^{in} \uplus X^{out} \quad \xrightarrow{(s_{\psi}|_{X^{in}}, \text{Id}_{X^{out}})} \quad Sp_{\psi} = Y^{in} \uplus Y^{out}
\]

in \( Fin_S \). To see that \( \overrightarrow{\psi} \) has no wasted cables (i.e., \((0,0)\)-cables) and no \((0, \geq 2)\)-cables, suppose \( c \in Sp_{\psi} \) is not in the image of the input soldering function \( (s_{\psi}|_{X^{in}}, \text{Id}_{X^{out}}) \).

We must show that \( c \) is a \((0,1)\)-cable in \( \overrightarrow{\psi} \). Since \( c \) is not in the image of \( \text{Id}_{X^{out}} \), we have \( c \in Y^{in} \). By the non-instantaneity requirement \((2.2.13.2)\), we also have \( c \not\in s_{\psi}(Y^{out}) \). Therefore, \( c \) is in the image of the output soldering function \( \text{Id}_{Y^{in}} \uplus s_{\psi}|_{Y^{out}} \) exactly once, so \( c \) is a \((0,1)\)-cable in \( \overrightarrow{\psi} \).
To improve readability, the other half of the second assertion—i.e., that every undirected wiring diagram with no wasted cables and no \((0, \geq 2)\)-cables is in the image of the operad map \(\chi\)—will be proved in Proposition 12.4.10 below.

First we consider the special case when there are no \((0, \geq 0)\)-cables.

**Definition 12.4.2.** Suppose

\[
\varphi = \left( \prod_{j=1}^{N} U_j \xrightarrow{f_\varphi} C_\varphi \xleftarrow{g_\varphi} V \right) \in \text{UWD}(U_{i_1}, \ldots, U_{i_n})
\]  

(12.4.2.1)

with \(N \geq 0\) and \(C_\varphi^{(0, \geq 0)} = \emptyset\).

(1) For each cable \(c \in C_\varphi\), pick a wire

\[
u_c \in f_\varphi^{-1}(c) \subseteq \prod_{j=1}^{N} U_j
\]  

(12.4.2.2)

in the \(f_\varphi\)-preimage of \(c\). This is possible because the assumption \(C_\varphi^{(0, \geq 0)} = \emptyset\) means exactly that \(f_\varphi\) is surjective. We will use the canonical bijection

\[
\left\{ u_c : c \in C_\varphi \right\} \xrightarrow{f_\varphi} C_\varphi \cong \text{Fin}_S
\]  

(12.4.2.3)

below.

(2) For each \(1 \leq j \leq N\) define a box \(X_j \in \text{Box}_S\) as

\[
X^\text{out}_j = \left\{ u_c \in U_j : c \in C_\varphi \right\} \subseteq U_j \quad \text{and} \quad X^\text{in}_j = U_j \setminus X^\text{out}_j.
\]

Note that we have \(\overline{X}_j = U_j\),

\[
X^\text{out} = \prod_{j=1}^{N} X^\text{out}_j = \left\{ u_c : c \in C_\varphi \right\} \subseteq C_\varphi, \quad \text{and} \quad X^\text{in} = \prod_{j=1}^{N} U_j \setminus \left\{ u_c : c \in C_\varphi \right\}.
\]

(3) Define \(Y = (\emptyset, V) \in \text{Box}_S\), so \(\overline{Y} = V\).

(4) Using the bijection (12.4.2.3), define \(\psi \in \text{WD}_\bullet(X^\text{out}_1, \ldots, X^\text{out}_N)\) whose supplier assignment

\[
\text{Dm}_\psi = Y^\text{out} \sqcup X^\text{in} = V \sqcup \left[ \prod_{j=1}^{N} U_j \setminus \left\{ u_c : c \in C_\varphi \right\} \right]
\]

(12.4.2.4)

\[
\text{Sp}_\psi = Y^\text{in} \sqcup X^\text{out} \cong C_\varphi
\]

is

- \(g_\varphi\) when restricted to \(V\);
• $f_{\varphi}$ when restricted to $\bigsqcup_j U_j \setminus \{u_c\}$.

**Lemma 12.4.3.** In the context of Def. 12.4.2 we have

$$\chi \psi = \varphi \in \UWD(\biguplus_{n=1}^{V} \bigvee_{m=1}^{X_n}) = \UWD(U_{u_1, \ldots, u_n})$$

**Proof.** By definition $\chi \psi$ is the cospan (12.2.2.3)

$$V = Y_{\text{in}} \sqcup Y_{\text{out}}$$

$$\begin{array}{c}
\text{Id}_{\varnothing} \sqcup s_{\psi} \\
\downarrow \\
\downarrow \\
\biguplus_{j=1}^{N} U_j = X_{\text{in}} \sqcup X_{\text{out}} \\
\psi_{(s_{\psi}, \text{Id})} \\
\to \\
S_{\psi} = Y_{\text{in}} \sqcup X_{\text{out}} \cong C_{\varphi}
\end{array}$$

in $\text{Fin}_S$. Using the bijection (12.4.2.3) and the definition of $s_{\psi}$ (12.4.2.4), it follows that this cospan is equivalent to the given cospan (12.4.2.1) in the sense of Def. 7.1.4. So they define the same undirected wiring diagram, i.e., $\chi \psi = \varphi$. □

**Example 12.4.4.** Consider $\varphi$ in (12.4.2.1) with $N = 0$. Then $\bigsqcup U_j = \varnothing$. Since $f_{\varphi}$ is surjective, it follows that $C_{\varphi} = V = \varnothing$. So $\varphi$ is the empty cell $e \in \UWD(\varnothing)$ (Def. 8.1.1). The construction (12.4.2.4) above yields $\psi = e \in \WD_{\bullet}(\varnothing)$, the empty wiring diagram. So the conclusion $\chi e = e$ agrees with Example 12.3.1.

**Example 12.4.5.** Suppose $\varphi$ with $C_{\varphi}^{(0, \geq 0)} = \varnothing$ is the following undirected wiring diagram.

Then one choice of a $\chi$-preimage $\psi \in \WD_{\bullet}$, as constructed in (12.4.2.4), is the following normal wiring diagram.

Then $X_1$ has 2 inputs and 4 outputs, and $X_2$ has 2 inputs and no outputs. Note that according to Convention 2.2.10 we should draw inputs on the left and outputs on the right. However, we drew $\psi$ to resemble $\varphi$ to make the construction easier to understand.
Next we consider the general case where there may be \((0,1)\)-cables in \(\varphi\). The idea is to decompose \(\varphi\) as \(\varphi_1 \circ \varphi_0\) such that the following statements hold.

- \(\varphi_0\) satisfies the hypotheses of Lemma 12.4.3, so it has no \((0,\geq 0)\)-cables.
- \(\varphi_1\) contains all the \((0,1)\)-cables in \(\varphi\); its other cables are all \((1,1)\)-cables.
- Each of \(\varphi_0\) and \(\varphi_1\) can be lifted back to \(\text{WD}_\bullet\) in such a way that the lifted wiring diagrams are operadically composable in \(\text{WD}_\bullet\).

The fact that \(\chi : \text{WD}_\bullet \longrightarrow \text{UWD}\) is an operad map will then show that \(\varphi\) has a \(\chi\)-preimage.

**Definition 12.4.6.** Suppose

\[
\varphi = \left( \prod_{j=1}^{N} U_j \xrightarrow{f_\varphi} C_\varphi \xleftarrow{g_\varphi} V \right) \in \text{UWD}(U_{v_0}, U_{v_n}) \quad (12.4.6.1)
\]

with \(N \geq 0\) and \(C^{(0,0)}_\varphi = C^{(0,22)}_\varphi = \emptyset\). By assumption there is a decomposition

\[C_\varphi = \text{Im}(f_\varphi) \sqcup C^{(0,1)}_\varphi\]

in which \(\text{Im}(f_\varphi)\) is the image of \(f_\varphi\).

- Define

\[V_0 = g_\varphi^{-1}(\text{Im}(f_\varphi)) \quad \text{and} \quad V_1 = g_\varphi^{-1}(C^{(0,1)}_\varphi). \quad (12.4.6.2)\]

So \(V = V_0 \sqcup V_1\), and there is a bijection \(g_\varphi : V_1 \cong C^{(0,1)}_\varphi\).

- Define

\[
\varphi_0 = \left( \prod_{j=1}^{N} U_j \xrightarrow{f_\varphi} \text{Im}(f_\varphi) \xleftarrow{g_\varphi} V_0 \right) \in \text{UWD}(U_{v_0}, U_{v_n}), \quad (12.4.6.3)
\]

in which the input soldering function is surjective, i.e., \(C^{(0,20)}_{\varphi_0} = \emptyset\).

- Define

\[
\varphi_1 = \left( V_0 \xrightarrow{\text{inclusion}} V_0 \sqcup V_1 = V \xleftarrow{=} V \right) \in \text{UWD}(U_{v_0}), \quad (12.4.6.4)
\]

which has only 1 input box \(V_0\).

- Define \(Y_0 = (\emptyset, V_0) \in \text{Box}_S\), so \(Y_0 = V_0 \in \text{Fin}_S\).
- Define \(Y = (V_1, V_0) \in \text{Box}_S\), so \(Y = V \in \text{Fin}_S\).

First we observe that the two undirected wiring diagrams in the previous definition give a decomposition of \(\varphi\).

**Lemma 12.4.7.** In the context of Def. 12.4.6 there is a decomposition

\[\varphi = \varphi_1 \circ \varphi_0.\]
Proof. Since \( \varphi \) is the cospan

\[
\begin{array}{ccc}
N \bigcup_{j=1}^{N} U_j & \xrightarrow{f_\varphi} & \text{Im}(f_\varphi) \\
\downarrow s_\varphi & & \downarrow \text{incl} \\
V & \xrightarrow{C_\varphi = \text{Im}(f_\varphi) \cup C_\varphi^{(0,1)}} & V_0 \sqcup V_1
\end{array}
\]

in \( \text{Fin}_S \), by the definition of \( \circ = \circ_1 \) in UWD (Def. 7.3.5) it is enough to check that the square is a pushout. Since \( s_\varphi : V_1 \cong C_\varphi^{(0,1)} \) is a bijection, a direct inspection reveals that the square is a pushout.

\[\square\]

Lemma 12.4.8. For \( \varphi_1 \in \text{UWD}^{V_0}_{U_0, \ldots, U_N} \) in (12.4.6.4), there exists \( \psi_1 \in \text{WD}^{V_0}_{Y_0, \ldots, Y_N} \) such that \( \chi \psi_1 = \varphi_1 \).

Proof. Define \( \psi_1 \in \text{WD}^{V_0}_{Y_0, \ldots, Y_N} \) whose supplier assignment

\[
\begin{align*}
Dm_{\psi_1} & = Y^\text{out} \sqcup Y_0^\text{in} = V_0 \\
Sp_{\psi_1} & = Y^\text{in} \sqcup Y_0^\text{out} = V_1 \sqcup V_0 = V
\end{align*}
\]

is the inclusion map. Then it follows from the definition of \( \chi \) (12.2.2.3) that \( \chi \psi_1 = \varphi_1 \).

\[\square\]

Remark 12.4.9. By Lemma 12.4.6 \( \psi_1 \) in (12.4.8.1) is an iterated operadic composition of \( |V_1| \) 1-wasted wires (Def. 3.1.8). Since \( V_1 \cong s_\varphi^{-1} \left( C_\varphi^{(0,1)} \right) \) (12.4.6.2), this means that the \((0,1)\)-cables in \( \varphi \) are lifted to external wasted wires in \( \psi_1 \).

Proposition 12.4.10. Every undirected wiring diagram \( \varphi \) with \( C_\varphi^{(0,0)} = C_\varphi^{(0,\geq 2)} = \emptyset \) is in the image of the operad map \( \chi : \text{WD} \longrightarrow \text{UWD} \).

Proof. Suppose \( \varphi \in \text{UWD}^{V_0}_{U_0, \ldots, U_N} \) with \( C_\varphi^{(0,0)} = C_\varphi^{(0,\geq 2)} = \emptyset \). By Lemma 12.4.7 there is a decomposition

\[
\varphi = \varphi_1 \circ \varphi_0 \tag{12.4.10.1}
\]

with \( \varphi_0 \in \text{UWD}^{V_0}_{U_0, \ldots, U_N} \) and \( \varphi_1 \in \text{UWD}^{V_1}_{Y_0, \ldots, Y_N} \) as in Def. 12.4.6. Moreover, \( \varphi_0 \) satisfies the hypotheses of Lemma 12.4.3 (i.e., that its input soldering function is surjective). So there exists \( \psi_0 \in \text{WD}^{V_0}_{X_0, \ldots, X_N} \) such that

\[
\chi \psi_0 = \varphi_0 \tag{12.4.10.2}
\]
With $\psi_1 \in \text{WD}_\bullet(\chi)$ as in Lemma 12.4.8 we have
\[
\chi(\psi_1 \circ \psi_0) = (\chi \psi_1) \circ (\chi \psi_0) \quad \text{by Theorem 12.2.4}
\]
\[
= \varphi_1 \circ \varphi_0 \quad \text{by Lemma 12.4.8 and (12.4.10.2)}
\]
\[
= \varphi \quad \text{by (12.4.10.1)}.
\]
This proves that $\varphi$ is in the image of $\chi$. $\square$

Proposition 12.4.10 finishes the proof of Theorem 12.4.1.

**Example 12.4.11.** This is an extension of Example 12.4.5. Suppose $\varphi$ with $C_{\varphi}^{(0,0)} = C_{\varphi}^{(0,2)} = \emptyset$ is the following undirected wiring diagram.

![Undirected Wiring Diagram](attachment:image1.png)

Then one choice of a $\chi$-preimage $\psi \in \text{WD}_\bullet$, as constructed in Prop. 12.4.10, is the following normal wiring diagram.

![Normal Wiring Diagram](attachment:image2.png)

Note that the two $(0,1)$-cables in $\varphi$ are lifted to external wasted wires in $\psi$.

### 12.5. Map from Strict to Undirected Wiring Diagrams

For a fixed class $S$, recall the Box$_S$-colored operad of strict wiring diagrams $\text{WD}_0$ (Prop. 5.4.6). As pointed out in Example 12.1.4 we can compose the operad map $\chi : \text{WD}_\bullet \longrightarrow \text{UWD}$ in Theorem 12.2.4 with the operad inclusion $\text{WD}_0 \longrightarrow \text{WD}_\bullet$ in Prop. 12.1.7 to obtain an operad map

![Operad Map](attachment:image3.png)

The purpose of this section is to identify precisely the image of this operad map.
Theorem 12.5.1. The image of the operad map $\chi^0 : \text{WD}_0 \rightarrow \text{UWD}$ consists of precisely the undirected wiring diagrams whose cables are either $(1,1)$-cables or $(2,0)$-cables.

Proof. To make the argument easier to read, we will prove the two required inclusions in Lemmas 12.5.2 and 12.5.3 below. □

Lemma 12.5.2. The image of each strict wiring diagram under the operad map $\chi^0 : \text{WD}_0 \rightarrow \text{UWD}$ has only $(1,1)$-cables and $(2,0)$-cables.

Proof. Suppose $\psi \in \text{WD}_0(X_{1,\ldots,n})$, so it has no delay nodes and its supplier assignment $Dm_\psi = Y^\text{out} \sqcup X^\text{in} \xrightarrow{s_\psi / \sqsubseteq} Y^\text{in} \sqcup X^\text{out} = \text{Sp}_\psi$ is a bijection, where $X^\text{in} = \bigsqcup_{i=1}^n X^\text{in}_i$ and $X^\text{out} = \bigsqcup_{i=1}^n X^\text{out}_i$. Since $s_\psi (Y^\text{out}) \subseteq X^\text{out}$ by the non-instantaneity requirement (2.2.13.2), there is a decomposition $X^\text{out} = X^\text{out}_+ \sqcup X^\text{out}_-$ such that there are bijections

$$Y^\text{out} \xrightarrow{s_\psi / \sqsubseteq} X^\text{out}_- = \text{Im} (s_\psi | Y^\text{out})$$

and

$$X^\text{in} \xrightarrow{s_\psi / \sqsubseteq} Y^\text{in} \sqcup X^\text{out}_+$$

in $\text{Fin}_S$. By definition (12.2.2.3), $\chi^0 \psi \in \text{UWD}(Y_{1,\ldots,n})$ is the following cospan.

$$\begin{align*}
\top & = Y^\text{in} \sqcup Y^\text{out} \\
\bigsqcup_{i=1}^n X_i & = X^\text{in} \sqcup X^\text{out}_+ \sqcup X^\text{out}_- \\
\text{Sp}_\psi & = Y^\text{in} \sqcup X^\text{out}_+ \sqcup X^\text{out}_-
\end{align*}$$

Observe that:

- $X^\text{out}_- \subseteq \text{Sp}_\psi$ consists of only $(2,0)$-cables in $\chi^0 \psi$;
- $Y^\text{in} \sqcup X^\text{out}_+ \subseteq \text{Sp}_\psi$ consists of only $(1,1)$-cables in $\chi^0 \psi$.

Since there are no other cables, this finishes the proof. □

Lemma 12.5.3. If $\varphi \in \text{UWD}$ has only $(1,1)$-cables and $(2,0)$-cables, then it is in the image of the operad map $\chi^0 : \text{WD}_0 \rightarrow \text{UWD}$.

Proof. Suppose

$$\varphi = \left( U = \bigsqcup_{j=1}^N U_j \xrightarrow{f_\varphi} C_\varphi \xleftarrow{s_\varphi} V \right) \in \text{UWD}(U_{1,\ldots,n}^V)$$

has only $(1,1)$-cables and $(2,0)$-cables, i.e., $C_{\phi} = C_{\phi}^{(1,1)} \cup C_{\phi}^{(2,0)}$. To construct a $\chi^0$-preimage of $\phi$, first note that there is a decomposition

$$U = U^1 \sqcup U_+^2 \sqcup U_-^2$$

such that the following statements hold.

- $U^1 = \left\{ u \in U : f_{\phi} u \in C_{\phi}^{(1,1)} \right\}$, so there are bijections

  $$\xymatrix{ U^1 \ar[r]^{f_{\phi}} & C_{\phi}^{(1,1)} \ar[l]_{g_{\phi}} & V. \quad (12.5.3.1) }$$

- $U_+^2 = \left\{ u_c \in f_{\phi}^{-1}(c) : c \in C_{\phi}^{(2,0)} \right\}$ with $u_c$ as in $(12.4.2.2)$.

- For each $c \in C_{\phi}^{(2,0)}$, there exist unique $u_+ = u_c \in U_+^2$ and $u_- \in U_-^2$ such that $f_{\phi}(u_+) = c$. The correspondence $u_+ \leftrightarrow u_-$ defines a bijection $U_+^2 \cong U_-^2$.

In $(12.4.2.4)$ we already defined $\psi \in WD_{\gamma}(X_{1\ldots N})$ with supplier assignment

$$\xymatrix{ Dm_{\psi} = Y^{\text{out}} \sqcup X^{\text{in}} = V \sqcup U \setminus \left\{ u_c : c \in C_{\phi} \right\} \ar[d]_{s_{\psi} = (g_{\phi}, f_{\phi})} \ar[r] & C_{\phi} = C_{\phi}^{(1,1)} \sqcup C_{\phi}^{(2,0)} }$$

such that $\chi_{\psi} = \phi$ by Lemma $12.4.3$. So it is enough to show that $\psi$ is a strict wiring diagram. Since $\psi \in WD_{\gamma}$ has no delay nodes, it suffices to show that its supplier assignment $s_{\psi}$ is a bijection. First note that the map $g_{\phi} : V \rightarrow C_{\phi}^{(1,1)}$, $(12.5.3.1)$ is a bijection.

It remains to show that the map

$$U \setminus \left\{ u_c : c \in C_{\phi} \right\} \xrightarrow{f_{\phi}} C_{\phi}^{(2,0)}$$

is also a bijection. We have

$$U \setminus \left\{ u_c : c \in C_{\phi} \right\} = U^1 \sqcup U_+^2 \sqcup U_-^2 \setminus \left\{ u_c : c \in C_{\phi}^{(1,1)} \sqcup C_{\phi}^{(2,0)} \right\} = U_+^2 \sqcup U_-^2 \setminus \left\{ u_c : c \in C_{\phi}^{(2,0)} \right\} = U_-^2.$$

Since $f_{\phi} : U_-^2 \rightarrow C_{\phi}^{(2,0)}$ is a bijection, the proof is complete. \hfill \square

The proof of Theorem $12.5.1$ is complete.

**Example 12.5.4.** The following generators in $UWD$ (Def. $8.1.7$) are in the image of the operad map $\chi^0 : WD_0 \rightarrow UWD$.

- the empty cell $\epsilon \in UWD^{(0)}$ (Def. $8.1.3$);
12.6. Summary of Chapter 12

- a name change $\tau_f \in \text{UWD}(^3_0)$ (Def. 8.1.3);
- a 2-cell $\theta_{X,Y} \in \text{UWD}(^3_{X,Y})$ (Def. 8.1.4);
- a 1-loop $\lambda_{X,x} \in \text{UWD}(^3_X)$ (Def. 8.1.5).

In fact, by Examples 12.3.1–12.3.4, these generators are $\chi^0$-images of strict generating wiring diagrams (Def. 5.4.7). On the other hand,

- a 1-output wire $\omega_* \in \text{UWD}(^*)$ (Def. 8.1.2) and
- a split $\sigma^{(X,x_1,x_2)} \in \text{UWD}(^3_X)$ (Def. 8.1.6)

are not in the image of $\chi^0$.

**Example 12.5.5.** In the following picture, the strict wiring diagram on the left is sent by $\chi^0 : \text{WD}_0 \rightarrow \text{UWD}$ to the undirected wiring diagram on the right.

On the right, there are two $(2, 0)$-cables, and the other cables are $(1, 1)$-cables.

**Example 12.5.6.** In the following picture, the strict wiring diagram on the left is sent by $\chi^0 : \text{WD}_0 \rightarrow \text{UWD}$ to the undirected wiring diagram on the right.

On the right, there are two $(2, 0)$-cables and three $(1, 1)$-cables.

### 12.6. Summary of Chapter 12

1. There is an operad map $\chi : \text{WD} \longrightarrow \text{UWD}$ given by forgetting directions whose image consists of precisely the undirected wiring diagrams with no wasted cables and no $(0, \geq 2)$-cables.

2. The restriction of $\chi$ to $\text{WD}_0$ is an operad map $\chi^0 : \text{WD}_0 \longrightarrow \text{UWD}$. Its image consists of precisely the undirected wiring diagrams whose cables are either $(1, 1)$-cables or $(2, 0)$-cables.
Chapter 13

Map from Wiring Diagrams to Undirected Wiring Diagrams

This chapter has two main purposes.

1. We extend the operad map $\chi : \text{WD} \rightarrow \text{UWD}$ in Theorem 12.2.4, defined for normal wiring diagrams (i.e., those without delay nodes), to an operad map $\rho : \text{WD} \rightarrow \text{UWD}$ that is defined for all wiring diagrams. See Theorem 13.1.4.

2. Furthermore, we will show that the operad map $\rho : \text{WD} \rightarrow \text{UWD}$ is surjective; see Theorem 13.3.3. In other words, every undirected wiring diagram is the $\rho$-image of some wiring diagram.

We remind the reader that the image of the operad map $\chi : \text{WD} \rightarrow \text{UWD}$ was identified in Theorem 12.4.1. It consists of precisely those undirected wiring diagrams with no wasted cables and no $(0, \geq 2)$-cables.

At first glance, the existence of the operad map $\rho : \text{WD} \rightarrow \text{UWD}$ is not obvious because a general wiring diagram has delay nodes, but undirected wiring diagrams have no obvious analogues of delay nodes. In fact, for this reason Rupel and Spivak (RS13 4.1) expressed doubt that there exists an operad map from WD to UWD. Our main results in this chapter, Theorems 13.1.4 and 13.3.3 show that not only is there an operad map $\rho : \text{WD} \rightarrow \text{UWD}$, but also it is surjective. As we will see in (13.3.1.6), delay nodes play a critical role in realizing wasted cables and $(0, \geq 2)$-cables in undirected wiring diagrams.
In Section 13.1 we prove that an operad map $\rho : \text{WD} \rightarrow \text{UWD}$ exists and that it extends the existing operad map $\chi : \text{WD} \rightarrow \text{UWD}$. The construction of the operad map $\rho$ is motivated in Example 13.1.1, where we discuss how delay nodes should be sent to undirected wiring diagrams.

In Section 13.2 we provide a series of examples, all containing delay nodes, to further illustrate the operad map $\rho : \text{WD} \rightarrow \text{UWD}$.

In Section 13.3 we prove that the operad map $\rho : \text{WD} \rightarrow \text{UWD}$ is surjective. This section ends with Example 13.3.4, which provides a detailed illustration of how to lift an undirected wiring diagram back to a wiring diagram.

13.1. Wiring Diagrams to Undirected Wiring Diagrams

The purpose of this section is to construct an operad map $\rho : \text{WD} \rightarrow \text{UWD}$ that extends the operad map $\chi : \text{WD} \rightarrow \text{UWD}$ in Theorem 12.2.4. Since normal wiring diagrams are wiring diagrams with no delay nodes, to construct the operad map $\rho$, we need to decide how to map the delay nodes to undirected wiring diagrams.

Example 13.1.1. Before we define the desired operad map $\rho : \text{WD} \rightarrow \text{UWD}$, let us consider a motivating example that explains what happens to delay nodes. In the following picture, the wiring diagram $\varphi \in \text{WD}^{(\gamma)}$ on the left is sent to the undirected wiring diagram $\overline{\varphi} \in \text{UWD}^{(\gamma)}$ on the right.

In $\varphi$ there are 3 delay nodes and no input boxes. In $\overline{\varphi}$ there are 3 cables and no input boxes. As in the operad map $\chi : \text{WD} \rightarrow \text{UWD}$, every supply wire $\{y, d_1, d_2, d_3\}$ in $\varphi$ yields a cable in $\overline{\varphi}$. However, since a delay node is both a demand wire and a supply wire, we need to identify the cables corresponding to a delay node $d$ and its supply wire $s(d)$.

- In $\varphi$ the top delay node $d_1$ supplies only itself, so the identification is trivial. It yields a wasted cable in $\overline{\varphi}$.
- The middle delay node $d_2$ is supplied by the global input $y$, so their cables are identified, yielding a $(0, 2)$-cable in $\overline{\varphi}$.
The bottom delay node $d_3$ supplies itself and three global outputs, so the identification is trivial. Its cable is a (0,3)-cable in $\mathfrak{V}$.

For a general wiring diagram, this identification is defined in (13.1.2.2) below.

Observe that in $\mathfrak{V}$, there are a wasted cable, a (0,2)-cable, and a (0,3)-cable, none of which is possible in the image of $\chi : \text{WD} \to \text{UWD}$ by Theorem 12.4.1. In fact, this example suggests that the desired operad map $\rho : \text{WD} \to \text{UWD}$ is surjective because wasted cables and (0, $\geq 2$)-cables are now realizable by carefully chosen delay nodes. We will prove in Theorem 13.3.3 that this is indeed the case.

We now define the operad map $\rho : \text{WD} \to \text{UWD}$ that extends the operad map $\chi : \text{WD} \to \text{UWD}$ in Theorem 12.2.4. Recall the color map $\chi_0 : \text{Box}_S \to \text{Fin}_S$ in (12.2.2.1) with $\chi_0 Y = Y_\text{in} \sqcup Y_\text{out} \in \text{Fin}_S$ for each $Y = (Y_\text{in}, Y_\text{out}) \in \text{Box}_S$.

**Definition 13.1.2.** Fix a class $S$. For each $(X_{i_1}, \ldots, X_{i_n}) \in \text{Prof}(\text{Box}_S) \times \text{Box}_S$ with $n \geq 0$, define the map

$$\rho_1 : \text{WD}(X_{i_1}, \ldots, X_{i_n}) \to \text{UWD}(X_{i_1}, \ldots, X_{i_n})$$

as follows. For $\psi \in \text{WD}(X_{i_1}, \ldots, X_{i_n})$, its image

$$\rho_1 \psi = \mathfrak{V} \in \text{UWD}(X_{i_1}, \ldots, X_{i_n})$$

is the cospan

$$\begin{align*}
Y = Y_\text{in} \sqcup Y_\text{out} & \xrightarrow{\text{Id}_{Y_\text{in}} \cup \psi_\text{out}} Y_\text{in} \sqcup Y_\text{out} \\
\text{Sp}_\psi = Y_\text{in} \sqcup X_\text{out} \sqcup \text{DN}_\psi & \xrightarrow{\text{quotient}} \text{C}_\psi = \left( d = s_\psi d : d \in \text{DN}_\psi \right)
\end{align*}$$

in $\text{Fin}_S$. Here:

- $X_\text{out} = \bigsqcup_{i=1}^n X_{i_1}^\text{out}$ and $X_\text{in} = \bigsqcup_{i=1}^n X_{i_1}^\text{in}$.
- The map

$$\text{Dm}_\psi = Y_\text{out} \sqcup X_\text{in} \sqcup \text{DN}_\psi \xrightarrow{\psi} Y_\text{in} \sqcup X_\text{out} \sqcup \text{DN}_\psi = \text{Sp}_\psi$$

is the supplier assignment for $\psi$ (Def. 2.2.13).
- $s_\psi | Y_\text{out} : Y_\text{out} \to X_\text{out} \sqcup \text{DN}_\psi$ by the non-instantaneity requirement (2.2.13.2).
13. Map from Wiring Diagrams to Undirected Wiring Diagrams

- \( C_{\rho \psi} \) in the lower right corner is the quotient set obtained from \( Sp_{\psi} \) by identifying \( d \) and \( s_{\psi} d \) for each delay node \( d \in DN_{\psi} \).

**Remark 13.1.3.** In Def. (13.1.2) suppose \( \psi \in WD_\bullet(\chi_{1,\ldots,\chi_n}) \), i.e., \( DN_{\psi} = \emptyset \). Then

\[
C_{\rho \psi} = Sp_{\psi} = Y_{in} \cup X_{out},
\]

so \( \rho_1 \psi \) in (13.1.2) is equal to \( \chi_1 \psi \) in (12.2.2.3). In other words, when applied to normal wiring diagrams, the entry maps \( \rho_1 \) and \( \chi_1 \) are the same. So Def. (13.1.2) is indeed an extension of Def. (12.2.2) to all wiring diagrams.

**Theorem 13.1.4.** The maps \( \rho_0 = \chi_0 \) (12.2.2.1) and \( \rho_1 \) (13.1.2.1) define a map of operads

\[
WD \xrightarrow{\rho} UWD. \tag{13.1.4.1}
\]

**Proof.** This proof is similar to that of Theorem (12.2.4). The difference here is that we now need to take into account the delay nodes.

We will write both \( \rho_0 \) and \( \rho_1 \) as \( \rho \). We must check that \( \rho \) preserves the operad structure in the sense of Def. (12.1.1). In both WD (2.3.1.1) and UWD (7.3.1.1), the equivariant structure is given by permuting the labels of the input boxes. So \( \rho \) preserves equivariance in the sense of (12.1.1.1). Likewise, it follows immediately from the definitions of the colored units in WD (2.3.2.1) and UWD (7.3.2.1) that they are preserved by \( \rho \) in the sense of (12.1.1.2).

To check that \( \rho \) preserves operadic composition in the sense of (12.1.1.3), suppose \( \varphi \in WD(\chi_{1,\ldots,\chi_n}) \) with \( n \geq 1 \), \( 1 \leq i \leq n \), and \( \psi \in WD(\chi_{1,\ldots,\chi_n}) \) with \( m \geq 0 \). We must show that

\[
\rho(\varphi \circ_i \psi) = (\rho \varphi) \circ_i (\rho \psi) \in UWD(\overline{Z})
\]

in which

\[
\overline{Z} = (\overline{X}, \overline{W}) = (\overline{X_1}, \ldots, \overline{X_{i-1}}, \overline{W_1}, \ldots, \overline{W_m}, \overline{X_{i+1}}, \ldots, \overline{X_n}) \in \text{Prof}(\text{Fin}_S)
\]

as in (2.1.10.2), \( \overline{X} = (X_1, \ldots, X_n) \), and \( \overline{W} = (W_1, \ldots, W_m) \).

To prove (13.1.4.2), on the one hand, by Def. (2.3.4) \( \varphi \circ_i \psi \in WD(\chi_{1,\ldots,\chi_n}) \) has supplier assignment

\[
Dm_{\varphi_0, \psi} = \bigcup_{j \neq i} X_j^{in} \cup W_j^{in} \cup DN_{\psi} \cup DN_{\varphi},
\]

\[
Sp_{\varphi_0, \psi} = Y_{in} \cup \bigcup_{j \neq i} X_j^{out} \cup W_j^{out} \cup DN_{\psi} \cup DN_{\varphi},
\]

that is given by \( s_{\varphi}, s_{\psi} s_{\varphi}, s_{\varphi}, s_{\psi} s_{\psi}, \) or \( s_{\psi} s_{\varphi} s_{\psi} \) according to (2.3.4.2) and (2.3.4.3). Here

\[
W_{in} = \bigcup_{k=1}^m W_k^{in} \quad \text{and} \quad W_{out} = \bigcup_{k=1}^m W_k^{out} \in \text{Fin}_S.
\]
So by (13.1.2.2) \( \rho(\varphi \circ_i \psi) \in \text{UWD}(\Sigma) \) is the cospan

\[
\begin{align*}
\Xi &= \Xi^\text{in} \sqcup \Xi^\text{out} \\
\downarrow &
\end{align*}
\]

\[
\text{in } \text{Fin}_S. \text{ In (13.1.4.3):}
\]

- \( Z = Z^\text{in} \sqcup Z^\text{out} \in \text{Box}_S \), so
  \[
  Z^\text{in} = \bigsqcup_{j \neq i} X_j^\text{in} \sqcup W^\text{in} \quad \text{and} \quad Z^\text{out} = \bigsqcup_{j \neq i} X_j^\text{out} \sqcup W^\text{out} \in \text{Fin}_S. \tag{13.1.4.4}
  \]

- The input soldering function is induced by
  - the identity map on \( Z^\text{out} \),
  - the supplier assignment \( s_{\varphi_0 \circ_i \psi} : Z^\text{in} \to s_{\varphi_0 \circ_i \psi} \).

- The output soldering function is induced by
  - the identity map on \( Y^\text{in} \),
  - the supplier assignment \( s_{\varphi_0 \circ_i \psi} : Y^\text{out} \to Z^\text{out} \sqcup \text{DN}_\varphi \sqcup \text{DN}_\psi \).

In (13.1.4.3) and in what follows, to simplify the notation, we use the same symbol to denote a map and a map induced by it.

On the other hand, by (13.1.2.2) and Def. 7.3.5 the \( \circ_i \)-composition

\[
(\rho \varphi) \circ_i (\rho \psi) \in \text{UWD}(\Sigma)
\]

is the cospan

\[
\begin{align*}
\Xi &= \Xi^\text{in} \sqcup \Xi^\text{out} \\
\downarrow &
\end{align*}
\]

\[
\text{in } \text{Fin}_S, \text{ in which the square is defined as a pushout. In (13.1.4.5):}
\]
\[ C_{\rho\varphi} \text{ and } C_{\rho\psi} \text{ are the sets of cables in } \rho\varphi \text{ and } \rho\psi, \text{ i.e.,} \]
\[ C_{\rho\varphi} = \{ s_{\rho\varphi}d : d \in DN_{\rho} \} \quad \text{and} \quad C_{\rho\psi} = \{ s_{\rho\psi}d : d \in DN_{\psi} \}. \]

- In the middle vertical map, the restriction to \( X^\text{out}_i \) is the composition \( X^\text{out}_i \xrightarrow{s_{\rho\psi}} W^\text{out}_i \cup DN_{\psi} \in Sp_{\psi} \xrightarrow{C_{\rho\psi}} \)
  - all other coproduct summands is induced by the identity map.

- In the bottom left horizontal map, the restriction to \( W^\text{in}_i \) is the composition \( W^\text{in}_i \xrightarrow{s_{\rho\psi}} Sp_{\psi} \xrightarrow{C_{\rho\psi}} \)
  - all other coproduct summands is induced by the identity map.

- In the middle right horizontal map, the restriction to \( X^\text{in}_i \) is the composition \( X^\text{in}_i \xrightarrow{s_{\rho\psi}} Sp_{\psi} \xrightarrow{C_{\rho\psi}} \)
  - \( X^\text{out}_i \) is induced by the identity map.

Therefore, to check the condition (13.1.4.2), it suffices to show that the cospans (13.1.4.3) and (13.1.4.5) are the same. So it is enough to show that the square

\[
\begin{align*}
X^\text{in} \cup \bigsqcup_{j \neq i} X^\text{out}_j \cup X^\text{out}_i &= X^\text{in} \cup X^\text{out} \\
\downarrow (\text{Id}, s_{\rho\psi}|_{X^\text{out}}) \quad \text{and} \quad \downarrow (\text{Id}, s_{\rho\psi}|_{X^\text{out}}) \\
\bigsqcup_{j \neq i} X^\text{in}_j \cup \bigsqcup_{j \neq i} X^\text{out}_j \cup C_{\rho\varphi} &= \bigsqcup_{j \neq i} X^\text{in}_j \cup C_{\rho\varphi} \quad \xrightarrow{h} \quad C_{\rho_{\varphi\psi}}
\end{align*}
\]

in \( \text{Fin}_S \) is a pushout (Def. 7.2.1). In (13.1.4.6) the map \( h \) is induced by

- the composition \( X^\text{in} \xrightarrow{s_{\rho\psi}} Sp_{\psi} \xrightarrow{C_{\rho\psi}} \)
  - \( C_{\rho_{\varphi\psi}} \);

- the identity map of \( \bigsqcup_{j \neq i} X^\text{out}_j \cup W^\text{out}_i \cup DN_{\psi} \).

A direct inspection reveals that the right vertical map and the map \( h \) in (13.1.4.6) are both well-defined.

To see that the square (13.1.4.6) is commutative, observe that both compositions when restricted to

- \( X^\text{in} \) is induced by \( (\text{Id}, s_{\rho\psi}|_{X^\text{out}}) \circ (s_{\rho\psi}|_{X^\text{in}}) \);

- \( \bigsqcup_{j \neq i} X^\text{out}_j \) is induced by the identity map;
13.1. Wiring Diagrams to Undirected Wiring Diagrams

- \( X_i^\text{out} \) is induced by \( s_\varphi|_{X_i^\text{out}} \).

It remains to check the condition (7.2.1.2) of a pushout. So suppose given a solid-arrow commutative diagram

\[
\begin{array}{c}
X_\text{in} \sqcup \bigsqcup_{j \neq i} X_j^\text{out} \xrightarrow{(s_\varphi|_{X_\text{in}}, \text{Id})} C_{\rho \varphi} \\
\left( \text{Id}, s_\varphi|_{X_i^\text{out}} \right) \downarrow \quad \downarrow \beta \\
\bigsqcup_{j \neq i} X_j^\text{in} \sqcup \bigsqcup_{j \neq i} X_j^\text{out} \xrightarrow{\beta} C_{\rho \varphi} \\
\end{array}
\]

in \( \text{Fin}_S \). We must show that there exists a unique dotted map \( \eta \) that makes the diagram commutative. Recall that

\[
C_{\rho \varphi} = \frac{\text{Sp}_\varphi = Y^\text{in} \sqcup X^\text{out} \sqcup \text{DN}_\varphi}{\left( d = s_\varphi d : d \in \text{DN}_\varphi \right)}, \quad C_{\rho \psi} = \frac{\text{Sp}_\psi = X^\text{in} \sqcup W^\text{out} \sqcup \text{DN}_\psi}{\left( d = s_\psi d : d \in \text{DN}_\psi \right)},
\]

and

\[
C_{\rho (\varphi \circ \psi)} = \frac{\text{Sp}_{\varphi \circ \psi} = Y^\text{in} \sqcup \bigsqcup_{j \neq i} X_j^\text{out} \sqcup W^\text{out} \sqcup \text{DN}_\varphi \sqcup \text{DN}_\psi}{\left( d = s_{\varphi \circ \psi} d : d \in \text{DN}_\varphi \sqcup \text{DN}_\psi \right)}.
\]

A direct inspection reveals that the only possible candidate for \( \eta \) is the map induced by the compositions

\[
\begin{array}{c}
Y^\text{in} \sqcup \bigsqcup_{j \neq i} X_j^\text{out} \sqcup \text{DN}_\varphi \subseteq \text{Sp}_\varphi \xrightarrow{\beta} V; \\
W^\text{out} \sqcup \text{DN}_\psi \subseteq \text{Sp}_\psi \xrightarrow{\alpha} V.
\end{array}
\]

(13.1.4.7)

One can check that these definitions indeed yield a well-defined map \( \eta \). So with \( \eta \) defined as in (13.1.4.7), it remains to check the equalities

\[
\eta \left( \text{Id}, s_\varphi|_{X_i^\text{out}} \right) = \beta \quad \text{and} \quad \eta h = \alpha.
\]

(13.1.4.8)

Both of these equalities can be checked by a direct inspection. This finishes the proof that the square (13.1.4.6) is a pushout and, therefore, that \( \rho \) preserves operadic composition (12.2.4.2). \( \square \)

**Example 13.1.5.** By Example 12.1.6 and Theorem 13.1.4, every UWD-algebra (Def. 11.1.1) induces a WD-algebra (Def. 6.2.1) along the operad map \( \rho : \text{WD} \longrightarrow \text{UWD} \). For example:
13. Map from Wiring Diagrams to Undirected Wiring Diagrams

- The relational algebra of a set $A$ (Def. 11.2.4 with $S = \ast$) induces a WD-algebra along the operad map $\rho$.
- The typed relational algebra (Def. 11.4.5 with $S = \text{Set}$) also induces a WD-algebra along the operad map $\rho$.

13.2. Examples of the Operad Map

In this section we provide examples of the operad map $\rho : WD \rightarrow UWD$ in Theorem 13.1.4.

Recall from Remark 13.1.3 that the operad map $\rho : WD \rightarrow UWD$ extends the operad map $\chi : WD_{\ast} \rightarrow UWD$. Therefore, the next example and Examples 12.3.1–12.3.7 give a complete description of the $\rho$-images of all the generating wiring diagrams (Def. 3.1.9).

Example 13.2.1. For an element $d \in S$, the 1-delay node $\delta_d \in WD^{(d)}$ (Def. 3.1.2) is sent by $\rho$ to the undirected wiring diagram on the right.

Indeed, the set of supply wires in $\varphi$ is

$$
Sp_\varphi = Y_{\text{in}} \cup DN_\varphi \cup X_{\text{out}} = \{y_1, y_2, d\} \cup X_{\text{out}}.
$$
Since the delay node \(d\) is supplied by the global input \(y_1\), by definition (13.1.2.2) the set of cables of \(\rho \varphi\) is

\[
C_{\rho \varphi} = \{y_1, y_2, d\} \cup X^{\text{out}} = \{y_1, y_2\} \cup X^{\text{out}}.
\]

Therefore, in \(\rho \varphi\) the cable represented by \(y_1\) is a \((2, 3)\)-cable. It is soldered to: \(y_1\), the input of \(X\) supplied by \(y_1\) in \(\varphi\), and the two global output wires and the input wire of \(X\) supplied by \(d\) in \(\varphi\). The cable represented by \(y_2\) is a \((0, 1)\)-cable. The other two cables are a \((1, 0)\)-cable and a \((2, 1)\)-cable.

**Example 13.2.3.** In the following picture, the wiring diagram \(\varphi \in \text{WD}(\mathcal{Y})\) with one delay node \(d\) is sent by \(\rho\) to the undirected wiring diagram on the right.

In \(\varphi\) the delay node is supplied by itself, so the set of cables in \(\rho \varphi\) is

\[
C_{\rho \varphi} = \text{Sp}_\varphi = Y^{\text{in}} \cup X^{\text{out}} \cup \{d\}.
\]

In \(\rho \varphi\) the cable corresponding to \(d\) is a \((1, 2)\)-cable. The other two cables are both \((1, 1)\)-cables.

**Example 13.2.4.** In the following picture, the wiring diagram \(\varphi \in \text{WD}(\mathcal{Y})\) with one delay node \(d\) is sent by \(\rho\) to the undirected wiring diagram on the right.

In \(\varphi\) the delay node \(d\) is supplied by the unique output wire \(x\) of \(X\), so their corresponding cables are identified in \(\rho \varphi\). This cable is a \((2, 2)\)-cable. The other cable is a \((1, 1)\)-cable.
13.3. Surjectivity of the Operad Map

The reader is reminded of Notation 9.1.1 regarding subsets of cables. The purpose of this section is to show that the operad map \( \rho : \text{WD} \to \text{UWD} \) in Theorem 13.1.4 is surjective. Our strategy is similar to the proof of Lemma 12.4.3, except that here the input soldering function may not be surjective. Cables not in the image of the input soldering function are \((0, \geq 0)\)-cables. Wasted cables (i.e., \((0, 0)\)-cables) and \((0, \geq 2)\)-cables are realized using delay nodes, similar to the delay nodes \(d_1\) and \(d_3\) in Example 13.1.1. Moreover, \((0, 1)\)-cables are realized using external wasted wires, similar to \(y\) in the picture (12.3.7.2).

Given an undirected wiring diagram, we now define a wiring diagram that will be shown to be a \(\rho\)-preimage. Below we will use the map \(\chi_0 = \rho_0 : \text{Box}_S \to \text{Fin}_S\) (12.2.2.1), usually denoted by \(\chi_0 Y = \overline{Y} = \overline{Y^{\text{in}}} \cup \overline{Y^{\text{out}}}\). The following definition is the general version of Def. 12.4.2 in the sense that now we do not require the input soldering function to be surjective. A detailed example of the following definition will be given in Example 13.3.4.

**Definition 13.3.1.** Suppose

\[
\varphi = \left( U = \bigoplus_{j=1}^{N} U_i \xrightarrow{f_\varphi} C_\varphi \xleftarrow{g_\varphi} V \right) \in \text{UWD}(U_{i_1}, \ldots, U_{i_N})
\]  

(13.3.1.1)

for some \(N \geq 0\). We will use the equalities

\[
C_\varphi^{(\geq 1, \geq 0)} = \text{Im}(f_\varphi)
\]

\[
C_\varphi^{(\geq 1, \geq 0)} = C_\varphi^{(0,1)} \cup C_\varphi^{(\geq 1, \geq 0)} \cup C_\varphi^{(0,0)} \cup C_\varphi^{(0,\geq 2)}
\]

(13.3.1.2)

\[
V = g_\varphi^{-1} C_\varphi^{(0,1)} \cup g_\varphi^{-1} C_\varphi^{(\geq 1, \geq 0)} \cup g_\varphi^{-1} C_\varphi^{(0,\geq 2)}
\]

below.

1. For each \(c \in C_\varphi^{(\geq 1, \geq 0)}\), pick a preimage

\[
u_c \in \varphi^{-1}(c) \subseteq U.
\]

We will use the bijection

\[
\{u_c\} = \left\{u_c : c \in C_\varphi^{(\geq 1, \geq 0)}\right\} \xrightarrow{f_\varphi} C_\varphi^{(\geq 1, \geq 0)}
\]

(13.3.1.3)

and its inverse below.

2. For each \(1 \leq j \leq N\) define a box \(X_j = (X_j^{\text{in}}, X_j^{\text{out}}) \in \text{Box}_S\) as

\[
X_j^{\text{out}} = \left\{u_c \in U_j : c \in C_\varphi^{(\geq 1, \geq 0)}\right\} \subseteq U_j \quad \text{and} \quad X_j^{\text{in}} = U_j \setminus X_j^{\text{out}}.
\]

(13.3.1.4)
Note that we have $\overline{X_j} = X_j^{in} \cup X_j^{out} = U_j$;

$$X^{out} = \bigcup_{j=1}^{N} X_j^{out} = \{ u_c : c \in C_{\varphi}^{(\geq 1,\geq 0)} \} \cong C_{\varphi}^{(\geq 1,\geq 0)};$$

$$X^{in} = \bigcup_{j=1}^{N} X_j^{in} = U \setminus \{ u_c : c \in C_{\varphi}^{(\geq 1,\geq 0)} \}.$$

(3) Define a box $Y = (Y^{in}, Y^{out}) \in \text{Box}_S$ as

$$Y^{in} = g_{\varphi}^{-1} C_{\varphi}^{(0,1)};$$

$$Y^{out} = g_{\varphi}^{-1} C_{\varphi}^{(\geq 1,\geq 0)} \cup g_{\varphi}^{-1} C_{\varphi}^{(0,2)}.$$

(13.3.1.5)

Note that $\overline{Y} = Y^{in} \cup Y^{out} = V$.

(4) Define $\psi \in \text{WD}(\gamma, Y^{in})$ with delay nodes

$$DN_{\psi} = C_{\varphi}^{(0,0)} \cup C_{\varphi}^{(0,\geq 2)}.$$  

(13.3.1.6)

Recall the sets

$$Dm_{\psi} = Y^{out} \cup X^{in} \cup DN_{\psi} \quad \text{and} \quad Sp_{\psi} = Y^{in} \cup X^{out} \cup DN_{\psi}$$

of demand wires and of supply wires. The supplier assignment for $\psi$

$$Dm_{\psi} = g_{\varphi}^{-1} C_{\varphi}^{(\geq 1,\geq 0)} \cup g_{\varphi}^{-1} C_{\varphi}^{(0,\geq 2)} \cup [U \setminus \{ u_c \}] \cup C_{\varphi}^{(0,0)} \cup C_{\varphi}^{(0,\geq 2)}$$  

(13.3.1.7)

$$\xrightarrow{\delta_{\varphi}}$$

$$Sp_{\psi} = g_{\varphi}^{-1} C_{\varphi}^{(0,1)} \cup \{ u_c \} \cup C_{\varphi}^{(0,0)} \cup C_{\varphi}^{(0,\geq 2)}$$

is defined by the restrictions:

$$g_{\varphi}^{-1} C_{\varphi}^{(\geq 1,\geq 0)} \cup [U \setminus \{ u_c \}] \xrightarrow{(\delta_{\varphi}, f_{\varphi})} C_{\varphi}^{(\geq 1,\geq 0)} \xrightarrow{f_{\varphi}^{-1}} \{ u_c \};$$

$$g_{\varphi}^{-1} C_{\varphi}^{(0,\geq 2)} \xrightarrow{\delta_{\varphi}} C_{\varphi}^{(0,\geq 2)};$$

$$C_{\varphi}^{(0,0)} \cup C_{\varphi}^{(0,\geq 2)} \xrightarrow{\delta_{\varphi}} C_{\varphi}^{(0,0)} \cup C_{\varphi}^{(0,\geq 2)}.$$

Here $f_{\varphi}^{-1}$ is the inverse of the bijection (13.3.1.3).

**Remark 13.3.2.** Consider Def. [13.3.1]

(1) If $C_{\varphi}^{(0,\geq 0)} = \emptyset$ (i.e., $f_{\varphi}$ is surjective), then Def. [13.3.1] reduces to Def. [12.4.2]

(2) The definition (13.3.1.4) of each box $X_j$ means that:

- For each cable $c \in C_{\varphi}^{(\geq 1,\geq 0)} = \text{Im}(f_{\varphi})$, one wire in $U = \bigsqcup_{j=1}^{N} U_j$, namely $u_c$, soldered to $c$ is made into an output wire in $\psi$.
- All other wires in $U$ are made into input wires in $\psi$. 


(3) The definition \(13.3.1.5\) of the box \(Y\) means that:
- Elements in \(V\) that are soldered to \((0,1)\)-cables in \(\varphi\) are made into global input wires in \(\psi\).
- All other elements in \(V\) are made into global output wires in \(\psi\).

(4) The supplier assignment \(s_\psi\) in \(13.3.1.7\) satisfies the non-instantaneity requirement \(2.2.13.2\) because \(Y_{in} = g^{-1}_\varphi C^{(0,1)}_\varphi\) is disjoint from the image of \(s_\psi\), which is \(\{u_c\} \cup C^{(0,0)}_\varphi \cup C^{(0,\geq 2)}_\varphi\). In fact, \(Y_{in} = g^{-1}_\varphi C^{(0,1)}_\varphi\) is exactly the set of external wasted wires in \(\psi\).

(5) Each delay node \(13.3.1.6\) is supplied by itself, i.e., \(d = s_\psi d\) for each \(d \in DN_\psi\).

**Theorem 13.3.3.** Consider the operad map \(\rho : WD \rightarrow UWD\) in Theorem \(13.1.4\).

1. \(\rho\) is surjective on colors.
2. In the context of Def. \(13.3.1\), we have that \(\rho_\psi = \varphi\). In particular, the operad map \(\rho\) is surjective on entries as well.

**Proof.** The color map of \(\rho\) is \(\rho_0 = \chi_0 : Box_S \rightarrow Fin_S\) \((12.2.2.1)\), which is surjective by Theorem \(12.4.1(1)\).

For the second assertion, the undirected wiring diagram

\[
\rho_\psi \in UWD(\varphi, X_1, \ldots, X_n) = UWD(\psi, Y_1, \ldots, Y_n)
\]

is by definition the cospan in \(13.1.2.2\). Since every delay node in \(\psi\) \(13.3.1.6\) is supplied by itself, the set of cables in \(\rho_\psi\) is \(C_{\rho_\psi} = Sp_\psi\), the set of supply wires in \(\psi\). Furthermore, there is a bijection

\[
C_{\rho_\psi} = C^{(0,1)}_\varphi \cup \{u_c\} \cup C^{(0,0)}_\varphi \cup C^{(0,\geq 2)}_\varphi = g^\varphi (f^{\varphi} \cup \text{id})
\]

in which \(f^{\varphi}\) is the bijection \(13.3.1.3\).
13.3. Surjectivity of the Operad Map

By the definition of $s_\varphi$ (13.3.1.7), $\rho \psi \in \text{UWD}(U_{1,. . .,1})$ is the cospan (13.1.2.2)

$$V = \overline{Y} = g_\varphi^{-1} C_{\varphi}^{(0,1)} \cup g_\varphi^{-1} C_{\varphi}^{(\geq 1,\geq 0)} \cup g_\varphi^{-1} C_{\varphi}^{(0,\geq 2)}$$

$$\text{Id}_{\chi_{\varphi}} \sqcup \varphi = \text{Id} \sqcup f_\varphi^{-1} g_\varphi$$

$$U = \left[U \setminus \{u_c\} \cup \{u_c\} \right]_{\chi_{\varphi}} = (f_\varphi^{-1} f_\varphi \sqcup \text{Id}) \rightarrow C_{\rho \psi} = g_\varphi^{-1} C_{\varphi}^{(0,1)} \sqcup \{u_c\} \sqcup C_{\varphi}^{(0,0)} \sqcup C_{\varphi}^{(0,2)}$$

in which $f_\varphi^{-1}$ is the inverse of the bijection (13.3.1.3). Combining this cospan for $\rho \psi$ with the bijection (13.3.3.1), there is a commutative diagram

$$V = g_\varphi^{-1} C_{\varphi}^{(0,1)} \sqcup g_\varphi^{-1} C_{\varphi}^{(\geq 1,\geq 0)} \sqcup g_\varphi^{-1} C_{\varphi}^{(0,\geq 2)}$$

$$\text{Id} \sqcup f_\varphi^{-1} g_\varphi$$

$$C_{\rho \psi} = g_\varphi^{-1} C_{\varphi}^{(0,1)} \sqcup \{u_c\} \sqcup C_{\varphi}^{(0,0)} \sqcup C_{\varphi}^{(0,2)}$$

$$(f_\varphi^{-1} f_\varphi \sqcup \text{Id})$$

$$U = \left[U \setminus \{u_c\} \cup \{u_c\} \right] \rightarrow f_\varphi \rightarrow C_{\varphi} = C_{\varphi}^{(0,1)} \sqcup C_{\varphi}^{(\geq 1,\geq 0)} \sqcup C_{\varphi}^{(0,0)} \sqcup C_{\varphi}^{(0,2)}$$

in $	ext{Fin}_S$. In this diagram, the outer cospan is $\varphi$ (13.3.1.1). Therefore, by Def. 7.1.4 we have proved $\varphi = \rho \psi$. \qed

**Example 13.3.4.** This is an illustration of Def. [13.3.1] and Theorem 13.3.3. Consider the undirected wiring diagram $\varphi \in \text{UWD}(U_1,U_2)$ in (7.17.1), depicted as

![Diagram](image)

with $V = \{v_1, \ldots, v_6\}$, $U_1 = \{u_1, \ldots, u_6\}$, $U_2 = \{u^1, u^2\}$, and $C_{\varphi} = \{c_1, \ldots, c_7\}$. 

Following Def. 13.3.1 first note that we have the subsets
\[ C_\psi^{(0,0)} = \{c_4\}, \quad C_\psi^{(0,1)} = \{c_5\}, \quad C_\psi^{(0,2)} = \{c_1\}, \quad \text{and} \]
\[ C_\psi^{(2,2)} = \text{Im}(f_\psi) = \{c_2, c_3, c_6, c_7\}. \]

Next, for each cable \( c \in C_\psi^{(2,2)} \), we are supposed to choose an \( f_\psi \)-preimage \( u_c \in U = U_1 \sqcup U_2 \). We may choose, for example,
\[ u_{c_2} = u_1, \quad u_{c_3} = u_2, \quad u_{c_6} = u_5, \quad \text{and} \quad u_{c_7} = u_6, \]
all in \( U_1 \). With such choices, the boxes \( X_1 \) and \( X_2 \in \text{Box}_S \) (13.3.1.4) are
\[ X_1 = (X_1^{\text{in}}, X_1^{\text{out}}) = \left( \{u_3, u_4\}, \{u_1, u_2, u_5, u_6\} \right); \]
\[ X_2 = (X_2^{\text{in}}, X_2^{\text{out}}) = \left( \{u^1, u^2\}, \emptyset \right). \]

The box \( Y \in \text{Box}_S \) (13.3.1.5) is
\[ (Y^{\text{in}}, Y^{\text{out}}) = \left( g^{-1}C_\psi^{(0,1)}, g^{-1}C_\psi^{(1,2)} \sqcup g^{-1}C_\psi^{(2,2)} \right) = \left( \{v_6\}, \{v_1, v_2, v_3, v_4, v_5\} \right). \]

The set of delay nodes of \( \psi \in \text{WD}(x_i, x_o) \) (13.3.1.6) is
\[ \text{DN}_\psi = C_\psi^{(0,0)} \sqcup C_\psi^{(0,2)} = \{c_1, c_4\}. \]

The supplier assignment for \( \psi \) (13.3.1.7) is the function
\[ \text{Dm}_\psi = Y^{\text{out}} \sqcup X^{\text{in}} \sqcup \text{DN}_\psi = \{v_1, v_2, v_3, v_4, v_5\} \sqcup \{u_3, u_4, u^1, u^2\} \sqcup \{c_1, c_4\} \]
\[ \xrightarrow{s_\psi} \]
\[ \text{Sp}_\psi = Y^{\text{in}} \sqcup X^{\text{out}} \sqcup \text{DN}_\psi = \{v_6\} \sqcup \{u_1, u_2, u_5, u_6\} \sqcup \{c_1, c_4\} \]
given by
\[ s_\psi(v_1) = s_\psi(v_2) = c_1, \quad s_\psi(v_3) = u_1, \quad s_\psi(v_4) = s_\psi(v_5) = u_2, \]
\[ s_\psi(u_3) = s_\psi(u^1) = u_2, \quad s_\psi(u_4) = s_\psi(u^2) = u_5, \]
\[ s_\psi(c_1) = c_1, \quad \text{and} \quad s_\psi(c_4) = c_4. \]

The supply wire \( v_6 \) is an external wasted wire, and \( u_6 \) is an internal wasted wire in \( \psi \). We may draw \( \psi \in \text{WD}(x_i, x_o) \) as follows.
By Theorem 13.3.3(2) or a direct inspection, the map $\rho : \text{WD} \to \text{UWD}$ sends $\psi$ to $\varphi$.

Note that $\psi \in \text{WD}(\text{Y})$ is certainly not the only $\rho$-preimage of $\varphi \in \text{UWD}(\text{V})$. For example, the wiring diagram

also satisfies $\rho \psi' = \varphi$. Here the output box is

$$Z = (Z^\text{in}, Z^\text{out}) = \left(\{v_1, v_6\}, \{v_2, v_3, v_4, v_5\}\right) \in \text{Box}_S,$$

and $s_{\psi'}(c_1) = v_1$. Everything else is the same as in $\psi$. 
13.4. Summary of Chapter 13

(1) The operad map $\chi : WD \to UWD$ extends to an operad map $\rho : WD \to UWD$ that sends each delay node to a cable.

(2) The operad map $\rho$ is surjective.
This final chapter contains some problems from the earlier chapters about operads and (undirected) wiring diagrams.

**Problem 14.1.** Give a detailed proof of Prop. 2.1.12, which states that the two definitions of a colored operad—one in terms of May’s \( \gamma \) (Def. 2.1.3) and the other in terms of the \( \circ_i \)-compositions (Def. 2.1.10)—are equivalent. The equivalence of the unity axioms is rather easy to check. However, to prove the equivalence of the associativity axioms and the equivariance axioms in the two definitions, a fair amount of bookkeeping and notations are needed.

**Problem 14.2.** For the collection \( WD \) of \( S \)-wiring diagrams (Def. 2.2.15), write down its structure map \( \gamma \) (2.1.3.2) and prove that:

1. \( WD \) is a \( \Box S \)-colored operad in the sense of Def. 2.1.3.
2. This structure map \( \gamma \) corresponds to the \( \circ_i \)-compositions in Def. 2.3.4 in the sense of Prop. 2.1.12.

In [RS13] the operad \( WD \) was in fact defined in terms of the structure map \( \gamma \).

**Problem 14.3.** Consider the 28 elementary relations in Section 3.3.

1. Give a detailed proof for each elementary relation. These proofs are similar to those for Lemma 2.3.8, Lemma 2.3.10, and Prop. 3.2.3.
2. For each elementary relation, draw a picture that depicts the operadic compositions, similar to those just before Prop. 3.3.9 and Prop. 3.3.11 if one was not given.

**Problem 14.4.** Write down the proof for Lemma 4.2.2.

**Problem 14.5.** In Example 4.2.3
(1) Write down precisely the wiring diagrams \( \pi, \pi_1, \) and \( \pi_2, \) including their supplier assignments.

(2) Check carefully that there is indeed a decomposition \( \pi = \pi_1 \circ \pi_2. \)

**Problem 14.6.** In Example 4.3.2

(1) Write down precisely the wiring diagrams \( \beta_1, \beta_2, \) and \( \beta_3, \) including their supplier assignments.

(2) Check carefully that there is indeed a decomposition \( \pi_2 = \beta_1 \circ \beta_2 \circ \beta_3. \)

**Problem 14.7.** In Remark 5.1.10 it was stated that stratified simplices of type (1) and of type (2) are mutually exclusive. Write down a detailed proof for this claim.

**Problem 14.8.** For the wiring diagram in (2.2.18.1), without using Theorem 5.1.11, prove directly that it has a stratified presentation.

**Problem 14.9.** Check carefully the proof of Theorem 5.3.7, which is the finite presentation theorem for the operad \( WD_\bullet \) of normal wiring diagrams.

**Problem 14.10.** Give a direct proof of Theorem 5.4.8–the finite presentation theorem for the operad \( WD_0 \) of strict wiring diagrams–without referencing the proofs of Theorem 5.1.11, Lemma 5.2.8, Lemma 5.2.9, and Lemma 5.2.10.

**Problem 14.11.** Give a detailed proof that Def. 6.1.2 and Def. 6.1.3 of an operad algebra are indeed equivalent. The reader may consult [Yau16] (Chapter 16) for more information about operad algebras.

**Problem 14.12.** In Def. 6.2.1 check that the 28 generating axioms in fact correspond to the 28 elementary relations in the sense of the associativity diagram (6.1.3.1).

**Problem 14.13.** In the proof of Theorem 6.3.16–the finite presentation theorem for the propagator algebra–we checked the generating axioms (6.2.1.16) and (6.2.1.17) that are the least obvious. Give detailed proofs for the other 26 generating axioms for the propagator algebra.

**Problem 14.14.** In Remark 6.3.23 we pointed out that the structure map of the propagator algebra in [RS13] when applied to the generating wiring diagrams (section 3.1), reduces to our 8 generating structure maps in Def. 6.3.11 Check carefully that this is indeed the case.

**Problem 14.15.** Check carefully the proofs of Theorems 6.4.2 and 6.6.2 the finite presentation theorems for \( WD_\bullet \)-algebras and \( WD_0 \)-algebras.

**Problem 14.16.** In the proof of Theorem 6.5.12–the finite presentation theorem for the algebra of discrete systems–one generating axiom was written down in detail. Check the other 27 generating axioms carefully.
Problem 14.17. In the proof of Theorem 6.7.9—the finite presentation theorem for the algebra of open dynamical systems—we checked the generating axiom (6.2.1.16) corresponding to a double-loop. Give detailed proofs for the other 7 generating axioms for the algebra of open dynamical systems.

Problem 14.18. In Remark 6.7.10 we pointed out that the structure map of the algebra of open dynamical systems in [VSL13], when applied to the strict generating wiring diagrams—namely, \( e, \tau_{X,Y}, \theta_{X,Y}, \) and \( \lambda_{X,x} \)—reduces to our 4 generating structure maps in Def. 6.7.7. Check carefully that this is indeed the case.

Problem 14.19. Check carefully the proof of Propositions 7.3.6 and 7.3.16.

Problem 14.20. Check that each elementary relation in Section 8.2 is indeed an equality in UWD.

Problem 14.21. In Example 8.3.1 check that the iterated operadic composition (8.3.1.1) is the intended undirected wiring diagram \( \phi \circ \psi \).

Problem 14.22. In Example 8.3.2 check that the iterated operadic composition (8.3.2.1) is actually equal to \( \zeta_Y \).

Problem 14.23. In Example 8.3.3 check that the iterated operadic composition (8.3.3.1) is actually equal to \( \zeta_Y \).

Problem 14.24. Following the hint in Remark 11.1.3 formulate and prove a finite presentation theorem for a colored operad with given finite sets of generators and relations.

Problem 14.25. In the proofs of Theorems 11.2.5 and 11.4.7—the finite presentation theorems for the (typed) relational algebra—we checked one of the generating axioms. Give detailed proofs for the other 16 generating axioms.

Problem 14.26. Prove or disprove Spivak’s Conjecture 11.3.2 regarding the quotient freeness of the relational algebra. Then send me an email and tell me how you do it.

Problem 14.27. In Example 12.1.6 check that \( A^f \) is indeed an O-algebra.

Problem 14.28. In the proof of Theorem 12.2.4 check that it is actually sufficient to prove that the diagram (12.2.4.5) is a pushout in \( \text{Fin}_S \). Then check the equalities (12.2.4.6).

Problem 14.29. In the proof of Theorem 13.1.4

1. Check that it is actually sufficient to prove that the diagram (13.1.4.6) is a pushout in \( \text{Fin}_S \).

2. In the diagram (13.1.4.6), check that the right vertical map and the map \( h \) are indeed well-defined.

3. Check that the definitions (13.1.4.7) actually yield a well-defined map \( \eta \).

4. Check the equalities (13.1.4.8).
Chapter 15

Further Reading

Listed below are some references for categories, operads, props, and their applications. Each topic is a huge subject, so this list is not meant to be complete. It represents only a small sample of the existing literature. The reader is encouraged to consult these books and articles and the references therein.

15.1. Category Theory

These are references for basic category theory, of which [Mac98] is the most advanced and [Awo10, Lei14, Rie16] are more basic. The basic concepts of categories, functors, and natural transformations were all introduced in the founding article [EM45]. The paper [JSV96] introduced traced monoidal categories, which appear in many recent applications of category theory. The other books all have a view toward applications in the sciences.

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[Mac98] S. Mac Lane, Categories for the working mathematician, Grad. Texts in Math. 5, 2nd ed., Springer-Verlag, New York, 1998.

[Pie91] B.C. Pierce, Basic Category Theory for Computer Scientists, MIT Press, 1991.

[Rie16] E. Riehl, Category Theory in Context, Dover, New York, 2016.

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15.2. Operads

These are references for operads, originally defined by Lambek [Lam69] without symmetric group action and called multicycle. The name operad was coined by May in [May72]. Many applications of operads in mathematics and physics are discussed in [MSS02]. The book [LV12] is an in-depth study of algebraic operads, and [Yau16] is a basic introduction to operads in a symmetric monoidal category.

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15.3. Props

While an operad models operations with multiple inputs and one output, a prop—short for product and permutation—models operations with multiple inputs and multiple outputs. A typical example of a prop is the collection of functions \( \text{Map}(X^m, X^n) \) for a set \( X \) with \( m, n \geq 0 \). Using the kind of pictures in Motivation 2.1.2, a function \( f : X^m \to X^n \) may be depicted as follows.

![Diagram](https://www.example.com/diagram.png)

While an operad models operations with multiple inputs and one output, a prop—short for product and permutation—models operations with multiple inputs and multiple outputs. A typical example of a prop is the collection of functions \( \text{Map}(X^m, X^n) \) for a set \( X \) with \( m, n \geq 0 \). Using the kind of pictures in Motivation 2.1.2, a function \( f : X^m \to X^n \) may be depicted as follows.

![Diagram](https://www.example.com/diagram.png)

Props were originally defined by Adams and Mac Lane [Mac65]. Variations of props include wheeled props, in which there are contraction operations, modeling maps

\[
\xi_{ij} : \text{Map}(X^m, X^n) \to \text{Map}(X^{m-1}, X^{n-1})
\]

with \( 1 \leq i \leq n \) and \( 1 \leq j \leq m \). If \( f \) is represented as in the previous picture, then its contraction \( \xi_{ij} f \) may be represented as follows.

![Diagram](https://www.example.com/diagram.png)

The articles [Mar08, Val12] provide surveys of these compositional structures. The book [YJ15] is a comprehensive foundation of this subject.

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15.4. Applications of Compositional Structures

This is a short list of applications of categories, operads, and props in the sciences, including dynamical systems, computer science, engineering, network theory, linguistics, biology, neuroscience, and machine learning.

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[D.I. Spivak, P. Schultz, and D. Rupel, String diagrams for traced and compact categories are oriented 1-cobordisms, arXiv:1508.01069.]

[D. Wagner, D.I. Spivak, and E. Lerman, Algebras of open dynamical systems on the operad of wiring diagrams, Theory Appl. Categ. 30 (2015), 1793-1822.]
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