TIGER: Topology-aware Assignment using Ising machines
Application to Classical Algorithm Tasks and Quantum Circuit Gates

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Abstract
Optimally mapping a parallel application to compute and communication resources is increasingly important as both system size and heterogeneity increase. A similar mapping problem exists in gate-based quantum computing where the objective is to map tasks to gates in a topology-aware fashion. This is an NP-complete graph isomorphism problem, and existing task assignment approaches are either heuristic or based on physical optimization algorithms, providing different speed and solution quality trade-offs. Ising machines such as quantum and digital annealers have recently become available and offer an alternative hardware solution to solve this type of optimization problems. In this paper, we propose an algorithm that allows solving the topology-aware assignment problem using Ising machines. We demonstrate the algorithm on two use cases, i.e. classical task scheduling and quantum circuit gate scheduling. TIGER—topology-aware task/gate assignment mapper tool—implements our proposed algorithms and automatically integrates them into the quantum software environment. To address the limitations of physical solver, we propose and implement a domain-specific partition strategy that allows solving larger-scale problems and a weight optimization algorithm that allows tuning Ising model parameters to achieve better results. We use D-Wave’s quantum annealer to demonstrate our algorithm and evaluate the proposed tool flow in terms of performance, partition efficiency, and solution quality. Results show significant speed-up compared to classical solutions, better scalability, and higher solution quality when using TIGER together with the proposed partition method. It reduces the data movement cost by 68% in average for quantum circuit assignment compared to the IBM QX optimizer [15].

Keywords
Topology-aware task assignment · gate scheduling optimization · Ising machine · quantum annealing.

1 Introduction
The task assignment problem aims to maximize application performance by balancing computational load among multiple and often heterogeneous processing units while reducing compute overhead. The task assignment problem has been shown to be equivalent to a graph isomorphism problem by Bokhari [1], which is known to be NP-complete [20,13]. Therefore, many solvers for this problem are heuristic [31] that inevitably tradeoff solution quality for computation speed, or physical optimization algorithms, such as simulated annealing [34], genetic techniques [25], and others. In addition, solvers can have different optimization metrics that are often contradictory, such as computational load, communication cost, or a weighted combination [29,4].

Scheduling quantum gates onto physical qubits is similarly a challenging problem, given the complexity and variety of quantum operations and physical restrictions of each quantum chip. To keep operations efficient, quantum gates should be scheduled on quantum hardware such as to minimize the number of operations and maximize quantum circuit fidelity (how much quantum
information is preserved), while taking into account the connectivity between physical qubits [10]. Consequently, many mapping algorithms scale poorly due to runtime, memory usage, and the quality of their generated solutions [21]. In addition, the quality of their solutions compared to the theoretical optimal is unknown [35]. These challenges indicate that gate assignment may hinder high-quality solutions on future quantum accelerators with more physical qubits and complex connectivity.

While genetic algorithms and simulated annealing are often considered best practices, recent Ising machines offer an alternative hardware solution for a set of optimization problems, such as task scheduling. These Ising machines can be implemented using different technologies and exploit various physical effects. Such examples include coherent Ising machines [37], Fujitsu’s digital annealer [9], and quantum annealers designed by D-Wave Systems Inc. [10]. Several studies on quantum annealers [22] [19] explore its capabilities and limitations projecting the potential of these machines for future use.

Despite the potential benefits offered by quantum annealers combined with a growing interest in alternative solutions, practical applicability of annealing machines remains highly questionable. One of the reasons is physical limitations of current machines, namely the relatively small size of the chip and the poor connectivity between qubits [10]. Problem sizes demonstrated in comparison studies are usually not competitive with those handled by classical solvers. Therefore, effective problem partitioning and post-processing are required to continue exploiting quantum solver capabilities while the solution for physical limitations is sought [38]. That makes most of the near-term quantum annealing-based approaches classical-quantum hybrids.

Another obstacle towards wide-spread quantum annealer adoption is programming complexity. Its programming model is based on the Quadratic Unconstrained Binary Optimization (QUBO) [12] model that is different form the conventional programming and requires special approaches. The highest level that users are required to program D-Wave is “virtual” QUBO, where “virtual” means that the compiler takes care of mapping and routing the problem while taking into account device connectivity. Transforming a problem into QUBO format is not a trivial task. Higher-level tools as well as efficient algorithms are typically required [27].

In this work, we present the Topology-aware task assignment mappER (TIGER) to solve the assignment problem using Ising machines. Namely, our contributions are:

- We develop an algorithm to assign Task-Communication Graph (TCG) to the architecture units minimizing the required data-movement and maximizing the performance. The assignment problem is expressed in the QUBO format to be used by an Ising machine.
- We develop an algorithm to assign Quantum Circuit Graph (QCG) to the qubits minimizing data movement (number of SWAP operations) and maximizing the fidelity. The assignment problem is expressed in the QUBO format to be used by an Ising machine.
- We develop a domain-specific QUBO partitioning algorithm (sub-QUBO) based on the graph dependency levels to overcome current physical limitations of existing quantum annealers and accelerate the solution search.
- We develop a weight optimization algorithm (WOA) to tune Ising equation parameters in order to prioritize target metrics and adjust them to obtain better solutions.
- We implement these algorithms as a TIGER tool. TIGER is written in Python and uses the NetworkX package [7] to create and manipulate TCG/QCG and ARC structures.
- We integrate TIGER into the D-Wave tool-flow by supporting qbsolv qubo [2], qmasm [26] formats and creating a feedback loop from D-Wave to TIGER in order to evaluate the solution for further optimizations.
- We evaluate the proposed algorithms and its implementation using D-Wave quantum annealer. We compare the D-Wave solver performance and quality of the task assignment (solution) to the classical TABU-search algorithm. We evaluate the quality of the quantum circuits assignment in terms of the circuit fidelity using real IBM systems [15] and compare it against IBM QX gate optimizer. Our results show that TIGER with the D-Wave annealer provides up to 8% of computation cost improvement and up to 25% of communication cost improvement compared to the classical TABU-search solver when assigning a TCG. It reduces the data movement cost by 68% in average for quantum circuit assignment compared to the IBM QX optimizer [15].

Given the relatively small size of the evaluated quantum annealer, we leave the discussion on general competitiveness of quantum annealers against classical computing out of the scope of this paper. Our results aim to provide useful insights on the entire tool-flow including classical decomposition, domain-specific partition and QUBO solvers. Last but not least, we would like to extend an invitation to the community to use TIGER and then contribute back to aid tool growth.
is an arbitrary superposition of up to $2^n$ different states simultaneously. Another inherent quantum property of qubits is quantum entanglement where a group of qubits is coupled to each other in such a way that the state of each qubit cannot be perceived separately, but as a whole system state instead \cite{24}.

Quantum annealers provided by D-Wave Systems Inc. have been commercially available since 2011 \cite{16}. D-Wave quantum chips are implemented using superconducting technology and require an extreme isolated environment with a temperature close to absolute zero. A closed cycle dilution refrigerator cools the processor down to 15 mK. Therefore, while the actual quantum chip is the size of a stamp, the physical volume of the whole D-Wave system reaches 20 m$^3$. However, D-Wave machines consume less than 25 kW of power, mostly for cooling and front-end servers \cite{17}. In around 10 years, quantum annealing chips have reached $10^3$ number of qubits, promising significant performance improvement for certain computing problems in the near future. Physically, qubits are connected to each other using a so-called Chimera topology. The smallest Chimera unit contains a complete bipartite graph of eight vertices, each of which is connected to its four neighbours inside the unit and to its two neighbours outside the unit.

In \cite{6}, authors compare the performance of physical quantum annealer (D-Wave 2X quantum annealer) to simulated annealing and quantum Monte Carlo methods executed on a classical processor.

Furthermore, authors in \cite{22} extend Google Inc. studies by comparing quantum annealing to state-of-the-art optimization methods, introducing more sophisticated assessment metrics. Their work considers four categories of optimization methods: sequential methods that include quantum annealing, simulated annealing and quantum Monte Carlo, tailored methods that solve simplified optimization problems, and non-tailored methods that are generic and thus represent the state of the art. Authors conclude that physical quantum annealing has better scaling compared to other sequential optimization methods, but it concedes to tailored as well as non-tailored state-of-the-art methods. Also, authors emphasize the importance of determining the application domain where quantum annealing maximizes its benefits, but this has yet to be defined.

Finally, King et al. in \cite{19} introduce a problem class that can maximize usefulness of the quantum tunneling effect. Authors again compare quantum annealers to classical solvers and demonstrate three to four orders of magnitude performance speed-up in favor of quantum annealing.

Several studies demonstrate the use of quantum annealing for task scheduling. In \cite{32}, authors introduce a hybrid quantum-classical approach to solving scheduling problems. Their framework integrates quan-
Quantum annealing with classical computing into a guided tree search. Classical algorithms manage a global tree search and communicate the node search in QUBO format to the quantum annealer. Authors test the proposed framework on three scheduling problems, i.e. graph-coloring, mars lander task scheduling, and airport runway scheduling. Results show that the quantum annealer’s output can effectively prune and guide the search process. Authors motivate their work by necessity to expand on the capabilities of current quantum annealers and do not expect quantum annealers to be competitive in the near-term against classical computers.

In our work, we address a different scheduling problem, i.e. topology-aware assignment. The proposed TIGER framework extends existing software environments by automatically generating and dynamically adjusting QUBO files. We evaluate the tool flow in terms of quantum solver performance, the quality of task/gate assignment and discuss the potential scalability of near-term machines.

2.1 Problem formulation and programming

Quantum annealers minimize the QUBO problem described by Equation 1. The equation describes the evolution of the time-dependent Hamiltonian that aims to find low-energy states in a system of interacting spins, i.e. qubits. In Equation 1, q represents qubits that take value from the set \{0, 1\}, \( h_i \) is a weight coefficient associated with each qubit, \( J_{ij} \) denotes the strength of the couplings between two qubits \( q_i \) and \( q_j \) and \( N \) is the number of qubits.

\[
E(q_1,...,q_N) = \sum_{i=1}^{N} h_i \cdot q_i + \sum_{i<j}^{N} J_{ij} \cdot q_i \cdot q_j
\]

D-Wave annealer architectural designs impose a number of limitations on Equation 1. Notably, chips do not support all-to-all qubit connectivity. Thus, to couple two qubits located on different sides of the Chimera grid, excessive routing through other qubits is required. That dramatically cuts the number of available qubits to be purely used for problem solving. Another limitation concerns qubit weights and coupler strengths that lie in a specific range, i.e. \([-2;2]\) and \([-1;1]\) respectively, affecting the precision of the machine.

A low-level D-Wave program is expressed in the form of Equation 1 as a list of \( h_i \) and \( J_{ij} \) with the associated qubit numbers. The provided solution is a list of \( q_i \) values. This program is usually referred to as Quantum Machine Instruction (QMI). At this level, all previously listed constrains, such as qubit connectivity, variable range as well as the number of physically available qubits, have to be taken into account. That makes D-Wave programming a challenging task. However, there are several tools to provide a certain level of abstraction by taking as input a so-called “virtual” QUBO that abstracts away the size or connectivity topology of the D-Wave system and maps the problem onto the physical hardware using different optimization techniques.
3 Task Assignment Mapping Algorithm

3.1 Linear assignment problem

In the task allocation context, the Linear Assignment Problem (LAP) consists of placing a set of independent tasks onto a set of Processing Units (PUs), with each assignment incurring a certain cost. The objective is to assign each task to a PU such that the total cost is minimized. 

Figure 1(a) illustrates the transformation of the LAP to QUBO. The qubit matrix $Q$ represents the permutation matrix $X$, where each qubit defines the assignment of a task to a specific PU similar to $x_{ij}$ above. An $x_{ij}$ value of 1 represents that task $i$ was assigned to PU $j$. A weight coefficient $h_i$ (not shown) represents the computational cost of the assignment. Since solvers in current machines find local minima, we transform positive computation costs into negative numbers to prevent the solver from giving all-zero answers. To respect assignment constraints such as assigning one task to one qubit, we use qubit couplings and give them high penalty values such as $J_{ij} \gg |h_i|$. For example, to prevent task 0 from being placed on multiple PUs, we couple qubits $(q_0 \cdot q_1)$, $(q_0 \cdot q_2)$, $(q_0 \cdot q_3)$, $(q_1 \cdot q_2)$, $(q_1 \cdot q_3)$ and $(q_2 \cdot q_3)$ for four qubits. Therefore, if two of these qubits have the same task assigned to them, the large penalty value will make the overall solution ineligible.

3.2 Task-communication graph assignment

Applications can be represented as a weighted directed acyclic graph, usually referred to as a Task Communication Graph (TCG). A TCG is defined as a tuple $G = (V, E), where V = (v_i)$ is a set of weighted vertices with the weight representing task computational cost, and $E = (e_{i,j})$ is a set of weighted edges with the weight representing inter-task communication cost. An example of TCG is shown in the upper part of Figure 1(b).

Mapping of such as TCG into QUBO differs from previously shown LAP in three aspects. First, a TCG includes not only computation cost, but also inter-task communication cost expressed with graph edges. Second, not all tasks are assigned to PUs within the same time frame. A TCG is divided into multiple dependency levels each of which represents a LAP. Dependency levels (groups) are shown with red dashed lines. Third, within each dependency level, the number of independent tasks can be different compared to the number of available PUs. The QUBO mapping transformation respects each of the above three constraints.

Communication edges. Each communication edge is included into QUBO by qubit coupling. Communication cost is represented by coupling strength. Total end-to-end cost is calculated based on the weight of each edge in the communication path. If both source and destination tasks are assigned to the same PU, communication cost is equal to zero. This is the most favorable case if the objective is to minimize data movement. For the example in Figure 1(b), to define the edge between task0 and task1 we couple qubits $(q_0 \cdot q_3)$ and $(q_1 \cdot q_2)$ with the associated topology-aware communication cost and qubits $(q_0 \cdot q_2)$ and $(q_1 \cdot q_3)$ with zero communication cost. Here, cost values are converted to negative numbers similar to computation cost values. The relative priority of communication and computation costs can be formulated by adding a weight factor to bias the solver.

Dependency levels. Because of dependencies, only a certain number of tasks can be assigned to PUs in parallel. This relaxes the second assignment constraint that says that no more than one task can be placed at a PU. This constraint is valid only for tasks belonging to the same dependency group. For the example shown in Figure 1(b), task 0 is separated from task 1 and task 2 with a red dashed line. Thus, we couple only qubits $(q_2 \cdot q_4)$ and $(q_3 \cdot q_5)$ with a high penalty cost to prevent placing them on the same PU, which would otherwise be a valid solution for the solver. The first assignment constraint that says that a task can not be placed on multiple PUs at the same time remains unchanged.

Level adjustments. When the number of parallel tasks exceeds the number of available computing resources, an important decision has to be taken to priori-
tize a set of tasks in the most efficient way. This decision is reflected in the qubit matrix, i.e. the order of columns associated to specific tasks and corresponding assignment constrain couplings. Multiple approaches exist in the field, but this study is out of the scope of this paper. Here, we apply a simple cut based on the task ID increment. Figure 1(b) illustrates the case in which task \( 4 \) belongs to dependency level 1, but is moved to the next level. In case there are no available slots in the following group of tasks, an additional level is created.

3.3 Domain-specific TCG partition

Given the number of logical qubits together with the potential number of couplings and constrains per single problem, we quickly exhaust the physical capabilities of quantum machines. Therefore, an intelligent problem partition is required. There has been extensive research on graph partitioning [30]. In this context, we apply the method shown in Figure 1(c). This method divides a TCG into sub-graphs (SGs) based on dependency levels. The example shown in Figure 1(c) illustrates partitioning with two and three dependency levels per sub-QUBO1/2 and sub-QUBO3 respectively. The lowest degree of granularity corresponds to one dependency level per sub-QUBO. Further division of the problem will distort the concept of optimal parallel tasks assignment. The weakness of such a partitioning is that only communication edges inside a SG are regarded. Thus, multiple communication edges get excluded from the problem and are not represented in the qubit matrix. Excluded edges are labelled with red crosses in Figure 1(c). This may have a significant impact on the quality of the provided solution, especially for communication-intensive applications.

Part of the novelty of our work is improving the partition by applying an interactive previous-placement-dependent approach. This approach takes advantage of dependency level-based partitioning. Sub-QUBOs are solved one after another and each previous SG placement is used to enhance following sub-QUBOs. Our mapper extends the qubit matrix with additional virtual qubits—one per each unique source task of all excluded input edges (edges that are inputs to a SG). This qubit is associated with a specific PU because the previous task placement is already known at this point. In Figure 1(c), virtual qubits are shown as red crosses inside the sub-QUBO matrices and missed edges previously shown as crossed out are illustrated with red arrows.

Our approach guides the solver towards a better solution than is possible with heuristics alone, but does not guarantee an optimal solution because the output edges of the sub-graphs are still excluded from the problem and the future placement is not available at this point. It should also be emphasized that QUBO minimizes the sum of given costs, which are abstract positive numbers. Minimizing the sum does not guarantee that parallel execution time is also minimized, if that is determined by the slowest task.

3.4 Binary solution interpretation

Figure 2 illustrates the binary solution interpretation by mapping the example graph from Figure 1(c) on the four-unit mesh architecture. Each block corresponds to a dependency level of the task-communication graph. It contains three illustrative components, i.e. a qubit sub-matrix with solution values, computation task placement corresponding to the solution and communication traffic based on the prior task placements. In case both source and destination tasks are placed on the same unit, the communication edge is marked as local communication. Local communications do not contribute to the data movement component of the objective function and represent the most favourable assignment for communication cost minimization.

3.5 Computation and Communication costs

Computation and communication costs have been previously discussed as abstract positive numbers. However, the nature of the cost metric determines whether the proposed method provides an optimal solution. If the cost is based on delay and the goal of task assignment is to minimize time, QUBO minimization will not provide the optimal placement. This is because QUBO minimizes the sum of the placement costs in each SG and it does not guarantee that if placed in parallel task execution time is minimum. For other metrics, such as data movement, power consumption, energy, the proposed method provides an optimal solution.

4 Gate Assignment Mapping Algorithm

4.1 Quantum Circuits

In the context of gate-based quantum computing, quantum algorithms are usually represented in the form of so called quantum circuits. Figure 3(a) shows an example of the quantum circuit. To avoid confusion, the qubits represented on the circuit will be referred to as logical qubits and the real qubits inside a quantum computer as physical qubits. Four horizontal lines represent logical qubit state evolution over time (from left to right).
Single- and two-qubit gates are applied on specific qubits according to algorithm computations. Quantum circuits can be transformed into a task-communication graph similar to the classical algorithm transformation. In this case, quantum gates represent tasks that have dependencies (black arrows). Figure 3(b) shows the Quantum Circuit Graph (QCG) in the form of the TCG. A two-qubit gate becomes two connected tasks in the QCG. Moreover, two-qubit gates are directional, i.e. there are source and destination qubits in the pair.

Topology-aware quantum gate assignment is based on physical qubit connectivity inside the quantum chip. Figure 3(c) shows an example of the 5-qubit chip connectivity. Arrows show not only the connection between two physical qubits, but also the supported direction for the two-qubit gates. Because of the limited connectivity between qubits, not all two-qubit gates can be directly applied. For example, consider a circuit where a two-qubit gate is applied to logical qubits 0 and 3, and the circuit is matched to the architecture on Figure 3(c). There are two ways to map the qubits to circuit.

First is to map the logical qubits to physical in a different order such that logical 0 and 3 are mapped to physical 0 and 2. Another is to swap the underlying logical qubit states, in case if they are already mapped to the architecture in the same order. For instance, if the states of qubits 2 and 3 are swapped, the physical qubit 2 now would contain the state of the logical qubit 3, making it possible to apply the desired 2-qubit gate.

4.2 Fidelity and SWAP operation costs

Unlike a classical assignment optimization problem that minimizes computation and communication costs (described in Section 3.5), in quantum gate assignment optimization we target different metrics. One of the most important parameters for quantum computations in the NISQ era is fidelity. Circuit fidelity is a measure of how much quantum information is preserved. Due to the noise, the experimentally-obtained output qubit state is different from the desired output qubit state which would have been obtained in the ideal scenario. There is a direct correlation between the number of gates and circuit fidelity.

Typically, in case of superconducting technology, single-qubit gates have higher fidelity than two-qubit gates, which require significantly more effort to tune and improve. Each physical qubit is unique in its properties and has different fidelity per gate. The fidelity resulting from mapping logical qubits and their corresponding gates to the underlying architecture’s physical qubits will be referred to as fidelity_{mapping}.

There are several types of two-qubit gates. SWAP gate swap the states between two-qubits. A SWAP gate is usually decomposed into a sequence of three CNOT two-qubit gates. CNOT belongs to the so-called native set of gates that is supported by the control hardware and quantum chip technology. The need of this operation is dictated by the nature of quantum computation - it is not possible to make a copy of a qubit state (no-cloning theorem [28] [36]). A SWAP gate is used to move the qubit state to the right location. Thus, the number of SWAP operations N_{swaps} is similar to the data movement (communication) cost of the classical TCG. Consequently, the quantum state movement is required to satisfy chip connectivity. This movement comes at a cost, because two-qubit gates are the main source of infidelity in quantum circuits. The reduction in fidelity resulting from insertion of SWAP gates, each having fidelity_{swap}, will be referred to as fidelity_{movement},

$$fidelity_{movement} = (fidelity_{swap})^{N_{swaps}}$$

$$fidelity_{total} = fidelity_{mapping} * fidelity_{movement}$$ (2)

Since two-qubit gates have lower fidelity, quantum gate assignment optimization can be formulated as N_{swaps} minimization. However, in order to obtain the best total fidelity for the quantum circuit both of the optimization parameters need to be taken into account, i.e. gate mapping fidelity and minimum number of SWAPs. That makes the optimization problem almost
identical to the classical topology-aware task assignment on extremely heterogeneous architectures, where fidelity\textsubscript{mapping} represents computation performance to be maximized and where N\textsubscript{swaps} represents the communication cost to be minimized. Equation 2 shows how optimization of these two metrics can be reformulated as total fidelity fidelity\textsubscript{total} maximization. A large number of recent studies target the total circuit fidelity maximization [8]. However, they solve the optimization problem of the circuit gate decomposition and assignment to minimize the number of gates, especially SWAP gates, without consideration of fidelity\textsubscript{mapping}.

4.3 Weight Optimization Algorithm

Ising machine weights allow us to vary the priority of one or another optimization metric. By scaling the weights associated with SWAP minimization, either the qubit fidelity or SWAP reduction can be prioritized. To scale the weights, a priority coefficient pref is introduced. To arrive at the optimal solutions either in terms of the resulting number of SWAP gates inserted or gate fidelity, we propose an optimization algorithm. It searches for the coefficient value that maximizes fidelity\textsubscript{total}. Since fidelity\textsubscript{total} is obtained from fidelity\textsubscript{mapping} and fidelity\textsubscript{movement}, the algorithm can also find a solution with maximum fidelity\textsubscript{mapping} or minimum qubit movement. Due to infidelity of SWAP gates, a solution with minimum N\textsubscript{swaps} should correspond to maximum fidelity\textsubscript{total} solution. However, in a hypothetical fully-connected architecture where qubit movement constraint is eliminated, fidelity\textsubscript{mapping} would correspond to fidelity\textsubscript{total}. In such a scenario it would be practical to maximize only mapping fidelity. Optimizing only fidelity\textsubscript{mapping} or N\textsubscript{swaps} metric can also give an estimate of the bounds of these metrics in case if no optimal solution is known beforehand. Moreover, the proposed optimization algorithm can be suitable when it is needed to maintain a specific computation to communication ratio in task assignment, for example. The pseudocode is given in Algorithm 1 on the facing page. The search starts with an initial preference coefficient, gets the corresponding metric value, for example fidelity\textsubscript{total}, and compares it to other solutions with a larger and smaller coefficient. The search space range is defined by setting the parameter sSpr. How fast the algorithm converges is defined by the parameter sRed, which reduces the search space at every step. For better local search space exploitation lines 6-17 can be repeated with sSpr = √sSpr.

5 TIGER

5.1 D-Wave programming environment

Qbsolv [2] is an open source decomposing solver that focuses on large-scale problems that do not fit into physical hardware. In addition to the D-Wave annealer interface, qbsolv has an embedded classical solver that implements the tabu search algorithm 11 to minimize the QUBO problem. Qmasm [26] is a quantum macro assembler that provides extra flexibility for programming. A qmasm program can be run on both D-Wave annealers and qbsolv classical solvers.

5.2 TIGER tool flow

Figure 4 shows the tool flow for the task/gate assignment problem optimization. The key component of the flow is our proposed TIGER tool. TIGER is an
open-source QUBO mapper written in Python. It uses NetworkX python package \[7\] to create and manipulate TCG/QCG and ARC structures, i.e. computing the computation and communication costs for classical problems and fidelity and SWAP costs for quantum problems taking into account hardware (architecture) topology. We demonstrate TIGER on the D-Wave machine.

TIGER receives two files as inputs (marked as red ‘1’ to denote step 1), namely TCG or QCG and ARC (architecture). TCG describes the classical application’s TCG, QCG describes the quantum algorithm’s QCG, while ARC describes the architecture (hardware topology). The format of these files is presented in Figure \[5\](a) and (b). The TCG file consists of lines of two types associated to application tasks and edges. Task lines contain a task ID and multiple cost values each of types associated to application tasks and edges. Task lines contain an edge ID and generates the QMI interface file (step ‘2’). It supports both qasm and qubo formats and can generate a single file per problem or multiple files in case the QUBO partitioning option is chosen. If the size of the problem is less than the physical limit value, i.e. qubit sub-matrix size, QUBO or sub-QUBO can be directly solved (step ‘3’). Otherwise, it has to be further decomposed by qbsolv and then solved (step ‘4’). In both cases the problem is solved by two available solvers: the D-Wave annealer or a TABU search qbsolv implementation (step ‘5’).

Finally, the solver generates mapping solutions that are sent back to the TIGER tool. If the solution corresponds to sub-QUBO (step ‘7’), it is used by TIGER to generate the next sub-QUBO as described in Section \[5.2\]. If the solution is complete (step ‘6’) or the last sub-QUBO problem is solved, TIGER calculates the final cost of the assignment through its Mapping-to-Metric (MtoM) interface (step ‘8’). This cost can be used to estimate the quality of the solution.

6 Results

6.1 Experimental setup

Experiments are conducted on a hybrid classical-quantum system that consists of an Intel Core i7 running at 3.3 GHz with 16 GB 2133 MHz LPDDR3 and a D-Wave 2X (DW2X) quantum annealer \[10\] that has 1152 qubits and 2400 couplers.

For classical TCG assignment optimization, we use three workload TCGs from the COSMIC benchmark set \[53\]. The choice of these three workloads is dictated by the differences in its problem size, number of tasks, and number of edges. A detailed analysis and classification of the application graphs in the context of the Ising model evaluation can provide additional insights. Such as study is out of the scope of this paper. The TCG files are provided by external modelling tool, i.e.
the COSMIC benchmark suite [33]. Table I shows the set of chosen benchmarks and their characteristics.

For quantum QCG assignment optimization, we create the QCG files formatted for TIGER from the quantum benchmark suite [39]. We create ARC files based on two IBM quantum chips [15]: IBM Yorktown (QX2) with 5 qubits and IBM Vigo with 5 qubits. Figure 3 (c) illustrates these two topologies. The quantum benchmark suite [39] provides 48 circuits for 5-qubit chips. We reduce the circuit size down to 50 gate.

6.2 Tool flow evaluation

For each workload we evaluate three scenarios: (I) TIGER QUBO mapper - qbsolv decomposer/TABU-search qbsolv solver - TIGER MtoM interpretor, (II) TIGER QUBO mapper - qbsolv decomposer/DW solver - TIGER MtoM interpretor and (III) TIGER QUBO mapper/TIGER SG partitioner - qbsolv decomposer/ TABU-search qbsolv solver - TIGER MtoM interpretor. For each scenario, we vary the size of the architecture to a 2×2 PU mesh, 4×4 PU mesh, and an 8×8 PU mesh.

Figure 6 shows evaluation results. Here, we report the delay normalized to the total delay of the longest case. Each delay is also broken down to its four major components. In all cases, the longest scenario is the one fully executed on a classical computer, e.g. scenario I. In addition, we show the number of logical qubits and couplers generated by TIGER’s mapper (qubits # and couplers #), the number of partitions provided by qbsolv’s decomposer (partitions #), and the number of SGs generated by TIGER’s partitioner (tiger sQs #). The number of qubits in scenarios I and II is equal, but it is higher in scenario III because additional qubits are required to define previous sub-QUBO placements as shown in Figure 1. Similarly, the number of couplers as well as the number of partitions in scenarios I and II are equal. It is lower in scenario III due to the optimized QUBO mapping. The number of TIGER sub-QUBOs is reported only for scenario III. In scenarios I and II this TIGER option is not applied (na).

**Discussion:** Performance evaluation results prove that the physical quantum annealer, i.e. DW2X, can significantly reduce delay-to-solution compared to the classical qbsolv solver. For the given set of benchmarks and architecture configurations, the performance speedup of the DECOMPOSER-SOLVER phase varies between 1.2× and 10.2×. The major portion of this improvement is caused by the replacement of the classical solver with the quantum annealer. The average value of the DW2X access time is around 20ms. This time includes programming time, sampling time and post-processing time. The sampling phase consists of multiple sample batches, each of which includes annealing, readout, and additional delay that allows the quantum annealer to cool down to the initial state. The annealing time is 20µs. Although QUBO is solved by a physical quantum annealer, a significant amount of time associated to the problem decomposition is spent by qbsolv DECOMPOSER. The total D-Wave SOLVER phase is composed of multiple D-Wave accesses, where the number of accesses is determined by the number of partitioned calls provided by qbsolv DECOMPOSER. Therefore, while using the quantum annealing solver the delay-to-solution phase highly depends on the quality of the classical decomposition.

In scenario III, we evaluate the impact of the domain-specific partitioning integrated into the QUBO mapper, i.e. TIGER level partitioner. Here, reported values represent the sum of all sub-QUBO parameters concerning the total number of qubits and couplers as well as delays per phase. Results show that by applying two-level QUBO partitioning (i.e. domain-specific first and classical qbsolv second), a massive speedup in time-to-solution can be achieved. For the given set of TCGs and ARCs, the DECOMPOSER-SOLVER phase is reduced down to 6% compared to the baseline scenario.
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(a) Ultrasound-9x5x10

(b) Reed-Solomon Encoder-32x28x8

(c) Reed-Solomon Decoder-32x28x8

Fig. 7: Task assignment sensitivity and quality of the solution. (DW, single): DW w/o sQ vs. classical TABU-search w/o sQ, (qbsolv, sQ): classical TABU-search with sQ vs. classical TABU-search w/o sQ and (DW, sQ): DW with sQ vs. classical TABU-search w/o sQ.

Such an improvement has several sources. First, TIGER partition significantly simplifies the task for qbsolv DE-COMPOSER, which performs better on a smaller subset of qubits and coupler tasks than on a single large problem. Consequently, qbsolv generates fewer partition calls thereby reducing D-Wave SOLVER phase delay. This effect is particularly noticeable for larger TCGs where the number of partitions is reduced twice. The total number of qubits and couplers is also different compared to the baseline. By applying the minimum number of qubits possible and adjusting the level of granularity (i.e. one sub-level per sub-QUBO), we reduce the total number of couplers. These improvements are achieved at the expense of having a larger number of qubits. This increase is 12% by average compared to the baseline. On the other hand, additional partitioning can potentially impact the quality of the generated solution. This effect is evaluated in the following section.

6.3 Task assignment evaluation

We evaluate the assignment quality and multiple-run sensitivity in three comparison scenarios: (i) single QUBO on quantum annealer versus classical qbsolv solver (dw, single), (ii) partitioned sub-QUBOs versus single QUBO assignment on classical qbsolv (qbsolv, sQ), and (iii) partitioned sub-QUBOs on quantum annealer versus single QUBO assignment on classical qbsolv solver (DW, sQ). Architecture configuration files represent a $2 \times 2$, $4 \times 4$, or $8 \times 8$ heterogeneous PU MESH with an abstract PU acceleration factor varied from $1 \times$ to $4 \times$. Link cost is equal to 2. Figure 7 shows the difference in computation, communication and total costs for the three evaluation scenarios compared to the baseline.

Discussion: In some cases, we obtain the same solution over multiple runs. If different solutions are returned, usually the variation is within 5% from the mean value. For a given set of experiments, DW2X quantum solver provides solution improvements for a single QUBO compared to the classical TABU-search solver. Results show up to 8% of computation cost improvement, up to 25% of communication cost improvement, and up to 15% of total improvement. Both qbsolv sQ and DW sQ scenarios show similar behaviour in most experiments. However, again DW2X quantum solver provides better solutions, e.g. RS-Encoder...
mapped on 2×2 MESH and RS-Decoder mapped on 2×2 MESH.

Qbsolv sQ and DW sQ evaluations show that dependency-level partitioning indeed can significantly impact assignment quality, namely its communication constituent. This impact increases when architecture size scales. MtoM communication difference rises from 35% to 45% and then to almost 4× for US TCG mapped on 2×2, 4×4 and 8×8 architectures shown in Figure 7(a). Similarly, it changes from -2% to 6% and then to 60% for RS Encoder TCG as shown in Figure 7(b). However, the computation constituent does not deteriorate. In both TCGs, task computation costs far outweigh communication edge cost. For instance, US computation cost ranges between 4,510 and 3,461,112, while communication highest cost is 20, 60 and 140 for 2×2, 4×4, and 8×8 MESHes respectively. Thereby, calculated edge weights and associated qubits couplings have low impact on the total QUBO cost. Indeed, the total MtoM difference follows the computational cost behaviors, e.g. DW sQ in Figure 7(b.1) or qbsolv SQ in Figure 7(a.2). By prioritizing the edge cost versus task cost, the communication MtoM difference can be significantly reduced. In contrast, RS Decoder TCG is communication intensive. The computation cost varies to 1,880, while the communication cost reaches 14,280 for 8×8 MESH. In this case, DW sQ partition does not impact the solution quality, but it improves it by 15%.

6.4 Gate assignment evaluation

In order to make an estimation of how scaling the weights would correlate with \( N_{\text{swaps}} \) and fidelity\(_{\text{mapping}}\) a set of experiments was performed on the QCGs mentioned in Section 6.1.2. The preference coefficient varies from 0.01 to 30. Figure 8 shows the mapping fidelity (fidelity\(_{\text{mapping}}\)), number of swaps (\( N_{\text{swaps}} \)) and total fidelity for different coefficient values. Smaller coefficients minimize qubit state movement, while larger ones prioritize mapping fidelity instead. Black box shows a near-optimum region of the priority coefficient. Using the priority coefficient smaller than 0.05 results in invalid solutions being produced by the algorithm and can even lead to the opposite effect, increasing \( N_{\text{swaps}} \) instead. Setting the coefficient larger than 20 provides only small improvement of fidelity\(_{\text{mapping}}\), but it only happens in some architectures and incurs an inadequate number of additional SWAPs. Hence, applicable coefficient values that produce the minimum \( N_{\text{swaps}} \) and maximum fidelity\(_{\text{mapping}}\) are approximately 0.05 and 20, respectively. Total fidelity strongly correlates with the number of SWAPs and mapping fidelity plays a negligible role in this scenario.

**Discussion:** Since fidelity\(_{\text{movement}}\) coming from \( N_{\text{swaps}} \) has a larger impact on fidelity\(_{\text{total}}\), usually \( N_{\text{swaps}} \) is minimized and gate fidelity is not considered. It means that the priority coefficient that maximizes fidelity\(_{\text{total}}\) is the same that minimizes \( N_{\text{swaps}} \), i.e. 0.05. However, as connectivity in quantum computing architectures increases, qubit movement might become less significant. In such a context maximization of fidelity\(_{\text{total}}\) would be entirely dependent on fidelity\(_{\text{mapping}}\).

### 6.4.1 Weight optimization algorithm evaluation

To tackle any possible scenario, fidelity\(_{\text{total}}\) can be maximized regardless of connectivity and gate fidelity. The priority coefficient that allows such a maximization is unknown, and can vary for every different circuit and architecture. We study the proposed weight optimization algorithm to assess its efficiency in finding the optimal priority coefficient for a combination of quantum circuit and device topology.

Figure 9 shows total fidelity and number of SWAPs optimization using WOA algorithm for multiple circuits for IBM Vigo and IBM QX2 topologies. The results include initial value at the beginning of the algorithm execution and the final value. For IBM Vigo topology (results in Figure 9(a) and (b)), the WOA finds the priority coefficient that reduces the number of SWAPs from the initial step value in 62.5% of cases. In 37.5% of cases the number of SWAPs remains unchanged. The results with strong reduction are highlighted in green. In average, WOA improves total fidelity by 39% for IBM Vigo topology. For IBM QX2 topology (results in Figure 9(c) and (d)), the WOA finds the priority coefficient that reduces the number of SWAPs from the initial step value in 83.3% of cases. In one case the number of SWAPs remains unchanged, and in 14.6% of cases WOA provides weak increase of the SWAPs number. In average, WOA improves total fidelity by 107% for IBM QX2 topology.
Discussion: The results show significant difference in WOA performance when applied on different topologies. While in general WOA allowed us finding more suitable combination of QUBO weights (preference coefficient) for both topologies, IBM QX2 mapping is much more sensitive towards priority coefficient choice. Moreover, in few cases WOA missed optimal solution that resulted in a weak increase in SWAPS number compared to the initial state value. We believe, that the reason lies in the complexity of the topology graph that calls for the QUBO weights adjustments to find the most suitable combination in a near-optimum region.

6.4.2 Comparison

Finally, we compare the performance of TIGER topology-aware SWAP optimizer against the IBM QX optimizer. Figure 10 shows the comparison results across multiple circuits for two topologies, i.e. vigo and qx2. The numbers show the final number of SWAPS. The SWAP reduction color map highlights the cases when one of the optimizer provides a better result with the SWAP number differences as follow: (i) 1-2 SWAPS, (ii) 3-4 SWAPS, (iii) 5-7 SWAPS or (iv) more than 7. For the vigo topology, TIGER and IBM QX provides same SWAP number in 18.7% of cases; IBM QX outperforms TIGER in 41.7% of cases with the total reduction difference of 51 SWAPS; and TIGER outperforms IBM QX in 39.6% of cases with the total reduction difference of 59 SWAPS. For the qx2 topology, TIGER and IBM QX provides same SWAP number only in 4.2% of cases; IBM QX outperforms TIGER in 8.3% of cases with the total reduction difference of 12 SWAPS; and TIGER significantly outperforms IBM QX in 87.5% of cases with the total reduction difference of 260 SWAPS. Moreover, TIGER found the perfect mapping reducing the data movement to 0 SWAPS in 16.7% of cases, while IBM QX found the perfect matching only in 4.2% of cases.

Discussion: Similar to the WOA evaluation results (see section 6.4.1), the comparison results show significant difference when applied on different topologies. TIGER allowed us significantly improve the mapping for IBM QX2 topology compared to the IBM QX optimizer. We believe, that the reason also lies in the topology graph complexity. Classical IBM QX optimizer is not suitable for more complex topologies with a larger number of potential combinations, while TIGER optimizer allows us to find the ‘perfect’ mapping regardless.
7 Conclusions

In this paper, we propose an algorithm for solving the topology-aware task/gate assignment problem on physical Ising machines in order to accelerate and improve the quality of the solution to this challenging NP-complete problem. We implement our solution in our TIGER tool that transforms weighted task-communication, quantum circuit, and architecture graphs into an appropriate format of the Hamiltonian function. Our solution takes into account both computation and communication costs for the classical problem or fidelity and SWAP number for the quantum problem. We evaluate the proposed approach using D-Wave’s quantum annealer. In order to overcome existing physical limitations of current quantum annealers, we propose domain-specific partitioning based on the task-communication graph dependency levels. Also, we propose weight optimization algorithm that enables adjusting the model parameters and find better solutions. We integrate TIGER into the D-Wave software stack that enables us to apply both our proposed dependency-level partitioning as well as the partitioning provided by the qbsolv tool in a dynamic iterative way. We demonstrate that our method can reach 15% higher-quality solutions 9% faster compared to the classical qbsolv heuristic algorithm. Finally, TIGER reduces the data movement cost by 68% in average for quantum circuit assignment compared to the IBM QX optimizer [15].

Our work alleviates the concern that task mapping may hinder high-quality solutions on future quantum accelerators with more physical qubits and complex connectivity. The TIGER tool is publicly available online[2].

For future work, we consider three major directions:

- **Comparison to a wide range of classical scheduling tools**: we plan to design a methodology to compare the hardware optimizer, i.e. Ising machine, to existing heuristic software tools.

- **Use other Ising machines**: we plan to expand our study running the problem on other Ising machines, such as digital annealer [9] and coherent Ising machine [37].

- **Problem partitioning algorithms and additional constrains mapping**: we plan to evaluate additional graph partitioning algorithms and alternative problem mapping algorithms, e.g. assigning multiple tasks in one node based on the node capacity.

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[2] https://github.com/lbnlcomputerarch/tiger

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Fig. 10: Optimizer comparison: TIGER vs. IBM QX
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