Simulation-Based Analysis of Ultra Thin-Body Double Gate Ferroelectric TFET for an Enhanced Electric Performance

Girdhar Gopal1 · Tarun Varma1

Received: 28 July 2021 / Accepted: 25 September 2021 / Published online: 8 October 2021 © Springer Nature B.V. 2021

Abstract
The ultra thin body double gate FE layer TFET (UTB-DG-FE-TFET) is proposed and investigated in this work. Electrical performance parameters such as surface potential $\psi(x)$, electrical field, drain current, sub-threshold swing, threshold voltage, and $I_{on}/I_{off}$ ratio are further analyzed using simulation-based analysis. Integration of Si: $HFO_2$ ferroelectric layer on top and bottom surfaces make the structure that provides negative capacitance, higher on current, enormous surface potential, peak electric field, and improvement in SS with degradation in off Current. The suggested design is evaluated in comparison with FE-TFET and standard TFET structures. Finally, the impact of device geometry variants like ferroelectric layer thickness ($t_{fe}$), intrinsic channel thickness ($t_{si}$), interfacial layer types, interfacial layer thickness ($t_{ox}$) and channel length $L_c$ on transfer characteristics are investigated through 2D TCAD Sentaurus Simulator for a clear validation of its optimization. The recommended work demonstrates that it is a suitable device enabling superior performance and helpful in ultra-low-power applications.

Keywords BTBT · Memory window · Subthreshold swing · Threshold voltage · UTB-DG-FE-TFET

1 Introduction

Short channel effects (SCEs) and an increase in leakage current are the main issues with downscaling the CMOS technology node [1–4]. Moreover, at room temperature $T=300\text{K}$, the scalability of threshold voltage $V_T$ is also limited due to Boltzmann tyranny (SS $\equiv K_B T/\ln 10 \approx 60\text{ mV/decade}$) that decides the steepest nature of the transition between on and off state [5–9]. In short, there is a need for in-depth research on steep subthreshold swing devices ($<60\text{ mV/decade}$) like Tunnel field-effect transistors (TFETs) [10, 11], Impact ionization MOSFETs (I-MOS-FETs) [12], Nano-electro-mechanical FETs (NEMFETs) [13] and Negative capacitance FETs [14]. These Emerging devices have been seriously explored in recent years due to impending physical constraints of conventional CMOS devices. Thereby TFETs or commonly called the green transistors, are the most promising contenders that operate on the quantum mechanical band-to-band tunneling (B2BT) principle [15–17]. A most claiming obstacle for TFET being low on-drive-current ($I_{on}$) because of less transmission probability $T_{WKB}$ of the interband tunneling barrier [18]. $T_{WKB}$ is estimated using Wentzel-Kramer-Brillouin (WKB) approximation. WKB approximation defines it as exponential function of effective mass $m^*$, energy band gap $E_g$, tunneling length $\lambda$, and the difference in energy between both the source’s conduction band and the channel’s valence band $\delta\phi$. That is tunneling barrier approximation is estimated by $T_{WKB} \approx \exp\left[-4\lambda\sqrt{2m^*E_g/\hbar}\sqrt{\frac{E_g}{3q(1+E_g/\delta\phi)}}\right]$. $I_{on}$ is obtained by integration of $T_{WKB}$ over depth of source-channel junction. Moreover, at fixed drain voltage, a rise in gate voltage $V_g$ changes the surface potential, minimizing $\lambda$ and raising $\delta\phi$. Thereby, maximum transmission probability $T_{WKB}$ of tunneling barrier implies a greater on-current $I_{on}$. Accordingly, there are many possible causes to increase $I_{on}$: (i) The usage of high-K gate material, for example, is a type of gate dielectric engineering technology, service of multi-gate structures for controlling channel potential perfectly, selection of the optimum value of spacer to enhance on-current $I_{on}$, asymmetric gate design by the use of different work functions and different gate dielectric materials, and ferroelectric gate oxide [19] (ii) Tunneling

---

1 Electronics and Communication Engineering Department, Malaviya National Institute of Technology Jaipur, Jaipur, Rajasthan 302017, India
junction engineering such as by use of the optimum value of source doping, by increasing effective tunneling area and heterojunction structure by use of low-bandgap materials [11] (iii) Material engineering techniques by use of unique materials like Ge and III-V semiconductors [20] (iv) by use of strained-silicon [21]. However, the ferroelectric gate oxidation technique is the best example of negative capacitance that can provide high \( I_{on} \) and sub-60 mV/decade at a modest voltage value [22]. Integration of FE layer on TFET has drawn much attention in boosting the performance, i.e., possible structures for negative capacitance TFETs are metal- ferroelectric- insulator- semiconductor (MFIS), metal-ferroelectric-metal-insulator-semiconductor (MFIMIS), metal-ferroelectric-semiconductor (MFS) and metal-ferroelectric-insulator-semiconductor-insulator-ferroelectric-metal (MFISIFM) [23]. It is well known that a combination of FE layers in the gate will provide internal voltage gain, which ultimately enhances tunneling probability \( T_{WKB} \) and improves on-current [24]. Thus on-current is obtained by integrating tunneling probability \( T_{WKB} \) over the source-channel junction. Salahuddin et al. [5] have shown that replacing the standard oxide film with ferroelectric oxide boosts the drive current and lowers the subthreshold swing (SS) in CMOS devices. M. H. Lee et al. [24] found that employing a lead zirconate titanate (PZT) ferroelectric in a stacked gate method may lead to nearly doubling of subthreshold slope (SS) with a 16% increment in drain current. Livio Lattanzio et al. [25] in the initial stages of the research of such kind suggested new structures of TFETs that he named as ferroelectric Tunnel FET (Fe-TFET), with an SS of about 880 mV/dec, based on poly (vinylidene fluoride-trifluoro ethylene) P (VDF-TrFE). Avinash Lahgere [26] et al. suggested a new negative capacitance ferroelectric (TFET) depending on the charge plasma method for improved on-current and steep SS less than 42 mV/decade. They reported remarkable tenfold progress in on-current, a hundred fold reduction in \( I_{off} \), and \( I_{on}/I_{off} \) ratio of 10\(^{11}\). Ashish Kumar Singh et al. [27] presented a ferroelectric-based heterojunction TFET on SELBOX with a back gate having a reduced SS value of 38.6 mV/dec and a 9.22 \( \times \) 10\(^{10} \) on off ratio. Puja Ghosh et al. [28] recently noted an improved-ON current in the range of 10\(^{-5}\) A/\( \mu \)m and an on to off current ratio of 5.8 \( \times \) 10\(^{11}\) with a minimal subthreshold swing (SS) of 29 mV/dec. Although many studies have been conducted to analyze the impact of electrical parameters such as SS, Memory Window, \( I_{on}/I_{off} \) ratio, and others for various structural improvements. A prominent structure that exceeds previous efforts is still needed. The proposed negative capacitance structure is MFISIFM, i.e., Ultra-thin body double gate FE layer TFET (UTB-DG-Fe-TFET).

In addition, device is also able to be implemented for low powered circuit (e.g., inverter, ring oscillator [1, 10] and non-volatile memory like SRAM, DRAM [18, 29] etc.). The paper’s organization follows with theory in part 2, followed by device construction and simulation setup in part 3, following with results and discussion in part 4. Lastly, part 5 concludes the paper.

2 Theory

The main reason for using the interfacing layer \( SiO_2 \) in between \( Si : HFO_2 \) and intrinsic silicon channel in UTB-DG-Fe-TFET is to rectify the lattice mismatch problem [14, 16, 30]. Moreover, \( Si : HFO_2 \) is the most compatible with the flow of the CMOS manufacturing process due to its low value of dielectric constant and smoother interface behavior [29]. The enticing characteristic of FE material is negative capacitance, which behaves like a voltage step-up transformer. Therefore, SS and drain current are improved. Any CMOS device’s subthreshold swing is generally calculated as the ratio of variation of gate bias potential (\( V_g \)) to variation of subthreshold drain current by unity decade. Mathematically it can be expressed as:

\[
SS = \frac{\partial V_g}{\partial (log \text{ } 10 \text{ } I_d)} = \frac{\partial V_g}{\partial \psi_s} \frac{\partial \psi_s}{\partial (log \text{ } 10 \text{ } I_d)}
\]

Where \( m \) is the body factor used to calculate the effective twisting of surface potential at a specific bias, and \( n \) is the transport factor that tells how much current flows along the channel by lowering the potential. From Fig. 1, it is evident that the capacitor voltage divider rule clearly shows that \( V_g \) and \( \psi_s \) are correlated, that is

\[
m = \frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_e}{C_g}
\]

where \( \frac{1}{C_{eq}} = \frac{1}{C_{ox}} + \frac{1}{C_{fe}} \) is equivalent gate inter-facial capacitance, \( C_{ox} \) is inter-facial layer capacitance, \( C_s \) is semiconductor or intrinsic channel capacitance and \( C_{fe} \) is ferroelectric layer negative capacitance. If \( Q \) is total charge observed by total capacitance across gate \( C_g \), then equivalent gate inter-facial capacitance \( C_{eq} \) is calculated by following expression: \( C_{eq} = \frac{C_{ox}C_{fe}}{C_{ox} + C_{fe}} = \frac{Q}{V_g - \psi_s}. \) Effective voltage (\( V_g - \psi_s \)) is seen across \( C_{eq} \) and voltage in proportional with total charge \( Q \) also observed by \( C_g \) being expressed by (\( \beta \) \( Q \)) where \( \beta \) is internal amplification factor having value greater than unity. Therefore,

\[
Q = C_g [(V_g - \psi_s) + \beta \text{ } Q]
\]

\[
\Rightarrow Q = C_g (V_g - \psi_s) + C_g \beta \text{ } Q
\]

\[
\Rightarrow Q(1 - \beta) \text{ } C_g = C_g (V_g - \psi_s)
\]

\[
\Rightarrow C_{eq} = \frac{Q}{(V_g - \psi_s)} = \frac{C_g}{(1 - \beta \text{ } C_g)} = \frac{C_g}{(1 - V_{fb})}
\]

If \( V_{fb} = \beta \text{ } C_g \gg 1 \) then equivalent gate-inter-facial capacitance \( C_{eq} \) attain negative value; hence it is called negative capacitance TFET. In other sense, the feedback
voltage \((V_{fb} \gg 1)\) must be positive to behave as negative capacitance TFET. It also implies amplifying internal voltage and reducing body factor \(m\) as clear from Eq. 2. Overall, \(SS\) is significantly decreased, as evident from Eq. 1. Moreover, Eq. 1 suggests that \(\psi_s \gg V_g\), i.e., acts as a step-voltage transformer which ultimately results in an improved electric field and enhanced on-current. In case of MOSFET, body factor \(m = 1\) results into a lower limit of \(SS = 60\) mV/decade i.e., Eq. 1 results into \(SS = \frac{\partial \psi_s}{\partial \log(I_d)} = \frac{KT}{q}\ln10\approx 60\) mV/decade. Moreover, ferroelectric polarization results in getting body factor \(m < 1\) in the proposed device structure. The benefits of using FE material on the top and bottom surface of the intrinsic channel over perovskite material like PZT and SBT is the best scaling in the nanometer range. Voltage across the MOS \((V_{MOS})\) and voltage across the FE material \((V_{FE})\) is related by \(V_g = V_{MOS} + V_{FE}\). Voltage amplification is given by [31]:

\[
A_v = \frac{V_{MOS}}{V_g} = \frac{|C_{fe}|}{|C_{fe}|-|C_{MOS}|}.
\]

With \(|C_{fe}|\) is less than \(|C_{MOS}|\), voltage amplification factor yields into negative voltage gain.

### 3 Device Construction and Simulation Set Up

The cross-section perspective of the UTB-DG-FE-TFET is depicted in Fig. 1, including its capacitive modeling. The channel is enclosed by an interfacial layer \((SiO_2)\) to reduce inter-diffusion. In a stacking having dielectric \((SiO_2)\) on sidewalls, a ferroelectric sheet of silicon doped hafnium oxide \((Si:HFO_2)\) is utilized. Because of the lower value of the dielectric constant \((32.5)\), \(Si:HFO_2\) is preferred over Strontium Bismuth Tantalate \((SBT)\) and Lead Zirconate Titanate \((PZT)\) to lessen the impacts of fringing [32, 33]. It enables thinner ferroelectric layers. As a result, the gate stack ratio is better for scaling. Furthermore, \(Si:HFO_2\) is compatible with the CMOS manufacturing process flow [17]. Design must always utilize an interfacial layer with the substrate to minimize lattice mismatch and enhance \(SS\). However, the memory window is restricted owing to a voltage drop throughout the interfacial layer [34]. As a result, the best value of \(t_{ox} = 0.5\) nm is chosen. The source is highly doped, via an impurity concentration of \(10^{20} \text{ cm}^{-3}\), compared to a weakly doped drain with an impurity concentration of \(5 \times 10^{18} \text{ cm}^{-3}\), to diminish ambipolar conduction. The channel is weakly doped, while not being entirely intrinsic, with a trivalent impurity concentration of \(10^{16} \text{ cm}^{-3}\). Table 1 lists the device variables used in the simulation. On the 2D TCAD Sentaurus Simulator, the device construction is simulated and tested [35]. Applying Fermi-Dirac statistics and the impact of band-gap narrowing, heavy doping at the drain, and source concerning channel is studied. Concentration-dependent mobility model, electric field-dependent mobility, band-gap narrowing model, Schockley-Read-Hall (SRH) recombination model, auger recombination model, and non-local band to band tunneling (BTBT) model are some of the models that are employed throughout computations. Ideal ferroelectric sheet having remanent polarisation \(P_r\), coercive field \(E_c\), and saturation polarisation \(P_s\) are 10.75 \(\mu\)C/cm\(^2\), 1.15 MV/Cm, and 11.37 \(\mu\)C/cm\(^2\), respectively, to eliminate hysteresis loss difficulties such as dc breakdown, retention, as well as fatigue [36]. For gate material, the proper work function \((\psi_m = 4.6eV)\) is used.

### 4 Simulation Results and Discussion

The effect of ferroelectric thickness on electric parameters in UTB-DG-FE-TFET is discussed. The paper investigates
**Table 1** Experimental device parameters for the simulation

| Parameter                  | Symbol | Value   | Parameter                  | Symbol | Value   |
|----------------------------|--------|---------|----------------------------|--------|---------|
| Gate length                | $L_g$  | 15 nm   | Gate stack Thickness       | $t_g$  | 4 nm    |
| Source length              | $L_s$  | 20 nm   | Source Thickness           | $t_s$  | 10 nm   |
| Drain length               | $L_d$  | 20 nm   | Drain Thickness            | $t_d$  | 10 nm   |
| Channel length             | $L_c$  | 30 nm   | Interfacial layer thickness| $t_{ox}$ | 0.5 nm |
| Ferroelectric layer thickness | $t_{fe}$ | 2 nm   | Intrinsic channel thickness | $t_{si}$ | 10 nm   |

**4.1 Comparison of TCAD Model Physics with Referenced Data**

Transfer characteristics of UTB-DG-FE-TFET are examined and simulated using experimental parameters shown in Table 1 and also compared with FE-TFET [30] and conventional TFET [37, 38], respectively in Fig. 2. Proposed UTB-DG-FE-TFET almost provides two times improvement in $I_{on}$ and 20 times improvement in $I_{on}$ in comparison with FE-TFET and conventional TFET, respectively. One can observe that the proposed structure also gives $10^4$ times reduction in $I_{off}$ and $10^2$ times reduction in $I_{off}$ as compared to FE-TFET and conventional TFET, respectively. Internal voltage amplification, such as that provided by a voltage step-up transformer, is the cause of this occurrence, which finally yields into increment in $I_{on}$ and reduction in $I_{off}$, i.e., it leads to enhancement in the current level.

Due to the particular hysteresis behavior of FE materials, forward and reverse sweeps for voltage are introduced in transfer characteristics for the proposed structure in Fig. 3.

| Variation     | Ferro thickness (nm) | $I_{on}/I_{off}$ ratio | MW (V) | SSpoint (mV/dec) |
|---------------|----------------------|------------------------|--------|------------------|
| Proposed Work | 2                    | $7.117 \times 10^{13}$ | 0.32   | 23               |
|               | 4                    | $3.459 \times 10^{11}$ | 0.25   | 19.6             |
|               | 6                    | $1.165 \times 10^{11}$ | 0.21   | 17.3             |
| [33]          | 10                   | $5 \times 10^{13}$     | 1.8    | –                |
|               | 30                   | $7 \times 10^{12}$     | 4      | –                |
| [29]          | 10                   | $1 \times 10^7$        | 1.7    | –                |
|               | 15                   | $9 \times 10^6$        | 2.05   | –                |
|               | 20                   | $2 \times 10^6$        | 2.3    | –                |
| [34]          | 100                  | $1 \times 10^7$        | 1.8    | 46               |
| [31]          | 153                  | $1 \times 10^{10}$     | –      | 5                |
| [26]          | 3                    | $1 \times 10^{11}$     | –      | 18               |
| [27]          | 2                    | $9.22 \times 10^{10}$  | –      | 38.6             |
| [28]          | 4                    | $5.8 \times 10^{11}$   | –      | 5                |
Comparison of output characteristics of UTB-DG-FE-TFET with FE-TFET and conventional TFET at $V_{gs} = 1$ V is illustrated in Fig. 4. In triode region up to $V_{ds} = 0.2$ V, a channel is formed due to the availability of large charge carriers, and when the $V_{ds}$ is increased beyond 0.2 V, the large numbers of charge carries starts to tunnel. Thus, $I_{ds}$ shows a growing exponential curve due to the lowering of drain induced barrier. The lateral electrical field from the drain is halted through the channel. That’s why a perfect saturation is also seen in output characteristics [39].

Moreover, incomplete charge compensation and decrease in polarization also happened due to depolarization field in FE materials. Figure 5 illustrates that approximately the same window is granted for two different structures of 15 nm gate length UTB-DG-FE-TFET and 30 nm gate length FE-TFET by sweeping the gate voltage. Comparison results confirm that approximately the same memory window (0.32 V for 15 nm gate length UTB-DG-FE-TFET and 0.32 V for 40 nm gate length FE-TFET) is obtained. Moreover, One can observe an enhancement in $I_{on}$ and also a reduction in $I_{off}$. Thereby 15 nm gate length UTB-DG-FE-TFET structure could be the best alternative for enriched electric performance.

Apart from data storage properties of FE materials, the surface potential of UTB-DG-FE-TFET is boosted over FE-TFET, and conventional TFET; and the output current level is amplified [24]. For this purpose, the change in the channel surface potential of UTB-DG-FE-TFET, FE-TFET, and conventional TFET to the varied value of $V_{gs}$ is presented in Fig. 6. Additionally, Fig. 6 depicts the change...
in the surface potential curve as a measure of channel length from source to drain for UTB-DG-FE-TFET as determined by TCAD simulations. The entire length of the channel is assumed to be 30 nm. Every 10 nm, potential changes are detected. When the channel length grows up to 10 nm, it is apparent that the surface potential of UTB-DG-FE-TFET grows exponentially. As the length of the channel advances from 10 nm to 20 nm, the surface potential response climbs gradually, and it takes a little jump and then grows as the length of the channel rises. This implies that short channel effects (SCEs) are minimized, and on the drain side, the gate material behaves like a screened gate. The sudden shift primarily in potential profile caused by the extensive work function of metal seen in Fig. 6 is attributable to higher carrier velocity and therefore improved carrier transport efficiency, leading to a rise in the drain $I_{ds}$. According to Fig. 6, the UTB-DG-FE-TFET has no significant difference in potential from FE-TFET and conventional TFET on the source side but a negligible difference on the drain side. Finally, as before shown in Fig. 4, $V_{ds}$ has a minimal impact on $I_{ds}$ after saturation, and irrespective of the supplied drain bias voltage, there is a minimal change within the proportion of the lowest surface potential. In general, as the gate voltage rises, so does the height of the barrier on the source and drain sides. Thereby, the surface potential increases in the channel area. During the $V_{gs}$ sweep, the surface potential of the UTB-DG-FE-TFET was amplified above that of the FE-TFET and conventional TFET, which increased the B2BT. Figure 7 demonstrates the comparison of UTB-DG-FE-TFET electrical fields with FE-TFET and conventional TFET [32]. Under the bias conditions having $V_{gs} = 1$ V and $V_{ds} = 0.5$ V, the maximum electric field for UTB-DG-FE-TFET at the interface of source and channel is 37.5% greater than conventional TFET and 10% greater than FE-TFET. This is owing to the excellent characteristics of positive feedback caused by FE materials.

4.2 Effect of Ferrothickness on Subthreshold Swing, Threshold Voltage, Electric Field Dependent Polarization and $I_{on}/I_{off}$

Due to negative capacitance, voltage is amplified to a great extent but with negative potential gain. Subthreshold swing is a crucial parameter for understanding any MOS switching behavior [4]. It is found that Polarization of ferroelectric layer improves the value of point subthreshold swing $SS_{point}$ as shown in Fig. 8. Figure 8 shows that as $t_{fe}$ varies from 4 to 16 nm, $SS_{point}$ value is reported below 36 mV/decade for a range of approximately ten orders of magnitude. Average sub-threshold swing $SS_{average}$ is noticed around below 45 mV/decade in Fig. 9 for the various value of $t_{fe}$. Because the subthreshold properties are significantly improved, the device is appropriate for ultra-low energy switching applications.

Figure 10 demonstrates the relation between threshold voltage $V_{th}$ and intrinsic channel thickness $t_{si}$ for different values of $t_{fe}$. The figure also reveals that as the intrinsic channel thickness $t_{si}$ and the FE layer thickness $t_{fe}$ increases, so does $V_{th}$. This was primarily because the tunneling volume was reduced with a rise in $t_{si}$ and the feedback charge lowered since $t_{fe}$ increased [32, 37]. A FE layer of $t_{fe} = 16$ nm shows a relatively thinner hysteresis curve having greater polarization on the application of

![Figure 6](image1.png)

**Fig. 6** Surface potential $\psi(x)$ variation across the channel positions of UTB-DG-FE-TFET, FE-TFET, and conventional TFET with channel length $L_c = 30$ nm at constant $V_{ds} = 0.5$ V and $V_{gs} = 1$ V. TCAD simulated data with the same variables as stated in Table 1 is depicted by symbols in the surface potential curve as a measure of channel length from source to drain for UTB-DG-FE-TFET as determined by TCAD simulations. The entire length of the channel is assumed to be 30 nm. Every 10 nm, potential changes are detected. When the channel length grows up to 10 nm, it is apparent that the surface potential of UTB-DG-FE-TFET grows exponentially. As the length of the channel advances from 10 nm to 20 nm, the surface potential response climbs gradually, and it takes a little jump and then grows as the length of the channel rises. This implies that short channel effects (SCEs) are minimized, and on the drain side, the gate material behaves like a screened gate. The sudden shift primarily in potential profile caused by the extensive work function of metal seen in Fig. 6 is attributable to higher carrier velocity and therefore improved carrier transport efficiency, leading to a rise in the drain $I_{ds}$. According to Fig. 6, the UTB-DG-FE-TFET has no significant difference in potential from FE-TFET and conventional TFET on the source side but a negligible difference on the drain side. Finally, as before shown in Fig. 4, $V_{ds}$ has a minimal impact on $I_{ds}$ after saturation, and irrespective of the supplied drain bias voltage, there is a minimal change within the proportion of the lowest surface potential. In general, as the gate voltage rises, so does the height of the barrier on the source and drain sides. Thereby, the surface potential increases in the channel area. During the $V_{gs}$ sweep, the surface potential of the UTB-DG-FE-TFET was amplified above that of the FE-TFET and conventional TFET, which increased the B2BT. Figure 7 demonstrates the comparison of UTB-DG-FE-TFET electrical fields with FE-TFET and conventional TFET [32]. Under the bias conditions having $V_{gs} = 1$ V and $V_{ds} = 0.5$ V, the maximum electric field for UTB-DG-FE-TFET at the interface of source and channel is 37.5% greater than conventional TFET and 10% greater than FE-TFET. This is owing to the excellent characteristics of positive feedback caused by FE materials.

4.2 Effect of Ferrothickness on Subthreshold Swing, Threshold Voltage, Electric Field Dependent Polarization and $I_{on}/I_{off}$

Due to negative capacitance, voltage is amplified to a great extent but with negative potential gain. Subthreshold swing is a crucial parameter for understanding any MOS switching behavior [4]. It is found that Polarization of ferroelectric layer improves the value of point subthreshold swing $SS_{point}$ as shown in Fig. 8. Figure 8 shows that as $t_{fe}$ varies from 4 to 16 nm, $SS_{point}$ value is reported below 36 mV/decade for a range of approximately ten orders of magnitude. Average sub-threshold swing $SS_{average}$ is noticed around below 45 mV/decade in Fig. 9 for the various value of $t_{fe}$. Because the subthreshold properties are significantly improved, the device is appropriate for ultra-low energy switching applications.

Figure 10 demonstrates the relation between threshold voltage $V_{th}$ and intrinsic channel thickness $t_{si}$ for different values of $t_{fe}$. The figure also reveals that as the intrinsic channel thickness $t_{si}$ and the FE layer thickness $t_{fe}$ increases, so does $V_{th}$. This was primarily because the tunneling volume was reduced with a rise in $t_{si}$ and the feedback charge lowered since $t_{fe}$ increased [32, 37]. A FE layer of $t_{fe} = 16$ nm shows a relatively thinner hysteresis curve having greater polarization on the application of
the highest electric field to get deep saturation that is evident from Fig. 11. Therefore, current level enhances in thinner FE layer with maximum negative capacitance. Due to spontaneous polarization in ferroelectric, a non-linear relationship exists between polarization and electric field, represented by a hysteresis loop. On increasing $t_{fe}$, magnetic polarization tries to become zero, as illustrated in Fig. 11. Thereby, Coercive field strength reduces considerably. Therefore, simulation results validate that characteristics governing parameter are $t_{fe}$ and memory window value is raised dramatically. The primary concern in the design of the proposed device is to choose an optimum value of FE layer thickness so that three key parameters SS, memory window, and drain current, are improved. Therefore, former is reduced, and the latter is increased.

Recently explored silicon doped hafnium oxide (Si:HFO$_2$) is selected not only to provide relatively coercive field $E_c$ over PZT (Lead-Zirconate-Titanate) and SBT (Strontium-Barium-Titanate) but also to present a large memory window [29].

Figure 12 depicts a summary of the effect of the ferroelectric device layer thickness on the $I_{on}/I_{off}$ ratio of the ferroelectric device. Figure 12 illustrates that the drive current $I_{on}$ rises as the thickness of the ferroelectric layer decreases due to polarisation trapped charges while the OFF current remains similar. This improves the ratio of $I_{on}/I_{off}$, as the ferroelectric layer’s thickness decreases.

At $t_{fe} = 2$ nm, it was discovered that the proposed device had a better SS, a large ratio of $I_{on}/I_{off}$, and a significant
memory window. Since the ferroelectric layer is placed on top and bottom of the gate dielectric. The ferroelectric layer thickness is controlled to get the best band to band tunneling (BTBT).

4.3 Effect of Device Geometry Variants on Transfer Characteristics

Figure 13 illustrates the logarithmic effect of ferroelectric layer thickness on drain current while changing gate voltage on a linear scale. Table 3 shows the ferroelectric characteristics for different Si:HFO$_2$ layer thicknesses. Table 4 displays the device’s parameter value concerning different device geometry variations. Table 4 demonstrates that improved SS, large memory window and high on-off current ratio are regarded to be the most suitable value when compared with other variations at $t_{fe} = 2$ nm, $t_{ox} = 0.5$ nm, $t_{si} = 10$ nm, SiO$_2$ as interfacial layer type and $L_c = 30$ nm.

The ferroelectric layer thickness has a significant effect on device performance. Negative capacitance rises as $t_{fe}$ decreases resulting in increased trapped charge density. These trapped charge densities within this ferroelectric sheet create a channel and start a tunneling process at low $V_{gs}$. It can be shown that when the thickness of ferroelectric oxide $t_{fe}$ increases from 2 nm to 4 nm, 6 nm, etc., the drain current significantly reduces. With an increase in $t_{fe}$, this results in the creation of a low feedback charge. However, in the absence of the FE layer ($t_{fe} = 0$), the drain current is observed to be less because of the absence of positive feedback. For $t_{fe} > 0$, a high current is seen due to positive feedback introduced by negative capacitance. Yet the coercive field $E_c$ hardly reduces on increasing $t_{fe}$. So it leads to an apparent dependency of $t_{fe}$ on the memory window (MW). For this reason, MW rises from 0.21 V to 0.32 V substantially.

Figure 14 illustrates the influence of varying the intrinsic channel thickness $t_{si}$ on the $I_{ds}$-$V_{gs}$ curve. The drain current $I_{ds}$ decreases with $t_{si}$, as shown in the figure. The reason for this is that when $t_{si}$ rises, the tunneling volume decreases. Moreover, one can notice that the memory window (MW) falls with $t_{si}$ due to a reduction in the coercive field $E_c$.

Figure 15 shows the impact of various interfacial layer types, i.e., 0.5 nm SiO$_2$ layer is replaced by HFO$_2$ and then by Si$_3$N$_4$. Detailed analysis is done by SiO$_2$ only because of two limitations of HFO$_2$: (i) lattice mismatch problem between HFO$_2$ and silicon substrate during fabrication process (ii) deterioration of $I_{on}/I_{off}$, instead of large ON current and large memory window of 0.56 V.

Impact of various interfacial layer thickness $t_{ox}$ of SiO$_2$ interfacial layer on transfer curve $I_{ds}$-$V_{gs}$ is depicted in Fig. 16. For the moderate value of $t_{ox} = 0.5$ nm, the enormous electric field is induced by a more significant voltage drop in the substrate material at the tunneling interface. Thus, on current increases with greater memory window as compared to a thicker layer of $t_{ox} = 1$ nm. Effective oxide thickness $t_{ox} = 0.5$ nm is one of optimum

![Fig. 12](image_url) Change in $I_{on}/I_{off}$ ratio with ferrothickness $t_{fe}$

![Fig. 13](image_url) Impact of different FE layer thickness on transfer characteristics

| $t_{fe}$ (nm) | $\varepsilon_r$ | $P_r$ ($\mu$C/cm$^2$) | $P_s$ ($\mu$C/cm$^2$) | $E_c$ (MV/cm) |
|-------------|---------|----------------|----------------|-------------|
| 2           | 37.2    | 13.5           | 13.7           | 1.52        |
| 4           | 35.8    | 12.1           | 12.2           | 1.48        |
| 6           | 33.1    | 10.65          | 10.7           | 1.44        |

Table 3 Si:HFO$_2$ ferroelectric characteristics increasing $t_{fe}$
Table 4 Extracted parameter value

| Device geometry variants | MW (V) | $V_{th}$ (V) | SS (mV/dec) | $I_{on}/I_{off}$         |
|--------------------------|--------|--------------|-------------|--------------------------|
| $t_{fe}$ (nm)            |        |              |             |                          |
| 2                        | 0.32   | 0.38         | 23          | $7.1 \times 10^{13}$     |
| 4                        | 0.25   | 0.59         | 19.6        | $3.4 \times 10^{14}$     |
| 6                        | 0.21   | 0.61         | 17.3        | $1.1 \times 10^{14}$     |
| $t_{si}$ (nm)            |        |              |             |                          |
| 10                       | 0.32   | 0.38         | 23          | $4.1 \times 10^{12}$     |
| 12                       | 0.22   | 0.50         | 26.5        | $2.3 \times 10^{14}$     |
| 14                       | 0.19   | 0.51         | 21.3        | $1.2 \times 10^{10}$     |
| Interfacial layer types  |        |              |             |                          |
| $HFO_{2}$                | 0.56   | 0.31         | 20.6        | $3.1 \times 10^{12}$     |
| $Si_{3}N_{4}$            | 0.41   | 0.32         | 21.5        | $5.1 \times 10^{14}$     |
| $SiO_{2}$                | 0.32   | 0.38         | 23          | $2.4 \times 10^{10}$     |
| $t_{ox}$ (nm)            |        |              |             |                          |
| 0.25                     | 0.31   | 0.45         | 38.5        | $2.3 \times 10^{12}$     |
| 0.5                      | 0.41   | 0.42         | 31.3        | $4.6 \times 10^{12}$     |
| 1                        | 0.37   | 0.38         | 23          | $3.1 \times 10^{14}$     |
| $L_{c}$ (nm)             |        |              |             |                          |
| 10                       | 0.32   | 0.36         | 13.7        | $5.6 \times 10^{14}$     |
| 20                       | 0.41   | 0.51         | 21.4        | $4.8 \times 10^{12}$     |
| 30                       | 0.58   | 0.65         | 23          | $3.1 \times 10^{13}$     |
| 70                       | 0.58   | 0.75         | 37.6        | $6.8 \times 10^{11}$     |

dimension over standard CMOS high dielectric/metal gate technique. In addition, for $t_{ox} = 0.25$ nm, on current is less with reduced memory window. Effect of different channel length $L_{c}$ on $I_{ds}$-$V_{gs}$ transfer curve is depicted in Fig. 17. It is noticed from the figure that $I_{on}$ remains the same for channel length up to 30 nm while the same $I_{off}$ is obtained for channel length greater than 20 nm. The figure shows that on-current $I_{on}$ decreases for channel length greater than 30 nm, and off-current $I_{off}$ rises for channel length smaller than 20 nm. The best suitable channel length $L_{c} = 30$ nm is chosen because of the larger $I_{on}$ and memory window.

5 Conclusions

UTB-DG-FE-TFET is demonstrated using Sentaurus TCAD simulation to investigate electrical characteristics like a surface potential $\psi$ (x), drain current $I_{ds}$, threshold voltage $V_{th}$, and subthreshold swing (SS) over conventional TFET and FE-TFET using Sentaurus TCAD 2D simulator. The results indicate that the current level is raised by increasing the gate voltage, with a drop in the off-current compared to other TFETs. It is also noticed that surface potential is boosted along with the channel position, and
at the source-channel interface, there seems to be a maximum electrical field. In contrast, $V_{th}$ rises with increment in $t_{si}$ and $t_{fe}$ and thinnest hysteresis loop is obtained for larger $t_{fe}$. It is also noticed that $SS_{point}$ and $SS_{average}$ are improved against $I_{ds}$ for different value of $t_{fe}$. Moreover, Effect of larger $t_{fe}$ and $t_{si}$ results into reduced tunneling current. While the type of interfacial layer, especially SiO$_2$ layer having $t_{ox} = 0.5$ nm over HFO$_2$ and Si$_3$N$_4$ is found to be best suitable because of lattice mismatch problem faced by HFO$_2$ against silicon substrate. In addition, larger on-current as well as huge width of memory window is noted for $t_{ox} = 0.5$ nm. Finally, channel length $L_c$ also has a significant effect on transfer characteristics. Furthermore, a high $I_{on}$ and a very little $I_{off}$ was shown for the proposed design to produce outstanding $I_{on}/I_{off} \approx 10^{13}$. Thus, Such TFETs may be appealing for ultra-low-power circuit applications like inverter, ring oscillator, and non-volatile memory like SRAM, DRAM while still providing high performance.

Acknowledgements The authors would like to acknowledge the support of the VLSI Laboratory at MNIT, Jaipur, originated from the SMSP-C2SD Project funded by MeitY, Govt. of India, for providing all the facilities for carrying out the work.

Author Contributions Girdhar Gopal Conceptualization, TCAD Simulation, Writing and Editing. Tarun Varma Supervision, Reviewing, Investigation and Validation.

Funding The authors received no financial support for their research, writing, or publication of this paper.

Declarations

In research involving human participants, all procedures were carried out in compliance with ethical guidelines.

Conflict of Interests The authors declare that they have no conflict of interest.

References

1. Nirschl T, Fischer J, Fulde M, Bargagl-Stoffi A, Sterkel M, Sedlmair J, Weber C, Heinrich R, Schaper U, Einfeld J, et al. (2006) Scaling properties of the tunneling field effect transistor (tft): Device and circuit. Solid-state Electron 50(1):44–51
2. Jena B, Bhol K, Nanda U, Taysal S, Routray SR (2021) Performance analysis of ferroelectric gaa mosfet with metal grain work function variability. Silicon 1–8
3. Vanlalawmpuia K, Bhowmick B (2019) Linearity performance analysis due to lateral straggle variation in hetero-stacked tft. Silicon 1–7
4. Sakib FI, Mullick FE, Shahnawaz S, Islam S, Hossain M (2019) Influence of device architecture on the performance of negative capacitance mfmis transistors. Semiconductor Science and Technology 35(2):025005
5. Salahuddin S, Datta S (2008) Can the subthreshold swing in a classical fet be lowered below 60 mv/decade? In: 2008 IEEE International Electron Devices Meeting. IEEE, pp 1–4
6. Taysal S, Ajayan J, Joseph LL, Tarunkumar J, Nirmal D, Jena B, Nandi A (2021) A comprehensive investigation of vertically stacked silicon nanosheet field effect transistors: an analog/rf perspective. Silicon 1–8
7. Zhang Q, Zhao W, Seabaugh A (2006) Low-subthreshold-swing tunnel transistors. IEEE Electron Dev Lett 27(4):297–300
8. Taysal S, Vibhu G, Meena S, Gupta R (2021) Optimization of device dimensions of high-k gate dielectric based dg-tft for improved analog/rf performance. Silicon 1–7
9. Varma T, Periasamy C, Boolchandani D (2018) Performance evaluation of bottom gate zno based thin film transistors with different w/l ratios for uv sensing. Superlattice Microst 114:284–295
10. Ionescu A, Riel H (2011) Tunnel field-effect transistors as energy-efficient electronic switches. Nature 479:329–37, 11
11. Toh E-H, Wang GH, Samudra G, Yeo Y-C (2008) Device physics and design of germanium tunneling field-effect transistor with source and drain engineering for low power and high performance applications. J Appl Phys 103(10):104504
back gated ferroelectric tfet on selbox substrate for ultra low power applications. Silicon 1–11
28. Ghosh P, Bhowmick B (2020) Investigation of electrical characteristics in a ferroelectric l-patterned gate dual tunnel diode tfet. IEEE Transactions on Ultrasonics Ferroelectrics, and Frequency Control 67(11):2440–2444
29. Saeidi A, Biswas A, Ionescu AM (2016) Modeling and simulation of low power ferroelectric non-volatile memory tunnel field effect transistors using silicon-doped hafnium oxide as gate dielectric. Solid State Electron 124:16–23
30. Ionescu AM, Lattanzio L, Salvatore GA, De Michielis L, Boucart K, Bouvet D (2010) The hysteretic ferroelectric tunnel fet. IEEE Trans Elect Dev 57(12):3518–3524
31. Liu C, Chen P-G, Xie M-J, Liu S-N, Lee J-W, Huang S-J, Liu S, Chen Y-S, Lee H-Y, Liao M-H et al (2016) Simulation-based study of negative-capacitance double-gate tunnel field-effect transistor with ferroelectric gate stack. Japanese Journal of Applied Physics 55(4S):04EB08
32. Kumar S, Goel E, Singh K, Singh B, Kumar M, Jit S (2016) A compact 2-d analytical model for electrical characteristics of double-gate tunnel field-effect transistors with a sio 2/high-k stacked gate-oxide structure. IEEE Trans Elect Dev 63(8):3291–3299
33. Mueller S, Yurchuk E, Slesazeck S, Mikolajick T, Müller J, Herrmann T, Zaka A (2013) Performance investigation and Optimization of si HfO 2 fetes on a 28 nm bulk technology. In: 2013 IEEE International Symposium on Applications of Ferroelectric and Workshop on Piezoresponse Force Microscopy (ISAF/PFM). IEEE, pp 248–251
34. Rusu A, Salvatore GA, Jiménez D, Ionescu AM (2010) Metal-ferroelectric-meta-oxide-semiconductor field effect transistor with sub-60mv/decade subthreshold swing and internal voltage amplification. In: 2010 International Electron Devices Meeting, pp 16.3.1–16.3.4
35. Synopsys T (2009) Sentaurus device user’s manual. Mountain view, CA
36. Biswas A, Dagtekin N, Grabinski W, Bazigos A, Le Royer C, Hartmann J-M, Tabone C, Vinet M, Ionescu AM (2014) Investigation of tunnel field-effect transistors as a capacitor-less memory cell. Appl Phys Lett 104(9):092108
37. Boucart K, Ionescu AM (2007) Double-gate tunnel fet with high-k gate dielectric. IEEE Trans Elect Dev 54(7):1725–1733
38. Yadav M, Bulusu A, Dasgupta S (2015) Super-threshold semi analytical channel potential model for dg tunnel fet. J Comput Electron 14(2):566–573
39. Venkatesh M, Balamurugan N (2021) Influence of threshold voltage performance analysis on dual gate stacked triple material dual gate tfet for ultra low power applications. Silicon 13(1):275–287

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.