Calculation and Experiment of Stray Inductance of PCB Double-Pulse Test Circuit Based on Three-Dimensional Simulation

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This work was supported in part by Sichuan Province Science and Technology Plan Project under Grant 2020YFG0184, in part by the Open project of the State Key Laboratory of Traction Power under Grant TPL1907 and the Key Scientific Research Fund of Xihua University under Grant Z1520909.

ABSTRACT In high-frequency electronic equipment and power electronic devices, the dynamic performance of switching devices is one of the important indicators, and a double-pulse test circuit is usually used to test the dynamic performance of switching devices. In order to reduce the stray inductance existing in the test circuit, a double-pulse test circuit structure based on PCB is firstly proposed, and then the basic principle of using the integral calculation method to extract the PCB stray inductance is analyzed. Then the 3D model of the PCB is established, and the PCB stray inductance extraction based on 3D simulation is completed. Finally, a 1200V/100A double-pulse test experimental platform is built. By comparing the three-dimensional simulation results with the numerical calculation results using the integral method under the double-pulse test experiment, the accuracy and effectiveness of the three-dimensional simulation method proposed in this paper are verified.

INDEX TERMS Printed circuit board (PCB), stray inductance, 3D simulation, double-pulse test, integration method

I. INTRODUCTION

With the rapid development of technology and economy, power electronic systems and electronic equipment are also developing rapidly. Among them, the requirements for power level, switching frequency and response speed of power semiconductor devices are getting higher and higher, and the volume and power of equipment and devices are increasing. Density requirements are getting higher and higher. At present, the Insulated Gate Bipolar Transistor (IGBT) can reach a voltage level of 6500V, a current level of 3600A, and a switching time of only about 0.2μs. At such a high voltage level and switching frequency, the stray inductance in the loop will cause a greater \( \frac{di}{dt} \), this will induce a higher voltage spike [1]-[2]. Voltage spikes often bring abnormal pulses to the device, causing problems such as high-frequency noise and EMI pollution [3]-[5]. For the inductance of the loop, the inductance of the switching device and the inductance of the connector, the interference and EMI caused by the circuit can be weakened by increasing the snubber circuit topology design or introducing passive and active filters [6]-[7]. However, the related problems caused by the existence of stray inductance in the PCB are still difficult to solve.

PCB with the advantages of small size, low loss and good parameter consistency have been widely used in switching power supplies and have gradually become one of the main components in power electronic systems and electronic equipment [8]. Due to its compact size, the PCB can greatly reduce the stray inductance, can effectively suppress the voltage spike when the switching device is turned off, and further improve the precision of the circuit structure. The stray inductance and current distribution of the PCB have a great influence on the PCB itself and the electrical performance of the equipment and system. Therefore, understanding the generation principle of its stray inductance and accurately extracting the stray inductance in the loop of great significance for optimizing the performance of the PCB and its corresponding equipment and systems.
Researchers have done a lot of work in studying the extraction of stray inductance. The common extraction methods include off-line test with impedance analyzor, analysis by numerical calculation, analytical method [9]-[11]. These methods have certain engineering guiding significance for extracting stray inductance in simple loops and have high accuracy.

The double-pulse test method is a classic test method. The voltage and current transient waveforms of the IGBT are obtained by testing, and then the differential relationship between the inductor current and the voltage is used to calculate, and the rate of change of the current \( \frac{di}{dt} \) is calculated by a linear approximation. After studying the turn-on and turn-off process of IGBTs in the literature [12], a laminated bus-bar structure was proposed to reduce the overall influence of stray inductance on the device and improve the performance stability of the device to a certain extent. However, the stray inductance existing at the connections between the bus bars still need to be further studied and solved. In [13] obtained the transient waveform of IGBT turn-on and turn-off through the double pulse test. The \( V_{ce} \) voltage drop during the second turn-on was used as the voltage value to calculate the stray inductance, and the waveform of the collector current during this period was used at the same time. Reference [14] uses the integral method to extract the stray inductance of the loop with complex structure, which reduces the influence of the current change rate and the waveform error on the accuracy. This method has certain reference value for extracting the stray inductance of the loop with complex structure. The above-mentioned design for reducing stray inductance structure and related stray inductance extraction methods have certain engineering application value, but for PCB with more compact and complex components distribution, the extraction method of stray inductance is less studied.

On the basis of the above research, this paper proposes a circuit structure of double-pulse test based on PCB. Firstly, the applicability of the integral method to extract the stray inductance of the test loop is analyzed. Secondly, the stray inductance of the entire loop of the double-pulse test circuit based on the PCB structure is extracted by establishing a three-dimensional model, and the current distribution in the PCB is calculated. Finally, combined with the double-pulse test experiment, the simulation results are compared with the numerical results of the PCB stray inductance calculated by the integral method, which further verifies the validity and accuracy of the three-dimensional simulation method in this paper.

II. STRAY INDUCTANCE EXTRACTION METHOD OF DOUBLE PULSE TEST CIRCUIT

The traditional stray inductance extraction method usually adopts the double pulse test method to realize, and its test circuit is shown in Fig. 1. It can be seen from the schematic diagram of the circuit that when the circuit is running, the switch S1 is closed at the beginning, DC power supply \( U_i \) charges its parallel DC support capacitor \( C \) to the value of \( V_{ce} \). After charging is completed, switch S1 is turned off, and then a pulse signal is applied to the IGBT. During the IGBT turn-off process, due to the existence of stray inductance \( L_s \) in the loop, voltage spikes will appear at both ends of the IGBT. Since the freewheeling diode \( D \) is forward-conducting at this time, the voltage on it will have a positive overshoot. In consideration of this, the transient waveform during the second turn-on pass of the IGBT is generally used to extract the stray inductance. In the circuit, the resistance \( R \) is the sampling resistance used to measure the IGBT collector current.

The second turn-on transient waveform of the IGBT in the traditional double pulse method is shown in Fig. 2. At \( t_s \), the IGBT is turned on, and the current \( i_c \) increases from zero, due to the effect of \( \frac{di}{dt} \), a voltage opposite to the capacitor voltage will be induced on the loop stray inductance, superimposed on both ends of the IGBT. At this time, the voltage \( V_{ce} \) starts to drop from \( V_{ce} \). In practical engineering applications, if the measured voltage drop of the freewheeling diode is very small, the influence of the voltage drop on the calculation result of the stray inductance can be ignored [14].

The traditional method uses the rising phase of the collector current and the phase of the voltage difference across the IGBT to calculate the stray inductance value. In the traditional method, the current change rate needs to obtain an accurate value, and the turn-on voltage waveform and current waveform also have a great influence on the calculation result, so using this method will make the result have a large error. The integration method integrates the voltage on the time scale. At this time, the calculation of the current change rate in the traditional differential method is not required, which avoids the error caused by using a linear approximation method to calculate the current change rate [15]-[16]. Based on the above analysis, this paper uses the integral method to numerically calculate the stray inductance of the PCB loop. In practice, the IGBT collector-emitter voltage \( V_{ce} \) and the voltage across the freewheeling diode \( V_{di} \) are measured by two different voltage probes. Obtain the IGBT collector current \( i_c \) from the sampling resistor \( R \).
FIGURE 1. Double pulse test circuit diagram

On the basis of the schematic diagram of the double pulse test circuit, combining Kirchhoff's voltage law, it can be obtained:

\[ V_c - V_d - V_{ce} = L_s \frac{I_{cm} - I_{cm}'}{t_m - t_m'} \]  

(1)

So, the method of extracting the stray inductance \( L_s \) of the double pulse test using the integral method [15] is:

\[ L_s = \frac{\int (V_c - V_d - V_{ce})dt}{I_{cm} - I_{cm}'} \]  

(2)

In formula (1) and formula (2), \( I_{cm} \) and \( I_{cm}' \) are the current values of the IGBT corresponding to the moments of \( t_m \) and \( t_m' \) respectively. According to the above theoretical analysis, the necessary condition for the integration method to be effective at all stages is that the denominator of formula (2) is not zero, therefore, moments \( t_m \) and \( t_m' \) can be chosen arbitrarily. In Fig. 3, the current of the IGBT in the \( t_0 - t_2 \) stage rises approximately linearly, and a voltage is induced in the stray inductance of the PCB, which causes the voltage of the PCB to drop at this time. At this stage, the change of current \( i_c \) is more obvious, which is suitable for the extraction of stray inductance.

FIGURE 2. IGBT second turn-on waveform

III. 3D SIMULATION OF STRAY INDUCTANCE

In this paper, a 3D simulation model of the PCB structure test circuit board is established, and the stray inductance of the entire circuit is extracted through the Q3D Extractor module in Ansys Electronics Desktop, and the current distribution in the PCB is solved, which provides a certain reference value for engineering applications.

A. 3D SIMULATION MODEL ESTABLISHMENT

Ansys Electronics Desktop is a section of the industry leading. Ansys series software is suitable for electromagnetic field analysis. It is an important electromagnetic field analysis tool for the development of various electromechanical products such as motors, transformers, inductance, and magnetic field analysis. The Q3D Extractor module in Ansys Electronics Desktop is a practical tool for extracting the parasitic parameters of the integrated circuit board composed of PCB and electronic devices. This article uses the Q3D Extractor tool to perform a three-dimensional simulation of the stray inductance parameters of the designed PCB [17]-[18].

Common PCB is laminated by core layers. The substrate layers are bonded by prepreg layers. The upper and lower surfaces of each substrate layer are copper-clad metal layers. The metal layers can be connected by metal vias. The PCB surface is also coated with a solder mask and a silk screen layer that identifies the device and model. PCB can be divided into single-sided structure, double-sided structure, and multi-sided structure. The single-sided structure PCB has one substrate layer and one metal layer, without metal vias and no prepreg layers; the double-sided structure PCB has one substrate layer and two metal layers, with metal vias and no prepreg layers; multi-sided structure PCB generally consist of multiple substrate layers superimposed and bonded by prepreg...
layers. Each substrate layer has two metal layers on the upper and lower surfaces with metal vias. There are some structural characteristics. The first one is that the whole is a non-homogeneous, relatively flat laminated structure. The second one is that the material of the substrate layer and the prepreg layer is generally FR-4 type epoxy resin insulating material. The third one is that the thickness of substrate layer is generally greater than 500μm, and the thickness of the prepreg layer is about 100μm. The last one is that the metal layer material is generally copper, and the thickness is generally 18-105μm [19].

Fig. 4 is a schematic diagram of a typical multi-layer PCB construction. It can be seen from figure that the whole PCB is laminated by 3 core layers and 2 substrate layers. The surfaces of top and bottom layer are copper-clad metal layers, which can be connected by metal vias. With a multi-layer board, it would typically dedicate one complete layer to a ground plane (InternalPlane1), and another to power VCC (InternalPlane2). There would even be a few signal tracks on the power layer if the design requires.

**FIGURE 4. Typical multi-layer PCB construction [20]**

In high-speed design, the ground plane is fundamental to preserving the integrity of signals and reducing EMI emissions. Double-sided design can offer the chance to make use of good ground plane techniques and it is suitable for high frequency design [20]. Based on the above analysis, double-sided PCB is chosen as the research object of this paper. The PCB of the double-sided structure has one substrate layer and two metal layers, with metal vias and no prepreg layers. Fig. 5 shows the 3D simulation model built by Ansys software. The specific structural parameters are shown in TABLE I. Combined with the double-pulse test circuit shown in Fig. 1 and the basic structure of PCB, to better illustrate the simulation process, the resistor $R$, IGBT and freewheeling diode $D$ are replaced by commutation circuit and connecting conductors 1 and 2. The conduction path of the PCB and the components in the three-dimensional model are divided into four parts according to the circuit. The corresponding relationship between the three-dimensional model and the circuit is shown in Fig. 6 and TABLE II. In the entire double-sided PCB, a total of 4 metal vias are used. The metal vias 1 and 2 are in a parallel relationship with the two vias on the right, respectively. Each metal via has an outer ring radius of 8 mm and an inner ring radius of 4 mm. The height of the entire via is 1.618 mm. The specific structure of the metal via is shown in Fig. 7.

**FIGURE 5. 3D simulation model of PCB**

| Structure         | Length | Width | Thickness |
|-------------------|--------|-------|-----------|
| Substrate         | 22 cm  | 16 cm | 1.6 mm    |
| Copper row 1      | 15 cm  | 13.5 cm | 18 μm    |
| Copper row 2      | 15 cm  | 4 cm  | 18 μm    |
| Copper row 3      | 15 cm  | 3 cm  | 18 μm    |
| Lower metal layer | 21.5 cm | 15 cm | 18 μm |

**FIGURE 6. Correspondence diagram of circuit and model**
TABLE II
CORRESPONDENCE BETWEEN MODEL AND CIRCUIT

| Model structure          | Corresponding position of the circuit |
|--------------------------|---------------------------------------|
| Metal vias (1, 2)        | 1                                     |
| Connecting conductor 1   | 2                                     |
| Connecting conductor 2   | 3                                     |
| Commutation circuit      | 4                                     |

**FIGURE 7. 3D cross-sectional view of metal vias**

**B. ANALYSIS OF CURRENT FLOW PATH IN PCB**

As shown in the three-dimensional model in Fig. 5 above, metal via 1 is selected as the positive electrode, and metal via 2 as the negative electrode. Apply DC excitation. The closed loop path is Metal via 1 $\rightarrow$ Lower metal layer $\rightarrow$ Commutation circuit $\rightarrow$ Copper row 3 $\rightarrow$ Connecting conductor 1 $\rightarrow$ Copper row 2 $\rightarrow$ Connecting conductor 2 $\rightarrow$ Copper row 1 $\rightarrow$ Metal via 2.

**C. MESHING**

The finite element numerical method uses grids to discretize the space. The finite element grid must be refined enough to analyze the spatial changes of the field with high accuracy, but the problem is that the solution time increases, and the memory usage increases. Therefore, ideally, small grids should be used for areas with a large rate of change in physical space; large grids should be used for other areas. According to the above principles, in the actual simulation process, small-cell grids are used for connecting conductors, current concentration points and commutation circuit; large-cell grids are used for the division of the main part of the copper rows and substrate.

The meshing results of the PCB are shown in Fig. 8. From the figure, the grids at the connecting conductors and the edges of the metal layer on the PCB are smaller and denser, while the grids on the remaining parts are relatively sparse. At the same time, it can be seen that the grids are more densely divided at the current concentration and near the commutation loop.

Under such mesh division, it not only solves the convergence and accuracy problems of Ansys when calculating stray inductance, but also ensures that the entire PCB model can be solved in a short time.

**FIGURE 8. 3D PCB meshing results**

**D. SIMULATION RESULTS**

Based on the above-built 3D simulation model and the analysis of the current flow path in the PCB, add excitation to metal via 1 and metal via 2. Each metal via selects the surface through which the current flows as the Source. The surface of the current flows out is used as a Sink, and the entire conductive loop is set as a Signal Net.

In simulation, the solver is used in the software to calculate the stray inductance value in the PCB loop. Ansys software uses Maxwell's equations as the basis for numerical calculations and needs to achieve a convergence of the equations by setting the convergence precision and the maximum number of iterations in the solver. During the actual simulation, the convergence accuracy in the solver is set to 0.1% and the maximum number of iterations is set to 20. Through running the solver, the solver reached target convergence accuracy after a total of 19 iterations. In order to observe the data trend more intuitively, MATLAB is used to perform data fitting processing on the Ansys simulation results.
Fig. 9 below shows the effect of the iterative process of stray inductance calculation under three conditions of 1 kHz, 10 kHz, and 1 MHz. It can be seen from the figure, after many iterations, the results of the three cases are similar, and the stray inductance value of the entire PCB loop under the 3D simulation is about 32nH.

After obtaining the stray inductance, the current flow path diagram of the three-dimensional simulation model can be obtained at the same time. Fig. 10 below shows the current distribution in the PCB calculated by Ansys, which is basically consistent with the previous analysis of the current flow path. It can be seen from the distribution diagram that the current distribution at the edge of the metal layer, the connecting conductor and the commutation circuit is relatively concentrated, and the current distribution in the conductor presents a mirror image distribution.

The test experiment was carried out on the built test platform, and the test DC voltage was selected as 600V. During the experiment, two DC voltage probes with a withstand voltage of 1000V were used to measure the IGBT collector-emitter voltage $V_{ce}$ and driving voltage $V_g$ respectively. The collector current $i_c$ of the IGBT was sampled with a 0.05 Ω resistor and was directly connected to the oscilloscope through the coaxial line of the BNC interface. The double-pulse test signal was set as the first pulse signal width is 180μs, the second pulse signal width is 5μs, and the intermediate interval is 20μs.

Fig. 12 shows the waveform of the double-pulse test experiment, and Fig. 13 shows the transient waveform of the second switching on of the IGBT. It can be seen from Fig. 13 that the voltage and current synchronization effect of the test
platform is relatively good, indicating that its stray inductance is relatively small. When the device is turned on, the delay is about 380ns, and the oscillation at the time of turning on is small. Some dynamic parameters of the device are shown in TABLE III.

| Device parameters | Value |
|-------------------|-------|
| Opening time $t_{on}$ | 380ns |
| Off time $t_{off}$ | 430ns |
| Peak voltage $V_{peak}$ | 680V |
| Peak current $I_{peak}$ | 200A |

Based on the theoretical analysis of the numerical calculation of the stray inductance in section II, the $t_{0} \sim t_{2}$ integration interval shown in Fig. 14 below is used as the benchmark for numerical calculation. Since there is a small amount of high-frequency noise in the measured current data, it needs to be processed to improve the accuracy. The result after processing is shown in Fig. 15, the diamond point in the figure is the current value measured in the experiment, and the curve is the current curve after fitting. After data processing, the stray inductance value of the PCB loop is 31.5245nH through relevant calculation, which is basically consistent with the 32nH of the three-dimensional simulation result.

V. CONCLUSION

This paper analyzes the method of extracting the stray inductance of the double-pulse test circuit based on the PCB structure, establishes a three-dimensional simulation model of the double-pulse test circuit of the PCB structure under Ansys software, and calculates the stray inductance through the model simulation. Finally, combined with the double-pulse test experiment, the three-dimensional simulation results are compared with the numerical calculation results using the integral method to verify the effectiveness of the three-dimensional modeling and simulation method in this paper. The research in this paper provides a method reference for the relevant engineers and technicians to extract the stray inductance of the double-pulse test circuit.

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