Emerging Plasma Nanotechnology
Atomic Layer Technologies for Nano Materials and Devices

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ABSTRACT
Developments in plasma process technology have led to innovative advances in the miniaturization and integration of semiconductor devices. However, when semiconductor devices are utilized in the nanoscale domain, defects or damage related to charged particles and ultraviolet (UV) rays emitted from the plasma can emerge, resulting in degraded characteristics for nano-devices. It is thus imperative to come up with a method that suppresses or controls the charge accumulation and ultraviolet (UV) damage in plasma processing. This paper reviews our work on a neutral beam process that suppresses the formation of defects at the atomic layer level on the processed surface, which makes it possible for ideal surface chemical reactions to occur at room temperature. This is vital for the creation of innovative nano-devices in the future.

INDEX TERMS
Atomic layer defect-free etching, Atomic layer defect-free deposition, 3D Fin FET, Quantum dot devices, Super low-k film, MRAM.

I. INTRODUCTION
Reactive plasmas are widely utilized in the fabrication of semiconductor devices for fundamental processes such as microfabrication, surface reforming, and film deposition. Meticulous processing precision is now required at the atomic layer level, along with high deposition accuracy to enable structures to be controlled at the molecular level. While ultra-miniature nanoscale devices are expected to be prevalent in the near future, the use of plasma processes can cause significant issues during fabrication, such as abnormal etching or breakdown of insulating films due to the accumulation of ions or electrons emitted from the plasma [1], [2], [3], as shown in Fig. 1. In the high-density low pressure plasma process, a charge accumulation of the mA order occurs on the substrate surface, and dielectric film breakdown occurs. In order to suppress it, it is necessary to reduce the charge accumulation to the order of μA or less by using a pulse-modulated plasma method or a bypass diode, both of which are extremely difficult to optimize [1], [2], [3]. Another issue is the formation of surface defects (e.g., dangling bonds) to depths over a few tens of nanometers stemming from exposure to ultraviolet (UV) emissions [4], [5]. Since nano-scale devices have a larger surface area than comparable bulk materials, plasma processes can significantly affect the electrical, optical, spintronic, and thermodynamic properties due to process-induced defects stemming from ultraviolet UV exposure. The interface state density due to defect generation in a plasma etching was maintained even after restoration annealing at 450 °C for 30 min [6]. This result suggests that simply restoring a defect (such as E’ center) by annealing is not sufficient, and that UV irradiation damage must be completely suppressed during the etching processes.

Another challenge is that next-generation nanodevices will require size control of three-dimensional structures with high precision and selectivity at the atomic layer level.

One promising approach to resolving these issues is the use of neutral beam process technology [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. The neutral beam atomic layer process reduces the incidence of charged particles and UV photon radiation from the plasma onto the substrate so that the substrate is exposed only to the energy-controlled neutral beam. In other words, it is possible to precisely control the kinetic energy of the neutral beam by means of the ion acceleration energy obtained with the applied electric field before neutralization. This subsequently enables ultra-precise nanoscale processing that can suppress the formation of defects at the atomic layer level and control the chemical reactions on the surface atomic layer with
high precision. Furthermore, high precision processing can be achieved by selecting various halogen-based gases (F₂, Cl₂, HBr, HI, etc.) in order to realize the optimum chemistry according to the material [19], [20], [21].

In this paper, we review the neutral beam generation technique [7], [8] developed by S. Samukawa and investigate research on its application to atomic layer etching (ALE) [19], [20], [21] and deposition (ALD) [22], [23].

II. NEUTRAL BEAM GENERATION SOURCE

Fig. 2 shows a conceptual diagram of our developed neutral beam source that evolves from a pulse-modulated plasma with an on/off switching time of 50 microseconds (μs) [13]. This source utilizes inductively coupled plasma (ICP) and features carbon ion acceleration electrodes positioned at the top and bottom of the quartz plasma chamber. Gas flows from the upper electrode in the form of a shower, and ions accelerated from the plasma move through 1-mm-wide, 10-mm long, 1mm hole pitch apertures (open aria: 60%) located in the lower graphite carbon electrode, where they are then neutralized by colliding with the aperture sidewalls. In a plasma modulated by 50-μs pulses, electrons lose energy during “off” periods and undergo dissociative attachment with a halogen gas having a large electron affinity (fluorine, chlorine, bromine, or iodine). Consequently, even in high-density, low-pressure plasma, an afterglow plasma consisting of both positive and negative ions is formed during “off” periods.

When an electric field with a frequency of 1 MHz or less is applied to the pulse-modulated plasma, which consists of positive and negative ions, the ions themselves follow the electric field and can be accelerated to the carbon aperture alternately [25]. The optimal frequency for accelerating both ions from the plasma to the carbon aperture is 600 kHz. This 600-kHz high-frequency electric field is applied only to the entirely pulse-modulated plasma, not to where there is no plasma generated. In cases like this, namely, when a 600-kHz RF electric field with DC bias applied to the plasma is varied and the positive and negative ion beams in the chlorine plasma move through the carbon apertures, nearly 100% of the negative ions are neutralized [9], [13], and approximately 70-80% of the positive ions are neutralized [9]. Analysis with time-dependent Kohn-Sham equations [26] has shown that the negative ions transition into electrons with high probability thanks to resonant transitions between orbitals having energies similar to those of graphite. In contrast, positive ions are neutralized with lower probability due to the low-probability electron transitions stemming from multi-stage Auger transitions between orbitals with disparate energy levels. As a result, a neutral beam formed by neutralizing negative ions using a pulse-modulated plasma has higher density and lower energy than when using positive ions. We measured the flux and energy of neutral particles, ions, and photons using a silicon wafer with a thermocouple and a Faraday cup and calculated the neutralization efficiency. A neutral beam flux of more than 1 mA/cm² in equivalent current density and a neutralization efficiency of more than 99% were obtained. The spatial uniformity of the neutral beam flux was within ±6% on a 100-mm diameter substrate. Thanks to neutralization, when the ion current density in plasma was about several mA/cm², the residual charge could be reduced to several μA/cm² by inserting a carbon aperture. The angular spread of the neutral beam was estimated to be 90 ± 5 ° from the neutral beam energy distribution [27], [28], after which the application of
silicon etching using a Cl2-based neutral beam resulted in no undercut. The etch rate uniformity was less than ±5% within the 200-mm diameter substrate and a perfectly uniform etching within a local area of 1 cm² on the Si substrate was achieved [27], [28]. The etch rate increased by applying bias power to the neutralization aperture plate, which shows that an accelerated neutral beam was successfully obtained. These results indicate that the neutral beam source is scalable, thus making it possible to obtain a large-diameter and uniform neutral beam, which is required for application to mass production [28].

In this paper, we discuss the application of sub-10-nm structure fabrication technology to several devices, [12], [13], [14], [15], [16], [17], [18], [19], [20], [21] a low-k film deposition technique utilizing control of polymerization reactions at the atomic level, [22] and an oxidation reaction for metal oxide (HfO₂) deposition [23].

III. EFFECTS OF UV IRRADIATION ON SURFACE REACTION DURING PLASMA ETCHING

We quantitatively investigated the effect of photon irradiation with a UV lamp during a high-density Cl neutral beam etching (NBE) process for Si [24]. Our objective here was to clarify the photon-wavelength range for enhancing surface reactions during chlorine Cl-plasma Si etching processes. Our results showed that UV light ranging from 220 to 380 nm significantly enhanced the Si surface reactions under the chlorine Cl atom beam. This indicates that irradiation with UV photons can potentially improve the surface chemical reactions during Cl₂ plasma etching (PE) processes. The UV lamp was placed at a 90° angle from the neutral beam source, as shown in Fig. 3. A short-arc Xe flash lamp (pulse discharge) was utilized for irradiating the UV photons on the Si sample surface. Fig. 4 shows the spectra (from 200 nm to the visible region) irradiated from the lamp to the substrate surface. As we can see, there was a higher photon intensity in the UV region from 220 to 400 nm than in the visible region. We measured the power density of the irradiated photons with a calorimeter fixed to 38 mW/cm². The photon irradiation frequency was fixed to 8 Hz (the “on”-time pulse width was 25 ms in full width at half maximum (FWHM)).

In addition, to further investigate the effect of UV and visible photons on the surface reactions, we cut the UV photons below 380 nm using a UV photon filter. Fig. 5 shows the effects of photon irradiation on etching depth as a function of the RF bias power during Cl neutral beam etching process. Irradiated photon wavelength was changed by applying a UV photon filter.
IV. ATOMIC LAYER GERMANIUM ETCHING FOR 3D HETEROGENEOUS INTEGRATION FET

The most commonly used material for IV group semiconductor devices is Si. However, the performance of Si semiconductor devices is limited by the inherent short-channel effects in conventional planar-type metal-oxide-semiconductor (MOS) transistors due to the short gate length [29]. The 3D Fin field-effect transistor (FinFET) has recently emerged as a potential way to overcome the short-channel effect problem for highly scaled MOSFETs [30], [31], [32]. Ge also shows promise for replacing Si as a new channel material thanks to its higher carrier mobility [33], and Ge FinFETs have attracted attention for use in MOSFETs with favorable high-mobility channels. Ge Fin structures with very tiny widths (less than 100 nm) have already been fabricated [34], [35], [36].

The etching reaction of silicon is understood to be an ion-assisted reaction [37], [38]. When a neutral beam is used, no defects are generated, so atomic layer processing can be achieved by controlling the beam energy. Unfortunately, however, the Ge channel formation for FinFETs has not been deeply investigated because the Ge etching reactions are less clear than the Si etching reactions. In addition, carrier mobility degradation occurs in Ge as a result of electron scattering due to surface roughness and defects on the channel sidewall surfaces etched by conventional plasma etching (PE) [39], [40], [41]. In PE, energetic ion bombardment and ultra-violet (UV) light irradiation lead to the surface defects and surface roughness, and a large side-etching on the Ge sidewall has also been known to occur. As a result, it is nearly impossible to control the channel width and taper angle of the Fin structure. Taken together, the sidewall defects, roughness, and under-cutting profile degrade the carrier mobility and I-V characteristics. If we want to achieve higher performance electrical characteristics without compromising the intrinsic high carrier mobility of Ge, sub-10-nm Ge FinFETs of the future will require atomic-layer, defect-free, roughness-free, and profile-controlled etching [18].

The neutral beam etching (NBE) technique we developed is a suitable way to meet these requirements, as it can achieve defect-free and roughness-free etching without irradiating any of the charged particles and/or UV and vacuum ultraviolet (VUV) photons from the plasma. We have already applied NBE to the fabrication of a Ge Fin-FET [34] and found that the device demonstrated an excellent performance [34].

In a prior work, we investigated the etching characteristics of Ge for 3D Ge FinFETs using pure Cl₂ gas through a comparison of the NBE and PE methods [18], [34]. The neutral beam system was composed of an inductively coupled plasma (ICP) source and a carbon aperture plate in which energetic ions are converted into a neutral beam. We found that the high-aspect-ratio (e.g., 10) carbon aperture was able neutralize the negative and positive ions in the plasma without reducing their kinetic energy was maintained by applying a 600-kHz RF bias power. After changing the aspect ratio of the carbon aperture from 0.7 to 10, it was possible to control both the neutralization ratio (from 0% to more than 95%) and the UV irradiation intensity (from 100% to almost nearly 0%) on the sample substrates. Previous research has reported the effects of different aspect ratios on the carbon aperture in more detail [18], [34]. The number of radicals and energetic particles (either accelerated ions or a neutral beam) passing through the aperture onto the surface will be different depending on the aperture open ratio. Both apertures in our evaluation had the same aperture open ratio (50%), and under this condition, the only difference between the two techniques was the UV/VUV photon irradiation on the surface. As for using a low aspect ratio (0.7) for the carbon aperture, the particle irradiation conditions corresponded almost exactly to those of conventional high-density plasma etching (i.e., “plasma mode”).

In this study, we etched Ge Fin structures utilizing SiO₂ hard masks patterned by electron-beam (EB) lithography or a nanoimprint technique and etched by conventional ICP etching processes. Both single-crystal Ge wafers and Ge-on-insulator (GeOI) wafers were utilized, as shown in Fig. 6. We set the sample substrate on a cooled stage and evaluated the etching characteristics by varying the substrate temperature from −20 to 150 °C. To compare the etching characteristics and damage of NBE to those of PE, some of the samples...
were etched using the plasma-mode configuration, where a low-aspect-ratio (0.7) carbon aperture plate having the same open area as the NBE configuration was used. In the plasma-mode operation, we immersed the sample substrates in an after-grow plasma that passes though the low-aspect-ratio apertures where irradiation of the UV light and charged particles (electrons and ions) exists. The gas flow rate was fixed to 40 sccm and the gas pressure in the plasma source and etching chamber was 1 Pa and 0.09 Pa, respectively. The ICP source power was fixed at 400 W. The pulse-time-modulation had a cycle time of 100 µs and a duty ratio of 50%. The bottom electrode bias was operated at 600 kHz and 18 W.

Fig. 7 shows the etching rate dependence of Ge, Si, and SiO\(_2\) using (a) NBE and (b) PE on the substrate at temperatures ranging from –20 to 150 °C. We include the SiO\(_2\) etching rate for reference, as it roughly corresponds to physical bombardment energies (e.g., ion energy and neutral beam energy). We can see from the SiO\(_2\) etching rate that the physical bombardment energies were almost the same under all conditions. Basically, my previous report revealed that the etching yield of Ge with Cl\(^+\) ions was three times higher than that of Si with Cl\(^+\) ions, as the Cl absorption layer on the Ge surface was thicker than that on the Si surface [35]. With both NBE and PE, the Ge etching rate was nearly three times higher than the Si etching rate, regardless of the temperature. These results are in reasonably good agreement with the etching yield. In addition, the etching rate of Ge using PE was dramatically increased compared to using NBE. In both processes, the energetic particles (e.g., accelerated positive ions and neutral beams) have almost the same flux and bombardment energy. In the case of the PE process, however, UV/VUV photons were also irradiated onto the Ge surface, which resulted in higher-density defect generation. We therefore conclude that the surface defect generation actually enhances the surface chemical reaction with chlorine. Further, it seems that the activation energy of the Ge etching reaction for PE (Aa PE = 0.008 eV) was reduced to almost half that of NBE (Aa NBE = 0.016 eV), whereas the activation energy for Si using PE (<0.004 eV) was basically the same as that using NBE (<0.004 eV). Due to the thick chlorinated layer on the Ge surface, the etching reactivity is more sensitive to defect generation compared to that on the Si surface. In other words, we found here that processing with higher precision is possible than with plasma processing.

Fig. 8 shows the side-wall etching rate of a Ge Fin structure using NBE and PE with temperatures ranging from –20 to 150 °C. With NBE, no side-wall etching occurred at –20 and 30 °C, whereas with PE, the side-wall etching rate was 8.7 nm/min at –20 °C. This suggests that the UV/VUV irradiation induces defects on the etching surface and thereby enhances isotropic etching. The activation energy of side-wall etching for NBE was 0.22 eV from 90 to 150 °C, and at less than 90 °C, no side-wall etching occurred. This means that the activation energy of the side-wall etching for NBE at low temperature is infinite. In contrast, the side-wall etching for PE was 0.043 eV even at the lowest substrate temperature of –20 °C. It is apparent from these results that the activation energy of PE for the side-wall etching is dramatically reduced by the UV/VUV irradiation, and that in contrast, NBE is able to achieve vertical etching without any side-wall etching.

Figs. 9 and 10 show SEM images of the Ge Fin structures obtained with NBE and PE, respectively, at each temperature. As we can see in Fig. 9, NBE obtained highly anisotropic Ge Fin structure etching even over the wide temperature range of –20 to 150 °C. In contrast (Fig. 10), PE caused larger side-etching on the Ge sidewall surface, even when the sample...
was cooled to –20 °C. At 150 °C, strong undercutting and a bowing shape appeared under the mask. On the Ge sidewall surface, in the case of PE, higher chemical reactivity and spontaneous reactions occurred due to Cl radicals. These results demonstrate that the Ge etching reaction is more sensitive to the surface defect generation, and that the defect generation on the Ge sidewall caused by UV/VUV photons needs to be eliminated for future nanoscale Ge Fin structures. These distinctive characteristics of Ge etching by a Cl neutral beam indicate that the etching reaction is limited by saturated adsorption coverage of Cl on the Ge surface and desorption of the byproduct GeCl4—in other words, the etching reaction occurs only when the chlorinated surface is bombarded by an energy-controlled neutral beam. The surface chlorination coverage and etching yield of Ge are much larger than those of Si, which means the etching rate of Ge seems much higher as well. Since GeCl4 has a smaller vapor pressure than SiCl4 [17], the chlorination density on the Ge surface is much higher than that on the Si surface. Therefore, the chlorinated Ge surface can be etched off only by the incident collimated Cl neutral beam bombardment with a certain kinetic energy, and as a result, the undercutting of a Ge Fin structure can be mostly eliminated when using the Cl NBE. When the substrate temperature is 150 °C, the neutral beam causes a slight bowing shape, probably because the etching product generated on the sidewall is completely detached, reflecting the angular distribution of the Cl neutral beam. Although it is not necessary to process germanium at the high temperature of 150 °C, if the pressure in the substrate is further reduced, the beam can be further collimated and processing with better verticality can be achieved.

In contrast, as we can see in Fig. 10, PE leads to a large undercutting of the Ge Fin structure beneath the hard mask when the ion bombardment energy is the same as the neutral beam bombardment energy. The undercut profile is almost exactly the same as the defect generation layer caused by irradiating UV/VUV photons from the plasma [18], [34]. We therefore assume that the UV/VUV photons also enhance the desorption of the chlorination layer on the Ge surface. These UV/VUV photons are isotropically irradiated on the etched sidewall surface. As a result, isotropic etching occurred when using the conventional plasma etching, whereas anisotropic etching occurred with NBE. This better directionality does not stem from the irradiated UV/VUV photons on the sample surface. We conclude from these results that vertical and smooth sidewalls can be better obtained by using our NBE technique compared to PE. The vapor pressures of germanium chloride and silicon chloride are comparable, and it is basically unlikely that they will remain on the sidewall when the substrate temperature is above room temperature. Side etching was therefore caused by defect generation effect. UV-induced defects increase sidewall reactivity and increase side etching. The defects are formed to a depth of several tens of nanometers from the surface and can be removed by sacrificial oxidation and wet etching, but the side etching becomes larger and the surface becomes rougher.

Effect of defect generation during the Fin fabrication on the performance of n- and p-type Ge FinFETs [34], was investigated. Fig. 11(a) shows the |Id|–Vg characteristics of n- and p-type Ge FinFETs with a 500-nm gate length (Lg) fabricated by neutral beam etching, as measured by the DC I–V method. As we can see, the n- and p-type Ge FinFETs fabricated by neutral beam etching without UV light irradiation have excellent |Id|–Vg characteristics. However, Ion for n- and p-type Ge FinFETs obtained in the DC I–V measurement is estimated to be less than 10% of that obtained in the pulsed I–V measurement, which is due to charge trapping in the high-k gate stack and self-heating during the I–V measurement. To mitigate these effects, we estimated the ion current (Ion) and the maximum gm (gm, max) using the pulsed I–V method, as shown in Fig. 11(b). We can clearly see here that the |Id|–Vd characteristics of the Ge FinFET fabricated by neutral beam etching are significantly improved compared to those fabricated by ICP etching. The difference between the |Id| improvement ratios of the n-FinFET and p-FinFET fabricated by neutral beam etching stems from the difference in the carrier masses in these FinFETs. Since the electron mass is lighter than the hole mass, the electrons in the n-FinFET are easily affected by etching damage. To determine why these mobility differences took place between NBE and ICP etching, we measured the CV characteristics of the FinFETs to check the interfacial trap density (Dit). The trap densities of the fabricated devices were calculated from the difference in the CV characteristics of the FinFETs with different frequencies. The traps were well suppressed by the diluted-hydrogen annealing, and the calculated maximum trap densities remained below 1011 cm−2 regardless of the fabrication method. Thus, the Coulomb scattering due to the interface trap does not explain the mobility difference. To further investigate, we checked the surface roughness that had caused a significant electron scattering [32], [42]. The NBE process can produce a defect-free and atomically smooth sidewall surface, whereas the conventional ICP etching process causes crystal defects.
and large roughness. The remarkable contrast of the device electric characteristics between the NBE and ICP can thus be explained by the difference in the atomic-level roughness and damages of the etched channels. The roughness might be created through high-energy ion bombardment and ultraviolet photon irradiation, which disconnect the Si–Si network.

For the first time, we have demonstrated heterogeneous complementary FETs (hCFETs) with Ge and Si channels fabricated using our neutral beam technologies, as shown in Fig. 12 [43]. The 3D channel stacking integration utilizes two key technologies to bond Ge channels onto Si wafers: 1) atomically defect-free/roughness-free neutral beam thinning processes and 2) a low-temperature (200 °C) hetero-layer bonding technique (LT-HBT) implemented by a surface activating chemical treatment at room temperature. The neutral beam thinning technique we developed was able to obtain the $R_{tv}$ (mean of maximum peak to valley height) of less than 0.39 nm, the uniformity of Ge thinning depth of less than ±0.75 nm, and the thinning rate of 15.3 nm/min, as shown in Fig. 13. These results demonstrate that our neutral beam technology can obtain atomic-layer-uniform and roughness-free Ge etching for the bonding surface. We also implemented a multi-channel structure consisting of two-channel Si and one-channel Ge to obtain a symmetric performance in n/p FETs. Wafer-scale LT-HBT was successfully demonstrated, thus opening the door to new opportunities for ultimate device footprint scaling with heterogeneous integration.

V. FABRICATION OF ATOMIC-LAYER DEFECT-FREE NANOSTRUCTURES

Moore’s Law is predicted to break down by 2020, at which point we will reach the physical limits of transistor operation. Several countries are therefore working on nanodevices utilizing new principles based on quantum effects. To fabricate quantum-effect devices, it is vital to form defect-free nanostructures (dots and wires) that can be formed with precision down to the atomic-layer level. Two approaches in this vein have been adopted: a top-down approach that utilizes processes such as plasma etching, and a bottom-up approach that utilizes self-organization techniques based on molecular beam epitaxy (MBE) and other processes. The main disadvantage of the top-down approach utilizing plasma etching is that the plasma emits ultraviolet UV rays and causes electrical charges to accumulate at the substrate surface. This reduces the selectivity of the mask and the underlying substrate material and leaves a high density of defects deep within the processed surface, thus limiting processing to dimensions of several tens of nanometers. In contrast, the bottom-up processing has fewer problems related to defects and the like thanks to utilizing a growth process that involves lattice strains. Unfortunately, it has problems such as non-uniformity and stress deformation of the arrangement and structure of the nano-dots, which means that quantum effects can only be achieved with a limited range of materials and structures. To utilize these structures in nanodevices, we need to be able to fabricate nanostructures without relying on more accurate materials.

In response to the above, we are currently researching how to form quantum nano-dots less than 10 nm in size by means of a top-down process utilizing a low-energy neutral beam capable of defect-free processing. A key advantage of the top-down process is that it can form nanostructures with an arrangement that can be uniformly controlled no matter what combination of materials is used. As an alternative to photolithography, we used a bio-template [44] as an etching mask with dots of a few nanometers in size. As shown in Fig. 14, the biological super-molecule ferritin (protein) has a 12-nm
diameter and 7-nm internal cavity. There is a negative charge inside the cavity, and when ferritin is placed in a solution containing dissolved Fe ions, Fe positive ions are introduced into the cavity of the ferritin molecules to form iron oxide cores sized 7 nm in diameter. We selectively placed ferritin molecules containing these iron cores into a two-dimensional arrangement on a silicon oxide film and then removed the protein by UV/ozone or heat processing, leaving behind 7-nm iron cores to serve as an etching mask [44].

A Cl₂-based neutral beam can etch any kind of surface material by using an etching mask consisting of 7-nm iron cores. We are currently utilizing this process to develop quantum-effect devices with a quantum nanodisc structure, which is a nano-scale cylindrical structure whose height (thickness) is smaller than its diameter. Fig. 15 shows nanodisc structures we fabricated with Si, Ge, GaAs, and graphene, all of which have a diameter of about 10 nm [45], [46], [47], [48]. As we can see, the sub-10 nm quantum nanodiscs are formed in an array configuration with uniform spacing.

Fig. 16(a) shows the photoluminescence from GaAs/AlGaAs quantum dots and the precise control of band gap energy in these nanodisc structures with different materials when varying the thickness of the dots but keeping the diameter fixed to 10 nm. Fig. 16(b) shows the photoluminescence from GaAs/AlGaAs quantum-dots. As we can see, the band gap can be controlled over a wide range with high precision by varying the nanodisc size and material [37]. No other quantum dot fabrication techniques can offer this kind of flexibility and precise band gap control. Moreover, this is the first time photoluminescence has been observed from GaAs quantum dots fabricated by a top-down process. Time-resolved measurements have demonstrated that this light originates from the quantum dots themselves and not from defects [24], [36]. We conclude that the advantages of the top-down process can be achieved for any material, with defects fully suppressed at the surface interface of sub-10 nm quantum dots formed by a neutral beam process. We are currently developing a high-efficiency quantum dot solar cell and a quantum dot laser with a flexible band structure [46], [47].

Micro-light emitting diode (micro-LED) displays are attracting a considerable amount of research interest and are expected to have low power consumption, high brightness, and high resolution suitable for use in next-generation wearable information devices. One of the biggest technical challenges when it comes to fabricating high-performance micro-LED displays is the strong decrease in internal quantum efficiency (IQE) with the decrease in chip size to below a few tens of μm, especially at the current density region lower than 20 A/cm [49]. In the fabrication of conventional GaN-based micro-LEDs, the typical approach is to use ICP etching to define the LED mesa, during which high-density crystalline defects acting as nonradiative recombination centers are inevitably generated on the sidewall surface of the LED mesa over a depth of a few tens of nm due to ion bombardment and high-energy and high-density (50 mW/cm²) UV photon irradiation from the plasma.

After the fabrication of the LED mesa and removal of the remaining SiO₂ hard mask, the sample was returned to the MOCVD reactor for GaN regrowth. To investigate the growth dynamics and surface microstructure of the LED mesa during the early stage of the regrowth process, the GaN layer was intentionally undoped with its thickness controlled at approximately 100 nm (nominal thickness for growth on a planar substrate). The LED mesa sample was cleaned using a standard RCA process before loading into the MOCVD reactor. The substrate was heated from room temperature (RT) to 800 °C within 5 min in an ambient atmosphere of N₂ and NH₃. A 10-nm undoped GaN layer was then grown to protect the LED mesa. After that, the temperature was increased to 950 °C and the 100-nm undoped GaN was grown. However, even
Fabricated micro-LED. The LED layer structure is composed of a 5-period InGaN (2 nm)/GaN (12 nm) multiple-quantum-well active layer and a 150-nm-thick Mg-doped p-GaN layer. The AlGaN electron blocking layer is omitted for simplicity.

If this regrowth is performed to terminate surface defects, the defects formed at a depth of several tens of nm cannot be recovered and these plasma-induced defects significantly reduce the IQE of micro-LEDs due to their very large sidewall surface area to volume ratio compared to conventional large-area LEDs, especially at low current densities. For example, at the current density of 1 A/cm², the external quantum efficiency (EQE) of a 10-μm GaN/InGaN micro-LED is typically more than ten times lower than that of a large-area (>100 μm) LED.

If we want to develop high-performance displays, the light intensity should be varied over a dynamic range as wide as 100000:1, which means a minimum luminance as low as 0.01 cd/cm² is required for a display with a maximum luminance of 1000 cd/cm². This makes a high IQE at the low current density region a prerequisite for fabricating high-performance micro-LED displays. One promising approach in this vein is the utilization of a damage-free mesa etching technique, which can significantly reduce the nonradiative defects on the sidewall surface of a GaN micro-LED compared to the conventional ICP technique. This technique has been used to fabricate In₀.₃Ga₀.₇N/GaN nanodiscs with a diameter as small as 10 nm, and an increase in the IQE values of the nanodisc with respect to an unetched reference sample by a factor of 100 times has been reported in photoluminescence studies. Our motivation in the present work is to develop GaN micro-LEDs with efficiencies independent of chip size by utilizing our NBE technique to fabricate the mesa structure of GaN micro-LEDs.

We used our NBE technique to fabricate a series of square GaN/InGaN micro-LEDs with mesa sizes ranging from 40 to 6 μm using a blue-emitting (440 nm) GaN LED wafer grown on a c-plane sapphire substrate by metal organic vapor phase epitaxy. We also fabricated a similar series of samples using the conventional ICP process as a reference. Fig. 17 shows a schematic of one of the fabricated micro-LEDs. The LED layer structure is composed of a 5-period InGaN (2 nm)/GaN (12 nm) multiple-quantum-well active layer and a 150-nm-thick Mg-doped p-GaN layer (the AlGaN electron blocking layer is omitted for simplicity). We used Cl₂ as the etching gas for the NBE etching here. The ICP power was 400 W and the RF power was 5 W. More detailed information about NBE etching can be found in previous studies. We implemented ICP etching using a commercial ICP system. After forming the micro-LED mesa, a 200-nm-thick SiO₂ layer was deposited on the sample surface by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C to serve as a passivation and electrical isolation layer. Tetraethoxysilane was used as the Si precursor in PECVD. Next, square Ni (2 nm)/Au (5 nm) semitransparent p-type electrodes were formed on the mesa’s top surface in a window opened into the SiO₂ layer by vacuum evaporation and liftoff. The p-electrode was designed to be 1 μm smaller than the micro-LED mesa. The sample was then annealed in N₂ at 500 °C for 2 minutes to form ohmic contact. Next, Cr/Au p- and n-type bonding pads were formed on the surface of the SiO₂ electrical isolation and n-GaN layers, respectively, and a 2-μm-wide Au stripe was prepared to connect the Ni/Au p-electrode and Cr/Au p-type bonding pad. The wafer was lapped to about 150 μm and cut into 11-mm [2] chips. The fabricated LED chips were then bonded to TO-18 packages with Ag paste without resin encapsulation and light was extracted from the p-GaN side through a Ni/Au semitransparent electrode. We measured the light output power using a calibrated Si photodiode placed 2 mm away from the LED chip with a receiving full angle of about 130 °, which could collect about 80% of the total emission assuming a Lambertian emission pattern.

The current density-dependent EQE characteristics of micro-LEDs with different sizes fabricated using the ICP and NBE techniques are shown in Fig. 18. As expected, the EQE of the ICP-etched micro-LEDs decreased significantly when the chip size was reduced from 40 to 6 μm. At the current density of 5 A/cm², the EQE decreased from 3.44% for the 40-μm micro-LED to about 0.66% for the 6-μm micro-LED. In particular, the EQE of the 6-μm micro-LED increased monotonically with increasing current density and never reached the maximum current density of 80 A/cm², indicating that the nonradiative recombination is dominant even at a current density as high as 80 A/cm². These are similar characteristics to those observed in GaN/InGaN micro-LEDs fabricated using the ICP technique. In contrast, all the NBE-etched micro-LEDs showed current density vs. EQE characteristics similar to those of large-area GaN/InGaN...
LEDs. The EQE of all four micro-LEDs increased rapidly when the current density was increased, reaching a maximum value at the current density of about 5 A/cm², and then decreased with a further increase to the current density due to the well-known efficiency droop effect in GaN LEDs grown on c-plane sapphire substrates. More importantly, the maximum EQE values at the current density of about 5 A/cm² for all four micro-LEDs varied by less than 10%. These micro-LEDs also showed very similar EQE values at an even lower current density of 1 A/cm²—about 2.58, 2.63, 2.74, and 2.74% for the 40-, 20-, 10-, and 6-µm micro-LEDs, respectively. The 40-µm micro-LED exhibited slightly lower (by about 10%) EQE values compared to the other micro-LEDs, especially at the higher current density region. This is presumably due to the fact that a smaller micro-LED can sustain a higher current density thanks to its better thermal dissipation, which means it suffers from a weaker efficiency droop effect. Nevertheless, the results clearly demonstrate that our NBE technique can almost completely eliminate the size-dependent-efficiency decrease typically observed in ICP-etched GaN micro-LEDs, at least down to the chip size of 6 µm. The size-independent feature of the EQE values of the NB-etched micro-LEDs indicate that non-radiative defects induced during the NBE process can essentially be ignored, which is a conclusion supported by the observation of enhanced IQE values in In₀.₃Ga₀.₇N/GaN nanodiscs fabricated by the NBE process.

VI. ATOMIC-LAYER DEPOSITION FOR LOW-K AND METAL OXIDE THIN FILM

Our neutral beam process will be crucial for future atomic-layer processes such as atomic layer deposition (ALD) in order to continue improving atomic-layer-based pure surface reactions. This is because the UV photon irradiation from plasma obstructs the atomic layer by preventing pure surface chemical reactions and promoting multi-layer chemical reactions due to surface defect generation. This makes it basically impossible for conventional plasma processes to control atomic layer chemical reactions. In this section, we present pure atomic layer processes that can be implemented using our neutral beam technique. Specifically, to determine the real atomic layer reactions induced by this technique, we examine a polymerization reaction for low-k material depositions, and introduce oxidation reactions for high-k metal oxide (HfO₂) deposition to determine the real atomic layer reaction when used in conjunction with our neutral beam process.

A. CONTROLLING MOLECULAR STRUCTURES IN LOW-K MATERIALS [22]

When semiconductor integrated circuits are scaled down to produce devices with higher processing speeds, the parasitic capacitance of the interlayer dielectrics between metal electrodes becomes increasingly problematic. This capacitance has caused the signals inside semiconductor devices to be delayed due to the effects of the interconnections (i.e., RC delay). One way to reduce the parasitic capacitance between interconnections is to reduce the dielectric constant of the inter-layer insulation film and/or reduce the resistance of the interconnection metal. Specifically, we can use SiOCH (a silicon oxide film with added carbon) as an inter-layer insulation film and add pores to the film to reduce its dielectric constant. Unfortunately, introducing pores can impair the mechanical strength of the film, and peeling of the film during the interconnection process can occur as a result. There are also various other problems that can arise, such an increase in the dielectric constant due to plasma damage after the interconnection stage or deterioration of the insulating properties stemming from the diffusion of metal during the heating process. Since adding pores to the film is unfeasible, we need to find some other way of reducing the dielectric constant in the film. We aim to achieve this by using a neutral beam to control the molecular structure with high precision [22].

Fig. 19 shows our theoretical calculations of the dipole moments of two small-scale SiOCH molecules: (a) one with a highly symmetrical structure and (b) one with low symmetry. The sum of the molecular dipole moments is reflected in the material’s polarizability, which means we can gain insight into the optimal molecular structure of SiOCH by determining the dipole moments of small-scale molecules. In these calculations, we estimated the dipole moments by using the B3LYP density functional (based on first principles) and the 6-31G(d) set for molecular orbitals to optimize the molecular structure and analyze the vibration frequencies. Using the results of these calculations as a basis, we were able to reduce the dipole moment by a factor of approximately 7 compared to a structure having high symmetry. We also calculated the theoretical dielectric constant of SiOCH molecules with high symmetry and found that a low value of about 2 can be achieved even with a large molecular structure. We therefore expect that the dielectric constant can be reduced with a non-porous structure if we first increase the symmetry of the molecular structure inside the SiOCH film [22].

To control the molecular structure in a thin film, we need to polymerize the film while directly reflecting the molecular structure of the material gas inside it. In this study, we used an Ar neutral beam to form a non-porous SiOCH film [24].
TABLE 1. The Properties of Porous SiCO and Non-porous SiCO Film

| Metric         | Porous SiCO by PECVD | Non-porous SiCO by NBECVD |
|----------------|-----------------------|---------------------------|
| k-value        | Hg-probe              | 2.6                       | 2.2                       |
| Modulus (GPa)  | Nano-indentener       | 6.0                       | 11.7                      |
| Density (g/cm³) | XRR                   | 1.27                      | 1.54                      |
| Pore size (nm) | SAXS                  | No detected               |

It is generally quite challenging to maintain the molecular structure of the material gas in a plasma, as it undergoes excessive decomposition in the gaseous phase and at the substrate surface due to exposure to UV light and charged particles. This makes it difficult to control the chemical reactions at the substrate surface and impossible to control the molecular structure of the deposited film. In contrast, if we utilize a neutral beam, the material gas can be excited and polymerized with the kinetic energy of an Ar neutral beam while maintaining the molecular structure of the material gas introduced into the lower deposition chamber. Ar neutral beams are generated through a carbon plate with multiple apertures, so a large and easily tunable neutral beam can be generated to completely cut off UV light and electrons from the plasma at the carbon aperture plate.

To investigate the above, we irradiated an Ar neutral beam onto a Si wafer surface while directly injecting a precursor into the surface in a CVD process chamber. We utilized a dimethoxy-tetramethyl-disiloxane (DMOTMDS) precursor, which has four Si–CH₃ and two SiO–CH₃ bonds. Each O–CH₃ and Si–CH₃ bond has 8 eV and 14 eV of bonding energy, respectively. An Ar neutral beam was tuned to 10 eV for polymerizing DMOTMDS to cut only the O–CH₃ bonds and make Si–O–Si chains to retain the Si–CH₃ bonds in the film [24]. We also fabricated a SiOCH sample by the conventional plasma-enhanced chemical vapor deposition (PECVD) method (PECVD SiOCH) for comparison with the SiOCH deposited by neutral beam etching CVD (NBECVD SiOCH). The properties of these two films are compared in Table 1.

We used mercury probes to evaluate the electrical characteristics, small-angle X-ray scattering to evaluate the porosity, a nano-indenteter to evaluate the mechanical strength, and X-ray reflectivity (XRR) to evaluate the film density. Note that although no porosity was detected in the NBECVD SiOCH, its dielectric constant was lower than that of PECVD SiOCH. Moreover, thanks to the lack of pores, it had greater mechanical strength and film density [22].

We used X-ray photoelectron spectroscopy (XPS) to evaluate the film structure in greater detail. When it is composed of a polymethylsiloxane (PMS) structure, the C:Si and O:Si ratios in the film are 2:1 and 1:1, respectively. Our XPS measurements showed that the NBECVD SiOCH had a C:Si ratio of 2 and an O:Si ratio of 1.5. In contrast, the PECVD SiOCH had a C:Si ratio of 0.6 and an O:Si ratio of 1.6. These findings indicate that PMS grew in the NBECVD SiOCH film. The oxygen ratio, however, suggests the formation of an oxygen-rich network of Si atoms stemming from these chained molecules, in addition to the PMS structure.

Next, we analyzed the molecular structure of the NBECVD SiOCH in more detail by examining the C1s spectrum (Fig. 20(a)) and Si2p spectrum (Fig. 20(b)) to clarify the bonding states of carbon and silicon. In the C1s spectrum, we measured peaks at 282.3 eV for Si-C bonds and at 284.5 eV for C-C bonds. The C-C bonds demonstrate cross-linking between the methyl groups bonded to the silicon Si atoms. In the Si2p spectrum, multiple peaks appeared at 101.5, 102.5, and 103.5 eV, which we attribute to the SiO₂-C₂, SiO₂-C, and Si-O₄ bonds, respectively. The largest Si2p peak was observed at 102.5 eV, indicating the growth of PMS inside the film. These findings demonstrate that the NBECVD SiOCH film structure mainly consisted of a PMS chain growth with Si-O and C-C bonds forming a network structure between the chain molecules. This process resulted in SiOCH that was non-porous yet had a low dielectric constant and high mechanical strength. We can conclude that our neutral beam process is an excellent technique for the deposition of thin films because, unlike conventional methods, it enables ideal bonding reactions with a controllable molecular structure to take place in a vacuum and at low temperatures.

B. ATOMIC LAYER DEPOSITION OF HFO₂/SIO₂ GATE STACKED DIELECTRIC FILM [23]

The transistor technical node has recently been scaled down to 5 nm, and the production of 3-nm transistors was started in 2021. Today’s integrated circuits (ICs) are typically composed of metal-oxide-semiconductor field-effect transistors (MOSFETs), and the physical thickness of the conventional gate dielectric material (silicon dioxide (SiO₂)) has become thinner. Ever since the transistor was reduced to a 45-nm process in 2007, Intel has been replacing the conventional SiO₂ material with a stacked high-k gate dielectric and gate insulating film by increasing the gate leakage current due to the short channel effect. When SiO₂ film approached its physical limit thickness at 0.7 nm, it became difficult to achieve the proportional scaling of devices.

Hafnium dioxide (HfO₂) film, which features a high-k material with a high dielectric constant, has a conduction band shift to Si that is greater than 1 eV, which means it can suppress the generation of tunneling currents when the gate...
dielectric layer is thinned. It also has good thermodynamic stability and good lattice matching properties when in contact with Si, making it the most promising new material to replace the traditional complementary-MOS (CMOS) gate insulating layer material (i.e., SiO$_2$). The CMOS gate layer is typically formed using film-deposition techniques such as chemical vapor deposition (CVD), physical vapor deposition (PVD), or atomic layer deposition (ALD). The dimensions of IC devices are constantly decreasing, which has resulted in a variety of complex trench functional structures with large aspect ratios. The surface of the substrate often contains relatively deep holes and trenches, which makes it extremely difficult to deposit high-quality films on them. CVD and PVD techniques face challenges in forming conformal, uniform, and high-quality thin films for high aspect-ratio (>10) nano-structures. ALD has emerged as a promising approach to resolve these problems and has gained widespread attention because it can achieve atomic layer control and conformal deposition using sequential, self-limiting surface reactions. This means it not only ensures the uniformity and step coverage of the film but also precisely controls its thickness on a nanometer scale.

To adapt the 3D integration development in the microelectronics industry to thermal budget reduction, we need a low-temperature thin-film growth technique that can form high-quality and conformal film for any semiconductor devices that include Si or Ge and silicon-germanium. Semiconductor fabrication on the sub-10-nm scale must be able to remove and control any fabrication damage such as dangling bond/defect formation and reduction in the breakdown voltage due to charge-build-up by the plasma process. These problems have been mitigated by our neutral beam (NB) technique that reduces the radiation damage caused by charge build-up and ultra-violet photons during the plasma process. We have also developed an ALD that utilizes a neutral beam (NB) to replace plasma in the irradiation step of the plasma enhanced (PE) ALD, which we call NB-enhanced ALD (NBEALD). Our previous research has shown that the NB process is both defect-free and charge-free, and NB particles with high motion energy and low activation energy ensure that the deposition process is completed at room temperature (20–30 °C). In this study, we utilized NBEALD to fabricate high-quality HfO$_2$ film at 30 °C [23].

We formed an HfO$_2$/SiO$_2$/Si stacked structure and investigated the resultant HfO$_2$/SiO$_2$ stacked gate oxide films. NBEALD was able to continuously form the interface SiO$_2$ film and high-k HfO$_2$ film. A SiO$_2$ film about 1 nm thick was fabricated on a cleaned Si (100) substrate by using O$_2$ NB irradiation (NB oxidation: NBO) at 20–30 °C for SiO$_2$/Si that had better interface properties compared to the direct-contact HfO$_2$/Si. To synthesize a 1.2-nm-thick SiO$_2$ layer, O$_2$ gas (30 sccm) was added to the NB source reactor, and after 100 seconds, NB was irradiated to the surface of the cleaned silicon substrate with a source power of 1300 W. O$_2$ NB was occupied by an O$_2$ neutral particle neutralized from O$_2^+$. For the O$_2$ NB kinetic energy, the energy was less than 25 eV because we set the source power to 1300 W and the bias power to 0 W. HfO$_2$ film was formed on the interface SiO$_2$ layer by using NBEALD at 20–30 °C. Tetrakis (ethylmethylamino) hafnium (TEMAH) was utilized as an Hf precursor gas and O$_2$ NB was used as an oxidant. Argon gas was used as both the carrier gas and purge gas. We stored the TEMAH precursor in a stainless-steel container and heated it to 70 °C. The gas flow of the precursor was 10 sccm. We opted to use argon carrier gas so as to improve the precursor delivery from the bubbler to the reaction chamber, which had a flow rate of 30 sccm. The precursor gas line was maintained at 100 °C, and the chamber wall was maintained at 120 °C to prevent precursor condensation and clogging during transport [23]. The stage temperature was controlled at 30 °C. An Ar purge step with 30 sccm of Ar flow was applied after the precursor feed and NB irradiation steps. For the oxidation step, 30 sccm of O$_2$ gas was added to a large-radius NB source reactor consisting of an ALD reaction chamber and inductively coupled plasma source. The source power was 1000 W, and no bias power was applied to the aperture.

The NBEALD cycle consists of five steps: TEMAH feed, TEMAH purge, O$_2$ gas injection, O$_2$ NB irradiation, and O$_2$ NB purge. The possible reaction mechanism is depicted in Fig. 21. The NBEALD process basically has two half-reactions: in the first, Bis(diethylamino)sihane (BDEAS) reacts with the oxidized surface of the SiO$_2$ interface and eliminates two alkylamine ligands, and in the second, the O$_2$ NB particles with high motion energy react with chemisorbed TEMAH to remove the other two alkylamine ligands and generate an oxidized surface. The by-product of this reaction is Ethylmethylamine (HNC$_2$H$_4$CH$_3$) [23].

We utilized a spectroscopic ellipsometer to measure the film thickness and performed X-ray photoelectron spectroscopy (XPS) to determine the chemical composition and stoichiometry of the HfO$_2$ film. The X-ray source was Al K$_\alpha$ (1486.6 eV). Surface roughness was measured using an atomic force microscope (AFM, SPM-9700, Shimadzu Corporation) with tapping mode. The crystal condition of the film was investigated by X-ray diffraction (XRD) with a Cu K$_\alpha$ X-ray. Fig. 22 shows the growth per cycle (GPC) of (a) precursor feed time, (b) precursor purge time, (c) O$_2$ NB irradiation.
time, and (d) O\textsubscript{2} gas purge time dependency at 30 °C. As we can see, the GPC curve became saturated at 0.16 nm/cycle due to sufficient feed, irradiation, and purge time. For the precursor purge time (Fig. 22(a)), GPC increased and saturated at 5 seconds. There was no change to the film thicknesses during precursor purge time (Fig. 22(b)) or the O\textsubscript{2} gas purge time dependency (Fig. 22(d)). As for the NB irradiation time dependency (Fig. 22(c)), the GPC decreased and converged at 20 seconds over time. Fig. 23 shows the thickness of HfO\textsubscript{2} films at 30 °C as a function of the number of deposition cycles under the reference recipe. As we can see, the thickness increased as the number of cycles increased, and GPC was 0.18 nm/cycle, which indicates a good agreement with the monoclinic Hf-O bond length (0.19–0.23 nm).

We utilized XPS to measure the chemical composition of the HfO\textsubscript{2} film. Fig. 24 shows the O1s and Hf4f of HfO\textsubscript{2} thin film before and after sputtering. The film was grown on a 1.2-nm-thick SiO\textsubscript{2} interface layer synthesized by NBO at 20–30 °C using our NBEALD. The sample was grown in 60 cycles. The O1s (Fig. 24(a)) was divided into two peaks, with the larger peak associated with hafnium dioxide (Hf-O-Hf) at 530.1 eV and the smaller peak with C=O at 532.0 eV. The C = O peak suggests that the C contamination could possibly be bonded with O, which would affect the electric properties of the film; this is undesirable because a thin nanoscale film is very sensitive to contamination. The Hf4f (Fig. 24(b)) was divided into two peaks, with the binding energies of 17.1 and 18.8 eV, respectively. These two peaks are associated with HfO\textsubscript{2}. The spin-orbit splitting value was 1.7 eV. Fig. 24(c) and (d) show the O1s and Hf4f spectra of the HfO\textsubscript{2} film after sputtering. There are two sputtering mechanisms, one for the bond breaking and one for the reformation:

\[
\text{HfO}_2 \rightarrow \text{HfO}_2(s) + \frac{1}{2}\text{O}_2(g) \tag{1}
\]

\[
\text{HfO}_2(s) \rightarrow \text{Hf}_0(s) + \frac{1}{2}\text{O}_2(g) \tag{2}
\]

There are three types of Hf bonds, namely, Hf\textsuperscript{0+} from the Hf metal, Hf\textsuperscript{2+} from HfO\textsubscript{2}, and Hf\textsuperscript{4+} from HfO\textsubscript{2} [30]. This reaction mechanism demonstrates that Hf metal is produced in the sputtering process, so we analyzed the Hf metal peak in the Hf4f spectra of XPS after sputtering. The O1s was divided into two peaks, Hf4f/2 and Hf4f/2\textsuperscript{2}, with the binding energies of 17.1 and 18.8 eV, respectively. These two peaks are associated with HfO\textsubscript{2}. The spin-orbit splitting value was 1.7 eV. Fig. 24(c) and (d) show the O1s and Hf4f spectra of the HfO\textsubscript{2} film after sputtering. There are two sputtering mechanisms, one for the bond breaking and one for the reformation:
of 17.26 eV, Hf4f5/2 peak (HfO2) at 18.93 eV, Hf4f7/2 metal peak at 15.33 eV, and Hf4f5/2 peak at 16.94 eV.

Fig. 25 shows the refractive index n measured by spectroscopic ellipsometry for each cycle of HfO2 film at 550-nm wavelength (λ). As we can see, the n increased as the number of cycles increased. For the 50-nm cycle, n was lower than the thicker sample due to its higher C impurity ratio to the volume. The n was 1.90 for the 200-cycle HfO2 film, which is close to the reference value of amorphous HfO2 film [27], [28], [29]. Since it is a gate dielectric film, amorphous HfO2 was able to achieve high insulation and a low leakage current. These findings demonstrate that the HfO2 film grown using our NBEALD at 20–30 °C was smooth thanks to the amorphous-HfO2 film.

We also demonstrated that our NBEALD can be used to fabricate high-quality HfO2/SiO2 gate stacked film at room temperature (20–30 °C). We fabricated HfO2 film using a combination of TEMAH as an Hf precursor and O2 NB as an oxidant. By bombarding with O2 NB, the surface oxidation process could proceed effectively and high-quality HfO2 was formed even at room temperature. Additionally, continuously grown high-quality HfO2 and silicon dioxide (SiO2) gate oxide films (stacked HfO2/SiO2 gate oxide film) could be successfully synthesized using NBEALD. The refractive index of this film was 1.9, demonstrating that it had an amorphous HfO2 structure with high insulation (more than 5 MV/cm) and a low leakage current (less than 10−7 A/cm²). Such film decreases the thermal budget and thereby enables high flexibility in designing the semiconductor structure.

VII. CONCLUSION

In this paper, we have reviewed our research into cutting-edge nano-devices using neutral beams. For advanced nano-devices of the future, it is vital to utilize ideal surface chemical reactions that do not cause surface defects and can be controlled at the atomic layer level. The neutral beam process is an intelligent nano-process that completely suppresses the ultraviolet rays and electrical charges emitted from a plasma, and thus it is able to achieve ideal surface atomic layer reactions and ideal surface atomic layer structure in good agreement with the computational analysis. This is exactly emerging plasma nanotechnology. We are currently investigating ways of applying this technique to various kinds of application, such as advanced CMOS, nano-photonic devices, nano-energy devices, formations of ultra-thin films and the reformation of inorganic surfaces. Ultimately, we hope that our technique will pave the way to the development and implementation of innovative new devices in the future.

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