High efficiency isolated power supply used for hybrid DC circuit breaker in high voltage direct current systems

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Abstract Hybrid DC circuit breaker is one of the most equipment in high voltage direct current (HVDC) systems. It includes numbers of power electronic (PE) devices and high efficiency isolated power supply is required to control these PE devices. The phase-shifted full-bridge (PSFB) converter is a popular topology for isolated power supply. However, the traditional PSFB converter has some well-known drawbacks. To solve these drawbacks, a novel ZVS FB converter is proposed in this paper. In the primary side of proposed converter, four FB switches, two main transformers and one shared capacitor constitute two half-bridge inverters. At the rectified stage, two FB rectifiers are connected in series by sharing diodes. This structure allows the proposed converter to achieve wide zero-voltage switching range and reduced filter requirement, which make the proposed converter well suited for the power supply for hybrid DC circuit breaker. The performances of proposed converter are verified with an experimental prototype.

Keywords: isolated power supply, circuit breaker, HVDC, phase-shifted full-bridge

Classification: Power devices and circuits

1. Introduction

High voltage direct current (HVDC) systems have been developed increasingly due to the urgent need for renewable energy sources and the development of power electronics technology. In HVDC systems, the hybrid DC circuit breaker (CB) is widely employed to handle the fault current and to improve the reliability \([1, 2]\). Fig. 1 shows the traditional scheme of hybrid CB. A hybrid CB comprises of a mechanical switch (MS), numbers of power electronic (PE) devices and a metal oxide varistor (MOV). It should be noted that all components require power supply to realize their functions \([3, 4]\). Moreover, galvanic isolation is required to ensure safety. The phase-shifted full-bridge (PSFB) converter is one of the most popular isolated power supplies for high power applications since all primary switches can achieve zero-voltage switching (ZVS) without the help of any auxiliary circuits \([5, 6, 7, 8]\). However, the traditional PSFB converter has some serious drawbacks \([9, 10, 11, 12]\). First, the ZVS range of lagging-leg switches is very narrow and the efficiency severely degraded at light loads. In addition, the primary current just circulates in the primary side without transferring any energy during the freewheeling interval, which results in high conduction loss and output filter requirement.

In order to extend the ZVS range and reduce the circulating current, many researches have been studied. The ZVS range can be easily extended by increasing the leakage inductance of main transformer. However, this method increases duty-cycle loss and secondary voltage stress, and the ZVS operation cannot still be obtained at very light loads. In \([13, 14, 15, 16]\), some improved PSFB converters with auxiliary inductors are proposed. In these converters, the auxiliary inductors act as the assistant current sources during the ZVS transition, thus the ZVS operation is independent of output current. However, excessive ZVS energy will degrade the conversion efficiency at heavy loads and the problem of circulating current still exists.

The technology of zero-voltage and zero-current switching (ZVZCS) is an effective solution to reduce circulating current \([17, 18, 19, 20, 21, 22]\). In these converters, primary current is reset by the additional auxiliary circuits and it is maintained at zero during freewheeling interval. The output power is mainly maintained constant by the energy stored in the output filter, thus large filter requirement is needed in ZVZCS converters.

Recently, some half-bridge (HB) integrated FB converters have been proposed for various applications \([23, 24, 25, 26, 27, 28, 29, 30]\). These integrated converters are very attractive due to their outstanding performance. In the primary side, a HB converter is integrated into full-bridge converter by sharing the lagging-leg switches. The HB converter can continuously deliver the primary power to secondary side and the ZVS range is extended by increasing the magnetizing current of HB transformer. However, in these converters,
two independent rectifiers are employed and the structures are very complex.

In this paper, a novel FB converter is presented, which can improve the performance of traditional PSFB converter. Fig. 2 shows the circuit configuration of the proposed converter. In the primary side, four FB switches, two main transformers and one shared capacitor constitute two half-bridge inverters. At the rectified stage, two FB rectifiers are connected in series by sharing diodes D1 and D4. Compared with the existing converters, the proposed converter overcomes the drawbacks of narrow ZVS range and large circulating current at the same time. Low filter requirement and high efficiency can be achieved. These features make the proposed converter well suited for the power supply for hybrid DC circuit breaker.

2. Operational principle

For simple illustration, the following several assumptions are made:

1. The output filter inductor \( L_{O} \) and blocking capacitor \( C_{B} \) are larger enough to be considered as constant current source and voltage source, respectively;
2. \( Q_{1} \sim Q_{4} \) are considered ideal switches with junction capacitors and body diodes;
3. For \( T_{1} \), the leakage inductance is \( L_{k1} \) and the magnetizing inductance is large enough to ignore the effect. For \( T_{2} \), the leakage inductance and magnetizing inductance are \( L_{k2} \) and \( L_{m} \), respectively. \( T_{1} \) and \( T_{2} \) have the same turns ratio of \( n \equiv n_{s1}/n_{p} \).

Fig. 3 and Fig. 4 shows the simplified equivalent circuit and key operating waveforms of proposed converter, respectively. In Fig. 4, \( T_{s} \) is switching period of primary switch, \( D \) is duty-cycle of rectified voltage. The converter is controlled by adjusting the phase time \( 0.5DT_{s} \) between lagging-leg \( Q_{2}-Q_{4} \) and leading-leg \( Q_{1}-Q_{3} \). There are 16 modes in one switching period, which can be divided into two half cycles, \( t_{0} \sim t_{8} \) and \( t_{8} \sim t_{16} \). Only the first half cycle is introduced due to the symmetry of the circuit. This half cycle is divided into eight modes and the corresponding operation circuits are shown in Fig. 5.

**Mode 1** \( [t_{0} \sim t_{1}] \): \( Q_{1}-Q_{4} \) are on-state. The output filter inductor \( L_{O} \) is reflected to primary side, thus the primary current is approximately constant. The primary voltages of \( T_{1} \) and \( T_{2} \) are \( 0.5V_{in} \) and the magnetizing current \( i_{m}(t) \) increases linearly from its initial value. Some key voltages and currents are calculated as follows:

\[
\begin{align*}
    v_{p1}(t) &= v_{p2}(t) = 0.5V_{in}  \\
    v_{rec}(t) &= nV_{in}  \\
    i_{m}(t) &= -I_{m} + \frac{0.5V_{in}}{L_{m}}(t - t_{0})
\end{align*}
\]

where \( I_{m} \) is the peak value of magnetizing current of \( T_{2} \).

**Mode 2** \( [t_{1} \sim t_{2}] \): The leading-leg switch \( Q_{1} \) is turned off at \( t_{1} \). All currents remain constant because the duration of this mode is very narrow. The junction capacitances of \( Q_{1} \) and \( Q_{3} \) are discharged linearly by \( i_{p1}(t) \), which is maintained at \( nL_{o} \). Thus, the leading-leg voltage \( v_{lea}(t) \) begins to decline linearly and it is calculated as follows:

\[
    v_{lea}(t) = V_{in} - nL_{o}(t - t_{1})/2C_{oss}
\]

where \( C_{oss} \) is the parasitic capacitance of MOSFET.

**Mode 3** \( [t_{2} \sim t_{3}] \): At \( t_{2} \), \( v_{p1}(t) \) falls to zero and \( D_{1} \) starts to conduct. The secondary voltage of \( T_{1} \) is clamped to zero by \( D_{1} \) and \( D_{2} \). During this mode, the resonance of \( L_{k1} \) and \( 2C_{oss} \) occurs in the leading-leg. According to the initial conditions and the Kirchhoff’s law, the voltage of leading-leg can be expressed as:

\[
    v_{lea}(t) = 0.5V_{in} - \frac{nL_{o}}{2C_{oss}\omega_{1}} \sin \omega_{1}(t - t_{2})
\]

where \( \omega_{1} = 1/\sqrt{2C_{oss}L_{k1}} \).

**Mode 4** \( [t_{3} \sim t_{4}] \): At \( t_{3} \), \( v_{lea}(t) \) drops to zero and the parasitic diode of \( Q_{3} \) begins to conduct, thus \( Q_{3} \) can be turned on with ZVS. During this mode, \( v_{lea}(t) \) is maintained at zero and
the voltage $0.5V_{in}$ appears on $L_{k1}$. Due to the existence of this voltage, $i_{p1}(t)$ decreases linearly until the commutation between $D_1$ and $D_2$ is completed. This mode ends when $i_{p1}(t)$ falls to zero at $t_4$.

Mode 5 [t_4–t_5]: The primary current of $T_1$, $i_{p1}(t)$ is maintained at zero and $D_1$-$D_1$-$D_6$ are in on-state. The primary voltage of $T_2$, $v_{p2}(t)$ is $0.5V_{in}$ and the rectified voltage is equal to the secondary voltage of $T_2$. Only $T_2$ transfers primary power to secondary side.

Mode 6 [t_5–t_6]: At $t_5$, $Q_3$ is turned off and $D_3$ starts to conduct. The secondary windings of $T_1$ and $T_2$ are connected in parallel and the resonance of leakage inductances and junction capacitances occurs in the primary side. The lagging-leg voltage $v_{lag}(t)$ increases and the voltage across $Q_2$ decreases with sinusoidal shapes, respectively. The key voltages in this mode are expressed as follows:

$$v_{lag}(t) = (nI_o + I_m)(L_{k1} + L_{k2})\omega_2 \sin \omega_2(t - t_5)$$

$$v_{Q2}(t) = V_{in} - v_{lag}(t)$$

where $\omega_2 = \frac{1}{\sqrt{2C_{oss}(L_{k1} + L_{k2})}}$.

Mode 7 [t_6–t_7]: $v_{lag}(t)$ reaches to $V_{in}$ and $Q_2$ can be turned on with zero voltage. In this period, constant voltages appear on $L_{k1}$ and $L_{k2}$ because the secondary wings of $T_1$ and $T_2$ are still in parallel. Thus, the primary currents change linearly. This mode ends when $i_{p2}(t)$ drops to the magnetizing current value at $t_7$.

Mode 8 [t_7–t_8]: At $t_7$, the secondary current of $T_2$ is zero and $D_3$ is turned-off. The commutation between $D_3$ and $D_6$ starts to be processed. $i_{D3}(t)$ increases while $i_{D6}(t)$ decreases. When $i_{D6}(t)$ drops to zero at $t_8$, this mode ends.

Mode 9–16 [t_8–t_16]: The converter enters into the second half cycle and the operations are similar to the previous modes.

3. Comparison with the traditional PSFB converter

3.1 Voltage gain

The output voltage is regulated by adjusting duty-cycle $D$ and it is equal to the averaged value of rectified voltage. For simple illustration, only Mode 1 [t_0–t_1] (duty-cycle interval) and Mode 5 [t_4–t_5] (freewheeling interval) are considered since the durations of other modes are very narrow. In the traditional PSFB converter, the rectified voltages are $nV_{in}$ and 0 during duty-cycle interval and freewheeling interval, respectively. They are $nV_{in}$ and $0.5nV_{in}$ in the proposed converter. The voltage gains can be obtained by averaging rectified voltage.

For the traditional converter,

$$G_{tra}(D) = \frac{V_o}{V_{in}} = nD$$

For the proposed converter,

$$G_{pro}(D) = \frac{V_o}{V_{in}} = nD + \frac{n(1 - D)}{2}$$

$G_{pro}(D)$ is higher than $G_{tra}(D)$ since $D$ is smaller than 1. The converter with higher voltage gain is helpful to reduce the turns ratio of main transformer. Thus, the voltage stress of rectified diodes in the proposed converter is lower than that in the traditional converter, which is helpful to reduce power loss.

3.2 Output filter requirement

$LC$ filter is employed in the proposed and traditional converters. Its main function is to achieve averaged value of rectified voltage. The required filter inductor is designed according to a given current ripple and rectified voltage. Its value in each converter converter can be expressed as follows:

$$L_{tra} = \frac{T_vV_o}{2\Delta I_o} \times (1 - D)$$

$$L_{pro} = \frac{T_vV_o}{2\Delta I_o} \times D(1 - D) \times (1 + D)$$

From (10) and (11), the inductance ratio for the required filter inductors is derived as follows:

$$k(D) = \frac{L_{pro}}{L_{tra}} = \frac{D}{1 + D} < 1$$

Therefore, the filter inductance of proposed converter is smaller than that of traditional converter. This advantage is very beneficial for the improvement of power density.

3.3 ZVS condition of lagging-leg switches

The ZVS operation is obtained by using the energy stored in inductive components to discharge the junction capacitor of switch. The ZVS condition of lagging-leg switches in the traditional PSFB converter can be expressed as

$$\frac{1}{2}L_{ik}(nI_o)^2 > C_{ox}V_{in}^2$$

The available inductive energy is insufficient to fully discharge the junction capacitor and ZVS operation cannot be
For the proposed converter, the ZVS of lagging-leg switches is achieved during **Mode 7**. The ZVS condition is calculated from (6) as

\[
\frac{(nI_o + I_m)(L_{k1} + L_{k2})}{\sqrt{2C_{oss}(L_{k1} + L_{k2})}} > V_{in} \quad (14)
\]

In the view of energy, (14) is modified as

\[
\frac{1}{2}(L_{k1} + L_{k2})(I_m + nI_o)^2 > C_{oss}V_{in}^2 \quad (15)
\]

It can be noted from (15) that the leakage inductances of $T_1$ and $T_2$ can be used to discharge the junction capacitors. Moreover, the magnetizing current $I_m$ is helpful to increase the available inductive energy. Therefore, the ZVS of lagging-leg switches can be achieved over a wide load range.

### 3.4 Primary circulating current

Fig. 6 shows the simplified primary voltage and current of transformers in the traditional and proposed converters. As shown in Fig. 6(a), the primary voltage is zero but the current is non-zero during freewheeling interval of $0.5(1 - D)T_s$ in the traditional converter. This circulating current causes excessive conduction loss. On the other hand, all primary voltages are in phase with currents in the proposed converter, as shown in Fig. 6(b). The primary energy is transferred to output side during the whole switching period. Thus, the primary circulating current is removed in the proposed converter.

### 4. Experimental results

In order to verify the feasibility of proposed converter, an experimental prototype is built. The prototype is designed with the following specifications: input voltage $V_{in} = 300 - 400$ V; output voltage $V_o = 120$ V; maximum output current 10 A; switching frequency $f_s = 100$ kHz. Another prototype based on the traditional PSFB converter is also built for the comparison with the performance of the proposed converter.

Fig. 7 shows the key waveforms of the proposed converter at $V_{in} = 400$ V, $I_o = 10$ A. As shown in Fig. 6(a), the primary voltage and current of transformer $T_1$ falls to zero simultaneously during freewheeling interval. Thus, the primary circulating current is removed. On the other hand, the voltage and current of $T_2$ are nonzero and they are kept in phase with each other. The primary power can be transferred to the secondary side through $T_2$ during the whole period. This feature contributes to reduce output filter requirement and voltage stress of rectified diodes. The experimental results are consistent with the theoretical waveform shown in Fig. 4.

Fig. 8 shows the ZVS waveforms of lagging switch at: (a) 2 A; (b) 10 A.
proposed converter and traditional converter. Due to lower filter requirement, wider ZVS range and removed circulating current, the proposed converter can achieve higher efficiency than the traditional PSFB converter.

5. Conclusion

In order to improve the performance of isolated power supply used for hybrid CB, a novel ZVS FB converter is proposed in this paper. Compared to the traditional PSFB converter, the proposed converter has the following advantages:

1. Higher voltage gain can be achieved;
2. The requirement of output filter is reduced;
3. ZVS range of lagging-leg switches is extended;
4. The circulating current is removed and the primary energy can be continuously transferred to secondary side.

An prototype based on the proposed converter is built. Experimental results show that all aforementioned advantages are verified and the proposed converter can achieve much higher efficiency than the traditional PSFB converter.

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