Smart-Switching Pulse Width Modulation for High-Density Power Conversion

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Power electronic converters comprise of solid-state switching devices and energy storage elements. With technological advancements in device technology, the power density of converters has significantly reduced since the 1970s. This paper discusses the principles of smart-switching pulse width modulation (PWM) approaches that can significantly reduce the energy storage requirements for high-density power conversion (0.1–10 µF vs. 100–1000 µF). Smart switching approaches feature an intelligent switching sequence, accurate duty ratio calculation, and robust fast bandwidth controls. Along with a discussion on the main features of smart-switching, several applications of smart-switching PWM approaches are presented with simulation and experimental results.

Keywords: capacitors, control bandwidth, energy storage, pulse width modulation

1. Introduction

Modern Power Electronics (PE) is an integral part of electricity generation, delivery and utilization systems. In addition to being the workhorse of various industrial applications, PE has become ubiquitous in our daily lives, being present in computers, air-conditioners, light dimmers, phone chargers, induction stoves, etc. It may be argued that our progress to-day’s generation of computing ICs are composed of several billions of transistors per chip (9). In contrast, PE has followed a rather modest growth trajectory, primarily due to two reasons which are tied to the two issues stemming from the essential ingredients of converters:

(1) Solid state power switches (SS): The current carrying and voltage blocking capacity of switches in PE applications are orders of magnitude higher than those in computers, making the monolithic integration of non-planar semiconductor realizations next to impossible.

(2) Energy storage elements (ES): The state-of-the-art PE converters require sizable inductors and capacitors in order to match the topological interconnection of switches between energy sources and loads, and meeting the functional requirements of the target applications.

Since the heterogeneity among these ingredients precludes an interconnection system amenable to an automated manufacturing process, PE converters are realized using bus bars, physical-wiring harnesses or printed-circuits, limiting the scope of their size, weight and cost reduction. Nevertheless, PE systems have achieved slow and steady significant milestones through incremental progress in SS technology, leading to modest improvements in new applications, improved power density, high reliability, reduced costs, etc, while ES technologies have remained relatively stagnant. The foundational modeling approach, based on state-space averaging, developed at in the 1970s and 80s, provided the the analytical backbone that enabled the physical PE artifacts to fulfill the application needs with adequate performance levels (8). After about five decades of slow and steady progress, the discipline is approaching its physical limits of growth that has been built on the current paradigm of semiconductor device technology led improvements. While the historical trends have been successful in establishing power electronics as a discipline and resulted in its systematic, but relatively slow growth, the large scale growth in future application requirements calls for a transformative technology revolution rather than an incremental evolution.

Recent developments in wide-band-gap devices (WBGs) are considered the latest catalysts for the next step in growth. Notably, SiC and GaN devices are relaxing, if not removing the constraints of interfacing bulky thermal management components to the semiconductor package. This has the long-term potential to remove one of the major complexities in the heterogeneity in system realization and manufacturing processes, thereby leading to size and cost reductions. On
the other hand, it is apparent that the advancements in SS devices would only lead to reduction of switch size and heat sink size, unless the issue of managing energy storage is addressed squarely. The persistence of large size energy storage needs across various applications is well-recognized, and is exemplified in Fig. 1. The figure shows a photograph of a state-of-the-art high PE converter, that illustrates the size of ES elements relative to the balance of system components. Therefore, if the promise and potential of WBGs in launching the next PE revolution is to become reality as may be illustrated by a conceptual S-curve shown in Fig. 2, the emerging paradigm shift cannot exclusively rely upon advances in SS, but should necessarily squarely address the sizing and scaling of ES elements. Inherent and native size reductions of ES elements would and could arise from advancements in magnetic and dielectric materials forming inductors and capacitors respectively(7)–(9). Some of the recent approaches of integrated design and realization of inductors and capacitors could also lead to rather modest size and cost reductions(10)(11). Furthermore, faster switches capable of operating at higher switching frequencies can and would lead to reduction of ES requirements. These size reductions in ES would be realized using the approaches of classical pulse width modulation (PWM), that presupposes a constant, (or infinitely stiff) voltage and/or current that is being modulated in order to realize the desired waveform synthesis by the PE system. The premise of this paper is that orders of magnitude in ES requirements of PE converters can be realized through faster implementation of control in comparison to current state of the art, even without, or in addition to the size reductions that arise from native advances in the SS and/or ES technology. Towards this end, the concept of smart-switching PWM is introduced. Smart-switching PWM is defined as an approach of modulating the duty ratio of the power converter switches without an implicit assumption that the modulated voltage and/or current variables remain constant during a switching period.

Due to the key relaxation of this fundamental assumption smart-switching PWM allows a synthesis of the desired functional characteristics of the converter even in the presence of rather large amount of ripple voltage and/or current in the intermediate energy storage devices. Thereby, much smaller energy storage devices may be employed in the power converter design. Naturally, this feature requires a faster implementation of the control and regulation function. Conventional realizations of feedback control such as proportional/integral (PI) approaches, illustrated in Fig. 3, manipulate a slowly-varying duty-ratio in a hierarchal manner using a series of inner and outer regulator loops that operate progressively at slower dynamic bandwidths. These loops are typically tuned at a bandwidths that are roughly a decade slower each, as the progress from the switching devices towards the terminal quantities of interest. As a result, larger ES elements are necessary to ensure sufficient margins of design to meet transient performance requirements. These state-of-the-art control approaches can be benchmarked using modeling approaches to understand their limitations(12).

On the other hand, smart-switching PWM uses more complex control approaches such as model predictive control (MPC), that can meet the required transient performance even with much smaller ES elements. To be sure, robustness of the overall system need to be guaranteed on approaches different from classical phase and gain margin estimates. The work presented by the authors recently(12)(13) pioneers a radically different switching approach, and the associated mathematical modeling techniques, which no longer need bulky and virtually infinite ES elements. In contrast to the traditional approach to improve the power converter density by increasing switching frequency or using new devices alone, it breaks down the conventional barrier that limits the power converter density by using smart switching. Using smart switching, converters such as shown in Fig. 4, can now employ only a few microfarads of buffer ES capacitances (0.1–10µF vs. 100–10,000µF). Due to the low capacitance requirement, PE converters can operate successfully with ceramic or film
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technology capacitors as opposed to electrolytic capacitors. Electrolytic capacitors are one of the least reliable and most lossy components of the system. Together with as much as a 90% reduction in capacitor volume, the use of film technology leads to a 10 times improvement in lifetime (Fig. 8). Detailed comparative analysis in terms of overall cost, volume, efficiency, lifetime have been previously published by the authors (14)(15). This paper aims to provide the basic formulation of smart-switching PWM using MPC as a process which can be implemented on any power electronic converter where one or several sources and loads are connected to the intermediate energy storage element via an active semiconductor device.

Section 2 presents the design aspects of a general power converter system with multiple sources and multiple loads for using the principles of smart-switching. The realization of smart-switching PWM is explained for a candidate voltage source power converter application in Section 3, along with a brief discussion of MPC and robustness. Two applications of smart-switching PWM for high density voltage source power converter realizations are illustrated in Section 4 with simulation and experimental results. Section 4.3 provides a summary of the results from the modulation of a current source power converter application illustrating the generalized scope of the principle of smart switching. A final concluding section provides a summary of smart-switching PWM outlining potential future directions.

2. Principle of Smart-Switching PWM

Let a power converter consist of specified states as external terminal variables that are continuous functions of time with specified power quality levels (THD, %ripple, etc.). Naturally, if the external terminal variables are specified to be currents, they would be inductor currents, and if they are voltages, they would be capacitor voltages. These external terminals are typically connected to energy sources and energy loads such as batteries, supercapacitors, motors, grid, etc. Consequently, such inductors and/or capacitors at the external terminals will carry a nominal amount of energy storage, most often, defined by the energy source and load specifications.

Let the vector of the state variables of the external terminals be labelled $x_f$.

Furthermore, the converter will consist of additional energy storage inductors and/or capacitors at the interfaces to the semiconductor switching devices internal to the power converter. These intermediate energy storage elements are presumed to be bulky for robust performance. Assuming that the energy transfer through the power converter during each switching period to be one per unit, the intermediate energy storage elements can typically store up to thousands of units of energy for robust performance. Consequently, the specified stiff current or voltage waveforms of such internal inductors or capacitors respectively will feature negligible ripple. While the size of the external terminal energy storage elements are defined by power converter performance requirements, the stiffness requirements of the internal elements are implicitly implied. Let the vector of the state variables that are internal currents and voltages without explicit stiffness specifications be labelled $x_i$.

Let the converter consist of several switching throws that interconnect the pathways among the internal and external energy storage elements, sources and loads, labeled by a switch vector $h_S$, whose elements can take values of 0 corresponding off-state and 1 corresponding to on-state. The switching intervals of each of the throws are commonly specified using the duty ratio of the corresponding throws, which may be labeled by the duty ratio vector $d_S$. In classical PWM converters operating in continuous conduction mode, the duty ratio of the switches determine the transfer property of the switching operation as a linear and reciprocal function between the stiff voltage/currents the switched current/voltages, due to the negligible ripple or infinite stiffness in the internal and external energy storage elements (16). The simple and linear duty ratio relationships facilitate in straightforward development of various modulation strategies (17). While this has been the traditional practice in converter design, it is well-known that the linear and reciprocal transfer properties do not hold when the stiffness assumptions are violated, for instance under discontinuous conduction mode (18). On the other hand, the relaxation of stiffness assumptions of the internal state variables of the internal energy storage devices are removed, power density of the converters can be dramatically increased. Here, the time-functions of each of the entries of $h_S$ are determined through an explicit nonlinear solution of the transfer characteristics of the switching converter without any explicit small ripple assumptions of the internal energy storage state variables of the power converter. To be sure, the state variables of the external terminal energy storage elements are still assumed to be stiff, featuring negligible ripple. This approach of determination of the time functions of $h_S$ is defined to be smart-switching, which enables size reduction of internal energy storage elements without compromising the power converter performance or effecting the terminal specifications at the source and the load.

3. Smart-Switching PWM for a Voltage Source Converter

This section discusses the underlying principles of smart switching pulse width modulation that enable lean PE conversion, permitting the use of tiny film capacitors.

3.1 Converter Topology

A typical application of a cascaded dc to three phase ac power converter shown in Fig. 4 is used to describe the operating principles of Smart-switching PWM (19). The boost converter stage may be considered to be the source, designated by $S$, and the dc to three phase inverter may be considered the load, designated by $L$. In general, the source and the load SS devices may or may not be operating at the same switching frequency. Hence,
the source and the load SS devices may not be synchronized. Further, the source or the load (S/L) can be connected directly to the ES element, without any SS devices. The underlying assumption for such operational approaches is the presence of a bulky ES element which will compensate for the energy imbalance over one or several switching cycles. Thus, the classical realization would be predicated on the use of a ‘large’ dc bus capacitor that maintains a ‘stiff’ dc bus voltage. Here inductor on the dc side and the inductors on the three phase ac side are the external terminal energy storage elements, while the dc link capacitor is the internal energy storage element.

The input dc to dc boost power converter stage would regulate the dc bus voltage at a desired command value. It would feature an inner current regulator loop and an outer voltage regulator loop. The intermediate dc bus voltage would be converted to three phase ac using a three phase modulator such as a space vector modulator, often incorporating its own inner current loop, etc. The design of the regulator for the boost converter and the design of regulator for the three phase inverter would be ‘decoupled’, on the basis of having a ‘stiff’ dc voltage, ensured by a large enough dc bus capacitor. Furthermore the modulation function and the control function are separated from each other, with the modulator providing a ‘gain’, and the controller providing dynamic features.

The design of controllers for such systems have been the subject of several publications. Some of the approaches have reduced the size of the dc bus capacitor through the use of dc link feed-forward with modest success. A systematic approach to the design of the classical system, with an explicit model that identifies the scaling and sizing properties of the dc capacitor size on the basis of transient voltage over shoot has been developed in. The alternative approach discussed further in this section considers the modulation and regulation problem of the source and the load as a whole, with dramatic reduction in the dc capacitor size compared to the classical approach. In other words, the approach of smart switching PWM poses the problem of modulating the converter switches when the capacitor ripple voltage is not negligible.

### 3.2 Switching Sequence Selection

The first step in the smart-switching PWM approach is selecting the sequence of switching operations based on selected performance features. Thus, in contrast to the conventional approach, under smart switching, the connection of switches of the S/L stages to the ES element is synchronized and sequenced in order to complete a cyclic energy transfer process in every switching cycle. This permits minimal or no energy storage at the intermediate element. In general, the connection of S/L together to the ES element, during any part of the switching cycle, minimizes the ripple across the ES element and reduces overall reactive power processing requirements. The sequencing of the switching functions of the S/L can be based on minimizing a predefined cost function or an optimization algorithm. The sequencing process can employ space-vector modulation paradigms for realizing the power transfer operation.

### 3.3 Duty Ratio Calculation

Once the sequence of operation of various switches are determined, the duty ratio intervals of each of the switches have to be determined. In the presence of a bulky capacitive ES element, duty ratio calculations can be a simple linear function of the desired quantity and the high-frequency variation in dc link quantity would not be necessary. This, in cases of scalar modulators, a simple comparison function with a triangular-carrier and in the case of vector modulator a matrix solution may be employed to determine the duty ratio. For instance, in Fig. 4, the duty ratio of the S converter may simply be based on averaging principles wherein \( d = \frac{v_{dc}}{V_{om}} \) where \( v_{dc} \) is the dc voltage and \( V_{Cap} \) is the constant dc link voltage. Further, the duty ratio calculations would be regulated by conventional feedback control realizations such as PI loops with a bandwidth much slower than switching frequency. On the other hand, smart switching PWM approaches require more complex analysis which can capture variations in ES element voltages/currents and source/load currents. Because of the use of small but finite size of the ES elements, the quantities of interest can vary significantly per switching interval in a switching cycle. Still the duty ratios, which include such high frequency variations, can be calculated based on energy balance and principles of averaging of piecewise solutions of the waveforms. Implementation of accurate duty ratios minimize steady-state errors and improve the output waveform quality. Further details on specific modulation approaches for the particular case are provided in Section 4.

### 3.4 Robustness

The natural outcome of the presence of bulky ES element in conventional cases is robustness during transient and steady state operating conditions through design margins. During any changes in operational conditions of source and/or load, the bulky energy storage presents itself as a virtually infinite and immediate source and/or sink of energy. The large sized ES elements may be sized to have acceptable transient performance in terms of overshoots/undershoots.

On the other hand, new ideas of robustness need to be introduced in the absence of bulky ES elements for high performance power conversion. Smart switching approaches have fast bandwidth control wherein the control bandwidth that is at least an order of magnitude faster than switching frequency, providing almost a real-time opportunity to control SS devices. Furthermore, the determination of the duty ratio of switching intervals naturally depends on the various parameters of the circuit and measured values of various state variables. The predetermined duty ratios are only as accurate as the estimates in parameters and the measured variables. Therefore, the waveforms that are being synthesized using the approach would have deviations (or residues) from the nominal and command values, particularly during large and sudden transients. Furthermore, the switching approach could potentially lead to unstable operating conditions.

Under smart switching PWM approach, the residues in the controlled variables are actively measured using feedback, and the predetermined switching intervals are adjusted to drive the residue down to acceptable values. This enables implementation of algorithms such as flux or capacitor charge restoration, wherein the charge in the lean energy storage element is restored in every high frequency switching cycle. The adjustment of the duty ratio intervals are done only on a certain switching interval, and not on any or all of the switching interval. This is a critical factor that ensures the stability.
of the smart switching PWM strategy. In essence, the algorithm is selected such that the product of the residue and the time derivative of the residue is always a negative quantity. This ensures that the overall residue returns to a predetermined boundary layer near zero, allowing for an acceptable error that is dictated by the resolution of the sensing, computing and implementation circuits. The robustness of the synthesis and regulation is guaranteed by the control laws using the theory of variable structure systems (21).

3.5 DSP/FPGA Implementation

Smart switching PWM eliminates the need of passive and bulky ES elements through the use of an intelligent controller. While conventional control approaches operate at bandwidths that are much slower than the switching frequency, the intelligent control implementation requires high performance DSPs, FPGAs or SoCs to implement fast bandwidth control with clock frequencies reaching hundreds of megahertz. The ES element sensing circuitry, which can implement algorithms such as capacitor charge restoration, can be implemented using mixed signal circuits employing op-amps, comparators, etc. Dropping prices of FPGA prices (22) will continue to pave the way for smart switching PWM approaches.

4. Application Examples

This section demonstrates the application of smart switching for the dc to three phase voltage source converters for high density PE conversion using two modulation approaches, stored energy modulation (SEM) and zero energy modulation (ZEM). The typical waveforms of the dc link capacitor voltage and the switched and modulated output voltages for the $S$ phase in the case of conventional PWM, SEM and ZEM are illustrated in Fig. 5.

4.1 Stored Energy Modulation

The stored energy modulation approach presumes lean energy storage at the dc link element which may be only 2–10 p.u. (vs. 100–1000 p.u. in the case of conventional approaches). Following the principles of smart switching, as discussed in Section 3, the dc link capacitor voltage features a predefined charge-discharge pattern as illustrated in Fig. 5. The switching period is divided into on idle (or zero-state interval) $d_0$, and 3 active intervals, namely $d_1$, $d_2$ and $d_3$. During the $d_1$ interval the switches corresponding the source and one of the 3-phase line-line to loads are connected to the dc bus. Following that, during each of the $d_2$ and $d_3$ intervals, two of the three 2-phase line-line to loads are connected to the dc bus, in a sequenced manner to follow a cost function which can minimize voltage ripple, peak voltage, ripple current, etc. The duty ratio calculation for each of the intervals may be calculated by (1) as follows (23):

$$d_j = \frac{C f_s V_N}{i_j} \left(1 + \frac{e_j}{E_N} - 1\right) \ldots (1)$$

where, $d_j$ is the $j^{th}$ interval duty ratio, $C$ is the dc link capacitance, $f_s$ is the switching frequency, $V_N$ and $E_N$ are the nominal dc link capacitor voltage and the energy level respectively, and $i_j$ and $e_j$ are the average dc link capacitor current and total energy transfer to/from the dc bus during the $j^{th}$ interval respectively. The values of $i_j$ and $e_j$ are determined using the command values and/or measured values of voltages and currents that are flowing in the $S$ and $L$ terminals during the $j^{th}$ interval.

Figures 6 and 7 illustrates experimental result from a 1.6 kW, 170 V dc to 170 V 3-phase ac power converter, switching at 40 kHz. In this example, the dc bus capacitor is maintained at a nominal dc link voltage of 340 V. The modular prototype features four tiny film capacitors of 5 μF for each of the phase legs of Fig. 4 with allowable ripple current of 4.5A each and ripple voltage of 20% of rated value. The high quality of the output waveforms in spite of a small dc link ES element is clearly evident from the experimental waveforms. In this case, the storage energy in the dc link represents 10 p.u. of the energy transferred to the load during a switching period with a ripple voltage of 6%. The capacitor size reduction is illustrated in the photograph shown in Fig. 8. For an electrolytic capacitor, the life expectancy at full rated voltage ($LV_{\text{op rated}}$) is multiplied by the voltage operating factor ($K_V$) to obtain the operating life expectancy at operating voltage (2) (15).

$$LV_{\text{op, life}} = LV_{\text{op, rated}} \times K_V = 20,000 \times 1.3 = 26,000 \ldots (2)$$

In contrast, for a film capacitor employed in the prototype, the life expectancy can be approximately calculated with a simplified formula (2).

$$LV_{\text{op, life}} = LV_{\text{op, rated}} \left(\frac{V_{\text{rated}}}{V_{\text{operating}}}\right)^8 \approx 98,000 \ldots (3)$$

where, $LV_{\text{op, life}}$ is rated life expectancy. A detailed comparison of the smart switching PWM system against conventional PWM in terms of the overall parameters, including models for losses, efficiency, capacitor lifetime, etc. for this application example may be found in (15).

4.2 Zero Energy Modulation

As may observed from Fig. 5, the SEM approach synthesizes the output waveforms using trapezoidal shapes during smart switching PWM as opposed to strictly rectangular waveforms as in the case of conventional PWM, while accommodating rather large variations in the dc link voltage. The ZEM approach takes this
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Fig. 6. Three phase output currents (top) and dc voltage (bottom) from the prototype converter obtained using (a) Simulation and (b) Hardware of the example photovoltaic inverter under SEM

Fig. 7. Zoom in of various switching function waveforms (top 4), dc bus voltage (middle) and various pole voltage waveforms (bottom 3) from the prototype converter obtained using (a) Simulation and (b) Hardware of the example photovoltaic inverter under SEM

Fig. 8. Photograph of the research prototype illustrating the capacitor size reduction

approach to its limit and allows the dc voltage to reach zero during each high frequency switching cycle. This can be observed in Fig. 5, where the dc link ES element returns to zero storage at the end of every high frequency switching cycle. Similar to smart switching SEM approach, the dc link capacitor voltage as a predefined charge-discharge pattern as illustrated in the figure. In this case, the duty ratio calculation for each of the switching intervals may be calculated as follows (4) (14):

\[
d_j = \frac{v_j}{\sqrt{C e_j}}
\]

where, \(d_j\) is the \(j^{th}\) interval duty ratio, \(C\) is the dc link capacitor voltage and \(e_j\) and \(v_j\) are the average dc link capacitor voltage and amount of energy transferred during \(j^{th}\) interval. The values of \(v_j\) and \(e_j\) are determined using the command values and/or measured values of voltages and currents that are flowing in the \(S\) and \(L\) terminals during the \(j^{th}\) interval.

Figure 9 illustrates experimental results from a prototype converter with a 30 W, 200 V, 400 Hz induction machine load.
operating under constant volts per hertz approach, switching at 7.8 kHz. The inverter features a tiny 39 nF film capacitor. The high quality of the output waveforms in spite of a small dc link ES element is clearly evident from the waveforms.

4.3 Application to Current Source Converters

The application of smart-switching in current source converter predates their application to the cascaded voltage source converter described in the previous section (17)–(19). The formulation of the problem and the subsequent solution was posed as a corrective scheme to accommodate proper operation of the converter under light loads when the dc link inductor current operates in discontinuous conduction. Nevertheless, the solution and the modulation approach follows the principle of smart switching that is generalized in this paper. The schematic of the current source inverter application is illustrated in Fig. 10. In this case, the dc link inductor is the internal energy storage element, while the capacitor at the dc input terminal and the three phase capacitors at the ac output terminals are the external terminal energy storage elements. Therefore, as in the case of the voltage source converter, the inductor current waveform can be constructed and shaped to maintain the required waveform synthesis functions using sequenced switching, duty ratio calculation and robust control. Reference (19) provides detailed steps and algorithms of the switching sequence selection and duty ratio calculation. In these references, the robustness aspect of smart-switching was ensured through the additional external feedback regulators. Figure 11 illustrates experimental results from a prototype 3 kW rated current source inverter. Operating at a switching frequency of 8 kHz, the inverter employs a 600 μH dc link inductor (18). The figure illustrates the sequenced three-phase duty ratios and characteristic charge-discharge pattern of dc link current featuring ZEM.

5. Conclusions

In order to realize the power density improvements promised by the use of faster switches based on WBG semiconductors requires a holistic view of power converter design, that considers the energy storage requirements within the converter and the implementation of the modulation and regulation. This paper posits that the conventional feedback control techniques based on state space averaged model for the switching operation places undue burden on the requirements of energy storage devices to ensure system stability and transient performance. Figure 12 illustrates this in conceptual manner along with a real concrete example case that is based on the smart switching PWM that is presented in this paper. Smart switching PWM develops the modulation problem, dynamic control and regulation problem in a single coupled step, instead of separating the regulation and control problem and the modulation problem as two separate steps. This paper presents the idea and illustrates the outline of its application in two dc to three phase voltage source converter examples, along with a summary of results from a dc to three phase current source converter example.

The radically new smart switching PWM lays a new foundation in PE which can be developed and applied across the discipline. The key idea of the approach is that as opposed to operating the power converter switches in any way with the assumption of the presence of a virtually infinite ES element, they are operated carefully with the assumption of lean ES elements. The foundational idea of smart switching which can be generalized to the power converter topologies beyond dc-three phase ac converters. The smart switching concept can be defined as the operation of the switches in a sequential
and a defined manner in order to complete the desired energy transfer operation while ensuring system stability and high performance. Such an operation has proved to be able to realize high-density power conversion by virtually eliminating the buffer ES element present in state-of-the-art PE converters with averaged switching concepts.

In order to maintain high performance, at the beginning or the end of the energy transfer cycle, the buffer ES element should be actively controlled to follow energy conservation wherein the energy storage is reset to a predefined level before or after the cycle. *Per cycle energy conservation* requires high bandwidth control where the controller is at least 10 times faster than the \( f_s \). This is in contrast to today’s practice of operating power converters at a limited bandwidth so that the maximum frequency is at most 10 times slower than the \( f_s \). This approach takes advantage of the declining costs of high performance digital signal processors (DSPs) and field programmable gate arrays (FPGAs) to implement advanced and computationally complex control techniques for smart power management. Further, such smart switching can facilitate numerous other high performance approaches, which has not been possible with standard slower control methods with limited intelligence. This idea of smart switching can be extended to other power converter topologies for dc-dc, dc-ac-dc, and ac-ac conversion with different switching configurations and variety of applications.

While this work emphasizes on aggressively reducing the size of the intermediate energy storage element, there may be certain limitations imposed by specific applications. Although the focus of this paper is on employing minimal energy storage at the dc link, this assumption may be modified depending on overall system specifications. For instance, the need to continue to operate during loss of power by providing ride-through capabilities may rely upon having adequate energy storage at the dc link. Alternatively, techniques such as utilizing load inertia or derating switches/loads may be employed to manage ride-through events. Some applications could employ separate energy storage elements such as supercapacitors to survive long ride-through conditions. Furthermore, since off-the-shelf capacitors are sized for rated voltage and current capabilities, radical reductions in capacitor size may lead to limited design choices for such realizations.

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