Nimble: Efficiently Compiling Dynamic Neural Networks for Model Inference

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Abstract
Modern deep neural networks increasingly make use of features such as dynamic control flow, data structures and dynamic tensor shapes. Existing deep learning systems focus on optimizing and executing static neural networks which assume a pre-determined model architecture and input data shapes—assumptions which are violated by dynamic neural networks. Therefore, executing dynamic models with deep learning systems is currently both inflexible and sub-optimal, if not impossible. Optimizing dynamic neural networks is more challenging than static neural networks; optimizations must consider all possible execution paths and tensor shapes.

This paper proposes \textit{Nimble}, a high-performance and flexible system to optimize, compile, and execute dynamic neural networks on multiple platforms. \textit{Nimble} handles model dynamism by introducing a dynamic type system, a set of dynamism-oriented optimizations, and a light-weight virtual machine runtime. Our evaluation demonstrates that \textit{Nimble} outperforms state-of-the-art deep learning frameworks and runtime systems for dynamic neural networks by up to $20 \times$ on hardware platforms including Intel CPUs, ARM CPUs, and Nvidia GPUs.

1 Introduction

As deep learning-based applications have become ubiquitous, so have systems for optimizing, executing, and deploying such applications. A number of systems research projects focus on enhancing the performance of a subset of pre-trained models produced by deep learning (DL) researchers [11, 16, 24, 46]. Specifically, these models represented as static data flow graphs where the sizes of each input and output (i.e. tensors or n-dimensional arrays) are known a priori, ensuring the execution path remains unchanged on every invocation. We refer to models with this static nature as static models. Continued advances in neural networks, especially those in natural language processing, have introduced new dynamism in models, such as control flow [18, 41], dynamic data structures [28, 42], and dynamic shapes [13]. We refer to models exhibiting these behaviors as dynamic models.

As dynamic models mature and continue to move from research to production, it calls for an efficient and cross-platform inference system. This poses new challenges for deep learning practitioners, as dynamic models introduce input-dependent graph topology, breaking existing system assumptions and invalidating optimizations designed for purely static data flow graphs. However, no existing solutions fulfill these requirements.

Many existing approaches to dynamic model optimization apply or extend existing deep learning frameworks [15, 22, 23, 30, 32, 44, 47]. However, deep learning frameworks optimized for training can be limiting in model inference settings due to their rich feature set. In order to realize these features frameworks are often monolithic, large, and non-portable. Moreover, approaches which inherit from frameworks rely on third-party kernel libraries such as OpenBLAS [49], cuDNN [10], and MKL-DNN [21] to achieve competitive performance. These libraries expose a fixed set of operators for the corresponding hardware, compromising the portability of dynamic models which require a large number of operators with varying data types and shapes. Designing a new interface independent of existing frameworks provides a clean programming model but often at the cost of performance, due to dynamic interpretation of the model [32].

An alternative approach which has generated significant interest in both academia and industry is the end-to-end optimization of neural networks using deep learning compilers, such as XLA [43], Glow [37], TVM [8], and MLIR [27]. Deep learning compilers differ from traditional deep learning frameworks by separating execution into a compilation, and runtime phase. The compilation phase enables whole-model optimization at the graph level, and workload specific kernel code-generation for multiple hardware platforms.

However, deep learning compilers have been primarily restricted to static models due to lack of support for dynamism. Specifically, in order to compile and execute the dynamic...
models, a system requires an intermediate representation (IR) which can statically represent dynamic constructs, a code generator which can generate kernels for dynamically varying data shapes, and a runtime to handle the dynamic execution and kernel dispatch accordingly. In addition, dynamic-specific optimizations, such as dynamic memory planning, the process of statically optimizing dynamic allocations, are necessary to achieve desirable performance. None of these features exist in the current deep learning compilers.

To this end, we present Nimble, a high-performance and portable system for compiling, optimizing and executing dynamic neural networks on multiple platforms. To the best of our knowledge, this is the first attempt to systematically handle dynamic models from a compiler perspective. First, we introduce type system extensions to handle data with unknown dimension, which is common in dynamic models, by performing type checking and inference for shapes with Any. Second, we devise several optimizations specific to dynamic models, including dynamic shape-aware code generation, memory planning, and device placement. Third, we propose a virtual machine (VM)-based runtime that contains tensor-level operations, enabling the exploration of new runtime and compiler optimizations as well as being portable, light-weight, and most importantly, able to execute dynamic models. Experimental results on LSTM [18], Tree-LSTM [42] and BERT [13] show that Nimble lowers the latency by 1.05× to 19.9× compared to the best solution whichever on mainstream hardware platforms both in the cloud (Intel CPUs and Nvidia GPUs) and at the edge (ARM CPUs).

In summary, this paper makes the following three core contributions:

- Proposes and builds an end-to-end system for efficient dynamic model inference across multiple hardware platforms, including an empirical study to benchmark the results;
- Devises several compilation and optimization techniques, including a dynamic type system, a memory planning pass, and heterogeneous device placement mechanism to place computation and data, and a symbolic kernel code generation and shape-based dispatch algorithm;
- Designs and implements tensor based abstract machine with a hardware-independent instruction set to efficiently and flexibly execute dynamic models across platforms.

The rest of the paper is organized as follows. Section 2 reviews the background of dynamic models from the system perspective and Section 3 gives the overview of Nimble. Section 4 presents the design and implementation of the compilation flow of Nimble, followed by VM-based runtime in Section 5. Section 6 provides the evaluation results using various models on different hardware platforms. Section 7 covers related work, and Section 8 concludes the paper.

2 A System Perspective to Dynamism

Dynamism is now common in state-of-the-art deep learning models in various forms, i.e. control flow, data-dependent model architecture, and variable data shapes imposed by dynamic batch size and/or input length. In the presence of these features, it becomes impossible to pre-compute certain program properties ahead of time, hence only a limited subset of optimizations available for static models can be directly reused. In this section, we first review the existing systems to support dynamism, followed by the discussion of supporting dynamic models using deep learning compilation techniques. Based on the observation, we propose our system Nimble and give an overview of it.

2.1 Existing systems

Researchers working on dynamic models typically use flexible deep learning frameworks to build proof of concept models, and then attempt to optimize the model using the built-in capabilities of the framework when deploying at scale.

Deep learning frameworks describe the model in either an imperative (define-by-run) or symbolic (define-then-run) fashion. Imperative frameworks, such as DyNet [32] and PyTorch [34], although user-friendly and flexible, may reduce performance due to eagerly executing each computation in isolation. Both DyNet and PyTorch support executing compute-intensive operators by reusing high-performance implementations from third-party libraries, however, the inherent nature of imperative execution substantially limits optimization, i.e. no operator fusion and batching. In addition each execution path requires the creation of a path specialized static data flow graph introducing overhead in dynamic cases, which can sometimes be unacceptable for particular application.

Not only do frameworks rely on vendor provided libraries, but many are written in a combination of multiple programming languages such as C++ and Python. The inclusion of platform specific libraries and/or arbitrary Python program fragments limits deployment and retargeting. Platforms such as resource limited edge or embedded devices do not support these libraries and/or languages limiting these solutions from executing on some platforms without serious re-engineering, leading to solutions such as Tensorflow Lite. Imperative programs are extremely effective at helping researchers prototype and test preliminary ideas, but not an ideal or systematic solution to deploying dynamic models at scale.

Alternatively, other deep learning frameworks use a symbolic approach, in which a user specifies the program as a data structure which can later be optimized, deployed, and executed. Frameworks in this style such as TensorFlow and MXNet already have introduced support for dynamism, such as control flow and dynamic batching [30, 47, 50]. Although these make it possible to use dynamic features, the extensions add complexity to an already complex programming model, and are often less integrated into the framework, requiring
users to use a sophisticated modified programming model when defining dynamic models.

In addition, in some cases, it is possible to reduce the dynamic model to a static one. For example, in RNN models with variable input length, a maximal input length can be used to statically unroll the network, and padding applied to the inputs in order to directly adopt optimizations performed on static models [48]. However, transforming a dynamic model into a static one for optimization is inflexible and only works for a subset of dynamic models. Programmability and flexibility aside, the above solutions inherit the cumbersome codebase of the deep learning frameworks which have poor portability to multiple platforms, especially edge devices. From a systems perspective, they are too heavy-weight to be adopted in these cases.

In order to enjoy the flexible description of dynamic models provided by high-level frameworks and the performance advantages of ahead of time optimization, prior work like Janus [22] attempted to bridge these two programming models for dynamic models. Janus was implemented as an extension to TensorFlow which parses the model defined in TF Eager and use speculative execution to eliminate control flow constructs within the model. Although this solution provides good performance in a subset of cases, it suffers from performance loss when speculative assumption is violated. Also, as it is still based on the framework, this solution inherits the drawbacks of poor portability.

Specific runtime systems were recently proposed to handle dynamic models [15, 44]. These systems are designed to address system-level issues that plague framework-based approaches, e.g., large overhead introduced by data flow graph construction. However, other issues, such as software dependencies, remain, which makes these runtime systems not standalone, but a customized component of a larger deep learning framework.

### 2.2 Limitation of Deep Learning Compilers

As discussed in 2.1, existing solutions to dynamic models have various limitations, the most pressing of which is the lack of portability and cross-platform support. A generic system which handles dynamic models for efficient inference is missing. Conceptually, this system should handle all dynamic models, provide portable performance across multiple platforms, and execute everywhere by virtue of being light-weight and dependency-free. With these goals in mind, deep learning compilers are a promising direction to explore, as these techniques aim to perform end-to-end optimization on models that can run with minimal memory footprint over multiple platforms.

However, current deep learning compilers are not able to process dynamic models due to missing the following dynamism-specific features.

- **An IR for representing dynamism.** Performing data type and shape inference on static models is straightforward as both the data type and shape of each operator are known during declaration and remain unchanged during runtime. However, the shape of an input tensor may vary wildly across different input samples in a dynamic model. The emergence of control flow constructs further complicates this problem as different execution paths can emit substantially different data. A fully static IR, hence, is inadequate to cope with the dynamic characteristics of these models.

- **A set of dynamic-oriented optimizations.** Existing deep learning compilers, e.g. TVM [8] and Glow [37], expect static input for each optimization. The memory size of each tensor is pre-allocated and their live cycles are determined using a dedicated optimization pass. They also ensure the homogeneous execution of the entire model because all kernels are executed on the same device with no data transfer between the host and device after a kernel is launched. However, these optimizations may completely break when dynamism appears. Now different execution path possibly requires different amount of memory and the sizes are not available before runtime. Certain simple IR nodes may also be introduced to help runtime type inference and memory allocation. The operations in these nodes are intrinsically more CPU friendly, which would lead to the serious performance problem if not placed on the correct device.

- **A symbolic kernel code generator.** Code generation (codegen) is responsible for generating high-performance executable kernels for operators. Recent research [4, 8, 9, 37, 51] has achieved impressive results in kernel performance with static shapes on multiple backends. Nonetheless, challenges in codegen with symbolic shapes remain unexplored. After applying the same set of loop optimization, kernels generated with symbolic shapes could still perform bad
after reviewing systems for dynamic deep learning models, workflow in multiple stages, with the missing parts to sup-

 Nimble are: enable us to only maintain one version of the execution logic, but focus more on the performance critical operator kernels. The kernels are highly-optimized for a specific hardware platform to achieve high performance.

To effectively support dynamic models without performance degradation for static models, we introduced various analysis and optimization techniques in Nimble’s compiler. First, a set of IR extensions are devised to represent dynamic shapes (Any shape) and dynamic allocations for static optimization of dynamic program behaviors (Section 4.1). Second, shape functions are attached to operators to compute the output shapes dynamically and perform type checking at runtime (Section 4.2). Third, a memory planning optimization is employed to reduce amount of memory consumed (Section 4.3). Fourth, a heterogeneous device placement mechanism is designed to place IR nodes on “the-best” device to reduce expensive cross-device data transferring and synchronization (Section 4.4). Finally, the compiler features a code generator that is capable of specializing the code generation of certain likely shapes (Section 4.5). Once the executable with dynamic behavior is compiled, the VM-based runtime can load and interpret it with intelligent dynamic kernel dispatching (Section 5). We detail the design and implementation of each of these features in the followed sections.

3 System Overview

After reviewing systems for dynamic deep learning models, this section gives an overview of Nimble, a high-performance and flexible system for compiling and optimizing dynamic models for multiple platforms. In general, the design goals of Nimble are:

1. Supporting dynamic models. Nimble targets models with all types of dynamism, including control flow, dynamic data structures and varied data shapes.
2. Being portable and light-weight. The module that Nimble produces should be executable across a number of platforms on the cloud (high-end CPUs and GPUs) and at the edge (low-power CPUs and GPUs). The runtime should be light enough to run on devices with minimal compute power and memory capacity.
3. Enabling high performance. Nimble should be performant in the context of dynamism across platforms.

Figure 2 shows the system architecture of Nimble that we propose to achieve the aforementioned design goals. It is a system consisting of two major components, namely a compiler and a runtime. Nimble takes a model in the format of mainstream deep learning frameworks, converts it into a unified intermediate representation (IR), then optimizes and compiles the IR into an executable that contains both platform-agnostic bytecode and platform-dependent kernel code, and finally loads the executable to execute in the VM-based runtime. The bytecode is executed by Nimble’s runtime interpreter, which is shareable across various platforms. This design effectively enables us to only maintain one version of the execution logic, but focus more on the performance critical operator kernels. The kernels are highly-optimized for a specific hardware platform to achieve high performance.

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4 Compiler Support for Dynamism

A key challenge preventing existing deep learning compilers from handling dynamism is the lack of a uniform and dynamic representation. For example, optimizations and runtime of existing IR, e.g. TVM [8], assume the presence of static shape information in numerous places. These assumptions are present in many other so-called graph compilers and introduce quite a few challenges for optimization.

In order to handle dynamism, we design a set of IR extensions which expose the essential semantics required to optimize dynamic programs. The approach is implemented in Nimble on top of the Apache TVM (version 0.6) deep learning compiler infrastructure [8] to leverage its frontend converters from various DL frameworks to its IR. TVM’s frontends alleviate the need to frontend specific details enabling our work to focus on contributions such as IR extensions and optimizations. To use Nimble, one only needs to feed it with a pre-trained model, perform compilation and then inference. Furthermore, the lessons here are applicable to other compiler efforts such
as TensorFlow’s MLIR support or PyTorch’s TorchScript and TensorExpr (a Halide and TVM inspired DSL for kernel codegen) work. The below section describes how we transform standard TVM programs into our dynamic dialect which enables us to easily apply static optimizations to dynamic programs, much as we do in traditional compiler optimization.

In this section, we detail three key components required to compile dynamic models.

- An extended type system which enables statically tracking dynamic shapes.
- A series of optimization passes that make dynamic output shapes, allocation, and device placement explicit.
- A set of codegen techniques for producing code for kernels with dynamic input and output shapes.

### 4.1 Typing

Deep learning compilers use type systems to represent, check and infer the data types and shapes of tensors. In some frameworks and compilers this is separated into two steps, shape inference and data type inference. TVM [36] performs both simultaneously and refer to them as type inference, terminology we will use throughout the section.

A Tensor Type is designated by an n-dimensional shape (defined as a tuple of integers describing the tensor’s dimensions) and a data type (e.g. float32 or int64). Current deep learning IRs only support codegen when all dimensions of a tensor’s shape are known at compile-time. Static shapes are mandatory for type inference and checking in existing deep learning compilers.

In the context of dynamic models, many data shapes can only be determined at runtime. Therefore, the previous assumption of static data shapes does not hold. In order to support dynamic data shapes, Nimble introduces a special dimension called Any to represent statically unknown dimensions. For example, we can represent a tensor type as $\text{Tensor}[(5, 1), f32]$, where the size of the third dimension in this tensor is unknown while the other two dimensions have concrete values. This concept is relatively uncontroversial, and has been introduced in other frameworks. Janus [22] uses similar denotation to represent a dynamic dimension but only for type unification, while Nimble extends type inference to handle Any as described next. We do not support tensor types with dynamic ranks given the relatively limited use cases and optimization opportunities.

**Operator Type Relation** A type relation describes the relationship between the types of operator inputs and outputs. The type system of TVM’s Relay IR relies on these type relations to infer and bidirectionally propagate type and shape relationships between inputs and outputs of operators across the whole program. For example, the type relation for broadcasting operators (e.g. broadcast_add) performs the shape calculation following the NumPy broadcasting rules\(^1\).

The type relation must be generalized to properly handle dynamic shapes. For example, a program which grows a tensor on each loop iteration (a case existing in the decoder of many NLP models) is both impossible to type and compile without proper type system support. With the introduction of Any, we are able to improve the existing type relations to support dynamic models.

There are two cases that must be handled after we introduce Any to the type relations. First, operators such as arange\(^2\) and unique\(^3\) have dynamic output shapes depending on the input data, which will be described in Any. Second, when input shapes of a type relation contain Any dimension, the type relation needs to propagate Any correctly to the output types and relax typing constraints that hold in the static cases when necessary. For example, the rules for broadcast type relation given the matching dimension from two inputs when having Any are defined as follows:

\[
\begin{align*}
\text{broadcast}_{\text{rel}}(\text{Any}, 1) & \rightarrow \text{Any} \\
\text{broadcast}_{\text{rel}}(\text{Any}, d) & \rightarrow d \quad (d > 1) \\
\text{broadcast}_{\text{rel}}(\text{Any}, \text{Any}) & \rightarrow \text{Any}.
\end{align*}
\]

Note that due the presence of dynamic shapes these type relation rules can no longer rule out all type errors at compile-time. For example, for the second rule shown above, when Any is neither 1 nor d at runtime, it then violates the broadcast type constraints. To address this, we take the gradual typing [38] approach and leave certain type checking at runtime after Any is instantiated by a concrete value (see Section 4.2 for more details). One could eliminate these errors using a more advanced type system, but at increased complexity.

**Type Inference** One caveat of the Any dimension is that unknown dimensions will propagate during type inference, reducing chances for shape specialization. For example, if we use an operator such as arange to produce a tensor with dynamic shape (i.e., $\text{Tensor}([\text{Any}, f32])$) and later broadcast_add to a tensor with static shape (i.e., $\text{Tensor}([5, 1], f32)$), the output shape will also contain an Any dimension (i.e., $\text{Tensor}([5, \text{Any}], f32)$).

To limit the contamination of Any, we further introduce sub-shaping to improve the precision of types computed by type-inference. Much like sub-typing used in popular programming languages [5, 29], our extension enables values with more specific shape information to be passed in contexts which require less specific shapes. Further, we perform extra analysis on each Any dimension to detect if two Any dimensions point to an identically sized dimension. We can use this analysis in the downstream compilation to generate shape-specialized code during codegen.

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\(^1\)https://docs.scipy.org/doc/numpy/user/basics.broadcasting.html

\(^2\)arange generates a range of values in a (start, stop, step) interval the arrays output size is a function of input arguments.

\(^3\)unique selects the unique elements of a tensor.
4.2 Shape Function

The introduction of Any dimension invalidates the pre-allocation mechanism adopted in the existing deep learning compiler. Instead, we now have to track the amount of memory required to be allocated in parallel to computing. Furthermore, static type checking cannot eliminate all type errors at compile-time due to dynamic tensor shapes. Consequently, we define a shape function to compute the output shape for storage allocation and verify the type relation in accord with the semantics of every operators. The shape function is similar in structure to the type relations described in Section 4.1 but are present at runtime instead of compile-time. The shape function enables compiling and embedding the computation of output shapes into the program.

According to the characteristics of the operator, we divide the shape functions in three different modes: data independent, data dependent, and upper bound. Data independent shape functions are used for operators in which the output shape only depends on the shapes of inputs such as normal 2-D convolution. Data dependent shape functions require the concrete input values to compute the output shapes. For example, the output shape of arange depends on the value of start, stop, and step. In addition, there are certain operators such as Non Maximum Suppression (nms) where the complexity of computing the output shape is on par with the complexity of executing the operator itself. In order to avoid the redundant computation, we use an upper bound shape function to quickly estimate an upper bound shape for the output. We also require such operators to return the output shape along with output value, so as to use the real shape to slice the output tensors into precise output shape and layout.

It is worth noting that in the presence of dynamic shape functions, operator fusion needs to be specially taken care of. Operator fusion, which combines basic operators into a composite operator, is a critical technique for performance optimization as it reduces unnecessary memory copies and improves the cache locality. The compiler can easily connect the shape functions of basic operators to form the shape function for a composite operator when all shape functions are data independent. However, a basic operator with a data dependent or upper bound shape function cannot be fused to other operators, i.e., taking the outputs of other operators as its inputs to fuse together, as the shape function requires to access to the intermediate result within a composite operator. As a result, we explicitly define the fusion policy to prevent this from happening.

4.3 Memory Planning

Deep learning workloads are dominated by two key aspects, compute-intensive kernels and memory allocation. Many deep learning compilers use a form of static memory planning which tries to coalesce memory and minimize allocations. For devices such as GPUs these optimizations are essential for reducing memory fragmentation and ensuring allocation does not hamper kernel performance. Existing deep learning compiler IRs hide memory allocation behind a functional interface, where each operator implicitly allocates their output storage. Then before execution, the system performs static memory planning on the data-flow graph enabling efficient pre-allocation of the required memory. Due to this “out-of-band” nature of memory allocation, it is challenging to customize, modify or compose memory optimizations with other passes. For example, if one needs to adjust memory allocation for heterogeneous execution, modifications to the runtime are required.

Alternatively, some systems lower the entire program to low-level IRs such as LLVM [26] in order to perform optimizations. Due to the coarse-grained memory semantics of deep learning models, it is essential that memory optimizations occur at a suitably high-level of abstraction before essential program facts are lost. Moreover, as discussed in Section 4.2, we have introduced new ways to account for the handling of dynamic allocations, which further complicate memory analysis. In order to perform dynamic memory planning we have extended TVM’s Relay IR, using these extensions we translate a IR dialect where all memory allocations are implicit to one where buffers are allocated and passed around explicitly. The key to this transformation is an inter-procedural change of calling convention, with each operator now taking its outputs explicitly it is possible to track and transform allocations. In particular, we have introduced four new IR constructs, (a) invoke_mut(op, inputs, outputs) which takes outputs as mutable in-out arguments, (b) alloc_storage(size, alignment, device) which allocates a region of memory of a particular size, (c) alloc_tensor(storage, offset, shape, dtype, attrs) which allocates a tensor at a particular storage offset with a shape and data type, and (d) kill(tensor) which frees a tensor before its reference count becomes zero due to exiting the frame. Note that in the below code examples Tensor<d1, ..., dn> is shorthand for a tensor of shape (d1, ..., dn) containing floating point values.

We can demonstrate how to transform a single statically shaped operation such as broadcasting addition.

```cpp
1 fn main() -> Tensor<10> {  
2 let t1, t2 : Tensor<10> = ...;  
3 add(t1, t2)  
4 } 
```

Here we only must allocate a single buffer, the return buffer for the addition operation.

```cpp
1 fn main() -> Tensor<10> {  
2 let t1 = ...; let t2 = ...;  
3 let storage = alloc_storage(40, 64, cpu(0));  
4 let outl= alloc_tensor(storage, 0, (10), f32);  
5 invoke_mut(add, (t1, t2), (outl));  
6 outl
```
The above transformation replaces all operator invocations with a call to `invoke_mut` allocating storage for backing a single tensor from allocated at offset zero. The key insight is to internalize a notion of memory allocation into the IR, enabling static optimization of both static and dynamic allocations presence of control and dynamic shapes. We realize our shape functions as fragments of TVM’s tensor expression language which computes the output shape for a particular operator. As detailed in Section 4.2 our shape functions may require the input, the input shape, or both. Our uniform treatment of shape functions as standard tensor expressions enables them to be fused and optimized like normal, but one challenge is that we must now manifest allocations in a fixed point until we allocate for both the compute and necessary shape functions. We illustrate this below with a single dynamic concatenation.

```csharp
fn (x: Tensor< ?,2>, y: Tensor<1,2>) -> Tensor< ?,2> {
  let in_sh0 = shape_of(x);
  let in_sh1 = shape_of(y);
  let storage_0 = alloc_storage(16, 64, ...);
  let out_sh0 = alloc_tensor(storage_0, ...);
  invoke_shape_func(concat, (in_sh0, in_sh1), (out_sh0), ...);
  let storage_01 = alloc_storage(...);
  let out_0 = alloc_tensor(
    storage_01, shape_func_out_0, ...);
  invoke_mut(concat, (x, y), (out_0));
  out_0
}
```

This is the same transformation as the previous example with the addition of carefully inserting invocations to the shape function to compute output buffers sizes for the dynamically sized kernel.

```csharp
fn (x: Tensor< ?,2>, y: Tensor<1,2>) -> Tensor< ?,2> {
  let in_sh0 = shape_of(x);
  let in_sh1 = shape_of(y);
  let storage_0 = alloc_storage(16, 64, ...);
  let out_sh0 = alloc_tensor(storage_0, ...);
  invoke_shape_func(concat, (in_sh0, in_sh1), (out_sh0), ...);
  let storage_01 = alloc_storage(...);
  let out_0 = alloc_tensor(
    storage_01, shape_func_out_0, ...);
  invoke_mut(concat, (x, y), (out_0));
  out_0
}
```

After the transformation you may notice we have introduced calls to `shape_func` which invokes a shape function for a kernel. The shape function requires input shapes as arguments which further require us to invoke `shape_of` for both `x` and `y`. `shape_of` will be directly mapped to a VM instruction to retrieve the shape of a tensor at runtime. More description of it will be provided in Section 4.4.

Now that the all allocations are explicit in the IR we can provide analogous optimizations in the static case on dynamic programs, for example we have implemented a storage coalescing pass which groups storage into a larger region which we can then multiplex tensor allocations on to.

### 4.4 Heterogeneous Device Placement

As discussed in Section 4.2, shape functions are executed at runtime to calculate the output shape of an operator. These functions must execute on the CPU due to the host-interaction model of GPU like devices. In the case of heterogeneous execution (i.e., CPU and GPU) it is essential to carefully schedule the execution of shape functions and kernels as improper scheduling can be disastrous for performance. For instance, considerable overhead will occur if inputs to shape functions must be copied from GPU due to the cost of data transfers and synchronization. To minimize the performance penalty, we analyze the program allocations to place sub-expressions on the most suitable devices.

We introduce a unification based analysis for computing the correct device placement and allocation based on the previous scheduling of the compute kernels. The goal of our device analysis is assigning each IR node in a way that minimizes the number of cross-device copies. We introduce a concept of `DeviceDomain` to represent the domain of a device, including source and destination. Each expression in the IR defaults to the empty domain, meaning there are no constraints on its device placement. In addition, two new IR constructs are introduced to facilitate the heterogeneous execution of VM, namely `device_copy` and `shape_of`. The former performs a data transfer between different devices and is inserted when a cross-device data copy is mandatory. The latter is used to retrieve the shape of a tensor at runtime and is used to efficiently compute the input shapes for shape functions. Our analysis is formulated as a set of device placement rules which describe how device constraints flow, and then we use unification, a technique common in type inference and compilers in order to compute precise device placement.

- **shape_of.** Defaults to the CPU domain because we can access a Tensor’s shape regardless of which device it is placed on.
- **Shape functions.** These IRs take the output of one or multiple `shape_of` and then derive the shape of an operation according to predefined type inference rules. The output of a shape function is used to compute the amount of memory that this operator requires at runtime, which only needs a few cheap scalar arithmetic computation. Therefore, the inputs and outputs would be better on a CPU domain as well.
- **device_copy.** The input and output of this IR are on different domains as it copies data from one domain to another. The device domains of the input and output are propagated in the opposite directions to other IR nodes that are reachable to/from the device copy node.
- **Memory operations.** The device domain of storage from `alloc_storage` is designated in the expression, and later is propagated to the device domain of the tensors allocated from this storage via `alloc_tensor`.
- **invoke_mut.** All arguments used in the `invoke_mut` must have the same device domain.
- **Other common IR nodes.** The device domain of other common IR nodes, e.g. variables, constants, operators, etc., can be directly propagated from the above nodes.

Based on the rules defined above, we use a union-find data
structure to bidirectionally propagate and unify the device placement of each IR node. We introduce two operations, \textit{union}(s, t) and \textit{find}(s), to achieve \textit{DeviceDomain} unification throughout the entire program. \textit{union}(s, t) unisons the equivalence device domains of s and t into one equivalence domain when the device types match. \textit{find}(s) returns the representative of the device domain that s belongs to. These two operations are applied until all IR nodes are annotated. The result of the heterogeneous device placement composes with memory planning and shape function insertion resulting in correctly placed allocations.

4.5 Symbolic Codegen

Deep learning compilers [8, 35] have demonstrated competitive performance compared to manually tuned kernels on multiple platforms. Recent trends apply machine learning based search to further reduce or eliminate complex manual performance tuning, existing work applies both template based [9, 51] and beam search based [4] ones. However existing work which focuses on tuning in the presence of static shapes falls short with symbolic or dynamic shapes. There are two inherent challenges with regard to codegen with symbolic shapes.

- How to achieve the same performance of kernels generated with symbolic shapes as that with static shapes when applying the same schedule?
- How to extend the machine learning based approach to tune kernels with symbolic shapes?

Loop parallelism and loop tiling are common optimization techniques that exploit multi-core capabilities by achieving data access patterns which are memory hierarchy aware for both CPUs and GPUs. However, the combination of these techniques lead to complex loop boundary conditions. In many static cases, it is possible to prove these conditions always hold, and thus eliminate checks which hamper further optimizations such as unrolling. While straightforward to handle with static shapes, it becomes a non-trivial challenge when performing symbolic codegen. If not carefully handled, the boundary condition checks will stay, leading to poor performance.

To address this issue, we generate multiple kernels according to the residues modulo of the tiling factor and then dispatch based on the actual shape at runtime. For example, suppose a symbolic dimension \(x\) is divided by a factor of 8, we then duplicate the generated kernel for 8 times, and replace the symbolic \(x\) by \(8k + r\) in each copy, where \(k = \lceil x/8 \rceil\) and \(r \in [0, 7]\). By applying this technique in conjunction with an enhanced symbolic expression simplification pass, we can eliminate most boundary checks to achieve performance that is nearly identical to kernels compiled with a single static shape. Lastly, we automatically generate a dispatch function that invokes the corresponding kernel based on the residue. In addition, the dispatch function can be extended to invoke either compiler generated kernels or third party library whichever is faster from the profiling results. The increased kernel size is relatively small compared to the overall deep learning models. In extreme cases where resources are extremely limited, we can either generate fewer number of kernels than the tiling factor or reduce the tiling factor to find an acceptable trade-off between code size and performance.

A known issue to machine learning based tuning is that it may take a long time (usually hours) to find the best schedule for a single kernel. When it comes to symbolic shapes, the tuning time may be exponentially longer if we naively tune for every possible shape. In this paper, we extend the template based tuning approach for symbolic shapes in order to make tuning time tractable. The template based tuning approach takes a human-defined code template and a search space, and searches the best configure within the search space by using machine learning algorithms. We observe that a good configuration for one shape usually performs well on other shapes. Based on this observation, we devise the following mechanism to tune the kernel for symbolic shapes.

1. First replace the symbolic dimensions by a large enough value (e.g., 64) such that the search space can cover most possibilities, and run the tuning algorithm on the static shape for a sufficient number of iterations.
2. Pick top \(k\) configurations, apply them to a selection of other shapes, and evaluate their performance.
3. Pick the configuration that performs best on average among shapes previously evaluated.

We found that \(k = 100\) covers most of the best configurations for other shapes. Current popular dynamic models usually only require kernels with one symbolic variable. As a result, we choose the values of power of two up to 256 in the cross evaluation of other shapes. If there is more than one symbolic variable, a more sophisticated selection approach might be required to limit the evaluation time of step 2. We leave this to the future work. Further, if the workload distribution is known, we could adjust the weighting of known shapes when picking the best configuration for step 3.

Though we address both challenges, we admit that our approach has limitations when all dimensions are unknown. In these cases symbolic codegen cannot completely replace manually tuned 3rd party libraries yet, but is complimentary when partial shapes are known.

5 Virtual Machine

The conventional runtime of existing deep learning compilers which naively executes a model node by node in topological order does not work for executing the compiled modules of dynamic models. A more intelligent and powerful execute engine is required to handle the control flow execution logic, and dispatch different kernels accordingly. In order to achieve
these goals and be portable to different platforms, we design
and implement a virtual machine (VM)-based runtime.

In Nimble, we compile a dynamic model into a VM exec-
cutable that contains platform-independent bytecode and
platform-dependent kernel code, which can be later loaded
and executed. The bytecode consists of a series of instruc-
tions that predicate the order of kernel invocation and control
flow execution logic. This design compliments conventional
runtime’s capability for executing highly optimized kernels
but not directly handling orchestration between kernels.

5.1 VM ISA

The design of the VM instruction set is motivated by the
simple observation that kernel execution dominates neural
network execution time. If we treat kernel invocation as a
single instruction, the cost of surrounding instructions is neg-
ligible in the total execution.

As a result, our design is quite different from traditional
language virtual machines, which contain many instructions
that perform little work, leading to a profile where the cost
of each instruction executed matters. Our ISA is composed of
CISC-style instructions in which each instruction corresponds
to a primitive IR expression on tensors, such as allocation and
kernel invocation, which in turn may correspond to execut-
ing multiple “low-level” operations. For example, $\text{LoadConst}
idx$, $\text{reg}$ is capable of multiple addressing modes as it first
reads the index $idx$ and then loads the data from a constant
pool to the destination register $\text{reg}$. A complete list of in-
struction set can be found in the appendices. We naturally
select a register-based virtual machine design [12] for compa-
ct a bytecode, which is easy for users to read and modify.
We provide the abstraction of an infinite set of virtual regis-
ters as it significantly simplifies optimizations and allocation
(similar to SSA) and minimizes conceptual barriers to rapid
prototyping and modification.

Instructions are represented using a traditional tagged union
containing the op-code and the data payload. This representa-
tion enables both efficient serialization and instruction de-
coding and dispatch. Nimble uses variable-length instruction
format due to the inclusion of variable sized operands such as
data shapes in the instructions.

5.2 Interpreter

After we have generated a VM executable, we can create
an interpreter by loading the executable. When execution
begins, the interpreter runs a dispatch loop which checks the
op-code and executes the appropriate logic, then repeats. As
our instructions are coarse-grained (i.e. they can be viewed as
super-instructions), the number of branches generated by the
dispatch-loop is lower than traditional programming language
VMs, adding negligible overhead compared to ahead of time
compilation.

VM uses a tagged object representation reminiscent of
those used by programming languages such as Haskell, and
OCaml. The tagged object representation smoothly integrates
with various data structures, including tensors, algebraic data
types, and closures. Due to the specialized object representa-
tion, VM instructions only need to interact with the coarse-
grained data (i.e. tensors) requiring infrequent memory allo-
cation in chunks.

In sum, the interpreter handles instructions in the following
categories.

- Register-to-Register Operations. Register-to-Register op-
erations, e.g. $\text{Move}$, transfers data between different offset
of the register file. Objects are reference counted, make
use of copy-on-write and passed by reference ensuring reg-
erator operations are cheap even if the size of underlying
container is large.

- Memory Operations. Memory operations can allocate
space for tensors, load constant tensors, and so on. Due
the design of our constant pool, weights (which are con-
stant during inference) can remain in-memory with no spe-
cialized support they can be referenced by the $\text{LoadConst}$
instruction.

- Call Operations. Call operations are the most frequently
executed instructions. The ISA has specialized call instruc-
tions for invoking a global function, a kernel primitive,
closure, copying data across devices, reshaping runtime ten-
sors, and calculating the shape of tensors. Kernel primitives
are ahead-of-time compiled through and can leverage both
compiler-generated kernels and the third-party libraries.

- Control Flow Operations. Unconditional jump instruc-
tions, e.g. $\text{ret}$, are used by both static and dynamic models to
jump to a specific program point. Only dynamic models
need conditional control operations to determine the direc-
tion of branching. The interpreter updates the PC using the
offset from either the true branch or false branch based on
the conditional value.

5.3 Discussion

An alternative solution to the VM could be ahead of time
compilation from our abstract machine into machine code.
But due to the granularity of the operations, dispatch time
makes up a very small portion of the execution time. More im-
portantly, the VM provides flexibility traditionally attributed
to virtual machines and a clear compiler/runtime split. We
see the potential of VM to be integrated as a runtime module
into a larger system. For example, VM can provide resource
isolation where multiple inference instances share the same
hardware in the cloud. Furthermore, a Quality of Service
(QoS)-aware system, e.g., [25, 45], could leverage VM to
pause the current model execution for a higher priority or
time-critical model. Last, because of the simplicity of the VM
design, one can verify the implementation of VM for security
and privacy purposes.
6 Evaluation

This section evaluates the performance of Nimble on dynamic models against existing state-of-the-art solutions, as well as discussing the role of the optimizations performed by Nimble. Specifically, the section seeks to answer the following questions:

- What is the overall performance of Nimble for dynamic models when compared against state-of-the-art alternatives on various hardware platforms?
- How much overhead does Nimble VM introduce for handling dynamism at runtime?
- How effective are the proposed optimization techniques, such as memory planning and symbolic codegen?

6.1 Experiment setup

All experiments were conducted on Amazon EC2 instances. We evaluated Nimble on three hardware platforms: Intel Skylake CPUs (c5.9xlarge, 18 physical cores, hereinafter called Intel CPU), Nvidia Tesla T4 GPUs (g4dn.4xlarge, 1 card, 2,560 CUDA cores, hereinafter called Nvidia GPU), and ARM Cortex A72 (a1.4xlarge, 16 physical cores, hereinafter called ARM CPU). Although all tests are done on the cloud, our results of ARM CPU are portable to the edge devices, e.g. Raspberry Pi, due to the same architecture.

To study the efficiency of Nimble in handling dynamic models, we compared it with mainstream deep learning frameworks, including TensorFlow (v1.15), MXNet (v1.6), PyTorch (v1.5)\(^4\), as well as dynamic-specific systems TensorFlow Fold based on TensorFlow v1.0. We were unable to compare Nimble with Cavs [44], JANUS [22], or Jeong et al. [23] as none of them is open-source. No public deep learning compiler has claimed support for dynamic models.

Three popular models that represent different classes of dynamism were chosen in this experiment, viz. LSTM [18] (dynamic control flow), Tree-LSTM [42] (dynamic data structure), and BERT [13] (dynamic data shape). The input size / hidden size used in the LSTM and Tree-LSTM model are 300/512 and 300/150, respectively. We used BERT base implementation. For LSTM and BERT, we used Microsoft Research’s Paraphrase Corpus (MRPC) [14] with variable input lengths as our input dataset. For Tree-LSTM, we used the Stanford Sentiment Treebank (SST) [40] with various tree structures as the input dataset.

6.2 Overall performance

We compare the overall performance of Nimble against baselines for each dynamic models. Nimble successfully accomplished inference for all models on all platforms. However, not all baseline systems could perform inference for these models. For instance, TensorFlow Fold was not designed to process LSTM and BERT hence no result was obtainable, and Tree-LSTM only runs on PyTorch and TensorFlow Fold as other frameworks cannot handle dynamic data structures. Finally the model inference of Tree-LSTM on Nvidia GPU was omitted as it’s hard to saturate GPU compute capability due to too many control flows and its model size, making GPUs less favorable deployment targets.

The baseline systems all make use of third-party kernel libraries to achieve high-performance by leveraging the heavily hand-optimized operators. We observe that dynamic models are often well-optimized on a single platform but perform poorly in other frameworks or on other targets. However, Nimble has the ability to select either the self-compiled kernels or the ones provided by third-party library based on which one maximizes performance. It uses dynamic dispatch logic to invoke the selected kernels using platform-independent bytecode at runtime. This enables Nimble to deliver portable and consistent results as many compiler optimizations are platform agnostic.

First, the latency results of Nimble, MXNet, PyTorch, and TensorFlow on LSTM are shown in Table 1. Nimble consistently outperforms the baseline on both 1- and 2-layer cases. For example, it reduces the latency of 1-layer LSTM model inference by 1.7×, 4.5×, and 6.3× over PyTorch, MXNet, and Tensorflow on Intel CPU, and 1.2×, 1.5×, 3.3× on Nvidia GPU, respectively. On ARM CPU, Nimble decreases the latency numbers even more remarkably, i.e. 9.5× over PyTorch, 20.3× over MXNet, and 5.4× over TensorFlow, respectively. The similar trend applies to 2-layer case of the LSTM model. We observe that latency on Nvidia GPU is higher than Intel CPU. This is because the size of LSTM model is relative small so that it cannot fully utilize the massive parallelism in the GPU. The significant performance improvement is due to Nimble encoding the control flow into platform-independent instructions that have minimal overhead while deep learning frameworks use control flow specific primitives to process the sequence, which introduces a large performance penalty.

Next, we inspect the performance of model inference on Tree-LSTM as exhibited in Table 2 by comparing Nimble with PyTorch and TensorFlow Fold. The table shows that Nimble runs substantially faster than the baselines. On PyTorch, the

| Unit: µs/token | 1 layer | 2 layers |
|---------------|--------|---------|
|              | Intel  | NV      | ARM     |
|              | Intel  | NV      | ARM     |
| Nimble        | 47.8   | 93.0    | 182.2   |
| PT            | 79.3   | 110.3   | 1729.5  |
| MX            | 212.9  | 135.7   | 3695.9  |
| TF            | 310.4  | 304.7   | 978.3   |

Table 1: LSTM model inference latency of Nimble, PyTorch (PT), MXNet (MX), and TensorFlow (TF) on Intel CPU, Nvidia (NV) GPU, and ARM CPU.

\(^4\)We use PyTorch v1.4 on ARM CPU because PyTorch v1.5 fails to build on ARM instance.
Table 2: Tree-LSTM model inference latency on Intel CPU and ARM CPU. TensorFlow Fold was not built successfully on ARM CPU.

| Device | TVM lat. (ms) | Nimble lat. (ms) | kernel lat. (ms) | others (ms) |
|--------|---------------|------------------|------------------|-------------|
| Intel  | 19.38         | 24.32            | 21.06            | 3.26        |
| ARM    | 223.50        | 237.41           | 228.59           | 8.82        |
| Nvidia | 5.58          | 5.86             | 5.60             | 0.26        |

Table 3: BERT model inference latency on Intel CPU, Nvidia GPU, and ARM CPU.

| Unit: µs/token | Intel | Nvidia | ARM  |
|----------------|-------|--------|------|
| Nimble         | 40.3  | 86.3   |      |
| PyTorch        | 701.6 | 1717.1 |      |
| TF Fold        | 209.9 |       | –    |

Table 4: BERT model latency (sequence length 128) using TVM and Nimble on different hardware. `kernel latency` shows the latency of kernel invocation in Nimble, and `others` shows the extra latency introduced by other instructions.

Performance speedups are 17.4× on Intel CPU and 19.8× on ARM CPU as PyTorch uses Python to handle the tree data structure. TensorFlow Fold is 5.2× slower than Nimble on Intel CPU because it has to re-compile upon every input.

Third, Table 3 summarizes the performance of BERT for Nimble, MXNet, and TensorFlow. The results indicate that Nimble outstrips the baselines for all frameworks on all platforms in the experiment. The reduction in latency compared to the best framework on each platform is 1.5×, 1.05×, and 1.3× on Intel CPU, ARM CPU, and Nvidia GPU, respectively. The reasons are two-fold: (a) similar to frameworks, Nimble is also able to use the well-tuned third-party libraries on Intel CPU (MKL) and Nvidia GPU (cuDNN). (b) Nimble can further enjoy the benefit of powerful operator fusion brought by the deep learning compiler. One can observe that we obtained more speedups on the ARM CPU for PyTorch and MXNet as the third-party libraries performed less favorable. However, Nimble is only slightly faster than TensorFlow on the ARM CPU. This is because the dense operators (contributing to more than 90% of the overall latency in BERT) on the ARM CPU was not well optimized by the underlying compiler. Therefore, the performance of the combination of operators it selected is on par with the ones used by TensorFlow.

In sum, the evaluation results demonstrate that Nimble produces more portable performance for all dynamic models on different platforms. Instead, the performance of frameworks is more platform dependent and varies from model to model.

6.3 Microbenchmark

This section analyzes the performance gain of Nimble by using BERT as the microbenchmark. Three studies will be conducted to examine (a) the overhead introduced by the VM, (b) the advantage of the proposed memory planning pass, and (c) the performance discrepancy between symbolic and static codegen.

**Overhead in handling dynamism** In order to understand the overhead that Nimble spends to take care of dynamism, we compared it to TVM where static sequence length and TVM static runtime is used to execute BERT. Table 4 details the performance difference between Nimble and TVM. TVM is 5% to 25% faster than Nimble on static shapes, though the absolute latency difference is small. The overhead comes from two aspects: (a) kernels generated with symbolic shapes cause extra overhead in the index computation. (b) other instructions in the virtual machine are required to handle the dynamic execution, such as shape functions, dynamic memory allocation, instruction dispatch, etc. On Nvidia GPU, most of bytecode latency is overlapped with the GPU execution thanks to heterogeneous device placement (Section 4.4), and therefore the overhead of other instructions is negligible.

**Memory planning** Section 4.3 proposed memory planning to coalesce memory allocation together and reuse the already allocated memory chunks. Thanks to this pass, we are able to reduce the number of buffer allocation by 47%, and the memory allocation latency is reduced by 75% from 2.0 ms to 0.5 ms on Intel CPU. We also compared the memory usage of Nimble with memory planning to TVM which statically

Figure 3: Relative latency comparison between symbolic codegen and static codegen of 3 dense operators on ARM CPU. The latency of kernel compiled with static shapes is used as the baseline. “dispatch/k” indicates that we generate k symbolic kernels to be dispatched at runtime. “no dispatch” means that only one symbolic kernel is generated and therefore no dispatching is needed.
analyze and pre-allocate memory on popular computer vision models such as ResNet [17], MobileNet [19], VGG [39] and SqueezeNet [20]. It turned out that Nimble leads up to 8% more memory footprint.

**Symbolic codegen** We selected 3 dense operators in the BERT model and compared the performance of symbolic codegen against static codegen on ARM CPU. Figure 3 illustrates the relative latency of kernels generated with symbolic shapes to the baseline – kernel compiled with static shapes. The auto-tuning algorithm chooses to tile the symbolic dimension corresponding to the dynamic sequence length by a factor of 8 in all three kernels. We varied the number of generated kernels to be dispatched during the symbolic codegen from 8 (full dispatch) to 1 (no dispatch) as described in Section 4.5. We observe that symbolic codegen with full dispatch can achieve nearly identical performance as that for static shapes. While reducing the number of kernels, latency increases up to 42%, 104%, and 45% for these 3 layers, respectively. We observe similar trends in dense operators with different shapes, other operators, and other platforms as well.

7 Related Work

Systems for machine learning is an active research area with a variety of techniques for ML inference engines which support dynamic features, cross-platform execution, and per-platform code generation. We discuss related work below.

**Deep learning frameworks** As a framework, TensorFlow [3] supports dynamism via the addition of control flow primitives such as switch and merge in its graph representation [47]. Similarly, MXNet [7,50] uses operators such as foreach, cond, and while_loop to support control flow. The main drawback of this approach is requiring a runtime that uses an inefficient and complex control flow encoding such as TensorFlow, or a hybrid runtime such as MxNet which is inflexible for deploying to edge devices. As a separate effort, TensorFlow Fold [31] adds front-end syntactic sugar to TensorFlow for simplifying dynamic models via dynamic batching. Specifically, TensorFlow Fold conducts an analysis of the user’s provided computation graphs and identifies dynamic operations that can be batched together. Once such operations are found, it transforms them into an intermediate representation (IR) that can be ingested by TensorFlow for evaluation. The nature of this approach can introduce large overhead as each path must be executed as a different sub-computation graph, as well as limiting further optimization.

Dynet [33] and PyTorch [34] use host language features to dynamically (i.e., Python’s control flow) to construct a dynamic model architecture. This allows a friendly and flexible programming model. However, it requires the creation of new static data flow graph for each path through the program introducing control flow overhead, and limiting the scope of optimization to a single trace through the program, a trace which often only executed once [44]. These challenges were similarly faced by tracing-JIT based systems in the JIT compiler literature. JAX [6] also supports both control flow and dynamic features in its programming model, but is fundamentally limited by the ability for XLA, TensorFlow’s deep learning compiler to optimize and compile dynamic code. To the best of our knowledge XLA still requires all loop nests to be static at code generation time.

Jeong et al. [23] and JANUS [22] both extend TensorFlow to improve the performance for dynamic models. Jeong et al. [23] introduces the recursive data structure in the programming model to replace the control flow primitives in the tree-like models. The solution is hard to generalize to other dynamic models though. JANUS [22] optimizes the dynamic model execution in TensorFlow via speculative execution. However, the conversion from imperative programs in Python to symbolic data graph in TensorFlow is incomplete due to dynamic typing, control flow, etc. Therefore, JANUS suffers the performance loss when it falls back to imperative execution. In addition, both work share the limitation in portability with the underlying framework.

Deep learning frameworks rely on third-party libraries to implement operators with different data shapes, namely, they achieve good performance for models with dynamic shapes on a specific hardware platform only if the corresponding high-performance third-party library is both used and supports an operation. Therefore, frameworks generally perform poorly on devices, such as ARM CPU, which are not in the first tier of device support such as Google’s TPU or Nvidia GPU in TensorFlow.

**Runtime systems** To address frameworks’ challenges with dynamism, e.g. prohibitively high overhead in reconstruction of computation graphs and difficulties in batching together computations with similar input shapes recent works has proposed deep learning runtime systems [15, 44]. These techniques exhibited effectiveness in improving the performance of dynamic models. However, these approaches suffer from a common limitation—they all heavily rely on the third party libraries, such as cuDNN [10] and MKL-DNN [21], raising concerns about portability. In addition, they usually only support a narrow subset of dynamic models on each platform.

**Deep learning compilers** Unlike the deep learning frameworks, Nimble is designed as an end-to-end deep learning compiler. The existing deep learning compilers, including XLA [43], TVM [8], and Glow [37], offer a means to compile deep learning models to run on multiple hardware platforms, but only focus on static models and fail to support models with dynamism. MLIR [27] provides compiler infrastructure for deep learning workloads which allows developers to implement new dialects and combine them into a sing application. Its graph-level dialect has the support for dynamism, but has not yet produced work demonstrating how to achieve good performance in dynamic scenarios. Nimble enables a deep learning compiler to support dynamism in an efficient and flexible way by adding a dynamic type system, a dynamic
code generator, a VM-based runtime and a series of dynamic-specific optimizations.

Nimble’s compilation and VM design is largely inspired by production compilers and VMs, such as LLVM [26], GCC [2], and JVM [1]. These generic solutions are able to easily handle dynamic behaviors, such as control flow and variable-length input arrays. However, the design of these compilers are heavily tailored to the optimization and execution profile of traditional programs. These programs manipulate small scalar values and consist of a large number of low level instructions. These VMs have a large number of instructions, which requires instruction execution and dispatch to be extremely efficient. Instead, deep learning compilers like Nimble manipulate primarily tensor values using a relatively small number of coarse-grained instructions, i.e. 16 instructions are sufficient for the Nimble VM. The execution hotspots of DL workloads are the compute-intensive operators (i.e. convolution) over large tensors. Thus, the micro-optimization of VM instruction dispatch is not essential to overall performance.

8 Conclusion

This paper proposed Nimble, an end-to-end compiler and runtime solution to dynamic deep learning models. Nimble is the first deep learning compiler that supports neural networks with dynamism, via a lightweight and portable VM-based runtime for executing compiled models on multiple platforms. We demonstrated a series of IR extensions and optimizations used to notably boost performance for dynamic models. Experimental results showed that Nimble efficiently executed popular dynamic models on multiple platforms with up to 20× speedup compared to the state-of-the-art solutions used in deep learning frameworks and runtime systems. Future work includes enabling dynamic model inference to run on emerging hardware platforms such as AI accelerators and in high-performance training of dynamic models.

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| Instruction       | Description                                                                 |
|------------------|-----------------------------------------------------------------------------|
| Move             | Moves data from one register to another.                                    |
| Ret              | Returns the object in the result register to the caller’s register.         |
| Invoke           | Invokes a function.                                                         |
| InvokeClosure    | Invokes a closure.                                                          |
| InvokePacked     | Invokes an optimized operator kernel.                                       |
| AllocStorage     | Allocates a storage block on a specified device.                           |
| AllocTensor      | Allocates a tensor object with a static shape from a storage.              |
| AllocTensorReg   | Allocates a tensor object given the shape in a register.                    |
| AllocADT         | Allocates a data type using the entries from a register.                   |
| AllocClosure     | Allocates a closure with a lowered virtual machine function.               |
| GetField         | Gets the value at a certain index from a VM object.                         |
| GetTag           | Gets the tag of an Algebraic Data Types (ADT) constructor.                  |
| If               | Jumps to the true or false offset depending on the condition.               |
| Goto             | Unconditionally jumps to an offset.                                         |
| LoadConst        | Loads a constant at an index from the constant pool.                        |
| LoadConsti       | Loads a constant immediate.                                                 |
| DeviceCopy       | Copies a chunk of data from one device to another.                          |
| ShapeOf          | Retrieves the shape of a tensor.                                            |
| ReshapeTensor    | Assigns a new shape to a tensor without altering its data.                  |
| Fatal            | Raises fatal in the VM.                                                     |

Table A.1: The opcode and the description of Nimble’s instruction set.

Appendices

A VM ISA

The appendix describes the complete list of instruction set in the Nimble VM. Table A.1 details the opcode and the functionality of each instruction. Recall that Nimble is designed to support neural networks with dynamic features, such as control flow and dynamic data structures etc., in a portable, high-performance, and light-weight manner. A set of instructions are proposed to fulfill this task. These instructions provide not only high-level information about the dynamic model behavior but also an architectural level interface for better orchestration and virtualization of the execution of control logic and optimized operator kernels.

Among these instructions, Ret, If, Goto, Invoke, and InvokeClosure are designed for control flow, i.e., the conditional and unconditional branches caused by if-then-else, function calls, and closure invocation. AllocADT and GetTag enable the support of dynamic data structures.

InvokePacked is the most performance-critical one. It is in charge of invoking the operator kernels that are optimized either by the underlying deep learning compiler or a third-party library.

To ease compiler optimizations (e.g. memory planning and device placement) and code generation, we offer the native support of several instructions in the VM, namely ShapeOf, DeviceCopy, and ReshapeTensor. These three instructions are used to directly manipulate runtime data, such as extracting the shape of a tensor, moving data between different devices, and transforming the shape of a tensor. With the help of them, we could preserve more coarse-grained IR at the frontend making optimization simpler.

The current instruction set only contains 20 instructions for dynamic model inference. It largely reduces the dispatching overhead and simplifies bytecode serialization and deserialization.