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Thomas Gerrer, a) Heiko Czap, Thomas Maier, Fouad Benkhelifa, Stefan Müller, Christoph E. Nebel, Patrick Waltereit, Rüdiger Quay, and Volker Cimalla

AFFILIATIONS
Fraunhofer Institute for Applied Solid State Physics, Tullastrasse 72, 79108 Freiburg, Germany

a)thomas.gerrer@iaf.fraunhofer.de

ABSTRACT

The integration of AlGaN/GaN thin film transistors onto diamond substrates enables the efficient dissipation of device heat, thus providing a boost in performance and reliability of current high-frequency GaN power amplifiers. In this paper, we show 3 GHz load-pull measurements of GaN transistors on silicon (Si) and single crystalline diamond (SCD) as fabricated by our recently presented direct low-temperature bond process. After the transfer onto SCD, the efficiency and output power are increased by 15%, which is explained by a calculated temperature difference of ∼100 K. In addition, the temperature between individual gate fingers is reduced such that the output power density ($P_{out}$) is independent of the amount of fingers. A drawback of our GaN epilayer is identified in the huge thermal resistance of the buffer layer so that the heat spreading performance of our technology is significantly impaired. Nevertheless, we demonstrate a large GaN-on-diamond output power of 14.4 W at a $P_{out}$ of 8.0 W/mm.

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Gallium nitride (GaN) heterostructure transistors have emerged as one of the most promising technologies for high-power high-frequency microwave amplifiers. The concept of a highly conductive two-dimensional electron channel within an otherwise insulating wide-bandgap semiconductor enables the fast transport and control of large electrical power. The device material is typically grown as a thin epitaxial film on silicon carbide (SiC), Si, or sapphire. Between the thin film and the substrate, a buffer layer is introduced, which reduces crystalline defects, improves the electrical isolation, and mitigates thermomechanical stress. However, since both the buffer layer and the substrate material limit the GaN device performance, several ways are investigated to release the thin film after the growth and transfer it onto a different substrate.

Such transfer technologies enable a greater freedom for the design and fabrication of GaN devices. After the release of the thin film from the substrate, the buffer layer can be removed so that the thin film features greatly improve electrical and thermal properties. In addition, the substrate can be chosen with perfect electrical, thermal, optical, acoustic, and mechanical characteristics for the final application. For microwave amplifiers, the potentially best substrate is diamond. The good electrical isolation of diamond minimizes high-frequency electrical losses, and its outstanding thermal conductivity enables an efficient spreading of heat, generated locally within the GaN device channel.

In our previous publication, we presented a direct low-temperature bond technology to fabricate GaN-on-diamond transistors by the hydrothermal conversion of a thin water film into a 30 nm thick, electrically isolating bond layer. Our bond process is based on the dissolution of AlN and the crystallization of aluminum hydroxides. The aluminum hydroxides fill intermediate voids as present between the bond interfaces and sustain a good mechanical and thermal contact to almost any substrate material. At present, AlGaN/GaN heterostructures and thereof fabricated devices were bonded onto various materials such as glass, SiC, sapphire, and polycrystalline/ single crystalline diamond (SCD). In this paper, we present detailed electrical measurements and thermal
simulations of RF transistors (3 GHz), which were transferred from Si onto SCD substrates.

The AlGaN/GaN heterostructures were grown by metal-organic chemical vapor deposition on Si substrates. Figure 1 shows the scanning electron microscopy (SEM) image of the thin film between the Si substrate and the top metallization of the transistor. The inset in Fig. 1 shows the 2 μm buffer layer, which consists of an Al-Ga-N superlattice (SL) with a 25 nm period. The overlying GaN channel layer has a thickness of ~0.8 μm. In our GaN-on-diamond process, 12 × 12 mm² GaN-on-Si chips with processed devices were separated from the Si substrate and bonded onto 9 mm diameter SCD substrates. This process was described in Ref. 7.

Figure 2 shows the two different transistors, which were characterized by 3 GHz load-pull measurements and thermal simulations. In Figs. 2(a) and 2(c), these transistors are processed on the Si growth substrate, and in Figs. 2(b) and 2(d), they are bonded onto SCD. Both transistor types have a similar design with a single gate-connected field plate, a gate length of 0.5 μm, a gate width of 300 μm, and a gate pitch of 60 μm. The main difference between these two transistors is the amount of gate fingers, i.e., two fingers in Figs. 2(a) and 2(b) and six fingers in Figs. 2(c) and 2(d).

The primary goal of our electrical characterization was the comparison of the transistor performance before and after the transfer onto SCD as well as the maximum $P_{\text{out}}$ of our transistors on SCD. To compare the two different substrate technologies, the smaller transistors in Figs. 2(a) and 2(b) were measured at equal bias conditions of 50 V. The larger transistor was only measured on SCD [see Fig. 2(d)] to quantify the influence of thermal cross talk between single device fingers.

Figure 3 shows the efficiency (PAE) and $P_{\text{out}}$ for the $2 \times 300 \mu m$ transistor on Si (red) and SCD (black), extracted from the 3 GHz simulations of RF transistors (3 GHz), which were transferred from Si onto SCD substrates.

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load-pull measurements at 50 V bias. The transistors were biased in continuous wave (cw) operation. Each measurement point marks a specific load impedance and input power presented to the transistor. On SCD, the maximum $P_{\text{out}}$ and PAE are significantly increased. At an equal $P_{\text{out}}$ of 6.8 W/mm, the PAE increased by 14%, i.e., from 51% (Si) to 58% (SCD), and the maximum $P_{\text{out}}$ increased by 15%, i.e., from 6.8 W/mm (Si) to 7.8 W/mm (SCD).

Following the measurement at 50 V bias, the transistor on SCD was operated in 10 μs pulses. In this short measurement, self-heating is less pronounced such that any device failure is primarily explained by an electrical breakdown. Table I lists the complete measurement sequence for the 2 × 300 μm transistor on SCD until its failure at 70 V bias. At 50 V bias, the maximum $P_{\text{out}}$ is 8.6 W/mm, which is 10% larger than in cw-operation. This difference could be associated with the smaller temperature rise in the pulsed measurement. At 60 V bias, $P_{\text{out}}$ increased to 9.6 W/mm, which, as compared to the 50 V pulsed measurement, is a 12% increase in $P_{\text{out}}$. At 70 V and $P_{\text{out}}$ of 10 W/mm, the transistor was destroyed before the end of the load-pull matching.

A simple estimation of the lateral electrical field within the channel at 70 V explains that the device failure was caused by an electrical breakdown. Under the assumption, that—within the phases of pinch-off—the 70 V is evenly dropped along a gate length of 500 nm, the average maximum field equals ~1.4 MV/cm, which is within the range of the GaN critical electric field strength of 3.3 MV/cm. In real devices, the electrical field is not homogeneously distributed along the gate but shows a strong peak at the gate-drain edge. The maximum field, therefore, is larger than the calculated average field strength of ~1.4 MV/cm. We, therefore, conclude that the device failure at 70 V was caused by an electrical breakdown and that—without self-heating—70 V represents the maximum bias voltage to be applied at these transistors.

Table II lists the measurement sequence of the 6 × 300 μm transistor on SCD. At every bias voltage, the transistor was first operated in the pulsed mode and subsequently in cw. The maximum continuous $P_{\text{out}}$ is 8.0 W/mm at a drain bias of 55 V. At a continuous operation at 60 V, the transistor was destroyed. In contrast to the 2 × 300 μm transistor, the 6 × 300 μm transistor failed already at 60 V so that the device failure could be explained by a locally combined effect involving high electric fields and a critical temperature increase. At 55 V, the total RF power is 14.4 W, which is the largest output power reported for GaN-on-diamond transistors.

### Table I. Measurement sequence (3 GHz) and performance metrics of the 2 × 300 μm AlGaN/GaN-SCD transistor. The bottom row shows the cw performance at 50 V bias for this transistor on Si.

| No. of measurement | Mode | $V_{DS}$ (V) | $P_{\text{out}}$ (W/mm) | $P_{\text{tot}}$ (W) | PAE (%) |
|--------------------|------|-------------|-------------------------|-------------------|---------|
| 1                  | cw   | 50          | 7.8                     | 4.7               | 55      |
| 2                  | 10 μs| 50          | 8.6                     | 5.2               | 55      |
| 3                  | 10 μs| 60          | 9.6                     | 5.8               | 55      |
| 4                  | 10 μs| 70          | 10                      | 6.0               | 55      |
| On Si              | cw   | 50          | 6.8                     | 4.1               | 51      |

### Table II. Measurement sequence (3 GHz) and performance metrics of the 6 × 300 μm AlGaN/GaN-SCD transistor.

| No. of measurement | Mode | $V_{DS}$ (V) | $P_{\text{out}}$ (W/mm) | $P_{\text{tot}}$ (W) | PAE (%) |
|--------------------|------|-------------|-------------------------|-------------------|---------|
| 1                  | 10 μs| 50          | 8.2                     | 14.8              | 51      |
| 2                  | 50 μs| 50          | 7.7                     | 13.9              | 51      |
| 3                  | 10 μs| 55          | 8.8                     | 15.8              | 50      |
| 4                  | cw   | 55          | 8.0                     | 14.4              | 50      |
| 5                  | 60 μs| 9.2         | 16.6                    | 16.6              | 52      |
| 6                  | cw   | 60          | ...                     | ...               | ...     |

The larger 6 × 300 μm transistor showed a similar performance to the 2 × 300 μm transistor. At 50 V bias, the maximum $P_{\text{out}}$ is 7.7 W/mm in continuous and 8.2 W/mm in pulsed operation. Compared to the smaller transistor, $P_{\text{out}}$ decreased by 0.1 W/mm in the cw mode and 0.4 W/mm for the pulsed measurement. From these electrical measurements, we, therefore, conclude that the diamond substrate efficiently dissipates the heat across the full distance of 60 μm between individual gate fingers so that the device $P_{\text{out}}$ scales almost independently of the number of fingers. The small differences in $P_{\text{out}}$ and PAE could be explained by the larger transistor periphery, i.e., a larger gate capacitance in the 6 × 300 μm transistor.

So far, the electrical characterization showed an improved performance of our transistors on SCD as compared to Si. In addition, the performance was shown to be similar for a different amount of gate fingers, thus suggesting a good thermal dissipation on SCD. To connect these electrical results with temperature distributions in the device channel, we performed 3D thermal simulations.

The transistors were modeled with the finite element analysis software COMSOL Multiphysics as illustrated in Fig. 4(a) for one quarter of the 2 × 300 μm transistor. Figures 4(b) and 4(c) show the top and the side view onto the transistor channel. As depicted in Fig. 4(c), the device layer stack consisted of a 200 nm SiN passivation layer, an 800 nm GaN layer, a 2 μm SiL buffer, a 150 nm AlN nucleation layer, and the substrate. On top of the GaN layer, a planar heat source with a length of 500 nm and a width corresponding to the gate width of the transistor was implemented. The heat load was assumed to be constant and set to the measured $P_{\text{out}}$, which is justified for PAEs of ~50%, where the consumed DC power equals the generated RF output power.

Table III lists the material parameters used in our simulations. The thermal conductivity as function of the temperature $T$ was modeled as

$$\kappa(T) = \kappa_{300} \left( \frac{T}{300 \, K} \right)^{\alpha},$$

where $\alpha$ is the coefficient of the power law and $\kappa_{300}$ is the thermal conductivity at 300 K. The 0.8 μm GaN thin film was assumed with $\kappa_{\text{GaN}} = 185$ W m$^{-1}$ K$^{-1}$ and $\alpha_{\text{GaN}} = -1.42$ as measured for GaN layers grown on Si. The thermal resistance of the SL arises from the dominant interface scattering, i.e., the mismatch in spectral phonon densities between the alternating SL layers. The effective thermal conductivity of AlN/GaN SLs was measured by Koh et al. as
FIG. 4. Thermal simulation of the 2 × 300 μm transistors on Si at 50 V bias: (a) perspective view, (b) top view onto the channel, and (c) side view at the channel.

TABLE III. Material parameters used in our thermal simulations.

| Material | d (μm) | κ (W m⁻¹ K⁻¹) | α (-) | Reference |
|----------|--------|----------------|-------|-----------|
| GaN      | 0.8    | 185            | −1.42 | 8         |
| SL       | 2      | ~10            |       | 9         |
| AlN      | 0.15   | ~15            |       | 10        |
| Si       | 650    | 148            | −1.65 | 11        |
| SCD      | 300    | 2200           | −1.85 | 11        |
| SiC      | 300    | 380            | −1.4  | 12        |

≥10 W m⁻¹ K⁻¹ (≥10 to 40 nm period length) and by Bougher et al. as ~7 W m⁻¹ K⁻¹ (22 nm period length). For our SL with a period length of 25 nm we assume an approximated thermal conductivity of 10 W m⁻¹ K⁻¹. The boundary resistance between the bufferer layer and the substrate was modeled as a 150 nm thick boundary layer. The thickness was matched with the real thickness of the AlN nucleation layer. The thermal conductivity of this boundary layer was set to 15 W m⁻¹ K⁻¹, which results in an effective thermal boundary resistance of 10 m² K⁻¹ GW⁻¹. Such value was measured in our previous experiments for GaN Schottky diodes bonded onto SCD by the same bond technology.

Figure 5 shows the temperature distribution within the 2 × 300 μm transistor on Si (red) and SCD (black) with the heat loads set to 6.8 W/mm (on Si) and 7.8 W/mm (on SCD). In the lateral direction [cp. Fig. 5(a)], the temperature at the hotspot region is 341 °C on Si and 260 °C on SCD. This temperature difference of 80 K is caused by the bad thermal spreading performance of Si. At x = 0, in the middle between the two gate fingers, the temperature on Si reaches 108 °C, whereas on SCD, the temperature reduces to 46 °C. On SCD, the temperature between the fingers almost equals the 40 °C fixed at the bottom of the simulation domain, thus making both fingers thermally independent of each other.

Figure 5(b) shows the temperature distribution in the vertical distance from the hotspot region on Si (red) and SCD (black). In this plot direction, the relative contribution of the different materials to the overall thermal resistance is identified. On both substrates, the SL buffer generates the dominant temperature increase of 150 K, which is three times larger than the temperature rise within the GaN layer. The 650 μm Si substrate, despite being considerably thicker, increases the temperature by only 100 K, whereas the SCD substrate’s thermal resistance becomes negligible. Even though the

FIG. 5. Temperature distribution within the 2 × 300 μm transistor in (a) the x-direction and (b) the z-direction on Si (red) and SCD (black) at the respective power levels of 50 V bias.
absolute impact of the SL on the overall thermal resistance is similar, the relative impact is more critical on SCD, where the overall temperature without the insulating SL would be significantly reduced. However, despite this technological downside, there is still a temperature difference of ~100 K between the channel temperature on Si and SCD.

In our next simulation we compare the temperature evolution in the 6 × 300 μm GaN transistor on SCD, SiC and Si as a substrate. On SiC, a GaN epilayer of similar quality as on Si (and SCD) wouldn’t require the SL buffer layer. Therefore, the epilayer on SiC was changed to a 2 μm GaN layer (without SL buffer) to allow a realistic comparison between these technologies. A better performance on SiC as compared to SCD can be expected, if the impact of the SL buffer layer impedes the positive effect of the large thermal conductivity of the SCD substrate.

Figure 6 shows the simulated temperature distribution for each substrate [Si (red), SiC (green) and SCD (black)] at a heat load of 8.0 W/mm (measured at 55 V bias on SCD) in (a) lateral and (b) vertical direction from the channel. In Fig. 6(a) the temperature at the hotspot of the central device fingers is 527 °C (Si), 185 °C (SiC) and 273 °C (SCD). On Si, the hotspot temperature is 250 K higher than on SCD, which is associated with the small thermal conductivity of Si and the large thermal crosstalk temperature reaching 184 °C between the central device fingers. On SiC, however, the hotspot temperature is 100 K lower than on SCD. Therefore, the excellent thermal conductivity of SCD and the reduced thermal crosstalk of 49 °C (SCD) vs 86 °C (SiC) in the device center cannot compensate the large thermal resistance of the SL buffer layer.

The impact of the SL buffer layer is clarified in Fig. 6(b), which shows the thermal resistance contributions of the individual layers. On Si (red) and SCD (black), the SL buffer adds around 170–200 K to the overall temperature increase of the hotspot. On SiC, however, the temperature between the GaN layer and the substrate only increases by 15 K as caused by the 150 nm thick boundary layer with an effective thermal boundary resistance of 10 m² K⁻¹ GW⁻¹. We note, that the large thermal resistance of the SL is caused by the combination of its small thermal conductivity and its close proximity to the hotspot. The logarithmic plot in z-direction shows, that a 2 μm SL buffer would cause a much smaller temperature increase if present at a distance of 3–4 μm thus leaving opportunities to improve the thermal resistance of epilayers on Si.

The thermal simulations show, that the SCD substrate efficiently dissipates the heat for the designed gate pitch of 60 μm. Similarly to the 2 × 300 μm transistor on SCD, the temperature of 49 °C in the device center in Fig. 6(a) is close to the backside temperature of 40 °C, which demonstrates that the individual channel temperature of each finger is thermally independent. A drawback in our GaN technology on SCD is revealed in the 2 μm thick SL buffer layer. Compared to a similar technology for our 6 × 300 μm transistors on SiC, the hotspot temperature on SCD is ~100 K larger.

The improved electrical and thermal performance of our transistors after the bond process could be explained by an improved electrical isolation and/or the excellent thermal conductivity of diamond. In our devices, we assume a similar electrical isolation on both substrates as provided by the 2 μm thick SL buffer layer so that the improved performance can be explained by reduced temperatures in the device channel. Specifically, the combined electrical and thermal analysis showed that the ~15% increase in PAE and P_out after the transfer of the 2 × 300 μm transistor from Si onto SCD can be explained by a temperature difference of ~80–100 K between the device channels of the respective substrates. The influence of temperature on the electrical performance is explained by its impact on the electron density and velocity.

The electron density in AlGaN/GaN transistors is almost independent of temperature. These electrons are induced by the net piezoelectric polarization charges between AlGaN and GaN and the piezoelectric polarization caused by the pseudomorphic strain within the AlGaN layer. With the pyroelectric temperature coefficient being very small, the additional pyroelectric polarization for an increased temperature is negligible. Similarly, the piezoelectric polarization, as caused by an identical change in mechanical stress within the AlGaN and GaN, also has a small effect on the overall polarization at the interface due to the similar piezoelectric coefficients.

The main impact of temperature on electrical performance is associated with the reduced electron velocities within regions of low electrical field. The low-field mobility strongly depends on temperature such that a temperature rise of 100 K reduces the electron mobility by ~40–50%. In contrast, the high-field saturation velocity only drops by ~5–7% within the same temperature range. This large difference that temperature has on different
channel regions, where either one of these effects dominates the transport, complicates any electrothermal analysis. With this simplified understanding, we can only conclude that the improvement of our device performance by 15% is explained by a combined effect that temperature has on the low-field mobility and the saturation velocity.

The key question regarding GaN-on-diamond technologies is the potential performance benefit of utilizing diamond as a heat spreader. With current limitations regarding the fabrication thereof, the answer to this question would require a detailed self-consistent electrothermal simulation of RF device performance with high spatial and temporal resolution. Such calculations are computationally not accessible or include large uncertainties regarding the electrical and thermal properties of thin films and interlayers. However, with our bond technique, we present an elegant experimental means to study the impact of substrates onto complex device behavior. With our bond technology, we, therefore, see not only a chance to improve device performance but also to understand device characteristics related individually to the thin film and the substrate.

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