An analytic virtual-source-based current-voltage model for ultra-thin black phosphorus field-effect transistors

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In this paper, we develop an analytic physics-based model to describe current conduction in ultra-thin black phosphorus (BP) field-effect transistors (FETs). The model extends the concept of virtual source charge calculation to capture the effect of both hole and electron charges for ambipolar transport characteristics. The model comprehends the in-plane band-structure anisotropy in BP, as well as the asymmetry in electron and hole current conduction characteristics. The model also includes the effect of Schottky-type source/drain contact resistances, which are voltage-dependent and can significantly limit current conduction in the on-state in BP FETs. Model parameters are extracted using measured data of back-gated BP transistors with gate lengths of 1000 nm and 300 nm with BP thickness of 7.3 nm and 8.1 nm, and for the temperature range of 180 K to 298 K. Compared to previous BP models that are validated only for room-temperature and near-equilibrium bias conditions (low drain-source voltage), we demonstrate excellent agreement between the data and model over a broad range of bias and temperature values. The model is also validated against numerical TCAD data of top-gated BP transistors with a channel length of 300 nm. The model is implemented in Verilog-A and the capability of the model to handle both dc and transient circuit simulations is demonstrated using SPECTRE. The model not only provides a physical insight into technology-device interaction in BP transistors, but can also be used to design and optimize BP-based circuits using a standard hierarchical circuit simulator.

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I. INTRODUCTION

Over the past decade, two dimensional (2D) materials, including graphene,\textsuperscript{1,2} transition metal dichalcogenides (TMDC),\textsuperscript{3,4} silicene,\textsuperscript{6,7} and germanane,\textsuperscript{8} have emerged as promising candidates for future generations of nanoelectronic devices due to their excellent electrostatic integrity, vertical scalability, and electronic properties that are considerably different from those in their bulk parental materials.\textsuperscript{9–12} In graphene, carriers have a limited phase space for scattering, which can allow quasi-ballistic transport at room-temperature.\textsuperscript{12–14} Several high-frequency devices using graphene have been experimentally demonstrated such as radio-frequency FETs, optical modulators, and photo-detectors.\textsuperscript{9} However, the use of graphene in digital switching applications is challenging due to its low on-off current ratio, which results from its zero band gap.\textsuperscript{15} On the other hand, TMDC-based FETs, with the band gap in the range of (1−2) eV, possess high on-off current ratios;\textsuperscript{12} however, the carrier mobility in TMDCs is much lower than that in graphene.\textsuperscript{16}

More recently, black phosphorus (BP) has emerged as one of the most interesting 2D materials for high performance transistor applications.\textsuperscript{17,18} In its bulk form, BP exhibits a band gap \( \approx 0.3 \) eV, while in its monolayer form, the band gap increases to \( \approx 2 \) eV.\textsuperscript{9,18,19} Additionally, the hole mobility in BP is reported to be as high as 1000 cm\(^2\)/Vs at room-temperature.\textsuperscript{18,20} Because of its puckered crystal structure, there exists a significant difference in the effective mass of carriers along the zigzag and armchair directions, with the armchair direction featuring light mass of carriers.\textsuperscript{9,18,19,21} With its tunable band gap, band-structure anisotropy, and high carrier mobility, BP is an excellent material to implement digital transistors for both high-performance and low-power electronic applications.\textsuperscript{19,22}

To understand, design, and simulate electronic circuits built with BP transistors, a physics-based compact model of current conduction is needed.\textsuperscript{23} So far, only a few models that describe current conduction in BP transistors have been reported in the literature.\textsuperscript{24,25} Prior BP FET models are mainly suited for near-equilibrium transport conditions, i.e. when the drain-source bias, \( V_{ds} \), is comparable to the thermal voltage, \( \phi_t = k_B T/q \) (\( k_B \) is Boltzmann constant, \( T \) is the operating temperature, and \( q \) is the elementary charge). Moreover, these models also do not include the effect of interface traps and non-linear contact resistances, which are important to interpret experimental data. The 2D FET models reported elsewhere either introduce significant empiricism in their approach due to thermally activated and hopping-based transport\textsuperscript{26–28} or suffer from a limitation of not being able to
reproduce the ambipolar characteristics. For example, the current-voltage (I-V) model for short-channel 2D transistors presented in Ref. 29 focuses mainly on intrinsic current conduction, while extrinsic effects due to contacts and traps are not included. The drift-diffusive I-V model presented in Ref. 30 is based on the calculation of the surface potential throughout the channel. However, the desired error-tolerance in the calculation of the surface potential must be in the range of sub-nV, which makes this model susceptible to convergence issues. Additionally, the broad-bias validity of the model in Ref. 30 requires numerical integration, which increases the computational complexity of the proposed model. As such, the model fit to experimental data has been demonstrated only for a limited bias range (gate-source bias greater than -1.5 V for transfer characteristics and drain-source bias of -1.2 V for output characteristics). Models based on the Landauer transport theory have also been reported in the literature. In Ref. 24, a Schottky-barrier (SB) model to describe current conduction in off-state is developed. This model is extended in Ref. 25 to cover the on-state regime by including the channel transmission. However, this model is not suited for broad-bias circuit simulations as its validity is restricted to $V_{ds} \leq 10$ mV at 300 K. We also note that none of the existing compact models for BP transistors has been implemented in Verilog-A to enable device-circuit co-design and optimization.

In this paper, we present an analytic I-V model of BP transistors to capture the ambipolar nature of current conduction over a broad range of bias voltages and temperatures. This model is based on the calculation of channel charges at the virtual source and is an extension of the previously published ambipolar virtual-source model applicable for graphene FETs. This paper extends the model in Ref. 23 in the following key ways. First, the threshold voltage, $V_t$, for electron and hole conduction is redefined due to the FET structure under study. Second, to handle the nonlinear behavior of Schottky source/drain contacts, we develop a new contact resistance model. Third, the model is extended to capture the low-temperature behavior of BP FETs. The model is validated by applying it to study BP FETs with gate lengths of 1000 nm and 300 nm and with BP thickness of 7.3 nm and 8.1 nm. This model has been implemented in Verilog-A and is used to simulate the circuit behavior of BP-based inverters and ring oscillators.
II. MODEL DESCRIPTION

In transistors with ambipolar current conduction, the net drain-source current, $I_{ds}$, for a given device width, $W$, is given as\(^{23}\)

$$I_{ds} = I_{elec} + I_{hole},$$  \hspace{1cm} (1a)

$$I_{elec} = WQ_{x0,e}v_{x0,e}F_{sat,e},$$  \hspace{1cm} (1b)

$$I_{hole} = WQ_{x0,h}v_{x0,h}F_{sat,h}. \hspace{1cm} (1c)$$

Note all quantities calculated at the top-of-the-barrier or the virtual source (VS) are denoted with the subscript $x_0$. In the above equation, $Q_{x0,e}$ and $Q_{x0,h}$ are the electron and hole charges, respectively, at the VS point in the channel (see Section II A for details.) The velocities, $v_{x0,e}$ and $v_{x0,h}$, are the electron and hole saturation velocities, respectively. The functions, $F_{sat,e}$ and $F_{sat,h}$ empirically capture the transition between linear and saturation regimes for the electron and hole branches, respectively. Per this model, it is assumed that there exist two VS points at opposite ends in the channel for electrons and holes. Unlike graphene FETs in which electron and holes typically have similar mobilities and velocities, BP FETs feature different physical properties for electrons and holes. As a result of this difference, $v_{x0,e}$ ($F_{sat,e}$) and $v_{x0,h}$ ($F_{sat,h}$) are treated separately in this paper. Moreover, in current state-of-the-art technology, the carrier mean free paths in BP FETs are on the order of few 10’s of nanometers. Given that the devices under study have gate lengths on the order of several 100’s of nanometers, we expect transport to be collision dominated\(^{33}\). As such, the velocities in Eq. [1] are treated as saturation velocities, rather than as injection velocities in the quasi-ballistic transport. This modified interpretation of $v_{x0}$ is similar to that reported in Ref. [34] to handle transport in long-channel gallium nitride transistors using the VS model.

The empirical function $F_{sat,i}$ ($i = e/h$ for electrons/holes) is given as\(^{23}\)

$$F_{sat,i} = \frac{V_{dsi}/V_{dsat,i}}{\left(1 + (V_{dsi}/V_{dsat,i})^{\beta_i}\right)^{1/\beta_i}}. \hspace{1cm} (2)$$

In this function, $V_{dsi}$ is the intrinsic drain-source voltage drop in the channel, $\beta_i$ is an empirical parameter, typically in the range of 1.5 to 2.5, and is obtained upon calibration with experimental data, and $V_{dsat,i} = v_{x0,i}L/\mu_i$ is the drain-source voltage at which the
current conduction changes from linear to saturation regimes. Here, \( L \) is the channel length and \( \mu_i \) is the mobility of carriers. Details of mobility and its temperature dependence are presented in Section [III].

All quantities in Eq. (1) vary with \( V_{gsi} \) and \( V_{dsi} \), which are the intrinsic gate-source and drain-source voltages, respectively. Intrinsic voltages are given as:

\[
V_{gsi} = V_{gs} - (I_{elec}R_{elec} + I_{hole}R_{hole}), \tag{3a}
\]

\[
V_{dsi} = V_{ds} - 2 (I_{elec}R_{elec} + I_{hole}R_{hole}), \tag{3b}
\]

where \( V_{gs} \) and \( V_{ds} \) denote the external gate-source and drain-source voltage drops, respectively. Contact resistances corresponding to electron and hole branches are denoted as \( R_{elec} \) and \( R_{hole} \), respectively. Section [II B] presents the analytic model of contact resistances.

### A. Channel charge model

The analytic model of electron and hole charges in Eq. (1), adapted from Ref. 23, are reproduced here for completeness and to drive the discussion that follows.

\[
Q_{x_0e} = C_g n_e \phi_t \log \left( 1 + \exp \left( \frac{V_{gsi} - V_{te}}{n_e \phi_t} \right) \right), \tag{4a}
\]

\[
Q_{x_0h} = C_g n_h \phi_t \log \left( 1 + \exp \left( \frac{V_{dgi} + V_{th}}{n_h \phi_t} \right) \right), \tag{4b}
\]

where \( C_g \) is the gate-channel capacitance in strong inversion, \( V_{te} \) (\( V_{th} \)) is the threshold voltage of electron (hole) branch, \( n_e \) (\( n_h \)) is the non-ideality factor of the electron (hole) branch, \( V_{dgi} = V_{dsi} - V_{gsi} \). The gate-channel capacitance is \( C_g = \epsilon_{ox}/CET \), where \( \epsilon_{ox} \) is the oxide permittivity, and \( CET \) is the capacitance equivalent thickness of the oxide. For thick oxides, \( CET \) is approximately equal to the physical thickness of the oxide, \( t_{ox} \). The non-ideality factor incorporates the effect of punch-through (\( n_d \)) and is given as \( n_{e(h)} = n_{0_{e(h)}} + n_{d_{e(h)}} V_{dsi} \). Here, \( n_0 \) is the value of the non-ideality factor when \( V_{dsi} \to 0 \).

The threshold voltage of the electron and hole branches is given as

\[
V_{te} = V_{min0} + \Delta V_e - \alpha_e \phi_t FF_e, \tag{5a}
\]

\[
V_{th} = V_{min0} - \Delta V_h + \alpha_h \phi_t FF_h. \tag{5b}
\]

Here, \( V_{min0} \) corresponds to the ambipolar (minimum-conductivity) point at \( V_{ds} = 0 \) V, \( \Delta V \) approximates the effect of interface traps, and \( \alpha_e \) and \( \alpha_h \) are empirical fitting parameters.
The functions $FF_e$ and $FF_h$ are logistic functions that control the change in the threshold voltage between weak inversion and strong inversion regimes and are given as

\[
FF_e = \frac{1}{1 + \exp \left( \frac{V_{gsi} - \left( V_{te} - \frac{\alpha_e \phi_t}{2} \right)}{\alpha'_e \phi_t} \right)}, \tag{6a}
\]

\[
FF_h = \frac{1}{1 + \exp \left( \frac{V_{dgi} + \left( V_{th} + \frac{\alpha_h \phi_t}{2} \right)}{\alpha'_h \phi_t} \right)} \tag{6b}
\]

Here, $\alpha'_e$ and $\alpha'_h$ are introduced as additional fitting parameters to adjust the rate and smoothness of transition of the threshold voltage between its weak inversion and strong inversion limits. Typical values of $\alpha_e / \alpha_h$ and $\alpha'_e / \alpha'_h$ are in the range of 3-11, depending on the channel length and the type of carriers.

Unlike graphene FETs in which the ambipolar point voltage does not shift with $V_{\text{ds}}$, in BP FETs, the ambipolar point voltage shows strong dependence on $V_{\text{ds}}$. Additionally, the thickness of the BP flakes studied in this work is less than 10 nm, which results in a narrow band gap of BP and a significant carrier injection at the drain end. Therefore, the on-off current ratio decreases by over two orders of magnitude as $|V_{\text{ds}}|$ increases (see Section IV on Results). The dependence of $V_{\text{min0}}$ on $V_{\text{ds}}$ and the degradation in on-off current ratio with $V_{\text{ds}}$ can be captured using the following equation:

\[
\Delta V_{e(h)} = \Delta_{1e(h)} - \Delta_{2e(h)} V_{\text{dsi}} - \Delta_{3e(h)} V_{\text{dsi}}^2, \tag{7}
\]

where $\Delta_{1e(h)}$, $\Delta_{2e(h)}$, and $\Delta_{3e(h)}$ are extracted from experimental calibration. The threshold voltage model uses 11 parameters, out of which seven parameters: $V_{\text{min0}}$, $\Delta_{1e(h)}$, $\Delta_{2e(h)}$, and $\Delta_{3e(h)}$, can be extracted from the transfer curves by measuring the change in the threshold voltage with $V_{\text{dsi}}$ (see Appendix A for details.) The remainder four parameters: $\alpha_{e(h)}$, $\alpha'_{e(h)}$ are tweaked in the range around 3-11 to match the transition between the on and off characteristics of the transistor, as well as to adjust the smoothness of the device transconductance. The validation of the charge model and gate capacitance against numerical data is discussed in Appendix C.
B. Contact resistance

The parasitic resistances associated with source and drain contacts in BP FETs are bias-dependent, nonlinear resistances. This is because at the interface between the contact metal and the BP channel, a Schottky barrier is formed, which shows a strong bias dependence.\(^\text{38-40}\)

The current, \( I_{SB} \), through a Schottky barrier (SB) for a given voltage drop \( V_{SB} \) across it is given as\(^\text{38,41}\)

\[
I_{SB} = A_{\text{jun}} A_R T^2 \exp \left( -\frac{\phi_B}{\phi_t} \right) \left[ \exp \left( \frac{V_{SB}}{\eta_{SB} \phi_t} \right) - 1 \right],
\]

where \( A_{\text{jun}} \) is the effective junction area of the SB contact, \( A_R \) is the Richardson constant, and \( \phi_B \) is the SB height. For purely thermionic emission at the SB contact, the non-ideality factor \( \eta_{SB} = 1 \). For other types of current conduction, such as thermally assisted tunneling and Fowler–Nordheim tunneling, \( \eta_{SB} > 1 \). Other factors that may lead to \( \eta_{SB} > 1 \) include bias dependence and image force lowering of the SB height, generation and recombination of carriers at the SB contact, and in-homogeneity of the junction.\(^\text{41}\) Equation (8) shows that the SB current is exponentially dependent on the SB height and the voltage drop across the barrier. The analytic model of contact resistance developed here captures these key aspects of current conduction through an SB contact. Moreover, in back-gated BP FETs we study, the region underneath the contacts is intrinsically p-doped. The application of a large negative gate voltage increases the hole doping under the contacts, which leads to a narrower barrier for hole injection and reduces the contact resistance corresponding to the hole branch.

To fully understand the effect of SB contacts on current conduction, we focus on the various paths in Fig. 1 that the carriers, once injected from the contacts, can take through the BP channel. In this figure, solid and dashed lines represent the flow of electrons and holes, respectively, through the channel. Note that in the model, we call electrical source as the terminal with lower voltage and electrical drain the terminal with higher voltage.
FIG. 1. Possible carrier transport paths in the channel. Solid and dashed lines represent the flow of electrons and holes, respectively, through the channel. Note that the figure is not drawn to scale.

In Fig. 1 path 1 for electrons and path 2 for holes are transparent for all values of $V_{gs}$ when $V_{ds} > 0$. For $V_{ds} > 0$, $V_{gs} > 0$, and $V_{ds} < V_{gs}$, paths labeled as 3 and 4 are unavailable for electron conduction. Likewise for hole, paths labeled as 5 and 6 are cut-off. Hence, we can conclude that for $V_{ds} < V_{gs}$, the only way carriers can be transported between the contacts is through the paths labeled as 1 and 2 in Fig. 1. Results of this discussion are summarized in Table I.

TABLE I. Possibility of different carrier transport paths in a Schottky barrier back-gated MOS-FET for $V_{ds} > 0$, $V_{gs} > 0$ and $V_{ds} < V_{gs}$.

| Carrier | From   | To     | Path | Possibility |
|---------|--------|--------|------|-------------|
| Electron| Source | Drain  | 1    | ✓           |
| Electron| Source | Drain  | 3    | x           |
| Electron| Drain  | Source | 4    | x           |
| Hole    | Drain  | Source | 2    | ✓           |
| Hole    | Source | Drain  | 5    | x           |
| Hole    | Drain  | Source | 6    | x           |

Next, we consider the case when $V_{gs} < V_{ds}$, $V_{ds} > 0$, and $V_{gs} > 0$. In this case, in addition to paths labeled as 1 and 2 in Fig. 1 there exist path 3 for electron conduction and path 6 for hole conduction. Results are summarized in Table II.

An appropriate bias-dependent model of the SB contact resistance in BP FETs must comprehend the distinct behavior for $V_{gs} > V_{ds}$ and $V_{gs} < V_{ds}$ regimes of transport when $V_{ds} > 0$ and $V_{gs} > 0$. When $V_{ds} > 0$ and $V_{gs} < 0$ the possible carrier transport paths are the
TABLE II. Possibility of different carrier transport paths in a Schottky barrier back-gated MOS-FET for $V_{ds} > 0$, $V_{gs} > 0$, and $V_{ds} > V_{gs}$.

| Carrier | From   | To     | Path | Possibility |
|---------|--------|--------|------|-------------|
| Electron| Source | Drain  | 1    | ✓           |
| Electron| Source | Drain  | 3    | ✓           |
| Electron| Drain  | Source | 4    | X           |
| Hole    | Drain  | Source | 2    | ✓           |
| Hole    | Source | Drain  | 5    | X           |
| Hole    | Drain  | Source | 6    | ✓           |

same as the results of the Table [II]. Note that the bias dependence of SB contact resistance is exacerbated for hole conduction. This is because of the use of Ti as the metal contact in the experimental BP FET devices examined here. Compared to metals, such as Pd or Ni, Ti has a much lower work-function, which gives rise to a larger SB height and, therefore, large contact resistance values.\textsuperscript{11,12} Also, the effect of contact resistance corresponding to hole conduction becomes especially significant in short channel devices in which the contact resistance could easily dominate the total drain-source resistance, limiting the maximum available current through the device.\textsuperscript{43} Here, we assume that $R_{\text{elec}}$ is a bias-independent, linear resistance. This is justified because of the p-type background doping in the devices under study.

The hole branch contact resistance assuming both ohmic resistance and the formation of the SB barrier at the metal/BP interface is given as

\[
R_{\text{hole}} = R_{\text{ohmic,1}}FF_R + R_{\text{ohmic,2}}(1 - FF_R) + \left(R_{01}FF_R + R_{02}(1 - FF_R)\right) \exp \left(aV_{\text{gs}}\right), \quad (9)
\]

where $a = a_1FF_R + a_2(1 - FF_R)$.

In the above set of equations, we use the logistic function $FF_R$ to model the drain-bias dependence of various parameters. This function is similar to the $FF_e/FF_h$ logistic function used in Eq. (6) and is given as

\[
FF_R = \frac{1}{1 + \exp \left(\frac{-V_{\text{ds}} + V_0}{\gamma} \right)}, \quad (10)
\]
where $\gamma$ is used to adjust the sharpness of transition between two different bias regions, and $V_0$ is the drain-gate voltage at which additional paths for current conduction between the contacts are introduced (see Fig. [1] and the discussion.) This voltage is given as

$$V_0 = V_{01}FF_h + V_{02}(1 - FF_h), \quad (11)$$

where $V_{01}$ and $V_{02}$ are fitting parameters, and $FF_h$ is given in Eq. (6b). The model for $R_{\text{hole}}$ described here captures the exponential dependence on $V_{gsi}$ as expected for SB contacts. Moreover, the model can also explain the drain-bias dependence of the contact resistance, following the discussion pertinent to Fig. [1]. The contact resistance model introduces 10 parameters: $R_{\text{elec}}, R_{\text{ohmic,1}}, R_{\text{ohmic,2}}, R_{01}, R_{02}, V_{01}, V_{02}, \gamma, a_1, a_2$. The methodology to extract the contact resistance parameters from experimental data is presented in Appendix A.

III. EFFECT OF TEMPERATURE

The main model parameters that are affected by temperature include the mobility, saturation velocity, non-ideality factor, and threshold voltage. Below we discuss the models to capture the temperature dependence of the various parameters.

a. Mobility: Experimentally measured mobility of carriers in 2D materials is generally much lower than that predicted theoretically based on phonon-dominated collision. Mobility degradation in 2D materials results from defects and charged impurities at room temperature.\textsuperscript{44–47} Previous published works indicate that the mobility of carriers in BP follows a power law relationship with respect to temperature ($T$). That is, $\mu \propto T^{-\xi_\mu}$ for $T > 100$ K\textsuperscript{22,44,48,49} with $\xi_\mu$ typically in the range of -0.4 to 1.2 based on the type and concentration of carriers, BP crystal orientation, and the dielectric environment of the sample.\textsuperscript{44} In this paper, we use a constant carrier mobility model with temperature dependence given as

$$\mu_{c/h} = \mu_{298,c/h} \left(\frac{298}{T}\right)^{\xi_{\mu,c/h}}. \quad (12)$$

Here, $\mu_{298,c/h}$ is the value of the mobility of carriers at 298 K. As a result of the weakened polarization charge screening for oxides with a high dielectric constant, such as HfO$_2$, we expect the temperature dependence of mobility in BP devices under study to be weak.\textsuperscript{44} As such, $\xi_{\mu,c/h}$ is expected to be in the range of 0.01 to 0.3.

The effect of carrier concentration on mobility, as demonstrated in recent experimental work,\textsuperscript{50} is studied in Appendix B. However, for validation of the model against experimental
data, we consider a constant carrier mobility model as in the equation above. This allows us to restrict the number of model parameters without compromising the quality of the model fits while also providing reasonable estimates of extracted parameters (see Sec. IV on results.)

b. Saturation velocity: The saturation velocity of carriers in BP is expected to decrease with an increase in temperature due to enhanced phonon-dominated scatterings.[51] Here, we model \( v_{x0} \) of both electrons and holes using a linear equation in the range of 180 K to 298 K. This model is similar to that used previously.[51]

\[
v_{x0,e/h} = v_{x0,298,e/h} - \xi v_{e/h} (T - 298),
\]

(13)

where \( v_{x0,298,e/h} \) is the saturation velocity of carriers at 298 K, and \( \xi v_{e/h} \) is the temperature coefficient of saturation velocity. Typical value of \( \xi v \) is in the range of 50 to 100 m/sK.

c. Non-ideality factor: At low \( V_{ds} \), sub-threshold slope is modeled as \( SS = 2.3n\phi_t \) where \( n \) is the non-ideality factor defined previously as \( n = n_0 + n_d V_{dsi} \). Experimental results in Section IV indicate that for low-\( V_{ds} \), \( SS \) is linearly proportional to temperature,[18] implying that \( n_0 \) is independent of temperature. At high \( V_{ds} \), tunneling current through the drain contact dominates, and the dependence of \( SS \) on temperature becomes sub-linear. This behavior can be reproduced by considering a linear temperature variation in the punch-through factor, \( n_d \):

\[
n_{d,e/h} = n_{d,298,e/h} - \xi n_{d,e/h} (T - 298),
\]

(14)

where \( n_{d,298,e/h} \) is the value of punch-through factor at 298 K, and \( \xi n_{d,e/h} \) captures the temperature sensitivity of \( n_d \). Typical values of \( \xi n_{d,e/h} \) are in the range of 0.009 to 0.025 1/VK.

d. Threshold voltage: The temperature dependence of threshold voltage is introduced in the parameter \( \Delta_{1,e/h} \) used in Eq. (7) according to

\[
\Delta_{1,e/h} = \Delta_{1,298,e/h} - \xi \Delta_{1,e/h} (T - 298),
\]

(15)

\( \Delta_{1,298,e/h} \) is the value of the parameter at \( T = 298 \) K, and \( \xi \Delta_{1,e/h} \) captures the temperature dependence of \( \Delta_{1,e/h} \) and it is on the order of \( 10^{-3} \). The linear variation of \( \Delta_{1,e/h} \) with temperature reproduces experimental and numerical results accurately as discussed in Section IV.
IV. RESULTS

The analytic I-V model developed here has 39 parameters, out of which 20 (11) parameters correspond to hole (electron) conduction, and 8 parameters (4 parameters for each carrier type) model the temperature sensitivity of current conduction. These models can be obtained through a systematic experimental validation methodology as explained in Appendix A.

There are four datasets available from experimental measurements and numerical simulation using the TCAD simulation tool Sentaurus from Synopsys. The first two datasets correspond to the back-gated BP FETs with Schottky source/drain contacts which are fabricated at the University of Minnesota. In these two datasets, the BP flakes are exfoliated from the bulk crystal and transferred onto the local back gates. The gate dielectric is HfO$_2$ with a thickness of 15 nm, and the gate metal is Ti(10 nm)/Pd(40 nm). The source and drain contacts are Ti (10 nm)/Au (90 nm). The device is passivated using 20-30 nm of Al$_2$O$_3$ to protect BP from atmospheric degradation. Additional fabrication details are given in Ref. 18. The third and fourth dataset are obtained numerically by simulating top and back-gated BP FETs with Schottky source/drain contacts to show model validity for both FETs structures. Model parameters extracted for all datasets are listed in Tables III and IV.

For all datasets that are discussed in this section, we refer to the terminal that is grounded as the source terminal ($V_s = 0$ V) and the drain terminal is biased at negative voltages ($V_d < 0$ V). Note that this terminology of labeling the source/drain contacts is different from that followed conventionally, but it does not impact the interpretation of the model and the results. The implementation of the model in Verilog-A, SPICE circuit simulations, and Gummel symmetry test are presented in Appendix D.

A. Dataset 1

Dataset 1 corresponds to back-gated BP FETs with $L = 1$ µm, $W = 7.32$ µm, $t_{BP} = 7.3$ nm, $t_{ox} = 15$ nm, with rotational angle $42^\circ$ (rotational angle $0^\circ$ is defined along the zigzag direction and $90^\circ$ is along the armchair direction.) Model fits to experimental transfer curves ($I_{ds}$-$V_{gs}$) and transconductance ($g_m = \partial I_{ds}/\partial V_{gs}$) for a broad range of $V_{ds}$ values at 298 K are shown in Figs. 2 (a) and (b). Figures 2 (c) and (d) show the model fits to measured output curves ($I_{ds}$-$V_{ds}$) and output conductance ($g_d = \partial I_{ds}/\partial V_{ds}$) for a broad range of $V_{gs}$ values.
Dataset 1: $L = 1 \mu m$, $W = 7.32 \mu m$, $t_{BP} = 7.3 \text{ nm}$, $t_{ox} = 15 \text{ nm}$, with rotational angle $42^\circ$, and $T = 298 \text{ K}$.

FIG. 2. Model fit to the experimental dataset 1 at room temperature: (a) transfer characteristics ($I_{ds}$-$V_{gs}$), (b) transconductance ($g_m = \partial I_{ds}/\partial V_{gs}$), (c) output characteristics ($I_{ds}$-$V_{ds}$), and (d) output conductance ($g_d = \partial I_{ds}/\partial V_{ds}$). Solid lines are model fits, while symbols correspond to experimental data.

at 298 K. The model provides an excellent fit to the measured data and has the required smoothness of current derivatives as expected of compact models. The maximum output current in this dataset is less than 100 A/m obtained at $V_{gs} = V_{ds} = -2.5 \text{ V}$. Due to its limited on-current, the effect of contact resistance is not discernible. As such, we are able to fit measured data with negligible contact resistance. Neglecting the contact resistance also allows us to extract values of carrier mobility and velocity that are within the expected range for this set of BP FETs.

We further validate this dataset using the model at $T = 280 \text{ K}$, 240 K, 200 K, and 180 K. Results are shown in Fig. 3. For all temperatures considered here, the maximum measured
Dataset 1: $L = 1 \mu m$, $W = 7.32 \mu m$, $t_{BP} = 7.3 \text{ nm}$, $t_{ox} = 15 \text{ nm}$, with rotational angle 42° at different temperatures.

FIG. 3. Model fit to the experimental dataset 1 at $T = (a) 280 \text{ K}$, (b) 240 K, (c) 200 K, and (d) 180 K for $V_{ds} : -0.1, -0.2, -1, -1.5, -2, \text{ and } -2.5 \text{ V}$. Solid lines are model fits, while symbols correspond to experimental data.

Current stays under 100 A/m, which can be explained by neglecting the contact resistances. The slight increase in on-current with a reduction in temperature is due to the increase in carrier saturation velocity. The dependence of $SS$ on temperature for this dataset is examined in Fig. 4. This figure shows that at low $V_{ds}$, $SS$ decreases at lower temperature, while at high $V_{ds}$, $SS$ is nearly independent of temperature. Hence, the assumption that $n_0$ is independent of temperature and that $n_d$ varies linearly with temperature (Eq. (14)) is justified.
Dataset 1: \( L = 1 \ \mu m, \ W = 7.32 \ \mu m, \ t_{BP} = 7.3 \ \text{nm}, \ t_{ox} = 15 \ \text{nm}, \) with rotational angle 42°

![Image of transfer characteristics](image1)

FIG. 4. Experimental data for transfer characteristics \( (I_{ds}-V_{gs}) \) of dataset 1 for \( V_{ds} = -0.1, -2.5 \) V at different temperatures. Solid line, dotted line, dash-dot line, and dashed line correspond to the \( T = 298 \ \text{K}, \ 240 \ \text{K}, \ 200 \ \text{K}, \ \text{and} \ 140 \ \text{K}, \) respectively.

Dataset 2: \( L = 0.3 \ \mu m, \ W = 3.16 \ \mu m, \ t_{BP} = 8.1 \ \text{nm}, \ t_{ox} = 15 \ \text{nm}, \) with rotational angle of 40°

![Image of transfer characteristics](image2)

FIG. 5. Transfer characteristics \( (I_{ds}-V_{gs}) \) of dataset 2 with constant \( R_{\text{hole}} \) and \( R_{\text{elec}} \) at room temperature. Solid lines are model fits, while symbols correspond to experimental data.

**B. Dataset 2**

The second dataset corresponds to back-gated BP FETs with \( L = 0.3 \ \mu m, \ W = 3.16 \ \mu m, \ t_{BP} = 8.1 \ \text{nm}, \ t_{ox} = 15 \ \text{nm}, \) and rotational angle of 40°. Unlike dataset 1, where the effect of contact resistances is not evident due to the low on-current of the device, a proper consideration of contact resistances is required to interpret dataset 2. This is because the channel length of the device in dataset 2 is \( 3 \times \) smaller than that of the device analyzed in dataset 1. Assuming a constant value for \( R_{\text{hole}} = 21 \times 10^{-4} \ \Omega \text{m}, \) the fit of the model to
Dataset 2: \( L = 0.3 \, \mu m, \, W = 3.16 \, \mu m, \, t_{\text{BP}} = 8.1 \, \text{nm}, \, t_{\text{ox}} = 15 \, \text{nm}, \) with rotational angle of 40\(^{\circ}\), and \( T = 298 \, \text{K} \).

FIG. 6. Model fit to the experimental dataset 2 at room temperature: (a) transfer characteristics \( (I_{\text{ds}}-V_{\text{gs}}) \), (b) transconductance \( (g_m = \partial I_{\text{ds}}/\partial V_{\text{gs}}) \), (c) output characteristics \( (I_{\text{ds}}-V_{\text{ds}}) \), and (d) output conductance \( (g_d = \partial I_{\text{ds}}/\partial V_{\text{ds}}) \). Solid lines are model fits, while symbols correspond to experimental data.

The measured \( I_{\text{ds}} - V_{\text{gs}} \) data is shown in Fig. 5. The figure clearly shows that a constant \( R_{\text{hole}} \) is inadequate to explain the experimental data. A higher value of \( R_{\text{hole}} \) for \( V_{\text{gs}} > -2.1 \, \text{V} \) and a lower value of \( R_{\text{hole}} \) for \( V_{\text{gs}} < -2.1 \, \text{V} \) can significantly improve the fit quality. Therefore, a bias-dependent nonlinear model of \( R_{\text{hole}} \) is necessitated in this case as discussed in Sec. II B.

Model fits to the experimental I-V, transconductance, and output conductance data for the dataset 2 are shown in Figs. 6 (a)-(d). Model parameters extracted from this fit are listed in Table III. The validation of the model at various temperatures \( T = 280, 240, 200, \) and 180 K for dataset 2 is shown in Fig. 7. Because of the lack of experimental data at low temperatures, we only focus on \( V_{\text{ds}} \leq -1 \, \text{V} \). The model provides an excellent match with
Dataset 2: $L = 0.3 \, \mu m$, $W = 3.16 \, \mu m$, $t_{BP} = 8.1 \, nm$, $t_{ox} = 15 \, nm$, with rotational angle of $40^\circ$.

FIG. 7. Model fit to the experimental dataset 2 at $T = (a) \, 280 \, K$, (b) $240 \, K$, (c) $200 \, K$, and (d) $180 \, K$ for $V_{ds} : -1, -1.5, -2, \text{ and } -2.5 \, V$. Solid lines are model fits, while symbols correspond to experimental data.

Experimental data over broad bias and temperature range for this device.

C. Datasets 3 and 4

The last two datasets are obtained through numerical simulations using the TCAD tool Sentaurus for top-gated and back-gated BP FETs with channel length $L = 0.3 \, \mu m$, $W = 3.16 \, \mu m$, $t_{BP} = 8.1 \, nm$, top-oxide thickness, $t_{ox, \text{top}} = 10 \, nm$ and back-oxide thickness $t_{ox, \text{back}} = 15 \, nm$, and source/drain contact length, $L_{\text{cont}} = 1.16 \, \mu m$. In Sentaurus, the Poisson and current continuity equations are solved self-consistently for both the contact and channel regions under the drift-diffusion approximation. Since Sentaurus does not provide parameters for 2D materials, we use previously published results obtained from experimental and theoretical calculations summarized in table $^{[12][18][24]}$. The Schottky contact is defined as a boundary
Dataset 3: $L = 0.3 \, \mu m$, $W = 3.16 \, \mu m$, $t_{BP} = 8.1 \, nm$, $t_{ox,back} = 15 \, nm$, $t_{ox,top} = 10 \, nm$, $L_{cont} = 1.16 \, \mu m$, and $T = 298 \, K$

FIG. 8. Model fit to the numerical dataset 3 at room temperature: (a) transfer characteristics ($I_{ds} - V_{gs}$), (b) transconductance ($g_m = \partial I_{ds} / \partial V_{gs}$), (c) output characteristics ($I_{ds} - V_{ds}$), and (d) output conductance ($g_d = \partial I_{ds} / \partial V_{ds}$). Solid lines are model fits, while symbols correspond to numerical data.

condition between the contacts and the semiconductor. The work function of the metal contact is chosen as $\phi_m = 4.046 \, eV$, and the electron affinity of BP is $\chi_{BP} = 3.655 \, eV$\footnote{18}

Besides the thermionic emission, thermally assisted and direct tunneling through the SB are also considered using a non-local tunneling model\footnote{23}. In this simulation, we ignore the effects of traps and carriers generation and recombination.

Model fits to the numerical I-V, transconductance, and output conductance data for the dataset 3 are shown in Figs. 8 (a)-(d). Model fits corresponding to dataset 4 also shown an excellent agreement with the data, but are omitted for brevity. Model parameters extracted from this fit are listed in Table IV\footnote{18}. Also, the validation of the model at various temperatures
Dataset 3: $L = 0.3 \, \mu m$, $W = 3.16 \, \mu m$, $t_{\text{BP}} = 8.1 \, \text{nm}$, $t_{\text{ox,back}} = 15 \, \text{nm}$, $t_{\text{ox,top}} = 10 \, \text{nm}$, and $L_{\text{cont}} = 1.16 \, \mu m$.

FIG. 9. Model fit to the numerical dataset 3 at $T = (a) 280 \, \text{K}$, (b) 240 K, (c) 200 K, and (d) 180 K for $V_{\text{ds}} : -0.1$, -1.5, -2, and -2.5 V. Solid lines are model fits, while symbols correspond to numerical data.

For all datasets, we observe that $\mu_{\text{hole}} > \mu_{\text{elec}}$, which is in agreement with experimental results previously reported in various BP FETs. The extracted values of carrier mobility, unfortunately, are notably smaller than those reported in prior work. Yet, the mobility values of these devices are very close to those extracted from $g_m$ measurements.
TABLE III. Model parameters for datasets 1 and 2 (experimental).

| Model parameter                                                                 | Dataset 1 | Dataset 2 | Dataset 1 | Dataset 2 |
|--------------------------------------------------------------------------------|-----------|-----------|-----------|-----------|
| Carrier mobility at 298 K, $\mu_{298}$ (cm$^2$/Vs)                          | Electron  | Hole      | Electron  | Hole      |
| Temperature dependence for mobility, $\xi_\mu$ (unit-less)                     | 0.01      | 0.17      | 0.2       | 0.3       |
| Carrier saturation velocity at 298 K, $v_{x0,298}$ (m/s)                      | $0.5 \times 10^4$ | $1.5 \times 10^4$ | $1.5 \times 10^4$ | $2 \times 10^4$ |
| Temperature dependence for saturation velocity, $\xi_v$ (m/sK)                | 50        | 50        | 50        | 50        |
| Non-ideality factor, $n_0$ (unit-less)                                       | 7         | 7.5       | 5.4       | 2.5       |
| Punch-through factor at 298 K, $n_d,298$ (1/V)                               | 0.12      | 3.42      | 3         | 3.5       |
| Temperature dependence for punch-through factor, $\xi_{nd}$ (1/VK)            | 0.025     | 0.02      | 0.009     | 0.013     |
| Shift in threshold voltage for charge trapping at 298 K, $\Delta_v,298$ (V)  | 0.67      | 1.02      | 1.02      | 0.71      |
| Temperature dependence for $\Delta_1$, $\xi_\Delta_1$ (V/K)                | $1.2 \times 10^{-3}$ | $-1.64 \times 10^{-3}$ | $0.44 \times 10^{-3}$ | 0        |
| Shift in ambipolar point at high $|V_{ds}|$, $\Delta_2$ (1/V)             | 0.14      | 0.52      | 1.05      | 0.79      |
| Threshold voltage adjustment parameter at high $|V_{ds}|$, $\Delta_3$          | 0.002     | 0.083     | 0.4       | 0.28      |
| Ambipolar point at $V_{ds} = 0$, $V_{min0}$ (V)                               | 0.162     | 0.162     | 0.181     | 0.181     |
| Adjustment the smoothness of $V_{se(h)}$ transition, $\alpha'$ (unit-less)   | 9         | 9         | 4         | 6         |
| Shift in the $V_{se(h)}$ in sub-threshold and strong inversion, $\alpha$ (unit-less) | 3         | 3         | 2         | 6         |
| Empirical parameter for $F_{sat}$, $\beta$ (unit-less)                       | 1.5       | 1.5       | 1.5       | 2         |
| Contact resistance at 298 K, $R_{elec(hole)}$ (\Omega-m)                     | $10^{-8}$ | $10^{-8}$ | $65 \times 10^{-4}$ | —         |
| Contact ohmic resistance, $R_{ohmic(1)}$ (\Omega-m)                         | —         | —         | —         | $3 \times 10^{-4}$ | ($14 \times 10^{-4}$) |
| Schottky barrier resistance coefficient, $R_{01(2)}$ (\Omega-m)             | —         | —         | —         | 0.105(0.014) |
| Gate voltage dependence for Schottky barrier resistance, $a_{1(2)}$ (1/V)   | —         | —         | —         | 2.053(1.39) |
| Transition point between two different transport paths, $V_{01(2)}$ (V)      | —         | —         | —         | 0(0.452)   |
| Adjustment the smoothness of $R_{hole}$, $\gamma$ (V)                        | —         | —         | —         | 0.67       |

of similar devices fabricated at the University of Minnesota.$^{36,37}$ The reason for low mobility values in these samples is attributed to a combination of interface scattering, remote phonon scattering from the gate dielectric and the substrate, defects, and charged impurity scattering.$^{36,44}$ However, recent experimental work has demonstrated that the carrier mobility in back-gated BP FETs with HfO$_2$ dielectric can be improved to 165 cm$^2$/Vs at room-temperature by optimizing the fabrication method.$^{50}$ The extracted values of the saturation velocity of carriers are also in agreement with those reported in prior work.$^{51,57,58}$

As a result of the large effective mass of electrons in BP, the model correctly predicts that $v_{x0,e} < v_{x0,h}$.$^{51}$

V. CONCLUSION

In this work, we develop a virtual-source-based analytic model to describe ambipolar current conduction in BP transistors over a broad range of bias and temperature values. The model comprehends the nonlinearity and the bias-dependence of Schottky source/drain


contacts, which is necessary to explain the I-V behavior of short-channel back-gated BP transistors. The model can also capture the low-temperature transport in BP transistors. To accomplish this, key parameters such as the carrier mobility, saturation velocity, punch-through factor, and threshold voltage are modeled as simple temperature-dependent functions. The accuracy of the model is demonstrated by applying to top- and back-gated BP transistors with channel lengths of 1000 nm and 300 nm with temperature from 300 K to 180 K.

TABLE IV. Model parameters for datasets 3 and 4 (numerical).

| Model parameter                                      | Dataset 3 | Dataset 4 |
|------------------------------------------------------|-----------|-----------|
| Carrier mobility at 298 K, $\mu_{298}$ (cm$^2$/Vs)  | 110       | 110       |
| Temperature dependence for mobility, $\xi_\mu$ (unit-less) | 0.05      | —         |
| Carrier saturation velocity at 298 K, $v_{298}$ (m/s) | $2.9 \times 10^4$ | $2.9 \times 10^4$ |
| Temperature dependence for saturation velocity, $\xi_v$ (m/sK) | 50        | —         |
| Non-ideality factor, $n_0$ (unit-less)               | 2.5       | 6         |
| Punch-through factor at 298 K, $n_{d,298}$ (1/V)     | 2.5       | 3         |
| Temperature dependence for punch-through factor, $\xi_{nd}$ (1/VK) | 0.0152    | —         |
| Shift in threshold voltage for charge trapping at 298 K, $\Delta_{1,298}$ (V) | 0.69      | 2         |
| Temperature dependence for $\Delta_1$, $\Delta_4$ (V/K) | $0.76 \times 10^{-3}$ | $0.5 \times 10^{-3}$ |
| Shift in ambipolar point at high $|V_{ds}|$, $\Delta_2$ (1/V) | 0.62      | 0.59      |
| Threshold voltage adjustment parameter at high $|V_{ds}|$, $\Delta_3$ (1/V$^2$) | 0.2       | 0.1       |
| Ambipolar point at $V_{ds} = 0$, $V_{min,0}$ (V)    | 0.02      | 0.17      |
| Adjustment the smoothness of $V_{te(h)}$ transition, $\alpha'$ (unit-less) | 3.9       | 4         |
| Shift in the $V_{te(h)}$ in sub-threshold and strong inversion, $\alpha$ (unit-less) | 2         | 5         |
| Empirical parameter for $F_{sat}$, $\beta$ (unit-less) | 2         | 2         |
| Contact resistance at 298 K, $R_{elec(hole)}$ (\Omega m) | $10^{-4}$ | $65 \times 10^{-4}$ |
| Contact ohmic resistance, $R_{ohmic1(2)}$ (\Omega m) | —         | —         |
| Schottky barrier resistance coefficient, $R_{01(2)}$ (\Omega m) | —         | —         |
| Gate voltage dependence for Schottky barrier resistance, $a_{1(2)}$ (1/V) | —         | —         |
| Transition point between two different transport paths, $V_{01(2)}$ (V) | —         | —         |
| Adjustment the smoothness of $R_{hole}$, $\gamma$ (V) | —         | —         |

TABLE V. BP parameters used for TCAD simulation obtained from the literature$^{[2][1][8][24]}$

| Parameter                          | Value |
|------------------------------------|-------|
| Band gap (eV)                      | 0.69  |
| Electron effective mass (unit-less) | 0.15 (armchair direction) 1.18 (zigzag direction) |
| Hole effective mass (unit-less)    | 0.14 (armchair direction) 0.89 (zigzag direction) |
| Dielectric constant (unit-less)    | 8.3   |
| Electron affinity (eV)             | 3.655 |
K. The smoothness of the current and its derivatives is guaranteed in the model, thus satisfying a key criteria for compact models. Since the model is based on threshold-voltage-based current calculation, it does not require a self-consistent solution based on surface potential. As such, the model is computationally less expensive and suitable to simulate and optimize BP-based circuits.

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Appendix A: Extraction methodology of model parameters

The parameter extraction begins by identifying the Dirac point (minimum conductivity), $V_{\text{min}0}$, at $V_{ds} = 0$ V. The values of $\Delta_{1e(h)}$, $\Delta_{2e(h)}$, and $\Delta_{3e(h)}$ are determined by matching the Dirac point from experimentally measured transfer curves and the model at all $V_{ds}$ values. As shown in Fig. 2(a) in Sec. IVA, the Dirac point voltage is a strong function of $V_{ds}$ which varies from 0.06 V for $V_{ds} = -0.1$ V to -1.14 V for $V_{ds} = -2.5$ V.

The on-off current ratio is about 400 at $V_{ds} = -0.1$ V. However, the on-off current ratio is as low as 4 at $V_{ds} = -2.5$ V. This implies that the device is nearly always on at high $V_{ds}$. This behavior can be explained by observing that even when the current due to hole conduction drops, the electron branch current increases, preventing the device from turning off at high $V_{ds}$. By using an appropriate model of the electron and hole threshold voltages as in Eq. 7, we can capture the on-off device behavior in both equilibrium and off-equilibrium transport conditions. With $\Delta_{3h} \neq 0$ (positive value), we can model the decrease (increase) in $V_{\text{te(h)}}$ at large negative $V_{ds}$ values. Figure 10(a) plots the hole threshold voltage ($V_{th}$) predicted by the model for the first dataset as a function of $V_{ds}$ for $\Delta_{3h} \neq 0$ (solid line), and $\Delta_{3h} = 0$ (dashed line). With $\Delta_{3h} = 0$, we see that $V_{th}$ monotonically decreases with $V_{ds}$, which is not the desired behavior. The transfer characteristics of the device using $\Delta_{3h} = 0$ and other parameters as listed in Table III are plotted in Fig. 10(b). The figure shows a
poor match between the model and experimental data at highly negative $V_{ds}$.

The transfer curve experimental data is used to obtain the values of the non-ideality factor ($n_0$) at $V_{ds} = 0$ V. Similarly, the punch-through factor ($n_d$) can be obtained from experimental data by measuring the sub-threshold slope (SS) at various $V_{ds}$ values. Moreover, the effective mobility values of these devices are chosen very close to those extracted from $g_m$ measurements of similar devices fabricated at the University of Minnesota.\textsuperscript{36,37} The extracted values of the saturation velocity of carriers are also in agreement with those reported in prior work.\textsuperscript{51,57,58}

In this model, $\beta_{e/h}$ and $\alpha_{e/h}$ are empirical fitting parameters, and according to previous published works for VS model,\textsuperscript{23,59,60} their values are tuned within a range of 1.5 to 2 and 2 to 6, respectively. Prior VS models have shown that the parameter $\alpha_{e/h}'$ is of the same order of magnitude as $\alpha_{e/h}$. Figure 10 (c) shows the transconductance of dataset 1 by using $\alpha_{e/h}' = 0.5 \alpha_{e/h}$, which is the typical value of $\alpha_{e/h}'$ in prior VS models. All other fitting parameters are the same as those listed in Table III. This figure shows that for $\alpha_{e/h}' = 0.5 \alpha_{e/h}$, the transconductance displays several kinks, which can be smoothed by using a slightly larger value of $\alpha_{e/h}'$ as listed in Table III.

The value of $R_{\text{elec}}$ is obtained using TLM measurements reported in Refs. 36 and 42. The process to find optimal parameters in $R_{h0}$, which is non-linear and bias-dependent, is as follows. First, we choose a large negative value of $V_{gs}$ such that the term $\exp(aV_{gsi}) \to 0$ (see Eq. (9)). This allows us to extract appropriate values of $R_{\text{ohmic,1(2)}}$ and $\gamma$ using the measured output characteristics. On the other hand, at very low $|V_{gs}|$, $\exp(aV_{gsi})$ in Eq. (9) approaches unity. Using experimental I-V data in this regime, we can identify the value of $R_{01(2)}$. The parameters $a_{1(2)}$ and $V_{01(2)}$ are empirical in nature and extracted by minimizing the least-square error between the model and experimental I-V data. Finally, we use the I-V measurements at different temperatures to identify the temperature dependence of key model parameters, namely mobility, saturation velocity, punch-through factor, and threshold voltage. The extracted temperature coefficients lie in the expected range based on previous experimental and theoretical predictions.

Appendix B: Carrier concentration dependent mobility model

In recent experimental work, the effect of carrier concentration on both hole and electron mobility in back-gated BP FETs was explored over a broad range of temperatures.\textsuperscript{60} As a
Dataset 1: \( L = 1 \ \mu m, \ W = 7.32 \ \mu m, \ t_{BP} = 7.3 \ \text{nm}, \ t_{ox} = 15 \ \text{nm}, \) with rotational angle 42°, and \( T = 298 \ \text{K} \)

FIG. 10. (a) hole threshold voltage \( (V_{th}) \) for first dataset obtained from the model, at room temperature, by using Eq. (7) for \( \Delta_{3h} \neq 0 \) (solid line), and \( \Delta_{3h} = 0 \) (dashed line), (b) transfer characteristics \( (I_{ds}-V_{gs}) \) for dataset 1, at room temperature, by setting \( \Delta_{3h} = 0 \) in Eq. (7), (c) transfer conductance \( (g_m = \partial I_{ds}/\partial V_{gs}) \) for dataset 1 with \( \alpha'_e/h = 0.5 \alpha_e/h \) at room temperature. Solid lines are model fits, while symbols correspond to experimental data.

result of electrostatic screening in the sample, the carrier mobility was found to increase with an increase in carrier concentration for all temperatures ranging from 77 K to 295 K.

To handle the variation in carrier mobility with carrier concentration, Eq.(12) is modified as

\[
\mu_{e/h} = \mu_{0,e/h} \left( 1 + \frac{Qx_{0,e/h}}{Q_{0,e/h}} \right)^{B_e/h} \left( \frac{298}{T} \right)^{\xi_{\mu,e/h}},
\]

where \( \mu_{0,e/h}, B_e/h, \) and \( Q_{0,e/h} \) are fitting parameters depending on the oxide dielectric constant, BP crystal orientation, and impurity density. \( Q_{x0,e/h} \) is also given in Eq. 4.

The updated model introduces an additional three fitting parameters, which can be determined from measurement data such as in Ref. 50. Model parameters corresponding to dataset 2 at 298 K are extracted using Eq.[B1] for the hole mobility. The fitting results are shown in Fig. 11. Here, only the parameters corresponding to the contact resistances \( (R_{ohmic1(2)}, R_{01(2)}, \) and \( a_{1(2)}) \), shift in threshold voltage \( (\Delta_{1h(2h)}) \), and empirical parameter \( \alpha' \) are tweaked, while the remainder model parameters are the same as those reported in Table III. With a positive value of \( B_e/h \), the carrier mobility increases at higher \( V_{gs} \) (higher carrier concentration), necessitating a slightly larger value of the hole contact resistance to match the experimental \( I_{ds} \) data in on-state.
Dataset 2: $L = 0.3\ \mu m$, $W = 3.16\ \mu m$, $t_{BP} = 8.1\ nm$, $t_{ox} = 15\ nm$, with rotational angle of $40^\circ$

![Graph showing transfer characteristics](image)

FIG. 11. Transfer characteristics ($I_{ds}$-$V_{gs}$) for dataset 2, at room temperature, by using Eq. B1 for hole mobility. $\mu_{0,e/h} = 60\ cm^2/Vs$, $B_{e/h} = 1.5$, $Q_{0,e/h} = 0.03\ C/m^2$, $R_{ohmic1(2)} = 0.0016(0.0017)$ $\Omega$-m, $R_{01(2)} = 0.1155(0.0146)$ $\Omega$-m, $a_{1(2)} = 2.0972(1.4910)\ 1/V$, $\Delta_{1h(2h)} = 0.69(0.81)\ V(1/V)$, and $\alpha' = 4.7$, all other fitting parameters are equal to the values mentioned in Table III. Solid lines are model fits, while symbols correspond to numerical data.

Appendix C: Electrostatic potential and contact resistances

To understand the nonlinearity of contact resistances, we consider the data obtained from numerical simulations using Synopsys Sentaurus (datasets 3 and 4 in the main text). In Fig. 12, electrostatic potential distribution for $V_{gs} = 1.1$, $V_{ds} = 0.1\ V$ and $2.5\ V$ is shown. Results in Fig. 12(a) and (b) show that the carriers paths between the source/drain contacts depend on the applied bias voltages for the back-gated device. This is in agreement with the discussion in Sec. II B. For $V_{ds} < V_{gs}$, only paths 1 and 2 labeled in Fig. 1 are transparent for current conduction. However, additional conduction paths for both carrier types contribute to current when $V_{ds} > V_{gs}$. On the other hand, for top-gated structure, as shown in Figs. 12(c) and (d), carrier transport is independent of the bias voltages.

The analytic charge model (Eq. 4 in Sec. IIA) is validated by comparing the results against the charges obtained numerically for dataset 4. Results are shown in Fig. 13. The model also faithfully reproduces the behavior of inversion capacitance ($-\partial(Q_{x0,e}+Q_{x0,h})/\partial V_{gs}$) versus $V_{gs}$, thus validating our charge modeling approach.
FIG. 12. Surface plot of the electrostatic potential for the back-gated simulated device with $L_{ch} = 0.3 \, \mu m$, $W = 3.16 \, \mu m$, $t_{BP} = 8.1 \, nm$, $t_{ox} = 15 \, nm$, and $L_{cont} = 1.16 \, \mu m$ (dataset 4) for (a) $V_{gs} = 1.1 \, V$ and $V_{ds} = 0.1 \, V$ and (b) $V_{gs} = 1.1 \, V$ and $V_{ds} = 2.5 \, V$, and top-gated structure (dataset 3) with $L = 0.3 \, \mu m$, $W = 3.16 \, \mu m$, $t_{BP} = 8.1 \, nm$, $t_{ox,back} = 15 \, nm$, $t_{ox,top} = 10 \, nm$, and $L_{cont} = 1.16 \, \mu m$ for (c) $V_{gs} = 1.1 \, V$ and $V_{ds} = 0.1 \, V$ and (d) $V_{gs} = 1.1 \, V$ and $V_{ds} = 2.5 \, V$.

Appendix D: Verilog-A and circuit simulation

The model is implemented in Verilog-A to perform circuit simulations in SPICE. In Fig. 14, the model is used to simulate the dc behavior of a BP-based inverter and the transient behavior of a BP-based 3-stage ring oscillator circuit. Transistor parameters corresponding to dataset 2 are used for these simulations. The results show the mathematical robustness of the model, ease of computation, and the capability to handle large-scale circuit simulations.

The model developed in this paper also satisfies the Gummel symmetry test (GST) required for physically accurate and well-behaved compact models. According to the GST, the model must have a symmetric formulation around $V_{ds} = 0 \, V$. Additionally, the higher order derivatives of current must be continuous. To demonstrate that the model passes the GST, the source and drain are biased differentially ($V_x$ and $-V_x$), while the gate terminal
Numerical simulation: $L_{ch} = 0.3 \, \mu m$, $W = 3.16 \, \mu m$, $t_{BP} = 8.1 \, nm$, $t_{ox} = 15 \, nm$, and contact length $L_{cont} = 1.16 \, \mu m$.

FIG. 13. Model fit to the numerical data obtained from TCAD simulation at room temperature for $V_{ds} = -0.1, -0.5 \, V$: (a) total charge ($Q_{x0,e} + Q_{x0,h}$) as a function of $V_{gs}$, (b) inversion capacitance ($-\partial (Q_{x0,e} + Q_{x0,h}) / \partial V_{gs}$) as a function of $V_{gs}$. Solid lines are model fits, while symbols correspond to numerical data.

FIG. 14. (a) DC simulation of inverter: output voltage as a function of input voltage for $V_{DD} = 1 \, V$. Inset shows schematic of an inverter, (b) transient simulation for 3-stage ring oscillator where $C_L = 3 \, fF$. Inset indicates the schematic of the 3-stage ring oscillator, (c) results of the Gummel symmetry test (GST) for the (i) current, (ii) first, (iii) second, and (iv) third order derivatives of current with respect to $V_x$ for $V_{gs} = 1 \, V$ with arbitrary units. Transistor parameters are same as dataset 2.

has a fixed voltage. Results of the GST reported in Fig. 14 (c) verify that the model and its higher order derivatives are symmetric around $V_x = 0 \, V$. 

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