A 55-dB dynamic range wideband RF logarithmic power detector with temperature and DC offset compensation

Yingdan Jiang1, 2, a), Xuelian Liu2, Qinfeng Zhang2, Xiaobo Su2–3, Zongguang Yu1–2, and Hong Zhang4

Abstract A wideband RF logarithmic power detector with large dynamic range is presented in this work. The power detector fabricated in 180-nm SiGe process employs the successive approximation technique over a 6-stage cascaded amplifier chain. A cross-coupled cascode amplifier architecture is proposed to expand bandwidth up to 8 GHz. With a temperature compensation circuit and a DC offset compensation loop, the detector provides consistent logarithmic performance at different temperatures in band, which can be applied in highly reliable RF systems. The measured input dynamic range is larger than 50 dB in 1 MHz–8 GHz with less than ±1 dB error and 55 dB at 8 GHz with less than ±3 dB error. The measured temperature drift is less than ±1.0 dB at 5 GHz over the temperature range from −40 to 85 °C.

Keywords: RF, power detector, limiting amplifier, wideband, wide dynamic range, highly reliable

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Power detectors (PDs) are widely used in radio link transceivers that require wide bandwidth, large dynamic range, high accuracy and stability over temperature. They are utilized to optimize the system’s performance by monitoring the RF power and forming a precise control loop to maintain constant amplitude of received signals or appropriate power of transmitted signals [1].

Most of the traditional power detectors are designed based on the nonlinear transfer function of diodes or MOSFETs, which show limited dynamic ranges [2, 3, 4, 5, 6]. Aided by a switched-capacitor structure, the power detector reported in [2] achieves 34-dB dynamic range with ±1 dB error at 5 GHz in 65 nm CMOS process. The detection of the PDs in [3] is realized by the emitter-base junction of a BJT and the rectified collector current is amplified through a PMOS current mirror, showing a measured dynamic range of 30 dB for millimeter-wave automatic level control usage. Logarithmic amplifier based detectors exhibit large dynamic range and linear-in-dB response, which are highly desirable in radio frequency systems [7, 8, 9, 10, 11]. Implemented in 0.13 μm CMOS process, the power detector in [7] combines three signal amplification and rectification branches in parallel for broadband operation over 43-dB dynamic range up to 14 GHz. However, its dynamic range changes a lot as the radio frequency goes from low to high.

This paper presents a wide dynamic range logarithmic RF power detector with compensation techniques. In order to enlarge the bandwidth, a cross-coupled cascode architecture is proposed. Both temperature and DC offset compensation loops are employed to ensure consistent in-band performance in a wide temperature range.

This paper is organized as follows. Section 2 describes the architecture and circuit design of the proposed detector. The measurement results are presented in Section 3 and the paper is summarized in Section 4.

2. Proposed detector architecture and circuit design

The architecture of the proposed RF power detector consists of a 6-stage cascaded amplifier (A) chain, and each stage is equipped with a rectifier (D), as illustrated in Fig. 1. The linear-in-dB function of the PD is realized by successive approximation technique. The tap voltages from the limiting amplifier stages are converted into currents by the rectifiers. The currents are summed together to produce a DC output voltage, which is proportional to the input power [12, 13, 14]. Consequently, a piece-wise linear approximation of the logarithmic function is obtained as follows [15]:

$$V_{out}[V] = K_{slope}(P_{in} - P_0),$$

where $K_{slope}$ is the slope of the transfer characteristic. Both the input power $P_{in}$ and the intercept power $P_0$ are expressed in dBm.

A DC offset cancellation circuit (DC OC) based on DC feedback is introduced to lower the DC gain of the PD. In
order to obtain a temperature-independent transfer characteristic, a temperature compensation circuit (TEMP COMP) injects a compensation current into the output branch, as illustrated in Fig. 1.

2.1 Limiting amplifier

If the amplitude of the input signal to the PD is small enough, it will be amplified by all limiting amplifiers. The last stage of the amplifier chain goes into saturation as the input signal amplitude is increased to a given level. Hence, a large input RF signal range is compressed to a smaller output voltage range. The bandwidth of the limiting amplifier is important for selecting the bandwidth of the PD, and the dynamic range of the PD is limited by the gain of the limiting amplifier [16].

Assuming the PD is designed with N-stage cascaded amplifiers, and requiring overall small signal gain \( A_{total} \) and bandwidth \( f_{total} \), then the normalized gain \( A_s \) and the bandwidth \( f_s \) of each stage can be derived as [17]:

\[
A_s = A_{total}^{-1/N}
\]  
(2)

\[
f_s = f_{total} \frac{1}{2^{1/N} - 1}
\]  
(3)

Once the overall gain and bandwidth of the PD are specified, the gain of each stage is obviously reduced as the cascading number of stage increases. Six limiting amplifier stages are applied in the proposed PD.

Various configurations have been studied to expand the bandwidth of limiting amplifiers, such as inductive peaking technology [18], capacitive degeneration technique [19], Cherry-Hopper topology [20], active negative feedback architecture [21], PMOS diode-connected load [22] etc. Compared to MOSFETS, SiGe HBTs usually provide larger transconductance. A cross-coupled cascode limiting amplifier with SiGe HBTs is proposed, as shown in Fig. 2. The cross-coupled cascode NPNs (Q3 and Q4) with positive feedback is introduced to eliminate the Miller effect and boost the gain by providing a negative resistance. The source follower at the output is used to decouple the load impedance from the input capacitance of the next stage while expand the bandwidth of the PD, which also shifts the output down to drive the next stage properly.

2.2 Temperature compensation circuit

As the amplitude of the input signal to the PD is held constant, the primary factor that lead to \( V_{OUT} \)’s variation with temperature is the drift of the intercept. The drift voltage can be cancelled by an additional voltage compensation circuit, which ensures temperature-independent transfer characteristic of the PD [23].

The proposed temperature compensation circuit is shown in Fig. 3, in which Q1 ~ Q4 are designed with the same size. Both \( I_{ptat} \) and \( I_b \) are generated by the biasing circuit of the PD. \( I_{ptat} \) is the current proportional to absolute temperature. \( I_b \) is the current complementary to absolute temperature. Thus, the output currents, \( I_{comp1} \) and \( I_{comp2} \), provide complementary temperature coefficients as illustrated in Fig. 4. Both the temperature compensation current \( I_{TC} \) and voltage \( V_{TC} \) can be obtained as follows:

\[
I_{TC} = I_{comp2} - I_{comp1}
\]  
(4)

\[
V_{TC} = (I_{comp2} - I_{comp1})R_{OUT}
\]  
(5)

As shown in Fig. 1, the temperature compensation current \( I_{TC} \) is added to get the final output current of the PD \( I_{OUT} \), in order to decrease the output temperature drift. According to the simulation results shown in Fig. 5 with 900 MHz RF input frequency, the temperature drift is decreased from ±3.2 dB to ±1.0 dB over the temperature range of −40–85°C after compensation.
2.3 DC offset compensation loop

Mismatches between devices may cause DC offset at the output of the amplifier. The DC offset is accumulated stage by stage along the cascaded amplifier chain, and is detected as an additional differential input signal by the rectifier. As a result, the output of the PD may be much larger than that indicated by the actual input signal, even saturate the signal chain, which deteriorate in detection accuracy severely [24, 25, 26]. The DC offset voltage of the proposed PD is simulated to be about 0.01 mV, which can be amplified by the 6-stage limiting amplifier chain to as large as 10 mV.

In order to suppress the DC offset’s effect, a DC offset compensation loop is designed to feed the output of the last stage back to the input of the first stage, as illustrated in Fig. 6, which provides a negative feedback loop to null the DC offset at the last stage’s output [27]. In order to preserve the frequency response to the signal of interest while attenuate the DC offset, the dominant pole of the feedback branch \( p_2 \) should be small enough to meet the following requirements [28]:

\[
(1 + G_1 G_2) p_2 \ll p_1, \quad (6)
\]

where \( p_1 \) is the dominant pole of the open-loop transfer function, \( G_1 \) and \( G_2 \) are DC gains of the feedforward and feedback branch, respectively.

According to the simulation results both shown in Table I and Fig. 7, the DC offset voltage is significantly cancelled from \(-9.25 \text{ mV}\) to \(-0.18 \text{ mV}\) by the proposed compensation loop, and the linearity performance of the proposed PD is optimized obviously.

### Table I

| Voltage | Without DC OC | With DC OC | Unit |
|---------|---------------|------------|------|
| VOP     | 2.76666      | 2.75092    | V    |
| VON     | 2.75592      | 2.7511     | V    |
| VOP-VON | -9.25        | -0.18      | mV   |

3. Measurement results

The presented wideband RF logarithmic power detector has been realized in 180-nm SiGe process with a chip size of 0.66 mm\(^2\), as depicted in Fig. 8. The measured output voltages and errors versus the input power of the proposed PD at 25°C are illustrated in Fig. 9, showing that the dynamic range is up to 50 dB with ±1 dB error from 1 MHz to 8 GHz. If error tolerance can be enlarged to ±3 dB, the dynamic range is increased to 55 dB from 1 MHz to 8 GHz. The dynamic range and accuracy of the proposed PD at 5 GHz over the
The proposed PD with compensation technique is compared with other published large dynamic range wideband PDs, as shown in Table II [22, 29, 30, 31]. This work achieves the largest dynamic range with a lowest minimum detectable power of $-54$ dBm. The wideband performance from 1 MHz to 8 GHz is obtained thanks to the limiting amplifiers with cross-coupled cascode architecture and compensation techniques.

### 4. Conclusion

This paper presents a successive approximation RF logarithmic power detector with both temperature and DC offset compensation loops. The PD is successfully implemented in 180-nm SiGe process, which achieves a dynamic range larger than 50 dB with ±1 dB error from 1 MHz to 8 GHz, and 55 dB with ±3 dB error at 8 GHz. A temperature drift of ±1.0 dB at 5 GHz from −40°C to 85°C is obtained simultaneously. The wideband RF logarithmic power detector provides large dynamic range, high accuracy and stable performance against ambient temperature variations.

### References

[1] J. Lee: “RF power detector design with temperature compensation for power amplifiers bias control,” IEICE Electron. Express 6 (2009) 418 (DOI: 10.1587/elex.6.418).

[2] C. Li, et al.: “A 34-dB dynamic range 0.7-mW compact switched-capacitor power detector in 65-nm CMOS,” IEEE Trans. Power Electron. 34 (2019) 9365 (DOI: 10.1109/TPEL.2019.2908283).

[3] A. Serhan, et al.: “A 700MHz output bandwidth, 30dB dynamic range, common-base mm-wave power detector,” IEEE IMS Dig. Tech. Papers (2015) 1 (DOI: 10.1109/MWSYM.2015.7166764).

[4] T. Zhang, et al.: “A novel 5GHz RF power detector,” IEEE ISCAS Dig. Tech. Papers (2004) 897 (DOI: 10.1109/ISCAS.2004.1328340).

[5] V. Milanovic, et al.: “CMOS foundry implementation of Schottky diodes for RF detection,” IEEE Trans. Electron Devices 43 (1996) 2210 (DOI: 10.1109/16.544393).

[6] T. Zhang, et al.: “Bipolar microwave RMS power detectors,” IEEE J. Solid-State Circuits 41 (2006) 2188 (DOI: 10.1109/JSSC.2006.880592).

[7] K. Kim and Y. Kwon: “A broadband logarithmic power detector in 0.13-μm CMOS,” IEEE Microw. Wireless Compon. Lett. 23 (2013) 498 (DOI: 10.1109/LMWC.2013.2274994).

[8] K.A. Townsend, et al.: “A CMOS integrated power detector for...
[9] S. Sakphrom and A. Thanachayamon: “A low-power CMOS RF power detector,” IEEE ICECS Dig. Tech. Papers (2012) 177 (DOI: 10.1109/ICECS.2012.6463771).

[10] X. Tian, et al.: “A low power dB-linear RSSI based on logarithmic amplifier,” IEICE Electron. Express 11 (2014) 20140431 (DOI: 10.1587/elex.11.20140431).

[11] C.-P. Wu, et al.: “A 110-MHz 84-dB CMOS programmable gain amplifier with integrated RSSI function,” IEEE J. Solid-State Circuits 40 (2005) 1249 (DOI: 10.1109/JSSC.2005.848023).

[12] Y. Tao, et al.: “A bipolar IF amplifier/RSSI for ASK receiver,” IEEE ASP-DAC Dig. Tech. Papers (2005) 1236 (DOI: 10.1109/ASPDAC.2005.1466566).

[13] J. Ramos, et al.: “Design of limiting/logarithmic amplifier for wide-band bioimpedance measuring devices,” IEEE BioCAS Dig. Tech. Papers (2010) 290 (DOI: 10.1109/BIOCAS.2010.5709628).

[14] Y. Melamed, et al.: “Systematic design of RSSI and logarithmic amplifiers circuits,” IEEE COMCAS Dig. Tech. Papers (2009) 1 (DOI: 10.1109/COMCAS.2009.5386086).

[15] E. Muja, et al.: “A 39 dB DR CMOS log-amp RF power detector with ±1 dB temperature drift from -40 to 85°C,” IEEE ESSCIRC Dig. Tech. Papers (2013) 287 (DOI: 10.1109/ESSCIRC.2013.6649129).

[16] P.-C. Huang, et al.: “A 2-V 10.7-MHz CMOS limiting amplifier/RSSI,” IEEE J. Solid-State Circuits 35 (2000) 1474 (DOI: 10.1109/4.871325).

[17] R.P. Jindal: “Gigahertz-band high-gain low-noise AGC amplifiers in fine-line NMOS,” IEEE J. Solid-State Circuits 22 (1987) 512 (DOI: 10.1109/JSSC.1987.1052765).

[18] S.S. Mohan, et al.: “Bandwidth extension in CMOS with optimized on-chip inductors,” IEEE J. Solid-State Circuits 35 (2000) 346 (DOI: 10.1109/4.826816).

[19] B. Shammasgamy, et al.: “A 24mW, 5GHz fully balanced differential output trans-impedance amplifier with active inductor and capacitive degeneration techniques in 0.18μm CMOS technology,” IEICE Electron. Express 7 (2010) 308 (DOI: 10.1587/elex.7.308).

[20] E.M. Cherry and D.E. Hooper: “The design of wide-band transistor feedback amplifiers,” Proceedings of the Institution of Electrical Engineers 110 (1963) 375 (DOI: 10.1049/piee.1963.0050).

[21] S. Galal and B. Razavi: “10GHz limiting amplifier and laser/ modulator driver in 0.18-μm CMOS technology,” IEEE J. Solid-State Circuits 38 (2003) 2138 (DOI: 10.1109/JSSC.2003.818567).

[22] J.-W. Wu, et al.: “A linear-in-dB radio-frequency power detector,” IEEE MTT-S International Microwave Symposium Dig. Tech. Papers (2011) 1 (DOI: 10.1109/MWSYM.2011.5972772).

[23] C. Bai and J. Wu: “A novel temperature compensating method of logarithmic amplifier in RSSI,” IEEE MELCON Dig. Tech. Papers (2014) 271 (DOI: 10.1109/MELCON.2014.6820545).

[24] A. Jain, et al.: “A variable gain amplifier with fast feedforward dc-offset compensation for 10GHz burst-mode receiver applications,” IET ISSC Dig. Tech. Papers (2012) 1 (DOI: 10.1049/ic.2012.0208).

[25] D. Tang, et al.: “A DC-coupled high dynamic range biomedical radar sensor with fast-settling analog DC offset cancellation,” IEEE Trans. Instrum. Meas. 68 (2019) 1441 (DOI: 10.1109/TIM.2018.2888917).

[26] J. Jin, et al.: “Fully configurable capacitor-less oversampling DC offset cancellation for direct conversion receivers,” IEEE Trans. Circuits Syst. II, Exp. Briefs 66 (2019) 1683 (DOI: 10.1109/TCSII.2019.2921895).

[27] T.B. Kumar, et al.: “A 4 GHz 60 dB variable gain amplifier with tunable DC offset cancellation in 65 nm CMOS,” IEEE Microw. Wireless Compon. Lett. 25 (2015) 37 (DOI: 10.1109/LMWC.2014.2361676).

[28] F. Xiangning, et al.: “An efficient CMOS DC offset cancellation circuit for PGA of low IF wireless receivers,” IEEE WCSP Dig. Tech. Papers (2010) 1 (DOI: 10.1109/WCSP.2010.5633563).

[29] S. Lakshminarayanan and K. Hofmann: “A wideband large dynamic range logarithmic RF power detector with 50 mV input offset cancellation range,” IEEE APCCAS Dig. Tech. Papers (2019) 85 (DOI: 10.1109/APCCAS47518.2019.8953120).

[30] S. Lakshminarayanan, et al.: “A wideband RF power detector with −56dB sensitivity and 64 dB dynamic range in SiGe BiCMOS technology,” IEEE ISCAS Dig. Tech. Papers (2017) 1 (DOI: 10.1109/ISCAS.2017.8050666).

[31] J. Choi, et al.: “Wide dynamic-range CMOS RMS power detector,” IEEE Trans. Microw. Theory Techn. 64 (2016) 868 (DOI: 10.1109/TMTT.2016.2519030).