A New Converter for Non-Isolated PV Systems

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Abstract: A new converter for the non-isolated PV (photovoltaic) system is presented in this paper. It has the advantage that the input terminal of the proposed converter is connected to the output negative terminal. In this way, the parasitic capacitance is bypassed to eliminate the undesirable leakage current. The proposed converter can achieve the step-up voltage with four switches only. Aside from that, the carried-based modulation is used, and the control structure is simple. The article analyzes the working modes and control strategy of the proposed converter. In addition, a comparative analysis is provided. The feasibility of the proposed converter under different working modes is verified by simulation. Finally, the digital control prototype with DSP plus FPGA is established and the experimental tests are carried out. The experimental results verify the effectiveness of the proposed converter.

Keywords: PV system; power converter; modulation

1. Introduction

In recent years, the PV power system has received widespread attention due to its pollution-free and renewable advantages [1,2]. It is mainly composed of a PV array and a power converter. The PV converter is an indispensable link in the solar power generation system. Whether the system contains a transformer is a key factor to distinguish PV grid-connected power systems, including the isolated and non-isolated ones [3,4]. The traditional, isolated PV inverter connects the transformer between the PV array and the grid to achieve electrical isolation. However, the overall structure is large, difficult to transport, and expensive with low efficiency [5]. Considering the above-mentioned problems, the non-isolated inverter system has been proposed. It does not contain a transformer, and thus it is small in size, low in cost, and low in energy loss [6–8]. Basically, the non-isolated inverters mainly have two structures [9]. Single-stage non-isolated inverter systems convert photovoltaic dc output to ac output through the traditional standard inverter structure. The advantages are simplified structure, low cost, low loss, and low difficulty in implementation [10], but this structure has higher requirements for the output voltage of the photovoltaic array, higher requirements for photovoltaic energy conversion on the DC input side, and corresponding difficulties in energy conversion efficiency and circuit design. Increasingly, it will also bring problems such as leakage current. Considering the two-stage non-isolated inverter, this circuit structure usually adds a boost circuit in the front stage of the inverter, and a chopper circuit such as a boost circuit is often used as its boost circuit. This type of circuit can output the voltage of the photovoltaic array and boost the voltage through the circuit structure and modulation method to improve the energy conversion efficiency, and then convert it to the ac voltage required by the load through the inverter structure. The advantage of this kind of circuit is that it can realize the decoupling of the front stage and the back stage by constructing the circuit. The overall circuit control is simple, the volume is light, and the interference is small. However, due to the increase in the number of stages, the stability of the combination of the two stages and the energy conversion efficiency is restricted [11–13]. Non-isolated inverters also have disadvantages, that is, the leakage current caused by parasitic capacitance, which can lead
to personal safety threats, grid harmonics, and other problems [14]. Therefore, the premise of ensuring the stability of the overall performance of the inverter system arises. Next, improving the inverter system’s ability to suppress leakage current has become a key point of non-isolated inverters.

Literature [15] proposed a two-stage integrated double-ended common-ground inverter. This inverter circuit can be combined with a full-bridge inverter and a boost converter. The negative terminal of the photovoltaic side and the negative terminal of the grid side can be combined. The ends are connected, which is a dual-end common-ground topology. This topology combines two switching converters into one topology. Due to the existence of the boost converter, the photovoltaic array needs to reduce the current ripple of the low-frequency input, but its shortcomings are also obvious. The number of switches is large, and the overall system needs to be reduced by 3 consisting of one inductor and three capacitors. The overall loss of the system will increase as the number of components increases. In [16], a four-switch non-isolated inverter is proposed. This topology is composed of four switches. The circuit structure of this topology is relatively simple, but the boosting capability is insufficient. A five-switch boost inverter topology is proposed in [17]. The main advantage is that the negative terminal of the input side and the negative terminal of the output side are connected. This circuit is composed of five switches. The voltage capability is better, but due to the larger ripple in the circuit, the switch in this circuit has higher voltage stress, which limits its practical application. In [18], a non-isolated efficient H7 inverter is proposed. The topology is interesting with experimental verification, but it is not able to achieve the step-up voltage capability with seven switches.

This paper proposes a new non-isolated inverter topology with step-up voltage capability with four switches only. The rest of the paper is organized as follows. Section 2 analyzes the proposed topology in different modulation modes and working modes. Section 3 provides the simulation and digital-control experimental results. The conclusion is reached in Section 4.

2. Proposed Converter
2.1. Circuit Configuration

The proposed converter is shown in Figure 1. It consists of a dc input source $V_{in}$, an input inductor $L_1$, a diode $D_2$, and a capacitor $C_1$. Switches $S_1$, $S_2$, $S_3$, and $S_4$ form an H-bridge circuit, which is connected in series on the input side of the circuit. A diode $D_1$ in the same direction is the input inductor current. The existence of this diode can ensure the unidirectional conductivity of the power supply and ensure the stable output waveform.

![Figure 1. The schematic of the proposed converter.](image)

The inverter circuit proposed in this paper is shown in Figure 1. It can be seen from the figure that the negative terminal of the photovoltaic array on the input side of the circuit is connected to the negative terminal of the output side load to form a double-ended common ground inverter topology. Analysis shows that this type of topology can achieve the effect of completely suppressing the leakage current by realizing a constant common-mode voltage. In one cycle, the inductance must experience a current discontinuous or
continuous state, which means the output current will be distorted at the zero-crossing point. Therefore, this topology ensures a standard output waveform by connecting a diode in series on the input inductor side, while ensuring that the power supply achieves unidirectional conductivity. At the same time, due to the existence of the front-end circuit and capacitor, the problem that the gain of this type of circuit is less than 1 can be solved. Moreover, the circuit structure is simple, including only four switches. Therefore, under the premise of ensuring a simple circuit structure, the proposed converter achieves the leakage current elimination, as well as the step-up voltage capability.

In order to theoretically support the above-mentioned novelty and contribution of the article, the theoretical analysis is conducted as follows. First of all, the leakage current is relevant to the parasitic capacitance and the voltage across it, which is determined by the common mode voltage [19].

As shown in Figure 2, the leakage current through the parasitic capacitance of $C_{pv}$ is related to the common-mode voltage of $U_{CM}$. By neglecting the impact of the grid voltage, the following equation can be obtained.

$$i = C_{pv} \frac{dU_{CM}}{dt}$$  \hspace{1cm} (1)

![Figure 2. Theoretical model of Leakage current generation.](image)

In the conventional H4 converter, the common-mode voltage is time-varying [20], and the leakage current is high. That is why different interesting converters such H5, H6, and Heric are proposed to reduce the leakage current. The idea behind these converters is based on the control algorithm that the common-mode voltage is regulated to be constant. In this way, the leakage current would be zero theoretically, as predicted by Equation (1). However, the impact of the grid voltage cannot be ignored in practice. Therefore, the new method should be further investigated. It should be noted that the proposed converter in this paper has the unique feature that the terminal A of input is connected to that B of output, as shown in Figure 1. That is, the voltage $U_{CPV}$ across the parasitic capacitance of $C_{pv}$ is zero. According to $i = C_{pv}(dU_{CPV}/dt)$, the proposed converter achieves the leakage current elimination.

2.2. Modulation

The inverter circuit adopts the SPWM modulation method. The modulation method is shown in Figure 3a. $d_1$ is switch $S_1$ modulation wave, $d_3$ is switch $S_3$ modulation wave, and $d_1$ and $d_3$ are two modulation waves with the same amplitude and 180° phase difference. The carrier is a triangular carrier with a carrier of 0 to 1. The volt-second balance expression for the inductance $L_1$ column in one cycle is:

$$V_{in}d_3T_s + (V_{in} - V_{c1})d_{L_1} = 0$$  \hspace{1cm} (2)
Among them, \( V_{C1} \) is the voltage across the capacitor \( C_1 \), is \( d_3 \) the duty cycle of switch \( S_3 \), \( d_{11} \) and is the time of the inductor \( L_1 \) in the discharge cycle. From this topology, it can be known that the inductor \( L_1 \) is working in an intermittent working state, and then is known \( d_{11} < (1 - d_3) T_s \).

When the load voltage is greater than zero in the positive half cycle, it can be seen from the working mode that the switches \( S_1 \) and \( S_3 \) are on at the same time. At this time, the capacitor \( C_1 \) is charged by the inductor \( L_1 \) and the input source. The voltage at both ends shows a trend of change.

The second modulation method is improved pulse width modulation. The modulation method is shown in Figure 3b, in which the driving signals of the switching \( S_2 \) and the switching \( S_1 \) are complementary, and the driving signals of the switching \( S_3 \) and the switching \( S_4 \) are complementary.

As can be seen from Figure 3b, \( M_a < (1 - M_1) \), \( M_a < M_2 \) and from the analysis of the inductor current diagram, in this modulation mode, when the load voltage is in the positive half cycle or the negative half cycle, only one inductor is in the intermittent working state, and \( M_a \) is the distance from \( M_1 \) to the highest point of modulating wave \( d_1 \).

It can be seen from the figure that the modulation wave of switch \( S_1 \) is consistent with the modulation wave in the SPWM modulation mode, and the modulation wave of switch \( S_3 \) is the offset of the amplitude \( M_1 \) and \( M_2 \), and \( d_1(t), d_3(t) \) the expression is:

\[
\begin{align*}
    d_1(t) &= \begin{cases} 
        M_a \sin \left( \frac{2 \pi t}{T_s} \right) + M_1, & 0 < t < \frac{T_s}{2} \\
        M_a \sin \left( \frac{2 \pi t}{T_s} \right) + M_2, & \frac{T_s}{2} < t < T_s 
    \end{cases} \\
    d_3(t) &= \begin{cases} 
        M_1, & 0 < t < \frac{T_s}{4} \\
        M_2, & 0 < t < \frac{3T_s}{4} 
    \end{cases}
\end{align*}
\]

2.3. Operating Mode

In order to ensure that this circuit has the principle of an inverter and boost performance, its working mode is now analyzed. It can be seen from the circuit structure that when switch \( S_1 \) is turned on, switch \( S_2 \) should be in the off state, and when switch \( S_3 \) is turned on, switch \( S_4 \) should be in the off state. In order to realize the standard inverter mode, there are only two switches each time. Each switch tube is turned on. It can be seen from the above that the circuit presents four working modes; in turn, the \( S_1 \) and \( S_2 \) are on, the \( S_2 \) and \( S_4 \) are off; the \( S_2 \) and \( S_3 \) are on, the \( S_1 \) and \( S_4 \) are off; the \( S_2 \) and \( S_4 \) are turned on, the \( S_1 \) and \( S_3 \) are off; the \( S_1 \) and \( S_4 \) are on, the \( S_2 \) and \( S_3 \) are off. Therefore, the driving signals of switch \( S_1 \) and switch \( S_2 \) are complementary, and the driving signals of switch \( S_3 \) and switch \( S_4 \) are complementary.

In addition, the working status of the switch is also specifically distinguished according to whether the load side voltage is a positive or negative half cycle. The details are as follows. When the load voltage is in the positive half cycle, the \( S_1 \) and \( S_3 \) are all on, and
switch $S_1$ is on, switch $S_3$ is off, and switches $S_1$ and $S_3$ are all off. When the load voltage is in the negative half cycle, switches $S_1$ and $S_3$ are all on, switch $S_1$ is off, switch $S_3$ is on, and switch $S_1$ and switch $S_3$ are all off. According to the above analysis, the working mode of the inverter circuit is shown in Figure 4. Due to the difference of the positive and negative half-cycle of the load voltage, there will be differences in the capacitor charging and discharging forms under the same switching mode. Now we will analyze it in detail.

Figure 4. Operation principle of different modes.

The working mode is as follows. When the load side voltage is in the positive half cycle, the inverter operating mode and the capacitor and inductor charging and discharging forms in the circuit are as follows, where $V_0$ is the load voltage, $V_{in}$ is the input voltage, and
$I_{C1}, I_{C2}$ is the voltage flowing through the capacitor $C_1$ and the capacitor $C_2$. The current $I_{L1}$ is the inductor current on the input side and the current $I_0$ on the load side.

Working mode 1: The switches $S_2$ and $S_4$ are kept in the on state, and the switches $S_1$ and $S_3$ are kept in the off state, as shown in Figure 4a. At this time, the inductor $L_1$ is discharged, and the capacitor $C_2$ is charged at this time. According to Kirchhoff’s law of voltage and current, this mode can be expressed by the following formula:

\[
\begin{align*}
V_{in} &= V_{L1} + V_{C1} \\
V_{C1} &= V_{C2} \\
I_{L1} &= I_{C1} + I_{C2} \\
I_{Lf} &= I_{Cf} + I_0
\end{align*}
\]

Working mode 2: The switches $S_1$ and $S_4$ are kept in the on state, and the switches $S_2$ and $S_3$ are kept in the off state, as shown in Figure 4b. The input source charges the capacitor $C_1$ through the inductor $L_1$, the input source charges the load side through switch $S_1$, and at the same time charges the capacitor $C_2$. According to Kirchhoff’s law of voltage and current, this mode can be expressed by the following formula:

\[
\begin{align*}
V_{in} &= V_{L1} + V_{C1} \\
V_{Lf} &= V_{C1} \\
V_{C1} &= V_{C2} \\
I_{L1} &= I_{C1} + I_{Lf} + I_{C2} \\
I_{Lf} &= I_{Cf} + I_0
\end{align*}
\]

Working mode 3: The switches $S_1$ and $S_3$ are kept in the on state, and the switches $S_2$ and $S_4$ are kept in the off state, as shown in Figure 4d. The input source charges the inductor $L_1$ through switch $S_3$ and diode $D_1$, and capacitor $C_1$ charges the load side at this time. At this time, the inductor $L_1$ is in a charged state, and the capacitor $C_1$ is in a discharged state. According to Kirchhoff’s voltage and current law, this mode can be represented as:

\[
\begin{align*}
V_{in} &= V_{L1} \\
V_{Lf} &= V_0 \\
I_{C1} &= I_{Lf} \\
I_{Lf} &= I_{Cf} + I_0
\end{align*}
\]

When the load side voltage is in the negative half cycle, the working mode of the circuit and the charging and discharging forms of the capacitors and inductors in the circuit are as follows:

Working mode 1: The switches $S_2$ and $S_4$ remain in the on state, and the switches $S_1$ and $S_3$ remain in the off state, as shown in Figure 4a. At this time, the inductor $L_1$ is in a discharged state, and the capacitor $C_2$ is in a discharged state. In this working mode, the loop voltage and current expressions are consistent with the load voltage in the positive half cycle.

Working mode 2: The switches $S_2$ and $S_3$ are kept in the on state, and the switches $S_1$ and $S_4$ are kept in the off state, as shown in Figure 4c. At this time, the inductor $L_1$ is in a charged state, and the capacitors $C_1$ and $C_2$ are in a discharged state. According to Kirchhoff’s law of voltage and current, this mode can be expressed by the following formula:

\[
\begin{align*}
V_{in} &= V_{L1} \\
V_{C1} &= V_{Lf} + V_0 \\
I_{Lf} &= I_{Cf} + I_0
\end{align*}
\]
Working mode 3: The switches $S_1$ and $S_3$ remain in the on state, and the switches $S_2$ and $S_4$ remain in the off state, as shown in Figure 4d. At this time, the inductor $L_1$ is in a charged state, and the capacitor $C_1$ is in a discharged state. In this working mode, the loop voltage and current expressions are consistent with the load voltage in the positive half cycle.

2.4. Parameter Design

According to the above analysis of the working mode, the inductor $L_1$ is charged by the input power. By combining the expression in the working mode and the inductor voltage expression, the current ripple of the inductor $L_1$ can be calculated, and the ripple expression is:

$$\Delta i_{L_1} = \frac{V_{in}d_3T_s}{L_1}$$

(12)

Among them, $d_3$, $\Delta i_{L_1}$ represents the on-time of switch $S_3$, the current ripple of the inductor $L_1$, and a switching cycle time. Therefore, the inductance $L_1$ can be obtained by the following formula:

$$L_1 = \frac{V_{in}d_3T_s}{\Delta i_{L_1}}$$

(13)

According to the above-mentioned working mode analysis and loop expression, the voltage ripple of the capacitors $C_1$ and $C_2$ is affected by the current of the inductor $L_1$ and the duty cycle of switch $S_3$ and switch $S_4$. Therefore, the capacitance calculation formula is:

$$\begin{cases}
C_1 = \frac{i_{i_t}d_3T_s}{\Delta V_{C_1}} \\
C_2 = \frac{i_{i_t}d_4T_s}{\Delta V_{C_2}}
\end{cases}$$

(14)

Among them, $\Delta V_{C_1}, \Delta V_{C_2}$ are the voltage ripples of capacitors $C_1$ and $C_2$, respectively. Through the above analysis, in the simulation and experiment, the inductance $L_1$ is set to $5 \, mH$, the capacitor $C_1$ is set to $30 \, \mu F$, and the capacitor $C_2$ is set to $50 \, \mu F$.

2.5. Comparative Study

Table 1 shows the comparative study of the proposed converter against the existing non-isolated converter with the leakage current suppression capability.

| Topology            | Switch | Step-Up Capability | Leakage Current |
|---------------------|--------|--------------------|-----------------|
| H4 + boost converter| 5      | Yes                | High            |
| H5 converter        | 5      | No                 | Small           |
| H6 converter        | 6      | No                 | Small           |
| ohH5 converter      | 6      | No                 | Very Small      |
| Proposed converter  | 4      | Yes                | Zero            |

From Table 1, it can be observed that the conventional H4 + boost converter has five switches with step-up voltage capability. However, the leakage current is high, which limits its application in a non-isolated PV system. For H5 and H6 converters, the number of switches is 5 and 6, respectively, but they are not able to achieve the step-up voltage capability. Compared to H5 and H6 converters, the leakage current is smaller, due to the clamped switch during the switching commutation. Nevertheless, it needs 6 switches to achieve it for ohH5 converter. In addition, it has no step-up voltage capability. For the proposed converter, it only needs four switches. Meanwhile, it has the step-up voltage capability. Aside from that, the leakage current is zero, due to the fact that the terminal of input is connected to that of the output. In summary, the proposed converter has the advantages of fewer switches, zero leakage current, as well as step-up voltage capability.
3. Simulation Results

In order to verify the feasibility of the proposed inverter, the time-domain simulation is carried out in MATLAB/Simulink. The simulation parameters are shown in Table 2. In the simulation, the input voltage is designed to be 70 V, and the output voltage RMS value is 110 V. In order to facilitate the design of the experimental device parameters, in the design and selection of the inductive capacitor device parameters, the value of the inductor current ripple is set to $\Delta i_L = 20\% i_L$ and the voltage ripple is set as $\Delta V_C = 7\% V_C$. The calculation of the inductance and capacitance value is based on the parameter design part of the previous section.

Table 2. Simulation parameters.

| Parameter      | Values |
|----------------|--------|
| Input voltage $V_{in}$ | 70 V   |
| Output voltage RMS         | 110 V/50 Hz |
| Input inductance $L_1$     | 5 mH   |
| Capacitance $C_1$          | 30 µF  |
| Capacitance $C_2$          | 50 µF  |
| Capacitance $C_f$          | 20 µF  |
| Inductance $L_f$           | 2 mH   |

Figure 5 shows the output current waveform, output voltage waveform, and FFT analysis of the proposed inverter circuit. The RMS value of the output voltage is 110 V, and the RMS of the output current is 1.1 A. Through fast Fourier analysis (FFT) analysis, THD = 2.53%, less than 5%, meet the design requirements. Figure 6 shows the voltage stress waveforms of switch $S_1$, switch $S_2$, switch $S_3$, and switch $S_4$, and the current stress waveform diagrams of switch $S_1$ and switch $S_4$. The switch voltage stress is about 320 V, and the current stress is less than 12 A. When selecting the switch, considering the voltage and current margin twice, the switch withstand voltage is higher than 640 V and the withstand current is higher than 24 A, so the model produced by Infineon is 1KW40T1202, and its collector and emitter can withstand 1200 V with DC voltage and the current withstand capability can reach 40 A, which meets the requirements of the experimental design.

![Figure 5](image_url)

(a) The output voltage

![Figure 5](image_url)

(b) The output current

Figure 5. Cont.
Figure 5. Simulation results of output voltage and current.

Figure 6. Voltage wave of (a) switch $S_1$, (b) switch $S_2$, (c) switch $S_3$, and (d) switch $S_4$ and the current wave of (e) switch $S_1$ (f) switch $S_4$.

4. Experimental Results

In order to further verify the effectiveness of the inverter circuit, an experimental platform was built for it, and experimental verification was carried out. In the experiment, the input voltage was maintained at 70 V, and the load was 100 $\Omega$. In order to meet the actual experimental environment requirements, the switch tubes were all selected as 1KWK40T1202 IGBTs.

First, the inverter circuit was tested under a 70 V input voltage. Figure 7a shows the voltage and current stress waveforms of switch $S_1$ when the effective value of the output voltage is 110 V. Figure 7b shows the voltage and current stress waveforms of switch $S_4$. Due to the characteristics of the circuit structure, the stresses of switch $S_3$ and switch $S_4$ are similar. Figure 7c is the output voltage waveform and the output current waveform and the voltage stress waveform of switch $S_2$. Figure 7d is the voltage and current stress waveform of the capacitor $C_2$, which can be seen from the figure. The experimental results
are in agreement with the simulation results, and the circuit gain can reach 2.2 times at this time.
In order to further verify the effectiveness of the proposed inverter under the input voltage variation, the input voltage is increased to 100 V. The experimental results are shown in Figure 8. Figure 8a shows the voltage and current stress waveform at both ends of switch S1, and Figure 8b is switch S4. Figure 8c shows the voltage and current waveforms at both ends of the inductor L1. Figure 8d shows the voltage and current waveforms at both ends of the capacitor C2. The above waveform shows that the circuit gain can reach 1.55 times at this time, which again verifies the effectiveness of the proposed converter.

Figure 8. Experimental results in the case of an input of 100 V.
5. Conclusions

This paper has presented a new non-isolated dual-grounded converter. The leakage current can be eliminated by the dual-ground structure of the converter, that is, the input terminal is connected to the output negative terminal. In addition, the converter can achieve the step-up voltage even with the input voltage variation. Experimental verification is also provided to verify the effectiveness of the proposal in this paper. In summary, compared with the existing methods, the proposed converter is simple with less switches, and the modulation is easy to implement. Aside from that, the leakage current is eliminated with step-up voltage capability. Therefore, it is attractive for non-isolated PV systems.

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