Frequency Measurement Device With Reconfigurable Bandwidth and Resolution

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Abstract—This letter presents a low-cost and compact reconfigurable frequency measurement circuit able to reconfigure bandwidth and resolution, the design uses a varactor loaded phase shifter, a reference delay line, and power divider/combiner to form a 2-bit frequency discriminator with four states for frequency measurement. The reconfigurable discriminator has four bandwidth states of 0.5, 0.9, 1.3, and 1.7 GHz, with uniform subband resolution of 125, 225, 325, and 525 MHz, for each bandwidth state of operation, respectively.

Index Terms—Delay line, frequency discriminator, frequency measurement, varactor loaded phase shifter.

I. INTRODUCTION

COLLECTING enemy communication or radar information remotely in the battlefield is important to gain the upper hand. Unknown frequency signals can be identified by binary encoding a fixed frequency band, resulting in the creation of frequency subbands used to detect unknown signals.

Early frequency measurement solutions have been incorporated in the electronic warfare systems, such as radar monitoring, weapon guidance, and communications, but the applications of frequency detection go far beyond, including unmanned aerial vehicles, signal intelligence, electronic intelligence, electronic support measures, and automated test equipment [1].

Frequency measurement receivers can be classified into two types: fixed and reconfigurable designs. The fixed instantaneous frequency measurement systems are based on a topology where the number of frequency discriminator circuits defines the resolution at the circuit output, where 1 bit per discriminator is obtained. Thus, the input signal is divided using a power divider network, where each signal part flows through a given discriminator, defining the bits used for frequency identification [2]–[4]. The reconfigurable frequency measurement systems use a switching circuit to send the input signal through a switched delay line bank, producing 1 bit at a time [5]–[7]. In both the fixed and reconfigurable designs, the output signal is sent to an analog-to-digital (A/D) converter to obtain the bit information used for frequency measurement. The reconfigurable designs present some advantages compared with the fixed designs, such as reduced size, the use of fewer components and two ports only, and reducing the overall power consumption of the frequency measurement system. On the other hand, the reconfigurable systems require a switching time, featuring them as noninstantaneous circuits [1].

The proposed reconfigurable discriminators in [5]–[7] require a switchable delay line per bit, where the delay line paths are selected using p-i-n diodes, and the response time depends on the p-i-n diode switching speed, when commuting between the bits used for frequency measurement.

This work reports the development of a very compact reconfigurable frequency measurement circuit without switchable delay lines, suitable for a low-power consumption reconfigurable frequency measurement system, adequate for class I unmanned aerial vehicle reconnaissance missions. The proposed device uses the mutual interference between the varactor loaded delay line and the reference line to perform frequency identification, with both signal paths having approximately the same physical length. This design aims to reduce the weight and the size of multiplexed frequency discriminators [1]–[4], and further miniature the reconfigurable designs based on p-i-n diodes [5]–[7]. The toggle switching time of the device is defined by the time constant of the bias circuit only, since the varactor diodes do not exhibit hysteresis and can be used for high tuning speeds, compared with the p-i-n diode-based designs [5]–[7].

The design uses a reconfigurable phase shifter to substitute the traditional switched delay line banks used in [5]–[7], resulting in a compact and reconfigurable low-cost implementation.

II. FREQUENCY MEASUREMENT USING A VARIATOR LOADED PHASE SHIFTER

Fig. 1(a) shows the frequency measurement system schematic, comprising electronic devices such as limiting amplifier to keep a constant unknown signal input power, frequency discriminator to determine the frequency identification resolution, RF detector to convert the signal power to a voltage signal, and A/D converter to provide a binary digital output. Fig. 1(b) shows the proposed reconfigurable discriminator,
comprising a power divider, reference line, phase shifter, and power combiner. The relative phase difference between the phase shifter and the reference line enables the use of 2 bits for frequency identification, adaptable to four different bandwidths of operation, each with a well-defined and uniform subband resolution. A 500-$\mu$m-thick FR-4 substrate with 50-$\mu$m-thick copper is used to make the device. The characteristic impedance of the power divider and the combiner is matched to 50-$\Omega$ and has a frequency of operation from 1 to 3 GHz. Fig. 2 shows a three-step $\pi$ filter performing as a reconfigurable phase shifter, designed using a 1.5-nH inductor in parallel with two varactors having a variable capacitance in the range from 0.52 to 0.88 pF. Adjusting the varactor diode capacitance, according to the reverse bias voltage applied to the diode, results in signal phase reconfiguration. The phase of the reconfigurable phase shifter is designed to decrease from 540$^\circ$ to 390$^\circ$ at 3 GHz, as the applied voltage increases from 7 ($C_j = 0.88$ pF) to 12 V ($C_j = 0.48$ pF). The dc bias circuit uses a resistor to avoid microwave or radio frequency signal leakage through the dc bias circuit. A series capacitor is used as a dc block, placed along the phase shifter. Table I provides the reconfigurable phase shifter parameters used in the proposed design.

### TABLE I
**PHASE SHIFTER DESIGN PARAMETERS**

| Parameters     | Value          |
|----------------|----------------|
| $R$            | 2.5 M$\Omega$  |
| $L$            | 1.5 nH         |
| $C$            | 100 pF         |
| $C_j$          | 0.48–0.88 pF   |
| Phase shift @ 3 GHz | 390–540$^\circ$ |

Fig. 3 shows the fabricated reconfigurable frequency discriminator, with two RF ports and cables used to provide dc bias to the varactor diodes. The size of the fabricated frequency discriminator is 51 $\times$ 72 mm$^2$ and the size without including the bulky dc bias circuit is 25 $\times$ 72 mm$^2$. This frequency discriminator is compact since it does not require multiple power division [1]–[4], NOR switched delay lines [5]–[7]. The measurements are obtained using an Agilent HP 8735-D vector network analyzer, after an SOLT calibration. Figs. 4 and 5 show the measured $S_{21}$ magnitude according to the voltage applied to the varactor diodes. (a) 7 and 8 V. (b) 7 and 9 V.

### III. EXPERIMENTAL RESULTS

Fig. 3 shows the fabricated reconfigurable frequency discriminator, with two RF ports and cables used to provide dc bias to the varactor diodes. The size of the fabricated frequency discriminator is 51 $\times$ 72 mm$^2$ and the size without including the bulky dc bias circuit is 25 $\times$ 72 mm$^2$. This frequency discriminator is compact since it does not require multiple power division [1]–[4], NOR switched delay lines [5]–[7]. The measurements are obtained using an Agilent HP 8735-D vector network analyzer, after an SOLT calibration. Figs. 4 and 5 show the measured $S_{21}$ magnitude according to the voltage applied to the varactor diodes. The reconfigurable
frequency measurement device can be used to produce four bandwidth states with uniform subband resolution, according to the varactor diode bias. The initial dc voltage for all the four states is 7 V, represented as a black curve in Figs. 4 and 5. The colored regions (red, yellow, green, and blue) represent the four frequency subbands used for frequency identification, according to the binary code used for frequency identification, provided below each frequency response in Figs. 4 and 5. To provide the 2-bit digital output, the threshold level is determined to divide the operational bandwidth into four subbands for frequency identification, having the same resolution.

The first state of operation produces 2 bits for frequency identification in the 1.8–2.3-GHz frequency band, considering an A/D conversion threshold at −18 dB, as shown in Fig. 4(a); the two states are produced when a dc bias voltage is toggled between 7 and 8 V, and the designed subband resolution is 125 MHz, where a maximum deviation of 5 MHz has been found through measurements, with a standard deviation (σ) of 5.7 MHz.

Fig. 4(b) shows the \( S_{21} \) response of the reconfigurable discriminator circuit when the dc bias voltage provided to the varactors is varied from 7 to 9 V, with an A/D conversion threshold at −14 dB; the frequency response of the discriminator has a bandwidth for frequency identification from 1.6 to 2.5 GHz, with a subband resolution of 225 MHz, where the maximum deviation found is 25 MHz, with σ of 19.1 MHz.

Fig. 5(a) shows the \( S_{21} \) response when the dc bias voltage provided to the varactors is switched between 7 and 10 V, with an A/D conversion threshold at −11 dB. The bandwidth for frequency identification goes from 1.4 to 2.7 GHz, with a sub-band resolution of 325 MHz, where the maximum deviation found is 25 MHz, with σ of 23.8 MHz.

The response shown in Fig. 5(b) corresponds to the varactor diode dc bias voltages of 7 and 12 V, with an A/D threshold of −9 dB. The bandwidth used for frequency identification goes from 1.2 to 2.9 GHz and the subband resolution is 425 MHz, with a maximum deviation of 35 MHz and σ of 35.1 MHz.

The proposed frequency discriminator requires toggling between two voltages to identify the subband where the unknown signal falls into. Therefore, frequency measurement is non-instantaneous, compared with instantaneous designs that use a discriminator per bit in a multiplexed design [1]–[4]. The proposed design requires as much as toggling the bias voltage eight times to search for an unknown signal throughout all the subbands of the design (see Figs. 4 and 5). The proposed frequency discriminator is a compact, two-port device with variable bandwidth and resolution defined by the bias voltage applied to the varactor diodes.

IV. CONCLUSION

This letter describes a low-cost reconfigurable frequency measurement discriminator implementation that does not require switched delay lines or electronic components by bit to form a frequency measurement system. The design is compact and reconfigured by varying the dc bias voltage applied to the varactor diodes, used to load a reconfigurable delay line. The reconfigurable frequency discriminator is proposed for low-power consumption frequency measurement systems with reduced size and low weight.

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