On Register Linearizability and Termination

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Abstract

It is well-known that, for deterministic algorithms, linearizable objects can be used as if they were atomic objects. As pointed out by Golab, Higham, and Woelfel, however, a randomized algorithm that works with atomic objects may lose some of its properties if we replace the atomic objects that it uses with objects that are only linearizable. It was not known whether the properties that can be lost include the all-important property of termination (with probability 1). In this paper, we first show that a randomized algorithm can indeed lose its termination property if we replace the atomic registers that it uses with linearizable ones.

Golab et al. also introduced strong linearizability, and proved that strongly linearizable objects can be used as if they were atomic objects, even for randomized algorithms: they can replace atomic objects while preserving the algorithm’s correctness properties, including termination. Unfortunately, there are important cases where strong linearizability is impossible to achieve. In particular, Helmi, Higham, and Woelfel showed a large class of “non-trivial” objects, including MWMR registers, do not have strongly linearizable implementations from SWMR registers.

Thus we propose a new type of register linearizability, called write strongly-linearizability, that is strictly stronger than (plain) linearizability but strictly weaker than strong linearizability. This intermediate type of linearizability has some desirable properties. We prove that some randomized algorithms that fail to terminate with linearizable registers, work with write strongly-linearizable ones. In other words, there are cases where linearizability is not sufficient but write strong-linearizability is. In contrast to the impossibility result mentioned above, we prove that write strongly-linearizable MWMR registers are implementable from SWMR registers. Achieving write strong-linearizability, however, is harder than achieving just linearizability: we give a simple implementation of MWMR registers from SWMR registers and we prove that this implementation is linearizable but not write strongly-linearizable. Finally, we prove that any linearizable implementation of SWMR registers is necessarily write strongly-linearizable; this holds for shared-memory, message-passing, and hybrid systems.

1 Introduction

Linearizability is a well-known and very useful property of shared object implementations [24]. Intuitively, with a linearizable (implementation of) object each operation must appear as if it takes effect instantaneously at some point during the time interval that it actually spans; for deterministic algorithms linearizable objects can be used as if they were atomic. As pointed out by the seminal work of Golab et al. [19], however, linearizable objects are not as strong as atomic objects in the following sense: a randomized algorithm that works with atomic objects may lose some of its properties if we replace the atomic objects that it uses with objects that are only linearizable. In particular, they present a randomized algorithm that guarantees that some random variable has expected value 1, but if we replace the algorithm’s atomic registers with linearizable registers, a strong adversary can manipulate schedules to ensure that this random variable has expected value $\frac{1}{4}$.

Throughout the paper we consider only implementations that are wait free [23].
1.1 Linearizability and termination

A natural question is whether termination is one of the properties that can be lost with the use of linearizable objects. More precisely: is there a randomized algorithm that (a) terminates with probability 1 against a strong adversary when the objects that it uses are atomic, but (b) when these objects are replaced with linearizable objects, a strong adversary can ensure that the algorithm never terminates? This question is particularly interesting because achieving termination is one of the main uses of randomized algorithms (e.g., to “circumvent” the famous FLP impossibility result [18] [19] [20] [21] [22], but it is not answered by the results in [19], and to the best of our knowledge, it is also not addressed in subsequent papers on this subject [14] [17] [22].

In this paper, among other things, we show that termination can be lost. Specifically, we give a randomized algorithm that uses registers such that: (1) if these registers are atomic then the algorithm terminates, i.e., all the processes halt, with probability 1, even against a strong adversary, and (2) if the registers are “only” linearizable, a strong adversary can prevent termination: it can always manipulate schedules so that processes never halt.

1.2 Strong linearizability

Golab et al. also introduced a stronger version of linearizability called strong linearizability [19]. Intuitively, while in linearizability the order of all operations can be determined “off-line” given the entire execution, in strong linearizability the order of all operations has to be fixed irrevocably “on-line” without knowing the rest of the execution. Golab et al. proved that strongly linearizable (implementations of) objects are “as good” as atomic objects, even for randomized algorithms: they can replace atomic objects while preserving the algorithm’s correctness properties including termination with probability 1. Unfortunately, there are important cases where strong linearizability is impossible to achieve.

For example, Helmi et al. proved that a large class of so-called non-trivial objects, including multi-writer multi-reader (MWMR) registers, do not have strongly linearizable implementations from single-writer multi-reader (SWMR) registers [22]. This impossibility result may affect many existing randomized algorithms (e.g.,[2 3 4 5 6 9]): these algorithms use atomic MWMR registers, so if we want to run them in systems with SWMR registers we cannot hope to automatically do so just by replacing their atomic MWMR registers with strongly linearizable implementations from SWMR registers.

Similarly, consider the well-known ABD algorithm that implements linearizable SWMR registers in message-passing systems [12] [13]. One important use of this algorithm is to relate message-passing and shared-memory systems as follows: any algorithm that works with atomic shared registers can be automatically transformed into an algorithm for message-passing systems by replacing its atomic registers with the ABD register implementation. It has been recently shown, however, that the ABD register implementation is not strongly linearizable [20]. Thus one cannot use the ABD implementation to automatically transform any shared-memory randomized algorithm that terminates with probability 1 into an algorithm that works in message-passing systems: using the ABD register implementation instead of atomic registers in a randomized algorithm may prevent termination.

1.3 Write strong-linearizability

Motivated by the impossibility of implementing strongly linearizable registers mentioned above, we propose a new type of register linearizability, called write strong-linearizability, that is strictly stronger than (plain) linearizability but strictly weaker than strong linearizability. Intuitively, while in strong linearizability the order of all operations has to be fixed irrevocably “on-line” without knowing the rest of the execution, in write strong-linearizability only the write operations must be ordered “on-line”. This intermediate type of linearizability has some desirable properties, as described below:

- In some cases where linearizability is not sufficient to achieve termination, write strong-linearizability is. To show this, we describe a randomized algorithm such that if the registers of this algorithm are only linearizable, then a strong adversary can prevent its termination; but if they are write strongly-linearizable, then the algorithm terminates with probability 1 (Section 3).
We then generalize this result as follows: for every randomized algorithm \( A \) that solves a task \( T \) and terminates with probability 1 against a strong adversary, there is a corresponding randomized algorithm \( A' \) for task \( T \) such that: (a) if the registers that \( A' \) uses are only linearizable, \( A' \) does not terminate, but (b) if they are write strongly-linearizable, \( A' \) terminates.

• In contrast to the impossibility result proved in [22], write strongly-linearizable MWMR registers are implementable from SWMR registers. To prove this we modify a known implementation of MWMR registers [26], and we linearize the write operations “on-line” by using vector timestamps that may be only partially formed (Section 4).

Achieving write strong-linearizability, however, is harder than achieving just linearizability. We give a simpler implementation of MWMR registers from SWMR registers that uses Lamport clocks to timestamp writes [25], and we prove that this implementation is linearizable but not write strongly-linearizable (Section 5).

• Although the ABD implementation of SWMR registers is not strongly linearizable, we show that it is actually write strongly-linearizable. In fact, we prove that any linearizable implementation of SWMR registers is necessarily write strongly-linearizable; this holds for message-passing, shared-memory, and hybrid systems (Section 6).

Finally, it is worth noting that even though we focus on registers here, our intermediate notion of linearizability can be extended to other types of objects and operations. Intuitively, an implementation of an object is strongly linearizable with respect to a subset of operations \( O \) if the order of all operations in \( O \) must be fixed irrevocably “on-line” without knowing the rest of the execution.

All the results presented are proven in this paper, but due to the space limitation several proofs are relegated to optional appendices.

2 Model sketch

We consider a standard distributed system where asynchronous processes that may fail by crashing communicate via registers and other shared objects. In such systems, shared objects can be used to implement other shared objects such that the implemented objects are linearizable and wait-free [23, 24].

2.1 Atomic registers

A register \( R \) is atomic if its read and write operations are instantaneous (i.e., indivisible); each read must return the value of the last write that precedes it, or the initial value of \( R \) if no such write exists. A SWMR register \( R \) is shared by a set \( S \) of processes such that it can be written (sequentially) by exactly one process \( w \in S \) and can be read by all processes in \( S \); we say that \( w \) is the writer of \( R \) [25]. A MWMR register \( R \) is shared by a set \( S \) of processes such that it can be written and read by all processes in \( S \).

2.2 Linearizable implementations of registers

In an object implementation, each operation spans an interval that starts with an invocation and terminates with a response.

Definition 1. Let \( o \) and \( o' \) be any two operations.

• \( o \) precedes \( o' \) if the response of \( o \) occurs before the invocation of \( o' \).

• \( o \) is concurrent with \( o' \) if neither precedes the other.

Roughly speaking, an object implementation is linearizable [24] if, although operations can be concurrent, operations behave as if they occur in a sequential order (called “linearization order”) that is consistent with the order in which operations actually occur: if an operation \( o \) precedes an operation \( o' \), then \( o \) is before \( o' \) in the linearization order (the precise definition is given in [24]).

Let \( \mathcal{H} \) be the set of histories of a register implementation. An operation \( o \) is complete in a history \( H \in \mathcal{H} \) if \( H \) contains both the invocation and response of \( o \), otherwise \( o \) is pending.
Definition 2. A function \( f \) is a linearization function for \( H \) (with respect to the type register) if it maps each history \( H \in \mathcal{H} \) to a sequential history \( f(H) \) such that:

1. \( f(H) \) contains all completed operations of \( H \) and possibly some non-completed ones (with matching responses added).

2. If operation \( o \) precedes \( o' \) in \( H \), then \( o \) occurs before \( o' \) in \( f(H) \).

3. For any read operation \( r \) in \( f(H) \), if no write operation occurs before \( r \) in \( f(H) \), then \( r \) reads the initial value of the register; otherwise, \( r \) reads the value written by the last write operation that occurs before \( r \) in \( f(H) \).

Definition 3. A function \( f \) is a strong linearization function for \( H \) if:

- (L) \( f \) is a linearization function for \( H \), and
- (P) for any histories \( G, H \in \mathcal{H} \), if \( G \) is a prefix of \( H \), then \( f(G) \) is a prefix of \( f(H) \).

By restricting the strong linearization requirement, i.e., property (P) to write operations only, we define the following:

Definition 4. A function \( f \) is a write strongly-linearization function for \( H \) if:

- (L) \( f \) is a linearization function for \( H \), and
- (P) for any histories \( G, H \in \mathcal{H} \), if \( G \) is a prefix of \( H \), then the sequence of write operations in \( f(G) \) is a prefix of the sequence of write operations in \( f(H) \).

Definition 5. An algorithm \( A \) that implements a register is linearizable, write strongly-linearizable, or strong linearizable, if there is a linearization, write strongly-linearization, or strong linearization function (with respect to the type register) for the set of histories \( \mathcal{H} \) of \( A \).

3 Termination under linearizability and write strong-linearizability

In this section, we show that in some cases linearizability is not sufficient for termination but write strong-linearizability is. To do so, we present a randomized algorithm, namely Algorithm 1 and prove that (a) it fails to terminate if its registers are only linearizable but (b) it terminates if they are write strongly-linearizable. We then use Algorithm 1 to show that every randomized algorithm \( A \) that solves a task and terminates with probability 1 against a strong adversary, has a corresponding randomized algorithm \( A' \) for the same task such that: (a) if the registers that \( A' \) uses are linearizable, \( A' \) does not terminate, but (b) if they are write strongly-linearizable, \( A' \) terminates.

Algorithm 1 uses three MWMR registers \( R_1, R_2, \) and \( C \). It can be viewed as a game executed by \( n \geq 3 \) processes, which are partitioned into two groups: the “hosts” \( p_0 \) and \( p_1 \) and the “players” \( p_2, \ldots, p_n \). The game proceeds in asynchronous rounds, each round consisting of two phases. In Phase 1 of a round \( j \), process \( p_1 \) writes \([1, j]\) into \( R_1 \); while \( p_0 \) first writes \( [0, j] \) in \( R_1 \), and then it writes the result of a 0-1 coin flip into \( C \) (lines 3-7). After doing so, each of \( p_0 \) and \( p_1 \) proceeds to Phase 2.

In Phase 1, each player \( p_i \) \((2 \leq i \leq n-1)\) reads \( R_1 \) twice (lines 21-22), and then it reads \( C \) (line 23). If \( p_i \) reads \( c \in \{0, 1\} \) from \( C \) and the sequence of two values that it read from \( R_1 \) is \([c, j]\) and then \([1-c, j]\), \( p_i \) proceeds to Phase 2, otherwise it exits the game (lines 24-29). Every player \( p_i \) that stays in the game resets \( R_2 \) to 0 (line 31) and tries to increment it by 1 (lines 32-34); thus \( R_2 \) holds a lower bound on the number of players that enter Phase 2. After doing so \( p_1 \) proceeds to the next round.

In Phase 2, each host \( p_0 \) and \( p_1 \) first resets \( R_2 \) to 0 (line 10) and then reads \( R_2 \) (line 11). If a host sees that \( R_2 \geq n-2 \) then it is certain that all the players remained in the game, and so it also remains in the game by proceeding to the next round; otherwise it exits the game.

We will show that if the registers are only linearizable, then a strong adversary \( S \) can manipulate schedules such that the game represented by Algorithm 1 continues forever; more precisely, regardless of the coin flip results, \( S \) can construct a run of Algorithm 1 in which all the processes loop forever (Theorem 6 in Section 3.1).

We then show that if the registers are write strongly-linearizable, then all the correct processes \( p_0 \) return from the algorithm with probability 1 (Theorem 7 in Section 3.2).

\(^3\)A process is correct if it takes infinitely many steps. We assume that processes continue to take steps (forever) even after returning from the algorithm in lines 10 or line 56.
Phase 1

Assume the registers of Algorithm 1 are only linearizable but Algorithm 1 where all the processes execute infinitely many rounds. If registers

Theorem 6.

3.1 Linearizability does not ensure termination

At high-level, the main idea of the proof is as follows. Assume the register \( R_1 \) is not atomic, so each of its operations spans an interval of time, and operations on \( R_1 \) can be concurrent. Consider the time \( t \) after \( p_0 \) flipped the coin (line 6). Suppose at that time \( t \), the write of \([1, j]\) into \( R_1 \) by \( p_1 \) is still pending and concurrent with the completed write of \([0, j]\) into \( R_1 \) by \( p_0 \).

If \( R_1 \) is linearizable, then adversary has the power to linearize the two writes in either order: \([0, j]\) before \([1, j]\), or \([1, j]\) before \([0, j]\). So based on the outcome \( c \) of the coin flip, the adversary can ensure that all the players read \([c, j]\) and then \([1 - c, j]\) from \( R_1 \) which forces them to stay in the game.

If, on the other hand, \( R_1 \) is write strongly-linearizable, the adversary does not have this power: at the time \( p_0 \) completes its write of \([0, j]\) into \( R_1 \) (and therefore before the adversary can see the result of the coin flip) the adversary must decide whether the concurrent write of \([1, j]\) by \( p_1 \) is linearized before \([0, j]\) or not. With probability at least 1/2, the result of the coin flip will not “match” this decision. So in each round, with probability at least 1/2, the players will not read \([c, j]\) and then \([1 - c, j]\) from \( R_1 \) and so they will exit the game. (Note that if \( R_1 \) is atomic, operations are instantaneous, and so of course the adversary has no power to continue the game forever.)

In Algorithm 1 only register \( R_1 \) is unbounded, but we can easily make \( R_1 \) bounded (see Appendix B).

3.1 Linearizability does not ensure termination

Theorem 6. If registers \( R_1, R_2, \) and \( C \) are only linearizable, a strong adversary \( S \) can construct a run of Algorithm 1 where all the processes execute infinitely many rounds.

Proof. Assume the registers of Algorithm 1 are only linearizable but not write strongly-linearizable. A strong adversary \( S \) can construct an infinite run of Algorithm 1 as follows (Figure 1):

Phase 1 (of round \( j = 1 \)):

1. Processes \( p_2, p_3, \ldots, p_{n-1} \) write \( \bot \) into \( R_1 \) and \( C \) in lines 19 and 20
2. At some time $t_0$ after all the above write operations are complete, process $p_0$ starts writing $[0,1]$ into $R_1$ in line 3. Process $p_1$ starts writing $[1,1]$ into $R_1$ in line 3 and processes $p_2, p_3, \ldots, p_{n-1}$ start reading $R_1$ in line 21.

3. At time $t_1 > t_0$, process $p_0$ completes its writing of $[0,1]$ into $R_1$ in line 3.

4. After time $t_1$, process $p_0$ flips a coin in line 6 and writes the result into the shared register $C$ in line 7.

Let $t_c > t_1$ be the time when $p_0$ completes this write of $C$. Depending on the result of $p_0$’s coin flip (and therefore the content of $C$), the adversary $S$ continues the run it is constructing in one of the following two ways:

**Case 1:** $C = 0$ at time $t_c$.

The continuation of the run in this case is shown at the top right of Figure 1.

(a) At time $t_2 > t_c$, $p_1$ completes its writing of $[1,1]$ into $R_1$ in line 3. Note that both $p_0$ and $p_1$ have now completed Phase 1 of round $j = 1$.

(b) The adversary $S$ linearizes the write of $[1,1]$ into $R_1$ by $p_1$ after the write of $[0,1]$ into $R_1$ by $p_0$.

(c) Note that $p_2, p_3, \ldots, p_{n-1}$ are still reading $R_1$ in line 21. Now the adversary linearizes these read operations between the above write of $[0,1]$ by $p_0$ and the write of $[1,1]$ by $p_1$.

(d) At time $t_3 > t_2$, processes $p_2, p_3, \ldots, p_{n-1}$ complete their read of $R_1$ in line 21. By the above linearization, they read $[0,1]$, and so they set (their local variable) $u_1 = [0,1]$ in line 21.

(e) Then processes $p_2, p_3, \ldots, p_{n-1}$ start and complete their read of $R_1$ in line 22. Since (1) these reads start after the time $t_2$ when $p_1$ completed its write of $[1,1]$ into $R_1$, and (2) this write is linearized after the write of $[0,1]$ by $p_0$ into $R_1$, processes $p_2, p_3, \ldots, p_{n-1}$ read $[1,1]$. So they all set (their local variable) $u_2 = [1,1]$ in line 22. Let $t_4 > t_3$ be the time when every process in \{ $p_2, p_3, \ldots, p_{n-1}$ \} has set $u_2 = [1,1]$ in line 22.

(f) After time $t_4$, processes $p_2, p_3, \ldots, p_{n-1}$ start reading $C$ in line 23. Since $C = 0$ at time $t_c$ and it is not modified thereafter, $p_2, p_3, \ldots, p_{n-1}$ read 0 and set (their local variable) $c = 0$ in line 23. So at this point, processes $p_2, p_3, \ldots, p_{n-1}$ have $u_1 = [0,1]$, $u_2 = [1,1]$ and $c = 0$.

(g) Then $p_2, p_3, \ldots, p_{n-1}$ execute line 24 and find that the condition ($u_1 = \perp$ or $u_2 = \perp$ or $c = \perp$) of this line does not hold, and so they proceed to execute line 27.

(h) When $p_2, p_3, \ldots, p_{n-1}$ execute line 27, they find that the condition ($u_1 \neq [c,j]$ or $u_2 \neq [1 - c,j]$) of this line does not hold, because they have $u_1 = [c,1] = [0,1]$ and $u_2 = [1 - c,1] = [1,1]$. 

![Figure 1: Phase 1 in round $j = 1$ of an infinite execution](image-url)
So \( p_2, p_3, \ldots, p_{n-1} \) complete Phase 1 of round \( j = 1 \) without exiting in line 28. Recall that both \( p_0 \) and \( p_1 \) also completed Phase 1 of round \( j = 1 \) without exiting.

**Case 2:** \( C = 1 \) at time \( t_0 \).

The continuation of the run in this case is shown at the bottom right of Figure 1. This continuation is symmetric to the one for Case 1: the key difference is that the adversary \( S \) now linearizes \( p_1 \)'s write of \([1, 1]\) into \( R_1 \) before \( p_0 \)'s write of \([0, 1]\) into \( R_1 \), and so processes \( p_2, p_3, \ldots, p_{n-1} \) have \( u_1 = \{c, 1\} = [1, 1] \) and \( u_2 = [1 - c, 1] = [0, 1] \) and so they will also complete Phase 1 without exiting in line 28.

Thus in both Case 1 and Case 2, all the \( n \) processes complete Phase 1 of round \( j = 1 \) without exiting, and are now poised to execute Phase 2 of this round. The adversary \( S \) extends the run that it built so far as follows (Figure 2).

**Phase 2** (of round \( j = 1 \)):

1. Processes \( p_0 \) and \( p_1 \) write 0 into \( R_2 \) in line 10 and processes \( p_2, p_3, \ldots, p_{n-1} \) write 0 into \( R_2 \) in line 31.

2. After all the above write operations complete, processes \( p_2, p_3, \ldots, p_{n-1} \) successively read and increment \( R_2 \) by executing lines 32–34 in the following order: \( p_2 \) executes lines 32 after \( p_1 \) completes its write of \( R_2 \) in line 31. Let \( t_0' \) be the time when the above \( n - 2 \) write operations by \( p_2, p_3, \ldots, p_{n-1} \) have completed.

   Note that at time \( t_0' \): (i) register \( R_2 \) contains \( n - 2 \), and (ii) all processes \( p_2, p_3, \ldots, p_{n-1} \) have completed Phase 2 of round \( j = 1 \).

3. After time \( t_0' \), \( p_0 \) and \( p_1 \) read \( R_2 \) into \( v \) in line 11 and so they set \( v = n - 2 \) in that line.

4. Then \( p_0 \) and \( p_1 \) execute line 12 and find that the condition “\( v < n - 2 \)” of this line does not hold. So \( p_0 \) and \( p_1 \) complete Phase 2 of round \( j = 1 \) without exiting in line 13.

   Thus all the \( n \) processes \( p_0, p_1, \ldots, p_{n-1} \), have completed Phase 2 of round 1 without exiting; they are now poised to execute round \( j = 2 \).

The adversary \( S \) continues to build the run by repeating the above scheduling of \( p_0, p_1, \ldots, p_{n-1} \) for rounds \( j = 2, 3, \ldots \). This gives a non-terminating run of Algorithm 1 with probability 1: in this run, all processes are correct, i.e., they take an infinite number of steps, but they loop forever and never reach the return statement in lines 16 or line 36.

\[\Box\]

### 3.2 Write Strong-Linearizability Ensures Termination

In Appendix A, we prove:

**Theorem 7.** If registers \( R_1, R_2, \) and \( C \) are write strongly-linearizable, then Algorithm 1 terminates with probability 1 against a strong adversary.

Combining Theorems 6 and 7 we have:
Corollary 8. If \( R_1, R_2, \) and \( C \) are

1. only linearizable, then a strong adversary can prevent the termination of Algorithm \([2]\)
2. write strongly-linearizable, then Algorithm \([2]\) terminates with probability 1 against a strong adversary.

Consider any randomized algorithm \( A \) that solves some task \( T \), such as consensus, for \( n \geq 3 \) processes \( p_0, p_1, p_2, \ldots, p_{n-1} \), and terminates with probability 1 against a strong adversary. Using \( A \), we can construct a corresponding randomized algorithm \( A' \) as follows: every process \( p_i \) with \( i \in \{0, 1, 2, \ldots, n-1\} \) first executes Algorithm \([2]\) if \( p_i \) returns then it executes algorithm \( A \). From Corollary \([8]\) we have:

Corollary 9. Let \( A \) be any randomized algorithm that solves a task \( T \) for \( n \geq 3 \) processes and terminates with probability 1 against a strong adversary. There is a corresponding randomized algorithm \( A' \) that solves \( T \) for \( n \geq 3 \) processes such that:

1. \( A' \) uses a set \( R \) of three shared registers in addition to the set of base objects of \( A \).
2. If the registers in \( R \) are only linearizable, then a strong adversary can prevent the termination of \( A' \).
3. If the registers in \( R \) are write strongly-linearizable, then \( A' \) terminates with probability 1 against a strong adversary.\([3]\)

4 Implementing write strongly-linearizable MWMR registers from SWMR registers

To implement a write strongly-linearizable MWMR register \( R \), we must be able to linearize all the write operations “on-line” without looking at what may happen in the future. The challenge is that at the moment \( t \) a write operation \( w \) completes, for each write \( w' \) that is concurrent with \( w \) and is still pending at time \( t \), we must have enough information to irrevocably decide whether \( w' \) should be linearized before or after \( w \); of course this linearization order must be consistent with the values that processes previously read and will read in the future from \( R \). Using simple “Lamport clocks” to timestamp and linearize write operations does not seem to work: in the next section, we give an implementation showing that Lamport clocks are sufficient to implement a linearizable MWMR register, but this implementation is not write strongly-linearizable.

In this section we give an implementation of a MWMR register from SWMR registers (Algorithm \([2]\)), and prove that it is write strongly-linearizable. This is a modification of an implementation given in \([26]\) and it uses vector clocks to timestamp write operations. The question is how to use vector timestamps to linearize write operations on-line. Specifically, at the moment \( t \) a write operation \( w \) completes, for each operation \( w' \) that is concurrent with \( w \) and still pending at time \( t \), how do we decide the order of \( w' \) with respect to \( w \)? Note that at time \( t \), while the vector timestamp of \( w \) is known, the vector timestamp of such \( w' \) may not be known: it is still being computed (it may be incomplete with just a few entries set). The proof of linearization given in \([26]\) does not work here; that proof can linearize all the write operations after seeing their complete vector timestamps; and it can do so because linearization is done “off-line”.

Algorithm \([2]\) uses SWMR registers \( \text{Val}[i] \) for \( i = 1, 2, \ldots, n \). Each write operation \( w \) is timestamped with a vector timestamp; roughly speaking, this represents the number of write operations that every process performed “causally before” \( w \). Each \( \text{Val}[k] \) contains the latest value that \( p_k \) wrote to \( R \) with its corresponding vector timestamp. To write a value \( v \) into \( R \), a process \( p_k \) first constructs a new timestamp \( \text{new}_{ts} \), incrementally one component at a time, by successively reading \( \text{Val}[1], \ldots, \text{Val}[n] \) (lines \([1],[2]\)); then \( p_k \) writes the tuple \((v, \text{new}_{ts})\) into \( \text{Val}[k] \) (line \([3]\)); finally \( p_k \) resets its \( \text{new}_{ts} \) to \([\infty, \ldots, \infty] \) (as we will see, this is important for the write strong-linearization). To read \( R \), a process \( p \) first reads all \( \text{Val}[1], \ldots, \text{Val}[n] \) (lines \([11],[13]\)); then \( p \) returns the value \( v \) with the greatest vector timestamp in lexicographic order \( \leq \) (lines \([14],[15]\)). Note that this is a total order.

We now prove that this MWMR implementation is indeed write strongly-linearizable. Before we do so, we first illustrate the problem that we mentioned earlier, namely, how to linearize write operations on-line based on incomplete vector timestamps, and then we give some intuition on how this problem is solved.

\(^4\) \( A' \) also terminates if the registers in \( R \) are atomic, because atomic registers are write strongly-linearizable.
Consider a write operation \( w_2 \) that finishes at time \( t \), as illustrated in Figure 3. For each write operation that is active at time \( t \) we must decide whether it should be linearized before or after \( w_2 \). We cannot treat all such operations in the same way: we cannot simply linearize all of them before or all of them after \( w_2 \). This is because the linearization order of these write operations depends on their timestamps (so as to respect the order of the read operations that read their values), which may not yet be fully formed at time \( t \). Indeed, the timestamp of a write operation active at \( t \) may end up being greater than, or smaller than, the timestamp of \( w_2 \). For example, in Figure 3 the timestamps eventually computed by the write operations \( w_1 \) and \( w_3 \), which are active at time \( t \), end up being, respectively, greater than and smaller than the timestamp of \( w_2 \). As we will see, by looking carefully at the progress that each of \( w_1 \) and \( w_3 \) has made by time \( t \) towards computing its vector timestamp, we can determine, at time \( t \), the correct linearization order of \( w_1 \) and \( w_3 \) relative to \( w_2 \). We do so by (a) initializing the timestamp of each write to \([\infty, \ldots, \infty]\) (so it gets smaller and smaller while it is being formed); and (b) ordering the writes by comparing their (possibly incomplete) timestamps in lexicographical order. This makes it possible to linearize the write operations on-line.

To prove that the MWMR implementation given by Algorithm 2 is write strongly-linearizable, we give a write strong-linearization function \( f \) for the set of histories \( \mathcal{H} \) of this algorithm. We describe \( f \) as an algorithm (Algorithm 3) that takes as input any finite or infinite history \( H \in \mathcal{H} \) and outputs a sequential history \( S \) that satisfies properties (L) and (P) of Definition 4. Intuitively, Algorithm 3 linearizes all the write operations on-line, as follows. It scans the input history \( H \) by increasing time; while doing so it maintains a sequence \( WS \) of write operations that it has linearized so far. When it sees that, at some time \( t_i \), a write operation \( w_i \) writes to \( Val[\cdot] \), it first checks whether \( w_i \) was already linearized i.e., whether \( w_i \) is in \( WS \) (lines 3–6). If \( w_i \) is not in \( WS \), it forms the set \( \mathcal{C}_i \) of all the write operations that are “active” at time \( t_i \) and are not yet in \( WS \) (line 7). It then determines the (possibly incomplete) timestamp of each operation in \( \mathcal{C}_i \) at time \( t_i \) (line 8); note that \( w_i \) is in \( \mathcal{C}_i \) and \( w_i \’s \) timestamp, denoted \( ts_{w_i} \), is complete. Finally, it selects the

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Algorithm 2 Implementing a write strongly-linearizable MWMR register \( R \) from SWMR registers

**Shared Object:**
For \( i = 1, 2, \ldots, n \):
- \( Val[i] \): SWMR register that contains a tuple \( (v, ts) \) where \( v \) is a value and \( ts \) is a vector timestamp; initialized to \([0, [0 \ldots 0]]\) where \( 0 \) is the initial value of \( R \) and \([0 \ldots 0]\) is an array of length \( n \).

**Local Object:**
- \( new_ts \): For each process, a local array of length \( n \); initialized to \([\infty, \ldots, \infty]\).

When writer \( p_k \) writes \( v \) to \( R \):
1: for \( i = 1 \) to \( n \) do  
2: if \( i \neq k \) then  
3: \( new\_ts[i] \leftarrow (Val[i].ts)[i] \)  
4: else  
5: \( new\_ts[i] \leftarrow (Val[i].ts)[i] + 1 \)  
6: end if  
7: end for  
8: \( Val[k] \leftarrow (v, new\_ts) \)  
9: \( new\_ts \leftarrow [\infty, \ldots, \infty] \)  
10: return done

When a process reads from \( R \):
11: for \( i = 1 \) to \( n \) do  
12: \( (v_j, ts_j) \leftarrow Val[i] \)  
13: end for  
14: let \( j \) be such that \( ts_j = \max\{ts_1, \ldots, ts_n\} \)  
15: return \( (v_j, ts_j) \)  

---

\( ^5 \) An operation that starts at time \( s \) and completes at time \( f \) is active at time \( t \) if \( s \leq t \leq f \).
operations in \( \mathcal{C} \), whose (possibly incomplete) timestamps are smaller than or equal to \( ts'_{\mathcal{C}} \) (line 9), and then it appends them to the linearization sequence \( WS \) in increasing timestamp order (line 10). To linearize the read operations, it collects all the read operations that return some value \((v, ts)\), and linearizes them after the write operation that writes \((v, ts)\), in increasing start time order (lines 22–31).

Intuitively, Algorithm 3 gives a write strongly-linearizable function \( f \) because: (1) by scanning \( H \) in increasing time, it linearizes each write operation by the time the operation completes without “peeking into the future”, and (2) it only appends write operations to \( WS \), and so it satisfies the “prefix property” (P) of Definition 4. In Appendix C we prove that Algorithm 3 defines a write strong-linearization function for \( \mathcal{H} \) and thus show:

**Theorem 10.** Algorithm 3 is a write strongly-linearizable implementation of a MWMR register from SWMR registers.

Helmi et. al show that there is no strongly linearizable implementation of MWMR registers from SWMR registers (Corollary 3.7 in [22]). Thus:

**Corollary 11.** Algorithm 3 is not a strongly linearizable implementation of a MWMR register.

This implies that strong linearizability is strictly stronger than write strong-linearizability.

## 5 Achieving write strong-linearizability is harder than achieving linearizability

As we will see, every linearizable implementation of an SWMR register is necessarily write strongly-linearizable. In contrast, here we prove that there is a linearizable implementation of an MWMR register from SWMR registers (namely, Algorithm 4) that is not write strongly-linearizable.

Algorithm 4 implements a MWMR register \( R \) from SWMR registers \( Val[i] \) for \( i = 1, 2, \ldots, n \). Each value written to \( R \) is timestamped with tuple \((sq, pid)\) where \( sq \) is a sequence number and \( pid \) is the id of the process that writes the value; intuitively, these are Lamport clocks that respect the causal order of write events. Each register \( Val[k] \) contains the latest value that \( p_k \) wrote to \( R \) with its corresponding timestamp. To write a value \( v \) into \( R \), \( p_k \) first reads every register \( Val[-] \) (lines 11–12); then \( p_k \) forms a new sequence number \( new\_sq \) by incrementing the maximum sequence number that it read from \( Val[-] \) (line 13); finally, \( p_k \) writes the tuple \((v, new\_ts)\), where \( new\_ts = \langle new\_sq, k \rangle \), into \( Val[k] \) (lines 16–17). To read \( R \), a process \( p \) first reads all registers \( Val[-] \) (lines 18–19); then \( r \) returns the value \( v \) with the greatest timestamp in lexicographic order (lines 20–21).

Intuitively, Algorithm 4 implements a linearizable MWMR register: the write operations can be linearized by their timestamps (which form a total order); the read operations are linearized according to the value that they read. The proof of the following theorem is given in Appendix D.

**Theorem 12.** Algorithm 4 is a linearizable implementation of a MWMR register from SWMR registers.
Algorithm 3 A write strongly-linearization function $f$ for the set of histories $H$ of Algorithm 2

Input: a history $H \in H$

Output: $S$, a sequential history of the operations in $H$

linearization of write operations in $H$
1: $WS_0 \leftarrow ()$
2: $m \leftarrow$ the number of operations that write to $Val[-]$ in $H$ // $m$ can be $\infty$
3: for $i = 1, 2, \ldots, m$ do
4: $t_i \leftarrow$ the time of the $i$th write to a register $Val[-]$ in $H$ (line 8 of Algorithm 2)
5: $w_i \leftarrow$ the operation that writes to $Val[-]$ at time $t_i$
6: if $w_i \notin WS_{i-1}$ then
7: $C_i \leftarrow \{w \mid w$ is a write operation such that $w \notin WS_{i-1}$ and $w$ is active at time $t_i$ in $H\}$
8: $\forall w \in C_i$, $ts_w^i \leftarrow$ the value of new $ts$, at time $t_i$, of the process executing $w$
9: $B_i \leftarrow \{w \mid w \in C_i$ and $ts_w^i \leq ts_w^i \}$
10: $WS_i \leftarrow WS_{i-1} \circ$ (the sequence of operations $w \in B_i$ in increasing order of $ts_w^i$)
11: else
12: $C_i \leftarrow \emptyset$; $B_i \leftarrow \emptyset$
13: $WS_i \leftarrow WS_{i-1}$
14: end if
15: end for
16: if $m = \infty$ then
17: $WS \leftarrow \lim_{i \to \infty} WS_i$
18: else
19: $WS \leftarrow WS_m$
20: end if

linearization of read operations in $H$
21: $S' \leftarrow WS$
22: for every value $(v, ts)$ that processes read in $H$ do
23: $R \leftarrow \{r \mid r$ is a read operation that returns $(v, ts)$ in $H\}$
24: $SR \leftarrow$ the sequence of operations in $R$ in increasing order of their start time
25: if $ts = [0, \ldots, 0]$ then
26: prepend $SR$ to $S'$
27: else
28: $w \leftarrow$ the operation in $S'$ that writes $(v, ts)$
29: insert $SR$ after $w$ and before any subsequent write operation in $S'$
30: end if
31: end for
32: $S \leftarrow S'$

The implemented register, however, is not write strongly-linearizable: roughly speaking the information provided by Lamport clocks is not sufficient to linearize the write operations on-line.

Theorem 13. Algorithm 4 is not a write strongly-linearizable implementation of a MWMR register.

Proof. Consider the set of histories $H$ of Algorithm 4 executed by $n = 3$ processes, $p_1$, $p_2$ and $p_3$. To prove that Algorithm 4 is not a write strongly-linearizable implementation, we show that $H$ is not write strongly-linearizable. More precisely, we prove that for any function $f$ that maps histories in $H$ to sequential histories, there exist histories $G, H \in H$ such that $G$ is a prefix of $H$ but $f(G)$ is not a prefix of $f(H)$.

Let $f$ be a function that maps histories in $H$ to sequential histories. Consider the following history $G \in H$ (shown at the left of Figure 4):

- Initially, $R$ contains 0, and each register $Val[i]$ contains $(0, (0, i))$. 
• At time $t_0$, process $p_1$ starts an operation $w_1$ to write a value $v \neq 0$ to $R$. By lines 1–2, $p_1$ first reads $(0, (0, 1))$ from $Val[1]$ into $(-, ts_1)$, say at time $t_1$, and then reads $(0, (0, 2))$ from $Val[2]$ into $(-, ts_2)$, say at time $t_2$. Thus, $p_1$ now has $ts_1 = (0, 1)$ and $ts_2 = (0, 2)$, i.e., $ts_1.sq = ts_2.sq = 0$.

• At time $t_3 > t_2$, process $p_2$ starts an operation $w_2$ to write a value $v'$ to $R$ such that $v' \neq v$ and $v' \neq 0$. By lines 4–6, $p_2$ reads $(0, (0, 1))$ from $Val[1]$ into $(-, ts_1)$, $(0, (0, 2))$ from $Val[2]$ into $(-, ts_2)$, and $(0, (0, 3))$ from $Val[3]$ into $(-, ts_3)$. Thus, $p_2$ now has $ts_1 = (0, 1)$, $ts_2 = (0, 2)$, and $ts_3 = (0, 3)$, i.e., $ts_1.sq = ts_2.sq = ts_3.sq = 0$. By lines 5–6, $p_2$ then writes $(v', (1, 2))$ to $Val[2]$ and completes $w_2$ at time $t_4$. Then at time $t_4$, $Val[1]$ contains $(0, (0, 1))$, $Val[2]$ contains $(v', (1, 2))$, and $Val[3]$ contains $(0, (0, 3))$.

Since the write operation $w_2$ completes in $G \in H$ and $f$ is a linearization function for $H$, by property 2 of Definition 2, $w_2$ is in $f(G)$. Since the write operation $w_1$ is concurrent with $w_2$, there are two cases: (1) $w_1$ is not before $w_2$ in $f(G)$, or (2) $w_1$ is before $w_2$ in $f(G)$.

Case 1: $w_1$ is not before $w_2$ in $f(G)$. Consider the following history $H \in H$ (shown at the top right of Figure 4):

- $H$ is an extension of $G$, i.e., $G$ is a prefix of $H$.
- At time $t_5 > t_4$, $p_1$ continues the operation $w_1$ and reads $(0, (0, 3))$ from $Val[3]$ into $(-, ts_3)$ so it has $ts_3.sq = 0$. By lines 5–6, $p_1$ reads $(v, (1, 1))$ to $Val[1]$. After that, $p_1$ completes $w_1$, say at time $t_6$. At time $t_6$, $Val[1]$ contains $(v, (1, 1))$, $Val[2]$ contains $(v', (1, 2))$, and $Val[3]$ contains $(0, (0, 3))$.

- At time $t_7 > t_6$, $p_3$ starts a read operation $r$ to read $R$. In lines 8–9, $p_3$ reads $ts_1 = (1, 1)$, $ts_2 = (1, 2)$, and $ts_3 = (0, 3)$. Since $ts_2 = (1, 2) > ts_1 = (1, 1) > ts_3 = (0, 3)$, by line 11, $r$ returns $(v', (1, 2))$ – the value written by $w_2$.

Since the read operation $r$ returns the value written by $w_2$ in $H \in H$, and $f$ is a linearization function for $H$, by property 2 of Definition 2, $r$ is after $w_2$ and before any subsequent write operation in $f(H)$. Since $r$ starts

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**Algorithm 4 Implementing a linearizable MWMR register $R$ from SWMR registers**

**Shared Object:**
For $i = 1, 2, ..., n$:
$Val[i]$: SWMR register that contains a tuple $(v, ts)$ where $v$ is a value and $ts$ is a tuple of the form $(sq, pid)$; initialized to $(0, (0, i))$.

**Local Object:**
$new\_sq$: a register initialized to 0.
$new\_ts$: a register initialized to $(0, k)$ for process $p_k$.

When writer $p_k$ writes $v$ to $R$ \hfill // $1 \leq k \leq n$

1: \textbf{for} $i = 1$ to $n$ \textbf{do}
2: \quad $(v_i, ts_i) \leftarrow Val[i]$
3: \textbf{end for}
4: new\_sq \leftarrow \max\{ts_1.sq, ..., ts_n.sq\} + 1
5: new\_ts \leftarrow (new\_sq, k)
6: Val[k] \leftarrow $(v, new\_ts)$
7: \textbf{return} done

When a process reads from $R$

8: \textbf{for} $i = 1$ to $n$ \textbf{do}
9: \quad $(v_i, ts_i) \leftarrow Val[i]$
10: \textbf{end for}
11: let $j$ be such that $ts_j = \max\{ts_1, ..., ts_n\}$ \hfill // lexicographic max
12: \textbf{return} $(v_j, ts_j)$

12
after \(w_1\) completes, by property 2 of Definition 2, \(r\) is after \(w_1\) in \(f(H)\). Thus, \(w_1\) is before \(w_2\) in \(f(H)\). Since, by assumption, \(w_2\) is in \(f(G)\) and \(w_1\) is not before \(w_2\) in \(f(G)\), \(f(G)\) is not a prefix of \(f(H)\).

**Case 2**: \(w_1\) is before \(w_2\) in \(f(G)\). Consider the following history \(H \in \mathcal{H}\) (shown at the bottom right of Figure 4):

- \(H\) is an extension of \(G\).
- At time \(t_5 > t_4\), process \(p_3\) starts an operation \(w_3\) to write \(v''\) to \(R\) such that \(v'' \neq v\). In lines 1–2 \(p_3\) reads \((0, (0, 1))\) from \(Val[1]\) into \((- , ts_1)\), \((v', (1, 2))\) from \(Val[2]\) into \((- , ts_2)\), and \((0, (0, 3))\) from \(Val[3]\) into \((- , ts_3)\). Thus, \(p_3\) now has \(ts_1 = (0, 1)\), \(ts_2 = (1, 2)\), and \(ts_3 = (0, 3)\), i.e., \(ts_1, sq = 0\), \(ts_2, sq = 1\), and \(ts_3, sq = 0\). By lines 5–6 \(p_3\) then writes \((v'', (2, 3))\) to \(Val[3]\), and completes \(w_3\) at time \(t_6\).
- At time \(t_7 > t_6\), \(p_1\) continues the operation \(w_1\) and reads \((v'', (2, 3))\) from \(Val[3]\) into \((- , ts_3)\) so it has \(ts_3, sq = 2\). By lines 5–6 \(p_1\) writes \((v, (3, 1))\) to \(Val[1]\). After that, \(p_1\) completes \(w_1\), say at time \(t_8\). At time \(t_8\), \(Val[1]\) contains \((v, (3, 1))\), \(Val[2]\) contains \((v', (1, 2))\), and \(Val[3]\) contains \((v'', (2, 3))\).

Since the read operation \(r\) returns the value written by \(w_1\) in \(H \in \mathcal{H}\), and \(f\) is a linearization function for \(\mathcal{H}\), by property 2 of Definition 2, \(r\) is after \(w_1\) and before any subsequent write operation in \(f(H)\). Since \(r\) starts after \(w_2\) completes, by property 2 of Definition 2, \(r\) is after \(w_2\) in \(f(H)\). Thus, \(w_2\) is before \(w_1\) in \(f(H)\). Since, by assumption, \(w_1\) is before \(w_2\) in \(f(G)\), \(f(G)\) is not a prefix of \(f(H)\).

Then, in both case 1 and case 2, there is a history \(H \in \mathcal{H}\) such that \(G\) is a prefix of \(H\) but \(f(G)\) is not a prefix of \(f(H)\). Therefore the theorem holds.

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**Figure 4**: Histories \(G\) and \(H\) for Cases 1 and 2

\(\times\)'s denote linearization points
Linearizable SWMR registers are necessarily write strongly-linearizable

In Appendix E, we show that any linearizable implementation of SWMR registers is write strongly-linearizable (this holds for message-passing, shared-memory, and hybrid systems). Thus, the well-known ABD implementation of SWMR registers in message-passing systems is not only linearizable; it is actually write strongly-linearizable.

**Theorem 14.** Any linearizable implementation of a SWMR register is necessarily write strongly-linearizable.

7 Concluding remarks

As we mentioned earlier, many randomized algorithms in the literature use atomic MWMR registers. An interesting open problem is to determine which ones can also (be made to) work in systems with atomic SWMR registers. If we replace a randomized algorithm’s atomic MWMR registers with linearizable implementations of MWMR registers from atomic SWMR registers, we may break it: it may lose some of its properties [19] including, as we showed in this paper, termination. On the other hand, we cannot replace an algorithm’s atomic MWMR registers with strongly linearizable implementations of MWMR registers from atomic SWMR registers — which would automatically preserve the correctness of this algorithm — simply because no such implementation exists [22]. But perhaps many (maybe even most) of the known randomized algorithms that use atomic MWMR registers do not actually need the full strength of strongly linearizable registers; in particular, they may not need the “strong linearizability property” to hold for both read and write operations. Randomized algorithms that need the strong linearizability properties only for write operations, also work in systems with atomic SWMR registers: just replace their MWMR registers with the register implementation given by Algorithm 2.

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\[\text{In fact, a recent paper shows that a well-known randomized algorithm by Aspnes and Herlihy that assumes atomic registers does not actually need any linearizability property: it works correctly with registers that are only regular [21].}\]
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Appendix A  Proof of Theorem 7

We now prove Theorem 7 in Section 3.2, namely, if registers $R_1$, $R_2$, and $C$ are write strongly-linearizable, Algorithm \[1\] terminates with probability 1 even against a strong adversary. To prove this, we first show four lemmas (Lemmas \[15\], \[18\]) about some safety properties of Algorithm \[1\]. Specifically, Lemma \[16\] and \[17\] state that processes $p_0$ and $p_1$ on one side, and processes $p_2, p_3, \ldots, p_{n-1}$ on the other side, remain within one round of each other. Lemma \[15\] and \[18\] state that the non-$\bot$ values that $p_2, p_3, \ldots, p_{n-1}$ read from registers $R_1$ and $C$ in any round $j$ were also written in round $j$.

To prove that Lemmas \[15\], \[18\] hold, we rely on our assumption that registers $R_1$, $R_2$, and $C$ are linearizable \[24\]. So in the following proofs, we refer to the linearization times of the read and write operations that are applied on these registers. For example, when we say "a process $p$ writes a value $v$ into $R_1$ at time $t'$", we mean that this write of $R_1$ "took effect" at time $t'$ in other words, this write operation is linearized at time $t$ (where $t$ is within the time interval of the operation).

In the following lemmas, we say that a process "enters round $r \geq 1$" if it executes line 1 or 17 with $j = r$.

**Lemma 15.** For all $j \geq 1$, if $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ reaches line 31 in round $j$, then $p_i$ previously read both $[b, j]$ and $[1 - b, j]$ for some $b \in \{0, 1\}$ from register $R_1$ in lines 21 and 22 in round $j$.

**Proof.** Suppose $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ reaches line 31 in a round $j \geq 1$. Since $p_i$ reaches line 31 in round $j$, $p_i$ did not exit in lines 23 and 28 in round $j$. So $p_i$ found the condition of lines 24 and 27 to be false in round $j$. Thus, $p_i$ found that $c \neq \bot$ and $(u_1 = [c, j]$ and $u_2 = [1 - c, j])$ in lines 24 and 27 in round $j$. Note that: (i) $u_1$ and $u_2$ contain the values that $p_i$ read from register $R_1$ in lines 21 and 22 in round $j$, and (ii) $c$ contains the value that $p_i$ read from register $C$ in lines 23 in round $j$; since $c \neq \bot$ and the only non-$\bot$ values written in $C$ are 0 or 1, $c = b \in \{0, 1\}$. Thus, $p_i$ read $[b, j]$ and $[1 - b, j]$ for $b \in \{0, 1\}$ from register $R_1$ in lines 21 and 22 in round $j$.

**Lemma 16.** For all $j \geq 1$, if $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ reaches line 31 in round $j$, then $p_0$ and $p_1$ previously entered round $j$.

**Proof.** Suppose $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ reaches line 31 in round $j$. By Lemma 15, $p_i$ previously read both $[b, j]$ and $[1 - b, j]$ for some $b \in \{0, 1\}$ from register $R_1$ in lines 21 and 22 in round $j$. So both $[0, j]$ and $[1, j]$ were previously entered into $R_1$. Since $p_0$ and $p_1$ are the only processes that write $[0, j]$ and $[1, j]$, and they only do so in (line 17 of) round $j$, we conclude that $p_0$ and $p_1$ previously entered round $j$.

**Lemma 17.** For all $j \geq 1$, if $p_0$ or $p_1$ enters round $j + 1$, then every $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ previously reached line 37 in round $j$.

**Proof.** To prove this part, we show the slightly stronger claim that if $p_0$ or $p_1$ enters round $j + 1$ at some time $t$, then every $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ writes $R_2$ in line 34 in round $j$ before time $t$. The proof is by induction on $j$.

**Base Case:** Let $j = 1$. Suppose that a process $p \in \{p_0, p_1\}$ enters round $j + 1 = 2$ at some time $t$. We must show that $p_1$ writes $R_2$ in line 34 in round $j = 1$ before time $t$.

**Claim 17.1** Up to and including time $t$, no process in $\{p_2, p_3, \ldots, p_{n-1}\}$ writes $R_2$ in line 34 in any round $r \geq 2$.

**Proof.** Suppose, for contradiction, that some process $p' \in \{p_2, p_3, \ldots, p_{n-1}\}$ writes $R_2$ in line 34 in a round $r \geq 2$ at some time $t < t \leq t$. So $p'$ reaches line 34 in round 2 at some time $t' < t \leq t$, i.e., $p'$ reaches line 34 in round 2 before $p \in \{p_0, p_1\}$ enters round 2 — a contradiction to Lemma 16.

Note that before $p$ enters round 2 at time $t$, $p$ does the following in round 1: it writes 0 into $R_2$ in line 10 at some time $t_1$, it reads $R_2$ into $v$ in line 11 at some time $t_2$, and then it finds that $v \geq n - 2$ in line 12 (because $p$ does not exit in line 13); clearly, $t_1 < t_2 < t$. Thus, some process $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ must have written a value $u \geq n - 2$ into $R_2$ in line 34 at some time $t' \in [t_1, t_2]$ in some round $r$. Since $t' \leq t_2 < t$, by Claim 17.1 $r \leq 1$. So $p_j$ writes $u \geq n - 2$ into $R_2$ in line 34 in round 1 at time $t' \in [t_1, t_2]$ (*).

**Claim 17.2** If a process in $\{p_2, p_3, \ldots, p_{n-1}\}$ writes $k \geq 1$ into $R_2$ in line 34 in round 1 at some time $t \leq t_2$, then at least $k$ distinct processes in $\{p_2, p_3, \ldots, p_{n-1}\}$ write $R_2$ in line 34 in round 1 by time $t$.
Proof. The proof is by induction on $k$.

- **Base Case:** For $k = 1$ the claim trivially holds.

- **Induction Step:** Let $k \geq 1$. Induction Hypothesis (\(\dagger\)): if a process in \(\{p_2, p_3, \ldots, p_{n-1}\}\) writes $k$ into $R_2$ in line 34 in round 1 at some time $t \leq t_2$, then at least $k$ distinct processes in \(\{p_2, p_3, \ldots, p_{n-1}\}\) write $R_2$ in line 34 in round 1 by time $t$.

Suppose that a process $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ writes $k + 1$ into $R_2$ in line 34 in round 1 at some time $t^{k+1}_w \leq t_2$, we must show that at least $k + 1$ distinct processes in \(\{p_2, p_3, \ldots, p_{n-1}\}\) write $R_2$ in line 34 in round 1 by time $t^{k+1}_w$.

Since $p_\ell$ writes $k + 1$ into $R_2$ in line 34 in round 1 at time $t^{k+1}_w \leq t_2$:

1. $p_\ell$ writes 0 into $R_2$ in line 31 in round 1 at some time $t^0_w$, and
2. $p_\ell$ reads $k$ from $R_2$ in line 32 in round 1 at some time $t^k_w$, such that $t^0_w < t^k_w < t^{k+1}_w \leq t_2 < t$.

Thus, some process $p^* \in \{p_2, p_3, \ldots, p_{n-1}\}$ must have written $k$ into $R_2$ in line 34 at some time $t^* \in [t^0_w, t^k_w]$ in some round $r$. Since $t^* < t$, by Claim 17.1, $r = 1$. So $p^*$ writes $k$ into $R_2$ in line 34 in round 1 at time $t^* \in [t^0_w, t^k_w]$. Since $t^* \leq t^k_w < t_2$, by the Induction Hypothesis (\(\dagger\)), at least $k$ distinct processes in \(\{p_2, p_3, \ldots, p_{n-1}\}\) write $R_2$ in line 34 in round 1 by time $t^*$. Recall that $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ also writes $R_2$ in line 34 in round 1 at time $t^{k+1}_w$. Thus, since each process in \(\{p_2, p_3, \ldots, p_{n-1}\}\) writes $R_2$ in line 34 in round 1 at most once, at least $k + 1$ distinct processes in \(\{p_2, p_3, \ldots, p_{n-1}\}\) write $R_2$ in line 34 in round 1 by time $t^{k+1}_w$.

\[\blacksquare\]

Recall that by (\(\ast\)), $p_j$ writes $u \geq n - 2$ into $R_2$ in line 34 in round 1 at time $t' \in [t_1, t_2]$. Since $t' \leq t_2$, by Claim 17.2 at least $n - 2$ distinct processes in \(\{p_2, p_3, \ldots, p_{n-1}\}\) write $R_2$ in line 34 in round 1 by time $t'$. Thus every process in \(\{p_2, p_3, \ldots, p_{n-1}\}\) writes $R_2$ in line 34 in round 1 by time $t'$. Since $t' \leq t_2 < t$, every $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ writes $R_2$ in line 34 in round 1 before time $t$.

- **Induction Step:** Let $j \geq 1$. Induction Hypothesis (\(\ast\)): for all $r$, $1 \leq r \leq j$, if $p_0$ or $p_1$ enters round $r + 1$ at some time $t$, then $p_j$ writes $R_2$ in line 34 in round $r$ before time $t$.

Suppose that a process $p \in \{p_0, p_1\}$ enters round $j + 2$ at some time $t$. We must show that $p_i$ writes $R_2$ in line 34 in round $j + 1$ before time $t$.

**Claim 17.3** Up to and including time $t$, no process in $\{p_2, p_3, \ldots, p_{n-1}\}$ writes $R_2$ in line 34 in any round $r \geq j + 2$.

**Proof.** Suppose, for contradiction, that some process $p' \in \{p_2, p_3, \ldots, p_{n-1}\}$ writes $R_2$ in line 34 in a round $r \geq j + 2$ at some time $\hat{t} \leq t$. So $p'$ reaches line 31 in round $j + 2$ at some time $t' < \hat{t} \leq t$, i.e., $p'$ reaches line 31 in round $j + 2$ before $p \in \{p_0, p_1\}$ enters round 2 — a contradiction to Lemma 16. \[\blacksquare\]

Note that before $p$ enters round $j + 2$ at time $t$, $p$ does the following in round $j + 1$: it writes 0 into $R_2$ in line 10 at some time $t_1$, it reads $R_2$ into $v$ in line 11 at some time $t_2$, and then it finds that $v \geq n - 2$ in line 12 (because $p$ does not exit in line 13); clearly, $t_1 < t_2 < t$. Thus, some process $p_j \in \{p_2, p_3, \ldots, p_{n-1}\}$ must have written a value $u \geq n - 2$ into $R_2$ in line 34 at some time $t' \in [t_1, t_2]$ in some round $r$. Since $t' < t_2 < t$, by Claim 17.3, $r \geq j + 2$.

**Claim 17.4** $r = j + 1$.

**Proof.** Suppose, for contradiction, $r \leq j$. Thus $p_j$ writes $R_2$ in line 34 in round $r \leq j$ at time $t' \in [t_1, t_2]$, i.e., after the time $t_1$ when $p$ writes 0 into $R_2$ in line 10 in round $j + 1$. So $p_j$ writes $R_2$ in line 34 in round $r \leq j$ after $p \in \{p_0, p_1\}$ enters round $r + 1 \leq j + 1$ — a contradiction to our Induction Hypothesis (\(\ast\)). \[\blacksquare\]

From Claim 17.4, $p_j$ writes $u \geq n - 2$ into $R_2$ in line 34 in round $j + 1$ at time $t' \in [t_1, t_2]$ (\(\dagger\)).

**Claim 17.5** If a process in $\{p_2, p_3, \ldots, p_{n-1}\}$ writes $k \geq 1$ into $R_2$ in line 34 in round $j + 1$ at some time $\hat{t} \leq t_2$, then at least $k$ distinct processes in $\{p_2, p_3, \ldots, p_{n-1}\}$ write $R_2$ in line 34 in round $j + 1$ by time $\hat{t}$.
Proof. The proof is by induction on $k$.

- **Base Case:** For $k = 1$ the claim trivially holds.

- **Induction Step:** Let $k \geq 1$. Induction Hypothesis (§8): if a process in $\{p_2, p_3, \ldots, p_{n-1}\}$ writes $k$ into $R_2$ in line 34 in round $j + 1$ at some time $t \leq t_2$, then at least $k$ distinct processes in $\{p_2, p_3, \ldots, p_{n-1}\}$ write $R_2$ in line 34 in round $j + 1$ by time $t$.

Suppose that a process $p_\ell \in \{p_2, p_3, \ldots, p_{n-1}\}$ writes $k + 1$ into $R_2$ in line 34 in round $j + 1$ at some time $t_w^{k+1} \leq t_2$, we must show that least $k + 1$ distinct processes in $\{p_2, p_3, \ldots, p_{n-1}\}$ write $R_2$ in line 34 in round $j + 1$ by time $t_w^{k+1}$.

Since $p_\ell$ writes $k + 1$ into $R_2$ in line 34 in round $j + 1$ at some time $t_w^{k+1} \leq t_2$:

1. $p_\ell$ reads 0 into $R_2$ in line 31 in round $j + 1$ at some time $t_0^w$, and
2. $p_\ell$ writes into $R_2$ in line 32 in round $j + 1$ at some time $t_1^w$, such that $t_0^w < t_1^w < t_w^{k+1} \leq t_2 < t$.

Thus, some process $p^* \in \{p_2, p_3, \ldots, p_{n-1}\}$ must have written $k$ into $R_2$ in line 34 at some time $t^* \in [t_0^w, t_1^w]$ in some round $r$. Since $t^* < t$, by Claim 17.3 $r \leq j + 1$.

**Claim 17.5.1 $r = j + 1$.**

*Proof.* Suppose, for contradiction, that $r \leq j$. Since $p_j$ reaches line 31 in round $j + 1$ at time $t_0^w$, by Lemma 16 both $p_0$ and $p_1$ entered round $j + 1$ before time $t_0^w$. So $p_0$ and $p_1$ enter round $r + 1 \leq j + 1$ before $p^*$ writes $R_2$ in line 34 in round $r \leq j$ (at time $t^*$) — a contradiction to our Induction Hypothesis (*).

From Claim 17.5.1 $p^*$ writes $k$ into $R_2$ in line 34 in round $j + 1$ at time $t^* \in [t_0^w, t_1^w]$. Since $t^* \leq t_1^w < t_2$, by the Induction Hypothesis (§8), at least $k$ distinct processes in $\{p_2, p_3, \ldots, p_{n-1}\}$ write $R_2$ in line 34 in round $j + 1$ by time $t^*$.

Recall that by (†), $p_j$ writes $u \geq n - 2$ into $R_2$ in line 34 in round $j + 1$ at time $t' \in [t_1, t_2]$. Since $t' \leq t_2$, by Claim 17.5 at least $n - 2$ distinct processes in $\{p_2, p_3, \ldots, p_{n-1}\}$ write $R_2$ in line 34 in round $j + 1$ by time $t'$. Thus every process in $\{p_2, p_3, \ldots, p_{n-1}\}$ writes $R_2$ in line 34 in round $j + 1$ by time $t'$. Since $t' \leq t_2 < t$, every $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ writes $R_2$ in line 34 in round $j + 1$ by time $t_w^{k+1}$.

**Lemma 18.** For all $j \geq 1$, if $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ reaches line 27 in round $j$, then in that line $p_i$ has $c = b$ such that $b \in \{0, 1\}$ and $p_0$ wrote $b$ into register $C$ in line 7 in round $j$.

*Proof.* Suppose that some $p_i \in \{p_2, p_3, \ldots, p_{n-1}\}$ reaches line 27 in round $j \geq 1$. We must show that $p_i$ has $c = b$ for some $b \in \{0, 1\}$ in line 27 in round $j \geq 1$, and $p_0$ wrote $b$ into $C$ in line 7 in round $j$.

Since $p_i$ reaches line 27 in round $j$, in each round $k$, $1 \leq k \leq j$, the following occurs:

1. $p_i$ first writes $\perp$ into register $C$ in line 20 then
2. $p_i$ reads some value $b_k$ from $C$ into $c$ in line 23

Note that $b_k \neq \perp$, because otherwise $p_i$ would exit in line 25 (by the condition of line 24) in round $k$ before reaching line 24 in round $j$. Moreover, since $b_k \neq \perp$ and $p_0$ is the only process that writes non-$\perp$ values (namely, 0 or 1) into $C$, $b_k$ must be a value in $\{0, 1\}$ that $p_0$ wrote into $C$ (in line 7). Therefore: in each round $k$, $1 \leq k \leq j$, $p_i$ writes $\perp$ into $C$ at some time $t_k$, and at some time $t_k' > t_k$, $p_i$ reads from $C$ a value $b_k \in \{0, 1\}$ written by $p_0$ into $C$ at some time in $[t_k, t_k']$ (*).
Since \( p_0 \) writes a value into \( C \) only once in each round, (*) implies that the value \( b_j \) that \( p_1 \) reads from \( C \) in round \( j \) was written by \( p_0 \) into \( C \) in some round \( r \geq j \) (**).

Let \( t \) be the time \( p_i \) reads \( b_j \) from \( C \) in round \( j \) (in line 34). At time \( t \), \( p_i \) has not yet reached line 34 in round \( j \). Thus, from Lemma 17 process \( p_0 \) has not entered round \( j + 1 \) by time \( t \). So, by time \( t \), process \( p_0 \) has not written any value into register \( C \) in any round \( \ell \geq j + 1 \). Therefore, by (**), the value \( b_j \) that \( p_i \) reads from \( C \) into \( C \) in line 34 in round \( j \) at time \( t \) was written by \( p_0 \) into \( C \) in round \( r = j \). We conclude that \( p_i \) has \( c = b_j \) for \( b_j \in \{0, 1\} \) in line 27 in round \( j \), and \( p_0 \) wrote \( b_j \) into \( C \) in line 7 in round \( j \).  

We now prove that if registers \( R_1, R_2, \) and \( C \) are write strongly-linearizable, then Algorithm 1 terminates with probability 1 even against a strong adversary (Theorem 7). Intuitively, this is because if \( R_1, R_2, \) and \( C \) are write strongly-linearizable, then the order in which \( [0, j] \) and \( [1, j] \) are written into \( R_1 \) in line 28 in round \( j \) is already fixed before the adversary \( S \) can see the result of the coin flip in line 6 in round \( j \). So for every round \( j \geq 1 \), the adversary cannot “retroactively” decide on this linearization order of write operations according to the coin flip result (like it did when \( R_1 \) was merely linearizable) to ensure that processes \( p_1, p_2, \ldots, p_{n-1} \) do not exit by the condition of line 28. Thus, with probability 1/2, all these processes will exit in line 28. And if they all exit there, then no process will increment register \( R_2 \) in lines 32, 34, and so \( p_0 \) and \( p_1 \) will also exit.

The proof of Theorem 7 is based on the following:

**Lemma 19.** For all rounds \( j \geq 1 \), with probability at least 1/2, no process enters round \( j + 1 \).

**Proof.** Consider any round \( j \geq 1 \). There are two cases:

(I) Process \( p_0 \) does not complete its write of \( [0, j] \) into register \( R_1 \) in line 3 in round \( j \).

Thus, \( p_0 \) does not invoke the write of any value into \( C \) in line 7 in round \( j \) (*).

**Claim 19.1** No process enters round \( j + 1 \).

**Proof.** We first show that no process in \( \{p_2, p_3, \ldots, p_{n-1}\} \) reaches line 34 in round \( j \). To see why, suppose, for contradiction, some process \( p_i \) with \( i \in \{2, 3, \ldots, n - 1\} \) reaches line 34 in round \( j \). By Lemma 18 in that line \( p_i \) has \( c = b \in \{0, 1\} \) such that \( p_0 \) invoked the write of \( b \) into \( C \) in line 7 in round \( j \) — a contradiction to (*).

Thus no process in \( \{p_2, p_3, \ldots, p_{n-1}\} \) reaches line 34 in round \( j \). By Lemma 17 neither \( p_0 \) nor \( p_1 \) enters round \( j + 1 \).

(II) Process \( p_0 \) completes its write of \( [0, j] \) into register \( R_1 \) in line 3 in round \( j \).

**Claim 19.2** With probability at least 1/2, no process enters round \( j + 1 \).

**Proof.** Consider the set of histories \( H \) of Algorithm 1; this is a set of histories over the registers \( R_1, R_2, C \). Since these registers are write strongly-linearizable, by Lemma 4.8 of [19], \( H \) is write strongly-linearizable, i.e., it has at least one write strong-linearization function that satisfies properties (L) and (P) of Definition 1. Let \( f \) be the write-strong-linearization function that the adversary \( S \) uses.

Let \( g \) be an arbitrary history of the algorithm up to and including the completion of the write of \( [0, j] \) into \( R_1 \) by \( p_0 \) in line 3 in round \( j \). Since \( p_0 \) completes its write of \( [0, j] \) into \( R_1 \) in \( g \), this write operation appears in the write-strong-linearization \( f(g) \). Now there are two cases:

- **Case A:** In \( f(g) \), the write of \( [1, j] \) into \( R_1 \) by \( p_1 \) in line 3 in round \( j \) occurs before the write of \( [0, j] \) into \( R_1 \) by \( p_0 \) in line 3 in round \( j \).

Since \( f \) is a write-strong-linearization function, for every extension \( h \) of the history \( g \) (i.e., for every history \( h \) such that \( g \) is a prefix of \( h \)), the write of \( [1, j] \) into \( R_1 \) occurs before the write of \( [0, j] \) into \( R_1 \) in the linearization \( f(h) \) (note that for all \( j \geq 1 \), each of \( [1, j] \) and \( [0, j] \) is written at most once in \( R_1 \), so it appears at most once in \( h \) and \( f(h) \)). Thus, in \( g \) and every extension \( h \) of \( g \), no process can first read \([0, j]\) from \( R_1 \) and then read \([1, j]\) from \( R_1 \) (**).
Let $\mathcal{P}$ be the subset of processes in $\{p_2, p_3, \ldots, p_{n-1}\}$ that evaluate the condition $(u_1 \neq [c, j] \text{ or } u_2 \neq [1 - c, j])$ in line 27 in round $j$. Note that for each process $p_i$ in $\mathcal{P}$, $u_1$ and $u_2$ are the values that $p_i$ read from $R_1$ consecutively in lines 21 and 22 in round $j$. By (†), $p_i$ cannot first read

$u_1 = [0, j]$ and then read $u_2 = [1, j]$ from $R_1$. Thus, no process $p_i$ in $\mathcal{P}$ can have both $u_1 = [0, j]$ and $u_2 = [1, j]$ in line 27 in round $j$ (**) .

Let $\mathcal{P}' \subseteq \mathcal{P}$ be the subset of processes in $\mathcal{P}$ that have $c = 0$ in line 27 in round $j$.

**Claim 19.2.1**

(a) No process in $\mathcal{P}'$ reaches line 34 in round $j$.

(b) If $\mathcal{P}' = \mathcal{P}$ then neither $p_0$ nor $p_1$ enters round $j + 1$.

**Proof.** To see why Part (a) holds, note that no process $p_i$ in $\mathcal{P}'$ can find the condition $(u_1 \neq [c, j] \text{ or } u_2 \neq [1 - c, j])$ in line 27 in round $j$ to be false: otherwise $p_i$ would have both $u_1 = [c, j] = [0, j]$ and $u_2 = [1 - c, j] = [1, j]$ in that line, but this is not possible by (**) . Thus, no process in $\mathcal{P}'$ reaches line 34 in round $j$ (it would exit in line 28 before reaching that line).

To see why Part (b) holds, suppose $\mathcal{P}' = \mathcal{P}$ and consider any process $p_i$ in $\{p_2, p_3, \ldots, p_{n-1}\}$. If $p_i \not\in \mathcal{P}$ then $p_i$ never enters round 3; and if $p_i \in \mathcal{P}'$, then $p_i \in \mathcal{P}'$, and so from Part (a), $p_i$ does not reach line 34 in round $j$. So in both cases, $p_i$ does not reach line 34 in round $j$. Thus, by Lemma 17 neither $p_0$ nor $p_1$ enters round $j + 1$.

Now recall that $g$ is the history of the algorithm up to and including the completion of the write of $[0, j]$ into $R_1$ by $p_0$ in line 3 in round $j$. After the completion of this write, i.e., in any extension $h$ of $g$, $p_0$ is supposed to flip a coin and write the result into $C$ in line 7 in round $j$. Thus, with probability at least $1/2$, $p_0$ will not invoke the operation to write 1 into $C$ in line 7 in round $j$. So, from Lemma 18 with probability at least $1/2$, every process in $\mathcal{P}$ has $c = 0$ in line 27 in round $j$; this means that with probability at least $1/2$, $\mathcal{P}' = \mathcal{P}$. Therefore, from Claim 19.2.1 with probability at least $1/2$:

(a) No process in $\mathcal{P}$ reaches line 34 in round $j$.

(b) Neither $p_0$ nor $p_1$ enters round $j + 1$.

This implies that in Case A, with probability at least $1/2$, no process enters round $j + 1$.

**Case B:** In $f(g)$, the write of $[1, j]$ into $R_1$ by $p_1$ in line 3 in round $j$ does not occur before the write of $[0, j]$ into $R_1$ by $p_0$ in line 3 in round $j$. This case is essentially symmetric to the one for Case A, we include it below for completeness.

Since $f$ is a write-strong-linearization function, for every extension $h$ of the history $g$, the write of $[1, j]$ into $R_1$ does not occur before the write of $[0, j]$ into $R_1$ in the linearization $f(h)$. Thus, in $g$ and every extension $h$ of $g$, no process can first read $[1, j]$ from $R_1$ and then read $[0, j]$ from $R_1$ (†). Let $\mathcal{P}$ be the subset of processes in $\{p_2, p_3, \ldots, p_{n-1}\}$ that evaluate the condition $(u_1 \neq [c, j] \text{ or } u_2 \neq [1 - c, j])$ in line 27 in round $j$. Note that for each process $p_i$ in $\mathcal{P}$, $u_1$ and $u_2$ are the values that $p_i$ read from $R_1$ consecutively in lines 21 and 22 in round $j$. By (††), $p_i$ cannot first read $u_1 = [1, j]$ and then read $u_2 = [0, j]$ from $R_1$. Thus, no process $p_i$ in $\mathcal{P}$ can have both $u_1 = [1, j]$ and $u_2 = [0, j]$ in line 27 in round $j$ (††). Let $\mathcal{P}' \subseteq \mathcal{P}$ be the subset of processes in $\mathcal{P}$ that have $c = 1$ in line 27 in round $j$.

**Claim 19.2.2**

(a) No process in $\mathcal{P}'$ reaches line 34 in round $j$.

(b) If $\mathcal{P}' = \mathcal{P}$ then neither $p_0$ nor $p_1$ enters round $j + 1$.

**Proof.** To see why (a) holds, note that no process $p_i$ in $\mathcal{P}'$ can find the condition $(u_1 \neq [c, j] \text{ or } u_2 \neq [1 - c, j])$ in line 27 in round $j$ to be false: otherwise $p_i$ would have both $u_1 = [c, j] = [1, j]$ and $u_2 = [1 - c, j] = [0, j]$ in that line, but this is not possible by (††). Thus, no process in $\mathcal{P}'$ reaches line 34 in round $j$ (it would exit in line 28 before reaching that line).

To see why (b) holds, suppose $\mathcal{P}' = \mathcal{P}$ and consider any process $p_i$ in $\{p_2, p_3, \ldots, p_{n-1}\}$. If $p_i \not\in \mathcal{P}$ then $p_i$ never evaluates the condition in line 27 in round $j$; and if $p_i \in \mathcal{P}$, then $p_i \in \mathcal{P}'$, and so
from (a) \(p_i\) does not reach line 34 in round \(j\). So in both cases, \(p_i\) does not reach line 34 in round \(j\). Thus, by Lemma 17, neither \(p_0\) nor \(p_1\) enters round \(j + 1\).

Now recall that \(g\) is the history of the algorithm up to and including the completion of the write of \([0, j]\) into \(R_1\) by \(p_0\) in line 3 in round \(j\). After the completion of this write, i.e., in any extension \(h\) of \(g\), \(p_0\) is supposed to flip a coin and write the result into \(C\) in line 27 in round \(j\). Thus, with probability at least 1/2, \(p_0\) will not invoke the operation to write 0 into \(C\) in line 27 in round \(j\). So, from Lemma 18, with probability at least 1/2, every process in \(P\) has \(c = 1\) in line 27 in round \(j\); this means that with probability at least 1/2, \(P' = P\). Therefore, from Claim 19.2.2 with probability at least 1/2:

(a) No process in \(P\) reaches line 34 in round \(j\).

(b) Neither \(p_0\) nor \(p_1\) enters round \(j + 1\).

This implies that in Case B, with probability at least 1/2, no process enters round \(j + 1\). Therefore, from Claims 19.1 and 19.2 of Cases (I) and (II), with probability at least 1/2, no process enters round \(j + 1\).

We can now complete the proof of Theorem 7, namely, that with write strongly-linearizable registers, Algorithm 1 terminates with probability 1 even against a strong adversary.

**Theorem 7.** If registers \(R_1\), \(R_2\), and \(C\) are write strongly-linearizable, then Algorithm 1 terminates with probability 1 against a strong adversary.

**Proof.** Consider any round \(j \geq 1\). By Lemma 19 with probability at least 1/2, no process enters round \(j + 1\). Since this holds for every round \(j \geq 1\), then, with probability 1, all the correct processes return in lines 16 or line 36 within a finite number of rounds \(r\).

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**Appendix B  Bounding the registers of Algorithm 1**

We now explain how to obtain our result of Section 3, namely Theorems 6–7, with bounded shared registers. Note that Algorithm 1 that we used to obtain our results uses three shared MWMR registers, and only one of them, namely register \(R_1\), is unbounded. Specifically, \(R_1\) is unbounded because each process \(p_i\), \(i \in \{0, 1\}\), writes a tuple \([i, j]\) into \(R_1\) in rounds \(j = 1, 2, \ldots\). As we show below, however, it is sufficient for \(R_1\) to contain only the values 0, 1, or \(\perp\). To achieve this, we modify Algorithm 1 as follows:

- Each process \(p_i\), \(i \in \{0, 1\}\), writes \(i\) (instead of the tuple \([i, j]\)) into \(R_1\) in line 3.
- The guard \((u_1 \neq [c, j] \text{ or } u_2 \neq [1 - c, j])\) is replaced by the guard \((u_1 \neq c \text{ or } u_2 \neq 1 - c)\) in line 27.

To understand why the above changes do not affect the behaviour of the algorithm (i.e., why Algorithm 1 and the modified algorithm have exactly the same runs), consider how the tuples \([i, j]\) written into \(R_1\) are actually used in Algorithm 1. In each round \(j \geq 1\), each process \(p \in \{p_2, p_3, \ldots, p_{n-1}\}\) reads \(R_1\) twice (in lines 21 and in line 22, respectively), and then it checks the two values \(u_1\) and \(u_2\) that it read in line 24 and in line 27. Specifically:

1. In line 24, \(p\) checks whether \(u_1\) or \(u_2\) is \(\perp\).

   Note that \(p\) has \(u_1 = [i, j] \neq \perp\) in line 24 in Algorithm 1 if and only if \(p\) has \(u_1 = i \neq \perp\) in line 24 in the modified algorithm. The same holds for \(u_2\) in line 24.

   Thus, the guard \((u_1 = \perp \text{ or } u_2 = \perp \text{ or } c = \perp)\) in line 24 has the same effect in the modified algorithm as in Algorithm 1.
2. In line 27, \( p \) checks whether \( (u_1 \neq [c, j] \text{ or } u_2 \neq [1 - c, j]) \) for some specific value \( c \).

Lemma 20 (proven below) states that when \( p \) reaches line 27 in round \( j \) and is poised to check whether \( (u_1 \neq [c, j] \text{ or } u_2 \neq [1 - c, j]) \), it must be the case that \( u_1 = [-j] \) and \( u_2 = [-j] \). So checking whether the second component of the two tuples is \( j \) or not is useless. Thus, the guard \((u_1 \neq [c, j] \text{ or } u_2 \neq [1 - c, j])\) in Algorithm 1 has the same effect as the guard \((u_1 \neq c \text{ or } u_2 \neq 1 - c)\) in the modified algorithm.

So to show that the modified algorithm behaves exactly as Algorithm 1, it now is sufficient to prove:

**Lemma 20.** For all \( j \geq 1 \), if \( p_i \in \{p_2, p_3, \ldots, p_{n-1}\} \) reaches line 27 in round \( j \), then in that line \( p_i \) has \( u_1 = [-j] \) and \( u_2 = [-j] \).

*Proof.* Suppose that some \( p_i \in \{p_2, p_3, \ldots, p_{n-1}\} \) reaches line 27 in round \( j \geq 1 \). We must show that \( p_i \) has \( u_1 = [-j] \) and \( u_2 = [-j] \) in line 27 in round \( j \).

Since \( p_i \) reaches line 27 in round \( j \), \( u_1 \neq \bot \) and \( u_2 \neq \bot \) in that line, because otherwise \( p \) would have exited in line 25 (by the condition of line 24) before reaching line 27 in round \( j \). Note that \( u_1 \) and \( u_2 \) contain the values that \( p_i \) reads from \( R_1 \) in lines 21 and 22 in round \( j \), after it wrote \( \perp \) into \( R_1 \) in line 19 in round \( j \). So in line 27 in round \( j \) of \( p_i \), each of \( u_1 \) and \( u_2 \) contains a non-\( \perp \) value that some process in \( \{p_0, p_1\} \) wrote into \( R_1 \) in line 19 in round \( j \) between the time \( t_w \) when \( p_i \) wrote \( \perp \) into \( R_1 \) in line 19 in round \( j \) and the time \( t_r \) when \( p_i \) read \( R_1 \) in line 22 in round \( j \) (*). Let \( p_0 \) be any process in \( \{p_0, p_1\} \) that writes \( R_1 \) (in line 19) at any time in \([t_w, t_r]\). Note that \( p_0 \) does this write before \( p_i \) reaches line 27 in round \( j \). Thus, by Lemma 17, \( p_0 \) does this write in a round \( r \leq j \). So this is a write of \([b, r]\) with \( r \leq j \) and \( b \in \{0, 1\} \) into \( R_1 \). Thus, from (*), \( p_i \) has \( u_1 = [b_1, r_1] \) and \( u_2 = [b_2, r_2] \) with \( 1 \leq r_1, r_2 \leq j \) and \( b_1, b_2 \in \{0, 1\} \) in line 27 in round \( j \) (**).

**Claim 20.1** \( r_1 = r_2 = j \)

*Proof.* Recall that \( 1 \leq r_1, r_2 \leq j \). If \( j = 1 \), it follows that \( r_1 = r_2 = j = 1 \). Now assume that \( j \geq 2 \). Suppose, for contradiction, that \( r_1 \neq j \) or \( r_2 \neq j \), and so \( 1 \leq r_1 \leq j - 1 \) or \( 1 \leq r_2 \leq j - 1 \). Without loss of generality, say that \( 1 \leq r_1 \leq j - 1 \). By (**), \( p_i \) has \( u_1 = [b_1, r_1] \) with \( b_1 \in \{0, 1\} \) in line 27 in round \( j \). So \( p_i \) read \([b_1, r_1]\) from \( R_1 \) in lines 21 in round \( j \), and \( p_i \) did so after writing \( \perp \) into \( R_1 \) in line 19 in round \( j \). Note that before \( p_i \) wrote \( \perp \) into \( R_1 \) in line 19 in round \( j \), the following occurred: (i) \( p_i \) reached line 32 in round \( r_1 \) \( \leq j - 1 \); and so by Lemma 15 (ii) \( p_i \) read the value \([b_1, r_1]\) from \( R_1 \) in round \( r_1 \) \( \leq j - 1 \). From the code of processes \( \{p_0, p_1\} \) it is clear that \([b_1, r_1]\) is written only once into \( R_1 \) (specifically, by process \( p_0 \) in round \( r_1 \)). Thus, since \( p_i \) read \([b_1, r_1]\) from \( R_1 \) in round \( r_1 \) \( \leq j - 1 \) before process \( p_i \) writes \( \perp \) into \( R_1 \) in line 19 in round \( j \), it cannot read \([b_1, r_1]\) again from \( R_1 \) in lines 21 in round \( j \) — a contradiction.

From Claim 20.1 and (**), process \( p_i \) has \( u_1 = [b_1, j] \) and \( u_2 = [b_2, j] \) with \( b_1, b_2 \in \{0, 1\} \) in line 27 in round \( j \).

**Appendix C**  **Proof of Theorem 10**

We now prove Theorem 10 in Section 3, namely, Algorithm 2 is a write strongly-linearizable implementation of a MWMR register from SWMR registers. In the following, we consider an arbitrary history \( H \in H \) of Algorithm 2 and the history \( S = f(H) \) constructed by Algorithm 3 on input \( H \). We first show \( f \) is a linearization function of \( H \), i.e., \( S \) satisfies properties 1, 2 of Definition 1.

**Definition 21.** An operation that starts at time \( s \) and completes at time \( f \) is active at time \( t \) if \( s \leq t \leq f \).

**Definition 22.** Let \( a \) and \( b \) be two timestamps then:

- \( a < b \) if and only if \( a \) precedes \( b \) in lexicographic order.
- \( a \leq b \) if and only if \( a = b \) or \( a < b \).

**Observation 23.** Relation \( \leq \) is a total order on the set of timestamps.

**Notation.** Let \( w \) be an operation that writes into \( Val[-] \). We denote by \( ts_w \) the timestamp that \( w \) writes into \( Val[-] \). That is, if \( w \) writes \((- , ts) \), \( ts_w = ts \).
Observation 24. The tuples \((v, ts)\) and \((v', ts')\) written to \(Val[-]\) by two distinct write operations have distinct timestamps, i.e., \(ts \neq ts'\).

Observation 25. Consider the execution of a write operation (lines 2–10) by a process \(p_k\). During that execution, the values of the variable new\_ts of \(p_k\) are non-increasing with time.

Observation 26. If a read operation returns \((v, ts) \neq (0, [0, \ldots, 0])\), then there is an operation \(w\) that writes \((v, ts)\) to \(Val[-]\).

Lemma 27. If a read operations \(r\) starts after an operation \(w\) writes to \(Val[-]\) and \(r\) returns \((-\), ts\), then \(ts \geq ts_w\).

Proof. Assume a read operations \(r\) starts after an operation \(w\) writes to some \(Val[k]\) and \(r\) returns \((-\), ts\). Then \(r\) reads \(Val[i]\) (line 12 of Algorithm 2) for every \(1 \leq i \leq n\) after \(w\) writes \((-\), ts\) to \(Val[k]\). Since the timestamps in each \(Val[-]\) are monotonically increasing, \(r\) reads \((-\), ts') from \(Val[k]\) for some \(ts' \geq ts_w\). Since \(ts\) is the largest timestamp that \(r\) reads among all \(Val[-]\) (lines 14–15 of Algorithm 2), \(ts \geq ts' \geq ts_w\).

Observation 28. If an operation \(w\) writes to \(Val[-]\), there is an \(i \geq 1\) such that \(w = w_i\).

Observation 29. If an operation \(w\) writes to \(Val[-]\), there is a unique \(j \geq 1\) such that \(w \in B_j\).

Observation 30. For every write operation \(w\), \(w \in S\) if and only if there is an \(i\) such that \(w \in B_i\).

By Observations 29 and 30 we have:

Corollary 31. If an operation \(w\) writes to \(Val[-]\), then \(w \in S\).

Observation 32. For any two write operations \(w\) and \(w'\), if \(w \in B_i\), \(w' \in B_j\), and \(i < j\), then \(w\) is before \(w'\) in \(S\).

Recall that \(ts^i_w\) is the value of new\_ts, at time \(t_i\), of the process executing the write operation \(w\) (see line 8 of \(f\)).

Observation 33. For all \(i \geq 1\), if \(w_i \in B_i\) then \(ts^i_{w_i} = ts_i\).

Observation 34. For all \(i \geq 1\), for all operations \(w \in B_i\), if \(w \neq w_i\) then \(ts^i_w < ts_i\).

By Observation 26 we have:

Observation 35. For all \(i \geq 1\), for all operations \(w \in B_i\) that write to \(Val[-]\), \(ts_w \leq ts^i_w\).

By Observations 34 and 35 we have:

Observation 36. For all \(i \geq 1\), for all operations \(w \in B_i\) that write to \(Val[-]\), \(ts_w \leq ts^i_w\).

Lemma 37. For all \(i \geq 1\), for all operations \(w\) that write to \(Val[-]\), if \(w \in C_i\) and \(w \notin B_i\), then \(ts_w > ts^i_w\).

Proof. Let \(i \geq 1\) and assume that an operation \(w\) writes to \(Val[-]\) such that \(w \in C_i\) and \(w \notin B_i\). By line 9 of Algorithm 3, \(ts^i_w > ts^i_w\). Since by Observation 32, \(ts^i_w = ts^i_{w_i}\) (\(*\)). There are two cases:

Case 1: \(ts^i_w\) contains no \(w\). This implies \(ts_w = ts^i_w\). Thus, by (\(*\)), \(ts_w = ts^i_w > ts^i_w\).

Case 2: \(ts^i_w\) contains \(w\). Then there is a \(k\) such that for every \(k \leq l \leq n\), \(w\) reads \((Val[l].ts)[l]\) (lines 3 and 5 of Algorithm 2) after time \(t_i\). Note that \(w_i\) reads \((Val[l].ts)[l]\) before time \(t_i\) for every \(k \leq l \leq n\), and \(w_i\) writes \((-\), ts\) to some \(Val[-]\) at time \(t_i\). Thus, for every \(k \leq l \leq n\), since \((Val[l].ts)[l]\) is non-decreasing, \(ts_w[l] \geq ts_i[l]\) (\(\dagger\)).

For every \(1 \leq l \leq k - 1\), since \(w\) reads \((Val[l].ts)[l]\) before time \(t_i\), \(ts_w[l] = ts^i_w[l]\). By (\(*\)), \(ts^i_w[1, \ldots, k-1] \geq ts^i_w[1, \ldots, k-1]\). So \(ts_w[1, \ldots, k-1] \geq ts^i_w[1, \ldots, k-1]\) (\(\dagger\)).

By (\(\dagger\)) and (\(\dagger\)), \(ts_w \geq ts^i_w\). Since \(w \notin B_i\), \(w \neq w_i\). By Observation 24, \(ts_w \neq ts^i_w\). Thus, \(ts_w > ts^i_w\).

Lemma 38. For all \(j > i \geq 1\), if \(w \in B_i\), \(w' \in B_j\), and \(w\) and \(w'\) both write to \(Val[-]\), then \(ts_w > ts^i_w\).
Proof. Assume $j > i \geq 1$, $w \in B_i$, $w' \in B_j$, and $w$ and $w'$ both write to $Val[-]$.  

Claim 38.1 $ts_{w'} > ts_{w_i}$. 

Proof. Since $w' \in B_j$ and $j > i$, $w' \notin B_i$ and $w' \notin WS_i$. There are two cases: 

Case 1: $w' \in C_i$. Since $w' \in C_i$ and $w' \notin B_i$, by Lemma 37, $ts_{w'} > ts_{w_i}$. 

Case 2: $w' \notin C_i$. By lines 10 and 13 of Algorithm 3 $WS_{i-1}$ is a prefix of $WS_i$. Since $w' \notin WS_i$, $w' \notin WS_{i-1}$. Since $w' \notin C_i$, by line 7 of Algorithm 3 $w'$ is not active at time $t_i$. Since $w' \in B_j \subseteq C_j$, by line 7 of Algorithm 3, $w'$ is active at time $t_j$. Since $i < j$, $t_i < t_j$. So $w'$ starts after $t_i$ and $w'$ reads all $(Val[-].ts)[i]$, by Observation 37. Note that $w_i$ reads $(Val[l].ts)[l]$ before time $t_i$ for every $1 \leq l \leq n$, and $w_i$ writes ($-ts_{w_i}$) to some $Val[-]$ at time $t_i$. Thus, for every $1 \leq l \leq n$, since $(Val[l].ts)[l]$ is non-decreasing, $ts_{w'}[l] \geq ts_{w_i}[l]$. So $ts_{w'} > ts_{w_i}$. Since $w' \notin B_i$, $w' \neq w_i$. By Observation 24, $ts_{w'} \neq ts_{w_i}$ and so $ts_{w'} > ts_{w_i}$. Therefore in both cases, $ts_{w'} > ts_{w_i}$. 

Since $w \in B_i$, by Observation 30 $ts_w \leq ts_{w_i}$. By Claim 38.1, $ts_{w'} > ts_{w_i} \geq ts_{w'}$. 

We now show that for every two operations $o_1$ and $o_2$, if $o_1$ completes before $o_2$ starts in $H$ and $o_1, o_2 \in S$, then $o_1$ is before $o_2$ in $S$. 

Lemma 39. If a write operation $w$ completes before a write operation $w'$ starts and $w, w' \in S$, then $w$ is before $w'$ in $S$. 

Proof. Assume a write operation $w$ completes before a write operation $w'$ starts and $w, w' \in S$. By Observation 30 there are $i$ and $j$ such that $w \in B_i$ and $w' \in B_j$. By line 7 of Algorithm 3 $w$ and $w'$ are active at time $t_i$ and $t_j$, respectively. Since $w'$ starts after $w$ completes, $t_i < t_j$ and so $i < j$. Thus, $w$ is before $w'$ in $S$. 

Lemma 40. If an operation $w$ writes to $Val[-]$ at time $t$ and $w \in B_i$ for some $i \geq 1$, then $t_i \leq t$. 

Proof. Assume, for contradiction, an operation $w$ writes to $Val[-]$ at time $t$, $w \in B_i$ for some $i \geq 1$, and $t_i > t$. By Observation 28 there is a $k \geq 1$ such that $w = w_k$ and $t = t_k$. By lines 6 and 10 of Algorithm 3 (the $k$th iteration of the for loop), $w_k \in WS_k$. Since $t_i > t = t_k$, $k \leq i - 1$. By lines 10 and 13 of Algorithm 3, $WS_k$ is a prefix of $WS_{i-1}$. Since $w_k \in WS_k$, $w_k \in WS_{i-1}$. Thus, by line 7 of Algorithm 3, $w_k \notin B_i$. Since $w_k = w$, this contradicts that $w \in B_i$. 

Lemma 41. If a read operation $r$ completes before a write operation $w$ starts and $r, w \in S$, then $r$ is before $w$ in $S$. 

Proof. Assume a read operation $r$ completes before a write operation $w$ starts and $r, w \in S$. Let $(-, ts)$ denote the value that $r$ returns. 

Case 1: $ts = [0, \ldots, 0]$. By lines 25 and 26 of Algorithm 3, $r$ is before all the write operations in $S$. Thus, $r$ is before $w$ in $S$. 

Case 2: $ts \neq [0, \ldots, 0]$. By Observation 26, an operation $w'$ writes $(-, ts)$ to $Val[-]$ and by Corollary 31, $w' \in S$. By lines 28 and 29 of Algorithm 3, $r$ is after $w'$ and before any subsequent write in $S$. So to show $r$ is before $w$ in $S$, it is sufficient to show that $w'$ is before $w$ in $S$. 

Claim 41.1 $w'$ is before $w$ in $S$. 

Proof. Since $w', w \in S$, by Observation 30 there are $i$ and $j$ such that $w' \in B_i$ and $w \in B_j$. Let $t'$ be the time when $w'$ writes $(-, ts)$ to $Val[-]$. Since $w' \in B_i$, by Lemma 10, $t_i \leq t'$. Since $r$ returns $(-, ts)$, $r$ reads $(-, ts)$ from $Val[-]$ and so $r$ completes after $t' \geq t_i$. Since $w$ starts after $r$ completes, $w$ starts after time $t_i$. Since $w \in B_j \subseteq C_j$, by line 7 of Algorithm 3 $w$ is active at time $t_j$. Thus, $t_i < t_j$ and so $i < j$. By Observation 24, $w'$ is before $w$ in $S$. Therefore, in both cases 1 and 2, $r$ is before $w$ in $S$. 

Lemma 42. If a write operation $w$ writes to $Val[-]$ before a read operation $r$ starts and $w, r \in S$, then $w$ is before $r$ in $S$. 

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Proof. Assume a write operation \( w \) writes to \( \text{Val}[-] \) before a read operation \( r \) starts and \( w, r \in S \). Let \((-ts)\) denote the value that \( r \) returns. By Lemma 27, \( ts \geq ts_w \) and so \( ts \neq [0, \ldots, 0] \). By Observation 26, an operation \( w' \) writes \((-ts)\) to \( \text{Val}[-] \) and by Corollary 31, \( w' \in S \). By lines 28 and 29 of Algorithm 3, \( r \) is after \( w' \) in \( S \). Since \( ts \geq ts_w \), there are two cases:

- **Case 1:** \( ts = ts_w \). By Observation 24, \( w = w' \). So \( r \) is after \( w = w' \) in \( S \).

- **Case 2:** \( ts > ts_w \). Since \( r \) is after \( w' \) in \( S \), to show \( w \) is before \( r \) in \( S \), it is sufficient to show that \( w \) is before \( w' \) in \( S \).

**Claim 42.1** \( w \) is before \( w' \) in \( S \).

**Proof.** Since \( w, w' \in S \), by Observation 30, there are \( i \) and \( j \) such that \( w \in B_i \) and \( w' \in B_j \).

- **Case (a):** \( i \neq j \). Since \( w \in B_i \), \( w' \in B_j \), \( i \neq j \), and \( ts > ts_w \), by Lemma 38, \( j > i \) (otherwise \( ts < ts_w \)). Thus, by Observation 32, \( w \) is before \( w' \) in \( S \).

- **Case (b):** \( i = j \). Then \( w, w' \in B_i \).

**Claim 42.1.1** \( w' = w_i \).

**Proof.** Since \( w \in B_i \subseteq C_i \), by line 7 of Algorithm 3, \( w \) is active at time \( t_i \). Since \( r \) starts after \( w \) completes, \( r \) starts after \( t_i \). Then by Lemma 27, \( ts \geq ts_w \). Since \( w' \in B_i \), by Observation 36, \( ts \leq ts_w \). Thus, \( ts \geq ts_w \) and by Observation 24, \( w = w_i \) before \( w' \) in \( S \).

Since \( ts \neq ts_w \), \( w' \neq w \). Thus, \( w \neq w_i \). Since \( w \in B_i \), by line 10 of Algorithm 3, \( w \) is before \( w_i = w' \) in \( S \).

Thus, in both cases (a) and (b), \( w \) is before \( w' \) in \( S \). Therefore, in both cases 1 and 2, \( w \) is before \( r \) in \( S \).

Note that a completed write operation \( w \) writes to \( \text{Val}[-] \) before it completes. Thus, Lemma 42 immediately implies the following:

**Corollary 43.** If a write operation \( w \) completes before a read operation \( r \) starts and \( w, r \in S \), then \( w \) is before \( r \) in \( S \).

**Lemma 44.** If a read operation \( r \) completes before a read operation \( r' \) starts and \( r, r' \in S \), then \( r \) is before \( r' \) in \( S \).

**Proof.** Assume a read operation \( r \) completes before a read operation \( r' \) starts and \( r, r' \in S \). Let \((-ts)\) denote the value that \( r \) returns and \((-ts')\) denote the value that \( r' \) returns.

**Case A:** \( ts' = ts \). By lines 23 and 24 of Algorithm 3, \( r \) and \( r' \) are in the same sequence \( S_R \) that is ordered by their start time. Since \( r' \) starts after \( r \) completes, \( r \) is before \( r' \) in \( S_R \). By lines 26 and 29, \( r \) is before \( r' \) in \( S \).

**Case B:** \( ts' \neq ts \).

**Subcase B.1:** \( ts = [0, \ldots, 0] \). By lines 25 and 26 of Algorithm 3, \( r \) is before all the write operations in \( S \). Since \( ts' \neq ts \), \( ts' \neq [0, \ldots, 0] \). By Observation 26, an operation \( w' \) writes \((-ts')\) to \( \text{Val}[-] \) and by Corollary 31, \( w' \in S \). By lines 28 and 29 of Algorithm 3, \( r' \) is after \( w' \) in \( S \). Since \( r \) is before \( w' \) in \( S \), \( r \) is before \( r' \) in \( S \).

**Subcase B.2:** \( ts > [0, \ldots, 0] \). By Observation 26, an operation \( w \) writes \((-ts)\) to \( \text{Val}[-] \) and by Corollary 31, \( w \in S \). Since \( r \) reads \((-ts)\) from \( \text{Val}[-] \) and \( r' \) starts after \( r \) completes, \( r' \) starts after \( w \) writes \((-ts)\) to \( \text{Val}[-] \). By Lemma 27, \( ts' \geq ts \). So \( ts' \geq ts > [0, \ldots, 0] \). By Observation 26, an operation \( w' \) writes \((-ts')\) to \( \text{Val}[-] \) and by Corollary 31, \( w' \in S \). Since \( ts' \neq ts \), \( w' \neq w \). By lines 28 and 29 of Algorithm 3, \( r' \) is after \( w' \) before any subsequent write in \( S \) and \( r \) is after \( w \) before any subsequent write in \( S \). Since \( r' \) starts after \( w \) writes to \( \text{Val}[-] \), by Lemma 42, \( w \) is before \( r' \) in \( S \). Thus, \( w \) is before \( w' \) in \( S \) and so \( r \) is before \( w' \) in \( S \). Since \( r' \) is after \( w' \) in \( S \), \( r \) is before \( r' \) in \( S \).

Therefore, in both cases A and B, \( r \) is before \( r' \) in \( S \).

From Lemma 39, Lemma 41, Corollary 43 and Lemma 44, we have the following:

**Corollary 45.** For every two operations \( o_1 \) and \( o_2 \), if \( o_1 \) completes before \( o_2 \) starts and \( o_1, o_2 \in S \), then \( o_1 \) is before \( o_2 \) in \( S \).
Lemma 46. $S$ contains all completed operations of $H$ and possibly some non-completed ones.

Proof. By Corollary 31, $S$ contains all the completed write operations in $H$ and possibly some non-completed ones. Let $r$ be any completed read operation in $H$. Since $r$ is completed, $r$ returns some value $(-ts)$. If $ts = [0, \ldots, 0]$, by line 26 of Algorithm 3, $r$ is in $S$. If $ts \neq [0, \ldots, 0]$, by Observation 26 and Corollary 31, there is a write operation $w$ in $S$ that writes $(v, ts)$. So by lines 28 and 29 of Algorithm 3, $r$ is in $S$. In both cases, $S$ contains the completed read operation $r$. Thus, $S$ contains all completed operations of $H$ and possibly some non-completed ones.

Observation 47. For any read operation $r$ in $S$, if no write precedes $r$ in $S$, then $r$ returns the initial value of the register; Otherwise, $r$ returns the value written by the last write that occurs before $r$ in $S$.

Lemma 48. $f$ is a linearization function of $H$.

Proof. Recall that: (1) $S$ is the output of Algorithm 3 “executed” on an arbitrary history $H \in \mathcal{H}$ of Algorithm 2 (the implementation on MRMW registers), and (2) Algorithm 3 defines the linearization function $f$; in other words, $f(H) = S$. Furthermore, $S$ satisfies properties 1, 2, and 3 of Definition 2 by Lemma 46, Corollary 45, and Observation 47, respectively. Thus, $f$ is a linearization function of $H$.

To prove that $f$ is a write strong-linearization function for the set of histories $\mathcal{H}$ of Algorithm 2, it now suffices to show that $f$ also satisfies property (P) of Definition 1, namely:

Lemma 49. For any $G, H \in \mathcal{H}$, if $G$ is a prefix of $H$, then the sequence of write operations in $f(G)$ is a prefix of the sequence of write operations in $f(H)$.

Proof. Consider two histories $G \in \mathcal{H}$ and $H \in \mathcal{H}$ such that $G$ is a prefix of $H$. If $G = H$, the lemma trivially holds. Henceforth we assume that $G$ is a proper prefix of $H$, and so $G$ is finite.

In the following we use superscripts $G$ and $H$ to distinguish the value of the variables of Algorithm 3 (that defines the linearization function $f$) when it is applied to input $G$ or $H$. For example, $WS^G_i$ denotes the value of $WS_i$ of Algorithm 3 on input $G$, and $WS^H_i$ denotes the value of $WS_i$ of Algorithm 3 on input $H$. Let $w_1, w_2, \ldots, w_k$ be the operations that write to $Val[-]$ in history $G \in \mathcal{H}$. Since $G$ is a prefix of $H$, then $w_1, w_2, \ldots, w_k$ are also the first $k$ operations that write to $Val[-]$ in history $H \in \mathcal{H}$. Furthermore, for $1 \leq i \leq k$, $w_i$ writes to $Val[-]$ at the same time in $G$ and $H$, say at time $t_i$.

Claim 49.1 $WS^G_k = WS^H_k$.

Proof. We use induction to prove that for all $0 \leq i \leq k$, $WS^G_i = WS^H_i$.

- **Base Case:** $i = 0$. By line 4 of Algorithm 3 ($WS^G_0 = WS^H_0 = ()$). The claim holds.

- **Inductive Step:** assume for some $0 \leq i < k$, $WS^G_i = WS^H_i$ (IH).

  **Case 1:** $w_{i+1} \in WS^G_i$. By (IH), $w_{i+1} \in WS^H_i$. By line 13 of Algorithm 3, $WS^G_{i+1} = WS^G_i$ and $WS^H_{i+1} = WS^H_i$. So by (IH), $WS^G_{i+1} = WS^H_{i+1}$.

  **Case 2:** $w_{i+1} \notin WS^G_i$. By (IH), $w_{i+1} \notin WS^H_i$. Since $G$ is a prefix of $H$, the set of write operations that are active at time $t_{i+1}$ is the same in $G$ and $H$. So by (IH) and line 7 of Algorithm 3, $C^G_{i+1} = C^H_{i+1}$. Furthermore, for all $w \in C^G_{i+1} = C^H_{i+1}$, $ts^G(w) = ts^H(w)$. By line 9 of Algorithm 3, $B^G_{i+1} = B^H_{i+1}$. So the sequence of operations $w \in B^G_{i+1}$ in increasing order of $ts^G(w)$ is equal to the sequence of operations $w \in B^H_{i+1}$ in increasing order of $ts^H(w)$. Thus, by (IH) and line 10 of Algorithm 3, $WS^G_{i+1} = WS^H_{i+1}$.

In both cases, the claim holds.

Thus, since $WS^G_k$ is a prefix of $WS^H$, $WS^G_i$ is a prefix of $WS^H$. Since $w_k$ is the last operation that writes to $Val[-]$ in $G$, $WS^G = WS^G_k$. So $WS^G$ is a prefix of $WS^H$. Note that $WS^G$ and $WS^H$ are the sequences of write operations in $f(G)$ and $f(H)$, respectively. So the lemma holds.

By Lemmas 48, 49, the function $f$ defined by Algorithm 3 is a write strong-linearization function for the set of histories $\mathcal{H}$ of Algorithm 2. Therefore:

Theorem 10. Algorithm 2 is a write strongly-linearizable implementation of a MWMR register from SWMR registers.
Appendix D  Proof of Theorem 12

We now prove Theorem 12 in Section 5, namely, Algorithm 4 is a linearizable implementation of a SWMR register from SWMR registers. Let \( \mathcal{H} \) be the set of histories of the Algorithm 4. Consider an arbitrary history \( H \in \mathcal{H} \). We first note that the timestamps of write operations respect the causal order of write events (they are Lamport clocks for these events).

**Lemma 50.** If operations \( w \) and \( w' \) write \((-ts)\) and \((-ts')\) to \( \text{Val}[\cdot]\), respectively, and \( w \) writes to \( \text{Val}[\cdot] \) before \( w' \) starts, then \( ts < ts' \).

*Proof.* Suppose operations \( w \) and \( w' \) write \((-ts)\) and \((-ts')\) to \( \text{Val}[\cdot] \) respectively and \( w \) writes to \( \text{Val}[\cdot] \) before \( w' \) starts. Then \( w' \) reads all \( \text{Val}[\cdot] \) after \( w \) writes \((-ts)\) to \( \text{Val}[\cdot] \). Since the timestamp in each \( \text{Val}[\cdot] \) are non-decreasing, \( w' \) reads \((-ts'\)) from \( \text{Val}[\cdot] \) for some \( ts'' \geq ts \). By lines 3, 6 of Algorithm 4 \( ts'.sq > ts''.sq \) and so \( ts' > ts'' \). So \( ts \leq ts'' < ts' \).  

**Observation 51.** The tuples \((v,ts)\) and \((v',ts')\) written to \( \text{Val}[\cdot] \) by two distinct write operations have distinct timestamps, i.e., \( ts \neq ts' \).

**Observation 52.** If a read operation \( r \) returns \((v,ts)\) such that \( ts.sq \neq 0 \), then there is a unique write operation \( w \) that writes \((v,ts)\) to \( \text{Val}[\cdot] \).

**Observation 53.** If a read operation \( r \) returns \((-ts)\) such that \( ts.sq = 0 \) then \( ts = (0,n) \).

Observation 53 implies:

**Observation 54.** If a read operation \( r \) returns \((-ts)\) and a read operation \( r' \) returns \((-ts')\) such that \( ts' > ts \), then \( ts'.sq > 0 \).

**Definition 55.** Let \( f \) be a function that maps the arbitrary history \( H \in \mathcal{H} \) of Algorithm 4 to a sequential history \( f(H) = S \) such that the following holds:

(i) \( S \) contains:

(a) all the write operations that write to \( \text{Val}[\cdot] \) (line 4 of Algorithm 4) in \( H \), and

(b) all the read operations that complete, i.e., return some value \((v,ts)\) (line 12 of Algorithm 4) in \( H \).

(ii) If two write operations \( w \) and \( w' \) write \((-ts)\) and \((-ts')\) to \( \text{Val}[\cdot] \) in \( H \) such that \( ts < ts' \), then \( w \) is before \( w' \) in \( S \).

(iii) If a read operation \( r \) returns some \((-ts)\) with \( ts.sq = 0 \) in \( H \), then \( r \) occurs in \( S \) before every write operation \( w \) in \( S \).

(iv) If a read operation \( r \) returns some \((-ts)\) with \( ts.sq \neq 0 \) in \( H \), then \( r \) occurs in \( S \) as follows:

(a) after the unique write operation \( w \) that writes \((-ts)\) in \( S \) (the operation \( w \) is well-defined by Observation 52), and

(b) before every other subsequent write operation in \( S \).

(v) If two read operations \( r \) and \( r' \) read some \((-ts)\), and \( r \) completes before \( r' \) starts in \( H \), then \( r \) occurs before \( r' \) in \( S \).

We now show that \( f(H) = S \) satisfies properties 1, 2 and 3 of Definition 2, and so \( f \) is a linearization function for the set of histories \( \mathcal{H} \) of Algorithm 4.

**Lemma 56.** \( S \) contains all completed operations of \( H \) and possibly some non-completed ones.

*Proof.* This follows immediately by (i) of Definition 55 and the fact that every completed write operation writes to \( \text{Val}[\cdot] \) (line 6 of Algorithm 4) before it completes in \( H \).  

By Lemma 50 and (ii) of Definition 55 we have:
Corollary 57. If a write operation \( w \) writes to \( \text{Val}[-] \) before a write operation \( w' \) starts and \( w, w' \in S \) then \( w \) is before \( w' \) in \( S \).

Corollary 58. If a write operation \( w \) completes before a write operation \( w' \) starts and \( w, w' \in S \), then \( w \) is before \( w' \) in \( S \).

Lemma 59. If a read operation \( r \) completes before a write operation \( w \) starts and \( r, w \in S \), then \( r \) is before \( w \) in \( S \).

Proof. Assume a read operation \( r \) completes before a write operation \( w \) starts and \( r, w \in S \). Since \( w \in S \), by \([1]\) \( w \) writes some \((-ts)\) to \( \text{Val}[-] \). Let \((-ts')\) denote the value that \( r \) returns.

Case 1: \( ts'.sq = 0 \). By \([iii]\) of Definition 55 \( r \) is before all the write operations in \( S \). So \( r \) is before \( w \) in \( S \).

Case 2: \( ts'.sq \neq 0 \). By \([iv]\) of Definition 55 there is a unique write operation \( w' \in S \) that writes \((-ts')\) to \( \text{Val}[-] \) such that \( r \) is after \( w' \) and before any subsequent write operations in \( S \). Since \( r \) reads \((-ts')\) from \( \text{Val}[-] \) and \( w \) starts after \( r \) completes, \( w \) starts after \( w' \) writes \((-ts')\) to \( \text{Val}[-] \). By Corollary 57 \( w' \) is before \( w \) in \( S \). So \( r \) is before \( w \) in \( S \).

Lemma 60. If a write operation \( w \) completes before a read operation \( r \) starts and \( w, r \in S \), then \( r \) is before \( w \) in \( S \).

Proof. Assume a write operation \( w \) completes before a read operation \( r \) starts and \( w, r \in S \). Since \( w \) completes, \( w \) writes some \((-ts)\) to \( \text{Val}[-] \). Let \((-ts')\) denote the value that \( r \) returns. Since \( w \) completes before \( r \) starts, \( r \) reads all \( \text{Val}[-] \) after \( w \) writes \((-ts)\) to \( \text{Val}[-] \). Since the timestamp in each \( \text{Val}[-] \) are non-decreasing, \( r \) reads \((-ts'')\) from \( \text{Val}[-] \) for some \( ts'' \geq ts \). By line 11 of Algorithm 4 \( ts'' \leq ts' \). So \( ts \leq ts'' \leq ts' \).

Case 1: \( ts = ts' \). By Observation 51 \( r \) returns the value that \( w \) writes. So by \([iv]\) of Definition 55 \( r \) is after \( w \) in \( S \).

Case 2: \( ts < ts' \). By Observation 54 \( ts'.sq > 0 \). By \([iv]\) of Definition 55 some write operation \( w' \in S \) writes \((-ts')\) to \( \text{Val}[-] \) and \( r \) is after \( w' \) in \( S \). Since \( ts < ts' \), by \([iii]\) of Definition 55 \( w \) is before \( w' \) in \( S \). Since \( r \) is after \( w', w \) is before \( r \) in \( S \).

Lemma 61. If a read operation \( r \) completes before a read operation \( r' \) starts in \( H \) and \( r, r' \in S \), then \( r \) is before \( r' \) in \( S \).

Proof. Assume a read operation \( r \) completes before a read operation \( r' \) starts in \( H \) and \( r, r' \in S \). Let \((-ts)\) and \((-ts')\) denote the values that \( r \) and \( r' \) return, respectively. Since \( r \) completes before \( r' \) starts, \( r' \) reads all \( \text{Val}[-] \) after \( r \) reads \((-ts)\) from \( \text{Val}[-] \). Since the timestamps in each \( \text{Val}[-] \) are non-decreasing, \( r' \) reads \((-ts'')\) from \( \text{Val}[-] \) for some \( ts'' \geq ts \). By line 11 of Algorithm 4 \( ts'' \leq ts' \). So \( ts \leq ts'' \leq ts' \).

Case 1: \( ts = ts' \). Since \( r \) completes before \( r' \) starts, \( r \) is before \( r' \) in \( S_R \). So by \([v]\) of Definition 55 \( r \) is before \( r' \) in \( S \).

Case 2: \( ts < ts' \). By Observation 54 \( ts'.sq > 0 \). By \([iv]\) of Definition 55 there is a write operation \( w' \in S \) that writes \((-ts')\) to \( \text{Val}[-] \) such that \( r' \) is after \( w' \) in \( S \).

Subcase 2.1: \( ts.sq = 0 \). By \([iii]\) of Definition 55 \( r \) is before all the write operations in \( S \). Then \( r \) is before \( w' \) in \( S \). So \( r \) is before \( r' \) in \( S \).

Subcase 2.2: \( ts.sq \neq 0 \). By \([iv]\) of Definition 55 some write operation \( w \in S \) writes \((-ts)\) to \( \text{Val}[-] \) and \( r \) is after \( w \) and before any subsequent write operations in \( S \). Since \( ts < ts' \), by \([ii]\) of Definition 55 \( w \) is before \( w' \) in \( S \). So \( r \) is before \( w' \) in \( S \). Since \( r' \) is after \( w' \) in \( S \), \( r \) is before \( r' \) in \( S \).

By Corollary 58 Lemma 59 Lemma 60 and Lemma 61 we have:

Corollary 62. If an operation \( o \) completes before an operation \( o' \) starts in \( H \) and \( o, o' \in S \), then \( o \) is before \( o' \) in \( S \).

By \([iii]\) and \([iv]\) of Definition 55 we have:

Observation 63. For any read operation \( r \) in \( S \), if no write operation precedes \( r \) in \( S \), then \( r \) reads the initial value of the register; otherwise, \( r \) reads the value written by the last write operation that occurs before \( r \) in \( S \).
Lemma 64. \( f \) is a linearization function for the set of histories \( \mathcal{H} \) of Algorithm \( 4 \).

Thus:

Theorem 12. Algorithm \( 4 \) is a linearizable implementation of a MWMR register from SWMR registers.

Appendix E  Proof of Theorem 14

We now prove Theorem 14 in Section 6, namely, any linearizable implementation of SWMR registers is write strongly-linearizable (this holds for message-passing, shared-memory, and hybrid systems). Thus, the well-known ABD implementation of SWMR registers in message-passing systems is not only linearizable; it is actually write strongly-linearizable. (This implementation however is not strongly linearizable [20].)

Consider an arbitrary implementation \( \mathcal{A} \) of a SWMR register. Let \( \mathcal{H} \) be the set of histories of \( \mathcal{A} \). Since \( \mathcal{A} \) implements a single-writer register, the following holds:

Observation 65. In any history \( H \in \mathcal{H} \),

1. there are no concurrent write operations, and
2. there is at most one incomplete write operation.

By part 1 of Observation 65 and property 2 of Definition 2, we have the following:

Observation 66. For any history \( H \in \mathcal{H} \) and any linearization function \( f \) of \( \mathcal{H} \), the write operations in \( f(H) \) are totally ordered by their start time in \( H \).

Lemma 67. If \( \mathcal{A} \) is linearizable, then \( \mathcal{A} \) is write strongly-linearizable.

Proof. Assume \( \mathcal{A} \) is linearizable. By Definition 5, there is a linearization function \( f \) for \( \mathcal{H} \). Consider a function \( f^* \) that is modified from \( f \) as follows: for any history \( H \) and its linearization \( f(H) \), if the last operation \( o \) in \( f(H) \) is a write operation that is incomplete in \( H \), then we obtain \( f^*(H) \) by removing \( o \) from \( f(H) \); otherwise, \( f^*(H) \) equals \( f(H) \).

Claim 67.1 If a write operation \( w \) is in \( f^*(H) \), then \( w \) is completed or read by some read operation in \( H \).

Proof. Assume, for contradiction, a write operation \( w \in f^*(H) \) is incomplete and not read by any read operation in \( H \). Since \( w \in f^*(H) \), \( w \) is in \( f(H) \) such that \( w \) is not the last operation in \( f(H) \) (\( \ast \)). Since \( w \) is incomplete, by Observation 65, \( w \) is the last write operation in \( H \). By Observation 66, \( w \) is the last write operation in \( f(H) \). Furthermore, since \( w \) is not read by any read operation in \( H \), no read operation is after \( w \) in \( f(H) \). Thus, \( w \) is the last operation in \( f(H) \), which contradicts (\( \ast \)).

Claim 67.2 If a write operation \( w \) is completed or read by some read operation in \( H \), then \( w \) is in \( f^*(H) \).

Proof. Assume a write operation \( w \) is completed or read by some read operation in \( H \).

Case 1: \( w \) is completed in \( H \). Since \( f \) is a linearization function for \( \mathcal{H} \), by property 1 of Definition 2, \( w \) is in \( f(H) \). Since \( f^*(H) \) removes only the incomplete operation from \( f(H) \), \( w \) is in \( f^*(H) \).

Case 2: \( w \) is read by some read operation \( r \) in \( H \). Since \( f \) is a linearization function for \( \mathcal{H} \), by property 3 of Definition 2, \( w \) is before \( r \) in \( f(H) \) and so \( w \) is not the last operation in \( f(H) \). Since \( f^*(H) \) removes only the last operation from \( f(H) \), \( w \) is in \( f^*(H) \).

Thus, in both cases 1 and 2, \( w \) is in \( f^*(H) \).

Claim 67.3 \( f^* \) is a linearization function of \( \mathcal{H} \).

Proof. Consider any history \( H \in \mathcal{H} \). Since \( f^*(H) \) removes from \( f(H) \) only the operation that is incomplete in \( H \), \( f^*(H) \) still satisfies properties 1 and 2 of Definition 2. Since \( f^*(H) \) removes only the last operation from \( f(H) \), \( f^*(H) \) still satisfies property 3 of Definition 2. Therefore, \( f^* \) is a linearization function of \( \mathcal{H} \).
Claim 67.4 \( f^* \) satisfies property (P) of Definition 4.

Proof. Consider histories \( G, H \in \mathcal{H} \) such that \( G \) is a prefix of \( H \). Let \( W_G \) and \( W_H \) denote the write sequences in \( f^*(G) \) and \( f^*(H) \) respectively. By Claim 67.1, all the operations in \( W_G \) are completed in \( G \) or read by some read operations in \( G \). Since \( G \) is a prefix of \( H \), all operations in \( W_G \) are also completed in \( H \) or read by some read operations in \( H \). So by Claim 67.2, \( W_H \) contains all the operations in \( W_G \). By Observation 66, the write operations in \( W_G \) and \( W_H \) are totally ordered by their start time in \( G \) and \( H \), respectively. Then since \( G \) is a prefix of \( H \) and \( W_H \) contains all the operations in \( W_G \), \( W_G \) is a prefix of \( W_H \). So \( f \) satisfies property (P) of Definition 4.

Thus, \( f \) is a write strong-linearization function for \( \mathcal{H} \) and \( A \) is write strongly-linearizable.

Theorem 14. Any linearizable implementation of a SWMR register is necessarily write strongly-linearizable.