In this paper, we formally describe the three challenges of mapping surface code on superconducting devices, and present a comprehensive synthesis framework to overcome these challenges. The proposed framework consists of three optimizations. First, we adopt a geometrical method to allocate data qubits which ensures the existence of shallow syndrome extraction circuit. The proposed data qubit layout optimization reduces the overhead of syndrome extraction and serves as a good initial point for following optimizations. Second, we only use bridge qubits enclosed by data qubits and reduce the number of bridge qubits by merging short path between data qubits. The proposed bridge qubit optimization reduces the probability of bridge qubit conflicts and further minimizes the syndrome extraction overhead. Third, we propose an efficient heuristic to schedule syndrome extractions. Based on the proposed data qubit allocation, we devise a good initial schedule of syndrome extractions and further refine this schedule to minimize the total time needed by a complete surface code error detection cycle. Our experiments on mainstream superconducting quantum architectures have demonstrated the efficiency of the proposed framework.
1 Introduction

Quantum hardware has advanced significantly in the last decade and demonstrated ‘Quantum Supremacy’ for the first time in 2020 [1]. Among various quantum hardware technologies [2,3,5,9], the superconducting (SC) qubit is currently one of the most promising technique candidates for building quantum processors due to its low error rates, individual qubit addressability, fabrication scalability, etc. Many latest quantum processors adopt the SC technology, e.g., IBM’s 65-qubit heavy-hexagon-architecture chip [3], Rigetti’s 32-qubit octagonal-architecture chip [9], Google’53-qubit 2D-lattice chip [1].

The low error rate of SC processors makes them an ideal platform for quantum error correction (QEC) [10-14] and thus realizing fault-tolerant (FT) quantum computation. Among various QEC codes, surface code [15] is a popular choice as it possesses one of the best error correction capabilities and can tolerate a high (up to 1%) physical error rate. Even on noisy near-term devices, the surface code family can encode an arbitrarily accurate logical qubit with a large enough array of physical qubits. This makes surface code one of the most feasible QEC choices for demonstrating near-term FT quantum computation.

With a readily available surface code array, many recent research efforts have been put into improving the efficiency of FT quantum computation, varying from compilation [16,17], communication scheduling [18,19], and micro-controller design [20]. All these works are based on a nontrivial assumption: we already find a scalable way to compose logical qubits on existing quantum devices, in particular SC devices, with the surface code family.

Yet, implementing surface code on SC devices itself is a difficult problem. The implementation of surface code separates physical qubits into two categories. The first category of qubits is called “data qubits” and is used to encode the logical qubit. Physical qubits in the second category are used to detect errors on data qubits, and are thus called “syndrome qubits”. Each syndrome qubit extracts error syndromes on four neighboring data qubits with a specialized quantum circuit, named “measurement circuit” [15]. To make measurement circuits executable, surface code requires a 2D-lattice qubit array where each qubit is connected or coupled to four other qubits. Nonetheless, such an architecture is not readily available on many latest quantum processors as the dense connection in the 2D qubit array would induce a high physical error rate. Previous work tackles the gap between surface code and the sparse-connected SC device either by tailoring the architecture with tunable coupling [5] or by designing a QEC code upon the surface code [21]. The former method is expensive and may introduce extra device noises while the latter method is not automated.

In this paper, we propose the first automatic synthesis framework “Surfmap” for stitching the surface code family to various SC devices, without any variation in device or surface code. Our framework builds upon recent theoretical work on generating individual measurement circuits over sparse-connected SC devices [21,22]. These works generalize the syndrome qubit to a tree of low-degree qubits (a.k.a a bridge tree with constituent qubits called bridge qubits) that connects to the four target data qubits. In essential, these work trades the qubit degree with the qubit number. Yet, these measurement circuit generation works are far from tackling the overall surface code synthesis. These works cannot generate measurement circuits unless the data qubits and bridge qubits for each measurement circuit are assigned. Even all measurement circuits are generated, how to efficiently execute them is still not answered by these works. Systematically, to tackle the surface code synthesis problem on SC devices, we should address three key challenges. First, the allocation of data qubits. If the four data qubits of a measurement circuit are far away from each other, many bridge qubits will be needed to connect these data qubits. Oppositely, if these data qubits are too close, there will not be enough space for a bridge tree. Second, the selection of bridge qubits. An improper selection of bridge qubits may cause conflicts in measurement circuits that several measurement circuits contend for one bridge qubit. Such bridge qubit conflict will cause a sequential execution of measurement circuits thus increasing the error detection latency and degrading the error correction performance. Third, the execution order of measurement circuits. As indicated above, sequential execution of measurement circuits is not acceptable and an efficient synthesis should utilize the parallelism between measurement circuits, as much as possible.

Our framework decouples the optimization space of surface code synthesis with a modular optimization scheme. To be specific, our framework consists of three key steps.

In the first step, we optimize the allocation of data qubits since data qubits are the key to gluing measurement circuits together, and once allocated their physical mapping should not change to avoid error proliferation. As long as allocated data qubit layout ensures the existence of measurement circuits, we prefer a shorter total distance between data qubits since this reduces bridge qubits overhead for constructing measurement circuits. To enable this optimization, we search data qubits over a series of “rectangular” blocks, with each block created by a pair of three-degree qubits or one four-degree qubit. The key insight behind such design is that existing SC architectures can always be embedded into a 2D lattice and the four data qubits for a measurement circuit exactly form a rectangle in the 2D lattice. Our design ensures the existence of measurement circuits since there are enough high-degree qubits in each rectangle to connect data qubits. Rectangle-based search is efficient as it enables a coarse-grained exploration over the search space. Furthermore, to reduce the possible conflicts of measurement circuits, we require the overlapping between rectangular blocks at most happens on rectangle boundaries.

In the second step, it naturally comes to the optimization of bridge qubits. The optimization goal is to reduce the conflicts between measurement circuits, i.e., reduce the mutual bridge qubits, and minimize the bridge tree connecting data qubits. The key insight for such optimization is that the size of the measurement circuit is proportional to the bridge tree size and measurement circuits without conflicts can be executed together to shorten the time window of error correction cycles. To meet these goals, we first limit the search scope of bridge qubits inside rectangular blocks enclosed by data qubits. Since rectangular blocks have zero overlapping areas, such local search could greatly reduce bridge qubit conflicts. On the other hand, to find small bridge trees, we adopt two different heuristics which complement each other. We then pick the best results from these two methods as bridge tree candidates.
In the third step, we optimize the order of measurement circuit execution. The reason for this optimization is that conflicts between measurement circuits can sometimes be inevitable. In such cases, we have to execute conflicted measurement circuits in sequential. To reduce the total time window of measurement circuits execution in this case, we propose an iterative refinement method. We first place conflicted measurement circuits into different partitions, and then refine the partitions by moving large measurement circuits into one partition while ensuring the compatibility between measurement circuits. The key insight behind such optimization is that when executing measurement circuits in parallel, the execution time depends on the one with the largest circuit depth. By moving large measurement circuits together, we can reduce the execution time of partitions consisting of small measurement circuits.

We evaluate the proposed synthesis framework by comparing it to manually designed QEC codes \cite{21} on two SC architectures. The results show the surface codes synthesized by our framework can achieve equivalent or even better error thresholds. This result is inspiring as it unveils the possibility that automated synthesis by machine can surpass the manual QEC code design of experienced theorists. We also investigate our framework on various mainstream SC architectures and present an analysis of several architecture design options based on the investigation result. The proposed synthesis framework would be of great interest to both QEC researchers and quantum hardware designers. Hardware researchers could benefit from our framework in two aspects: a) they could focus on improving the device without worrying about meeting the requirements of a specific QEC code; b) they can identify inefficient architecture designs for QEC codes with our synthesis framework.

Our contributions in this paper are summarized as follows:

- We promote the importance of a synthesis framework for achieving good QEC implementations towards different quantum hardware architectures.
- We systematically formulate the surface code synthesis problem on SC devices for the first time and identify three key challenges: data qubit allocation, bridge qubit selection and measurement circuit execution scheduling.
- We design and implement a modular synthesis framework that tackles the identified three challenges step by step, with a series of insights extracted from surface code and SC architectures.
- Our evaluation demonstrates the effectiveness of the proposed synthesis framework with one comparative study to manually designed QEC codes and a comprehensive investigation on various mainstream SC architectures.

2 Background

In this section, we introduce the key concepts for understanding the implementation requirements of surface code \cite{14,23,24}. We do not cover the basics of quantum computing and recommend \cite{25} for reference.

![Figure 1: Common components of the surface code. (a) Surface code lattice with data qubits (blue dots) and syndrome qubits (red dots). (b) Z-type syndrome extraction and its circuit. (c) X-type syndrome extraction and its circuit.](image-url)

**Data and syndrome qubits:** Surface code encodes logical qubit information in a 2D lattice of physical qubits shown in Figure 1(a). Physical qubits in the code lattice can be divided into two types: data qubits and syndrome qubits (represented as blue and red dots respectively, see Figure 1(a)). The logical information is encoded in the data qubits. The error information on these data qubits can be extracted by applying surface code operations and measuring syndrome qubits.

**Pauli operator and stabilizer:** In surface codes, the relationship between one syndrome qubits and its neighboring data qubits is represented by the product of an array of Pauli operators (a.k.a Pauli string) labeled on the edges between data qubits and syndrome qubits (Figure 1(b)). For each syndrome qubit, the Pauli string on its edges can be in one of two possible patterns. The first one (Z-type) is shown in Figure 1(b). The connections between the center syndrome qubit and the four data qubits are all labeled by the Z operators and represented by the Pauli string \(Z_aZ_bZ_cZ_d\). The second one (X-type in Figure 1(c)) is similar but all connections are labeled by the X operators and represented by the Pauli string \(X_aX_bX_cX_d\). For these two different patterns, we will have corresponding syndrome measurement circuits to detect errors in the data qubits (shown on the right of Figure 1(b) and (c)). The syndrome extraction circuits project the state of data qubits \(\{a, b, c, d\}\) into the eigenstates of the corresponding Pauli strings. In the context of QEC, the specific Pauli strings that one measures are called **stabilizers** \cite{26} and the syndrome extraction circuits are also known as **stabilizer measurements** \cite{27}. Without ambiguity, we use the stabilizer notation to represent a syndrome extraction. And we denote the stabilizer \(Z_aZ_bZ_cZ_d\) \((X_aX_bX_cX_d)\) with \(Z_{abcd}\) (respectively \(X_{abcd}\)) for simplicity.

**Error detection:** Surface code can detect Pauli X- and Z-errors on data qubits by using Z- and X-type stabilizer measurement circuits, respectively. An error on a data qubit may affect the measurement results of stabilizers associated with this data qubit. By gathering all such stabilizer measurement results, a surface code error correction protocol can infer what errors occurred in the lattice and consequently apply the corresponding correction. Further details of the error correction protocol can be found in \cite{15}. 

---

\[ \text{Pauli string: } \begin{cases} Z_aZ_bZ_cZ_d, & \text{Z-type} \\ X_aX_bX_cX_d, & \text{X-type} \end{cases} \]

\[ \text{Stabilizer measurements: } \{a, b, c, d\} \]
of measurement circuits.

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3.1 Surface code synthesis on SC architectures

We consider implementing the (rotated) surface code in Figure

(b) a quantum device with a hexagon architecture (see Figure

(a)) [21]. In this hexagon device, each qubit connects to at

most three other qubits. This imposes a challenge to synthesize

measurement circuits of a surface code since a syndrome

qubit in either an X- or Z-type stabilizer measurement should con-
nnect to four data qubits (see Figure 1(b) and (c)).

To resolve this constraint, we can introduce ancillary qubits when

synthesizing a stabilizer measurement circuit. Suppose a mapping

of the logical qubit in Figure 2(b) onto the hexagon architecture

is shown in Figure 4(b). To measure the stabilizer

, one needs to connect the four data qubits

{b, c, i, d} with a syndrome qubit. In Figure

(b), data qubits

{b, c, i, d} are mapped to physical qubits

{Q_9, Q_{16}, Q_{11}, Q_{20}}, and the syndrome qubit is on

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Q_{18} and

Q_{18}, Q_{16}, Q_{11}, Q_{20},} one can use the two ancillary

qubits

Q_{17} and

Q_{19}. Qubits

Q_{17}, Q_{18} and

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tree that bridges the gap between data qubits

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3.2 Optimization opportunities

To deploy an entire surface code QEC protocol onto an SC archi-
tecture requires synthesizing a series of non-independent stabilizer
measurements, which is far more complicated than handling one
single stabilizer measurement. In this section, we formulate the
overall surface code synthesis problem into three key steps: data
qubit allocation, bridge tree construction, and stabilizer measure-
ment schedule. We briefly introduce the objectives and the design
considerations of each step.

Data qubit allocation: In this paper, we choose to allocate and
fix the position of data qubits first as data qubits are the key to
 glueing stabilizer measurement circuits together and should not be
changed once allocated. Comparing to data qubits, bridge qubits
are dynamic resources which are initialized, used, measured and
decoupled in every QEC cycle, making them unsuitable for a pre-
allocation.

The layout of the data qubits affects how efficiently stabilizer
measurement circuits can be executed. For example, we syn-
thesize the (rotated) distance-3 surface code in Figure 2(b) with

Our framework targets at the high-level synthesis of the entire sur-
face code and use these low-level stabilizer synthesis methods as
the backend.

3 Design Overview

The surface code relies on a 2D square-grid connectivity between
physical qubits, while actual superconducting (SC) processors may
not satisfy this requirement and then fail to execute the vanilla sur-
face code. In this paper, we aim to mitigate this gap by resynthesiz-
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two data qubit layouts in Figure 4(b) and Figure 4(c). In Figure 4(b), the stabilizer $X_{idf_e}$ cannot be measured without moving data qubits and inserting SWAP gates, which are not allowed to avoid error proliferation. In contrast, all stabilizer measurements ($\{X_{abhi}, X_{idfe}, X_{fg}, X_{bc}, Z_{beid}, Z_{higf}, Z_{ah}, Z_{de}\}$) can be executed on Figure 4(c) since bridge trees for these stabilizers are readily available.

**Bridge tree construction**: After the data qubits are placed, the next step is to select the bridge qubits and construct bridge trees for stabilizer measurements. The first constraint in this step is that we should minimize the number of bridge qubits since using more physical qubits results in larger measurement circuits which are naturally more error-prone. The second constraint is that the construction of bridge trees affects the efficiency of error detection because two stabilizers can be simultaneously measured only if their bridge trees do not intersect. For instance, referring to Figure 4(c), if we measure $X_{bc}$ with bridge qubits $\{r, s\}$, these two qubits cannot be used as bridge qubits in the measurement circuit of $X_{abhi}$ at the same time because the bridge qubits need to be reset at the beginning of any new measurement circuit. However, if we measure $X_{bc}$ with bridge qubits $\{p, q\}$ in Figure 4(d), we can measure $X_{bc}$ and $X_{abhi}$ in parallel. An efficient bridge qubit selection and tree construction should enable the concurrent measurement of as many stabilizers as possible.

**Stabilizer measurement scheduling**: The third step is to schedule the execution of the stabilizer measurement circuits. It would be desirable to execute the stabilizer measurement in parallel as much as possible since it can reduce the execution time and mitigate the decoherence error. However, stabilizer measurement circuits have overlapped bridge qubits (a.k.a. bridge qubit conflict) cannot be executed simultaneously. For example in Figure 4(c), the measurement circuit of $X_{abhi}$ and $Z_{beid}$ cannot be measured together since they share bridge qubits $\{q9, q10\}$. One possibility is to measure $X_{abhi}$ and $X_{idfe}$ first, then measure $Z_{higf}$ and $Z_{beid}$. Though seems promising, it is not optimal as these two groups of measurements take 20 operation steps in total, using the flag-bridge circuit [22] (Figure 3) as backend. As a comparison, if we measure $X_{abhi}$ and $Z_{higf}$ first and measure $X_{idfe}$ and $Z_{beid}$ second, the total operation step number is only 18. It is usually not a simple task to schedule the stabilizer measurements optimally. Our objective is to identify the potential parallelism in stabilizer measurements and figure out an efficient heuristic scheduling method to minimize the overall error detection cycle time (running all stabilizer measurements once is a cycle in the surface code QEC protocol).

4 Synthesis Algorithm Design

In this section, we introduce our surface code synthesis flow. As discussed above, we will introduce three key steps, data qubit allocation, bridge tree construction, and stabilizer measurement scheduling.

4.1 Data qubit allocator

Since we decided to fix the location of data qubits, the basic requirement is that the measurement circuits can be feasibly constructed for all stabilizers. To ensure this property is guaranteed in the data qubit mapping we found, we have the following proposition regarding the bridge tree construction.

**Proposition 1.** In any bridge tree for a stabilizer having support on four data qubits, there are at least one four-degree node or two three-degree nodes.

**Proof.** For any graph $G(V, E)$ where $V$ is the vertex set and $E$ is the edge set, we have $\sum_{v \in V} \text{deg}(v) = 2|E|$. An $n$-vertex tree always has $n - 1$ edges. A bridge tree with four data qubits has four 1-degree leaf nodes and all other nodes should have degree of at least 2. Therefore we have $4 + \sum_{v \in V \setminus \text{data qubits}} \text{deg}(v) = 2n - 2$ and $\sum_{v \in V \setminus \text{data qubits}} \text{deg}(v) = 2n - 6 = 2(n - 4) + 2$. We only have $n - 4$ vertices after removing the four leaf nodes. So we must have at least one four-degree node or two three-degree nodes.

**Proposition 1** provides a necessary condition for a feasible data qubit layout. For each stabilizer to be executable, we should ensure...
that there are enough three-degree or four-degree qubits around data qubits of this stabilizer. We then introduce a graph-based data qubit layout where we can find bridge trees ‘locally’. A local bridge tree locates inside the spatial area bounded by the data qubits of a stabilizer. Such a bridge tree is promising as it often leads to a shallow measurement circuit. We use the SC device shown in Figure 4(a) to illustrate the data qubit allocation algorithm. We embed the coupling graph of this SC device into a 2D grid so that all qubits can be referenced by the spatial coordinates on the plane. Such embedding is possible as latest SC processors are usually designed in a modular structure.

Since high-degree nodes are critical, we keep a list (denoted by $L_h$) of all three- and four-degree nodes in the device grid and record their coordinates. In Figure 5(a), $L_h = \{Q_2, Q_4, Q_{10}, Q_{12}, Q_{13}, Q_{18}, Q_{21}\}$. We then process the list of high degrees sequentially. For the next node $n_a$ in $L_h$, if it is a three-degree node, we search for its nearest high-degree node $n_b$ and then create a minimal rectangle that contains $n_a$ and $n_b$ as well as their neighboring qubits. If $n_a$ is node with degree $\geq 4$, then we create a rectangle that contains $n_a$ and its neighboring qubits. The rectangle created at this step is called “bridge rectangle”. Figure 5(a) depicts five bridge rectangles resulted from $\{Q_2, Q_{10}\}$, $\{Q_4, Q_{12}\}$, $\{Q_{13}, Q_{21}\}$ and $\{Q_{18}, Q_{10}\}$, and we index them from 1 to 5. There are also other bridge rectangles that can be identified, but we omit them here for simplicity.

We can now determine the position of data qubits by using bridge rectangles. As shown in Figure 4 each data qubit is shared by four stabilizers. Thus, we can fix the position of a data qubit with four bridge rectangles. We begin with rectangle 1 to find four compatible bridge rectangles. We can also begin with rectangle 2 which is created from a four-degree qubit. This will create a different surface code synthesis and we will discuss it in Section 5. Here we focus on rectangle 1. Two bridge rectangles are said to be compatible if their intersection area is zero. As we can see in Figure 5(b), rectangle 2 is not compatible with rectangle 1 and rectangle 4, while rectangles 1, 3, 4, and 5 are mutually compatible. We do not use incompatible rectangles because they may not allow a feasible data qubit mapping. We then search for data qubits in the potential data area (black rectangle in Figure 5(c)) which is enclosed by four compatible bridge rectangles, as shown in Figure 5(c). If the potential data area is empty, we choose another four compatible bridge rectangles. Otherwise, we pick the qubit at the center of the potential data area as a data qubit.

For boundary cases, we may not have enough bridge rectangles to locate one data qubit. For example, for rectangle 3, its bottom right corner is only neighbored by rectangle 5. In this case, we should locate the data qubit with constraints only from these two bridge rectangles. Specifically, a potential data qubit should satisfy: A) its x axis value $\geq$ the largest x axis value in rectangle 3 and 5; B) its y axis value should lie between the largest y axis value of rectangle 3 and the smallest y axis value of rectangle 5. With these spatial constraints, the only qubit we can find is $Q_{14}$, as shown in Figure 5(c). Other data points are found in a similar way.

The final layout for data qubits and syndrome rectangles defined by data qubits are shown in Figure 5(d). A syndrome rectangle is the extension of the bridge rectangle to include allocated data qubits. We can then assign a stabilizer to each syndrome rectangle and synthesize the corresponding measurement circuits locally (using qubits inside each syndrome rectangle). The syndrome rectangle ensures the existence of local bridge trees and enables a natural data qubit assignment for the assigned stabilizer. For the stabilizer $X_{abcd}$ (or $Z_{abcd}$) in Figure 4 we can simply assign the topmost data qubit in a syndrome rectangle to be the data qubit ‘a’, with the leftmost, rightmost, and bottom data qubit being data qubits ‘b’, ‘c’, ‘d’, respectively. In the next section, we will discuss how to find an efficient bridge tree to connect data qubits $\{a, b, c, d\}$.

### 4.2 Bridge tree finder

After locating the data qubits and syndrome rectangles, we then construct the bridge tree for each syndrome rectangle. Since syndrome rectangles only intersect at borderlines, strict local bridge

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Figure 5: Data qubit allocation example. (a) A modified device from Figure 4(a). Red circles indicate physical qubits with high degree of connectivity (i.e. with 3 or more edges). (b) Finding compatible bridge rectangles. (c) Locating data qubits. (d) Final data qubit layout and syndrome rectangles.
Algorithm 1: Data qubit allocation

Input: Device architecture graph \( G \)
Output: Data qubit layout \( \text{data} \_\text{layout} \)
1: \( L_0 = \) all three- and four-degree nodes in \( G \);
2: \( \text{bridge} \_\text{rects} = [] \); \( \text{// the set of bridge rectangles} \)
3: for \( n_a \) in \( L_0 \) do
4: \( \text{if } \deg(n_a) = 3 \) then
5: \( n_b = \) the nearest high-degree node of \( n_a \);
6: \( \text{rect} = \) the minimal rectangle containing \( n_a, n_b \) and their neighboring qubits;
7: else
8: \( \text{rect} = \) the minimal rectangle containing \( n_a \) and its neighboring qubits;
9: end
10: \( \text{bridge} \_\text{rects}.append(\text{rect}); \)
11: end
12: \( r_0 = \) the bridge rectangle at the top left corner of \( G \);
13: \( \text{bridge} \_\text{rect} \_\text{tuple} = [] \); \( \text{// tuples of compatible bridge rectangles} \)
14: repeat
15: for \( (r_1, r_2, r_3) \in \cap^3 \text{bridge} \_\text{rects} \) do
16: \( \text{potent} \_\text{dqbits} \) = qubits enclosed by \( r_0, r_1, r_2, r_3 \); \( \text{// potential data area} \)
17: if \( \text{potent} \_\text{dqbits} \neq \emptyset \) then
18: \( \text{bridge} \_\text{rect} \_\text{tuple}.append((r_0, r_1, r_2, r_3)); \)
19: break;
20: end
21: set \( r_0 \) to \( r_1, r_2, r_3 \) in turn to find new combination of \( r_0, r_1, r_2, r_3 \) that has non-empty \( \text{potent} \_\text{dqbits} \);
22: \( \text{data} \_\text{layout} = [] \);
23: for \( r_0, r_1, r_2, r_3 \) in \( \text{bridge} \_\text{rect} \_\text{tuple} \) do
24: \( \text{dq} = \) the qubit at the center of \( \text{potent} \_\text{dqbits} \) of \( r_0, r_1, r_2, r_3 \);
25: \( \text{data} \_\text{layout}.append(dq); \)
26: until \( \text{bridge} \_\text{rect} \_\text{tuple} \) converges;
27: \( \text{data} \_\text{layout} = [] \);
28: end

Algorithm 2: Bridge tree finder

Input: A syndrome rectangle \( R \) with data qubits \( \{a, b, c, d\} \)
Output: Candidate bridge trees
1: \( \text{star} \_\text{trees} = [] \); \( \text{// bridge trees generated by the star tree method} \)
2: \( \text{branching} \_\text{trees} = [] \); \( \text{// bridge trees generated by the star tree method} \)
3: for \( qb \) in \( R \) do
4: \( T = \) the bridge tree by connecting qubit \( qb \) to data qubits \( \{a, b, c, d\} \) with shortest paths;
5: update \( \text{star} \_\text{trees} \) s.t. it only contains trees no larger than \( T \);
6: end
7: let \( \{a', b', c', d'\} \) be a arrangement of \( \{a, b, c, d\} \) s.t.
8: \( l_{a'b'} + l_{c'd'} = \min(l_{ab} + l_{cd}, l_{ac} + l_{bd}, l_{ad} + l_{bc}); \)
9: \( l_{ab} \) is the distance of \( a \rightarrow b \);
10: connect \( a' \) and \( b', c' \) and \( d' \) with shortest paths, respectively;
11: connect the path \( a' \rightarrow b' \) and \( c' \rightarrow d' \) with shortest paths;
12: for \( qb_1 \) in \( a' \rightarrow b', qb_2 \) in \( c' \rightarrow d' \) do
13: \( T = \) the bridge tree by connecting \( qb_1 \) and \( qb_2 \) by shortest paths;
14: update \( \text{branching} \_\text{trees} \) s.t. it only contains trees no larger than \( T \);
15: end
16: Merge \( \text{star} \_\text{trees} \) and \( \text{branching} \_\text{trees} \) to find a list of minimal bridge trees;

Figure 6: Finding bridge trees in a syndrome rectangle with data qubits \( \{a, b, c, d\} \). (a)(b) shows the case where path merge is efficient, while (c) shows when path merge incurs extra overhead. (a) Green edges denote the shortest paths from qubit \( E \) to data qubits and these paths form a bridge tree with length 10. (b) Blue edges form a bridge tree with length 8. (c) An example where data qubits are close to each other.

Because one more edge in the bridge tree will result in two more CNOT gates in the measurement circuit and likely leads to a high probability of correlated errors which are hard to detect and correct. Thus, bridge trees should be as small as possible.

One natural way for finding small bridge trees is to first locate the bridge tree root and then connect the tree root to data qubits with shortest paths. We denote this method by “star tree” method. One drawback of this method is that it may miss the opportunity of path merge. For example, in the syndrome rectangle in Figure 6(a), the bridge tree induced by the shortest paths from interior qubit \( E \) to data qubits has a length 10 (green edges). In contrast, by merging paths \( E \rightarrow F \rightarrow b \) and \( E \rightarrow d \), we can get a bridge tree of length 8 (blue edges in Figure 6(b)), which reduces the number of CNOT gates by at most 4 in the resulting stabilizer measurement circuit.

To overcome the problem above, we propose the “branching tree” method, which first connects close data qubit pairs by shortest paths and then connects these shortest paths to build a complete bridge tree (pseudo code in Algorithm 2). Suppose we are constructing the bridge tree for the syndrome rectangle in Figure 6(a). We first find the shortest paths \( a \rightarrow c \) and \( b \rightarrow d \), since \( l_{ac} + l_{bd} \) (\( l_{ac} \) is the length of the shortest path from \( a \) to \( c \)) is shorter than \( l_{ab} + l_{cd} \) and \( l_{ad} + l_{bc} \). We then connect path \( a \rightarrow c \) and \( b \rightarrow d \) with the path \( E \rightarrow F \), immediately resulting in the small bridge tree (blue edges) in Figure 6(b). The following proposition bounds the length of the bridge tree generated by the branching tree method:

**Proposition 2.** Let the total edge length of the bridge tree \( T \) generated by the branching tree method be \( E(T) \), then

\[
E(T) \leq \frac{1}{2} \left( l_{ab} + l_{ac} + l_{ad} + l_{bc} + l_{bd} + l_{cd} \right).
\]

**Proof.** W.l.o.g., we assume \( l_{ab} + l_{cd} \leq \min(l_{ac} + l_{bd}, l_{ad} + l_{bc}) \). Then in \( T \), we first connect \( a \) and \( b \), and \( c \) and \( d \). On the
other hand, the distance between shortest paths $a \rightarrow b$ and $c \rightarrow d$ is smaller than $\min\{l_{ab}, l_{cd}, l_{ac} + l_{bd}, l_{ad} + l_{bc}\}$. This proposition then can be proved by combining these two inequalities.

Generally, the branching tree method is more efficient if $\min\{l_{ab} + l_{cd}, l_{ac} + l_{bd}, l_{ad} + l_{bc}\}$ is small, as shown in Figure 2(a)(b). In this case, the length of the resulted branching tree is very close to $\frac{1}{2}(l_{ad} + l_{bc})$. Instead, the length of a star tree is at least $\max\{l_{ad}, l_{bc}\} + 2$, thus leading to a larger bridge tree. On the other hand, if $\max\{l_{ab} + l_{cd}, l_{ac} + l_{bd}, l_{ad} + l_{bc}\}$ is small, the benefit of path merge may not cancel out its overhead for not using shortest paths. Figure 2(c) shows an example where the star tree has shorter length. In practice, we will run both star tree method and branching tree method and find small bridge trees by merging the result of these two methods, as shown in Algorithm 2. Once the bridge tree is determined, we can assign the syndrome qubit to the center node of the bridge tree.

Overall, Algorithm 2 can generate small bridge trees that approximate the optimal bridge tree as long as the distance between data qubits is small (by Proposition 2). Another feature of Algorithm 2 is that it may find many different bridge trees for a stabilizer since the shortest paths between nodes are not unique. This feature provides some flexibility for the stabilizer scheduling discussed in the next section.

### 4.3 Stabilizer measurement scheduler

**Algorithm 3: Iterative stabilizer scheduler**

**Input:** Binary tuples of stabilizer and syndrome rectangle: $\{(s, R)\}$.

**Output:** A schedule $P$ of binary tuples of stabilizer and bridge trees.

// Schedule initialization:
1. $S_1 = \text{tuples of X-stabilizers and syndrome rectangles};$
2. $S_2 = \text{tuples of Z-stabilizers and syndrome rectangles};$
3. if $\text{exec\_time}(S_1) < \text{exec\_time}(S_2)$ then
   swap($S_1, S_2$);
// Iterative refinement:
repeat
5. $r_2 = (s, R) \in S_2$ that has longest execution time;
6. swap_list = [r2];
7. for $i \in [0 : K]$ do
   8. $S = S_{S2+1}$;
   9. for $r \in \text{swap\_list}$ do
      10. swap_list.remove(r); S.append(r);
      11. for $r_1 \in S$ in descending order do
         12. if $r_1$ and $r$ do not have compatible bridge trees then
            13. if $\text{exec\_time}(r_1) > \text{exec\_time}(r)$ then
               14. terminate the refinement loop;
               15. swap_list.append($r_1$);
               16. S.remove($r_1$);
            end
         end
      end
   end
   17. if swap_list == {} then
      18. break;
   end
   19. if swap_list ≠ {} then
      20. recover $S_1$ and $S_2$ to the values before this iteration;
      21. break;
   end
until $S_1$ converges;

The order of stabilizer measurements affects the time required by the error detection protocol. Our goal is to reduce the time requirement for all stabilizer measurements since it will naturally reduce the decoherence error during the process of stabilizer measurements. To achieve this goal, we need to measure as many stabilizers as possible in parallel. Yet the fact that only compatible bridge trees that do not have common bridge qubits can be measured simultaneously imposes a constraint for stabilizer measurement scheduling: only stabilizers that have compatible bridge trees can be measured in the same time. A valid schedule for the order of stabilizer measurements should avoid executing two “conflicted” stabilizers together. To satisfy the constraint of stabilizer measurement scheduling yet exploit the parallelism in stabilizer measurements, we propose a heuristic scheduling approach in Algorithm 3 which consists of two steps: schedule initialization and refinement loop.

**Schedule initialization** the proposed data qubit allocation ensures that syndrome rectangles of the same type do not have bridge tree conflicts, i.e., the measurements of X (or Z) stabilizers are compatible with each other. We then initialize the stabilizer measurement schedule by two sets $S_1$ and $S_2$ which contain X- and Z-type stabilizers, respectively.

**Refinement Loop** the core idea of the refinement loop in Algorithm 3 is to move stabilizers with large bridge trees into one set. The motivation for such refinement is that the execution time for a set of stabilizers is determined by the stabilizer with the deepest measurement circuit. With the refinement loop, except one stabilizer set which contains stabilizers with large bridge trees, remaining stabilizer sets only include stabilizers with small bridge trees and can be measured in a short time.

To illustrate how the Algorithm 3 works, suppose we are given stabilizers and syndrome rectangles in Figure 7. Initially, we have $S_1 = \{(s_1, R_1), (s_4, R_4), (s_5, R_5)\}$ and $S_2 = \{(s_2, R_2), (s_3, R_3), (s_6, R_6)\}$. We then send the largest element in $S_2$, which is $(s_2, R_2)$ in this case, to the swap_list and swap it into $S_1$. Since $(s_4, R_4)$ and $(s_2, R_2)$ do not have compatible bridge trees, we will move $(s_4, R_4)$ to $S_2$. In $S_2$, $(s_6, R_6)$ is not compatible with $(s_4, R_4)$, so it will be swapped into $S_1$. After this swap, the refinement loop will stop since the swap_list is empty and every stabilizer in $S_1$ has a larger bridge tree than the stabilizer in $S_2$. The resulted stabilizer schedule is shown in Figure 7(b). Comparing to the initial schedule, the refined schedule in Figure 7(b) reduces the error detection cycle by one time step, and reduces the CNOT gate number by two.

The stabilizer measurement schedule found by the proposed heuristic should be better than the schedule where different types of stabilizers are measured in different rounds since every successful refinement iteration returns a better stabilizer measurement schedule.

### 5 Evaluation

In this section, we first evaluate the proposed synthesis framework “Surfmap” by comparing the generated surface codes with state-of-the-art manually designed QEC codes. We then demonstrate the efficiency of the proposed synthesis framework by analyzing the
error correction performance and resource overhead of the synthesized surface codes on mainstream SC architectures.

5.1 Experiment Setup

Evaluation setting We use the flag-bridge circuit \([22]\) as the backend for instantiating stabilizer measurement circuits. We select this backend because it provides the extra feature of fault-tolerant error correction. We implement all numerical simulations with stim v1.5.0, which is a fast stabilizer circuit simulator \([32]\). We use PyMatching v0.4.0 \([33]\) for error decoding with measurement signals from bridge qubits. Error rates are computed by performing $10^5$ simulations, on a Ubuntu 18.04 server with a 6-core Intel E5-2603v4 CPU and 32GB RAM.

Metrics We evaluate the error threshold of the synthesized surface codes to demonstrate their error correction performance. Error threshold indicates what hardware error rates can be tolerated and a higher error threshold is preferred. Time-step counts in an error detection cycle can also indicate the error correction performance \([15]\). The time-step counts also determines the execution speed of the surface code. A small time-step count is preferred. Finally, we evaluate the resource requirement of the synthesized surface codes with CNOT counts and qubit counts. A resource-efficient synthesis should use less CNOT gates and bridge qubits.

Device Architectures We use two categories of device architectures. The architectures are shown in Table 1. The first category architectures are built by tiling polygons and serve as basic structures for many SC devices, e.g. Google’s Sycamore \([1]\) and IBM’s latest machines \([34]\). The second category architectures consist of ‘heavy’ architectures which insert one qubit for each edge of polygon devices. Edges with one extra qubit in the middle are called “heavy edges”. Heavy architectures have lower average qubit connectivity because of the inserted two-degree qubits. Heavy architectures are used by IBM devices \([34]\). Square and heavy square architectures can be embedded into a 2D grid naturally. Hexagon and heavy hexagon architectures can be embedded into a 2D grid by squashing the hexagon into the shape of a rectangle.

Error model In all simulations, we assume the following circuit-level error model: For the gate error, we assume an error probability $p_e$ for the single-qubit depolarizing error channel on single-qubit gates, the two-qubit depolarizing error channel on two-qubit gates and the Pauli-X error channel on measurement and reset operations. For the idle decoherence error, we assume each idle qubit is followed by a single-qubit depolarizing error channel per gate duration with error probability 0.0002, which is estimated by the decoherence error formula \(1 - e^{-\frac{t}{T}} \approx 0.0002\), with the gate execution time $t = 20\,\text{ns}$ and the relaxation or dephasing time $T = 100\,\mu\text{s}$.

These errors happen on all qubits, including data qubits and bridge qubits.

5.2 Comparing to manually designed QEC code

We first compare our synthesized surface code to the two manually designed QEC codes by Chamberland et al. \([21]\) on heavy architectures. Figure 9(a)(b) shows the qubit layout and stabilizer measurement circuits of our synthesized surface codes on the heavy square architecture (‘Surfmap Heavy Square’) and the heavy hexagon architecture (‘Surfmap Heavy Hexagon’), Figure 9(c)(d) shows the manually designed QEC codes on the heavy square architecture (‘IBM Heavy Square’) and the heavy hexagon architecture (‘IBM Heavy Hexagon’). The error thresholds of these codes are in Figure 9.

Overall, compared with the manually and specifically designed codes on the two architectures, the surface codes synthesized by Surfmap can have comparable or even better performance. On the heavy hexagon architecture, the error threshold of ‘Surfmap Heavy Hexagon’ is 0.0033% which is 106% higher than that of ‘IBM Heavy Hexagon’ (0.0016%), as shown in Figure 9(a). Such benefit comes from the fact that the ‘IBM Heavy Hexagon’ code uses the Bacon-Shor scheme for Pauli Z-error correction (Figure 8(d)) which is not as effective as the surface code. On the heavy square architecture, the error threshold of ‘Surfmap Heavy Square’ is the same as that of ‘IBM Heavy Square’, as shown in Figure 9(b). This is because the code synthesized by Surfmap is almost identical to that of ‘IBM Heavy Square’ except stabilizers on boundaries, as shown in Figure 8(a)(c). In summary, Surfmap can automatically generate QEC codes that have similar or even better error correction performance compared with manually designed codes on the two studied architectures.
Figure 8: The synthesized distance-3 surface code by Surfmap and the two manually designed QEC codes by IBM [21]. IBM removes some boundary nodes (dotted) and edges (dotted) for better efficiency of stabilizer measurements on borderline.

Figure 9: The simulated error thresholds of the synthesized surface codes by Surfmap and the two manually designed QEC codes by IBM [21].

5.3 Synthesis on various SC architectures

We then apply Surfmap on the square architecture and the hexagon architecture to demonstrate that Surfmap can accommodate various architectures. The synthesized surface codes on these two architectures are shown in Figure 10. We also include another two surface code synthesis generated by using syndrome rectangles centering around four-degree qubits, as shown in Figure 11. Table 2 and Figure 12 summarizes the error correction performance of these synthesized surface codes. Table 3 shows the resource requirement of the synthesized surface codes, and is obtained by finding the smallest tiling of building blocks for each architecture that is able to support the distance-5 surface code, and then computing the ratios of different types of qubits.

The effect of architecture High-degree architectures are more effective for surface code synthesis than low-degree architectures, both in error correction performance and resource requirement. Comparing to polygon architectures, heavy architectures reduces the error threshold by 26.7% on average and they increases the average time-step number by 40.7% averagely. Heavy architectures also increase bridge qubit number by 114% averagely, up to 400%. However, low-degree devices has a much lower physical error rate and are easier to fabricate than high-degree devices.

The effect of synthesis design Synthesis centering four-degree qubits has higher resource overhead than the synthesis induced by a pair of three-degree qubits. In Table 3, 26.7% and 93.7% more qubits are required for ‘Surfmap Square-4’ and ‘Surfmap Heavy Square-4’ than ‘Surfmap Square’ and ‘Surfmap Heavy Square’, respectively. Also, on low-degree architectures, the synthesis induced by four-degree qubits may have lower error threshold. Comparing to ‘Surfmap Heavy Square’, ‘Surfmap Heavy Square-4’ downgrades the error threshold by 20.8%.

In summary, not only the architecture design but also the synthesis design have a critical impact on the resource overhead and error correction performance of the synthesized code. By optimizing...
Table 2: Error correction metrics of the synthesized surface codes. The average numbers of bridge qubits, CNOT gates, and time steps are computed over all X-type stabilizers.

| Code               | Avg. bridge qubit # | Avg. CNOT # | Avg. time-step # | Tot. time-step # | Estimated error threshold |
|--------------------|---------------------|-------------|------------------|------------------|--------------------------|
| Surfmap Heavy Square | 3                   | 8           | 12               | 24               | 0.53%                    |
| Surfmap Heavy Hexagon | 7                   | 19          | 20               | 40               | 0.33%                    |
| Surfmap Square      | 2                   | 6           | 10               | 20               | 0.63%                    |
| Surfmap Hexagon     | 4                   | 10          | 13               | 26               | 0.47%                    |
| Surfmap Square-4    | 1                   | 4           | 8                | 8                | 0.70%                    |
| Surfmap Heavy Square-4 | 5                  | 12          | 13               | 13               | 0.42%                    |

Table 3: Qubit utilization of the distance-5 surface codes synthesized by Surfmap on different architectures.

| Code               | data qubit % | bridge qubit % | unused qubit % | Tot. qubit # |
|--------------------|--------------|----------------|----------------|--------------|
| Surfmap Heavy Square | 31.7%        | 45.6%          | 22.8%          | 79           |
| Surfmap Heavy Hexagon | 18.8%        | 59.4%          | 21.8%          | 133          |
| Surfmap Square     | 55.6%        | 44.4%          | 0.0%           | 45           |
| Surfmap Hexagon    | 30.5%        | 48.8%          | 20.7%          | 82           |
| Surfmap Square-4   | 43.9%        | 56.1%          | 0.0%           | 57           |
| Surfmap Heavy Square-4 | 16.3%      | 83.7%          | 0.0%           | 153          |

Figure 13: An example for potential architecture design.

5.4 Architecture Design Implications

Our synthesis results provide some insights for designing future SC quantum architectures that can efficiently execute the surface code. Starting from the ideal 2D qubit array equipped with the surface code in Figure 13(a), we discuss how to reduce the connectivity of the ideal 2D qubit array while preserving the efficiency for surface code synthesis.

Insert two-degree nodes selectively Heavy edges or extra two-degree nodes are harmful to the synthesized surface code. Yet, they can be essential when lowering the device design and fabrication complexity [35]. As a compromise, we can insert two-degree nodes selectively.

First, we should avoid inserting two-degree nodes both in X-type syndrome rectangles and Z-type syndrome rectangles. This is because we can confine the detrimental effect of two-degree nodes only within one stabilizer set in this way. Figure 13(b) gives an example where two-degree nodes are inserted into both X- and Z-type syndrome rectangles. Comparing to the architecture in Figure 13(c) which only inserts nodes in Z-type syndrome rectangles, the architecture in Figure 13(b) will have two more time-steps in each error detection cycle. Second, it may be of merit to insert two-degree nodes in small syndrome rectangles of a scheduled stabilizer set. A stabilizer set may have syndrome rectangles of different sizes. Inserting two-degree nodes in small syndrome rectangles may not increase the error detection cycle time. For example, the error detection cycle length of the architecture in Figure 13(d) is the same as the one in Figure 13(c).

Remove useless structures The unused qubits and physical connections for hexagon and heavy architectures are not a few, as indicated by Table 3. There are several types of useless structures in these architectures, including the architecture in Figure 13(d). First, connections between data qubits do not provide any benefits for constructing non-conflicted bridge trees. We can remove such connections to lower device complexity, as shown in Figure 13(e). Second, qubits and connections on the boundaries of these architectures may not be used by any stabilizers and can thus be removed. For example, the qubits on the top right and bottom left corners of Figure 13(e) can be removed and the resulted architecture is shown in Figure 13(f).
6 Related Work

Circuit compilation on surface code are at the higher logical circuit level. Javadi et al. [18] and Hua et al. [19] studied the routing congestion in circuit compilation over the surface code. Ding et al. [16] and Paler et al. [17] studied the compilation of magic state distillation circuits with existing surface code logical operations. These works usually assume that the ideal surface code array is already available and do not consider the problem of surface code synthesis on hardware. In contrast, this paper focuses on optimizing the lower-level surface code synthesis on various SC architectures.

QEC code and architecture: most efforts on QEC code synthesis are still on looking for an architecture that is suitable for the target code. Reichardt [36] proposes three possible planar qubit layouts for synthesizing the seven-qubit color code. Chamberland et al. [21] proposes a trivalent architecture where it is straightforward to allocate data qubits of triangular color codes. Chamberland et al. [21] introduces heavy architectures which reduces frequency collision while still provides support for surface code synthesis. Instead, the synthesis framework in this paper can automatically synthesize the surface code onto various mainstream architectures and avoid manually redesigning code protocols for the ever-changing architectures. Another line of research targets at compiling stabilizer measurement circuits to existing architectures. Lao and Almudever [22] proposes the flag-bridge circuit which can measure the stabilizer of the Steane code on the IBM-20 device. However, their work relies on manually appointed data qubits and bridge qubits, and focuses on the IBM-20 device. Methods in this category are orthogonal to our work, and can be easily merged into our framework.

7 Discussion

Though we propose a comprehensive framework to synthesize surface code on various SC devices, there is still much space left for potential improvements. For example, besides heuristic data qubit allocation schemes, it is also promising to train a neural network to allocate data qubits of triangular color codes. Another line of research targets at compiling stabilizer measurement circuits to existing architectures. Lao and Almudever [22] proposes the flag-bridge circuit which can measure the stabilizer of the Steane code on the IBM-20 device. However, their work relies on manually appointed data qubits and bridge qubits, and focuses on the IBM-20 device. Methods in this category are orthogonal to our work, and can be easily merged into our framework.

Another interesting future direction is to adapt our synthesis framework to other error correction codes. Though surface code can be implemented on various SC devices, it may not be the most efficient one. Extending our framework to other error correction codes can help us fully exploiting existing device architectures for FT computation. On the other hand, the proposed surface code synthesis framework can provide guidance for SC architecture design. Using our framework as the baseline, we can compare the efficiency of different device architectures for implementing surface code and identify the most efficient one.

8 Conclusion

In this paper, we formally describe the three challenges of synthesizing surface code on SC devices and present a comprehensive synthesis framework to overcome these challenges. The proposed framework consists of three optimizations. First, we adopt a geometrical method to allocate data qubits in a way that ensures the existence of shallow measurement circuits. Second, we only consider bridge qubits enclosed by data qubits and reduce the number of bridge qubits by merging short paths between data qubits. The proposed bridge qubit optimization reduces the resource conflicts between syndrome measurement. Third, we propose an iterative heuristic to schedule the execution of measurement circuits based on the proposed data qubit allocation. Our comparative evaluation to manually designed QEC codes demonstrates that, with good optimization, automated synthesis can surpass manual QEC code design by experienced theorists.

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