On the Application of Error Backpropagation to the Background Calibration of Time Interleaved ADC for Digital Communication Receivers

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Abstract—This paper introduces a backpropagation-based technique for the calibration of the mismatch errors of time-interleaved analog to digital converters (TI-ADCs). This technique is applicable to digital receivers such as those used in coherent optical communications. The error at the slicer of the receiver is processed using a modified version of the well known backpropagation algorithm from machine learning. The processed slicer error can be directly applied to compensate the TI-ADC mismatch errors with an adaptive equalizer, or it can be used to digitally estimate and correct said mismatch errors using analog techniques such as delay cells and programmable gain amplifiers (PGA). The main advantages of the technique proposed here compared to prior art are its robustness, its speed of convergence, and the fact that it always works in background mode, independently of the oversampling factor and the properties of the input signal, as long as the receiver converges. Moreover, this technique enables the joint compensation of impairments not addressed by traditional TI-ADC calibration techniques, such as I/Q skew in quadrature modulation receivers. Simulations are presented to demonstrate the effectiveness of the technique, and low complexity implementation options are discussed.

Index Terms—TI-ADC mismatch calibration, Error Backpropagation, Background Calibration, MIMO equalization.

I. INTRODUCTION

HIGH speed digital receivers such as those used in coherent optical communications [1]–[9] require high bandwidth, high sampling rate analog to digital converters (ADC). Current coherent receivers operate at symbol rates around 96 Giga-baud (GBd) and require ADC bandwidths of about 50 GHz and sampling rates close to 150 GHz. In the near future symbol rates will increase to 128–150 GBd or higher, required bandwidths will be in the range of 65–75 GHz, and sampling rates in the 200–250 GHz range. The technique universally applied so far to achieve these high bandwidths and sampling rates in coherent transceivers is the time interleaved ADC (TI-ADC) [10], [11]. Frequency interleaved ADCs (FI-ADC) may become a promising alternative in the near future [12].

The performance of TI-ADCs is affected by mismatches among the interleaves, particularly the mismatches of sampling time, gain, and DC offset [13], [14]. There has been a large body of literature dedicated to various techniques to calibrate these mismatches [15]–[30]. For a thorough review and discussion of previous TI-ADC calibration techniques, please see [31], [32] and references therein. In general, existing techniques suffer from one or more of the following drawbacks: i) Dependence on the properties of the input signal or the oversampling factor for proper operation [19]–[23], [33]; ii) Requiring an extra ADC to provide a reference [16], [18]; iii) Introducing intentional degradations (e.g., dither) in the ADC output in order to find the calibration parameters [24], [25], and iv) Slow convergence [15], [17]. In this paper we propose a new background technique that overcomes the above limitations, and is applicable to receivers for digital communications such as those used for coherent optical transmission [1]. The basic idea consists in the use of a low complexity adaptive equalizer, called Compensation Equalizer (CE), to compensate the mismatches of the TI-ADC. The CE is adapted using the stochastic gradient descent (SGD) algorithm and a post processed version of the error available at the slicer of the receiver, where the post processing is done using the backpropagation algorithm [34], [35].

Next we discuss some of the state-of-the-art TI-ADC calibration techniques and compare them to the one proposed in this paper. The approaches developed in [16], [19], [21]–[23] use the autocorrelation of the quantized signal to estimate the timing mismatches and adjust them in the analog or digital domain. One serious limitation of this technique is related to the properties of the input signal [19], [21], which cause the calibration algorithm to diverge for some particular input frequencies (given by \( f_{\text{in}} = m \frac{f_s}{M} \)), with \( m \in \{0, \cdots, M-1\} \) where \( f_s \) is the sampling rate and \( M \) is the number of interleaves of the TI-ADC. This makes this technique not suitable for receivers with a particular oversampling ratio (OSR).

Other techniques perform the calibration based on statistical properties of the quantized signal [20], [26], [27], [33]. Histograms of sub-ADC outputs are created and calculations such as the variance or cumulative distribution function are made to estimate the error introduced by the timing mismatch. The effectiveness of these approaches depends on the input signal characteristics and therefore their robustness is problematic. In other examples, [20], [26] an auxiliary channel (working at the overall sampling rate of the TI-ADC) is required to provide a reference or to enable the estimation, respectively.
Dither injection techniques are based on the addition of a signal in either the analog or digital domain to facilitate the estimation of the calibration parameters [25], [28], [29], [36]. They are often used in high resolution ADCs (> 10 effective number of bits or ENOB). Depending on the level of the dither signal, this technique can limit the swing of the input signal. One of the most common limitations of existing techniques is their inability to adjust calibration parameters of different nature simultaneously. A technique where calibration of a given impairment does not depend on calibration of the other impairments is highly desirable. For example, the stability of the calibration of the timing mismatch should not rely on how free from offset, gain or bandwidth mismatches the sampled signal is.

This work presents a new technique based on adaptive equalization [37] that runs inherently in background and is able to overcome the aforementioned limitations. The proposed technique is intended to be applied in high-speed receivers for digital communication systems such as those used in coherent optical transmission [1].

Adaptive equalization has been shown [30], [38] to be a powerful technique to compensate errors in TI-ADCs. However, its application to some types of receivers for digital communications, particularly coherent optical transceivers, has been limited by the lack of availability of a suitable error signal to use in the SGD algorithm. In [30], [38] the equalizer used to compensate TI-ADC impairments is the main receiver equalizer, or Feedforward Equalizer (FFE). This is possible in the referenced works because the FFE is immediately located after the TI-ADC, without any other blocks in between. Therefore the FFE can access and compensate directly the impairments of the different interleaves. Also, the slicer error carries information about the impairments of the individual interleaves and therefore the FFE adaptation algorithm can drive its coefficients to a solution that jointly compensates the channel and the TI-ADC impairments. In the case of coherent optical receivers there is at least one block, the Bulk Chromatic Dispersion Equalizer (BCD) between the TI-ADC and the FFE. The BCD causes signal components associated with different interleaves of the TI-ADC to be mixed in a way that makes the use of the FFE unsuitable to compensate them. Therefore a separate equalizer, immediately located after the TI-ADC, is necessary. This is the previously mentioned CE. Although in this way the CE has direct access to the impairments of the different TI-ADC interleaves, the slicer error is not directly applicable to adapt it, because error components associated with different TI-ADC have also been mixed by the BCD (and possibly other signal processing blocks, depending on the architecture of the receiver). This paper solves that problem through the use of the backpropagation algorithm [34], an algorithm widely used in machine learning [35]. Its main characteristic is that, in a multi-stage processing chain where several cascaded blocks have adaptive parameters, it is able to determine the error generated by each one of these sets of parameters for all the stages. Backpropagation is used in combination with the SGD algorithm to adjust the parameters of the CE in order to minimize the Mean Squared Error (MSE) at the slicer of the receiver. The use of the CE in combination with the backpropagation algorithm results in robust, fast converging background compensation or calibration. As mentioned before, the compensation is not limited to the impairments of individual TI-ADCs (which is the case for traditional calibration techniques), but it extends itself to the entire receiver analog front end, enabling the compensation of impairments such as time skew between the in-phase and the quadrature components of the signal in a receiver based on Quadrature Amplitude Modulation (QAM) or Phase Modulation (PM).

In the architecture just described, the compensation is achieved by an all-digital technique. A variant of the technique based on a mixed-signal calibration is also proposed in this paper. In this variant, the backpropagation and the SGD algorithms are used to estimate the TI-ADC mismatch errors, but the equalizer per se is not built.

Because ultrafast adaptation is usually not necessary, the backpropagation algorithm can be implemented in a highly subsampled hardware block which does not require parallel processing. Therefore the implementation complexity of the proposed technique is low, as discussed in detail in Section V.

The rest of this paper is organized as follows. Section II presents a discrete time model of the TI-ADC system in a dual polarization optical coherent receiver. The error backpropagation based adaptive compensation equalizer is introduced in Section III. Simulation results are presented and discussed in Section IV. The hardware complexity of the proposed compensation scheme is discussed in Section V, and conclusions are drawn in Section VI.

II. System Model

Although the new compensation algorithm proposed in this work can be applied to any high-speed digital communication receiver, to make the discussion more concrete we focus the study on dual-polarization (DP) optical coherent transceivers [1]–[5]. A block diagram of an optical front-end (OFE) for a DP coherent receiver is shown in Fig. 1. The optical input signal is decomposed by the OFE to obtain four components, the in-phase and quadrature (I/Q) components of the two polarizations (H/V). The photodetectors convert the optical signals to photocurrents which are amplified by trans-impedance amplifiers (TIAs). The analog front-end (AFE) is in charge of the acquisition and conversion of the electrical signal to the digital domain. Typically, oversampled digital receivers
are used to compensate the dispersion experienced in optical links (e.g., $T_s = \frac{T}{2}$ where $T_s$ and $T$ are the sampling and symbol periods, respectively) [4]. Next we develop the model of the optical channel used in the remainder of this paper.

Let $a_k^{(P)} = a_k^{(P),I} + j a_k^{(P),Q}$ be the $k$-th quadrature amplitude modulation (QAM) symbol in polarization $P \in \{H, V\}$. An optical fiber link with chromatic dispersion (CD) and polarization-mode dispersion (PMD) can be modeled as a $2 \times 2$ multiple-input and multiple output (MIMO) complex-valued channel [4] encompassing four complex filters with impulse responses $h_{m,n}(t)$ where $m, n = 1, 2$. Then, the received noise-free electrical signals provided by the optical demodulator can be expressed as [4]

$$s^{(H)}(t) = s^{(H,I)}(t) + j s^{(H,Q)}(t)$$

$$= e^{j \omega_0 t} \left[ \sum_k a_k^{(H)} h_{1,1}(t - kT) + a_k^{(V)} h_{1,2}(t - kT) \right],$$

where $1/T$ is the symbol rate and $\omega_0$ is the optical carrier frequency offset.

### A. Discrete-Time Model of the AFE and the TI-ADC

In this section we introduce a discrete-time model for the AFE and TI-ADC system of Fig. 1 including its impairments. A simplified model of the analog path for one component $C \in \{I, Q\}$ in a given polarization $P \in \{H, V\}$ is shown in Fig. 2. Each lane of the AFE includes a filter with impulse response $c_{m,n}^{(P,C)}(t)$ that models the response of the electrical interconnections between the optical demodulator and the TIA, the TIA itself, and any other components in the signal path up to an $M$-parallel TI-ADC system. Mismatches between $c_{m,n}^{(P,I)}(t)$ and $c_{m,n}^{(P,Q)}(t)$ may cause time delay or skew between components $I$ and $Q$ of a given polarization $P$, which degrade the receiver performance. As we shall show here, the proposed background calibration algorithm is able to compensate not only the imperfections of the TI-ADC, but also the I/Q skew and any other mismatches among the signal paths.

The independent frequency responses of the $M$ track and hold units in an $M$-channel TI-ADC system are modeled by blocks $f_{m}^{(P)}(t)$ with $m = 0, \ldots, M - 1$. Each $M$-way interleaved TI-ADC path is sampled every $1/T_s$ seconds with a proper sampling phase. Parameters $\delta_{m}^{(P,C)}$ and $\alpha_{m}^{(P,C)}$ model the sampling time errors and the DC offsets, respectively. Path gains are modeled by

$$\gamma_{m}^{(P,C)} = 1 + \Delta_{\gamma_{m}^{(P,C)}},$$

where $\Delta_{\gamma_{m}^{(P,C)}}$ is the gain error.

Following [30], [38], the sampling phase error $\delta_{m}^{(P,C)}$ and the path gain $\gamma_{m}^{(P,C)}$ are modeled by an analog interpolation filter with impulse response $p_{m}^{(P,C)}(t)$ followed by ideal sampling as depicted in Fig. 3. Assuming that the bit-resolution of the ADC’s is sufficiently high, the quantizer can be modeled as additive white noise with uniform distribution. Also, at high-frequency (i.e., $1/T_s$), the offsets $\alpha_{m}^{(P,C)}$ generate an $M$-periodic signal denoted as $\tilde{o}_{m}^{(P,C)}[n]$ such that $\tilde{o}_{m}^{(P,C)}[n] = \tilde{o}_{m}^{(P,C)}[n + M]$ with

$$\tilde{o}_{m}^{(P,C)}[n] = \alpha_{m}^{(P,C)} - \delta_{m}^{(P,C)}, \quad m = 0, \ldots, M - 1. \quad (4)$$

Then, the digitized high-frequency samples can be expressed as

$$y_{m}^{(P,C)}[n] = r_{m}^{(P,C)}[n] + \tilde{o}_{m}^{(P,C)}[n] + q_{m}^{(P,C)}[n], \quad (5)$$

where $r_{m}^{(P,C)}[n]$ is the signal component provided by the $M$-channel TI-ADC, and $q_{m}^{(P,C)}[n]$ is the quantization noise (see Fig. 3).

We define the total impulse response of a given subchannel as

$$h_{m}^{(P,C)}(t) = c_{m}^{(P,C)}(t) \otimes f_{m}^{(P,C)}(t) \otimes p_{m}^{(P,C)}(t), \quad (6)$$

where $m = 0, \ldots, M - 1$ and $\otimes$ denotes the convolution operation. Let $H_{m}^{(P,C)}(j\omega)$ and $S_{m}^{(P,C)}(j\omega)$ be the Fourier transforms (FTs) of $h_{m}^{(P,C)}(t)$ and $s_{m}^{(P,C)}(t)$, respectively.

In digital communication systems with spectral shaping $|S_{m}^{(P,C)}(j\omega)| \approx 0$ for $|\omega| \geq \pi/T_s$. Further assuming that $|H_{m}^{(P,C)}(j\omega)| \approx 0$ for $|\omega| \geq \pi/T_s$, the analog filtering of Fig. 3 can be represented by a real discrete-time model as depicted in Fig. 4 by using

$$h_{m}^{(P,C)}[n] = T_s h_{m}^{(P,C)}(nT_s), \quad m = 0, \ldots, M - 1. \quad (7)$$

Therefore it can be shown that the digitized high-frequency signal can be expressed as

$$y_{m}^{(P,C)}[n] = \sum_{l} \tilde{i}_{m}^{(P)}[l] s^{(P,C)}[n - l], \quad (8)$$

where $s^{(P,C)}[n]$ is the received signal.
where \( s^{(P,C)}[n] = s^{(P,C)}(nT_s) \) and \( \hat{h}_n^{(P,C)}[l] \) is the impulse response of a time-varying filter, which is an \( M \)-periodic sequence such \( \hat{h}_n^{(P,C)}[l] = \hat{h}_{n+M}[l], \) and defined by

\[
\hat{h}_n^{(P,C)}[l] = h_n^{(P,C)}[l], \quad n = 0, \ldots, M - 1, \forall l,
\]

(9)

with \( h_n^{(P,C)}[l] \) given by (7). We highlight that (8) includes the impact of both the AFE mismatches and the \( M \)-channel TI-ADC impairments. Replacing (8) in (5), the digitized high-frequency sequences result

\[
y^{(P,C)}[n] = \sum_l \hat{h}_n^{(P,C)}[l] s^{(P,C)}[n-l] + \hat{o}^{(P,C)}[n] + q^{(P,C)}[n].
\]

(10)

B. Compensation of AFE Mismatch and TI-ADC Impairments

Similar to what was done in previous works [30], [38], [39], we propose to use an adaptive digital compensation filter applied after the mitigation of the offset sequence, i.e.,

\[
x^{(P,C)}[n] = \sum_{l=0}^{L_q-1} \hat{g}_n^{(P,C)}[l] w^{(P,C)}[n-l],
\]

(11)

where \( \hat{g}_n^{(P,C)}[l] \) is the \( M \)-periodic time-varying impulse response of the compensation filter (i.e., \( \hat{g}_n^{(P,C)}[l] = \hat{g}_{n+M}[l] \)), \( L_q \) is the number of taps of the compensation filters, and \( w^{(P,C)}[n] \) is the offset compensated signal given by

\[
w^{(P,C)}[n] = y^{(P,C)}[n] - \hat{o}^{(P,C)}[n],
\]

(12)

with \( \hat{o}^{(P,C)}[n] \) being the estimated \( M \)-periodic offset sequence. The combination of the offset compensation blocks and the compensation filters \( \hat{g}_n^{(P,C)}[l] \) constitutes the Compensation Equalizer (Fig. 5).

A proper strategy to estimate the response of the CE is required. Notice that adaptive calibration techniques based on a reference ADC such as in [39] cannot be used to compensate mismatches between the I and Q signal paths. In the following we propose the backpropagation technique to adapt the CE.

III. ERROR BACKPROPAGATION BASED COMPENSATION OF AFE AND TI-ADC IMPAIRMENTS IN DP OPTICAL COHERENT RECEIVERS

Based on the previous analysis, Fig. 5 depicts a block diagram of the AFE+TI-ADC in a dual-polarization optical coherent receiver with the adaptive calibration block, which includes four instances of the real filter as defined by (11). For simplicity, we modified the notation of the system model of Fig. 4. Note that we use an integer index between 1 and 4 to represent a certain component in a given polarization: “(1)” = (H, I), “(2)” = (H, Q), “(3)” = (V, I), and “(4)” = (V, Q).

The main receiver functions are included in the digital signal processing (DSP) block of Fig. 5, which works with samples every \( T_s \) seconds. In summary, some of the most important DSP algorithms used in these receivers are the chromatic dispersion equalizer (or BCD), the MIMO FFE to compensate the polarization-mode dispersion, Timing Recovery (TR) from the received symbols, the Fine Carrier Recovery (FCR) to compensate the carrier phase and frequency offset, and the Forward Error Correction (FEC) decoder. Readers interested in more details on optical coherent receivers can see [1]–[3] and references therein.

A. All Digital Compensation Architecture

Let \( g^{(i)}[l] \) with \( i = 1, \ldots, 4 \) be the filter impulse response \( \hat{g}^{(i)}[l] \) in one period defined as

\[
g^{(i)}[l] = \hat{g}^{(i)}[l], \quad m = 0, \ldots, M - 1,
\]

(13)

where \( l = 0, \ldots, L_q - 1 \) and \( n_0 \) is an arbitrary time index multiple of \( M \). The filter taps of the CE \( \hat{g}^{(i)}[l] \) are adapted by using the slicer error at the output of the receiver DSP block. Let \( e_k^{(j)} \) be the slicer error defined by

\[
e_k^{(j)} = u_k^{(j)} - a_k^{(j)}, \quad j = 1, \ldots, 4,
\]

(14)

where \( u_k^{(j)} \) is the input of the slicer and \( a_k^{(j)} \) is the \( k \)-th detected symbol at the slicer output (see Fig. 5). Notice that the sampling rate of the slicer inputs \( u_k^{(j)} \) is \( 1/T \), therefore

\[
\sum_{l=0}^{L_q-1} \hat{g}^{(i)}[l] s^{(P,C)}[n-l] + \hat{o}^{(P,C)}[n] + q^{(P,C)}[n].
\]
a subsampling of $T_s/T$ is carried out after the receiver DSP block. Then, we define the total squared error at the slicer as

$$E_k = \sum_{j=1}^{4} |e_k^{(j)}|^2.$$  \hspace{1cm} (15)

Let $E\{\mathcal{E}_k\}$ be the MSE at the slicer with $E\{\cdot\}$ denoting the expectation operator. In this work we use the least mean squares (LMS) algorithm to iteratively adapt the real coefficients of the CE given by (13), in order to minimize the MSE at the slicer:

$$g^{(i)}_{m,p+1} = g^{(i)}_{m,p} - \beta \nabla_{g^{(i)}_{m,p}} E\{\mathcal{E}_k\},$$  \hspace{1cm} (16)

where $i = 1, \ldots, 4; \ m = 0, \ldots, M-1; \ p$ denotes the number of iteration, $g^{(i)}_{m,p}$ is the $L_g$-dimensional coefficient vector at the $p$-th iteration given by

$$g^{(i)}_{m,p} = \left[g^{(i)}_{m,p}[0], g^{(i)}_{m,p}[1], \ldots, g^{(i)}_{m,p}[L_g-1]\right]^T.$$  \hspace{1cm} (17)

$\beta$ is the adaptation step, and $\nabla_{g^{(i)}_{m,p}} E\{\mathcal{E}_k\}$ is the gradient of the MSE with respect to the filter vector $g^{(i)}_{m,p}$.

We emphasize that the computation of the MSE gradient is not trivial since $\mathcal{E}_k$ is not the error at the output of the CE block. To get the proper error samples to adapt the coefficients of the filters as expressed in (16), we propose the backpropagation algorithm widely used in machine learning [34], [35]. Towards this end, the slicer errors are backpropagated as described in [40]. Finally, based on these backpropagated errors we can estimate the gradient $\nabla_{g^{(i)}_{m,p}} E\{\mathcal{E}_k\}$ as usual in the classical LMS algorithm.

**B. Error Backpropagation (EBP)**

Without loss of generality, we assume that the receiver DSP block can be modeled as a real time-varying $4 \times 4$ MIMO $T/2$ fractional spaced equalizer (i.e., $T_s = T/2$), which is able to compensate CD and PDM among other optical fiber channel effects. Then, the downsampled output of the $T/2$ receiver DSP block can be written as (see Fig 6)

$$u_k^{(j)} = \sum_{i=1}^{L} \sum_{l=0}^{L_t-1} \Gamma^{(j,i)}_{n+l}[l] x^{(i)}[2k-l], \ j = 1, \ldots, 4, \hspace{1cm} (18)$$

where $\Gamma^{(j,i)}_{n+l}[l]$ is the time-varying impulse response of the filter with input $i$ and output $j$, $L_t$ is the number of taps of the filter, while $x^{(i)}[l]$ is the signal at the DSP block input $i$ given by (11), i.e.,

$$x^{(i)}[n] = \sum_{l'=0}^{L_t-1} g^{(i)}_{m,n+l'}[l'] w^{(i)}[n-l'], \ i = 1, \ldots, 4,$$  \hspace{1cm} (19)

where $g^{(i)}_{m}$ is the impulse response defined by (13), $\lfloor \cdot \rfloor_M$ denotes the modulo $M$ operation, and $w^{(i)}[n]$ is the DC compensated signal (12).

As usual with the SGD based adaptation, we replace the gradient of the MSE, $\nabla_{g^{(i)}_{m,p}} E\{\mathcal{E}_k\}$, by a noisy estimate, $\nabla_{g^{(i)}_{m,p}} \mathcal{E}_k$. In the Appendix we show that an instantaneous gradient of the squared error (15) can be expressed as

$$\nabla_{g^{(i)}_{m,p}} \mathcal{E}_k = \alpha e^{(i)}[m + k M] w^{(i)}[m + k M],$$  \hspace{1cm} (20)

where $\alpha$ is a certain constant, $w[n]$ is the $L_g$-dimensional vector with the samples at the CE input, i.e.,

$$w^{(i)}[n] = \left[w^{(i)}[n], w^{(i)}[n-1], \ldots, w^{(i)}[n-L_g+1]\right]^T,$$  \hspace{1cm} (21)

while $\hat{e}^{(i)}[n]$ is the backpropagated error given by

$$\hat{e}^{(i)}[n] = \sum_{j=1}^{4} \sum_{l=0}^{L_t-1} \Gamma^{(j,i)}_{n+l}[l] e^{(j)}[n+l],$$  \hspace{1cm} (22)

with $e^{(j)}[n]$ being the oversampled slicer error obtained from the baud-rate slicer error $e^{(j)}_k$ in (14) as

$$e^{(j)}[n] = \begin{cases} \hat{e}^{(j)}_{n/2} & \text{if } n = 0, \pm 2, \pm 4, \ldots \vspace{0.4cm} \\ 0 & \text{otherwise} \end{cases} \hspace{1cm} (23)$$

Then, a full digital compensation architecture can be derived by using an adaptive CE with

$$g^{(i)}_{m,p+1} = g^{(i)}_{m,p} - \mu \nabla_{g^{(i)}_{m,p}} \mathcal{E}_k,$$  \hspace{1cm} (24)

where $\mu = \alpha \beta$ is the step-size. Furthermore, based on the backpropagated error (22) it is possible to estimate the DC offsets in the input samples as follows

$$\hat{o}^{(p+1)}_{m}[n] = \hat{o}^{(p)}_{m}[n] - \mu_o \hat{e}^{(p)}[n + m], \ m = 0, \ldots, M-1,$$  \hspace{1cm} (25)

where $\hat{o}^{(p)}_{m}[n]$ is the estimate at the $p$-th iteration of the DC offset sequence in one period (see (12)), and $\mu_o$ is the step-size of the DC offset estimator.

Competition between the CE and any adaptive DSP blocks in $\Gamma^{(j,i)}_{n+l}[l]$ (e.g., the FFE) may generate instability, therefore an adaptation constraint must be included. For example, one of the $4M$ sets of the filter coefficients can be limited to only be a time delay line, for example, $g^{(0)}_0[l] = \delta_{l,l_d}$ where $l = 0, \ldots, L_g - 1$ and $l_d = \frac{L_g}{2} - 1$ ($L_g$ is assumed odd).
Since channel impairments change slowly over time, the coefficient updates given by (24) and (25) do not need to operate at full rate, and subsampling can be applied. The latter allows implementation complexity to be significantly reduced. Additional complexity reduction is enabled by: 1) strobing the algorithms once they have converged, and/or 2) implementing them in firmware in an embedded processor, typically available in coherent optical transceivers. Practical aspects of the hardware implementation shall be discussed in Section V.

C. Mixed-Signal Compensation Architecture

A mixed-signal based calibration technique can be also derived from the error backpropagation (EBP) algorithm described in the previous section. Toward this end, sampling phase, gain, and offsets are adjusted before the ADC\(^2\) by using the gradient of the backpropagated slicer error as depicted in Fig. 7. Similarly to the full digital solution, the DC offsets in the mixed-signal calibration approach are compensated by using (25). The gain is iteratively adjusted by using

\[
\hat{r}_{m,p+1}^{(i)} = \hat{r}_{m,p}^{(i)} - \mu \hat{e}^{(i)} [m + kM] w^{(i)} [m + kM], \quad \forall k, (26)
\]

where \(m = 0, \ldots, M - 1\) and \(i = 1, 2, 3, 4\). Finally, since the backpropagated slicer error is available at the ADC outputs, the sampling phase can be iteratively adjusted by using the MMSE timing recovery algorithm [41], i.e.,

\[
\hat{r}_{m,p+1}^{(i)} = \hat{r}_{m,p}^{(i)} - \mu \hat{e}^{(i)} [m + kM] \times \\
\left( w^{(i)} [m + kM + 1] - w^{(i)} [m + kM - 1] \right), \quad \forall k
\]

with \(m = 0, \ldots, M - 1\). The calibration algorithm adjusts analog elements already present in most implementations of the TI-ADC [17], [42], [43]. The clock sampling phase is adjusted with variable delay lines, gain and offset can be corrected in the comparator or with programmable gain amplifiers (PGA), if needed.

IV. Simulation Results

The performance of the proposed backpropagation based adaptive CE is investigated by running Montecarlo simulations of the setup shown in Fig. 8 and defined in Table I. Each test consists of 500 cases where the impairment parameters are obtained by using uniformly distributed random variables (UDRV). The electrical analog path responses (6) are simulated with first-order lowpass filters with 3dB-bandwidth defined by

\[
B_{(m)}^{(i)} = B_0 + \Delta B_{(m)}^{(i)}; \quad i = 1, 2, 3, 4; \quad m = 0, \ldots, M - 1,
\]

where \(B_0\) is the nominal BW and \(\Delta B_{(m)}^{(i)}\) is the BW mismatch. Let \(\tau_{m}^{(i)}\) be the mean group delay of the filter of the \(m\)-th channel and \(i\)-th component. The impact of the I/Q time skew of polarizations \(H\) and \(V\) defined as

\[
\tau_H = \tau^{(1)} - \tau^{(2)}, \quad \tau_V = \tau^{(3)} - \tau^{(4)}
\]

with \(\tau^{(i)} = \frac{1}{M} \sum_{m=0}^{M-1} \tau_{m}^{(i)}\), is also investigated. We consider a 16-QAM modulation scheme with a symbol rate of \(1/T = 96 \text{ Gb/d}\). Raised cosine filters with rolloff factor 0.10 for transmit pulse shaping are simulated (i.e., the nominal BW of the channel filters is \(B_0 = 1.1 \times \frac{96}{T \times 4} \approx 53 \text{ GHz}\)). The optical signal-to-noise ratio (OSNR) is set to that required to achieve a bit-error-rate (BER) of \(\sim 1.2 \times 10^{-3}\) (see [44], [45] for the definition of OSNR). The oversampling factor in the DSP blocks is \(T/T_s = 4/3\). The fiber length is 100 km with 10 ps of differential group delay (DGD) and 1000 ps\(^2\) of second-order PMD (SOPMD). Rotations of the

| Parameter                     | Value |
|-------------------------------|-------|
| Modulation                    | 16-QAM|
| Symbol Rate \((f_0 = 1/T)\)   | 96 Gb/d|
| Receiver Oversampling Factor \((T/T_s)\) | 4/3   |
| Fiber Length                  | 100 km|
| Differential Group Delay (DGD)| 10 ps |
| Second Order Pol. Mode Disp. (SOPMD)| 1000 ps\(^2\) |
| Speed of Rotation of the Pol. at the Tx| 2 kHz |
| Speed of Rotation of the Pol. at the Rx| 20 kHz |
| TI-ADC Resolution            | 8 bit |
| TI-ADC Sampling Rate (all interleaves) | 128 GS/s |
| Number of Interleaves of TI-ADC (\(M\)) | 16 |
| Number of Taps of CE (\(L\)) | 7 |
| Rolloff Factor                | 0.10  |
| Nominal BW of Analog Paths (\(B_0\) (see (28))) | 53 GHz |
| Gain Errors (see (3)) - UDRV | \(\Delta (m) \in [\pm 0.15]\) |
| Sampling Phase Errors - UDRV | \(\Delta (m) \in [\pm 0.10]/T\) |
| Bandwidth Mismatches (see (28)) - UDRV | \(\Delta (m) \in [\pm 0.075]/B_0\) |
| I/Q Time Skew (see (29)) - UDRV | \(\tau_H, \tau_V \in [\pm 0.10]/T\) |
| DC Offsets - UDRV            | \(\delta m \in [\pm 0.025]/VFS\) |

Figure 7. Block diagram of the mixed-signal calibration variant. The calibration with analog elements enables power consumption reduction. The EBP is the same as the all-digital variant.

Figure 8. Block diagram of the system model used in the simulations.
state of polarization (SOP) of 2 kHz and 20 kHz are included at the transmitter and receiver, respectively. TI-ADCs with 8-bit resolution, 128 GS/s sampling rate, and $M = 16$ are simulated. The number of taps of the digital compensation filters is $L_g = 7$.

A. Montecarlo Simulations of the Adaptive CE

Figs. 9 and 10 show the histograms of the BER for the receiver with and without the CE in the presence of gain errors, phase errors, I/Q time skew, and BW mismatches. Only one effect is exercised in each case. Results of 500 random gain and phase errors uniformly distributed in the interval $\Delta_{\gamma}^{(i)} \in [\pm 0.15]$ (see (3)) and $\delta_{\phi}^{(i)} \in [\pm 0.10]T$, respectively, are depicted in Fig. 9, whereas Fig. 10 shows results for 500 random BW mismatches (see (28)) and I/Q time skews (see (29)) uniformly distributed in the interval $\Delta B_{\gamma}^{(i)} \in [\pm 0.075]B_0$ and $\tau_H, \tau_T \in [\pm 0.10]T$, respectively. In all cases, it is observed that the proposed compensation technique is able to mitigate the impact of all impairments when they are exercised separately\(^3\). In particular, notice that the proposed CE with $L_g = 7$ taps practically eliminates the serious impact on the receiver performance of the I/Q time skew values of Table I.

Fig. 11 shows histograms of the BER for the receiver with and without the CE in the presence of the combined effects. Results of 500 cases with random gain errors, sampling phase errors, I/Q time skews, BW mismatches, and DC offsets as defined in Table I, are presented. Performance of the CE with $L_g = 13$ taps is also depicted. As before, note that the CE is able to compensate the impact of all combined impairments. Moreover, note that a slight performance improvement can be achieved when the number of taps $L_g$ increases from 7 to 13.

\(^3\)Similar performance has been verified with random DC offsets [37].

As mentioned in Section III-B, the impairments of the AFE and TI-ADCs change very slowly over time in multi-gigabit optical coherent transceivers. Therefore the coefficient updates given by (24) and (25) do not need to operate at full rate, and subsampling can be applied. Block processing and frequency domain equalization based on the Fast Fourier Transform (FFT) are widely used to implement high-speed coherent optical transceivers [1]. Then we propose to use block decimation of the error samples to update the CE. Let $N$ be the block size in samples to be used for implementing the EBP. Define $D_B$ the block decimation factor. In this way, only one block of $N$ consecutive samples of the oversampled slicer
error (23) every $D_B$ blocks, i.e.,

$$e^{(i)}[kNDB + n], \quad n = 0, 1, \ldots, N - 1, \forall k$$

with $k$ integer, is used to adapt the CE. Fig. 12 depicts an example of the temporal evolution of the BER in the presence of combined impairments according to Table I for different values of the block decimation factor $D_B$ with $N = 8192$. The instantaneous BER is evaluated every $10^5$ symbols and then processed by a moving average filter of size 40. Gear shifting is used to accelerate the convergence of the CE and reduce the steady-state MSE. In all cases, notice that the use of block decimation practically does not impact on the resulting BER. Therefore it can be adopted to drastically reduce the implementation complexity, as shall be discussed in Section V.

B. Mixed-Signal Compensation of TI-ADC with Highly Interleaved Architectures

The performance of the mixed-signal scheme of Section III-C is investigated in typical hierarchical ultra high-speed TI-ADCs such as those used in high speed receivers [42], [43], [46]. This hierarchical TI-ADC architecture organizes the T&H in two or more ranks with a high number of sub-ADCs. Fig. 13 depicts an example with two ranks. Rank 1 includes $M_1$ switches each of which feeds $M_2$ T&H stages of Rank 2. Then, $M_1 \times M_2$ ADCs are used to digitize the input signal. Successive approximation register (SAR) ADCs are used for this application due to their power efficiency at the required sampling rate and resolution. This approach relaxes the requirements for the clock generation and synchronization. Furthermore, the impact on the input bandwidth is reduced in contrast to T&H with direct sampling [47]. As an example of application of the mixed-signal compensation scheme of Section III-C, its performance in a hierarchical TI-ADC with $M_1 = 16$ and $M_2 = 8$ (i.e., $M_1 \times M_2 = 128$ individual converters) is evaluated. A clock jitter of 100 fs RMS is added to this simulation. Notice that the mixed-signal calibration algorithm adjusts the $M_1$ sampling phases of the switches in the first rank, and the $M_1 \times M_2$ gains and offsets of the individual sub-ADCs.

Fig. 14 shows the temporal evolution of both the BER and the mean signal-to-noise-and-distortion-ratio (SNDR) [42]. A slower convergence than the previous simulation is observed as a result of the larger number of converters (i.e., 128 vs 16). Nevertheless, we verify that the proposed backpropagation based mixed-signal compensation in the presence combined impairments, $M_1 = 16$ and $M_2 = 8$. 

V. HARDWARE COMPLEXITY ANALYSIS

This section discusses some practical aspects of the implementation of the proposed compensation technique. We focus on the two main blocks of the all digital architecture: the compensation equalizer and the error backpropagation block.

A. Implementation of the Compensation Equalizer

As described in Section III, the compensation equalizer in a DP optical coherent receiver comprises 4 real valued finite impulse response (FIR) filters $g^{(i)}[l]$ with $i = 1, 2, 3, 4$, and $l = 0, \ldots, L_g - 1$. From computer simulations of Section IV it was observed that $L_g = 7$ is enough to properly compensate the AFE and TI-ADC impairments. Therefore a time domain implementation is preferred for the CE. Each of these filters has $M$ independent impulse responses $g^{(i)}_n[l]$ which are time multiplexed as $g^{(i)}_n[l] = g^{(i)}_{n+jM}[l]$ (see (13)). Note that time multiplexing of filters with independent responses does not translate to additional complexity when the
filter is implemented with a parallel architecture. The use of parallel implementation is mandatory in high speed optical communication where parallelism factors on the order of 128 or higher are typical. In these architectures, the parallelism factor $P$ can be chosen to be a multiple of the ADC parallelism factor $M$, i.e., $P = q \times M$ where $q$ is an integer. Therefore, the different time multiplexed coefficients are used in fixed positions of the parallelism without incurring in significant additional complexity in relation to a filter with just one set of coefficients (see Fig. 15). We highlight that the resulting filter is equivalent in complexity to the I/Q skew compensation filter already present in current coherent receivers [1]. Since the proposed scheme also corrects skew, the classical skew correction filter can be replaced by the proposed CE without incurring significant additional area or power.

B. Implementation of the Error Backpropagation Block

A straightforward implementation of error backpropagation must include a processing stage for each DSP block located between the ADCs and the slicers. Typically these blocks comprise the BCD, FFE, TR interpolators, and the FCR. All these blocks can be mathematically modeled as a sub-case of the generic receiver DSP block used in Section III-B and the Appendix. The EBP block is algorithmically equivalent to its corresponding DSP block with the only difference that the coefficients are transposed (i.e., compare (36) and (45)). Therefore, in the worst case, the EBP complexity would be similar to that of the receiver DSP block$^4$. Since doubling power and area consumption is not acceptable for commercial applications, important simplifications must be provided.

Considering that AFE and TI-ADC impairments change very slowly over time in multi-gigabit optical coherent transceivers, the coefficient updates given by (24) and (25) do not need to operate at full rate, and subsampling can be applied. The latter allows implementation complexity, and particularly power dissipation, to be drastically reduced. In Section IV-A we evaluated the performance with block decimation where one block of $N$ consecutive samples of the oversampled slicer error are used every $D_B$ blocks. Simulation results not included here have shown a good performance even with $N = 8192$ and $D_B = 256$. The block based decimation approach allows the EBP algorithm to be implemented in the frequency domain when necessary to reduce complexity (for example in the EBP of the BCD and FFE). This error decimation reduces the power dissipation of the EBP to only $1/D_B$ of the power of the corresponding DSP blocks, equivalent to less than 1% in the simulated example. However, the areas of the EBP blocks are still equivalent to the area of their corresponding DSP blocks. To reduce area, the EBP blocks could be implemented using a serial architecture$^5$ or a lower parallelism factor. If a serial implementation is chosen, an area reduction proportional to the parallelism factor is expected at the expense of increasing the latency by a similar amount. The resulting latency is $2 \times (N_{BCD} + N_{FFE}) \times P$ samples, where $N_{BCD}$ and $N_{FFE}$ are the block sizes of the FFTs used to implement the BCD and FFE, respectively (factor 2 includes the FFT / IFFT pair). The latencies of the EBP blocks for the TR interpolators and FCR can be neglected. Therefore the CE adaptation speed is not reduced by a serial implementation of the EBP blocks if $2 \times (N_{BCD} + N_{FFE}) \times P < N \times D_B$.

Details of efficient architectures for implementing the error backpropagation block will be addressed in a future work.

VI. CONCLUSIONS

A new TI-ADC background calibration algorithm based on the backpropagation technique has been presented in this paper. Two implementation variants were presented, one of them all-digital and the other mixed-signal. Simulation results have shown a fast, robust and almost ideal compensation/calibration of TI-ADC sampling time, gain, offset, and bandwidth mismatches as well as I/Q time skew effects under different test conditions in the example of application of a DSP-based optical coherent receiver. Hardware complexity is minimized with serial processing and decimation. As the technique runs in background, the calibration can track parameter variations caused by temperature, voltage, aging, etc., without operational interruptions.

ACKNOWLEDGEMENTS

The authors would like to thank Dr. Ariel Pola for his helpful advice on various technical issues related to the hardware implementation.

$^4$Note that the LMS adaptation hardware of the FFE, the PLL of the FCR and the PLL of the TR do not need to be implemented in the EBP path, which further reduces the complexity of the latter.

$^5$Typically, a serial implementation requires that hardware such as multipliers be reused with variable numerical values of coefficients, whereas in a parallel implementation hardware can be optimized for fixed coefficient values. This results in a somewhat higher power per operation in a serial implementation. Nevertheless, the drastic power reduction achieved through decimation greatly outweighs this effect.
where the time index \( l \) is the Kronecker delta function (i.e., \( \delta_{n,m} = 1 \) if \( n = m \) and \( \delta_{n,m} = 0 \) if \( n \neq m \)). Replacing (41) in (39) we get
\[
\frac{\partial u^j[m + k'M]}{\partial g_{(i_0)}[l_0]} = \sum_{l=0}^{L-1} \Gamma^{(j,i_0)}_{m+k'M}[l] u^{(i_0)}[m+k'M-l-l_0] \delta_{m,m_0}.
\] (42)

Using (42) in (38), we obtain
\[
\frac{\partial \mathcal{E}_N}{\partial g_{(i_0)}[l_0]} \propto \sum_{k'} \sum_{j=1}^{4} \partial e^j[m_0 + k'M] \times \left[ \begin{array}{c} \frac{1}{2} \sum_{l=0}^{L-1} \Gamma^{(j,i_0)}_{m+k'M}[l] u^{(i_0)}[m_0+k'M-l-l_0] \end{array} \right].
\] (43)

Finally, we set \( kM = k'M - 1 \) resulting
\[
\frac{\partial \mathcal{E}_N}{\partial g_{(i_0)}[l_0]} \propto \sum_{k} \sum_{j=1}^{4} \partial e^j[n] \left[ \begin{array}{c} \frac{1}{2} \sum_{l=0}^{L-1} \Gamma^{(j,i_0)}_{n+l}[l] e^j[n+l] \end{array} \right].
\] (44)

where
\[
e^j[n] = \sum_{j=1}^{4} \sum_{l=0}^{L-1} \Gamma^{(j,i_0)}_{n+l}[l] e^j[n+l].
\] (45)

is the backpropagated error. Notice that (44) is the average of the instantaneous gradient component given by \( e^j[n_0 + k'M] w^{(i_0)}[n_0 + k'M - l_0] \). Therefore, an instantaneous gradient of the square error can be obtained as
\[
\nabla_{g_{(i_0)}} \mathcal{E}_N \propto e^j[m + k'M] w^{(i_0)}[m + k'M],
\] (46)

where \( w[n] \) is the \( L_0 \)-dimensional vector with the samples at the CE input defined by (21).

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