Supervised Learning Enhanced Quantum Circuit Transformation

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Abstract—A quantum circuit transformation (QCT) is required when executing a quantum program in a real quantum processing unit (QPU). Through inserting auxiliary SWAP gates, a QCT algorithm transforms a quantum circuit to one that satisfies the connectivity constraint imposed by the QPU. Due to the non-negligible gate error and the limited qubit coherence time of the QPU, QCT algorithms which minimize gate number or circuit depth or maximize the fidelity of output circuits are in urgent need. Unfortunately, finding optimized transformations often involves exhaustive searches, which are extremely time-consuming and not practical for most circuits. In this paper, we propose a framework that uses a policy artificial neural network (ANN) trained by supervised learning on shallow circuits to help existing QCT algorithms select the most promising SWAP gate. ANNs can be trained off-line in a distributed way. The trained ANN can be easily incorporated into QCT algorithms without bringing too much overhead in time complexity. Exemplary embeddings of the trained ANNs into target QCT algorithms demonstrate that the transformation performance can be consistently improved on QPUs with various connectivity structures and random or realistic quantum circuits.

Index Terms—quantum circuit transformation, machine learning, supervised learning, artificial neural network

I. INTRODUCTION

It is widely recognized that Moore’s law, which states that the number of transistors in a dense integrated circuit doubles about every two years, will, if not already has, come to an end in the near future. On the other hand, although still in their infancy, quantum computers or, more precisely, quantum processing units (QPUs) have seen a steady increase in the number of valid qubits in the past several years. QPUs in the Noisy Intermediate-Scale Quantum (NISQ) era have rather limited qubit coherence time and only support a few kinds of one- or two-qubit elementary quantum gates, which usually have non-negligible gate error. Nevertheless, quantum supremacy was demonstrated in Sycamore, Google’s recent 53-qubit QPU [1]. More and more quantum or hybrid quantum-classical algorithms have already been decomposed into an end in the near future. On the other hand, although still in their infancy, quantum computers or, more precisely, quantum processing units (QPUs) have seen a steady increase in the number of valid qubits in the past several years. QPUs impose strict connectivity constraints which require that any two-qubit operation can only be applied between connected qubits. This presents a challenge for quantum computing in the NISQ era. Assume that all quantum gates in a quantum circuit $C$ have already been decomposed into elementary gates supported by the QPU. Before executing $C$, we need to transform $C$ into a functionally equivalent one while obeying the connectivity constraints imposed by the QPU. This process was first considered in [3] and has many different names. In this paper, following [3], we term it as quantum circuit transformation (QCT).

Usually, the QCT process will introduce a large number of auxiliary SWAP gates, which will, in turn, significantly decrease the fidelity of the output. Therefore, algorithms need to be designed that can minimize the gate number or circuit depth and/or maximize the fidelity of the circuit [5]. While it is not difficult to transform a circuit into a functionally equivalent one that satisfies the connectivity constraints, the real challenge lies in finding an optimal one. Currently, there are a few exact QCT algorithms which can construct an equivalent executable circuit with either the minimal number of auxiliary SWAPs [6], [7] or the smallest circuit depth [8]. The problem with these exact algorithms is that they are extremely time-consuming and can only process quantum circuits with very small size and very shallow depth on QPUs with very small number of qubits. For example, it was shown in [7] that the exact solution can be computed within an acceptable time only for circuits with no more than 5 qubits and 100 gates. As a consequence, most existing algorithms are approximate. Roughly speaking, these approximate algorithms can be further divided into two categories. Algorithms in the first category reformulate the QCT problem and apply some off-the-shelf tools to solve it [9], [10], while those in the second use heuristic search to construct the output circuit step-by-step [11]–[18]. As empirically evaluated in [19], these algorithms are still very far from being optimal. Take the industry-level QCT algorithm developed by the Cambridge Quantum Computing (addressed as t|ket⟩ henceforth) as an example. It was shown in [19] that, for IBM Q Tokyo and input circuits with depths from 5 to 45, the optimality gap (the ratio of the output circuit depth of t|ket⟩ to the optimal depth) could still be as high as 5x! Meanwhile, it is worth mentioning that there are QCT algorithms that have significantly better outputs than t|ket⟩. The Monte Carol Tree Search (MCTS) based algorithm devised in [20], called MCTS in this paper, seems to be the best reported QCT algorithm on IBM Q Tokyo,
which inserts in average 60% less SWAP gates than \( t | \text{ket} \) on a set of 114 real benchmark circuits.

Inspired by the recent success of artificial neural network (ANN) \([21]\) in enhancing the MCTS algorithm adopted by AlphaGo \([22]\), we propose a framework in which a policy ANN is trained by supervised learning on shallow circuits to help existing QCT heuristic search algorithms select the most promising SWAP. Supervised learning \([23]\) is the machine learning paradigm of learning a function that maps an input to an output under the supervision of a ‘teacher’ whose role is to provide a set of training examples, represented as a set of labeled training data. For each connectivity structure, such a policy ANN could be trained by using an (almost) exact algorithm or the target QCT algorithm. This is very attractive as ANNs can be trained in a distributed way off-line and more precise training data can be obtained and accumulated by applying (time-consuming) exact or near-exact QCT algorithms on shallow random circuits. Moreover, the trained policy ANN can be embedded in the target heuristic search-based QCT algorithm to enhance its performance. We provide two exemplary embeddings, one uses the SAHS algorithm \([14]\) and the second the MCTS algorithm \([20]\) (cf. Sec.s \([4]\) and \([V]\) for their detailed implementations). Empirical results on QPUs with various connectivity structures and random or realistic quantum circuits demonstrate that the performance of both SAHS and MCTS can be consistently improved by employing the trained policy ANNs.

In the literature, there are also several QCT algorithms which have exploited machine learning techniques. In \([24]\), machine learning is used to optimize the hyper-parameters of QCT algorithms, not being directly involved in the transformation process. Reinforcement learning is utilized in \([25]\) to reduce the depth of the transformed quantum circuit. Different from these works, the proposed policy ANN can be embedded in many existing search-based QCT algorithms to enhance their performance, and the experimental results in Sec. \([IV-C]\) and \([V-C]\) demonstrate that the improvement is obvious and consistent.

The remainder of this paper is organized as follows. After a brief introduction of the QCT problem in Sec. \([I]\) we describe in detail the modules of the proposed framework and validate the efficacy of the trained ANN and its embedding process in Sec. \([III]\). Two exemplary applications of the proposed framework based on different state-of-the-art QCT algorithms are then introduced in Sec. \([IV]\) and \([V]\). The last section concludes the paper with an outlook for future research. The scalability of our framework in terms of the qubit number is discussed in Appendix.

II. THE QUANTUM CIRCUIT TRANSFORMATION PROBLEM

In classical computing, binary digit, or bit, is the basic unit of information which has only two states, 0 or 1. In contrast, quantum bit, or qubit, serves as the basic unit of quantum information, which can be in the superposition \( \alpha |0\rangle + \beta |1\rangle \) of the two basis states, denoted \( |0\rangle \) and \( |1\rangle \) respectively, where \( \alpha, \beta \) are complex numbers and \( |\alpha|^2 + |\beta|^2 = 1 \).

States of qubits can be manipulated by quantum gates. Depicted in Fig. \([1]\) are graphic representation of three quantum gates: Hadamard, CNOT and SWAP. Hadamard is a single-qubit gate that has the ability to generate superposition: it maps \( |0\rangle \) to \( (|0\rangle + |1\rangle)/\sqrt{2} \) and \( |1\rangle \) to \( (|0\rangle - |1\rangle)/\sqrt{2} \). CNOT and SWAP are both two-qubit gates. CNOT flips the target qubit depending on the state of the control qubit; that is, CNOT: \( |c\rangle |t\rangle \rightarrow |c\rangle |c \oplus t\rangle \), where \( c, t \in \{0, 1\} \) and \( \oplus \) denotes exclusive-or. SWAP exchanges the states of its operand qubits: it maps \( |a\rangle |b\rangle \) to \( |b\rangle |a\rangle \) for all \( a, b \in \{0, 1\} \). Note that, as shown in Fig. \([2]\) one SWAP gate can be decomposed into three CNOT gates.

Quantum algorithms are often expressed as quantum circuits each of which consists of a set of qubits and a sequence of quantum gates. Shown in Fig. \([3]\) (left) is a quantum circuit with 5 qubits and 5 gates. The gates in a quantum circuit can be divided into different layers such that gates in the same layer can be executed simultaneously. The first or front layer of circuit \( C \) is denoted by \( L_0(C) \). Likewise, for any \( i \geq 1 \), \( L_i(C) \) represents the \( i \)-th layer of \( C \).

In a QPU, only a limited set of quantum gates, called elementary gates, can be directly executed. Without loss of generality, we assume that the elementary gates of a QPU form a universal set of quantum gates, which consists of the (two-qubit) CNOT gate and some single-qubit gates. Furthermore, we represent the connectivity structure of the QPU as an undirected graph, \( AG = (V, E) \), called the architecture graph \([4]\) (see Fig. \([4]\) for a few examples), in which each node represents a qubit and two qubits are connected if and only if
CNOT gates can be applied between them.

Before executing a quantum circuit on a QPU, two procedures need to be done. The first one is to decompose the gates in the circuit into elementary gates\(^2\) and obtain an equivalent one which we call the elementary circuit; the second is to transform the elementary circuit into one that satisfies the connectivity constraints imposed by the QPU while not changing its functionality. This latter procedure is called quantum circuit transformation (QCT)\(^{[4]}\). Henceforth, we will call the input elementary quantum circuit of QCT logical circuit, its qubits logical qubits, the output circuit physical circuit, and its qubits physical qubits. In this paper, we only consider the QCT procedure. Furthermore, as single-qubit elementary gates can be directly executed on a QPU, we assume that the logical circuits to be transformed consist solely of CNOT gates.

To transform a logical circuit \(LC\) to a physical one executable on a QPU, we first map (or allocate) the logical qubits in \(LC\) to the physical qubits in \(V\). A two-qubit (CNOT) gate in the front layer of \(LC\) is executable if the allocated physical qubits of its operand logical qubits are adjacent in the architecture graph \(AG\) of the QPU. Note that in general it is unlikely that all gates in \(LC\) are executable by a single mapping. Once no gates are executable by the current mapping \(\tau\), a QCT algorithm seeks to insert into the circuit one or more ancillary SWAP gates to change \(\tau\) into a new mapping so that more gates are executable. This insertion-execution process is iterated until all gates from \(LC\) are executed. Fig.\(^3\) shows a physical circuit transformed from the logical circuit on the left.

The objective of the QCT procedure may vary in different algorithms, e.g., gate count\(^{[11],[12]}\), depth\(^{[8]}\) and fidelity\(^{[27]}\). In this paper, we only consider algorithms which aim to minimize the total number of CNOT gates in the output physical circuit. Recall that each SWAP can be decomposed into 3 CNOT gates as shown in Fig.\(^2\). This is equivalent to minimizing the number of inserted SW AP gates.

III. SUPERVISED LEARNING FOR QUANTUM CIRCUIT TRANSFORMATION

Recall that the main idea behind the QCT process is to insert SWAP gates step-by-step to construct the physical circuit. Hence, the strategy used to select the most promising SWAP among the candidate set often has a significant impact on the performance of the QCT algorithm. A wide range of QCT algorithms utilize heuristic-based evaluation functions to assist this process. Whereas, this evaluation strategy is usually ‘short-sighted’ and only able to take the information in the current state into consideration. To tackle this issue, a trained policy ANN can be used to boost the accuracy of the evaluation process.

The idea of our ANN-based framework is to first train an ANN using a ‘feeding’ QCT algorithm, say QCT-A, and then boost the target QCT algorithm (possibly different from QCT-A), say QCT-B, with the trained ANN. In this section, after describing the ANN-based framework in detail, we show that the ANN trained itself can be directly used for quantum circuit transformation. Furthermore, we introduce a baseline QCT algorithm, called BASE, and then demonstrate how to boost BASE with a trained ANN.

For all experimental evaluations in this paper, we use Python as the programming language, and all experiments are done on a laptop with i7-11800 CPU, 32 GB memory and RTX 3060 GPU. We use both random and realistic circuits as benchmarks, which, together with detailed experimental data, can be found in GitHub\(^1\).

A. Details of the Framework

For any QPU with architecture graph \(AG = (V,E)\) and any target QCT algorithm QCT-B, our framework intends to generate an enhanced QCT algorithm that performs better than QCT-B. This is achieved by employing supervised learning to train a policy ANN which is able to evaluate and recommend possible SWAP operations for input circuits. Fig.\(^5\) shows the basic modules of the proposed framework and their detailed implementations are elaborated as follows.

Training Circuits Generation. In this module, a large number of training circuits containing \(n_l\) layers of gates and \(n_q = |V|\) qubits will be randomly generated. More precisely, suppose we want to generate \(n_c\) circuits for training. Starting from an empty circuit \(C\) with \(n_q\) qubits, we keep adding to \(C\) randomly placed CNOT gates until its depth reaches \(n_1 \cdot n_c\). The final circuit set is then obtained by sequentially slicing \(C\) into \(n_c\) sub-circuits each with \(n_l\) layers.

Label Generation. For each training circuit \(C_i\) generated in the previous module, we attach a probability distribution \(p_i\) of recommended SWAPs, which is called the label of \(C_i\) and is calculated by appropriately invoking the feeding QCT algorithm on \(C_i\) and extracting a non-negative number for each.

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1https://github.com/BensonZhou1991/Supervised-Learning-Enhanced-Quantum-Circuit-Transformation/
edge (corresponds to a SWAP operation) in \( AG \). The concrete implementation depends on the specific feeding algorithm. Shortly we shall see two examples in Sec.s V-A and V-B.

**ANN Training.** With the circuits \( C_i \) and labels \( p_j \) generated in the previous modules as the ‘teacher’, we now train a policy ANN which, for any input circuit \( C \) with \( n_l \) layers and \( n_q \) qubits, outputs a discrete probability distribution \( p \), called the recommendation probability distribution of \( C \) henceforth, representing how strongly the ANN recommends each valid SWAP operation (corresponding to an edge in \( AG \)).

The ANN training process takes the mean squared error (MSE) and Adam [28] as, respectively, the loss function and optimization method.

The input circuits of the policy ANN are encoded as a sequence of symmetric 0-1 matrices \( M^k : 1 \leq k \leq n_l \) of dimension \( n_q \times n_q \), where \( M^k_{i,j} = 1 \) if and only if in the \( k \)-th layer there exists a CNOT gate acting on the \( i \)-th and \( j \)-th qubits (the direction is irrelevant). Obviously, these matrices are all symmetric. In our implementation, these matrices are further flattened and concatenated into a 0-1 vector.

**Example 1:** Consider the logical circuit and the target \( AG \) depicted in Fig. 6 where \( n_q = 6 \) and \( n_l = 5 \). Then we have

\[
M^1_{1,5} = M^1_{5,1} = \cdots = M^5_{0,2} = M^5_{2,0} = 1
\]

and other entries are all 0.

For each input circuit \( C \), let \( p \) be the recommendation probability distribution of \( C \) output by the ANN. Intuitively, the higher the probability a SWAP operation in \( p \), the more the ANN ‘thinks’ the corresponding SWAP is promising and the QCT algorithm should be more inclined to select it as the next SWAP in constructing the executable physical circuit.

**Example 2:** Back to the logical circuit and the target \( AG \) depicted in Fig. 6 Taking the MCTS algorithm [20] as the feeding algorithm (cf. Sec. V), the output probability distribution of our trained ANN can be converted to a histogram that shows to what extent the ANN recommends each valid SWAP (cf. Fig. 6), where the SWAP \((v_1, v_3)\) gets the highest value (around 33%). This reflects the fact that if inserting the SWAP \((v_1, v_3)\) then only two SWAPs are required in the whole QCT process (i.e., the SWAP \((v_1, v_3)\) at the beginning and then another SWAP \((v_1, v_3)\) in front of the 4th layer), which is the minimal number we can have.

**ANN Embedding.** The trained ANN can be used in several ways. We can use it to completely replace the evaluation process and thus devise a new algorithm (called ANN-QCT henceforth) for circuit transformation (cf. Sec. III-B), or use it to assist in the evaluation process when ties need to break (cf.

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**Fig. 5.** The modules composing the proposed framework (left) and the system diagrams for Label Generation (middle) and (ANN-embedded) QCT algorithm (right), where LC and AG stand for logical circuit and architecture graph, respectively.

**Fig. 6.** An example logical circuit with 6 qubits and 5 layers (a) and the corresponding output probability distribution (c) of the ANN trained under the Grid 2X3 AG (b). The naive mapping, which allocates \( v_i \) to \( v_i \) for \( 0 \leq i \leq 5 \), is used here.
Algorithm 1: BASE

input: An architecture graph \( AG = (E, V) \), a logical circuit \( LC \), and an initial mapping \( \tau_{\text{ini}} \).
output: A physical circuit satisfying the connectivity constraints in \( AG \).

begin
\( PC \leftarrow \) all gates in \( LC \) executable under \( \tau_{\text{ini}} \);
\( LC \leftarrow LC \) with gates in \( PC \) deleted;
\( \tau \leftarrow \tau_{\text{ini}} \);
while \( LC \neq \emptyset \) do
    \( \text{best\_cost} \leftarrow \infty \);
    for all \((v_i, v_j) \in E\) do
        \( \tau' \leftarrow \tau[\tau^{-1}(v_i) \mapsto v_j, \tau^{-1}(v_j) \mapsto v_i] \);
        \( \text{current\_cost} \leftarrow \text{COST}(LC, \tau') \);
        if \( \text{current\_cost} < \text{best\_cost} \) then
            \( \text{best\_swap} \leftarrow \text{SWAP}(v_i, v_j) \);
            \( \text{best\_mapping} \leftarrow \tau' \);
            \( \text{best\_cost} \leftarrow \text{current\_cost} \);
        \end{if}
    \( \tau \leftarrow \text{best\_mapping} \);
    \( C \leftarrow \) the set of all executable gates in \( LC \) under \( \tau \);
    \( LC \leftarrow LC \) with all gates in \( C \) deleted;
    \( PC \leftarrow PC \) by adding \( \text{best\_swap} \) and all gates in \( C \);
    return \( PC \)
end

Example 3: Back to the logical circuit, denoted \( LC \), in Fig. 6. Given the naive mapping \( \tau_0 \) which allocates \( q_1 \) to \( v_i \) for \( 0 \leq i \leq 5 \), since the first layer contains only one CNOT gate (involving \( q_1 \) and \( q_3 \)), it is easy to observe that both \( (v_1, v_3) \) and \( (v_3, v_5) \) take \( \tau_0 \) to a new mapping for which the total distance in Eq. 1 achieves its minimum 0. BASE does not distinguish between them and simply chooses the first found one to insert into the output circuit.

We have done experiments on two AGs, Grid 4X4 and IBM Q Tokyo (cf. Fig. 3) for which the ANNs are trained by SAHS (cf. Sec. IV) and MCTS (cf. Sec. V), respectively. The benchmark set consists of 10 circuits each with \(|V|\) qubits and 200 randomly placed CNOT gates, where \(|V|\) represents the number of vertices in the corresponding AG, i.e., number of physical qubits. The results are shown in Table I and the improvement is calculated as

\[
gate\_count\_reduction = (n_{\text{base}} - n_{\text{test}}) / n_{\text{base}},
\]

where \( n_{\text{test}} \) and \( n_{\text{base}} \) are, respectively, the CNOT overheads brought by the tested algorithm and the baseline algorithm. From Table I we can see that, when compared to BASE, both trained ANNs are able to get significantly better solutions (up to 23%), indicating the accuracy of the outputs of the trained ANN. Surprisingly, ANN-QCT is even better than the Qiskit\footnote{https://qiskit.org/} and comparable to \( t\)ket\footnote{https://qiskit.org/}, which are two widely used industry-level QCT algorithms.

| AGs          | Algorithms | CNOT Overhead | Comp. |
|--------------|------------|---------------|-------|
| Grid 4X4     | BASE       | 8388          | 0.00% |
|              | Qiskit     | 7590          | 9.51% |
|              | t\ket      | 5895          | 29.72%|
|              | ANN-QCT    | 6789          | 19.06%|
|              | BASE-ANN   | 6050          | 28.11%|
| IBM Q Tokyo  | BASE       | 6396          | 0.00% |
|              | Qiskit     | 6294          | 1.59% |
|              | t\ket      | 4854          | 28.33%|
|              | ANN-QCT    | 4896          | 23.45%|
|              | BASE-ANN   | 4821          | 24.62%|
| Google Sycamore | BASE       | 22464         | 0.00% |
|              | Qiskit     | 17967         | 20.02%|
|              | t\ket      | 15837         | 29.50%|
|              | BASE-ANN   | 17904         | 20.30%|

Remark 1: The layer number \( n_L \) selected in the framework has two direct effects on the ANN Training and Embedding modules. On one hand, a small \( n_L \) implies that the circuits generated in the ‘Training Circuits Generation’ module are easy to train; on the other hand, a large \( n_L \) may increase the prediction precision of the trained policy ANN. Therefore, we need to trade off easy training with precision by selecting the appropriate value for \( n_L \). We refer the reader to Sec. V-C for more detailed discussion.

B. ANN-QCT and BASE

As said above, the trained ANN derives a QCT algorithm called ANN-QCT, which, at each step, applies the SWAP operation with the highest recommendation probability provided by the ANN. We now validate the efficacy of the trained ANN by experimentally comparing ANN-QCT with a baseline algorithm (denoted BASE) which utilizes straightforward strategies and considers only the first layer of the current logical circuit.

The strategy of selecting the appropriate SWAP at each step plays a key role in the performance of a QCT algorithm. In BASE, this is achieved with the help of a cost function defined as the total distance of the first layer of CNOT gates:

\[
\text{COST}(LC, \tau) = \sum_{g \in L_0(LC)} \text{dist}_{AG}(g, \tau)
\]

where \( LC \) is the logical circuit under consideration, \( \text{dist}_{AG}(g, \tau) \) is the minimal distance in \( AG \) of the two operands physical qubits of CNOT gate \( g \) under the mapping \( \tau \). Then the first (best) SWAP which minimizes this cost function will be chosen to be added to the physical circuit. The detailed pseudo code can be found in Alg. I.

Example 1: Back to the logical circuit, denoted \( LC \), in Fig. 6. Given the naive mapping \( \tau_0 \) which allocates \( q_1 \) to \( v_i \) for \( 0 \leq i \leq 5 \), since the first layer contains only one CNOT gate (involving \( q_1 \) and \( q_3 \)), it is easy to observe that both \( (v_1, v_3) \) and \( (v_3, v_5) \) take \( \tau_0 \) to a new mapping for which the total distance in Eq. 1 achieves its minimum 0. BASE does not distinguish between them and simply chooses the first found one to insert into the output circuit.
C. BASE-ANN

To exhibit the potential of the ANN Embedding module in our framework, an exemplary embedding strategy for BASE is proposed and evaluated.

As shown in Example 3, it is often the case that more than one SWAP achieve the minimal cost of Eq. 1 and BASE may choose the wrong one which performs worse in converting the whole circuit. To resolve this problem, we utilize the trained ANN to help further evaluate the best SWAP operations found in the FOR loop of Alg. 1.

More specifically, let \( \text{best}_{\text{swaps}} \) be the set of SWAPs which achieve the minimal cost with respect to the current logical circuit \( LC \) and mapping \( \tau \). To break the tie in choosing a best SWAP from \( \text{best}_{\text{swaps}} \), the next \( n_l \) layers of gates in \( LC \) are extracted and a trained policy ANN is invoked to provide a recommendation probability distribution. The SWAP in \( \text{best}_{\text{swaps}} \) with the highest recommendation probability will be chosen to be added to the physical circuit. We call the enhanced algorithm BASE-ANN henceforth.

For BASE-ANN, three AGs — IBM Q Tokyo, Grid 4X4, the 53-qubit Google Sycamore (cf. Fig. 4) — are tested. The ANNs for two small AGs are trained by SAHS (cf. Sec. IV), while the ANN for Sycamore is trained by BASE, which is similar to the one trained by SAHS, except that \( \text{BASE} \) is replaced with \( \text{BASE}(LC', AG, \tau', d) \)

\[
\text{PC}' \leftarrow \text{SAHS}(LC', AG, \tau', d)
\]

in Alg. 2 is replaced with \( \text{PC}' \leftarrow \text{BASE}(LC', AG, \tau') \).

This is mainly because the label generation process for SAHS and Sycamore is too expensive (in terms of computer time consumption). Besides that, the settings and other ANNs used in the experiment are identical to that for ANN-QCT (cf. Table. I). It can be observed that even this simple embedding strategy suffices to manifest the efficacy of the ANN embedding process (up to 28% improvement brought by BASE-ANN compared with BASE). Furthermore, the improvement of BASE-ANN is consistent (>20%) even on Google Sycamore, a QPU with 53 qubits, demonstrating the potential of the proposed method in AGs with large number of qubits.

In above we have seen that the ANN framework can greatly boost the performance of a baseline QCT algorithm. In the following sections, we shall see that it can also steadily boost the performance of two state-of-the-art QCT algorithms, SAHS [14] and MCTS [20].

IV. SUPERVISED LEARNING EMBEDDED IN SAHS

Proposed in [14], SAHS (simulated annealing and heuristic search) is an efficient QCT algorithm which utilizes a double look-ahead mechanism to implement the multi-depth heuristic search. In SAHS, the search depth, denoted by \( d \) henceforth, is a pre-set parameter, through which the trade-off between the running time and the quality, i.e., number of gates, of the transformed circuit can be adjusted. In this section, SAHS is used as both the feeding and target QCT algorithms to showcase the efficacy of the proposed framework, and its ANN enhanced counterpart is named SAHS-ANN.

A. Label Generation

Described in Alg. 2 is a rough overview for the label generation process based on SAHS, the detailed implementation of which can be found in [14]. As seen in Alg. 2, SAHS will be invoked multiple times to evaluate the candidate SWAPs to generate the label for each training circuit. In this label generation process, the layer number \( n_l \) of the training circuits is fixed as 3. Besides, the search depth \( d \) for SAHS is set to 2, which is also the default value in its original implementation.

![Algorithm 2](https://example.com/algorithm2.png)

**Algorithm 2: Label generation via SAHS**

**input:** An architecture graph \( AG \) and a logical circuit \( LC \).

**output:** A recommendation probability distribution.

begin

\[
\tau \leftarrow \text{the naive mapping};
\]

\[
d \leftarrow 2;
\]

for all \( e \in E \) do

\[
\tau'[e] \leftarrow \tau^{-1}(v_i) \rightarrow v_j, \tau^{-1}(v_j) \rightarrow v_i;
\]

\[
\text{LC}' \leftarrow \text{LC} \text{ with all executable gates under } \tau' \text{ deleted};
\]

\[
\text{PC}' \leftarrow \text{SAHS}(\text{LC}', \text{AG}, \tau', d);
\]

\[
w(e) \leftarrow \text{number of SWAPs inserted in } \text{PC}';
\]

\[
p \leftarrow \text{the probability distribution proportional to } w(e)\frac{1}{w(e)+1};
\]

return \( p \)

B. ANN Embedding

In the original SAHS algorithm, the quality of the solution can be significantly improved through increasing \( d \). However, this will also exponentially increase the running time, making it unacceptable even for small-size circuits (see data with pruning ratio 0 in Fig. 8). To offset this time overhead, the policy ANN which solely consists of fully connected layers and is trained via circuits randomly generated in the ‘Training Circuits Generation’ module (cf. Sec. III-A) and labels will be embedded in the evaluation process of SAHS.

In SAHS, the QCT problem is reformulated as a search problem, each node and each edge in which contain, respectively, an unfinished physical circuit and a specific SWAP gate to be added to the circuit in its connected parent node. During the search process, the leaf nodes will be opened iteratively until reaching the pre-defined search depth \( d \). In the enhanced algorithm SAHS-ANN, the trained policy ANN will be invoked before a node is opened and each candidate SWAP is given a recommendation probability. Then, a proportion, which is termed as the pruning ratio henceforth, of SWAPs will be pruned to decrease the branching factor of the node. Besides that, all other modules are identical to that in SAHS.

This ANN-aided pruning mechanism is able to make the search process go deeper while significantly reducing the time overhead when compared to the original SAHS algorithm.
C. Experimental Results

To demonstrate the efficacy of SAHS-ANN, experiments have been done on Grid 4X4. Figs. 7 and 8 show, respectively, the improvement compared to the original SAHS with depth 2 and the time efficiency under different depth and pruning ratio settings. Note that the improvement data in this section are always obtained by comparing with SAHS in depth 2. From Figs. 7 and 8 we observe that, for SAHS, the quality of solutions can be improved via increasing the search depth (9.2% when depth is 4) at the cost of a dramatic time efficiency degrading (from 84.7 gates per second to only 0.4). Very attractively, SAHS-ANN is able to obtain a similar quality improvement in depth 5 and pruning ratio 0.7 while its time efficiency is much more promising (7.4 gates per second vs. 0.4) than that of SAHS. It can be found in Fig. 9 that SAHS-ANN is able to gain more than 6% improvements on most tested circuits in depth 5 and pruning ratio 0.7, indicating the stability of the proposed algorithm. Moreover, a 11% improvement can be derived from SAHS-ANN when the search depth is increased to 6 and, while its time efficiency is still significantly better (1.6 gates per second vs. 0.4).

It is worth mentioning that, when the pruning ratio reaches 0.9, the performance of SAHS-ANN degrades steeply, making the algorithm almost unusable (cf. Fig. 7). This is perhaps due to that the ANN used is not always precise and most promising candidates may be pruned away when the ratio is too large.

Now we discuss the influence brought by increasing the search depth to the running time of SAHS and SAHS-ANN. As can be seen from Fig. 10, the time efficiency of SAHS decreases dramatically as the search process goes deeper, especially when the depth exceeds 3. At the mean time, the time efficiency of SAHS-ANN (with pruning ratio 0.7) is much larger than that of SAHS (24.5 vs. 0.4 when the search depth is 4), which makes it possible for SAHS-ANN to go deeper and, in return, better solutions can be obtained (e.g., an improvement of 11.0% with time efficiency 1.6 when the search depth goes to 6).

At last, we evaluate the effect of the parameter \( n_l \) (layer number) of the training circuits on Grid 4X4 AG. Intuitively, the efficacy of embedding an ANN trained with a larger \( n_l \) to the target QCT algorithm should be more promising than that with a smaller \( n_l \). However, a larger \( n_l \) also results in the blow-up of the amount of the information needed to be learned by the ANN, which, in turn, brings a huge challenge for the training process. As depicted in Fig. 11 better solutions can be derived when the value of \( n_l \) is set to 2 or 3, manifesting the rationality of the parameter selection in SAHS-ANN.

Besides Grid 4X4, experiments are done on IBM Q...
Guadalupe\textsuperscript{3} with 16 qubits. The results show that the improvement of SAHS-ANN is consistent, 6.0% in depth 5 and pruning ratio 0.7 and 9.3% in depth 6 and pruning ratio 0.7.

To further demonstrate the practicability of the proposed framework, additional experiments are devised on one new benchmark set with 159 realistic circuits, and Grid 4X4. For this benchmark set, 11 circuits are randomly selected as the test set and the rest are used to compose the training set for the ANN. To make the training set large enough, those circuits are further sliced into multiple sub-circuits each containing $n_l$ layers of CNOT gates.\textsuperscript{4} The results show that a 7.09% improvement can be obtained in depth 5 and pruning ratio 0.5. Furthermore, we also test SAHS-ANN in another benchmark set containing 143 quantum circuits extracted from the quantum algorithm library in Qiskit. SAHS-ANN works much better in this benchmark set, obtaining a 19.50% improvement in depth 5 and pruning ratio 0.7 on Grid 4X4.

To show the scalability of the proposed framework in terms of gate numbers, experiments are also done on a benchmark set consisting of 60 circuits with 16 qubits. Circuits in this benchmark set contain only CNOT gates and their numbers range from 50 to 300. For each number, we transform all circuits under Grid 4X4 using SAHS-ANN with depth 5 and pruning ratio 0.7. Fig. 12 shows the average improvement when compared with SAHS with search depth 2. Fig. 13 shows the average time efficiency, which is the ratio of the number of gates to the running time (seconds). The results show that the improvement and time efficiency of the proposed SAHS-ANN are consistent and steady (ranging from 6.4% to 12% and 7 to 8.4 gates per second) under various input circuit sizes, and hence demonstrate the scalability of SAHS-ANN in terms of gate numbers of the input circuits.

V. Supervised Learning Embedded in MCTS

A Monte-Carlo-Tree-Search based QCT algorithm, abbreviated as MCTS henceforth, is proposed in [20]. MCTS consists of five modules, Selection, Expansion, Simulation, Backpropagation, and Decision. Through each invoking of the Decision module, a SWAP gate will be added to the output physical circuit. Before each Decision, the Selection, Expansion, Simulation modules will be iteratively executed $n_{bp}$ (a pre-defined parameter) times to provide evaluations for each candidate SWAP gate. Naturally, a larger $n_{bp}$ will increase the precision of the evaluation process at the cost of significant time overhead. MCTS is able to reach a much larger search depth while the complexity is still polynomial and the experimental results show that it exceeds the state-of-the-art QCT algorithms by a large margin in terms of the gate overhead on IBM Q Tokyo. In this section, MCTS is used as the feeding and target QCT algorithm to further demonstrate the efficacy of the proposed framework.

A. Label Generation

To label the training circuits, a modified version of MCTS is used to generate the probability distribution of recommended SWAPs (see Alg. 3 for the details). To increase the reliability of output distributions, we empirically set the parameter $n_{bp}$ to 200, which is much larger than the original value 20 chosen in [20], in the label generation process. Note that the layer number $n_l$ of the training circuits is empirically set to 5.

Algorithm 3: Label generation via MCTS

\begin{verbatim}
input : An architecture graph $AG$ and a logical circuit $LC$.
output: A recommendation probability distribution.
begin
\texttt{\tau}_{ini} \leftarrow \text{the naive mapping};
PC \leftarrow \text{all gates in } LC \text{ executable under } \tau_{ini};
LC \leftarrow LC^{'} \text{ with gates in } PC \text{ deleted};
T \leftarrow \text{a search tree with a single (root) node } (\tau_{ini}, PC, LC);
\textbf{do}
\quad s \leftarrow \text{Select}(T);
\quad \text{Expand}(T, s);
\quad \text{Simulate}(T, s);
\quad \text{Backpropagate}(T, s);
\textbf{for} $n_{bp}$ \textbf{times};
\quad p \leftarrow \text{the probability distribution proportional to the scores of all child nodes of root}(T);
\textbf{return} p
\end{verbatim}

B. Embedding ANN to MCTS

As shown in Alg. 3, the main part of MCTS consists of four modules: Selection, Expansion, Simulation, and Backpropagation. Similar to SAHS-ANN, we integrate the trained

\begin{footnote}{https://quantum-computing.ibm.com/}
\end{footnote}

\begin{footnote}{Single-qubit gates will be ignored because they have no effect to the QCT process when the objective is minimizing the gate count.}
\end{footnote}
policy ANN to the Decision module to prune the unpromising child nodes of the root. Specifically, when reaching a new root in Decision, the ANN is invoked and each child of that root is given a recommendation probability according to its corresponding SW AP operation. Then a proportion, called the pruning ratio, of the children are pruned. This ANN-based pruning process helps MCTS to focus only on nodes with more potential. Besides that, all other modules and parameters are identical to that in the original MCTS in \cite{20}. The ANN-enhanced MCTS algorithm is called MCTS-ANN henceforth.

C. Experimental Results

In this section, experimental results are exhibited to show the performance of MCTS-ANN.

We trained a policy ANN via the strategy introduced in Sec. V-A for IBM Q Tokyo (cf. Fig. 4) with MCTS the feeding QCT algorithm and \( n_t \) being empirically set to 5. Furthermore, since MCTS is a stochastic process, we run both MCTS and MCTS-ANN 5 times for each circuit and record the minimal gate counts in the output circuits. For running time, the average for each input circuit is recorded.

The performance of MCTS-ANN on IBM Q Tokyo in terms of gate count reduction and time efficiency are depicted in Figs. 14 and 15 respectively, where the benchmarks used are those used for experiments for Table I. The figures show that the performance of MCTS is effectively improved by MCTS-ANN. For example, the improvement is the most promising (up to 8%) when the pruning ratio reaches 0.7. This is because a larger pruning ratio will reduce the branching factor of the root and therefore ‘encourage’ the search process to go deeper under the limited expansion times. As for time efficiency, MCTS-ANN is slightly worse than MCTS, which is acceptable considering the performance improvement (up to 8%).

VI. Conclusion

In this paper, we proposed an effective framework based on the idea of using policy ANNs to help existing QCT algorithms in selecting the best SWAP operation. The policy ANNs can be trained through supervised learning for any specific architecture graph. To demonstrate the effectiveness of the approach, two exemplary ANN-enhanced algorithms, SAHS-ANN and MCTS-ANN, are presented. Experimental results confirm that the trained policy ANN can indeed bring a consistent improvement to their performance on various sets of random and real benchmark circuits and architecture graphs.

Our current implementation of the framework is far away from being optimal. As can be seen from Figs. 7 and 14, the best improvement brought by ANNs is limited (less than or around 10%). This is possibly due to the poor quality of the currently available training data, and can be fixed by utilizing more advanced (or exact) algorithms to generate the labels. One candidate is the recently developed near-exact algorithm TB-OLSQ \cite{8}, which encodes the QCT problem as a satisfiability modulo theories optimization problem (SMT) and outperforms several leading heuristic approaches in output circuit quality while being much more efficient than those exact algorithms. Alternatively, labels with better qualities may also be obtained by heuristic algorithms with a radical parameter setting. For example, we can set search depth to 3 or even larger for SAHS where the default value is 2.

Both methods are particularly time-demanding for the hardware we used — a laptop with i7 CPU and 32 GB memory. For example, the time consumption for generating labels for 1000 random circuits on Grid 4X4 is about 15 minutes using SAHS in depth 2; this figure will be boosted to more than 4 hours when the depth is increased to 3. The situation becomes even worse when the architecture graph has more qubits. In that case, distributed or cloud computing could be used to speed-up the training process and improve the quality of the trained ANN. Moreover, using the proprietary \( \langle |\text{ket}\rangle \), instead of SAHS, as the feeding algorithm could reduce the training time by 90%. More importantly, this can be done off-line and only one ANN is required for each architecture graph. With affordable computing resource, these approaches are viable and will be one direction of our future research.

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APPENDIX

We analyze the scalability in terms of the qubit number both theoretically and experimentally for the label generation process. Assume the target algorithm used is SAHS in search depth 2, the layer number \( n_l \) for training circuits is 3, and the AGs are all Grid \( k \times k \) like architectures. That is, the AGs have \( |V| = k^2 \) physical qubits. Recall that the time complexity of SAHS is \( O(V^k \cdot |E|) \) for each circuit is \( 3, \) and the \( m \) are the number of edges in AG and gates in the logical circuit, respectively. Hence, the complexity for generating a label for one circuit is \( O(V^{k} \cdot |E|^{1/2} \cdot m) \) because at most \( |E| \) SWAP gates will be evaluated and for each evaluation process, SAHS has to be invoked for one time. Then, according to the previously made assumptions, it can be derived that \( |E| = 2(|V| - \sqrt{|V|}) \) and \( m \leq 1.5|V| \). As a result, the overall complexity for generating one label is bounded by \( O(V^5) \).

Experiments are done to further reveal this scalability. For AGs with different qubit numbers, we use SAHS in search depth 2 to generate labels for 100 random circuits each containing 3 layers of CNOT gates, and record the running time. As can be seen from Fig. 16 the real time cost is about the 4.4th power in the number of physical qubits. For example, the time consumption of generating 100 labels via SAHS for Grid 4X4 and Sycamore are about 130 and 45,820 seconds, respectively. Note that \( 130 \times (\frac{51}{4 \sqrt{2}})^{4.4} = 25,271 \), which is in the same order of magnitude as 45,820.

Fig. 16. Running time (seconds, vertical axis) obtained by using SAHS in search depth 2 to generate labels for 100 random circuits vs. various qubit numbers in AGs (horizontal axis), where the subgraph inside is a zooming in to curves between 4 and 16 qubits.