Bandwidth-Increased Ripple-Mitigating Scheduling Algorithm for Dynamically Reconfigurable Batteries

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ABSTRACT  Modular cascaded circuits offer attractive qualities in reconfigurable battery applications, including improved fault tolerance and flexibility. In contrast to conventional hard-wired dc battery packs, however, cascaded topologies, such as modular multilevel circuits (MMC) with serial or serial and parallel connectivity, load modules with substantial low-frequency current ripple, which generates additional loss and can accelerate battery aging. Recent studies reveal that low-frequency ripple can cause noticeable battery aging, whereas high frequencies are insignificant, presumably mainly as they can be absorbed by the dielectric electrode capacitance, and reduce heating associated with lower high-frequency battery impedance. Previous MMC–battery control methods solely focus on state-of-charge and thermal balancing of individual modules, while the few existing methods for suppressing ripple tend to form low-frequency patterns in the modules’ load, which increase battery cycling as well as loss. This paper presents a ripple-oriented high-bandwidth control technique that minimizes low-frequency components in the module load spectrum and improves battery treatment, while maintaining the average switching frequency. The control method takes limitations related to module data acquisition into account and enhances the feedback bandwidth using observers. It works with a wide range of topologies including modules with series connectivity only as well as series/parallel. The measurements in the laboratory verify the shift of the module load from the 10 – 100 Hz range to $\sim$5 kHz and a reduction of battery losses by up to 20%.

INDEX TERMS Modular battery, modular multilevel converter, cascaded bridge converter, reconfigurable battery, battery ageing model, ripple suppression, influence of ripple current, second harmonic, scheduling, battery energy storage systems (BESS), electric vehicle drive trains.

I. INTRODUCTION

A. RECONFIGURABLE BATTERIES

Both electromobility and grid storage are rapidly developing applications of power electronics and batteries. They use battery packs as an energy tank and an electronic inverter to generate the ac output for the motor or grid. Conventionally, cells are hard-wired in a battery pack with certain fixed parallel and serial configuration [1].

For both electric vehicles and grid-connected storages with hard-wired batteries, the dominant load is determined by the inverter. The ac side of the inverter supplies the grid or an electric motor with ac current, whereas the dc link of the inverter loads the battery [2]. For three-phase output, the dc-link load typically contains a dc component with the 6th harmonic as well as further multiples of the ac frequency [3]. In addition, the spectrum includes the switching frequency of the inverter and its harmonics. The distribution of the current in the battery pack among individual cells is determined by the impedance of interconnections and cells, and their voltage differences. Different impedances of current paths through the battery can lead to unequal discharge rates and consequently to a spread in cell ageing [4], [5], [6], [7].
with pair-wise module interconnection for CHB with grid connection as storage or charging vehicle. This macro-topology reduced and varied versions. (b) Overall system topology in drive trains or latter also paralleling of modules, both existing also in a number of former exclusively allowing series/bypass inter-module connectivity, the

![FIGURE 1. Diagram of the system topology: (a) battery module with CHB (left) and CHB\(^2\) (right, micro-topology used here) switch topology; the former exclusively allowing series/bypass inter-module connectivity, the latter also paralleling of modules, both existing also in a number of reduced and varied versions. (b) Overall system topology in drive trains or with grid connection as storage or charging vehicle. This macro-topology with pair-wise module interconnection for CHB\(^2\) modules also serves for the experimental demonstration here.](image)

Alternatively, modular circuit structures such as modular multilevel converters (MMC) with batteries—batteries of usually several cells, together typically below 100 V (due to a sweet spot in present transistor technology and safety regulations), rarely just single cells in each module (associated with a high overhead for the necessary peripheral electronics and control)—offer interesting advantages and can form battery systems with immediate multiphase ac output [8]. The MMC–battery topology combines power electronics and batteries, most frequently based on cascaded H bridges (CHB). In contrast to hard-wired batteries, the distributed power electronics can dynamically reconfigure the module interconnection and control the power of individual modules. Thus, reconfigurable MMC–battery systems offer excellent balancing of the state of charge [9], [10] and state of health [11], [12], [13], [14], introduce fault tolerance by bypassing defective modules or even semiconductors [15], [16], [17], [18], and increase the effectively available capacitance of battery systems [9], [19]. Several companies are developing or already market commercial systems based on battery-integrated CHB/MMC [20], [21], [22], [23], [24], [25], [26], [27]. Further advantages of reconfigurable batteries and comparison with hard-wired ones can be found in the literate [28], [29].

### B. MODULE-LOAD RIPPLE

In all CHB circuits, the load currents of the individual module batteries depend on the macro-level topology. In case of a star configuration and ac output, the modules are divided into phase strings, where each of the phase strings supplies one output phase, for instance of a motor or the grid. As a result, the module load is rippled. The spectrum of the module load contains a strong 2\(^{\text{nd}}\) harmonic of the output ac frequency [30], [31], [32]. CHBs without parallel module connectivity alternate between an active state of the module (series module connection), where modules run on phase load, and an inactive state of the module (bypass state), where modules have zero load [33]. Alternating these states introduces components of variable frequency in the module load spectrum. Thus, they depend on the specific control strategy. Such ripple load on the battery cells inside a module occurs in addition to the load current. The ripple load does not contribute to the active output power but constitutes reactive power fluctuations. As the reactive ripple current loads the equivalent resistances of module components and connections, it generates unnecessary additional loss. The associated extra heating can easily cause derating in typical thermally limited automotive batteries, and may further degrade the battery.

Load ripple is commonly subjected to hardware filtering, most prominently the dc-link capacitance. Separate filtering often serves for the reduction of the load ripple in CHB modules but increases cost and size [34]. Furthermore, a voltage controller can systematically inject specific voltage harmonics in multi-phase systems to even out currents across the individual phases and consequently reduce the load ripple on the module level [30], [35].

Among the various CHB topologies, those with parallel connectivity (e.g., CHB\(^2\) in Figure 1, sometimes also denoted as modular multilevel series/parallel converters, MMSPC) [33], [36], [38] offer better load distribution among battery modules, lower effective source impedance, and lower ripple load, which is a major advantage particularly for battery applications [39]. Paralleling modules instead of bypassing eliminates no-load states and lowers the load of the active modules to bring both closer to the mean [40], [41]. More details on MMSPC operation and topologies are described in the literature [37], [42], [43].

In addition to the averaging effect of paralleling modules within a phase string, MMSPC topologies allow a reduction of the module load ripple through a double neutral point (see Figure 1(b) at the right end), which can parallel modules across the previously widely independent phase module strings [30], [39], [40], [41], [44] [45], [46]. Such dynamical module paralleling across the module strings through this double neutral point can exchange power and improve the load distribution. The load ripple reduction can be an objective of the control algorithm, as will be presented further later on.

### C. RIPPLE-SHUNTING DIELECTRIC CAPACITANCE

During operation, the elements and materials of the battery cells in the reconfigurable battery undergo degradation processes so that the cells gradually lose their capacity and performance [47], [48], [49], [50], [51], [52]. The degradation is a result of many physical and particularly electrochemical processes, also called faradaic processes, connected to...
charging and discharging of the cell. Nevertheless, rippled load does not necessarily lead to faradaic processes. Electrically charged electrodes and the adjacent electrolyte form a charge double layer [53], [54], [55], [56]. Due to the small spacing of relatively large charges, the capacitance of the double layer can be immense. Furthermore, the electrolytes of modern batteries are strongly polar for high lithium-ion solubility, entailing a large dielectric constant as an advantageous side product [57]. Thus, the resulting merely dielectric capacitance can absorb the entire charge of short current pulses without further chemical reactions [58]. In addition, in contrast to the electrochemical capacitance, the dielectric capacitance offers lower impedance and cell heating. The dielectric capacitance is proportional to the active area of the battery cell electrode [58] and remains relatively constant during lifetime, or can even slightly increase [59].

Electrochemical reactions have limited kinetics, often constrained by diffusion, and electrically appear as low-pass system. To initiate sufficient chemical reactions, a current has to be maintained for an extended period of time in the range of milliseconds, supporting the dielectric shunting for short pulses and higher frequencies [60], [61], [62].

Bessman et al. demonstrated that rippled load particularly at higher frequencies can be negligible for ageing [63]. Results reported in previous experiments mainly support their conclusion and suggest the existence of a corner frequency or transition band above which the dielectric charge absorption capability of electrodes dominates and leads to a decrease in battery ageing [64]. Operation in this transition band is necessarily accompanied by a decrease in the cell impedance for the battery ripple. Thus, a reduction of low-frequency content of a battery’s load spectrum is the main aspect for proper treatment of battery cells, which also complies with most recent experiments particularly focusing on MMC load [65].

The method in this paper for the first time solves a major problem of MMCs with batteries and other reconfigurable battery systems, specifically their large low-frequency ripple load, which particularly arises in realistic real-world setups that use bandwidth-limited sensors, control busses, and/or control hardware that introduces latency. The control approach aims to exploit the filtering effect of the dielectric electrode capacitance. The method introduces a battery ripple modulation loop in the scheduling algorithm, which shifts the load ripple toward higher frequencies, where the electrode capacitance can absorb it, reducing loss ageing potential. Considering practical limitations of the monitoring and communication system speed, the control method uses state observers to sufficiently increase the bandwidth of the battery ripple modulation loop.

Section II analyzes the key gap in known control strategies. Section III will introduce our novel method for mitigating low-frequency ripple load for slower ageing potential and less heating loss, which is further analyzed and experimentally validated in Section IV.

II. PREVIOUS CONTROL OF BATTERY-INTEGRATED POWER ELECTRONICS

The high number of individually governable transistors in reconfigurable batteries challenges the control but provides the degrees of freedom to optimize additional objectives, such as active balancing of the module charge [66], [67], [68], [69], [70], [71]. While online-optimizing model-predictive approaches can trade off all degrees of freedom but suffer from the high computational load, phase-shifted carrier control, for instance, is a rather simple way to manage the complexity and can further use the parallel mode to maximize utilization of the modules [37], [41], [45], [46], [72], [73], [74]. Other methods range in between. The majority of the control methods considers only certain useful switch states on the module level to reduce the complexity, such as parallel P, series plus S+, bypass plus B+, series minus S−, and bypass minus B− [36]. The complexity can be further reduced by limiting the options to feasible series–parallel configurations of the whole string of modules, so-called string states S [75].

Whereas state of charge (SoC) or voltage balancing alone may be sufficient for modules with capacitors, batteries behave differently. Battery cells require control of the individual load current’s absolute amplitude and ideally also ripple. A recently presented approach for controlling those expands above multi-objective optimization approaches of module states and includes criteria such as SoC, temperature T, phase current demand i∗, measured phase current i_m, and the previous string state S−1 for the selection of the next string state to comply with the voltage demand v∗, discretized in the voltage modulator to v_d [75].

As outlined in the above-discussed online-optimization literature, different dynamics of typically fast output voltage modulation versus comparably slow discharge rates of batteries appears to justify a separation of the optimization into two parts running on a controller at different speeds to enable online optimization but reduce computational effort: A fast, strictly real-time loop of the controller selects optimal module-string states S_o from an optimized statelist provided by a slower loop with more time for the computational optimization and no need to face deadlines associated with the fast real-time part (see Figure 2).

The optimal string states are selected with respect to state of charge weighted by estimated module current load J, where the calculated string state cost (SC) may optionally further include a ripple reduction term J_k scaled by a weight factor w [75], as

\[
SC (S) = \sum_{k=1}^{N} J_k (S) (S_oC_k - S_oC_{mean}) + w J_k^2 (s).
\]  

Whereas the load distribution is partly reflected in the string state selection, the actual waveform of the load remains uncontrolled. Specht et al. suggest updating the content of the optimized list of states once every second [75], which leaves the content constant during the update period and introduces persistent and regular switching patterns that get
translated to low-frequency and even sub-harmonic ripple content in the module load (see the measurement data in Figure 10a). Any imbalance of controlled values results in either extensive utilization or mitigation of the module load in the switching pattern. Thus, these low-frequency patterns are a result of the interaction of various control objectives and the reality of limited control bandwidth and feedback speed. Formation of temporal patterns can be especially harmful, when reaching the millisecond range as outlined above for the faradaic dynamics. Increasing the update rate is limited by relying on slow acquisition of module information, which is often collected through data communication busses with considerable latency [76], [77], [78], [79], [80]. The communication bus latency in addition to signal processing can readily reach 10 – 100 ms, while the switching rate of the phase voltage period is in the microsecond range. The other existing solutions struggle (and fail) in view of one fundamental trade-off: the need for lab-grade low-latency sensors, a fast direct, bus-less connection of all sensors as well as gate signals, and high-performance embedded control for rapid scheduling as described, for instance, in Li et al. [73] clashes with the conditions in more realistic larger systems as used in commercial set-ups. In commercial systems, a larger number of modules is typically connected to a more economic off-the-shelf controller via a communication bus, more affordable industry-grade sensors provide slower and lower-bandwidth data, and off-the-shelf economic processing power introduces bottle necks as described in Specht et al. [75], Rietmann et al. [81], and Hao et al. [77].

III. PROPOSED CONTROL APPROACH

To achieve optimal battery treatment, the load distribution and the ripple modulation become the major objectives of our scheduling algorithm, constrained by the voltage demand of the modulator so that the phase current remains unaffected. The scheduler relies on two major components, a strictly real-time-compliant state selection as well as the high-bandwidth but asynchronous and not strictly real-time state optimization. The latter writes information into look-up table, which the former reads, enabling concurrent operation. The state optimizer comprises a set of ripple modulators, one assigned to each module, an optimization routine for the selection of optimal module-string states, and a battery-ripple observer, which closes the control loop. Instead of waiting for slow measurement data, the battery-ripple observer rapidly delivers information for control and is the core element that enables the high bandwidth.

Figure 3 outlines the complete control loop of the scheduler together with a phase-current controller and a voltage modulator. Our control scheduling algorithm is widely independent and therefore works with any voltage and current controller; so the following will treat them as given and refers to the literature for such controllers [82]. Similarly, the battery-management-system (BMS) block typically acquires battery module data relatively slowly and adjusts the individual current demands and limitations of each battery module as established in the prior art [83].

More importantly, our algorithm aims for a maximization of the bandwidth, which reduces artefactual patterns in switching and reduces loss as well as battery ageing potential associated with low-frequency load ripple. Efficient suppression of switching patterns follows from matching the module control loop and the phase control loop in speed. Therefore, in contrast to previous suggestions in the literature [75], all blocks of the ripple modulator preferably run within a switching period of the phase control loop. Faster execution of the control loop is achieved by pre-calculation of repetitive routines and storing their results in look-up tables (LUTs). The look-up tables are stored in fast block RAM memory of the FPGA, which minimizes latencies and further boosts the speed of the control loop. Reading from the block RAM can be achieved in a single clock cycle, whereas the result of the matrix operation requires $N \times 3–5$ cycles, where $N$ denotes the number of modules (5 modules in the experimental demonstration below, so using LUTs results
in 15–25 times faster execution of the algorithm than regular solving of matrices).

Nevertheless, the ripple modulator loop still has a fundamentally asynchronous design and is not strictly time-critical so that any delay in execution does not halt control but might only introduce a short artefactual switching pattern and small ripple with length respective to the delay. Indeed, any loop execution time shorter than the period of the phase load helps decreasing the low-frequency ripple content.

Further, the ripple-modulator loop aims for only the temporal shape of the module load, which allows for operation with proportional units, and independently controls the module discharge rate and the ripple modulation. In principle, the discharge rates define a set of string states, i.e., what has to be done—the ripple modulator controls their time sequence, i.e., when and how this is done on the microscale. Therefore, voltage and SoC balancing capability of the proposed method does not degrade in contrast to Specht et al.

### A. BATTERY RIPPLE MODULATOR

The battery-ripple modulator, e.g., implemented with a PI controller as here, guarantees discharging and charging of the modules at the demanded rate \( I^* \) and provides an interface for any higher-level entity that balances the SoC and for any BMS functionality. The use of proportional units in the demanded discharge rate reference \( I^* \) distributing the load between the modules ignores one degree of freedom, i.e., scaling, and solves eventual contradictions with the phase-current demand \( i^* \).

The modulator needs to implement a controller with highly integrational character, also known as reset controller, which brings a controlled variable close to the demanded value. The requirement follows from the distinct distribution \( J_m \) of the phase load \( i_m \) among modules in each string state \( S_0 \), which does not necessarily allow the demanded current distribution in each step (see Figure 4). The integrated value of the battery ripple \( J^* \) is passed to the optimization routine, which modulates an appropriate sequence of string states and provides the demand on average while controlling the battery ripple.

### B. BATTERY RIPPLE OBSERVER

The ripple-modulator loop requires considerably fast feedback to run at maximum speed. An acquisition of the module current and transmission of the measured value to the controller represents either unacceptable propagation delay and/or heavy load of a data bus [23].\cite{75, 77, 80}, [81].

The typical period of the data acquisition is on the order of milliseconds, which is comparable to the load frequency and may not be sufficient for proper control of the module load frequency. Our modulator architecture solves the slacking feedback using an observation technique. The observation technique needs to sufficiently approximate the module load but primarily provide minimal delay. We further derive a simplified observation technique with aforementioned qualities.

The actual current load \( I_{bk} \) of module \( k \) is a result of the phase string state (series–parallel configuration of modules), current load of the phase \( I_L \), and voltage \( V_B \) as well as impedance ratios of modules \( R_B \) vs. their interconnection paths \( R_S \) (\( R_{LS} \) designates resistance of the low-side and \( R_{HS} \) designates resistance of the high-side interconnection) [7]. In principle, the string configuration comprises a set of parallel groups, where each parallel group forms one level of the output voltage and is loaded by the phase current. Equation set

\[
\begin{bmatrix}
R_{D1} & R_{U2} & 0 & 0 & 0 \\
R_{L1} & R_{D2} & R_{U3} & 0 & 0 \\
R_{L2} & R_{L2} & R_{D3} & R_{U4} & 0 \\
R_{L3} & R_{L3} & R_{L3} & R_{D4} & R_{U5} \\
1 & 1 & 1 & 1 & 1
\end{bmatrix}
\begin{bmatrix}
i_h1 \\
i_h2 \\
i_h3 \\
i_h4 \\
i_h5
\end{bmatrix}
= \begin{bmatrix} B_1 \\ B_2 \\ B_3 \\ B_4 \\ I_L \end{bmatrix},
\]

where

\[
\begin{align*}
R_{Dk} &= -(R_{bk} + R_{LSk} + R_{HSk}) \\
R_{Lk} &= -(R_{HSk} + R_{LSk}) \\
R_{Uk} &= R_{bk} \\
B_k &= V_{bk+1} - V_{bk} - R_{LSk} I_L
\end{align*}
\]

(2)
governs further distribution of the phase current among paralleled modules, where the dimension of the problem is equal to the number of parallel modules, and subscript \( k \) designates the index of the module in the phase string.

Considering constant values of all resistances allows precalculation of the impedance matrix and significantly simplifies the algorithm complexity solving (2). The current distribution is then reduced to a function of module voltage differences, which are—through the effort of the controller—kept minimal and change only slowly over time, dependent on the battery capacity. Under the assumption of relatively constant module voltages within the relevant periods, the whole problem can be further simplified to a look-up table where the observer pre-estimates the expected module current distribution of each feasible string state in the look-up table. Values in the look-up table may occasionally update once the governing quantities noticeably change. However, also an entirely constant look-up table can temporally approximate the module load and sufficiently substitutes missing feedback within the acquisition period (see Figure 5).

In the simplest embodiment of the module ripple observer in Figure 5, the values in the look-up table correspond to the ideal share of the load across paralleled modules for each output state \( S_0 \). In fact, operating conditions of the system are usually not too far to meet the ideal share per module. First,
balance of modules is an objective of the system controller, and a properly controlled system guarantees voltage balance. Second, the resistance ratio between electronic switches and battery cells typically stays high enough to keep the error on the order of few percent. In addition, the cumulative error of the ideal current share estimation is further compensated through symmetrical alternation of phase string configurations for the positive and negative half-period of the output voltage. Alternatively, any higher-level entity may ultimately cancel the error by projection of the error onto the modulator reference of the module load.

We further demonstrate an example of the observation technique on a particular string configuration in Figure 6. The figure displays the resultant configuration of the examined converter string state $s$, which corresponds to the state of the individual modules per

$$s = \{ P, P, S_+, P, S_+ \}. \quad (3)$$

The string state $s$ connects modules such that Modules 1 to 3 form a first and Modules 4 and 5 a second parallel group (where $P$ denotes parallel connection, and $S_+$ denotes series connection of neighboring modules). The last element of the state vector controls the output terminals of the string. Since none of the groups of state $s$ bypasses the load, the vector of relative distribution $J_m$ can be approximated by the inverse of the number of modules in each parallel group by

$$J_m(s) = (0.3, 0.3, 0.3, 0.5, 0.5). \quad (4)$$

The current distribution is multiplied by the signum of the actual phase current and provided to the output of the observer block $J_m(s)$ at every occurrence of the string state $s$. Similarly, the look-up table of the battery-ripple observer defines distribution $J_m$ for each feasible string state. The implementation outlined in Figure 5 significantly reduces the real-time computational burden through the pre-calculated look-up tables and allows for fast and efficient execution of the control loop.

Thus, even a very simple implementation of the model neglecting any disturbance of the current distribution and therefore moderate accuracy can very effectively suppress low-frequency ripple on the batteries as our experimental measurement demonstrates.

### C. STATE OPTIMIZATION

The optimization routine also deals with the special setting in case of additional parallel connectivity. The selection of the optimal state is subject to individual demands of the battery-ripple modulator $J^*$. While topologies without parallel state can easily handle the controller demands by sorting algorithms and prioritized active/inactive states for modules with high/low regulator demand, topologies with parallel state need to deal with an increased number of feasible string states to exploit the full additional potential. To equally distribute the phase load, the majority of modules preferably stay in the active state and rather control their contribution to the phase current by appropriate clustering in parallel groups. Similar to the battery-ripple observer, all string states in the optimization block are represented by the current distribution (in a look-up table). The optimization routine selects one state $S_0$ with optimal current distribution $J_{k,m}$ respecting the demand of the module current controllers $J^*$.

Our algorithm uses a typical least-square criterion of optimality to evaluate each state per

$$SC(S) = \sum_{i=1}^{N} \left( J^* - J_{k,m}(S) \right)^2. \quad (5)$$

The least-squares criterion guarantees sufficient effort to meet the regulator demands and simultaneously reduces conduction losses by preventing states with far outlying load distribution (e.g., excessive use of bypassing). Results of the evaluation of each feasible state are stored in a look-up table, which interfaces and decouples the ripple modulator loop and the strictly real-time phase-current control loop as outlined above (see Figure 7).

To achieve a sufficient speed of the optimization routine, we constrain transitions between consecutive string configurations by limiting the number of switches that can toggle in each step. In other words, to increase the phase voltage only one parallel (or bypass) connection of the previous state changes and is switched to a series connection; and to decrease the phase voltage only one series connection of the actual state is switched to parallel (or bypass). Besides reducing the list of feasible state candidates $S_f$ (saved in a look-up table and chosen with respect to the voltage demand and present output state $S_0^{-1}$), this rule also limits the number of commuting switches and consequently reduces switching losses.

### D. BANDWIDTH ANALYSIS

A high bandwidth of the control algorithm is essential for appropriate modulation of the module ripple and can be
exploited by tuning it to the control-loop transfer function. The control loop is displayed in Figure 8 and further highlighted in Figure 10 (in light blue). It consists of the unity transfer function of the state optimization ① (simplified with an approach similar to conventional inverters [84]), the time delay of the ripple observer $T_d$ with unity gain ② (observed and controlled quantities have the same units), and the ripple modulator ③ (conventional proportional–integral controller) transfer function per

$$L(s) = \frac{1}{s} \frac{e^{-Ts}}{K_p + K_i/s}. \quad (6)$$

Tuning the proportional–integral (PI) controller (6) with proportional gain $K_p$ and integral constant $K_i$ with respect to the typical demands on phase margin $PM = 40^\circ$ and gain margin $GM = 3$ dB allows for the calculation of the controller parameters and bandwidth of the control loop for characteristic time delay. The delay of the reference method is given by the acquisition time $T_{d,ref} = 100$ ms, whereas the ripple observer can provide feedback in the very next period of a switching. The delay amounts to $T_{d,prop} = 0.05$ ms assuming switching period of 20 kHz. The huge difference in the delay time between the reference and the proposed method yields an increase of the bandwidth by approximately a factor of 1000, which correlates with proportions between the delay times (see Table 1).

![FIGURE 7. Schema of the optimization routine selecting the most appropriate output state $S_0$ out of feasible state candidates $S_i$ with respect to the demand of the ripple modulator $J^*$. The current distribution of each available state is evaluated to comply with the demand $J^*$. The optimization routine uses a look-up table to improve the execution time of the algorithm. The figure displays example values under each signal line (we show two alternative candidates $s$, $s'$).](image1)

### TABLE 1. Bandwidth estimation.

| Method            | $K_p$ | $K_i$ | Bandwidth |
|-------------------|-------|-------|-----------|
| Reference ($T_d = 100$ ms) | 14    | 14694 | 2 Hz      |
| Proposed ($T_d = 0.05$ ms) | 0.48  | 12    | 3800 Hz   |

![FIGURE 8. Small-signal model of the ripple-modulator loop.](image2)

### IV. EXPERIMENTAL RESULTS

#### A. SETUP AND PROCEDURE

We built a single-phase laboratory test setup for experimental evaluation and prepared two control methods: the presented one and as a reference from the state of the art the method of [75]. The aim of the demonstration is to illustrate the effect of the fast feedback and control loop in preventing fixed switching patterns for long intervals.

The test setup comprises five MMSPC modules (see Figure 9) with the CHB$^2$ topology presented in Figure 1. Each module uses two parallel silicon field-effect transistors (100 V, 1.5 mΩ, IAUT300N10S5N015, Infineon) per logical switch, and ceramic capacitors with a total nominal capacitance of 490 µF (the capacity effectively drops with increasing voltage as in most ceramic capacitors) on the dc bus. The capacity of the laboratory module board is primarily designed for commutation of 200 A within 1 µs with allowed voltage drop of 1 V. The dc bus of each module contains a six-cell LiFePO4 battery (22.5 V, 6s, 6.2 Ah, Zippy compact).

![FIGURE 9. String of five CHB$^2$ modules forming the laboratory setup.](image3)

The system controller uses a Mars ZZ3 module (Enclustra) with Xilinx’s Zynq-7020 system-on-chip. The control algorithm runs fully on the FPGA part. The setup implements a sigma–delta modulator running at 20 kHz.

The implementation of the proposed control method follows the structure given in Figure 10, where the scheduler aims at equal utilization of the battery modules and an observer estimates the module load based on state and overall load information within the cycle time of the control loop. The method of Specht et al. (see Figure 2), which represents conventional methods that collect module information with a
FIGURE 10. Block diagram of the control algorithm adapted for sensorless operation and open-loop control. The ripple-modulator loop (light blue) works directly with current distribution $J_m$ without the need for scaling it with the phase-current magnitude. The demand of the ripple modulator considers an equal distribution of load and is calculated from the discrete phase-voltage demand divided by the total number of modules $N$. The ripple modulator uses an integrator to cumulate any disturbances from the demanded load distribution. The cumulated value is used in the optimizer, which evaluates all states according to given criteria and assigns their cost SC in the state cost table. The phase-voltage loop independently selects feasible states according to the demanded voltage and finds the state with minimal cost function, which most effectively compensates cumulated load disturbances. The load distribution of the state is observed, fed back, and cumulated in the ripple modulator.

TABLE 2. Experimental load.

| Load parameter      | Value   |
|---------------------|---------|
| Module power        | 240 W   |
| Modulation index    | 30 – 100 % |
| Load frequency      | 50 Hz   |
| Switching range     | 20 kHz  |

limited rate due to physical issues such as sensor data processing and data busses, serves as a reference [75]. It delivers measured module load data at an update rate of $\sim 10$ Hz with an execution cycle time at 100 ms for the measurement loop, which in turn leads to slacking in the feedback and which we implemented accordingly.

We perform the measurement at various output voltages, resp. modulation indices ranging from 30 % up to 100 % with adjustable resistive load and a small inductance to ensure hard switching conditions for the electronics. We adjust the load to maintain the power per module under all conditions at 240 W, which corresponds to an average module dc-side current of 10 A ($\sim 1.5$ C rate) (see Table 2, Figure 11). We recharge the batteries before every experimental condition, such as different phase voltages, to 75 % SoC and perform a few calibration measurements. The experimental measurements follow the calibration, where the first and the last measurements are compared to ensure repeatability. Each measurement provides a window for monitoring the open-circuit voltage before and after applying the load (see Figure 12).

FIGURE 11. Experimental current (blue curve, 20 A/div) and terminal voltage (red curve, 20 V/div) of the eleven-level MMSPC phase string measured at $m = 0.7, I_{pk} = 25$ A.

B. RESULTS

Figure 11 displays the output current (blue curve) and the output voltage (red curve) of the system, while Figure 13 presents the module current comparison between the proposed method (red curve) with high bandwidth and the reference method (blue curve) from the literature. The slacking feedback of the reference method is noticeable in the module current as it results in artifactual load patterns (see Figure 13a).

These artifacts obviously form intervals that correspond to the cycle time of the feedback loop around 100 ms. The output
states (and consequently the load distribution) do hardly vary within such an interval, and their repetition generates a regular pattern in the module current provided by the batteries. The patterns may change with every update of the feedback values, and so does the character of the load artifacts. The artifacts can, as captured in the recording (Figure 13a), largely vary in amplitude, and cover the entire range from full phase current to practically no battery current in a module at all. These large variations increase the root-mean square current even for the same average. In between these two extremes, the frequency content may differ from relatively continuous switching to intensive switching bursts.

In stark contrast to this established method from the literature, the proposed control allows full utilization of the switching rate and evenly distributes the switching events in time (see Figure 13b). As intended, the distribution of the switching prevents extensive utilization of individual modules and naturally reduces the low frequency content. Yet, the module load can contain some minor residual switching patterns, which we found to be mostly emerging in case of long propagation delay. As long as the period length of the pattern stays negligible compared to the phase frequency of 50 Hz, however, the control method efficiently suppresses low-frequency content through distributed switching.

The impact of the proposed control method on the module current is more obvious in the frequency domain (see Figure 14). The spectrum of the reference method’s module current exhibits dominant peaks at twice the phase load frequency ($f = 2 \times 50 \text{ Hz} = 100 \text{ Hz}$). Further peaks can be observed at 5 Hz, which repeats at 10 Hz, 15 Hz, etc. These peaks follow from the update period of 100 ms and the patterns in the module load. The reference method displays relatively low content at frequencies above 100 Hz, which rises again around the switching frequency.

In contrast to the prior art, the frequency content of our proposed method is practically negligible for low frequencies, just starts at 100 Hz, and features increased content up to a fraction of the switching frequency. The reduction of lower frequencies and the partial shift to higher ones is a result of appropriate switching distribution and prevention of pattern formation. Depending on the modulation index, the ripple is shifted to a region corresponding to a fraction of the switching frequency. The 5 kHz results from equal distribution of the effective converter switching $f = 20 \text{ kHz}$ among five modules, leading to roughly 5 kHz switching load per module.

Despite a rather simple embodiment of the observation technique and no SoC or voltage feedback loop, the discharge rates of both methods exhibit minimal differences between
modules. Oscillograms of the module current (see Figure 12) reveal that the reference method keeps the average error of removed charge under 5%, and the proposed method reports an error of less than 2% throughout the whole modulation index range.

C. EFFECTIVE IMPEDANCE REDUCTION THROUGH NONFARADAIC SHUNTING

Low-frequency ripple contains larger charge quantities, generates losses, and can age batteries either through the associated heating stress or potentially also electrochemical degradation [58]. Above a certain frequency, however, the impedance of battery cells drops steeper (closer to a dielectrically capacitive $f^{-1}$) than the diffusion-limited $f^{-1/2}$ behavior of faradaic reactions until at very high frequencies the inductance sets a minimum [85]. At such high frequencies, not only the losses decrease but also faradaic processes cease as they cannot follow those charge oscillations anymore; the detected reduction in ageing potential at higher frequencies concurs with this effect [63]. Impedance spectroscopy indicates the transition from faradaic processes, i.e., electrochemical charge-transfer reactions, as the key source of the currents to the dielectric electrode capacitance for most cells above 100 Hz – 1 kHz.

This behavior can be represented with a small-signal approximation of the widely used Randles’ equivalent circuit for the electrochemical interface (see inset of Figure 15) [86]. With increasing frequency, the dielectric electrode capacitance bypasses the slow diffusion-limited charge-transfer processes, reducing loss. Consequently, the proposed control method should lead to lower losses.

To quantify the losses, we further process module voltage and current measurement during the load tests under various modulation indices specified in Table 2 (see results in Figure 16). Each load test lasts 30 seconds and provides no-load windows before and after for monitoring internal voltages as Figure 12 outlines. First, we extracted the value of the internal voltage $V_i$ with a delay of 15 seconds after the load reaches 0 A (for voltage settling). If we only consider processing a short time window of the preceding load test $T_w$, the power loss can be calculated per

$$P_{\text{loss}} = \frac{1}{T_w} \int_{T_w}^{T_e} (V_i - v_m(t)) i_m(t)$$  \hspace{1cm} (7)
V. CONCLUSION

This paper presents a novel control method for modular multilevel converters with integrated batteries, which suffer from substantial ripple load on the batteries and associated additional heating as well as degradation. The method aims for battery applications and their specific need for better battery treatment. Based on previous observations that the impedance of the battery cells as well as the ageing potential tend to decrease with frequency, since higher frequencies are absorbed by the dielectric electrode capacitance.

In conventional methods, the limited speed and nonnegligible latency of sensor data collection from the individual modules in addition to often slow update rates of scheduling tables typically generate regular patterns in the module load. Accordingly, also module-balancing loops of the state of the art have to adjust their bandwidth to these conditions to avoid instability and driving oscillations. To solve this issue, we developed a battery-ripple observer, which allows us to create a fast feedback loop despite unavoidable latencies so that our control algorithm can actively modulate the module ripple and operate with comparably high bandwidth. We designed a control algorithm to minimize particularly low-frequency content of the module load spectrum.

We evaluated our novel control technique experimentally and compared it to the state of the art. Due to above-mentioned limitations, the conventional method from the literature indeed produced fluctuating module load below 100 Hz and even below 10 Hz, which corresponds to the module data acquisition period, latencies, and bandwidth limits of the feedback, whereas our proposed method could prevent the formation of harmonics in this frequency range and shift fluctuations to the band around 5 kHz. Consequently, our control approach does effectively exploit lowered impedance at higher frequencies and reduces losses in the battery modules by up to 20%.

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