High throughput and variable temperature superconductor integrated circuit test and evaluation using ICE-T

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Abstract. Superconductor digital integrated circuits (ICs) require rapid evaluation of multiple copies to obtain statistical operational data. These data are used for assessing model-to-hardware correlation and facilitate iterative IC design development. The Integrated Cryogenic Electronics Testbed (ICE-T) is a cryogen-free test platform, which can test multiple chips simultaneously with similar convenience to a liquid-helium immersion probe and with cooldown times of between 3.3 to 4.5 hours. We have developed a three-chip insert to increase the volume of chip testing and demonstrated simultaneous cooling of six chips with two such inserts. We report the test statistics collected from 27 chips across a single wafer. We have also used the ICE-T’s convenient temperature control system to evaluate chips in the 3.5 - 6 K range. Such evaluation determines the robustness of circuit design and its tolerance to critical current fluctuations due to fabrication variation.

1. Introduction
As superconductor electronics mature from research prototype to productization, testing and characterizing a large volume of superconductor integrated circuits (ICs) over a short period of time (high throughput testing) becomes a must. One major barrier in testing, development, and use of superconductor electronics is the cost and availability of liquid helium to cool down these devices and ICs to the required temperature. Traditionally, liquid helium cryostats have allowed researchers to quickly cool down and test these ICs using immersion probes [1]. However, refilling these cryostats and maintaining a liquid helium test facility contribute significantly to operational cost. Worldwide shortage of liquid helium, irregular supplies, and multifold price increases have been disrupting the operations of research labs in recent years [2]. Additionally, since most of these cryostats require frequent re-filling of liquid helium, they are difficult to use for long term continuous testing.

Cryocooled systems have been around for a while as an alternative to the liquid helium testing paradigm. However, they have suffered from their own drawbacks. These cryocooled systems have been designed and constructed to be rather experiment-specific. Since the configuration of the external interface varies between different devices and circuits, in terms of number of connections and their type (input vs output vs data), the user is required to spend significant time and effort to reconfigure the system which also requires an expertise in cryo-packaging. Even something as simple as switching out a chip and replacing it with a substitute of the exact same type requires the user to have extensive training in cryo-packaging and would require a day or two of the user’s time [3].

To address these problems, we developed the Integrated Cryogenic Electronics Testbed (ICE-T) [4], a cryogen free testbed to do cost-effective high throughput testing and eliminate the need of cryo-
packaging for the end-user. ICE-T was designed with interchangeable top loading inserts, which house all the experiment specific cabling and cryo-packaging. This provides a user convenience similar to that of liquid helium immersion probes. At the same time, electricity and periodic maintenance are the only cost of running ICE-T, and these costs are rather low compared to the cost of liquid helium in a traditional setting [4]. The modularity and flexibility of ICE-T, as well as its fast cooldown and warmup time, make the ICE-T the preferred testing platform for superconducting ICs. This is especially true in an R&D environment where the ability to test chips of different designs quickly is a priority.

The ability to test multiple chips quickly and seamlessly is important at each phase of R&D work. In the screening phase this ability allows testers to quickly characterize the wafer and exclude poorly performing chips. In the iterative phase of IC design such an ability helps facilitate model-to-hardware correlation. And in the final phase of the design cycle the user can measure the robustness and tolerance of a design to variations in the fabrication process.

For a foundry, a testbed with the capacity for high throughput testing can be extremely valuable, as it enables the quick collection of full statistics on several fabricated wafers. This capacity allows for a robust analysis of fabrication parameters such as critical current density ($J_C$), critical current ($I_C$), missing area, wafer yield, etc.

Another significant advantage of ICE-T is its inbuilt temperature control system which allows a user to vary the testing temperature in a controlled manner; something which is extremely difficult to implement in liquid helium cryostats. This enables measurements of superconductor ICs, cryogenic semiconductor circuits, or a combination of both at different user-controlled temperatures. By varying the temperature during measurement one can thermally tune the critical current of superconductor circuits, which can be very useful for analyzing a circuit’s behavior at different critical currents of the Josephson junctions (JJ) [4] [5].

2. Description of the Testbed

ICE-T is designed with seats for two interchangeable inserts which make thermal contact to the cold-head’s two native temperature stages via a clamping mechanism. Each seat uses an ISO-100 vacuum port, which accommodates a cylindrical insert ~4" in outer diameter and extending ~19" inside the vacuum chamber. Both the inserts and the body of ICE-T have thermometers and heaters located at each stage. The placement of these in the system can be seen in figure 1. The thermometer and heater at the 2nd stage of the insert, together with the temperature controller, serve as a temperature regulator for variable temperature measurements. They also enable rapid (under 5 minutes) de-fluxing of superconductor ICs [6]. As ICE-T can accommodate two inserts for two independent experiments, and each insert has its own heaters, chip(s) in each insert can be de-fluxed independently.

![Figure 1. CAD drawing of ICE-T with the inside of the vacuum chamber visible.](image-url)
2.1. Standard ICE-T Insert Design

ICE-T’s modular design allows for many types of inserts customized to fit specific experimental requirements; each of which can be swapped out in minutes without having to open and reconfigure the entire testbed. For the testing presented in this paper we used some of the inserts that come as a standard option with the ICE-T. These standard inserts are designed to take either a 5x5 mm$^2$ or 10x10 mm$^2$ chip using a standardized pad layout; this accommodates the testing of a wide variety of different superconducting IC designs. The superconductor chips are pressure mounted in the sample holder of standard inserts the same way as in traditional helium-immersion probes [1].

One type of standard insert is what we call a “universal insert”, as all the lines running from the room temperature connector panel to the chip are identical and can handle any frequency from DC to 26.5 GHz with < 2 dB loss, allowing the chip designer/tester to use any line for either input, output or bias [7]. The universal insert comes with the option of either 40 or 80 high frequency (HF) lines. The universal inserts and their vacuum flanges can be seen in figure 2(a) and figure 2(d) respectively. The benefit of these two inserts is the ability to test any chip matching the standardized pad layout, independent of the number of high or low speed lines the chip requires. This provides the greatest flexibility in designing and testing all chips with a 40-pad or 80-pad layout.

The other standard insert option is our 3×40 insert designed for low frequency (LF) basic functionality level testing of superconductor ICs. The insert, as shown in figure 2(b) with its vacuum flange shown in figure 2(c), is capable of supporting three chips simultaneously with 40 low speed lines running to each chip. The benefit of the 3-chip insert is a much higher throughput of testing. When loading two inserts the design allows a user to cool down a total of 6 chips simultaneously.

2.2. ICE-T Cooldown and Warmup Time

For a cryocooler based testbed, the testing cycle includes the cooldown time to the required temperature, the chip test time, and the warmup time to room temperature. For high throughput testing of superconductor ICs it is very important that the cooldown time and warmup time are acceptably low. For reference, Table 1 shows the cooldown and warmup times for ICE-T’s standard inserts. As ICE-T can accommodate up to two inserts we show how long it takes to cool down one or two inserts at the same time as separate entries. The time was measured in HYPRES’s ICE-T development unit. The number of chips per insert which can be cooled down simultaneously are shown too. For example, cooling down 6 chips in two 3×40 LF line inserts, will take 3.7 hours. Similarly, it would take 4.5 hours to cool down 2 chips in two 80 HF line universal inserts. The warmup time is only 2.5 hours for any combination of inserts when HYPRES’s proprietary heating method for accelerated warmup is used.
Table 1. Cooldown and warmup times for standard ICE-T inserts.

| Insert Type                        | # of Inserts | # of ICs | Cooldown\(^a\) Time to 4.2 K (Hrs) | Warmup\(^b\) Time to 293 K (Hrs) |
|------------------------------------|--------------|----------|-----------------------------------|----------------------------------|
| 3 x 40 LF Line (High Throughput)   | 1            | 3        | 3.3                               | 2.5                              |
| Insert                             | 2            | 6        |                                    |                                  |
| 40 HF Line Universal Insert        | 1            | 1        | 3.7                               |                                  |
|                                    | 2            | 2        |                                    |                                  |
| 80 HF Line Universal Insert        | 1            | 1        | 4.0                               |                                  |
|                                    | 2            | 2        |                                    |                                  |

\(^a\) As measured in HYPRES’s test lab unit
\(^b\) Using HYPRES’s propriety heating system

3. Novel Testing Methods Using ICE-T

In this section we present the results of several experimental studies of superconductor circuits that are made possible only by the versatility, customizability, and modularity of the HYPRES ICE-T.

3.1. High Throughput Testing

The flexibility and ease of swapping a chip in an immersion probe and the speed of cooldown and warmup are often cited by researchers as reasons to use traditional liquid helium test setups. This is particularly true in an R&D environment, despite the increasing cost of liquid helium and the cost to build and maintain the liquid helium infrastructure. When compared to traditional cryocooled systems, which are highly specific to a narrow set of chips and require cryopackaging expertise and extensive labor to dismantle much of the system to access or swap a chip, the argument for traditional liquid helium testing in an R&D environment seems reasonable. ICE-T, however, has become a game changer in the liquid helium vs. cryocooled system debate. The ease of loading multiple chips into ICE-T inserts and speed of cooldown and warmup as mentioned in Table 1, eliminated the main disadvantages of cryocooled systems vs liquid helium thermostats and enabled ICE-T to test chips at higher throughput without requiring cryopackaging expertise on the user’s side.

High throughput testing is an important step in design certification as it measures the tolerance of a design to several fabrication parameters and wafer runs. In this experiment we tested 27 chips from various locations of the same wafer at 4 K. The chips were tested in the ICE-T with two 3×40 LF line inserts, as seen in figure 2(b). This setup allowed us to cool down 6 chips simultaneously, test them and warm up in one extended 10-12 hour workday; providing sufficient time to swap the chips and cooldown overnight for testing the following day. At this pace we were able to test all 27 chips available over 5 extended workdays, in a total of 60 man-hours.

Each chip, as shown in figure 3, contains a set of 3-to-2 and 7-to-3 parallel counters [8] whose operating circuit bias margins were measured for functional level testing at low frequency (< 1 kHz) using the Octopux automated test system [9]. Test patterns were randomly generated at each bias point to measure the margins. The margin is the range of DC bias currents at which the circuit operates as designed and is characterized by the minimum and maximum bias current values as well as the center point.
Wider operating margins indicate potential higher frequency operation and better performance, thus signifying a better IC design and/or better fabrication quality. When some chips of a particular design have wider operating margins than other chips of the same design, it indicates a higher fabrication quality of the wafer or of an area of the wafer.

Table 2 shows the average bias center in millivolts (mV) and bias margins which were calculated from measuring 27 chips, all from the same SFQ584-17-1-W3 wafer fabricated at MIT-LL [10] [11] [12]. The margins and values of both circuits’ key biases were measured and analyzed. Critical bias margin is the lowest bias margin of all the biases. As seen from Table 2, logic bias is the critical bias for both circuits.

The spread and variation of critical margin of both circuits are shown in figure 4. The wafer location map is shown as provided by the MIT-LL foundry. From testing twenty-four 3-to-2 parallel counter we found that the average margin of all the biases was greater than ±20%. Having comparatively wide and uniform operating margins indicates that this design is very robust and tolerant to fabrication variation across the wafer. However, when testing the twenty-seven 7-to-3 parallel counters we found that the logic bias had a suppressed average margin of less than ±10% as compared to the others with greater than ±20%. Pre-layout simulations predicted more than a ±20% for all biases. A consistent suppression of the logic bias across the entire wafer indicates a mismatch between the simulation and post-fabrication parameters.

Table 2. Cooldown and warmup times for standard ICE-T inserts.

| Circuit Name       | # of Circuits Tested | Bias Name | Average Bias Center (mV) | Standard Deviation of Bias Center (mV) | Average ±% Margin |
|--------------------|----------------------|-----------|--------------------------|----------------------------------------|-------------------|
| 3-to-2 Parallel Counter | 24                  | Data      | 2.40                     | 0.08                                   | 36%               |
|                     |                      | Clock     | 2.02                     | 0.08                                   | 33%               |
|                     |                      | Logic     | 2.29                     | 0.07                                   | 25%               |
| 7-to-3 Parallel Counter | 27                  | Data      | 2.63                     | 0.10                                   | 24%               |
|                     |                      | Clock     | 2.26                     | 0.09                                   | 30%               |
|                     |                      | Logic     | 2.03                     | 0.08                                   | 9%                |

Figure 3. Layout of chip with 7-to-3 parallel counter and 3-to-2 parallel counter circuits.
Figure 4. Performance of circuit as a function of critical margin across the wafer. The upper half of each circle represents the critical margin for the 7-to-3 parallel counter on the chip at that location; while lower half represents the critical margin for the 3-to-2 parallel counter circuit on the chip at that location. Different patterns for different critical margins are shown in table on left.

3.2. Variable Temperature Testing

Liquid helium (4He) environments restrict a chip's operating temperature to 4.2 K. Even though measuring superconductor IC above 4.2 K is possible in liquid helium immersion probes, such measurements are difficult and imprecise because controlling the temperature of the chip in helium vapor is difficult. ICE-T, being a cryocooled system with integrated native heaters at two temperature stages, provides complete control over the temperature environment. By varying the temperature, the critical currents of all the JJs on a chip can be adjusted for optimal circuit performance.

Figure 5. Operating bias margins of a 7-to-3 parallel counter as a function of temperature from a (a) 10 kA/cm² wafer and (b) 20 kA/cm² wafer fabricated at MIT Lincoln Laboratory.

Figure 5(a) and 5(b) show the result of varying the temperature of the superconductor chips from two different wafers. The chip design is same as shown in figure 3 with each chip containing a set of 3-to-2 and 7-to-3 parallel counters [8]. The operating bias margins were measured using the Octopux automated test system in the same way as described in the previous experiment. These margins were measured for all circuit biases at different temperatures, ranging from 3.5 K to 5.4 K. Each bias is plotted with its center point and the bias range. Each bin in figure 5(a) and 5(b) is the operating temperature of the chip and the critical bias margin is mentioned below the bias margins at that temperature.
The designs of the chips are normally optimized for the best IC performance at 4.2 K. However, some chips have better performance at a different temperature which can be due to either imperfect simulations at the design stage or fabrication process variations. As the temperature is raised from 3.5 K to 5.2 K, the critical margin increases from ±9 % at 3.6 K to ±16 % at 5.2 K and ±5% at 3.5 K to ±12% at 4.8 K for the chip in figure 5(a) and figure 5(b) respectively. The margins then start decreasing above 5.2 K and both chips stop working above 5.4 K. By increasing the temperature we are lowering the critical current of the all the JJs. This indicates a mismatch in the designed critical current and the fabricated critical current.

Similarly, a temperature vs bias margin plot is shown in figure 6 for a 256-bit long shift register with six different biases. The chip was tested in ICE-T from 3.3 – 6.0 K. The bias margin was measured in Octopux automated test setup [9]. The critical bias margin is above 15% in the 3.3 – 5.5 K temperature range and the chip works all the way to 6.0 K. This shows that the design is very robust and has a high tolerance to fluctuation to critical current. In fact, it works the best at temperatures below the nominally designed optimal of 4.2 K. This is the opposite trend of the previous chip design. It also points an anomaly in one of the biases identified as BK32. The bias center is lower compared to the other biases, which will result in lower overlapping margin.

This technique allows testers to find the optimal temperature for a particular chip as well as to characterize how closely the design and fabrication meet the spec parameters.

**Figure 6.** Bias margin as a function of temperature for 256-bit long shift register. The width of biases is the bias margin. Each bin contains 6 bias margins at specific temperature.

4. Conclusions
High throughput and variable temperature testing are a relative new testing paradigm in the field of superconductor electronics. The ability to vary temperature precisely while testing the 3-to-2 and 7-to-3 parallel counters and the 256-bit shift register design allowed us to determine the critical current of the JJs that gave the most robust performance. When the optimal operating temperature is different than the nominal designed 4.2 K, how much and in what direction it differs provides important feedback to the circuit designer. Using this information, they can then run post-layout simulations varying the parasitics to match those found in the experimental results. From these empirically derived parasitic values the IC designs can then be optimized, and the model-to-hardware correlations can be iteratively improved. These provide better clues to circuits designers than testing at a single temperature point.
High throughput testing of the 7-to-3 parallel counter circuits uncovered wafer-wide reduced margins and low center points for the logic bias, while affirming the robustness of the 3-to-2 parallel counter. If only one or two chips were tested, some of the 3-to-2 chips showed suppressed operating margin while some of the 7-to-3 chips showed higher operating margins. This would have created a false impression of circuit performance and would lead to poor decisions in future designs. When enough statistics are collected the average circuit parameters provide far more reliable indicators for the designer.

References
[1] Gaidarenko D and Robertazzi R 1999 High performance packaging system for superconducting electronics IEEE Trans. Appl. Supercond. 9 3668-3671
[2] Kramer D 2017 Erratic helium prices create research havoc Physics Today 70 26-29
[3] Mukhanov O, Kirichenko D, Vernik I, Filippov T, Kirichenko A, Webber R, Dotsenko V, Talalaevskii A, Tang J, Sahu A, Shevchenko P, Miller R, Kaplan S, Sarwana S and Gupta D 2008 Superconductor digital-RF receiver systems IEICE Trans. Electron. E91-C 306-317
[4] Dotsenko V, Chonigman B, Sahu A, Tang J, Lehmann A, Sarwana S and Gupta D 2017 Superconductor Integrated Circuit (IC) Testing with the integrated cryogenic electronics testbed (ICE-T) IEEE Trans. Appl. Supercond. 27 1-7
[5] Van Duzer T and Turner C 1999 Principles of superconductive devices and circuits (Upper Saddle River, NJ: Prentice Hall PTR)
[6] Narayana S, Polyakov Y and Semenov V 2009 Evaluation of flux trapping in superconducting circuits IEEE Trans. Appl. Supercond. 19 640-643
[7] Dotsenko V, Sahu A, Chonigman B, Tang J, Lehmann A, Gupta V, Talaleevskii A, Ruotolo S, Sarwana S, Webber R and Gupta D 2017 Integrated cryogenic electronics testbed (ICE-T) for evaluation of superconductor and cryo-semiconductor integrated circuits IOP Conf. Ser.: Mater. Sci. Eng. 171 012145
[8] Filippov T, Sahu A, Kirichenko D, Celik M, Sarwana S, Lehmann A and Gupta D 2018 Parallel Counters for low-pass phase modulation–demodulation ADCs IEEE Trans. Appl. Supercond. 28 1-5
[9] Zinoviev D and Polyakov Y 1997 Octopux: an advanced automated setup for testing superconductor circuits IEEE Trans. Appl. Supercond. 7 3240-3243
[10] Tolpygo S, Bolkhovsky V, Weir T, Johnson L, Gouker M and Oliver W 2015 Fabrication process and properties of fully-planarized deep-submicron Nb/Al–AlO/Nb Josephson junctions for VLSI circuits IEEE Trans. Appl. Supercond. 25 1-12
[11] Tolpygo S, Bolkhovsky V, Weir T, Wynn A, Oates D, Johnson L and Gouker M 2016 Advanced fabrication processes for superconducting very large scale integrated circuits IEEE Trans. Appl. Supercond. 26 1-1
[12] Tolpygo S, Bolkhovsky V, Zarr S, Weir T, Wynn A, Day A, Johnson L and Gouker M 2017 Properties of unshunted and resistively shunted Nb/AlOx-Al/Nb Josephson junctions with critical current densities from 0.1 to 1 mA/μm^2 IEEE Trans. Appl. Supercond. 27 1-15

Acknowledgments
The authors would like to thank A. Erik Lehmann and Saad Sarwana for their help in conceiving the product, Mustapha Habib for his help with data recording, and Timur Filippov for his editorial contributions.