A Ka band CMOS LO distribution buffer using transformer-based three-way power divider

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Abstract: A Ka band CMOS LO distribution buffer with one single-ended input and three differential outputs is presented. In order to split the input power to three differential ones, a new transformer-based unequal differential three way power divider is proposed and adopted. Based on the traditional dual way power divider transformer, an additional concentric winding loop for the third differential output is implemented in the proposed three-way power divider. Two stages of unit differential cascode amplifier are added to boost the gain and isolation. The area of LO distribution network is only 780 $\mu$m $\times$ 690 $\mu$m and thus is more compact. Measurements show that the output buffer offers a 5.8 dB peak gain at 35.7 GHz with amplitude and phase balances better than 6° and 0.5 dB.

Keywords: LO distribution buffer, transformer, three-way power divider, CMOS

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

LO distribution buffers are commonly used in millimeter wave transceivers, to drive the following stages: mixers, power amplifiers [1, 2, 3]. Isolation, area, insertion losses are the key parameters for the LO buffer that needs to provide enough LO swings for the following stages at the minimum power and area consumption [4]. The key component in LO buffer is the power divider which splits the input power to different outputs. There are mainly two types of on-chip power dividers, Wilkinson power divider and transformer-based divider. Wilkinson power dividers based on 1/4 λ transmission line are often adopted in complex LO distribution networks in which the spacing between the following modules is comparable to 1/4 λ [2, 5]. And most of the Wilkinson power splitters in CMOS technology are single-ended with two outputs [5, 6]. Few previous works report Wilkinson power dividers with over two output ports in CMOS technology because on-chip transmission line with high characteristic impedance is hard to implement, no more than 80 Ω for most designs. And most of the Wilkinson power dividers in CMOS technology are single-ended. Converting the single-ended signal to differential ones will introduce additional losses.

Another method for power split is transformer, which is often used to split or combine the input power [7, 8, 9, 10, 11]. To the best of the author’s knowledge, most of the transformer based power dividers have only two outputs [7, 8, 9, 11].
Providing three outputs is mostly realized by duplicating dual-way dividers physically. However, cascading two stages of transformers will double the chip area and lower the efficiency due to insertion losses.

Using the aforementioned transformer or transmission line based divider, there are several works reporting the LO distribution networks with active amplifiers to compensate for the insertion losses from passive components [11, 12, 13, 14]. Transmission line based dividers [12, 14] have broader bandwidth compared with transformer based one [11]. However, most of the transmission line based dividers are single-ended, that need additional balun to convert the signal to differential ones. Another disadvantage of transmission line (TL) power divider is that it consumes too much area and is less compact than transformers. In addition, to the best of the author’s knowledge, most of the previous works on LO distribution network provide even number of outputs [11, 12, 13, 14]. It is hard to implement three-way power divider in CMOS technology.

In this work, to further reduce chip size and provide three outputs, a Ka band CMOS LO buffer using transformer-based three-way differential power divider is proposed. As shown in Fig. 1, the LO distribution buffer is used to divide the input LO signals into three differential ways: to two mixers and power amplifier. As shown in Fig. 2(b), the core of the LO distribution buffer is a new 2:2:1:1 three-way transformer-based unequal power divider. Compared with the traditional two way power divider in Fig. 2(a) [7, 8], the secondary loops in blue ($V_{out2}$ and $V_{out3}$) are same as the traditional one. An additional concentric winding loop $V_{out1}$ is

![Fig. 1. Topology of LO buffer.](image1)

![Fig. 2.](image2)

(a) Traditional dual-way power divider. (b) The proposed three-way power divider.
implemented for the third differential output (the green one), using the same metal of the primary input loop. Since $V_{out2}$ and $V_{out3}$ are totally symmetric, the output power at $V_{out2}$ and $V_{out3}$ are equal. The proposed three-way power split transformer occupies an area of $160 \mu m \times 160 \mu m$, and therefore is compact enough to be adopted in LO distribution buffer.

2 LO distribution buffer

2.1 Circuits topology

The schematic of the Ka band LO distribution buffer is shown in Fig. 3. For the measurement requirements, the LO buffer is designed as one single-ended input with three differential outputs. An input transformer balun (T1) and output buffers are used in order to obtain good matching and isolation. Differential unit cascode amplifier (UCA) with transformer (T31, T32, and T33) is adopted in the output buffer stage, to provide enough gain and output matching. As in Fig. 3, $V_{out2}$ and $V_{out3}$ are sensitive to the variations of the input resistance of the UCA2 and UCA3 driven by the power divider. Thus the output buffers of $V_{out1}$, $V_{out2}$, and $V_{out3}$ are designed to be same (20 μm/60 nm) to minimize the differences. All of these methods help reduce imbalances at the outputs. Each of the differential UCA consumes about 4.8 mA current and the whole power consumption is 23.1 mW from 1.2 V.

![Fig. 3. The schematic of Ka band LO distribution buffer.](image)

2.2 Three-way power divider

Fig. 4(b) depicts the physical layout of the proposed three-way power divider. The primary loop uses top metal (M8) for a higher quality factor. The thickness of M8 is 3.25 μm and the widths of all traces are selected to be 8 μm. The physical dimension of the proposed power divider transformer is carefully designed to form LC tank resonance with UCA0 at frequency of interest. Same like the traditional dual-way transformer in Fig. 4(a) [7, 8], two secondary loops are placed beneath the primary loop in Metal 7 so that the voltage of primary loop will be split in $V_{out2}$ and $V_{out3}$ in series way. Because the primary loop of $V_{in}$ is in parallel with $V_{out1}$ and
$V_{out2} + V_{out3}$, the input current is divided in parallel way to the output loops ($V_{out1}$ and $V_{out2} + V_{out3}$). In sum, the proposed power divider transformer splits input power in hybrid way [7, 9], both in parallel and series manner. The center taps of the secondary loop are connected together because all of UCA output buffers share the same dc bias.

According to the EM simulations of the proposed power divider transformer, quality factor of primary loop is over 10 from 34 to 37 GHz. Phase and magnitude balance of the output three ways are further investigated that all the amplitude phase balances are better than 0.3 dB and 3°. Finally, the area of the core three-way power divider is $160 \times 160 \mu m^2$, which is more compact than the traditional $\lambda/4$ Wilkinson power divider.

3 Experimental results

The proposed LO distribution buffer is fabricated in 1.2 V standard 65 nm 1P8M CMOS process. The chip microphoto is shown in Fig. 5 and the chip area including all pads is about 780 $\mu m \times 690 \mu m$. Three-port S parameters of P1, P2 and P3, as well as P1, P4 and P5 are measured using Agilent 5244A four-port vector network analyzer and RF probes up to 40 GHz. The gains of $RF_{out1}$ and $RF_{out2}$ are also measured with signal sources and spectrum analyzer. Since the $RF_{out2}$ and $RF_{out3}$ are totally symmetric, pads on left side are used for DC bias instead of RF pads of $RF_{out3}$.

Fig. 6 illustrates the measured gains of the differential outputs, P2 and P3 of $RF_{out1}$, up to 40 GHz in dots, which fits well with the simulated results in lines. The measured gains ($S_{21}$ and $S_{31}$) are 5.8 dB at 35.7 GHz and over 2.8 dB gains from 34.1 GHz to 37.4 GHz, as in Fig. 6. Phase balances of these two ports (phase($S_{31}$)-phase($S_{21}$)) are also measured and depicted in Fig. 8. Amplitude and phase balances of P2 and P3 are better than 0.3 dB and 4°.

The measured gains ($S_{41}$ and $S_{51}$) of the differential outputs, P4 and P5 in $RF_{out2}$, are illustrated in Fig. 7, which are 3.2 dB and 2.9 dB at 35.5 GHz and over

![Physical layout of power divider transformers. (a) Traditional dual-way power divider. (b) Proposed three-way power divider.](image-url)
Fig. 5. Chip microphoto of the LO distribution buffer.

Fig. 6. Measured and simulated gains of P2 and P3 in $RF_{out1}$ versus frequency.

Fig. 7. Measured and simulated gains of P4 and P5 in $RF_{out2}$ versus frequency.
0.2 dB gains from 33.8 GHz to 36.7 GHz. Fig. 8 shows the measured and simulated phase balances of these two ports (phase($S_{51}$)-phase($S_{41}$)). According to Fig. 7 and Fig. 8, amplitude and phase balances of P4 and P5 are better than 0.5 dB and 6° from 34 GHz to 40 GHz. $RF_{out2}$ and $RF_{out3}$ are sensitive to the imbalance arisen from the input transformer (T1). Thus the balance of differential outputs can be further improved if the input signals are in differential forms.

Fig. 9 shows the return losses of P1, P2, and P3, that are better than 10 dB in the frequency band of interest (34.5–36.5 GHz). As shown in Fig. 10, the reverse isolation of these three ports is over 40 dB in the frequency band of interest. Since the output buffers of all the three outputs ($RF_{out1}$, $RF_{out2}$, and $RF_{out3}$) are same, measured results of return losses and reverse isolation of P4 and P5 in $RF_{out2}$ are similar like P2 and P3 in $RF_{out1}$, better than 10 dB and 40 dB respectively in the frequency band of interest (34.5–36.5 GHz).

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**Fig. 8.** Measured and simulated phase balances of differential outputs in $RF_{out1}$ and $RF_{out2}$.

**Fig. 9.** Measured and simulation results of return losses.
The S parameters of P2, P3, P4 and P5 are also measured using vector network analyzer to demonstrate the isolation between different outputs. Fig. 11 depicts the measured and simulated isolation between RF\textsubscript{out1} and RF\textsubscript{out2}, with the simulated results in line and measured results in dots. The isolation between RF\textsubscript{out1} and RF\textsubscript{out2} is better than 22 dB at the working frequency (30 GHz–40 GHz), which will largely reduce the couplings between different modules.

According to simulated results in Fig. 12, the magnitude and phase differences between RF\textsubscript{out2} and RF\textsubscript{out3} are below 2° and 0.6 dB from 32 GHz to 38 GHz. Thus RF\textsubscript{out3} are totally symmetric to RF\textsubscript{out2} and simulation results of RF\textsubscript{out3} are not listed.
In Fig. 13, large signal test is performed and shows that output compression point ($P_{1dB_{out}}$) of P2 and P4 are $-2.7$ dBm and $-3.2$ dBm respectively. The whole Ka band LO distribution network consumes 19.2 mA from 1.2 V power supply.

Finally, the performances of the proposed CMOS Ka band LO distribution network are summarized in Table I and compared to those of state-of-the-art.
4 Conclusion

This article presents a Ka band CMOS LO distribution buffer with one single-ended input and three differential outputs in standard 65 nm CMOS technology. A new transformer-based unequal differential three way power divider is proposed and adopted to split the input power to three differential ones. It is worth noting that the two stage LO buffer offers 5.8 dB peak gain at 35.7 GHz with excellent amplitude and phase balance. The isolation between different output ports is better than 22 dB and the reverse isolation is over 37 dB according to the measurement. Moreover, the area of the LO distribution network is only $780 \mu\text{m} \times 690 \mu\text{m}$, which is more compact and can be widely used in Ka band CMOS millimeter wave transceiver.

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