A survey of digital down converter architecture for next generation wireless applications

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Abstract: This article presents a brief survey of Digital down Converter (DDC) architecture and its extensive applications. The distinctive feature of the DDC architecture is its frequency translation from real data signal at an intermediate frequency to a complex baseband signal at zero frequency. The architecture of DDC comprises of Numerically Controlled Oscillator (NCO) and decimation filters. The components of ultra efficient DDC architecture have been implemented in Field Programmable Gate Array (FPGA) device. This down converter provides high malleability, customizability and bearable cost. Due to its amenities, digital down converter was utterly studied and applied in many wireless communication technologies.

1. INTRODUCTION

In wireless applications, the demand on high speed data communication is a driving force in the development of flexible wireless communication technology. Some of the high frequency wireless communication standards, namely IEEE802.11a, IEEE802.11b, IEEE802.11g, IEEE802.11n and IEEE802.11ac is regularized with the frequency of the carrier up to 5GHz and broadly used. IEEE802.11ad is an extremely high frequency band (EHF) wireless networking standard called millimeter wave (mmWave) whose frequency upto 60GHz is an arising frequency band in 5G wireless communication [1-2]. The conventional radio frequency (RF) receivers (RX) involves three major blocks, namely Low noise amplifier, Downconverting mixers, intermediate frequency filters/amplifiers and analog to digital converters. Despite that, the RF receiver blocks should be cautiously designed to evade some common issues such as AC coupling, DC offsets, I/Q mismatch, mixer linearity, etc. [3]. Similarly, in the high frequency band (mmWave), problems associated with analog circuits are tedious to handle in standard CMOS or SOI process [4,5].

The above mentioned issues can be solved by using DDC receiver next to Radio Frequency front end comprised of the radio frequency antenna and the low noise amplifier, which solves the problems related to EHF analog circuits. The digital down converter (DDC) has turned into crucial technique in advanced wireless communication systems. The DDC plays an essential role in signal processing applications which converts real digitized intermediate frequency signal into a baseband complex signal. It consists of three main blocks such as Numerically Controlled Oscillator (NCO), Mixer and Filter. The NCO is also called as Direct Digital Synthesizers (DDS) is used to generate discrete-time representation of a waveform generally sinusoidal. A mixer is a circuit which shifts a signal from one range of frequency into another range of frequency and this process is known as heterodyning and the filter deals with down sampling process which decreases the sampling rate of output signal. DDC can be classified into two types, namely narrow band DDCs whose bandwidth are below 1MHz and
wideband DDCs which have above 1MHz bandwidth. Narrow band DDCs are suitable for commercial broadcast applications and wideband DDCs are used in satellite applications.

Many research scholars are endeavoring to implement efficient, high speed Digital Down Converter architecture for various applications [6]. In recent times, reconfigurable FPGA based DDC architecture was designed that down converted the range of input frequency from 3.6GHz to the output range of 1KS/s to 225MS/s and it was implemented on a Xilinx Kintex-7 device [7-9]. This paper reviews some of the applications of DDC architecture from the past two decades.

1.1 DDC Architecture
The Digital Down conversion is one of the digital processing technique broadly used in digital radio receivers which conserves all the information in the original signal.

![Figure 1. Basic Block Diagram of DDC](image)

The architecture of DDC consists of three subcomponents namely NCO, mixer and filter structure as shown in the figure 1. The output of Analog to Digital converter is given as input to DDC which down converts the radio frequency signal into a complex base band signal.

Let the output of the ADC $S(t)$ is down converted into a complex baseband signal which is expressed in terms of Sine and Cosine terms.

$$S(t) = \cos(\omega_0 t)$$

Let the oscillating frequency $\omega_0$, then the output of decimating filter is given by

$$S_\ell(t) = \cos(\omega_0 t) \ast \cos(\omega_\ell t)$$

This can be expanded as

$$S_\ell(t) = \frac{\cos(\omega_\ell - \omega_0) t}{2} + \frac{\cos(\omega_\ell + \omega_0) t}{2}$$

The imaginary term $S_Q(t)$ can be derived as

$$S_Q(t) = S(t) \ast \left[\sin(\omega_0 t)\right]$$

$$S_Q(t) = \frac{\sin(\omega_\ell - \omega_0) t}{2} - \frac{\sin(\omega_\ell + \omega_0) t}{2}$$

2. EXPLORATION OF DIGITAL DOWN CONVERTER

The recent development of digital down converter (DDC) architecture is described in this section. One of the major components in DDC architecture is digital filter. The major advantages of digital filter are accurate and precise realization of linear phase transmission. The digital filter consists of the input signal as in quantized time series $[x(kT)]$ and it generates the output in other form of quantized timeseries $[y(kT)]$ which is defined by linear difference equation[10]
2.1 CORDIC processor and CIC Filter
The numerically controlled oscillator is used in DDC architecture for generating sine and cosine waveforms. This system needs a large LUT (2n X n bit) for high resolution; hence it occupies a huge area, resulting in the large power dissipation and less operating speed. To overcome these problems, CORDIC processor is used by replacing NCO and mixer [11] in DDC architecture. This CORDIC processor desires small LUT for In-phase and Quadrature modulation system.

The CORDIC processor has three inputs; a first input (P0) is considered as zero, sample of S(t) is applied to the second input (Q0) in each and every clock cycle and the last input (R0) is from phase accumulator to afford sample frequency of the CORDIC processor. The output of this processor is spurious-free dynamic range (SFDR) complex signal. The CORDIC algorithm can work in linear, circular and hyperbolic configurations [12,31] and operates in rotation or vectoring modes. To generate sine and cosine waves, the processor operates in rotation mode [13]. During each iteration, the vector components in this mode of operation are described as [14].

\[ p_{i+1} = p_i - d_i q_i 2^{-i} \quad \text{---(7)} \]
\[ q_{i+1} = q_i + d_i p_i 2^{-i} \quad \text{---(8)} \]
\[ r_{i+1} = r_i - d_i \arctan(2^{-i}) \quad \text{---(9)} \]

The output of the CORDIC is obtained after n iterations and they are

\[ P_n = K_n [P_0 \cos(Z_0) - Q_0 \sin(Z_0)] \quad \text{---(10)} \]
\[ Q_n = K_n [Q_0 \cos(Z_0) + P_0 \sin(Z_0)] \quad \text{---(11)} \]
\[ R_n = 0 \quad \text{---(12)} \]

where \( P_n, Q_n, R_n \) represents CORDIC outputs, \( K_n \) indicated as gain factor and it can be defined as

\[ K_n = \prod_{i=0}^{n} \sqrt{1 + 2^{-2i}} \quad \text{---(13)} \]

Thus, this CORDIC can be realized only using adders, shifters and comparators devoid of multiplier and divider units. Hence the realization of CORDIC architecture in FPGA unit has high throughput and also saves the hardware resources.

The output of the CORDIC processor is given to multi-stage CIC decimation filter. As depicted in the figure 2, the cascaded Integrator Comb (CIC) filter comprises of Integrator section that driving at the highest sampling frequency (fs) and comb section driving at a low sampling frequency (Nyquist rate) of (fs/R) where R is the decimation factor. The transfer function of the composite CIC filter [15] is given by

\[ H(z) = \left( \sum_{i=0}^{RM-1} Z^{-i} \right)^N \quad \text{---(14)} \]
Nevertheless, the CIC decimation filter has high power consumption in down sampling the signals because of adders with high sampling rate in integrator section [15-17]. To reduce the power consumption, numerous techniques such as two stage and multistage non-recursive CIC structures have been proposed [17-25].

As depicted in the figure 3, the CIC filter is connected with Multi-Channel Systolic Finite Impulse Response named MSFIR filter to override the magnitude droop of the comb section. This MSFIR filter is mainly used to perform band stop attenuation and to attain accurate bandwidth transition [26-30]. Thus the implementation of the CIC and MSFIR filter for DDC in FPGA platform enhances area optimization and consumes less power.

2.2 ISOP Filter sharpening method

The CIC filter is cascaded with interpolated second order polynomial (ISOP) filter for efficient DDC design. The ISOP filter is designed in [32] which is used to balance the passband droop caused by the CIC filter. The system function $F(z)$ of ISOP is defined as

$$F(z) = \frac{1}{d+2} (1 + dz^{-1} + z^{-2l})$$

where $F(z)$ represents an interpolated form of second order polynomial, $d$ is indicated as real number and $l$ is defined as an integer that should be in the range of $1 \leq l \leq \frac{1}{2f_s}$. This polynomial has a property such that, the amplitude response of the polynomial function $F(z)$ is described as

$$F(e^{j\omega}) = \frac{1}{|d+2|} |d + 2\cos\omega| \quad \text{(when } d \text{ is real)}$$

As depicted in the figure 4, the CIC filter is cascaded with ISOP filter to further sharpen the response. This cascading helps in achieving a sharper transition and reduces the second order droop in the passband.
The figure 4 shows that the output of the CIC filter is given to ISOP filter. For this structure, Modified Parks-McClellan [33,34] and linear programming method [35,36] can be used for designing the ideal ISOP filter.

2.3 Polyphase Digital down Converter

The polyphase filter is mainly used in wideband digital system to perform sampling rate conversion and also to reduce computational complexity [37]. Polyphase filters are classified as two types such as polyphase interpolation filter and polyphase decimation filter based on sampling rate conversion. The wideband system is always divided into narrow sub-band channels and these sub-band channels are put together in polyphase form to acquire the function of wideband system. The fundamental idea of polyphase filter is to crumble the linear transfer function $H(z)$ into $H_n(zR)$.

$$H(z) = \sum_{n=0}^{R-1} H_n(z^R)z^{-n}$$

$$H(z) = H_0(z^4) + z^{-1}H_1(z^4) + z^{-2}H_2(z^4) + z^{-3}H_3(z^4)$$

where $R$ represents the decimation factor whose value is assigned as 4. The basic polyphase DDC architecture comprises of a polyphase CIC filter and a compensation FIR filter (CFIR) stage which is preferable for high sampling rate (e.g. $R \geq 16$).

![Figure 5. Polyphase DDC architecture for in-phase (I) path (R=4, N=3 and fs = 4 X fc)](image)

As shown in the figure 5, the polyphase DDC architecture has been designed based on the following condition for I-path and the same procedure also has been followed in the Q-path. The path for the output 1 of NCO can be connected to input x and in the path of NCO output -1, binary negator is introduced. Polyphase filter is used to enhance the digital system block in terms of sampling rate [38,39]. Efficient multiplierless polyphase FIR filter is designed based on Distributed Arithmetic (DA) to diminish the hardware complexity.
2.4 Variable Digital Filter

Variable digital filters (VDF) are widely used in software-defined radio (SDR) for separating the appropriate radio channels from wide band input signal for different wireless communication standards. A digit-based reconfigurable FIR filter design was suggested in [40]. This filter structure has high hardware complexity. The frequency response masking (FRM) technique [41] was suggested to attain fine transition bandwidth. Based on this technique, a reconfigurable FIR filter was put forward for Software Defined Radio receivers. In order to attain low intricacy reconfigurable FIR filters, a coefficient decimation method (CDM) was suggested which utilize coefficients of filter selectively to acquire arbitrary frequency responses.

![Fig 6. ICDM based VDF Hardware architecture](image)

To enhance the frequency response flexibility, modified coefficient decimation method (MCDM) was schemed in. Furthermore, an improved CDM (ICDM) technique was implemented which involve both CDM as well as MCDM method. The hardware architecture of ICDM based VDF filter is depicted in the figure 6 which is based on transposed direct form FIR filter architecture. The ICDM comprises of two operations, namely ICDM-I and ICDM-II. The ICDM-I operation is for replacing the filter coefficients by 0’s to attain a frequency response for the desired type of filter based on decimation factor M1 and ICDM-II for eliminating the filter coefficients to alter the bandwidth of sub bands in

\[ s(t) = d(t)\cos[2\pi f_c t + \phi(t)] \]  

According to bandpass sampling frequency:

\[ f_s = \frac{4f_c}{2^n+1} = \frac{f_c}{3} \quad (if \ n = 1) \]

Then the sampling sequence is given by

\[ s(n) = d(n)\cos\left[\frac{2\pi f_c n}{f_s} + \varphi(n)\right] \]

Substitute \( f_s \) and elaborate the above equation, we can get

\[ s(n) = d(n)\cos\varphi(n)\cos\left(\frac{3\pi n}{2}\right) - d(n)\sin\varphi(n)\sin\left(\frac{3\pi n}{2}\right) \]

This equation can be rewritten as

\[ s(n) = s_I(n)\cos\left(\frac{3\pi n}{2}\right) - s_Q(n)\sin\left(\frac{3\pi n}{2}\right) \]

where \( s_I(n) = d(n)\cos\varphi(n) \) and \( s_Q(n) = d(n)\sin\varphi(n) \) are called as signal in-phase and quadrature phase components.
the output frequency response of ICDM-I based on decimation factor M2. The add/sub blocks are utilized to execute either addition or subtraction operation based on select (sel) signal. This method was implemented to select channels according to various wireless communication standards such as Worldwide Interoperability for Microwave Access (WiMAX) Wideband Code Division Multiple Access (WCDMA) and Long Term Evolution (LTE) at different time intervals.

3. DEPLOYMENT OF DDC

Now-a-days Digital Down Converter (DDC) is employed in many applications in the field of communication. The following are some of the applications based on DDC.

3.1 Broadband Communication

The software defined radio communications are moving from analogue components towards the digital parts of the transmitter and receiver using FPGA based Digital Signal Processing (DSP) devices. The first phase of digital receiver is DDC for evading IQ imbalances of analogue demodulators. As suggested in the figure 7, the digital down converter is added with timing synchronization circuit at receiver side for efficient broadband communication and also pass band sampling is used in place of the Nyquist sampling. The function of the DDC is to decimate the intermediate frequency signal at a sampling rate of (1/Ts>2/T) which is done by using free running direct digital synthesizer and decimation filters. The timing synchronization circuit generates an absolute error free sample with the help of fractional interpolator timing error corrector and detector.

![Figure 7. Receiver Architecture for Broadband Communication](image)

The following are the advantages of this system. First, high throughput because of phase synchronizer circuit. Second, the sampling frequency of the ADC can be chosen freely by a designer which enhances the performance of digital down converter. Furthermore, it uses only simplified small area of mixers which reduces the cost of the mixer and decimating filters.

3.2 Powerline Communication

Power line communication (PLC) is an optimistic methodology for high speed transmission of data. In this methodology, the power line network has been used especially for delivering electricity in lieu of sending data. These PLC technologies can be employed in the area where the orbit can be either an extended range high voltage or short-distance moderate voltage. The ITU-T Recommendation certified G.9960 as a standard for high speed wire-line based home networking, which is deliberated to operate over shared media as power lines, phone lines and coaxial cables [41]. IEEE standard 1901 is a standard for rapid communication over power lines that were published in the year 2010 [42]. Most of the Powerline communication networks operate in the frequency range of below 30MHz [43-45]. The HomePlug Powerline Alliance has utilized adaptive OFDM method over a transmission capacity of 26MHz for establishing HomePlug AV system, to acquire a data rate of a physical layer up to 200Mb/s [46]. In [47], UWB pulse transmission has been achieved at 100MHz. Multi user
Powerline communication has been achieved by impulse modulation schemes and receiver algorithms [48,49].

The desired frequency range of Indoor low voltage (LV) cable is up to 578 MHz; henceforth the RF signal is converted into a required power line frequency range of 50-578 MHz by using frequency up converter and frequency down converter circuits [50-52]. Therefore, PLC requires Multi-band Orthogonal Frequency Division Multiplexing (MB-OFDM) signal which is generated by integrating MB-OFDM ultra wideband with digital down converter (DDC). Figure 8 shows the MB-OFDM ultra wideband system interfaced with digital up converter and down converter.

The architecture of digital down converter (DDC) is described in the figure 9. In order to minimize the harmonics, efficient DDC architecture has been used for power line communication which consists of 2-stage CIC and PFIR filters.

### 3.3 Ionospheric Link

The efficient digital transceiver is designed for long distance, low power high frequency ionospheric link across the Spanish Antarctic Base and Spain. In this project, cascaded short FIR filter based DDC is implemented for minimizing the stipulated arithmetic bit-width as well as for adjacent channel interference rejection. The HF ionospheric links are mainly used in communications to remote areas where the satellite communications are not feasible. The major goal of this scheme is to attain large data rates and channel availability by optimizing the transmission parameters.

![Figure 9. Block Diagram of DDC](image_url)

![Figure 10. Block Diagram of Receiver](image_url)
The digital direct conversion architecture has been used for implementing the receiver. As described in the figure 10, the receiver diagram comprises of (i) Low Noise Amplifier (LNA) whose gain (G) is 20dB, Noise Figure (F) 2.5 and compression point P1dB =22dBm (ii) Band Pass Filter (BPF) is used to attenuate interference by tuned digitally across an entire HF band (iii) Variable Gain Amplifier (VGA) for adjustment in receiving power level (iv) LPF that allows frequency lower than cutoff frequency of 21.5MHz and finally (v) 14 bits, 60MSPS A/D converter is used for generating digital signal, given as input to digital down converter (DDC).

3.4 Underwater Wireless Communication

Underwater wireless communication systems plays a crucial role in exploring the ocean potential in field such as oil, minerals, pharmaceutical, Disaster prevention, military, environmental and biodiversity [53,54]. This system is mainly for high data rates and long distance communications between overwhelmed mobile and static agents. The wireless communication technologies using electromagnetic waves are not very proficient owing to large attenuation in the marine environment.

![Figure 11. Block Diagram of Underwater Acoustic Modem](image)

Due to this, Underwater Wireless Sensor Networks (UWSN) use acoustic waves with lower attenuation for long distance communication and face major research challenges viz insufficient bandwidth, high energy consumption, large propagation delay [55-58].The Medium Access Control (MAC) protocol was designed [59] for UWSNs that allows multiple nodes to communicate through an apportioned medium, but it has a high bit error rate, also bulky and expensive. Thus, low-cost, lowpower Acoustic Modem is designed as depicted in the figure 11 to overcome those problems in underwater communication[60-61].

![Figure 12. Schematic Diagram of FPGA Implementation of FSK Modem](image)
Based on this modulation scheme as depicted in the figure 12, the DDC in digital transceiver redeems the signal to the digital baseband for subsequent processing. Then symbol synchronizer is used to allocate precise sampling and decision timing for demodulation. Finally, FSK demodulation scheme is used to retrieve the output signal.

4. CONCLUSION

This article presented a brief exploration of digital down converter architecture. First, it reviewed the basic concept of digital down converter and it summarized existing concepts for implementing digital down converter. Then, the deployment of DDC on different applications has been surveyed. This article afforded our insights on emerging research for future wireless applications.

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