A Design of Single Event Effect Test System

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Abstract. The single event effect brings great risks to spacecraft operating in special environments such as space. In response to this phenomenon, single-particle tests for evaluating its radiation performance are becoming more and more frequent. This article introduces a single event effect test system. The design method of the single event effect test system is introduced from the system architecture, test principle, and software and hardware design. The system is used for single event effect irradiation test research. And finally analyzed the experimental results.

1. Introduction

Spacecraft work in a space radiation environment. Due to the complexity of the environment[1], aerospace components must have high reliability, especially high resistance to single event radiation effects. The single event effect, that is, a single high-energy particle acts on a semiconductor device, causing an abnormal change in the logic state of the device, forming a logic soft error[2][3]. With the rapid development of the manufacturing process, the circuit integration level is getting higher and higher, the energy threshold required for the effect has become smaller, and the single event effect is more sensitive. The single event effect test is currently the main method to measure the anti-radiation performance of aerospace components. Digital circuits are mainly concerned with effects such as single event door locks, single event function interruption, and single event flipping. By simulating the special environment of the universe in a specific environment in the ground laboratory, the working condition of the device under the radiated state is characterized to achieve the purpose of ground verification. In view of the substantial increase in the demand for single-particle tests in recent years, it is necessary to carry out further research on the design of the test system.

This paper proposes a single event effect test system, and introduces the design method of the single event effect test system from several aspects of system architecture, hardware design and software design. Based on this system, the development of the single event effect test system can be conveniently carried out, and the efficiency can be improved. Finally, the system is used to carry out single event effect experiments on the unit test chip, and the obtained test results are analyzed.

2. System solutions

2.1. Test system composition

Single event flipping and transient effects appear as soft errors, so it is necessary to conduct online testing of the device under test under the irradiation of the radiation source. The structure of the single
The event test system is determined by the type and function of the test period. The basic requirements are as follows:

1. Able to test the functions actually used by the device;
2. Able to initialize the parameters of the tested device;
3. Diagnosis and recording function of single event effect events;
4. Real-time data processing, storage and retrieval;
5. With the function of automatic reset or manual reset;
6. It has good anti-electromagnetic interference ability.

Based on the above principles, the design of a single particle test environment is shown in Figure 1. The hardware part includes a single particle test board, control computer, program-controlled computer, power supply, and cable, and the software part includes control computer software[4].

![Figure 1. Schematic diagram of single particle test environment](image)

The single particle test board has the following functions:
- The test control and monitoring host adopts a commercial MCU to provide test functions such as excitation, monitoring, comparison, and recording;
- The system software reset of the detection system can be controlled in real time;
- Selection of test functions and provision of excitation sources;
- Power supply management;
- Test results monitoring, comparison and real-time transmission.

2.2. Test plan

The schematic diagram of the single particle irradiation test principle is shown in Figure 2, including four functional modules: analog source, unit test chip, control, and monitoring[5]. According to the test purpose and the condition of the test equipment, the laboratory provides one or several types of particles with the LET threshold, and provides a single-particle irradiation simulation according to a certain fluence rate. When the total fluence of each particle irradiation reaches the requirements of the test specification, replace the next particle for irradiation.

![Figure 2. Schematic diagram of single particle irradiation test principle](image)

The single-particle irradiation test uses an online test, and the control part provides functions such as power supply, excitation generation and response collection for the unit test chip[6]. During the single event irradiation test, it is necessary to monitor the current of the unit test chip in real time to avoid the
single event latch-up effect. At the same time, monitor the function running status of the unit test chip. Once the program runaway caused by single event flip occurs, it must pass the remote monitoring system initiates a command to the unit test chip to restart it[7].

The single particle irradiation test procedure is as follows:
1. Sample preparation: the selection of simulation source parameters.
2. Test layout: According to the conditions of the simulated source, arrange the experimental support, samples and detectors, and consider the influence of the simulated source on the test system. The sample should be placed as close as possible to the monitor or where it is easy to calculate the intensity of the analog source to ensure accurate measurement of the intensity of the analog source.
3. Test system debugging: debug the system before the experiment to ensure the normal operation of the test system, DUT board and test monitoring equipment; ensure the normal operation of the analog source intensity monitoring system and accelerator system.
4. Start the test: Under the normal operation of the test system, start the test, monitor and record the number of soft errors occurring in the device and the intensity of the analog source in real time. During the entire test process, it is required to monitor and record the intensity of the analog source at the device to ensure that the unevenness of the interference space of the analog source is less than ±10%.

3. Hardware design
The hardware design of the test system is mainly a test board design. Because the test board needs to be placed in a vacuum tank during the test, there is a space limitation, so the test board design must not only meet the requirements of functional testing, but also meet the corresponding structural requirements. In this paper, the control device and the irradiated device are respectively designed on the daughter board, and the chip under test is designed on the daughter board and placed on the top layer, and the control device is designed on the core control mother board and placed on the bottom layer. Figure 3 is a schematic diagram of the single particle test board structure, Figure 4 is the physical diagram of the designed universal core board (mother board), and Figure 5 is the physical diagram of the designed daughter board, which is connected to the motherboard through a rectangular printed circuit connector.
4. Software design
The single component runs in the on-chip MRAM. As shown in Figure 6, the two MRAMs are the program and check code storage areas of the test software respectively. Before the test, the curing program is burned through the serial debugging port.

![Figure 6. Schematic diagram of the partial structure of the single particle control board](image)

The control computer software is the user's direct control software, with a user interface, and its main functions are as follows:

1. Selection of test sample: After the user selects the test sample through the software interface, the test sample number selected by the test monitoring software module will be notified;
2. Power-on, reset and other control: After the user performs the corresponding operation through the interface, the corresponding command is sent to the test monitoring software through the asynchronous serial port;
3. Test item configuration;
4. Reading and display of test results: During the test, a read command is sent to the test monitoring software at a fixed time length to read the current test results of the test samples and display them on the software interface.

The software workflow of the control computer is shown in Figure 7, and the software interface is shown in Figure 8.

![Figure 7. Control computer software work flow chart](image)

![Figure 8. Control computer software interface](image)
5. System test

5.1. Unit test chip
In order to test the designed single event effect test system, a unit test chip is used for single event effect test. This unit test chip uses a semi-customized method for wiring connection. It has been proved that the design speed is faster than the fully customized test chip, and the wiring is more convenient. Figure 9 is a photo of the layout of the unit test chip. The DIE size without the dicing groove is 3.94mm*4.04mm. The package form adopts CQFP128.

![Unit test chip layout](image)

The unit test chip concentrates on the test for each library unit, including the STD unit and the IO unit. Its core feature is to cover the functional test of all units. Through the chain structure design, the performance test is realized. Figure 10 is a schematic diagram of the structure of the unit test chip.

![Schematic diagram of unit test chip structure](image)

This article is oriented to the test of anti-single event irradiation test. In the design of the unit test chip, the basic D-type trigger chain structure of TMR type and the D-type trigger of DICE structure (hereinafter referred to as RH type D trigger) are realized respectively. Chain structure. Each type of register forms a test chain of 400 cells, and each flip-flop chain adopts a three-mode structure, as shown in Figure 11, with a total of 1.92W registers.

![Diagram of D flip-flop test structure](image)

Select INV, BUF, and DEL to form a chain of 4000 cells each, and select cells with driving capabilities of X1 and X3 to form the chain respectively. The chain is organized in two ways: single drive and triple drive. Fig. 12 is a schematic diagram of the structure of a single-drive test chain, and Fig. 13 is a schematic diagram of the structure of a three-fold drive test chain.
5.2. Single event test

The unit test chip directly outputs the results to the port for each test unit, and the output frequency is controlled by the input CLK_in. During the test, the signal from the output port is collected and compared with the target result in each cycle, and each cycle can be obtained. The on-line monitoring system will record this result as the judgment result of the final test to determine whether a single event flip occurs inside the internal chip. In this paper, the designed test chip is used to carry out the single-event inversion irradiation experiment. The experimental equipment used is the HI-13 tandem accelerator.

| Particle type | LET value | Total fluence | Range  |
|---------------|-----------|---------------|--------|
| $^{48}$Ti$^{10,15+}$ | 21.8 MeV•cm$^2$/mg | 1.00E+7 | 34.7μm |
| $^{56}$Fe$^{10,15+}$ | 27.9 MeV•cm$^2$/mg | 1.00E+7 | 30.0μm |
| $^{63}$Cu$^{13,19+}$ | 32.2 MeV•cm$^2$/mg | 1.00E+7 | 33.1μm |

During the test, the current changes and the correctness of the chip function were recorded in real time, and the number of flips was detected in real time. According to the established test plan combined with the current test data, it can be concluded that all devices in the test process did not turn over. During the test process of the two chips designed this time, the test chip current is stable, the function is normal, the number of flips is zero, and both have greater than 32.2 MeV•cm$^2$/mg anti-single particle flipping ability.

6. Conclusion

This article introduces a single event effect test system. The design method of the single event effect test system is introduced from the aspects of system architecture, test principle, and software and hardware design. And based on this system, the unit test chip is used to carry out the anti-single particle irradiation test, and the experimental results are analyzed.

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