Abstract—This work presents design of a low power high-speed and high performance Time based ADC using TIQ(Threshold Inverter Quantizer) Comparator. This project helps to choose a low power with uW and less delay with nanosec high-speed VCO based ADC in designing of different systems. VCO stands for voltage controlled oscillator and the proposed ADC designed is based on 1-bit Quantizer and it is designed using TSPC (True Single Phase Clock) DFFs and followed by a XOR gate. Power and delay of ADC with different ADCs designs are compared. The working of VCO based ADC using different blocks helps to frame a better system with less power consumption and high speed. The entire design is done using CADENCE Tool with power supply of 1V in GPDK 45nm technology.

Index Terms—VCO –Voltage Controlled Oscillator, TIQ-Threshold Inverter Quantizer, ADC – Analog to Digital convertor, TSPC-DFFs, Time based ADC, 1-bit Quantizer.

I. INTRODUCTION

The design of analog-to-digital converter (ADC) based[1] on voltage-domain signal processing is becoming more difficult due to the low supply voltage that comes along with technology scaling. However, for time-based architectures, time resolution is improved from the reduced transition time of digital signals, which is on the order of tens of picoseconds for 45-nm CMOS processes and below. An ADC based on a voltage-controlled oscillator (VCO) generates a time-based signal whose frequency is proportional to the analog input. The frequency is then quantized by counting the edges of the VCO output during a sampling period. Since the VCO produces a continuous phase output, the quantization noise of the previous sample affects that of the current sample, and hence, an inherent first-order quantization noise shaping property can be achieved. However, unlike conventional delta-sigma ADCs that require complex analog building blocks such as op-amps and digital-to-analog converters (DACs), the VCO-based ADC can be implemented using only a VCO and digital circuits. Since the operating frequency is limited by the speed of the logic gates, it could easily reach up to giga samples per second in advanced CMOS processes.

Fig 1. Block diagram VCO based quantizer
VCO based ADCs[8] differ from traditional ADCs because there is an intermediate conversion to time. First the analog voltage is converted to time information then from time information to digital bits. Block diagram of typical Quantizer and VCO Based Quantizer is shown in figure1. This conversion process involves a VCO and time quantizer that will be examined in detail in later sections. To gain some understanding of how this process works it is necessary to know the operation of the VCO. The output frequency of the VCO is dependent on the input voltage and a larger input voltage means a higher frequency of operation and vice versa. Thus there must be some way of quantizing the VCO waveform to give a representation of the input signal to the VCO.

II. OVERALL IMPLEMENTED ARCHITECTURE

VCO-based ADC consists of a TIQ (Threshold Inverter Quantizer) comparator based on VCO to convert analog signal to an binary (or) digital data having reference voltage upon analog input signal. The phase detector based ADC using 1-bit quantizer is used further to quantize the analog signal. A 1-bit quantizer to convert the binary data to equivalent to digital data and it is equivalent to analog signal by using the two TSPC based DFFs and followed by a XOR gate is then employed to count the edges and finally gives the phase difference output. These edges are proportional to analog input value. And the output of a quantizer is then summing the adder circuit by using half adder and it can be summed and arranged to the equivalent analog input. And finally the adder circuit arrange the output of a quantizer and gives the equivalent binary output to analog signal.

2.1 TIQ (Threshold Inverter Quantizer) used as a VCO

Fig 2. proposed overall Architecture

Till now this comparator is used in other conventional based ADCs like Flash ADCs and some other Voltage based ADCs. But Time –based ADCs using this comparator can not have so, for the first time this paper explains the TIQ (Threshold Inverter Quantizer) comparator based VCO design for the Time based ADC's design has explained in this paper. The use of two cascading inverters as a voltage comparator[2] is the reason for the technique's name. The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters. Hence, we do not need the resistor ladder circuit used in a conventional ADCs.
Comparator’s role is to convert an input voltage (Vin) into a logic ‘1’ or ‘0’ by comparing a reference voltage (Vref) with the Vin. If Vin is greater than Vref, the output of the comparator is ‘1’, otherwise ‘0’. The TIQ comparator uses two cascading CMOS inverters as a comparator for high speed and low power consumption. The reduction of comparator count is obtained by analogue pre-processing circuits. These circuits consist of cross-coupled differential pairs having different DC offset voltage values applied to one of the inputs of each pair. The result is the folded input signal obtained differentially from the common output nodes of differential pairs. Here, as the resolution of fine-ADC part is increased, the number of differential pair needed is also increased accordingly.

2.2 VTC characteristics

The inverter threshold (Vm) is defined as the Vin = Vout in the Voltage Transfer Characteristics (VTC) of an inverter as shown in Fig. 4. We can set inverter threshold voltage from following equation:

\[ V_m = \frac{(r(V_{dd} + |V_{tp}| + V_{tn}))}{(1+r)} \]

with \( r = (k_p/k_n)^{1/2} \)

III.1-BIT QUANTIZER AS A PHASE DETECTOR
Fig 5. 1-bit Quantizer as a phase detector

Two DFFs and an XOR gate is operate as phase detector. High performance flip-flops are key elements in the design of contemporary high speed integrated circuits[4]. The ability to absorb clock skew and clock jitter is becoming more and more relevant today therefore the design of high performance flip-flops with reduced power dissipation, reduced clock to output time, near zero or negative setup time ,and clock skew absorption property is a major concern in modern high performance applications . A 5T TSPC DFF is used in this circuit which is a edge triggered DFF. 5T TSPC DFF consumes lesser power and area, compared with other DFF topologies like 9T and 11T TSPC. Standard cells are used in case of XOR gate. The schematics of 5T DFF is shown in fig 6. The schematic shows a 5T TSPC DFF which contains 3 NMOS and 2PMOS transistors. When the clock input is high whatever is the input that will becomes the output.

One major advantage of 5T TSPC DFF is reduced[5] area and power. The true single-phase clock (TSPC) is a common dynamic flip-flop variety which performs the flip-flop operation at high speeds and with little power, in the design of TSPC flip-flop edge triggered (positive or negative) D flip-flop is used. The circuit consists of alternating stages called n-blocks and p-blocks and each block is being driven by the same clock signal. The schematic of original TSPC flip-flop is shown in Figure 6.1 In this design a single global clock signal needs to be generated and distributed in order to simplify the design. Figure 6 presents Negative edge triggered TSPC D-flip-flop. It is operated as when the clock signal clk is HIGH, the input is isolated from the output. When clock makes a LOW-to-HIGH the output will latch the complement of the input. The true single phase clock dynamic CMOS[6] circuit uses only one clock signal for synchronization and it also reduces complexity. As the circuit uses only one clock signal so that it is suitable for both static and dynamic CMOS circuits. In TSPC flip-flop design a single global clock signal needs to be generated and distributed in order to simplify the design. The clocking system in the design may have single phase clock or multiple phase clocks. The clock phase controls the transfer of data between clock storage devices used in the synchronous VLSI digital systems[7]. In the output is same as input at both the rising and falling edge of the clock signal. True single phase clocking D flip-flop has several advantages as it eliminates clock skew caused by different clock phases and clock signals are generated off-chip which significantly saves chip area and power consumption.
3.1 XOR Gate

XOR compares the phase difference between the Two- DFF’s , using TSPC (True Single Phase Clock) DFF ,if any phase difference is occurred will get HIGH value other wise will get LOW value. And these value is equivalent to the thermometer code and these value is given to the adder circuit these will adding the thermometer code and arranging the code into the equivalent binary data like analog input.

IV. ADDER CIRCUIT

Current and previous states of a particular VCO element are quantized using combination of two D-latches in series. Quantized values are further differenced with XOR gate. And these value is equivalent to the thermometer code and these value is given to the adder circuit these will adding the thermometer code and arranging the code into the equivalent binary data like analog input. But in these half adder using as a adder circuit for adding the output of a XOR output and these can be arranged as a binary output as equivalent to the analog input.
V. OVERALL VCO BASED ADC DESIGN

The VCO Phase Detector based ADC in figure 9, was designed in a CMOS technology. The VCO was implemented using single ended TIQ comparator circuit. The Ring VCO is followed by 16 bit quantized phase detectors and a 16-bit Adder. The Phase detector consists of two DFFs and an XOR gate. And the DFFs uses a True Single Phase Clocked Register (TSPC) for low power consumption, and high performance and less transistor count. The 16-bit Adder is based on simple half adder Architecture which acts as normal adder. The designed ADC requires a for 8-bit it requires 3.669uW power, and for 16-bit it requires 7.336uW, and for both 8-bit and 16-bit as 27.76nanosec and 57.76nanosec at analog input voltage of 500mV, 1MHZ signal. The Schematic of VCO Based ADC using Phase Detector method is shown in figure 9. The proposed phase detector based ADC using 1-bit Quantizer is produces digital output by comparing analog input with the TIQ comparator reference Voltage and giving the binary output equivalent to the analog input. For theoretical analysis of VCO based ADC design conversion formula of analog to digital converter both these will give same binary data.
VI. RESULTS

6.1 Wave form of a TIQ as a VCO

The results of VCO as getting binary output by comparing analog input voltage with the reference voltage.

![Waveform of TIQ as VCO](image)

Fig 10. Waveform of TIQ as VCO

6.2 Simulation results of 1-bit Quantizer

Output from each delay element of VCO is quantized and differenced using combination of two D-latches and a XOR gate. D1 and D2 in figure 5, and stores the current and previous state of a particular delay element for a particular instant of voltage, respectively. These two states are further differenced using a XOR gate.

![DC analysis of a TIQ comparator](image)

Fig 11. DC analysis of a TIQ comparator
6.3 Simulation results of a Overall VCO based ADC using TIQ comparator

The simulation results of overall VCO based ADC using TIQ of 8-bit and 16-bit can be shown in below figures

![Simulation results of 8-bit VCO based ADC](image)
VII. POWER AND DELAY CALCULATIONS OF ADC

Table 1. Power and delay calculations of functional blocks of VCO based ADC.

| Functional Block                  | Power (45nm) | Delay (45nm) |
|-----------------------------------|--------------|--------------|
| VCO (TIQ comparator)              | 5.433μW      | 6.71ns       |
| 5T-TSPC DFF                       | 505.0μW      | 54.3ps       |
| XOR                               | 9.77nW       | 27.28ns      |
| 1-bit Quantizer                   | 32.06μW      | 4.28ns       |
| Adder                             | 27.85μW      | 20.25ns      |
| 8-bit VCO based ADC               | 3.669μW      | 27.76ns      |
| 16-bit VCO based ADC              | 7.336μW      | 57.76ns      |

Table 2. Comparison table of power and delay calculations of VCO based ADCs

Fig 14. Simulation results of 16-bit VCO based ADC
### Table 1

| VCO based ADC’s                      | Power   | Delay   |
|-------------------------------------|---------|---------|
| 8-bit phase detector based ADC using currentstraved VCO | 400.3mV | 9.801ns |
| 8-bit Quantizer based ADC           | 3.669uW | 27.76ns |
| 16-bit Quantizer based ADC (TIQ-VCO) | 7.336uW | 57.76ns |

Power and Delay of VCO based ADCs are tabulated in Table 1. From table 2, it is evident that using TIQ comparator as a VCO has less delay and power consumption and high performance. In Table I power and delay of functional blocks of VCO based ADCs are tabulated.

### CONCLUSION

The Time based ADCs like VCO based ADC using TIQ-Comparator (Threshold InverterQuantizer) is highly beneficial in order to reach a very low voltage supply, low power consumption, area and delay specification. This type of specification would be required for implementation for modern days applications. Designers nowadays apply power reduction techniques in every level of abstraction in order to achieve optimum level of speed, power and area. These reduction schemes must be applied to know the importance of maintaining the system performance.

The aim of this work is achieved by designing the VCO Based ADC using CMOS (Complementary Metal–Oxide Semiconductor). In CMOS technology the logic levels for logic 0 is 0V and logic 1 is 1V, the another advantage of CMOS Technology in 45nm Technology compared to other Technologies is the power consumption and also delay is less. While it has more speed of operation and consumes very low energy power computation. The CMOS-based digital systems is highly suitable for designing the digital part of the VCO Based ADC.

The CMOS based VCO Based ADC is designed at a power supply of 1.2V in 45nm Technology using cadence tools. The schematic are drawn using cadence virtuoso, schematic editor, symbol editor and while the simulations are done using Analog design environment (ADE L) Tools. The delay of CMOS inverter in 45nm is 35.57ps. It is observed that all the remaining other basic gates has less delay compared to other Technologies of CMOS. Hence CMOS is more advantageous. The power and delay of CMOS basic gates are calculated in 45nm Technology. The overall power and delay of 8-bit ,16-bit VCO based ADC is 3.656uW, 7.336uW and 27.28ps, 57.28ps.

### FUTURE WORK

The motivation behind this work is primarily to understand the applicability of using of TIQ comparator for VCO based ADCs in CMOS logic for designing digital systems. The results obtained, reflect on the advantages of using single ended TIQ comparator.

Future changes in this approach can reduce the power, delay and transition count by using the replica bias circuit. This design can be compared with other low power technologies like STSCL, reversible logic, MTCMOS and GDI, modified GDI techniques and implement 8 bit microprocessor. CMOS based VCO Based ADC using TIQ-comparator can be implemented in 180nm, 90nm and future other technologies also. The goal of this work has been to study, find, and suggest the CMOS as a better replacement over other techniques and other sub-threshold logic.
designs. The designed systems will later on can be used for different technologies, where low voltage and low energy specifications are highly influential. This thesis work suggests on achieving those specifications, but only at the schematic level. There by proper and satisfactory evaluation of the CMOS based systems will need chip level implementation of the designs to serve the ultimate objective of this paper.

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