High-performance flexible nanoscale transistors based on transition metal dichalcogenides

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Two-dimensional (2D) semiconducting transition metal dichalcogenides could be used to build high-performance flexible electronics. However, flexible field-effect transistors (FETs) based on such materials are typically fabricated with channel lengths on the micrometre scale, not benefitting from the short-channel advantages of 2D materials. Here, we report flexible nanoscale FETs based on 2D semiconductors; these are fabricated by transferring chemical-vapour-deposited transition metal dichalcogenides from rigid growth substrates together with nano-patterned metal contacts, using a polyimide film, which becomes the flexible substrate after release. Transistors based on monolayer molybdenum disulfide (MoS2) are created with channel lengths down to 60 nm and on-state currents up to 470 μA μm−1 at a drain–source voltage of 1 V, which is comparable to the performance of flexible graphene and crystalline silicon FETs. Despite the low thermal conductivity of the flexible substrate, we find that heat spreading through the metal gate and contacts is essential to reach such high current densities. We also show that the approach can be used to create flexible FETs based on molybdenum diselenide (MoSe2) and tungsten diselenide (WSe2).

The Internet of Things (IoT) envisions electronics physically present in all aspect of our daily lives—providing information about the machines and environment around us, as well as our own bodies. Some of the devices required for this can be created with rigid silicon, but there is also a need for electronics with non-planar form factors2–4, in other words, devices that are thin and light and can be conformally attached to objects with unusual shapes, on human skin or implanted in the body5. This will require easy to integrate, and capable of low-power consumption and high performance5–7.

Two-dimensional (2D) materials are good candidates for flexible electronics due to their lack of dangling bonds, good electron or hole mobility in atomically thin (sub-1-nm) layers, low short-channel effects and ability to be transferred onto different substrates8–10. Although, channel lengths on flexible substrates11, as well as the fact that the TMD transfer process can lead to contamination or damage of the atomically thin material12–15. The shortest flexible MoS2 transistors reported so far, which had channel lengths of ~68 nm, used three-layer exfoliated material and had on-state currents of 135 μA μm−1, probably limited by their contact resistance16. Currently, for large-scale practical applications, MoS2 must be synthesized by chemical vapour deposition (CVD). The shortest channel length reported for devices based on CVD MoS2 is ~750 nm (with a gate length of ~500 nm) with 85 μA μm−1 on-state current, which is also contact-limited17. Beyond MoS2, there have also been some reports on flexible transistors based on other TMDs, such as WSe218–20. Importantly, achieving a high transistor on-state current requires both short channels and low contact resistance, for example, by doping the TMD21–23 and optimizing the metal–TMD interface24,25.

In this Article, we report flexible monolayer MoS2 transistors with on-state currents up to ~470 μA μm−1 at drain–source voltage V_DS = 1 V in sub-100-nm channels. The devices are created by transferring the TMDs together with lithographically predefined metal contacts onto flexible substrates. The TMD is grown using CVD on a SiO2/Si substrate and the critical contact separation is defined while the channel is still on the rigid substrate, enabling the fabrication of nanoscale devices. Flexible polyimide (PI) is spin-coated onto the pre-patterned structures and they are released together, with the remaining process continuing on the PI. The approach is also used to create flexible FETs based on MoS2, WSe2 and MoSe2, all of which have staggered device configurations26: that is, the channel is sandwiched between the source/drain and the gate.

Transfer process with embedded contacts
The TMDs were grown by CVD on SiO2/Si substrates as previously reported27–30. Information on substrate preparation and MoS2 properties, including Raman, photoluminescence (PL), atomic-force microscopy and layer homogeneity, is provided in Supplementary Sections 1 and 2, and details about the Au liftoff process are given in the Methods. Subsequently, we lithographically patterned Au metal contacts on top. We chose Au without an adhesion layer because of its good contact resistance24 (Rc) to MoS2 and its low adhesion to SiO231. Both the Au and TMD (lacking out-of-plane dangling bonds) can be released from the SiO2 surfaces without damage, as shown below. After the contacts were defined, we conformally covered the pre-patterned structures with ~5 μm of PI, which was released, together with the TMD and Au, from the SiO2/Si growth substrate by immersion and agitation in deionized (DI) water (Methods). Although performing the entire device fabrication before transfer could be envisaged, most dielectrics will stick to the SiO2 substrate.

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and complicate the release procedure. Thus, we decided to continue processing the gate stack after transfer to the PI substrate (as further described below and in the Methods).

Figure 1a shows the SiO_2/Si substrate with TMD, contacts and PI, Fig. 1b displays the release schematic and Fig. 1c shows the transparent PI substrate after release. We note that a similar damage-free transfer of MoS_2 layers (without contacts) for coplanar nanometre-sized FETs has recently been demonstrated over 4-inch wafers, indicating that this approach could be scaled up.

The optical image in Fig. 1d shows that the TMD (here MoS_2) is completely delaminated from the area that had been covered by PI on the SiO_2/Si substrate. Note that agitation in DI water also causes some delamination of MoS_2 in the area that is not covered by PI (for example, at the bottom left and edges). We can transfer continuous (Fig. 1e) as well as pre-patterned (Fig. 1f) MoS_2 films with embedded contacts, enabling us to realize devices based on a number of fabrication approaches. As shown later, we have fabricated FETs with MoS_2, MoSe_2, and WSe_2, where only the contacts were patterned before transfer, minimizing the process steps on unprotected TMDs (Fig. 1e and Supplementary Section 3), but leading to channel widths greater than the electrode widths (referred to as type A devices). We also realized FETs where the MoS_2 channel was predefined by reactive ion etching (RIE) before transfer (Fig. 1f), which enables accurate channel width definition (referred to as type B). Further details on device fabrication are provided in the Methods.

To confirm that the TMDs remain intact throughout the transfer process, we performed extensive Raman spectroscopy and PL measurements before and after transfer (Supplementary Section 4). We observe that the PI background signal and quenching on Au surfaces affect the resolution and visibility of TMD peaks. The Raman and PL spectra on SiO_2/Si indicate TMDs with monolayer thickness; however, MoSe_2 also had regions with bilayers (Supplementary Section 4). Generally, the absence of major changes in the Raman and PL results before and after transfer indicates that mono- as well as multilayer TMDs can be readily transferred with this technique, without apparent damage. In addition, we found that the surface roughness does not discernibly increase after transfer, preserving root-mean-square roughness below 0.5 nm (Supplementary Section 4). The electrical results presented in the following further confirm the excellent viability of this transfer approach.

**Flexible top-gated FETs**

After the transfer process, the material stack was flipped with the source and drain contacts embedded in the PI substrate and the TMD semiconductor on top. To prevent contamination of this exposed TMD surface, we deposited an Al_2O_3 gate dielectric immediately after the transfer process and before any other patterning steps. The fabrication process was finalized with gate metal definition, leading to a staggered device geometry. For MoS_2, FETs of type A, we used RIE to pattern the channel and gate dielectric together, after gate metal deposition, but channels of type B devices were already patterned by RIE before transfer (additional fabrication details are provided in the Methods). The device cross-section is schematically shown in Fig. 2a, and Fig. 2b–d displays optical images of the WSe_2, MoSe_2, and MoS_2 FETs. Measured transfer and output characteristics of micrometre-scale FETs with WSe_2, MoSe_2, and MoS_2 FETs were already patterned by RIE before transfer (additional fabrication details are provided in the Methods). The device cross-section is schematically shown in Fig. 2a, and Fig. 2b–d displays optical images of the WSe_2, MoSe_2, and MoS_2 FETs. Measured transfer and output characteristics of micrometre-scale FETs with WSe_2, MoSe_2, and MoS_2 FETs were already patterned by RIE before transfer (additional fabrication details are provided in the Methods).

The extracted device parameters for all TMDs are listed in Table 1. Threshold voltage (V_TH) and extrinsic field-effect mobility (μ_FE,ext) were estimated at the maximum transconductance (g_m), using the measured Al_2O_3 gate oxide capacitance (C_ox = 0.21–0.32 μF cm⁻²) from the TMD FETs obtained in accumulation (Supplementary Section 5). The ~1.7-μm-long monolayer WSe_2 FET exhibits a maximum on-state current of I_DS = 3.6 ± 0.1 μA μm⁻¹ (the source of the error bars is explained below) at a drain–source voltage of V_DS = 1 V, which is over twice larger than the highest previously reported for flexible WSe_2 (using bilayer exfoliated material). The ~2.7-μm-long MoSe_2 FET reaches I_DS = 4.2 ± 0.4 μA μm⁻¹ at V_DS = 4 V, which is also a clear demonstration of flexible MoSe_2 FETs.

The mobility and width-normalized current of type A devices are listed with error bars because their channel width was not patterned and they were subject to (some) current spreading effects,
which we account for with numerical simulations (Supplementary Section 15). For example, the unpatterned hexagonal crystals for the Se-based FETs are shown in Fig. 2b,c. Their measured data are shown in plain current units (μA) in Fig. 2d,e and Fig. 2f,g, respectively, but the error bars are included when presenting their width-normalized current (μA·μm⁻¹), for example in Table 1.

The correction is not needed for our type B devices because of the optimized geometry and modified fabrication process. Hence, Fig. 2h,i for type B MoS₂ FETs, is displayed in width-normalized units and the better quality of this material also enables larger \( I_g \approx 67.3 \, \mu A \cdot \mu m^{-1} \) in a ~4.7-μm-long FET at \( V_{DS} = 5 \, V \). In comparison, type A MoS₂ FETs had higher subthreshold swing (SS) and off-state current, reducing their on/off ratio (Table 1 and Supplementary Section 6). Furthermore, the process flow for type B devices facilitates the fabrication of circuits, and an example inverter is shown in Supplementary Section 7. Comparing device hysteresis, we find it ranges from ~0.1 V (WSe₂) to ~1.6 V (MoSe₂) for all devices and TMDs, indicating that the additional patterning step of type B devices does not deteriorate TMD interfaces (Supplementary Section 8). We have also verified the stability of the flexible TMD FETs under tensile bending and found no notable changes for a bending radius of 4 mm or a tensile strain of ~0.063% (Supplementary Section 9).

**Nanoscale flexible MoS₂ transistors**

As MoS₂ has the most mature growth process with the highest electrical quality and best surface coverage, we further studied its FET scaling down to ~60 nm (Supplementary Section 10) with electron-beam lithography (EBL) for source–drain contact patterning. Importantly, this nanoscale resolution is enabled by our approach, wherein the contact patterning is first performed on the atomically smooth SiO₂/Si surface instead of the PI, which is prone to waviness, enhanced charging effects and possible damage in EBL.⁰ We also verified that this process is benign to MoS₂, performing Raman and PL measurements before and after EBL, finding no apparent evidence of damage to the MoS₂ (Supplementary Section 11). The remaining device fabrication and transfer were performed as described above.
The extrinsic field-effect mobility \( \mu_{\text{FE,ext}} \) and threshold voltage \( V_t \) were extracted from the maximum \( g_m \) in the linear operating regime at a drain–source voltage \( V_{DS} = 0.1 \text{V} \). The subthreshold swing (SS) value denotes the extracted minimum. We note some \( V_t \) variability, which is not unusual for 2D transistors in academic fabrication facilities. *Values corrected for current spreading.

The measured output characteristics (Fig. 3c,f) show signs of self-heating and velocity saturation23,39 due to the onset of current saturation at lower \( V_{DS} \) with higher gate–source voltages \( V_{GS} \) which is similar to the self-heating of MoS2 FETs on SiO2/Si substrates. We estimate that the temperature of this FET channel exceeds 350 °C at the peak input power in Fig. 3f, but the PI remains below its glass transition temperature because the device heat spreading occurs primarily through the gate stack and contacts (Supplementary Section 12). To gain additional insight into intrinsic device parameters, we extracted \( I_D \) (at an overdrive \( V_{GS} = V_{DS} - V_t = 8 \text{V} \)) and \( \mu_{\text{FE,ext}} \) for channel lengths from ~60 nm to ~10 µm in Fig. 3d,e. Measuring numerous devices allows us to comment both on ‘typical’ and ‘best-case’ device performance. We used a model that relates \( I_D \) and \( \mu_{\text{FE,ext}} \) to \( L \).

### Table 1 | Electrical parameters of flexible FETs

| Device       | Channel length (nm) | \( \mu_{\text{FE,ext}} \) (cm²V⁻¹s⁻¹) | \( I_D \) at \( V_{GS} = 1 \text{V} \) (µAµm⁻¹) | \( V_t \) (V) | SS (mVdec⁻¹) | On/off ratio |
|--------------|---------------------|--------------------------------------|---------------------------------------------|---------------|--------------|-------------|
| WSe₂ (type A)| 1,700               | 4.1 ± 0.1ᵃ                         | 3.6 ± 0.1ᵇ                                  | 1.6               | 380                        | 3 × 10⁶      |
| MoSe₂ (type B)| 2,700               | 1.9 ± 0.1ᵇ                         | 2.1 ± 0.1ᵇ                                  | -2               | 430                        | 1×10⁶        |
| MoSe₂ (type A)| 4,700               | 16.2 ± 0.1ᵇ                        | 5.5 ± 0.9ᵃ                                  | 3.9               | 1,700                      | 3.6 × 10³    |
| MoSe₂ (type B)| 4,700               | 24                                  | 21                                           | -5.2              | 850                        | 1×10⁴        |
| MoS₂ (type A)| 112                 | 8.1                                 | 229                                          | 0.6               | 730                        | 2×10⁴        |
| MoS₂ (type A)| 82                  | 23.2 ± 1.4ᵃ                         | 466 ± 4.0ᵃ                                  | 6                 | 1,000                      | 4×10⁴        |

Figure 3a presents a top-view optical image of a nanoscale channel after transfer and a post-fabrication-device cross-section. The cross-section shows that the Al₂O₃ gate dielectric covers the planar source and drain electrodes, including the ~100-nm nanogap between them, illustrating the absence of steps in the surface topography enabled by this fabrication technique with contacts embedded in the flexible substrate (Supplementary Section 2). Electrical measurements of a similar type B device with ~112-nm-long channel are shown in Fig. 3b,c, showing a good on/off ratio (>10⁸), high \( I_D \approx 303 \text{µAµm}⁻¹ \) (at \( V_{DS} = 1.4 \text{V} \)) and \( \mu_{\text{FE,ext}} \approx 8.1 \text{cm²V}⁻¹\text{s}⁻¹ \). The mobility appears smaller than in micrometre-scale devices due to the greater contribution from \( R_C \), as discussed in the following (for other device parameters see Table 1).
Fig. 4 | Benchmarking flexible FETs. a, b, Extrinsic-field-effect mobility $\mu_{FE,ext}$ (a) and drain current $I_D$ (at $V_{DS} = 1 V$) (b) for flexible MoS$_2$ transistors as a function of channel length ($L$) (3L: 12, 14, 31). Three studies reported $\mu_T$, excluding contact resistance, with the y-function method (YF). A few points correspond to three-layer (3L) MoS$_2$, one of them at $V_{DS} = 2 V$, one ($L = 68 n m$) at unspecified voltage. Most CVD-grown MoS$_2$ are monolayers (1L); the other thicknesses are as labelled up to five layers (5L), and unlabelled points are all thicker exfoliated channels. All thicknesses and more details from other works are listed in Supplementary Section 16. The MoS$_2$ films in this work are mostly monolayers with some multilayer islands (up to 34%; Supplementary Section 1). c, Reported $I_D$ (at $V_{DS} = 0.5 V$) versus on/off current ratio for flexible FETs with channel $L \leq 200 n m$ (refs. 43, 54–58). For comparison, two data points are shown for graphene (Gr), two for crystalline silicon (c-Si), two for oxide semiconductors (indium tin oxide (ITO) and indium gallium zinc oxide (IGZO)) and the others for MoS$_2$ (our CVD monolayer data and two reports on 3L exfoliated). Blue and red symbols are type A and B devices from this work, respectively. Error bars on blue symbols represent uncertainty from current spreading correction.

$R_C$ and the intrinsic field-effect mobility $\mu_{FE}$. (The adapted model, the $V_T$ and $\mu_{FE,ext}$ extractions are described in Supplementary Sections 5 and 14.) Figure 3d,e shows that $I_D$ plateaus and $\mu_{FE,ext}$ decreases at sub-1-μm channel lengths, which clearly indicates that these devices are limited by $R_C$. The dashed black lines show the model for ‘typical’ type B devices (red circles), which we fitted with an average $\mu_{FE}$ (~11.5 cm$^2$V$^{-1}$s$^{-1}$) for micrometre-scale devices where the impact of $R_C$ is small, and by setting $R_C = 5 k\Omega$ to follow the middle of the distribution for shorter $L$.

The solid black lines in Fig. 3d,e are based on a similar approach but using higher $\mu_T$ (~27 cm$^2$V$^{-1}$s$^{-1}$) to fit the best-performing type B devices with $R_C = 2.3 k\Omega$. Also taking into account the ‘best’ type A devices (blue symbols and error bars, corrected for current spreading), we fit $R_C = 250 \Omega / \mu m$ for one device (at $L = 82 n m$) and a slightly higher $\mu_T = 30 cm^2 V^{-1} s^{-1}$, generating the blue dotted lines. The FET with the highest on-state current achieves an impressive $I_D = 466 \pm 40 \mu A / \mu m$ at $V_{DS} = 1 V$ (Supplementary Section 13 provides electrical data and Supplementary Section 15 the current spreading correction), and its electrical characteristics are shown in Fig. 3f and Supplementary Fig. 22b. The presence of a ‘hero’ device is not surprising when dozens (or hundreds) of devices are measured, being both an indicator of academic fabrication and growth variability, and of the promise of these 2D semiconductors if variability challenges are eventually mitigated by industrial optimization. (We note that our type A and B devices have similar variability; Supplementary Section 13.)

Our estimated best-case $\mu_T$ and $R_C$ are comparable to the best reported values for monolayer MoS$_2$ on flexible substrates and on SiO$_x$/Si rigid substrates, respectively. The highest on-state current, $I_{DS}$, is over three times greater than in previous reports for flexible MoS$_2$ FETs, similar to the best TMD FETs on rigid substrates, and even comparable to flexible FETs based on graphene and crystalline Si (c-Si). Moreover, this fabrication technique enables us to scale flexible MoS$_2$ FETs to the shortest channel lengths reported so far (Supplementary Fig. 22c)

Figure 4 displays benchmarking of our flexible MoS$_2$ transistors compared to other technologies on flexible substrates. Displaying the extrinsic mobility $\mu_{FE,ext}$ and drain current $I_D$ (at $V_{DS} = 1 V$, unless noted otherwise) for flexible MoS$_2$ FETs versus $L$ (Fig. 4a,b) reveals that nanoscale devices have received little attention until now (values are listed in Supplementary Table 2) (16, 17, 32, 44–5). Figure 4c compares the on-state current and on/off ratio of the few existing sub-200-nm flexible FETs (at $V_{DS} = 0.5 V$, unless noted otherwise), showing the good performance of our MoS$_2$, even next to high-mobility materials (values are listed in Supplementary Table 3) (13, 54–56). The on/off ratio of MoS$_2$ is many orders of magnitude higher than graphene (on/off <10), making MoS$_2$ more suitable for low-power applications among existing 2D channel materials. Compared to flexible c-Si FETs, flexible TMD FETs have a fundamentally different structure, with a sub-nanometre thin channel without out-of-plane dangling bonds. This enables shorter channel lengths, better mechanical robustness and potentially lower cost (due to the simple transfer processes), all of which are advantageous for higher-performance and lower-power operation on flexible substrates.

Conclusions

We have reported high-performance MoS$_2$ transistors on flexible substrates, created using a transfer process that includes nano-patterned contacts. The approach allows devices with channel lengths as low as ~60 nm to be fabricated. Our devices exhibit drive currents up to ~470 μA / μm at $V_{DS} = 1 V$, among the highest for any monolayer 2D semiconductor, including those on rigid Si substrates. The on-state current is also comparable to those of flexible graphene and c-Si transistors, while maintaining an on/off current ratio over 10$^4$. The high current is achieved despite the low thermal conductivity of the PI substrate, as the short channel devices benefit from heat spreading through the gate and contacts. We have also shown that the fabrication technique can be applied to other 2D semiconductors, creating flexible MoSe$_2$ and monolayer WSe$_2$ FETs. Our approach could be used as a template for making flexible transistors with other materials that have few demonstrations of short-channel devices, including oxides, organics and carbon nanotubes. Together with further optimization of electrostatic control (such as thinner gate dielectrics or double gates) and reduced parasitics (such as lower parasitic capacitance; Supplementary Section 17), the technique could allow flexible TMD electronics to be incorporated into low-power and high-performance IoT applications.

Methods

Raman and PL measurements. The Raman and PL measurements were performed on a HORIBA Scientific LabRAM HR Evolution spectrometer using an excitation
Device fabrication including transfer process and liftoff procedure. Fabrication of type A devices, channel defined last. The TMDs were grown on SiO2/Si, for acquisition time, accumulations, laser power and optical grating we used s = 3, 0.14 mW and 1.800 s.cm⁻¹, and the spot size was less than 1 μm. For the Raman measurements after transfer on PI or Au/PI surfaces, the acquisition time was increased to 45 s, while the other parameters remained the same. For PI measurements on SiO2/Si, PI and Au/PI, the acquisition time, accumulations, laser power and optical grating were s = 3, 0.14 mW, 600 gr.cm⁻¹⁻¹.

Device fabrication including transfer process and liftoff procedure. Fabrication of type B devices, channel defined before transfer. Up to the source and drain contact metallization, the fabrication of the type B device is the same as for the type A device. However, after source and drain metallization, the MoS2 channels were patterned by RIE (Oxford 80 RIE) in CF₄/O₂, at gas flows of 50 s.cm⁻¹:50 s.cm⁻¹, power of 150 W and pressure of 30 mtorr. After nitrogen blow-drying the substrate, a 1.5-nm-thick Al blanket film was deposited on top by electron-beam evaporation. This film acts as a seed layer for the subsequent atomic-layer deposition of an Al₂O₃ gate dielectric at 200°C. Note that we used 35 nm Al₂O₃ for the MoS₂ devices and 23 nm-thick Al₂O₃ for the MoSe₂ and WSe₂ devices. This yields Cₓ = 0.21–0.23 μF/cm², as directly measured in Supplementary Fig. 12. The oxide thicknesses were chosen to ensure higher device yield and to have numerous FEts for measurement. After the atomic-layer deposition, the gate metal was deposited by electron-beam evaporation of Ti/ Au (5/60 nm) and patterned by optical lithography and liftoff. This concluded the fabrication for MoSe₂ and WSe₂ devices. For MoS₂ devices, as a final step, the Al₂O₃ and MoS₂ were patterned together using RIE (Oxford 80 RIE) in CF₄/O₂, at gas flows of 50 s.cm⁻¹:50 s.cm⁻¹, power of 150 W and a pressure of 30 mtorr.

Liftoff procedure. The source and drain contacts in this work consist of bare Au, which is known to have poor adhesion, especially to SiO₂. Thus, we needed to perform this step carefully to avoid delamination of the electrodes. The procedure is the same for liftoff after optical lithography and after EBL. In both cases, we used a double layer of resist (LOL2000 and SPR3612 from Shipley for optical lithography, see next section for EBL), which provided an undercut in the resist stack. Thus, the Au, which was evaporated on top of the entire sample, is disconnected over the resist steps. This is important, because we wish to avoid strong mechanical forces (for example, no sonication), which could delaminate either the Au or the TMD. After the Au was evaporated on top of the resist stack, we soaked the samples for >12h in N-methyl pyrrolidone (for optical lithography) or acetone (for EBL). The Au was then gently removed from the undesired locations by pulsing the solvent over the sample surface with a pipette. This step lifted off most metal (>95% by visual inspection), but to remove remaining stubborn metal residue, the samples were immersed in acetone followed by isopropanol, and gentle solvent pulsing with a pipette was applied in each solvent. Finally, the samples were removed from the isopropanol and nitrogen blow-dried.

EBL on MoS₂. We used a double layer of poly(methyl methacrylate) (PMMA) for liftoff patterns defined by EBL. The bottom and top layer were 50 nm-thick 495 K A2 PMMA and 200 nm-thick 950 K A4 PMMA, respectively. EBL was performed on a JEOL JBX 6300 lithography system at a dose of 900 μC·cm⁻² and an acceleration voltage of 100 kV.

Electrical measurements. All transistors were tested with a Keithly 4200 system on a probe station in ambient air. For the bending experiments, the substrates were attached to a metallic cylindrical rod with a radius of 4 mm.

Data availability

The data that support the plots within this paper and other findings of the study are available from the corresponding author upon reasonable request.

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Author contributions

A.D. conceived the work and performed the device fabrication and characterization. A.D. and S.V. developed the TMD transfer process. R.W.G. performed the MoS2 CVD growth and C.S.B. the WSe2 and MoSe2 CVD growths. V.C. carried out the electron beam lithography and atomic-force microscopy. A.D. and K.S. performed optical material analysis with help from K.B. H.R.L. carried out scanning electron microscopy. C.R. set up numerical current spreading simulations and thermal simulations with E.P. A.D. analysed all data and wrote the manuscript with help from V.C., C.K. and E.P. All authors revised and commented on the manuscript. E.P. supervised the work.

Competing interests

The authors declare no competing interests.

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High-performance flexible nanoscale transistors based on transition metal dichalcogenides

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Supplementary Information

High-performance flexible nanoscale transistors based on transition metal dichalcogenides

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1. MoS₂ film properties, growth conditions, SiO₂/Si substrate preparation

MoS₂ was synthesized by CVD growth as described in prior work.²⁷,²⁸ The SiO₂/Si substrates were pretreated by hexamethyldisilazane (HMDS) vapor to provide a hydrophobic surface for the subsequently applied seeding promoter (PTAS, i.e. perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt dissolved in DI water and dried on a hot plate) on the edges of the chip, which prevents spreading towards the chip center. The same substrate treatments were applied for the growth of the other TMDs. The MoS₂ growth from solid precursors (MoO₃ and S) then forms large single crystal triangles with sizes in the order of tens of microns which coalesce into a continuous film in the chip center, and non-continuous areas closer to the chip edge (see Fig. 1 in previous work²⁷).

Although the MoS₂ film can essentially be characterized as a monolayer film, some small multilayer islands and overgrowth are present at grain boundaries or nucleation sites. Supplementary Fig. 1 and 2 display Raman and photoluminescence (PL) mapping of a multilayer region and grain boundary, respectively, each surrounded by monolayer MoS₂. As visible from the peak positions, the Raman peak separation is increased in these multilayer regions suggesting a thickness of about 2-3 MoS₂ layers.⁵⁹

The amount of overgrowth and multilayers can vary depending on the location on the sample (edge vs. center) and between growths. This is further quantified by optical image analysis performed on samples used for flexible devices based on the transfer process described in this work. Supplementary Fig. 3a,b shows examples where unpatterned MoS₂ was transferred together with contacts (for Type A devices)
from the center of the chip (a) and from the chip edge (b). The threshold brightness analysis of these images indicates a multilayer coverage of 8-19%. For another example of Type B devices during processing (located in chip center), we find that the multilayer coverage can be as high as 34 %

Supplementary Fig. 1 | Raman and photoluminescence (PL) mapping of an MoS$_2$ multilayer island surrounded by monolayer MoS$_2$ on SiO$_2$/Si. a, Optical image of mapped area. b, PL peak height. c, PL peak position. d, Raman E’ peak height. e, Raman E’ peak position. f, Raman A$_1'$ peak height. g, Raman A$_1'$ peak position.

Supplementary Fig. 2 | Raman and photoluminescence (PL) mapping of an MoS$_2$ grain boundary surrounded by monolayer MoS$_2$ on SiO$_2$/Si. a, Optical image of mapped area. b, PL peak height. c, PL peak position. d, Raman E’ peak height. e, Raman E’ peak position. f, Raman A$_1'$ peak height. g, Raman A$_1'$ peak position.
Thus, for micron-scale devices we can assume that the channel will mostly composed of monolayer MoS$_2$ (including multilayer islands), while most nanoscale channels will likely be monolayers with the occasional chance of continuous bilayers in the channel gap.

2. Surface analysis before and after transfer

To investigate the surface morphology of the MoS$_2$ covered regions before and after transfer, we performed atomic force microscopy (AFM). We find that the as-grown MoS$_2$ has a root-mean-square (rms) roughness of 0.18 – 0.45 nm depending on growth run and sample location, which is comparable to or slightly larger than the nominal SiO$_2$ roughness (Supplementary Fig. 4). In addition, we have also measured the roughness after transfer and capping with 35 nm Al$_2$O$_3$ (evaporated Al seed layer + atomic-layer deposition as described in Methods), which yielded a roughness of 0.39 nm on the MoS$_2$ covered region and 0.44 nm where MoS$_2$ was etched prior to transfer. This confirms that the extremely smooth MoS$_2$ surface is preserved even after transfer. In addition, the AFM reveals that the height difference between MoS$_2$ and Au surfaces is less than 2 nm which confirms that the 45 nm thick contacts are embedded in the substrate and topography is effectively eliminated. This is further visualized in the cross-section SEM image after completed device fabrication in Supplementary Fig. 5, where Al$_2$O$_3$ and Au cover the contacts and channel without any “steps” in surface topography.
Supplementary Fig. 4 | Atomic Force Microscopy (AFM) of a, a single MoS$_2$ triangle on SiO$_2$/Si with a root mean square (rms) roughness of 0.18 nm measured in region of light blue dashed box, b, an MoS$_2$ on SiO$_2$/Si region of coalescing grains with rms roughness of 0.45 nm for MoS$_2$ (light blue dashed box) and 0.23 nm for the bare SiO$_2$ surface (white dashed box), and c, the MoS$_2$ and Au structures on polyimide after transfer and alumina capping (on the entire area) with rms roughness of 0.39 nm on the region with MoS$_2$ (light blue dashed box) and of 0.44 nm on the region where MoS$_2$ was etched (green dashed box).

Supplementary Fig. 5 | Scanning-electron microscopy (SEM) cross-section of a ~100 nm long channel MoS$_2$ transistor, colorized version of Fig. 3a. Red dashed lines show the source and drain electrodes are embedded in the PI, and no “steps” in surface topography can be discerned.

3. Optical microscope images for WSe$_2$ and MoSe$_2$ before and after the transfer process

Supplementary Fig. 6a,c displays the hexagonally shaped WSe$_2$ and MoSe$_2$ crystal grains grown on SiO$_2$/Si substrates after the patterning of source/drain metal contacts, and before the transfer. As visible here, the Au contacts are on top of the TMDs. When the polyimide (PI) is applied on top, it uniformly covers and embeds the contacts. After releasing the PI together with metals and TMDs from the SiO$_2$/Si substrates (main text Fig. 1b), the substrate is flipped over as visible in the numbering (“10”) when comparing Supplementary Fig. 6a,b. This also leads to a reversal of the material stack, where the TMDs are on top of Au/PI or PI, as visible in Supplementary Fig. 6b,d.

4. Raman spectroscopy and Photoluminescence measurements before and after transfer process

The different TMDs were monitored with Raman spectroscopy and photoluminescence (PL) throughout the transfer process to investigate any changes in material properties. Supplementary
Fig. 7a-f display the spectra for MoS\textsubscript{2}, WSe\textsubscript{2} and MoSe\textsubscript{2} before and after transfer. Because we have deposited and patterned metal contacts before the transfer, released all materials together, and flipped the flexible PI substrate, we were able to measure the TMDs after transfer on the metal surface and on the PI surface.

We observed that the measurements directly on PI (without a metal in between the TMD and PI) have a broad background signal, which is absent on the SiO\textsubscript{2}/Si substrates and on Au surfaces. This background signal is in the range where we expect the vibrational modes of the TMDs, and there is, for instance, a significant overlap with the PL energy maximum of monolayer MoS\textsubscript{2} (Supplementary Fig. 7b). The Raman and PL measurements for bare PI (on Si) are shown in Supplementary Fig. 7g,h for comparison. Because of this background signal, the MoS\textsubscript{2} Raman and PL peaks are buried and not visible in our measurements on PI. However, the peaks of WSe\textsubscript{2} and MoSe\textsubscript{2} on the PI surface can be resolved (Supplementary Fig. 7c-f). We note that a Raman laser with shorter wavelength could possibly help to reduce the background signal from PI and improve detection of TMDs.\textsuperscript{60} Further, the insertion of Au between PI and the TMD suppresses this background signal and enables the detection of the Raman signature of all three TMDs.

**Supplementary Fig. 6 | Microscope images of WSe\textsubscript{2} and MoSe\textsubscript{2} with patterned Au metal electrodes.**

- **a**, WSe\textsubscript{2} on SiO\textsubscript{2}/Si before transfer.
- **b**, WSe\textsubscript{2} on polyimide (PI) after transfer.
- **c**, MoSe\textsubscript{2} on SiO\textsubscript{2}/Si before transfer.
- **d**, MoSe\textsubscript{2} on PI after transfer.
Supplementary Fig. 7 | Raman (left column) and photoluminescence (right column) spectra. 

a,b, MoS$_2$. c,d, WSe$_2$. e,f, MoSe$_2$. g,h bare polyimide (PI) on silicon.
We find that the PL peaks for WSe$_2$ and MoSe$_2$ can be detected on PI and Au/PI despite the strong PL quenching that is known to appear on Au surfaces.\textsuperscript{33,34} The PL peak energies of MoS$_2$, WSe$_2$ and MoSe$_2$ are \~1.86 eV, \~1.59 eV and \~1.54 eV, all indicating monolayer thickness.\textsuperscript{29,61-63} While these results were consistent for MoS$_2$ and WSe$_2$ across the substrate, we found that MoSe$_2$ had areas with monolayers and bilayers (~50%) (Supplementary Fig. 8), where the PL peak is shifted towards \~1.50 eV and its intensity is significantly reduced. The noticeable spread in PL energies for MoS$_2$ can be attributed to a variety of effects such as nanoscale bilayer regions\textsuperscript{27,28} or small local variations in strain or doping. For MoSe$_2$, however, we find two sets of PL energy peak positions, which indicate that some areas mainly consist of monolayers and some mainly of bilayers (~50% each).\textsuperscript{29,61}

Changes in the Raman and PL spectra before vs. after transfer can be interpreted as strain release effects or phonon interactions with the bottom surfaces (PI or Au), as will be discussed in the following. For MoS$_2$ on Au, we find that the E’ peak shifts by about -1.8 cm$^{-1}$ and its full-width-half-maximum (FWHM) increases, whereas the A$'$ peak does not change discernably (see Supplementary Fig. 9), which has been observed for non-transferred Au/MoS$_2$ stacks and thus cannot be correlated with the transfer process. Possible mechanisms for this E’ peak shift and broadening can be tensile strain induced from the Au deposition\textsuperscript{64,65} or electron-phonon interactions due to Au plasmons.\textsuperscript{66,67} For WSe$_2$, the changes in the Raman and PL spectra are small (Supplementary Fig. 10). The minor shifts in the PL peak position and Raman E’ peak of about +0.02 eV and -0.1 to -0.2 cm$^{-1}$, respectively cannot be consistently correlated with any strain release during transfer,\textsuperscript{68} and may be related to small effects from interactions with the substrate.\textsuperscript{69} It is difficult to deduce any strain effects from PL and Raman for MoSe$_2$, due to small changes and existence of mono- and bilayers adding uncertainty to the Raman and PL analysis. Still, the results suggest the possibility of slight strain changes in tensile and compressive directions on Au/PI and PI surfaces, respectively (see Supplementary Fig. 11).\textsuperscript{70-72}

Supplementary Fig. 8 | PL measurements before transfer of a, MoS$_2$, b, WSe$_2$ and c, MoSe$_2$. 
Overall, the FWHM of the Raman and PL peaks for all the TMDs do not increase except on Au electrodes, where previously discussed plasmonic effects could be the leading cause. This indicates that the disorder, which would be affected by crystal grain size or defect density, in the materials is not increased throughout the transfer process. This conclusion is also supported by the good electrical

**Supplementary Fig. 9** | Averaged Raman (over ~5 spots on the same chip) a, peak positions and b, Full-width-half-maximum (FWHM) of MoS$_2$ before transfer (as-grown, on SiO$_2$/Si substrate) and after transfer (on Au/PI).

**Supplementary Fig. 10** | Averaged (over ~5 spots on the same chip) a, Raman and b, photoluminescence (PL) peak positions of WSe$_2$ before and after transfer. Averaged full-width-half-maximum (FWHM) for c, the Raman and d, the PL measurements.
9

properties, which are comparable on the materials after transfer with those before transfer (i.e. on rigid SiO\textsubscript{2}/Si substrates) from previous studies using the same CVD material type.\textsuperscript{27,28,35}

5. Mobility, Gate Capacitance, and Threshold Voltage Extraction

We performed the extraction of the extrinsic field-effect mobility $\mu_{\text{FE,ext}}$ and threshold voltage $V_T$ from the $g_m$ maximum based on the following equation (valid for small drain-source voltages $V_{DS}$):

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_{\text{FE,ext}} C_{ox} V_{DS} W}{L},$$

where the $I_D$ plotted vs. $V_{GS}$ can be fitted linearly to obtain $\mu_{\text{FE,ext}}$. Furthermore, the intercept with the $V_{GS}$ axis yields $V_T$.\textsuperscript{75,76} The channel width $W$ and the channel length $L$ are given by the device geometry. The gate oxide capacitance per unit area ($C_{ox}$) is determined by connecting source and drain of the

Supplementary Fig. 11 | a, Averaged Raman (over ~5 spots on the same chip) and b, photoluminescence (PL) peak positions of MoSe\textsubscript{2} before and after transfer. Averaged full-width-half-maximum (FWHM) for c, the Raman and d, the PL measurements (~10 spots across two chips). Note, missing data e.g., for the Raman E\textsubscript{12G} peak on PI means that these peaks could not be detected on that particular surface.
transistors to ground, and applying a voltage to the gate electrode. We then perform small-signal capacitance-voltage (C-V) measurements where the direct-current (dc) voltage is swept while applying an alternating-current (ac) voltage with an amplitude = 100 mV and frequency = 20 kHz. The results for Al₂O₃ gate dielectrics (including 1.5 nm Al seed layer) deposited in 300 cycles (MoS₂ FETs) and 200 cycles (WSe₂ and MoSe₂ FETs) are shown in Supplementary Fig. 12a and b, respectively.

As all transistors are n-channel devices, we estimate the capacitance of the Al₂O₃ gate dielectrics at positive bias voltage (when the channel is in accumulation) by dividing the measured capacitance (Supplementary Fig. 12) with the overlap area of the gate with the source, drain, and semiconductor channel. For MoS₂ FETs the extracted \( C_{ox} \approx 0.21 \mu \text{F cm}^{-2} \) or an equivalent oxide thickness (EOT) \(~16.4 \text{ nm}\), and for WSe₂ and MoSe₂ FETs we obtain \( C_{ox} \approx 0.32 \mu \text{F cm}^{-2} \) or EOT \(~10.8 \text{ nm}\). Estimating the relative dielectric constant \( \varepsilon_r \) from \( C_{ox} \) and the Al₂O₃ thickness obtained by ellipsometry, we find \( \varepsilon_r \approx 7-8 \), which is in the expected range. Note, the ellipsometric thickness of 200 cycles and 300 cycles of atomic-layer deposited (200°C) Al₂O₃ measured on silicon is around 22 nm and 35 nm, respectively.

However, for the transistor capacitance the 1.5 nm oxidized Al seed layer adds to the overall thickness, while the optical lithography and lift-off process of the top (gate) electrode exposes the Al₂O₃ to the basic photoresist developer which can etch the material, thus slightly reducing its thickness.

6. Flexible MoS₂ Field-Effect Transistors of Type A

Supplementary Fig. 13 displays a top-down optical microscope image and the electrical characteristics of a flexible MoS₂ field-effect transistor (FET) of Type A with 4.7 \( \mu \text{m} \) channel length. The device exhibits an extrinsic field-effect mobility \( \mu_{FE,ext} \approx 14.2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \), on-current \( I_D \approx 5.5 \mu \text{A} \mu \text{m}^{-1} \) at a drain-
source voltage \( V_{DS} = 1 \) V, threshold voltage \( V_T = 3.9 \) V, minimum subthreshold swing \( SS \approx 1.7 \) V dec\(^{-1}\) and on/off ratio \( \approx 3.6 \times 10^3 \). Note that \( \mu_{FE,ext} \) and \( I_D \) have been corrected for current spreading, which is described in Section 15 below.

7. Flexible MoS\(_2\) Inverter based on Type B device fabrication process

The fabrication process for Type B devices further facilitates the realization of circuits because MoS\(_2\) is already defined before gate dielectric deposition and the second metallization, which simplifies connecting bottom and top metallization layers. For instance, these are useful for practical circuits, where the gates and source/drain contacts of some transistors need to be connected (see inset of Supplementary Fig. 14a). Supplementary Fig. 14 shows the characteristics of a proof-of-concept flexible inverter realized with two \( n \)-type MoS\(_2\) transistors.

Supplementary Fig. 13 | MoS\(_2\) field-effect transistors (FETs) of Type A. a, Top-down optical microscope image, white dotted line marks the outline of the MoS\(_2\) area. b, Measured transfer characteristics. Red and blue lines represent drain current, \( I_D \). c, Output characteristics.

Supplementary Fig. 14 | Flexible inverter with Type B MoS\(_2\) transistors. a, Transfer characteristic of the inverter. Inset shows the schematic circuit diagram with transistors T1 (\( W_{ch}/L \approx 20/39.7 \) µm) and T2 (\( W_{ch}/L \approx 300/4.7 \) µm) b, Gain of the inverter shown in a. Inset shows an optical microscope image of the inverter after fabrication.
Comparing hysteresis for Type A and Type B devices, we find similar maximum values of ~1.2 V for MoS$_2$ FETs, which indicates that the additional etch step before transfer does not deteriorate the TMD interfaces (Supplementary Fig. 15a,b). The WSe$_2$ FET displays low hysteresis ~0.1 V (Supplementary Fig. 15c), and the MoSe$_2$ FET has maximum hysteresis of ~1.6 V (Supplementary Fig. 15d).

8. Hysteresis

Comparing hysteresis$^{77}$ for Type A and Type B devices, we find similar maximum values of ~1.2 V for MoS$_2$ FETs, which indicates that the additional etch step before transfer does not deteriorate the TMD interfaces (Supplementary Fig. 15a,b). The WSe$_2$ FET displays low hysteresis ~0.1 V (Supplementary Fig. 15c), and the MoSe$_2$ FET has maximum hysteresis of ~1.6 V (Supplementary Fig. 15d).

9. Bending of flexible TMD FETs

Flexible electronics need to remain unaltered when mechanically deformed, for instance, by bending the substrate. While the ductility of materials matter for the maximum strain that flexible electronics can sustain,$^{79}$ the easiest way to minimize impacts of strain on flexible electronic devices is to minimize the substrate thickness. The strain at a given bending radius can be approximated as$^{80}$

$$strain = \frac{d}{2r},$$

where $d$ represents the thickness of the substrate and $r$ is the bending radius.
where \( d \) is the substrate thickness and \( r \) is the radius of curvature. Thus, by minimizing \( d \) to a few micrometers, the strain at common bending radii on the order of millimeters is minimized. We show this by using a \(~5\) \( \mu \text{m} \) thick PI substrate and bending it to a radius of \(~4\) mm, which results in \(~0.063\)% strain. Consequently, the electrical characteristics of the TMD FETs remain visually unaltered in this condition as shown in Supplementary Fig. 16.

For a detailed quantitative evaluation, we have further analyzed transistor parameters such as drain current \( I_D \), threshold voltage \( V_T \) and transconductance \( g_m \) (see Supplementary Fig. 17). Average \( I_D \) and \( g_m \) changes remain within 10\% of the flat state values and absolute \( V_T \) shifts are mostly < 0.5 V. Given that the applied strain is low even at \( r = 4 \) mm, we conclude that no systematic correlations of strain with device performance parameters can be deduced from these results and we successfully confirmed the bending stability of our devices.

**Supplementary Fig. 16** | Mechanical bending of flexible TMD-FETs. a, Photograph and microscope image (scale bar: 200 \( \mu \text{m} \)) of the measurement setup where the FETs are bent to a tensile radius of 4 mm. Measured transfer characteristics of b, WSe\(_2\) (Type A), c, MoSe\(_2\) (Type A) and d, MoS\(_2\) (Type A). All show no significant changes on substrate bending at the 4 mm radius.

| Material | Diameter | Length | Width | Change |
|----------|----------|--------|-------|--------|
| WSe\(_2\) | 8 mm | 3.7 \( \mu \text{m} \) | 30 \( \mu \text{m} \) | Flat |
| MoSe\(_2\) | 8 mm | 3.7 \( \mu \text{m} \) | 30 \( \mu \text{m} \) | Flat |
| MoS\(_2\) | 8 mm | 82 \( \text{nm} \) | 2 \( \mu \text{m} \) | Flat |
Supplementary Fig. 17 | Quantitative analysis of TMD transistors under bending to a radius of 4 mm. For MoS$_2$, MoSe$_2$ and WSe$_2$, displayed values represent the average and standard deviation of 12, 6 and 3 devices, respectively. 

a, Maximum drain current $I_D$ under bending normalized by its value in flat condition. b, Threshold voltage shift $V_{T,bent} - V_{T,flat}$. c, Maximum transconductance $g_m$ normalized by its value in flat condition.

10. SEM images of transistor channels fabricated with electron-beam lithography (EBL)

We verified the channel dimensions in our transistors by performing scanning-electron microscopy (SEM), which reveals the channel lengths and widths even after the top gate metal is deposited. Supplementary Fig. 18 shows two exemplary Type B devices with channel lengths of ~60 nm and ~400 nm. Note that the surface consists of Au across the whole area displayed since everything is covered with the top gate. Nevertheless it is possible to discern the edges where the MoS$_2$ has been etched. The MoS$_2$ etch mask consists of 2 µm wide metal leads (left and right) and photoresist covering the 1 µm wide channel region, which results in no discernable edge across the MoS$_2$ on Au and the MoS$_2$ in the channel. This is consistent with the absence of “steps” in surface topography from the SEM cross-sections (Supplementary Fig. 5) and AFM images (Supplementary Fig. 4). In our EBL process, the intended channel length was 50 nm, and after evaluating Supplementary Fig. 18a, we
estimate its actual length is $63 \pm 7$ nm. Analyzing 9 devices with sub-micron channels we find that on average the channel length is $\sim 12$ nm longer than intended in our device layout. Thus, we have corrected our extractions and evaluations on devices fabricated by EBL by $\Delta L = +12$ nm. Similarly, we applied $\Delta L = -0.3 \ \mu m$ for devices fabricated by optical lithography based on SEM measurements.

11. Electron Beam Lithography on top of MoS$_2$

Previous reports have indicated that MoS$_2$ could be damaged by highly energetic electron beams which cause strain and defect formation.$^{81-84}$ We investigated this for our EBL process (details in the Methods section) performing Raman and PL measurements before and after the electron beam exposure and development of the poly(methyl methacrylate) (PMMA) layer that was used for the lift-off of the later deposited source/drain metal. Supplementary Fig. 19 displays exemplary Raman and PL spectra, while Supplementary Fig. 20 provides the analysis of Raman and PL peak center shifts as well as the changes in the intensity and FWHM of the PL spectra. We found negligible differences in the Raman spectra. The slight reduction in the PL intensity (Supplementary Fig. 19b) occurs independently of the exposure to the electron beam, and may be caused by PMMA residues or minor effects from processing and aging of the material. Thus, we conclude that here we do not cause significant damage during the EBL process, which may have been due to our 200 nm thick high molecular weight (950K) PMMA layer on top that should reduce the impact energy and dosage of electrons that hit the MoS$_2$. The other parameters of our EBL process and the device fabrication can be found in the Methods section.
Temperature Rise Estimates

We estimate the MoS$_2$ and PI substrate temperature rises in a short-channel ($L \sim 82$ nm, $W_c = 2$ μm) Type A MoS$_2$ device. This particular “hero” device was chosen because it achieved the highest power dissipation, and is therefore expected to reach the highest temperatures during device operation. The operating point simulated is $V_{GS} = 16$ V, $V_{DS} = 1.2$ V and $I_D = 1.225$ mA, which corresponds to the highest power (1.47 mW) demonstrated in Fig. 3f. In order to account for interface thermal resistances and various heat paths and current spreading, we perform 3D steady-state thermal finite element method (FEM) simulations, with the device geometry shown in Supplementary Fig. 21a. The 5 μm thick PI substrate is attached to a heat sink at $T_0 \approx 20$°C via photoresist (SPR 3612, Shipley), which serves as the thermal interface material. For simulations, a thermal contact resistance of 0.1 K·cm$^2$/W was assumed at the bottom of the PI substrate (typical of contact resistances in device packaging$^{85}$), although the exact value has little effect on simulated peak temperatures in this case, because its contribution to the total thermal resistance is much less than the thermal resistance of the PI substrate and the device thermal circuit. The thermal conductivities of the materials used in the simulations and the thermal boundary resistances (TBR) of material pairs are given in Supplementary Table 1.

Supplementary Fig. 20 | Averaged optical material analysis of MoS$_2$ during electron-beam lithography (EBL) with spin-coating and stripping of poly(methyl methacrylate) (PMMA). a, Raman A’ peak center. b, Raman E’ peak center. c, Averaged full-width-half-maximum (FWHM) of the Raman peaks. d, Photoluminescence (PL) peak center. e, PL peak height. f, PL FWHM.

12. Temperature Rise Estimates

We estimate the MoS$_2$ and PI substrate temperature rises in a short-channel ($L \sim 82$ nm, $W_c = 2$ μm) Type A MoS$_2$ device. This particular “hero” device was chosen because it achieved the highest power dissipation, and is therefore expected to reach the highest temperatures during device operation. The operating point simulated is $V_{GS} = 16$ V, $V_{DS} = 1.2$ V and $I_D = 1.225$ mA, which corresponds to the highest power (1.47 mW) demonstrated in Fig. 3f. In order to account for interface thermal resistances and various heat paths and current spreading, we perform 3D steady-state thermal finite element method (FEM) simulations, with the device geometry shown in Supplementary Fig. 21a. The 5 μm thick PI substrate is attached to a heat sink at $T_0 \approx 20$°C via photoresist (SPR 3612, Shipley), which serves as the thermal interface material. For simulations, a thermal contact resistance of 0.1 K·cm$^2$/W was assumed at the bottom of the PI substrate (typical of contact resistances in device packaging$^{85}$), although the exact value has little effect on simulated peak temperatures in this case, because its contribution to the total thermal resistance is much less than the thermal resistance of the PI substrate and the device thermal circuit. The thermal conductivities of the materials used in the simulations and the thermal boundary resistances (TBR) of material pairs are given in Supplementary Table 1.
Material | Thermal conductivity (Wm⁻¹K⁻¹) | Material interface | Thermal boundary resistance (Km²/GW) |
|---------|-------------------------------|-------------------|----------------------------------|
| MoS₂⁸⁶ | 20 (in-plane) | MoS₂ – polyimide⁸⁷ | 100 |
| Polyimide (PI)⁸⁸ | 0.2 | MoS₂ – Au⁹⁷ | 67 |
| Au⁹⁰ | 150 | MoS₂ – Al₂O₃⁸⁹ | 67 |
| ALD Al₂O₃⁹¹,⁹² | 2.5 | Au/Ti – ALD Al₂O₃⁹²,⁹⁵ | 20 |
| | | Au – polyimide⁹⁶ | 400 |

**Supplementary Table 1**: Nominal values of material thermal properties in the simulations. Some thermal boundary resistance (TBR) values not available in literature were approximated by TBRs for pairs of similar and/or better-studied materials, using the larger estimates to model a worst-case scenario. Actual values can vary depending on the material/interface quality and deposition conditions. For Au, the thermal conductivity of films with comparable thickness (not bulk) is used.⁹⁰ For PI and Al₂O₃, the thermal conductivities above room temperature (in the 100-200°C range) are used.

To estimate the temperature rise, we first obtain the current distribution in the device. With \( V_{DS} < V_{GS} - V_T \), the device was assumed to be in the linear region, where the MoS₂ film is characterized by a uniform sheet resistance and the current density is symmetric about the center of the device. With an assumed contact resistance of 400 Ωµm and a contact transfer length of 50 nm (in this “hero” device), 2D electrical simulations were performed as described in Supplementary Section 15 to account for current spreading, and a mobility of 25 cm²V⁻¹s⁻¹ was found to yield the correct device current. The power dissipated per unit area in the channel and across the contact interface were calculated from the simulated current densities and potential drops across the contact-MoS₂ interfaces. This power distribution was then used in the thermal simulation with the complete 3D geometry.

With the nominal thermal properties specified in Supplementary Table 1, the Supplementary Fig. 21 shows the 2D temperature rise distributions (b) in a vertical device cross section, (c) within the MoS₂ film and (d) immediately below the MoS₂ film, showing temperatures in the upper surface of the PI substrate and the Au contacts. We determine a peak temperature rise \( \Delta T \sim 361 \text{ K} \) in MoS₂ and 291 K in PI (The difference between the two is due to the TBR between MoS₂ and PI.). Because TBRs across interfaces depend strongly on materials and the interface quality, the TBRs in the actual device might differ from the values given in Supplementary Table 1. Thus, we performed sensitivity analysis of the peak MoS₂ and PI temperature rise on the TBRs (for all interfaces), in Supplementary Fig. 21e,f.

Supplementary Fig. 21e shows that peak device temperatures are most sensitive to channel-gate insulator (MoS₂-Al₂O₃) and gate insulator-top electrode (Al₂O₃-Ti/Au) TBRs, which indicates that TBRs that control heat flow into the gate stack have the greatest influence. This also indicates the heat
generated in the device spreads (at first) mainly through the gate stack, which has substantial overlap (~10 μm) with the source/drain electrodes. As the heat sink is at the bottom of the PI substrate, after spreading via the gate insulator and top gate, the heat flows back down into PI via MoS₂ and the Au contacts. We note that only ~10% of the heat flows from MoS₂ directly into the PI (the channel-substrate TBR), thus even if the PI surface were severely compromised (e.g. due to heating during

**Supplementary Fig. 21 | Thermal simulations.** a, Simulated Type A device geometry. Inset: closer view of the channel, with the top gate stack not shown. b, Cross section of temperature rise along the direction of current flow. Note the gate has significant overlap with the source/drain. c, Top view of temperature rise in the MoS₂ channel, where the highest temperatures occur. d, Top view of temperature rise at the top of the PI substrate and Au contacts, just below the MoS₂ channel. e, The variation of the device peak temperature rise as a function of the TBR of each material pair. f, The variation of the highest temperature rise in the PI substrate as a function of the TBR of each material pair. In e and f the horizontal dashed lines indicate the peak temperature rise, and the intersection of each curve with this line occurs at each nominal TBR value.
device operation), the device could continue to function by dissipating heat into the gate and contacts. The PI glass transition temperature is 360°C and the decomposition temperature is 620°C. Thus, for the nominal properties in Supplementary Table 1, these devices have additional headroom to operate at higher power, thanks to heat spreading through their gate and source/drain electrodes.

13. Additional Type A Device Data and Overall Variability

The variability of $I_D$ for Type A devices shows a similar distribution compared to devices of Type B (compare Supplementary Fig. 22a with Fig. 3d). The transfer characteristic of the device with the highest on-current is displayed in Supplementary Fig. 22b. The shortest channel lengths which we realized were ~60 nm and an exemplary electrical characteristic and scanning-electron microscopy cross-section are shown in Supplementary Fig. 22c.

In Supplementary Fig. 23 we display the $V_T$ histogram for all MoS$_2$ devices measured. Academic fabrication and growth variations (e.g., variations in S vacancy concentration) cause $V_T$ variability, which could be much improved with industrial process optimization (beyond the scope of this work).

14. Drain current vs channel length in flexible MoS$_2$ FETs and Modeling

The drain current $I_D$ that is obtained when probing a short-channel FET typically has contributions from the channel resistance $R_{ch}$ and contact resistance $R_C$, which makes the accurate extraction of the intrinsic mobility $\mu_{FE}$ difficult. Furthermore, since short-channel devices can be contact dominated, an estimation of $R_C$ is also important. Taking into account $R_{ch}$ and equal source and drain $R_C$ we can estimate the overall resistance $R_{tot}$ (all normalized by device width $W$, in units $\Omega \cdot m$) as follows:

$$R_{tot}/W = 2R_C/W + R_{ch}/W.$$
In the linear transistor operating region (at small $V_{DS}$), $R_{ch}$ can be approximated as

$$R_{ch} = \frac{V_{DS}}{I_D} \approx \frac{L}{\mu_{FE}C_{ox}(V_{GS}-V_T)},$$

where $I_D$, $L$, $\mu_{FE}$, $C_{ox}$, $V_{GS}$ and $V_T$ are the drain current, channel length, intrinsic field-effect mobility, gate oxide capacitance per unit area, gate-source voltage and threshold voltage, respectively. Hence, taking into account $R_{tot}$ when measuring the drain current ($I_{D,meas}$) while applying a voltage between drain and source ($V_{DS,appl}$), we obtain the following for $I_{D,meas}$ (normalized by $W$, unit: A m$^{-1}$):

$$I_{D,meas} = \frac{V_{DS,appl}}{R_{tot}} = \frac{V_{DS,appl}}{2R_C + \frac{L}{\mu_{FE}C_{ox}(V_{GS}-V_T)}}.$$

Thus, we have an expression for $I_{D,meas}$ where the denominator has two competing components which limit the maximum $I_{D,meas}$ that can be obtained. Further, we can find that for ultra-scaled transistors in the limit $L \to 0$, the maximum $I_{D,meas}$ is fully limited by $R_C$. In contrast, at long channel devices (here, $L \geq 10$ µm) the $R_C$ no longer has significant impact and $I_{D,meas}$ is mainly defined by $\mu_{FE}$, given the electrostatics and carrier concentration are fixed ($C_{ox}$, $V_{GS}$ and $V_T$ constant).

In the following, we use this model to identify lower and upper bounds for $R_C$ and $\mu_{FE}$ based on our experimentally obtained results in flexible MoS$_2$ FETs with channel lengths ranging from ~10 µm down to ~60 nm. For that we extract $I_{D,meas}$ at $V_{DS} = 0.1$ V (Fig. 3d) at an overdrive gate voltage ($V_{ov} = V_{GS} - V_T = 8$ V) using a $V_T$ extracted from a linear fit of $g_m$ vs $V_{GS}$. In addition, our model needs $C_{ox}$, which in this case is 0.21 µF cm$^{-2}$ or EOT ~16.4 nm (Supplementary Fig. 12a). With that, we can use
$R_C$ and $\mu_{FE}$ as fitting parameters. We obtain upper bounds for $R_C = 2.3 \, \text{k}\Omega \, \mu\text{m}$ and $\mu_{FE} = 27 \, \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for Type B devices. Taking into account also the best Type A devices, the upper bounds become $R_C = 0.25 \, \text{k}\Omega \, \mu\text{m}$ and $\mu_{FE} = 30 \, \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ indicating a remarkably reduced $R_C$ for the Type A device at $L \sim 82$ nm. Furthermore, it becomes evident that at channel lengths of $\sim 10 \, \mu\text{m}$ the devices are dominated by $\mu_{FE}$ as changes in $R_C$ do not significantly impact $I_D$ (dotted blue and solid black lines converge in Fig. 3d). This gives us the opportunity to fix the $\mu_{FE}$ range at $L \sim 10 \, \mu\text{m}$ and then subsequently fit $R_C$ to the highest data points at the smallest channel lengths, where $R_C$ has a larger impact then $\mu_{FE}$, which gives us an estimate for the best $R_C$. We performed the fitting at $V_{DS} = 0.1$ V (Fig. 3d) to ensure that the devices are in the linear operating regime. We show in Fig. 3c,f that the devices with the highest $I_D$ display effects of self-heating and velocity saturation even below $V_{DS}$ values that would warrant channel pinch-off, which can be commonly observed for sub-100 nm channel length in MoS$_2$ FETs. However, this does not impact our model because we only use it at low $V_{DS}$. The model can also be used to predict the extrinsic field-effect mobility $\mu_{FE,ext}$. The above equations can be modified to:

$$\mu_{FE,ext} = \frac{\mu_{FE}}{1 + \frac{\mu_{FE}C_{ox}(V_{GS}-V_T)^2R_C}{L}}.$$  

We used the same input parameters ($R_C$ and $\mu_{FE}$) for $\mu_{FE,ext}$ as for our $I_D$ fitting. The result shown in Fig. 3e agrees with our extracted $\mu_{FE,ext}$ based on the maximum $g_m$ method, confirming our calculations.

### 15. Correction for Lateral Current Spreading in Type A FETs

In all our TMD FETs of Type A, where the semiconductor width is greater than the electrode width, fringe currents can contribute non-negligibly to the total measured current depending on a number of factors including contact width and spacing, contact resistance and semiconductor mobility. In order to provide an accurate extraction and comparison of $I_D$ and $\mu_{FE,ext}$ for Type A devices and estimate the fringe current effects, we define a dimensionless correction factor:

$$CF = \frac{I_D}{WI_{D,1D}}$$

where $I_D$ is the total current (in $\mu$A), $W$ is width of the contact and semiconductor overlap, and $I_{D,1D}$ is the width-normalized current (in $\mu$A $\mu$m$^{-1}$) in a FET with the same electrical parameters (sheet and contact resistances) but a channel geometry without current spreading. For FETs without a well-defined patterned channel, $CF > 1$, reflecting the contribution of fringe currents. In the linear regime of the transistor, given $R_C$, $\mu_{FE}$ and bias voltages; $I_{D,1D}$ can be calculated as $V_{DS} \cdot W \cdot R_{tot}^{-1}$, with $R_{tot}$
calculated as defined in the previous section. $I_D$ depends on the device and contact geometry as well: we estimate it using 2D finite element method (FEM) simulations using COMSOL Multiphysics to calculate the current distribution. With CF so obtained, width-normalized corrected currents are then

$$I_{D,corr} = \frac{1}{\text{CF}} \frac{I_{D,meas}}{W}.$$  

In FEM simulations, the transistor is assumed to be in the linear region of operation with $V_{DS} \ll V_{GS} - V_T$, so the semiconductor sheet resistance is assumed to be the same everywhere (except where the semiconductor overlaps with contacts), and given by

$$R_{sh} = \frac{1}{\mu_{FE} C_{ox} (V_{GS} - V_T)}.$$  

For purposes of calculating this current distribution, the contacts are assumed to be edge contacts with a contact resistance per unit width of $R_C$. The edge contact assumption is equivalent to contacts with current transfer length $L_T < 50$ nm.

The two unknown electrical parameters that influence CF are $\mu_{FE}$ and $R_C$. However, for devices without a patterned channel, it is not straightforward to extract these directly from electrical data while simultaneously correcting for fringe currents: a range of CF are possible for different combinations of $\mu_{FE}$ and $R_C$. For the lower end of this range, we assume an $R_C = 250 \ \Omega \ \mu m$ (best prior reported results for CVD MoS$_2$ with Au contacts),$^{28}$ and fit $\mu_{FE}$ to get the measured $I_D$. For the upper CF estimate, we assume $\mu_{FE}$ about 2-fold higher than in our best devices (for CVD MoS$_2$ a similar value to best prior results on silicon)$^{28}$ resulting in $\mu_{FE} = 56 \ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for MoS$_2$, $5 \ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for MoSe$_2$ and $10 \ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for WSe$_2$, then fit $R_C$ to get the measured $I_D$. The range of CF calculated this way yields a range of $I_{D,corr}$ and $\mu_{FE,ext}$, which is illustrated as vertical bars in e.g., Figs. 3d and 3e.

An example for the current spreading correction is displayed in Supplementary Fig. 24 for an 82 nm long MoS$_2$ FET. The FEM simulation result displays the current flow paths for two different scenarios of fitted $R_C/\mu_{FE}$ (Supplementary Figs. 24c,e). It is visible that the spreading is more pronounced for the scenario with higher $\mu_{FE}$ and higher $R_C$. In Supplementary Figs. 24d and f, the respective $I_D$ distributions with a hypothetical channel width = electrode width are shown which yield $I_{D,1D}$. For this device, we reported in the main manuscript the average values for these two bounds, which is $\sim 466 \ \mu A \ \mu m^{-1}$. Finally, Supplementary Fig. 24g displays the current distribution in the y-direction (perpendicular to the channel) at the channel center (defined as $x = 0$), which visualizes the current spreading effect for the two different fitting scenarios.
Supplementary Fig. 24 | Numerical current spreading simulations. a, Top view of a Type A device. The regions in gold indicate where the drain and source electrodes are in contact with the semiconductor film. b, Top view of a Type B device. c, The simulated current distribution in a Type A device with 2 µm contact width, 82 nm contact spacing, \(V_{GS} - V_T = 10\) V, \(V_{DS} = 1\) V, \(R_C = 250\) Ω µm, \(\mu_{FE} = 26.8\) cm²V⁻¹s⁻¹. The resulting current is 1.225 mA, with \(I_{D,corr} = 506\) µA µm⁻¹ \((CF = 1.211)\). This set of \(R_C\) and \(\mu_{FE}\) yields the upper bound of our estimated range of \(I_{D,corr}\) values. d, The current distribution in the corresponding Type B device with the same electrical parameters as in c. The width-normalized current is equal to \(I_{D,corr} = 506\) µA µm⁻¹. e, The simulated current distribution in a Type A device with 2 µm contact width, at the same bias conditions as in c but with \(R_C = 821\) Ω µm, \(\mu_{FE} = 56\) cm²V⁻¹s⁻¹. The resulting current is also 1.225 mA, with \(I_{D,corr} = 426\) µA µm⁻¹ \((CF = 1.438)\). This set of \(R_C\) and \(\mu_{FE}\) yields the lower bound of our estimated range of \(I_{D,corr}\) values. f, The current distribution in the corresponding Type B device with the same electrical parameters as in e. The width-normalized current is equal to \(I_{D,corr} = 426\) µA µm⁻¹. g, The current density midway between the contacts \((x = 0)\) as a function of the y-coordinate. Red and blue curves correspond to the Type A devices c and e, respectively.
16. Benchmarking Tables

| Reference          | Synthesis method | Thickness (nm) | Length (nm) | $\mu_{\text{FE}}$ or $\mu_{\text{FE,ext}}$ (cm$^2$V$^{-1}$s$^{-1}$) | $I_D$ at $V_{DS} = 1$V (µA µm$^{-1}$) |
|--------------------|------------------|----------------|-------------|-------------------------------------------------|----------------------------------------|
| Kwon et al. $^{44}$ | exfoliated       | 30-80          | 7000        | 44.8                                            | 4.1                                    |
| Chang et al. $^{45}$ | exfoliated      | 7.9            | 1000        | 30*                                             | 13                                     |
| Yoon et al. $^{46}$ | exfoliated       | 3.075 (5 layers) | 4000        | 4.7                                             | 0.3                                    |
| Lee et al. $^{47}$  | exfoliated       | 1.845 (3 layers) | 800         | 29                                              | NA                                     |
| Salvatore et al. $^4$ | exfoliated     | 3.5            | 4300        | 19                                              | 1.3                                    |
| Yoo et al. $^{48}$  | exfoliated       | 66.5           | 8300        | 83.5                                           | 3                                      |
| Song et al. $^{49}$ | exfoliated       | 79.3           | 22600       | 141.3                                          | 1.2                                    |
| Cheng et al. $^{16}$ | exfoliated      | 1.845 (3 layers) | 116         | NA                                             | 48**                                   |
| Cheng et al. $^{16}$ | exfoliated      | 1.845 (3 layers) | 68          | NA                                             | 135***                                 |
| Ma et al. $^{50}$   | exfoliated       | 18.3           | 17500       | 15.5 ±15.9                                     | 0.32                                   |
| Chang et al. $^{17}$ | CVD              | 0.615 (1 layer) | 750         | 31*                                             | 66                                     |
| Amani et al. $^{51}$ | CVD              | 0.615 (1 layer) | 13000       | 18.9*                                           | 0.2                                    |
| Shinde et al. $^{32}$ | CVD             | 0.615 (1 layer) | 4000        | 6.7 ±20                                         | 2.2                                    |
| Woo et al. $^{52}$  | CVD              | 1.538 (2.5 layers) | 10000     | 9                                               | 1.4                                    |
| Park et al. $^{33}$ | CVD              | 1.23 (2 layers) | 4000        | 17.4                                           | 0.13                                   |

**Supplementary Table 2:** Literature values for flexible MoS$_2$ field-effect transistors used to generate Figs. 4a,b. The synthesis method denotes whether the material was mechanically exfoliated or grown by chemical vapor deposition (CVD). * indicates that in these cases the field-effect mobility $\mu_{\text{FE}}$ was extracted by the y-function method and contact resistance $R_C$ is excluded. For the other cases the method was either not specified or the transconductance $g_m$ maximum method was used which results in an extrinsic $\mu_{\text{FE,ext}}$. The drain current $I_D$ is in most cases specified at a drain-source voltage $V_{DS} = 1$V, unless labeled: ** $V_{DS} = 2$ V, *** $V_{DS}$ not specified.

| Reference            | Channel material | Length (nm) | on/off ratio | $I_D$ at $V_{DS} = 0.5$ V (µA µm$^{-1}$) |
|----------------------|------------------|-------------|--------------|----------------------------------------|
| Park et al. $^{55}$   | graphene          | 140         | 1.5          | 248                                    |
| Yeh et al. $^{56}$    | graphene          | 200         | 8.8          | 516                                    |
| Zhai et al. $^{54}$   | single-crystal silicon (c-Si) | 150       | 6×10$^7$     | 369                                    |
| Shahjerdi et al. $^{43}$ | single-crystal silicon (c-Si) | 30         | 2×10$^3$     | 714                                    |
| Wang et al. $^{57}$   | InSnO (ITO)       | 160         | 7×10$^8$     | 34                                     |
| Münzenrieder et al. $^{58}$ | InGaZnO (IGZO)       | 160        | 7.1          | 119                                    |
| Cheng et al. $^{16}$  | MoS$_2$           | 116         | 2×10$^6$     | 48*                                    |
| Cheng et al. $^{16}$  | MoS$_2$           | 68          | 10$^6$       | 135**                                  |

**Supplementary Table 3:** Literature values for flexible field-effect transistors with channel lengths ≤ 200 nm used to generate Fig. 4c. The drain current $I_D$ is in most cases specified at a drain-source voltage $V_{DS} = 0.5$ V, unless labelled: * $V_{DS} = 2$ V, ** $V_{DS}$ not specified.

17. Estimation of the transit frequency

The scope of this work has been to demonstrate nanoscale flexible TMD transistors with high dc performance. The top gate, fabricated after release of the flexible substrate, is currently still limited by available process accuracy for alignment and feature size in the optical lithography on the ultra-thin flexible substrate. This leads to a large overlap area, and hence high overlap capacitance, which will
limit the ac device performance. The reduction of parasitic overlaps will be addressed in future work. Nevertheless, to evaluate the potential of our devices for high frequency applications, we calculated the expected transit frequency $f_T$ of our transistors with highest performance. We have used the extracted $\mu_{FE,ext}$ at $V_{DS} = 1$ V, which lumps together material parameters ($\mu_{FE}$) and other device parasitics ($R_C$), and hence we can estimate $f_T$, based on the following equation (adapted from other works\textsuperscript{40,101}):

$$f_T = \frac{\mu_{FE,ext} V_{DS} C_{ox} W_{ch}}{2\pi L_{ch} C_{tot}}$$

where $C_{tot}$ is the total capacitance and other variables were previously defined (see Supplementary Section 14). $C_{tot}$ has several components: 1) the total gate oxide capacitance including overlaps ($C_{ox,tot}$), 2) the parasitic capacitance from the sidewall of the gate ($C_{side}$), and 3) the fringing parasitic capacitance from the top surface of the gate ($C_{top}$).

$$C_{tot} = C_{ox,tot} + 2(C_{side} + C_{top})$$

$C_{ox,tot}$, $C_{side}$ and $C_{top}$ are then estimated as follows:\textsuperscript{40,101,102}

$$C_{ox,tot} = C_{ox}(L_{ch} W_{ch} + L_{ov} W_C)$$

$$C_{side} = \frac{W_C \varepsilon_0 \varepsilon_r}{\pi} \ln \left( (K^2 - 1) \left( \frac{K^2}{K^2 - 1} \right)^{K^2} \right)$$

$$C_{top} = \frac{W_C \varepsilon_0 \varepsilon_r}{\pi} \ln \left[ 1 + \frac{L_{ch} + L_{ov}}{t_{ox} + t_{gate}} \right]$$

where $K = 1 + t_{gate}/t_{ox}$ with $t_{gate}$ as the gate metal thickness and $t_{ox}$ as the gate oxide thickness, $\varepsilon_0$ as the vacuum permittivity, $\varepsilon_r$ as the relative gate oxide permittivity, $L_{ov}$ is the gate-source/drain overlap length (see inset of Supplementary Figure 25) and other variables were previously defined.

Thus we calculate $f_T$ as a function of $L_{ov}$, which is displayed in Supplementary Figure 25 taking the corresponding dc data from the devices shown in Fig. 3c.f. Initially, we assumed similar device geometry as in our Type B devices with our measured $C_{ox} \approx 0.21 \mu F \text{ cm}^{-2}$, $\varepsilon_r \approx 8$, $t_{ox} \approx 35 \text{ nm}$ (see Supplementary Section 5), $t_{gate} = 65 \text{ nm}$, $W_{ch} = 1 \mu m$ and $W_C = 2 \mu m$. The inset sketches the different geometrical parameters in top view. The resulting $f_T$ is displayed in red. We find a strong dependence on $L_{ov}$ for large overlaps > 0.1 $\mu m$ where the parasitic overlap capacitance dominates. A general improvement in $f_T$ can be expected when $W_{ch}$ is increased to a value equal to $W_C$ (blue lines, and arrows in Supplementary Figure 25b). In addition, decreasing the gate oxide thickness will only lead to higher $f_T$ if gate-source/drain overlaps are minimized (< 0.1 $\mu m$, green dashed lines, and arrows in Supplementary Figure 25a). We have estimated here the case for reducing our Al$_2$O$_3$ gate dielectric thickness to 5 nm, which would lead to a lower $\varepsilon_r$ due to interface effects and $C_{ox}$ would become $\approx 1 \mu F \text{ cm}^{-2}$.$^{77,103}$ The maximum $f_T$ estimated after these modifications reaches ~26 GHz, and could be increased slightly more by reducing $t_{gate}$ which for instance would lead to ~27 GHz for $t_{gate} = 15$ nm.
These results indicate that the first priority should be minimizing $L_{ov}$ which could be done by advanced lithography techniques or fabrication tricks (like self-alignment\textsuperscript{104}). However, it should be noted that an underlapped device structure, which avoids parasitic overlap capacitance overall could significantly increase the access resistance (and $R_C$)\textsuperscript{17} without a stable and reliable TMD doping technology. Thus, a careful optimization of the device geometry will be necessary. Nevertheless, our estimation of maximum $f_T$ of ~7 GHz and ~27 GHz for the two selected devices demonstrate the potential of high frequency operation in flexible MoS\textsubscript{2} transistors.

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