Exploring a homotopy approach for the design of nanometer digital circuits tolerant to process variations

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**Abstract:** It is known that process parameter variation degrades the performance of nanometer integrated circuits. Process variations reduce the maximum clock frequency operation of the chips. Diverse strategies have been proposed in the literature to overcome this issue, especially optimization algorithms (gate-sizing algorithms). However, convergence related problems have limited their use. In this work, a homotopy approach for the design of nanometer digital circuits tolerant to process variations is proposed. Two optimization strategies are developed in this work, the first based on the homotopy continuation method (HCM) and the second based on a modification of HCM, called in this work reboot homotopy continuation method (RHCM). Three logic paths were implemented to validate the algorithms. The optimization results obtained with the proposed strategies are compared with a Lagrange-Multipliers-based framework. Results obtained from HCM method are equivalent to the obtained with Lagrange Multipliers. On the other side, results obtained from the RHCM method are more accurate than the obtained with HCM and Lagrange Multipliers. Furthermore, the area used to implement the logic paths is lower when RHCM is applied. Moreover, the number of Newton-Rhapson iterations required to find the solutions are lower when RHCM is used; consequently, time computing is also lower.

**Keywords:** process variation, homotopy continuation method, Lagrange Multiplier, gate-sizing, optimization algorithm

**Classification:** Integrated circuits

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1 Introduction

Manufacturing process variation is the cause of deviation in the nominal values of the device physical parameters [1]. These variations change the nominal value of the device electrical parameters. Both physical and electrical parameters define the performance of the electronic circuits and systems. Due to process variations, the performance of a manufactured circuit can be upper or lower to the intentionally designed value [2, 3]. Process parameter variations define the maximum clock frequency and power consumption that the chip can operate [2, 4]. Process variations and the continuous demand for more performance electronic devices and systems have put in struggled the semiconductor industry [5, 6]. Device sizes have scaled-down in the order of few nanometers to fulfill the consumer demand. On this path, manufacturing process variations have surged as one of the main constraints to overcome in the flow of design of integrated circuits. This effect is more prominent as the feature size of devices is smaller.

It is because process variations that the design of modern circuits must follow a well-defined design flow in order manufactured chips be able to work correctly despite process parameter variations. The industry and the academia have dedicated much research effort to developing design methodologies to make circuits robust to the process variations. The use of CAD tools to design optimization of the overall circuit delay has been proposed in the literature [7, 8, 9]. Most common methodologies used to design circuits tolerant to process variations are the gate-sizing optimization algorithms [7, 8, 9], custom design [5, 10, 11], parallel-gates [10, 12] and specialized libraries [13].

Regarding the gate-sizing optimization algorithms, some relevant works are the following: In [14, 15, 16, 17, 18, 19] gate-sizing are based on the geometric
programming technique. In [20, 21] gate-sizing are based on the linear programming and non-linear programming technique respectively. In [22, 23, 24] gate-sizing are based on the Lagrangian Relaxation technique. Other gate-sizing optimization algorithms techniques are proposed in [25, 26, 27, 28]. These aforementioned gate-sizing optimization algorithms have been studied and used to design of digital circuits tolerant to process variations in order to minimize the impact on the circuit yield. However, their use has been limited mainly because of convergence problems.

In this work, a homotopy approach for the optimum gate-sizing on digital circuits, robust to process variations, is proposed. This is implemented in two ways, using the fundamentals of homotopy continuation method (HCM) and using a modification of HCM called in this work reboot homotopy continuation method (RHCM). Both methods find the solution of an equation system which provides the optimum size of the gates of the logic path for a given target delay. A sensitivity delay metric is used to select the gate to be sizing-up. With HCM, the selected gate by the metric is sizing-up until it produces a minimum delay of the logic path. This process is repeated for all gates of the logic path until the target delay of the path is achieved. On the other side, with RHCM, the selected gate by the metric is sizing-up smoothly until the selection metric choses another gate to be sizing-up; then the function to be evaluated is rebooted. This process is repeated for all gates of the logic path until the target delay of the path is achieved. The way RHCM works produces more accurate results than HCM; furthermore, the number of Newton-Rhapson iterations required to find the solution is lower. Moreover, the area cost to implement the logic paths and the time-computing are lower when RHCM is applied.

The remain of this paper is organized as follows. Section 2 gives the fundamentals of the Homotopy continuation method. Section 3 proposes a reboot homotopy approach (HCM) for the design of nanometer digital circuits tolerant to process variations. Section 4 presents the simulation results for different logic paths. Finally, Section 5 outlines the main conclusions of this work.

2 Homotopy continuation method generalities

The homotopy continuation method (HCM) is a technique recommended to solve nonlinear equation systems with multiple solutions [29, 30]. Fig. 1 shows the procedure to give solution of a nonlinear equation system by means the HCM method. This is described step by step as follows,

![Fig. 1. Homotopy continuation method procedure](image-url)
Step 1, define the nonlinear equation that model the problem to solve. It has the form,

\[ f(x) = 0, \quad f : \mathbb{R}^n \rightarrow \mathbb{R}^n \] (1)

where \( x \) represents the \( n \) variable(s) of the problem.

Step 2, define the general homotopy function that transform the problem (1). Its general form is as follows,

\[ H(f(x), \lambda) = 0, \quad H : \mathbb{R}^{n+1} \rightarrow \mathbb{R} \] (2)

where \( \lambda \) is the homotopy parameter.

An specific formulation of (2) is the Newton Homotopy. It is given by

\[ H(f(x), \lambda) = f(x) - (1 - \lambda)f(x_0) = 0 \] (3)

This represents the homotopy map of the problem, where \( x_0 \) is the initial point of the trajectory.

If \( \lambda = 0 \), the homotopy map (is just a trivial problem) is given by,

\[ H(f(x), \lambda) = f(x) - f(x_0) = 0 \] (4)

If \( \lambda = 1 \), the solution is found. It is given by,

\[ H(f(x), \lambda) = f(x) = 0 \] (5)

Step 3, trace the homotopy trajectory (\( \gamma \)). This trajectory represents the continuous homotopy deformation of the homotopy parameter \( \lambda \), from \( \lambda = 0 \) towards \( \lambda = 1 \), i.e., changing the problem from (4) to (5).

Fig. 2 depicts graphically the procedure for tracing the homotopy trajectory (\( \gamma \)). The trajectory tracing is based on hyperspheres [29] following the next steps: 1) a first hypersphere \( (S_0) \) of radius \( r \) is traced over the initial point \( (O_0 = (x_0, \lambda_0)) \). 2) a predictor \( (v_{p0}) \) is applied to approach the centre of the second hypersphere. 3) a Newton-Raphson (NR) corrector is applied to find the real centre \( (O_1 = (x_1, \lambda_1)) \) of the hypersphere \( S_1 \). 4) a new predictor \( (v_{p1}) \) is applied to approach the centre of the third hypersphere. 5) a NR corrector is applied to find the centre \( (O_2 = (x_2, \lambda_2)) \) of the hypersphere \( S_2 \). 6) the predictor and corrector of steps 4 and 5 are repeatedly applied to trace the homotopy trajectory until \( \lambda = 1 \). The radius value \( (r) \) of the hyperspheres contribute the accuracy of the result. The smaller the value of \( r \), the higher the accuracy of the result is.

Step 4, the solution \( (x_s) \) is found when the trajectory intersects the solution line at \( \lambda = 1 \).

3 Reboot homotopy approach (RHCM) for the design of nanometer digital circuits tolerant to process variations

A reboot homotopy-based framework for the design of digital circuits tolerant to process variations was developed. In this case, the function to be evaluated changes (is rebooted) every time the selection metric choses a different gate to be sizing-up. Spatial correlations between gates are accounted for an accurate estimation of the circuit delay.

Fig. 3 shows the flow diagram of the proposed framework. The aim of this framework is to size a logic path to achieve a target timing performance considering
process variations. Four main blocks can be observed in Fig. 3. Block by block is described next: B-1) Firstly, the circuit information and design constraints are defined. The spatial correlation information is also given. B-2) Statistical performance of the logic path \( (\mu_{D_{\text{path}}}, \sigma_{D_{\text{path}}}) \) is computed accounting for the spatial correlation between gates on the chip. The statistical delay of each gate under process variations \( (\mu_{D_{\text{g}}}, \sigma_{D_{\text{g}}}) \) is obtained using a linear model and considers the input slew-rate and loading capacitance \( (C_L) \). These data are computed initially, and each time a gate of the circuit is sizing-up. B-3) The metric (6) is used to select the gate to be sizing-up. This metric evaluates which gate is more sensitivity to the path delay \( (\sigma_{D_{\text{path}}}) \) respect its size \( (KG_i) \). \( KG_i \) is the variable that represents the size of the gate \( i \).

\[
\frac{\partial \sigma_{D_{\text{path}}}(KG_i)}{\partial (KG_i)}
\]

(6)

B-4) The gate sizes are obtained by applying the Homotopy continuation method described in section 2 (See Fig. 1) but with different tracing technique. The trajectory-tracing technique performed in block B-4 is described below. Moreover, the statistical performance of the logic path is computed into block B-4 using B-2.

Fig. 4 depicts graphically the procedure for tracing the homotopy trajectory (\( \gamma \)). The tracing is mapped following the next steps: 1) a first hypersphere \( (S_0) \) of radius \( r \) is traced over the initial point \( (O_0 = (x_0, \lambda_0)) \). The initial function is \( f_1 \). 2) a predictor \( (v_{p0}) \) is applied to approach the centre of the second hypersphere. 3) a Newton-Raphson (NR) corrector is applied to find the real centre \( (O_1 = (x_1, \lambda_1)) \) of the hypersphere \( S_1 \). At this point, the statistical performance of the circuit is again
computed using the gate size obtained. 4) The gate selection metric (6) is again applied. If the gate selected is the same, the function to evaluate is the same $f_1$, but if the gate selected by the metric is other, the function is rebooted (changes) to $f_2$ and the Homotopy trajectory changes from $\gamma_1$-to-$\gamma_2$. In this latter, the first hypersphere to trace is $S_0$. In both cases, the process continues as follows, 5) a new predictor ($\tilde{v}_{\gamma}$) is applied to approach the centre of the next hypersphere. 6) a NR corrector is applied to find the centre of the next hypersphere. At this point, the statistical performance of the circuit is again computed using the gate size obtained. Steps 4 to 6 are repeatedly applied until the Homotopy trajectory composed by a family of trajectories ($\gamma_1 \ldots \gamma_f$) reaches $\lambda = 1$. The radius value ($r$) of the hyperspheres affect the optimization process; then, it can produce changes in the optimization result.

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**Fig. 4.** Reboot Homotopy trajectory ($\gamma$) tracing. Multiple functions are evaluated during tracing.

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### 4 Simulation results for different circuits

The homotopy continuation method (HCM) and the reboot HCM (RHCM) have been applied to different logic paths; and with the purpose to have a reference point, a Lagrange-Multipliers-based framework was also implemented (non-presented in this work). Lagrange-Multipliers is the most common optimization method [22, 23, 24] used on the circuit design.

Fig. 5 shows the three logic paths studied: NAND-based path, NOR-based path and Mixed-gates-based path. All them have a logic depth of ten gates. Each path considers intermediate loading capacitances which are randomly assumed according to the technology node used. The delay performance of logic paths is impacted by process variations of the parameters. Correlated variations in the channel length ($L$), the channel width ($W$), oxide thickness ($Tox$) and purely random variations in threshold voltage ($V_{th}$) are considered. A 15% of variation in $L$, $W$ and $Tox$ and 25% of variation in $V_{th}$ are assumed. The transistor threshold voltages accounting for the effect of random dopant fluctuations (RDF) are also considered. The spatial correlation between parameters of different gates is considered for a proper estimation of the path delay. For the purpose of simplicity and to maintain the
main focus of the analysis on the path delay evaluation, the values of spatial correlations among the gates can be approached assuming that these are placed horizontally one after the other. The statistical performance of the logic paths with nominal dimensions are the following: For the NAND-based path, $\mu_{D_{\text{Path}}} = 549.528$ ps and $\sigma_{D_{\text{Path}}} = 17.183$ ps. For the NOR-based path, $\mu_{D_{\text{Path}}} = 587.18$ ps and $\sigma_{D_{\text{Path}}} = 17.638$ ps. For the MIXED-based path, $\mu_{D_{\text{Path}}} = 517.449$ ps and $\sigma_{D_{\text{Path}}} = 15.709$ ps. The maximum delay of a logic path is defined by summing the mean delay and three times the standard deviation ($\mu_{D_{\text{Path}}} + 3\sigma_{D_{\text{Path}}}$). The target optimization is obtained over the maximum delay of the path.

Fig. 5. Logic paths with a logic depth of ten gates: NAND-based path, NOR-based path and Mixed-gates-based path

Fig. 6 displays the bar graphs of the statistical delay performance of the three logic paths obtained with the Lagrange-Multipliers-based and Homotopy-based frameworks for 20% and 40% of the target reduction of the path delay. The top of the bars gives the mean value ($\mu_{D_{\text{Path}}}$) of the path and inner vertical line in the bar gives the spreading of the delay ($\pm 3\sigma_{D_{\text{Path}}}$). For instance, for the NAND-based path

Fig. 6. Statistical delay performance of the logic paths obtained with Lagrange (LG), homotopy continuation method (HCM) and reboot HCM (RHCM) for 20% and 40% of the target reduction of the maximum path delay. NOM represents the delay performance with nominal dimensions.
(see Fig. 6a), it can be noted that with Lagrange (LG) the obtained optimization is larger than homotopy continuation method (HCM) and reboot HCM (RHCM). This occurs for both target optimizations. This behavior is because the way the methods work; with RHCM the selected gate is smoothly sizing until the selection metric chooses another gate (See section 3). NOM represents the delay performance with nominal dimensions. Similar behavior is obtained for the NOR-based path and MIXED-based path.

Fig. 7 displays the gate size obtained for the three logic paths implemented with Lagrange multipliers and Homotopy approaches for 20% and 40% of target reduction of the path delay, where 1X denotes the nominal dimension of the gate. The considered nominal dimension for the N-network/P-network of the logic gates used are: Inverter 200 nm/280 nm, Nand 200 nm/280 nm and Nor 200 nm/350 nm. From this plots the following notes can be highlighted: 1) Gate sizing pattern from HCM method is similar to the obtained with Lagrange Multipliers. 2) Gate sizing values with RHCM presents a more uniform behavior and according to the loading capacitances of each gate compared to the obtained with HCM and Lagrange Multipliers. This behavior is because with RHCM the selected gate is smoothly

![Gate sizing plots](image)

Fig. 7. Gate sizing of the logic paths obtained with Lagrange (LG), homotopy continuation method (HCM) and reboot HCM (RHCM) for 20% and 40% of target reduction of the maximum path delay.
sizing until the selection metric chooses another gate (See section 3). 3) The area used to implement the logic path is lower when RHCM is used (See Table I). 4) It can be noted that gate sizing pattern for both obtained optimizations (20% and 40%) when RHCM is used have a similar behavior. This behavior suggests that at more optimization the gates can be sizing-up proportionally.

Table I. Characteristics of the frameworks implemented for 20% and 40% of the target reduction of the path delay. Maximum delay of the path, obtained optimization, area cost, NR iterations, and the number of hyperspheres.

| Method               | $\mu_{D_{\text{end}}} + 3\sigma_{D_{\text{end}}}$ (ps) | Obtained optimization (%) | Area (pm$^2$) | Iter. N-R | N° of Spheres |
|----------------------|-----------------------------------------------------|---------------------------|---------------|-----------|---------------|
| NAND-based path      |                                                     |                           |               |           |               |
| Lagrange multipliers |                                                     |                           |               |           |               |
| 20%                  | 459.056                                             | 23.628                    | 1.537         | 33        | –             |
| 40%                  | 352.789                                             | 41.307                    | 2.396         | 62        | –             |
| Homotopy             |                                                     |                           |               |           |               |
| HCM(Sec. 2) 20%      | 460.366                                             | 23.410                    | 1.491         | 184       | 185           |
| HCM(Sec. 2) 40%      | 344.816                                             | 42.634                    | 3.507         | 379       | 377           |
| RHCM(Sec. 3) 20%     | 480.379                                             | 20.080                    | 0.938         | 18        | 14            |
| RHCM(Sec. 3) 40%     | 359.108                                             | 40.256                    | 1.774         | 47        | 30            |
| NOR-based path       |                                                     |                           |               |           |               |
| Lagrange multipliers |                                                     |                           |               |           |               |
| 20%                  | 482.348                                             | 24.644                    | 1.623         | 38        | –             |
| 40%                  | 353.721                                             | 40.413                    | 2.694         | 55        | –             |
| Homotopy             |                                                     |                           |               |           |               |
| HCM(Sec. 2) 20%      | 482.978                                             | 24.546                    | 1.511         | 153       | 152           |
| HCM(Sec. 2) 40%      | 378.825                                             | 40.817                    | 2.956         | 392       | 395           |
| RHCM(Sec. 3) 20%     | 501.794                                             | 21.606                    | 1.023         | 17        | 14            |
| RHCM(Sec. 3) 40%     | 382.596                                             | 40.228                    | 2.098         | 43        | 31            |
| MIXED-based path     |                                                     |                           |               |           |               |
| Lagrange multipliers |                                                     |                           |               |           |               |
| 20%                  | 427.134                                             | 24.344                    | 1.231         | 33        | –             |
| 40%                  | 338.250                                             | 40.088                    | 2.208         | 65        | –             |
| Homotopy             |                                                     |                           |               |           |               |
| HCM(Sec. 2) 20%      | 432.036                                             | 23.475                    | 1.140         | 159       | 156           |
| HCM(Sec. 2) 40%      | 336.044                                             | 40.478                    | 2.175         | 571       | 501           |
| RHCM(Sec. 3) 20%     | 449.873                                             | 20.317                    | 1.055         | 26        | 16            |
| RHCM(Sec. 3) 40%     | 335.060                                             | 40.653                    | 2.321         | 51        | 40            |
applied; moreover, the area is considerably lower when RHCM is applied. 5) The number of NR iterations are lower when RHCM is used than that when Lagrange and HCM are applied. 6) The number of hyperspheres required for the trajectory tracing is lower when RHCM is applied than that when HCM is applied.

Fig. 8 plots the delay variability ($\sigma_D/\mu_D$) of the three logic paths as a function of the consumed area. Each dot represents a sizing condition of the logic gates of the paths. The delay variability and the corresponding path area (each dot) were obtained from 1500 random combinations of the gate sizes using the block B-2 of the framework (See Fig. 3). It can be noted that a given delay variability of the paths can be obtained at different area cost. The sizing conditions for 40% of target optimization obtained with the Lagrange multipliers (LG) and Homotopy approaches (HCM and RHCM) are indicated on the plots. NOM represents the delay variability of the path with nominal dimensions. The solid curve gives the optimum designs, i.e., path designs with the best trade-off between delay variability and area. It can be observed that optimization results with RHCM produce results very close the optimum curve. However, more optimal designs could be obtained using a best gate selection metric and by reducing the step size in the algorithms proposed.

Fig. 8. Delay variability of the paths versus the area cost, implemented with Lagrange (LG), homotopy continuation method (HCM) and reboot HCM (RHCM) for 40% of target reduction of the path delay. NOM represents the delay variability of the path with nominal dimensions.

The proposed design procedure (HCM and RHCM) presented in this work fulfills the goal of designing a logic path under process variations for a targeted optimization, and these results agree with the obtained with the Lagrange Multipliers. The obtained delay performance optimizations of the logic paths with RHCM present more accurate results than that with HCM. Moreover, RHCM
generates an optimum gate sizing on the logic paths according the loading capacitances. This is because in the sizing procedure the selected gate is smoothly sizing until the selection metric chooses another gate (See Fig. 4); i.e., until the function to be evaluated is rebooted. Therefore, according to the obtained results, over-sizing and over-optimization can be canceled with this proposal. Furthermore, the number of hyperspheres and NR iterations required to reach the solution is considerably low (See Table I) RHCM is applied.

5 Conclusions

A novel gate-sizing optimization algorithm based on the Homotopy continuation method was proposed. Two optimization strategies were implemented in this work, the first based on the homotopy continuation method (HCM) and the second based on a reboot homotopy continuation method (RHCM). These methodologies allow minimizing the impact of process variations on the circuit yield while convergence problems are canceled. Several logic paths were implemented to validate the algorithms. The optimization results obtained with the proposed strategies were compared with a Lagrange-Multipliers-based framework. Results obtained from HCM method are equivalent to the obtained with Lagrange Multipliers. Results obtained from the RHCM method are more accurate than the obtained with HCM and Lagrange Multipliers. The area used to implement the logic paths is lower when RHCM is used. Moreover, the number of Newton-Rhapson iterations required to find the solutions are lower when RHCM is used; consequently, time computing is also lower.