Evaluation of Nanoimprinting Multilayer Lift-off Process using Spin-on-glass for Nanogap Electrode Array

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Nanogap electrodes are expected to aid in the study of the electrical properties of single molecules and nanoparticles, and have also been applied to non-volatile memory. However, an electrode that exhibits a large area and good reproducibility is yet to be found. We investigate the nanogap fabrication method combining UV nanoimprint lithography and electromigration. A three-layer lift-off process, using spin-on-glass as an intermediate layer with high etching selectivity, is evaluated. Nanowire array patterns are fabricated in a 9-mm square in the process, which demonstrate the nanogap characteristics of resistance switching effects.

Keywords: UV nanoimprint, Spin-on-glass, Lift-off, Electro-migration, Nanogap electrode array

1. Introduction

Nanogap electrodes consist of two metal electrodes separated from each other by nanometers. These electrodes can be used to investigate the electrical properties of nanoscale materials such as molecules and nanoparticles [1-3]. In addition, nanogap electrodes have been found to exhibit various characteristic phenomena such as surface plasmon enhancement, magnetic resistance, and field emission [4-6]. Most of the above investigations involved nanoscale structures fabricated by electron-beam lithography (EBL). However, because EBL is expensive and time-consuming, a procedure that does not require the use of EBL is preferred for industrialization [7].

Ultraviolet nanoimprint lithography (UV-NIL) is a recently developed technology that allows low-cost nanopatterning in a UV curable resin [8-10]. In addition, once a master mold (stamp) is fabricated, it is possible to efficiently fabricate nanopatterns over large areas.

We have developed a process involving UV-NIL and electromigration for the efficient fabrication of nanogap electrodes [11]. We have used these processes to fabricate a 300-nm-wide nanowire and its nanogap that demonstrated the switching effect of a metal nanogap. However, the nanogap electrode patterns could only be fabricated in the small area of a chip.

In this study, we evaluated a two-layer lift-off UV-NIL process over a wider area. As an alternative method, we attempted three-layer lift-off UV-NIL using spin-on-glass (SOG). SOG exhibits high etching selectivity for the intermediate layer owing to the high resistance to oxygen dry etching, which is more than two orders of magnitude higher than an ordinary resist [12].

2. Experimental

The two quartz molds used for UV-NIL in the two-layer and three-layer lift-off processes were fabricated as follows. A 5-nm-thick Cr film was
deposited on 10 × 10 mm² quartz substrates with a thickness of 3 mm and a flatness error of \( \lambda/20 \). Electrode array patterns of nominal 300- and 400-nm-wide nanowires were delineated using an EBL system (Elionix, ELS-7700H), as shown in Fig. 1. The patterns were then etched into the quartz substrates by a reactive ion etching (RIE) system (Samco, RIE-10NR) using CHF₃ gas at 30 sccm. The depths of the molds for the two-layer and three-layer lift-off processes were 168 and 152 nm, respectively. The molds were treated with an anti-adhesion reagent (Gelest, Aquaphobe CF) for 15 min after removal of the EBL resist and Cr.

Figure 1. Schematic image of an electrode array.

Figure 2 shows the two-layer lift-off UV-NIL process. A lift-off resist (Micro Chem, LOR1A) and UV-curable resin (Toyo Gosei PAK-01-200) were spin-coated on a 4 in. Si wafer with a silicon oxide film. The thicknesses of the lift-off resist and the UV curing resin, which were measured using a reflective film thickness monitor (Otsuka Electronics FE-3000), were 100 and 370 nm, respectively. Four shots of UV-NIL were carried out on the wafer using a UV-NIL stepper equipped with a 1,1,1,3,3-pentafluoropropane (PFP) gas introduction system to attain bubble-free imprinting [13]. The conditions of UV-NIL were an imprint pressure of 0.1 MPa, contact time of 10 s, an exposure dose of 100 mJ/cm², and PFP flow rate of 1000 sccm. After UV-NIL, the sample was cut into a 9-mm square. The residual layer of PAK-01 was removed under the conditions of CHF₃ and O₂ gas flow rates of 10 sccm, a chamber pressure of 2.6 Pa, and an RF power of 150 W. The etching time was 41 s. Subsequently, the sample was dipped in tetramethylammonium hydroxide (TMAH) aqueous solution (1.2%) for 10 s. A 7-nm-thick Ti film and 15-nm-thick Pt film were deposited on the sample using a sputtering system (ULVAC, j sputter). Finally, the lift-off resist was etched in N-methyl-2-pyrrolidinone solution using an ultrasonic cleaning system for 30 min. The samples were inspected using an optical microscope and a field emission scanning electron microscope (FE-SEM; Hitachi S-4800).

Figure 2. Two-layer lift-off/UV-NIL including a wet process: (a) coating of LOR1A and PAK-01, (b) UV nanoimprinting, (c) residual layer removal etching, (d) TMAH wet etching, (e) deposition of Pt/Ti, and (f) removal of layers including LOR1A.

Figure 3 shows the three-layer lift-off UV-NIL process using SOG. A lift-off resist (Micro Chem, LOR1A) was spin coated on a 4 in. Si wafer with a silicon oxide film. An SOG (Honeywell, accuglass T-11) was spin coated on the sample at a rotation speed of 7000 rpm for 2 min, and baked at 200 °C for 10 min. Thus, SOG could easily be formed into a glass-like film by changing from a liquid to a solid by heat treatment after spin coating film formation. A UV-curable resin (Toyo Gosei, PAK-01-200) was spin-coated on the SOG layer treated with O₂ plasma. The thicknesses of the lift-off resist, the PAK-01, and SOG were 100, 182, and 100 nm, respectively. UV-NIL and the residual layer
removal etching were carried out under the same conditions as those shown in Fig. 2. The etching time for residual layer removal was 17 s. Subsequently, the SOG was dry etched for 200 s using the RIE system with a CHF$_3$ gas flow rate of 80 sccm, a chamber pressure of 2 Pa, and an RF power of 250 W. The lift-off resist was dry etched for 40 s using the RIE system with an O$_2$ gas flow rate of 50 sccm, a chamber pressure of 5 Pa, and an RF power of 150 W. A 5-nm-thick Ti film and 30-nm-thick Au were deposited on the sample using a DC sputtering system. Finally, the lift-off resist was etched in N-methyl-2-pyrrolidinone solution using an ultrasonic cleaning system for 15 min. The samples were inspected using the optical microscope and the FE-SEM.

![Three-layer lift-off/UV-NIL process](image)

The nanogap-breakdown process was conducted using samples of the nominal 300- and 400-nm-wide nanowires, which were fabricated by the three-layer lift-off process shown in Fig. 3. The voltage applied to the nanowires was controlled using the previously reported procedures [14,15]. The voltage was increased in 10 mV steps and the current was monitored with a source meter (Keithley, 2600B, USA) under a vacuum chamber (<1×10$^{-3}$ Pa). When the resistance of the nanowire changed drastically, the applied voltage was immediately returned to 0 V and then increased. When the current–voltage (I–V) characteristics deviated from a linear relationship, the procedure was terminated. This method applied a feedback voltage to the nanowire by monitoring its resistance change. As the nanowire was destroyed, the feedback voltage applied was lowered. The end point voltage at which the nanowire broke down was determined by the resistance value. The number of cycles of applied feedback voltages for the 300- and 400-nm-wide nanowires were 310th and 600th, respectively.

### 3. Results and discussion

#### 3.1. Two-layer lift-off/UV-NIL including wet process

Figure 4 shows the optical microscope images of four samples of nanowire electrode arrays in 9 × 9 mm$^2$ after the lift-off process shown in Fig. 2. It was observed that no patterns were observed over a large area in the chip, and a SiO$_2$ layer appeared. We also observed each process separately using the optical microscope. Although electrode patterns were formed without any defects after UV-NIL, as shown in Fig. 2 (c), the defects appeared after TMAH wet etching for the LOR1A layer, as shown in Fig. 2 (d). Figure 5(a) shows the optical microscope image of the four electrode patterns in the defect area at the lower left of the chip shown in Fig. 4(a). We propose that the main cause of the pattern defects was the disappearance of the PAK-01 pattern during unoptimized residual layer removal etching owing to the non-uniform residual layer thickness of PAK-01 in UV-NIL. Alternatively, the PAK-01 pattern may be peeled away from the substrate during TMAH wet etching. In particularly, it was difficult to control the etching amount during TMAH wet etching because of the short etching time of 10 s. Figures 5(b) and 5(c) show the optical microscope images of the nominal 300- and 400-nm-wide nanowires. Although there were no defects observed in the bright field image, a lot of defects and particles were observed in the
nanowire patterns from the magnified dark-field images. Figure 6 shows the SEM images of the nominal 300- and 400-nm-wide nanowires. It was confirmed that a Pt nanowire with a width of 300 nm and a length of 4 µm was fabricated, as shown in Fig. 6(a), whereas burrs were formed in the nanowire pattern of the 400-nm-wide nanowire, as shown in Fig. 6(b).

![Fig. 4. Optical microscope images of four samples of nanowire electrode arrays in a 9 × 9 mm² area after the lift-off process shown in Fig. 2.](image)

![Fig. 5. Optical microscope images of fabricated nanowire electrode devices of the sample shown in Fig. 4(a): (a) four electrode patterns at the defect area in the lower left of the chip, (b) nominal 300-nm-wide nanowire, and (c) 400-nm-wide nanowire.](image)

![Fig. 6. SEM images of the (a) nominal 300-nm-wide nanowire and (b) 400-nm-wide nanowire.](image)

3.2. Three-layer lift-off/UV-NIL using SOG

Figure 7 shows the optical microscope images of four samples of the nanowire electrode arrays in a 9 × 9 mm² area after the lift-off process shown in Fig. 3. In all chips, the electrode patterns were mostly fabricated in the 9-mm square except for the upper left area of the chip. The few defects were caused by mold defects of UV-NIL because the pattern defect area was same in all chips. Figures 8(a) and 8(b) show the optical microscope images of the nominal 300- and 400-nm-wide nanowires. The nanowire structure was formed in the center of the electrodes without any defects and particles from the magnified dark-field images. Figure 9 shows the SEM images of the nominal 300- and 400-nm-wide nanowires. Although nanowires were formed without burrs in both patterns, the pattern widths of the nominal 300- and 400-nm-wide nanowires were 413 and 502 nm, respectively. Both nanowires became approximately 100 nm wider than the design sizes. Figure 10 shows the cross-sectional SEM images of the nominal 300-nm-wide nanowire pattern before the lift-off process. The pattern opening widths of the PAK-01 and SOG layers were approximately 300 nm, whereas the width of LOR1A was 410 nm, which was wider than the upper layers. Thus, it was confirmed that Au film was deposited on the opening pattern area of LOR1A by a metal sputtering process owing to diffusion of Au deposition into the shadow of the opening of the PAK-01/SOG patterns.
Fig. 7. Optical microscope images of four samples of nanowire electrode arrays in a 9 × 9 mm² area after the lift-off process shown in Fig. 3.

Fig. 8. Optical microscope images of fabricated nanowire electrode devices of the sample shown in Fig. 7(a): (a) nominal 300-nm-wide nanowire and (b) 400-nm-wide nanowire.

Furthermore, we evaluated the electrical characteristics of the nanogap fabricated from the nominal 300- and 400-nm-wide nanowires. Figures 11(a) and 11(b) show the characteristics of the repeated switching operations in the nominal 300- and 400-nm-wide nanowires. The resistances of the Au nanogaps were measured at 0.6 V when sweep voltages from the high resistance state (HRS) to the low resistance state (LRS) and from the LRS to the HRS were alternately applied under vacuum (<1 × 10⁻³ Pa) for 100 cycles. In these cycles, the HRS-to-LRS transition was achieved using a sweep voltage of 5 V, while the LRS-to-HRS transition was attained using a sweep voltage of 7 V. The reading voltage was set at a low voltage at which the gap width did not change. The HRS and LRS were obtained near 10⁹ Ω and 10⁸ Ω to 10⁶ Ω, respectively. A few points showed a poor resistance ratio; however, the majority of points indicated a large resistance ratio of over 10². Thus, the fabricated nanogap electrodes exhibited a reversible memory effect with a large resistance ratio. These results indicated that Au nanogap structures with a size of less than 2 nm were successfully fabricated in the process.

Fig. 9. SEM image of (a) nominal 300-nm-wide nanowire and (b) 400-nm-wide nanowire.

Fig. 10. Cross sectional SEM images of nominal 300-nm-wide nanowire pattern before the lift-off process.
Fig. 11. Electrical characteristics of Au nanogap electrodes fabricated by three-layer lift-off/UV-NIL and electromigration: (a) former nominal 300-nm-wide nanowire and (b) former nominal 400-nm-wide nanowire.

4. Conclusion

In this study, we evaluated multilayer lift-off UV-NIL using spin-on-glass (SOG) having high etching selectivity for the intermediate layer. By using SOG, the formation of metal nanowires on the whole area of the imprint surface was demonstrated and the formation of a metal nanogap was structured by the electromigration method. The switching effect of the gap was demonstrated by measuring the electrical properties of the structure. The developed process is promising as a low cost and large-scale fabrication approach to produce metal nanogap devices.

Acknowledgements

This work was supported by JSPS KAKENHI Grant Number of JP17K14575, and JP17K14100. This work was partly supported by JST-CREST, and MEXT-Supported Program for the Strategic Research Foundation at Private Universities.

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