BrainTTA: A 35 fJ/op Compiler Programmable Mixed-Precision Transport-Triggered NN SoC

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Abstract—Recently, accelerators for extremely quantized deep neural network (DNN) inference with operand widths as low as 1-bit have gained popularity due to their ability to largely cut down energy cost per inference. In this paper, a flexible SoC with mixed-precision support is presented. Contrary to the current trend of fixed-datapath accelerators, this architecture makes use of a flexible datapath based on a Transport-Triggered Architecture (TTA). The architecture is fully programmable using C. The accelerator has a peak energy efficiency of 35/67/405 fJ/op (binary, ternary, and 8-bit precision) and a throughput of 614/307/77 GOPS, which is unprecedented for a programmable architecture.

I. INTRODUCTION
Edge computing is a rising computing paradigm with the ability to overcome privacy, latency, and energy issues that are currently being faced in the deployment of neural networks (NNs) on embedded devices. While modern neural networks can solve complex tasks in the fields such as Computer Vision (CV) and Natural Language Processing (NLP), the sheer size of these networks prevents deploying such a network directly on embedded devices, which typically have limited storage capacity. Alongside the required storage for the parameters of these networks, the compute power also interferes with the deployment of such networks due to the energy constraints typically imposed on embedded hardware. To overcome these challenges, several approaches to optimize the models for low-power hardware have been explored. These include Hardware-aware Neural Architecture Search (NAS) [1], model compression in the form of pruning [2] and quantization [3] and efficient data reuse [4].

In parallel, research has been performed on creating highly specialized accelerators for neural network inference, exploiting the aforementioned model compression techniques. While these architectures perform great in terms of energy efficiency, the datapath structure is often not flexible and programmability is limited to some assembly dialect if programmable at all.

In short, current efforts towards low-power accelerators lack the flexibility to efficiently support different layers with varying sizes and varying parameter precision. Furthermore, the usability of these accelerators is hindered due to the absence of a compiler. In this paper, we present BrainTTA, the first flexible-datapath mixed-precision high-level programmable NN accelerator with compiler support. We showcase the flexibility of this architecture and the energy trade-off when running layers with different bit-widths. The contributions of this paper are threefold:

- An energy-efficient TTA-based SoC for neural network inference supporting multiple precisions (binary, ternary and 8-bit) with a high energy efficiency of 35/67/405 fJ/op respectively (section III & IV).
- A thorough analysis of the system energy consumption for various operand bit-widths; it is found that the total system energy cost per operation grows superlinear with the bit-width of the operands (section V).
- A detailed analysis on the trade-off between energy efficiency and flexibility. BrainTTA is more flexible than state-of-the-art architectures while limiting the overhead (section VI).

The remainder of this paper is organized as follows. In section II, the background knowledge is discussed. Thereafter, in section III, an overview of the full system architecture is discussed after which in section IV the mapping of the network onto the proposed architecture is described. The results are presented in section V and a comparison with respect to state-of-the-art architectures is presented in section VI. The paper is concluded in section VII.

II. BACKGROUND INFORMATION
To relieve the burden on the memory and reduce the arithmetic complexity, quantization can be applied. Quantization can be applied down to 8-bit without significant loss of accuracy [5]. But even with 8-bit quantization, the storage requirements of modern networks are not in line with the storage size typically found in embedded hardware. Therefore, a push towards even lower bit-width quantization was made.

A. Binary and Ternary Quantization
Binary quantization restricts the weights and activations to a single bit; therefore the weights and activations are \( w, a \in \{-1, +1\} \) whereas ternary trits can additionally represent zero. This low operand precision introduces several advantages: the memory footprint is drastically reduced, the computations can be simplified, and the required bandwidth decreases sharply [6][7]. When both weights and activations are binarized or ternarized, the computations can be simplified by replacing the MAC (Multiply-Accumulate) operation with XNOR and popcount for binary and Gated-XNOR
III. ARCHITECTURAL OVERVIEW

The proposed full system architecture is displayed in Fig. 2 and the TTA core in Fig. 3. In this paper, the TTA-based Co-design Environment (TCE) is used to create the TTA instance. This is an open-source toolchain that provides full compiler support. The compiler supports C, C++ and OpenCL. The TCE framework allows creation of any Functional Unit (FU) with arbitrary functionality and number of input and output ports. The FUs are controlled with custom instructions that can be added into the TCE compiler; the instructions can be inferred by the compiler or directly called using intrinsics. The main system components are:

- **RISC-V host processor**, to start/stop the execution on the TTA core, initialize the memories and send and receive information via the external interfaces.
- **TTA core**, used to perform the mixed-precision inference, more details will follow in the next paragraph.
- **SRAM**, with separate memories for the RISC and TTA core, the TTA core. Memories are banked to allow efficient access of smaller bit-widths.
- **Debugger (DBG)**, can halt the execution on the TTA core and signal completion of a task to the RISC-V host.
- **AXI interconnect**, used for on-chip communication between the RISC and TTA-core and interfaces with the peripherals (APB) for off-chip communication.

At the heart of the SoC is the TTA core. This core is used for the neural network inference and is based on TTA explained in Section II-B. The instantiation of the TTA core used in this paper is shown in Fig. 3. The core contains different FUs. The FUs are interconnected via buses, with scalar buses (bus 0-5) and vector buses (bus 6-11). The data transports (moves) on these buses are explicitly programmed. The core consists of the following units:

- **Control Unit (CU)**; this unit contains the logic to fetch and decode instructions and steers the other units to execute the correct operations. Furthermore, the CU contains a hardware loopbuffer. Since the network layers are essentially described by multiple nested loops (listing I), having a hardware loopbuffer can greatly cut-down instruction fetch costs.

- **Vector Multiply-Accumulate (vMAC/vBMAC/vTMAC)** unit is the workhorse of the TTA core. MAC operations are performed for binary, ternary, and 8-bit operands. The unit multiplies two 1024-bit vectors with 32 entries of 32-bits per each, thus the vMAC contains 32 reduction trees, where each tree has 4 8-bit, 16 ternary, or 32 binary inputs. Input data reuse is exploited by broadcasting the input feature map to multiple units with different weights. The fixed vector width implies that for each bit-width, different vectorization factors are applied; this is further explained in Section IV-B.

- **Vector Add (vADD)** is used to add two (either 512- or 1024-bit) vectors, this can be used to support residual layers.

- **Vector Operations (vOPS)**, auxiliary (vector) operations that are required in the network, alongside the computations. This FU can perform quantization as well as apply activation functions e.g. ReLU and pooling functions such as MaxPool. This FU also supports scalar element insertion and extraction on vectors.

- **(Vector) Register Files (vRFs/RFs)** to store intermediate values or buffer weights to increase data reuse.

- **Load-Store Units (LSUs)** are the interface between to the SRAM. There are two LSUs, mainly used to load weights (from PMEM) and one to load and store feature maps (DMEM). Since the memories are banked, multiples of 32-bit data can be loaded at low cost by selectively turning on memory banks.
Scalar Units are primarily used for address calculations needed as inputs to the LSUs.

The above mixture of units and supported operations is carefully selected after inspecting and scheduling frequently used DNN workloads.

**IV. Application Mapping**

The different layers in a neural network can generally be described in terms of nested for-loops, see listing 1 for an example.

```plaintext
for h in [0, H - R + 1):
    for w in [0, W - R + 1]:
        for tm in [0, M/32]:
            acc = bias[tm]
            for tc in [0, C/4]:
                for s in [0, S]:
                    acc += in_buffer[h + r][w + s][tc] * weights[n][r][s][tm]
            out_buffer[h][w][tm] = acc
```

Listing 1: An example of an 8-bit convolutional layer with output-stationary schedule, where \( v_C \) and \( v_M \) are the vectorization factors for the input- and output-channels.

Since applications for the TTA can be programmed in C, the schedule can easily be altered for each layer separately. Changing the schedule simply boils down to applying loop transformations (e.g. unroll, interchange, tile). This scheduling freedom, in combination with the exposed-datapath operating principle, allows the creation of an efficient schedule on a per-layer basis with minimized data movements.

**A. Layer Support**

Different neural networks constitute different layer types. Among the layer types that are supported in BrainTTA are:

1) Convolutional layer (8b in, 32b out)
2) Binary convolutional layer (1b in, 16b out)
3) Ternary convolutional layer (2b in, 16b out)
4) Depth-wise convolutional layer (8b in, 32b out)
5) Fully-connected layer (8b in, 32b out)
6) Residual addition (16/32b in, 16/32b out)
7) Requantization (to 8b, 2b or 1b)

All above layers are supported by BrainTTA, an energy breakdown of the first three is given in Section V. The supported layers are described by:

**Convolutional layers** are supported with three different bit-widths, namely 8-bit, ternary and binary. Depending on the bit-width of the convolutional layer, the 1024-bit weight and input vector are split in different ways (more information in section IV-B). Since different output feature maps use the same input feature maps, input broadcasting is possible for data reuse.

**Depth-wise convolutional layers** are supported by changing the scalar-vector product used in convolutional layers to vector-vector products which is required since each weight kernel is bound to a single input channel; in other words, input broadcasting is not possible.

**Fully-connected layers** execution is similar to that of convolutional layers, however, the kernel size is now 1x1.

**Residual addition** is adding two higher bit-width values, but to support this, the scaling factor of the values added together needs to match. The latter is called requantization.

To keep down the overhead that comes with the flexibility and programmability of BrainTTA, parallelism is introduced in several scheduling dimensions (i.e. dimensions that are shown in listing 1; in the next paragraph, the choice of vectorization dimensions to achieve this parallelism will be elaborated.

**B. Vectorization**

The vectorization is visualized in Fig. 4. The choice of vectorization dimensions is based on three observations. First of all, modern networks typically have more feature maps (higher \( C, M \)) but the size of each individual feature map can be smaller \((W, H)\). This means that to populate a large vector, one should not only vectorize over \( W \) and \( H \). Secondly, the MAC, binary and ternary popcount operations produce an intermediate output value with a much higher bit-width than the quantized value; requantization should happen as soon as possible to reduce movement of large intermediate values. Therefore, the final value of a single pixel in the output feature...
map should be calculated as early as possible, which makes an output-stationary schedule favorable. Lastly, the popcount outputs the sum of its inputs. Therefore, the inputs supplied to the popcount module should contribute to the same output pixel. This means that the inputs supplied to a single popcount module (which corresponds to a single vector element), should either have a different \( W \& H \) indices in the same receptive field or from a different input channel \( C \). In BrainTTA, the datapath width is 1024-bits and the output vectorization factor is \( v_M = 32 \); therefore, to fill the 1024-bit datapath, \( v_C = 32 \) for binary, \( v_C = 16 \) for ternary and \( v_C = 4 \) for 8-bit inputs.

V. RESULTS

The design that is shown in Fig. 2a is synthesized using GlobalFoundries 22nm FDX technology using an operating voltage of 0.5V while targeting the typical corner. After synthesis, the layout is created which can be seen in Fig. 2b. A. Experimental setup

The flow that is used to go from RTL to layout consists of Cadence Genus 21.10 for the logic synthesis and Cadence Innovus 21.11 for the back-end implementation. These tools are also used to obtain energy numbers. The energy numbers are obtained by annotating the switching activity found during the post-layout simulation in order to gain the most accurate energy figures possible.

B. Post-layout simulation results

The area of the SoC is 3.0mm\(^2\) excluding IO pads as can be seen in Fig. 2b. The largest part of the floorplan is dedicated to the data (DMEM) and parameter (PMEM) memory of the TTA core, holding the input/output feature map and weights respectively. Both the DMEM and PMEM are made by combining 32 banks of 16kB each, resulting in a combined data storage capacity of 1MB.

Fig. 5 displays the energy that is required to perform three convolution layers, with binary, ternary, and 8-bit operands. A MAC is counted as two operations. It can be seen that the energy per operation difference between the binary and ternary convolution is nearly a factor of 2. Furthermore, the breakdowns between the two different scenarios are very similar with the exception of the instruction memory. The reason for this similarity is that the compute unit (vMAC) circuitry and usage of the binary and ternary convolution are very alike, and their utilization of the other components is identical but the amount of computations per second is halved since the ternary digits (trits) take up twice the space of single binary digits, hence the doubled energy per operation. In other words, the overhead per computation is doubled when doubling the number of bits of the operands.

Furthermore, the interconnect (IC) of the TTA core takes second place in energy usage in the logic after the vMAC. This is one of the architectural characteristic components where a price is paid for flexibility. In contrast, the fixed-datapath architectures discussed in the related work do not provide the freedom to freely move data around between different units in a programmable way. The routing flexibility in BrainTTA in combination with the freedom to implement any FU (and retain compiler support) makes it possible to run more complex networks like ResNet and even non-DNN workloads independently of the general purpose processor.

VI. COMPARISON WITH STATE-OF-THE-ART

Various papers have been published about architectures containing accelerators to bring down the energy per inference as much as possible. Most of these accelerators can be grouped
into: fully-digital implementations, mixed-signal approaches and Compute-in-Memory (CIM) approaches. Although CIM architectures [16][17] can currently go beyond 500 TOPS/W, they suffer from the design time required for the complex analog compute blocks. Furthermore, these analog compute blocks show chip-to-chip variation due to CMOS process variation which makes them error-prone and difficult to benchmark the exact performance. Therefore, the related work focuses on fully digital implementations, specifically designed for inference on heavily quantized networks.

A. Related work

XNOR-Neural Engine (XNE) [18] and ChewBaccaNN [19] are binary accelerators that support the previously described reduced arithmetic complexity introduced by binary quantization. In [18], a full SoC is presented able to run neural networks autonomously with the help of a configurable Micro-Controller Unit (MCU). Due to the lack of input data reuse, the SRAM reads dominate the energy consumption. This is circumvented by turning the SRAMs completely off and storing all data in RFs, therefore making it unable to run any realistic workloads. In [19], SRAM is avoided at all by using SCM only. Although the authors claim flexibility, the kernel size is hard-wired into the design (with a dramatic drop in performance when using a different kernel size).

In [20] a ternary accelerator called CUTIE is presented. By spatially unrolling all the convolutional loops (seen in Listing 1), iterating can be avoided and great data reuse is guaranteed if the convolutional loop iterators match the hardware design point. Spatially unrolling the loop dimensions directly constrains the network layer sizes that can be run efficiently on the hardware, therefore sacrificing flexibility.

In [21], the idea of having scheduling flexibility in BNN inference is explored. The schedule flexibility is motivated by the change in layer parameters from the first layers into the deeper layers ($c > w, h$). Although an increase in throughput is reported by adding scheduling flexibility, power numbers for ASIC implementation are omitted, therefore this paper is not taken into account in the actual comparison.

In [22], a binary accelerator is implemented based on the compute-near-memory principle. All kernel sizes are hard-wired, therefore it offers little to no flexibility.

B. Comparison

The BrainTTA is compared to state-of-the-art accelerators in Table I. It is partitioned into three different sets: the general properties of each architecture, the neural network layer requirements for full utilization of the chip, and the support of other layers and programmability. BrainTTA beats XNE in energy efficiency, while XNE is the only accelerator that has comparable flexibility to BrainTTA. This flexibility does incur overhead; to lower the overhead, the hardware loop-buffer was used to reduce instruction fetches and data reuse was implemented using a combination of data broadcasting and parameter buffering in the vector register files. CUTIE, ChewBaccaNN and [22] all have a higher efficiency per operation, however, these architectures are not programmable and flexibility of these architectures is severely lacking due to the hard-wired datapaths. Furthermore, if a look is taken at the dimensions that are hard-wired into the design of the SotA competitors, attaining the peak throughput and peak efficiency becomes very challenging since the neural network layers would need to adhere to very specific layer size requirements. Illustrative to this problem is ChewBaccaNN, which reports a maximum throughput of 240 GOPS while only achieving 23 GOPS in XNORNET-++ [8]. Furthermore, none of these architectures supports 8-bit operands or is programmable in a high-level language.

VII. CONCLUSION

A novel TTA-based SoC for neural network inference that seamlessly combines flexibility with efficiency is presented in this paper. The SoC is able to perform operations at
with a hardware-aware mapping tool such as ZigZag [23].

**Future work:** The authors still see options for future improvements such as including ternary compression, adding more vMAC units to sequentially calculate outputs in a systolic way, and intertwining the compiler with a hardware-aware mapping tool such as ZigZag [23].

### TABLE I: Comparison of performance, efficiency and flexibility of the architectures discussed.

| Implementation characteristics                        | ChewBaccaNN [19] | CUTIE [20] | XNE [18] | 10nm FinFet [23] | BrainTTA |
|--------------------------------------------------------|------------------|------------|----------|------------------|----------|
| Technology node [nm]                                   | 22               | 22         | 22       | 10               | 22       |
| Supply voltage [V]                                     | 0.4              | 0.65       | 0.6      | 0.4              | 0.39     |
| Inference precision\(2\)                              | \(b\\)           | \(b, t\)   | \(b\\)   | \(b\) \(t, 1\)  | \(b\) \(t, 1\) |
| Memory technology                                      | SCM              | SRAM       | SCM      | SRAM             | SCM      |
| **Key Performance Indicators**                         |                  |            |          |                  |          |
| Peak throughput [GOPS]                                 | 240              | 16000      | 67       | 5                | 3400     |
| Energy/op [fJ] binary                                  | 4.48/15.38\(3\)  | -          | 115      | 21.6             | 1.62     |
| Energy/op [fJ] ternary                                 | -                | 2.19       | 1.70     | -                | 67       |
| Energy/op [fJ] 8-bit                                   | -                | -          | -        | 405              |          |
| Core area [mm\(2\)]                                    | 0.7              | 7.5        | 2.32     | 0.39             | 2.98     |
| Area efficiency [GOPS/mm\(2\)]                        | 343              | 2133       | 28.88    | 8717             | 206      |
| Memory capacity [kB] (excl. instruction memory)        | 153              | -          | 520      | 16               | 161      |
| **Flexibility**                                        |                  |            |          |                  |          |
| Full utilization for                                   |                  |            |          |                  |          |
| Number of IFMs (C) multiple of                         | 16               | 128        | 128      | 1024             | 32/16/4\(4\) |
| Number of OFMs (M) multiple of                         | Any              | 128        | 128      | 128              | 32       |
| Kernel height (R) is                                   | 7                | 3          | Any      | 2                | Any      |
| Kernel width (S) is                                    | 7                | 3          | Any      | 2                | Any      |
| Partial result support (for scheduling freedom)        | Yes              | No         | No       | No               | Yes      |
| Residual layer support                                 | Yes              | No\(5\)    | No       | No               | Yes      |
| Programmability                                        | None             | None       | None     | None             | C/C+++/OpenCL |

1 \(b = \text{binary}, t = \text{ternary}, i8 = \text{integer8}.\)
2 Only estimates were provided, under the assumption that all ternary-specific hardware is removed.
3 For 7x7 and 3x3 convolution respectively.
4 For \text{binary, ternary} and \text{integer8} respectively.
5 Partial result support is not needed since the output pixel computation is fully unrolled in hardware.

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35/67/405 fJ/op for binary, ternary and 8-bit operands respectively. Still, it is highly flexible and can easily adapt to different types of networks such that it can advance together with the algorithmic inventions in the area of heavily quantized neural networks. The support for mixed-precision allows the SoC to mitigate accuracy loss in layers that are most adversely affected by low-bit-width quantization (typically the first and last layer of the network). The mixed-precision and compiler support, in combination with the exposed-datapath to minimize data movement make this architecture very versatile while approaching the energy efficiency of much less flexible architectures of competitors. **Future work:** The authors still see options for future improvements such as including ternary compression, adding more vMAC units to sequentially calculate outputs in a systolic way, and intertwining the compiler with a hardware-aware mapping tool such as ZigZag [23].
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