Semi-Asymmetric Parallel Graph Algorithms for NVRAMs *

Laxman Dhulipala
CMU
Charles McGuffey
CMU
Hongbo Kang
CMU
Yan Gu
MIT CSAIL
Guy E. Blelloch
CMU
Phillip B. Gibbons
CMU
Julian Shun
MIT CSAIL

Abstract

Emerging non-volatile main memory (NVRAM) technologies provide novel features for large-scale graph analytics, combining byte-addressability, low idle power, and improved memory-density. Systems are likely to have an order of magnitude more NVRAM than traditional memory (DRAM), allowing large graph problems to be solved efficiently at a modest cost on a single machine. However, a significant challenge in achieving high performance is in accounting for the fact that NVRAM writes can be significantly more expensive than NVRAM reads.

In this paper, we propose an approach to parallel graph analytics in which the graph is stored as a read-only data structure (in NVRAM), and the amount of mutable memory is kept proportional to the number of vertices. Similar to the popular semi-external and semi-streaming models for graph analytics, the approach assumes that the vertices of the graph fit in a fast read-write memory (DRAM), but the edges do not. In NVRAM systems, our approach eliminates writes to the NVRAM, among other benefits.

We present a model, the Parallel Semi-Asymmetric Model (PSAM), to analyze algorithms in the setting, and run experiments on a 48-core NVRAM system to validate the effectiveness of these algorithms. To this end, we study over a dozen graph problems. We develop parallel algorithms for each that are efficient, often work-optimal, in the model. Experimentally, we run all of the algorithms on the largest publicly-available graph and show that our PSAM algorithms outperform the fastest prior algorithms designed for DRAM or NVRAM. We also show that our algorithms running on NVRAM nearly match the fastest prior algorithms running solely in DRAM, by effectively hiding the costs of repeatedly accessing NVRAM versus DRAM.

1 Introduction

Over the past decade, there has been a steady increase in the main-memory sizes of commodity multicore machines, which has led to the development of fast shared-memory algorithms for processing massive graphs with hundreds of billions of edges \cite{65, 58, 67, 30} on a single machine. Single-machine analytics by-and-large outperform their distributed memory counterparts, running up to orders of magnitude faster using much fewer resources \cite{65, 52, 67, 30}. The trend in increasing memory sizes continues today in the form the new non-volatile memory technologies that are now emerging on the market (for example, Intel's Optane DC Persistent Memory is now available from many retailers \cite{38}). These devices provide an order of magnitude greater memory capacity per DIMM than traditional DRAM, and offer byte-addressability and low idle power, thereby providing a realistic and cost-efficient way to equip a commodity multicore machine with multiple terabytes of non-volatile RAM (NVRAM).

*This is a preliminary version of a paper currently under review. The authors can be contacted at \{ldhulipa, cmcguffey, hongbok\}@andrew.cmu.edu, ygu@mit.edu, \{guyb, gibbons\}@cs.cmu.edu, and jshun@mit.edu.
Due to these advantages, NVRAMs are likely to be a key component of many future memory hierarchies, likely in conjunction with a smaller amount of traditional DRAM. However, a challenge of these technologies is to overcome an asymmetry between reads and writes—write operations are more expensive than reads in terms of energy and throughput. This property requires rethinking algorithm design and implementations to minimize the number of writes to NVRAM [11, 7, 20, 74].

As an example of the technology and its tradeoffs, the experiments in this paper are done on a 48 core machine that has 8x as much NVRAM as DRAM (and we are aware of machines with 16x as much NVRAM as DRAM [34]), where combined read throughput for all cores from the NVRAM is about 3x slower than reads from the DRAM, and writes on the NVRAM are a further factor of about 4x slower [72, 39] (a factor of 12 total).

A property of most graphs used in practice is that they are sparse, but still tend to have many more edges than vertices, often from one to two orders of magnitude more. This is true for almost all social network graphs [45], but also for many graphs that are derived from various simulations [25]. Given that a large graph can have over 100 billion edges (requiring around a terabyte of storage), but only a few billion vertices, a popular and reasonable assumption is that vertices, but not edges, fit in DRAM [1, 53, 61, 82, 83, 70, 42, 51, 57, 32].

With these characteristics of NVRAM and real-world graphs in mind, in this paper we propose a semi-asymmetric approach to parallel graph analytics, in which (i) the full graph is stored in NVRAM and is accessed in read-only mode and (ii) the amount of DRAM is proportional to the number of vertices. Although completely avoiding writes to the NVRAM may seem overly restrictive, the approach has the following benefits: (i) algorithms avoid the high cost of NVRAM writes, (ii) the algorithms do not contribute to NVRAM wear-out or wear-leveling overheads, and (iii) algorithm design is independent of the actual cost of NVRAM writes, which has been shown to vary based on access pattern and number of cores [72, 39] and will likely change with innovations in NVRAM technology and controllers. Moreover, it enables an important NUMA optimization in which a copy of the graph is stored on each socket (Section 5), for fast read-only access without any cross-socket coordination. Finally, with no graph mutations, there is no need to re-compress the graph on-the-fly when processing compressed graphs [29, 30].

The key question, then, is the following: Is the (restrictive) semi-asymmetric approach effective for designing fast graph algorithms? In this paper, we provide both theoretical and experimental evidence of the approach’s effectiveness.

We consider over a dozen well-studied graph problems (see Table 1) and design fast and highly scalable semi-asymmetric algorithms for them. The key innovations are in ensuring that the updated state is associated with vertices and not edges, which is particularly tricky (i) for certain edge-based parallel graph traversals and (ii) for algorithms that “delete” edges as they go along in order to avoid revisiting them once they are no longer needed. We provide general techniques (Section 4) to solve these two problems. For the latter, used by four of our algorithms, we require relaxing the prescribed amount of DRAM to be on the order of one bit per edge. Details of our algorithms are given in Section 4.3.

From a theoretical perspective, we propose a model for analyzing algorithms in the semi-asymmetric setting (Section 2). The model, called the Parallel Semi-Asymmetric Model (PSAM), consists of a shared asymmetric large-memory with unbounded size that can hold the entire graph, and a shared symmetric small-memory with $O(n)$ words of memory, where $n$ is the number of vertices in the graph. In a relaxed version of the model, we allow small-memory size of $O(n + m/\log n)$ words, where $m$ is the number of edges in the graph. Although we do not use writes to the large-memory in our algorithms, the PSAM model permits writes to the large-memory, which are $\omega > 1$ times more costly than reads. We prove strong theoretical bounds in terms of PSAM work and depth for all of our parallel algorithms, as shown in Table 1. Most of our algorithms are work-efficient.
Table 1: Running times (in seconds) and speedup of our algorithms on the Hyperlink2012 graph using NVRAM. (1) corresponds to the single-threaded time, (48h) corresponds to the running time on 48 cores with hyper-threading, and (SU) is the parallel speedup. Note that the single-threaded times for triangle counting and PageRank are omitted since they did not finish in a reasonable amount of time. Also shown are the work and depth on the PSAM model. We use † to denote that our algorithm uses $O(n + m/log n)$ words of memory. We use * to denote that a bound holds in expectation and ‡ to denote that a bound holds with high probability or whp ($O(kf(n))$ cost with probability at least $1 - 1/n^k$). $d(G)$ is the diameter of the graph, $\Delta$ is the maximum degree, $L = \min(\sqrt{m}, \Delta) + \log^3 \Delta \log n / \log \log n$, and $P_B^l$ is the number of iterations of PageRank until convergence. In all cases we assume $m = \Omega(n)$.

(performing asymptotically the same work as the best sequential algorithm for the problem) and have polylogarithmic depth (parallel time). Our theoretical guarantees ensure that our algorithms perform reasonably well across graphs with different characteristics, machines with different core counts, and NVRAMs with different read-write asymmetries.

We experiment with implementations of our algorithms on a variety of large-scale real-world graphs (Section 5). Our implementations are able to scale to the largest publicly-available graph, the Hyperlink2012 graph with over 3.5 billion vertices and 128 billion edges (and 225 billion edges for algorithms running on the symmetrized graph). Table 1 shows the running times on the Hyperlink2012 graph using a 48-core machine with 3TB of NVRAM and 375GB of DRAM. Note that we cannot fit the entire Hyperlink2012 graph and run algorithms on this graph in the DRAM of this machine. Compared to the state-of-the-art DRAM-only algorithms from the Graph Based Benchmark Suite (GBBS) [30], our times are 1.03x faster on average and 1.87x faster on average than Galois algorithms [34] (state-of-the-art algorithms designed for NVRAM). Moreover, our algorithms running on NVRAM nearly match the running times of GBBS algorithms running entirely in DRAM, with all but three algorithms within 17%, by effectively hiding the costs of repeatedly accessing NVRAM versus DRAM.

The main contributions of this paper are:

1. We propose a semi-asymmetric approach to parallel graph analytics that avoids writing to the NVRAM and uses DRAM proportional to the number of vertices.

2. We design semi-asymmetric algorithms for 18 fundamental graph problems, and present general techniques for devising such algorithms. All of our codes will be released open source.
We introduce the Parallel Semi-Asymmetric Model, and show that our algorithms are (near) work-optimal in the model.

We evaluate our algorithms on a state-of-the-art NVRAM system, and show that our algorithms outperform prior work and nearly match DRAM-only performance.

2 Parallel Semi-Asymmetric Model

We now define the Parallel Semi-Asymmetric Model (PSAM). The PSAM consists of an asymmetric large-memory (NVRAM) with unbounded size, and a symmetric small-memory (DRAM) with $O(n)$ words of memory. In a relaxed version for graph filtering, we allow small-memory size of $O(n + m/\log n)$ words. This models the ratio of NVRAM vs. DRAM size matching the average degree of real-world graphs (see Table 2). In the PSAM, multiple threads share both the large-memory and small-memory. We use the classic work-depth measure for the cost of algorithms on the PSAM. We assume unit cost for a read from the large-memory or any instruction only accessing the small-memory. A write to the large-memory has a cost of $\omega > 1$, which is the cost of a write relative to a read on NVRAMs. The overall work $W$ of an algorithm is the cost for all memory accesses by all threads. The depth $D$ is the highest cost sequence of dependent instructions in the computation. A work-stealing scheduler can execute a computation in $W/p + O(D)$ time with high probability on $p$ processors [7]. A more formal definition of the model is given in Appendix A.

We note that although NVRAM reads are about 3x more costly than accesses to the small-memory [72], we charge both unit cost. When this cost gap needs to be studied (especially for showing lower bounds), we can use an approach similar to the asymmetric RAM (ARAM) model [12], and define the I/O cost $Q$ of an algorithm without charging for instructions or DRAM accesses. All algorithms in this paper have asymptotically as many instructions as NVRAM reads, and therefore have the same I/O cost $Q$ as work $W$ up to the constant factor representing the difference in DRAM vs. NVRAM read cost.

Although in our approach we do not perform writes to the large-memory, the PSAM is designed to be flexible to allow for analyzing alternate approaches that do perform writes to large-memory. Furthermore, permitting writes to the large-memory allows us to consider the cost of algorithms from GBBS [30] and observe that many of the algorithms that perform $\Omega(W)$ work when analyzed in the work-depth model have a work of $O(\omega W)$ for the corresponding semi-asymmetric algorithm.

The PSAM borrows ideas from the semi-external memory model [1, 61], the semi-streaming model [57, 32], the ARAM model [12], and the asymmetric nested-parallel (ANP) model [7]. Compared to the more general ARAM and ANP models, the PSAM is specially designed for graphs. The PSAM is different from the semi-streaming model in that NVRAMs allow random access rather than only sequential streaming, and from the semi-external memory model in that I/O does not take place in large blocks and accesses to the small-memory are charged.

3 Background and Notation

Graph Notation. We denote an unweighted graph by $G(V, E)$, where $V$ is the set of vertices and $E$ is the set of edges in the graph. A weighted graph is denoted by $G = (V, E, w)$, where $w$ is a function which maps an edge to a real value (its weight). The number of vertices in a graph is $n = |V|$ and the number of edges is $m = |E|$. Vertices are assumed to be indexed from 0 to $n - 1$. We use $N(v)$ to denote the neighbors of vertex $v$ and $deg(v)$ to denote its degree. We focus on undirected graphs in this paper, although many of our algorithms and techniques naturally generalize to directed graphs. We assume that $m = \Omega(n)$ when reporting bounds. We use $diam(G)$ to refer to the diameter of the graph, or the longest shortest path distance between any vertex $s$ and any vertex $v$ reachable from $s$. $\Delta$ is used to denote the maximum degree of the graph. We assume that there are no self-edges or duplicate edges in the graph. We refer to graphs stored in
the compressed sparse column and compressed sparse row formats as \textit{CSC} and \textit{CSR}, respectively. We also consider compressed graphs that store the differences between consecutive neighbors using variable-length codes for each sorted adjacency list, as done in Ligra+ [67].

\textbf{Ligra, Ligra+, and Julienne}. We make use of the Ligra, Ligra+, and Julienne frameworks for shared-memory graph processing and review components from these frameworks here [65, 67, 29]. Ligra provides the \textit{vertexSubset} data structure for representing subsets of vertices in a graph. We use the \textit{edgeMap} function provided by Ligra, which maps computations over edges. \textit{edgeMap} takes as input a graph \( G(V,E) \), a vertexSubset \( U \), and two boolean functions \( F \) and \( C \). \textit{edgeMap} applies \( F \) to \((u,v) \in E\) such that \( u \in U \) and \( C(v) = true \) (call this subset of edges \( E_a \)), and returns a vertexSubset \( U' \) where \( u \in U' \) if and only if \((u,v) \in E_a \) and \( F(u,v) = true \). \( F \) can side-effect data structures associated with the vertices. \textit{edgeMap} runs in \( O(\sum_{u \in U} \deg(u)) \) work and \( O(\log n) \) depth assuming \( F \) and \( C \) take \( O(1) \) work. \textit{edgeMap} either applies a \textit{sparse} or \textit{dense} method based on the number of edges incident to the current frontier. Both methods run in \( O(\sum_{u \in U} \deg(u)) \) work and \( O(\log n) \) depth. We note that our experiments use an optimized version of the dense method which examines in-edges sequentially and stops once \( C \) returns \textit{false}. This optimization lets us potentially examine significantly fewer edges than the \( O(\log n) \) depth version, but at the cost of \( O(\deg(v)) \) depth.

4 Semi-Asymmetric Techniques

In this section, we describe the main techniques that we use for designing efficient graph algorithms in the Parallel Semi-Asymmetric Model. Due to space constraints, we describe details about our techniques, and additional techniques in the appendix in Appendices C, D, and E.

4.1 Graph Filtering

Several of the parallel graph algorithms considered in this paper—biconnectivity, maximal matching, approximate set cover, and triangle counting—\textit{delete} edges incident to vertices during the course of the algorithm. In prior work in the shared-memory setting, the deleted edges are handled by physically removing them from the adjacency lists in the graph. We note that none of the existing techniques for algorithms for triangle counting, approximate set cover, maximal matching or biconnectivity achieve work-efficiency without either mutation of the input graph, or the use of \( O(m) \) words of fast memory to store a mutable representation of the graph [15, 29, 30].

The removal of such edges is important for two reasons. First, it reduces the amount of work done when edges incident to the vertex are examined again, and second, removing the edges is important to bound the theoretical efficiency of the resulting implementations [29, 30]. However, in the Parallel Semi-Asymmetric Model deleting edges is expensive because it requires writes to the large-memory.

In our Parallel Semi-Asymmetric Model algorithms, instead of directly modifying the underlying graph, we build an auxiliary data structure which we refer to as a \textit{graphFilter} that efficiently supports updating a graph with a sequence of deletions. The \textit{graphFilter} data structure requires \( O(m) \) \textit{bits} of memory to represent, and can be viewed as a bit-packed representation of the original graph that supports mutation. Importantly, this data structure fits into the relaxed version of the Parallel Semi-Asymmetric Model model.

\textbf{Graph Filtering Interface}. Before describing the implementation of our data structure, we first specify the high-level interface that it implements. The interface provides functions for creating a new \textit{graphFilter}, filtering edges from a graph based on a user-defined predicate, and a function similar to \textit{edgeMap} which filters edges incident to a subset of vertices based on a user-defined predicate. Since edges incident to a vertex can be deleted over the course of the algorithm by using a \textit{graphFilter}, we call edges that are currently part of the graph represented by the \textit{graphFilter} as
active edges. It is useful to first discuss an important semantic issue that arises when trying to define such an interface.

Suppose the user builds a filter $G_f$ over a symmetric graph $G$. Now, if the predicate used to filter the symmetric graph takes into account the directionality of the edge, then the resulting graph filter can become directed, which is unlikely to be what the user intends. Therefore, by default, filtering operations over a graphFilter should preserve whether the graph is symmetric unless the user specifies otherwise.

In our interface, we explicitly capture this requirement by defining constructors to construct both asymGraphFilters (directed) and symGraphFilters (undirected) filters. The remaining primitives in the interface are defined over graphFilters in general. Given these constraints, we define our filtering interface as follows:

- **makeFilter**$(G : symGraph, P : edge \mapsto bool) : symGraphFilter$
  
  Creates a symGraphFilter $G_f$ for the immutable symmetric graph $G$ with respect to the user-defined predicate $P$.

- **makeAsymFilter**$(G : graph, P : edge \mapsto bool) : asymGraphFilter$
  
  Creates an asymGraphFilter $G_f$ for the immutable graph $G$ with respect to the user-defined predicate $P$. The underlying graph can either be symmetric or asymmetric.

- **filterEdges**$(G_f : graphFilter) : int$
  
  Filters all active edges in $G_f$ that do not satisfy the predicate $P$ from $G_f$. The function mutates the supplied graphFilter, and returns the number of edges remaining in the graphFilter.

- **edgeMapPack**$(G_f : graphFilter, S : vertexSubset) : vertexSubset$
  
  Filters the edges incident to $v \in S$ that do not satisfy the predicate $P$ from $G_f$. Returns a vertexSubset on the same vertex set as $S$, where each vertex is augmented with its new degree in $G_f$.

In addition to these new primitives, the graphFilter object implements the same interface for graphs as used in the GBBS library, which is an extension of Ligra’s graph interface. Namely, it provides access to an underlying vertex object which supports fetching the vertex’s degree, fetching the $i$’th active edge incident to the vertex, mapping and reducing over its neighbors, and other internal primitives required to implement versions of edgemap, including the optimized sparse traversal described in Section 4.2. Note that the edges traversed by these functions depend on the current graph logically represented by the graphFilter, which is a function of the filterEdges and edgeMapPack calls made by the algorithm. By extending the functions in GBBS to treat the underlying graph type generically, the high-level functions in Ligra such as edgemap can be extended to handle both immutable graphs and graphFilters uniformly.

**Graph Filter Data Structure.** For simplicity, we describe only the symmetric version of the graph filter data structure, and note that the directed filter follows naturally by using two copies of the data structure described below, one for the in-edges and one for the out-edges.

We first review how edges are represented in uncompressed and compressed graphs in the framework, since the graph filter is stored similarly. Consider a vertex’s neighbors, $N(v)$. In the (uncompressed) CSR format, the neighbors are stored contiguously in an array. If the graph is compressed using one of the parallel compression methods from Ligra+ [67], the incident edges are divided into a number of blocks, where each block is sequentially encoded using a difference-encoding scheme with variable-length codes. Each block must be sequentially decoded to retrieve the neighbor

\[1\] However, this is precisely the behavior we want in triangle counting.
Figure 1: This figure illustrates our graph filter data structure. The original graph data is stored in the CSR format and is stored on NVRAM and is read-only. On DRAM, we maintain the filter structure that consists of blocks. Each block corresponds to \( F_B \) many edges in a consecutive range, and stores \( F_B \) many bits for these edges. In addition it stores an offset and the original block-id for each block, which are used by our algorithms. When an edge is deleted, its corresponding bit is set to 0, and the offsets of the blocks for the vertex are updated accordingly.

IDs within the block, but by choosing an appropriate block size, the edges incident to a high-degree vertex can be traversed in parallel across the blocks.

The graph filter is designed similarly to the CSR representation described above, and uses blocking similar to the parallel compression scheme from Ligra+ [67]. The design of our structure is inspired by similar bit-packed structures, most notably the cuckoo-filter by Eppstein et al. [31]. Figure 1 illustrates the graph filter structure and provides a visual representation of the description that follows. Given a user-defined block size, the data structure sets a \textit{filter block size}, \( F_B \), which is the user block size rounded up to next multiple of the number of bits in a machine word, inclusive (64 bits on modern architectures and \( \log n \) bits in theory). This block size is equal to the compression block size for compressed graphs, and can be tuned arbitrarily for uncompressed graphs. Next, the edges incident to each vertex are divided into blocks of size \( F_B \). For each block, we store \( F_B \) many bits, where the bits correspond one-to-one to the edges in the block. Each block also stores two words of metadata, which store the \textit{original block-ID} in the adjacency list that the block corresponds to, and the \textit{offset}, which stores the number of active edges before this block. The original block-IDs are necessary since over the course of the algorithm, only a subset of the original blocks used for a vertex may be currently present in the graph filter, and the data structure must remember the original position of each block. The offset is needed to copy all active edges incident to a vertex into an array with size proportional to the degree of the vertex.

The overall graph filter structure consists of the blocked bitsets per vertex. It packs the per-vertex blocks contiguously, and stores an offset to the start of each vertex’s blocks. It also stores each vertex’s current degree, as well as the number of blocks in the vertex structure. Finally, the structure stores an additional \( n \) bits of memory which are used to mark vertices as dirty. Due to space constraints, we describe details about the algorithms used to implement the graph filter in Appendix C.

\textbf{Memory Usage.} The overall memory requirement of a graphFilter is \( 3n \) words to store the degrees, offsets, and number of blocks, plus \( O(m) \) bits to store the bitset data and the metadata. The metadata increases the memory usage by a constant factor, since \( F_B \) is at least the size of a machine word, and so the metadata stored per block can be amortized against the bits stored in the block. The overall memory usage is therefore \( O(n + m / \log n) \) words of memory. We report the memory usage of the graph filter structure for our input graphs in Table 7 and discuss the results in detail in Section 5.4.
4.2 Memory-Efficient Parallel Graph Traversal

In this subsection we describe a cache-friendly and memory-efficient sparse graph traversal primitive which works in the PSAM. This technique is useful for obtaining PSAM algorithms for many of the problems studied in this paper. Graph traversals are a basic graph algorithm primitive, used throughout a wide array of fundamental graph algorithms. A parallel graph traversal starts with a frontier (subset) of seed vertices. It then runs a number of iterations, where in each iteration, the edges incident to the current frontier are explored, and vertices in this neighborhood are added to the next frontier based on some user-defined conditions. For concreteness, we adopt the terminology used by Ligra in what follows (see Section 3).

Memory-Inefficient Traversal in Existing Frameworks. Ligra implements the direction-optimization proposed by Beamer, which runs either a sparse (push-based) or dense (pull-based) traversal, based on the number of edges incident to the current frontier. The sparse traversal processes the out-edges of the current frontier to generate the next frontier. The dense traversal processes the in-edges of all vertices, and checks whether they have a neighbor in the current frontier. Ligra uses a threshold to decide which method to pick, which by default is a constant fraction of $m$ to ensure work-efficiency.

The dense method is memory-efficient—theoretically, it only requires $O(n)$ bits to store whether each output vertex is on the next frontier. On the other hand, the sparse method can be memory-inefficient, since it works by allocating an array with size proportional to the number of edges incident to the current frontier, which can be up to $O(m)$. In the PSAM, an array of this size can only be allocated in the large-memory, so the traversal will be inefficient. This is also true for the real graphs and machines that we tested in this paper.

The GBBS algorithms [30] use a blocked sparse traversal, referred to as edgemapblocked, that improves the cache-efficiency of parallel graph traversals by only writing to as many cache lines as the size of the newly generated frontier. Although this technique makes good uses of the caches, it is not memory-efficient, as it still allocates an intermediate array with size proportional to the number of edges incident to the current frontier which can be up to $O(m)$ in the worst-case.

edgeMapChunked. In this paper, we use a chunk-based approach which improves the memory-efficiency of the sparse (push-based) edgemap. Our approach, which we refer to as edgemapchunked, achieves the same cache performance as the edgemapblocked implementation used in GBBS [30], but significantly improves the intermediate memory usage of the approach. Due to space constraints, we provide the full details of our algorithm and its pseudocode in Appendix D in the supplementary materials.

The high-level idea of our approach is as follows. The algorithm first divides the edges that are to-be traversed into grouped units of work. This is done based on the underlying filter block size of the graph, $B$, which we will describe how to set momentarily. The edges incident to each vertex are partitioned into groups based on $B$. The algorithm then performs a work-assignment phase, which statically load-balances the work over the incident edges to $O(P)$ virtual threads. Next, in parallel for each virtual thread, it processes the edges assigned to the thread. For each block, it uses a thread-local allocator to obtain a chunk which is ensured to have sufficient space to store the output of mapping over the edges in the block. The chunks are stored in thread-local vectors. Upon completion of processing all edges incident to the vertexSubsetData, the algorithm aggregates all chunks stored in the thread-local vectors and uses a prefix-sum and a parallel copy to store the output neighbors contiguously in a single flat array. As discussed in Appendix D, the algorithm obtains the same cache-efficiency as the edgemapblocked implementation from [30], while improving the memory usage of the algorithm to $O(n)$ words. Obtaining this bound requires setting the underlying block size of the graph to the average degree, as discussed in the appendix. The overall work of the
procedure is \( O(\sum_{u \in U} \deg(u)) \) where \( U \) is the input vertex subset, and the depth is \( O(\log n + d_{\text{avg}}) \), which match the work and depth bounds of the previous edgemapblocked implementation.

### 4.3 Semi-Asymmetric Graph Algorithms

Due to space constraints, we provide formal specifications of the problems, and most of the details and analysis of the algorithms in Appendix F. The work and depth of each problem studied in this paper is listed in Table 1 of the introduction.

We consider mostly the same algorithms and problems as studied in Dhulipala et al. [30]. In addition, we consider 4 problems not discussed in that paper, but made publicly-available in the Graph Based Benchmark Suite (GBBS) [28], namely single-source widest path, spanning forest, approximate densest subgraph, and PageRank. GBBS provides shared-memory DRAM implementations for these problems, and these codes serve as the starting point for the implementations developed in this paper.

At a high-level, the main techniques we use to obtain theoretically-efficient semi-asymmetric versions of the 18 problems studied in this paper are the graph filtering and edgemapchunked techniques described in Section 4. We discuss the problem-specific details of applying these techniques, their work and depth complexities, and the amount of small-memory required for each problem in Appendix F.

### 5 Experiments

In this section, we describe our experimental results on a set of real-world graphs. We rely on the techniques described in Section 4 to extend the compression schemes designed in Ligra+ [67] and GBBS [30].

**Machine Configuration.** We run our NVRAM experiments on a 48-core, 2-socket machine (with two-way hyper-threading) with 2 \( \times \) 2.2Ghz Intel 24-core Cascade Lake processors (with 33MB L3 cache) and 375GB of DRAM. The machine is equipped with 3.024TB of NVRAM, which is spread across 12 252GB NVRAM DIMMS (6 per socket). All speedup numbers that we report in this setting are the running times on 48-cores with hyper-threading over the running time on a single thread.

**NVRAM Configuration.** Optane DC Persistent Memory can be used in either Memory Mode or App-Direct Mode.

In Memory Mode, the DRAM acts like a direct-mapped cache between L3 and the NVRAM for each socket. NVRAM in Memory Mode is transparent, providing access to higher memory capacity without software modification. In this mode, the read-write asymmetry of NVRAM is obscured by the DRAM cache. This causes the DRAM hit rate to dominate memory performance, encouraging traditional cache optimization methods. However, it is not possible to use NVRAM in Memory Mode as persistent storage since all accesses must go through DRAM.

In App-Direct Mode, NVRAM acts as byte-addressable storage independent of DRAM. The NVRAM is mapped as a file system, and accessed through memory-mapped files. As the name suggests, App-Direct Mode provides developers with direct access to the NVRAM, including both its persistence and its read-write asymmetry.

In all of our experiments, we configure the NVRAM to use App-Direct Mode unless otherwise mentioned. The block devices are configured using the fsdax mode, which removes the page cache from the I/O path for the device and allows mmap to directly map to the underlying memory.

**Graph Storage.** The approach used in this paper is to store two separate copies of the graph, one copy on the local NVRAM of each socket. We discuss the rationale behind this approach more in the supplementary materials in Appendix H.1 This duplication is 1.6x faster than using a single
| Graph Dataset  | Num. Vertices  | Num. Edges    | Avg. Degree |
|----------------|----------------|--------------|-------------|
| LiveJournal    | 4,847,571      | 85,702,474   | 17.6        |
| com-Orkut      | 3,072,627      | 234,370,166  | 76.2        |
| Twitter        | 41,652,231     | 2,405,026,092| 57.7        |
| ClueWeb        | 978,408,098    | 74,744,358,622| 76.3        |
| Hyperlink2014  | 1,724,573,718  | 124,141,874,032| 72.0        |
| Hyperlink2012  | 3,563,602,789  | 225,840,663,232| 63.3        |

Table 2: Graph inputs, including number of vertices, edges, and the average degree.

socket and 6.2x faster than using threads across both sockets to access graph data stored locally within a single socket.

**Scheduling.** Our programs use a work-stealing scheduler that we implemented. The scheduler is implemented similarly to Cilk \[16\] for parallelism. Threads can determine which socket they are running on by reading a thread-local variable. Furthermore, we pin threads to sockets by using `set affinit` to bind them to a particular virtual core.

**Options and Flags.** Our programs are compiled with the `g++` compiler (version 7.3.0) with the `-O3` flag. For parallel experiments, we use the command `numactl -i all` to balance the memory allocations across the sockets.

**Graph Data.** To show how our algorithms perform on graphs at different scales, we selected a representative set of real-world graphs of varying sizes. These graphs are Web graphs and social networks, which are low-diameter graphs that are frequently used in practice. We list the graphs used in our experiments in Table 2, which we symmetrized to obtain larger graphs and so that all of the algorithms would work on them. Hyperlink 2012 is the largest publicly-available real-world graph. We create weighted graphs for evaluating weighted BFS, Bellman-Ford, and Widest Path by selecting edge weights in the range \([1, \log n]\) uniformly at random. We process the ClueWeb, Hyperlink2014, and Hyperlink2012 graphs in the parallel byte-encoded compression format from Ligra+ \[67\], and process LiveJournal, com-Orkut, and Twitter in the uncompressed (CSR) format.

### 5.1 NVRAM vs. DRAM-only Performance

In this subsection, we study how fast our read-only codes are when run in DRAM (DRAM-only) compared to state-of-the-art shared-memory DRAM algorithms from GBBS run using DRAM-only. We also study how fast our read-only code is when run using DRAM-only, compared to when it is run on NVRAM.

For these experiments, we focus on the ClueWeb graph since it is the largest graph among our inputs that all of the codes (GBBS and ours) can successfully process using DRAM-only. Table 3 reports the results of these experiments for ClueWeb, including running times for the problems reported in \[30\] on a 72-core machine with 2-way hyper-threading and 1TB of RAM.

Comparing our read-only codes to GBBS in DRAM-only shows that our code is faster than the original GBBS implementations (between 1.1x faster to 1.17x slower) on most algorithms. The main exception is for triangle counting, where our new code is 1.78x slower than the GBBS code in DRAM-only. We discuss the reason for this slowdown in Appendix H.2. Some of our codes (connectivity and approximate densest subgraph) are faster than the GBBS implementations due to optimizations made in our codes that are absent in GBBS, such as a faster implementation of graph contraction.

Our read-only codes when run using NVRAM are only about 5% slower on average than when run using DRAM-only. This difference in performance is likely due to the higher cost of NVRAM reads compared to DRAM reads.

Taken together, these results show that for many parallel graph algorithms, the performance gap between shared-memory DRAM algorithms and NVRAM algorithms can be bridged by adopting...
Table 3: Parallel running times (in seconds) of the implementations from GBBS (GBBS) and our implementations (Us) for problems considered in this paper on the ClueWeb graph. The machine configuration reports whether the experiment was run fully using DRAM (DRAM-only), or whether it uses NVRAM in App-Direct Mode (NVRAM). The first column reports the DRAM-only numbers of GBBS on a 2-way hyper-threaded 72-core machine with 1TB of memory reported in [30]. The second column reports the running times we observed when running GBBS codes in DRAM-only mode on our machine. The last two columns report the running times of our codes when run in DRAM-only mode, and using NVRAM. We use — to denote times that are not reported in [30].

| Implementations              | (GBBS) | (GBBS) | (Us) | (Us) |
|------------------------------|--------|--------|------|------|
| Num. hyper-threads          | 144    | 96     | 96   | 96   |
| DRAM                         | 1 TB   | 375    | 375  | 375  |
| Machine configuration        | DRAM-only | DRAM-only | NVRAM |
| BFS                          | 2.29   | 2.64   | 2.05 | 2.35 |
| Weighted BFS                 | 14.4   | 26.6   | 24.0 | 25.9 |
| Bellman-Ford                 | 16.2   | 27.3   | 25.5 | 26.3 |
| Single-Source Widest Path    | —      | 29.9   | 27.1 | 29.6 |
| Single-Source Betweenness    | 27.7   | 24.4   | 22.7 | 23.1 |
| $O(k)$-Spanner               | —      | 16.6   | 13.0 | 15.1 |
| LDD                          | 3.62   | 4.08   | 3.46 | 3.72 |
| Connectivity                 | 11.2   | 8.63   | 7.9  | 8.29 |
| Spanning Forest              | —      | 15.7   | 14.7 | 15.0 |
| Biconnectivity               | 48.7   | 62.3   | 55.8 | 57.3 |
| MIS                          | 8.44   | 12.6   | 12.0 | 12.9 |
| Maximal Matching             | 31.8   | 46.4   | 41.6 | 42.9 |
| Graph Coloring               | 49.8   | 54.1   | 53.8 | 63.8 |
| Apx Set Cover                | 28.1   | 32.3   | 49.0 | 58.8 |
| $k$-core                     | 62.7   | 66.3   | 66.0 | 70.3 |
| Apx Densest Subgraph         | —      | 28.2   | 11.8 | 12.5 |
| Triangle Counting            | 272    | 279    | 485  | 498  |
| PageRank Iteration           | —      | 5.73   | 5.87 | 5.94 |
| PageRank                     | —      | 204    | 209  | 217  |

5.2 Comparison to other NVRAM approaches

In this section, we compare the performance of our implementations to the performance obtained by a recent paper studying using NVRAM for large-scale parallel graph processing, and also to other approaches of using the new NVRAM technology. First, we compare our implementations to the recently developed NVRAM implementations based on Galois by Gill et al. [34]. We then compare our running times using NVRAM in App-Direct Mode to the unmodified shared-memory codes from GBBS when run on a larger-than-memory dataset using Memory Mode.

Comparison with Galois [34]. In a very recent paper, Gill et al. [34] study the performance of three state-of-the-art graph processing systems, including Galois [58], GraphIt [81], and GAP [6] when run on NVRAM configured to use Memory Mode. They perform their experiments on a machine nearly identical to ours, equipped with the same amount of DRAM in an identical configuration. However, their machine is configured with 6.144TB of NVRAM, using 12 NVRAM DIMMs that have 512GB of capacity each.

Gill et al. [34] find that their Galois-based codes outperform GraphIt and GAP by between 1.6–3.6x on average for three large graphs inputs, including the ClueWeb and Hyperlink2012 graphs. There are several important differences between our experiments and theirs which are worth explicitly mentioning. First, their experiments run on the directed version of the Hyperlink2012 graph, which has $1.75 \times$ fewer edges than the symmetrized version (225.8B vs. 128.7B edges). The
Table 4: Parallel running time in seconds for Galois implementations using Memory Mode (Gal-MM) and unmodified GBBS codes run using Memory Mode (GBBS-MM) for the Hyperlink2012 graph. The columns (Gal-MM/Us) and (GBBS-MM/Us) provide the ratio of the Gal-MM and GBBS-MM times compared to our NVRAM codes run using App-Direct Mode for the same problem and graph. Note that the Gal-MM times are obtained using the directed version of the Hyperlink2012 graph. The times reported for Galois are courtesy of the authors, who run on an identically configured machine, but with 6TB of NVRAM. We mark entries for problems that they do not report numbers for with —. All of our experiments are run on a system with 375GB of DRAM, extended to 1.5TB of memory using Memory Mode, and using 48 cores with hyper-threading.

The symmetrized graph exhibits a massive connected component, which a BFS, betweenness centrality, or shortest-path algorithm will process for most source vertices. Comparatively, running shortest path and search algorithms on the directed graph is much faster, as reported in [29].

We show the experimental results for their Galois-based system on the directed Hyperlink2012 graph in Table 4 and are grateful to the authors of [34] for providing us with the exact numbers reported in their paper. On all problems other than betweenness centrality, our NVRAM codes are $1.43 - 2.88x$ faster than their fastest reported times. We note that their codes use the maximum degree vertex in the directed graph as the source for BFS, SSSP, and betweenness centrality. We also used the maximum degree vertex in the symmetric graph to make a fair comparison, but running these codes on the symmetric graph biases the comparison against our implementations, since they must perform more work, and so the comparison must be taken in light of this difference. Despite the fact that our algorithm must perform more work, our running times for BFS are $2.88x$ faster than the time reported for Galois, and our SSSP time is $1.43x$ faster. For connectivity and PageRank, our times are $2.09x$ faster and $2.12x$ faster respectively. Our betweenness centrality time may be slower due to the fact that we are running on the symmetrized version of the graph. We note that the authors also report running times for an implementation of $k$-core which computes the vertices participating in a single $k$-core, for a given value of $k$. This requires significantly fewer rounds than the $k$-core computation studied in this paper, which computes the coreness number of every vertex, or the largest $k$ such that the vertex participates in the $k$-core. They report that their algorithm requires 49.2 seconds to find the 100-core of the Hyperlink2012 graph. Our code finds all $k$-cores of this graph in 259 seconds using NVRAM, which requires running 130,728 iterations.
of the peeling algorithm and also discovers the value of the largest $k$-core supported by the graph ($k_{\text{max}} = 10565$).

In summary, our results show that our new codes when run on NVRAM using App-Direct Mode are 1.86x faster on average than the Galois codes run using Memory Mode. It would be interesting to make this comparison more direct in future work by comparing both systems on symmetric versions of the same graphs.

**Algorithms using Memory Mode.** Next, we evaluate the performance of using memory mode to run unmodified GBBS codes on graphs that are larger than the DRAM size of the machine. Since our machine has 375GB of fast memory, this comparison is only meaningful for the Hyperlink2012 graph, which is the only one of our graphs where both the graph and intermediate data used by the algorithm are larger than DRAM. We run our Memory Mode experiments on the same machine with 3TB of NVRAM, where 1.5TB is configured to be used in Memory Mode.

Table 4 reports the parallel running times of the GBBS codes using NVRAM configured in Memory Mode for the Hyperlink2012 graph. The last column of the table shows the ratio of the GBBS times using Memory Mode to our NVRAM times using App-Direct Mode. The experimental results show that in all but two cases our running times are faster (between 1.15–2.92x). Our new codes are slower for graph coloring and triangle counting (1.1x slower and 2.12x slower respectively). The modest slowdown for graph coloring could be due to caching effects for the Memory Mode execution, and due to the fact that our NVRAM code gets no benefit due to caching in memory since reads in App-Direct Mode bypass DRAM caching. For the case of triangle counting, the directed version of the Hyperlink2012 graph fits in about 180GB of memory, which fits within the DRAM of our machine and will therefore reside in memory. We note that we also ran our Memory Mode experiments on the ClueWeb graph, which fits in memory. The running times we observed incurred a between 5–10% performance penalty compared to the DRAM-only running times for the ClueWeb graph reported in Table 3.

In summary, our results for this experiment show that the techniques developed in this paper produce meaningful improvements (1.87x speedup on average, across all 18 problems) over simply running unmodified shared-memory graph algorithms using Memory Mode to handle graph sizes that are larger than DRAM.

### 5.3 Scalability

In this subsection, we discuss the scalability of the implementations of semi-asymmetric algorithms developed in this paper. Tables 5 and 6 show the running times for our implementations on all of our graphs. In all of these experiments, we store all of the graph data in NVRAM and use DRAM for all temporary data. As described earlier, we have two copies of the graph on NVRAM, one on each chip.

**SSSP Problems.** Our BFS, weighted BFS, Bellman-Ford, and betweenness centrality implementations achieve between parallel speedups of 31–51x across all inputs. For $O(k)$-Spanner, we achieve between 39–51x speedup across all inputs. All of our codes use the memory-efficient sparse traversal (i.e., `edgemapchunked`) designed in this paper. We note that the new weighted-SSSP implementations using `edgemapchunked` are up to 2x more memory-efficient than the implementations from [30]. We ran our $O(k)$-Spanner implementation with $k$ set to $\lceil \log_2 n \rceil$ by default.

**Connectivity Problems.** Our low-diameter decomposition implementation achieves a speedup of 28–42x across all inputs. Our connectivity and spanning forest implementations achieve speedups of 37–53x across all inputs. Our biconnectivity implementation achieves a speed up of 38–46x across all inputs. Although the average degree in our inputs is closer to $\Theta(\log n)$, we found that setting $\beta = 0.2$ performs best in practice, and creates significantly fewer than $m\beta = m/5$ inter-cluster edges predicted by the theoretical bound [56], due to many duplicate edges that get removed.
Application | LiveJournal (1) | Orkut (48h) (SU) | Twitter (1) (48h) (SU)
--- | --- | --- | ---
BFS | 0.660 | 0.016 | 41.2 | 0.697 | 0.019 | 41.4 | 6.03 | 0.130 | 46.3
Weighted BFS | 6.01 | 0.186 | 32.3 | 4.78 | 0.129 | 37.0 | 59.1 | 1.25 | 47.2
Bellman-Ford | 4.27 | 0.111 | 38.4 | 7.19 | 0.201 | 40.7 | 42.4 | 1.82 | 45.2
Widest Path | 4.37 | 0.109 | 40.0 | 6.54 | 0.163 | 40.1 | 55.2 | 1.55 | 48.0
BC | 4.87 | 0.095 | 51.2 | 4.33 | 0.084 | 51.5 | 56.0 | 1.23 | 45.5
O(k)-Spanner | 1.73 | 0.042 | 41.1 | 2.92 | 0.057 | 51.2 | 38.8 | 0.878 | 41.1
LDD | 0.56 | 0.020 | 28.0 | 0.435 | 0.019 | 22.8 | 10.3 | 0.244 | 42.2
Connectivity | 1.43 | 0.033 | 43.3 | 2.25 | 0.042 | 35.3 | 38.6 | 0.795 | 48.5
Spanning Forest | 1.56 | 0.039 | 40.0 | 2.39 | 0.048 | 41.7 | 42.3 | 0.880 | 48.0
Biconnectivity | 11.1 | 0.289 | 38.4 | 11.5 | 0.277 | 41.5 | 191 | 4.39 | 43.5
MIS | 1.97 | 0.043 | 45.8 | 1.24 | 0.069 | 49.5 | 43.9 | 0.929 | 44.1
Maximal Matching | 4.59 | 0.138 | 33.2 | 5.30 | 0.143 | 37.0 | 61.0 | 1.36 | 44.6
Graph Coloring | 7.94 | 0.433 | 18.3 | 12.8 | 0.776 | 16.4 | 182 | 7.15 | 25.4
Apx Set Cover | 11.9 | 0.461 | 25.8 | 10.2 | 0.537 | 18.9 | 127 | 5.21 | 24.3
k-core | 4.66 | 0.498 | 9.35 | 9.09 | 1.01 | 9.00 | 103 | 5.60 | 18.3
Apx Densest Subgraph | 2.35 | 0.048 | 48.9 | 2.58 | 0.056 | 46.0 | 36.3 | 0.835 | 43.4
Triangle Counting | 24.9 | 0.392 | 63.5 | 152 | 2.62 | 58.0 | 3734 | 79.6 | 46.9
PageRank Iteration | 1.07 | 0.019 | 56.3 | 1.24 | 0.030 | 54.6 | 22.0 | 0.523 | 42.0

Table 5: Running times (in seconds) of our algorithms on small graph inputs on a 48-core machine (with 2-way hyper-threading) where (1) is the single-thread time, (48h) is the 48 core time using 2-way hyper-threading, and (SU) is the parallel speedup (single-thread time divided by 48-core time). We mark experiments that did not finish within 5 hours with —.

| Application | ClueWeb (1) | Hyperlink2014 (48h) (SU) | Hyperlink2012 (1) (48h) (SU)
--- | --- | --- | ---
BFS | 99.0 | 2.35 | 42.1 | 220 | 5.10 | 43.1 | 561 | 12.2 | 45.9
Weighted BFS | 1120 | 25.9 | 43.2 | 1782 | 40.7 | 43.7 | 4618 | 102 | 45.2
Bellman-Ford | 1201 | 26.3 | 45.6 | 1534 | 32.8 | 46.7 | 3760 | 82.3 | 45.6
Widest Path | 1258 | 29.6 | 42.5 | 1614 | 41.1 | 39.2 | 3479 | 77.5 | 44.8
BC | 793 | 23.1 | 34.3 | 1317 | 30.7 | 42.8 | 3267 | 68.5 | 47.6
O(k)-Spanner | 577 | 15.1 | 38.2 | 857 | 7.39 | 36.8 | 2219 | 55.1 | 40.2
LDD | 145 | 3.72 | 38.9 | 272 | 7.39 | 36.8 | 985 | 24.0 | 41.0
Connectivity | 359 | 8.29 | 43.3 | 643 | 15.8 | 40.6 | 1564 | 36.3 | 43.2
Spanning Forest | 563 | 15.0 | 37.5 | 1047 | 29.0 | 36.1 | 2439 | 61.3 | 38.3
Biconnectivity | 2502 | 15.0 | 43.6 | 4245 | 94.7 | 44.8 | 10930 | 24.0 | 41.0
MIS | 593 | 12.9 | 45.9 | 989 | 22.5 | 43.9 | 2308 | 52.3 | 44.1
Maximal Matching | 1887 | 42.9 | 43.9 | 3214 | 72.9 | 44.1 | 7280 | 166 | 43.1
Graph Coloring | 2580 | 63.8 | 40.4 | 3638 | 88.7 | 41.0 | 10880 | 276 | 39.4
Apx Set Cover | 1965 | 58.8 | 33.4 | 2120 | 65.0 | 32.6 | 7968 | 193 | 41.2
k-core | 2714 | 70.3 | 38.6 | 3652 | 96.0 | 38.0 | 8348 | 215 | 38.8
Apx Densest Subgraph | 543 | 12.5 | 43.4 | 775 | 17.1 | 45.3 | 1930 | 42.2 | 45.7
Triangle Counting | — | 409 | 8.99 | — | 5722 | — | — | 3529 | —
PageRank Iteration | 266 | 5.94 | 44.7 | 409 | 8.99 | 45.4 | 1033 | 23.6 | 43.5

Table 6: Running times (in seconds) of our algorithms on large graph inputs on a 48-core machine (with 2-way hyper-threading) where (1) is the single-thread time, (48h) is the 48 core time using 2-way hyper-threading, and (SU) is the parallel speedup (single-thread time divided by 48-core time). We mark experiments that did not finish within 5 hours with —.

Covering Problems. Our MIS, maximal matching, and graph coloring implementations achieve speedups of 43–49x, 33–44x, and 16–39x, respectively. Our MIS implementation is similar to the implementation from GBBS. Our maximal matching implementation implements several new optimizations over the implementation from GBBS, such as using a parallel hash table to aggregate edges that will be processed in a given round. These optimizations result in our code (using the graph
| Graph       | |E| |Graph Size| Num. Blocks| Mem. Usage |
|-------------|--------------|----------------|-----------|------------|-----------|
| LiveJournal | 0.0857 B     | 0.355 GB       | 4.88·10^{-3} B | 0.0761 GB |
| com-Orkut   | 0.234 B      | 0.895 GB       | 3.26·10^{-3} B | 0.110 GB  |
| Twitter     | 2.40 B       | 9.26 GB        | 0.0468 B     | 1.47 GB   |
| ClueWeb     | 74.7 B       | 100 GB         | 1.07 B       | 35.9 GB   |
| Hyperlink2014| 124 B      | 186 GB         | 1.86 B       | 62.1 GB   |
| Hyperlink2012| 225 B      | 354 GB         | 3.81 B       | 125 GB    |

Table 7: This table reports statistics about graph filters for each of our graph inputs, including the number of edges, the graph size on disk (gigabytes), the number of blocks constructed by the filter (billions) and the total memory usage of the filter (gigabytes). The block size for the graph filter, $F_B$, is set to 256 for all graphs.

filter) running faster than the original code when run in DRAM-only, outperforming the 72-core DRAM-only times reported in [30] for some graphs. Finally, the graph coloring implementation used in GBBS also achieves similar speedups (11–56x) when run on the same set of graph inputs.

Our graph coloring code colors our inputs with the same number of colors as those reported in [30].

**Substructure Problems.** Our $k$-core, approximate densest subgraph, and triangle counting implementations achieve speedups of 9–38x, 43–48x, and 46–63x, respectively. Our code achieves similar speedups and running times on NVRAM compared to the previous times reported in [30]. We ran the approximate densest subgraph implementation with $\epsilon = 0.001$ which produces subgraphs of similar density to the 2-approximation of Charikar [21]. Lastly, our triangle counting algorithm uses the iterator defined over graph filters to perform parallel intersection. The running time of our implementation is affected by the number of edges that must be decoded (for compressed graph inputs), and we discuss how the number of edges to decode affects the running time of the triangle counting implementation in more detail in Appendix H.2.

**Eigenvector Problems.** Our PageRank implementation achieves a parallel speedup of 42–56x. Our implementation is based on the PageRank implementation from Ligra, and improves the parallel scalability of the Ligra-based code by aggregating the neighbor’s contributions for a given vertex in parallel. We ran our PageRank implementation with $\epsilon = 10^{-6}$, and a damping factor of 0.85.

### 5.4 Techniques

Finally this subsection, we consider the experimental characteristics of our techniques in terms of memory-efficiency and applicability to various problems. Due to space constraints, we discuss additional experiments about the efficacy and applicability of our techniques in Appendix H.2.

**Graph Filter Size.** In Table 7, we report the number of blocks used, and the graph filter size (in gigabytes) for each of our graphs. We report the uncompressed sizes for our three small inputs (LiveJournal, com-Orkut, and Twitter) and the compressed sizes for our three large inputs (ClueWeb, Hyperlink2012, and Hyperlink2014). For our uncompressed inputs, the size of the graph filter is between 4.6–8.1x smaller than the size of the uncompressed graph. For our compressed inputs, the size of the filter is between 2.7–2.9x smaller than the size of the compressed graph. We note that the memory sizes for the graph filter that we report in Table 7 include the 16n bytes required to store vertex information, as well as the block metadata.

### 6 Related Work

A significant amount of research has focused on reducing expensive writes to NVRAMs. Early work has designed algorithms for database operators [23, 73, 74]. Blelloch et al. [12, 7, 11] formally define computational models to capture the asymmetric read-write cost on NVRAMs, and many algorithms and lower bounds have been obtained based on the models [40, 36, 14, 8]. Other models, algorithms, and systems to reduce writes or memory footprint on NVRAMs have also been described [20, 59, 19, 49, 78, 22, 62].

15
Persistence is a key property of the NVRAMs due to their non-volatility. From the algorithmic perspective, many new persistent data structures have been designed for NVRAMs [10, 9, 4, 64, 60, 24, 33]. There has also been systems research on automatic recovery schemes and transactional memory for NVRAMs [48, 75, 3, 44, 80, 27, 47, 84]. Blelloch et al. [13] introduce a programming model for fault-tolerant programming on NVRAMs. Finally, there has been several recent papers on benchmarking performance on NVRAMs [46, 72, 39].

Parallel graph processing frameworks have received significant attention due to the need to quickly analyze large graphs. The only previous graph processing work targeting NVRAMs is by Gill et al. [34], which we compare with in Section 5. Dhulipala et al. [29, 30] design the Graph Based Benchmark Suite, and show that the largest publicly-available graph, the Hyperlink 2012 graph, can be efficiently processed on a single multicore machine. We compare with their algorithms in Section 5. Other multicore frameworks include Galois [58], Ligra [65, 67], Polymer [79], Gemini [85], GraphGrind [69], Green-Marl [37], GraphMat [71], Grazelle [35], and GraphIt [81]. We refer the reader to surveys by Yan et al. [76], McCune et al. [50] and Shi et al. [63] for detailed discussions of various frameworks for different settings.

7 Conclusion
In this paper, we have introduced a semi-asymmetric approach to designing parallel graph algorithms that avoid writing to the NVRAM and use DRAM proportional to the number of vertices. We have designed a new model, the Parallel Semi-Asymmetric Model, and have shown that all of our algorithms are theoretically-efficient, and often work-optimal in the model. Our empirical study shows that efficient parallel semi-asymmetric graph algorithms can bridge the performance gap between NVRAM and DRAM. This enables NVRAMs, which are more cost-efficient and support larger capacities than traditional DRAM, to be used for large-scale graph processing. Future work includes designing and implementing algorithms for other graph problems using a semi-asymmetric approach.

Acknowledgements
This research was supported in part by NSF grants #CCF-1408940, #CCF-1533858, and #CCF-1629444, NSF CAREER Award #CCF-1845763, DOE Early Career Award #de-sc0018947, DARPA SDH Award #HR0011-18-3-0007, and Applications Driving Architectures (ADA) Research Center, a JUMP Center co-sponsored by SRC and DARPA.

References
[1] J. Abello, A. L. Buchsbaum, and J. R. Westbrook. A functional approach to external graph algorithms. Algorithmica, 32(3):437–458, Mar 2002.
[2] A. Aggarwal and J. S. Vitter. The Input/Output complexity of sorting and related problems. Commun. ACM, 31(9), 1988.
[3] M. Alshboul, H. Elnawawy, R. Elkhouly, K. Kimura, J. Tuck, and Y. Solihin. Efficient checkpointing with recompute scheme for non-volatile main memory. ACM Transactions on Architecture and Code Optimization (TACO), 16(2):18, 2019.
[4] H. Attiya, O. Ben-Baruch, P. Fatourou, D. Hendler, and E. Kosmas. Tracking in order to recover: Recoverable lock-free data structures. arXiv preprint arXiv:1905.13600, 2019.
[5] S. Beamer, K. Asanović, and D. Patterson. Direction-optimizing breadth-first search. In SC, 2012.
[6] S. Beamer, K. Asanovic, and D. A. Patterson. The GAP benchmark suite. *CoRR*, abs/1508.03619, 2015.

[7] N. Ben-David, G. E. Blelloch, J. T. Fineman, P. B. Gibbons, Y. Gu, C. McGuffey, and J. Shun. Parallel algorithms for asymmetric read-write costs. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, 2016.

[8] N. Ben-David, G. E. Blelloch, J. T. Fineman, P. B. Gibbons, Y. Gu, C. McGuffey, and J. Shun. Implicit decomposition for write-efficient connectivity algorithms. In *IPDPS*, 2018.

[9] N. Ben-David, G. E. Blelloch, M. Friedman, and Y. Wei. Delay-free concurrency on faulty persistent memory. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 253–264, 2019.

[10] N. Ben-David, G. E. Blelloch, Y. Sun, and Y. Wei. Multiversion concurrency with bounded delay and precise garbage collection. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 241–252. ACM, 2019.

[11] G. E. Blelloch, J. T. Fineman, P. B. Gibbons, Y. Gu, and J. Shun. Sorting with asymmetric read and write costs. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, 2015.

[12] G. E. Blelloch, J. T. Fineman, P. B. Gibbons, Y. Gu, and J. Shun. Efficient algorithms with asymmetric read and write costs. In *European Symposium on Algorithms (ESA)*, 2016.

[13] G. E. Blelloch, P. B. Gibbons, Y. Gu, C. McGuffey, and J. Shun. The parallel persistent memory model. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, 2018.

[14] G. E. Blelloch, Y. Gu, J. Shun, and Y. Sun. Parallel write-efficient algorithms and data structures for computational geometry. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, 2018.

[15] G. E. Blelloch, H. V. Simhadri, and K. Tangwongsan. Parallel and I/O efficient set covering algorithms. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, 2012.

[16] R. D. Blumofe, C. F. Joerg, B. C. Kuszmaul, C. E. Leiserson, K. H. Randall, and Y. Zhou. Cilk: An efficient multithreaded runtime system. In *ACM Symposium on Principles and Practice of Parallel Programming (PPOPP)*, 1995.

[17] P. Boldi and S. Vigna. The WebGraph framework I: Compression techniques. In *International World Wide Web Conference (WWW)*, 2004.

[18] S. Brin and L. Page. The anatomy of a large-scale hypertextual web search engine. In *International World Wide Web Conference (WWW)*, pages 107–117, 1998.

[19] T. Cai, F. Chen, Q. He, D. Niu, and J. Wang. The matrix kv storage system based on nvm devices. *Micromachines*, 10(5):346, 2019.

[20] E. Carson, J. Demmel, L. Grigori, N. Knight, P. Koanantakool, O. Schwartz, and H. V. Simhadri. Write-avoiding algorithms. In *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, 2016.
[21] M. Charikar. Greedy approximation algorithms for finding dense components in a graph. In International Workshop on Approximation Algorithms for Combinatorial Optimization, pages 84–95, 2000.

[22] Q. Chen, H. Lee, Y. Kim, H. Y. Yeom, and Y. Son. Design and implementation of skiplist-based key-value store on non-volatile memory. Cluster Computing, 22(2):361–371, 2019.

[23] S. Chen, P. B. Gibbons, and S. Nath. Rethinking database algorithms for phase change memory. In Conference on Innovative Data Systems Research (CIDR), 2011.

[24] N. Cohen, R. Guerraoui, and M. I. Zablotschi. The inherent cost of remembering consistently. In ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2018.

[25] S. M. Collection. https://sparse.tamu.edu/.

[26] T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein. Introduction to Algorithms (3. ed.). MIT Press, 2009.

[27] A. Correia, P. Felber, and P. Ramalhete. Romulus: Efficient algorithms for persistent transactional memory. In ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), pages 271–282, 2018.

[28] L. Dhulipala, G. E. Blelloch, and J. Shun. https://github.com/ldhulipala/gbbs.

[29] L. Dhulipala, G. E. Blelloch, and J. Shun. Julienne: A framework for parallel graph algorithms using work-efficient bucketing. In ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2017.

[30] L. Dhulipala, G. E. Blelloch, and J. Shun. Theoretically efficient parallel graph algorithms can be fast and scalable. In ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), pages 293–304, 2018.

[31] D. Eppstein, M. T. Goodrich, M. Mitzenmacher, and M. R. Torres. 2-3 cuckoo filters for faster triangle listing and set intersection. In pods, pages 247–260, 2017.

[32] J. Feigenbaum, S. Kannan, A. McGregor, S. Suri, and J. Zhang. On graph problems in a semi-streaming model. Theoretical Computer Science, 348(2-3):207–216, 2005.

[33] M. Friedman, M. Herlihy, V. Marathe, and E. Petrank. A persistent lock-free queue for non-volatile memory. In ACM Symposium on Principles and Practice of Parallel Programming (PPOPP), volume 53, pages 28–40, 2018.

[34] G. Gill, R. Dathathri, L. Hoang, R. Peri, and K. Pingali. Single machine graph analytics on massive datasets using intel optane DC persistent memory. CoRR, abs/1904.07162, 2019.

[35] S. Grossman, H. Litz, and C. Kozyrakis. Making pull-based graph processing performant. In ACM Symposium on Principles and Practice of Parallel Programming (PPOPP), pages 246–260, 2018.

[36] Y. Gu, Y. Sun, and G. E. Blelloch. Algorithmic building blocks for asymmetric memories. In European Symposium on Algorithms (ESA), 2018.
[37] S. Hong, H. Chafi, E. Sedlar, and K. Olukotun. Green-Marl: a DSL for easy and efficient graph analysis. In ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), pages 349–362, 2012.

[38] Intel. www.intel.com/content/www/us/en/products/docs/processors/xeon/xeon-scalable-platform-where-to-buy.html, 2019.

[39] J. Izraelevitz, J. Yang, L. Zhang, J. Kim, X. Liu, A. Memaripour, Y. J. Soh, Z. Wang, Y. Xu, S. R. Dulloor, et al. Basic performance measurements of the Intel Optane DC persistent memory module. arXiv preprint arXiv:1903.05714, 2019.

[40] R. Jacob and N. Sitchinava. Lower bounds in the asymmetric external memory model. In ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2017.

[41] J. Jaja. Introduction to Parallel Algorithms. Addison-Wesley Professional, 1992.

[42] L. Kliemann. Engineering a bipartite matching algorithm in the semi-streaming model. In Algorithm Engineering - Selected Results and Surveys, volume 9220 of Lecture Notes in Computer Science, pages 352–378. 2016.

[43] H. Kwak, C. Lee, H. Park, and S. Moon. What is twitter, a social network or a news media? In International World Wide Web Conference (WWW), 2010.

[44] L. Lersch, W. Lehner, and I. Oukid. Persistent buffer management with optimistic consistency. In International Workshop on Data Management on New Hardware, pages 14:1–14:3, 2019.

[45] J. Leskovec and A. Krevl. SNAP Datasets: Stanford large network dataset collection. 2014.

[46] J. Liu and S. Chen. Initial experience with 3D XPoint main memory. In IEEE International Conference on Data Engineering Workshops (ICDEW), pages 300–305, 2019.

[47] Q. Liu, J. Izraelevitz, S. K. Lee, M. L. Scott, S. H. Noh, and C. Jung. ido: Compiler-directed failure atomicity for nonvolatile memory. In Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), pages 258–270, 2018.

[48] Q. Liu, J. Izraelevitz, S. K. Lee, M. L. Scott, S. H. Noh, and C. Jung. Compiler-directed failure atomicity for nonvolatile memory. Technical report, Virginia Polytechnic Institute, 2019.

[49] X. Liu, Y. Hua, X. Li, and Q. Liu. Write-optimized and consistent rdma-based nvm systems. arXiv preprint arXiv:1906.08173, 2019.

[50] R. R. McCune, T. Weninger, and G. Madey. Thinking like a vertex: A survey of vertex-centric frameworks for large-scale distributed graph processing. ACM Comput. Surv., 48(2), Oct. 2015.

[51] A. McGregor. Graph stream algorithms: A survey. SIGMOD Rec., 43(1):9–20, May 2014.

[52] F. McSherry, M. Isard, and D. G. Murray. Scalability! But at what COST? In Workshop on Hot Topics in Operating Systems (HotOS), 2015.

[53] K. Mehlhorn and U. Meyer. External-memory breadth-first search with sublinear i/o. In European Symposium on Algorithms (ESA), pages 723–735, 2002.

[54] R. Meusel, S. Vigna, O. Lehmann, and C. Bizer. The graph structure in the web—analyzed on different aggregation levels. The Journal of Web Science, 1(1), 2015.
[55] G. L. Miller, R. Peng, A. Vladu, and S. C. Xu. Improved parallel algorithms for spanners and hopsets. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 192–201, 2015.

[56] G. L. Miller, R. Peng, and S. C. Xu. Parallel graph decompositions using random shifts. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, 2013.

[57] S. Muthukrishnan. Data streams: Algorithms and applications. *Foundations and Trends in Theoretical Computer Science*, 1(2):117–236, 2005.

[58] D. Nguyen, A. Lenharth, and K. Pingali. A lightweight infrastructure for graph analytics. In *ACM Symposium on Operating Systems Principles (SOSP)*, 2013.

[59] R. Nissim and O. Schwartz. Revisiting the i/o-complexity of fast matrix multiplication with recomputations. In *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, pages 714–716, 2019.

[60] W. Pan, T. Xie, and X. Song. Hart: A concurrent hash-assisted radix tree for dram-pm hybrid memory systems. In *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, 2019.

[61] R. Pearce, M. Gokhale, and N. M. Amato. Multithreaded asynchronous graph traversal for in-memory and semi-external memory. In *ACM/IEEE International Conference for High Performance Computing, Networking, Storage and Analysis*, pages 1–11, 2010.

[62] Y. Shen and Z. Zou. Efficient subgraph matching on non-volatile memory. In *International Conference on Web Information Systems Engineering*, pages 457–471. Springer, 2017.

[63] X. Shi, Z. Zheng, Y. Zhou, H. Jin, L. He, B. Liu, and Q.-S. Hua. Graph processing on GPUs: A survey. *ACM Comput. Surv.*, 50(6), Jan. 2018.

[64] T. Shull, J. Huang, and J. Torrellas. Autopersist: an easy-to-use java nvm framework based on reachability. In *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 316–332, 2019.

[65] J. Shun and G. E. Blelloch. Ligra: A lightweight graph processing framework for shared memory. In *ACM Symposium on Principles and Practice of Parallel Programming (PPOPP)*, 2013.

[66] J. Shun, L. Dhulipala, and G. E. Blelloch. A simple and practical linear-work parallel algorithm for connectivity. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, 2014.

[67] J. Shun, L. Dhulipala, and G. E. Blelloch. Smaller and faster: Parallel processing of compressed graphs with Ligra+. In *Data Compression Conference (DCC)*, 2015.

[68] J. Shun and K. Tangwongsan. Multicore triangle computations without tuning. In *IEEE International Conference on Data Engineering (ICDE)*, 2015.

[69] J. Sun, H. Vandierendonck, and D. S. Nikolopoulos. GraphGrind: Addressing load imbalance of graph partitioning. In *International Conference on Supercomputing (ICS)*, pages 16:1–16:10, 2017.
[70] P. Sun, Y. Wen, T. N. B. Duong, and X. Xiao. Graphmp: An efficient semi-external-memory big graph processing system on a single machine. In *IEEE International Conference on Parallel and Distributed Systems (ICPADS)*, pages 276–283, 2017.

[71] N. Sundaram, N. Satish, M. M. A. Patwary, S. R. Dulloor, M. J. Anderson, S. G. Vadlamudi, D. Das, and P. Dubey. GraphMat: High performance graph analytics made productive. *Proc. VLDB Endow.*, 8(11):1214–1225, July 2015.

[72] A. van Renen, L. Vogel, V. Leis, T. Neumann, and A. Kemper. Persistent memory i/o primitives. In *International Workshop on Data Management on New Hardware*, pages 12:1–12:7, 2019.

[73] S. D. Viglas. Adapting the B+-tree for asymmetric I/O. In *Advances in Databases and Information Systems (ADBIS)*, 2012.

[74] S. D. Viglas. Write-limited sorts and joins for persistent memory. *PVLDB*, 7(5), 2014.

[75] C. Wang, S. Chattopadhyay, and G. Brihadiswarn. Crash recoverable armv8-oriented b+-tree for byte-addressable persistent memory. In *ACM SIGPLAN/SIGBED International Conference on Languages, Compilers, and Tools for Embedded Systems*, pages 33–44, 2019.

[76] D. Yan, Y. Bu, Y. Tian, and A. Deshpande. Big graph analytics platforms. *Foundations and Trends in Databases*, 7, 2017.

[77] J. Yang and J. Leskovec. Defining and evaluating network communities based on ground-truth. *Knowledge and Information Systems*, 42(1):181–213, Jan 2015.

[78] M. Zarubin, P. Damme, T. Kissinger, D. Habich, W. Lehner, and T. Willhalm. Integer compression in nvrain-centric data stores: Comparative experimental analysis to dram. In *ACM International Workshop on Data Management on New Hardware*, page 11, 2019.

[79] K. Zhang, R. Chen, and H. Chen. Numa-aware graph-structured analytics. In *ACM Symposium on Principles and Practice of Parallel Programming (PPOPP)*, 2015.

[80] L. Zhang and S. Swanson. Pangolin: A fault-tolerant persistent memory programming library. In *USENIX Annual Technical Conference (USENIX ATC)*, 2019.

[81] Y. Zhang, M. Yang, R. Baghdadi, S. Kamil, J. Shun, and S. Amarasinghe. GraphIt: A high-performance graph DSL. *Proc. ACM Program. Lang.*, 2(OOPSLA):121:1–121:30, Oct. 2018.

[82] D. Zheng, D. Mhembere, R. Burns, J. Vogelstein, C. E. Priebe, and A. S. Szalay. Flashgraph: Processing billion-node graphs on an array of commodity ssds. In *USENIX Conference on File and Storage Technologies (FAST)*, 2015.

[83] D. Zheng, D. Mhembere, V. Lyzinski, J. T. Vogelstein, C. E. Priebe, and R. Burns. Semi-external memory sparse matrix multiplication for billion-node graphs. *IEEE Trans. Parallel Distrib. Syst.*, 28(5):1470–1483, May 2017.

[84] T. Zhou, P. Zardoshti, and M. Spear. Brief announcement: Optimizing persistent transactions. In *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 169–170, 2019.
[85] X. Zhu, W. Chen, W. Zheng, and X. Ma. Gemini: A computation-centric distributed graph processing system. In *USENIX Symposium on Operating Systems Design and Implementation (OSDI)*, pages 301–316, 2016.
A Model Details

In this section, we define the Parallel Semi-Asymmetric Model, which borrows ideas from the semi-external memory model [1, 61], the semi-streaming model [57, 32], the T-RAM model [30], and the asymmetric nested-parallel (ANP) model [7]. We believe that the new model captures the performance considerations in designing graph algorithms on the existing systems based on NVRAMs. Similarities and differences compared to the previous models will be discussed later in this section.

A.1 Parallel Semi-Asymmetric Model

The Parallel Semi-Asymmetric Model consists of an asymmetric large-memory with unbounded size that can hold the entire graph, and a symmetric small-memory with \( O(n) \) words of memory. In a relaxed version, we allow the small-memory size to store \( O(n + m / \log n) \) words. The Parallel Semi-Asymmetric Model has a set of threads that share both the large-memory and small-memory. Each thread acts like a sequential RAM plus a fork instruction that forks two new child threads. When a thread performs a fork, the two child threads all start by running the next instruction, and the original thread is suspended until all the children terminate. A computation starts with a single root thread and finishes when that root thread finishes. This model supports what is often referred to as nested-parallelism. This computational model is referred to as the T-RAM model or the binary-forking model. More details are discussed in [30].

We use the classic work-depth measure for the cost of algorithms on the Parallel Semi-Asymmetric Model. Similar to the ANP model, we assume unit cost for a read or write to the small-memory, and a read from the large-memory, both in the unit of a word. A write to the large-memory has a cost of \( \omega \), which is the cost of a write relative to a read. The overall work \( W \) of an algorithm is the cost for all memory accesses by all threads. The depth \( D \) is the longest sequence of dependent instructions in this computation. A work-stealing scheduler can execute such computation in \( W/p + O(D) \) time with high probability on a PRAM with \( p \) processors [7].

A.2 Comparison to Existing Models

T-RAM and Binary-Forking Model. The Parallel Semi-Asymmetric Model extends the memory in these models to two memories—the small-memory resembles DRAM and the large-memory resembles NVRAM.

Semi-External Memory Model. The semi-external memory model [1] is a variant of the external-memory model [2] where there is a small-memory that can hold the vertices but not the edges. Compared to the Parallel Semi-Asymmetric Model, the semi-external memory model does not account for the cost in accessing the small-memory (DRAM), while we believe that for existing systems with NVRAMs, this cost is not negligible. Second, the semi-external memory model has a parameter \( B \) for the unit of data movement. As opposed to external memories, NVRAMs support random access. We decided to not use the parameter \( B \) for ease of algorithm design and analysis.

Semi-Streaming Model. In the semi-streaming model [57], there is a memory size of \( O(n \cdot \text{polylog}(n)) \) bits and algorithms can only read over the graph in a sequential streaming order (with possibly multiple passes). In contrast, the Parallel Semi-Asymmetric Model allows random access to the input graph because NVRAMs intrinsically support random access. Furthermore the Parallel Semi-Asymmetric Model allows writes to the large-memory with a higher cost.

B Parallel primitives

The following parallel procedures are used in the remainder of the Appendix. Scan takes as input an array \( A \) of length \( n \), an associative binary operator \( \oplus \), and an identity element \( \bot \) such that \( \bot \oplus x = x \) for any \( x \), and returns the array \( (\bot, \bot \oplus A[0], \bot \oplus A[0] \oplus A[1], \ldots, \bot \oplus \oplus_{i=0}^{n-2} A[i]) \) as well as the overall sum, \( \bot \oplus \oplus_{i=0}^{n-1} A[i] \). Reduce takes an array \( A \) and a binary associative function \( f \) and
returns the sum of the elements in \( A \) with respect to \( f \). **Filter** takes an array \( A \) and a predicate \( f \) and returns a new array containing \( a \in A \) for which \( f(a) \) is true, in the same order as in \( A \). If done in small-memory, scan, reduce and filter can all be done in \( O(n) \) work and \( O(\log n) \) depth (assuming \( \oplus \) and \( f \) takes \( O(1) \) work) [11].

C Graph Filtering

In this section, we provide additional details on the algorithms used to implement graph filter primitives and their work-depth bounds in the PSAM. The algorithms use the parallel primitives defined in Section 3.

Graph Filter Algorithms. We now describe our algorithms implementing primitives over the graph filter structure, and analyze their costs. Our algorithms support both uncompressed graphs, and graphs compressed using the parallel encoding scheme from Ligra+ [67], and we describe any encoding-specific changes required in what follows.

**Creation.** To create a graph filter, the algorithm first computes the number of blocks that each vertex requires, based on \( \mathcal{F}_B \), and writes the space required per vertex into an array. Next, it scans the array, and allocates the required \( O(m) \) bits of memory contiguously. It then initializes the blocks per-vertex, in parallel, marking all edges as initially active (their corresponding bit is set to 1). Finally, it allocates an array of per-vertex words storing the initial degree, offset into the bitset structure corresponding to the start of the vertex’s blocks, and the number of blocks for that vertex. Lastly, it marks each of the \( n \) per-vertex dirty bits to false, as vertices are not initially marked dirty. The overall work of the procedure is \( O(m) \) and the overall depth is \( O(\log n + \mathcal{F}_B) \). If the user specifies that the initially supplied predicate returns false for some edges, the implementation calls **filterEdges** (described below), which runs within the same work and depth bounds.

**Packing.** Next, we describe the algorithm used to pack out the edges incident to a vertex given a predicate \( P \). The same algorithm is used to implement both **filterEdges** and **edgeMapPack**. The algorithm first maps over all blocks currently incident to the vertex in parallel. For each block, it finds all active bits in the block, reads the edge corresponding to the active bit and applies the predicate \( P \). The algorithm unsets the bit if and only if the predicate returns false. If the bit for an edge \((u, v)\) is unset, the algorithm marks the dirty bit for \( v \) to true. Note that for uncompressed graphs, the edge corresponding to an active bit can be directly read, whereas for a compressed graph, the entire block may have to be decoded to retrieve the value of a particular edge.

The algorithm also keeps track of how many bits are still active after processing the entire block, and stores these per-block counts in an array with size proportional to the number of blocks. Next, it performs a reduction over this array to compute the number of blocks with at least one active edge. For work-efficiency, if this value is less than a constant fraction of the current number of blocks for this vertex, the algorithm filters all blocks with no active elements, and packs the active blocks contiguously in the same memory. This operation is implemented by performing a parallel filter over the blocks. Next, the algorithm updates the offsets for all blocks by performing a parallel scan. Lastly, the algorithm updates the vertex degree and number of currently active blocks incident to the vertex. The overall work done is \( O(A \cdot (\mathcal{F}_B/\log n) + d_{\text{active}}(v)) \) and the depth is \( O(\log n + \mathcal{F}_B) \), where \( A \) is the number of non-empty blocks corresponding to \( v \) and \( d_{\text{active}}(v) \) is the number of active edges incident to vertex \( v \). Note that the framework does not expose this primitive directly to graph algorithms, since the number of edges in the graph is not updated.

**filterEdges.** The **filterEdges** primitive can be easily implemented using the algorithm for packing a vertex above by packing each vertex in parallel. The algorithm then returns the new degree of the graph by reducing all vertex degrees. By summing over all calls to the vertex packing primitive above, and accounting for the reduction over \( n \) vertices, the work is \( O(n + A \cdot (\mathcal{F}_B/\log n) + |E_{\text{active}}|) \),
and the depth is $O(\log n + F_B)$, where $A$ is the number of non-empty blocks in the graph and $E_{active}$ is the set of active edges represented by the graph filter.

**EDGEMAPPACK.** The EDGEMAPPACK primitive is implemented by packing each vertex in the vertexSubset in parallel. The overall work is the sum of the work for packing out each vertex in the vertexSubset, $S$, which is $O(A \cdot F_B / \log n + \sum_{v \in S}(1 + d_{active}(v)))$, and the depth is $O(\log n + F_B)$, where $A$ is the number of non-empty blocks corresponding to all $v \in S$.

**Vertex Primitives.** When calling vertex primitives on a graph filter, such as accessing the degree of the vertex, or mapping over its incident active edges, we first check whether the vertex is marked dirty. If so, we pack it out using the algorithm described above before performing the requested operation.

**Implementation and Optimizations.** Our routines were initially implemented by testing single bits at a time when decoding a block for its active edges. However, if a block is mostly empty, a large amount of CPU time is wasted checking bits that are set to 0. Instead, we use the Tzcnt and Blsr intrinsics that are provided on modern x86 CPU architectures to accelerate block processing. Since each block is logically divided into a number of machine words, we consider processing a single machine word. If the word is non-zero, we create a temporary copy of the word, and loop while this copy is non-zero. In each iteration, we use Tzcnt to find the index of the next lowest bit, and clear the lowest bit using the Blsr instruction. Doing so allows us to process a block with $q$ words and $k$ non-zero bits in $O(q + k)$ instructions.

We also implemented intersection primitives, which are used in our triangle counting algorithm based on the decoding implementation described above. For compressed graphs, since we may have to decode an entire block, we first decompress the entire block and store it locally in the iterator’s memory. We then process the graph filter’s bits word-by-word using the intrinsic-based algorithm described above.

Finally, we avoid the use of dirty bits in the algorithms using the graph filtering structure studied in this paper by supplying the framework’s primitives with a flag which informs the framework that the algorithm will not operate on vertices which are not packed. By avoiding using the dirty bits, our algorithms avoid an extra random-write of a neighbor’s dirty-bit when performing pack operations, an a random-read to check a dirty-bit when performing operations on vertices.

## D Memory-Efficient Parallel Graph Traversal

In this section, we review related work on graph traversals, and provide additional details on our memory-efficient parallel graph traversal algorithm. The algorithm description uses the parallel primitives defined in Section 3.

**Chunked Parallel Traversal.** We use a chunk-based method to optimize the memory-efficiency of the sparse (push-based) EDGEMAP. Our approach, which we refer to as EDGEMAPCHUNKED, shares some similarities, and achieves the same cache performance as the EDGEMAPBLOCKED implementation used in GBBS [30], but crucially it significantly improves the intermediate memory usage of the approach.

We provide pseudocode for our algorithm in Algorithm 1. The algorithm is based on two types of chunking. It first performs grouping of the outgoing edges to traverse. It also performs chunking of the output that is generated, writing out the neighbors that must be emitted in the next vertexSubset into fixed-size chunks. The algorithm first breaks each vertex up into units of work based on the filter block size of the underlying graph. This block size is equal to the compression block size for compressed graphs, and can be tuned arbitrarily for uncompressed graphs. We discuss how to set this block size in the next paragraph. Next, the algorithm decides the number of groups to create (Lines 14–19). It then processes the groups in parallel. For each group, it processes the blocks within the group one at a time. When starting the next block, it calls the FETCHCHUNK
procedure (Lines 4–10), which returns an output chunk for the current group, allocating a fresh chunk if the current chunk is too full (Line 23). Each group stores the chunks allocated for it in a per-group vector of output chunks, which can be accessed safely without any atomics, since each group is processed by a single thread. The chunk-allocations are done in our implementation using a pool-based thread-local allocator. Next, the algorithm processes the block and writes all neighbors that should be emitted in the next vertexSubset to the chunk, and update its block size. Note that FetchChunk procedure ensures that the returned chunk has sufficient space to store all neighbors in the block being processed. The remaining steps aggregate the chunks from the per-group vectors (Line 25), perform prefix sum on the chunk sizes (Line 26), and copy the data within the chunks into an array with size proportional to the number of returned neighbors (Lines 28–30). After copying the data within a chunk, the algorithm frees the chunk (Line 30). Finally, the algorithm returns the output vertexSubset (Line 31).

Memory-Usage, Work and Depth. First note that in the degenerate case where all edges are processed using our implementation, the code can create up to $m/G_{size}$ many blocks, which can be $\Omega(n)$. Instead, we ensure that $G_{size} = d_{avg} = \lceil m/n \rceil$, or the average degree. In this case, the maximum number of blocks used is $m/G_{size} = m/d_{avg} = O(n)$. It is simple to check the remainder of the code and observe that the amount of intermediate memory, and the output size is all bounded by $O(n)$ words. The overall small-memory usage of the procedure is therefore $O(n)$ words.

To ensure that we do not create an unnecessarily large number of groups, we set the number of groups to $O(\min(8p, \sum_{u \in U} \deg(u)/4096))$ on $p$ processors (Lines 15–17). These parameters balance between providing enough parallel slackness for work-stealing when there is a large amount of work to be done (the $8p$ term in the min) while also ensuring that we do not over-provision parallelism in the case when the number of edges incident to the frontier is small (the second term).

The overall work of the procedure is $O(\sum_{u \in U} \deg(u))$ work, and the overall depth is $O(\log n + d_{avg})$, since each block is processed sequentially, and each call to the procedure requires aggregating the per-group chunks which can be done in parallel. The work done for the chunk-aggregation is proportional to the number groups (and number of output chunks), both of which are upper-bounded by $O(\sum_{u \in U} \deg(u))$. Since $d_{avg}$ is usually a small constant in real-world graphs (see Table 2), practically speaking, its contribution to the depth can be ignored in practice.

E Semi-Asymmetric Bucketing

We now briefly describe how to adapt the work-efficient bucketing structure from Julienne [29] to the PSAM. A bucketing structure maintains a dynamic mapping between a set of elements and buckets, and is used in several important graph algorithms for work-efficiency: weighted breadth-first search, $k$-core, approximate densest subgraph, and approximate set cover. The bucketing strategy in Julienne is based on lazy bucketing, which avoids deleting the bucketed elements from buckets they are moved out-of. If the elements that are bucketed are the vertices, and the total number of bucket updates is $O(m)$, the use of lazy bucketing will require the bucket structure to use $O(m)$ words of space, violating the model requirements.

We can address this issue by using semi-eager bucketing. In the semi-eager version, each bucket contains two counters, storing the number of live elements currently in the bucket, and the number of dead elements. When moving a vertex out of a bucket, we increment the dead-element count in that bucket. When a bucket contains more than a constant factor of dead elements, we pack it out. Since each vertex is contained in a single bucket, it is easy to check that this scheme only uses $O(n)$ words of memory.

In practice, we use the practical variant of the bucketing structure proposed in Julienne [29], which is based on maintaining some number of active buckets, and an overflow bucket. By ensuring that the number of active buckets is a small constant, we only use $O(n)$ words of memory.
**Algorithm 1 edgeMapChunked**

1: chunk\_size = max(4096, d\_avg)
2: min\_group\_size = 4096
3: chunk\_alloc := Initialize thread-local allocator with chunk\_size
4: procedure FetchChunk(b\_size, V)
5:    chunk := Last chunk from V
6:    \triangleright V : vector of output chunks for this group
7:    if chunk = null or chunk\_size + b\_size > chunk\_size then
8:        chunk := chunk\_alloc\_allocate()
9:        Insert chunk into V
10:        return chunk
11: procedure edgeMapChunked(G, U, F)
12:    G\_b\_size := d\_avg \triangleright underlying block size used in G
13:    B := Output blocks corresponding to u \in U
14:    O := Prefix sums of block-degrees for blocks in B
15:    d\_U := \sum_{u \in U} deg(u)
16:    group\_size := max([d\_U/8p], min\_group\_size)
17:    num\_groups := [d\_U/group\_size]
18:    idxs := \{i \cdot group\_size | i \in [num\_groups]\}
19:    Offs := Offsets into O resulting from a parallel merge of idxs and O
20:    V := Array of vectors storing chunks of size num\_groups
21:    \textbf{parfor} i \in [\|Offs\|] \triangleright In parallel over the groups
22:        \textbf{for} j in [Offs[i], Offs[i + 1]] \triangleright \leq G\_b\_size edges in block j
23:            chunk := FetchChunk(G\_b\_size, V,)
24:            Process block j, and write live neighbors into chunk
25:    C := All chunks extracted from V
26:    output\_size := Prefix sum chunk sizes from C
27:    output := Array of size output\_size
28:    \textbf{parfor} c \in C \textbf{do}
29:        Copy elements in c to offset in output corresponding to c
30:        chunk\_alloc\_release(c)
31:    return output

**F Algorithm Specification and Analysis**

**F.1 Shortest Path Problems**

**Breadth-First Search (BFS)**

Input: G = (V, E), an unweighted graph, src \in V.
Output: D, a mapping where D[v] is the shortest path distance from src to v in G and \infty if v is unreachable.

**Integral-Weight SSSP (Weighted BFS)**

Input: G = (V, E, w), a weighted graph with integral edge weights, src \in V.
Output: D, a mapping where D[v] is the shortest path distance from src to v in G and \infty if v is unreachable.
General-Weight SSSP (Bellman-Ford)

Input: $G = (V, E, w)$, a weighted graph, $src \in V$.
Output: $D$, a mapping where $D[v]$ is the shortest path distance from $src$ to $v$ in $G$ and $\infty$ if $v$ is unreachable. All distances must be $-\infty$ if $G$ contains a negative-weight cycle reachable from $src$.

Single-Source Betweenness Centrality (BC)

Input: $G = (V, E)$, an undirected graph, $src \in V$.
Output: $S$, a mapping from each vertex $v$ to the centrality contribution from all $(src, t)$ shortest paths that pass through $v$.

Single-Source Widest Path

Input: $G = (V, E, w)$, a weighted graph with integral edge weights, $src \in V$.
Output: $D$, a mapping where $D[v]$ is the maximum over all paths between $src$ and $v$ in $G$ of the minimum weight on the path and $\infty$ if $v$ is unreachable.

$O(k)$-Spanner

Input: $G = (V, E)$, an undirected, unweighted graph, and an integer stretch factor, $k$.
Output: $H \subseteq E$, a set of edges such that for every $u, v \in V$ connected in $G$, $dist_H(u, v) \leq O(k)$.

We consider six shortest-path problems in this paper: breadth-first search (BFS), integral-weight SSSP (wBFS), general-weight SSSP (Bellman-Ford), single-source betweenness centrality, single-source widest path, and $O(k)$-spanner. Our implementations of BFS, Bellman-Ford, and betweenness centrality are based on the implementations in Ligra [65], and our wBFS implementation is based on our earlier work on Julienne [29]. We provide two implementations of the single-source widest path algorithm, one based on Bellman-Ford, and another based on the wBFS implementation from Julienne [29]. We obtain semi-asymmetric algorithms for the first five these problems by using EDGE_MAP_CHUNKED (Section 4.2) for performing sparse graph traversals.

Our $O(k)$-spanner implementation is based on a recently described spanner algorithm due to Miller et al. [55]. A $O(k)$-spanner is a subgraph that preserves shortest path distances within a factor of $O(k)$. Their construction computes an $O(k)$-spanner with size $O(n^{1+1/k})$, and runs in $O(m)$ expected work and $O(k \log n)$ depth whp. The implementation uses our low-diameter decomposition algorithm, which we describe below. In our experiments, we set $k$ to be $\Theta(\log n)$, and finds a spanner which has $O(n)$ size.

F.2 Connectivity Problems

Low-Diameter Decomposition (LDD)

Input: $G = (V, E)$, a directed graph, $0 < \beta < 1$.
Output: $\mathcal{L}$, a mapping from each vertex to a cluster ID representing a $(O(\beta), O((\log n)/\beta))$ decomposition. A $(\beta, d)$-decomposition partitions $V$ into $V_1, \ldots, V_k$ such that the shortest path between two vertices in $V_i$ using only vertices in $V_i$ is at most $d$, and the number of edges $(u, v)$ where $u \in V_i, v \in V_j, j \neq i$ is at most $\beta m$. 
Connectivity
Input: $G = (V, E)$, an undirected graph.
Output: $L$, a mapping from each vertex to a unique label for its connected component.

Spanning Forest
Input: $G = (V, E)$, an undirected graph.
Output: $T$, a set of edges representing a spanning forest of $G$.

Biconnectivity
Input: $G = (V, E)$, an undirected graph.
Output: $L$, a mapping from each edge to the label of its biconnected component.

We consider four connectivity problems in this paper: low-diameter decomposition (LDD), connectivity, spanning forest, and biconnectivity. Our implementations in this paper are extensions of the implementations provided in GBBS [30]. First, we replace the calls to EDGE_MAP_BLOCKED with calls to EDGE_MAP_CHUNKED within the framework, which ensures that the graph traversal step uses $O(n)$ words of small-memory. This modification alone results in PSAM algorithms for LDD. For connectivity, to ensure theoretical efficiency we must set the $\beta$ parameter, which controls the number of edges cut by the LDD step correctly to ensure that the contracted graph contains $O(n)$ edges in expectation. Specifically, we set $\beta = 1/d_{\text{avg}}$, where $d_{\text{avg}} = \lceil m/n \rceil$, which ensures that the number of cut edges is $m\beta = O(n)$ in expectation. We make this modification for spanning forest and biconnectivity as well, since they either use LDDs, or call connectivity as a sub-routine in a similar fashion. Finally, our biconnectivity implementation uses the graph filtering structure to optimize a call to connectivity which runs on the input graph, with a large subset of the edges removed. Our algorithms for connectivity, spanning forest, biconnectivity, and $O(k)$-spanner use $O(n)$ words of small-memory in expectation but we can obtain the same space bound in the worst case without affecting the work and depth, which we describe in Appendix G.

F.3 Covering Problems

Maximal Independent Set (MIS)
Input: $G = (V, E)$, an undirected graph.
Output: $U \subseteq V$, a set of vertices such that no two vertices in $U$ are neighbors and all vertices in $V \setminus U$ have a neighbor in $U$.

Maximal Matching
Input: $G = (V, E)$, an undirected graph.
Output: $E' \subseteq E$, a set of edges such that no two edges in $E'$ share an endpoint and all edges in $E \setminus E'$ share an endpoint with some edge in $E'$.
Graph Coloring

Input: $G = (V, E)$, an undirected graph.
Output: $C$, a mapping from each vertex to a color such that for each edge $(u, v) \in E$, $C(u) \neq C(v)$, using at most $\Delta + 1$ colors.

Approximate Set Cover

Input: $G = (V, E)$, an undirected graph representing a set cover instance.
Output: $S \subseteq V$, a set of sets such that $\bigcup_{s \in S} N(s) = V$ with $|S|$ being an $O(\log n)$-approximation to the optimal cover.

We consider four covering problems in this paper: maximal independent set (MIS), maximal matching, graph coloring, and approximate set cover. Our implementations are extensions of the implementations described in [30]. First, for MIS and graph coloring, we derive PSAM algorithms by applying our EDGE\textsc{MapChunked} optimization since other than graph traversals, both algorithms already use $O(n)$ words of small-memory. Both maximal matching and approximate set cover require using our graph filtering technique to achieve immutability and reduced memory usage without affecting the theoretical bounds of the algorithms.

Our maximal matching algorithm runs iterations of the filtering-based maximal matching algorithm described in [30] on subsets of the edges such that they fit in small-memory. The algorithm has access to $O(n + m/\log n)$ words of memory, so we can solve the problem by extracting the next $O(m/\log n)$ unprocessed edges on each iteration, and running the random-priority based maximal matching algorithm on the subset of edges. By performing this step $O(\log n)$ times the algorithm will finish. This does not affect the overall work and increases the depth by an $O(\log n)$ factor. In practice, we use a similar approach that is theoretically motivated and makes use of our graph-filtering structure. In each step we extract $O(n)$ unmatched edges, and process them using the random-priority based algorithm. All unmatched edges from this set are discarded, and the graph is filtered using \textsc{filterEdges} to pack out edges incident to matched vertices. Theoretically, we can switch to the previously described version after a constant number of such steps. However, we observed that in practice, a constant number of iterations of the filtering procedure suffices for all graphs we tested on.

Our approximate set cover implementation is similar to the implementation from [30], with the exception that the underlying filtering is done using a graph filter, instead of mutating the original graph. The bounds obtained for the graph filter structure match the bounds on filtering used in the GBBS code which mutates the underlying graph, and so our implementation also computes a $(1 + \epsilon)$-approximate set cover in $O(m)$ expected work and $O(\log^3 n)$ depth whp.

F.4 Substructure Problems

$k$-core

Input: $G = (V, E)$, an undirected graph.
Output: $D$, a mapping from each vertex to its coreness value.
Approximate Densest Subgraph

Input: \( G = (V,E) \), an undirected graph, and a parameter \( \epsilon \).
Output: \( U \subseteq V \), a set of vertices such that the density of \( G_U \) is a \( 2(1 + \epsilon) \) approximation of density of the densest subgraph of \( G \).

Definition: Given an undirected graph \( G = (V,E) \), the density of a set \( S \subseteq V \) is defined as \( \rho(S) = \frac{|E(S)|}{|S|} \), where \( E(S) \) are the edges in the induced subgraph on \( S \).

Triangle Counting

Input: \( G = (V,E) \), an undirected graph.
Output: \( T_G \), the total number of triangles in \( G \).

We consider three substructure-based problems in this paper: \( k \)-core, approximate densest subgraph and triangle counting. Our \( k \)-core implementation is similar to the implementation from GBBS [30]. We note that for the algorithm to use \( O(n) \) words of small-memory, it should use the fetch-and-add based implementation of \( k \)-core, which avoids the use of a contention-avoiding histogram procedure and performs atomic accumulation in an array instead to update the degrees. However, as shown in [30], the fetch-and-add based implementation has poor performance on real-world graphs, where it incurs high contention to update the degrees of vertices incident to many removed vertices. In practice, therefore, we use the histogram-based version of the code which always runs faster than the fetch-and-add based implementation. We implemented a dense version of the histogram routine, which performs reads for all vertices in the case where the number of neighbors of the current frontier is higher than a threshold, \( t \). The work of the dense version is \( O(m) \). By setting the threshold to be \( m/c \) for some constant \( c \), the work of the implementation is still \( O(m) \), and we found that the memory used is \( O(n) \) words in practice.

Our approximate densest subgraph algorithm is similar to our \( k \)-core algorithm, and uses a histogram to accelerate processing the removal of vertices. The code also uses the dense histogram algorithm described above.

Finally, our triangle counting code is based on the GBBS implementation, which is an implementation of the parallel triangle counting algorithm from Shun and Tangwongsan [68]. Our implementation in this paper uses the graph filter structure to orient edges in the graph from lower degree to higher degree. Since we only require outgoing edges, we supply a flag to the framework which permits it to only represent the outgoing edges of the directed graph, halving the amount of internal memory required. The code uses the new iterator implemented over the graph filter structure to perform intersections between the outgoing edges of two vertices. We note that in our current implementation, we perform intersection sequentially which theoretically guarantees a depth of \( O(\sqrt{m}) \). However, the parallelism of this algorithm is \( O(m^{3/2}/m^{1/2}) = O(m) \) which in practice is sufficiently high that reducing the depth using a parallel intersection routine is unnecessary, and can hurt performance due to using a more complicated intersection algorithm.

F.5 PageRank

PageRank

Input: \( G = (V,E) \), an undirected graph.
Output: \( \mathcal{P} \), a mapping from each vertex to its PageRank value after a single iteration of PageRank.

We consider the PageRank algorithm, designed to rank the importance of vertices in a graph [18]. Our PageRank implementation is based on the implementation from Ligra, which we optimized to
improve the depth of the algorithm. The implementation from Ligra runs dense iterations, where the aggregation step for each vertex (reading its neighbor’s PageRank contributions) is done sequentially. We implemented a reduction-based method which reduces over these neighbors using a parallel reduce. Therefore, each iteration of our implementation requires $O(m)$ work and $O(\log n)$ depth. The overall work is $O(P_{it} \cdot m)$ and depth is $O(P_{it} \log n)$, where $P_{it}$ is the number of iterations required to run PageRank to convergence with a convergence threshold of $\epsilon = 10^{-6}$.

G Additional Algorithm Details

We now provide additional details about our algorithms that did not fit in the main body of the paper.

Handling Restarts in Low-Diameter Decomposition-Based Algorithms. One issue that arises when running in the PSAM is that algorithms which run in $O(n)$ words of space in expectation may need to be restarted if the space bound is violated. This situation can occur for several of our algorithms which are based on running a low-diameter decomposition, and contracting, or selecting inter-cluster edges based on the decomposition. In what follows, we focus on the connectivity algorithm, since our spanning forest, biconnectivity, and $O(k)$-spanner algorithm are also handled identically.

In our connectivity algorithm, we can ensure that the algorithm runs in $O(n)$ words of space by re-running the LDD algorithm until it succeeds. Checking whether an LDD succeeds can be done in $O(n)$ space and $O(n+m)$ work by simply counting the number of inter-cluster edges formed by the partition of vertices. Once the LDD succeeds, the rest of the algorithm does not require restarts, since the recursive calls in the connectivity algorithm always fit within $O(n)$ words of space [66].

We note that since the LDD succeeds with constant probability, an expected constant number of iterations are needed for the connectivity algorithm to succeed. We also note that the work bounds obtained using restarting are still $O(m)$ in expectation. Furthermore, the depth bounds of our LDD-based algorithms is not affected by restarts because we only need to perform restarts at the first level of recursion in the algorithm. Since we must perform at most $O(\log n)$ restarts at this level to guarantee success whp, the overall contribution to the depth of re-running an LDD at this step is $O(\log^2 n)$ whp, which is subsumed by the algorithm’s overall depth.

H Experiments

H.1 Configuration Details of our NVRAM Configuration. When first experimenting with these devices, we observed that the performance of cross-socket reads to graph data that is stored on NVRAM was extremely poor, and that many of our applications experienced a significant slowdown when moving from threads allocated within the same socket as where the data is stored, to threads allocated across both sockets. We designed a simple micro-benchmark which illustrates this phenomena. The benchmark runs over all vertices in parallel. For the $i$’th vertex, it sums the number of neighbors incident to it by scanning all of the incident edges and writes this value to to an array location corresponding to the $i$’th vertex. The graph is stored in CSR format, and so the benchmark reads each offset exactly once, and reads the edges incident to each vertex exactly once. The total bytes read is therefore proportional to the size of the graph in bytes, and the number of writes is proportional to the number of vertices. For the ClueWeb graph, we observed that running the benchmark on the same socket that the data is allocated from results in a running time of 7.1 seconds. However, using `numactl -i all`, and running the benchmark across both sockets results in a running time of 26.7 seconds, which is 3.7x worse, despite using twice as many hyper-threads. While we are not certain as to the underlying reason for this slowdown, we suspect that it to be due to the granularity size for the current generation of NVRAM DIMMs, which have a larger effective
Table 8: Tradeoff between $F_B$, the graph filter block size, the number of directed wedges that must be checked for this graph (Intersection Work), the total amount of work performed decoding edges within blocks in triangle counting (Total Work), and the running time of triangle counting for the ClueWeb graph. The second half of the table reports the same statistics for the Hyperlink2014 and Hyperlink2012 graphs for the configurations in which the running times in Table 6 were run.

| Graph     | Block Size | Intersection Work | Total Work   | Time (s) |
|-----------|------------|-------------------|--------------|----------|
| ClueWeb   | 64         | $2.24 \times 10^{10}$ | $7.16 \times 10^{10}$ | 489      |
| ClueWeb   | 128        | $2.24 \times 10^{10}$ | $9.54 \times 10^{10}$ | 567      |
| ClueWeb   | 256        | $2.24 \times 10^{10}$ | $12.8 \times 10^{10}$ | 683      |
| Hyperlink2014 | 64         | $4.8 \times 10^{12}$ | $101 \times 10^{12}$ | 5722     |
| Hyperlink2012 | 64         | $10.4 \times 10^{12}$ | $67.2 \times 10^{12}$ | 3529     |

As described in Section 5, the approach used in this paper is to store two separate copies of the graph, one on the local NVRAM of each socket. Threads can determine which socket they are running on by reading a thread-local variable. Furthermore, we pin threads to sockets by using `set_affinity` to bind them to a particular virtual core. Using this new configuration, our running times for the micro-benchmark becomes 4.3s using all 96 hyper-threads, which is 1.6x faster than the single-socket experiment and 6.2x faster than using threads across both sockets to access graph data stored locally within a single socket.

H.2 Techniques

Graph Filtering and Triangle Counting. Next, we consider the effect that the underlying block size used in the graph filter has on the performance of the triangle counting implementation in this paper. Recall that for our compressed inputs, extracting a given edge from a block requires possibly (sequentially) decompressing the full block to retrieve the desired edge. We refer to the work done to decompress edges within the decoded blocks as the total work done by our triangle counting implementation. We also that this measure is a function of both the block size used in the graph filter, as well as the underlying graph ordering. We refer to the work that has to be done to perform all directed intersections as the intersection work done by the triangle counting implementation, not including decoding blocks. Note that the intersection work for a graph is a fixed quantity for a given total ordering of the vertices. The intersection work is a lower bound on the total amount of work that has to be done, but the total amount of work can be much larger if the blocks containing active edges (edges in the directed graph) are very sparse.

Table 8 reports numbers displaying this tradeoff between $F_B$, the graph filter block size, total amount of work required to decode all edges within blocks, and the running time of the implementation. We observe that using a smaller $F_B$ results in a more work-efficient implementation, which directly translates to a faster running time.

Finally, Table 8 also reports the block sizes, intersection work and total work required to run triangle counting on the Hyperlink2014 and Hyperlink2012 graph with $F_B = 64$. Recall that the intersection work is a lower bound on the total amount of work that is done, and that the total work is the amount of decoding operations actually performed by our implementation. We note that triangle counting on the Hyperlink2014 graph incurs a much larger penalty in terms of total work than Hyperlink2012 (1.5x larger). The running time of code on the Hyperlink2014 graph is also 1.6x larger than the time for the code on Hyperlink2012, which validates the hypothesis that the total work is largely responsible for the running time of the triangle counting intersection.
| Graph         | Algorithm             | DRAM Usage | Time (s) |
|--------------|-----------------------|------------|----------|
| ClueWeb      | EDGE_MAP_SPARSE       | 33.0GB     | 2.52     |
| ClueWeb      | EDGE_MAP_BLOCKED      | 28.2GB     | 2.43     |
| ClueWeb      | EDGE_MAP_CHUNKED      | 26.6GB     | 2.35     |
| Hyperlink2014| EDGE_MAP_SPARSE       | 54.0GB     | 5.61     |
| Hyperlink2014| EDGE_MAP_BLOCKED      | 42.7GB     | 5.20     |
| Hyperlink2014| EDGE_MAP_CHUNKED      | 42.3GB     | 5.10     |
| Hyperlink2012| EDGE_MAP_SPARSE       | 115GB      | 12.5     |
| Hyperlink2012| EDGE_MAP_BLOCKED      | 90.3GB     | 12.3     |
| Hyperlink2012| EDGE_MAP_CHUNKED      | 87.5GB     | 12.2     |

Table 9: Effect of the sparse traversal algorithm (EDGE_MAP_SPARSE, EDGE_MAP_BLOCKED, and EDGE_MAP_CHUNKED) on the total DRAM usage and the running time of our BFS implementation.

**Memory usage of edgeMapChunked.** Next, we study the memory improvements in terms of total memory used by the program due to the edgeMapChunked optimization. We report both the total memory used, and the running times for running BFS from a given source vertex within the massive connected components for the ClueWeb and Hyperlink2012 graphs. We compare our implementation to the BFS implementation from GBBS, which uses the edgeMapBlocked algorithm, which allocates an intermediate array with size proportional to the number of out-neighbors of a frontier. Both implementations use the same source vertex.

Table 9 shows the results of the experiments. We observe that our new chunk-based implementation requires roughly the same order of magnitude of memory as the previous edgeMapBlocked implementation, and also results in similar running times. Both edgeMapBlocked and edgeMapChunked use significantly less memory than using edgeMapSparse. Specifically, edgeMapChunked uses 1.24x less memory than edgeMapSparse on ClueWeb, 1.27x less memory on Hyperlink2014, and 1.31x less memory on Hyperlink2012. The memory usage between edgeMapChunked and edgeMapBlocked is likely similar since edgeMapBlocked only performs DRAM writes proportional to the output size of edgeMap, which is the same number of writes (and therefore physical pages) as performed by edgeMapChunked.

In addition, using our edgeMapChunked implementation we can run a “sparse-only” edgeMap with limited memory. Although running only the sparse version of a breadth-first search is not particularly practical, it is useful for understanding the performance improvement gained by using Beamer’s direction-optimization on very large real-world graphs. Trying to run a similar sparse-only using either edgeMapSparse or edgeMapBlocked segmentation faults due to malloc on the Hyperlink2012 graph when the graph tries to allocate an 492GB array from DRAM, which is larger than the DRAM size of our machine. The edgeMapChunked-based implementation runs in 38.8s and has a peak-memory usage of 120GB of memory, which is less than 1/3 of our machine’s memory DRAM capacity. Our implementation allows us to see that using direction-optimization results in a 3.1x speedup over running the sparse-only code for this graph.