2D Discrete Fourier Transform with Simultaneous Edge Artifact Removal for Real-Time Applications

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Abstract—Two-Dimensional (2D) Discrete Fourier Transform (DFT) is a basic and computationally intensive algorithm, with a vast variety of applications. 2D images are, in general, non-periodic, but are assumed to be periodic while calculating their DFTs. This leads to cross-shaped artifacts in the frequency domain due to spectral leakage. These artifacts can have critical consequences if the DFTs are being used for further processing. In this paper we present a novel FPGA-based design to calculate high-throughput 2D DFTs with simultaneous edge artifact removal. Standard approaches for removing these artifacts using apodization functions or mirroring, either involve removing critical frequencies or a surge in computation by increasing image size. We use a periodic-plus-smooth decomposition based artifact removal algorithm optimized for FPGA implementation, while still achieving real-time (≥23 frames per second) performance for a 512×512 size image stream. Our optimization approach leads to a significant decrease in external memory utilization thereby avoiding memory conflicts and simplifies the design. We have tested our design on a PXIe based Xilinx Kintex 7 FPGA system communicating with a host PC which gives us the advantage to further expand the design for industrial applications.

Keywords—2D FFT, Discrete Fourier Transform, Fast Fourier Transform, Edge Artifact Removal, FPGA, High-level synthesis, Boundary Effect

I. INTRODUCTION

Discrete Fourier Transform (DFT) is a commonly used and vitally important function for a vast variety of applications including, but not limited to digital communication systems, image processing, and biomedical imaging. Fourier image analysis simplifies computations by converting complex convolution operations in the spatial domain to simple multiplications in the frequency domain. Due to their computational complexity, DFTs often become a computational constraint for applications requiring high throughput and near real-time operations. The Cooley-Tukey Fast Fourier Transform (FFT) algorithm [1], first proposed in 1965, reduces the complexity of DFTs from \(O(N^2)\) to \(O(N\log N)\) for a 1D DFT. However, in the case of 2D DFTs, 1D FFTs have to be computed in two-dimensions, increasing the complexity to \(O(N^2\log N)\), thereby making 2D DFTs a significant bottleneck for real-time machine vision applications [2].

There are several resource-efficient, high-throughput implementations of 2D DFTs. Most FPGA based 2D FFT implementations rely upon repeated invocations of 1D FFTs by row and column decomposition (RCD) with efficient use of external memory [2][3][4]. Many of these achieve real-time or near real-time performance (≥23 frames per second for a standard 512×512 image).

While calculating 2D DFTs it is assumed that the image is periodic, which is usually not the case. The non-periodic nature of the image leads to artifacts in the Fourier transform, usually known as edge artifacts or series termination errors. These artifacts appear as several crosses of high-amplitude coefficients in the frequency domain, as seen in [6]. Such edge artifacts can be passed to subsequent stages of processing and in biomedical applications they may lead to critical misinterpretations of results. No current 2D FFT FPGA implementation addresses this problem directly. These artifacts may be removed during pre-processing, using mirroring, windowing, zero padding or post-processing, e.g., filtering techniques; however, these techniques are usually computationally intensive and often tend to modify the transform. The most common approach is by ramping the image at corner pixels to slowly attenuate the edges. Ramping is usually accomplished by an apodization function such as a Tukey (tapered cosine) or a Hamming window, which smoothly reduces the intensity to zero. Such an approach can be implemented on an FPGA as a pre-processing operation by storing the window function in a Look-up Table (LUT) and multiplying it with the image stream before calculating the FFT [5]. Although, this approach is not extremely computationally intensive for small images, it inadvertently removes necessary information from the image. Loss of this information may have serious consequences if the image is being further processed with several other images to reconstruct a final image that is used for diagnostics or other decision-critical applications. Another common method is by mirroring the image from \(N \times N\) to \(2N \times 2N\). Doing so makes the image periodic, thereby removing edge artifacts. However, this not only increases the size of the image by 4x, but also makes the transform symmetric, which generates an inaccurate phase component.

Most RCD-based 2D FFT FPGA implementations have two major design challenges: 1) The 1D FFT implementation needs to have a reasonably high-throughput and needs to be resource efficient. 2) External DRAM needs to be efficiently addressed and have a high-bandwidth because images are usually large and intermediate storage is required between row and column 1D FFT operations.

Periodic plus smooth decomposition (PSD) [6], described in section II, provides an efficient solution for edge artifact removal from 2D DFTs with minimal amputation of useful information from the image. In section III, we describe an optimization of PSD for FPGA implementation, which reduces the number of 1D FFT invocations and requires less frequent access to external DRAM. In section IV we further describe the hardware set-up and propose an architecture for optimized...
and therefore, \( V \) has the same structure as \( W \) but is \( m \)-dimensional. Since \( w^k \) has period \( n \) which means that \( w^k = w^{k+n} \), \( \forall k, l \in \mathbb{N} \) and therefore,

\[
W = \begin{pmatrix}
1 & 1 & 1 & \ldots & 1 \\
1 & w & w^2 & \ldots & w^{n-1} \\
1 & w^2 & w^4 & \ldots & w^{2(n-1)} \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
1 & w^{n-2} & w^{n-4} & \ldots & w^{2(n-1)} \\
1 & w^{n-1} & w^{n-2} & \ldots & w^1
\end{pmatrix}
\quad \text{(2)}
\]

Since in general \( I \) is not \( (n,m) \)-periodic, there will be high amplitude edge artifacts present in the DFT stemming from sharp discontinuities between the opposing edges of the image as shown in figure 1b. Moisan [6] proposed a decomposition of \( I \) into a periodic component \( P \), that is periodic and captures the essence of the image with all high frequency details, and a smoothly varying background \( S \), that recreates the discontinuities at the borders. So, \( I = P + S \). Periodic plus smooth decomposition can be computed by first constructing a border image \( B = R + C \), where \( R \) represents the boundary discontinuities when transitioning row-wise and \( C \) when going column-wise

\[
R(i,j) = \begin{cases} 
I(n-1-i,j) - I(i,j), & i = 0 \text{ or } i = n-1 \\
0, & \text{otherwise}
\end{cases}
\]

\[
C(i,j) = \begin{cases} 
I(i,m-1-j) - I(i,j), & j = 0 \text{ or } j = m-1 \\
0, & \text{otherwise}
\end{cases}
\]

\quad \text{(5)}

It is obvious that the structure of the border image \( B \) is simple with nonzero values only in the edges as shown below:

\[
B = R + C = \begin{pmatrix}
b_{11} & b_{12} & \ldots & b_{1,m-1} & b_{1m} \\
b_{21} & 0 & \ldots & 0 & -b_{21} \\
\vdots & \vdots & \ddots & \vdots & \vdots \\
b_{n-1,1} & 0 & \ldots & 0 & -b_{n-1,1} \\
b_{n1} & -b_{12} & \ldots & -b_{1,m-1} - b_{nm}
\end{pmatrix}
\quad \text{(6)}
\]

The DFT of the smooth component \( S \) can be then found by the following formula:

\[
\hat{S}(s,t) = \frac{\hat{B}(s,t)}{2 \cos \frac{2 \pi s}{n} + 2 \cos \frac{2 \pi t}{m} - 4}, \quad \forall (s,t) \in \Omega \setminus \{(0,0)\}
\quad \text{(7)}
\]

The DFT of the image \( I \) with edge artifacts removed is then \( \hat{P} = \hat{I} - \hat{S} \). Figures 1c and 1d show the DFT of the smooth and periodic components, respectively.

III. PSD OPTIMIZATION FOR FPGA IMPLEMENTATION

In this section we optimize the original PSD algorithm so that it can be effectively configured on an FPGA. This is accomplished by using inherent symmetry between rows and columns to reduce the number of 1D FFT invocations and minimize utilization of external DRAM. On inspecting equation (6) we realize that the boundary image \( B \) is symmetrical in the sense that boundary rows and columns are an algebraic negation of each other. An FFT of a column vector \( v \) with length \( n \) is \( \mathbf{W}v \), where \( \mathbf{W} \) is given in eq. (4). The column-wise FFT of the matrix \( B \) is then

\[
\hat{B} = \mathbf{W}B.
\quad \text{(8)}
\]
It can be shown that the 1D FFT of the column \( j \in \{2, 3, \ldots, m - 1\} \) is

\[
\hat{B}_j = WB_j = b_{1j} \begin{pmatrix} 1 - w^{n-1} \\ 1 - w^{n-2} \\ \vdots \\ 1 - w^2 \\ 1 - w \end{pmatrix} = b_{1j} \nu, \tag{9}
\]

The 1D FFT of the last column \( B_{m} \) is

\[
\hat{B}_m = WB_m \tag{10}
\]

\[
\hat{B}_m = -\hat{B}_1 + (b_{11} + b_{1m}) \nu. \tag{11}
\]

So, the column-wise FFT of the matrix \( B \) is

\[
\hat{B} = (\hat{B}_j)_{j=1}^{m} = b_{12} \nu \ldots b_{1,m-1} \nu - \hat{B}_1 + (b_{11} + b_{1m}) \nu. \tag{12}
\]

To compute the column-by-column 1D FFT of the matrix, \( B \), we only have to compute the FFT of the first vector and then use the appropriately scaled vector, \( \nu \), to derive the remainder of the columns. The row-by-row FFT has to be calculated normally. By reducing column-by-column 1D FFT computations for the boundary image, this method can significantly reduce the number of 1D FFT invocations and reduce DRAM access for an FPGA-based implementation. This can be implemented by temporarily storing the initial vector \( \hat{B}_1 \) and scaling factors \( b_{1j} \) in the block RAM/register memory, drastically reducing DRAM access and lowering the number of required 1D FFT invocations.

For a \( N \times M \) image, this can reduce DRAM access from \( 4NM \) points to \( 3NM + N + M - 1 \) points and can reduce the number of 1D FFT invocations from to 1 column vector rather than \( M \) column vectors while calculating the column-by-column component of the 2D FFT. In other words, the number of DFT points to be computed can be reduced from \( 4NM \) to \( 3NM + M \). Table I shows a comparison of Mirroring, PSD and our proposed Optimized PSD (OPSD) with respect to DRAM access points and DFT points. Figure 2 graphically shows that our optimized PSD method can significantly reduce reading from external memory and can reduce the overall number of DFT computations required.

| Algorithm                  | DRAM Access | DFT Points |
|----------------------------|-------------|------------|
| Mirroring                  | 8NM         | 8NM        |
| P+S Decomposition (PSD)    | 4NM         | 4NM        |
| Optimized PSD (Proposed)   | 3NM + N + M - 1 | 3NM + M    |

Fig. 3. Block diagram of a PXIe based multi-FPGA system with a host PC controller connected through a high-speed bus on a PXIe chassis.

IV. FPGA IMPLEMENTATION OF OPTIMIZED PSD

A. Hardware Configuration

Since 2D DFTs are usually used for simplifying convolution operations in complex image processing and machine vision systems we needed to prototype our design on a system that is expandable for next levels of processing. For rapid-prototyping of our proposed optimized periodic-plus-smooth decomposition algorithm we used a PXIe (PCI eXtensions for Industry express)-based reconfigurable system. PXIe is an industrial extension of a PCI system with an enhanced bus structure that gives each connected device dedicated access to the bus with a maximum throughput of 4 GB/s. This allows a high-speed dedicated link between a host PC and several FPGAs. We used a National Instruments FlexRIO (Flexible Reconfigurable I/O) PXIe-7976R FPGA board plugged into a PXIe chassis. PXIe-7976R is equipped with a Kintex 7 FPGA and 2 GB external DRAM with data bandwidth upto 10.5 GB/s. PXIe FlexRIO FPGA boards are very adaptable and can be used to achieve high-throughput since they allow direct data transfer between multiple FPGA at rates as high as 1.5 GB/s. This can significantly simplify multi-FPGA systems, which often communicate via a host PC. This feature allows expansion of our system to further processing stages, making it flexible for a variety of applications. Figure 3 shows a basic overview of a PXIe-based, multi-FPGA system with a host PC controller connected through a high-speed bus on a PXIe chassis.

B. Basic Architecture

Most 2D FFT implementations on FPGAs use row and column decomposition (RCD) with intermediate external DRAM storage. Acceleration of RCD-based 2D FFTs is usually dependent on the throughput of the 1D FFT used for column-by-column and row-by-row 1D FFT computations. This RCD for a \( N \times M \) image requires computation of \( N \) row-wise and \( M \) column-wise 1D FFTs. This means \( MN \) (or \( N^2 \) if \( M = N \)) values must be stored after the first (row or column)-wise computations. Since 2D FFTs are usually calculated for large images, which cannot be stored on the limited embedded-block RAM, external memory must be used. Hence, acceleration also depends on bandwidth and efficient
addressing of external memory. For small images block RAM or memory implemented via registers may be used as opposed to external memory. Register memory is usually faster and easier to use. Unlike external memory, it does not have limitations in terms of the number of available channels and bandwidth. However, such an approach is resource-intensive if the image is large. Uzun [3] presented an architecture for real-time 2D FFT computations using several 1D FFT processors with shared external RAM. For our 2D FFT implementation, we also used an approach based on RCD with multi-core 1D FFTs. We needed a 1D FFT implementation which did not require significant resources to achieve reasonably high throughput. After comparing several 1D FFT implementations including LabView FPGA’s own standard implementation, we used an Inner Loop Unrolling Technique (ILUT) [2]. A 1D FFT of length N has \( \log N \) FFT stages and each stage has \( N/2 \) butterfly units. ILUT unrolls a single FFT stage by executing several butterfly units in parallel. Figure 4 shows a basic flow of a 2D FFT implementation using ILUT. Local memory shown in Figure 4 is used to buffer data between external memory and 1D FFT cores. This local memory is divided into read and write components and is implemented using FPGA slices. This reserves block RAM (BRAM) for temporary storage of vectors required for calculating the 2D FFT of the boundary image. The Control Unit (CU) organizes scheduling of transferring data between local and external memory.

As shown mathematically in the previous section, the initial row-wise FFTs for the boundary image can be calculated by computing the 1D FFT of the first (boundary) vector and the FFTs of reaming vectors can be computed by appropriate scaling of this vector. The boundary image is calculated in the host PC. The entire boundary image does not need to be transferred to the FPGA, we only need the boundary column vector for 1D FFT calculation of the first and last column. We also need the boundary row vector for appropriate scaling of \( \hat{v} \) for the 1D FFT of every column between the first and last columns. To minimize data transfer between the host and the FPGA we associate an extra row and a column vector for 1D FFT calculation of the first and last columns. To minimize data transfer between the host and the FPGA we associate an extra row and a column vector at the end of each image frame being transferred. So when transferring a \( N \times M \) image frame, the number of data points sent from the host PC is \( NM+N+M \). Row and column vectors of the boundary image are stored in block RAM (BRAM) while the image frame is directly stored in external DRAM. This allows column-by-column 1D FFT calculations of the boundary image to be processed in parallel with FFT computations of the actual image. A control unit schedules all read-write operations between external and local memories.

V. RESULTS

Table II compares several different RCD-based 2D FFT hardware implementations. None of the previous implementations use periodic-plus-smooth decomposition to simultaneously remove edge artifacts. Our implementation effectively performs twice the number of 1D FFT computations (for the original and boundary image) for each image frame, but requires only a fraction of higher run time. As demonstrated above, this acceleration has been achieved by parallelization of 2D FFT calculations for the original and boundary images and by reducing the external DRAM access by optimizing the original periodic-plus-smooth decomposition algorithm. Our methods were tested using extensive synthesis and benchmarking using a Xilinx Kintex 7 FPGA communicating with a host PC on a high-speed PXIe bus.

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