An Efficient FIR Filter Based on Hardware Sharing Architecture Using CSD Coefficient Grouping for Wireless Application

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Abstract
FIR filter is an essential part of digital signal processing that is extensively used in many areas such as wireless applications and digital processing system. The FIR filter design is inherently stable and has a linear phase characteristic under symmetric conditions, but its implementation often involves complexity and a large filter length to achieve specific design requirements. In this paper, the complexity of the FIR filter is reduced by eliminating the repeated subexpression in a canonic signed digit (CSD) number system based filter operation. A new grouping method has been proposed for the CSD number system-based filter coefficient to minimize the number of unpaired nonzero bits in the filter coefficient. The statistical analysis of the proposed grouping method is performed and compared with other existing schemes. The number of unpaired nonzero bits in the proposed grouping scheme is reduced by an average of 24.11% as compared to other existing schemes. Further, an efficient FIR filter with hardware sharing architecture is designed and implemented to achieve a 14.65% reduction in average power consumption, and the average operation speed is increased by 10.1% compared to the other existing filter structures.

Keywords Finite impulse response (FIR) · Common subexpression elimination (CSE) · Binary sub-expression elimination (BSE) · Grouping methods · Filter architecture

1 Introduction

The digital filter is one of the most important processing element in any digital signal processing (DSP) system. FIR and IIR filters are the two basic structures used in DSP. Compared with IIR filter, FIR filter is the most applicable processing element in all modern digital applications such as multimedia application, mobile communication, wireless communication, etc., because of its linear phase characteristic under symmetric condition,
precision, adaptability using a programmable processor, and exact reproducibility. The Digital system can be realized using a DSP processor or customized hardware circuit fabricated using very large scale integrated (VLSI) circuits and can process both real-time and offline data. The FIR filter can be designed using various structures, each representing a different implementation with the same functionality. The data broadcast structure is preferred over various types of existing filter structures for a limited number of taps because of constant data arriving time and pipelined data flow, as shown in Fig. 1. Multi-standard communications facilities with the least amount of overlap between multiple input radio channels are required by advanced wireless communications devices such as modern RF receivers and battery-powered portable communications transceivers. A sharp digital filter with a very narrow transition width enables alias-free switching between the desired frequency bands. Thus the low pass filter employed in wireless communication must be realized to operate at high speed and consume low power, which can be achieved by using efficient and low power FIR filter architecture. This kind of filter implementation has gained more attention in the last decade. The number of algorithms has been presented in the literature for coefficient multiplication with low power requirement and fast FIR filter with an optimized number of add and shift operations [1, 2]. A low complex FIR filter based on a binary subexpression elimination method has been presented to provide neighboring channel attenuation specification and related narrow transition bands, particularly for wireless applications. The computation in FIR filter is mainly dependent on coefficient multiplication and the use of partial products in the multiplier that limits the silicon area and power requirement of the filter operation [3].

T. Sinha and Bhaumik [4] presented the modified multistage frequency response masking based FIR filter structure to reduce arithmetic operations. Vinod et al. [5, 6] introduced a standard subexpression elimination method to reduce hardware requirements by eliminating the redundant set of computations in the fixed coefficient FIR filter. The comparative analysis for hardware reductions was achieved using the horizontal common subexpression (HCS) and the vertical common subexpression (VCS) in digital filters realization. It is found that HCS provides better reductions in the hardware requirements in comparison to VCS based filter operation. Chang et al. [7] proposed an efficient hardware architecture for FIR filter by using CSD multiplier with runtime recovery strategy. A novel structure of the product accumulation section based FIR filter was presented by relocating the existing delays into the structural adders [8]. Jiang et al. [9] proposed a method for FIR filter design for multicarrier modulation systems. A new programmable CSD encoding structure was outlined to make high speed, low power filter operations. An algorithm was described to reduce the number of CS for coefficient multiplication in filter operation [10–12]. Mahesh et al. [13] presented a low power and high order FIR filter based on a new CSE method. The signed digit number system, such as CSD-based filter coefficient, was analyzed and found that HCS or VCS is not completely exploited due to the opposite sign of CSD coefficient digits. Another issue with the sign digit number system compared to the binary

Fig. 1 Block diagram of L-tap data broadcast FIR filter
number system is the subtraction operation in the coefficient multiplication process. The proposed approach uses a binary representation of a coefficient that reduces the hardware resource in filter operation. An optimization-based FIR filter approach was presented with low power consumption and reducing ripples in passband and stopband [14, 15]. Yao et al. [16] introduced a novel CSE scheme for a fixed-point FIR filter. In this method, the coefficient multiplier is realized using add and shift operation and the requirement of the adder is directly related to the number of nonzero digits present in the filter coefficient. Hameed et al. [17] demonstrated a sharp programmable analog FIR filtering response with low power consumption. Seshadri et al. [18] suggested the fast moving average FIR filter response using look ahead arithmetic with reduced pipeline delay and less hardware complexity. A new design algorithm using an extended double-base number system has been discussed for low complexity FIR filters [19, 20]. Touli et al. [21] presented a combination of multibit flip flop and a data-driven clock gating approach for power efficient filter structure. Patali et al. [22] developed a high throughput filter by using pipelining and retiming structure. This design was used for denoising of ECG signals. Another way of implementing an efficient FIR filter was proposed by Jia et al. [23], in which a novel CSD coefficient grouping scheme was used to remove the redundant set of computation in coefficient multiplication. An efficient filter architecture was proposed based on a new grouping scheme that is advantageous in silicon area, minimizing power consumption, and fast speed for large length of FIR filter. Vishal et al. [24] presented a framework for FIR decimator using hybrid signed digit arithmetic. A novel FIR filter was described using retimed MAC unit with delay optimization by Subathradevi et al. [25].

In this paper, we propose a new grouping method for nonzero digits present in CSD encoder of the filter coefficient. The number of redundant computations in coefficient multiplication is further eliminated, and its statistical analysis is presented. Furthermore, the reconfigurable filter architecture is illustrated based on the hardware sharing structure to minimize the logic resources.

The remaining part of the paper is organized as follows. A new grouping method for CSD number system based filter coefficient is shown in Sect. 2. Section 3 presents the statistical analysis of all possible common subexpression patterns based on the proposed grouping method in a 16 bits quantized filter coefficient. A reconfigurable FIR filter based on hardware sharing architecture is described in Sect. 4. The layout of the novel preprocessing unit is also illustrated. The performance evaluation of the proposed efficient FIR filter with hardware sharing is described in Sect. 5. The conclusion of the paper is provided in Sect. 6.

## 2 Proposed new grouping method for CSD filter coefficient

### 2.1 FIR Filter Using CSD

A linear, time-invariant, and nonrecursive finite impulse response (FIR) filter is explained by the difference equation as given below.

\[
y[n] = \sum_{i=0}^{L-2} b_i \cdot x[n - i]
\]  

(1)
where \( L - 1 \) is the filter length, \( y[n] \) is the output signal, \( b_i \) is filter coefficient of \( i \)th order and \( x[n - k] \) is the input sampled signal at particular time. Further \( b_i \) coefficient can be encoded in a CSD number system as follows,

\[
b_i = \sum_{j=0}^{M_i-1} C_{ij} \cdot 2^{-S_{ij}}
\]

(2)

where \( M_i \) represents the total number of nonzero bits in a coefficient \( b_i \) and \( C_{ij} \in \{0, \ldots, W-1\} \) where \( W \) is the word length of quantized coefficient. Therefore the equation (1) may be rearranged as-

\[
y[n] = \sum_{i=0}^{L-1} \sum_{j=0}^{M_i-1} C_{ij} \cdot 2^{-S_{ij}} \cdot x[n - i]
\]

(3)

### 2.2 CSD Arithmetic

It is well known that the number of additions performed in a coefficient multiplication equals one less than the number of nonzero bits available in the \( b_k \) coefficient of the filter. The constant coefficient can be represented in a number system with a minimum number of nonzero bits to reduce the power demand and silicon area. Since CSD representation contains a minimum number of nonzero bits, it is preferably used to represent the filter coefficient. A CSD number system is a special case, where a radix-2 signed digit is represented with the set \{1 0 − 1\}. The salient properties of CSD number representation are as follows-

- This is unique number.
- The product of any two adjacent digits is zero.
- The CSD representation of a number has the least possible number of nonzero bits.

\[
P_{nz} = 1/3 + (1/9N)[1 - (-1/2)^N]
\]

(4)

where \( N \) is number of bits. As \( N \) becomes larger, the probability of nonzero bit tends to be one-third. however for binary \( N \)-bit number, the probability of one particular bit being nonzero is 1/2.

The main objective of this work is to demonstrate use of an unique method by considering a group with two nonzero bits separated by two zeros in coefficient multiplication. In previous work [23], two prime pattern \{1 0 1\}/[− 1 0 − 1] and \{1 0 − 1\}/[− 1 0 1] have been considered in grouping method to reduce the set of redundant computation in filter operation. This grouping pattern covers almost 70% nonzeros in terms of average frequency of occurrence in a 16 bit quantized filter coefficient. The proposed new grouping method defined for CSD number system based filter coefficient is as follow:

- **I prime pattern**—The group of two nonzero bits separated by a zero bit. e.g. \{1 0 1\}/[− 1 0 − 1] and \{1 0 − 1\}/[− 1 0 1].
- **II Prime Pattern**—A Pair of nonzero bits separated by two zero bits are considered as an individual group. e.g. \{− 1 0 0 − 1\}/[1 0 0 1] and \{− 1 0 0 1\}/[1 0 0 − 1].
- **III Prime Pattern**—If there are three or more zeros between two nonzero bits then each nonzero bit is recognized as an individual representation. e.g. \{1\}/[− 1].
\[ bi = \begin{bmatrix}
1 & 0 & 1 \\
0 & 0 & 0 & 1 \\
1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1
\end{bmatrix}_{\text{CSD}} \\
G_1 = [1, 0, -1], \quad G_2 = [1, 0, 0, -1], \quad G_3 = [1] \\
\]

Fig. 2 Proposed grouping pattern for CSD based filter coefficient

Fig. 3 The flowchart of proposed grouping method for CSD coefficient
The flowchart for proposed grouping method of the CSD based 16 bits quantized filter coefficient $b_i = [10 - 100100 - 100010]$ is shown in Fig. 3 to extract the common subexpressions as

1. The nonzero bits in CSD filter coefficient are noted;
2. Two nonzero bits separated by a zero bit is considered as I CS pattern;
3. Two zero bits between two nonzero bits is selected as II CS pattern;
4. if more than two zero bits between two nonzero bits, each nonzero bit is considered as independent group as III CS pattern.

The grouping patterns should be computed first, and then applied to each tap for completion of the local computation. As a result, $b_i$ coefficient may be expressed as

$$b_i = \sum_{j=0}^{M-1} (-1)^{P_{ij}} C_{ij} \cdot 2^{-S_{ij}}$$

(5)

Here $P_{ij} \in \{01\}$, $S_{ij} \in \{0, \ldots, W - 1\}$ is the number of shifts of subgroup j and W is the wordlength of quantized coefficient. $C_{ij}$ is defined as a set of all possible prime pattern $(1 0 1)(1 0 -1)(1 0 0 1)(1 0 0 -1)$ in CSD $b_i$. This grouping pattern for CSD based coefficient of sample FIR filter shown in Fig. 2 can be explained as

- The group of bit $G_1 = [1 0 -1]$ is considered as Prime Pattern I.
- The group of bit $G_2 = [1 0 0 -1]$ is in Prime Pattern II.
- The $G_3 = [1]$ is considered as Prime Pattern III.

## 3 Statistical Analysis of Proposed Grouping Method for CSD Based Filter Coefficient

A new method for eliminating common subexpression method for CSD number system based filter coefficients is proposed. The main focus of this method is to explore and remove the redundant computation in filter operation. In previous works, the most common subexpression elimination methods are used on either CSD representation or binary number system based filter coefficients. But CSD coefficient is more popular because the number of nonzero bits is about 30% less than the binary coefficient in filter operation. Thus, less hardware resource is required to realize the coefficient multiplier compared to binary representation [14]. The grouping method in the filter coefficient further reduces the hardware requirement in the realization of the coefficient multiplier [25]. This grouping method has enhanced computational efficiency due to the hardware sharing structure. The hardware sharing method is influenced by three main factors viz.

- The total number of nonzero bits present in filter coefficient.
- The number of common subexpression (CS) generated from the nonzero bits.
- The number of unpaired nonzero bits that do not contribute to the CSE.
In paper [12], the number of unpaired nonzero bits of the filter coefficient mainly affects the hardware requirement. Next, the number of CS of the filter coefficient influenced the hardware sharing method. Aforementioned both factors are dependent on the number of nonzero bits present in the filter coefficient. In this work, the sample FIR filter was designed with different passband frequency ($\omega_p$) and stopband frequency ($\omega_s$) in normalized mode i.e. distributed over the range from (0, 1)$\pi$. A narrow transition band $|\omega_s - \omega_p|$ varies from 0.01$\pi$ to 0.05$\pi$ has considered and relatively large transition band $|\omega_s - \omega_p|$ varies from 0.15$\pi$ to 0.20$\pi$ for designed low pass FIR filter. The narrowband filters are frequently used in wireless applications to attenuate the stringent adjacent channel.

The statistical analysis of the proposed grouping method for sample filter was performed for low pass FIR filter coefficients of different filter lengths as 20, 40, 80, 120, 200, 300, 400, 500, and 600 taps with 16-bits wordlength. The number of adders/subtractors mainly depends on the unpaired nonzero bits in the filter coefficient. The number of unpaired nonzero bits in the CSD number system-based filter coefficient is analyzed. Figure 4 illustrates the comparison of the average number of unpaired nonzero bits in CSD representation of the filter coefficient of commonly defined grouping scheme as [1 0 1]/[− 1 0 1] with proposed grouping scheme as [1 0 1], [− 1 0 1], [1 0 0 1] and [− 1 0 0 1]. In this comparison, the order of FIR filter varying from 20 to 600 with the same specifications as Table 1 is used. A binary coefficient shows the minimum number of unpaired nonzero bits, but it contains a large number of nonzero bits in the filter coefficient. Thus a binary coefficient involves a large number of arithmetic computations. Whereas in CSD representation, the proposed grouping method shows less number of unpaired nonzero bits than the other existing grouping pattern by an amount of 24.11% resulting in a reduction in hardware requirement as in Table 2. The number of adders/subtractors in filter operation is further reduced by the hardware sharing structure.

In the proposed grouping method, the occurrence of common subexpression of the new grouping pattern is also analyzed. The sample filter is designed with filter lengths varying from 20 to 600 taps. In each filter order, there are six sample filters designed with various passband ($\omega_p$) and stopband ($\omega_s$) frequency in normalized mode as defined earlier. The number of CS of each sample filter is calculated, and the results are shown in Fig. 5. It is found that the number of CS of the proposed grouping pattern increases for a narrow transition band with increasing filter order.

| Table 1 Sample FIR filter specification |
|-----------------------------------------|
| Sample FIR filter | Specifications |
| Filter order | 20–600 |
| Wordlength of coefficient | 16-bits |
| Narrow transition band $|\omega_s - \omega_p|$ | 0.01–0.02 |
| Wide transition band $|\omega_s - \omega_p|$ | 0.15–0.25 |
| Used number system | CSD representation |
A reconfigurable FIR filter with hardware sharing architecture based on the analysis performed in Sect. 3 is presented in Fig. 6. In digital filter, the coefficient multiplication can efficiently be performed by using shift and add operations. In order to reduce the computational load due to redundant operation in constant multiplication,
an subexpression elimination method can be used. This grouping method has enhanced computational efficiency due to hardware sharing structure. This filter architecture consists of a preprocessing unit and cascade of the filter section depending on the filter order. The preprocessing unit operates as a common computation engine to generate the partial product of five common subexpressions proposed in the new grouping method as \([1 \ 0 \ 1], [1 \ 0 \ -1], [1 \ 0 \ 0 \ 1], [-1 \ 0 \ 0 \ 1]\) and \([1]\). The filter section is used to further process the partial product generated by the preprocessing unit. All the filter sections are identical in the filter structure. In Fig. 6, \(x[n]\) is used as an input for preprocessing unit to produce partial products \(Y_1-Y_5\). These partial products are shared with all filter section. Each filter section computes the coefficient multiplication by using shifts and add/subs
operation and producing output signal $y[n]$. Details of subunit of filter architecture is discussed below.

### 4.1 Layout of Preprocessing Unit

The preprocessing unit is an integral part of filter architecture. This circuit structure is used to generate the partial products that are required in coefficient multiplication. In the proposed new extended grouping scheme, there are five common subexpressions as

$$Y_1 = x = [1]$$  \hspace{1cm} (6)

$$Y_2 = x + x_1 = [1, 0, 1]$$  \hspace{1cm} (7)

$$Y_3 = x - x_1 = [1, 0, -1]$$  \hspace{1cm} (8)

$$Y_4 = x + x_2 = [1, 0, 0, 1]$$  \hspace{1cm} (9)

$$Y_5 = x - x_2 = [1, 0, 0, -1]$$  \hspace{1cm} (10)

where $x_1$ and $x_2$ is defined as.

$$x_1 = (x \gg 2), \ x_2 = (x \gg 3)$$

A separate layout of the preprocessing unit is shown in Fig. 7. Where $\gg 2$ indicates an arithmetic shift-right through 2 bit operation and this is equivalent to the scaling method $2^{-2}$ and similarly for $\gg 3$. In the given layout, $x$ denotes the input signal. This input signal is fed to the preprocessing unit that computes the five output signals corresponding to the five common subexpressions. In this case, two adders, two subtractors and 2 bit/3 bit shifter are required to design the preprocessing unit. These precomputed terms $Y_1, Y_2, Y_3, Y_4$ and $Y_5$ are fed to corresponding five buses of filter section. Thus the filter output is computed by using the preprocessing unit and filter section.

Fig. 7 Layout of preprocessing unit
5 Performance Evaluation

The proposed reconfigurable FIR filter with hardware sharing architecture is designed and synthesized based on the FPGA family: Virtex 6, Device XC6vLx-75t, Package-1Lff484, which is a widely used logic family with large packing capacity and low power requirement. The sample FIR filter of order varying from 50 to 600 is designed with the narrow transition band of different passband and stopband frequencies in normalized mode $\omega_p$ and $\omega_s$ respectively. Next, the proposed FIR filter design with a new grouping scheme is compared to other existing FIR filters based on the common grouping method.

5.1 Comparison of Unpaired Nonzero Bits and Number of Common Subexpression in Filter Coefficient

As mentioned earlier, this paper proposes a new grouping scheme based on the CSD number system of the filter coefficient shown in Fig. 2. The average number of unpaired nonzero bits in CSD based filter coefficient is compared for three grouping methods (i) proposed grouping scheme, (ii) an existing grouping method [23], and (iii) binary number system based filter coefficient as shown in Fig. 4. The average numbers of unpaired nonzero bits that do not participate in Common Subexpression of CSD based filter coefficient are analyzed through the statistical method. The result shows that the average number of unpaired nonzero bits that do not contribute to Common Subexpression is reduced by 24.11% in CSD based filter coefficient compared to other existing grouping schemes. This average number of unpaired nonzero bits in the filter coefficient directly determines the number of computations in filter operation. The occurrence of the proposed grouping method in CSD based filter coefficient is also increased with the higher order of low pass

![Figure 8](image_url)  
**Fig. 8** Number of common subexpression for proposed grouping method, other existing grouping pattern in CSD based filter coefficient and total number of all possible grouping pattern
Table 3  Comparative chart of power consumption

| Filter order | Binary coefficient (mW) | Existing CSD grouping method (mW) | Proposed grouping method (mW) | Ratio-I OE-proposed/OE (%) | Ratio-II binary-proposed/binary (%) |
|--------------|-------------------------|----------------------------------|-------------------------------|---------------------------|-------------------------------------|
| 50           | 14.81                   | 13.48                            | 13.21                         | 2.0                       | 10.80                               |
| 100          | 23.43                   | 21.42                            | 20.92                         | 2.33                      | 10.71                               |
| 200          | 42.65                   | 38.31                            | 37.84                         | 1.22                      | 11.27                               |
| 300          | 64.32                   | 57.25                            | 55.28                         | 3.44                      | 14.05                               |
| 400          | 81.24                   | 71.09                            | 67.10                         | 5.61                      | 17.40                               |
| 500          | 104.72                  | 88.64                            | 85.16                         | 3.92                      | 18.67                               |
| 600          | 121.22                  | 102.94                           | 97.32                         | 5.46                      | 19.71                               |

Average power consumption 3.42 14.65

OE = Other existing grouping scheme

Table 4  Comparison chart

| S. no. | Touil et al. [21] | Seshadri et al. [18] | Jia et al. [23] | This work |
|--------|-------------------|----------------------|----------------|-----------|
| Architecture | Low power re-structural FIR filter | MA FIR filter using CIC method | Existing CSD Grouping method | Proposed grouping method |
| Taps   | 50–75             | 8–64                 | 50–500         | 50–600    |
| Power consumption (mW) | 37.82–49.34 | 132.42–138.50 | 13.25–87.94 | 13.21–97.32 |
| Maximum frequency (MHz) | – | – | 106.72–100.60 | 92.00–82.00 |

Fig. 9  Average of power consumption of binary and CSD coefficient
A new grouping method considering a group formed by pair of nonzero bits separated by two zeros was implemented to design FIR filter architecture with hardware sharing. When compared to an alternate scheme in a design example, the proposed method shows 24.11% reduction in the number of unpaired nonzero bits based on a statistical analysis of the sample FIR filter as shown in Fig. 8. The number of all possible grouping patterns is also increased by 31.4% for a higher-order filter compared to other existing grouping patterns in the filter coefficient.

5.2 Comparison of Average Power Consumption

The average power consumption of the proposed new grouping scheme based CSD filter coefficient multiplication in filter operation is compared with an existing CSD grouping method [23] and a binary representation of filter coefficient multiplication as shown in Fig. 9. The results given in Table 3 reveal that the average power consumption of sample FIR filter with the order below 200 and narrow transition band as $|\omega_s - \omega_p|$ varying from 0.01π to 0.05π is approximately equal. Whereas for higher order above 300 taps, it reduces by 3.42% compared to other existing grouping pattern CSD based filter coefficient. Table 4 compares this work with other previously published papers. Further, the average power consumption in the proposed filter design for higher order is reduced by 14.65% compared to filter design based on the binary representation of filter coefficient.

5.3 Comparison of Clock Frequency

The maximum clock frequency of the proposed FIR filter is shown in Fig. 10. The results show that the maximum clock frequency is comparatively low for binary coefficient filter design which can be attributed to a large number of computations in filter operation. The maximum working frequency of the proposed layout is increased by 10.1% given in Table 5 as it uses a considerably less number of partial products in filter operation.

6 Conclusion

A new grouping method considering a group formed by pair of nonzero bits separated by two zeros was implemented to design FIR filter architecture with hardware sharing. When compared to an alternate scheme in a design example, the proposed method shows 24.11% reduction in the number of unpaired nonzero bits based on a statistical analysis of the sample FIR filter as shown in Fig. 8. The number of all possible grouping patterns is also increased by 31.4% for a higher-order filter compared to other existing grouping patterns in the filter coefficient.

Table 5 Comparison of maximum frequency (MHz)

| Filter order | Binary coefficient (MHz) | Existing CSD grouping method (MHz) | Proposed grouping method (MHz) | Ratio-I binary-proposed/binary (%) | Ratio-II OE-proposed/OE (%) |
|--------------|--------------------------|-----------------------------------|-------------------------------|----------------------------------|----------------------------|
| 50           | 74.34                    | 89.36                             | 92.00                         | 23.75                            | 2.95                       |
| 100          | 71.17                    | 86.50                             | 91.10                         | 28.00                            | 5.31                       |
| 200          | 65.60                    | 78.24                             | 89.00                         | 35.67                            | 13.75                      |
| 300          | 76.00                    | 78.00                             | 88.20                         | 16.05                            | 13.07                      |
| 400          | 59.00                    | 74.09                             | 86.50                         | 46.61                            | 16.74                      |
| 500          | 57.00                    | 75.50                             | 82.00                         | 43.85                            | 8.60                       |

OE = Other existing grouping scheme
simulation results. The average power consumption of the proposed filter design for higher order is reduced by 14.65% compared to the filter design based on the binary coefficient and 3.42% less in comparison to other existing grouping pattern CSD based filter coefficients. The operation speed is increased by 10.1% in comparison to other existing grouping methods. Overall it can be concluded that the proposed scheme has significant savings on hardware resources and power consumption along with a moderate increase in speed of computational operation. Further studies can take a more narrow transition band and determine the hardware area requirements.

References

1. Hartley, R. I. (1996). Subexpression sharing in filters using canonic signed digit multipliers. *IEEE Transactions on Circuits Systems II, Analog Digital Signal Processing, 43*(10), 677–688.
2. Chandra, A., & Chattopadhyay, S. (2016). Design of hardware efficient FIR filter: A review of the state-of-the-art approaches. *Engineering Science and Technology, an International Journal, 19*(1), 212–226. https://doi.org/10.1016/j.jestch.2015.06.006.
3. Farshchi, F., Abrishami, M. S., & Fakhraie, S. M. (2020). New approximate multiplier for low power digital signal processing. In *Proceedings of 17th international symposium on computer architecture and digital systems (CADS)* (pp. 25–30).
4. Sinha, T., & Bhaumik, J. (2019). Design of computationally efficient sharp FIR filter utilizing modified multistage FRM technique for wireless communications systems. *Journal of Electronic Science and Technology, 17*(2), 185–192. https://doi.org/10.11989/JEST.1674-862X.70728080.
5. Vinod, A. P., Lai, E., Maskell, D., & Meher, P. K. (2010). An improved common subexpression elimination method for reducing logic operators in FIR filter implementations without increasing logic depth. *Integration, the VLSI Journal, 43*(1), 124–135. https://doi.org/10.1016/j.vlsi.2009.07.001.
6. Vinod, A. P., & Lai, E. M-K. (2005). Comparison of the horizontal and the vertical common subexpression elimination methods for realizing digital filters. In *IEEE International Symposium on Circuits and Systems* (pp. 496–499). https://doi.org/10.1109/TCAD.2004.840552.
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7. Chang, K. C., Lin, C. H., & Liu, C. W. (2014). Complexity-effective implementation of programmable FIR filters using simplified canonic signed digit multiplier. *Technical Paper 2014 International Symposium on VLSI Design Automation Test, VLSI-DAT 2014*, 1(2), 31–34. https://doi.org/10.1109/VLSI-DAT.2014.6834886.

8. Lou, X., Yu, Y. J., & Meher, P. K. (2016). Analysis and optimization of product-accumulation section for efficient implementation of FIR filters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 63(10), 1701–1713. https://doi.org/10.1109/TCASI.2016.2587105.

9. Jiang, L., Zhang, H., Cheng, S., Lv, H., & Li, P. (2020). An overview of FIR filter design in future multichannel communication systems. *Electron*. https://doi.org/10.3390/electronics9040599.

10. Ding, W., & Chen, J. (2015). Design of low complexity programmable FIR filters using multiplexers array optimization. *Proceedings of IEEE International Symposium on Circuits Systems (ISCAS)* (pp. 2960–2963). https://doi.org/10.1109/ISCAS.2015.7169308.

11. Tanaka, Y. (2016). Efficient signed-digit-to-canonical-signed-digit recoding circuits. *Microelectron. J.*, 57, 21–25. https://doi.org/10.1016/j.mejo.2016.09.001.

12. Mittal, A., Nandi, A., & Yadav, D. (2016). Comparative study of 16-order FIR filter design using different multiplication techniques. *IET Circuits, Devices and Systems*, 11(3), 196–200. https://doi.org/10.1049/iet-cds.2016.0146.

13. Mahesh, R., & Vinod, A. P. (2008). A new common subexpression elimination algorithm for realizing low complexity higher order digital filters. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(2), 217–229. https://doi.org/10.1109/TCAD.2007.907064.

14. Dwivedi, A. K., Ghosh, S., & Londhe, N. D. (2017). Low-power FIR filter design using hybrid artificial bee colony algorithm with experimental validation over FPGA. *Circuits, System and Signal Processing*, 36(1), 156–180. https://doi.org/10.1007/s00034-016-0297-4.

15. Sadeghipour, K. D., & Abbaszadeh, A. (2011). Efficient realization of reconfigurable FIR filter using the new coefficient representation. *IEEE International Symposium on Electrical Engineering, 8*(12), 902–907. https://doi.org/10.1109/TCAD.2004.840552.

16. Yao, C. Y., Hsia, W. C., & Ho, Y. H. (2014). Designing hardware-efficient fixed-point FIR filters in an expanding subexpression space. *IEEE Transactions on Circuits Systems I*, 61(1), 202–212. https://doi.org/10.1109/TCSI.2013.2268551.

17. Hameed, S., & Pamarti, S. (2018). Design and analysis of a programmable receiver front end based on baseband analog-FIR filtering using an LPTV resistor. *IEEE Journal of Solid-State Circuits*. https://doi.org/10.1109/JSSC.2018.2804044.

18. Seshadrir, R., & Ramakrishnan, S. (2021). FPGA implementation of fast digital FIR and IIR filters. *Concurrent Computing*, 33(3), 1–11. https://doi.org/10.1002/cpe.5246.

19. Chen, J., Chang, C. H., Feng, F., Ding, W., & Ding, J. (2015). Novel design algorithm for low complexity programmable fir filters based on extended double base number system. *IEEE Transactions on Circuits and Systems-I*, 62(1), 224–233. https://doi.org/10.1109/TCSI.2014.2348072.

20. Ray, D., George, N. V., & Meher, P. K. (2018). Efficient shift-add implementation of FIR filters using variable partition hybrid form structures. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 65(12), 4247–4257. https://doi.org/10.1109/TCSI.2018.2838666.

21. Touil, L., Hamdi, A., Gassoumi, I., & Mtibaa, A. (2020). Design of low-power structural FIR filter using data-driven clock gating and multibit flip-flops. *Journal of Electrical and Computer Engineering*. https://doi.org/10.1155/2020/8108591.

22. Patali, P., & Kassim, S. T. (2020). High throughput and energy efficient FIR filter architectures using retiming and two level pipelining. *Procedia Computer Science*, 171(2019), 617–626. https://doi.org/10.1016/j.procs.2020.04.067.

23. Jia, R., Yang, H.-G., & Guo, Z.-H. (2016). A computationally efficient Reconfigurable FIR Filter architecture based on coefficient occurrence probability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 35(8), 1297–1308. https://doi.org/10.1109/TCAD.2015.2504922.

24. Awasthi, V., & Raj, K. (2016). Compensated CIC-hybrid signed digit decimation filter. *World Academy of Science, Engineering and Technology International Journal of Electronics and Communication Engineering*, 10(12).

25. Subathradevi, S., & Vennila, C. (2017). Delay optimized novel architecture of FIR filter using clustered-retimed MAC unit Cell for DSP applications. *Applied Mathematics and Information Sciences*, 11(4), 1199–1205. https://doi.org/10.18576/amis/110427.

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