Profile-Guided, Multi-Version Binary Rewriting

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Abstract
The static instrumentation of machine code, also known as binary rewriting, is a powerful technique but suffers from high runtime overhead compared to compiler-level instrumentation. Recent research has shown that tools can achieve near-to-zero overhead when rewriting binaries (excluding the overhead from the application-specific instrumentation). However, the users of binary rewriting tools often have difficulties in understanding why their instrumentation is slow and how to optimize their instrumentation.

We are inspired by a traditional program optimization workflow, where one can profile the program execution to identify performance hotspots, modify the source code or apply suitable compiler optimizations, and even apply profile-guided optimization. We present profile-guided, Multi-Version Binary Rewriting to enable this optimization workflow for static binary instrumentation. Our new techniques include three components. First, we augment existing binary rewriting to support call path profiling; one can interactively view instrumentation costs and understand the calling contexts where the costs incur. Second, we present Versioned Structure Binary Editing, which is a general binary transformation technique. Third, we use call path profiles to guide the application of binary transformation.

We apply our new techniques to shadow stack and basic block code coverage. Our instrumentation optimization workflow helps us identify several opportunities with regard to code transformation and instrumentation data layout. Our evaluation on SPEC CPU 2017 shows that the geometric overhead of shadow stack and block coverage is reduced from 7.6% and 161.3% to 1.4% and 4.0%, respectively. We also achieve promising results on Apache HTTP Server, where the shadow stack overhead is reduced from about 20% to 3.5%.

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1 Introduction
Binary rewriting is a powerful technique that statically instrument the machine code of an application to monitor and collect data from its execution. It can be used to add security checks [14, 33, 34, 44], insert performance measurements code to analyze performance [36, 37, 39], and assess software correctness [5, 21].

While powerful, binary rewriting suffers from high runtime overhead compared to compiler-level instrumentation. We classify the runtime overhead incurred by binary rewriting into two types: tool overhead, which refers to overhead incurred by binary rewriting tools to support instrumentation, and application overhead, which refers to the overhead incurred by application specific instrumentation. Recent research on binary rewriting focuses on reducing tool overhead and has achieved near-to-zero tool overhead in many cases [16, 24, 38].

On the other hand, application overhead is optimized by binary rewriting application researchers, who design drastically different optimization strategies tailored to their own applications [5, 21]. These optimization strategies are often the results of numerous, trial-and-error attempts. We believe it is valuable to have a systematic approach for optimizing binary rewriting applications.

A traditional optimization approach for software programs is to profile the program to identify performance hotspots and transform the hotspots either through manual source code modification or tailored compiler optimizations. In addition, profile-guided optimizations have been shown to be effective for general program optimization [27] and even for compiler-level instrumentation [18].

Unfortunately, users of binary rewriting tools do not have aforementioned powerful weapons at their disposal. First, rewritten binaries generated by existing binary rewriting tools are not suitable for call path profiling [22]. Profiling tools such as HPC Toolkit [1] use call path profiling to attribute performance metrics, including running time, cache misses, and page faults, to program calling contexts. Users can know the specific functions, loops or statements that incur the most costs. Without call path profiling, users may know the overall inefficiency in their instrumentation, but cannot pinpoint the specific program contexts to design optimization strategies.

Second, existing binary rewriting tools are unable to perform necessary binary transformation to support instrumentation optimization. Compilers can drastically change program structures to perform a variety of optimizations, including function inlining and loop unrolling. While we should not expect a binary rewriting tool to have the strength of a
compiler with regard to program transformations, we believe there is a middle ground where useful optimizations can be achieved at the binary level.

In this paper, we present multi-version binary rewriting (MVBR) to fill this void. The basic idea of MVBR is to create multiple copies of a piece of code and support arbitrary control flow redirection among copied code, original code, and instrumentation. We can instrument these different copies in different ways (including not instrumenting some copies). “a piece of code” can refer to any programming language code constructs available at the binary level, including functions, loops, and basic blocks. This capability enables us to drastically transform the binary and customize instrumentation according to its invoking contexts.

We design Versioned Structure Binary Editing (VSBE) to support the binary transformations used by MVBR. VSBE provides a set of primitive binary transformation operations, including cloning a basic block, redirecting a control flow edge, and splitting a basic block. The composition of these operations can lead to power binary transformation.

MVBR also generates rewritten binaries that are suitable for call path profiling. Application researchers can interactively view performance metrics attributed to source code, investigate the conditions where the instrumentation incurs high overhead, and design new instrumentation strategies accordingly. In addition, we leverage profiles to guide where to apply MVBR, as making copies of code blindly will cause negative effects on the instruction cache. Profile-guided MVBR makes it possible to perform familiar, powerful optimizations, such as function inlining, at the binary level. For profile-guided MVBR, we directly use performance metrics collected at the binary level, so debug information or symbol tables is not needed.

To demonstrate the effectiveness of our new techniques, we apply MVBR to two typical binary rewriting applications and show how instrumentation profiling can reveal optimization opportunities and how profile-guided MVBR can materialize these opportunities.

The first one is shadow stack [14], which is a software security policy to mitigate return based attacks. It works by creating a thread-local shadow stack and inserting instrumentation that saves return addresses to the shadow stack at a function entry, and validating the actual return address on the original stack with the one from the shadow stack before function exits. The second one is basic block code coverage, which is a building block for software correctness assessment and fuzzing. The instrumentation allocates a new region of memory, where each byte of the memory represents whether an instrumented block has been executed or not, and inserts code that instrumented blocks to write the execution information. We choose these two applications because (1) they instrument at different code granularity (function vs basic block), and (2) they are from different application domains.

For both applications, we take the same optimization workflow: (1) implement a baseline instrumentation, (2) profile it to observe its performance characteristics and identify optimization opportunities, and (3) use profile-guided MVBR to realize the optimizations.

For shadow stack, among several optimizations, we highlight binary function inlining. An inlined callee does not need instrumentation as there is no return address any more. The original callee remains instrumented as we do not necessarily want to inline all calls to function. Existing work on function inlining [3, 4, 10, 30] focuses on when to inline a function and operates at the compiler level. We will present a new algorithm based on VSBE to inline functions at the binary level, which has to address several additional challenging regarding stack pointer adjustment and tail calls.

For block coverage, we identify performance issues caused by false sharing when running with multiple threads, hot instrumentation inside loops, and instrumentation data allocation that causes inefficient data cache utilization. We design a new instrumentation instruction sequence, profile-guided loop transformation, and profile-guided instrumentation data allocation to address these problems.

We evaluate our work using SPEC CPU 2017. For shadow stack, our optimizations reduced the maximal overhead from 31.0% to 10.0% and the (geometric) mean overhead from 7.6% to 1.4%. For block coverage, our optimizations reduced the overhead from over 100% to 12.1% maximal and 4.0% mean overhead. We also our optimizations to two real world software, including Apache HTTP Server, where the shadow stack overhead is reduced from over 20% to about 3%.

In summary, this work makes the following contributions:

- Multi-Version Binary Rewriting, a new binary-rewriting instrumentation technique that supports customizing instrumentation by transforming binaries,
- Versioned Structure Binary Editing, a new binary transformation technique as the foundation of multi-version binary rewriting,
- support for call path profiling in rewritten binaries, which enables interactive instrumentation performance analysis and profile-guided multi-version binary rewriting,
- instrumentation profiling analysis and new optimizations to improve shadow stack and basic block code coverage.

2 Related Work

We put our work in context by surveying related work of binary rewriting tools, profile-guided optimizations, and application specific research that uses binary rewriting.
2.1 Binary Rewriting Tools

Binary rewriting tools support inserting arbitrary code at arbitrary locations in the original binary. There are two main approaches to achieve this goal.

The first approach is code patching, which patches original code with trampolines (typically branch instructions) to redirect control flow from original code to a new area of code where instrumentation is inserted. Tools using this approach include Dyninst [6, 8, 24] and E9Patch [17].

E9Patch [17] uses instruction patching, which modifies individual instrumented instructions to branch to the new area of code. The new area of code contains only the instrumentation, the modified instruction, and a branch back to the original code. Instruction patching does not require any binary analysis and thus enjoys high generality. However, it incurs high tool overhead as the control flow may frequently bounce between original and instrumented code.

Incremental CFG Patching [24], implemented as an extension to the mainstream Dyninst, significantly reduces tool overhead by relocating all instrumented functions to the new area of code, modifying direct control flow to stay in relocated code area, and opportunistically modifying indirect control flow including jump tables and function pointers. Incremental CFG patching can achieve near-to-zero tool overhead and provides a failure mode analysis when the underlying binary analysis failed.

The second approach is IR lowering, which first lifts the binary to a low-level IR and then re-generate the rewritten binary. Tools in this category lift binaries to either tool specific IR [23, 38] or the assembly language [16, 19, 35]. Recent IR lowering tools enjoy near-to-zero tool overhead. However, this approach relies on complete binary analysis to be able to fully lift a binary. Tools either rely on runtime relocation entries [16, 38] or binary analysis heuristics without clear failure mode analysis [19, 23].

We observe that neither approaches can leverage optimization passes implemented in modern compilers. Such optimization passes in compilers typically work at a higher-level IR (such as LLVM IR). Our work is orthogonal to the research of binary rewriting tools.

2.2 Profile-Guided Optimization

Profile-Guided Optimization (PGO) has been successful in improving program performance [11–13, 26]. Representative PGO tools include Facebook BOLT [27, 28] and Google Propeller [20].

Our work leverages profiles to optimize instrumentation and differs from existing PGO research on the following two aspects. First, we work fully at the binary level, requiring no recompilation or relinking. While BOLT also performs optimization at binary level, BOLT requires link-time relocations to be present in the binary. Users of BOLT often have to recompile the program with flag `-Wl, -q` to instruct the linker to retain link time relocation entries. Google Propeller also requires recompilation to perform PGO.

Second, existing PGO focuses on improving code and data layout to improve instruction and data cache efficiency. In contrast, our work uses profiles to guide binary transformation to elide instrumentation. In other words, our work uses PGO to improve instrumentation policies, while existing PGO research focuses on improve general program execution efficiency. Orthogonally, we can leverage existing code layout PGO policies to further improve overall performance.

Duta et al. [18] uses profiles to elide instrumentation to reduce the overhead of the defenses for transient execution attacks at the compiler level. Compared to this work, we work at the binary level and provides a general instrumentation optimization strategy.

2.3 Binary Rewriting Applications

We discuss the state-of-the-art implementations of shadow stack and block coverage at the binary level, which will serve as the baselines in this work.

2.3.1 Shadow Stack. Shadow stacks prevent control flow hijacking attacks which are based on modifying a return address on the call stack. Shadow stacks maintain a copy of the regular stack in a tamper-proof region, and check that both copies match on all function returns. This scheme is effective against code reuse attacks like Return-oriented programming (ROP) [29] and return-to-libc [40].

The basic implementation of shadow stack instruments every function entry and exits. Naturally, one can skip instrumenting a function if the function will never overwrite any return address. The idea of using program analysis to reduce instrumentation is often leveraged by compiler level instrumentation. For example, gcc’s `-fstack-protector` flag will insert stack guard for functions that call `alloca`, and functions with buffers larger than 8 bytes.

We find that there is no existing work that utilize static binary analysis to improve shadow stack done at the binary level. Therefore, for shadow stack, the baseline used in this work instruments every function.

2.3.2 Block Coverage. Code coverage determines how much and which piece of code is executed for a given input. We use block coverage as the example. Our optimization strategies can be extended to edge coverage.

A naive implementation is to instrument every basic block. Previous research showed that we can reduce instrumentation by performing dominator analysis on the control flow graph of a function [2]. This optimization has been shown to be also effective at binary level [5], which will be the baseline for block coverage in our work.
3 Versioned Structure Binary Editing

VSBE improves the seminal work of Structure Binary Editing (SBE), presented by Bernat and Miller [7]. SBE defines a set of binary transformation operations, including block cloning, control flow edge redirection, and function cloning. However, SBE does not support redirecting indirect control flow that uses jump tables, which are often used by compilers to generate switch statements in C/C++. In addition, transformation operations provided by SBE do not always compose, which limits its capability to design complex binary transformations. In this section, we describe how VSBE to address these weaknesses.

3.1 Definitions

We build upon the definitions used by SBE.

Control Flow Graph: We start with a standard CFG definition, \( G = \langle B, E, F \rangle \), where \( B \) is a set of basic blocks, \( E \) is a set of control flow edges between the basic blocks, and \( F \subseteq B \) is a set of entry blocks of functions.

Basic Block: A basic block, \( b = \langle s, t, v, j > \), represents a sequence of machine instrumentations that have incoming control flow only at its start and outgoing control flow only at its exit. \( s \) and \( t \) represent the start and end address of a basic block.

We add a version number \( v \) to the definition of a basic block. Given an original block \( b \) starting at address \( s \), all clones of this block will have the same starting address \( s \). Therefore, it is necessary to have a distinct version number for each of them. Conventionally, the version number for all original blocks are 0. The version numbers of cloned blocks should be set based on certain semantic grouping. For example, when we clone a loop, all basic blocks inside the loop should have the same version number. In Section 4, we will present examples of setting version numbers.

We add \( j \) to represent a potential jump table used by a basic block. If a basic block does not use a jump table to compute indirect jump targets, \( j \) is empty. Otherwise, \( j = \langle ts, te, stride, slice \rangle \), where \( ts \) is the start address of the jump table; \( te \) is the end address; \( stride \) is the size of a jump table entry; \( slice \) is a backward slice from the indirect jump that includes all instructions needed for computing the control flow target. The values for each element in \( j \) can be calculated during CFG construction, which is a capability provided by many modern binary analysis tools [15, 25, 32].

Control Flow Edge: A control flow edge, \( e = \langle b, b', type \rangle \), represents control flow transfer from a source block \( b \) to a target block \( b' \), annotated with a transfer type \( type \). In SBE, edge types include direct, conditional-taken, condition-not-taken, fall-through. We reduce conditional-not-taken, fall-through all to direct. The reason for this change is that after making multiple copies of a code, copies of a fall-through edge will not be fall-through any more.

Function: A function is defined as a set of basic blocks that is reached by traversing only intra-procedural edges from the entry block. This definition for a function can cope with challenging cases where functions share basic blocks and functions have non-contiguous basic blocks.

3.2 Primitive CFG Transformation Operations

SBE defined several primitive CFG transformation operations as the foundation for performing binary transformation. We discuss how we improve these operations in VSBE.

Figure 1 shows an example of cloning a function. The steps of cloning a loop are similar. Figure 1a shows the original CFG of the example function. This function has four basic blocks. The entry block A has an indirect jump, whose targets include block B, C, and D. Block B, C, and D are return blocks. The subscripts after the block name represents its version number. Blocks with version number 0 are original code. Blocks with version number 1 are copied code.

Block Clone: In SBE, cloning a basic block \( b \) includes cloning the block itself and also cloning the outgoing edges of the block. The cloned block does not have any incoming edges. Users of SBE must perform edge redirection to create incoming control flow to the new block. As shown in Figure 1b, we clone all blocks in the function. Outgoing edges of block \( A_0 \) remain targeting \( B_0, C_0, \) and \( D_0 \).

Edge Redirection: Conceptually, edge redirection is simple to do as we only need to update the target block of an edge. However, SBE does not support redirecting indirect edges. The targets of indirect edges are determined through runtime computation. To redirect indirect edges, we must modify the computation of the indirect edge targets. VSBE support redirecting indirect edges by cloning jump tables and modifying jump target calculation. As shown in Figure 1c, we redirect the targets of the new edges from \( B_0, C_0, \) and \( D_0, \) to \( B_1, C_1, \) and \( D_1, \) respectively.

Block Split: SBE defines that we can split a block by choosing an address inside the block range. The result of block split is that the original block is shrunk, a new block is created at the split address, and a new edge is created from the shrunk block pointing to the new block.

The newly created edge can then be redirected to other blocks, which makes the second half of the block dead code. This achieves the goal of removing instructions.

3.3 Code and Data Generation

For a basic block \( b = \langle s, t, v, j > \), we copy the instructions in the address range \( [s, t] \) from the original binary and update every instruction that uses PC-relative addressing to the same global data is referenced. During this step, if \( j \) is not empty, we do not emit new a jump table as the addresses of the indirect jump targets in the rewritten binary may have not been set.

When generating a control flow edge, for direct edges and condition-taken edges, we generate a direct branch and
We show how to compose primitive binary transformation operations that reference them. Suppose we need to update a block \( b_1 =< s_1, t_1, v_1, j_t > \) and \( j_t =< t_{s'}, t_e', \text{stride}, \text{slice} > \) to use a new jump table. The new jump table \( j_t' =< t_{s'}, t_e', \text{stride}, \text{slice} > \) is allocated with the following property. First, \( t_{s'} \) will be the first available virtual address to hold the new table and \( t_{s'} \) is aligned based on the table stride to avoid access violation. \( t_{e'} \) can be computed by adding the table size to \( t_{s'} \). The contents of the jump table are determined by target blocks, which may have been redirected and are different from the original targets. If the entry of a target block is instrumented, the target address should be the beginning of instrumentation. Otherwise, instrumentation may be skipped. We also need to update the instruction that computes the location of the jump table to reference the new table. From \( \text{slice} \), we can determine the original instruction and its belonging basic block that performs the computation. Finally, we use the version number \( v_1 \) to lookup the correct clone that contains the instruction to update.

Next, we describe the algorithm for inlining binary functions. As shown in Algorithm 1, it takes a call block \( cb \) as input. Here, we assume that \( cb \) makes a direct function call. For an indirect call, we first do indirect call promotion [18] that transforms an indirect call site to directly call a subset of the call targets, and then apply direct call inlining to the promoted calls.

Line 2 - 4 identify and clone the callee for inlining. At line 5, we utilize procedure \( \text{SplitAndRedirect} \) to split the input call block \( cb \) before its last instruction (i.e. the call instruction), and redirect the outgoing edge to the cloned function entry block. At line 6, procedure \( \text{RedirectReturns} \) will iterate every cloned return block and use \( \text{SplitAndRedirect} \) to remove its last instruction (i.e. the return instruction), and redirect outgoing control Flow to the call fall-through block in the caller.

\( \text{SplitAndRedirect} \) is shown at line 9 - 18. If the block to split only has one instruction, we do not need to split block. Instead, we need to redirect every incoming control flow edge to the new target, as shown at Line 11 - 13. Otherwise, we split the block at its last instruction and redirect outgoing edge to the new target.

Algorithm 1 An algorithm for binary function inlining.

1: procedure \( \text{BinaryFunctionInlining}(cb) \)
2: \( \text{callee} \leftarrow \text{getCallee}(cb) \)
3: \( \text{cftb} \leftarrow \text{getCallFTBlock}(db) \)
4: \( \text{cloneEntry, cloneRetBlocks} \leftarrow \text{CloneFunction(callee)} \)
5: \( \text{SplitAndRedirect}(cb, \text{cloneEntry}) \)
6: \( \text{RedirectReturns}(\text{cloneRetBlocks, cftb}) \)
7: end procedure
8: procedure \( \text{SplitAndRedirect}(b, \text{newTarget}) \)
9: if numberofInstruction\((b) == 1\) then
10: for \( e \in \text{pred} (b) \) do
11: \( \text{RedirectEdge}(e, \text{newTarget}) \)
12: end for
13: else
14: \( e \leftarrow \text{SplitBlock}(b, \text{lastInstructionAddress}(b)) \)
15: \( \text{RedirectEdge}(e, \text{newTarget}) \)
16: end if
17: end procedure
**Setting Version Number:** For each original function, we prepare a version number counter. When we make a copy of a basic block during inlining, we increment and use the counter of the original function where the cloned block belongs to. This strategy can support the case where an original function is instrumented multiple times to another function.

**Stack Pointer Adjustment:** The removal of call and return instructions means that the inlined callee will be executed with a +8 offset for the stack pointer compared to without inlining. This can cause access violation when the callee stores or loads a 16-byte (or larger) data element using the stack, as these memory accesses must be aligned at 16-byte (or larger) boundary. Note that function inlining at the compiler level does not need to worry this problem as the compiler will adjust these memory references accordingly. We address this issue by emitting a "lea %rsp, -8" instruction before the inlined code and a "lea %rsp, 8" instruction after the inlined code to ensure our inlining does not change the stack pointer.

**Tail Calls:** Suppose we have function A calls B, B tail calls C, and we want to inline B into A. Without inlining, C will return to A’s call site to B. After performing inlining B into A, C cannot return to A anymore as there is no return address. To handle this issue, we put the address of A’s call site to the stack pointer before the tail call in B. In this way, C will correctly return. Note that C is still instrumented.

### 4.2 Multi-Version Loop Instrumentation

For idempotent instrumentation, executing it once is equivalent to executing it multiple times with regard to its semantics. We observe that such idempotent instrumentation often incurs unnecessary overhead when it is inside loop. We present multi-version loop instrumentation to optimize this case. Without loss of generality, we use block coverage, which is idempotent, as an example in this section.

We start with an example shown in Figure 2 to illustrate the basic idea of multi-version loop instrumentation, and then describe an algorithm for it. Figure 2a shows the baseline instrumentation for block coverage. In this example, we have a function with four basic blocks, denoted as $A_0$, $B_0$, $C_0$, and $D_0$ respectively. Instrumented blocks are shaded. $B_0$ and $C_0$ are inside a loop and are instrumented. In this baseline instrumentation, if the loop is executed many times, instrumentation in $B_0$ and $C_0$ will incur unnecessary overhead, without increasing any coverage information.

Figure 2b shows the results of applying multi-loop instrumentation. First, we loop three times, so we have block $B$ and $C$ with version number from 1 to 3. Different loop versions are instrumented differently: for version 1, only $C$ is instrumented, while $B$ is not; for version 2, only $B$ is instrumented, while $C$ is not; for version 3, neither $B$ nor $C$ is instrumented.

To understand why loop clones are instrumented in the aforementioned way, we denote a bit vector $< iSC, iSB >$, where $iSB$ ($iSC$) is 1 if and only if the instrumentation for $B$ ($C$) has been executed. Instrumentation for loop version 1 represents state $< 0, 1 >$. Since instrumentation for $B$ has been executed before, $B_3$ does not need to be instrumented. And since instrumentation for $C$ has not been executed, $C_1$ is instrumented. The same reasoning applies to loop version 2 and 3. In addition, if we convert the state bit vector to the corresponding decimal value, it matches the version number of the loop.

Next, we redirect control flow edges among loop clones. The principle is still based on the state bit vector. For example, for version 0 whose state vector is $< 0, 0 >$, if $B_0$ is executed, it means the state has transitioned to $< 0, 1 >$; therefore, the outgoing edges of $B_0$ should be redirected to the loop representing state $< 0, 1 >$, which is loop version 1. Similar, if $C_0$ is executed, it means the state has transitioned to $< 1, 0 >$; therefore, the outgoing edges of $C_0$ should be redirected to loop version 2. For targets outside the loop, we do not need to redirect edges. For example, $C_0$’s outgoing edge to $D_0$ is not redirected.

For blocks inside a cloned loop that are not instrumented, executing such blocks do not change the instrumentation state. Therefore, we should not redirect their outgoing edges. For example, as $B_1$, $C_2$, $B_3$, $C_3$ are not instrumented, their outgoing edges are not changed.

Then, we consider a sample execution trace of the function to compare multi-version loop instrumentation with the baseline. Suppose we have a block execution trace

$$A_0 \rightarrow B_0^N \rightarrow (C_0 \rightarrow B_0)^M \rightarrow C_0 \rightarrow D_0$$

(T1)

where the superscript means the number of iteration. In the baseline, instrumentation for $B$ will be executed $N + M$ times, and instrumentation for $C$ will be executed $M + 1$ times. In the multi-version loop instrumentation, the execution trace is converted to

$$A_0 \rightarrow B_0 \rightarrow B_1^{N-1} \rightarrow C_1 \rightarrow (B_3 \rightarrow C_3)^M \rightarrow D_0$$

(T2)

Trace T2 and Trace T1 are semantically equivalent. However, as only $B_0$ and $B_2$ contain instrumentation for $B$, instrumentation for $B$ is executed only once in Trace T2. Similarly, as only $C_0$ and $C_1$ contains instrumentation for $C$, instrumentation for $C$ is also only executed once in Trace T2.

Now we describe the algorithm for performing multi-version loop instrumentation. Given a loop $L_0 = \{ b_1 , \ldots , b_n \}$ and a subset of instrumented blocks $\text{insto} \subseteq L_0$, Algorithm 2 shows the steps for multi-version loop instrumentation.

At Line 2, we calculate the number of copies needed, which is exponential to the size of $\text{insto}$. Obviously, this will not scale to large loop where we may need to instrument thousands of blocks. In Section 5, we will show how to use profiles to identify the top $K$ hot blocks, and only make loop clones for these hot blocks.
We augment binary rewriting to support call path profiling (Line 18), and enumerate every outgoing edge of the current version number \( v \) to call path profiling. RA address mapping [24] to call path profiling. RA address mapping may cause stack unwind to fail for rewritten binaries. In addition, there is no corresponding frame information for the inserted instrumentation. These two factors may cause stack unwind to fail for rewritten binaries.

At Line 3 - 5, we clone the loop and set the version number for each clone accordingly. At this point, the control flow of each clone loop stay in the same version. The main part of the algorithm is devoted to redirect control flow among copies of loops. We enumerate every version of loop (Line 6), and for each version of loop, we enumerate every instrumented block with an index (Line 7) and denote the corresponding cloned block with \( \text{inst}_0, \text{index} \) (Line 8), where \( v \) is the version number and \( \text{index} \) is the assigned index of the block.

If the \( \text{index} \)th bit of \( v \) is set, it means that the corresponding block does not need instrumentation as the instrumentation has been executed already. If not set, we instrument the block (Line 10), and handle transitions between loop clones by using procedure \( \text{LoopCloneTransition} \) (Line 11).

\( \text{LoopCloneTransition} \) computes the new version number (Line 18), and enumerate every outgoing edge of the current block to determine if we need to redirect this edge (Line 19 - 24). At Line 20, BlockLookup\((b, v)\) returns the block that has version number \( v \) and has the same start address as input \( b \). It is used to lookup a transition target.

### 5 Instrumentation Performance Analysis

We augment binary rewriting to support call path profiling and integrate the support in HPCToolkit [1].

HPCToolkit uses call path profiling. It interrupts program execution either periodically (using timer interrupts) or when the event buffer of the Performance Monitoring Unit (PMU) is full. It then processes corresponding performance events and performs a stack unwind to associate a sample with the current calling context.

Stack unwinding is often based on frame information encoded in .eh_frame sections. Existing binary rewriting tools do not update .eh_frame sections when generating rewritten binaries. In addition, there is no corresponding frame information for the inserted instrumentation. These two factors may cause stack unwind to fail for rewritten binaries.

#### 5.1 Address Mapping Table

We augment RA Address Mapping introduced by Incremental CFG patching [24] to call path profiling. RA address mapping instruments the stack unwinding code in language runtime to translates the return address on stack back to original return address, which enables rewriting C++ exceptions and Go binaries. However, RA address mapping only captures return addresses of call sites in a binary. During call path profiling, a software interrupt can happen at any address, not just at return addresses. We augment this mapping to cover all the code.

Each entry in our address mapping table represents a contiguous interval in the rewritten binary. It includes three fields: the start of the address in the rewritten binary, the length of the interval, and the start of the address in the

### Algorithm 2 An algorithm for multi-version loop instrumentation.

```plaintext
1: procedure MVLoopInstrumentation( \( L_0, \text{inst}_0 \) )
2: \( \text{copies} \leftarrow 2^{\text{inst}_0} \)
3: for \( v \in \{1, \ldots, \text{copies} - 1\} \) do
4: \( L_0, \text{inst}_0 \leftarrow \text{cloneLoop}(L_0, v) \)
5: end for
6: for \( v \in \{0, \ldots, \text{copies} - 1\} \) do
7: for \( \text{index} \in \{0, \ldots, |\text{inst}_0| - 1\} \) do
8: \( \text{srcb} \leftarrow \text{inst}_0, \text{index} \)
9: if isBitClear(v, index) then
10: \( \text{Idempotent instrumentation(srcb)} \)
11: \( \text{LoopCloneTransition}(v, \text{index}, \text{srcb}) \)
12: end if
13: end for
14: end for
15: end procedure

16: procedure LoopCloneTransition(v, index, srcb)
17: \( \text{newV} \leftarrow \text{setBit}(v, \text{index}) \)
18: for \( e \in \text{succ}(%\text{srcb}) \) do
19: \( \text{trgb} \leftarrow \text{BlockLookup(targetBlock(e), newV)} \)
20: if isInLoop(trgb, b_{newV}) then
21: \( \text{RedirectEdge}(e, \text{trgb}) \)
22: end if
23: end for
24: end procedure
```

Figure 2. An example of multi-version loop instrumentation to optimize idempotent instrumentation.
corresponding original binary. For instrumentation code, there is no original corresponding address, so the third field is set to -1.

We then modify HPCToolkit to load this mapping address table during profiling and change its code to translate the PC values.

Our address mapping table is only needed if we want to do instrumentation performance analysis or perform profile-guided instrumentation. It is not needed in production runs.

5.2 Alternative Stacks
Traditionally, instrumentation shares the same stack with the original program. This leads to several issues that require additional instructions, which not only cause runtime overhead but also make it more difficult to perform stack unwinding. We present a new instrumentation scheme, which uses segment register gs to hold a pointer to a memory region allocated at program and thread startup time.

System V ABI specifies a 128-byte red zone space beyond stack pointer. Program can directly save temporary values in the red zone without allocating a stack frame. For this reason, to guard against overwriting red-zone, original stack instrumentation first needs to move down the stack pointer. Under alternative stack instrumentation, we do not need to worry about the red-zone space on the original stack.

If the instrumentation includes a function call, it must conform to the stack pointer alignment requirement specified by the ABI. While stack pointer can be aligned with a simple and instruction, it causes other implications that must be addressed.

First, an and instruction overwrites flags; we may have to save and restore flags if the flag register is live at the instrumentation point. Second, the effect of stack pointer alignment cannot be easily reversed. This is contrary to moving down stack pointer with a constant offset, where we can move up the stack pointer with the same constant to reverse its affect. For this reason, we save %rsp to a scratch register, align the stack pointer, and save the original stack pointer to the current stack top. In this way, after instrumentation, we can recover the original stack pointer through a pop.

In contrary, instrumentation using alternative stacks only needs to two instructions. We save %rsp to the scratch space so that later we can restore it, and we change %rsp to the start of the alternative stack. Here, we do not need to align stack as we can pre-align the alternative stack when we allocate it.

Under our new alternative stack design, unwinding in instrumentation code is the same as unwinding from the first instruction after the instrumentation. In addition, instrumentation does not need to compensate the side effects caused by using the original stack.

5.3 Viewing Instrumentation Costs

Figure 3 shows using HPCViewer from the HPCToolkit to view instrumentation costs. The scope column represents individual functions. The dyninst_instrumentation_op represents a summary placeholder for instrumentation. In this example, we can see that instrumentation costs 7.5% of the total cycles.

Underneath the instrumentation placeholder, there are instrumentation costs attributed to different call paths. Source line 553 in function bt_skip_func incurs 1.4% instrumentation overhead, while source line 530 incurs 0.5% instrumentation overhead.

Binary rewriting application researchers can pinpoint the source of costs and design optimizations.

6 Optimizing Binary Rewriting Applications

We show how to use instrumentation profiling, static binary analysis, and multi-version instrumentation to improve shadow stack and block coverage.

6.1 Shadow Stack

For shadow stack, our instrumentation requires a slot for the shadow stack pointer (%gs: 0x0) and at most two slows for two scratch registers (%gs: 0x8 and %gs: 0x10). Memory locations after %gs: 0x10 are used for the shadow stack.

The push and pop operations mirror regular call stack operations. To support C++ exceptions and setjmp/longjmp, we repeatedly pop the values from the stack until a match or an under-flow occurs. Listing 1 shows the instruction sequence for push. The pop is similar (though with the loop).

As per Listing 1 the instruction sequence for a push consists of 9 instructions and 6 memory accesses. The pop operation incurs a similar overhead leading to about 20 instructions and 12 memory accesses per function call from shadow stack instrumentation. We use this instrumentation sequence as the baseline for shadow stack.

Figure 3. Instrumentation costs incurred at different program locations shown in HPCViewer.
6.1.1 Safe Function Elision. We use static binary analysis to determine whether a function is “safe” regarding return addresses and elide instrumentation for safe functions. Memory writes to global variables and stack variables within the current function frame (such as stack writes for spilling registers) are safe. If a function and all of its callees contain only safe memory writes, we do not instrument such function. For indirect calls, as we cannot statically determine its targets; we conservatively treat any function that may reach an indirect call as unsafe.

6.1.2 Dead Register Chasing. The basic shadow stack push and pop each need two GPRs as scratch space. It is a well-known strategy to leverage register liveness analysis to identify dead registers. We can avoid register save and restore if the scratch register is dead.

We observe that we can move our instrumentation to realize more dead registers compared to fixing our instrumentation at function entry and exit. For example, in Listing 2 if we instrument at the function entry, %rbx and %r10 are live because their values are then pushed to the stack. If we move our shadow stack push operation after the push instruction sequence, we have two dead registers. In this scenario, we need to adjust the offset for retrieving return address from the stack as we have pushed two GPRs to the stack. We call this technique dead register chasing. Currently, we only move instrumentation within the same basic block and we cannot move instrumentation beyond unsafe memory writes or unsafe function calls.

6.1.3 Leaf Function Optimization. Our profiling shows that in many cases, top hot functions are leaf functions. Instead of storing the return address to the shadow stack, we use a free register to implement a register stack frame. Listing 3 shows an example of a register frame push operation.

6.1.4 Profile-Guided Inlining. We use call path profiles to guide binary function inlining. We mainly attribute instrumentation costs to a pair of the call site and the corresponding callee, and perform inlining from the most expensive call sites until we cover 99% of the instrumentation costs. We handle two special cases. First, call site attribution is not sufficient to determine whether cascaded inlined should be done. Suppose we have three functions A, B, and C, where A calls B and B calls C. In addition, the call site data tells us to inline C into B and inline B into A. When we inline B into A, should we just inline the original B (without C) or inline the modified B (including C)? If the call paths associated with costs of B calling C do not include A, then there is not need to inline C into A as the the cost of B calling C is not incurred when A calls B; otherwise, we should also inline C into A.

Second, it is possible that a call site and callee pair does not match. Suppose A calls B, and B tail calls C. When we take a sample in C, as B performs tail calls into C, there is no stack frame or return addresses in B. So, the call paths will look like that A directly calls C. For such unmatched call sites and callees, we skip them.
6.2 Block Coverage

We use the block coverage implementation described by Khadra et al. [5] as the baseline. We re-implement their approach with Dyninst to avoid overhead differences caused by the binary rewriting tool.

6.2.1 Thread Local Instrumentation Data. The baseline implementation allocates static global memory to store coverage information. The advantage is that instrumentation can be achieved with a single instruction using PC-relative addressing: movb 1, %rip:off. This instruction pattern is also used for other instrumentation tasks, such as counting execution frequency of functions [38]. We find that this instrumentation strategy will cause prohibitively overhead when running multi-threaded programs, and the overhead will deteriorate with more threads. We observed over 10X slowdown when using 8 threads.

The root cause was quickly revealed when we profile it. We observed that instrumented code incurred a few times more last level cache misses than the uninstrumented code. This points to the false sharing of the cache lines for the global memory used to store coverage information, where different hardware threads may constantly write to the same cache line, causing this cache line to be invalidated on other cores.

To mitigate this problem, we store coverage information in the alternative stack region described in Section 5.2, though we do not treat the memory region as a stack in this case. A single instruction, movb 1, %gs:off, can write coverage information to the alternative stack region. We union the coverage information at the end of the execution to derive the coverage information for the process.

6.2.2 Profile-Guided Instrumentation Data Allocation.

We then observed a performance problem with regard to the order of coverage data allocation. In Listing 4, we have two functions, whose function entries are instrumented. We call the instrumentation at the entry of A (B) as IA (IB).

Our profile shows that IA is a hot spot, which takes \(1.0 \times 10^6\) cycles. In addition, the call stacks of the samples for IA show that all the cost by IA come from the call site at address 0xb6effd inside B. Therefore, A should have the same execution frequency as B. However, our profile shows that IB only takes \(5.3 \times 10^7\) cycles, which is half of what IA takes. Since IA and IB executed similar amount of time and both have the similar instruction (a memory write), we concluded that IA is suffering from cache related problems. It turned out that when we allocate which byte in the instrumentation data region to store coverage information for which basic block, we (and existing work) just allocate one byte at time sequentially based on the processing order of the code, which is typically in increasing order of the starting address of basic blocks.

| A: | # Instrumentation A takes 1.0 X 10^8 cycles |
|---|---|
| # Call stacks for all samples include B |
| 0xb416290: mov 0x8(%rdi),%rdx |
| 0xb416294: test %rdx,%rdx |

| B: | # Instrumentation B takes 5.3 X 10^7 cycles |
|---|---|
| 0xb6eff0: sub $0x8,%rsp |
| 0xb6eff4: mov %edi,%esi |
| 0xb6eff6: mov 0x61701b(%rip),%rdi |
| 0xb6effd: callq 416290 <A> |
| 0xb6f002: add $0x8,%rsp |
| 0xb6f006: retq |

Listing 4. A performance problem in code coverage instrumentation revealed by performance analysis.

In this case, IA writes coverage information for basic block at 0xb416290 while IB writes coverage information for basic block at 0xb6eff0. So, the IA and IB are writing to memory location separated by many cache lines. Each time when B calls A, we will first access to one cache line for IB and then immediately access to another cache line for IA. So, there is no cache line reuse between IA and IB.

To address this issue, we design a profile-guided coverage data allocation scheme. We rank all function call pairs X and Y based on the costs attributed to function X calling Y. From the highest pair, we try to allocate coverage data for X and Y as close as possible. This way, high overhead pairs will enjoy better data locality.

6.2.3 Profile-Guided Loop Cloning. As described in Section 4.2, idempotent instrumentation such as block coverage can benefit from loop cloning to elide instrumentation. We attribute instrumentation costs to the basic blocks and rank them in decreasing order of their costs. We go through the ranked list and add a block to perform clone if its belonging loop contains fewer than K blocks to clone. Empirically, we set K = 5, so we make at most 32 copies for a loop. We skip basic blocks that are not in any loop.

6.2.4 Sampling Skid. As each instrumentation point contains only one memory write instruction, the sampling skid of performance events may seriously distort where the instrumentation costs come from. Sampling skid refers to the delay between where a performance event happens the signal delivery to the performance tool. For code coverage instrumentation, the skid can cause instrumentation costs to be attributed to original code. In some cases, we have seen all costs incurred by instrumentation are attributed to original code, which defeats the purpose of profiling analysis of instrumentation and profile-guided instrumentation.
Table 1. Shadow stack and block coverage results.

|                | Time overhead | Size increase |
|----------------|---------------|---------------|
|                | max | mean | max | mean |
| empty          | 1.0%| 0.20%| 101.53%| 64.27%|
| SS-base        | 31.0%| 7.6%| 141.4%| 81.0%|
| SS-static      | 13.3%| 3.1%| 119.0%| 73.8%|
| SS-inline      | 10.0%| 1.4%| 126.2%| 78.5%|
| BC-base        | 1495.4%| 161.3%| 114.6%| 76.4%|
| BC-thread      | 51.1%| 9.8%| 126.5%| 77.7%|
| BC-loop        | 14.0%| 5.9%| 1813.8%| 145.0%|
| BC-data        | 12.1%| 4.0%| 1813.8%| 145.0%|

Vendors provide hardware support to mitigate sampling skid, including Intel’s precise event-based sampling (PEBS) and AMD’s instruction-based sampling (IBS). However, recent studies have shown that these “precise” sampling technologies may still be imprecise [41, 43].

In our case, profiles collected using Intel’s PEBS for block coverage enabled us to identify the data allocation problem described above, and are effective for performing profile-guided instrumentation. It is an interesting future research topic to see whether a sophisticated handling of sampling skid can yield better results.

7 Evaluation

We evaluate our implementation with SPEC CPU 2017 and two real world software.

7.1 SPEC CPU 2017

We are able to compile and run 19 of the 20 available benchmarks. 627.cam4_s does not compile on any of the systems, so is excluded. 8 of the 19 benchmarks are written in Fortran or have Fortran components. The other benchmarks are in C/C++.

All profile-guided versions utilize the training workloads in SPEC CPU 2017, which are different from the reference workloads that are used for reporting the results. Some benchmarks provide multiple training workloads. For these benchmarks, the final profiles are the aggregation of the individual profiles.

We run all instrumentation versions 10 times using 8 hardware threads and use the selected runs by SPEC CPU 2017 to compute overhead. Table 1 shows the result summary. The empty shows the overhead of instrumenting every basic block with empty instrumentation and represents the tool overhead caused by incremental CFG patching [24].

7.1.1 Shadow Stack. We compare three versions: SS-base represents a baseline binary level shadow stack implementation, where we instrument every function entry and exit with the baseline instrumentation sequence shown in Listing 1; SS-static represents an improved shadow stack implementation using static binary analysis to elide instrumentation of safe functions, leaf function frame optimization, and dead register chasing; SS-inline is SS-static with profile-guided binary function inlining. The experiments for shadow stack are done on an AMD EPYC 7402 server, which has 512GB memory and runs Red Hat 8.3. We use the system default compiler gcc-8.3.1. Profile data is collected with CPU timers.

Overall, we can see that SS-static significantly reduces runtime overhead compared to SS-base, showing that static binary analysis and careful instrumentation instruction sequence designs are two power weapons to optimize binary instrumentation applications. Equipped with call path profiling, users can identify to where to pay attention. SS-inline cut the average overhead by half compared to SS-static, showing that profile-guided inlining is a useful for optimizing binary instrumentation.

Next, we dive into the results of three benchmarks to better understand the capability of profile-guided inlining. One of the most successful benchmark for SS-inline is 620.omnetpp_s, which is written in C++. Our profile shows that an indirect function call, which implements a virtual function call, incurred the most costs. And almost all costs of this indirect call site goes to a single function. The combination of indirect call promotion and function inlining can eliminate most of the costs. It is often challenging for static binary analysis to analyze indirect calls. SS-static incurred 10.6% overhead for this benchmark and its overhead was reduced to 3.9% with SS-inline.

SS-inline incurred the highest overhead with 600.perlbench_s. Its overhead is centered around an indirect call that serves as a dispatcher to call different interpreter operations. This indirect call can go to over 60 different functions. It returns the next operation to invoke and is executed inside a small loop repeatedly that fits in a single cache line. We observed that when attempting to promote more than 5 indirect call targets for this indirect call, instruction cache pressure will make performance worse than without any inlining.

The call site profile for 602.gcc_s exhibits a long-tail distribution, which means that we have to inline much more code for this benchmark to cover instruction. We find that the net effect of binary function inlining is negligible compared without inlining.

7.1.2 Block Coverage. For block coverage, we compare four versions: BC-base represents a baseline of binary-level block coverage implementation [5]; BC-thread represents the version that store coverage information in thread local memory; BC-loop represents BC-thread with profile-guided multi-version loop instrumentation; BC-data is BC-thread with profile-guided coverage data allocation. The experiments are done on an Intel(R) Xeon(R) CPU E5-2695 server,
which has 128GB memory and runs Red Hat 7.9. We use a gcc-7.3.0 built by the system admin as the system compiler for Red Hat 7.9 is gcc-4.8.5, which is too old. Profile data is collected with the PEBS cycle counter to mitigate the sampling skid.

BC-base suffers from false sharing, incurring over 100% overhead on average. BC-thread stores coverage information in thread local memory regions, thus avoiding false sharing. BC-base and BC-thread have similar overhead numbers for benchmarks that do not use multi-threading. BC-thread incurs slightly higher size overhead as the instruction that writes a memory location related to %gs is two-byte longer than the instruction that is PC-relative.

BC-thread incurred highest overhead, 51.1%, with 644.nab_s. BC-1-loop and BC-data reduced the overhead to 10.0% and 3.7%, respectively.

BC-1-loop and BC-data have the same size overhead as BC-data only reorders instrumentation data allocation. Both incurred over 18X binary size increase for 648.exchange2_s. This dramatic size increase is caused by making copies of loops that are over a few KB in size. The net effect is that BC-1-loop does not reduce overhead for this benchmark compared to BC-thread.

7.2 Real World Software

We also evaluated shadow stack and block coverage instrumentation using two real world software: Apache HTTP Server and Firefox. The experiments were done on the Intel system mentioned above.

7.2.1 Apache HTTP Server. We compiled httpd-2.4.43 and instrumented the server executable httpd. We used the provided benchmarking program ab to measure instrumentation overhead by transferring a 595KB HTML file 100,000 times. We collect call path profiles by transferring the same file, but only 10,000 times. The experiments were repeated 20 times.

For shadow stack instrumentation, SS-base caused 18.4% throughput reduction and 22.3% latency increase; SS-static improved these numbers to 10.7% throughput reduction and 12.0% latency increase; SS-inline performed the best, causing 3.3% throughput reduction and 3.6% latency increase.

For block coverage instrumentation, all versions incurred negligible overhead.

7.2.2 Firefox. We used the Firefox shipped with Red Hat 7.9, which is 78.4.0. We instrument the libxu.so library in Firefox. This library is the main component of Firefox and its .text section is over 100MB in size.

To our surprise, none of our profile-guided instrumentation for shadow stack or block coverage can reduce instrumentation overhead, even when we collected profiles using the same benchmarks for testing.

The idea of multi-version binary rewriting centers on creating multiple copies of code to elide instrumentation, which increase the code size. If the root cause of binary instrumentation overhead are data accesses, multi-version binary rewriting can be beneficial. However, if the root cause of instrumentation overhead is related to instruction fetching, multi-version binary rewriting will not be helpful.

For Firefox, when we replaced the actual instrumentation with nops in the same length, we found that the nop instrumentation incurred similar overhead as the actual instrumentation. The nop instrumentation causes no additional data accesses but has the effect on instruction cache as the original instrumentation. This confirms that the instrumentation overhead for Firefox is instruction fetching related.

We also found that for libxu.so, even after dominator analysis, we need to instrument over 2 million basic blocks. Each memory write instruction in BC-thread is 9-byte long. So the instrumentation increased the code size by over 18MB! The profiles for Firefox also exhibited long-tail distributions. These two factors together explains why instrumentation overhead for Firefox is mainly caused by instruction fetching.

While it is disappointing, we believe this “negative” result and our analysis above are beneficial for understanding the scenarios where our new techniques can be useful.

8 Discussion

Last Branch Record: Recent studies on PGO [18, 27, 28] utilize the last branch records (LBR) provided by Intel to extract execution counts of control flow edges. LBR has very limited availability on non-Intel hardware. Our work enables call path profiling for binary instrumentation, which can collect performance information utilizing timer interrupts and hardware performance counters, thus has a wider applicability. We note that our approach can also be improved by incorporating LBR when available. We mentioned that call path profiling will miss functions performing tail calls, which can potentially be captured by LBR.

Application Specific Issues: From binary rewriting application researchers’ perspectives, there are other application specific issues to consider besides the instrumentation overhead. For shadow stack, the shadow memory region must be isolated from the original program, which is an important but orthogonal research area [9, 31]. There are also concerns on cross-thread attacks [42]. For code coverage, edge coverage may reveal more information compared to block coverage [45]. Our message is that by showing we can improve two typical binary rewriting applications in conventional settings, our can benefit binary rewriting application researchers in other scenarios.

9 Conclusion

We have presented multi-version binary rewriting, a new technique for optimizing static binary instrumentation. We enabled call path profiling for static binary instrumentation, designed primitive binary transformation operations to
support complex binary transformation, and applied instrumentation performance analysis and profile-guided binary transformation to optimize shadow stack and block coverage, two typical binary rewriting applications. Our results of SPEC CPU 2017 benchmarks, Apache HTTPD Server, and Firefox show that our techniques work well on programs where the root cause of instrumentation overhead is data accesses, and point out future research direction for designing optimization strategies to reduce instrumentation overhead caused by instruction fetching issues.

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