Pixel Detectors ... where do we stand?

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Abstract

Pixel detectors have been the working horse for high resolution, high rate and radiation particle tracking for the past 20 years. The field has spun off into imaging applications with equal uniqueness. Now the move is towards larger integration and fully monolithic devices with to be expected spin-off into imaging again. Many judices and prejudices that were around at times were overcome and surpassed. This paper attempts to give an account of the developments following a line of early prejudices and later insights.

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1. Introduction

Pixel detectors have entered particle physics experiments in the early nineties, first with small scale devices [1,2] and soon after with developments of detectors with $10^8$ pixels for the LHC experiments (see e.g. [3]). Despite early approaches with monolithic devices [4, 5, 6] so-called hybrid pixels in which pixel sensor and readout chip are separated entities, mated by employing bumping and flip-chipping technology, have been the technology of choice, in particular for applications in high rate and radiation environments [7] as at the LHC. Soon after also developments targeting imaging applications, in particular biomedical and synchrotron light X-ray imaging [8, 9] have been started, commencing their own development branches. As of today these development have culminated in very successful large scale detectors in the LHC experiments [10, 11, 12, 3] on the one hand and in imaging detectors on the other [13, 14, 15].

A bit later though, monolithic pixel detectors also reached a state of performance that made them attractive for particle and heavy ion physics experiments where low material budget plays an overwhelming role due to the low average momenta of particles emerging from the interactions. Fully monolithic pixel detectors where realised in the STAR experiment at RHIC [16] and a follow-up 10 m² detector is in production for the ALICE Inner Tracker ITS [17]. Also for the extreme radiation and rate environment encountered at the HL-LHC so-called depleted monolithic active pixels (DMAPS) have been developed [18, 19] that are able to cope with them (section 4). As was the case for hybrid pixels monolithic imaging devices are also spinning off, targeting X-ray and synchrotron radiation applications in astrophysics, biomedical imaging, and spectroscopy. This conference has devoted an integrated workshop on SOI-pixels in particular addressing such applications [20].

Early prejudices. In order to put the developments into some perspective I have chosen to follow a personal line of some early thinking and prejudices on pixel detectors, in particular those developed for LHC rate and radiation levels. Such statements are for example:

- Radiation levels at LHC and HL-LHC are tough for pixel sensors; and there is no alternative to planar pixels.

- Diamond will never become a material suited for a pixel tracker.

- The bulk material choice has to be p-type.

- Pixel sensors from CMOS IC fabrication lines do not have sufficient performance in terms of charge collection and radiation tolerance.
- A complex chip with $o(10^9)$ transistors can only be done by industry, needs many years of development, and is too expensive. However, as the 250 nm technology was already radhard, the 65 nm technology will be even better.

- Only hybrid pixel designs can cope with LHC conditions. Monolithic pixels will never stand the LHC rate and radiation environment.

- SOI pixel technology is fine, but it is extremely difficult to get around the many challenges of shielding sensitive structures.

- Silicon micropattern detectors are good for spatial resolution, but not for timing.

Much of this early thinking was wrong or has been overcome today as will be addressed in this paper.

2. Pixel sensors in high radiation environments

N- or p-type bulk. Apart from rate capability the required radiation tolerance is the dominant issue to cope with in most high energy physics experiments today. At the HL-LHC every Si lattice cell will see about 50 particles during its lifetime. The recipe developed over the years has been (i) readout at n$^+$ electrodes (e$^-$ collection), (ii) operation at high bias voltages, (iii) a careful planning of the annealing scenario, (iv) proper electrode and guard ring design, and recently (v) to use p-substrates with n electrodes (rather than n-in-n). While there is empirical evidence for the latter [21] it became evident that details of the electrode structure and sensor thickness complicated the issue [21]. Only recently p-type silicon as a sensor material has been studied in some detail. Bombardment with hadrons (p,n,π) causes damage to the silicon lattice which is independent of the type of doping. However, the effective doping concentration changes due to different effects. While in n-type silicon shallow donors (like phosphorus) are removed when a V-P complex is formed, the acceptor (boron B) abundance seems to be dominantly decreased by an interstitial B,O$_2$ complex [22,23], decreasing the negative space charge of the bulk. For n-type material a practical and efficient mitigation has been invoked by oxygen enrichment having VO complexes competing with VP. For p-type material such an efficient cure still has to be established [24].

Therefore, while for LHC upgrades the change from $p^+ – in – n$ to $n^+ – in – p$ for LHC experiment upgrades is necessary for strip detectors, from the radiation point of view, $n^+ – in – n$ (present pixel choice) is equally suited at least, except that for the fabrication of the latter double sided processing is needed. Hence strip and hybrid planar pixel sensors for the HL-LHC upgrades both plan on employing p-type substrates. For planar pixel detectors fig. 1(a) shows the cross section developing from the current $n^+ – in – n$ LHC pixels (250–300 µm) to thin $n^+ – in – p$ pixel sensors (100–150 µm); fig. 1(b) shows their performance under extreme radiation damage. Note in fig. 1(a) that the readout chip (ROC) must be placed in very close distance to parts of the sensor being under high voltage potential. Special isolation protection must be applied.

3D pixel electrodes. Very high fluences have imposed a real threat to standard pixel detector designs using planar electrodes, coped with only by thin sensors and high bias voltages (see previous section). Alternative pixel electrodes have been proposed and developed since the late 1990s [25,26] as so-called 3D-silicon sensors featuring columnar electrode implants driven into the Si substrate perpendicular to the sensor surface (fig. 2). The smaller electrode distance than sensor thickness renders shorter drift distance and higher fields at moderate bias voltages, together resulting in an increased radiation tolerance.

Within the ATLAS IBL detector 3D-Si pixel sensors have been proven to operate well in a running experiment [29]. After two years of operation the performance of 3D-Si pixel modules in terms of operation charac-
Diamond pixels. Diamond has been considered the material for radiation hard pixels due to (a) its large band gap switching off any leakage current and (b) its twice as high energy kick-off threshold (43 eV) to remove an atom from the lattice compared to Si, mitigating lattice damage at a given fluence. However, manufacturing and cost issues in producing single crystal sensor grade material (scCVD) as well as charge collection performance and other systematic issues associated with the grain structure of polycrystalline (pCVD) diamond, have so far prevented diamond pixels to become real tracking devices in an experimental arrangement. However, large progress has been made in developing ‘quasi tracker’ like detectors, as for example the ATLAS Diamond Beam Monitor (DBM) consisting of four 3-layer telescopes arranged symmetrically around the beam at small forward and backward angles (see also [35]). An efficiency map [36] exhibiting also the grain structure is shown in fig. 3(a). With a mean overall efficiency of 87.6% and remaining inhomogeneities due to the grain boundaries in pCVD, the demands on a stand alone tracking device for individual particles are not yet sufficiently met. For applications, however, where robustness of response and radiation immunity (e.g. for beam monitors) plays a larger role, pCVD diamond is a suitable choice.

The 3D technique can in diamond be realized by laser drilling sub-micrometer resistive holes [37, 35]. A diamond 3D assembly is shown in Fig. 3(b). With 150 µm² cell size a signal of 13 500 e⁻ corresponding to a charge collection distance CCD > 350 µm was measured with 92% column efficiency [35].

Sensors fabricated in CMOS production lines. In the past high ohmic pixel sensors were fabricated by dedicated sensor production vendors. Employing high

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**Figure 2:** 3D-Si sensors: (a) Than 3D-Si design optimized for HL-LHC (adapted from [27]) with two top view sketches for 50 × 50 µm² and 25 × 100 µm² pixel sizes, respectively [28]. While the p⁺ columns are deep etched through to a handle wafer, the n⁺ columns stop about 15 µm short. (b) Hit efficiency as a function of bias voltage for different fluences and design variants [29].

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**3D-Si design for HL-LHC**

**Performance**

![Diagram](image-url)
Figure 3: Diamond pixels: (a) Efficiency map obtained in a high energy test beam showing the grain structure of the substrate. The mean overall efficiency is 87.6%. (b) Assembled 3D device.

Figure 4: Hybrid pixel module using passive CMOS pixel sensors (schematic). Depleted sensor employing CMOS technology with 1-2 metal planes that can be used for (i) AC coupling and (ii) rerouting. These features are detailed on top. The yellow area in every pixel denotes the charge collection node. (b) Hit efficiency measured in 3.2 GeV electron test beams [38] as a function of bias voltage, before irradiation as well as irradiated for two fluence levels. Close to 100% efficiencies are achievable after a fluence of $1.1 \times 10^{15} \text{n}_	ext{eq}/\text{cm}^2$.

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throughput chip wafer manufacturers for sensor fabrication was believed to be too risky since the HEP community is not a large market to receive sufficient attention, and that the sensor quality would generally be insufficient. On the other hand, a number of advantages are in reach as there are: (i) Large volume production lines with price and turn-around benefits, (ii) 8" or 12" wafer sizes, (iii) wafers can be purchased to come with solder bumps of mid-size pitch (150 µm), (iv) standardly available metal layers can be exploited for (a) AC coupling and (b) optimal line redistribution when connecting sensor to R/O chip, such that large and ganged pixels can be avoided (see fig. 4(a)).

The early conception is about to change as has been successfully demonstrated for strip [39, 40] and pixel sensors [38]. Measurements on passive CMOS pixel sensors, 100 µm and 300 µm thick, irradiated to fluences of $1.1 \times 10^{15} \text{n}_	ext{eq}/\text{cm}^2$ have shown lab and test beam performance at least equal to those of planar sensors fabricated in dedicated sensor production lines [38].
This is evident from fig. 4(b) where very high mean hit efficiency are reached for DC and particularly for AC coupled passive CMOS sensors bonded to the readout chip FE-I4 [41].

3. Pixel readout chip

Indeed, as said in the introduction, a large and complex readout chip with o(10⁹) transistors is a huge and costly enterprise which has been addressed by the RD53 collaboration at CERN [42]. In comparison to the chips of the previous hybrid pixel generation which were column drain architectures without (1st generation) or with (2nd generation) a local (4-pixel) cluster efficient hit storage, this 3rd generation contains architecture blocks with grouped logic enabling regional hit draining surrounded by synthesized logic, dubbed the ‘digital sea’ [43] and [44].

Regarding radiation it seemed that the 250 nm and 130 nm technologies have hit a sweet spot. The naive belief that smaller deep submicron technologies would be even more radhard neglected radiation induced narrow/short channel effects (RINCE and RISCE, respectively, Fig. 5(b)) as is detailed by F. Faccio’s presentation at this conference [45].

4. Monolithic Pixels

The many advantages of hybrid pixel detector face some serious drawbacks, among them the material budget and the laborious assembly of the hybrid parts. In recent years monolithic pixel approaches have strongly emerged, first by employing CMOS imaging technologies leading to so-called MAPS devices with charge collection by diffusion in the chip’s epitaxial layer [5, 6]. This technology has also found its way into HEP experiments in need for low material budget and small pixel devices, but facing lower than LHC rates, such as RICH’s STAR experiment [46, 16] and culminating in the 10 m² pixel detector of the ALICE upgrade [17] (see also [7]).

It was believed for a long time that LHC rates and radiation levels were prohibitive for MAPS, but they could be addressed by monolithic pixels in special processes, featuring high voltage and high resistive wafers, multiple wells, and backside processing [18]. In the past four years this approach culminated in fully monolithic designs that can cope with the LHC radiation levels of above 10¹⁵neq.cm⁻² (fluence) and 1 MGy (dose) as well as the corresponding particle rates. For the HL-LHC they are thus suited at least for the outer pixel layers.
Two promising lines of actual research are currently followed: (a) large electrode designs (large fill factor, FF), where the electronics is embedded in the electrode covering a large fraction of the pixel area and (b) small electrode (small FF) designs where the collection electrode is set aside from the shielded electronics area (see also [47]). The pros and cons are obvious. While the large FF design provides short average drift distances and hence promises radiation hardness it suffers from a relatively large input capacitance to the amplifier, governed by its large area and, in addition, by the capacitance introduced between the deep p-well and the deep n-well. The latter also represents a coupling path between electronics and sensor such that transient digital signals coupling into the sensor must be prevented by dedicated circuitry. The small FF approach offers all the benefits imposed by the small (≤ 15 FF) input capacitance, suffers, however, from larger average drift distances for the same pixel area. A process modification [48] (see also [47]), strengthening the lateral drift by sideward depletion, improves the charge collection towards the small collection electrode.

Both approaches have been matured by intensive prototyping R&D leading to large (∼ cm²) fully monolithic pixel chips with full readout architectures suitable for LHC rates as shown in fig. 7. The large FF chips are under test, the small FF design is currently fabricated (see also [49]).

The main results for large FF devices are summarized in fig. 8. (i) Depletion depths in excess of 100 µm are reached even after 2 · 10^{15} n_{eq} cm^{-2} (fig. 8(a)); (ii) gain decreases and noise increases remain below 10% and 30%, respectively, after radiation doses of 1 MGy; (iii) the timing requirements after irradiation are close to being met after a correction; and (iv) the hit efficiency after 1 · 10^{15} n_{eq} cm^{-2} is still close to 99% at a noise occupancy of 10^{-7}.

SOI pixels. A full workshop within this conference is devoted to SOI pixels (see for example [20] and references therein). Mastering complex device variations in this so-called fully-depleted SOI technology the groups managed to fabricate powerful detection devices for many application areas: particle tracking with sub-µm resolutions (FPix and SOFIST), X-ray imaging (INTPIX), X-ray astro (XRPIX, SOPIX-PDD), synchrotron radiation (SOPHIAS), far infrared (cryogenic), biomedical counting (CNIPIX), and ion spectroscopy (MALPIX). A full account is given elsewhere at this conference. Previously existing issues like the back-gate effect, coupling between circuit and sensor, and radiation (TID) issues have been cured by several variants of buried well and nested well arrangements. The present devices are radiation hard to TIDs of 100 kGy.

Regarding SOI pixels for LHC radiation levels, it should be mentioned that promising prototyping has been done [51] using partially depleted SOI, for which the back-gate and other effects do largely not exist due to shielding wells in the electronics layer.

5. Fast timing with pixels

Sub-ns to ps timing was believed to be very difficult with silicon detectors. So-called low gain avalanche diodes, having mm² size patterns, have been developed to cope with this challenge (see also [52] and [53]). In order to minimize time fluctuations in the signal generation process, an amplification structure is realized by a p⁺ implantation right underneath the n⁺ electrode (fig. 9(a)). The fast signal is governed by fast e/h movements in high fields of thin detectors plus large slew rates (dV/dt) from amplified holes moving away from the readout electrode [54]. Gains below 50 are targeted in order to avoid amplification excess noise. The structure needs a homogeneous weighting field such that small pixels are not easily realized.

The time resolution has several contributions [59]:

\[ \sigma_t^2 = \left( \frac{V_{th}}{dV/dt_{th}} \right)^2 + \left( \frac{\text{Noise}}{dV/dt} \right)^2 + \sigma_{\text{arrival}}^2 + \sigma_{\text{dist}}^2 + \sigma_{\text{DD}}^2 \]

The terms represent time walk, noise jitter, non-uniform charge depositions along a track, position dependent signal distortion, and digitisation. The first two contributions can be made small when large slew rates are achieved.
Figure 8: Performance of depleted MAPS: (a) Measured depletion depth as a function of bias for various irradiation levels (LFoundry 150 nm) [50]. (b, top) Appearance of hits in bunch crossing time bins (AMS 180 nm); (b, bottom) hit efficiency (LFoundry 150 nm), both after $10^{15}$ n$_{eq}$ cm$^{-2}$.

Figure 9: Low gain avalanche diodes are capable to provide high time resolutions. (a) LGAD structure featuring a high ohmic p-type bulk, and an amplification junction (adapted from [55]). The electric field is sketched on the left. (b) Comparison of time resolutions from simulations (WF2) and from test beam measurements. Data points from [55, 56, 57, 58], and [59].

The results of this R&D are encouraging as shown in fig. 9(b) comparing data and simulations as a function of sensor thickness. In ATLAS and CMS proposals exist to employ LGADs for some timing applications for the HL-LHC upgrade. The main concern currently is the radiation tolerance since the gain varies strongly with radiation fluence due to acceptor removal in the relatively highly doped p$^+$ layer of the multiplication region.

6. Imaging with Hybrid Pixels

As mentioned in the introduction, the hybrid pixel developments made for particle tracking shortly afterwards entered X-ray imaging for biomedical (e.g. MEDIPIX [60]) or synchrotron light applications (see also [61]). The first big detectors addressing signals with huge dynamic range (1 - $10^5$) have come into live. Examples are among others the series of developments at PSI called EIGER (500 k pixels, 75 µm pitch, photon counting, 23 kHz frame rates), MÖNCH (charge integrating, 25 µm pixel pitch, low noise, low energies) [62], and JUNGFRAU (charge integrating, 75 µm pixel pitch, dynamic gain switching) [63] for the SLS and for SWISSFEL, with which a step function in synchrotron light imaging is achieved. For the EUROPEAN XFEL first pictures of the adaptive gain imaging pixel detector AGIPD [64] have been recorded.

Also in imaging applications monolithic pixels are now taking an important role, as can for example by
seen be the 'Double SOI' pixel detector presented at this conference [63].

7. Conclusions

Pixel detectors have paved the way of high resolution, high rate, and high radiation devices indispensable from particle tracking and imaging experiments. The path first laid by hybrid pixel detectors is now followed into monolithic devices and devices tuned for high timing resolution, at first again for tracking. For sure imaging applications will follow.

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