A reliability study of Non-uniform Si TFET with dual material source: Impact of interface trap charges and temperature

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Research Article

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Abstract

The article reports the extraction of DC characteristics and small signal parameters of Non-uniform Si TFET with dual material source (NUTFET-DMS) at different frequencies followed by its reliability investigation. The reliability of the device is examined by analysing: 1) the impact of the presence of interface trap charges, 2) the impact of temperature variation (200 K - 400 K). In the analysis it has been observed that in case of absence of interface trap charges the increase in frequency reduces the value of parasitic capacitances. In addition, the presence of interface trap charges lessens the value of parasitic capacitances up to a certain gate to source voltage after that it shows a reverse effect. Further, it has been perceived that the effect of change in temperature is more on device ambipolar current when interface trap charges are present, whereas the reverse is true in the case of OFF state current and different parasitic capacitances.

1. Introduction

Over the past decades, MOSFET played a very crucial role, however as devices scale down short channel effects of MOSFET dominated the platform. Hence, new alternative structures are on demand which can mitigate the drawbacks associated with MOSFET. One of the promising alternatives in place of MOSFET is the tunnel field effect transistor (TFET). It is reported that TFET has the ability to exceed subthreshold swing (SS) from the physical limit of 60mV/decade and have an extremely low leakage current because of its unique current conduction mechanism. The mechanism is called band to band tunneling, where electrons move from source valance band to the channel conduction band [1–4]. These advantages of TFET attracted the attention of a lot of researchers as a reliable contender for low power applications.

For low power applications maintaining the minimum SS is not sufficient, in this case, an average SS should be taken into consideration for $V_{dd}$ reduction [5–6]. Unfortunately, in TFET the value of SS increases for an increase in gate to source voltage, thus can not provide lower average SS, which can be generally explained by $(V_T-V_{OFF})/\log(I_T/I_{OFF})$ [5]. Further, limited ON current of TFET is another factor of concern. To overcome these problems, many new TFET structures have been proposed some are Double gate TFET [7], III–V-semiconductor-based TFET [8], SOI TFET [9], Carbon-based TFET [10], SG-ESTFET [11], etc. However, in the process of device optimization, it is a challenge to preserve all the parameters in a single device. In this case, [12] has proposed a non-uniform silicon TFET with a dual-material source to maintain lower average SS, the non-uniform body which increases the ON current and the compressed body of the drain side maintains a low OFF and ambipolar current too. The performance of the structure has been analysed in terms of various structural and material parameters in literature.

Counting the switching characteristics of device a detailed analysis of analog/RF parameters of the device needs to be investigated to know the perspective in the analog and digital applications. In literature, different parasitic capacitances are studied and it has been analyzed that the gate to drain capacitance ($C_{gd}$) is much higher than gate to source capacitance ($C_{gs}$), which limits the performance of TFET [13]. However when reliability of a device is concerned the above mentioned small signal
parameters along with DC characteristics need to undergo various situation where consistency of the device can be examined. Further, the temperature of the device plays a dominant role in device performance, as with the advancement in technology node number of transistors on-chip increases, which leads to large heat dissipation and change in the operating temperature of the transistors. It is observed that, the current conduction mechanism of TFET depends on band gap energy which is a function of temperature [15–16]. In addition, it is also articulated that the effect of temperature on device performance is more when interface trap charges are present [16]. Hence a detailed understanding of device parasitic capacitances and DC performance parameters need to be analyzed in the presence of trap charges as well as in varied temperature conditions. This work investigates the analog/RF analysis of the device in the presence of interface trap charges at various frequencies. Further, a temperature analysis of the structure has been executed for both DC and AC performance parameters. The paper is structured in four sections including introduction, the depiction of the device structure, and simulation methodology provided in Sect. 2. Section 3 explains the analysis of results and finally, Sect. 4 concludes the work in brief.

2. Device Structure And Simulation Methodology

Figure 1 shows the schematic structure of Non-uniform Si TFET with dual material source (NUTFET-DMS) [12] having p + source and n + drain regions. The entire device length is 60 nm. The thickness of the source is 15nm and the drain is 7nm each. The upper gate and lower gate are made up of aluminium and PolySi, respectively. The dielectric material for the upper, lower gates is HfO2 in the source side and SiO2 in the drain side, respectively.

Sentaurus TCAD has been used to simulate the structure. Fermi-Dirac statistic transport model has been used for the incorporation of high doping concentration and the doping dependent mobility model is used for the resulting mobility of the device. Non-local BTBT model has been activated at each mesh point of the tunneling region to consider the generation of carriers and the basic operation of TFET. Bandgap narrowing model is enabled to reduce the semiconductor bandgap. Shockley-Read-Hall (SRH) recombination model is used for the recombination of carriers [17]. The simulation models mentioned above is tested and calibrated with the experimentally validated structure of [18]. The appraisal among drain current characteristics of the structure are shown in Fig. 2, the adjacency between the current characteristics demonstrates the validity of the models used. In addition, the performance of the device has been analysed by considering the fluctuation of temperature from 200K to 400K. Finally, the presence of both uniform and Gaussian distribution of trap charges of varying concentration is incorporated at both the semiconductor-insulator interface. Different interface trap charge distribution parameters for simulation of NUTFET-DMS are indicated in Table I.

Table I: Typical values of various parameters of trap charge allocation:
### Table 1

| Parameter | Explanation | Values |
|-----------|-------------|--------|
| \( N_0 \) | Concentration of trap charge in Gaussian and uniform distribution. | \( 1 \times 10^{13}/\text{cm}^3 \) to \( 1 \times 10^{14}/\text{cm}^3 \) |
| \( E_0 \) | Energy Mid for Gaussian distribution | 0 eV |
| \( E_S \) | Energy Sig for Gaussian distribution | 0.1 eV |

### 3. Results And Discussion

#### 3.1 Impact of trap charges on small signal parameters of NUTFET-DMS:

In this module, the effect of trap charges on different capacitances of NUTFET-DMS is explored. The capacitances among different pairs of electrodes viz. source, drain, and gate are calculated at various frequencies in the presence and absence of trap charges. Figure 3(a) and 3(b) show the variation of \( C_{gd} \), \( C_{gs} \), and \( C_{gg} \) vs. gate to source voltage of the device for the absence of trap charges. In TFET as the inversion layer is connected to the drain side even at the higher drain to source voltages the \( C_{gd} \) contribution in total capacitance \( C_{gg} \) is more, which limits the performance of the device. But the device presented in this work has reduced the value of \( C_{gd} \) in comparison to other structures, which is for the sake of the low-K dielectric near drain side of the device for both front and back gates [19]. From Fig. 3(a) it can be observed that the value of the \( C_{gs} \) remains comparable to \( C_{gd} \) up to a higher value of gate to source voltage (Vgs) (near 0.7 V) but later \( C_{gd} \) dominates. It can be observed that the value of capacitances (\( C_{gs} \), \( C_{gd} \) and \( C_{gg} \)) decreases with an increase in frequency this is because of the inverse relation between capacitance and frequency. Figure 3(c) reports the cut-off frequency \( (f_T) \) of the device, at 10 GHz signal frequency the \( f_T \) of the device rises as compared to the case of 10 MHz. This is because of the increased \( C_{gg} \) value at 10 MHz, as

\[
f_T = \frac{g_m}{2\pi C_{gg}},
\]

where \( g_m \) and \( f_T \) are the transconductance and cut-off frequency of the device, respectively.

The plot of different capacitances of the device against gate to source voltage for the presence of trap charges is shown in Fig. 4. Two different frequencies have been considered to analyse the effect of presence of interface trap charges on parasitic capacitances at different concentrations. From Fig. 4(a) and 4(b) it can be observed that till Vgs = 0.7 V, \( C_{gs} \) dominates and the introduction of trap charges reduces the value of \( C_{gs} \), hence the value of \( C_{gg} \). This is due to the presence of trap charges at various interfaces which causes carrier fluctuations and reduces the effect of drain to source voltage.
It can be observed from Fig. 4(a) and (c) that for Vgs greater than 0.7 V, Cgd dominates Cgs, and the effect of trap charges gets reversed. In addition, as the concentration of trap charges increases the value of Cgd increases which is due to the higher e-density at higher values of Vgs. At higher values of Vgs the rising Fermi level and the effect of traps charges lead to a significant change in Cgd [21]. In addition, at very high Vgs and higher frequencies the capturing and emitting process of trap charges cannot track the AC signal which increases Cgd as compared to the case of no trap charges, thus results in more delay [20, 21]. Similarly, the same variation can be noticed in the case of total capacitance Cgg which can be observed in Fig. 4(b) and 4(d). Finally, it can be observed that the existence of the uniform trap distribution has less effect on parasitic capacitances as compared to the case of Gaussian trap distribution due to its lower rate of carrier fluctuations.

3.2 Impact of temperature on the performance of NUTFET-DMS:
The existence of interface trap charges and the effect of change in temperature fluctuates the sensitivity of the device which may cause severe complications for various sensing-based applications of the device. Hence, in this section, several DC and analog/RF performance parameters of NUTFET-DMS are analysed at various temperatures (200K-400K) considering the presence of trap charges with Gaussian and uniform types of distribution.

Figure 5 presents the drain current aspect of NUTFET-DMS at various temperatures including the existence of trap charges at the Si-insulator interface at 10MHz frequency. It can be noticed that, as the temperature increases the device OFF current increases, which is due to the dominancy of the SRH mechanism in the subthreshold region [22]. A change in OFF current in the order of 10–17 to 10–14 A/µm, 10–16 to 10–12 A/µm, 10–13 to 10–12 A/µm can be observed for no trap charges, uniform and Gaussian distribution of trap charges, respectively. It can be perceived that, temperature effect is prominent on the device ambipolar current, because of the introduction of gate-drain underlap which makes the ambipolar current dependent on TAT (trap assisted tunneling) and SRH [23]. However, in case of no trap charges, the effect of temperature on ambipolar current is less as compared to the case of presence of trap charges. The impact of temperature on ON current is less as compared to OFF and ambipolar current. This is because of less dependency of BTBT mechanism on temperature, a small increment can be observed which is because of the increase in the electric field.

Analysis of device parasitic capacitances considering the temperature effect and the presence of non idealities is very important for different analog and digital applications. In order to analyse the impact of temperature on parasitic capacitances, the Cgd, Cgs, and Cgg as a function of Vgs are examined under varied temperature conditions. In Fig. 6 parasitic capacitance vs. gate to source voltage characteristics of NUTFET-DMS are presented in the presence of interface trap charges, various temperatures at a frequency of 10MHz. It can be perceived that, with the increase in temperature Cgd and Cgs increase, which leads to an increase in Cgg for both presence and absence of trap charges. This is due to the decrease in potential at channel drain junction with the increase in temperature. Further, the presence of trap charges enhances the value of parasitic capacitances at higher temperatures. This is because when the temperature is increased, the thermal electron and tunneling effect get intensified which makes the
trap charges to capture or emit more charges. However, at various temperatures (200K to 400K) the percentage increase of $C_{gg}$ is 13%, 12%, and 10%, in case of $C_{gs}$ and $C_{gd}$ are 25%, 23%, 23%, and 12%, 10%, 9% for no trap charge, uniform, and Gaussian distribution of trap charges respectively. It is found that the effect of temperature is more on the device with no trap charges as compared to the case of the presence of trap charges.

4. Conclusion

In this work small signal analysis of Non-uniform Si TFET with dual material source (NUTFET-DMS) is performed at different frequencies. In addition, the reliability check of the device in presence of interface trap charges and varying temperature conditions in terms of DC and small signal performance parameters have been studied. It is observed that, in the absence trap charges the increase in frequency reduces the value of parasitic capacitances. Further the results show that, in presence of trap charges the values of $C_{gg}$, $C_{gd}$, and $C_{gs}$ reduces for an increase in gate to source voltage, but after attaining a certain voltage of 0.7V the values of these capacitances increase predominantly. Finally, it is found that the impact of temperature on OFF state current and different parasitic capacitances reduces when trap charges are present but increases in case of ambipolar current. The analysis provided in this article could be valuable for the design of different TFET at an unstable temperature environment and in the presence of non-idealities.

Declarations

CONFLICT OF INTEREST:

We do not have involvement in any organization or entity with any financial interest (such as honoraria; educational grants; participation in speakers' bureaus; membership, employment, consultancies, stock ownership, or other equity interest; and expert testimony or patent-licensing arrangements), or non-financial interest (such as personal or professional relationships, affiliations, knowledge or beliefs) in the subject matter or materials discussed in this manuscript.

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References

[1] A. M. Ionescu, H. Riel, Nature, 479, 7373 (2011).

[2] H. LU, A. SEABAUGH, Electron Devices Society, 2, 4 (2014).

[3] J. Knoch, S. Mantl, J. Appenzeller, Solid-State Electronics, 51, 4 (2007).

[4] A. M., N. M. Biju, R. Komaragiri, International Conference on Advances in Computing and Communications, 138-141. 10.1109/ICACC.2012.31.

[5] A. C. Seabaugh, Q. Zhang, Proceedings of the IEEE, 98, 12 (2010).

[6] H. Kam, T.-J. K. Liu, E. Alon, IEEE Transaction on Electron Devices, 59, 2 (2012).

[7] K. Boucart, A.M. Ionescu, IEEE Transaction on Electron Devices, 54, 7 (2007).

[8] M. Hellenbrand, E. Memišević, M. Berg, O. Kilpi, J. Svensson, L. Wernersson, IEEE Electron Device Letters, 38, 11 (2017).

[9] S.K.Mitra, R.Goswami and B.Bhowmick, Superlattices Microstruct., 92 (2016).

[10] Y. Gao, T. Low, M. Lundstrom, Symposium on VLSI Technology (2009), pp. 180-181.

[11] J. Talukdar, G. Rawat K. Mummaneni, Silicon, 2 (2020), https://doi.org/10.1007/s12633-019-00321-3.

[12] J. Talukdar, K. Mummaneni, Applied Physics A, 126, 81 (2020).

[13] S. Mookerjea, R. Krishnan, S. Datta, V. Narayanan, IEEE Electron Device letters. 30, 10, (2009).

[14] C. Liu, S. Glass, G. V. Luong, K. Narimani, Q. Han, A. T. Tiedemann, A. Fox, W. Yu, X. Wang, S. Mantl, and Q.T. Zhao, IEEE Electron Device letters, 38, 6 (2017).

[15] Y. P. Varshni, Physica, 34, 1 (1967).

[16] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, S. Datta, IEEE Electron Device Lett., 31, 6 (2010).

[17] TCAD Sentaurus Device User’s Manual, Synopsys, Inc., Mountain View, CA, USA, 2010.

[18] A. Biswas, S. S. Dan, C. L. Royer, W. Grabinski, A. M. Ionescu, Microelectronic Engineering, 98 (2012).

[19] C. Alper, L. De Michielis, N. Dag˘tekin, L. Lattanzio, D. Bouvet, A.M. Ionescu, Solid-State Electronics, 84, (2013).
[20] Z. Jiang, Y. Zhuang, C. Li, P. Wang, Y. Liu, Journal of Electrical and Computer Engineering, (2015), https://doi.org/10.1155/2015/630178.

[21] R. Goswami, B. Bhowmick, S. Baishya, Microelectronics Journal, 53, (2016).

[22] S. Chander, S. K. Sinha, S. Kumar P. K. Singh, K. Baral, K. Singh, S. Jit, Superlattices Microstructure, 110 (2017).

[23] P. G. D. Agopian, M. D. V. Martino, S. G. d. S. Filho, J. A. Martino, R. Rooyackers, D. Leonelli, C. Claeys, Solid-State Electronics, 78, (2012).

Figures

Figure 1
Non-uniform Si TFET with dual material source (NUTFET-DMS).

Figure 2
Calibrated Id-Vgs characteristics.
Figure 3

Capacitance vs. gate to source voltage characteristics of NUTFET-DMS (a) Cgs, Cgd, (b) Cgg, (c) cut-off frequency (fT) at 10MHz and 10GHz in absence of trap charges.
Figure 4

Capacitance vs. gate to source voltage characteristics of NUTFET-DMS (Vgs) at 10MHz and 10GHz in presence of trap charges for NUTFET-DMS (a) Cgs, Cgd (b) Cgg for Gaussian distribution, (c) Cgs, Cgd, (d) Cgg for uniform distribution.
Figure 5

Drain current vs. gate to source voltage characteristics of NUTFET-DMS for (a) no trap charges, (b) uniform distribution of trap charges, (c) Gaussian distribution of trap charges.
Figure 6

Capacitance (Cgs, Cgd, Cgg) vs. gate to source voltage characteristics of NUTFET-DMS (Vgs) characteristics of NUTFET-DMS for (a) no trap charges, (b) uniform distribution of trap charges, (c) Gaussian distribution of trap charges.