A self-rectifying memristor model for simulation and ReRAM applications

Sinan Sabah1, Nasri Bin Sulaiman2
1 Department of Electronic and Communications Engineering, University of Baghdad, Iraq
2 Departement of Electrical and Electronic Engineering, Universiti Putra Malaysia, Malaysia

ABSTRACT
In this paper, a self-rectifying memristor (SRM) model is proposed for memristive circuit simulations. This model is based on the behavior of voltage controlled, bipolar memristors that exhibit diode-like rectification behavior when reverse biased. Such unique feature can solve the sneak path problem in crossbar memristive memory structures without requiring additional cell selectors. The results show that the proposed model satisfies the basic memristor’s i-v characteristics and fits many different memristor devices adequately. The proposed model is implemented in Verilog-A so that it is conveniently incorporated into various memristor applications with different circuit simulators.

1. INTRODUCTION
The everyday growing usage of portable electronic gadgets and embedded systems is pushing the demands for smaller electronic devices with lower power consumption and higher memory density. However, the current CMOS technology is scarcely scaled to few nanometers due to higher leakage of tunneling currents, short channel effect, and difficult gate control [1]. Consequently, the electronic device market is demanding alternative technologies to satisfy the consumers. Over the past decade, several research groups have brought to light different emerging memory technologies [2]. However, the memristor-based memories have been identified as the leading competitive memory technology among the other candidates [3]. A memristor is a two-terminal passive device whose electrical resistance (referred to as memristance) depends on the magnitude and polarity of the applied voltage [4]. Regarded as the fourth basic circuit element, the memristor retains its memristance even if the signal is turned off. Besides its compatibility with CMOS technology [5], the hybrid CMOS/memristor circuits are smaller, faster, and consume less energy [6]. Memristors can fit into many analog, digital, memory, and even neuromorphic applications [7-8].

Despite that the first memristor is based on metal-insulator-metal structure [9], several binary oxide and perovskite oxide materials have been reported to act as resistive switches under an electric field [10]. Moreover, memristor electrodes are either fabricated from inert materials (e.g. Pt and Au) that serves as electrical contacts only, or active materials (e.g. Ag and Cu) that act as cation sources [5]. Therefore, several memristor models have been proposed to describe the behavior, dynamics, and applications of various structures [11]. However, these models are proposed to describe the behavior of linear memristors only and none of them is able to reproduce the i-v characteristics of the SRM devices [12]. The aim of this study is to propose a mathematical model for the voltage-controlled, bipolar SRM devices. The proposed model satisfies the basic memristor fingerprints and is flexible to capture the characteristics of different memristors.

Copyright © 2020 Institute of Advanced Engineering and Science. All rights reserved.
The remaining part of this paper is arranged as follows. In Section 2, a brief description of the reported bipolar SRM devices is introduced. Section 3 comprehensively describes the development of the proposed SRM model. A model validation process is presented in Section 4, followed by a conclusion in Section 5.

2. RESEARCH METHODS

In this section, a brief description of several SRM devices is introduced. Next, a state-of-the-art SRM device model is proposed by developing the two main memristive device equations required for device modeling.

2.1. Bipolar SRM devices

Several memristive devices that exhibit diode-like behavior have been reported. Kim et al. fabricated a bipolar memristor with Ag/a-Si/p-Si structure [13]. The Ag top electrode serves as a cation source that can change the conductivity of the a-Si layer depending on the polarity of the applied signal. Assuming that the device is initially in its low resistance state (LRS), a small negative bias causes a partial retraction of Ag cations, thus decreasing the memristor’s conductivity. The initial resistance state can be restored by applying a small positive voltage across the terminals. Furthermore, the switch state can only be changed to its high resistance state (HRS) if the magnitude of the applied bias exceeds a certain threshold ($V_{th}$). This structure is CMOS compatible and has a rectification ratio $>10^6$ and a reverse bias current below $10^{-13}$ A [5]. A similar rectifying behavior was also observed in other memristor structures such as TiN/HfO$_x$/Si [14], Cu/aSi/WO$_3$/Pt [15], Cu/Al$_2$O$_3$/a-Si/Ta [16], and gold nanocrystal-embedded ZnO$_2$ [17]. The intrinsic rectification behavior of these memristors is a promising feature that can be used to solve the sneak path problem in crossbar array memories [18].

2.2. The proposed SRM device model

Generally, a memristor device requires two main equations in order to be modeled. The first equation is a differential equation that describes the dynamics of change in the memristor's state. The second equation describes the relationship between the applied voltage and current. The device development process is shown in Figure 1. It consists of four basic tasks to be accomplished sequentially. The first and second tasks are related to the mathematical derivation of the state variable equation and $i$-$v$ relationship, respectively. The third task consists of a verification process to validate the memristor fingerprints and compliance with SRM experimental data. In the last task, a Verilog-A code is developed based on the memristor’s mathematical model.

![Figure 1. The development process of the proposed SRM device model](image)

2.3. State variable equation

The state variable derivative ($dw/dt$) is responsible for determining the memristance ($R_m$) according to the past history of the applied bias. Assuming that the device is voltage-controlled and the state variable ($w$) is unchanged unless the applied voltage ($v(t)$) exceeds a certain threshold. Moreover, it is

A self-rectifying memristor model for simulation and ReRAM applications (Sinan Sabah)
necessary to include a nonlinear dependence between the state variable and applied voltage. Under these assumptions, the proposed state variable derivative is a polynomial function determined by the following expression:

\[
\frac{dw}{dt} = \begin{cases} 
-k_{off} \left( \frac{v}{v_{off}} - 1 \right)^{a_{off}} \cdot f_{off}(w), & v \leq v_{off} \\
0, & v_{off} < v < v_{on} \\
k_{on} \left( \frac{v}{v_{on}} - 1 \right)^{a_{on}} \cdot f_{on}(w), & v \geq v_{on}
\end{cases}
\]  

(1)

where \(k_{off} \in \mathbb{R}^+\), \(k_{on} \in \mathbb{R}^+\), \(a_{off} \in \mathbb{Z}^+\), and \(a_{on} \in \mathbb{Z}^+\) are fitting parameters, \(v_{on}\) and \(v_{off}\) are high to low resistance and low to high resistance switching voltage thresholds, respectively. \(f_{off}(w)\) and \(f_{on}(w)\) are window functions that limit the value of \(w\) within the physical device boundaries \(w_{off}\) and \(w_{on}\). Note that the magnitude of the polynomial \((k_{off} \text{ and } k_{on})\) represent how quickly the memristor’s state changes once \(v\) surpasses the threshold voltage. This will help to simulate SRMs with different SET and RESET switching speeds [19].

Unlike the model presented in [20], the proposed model supports both symmetric programming voltage (i.e. \(v_{off} = -v_{on}\)) and asymmetric programming voltage (i.e. \(v_{off} \neq -v_{on}\)) for bipolar SRM operation. In addition, it allows for different OFF and ON switching times by adjusting the magnitude of the polynomial \((k_{off} \text{ and } k_{on})\) since a practical memristive device exhibits non-identical OFF and ON switching speeds [21]. Lastly, it improves the computational runtime by choosing lower value for \(a_{off}\) and \(a_{on}\) (yet such trend produces lower simulation accuracy).

2.4. Current-voltage relationship

As mentioned before, at any given instance of time, the memristor acts as a simple resistor of value \(R_m\) that comply to Ohm’s law. However, the value of \(R_m\) depends on the state variable obtained by computing (1). Then, the \(i-v\) relationship is given by the following expression:

\[
i(t) = R_m^{-1} \cdot v(t)
\]

(2)

According to the SRM behavior, the device exhibits a higher resistance state when reverse biased (i.e. \(R_m = R_{off}\) for \(v < 0\)). Moreover, the device acts as a normal switch of resistance \(R_m\) that can be any value between \(R_{off}\) and \(R_{on}\) depending on \(w\). On one hand, if \(w = w_{on}\) then \(R_m = R_{on}\) and the memristor is said to be OFF. As \(w\) moves away towards \(w_{off}\), then \(R_m\) starts to increase nonlinearly. On the other hand, if \(w = w_{off}\) then \(R_m = R_{off}\) and the memristor is said to be OFF. In accordance, \(R_m\) is given by the formula:

\[
R_m(w) = \begin{cases} 
R_{off}, & \text{for } (v(t) < 0) \\
R_{on} + \frac{(w - w_{on})}{(w_{off} - w_{on})} (R_{off} - R_{on}), & \text{for } (v(t) \geq 0)
\end{cases}
\]

(3)

3. RESULTS AND DISCUSSION

In this section, the proposed model is verified based on three aspects; memristor’s fingerprints, symmetric bipolar operation, and asymmetric bipolar operation.

3.1. Memristor’s fingerprints

Any memristive device is distinguished by two fingerprints [22]. First, the \(i-v\) characteristics is always a zero-crossing hysteresis loop. Second, the lobe area of the \(i-v\) characteristics shrinks as the signal frequency increases. In the case of infinite frequency, the memristor acts as a single-values linear resistor [23].

The simulated \(i-v\) characteristics of the proposed SRM model is shown in Figure 2. From the graph, it can be seen that \(i(t)\) is always zero when \(v(t)\) is zero regardless of the value of \(R_m\). Furthermore, the hysteresis loop shrinks as the frequency increases. At very high frequency, the state variable is ceased at (or near) one of the device boundaries (i.e. \(w_{off}\) or \(w_{on}\)). Taken together, these results suggest that the memristor at higher frequencies involves a lower difference between \(R_{off}\) and \(R_{on}\). The following simulations show that the proposed model is capable of reproducing the \(i-v\) characteristics of different bipolar SRM devices.
A self-rectifying memristor model for simulation and ReRAM applications (Sinan Sabah)

3.2. Fitting the proposed SRM Model to experimental data

An example of a bipolar memristor with asymmetric threshold voltages and self-rectification property is the Ag/a-Si/p-Si memristor [24]. Figure 3 shows the simulated $i$-$v$ response of the Ag/a-Si/p-Si memristor using the proposed SRM model. The model parameters listed in Table 1 are experimentally chosen to fit the reference memristor reported in [13]. Assuming an OFF initial state, the memristor does not change its resistance immediately as the voltage increases. It is not until $v(t)$ exceeds $v_{on}=2V$ then the state variable starts to change until the device is switched ON. During negative voltage sweep, a diode-like rectification behavior takes place as the device shows higher resistance but without changing $w$. The device is switched OFF only when $v(t)$ goes below $v_{off}=-3.5V$. Lastly, the remaining parameters of the proposed model are regarded as fitting parameters that can be experimentally adjusted so as to produce the same $i$-$v$ characteristics of the memristor to be simulated.

![Figure 2](image1.png)

Figure 2. $i$-$v$ response of the proposed SRM model for different input frequencies. Inset: input voltage

![Figure 3](image2.png)

Figure 3. Fitting the proposed SRM model to Ag/a-Si/p-Si memristor. (a) $i$-$v$ characteristics produced by the proposed SRM model, (b) The actual $i$-$v$ characteristics of Ag/a-Si/p-Si memristor [13]. Inset window is the applied voltage across the memristor

| Memristor       | SRM model parameters | Value |
|-----------------|----------------------|-------|
|                 | $R_{off}$            | $10^9$ Ω |
|                 | $R_{on}$             | $10^6$ Ω |
|                 | $v_{off}$            | $-3.5$ V |
|                 | $v_{on}$             | $2$ V |
| Ag/a-Si/p-Si    | $k_{off}$            | $12$ m/sec |
|                 | $k_{on}$             | $4$ m/sec |
|                 | $a_{off}$            | $1$ |
|                 | $a_{on}$             | $1$ |
|                 | $w_{off}$            | $0$ nm |
|                 | $w_{on}$             | $10$ nm |

Table 1. Proposed SRM model parameters fitted to simulate Ag/a-Si/p-Si memristor
### 3.3. Fitting and comparison of the proposed SRM model with another model

Another feature of the proposed model is reproducing the $i$-$v$ characteristics of the previous SRM model introduced by Gao et al., [20]. The latter one is based on a bipolar SRM device with symmetric threshold voltages. On one hand, $R_{off}$, $R_{on}$, $v_{off}$, and $v_{on}$ of Gao’s model are first extracted and then used in the proposed model to reproduce the $i$-$v$ characteristics. On the other hand, $k_{off}$, $k_{on}$, $\alpha_{off}$, and $\alpha_{on}$ are experimentally calculated so as to produce the same $i$-$v$ characteristics of Gao’s model as given in Table 2. The $i$-$v$ characteristics for both models are shown side-by-side in Figure 4 where the supplied input is a sine-wave voltage whose amplitude is 2V and frequency is 10MHz. Unlike the proposed SRM model, the memristance in Gao’s model depends exponentially on $w$ in a similar manner to the memristor model presented in [25].

![Figure 4. Fitting the proposed SRM model to other SRM models. (a) SRM model fitted to Gao’s model, and (b) $i$-$v$ characteristics of Gao’s SRM model [20]. Inset window is a logarithmic plot of the $i$-$v$ curve.](image)

### Table 2. Proposed SRM model parameters fitted to other SRM models

| Memristor Model | SRM model parameters | Value          |
|-----------------|----------------------|----------------|
| Gao et al. [20] | $R_{off}$            | 500MΩ          |
|                 | $R_{on}$             | 500kΩ          |
|                 | $v_{off}$            | -1.5 V         |
|                 | $v_{on}$             | 1.5 V          |
|                 | $k_{off}$            | 15.25 m/sec    |
|                 | $k_{on}$             | 11.67 m/sec    |
|                 | $\alpha_{off}$       | 1              |
|                 | $\alpha_{on}$        | 1              |
|                 | $w_{off}$            | 10nm           |
|                 | $w_{on}$             | 0nm            |

### 4. CONCLUSION

In this paper, a mathematical model for bipolar memristors with self-rectifying behavior is proposed. The introduces a nonlinear relationship between the internal state variable and the memristance. In addition, the model is flexible to simulate different SRM devices with either symmetric or asymmetric threshold voltages by experimentally adjusting the fitting parameters. A verification process is performed that shows compliance of the model with the basic memristor fingerprints as well as memristor’s experimental data and other existing SRM models. The findings in this study will help to implement memristor-based circuits and applications as well as examining the sneak path current issue in memristive crossbar structure memories.

### REFERENCES

[1] N. F. Kosmani, F. A. Hamid, and M. A. Razali, "A comparison of performance between double-gate and gate-all-around nanowire MOSFET," Indonesian Journal of Electrical Engineering and Computer Science (IJEECS), vol. 13, no. 2, pp. 801-807, 2019.

[2] A. Chen, "A review of emerging non-volatile memory (NVM) technologies and applications," Solid-State Electronics, vol. 125, pp. 25-38, 2016.

[3] C. Xu, X. Dong, N. P. Jouppi, and Y. Xie, “Design implications of memristor-based RRAM cross-point structures,” in 2011 Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, pp. 1-6, 2011.

[4] J. H. L. Teo, N. A. N. Hashim, A. Ghazali, and F. A. Hamid, "Configurations of memristor-based APUF for improved performance," Bulletin of Electrical Engineering and Informatics (BEEI), vol. 8, no. 1, pp. 74-82, 2019.
[5] F. Pan, S. Gao, C. Chen, C. Song, and F. Zeng, "Recent progress in resistive random access memories: materials, switching mechanisms, and performance," *Materials Science and Engineering: R: Reports*, vol. 83, pp. 1-59, 2014.

[6] B. Mohammad, D. Homouz, and H. Elgabra, "Robust hybrid memristor-cmos memory: modeling and design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 11, pp. 2069-2079, 2013.

[7] E. S. Yadav, B. Rajesh, C. Srivivasan, and P. S. Kalyan, "A Study on Non-Linear Behavior of Memristor Emulator Using Multism," *Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)*, vol. 16, no. 3, pp. 1213-1220, 2019.

[8] F. García-Redondo, M. López-Vallejo, and P. Iuero, "Building memristor applications: From device model to circuit design," *IEEE Transactions on Nanotechnology*, vol. 13, no. 6, pp. 1154-1162, 2014.

[9] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80-83, 2008.

[10] S. Munjal and N. Khare, "Advances in resistive switching based memory devices," *Journal of Physics D: Applied Physics*, vol. 52, no. 43, 2019.

[11] M. Khalid, "Review on Various Memristor Models, Characteristics, Potential Applications, and Future Works," *Transactions on Electrical and Electronic Materials*, vol. 20, pp. 289-298, 2019.

[12] A. Ascoli, F. Corinto, V. Senger, and R. Tetzlaff, "Memristor model comparison," *IEEE Circuits and Systems Magazine*, vol. 13, no. 2, pp. 89-105, 2013.

[13] K.-H. Kim, S. Hyun Jo, S. Gaba, and W. Lu, "Nanoscale resistive memory with intrinsic diode characteristics and long endurance," *Applied Physics Letters*, vol. 96, no. 5, p. 053106, 2010.

[14] P. Huang, S. Chen, Y. Zhao, B. Chen, B. Gao, L. Liu, et al., "Self-selection RRAM cell with sub-μA switching current and robust reliability fabricated by high-K/metal gate CMOS compatible technology," *2016 IEEE Silicon Nanoelectronics Workshop (SNW)*, Honolulu, HI, pp. 38-39, 2016.

[15] H. Lv, Y. Li, Q. Liu, S. Long, L. Li, and M. Liu, "Self-rectifying resistive-switching device with a-Si/WO3 bilayer," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 229-231, 2013.

[16] J. Zhou, F. Cai, Q. Wang, B. Chen, S. Gaba, and W. D. Lu, "Very low-programming-current RRAM with self-rectifying characteristics," *IEEE Electron Device Letters*, vol. 37, no. 4, pp. 404-407, 2016.

[17] Q. Zuo, S. Long, Q. Liu, S. Zhang, Q. Wang, Y. Li, et al., "Self-rectifying effect in gold nanocrystal-embedded zirconium oxide resistive memory," *Journal of Applied Physics*, vol. 106, no. 7, p. 73724, 2009.

[18] S. Sabah, N. B. Sulaiman, N. A. M. Yunus, M. N. Hamidion, and N. H. B. Hamid, "Read Operation Performance Analysis of Modified Crossbar Array Structures with Self-Rectifying Memristive Device Model," *International Journal of Control Theory and Applications*, vol. 9, no. 31, pp. 53-61, 2016.

[19] S. Sabah, "Sneak Path CurrentTolerant Resistive Crossbar Array Structures based on Self-Rectifying Memristor Model for Memory Applications," Ph.D. Thesis, Universiti Putra Malaysia, 2017.

[20] Y. Gao, O. Kavehei, S. F. Al-Sarawi, D. C. Ranasinghe, and D. Abbott, "Read operation performance of large selectortless cross-point array with self-rectifying memristive device," *INTEGRATION*, vol. 54, pp. 56-64, 2016.

[21] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: threshold adaptive memristor model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 211-221, 2013.

[22] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on circuit theory*, vol. 18, no. 5, pp. 507-519, 1971.

[23] L. Chua, "If it’s pinched it’s a memristor," *Semiconductor Science and Technology*, vol. 29, no. 10, p. 104001, 2014.

[24] K.-H. Kim, S. Gaba, D. Wheeler, J. M. Cruz-Albrecht, T. Hussain, N. Srivivasan, et al., "A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications," *Nano letters*, vol. 12, no. 1, pp. 389-395, 2011.

[25] M. D. Picket, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, et al., "Switching dynamics in titanium dioxide memristive devices," *Journal of Applied Physics*, vol. 106, no. 7, p. 074508, 2009.

**BIOGRAPHIES OF AUTHORS**

**Sinan Sabah** received the B.Sc. degree in electronic and communications engineering from University of Baghdad and M.Sc. in information technology from Iraqi Commission for Computers and Informatics, Iraq, in 2003 and 2006, respectively. He was awarded the Ph.D. degree in electronics engineering from Universiti Putra Malaysia in 2018. He is currently a lecturer in the department of electronic and communications engineering at University of Baghdad, Iraq. His research interests include memristive switches, memristor-based circuits and fault tolerant architecture.

**Nasri bin Sulaiman** is an associate professor at the Department of Electrical and Electronic Engineering, Faculty of Engineering, Universiti Putra Malaysia. He received a B.Sc. degree in electronics and computer engineering from the Universiti Putra Malaysia (UPM), Malaysia in 1994 and a master degree in microelectronics system design from the University of Southampton, United Kingdom in 1999. He also awarded a Ph.D. degree in adaptive hardware from the University of Edinburgh, United Kingdom in 2007. His areas of interest include evolutionary algorithms, digital signal processing, digital communications, and low power VLSI designs.