Improvements on the Interfacial Properties of High-k/Ge MIS Structures by Inserting a La$_2$O$_3$ Passivation Layer

Lu Zhao, Hongxia Liu *, Xing Wang **, Yongte Wang and Shulong Wang

Key Laboratory for Wide Band Gap Semiconductor Materials and Devices of Education, School of Microelectronics, Xidian University, Xi’an 710071, China; lzhaoxd@163.com (L.Z.); mikewyt@163.com (Y.W.); slwang@xidian.edu.cn (S.W.)

* Correspondence: hxliu@mail.xidian.edu.cn (H.L.); xwangsm@xidian.edu.cn (X.W.)

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Abstract: In this paper, the impact of La$_2$O$_3$ passivation layers on the interfacial properties of Ge-based metal-insulator-semiconductor (MIS) structures was investigated. It was proven that the formation of a thermodynamically stable LaGeO$_x$ component by incorporating a La$_2$O$_3$ interlayer could effectively suppress desorption of the interfacial layer from GeO$_2$ to volatile GeO. The suppression of GeO desorption contributed to the decrease in oxide trapped charges and interfacial traps in the bulk of the gate insulator, or the nearby interfacial regions in the Al$_2$O$_3$/La$_2$O$_3$/Ge structure. Consequently, the hysteretic behavior of the dual-swept capacitance-voltage ($C$-V) curves and the frequency dispersion of multi-frequency $C$-V curves were remarkably weakened. Besides, more than one order of magnitude decrease in the gate leakage current density, and higher insulator breakdown electric field were obtained after inserting a La$_2$O$_3$ passivation layer.

Keywords: atomic layer deposition; Ge-based MIS; surface passivation; interfacial properties

1. Introduction

For a very long time, the excellent properties of a SiO$_2$/Si interface, with high band offsets and few interfacial defects, have been the key reasons for supporting Si use as the main semiconductor material in integrated circuits (IC) [1]. However, with the continued scaling of the device’s size feature on a Si-based complementary metal oxide semiconductor (CMOS) process, high dielectric constant (high-k) materials have been introduced as alternative gate oxide dielectrics to replace ultrathin SiO$_2$. The purpose was to reduce gate leakage current and power consumption beyond 45-nm technology nodes [2,3]. The introduction of high-k dielectrics into the Si-based CMOS process results in poorer insulator/Si interfaces compared to that of SiO$_2$/Si, bringing in some unfavorable impacts such as instability problems and mobility degradation [4]. Considering this, alternative technological progress to dimension scaling, such as changing channel material, is also necessary for achieving high performance devices [5]. Owing to its high intrinsic hole mobility, Ge has drawn remarkable attention for realizing high performance applications in the past decade [6,7]. Ge-based metal-insulator-semiconductor (MIS) devices have shown great potential for integration into the Si CMOS technology, since promising electrical characteristics beyond those of Si devices could be realized by high-k/Ge structures [8]. However, there are some obstacles to overcome before employing Ge into a CMOS-compatible processing scheme with high performance. One of the most critical issues to solve is the Ge surface passivation engineering prior to the deposition of gate oxides [9]. For most high-k dielectric films deposited on Ge substrates without any surface passivation treatments, the generation of unstable Ge oxides is unavoidable during the thermal annealing process. That is,
at temperatures higher than 400 °C, GeO₂ reacts with Ge atoms at high-k dielectrics/Ge interface, which then form substoichiometric Ge oxides, including volatile GeO [10,11]. The desorption of GeO brings in a large number of structural defects, which would deteriorate the properties of the insulator/Ge interface [12].

Recently, it has been reported that rare earth oxides (REOs; i.e., Y₂O₃, CeO₂, Sm₂O₃, and La₂O₃) show high affinity for Ge atoms. That is, the strong reaction between REOs and Ge substrates leads to the catalytic oxidation of Ge, which results in the spontaneous formation of stable interfacial layers [13–16]. Amongst the REOs, due to their large dielectric constant and high band offset relative to Ge, La-based oxides are considered as one kind of promising alternative gate dielectrics in Ge-based MIS devices, which can achieve more aggressive equivalent oxide thickness (EOT) scaling [17,18]. Furthermore, as the interface between La-based oxides and Ge substrates shows much better thermodynamic stability than that of GeO₂/Ge, La-based oxides have promising interfacial passivation effects and could improve the electrical performance of Ge-based MIS devices [19,20]. Considering this, the effects of inserting a La₂O₃ passivation layer between an Al₂O₃ dielectric and Ge substrate, on the interfacial properties of Al/Al₂O₃/Ge and Al/Al₂O₃/La₂O₃/Ge MIS structures was investigated in this paper.

2. Experimental Section

La₂O₃ and Al₂O₃ gate stack films were deposited on n-type Ge (100) substrates, with electrical resistivity of about 0.1–1 Ω-cm, in an atomic layer deposition (ALD) reactor (R-150, Picosun, Espoo, Finland). Prior to the deposition, Ge substrates were treated with acetone and hydrous alcohol, and then cyclically dipped into a diluted HF solution (HF:H₂O = 1:50) 5 times to remove the native GeO₂ layer. During the deposition process, La(i–PrCp)₃ and trimethylaluminum (TMA) were used as La and Al precursors, respectively, while H₂O was used as an oxidant. The precursors were alternately introduced to the reactor chamber, and were carried by high purity N₂ (>99.999%). A typical ALD growth cycle for La₂O₃ was 0.3 s La(i–PrCp)₃ pulse, followed by 4 s N₂ purge and 0.3 s H₂O pulse, followed by 9 s N₂ purge. The Al₂O₃ ALD cycle structure was set as 0.1 s TMA pulse/3 s N₂ purge/0.1 s H₂O pulse/4 s N₂ purge. By varying the number of ALD cycles, a 2 nm La₂O₃ oxide layer was deposited on the cleaned Ge substrate at 300 °C, followed by deposition of a 4 nm Al₂O₃ layer. For comparison, a control sample with only 6 nm Al₂O₃ as gate dielectrics was also prepared. After the deposition, rapid thermal annealing (RTA) was performed at 600 °C for 90 s in N₂ ambient for both Al₂O₃/La₂O₃/Ge and Al₂O₃/Ge structures.

The surface morphology of the deposited films was monitored using atomic force microscopy (AFM, Dimension 3100, Veeco Digital Instruments by Bruker, Billerica, MA, USA) in tapping mode. The physical thickness was optically measured using Woollam M2000D spectroscopic ellipsometry (SE, Woollam Co. Inc., Lincoln, NE, USA) fitted with a Cauchy model. The chemical bonding state of the deposited films was used to evaluate the electrical properties of the deposited films. Al was evaporated using electron-beam evaporation as a metal gate through a shadow mask with a diameter of 300 μm followed by a post metallization annealing (PMA) carried out in 97% N₂/3% H₂ ambient at 400 °C for 20 min to form a good Ohmic contact with gate dielectrics. Then the electrical properties of the fabricated MIS capacitors were evaluated using an Agilent B1500A parameter analyzer (Santa Clara, CA, USA).

3. Results and Discussion

The Ge 3d spectra of the samples with and without the La₂O₃ passivation layer are shown in Figure 1. During the analysis of XPS data, the C 1s peak extracted from adventitious carbon at 284.6 eV was chosen as a bonding energy calibration reference. Compared with Figure 1a, a noteworthy change in Figure 1b was the appearance of a LaGeOₓ peak, indicating that a LaGeOₓ component was generated after inserting a thin La₂O₃ interlayer. Besides, the Ge oxide (GeOₓ) spectra could be divided into
The existence of these GeO properties of Ge-based MIS structures, the electrical properties of the fabricated MIS capacitors were measured simultaneously with the backward swept C-V curves. The capacitance values at the accumulation and inversion states were obtained by biasing the gate-applied voltage from accumulation to inversion (backward sweep), and sweeping the back (forward sweep) at 100 kHz. C-V measurements were performed simultaneously with the gate leakage current density-voltage (J-V) characteristics of the fabricated MIS capacitors. The dual-swept C-V curves of the MIS capacitor with La2O3 as an interfacial passivation layer were obtained by biasing the gate-applied voltage from accumulation to inversion (backward sweep), and sweeping back (forward sweep) at 100 kHz. G-V measurements were performed simultaneously with the gate leakage current density-voltage (J-V) characteristics of the fabricated MIS capacitors.
backward swept C-V curves. The capacitance values at the accumulation region of the C-V curves for capacitor S1 and S2 were 1.06 and 1.41 μF/cm², respectively. The dielectric constant values of the samples were estimated using the following equations [25,26]:

\[ C_{ox} = C_{ac} \left[ 1 + \left( \frac{G_{ac}}{\omega C_{ac}} \right)^2 \right] \] (1)

\[ CET = \frac{\varepsilon_0 \varepsilon_{SiO_2} A}{C_{ox}} \] (2)

\[ k = \frac{\varepsilon_{SiO_2} t_{ox}}{CET} \] (3)

where \( C_{ac} \) is the capacitance value at the accumulation region, \( G_{ac} \) is the conductance corresponding to the accumulation region of the C-V curves, \( \omega \) is the angular frequency, \( C_{ox} \) is the oxide capacitance of dielectric films, \( A \) is the electrode area, \( t_{ox} \) is the measured thickness of gate dielectrics, \( \varepsilon_0 \) and \( \varepsilon_{SiO_2} \) are the permittivity values of vacuum and SiO₂, respectively. The physical thickness of the gate dielectric films in S1 and S2 was measured to be 6.42 and 6.83 nm, separately. Therefore, the effective dielectric constant values of S1 and S2 were calculated to be 7.95 and 11.10, respectively. The increment in the dielectric constant value for the sample with a La₂O₃ interfacial passivation layer was attributed to the introduction of La elements into dielectric films, since the \( k \) values of La₂O₃ [27], and LaₓAlₓO [28] formed by the interdiffusion of La₂O₃ and Al₂O₃ were much higher than that of Al₂O₃ [29].

Figure 2. (a) Two- and (b) three-dimensional AFM images of the Al₂O₃ films on Ge substrates without La₂O₃ passivation; and (c) two- and (d) three-dimensional AFM images of the Al₂O₃ films on Ge substrates with a La₂O₃ interfacial passivation layer.

The flat band voltages (\( V_{FB} \)) of the C-V curves in Figure 3 were extracted from the Hauser NCSU CVC simulation software (North Carolina State University, Raleigh, NC, USA), taking quantum mechanical effects into account [30]. It was observed that the Al/Al₂O₃/Ge MIS capacitor showed a much larger flat band voltage hysteresis width (\( \Delta V_{FB} \)), ~863 mV, than that of S2 (~174 mV).
The hysteretic behavior of the dual-swept C-V curves has been proven to be caused by the existence of oxide trapped charges ($Q_{ox}$) in the bulk of the gate insulator or nearby the interfacial region [31]. Using the midgap charge separation method, the oxide-trapped charge density ($N_{ot}$) for the fabricated capacitors was calculated using the following equation [32]:

$$N_{ot} = \frac{\Delta V_{FB}C_{ox}}{qA}$$

where $\Delta V_{FB}$ is the hysteresis width of $V_{FB}$, $C_{ox}$ is the oxide capacitance, $q$ is the elementary charge ($1.602 \times 10^{-19}$ C), and $A$ is the electrode area. The $N_{ot}$ values were calculated to be $5.91 \times 10^{12}$ cm$^{-2}$ for the Al/Al$_2$O$_3$/Ge MIS capacitor, and $1.56 \times 10^{12}$ cm$^{-2}$ for the case with a La$_2$O$_3$ passivation layer. A visible decrease of $N_{ot}$ was observed after inserting a La$_2$O$_3$ passivation layer.

![Figure 3. C-V characteristics for the fabricated MIS capacitors using Al$_2$O$_3$ films as insulators (a) without and (b) with a La$_2$O$_3$ interfacial passivation layer.](image)

The C-V curves of the MIS capacitors without the La$_2$O$_3$ interlayer showed a significant anomalous hump phenomena at the weak inversion regions as shown in Figure 3a, which were reported to be caused by slow interfacial traps existing between the gate insulator and substrate [33]. Besides, as shown in Figure 4, different amounts of interfacial traps caused different degrees of frequency dispersion phenomena at the weak inversion regions of the C-V curves measured at multi-frequencies. Considering this, we discussed the interface state density ($D_{it}$) values of S1 and S2, extracted from the combination of the backward swept C-V and G-V characteristics, using the following relation of single-frequency approximation method [29,34]:

$$D_{it} = \frac{2}{qA} \left[ \frac{C_{max}}{G_{ox}} \right]$$

where $A$ is the electrode area, $C_{ox}$ is the gate oxide capacitance as defined in Equation (1), $G_{max}$ is the peak value of G-V curve, and $C_{max}$ is the capacitance corresponding to $G_{max}$ at the same gate-applied voltage. The various parameter results discussed above are shown in Table 1. For the fabricated MIS capacitors without a La$_2$O$_3$ passivation layer, the value of $D_{it}$ was about $1.13 \times 10^{13}$ eV$^{-1}\cdot$cm$^{-2}$. After the Ge surface passivation treatment using a La$_2$O$_3$ interlayer, the $D_{it}$ value decreased evidently to $\sim 4.97 \times 10^{12}$ eV$^{-1}\cdot$cm$^{-2}$, indicating that to some extent, the insertion of a La$_2$O$_3$ passivation layer inhibited the generation of interface traps, which gave an explanation to the pronounced weak anomalous hump tendency. It is worth noting that, the frequency dispersion phenomenon was also observed at the accumulation region of the C-V curves. It has been reported by Kouda et al. that the frequency-dependent variations in the dielectric constant of the gate stacks caused by oxygen vacancies should be responsible for the frequency dispersion phenomenon at the accumulation region [14,35]. As shown in Figure 4, the frequency dispersion phenomenon at the
accumulation region became weaker after inserting a La$_2$O$_3$ interlayer, indicating that the introduction of this interlayer suppressed the generation of oxygen vacancies in the stack structures.

Table 1. The electrical parameters extracted from the fabricated MIS capacitors without and with a La$_2$O$_3$ interfacial passivation layer.

| Sample | $C_{ox}$ ($\mu$F/cm$^2$) | $k$ | $\Delta V_{FB}$ (mV) | $N_{ot}$ (cm$^{-2}$) | $D_{it}$ (eV$^{-1}$·cm$^{-2}$) |
|--------|----------------|-----|---------------------|-----------------|-----------------|
| S1     | 1.096          | 7.95| 863                 | $5.91 \times 10^{12}$ | $1.13 \times 10^{13}$ |
| S2     | 1.438          | 11.10| 174                | $1.56 \times 10^{12}$ | $4.97 \times 10^{12}$ |

Figure 4. C-V characteristics measured at various frequencies for the fabricated MIS capacitors using Al$_2$O$_3$ films as insulators (a) without, and (b) with a La$_2$O$_3$ interfacial passivation layer.

The contribution of the La$_2$O$_3$ interfacial passivation layer to the decrease in trapped oxide charges and interfacial traps could be explained as follows: when Al$_2$O$_3$ dielectrics were deposited on the Ge substrates without any passivation treatment, the outdiffusion of Ge atoms to the Al$_2$O$_3$ dielectric films generated unstable Ge oxides at the Al$_2$O$_3$/Ge interface. The quality of the interface between Ge and its oxides tends to deteriorate during the PDA process because the decomposition or desorption from GeO$_2$ to GeO following the reaction equation of $\text{GeO}_2 + \text{Ge} \rightarrow 2\text{GeO}$ leads to the formation of structural defects mainly consisting of dangling bonds and oxygen vacancies [36]. While after inserting the La$_2$O$_3$ interfacial passivation layer, La$_2$O$_3$ could react with the outdiffused Ge atoms to form the stable LaGeO$_3$ compound, which would effectively suppress the generation of volatile GeO$_x$ contributing to the decrease of structural defects in the bulk of the insulator and/or in the interfacial region. As a result, the $N_{ot}$ and $D_{it}$ values were obviously decreased by inserting a La$_2$O$_3$ passivation layer of insulator/Ge interfaces, contributing to the suppression of hysteresis in dual-swept C-V curves and frequency dispersion in multi-frequency C-V curves.

Figure 5 shows the gate leakage current density of the fabricated MIS capacitors as a function of the gate-applied electrical field. The gate leakage current density for capacitors S1 and S2 were separately measured to be $1.92 \times 10^{-4}$ and $1.29 \times 10^{-5}$ A/cm$^2$ when the gate-applied electrical field was 3 MV/cm. More than one order of magnitude decrease in the gate leakage current density was achieved after inserting a La$_2$O$_3$ passivation layer. Furthermore, it is worth noting that the gate insulator breakdown electric field of capacitor S2 (~ 7.07 MV/cm) was apparently higher than that of capacitor S1 (~ 5.86 MV/cm), which revealed that the inserted La$_2$O$_3$ passivation layer had a positive effect on the breakdown characteristics of the gate insulators. The improvements in gate leakage current density and gate insulator breakdown characteristics were suspected to benefit from the reduction of structural defects including dangling bonds and oxygen vacancies [37]. For the sample with a La$_2$O$_3$ passivation layer, less structural defects in the gate insulator meant a smaller possibility of creating a continuous chain connecting the gate electrode to the substrate semiconductor, contributing to the realization of lower gate leakage current density and higher insulator breakdown electric field [38].
4. Conclusions

The Ge surface engineering using La$_2$O$_3$ as a passivation layer was carried out and investigated systematically in this paper. The formation of a thermodynamically stable LaGeO$_x$ interfacial layer effectively suppressed the desorption of volatile GeO, resulting in smaller $N_{ot}$ and $D_{it}$ values achieved after the insertion of a La$_2$O$_3$ passivation layer compared with the control sample. These improvements on the interfacial properties significantly weakened the hysteresis in dual-swept C-V curves and frequency dispersion in multi-frequency C-V curves. Besides, the gate leakage current and insulator breakdown characteristics for the MIS structure with La$_2$O$_3$ passivation were also improved.

**Author Contributions:** L.Z. generated the research idea, analyzed the data, and wrote the paper; L.Z., X.W., and Y.W. carried out the experiments and the measurements; S.W. participated in the discussions; H.L. gave final approval of the version to be published. All authors read and approved the final manuscript.

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**Conflicts of Interest:** The authors declare no conflicts of interest.

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