Single Event Effect Characterization of High Speed Serial JESD204B Data Receiver

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Abstract. This work proposed and discussed a serial JESD204B data receiver and conducted a single event effect test on it. The test is used to analyze the Single Event Upset (SEU), single Event Latch-up (SEL) and Single Event Functional Interrupt (SEFI). The purpose of the test is to determine if single event effect caused the chip to crash or increase the on-track error rate. The results show that the circuit has a strong ability to resist Single event effect.

1. Introduction
The data transmission speed between high performance data converter based on space system and ASICs or FPGAs is required to reach Gbps level. Compared with its predecessors CMOS and LVDS products, JESD 204B has advantages in speed, size and cost [1-2].

Radiation sensitivity testing of the circuit for including Single event effect and Total Ionizing Dose effects [3-4]. This paper mainly focuses on the study of single ion effect. We conducted multiple Single event effect (SEE) tests on a high-speed serial JESD204B data receiver in China institute of atomic energy and Institute of modern physics, Chinese Academy of Sciences.

In the experiment, we mainly analyzed and discussed the Single Event Upset (SEU), single Event Latch-up (SEL) and Single Event Functional Interrupt (SEFI) of the chip, and analyzed the influence of single event effect on bit error rate of the chip.

In this article, we will introduce our test chip and its functions in the first part. In the second part, we introduce our test equipment and process. In the third part, we analyze the test data and phenomena.

2. Chip introduction
The block diagram of the test chip is shown in Figure 1. The protocol layer is compatible with JESD204B specification and supports multi-chip synchronous applications of ADC or DAC chips. The chip is encapsulated in FC-CBGA160. And it has a variety of working modes, the highest serial data rate of a single channel >8Gbps. In Single event effect tests, we choose two modes: 4 Gbps and 6.25 Gbps.
Figure 1. block diagram

Key functions of radiation resistant high-speed serial JESD204B data receiver:

a) The protocol layer is compatible with JESD204B specification and supports multi-chip synchronous application of ADC or DAC chips.

b) Support 12 bit sampling accuracy dual channel DAC with LVDS input and double data rate.

c) Maximum data rate of parallel terminal: \( \geq 800 \text{Mbps} \), minimum data rate: \( \leq 125 \text{Mbps} \).

d) Single channel data rate range: the highest data rate \( \geq 8 \text{Gbps} \), the lowest data rate \( \leq 1.25 \text{Gbps} \). The optimal design range is 4.7Gbps-8Gbps.

e) Error detection function: provide error detection indication signal through output, and report the following error information: 8B/10B code table error, polarity error, wrong K code reception, PLL loss of lock, CDR loss of lock, 204B controller failure.

f) High-speed data channel (lane) RX receiver is equipped with adjustable equalizer to realize 9-15dB receiving signal equalization and meet the requirements of channel attenuation compensation.

g) The JESD204B revision provides a mechanism to ensure that delays are reproducible and deterministic between two power cycles and during link resynchronization.

h) The circuit has PRBS self-detection function. A variety of parallel and serial loop backchannels are built inside the circuit and PRBS data are generated for checking the circuit.

3. Introduction of test equipment and process

The SEE test equipment is composed of FPGA irradiation board (as shown in the figure 2), power supply, oscilloscope, upper computer, network analyzer, etc. The test board is connected to the upper computer and power through RS232 serial port, and the upper computer downloads the program to the test board through the downloader.
3.1. Test process

3.2. Detection mechanism:
The incremental data of 32'h 00000000-32'h FFFFFFFF (divided into 256 number one packet) is sent by the FPGA to the parallel input of the circuit. We replace the first two bits of each packet as the header. The first bit is the header data of 32'h FFFFFFFF, and the second header data is the 24-bit packet count. The two-bit header is detected by the FPGA. After the detection is successful, a synchronous 32-bit increment data is generated by the FPGA. The error is calculated by comparing the two sets of data. Through this packaging, we believe that it can avoid the “function interruption” caused by data misalignment.

3.3. Error type:
In SEE test, we stipulated that:

a) When an error occurs in one bit of 32-bit data, it is recorded as a unit error.

b) When a multi-bit error occurs in a 32-bit data sequence, it is recorded as a Multiple error.

c) When continuous errors occur in 32-bit data at the same time, they are recorded as burst errors.

d) The sum of the number of bits of all errors in the experiment is Total number of error bits.

Four error counters were set up to record the number of Four kinds of errors, the total number of single particle dislocation. The number of errors is sent back to the host through the serial port and recorded every 1/14 second.

3.4. Functional interruption (SEFI) criterion:
If the number of errors uploaded to the host computer occurs a continuous error. The irradiation is stopped. Observe whether the number of errors is still changing. If the change occurs, the single event
function interruption occurs. Increase the number of interruptions by 1. If the number of errors stops changing, it is determined to be a single event upset and the experiment continues.

3.5. Single event Latchup criterion:
In the test, the operating voltage VDD and VCORE of the power supply are 2.75V and 1.32V respectively, and the error is less than <1%. The circuit runs a single event reversal test program, and monitors the current in real time through digital multimeter and programmable power supply. If the working current of the device suddenly exceeds 50% of the normal working current, it is determined to be a single-particle latch-up. If latch-up occurs, power off and record the current at this time, then stop irradiation and end irradiation test.

3.6. Total ion flux
When the total ion flux reaches 1.0E+07 particles/ cm², the irradiation will stop and the experiment will be finished.

3.7. Other monitoring quantity
a) SYNC monitoring: On the basis of error records, in order to analyze the data loss, performance loss and the causes of link interruption, we use FPGA to collect relevant data and monitor SYNC (indicating whether the data link is connected successfully) through ISE ChipScop.

b) Clock monitoring: In order to determine the effect of single event effect on the state of circuit CDR clock. We divide the output clock of the circuit and send the signal to the host computer through the FPGA for monitoring. In the data analysis phase, the error counter is compared with the image captured by ChipScop to analyze the data loss, performance loss and the cause of the link link interruption.

c) Error indication signal monitoring: The circuit can provide error detection indication signal through output (STATUS_OUT<2:0>) to correct the following error information: 8B/10B code table error, polarity error, error K code reception. We can locate specific errors by querying SPI registers. Through the SPI register, the working state of the internal circuit can be queried.

3.8. Heavy ion Sample Information
In SEE test, the heavy ion samples we used for the SEE test are shown in the following table I.

| Ion | Energy (MeV) | LET (MeV-cm²/mg) | Ion Range(um) | Fluence rate (/cm²-s) | Total ion flux (/cm²) |
|-----|--------------|-----------------|---------------|----------------------|----------------------|
| Cl  | 164          | 12.9            | 47.4          | 4000                 | 4.5E+6               |
| Ge  | 208          | 37.3            | 30.3          | 5.0E+01              | 2.14E+04             |
| Kr  | 465.8        | 37.83           | 56.9          | 500                  | 1.32E+5              |
| Ta  | 1603         | 79.24           | 94.2          | 200                  | 1.4E+05              |

4. Test data and phenomenon analysis

4.1. Test data
We conducted a Single event effect test (Cl, Ge) at China institute of atomic energy on May 15, 2019. And another Single Event effect test (Ta, Kr) at Institute of modern physics, Chinese Academy of Sciences on April 16 and June 24 2019. The test results are shown in table II.
### Table 2. Test data

| Ion | Test rate | SEL | SEFI | Unit error number | Burst errors Number | Multiple error number | Total number of error bits |
|-----|-----------|-----|------|-------------------|----------------------|-----------------------|---------------------------|
| Cl  | 4Gbps     | 0   | 0    | 0                 | 7                    | 994                   | 17989                     |
| Ge  | 4Gbps     | 0   | 0    | 0                 | 0                    | 0                     | 0                         |
| Kr  | 4Gbps     | 0   | 0    | 7                 | 1001                 | 15704                 |
| Ta  | 4Gbps     | 1   | 67   | 4094              | 152                  | 25381                 | 448513                    |
| Kr  | 6.25Gbps  | 2   | 39   | 8741              | 140                  | 76982                 | 1473540                   |

#### 4.2. Experimental phenomena and analysis

**a) Ion Ge did not cause any rollover:**
- Due to the lack of range.

**b) The error number of Ion Kr increases significantly at the rate of 6.25 Gbps:**
- The increase in the transmission rate will lead to an order of magnitude increase in the error interface.

**c) No single-particle latch-up in the experiment:**
- The experimental particles did not reach the single-particle latch-up threshold of the chip.

**d) Three interruptions occurred in the experiment:**
- Functional interruption occurred at the beginning of the experiment. It may be due to circuit and program instability. There was no functional interruption again for a long experiment time.

#### 4.3. Analysis of SYNC Falling:

In the experiment, we found that unit error would not cause SYNC to fall. Only BURST errors cause SYNC to drop. The maximum time is 2.2us. The waveform is shown in Figure 4.

![Waveform of link reconnection caused](image)

Because of the characteristics of JESD204 protocol, Links are automatically reconstructed when errors such as 8B/10B code table errors, polarity errors, wrong K code reception, PLL lockout, CDR lockout, 204B controller failure occur. The error caused by this phenomenon will not continue to increase after reconnection, and manual reset is not required, so it is not judged as function interruption.

**a) During the Ion Cl test:**
- The number of burst errors is 142 each time, and SYNC drops are detected at the same time. After analysis, we believe that the errors were all caused by 8b/10b code table errors or polarity errors. When the system detects errors, it immediately rebuilds the link according to the protocol. The rebuilding time of the link is the same, so the recovery time of SYNC drops is the same.
During the high energy Ion Ta test:
There is the same error form and reconstruction time as that of low energy Cl particle. But the recovery time of SYNC dropping is more than one, and the phenomenon of SYNC dropping repeatedly appears. We believe that this is due to the error of CDR clock recovery caused by energetic ion (which can be observed from the output clock clk_rx). Because of the inconsistency of clock recovery time, the recovery time of SYNC drops increases exponentially.

After analysis, we believe that the different link reconstruction time is due to the different physical structure of the chip has different sensitivity to single event effect. The chip threshold of single event effect is also different. In the future work, we will carry out laser simulation single event effect test to verify our idea.

5. Data process
In this part, we calculate the cross sections of single event effect with different error modes using effective experimental data. We draw the Weibull curve of single event effect cross section and estimate the single event effect threshold of the chip. Finally, we calculate the on-orbit error rate with Space Radiation software.

5.1. Single event effect causes burst errors
The error cross-section is shown in Table III. The LET threshold of 10% saturated cross section is 38.95 MeV·cm²/mg. Using Space Radiation, we calculated the on-orbit error rate of 7.51E-02 errors/day for single event effect causing burst errors. The Weibull curve of the number of errors caused by burst errors is shown in Figure 9. The threshold of burst errors caused by single event effect is 9 MeV·cm²/mg.
Table 3. Burst errors cross-section

| Ion | LET (MeV·cm²/mg) | Burst errors number cross-section |
|-----|-----------------|----------------------------------|
| Cl  | 12.9            | 1.55E-6                          |
| Kr  | 37.83           | 5.30E-5                          |
| Ta  | 79.24           | 1.09E-3                          |

Figure 7. Weibull curve of burst errors

5.2. Single event effect causes Multiple errors
The error cross-section is shown in Table IV. The LET threshold of 10% saturated cross section is 42.31 MeV·cm²/mg. Using Space Radiation, we calculated the on-orbit error rate of 1.32E+00 errors/day for single event effect causing Multiple errors. The Weibull curve of the number of errors caused by Multiple errors is shown in Figure 9. The threshold of Multiple errors caused by single event effect is 9 MeV·cm²/mg.

Table 4. Multiple errors cross-section

| Ion | LET (MeV·cm²/mg) | Multiple errors number cross-section |
|-----|-----------------|-------------------------------------|
| Cl  | 12.9            | 4.00E-3                             |
| Kr  | 37.83           | 1.19E-1                             |
| Ta  | 79.24           | 3.20E-0                             |

Figure 8. Weibull curve of Multiple errors

5.3. Single event effect causes Total number of error bits
The error cross-section is shown in Table V. The LET threshold of 10% saturated cross section is 42.29 MeV·cm²/mg. Using Space Radiation, we calculated the on-orbit error rate of 1.32E+00 errors/day for single event effect causing Total number of error bits. The Weibull curve of the number of errors caused by Total number of error bits is shown in Figure 8. The threshold of Total number of error bits caused by single event effect is 8 MeV·cm²/mg.
Table 5. Multiple errors cross-section

| Ion | LET (MeV·cm²/mg) | Total number of error bits cross-section |
|-----|-------------------|----------------------------------------|
| Cl  | 12.9              | 4.00E-3                                |
| Kr  | 37.83             | 1.19E-1                                |
| Ta  | 79.24             | 3.20E-0                                |

Figure 9. Weibull curve of Total number of error bits

5.4. BER calculation

\[
\text{BER} = \frac{\text{OER} \times T}{60s \times 60\text{min} \times 24\text{h}}
\]

[5](1)

T, Recovery Time of PLL (The maximum recovery time of PLL is about 2.2us).

OER, On-orbit Error Rate.

According to formula 1

a) The bit error rate of the burst errors caused by single event is 1.30E-14.

b) The bit error rate of the Multiple errors caused by single event is 1.19E-12.

c) The bit error rate of the Total number of error bits caused by single event is 3.36E-11.

6. Conclusion

We conducted multiple Single event effect (SEE) tests on the high-speed serial JESD204B data receiver in China institute of atomic energy and Institute of modern physics, Chinese Academy of Sciences.

In the experiment, we found a variety of experimental phenomena and analyzed their causes. We defined three types of errors: unit error, multi-bit error and burst error. We explored the relationship between the transmission rate and the number of errors caused by single event effect. We also calculate the error cross sections and the on-orbit error rate of different kinds of errors.

The results show that the chip has a strong ability to resist Single event effect. There is no current jump in the chip under the condition of continuous test. This shows that the chip has a strong ability to resist single event latch-up. Multiple link reconstruction occurs in the experiment. This reconstruction is based on JESD204B protocol to ensure the correct data transmission, which is automatically carried out in case of link errors. The reconstruction mechanism of JESD204 protocol improves the ability of physical layer to resist Single event effect.

Finally, according to the valid data of the experiment, we draw the conclusion that the single event effect threshold of chip is more than 8 MeV·cm²/mg. The error rate caused by single event effect is less than 10E-10. The single event latch-up threshold is more than 79.24 MeV·cm²/mg.

References

[1] SAHEB H, HAIDE R S. Scalable high speed serial interface for data converters: using the JESD204B industry standard [C] // IEEE Design & Test Symp. Algiers, Algeria. 2015: 6-11.

[2] CHATTOPADHYAY B, BHAT S N, NAYAK G, et al. A 12.5 Gbps transmitter for multi-standard SE RDES in 40nm low leakage CMOS process [C] // IEEE Int Conf VLSI Des & Embed Syst. Pune, India. 2018:13-18.
[3] Carts, M.A., et al., “Single event test methodology and test results of commercial gigabit per second fiber channel hardware,” IEEE Trans/ Nucl., 44, pp1878-1884, 1997.
[4] LaBel, K.A., et al., “Single event effect results for candidate spacecraft electronics,” IEEE REDW, pp14-21, 1997.
[5] Anthony Wilson, Sasko Zarev, Mark Kazmier. Radiation Effect Characterization of a 3.125Gbps 90 nm Serdes IP. IEEE. pp.3-4.