To achieve a package-level DC power grid for the next-generation power delivery to LSIs, multiple point-of-load (POL) buck DC-DC converters must be integrated into the package. We developed a 180 nm CMOS switch DC-DC buck converter for the POL DC power supply using a Zn-Fe ferrite core planar inductor embedded in an organic interposer. The embedded inductor had a 25 μm thick copper spiral coil sandwiched by 10 μm thick Zn-Fe ferrite thick film fabricated using the spin-spray method, which exhibited an inductance of 4.6 nH and a Q-factor of 11 at 50 MHz. A 180 nm CMOS switch was mounted using a flip-chip scheme on the organic interposer with the embedded inductor. The developed 50 MHz switching CMOS switch buck DC-DC converter exhibited a power conversion efficiency of about 68% when the input voltage was 2 V, the on-duty ratio was 0.5, the output voltage was 0.855 V, and the current was 1 A.

Key words: package-level DC power grid, point of load, buck DC-DC converter, Zn-Fe ferrite, CMOS switch, organic interposer

1. Introduction

Recently, DC power delivery to LSIs has been going for a low-voltage/large-current DC power transmission. Fig. 1 shows a schematic illustration of a simple DC power delivery to CMOS logic LSI, where $r$ is the power-line resistance, $l$ is the line inductance. Not only static current $I_{dc}$, but also transient current $\Delta i$ due to the CMOS logic LSI operation flows in the DC power-transmission line. The line-voltage variation $\Delta v$ can be written as follows,

$$\Delta v = r(I_{dc} + \Delta i) + l \frac{\Delta i}{\Delta t} \quad \text{…………………………..(1).}$$

The first term in Eq. (1) means the voltage drop, and the second term means the line-noise. Since the static current $I_{dc}$ is usually much larger than the transient current $\Delta i$ ($I_{dc} \gg \Delta i$), the power-line loss $P_{PL}$ can be denoted as a simple expression,

$$P_{PL} = r I_{dc}^2 \quad \text{…………………………………………(2).}$$

The line-voltage variation $\Delta v$ and the power-line loss $P_{PL}$ increase with increasing the power-line length. In order to reduce the power-line loss and the line-noise, the distributed power supply system with POL (Point of Load) DC-DC converters has been widely employed. Recently, the package-level DC power grid has been proposed 1) as the next generation power delivery to LSIs, which consists of a main buck DC-DC converter and the multiple POL converters integrated into the package. Since the power supply voltage for CMOS logic LSI has been lowered to 1 V or below, it is considered that the POL converter operates under low-voltage output condition. When the package-level DC power grid has a two-step buck converter topology, low-voltage CMOS switch can be selected for the POL converter.

The CMOS switch DC-DC converter using an air-core inductor has been developed by some institutes 2),3). Although the air-core inductor can be fabricated easily using metal process only, there are serious demerits such as low inductance, large footprint and undesired EMI noise owing to widespread alternating magnetic flux. Therefore, magnetic core should be introduced to the inductor in order to make the footprint small and suppress the EMI noise. This paper describes an embedded Zn-Fe ferrite core inductor in an organic interposer and its application to the CMOS switch buck DC-DC converter for POL DC power supply used in the package-level DC power grid.
2. Zn-Fe Ferrite Core Inductor Embedded in Organic Interposer

2.1 Zn-Fe ferrite core made by spin-spray method
In this study, the Zn-Fe ferrite film made by spin-spray method\(^4\) has been used as a magnetic core for the power inductor embedded in the organic interposer. Since the spin-sprayed ferrite can be deposited using oxidizing solution and reaction solution at low temperature around 90 degrees-C, the ferrite synthesis does not give any thermal damage to the organic interposer. A chemical composition of the ferrite is Zn\(_{0.36}\)Fe\(_{2.64}\)O\(_4\) with high saturation magnetization of 0.57 T, and the thick film with 10 \(\mu\)m thickness has been used in order to apply it to the power inductor.

2.2 Zn-Fe ferrite thick film deposited on Polyimide under-layer
In order to embed the Zn-Fe ferrite core inductor in the organic interposer, 10 \(\mu\)m thick Zn-Fe ferrite film must be deposited on a build-up layer of the organic interposer. The build-up layer consists of a few microns glass fillers and epoxy resin, and it has a few microns rough surface. As already reported\(^5\), the Zn-Fe ferrite film deposited directly on the rough surface build-up layer exhibits a degradation of soft magnetic properties such as large coercive force and low permeability because of random orientation grain growth. To improve the degradation of magnetic properties, a 3 \(\mu\)m thick Polyimide film has been introduced as an under-layer for ferrite deposition, which plays an important role of the planarization of the rough-surface build-up layer.

Fig. 2 shows the static magnetization curve and the complex permeability of 10 \(\mu\)m thick Zn-Fe ferrite film with and without Polyimide under-layer on build-up layer of organic interposer\(^5\).

2.3 Zn-Fe ferrite core inductor
By using the embedded inductor technology\(^6\), the Zn-Fe ferrite magnetic core inductor has been embedded in the organic interposer with an 800 \(\mu\)m thick epoxy/glass-fiber center core and 80 \(\mu\)m thick epoxy/glass-filler build-up layers.

The embedded Zn-Fe ferrite core inductor with a 1 \(mm^2\) footprint and about 70 \(\mu\)m heights is shown in Fig. 3, which has an opened magnetic circuit with top and bottom 10 \(\mu\)m thick Zn-Fe ferrite films. A 25 \(\mu\)m thick electroplated copper spiral coil for the embedded inductor has a 2-turn winding with 100/30 \(\mu\)m line/space and 800 \(\mu\)m\(^2\) footprint, which has a DC coil resistance of 25 m\(\Omega\) and is sandwiched by 10 \(\mu\)m thick ferrite film. The epoxy/glass-filler build-up layer is usually formed by thermal laminator in the organic
Fig. 4 Frequency dependence of inductance and resistance in embedded Zn-Fe ferrite core and air-core inductor with 100/30 μm line/space and 25 μm thick 2-turn copper spiral coil.

Fig. 5 Superimposed DC current characteristic of embedded Zn-Fe ferrite core inductor.

interposer fabrication process. As shown in Fig. 3, in our embedded ferrite inductor fabrication process, the 25 μm thick spiral coil can be planarized by using build-up layer laminated directly on the spiral coil. The top and bottom Zn-Fe ferrite films shown in Fig. 3 are deposited on the Polyimide under-layer and patterned by using a photo resist lift-off process.

Fig. 4 shows the frequency dependence of series inductance and resistance measured in the embedded Zn-Fe ferrite core inductor. Also the characteristics of the air-core inductor using the same 2-turn spiral coil are shown in the figure. As shown in Fig. 4, both inductances decrease gradually with increasing frequency. Since the 2-turn spiral coil used in both inductors has 100 μm wide conductor lines, it is considered that the skin effect and proximity effect in the conductor-width direction cause the inductance to decrease and the resistance to increase. The embedded Zn-Fe ferrite core inductor has 4.2 times higher inductance (4.6 nH) than that of the air-core inductor (1.1 nH) at 50 MHz. Q factors of the Zn-Fe ferrite core inductor and the air-core inductor are 11.0 and 7.9 at 50 MHz.

Fig. 5 shows the superimposed DC current characteristic of the embedded Zn-Fe ferrite core inductor measured at 50 MHz. Since the inductance drop at a DC current of 2 A is about 17%, it is considered that the Zn-Fe ferrite core inductor has a possible application to a 1 A output buck DC-DC converter.

3. CMOS Switch for Buck DC-DC Converter

3.1 Schrom’s CMOS switch design method

G. Schrom et al. reported an optimal design of the CMOS switch used in a buck DC-DC converter. Fig. 6 shows an equivalent circuit of the buck DC-DC converter for CMOS switch design, where the CMOS switch is shown as the ideal PMOS/NMOS FET with parasitic resistance $R_b$ and capacitance $C_b$. The parasitic resistance $R_b$ and capacitance $C_b$ can be written as follows,

$$C_b = W_N C_N + W_P C_P, \quad R_b = \frac{R_N}{W_N} (1 - D) + \frac{R_P}{W_P} D \quad (3),$$

where $W_N$ and $W_P$: Gate width of NMOS and PMOS FET, $C_N$ and $C_P$: Capacitance per unit gate width of NMOS and PMOS FET, $R_N$ and $R_P$: On resistance per unit gate width of NMOS and PMOS FET, $D$: On-duty ratio of high side PMOS FET, respectively, and

$$C_b = W_C, \quad R_b = \frac{R_C}{W_C}, \quad W = W_N + W_P \quad (4),$$

$$C_b = \frac{C_N + \alpha C_P}{1 + \alpha}, \quad R_b = (1 + \alpha) \left( R_N (1 - D) + \frac{1}{\alpha} R_P D \right) \quad (5),$$

$$\alpha = \frac{W_P}{W_N} \quad (6),$$

where $\alpha$ is a gate width ratio of PMOS FET and NMOS FET. In order to realize the optimal CMOS switch with small switching loss and small on-loss, the product $C_b R_b$ must be minimized by considering a trade-off relation of $C_b$ and $R_b$ related to the total gate width $W (= W_P + W_N)$. The optimal gate width ratio $\alpha_{opt}$ for minimum $C_b R_b$ can be obtained as follows:

$$\alpha_{opt} = \frac{C_N R_P D}{C_P R_N (1 - D)} \quad (7).$$

Fig. 6 Equivalent circuit of buck DC-DC converter circuit for CMOS switch design.
3.2 CMOS switch design using numerical simulation

Schrom’s optimal CMOS gate width design for the optimal efficiency buck DC-DC converter is based on an assumption on the frequency independent inductor with constant inductance and resistance versus frequency. However, in many cases, a real power inductor for a high frequency power conversion application operates as a frequency dependent device. Also, the fabricated Zn-Fe ferrite core inductor exhibits the frequency dependent characteristics as shown in Fig. 4. Therefore, the Schrom’s method could not be applied to the CMOS switch design. In order to develop the CMOS switch used for the buck DC-DC converter, in this study, a 3.3 V breakdown MOS FET has been selected and fabricated through a 180 nm CMOS process. The CMOS switch design is based on a SPICE simulation by using the equivalent circuit shown in Fig. 6, where the S parameter measured in the fabricated inductor is used as the inductor characteristics for simulation.

Target specifications of the buck DC-DC converter for the CMOS switch design are listed in Table 1 and as follows, the input voltage is 2 V, the load current is 1 A and the constant on-duty ratio $D$ of high-side PMOS FET is 0.5. In case of 3.3 V breakdown 180 nm CMOS switch, the optimal gate width ratio $\alpha_{\text{opt}}$ is 2.26 when the duty ratio $D$ is 0.5.

In this study, the CMOS switch buck DC-DC converter using the Zn-Fe ferrite core inductor has been compared with the converter using the air-core inductor with the same 2-turn spiral coil. A main reason for the selection of the 2-turn spiral coil air-core inductor for comparison is that both inductors have the same DC coil resistances though both have different inductances.

Fig. 7 shows the relationship between the total gate width $W (=W_N + W_D)$, switching frequency and total power loss of the buck DC-DC converter when $V_N$, $I_{\text{LOAD}}$, and $D$ are 2 V, 1 A and 0.5, respectively. As shown in Fig. 7(a), in case of using the Zn-Fe ferrite core inductor, the minimum power loss is obtained around the total gate width $W$ of 150 mm and switching frequency $f$ of 40 MHz. On the other hand, in case of using the air-core inductor, the minimum power loss is obtained around the total gate width $W$ of 130 mm and switching frequency $f$ of 70 MHz.

Table 2 shows the parameters of the designed CMOS switches, the switching frequencies and the expected efficiencies of two kinds of the buck DC-DC converters using the Zn-Fe ferrite core inductor and air-core inductor.

Fig. 8 shows the calculated electrical characteristics of the 2 V input CMOS switch buck DC-DC converters, where the converter circuit under simulation includes a CMOS switch gate driver. In Fig. 8(a), the output

| Item                        | Specification           | Remarks                |
|-----------------------------|-------------------------|------------------------|
| Input Voltage, $V_N$        | 2.0 V                   | ---                    |
| Load current, $I_{\text{LOAD}}$ | 1.0 A                | $D : 0.5$              |
| CMOS switch                 | 3.3 V breakdown         | 180nm CMOS             |
| Zn-Fe ferrite core inductor | 4.6 nH@50 MHz           | $R_{\text{DC}} : 25 \text{ m}\Omega$ |
| Air-core inductor           | 1.1 nH@50MHz            |                        |

Table 2 Designed parameters of 180 nm CMOS switches, optimal switching frequencies and expected conversion efficiencies of buck DC-DC converters.

| Item                        | Using Zn-Fe ferrite core inductor | Using air-core inductor |
|-----------------------------|-----------------------------------|-------------------------|
| Total gate width $W$        | 150 mm                            | 130 mm                  |
| Optimal gate width ratio $\alpha$ | 2.26                              |                         |
| Gate width $W_N$ of PMOS FET | 104 mm                            | 90 mm                   |
| Gate width $W_D$ of NMOS FET | 46 mm                             | 40 mm                   |
| Optimal switching frequency | 40 MHz                            | 70 MHz                  |
| Expected conversion efficiency | 78.8 %                            | 73.4 %                  |
voltage is estimated to be about 0.9 V at a load current of 1 A. The expected conversion efficiencies at 1 A load current are 79% in case of using the Zn-Fe ferrite core inductor and 73% in case of using the air-core inductor.

4. CMOS Switch Buck DC-DC Converter Fabricated in Organic Interposer and Its Electrical Characteristics

4.1 Fabrication of CMOS switch buck DC-DC converter

Fig. 9 shows the CMOS switch buck DC-DC converter fabricated in the organic interposer, (a) circuit diagram, (b) top view and (c) schematic cross-section. As shown in Fig. 10, a 2.5 mm-square CMOS switch LSI chip has not only PMOS/NMOS FET but also gate-drive buffer and MOS capacitors. The CMOS-LSI chip is mounted on the organic interposer using a face-down flip-chip scheme, and the 1 mm-square Zn-Fe ferrite core inductor is embedded just underneath the CMOS-LSI chip. The chip capacitors are mounted on the organic interposer. Not only chip capacitors, but also MOS capacitors are used for the DC line decoupling and output smoothing capacitor. The parallel connection of the plural capacitors can maintain low impedance in a wide frequency range.
Since the fabricated CMOS switch buck DC-DC converter has no PWM controller, the electrical characteristics have been evaluated under constant on-duty ratio $D$ of 0.5 in the high side PMOS FET.

For comparison, the CMOS switch buck DC-DC converter using the air-core spiral inductor has also been fabricated and evaluated.

### 4.2 Measured electrical characteristics

A pulse generator has been used for the external gate-pulse for PMOS/NMOS FET. Fig. 11 shows the measured electrical characteristics, where the input voltage $V_{IN}$ is 2 V, the on-duty ratio $D$ of PMOS FET is 0.5, and the conversion efficiency can be estimated by using the following equation,

$$\eta = \frac{V_{OUT}}{V_{IN}} \frac{I_{LOAD}}{I_{IN}} \quad \text{………………………………………} (8)$$

where the input power $V_{IN} I_{IN}$ includes the gate drive power for CMOS switch.

In Fig. 11(a), the output voltage decreases linearly with increasing load current, and the voltage drop is nearly independent on the switching frequency. Such tendency is confirmed in both converters using the Zn-Fe ferrite core and the air-core inductor. The voltage drop at 1 A load current is about 0.2 V, which is two times higher than the calculated one shown in Fig. 8(a). It is considered that the large voltage drop may be owing to the conductor line with parasitic resistance in the organic interposer.

In Fig. 11(b), the conversion efficiency increases gradually with increasing load current. When using the Zn-Fe ferrite core inductor, the maximum conversion efficiency at 1 A load current is about 64 % at around the switching frequency of 40-50 MHz. On the other hand, when using the air-core inductor, the maximum conversion efficiency is about 54 % at around the switching frequency of 70-80 MHz. The optimal switching frequencies are close to the simulation results shown in Table 2. However, the maximum efficiencies of 64 and 54% are considerably low compared with the simulation results.

Fig. 12 shows a typical switching waveform of the low side NMOS FET observed at the M-G point (Fig. 9(a)) in the buck DC-DC converter using the Zn-Fe ferrite core inductor, where the switching frequency is 50 MHz, the input voltage $V_{IN}$ is 2 V and the load current $I_{LOAD}$ is 1 A. The rise and fall times are about
Fig. 13 Switching dead time of NMOS FET to minimize switching loss and suppress shoot-through current.

4.3 Switching dead time of CMOS switch

To minimize the switching loss and suppress the shoot-through current of the CMOS switch, the optimal switching dead time condition has been investigated. In this study, the switching dead time has been changed for NMOS FET only. Fig. 13 shows the gate pulses CLKP, CLKN for PMOS and NMOS FET, where the Dead_time_1 means ON-timing delay and the Dead_time_2 means advanced OFF-timing of NMOS FET.

Fig. 14 shows the relationship between conversion efficiency and switching dead time of N-MOS FET in the buck DC-DC converter using the Zn-Fe ferrite core inductor when the switching frequency $f$, the input voltage $V_{IN}$, the on-duty ratio $D$ of the PMOS FET and the load current $I_{LOAD}$ are 50 MHz, 2 V, 0.5, and 1 A, respectively. The optimal Dead_time_2 for the maximum conversion efficiency is -0.05 ns. Such negative Dead_time_2 means the OFF-timing delay of NMOS FET. The conversion efficiency increases with increasing Dead_time_1 from 0.05 to 0.35 ns and decreases in the Dead_time_1 over 0.35 ns. Therefore, the optimal Dead_time_1 for the maximum conversion efficiency is 0.35 ns. Though not shown here, the optimal switching dead time effect has also been confirmed in the buck DC-DC converter using the air-core inductor.

Fig. 15 shows the best results of the optimal efficiency buck converters, (a) is the output voltage versus load current, and (b) is the conversion efficiency versus load current. The optimal switching frequencies of both buck DC-DC converters using the Zn-Fe ferrite magnetic core and the air-core inductor are 50 MHz and 90 MHz, which are close to the predicted ones in Table
2. In Fig. 15(a), the output voltage drop is about 0.19 V at 1 A load current condition.

In Fig. 15(b), the measured conversion efficiency of the buck converter using the Zn-Fe ferrite magnetic core inductor is about 68 % at 1 A load current, which is 4 % lower than the calculated one based on the SPICE simulator taking the residual parasitic resistance of the organic interposer into account. It is considered that such deviation is owing to non-linear power loss, such as iron loss under large amplitude induction in the Zn-Fe ferrite core. The main conversion efficiency excluding CMOS gate drive power of 0.1 W is about 74% when the output voltage and load current are 0.855 V and 1 A. On the other hand, the maximum conversion efficiency of the buck converter using the air-core inductor is 59 %, and the main conversion efficiency excluding CMOS gate drive power of 0.18 W is 67 % when the output voltage and load current are 0.86 V and 1 A.

5. Discussion

The most important issue in the obtained results is that the conversion efficiency is low even when the Zn-Fe ferrite inductor is used in the CMOS switch buck DC-DC converter.

A scheme to achieve the higher optimal conversion efficiency has been discussed on the basis of Schrom’s study\(^7\) for the optimal CMOS switch buck DC-DC converter. The optimal switching frequency and optimal conversion efficiency are written as follows\(^7\),

\[
 f_{\text{opt}} = \sqrt{\frac{D^2 (1 - D)^2}{3 R_c C_s \tau_L}}, \quad \eta_{\text{opt}} = \frac{1}{1 + \frac{24 R_c C_s (1 - D)}{D^2 \tau_L}} \quad \ldots \quad (9),
\]

where \(R_c\) and \(C_s\) are shown in Eq.(5), \(\tau_L\) is an inductor parameter defined as the frequency independent series inductance \(L_s\) and resistance \(R_s\),

\[
 \tau_L = \frac{L_s}{R_s} \quad \ldots \quad (10).
\]

Fig. 16 shows the relationship between optimal switching frequency, optimal conversion efficiency and the inductor parameter \(\tau_L\), where the calculation results for both 65 nm and 180 nm CMOS switch buck DC-DC converters excluding the CMOS gate driver are shown in Fig. 16. In order to obtain conversion efficiency over 80%, an inductor is required to have \(Q\) factor over 26. The \(Q\) factor must be over 57 in order to obtain conversion efficiency over 90%. Although it is not so easy to realize such a high \(Q\) factor, by using the closed magnetic circuit consisting of the Zn-Fe ferrite core and the Carbonyl-Fe/Epoxy composite core, the \(Q\) factor close to 20 can be obtained\(^6\).

In the future, the authors will investigate a novel structured inductor using novel magnetic core material in order to obtain high \(Q\) factor over 50.

\(\text{Fig. 16 Relationship between optimal switching frequency, optimal conversion efficiency and inductor parameter } \tau_L \text{ in the optimally designed CMOS switch buck DC-DC converter, where on-duty ratio } D = 0.5 \text{ in the PMOS FET.}\)

6. Conclusion

To establish a basic technology of the package-level DC power grid for the next generation power delivery to LSIs, a CMOS switch buck DC-DC converter fabricated in an organic interposer with an embedded Zn-Fe ferrite core inductor was developed and evaluated. The developed 50 MHz switching CMOS switch DC-DC buck converter with the embedded Zn-Fe inductor exhibited a power conversion efficiency of 68% and a main power conversion efficiency of 74% excluding CMOS gate drive power of 0.1 W when the input voltage, the output voltage and the load current were 2 V, 0.855 V and 1 A, respectively.

Such a low conversion efficiency is considered to be mainly owing to the low \(Q\) factor inductor. The acceptable conversion efficiency for a real application to the point-of-load power supply is required to be at least over 80%, desirably over 90%. In the future, the authors will investigate the \(Q\) factor increase by means of a novel structured inductor using novel magnetic core material.

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