Process Simulation and Characterization of Substrate Engineered Silicon Thin Film Transistor for Display Sensors and Large Area Electronics

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Abstract. Design, simulation, fabrication and post-process qualification of substrate-engineered Thin Film Transistors (TFTs) are carried out to suggest an alternate manufacturing process step focused on display sensors and large area electronics applications. Damage created by ion implantation of Helium and Silicon ions into single-crystalline n-type silicon substrate provides an alternate route to create an amorphized region responsible for the fabrication of TFT structures with controllable and application-specific output parameters. The post-process qualification of starting material and full-cycle devices using Rutherford Backscattering Spectrometry (RBS) and Proton or Particle induced X-ray Emission (PIXE) techniques also provide an insight to optimize the process protocols as well as their applicability in the manufacturing cycle.

1. Introduction
Ion beam technique is widely used as a flexible and powerful tool for material’s defect and substrate engineering [1], and Silicon ICs and transistor fabrication. The controlled introduction of implantation-induced defects is also used to tailor specific electrical and optical properties of the material and devices [2, 3]. Top gate Thin Film Transistors (TFTs) are generally manufactured by exploiting the physical characteristics of amorphous silicon films. The commercial TFTs used in Liquid Crystal Display (LCD) and Large Area Electronics (LAE) technologies have staggered bottom gate geometry with the channel passivated by SiNₓ [4]. The physical platforms (both as-grown and engineered using ion implantation technology) of the transistors are usually annealed after fabrication for device and electrical efficiency activation [4]. Fabrication of such devices is made possible with many process recipes including the coplanar amorphous-Si:H TFT on glass [5] and inverted staggered TFT with a combination of SiNₓ, a-Si:H and n+a-Si:H [6].

2. Si substrate engineered TFT: Model and Design
The TFT device design was modeled using commercially licensed SILVACO TCAD software. An inverse staggered bottom gate a-Si TFT on 200nm thick Si substrate was used as test structure to imitate a commercial device. First a layer of amorphous silicon (a-Si) followed by a 300nm Si₃N₄ layer, and 200 nm thick silicon dioxide layer, were sequentially deposited at 300°C by Plasma Enhanced Chemical Vapour Deposition (PECVD) [7-8]. Then, source and drain regions are defined using aluminum by photolithography and the oxide is etched off from these regions. Implantation of 130 keV Helium (He⁺) and 160 keV Silicon (Si) ions with doses from1×10¹³ cm⁻² to 1×10¹⁶ cm⁻² and 1.5×10¹⁵ cm⁻², was carried out at commercial implanter, respectively. During the implantation experiments, a tilt of 7°, rotation of 22 to 24 degrees and nominal room temperature was purposely maintained. The key design parameters
are summarized in Table 1, whereas the corrected, simulated and modeled TFT designs are presented in Figures 1 and 2 below.

**Table 1: Design Parameters of TFT Fabrication**

| Process Steps                                      | TFT Design parameters                                                                 |
|---------------------------------------------------|---------------------------------------------------------------------------------------|
| Platform/Substrate: Cz-Silicon                    | <100> orientation Depth 0.2um (200nm) With doping of phosphorous with sheet concentration=1.0×10^{13} cm^{-2} |
| Oxide Deposition: oxide layer(SiO₂)                | 0.20um (200nm)                                                                        |
| Etching: oxide layer(SiO₂)                        | left p1.x=2.0                                                                           |
| Nitride Deposition: (Si₃N₄)                        | 0.30um (300nm)                                                                          |
| Amorphous Silicon Definition                      | 0.20um (200nm)                                                                          |
| Substrate Engineering Implants: Implant He and Si' ions | Helium ion doses=(1×10^{13}, 1×10^{14}, 1×10^{15}, 1×10^{16}) cm^{-2} energy=130keV, Silicon dose=1.5×10^{15} cm^{-2} energy=160keV crystal tilt=7° rotation=24° |
| Source/drain contact                               | thickness=0.2um                                                                        |
| Metallization: Deposition of Aluminum (Al)        |                                                                                       |
| Etching of Aluminum (Al)                          | left p1.x=0.8, right p1.x=2.4                                                           |
| Mirror to get full structure                      | Structure defined: mirror right                                                        |
| Electrodes specifications                         | Source x=1.0 y=-0.6, Drain x=5.0 y=-0.6                                                 |

Figure 1. Tony plot of complete device: substrate engineered TFT
3. Post-process qualification of substrate engineered devices
Rutherford Backscattering (RBS) [9] and Particle/Proton Induced X-ray Emission (PIXE) [10] techniques are used for post-process qualification of devices and engineered material for possible LCD sensing and LAE applications. This is important for the qualification of our proposed design in order to address the pertaining issues in fabrication and full-cycle manufacturing of the device. Both RBS and PIXE measurements are performed in Accelerator Laboratory, National Centre for Physics, Islamabad. The general parameters used for Rutherford backscattering are shown in table 2. Standard RUMP software is used to analyze the RBS data presented in Figures 3 and 4. RBS spectra are obtained by bombarding $^4$He$^{++}$ ions with energy of 3MeV and scattering angle of 170° on N-type (Phosphorous doped; refer to Table 1) Cz-Si wafers. In the helium and silicon implanted Si wafers, no peaks are detected up to 3.5um, because helium cannot be detected with conventional RBS technique. Less than 1% concentration of phosphorus peak due to lightly doped N-type Si wafer is observed in Fig. 3 whereas the post-annealed (~900-1000°C regime) full-cycle TFT device reveals a further loss of phosphorous (owing to other dopants such as Galium to define p-type regions) to 0.5% in Fig. 4. Approximately equal amount of backscattering yield shows Gaussian distribution in device suggesting a uniform damage distribution across the active device or a pseudo-amorphized region. The calculated Kinematic factor is 0.77. The highest normalized yield is obtained at 0.31MeV at channel number 256 (refer to Fig. 3). The percentage composition of silicon is 99.5% and phosphorous is only 0.5 to 1%. The analyzing depth is 3500nm.

In the present work, PIXE analysis has been used to analyze the presence of in-situ or post-process impurities/contaminations in the device, known to affect the efficiency of electrical characteristics of the TFT and response time in display sensors. The incident beam of protons (H$^+$) of typically of
2.5MeV energy (beam size: 2mm, beam current: 3nA and charge: 5μC) is used for PIXE analysis. Si (Li) x-ray detector is used with energy resolution 180eV and detector to sample distance is about 12.5cm. Figure 5 reveals a very less amount of contaminations of Ca, Ti and Zr found in all the analyzed samples. The backscattering yield of Calcium varies from 40 to 290, Titanium ranging from 140 to 800 and Zirconium from 20 to 200. The intensity of these contaminations is very low and negligible to affect the overall device characteristics in any significant ways, as depicted in Figures 5 and 6.

Table 2: RBS Parameters used in post-qualification experiments

| Ion Beam       | He⁺⁺       |
|----------------|------------|
| Beam Energy    | 3MeV       |
| Beam Size      | 2.00mm     |
| Analyzable Elements | Be⁺ to U⁺ |
| Analyzing Depth | 3μm       |
| Charge         | 20μC       |
| Beam Current   | ≈55nA      |
| Scattering Angle | 170°     |
| Incident Angle | 7°         |
| FWHM           | 15.0KeV    |
| Sensitivity    | 10 parts per million |

Figure 3. RBS spectrum: Substrate Engineered Silicon (Starting Material with the damage implants with parameters given in Table 1)
Figure 4. RBS spectrum: Substrate Engineered Silicon TFT-Full cycle post-process annealed device (Starting Material with the damage implants with parameters given in Table 1)

Figure 5. PIXE spectrum: Substrate Engineered Silicon (Starting Material with the damage implants with parameters given in Table 1)
4. Results and Discussion

While doing RBS measurements, it provides us a chance to analyze the collision kinematics, the energy loss and analytical Rutherford cross-section. The collision kinematics, electronic part of the energy loss of the helium beam in the Si-matrix and the yield (connected to the analytical Rutherford Backscattering) refer to the mass of the constituents in the matrix (Si and P in our case), where (how deep and in what form) they are found in the substrate and how much (The content percentage), respectively.

The spectral variation in all such cases, where implantation of He$^+$ and Si$^+$ into n-type Si-wafer is carried out, is minimal up to a certain depth resolution (surface and near surface region of interest). This is valid owing the fact that the damage created due to helium implants together with the consequent damage of the lattice due to silicon implantation acted in such a balance that the whole region of interest behaved as a flat/nearby uniformed damage distribution causing a pseudo-amorphous layer exhibiting the properties of amorphous silicon material generally used for LCD/TFT environments. This is indeed a very important physical parameter while optimizing the response time in the display sensors based on TFT/LCD technologies.

The similarity of spectral variation amongst the substrate engineered devices represented reveal that the helium or silicon atoms have sufficiently created a damage which is solely responsible for the subsequent creation of the amorphized region in the active device area. The RBS resolution and channel information prove this understanding for all such cases without a single trace where the displacement/replacement caused a localized trace of evolution of crystalline region or boundary. In Fig. 4: the post process and annealed devices show a loss of phosphorous by 0.5% for relatively high thermal treatment and a slightest recovery of the amorphization region. No substantial variation is exhibited for
annealing performed at lower temperatures such as $T_{\text{anneal}}=500^\circ\text{C}$ (not shown here); which in silicon devices does not provide a defect-annihilation process window.

The combination of He$^+$ and Si$^+$ damage implants seems to be perfect way to hinder Si$^+$ from being dopant into Si-substrate either on” as-grown damage/defect sites” or because of deficient solubility in the matrix. He$^+$ is a perfect choice for attaining the right kind of damage extent to create a uniform damage profile necessary for an amorphous layer. This “engineered amorphized region” is created due to carefully designed implantation experiment by varying process parameters such as energy, selection of ion specie, fluence etc. Moreover; the extent and nature of damage caused due to physical bombardment of atoms onto the target and collision kinematics is also carefully controlled externally by the specific experimental design. The damage caused by point defects (vacancies, interstitials etc.) , any extended or complex defects (clusters, dislocation etc.) or unwanted contamination or impurities added during the various device fabrication processes play a vital role in making the TFT/LCD building blocks functional/dysfunctional and efficient/inefficient. The unnecessary and uncontrolled damage near the surface or device region badly impacts the electrical characteristics of the device (such as I-V operational trend, drain and transfer curves, sensors response time etc.) and physical electronic parameters (such as conductivity and electron/hole mobilities) be creating meta-stable defects traps leading to a large leakage current and lower life time of the carriers responsible for the efficient functioning of the device. PIXE measurements confirm that our designed implantation experiments do not create any such issues while translating the process into a junction based full cycle TFT/LCD like unit device. There are no traces of ‘Si’ or ‘He’ or ‘Si-He complex’ piled up as residual dopants/ cluster defect (agglomerated on anti-sites or start acting as impurities/defect centers) within the active device region of the substrate. The minor traces of ‘Ca’, ‘Zr’ and ‘Ti’ are process based contamination with a very low content (and that too with progressively lower yield with higher annealing temperatures as observed in Fig. 6) and hence unable to become profound in affecting the electrical characteristics of transistor (the TFT/LCD building block) by creating any substantial defect trap levels. This suggests that the designed implantation process routine may successively be used with full confidence as a “substrate engineering” technique to produce a stable amorphized region for the TFT or LCD-like device application. The combined RBS and PIXE results in direct conjunction of TCAD SILVACO results (refer to Table 1, and Figures 1 and 2 together with numerous iterations and ATLAS based simulated electrical characteristics of TFT devices which are not shown here) also suggest that the variation of the He$^+$ implant doses within acceptable fluence regions of $1 \times 10^{13} \text{ion/cm}^2$ and $1 \times 10^{16} \text{ion/cm}^2$ play a decisive role in the adjustment of the controllable damage extent (using annealing as process routine for subsequent process steps where a higher or lower value of such damage extent is required). The medium to slightly higher concentration of interstitials up to a certain depth (owing the fact that helium ions with varying doses are impinged onto the n-type Si substrate at a given energy) can be achieved and controlled with respect to the derived physical or electrical device characteristics.

The effect of helium implantation with theses carefully chosen parameters is important to create a “depth specific”, “controlled and almost uniform damage profile” acting as an amorphized layer which may be reversible to crystalline undergoing the annealing process, if required. The effect of Si-implantation is also vital to control the nature of aforementioned damage as it is evident that the persistent damage in this case is not of interstitials but vacancies, which play an important role while determining the desirable mobility of free carriers in the device at any given depth and process temperature. Thus both He$^+$ and Si$^+$ implants owing the roles of interstitials (with changing depth profile) and vacancies (with an ability to be mobile in great deal from surface to bulk and vice-versa) seem necessary to engineer the substrate in a way to alter the n type surface/near surface region into a pseudo-amorphized region highly suitable for TFT fabrication and consequent applications.
5. Conclusion
Ion implantation induced damage of silicon substrate particularly by implantation of Si$^+$ and He$^+$ ions into the Si-matrix is studied to evaluate and optimize the process control for TFT applications in Large Area Electronics and Display Sensing Technologies. The substrate engineering protocol was also utilized in the conventional TFT device design to ascertain its applicability in the manufacturing process. Post-processing characterization tools such as RBS and PIXE were also focused to evaluate the scope of “precisely controlled” and “fully design optimized” substrate-engineered TFT devices in the real fabrication environment. The process-altered design recipe of such TFT devices may prove to be useful in special reference to the control on the efficiency and response specific physical characteristics of the devices used in display sensors and consumer electronics industry.

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