High mobility Ge pMOSFETs with amorphous Si passivation: impact of surface orientation

Huan Liu¹, Genquan Han¹*, Yan Liu¹, Xiaosheng Tang², Jingchen Yang¹ and Yue Hao¹

Abstract

We report the amorphous Si passivation of Ge pMOSFETs fabricated on (001)-, (011)-, and (111)-orientated surfaces for advanced CMOS and thin film transistor applications. Amorphous Si passivation of Ge is carried out by magnetron sputtering at room temperature. With the fixed thickness of Si $t_{Si}$, (001)-oriented Ge pMOSFETs achieve the higher on-state current $I_{ON}$ and effective hole mobility $\mu_{eff}$ compared to the devices on other orientations. At an inversion charge density $Q_{inv}$ of $3.5 \times 10^{12} \text{cm}^{-2}$, Ge(001) transistors with 0.9 nm $t_{Si}$ demonstrate a peak $\mu_{eff}$ of 278 cm²/V · s, which is 2.97 times higher than the Si universal mobility. With the decreasing of $t_{Si}$, $I_{ON}$ of Ge transistors increases due to the reduction of capacitive effective thickness, but subthreshold swing and leakage floor characteristics are degraded attributed to the increasing of midgap $D_{it}$.

Keywords: Germanium, MOSFET, Amorphous Si passivation, Mobility, Surface orientation

Background

Germanium (Ge) has been attracting tremendous research interests for advanced CMOS and thin film transistor applications due to its higher hole mobility and lower thermal budget processing compared to Si [1–6]. To achieve the high channel mobility, the surface passivation process leading to a high interface quality is required before gate stack formation. Several surface passivation techniques have been developed to deliver the carrier mobility benefits in Ge metal-oxide-semiconductor field-effect transistors (MOSFETs) [1, 2, 7–10]. Among these techniques, a silicon (Si) cap passivated on Ge has been the hotspot in recent years, due to its advantages of effective suppressing of interface states and good thermal stability and reliability [11]. Formation of Si passivation cap has been widely studied using chemical vapor deposition (CVD) with precursors of SiH₄ [1], Si₂H₆ [4], Si₃H₈ [12], and E-beam evaporation [13]. Although CVD method could provide the more uniform passivation layer over physical vapor deposition (PVD), its passivation rate has the strong correlation in channel surface orientation and the process temperature. PVD technique could provide the improved passivation rate even at room temperature, which has the advantages of low thermal budget and low cost, making it more suitable for the thin film transistors and back-end-of-line 3D integration applications. In this letter, we fabricated high mobility Ge pMOSFETs on (001)-, (011)-, and (111)-oriented surfaces utilizing amorphous Si passivation by magnetron sputtering. Significantly improved effective hole mobility $\mu_{eff}$ is achieved in Ge transistors compared to the Si universal mobility. Impacts of surface orientation and thickness of amorphous Si $t_{Si}$ on the boosting effect of amorphous Si passivation on $\mu_{eff}$ are studied.

Methods

Figure 1a shows the key process steps for fabricating Ge pMOSFETs on (001)-, (011)-, and (111)-orientated surfaces. After pre-gate cleaning in diluted HF (1:50) solution, ultrathin amorphous Si passivation layer over physical vapor deposition (PVD), its passivation rate has the strong correlation in channel surface orientation and the process temperature. PVD technique could provide the improved passivation rate even at room temperature, which has the advantages of low thermal budget and low cost, making it more suitable for the thin film transistors and back-end-of-line 3D integration applications. In this letter, we fabricated high mobility Ge pMOSFETs on (001)-, (011)-, and (111)-oriented surfaces utilizing amorphous Si passivation by magnetron sputtering. Significantly improved effective hole mobility $\mu_{eff}$ is achieved in Ge transistors compared to the Si universal mobility. Impacts of surface orientation and thickness of amorphous Si $t_{Si}$ on the boosting effect of amorphous Si passivation on $\mu_{eff}$ are studied.
TaN gate electrode was deposited by reactive sputtering. Next, the gate electrode was patterned and etched, which was followed by BF$_2$+ implantation into source/drain (S/D) regions at 30 KeV with a dose of $1 \times 10^{15}$ cm$^{-2}$. Non-self-aligned S/D metals of 15-nm nickel were formed by lift-off process. Finally, rapid thermal annealing at 400 °C was carried out for dopant activation and S/D metallization. Figure 1a shows the cross-sectional schematic of the Ge pMOSFET with Si/SiO$_2$ interfacial layer (IL). Figure 1b shows top-view microscope image of a fabricated Ge pMOSFET.

Results and discussion

Figure 3a plots the measured $I_{DS} - V_{GS}$ and $I_{G} - V_{GS}$ curves of the typical Ge pMOSFETs on (001)-, (011)-, and (111)-oriented surfaces with 0.9 nm $t_{Si}$, which show the excellent transfer characteristics. All transistors have a gate length $L_G$ of 3 µm and a gate width $W$ of 100 µm. The channel direction is [110] for all the orientations. The $I_{DS} - V_{DS}$ curves of the devices measured at different gate overdrive $V_{GS} - V_{TH}$ are shown in Fig. 3b. Here, threshold voltage $V_{TH}$ is defined as the $V_{GS}$ at $I_{DS}$ of $10^{-7}$ A/µm. It is observed that Ge(001) pMOSFET achieves the higher drive current $I_{ON}$ compared to the transistors on (011) and (111) surfaces at the fixed $V_{GS} - V_{TH}$. Later, we will show that this is attributed to the fact that Ge(001) pMOSFETs have a higher effective hole mobility $\mu_{eff}$ in comparison with the devices on the other two surface orientations. We perform a comprehensive comparison of electrical performance for the devices with the fixed $t_{Si}$ of 0.9 nm, including $I_{ON}$, leakage floor $I_{leak}$, subthreshold swing (SS), and $V_{TH}$ characteristics. $I_{leak}$ is defined as the minimum $I_{DS}$ at $V_{DS}$ of $-0.05$ V. Figure 4a presents the statistical plot of the $I_{ON}$ for Ge pMOSFETs on various orientations, and $I_{ON}$ was defined as $I_{DS}$ at a $V_{DS}$ of $-0.5$ V and a $V_{GS} - V_{TH}$ of $-0.8$ V. All the transistors in this plot have the $L_G$ of 3 µm and $W$ of 100 µm. (001)-oriented devices exhibit the improved mean $I_{ON}$ as compared to those on (011) and (111) orientations, which is attributed to the higher $\mu_{eff}$. Figure 4b compares the $I_{leak}$ for the devices, showing that Ge(001) transistors have the lowest $I_{leak}$ of them, and Ge(011) pMOSFETs have the lower $I_{leak}$ than...
(111)-oriented devices. It should be noted that the $I_{\text{leak}}$ is determined by the reverse current of the $p^+$/n junction in drain region, which is affected by the background n-type doping concentration in Ge substrate and activation of the implanted $p^+$ dopants. The n-type doping concentrations in the wafers with various orientations are not exactly the same. The surface orientation affects the dopant activation rate and recrystallization quality of S/D regions. Furthermore, although the $I_G$ is lower than $I_{DS}$ before the turn-on of the transistors, it would influence the $I_{\text{leak}}$. Similarly, (001)-oriented Ge pMOSFETs demonstrate the improved SS characteristics in comparison with other two orientations, which is due to that transistors on (001) surface have the lower midgap density of interface state $D_{it}$ compared to the other devices. Figure 4d shows that the devices on different orientations have the different $V_{\text{TH}}$. Based on the results in Fig. 4, it is concluded that, with the fixed $t_{Si}$ of 0.9 nm, (001)-oriented Ge pMOSFETs obtain the best electrical characteristics.

The thicknesses of Si/SiO$_2$ IL in transistors with 0.9 nm $t_{Si}$ on different surface orientations are studied by using inversion capacitance $C_{inv}$ versus $V_{GS}$ measurement, as shown in Fig. 5. Forward and reverse sweeping measurements exhibit the negligibly small hysteresis in the devices. The transistors exhibit the similar magnitude of $C_{inv} \approx 1.56 \mu \text{F/cm}^2$, corresponding to the capacitive effective thickness (CET) of 2.2 nm. Figure 5b show the statistical results of saturated $C_{inv}$ for the devices, which demonstrate the very small difference in $C_{inv}$ in the transistors on different surface orientations. This indicates that the passivation rate of amorphous Si by magnetron sputtering is independent of the surface orientation. The rule of left-right shifts of the $C_{inv}$-$V_{GS}$ curves is well consistent with that of $V_{\text{TH}}$ for the devices in Fig. 4d, which might be induced by the slightly different doping concentration in different orientation substrates.

Figure 6 compares the mobility characteristics of the transistors with 0.9 nm $t_{Si}$ on various surface orientations. The $\mu_{\text{eff}}$ was extracted using a total resistance slope-based method [14]. Ge(001) pMOSFETs exhibit the much higher channel mobility compared to the devices on (011) and (111) orientations. Transistors on (001) substrate achieve a peak $\mu_{\text{eff}}$ of 278 cm$^2$/V·s at an inversion charge density $Q_{\text{inv}} \approx 3.5 \times 10^{12}$ cm$^{-2}$, which is 2.97 times higher than the Si universal mobility. Surface roughness at the Si/Ge interface and density of interface states ($D_{it}$) can affect $\mu_{\text{eff}}$ of the devices at high inversion carrier density. It is unlikely that the commercially purchased Ge wafers with various surface orientations have the obvious difference in surface roughness. Therefore, it is speculated that the mobility enhancement in (001)-oriented devices is mainly due to reduced carrier scattering contributed by interface states in this work, we evaluate the midgap $D_{it}$ of the devices, and with the fixed $t_{Si}$ of 0.9 nm, the (001)-oriented Ge pMOSFETs indeed have the lower midgap $D_{it}$ compared to the other orientations.

The impact of $t_{Si}$ on the electrical performance of Ge pMOSFETs is also investigated. Figure 7a, b present the measured $I_{DS}$-$V_{GS}$ and $I_{DS}$-$V_{DS}$ curves, respectively, of the (111)-oriented Ge pMOSFETs with $t_{Si}$ of 0.5, 0.7, and 0.9 nm at a $V_{DS}$ of −0.05 and −0.5 V. The transistors have a $L_G$ of 1.5 μm. It is observed that Ge pMOSFETs with 0.9 nm $t_{Si}$ exhibit improved transfer characteristics compared to the devices with thinner $t_{Si}$, but $I_{\text{ON}}$ of the device decreases with the increasing of $t_{Si}$. At $V_{DS}$ of −1.5 V and $V_{GS}$-$V_{TH}$ of −0.8 V, Ge(111) pMOSFET with 0.5 nm $t_{Si}$ demonstrates a 32% improvement in $I_{\text{ON}}$ compared to the device with 0.9
Fig. 4 Comparison of a $I_{ON}$, b $I_{leak}$, c SS, and d $V_{TH}$ for (001)-, (011)-, and (111)-oriented Ge pMOSFETs with a $t_{Si}$ of 0.9 nm.

Fig. 5 a Comparison of inversion $C_{inv}$-$V_{GS}$ curves among the Ge pMOSFETs with 0.9 nm $t_{Si}$ on different orientations. Both forward and reverse sweeping are shown. b Statistical plots for the saturated $C_{inv}$ of the devices showing the negligible differences in $C_{inv}$ in the inversion regime.
Figure 8 plots the statistical results of $I_{\text{ON}}$, $I_{\text{leak}}$, SS, and $V_{\text{TH}}$ of the Ge pMOSFETs on (111)-orientation with different $t_{\text{Si}}$. From Fig. 8a, we see that transistors with 0.5 nm $t_{\text{Si}}$ achieve the improved $I_{\text{ON}}$ in comparison with the devices with thicker $t_{\text{Si}}$, which is due to the transistor with 0.5 nm $t_{\text{Si}}$ that has a smaller CET, leading to a higher $C_{\text{inv}}$. It is noticed that $I_{\text{leak}}$ decreases with the increasing of $t_{\text{Si}}$ (Fig. 8b), and transistors with 0.5 nm $t_{\text{Si}}$ has the inferior SS characteristics to those of the devices with 0.7 and 0.9 nm amorphous Si passivation layer (Fig. 8c). This might be due to those transistors with 0.5 nm $t_{\text{Si}}$ having a higher midgap $D_{\text{it}}$. The relation between SS and midgap $D_{\text{it}}$ of Ge pMOSFETs can be expressed by

$$SS = \ln(10) \cdot \left(\frac{kT}{q}\right) \cdot \left[1 + \left(\frac{C_{\text{it}} + C_{\text{d}}}{C_{\text{ox}}}\right)\right]$$

where $C_{\text{ox}}$, $C_{\text{d}}$, and $C_{\text{it}}$ are oxide capacitance, depletion-layer capacitance, and capacitance from interface traps, respectively. $C_{\text{it}}$ can be calculated by $q \times D_{\text{it}}$, where $D_{\text{it}}$ is the interface trap density. Although transistor

![Figure 6](image-url)  
Fig. 6 Plot of $\mu_{\text{eff}}$ versus $Q_{\text{inv}}$ for Ge pMOSFETs with 0.9 nm $t_{\text{Si}}$ on (001)-, (011)-, and (111)-oriented substrates. Ge(001) pMOSFETs achieve the 2.97 times enhancement in $\mu_{\text{eff}}$ at a $Q_{\text{inv}}$ of $3.5 \times 10^{13}$ cm$^{-2}$ as compared to the Si universal mobility. The $\mu_{\text{eff}}$ was extracted using a total resistance slope-based method [17].

![Figure 7](image-url)  
Fig. 7 a $I_{\text{DS}}$-$V_{\text{GS}}$ and $I_{\text{G}}$-$V_{\text{GS}}$ and b $I_{\text{DS}}$-$V_{\text{DS}}$ curves of Ge(111) pMOSFETs with various $t_{\text{Si}}$. Transistor with 0.5 nm $t_{\text{Si}}$ exhibits a 32% improvement in $I_{\text{ON}}$ compared to the device with 0.9 nm $t_{\text{Si}}$ at $V_{\text{GS}}$ of $-1.5$ V and $V_{\text{G}}$-$V_{\text{TH}}$ of $-0.8$ V.
with 0.5 nm $t_{Si}$ has the larger $C_{ox}$ compared to the other two devices, its higher midgap $D_{it}$ can lead to the inferior SS to the devices with the thicker $t_{Si}$. The surface passivation will also affect the $I_{leak}$ from drain to source. With the sweeping of $V_{GS}$ from position to negative, the channel transfers from accumulation mode to inversion mode. However, if the $D_{it}$ is high, some points in channel surface are pinned by the interface traps, and the leakage paths can be formed, increasing $I_{leak}$ from drain to source. As shown in Fig. 8d, Ge(111) pMOSFETs show the shift of $V_{TH}$ to negative $V_{GS}$ direction with the increasing of $t_{Si}$ which is attributed to the increased CET. In addition, the density of traps in the lower bandgap half seems to increase for the thinner $t_{Si}$ which might lead to the shift of $V_{TH}$ [2].

Figure 9a shows the $C_{inv}$ as a function of $V_{GS}$ curves for the Ge pMOSFETs on (111)-oriented surface with $t_{Si}$ of 0.5, 0.7, and 0.9 nm measured at a frequency of 300 kHz. The CET values in inversion regions are extracted to be 1.8, 1.9, and 2.2 nm for the devices with 0.5, 0.7, and 0.9 nm $t_{Si}$ respectively. $\mu_{eff}$ as a function of $Q_{inv}$ characteristics of the devices are extracted and shown in Fig. 9b. The (111)-oriented Ge pMOSFET with 0.7 nm $t_{Si}$ achieves the highest peak mobility of 229 cm$^2$/V s, which is 2.27 times higher compared to the Si universal mobility. It should be noted that the devices with 0.5 nm $t_{Si}$ exhibit a significantly improved $\mu_{eff}$ over the transistors with thicker $t_{Si}$ at high $Q_{inv}$ (e.g. $10^{13}$ cm$^{-2}$). This also leads to the higher $I_{ON}$ at high $V_{GS}$-$V_{TH}$ in the devices with 0.5 nm $t_{Si}$ compared to the devices with 0.7 and 0.9 nm $t_{Si}$. The $\mu_{eff}$ at high $Q_{inv}$ decreases as $t_{Si}$ increases from 0.5 nm to 0.7~0.9 nm, which is attributed to the fact that the larger surface roughness leads to the stronger surface roughness scattering of the carriers. During the passivation of Ge surface using magnetron sputtering at room temperature, the diffusion of surface atoms is greatly suppressed. So with the increasing of $t_{Si}$, the surface roughness is larger, which can be observed from the HRTEM images in Fig. 2.
In Fig. 10, we benchmark the $\mu_{\text{eff}}$ of the Ge pMOSFETs in this work with those of the reported relaxed Ge transistors with Si by E-beam evaporation, SiH$_4$, Si$_2$H$_6$, and Si$_3$H$_8$ passivation. Compared to the amorphous Si by E-beam evaporation in Ref. [15], Ge pMOSFETs in this work exhibit the significantly improved $\mu_{\text{eff}}$. It is seen that, at the similar CET, Ge pMOSFETs utilizing amorphous Si passivation by magnetron sputtering have the lower $\mu_{\text{eff}}$ in comparison with the devices with Si$_2$H$_6$ passivation. The process of passivation using amorphous Si needs to be further optimized to enhance the carrier mobility.

Ge pMOSFETs with the different $t_{\text{Si}}$ on (001)-oriented surface are also characterized. Figure 11a, b illustrate the measured $I_{DS}$-$V_{GS}$ and $I_{DS}$-$V_{DS}$ curves, respectively, of a pair of Ge(001) pMOSFETs with 0.5 and 0.9 nm $t_{\text{Si}}$. Similar to the (111)-oriented devices, Ge(001) pMOSFET with 0.5 nm $t_{\text{Si}}$ obtains the improvement in $I_{\text{ON}}$ but the degradation in $I_{\text{leak}}$ compared to the transistor with 0.9 nm $t_{\text{Si}}$.

The midgap $D_{\text{it}}$ characteristics of Ge pMOSFETs are studied by the method in [16], and values of $D_{\text{it}}$ are calculated by $D_{\text{it}} = [\text{SSlog}(e)/(kT/q) - 1]C_G/q$, [16] where $q$ is the electron charge, $k$ is Boltzmann’s constant, $T$ is the absolute temperature, and $C_G$ is the measured gate capacitance per unit area. Figure 12 shows $D_{\text{it}}$ as a function of the thickness of amorphous Si with various Ge surface orientations. For (111)-oriented surface, a device with 0.7-nm $t_{\text{Si}}$ has the lowest $D_{\text{it}}$ value. With the 0.9 nm $t_{\text{Si}}$, (001)-oriented device has the lower $D_{\text{it}}$ compared to the transistors on other orientations.

---

**Fig. 9** a $C_{\text{inv}}$-$V_{GS}$ characteristics measured at 300 kHz for (111)-oriented devices with 0.5, 0.7, and 0.9 nm $t_{\text{Si}}$. b $\mu_{\text{eff}}$ as a function of $Q_{\text{inv}}$ for Ge pMOSFETs [17].

**Fig. 10** a $\mu_{\text{eff}}$ for the Ge pMOSFETs in this work vs. the published results for relaxed Ge pMOSFETs. b, c Benchmarking of $\mu_{\text{eff}}$ extracted at $Q_{\text{inv}} = 5 \times 10^{12}$ and $1 \times 10^{13}$ cm$^{-2}$, respectively, of the Ge pMOSFETs with the different CET values [18, 19].
Finally, we compare the key electrical characteristics of Ge pMOSFETs on the different orientations in Table 1. With a fixed $t_{Si}$, Ge(001) pMOSFET has the improved electrical performance compared to the other two orientations. The drive current can be enhanced by reducing the $t_{Si}$ from 0.9 nm to 0.5 nm, which is due to that the thinner $t_{Si}$ provides a significantly reduced CET without causing degradation in $\mu_{eff}$.

**Conclusions**

Ge pMOSFET passivated by amorphous Si are demonstrated on (001)-, (011)-, and (111)-oriented substrate. With a $t_{Si}$ of 0.9 nm, the improved $I_{ON}$ and SS characteristics are obtained in (001)-oriented Ge pMOSFETs in comparison with the devices on (011) and (111) orientations, due to the higher $\mu_{eff}$ and lower midgap $D_{it}$. Ge(001) pMOSFETs with 0.9 nm $t_{Si}$ achieve a peak...
mobility of 278 cm²/V s at a \( Q_{\text{inv}} \) of 3.5 \( \times 10^{12} \) cm⁻², which is 2.97 times higher than the Si universal mobility. It is demonstrated that \( I_{\text{ON}} \) of the devices is improved with the decreasing of \( t_{\text{Si}} \) due to the reduction of CET. But Ge pMOSFETs with thicker \( t_{\text{Si}} \) exhibit the superior subthreshold swing and leakage floor, owing to the mid-gap \( D_{\text{it}} \) can be reduced by increasing \( t_{\text{Si}} \).

### Abbreviations
- ALD: Atomic layer deposition; BF²⁺: Boron fluoride ion; CET: Capacitive effective thickness; Ge: Germanium; GeOₓ: Germanium oxide; HF: Hydrofluoric acid; HfO₂: Hafnium dioxide; HRTEM: High-resolution transmission electron microscope; IL: Interfacial layer; MOSFETs: Metal-oxide-semiconductor field-effect transistors; Ni: Nickel; Si: Silicon; SS: Subthreshold swing; TaN: Tantalum nitride; TDMAHf: Tetrakis (dimethylamido) hafnium

### Acknowledgements
Not applicable.

### Funding
The authors acknowledge support from the National Natural Science Foundation of China under Grant No. 61534004, 61604112, and 61622405.

### Availability of data and materials
The datasets supporting the conclusions of this article are included within the article.

### Authors’ contributions
HL carried out the experiments and drafted the manuscript. GQH and YL supported the study and helped to revise the manuscript. XST and JCY helped to carry out the measurements. YH provided constructive advice. All the authors read and approved the final manuscript.

### Competing interests
The authors declare that they have no competing interests.

### Publisher’s Note
Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

### Author details
1. State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi’an 710071, China. 2. College of Optoelectronic Engineering, Chongqing University, Chongqing 400044, China.

### Received
28 September 2018 Accepted: 26 December 2018 Published online: 08 January 2019

### References
1. Wu N, Zhang Q, Zhu C, Chan DSH, Du A, Balasubramanian N, Li MF, Chin A, Sin JKO, Kwong DL (2004) A TaN-HfO₂-Ge pMOSFETs with novel SiH₄ surface passivation. IEEE Electron Device Lett 25:631–633
2. Mitard J, Jaeger BD, Leys FE, Hellings G, Martens K, Eneman G, Brunco DP, Loo R, Lin IC, Shamiryan D, Vandeveney T, Winderickx G, Vanclavc E, Yu CH, Meyer KD, Caymax M, Pantisano L, Meurs M, Heys MW (2008) Record \( I_{\text{ON}}/I_{\text{OFF}} \) performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability. In: IEDM Tech Dig, pp 873–876 https://doi.org/10.1109/IEDM.2008.4796837
3. Vincent B, Loo R, Vandervorst W, Delmotte J, Douhard B, Valey VK, Vanbel M, Verbeist T, Rip J, Brijs B, Conard T, Claypool C, Takeuchi S, Zaina S, Mitard J, Jaeger BD, Dekoster J, Caymax M (2011) Si passivation for Ge pMOSFETs: impact of Si cap growth conditions. Solid State Electron 60:116–121
4. Liu Y, Yan J, Han GQ, Wang HJ, Liu MS, Zhang CF, Cheng BW, Hao Y (2014) Strained Ge/Si/SiO₂/Ge p-MOSFETs with in situ low temperature SiH₄ surface passivation. In: IEDM Tech Dig, pp 107–108 https://doi.org/10.1109/IEDM.2014.6874637
5. Liao CY, Chen SH, Huang WH, Shen CH, Shiai JM, Cheng HC (2018) High-performance recessed-channel germanium thin-film transistors via excimer laser crystallization. IEEE Electron Device Lett 39:367–370
6. Sadot T, Kamizuru H, Kenjo A, Miyao M (2006) Low-temperature formation (< 500 °C) of poly-Ge thin-film transistor with NiGe Schottky source/drain. Appl Phys Lett 89:192–114
7. Xie R, Phung TH, He W, Sun Z, Yu M, Cheng Z, Cui H (2008) High mobility high-k/Ge pMOSFETs with 1 nm EOT-new concept on interface engineering and interface characterization. In: IEDM Tech Dig, pp 1–4 https://doi.org/10.1109/IEDM.2008.4976073
8. Takagi S, Noguchi M, Kim M, Kim SH, Chang CY, Yokoyama M, Nishi K, Zhang R, Ke M, Takenaka M (2016) III-V/Ge MOS device technologies for low power integrated systems. Solid State Electron 125:82–102
9. Kuzum D, Pethe AJ, Krishnamohan T, Sarwat KS (2009) Ge (100) and (111) N- and P-FETs with high mobility and low-T mobility characterization. IEEE Trans Electron Devices 56:648–655
10. Hashemi P, Hoyt JL (1998) Field effect devices and applications: devices for portable, high-performance recessed-channel germanium thin-film transistors via excimer laser crystallization. IEEE Electron Device Lett 33:173–175
11. Kazcer B, Franco J, Mitard J, Roussel PJ, Veloso A, Groeseneken G (2009) Improvement in NBi reliability of Si-passivated Ge/high-k/metal-gate pFETs. Microelectronic Eng 86:1582–1584
12. Mitard J, Martens K, Jaeger BD, Franco J, Shee C, Plourde C, Leys FE, Lin IC, Kazcer B, DeMeyer K, Hoffmann T, DeGendt S, Caymax M, Meurs M, Heys MS (2009) Impact of epi-Si growth temperature on Ge-pFET performance. In: European Solid State Device Research Conference, pp 411–414 https://doi.org/10.1109/ESSDERC.2009.5331351
13. Chen WB, Chin A (2010) High performance of Ge nMOSFETs using SiO₂ interfacial layer and TiLaO gate dielectric. IEEE Electron Device Lett 31:80–82
14. Niu G, Cressler JD, Mathew SJ, Subbanna S (1999) A total resistance slope of poly-Si gate-Ge Schottky source/drain. Jpn J Appl Phys 38:108–114
15. Lee CH, Nishimura T, Tabata T, Wang SK, Nagashio K, Kita K, Toriumi A (2010) Ge MOSFETs performance: impact of Ge interface passivation. In: IEDM Tech Dig, pp 416–419 https://doi.org/10.1109/IEDM.2010.5703384
16. Greve DW (1998) Field effect devices and application: devices for portable, low-power, and imaging systems, 1st edn. Prentice-Hall, Englewood
17. Takagi S, Twaes M, Toriumi A (1998) On the universality of inversion-layer mobility in n- and p-channel MOSFETs. In: IEDM Tech Dig, pp 398–401 https://doi.org/10.1109/IEDM.1998.732840
18. Pillarisetty R, Chu-Kung B, Concoran S, Dewey G, Kavaleros J, Kennel H, Kotlyar R, Le V, Lionberger D, Metz M, Mukherjee N, Nah J, Rachmady W, Radosavljevic M, Shah U, Taft S, Then H, Zelick N, Chau R (2010) High mobility strained germanium quantum well field effect transistor as the p-channel device option for low power (V_{dd} = 0.5 V) III-V CMOS architecture. In: IEDM Tech. Dig, pp 150–153 https://doi.org/10.1109/IEDM.2010.5703312

19. Mitard J, Witters L, Vincent B, Franco J, Eavia P, Hikavyy A, Eneman G, Loo R, Brunco DP, Kabir N, Bender H, Sebaai F, Vos R, Mertens P, Milenin A, Vecchio E, Ragnarsson L-Å, Collaert N, Thean A (2013) First demonstration of strained Ge-in-STI IFQW pFETs featuring raised SiGe75% S/D, replacement metal gate and germanided local interconnects. In: VLSIT Dig, pp T20–T21