Predictive Direct Torque Control Application-Specific Integrated Circuit with a Fuzzy Proportional–Integral–Derivative Controller and a New Round-Off Algorithm

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ABSTRACT This study developed a predictive direct torque control (PDTC) application-specific integrated circuit (ASIC) with a fuzzy proportional–integral–derivative (PID) controller and a new round-off calculation circuit for improving the ripple response of a hysteresis controller when sampling and calculating delay times in an induction motor drive. The proposed PDTC ASIC not only calculates the stator’s magnetic flux and torque by detecting three-phase currents, three-phase voltages, and rotor speed but also eliminates large ripples in the torque and flux by using the fuzzy PID controller. Furthermore, the proposed round-off algorithm reduces the calculation error of the composite flux. A fuzzy voltage vector switching table is proposed not only to speed up the calculating speed but also to resolve the instability generated by its large torque and flux ripples. The Verilog hardware description language was used to implement the hardware architecture, and the aforementioned ASIC was fabricated using the 0.18-μm 1P6M CMOS process of the TSMC by employing the cell-based design method. The predictive calculations, fuzzy PID controller, fuzzy voltage vector switching table, and round-off calculation algorithm improved not only the ripple issue faced in traditional direct torque control but also the control stability and robustness. The measurement results indicate that the proposed PDTC ASIC has an operating frequency, a sampling rate, and a dead time of 50 MHz, 100 kHz, and 100 ns, respectively, at a supply voltage of 1.8 V. The power consumption and chip area of this ASIC are 1.0027 mW and 1.169 × 1.168 mm2, respectively. The main advantages of the proposed PDTC ASIC are its low power consumption, small chip area, robustness, and convenience.

INDEX TERMS Direct torque control (DTC), Predictive calculation, fuzzy PID controller, round-off algorithm, application-specific integrated circuit (ASIC), induction motor (IM), hardware description language (HDL).

I. INTRODUCTION Direct torque control (DTC) schemes can produce rapid and robust responses; however, they usually perform similar to a hysteresis controller with low switching frequencies. In [1], two schemes were investigated to modify the classical DTC method. A new approach was presented to compensate for torque ripples by referring to the tolerance band around the command torque. The best results were obtained with 25% of the applied voltage compensating for the voltage drops within the motor drive. Next, a predictive algorithm was used to command the flux value for reducing the torque ripple of the IM drive. Experimental results confirmed that the switching frequency remained constant and that the torque ripple was improved with two schemes [1]. However, a DTC system with a traditional proportional–integral–derivative (PID) controller cannot easily exhibit ideal performance because the IM drive performs with multivariable, strong-coupling, nonlinear, and time-varying characteristics [2]. A
fuzzy logic PID regulator for motor speed was proposed in [2] to adjust the nonlinear control variables. Compared with a conventional PID controller, the aforementioned controller provides superior performance in terms of dynamic response and static deviation in a DTC system [2]. Furthermore, a novel model predictive direct torque control (MPDTC) scheme was proposed in [3] for maintaining the motor torque, stator flux, and inverter’s neutral point potential within the given hysteresis bounds while minimizing the switching frequency of the inverter. Specifically, compared with the standard DTC scheme, the aforementioned scheme reduces the switching frequency by up to 50% while maintaining the torque and flux more accurately within their bounds [3]. Moreover, compared with the standard DTC scheme, the proposed MPDTC scheme reduces the inverter switching frequency by 16.5% on average (over the entire operating range) and up to 37.4% under specific operating conditions [4]. The results in [4] prove that computational control solutions are becoming computationally and economically feasible and that versatile and flexible control algorithms can be developed for electric motor drives with favorable performance.

A new quick-response and high-efficiency control method for an IM was proposed in [5]. This method is based on the limit cycle control of the flux and torque by using the optimum pulse-width-modulated (PWM) output voltage, which can be achieved by controlling the amplitude of the flux according to the torque command. The aforementioned approach is superior to the corresponding field-oriented control method. The control circuit used in the aforementioned method can be compensated easily and automatically to minimize the effect of the variation of machine constants [5]. In practice, DTC is achieved using a two-level voltage source inverter that requires limited computation time and can be implemented without mechanical speed sensors. However, DTC based on hysteresis controllers suffers from certain drawbacks such as variable switching frequency and high torque ripple [6]. A DTC scheme with a constant switching frequency was proposed in [6] according to the concept of imaginary switching time. Simulation results indicate that the performance of classical DTC can be improved using a voltage modulation scheme with a constant switching frequency. The imaginary switching vector designed in [6] requires low memory and a short computation time.

An improved DTC scheme based on the fuzzy logic technique was developed in [7]. This scheme not only reduces the torque and flux ripples but also improves the performance of a DTC drive system. The control algorithm of the aforementioned scheme is based on the space vector modulation (SVM) technique so that a constant inverter switching frequency can be obtained. Furthermore, an MPDTC scheme was developed in [8] as an alternative control strategy for permanent magnet synchronous motor drives. This control strategy is based on the control model system, prediction components, and optimization problem [8]. MPDTC is a complicated control scheme because it computes the stator flux reference and predicts the stator flux in the next cycle. The MPDTC scheme can improve the speed tracking performance of a DTC system and its robustness against disturbance and uncertainties [8].

Despite the increasing interest in the use of multiphase drives for fault-tolerant applications [9]–[11], three-phase machines remain dominant in industrial applications. Various fault-tolerant, three-phase motor drive topologies have been developed, and their performances have been investigated by considering the effects of current and voltage limits for the inverter and machine. In the evaluation of the postfault power of a fault-tolerant drive, the postfault torque and speed, which depend on the postfault current and voltage limits, should be considered [12]. However, the gains in postfault torque and power depend on machine parameters, which are floating-point numbers. A tariff plan is recommended to not only eliminate the rounding-off error completely but also reduce the floating-point-number operations [13]. Furthermore, two models have been proposed for reducing the rounding-off error in fixed-point arithmetic. The first model is a generic model with no assumptions on the predicted system or weight matrices, and the second model is a parametric model that exploits the Toeplitz structure of the linear model predictive control (MPC) problem for a Schur stable system. Experimental results obtained using the aforementioned two models indicate that they significantly reduce the resource usage, computational energy, and execution time of a field-programmable gate array (FPGA) [14]–[15]. To minimize torque ripples, a heuristic-based optimization technique was applied in [16]–[17] to an IM model. Next, the feasibility condition for the design parameters was checked, and the optimized design parameters were rounded off to the nearest feasible design values. The torque ripple was reduced to a negligible value in the optimized machine model [16].

The Model predictive control (MPC) is a popular and effective technique to fulfill high drive performance in electrical machines and systems. The finite control set model predictive control (FCS-MPC) [18], continuous control set model predictive control (CCS-MPC) [19], and finite control set model predictive direct torque control (FCS-MPDT) [20]–[21] have been presented with optimum duty ratio for electric drives in [22]. Those issues and solutions for the abovementioned control techniques have been discussed in details with many experimental results based on different kinds of machines and drives. However, there are some serious issues for the MPC to be solved in future, which include large computation time, heavy dependence on parameter, slow dynamics, and lack robustness [23]. As the rapid technology evolution of the microcontroller and digital signal processor, the MPC would find more opportunities for the industrial application [22]. Furthermore, the FPGA development board and ASIC technology not only provide...
fast computation time but also give more and more opportunities to improve the robustness and to enhance convenience, especially in ASIC with low power consumption and small chip area.

The present study proposes a predictive DTC (PDTC) application-specific integrated circuit (ASIC) with a fuzzy PID controller and a proposed round-off calculation circuit. The fuzzy controller and round-off calculation circuit can improve the performance of a three-phase induction motor (IM) drive system. The rest of this paper is organized as follows. Section II describes the design of the proposed circuit for an IM drive system. Section III presents the simulation and measurement results for functional verification. Finally, Section IV presents the conclusions of this study.

II. CIRCUIT DESIGN OF THE PROPOSED FUZZY PDTC ASIC

Figure 1 shows a block diagram of the proposed PDTC ASIC with a fuzzy PID controller and a new round-off calculation circuit. The aforementioned scheme was developed for IM drives. The scheme involves three-phase to two-phase transformation (abc–dq transformation), voltage calculation, flux calculation, torque calculation, speed feedback, predictive calculation, sector selection, fuzzy PID control, fuzzy voltage vector switching, and short-circuit prevention. All the blocks were designed using the Verilog hardware description language (HDL) and verified using a FPGA development board. Finally, an ASIC was fabricated in 0.18-μm 1P6M CMOS process for a three-phase IM drive system.

A. COORDINATE TRANSFORMATION AND CALCULATION FORMULAS

The advantage of coordinate transformation is that it reduces the calculation burden and increases response speed. The three-phase voltages, namely \( v_{\text{as}} \), \( v_{\text{bs}} \), and \( v_{\text{cs}} \), and three-phase currents, namely \( i_{\text{as}} \), \( i_{\text{bs}} \), and \( i_{\text{cs}} \), can be transformed into two-phase voltages, namely \( v_{\text{ds}} \) and \( v_{\text{qs}} \), and two-phase currents, namely \( i_{\text{ds}} \) and \( i_{\text{qs}} \), respectively. Then the stator current vector \( i'_{\text{s}}(t) \) and stator voltage vector \( v'_{\text{s}}(t) \) can be calculated in the stationary coordinate system.

\[
i'_{\text{s}}(t) = i'_{\text{ds}}(t) + ji'_{\text{qs}}(t) \tag{1}
\]

\[
v'_{\text{s}}(t) = v'_{\text{ds}}(t) + jv'_{\text{qs}}(t) \tag{2}
\]

where \( i'_{\text{ds}} \) and \( i'_{\text{qs}} \) are the real and imaginary parts of the stator current vector; and that \( v'_{\text{ds}} \) and \( v'_{\text{qs}} \) are the real and imaginary parts of the stator voltage vector. By adding a conversion constant \( c \) to the stationary coordinate system, the \( i'_{\text{ds}} \) and \( i'_{\text{qs}} \) can be expressed as follows [24], [25]:

\[
i'_{\text{ds}}(t) = c \times \text{Re}\{i'_{\text{ds}}(t)\} = c \times \text{Re}\{i'_{\text{ds}}(t) + i'_{\text{qs}}(t)e^{j2\pi/3} + i'_{\text{qs}}(t)e^{j4\pi/3}\}
\]

\[
i'_{\text{ds}}(t) = c \times \{i'_{\text{ds}}(t) - \frac{1}{2} i'_{\text{qs}}(t) - \frac{1}{2} i'_{\text{qs}}(t)\} \tag{3}
\]

Next, we find that the instantaneous power \( P_{\text{abc}} \) of the three-phase system and the instantaneous power \( P_{\text{dq}} \) of the two-phase system can be expressed in (5) and (6), respectively.

\[
P_{\text{abc}} = i'_{\text{ds}} \times v'_{\text{as}} + i'_{\text{bs}} \times v'_{\text{bs}} + i'_{\text{cs}} \times v'_{\text{cs}} \tag{5}
\]

\[
P_{\text{dq}} = i'_{\text{ds}} \times v'_{\text{ds}} + i'_{\text{qs}} \times v'_{\text{qs}} \tag{6}
\]

Substituting (3) and (4) into (6), we can prove that the following equation is correct between \( P_{\text{abc}} \) and \( P_{\text{dq}} \) with \( i'_{\text{as}} + i'_{\text{bs}} + i'_{\text{cs}} = 0 \).

\[
P_{\text{dq}} = \frac{3}{2}c^2 P_{\text{abc}} \tag{7}
\]

Considering the non-power constant, the conversion constant \( c \) can be selected to be 2/3. Then the following equation can be obtained.

\[
P_{\text{dq}} = \frac{2}{3} P_{\text{abc}} \tag{8}
\]

Thus, the two-phase currents, \( i'_{\text{ds}} \) and \( i'_{\text{qs}} \), can be expressed as follows:

\[
\begin{align*}
&i'_{\text{ds}}(t) + i'_{\text{bs}}(t) + i'_{\text{cs}}(t) = 0 \\
&i'_{\text{ds}}(t) = c \times \{i'_{\text{ds}}(t) - \frac{1}{2} i'_{\text{qs}}(t) - \frac{1}{2} i'_{\text{qs}}(t)\} = 0 \\
&i'_{\text{qs}}(t) = c \times \left\{\frac{\sqrt{3}}{2} i'_{\text{bs}}(t) - \frac{\sqrt{3}}{2} i'_{\text{cs}}(t)\right\} \\
&i'_{\text{ds}}(t) = -i'_{\text{cs}}(t) - i'_{\text{cs}}(t) = i'_{\text{ds}}(t) \\
&i'_{\text{qs}}(t) = \frac{1}{\sqrt{3}} i'_{\text{bs}}(t) + \frac{2}{\sqrt{3}} i'_{\text{qs}}(t) \tag{9}
\end{align*}
\]

Similarly, the two-phase voltages, \( v'_{\text{ds}} \) and \( v'_{\text{qs}} \), can be expressed as follows:

\[
\begin{align*}
&v'_{\text{ds}}(t) = -v'_{\text{bs}}(t) - v'_{\text{cs}}(t) = v'_{\text{ds}}(t) \\
&v'_{\text{qs}}(t) = \frac{1}{\sqrt{3}} v'_{\text{bs}}(t) + \frac{2}{\sqrt{3}} v'_{\text{qs}}(t) \tag{10}
\end{align*}
\]

For the voltage calculation, the output voltages of the U, V, and W phases, namely \( S_a \), \( S_b \), and \( S_c \), respectively, and the dc voltage \( V_d \) are measured at the output terminals of the inverter. Then, the two-phase voltages \( V_D \) and \( V_Q \) are calculated as follows:

\[
V_d = \frac{V_d}{3}(2S_a - S_b - S_c) \tag{11}
\]
\[ V_o = \frac{\sqrt{3}}{3} V_a (S_b - S_c) \]  

(14)

Next, the flux and torque calculations can be completed using the two-phase output voltages \( v'_{ds} \) and \( v'_{qs} \) and two-phase output currents \( i'_{ds} \) and \( i'_{qs} \). The flux (\( \phi \)) can be calculated using the single-phase stator winding resistance \( R_s \) as follows:

\[
\begin{bmatrix}
\phi'_{ds} \\
\phi'_{qs}
\end{bmatrix} = \frac{1}{p} \begin{bmatrix}
v'_{ds} \\
v'_{qs}
\end{bmatrix} - R_s \begin{bmatrix}
i'_{ds} \\
i'_{qs}
\end{bmatrix}, \quad p = \frac{d}{dt}
\]  

(15)

According to the Laplace transform, the variable \( p \) is defined as the complex \( s \), and \( T \) is the sampling period. Then, the following transform can be obtained:

\[
\frac{1}{p} = \frac{1}{s} = T \times \frac{z}{z - 1}
\]  

(16)

Thus, the fluxes \( \phi'_{ds} \) and \( \phi'_{qs} \) can be expressed as follows [25]:

\[
\begin{align*}
\phi'_{ds}(z) &= \frac{1}{z} \phi_{ds}(z) + T \times \left[ V'_{ds}(z) - R_s \times i'_{ds}(z) \right] \\
\phi'_{qs}(z) &= \frac{1}{z} \phi_{qs}(z) + T \times \left[ V'_{qs}(z) - R_s \times i'_{qs}(z) \right]
\end{align*}
\]  

(17)

Furthermore, the torque (\( T_e \)) is calculated according to DTC theory as follows:

\[
T_e = \frac{3}{2} P \left( \phi'_{dqs} i'_{qds} - \phi'_{qds} i'_{dqs} \right)
\]  

(18)

where \( P \) is the motor pole number.

In the speed calculation, the rotating speed \( \omega_a \) is equal to the frequency of the digital signal obtained from the rotary encoder (\( \omega_a \)). The phase difference between two digital signals, namely \( P_a \) and \( P_b \), indicates the rotation direction of the IM.

**B. SECTOR SELECTION**

Sector selection can be completed by calculating the two-phase stator fluxes \( \phi'_{ds} \) and \( \phi'_{qs} \) and determining the resultant magnetic flux \( \phi_{dqs} \). In general, the voltage space vector can be divided into six sectors, each of which has an angle of 60°.

To simplify the analysis, the first quadrant contains \( \phi'_{ds} \) and \( \phi'_{qs} \) with the phase difference between two digital signals, namely \( S_a \) and \( S_b \). The first sector \((S_1)\) extends from 0° to 30°, and the second sector \((S_2)\) extends from 30° to 90°. In trigonometry, the following relations exist:

\[
\phi'_{ds} = |\phi'_{dqs}| \times \cos 30°
\]  

(19)

\[
\phi'_{qs} = |\phi'_{dqs}| \times \cos 60°
\]  

(20)

The following equation is obtained by dividing (19) by (20):

\[
\frac{3}{2} \phi'_{qs} - \phi'_{ds} = 0
\]  

(21)

If both stator fluxes, \( \phi'_{ds}(t) \) and \( \phi'_{qs}(t) \), are positive in the
first sector, the value of \( \sqrt{3} |\phi^s_{ds}| - |\phi^s_{qs}| \) is negative (<0) for large \( \phi_{ds}(t) \), but it is positive (>0) with large \( \phi^s_{ds}(t) \). Table I presents the sector selection table for the proposed PDTC ASIC. The output sector can be easily selected using this table. The symbols “0” and “1” represent a positive value (>0) and negative value (<0), respectively [26].

![FIGURE 2. Coordinate stator fluxes, \( \phi_s \) and \( \phi^s_{qs} \) and resultant flux \( \phi^s_{avr} \) in the first quadrant.](image)

| \( \sqrt{3} |\phi^s_{ds}| - |\phi^s_{qs}| \) | \( \phi^s_{ds} \) | \( \phi^s_{qs} \) | Output Sector |
|---|---|---|---|
| 1 | 0 | 0 | S1 |
| 1 | 0 | 1 | S1 |
| 1 | 1 | 0 | S4 |
| 1 | 1 | 1 | S4 |
| 0 | 0 | 0 | S2 |
| 0 | 0 | 1 | S6 |
| 0 | 1 | 0 | S3 |
| 0 | 1 | 1 | S5 |

**C. PREDICTION CALCULATION CIRCUIT**

A DTC scheme can achieve satisfactory decoupled flux and torque control through prediction calculation circuit (PCC) and thus reduce voltage and current ripples. Figure 3 displays block diagrams of PCC for flux (\( \phi_s \)) and torque (\( T_e \)) calculations. It is used to calculate the flux or torque without increasing the burden on the processor. In general, reluctance torque ripples are generated by the time delay in traditional DTC systems. High-speed and high-precision motor control can alleviate the aforementioned problem. The predictive control model is used to reduce the calculation burden and to decide the motor position rapidly [26].

As depicted in Fig. 3(a), the delay (\( \tau^{-1} \)) block is implemented with a D-type flip-flop (DFF) circuit. The subtraction block (\( \setminus \)) is used to obtain the deviation between the present flux \( \phi_i[k] \) and the previous flux \( \phi_i[k-1] \). Furthermore, the absolute block (Abs.) provides the magnitude of the deviation, and the multiplier determines the output \( \Delta \phi_i[k] \) according to the control flux signal \( C_{\phi_i}[k] \). A similar control mechanism comprising the present torque \( T_i[k] \), previous torque \( T_i[k-1] \), and control torque signal \( C_{T_i}[k] \) is presented in Fig. 3(b). By adding the designed PCC scheme, the proposed PDTC scheme not only has the advantages of the traditional DTC scheme but also reduces the delay time and thus improves the IM drive performance.

**D. FUZZY PID CONTROLLER**

A PID controller is a well-known tool for controlling the speed of an IM drive. In general, the Ziegler–Nichols (Z–N) method is used to define three key parameters of the traditional PID controller: \( K_p, K_i, \) and \( K_d \) [27]. The general formula of a PID controller is expressed as follows:

\[
\frac{U(s)}{E(s)} = K_p + \frac{K_i}{s} + sK_d,
\]

where \( s \) is a complex frequency and \( K_P, K_i, \) and \( K_d \) represent the proportional, integral, and derivative coefficients, respectively. These three coefficients significantly influence the stability of the PID controller. The performance of a fuzzy controller is superior to that of a non-fuzzy linear proportional–integral controller because of the nonlinearities introduced in the fuzzy controller by the nonlinear defuzzification algorithm [28].

Figure 4 illustrates a block diagram of the adopted fuzzy PID controller. It operates with an input error \( e(t) \) and input error variation \( \Delta e(t) \). By passing through the fuzzy PID controller, two outputs, namely \( K_p \) and \( K_d \), can be obtained. The integral coefficient \( K_i \) can be calculated as follows:

\[
K_i = \frac{K_p^2}{\alpha \times K_d}
\]

where \( \alpha \) is a constant.

The operating principle of the fuzzy controller is to determine the output \( u(t) \) with three coefficients by using the membership function and fuzzy rule base. The output of the fuzzy PID controller (\( u(t) \)) is expressed as follows:
where \( e(t) \) is the input error.

After \( u(t) \) is calculated, a closed-loop control procedure is executed for the IM drive system. This self-adjusting mechanism is completed with the feedback speed \( \omega_i \). The fuzzy PID controller works with adequate adaptability. The fuzzy rule tables of \( K_p, K_d, \) and \( \alpha \) are listed in Tables II–IV, respectively [24]. The fuzzy membership functions of \( K_p \) and \( K_d \) vary between 0.0 and 1.0 while the \( \alpha \) parameter alters from 0.2 to 1.2. Figure 5 depicts the block diagram of the adopted fuzzy controller.

**TABLE II**

| \( \Delta e \) | PB | PS | ZE | NS | NB |
|---------------|----|----|----|----|----|
| PB            | PB | PB | PB | PB | PB |
| PS            | PS | PB | PB | PB | PS |
| ZE            | PS | PS | PB | PS | PS |
| NS            | PS | PB | PB | PB | PS |
| NB            | PB | PB | PB | PB | PB |

**TABLE III**

| \( \Delta e \) | PB | PS | ZE | NS | NB |
|---------------|----|----|----|----|----|
| PB            | PS | PS | PS | PS | PS |
| PS            | PB | PB | PB | PB | PB |
| ZE            | PB | PB | PB | PB | PB |
| NS            | PB | PS | PB | PB | PB |
| NB            | PS | PS | PS | PS | PS |

**TABLE IV**

| \( \Delta e \) | PB | PS | ZE | NS | NB |
|---------------|----|----|----|----|----|
| PB            | 2  | 2  | 2  | 2  | 2  |
| PS            | 4  | 3  | 2  | 3  | 4  |
| ZE            | 5  | 4  | 3  | 4  | 5  |
| NS            | 4  | 3  | 2  | 3  | 4  |
| NB            | 2  | 2  | 2  | 2  | 2  |

**TABLE V**

| \( \Delta e \) | PB | PS | ZE | NS | NB |
|---------------|----|----|----|----|----|
| PB            | NB | NS | NS | NS | ZE |
| PS            | NB | NS | NS | NS | ZE |
| ZE            | NS | NS | NS | NS | ZE |
| NS            | NS | ZE | PS | PS | PB |
| NB            | ZE | ZE | PS | PS | PB |

**E. FUZZY CONTROLLER**

As shown in Fig. 5, the error \( e_t \) and error variation \( \Delta e_t \) derived from the speed feedback are input variables of the fuzzy controller. Moreover, the output variable \( u \) is obtained through with the fuzzy controller. Figure 6 illustrates the five-stage fuzzy membership function. In this figure, two input variables, namely \( e_t \) and \( \Delta e_t \), are divided into five fuzzy sets: the negative big (NB), negative small (NS), zero (ZE), positive small (PS), and positive big (PB) fuzzy sets. Those parameters, PB, PS, ZE, NS, and NB, are 32, 16, 0, -16, and -32, respectively. Table V presents the rule table for the five-stage fuzzy controller.

**F. FUZZY VOLTAGE VECTOR SWITCHING TABLE**

The main disadvantage of the conventional DTC hysteresis controller is the instability generated by its large torque and flux ripples. A fuzzy voltage vector switching table is proposed to resolve the aforementioned problem. Figure 7 illustrates the fuzzy torque of the five-stage hysteresis controller. The input variables of this controller are the torque error \( d_T \), which is defined as \( d_T = T_e^* - T_a \), and the torque error variation \( \Delta d_T \). The output variable is the torque selection value \( \tau \) for the torque control \( T_T \). The five-stage
hysteresis controller comprises five torque sets: PB, PS, ZE, NS, and NB. Moreover, the three-stage hysteresis controller comprises three flux sets: P (positive), Z (zero), and N (negative). Table VI presents a fuzzy voltage vector switching table for the five-stage torque (T) hysteresis controller, three-stage flux (ϕ) hysteresis controller, and angle interval θ. Each angle interval (θ) is 60°. The first angle (θ1) varies from -30° to 30°, and the second angle (θ2) varies from 30° to 90°. Similarly, the last angle (θ3) varies from 270° to 330°. When the angle interval is θ1, the magnetic flux (ϕ) increases (P), the torque (T) increases significantly (PB), and the stator voltage vector is selected as V2.

**TABLE VI**

FUZZY VOLTAGE VECTOR SWITCHING TABLE FOR FLUX (ϕ), TORQUE (T), AND ANGLE (θ)

|  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|
| θ |  |  |  |  |  |  |
| PB | V2 | V3 | V4 | V5 | V6 | V1 |
| PS | V2 | V3 | V4 | V5 | V6 | V1 |
| ZE | V1 | V2 | V3 | V4 | V5 | V6 |
| NS | V6 | V1 | V2 | V3 | V4 | V5 |
| NB | V6 | V1 | V2 | V3 | V4 | V5 |

|  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|
|  |  |  |  |  |  |  |
| PB | V3 | V4 | V5 | V6 | V1 | V2 |
| PS | V3 | V4 | V5 | V6 | V1 | V2 |
| ZE | V6 | V1 | V2 | V3 | V4 | V5 |
| NS | V6 | V1 | V2 | V3 | V4 | V5 |
| NB | V3 | V4 | V5 | V6 | V1 | V2 |

|  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|
|  |  |  |  |  |  |  |
| PB | V3 | V4 | V5 | V6 | V1 | V2 |
| PS | V3 | V4 | V5 | V6 | V1 | V2 |
| ZE | V6 | V1 | V2 | V3 | V4 | V5 |
| NS | V6 | V1 | V2 | V3 | V4 | V5 |
| NB | V3 | V4 | V5 | V6 | V1 | V2 |

**G. PROPOSED ROUND-OFF ALGORITHM**

After the two electric fluxes, namely ϕs and ϕq, are obtained, the synthetic flux ϕsq can be calculated using a square root circuit, a round-off calculation circuit, and a DFF circuit. The aforementioned square root circuit is determined using the shadow tree algorithm [5], and the DFF circuit is used to achieve synchronization according to the clock signal (Clk). The round-off method is used to reduce the calculation error of the square root circuit. Figure 8 displays the calculation blocks of the synthetic flux ϕsq for the square root, round-off, and DFF circuits. Note that the synthetic flux ϕsq is expressed as follows:

\[
ϕ_{sq} = \sqrt{ϕ_{ds}^2 + ϕ_{qs}^2}
\]

To complete the round-off calculation, a calibration constant Cal is used for modifying the output code of the round-down calculation. Table VII presents the calculation results of the round-down and round-off algorithms. The second and third columns of this table present the initial values of the square root and their output digital codes in the round-down calculation (RD) when the input data (IN) vary from 1 to 10. A calibration constant (Cal) is used to modify the output codes in the round-off calculation (RO). The constant Cal is defined as follows:

\[
Cal = \left[ IN - RD^2 \right] - \left[ (RD + 1)^2 - IN \right] = 2 \times \left[ IN - RD \times (RD + 1) \right] - 1
\]

Moreover, the decision formula is expressed as follows:

\[
\begin{align*}
RO &= RD, \quad \text{if } Cal \leq 0 \\
RO &= RD + 1, \quad \text{if } Cal > 0
\end{align*}
\]

**TABLE VII**

| IN  | SR | RD  | Cal  | RO  | |Eao| |Eao| |
|-----|----|-----|------|-----|------|------|------|
| 1   | 1  | 1   | -3   | 1   | 0    | 0   |
| 2   | 1.414 | 1   | -1   | 1   | 0.414 | 0.414 |
| 3   | 1.732 | 1   | 1    | 2   | 0.732 | 0.268 |
| 4   | 2   | 2   | -5   | 2   | 0    | 0   |
| 5   | 2.236 | 2   | -3   | 2   | 0.236 | 0.236 |
| 6   | 2.449 | 2   | -1   | 2   | 0.449 | 0.449 |
| 7   | 2.646 | 2   | 1    | 3   | 0.646 | 0.354 |
| 8   | 2.828 | 2   | 3    | 3   | 0.828 | 0.172 |
| 9   | 3   | 3   | -7   | 3   | 0    | 0   |
| 10  | 3.162 | 5   | -3   | 3   | 0.162 | 0.162 |
| |Eao| |Eao| |Eao| |Eao| |Eao| |
| -   | -   | -   | -    | -   | 0.3467 | -    |
| -   | -   | -   | -    | -   | -    | 0.2055 |

As shown in Table VII, there are two differences at input values (IN) of 3 and 7. For IN = 3, the RD is 1, but RO is 2; and that RD = 2 and RO = 3 for IN = 7. The absolute deviations of the round-down and round-off calculation circuits, namely |Eao| and |Eao|, obtained using (26) and (27), respectively, are listed in the sixth and seventh columns of Table VII, respectively. The mean deviation of the round-off calculation circuit |Eao| is approximately 0.2055, and the
mean deviation of the round-down circuit [MEAD] is approximately 0.3467. Thus, the round-off method exhibits a significantly lower mean deviation than does the round-down method. In general, the round-off calculation is widely used in microprocessor with analog output, which is not suitable for calculating in digital circuit. This is the reason why we need to propose a new round-off algorithm to complete the digital calculation in FPGA development board.

III. SIMULATION AND MEASUREMENT RESULTS

After the designed modules were implemented using the Verilog HDL, the ModelSim software was used to complete the behavioral simulation with the HDL test bench file. Figure 9 shows the simulated waveforms of the six-arm voltage signals of the inverter at a clock frequency of 10 MHz and a basic frequency of 1200 rpm (approximately 50 ms). As depicted in this figure, the up arm (S_u) and down arm (S_d) move in accordance with inverse waveforms in each phase with \( i = a, b, \) and \( c \). Thus, \( S_u, S_d \), and \( S_f \) are the up-arm output voltages of the U, V, and W phases, respectively. The behavior simulation confirms that the designed functions work correctly. Table VIII summarizes the system specifications of the proposed PDTC ASIC. According to the simulation results, the proposed PDTC ASIC with a fuzzy PID controller and round-off calculation circuit achieves a test coverage of 99.10%, a fault coverage of 98.28%, and a power consumption of 1.0027 mW at an operating frequency of 10 MHz and a supply voltage of 1.8 V. Furthermore, the gate count of the proposed ASIC is 56,766, and its chip area, including the area of the pads, is approximately 1.169 \( \times \) 1.168 mm\(^2\).

| TABLE VIII | SYSTEM SPECIFICATIONS OF PROPOSED PDTC ASIC |
|------------|------------------------------------------|
| Items      | Specifications                           |
| Technology | 0.18-\( \mu \)m 1P6M CMOS                |
| Supplied Voltage | 1.8 V                                  |
| Test Coverage          | 99.10%                                  |
| Fault Coverage          | 98.28%                                  |
| Operating Frequency     | 10 MHz                                  |
| Power Consumption       | 1.0027 mW                               |
| Gate Counts             | 56,766                                  |
| Chip Size              | 1.169x1.168 mm\(^2\)                    |
| Package                | CLCC 84                                  |

After the behavior simulation was completed, an FPGA development board was used to verify the designed functions and a logic analyzer was used to analyze the measured digital signals. Figure 10 illustrates the measured waveforms of the six-arm voltage signals of the inverter. These waveforms were measured using the logic analyzer at a clock frequency of 10 MHz and a basic frequency of 1200 rpm (approximately 50 ms). The measured waveforms are similar to those obtained in the behavior simulation, as displayed in Fig. 9. Furthermore, a dead time must be generated between the up arm and the down arm to prevent the three-phase IM from burning because of the short-circuit current. Figure 11 presents the dead time measured in the U phase with the logic analyzer (3 \( \mu \)s), which is suitable for the adopted IM drive system.

The proposed PDTC ASIC with a fuzzy PID controller exhibits smaller ripples in the stator flux than does a conventional DTC system, which generates a stator flux with a hysteresis controller [29]. Figure 12 shows the measured locus of the stator flux from 10 to 200 ms with the FPGA board for the proposed PDTC with a fuzzy PID controller and the conventional DTC with a hysteresis controller, respectively. As displayed in Fig. 12(a), the proposed controller exhibited small flux ripples and a smooth unit cycle. The stator flux ripples are significantly lower in the proposed PDTC scheme than in the conventional DTC system. Figure 13 displays the standardized composite flux \((\phi_w)\) values for the proposed ASIC and traditional DTC system, respectively. The proposed PDTC ASIC that performs with new round-off calculation exhibits small composite flux ripples in Fig. 13(a). The proposed round-off algorithm can improve the performance of IM drive.
After the designed functions were verified with the FPGA board, the Verilog HDL codes were incorporated into an ASIC and fabricated using the 0.18-μm 1P6M CMOS process of TSMC. A generic digital IC (ASIC) design method was used to complete the logic synthesis based on the standard cell library, which is provided with TSMC in 0.18-μm 1P6M CMOS process. Figure 14 shows the measurement instruments, including an ac motor with a speed controller, an inverter, an oscilloscope, a differential probe, and a chip test platform (printed circuit board). Figure 15 illustrates the measured stator fluxes of the proposed PDTC ASIC, namely $\phi_{ds}$ and $\phi_{qs}$. The measured phase shift was approximately 91°. As depicted in Fig. 16, the measured dead time was 200 ns, which is suitable for preventing short-circuiting.

Figures 17 and 18 illustrate the locus of the stator flux in the proposed PDTC ASIC and traditional DTC system, respectively. A comparison of the stator flux trajectories of the proposed PDTC and traditional DTC system confirmed that the performance of the proposed PDTC ASIC is superior to that of the traditional DTC system. The circular ripples of the PDTC ASIC with a fuzzy PID controller and round-off calculation circuit were smaller than those of the conventional DTC system. Figure 19 shows the photomicrograph of the proposed PDTC ASIC with a fuzzy PID controller and round-off calculation circuit. The measurement results indicate that the proposed PDTC ASIC works correctly at an operating frequency of 10 MHz and a sampling rate of 100 kS/s.

**FIGURE 12.** Measured locus of the stator flux from 10 to 200 ms with an FPGA board: (a) proposed PDTC with a fuzzy PID controller and (b) conventional DTC with a hysteresis controller.

**FIGURE 13.** Measured standardized composite flux $\phi_{sdc}$: (a) proposed PDTC ASIC with round-off calculation and (b) traditional DTC system without round-off calculation.

**FIGURE 14.** Measurement instruments (motor, inverter, and FPGA development board).
Figure 15. Measured stator fluxes of the proposed PDTC ASIC ($\phi_s^d$ and $\phi_s^q$).

Figure 16. Measured dead time (0.2 $\mu$s) for the proposed PDTC ASIC.

Figure 17. Measured locus of stator flux in the proposed PDTC ASIC.

Figure 18. Measured locus of stator flux in the traditional DTC system.

Figure 19. Photomicrograph of the proposed PDTC ASIC.

Figure 20. Measured line currents ($I_{as}$, $I_{bs}$, and $I_{cs}$). The proposed PDTC ASIC operates correctly, and the three-phase IM is driven smoothly with small ripples.

Figure 20 displays the measured line currents ($I_{as}$, $I_{bs}$, and $I_{cs}$) at a sampling frequency of 100 kHz and a rotation frequency of 1200 rpm for a three-phase, 0.75-kW IM. As presented in (11), $I_{as}$ and $I_{bs}$ can be transformed into the two-phase stator currents $i_{as}$ and $i_{qs}$, respectively, through trigonometric calculations. Furthermore, Figures 21 and 22 illustrate the measured line voltages for the U–V, V–W, and W–U phases ($V_{ab}$, $V_{bc}$, and $V_{ca}$, respectively). The proposed
IV. CONCLUSIONS

In this study, a PDTC ASIC with a fuzzy PID controller and a new round-off calculation circuit was designed to achieve stable control for a three-phase IM drive. After the designed functions were verified using an FPGA development board, an ASIC was fabricated using the 0.18-µm 1P6M CMOS process of TSMC. The measurement results indicate that the stator flux trajectory of the proposed PDTC ASIC is superior to that of the traditional DTC system with a hysteresis controller. Furthermore, the standardized composite flux \( \Phi_{dqs} \) in the proposed ASIC is more accurate than that in the traditional DTC system. The proposed round-off algorithm results in small composite flux ripples and improves the IM drive performance. A fuzzy voltage vector switching table is proposed not only to speed up the calculating speed in FPGA design but also to resolve the instability generated by its large torque and flux ripples. The predictive calculations, fuzzy PID controller, fuzzy voltage vector switching table, and round-off calculation algorithm improved not only the ripple issue faced in traditional direct torque control but also the control stability and robustness. The measurement results indicate that the dead time and power consumption of the developed ASIC are 100 ns and 1.0027 mW, respectively, at an operating frequency of 10 MHz, a sampling rate of 100 kS/s, and a supply voltage of 1.8 V. Moreover, the gate counts and chip area of the proposed ASIC are 56,766 and 1.169 x 1.168 mm², respectively. The proposed PDTC ASIC has a smaller chip area and lower power consumption than does the traditional DTC system developed using an FPGA board. It can be used in various kinds of motors. The main advantages of the proposed PDTC ASIC are its low power consumption, small chip size, robustness, convenience, and correctness.

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