Comparative Analysis and Enhancement of CFG-based Hardware-Assisted CFI Schemes

Mario Telesklav  
Embedded Computing Systems Group  
TU Wien  
mario.telesklav@ecs.tuwien.ac.at

Stefan Tauner  
Embedded Computing Systems Group  
TU Wien  
stauner@ecs.tuwien.ac.at

Abstract—Subverting the flow of instructions (e.g., by use of code-reuse attacks) still poses a serious threat to the security of today’s systems. Various control flow integrity (CFI) schemes have been proposed as a powerful technique to detect and mitigate such attacks. In recent years, many hardware-assisted implementations of CFI enforcement based on control flow graphs (CFGs) have been presented by academia. Such approaches check whether control flow transfers follow the intended CFG by limiting the valid target addresses. However, these papers all target different platforms and were evaluated with different sets of benchmark applications, which makes quantitative comparisons hardly possible. For this paper, we have implemented multiple promising CFG-based CFI schemes on a common platform comprising a RISC-V SoC within an FPGA. By porting almost 40 benchmark applications to this system we can present a meaningful comparison of the various techniques in terms of run-time performance, hardware utilization, and binary size. In addition, we present an enhanced CFI approach that is inspired by what we consider the best concepts and ideas of previously proposed mechanisms. We have made this approach more practical and feature-complete by tackling some problems largely ignored previously. We show with this fine-grained scheme that CFI can be achieved with even less overheads than previously demonstrated.

I. INTRODUCTION

The eventual goal of any attacker is to manipulate the execution flow of a program, e.g., to exfiltrate data by overcoming restrictions or to execute malicious code. To that end, input data is manipulated to exploit the abstract machines that programming languages/environments and the underlying hardware provide. Prominent examples are the notorious class of stack buffer overflows [23] and format string vulnerabilities [28]. These approaches take advantage of the fact that targets of indirect control flow transfers like return addresses of functions are often stored on the stack where they can easily be overwritten if certain faulty constructs end up in programs.

In earlier days one could not only change the control flow that way but even directly supply malicious code to be executed from the stack. However, in the last two decades defenses against these and more advanced threats have been improved. Unfortunately, there is still no silver bullet in sight: Static and dynamic bug finding tools [30] have become able to warn programmers of the exploitable bugs before they creep into the code base (but they have to be utilized); CPUs (often even those in embedded systems) can enforce non-executability of certain address ranges like the stack (if set up correctly [2]); Address space layout randomization (ASLR) makes it harder (but not impossible [17]) to derive the addresses necessary to mount return-to-libc attacks or exploit use-after-free vulnerabilities; sandboxing and splitting applications into multiple (micro)services simplifies logic locally (but increases overall complexity) [25].

A. Code-Reuse Attacks

While the improved defense mechanisms have triggered an arms race with attackers that made possible attacks very sophisticated [26], the basic ideas have remained the same: 1) establish a write primitive to manipulate the stack or heap, 2) determine a suitable address to overwrite, 3) overwrite data there to branch off into an unintended flow of instructions.

Due to the mitigations typically employed in modern systems it is usually not possible to simply inject new instructions to be executed. Therefore, adversaries rely on the existing code to chain together snippets called gadgets in code-reuse attacks (CRAs). This can, for example, be accomplished by jumping to a short code sequence ending in a ret whose target address was manipulated in return-oriented programming (ROP) [29], or exploit similar semantics of indirect jumps in jump-oriented programming (JOP) [7]. In either case the attacker can produce Turing-complete arrangements by completely mangling the sequence of instructions intended by the programmer.

B. Control Flow Integrity

The intended flow is captured by the control flow graph (CFG) of a program consisting of basic blocks (BBs) connected by control transfer instructions. Depending on the instruction set architecture (ISA) the latter consist of instructions to call and return from functions, direct and indirect jumps etc. The connections in the CFG spanned by returns are called backward edges while all other control transfers are forward.

To counter attacks that try to break out of the intended CFG, various forms of control flow integrity (CFI) enforcement ideas have been presented. Interestingly, the earliest concepts to guarantee CFI have not been proposed for security but safety reasons. In the 1990s Wilken and Shen developed continuous signature monitoring (CSM) as a countermeasure against transient faults in the control logic of processors [35].
The groundwork for nowadays security-centered CFI was laid in 2005 by Abadi et al. with their original CFI proposal [1]. The attack model comprises an adversary with full control of the entire data memory (while code is thought to be read-only). Under these assumptions, direct calls and jumps do not pose a threat because their target cannot be changed. The main idea is to enforce that every indirect control flow transfer only targets one of its allowed destinations. The authors suggest to guarantee this by checking labels inserted at the respective target BBs. Every indirect call, jump, and also return has to verify that their inherent label from the originating BB matches the target. This basic approach is independent of the ISA and can be implemented in software only or by extending the hardware to handle the checks directly.

In this work we focus on CFI implementations that rely on hardware support. For a review of software-only approaches we refer to the survey by Burow et al. [5].

Even when CFI is able to enforce a fully-precise CFG it is not very effective on its own. The problem stems from the fact that without a run-time state it is impossible to determine securely if a return address is matching the correct caller or if it was manipulated to follow another allowed edge of the CFG. For that reason backward edges have to be protected by additional mechanisms, e.g. by a shadow stack, to remain effective [6].

A shadow stack (or return address stack) is an extra protected memory for redundantly keeping track of return addresses. Its basic concept was already proposed in the early 2000s as return address repository (RAR) [8]. In hardware it can be implemented without run-time overhead if the respective memory is directly attached to the CPU pipeline.

C. Instrumentation

The process of injecting instructions into some program at certain well-defined positions is called instrumentation. Doing so in an already compiled binary is referred to as binary rewriting, with a broad field of applications like emulation, optimization and profiling [34]. Using binary rewriting for instrumentation of CFI entails that CFG extraction is harder, especially for stripped binaries and in the absence of debug symbols. For that reason, our implementation is based on a compiler extension that has the source code available.

D. Contribution & Outlook

In this work we answer how well proposed schemes for hardware-assisted CFI enforcement fare with respect to performance, hardware utilization and code size. To that end, we have implemented selected existing CFI protections on and ported numerous benchmark applications to a common platform allowing for a meaningful comparison. Additionally, we improve on these schemes and present a novel “best of” approach that borrows the best concepts and ideas of previously proposed mechanisms. We show with this fine-grained approach that CFI can be achieved with even less overheads than previously demonstrated. In the original articles evaluations have been executed on small SoCs in FPGAs due to the need of customizing the CPU pipeline. While none of the concepts hereinafter are necessarily limited to embedded systems we have to act under the same constraints. However, in addition to incrementally improving the concept of hardware-assisted CFI enforcement on small systems, we also show how to work around some practical problems that have to be solved to employ this method on larger systems. In the next section we review the academic literature on hardware-assisted CFI approaches. Out of those we have selected what we think are the most diverse and promising techniques for comparison. Their implementation details are reviewed in Section III together with our own improved variant of CFI enforcement. In Section IV we outline the test environment including benchmarks, the instrumentation process and the chosen hardware parameters. Eventually, we present and discuss the measurement results in the categories performance, hardware utilization and code size in Section V before ending with the conclusion.

II. RELATED WORK

We give a brief overview of existing hardware-based CFI approaches in this section and refer the interested reader to further literature such as the extensive survey of hardware-based CFI approaches by De Clercq and Verbauwhede in [14] for more details.

CFGs can be viewed as sequence diagrams, where some application’s functions or BBs correspond to states in the diagram. In [3] such statically determined CFG information is encoded into a finite state machine (FSM) where legit control flow transfers relate to allowed state transitions. In the same way also intra-procedural jumps are monitored on BB level. Similarly, [24] focuses on system calls and encodes allowed application-specific sequences thereof in an FSM to detect invalid executions.

SCRAP [22] uses an FSM for implementing a signature-based CFI approach. The concept monitors execution traces at runtime and applies heuristics to detect sequences of short gadgets that are often an indicator for some CRA. The frequency of gadget executions is also sometimes used in heuristic concepts because CRAs tend to reuse the same gadgets multiple times.

A whole other class of concepts tries to reduce the gadget space by limiting control flow transfers to BB boundaries in some way. Branch Regulation (BR) [21] restricts control flow transfers to entries of target functions and locations within the same function. This approach does not require CFG information. BB-CFI [10] went one step further and enforces that forward-edge control flow transfers only target the very beginning of certain BBs, thereby requiring a statically created CFG. BBB-CFI [19] ensures that forward-edge control flows only target the entry of BBs in general and thereby prevents jumps to positions in the middle, which is often required for gadgets. Similarly, Intel Control-flow Enforcement Technology (CET) [20] ensures that indirect jumps and calls can only target certain labels and function entries. CET is more precise but requires static analysis of the control flow and additional
protection is implemented by means of a policy matrix, which
shadow stack for securing backward edges. Forward-edge
A. FIXER
in the sections below. Changes to the original concepts were required, we note them
only happens implicitly during control transfers. Whenever
protected from deliberate software access and modification
same complete CFG everywhere. All memory elements are
flops (FFs) for all memory elements to enable in-cycle access
signals resulting from CFI violations. However, we use flip-
flops (FFs) for all memory elements to enable in-cycle access
for all implementations and also assume the availability of the
same label for functions that are called from multiple callers.
Table-based concepts, where a flag indicating the validity of
a certain branch target is looked up in a table upon every indirect control flow transfer, are another fine-grained but
very memory-intense approach for forward-edge protection.
FIXER [13] and [3] represent examples thereof.
CFI enforcement on backward edges requires different
techniques. Most CFI implementations use a shadow stack for
that. Examples for such proposals are HCFI [9], FIXER [13]
and Intel CET [20], which all redundantly store the return
address of function calls. This concept was slightly modified
in [31], where unique labels are stored on the stack instead
of addresses. Usually less memory is required for this variant, but
instrumentation is more complex. HAFIX [11] implements an
alternative concept for backward-edge protection by means of
an Active Set that keeps track of currently active functions and
only allows returns to functions flagged active there. However,
it has been shown that the concept is more vulnerable in
comparison to shadow stacks [33].

III. IMPLEMENTATIONS
We have selected four of the academic fine-grained CFG-
based CFI approaches listed above for a more detailed exami-
nation and, more importantly, implemented these concepts on a
common RISC-V platform. The criteria with which we made
this selection were the precision of their CFI enforcement as well as the variety of CFI concepts they implement. To
widen the view we have also included a rather coarse-grained
approach that is similar to a commercially available concept.
Our implementations of the presented concepts are as accurate
as their originals as possible. We have designed all of them
as separate modules, which are individually attached to the
core’s pipeline. Changes to the core itself only consist of
extensions to its decoder for custom instructions and modi-
fications in the pipeline controller for handling of exception
signals resulting from CFI violations. However, we use flip-
flops (FFs) for all memory elements to enable in-cycle access
for all implementations and also assume the availability of the
same complete CFG everywhere. All memory elements are
protected from deliberate software access and modification
only happens implicitly during control transfers. Whenever
changes to the original concepts were required, we note them
in the sections below.

A. FIXER
De et al. presented FIXER [13] in 2019, which uses a
shadow stack for securing backward edges. Forward-edge
protection is implemented by means of a policy matrix, which
holds flags for each pair of indirect function calls and their
potential targets. Upon performing a call, the flag is looked up
for the current combination of addresses and the call is only
executed when the respective flag is set. An address decoder
translates 32-bit addresses to matrix indices for the lookup.
The authors have realized the security mechanisms as a co-
processor to a RISC-V SoC, thereby making it unnecessary
to modify the actual core at all. However, using this approach
requires additional instructions for accessing pipeline registers
like the current program counter. The original FIXER concept
therefore needs multiple instructions for each CFI operation.
Given the possibility to implement the module for CFI en-
forcement directly attached to the pipeline in our setup, we
have removed this limitation so that only one instruction is
needed. De et al. reported a performance overhead of 1.5%
for backward edge protection, on average, and respectively
0.61% for forward edges. Area overhead was reported to be
2.9%.

B. HAFIX
In 2015, Davi et al. proposed an extension to [12] called
HAFIX [11]. Their approach only covers backward-edge
protection but contains two enforcement concepts, namely a
shadow stack and a concept for limiting function returns to
active call sites with the help of an Active Set. The authors
argue that software-side forward edge protection is sufficiently
effective. We only consider the Active Set approach since it
is their distinctive feature compared to other CFI concepts.
Every function is marked active at the very start of its
execution, and inactive when returning. This is done with
custom instructions holding a label unique for each function
that acts as an index to the Active Set. In addition, it is
enforced that functions can only return to an active function by
checking the active state of the function that it is returning to.
Simple forms of recursion are specifically handled by means
of a counter measuring the recursion depth, while special cases
like nested recursion are not supported.
Davi et al. presented HAFIX as an extension to an x86
Intel Siskiyou Peak softcore. The proposed concept involves
an average performance overhead of around 2%. 2.5% more
registers and less than 1% of additional look-up tables (LUTs)
were required.

C. HCFI
Christoulakis et al. presented HCFI [9] in 2016, which
provides protection for both forward and backward edges. They
have implemented their concept on a LEON3 SPARC
softcore. The SPARC ISA allows for using branch delay slots
to execute some of the additionally required instructions. This
is not possible on our RISC-V platform.
The authors highlight the importance of a shadow stack for
CFI enforcement of function returns and implement such with
dedicated recursion handling and support for C’s \texttt{setjmp}.
Forward-edge protection is achieved by instrumenting indirect
function calls and the entries of indirectly called functions with
labels. Upon calling such a function, the label set at the caller
side is stored in the CFI monitor and compared to the label in the callee. An internal FSM checks that such instructions are executed back-to-back.

About 1% run-time overhead and a hardware overhead of 2.5% (LUTs and FFs combined) were reported.

D. Policy-Agnostic Hardware-Enhanced Control-Flow Integrity (HECFI)

Sullivan et al. proposed a concept similar to HCFI in 2016 in [31], but with added support for securing indirect jumps and a very fine-grained approach for forward-edge protection. For easier reference we call this unnamed approach HECFI in the remainder of this work but want to note that its origins stem from HAFIX.

In HECFI, label checks for indirect calls are enriched with trampolines. Simple label-based approaches assign the same label to all functions, which are indirectly called from multiple places, and thus introduce some imprecision in the enforced CFG. Trampolines improve on that and act as an intermediate step between caller and callee where the actual target is compared to a jump table of allowed call targets. A failed lookup in this table indicates a manipulated call and results in a CFI exception. With this concept, the function call is CFI-enforced in a very fine-grained way because every indirect control flow transfer has a maximum of one assigned trampoline. The direct jump from the trampoline to the actual stack then needs no additional CFI protection. Backward edges are secured with a shadow stack. The authors used a SPARC LEON3 processor on an FPGA board for their evaluation. They reported an average run-time overhead of 1.75%, average code size overhead of 13.5% and area overhead of 1.78%.

E. Intel CET

Intel published the specification for their hardware-assisted CET in 2016 [20]. To the best of our knowledge, the concept, which is first used in the 2020 Tiger Lake CPU generation, is the first commercially available CFI implementation remotely comparable to the previously described CFG-based concepts. Intel combines a shadow stack for backward-edge protection with a coarse-grained approach for indirect branches called Indirect Branch Tracking (IBT).

With IBT enabled, all targets of indirect branches are instrumented with a custom ENDBRANCH instruction. Whenever an indirect control flow transfer occurs, a state machine internal to the CPU makes sure that the transfer targets such an instruction. This is very similar to what is described as Branch Limitation in other concepts. Intel’s coarse-grained approach eases practical problems in supporting very complex applications, where the extraction of a fine-grained CFG might not be possible. Presumably, it also helps integrating the concept into high-end x86 CPUs.

We have performed some basic build tests with Intel’s own ICC 19.0.1, GCC 10.2 and Clang 11.0.0. All of them are able to instrument their outputs with ENDBRANCH instructions to exploit this feature but it has to be enabled explicitly. They act conservatively in the sense that any function entry is instrumented if the compiler cannot derive with certainty that the respective function is not called indirectly. To allow the compilers to do so one can declare functions as static or enable link-time optimization (LTO). In order to enable a fair comparison, we improved on this behavior and instrumented the targets of indirect control flow transfers only.

In Intel’s CFI implementation ENDBRANCH uses an encoding that is interpreted as a (multi-byte) NOP instruction by legacy hardware allowing for backwards compatibility within a single binary. In our basic emulation of this scheme on RISC-V this is emulated by a custom 4-byte instruction.

While CET targets a different class of processors and protection on forward edges is less fine-grained in comparison to the previously described approaches, its inclusion in our evaluation gives insights into possible gains of following a coarse-grained approach.

F. EXCEC

We present an enhanced hardware-based CFI scheme called EXtensive CFI Enforcement Concept (EXCEC) that is based on what we consider the best concepts and ideas from the existing approaches described in the previous sections. As we will later show in Section V, EXCEC outperforms comparable approaches in terms of run-time overhead and code size while keeping hardware complexity at similar levels. We manage to do this while maintaining the security level of fine-grained CFI and supporting often omitted language features that complicate implementation of the CFI mechanism.

EXCEC offers protection for both forward and backward facing edges. In addition to basic CFI enforcement on indirect function calls, we have added protection of indirect jumps, dedicated recursion handling and support for set jmp calls. The custom CFI instructions required for CFI enforcement are shown in Table I.

| Instruction       | Description                                                                 |
|-------------------|------------------------------------------------------------------------------|
| CFI_CALL label    | Announces label for indirect function call. Placed right before the call instruction. Enables label check in CFI module. |
| CFI_JUMP label    | Announces label for indirect jump. Placed right before the jump instruction. Enables label check in CFI module.          |
| CFI_CHECK label   | Compares label with the one of a preceding CFI_CALL or CFI_JUMP instruction. Placed in the entry of indirectly called functions and at targets of indirect jumps. Has no effect when not enabled by a preceding indirect jump or call unless the label is 0x0 (indicating a violation). |
| CFI_SETJMP index  | Stores current shadow stack pointer in CFI module at position of index when no preceding CFI_LONGJMP occurred. Otherwise, it unwinds the shadow stack to the previously stored position. Placed right after set jmp calls. |
| CFI_LONGJMP       | Announces longjmp to the CFI module for subsequent CFI_SETJMP instruction. Placed right before calls of longjmp.         |

Table I: CFI instructions for EXCEC
1) Forward Edges: For protection of forward edges we use label checks between the caller and the callee, similar to what Abadi et al. proposed in their original CFI paper [1]. Indirect function calls and jumps are annotated with custom CFI_CALL or CFI_JUMP instructions, which bring the CFI module in a state where it expects a CFI_CHECK with a matching label. In addition, we borrow the concept of *trampolines* from Sullivan et al. [31] in order to achieve a more fine-grained protection.

When an indirect call targets functions that are potentially called from multiple places, a common label-based approach would require to instrument all of these callers and callees with the same label. This of course reduces the precision of the abstract CFG used for CFI enforcement. However, *trampolines* help to solve this problem by introducing a unique intermediate step between some indirect function call and its targets. Figure 1 depicts the workings of an exemplary trampoline in EXCEC.

```
foo:
...
addi sp, sp, -4
sw s3, 0(sp)
lw s3, _tr_foo
CFI_CALL 0x42
call s3
...
ret

_tr_foo:
CFI_CHECK 0x42
cfi_check 0x42
lw s3, 0(sp)
addi sp, sp, -4
la t0, <lt>
beq s3, t0, lt + 4
la t0, <gt>
beq s3, t0, gt + 4
CFI_CALL 0x60
...
ret
gt:
CFI_CHECK 0x70
...
ret
```

Figure 1: Application of trampoline in EXCEC

When using this concept, the target of an indirect call is changed such that it points to its unique trampoline (_tr_foo in Figure 1), while storing the actual target address of the call on the stack. This control flow transfer is protected with a unique label (0x42 in the example). The trampoline itself contains a jump table with all valid call targets (lt and gt in this case) and checks whether the target address of the indirect function call, which is retrieved from the stack at the beginning of the trampoline, is contained in this table. When some matching entry is found, the trampoline branches to the intended function but bypasses the CFI_CHECK at its entry. Such a check is not required here because the branch is only a direct jump now. Otherwise, when no entry is found in the table, a CFI violation is triggered by the CFI_CHECK instruction at the end of the trampoline. This instruction is only reached when all previous lookups in the table failed. The jumps to a trampoline and from there further to the actual function are unidirectional, i.e., the function does not return to the trampoline but to its original call site.

Note that trampolines are only required for functions that can be called from multiple callers and are not generated otherwise. For frequently visited indirect call sites with many targets the order of branches in the trampoline influences the overall performance. Some kind of optimization, e.g., ordering them according to profiling information, can be applied to reduce runtime.

2) Backward Edges: We implement backward-edge CFI enforcement with a shadow stack to provide optimal protection. Unlike other concepts, we utilize existing RISC-V JAL/JALR and RET instructions for immediately manipulating the shadow stack. This is possible in our setup because we can directly access the respective signals in the core’s decoder. By doing so we are able to implement protection of function returns with zero run-time and code size overhead.

Furthermore, we do not store full 32-bit addresses on the shadow stack but only the bits [18:1], which cuts memory demands of the stack almost in half. This is reasonable because the remaining bits are not relevant in our environment. First of all, instructions always start at even addresses in the RISC-V ISA, meaning the LSB is always 0. In PULPissimo’s memory map the 13 MSBs have a fixed value because of the limited use of address space, which makes storing and comparing them meaningless. This reduction to the relevant bits is of course only possible in our setup and might not be generally applicable.

Dedicated recursion handling is implemented for EXCEC in order to reduce utilization of the shadow stack. Configurable counters are attached to all stack entries to keep track of the recursion depth. This allows for precise monitoring of both recursive and non-recursive function calls.

EXCEC also supports set jmp calls similarly to [9]. To that end, we store the current shadow stack pointer when set jmp calls occur. Later, when the stack is unwound because of a long jmp call, the CFI module also unwinds the shadow stack to the index previously stored.

We have implemented custom CFI management commands in addition to the instructions already presented in Table I. CFI_ENABLE and CFI_DISABLE can be used to turn CFI protection on, respectively off. This is used to exclude certain sections like the startup code. Any CFI instruction occurring while CFI is disabled is handled as a NOP and has no further effect. CFI_RESET resets all internal CFI registers and disables CFI. We use the reset, for example, when an exit occurs because the shadow stack would otherwise not be unwound.

The correct sequence of the instructions listed in Table I is enforced with an internal state machine. We show all of such valid sequences in Figure 2. In particular, the indirect control transfer instructions JR and JALR must be followed by CFI_CHECK. JR and JALR are always inherently preceded by CFI_JUMP or CFI_CALL due to the instrumentation. CFI_CHECK makes sure the labels match. Similarly, RET compares the data from the top of the shadow stack with the return address. Any deviations result in a CFI violation, which triggers an exception in the core’s pipeline controller that leads to immediate program termination if no exception handler recovers from this situation. Instrumentation ensures that CFI_CALL and CFI_JUMP only occur before control flow transfers. CFI_CHECK with label 0x0 always triggers a CFI exception.

Reacting upon such exceptions would make it possible to, for example, log the error cause and reset otherwise left dirty
CFI registers with the previously mentioned \texttt{CFI\_RESET} instruction. In addition, the CFI module tests whether the stack is already full before pushing a new entry (or whether a bound recursion counter is exceeded), respectively whether it is empty before popping one. While the former is technically no CFI violation, the latter hints at an invalid control flow.

![Diagram of instruction sequences in EXCEC](image)

3) **Interrupts:** Unlike the referenced work on fine-grained CFI enforcements we make sure that regular interrupt handling is not perturbed. To that end, we enforce atomicity on all guarded control flow transitions by disabling interrupts temporarily while the CFI state machine is active, i.e., between the \texttt{CFI\_CALL} and \texttt{CFI\_JUMP} and \texttt{CFI\_CHECK} instructions. This guarantees consistency of EXCEC’s internal state and enables the enforcement of CFI even in interrupt service routines (ISRs) at the cost of a few additional cycles of interrupt latency.

IV. Evaluation

A. **Platform**

We implemented all of the CFI schemes discussed in this work on the open-source PULP platform [L 36], which contains the fully synthesizable PULPissimo microcontroller architecture [L 37] as well as the associated RISC-V toolchain [L 38] and SDK with platform-specific code [L 39]. In our setup, the PULPissimo SoC has one 16 MHz CPU core and a total of 512 KiB of memory, which limits possible benchmark applications. The system comes with two selectable 32-bit core variants, namely CV32E40P [L 40] (formerly RISCY [16]) and Ibex [L 41] (formerly Zero-riscy [27]). We decided to use the CV32E40P core since it is the more capable default selection and bears a closer resemblance to commercial platforms that presumably are most likely to get additional security features (which is a monetary burden for SoCs based on very small cores). CV32E40P is an in-order core with a 4-stage pipeline and implements the standardized RISC-V extensions for compressed instructions, integer multiplications/division and (optionally) floating point operations additionally to the base integer ISA. A PULP-specific extension is also supported, adding for example dedicated hardware loops and bit-wise operations. The core does not come with caches but uses a prefetch buffer for instruction fetching. For evaluation we used a Xilinx Zedboard [L 42], which has the Zynq Z-7020 SoC-FPGA installed. We only used its programmable logic (PL) part that offers 53,200 LUTs and 106,400 FFs. All benchmarks presented here result from executions on this FPGA with the GCC options \(-02\) \(-g0\). We also used the \(-fno-optimize-sibling-calls\) flag in order to disable sibling- and tail recursive call optimizations, which are not compatible with CFI. This is because such calls violate the principle that function calls must return to their original call site. Not doing so leads to CFI inconsistencies on backward edges, e.g., with shadow stacks [9]. In this configuration, the PULPissimo SoC with the CV32E40P core achieves a CoreMark [L 43] score of 43.85 and 37.44 with and without the PULP extension (i.e., 2.74 and 2.34 CoreMarks/MHz), respectively, with GCC 7.1.1.

B. **Instrumentation**

All control flow transfers span a CFG that is required for the instrumentation process. CFG information is implicitly available for direct branches and function returns at build time. Indirect jumps and calls, however, require explicit information. The precision of the resulting CFG directly translates to granularity of CFI protection. Extracting the possible set of targets of indirect control flow transfers in order to construct such a CFG perfectly is (in general) undecidable [18] and out of the focus of this work.

Therefore, we have manually prepared CFG information on all indirect calls in the chosen benchmark applications. This resembles what a perfect compiler would do and thus might be more precise than automatically generated CFGs. CFG information consists of a list of indirect control flow transfers identified by file name, function name and line number where they occur, along with a label for forward edge protection. This approach is practicable because only five of our benchmark applications use indirect function calls at all in their actual code and none contains indirect jumps other than the ones generated with jump tables for switches.

To make full use of symbol information available at build time, we have implemented instrumentation by means of a GCC plugin. GCC performs various phases called passes and allows external plugins to register additional passes. Our plugin is hooked in as one of the very last steps to be executed where we determine for each function if and where CFI instructions need to be injected.

We use LTO in order to enable unified optimization when linking all compilation units. This allows us to also instrument the target-specific functions statically linked from the PULP SDK. Unfortunately, the \texttt{libgcc} library that implements all compiler builtins (e.g., to handle arithmetic operations that the target processor does not support) cannot be properly built to support LTO as of this time. While this is not a fundamental flaw of our approach, any calls to functions of \texttt{libgcc} cannot be properly instrumented because they have to be linked unmodified without LTO. Therefore some functions, for example those declared by \texttt{math.h}, need to be excluded from CFI instrumentation. Otherwise only calls of respective functions would be instrumented but not their returns, which breaks backward edge protection concepts. We
add NOPs instead wherever possible to account for the missing instrumentations so that we achieve the same result in terms of run-time- and code size overhead in the end. Our implementation of Intel CET particularly suffers from this limitation because its CFI module automatically switches to a state where a specific instruction is expected upon every indirect jump and call. We cannot inject these expected instructions into libgcc code, which forced us to disable CFI enforcement for CET during our benchmarks. This does, however, neither affect performance nor code size and thus does not harm comparability with other concepts because indirect function calls in libgcc are nowhere instrumented.

C. Benchmarks

Our evaluation is based on a set of 39 applications, most of which are part of respected benchmark suits. To enable a meaningful evaluation and avoid any selection bias we include a wide range of diverse and commonly used programs for embedded systems tests. The restriction on embedded applications is primarily necessary due to the memory constraints of our platform. In most cases it was possible to port and execute whole suits.

A key component is CoreMark [L 43], which is an industry standard for benchmarking embedded CPUs. We also use all programs of the Embench-IoT suite [L 44] and all single-threaded applications of UCB’s RISC-V benchmarks [L 45]. Furthermore, we use a selection of small programs from the MiBench suite [L 46]. The excluded programs are not suitable for embedded platforms due to large problem sets or using file I/O. In addition, we included three supplementary custom applications for dedicated recursion tests.

In total, five out of the 39 applications contain indirect function calls, which is particularly relevant for evaluating run-time overhead of forward edge CFI protections. While their focus on embedded applications might seem to limit the possible conclusions drawn, the distribution of instructions for control flow transfers is not vastly different in much bigger applications [4]. However, with some work loads this can be significantly different: For example, interpreters have a notoriously high amounts of indirect control transfers of about 5–10% of all executed instructions [15].

The selected benchmarks work with all of our hardware-based CFI implementations, with two exceptions: slre of the Embench-IoT suite contains nested recursive calls, which are not supported by HAFIX, and towers of the RISC-V benchmarks for HCFI, also because of problems with recursion. We omit these two applications when computing aggregated results of the run-time overheads for all of our CFI implementations.

The only changes to the original benchmarks’ code are a unified approach for timing for all applications, which we implemented by reading the RISC-V Control and Status Registers (CSRs) for cycles and instructions before and after executing the benchmark’s actual core algorithms, and some minor modifications such as replacements for library functions not provided by the PULP SDK. In addition, we had to decrease the problem set size for qsort and susan (both from the MiBench suite) due to the memory size limitations of the platform. For the same reason we have increased the stack size of applications from 2 KiB to 18 KiB. Execution of multiple benchmarks would not be feasible otherwise.

D. Implementation parameters

We first define the set of common parameters shown in Table II in order to enable a meaningful comparison of the hardware utilization overhead entailed by various CFI concepts. They specify the dimensions of all relevant memory elements and are employed in a consistent way throughout all implementations wherever applicable. The values are based on our set of benchmarks but also consider constraints imposed by the limited hardware resources available on the FPGA.

| Parameter                | Value |
|--------------------------|-------|
| SHADOW_STACK_SIZE        | 128   |
| RECURSION_DEPTH          | 128   |
| INDIRECT_CALLS           | 64    |
| INDIRECT_JUMPS           | 64    |
| INDIRECTLY_CALLED        | 64    |
| NUM_FUNCTIONS            | 1024  |
| SETJMP_CALLS             | 8     |

Table II: Common implementation parameters

The call depth of nested function calls never exceeds 50 in our applications. This is particularly true for non-recursive programs, where call depth hardly exceeds 10. The SHADOW_STACK_SIZE parameter used allows for some realistic headroom in other applications and bigger data sets. RECURSION_DEPTH defines the maximal supported recursion depth used in CFI concepts with dedicated recursion handling using counters (with a width of 7 bits in the evaluation).

A value greater than the supported stack size is not meaningful, considering that some CFI schemes do not specifically handle recursion at all. INDIRECT_CALLS, INDIRECT_JUMPS and INDIRECTLY_CALLED gives the numbers of indirect calls, jumps and indirectly called functions, respectively, and thus determine required label widths and matrix dimensions. Those are based on observations regarding the number of indirect control flow transfers in our set of benchmark applications. NUM_FUNCTIONS specifies the total number of functions a program may contain. This information is required, for example, to determine the dimensions of the Active Set. Eventually we use SETJMP_CALLS to define the number of distinct setjmp calls supported. We note that none of the programs we use for evaluation contains such calls. Where available, the respective hardware mechanisms have been enabled for completeness and verified by custom test cases.

The parameters presented here can be translated directly to FF demand. For instance, a common shadow stack requires 128x32 FFs on our 32-bit platform when applying the SHADOW_STACK_SIZE we defined in in Table II. Naturally, doubling the shadow stack size to support 256 nested function calls doubles its FF requirements and also needs significant
amounts of additional LUTs and multiplexers (MUXs). This must be taken into account when discussing dimensions of every memory element.

V. RESULTS

Implementations of the previously presented CFI approaches on a common platform made it possible to generate meaningful benchmark results. In this section we first give an introductory overview of the protectional scope of the respective CFI implementations and then present comparisons of the introduced overheads.

A. Security

The CFI schemes presented in this work mostly support different CFI protection mechanisms. We give a brief overview in Table III, although qualitative security evaluations are not our focus. The table shows which control flow transfers are protected by each of the CFI schemes. Fine-grained CFG means that the respective approach is based on some precise CFG and does not only protect control flow transfers in a way similar to Branch Regulation. We refer again to [14] and the respective papers for details on each of the CFI approaches.

The functional scope of CFI schemes must be considered when interpreting the overheads on run-time performance, code size and hardware utilization, which we present in the following sections. However, it is also important how certain features are implemented. For example, FIXER and HCFI offer the same functional scope in principle but use very different concepts for forward edge protection. HAFIX on the other hand only protects function returns by means of an Active Set, thereby sacrificing some granularity. CET only enforces CFI based on overapproximated, i.e., coarse-grained, CFGs on forward edges, which is far less restrictive and thus prevents less attacks. These important distinctions will also be reflected in the following evaluation results.

B. Performance

Arguably the most important aspect when comparing CFI schemes is their impact on the runtime of applications. Figure 3 shows the relative performance overhead for all CFI implementations as an average over all benchmark applications. CET and EXCEC each introduce no more than 0.16% overhead, which is due to the fact that these two concepts do not require additional instructions for backward edge protection but extend semantics of existing branch instructions instead. Quite the opposite can be seen for HAFIX with an extra of 1.96% because every function call involves at least three additional instructions, which is more than any other concept. FIXER, HCFI and HECFI follow a similar approach for backward edge protection, what explains why their results are close. Forward edge protection, which is required less frequently, accounts for minor differences only. However, applications with a large share of indirect function calls represent a worst-case scenario for most CFI schemes: Their different instrumentation concepts lead to an overhead of up to 4 CFI instructions for every indirect call. Schemes, that offer a very fine-grained protection by using trampolines can even add a multiple of this number in case they are needed.

For some combinations of CFI schemes and benchmark applications the CFI variants actually resulted in a lower execution time compared to a run without CFI enforcement. Instrumentation with CFI instructions naturally changes the alignment of symbols within the .text section, which in individual cases even leads to improved performance. A significant share of cycles, which make up these effects, can be traced to stalls resulting from non-ideal instruction fetches from memory. For that reason we consider the number of executed instructions instead of the cycles required for execution throughout the evaluation. Instruction counts are not affected by the above mentioned phenomenon. Also, all run-time overheads presented here represent the average overhead for executions with and without using the PULP extension available on our platform. As we later discuss, these account for considerable differences in individual cases, which are not strictly related to CFI enforcement.

The detailed effects of CFI protection on runtime for all CFI schemes are shown in Table IV. The numbers represent the relative overhead compared to a baseline without CFI enforcement. Indirect function calls make up only a small minority of forward control transfers and are contained in only 5 of our benchmark applications: In coremark indirect function calls make up 15.4% of all function calls, in picojpeg 0.1%, in wikisort 25.7%, and in bitcount 61.2%. The sglie benchmark contains indirect call instructions but they are never executed due to dynamic checks. Indirect jumps are only marginally used for jump tables in picojpeg and qrduino.

The averaged numbers shown before in Figure 3 hide significant deviations of particular benchmarks. Therefore, we specifically analyze the remarkable results of some benchmark applications as seen in Figure 4 to make them more

| Function returns | FIXER | HAFIX | HCFI | HECFI | CET | EXCEC |
|------------------|-------|-------|------|-------|-----|-------|
| Indirect calls   | ●     | ○     | ●    | ●     | ●   | ○     |
| Indirect jumps   | ○     | ○     | ●    | ●     | ●   | ○     |
| Fine-grained CFG | ●     | ○     | ●    | ○     | ●   | ○     |
| Protected Interrupts | ○     | ○     | ●    | ○     | ●   | ○     |

Table III: Overview of supported CFI protection scope

Figure 3: Relative runtime performance overhead

| Relative overhead [%] | FIXER | HAFIX | HCFI | HECFI | CET | EXCEC |
|----------------------|-------|-------|------|-------|-----|-------|
| 0                    | 0     | 0     | 0    | 0     | 0   | 0     |
| 1                    | 0.1   | 0.16  | 1.47 | 1.53  | 0.1 | 0.16  |
| 2                    | 1.37  | 1.96  |      |       |     |       |

The averaged numbers shown before in Figure 3 hide significant deviations of particular benchmarks. Therefore, we specifically analyze the remarkable results of some benchmark applications as seen in Figure 4 to make them more
direct function calls, meaning they introduce no direct run-time overhead for direct function call, or rather its return, resulting in their 15% about 7.5% of all instructions. For instance, HCFI and FIXER.

The opposite is true for recursive applications timed portion of the program only contains a small number of basicmath example, the case for the transfers of course entail fewer CFI instructions. This is, for comprehensible. Applications with hardly any control flow implementation, where calls make up about 7.5% of all instructions. For instance, HCIF and FIXER both require two additional instructions for protecting each direct function call, or rather its return, resulting in their 15% run-time overhead for factorial.

Intel CET and EXEC do not require instrumentation of direct function calls, meaning they introduce no direct run-time overhead at all for most applications. However, their performance numbers for coremark bear witness to the fact that it contains indirect branches. For all variants of CFI enforcements the results for coremark are relatively close to the average values shown in Figure 4. Indirect function calls also occur in bitcount, only now these make up for almost two thirds of all calls. The dhrystone benchmark contains particularly many direct function calls, as can be seen from the run-time overhead introduced by FIXER, HAFI, HCFI and HECFI.

The run-time performance overhead of HAFI and HECFI measured by us is more or less identical to what is stated in the original papers of the two approaches. Minor differences for the HCFI numbers presumably result from the set of benchmark applications. However, the performance indicators for FIXER need to be put into perspective because the original concept as described in [13] uses more instructions for instrumenting control flow transfers than our implementation does. We described the reasons before when introducing FIXER. The benchmarks used for evaluation in the original paper mostly only contain few function calls, so CFI protection is naturally very cheap there. The more extensive set of benchmarks used in this work would result in a significantly higher run-time overhead if instrumenting in the way proposed in the original concept.

The PULPissimo platform we used for all evaluations extends the RISC-V ISA with an optional PULP extension for platform specific instructions like hardware loops. These have a very positive effect on performance in many cases. For example, 92% more instructions are executed for the edn benchmark when compiling the application without the PULP extension and without any CFI enforcement. Minor impacts thereof are also reflected in the run-time performance overhead introduced by our CFI schemes though. We take this into account by always averaging run-time overheads of executions with and without PULP extensions.

In conclusion it can be said that all CFI schemes are very performant on average and differences are rather small. Noticeable differences can be seen in certain individual examples though, especially for applications containing an above-average number of (indirect) function calls. In some extreme cases it might be beneficial to benchmark the set of actual applications to be executed to determine the most suitable CFI enforcement scheme.

C. Hardware Utilization

Our CFI implementations affect the maximum frequency of the overall hardware design to a small extent. The vanilla PULPissimo platform with the CV32E40P core can be synthesized for the ZedBoard with 16 MHz without any timing violations and still some margin available. Most implementations have negligible impact on the timing but FIXER decreases the available margin noticeably. In our implementation, of all concepts FIXER also introduces the most levels of logic (i.e., the highest amount of combinational elements between any two synchronous points) in its CFI module. The reason is

| Benchmark | FIXER | HAFI | HCFI | HECFI | CET | EXEC |
|-----------|-------|------|------|-------|-----|------|
| coremark  | 1.42  | 2.13 | 1.53 | 1.64  | 0.11| 0.22 |
| aha-mont64| 0.06  | 0.08 | 0.06 | 0.06  | 0.00| 0.00 |
| crc32     | 0.00  | 0.00 | 0.00 | 0.00  | 0.00| 0.00 |
| basicmath | 0.28  | 0.28 | 0.28 | 0.28  | 0.00| 0.00 |
| nbody     | 1.07  | 1.07 | 1.07 | 1.07  | 0.00| 0.00 |
| ssort     | 0.00  | 0.00 | 0.00 | 0.00  | 0.00| 0.00 |
| sort      | 0.00  | 0.00 | 0.00 | 0.00  | 0.00| 0.00 |
| spmv      | 1.43  | 1.43 | 1.43 | 1.43  | 0.00| 0.00 |
| towers    | 5.52  | 8.28 | n/a  | 5.52  | 0.00| 0.00 |
| basicmath | 0.28  | 0.28 | 0.28 | 0.28  | 0.00| 0.00 |
| dijkstra  | 5.95  | 8.93 | 8.93 | 10.75 | 2.98| 4.80 |
| bitcount† | 0.15  | 0.15 | 0.15 | 0.15  | 0.00| 0.00 |
| fff       | 0.66  | 0.66 | 0.66 | 0.66  | 0.00| 0.00 |
| ssort‡    | 0.76  | 1.15 | 1.15 | 0.76  | 0.00| 0.00 |
| stringsearch | 0.00 | 0.00 | 0.00 | 0.00  | 0.00| 0.00 |
| susan‡    | 0.08  | 0.08 | 0.08 | 0.10  | 0.00| 0.00 |
| factorial | 14.88 | 22.31| 14.88| 14.88 | 0.00| 0.00 |
| nqueens   | 0.77  | 1.15 | 0.77 | 0.77  | 0.00| 0.00 |
| tak       | 7.26  | 10.89| 7.26 | 7.26  | 0.00| 0.00 |

Table IV: Detailed runtime performance overhead [%].

* excluded from aggregated results due to missing support contains indirect function calls† or jumps‡
† reduced problem set
that its significant amount of memory also requires a lot of associated logic, especially for the policy matrix lookup.

When evaluating hardware utilization overhead, we differentiate between LUTs and FFs. While the former is more sensitive to implementation details, the latter mostly depends on the dimensions used for the various memory elements. We defined the parameters used for such components in Section IV-D. Figure 5 shows the resulting utilization overhead for all of our CFI variants. Note that absolute numbers are shown here instead of relative increases to ease future comparisons with other platforms. We discuss how the respective FFs demands are composed below. Unfortunately, additional LUTs can not be trivially assigned.

Optimization EXCEC would require 10,070 LUTs and 5,318 FFs, i.e., about 67% and 54% more overhead.

Most parts of FF demand can be directly deduced from the dimensions of required memory modules. For example, the 64x64 policy matrix used in FIXER requires 4096 FFs with the parameters defined in Table II. The associated address decoder, which we implemented as a 64x18 lookup table, accounts for 1152 FFs and the 128x32 bit shadow stack is built from another 4096 FFs. Other small registers make up the difference to the sum shown in Figure 5. EXCEC’s reduced shadow stack width results in a lower requirement of 2304 FFs (128x18).

It becomes apparent that approaches, which are based on some sort of policy matrix, are hard to implement and very expensive. Matrix dimensions are defined by the numbers of supported callers and callees. Doubling these parameters would quadruple the number of required FFs. In contrast, label-based concepts hardly require any resources but still offer a good CFG precision when being used with fine-grained labels or in combination with trampolines.

A direct comparison with the hardware utilization overhead stated in the original papers of the respective CFI concepts is hardly meaningful: The dimensions of various memory elements are mostly unknown and the different platforms used for evaluations vary greatly. For example, about 2.5% of additionally required FFs are reported for both HAFIX and HCFI and a general area overhead of 2.9% is specified for FIXER. These numbers differ significantly from ours – sometimes even by a magnitude.

### D. Code Size

The effects of CFI instrumentation on the .text section size are shown in Figure 6. Note that the figure shows a logarithmic scale in order to better represent the differences. In general, great outliers can be seen for all CFI implementations. Particularly small code size overheads are introduced by applications with only few function calls, and vice versa.

FIXER and HCFI show an almost identical overhead because the two concepts follow a very similar approach when it comes to instrumenting direct branches. Both add one instruction each to the caller and callee for every function call. The Active Set approach used in HAFIX on the other hand requires instrumentation of every function, regardless how often it is invoked, and an additional instruction for
addition, we unify the most promising concepts and ideas state-of-the-art CFG-based hardware-assisted CFI schemes. In small share of all control flow transfers. indirect control flow transfers, which only account for a very differences in the results stem from the instrumentation of of them needs to instrument direct function calls. Only minor larger. CET and EXCEC stand out positively because neither of executed instructions, but the code size is significantly differences. The biggest outlier over all dimensions is FI. The biggest outlier over all dimensions is FIXER’s hardware utilization, which is caused by its expensive policy matrix. Apart from that, the proportionally small performance overheads of all implementation seem to be almost negligible in comparison.

**E. Summary**

We present a final summary of the impact of CFI enforce-ment on the previously described aspects performance, binary size and hardware utilization in Figure 7. For clarity the figure shows the relative overhead of hardware utilization as average of LUTs and FFs increase. When ignoring security aspects then Intel CET and EXCEC appear equivalent in this very simplified representation. However, EXCEC enforces a much more fine-grained CFI. The biggest outlier over all dimensions is FIXER’s hardware utilization, which is caused by its expensive policy matrix. Apart from that, the proportionally small performance overheads of all implementation seem to be almost negligible in comparison.

**VI. CONCLUSION**

In this work we present an extensive evaluation of various state-of-the-art CFG-based hardware-assisted CFI schemes. In addition, we unify the most promising concepts and ideas into a novel and precise CFI approach called EXtensive CFI Enforcement Concept (EXCEC).

The elaborate set of benchmarks that has been ported to as well as the usage of a single platform allows for a fair, transparent and thorough evaluation. The instrumentation is carried out largely automatically by a compiler plugin without the need to change the latter directly. The results reveal the biggest differences in hardware costs and many implementations require a non-negligible amount of additional instructions inserted to the binaries increasing their size.

Our own protection scheme is shown to be more efficient in terms of run-time performance and binary size while involving an average hardware utilization overhead and enforcing a fine-grained CFG. We prove with this approach that fine-grained CFI enforcement can be achieved with even less overheads than previously demonstrated, even if peculiar details (e.g., set jmp) are handled. It follows that here is no need to resort to less precise and most often even costlier solutions as long as the CFG is available.

We have released all our implementation artifacts including the Verilog hardware descriptions, GNU Binutils, and the GCC plugin as open-source in Git repositories [32].

**A. Future Work**

The focus of this paper lies on benchmark applications written in C because of constraints imposed by the PULP SDK. However, an extension of our GCC plugin for C++ support would allow us to investigate the challenges to CFI enforcement posed by object-oriented languages.

Our instrumentation is based on partially manually con-structed CFGs, which is practicable for academic evaluation but lacks broad applicability. A combination of our instrumen-tation with some framework for extractingCFG information from source code would alleviate this problem.

The modularity of our hardware mechanisms opens up opportunities to examine the effects of CFI enforcement on other platforms, e.g., out-of-order pipelines, multi-core CPUs or alternative ISAs. While the protection of the CFI state (e.g., shadow stack contents and FSM state) from deliberate direct manipulation in the current scheme is an important security feature in embedded systems without layered privileges it also prohibits an effective implementation of preemptive multitask-ing. Providing privileged instructions to access this internal data would allow an operating system (OS) to spill the state to memory during context switches. Similarly, this could raze the upper limit on call depths and recursions. The way EXCEC handles interrupts could be applied for other asynchronous events such as (Unix) signals.

All of the above combined would also allow for imple-mentations and evaluations on larger systems including an OS since there are no fundamental obstacles to do so. Limiting CFI enforcements to selected processes only would enable a gradual migration for legacy applications. In such systems we predict an increased overhead due to additional indirect jumps, e.g., for dynamic linking, and from the bigger process metadata but this needs to be verified.
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