Design and Implementation of High Gain, High Unity Gain Bandwidth, High Slew Rate and Low Power Dissipation CMOS Folded Cascode OTA for Wide Band Applications

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Abstract
A novel differential input pair and single output OTA is designed in this paper. This FCOTA is designed by using current mirror and its enhanced gain parameter and also is reduce the power dissipation and increase the gain bandwidth. Simulation results are performed using Mentor Graphics software model for CMOS TSMC 180 nm process technology. The supply voltage is given 1.8 v. The designed FCOTA has different capacitive load and according its Gain, Unity Gain Bandwidth, Power Dissipation, Phase Margin and Slew Rate are measured. Gain, Unity Gain Bandwidth and Slew Rate are optimizing up to 97.37 db, 20.83 GHz and 3.5075 KV/µs respectively. The power dissipation reduces up to 8.31 µW. This FCOTA is designed for wide band application because of high gain and high bandwidth and low power dissipation.

Design Approach
One way of increasing the impedance is to add some MOSFETs at the output side or in second stage to include for using an active load. MOSFETs are stacked on top of each other. The MOSFETs have been chosen to ensure the largest gain required. For a folded OTA bandwidth performance is high. So here N-MOS input pair and second stage is cascode stage and third stage is biasing stage. Current mirror is one type of approach to copy current at output side [4].

\[ I_{out} = \left( \frac{W}{L} \right)^2 I_{ref} \]

Constructing the bias circuit of an amplifier to provide the required bias current [7]. Transistor trans-conductance is the most important parameters in amplifier that must be stabilized. In general biasing of an amplifier is to ensure the proper operation of the circuit.

Design Analysis
This schematic design is consisting of three stages. First stage is NMOS input pair, second stage is cascode stage and third stage is biasing circuit. The input stage is designed by N-MOS input pair. Due to the greater mobility of NMOS device, PMOS input differential pair has a lower transconductance than carrier a NMOS pair. Thus, NMOS MOSFET has been chosen to ensure the largest gain required. For a folded OTA bandwidth performance is high. So here N-MOS input pair is applied for high transconductance. So as shown in Figure 2 M1 and M2 are NMOS input pair MOSFETs.

MOSFETs M1 and M2 are input pair of the OTA. M1 transistor work as a load register of MOSFET pair. Second Stage is the Cascode OTA with current mirror or it’s also called current mirror biasing.

Cascode stage design for higher isolation at input and output side, higher input impedance, higher output impedance, higher gain and higher bandwidth. So (M3, M4), (M5,M6) are NMOS pair and (M7,M8), (M9,M10) are PMOS pair working as a current mirror self biased. Third stage is biasing circuit. The width of the M12 is low because if the width of M13 is higher the internal resistor value will increase.

Keywords: Folded cascode structure; Current mirror; Gain; Unity gain bandwidth; Power dissipation; Slew rate

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be low and its gate terminal is directly connected to the M11, which is work as a PMOS load resistor.

\[ g_{m1} = \mu \frac{W}{L} I_{ds1} (V_{gs} - V_{th}) \]

And internal resistance is defined by \( R_{\text{int}} \):

\[ R_{\text{int}} = (g_{m1}r_{th}) || (g_{m1}r_{th}) \]

So, Voltage gain \( A \):

\[ A = g_{m1}R_{\text{int}} \]

\[ A_1 = g_{m1}R_{\text{int}} \text{ where, } g_{m1} = G_{m1} \]

Internal resistance of M8 is represent as \( r_{th} \) and it’s defined as

\[ r_{th} = \frac{1}{\lambda I_{ds}} \]

Where, \( \lambda \) is channel length modulation and \( I_{ds} \) is the drain current.

\[ I_{ds} = \frac{1}{2} \mu \frac{W}{L} \left( V_{gs} - V_{th} \right)^2 \]

There are two poles exits and it is denoted by P1 and P2

\[ P_1 = \frac{1}{R_{\text{out}} C_L} \]

Where \( R_{\text{out}} = g_{m1}r_{th} \left( 2r_{th} \parallel r_{th} \right) \)

According to mathematical calculation, there are minor changes in mathematical calculation and theoretical calculation. Now, there is present waveform of FCOTA’s schematic.

### Performance Parameter

Table 1 presents different sizes of MOSFETs according to its operation.

Table 2 represents the summary of proposed performance parameter using 180 nm technology. There are different capacitive load such as 1 pF, 2 pF and 5.6 pF.

### Simulation Result

All simulation results are measured by using 180 nm or 0.18_m technology using Mentor Graphics-Pyxis (Figures 3-6).

### Conclusion

A novel design of Folded Cascode Operational Transconductance Amplifier (FCOTA) using current mirror as self biasing and biasing of the driving stage has been presented in this research work. The proposed design of FCOTA has been simulated and analyzed using Mentor Graphics tools. Improvement in performance parameters such as Gain up to 97.36 db, UGB up to 20.83 GHz, Reduction in Power Dissipation is 8.31 W and Slew Rate enhanced up to 3.5075 KV/\( \mu \)s has been achieved with respect to reference papers designs. So this FCOTA is designed for low power, high gain and high UGB. And it’s used for wide band applications.

### Performance Parameter

| Parameters | CL=1pF | CL=2pF | CL=5.6pF |
|------------|--------|--------|----------|
| Gain (db)  | 58.37  | 97.37  | 68.48    |
| Gain Margin(db) | N.A | 14.89 | 20.86 |
| Phase Margin (°) | 62.5 | 38.32 | 26.3 |
| UGB       | 315 MHz | 20.83 GHz | 247.1 MHz |
| Slew Rate | N.A | 3.5075 KV/\( \mu \)s | 92.8V/S |
| Power Dissipation | 540 \( \mu \)W | 8.31 \( \mu \)W | 2.943 mW |

Note: CFC = Conventional Folded Cascode
Figure 3: 1 pF Capacitive Load.

Figure 4: 2 pF Capacitive Load.
Figure 5: 5.6 pF Capacitive Load.

Figure 6: Slew Rate.
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