Abstract

A modular, programmable, and high performance Power Gating strategy, called cluster based tunable sleep transistor cell Power Gating, has been introduced in the present paper with a few modifications. Furthermore, a detailed comparison of its performance with some of the other conventional Power Gating schemes; such as Cluster Based Sleep Transistor Design (CBSTD), Distributed Sleep Transistor Network (DSTN) etc.; has also been presented here. Considering the constraints of power consumption, performance, and the area overhead, while doing the actual implementation of any Power Gating scheme, it becomes important to deal with the various design issues like the proper sizing of the sleep transistors (STs), controlling the voltage
drop (IR drop) across the STs, and obviously maintaining a desired performance with lower amount of delay degradation. With this notion, we tried to find out an efficient Power Gating strategy which can reduce the overall power consumption of any CMOS circuit by virtue of reducing the standby mode leakage current. Taking the different performance parameters into account, for an example circuit, which is actually the conventional 4×4 multiplier design, we found that the modified tunable sleep transistor cell Power Gating gives very much promising results. The reported architecture of the 4×4 multiplier with the tunable sleep transistor cell Power Gating, is designed using 45 nm technology and it consumes 1.3638×10⁻⁵ Watt of Average Power while being operated with the nominal case of the bit configuration word, that is, "1000". At the same time, this design provides a delay of 2.5455×10⁻¹⁰ second, which conveys a 2.29% improvement in the performance with respect to the best case delay as obtained in case of the conventional Power Gating scheme. The entire simulation work has been done using SPICE, whereas the results are obtained for a Supply Voltage (Vdd) of 1 Volt and a frequency of 200 MHz.

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Index Terms

Computer Science

Power Electronics

Keywords

multiplier  Power Gating  leakage power  sub-threshold current  delay  critical path  IR drop  delay degradation  CBSTD  DSTN  tunable sleep transistor cell
