Implementation of a probabilistic subtractor based on a probabilistic adder

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Abstract. The paper provides basic mathematical calculations for performing arithmetic operations of addition and subtraction on operands represented as a non-positional probability mapping. The probabilistic form of presentation and transformation of information has undeniable advantages over the "classical" digital, which consist in reducing the hardware volume and increasing the performance of computing devices. A method for the implementation of probabilistic subtraction through probabilistic addition is proposed. A simulation was carried out, confirming the theoretical presentation.

1. Introduction
The principle of representing the value of any signal parameter by probability is not new [1 – 12]. With the development of digital computing and simulation methods, the method of statistical tests has become widely used, the main idea of which is the relationship between the probabilistic characteristics of random processes and quantities that are solutions to mathematical analysis problems.

The advantages of the probabilistic form of data representation include the following:
- reducing the hardware volume of devices and, consequently, their linear dimensions and power consumption;
- reducing the cost of devices by reducing hardware costs;
- stability in the event of interference.

However, there are disadvantages, such as:
- limited range of measured values;
- operating with only positive or only negative numbers;
- the accuracy of calculations depends on the selected range and number of statistical tests.

Thus, we can conclude that creating universal probabilistic devices is a complex and time-consuming task. However, this form of data representation is particularly suitable for use in measuring systems, since the range of their measurement is limited by the range of signals sent from sensors, which allows you to take advantage of the probabilistic form of data representation and create accurate probabilistic devices based on it.

2. Problem statement
The purpose of this work is to improve the method for performing arithmetic subtraction operations in the probabilistic form of data representation.

The purpose of the study determines the tasks:
Performing the presentation of data in a probabilistic way.
Consider performing arithmetic operations of addition and subtraction in the probabilistic form of data representation.
Considering the disadvantages of the existing method of performing probabilistic subtraction, develop an improved method.
Simulate the operation of a probabilistic subtractor and analyze the results.

3. Performing arithmetic operations of addition and subtraction in the probabilistic form of data representation

The mathematical expectation of a random sequence $S$ can be considered as the sum of the mathematical expectations of probabilistic maps of its members [3, 13], i.e.

$$M[S] = M[Y_1] + M[Y_2] + ... + M[Y_N] = \sum_{i=1}^{N} \sum_{j=1}^{N} y_{ij} p_i = \sum_{i=1}^{N} P(y_{ij} = 1) = \sum_{i=1}^{N} P(R_j < (r = x_i)) = \sum_{i=1}^{N} F_{x_i}(R).$$

For an auxiliary random variable $R$ distributed uniformly, we have

$$M[Y_i] = \sum_{j=1}^{N} y_{ij} P_i = P(y_{ij} = 1) = x_i \quad \text{(2)}$$

and then we get

$$M[S] = \sum_{i=1}^{N} x_i. \quad \text{(3)}$$

As an estimate for the sum of input terms we get

$$\left( \sum_{i=1}^{N} x_i \right)^* = \frac{X_{\text{max}}}{K} \sum_{i=1}^{N} \sum_{j=1}^{K} y_{ij}, \quad \text{(4)}$$

where $y_{ij}$ – the j-th term of the probability map of the i-th operand.

Thus, the sum of the probabilistically represented values will be equal to the sum of the units included in the probabilistic representation of each of the operands, divided to the number of statistical tests $K$, multiplied by the value of the upper bound of the Xmax range [14 – 16].

Based on the above, the probability adder (figure 1) can be implemented on a binary counter, the input of which is fed probabilistic mappings of operands. In this case, the values of the probabilistic display of the second operand must be received via a single-step D-trigger that performs a delay of half the clock frequency period of the device. The estimate of the amount is read out through the census block, implemented by a group of gates in the form of a positional binary code.

To perform the subtraction operation, performing the same actions as for adding two summands, the second of which is taken with the opposite sign, we get from expression (1)

$$M[S] = M[Y_1] - M[Y_2] = F_{x_1}(R) - F_{x_2}(R). \quad \text{(5)}$$
For a uniform distribution of the auxiliary random sequence $R$ we have an expression for probabilistic subtraction

$$\left(x_1 - x_2\right)^* = \frac{X_{\text{max}}}{K} \sum_{j=1}^{K} (y_{1j} - y_{2j}).$$  \hspace{1cm} (6)

The probability subtractor will have the form shown in figure 2.

For the hardware implementation of the subtractor is necessary that the values of probabilistic display of minuend $y_{1j}$ were received at the summing input of the reverse counter, and on the subtractive input – values $y_{2j}$ via a single-stroke D-trigger, performing a delay of half the clock frequency period of the probability display of the subtracted relative to the probability display of the minuend. The difference estimation is read to the output via the census block implemented by the gate group as a positional binary code.

The difficulty of implementing a probabilistic subtractor in comparison with a probabilistic adder is the need to use a reverse counter. And when designing probabilistic computing devices, you will need to introduce an additional node compared to digital devices, where subtraction and addition operations are performed on the same device.

4. Improved method for performing probabilistic subtraction operations

As in the case of digital binary data representation, the probability representation operation can be implemented based on addition. In the digital binary number system additional and reverse code is used to perform subtraction. In the case of a probabilistic form of data representation, you can use an
inversion of the probabilistic display. When inverting all the digits of the probability sequence we get
\[ \overline{Y} = \{\overline{y}_1; \overline{y}_2; \ldots \overline{y}_j; \ldots \overline{y}_K\} = 1 - Y. \quad (7) \]

Applying this property to the first operand when adding two numbers, we get
\[ \overline{Y}_1 + Y_2 = (1 - Y_1) + Y_2 = 1 - (Y_1 - Y_2). \quad (8) \]

Converting the expression (8):
\[ \overline{Y}_1 + Y_2 = 1 - (\overline{Y}_1 + Y_2) = 1 - (1 - Y_1 + Y_2) = 1 - 1 + Y_1 - Y_2 = Y_1 - Y_2. \quad (9) \]

It can be seen from expression (9) that the difference between two probabilistically represented
numbers can be found in terms of the sum by inverting the first operand and the result of the operation.

In this case, you must apply rationing:
\[ (x_1 - x_2)^* = X_{\max} \cdot \left( 1 - \frac{\sum_{j=1}^{K} \overline{y}_{1j} + \sum_{j=1}^{K} \overline{y}_{2j}}{K} \right) = \frac{X_{\max}}{K} \left( K - \left( \sum_{j=1}^{K} \overline{y}_{1j} + \sum_{j=1}^{K} \overline{y}_{2j} \right) \right). \quad (10) \]

In accordance with expression (10), a probabilistic subtractor can be implemented on a binary
subtractor counter, in which the value \( K \) is pre-set. In this case, the values of the probabilistic display
of the first operand must be received through the inverter, and the second operand-through a single-
stroke D-trigger that performs a delay of half the clock frequency period of the device (figure 3).

![Figure 3. Improved probability subtractor.](image)

The structure of the scheme includes:
1 – inverter;
2 – disjunctor;
3 – single-stroke D-trigger;
4 – binary subtractive counter.

The processes in the probability subtractor scheme proceed in the following sequence. After filing
for the power plan in a binary subtractive counter takes on the value \( K \) – the number of statistical tests,
the probabilistic display of the minuend is fed to the inverter (1), at the output of which as a result of
inverting all the digits of the probability sequence we get the value \( 1 - Y_1 \), which is received at the first
input of the disjunctor (2). Subtrahend \( Y_2 \) enters the input of a single-stroke D-trigger (3), in which
the transmission delay of the probabilistic display of the subtrahend \( Y_2 \) is made by half-stroke then
with the direct output of a single-stroke D-trigger (3) probabilistic display of the subtrahend \( Y_2 \).
supplied to the second input of disjuncture (2), at the output of which the value of the sum of probability mappings $Y_1 + Y_2$ is formed, which is received at the information input of the subtracting counter, at the output of which it is formed, in accordance with the expression (9), difference $(x_1 - x_2)^Y = Y_1 - Y_2$.

Figure 4 shows a mathematical model of a probabilistic adder and an advanced subtractor performed in Mathcad.

The presented model corresponds to the stated analytical calculations and confirms them.

Figure 4. The model is probabilistic adder and subtractor.

The advantage of the improved probability subtractor is that the reverse counter is replaced by a subtractor, whose hardware implementation is much simpler.

The hardware volume of this scheme is 10 times less than the classic digital subtractor.

5. Conclusion

As a result of this work, the possibility of implementing probabilistic subtraction through probabilistic addition based on the inversion of the probabilistic mapping is shown. This makes it possible to use devices containing a probabilistic subtractor in the design of measuring systems and use a subtractive counter instead of a reverse counter, the hardware implementation of which is much simpler.

To test the theoretical calculations, the probability adder and subtractor were modeled in Mathcad. Theoretical calculations are confirmed by simulation results.

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