A New Process for On-Chip Inductors with High Q-Factor Performance

Kevni Büyüktas, Klaus Koller, Karl-Heinz Müller, and Angelika Geiselbrechtinger

Department Automotive/Industrial, Infineon Technologies AG, Am Campeon 1-12, D-85579 Neubiberg, Germany

Correspondence should be addressed to Kevni Büyüktas, kevni.bueyuktas@infineon.com

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A novel technological method to improve the quality factor (Q) of RF-integrated inductors for wireless applications is presented in this paper. A serious reduction of substrate losses caused by capacitive coupling is provided. This is realised by removing the oxide layers below the coils with optimized underetching techniques. This special etching procedure is used to establish an environment in the inductor substructure with very low permittivity. A set of solid oxide-metal-columns placed below the metal windings stabilize the coil and prevent the hollowed out structure from mechanical collapse. The oxide capacitance is lowered significantly by the reduction of the permittivity \( \varepsilon \) from values around 4 to nearly 1. Capacitive coupling losses into substrate are decreasing in the same ratio. The resulting maximum Q-factors of the new designs are up to 100% higher compared to the same devices including the oxide layers but shifted significantly to higher frequencies. Improvements of \( Q \) from 10 up to 15 have been obtained at a frequency of 3 GHz for a 2.2 nH inductor with an outer diameter of 213 \( \mu \)m. The resonance frequency (\( f_{\text{res}} \)) and frequency at maximum \( Q \) (\( f_{Q_{\text{max}}} \)) are shifted to higher frequencies, caused by the shrunk total capacitance of the structure. This enables the circuit designer to use the inductors for applications working at higher frequencies. Coils with different layouts and values for inductance (\( L \)) were verified and showed similar results.

1. Introduction

The increasing development of wireless communication products demands more and more high-performance on-chip inductors. In analog circuits still the coils restrict the electrical characteristics of the designs. Modern RF designs like filters, oscillators, transceivers, or amplifiers require high Q-factors at high frequencies. Additionally, the chip size is mainly determined by the extensive layout of the inductors, which raises the costs for production.

On-chip coils with high Q-factors and small geometries are required to establish a new generation of RF circuits. Generally the inductors performance is determined by its layout design and its physical characteristics regarding the loss mechanisms like resistive losses of the metal windings and substrate losses. First investigations to improve the Q-factor were focused on optimizing the layout, with satisfying results [1–3].

Metal losses can be reduced by using low resistive materials like copper or gold, instead of aluminum. The substrate losses, which are not trivial to characterize, have been well explored in the last years [4, 5].

The substrate losses are divided in two sections: losses caused by capacitive coupling between metal windings to substrate and eddy current effects in the substrate layer. Several methods have been reported about how these types of substrate losses can be reduced. The capacitive coupling can be decreased by the implementation of shielding layers [6] or providing thick oxide layers to decouple the inductor [7]. The eddy currents can be lowered by choosing an appropriate substrate resistivity [5] or by etching out the substrate below the spiral inductor [8].

Recent developments show new ways in designing three-dimensional micro machined on-chip inductors [9–12]. Those structures are considerably better decoupled due to their higher spacing to substrate.
This paper presents a new technological procedure for reducing substrate losses by improving the insulation to the inductor [13]. The oxide layers in the substructure are removed by an optimized etching technique. The resulting oxide capacitance is minimized and determined by the remaining permittivity which can be considered as $\varepsilon_r = 1$ for vacuum. The $Q$ factor is maximized, especially for higher frequencies. The experimental results are illustrated by comparing the electrical characteristics of these underetched coils with conventional processed on-chip inductors.

The reduction of capacitive losses into substrate is optimized by a new developed fabrication procedure. The front-end-of-line (FEOL) processing is identical for the new process. The conventional back-end-of-line (BEOL) processing was used initially without any change of process. All metallization layers are of aluminum. The final process step of the conventional technique is the structuring of the last thick metal 3. The following additional five process steps are necessary for the realization of the underetched inductor coils. In Table 1 the process flow is listed. The standard BEOL process is compared to the new additional process steps. It is documented that an additional lithography step with a 3 $\mu$m thick i-line resist was used as a protection mask for the CMOS and RF circuitry during the following etch steps.

The resist was exposed only at the inductor areas, where the oxide underetching should take place (Figure 2(a)). The following oxide etch procedure was divided into two etch steps. In the initial step, the oxide etching started with an anisotropic RIE (reactive ion etch) in a parallel-plate
Figure 2: (a) Schematic cross-section of inductor with supporting pillars in all metal layers, resist mask for oxide etching. (b) Schematic cross-section of inductor after 1st step oxide removal by anisotropic oxide etch. (c) Schematic cross-section of inductor after 2nd step oxide removal by isotropic oxide etch. (d) Layer thicknesses of oxide and metal.

electrode plasma reactor. Etch chemistry CHF₃/O₂ was used for the anisotropic etch. After removing around 2/3 of the total oxide intermetal dielectric (Figure 2(b)), in the second step the oxide was removed by a following isotropic etch. The isotropic etch was done in a downstream microwave plasma reactor. For the isotropic etch, fluorine chemistry (SF₆/O₂ or CF₄/O₂) was used (Figure 2(c)). The optimal ratio of the etching time between anisotropic and isotropic steps was found to be 2:1.

Finally, the thicknesses of the oxide and metal layers is documented in Figure 2(d). Metal 1 starts at 900 nm above substrate based on the oxide layer.

The determination of the oxide etching time for both etch steps could not be controlled by endpoint detection but only by time. To guarantee a reliable process, an accurate control of the etching rate on blanket test wafers, for both etch steps (anisotropic and isotropic), has to be done prior of each lot. Additionally, the etch rate depends on the open area of the chip layout. Open area is defined by the area which is not covered by resist and where the oxide etch will occur. Especially for different product layouts (different masks), which vary more than 5–10% open area in total per mask, the etch rate can differ dramatically and has to be controlled anyway for the first trial additional on product wafers. For the production, the adjustment of the mask-dependent etch rate can be easily controlled by determination of the oxide etch rate on blanked oxide deposited wafers, because the correlation of the blanket and the structured wafers fits very well and was reproducible for the investigated material in our study.
The etch process was optimized in such a way that the oxide underneath the upper inductor winding was totally removed and below the supporting pillars a remaining oxide was left to fulfill the adhesion contact to the substrate. The supporting metal-1 and metal-2 pillars were arranged underneath the upper inductor windings (Figure 3), connected with tungsten plug vias. The placement of the pillars was arranged in certain areas for mechanical stability reasons (see Figure 4).

Finally, after removal of the protection resist (Figure 5), the chip was protected by a conventional deposited passivation layer (SEM cross-section, Figure 6).

The next steps were concentrating on the improvement of the protection mask layout. Further layout optimization was necessary to reduce the proximity effects during the anisotropic etch. At a certain minimal distance of the windings (<1.0 μm) and at a minimal distance of the protection mask to the windings (<2.0 μm), the etch rate of the oxide was lower and led to insufficient oxide etch at these areas. In addition, if the size of the inductors becomes very small (outer diameter <200 μm), area etch effects become critical. These lead to etch rate reduction on the one hand and to a faster etch rate on the other hand. Both effects will cause an inhomogeneous oxide removal. Hence new definitions of specific layout rules for the protection mask were required. The minimal allowed distance between the windings was determined by ≥1.0 μm. To minimize the macroscopic etch effects, for small inductors the protection mask opening was designed larger and for huge inductors the protection mask was built with certain fillers to compensate the open area differences.

One of the most important topics for all mechanical uncoupled inductor constructions is their mechanical stability. In the present case, this critical behavior could be controlled very well by using supporting pillars designed in metal, via, and oxide layers. These pillars remain after the removal of the surrounding oxide and are physically (not electrically) connected to the silicon substrate, and hence they provide a statical stabilization. The implementation was easily established by optimizing the layout. Within our product qualification tests, we demonstrated that this method is very effective to show the influence of thermal-mechanical stress. Several samples were tested with 1 k temperature cycling steps from −50°C up to +125°C, without any electrical failure.

3. Electrical Characterisation

The inductor devices are embedded in a measurement teststructure as shown in Figure 1. Ground-signal-ground
pads are provided with a pitch of 100 μm. The ground pads are connected to substrate to ensure excellent RF ground for the total environment of the device under test. High frequency S-parameter (scattering parameter) measurements were performed up to 20 GHz using the Agilent network analyser (NWA) 8510C. For the calibration of the NWA system, the impedance standard substrate (ISS) of Cascade and Infinity probes was applied. All measurements were performed at an average ambient temperature of about 22°C. The S-parameters of the coils are two-step deembedded, using OPEN and THRU structures. Figure 1(b) shows the screenshot of an OPEN structure, corresponding to the inductor from Figure 1(a). This structure is taken for deembedding the pad and contact line capacitances. The related THRU structure is depicted in Figure 1(c). It is important to design the THRU with identical effective conductor line length as used in the OPEN and the device structure. Otherwise wrong values for series resistance and inductance are deembedded, which results in an overestimated Q-factor. The deembedding is performed by using admittance parameters (Y-parameters) for removing the pad capacitances represented by the OPEN. Second the series resistance and inductance of the measurement structure are subtracted by using the A-matrix (chain parameters) for the THRU. The THRU impedance is divided in two halves and removed from the inductor parameters by multiplying the inverse ABCD-matrix. In detail the parameters are deembedded using the following procedure [14, 15]:

\[
S_{\text{Coil}}S-\text{parameter of the measured inductor};
S_{\text{OPEN}}S-\text{parameter of the measured OPEN structure};
S_{\text{THRU}}S-\text{parameter of the measured THRU structure}.
\]

**Step 1 (OPEN Deembedding).**

\[
S_{\text{Coil}} \rightarrow Y_{\text{Coil}}
S_{\text{OPEN}} \rightarrow Y_{\text{OPEN}},
Y'_{\text{Coil}} = Y_{\text{Coil}} - Y_{\text{OPEN}}.
\]

**Step 2 (THRU Deembedding).**

\[
S_{\text{THRU}} \rightarrow Y_{\text{THRU}},
Y''_{\text{THRU}} = Y_{\text{THRU}} - Y_{\text{OPEN}},
Y''_{\text{THRU}} \rightarrow A''_{\text{THRU}},
A'12 = R_{\text{THRU}} + j\omega L_{\text{THRU}},
R_{\text{THRU}} \text{ series resistance of THRU structure},
L_{\text{THRU}} \text{ series inductance of THRU structure},
A'12 = A' 12/2,
A''_{\text{Coil}} = 1/(A'_{\text{THRU}}) \ast A''_{\text{Coil}} \ast 1/(A'_{\text{THRU}}).
\]

The Q-factor is the main parameter that is characterising the inductor performance over frequency. After transforming measured and deembedded S- to Y-parameters (admittance matrix) Q can be extracted directly with the following traditional approach that is only valid for frequencies below self-resonance [16]:

\[
Q = \frac{\text{IM}[Y_{11}]^{-1}}{\text{RE}[Y_{11}]^{-1}}. \tag{1}
\]

The series inductance is extracted as follows:

\[
L_s = \frac{\text{IM}[Y_{11}]^{-1}}{\omega} \bigg|_{f \rightarrow 0}. \tag{2}
\]

In Figure 7 measured results for the Q-factor versus frequency are plotted. We selected the 2.2 nH inductor device with 213 μm outer diameter displayed in Figure 1(a). The curves for the new developed under-etching process and the standard micromachined device are included for comparison. The standard coil is featured once with the supporting pillars, included. In addition to demonstrate the influence of the pillars measured data for the standard devices excluding the pillars are provided. Referring to Table 1 the standard and the new processed device are identical, considering the conductive layers. The inductor wires are realized only in top metal (metal-3); the crossing sections are defined in metal-2. In summary, the differences for the new underetched coil are the removed oxide layers and the supporting pillars.

For frequencies \( f < 1.5 \text{ GHz} \) the Q curves show no significant delta for the underetched coil. The reason for this unchanged behavior is that the capacitive power coupling to substrate is not dominant in this range and losses are mainly determined by the series resistance represented by the metallization. In this lower frequency range there is no benefit of an underetching process regarding Q.

The standard processed inductor without pillars features a \( Q_{\text{max}} = 10.5 \) at \( f = 3.0 \text{ GHz} \) whereas the standard inductor including the pillars shows its \( Q_{\text{max}} = 9.4 \) at \( f = 2.6 \text{ GHz} \). This discrepancy is caused by capacitive and inductive losses of the stacked pillar structure. These parasitic losses are kept.
small since the pillar geometry is small too and only few of them are required for stabilisation. The underetched device
gives at the same frequency a value of $Q = 12.5$ which is representing a relative improvement of almost 33%. For this
frequency region we already observe considerable lower substrate power losses caused by the significant smaller metal-to-
substrate capacitances. But the main parameters affected by the etching methodology are $Q_{\text{max}}$ and $f(Q_{\text{max}})$ which offer
the designers new prospects. The maximum quality factor for our underetched coil reaches outstanding $Q_{\text{max}} = 19.0$ at
a frequency $f(Q_{\text{max}}) = 6.5$ GHz. Since the standard device shows only a $Q = 3.8$ we can state an improvement of 500%
in the higher frequency region. Comparing specifically the $Q_{\text{max}}$ we see an improvement of about 100% for the under-
etched version. The significant shift to higher frequency is the consequence of lower capacitive coupling. Conventionally
the coils are applied in the frequency range $f < f(Q_{\text{max}})$. This means with respect to the new approach that the
inductors are covering a wider range for applications since $f(Q_{\text{max}})$ is raised up to 250%.

Similar results were reported in [17, 18], but a direct comparison of the process concept and the different approaches is not meaningful. For instance, copper met-
allization is applied instead of aluminum, and substrate is removed by etching. In this current work, we present a concept for realization of high $Q$-factors using standard alu-
minum metallization and conventional technology, without changing metallization material or Si substrate removing.

The comparison of the series inductance between under-etched and standard processed devices is depicted in Figure 8(a). Additionally Figure 8(b) gives information of the THRU series resistance used for deembedding. The resistance is displayed versus frequency and is very low. At frequencies close to DC we get $R_s = 168$ m$\Omega$. The series inductance of the THRU structure is plotted in Figure 8(c). An inductance of $L_s = 138$ pH at low frequencies can be observed. An overestimation of $Q$ can be excluded using this low-impedance THRU structures.

With formula (2) $L_s$ is extracted at lower frequencies:

$$L_s (\text{Standard}) = 2.22 \text{ nH},$$
$$L_s (\text{Under-etched}) = 2.17 \text{ nH}.$$  

The inductor value is determined by its geometrical layout. In our benchmark the $L_s$ is hardly changing which proves that the coils geometry is identical. The slight difference of $-2.25\%$ can be assumed as measurement tolerance.

The device geometries and measurement results for a selection of three typical inductors are listed in Table 2. The following are abbreviations:

$L_o$: Outer diameter of coil structure

$n$: Number of windings

$w$: Track width of inductor winding

$s$: Spacing or gap between the wiring

$L_i$: Inner diameter of coil structure

$Q$: Measured quality factor

![Figure 8: (a) Series inductance of benchmark, standard, and under-etching processed for typical inductor with outer diameter 213 $\mu$m, inductance $L = 2.2$ nH. (b) Series resistance of THRU deembedding structure versus frequency; $R_s = 168$ m$\Omega$ extracted at very low frequency (200 MHz). (c) Series inductance of THRU deembedding structure versus frequency; $L_s = 138$ pH extracted at very low frequency (200 MHz).]
Table 2: Measurement results for inductors of three different sizes, benchmarking the under-etching effect and the losses considering the standard devices with and without pillars provided.

| No. | Name                | Geometry | Electrical Results |
|-----|---------------------|----------|-------------------|
|     |                     | $L_o$ ($\mu m$) | $n$ | $w$ ($\mu m$) | $s$ ($\mu m$) | $Q_{\text{max}}$ | $f_{\text{res}}$ (GHz) |
| 1   | 1.5 nH underetched  | 213 3    | 18 2.4 95 14.9 5.2 1.51 1.08  >20 |
| 1   | 1.5 nH standard no pillar | 213 3    | 18 2.4 95 10.3 2.9 1.49 1.03 >20 |
| 1   | 1.5 nH standard inc. pillar | 213 3    | 18 2.4 95 9.4 2.6 1.53 1.01 >20 |
| 2   | 2.2 nH underetched  | 213 3    | 11 2.4 137 19.0 6.5 2.17 1.88 >20 |
| 2   | 2.2 nH standard no pillar | 213 3    | 11 2.4 137 10.5 3.0 2.18 1.85 >20 |
| 2   | 2.2 nH standard inc. pillar | 213 3    | 11 2.4 137 9.4 2.5 2.22 1.83 >20 |
| 3   | 6.8 nH underetched  | 213 6    | 7 2.4 105 13.0 3.5 6.74 5.64 9.3 |
| 3   | 6.8 nH standard no pillar | 213 6    | 7 2.4 105 8.2 2.2 6.71 5.59 7.9 |
| 3   | 6.8 nH standard inc. pillar | 213 6    | 7 2.4 105 7.8 1.7 6.83 5.52 7.4 |

Figure 9: Comparison of $Q_{\text{max}}$ for standard and under-etched processed coils.

- **Underetched**
- **Standard**

$Q_{\text{max}}$: Measured maximum quality factor  
$L_s$: Measured series inductance  
$R_s$: Measured series resistance  
$f_{\text{res}}$: Measured self-resonance frequency.

The quality factor improvement is obvious for all inductor designs. The series inductance $L_s$ and the series resistance $R_s$ were extracted at very low frequencies (<200 MHz). The low variations of these parameters for under-etched and standard coils prove that only capacitances are affected by our methodology. The variations are in the range of a few percent which is related to the measurement accuracy and the resolution of the RF equipment and definitely not provoked by the under-etching.

In Figure 9 the conventional and new processed inductors are compared, considering their maximum quality factor.

Finally, an evaluation of the influence on the resonance frequency ($f_{\text{res}}$) must be discussed. The self-resonance is determined as frequency where $Q$ becomes zero. Generally we observed for all designs a significant increment for $f_{\text{res}}$. For example, the 6.8 nH coil shows a shift of resonance frequency from 7.4 to 9.3 GHz. Most of our other designs cannot be evaluated because self-resonance is beyond the maximum measured frequency of 20 GHz. The frequency shift for $Q_{\text{max}}$ and $f_{\text{res}}$ can be explained with the common inductor subcircuit depicted in Figure 10.

The element $C_f$ represents the fringe capacitance of the metal windings. Combined with the series inductance $L_s$ and the series resistance $R_s$ a resonator is given.

New inductor designs with this under-etching procedure can be used for new applications.

(i) Smaller geometries provide high $Q$-factors compared to larger coils in the conventional process.  
(ii) Very high $Q$-factors can be reached with a range that standard processed inductors cannot offer.  
(iii) Shift of $f(Q_{\text{max}})$ to higher frequencies allows wider range of applications.  
(iv) Inductors with very wide metal windings show an enhanced frequency behaviour. Generally wide metallisation layers cause higher capacitive losses into substrate.  
(v) Higher self-resonance allows better tuning opportunities in oscillator designs.
The new methodology of removing oxide layers in the substructure of on-chip inductors is a process measure for optimizing Q-factors and the RF performance. In addition, the here-presented methodology shows further advantages concerning mechanical stability. The coils are physically placed on supporting pillars. After this, a passivation layer stabilizes the construction. Mechanical instability would show massive effects on the measurements; a reproducibility of electrical verification would not be possible. The etching procedure is only removing the oxide layers below the structures. This method, in combination with the mechanical stability, establishes accurate measurements and provides a predictable performance of the electrical characteristics, which is the main advantage of our process. These circumstances are strongly required to assign product qualification status. In addition, we do not have to fear impacts caused by packaging process like change in electrical performance or demolition of our sophisticated structure.

4. Conclusion

A new methodology for processing on-chip inductors with high-performance RF characteristics was presented. The optimized process for under-etching coils is discussed in detail, showing the new micromachined devices and pointing out the special supporting pillars used for mechanical stabilization of the devices. Only five additional process steps are necessary for this new methodology, compared to a conventional process. Based on the electrical characterization the loss mechanism is documented. The oxide layers in the inductors substructure are clearly contributing to the capacitive substrate losses. The analysis of the Q factor and the benchmark of the standard and under-etched chip coils shows outranging results for Q, that is almost rising 500% measured at the same frequency. The improvement in $Q_{\text{max}}$ is evident where $Q = 19.0$ (@ $f = 6.5$ GHz) was achieved for the new process compared to $Q = 9.4$ (@ $f = 2.5$ GHz) for the standard coils. The significant frequency shift of $Q_{\text{max}}$ to higher ranges offers a new and wider field of application. Smaller and cost saving inductor designs can be realized without loosing performance. This process technology is widely applicable for a variety of chip products such as VCOs, RF power amplifier, RF filters, and RF matching networks. Finally, the new methodology highlights also its excellent mechanical stability, which is generally a critical issue for under-etched constructions.

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