Temperature Dependence of Reverse Annealing in Bulk Damaged Silicon

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Abstract

A recent proposal [1] has suggested a model for the operation of silicon detectors which should give rise to the suppression of reverse annealing after neutron irradiation. The results of an experiment to investigate that model, in which the silicon is cooled during irradiations and annealed at high temperature between irradiations, are presented.
1 Introduction

The unprecedented levels of radiation expected at the Large Hadron Collider (LHC) will provide a challenging environment for the operation of silicon detectors. Studies of the effects of bulk damage in high-resistivity silicon incurred by neutron irradiations comparable to those expected during the lifetime of the LHC have been performed independently by several experiments [2]. Increased leakage currents and decreased charge collection efficiency are observed due to the creation by lattice defects of additional energy levels in the silicon band gap. The other significant effect is the removal of donor states and creation of acceptor states within the silicon bulk, eventually leading to a conversion of the bulk from n-type to p-type. Of primary concern is the mechanism of reverse annealing of the effective doping concentration, $N_{\text{eff}}$. Once conversion from n-type to p-type has occurred, the number of acceptor states, and therefore $N_{\text{eff}}$, continues to increase even after the irradiation has ceased. The voltage required to maintain full depletion of the detector therefore increases, possibly to a level sufficient to initiate breakdown within the detector. Suppression of the reverse annealing of $N_{\text{eff}}$ would therefore significantly enhance the survivability of silicon detectors at the LHC.

2 A Model for Reverse Annealing of $N_{\text{eff}}$

Recent studies [3] have suggested the dependence of $N_{\text{eff}}$ on neutron fluence, $\phi$, follows:

$$N_{\text{eff}} = N_{D0}e^{-c\phi} - N_{A0} - b\phi$$

where $N_{D0}$ and $N_{A0}$ are the initial concentrations of donor and acceptor states respectively. The parameter $c$ characterises the rate of donor removal, and $b$ characterises the creation of radiation induced acceptor states. The parameter $b$ can be further expressed as

$$b = b_s + b_n R(t, T)$$

where $b_s$ refers to the number of stable acceptor states produced, and $b_n$ refers to the number of initially neutral defects that subsequently produce acceptor states through reverse annealing. In this simple model, the dependence of $N_{\text{eff}}$ on time after irradiation ($t$) and temperature ($T$) is due to the function $R$ only, where $R = 0$ at $t = 0$, rising to $R \sim 1$ when $t$ is very large. $R$ has been shown experimentally to have a strong dependence on temperature. Significant reverse annealing is observed at room temperature, even after several months of anneal time. Reverse annealing appears to be suppressed at low temperatures ($\sim 0^\circ C$), but resumes quickly should the temperature increase.

A model [1] for the operation of silicon detectors has recently been proposed which would suppress reverse annealing without the requirement to maintain the detectors at low temperatures throughout the lifetime of the LHC. The model requires the silicon detectors to be operated at high temperatures; defects generated by bulk damage then diffuse to the surface, where they are expected to lose their properties. However, high leakage currents would make this method of operation impractical. A best compromise is to run the silicon detectors at low temperature during LHC operation, and perform a high temperature anneal during breaks in the LHC schedule. This cycle of operation would require small integrated doses ($\sim 2 \times 10^{12}$ neutrons cm$^{-2}$) between subsequent high temperature anneals, in order to limit the number of defects and ensure their diffusion to the surface.
3 Experimental Procedure

In this study, ten silicon diodes (see Table 1) were irradiated unbiased every 48 hours at the ISIS neutron spallation source. Each irradiation, of duration $\sim$40 minutes, corresponded to a fluence$^1$ of $\sim 4 \times 10^{12}$n.cm$^{-2}$. There were a total of seven irradiations, corresponding to an integrated fluence received by each diode of $2.8 \times 10^{13}$n.cm$^{-2}$. All diodes were cooled to 7°C prior to each irradiation. Between irradiations, half of the diodes were stored at 7°C, and half were stored at 98°C (hereafter referred to as cooled diodes and heated diodes respectively). After the final irradiation cycle, all diodes were baked at 80°C for a few days in order to promote any further reverse annealing.

The depletion voltage and leakage current for every diode were determined at key stages throughout the experiment, using a Keithly 487 Picoammeter/Volt Source and Hewlett-Packard 4285A and Wayne Kerr 6425B LCR meters to measure the CV and IV characteristics. Capacitance values were measured at 75kHz and 300kHz, and depletion voltages were extracted by straight line extrapolations on the logC-logV curves. After each irradiation, the cooled diodes were measured immediately, whereas the heated diodes were measured after 44 hours at high temperature. During the 80°C bake, all diodes were remeasured after three hours, three days and six days. Diodes were measured within 3 hours of their removal from the oven. Further measurements were taken while the diodes were stored at room temperature after the end of the 80°C bake.

4 Results

The variation of depletion voltage with fluence for the heated and cooled diodes is listed in Tables 2 and 3 respectively. Both heated and cooled diodes clearly exhibit inversion; heated diodes show accelerated reverse annealing with respect to the cooled diodes. Figures 1 and 2 show the variation of $N_{\text{eff}}$ with fluence for 300$\mu$m and 200$\mu$m thick diodes respectively. Fits to the data using the above expression for $N_{\text{eff}}$ are superimposed on the figures; parameter values yielded by the fits are listed in Table 4.

Tables 5 and 6 list the variation of depletion voltage for heated and cooled diodes respectively during baking at 80°C and during subsequent storage at room temperature. The corresponding variation in $N_{\text{eff}}$ with time for the 300$\mu$m and 200$\mu$m thick diodes is shown in Figures 3 and 4 respectively.

During the 80°C bake, diodes that had been heated between irradiations showed no significant variation in $N_{\text{eff}}$, suggesting that the inter-irradiation heating at 98°C was sufficient for $N_{\text{eff}}$ to reach saturation. However reverse annealing was observed for the cooled diodes, with $N_{\text{eff}}$ close to saturation after 135 hours. Final averaged values for $N_{\text{eff}}$, measured at room temperature one day after the end of the 80°C bake, were $1.3 \pm 0.1 \times 10^{12}$cm$^{-3}$ ($1.2 \pm 0.1 \times 10^{13}$cm$^{-3}$) for the 300$\mu$m heated (cooled) diodes, and $1.3 \pm 0.1 \times 10^{12}$cm$^{-3}$ ($1.0 \pm 0.1 \times 10^{13}$cm$^{-3}$) for the 200$\mu$m heated (cooled) diodes.

After the 80°C bake, it was noted that $N_{\text{eff}}$ had developed a strong dependence on temperature. Between 80°C and 20°C, the reduction in $N_{\text{eff}}$ was $\sim 24$% for the 300$\mu$m heated diodes, $\sim 13$% for the 300$\mu$m cooled diodes, $\sim 15$% for the 200$\mu$m heated diodes, and negligible for the 200$\mu$m cooled diodes. $N_{\text{eff}}$ increased immediately with increasing temperature, but took about 0.5 days to decrease after the temperature was lowered.

Leakage current was monitored at all stages following the second neutron dose. Current was measured through the p-side of the diode, with the p-side guard ring held at the same potential. For

$^1$All fluences quoted are for 1 MeV-equivalent neutron irradiations [4].
the cooled samples, at all stages of the irradiation cycle the current-voltage characteristic reached a plateau at depletion corresponding to a damage constant of \( \sim 6 \times 10^{-17} \text{ A cm}^{-1} \), in reasonable agreement (allowing for annealing) with previous measurements. During the subsequent reverse annealing at 80°C the characteristic became peaked close to the depletion voltage, exhibiting a sharp fall in diode current, accompanied by a similar increase in guard current. This behaviour was present at all stages in the baked samples, and appears to depend strongly on the diode geometry and proximity to the edge of the wafer. Although a plateau was still exhibited when probing the n-side we do not have a sufficient understanding of this behaviour to draw quantitative conclusions for the leakage current following high temperature treatment.

5 Conclusions

All diodes irradiated with neutrons in this experiment exhibited both inversion of the silicon from n-type to p-type, and reverse annealing. The evolution of effective doping concentration with fluence was described by \( N_{\text{eff}} = N_{D0} e^{-c\phi} - N_{A0} - b\phi \). Reverse annealing was accelerated for diodes stored at 98°C between irradiations, compared to those stored at 7°C; the difference was quantified by parameter \( b \). The measured initial doping concentrations, \( N_{D0} \) and \( N_{A0} \), were consistent with expectations, and with the fact that the 300µm and 200µm diodes were processed from different starting material. The rate of donor removal, characterised by parameter \( c \), was consistent with previous measurements at ISIS [4].

Diodes that had been irradiated and baked at high temperature were observed to develop a strong dependence of \( N_{\text{eff}} \) on temperature, in agreement with other recent studies [5]. This suggests that a significant fraction of the radiation-induced acceptor states generated by reverse annealing at high temperature are not electrically active at room temperature. As a consequence of this effect, the value of parameter \( b \) (which describes the rate of radiation-induced acceptor state creation) listed in Table 4 for the diodes heated between irradiations may include a contribution from defects which are electrically inactive at room temperature.

A model [1] had predicted that the diffusion of radiation induced defects to the surface during high temperature annealing between irradiations may suppress reverse annealing. A re-evaluation [6] of the model predictions according to the conditions of this experiment provisionally suggest a significant suppression of \( N_{\text{eff}} \). However no such effect was observed in this experiment.

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[5] Observation of a Bistable Defect Generated and Activated by Heat Treatments in Irradiated High Resistivity Silicon, M. Moll et al., Submitted to International Conference on Advanced Technology and Particle Physics, Como, 3-7 October 1994.

[6] G. Lutz, private communication.
Table 1: Diodes used in this Experiment. All were manufactured by Micron Semiconductors Ltd, and supplied on ~2cm×7cm wafer fragments. RD20 diodes were from a double-sided wafer. All diodes had a p-side guard ring, and four of the RD20 diodes also had a guard ring on the n-side.

| Diode | Size (mm) | Thickness (µm) | Design | Use in this Experiment |
|-------|-----------|----------------|--------|------------------------|
| A1    | 7×7       | 203            | OPAL   | Cooled                 |
| B1    | 7×7       | 203            | OPAL   | Heated                 |
| C1    | 5×5       | 311            | RD20   | Control diode          |
| C2    | 5×5       | 311            | RD20   | Heated                 |
| C3    | 5×5       | 311            | RD20   | Cooled                 |
| C4    | 5×5       | 311            | RD20   | Cooled                 |
| D1    | 5×5       | 311            | RD20   | Heated                 |
| D2    | 5×5       | 311            | RD20   | Cooled                 |
| E1    | 5×5       | 302            | RD20   | Heated                 |
| E2    | 5×5       | 302            | RD20   | Heated                 |
| E3    | 5×5       | 302            | RD20   | Cooled                 |

Table 2: Variation of Depletion Voltage with Fluence for Heated Diodes. Note diode C1 was not irradiated, but used as a control sample to monitor any variation with temperature alone. Uncertainties are ±0.5V, ±1V and ±4V for depletion voltages up to 5V, up to 30V and above 30V respectively.

| Fluence (×10¹²n.cm⁻²) | Depletion Voltage (Volts) |
|------------------------|----------------------------|
|                        | C1     | C2     | D1     | E1     | E2     | E3     |
| 0                      | 17.5   | 17.0   | 16.3   | 20.6   | 19.2   | 19.6   |
| 3.3                    | 18.0   | 4.2    | 4.0    | 4.0    | 4.2    | 11.8   |
| 7.4                    | 18.5   | 21.5   | 20.5   | 15.0   | 18.5   | 4.5    |
| 11.6                   | -      | -      | -      | -      | -      | -      |
| 15.6                   | 18.3   | 77     | 79     | 62     | 65     | 22     |
| 20.1                   | 17.5   | 90     | 89     | 80     | 81     | 32     |
| 24.0                   | 17.9   | 125    | 114    | 104    | 108    | 42     |
| 28.7                   | 17.8   | 120    | 119    | 110    | 118    | 55     |

Table 3: Variation of Depletion Voltage with Fluence for Cooled Diodes. Uncertainties are ±0.5V, ±1V and ±4V for depletion voltages up to 5V, up to 30V and above 30V respectively.

| Fluence (×10¹²n.cm⁻²) | Depletion Voltage (Volts) |
|------------------------|----------------------------|
|                        | E3     | D2     | C3     | C4     | A1     |
| 0                      | 20.0   | 17.2   | 16.1   | 16.5   | 22.9   |
| 3.3                    | 8.5    | 7.0    | 6.0    | 6.0    | 17.0   |
| 7.4                    | 3.0    | 2.0    | 3.0    | 3.0    | 6.5    |
| 11.6                   | 7.0    | 6.0    | 8.0    | 7.0    | 5.6    |
| 15.6                   | 10.0   | 8.0    | 11.0   | 13.0   | 2.8    |
| 20.1                   | 16     | 14     | 16     | 20     | 4.2    |
| 24.0                   | 21     | 20     | 22     | 22     | 5.0    |
| 28.7                   | 26     | 32     | 26     | 28     | 7.0    |
Table 4: Results of fits to Data using \( N_{\text{eff}} = N_D e^{-c\phi} - N_A - b\phi \)

| Diode        | \( c \times 10^{-14}\text{cm}^2 \) | \( b \times 10^{-2}\text{cm}^{-1} \) | \( N_A \times 10^{13}\text{cm}^{-3} \) |
|--------------|-------------------------------------|--------------------------------------|--------------------------------------|
| 300\(\mu\)m Heated | 5.8\pm0.6                           | 5.6\pm0.1                           | 1.6\pm0.3                           |
| 300\(\mu\)m Cooled | 7.0\pm0.3                           | 0.81\pm0.04                         | 1.7\pm0.1                           |
| 200\(\mu\)m Heated | 5.6\pm0.4                           | 5.2\pm0.2                           | 2.0\pm0.4                           |
| 200\(\mu\)m Cooled | 7.8\pm0.3                           | 0.51\pm0.06                         | 2.1\pm0.2                           |

Table 5: Annealing of Heated Diodes after last Irradiation. All diodes had been stored at 98°C between irradiations. Note diode C1 was not previously irradiated, but used as a control sample to monitor any variation with temperature alone. Diode C2 was not annealed at high temperature, but stored throughout at 7°C for comparison.

| Anneal Condition | Depletion Voltage (Volts) |
|------------------|---------------------------|
|                  | C1 | C2 | D1 | E1 | E2 | B1 |
| Store at 7°C     | 18 | 125| 126| 124| 110| 42 |
| After 1 day      |    |    |    |    |    |    |
| Bake at 80°C     | 18 | 120| 131| 127| 118| 53 |
| After 3 hrs      |    |    |    |    |    |    |
| After 69 hrs     | 18 | 90 | 122| 127| 119| 48 |
| After 135 hrs    | 18 | -  | 133| 125| 118| 48 |
| Store at 20°C    | 18 | -  | 100| 99 | 88 | 41 |
| After 1 day      |    |    |    |    |    |    |
| After 4 days     | 18 | -  | 98 | 98 | 93 | 46 |
| After 54 days    | 18 | 92 | 92 | 88 | 83 | 38 |

Table 6: Annealing of Cooled Diodes after last Irradiation. All diodes had been stored at 7°C between irradiations. Note diode E3 was not annealed at high temperature, but stored throughout at 7°C for comparison.

| Anneal Condition | Depletion Voltage (Volts) |
|------------------|---------------------------|
|                  | E3 | D2 | C3 | C4 | A1 |
| Store at 7°C     | 21 | 22 | 25 | 26 | 4.4 |
| After 3 days     |    |    |    |    |    |
| Bake at 80°C     | 16 | 53 | 61 | 57 | 15 |
| After 3 hrs      |    |    |    |    |    |
| After 69 hrs     | -  | 87 | 96 | 99 | 31 |
| After 135 hrs    | -  | 94 | 97 | 102| 33 |
| Store at 20°C    | -  | 82 | 84 | 88 | 32 |
| After 1 day      |    |    |    |    |    |
| After 3 days     | -  | 87 | 92 | 92 | 33 |
| After 54 days    | 17 | 76 | 81 | 83 | 30 |
Fig. 1: Effective Doping Concentration versus fluence for 300 μm thick diodes.

Fig. 2: Effective Doping Concentration versus fluence for 200 μm thick diodes.

Fig. 3: Annealing of $N_{\text{eff}}$ after last irradiation for 300 μm thick diodes.

Fig. 4: Annealing of $N_{\text{eff}}$ after last irradiation for 200 μm thick diodes.