Automated Generation of High-Performance Computational Fluid Dynamics Codes

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Abstract

Domain-Specific Languages (DSLs) improve programmers productivity by decoupling problem descriptions from algorithmic implementations. However, DSLs for High-Performance Computing (HPC) have two critical non-functional requirements: performance and scalability. This paper presents the automated process of generating, from abstract mathematical specifications of Computational Fluid Dynamics (CFD) problems, optimised parallel codes that perform and scale as manually optimised ones. We consciously combine within Saiph, a DSL for solving CFD problems, low-level optimisations and parallelisation strategies, enabling high-performance single-core executions which effectively scale to multi-core and distributed environments. Our results demonstrate how high-level DSLs can offer competitive performance by transparently leveraging state-of-the-art HPC techniques.

Keywords: Domain-Specific Languages, High-Performance Computing, Computational Fluid Dynamics, Code Optimisation

1. Introduction

Scientific applications face the challenge of efficiently exploiting increasingly complex parallel and distributed systems. Extracting high performance requires deep expertise in parallel programming models, libraries and algorithms, and in-depth knowledge of the target architecture. Hand-tuned codes are built under this assumed knowledge, and therefore, able to provide both low-level optimised and efficient parallel implementations. Data structures, optimisations and parallelisation strategies are intertwined with the application code and exposed to the compilers. Nevertheless, developing such codes is a time-consuming, tedious and hardly reusable task. In this scenario, reaching high performance appears
detrimental to productivity and portability and unreasonable to expect from scientists. Domain-Specific Languages (DSLs) have arisen as a separation of concerns approach through high-level abstraction layers to overcome such difficulties. On the one hand, productivity and portability can be reached by abstracting the application layer from the final parallel low-level code. On the other hand, since DSLs are restricted to specific problem domains, performance can be tackled at the set of algorithmic patterns they implement. However, this dissociation might blind the compilers and prevent using state-of-the-art HPC techniques such as vectorisation and tiling or advanced parallelisation strategies. Thus, pressure has moved to DSLs researchers expecting from their framework a high level of generality and abstraction while delivering high-performance on par with hand-tuned codes.

The aim of this paper is to enhance a DSL framework to automatically generate code optimised to exploit an HPC cluster from high-level specifications. We focus on the Computational Fluid Dynamics domain and use Saiph as DSL platform. Saiph targets the resolution of CFD problems through a high-level syntax and a generic numerical library implementing explicit and Finite Differences Methods (FDM). We profit from the layered design and adapt the build process for a new code generation, ensuring the extraction and propagation of information from the input code to the final binary. From Saiph applications, we automate the combination of state-of-the-art and advanced HPC techniques by generating an intermediate annotated code exposing detailed information to the compiler. For that, we study such techniques and determine (i) the information needed at the intermediate code to enable it, (ii) how to extract and generate such information from a high-level specification and (iii) how to combine it with the rest of the techniques.

In particular, the combination of HPC techniques is a non-trivial task. Simultaneously vectorising, blocking, parallelising and distributing a loop requires a harmonious combination ensuring aligned data access, good cache locality and well-balanced domain partition at the same time. Our approach ensures the automated, generic and effective combination of such techniques by coupling the efficient exploitation of three levels of HPC resources: intra-core (single-core), inter-core (multi-core) and inter-node (cluster), in a bottom-up manner:

**Intra-core performance** We target single-core performance by exploiting parallelism and memory hierarchy through code-vectorisation and cache locality enhancement using data-blocking mechanisms. To that end, we explore suitable data layout, traversal and alignment, compiler hints and compile-time evaluations.

**Inter-core performance** We inquire how to adapt the data-blocking for subsequent appropriate shared-memory usage at the node level when exploiting inter-core resources. We target different shared-memory models such as fork-join and tasking through OpenMP, and OmpSs-2 programming models. Hence, we address inter-core parallelism for load imbalance or data locality improvements. To the best of our knowledge, this work
presents an unprecedented approach for the automatic generation of taskified codes within a DSL framework.

**Inter-node performance** On top of it, we research how to extend distributed executions based on MPI and scalable domain decomposition to preserve the underlying optimisations. Moreover, combining inter-node strategies with different inter-core parallel version produce hybrid configurations with different interoperability characteristics. We study such hybrid configurations using MPI and TAMPI [4] combined with fork-join and task models.

The paper makes the following contributions:

1. A DSL build process and code generation ensuring automated code annotations and optimisations.
2. An effective automated combination of state-of-the-art HPC techniques and parallelisation strategies at single/multi-core and cluster levels.

2. **Background**

2.1. **Computational Fluid Dynamics**

CFD is a physics domain to solve problems related to fluid flows numerically. The governing equations modelling density-based CFD problems are the Navier-Stokes equations and the equation of state. The former is a set of space-time dependent Partial Differential Equations (PDEs) describing the motion of a fluid; the latter corresponds to a non-time derivative equation relating the fluid’s state variables. Depending on the equations’ unknowns, we incorporate other thermodynamic relations between state variables to close the system. To unambiguously define a CFD problem, we state the equations’ system, the space-time modelling scope and the initial and boundary fluid conditions (ICs, BCs). We use space-time discretisation methods for CFD system resolution.

2.1.1. **Explicit and Finite Difference Method (FDM)**

Explicit FDM defines a closed set of computation patterns involving finite difference discretisations and explicit time solvers to solve a wide range of CFD problems. FDM discretises a spatial domain mapping continuous field information into a Cartesian grid of points; points store field values according to spatial coordinates. Explicit methods discretise the temporal dimension through a time-stepping loop at which each iteration defines the state of a system using previous time-step states. In such methods, PDEs are approximated by algebraic equations at each spatial coordinate at each time-step. Computationally, a time-step loop encloses a spatial traversal at which linear algebra and stencil computations occur.

2.1.2. **Challenges of HPC explicit FDM**

Explicit FDM can benefit from different levels of optimisations to fully exploit HPC systems.
Intra-core level. Algebraic operations and stencils calculations can benefit from basic compiler optimisations and code-vectorisation if the compiler has enough information and the data structures are adequately aligned and traversed. Moreover, stencil calculations access neighbouring mesh point values from previous time-iterations, so data-blocking mechanisms enabling data reuse can improve data locality at the memory hierarchy.

Inter-core level. Within explicit FDM time-steps, new values are computed from previous time iterations ones. Hence, at each time step, the absence of data dependencies ensures the spatial loop’s embarrassingly parallelism. Such patterns can benefit from shared-memory parallelism through parallel programming model annotations. Explicit FDM codes must ensure balanced work partition and minimum synchronisation overheads. Moreover, the neighbouring data dependencies across time-steps restrict the time loop parallelism, but the end of each time step is not globally synchronised; distant spatial regions can profit from asynchronous parallel time progress.

Inter-node level. The computation domain decomposition approach within explicit FDM corresponds to a spatial domain distribution across available nodes. Thus, each node is in charge of a portion of the initial domain, and data redundancy and message passing mechanism manage dependencies. Such distribution must be scalable and preserve and combine with lower-level optimisations.

In this paper, we consider all previous points together and detail their application and combination.

2.2. Saiph

Saiph is a DSL easing the simulation of physical phenomena from the CFD domain in HPC environments. Users specify CFD problems through high-level constructs defining systems of PDEs with time-space configurations. Mathematical specifications, Saiph codes, evaluations and output results can be accessed online \cite{5}.

The DSL is embedded in Scala \cite{6} and comprises two main divisions: the Scala and the C++ layer. The Scala layer defines the language syntax; the C++ layer implements numerical methods and parallelisation strategies on separated libraries forming the modules. Figure\cite{4} illustrates the macroscopic compilation flow. Input code is first compiled to be parsed by the Scala layer producing a C++ intermediate code. The C++ code is then linked to the C++ library, and a second compilation produces the final parallel binary. Because of this dissociation, discretisation methods and algebraic kernels are generic enough to support any input problem configuration. Moreover, at the first compilation step, selecting a module determines the intermediate C++ generated code with function calls to the matching library.

At the Saiph intermediate output, PDEs are represented by equation trees modelled as abstract graphs. Vertices correspond to mathematical operators that relate the fluid fields designated by leaves. At run-time, the numerical library traverses these graphs for each spatial coordinate at each time-step,
applying basic parallelisation strategies. However, single-core performance is far from optimal because graph data structures blind the compiler preventing optimisations. This design offers high productivity and extensibility but limits Saiph from being a competitive HPC tool. In this paper, we enhance Saiph to leverage the specific domain knowledge and propagate it through the different compilation phases to achieve competitive and scalable performance. We focus on generating a specific, detailed and optimisable spatial loop from the Scala layer for any input application within the explicit FDM modules. Moreover, we implement advanced parallelisation strategies at the underlying C++ libraries, embracing and boosting the spatial loop execution, where computations and memory accesses happen iteratively.

3. New Design and implementation

We present a new design to extract and propagate information from the high-level code to the underlying layers. Based on this information, we develop, adopt and combine different numerical parallel strategies. As stated in the previous section, 2.1.1, the FDM-CFD algorithmic patterns occur within the spatial loop, at the mesh traversal. To get a significant benefit in performance, we focus on optimising such a loop.

3.1. Code generation

We present a generic build process ensuring productivity while enabling high-performance. For an efficient equation resolution, we remove the spatial loop construct from the C++ library to generate it from the Scala layer encapsulating the generated code in a lambda function. Figure 2 shows how we generate a C++ lambda function from a high-level specification of a PDE. From the input

Figure 1: Saiph layered abstraction
heat equation code, we traverse the equation tree at the Scala layer and generate, at the loop body, the corresponding method call for each vertex. Computations and memory allocations and accesses remain at the C++ library, guaranteeing their unique, efficient implementation.

To minimise mesh traversals, we group the resolution of the equations into the same spatial loop. Still, the equation time update depends on the equation nature. We generate two independent lambda functions grouping the spatial resolution of time-derivative and non-time derivative equations, respectively. For each loop body, we enable common subexpression elimination (CSE) at the Scala layer through the Lightweight Modular Staging (LMS) [7], allowing partial results to be reused even for different equations. Figure 3 exemplifies this reuse for two equations grouped into the same lambda; tmp4 corresponds to the partial result of the common highlighted subexpression so its result is used at both equation updates.

Figure 4 illustrates the overall execution workflow. Once the Scala layer outputs the C++ generated code from the input one, we use the lambdas as arguments of new setters methods from the C++ library, stating the resolution function attributes. Once these attributes are defined, we call them from the library within the integration methods’ time loop. The lambdas executed at each time-step act as links between layers: from the generated code scope their capture the references of the fluid fields defined at the input code and call the C++ library methods that state the calculations over them.

Once we automatically generate specific spatial loops, we further investigate how to detail and annotate them to obtain the desired optimisation level.

3.2. Exploiting low-level optimisations
3.2.1. Code efficiency

To benefit from compiler optimisations, we want detailed programs using simple structures and constant parameters. The extraction of semantic information from the input code enables compile-time evaluations leading to an
equivalent, more efficient program. Linear algebra and stencil computations can enormously benefit from such transformations. Within the spatial loop, Saiph equation resolution happens through function calls. At the C++ layer, those functions perform algebraic operations, stencil computations and integration updates. We implement them to encapsulate memory accesses and basic mathematical operations coded through simple structures involving conditional branches and few-iterations loops over problem variables. Moreover, we define them as **static inline functions**, so these small, recurrent-used kernels avoid being called and escape the associated overhead. We also generate the clause `#pragma forceinline recursive` right before the spatial loop, at the `lambda` function, to ensure the inline. Consequently, we enable context-specific optimisations on the body of the inline functions. By defining control variables such as mesh dimensions, operands dimensions and stencil neighbouring as literals, `const`, or `constexpr`, we expose them, and compile-time evaluation automatically applies. Listing 1 shows how accessing a field at a spatial position, `idx`, involves a loop that can be unrolled if the operand’s dimensions are known at compile-time. Similarly, spatial derivative kernels iterate over mesh
dimensions and stencil accuracy control variables.

```
static inline real_t* var(real_t* varBuff, int idx, int varDims, real_t* res) {
    for(int i = 0; i < varDims; ++i)
        res[i] = varBuff[idx*varDims + i];
    return res;
}
```

Listing 1: C++ variable access kernel

To benefit from these optimisations, we want the Scala layer to generate an intermediate code with information over the control variables. Mesh dimensions, fields dimensions and stencil accuracy are generated as literals by retrieving user code’s information. For other kernels’ control variables, we extract the information when traversing the equation tree. At the bottom-up graph traversal, we calculate specific semantic information for each vertex from leaves’ known dimensions, depending on the operator nature and its children’s dimensions.
We enhance the Scala layer to characterise graphs and generate kernel calls with evaluable control variables. Figure 5 shows the tree characterisation of the heat equation and the specific generated var call for accessing a scalar problem field. Before the operator call, we generate the operand dimensions’ evaluation and allocate the temporal memory for the partial result. The call to the kernel from Listing 1 is specific and determined to be automatically optimised by the compiler.

3.2.2. Micro-architecture use

As hardware moves forward to boost executions, we adapt code to the architecture design to well-exploit resources and core pipeline.

Vectorisation. Due to its embarrassingly parallel nature, the generated spatial loop can benefit from auto-vectorisation [8] using machine knowledge (SIMD length) and loop dependence analysis. Still, compilers need assistance in applying this optimisation. We transparently ensure data alignment at the library level for each field buffer by allocating memory at an address multiple of parameter alignment set to the cache line size, optimal for memory movements. Apart from base pointer alignment, vectorisation relies on known and aligned accesses. Within Saiph FDM modules, stencil computations represent the principal cause of memory access. Applying a stencil at a specific mesh element (i,
implies accessing its neighbours. For the first dimension, $\text{meshXdim}$, the stencil involves contiguous memory accesses; the other dimensions neighbouring have non-unit strides, computed from the $(i, j, k)$ element address plus an offset multiple of $\text{meshXdim}$. To maximise aligned accesses, we apply a padding strategy; $\text{meshXdim}$ adds extra points to force its size to be multiple of memory cache lines. Thus, each data row perfectly fits into several cache lines ensuring contiguous or aligned stencil access. Moreover, cache lines size is multiple of the vector units instruction size (set through $\text{vectorSize}$ parameter) so, as long as the starting index of the spatial loop matches the start of a data row, the spatial loop is vectorised without peeled or remainder loops.

Figure 6 shows this automated aligned access pattern for a first order stencil computation in a 2D spatial domain. The neighbouring access of the $(i, j)$ element is contiguous for the first dimension and aligned for the second.

To hint the compiler about data alignment, we automatically emit specific clauses at the intermediate code. We declare field buffer pointers with underscored attributes for Intel or GNU, respectively. We mark $\text{meshXdim}$ and the lower bound of the spatial loop as multiples of alignment: underscored for Intel, $\text{idx} \& -\text{alignment}$ for GNU, and we add the portable pragma `omp simd` right before the loop. Similarly, we use the clause `omp declare simd` at library kernels to enable their SIMD versions.

**Spatial blocking.** Stencil data-locality improves if implemented by means of data chunks; memory pieces fitting into the cache optimise their reuse [9, 10]. For that, we add blocking strategies at different levels of the DSL. At the C++ library, once the mesh is discretised, we compute the number of blocks per mesh dimension through iterative cuts based on the $\text{L3size}$ parameter (L3 cache size).
We adopt a 2.5D blocking technique \[11, 12\]: blocking non-contiguous dimensions while streaming the computations over the first one, thus maintaining the innermost loop well-conditioned for vectorisation. At the Scala layer, we generate a code able to support any blocking decision taking place at the C++ library. Listing 2 shows the generic skeleton of the loop. Intermediate code includes library method calls setting upper loop bounds.

3.3. Exploiting intra-node parallelism

3.3.1. Fork-join model

We transparently obtain a parallel code by generating the OpenMP clause 
\#pragma omp parallel for collapse(3) at the intermediate code, right before the embarrassingly parallel spatial loop. The clause envelops the loop so that blocks are distributed among threads, each of them starting at a vectorisation beneficial aligned index. Since threads share the local memory, we adapt the blocking decisions to maintain a good locality; we increment the number of blocks to have, at least, as many blocks as working threads (parameter numThreads) fitting simultaneously into the cache. In such a way, there is enough parallel work to feed numThreads while the blocks computed in parallel occupy less than L3size, ensuring a good locality.

3.3.2. Task model

This paradigm represents an appealing approach for HPC-CFD problems \[13, 14\]. The model requires annotating the code with task constructs enclosing pieces of code that will be asynchronously executed in parallel; we specify tasks data-dependencies to ensure correct execution order. We develop two new DSL modules using OpenMP and OmpSs-2 \[3\] programming models, respectively. In both, we generate an annotated intermediate code creating tasks that envelop spatial block updates. This code generation happening at the Scala layer precedes the allocation of problems fields. Thus, to state task dependencies over the not-yet-allocated buffers, we use abstract representative structures whose elements represent blocks. At the numerical library, we define such structure, shown in Figure 7 as a multi-dimensional array of chars, with as many dimensions as the input mesh and as many elements as the number of blocks per dimension plus two. Adding two elements per dimension allows us to specify stencil dependencies generically without worrying about boundary block cases.

We handle two of such structures mapping the source (read) and the destination (write) buffers, respectively, to state the time dependencies. Finally, we use the pointers to the structures as lambda functions’ arguments to enable their use at the spatial loop. Listing 2 shows the annotated loop generated within the OmpSs2-module.

```c
for(int zb = 0; zb < nbz; ++zb) {
    for(int yb = 0; yb < nbY; ++yb) {
        for(int xb = 0; xb < nbX; ++xb) {
            #pragma oss task in(repSRC[xb][yb][zb]) in(repSRC[xb+1][yb][zb]) ... out(repDST[xb][yb][zb])
        }
    }
}
```
for(int z = 0; z < bsz; ++z) {
  for(int y = 0; y < bsy; ++y) {
    #pragma forceinline recursive
    #pragma omp simd
    for(int x = 0; x < bsx; ++x) {

Listing 2: Generated spatial loop skeleton for OmpSs-2 use

Taskifying the spatial loop requires protecting or applying the equivalent tasking strategy to other computations at the exact buffer locations. Thus, we adapt BCs computations to happen within tasks at the same spatial blocks and use abstracted dependencies to relate them to the ones from the lambda function. We exploit the hidden temporal parallelism allowing asynchronous block time progress. Figure 8 shows the Saiph task scheme for a generic block update. The task $A$ encapsulating a block update depends on previous BCs computations tasks $B$ over neighbouring blocks. Once executed, the current BCs task is ready for execution.

Figure 8: Explicit FDM task scheme for a 2D block update

3.4. Exploiting inter-node parallelism

We transparently apply a domain decomposition approach at the C++ library to exploit inter-node parallelism [15, 16]. Each node is in charge of a
portion of the domain, and we manage dependencies through data redundancy and message passing mechanisms. We use the standard Message Passing Interface (MPI) library for communications. We permit cuts in each dimension of the input mesh depending on the parameter `numProcs`, stating the number of MPI processes of the execution. Redundant data, or halos, are communicated to neighbouring MPI processes at the end of each step. We apply gathering and scattering techniques for non-contiguous halos messages.

Cutting a dimension implies adding halos to each local mesh, adjusting the spatial loop bounds accordingly. Figure 9 schematizes a local mesh portion of a 3D distributed mesh. We ensure a vectorisable contiguous spatial traversal while minimising redundant computations by avoiding last dimension halos updates. Moreover, to adjust to the single/multi-core automated optimisations, we apply padding to each mesh portion’s contiguous dimension.

![Figure 9: MPI 3D local mesh](image)

### 3.5. Exploiting hybrid parallelism

We can explore different levels of parallelism, independently or consciously combined. We mix inter and intra-node parallelism within Saiph hybrid modules, combining fork-join/task model and message passing libraries. While combining fork-join and MPI distribution does not imply interoperability issues, task model requires to protect communications using barriers or encapsulating them inside other tasks. The Task-Aware MPI Library (TAMPI) \[4\] improves the interoperability between MPI and OpenMP/OmpSs-2 by efficiently executing MPI operations from inside tasks constructs. The non-blocking TAMPI model avoids barriers and the underuse of computational resources when waiting for communications. Thus, computations and communications overlap. Figure 10 shows the task flow of a hybrid taskified time-step. We encapsulate communications into \(C\) tasks with their corresponding dependencies. While inner mesh blocks do not contain halos, we can group boundary block communications within the same task to take profit from established connections. This allows us to explore communication task granularity. We set the number of grouped blocks through parameter `commBlocks`.

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4. Evaluation

In this section we evaluate the quality of the code generated by Saiph and the parallelisation strategies implemented. On section 4.1 we describe the contextual framework for such evaluation. Then, sections 4.2, 4.3 and 4.4 conduct the Saiph performance evaluation at single-core, multi-core and distributed levels respectively.

4.1. Methodology

4.1.1. Saiph apps

We use several Saiph applications [2] to evaluate our contributions. These applications are open-source [5], and they include a reference output to validate their correctness. Table 1 details the applications used and their memory accesses and operations required to update a mesh point. Each application involves a fixed number of stencil operations (\(\text{ops}\)) computed with a certain spatial accuracy (\(\text{acc}\)). This spatial accuracy is a Saiph parameter stated by users to determine the numerical precision of stencils. Computationally, the accuracy determines the number of neighbour points involved per stencil, which determines the computational intensity of the application.

Table 1: Saiph apps speedups and details per mesh point update depending on stencil operations and accuracy (\(\text{ops/acc}\))

| App            | Mesh points & Mem. use (MB) | Mem access/point \(x+\text{ops(acc+1)}\) | FLOP/point \(y+\text{ops(2(acc+1)+1)}\) | Saiph-\(\lambda\) vs tree-traversal |
|----------------|-----------------------------|---------------------------------|---------------------------------|----------------------------------|
| 1DSineWave     | 100001 - 1.5                | 13+1(acc+1)                     | 2+1(2(acc+1)+1)                 | 3.9x                             |
| 2DSmithHutton  | 2001*1001 - 61              | 24+4(acc+1)                     | 8+4(2(acc+1)+1)                 | 13.9x                            |
| 2DInviscidVortex | 1601*1601 - 215             | 69+12(acc+1)                    | 25+12(2(acc+1)+1)               | 13.8x                            |
| 3DHeat         | 301*201*201 - 185           | 13+3(acc+1)                     | 2+3(2(acc+1)+1)                 | 4.5x                             |

4.1.2. Hand-tuned codes

We develop hand-tuned codes for each of the Saiph applications tested. Such codes explicitly implement the targeted single-core optimisations that Saiph
automatically applies. We validate the results produced by the optimised hand-tuned codes and we use them as baselines to appraise the performance of Saiph automatic optimisations.

4.1.3. Yask kernels

Yask [17] is a state-of-the-art framework for the exploration of the HPC stencil-performance design space. The tool provides automatic stencil optimisations, including cache blocking, vector folding and vectorisation from high-level stencil kernels specifications and generates, from the user code, parallel programs using multiple cores through OpenMP threads. Yask and Saiph tackle different domains and levels of abstractions but can be compared regarding the quality of the code generated. To conduct such a comparison, we develop a 3D Heat equation kernel within Yask. For that, we use Yask version 3.05.06 [18] and compile the kernel using different compilers with default optimisation parameters.

4.1.4. Tests

All applications use double-precision floating-point formats. We firstly address, on Section 4.2, the single-core absolute performance of Saiph generated code using different native compilers and compare such results against manually optimised codes and literature results. Then, on Sections 4.3 and 4.4 we explore parallelisation strategies through scaling performance studies tackling the three levels of HPC resources.

This evaluation procedure aims to validate the proposed collection of optimisations and the strategies to apply and combine them automatically to demonstrate the DSL scalability and high performance. Quantifying productivity and comparing Saiph to other CFD tools is an extremely challenging task because each framework targets a different level of abstraction and provides different optimisations. This extended evaluation scapes the scope of the paper and we contemplate it as future work.

4.1.5. Hardware

We run the applications on BSC’s Marenostrum 4 supercomputer [19]. Compute nodes are equipped with two sockets, Intel Xeon Platinum 8160 CPU with 24 cores each, supporting vectorisation instructions up to AVX-512 and sharing an L3 cache of 33MB. The experiments in Section 4.3 are limit to single socket to avoid NUMA issues. For the same reason, the hybrid MPI+OmpSs-2 experiments described on Section 4.4 use one MPI rank per socket. In this case, the 24 cores assigned to each rank are exploited through OpenMP/OmpSs-2 threads.

4.1.6. Parametric runs

Saiph runs are defined by the set of parameters (alignment, vectorSize, L3size, numThreads, numProcs, commBlocks). The firsts are hardware-dependent, and we set them to 64 bytes (L3 lines size), 8 (double-precision floating-points fitting on AVX-512) and 33MB, respectively. Regarding computing resources,
we select \texttt{numThreads} and \texttt{numProcs} according to the execution test. Finally, the \texttt{commBlocks} parameter allows exploring performance enhancement at hybrid TAMPI and OmpSs-2 runs. We empirically set it to 4. Once set, parameters automatically combine and determine the code transformations that lead to specific optimised parallel code.

4.1.7. Compilers

Table 2 displays the compiler versions and corresponding flags used to compile Saiph, Yask and the hand-tuned codes. All the codes involving the OmpSs-2 programming model have been compiled using LLVM; for other codes, if nothing is specified, binaries are built from Intel.

| Compiler-Versions | Flags                                      |
|-------------------|--------------------------------------------|
| ICC - 2020.1      | -O3 -qopenmp -qopenmp-simd                |
| icpc              | -inline-forceinline                        |
|                   | -xCORE-AVX512                              |
|                   | -qopt-zmm-usage=high                       |
| GCC - 9.2.0       | -O3 -fopenmp -fopenmp-simd                 |
| g++               | --forceinline -ftree-vectorize             |
|                   | -march=skylake-avx512                      |
| LLVM- 13.0.0      | GCC flags                                  |
| ompss-2[2]        | [+] -fompss-2                              |

4.2. Single-Core Performance

We test the performance of spatial loops for the applications of Table 1 using a default stencil accuracy of 2. At this level, we choose small problem sizes to stress vector units and assert the generated code’s effectiveness.

4.2.1. Saiph-lambda vs Saiph-tree-traversal

We start comparing the new method to solve Saiph’s equations based on \texttt{lambdas}’ generated at compile-time against the original method based on traversing equation trees at runtime. Results are presented in the last column of Table 1. Saiph based on \texttt{lambdas} outperforms old implementations [1] [2] by a factor of 4x to 14x depending on the length of the equation trees. This performance increase comes from the fact that lambda functions generated at compile-time enable native compiler optimisations that cannot be applied when tree-traversals take place at runtime.
4.2.2. Hand-tuned code vs Yask kernel

To evaluate the quality of our hand-tuned codes, we compare the single-core performance of the 3D Heat equation application manually implemented against Yask results. The application mainly involves the computation of a second-order stencil, so it can be easily specified using Yask. Moreover, stencils represent the most challenging patterns to optimise within Saiph. Thus, by proving the high quality of stencil computations, we demonstrate the overall quality of the explicit FDMs for CFD. We confront the 3D Heat equation hand-tuned code against the corresponding Yask kernel, using different compilers. Table 3 show the performance results of the different implementations of the 3D Heat equation running on a single-core. Results are reported using memory bandwidth, GFLOPS and Mpoints/s as absolute performance metrics. While the first two are implementation and optimisation dependent, Mpoints/s is based on the problem size, a user-fixed parameter. Hence, we focus on this last metric for a more fair comparison across implementations.

| Compiler | Heat3D app implementation | GB/s | GFLOPS | Mpoints/s |
|----------|---------------------------|------|--------|-----------|
| icpc     | Hand-tuned                | 99.01| 12.87  | 574       |
|          | Yask                      | 61.41| 9.92   | 524       |
|          | Saiph                     | 96.43| 12.54  | 559       |
| g++      | Hand-tuned                | 32.79| 4.26   | 190       |
|          | Yask                      | 24.25| 3.90   | 230       |
|          | Saiph                     | 27.82| 3.61   | 161       |
| clang++  | Hand-tuned                | 97.09| 12.62  | 562       |
|          | Yask                      | 58.92| 9.49   | 586       |
|          | Saiph                     | 98.14| 12.76  | 569       |

Hand-tuned and Yask implementations deliver comparable results between each other and when using Intel and LLVM compilers. However, when using the Gnu C++ compiler, the Yask kernel runs about 56% slower than the same kernel built with the Intel C++ compiler. This performance drop is higher for the hand-tuned implementation, which shows a 67% of performance drop when using g++. Overall, those results demonstrate that our manually developed codes successfully encode optimisations benefiting explicit FDMs patterns. Moreover, the compiler choice determines the performance of the final binary.

4.2.3. Saiph vs hand-tuned codes

We appraise Saiph automated optimisations from implementations in section 3.2 against our manually optimised codes versions, using different native compilers. Figure 11 shows normalised results, taking the most performant run as the baseline for Intel, GNU and LLVM compilers. At each barplot, the first set
of bars corresponds to hand-tuned loop bodies. The second set, *Saiph-lambda*, refers to the new implementation based on the lambdas, described above, which do not include any additional optimisation. We use this version as the baseline for the last three code sets, incrementally enabling compile-time evaluations, vectorisation and blocking. For *icpc*, the most optimised Saiph version provides 28x, 25x, 28x, and 26x of performance increase compared to the *Saiph-lambda* results and 0.95x, 1.2x, 1.1x, and 0.98x against hand-tuned codes. The use of other compilers show similar results. Although the use of the *g++* compiler presents lower performance results in overall, Saiph optimised codes reach or surpass hand-tuned ones’ performance; the automatically generated regular structures can overcome hand-written codes. Binaries built from *g++* and *clang++* show how vectorisation can be enabled without clauses, happening at +compOpts versions. In such cases, we see a slight performance drop when using clauses: compiler transformations can produce different codes depending on the order they are applied so that default automated decisions can be preferable. However, benefits, when such transformation is not guaranteed, justify the use of clauses. Finally, multi-dimensional blocking shows low impact because substantial concurrency is necessary to push the limits of the memory system [21]. However, memory pressure at the cache level will appear for memory demanding cases under shared-memory parallelism.

4.2.4. *Saiph vs Yask*  
Finally, we compare Saiph single-core optimised code against Yask results. For that, we use the 3D Heat equation application and the fully automatically optimised Saiph version. Table 3 adds Saiph performance results along with the already evaluated hand-tuned and Yask ones. Numbers illustrate how Saiph single-core performance is comparable with Yask results. Using the GNU C++ compiler, Saiph suffers from a higher drop in performance than Yask, compared to Intel results. Binaries built from other compilers show competitive performance. Saiph single-core optimisations and their automatic application are thus validated.
4.3. Multi-core Scaling Performance

We use the already evaluated Saiph optimised single-core results as baselines to address the spatial loop’s scalability at the inter-core level. We evaluate the fork-join model from section 3.3 and verify that previous optimisations are preserved. Figure 12 show results up to a socket (24 cores) for the 3D Heat application comparing Saiph vectorised and non-vectorised implementations against Yask results.

![Figure 12: Multi-core performance comparisons of Saiph and Yask OpenMP fork-join 3D Heat application](image)

All versions scale up to 16 cores while vectorised results outperform scalar ones by a factor of > 3. We conduct a roofline analysis [22] to obtain the actual upper bounds of performances for the Saiph vectorised runs using 16 cores. Within such runs, the spatial loop delivers 742.88 GB/s, surpassing the DRAM and L3 bandwidth peak performances of 114 GB/s and 353 GB/s, respectively. Stencil computations are usually memory-bounded, but the working set of the analysed application is small (185 MB). Moreover, the Saiph blocking technique enables the reuse of cached memory, crucial for surpassing the roof of L3 cache bandwidth. Hence, the loop’s performance is not limited by the simultaneous accesses of the 16 cores to the same L3 cache of 33 MB. A deeper analysis characterises the loop as a cache-bound workload, where the L1 and L2 cache stalls are the most significant cause of performance loss. Saiph optimised results are close to the machine peak performance. Moreover, Saiph and Yask present similar scaling results. The Saiph automated combination of low-level optimisation and shared-memory parallelism is then validated. Saiph multi-core support provides competitive performance close to the processor peak performance.

We repeat the previous scaling study for the different Saiph applications. Figure 13 shows scaling results for blocked and vectorised applications taking the optimised single-core execution as a baseline. We assess that Saiph blocking technique ensures good memory locality and enough parallel work for linear scaling performance. However, the number of cores (numThreads) determines
the blocks, so the performance of the parallel code. Hence, efficiency is suboptimal for ill-suited configuration; load imbalances appear if `numThreads` is not multiple of the number of blocks. This fact can be hypothesised when using 24 threads and confirmed with the corresponding trace on the left of Figure 14. The execution on the right shows how using the tasking module can prevent such a performance drop.

![Figure 13: Fork-join parallel scalability at socket level](image)

![Figure 14: Main mesh and BCs updates using fork-join (left) and tasks (right) models.](image)

The shared-memory parallelism is firmly bound to the automatic loop blocking technique and the balanced work partition, leading to linear scalability under the appropriate combination of parallel paradigms and hardware resources. Saiph eases the exploration of such key parameters that affect performance, giving insight into the best running configurations. In the previous tests, we realised that runs using 16 core provide the same performance as those using 24 cores but using less power. Similarly, Saiph modules permit us to compare different parallel paradigms to choose the best fitting one.

### 4.4. Distributed Scaling Performance

Lastly, we evaluate the applications’ inter-node parallelism through weak and strong scaling studies. For that, we use bigger problem sizes and evaluate memory bound workloads and communications overheads.
We present a weak scaling study for the evaluation of the distribution strategy from sections 3.3 and 3.5. For distributed executions assessment, communications and their required data manipulations play an essential role. Thus, we take one-node executions (2 MPIs) as baselines for 2D applications and four-node executions (8 MPIs, 3D mesh partition) for 3D use cases. Tests results in Figure 15 show linear scalability of up to 32 nodes for pure MPI and hybrid OpenMP fork-join modules.

Finally, we carry out a strong scaling study for the 3D Heat equation application. For that, we enlarge the spatial mesh, set the spatial stencil accuracy to 8 and compute 500 time-steps. According to Table 1, the new problem size of 2401*1201*1201 mesh points, occupy 51.6 GB (2 buffers read/write using double precision) and involves 63 Tera memory accesses, 4.72 Tera stencils and a total of 93 TFLOPs. Figure 16 displays the absolute performance behaviour from 4 to 32 nodes using and combining different shared-memory and distributed parallel paradigms from Saiph. Pure MPI runs use as many MPI processors as available cores in the nodes, while hybrid runs bind MPI processors to sockets and use as many threads as cores in the socket. Finally, the blocking technique is automatically applied to each local mesh to use the most appropriate granularity for the intra-node parallel work.

Distributing the same problem size across a different number of nodes illustrates the transition from memory-bound to compute-intensive workloads ending up in scenarios where communications overheads become costly. Saiph hybrid executions show linear scaling up to 16 nodes. When using 32 nodes, local computations decreases while communications increase, producing imbalances leading to a non-linear performance scaling. Overall, task versions deliver higher performance and better scalability than the fork-join version by reducing computation load imbalances. Concretely, the use of TAMPI presents higher performance than the rest of Saiph versions, including the pure MPI one. TAMPI allows computations and communications to overlap, increasing the overall per-
Figure 16: Strong scaling for the 3D Heat application using different hybrid parallelisations performance and scalability of the runs. By taking the four-node execution as a
reference, the TAMPI-OmpSs-2 module outperforms the MPI fork-join, tasks
and pure versions by a factor of 1.7x, 1.3x and 1.3x, respectively. Those re-
results validate Saiph implementations and demonstrate its competitive results.
Different modules allow a parallel exploration to select the most performant
paradigms.

5. Related Work

Many tools target the CFD domain to deliver performance, portability, or
productivity [23]. Mainly divided into two main branches, there are frameworks
tackling stencil computation performance and DSLs facing complete CFD, PDEs
system resolution.

In the first group, different existing frameworks provide automated low-level
stencil optimisations and parallel implementations. Liszt [24] is a DSL for un-
structured mesh computations. The language is designed for code portability
across heterogeneous platforms. Liszt users work at the numerical level giving
information to ensure that the compiler can infer data dependencies. Similarly,
for unstructured mesh computations, OPS/OP2 [25, 26] and PyOP2 [27] as
the Python extension, give an abstraction for stencil computations at CPUs,
GPUs, and distributed systems. Such DSLs are embedded in C/Fortran and
Python, respectively. Yask [17] is a C++ library also for automatic stencil
optimisations. Cache blocking, vector folding and vectorisation are automati-
cally applied. Moreover, Yask generates from the user code parallel programs
using multiple cores and distributed-memory parallelism. ExaSlang [28] is an-
other stencil-specific programming language that provides different layers of
abstraction and exploits domain information for neighbouring access optimisa-
tions. Targeting ExaSlang, ExaStencils [29] is a code generator to generate all
optimised lower layers codes to automatically get optimal configurations and
implementations. The above tools cover a wide range of domains, designs, de-
development platforms, languages and hardware targeted, optimisations and par-
allelisation strategies. However, they lack the abstraction of the whole picture of
a CFD problem. While stencils are highly optimised, time integration methods
or ICs and BCs are not part of the language, leaving users to code the complete
parallel workflow.

The second approach uses a top-level abstraction expressing the CFD prob-
lem in terms of actual differential equations. Those tools focus on a particular
set of parallel numerical methods, leaving the implementation’s details to lower-
level libraries. This is the case of FEniCS [30], a complete simulation infra-
structure for many real-world problems. FEniCS relies upon expressing PDEs
at the mathematical level using Python and C++ interfaces. The tool defines a
language for the Finite Element Method and generates parallel codes that can
be executed in parallel using MPI. Although FEniCS is a compelling solution
for many complex problems, it requires deep expertise in numerical methods
to be used. Similarly, Firedrake [31] uses the PyOP2 library for parallelising
user high-level code. OpenSBLI [32] focus on the solution of the compressible
Navier-Stokes equations. The tool uses symbolic Python to allow the specifi-
cation of PDEs using Einstein notation which automatically discretises to generate
OPS code. Devito [33] uses similar symbolic Python mainly focusing on seis-
mic inversion problems. Devito optimisations include common sub-expression
elimination, vectorisation, blocking and inter and intra-node parallelism.

While the first type of tools lacks part of the PDEs resolution process, the
last usually rely on other frameworks to apply low-level optimisations and paral-
lelisation strategies. This top-down dependence can worsen the use of advanced
parallel paradigms such as the task model. Saiph comprehends the combination
of the above-targeted philosophies. It offers a CFD high-level syntax hiding
numerical complexities while combining low-level automatic optimisations and
parallelisation strategies leading to high-performance executions codes. As the
above tools, Saiph design is based on layers separating concerns, however, the
proposed execution model ensures the interaction between the high-level syntax
layer and the low-level modules enabling to intertwine user code and low-level
optimisations and parallelisation strategies.

6. Conclusions

In this work, we have enhanced Saiph, a high-level DSL for solving CFD
problems using FDM, to generate optimised algorithmic patterns that leverage
state-of-the-art optimisation techniques. This work demonstrates how to enable
and combine the most relevant optimisation techniques from a high-level specifi-
cation code. We extend Saiph to exploit high-performance algorithmic patterns
found in FDM. While maintaining abstraction and generality, we establish the
procedure to generate codes exploiting single, multi-core, and cluster resources:
Saiph ensures high efficient sequential runs enabling compiler optimisations and
vectorisation through automated compile-time evaluations, data-alignment and
padding strategies. Moreover, the DSL transparently provides scalable par-
allel codes preserving single-core optimisations; using an appropriate blocking
technique Saiph offers enough and well-balanced inter-core parallelism while
enhancing data locality and preserving data alignment at each parallel chunk.
Tasking and fork-join parallelisation versions are available. Saiph automatically distributes the mesh across several nodes but preserving the optimisations applied at the core and node level. Thus, following a bottom-up approach, we consciously combine such strategies from single-core to cluster level, preserving their effectiveness and obtaining high performance, competitive with hand-tuned codes. We conclude that exploiting domain knowledge allows DSLs to assume and retrieve information from the high-level code. Then, generic underlying implementations of optimisations and parallelisation strategies can be intertwined with the user code through the build process proposed. In such a scenario, we automatically generated optimised codes using advanced parallelisation strategies and different parallel paradigms performing and scaling as much as manually optimised ones. Further, due to the customisable nature of Saiph, it is possible to conduct a performance exploration under different parallelisation strategies. Looking forward, we see the opportunity of transparently applying the best strategy for each input application.

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