A Family of Transformerless Quadratic Boost High Gain DC-DC Converters

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Abstract: This paper presents three new and improved non-isolated topologies of quadratic boost converters (QBC). Reduced voltage stress across switching devices and high voltage gain with single switch operation are the main advantages of the proposed topologies. These topologies utilize voltage multiplier cells (VMC) made of switched capacitors and switched inductors to increase the converter’s voltage gain. The analysis in continuous conduction mode is discussed in detail. The proposed converter’s voltage gain is higher than the conventional quadratic boost converter, and other recently introduced boost converters. The proposed topologies utilize only a single switch and have continuous input current and low voltage stress across switch, capacitors, and diodes, which leads to the selection of low voltage rating components. The converter’s non-ideal voltage gain is also determined by considering the parasitic capacitance and ON state resistances of switch and diodes. The efficiency analysis incorporating switching and conduction losses of the switching and passive elements is done using PLECS software (Plexim, Zurich, Switzerland). The hardware prototype of the proposed converters is developed and tested for verification.

Keywords: voltage multiplier cell (VMC); quadratic boost; voltage stress; non-isolated

1. Introduction

High gain DC-DC converters are now used in several applications when high DC voltage is required. These converters can work in the power range of few milliwatts to a megawatt range. They are used in solar photovoltaic (PV) applications, robotics, aircraft, medical equipment, high voltage DC systems, and electric vehicles. These converters are made up of different combinations of inductors, capacitors, diodes, and switches that are connected suitably so that energy transfer can take place between inductors and capacitors. The energy is stored in the switched inductors and then transferred to the capacitors to obtain a high voltage [1] at the output. Conventional switch mode boost converter (CBC) and other variants like single-ended primary-inductor converter (SEPIC) and ZETA converters cannot produce high voltage gain, and the active and passive components have high voltage and current stress. Moreover, the efficiency also decreases significantly at higher duty ratios. Several topologies utilize a combination of switched capacitors [2] and switched inductors to obtain high voltage. Topologies that utilize coupled inductors and transformers are also used to obtain a very high voltage. A voltage multiplier cell (VMC) is also used to boost or buck-boost [3] the voltage at low duty cycles. High gain with reduced stress voltage and current stress on the switching devices and passive components, common ground, continuous input current, and reduced number of components are...
desirable features that are required in any high gain DC-DC converter. The converter has high efficiency and reduced stress across capacitors. A modified boost converter using switched inductors VMC is proposed in [4]. A single switch modified boost and SEPIC converters with continuous input current and low voltage stress across the switch are proposed in [5,6]. Hybrid structures with switched inductors [7] and multilevel structures using switched capacitors [8] are used to increase the gain of the converter. A VMC made up of a switched inductor limits the high ripple in input current, whereas in switched capacitor topologies high spike in charging current is noticed [9]. Some topologies use voltage doublers before the output to reduce the stress and increase the voltage gain, at the cost of an increase in the number of components [10]. The topologies proposed in [11,12] have quadratic voltage gain and utilize only a single switch. In [13], a three-winding coupled inductor is used but that makes the circuit complex. The problems associated with leakage inductance of the coupled inductor is addressed in [14] without using the snubber circuit. A transformer with a voltage doubler is designed to obtain very high voltage is developed in [15]. A converter is proposed in [16] which can work in triple duty mode, but to obtain a high gain, the number of switches is high. To achieve high gain, boost converters with different types of VMC combinations are shown in [17]. Single input, dual output DC-DC converters have the advantage of two outputs [18] with reduced stress on the output capacitors. The interleaved high gain boost converter has H-bridge structure with unidirectional switches. The converters utilize many VMCs to output to increase the voltage gain, which is a disadvantage. These converters utilize at least [19–21] two switches that can be operated at the same or different duty cycle. In quasi-Z-source topologies, the duty cycle is mostly limited up to less than 0.5. These converters need a careful operation as the converter can become [22,23] unstable at smaller duty ratios close to the maximum limit. In these converters, the input current is continuous. The converter gain is affected by several factors such as parasitic resistance of inductors and capacitors and ON-state resistance of switches and diodes. Hence, a non-ideal model [24] should be developed to calculate the gain in non-ideal conditions. Quadratic boost converters (QBC) produce high voltage gain at low duty ratios. High voltage gain at low duty ratios reduces the current and voltage stress high efficiency can be achieved. These converters mostly utilize VMC and several inductors and capacitors to achieve the high voltage gain. Non-isolated topologies of these converters are suitable in microgrid operations [25–28] for medium power applications. These converters can be put at the front end of the inverter to maintain the DC-link voltage. In [29] an ultra-high gain DC-DC converter is proposed with three inductors and two switches.

Table 1 presents the summary of important high gain DC-DC converters discussed above in the literature. From the table, it can be observed that topologies can be differentiated based on the features such as voltage gain, switch voltage stress, components count, and common ground. It is to be mentioned that the desirable features such as high voltage gain and low voltage stress with a reduced number of components may not always be present in all topologies. A tradeoff between high gain and the number of components always exists. Similarly, other features like common ground and continuous input current may also be important in different applications.

| Topology | Inductors | Capacitors | Switch | Diodes | Voltage Gain | Voltage across Switch | Common Ground |
|----------|-----------|------------|--------|--------|--------------|----------------------|---------------|
| [3]      | 1         | 3          | 1      | 3      | \(\frac{2}{1-D}\) | Low                  | Yes           |
| [4]      | 2         | 1          | 2      | 2      | \(\frac{1+D}{1-D}\) | Low                  | Yes           |
| [5]      | 2         | 4          | 1      | 3      | \(\frac{1}{D(1-D)}\) | Low                  | Yes           |
| [6]      | 2         | 4          | 1      | 4      | \(\frac{3+D}{1-D}\) | Low                  | Yes           |

Table 1. Characteristic features of the converters discussed in the literature.
In this paper, a family of quadratic boost converters with switched capacitors is proposed. Further, the structure can be extended to increase the voltage gain. The proposed converter’s gain is double the gain of a conventional quadratic boost converter (CQBC), and the voltage stress is half the output voltage. The converters have only one switch and continuous input current, which makes them suitable for solar PV and microgrid applications. Moreover, no transformer or coupled inductor is used to achieve such a high gain. In Sections 2–4 the structure and working of the proposed three converters are discussed in detail. In Section 5, the comparison of the proposed converter with other high

| Topology       | Inductors | Capacitors | Switch | Diodes | Voltage Gain | Voltage across Switch | Common Ground |
|-----------------|-----------|------------|--------|--------|--------------|-----------------------|---------------|
| [7]             | 3         | 1          | 2      | 3      | \(\frac{1+2D}{1-D}\) | Low                   | No            |
| [8]             | 2         | 4          | 1      | 4      | \(\frac{3+D}{1-D}\)  | Low                   | No            |
| [9]             | 2         | 5          | 1      | 5      | \(\frac{3(1+D)}{(1-D)^2}\)  | Low                   | Yes           |
| [10]            | 2         | 3          | 1      | 6      | \(\frac{2(1+D)}{(1-D)^2}\)  | Low                   | No            |
| [11]            | 1 + 1 Coupled Inductor | 3      | 1      | 3      | \(\frac{(1+n)D}{(1-D)^2}\)  | High for a low value of n | Yes           |
| [14]            | 1 + 1 Coupled Inductor | 3      | 1      | 5      | \(\frac{2-D}{(1-D)^2}\)  | n = 1                  | Yes           |
| [15]            | 1 + 1 Transformer | 4      | 1      | 5      | \(\frac{(1+n)}{(1-D)^2}\)  | Low                   | Yes           |
| [16]            | n + 1     | n + 1     | n + 2  | n + 2  | \(\frac{n+1}{(1-D)^2}\)  | n = no. of legs       | Low           | No            |
| Conventional QBC | 2         | 2          | 1      | 3      | \(\frac{1}{(1-D)^2}\)  | High                   | Yes           |
| [22]            | 2         | 3          | 1      | 3      | \(\frac{1}{(1-D)^2}\)  | Low                   | No            |
| [23]            | 2         | 5          | 2      | 5      | \(\frac{3(1-D)}{(1-D)^2}\)  | Low                   | No            |
| [26]            | 3         | 3          | 1      | 5      | \(\frac{2}{(1-D)^2}\)  | High                   | Yes           |
| [27]            | 3         | 6          | 2      | 5      | \(\frac{2+D}{(1-D)^2}\)  | Low                   | No            |
| [28]            | 3         | 6          | 1      | 6      | \(\frac{2+D}{(1-D)^2}\)  | Low                   | No            |
| [29]            | 3         | 4          | 1      | 6      | \(\frac{3-D}{(1-D)^2}\)  | Low                   | Yes           |
| [30]            | 8         | 1          | 4      | 17     | \(\frac{1+7D}{(1-D)^2}\)  | Low                   | Yes           |
| Proposed Converter I | 2       | 4          | 1      | 5      | \(\frac{2}{(1-D)^2}\)  | Low                   | No            |
| Proposed Converter II | 2     | 4          | 1      | 5      | \(\frac{2}{(1-D)^2}\)  | Low                   | No            |
| Proposed Converter III | 3    | 5          | 1      | 7      | \(\frac{4}{(1-D)^2}\)  | Low                   | No            |
gain converters in terms of voltage gain, voltage, and current stresses are described. In Section 6, the experimental results of all three converters are presented. In Section 7, the conclusion is discussed.

2. Proposed Converter I

The power circuit in Figure 1a comprises one active switch S, two inductors \( L_1 \) and \( L_2 \), four capacitors \( C_1, C_2, C_3, \) and \( C_0 \) and five diodes \( D_1, D_2, D_3, D_4, \) and \( D_5 \). The converter is operated at high-frequency \( f_s \). The network consisting of \( D_2, C_2, C_3, \) and \( D_5 \) constitutes a voltage boosting cell. The advantage of this circuit is that it has a single switch S with lower complexity with continuous input current and utilizing energy with a single input DC source.

Figure 1. (a) Proposed converter I and operating modes of the converter: (b) Mode I and (c) Mode II.

2.1. Analysis in CCM Mode

There are two modes of operation based on the switching signal. The first is when the switch is ON, and the second one is when the switch is OFF. Important waveforms for the proposed converter are shown in Figure 2.
2.1.1. MODE I [0-DT]

When the switch S is turned ON, the equivalent circuit is depicted in Figure 1b. The diode D₃ and D₄ are conducting, and other diodes are reverse biased. Both the inductor currents rise while capacitor C₁, C₂, and C₃ discharge to feed the load R and the related equations are as follows:

\[
\begin{align*}
V_{L1} &= V_{in} \\
V_{L2} &= V_{C1} \\
V_{C2} - V_{O} + V_{C3} + V_{L1} &= 0 \\
V_{C2} + V_{C3} + V_{in} &= V_{o}
\end{align*}
\] (1)

2.1.2. MODE II [DT-T]

The switch S is turned OFF, as shown in Figure 1c. The diodes D₁, D₂, and D₅ are conducting and the rest diodes are OFF. The inductor currents fall, and C₁, C₂, and C₃ discharge and load R are fed by Cₒ. The related equations are as follows:

\[
\begin{align*}
V_{L1} &= V_{in} - V_{C1} \\
V_{L2} &= V_{C1} - V_{C3} \\
V_{C2} + V_{L2} + V_{L1} &= 0 \\
V_{C2} &= V_{C3} - V_{in}
\end{align*}
\] (2)

From Equations (1) and (3), we obtain

\[V_{C3} = V_{o}/2\] (5)

Applying the principle of voltage–second balance on the inductors L₁ and L₂

\[
\begin{align*}
\int_{0}^{T} V_{L1}(t) \cdot dt &= 0 \\
V_{in} \times DT + (V_{in} - V_{C1}) \times (1 - D)T &= 0 \\
V_{C1} &= \frac{V_{in}}{(1-D)}
\end{align*}
\] (6)

\[
\begin{align*}
\int_{0}^{T} V_{L2}(t) \cdot dt &= 0 \\
V_{C1} \times DT + (2V_{C1} - V_{O}) \times (1 - D)T &= 0 \\
V_{O} &= \frac{2V_{C1}}{(1-D)}
\end{align*}
\] (7)

The relations obtained from (6) and (7) can be used to find the voltage gain

\[M_{CCM} = \frac{V_{o}}{V_{in}} = \frac{2}{(1-D)^2}\] (8)

It is assumed that the circuit is ideal by applying the energy conservation principle

\[
\begin{align*}
V_{in}I_{in} &= V_{o}I_{o} \\
I_{in} &= I_{L1} \\
I_{L1} &= \frac{V_{o}}{V_{in}}I_{o} = \frac{2}{(1-D)}I_{o}
\end{align*}
\] (9)

where Iₖ₁ is the average current of inductor L₁ and Iₒ = \(\frac{V_{o}}{R}\) is the load current.
The average value of the inductor current $I_{L2}$ can be calculated by applying a charge balance on the capacitor $C_1$.

$$
\begin{aligned}
0 \leq t & \leq D \times (1-D)T, \\
0 & \leq t \leq D \times (1-D)T,
\end{aligned}
\begin{align*}
\int_0^T I_{C1}(t) \, dt &= 0 \\
D \times (-I_{L2}) + (1-D) \times (I_{L2} - I_{L1}) &= 0 \\
I_{L2} &= (1-D)I_{L1} = \frac{2I_o}{1-D} \\
I_S &= I_{in} - I_o = \frac{(1+2D-D^2)I_o}{(1-D)^2}
\end{align*}
(10)

The current stress on the switch of the proposed converter I is given by (10).

![Typical waveforms of the proposed converter I in CCM.](image)

The voltage stress or blocking voltage of a power device is important for deciding the voltage rating of the switch. The voltage stress across the power switch ($V_S$) and diodes ($D_1$, $D_2$, $D_3$, $D_4$, and $D_5$) of the converter I can be derived as

$$
\begin{align*}
V_S &= \frac{V_{in}}{1-D} = \frac{V_o}{2} \\
V_{D1} &= \frac{V_{in}}{1-D} = \frac{(1-D)}{2}V_o \\
V_{D2} &= V_{D4} = \frac{V_{in}}{(1-D)^2} = \frac{V_o}{2} \\
V_{D3} &= \frac{D V_{in}}{(1-D)^2} = \frac{D}{2}V_o \\
V_{D5} &= \frac{V_{in}}{(1-D)^2} = \frac{V_o}{2}
\end{align*}
(11)

It can be inferred from (11) that the stress across $D_1$, $D_3$, $D_4$, and $D_5$ and switch $S$ is equal to half of the output voltage.

2.2. Passive Components Selection

The peak-to-peak ripple values of the inductor current can be expressed as

$$
\begin{align*}
L_1 &= \frac{V_{in}}{M_{L1}} DT = \frac{V_{in}}{M_{L1}} DT = \frac{V_{in}}{M_{L1}} DT = \frac{V_{in}}{M_{L1}} DT = \frac{V_{in}}{M_{L1}} DT = \frac{V_{in}}{M_{L1}} DT
\end{align*}
(12)
With known values of D, the input source $V_{\text{in}}$, and switching frequency $f_s$, the design values of inductors $L_1$ and $L_2$ can be calculated.

For achieving the boundary condition, $I_{L_1} = \frac{\Delta I_1}{2}$ and $I_{L_2} = \frac{\Delta I_2}{2}$. The condition of continuous conduction mode can be achieved using (9) and (12):

$$
\begin{align*}
L_1 &> \frac{D(1-D)^2R}{4f_s} \\
L_2 &> \frac{D^2(1-D)^2R}{4f_s}
\end{align*}
$$

(13)

The peak-to-peak ripple across the capacitors $C_1$, $C_2$, $C_3$, and $C_0$ is $\Delta V_{C1}$, $\Delta V_{C2}$, $\Delta V_{C3}$, and $\Delta V_{C4}$ respectively, and can be expressed as

$$
\begin{align*}
C_1 &= \frac{\Delta Q_1}{\Delta V_{C1}} = \int_0^{D} i_{C1} \cdot dt = \frac{-2DV_o}{R(1-D)R\Delta V_{C1}s} \\
C_2 &= \frac{\Delta Q_2}{\Delta V_{C2}} = \int_0^{D} i_{C2} \cdot dt = \frac{V_o}{R\Delta V_{C2}s} \\
C_3 &= \frac{\Delta Q_3}{\Delta V_{C3}} = \int_0^{D} i_{C3} \cdot dt = \frac{V_o}{R\Delta V_{C3}s} \\
C_0 &= \frac{\Delta Q_0}{\Delta V_{C0}} = \int_0^{D} i_{C0} \cdot dt = \frac{V_o}{R\Delta V_{C0}s}
\end{align*}
$$

(14)

With known values of D, the input source $V_{\text{in}}$ and switching frequency $f_s$, the design values of capacitances can be calculated from Equation (14).

2.3. Boundary Condition Mode

It is assumed that the inductor current $I_{L_1}$ remains continuous while inductor current $I_{L_2}$ goes in discontinuous conduction mode with zero current at the end of every switching period.

The DC value of the inductor current $L_2$ can be found as

$$I_{L_{2dc}} = \frac{V_{C1}}{2L_2} DT$$

(15)

The boundary normalized inductor time constant on the inductor $L_2$ is defined as

$$\tau_{L_2} = \frac{L_2f_s}{R}$$

(16)

The boundary normalized inductor time can be derived from (10) and (12):

$$\tau_{L_{2b}} = \frac{D^2(1-D)^2}{4}$$

(17)

To operate the converter in CCM mode, $\tau_{L_2}$ must be greater than $\tau_{L_{2b}}$. Otherwise, the converter goes in DCM, as depicted in Figure 3.

Figure 3. Boundary between CCM and DCM mode of operation.
3. Proposed Converter II

The proposed converter II is shown in Figure 4a and has an equal number of components of converter I. The power circuit consists of one switch $s$, two inductors $L_1$ and $L_2$, five diodes $D_1$, $D_2$, $D_3$, $D_4$, and $D_5$, and four capacitors $C_1$, $C_2$, $C_3$, and an output capacitor $C_0$ supplying energy to load $R$. The proposed converter has the inductor on the input side, which makes the current continuous with very low ripple.

![Diagram of Proposed Converter II](image)

**Figure 4.** (a) Proposed converter II and operating modes: (b) switch is ON and (c) switch is OFF.

### 3.1. Analysis in CCM Mode

The two modes of operation follow.

#### 3.1.1. Mode I $[0-DT]$

When the switch is turned ON, the equivalent circuit is depicted in Figure 4b. The diodes $D_2$ and $D_5$ are conducting while $D_1$, $D_3$, and $D_4$ are reversed biased. The switch $S$ is conducting an interval of $DT$ where $D$ is the duty ratio, and $T$ is the switching signal.
period. The currents of both inductors rise and capacitors $C_1$, $C_2$, and $C_3$ discharge to charge output capacitor $C_0$ to feed load $R$. The related equations follow:

\[
\begin{align*}
V_{L1} &= V_{\text{in}} \\
V_{L2} &= V_{C1} \\
V_{C2} + V_{C3} &= V_o
\end{align*}
\]  

(18)  

(19)

3.1.2. Mode II [DT-T]

Contrarily, the switch is in OFF condition, and diodes $D_1$, $D_3$, and $D_4$ are conducting while diode $D_2$ and $D_5$ are in reverse biased, as shown in Figure 4c. The important waveforms for this converter are shown in Figure 5. The currents of both inductors fall to charge capacitors $C_1$, $C_2$, and $C_3$, while $C_0$ separately feeds the load $R$. The related equations follow:

\[
\begin{align*}
V_{L1} &= V_{\text{in}} - V_{C1} \\
V_{L2} &= V_{C1} - V_{C2} \\
V_{C2} &= V_{C3}
\end{align*}
\]  

(20)  

(21)

Using (15) and (17), the capacitor voltages are

\[
V_{C2} = V_{C3} = \frac{V_o}{2}
\]  

(22)

Applying the principle of voltage–second balance on the inductors $L_1$ and $L_2$ by using (14)–(18) gives

\[
\begin{align*}
\int_0^T V_{L1}(t) \cdot dt &= 0 \\
V_{\text{in}} \times DT + (V_{\text{in}} - V_{C1}) \times (1 - D)T &= 0 \\
V_{C1} &= \frac{V_{\text{in}}}{(1 - D)}
\end{align*}
\]

(23)

\[
\begin{align*}
\int_0^T V_{L2}(t) \cdot dt &= 0 \\
V_{C1} \times DT + \left(\frac{2V_{C1} - V_o}{2}\right) \times (1 - D)T &= 0 \\
V_o &= \frac{2V_{C1}}{(1 - D)}
\end{align*}
\]

(24)

Results obtained from (20) and (21) are used to find voltage gain of the proposed converter II:

\[
M_{\text{CCM}} = \frac{V_o}{V_{\text{in}}} = \frac{2}{(1 - D)^2}
\]  

(25)

It is assumed that the circuit is ideal by applying the energy conservation principle:

\[
\begin{align*}
\frac{V_{\text{in}}}{V_{\text{in}}} I_{\text{in}} &= V_o I_o \\
I_{\text{in}} &= I_{L1} \\
I_{L1} &= \frac{V_o}{V_{\text{in}}} I_o = \frac{2}{(1 - D)^2} I_o
\end{align*}
\]

(26)

where $I_{L1}$ is the average current of inductor $L_1$ and $I_o = \frac{V_o}{R}$ is the load current.
The average value of the inductor current $I_{L2}$ could be calculated by applying charge balance on the capacitor $C_1$:

$$
\begin{align*}
D \times (-I_{L2}) + (1-D) \times (I_{L2} - I_{L2}) &= 0 \\
I_{L2} &= (1-D)I_{L2} = \frac{2D}{2(1-D)} \\
I_S &= I_{in} - I_o = \left(1+2D-D^2\right)I_o \\
&= \frac{1}{1-D}
\end{align*}
$$

The current stress on the switch of proposed converter II is given by (27). The voltage stress or blocking voltage of a power device is important to decide the ratings of the semiconductor devices. The stress of the power switch ($V_S$) and across $D_1, D_2, D_3, D_4$, and $D_5$ of the converter II can be shown as follows

$$
\begin{align*}
V_S &= \frac{V_{in}}{(1-D)^2} = \frac{V_o}{2} \\
V_{D1} &= \frac{V_{in}}{(1-D)^2} = \frac{(1-D)V_o}{2} \\
V_{D2} &= \frac{D_{V_{in}}}{(1-D)^2} = \frac{D}{2}V_o \\
V_{D3} &= V_{D4} = \frac{V_{in}}{(1-D)^2} = \frac{V_o}{2} \\
V_{D5} &= \frac{V_{in}}{(1-D)^2} = \frac{V_o}{2}
\end{align*}
$$

It can be inferred from (28) that the stress across diodes $D_1, D_3, D_4, D_5$ and switch $S$ is equal and half of the output voltage.

### 3.2. Passive Component Selection

The peak-to-peak ripple values of the inductor current can be expressed as

$$
\begin{align*}
L_1 &= \frac{V_{in}}{\Delta I_{L1}}DT = \frac{V_{in}}{\Delta I_{L1}}DT = \frac{V_{in}}{\Delta I_{L1}}DT = \frac{V_{in}}{\Delta I_{L1}}DT \\
L_2 &= \frac{V_{in}}{\Delta I_{L2}}DT = \frac{V_{in}}{\Delta I_{L2}}DT = \frac{V_{in}}{\Delta I_{L2}}DT
\end{align*}
$$

With known values of $D$, the input source $V_{in}$ and switching frequency $f_s$, the design values of inductors $L_1$ and $L_2$ can be calculated.
The boundary condition is achieved when the minimum inductor current reaches zero, i.e., \( I_{L1} = \frac{\Delta v_1}{2} \) and \( I_{L2} = \frac{\Delta v_2}{2} \). The condition of continuous conduction mode can be achieved as

\[
\begin{align*}
L_1 &> \frac{D(1-D)^2R}{4L} \\
L_2 &> \frac{D^2(1-D)^2R}{4L}
\end{align*}
\]  

(30)

The peak-to-peak ripple across the capacitors \( C_1, C_2, C_3, \) and \( C_0 \) is \( \Delta v_1, \Delta v_2, \Delta v_3, \) and \( \Delta v_4 \), respectively, and can be expressed as

\[
\begin{align*}
C_1 &= \frac{\Delta Q_1}{\Delta v_1} = \frac{\int_{0}^{DT} i_{C1} \, dt}{\Delta v_1} = \frac{2DV_0}{(1-D)R \Delta v_1} \\
C_2 &= \frac{\Delta Q_2}{\Delta v_2} = \frac{\int_{0}^{DT} i_{C2} \, dt}{\Delta v_2} = \frac{V_o}{R \Delta v_2} \\
C_3 &= \frac{\Delta Q_3}{\Delta v_3} = \frac{\int_{0}^{DT} i_{C3} \, dt}{\Delta v_3} = \frac{V_o}{R \Delta v_3} \\
C_0 &= \frac{\Delta Q_0}{\Delta v_4} = \frac{\int_{0}^{DT} i_{C0} \, dt}{\Delta v_4} = \frac{(1-D)V_o}{R \Delta v_4}
\end{align*}
\]  

(31)

With known values of \( D \), the input source \( V_{in} \), and switching frequency \( f_s \), the design values of capacitances can be calculated using (31) with the assumption of \( C_2 = C_3 \).

### 3.3. Boundary Condition

It is assumed that the inductor current \( I_{L1} \) remains continuous while inductor current \( I_{L2} \) goes in discontinuous conduction mode with zero current at the end of every switching period.

The DC value of the inductor current \( L_2 \) can be found as

\[
I_{L2,dc} = \frac{V_{C1}}{2L_2}DT
\]  

(32)

The boundary normalized inductor time constant on the inductor \( L_2 \) is defined as

\[
\tau_{L2} = \frac{L_2f_s}{R}
\]  

(33)

The boundary normalized inductor time can be derived from (27) and (29):

\[
\tau_{L2b} = \frac{D^2(1-D)^2}{4}
\]  

(34)

To operate the converter in CCM mode, \( \tau_{L2} \) must be greater than \( \tau_{L2b} \); otherwise, the converter goes in DCM, as depicted in Figure 6.

![Figure 6. Boundary between CCM and DCM mode of operation.](image)
4. Proposed Converter III

Proposed converter III is an extension of proposed converter II in which inductor $L_2$ is replaced with a switched inductor boost cell consisting of $D_3$, $D_4$, $L_2$, and $L_3$ as shown in Figure 7a, with single switch $S$ and energy increased by boosting cell to feed load $R$. The proposed converter has two voltage multiplier cells that increase output voltage by four times.

![Proposed Converter III](image)

**Figure 7.** (a) Proposed converter III and operating modes: (b) switch is ON and (c) switch is OFF.

4.1. Analysis in CCM Mode

The continuous conduction mode of the converter can be discussed in detail with two modes of operation.

4.1.1. Mode I [0-DT]

When the switch is turned ON, the equivalent circuit is depicted in Figures 7b and 8. The diodes $D_2$, $D_3$, $D_5$, and $D_7$ are conducting while $D_1$, $D_5$, and $D_6$ are reversed biased.
All three inductor currents rise and capacitors C₁ to C₄ discharge to feed the load R. The switch S conducts for the DT period. The related equations follow:

\[
\begin{align*}
V_{L1} &= V_{in} \\
V_{L2} &= V_{L3} = V_{C1} = V_{C2} \\
V_{C3} + V_{C4} &= V_o
\end{align*}
\] (35) (36)

4.1.2. Mode I [DT-T]

Contrarily, the switch is in OFF condition, and diodes D₁, D₅, and D₆ are conducting while diode D₂, D₃, D₄, and D₇ are in reverse biased, as shown in Figures 7c and 8. The switch is conducting for an interval of (1-D) T. Both the inductor currents fall to charge capacitors C₁, C₂, and C₃, while C₀ separately feeds the load R. The related equations follow:

\[
\begin{align*}
V_{L1} &= V_{in} - V_{C1} \\
V_{L2} &= V_{L3} \\
V_{C1} - V_{L2} - V_{L3} + V_{C2} &= V_{C3} \\
V_{L2} &= V_{L3} = V_{C1} - \frac{V_{C1}}{2} \\
V_{C3} &= V_{C4} = \frac{V_o}{2}
\end{align*}
\] (37) (38)

Applying the principle of voltage–second balance on the inductors L₁ and L₂ and L₃ and by using (33)–(36), V₀ and V₇ can be obtained as shown in (39) and (40).

\[
\begin{align*}
\int_0^{T} V_{L1}(t) \cdot dt &= 0 \\
V_{in} \times DT + &\left(V_{in} - V_{C1}\right) \times (1-D)T = 0 \\
V_{C1} &= \frac{V_{in}}{1-D} \quad \text{(39)}
\end{align*}
\]

\[
\begin{align*}
\int_0^{T} V_{L2}(t) \cdot dt &= 0 \quad \text{or} \quad \int_0^{T} V_{L3}(t) \cdot dt &= 0 \\
V_{C1} \times DT + &\left(V_{C1} - \frac{V_{C2}}{2}\right) \times (1-D)T = 0 \\
V_{C1} \times D + &\left(V_{C1} - \frac{V_o}{2}\right) \times (1-D) = 0 \\
V_{o} &= \frac{4V_{C1}}{(1-D)} \quad \text{(40)}
\end{align*}
\]

Figure 8. Typical waveforms of the proposed converter II in CCM.
Results obtained from (37) and (38) are used to find the voltage gain of the proposed converter III:

\[
M_{CCM} = \frac{V_o}{V_{in}} = \frac{4}{(1-D)^2} \tag{41}
\]

It is assumed that the circuit is ideal by applying the energy conservation principle:

\[
\begin{align*}
V_{in}I_{in} &= V_oI_o \\
I_{L1} &= \frac{V_o}{V_{in}}I_o = \frac{4}{(1-D)^2}I_o \\
\end{align*}
\tag{42}
\]

where \(I_{L1}\) is the average current of inductor \(L_1\) and \(I_o\) is the load current.

The DC component of the inductor currents of \(L_2\) and \(L_3\) \((I_{L2} = I_{L3})\) can be calculated by applying charge balance on capacitors \(C_1\) and \(C_2\):

\[
\begin{align*}
I_{L2} &= I_{L3} = \frac{2V_o}{(1-D)} \\
I_S &= I_{in} - I_o = \frac{(3+2D-D^2)}{(1-D)^2}I_o
\end{align*}
\tag{43}
\]

The current stress on the switch of the proposed converter III is given by (43). The voltage stress or blocking voltage of a power device is important to decide the semiconductor device rating.

The stress of the power switch \(S\) and diodes of the converter III can be derived as

\[
\begin{align*}
V_S &= \frac{2V_{in}}{(1-D)^2} = \frac{V_o}{2} \\
V_{D1} &= \frac{V_{in}}{(1-D)} = \frac{(1-D)}{4} V_o \\
V_{D2} &= \frac{(1-D)V_{in}}{(1-D)^2} = \frac{1}{4} V_o \\
V_{D3} &= V_{D4} = \frac{V_{in}}{(1-D)} = \frac{V_o}{4} \\
V_{D5} &= V_{D6} = \frac{2V_{in}}{(1-D)^2} = \frac{V_o}{2} \\
V_{D7} &= \frac{2V_{in}}{(1-D)^2} = \frac{V_o}{2}
\end{align*}
\tag{44}
\]

With known values of \(D\), the input source \(V_{in}\), and switching frequency \(f_s\), the design values of inductors \(L_1\) and \(L_2 = L_3\) can be calculated.

The boundary condition is achieved when the minimum inductor current reaches zero, i.e., \(I_{L1} = \frac{\Delta i_{L1}}{2}\) and \(I_{L2} = \frac{\Delta i_{L2}}{2}\). The condition of continuous conduction mode can be achieved as

\[
\begin{align*}
L_1 &> \frac{D(1-D)R}{8f_s} \\
L_2 &= L_3 > \frac{D^2(1-D)^2R}{4f_s}
\end{align*}
\tag{46}
\]
The peak-to-peak ripple across the capacitors $C_1$, $C_2$, $C_3$, $C_4$, and $C_0$ are $\Delta V_{C1}$, $\Delta V_{C2}$, $\Delta V_{C3}$, $\Delta V_{C4}$, and $\Delta V_{C0}$, respectively, and can be expressed as

$$
\begin{align*}
C_1 &= \frac{\Delta Q_1}{\Delta v_{C1}} = \frac{I_{L1}^{d} t_{L1}^{d} dt}{\Delta v_{C1}} = \frac{(1+D)V_o}{(1-D)R\Delta v_{C1}S} \\
C_2 &= \frac{\Delta Q_2}{\Delta v_{C2}} = \frac{I_{L1}^{d} t_{L1}^{d} dt}{\Delta v_{C2}} = \frac{2V_o}{R\Delta v_{C2}S} \\
C_3 &= \frac{\Delta Q_3}{\Delta v_{C3}} = \frac{I_{L1}^{d} t_{L1}^{d} dt}{\Delta v_{C3}} = \frac{V_o}{R\Delta v_{C3}S} \\
C_4 &= \frac{\Delta Q_4}{\Delta v_{C4}} = \frac{I_{L1}^{d} t_{L1}^{d} dt}{\Delta v_{C4}} = \frac{V_o}{R\Delta v_{C4}S} \\
C_0 &= \frac{\Delta Q_0}{\Delta v_{C0}} = \frac{I_{L1}^{d} t_{L1}^{d} dt}{\Delta v_{C0}} = \frac{(1-D)V_o}{R\Delta v_{C0}S}
\end{align*}
$$

With known values of $D$, the input source $V_{in}$, and switching frequency $f_s$, the design values of capacitances can be calculated using (47) with the assumption of $C_3 = C_4$.

4.3. Boundary Condition

It is assumed that the inductor current $I_{L1}$ remains continuous while inductor current $I_{L2} = I_{L3}$ goes in discontinuous conduction mode with zero current at the end of every switching period.

The DC value of the inductor current $L_2 = L_3$ in this mode can be found as

$$I_{L2,dc} = I_{L3,dc} = \frac{V_{C1}}{2L_2} DT \quad (48)$$

The boundary normalized inductor time constant on the inductor $L_2 = L_3$ is defined as

$$\tau_{L2,3} = \frac{L_2 f_s}{R} \quad (49)$$

The boundary normalized inductor time can be derived from (43) and (45):

$$\tau_{L2,3b} = \frac{D^2(1-D)^2}{4} \quad (50)$$

To operate the converter in CCM mode, $\tau_{L2,3}$ must be greater than $\tau_{L2,3b}$. Otherwise, the converter goes in DCM, as depicted in Figure 9.

![Figure 9](image-url) Boundary between CCM and DCM mode of operation.

5. Comparison of the Proposed Topologies

Several DC-DC converters have been proposed to achieve high gain and improved high efficiency. In this section, the comparison of the proposed converter with other recently introduced topologies in Table 2 is shown. The converters are compared based on voltage...
gain, switch voltage stress, current stress, and component count. Converter I and III have lower components than the proposed converter in [7]. The proposed converter in [30] has more components than all the proposed converters. In addition, it utilizes many power switches, which makes the circuit bulky. The curve of the proposed converter III is the highest among all the curves of Figure 10. Proposed converters I and II also have a high voltage gain compared to the other topologies above $D = 0.3$. The gain of converters I and II is also high as compared to other converters, which substantially increases above $D = 0.4$. The proposed converter in [7] has three inductors, but the gain is much less than the proposed family of converters. Similarly, the topology of [8] uses two inductors, but the gain is limited at higher duty ratios. The conventional quadratic boost converter (QBC) has a low gain compared to the proposed topologies. The voltage stress across the switch as a function of voltage gain is shown in Figure 11a. As the gain increases, the voltage stress across the switch of converters I and II is much less than the other topologies, except for the topologies proposed in [8,30]. Moreover, for voltage gain up to 12 times, the stress across the converter III is less than other converters proposed in [6,7,14,18,30]. The low voltage stress across components results in increased efficiency and low cost of the converter. The efficiency of the converter depends on factors such as voltage/current ratings, components count, and the type of converter. The comparison concerning the switch current stress is shown in Figure 11b. The proposed converters have lower current stress than the converter proposed in [6]. The switch current stress of all three proposed converters and the converter presented in [14] is the same as QBC, but QBC has low voltage gain and high voltage stress. The curve in Figure 12 presents the variation of efficiency with the output power at constant voltage stress on the switch, but it has a more components, which makes the circuit bulky.

Table 2. Comparison with other converters.

| Topology           | $N_L$ | $N_C$ | $N_SW$ | $N_D$ | $M_{CCM}$ $(V_d/V_{in})$ | Average Switch Current Stress $(I_s/I_{in})$ | $M_{CCM}$ at $D = 0.5$ | $S_{CCM}$ $(V_s/V_{in})$ |
|--------------------|-------|-------|--------|-------|---------------------------|--------------------------------|------------------------|-------------------------|
| [6]                | 2     | 4     | 1      | 4     | $\frac{3\times D}{1-D}$  | $\frac{1+3D}{(1+D)^2}$                    | 3.5                    | $\frac{1}{1-D}$        |
| [7]                | 4     | 1     | 2      | 7     | $\frac{1+3D}{(1+D)^2}$    | $\frac{D}{(1+D)^2}$                     | 5                     | $\frac{1}{1-D}$        |
| [8]                | 2     | 3     | 2      | 3     | $\frac{1+D}{(1+D)^2}$     | $\frac{1}{(1+D)^2}$                    | 7                     | $\frac{1}{1-D}$        |
| [14] Coupled Inductor | 3     | 1     | 5      |       | $2 \times \frac{D}{1-D} \frac{1-D}{n=1}$ | $\frac{1-D-D^2}{2}$                        | 6                     | $\frac{2}{1-D}$        |
| QBC                | 2     | 2     | 1      | 3     | $\frac{1}{(1-D)^2}$       | $2D - D^2$                                | 4                     | $\frac{1}{1-D^2}$      |
| [30] Proposed Converter I | 8     | 1     | 4      | 17    | $\frac{1+7D}{(1+D)^2}$    | $\frac{4(1-D)}{1+7D}$                    | 9                     | $\frac{S = 1}{1+3D}$   |
| Proposed Converter II | 2    | 4     | 1      | 5     | $\frac{2}{(1-D)^2}$       | $\frac{1+2D-D^2}{2}$                      | 8                     | $\frac{1}{1-D^2}$      |
| Proposed Converter III | 3    | 5     | 1      | 7     | $\frac{4}{(1-D)^2}$       | $\frac{1+2D-D^2}{2}$                      | 16                    | $\frac{2}{1-D^2}$      |
Figure 10. Voltage gain vs. duty cycle.

(a) 
(b) ...

Normalized Switch Current Stress
(Is/Iin)
Voltage Gain
[Proposed (I/II/III)/QBC/14]
[6]
[7/S1]
[7(S2)/8]
[30]

Figure 11. (a) Voltage stress vs. voltage gain. (b) Normalized current switch stress vs. voltage gain.
The measured and ideal voltage gain for converters I and II are presented in Figure 13a. At lower duty, the difference between the ideal and measured voltage gain is very low; however, the difference increases with the duty ratio increase. This happens because, at a higher duty ratio, the internal losses in the circuit become higher. The measured gain is taken in experimental conditions. Loss calculation is done on PLECS software by putting the switching and conduction loss data into the lookup table of the developed thermal model. In PLECS software, accurate loss analysis can be done by using the real models of switches and diodes from the datasheet to calculate the conduction and switching losses. The bifurcation of power loss in different components for converter I and II are shown in Figure 13b.

![Efficiency vs. output power curve.](image1)

**Figure 12.** Efficiency vs. output power curve.

![Comparison between the ideal and experimental gain of converters I and II. Bifurcation of power loss in different components for converter I and II.](image2)

**Figure 13.** (a) Comparison between the ideal and experimental gain of converters I and II. (b) Bifurcation of power loss in converters I and II.

6. **Experimental Verification of the Proposed Converters**

The laboratory prototype of each proposed converter was developed and tested under laboratory conditions. The hardware setup is shown in Figure 14.
6.1. Proposed Converter I

The design specification of the proposed converter I is presented in Table 3. The laboratory hardware prototype of the converter is shown in Figure 15.

Table 3. Design specification of converter I (adapted from [31]).

| Elements            | Specification                                           |
|---------------------|---------------------------------------------------------|
| Maximum Power       | 150 W                                                   |
| Input Voltage       | 24 V                                                    |
| Switching Frequency | 50 kHz                                                  |
| Load Resistance     | $R = 200–400 \, \Omega$, Chroma electronic load simulator model 63202 |
| Inductors           | $L_1 = L_2 = 330 \, \mu H$                             |
| Capacitors          | $C_1 = 100 \, \mu F/63 \, V$, $C_2 = C_3 = 47 \, \mu F/200 \, V$ & $C_O = 68 \, \mu F/250 \, V$ |
| Power MOSFET        | SPW52N50C3                                             |
| Diodes              | SF8L60USM                                              |
| Gate Drivers IC     | TLP250H                                                 |
| Microcontroller     | STM32 Nucleo H743Z12, STM Microelectronics, Geneva, Switzerland |

The results shown in Figure 16 are shown at a duty ratio of 0.4 with a load resistance of 200 Ω.
6.2. Proposed Converter II

The design specification of the proposed converter II is presented in Table 4. The laboratory hardware prototype of the converter is shown in Figure 17.

Table 4. Design specification of converter II (adapted from [31]).

| Elements                  | Specification                                                                 |
|---------------------------|-----------------------------------------------------------------------------|
| Maximum Power             | 150 W                                                                       |
| Input Voltage             | 24 V                                                                        |
| Switching Frequency       | 50 kHz                                                                      |
| Load Resistance           | R = 350 Ω, Chroma electronic load simulator model 63202                     |
| Inductors                 | $L_1 = L_2 = 330 \mu H$                                                     |
| Capacitors                | $C_1 = 100 \mu F/63 V, C_2 = C_3 = 47 \mu F/200 V \& C_O = 68 \mu F/350 V$ |
| Power MOSFET              | SPW52N50C3                                                                  |
| Diodes                    | SF8L60USM                                                                   |
| Gate Drivers IC           | TLP250H                                                                      |
| Microcontroller           | STM32 Nucleo H743ZI2, Microelectronics, Geneva Switzerland                  |
The results shown in Figure 18 are taken at a duty ratio of 0.4 with a load resistance of 350 Ω.

Figure 18. Related waveforms of the experimental results for proposed converter II. (a) Gating pulse, input voltage, and output voltage; (b) gating pulse, voltage for capacitor C₁ and C₂; (c) gating pulse, inductor current for L₁ and L₂; and (d) gating pulse, switch voltage, and output voltage.
6.3. Proposed Converter III

The design specification of the proposed converter III is presented in Table 5. The laboratory hardware prototype of the converter is shown in Figure 19.

Table 5. Design specification of converter III (adapted from [31]).

| Elements                  | Specification                                                                 |
|---------------------------|-------------------------------------------------------------------------------|
| Maximum Power             | 150 W                                                                         |
| Input Voltage             | 24 V                                                                          |
| Switching Frequency       | 50 kHz                                                                        |
| Load Resistance           | \( R = 200 \, \Omega \), Chroma electronic load simulator model 63202         |
| Inductors                 | \( L_1 = L_2 = L_3 = 330 \, \mu H \)                                         |
| Capacitors                | \( C_1 = C_2 = C_3 = C_4 = 47 \, \mu F/200 \, V \), \( C_O = 68 \, \mu F/350 \, V \) |
| Power MOSFET              | SPW52N50C3                                                                    |
| Diodes                    | SF8L60USM                                                                     |
| Gate Drivers IC           | TLP250H                                                                        |
| Microcontroller           | STM32 Nucleo H743ZI2                                                          |

![Gate Driver Circuit](image)

Figure 19. Proposed converter III hardware prototype.

The results shown in Figure 20 are taken at a duty ratio of 0.2 with a load resistance of 350 \( \Omega \).

![Waveform Diagram](image)

Figure 20. Cont.
The paper presents three different high gain DC-DC converter topologies of the quadratic gain family. While two of the topologies have twice the quadratic boost gain, the third has four times the quadratic boost gain, making them extremely effective for low duty high gain operation at high efficiency. None of the topologies uses any transformers and has a gain of more than ten times at a duty ratio of less than 0.5. Topology II is found to have

### Table 6. Experimental results.

| Topology | Duty Ratio | Load Resistance | Capacitor Voltage | Inductor Current | Switch Stress | Output Voltage | Deviation from Ideal Voltage | Efficiency |
|----------|------------|-----------------|-------------------|-----------------|---------------|----------------|-----------------------------|------------|
| I        | 0.4        | R = 200 Ω       | V_{C1} = 38.1 V, V_{C2} = 39.6 V, V_{C3} = 60.8 V | I_{L1} = 4.01 A, I_{L2} = 2.22 A | V_S = 60.8 V, V_o = 127 V | 4.75% | 95.33% |
| II       | 0.4        | R = 350 Ω       | V_{C1} = 38.5 V, V_{C2} = 64.9 V, V_{C3} = 28.3 V | I_{L1} = 2.10 A, I_{L2} = 1.21 A | V_S = 61.9 V, V_o = 130 V | 2.55% | 97.5% |
| III      | 0.2        | R = 200 Ω       | V_{C1} = 25.1 V, V_{C2} = 61.2 V | I_{L1} = 4.04 A, I_{L2} = 1.62 A | V_S = 61.2 V, V_o = 128 V | 14.66% | 85.33% |

7. Conclusions

In the first converter case, the hardware prototype’s measured output voltage is 127 volts at a 0.4 duty ratio. However, in the second topology, the output voltage is measured as 130 volts at the same input voltage and duty ratio as that of the first converter; due to higher load resistance, the voltage is higher in the second converter case. In the first converter case, the load resistance is only around 60% of the load resistance, as in the second converter case. Thus, the current is high in the first converter circuit, which increases the first converter’s internal losses compared to that of the second converter. With the increase in the load current, the output voltage decreases because of the rise in the circuit’s internal losses.

In the third converter case, the measured output voltage is 128 volts at a duty ratio of 0.2 and load resistance of 200 Ω, which is almost 15% lower than the calculated voltage for the ideal condition. The deviation from the ideal voltage is the same as explained before, which is internal power loss. These internal losses depend on the number of components in the circuit, ESR (equivalent series resistance) of the passive components, diode forward voltage drop, switching frequency and load, etc. The findings of the experimental results are provided in Table 6.
comparatively high efficiency as compared to topology 1 and III. The stress in switches in the three topologies are less for a wide operating range as compared to many recently proposed high gain quadratic converters. The efficiency of converter I and converter II at 100 W is found to be 92% and 93.2% respectively. The efficiency of converter III is close to 87%. The continuous input current along with reduced voltage stress makes all of the proposed topologies suitable for renewable energy applications.

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**References**

1. Forouzesh, M.; Siwakoti, Y.P.; Gorji, S.A.; Blaabjerg, F.; Lehman, B. Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications. *IEEE Trans. Power Electron.* 2017, 32, 9143–9178. [CrossRef]
2. Maroti, P.K.; Padmanaban, S.; Holm-Nielsen, J.B.; Bhaskar, M.S.; Meraj, M.; Iqbal, A. A New Structure of High Voltage Gain SEPIC Converter for Renewable Energy Applications. *IEEE Access* 2019, 7, 89857–89868. [CrossRef]
3. Shayeghi, H.; Pourjafar, S.; Hashemzadeh, S.M. A switching capacitor based multi-port bidirectional DC–DC converter. *IET Power Electron.* 2021. [CrossRef]
4. Sadaf, S.; Bhaskar, M.S.; Meraj, M.; Iqbal, A.; Al-Emadi, N. A Novel Modified Switched Inductor Boost Converter With Reduced Switch Voltage Stress. *IEEE Trans. Ind. Electron.* 2021, 68, 1275–1289. [CrossRef]
5. Shahir, F.M.; Babaei, E.; Farsadi, M. Extended Topology for a Boost DC–DC Converter. *IEEE Trans. Power Electron.* 2019, 34, 2375–2384. [CrossRef]
6. Saravanan, S.; Babu, N.R. Design and Development of Single Switch High Step-Up DC–DC Converter. *IEEE J. Emerg. Sel. Top. Power Electron.* 2018, 6, 855–863. [CrossRef]
7. Tang, Y.; Fu, D.; Wang, T.; Xu, Z. Hybrid Switched-Inductor Converters for High Step-Up Conversion. *IEEE Trans. Ind. Electron.* 2015, 62, 1480–1490. [CrossRef]
8. Tang, Y.; Wang, T.; He, Y. A Switched-Capacitor-Based Active-Network Converter with High Voltage Gain. *IEEE Trans. Power Electron.* 2014, 29, 2959–2968. [CrossRef]
9. Arunkumari, T.; Indragandhi, V.; Arunkumar, G.; Sanjeevikumar, P.; Holm-Nielsen, J.B. Implementation of a high-gain non-isolated DC-DC converter for PV-fed applications. *Int. Trans. Electr. Energy Syst.* 2020, 30, 1–18. [CrossRef]
10. Shanthi, T.; Prabha, S.U.; Sundaramoorthy, K. Non-isolated n-stage High Step-up DC-DC Converter for Low voltage DC Source Integration. *IEEE Trans. Energy Convers.* 2021. [CrossRef]
11. Hasanpour, S.; Baghramian, A.; Mojallali, H. Analysis and Modeling of a New Coupled-Inductor Buck–Boost DC–DC Converter for Renewable Energy Applications. *IEEE Trans. Power Electron.* 2020, 35, 8088–8101. [CrossRef]
12. Hasanpour, S.; Siwakoti, Y.P.; Mostaan, A.; Blaabjerg, F. New Semiquadratic High Step-Up DC/DC Converter for Renewable Energy Applications. *IEEE Trans. Power Electron.* 2021, 36, 433–446. [CrossRef]
13. Moradpour, R.; Tavakoli, A. A DC–DC boost converter with high voltage gain integrating three-winding coupled inductor with low input current ripple. *Int. Trans. Electr. Energy Syst.* 2020, 30, 1–23. [CrossRef]
14. Lee, S.; Do, H. Quadratic Boost DC–DC Converter with High Voltage Gain and Reduced Voltage Stresses. *IEEE Trans. Power Electron.* 2019, 34, 2397–2404. [CrossRef]
15. Wang, Y.; Qu, Y.; Bian, Q.; Guan, Y.; Xu, D. A Single Switch Quadratic Boost High Step Up DC-DC Converter. *IEEE Trans. Ind. Electron.* 2019, 66, 4387–4397. [CrossRef]
16. Bhaskar, M.S.; Almakhles, D.J.; Padmanaban, S.; Holm-Nielsen, J.B.; Kumar, A.R.; Masebinu, S.O. Triple-Mode Active-Passive Parallel Intermediate Links Converter With High Voltage Gain and Flexibility in Selection of Duty Cycles. *IEEE Access* **2020**, *8*, 134716–134727. [CrossRef]

17. Abdel-Rahim, O.; Funato, H.; Haruna, J. A comprehensive study of three high-gain DC-DC topologies based on Cockcroft-Walton voltage multiplier for reduced power PV applications. *IEEE Trans. Electr. Electron. Eng.* **2018**, *13*, 642–651. [CrossRef]

18. Farhadi-Kangarlu, M.; Khiavi, A.M.; Neyshabouri, Y. A non-isolated single-input dual-output boost DC–DC converter. *IET Power Electron.* **2021**, *14*, 936–945. [CrossRef]

19. Alzahrani, A.; Ferdowsi, M.; Shamshi, P. A Family of Scalable Non-Isolated Interleaved DC-DC Boost Converters with Voltage Multiplier Cells. *IEEE Access* **2019**, *7*, 11707–11721. [CrossRef]

20. Meraj, M.; Bhaskar, M.S.; Iqbal, A.; Al-Emadi, N.; Rahman, S. Interleaved Multilevel Boost Converter with Minimal Voltage Multiplier Components for High-Voltage Step-Up Applications. *IEEE Trans. Power Electron.* **2020**, *35*, 12816–12833. [CrossRef]

21. Pan, C.; Chuang, C.; Chu, C. A Novel Transformer-less Adaptable Voltage Quadrupler DC Converter with Low Switch Voltage Stress. *IEEE Trans. Power Electron.* **2014**, *29*, 4787–4796. [CrossRef]

22. Padmavathi, P.; Natarajan, S. Single switch quasi Z-source based high voltage gain DC-DC converter. *Int. Trans. Electr. Energy Syst.* **2020**, *30*, 1–25. [CrossRef]

23. Meinagh, F.A.A.; Yuan, J.; Yang, Y. Analysis and design of a high voltage-gain quasi-Z-source DC–DC converter. *IET Power Electron.* **2020**, *13*, 1837–1847. [CrossRef]

24. Martinez, W.; Cortes, C.; Yamamoto, M.; Imaoka, J. Effect of inductor parasitic resistances on the voltage gain of high step-up DC–DC converters for electric vehicle applications. *IET Power Electron.* **2018**, *11*, 1628–1639. [CrossRef]

25. Ahmad, J.; Zaid, M.; Sarwar, A.; Lin, C.-H.; Asim, M.; Yadav, R.K.; Tariq, M.; Satpathi, K.; Alamri, B. A New High-Gain DC-DC Converter with Continuous Input Current for DC Microgrid Applications. *Energies* **2021**, *14*, 2629. [CrossRef]

26. Ahmad, J.; Zaid, M.; Sarwar, A.; Tariq, M.; Sarwer, Z. A New Transformerless Quadratic Boost Converter with High Voltage Gain. *Smart Sci.* **2020**, *8*, 1–21. [CrossRef]

27. Jalilzadeh, T.; Rostami, N.; Babaei, E.; Maalandish, M. Non-Isolated Topology for High Step-Up DC-DC Converters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *3*, 309–320. [CrossRef]

28. Hu, D.; Yin, A.; Ghaderi, D. A transformer-less single-switch boost converter with high-voltage gain and mitigated-voltage stress applicable for photovoltaic utilisations. *Int. Trans. Electr. Energy Syst.* **2020**, *30*, 1–22. [CrossRef]

29. Zaid, M.; Ahmad, J.; Sarwar, A.; Sarwer, Z.; Tariq, M.; Alam, A. A Transformer less Quadratic Boost High Gain DC-DC Converter. In Proceedings of the 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, 16–19 December 2020; pp. 1–6. [CrossRef]

30. Babaei, E.; Maheri, H.M.; Sabahi, M.; Hosseini, S.H. Extendable Nonisolated High Gain DC-DC Converter Based on Active-Passive Inductor Cells. *IEEE Trans. Ind. Electron.* **2018**, *65*, 9478–9487. [CrossRef]

31. Mahmood, A.; Zaid, M.; Ahmad, J.; Khan, M.A.; Khan, S.; Sifat, Z.; Lin, C.-H.; Sarwar, A.; Tariq, M.; Alamri, B. A Non-Inverting High Gain DC-DC Converter with Continuous Input Current. *IEEE Access* **2021**, *9*, 54710–54721. [CrossRef]