Analysis of SET pulses propagation probabilities in sequential circuits

Shuo Cai, Fei Yu and Yiqun Yang
1 School of Computer and Communication Engineering, Changsha University of Science and Technology, Changsha 410114, China
2 Hunan Provincial Key Laboratory of Intelligent Processing of Big Data on Transportation, Changsha University of Science and Technology, Changsha 410114, China
caishuo@csust.edu.cn

Abstract. As the feature size of CMOS transistors scales down, single event transient (SET) has been an important consideration in designing logic circuits. Many researches have been done in analyzing the impact of SET. However, it is difficult to consider numerous factors. We present a new approach for analyzing the SET pulses propagation probabilities (SPPs). It considers all masking effects and uses SET pulses propagation probabilities matrices (SPPMs) to represent the SPPs in current cycle. Based on the matrix union operations, the SPPs in consecutive cycles can be calculated. Experimental results show that our approach is practicable and efficient.

1. Introduction
Due to the reduction in device feature size, transient faults in logic circuits induced by radiations increase dramatically. Transient faults can be categorized into SETs and single event upsets (SEUs) [1, 2]. As technology feature size shrinks, reduced supply voltage and increased frequency result in more SETs being propagated to latches or primary outputs of circuits and creates more failures than before [3, 4]. Sequential circuit elements, namely logic gates (GTs) and flip-flops (FFs), are most susceptible to transient faults [5]. One common approach to analyze the impact of SETs is to inject the pulses at given nodes and simulate the circuit for different input vectors so as to find whether the SET pulses propagate [6]. Nevertheless, it becomes intractable for large circuits and large number of inputs. On the contrast, another type of approaches use the signal probability theory to analyze the SPPs [7]. The computational complexity of these approaches is lower but its accuracy is compromised because the influence of signal correlations have not been considered. Furthermore, above both kinds of approaches usually fail to include at least one of the following: 1) considering all masking effects (logical, electrical and latching-window masking effects). 2) being suitable for sequential circuits working in consecutive cycles. Therefore, better approaches that use concise mathematical tools and reasonable method are required to analyze the SPPs. In this paper, we present a new approach for analyzing the SPPs in sequential logic circuits. The SPPs of gates and flip-flops in current cycle are represented with SPPMs, then the SPPs in consecutive cycles are calculated by matrix union operation. On the basis of this, the SETs’ influence on the soft error rate (SER) and reliability of circuit can be evaluated efficiently.
2. SET pulses propagation probability matrices

SET pulses can be directly propagated to primary outputs (POs) and cause the circuit failure currently, or they can be propagated to flip-flops repeatedly, and finally appear as failure on POs several cycles later. Our definitions refer to the synchronous sequential logic circuit which consists of m logic gates and n flip-flops.

**Definition 1.** SPPM\(_{GT,PO}\) is defined as a \(m\times1\) column vector \([P(PO|GT_1) \ P(PO|GT_2) ... P(PO|GT_m)]^T\), where \(P(PO|GT_i)\) is the average probability of the SET pulse propagated from error site \(GT_i\) to POs at current cycle.

We use \(\alpha, \beta\) and \(\gamma\) to represent logical, electrical and latching-window propagation factor of SET pulse respectively. \(\alpha_{GT,PO}^{(i)}\) means the SPP from \(GT_i\) to POs avoiding logical masking effect under the stimulus of input vector \(V_a\). Obviously, the value of \(\alpha_{GT,PO}^{(i)}\) is either 0 or 1. If it is 1, then mark all the sensitive paths from \(GT_i\) to reachable POs under the stimulus of \(V_a\) and find out the shortest one (labeled as \(S_{path}\)). If the SET pulse is electrical masked through \(S_{path}\), then the value of \(\beta_{GT,PO}^{(i)}\) is 0, otherwise, \(\beta_{GT,PO}^{(i)}\) is 1. Based on this, \(P(PO|GT_i)\) can be computed as

\[
P(PO|GT_i) = \sum_{k=1}^{n} \alpha_{GT,PO}^{(i)} \beta_{GT,PO}^{(i)}\]

where \(k\) is the number of applied input vectors.

**Definition 2.** SPPM\(_{GT,FF}\) is defined as a \(m\times n\) matrix

\[
\begin{bmatrix}
P(FF_1|GT_1) & ... & P(FF_1|GT_m) \\
... & ... & ... \\
... & ... & ... \\
... & ... & ... \\
P(FF_n|GT_1) & ... & P(FF_n|GT_m)
\end{bmatrix},
\]

where \(P(FF_j|GT_i)\) is the average probability of the SET pulse propagated from error site \(GT_i\) to \(FF_j\) at current cycle.

We use \(\alpha_{GT,FF}^{(i,j)}\), \(\beta_{GT,FF}^{(i,j)}\) and \(\gamma_{GT,FF}^{(i,j)}\) to represent the SPP from \(GT_i\) to \(FF_j\) avoiding logical, electrical and latching-window masking effects under the stimulus of input vector \(V_a\) respectively. If \(\alpha_{GT,FF}^{(i,j)}\) and \(\beta_{GT,FF}^{(i,j)}\) are both 1, then update the width of SET pulse and calculate \(\gamma_{GT,FF}^{(i,j)}\) further. The matrix element \(P(FF_j|GT_i)\) can be expressed as

\[
P(FF_j|GT_i) = \sum_{k=1}^{n} \alpha_{GT,FF}^{(i,j)} \beta_{GT,FF}^{(i,j)} \gamma_{GT,FF}^{(i,j)}
\]

**Definition 3.** SPPM\(_{FF,FF}\) is defined as a \(n\times n\) matrix

\[
\begin{bmatrix}
P(FF_1|FF_1) & ... & P(FF_1|FF_n) \\
... & ... & ... \\
... & ... & ... \\
... & ... & ... \\
P(FF_n|FF_1) & ... & P(FF_n|FF_n)
\end{bmatrix},
\]

where \(P(FF_j|FF_i)\) is the average probability of the SET pulse propagated from error site \(FF_i\) to \(FF_j\) at current cycle. By considering three masking effects, \(P(FF_j|FF_i)\) can be expressed as

\[
P(FF_j|FF_i) = \sum_{k=1}^{n} \alpha_{FF,FF}^{(i,j)} \beta_{FF,FF}^{(i,j)} \gamma_{FF,FF}^{(i,j)}
\]

We also define \(SPPM^{*}_{FF,FF}\) as

\[
\begin{bmatrix}
P^*(FF_1|FF_1) & ... & P^*(FF_1|FF_n) \\
... & ... & ... \\
... & ... & ... \\
... & ... & ... \\
P^*(FF_n|FF_1) & ... & P^*(FF_n|FF_n)
\end{bmatrix},
\]

where \(P^*(FF_j|FF_i)\) is the probability of the pulse latched by \(FF_j\) propagated from \(FF_i\) to \(FF_j\) and latched by \(FF_j\) at next cycle. Here, \(\beta\) and \(\gamma\) are different from Eq.(3) because of the variation of initial SET pulse width. More specifically, the pulse width has been changed to a complete clock cycle. The expression can be written as

\[
P^*(FF_j|FF_i) = \sum_{k=1}^{n} \alpha_{FF,FF}^{(i,j)} \beta_{FF,FF}^{(i,j)} \gamma_{FF,FF}^{(i,j)}
\]

**Definition 4.** SPPM\(_{FF,PO}\) is defined as a \(n\times1\) column vector \([P(PO|FF_1) \ P(PO|FF_2) ... P(PO|FF_n)]^T\), where \(P(PO|FF_i)\) is the average probability of the SET pulse propagated from \(FF_i\) to POs at current cycle. It can be achieved as
\[ P(PO|FF) = \sum_{k=1}^{K} \alpha_{V_{k}} \beta_{V_{k}} \]

We define SPPM* as \([P^*(PO|FF_1) \quad P^*(PO|FF_2) \quad \ldots \quad P^*(PO|FF_n)]^T\), where \(P^*(PO|FF_i)\) is the probability of the pulse latched by FFₐ propagated from FF to POs at next cycle, and \(P^*(PO|FF)\) can be written as

\[ P^*(PO|FF) = \sum_{k=1}^{K} \alpha_{V_{k}} \beta_{V_{k}} \]

The above SPPMs can be obtained in advance. To obtain \(\alpha\) in Eq.(1-6), a simulation-based method is adopted. This method injects SET pulse per each node respectively and applies certain vector randomly. Afterwards, \(\alpha\) can be computed by simulating the circuit and comparing the logical values to the correct ones of POs or specific FF. For a specific SET pulse, if its corresponding \(\alpha \neq 1(\alpha = 1, \ldots, k)\), then find out the shortest path from all sensitive paths between fault site to reachable PO or FF under the stimulus of \(V_a\). (If the pulse can be electrical masked through the shortest path, it can be also be electrical masked through any other sensitive paths). For a gate delay of \(D_{GT}\) and pulse width of \(W_p\) at the gate input, pulse width at the output of the gate, \(W_{po}\), can be approximated as [8]

\[ W_{po} = \begin{cases} 0, & W_p < D_{GT} \\ 2(W_p - D_{GT}), & D_{GT} \leq W_p < 2D_{GT} \\ W_p, & W_p \geq 2D_{GT} \end{cases} \]

For a given SET pulse, if \(\alpha \neq 0\) and \(\beta \neq 0\) are both equal to 1, \(\gamma\) can be evaluated by Eq.(8). Here, \(T_c\) is the clock period, \(T_{setup}\) and \(T_{hold}\) are the setup time and hold time of the latching flop-flop respectively [9]. Given \(W_{po}, D_{GT}, T_{setup}, T_{hold}\) and \(T_c\), the elements of SPPMs can be obtained by applying \(k\) test vectors and using Eq. (1-8).

\[ \gamma = \begin{cases} 0, & W_{po} < T_{setup} + T_{hold} \\ \frac{W_{po} - (T_{setup} + T_{hold})}{T_c}, & W_{po} \geq T_{setup} + T_{hold} \end{cases} \]

Besides that, based on Eq. (7-8), we find that \(\beta^*\) and \(\gamma^*\) are approximated 1 when the clock frequency is lower than 20GHz. Therefore, Eq. (4) and Eq. (6) can be simplified into \(P^*(FF_i|FF) = \sum_{k=1}^{K} \alpha_{V_{k}} \beta_{V_{k}} \) respectively.

3. SPPs analysis in consecutive clock cycles

**Definition 5.** The operator of matrix union operation is expressed as “∪”. If the number of columns of matrix \(M\) is equal to the number of rows of matrix \(N\), then the matrix union operation can be described as follows:

\[ M_{\text{rxd}} = \begin{bmatrix} m_{11} & \ldots & m_{1r} \\ \vdots & \ddots & \vdots \\ m_{r1} & \ldots & m_{rr} \end{bmatrix}, \quad N_{\text{xst}} = \begin{bmatrix} n_{11} & \ldots & n_{1i} \\ \vdots & \ddots & \vdots \\ n_{si} & \ldots & n_{st} \end{bmatrix}, \quad M_{\text{rxd}} \cup N_{\text{xst}} = \begin{bmatrix} l_{11} & \ldots & l_{1i} \\ \vdots & \ddots & \vdots \\ l_{si} & \ldots & l_{st} \end{bmatrix}, \quad \text{where} \quad 0 \leq m_{ij}, n_{ij} \leq 1 \quad (m_{ij} \in M, n_{ij} \in N) \quad \text{and} \quad l_{ij} = 1 - \prod_{k=1}^{l} (1 - m_{ik} n_{ik}), (1 \leq i \leq r, 1 \leq j \leq t) \]

**Definition 6.** The matrix exponentiation operation based on union operation is described as follows:

\[ M^c = M \cup M \cup \ldots \cup M \] (the number of \(M\) is \(c\)).

**Theorem 1.** The probability of a circuit failure at \(c\)th cycle given a SET occurs at \(GT_i\) (the time for pulse occurring is 1st cycle), \(P^i(PO|GT)\), is described as:

\[ P^i(PO|GT) = \begin{cases} \text{Row}_c((\text{SPPM}_{GT,PO})) & c = 1 \\ \text{Row}_c(\text{SPPM}_{GT,FF} \cup (\text{SPPM}_{FF,FF})^2 \cup \text{SPPM}_{FF,PO}) & c \geq 2 \end{cases} \]

**Proof.** Here, we consider that the fault propagation to FFs are approximately independent. If \(c = 1\), \(P^i(PO|GT) = i\)th row of \(\text{SPPM}_{GT,PO}\); If \(c = 2\), assume that a SET pulse occurs at \(GT\) at 1st cycle, which can be propagated to any flip-flop (e.g. FF) at current cycle, and then propagated from FF to POs at
next cycle. That is: 

\[ P^c(PO|GT_c) = 1 - \prod_{j=1}^{m}(1 - P(FF_j|GT_c)P^c(PO|FF_j)) = i^{th}\text{ row of } (SPPM_{FF,FF}^c \cup SPPM_{FF,PO}^c). \]

The SET pulse can also be propagated to FF\(_j\) currently, then propagated to FF\(_k\) after one cycle, and to POs after two cycles. Assume \( P^c(FF_j|GT_c) \) is the probability that the SET pulse is propagated to FF\(_j\) one cycle after the pulse occurs given that GT\(_c\) is erroneous, and it is the \( i^{th}\) row, \( j^{th}\) column element of \((SPPM_{FF,FF}^c \cup SPPM_{FF,PO}^c)\). Additionally, \( P^c(PO|GT_c) = i^{th}\text{ row of } (SPPM_{GT,FF}^c \cup (SPPM_{GT,FF}^c)^7 \cup SPPM_{FF,PO}^c). \)

Similarly, \( P^c(FF_j|GT_c) \) is the probability that the SET pulse is propagated to FF\(_j\) two cycles after the pulse occurs given that GT\(_c\) is erroneous. Based on the induction, \( P^c(PO|GT_c) \) is \( i^{th}\) row of \((SPPM_{GT,FF}^c \cup (SPPM_{FF,FF}^c)^{c-2} \cup SPPM_{FF,PO}^c). \)

**Theorem 2.** The probability of a circuit failure at \( c^{th}\) cycle given a SET occurs at FF\(_j\) (the time for pulse occurring is \( 1^{st}\) cycle), \( P^c(PO|FF_j) \), is described as:

\[
P^c(PO|FF_j) = \begin{cases} 
\text{Row}_{i}(SPPM_{FF,PO}^c), & c = 1 \\
\text{Row}_{i}(SPPM_{FF,FF}^c \cup (SPPM_{FF,FF}^c)^{c-1} \cup SPPM_{FF,PO}^c), & c \geq 2 
\end{cases}
\]  

(10)

The proving process is similar to that of Theorem 1.

4. Experimental results

Experimental results in the ISCAS’89 circuits are given in this section. We use NANGATE 45-nm technology models to compute the SPPs [10]. \( V_{DD} \) is 1.0V, \( T_s \) is 1ns, \( D_{GT} \) is 20ps, \( T_{d}(T_{setup} + T_{hold}) \) is 30ps. All experiments have been performed on the system equipped with Intel i3-3110M processor and 4GB memory.

![Figure 1. SPPs (GT-FFs at current cycle) with different masking effect considering](image)

Figure 1 shows the average SPPs from GT to FFs of S27 when \( W_{pi} \) is 35ps at current cycle. LME, EME and WME represent the logical, electrical and latching-window masking effect respectively. If \( W_{pi} \) changes, the SPPs will change accordingly. Figure 2 shows the average SPPs from GT to FFs of S27 at current cycle with different \( W_{pi} \) when considering all masking effects.

![Figure 2. SPPs (GT-FFs at current cycle) with different \( W_{pi} \) considering all masking effects](image)

Based on our theorems, we have found the average SPPs from GT (FF) to POs will converge with clock cycles extend. Figure 3 shows the average SPPs and corresponding calculation times of some ISCAS’89 circuits in consecutive cycles when \( W_{pi} \) is 100ps. Figure 4 shows the number of applied vectors to circuits in our experiments and their convergence cycles. Note that the right Y-axis in Figure 3 and left Y-axis in Figure 4 are logarithmic.
The accuracy of our approach is more than 99.4% compared with Monte Carlo simulation techniques, while its run time is 2 to 3 order magnitudes shorter than that of the latter for experimental circuits[6]. For a sequential circuit with amounts of $m$ gates and $n$ flip-flops, assume the number of applied input vectors is $k$. In Monte Carlo simulation, the total number of input vectors is $k'$ when considering the SET pulse propagation during $c$ clock cycles [7, 11]. For a specified SET pulse, the simulation feeds all $k'$ input vectors and traverses $(m+n)$ elements for each vector to get the result. Therefore, the computational complexity of Monte Carlo simulation is $O(k' \times (m+n))$. For proposed approach, the SPPs in sequential circuit is obtained by unioning an $n \times n$ matrix $c$ times. So the computational complexity of our approach is $O(c \times n^2)$. It can be seen that the acceleration of our approach will increase with the continuation of clock cycles for larger circuits.

5. Conclusions
In this paper, we have proposed a new SPPs analysis approach in sequential circuits. The approach has two main features: 1) all masking effects that affect the SPPs are considered; 2) the SPPs can be calculated in consecutive cycles efficiently based on SPPMs. These two features make our approach applicable to the reliability evaluation of circuits.

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