Manipulation of random telegraph signals in a silicon nanowire transistor with a triple gate

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Abstract
Manipulation of carrier densities at the single electron level is inevitable in modern silicon based transistors to ensure reliable circuit operation with sufficiently low threshold-voltage variations. However, previous methods required statistical analysis to identify devices which exhibit random telegraph signals (RTSs), caused by trapping and de-trapping of a single electron. Here, we show that we can deliberately introduce an RTS in a silicon nanowire transistor, with its probability distribution perfectly controlled by a triple gate. A quantum dot (QD) was electrically defined in a silicon nanowire transistor with a triple gate, and an RTS was observed when two barrier gates were negatively biased to form potential barriers, while the entire nanowire channel was weakly inverted by the top gate. We could successfully derive the energy levels in the QD from the quantum mechanical probability distributions and the average lifetimes of RTSs. This study reveals that we can manipulate individual electrons electrically, even at room temperature, and paves the way to use a charged state for quantum technologies in the future.

Keywords: random telegraph signal, silicon nanowire, quantum dot, MOSFET

1. Introduction
A random telegraph signal (RTS) [1–5] is a phenomenon whereby a single carrier is randomly trapped and detrapped in a charge trap so that the output signal of electronic devices, such as metal-oxide-semiconductor field-effect transistors (MOSFETs) or complementary metal-oxide-semiconductor (CMOS) image sensors, show undesirable discrete features over time. In MOSFETs, for example, drain current ($I_d$) shows two discrete levels at a given voltage condition [3–5]. These variations over time impose significant constrains on circuit designs, especially for static random access memory [6, 7] and flash memories [4, 8–12], since an RTS induces threshold-voltage ($V_{th}$) shifts and it directly affects bit error rates for the read/write cycles. Floating gate multilevel flash memory will be the first digital devices to be significantly affected by RTSs in the 45 nm node and beyond [13]. In CMOS circuits beyond the 14 nm technology node, variations in performance are considered to be dominated by RTSs over the random dopant fluctuation [14, 15]. RTSs are believed to be the dominant source of the noise over shot noise [16] up to a clock speed of 100 GHz [17].
Conventionally, the main method of studying RTSs is to statistically investigate a large number of devices in order to find a device which shows typical RTS behaviours [6, 7, 11, 13–15, 18]. Analysing the microscopic mechanism of RTSs for trapping and de-trapping leads to the possibility of giving feedback on how to improve the fabrication process, so as to avoid RTSs [18]. Recently, we reported a systematic method to find RTSs without relying on statistical analysis [19]. By measuring single electron transistor characteristics at low temperatures, the bias conditions to observe RTSs in CMOS transistors [19] can be identified, which allows the nature of the trap to be investigated. However, the positions of traps are randomly distributed over the device, making it difficult to control the occupancy of the quantum energy level to show RTSs [19].

Here, we have fabricated a silicon (Si) nanowire transistor to investigate the nature of RTSs in more detail by manipulating the quantum level and the barrier height, which are highly tunable by the triple gates surrounding the nanowire. The device was measured at room temperature and an RTS was observed at certain bias conditions, where the two bottom gates formed potential barriers to create an artificial quantum dot (QD) at the centre of the device. By tuning the quantum level using the top gate (TG), we successfully controlled the occupancy and the lifetimes of the trapped single electron. This means that we can electrically control RTSs, which will be useful to understand the mechanism of single electron trapping and de-trapping to enhance the reliability of nano-electronic devices.

RTSs will also be important for quantum technology in the future [20–34], since the manipulation of a single electron will be beneficial for quantum information processing [35, 36] using charge and spin qubits [37–40]. For quantum metrologies, single electron pumps are thought to be candidates to realise a new definition of the Ampere based on fundamental physical constants such as elementary charge [20–34]. It has already been reported that an interface trap level could be used as a QD for a single electron pump to allow stable current operation [29, 33]. In order to guarantee the high precision required to realise the new definition of the unit, RTSs must be avoided and the mechanism for trapping and de-trapping must be well understood. Our analysis shows that there exists certain bias conditions to avoid RTSs, so that the optimisation of waveforms will improve the future performance of the single electron pumps [25].

2. Device fabrication

A Si nanowire was patterned by electron beam (E-beam) lithography on a si-on-insulator (SOI) wafer with 145 nm thick buried oxide (BOX) (figure 1). The SOI layer was originally 100 nm in thickness and through oxidation was reduced to be 24 nm. The width of the nanowire (W) was 30 nm (figure 1(b)). Anisotropic wet etching was employed to realise an atomically flat interface with Si (111) surfaces to avoid line edge roughness. A 17.6 nm thick thermal oxide ($t_{ox}$) was grown on top of the Si nanowire, resulting in the thickness of the SOI to be 14 nm. Then, an oxide window was opened to raise the source and drain regions (figures 1(a) and (b)) by depositing 100 nm thick polycrystalline-Si (poly-Si) layer using low-pressure-chemical- vapour-deposition. The poly-Si was heavily doped with phosphorous (P) using spin-on-dopant, which was activated at 950 °C by rapid-thermal-annealing. The same poly-Si layer was also used to pattern the first gate (FG) to create the potential barriers in the Si nanowire (figure 1(d)). E-beam lithography and inductively-coupled-plasma etching were employed for the FG patterning (figure 1(c)). Then, the surface of the poly-Si FG was successively oxidised to form 9 nm thick thermal oxide, and the second poly-Si layer was deposited and doped to from the TG in the same way as to form the FG. The gate length of FG ($L_{FG}$) was 75 nm, and the gate lengths of TG ($L_{TG}$) were 125 nm. The passivation oxide layer was formed and an aluminium (Al) layer was used for the final metallisation. H$_2$ sintering was used to terminate the interface traps.

3. Characterisation

All devices were carried out at room temperature using a Keysights B1500A and a Cascade M150 probe station. Our device has three gates (two FGs and one TG), leading to many biasing conditions to be explored when compared with a standard MOSFET. In order to focus on a limited parameter space, we applied the same voltage ($V_{FG}$) between the left and the right FGs (figure 1). Throughout our experiments, we also applied the same voltage between source and drain ($V_d$ = 50 mV). The substrate and the source electrode were grounded, and the gate-leakage currents were always below 200 fA, which was below the detection limit in our measurement.

First, the current–voltage characteristics was measured by sweeping the TG voltage ($V_{TG}$) under a fixed applied $V_{FG}$ and $V_d$ (figure 2(a)). Sweeping the gate voltage is known to be useful as a fast ramped voltage characterisation method [18, 41] to capture the overall features to see RTSs. Standard transfer characteristics of $I_d$ was observed from subthreshold to linear regions by increasing $V_{TG}$. The drain current was reduced upon decreasing $V_{FG}$ as expected, since such $V_{FG}$ limits current flow by creating potential barriers (figure 2(a)). Moreover, we observed unstable $I_d$ fluctuations (figure 2(b)), which corresponds to a shift of $V_{th}$ ($\Delta V_{th}$) of around 5 mV. This is consistent with $\Delta V_{th}$ estimated from single electron charging of the QD, given by $C_{QD} = \epsilon / \Delta V_{th}$, where $\epsilon$ is the elementary charge. $C_{QD} = \epsilon_0 \kappa_{ox} S \mu_{ox}$ is the capacitance of QD, $\epsilon_0$ is dielectric constant of vacuum and $\kappa_{ox} = 3.9$ is the relative dielectric constant of the oxides and $S$ is the area of the QD. $S$ is estimated to be 65 nm in width and 125 nm in length. The width of the nanowire includes the top surface of the nanowire (30 nm wide) as well as its two sidewalls, each of which has 17.5 nm width. Using these values, $\Delta V_{th}$ is calculated as 10 mV, which is in a reasonable agreement with the measurement data considering the uncertainty associated with the physical dimension of the device and the electrical measurement. Also, positive charges in the poly-Si could
Figure 1. Our silicon nanowire transistor with a triple gate. (a) A birds-eye view of the device. TG is not shown. Oxide covering the nanowire is omitted to clarify the structure. (b) Device cross sectional view. (c) A SEM image of a similar device after FG patterning by ICP etching. The actual width of the nanowire is narrower than displayed, as the oxide covers the nanowire in this image. The width of the nanowire (W) is estimated to be 30 nm and the width of the FG (L_{FG}) is 75 nm with the spacing between two FGs (L_{TG}) being 125 nm. (d) Schematic of the energy diagram in the QD, which is discussed in Discussion section. (e) The effective circuit model of the nanowire FET system.

Figure 2. Current–voltage characteristic of the silicon nanowire transistor. (a) The transfer characteristic of TG with \( V_D = 50 \text{ mV} \) and different \( V_{FG} \) values in log scale. (b) Close-up view of the area in the dotted circle in linear scale, with \( V_{FG} = 0 \text{ V} \). (c) The transfer characteristic of FG1 with \( V_D = 50 \text{ mV} \) and \( V_{TG} = V_{FG2} = 0 \text{ mV} \). (d) The transfer characteristic of FG2 with \( V_D = 50 \text{ mV} \) and \( V_{TG} = V_{FG1} = 0 \text{ mV} \).
screen the charge of a trapped electron, leading to the smaller effective charge and hence small $\Delta V_{th}$. Therefore, we believe the observed noise is coming from single electron trapping and de-trapping in a QD, created by the triple gate. To confirm the symmetry of the two FGS, $I_d-V_{TG1}$ and $I_d-V_{TG2}$ characteristic were measured and shown in figures 2(c) and (d). Both of the transistors worked almost identically. Process variations such as misalignment in E-beam lithography and poor patterning may have degraded them or induced asymmetry between two FGSs. However, the $V_{th}$ did not shift significantly and the ON current were in the same order of magnitude. Therefore, we believe the system is symmetry and any asymmetry present in the system is negligible for FG to work as a barrier.

Next, we performed time-domain measurements. All parameters were measured with a time step ($\Delta t$) of 88 ms with constant $V_{FG} = 0$ V and $V_{TG}$ (figure 3). We obtained RTSs at several $V_{TG}$ values, from 0.15 to 0.4 V with a 0.05 V step, allowing the nature of $\Delta V_{th}$ to be identified as an RTS (figures 3(a)–(f)). Using this data, histograms of $I_d$ were made, corresponding to the probability distribution as a function of $I_d$, $P = P(I_d) = |\psi_{QD}|^2$, where $\psi_{QD}$ is the wavefunction [19] of the QD (figures 3(g)–(l)). At each bias condition (e.g., figure 3(c)), two peaks were clearly visible in the probability distributions (e.g., figure 3(i)), and we assigned high and low states for the peaks, corresponding to high and low $I_d$ states. At $V_{TG} = 0.4$ V, the low state is dominant (figure 3(g)), while the high state becomes dominant as $V_{TG} = 0.15$ V (figure 3(l)), meaning that the distribution of the two current states is controlled by $V_{TG}$. At a higher voltage of $V_{TG} = 0.4$ V, the energy level of the QD should be well below the Fermi energy of source, $E_s$, meaning that the energy level must be predominantly occupied. Then, we expect positive $\Delta V_{th}$, which results in the reduction of $I_d$ under the constant $V_{TG}$, and therefore, the low state dominated. On the other hand, at lower voltage of $V_{TG} = 0.15$ V, the energy level of the QD is well above $E_s$, so that the QD cannot be occupied. From this, we expect no $\Delta V_{th}$, so that the $I_d$ is higher than the state with trapped electron in the QD (figure 3(l)). This argument is discussed in more detail in Discussion section. We confirmed the systematic trend of the change of the occupancy in the QD, controlled by $V_{TG}$ (figure 3(m)). The occupancy of the high state and the low states are given by

$$n_{High} = \frac{1}{I_T} \int_{I_{th}}^{\infty} P(I_d) dI_d,$$

$$n_{Low} = \frac{1}{I_T} \int_{-\infty}^{I_{th}} P(I_d) dI_d,$$

where $I_{th}$ is the local minimum of the probability distribution function between the two peaks, which was accurately calculated by an average of the $I_d$ values that give the maxima of the high state ($I_{th,h}$) and the low state ($I_{th,l}$) ($I_{th} = (I_{th,h} + I_{th,l})/2$), and $I_T = \int_{-\infty}^{\infty} P(I_d) dI_d$ is the normalising factor. In other words, we are observing the single electron states of the QD, through measuring $I_d$, and the state is highly tunable electrically.

Lastly, in order to investigate how the occupancy of QD depends on $V_{FG}$, $V_{TG}$ is fixed to 50 mV and $V_{FG}$ was swept from −1.6 to 0.4 V with a 0.2 V step. The result is shown in

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**Figure 3.** Random telegraph signals of the silicon nanowire transistor controlled by the energy level of the QD. $V_{TG}$: (a)–(f) Results of time-domain measurement, under application of $V_{FG} = 0$ V and $V_{TG} = 0.40$ V (a) to 0.15 V (f) with a 50 mV step. X-axis is time (t) and y-axis is $I_d$ in unit of nA. The total measurement time was 480 s and the first 100 s are shown. The sampling interval was 88 ms. (g)–(l) The probability distributions of the corresponding time domain characteristic, displaying the probability to find $I_d$ to be at a certain value. In each graph, $I_{th,m}$ is defined as the local minimum of the distribution function. (m) The occupation of two current states, high and low. (n)–(p) Schematics of the energy diagram. (n) Corresponds to $V_{TG} = 0.35$ and 0.40 V, (o) is for $V_{TG} = 0.25$ and 0.30 V and (p) is for $V_{TG} = 0.15$ and 0.20 V.
figure 6(a) and it can be seen that at $V_{FG} = -1.6, -1.4, -1.2, -1.0 \text{ V}$, an RTS with a long lifetime of around 20 s was observed (RTS1). However, at $V_{FG} = -0.8 \text{ V}$, RTSs were not observed and at $V_{FG} = -0.6, -0.4, -0.2, 0 \text{ V}$ another RTS with shorter lifetime appeared, which is similar to the one observed when $V_{TG}$ was swept (RTS2). Figures 6(b)–(e) show the probability distributions at $V_{TG} = -1.4, -0.8, -0.4, 0.4 \text{ V}$. At $V_{FG} = -1.4 \text{ V}$ due to RTS1 the distribution has two peaks (figure 6(e)), and after $V_{FG}$ was increased up to $-0.8 \text{ V}$ (figure 6(d)), it shows only a single peak since no RTS was observed. However, the distribution shows two peaks again when $V_{FG}$ was increased to $-0.4 \text{ V}$ (figure 6(c)) due to RTS2, and disappeared at $V_{FG} = 0.4 \text{ V}$. We can attribute this appearance and disappearance of multiple RTSs to the presence of multiple energy level in the QD.

The reason why we observed RTSs while $V_{FG}$ was swept is considered to be a weak coupling of FG to the QD, although the capacitance between TG and the QD is the dominant capacitance in the equivalent circuit of our device. An equivalent circuit model of our system is shown in figure 1(e). Two FGs are modelled as transistors with coupling capacitances to the QD ($C_{FG1}$ and $C_{FG2}$), and TG is simply modelled as a capacitance coupled to the dot ($C_{QD}$). The main role of TG is assumed to change the energy level in the QD, while FG is presumed to govern the potential profile. There should also be an accompanying coupling from TG to the potential profile and one from FG to the energy level in the QD. The strength of the capacitive coupling can be evaluated from the width of the voltage window to observe the transition from appearance of the RTS to disappearance of the RTS. In figure 3, the RTS starts to appear at $V_{FG} = 0.15 \text{ V}$ and almost disappears at $V_{FG} = 0.40 \text{ V}$, meaning that the voltage window to observe one energy level in the QD is 0.25 V. However, in figure 6(a), the RTS starts to appear at $V_{FG} = -0.4 \text{ V}$ and almost disappears at $V_{FG} = 0.4 \text{ V}$, meaning that the voltage window to observe one energy level in the QD is 0.8 V. This means that the coupling between FG and QD is weak compared to TG and QD. Therefore, it is safe to say that $C_{QD}$ plays the dominant role in the circuit among the other capacitive components.

### 4. Discussion

Clearly, the occupancy of the energy level in the QD is well controlled by the application of TG. While $n_{High}$ and $n_{Low}$ gives a static picture of the single electron state in the QD (how likely one will find $I_d$ to be in the high state or the low state in a given amount of time), the stability of each current state (how long one state can persist before transitioning to the other) is also important, because this can give a dynamic picture of the trapping and de-trapping process in the QD. Appropriate parameters to evaluate the stability are the average lifetimes of two current states (see figure 3(a))

$$\tau_{High} = \frac{T_{High}}{N_{High}},$$

$$\tau_{Low} = \frac{T_{Low}}{N_{Low}},$$

where $T_{High}$ ($T_{Low}$) is the total time for observing the high (low) state in the total measurement time of $T_{Total} = 480 \text{ s} = N_{Total} \Delta t$ over the total number of sampling events of $N_{Total} = 5459$. $N_{High}$ ($N_{Low}$) is the total number of transitions observed from high to low (from low to high). $T_{High}$ and $T_{Low}$ are obtained by

$$T_{High} = n_{High} T_{Total},$$

$$T_{Low} = n_{Low} T_{Total},$$

To extract $N_{High}$ and $N_{Low}$, we need to make differential histograms, which display the difference in $I_d$ values ($\Delta I_d(t) = I_d(t) + \Delta t - I_d(t)$) for a given time ($t$) over the measurement time interval of $\Delta t$. To focus on the transition between the high state and the low state only, any $[\Delta I_d(t)]$ that is more than 2($I_{d,High} - I_{d,Low}$) is neglected in the following analysis.

Figure 4 shows an example of the differential histogram at $V_{FG} = 0 \text{ V}$ and $V_{TG} = 0.3 \text{ V}$. When the transition from the high state to the low state occurs, $\Delta I_d$ is negative. When the opposite transition happens, $\Delta I_d$ is positive. The histogram has three peaks; one main peak at $\Delta I_d = 0 \text{ nA}$ shows no transition (named as Peak-o), one sub-peak at positive $\Delta I_d$ corresponds to the transition from the low to the high (Peak-p) and the other sub-peak at negative $\Delta I_d$ corresponds to the transition from the high to the low (Peak-n). The integration of these sub-peaks gives

$$N_{High} = \frac{N_{Total}}{\Delta I_d} \int_{-\infty}^{\Delta I_d} P(\Delta I_d) d\Delta I_d,$$

$$N_{Low} = \frac{N_{Total}}{\Delta I_d} \int_{\Delta I_d}^{\infty} P(\Delta I_d) d\Delta I_d,$$
where $P(\Delta I_d)$ is the probability distribution of $\Delta I_d$, $\Delta I_{d,n} = (I_{d,1} - I_{d,h})/2$ is the positive edge of Peak-n, $\Delta I_{d,p} = (I_{d,h} - I_{d,1})/2$ is the negative edge of Peak-p, and $\Delta f_T = \int_{-\infty}^{\infty} P(\Delta I_d) d\Delta I_d$ is the normalising factor.

We show extracted $\tau_{\text{High}}$ and $\tau_{\text{Low}}$ against $V_{\text{TG}}$ in figure 5. $\tau_{\text{Low}}$ corresponds to the lifetime of an electron trapped in the QD. $\tau_{\text{Low}}$ became larger as $V_{\text{TG}}$ was increased (figure 5(a)), which is consistent with the physical picture that the electron is more likely to occupy the quantum level in the QD. On the contrary, $\tau_{\text{High}}$ corresponds to the time scale for the QD to capture an electron. $\tau_{\text{High}}$ decreased upon increasing $V_{\text{TG}}$ (figure 5(a)), which shows that the quantum level was already occupied by an electron, and Pauli’s exclusion principle prevented another electron occupying it. In figure 5(b), the ratio of the lifetimes $\tau_{\text{High}}/\tau_{\text{Low}}$ is plotted against $V_{\text{TG}}$ in log scale, which shows...
a linear dependence on $V_{TG}$. This suggests that $V_{TG}$ does control the lifetimes of RTSs as well as the statistical properties of RTSs.

The ratio of the lifetimes can also be used to estimate the energy level with respect to Fermi energy of source [42]. According to Boltzmann distribution, the probability for an
electron to surpass the energy barrier, $\Delta E$, is given by

$$P \propto \exp \left(-\frac{\Delta E}{kT}\right).$$

(9)

Therefore, the probabilities for an electron to be trapped/detrapped in the QD are given as follows,

$$\frac{\Delta t}{\tau_{\text{High}}} \propto \exp \left(-\frac{\Delta E - E_s}{kT}\right),$$

(10)

$$\frac{\Delta t}{\tau_{\text{Low}}} \propto \exp \left(-\frac{E - E_s - (e - E_s)}{kT}\right),$$

(11)

where $k$ is the Boltzmann constant, $T$ is temperature of $300$ K, $\Delta E - E_s$ is the energy barrier controlled by $V_{\text{FG}}$ and $\tau_{\text{High}}$ and $\tau_{\text{Low}}$ are the lifetimes of the QD, both with respect to the Fermi energy of source, $E_s$. From these, we reach a formula to calculate the energy level in the QD:

$$\epsilon - E_s = kT \ln \left(\frac{\tau_{\text{High}}}{\tau_{\text{Low}}}\right).$$

(12)

This equation means that, if the simple model stated above holds, the energy level of the QD can be evaluated from the ratio of the lifetimes of RTSs. In figure 7(a), $\epsilon - E_s$ against $V_{\text{FG}}$ is plotted, showing the energy level at certain $V_{\text{FG}}$ values. We set $E_s = 0$ meV for simplicity. As can be seen, the energy level linearly decreased as $V_{\text{FG}}$ was increased. Figures 7(b)–(d) show schematics of energy diagram along the nanowire when the energy level is well above, in line with and well below $E_s$, respectively.

This implies that the RTS is most active when the energy level is aligned to $E_s$. Figure 7(a) is essentially the same figure as figure 5(b) with the only difference being the meaning of the $y$-axis. However, the linear dependence of $\ln(\tau_{\text{High}}/\tau_{\text{Low}})$ against $V_{\text{FG}}$ in figure 5(b) is now clear; the energy level in the QD is linearly controlled by $V_{\text{FG}}$. Our discussion so far states that we also successfully controlled the trapping and de-trapping dynamics of a single electron to the QD by $V_{\text{FG}}$ and the energy level is controlled linearly by $V_{\text{FG}}$.

This discussion can naturally be extended to explain RTS1 and RTS2 in figure 6. RTS1 corresponds to the lowest energy level available in the QD, and it starts to be occupied and cause RTS1 (figures 6(e), (i)). After this ground state has been fully occupied, RTS1 disappears because no energy level is available for RTS (figures 6(d), (h)). When $V_{\text{FG}}$ was decreased further, another energy level starts to appear and cause RTS2 (figures 6(c), (g)). After this energy level was completely occupied, no energy level is available and no RTS was observed (figures 6(b), (f)). RTS1 and RTS2 can be clearly distinguished by the different lifetimes, with RTS1 having a lifetime of more than $20$ s while the other has a lifetime of less than $10$ s.

Using this method, we can successfully calculate the energy separation between two energy levels that are responsible for RTS1 and RTS2 shown in figure 6(a). Since $E_i$ is always used as the origin to measure the energy level in the QD, if there exists two different RTSs, we can estimate the energy level spacing between two levels that cause those RTSs. We employed the same analysis to the result shown in figure 6, and the energy levels against $V_{\text{FG}}$ are shown in figure 7(c).

This energy splitting has been attributed to the quantum confinement along the direction perpendicular to the substrate [45, 46]. The quantum confinement energies in the inversion layers on the Si (100) surface are estimated as

$$E_n^h = \frac{(n + 1)^2}{2m_h} \left(\frac{\pi}{t_o}\right)^2 = E_0^h (n + 1)^2,$$

(13)

$$E_n^l = \frac{(n + 1)^2}{2m_l} \left(\frac{\pi}{t_o}\right)^2 = E_0^l (n + 1)^2,$$

(14)

where $h$ is the Planck constant divided by $2\pi$, $m_h = 0.980m_0$ and $m_l = 0.198m_0$ are the effective masses for heavy and light electrons in conduction band valleys with the mass of an electron in vacuum $m_0$. $t_o$ is the effective thickness of the inversion layer [45–47] and $n \geq 0$ is an integer to describe the number of nodes in the envelop wavefunction along the depth. We found that the lowest energy level responsible for RTS 1 was $E_0^h$, and the next energy level responsible for RTS 2 was $E_0^l$. By assuming linear band bending, we fitted experimental data to obtain $t_o = 1.6$ nm for the energy separation of $E_1^h - E_0^h = 446$ meV. The estimated $t_o$ is in reasonable agreement with the previous study on quantum confinement [45, 46]. $E_0^l$ was estimated to be $141$ meV higher than $E_0^l$, meaning that the valley with the heavy electron mass was dominated as expected for the inversion layer on the Si (100) interface [45, 46].

The physical mechanism of a trapping and de-trapping of single electron in our device was successfully explained by thermal activation processes [18, 42, 48–50]. We did not observe Coulomb blockades at room temperature however, since the estimated charging energy of $5$ meV, given by $E_C = e^2/2C_QD$, is lower than the thermal energy of $26$ meV [51]. We can estimate the barrier height to be $150$ meV from figures 7(a)–(c). At $V_{\text{FG}} = 0.15$ V, the ground state was vaguely formed by TG inverting the channel (figure 7(b)). This means that the bottom of the potential profile is slightly lower than the height of the barrier. At $V_{\text{FG}} = 0.3$ V, the ground state was in line with $E_s$, meaning that the bottom of the potential profile is lower than $E_s$.

5. Conclusion

In summary, we have investigated RTSs in a silicon nanowire transistor with a triple gate. We obtained the probability distribution functions by analysing drain current fluctuations in the time domain, and demonstrated that we can control the occupancy of the single electron energy level of the electrically defined QD. The transport mechanism of trapping and de-trapping was successfully explained by thermal activation. Furthermore, we showed that RTSs can be a useful spectroscopic technique to investigate the energy structure of a QD.
Our results show that we can control a single electron in a silicon nanowire even at room temperature by field effects. Single electron manipulation will also be important to establish the stable operation of single electron pumps targeting a new definition of the Ampere and it may also pave the way towards quantum computing using silicon based nano-electronics in the future.

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References

[1] Machlup S 1954 Noise in semiconductors: spectrum of a two-parameter random signal J. Appl. Phys. 25 341–3
[2] Uren M, Day D and Kirton M 1985 1/f and random telegraph noise in silicon metal-oxide-semiconductor field-effect transistors Appl. Phys. Lett. 47 1195–7
[3] Hung K K, Ko P K, Hu C and Cheng Y C 1990 Random telegraph noise of deep-submicrometer MOSFETs IEEE Electron Device Lett. 11 90–2
[4] Fukuda K, Shimizu Y, Amemiya K, Kamoshida M and Hu C 2007 Random telegraph noise in flash memories-model and technology scaling IEDM Tech. Dig. (Piscataway, NJ: IEEE) pp 169–72
[5] Grasser T, Reisinger H, Goes W, Aichinger T, Hehenberger P, Wagner P J, Nehiebel M, Franco J and Kaczer B 2009 Switching oxide traps as the missing link between negative bias temperature instability and random telegraph noise IEDM Tech. Dig. (Piscataway, NJ: IEEE) pp 729–32
[6] Tega N, Miki H, Yamaoka M, Kume H, Mine T, Ishida T, Mori Y, Yamada R and Torii K 2008 Impact of threshold voltage fluctuation due to random telegraph noise on scaled-down SRAM Proc. 46th Annual Int. Reliability Physics Symp.-IRPS08 (Piscataway, NJ: IEEE) pp 541–6
[7] Yamaoka M, Miki H, Bansal A, Wu S, Frank D, Leobandung E and Torii K 2011 Evaluation methodology for random telegraph noise effects in sram arrays IEDM Tech. Dig. (Piscataway, NJ: IEEE) pp 745–8
[8] Kurata H, Otsuga K, Kotabe A, Kajiyama S, Osabe T, Sasago Y, Narumi S, Tokami K, Kamohara S and Tsuichya O 2007 Random telegraph signal in flash memory: Its impact on scaling of multilevel flash memory beyond the 90-nm node IEEE J. Solid-State Circuits 42 1362–9
[9] Li S R, Lu Y L R, McMahon W, Lee Y H and Mielke N 2007 RTS and 1/f noise in flash memory Symp. on VLSI Technol. Dig. Tech. Papers (Piscataway, NJ: IEEE) pp 56–7
[10] Ghetti A, Compagnoni C M, Biancardi F, Lacaita A, Beltrami L, Chiavarone L, Spinelli A and Visconti A 2008 Scaling trends for random telegraph noise in deca-nanometer flash memories IEDM Tech. Dig. (Piscataway, NJ: IEEE) pp 835–8
[11] Ghetti A, Compagnoni C M, Spinelli A S and Visconti A 2009 Comprehensive analysis of random telegraph noise instability and its scaling in deca-nanometer flash memories IEEE Trans. Electron Devices 56 1746–52
[12] Ielmini D 2009 Reliability issues and modeling of flash and post-flash memory Microelectron. Eng. 86 1870–5
[13] Tega N, Miki H, Osabe T, Kotabe A, Otsuga K, Kurata H, Kamohara S, Tokami K, Ikeda Y and Yamada R 2006 Anomalously large threshold voltage fluctuation by complex random telegraph signal in floating gate flash memory IEDM Tech. Dig. (Piscataway, NJ: IEEE) pp 218–21
[14] Tega N, Miki H, Pagette F, Frank D, Ray A, Rooks M, Haensch W and Torii K 2009 Increasing threshold voltage variation due to random telegraph noise in FETs as gate lengths scale to 20 nm Symp. on VLSI Technol. Dig. Tech. Papers (Piscataway, NJ: IEEE) pp 50–1
[15] Takeuchi K, Nagumo T, Yokogawa S, Imai K and Hayashi Y 2009 Single-charge-based modeling of transistor characteristics fluctuations based on statistical measurement of RTN amplitude Symp. on VLSI Technol. Dig. Tech. Papers (Piscataway, NJ: IEEE) pp 54–5
[16] Blanter Y M and Büttiker M 2000 Shot noise in mesoscopic conductors Phys. Rep. 336 1–166
[17] Kanioka T, Imai H, Kamakura Y, Ohmori K, Shiraiishi K, Niwa M, Yamada K and Watanabe T 2012 Current fluctuation in sub-nano second regime in gate-all-around nanowire channels studied with ensemble monte carlo/ molecular dynamics simulation IEDM Tech. Dig. (Piscataway, NJ: IEEE) pp 399–402
[18] Simoen E and Claey s C L 2016 Random Telegraph Signals in Semiconductor Devices (Bristol: IOP Publishing)
[19] Li Z, Sotto M, Liu F, Husain M K, Yoshimoto H, Sasago Y, Hisamoto D, Tomita I, Tsuichya Y and Saito S 2018 Random telegraph noise from resonant tunnelling at low temperatures Sci. Rep. 8 250
[20] Ono Y and Takahashi Y 2003 Electron pump by a combined single-electron/field-effect-transistor structure Appl. Phys. Lett. 82 1221–30
[21] Fujiwara N, Nishiguchi K and Ono Y 2008 Nanoamperp charge pump by single-electron ratchet using silicon nanowire metal-oxide-semiconductor field-effect transistor Appl. Phys. Lett. 92 042102
[22] Fujiwara A, Zimmerman N M, Ono Y and Takahashi Y 2004 Current quantization due to single-electron transfer in Siwire charge-coupled devices Appl. Phys. Lett. 84 1323–5
[23] Pekola J P, Vartiainen J J, Mottinen M, Saira O P, Meschke M and Averin D V 2008 Hybrid single-electron transistor as a source of quantized electric current Nat. Phys. 4 120–4
[24] Giblin S, Wright S, Fletcher J, Kataoka M, Pepper M, Janssen T, Ritchie D, Nicoll C, Anderson D and Jones G 2010 An accurate high-speed single-electron quantum dot pump New. J. Phys. 12 073013
[25] Giblin S, Kataoka M, Fletcher J, Lee P, Janssen T, Griffiths J, Jones G, Farrer I and Ritchie D 2012 Towards a quantum representation of the amperes using single electron pumps Nat. Commun. 3 930
[26] Jehl X et al 2013 Hybrid metal-semiconductor electron pump for quantum metrology Phys. Rev. X 3 021012
[27] Connolly M et al 2013 Gigahertz quantized charge pumping in graphene quantum dots Nat. Nanotechnol. 8 417–20
[28] Rossi A, Tanttu T, Tan K Y, Isakka I, Zhao R, Chan K W, Tettamanzi G C, Rogge S, Dzurak A S and Möttönen M 2014 An accurate single-electron pump based on a highly tunable silicon quantum dot Nano Lett. 14 3405–11

[29] Yamahata G, Nishiguchi K and Fujiwara A 2013 Gigahertz single-trap electron pumps in silicon Nat. Commun. 5 5038–5038

[30] Stein F et al 2015 Validation of a quantized-current source with 0.2 ppm uncertainty Appl. Phys. Lett. 107 103501

[31] Bae M H, Ahn Y H, Seo M, Chung Y, Fletcher J, Giblin S, Kataoka M and Kim N 2015 Precision measurement of a potential-profile tunable single-electron pump Metrologia 52 195

[32] Giblin S, Bae M, Kim N, Ahn Y H and Kataoka M 2017 Robust operation of a GaAs tunable barrier electron pump Metrologia 54 299

[33] Yamahata G, Giblin S P, Kataoka M, Karasawa T and Fujiwara A 2017 High-accuracy current generation in the nanoampere regime from a silicon single-trap electron pump Sci. Rep. 7 45137

[34] Zhao R, Rossi A, Giblin S, Fletcher J, Hudson F, Möttönen M, Kataoka M and Dzurak A 2017 Thermal-error regime in high-accuracy gigahertz single-electron pumping Phys. Rev. Appl. 8 044021

[35] Imamog A et al 1999 Quantum information processing using quantum dot spins and cavity QED Phys. Rev. Lett. 83 4204

[36] Zheng S B and Guo G C 2000 Efficient scheme for two-atom entanglement and quantum information processing in cavity QED Phys. Rev. Lett. 85 2392

[37] Xiao M, Martin I, Yablonovitch E and Jiang H 2004 Electrical detection of the spin resonance of a single electron in a silicon field-effect transistor Nature 430 435

[38] Press D, Ladd T D, Zhang B and Yamamoto Y 2008 Complete quantum control of a single quantum dot spin using ultrafast optical pulses Nature 456 218

[39] Kochl W F, Buckley B B, Heremans F J, Calusine G and Awschalom D D 2011 Room temperature coherent control of defect spin qubits in silicon carbide Nature 479 84

[40] Maurand R et al 2016 A cmos silicon spin qubit Nat. Commun. 7 13575

[41] Toledano-Luque M, Degraeve R, Roussel P J, Ragnarsson L Å, Chiarella T, Horiguchi N, Mocuta A and Thean A 2014 Fast ramped voltage characterization of single trap bias and temperature impact on time-dependent Vth variability IEEE Trans. Electron Device 61 3139–44

[42] Nishiguchi K, Ono Y and Fujiwara A 2014 Single-electron thermal noise Nanotechnology 25 275201

[43] Kirton M, Uren M, Collins S, Schulz M, Karmann A and Scheffer K 1989 Individual defects at the si: SiO2 interface Semicond. Sci. Technol. 4 1116

[44] Amarasinghe N V, Çelik-Butler Z and Vasina P 2000 Characterization of oxide traps in 0.15 μm2 mosfets using random telegraph signals Microelectron. Reliab. 40 1875–81

[45] Ando T, Fowler A B and Stern F 1982 Electronic properties of two-dimensional systems Rev. Mod. Phys. 54 437

[46] Saito S I, Torii K, Hiratani M and Onai T 2002 Analytical quantum mechanical model for accumulation capacitance of MOS structures IEEE Electron Device Lett. 23 348–50

[47] Hartstein A and Albert N 1988 Determination of the inversion-layer thickness from capacitance measurements of metal-oxide-semiconductor field-effect transistors with ultrathin oxide layers Phys. Rev. B 38 1235

[48] Nishiguchi K, Ono Y and Fujiwara A 2011 Single-electron counting statistics of shot noise in nanowire Si metal-oxide-semiconductor field-effect transistors Appl. Phys. Lett. 98 193502

[49] Chida K, Nishiguchi K, Yamahata G, Tanaka H and Fujiwara A 2015 Thermal-noise suppression in nanowire Si field-effect transistors by feedback control based on single-electron detection Appl. Phys. Lett. 107 073110

[50] Chida K, Desai S, Nishiguchi K and Fujiwara A 2017 Power generator driven by Maxwell’s demon Nat. Commun. 8 15510

[51] Grabert H and Devoret M H 1992 Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures vol 294 (New York: Springer)