Efficient Construction of a Control Modular Adder on a Carry-Lookahead Adder Using Relative-phase Toffoli Gates

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ABSTRACT Control modular addition is a core arithmetic function, and we must consider the computational cost for actual quantum computers to realize efficient implementation. To achieve a low computational cost in a control modular adder, we focus on minimizing $KQ$, defined by the product of the number of qubits and the depth of the circuit. In this paper, we construct an efficient control modular adder with small $KQ$ by using relative-phase Toffoli gates in two major types of quantum computers: Fault-Tolerant Quantum Computers (FTQ) on the Logical layer and Noisy Intermediate-Scale Quantum Computers (NISQ). We give a more efficient construction compared to Van Meter and Itoh’s, based on a carry-lookahead adder. In FTQ, $T$ gates incur heavy cost due to distillation, which fabricates ancilla for running $T$ gates with high accuracy but consumes a lot of specially prepared ancilla qubits and a lot of time. Thus, we must reduce the number of $T$ gates. We propose a new control modular adder that uses only 20% of the number of $T$ gates of the original. Moreover, when we take distillation into consideration, we find that we minimize $KQ_T$ (the product of the number of qubits and $T$-depth) by running $\Theta\left(\frac{n}{\sqrt{\log n}}\right)$ $T$ gates simultaneously. In NISQ, CNOT gates are the major error source. We propose a new control modular adder that uses only 35% of the number of CNOT gates of the original. Moreover, we show that the $KQ_{\text{CX}}$ (the product of the number of qubits and CNOT-depth) of our circuit is 38% of the original. Thus, we realize an efficient control modular adder, improving prospects for the efficient execution of arithmetic in quantum computers.

INDEX TERMS Carry-lookahead adder, Control Modular adder, Fault-Tolerant Quantum Computers, Noisy Intermediate-Scale Quantum Computers, Shor’s algorithm

I. INTRODUCTION Recently, functional but imperfect quantum computers have emerged, called Noisy Intermediate-Scale Quantum Computers (NISQ) [2], with machines from IBM [3], [4], Google [5], Rigetti [6], IonQ [7], and Honeywell [8] all accessible via the web.

Many researchers have constructed simple quantum circuits for NISQ machines. Researchers at IBM implemented the first $15 = 3 \times 5$ factoring circuit on a liquid NMR machine in 2001 [9]. Since then, researchers have implemented Shor’s algorithm on a variety of machines [10]–[15], though care must be taken not to extrapolate too far from these demonstrations [16]. Researchers have also demonstrated small instances of Grover’s algorithm [17], [18].
However, we cannot realize large-scale quantum computation on NISQ, due to the high error rate. These errors propagate as the calculation proceeds, and we cannot extract the correct result. Thus, we must reduce the error rate in quantum computers. To realize computation with high accuracy, research on Fault-Tolerant Quantum Computers (FTQ) is proceeding [19]–[21].

Jones et al. [22] proposed a method for constructing FTQ as a layered architecture. Specifically, we conduct the accurate computation on the Logical layer, which is achieved using large numbers of physical qubits with errors.

However, $T$ gates impose an additional cost when run on FTQ. By the Gottesman-Knill theorem [23], we can conduct classical simulation of quantum circuits composed only of Clifford gates, but to realize universal quantum computation, we require non-Clifford gates such as a $T$ gate, taking us into a realm that cannot be simulated classically. We achieve high-fidelity $T$ gates by incorporating distillation [24], which requires a lot of logical qubits and a lot of time; research on optimization of distillation is being carried out [25]. In FTQ, we may realize large-scale quantum algorithms such as Shor’s algorithm [26] and Grover’s algorithm [27]. Shor’s algorithm is of particular interest if it can be implemented as Shor’s algorithm [26] and Grover’s algorithm [27]. Shor’s algorithm is particularly interesting if it can be implemented effectively, because it solves the factorization problem or the discrete logarithm problem in polynomial time, breaking the security of current cryptosystems, such as RSA [28] or elliptic curve [29], [30], whose security is based on the factorization problem or the discrete logarithm problem, respectively.

In Shor’s algorithm, the control modular exponentiation step dominates the total cost, leading many researchers to study its construction [31]–[41]. The control modular exponentiation calculates

$$|j\rangle |1\rangle \rightarrow |j\rangle |a^j \mod N\rangle . \tag{1}$$

In eq. (1), $a$, $N$, and $j$ are non-negative integers satisfying $a < N$.

One strategy realizes a control modular exponentiation by the repeated calling of control modular additions. More precisely, this construction is realized by following two steps:

1) Decomposition of a control modular exponentiation into control modular multipliers
2) Decomposition of a control modular multiplier into control modular adders

The first decomposition is based on the following equation where $j$ can be expressed in $n$-bit, namely $j = (j_{n-1} \ldots j_0)_2$:

$$a^j \mod N = \prod_{i=0}^{n-1} (a^{2^i} \mod N)^{j_i} \mod N \tag{2}$$

In eq. (2), $a^j$ is decomposed into $n$-times multiplications, namely $a^{2^i}$. For example, a exponentiation $2^5$ is decomposed into $2^5 = 2^{1011_2} = 2^4 \times 2^1$.

Next, we consider the second decomposition. In quantum computation, a multiplication $ka$ is based on the following operation:

$$|k\rangle |0\rangle \rightarrow |k\rangle |0 + ka\rangle \rightarrow |k - a^{-1}(ka)\rangle |ka\rangle = |0\rangle |ka\rangle \tag{3}$$

The operation of (3) requires an addition by the result of multiplication. This addition can be decomposed as follows, where $a$ and $b$ are non-negative integers less than $N$, and $k$ is a $n$-bit number expressed as $k = (k_{n-1} \ldots k_0)_2$:

$$b + ak \mod N = b + \sum_{l=0}^{n-1} (a2^{k_l} \mod N) \mod N \tag{4}$$

For example, $6 \cdot 5$ is decomposed into $6 \cdot 5 = 6 \cdot (4 + 1) = 6 \cdot 4 + 6 \cdot 1$, because $5 = 101_2 = 4 + 1$.

From the above discussion, a control modular exponentiation is decomposed into control modular adders. Thus, if we reduce the cost of a control modular adder, the total cost of Shor’s algorithm will shrink. In this paper, we focus on the efficient construction of a control modular addition.

A. BACKGROUND

A control modular addition is defined by a control qubit $x$ and $n$-bit numbers $a$, $b$, and $N$. $a$ and $b$ satisfy $0 \leq a, b \leq N - 1$, and $a$ and $N$ are classical numbers. A control modular addition calculates

$$|x\rangle |b\rangle \rightarrow |x\rangle |b + xa \mod N\rangle \tag{5}$$

An overview is shown in Figure 1.

However, the optimal construction of a control modular adder is not obvious. A control modular adder is constructed from simple adders [32], [33], [45], [38]–[41], and there are many kinds of adders [39], [40], [42]–[46]. Previous constructions follow similar overall structure, but differ in detail. We need to determine which combination is the best.

This paper focuses on minimizing KQ [47] to construct a circuit with low execution cost. KQ is defined by the product of the number of qubits and the depth of the circuit. Minimizing KQ benefits both FTQ [22] and NISQ [18]. Much previous research focuses only on depth or the number of qubits, but reducing only one metric improves only one performance. We believe KQ more accurately represents the total resource consumption, especially for deep circuits, capturing the total “qubit-time steps” of a circuit.

FIGURE 1: Overview of a control modular adder. The first register has a single qubit which is used as a control bit. The second register has $n$ qubits which are used to store the result. $a$ and $N$ are $n$-bit classical numbers.
This paper proposes our new circuit based on Van Meter and Itoh’s construction [39], which uses three of Draper et al.’s carry-lookahead adders [43]. Van Meter and Itoh’s construction has small KQ values than the other constructions but has room for further minimization of KQ. For example, Thapliyal et al. [48] proposed a means of minimizing the number of T gates in a carry-lookahead adder by using Gidney’s relative-phase Toffoli gates [45]. Thapliyal et al.’s construction reduces KQ in FTQ, but similar optimization can be applied to NISQ by Maslov’s relative-phase Toffoli gates [49]. Thus, we reduce KQ by applying relative-phase Toffoli gates on the Van Meter-Itoh construction.

B. OUR CONTRIBUTION

In this study, we propose a method for optimizing a control modular adder based on a carry-lookahead adder for both FTQ and NISQ. We apply two-level optimization on the original Van Meter-Itoh construction [39] as in Figure 2.

In first-level optimization, we optimize the construction of a control modular adder (Section III). Specifically, we optimize by focusing on the efficiency of the comparator in a control modular adder (Section IV.A). For example, we reduce KQ by applying relative-phase Toffoli gates [49]. Thus, we need carries to calculate an addition. To calculate the carry C, we employ a carry c_i. Carry c_i is defined as an overflow from the (i-1)-th bit to the i-th bit. In more detail, we define c_i as

\[ c_i = \begin{cases} 0 & \text{if } i = 0 \\ \frac{a_{i-1} + b_{i-1} + c_{i-1}}{2} & \text{otherwise} \end{cases} \]

Then, (a+b)_i, the i-th bit of a + b, is calculated as

\[ (a+b)_i = a_i \oplus b_i \oplus c_i. \]

Thus, we need carries to calculate an addition.

II. PRELIMINARIES

In this paper, we optimize a carry-lookahead adder by replacing Toffoli gates with relative-phase Toffoli gates. To maintain an accurate calculation, we must consider the role of Toffoli gates well. Moreover, we reduce computational costs by decomposing Toffoli gates into single-qubit gates and CNOT gates.

In subsection A, we explain the quantum gate set used in this paper. Next, to clarify the role of Toffoli gates, we review Draper et al.’s carry-lookahead adder [43] briefly in subsection B. We explain T-minimization [48] by using Gidney’s relative-phase Toffoli gates [45] in subsection C. We review the general construction of a control modular adder in subsection D.

A. QUANTUM GATE SET

In this paper, we use the following:

- **Clifford gates**: X gate, Y gate, Z gate, H gate, S gate, CNOT gate
- **non-Clifford gates**: T gate

The CNOT gate is a two-qubit gate, and the others are one-qubit gates. We express X gates as \( \oplus \) in the circuit.

In this paper, we focus on two gates: T and CNOT, which are non-Clifford gates. We explain the calculation of (a+b) when a and b are \( n \)-bit numbers. We express a as \( a_{n-1}a_{n-2} \cdots a_0 \) and b as \( b_{n-1}b_{n-2} \cdots b_0 \), where \( a_i \) and \( b_i \) are 0 or 1. To calculate \( a+b \), we employ a carry \( c_i \). Carry \( c_i \) is defined as an overflow from the (i-1)-th bit to the i-th bit. In more detail, we define \( c_i \) as

\[ c_i = \begin{cases} 0 & \text{if } i = 0 \\ \frac{a_{i-1} + b_{i-1} + c_{i-1}}{2} & \text{otherwise} \end{cases} \]

Then, (a+b)_i, the i-th bit of a + b, is calculated as

\[ (a+b)_i = a_i \oplus b_i \oplus c_i. \]
Now, we give a brief explanation of a carry-lookahead adder. Before calculating an addition, we determine the propagation of a carry from the \( i \)-th bit to the \( j \)-th bit as a function of the following three conditions:

- **propagate**: A carry is propagated from the \( i \)-th bit to the \( j \)-th bit. Namely, \( c_j = c_i \).
- **generate**: A carry is generated in the \( j \)-th bit, namely \( c_j = 1 \), regardless of the value of \( c_i \).
- **kill**: A carry is killed in the \( j \)-th bit, namely \( c_j = 0 \), regardless of the value of \( c_i \).

To calculate the propagation, we define two functions \( p[i, j], g[i, j] \in \{0, 1\} \). \( p[i, j] \) is true when the carry from the \( i \)-th bit to the \( j \)-th bit should be propagated. Similarly, \( g[i, j] \) is true when the carry out at the \( j \)-th bit is independent of the value of the carry in at the \( i \) bit. We do not need a separate function for \( \text{kill} \), as its value can be inferred from \( p \) and \( g \). By using these functions, we can calculate the propagation state over a wider span. Specifically, when \( i < k < j \),

\[
p[i, j] = p[i, k] \land p[k, j],
\]

\[
g[i, j] = g[k, j] \oplus (g[i, k] \land p[k, j]),
\]

where \( \land \) is Boolean AND, and \( \oplus \) is Boolean XOR. By using these properties, we calculate \( c_j = g[0, j] \).

Now, we explain Draper et al.’s carry-lookahead adder for \( |a⟩ |b⟩ \rightarrow |a⟩ |b + a⟩ \). This requires an additional \( n \) qubits for the carry register \( |c⟩ \) and \( n \) qubits for register \( |p⟩ \), containing \( p[i, j] \). Thus, a carry-lookahead adder requires \( 4n \) qubits.

Now, we explain the implementation briefly. This implementation consists of five phases: Initialization, P-rounds, G-rounds, C-rounds, and inverse P-rounds. In each round,

- **Initialization**: we calculate \( g[i, i + 1] \) in \( |c_{i+1}⟩ \) and \( p[i, i + 1] \) in \( |b⟩ \),
- **P-rounds**: we calculate the \( p \)-function and write result in \( |p⟩ \),
- **G-rounds**: we calculate \( |c_{2k}⟩ \) \( (k \in \mathbb{N}) \) by calculating some \( g \)-function,
- **C-rounds**: we calculate all carry \( |c⟩ \) by calculating some \( g \)-function,

and we clean \( |p⟩ \) in inverse P-rounds. After inverse P-rounds, we calculate each bit of \( a + b \) by using these carries \( |c⟩ \). In this calculation, we run P-rounds and G-rounds simultaneously, and we run C-rounds and inverse P-rounds simultaneously. However, the value of carries remain on \( |c⟩ \). Thus, we must clean \( |c⟩ \) to \( |0⟩ \) except for \( c_n \). Draper et al. found that the value of carries \( c_i \) except \( c_n \) in \( a + b \) is the same in \( a + (2^n - 1) - a - b \). Therefore, we erase carries by performing the addition \( a + (2^n - 1) - a - b \) on the lower \( n - 1 \) qubits. The block level circuit is shown in Figure 3.

As noted above, a carry-lookahead adder is mainly constructed by a calculation on \( p \) and \( g \). We calculate \( p \) and \( g \) with eq. (9) or (10) respectively, and those are implemented by Toffoli gates as shown in Figure 4. The detailed explanation of Draper et al.’s adder, including which \( p \)-function or \( g \)-function we calculate, is given in Appendix A. In total, a carry-lookahead adder requires \( 10n \) Toffoli gates and \( 4n \) CNOT gates. Moreover, the Toffoli depth is \( 4 \log n \).

Up to this point, we have explained the construction of an adder. Draper et al. also proposed other operations, such as a subtractor and a comparator, based on their adder. The number of gates and the depth in a subtractor is almost the same as those in an adder. In a comparator, the number of gates is 60% of an adder and the depth is 50% of an adder. Draper et al. implement a comparator using only Initialization, P-rounds, G-rounds, and their inverses. More precisely, Draper et al. regard \( a \) and \( b \) as \( 2^{\log n} \)-bit numbers by padding 0 in higher bits, but we do not use these qubits. If we calculate \( p[i, j] \) or \( g[i, j] \) when \( i \leq n - 1 \) and \( j \geq n \), we calculate \( p[i, n] \) or \( g[i, n] \) respectively. Then, we calculate \( g[0, n] \) after G-rounds.

### C. T-COUNT MINIMIZATION OF A CARRY-LOOKAHEAD ADDER

Thapliyal et al. \(^{48}\) proposed \( T \)-count minimization by using relative-phase Toffoli gates. The standard Toffoli gate (ST) \(^{23}\) decomposition is given in Figure 5. However, we can calculate correctly even if we replace some Toffoli gates with Gidney’s relative-phase Toffoli gate (GRT) or its inverse (IGRT) \(^{45}\). GRT is shown in Figure 6 and the corresponding unitary matrix of GRT in the computational
FIGURE 5: The standard decomposition of a Toffoli gate \[23\]. We call this decomposition ST. The control bits are the first and second qubits, and the target bit is the third qubit. This calculation preserves the phase.

FIGURE 6: Gidney’s relative-phase Toffoli gate \[45\] given by the unitary matrix \((11)\). We call this decomposition GRT. The control bits are the first and second qubits, and the target bit is the third qubit. This calculation preserves the phase only when the target qubit is \(|0\rangle\) on input.

basis is

\[
\begin{pmatrix}
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & i & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -i & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -i & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -i & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0
\end{pmatrix},
\]

and we calculate correctly when the target bit is \(|0\rangle\). IGRT is shown in Figure 7. In the carry-lookahead adder, as in many circuits, we must clean our ancilla qubits, returning them to a known, disentangled state, typically \(|0\rangle\). In this case, we can reduce our cost by measuring the ancilla on IGRT. Gidney’s paper \[45\] shows that using measurement reduces 2 T gates. Using measurement is better because one accurate T gate requires many measurements.

Thapliyal et al. proposed two constructions. The first construction replaced Toffoli gates in Initialization and P-rounds.

FIGURE 7: Inverse of Gidney’s relative-phase Toffoli gate \[45\]. We call this decomposition IGRT. This calculation preserves the phase when we input \(|000\rangle, |010\rangle, |100\rangle\), or \(|111\rangle\), which are outputs of GRT having valid phase. Control-Z is a Clifford gate, and we use no T gate.

The second construction replaced all Toffoli gates with GRT or IGRT, increasing the required number of ancilla qubits. Thapliyal et al. call this construction qubit-optimize. The number of qubits is \(4n\) and the number of T gates is \(40n\).

The second construction replaced all Toffoli gates with GRT or IGRT, increasing the required number of ancilla qubits. Thapliyal et al. call this construction qubit-optimize. The number of qubits is \(4n\) and the number of T gates is \(40n\). However, we recalculated these results and our results differ from results in \[48\]. In our result, the number of qubits is \(4.5n\) and the number of T gates is \(28n\). The difference in the number of qubits occurs from our method for preparing ancilla qubits. Thapliyal et al. prepare new ancilla qubits for G-rounds and C-rounds respectively, while they recycle ancilla qubits for P-rounds. We apply this to G-rounds and C-rounds similarly.
D. THE GENERAL CONSTRUCTION OF A CONTROL MODULAR ADDER
In this subsection, we explain the calculation of
\[ |x\rangle |b\rangle |0\rangle \rightarrow |x\rangle |b + ax \text{ mod } N\rangle |0\rangle. \] (12)
The general construction of a control modular adder is shown in Figure 9. The first register has a single qubit which is used to hold the value of the control. We call this the CTRL qubit. The second register has \( n \) qubits which are used to hold the result of a control modular addition. The third register has a single qubit which is used to hold the result of a comparison temporarily. We call this the COMP qubit. Specifically, we determine whether we subtract \( N \) or not based on COMP. We conduct a comparator with one control qubit and an adder with two control qubits, and we write these as a C-comparator and a CC-adder, respectively.

To execute a control modular adder, we conduct operations in this order:

1) We compare the second register \( |b\rangle \) and the classical value \( N - a \). If \( b \geq N - a \), namely \( a + b \geq N \), we flip COMP.
2) If both CTRL and COMP are 1, we subtract \( N - a \) from the second register. If CTRL is 1 and COMP is 0, we add \( a \). Otherwise, we add no value.
3) If the second register is strictly less than \( a \), we flip COMP.

III. FIRST-LEVEL OPTIMIZATION: OUR CONSTRUCTION OF A CONTROL MODULAR ADDER
In this section, we explain first-level optimization on the original construction [39]. In the general construction, a comparator has about 1/2 the depth of a carry-lookahead adder. Thus, by constructing a carry-lookahead adder using the same general construction, the depth is about the same as 2 adders, because a carry-lookahead adder is composed of two comparators and one adder. In the original construction, we use 3 adders. Thus, we use only 2/3 of QK of the original construction when comparing two constructions of a control modular adder. The original construction applies two optimizations on repeating control modular adders. Our construction will be more efficient by adopting the same optimizations with some overhead, but the detail, such as the amount of overhead, should be evaluated in future work.

Based on the above discussion, we need to give the construction of

- C-comparator (subsection A)
- CC-adder (subsection B)

on a carry-lookahead adder. In this construction, we do not decompose Toffoli gates, because the decomposition of Toffoli gates is different in FTQ or NISQ respectively. Thus, we leave Toffoli gates as they are, and we consider the decomposition of Toffoli gates in Section IV.

In our construction, we consider the classicality of \( a \) and \( N \) as described by Markov and Saeedi [36] to realize higher efficiency. Moreover, we give a construction of C-comparator that is not given in the original paper. By doing these, we propose a circuit construction of a control modular adder.

Based on Figure 9, we construct our circuit as shown in Figure 10. We add the second \( n \)-qubit ancilla register for embedding value with CTRL. In addition to these registers, we use the carry register \( |c\rangle \) with \( n \) qubits and the \( p \)-function register \( |p\rangle \) with \( n \) qubits to realize the carry-lookahead adder, not represented in Figure 10. Thus, our control modular adder requires \( 4n + 2 \) qubits. The number of gates and the depth is given in Table 1 and the breakdown of this is given in Table 5 in Appendix B. Now, we explain the C-comparator and the CC-adder briefly.

A. CONSTRUCTION OF A C-COMPARATOR
In a C-comparator, only COMP is changed and other qubits do not change. Thus, to implement a C-comparator, it is sufficient that we add control operations only on the gates including COMP and remain other gates.

In our construction of a control modular adder, we use two types of C-comparators. In the first C-comparator, we flip COMP if CTRL is 1 and \( b \geq N - a \). In the final C-comparator, we flip COMP if CTRL is 1 and \( b < a \). In both cases, we judge whether \( b \geq d \) or \( b < d \) with a classical value of \( d \).

We construct these operations taking advantage of the classicality of \( d \). The intuitive explanation of this operation is that we calculate \( b + (2^n - d) \) and check whether there is an overflow in the \( n \)-th bit. Specifically,
\[ b + (2^n - d) = 2^n + (b - d) \] (13)
and there is an overflow when \( b \geq d \). This construction is similar to previous constructions by Markov and Saeedi [36], but slightly different from them because our construction does not require \( X \) gates on \( |b\rangle \). The number of gates and the depth is given in Table 1. The detailed construction is
TABLE 1: Gate count and depth of our proposed control modular adder. The breakdown of this is shown in Table 5 in Appendix B.

| Operation        | Count | Depth |
|------------------|-------|-------|
| C-comparator (twice) | 4n    | n     |
| CC-adder         | 9.5n  | 4.75n |
| Total            | 17.5n | 6.75n |

B. CONSTRUCTION OF A CC-ADDER

In a CC-adder, we embed values before and after an adder, similar to a C-adder [40]. Based on this construction, we apply optimization by considering the classicality of a and N. From this point forward, we mainly focus on embedding on |d⟩. In a CC-adder, we conduct the following:

- If CTRL is 1 and COMP is 1, we add a and subtract N. This operation can be realized by adding $2^n + a - N$ and disregarding the calculation of a carry $c_n$.
- If CTRL is 1 and COMP is 0, we add a.
- Otherwise, we add no value.

Thus, the embedding is conducted as in Figure 12. The resetting is conducted by inverting the embedding circuit.

After embedding, we apply a standard adder. Then, we conduct two optimizations as follows:

- disregarding gates including $|g [0, n]⟩$.
- eliminating gates in Initialization where we know the control bit is 0.

The number of gates and the depth is given in Table 1. The detailed construction and example circuit of a CC-adder are given in Appendix B.

FIGURE 11: Block-level view of our construction of a C-comparator. In this figure, we sort qubits from the low-order qubits to the high-order qubits, top to bottom. This circuit is symmetric about the Toffoli gate surrounded by a dotted box. $|c_i⟩$ is given as |0⟩ at the beginning of this circuit and these are cleared back to |0⟩ after the computation. The example circuits are shown in Figure 22 and 24 in Appendix B.

IV. SECOND-LEVEL OPTIMIZATION: CONSTRUCTING A CONTROL MODULAR ADDER FOR FTQ AND NISQ DEVICES

In this section, we explain our second-level optimization. We evaluate the computational cost for both FTQ on the logical layer, and NISQ, focusing on the decomposition of Toffoli gates. We define KQ more specifically for FTQ and NISQ and minimize this value. For FTQ, we minimize the number of $T$ gates by using Gidney’s relative-phase Toffoli gates. However, this construction does not take into consideration the cost of distillation. We take into account the cost of distillation by finding the maximal number of $T$ gates which should be run simultaneously, optimizing KQ$_T$. For NISQ, we apply Maslov’s relative-phase Toffoli gates with a small number of CNOT gates [49] and minimize KQ$_{CX}$. By doing these, we propose a control modular adder that is more efficient than Van Meter and Itoh [39], called the original construction in this section. In the following discussion, we disregard the rounds with $O(1)$ gates. In this section, we explain the optimization for FTQ in subsection A and the optimization for NISQ in subsection B.

A. COMPUTATIONAL COST ON THE FTQ LOGICAL LAYER

Next, we consider the optimal circuit for FTQ on the Logical layer, using Jones et al.’s architecture as a model [22]. This architecture, in common with other error corrected-architectures, provides a fundamental gate set consisting of $X$, $Y$, $Z$, CNOT, and $H$ gates, and measurement; here, we ignore qubit movement in the surface code. To run an $S$ gate, we prepare an ancilla qubit $|Y⟩ = (|0⟩ + i|1⟩)/\sqrt{2}$ and run the circuit shown in Figure 13. An $S^\dagger$ gate can be realized by the reverse circuit of Figure 13.

To achieve universal computation, we also need a non-Clifford gate; the choice of $T$ is typical. To run a $T$ gate, we prepare an ancilla qubit $|A⟩ = (|0⟩ + e^{i\pi/4}|1⟩)/\sqrt{2}$ and...
run the circuit shown in Figure 14. To run a $T^\dagger$ gate, we apply an $S^\dagger$ gate instead of a $S$ gate. To realize accurate $T$ gates, we must prepare accurate $|A\rangle$ states defined by $(|0\rangle + e^{\pi/4}|1\rangle)/\sqrt{2}$. Preparing $|A\rangle$ is done by distillation, as shown in Figure 23 in Appendix E. This distillation circuit requires 15 qubits and 6 time steps, even assuming all of the CNOT gates can be implemented concurrently, but this is difficult to realize. Distillation is an expensive operation, and its optimization is an ongoing topic of research [25]. Thus, a $T$ gate is the greatest factor in the cost of an FTOQ circuit, leading us to focus on reducing the number of $T$ gates.

We now minimize the number of $T$ gates on our control modular adder. We adopt the Thapliyal construction with minor modifications, namely the replacement into relative-phase Toffoli gates, except G-rounds in a C-comparator. We employ GRT in G-rounds and IGRT in inverse G-rounds as Figure 15. Our construction calculates correctly because Toffoli gates in G-rounds and inverse G-rounds are symmetric about the Toffoli gate surrounded by a dotted box as the block level circuit of a C-comparator shown in Figure 17.

Our construction requires an additional $n$ qubits to preserve in a C-comparator. Fortunately, we do not need $n$ qubits for $|d\rangle$ in Figure 10. Thus, we realize this construction without an overhead of qubits. We give example circuits as Figure 22 or 23 in Appendix B.

The computational cost of our control modular adder is shown in Table 3 and the breakdown of constructions based on our construction is given in Table 6 in Appendix D. From Table 2, our construction requires $43n$ $T$ gates. We call this construction a $T$-optimal control modular adder. The original construction requires $30n$ Toffoli gates, which when implemented using ST (each requiring 7 $T$ gates) gives $210n$ $T$ gates in total. Thus, our construction requires only $43/210 \approx 20\% T$ of the number of $T$ gates of the original construction.

Now, we focus on KQ of a $T$-optimal control modular adder. In this circuit, we use $O(n)$ qubits and $O(\log n)$ depth, giving a KQ of $O(n \log n)$. However, we do not consider the computational costs for distillation in this calculation. We can trade space for time, with substantial flexibility, by allocating more qubits to ancilla “factories”, corresponding to increasing the number of $T$ gates that are in concurrent execution [21], [52].

To realize an efficient circuit, we should consider the trade-off between the depth and the number of qubits allocated for distillation. For example, Kim et al. [53] showed that it is possible to run Shor’s algorithm with as little as 2% of the qubits dedicated to distillation, but this construction runs only a single $T$ gate at a time. Since the circuit still requires $O(n)$ $T$ gates, this construct is unable to run in depth $O(\log n)$ and is instead still constrained to $O(n)$ depth. To realize smaller KQ, we must run many $T$ gates parallel. However, there is an upper bound on the number of $T$ gates that can be usefully run in parallel, with the depth limited by the cascading reuse of the qubits. Paler and Basmadjian also consider this problem [54], and they have concluded that we must determine optimal scheduling methods for $T$ gates. To realize an accurate estimate of the cost and to enable fair comparison with prior research, we must take into account the $T$ gate costs, including the space for distillation [22], [52], [55], allowing a circuit to run at “the speed of data” [55].

However, it is difficult to calculate computational costs for distillation precisely, because the cost depends on many architecture-specific parameters. Instead of KQ, we define a new index $KQ_T$, defined as the product of the number of logical qubits and $T$-depth. We define $n_T$ as the $T$-width, the upper-bound of the number of $T$ gates running simultaneously. We assume that we require a constant $c_9$ logical qubits for the distillation step. By calculating $n_T$ minimizing $KQ_T$, we reduce the computational cost of our control modular adder.

In the above discussion, our control modular adder uses $4n + 2$ qubits for calculation, as explained in Section III. In addition, we require ancilla qubits for running $n_T$ $T$ gates. Specifically, to run one $T$ gate, we require one qubit $|Y\rangle$ for running $S$ gates and $c_9$ qubits for generating $|A\rangle$. Thus, when we run $n_T$ $T$ gates simultaneously, we use the following.
TABLE 2: \( T \)-count of our control modular adder and prior work. The latter four constructions are based on our construction proposed in Section III. The breakdown of the latter four constructions is shown in Table 2 in Appendix D.

| Construction                  | # comparators | # adders | Total \( T \)-count |
|-------------------------------|--------------|----------|---------------------|
| Van Meter and Itoh [39]       | 0            | 3        | 210n                |
| Draper et al. [43]            | 2            | 1        | 122.5n              |
| Thapliyal et al. (qubit-optimize) [48] | 2       | 1        | 70n                 |
| Thapliyal et al. (T-optimize) [48] | 2       | 1        | 51n                 |
| Ours                         | 2            | 1        | 43n                 |

qubits:
- \(| y \rangle\) (Contains \(| Y \rangle\) states) \( n_T \) qubits
- \(| g \rangle\) (Generates \(| A \rangle\) states) \( c_g n_T \) qubits.

The number of qubits in \(| y \rangle\) is given as \( n_T \), because we consume one \( S \) gate in each \( T \) gate. Then, the number of qubits is

\[
4n + (c_g + 1)n_T + 2. \tag{14}
\]

Now, we calculate \( T \)-depth. To calculate \( T \)-depth, we assume that we run GRT with the same timing, and each GRT has 2 \( T \)-depth from Figure 6. \( T \)-depth depends on \( n_T \) as Figure 16. Then, \( T \)-depth is

\[
\frac{86n}{n_T} + 12 \log n_T - 12. \tag{15}
\]

The detailed calculation is given in Appendix C.

FIGURE 16: Calculating \( T \)-depth. Distill means distillation circuits. In the naive construction, we run as many \( T \) gates as possible. In our construction, we restrict the upper-bound of the number of simultaneous \( T \) gates to \( n_T \). When we reduce \( n_T \), the total number of qubits is smaller and \( T \)-depth is larger.

Now, we minimize \( KQ_T \) on \( n_T \). \( KQ_T \) is

\[
(4n + (c_g + 1)n_T + 2) \left( \frac{86n}{n_T} + 12 \log n_T - 12 \right). \tag{16}
\]

We minimize this on \( n_T > 0 \).

Letting the expression in Eq. 16 be \( f(n_T) \), we see that

\[
\frac{d^2 f(n_T)}{dn_T^2} > 0 \tag{17}
\]

in \( n_T > 0 \). Thus, \( f(n_T) \) is a convex function and it is sufficient to search for only one optimal value of \( n_T \). Then, the optimal value

\[
n_T = \sqrt{\frac{86}{3(c_g + 1)} \frac{n}{\sqrt{\log n}}} \tag{18}
\]

Thus, \( O\left(\frac{n}{\sqrt{\log n}}\right) \) \( T \)-width minimizes \( KQ_T \). Plugging this value into Eq. 16

\[
4n + (c_g + 1)n_T + 2 \sim 4n \tag{19}
\]

\[
\frac{86n}{n_T} + 12 \log n_T - 12 \sim 12 \log n \tag{20}
\]

Therefore, the dominant term of \( KQ_T \) is \( 48n \log n \).

B. OPTIMIZATION FOR NISQ

Now, we propose a form of the control modular adder reducing CNOT gates. To reduce this number, we review the decomposition of Toffoli gates into CNOT gates. We use relative-phase Toffoli gates with differences in phase as in Figures 7 and 18 proposed by Maslov [49]. The corresponding unitary matrix of Figure 17 in the computational basis is

\[
\begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -i \\
0 & 0 & 0 & 0 & 0 & 0 & i & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & i & 0
\end{bmatrix} \tag{21}
\]

This calculation changes the phase when we input \(| 1 \rangle | 0 \rangle | 1 \rangle \), \(| 1 \rangle | 1 \rangle | 0 \rangle \), or \(| 1 \rangle | 1 \rangle | 1 \rangle \). We call this relative-phase Toffoli gate RT3, and we call its inverse IRT3. The corresponding unitary matrix of Figure 18 in the computational basis is

\[
\begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -i \\
0 & 0 & 0 & 0 & 0 & 0 & -i & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix} \tag{22}
\]

This calculation changes the phase when both control bits are 1. We call this relative-phase Toffoli gate RT4, and its inverse...
requires 30n Toffoli gates implemented by ST using 6 CNOT gates, and we use an additional 4.5n CNOT gates in embedding or resetting. Thus, the original construction requires 184.5n CNOT gates in total. Therefore, our construction reduces the number of CNOT gates to only 35% of the number in the original.

Next, we compare KQ_{CX}, defined as the product of the number of qubits and CNOT-depth. Our construction requires 120n log n KQ_{CX}. The original construction requires 12 log n Toffoli depth implemented by ST requiring 6CNOT-depth, and we require 6 log n CNOT-depth for the embedding step. Thus, the original construction requires 78 log n CNOT-depth and 312n log n KQ_{CX}. Therefore, our construction requires only 38% of the KQ_{CX} of the original construction.

V. CONCLUSION AND FUTURE WORK

In this study, we proposed a method of optimizing a control modular adder based on a carry-lookahead adder [43] and Van Meter and Itoh’s construction [39]. First, we show that the general construction given as Figure 9 is about 2/3 of the KQ of the original construction. Then, we construct a more efficient circuit. We evaluate the computational cost in FTQ and we show that our circuit requires only 20% of the T gates of the original. Moreover, we show that our circuit achieves its minimum KQ_{T} when we run $\Theta \left(\frac{n}{\sqrt{\log n}}\right)^T$ gates simultaneously. Finally, we propose an efficient circuit for use in the NISQ era, and we show that our circuit requires only 35% of the CNOT gates and 38% KQ_{CX} of the original.

In this work, we have focused on optimizing Toffoli gates by using relative-phase Toffoli gates. However, in previous research [56], [57], other researchers have used gates such as Fredkin and Peres gates. These gates also may be simplified by replacing them with relative-phase gates. Thus, we expect that those circuits would also show an improvement with these techniques applied.

In this paper, we have considered only the single control modular addition. In additional future work, the circuits that postpone and summarize multiple modular arithmetic operations, as proposed by Van Meter and Itoh [39], should be addressed using similar optimization techniques. In addition, it is important to minimize KQ by reordering gates [37], [58].

Our construction does not consider the architecture of quantum computers as linear nearest neighbor architecture [33], [50], [51]. Thus, in the next step, we will consider the appropriate architecture and additional cost for our construction.

Lastly, we focused only on the Logical layer of FTQ in this study. Future work, we must consider the mapping to physical qubits, as well as distillation protocols.

APPENDIX.

A. DETAILED EXPLANATION OF DRAPER ET AL.’S CARRY-LOOKAHEAD ADDER

Draper et al.’s carry-lookahead adder is given as follows:

**Initialization**: (n Toffoli gates and n CNOT gates)

![Figure 17](image1.png)  
**Figure 17**: A relative-phase Toffoli gate with 3 CNOT (RT3). This calculation changes the phase when we input $|1\rangle \langle 0|$, $|1\rangle \langle 1|$, and $|1\rangle \langle 1|$. We call the inverse circuit of RT3, IRT3.

![Figure 18](image2.png)  
**Figure 18**: A relative-phase Toffoli gate with 4 CNOT (RT4). This calculation changes the phase when both control bits are 1. We call the inverse circuit of RT4, IRT4.
TABLE 3: CNOT count of our control modular adder and prior work. The latter four constructions are based on our construction proposed in Section III. The breakdown of the latter four constructions is shown in Table 7 in Appendix D.

| Construction                                | #comparators | #adders | Total CNOT count |
|----------------------------------------------|--------------|---------|------------------|
| Van Meter and Itoh [59]                      | 0            | 3       | 184.5n           |
| Draper et al. [43]                           | 2            | 1       | 111.75n          |
| Thapliyal et al. (qubit-optimize) [48]        | 2            | 1       | 88n              |
| Thapliyal et al. (T-optimize) [48]           | 2            | 1       | 104n             |
| Ours                                         | 2            | 1       | 64.75n           |

TABLE 4: KQ <sub>CX</sub> of our control modular adder and prior work. The latter four constructions are based on our construction proposed in Section III. The breakdown of the latter four constructions are shown in Table 8 in Appendix D.

| Construction                                | #qubits | The depth of the circuit | KQ <sub>CX</sub> |
|----------------------------------------------|---------|--------------------------|------------------|
| Van Meter and Itoh [59]                      | 4n      | 78 log n                 | 312n log n       |
| Draper et al. [43]                           | 4n      | 50 log n                 | 200n log n       |
| Thapliyal et al. (qubit-optimize) [48]        | 4n      | 50 log n                 | 200n log n       |
| Thapliyal et al. (T-optimize) [48]           | 4.5n    | 66 log n                 | 297n log n       |
| Ours                                         | 4n      | 30 log n                 | 120n log n       |

We calculate all carries |c⟩ by using eq. (10). We use a parameter t<sub>c</sub> similar to the way we used it in P-rounds. We decrease t<sub>c</sub> from ⌈log(2n/3)⌉ to 1. In each t<sub>c</sub>, we calculate |c<sub>2<i>c</sub>+2<i><sub>c</sub>-1</sub>| (1 ≤ i ≤ ⌈(n − 2<sup>c</sup>−1) / 2<sup>c</sup> − 1⌉) by setting |c<sub>2<i>c</sub>+1</sub>| and |p[2<sup>c</sup>·i, 2<sup>c</sup>·i+2<sup>c</sup>−1</sup>−1</sup>−1), as the control qubits and |c<sub>2<i>c</sub>+2<i><sub>c</sub>-1</sub>| as the target qubit in Toffoli gate in Figure 4b. These Toffoli gates are applied simultaneously in each t<sub>c</sub>.

**Inverse P-rounds** (n Toffoli gates and log n Toffoli depth)

We apply the same gates as P-rounds in reverse order. Rounds with t<sub>p</sub> can be run in parallel with former C-round with t<sub>p</sub> + 1.

**Calculating |a + b⟩ (n CNOT gates)**

We calculate (a + b), (0 ≤ i ≤ n − 2) on |b<sub>i</sub>⟩. We apply CNOT gates with the control qubit of |c<sub>i+1</sub>⟩ and the target qubit of |b<sub>i+1</sub>⟩. These CNOT gates are applied simultaneously.

**Erasing Carry** (5n Toffoli gates, 2n CNOT gates, and 2 log n Toffoli depth)

We erase all carries by applying the inverse circuit of a + (2<sup>n</sup>−1 − a − b) on the lower n − 1 bits, as shown in Figure 20. We apply gates before P-rounds and after inverse initialization to erase carries. We call these gates PE-rounds and inverse PE-rounds respectively.

Now, we show the example circuit of Draper et al.’s carry-lookahead adder as given in Figure 21. In this example, we define a and b as 6-bit values, and we calculate |a⟩|b⟩ → |a⟩|a + b⟩. In Figure 21, in contrast to Figure 9, qubits are sorted from low order to high order.

**B. DETAILED CONSTRUCTION OF OUR CONTROL MODULAR ADDER**

In this section, we explain detail of our control modular adder. We show the example figures of our control modular adder too.

1) A C-Comparator

Now, we explain the construction of a C-comparator in more detail. In a C-comparator, we judge whether or not b ≥ d, where b is a quantum value and d is a classical value. As
noted in Section III. A., we conduct this by calculating the carry out of the entire circuit \( b + (2^n - d) \). Our construction is given as follows:

**Initialization**

If we conduct Initialization naively, we apply a Toffoli gate and a CNOT gate for each bit. However, the compilation of a quantum algorithm often requires compilation (selection of the sequence of gates) to be adapted to the specific classical values that are inputs to the overall algorithm. Because \( 2^n - d \) is a classical value, we can convert some Toffoli gates to CNOT gates and eliminate other gates. Then, we calculate each \( (2^n - d)_i \) \( (0 \leq i \leq n - 1) \). If \( (2^n - d)_i = 1 \),

1) We apply CNOT gates with the control qubit \( |b_i\rangle \) and the target qubit \( |c_{i+1}\rangle \).

2) We apply X gates with \( |b_i\rangle \).

These operations correspond to Toffoli gates or CNOT gates in the Initialization phase in Draper et al.’s construction, respectively.

**P-rounds and G-rounds**

We conduct P-rounds and G-rounds similar to Draper et al.’s construction.

**Writing result on the COMP qubit** \((O(1)\text{ gates and } O(1)\text{ depth})\)

If we want to flip COMP when \( b \geq d \), we apply Toffoli gates with the control qubits of CTRL and \( |0, n_i\rangle \), and with the target qubit of COMP. If we want to flip COMP when \( b < d \), we apply Toffoli gates similarly to \( b \geq d \), but we apply NOT gates on \( |0, n_i\rangle \) before and after the Toffoli gate.

**Resetting qubits**

We conduct inverse G-rounds and inverse P-rounds similar to Draper et al.’s construction. Moreover, we conduct the inverse of our Initialization. Then, we reset all qubits except COMP as the initial values.

2) A CC-adder

First, we explain the construction of embedding in more detail. We want to embed as follows:

- If CTRL is 1 and COMP is 1, we embed \( 2^n + a - N \).
- If CTRL is 1 and COMP is 0, we embed \( a \).
- Otherwise, we embed no value.

Therefore, we embed on the second register on Figure 10 as follows:

- If CTRL is 1 and \( (2^n + a - N)_i = a_i = 1 \), \( i \)-th qubit is \( |1\rangle \).
- If CTRL is 1, COMP is 1, \( (2^n + a - N)_i = 1 \), and \( a_i = 0 \), \( i \)-th qubit is \( |1\rangle \).
- If CTRL is 1, COMP is 0, \( (2^n + a - N)_i = 0 \), and \( a_i = 1 \), \( i \)-th qubit is \( |1\rangle \).
- Otherwise, we do nothing.

In the above condition, the values of \( (2^n + a - N)_i \) and \( a_i \) are classical information, and CTRL and COMP are quantum
information. Thus, embedding in the first condition can be realized by CNOT gates with the control qubit of CTRL. Moreover, embedding in the second and third condition can be realized by Toffoli gates with the control qubits of CTRL and COMP. However, the set of i in each classical condition has no overlap. Therefore, once we embed one of i, we can embed the remaining value as CNOT gates. In each set, we have average n/4 elements requiring n/4 CNOT gates, O(1) additional gates. Thus, these embedding can be implemented by 3n/4 CNOT gates. Moreover, because we can run these simultaneously, embedding requires log n CNOT depth. The reset of embedding can be implemented similarly.

Next, we explain the optimization in an adder. In our calculation, there is no carry for \( g[0, n] \) whether we subtract \( N - a \) or add \( a \). Thus, we can disregard calculation of carry qubit \( g[0, n] \). To realize this, we omit calculation of \( p[i, n] \) and \( g[i, n] \) (\( i < n \)). Moreover, by using classicality of \( a \) and \( N \), we know that we embed no value in average n/4 qubits on the second register of Figure [10]. In these qubits, we can omit Initialization, inverse Initialization, and CNOT gates with the control qubit of \( |a_i\rangle \) and the target qubit of \( |b_i\rangle \) in erasing carry. By considering these optimizations, we reduce n/2 Toffoli gates and 3n/4 CNOT gates.

The gate count and depth is shown in Table 5.

3) Example of Our Control Modular Adder
We show an example of a 6-bit control modular adder when \( N = 59 \) and \( a = 37 \). Circuits are given in Figures [22][24].

In these example figures registers are shown with low-order qubits at the top, in contrast to Figure [10]. In this subsection, the register \( |b\rangle \) contains a quantum value.

The algorithm follows in this order:

1) Conduct a C-comparator with the control qubit CTRL. Compare \( |b\rangle \) and \( N - a = 22 \). If \( b \geq 22 \), flip COMP. This is implemented by adding \( 2^6 - (N - a) = 42 \) and using the carry out.

2) Conduct a CC-adder. If both CTRL and COMP are 1, subtract \( N - a = 22 \). This is implemented by adding \( 2^6 - (N - a) = 42 \) without calculating carry \( c_6 \). If CTRL is 1 and COMP is 0, add \( a = 37 \), otherwise, add no value.

3) Conduct a C-comparator with the control qubit CTRL. Compare \( |b\rangle \) and \( a = 37 \). If \( b < 37 \), flip COMP. This is implemented by calculating carry of adding \( 2^6 - a = 27 \).

These steps correspond to Figure [22][23] and [24] respectively.

C. DETAILED CALCULATION OF DEPTH
In this section, we analyze the T-depth of our T-optimal control modular adder. We assume that we run GRT with the same timing, and each GRT has T-depth 2 from Figure [6]. We focus on the parts that can be run concurrently. Except for Initialization, we run

- P-rounds and G-rounds simultaneously,
- C-rounds and inverse P-rounds simultaneously,

We add \( 2^6 - 22 = 42 = 101010_2 \) and use the COMP qubit as the carry out of the adder. The Init phase consists of pairs of gates, a CNOT and an X, on the second, fourth, and sixth groups of qubits including \( |d_i\rangle \), \( |b_i\rangle \), and \( |c_{i+1}\rangle \) from the lowest bit. This circuit is symmetric about the Toffoli gate surrounded by a dotted box. Init, IP, IG, and IInit mean Initialization, Inverse P-rounds, Inverse C-rounds, Inverse G-rounds, and Inverse Initialization respectively.
TABLE 5: Gate count and depth of our proposed control modular adder. We omit the rounds whose gate count is $O(1)$ and whose depth is $O(1)$.

| Operation       | Rounds      | CNOT | Depth |
|-----------------|-------------|------|-------|
| C-comparator    |             |      |       |
| (twice)         | Initialization | 0    | $O(1)$ |
|                 | P           | $0.5n$ | \(\log n \) |
|                 | G           | $n$   | 0     |
|                 | Inverse G   | $n$   | \(\log n \) |
|                 | Inverse P   | $n$   | 0     |
|                 | Inverse Initialization | 0    | $O(1)$ |
|                 | Total       | $4n$  | $2\log n$ |
| CC-adder        |             |      |       |
|                 | Embedding   | $O(1)$ | $\log n$ |
|                 | Initialization | 0.75n | $O(1)$ |
|                 | P           | $n$   | \(\log n \) |
|                 | G           | $n$   | 0     |
|                 | C           | $n$   | \(\log n \) |
|                 | Inverse P   | $n$   | 0     |
|                 | Calculating | $|a + b|$ | 0     |
|                 | PE          | 0     | $O(1)$ |
|                 | Inverse C   | $n$   | \(\log n \) |
|                 | Inverse G   | $n$   | 0     |
|                 | Inverse P   | $n$   | \(\log n \) |
|                 | Inverse Initialization | 0.75n | $O(1)$ |
|                 | Resetting   | $O(1)$ | $\log n$ |
|                 | Total       | 9.5n  | $4 \log n$ |

P-rounds and inverse C-rounds simultaneously, and inverse G-rounds and inverse P-rounds simultaneously.

In the first and third steps, we run many $T$ gates simultaneously at the start and fewer $T$ gates as the calculation progresses. In the second and fourth steps, we run only a few $T$ gates simultaneously initially and more as the calculation progresses. Thus, there is a difference in the number of $T$ gates we can run simultaneously.

As noted in Section IV. A., we define $n_T$ as the upper-bound of the number of $T$ gates running simultaneously, and we calculate $T$-depth based on $n_T$ as in Figure 16. In each round, there are parts where we can run more than $n_T$ $T$ gates. However, by setting $n_T$, we run these $T$ gates separately. Compared to this, in the parts having less than $n_T$ $T$ gates, we can run these $T$ gates simultaneously.

First, we consider the parts having fewer than $n_T$ $T$ gates, which happens when we run P-rounds and G-rounds simultaneously, C-rounds and inverse P-rounds simultaneously, P-rounds and inverse C-rounds simultaneously, and inverse G-rounds and inverse P-rounds simultaneously. In these rounds, if we have no restriction on running $T$ gates, patterns are given as follows:

- In the first and the third cases, the number of $T$ gates we can run simultaneously decreases by one half as the calculation progresses. Thus, in the latter part of the calculation, we run fewer than $n_T$ $T$ gates simultaneously. This part has $T$-depth $2 \log n_T$ and $n_T$ $T$ gates in total.
- In the second and the fourth cases, the number of $T$ gates we can run simultaneously doubles as the calculation progresses. Thus, in the former part of the calculation, we run less than $n_T$ $T$ gates simultaneously. This part has $T$-depth $2 \log n_T$ and $n_T$ $T$ gates in total.

We have 6 parts each with a small number of $T$ gates, as follows:

- P-rounds and G-rounds in the first C-comparator,
- P-rounds and G-rounds in the CC-adder,
- C-rounds and inverse P-rounds in the CC-adder,
- P-rounds and inverse C-rounds in the CC-adder,
- inverse G-rounds and inverse P-rounds in the CC-adder, and
- P-rounds and G-rounds in the final C-comparator

Thus, we consume $2 \log n_T$ $T$-depth and $6n_T$ $T$ gates in these.

Next, we consider the remaining parts. In these parts, we run $T$ gates $n_T$ each. The number of total $T$ gates is $43n$ from Table 5 and we run $43n - 6n_T$ $T$ gates. Thus, $T$-depth of this part is given by

$$\frac{2 (43n - 6n_T)}{n_T} = \frac{86n}{n_T} - 12. \quad (25)$$

In conclusion, $T$-depth is given by

$$\frac{86n}{n_T} + 12 \log n_T - 12. \quad (26)$$

D. DETAILED GATE COUNT ON FTQ OR NISQ

In this section, we detail the $T$ gate count on FTQ or NISQ. The FTQ count is shown in Table 7. The detailed CNOT gate count on NISQ is shown in Table 8. The detailed CNOT depth count and KQ$_{CX}$ on NISQ are shown in Table 8.

E. A DISTILLATION CIRCUIT FOR A $T$ GATE

A distillation circuit for a $T$ gate is given as Figure 25.
TABLE 6: The breakdown of Toffoli count and \( T \)-count of our control modular adder. Tof means the number of Toffoli gates in each round. Gate means the type of using relative-phase Toffoli gates in each round. Cost means the number of T gates in each relative-phase Toffoli gate. Count means \( T \)-count in each round. We omit the rounds whose \( T \)-count is \( O(1) \). Inv means Inverse, C-comp means a C-comparator, CC-add means a CC-adder, and Init means Initialization.

| Operation | Rounds | Tof | gate count | Tof | gate count | Tof | gate count | Tof | gate count |
|-----------|--------|-----|------------|-----|------------|-----|------------|-----|------------|
| C-comp (twice) |        |     |            |     |            |     |            |     |            |
| P         | \( n \) | ST 7 7n | GRT 4 4n | GRT 4 4n | GRT 4 4n |
| G         | \( n \) | ST 7 7n | ST 7 7n | PGRT 4 4n | PGRT 4 4n |
| InvG      | \( n \) | ST 7 7n | ST 7 7n | PGRT 4 4n | IGRT 0 0 |
| InvP      | \( n \) | ST 7 7n | IGRT 0 0 | IGRT 0 0 | IGRT 0 0 |
| InvInit   | \( 0.75n \) | ST 7 7n | ST 7 7n | ST 7 7n | ST 7 7n |
| Total     |       |     |            |     |            |     |            |     |            |
| CC-add    |        |     |            |     |            |     |            |     |            |
| Init      | \( 0.75n \) | ST 7 5.25n | GRT 4 3n | GRT 4 3n | GRT 4 3n |
| P         | \( n \) | ST 7 7n | GRT 4 4n | GRT 4 4n | GRT 4 4n |
| G         | \( n \) | ST 7 7n | ST 7 7n | PGRT 4 4n | PGRT 4 4n |
| C         | \( n \) | ST 7 7n | ST 7 7n | PGRT 4 4n | PGRT 4 4n |
| InvP      | \( n \) | ST 7 7n | IGRT 0 0 | IGRT 0 0 | IGRT 0 0 |
| InvG      | \( n \) | ST 7 7n | ST 7 7n | PGRT 4 4n | PGRT 4 4n |
| InvP      | \( n \) | ST 7 7n | IGRT 0 0 | IGRT 0 0 | IGRT 0 0 |
| InvInit   | \( 0.75n \) | ST 7 5.25n | IGRT 0 0 | IGRT 0 0 | IGRT 0 0 |
| Total     |       |     |            |     |            |     |            |     |            |
| Total     |       |     |            |     |            |     |            |     |            |

TABLE 7: The breakdown of Toffoli count and CNOT count of our control modular adder. Gate means the type of using relative-phase Toffoli gates in each round. Cost means the number of CNOT gates in each relative-phase Toffoli gate. Count means CNOT count in each round. We do not show the rounds whose CNOT count is \( O(1) \). Inv means Inverse, C-comp means a C-comparator, CC-add means a CC-adder, Init means Initialization, Embed means Embedding, Calc means Calculating of \((a + b)\), and Reset means Resetting.

| Operation | Rounds | CNOT | gate count | CNOT | gate count | CNOT | gate count | CNOT | gate count |
|-----------|--------|------|------------|------|------------|------|------------|------|------------|
| C-Comp (twice) |        |      |            |      |            |      |            |      |            |
| Embed     | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |
| Init      | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |
| P         | \( n \) | ST 6 6n | GRT 6 6n | GRT 6 6n | RG3 3 3n |
| G         | \( n \) | ST 6 6n | ST 6 6n | PGRT 8 8n | RT3 3 3n |
| C         | \( n \) | ST 6 6n | ST 6 6n | PGRT 8 8n | RT3 4 4n |
| InvP      | \( n \) | ST 6 6n | IGRT 1 n | IGRT 1 n | IRT3 3 3n |
| InvInit   | \( 0.75n \) | ST 6 6n | IGRT 1 n | IGRT 1 n | IRT3 3 3n |
| Total     |       |      |            |      |            |      |            |      |            |
| CC-add    |        |      |            |      |            |      |            |      |            |
| PE        | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |
| P         | \( n \) | ST 6 6n | GRT 6 6n | GRT 6 6n | RG3 3 3n |
| InvC      | \( n \) | ST 6 6n | ST 6 6n | PGRT 8 8n | IRT4 4 4n |
| InvG      | \( n \) | ST 6 6n | ST 6 6n | PGRT 8 8n | IRT4 4 4n |
| InvP      | \( n \) | ST 6 6n | IGRT 1 n | IGRT 1 n | IRT3 3 3n |
| InvInit   | \( 0.75n \) | ST 6 4.5n | IGRT 1 0.75n | IGRT 1 0.75n | RT4 4 4n |
| Reset     | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |      | \( 0.75n \) |
| Total     |       |      |            |      |            |      |            |      |            |
TABLE 8: The breakdown of Toffoli count and CNOT-depth of our control modular adder. Gate means the type of using relative-phase Toffoli gates in each round. Cost means the number of CNOT gates in each relative-phase Toffoli gate. Depth means CNOT-depth in each round. We omit the rounds whose CNOT-depth is $O(1)$. Inv means Inverse, C-comp means a Comparator, CC-add means a CC-adder, Init means Initialization, Embed means Embedding, and Reset means Resetting.

| Operation | Rounds | Draper et al. [43] | Thapliyal et al. [48] (qubit-optimize) | Thapliyal et al. [48] (T-optimize) | Ours |
|-----------|--------|-------------------|--------------------------------------|-----------------------------------|------|
| C-Comp (twice) | | | | |
| Toffoli | $\log n$ | $36 \log n$ | $4 \log n$ | $3 \log n$ | $3 \log n$ |
| G | ST | 6 | $6 \log n$ | $6 \log n$ | $6 \log n$ |
| InvG | ST | 6 | $6 \log n$ | $6 \log n$ | $6 \log n$ |
| InvP | ST | 6 | $6 \log n$ | $6 \log n$ | $6 \log n$ |
| Total | | $2 \log n | 12 \log n | 12 \log n | 12 \log n |
| CC-add | | | | |
| P | Toffoli | $\log n$ | $\log n$ | $\log n$ | $\log n$ |
| G | ST | 6 | $6 \log n$ | $6 \log n$ | $6 \log n$ |
| C | ST | 6 | $6 \log n$ | $6 \log n$ | $6 \log n$ |
| InvP | ST | 6 | $6 \log n$ | $6 \log n$ | $6 \log n$ |
| Total | | $2 \log n | 20 \log n | 20 \log n | 20 \log n |
| Total #qubits | $50 \log n$ | $50 \log n$ | $60 \log n$ | $60 \log n$ |
| KOCCX | $200 \log n$ | $200 \log n$ | $297n \log n$ | $120n \log n$ |

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FIGURE 23: An example of the CC-adder. If both CTRL and COMP are 1, we subtract $N - a = 22$. This is implemented by adding $2^6 - (N - a) = 42 = 101010_2$ without calculating carry $c_6$. If CTRL is 1 and COMP is 0, we add $a = 37 = 100101_2$. Based on these, we conduct embedding and resetting. The remaining part is an adder, and we omit the calculation of $p[i, 6]$ and $q[i, 6]$ ($i < 6$).

FIGURE 24: An example of the last C-comparator. We flip the COMP qubit if $b < 37$. This is achieved by adding $2^6 - 37 = 27 = 011011_2$ and using the carry out. First, we apply pairs of gates, a CNOT and an $X$ gate, on the first, second, fourth, and fifth groups of qubits. In contrast to Figure 22, we apply $X$ gates before and after the center Toffoli gate. This circuit is symmetric about the Toffoli gate surrounded by a dotted box. Init, IP, IG, and IInit means Initialization, Inverse P-rounds, Inverse C-rounds, Inverse G-rounds, and Inverse Initialization respectively.
FIGURE 25: A distillation circuit of $|A\rangle$. By this distillation circuit, we reduce the error rate of $|A\rangle$ from $p$ to $35p^3$.
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