Fabrication process of InGaAs-based nanodiode array using electron-beam lithography technique

Shahrir R. Kasjoo1*, Arun K. Singh2, Linqing Q. Zhang3

1 School of Microelectronic Engineering, Universiti Malaysia Perlis, Pauh Putra Campus, 02600 Arau, Perlis, Malaysia
2 Department of Electronics and Communication Engineering, Punjab Engineering College (Deemed to be University), Sector-12, Chandigarh-160012, India
3 School of Electrical and Electronic Engineering, University of Manchester, Manchester M13 9PL, United Kingdom

*shahrirrizal@unimap.edu.my

Abstract. Self-switching diode (SSD) is a unipolar two-terminal planar device which has a typical channel in nanoscale dimension. It has shown outstanding properties as a microwave and submillimeter wave rectifier by exploiting its nonlinear current-voltage (I-V) characteristic and intrinsically low parasitic capacitance. In detection systems, SSDs are often used with an antenna to form a rectifying antenna (rectenna). The large impedance mismatch between SSD and antenna, due to high resistance of a single SSD, has always hampered the rectenna to achieve good extrinsic rectification performance (e.g., voltage responsivity > 400 V/W). As such, a large array of SSDs connected in parallel is very much desired to reduce the device resistance, and hence minimizing the impedance mismatching issue. In this work, an interdigital structure which can accommodate approximately 2,000 SSDs in parallel has been utilized. The material used was InGaAs/InAlAs heterostructure grown onto an InP substrate. The fabrication of the SSD array has implemented an electron-beam lithography (EBL) technique and the use of polymethyl methacrylate (PMMA) as a masking layer. The fabricated SSD array has shown a typical diode-like I-V characteristic, indicating that EBL method is not only convenient to realize nanoscale electronic devices, but also very practical for large area operations.

1. Introduction
The resolution of conventional photolithography equipment is typically more than 1 μm. Higher resolution photolithography machines are commercially available but they are far too expensive and often unaffordable by university research groups. Alternative high-resolution lithography methods are therefore required to fabricate electronic devices in sub-micron dimensions. Electron-beam lithography, also known as EBL, is one of the most commonly used techniques for the patterning of nanoscale structures. Indeed, modern EBL systems can routinely achieve patterns with feature sizes well below 20 nm. The EBL machine employs similar technology to that used in scanning electron microscope (SEM). Therefore, EBL can be performed by simply modifying an SEM with an additional beam-blanker and electron-beam controller. In fact, the first EBL system was developed in the 1960s using existing SEM technology [1, 2]. Unlike photolithography, EBL does not require the fabrication of masks, which can be very expensive, especially for nanoscale features. However, a
major drawback of using EBL is the extremely low throughput, making it impractical to use in high-volume production.

In this report, an EBL system was utilized to fabricate nanodiodes, known as the self-switching diodes (SSDs) [3], which typically have channels close to nanoscale dimensions (see Figure 1). The material used in this work was In\(_{0.53}\)Ga\(_{0.47}\)As/In\(_{0.52}\)Al\(_{0.48}\)As heterostructure grown onto an InP substrate. The SSD is a unipolar two-terminal planar device which has shown promising properties as a high-speed rectifier (up to several terahertz frequencies) by the exploitation of its nonlinear current-voltage (I-V) characteristic and intrinsically low parasitic capacitance [4–6]. Details of its working principle can be found in refs. [3, 4].

For detection at high frequencies, the SSDs are often integrated with an antenna to form a rectifying antenna, also known as rectenna. The large impedance mismatch between SSD rectifier and antenna (due to high resistance of SSDs) has always hampered the rectenna to achieve high extrinsic responsivity towards the rectified signals [5, 6]. A large array of SSDs connected in parallel is therefore very much desired to reduce the impedance of the device, and hence minimizing this mismatching issue. As such, EBL is a very convenient method to realize a large SSD array. It is also faster and more practical for large area operations when compared to our previous reported fabrication technique using atomic-force microscope (AFM) lithography [7].

In this work, an interdigital structure which can house approximately 2,000 SSDs connected in parallel has been utilized as shown in Figure 2(a) i.e., ~ 1,000 SSDs can be placed in each of the left-hand side (LHS) and right-hand side (RHS) of the interdigital structure. These SSDs were fabricated within the fingers of the interdigital structure using an EBL system manufactured by Raith Inc. (modified version of LEO SEM) with RAITH ELPHY GDS II editor. The planar structure of the SSD has allowed the fabrication of a large number of the devices in a single lithography step. Interconnection layers, which may introduce parasitic elements, are therefore no longer required. This is one of the main advantages of SSD over conventional electronic devices in which the whole fabrication process, presented in the next section, has been made simpler, faster and at lower cost.

It is worth noticing that, the SSD array fabricated in this work was the same device reported in refs. [8, 9] which has been utilized as a microwave rectifier. However, in this report, the fabrication process of the device is discussed in more detail.

![Figure 1](image1.png)

**Figure 1.** Illustration of a typical structure of a single self-switching diode (SSD) with two terminals.
2. Device Fabrication

An In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As quantum well heterostructure grown onto an InP substrate (purchased from IQE) has been utilized in this work for the fabrication of high-speed SSDs. The quantum well where the free charge carriers were confined was located 25 nm below the surface, forming a 2-D electron gas (2-DEG) layer, as illustrated in Figure 2(b). The electron mobility and density at room temperature were 10,400 cm$^2$/Vs and $1.3 \times 10^{12}$ cm$^{-2}$, respectively, as determined by Hall measurement.

The device fabrication started with the construction of mesa structures on the substrate using a standard photolithography and wet chemical etching processes. The etching recipe used to form mesa structures was based on the mixture of orthophosphoric acid (H$_3$PO$_4$) solution with concentration of 86 %, deionized water (DIW) and 30 % concentration of hydrogen peroxide (H$_2$O$_2$) solution. The etching rates for GaAs and InAlAs materials were ~ 60 nm/min and ~ 80 nm/min, respectively. Since the materials used in this work consisted of a thin layer of InGaAs embedded in InAlAs, the etching rates cannot be accurately determined. Nevertheless, InP was not etched by this H$_3$PO$_4$/H$_2$O$_2$/H$_2$O-based solution, allowing for a proper formation of mesa structures.

Ohmic contacts on the mesas, in the form of interdigital structure, were then constructed using a standard photoresist lift-off process. The ohmic contacts were formed by thermal evaporation of a 50 nm of Au/Ge/Ni alloy, followed by 200 nm of Au. They were annealed in stages at 110 °C for five minutes, then at 360 °C for four minutes and then at 390 °C for one minute, before they were cooled down slowly.

![Figure 2](image-url)

**Figure 2.** (a) Optical image of the interdigital structure which can accommodate approximately 2,000 SSDs within its fingers. (b) Schematic of the material used in this work. (c) Illustration of the dose-test pattern, which was transferred within the fingers of the interdigital structure. It consisted of five SSDs connected in parallel, each of which has a different channel width, ranging from 350 – 550 nm. The exposure dose was varied from $0.5 \times$ ND to $1.2 \times$ ND. Here, the numbers refer to the dose as a fraction of the nominal dose (ND).
The next step was to fabricate a large number of SSDs connected in parallel within the fingers of the interdigital structure. An experiment has been conducted to obtain the optimum process in fabricating this large SSD array using an EBL technique. A commercial polymethyl methacrylate (PMMA), with a molecular weight (MW) of 950K and diluted in 4% anisole, was used as a masking layer for the EBL operation. This PMMA was spin coated onto the substrate at 4,000 rpm for two minutes. The resulted PMMA film was then baked at 180°C for 3 minutes. The thickness of the PMMA film obtained was between 120 – 150 nm.

Figure 2(c) shows the dose-test pattern for the SSD fabrication which consisted of five SSDs with their channel widths ranging from 350 – 550 nm. The nominal dose (ND) of the EBL system was set with the exposure at 30 kV, and also with area dose and line dose of 600 μC/cm² and 70,000 pC/cm, respectively, using a 10-μm aperture and a working distance of 8 mm. The exposure dose was varied from 0.5 × ND – 1.2 × ND, where the numbers refer to the dose as a fraction of the ND.

This pattern was exposed within the fingers of the interdigital structure. The exposed sample was then developed for 30 seconds using a mixture of methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA) solutions with a ratio of 1:1. Figs. 3(a) – 3(d) show the AFM images of the developed structures. As can be observed, the pattern exposed at 0.5 × ND was marginally well developed, but has a tendency to under exposure. At 0.7 × ND and 1.0 × ND, the patterns were all well defined. The pattern started to show the first sign of over exposure at 1.2 × ND. As can be seen, the boundary lines of the SSD channel marked (1), i.e. 350 nm, were clearly merged. Based on these results, the exposure dose used for the fabrication of a large SSD array of approximately 2,000 SSDs connected in parallel was 0.7 × ND.

In the next step, a Br₂/HBr/HNO₃/H₂O-based chemical solution was used to perform the etching process in order to realize a large array of SSDs. This solution has been developed as the following. A solution of saturated bromine water (SBW) was prepared by adding 3 ml of bromine into 100 ml of DIW. A 0.3 ml of the SBW solution was then mixed with 10 ml of bromic acid (HBr) with 48% concentration. It was observed that the color of this mixture has turned into a light yellow. Then, 5 ml of SBW/HBr mixture was added to 40 ml of DIW, and finally, 5 ml of nitric acid (HNO₃) with 68% concentration was added to the prepared SBW/HBr/DIW solution. This resulting solution was used in

Figure 3. (a) AFM images of SSDs with different channel widths, after being exposed and developed. Note that the darkest region was the exposure area by means of EBL. Here, (1), (2), (3), (4), and (5) refer to the channel widths of 350, 400, 450, 500, and 550 nm, respectively. The devices were exposed using EBL at (a) 0.5 × ND, (b) 0.7 × ND, (c) 1.0 × ND, and (d) 1.2 × ND.
the etching process to form SSD structures, and the etching rate was \( \sim 200 \text{ nm/min} \) for the InGaAs/InAlAs heterostructure utilized in this work.

Figure 4 illustrates the whole fabrication process of SSDs, starting from the blanket InGaAs/InAlAs/InP substrate until the realization of an SSD array. As can be seen, a large array of SSDs can be produced by means of one single nanolithography step only. In fact, this single-step process has enabled the use of cost-effective fabrication methods, such as nanoimprinting lithography (NIL), to manufacture the nanodiodes in a large scale [10]. A multilevel NIL [11] can also be utilized to define simultaneously both the terminal (ohmic) pads and the patterns of SSD array, allowing for denser structures at a lower cost.

In order to merge the SSD arrays located on the LHS and RHS of the interdigital structure, a thermal evaporation process of 100 nm of aluminum has been conducted and the optical image of the merged SSD arrays is shown in Figure 5(a).

Figure 4. Diagrams showing the whole fabrication process of SSDs, starting from the formation of mesa and interdigital (ohmic) structures until the realisation of an SSD array. This process only requires one nanolithography step, which is simpler, faster and at lower cost, compared to other electronic nanodevices. The last diagram illustrates the top view and the cross-sectional (dotted line) of the SSD array fabricated within the fingers of the interdigital structure (ohmic contacts).
3. Results and Discussion
Figs. 5(b) and 5(c) show the etched results of the SSD array. As can be observed, the SSDs were uniformly fabricated within the fingers of the interdigital structure with their channels were approximately 1,500 nm long and 300 nm wide. The width and depth of the etched trenches were 200 nm and 45 nm, respectively. The I-V characteristic of the merged SSD arrays was measured in the dark at room temperature, and the result is shown in Figure 5(d). As expected, a nonlinear I-V behavior of the device can be observed which resembles the characteristic of a typical p-n diode. As can be seen, the turn-on (i.e., threshold) voltage is close to zero which offers several advantages including the ability of the device to perform zero-bias electrical rectification (i.e., biasing circuits are not required) with low noise performance for better responsivity compared to the biased device.

As mentioned earlier, one of the major advantages of SSD is the ability to connect a large number of this device in parallel without the use of interconnection layer by means of a single nanolithography step only. In this case, both SSD arrays on the LHS and RHS of the interdigital structure, each of which has approximately 1,000 SSDs connected in parallel. This feature not only can improve the signal-to-noise ratio (SNR) of the array as the number of SSDs in the array increases [12], but also can avoid introducing undesirable parasitic elements in the interconnection layers which might be challenging for other technologies in the similar field such as high-speed Schottky diodes. This factor, along with the intrinsically low parasitic capacitance of SSD due to its planar structure, has enabled signal rectification using SSDs at high frequencies, as demonstrated previously in refs. [8, 9] using this SSD array.

![Figure 5](image-url)

**Figure 5.** (a) Optical image of the merged SSD arrays. (b) AFM image of a large SSD array which was fabricated within the fingers of the interdigital structure (after etching process). (c) AFM image of two SSDs captured from (b) with higher magnification. The darker areas are the etched trenches of the devices. The channel length and width of the SSDs were 1,500 nm and 130 nm, respectively. The trench width and depth were 200 nm and 45 nm, respectively. (d) I-V characteristics of the merged SSD arrays.
4. Conclusion
To conclude, a nanolithography technique, namely the EBL, has been demonstrated to define a large array of SSDs. The fabricated SSD array shows a typical diode-like characteristic, indicating the capability of this method as a convenient and an alternative tool for patterning not only SSDs but also other electronic devices in nanoscale dimensions including geometric diodes [13], ballistic rectifiers [14], ballistic deflection transistors [15], and planar barrier diodes [16]. Moreover, the fabrication of large SSD arrays might be useful to enhance the devices’ performance as detectors in the terahertz imaging systems as previously reported [17].

Acknowledgement
The authors would like to thank all staff in the Microelectronics and Nanostructures Group from the School of Electrical and Electronic Engineering, University of Manchester, United Kingdom, for their support and technical help. This work is partly supported by the Royal Society-Newton Advanced Fellowship (reference number: NA170415) which is funded as part of the Newton-Ungku Omar Fund.

References
[1] Pfeiffer H 2010 C Proc. of SPIE vol 7823 p 782316-1–782316-6
[2] McCord M A, Rooks M J and Rai-Choudhury P 1997 Handbook of Microlithography, Micromachining, and Microfabrication (Washington: SPIE Optical Engineering Press, Bellingham) vol. 1
[3] Song A M, Missous M, Omling P, Peaker A R, Samuelson L and Seifert W 2003 Appl. Phys. Lett. 83 1881–3
[4] Mateos J, Vasallo B G, Pardo D and González T 2005 Appl. Phys. Lett. 86 212103-1–212103-3
[5] Balocco C, Kasjoo S R, Lu X F, Zhang L Q, Alimi Y, Winner S and Song A M 2011 Appl. Phys. Lett. 98 223501-1–223501-3
[6] Kasjoo S R and Song A M 2013 IEEE Electron Device Lett. 34 1554–6
[7] Kasjoo S R, Hashim U and Song A M 2013 Proc. of IEEE Regional Symp. on Micro and Nanoelectronics (Langkawi, Malaysia) p 297–9
[8] Kasjoo S R, Singh A K and Song A M 2015 Phys. Status Solidi A 212 2091–7
[9] Kasjoo S R, Singh A K, Mat Isa S S, Ahmad N, Nora N I M, Khalid N and Song A M 2016 Solid-State Electron. 118 36–40
[10] Kettle J, Whitelegg S, Song A M, Madec M B, Yeates S, Turner M L, Kotacka L and Kolarik V 2009 J. Vac. Sci. Technol. B 27 2801–4
[11] Lausecker E, Huang Y, Fromherz T, Sturm J C and Wagner S 2010 Appl. Phys. Lett. 96 263501-1–263501-3
[12] Balocco C, Halsall M, Vinh N Q and Song A M 2008 J. Phys. Condens. Matter. 20. 384203-1–384203-5
[13] Zhu Z, Joshi S and Model G 2014 IEEE J. Selected Topics in Quantum Electronics 20 3801409-1–3801409-9
[14] Singh A K, Kasjoo S R and Song A M 2014 Low-frequency noise of a ballistic rectifier IEEE Trans. Nanotech. 13 527–31
[15] Wolpert D, Diduck Q and Ampadu P 2011 IEEE Trans. Nanotech. 10 150–4
[16] Zakaria N F, Kasjoo S R, Zailan Z, Isa M M, Arshad M K M and Taking S 2018 Jpn. J. Appl. Phys. 57 064101-1-064101-7
[17] Balocco C, Pan Y, Kasjoo S R, Alimi Y, Zhang L Q and Song A 2014 Proc. of 39th Int. Conf. on Infrared, Millimeter, and Terahertz Wave (Tucson, AZ, USA)