Triad-NVM: Persistent-Security for Integrity-Protected and Encrypted Non-Volatile Memories (NVMs)

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Abstract—Emerging Non-Volatile Memories (NVMs) are promising contenders for building future memory systems. On the one hand, unlike DRAM systems, NVMs can retain data even after power loss and thus enlarge the attack surface. While data encryption and integrity verification have been proposed earlier for DRAM systems, protecting and recovering secure memories becomes more challenging with persistent memory. Specifically, security metadata, e.g., encryption counters and Merkle Tree data, should be securely persisted and recovered across system reboots and during recovery from crashes. Not persisting updates to security metadata can lead to data inconsistency, in addition to serious security vulnerabilities.

In this paper, we pioneer a new direction that explores persistency of both Merkle Tree and encryption counters to enable secure recovery of data-verifiable and encrypted memory systems. To this end, we coin a new concept that we call Persistent-Security. We discuss the requirements for such persistently secure systems, propose novel optimizations, and evaluate the impact of the proposed relaxation schemes and optimizations on performance, resilience and recovery time. To the best of our knowledge, our paper is the first to discuss the persistence of security metadata in integrity-protected NVM systems and provide corresponding optimizations. We define a set of relaxation schemes that bring integrity-protected NVM systems and provide corresponding optimizations. We define a set of relaxation schemes that bring better trade-offs between performance and recovery time for large capacity NVM systems. Our results show that our proposed design, Triad-NVM, can improve the throughput by an average of 2x (relative to strict persistence). Moreover, Triad-NVM maintains a recovery time of less than 4 seconds for an 8TB NVM system (30.6 seconds for 64TB), which is 3648x faster than a system without security metadata persistence.

I. INTRODUCTION

Securing Non-Volatile Memory (NVM) systems is a critical requirement for their deployment. Unlike DRAM, NVMs retain data after powering off the system, which necessitates encrypting them to avoid data remenance attacks. Moreover, NVMs enable persistent applications which can recover after a crash by frequently persisting their data on NVMs. However, while both concepts, persistency and security, seem orthogonal, they become naturally relevant with emerging NVMs; the system should be able to recover securely and guarantee its data integrity and confidentiality across crashes. Unfortunately, such synergy between persistency and security has received limited attention from the research community, which we believe is due to the following reasons. First, securing memory systems, e.g., encryption and data integrity verification, has been originally developed for DRAM systems to defeat cold-boot attacks [1], [2], [3]. In such systems, persistency and data recovery is not anticipated and thus all security metadata are expected to be reinitialized [4]. Second, the research on encrypting and securing NVMs has been mostly focused on performance of normal-operation without consideration of maintaining consistency across crashes [5], [6], [7], [8]. Third, persisting data in emerging NVMs has many compelling models, notably JUSTDO logging [9] and epoch-based persistence [10], where the focus is on data persistency than its accompanying security metadata [11], [12], [13], [14].

While the Asynchronous DRAM Refresh (ADR) feature has been a requirement for many NVM form factors, e.g., NVDIMM [15], most processor vendors limit persistent domains within the processor chip to tens of entries in the write pending queue (WPQ) [16]. The main reason is the high costs for ensuring a long-lasting sustainable power supply in case of power loss in addition to the power-consuming nature of NVM writes. As security metadata can be hundreds of kilobytes or megabytes, the system-level ADR support would fail to guarantee the persistence of all their updated values within the processor chip. For many users, affording powerfull backup batteries or deploying expensive power-supplies is infeasible, either due to environmental, limited area or cost limitations, thus battery-free solutions are always in demand [17].

Recently, several work have explored persisting encryption counters on secure NVMs [18], [17], [19]. Unfortunately, none of the previous work investigate persisting integrity protected systems and its accompanying metadata, but rather limit their schemes to encryption counters only. In fact, persisting integrity-verification metadata has much higher overhead. Moreover, most of the previous work do not clearly define which security metadata need to be persisted and the impact of relaxing the persistence of such metadata on security, recovery time, resilience, performance and write endurance. In summary, the current literature in persisting security metadata lacks the following: ① Solid definition of what data needs to be persisted in secure memory systems, especially for systems with integrity protection. ② Complete understanding of the...
impact of relaxing security persistence, e.g., selective counter persistence \cite{18}, on security and best practices that must accompany such relaxation schemes. 3) Understanding of the impact of different relaxation schemes on recovery time and resilience of the system, i.e., possibility of recovery failure. To address all these shortcomings, we first discuss the problem of persisting security metadata in integrity-protected secure systems. Later, we define a new concept, Persistent Security, which defines the requirements for securely recovering integrity-protected and encrypted memory systems. Finally, we discuss several relaxation schemes and a comprehensive design that leverages them to optimize performance.

To reduce the overhead of persisting Merkle Tree and encryption counters after each update, we propose Triad-NVM, a novel design that leverages four key insights: 1) Current systems and support for NVM clearly define regions of the NVM device that can be used as persistent memory, e.g., initializing the Linux kernel with the parameter memmap=4G:12G, can be used to dedicate the 4GB starting from address 12GB to be mounted/mapped as persistent memory. 2) Being able to spatially divide the address space into persistent and non-persistent regions allows to partition Merkle Tree vertically into persistent and non-persistent subtrees. While prior work \cite{18} distinguish between persistent and non-persistent data through modifying applications to explicitly hint hardware and memory controller, we observe that such modifications might be not needed if persistent regions are well-defined and spatially distinguishable. 3) Merkle Tree can be reconstructed after a crash by only ensuring the persistence of low levels, however, at the cost of resilience (single-point of failure) and recovery time. 4) Building Merkle Tree for Non-Persistent regions at recovery time can be very expensive, however, it can be mitigated by encoding special values at some levels of the Merkle Tree during recovery.

To evaluate our design, we use Gem5 \cite{20}, a full-system cycle-accurate simulator. We use Linux kernel version 4.14 along with a disk image based on Ubuntu 16.04. Additionally, we initialize the kernel to dedicate the last 4GB (out of 16GB) as a persistent region, which we later mount as a directly-accessible (DAX) ext4 filesystem. The persistent region can be used by any library that supports persistent memory, however, we opt for using Intel’s PMDK library \cite{21} (previously known as PMEM) to build 3 microbenchmarks, in addition to 4 DAX-based synthetic workloads, along with 12 benchmarks from the SPEC2006 suite \cite{24}. We additionally evaluate 4 workloads that run combinations of persistent (PMDK and DAX) and non-persistent (SPEC) workloads. Our simulation results show that Triad-NVM can improve the throughput by an average of 2x (relative to strict persistence). Moreover, Triad-NVM maintains a recovery time of less than 4 seconds for an 8TB NVM system (30.6 seconds for 64TB), which is 3648x faster than a system without security metadata persistence.

The rest of the paper is organized as follows. First, we discuss the problem and background of secure NVM systems in Section \cite{11} where we also discuss the conventional way of persisting security metadata in secure NVMs. Later, in Section \cite{11} we discuss the requirements of strictly-persistent secure memory systems. Later, we discuss different relaxation schemes and their impact on security, performance and resiliency of NVM systems. In Section \cite{14} we discuss our evaluation methodology. Our results and discussion of our evaluation are presented in Section \cite{15} Section \cite{16} discusses the most relevant work to our paper. Finally, we conclude our work in Section \cite{17}.

II. BACKGROUND AND MOTIVATION

We will start our section with background discussion followed by demonstrating the issue of crash consistency of security metadata. Later, we present motivational data of the impact of the problem.

A. Background

Emerging Non-Volatile Memories (NVMs), such as Intel’s and Micron’s 3D XPoint \cite{23}, are just around the corner and they are expected to be on the market soon. Unlike DRAM, they feature high-density, ultra-low idle power (no need to refresh cells), low latency and persistence of data \cite{24}, \cite{25}, \cite{26}. Due to their ability to retain data across system reboots, they can be also used to store files and persistent data structures. Hence, NVMs can be used as a memory and a storage device at the same time. Specifically, NVM-based DIMMs can be used to hold files and also regular memory pages, and can be accessed in a way similar to DRAM through load/store operations. To realize this, new Operating Systems (OSes) started to support configuring the memory as both filesystem and conventional memory. In particular, recent linux kernels and Windows started to support directly-access (DAX) support filesystems \cite{27}. In DAX supported filesystems, e.g., ext4 with DAX, a file can be directly memory-mapped and accessed through typical load/store operations, however, without the need to copy its pages to page cache as in conventional filesystems. For example, the NVM memory can be configured to have a part dedicated to hold filesystem. In linux systems, when initializing the kernel, the parameter memmap=4G:12G can be used to dedicate the 4GB starting from address 12GB to directly-accessible filesystems. Thus, the same memory chip will be accessed for both files and conventional memory pages.

1) NVM Security: Due to non-volatility, emerging NVMs facilitate data remanence attacks; data remains there even after losing power. Accordingly, emerging NVMs are commonly coupled with memory encryption and data integrity verification. State-of-the-art secure NVM systems use counter-mode encryption \cite{6}, \cite{7}, \cite{18}. Counter-mode encryption can protect against replay attacks, scanning memory and bus snooping attacks. Counter-mode memory encryption associates a counter with each 64B block in memory and this counter changes each time the corresponding block is being written to memory and the new counter value will be used to do the encryption. The most-recent value of the counter must be book-kept to be later used for decryption. In counter-mode encryption, repeating the same counter value can result in serious security vulnerabilities, e.g., known-plaintext attacks. To avoid replaying counters, they are typically protected against tampering through Merkle Tree. State-of-the-art work, e.g., Bonsai Merkle Tree \cite{4}, applies Merkle Tree over the encryption counters and protects data through computing MAC value over ciphertext and data.
As shown in Figure 1, each encryption counter, which is associated with a data block, is used to calculate a hash value (MAC) that will be used along with other hash values from other groups of counters to create a lower level hash value. Finally, the resulting MAC value, which is called root, is kept in the processor. Each time a counter is brought from the insecure area, e.g., memory module, it will be verified by calculating the upper hash values and see if the result matches the root kept in the processor. Furthermore, when the processor writes a memory block and updates the corresponding counter, the Merkle Tree intermediate nodes and root should be updated to reflect the most-recent change.

2) Memory Counter-Mode Encryption: In counter-mode encryption, the encryption algorithm, e.g., AES, takes initialization vector (IV) as its input to create a one-time pad (OTP) as explained in Figure 2. Later, when the block arrives the processor chip, a low-cost bitwise XOR with the pad (encrypted IV) is needed to obtain the plaintext. By doing so, the decryption latency is hidden by the memory access latency. In our paper, we use state-of-the-art design for organizing encryption counter, split-counter scheme [6], [4], where each IV consists of a unique ID of a page (to distinguish between swap space and main memory space), page offset (to guarantee different blocks in a page will get different IVs), a per-block minor counter (to make the same value encrypted differently when written again to the same address), and a per-page major counter (to guarantee uniqueness of IV when minor counters overflow).

As in previous work [6], [18], [17], [28], [4], [7], we assume counter-mode memory encryption. In addition to its performance advantages, it also provides strong security defenses against a wide range of attacks. Counter-mode encryption is secure against dictionary-based attacks, known-plaintext attacks, bus snooping and replay attacks. In split-counter scheme, the encryption counters are organized as major counters (shared between cache blocks of the same page) and minor counters that are specific for each cache block [4]. Such organization allows packing 64 cache blocks’ counters in a 64B block; 7-bit minor counters and 64-bit major counter. Major counters are incremented when one of its minor counters overflows, in which all corresponding minor counters will be reset and the whole page will be re-encrypted using the new major counter [4]. When the major counter of a page overflows (64-bit counter), a new key is generated and the memory contents will be re-encrypted using the new key. Split-counter scheme provides significant reduction of memory re-encryption rate and minimizes the storage overhead of encryption counters when compared to other schemes, e.g., monolithic counter scheme or independent counter for each cache block. Moreover, split-counter exploits the spatial locality of encryption counters, and hence achieves a higher counter cache hit rate. Similar to state-of-the-art work [6], [29], [5], [4], we use split-counter scheme for organizing the encryption counters.

3) Impact of Persistency on Security: As persistent memory can be utilized to store checkpoints and recover from crashes, the accompanying security metadata should be persisted too. For instance, we mentioned earlier that the counter used for encryption will be updated on each write operation of the associated memory block, however, such update can occur on a volatile counter cache inside the processor chip, hence not persisted to the NVM memory. Accordingly, the data block could be encrypted with the new counter value and written to NVM, but the counter is not updated in memory. Clearly, if a crash occurs, a stale counter value will be used to do the decryption, which will result in incorrect decryption. While the recovery of non-persistent data is not important, it is critical to avoid reusing their counters’ previous values; repeating an old (not persisted) counter will result in a reuse of OTP that could have been observed earlier, which results in security vulnerabilities as described below.

4) Attack on Reusing Counters for Non-Persistent Data: As described by Ye et al. [17], assume an adversarial application uses known-plaintext and writes it to memory, however, if the memory location is non-persistent, the encrypted data will be written to memory but the counter might be not updated in
memory yet. By observing the memory bus, the attacker can learn the encryption pad, i.e., OTP, by XOR’ing the observed ciphertext, \( E_{key}(IV_{new}) \oplus Plaintext \), with the Plaintext. Even worse, it is also possible to predict the plaintext for initial accesses, for instance, zeroing at first access. To this end, the attacker knows the encryption pad, i.e., \( E_{key}(IV_{new}) \). Later, after recovering from a crash, the memory controller will fetch \( IV_{old} \) and increment it, which generates \( IV_{new} \), and then uses it to encrypt the new data written to that location to become \( E_{key}(IV_{new}) \oplus Plaintext' \). As the attacker knows the encryption pad, revealing the value of Plaintext'2 only can be done by XORing the ciphertext with the previously observed encryption pad, i.e., \( E_{key}(IV_{new}) \). Note that the stale counter could have been incremented multiple times before the crash, hence multiple writes of the new application can reuse counters with known encryption pads. Note that such an attack only need a malicious application to run (or just predictable initial plaintext of an application) and having a physical attacker.

B. Security Metadata Crash Consistency

After a crash occurs, the system must be able to recover and restore its encrypted memory data along with its accompanying security metadata. Figure 3 discusses the logical steps needed for crash consistency as described by Ye et al. [17].

Fig. 3: Description of write process that ensures crash consistency.

As depicted by Figure 3, the root of the Merkle tree (on-chip) should be updated/persisted (as shown in step 1) along with affected intermediate nodes inside the processor. However, only the root of the Merkle Tree needs to be kept in the secure region.

In step 2, the updated counter block is written back to memory as it gets updated in the counter cache. Counters are critical to keep and persist to avoid having the security of the counter-mode encryption be compromised. Note that even if the data is not expected to be recovered, the counters must be persisted to avoid repetition. While losing counter values can cause inability to restore encrypted memory data, Liu et al. [18] observe that it is possible to only persist counters of persistent data structures (or subset of them) to enable consistent recovery.

Unfortunately, this can lead to serious security vulnerabilities as discussed earlier; reusing counter values even for non-persistent memory locations can compromise the security of the counter-mode encryption. Moreover, modifying applications to expose their persistent ranges to the memory controller is challenging, especially for legacy applications.

Finally, in Step 3, the written data block will be sent to the memory.

C. Motivation

As we now understand the issue of guaranteeing security metadata crash consistency, let’s now discuss the impact of ensuring such consistency on performance of Non-Volatile Memories (NVMs). As mentioned earlier, a strictly persistent secure system would persist any changes to Merkle Tree and the corresponding encryption counter before each memory write operation. Figure 4 depicts the relative system throughput when using strict persistent security.

As shown in Figure 4, most workloads get severe performance degradation due to the impact of additional write operations to ensure persistency of security metadata. Notably, some workloads can be slowed down by as much as 9.4x compared to a system that does not guarantee such type of persistency. The impact of persisting security metadata depends mainly on the memory behavior and write-intensity of the running applications. Unfortunately, with such performance overheads, most users would avoid enabling persistent security which would leave their systems insecure and potentially their data unrecoverable. To address this issue, in this paper, we define the requirements of persistently-secure systems and study the impact of different schemes on performance, recovery time and resilience of the system. To the best of our knowledge, our paper is the first to discuss the issue of persisting both encryption counters and Merkle tree in NVM-based systems.

III. DESIGN

In this section, we first define the requirements of persistently secure systems. Later, we discuss the different design options that can be adopted for the purpose of implementing persistently secure systems. Finally, we discuss our proposed design that combines several novel optimizations.
A. Persistently Secure Systems

In order to start our discussion of the requirements of persistently secure system, let’s first formally define such systems.

**Definition 1:**
A Persistently Secure System is any secure system that is capable of recovering its security metadata, e.g., encryption counters and Merkle Tree, in case of power-loss or system crash. Such a system should be able to verify that any (persistent) memory data being read after the crash reflects the most-recent value before or after system recovery. Specifically, if using counter-mode encryption, such a system should guarantee that one-time pads are never repeated regardless of the nature (persistent or non-persistent) of their corresponding data.

As mentioned earlier, state-of-the-art designs for secure NVMs deploy counter-mode encryption along with an optimized Merkle Tree that protects tampering with data and encryption counters. Two key requirements for such schemes

1. **Encryption Counters:** While losing the most recent values of encryption counters of non-persistent data structures or data would likely not affect the correctness of the system, it can compromise its security as discussed earlier. Accordingly, to prevent such security vulnerability, encryption counters should be strictly persisted or there must be a guarantee of not repeating one-time pads.

2. **Merkle Tree:** Persisting Merkle Tree updates is necessary to ensure the system ability of verifying encryption counters when recovered. However, we observe that not all parts of the Merkle Tree need to be persisted. Instead, just persisting the lowest levels of Merkle Tree is sufficient to rebuild the whole Merkle Tree at the time of recovery, however, at the cost of creating a single-point of failure and increasing recovery time as we will discuss later.

1) **Encryption Counters Persistence:** Encryption counters of persistent data must be updated strictly before updating the data to ensure consistent recovery of data. Meanwhile, as also observed by Liu et al. [18], counters of non-persistent data do not need to be strictly persisted. However, while prior work completely relaxes the persistence of such counters, we argue that we additionally need to ensure that such counters should never repeat with the same encryption key. Later, we will discuss a scheme that relaxes counters of non-persistent data while ensuring that they will never repeat. Meanwhile, the encryption counters of persistent data will be strictly persisted before updating their corresponding data.

**Observation 1:** Encryption counters of persistent data must be persisted and up-to-date during normal operation and across system failures/crashes. In contrast, for non-persistent data, the encryption counters must be up-to-date during normal operation and guaranteed not to repeat old values after recovering from crash.

2) **Merkle Tree Persistence:** While Merkle Tree covers all encryption counters, regardless of their persistence requirements, not all parts of the Merkle Tree need to be persisted. Specifically, given that current systems define the persistent regions of the NVM during bootup time, there is a range in memory that is guaranteed not to be used for persistent data. For instance, if the Linux Kernel defines the first 4GB of memory to be used for persistent memory, i.e., can be mounted and used by PMEM and DAX applications, then other parts of the memory do not ensure any persistence of data. Thus, persisting the updates to Merkle Tree intermediate nodes that only cover non-persistent regions might be relaxed as long as this ensures integrity during the normal operation.

**Observation 2:** For non-persistent data, it is important to ensure their integrity during run-time, however, after a crash, we are no longer concerned about their values being lost or tampered with. In contrast, for persistent data, the data and counters integrity must be ensured during normal operation and across system failures/crashes.

Based on the above observation, a Merkle Tree can be subdivided into multiple subtrees, i.e., some parts only cover...
the first 4GB of the main memory as aforementioned, hence only that part of the tree needs to be persisted strictly. In other words, the Merkle Tree can be vertically divided into persistent and non-persistent tree. We also observe that just persisting the leaves of the Merkle Tree is sufficient to allow its reconstruction, however, this can increase the recovery time and create single-point of failure, which would require additional fault isolation mechanisms.

### B. Relaxed Schemes

In this part of the paper, we will discuss several optimizations and their potential impacts.

1) **Relaxed-but-Secure Persistence of Encryption Counters:**

To understand this scheme, let’s first discuss how current systems adopt persistent memory. In current systems, at the time of bootup, the kernel is initialized with a value that determines which range of the memory module is considered persistent. Such region can be formatted and mounted as a filesystem, e.g., ext4 filesystem. Additionally, such persistent region can be used by persistency APIs, such as PMDK, which would backup the persistent data structures by files in the persistent region. Any file in the persistent region can be memory-mmaped, i.e., `mmap`ed, and accessed through typical load/store operations. Meanwhile, the non-persistent region in the NVM device is not ensured recoverability after a crash; an application will only be able to access data persisted to the persistent region after recovery. Figure 5 depicts a system with encryption counters of persistent and non-persistent regions in an NVM device. Note that such distinction between persistency of regions does not require modifying applications to explicitly define persistent data structures and expose them to hardware as in prior work [18].

As we now understand how future NVM devices will be leveraged by OS, let’s now discuss how encryption counters should be treated differently based on that. While encryption counters of persistent data must be recovered correctly for both correctness and security reasons, those of non-persistent data can be relaxed from ensuring correctness after recovery. The only requirement of encryption counters of non-persistent data is that they should not produce a previously used one-time pad, which we can ensure by using a different encryption key.

Based on our observation that non-persistent data can lose their most-recent counter values after recovery, however, they should be never reused with the *same key*, we devise a design that uses two different keys. One key, which we refer to by *Persistent Key*, and the other key which we refer to by *Volatile Key*. The persistent key is used for encrypting/decrypting persistent data regions, whereas the volatile key is used for non-persistent data. The volatile key will be changed after each system reboot or recovering from crash, which allows us to securely relax the persistence of encryption counters of non-persistent data. Our design only requires modifying the memory controller to be able to receive a command from the kernel which notifies the MC about the start and end address of the persistent region, and to use such information to decide which key to use. Moreover, the kernel needs to send the memory controller, through a memory-mapped register, a command to change the volatile key at the time of recovery or reboot.

**Observation 3:** In systems with persistent and non-persistent regions, if counter-mode encryption scheme is employed, separate keys can be used for each region. As encryption counters of the non-persistent region can repeat due to optional persistence necessity, the key used for such region must be changed after recovery or system reboot. By doing so, even if the same IV gets reused, the one-time pad will be different: $E_{key_1}(IV) \neq E_{key_2}(IV)$. Thus, updating encryption counters of non-persistent data can occur in counter-cache and use a write-back scheme instead of write-through.

2) **Relaxed-Persistence Subtrees of Merkle Tree:** As we have discussed in the prior part, some parts of the memory are not expected to recover data correctly after a crash. However, such regions require that their integrity be protected during normal run-time, but do not have any expectation of integrity-protection after recovery from crash as the data will be discarded anyway. To better understand how an optimized scheme that relaxes persistence of non-persistent sub-trees of Merkle Tree, Figure 6

![Fig. 6: Updating Merkle for counters correspond to data with different persistency requirements.](image-url)
shows how Merkle Tree can be updated based on the persistency requirement of the underlying data.

As depicted in Figure 6 when an update occurs for a persistent memory location, all the corresponding parts for such location in Merkle Tree at all levels should be updated up to the root (inside the processor chip). Updates to Merkle Tree for persistent data should be updating both the memory copy and the cache copy of (1) The root of the Merkle Tree, (2) The root’s child node that owns the updated counter, and all other intermediate nodes correspond to the updated counter. Finally, as in (4), updating the counter in both the memory and counter cache. Note that, for non-persistent data, updating the intermediate nodes and counters in the cache and lazily write it back to memory is sufficient. Clearly, the subtrees that belong to persistent regions should be separable, i.e., some parts of the root only belongs to persistent-region and others only to non-persistent regions. Having some parts belong to both is challenging can lead to unverifiable parts after recovery; that part will reflect most-recent values of both types of data, but we will be unable of reproducing the root due to the lost updates of intermediate nodes and counters of non-persistent data. The only level that has MAC values on the same block for both persistent and non-persistent data is the root, however, they are clearly separable. To avoid cases of MAC values cover both types of data, the memory space ratio between persistent and persistent-data should 0:8, 1:7, 2:6, 3:5, 4:4, 5:3, 6:2, 7:1 or 8:0. In other words, each MAC value in the root should cover either persistent or non-persistent data but not both. Note that updates to the root does not need to be updated in memory as it is guaranteed to be persistent in the processor, i.e., in a NVM register inside the processor.

Observation 4: Merkle Tree can be logically divided into subtrees that either belong to persistent data or non-persistent data. Due to the architectural layout of the tree, the ratio of persistent to non-persistent data is limited to specific values that guarantee each MAC value in the root belongs to either persistent or non-persistent data. To this end, the Merkle Tree subtrees that belong to the non-persistent ranges can be updated in the MT cache and lazily updated in memory when written back.

3) Bottom-Up Merkle Tree Persistence: As we discussed in the previous part on how to divide Merkle Tree vertically into persistent and non-persistent subtrees, we now will discuss which levels of Merkle Tree need to be updated and the impact of possible relaxation schemes.

Unlike encryption counters, Merkle Tree intermediate nodes can be rebuilt if lost and their main use is to speed up verification and updating the root of the Merkle Tree. However, if encryption counters are guaranteed to be strictly persistent and up-to-date, then after a crash it is possible to rebuild all levels of intermediate nodes all the way up to the root which needs to match the root value in the processor. While this looks like a straightforward optimization, it can actually create a single-point of failure; if any counter has been corrupted, e.g., due to memory error, we can only know that the Merkle Tree root has not matched and thus none of the memory is integrity-verifiable. While a Merkle Tree root can hold 64B instead of only 8B values, still an uncorrectable counter error would result in a third of the memory being lost/unverifiable. As emerging NVMs are expected to contain terabytes of data, the chance that an uncorrectable error of any counter can lead to large part of memory being unverifiable is unacceptable. Moreover, only guaranteeing the persistence of encryptions would require high recovery time due to the need of iterating over all encryption counters to rebuild all levels of Merkle Tree.

To enable high-resolution of identifying unverifiable locations in addition to keep the recovery time manageable, we propose persisting the first $N$ levels of the Merkle Tree (from bottom to up) while optionally maintaining several NVM registers within the processor. The value of $N$ depends on the acceptable performance/recovery-time trade-off. Persisting low levels of Merkle Tree can help isolating problems and identifying which counters are corrupted/uncorrectable. Moreover, more number of levels being guaranteed persistence allows shorter recovery time to reconstruct the Merkle Tree. Also note that since higher levels of the Merkle Tree has much less intermediate nodes, persisting them reduces the chances of the inability to construct Merkle Tree due to uncorrectable errors.

Observation 5:
Persisting parts of the Merkle Tree can avoid single-point of failures resulting from uncorrectable errors of encryption counters. Moreover, it reduces the Merkle Tree recovery time by reducing the number of levels need to be rebuilt after recovery. Internal NVM registers inside the processor can be also used to hold upper levels of Merkle Tree, e.g., root’s immediate children and grand children (a total of 73 blocks), thus it can declare only a small percentage of memory unverifiable in case uncorrectable errors corrupt encryption counters or the persisted parts of the Merkle Tree.

C. Triad-NVM

Our design that includes all of the proposed optimizations is referred to as Triad-NVM. Triad-NVM logically divides the Merkle Tree into subtrees, persistent and non-persistent. Moreover, it strictly persists counters that belong to persistent regions. Finally, for persistent regions, the Merkle Tree must be reconstructed after crash, thus it is necessary to ensure resiliency through persisting additional levels as configured by system owner or recommended by the system architects. For non-persistent regions, there is no need to ensure reconstruction of the corresponding subtree of the Merkle Tree, thus updates to such subtree are not strictly persisted.

At the recovery time, the Merkle Tree has to be reconstructed again to be able verify any tampering. During recovery, before admitting the current status of the system as verified, all persistent locations need to be verified through reconstructing the corresponding parts of the Merkle Tree and verifying that it generates a correct root. This ensures that the data has not been tampered with from (or before) crash time till recovery time. However, for non-persistent data locations, while we do not need to verify the integrity of data at the recovery time, we need to be able to verify it after recovery. Thus, Merkle Tree subtrees that correspond to non-persistent regions should
be constructed. Now the question is how can we do that in an efficient way.

**Reconstructing Subtree of Non-Persistent Region:** As mentioned earlier, in state-of-the-art schemes, e.g., Bonsai Merkle Tree [28], the MAC values stored with data are calculated over data and encryption counters and hence all data and its accompanying MAC values need to be reinitialized based on the updated counter values after recovery. Note that since persisting updates to Merkle Tree and counters of non-persistent data is relaxed, there is no guarantee that the recovered counter values are similar to those used to calculate the MAC values accompanying their corresponding data. Accordingly, there will be inconsistency that will result in errors and mistakenly flagging tampering/errors during normal operations after recovery.

Unfortunately, it is very time-consuming to iterate over all non-persistent data to reinitialize counters, data and its MAC values. To better understand the overhead, let’s assume a 6TB of NVM, where 50% is used as non-persistent data, i.e., normal memory. At recovery time, if reading each data block and initializing it takes 100ns, then just iterating over the 3TB (non-persistent region) would take 5154 seconds (almost 85.9 minutes). However, for the persistent data (the other 3TB), since the low-levels of Merkle Tree along with data and counters have been strictly persisted, only the upper levels of Merkle Tree. For instance, if only the first level of Merkle Tree (the parents of counter blocks), and reading each block and calculating its MAC values takes 1000ns, then that will take only 92 seconds (1.5 minutes). For more aggressive persistence of Merkle Tree such as up to level 2 (the grandparents of counter blocks), then the construction time will take only 11.5 seconds.

**Observation 6:**

Relaxing the persistence of Merkle Tree parts and counters that correspond to non-persistent data can result in significant increase in recovery time. Unfortunately, given the significant costs of system downtime (hundreds of thousands per minute [30]), completely reconstructing counters and Merkle Tree parts of non-persistent data at the recovery time can lead to unanticipated system unavailability.

To avoid an unanticipated long recovery time of rebuilding counters and Merkle Tree parts of non-persistent regions, we additionally propose **Lazy Recovery of Low-Levels of Non-Persistent Merkle-Tree.** As the number of counter and data blocks is the largest and they consume most of the rebuilding time, we can lazily update them as following. By initializing all intermediate nodes at level 1 (parents of counter blocks) with zeros, and constructing all upper levels sequentially, we can obtain an initial root value (or part of root) for non-persistent data. Later, any update for any counter value, if the parent intermediate node has a zero value, we do not flag an error or tampering as the upper levels of Merkle Tree (and root) are already updated to reflect such value, however, we know that this is the first write to the counter block after recovery and hence we zero out (or initialize) the counter value and update the parent node accordingly. Note that since each counter block has its MAC value stored in 8 bytes of the 64B parent node, only the corresponding 8B in the parent node would indicate if it is the first update after recovery or not. While the odds that a counter block value would naturally lead to 64-bit zero value is only $\frac{1}{2^{64}}$, to avoid falsely assuming an initialized counter value, if a counter block naturally has a MAC value of 0, we re-encrypt one of its cachelines and accordingly increment its minor value and calculate its new MAC value and use it to update the parent block if new MAC value does not equal to 0. By lazy update of non-persistent data and counter blocks, we ensure a recovery process that only needs to iterate over levels 1 or 2 instead of all corresponding data and counter blocks.

![Fig. 7: High-Level Overview of Write Operation on TriadNVM.](image)

Figure 7 depicts the Triad-NVM design. As mentioned earlier, Write-Pending Queue (WPQ) is considered part of the persistence domain (power-fail protected domain) in modern processors [16]. Thus, anything reaches there should be consistent or there is a way to ensure its consistency. To do so, each write operation, before being persisted (removed from volatile buffer), it logs all its corresponding updates (counter, data, MT nodes and root) to persistent registers inside the processor and then set a persistent bit (called READY_BIT). If a crash occurs while copying the updates in persistent registers to WPQ, then when the system restores the memory controller will attempt to write the persistent registers to NVM (or WPQ) again. At the time of copying the contents from the registers to WPQ, Triad-NVM selectively chooses if the counter or Merkle Tree nodes should be copied to WPQ or it is just enough to update them in caches (as shown in steps 8 and 9). Note that once a dirty block gets evicted from these caches it will go to WPQ as usual. Persistent registers can be implemented as fast NVM registers or volatile registers will be flushed to slower NVM registers once a crash occurs through leveraging ADR or residual power. The number of persistent registers depends on the Triad-NVM model, e.g., if TriadNVM-2 is used then we only need 5 registers, whereas if we use the impractical strict persistence then we might need up to 15 registers. Note that using persistent registers have been also assumed in state-of-the-art work [17].

If the updated encryption counter corresponds to a persistent memory region, it will be strictly updated (copied to WPQ).
However, for Merkle Tree, if the updated parts belong to a persistent memory region and in a level higher than the persist level, then the updates will be persisted to NVM (copied to WPQ). Note that the persist level is the highest level of Merkle Tree that is guaranteed to be strictly persisted, e.g., if such a level is 2, then counters, their parents and grandparents are guaranteed to be persisted after each update. Note that TriadNVM recovery process is as simple as iterative over the intermediate notes at the persist level and construct the upper levels of the persistent memory regions, however, additionally initialize the intermediate nodes of such level to zeros for non-persistent memory regions before constructing their upper levels of the tree.

IV. METHODOLOGY

In this section, we describe our evaluation methodology. Since our work involves kernel modifications and both persistent and non-persistent applications, we use Gem5 simulator[20] in its full-system mode. The kernel we simulate is based on Linux Kernel 4.14. Moreover, the disk image we use is based on Ubuntu 16.04 distribution. The kernel was initialized with configuring the 4GB starting from 12GB as a persistent region, e.g., the kernel was initialized with memmap=4G!12G. Later, the persistent regions was formatted with DAX-enabled ext4 filesystem and mounted to be used by persistent applications and libraries. Table I presents the architectural configurations of our simulated system:

| Processor                          | Capacity | PCM Latencies | Organization                                                                 |
|------------------------------------|----------|---------------|------------------------------------------------------------------------------|
| CPU                                | 16 GB    | 60ns read, 150ns write | 2 ranks/channel, 8 banks/rank, 1KB row buffer, Open Adaptive page policy, RoRaHaChCo address mapping |
| L1 Cache                           |          |               |                                                                               |
| Cache                              |          |               |                                                                               |
| DDR-based PCM Main Memory           |          |               |                                                                               |
| Counter Cache                       |          |               |                                                                               |
| Merkle-Tree Cache                   |          |               |                                                                               |
| Merkle-Tree                         |          |               |                                                                               |

To evaluate the impact of our proposed optimizations, we run 3 sets of workloads: persistent applications, non-persistent applications and a combination of both. For the benchmarks being used, following is the description of the major applications followed by Table II which shows the mixed workloads we use. For non-persistent workloads, we use representative benchmarks from SPEC2006[22]. We also implement persistent Hashtable, ArraySwap and Queue benchmarks using Intel’s PMDK library. Additionally, we implement synthetic benchmark, DAXBENCH-S-RW that leverages DAX to mmap a file directly in the persistent region and access it through memory load/store operations with S stride and RW read to write ratio. Finally, we use those benchmarks to create multi-programmed workloads to enable studying the optimizations that relax persistence of security metadata for non-persistent data applications.

V. EVALUATION

In this section, we evaluate our proposed optimizations and study the impact of combining them on Triad-NVM. We will first study the impact of each optimization on performance, and later study and analyze the trade-off between recovery-time and performance overhead when relaxing the persistence of Merkle Tree.

A. The Impact of Relaxation Schemes on Performance

Figure 8 shows the impact of Triad-NVM on performance. TriadNVM-N represents TriadNVM with strict persistence of persistent regions up to the Nth level of the Merkle Tree. As expected, for the persistent region, TriadNVM-1 is expected to perform better than TriadNVM-2 and TriadNVM-3. The main reason for that is that less number of writes need to occur to memory to ensure strict persistence of Merkle Tree, i.e., in TriadNVM-1 only the parent of the updated counter block needs to be persisted along with the counter block, whereas in TriadNVM-2 both the parent and the grandparent of the updated counter block need to be persisted along with the counter block. Clearly, there will be no difference between different TriadNVM persistence levels for non-persistent workloads, e.g., LBM and MCF. Moreover, in mixed workloads, only the writes to persistent regions will make difference between TriadNVM models.
Our results show that using strict persistence scheme can lead to an average of 2.21x slowdown, whereas TriadNVM-1, TriadNVM-2 and TriadNVM-3 lead to only 4.9%, 10.1% and 15.6% performance overheads, respectively. Moreover, we observe that write-intensive workloads with non-persistent region allocations, e.g., Libquantum, can get an almost order of magnitude speed up when using schemes that are aware of persistent regions and thus relax the requirements of non-persistent memory ranges.

As mentioned earlier, one major shortcomings of the emerging NVMs are their slow writes and limited write endurance. However, while ensuring higher level of persistence would possibly reduce the recovery time and also avoid single-point of failures, it can excessively increase the number of writes. However, more relaxed schemes, e.g., TriadNVM-1, would lead to additional recovery time and potentially single-point of failure, however, it incurs smaller number of extra writes.

The Impact of Merkle Tree Persistence on Recovery Time

As resilience of the system is also important, TriadNVM-2 and TriadNVM-3 provide a higher resolution of pinpointing errors. In TriadNVM-2, if calculating the MAC values starting from level 2 does not eventually generate the root value stored in the processor, then TriadNVM restarts form level 1 and find out which node in Level 2 does not match with that calculated from its children, and hence only declaring the corresponding 32KB as unverifiable. Note that the root must match with that
generated from those in Level 1, before declaring that Level-2 node to be the source of error. Similarly, if an uncorrectable error occurs in Level-1 nodes, while Level-2 nodes ended up generating the same root value, i.e., verified, then we can use Level-2 nodes to pinpoint which Level-1 node is the corrupted one. TriadNVM-3 follows the same logic but now add an additional level of isolation in case uncorrectable errors occurred on both Level 1 and Level 2. It is also important to note that since the number of levels of Level-2 and Level-3 are 8 and 64 times, respectively, smaller than that of Level-1, then the chances of uncorrectable errors on them is also smaller.

VI. RELATED WORK

Persisting security metadata has been rarely studied up until recently. Recent work [13] proposed selective persistence of encryption counters without any discussion of how Merkle Tree persistence can be handled. Moreover, as discussed earlier, selective encryption counter is vulnerable to known-plaintext attacks as it allows the reuse of encryption counters for non-persistent data. In contrast, our work takes a more holistic approach of studying all relevant security metadata and discuss their persistence impact on recovery-time, resiliency and performance. Additionally, we propose solutions to mitigate such overheads and to protect against potential repetition of one-time pad.

Recently, Zuo et al. [19] proposed combining multiple updates of encryption counter block into one write to memory, especially for large transactions. Unfortunately, such a solution works only well if we can predict the spatial locality of writes to memory, which is typically hard to predict as they can result and interfere with evictions/write-hacks from the Last-Level Cache (LLC). Thus, such a solution would be beneficial only when many writes to memory are spatially contiguous and occur at relatively close time. In contrast, our solutions are generic and do not expect any special behavior from workloads. Additionally, we investigate Merkle Tree persistence, which has not been discussed or explored in any of the previous work we are aware of. Nevertheless, SecPM can be orthogonal to our proposed solutions. Another recent work explore repurposing Error-Correcting Codes (ECC) to be additionally used as a sanity-check for the encryption counter [17]. By doing so, Ye et al. [17] propose a novel scheme that can be used to relax the persistence of encryption counters and rely on restoring it through trying several values until ECC match or indicate natural number of errors. Our work is orthogonal to Osiris and can be integrated with it to reduce the number of writes to persist counters in the persistent memory regions.

Persisting data in NVMs have different models based on the required software and hardware changes [31], [10], [32], [33]. Several APIs and libraries have been developed for the purpose of persisting data in emerging NVMs and utilizing the OS support for PMEM, e.g., Intel’s PMDK [21]. In this paper, our support focuses on persisting security metadata accompanying persistent data when being written to NVM, and thus we do not require any changes at application or library level, hence Triad-NVM can be integrated with most persistency models. Other works that target reducing NVM writes have not considered the problem of persisting security metadata [6], [7]. All of these solutions can employ TriadNVM to ensure persistence and recoverability of security metadata.

VII. CONCLUSION

In this paper, we propose TriadNVM, a set of schemes that enable efficient, resilient and performance-friendly recovery mechanism for security metadata. TriadNVM ensures the persistence of Merkle Tree and encryption metadata while incurring minimal overheads. Moreover, TriadNVM can be customized to different modes based on the desired recovery-time/performance trade-offs.

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