Design of RLC Circuit Parameter and Fault Location Test Device

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Abstract. In order to improve the quality and performance of electronic equipment, circuit parameters and fault detection technology are also very important. The impedance value, which differs obviously under different input signals in the analog circuit, is also an important parameter. Through the analysis of this parameter, RLC circuit parameters and fault location detection can be realized. In this paper, STM32 is used as the main controller to control the signal source to generate sinusoidal signal. The signal processing is completed by designing the amplifier module, and the signal acquisition is completed by the digital to analog conversion module. In the controller, the impedance analysis, the measurement of component parameters, the detection of load network structure and the measurement of short-circuit point position are completed. Finally, the designed system was used to test different structural loads, and the detection results of component parameters, load network structure and short-circuit point position are accurate and reliable.

1. Introduction
With the development of circuit design and manufacturing technology, the overall structure complexity and scale are increasing, and the possibility of failure is also increasing. Especially in the long-term operation of the circuit, the components in the circuit will be gradually aging and fail. Failure will affect the normal operation of the circuit [1]. Therefore, the fault detection and diagnosis of the circuit is an important part of the circuit design [2]. Resistance, capacitance and inductance are the three most widely used components in electronic circuit system, and the accuracy of these three components parameters plays a very important role in the stability of the circuit. It is necessary to design an accurate and reliable resistance, inductance and capacitance tester [3].

2. Overall design scheme
The device, shown in Figure 1, has two ports connected to the external load, and the distance from point A is between 20cm and 50cm. The load is composed of capacitance, inductance and resistance in series and parallel. The parameter values of the energy components of the device can detect and display the load network structure, measure the parameter values of individual components, detect the open and short-circuit faults of the load, and measure the location of the short-circuit faults when a short-circuit occurs.
The load parameters and fault detection are implemented by measuring the impedance and phase angle of the load. The overall system is shown in Figure 2.

The system is divided into three parts: excitation source, signal conditioning and signal acquisition. The signal source part has a constant current source, signal generator, amplifier, relay module, which mainly completes signal generation and switching. The signal conditioning part mainly consists of differential amplifier module, voltage follower module and root mean square detection module. It mainly completes the conditioning of the excitation source signal to get the signals at both ends of the load that can be collected by the controller. The signal acquisition module mainly includes display module, control module and ADC module. It mainly completes the signal collection, the control of the excitation source and the display of the results.

3. Design of System Hardware
The hardware design of the device mainly includes the selection of the main control chip, the design of the excitation source part, and the design of the signal conditioning part. The main control chip uses STM32F407ZGT6, which has sufficient on-chip resources to implement more complex floating point operations \(^{[4-5]}\). It also can meet the functional requirements of the device.

3.1. Design of excitation source module
When the circuit is working normally, the sinusoidal signal generator module is used to drive the circuit. A constant current source drive circuit is used to measure the position of the short circuit point. Two excitation sources are switched by relays.

3.1.1. Configuration of sine signal generator module
The signal generator part of the device uses the digital frequency synthesizer AD9959 module, which is composed of four DDS (Direct Digital Synthesis) cores. The amplitude, frequency and phase of the output sine signal can be independently controlled in each of the four DDS channels, which means it can linearly scan and modulate frequency, phase and amplitude, even up to 16-order amplitude, frequency or phase modulation \(^{[6]}\).
The AD9959 module is connected to the microcontroller through the user interface, and the functional diagram is shown in Figure 3. P0-P3 is the interface of modulation signal; SDIO_0-SDIO_3 is used for serial communication; CS is a slice selection signal. Slice selection allows multiple AD9959 devices to be located on the same set of serial communication lines. Low level effective; SCLK is a serial clock signal; PWR_DWN_CTL is an external power-off control; I/O_UPDATE is an update register signal[7-8].

Figure 3. AD9959 Module Function Diagram

Figure 4 is a sequence diagram of when I/O port data is transferred from a buffer to a register. I/O_UPDATE and the SYNC_CLK control together the register that transfers data from the serial I/O buffer to the device[9]. Data are invalid in buffer in initial state. Synchronized Clock The SYNC_CLK is a 4-way frequency division of the system clock, which is used to synchronize external hardware with the internal clock of AD9959. The SYNC_CLK rising edge is valid. When the I/O_UPDATE rise edge arrives, the buffer transfer starts[10].

Figure 4. Time Series Diagram of I/O Port Data Transfer

3.1.2. Design of constant current source module
The controlled precision regulator TL431 can set 2.5V~36V output voltage. The working current can be 1~100mA. The typical dynamic impedance is only 0.2. The voltage reference error is 0.4%, and the output voltage ripple is low[11].

Constant current source is constructed using TL431 and triodes. The circuit diagram shows in Figure 5. Current feedback is introduced into the circuit, and the voltage at the reference end will be stable at 2.5V, so the current flowing through the resistance at between the reference and ground should be constant. Output current I satisfies

\[ I = \frac{V_{\text{ref}}}{R_2} \]  (1)
The actual design process is triode type 2N2222, the value of R2 is changed in the test, and the final output current is 90mA.

![Figure 5. Circuit Diagram of Constant Current Source](image)

3.2. Signal conditioning module design

The signal conditioning module is mainly the design of the voltage effective value conversion module and the differential amplifier module.

3.2.1. Design of detector

Because the software has poor accuracy in obtaining the amplitude of AC signal, the true valid value detection method is used to obtain the amplitude value. AD637 can measure the true valid value of the AC signal and provide DC output, which is equal to the root mean square value of the input signal. When the valid value of AD637 input signal is 2V, the bandwidth is 8MHz, which meets the design requirements. Converts sinusoidal signal to DC signal, the data is stable and accurate. The module schematic diagram is shown in Figure 6.

![Figure 6. Circuit Diagram of AD637](image)

3.2.2. Design of amplifier module

Some signals in the circuit are weak or not in the range of ADC collection. Signal conditioning circuit is needed to adjust the signal in order to facilitate ADC collection and obtain correct data. When the load is in short-circuit state, the output of constant current source is used to measure short-circuit resistance. Because the resistance of the copper wire is very small and the voltage between points A and B is very low. Although it is a DC signal, the signal voltage value is very low and cannot be collected directly through ADC, so the signal needs to be amplified and collected again. The device uses INA128 precision instrument amplifier to amplify weak signal.

The chip is designed with a multifunctional three-stage operational amplifier. The current feedback input circuit enables the chip to have a large bandwidth at high gain. The module circuit diagram is shown in Figure 7.
The common mode rejection ratio of INA128 is large. The input impedance is high. The common mode rejection ratio can reach 130dB, and the gain range is 1-10000. Differential input increases the ability to suppress common-mode interference while making the input impedance extremely high\textsuperscript{[14-15]}. The gain (G) of INA128 satisfies:

\[ G = 1 + \frac{50K\Omega}{R_g} \]  

(2)

3.3. Design of ADC

The device uses ADS1256 module and ADC inside the microcontroller as the analog-to-digital conversion module, because the values to be collected are as accurate as possible. The functions of ADS1256 are the precision of 24 bits, the noise-free resolution of 23 bits, the data rate of 30 ksps per second and the low noise. It is suitable for high-resolution measurement schemes\textsuperscript{[16-17]}. ADS1256 module circuit diagram (Figure 8) uses 7.68MHz passive crystal vibration, and its output level can be adjusted and more flexible.

4. Design of system software

The program part design flowchart is shown in Figure 9. After the program starts, the system clock, interrupt, serial port, ADS1256, AD9959, LCD screen are initialized, the initial interface is displayed on the LCD screen, and the output frequency of AD9959 is controlled at 1 kHz with a peak value of 500 mV. Then enter the main cycle, make load open circuit judgment, load short circuit judgment, load network detection, and display the results on the LCD screen after executing the corresponding detection code.
4.1. Module driver design
The module driver design is mainly the driver design of AD9959 signal source and ADS1256 module. Mainly for the communication between the controller and the module chip, configure the internal register of the chip to complete the corresponding functions, so that the signal source module can output the sinusoidal signal with corresponding frequency and amplitude, and the analog-to-digital conversion module can collect the correct signal value.

4.1.1. Design of Signal generator control program
AD9959 part of the program mainly sets the initialization of the module and configures different frequency, phase and amplitude information. The code control flow chart is shown in Figure 10.

4.1.2. Design of ADC data acquisition program
The program of ADS1256 mainly initializes the module and configures the data collection function. The parameters, gain and data output rate of ADS1256 are mainly configured. In the interrupt service program, eight channels of data are obtained, stored in the register, and the microcontroller reads the ADC sampling results from the buffer. The ADS1256 control flow is shown in Figure 11.
4.2. Design of fault and fault location detection algorithms

After the program runs, the AD9959 output frequency 1 kHz sine signal is controlled by default, and the subsequent circuit is driven by the amplifier. When the load is open, the voltage value measured at point A is larger than that measured at point B. When the load is short-circuited, the voltage values at points A and B are larger and approximately equal. After detecting the short circuit of the load, switch to the output of the constant current source, get the voltage at both ends of the load through analog-to-digital conversion, and get the position of the circuit point based on the resistivity of the conductor. The flowchart of the subroutine is shown in Figure 12.

Figure 11. ADS1256 Control Flow Diagram

Figure 12. Flowchart of Fault and Fault Location Detection Algorithms

The device uses the inner core of six types of 0.58M m network wires as its conductor, with a resistivity of 0.07/m and a constant current source output current of 90mA. A total of three crocodile clip wires are used as the connection lines between the device and points A and B, as well as short-circuit lines. The total resistance R=0.01 of the three alligator clip wires can be obtained by measuring. If the distance between the short-circuit point and point A is x.
\[ x = \left[ \frac{(U_A - U_B)}{U_B} \cdot R_1 \right]^{1/\beta} \]  

(3)

4.3. Design of load network architecture algorithm

The controller controls the sinusoidal signals with AD9959 output frequencies of 1 kHz and 1 MHz, records the data collected by the analog-to-digital conversion module, and calculates the impedance modulus \( Z_1 \) and \( Z_2 \).

The signal source outputs 1 kHz sine signal and the measured impedance value \( Z_1 \). When \( Z_1 \) is less than 10 \( \Omega \), the load network structure may be single L, RL parallel, LC parallel or RLC parallel; The remaining load network structures are larger than 10 \( \Omega \). The signal source outputs 1 MHz sine signal and the measured impedance value \( Z_2 \). When \( Z_2 \) is less than 10 \( \Omega \), the load network structure may be single-C, RC parallel, LC parallel or RLC parallel. The remaining load network structures are larger than 10\( \Omega \).

Considering that \( Z_1 \) is less than 10 as condition 1 and \( Z_2 \) is less than 10 as condition 2, the load network structure can be divided into four broad categories according to the results of two frequencies:

(1) Both condition 1 and condition 2 are satisfied, and the load network structure may be LC parallel or RLC parallel. The signal source outputs the frequency sweep signal, finds the resonance point of the load, and obtains the phase of the resonance point. If the phase value is 0, then the load network structure is RLC parallel, otherwise it is LC parallel.

(2) If condition 1 does not meet condition 2, the load network structure may be single-L or RL parallel. The signal source outputs 10 MHz sine signal. If the inductive reactance range of the measured inductance is between 6283 \( \Omega \) and 62830 \( \Omega \) and the measured impedance value is less than 200 \( \Omega \), then the load network structure is RL parallel, otherwise it is single L structure.

(3) If condition 1 does not meet condition 2, the load network structure may be single-C or RC parallel. The signal source outputs 100 Hz sine signal. If the inductance range of the measured capacitance is between 795.8 \( \Omega \) and 7958 \( \Omega \) and the measured impedance value is less than 200 \( \Omega \), then the load network structure is RC parallel, otherwise it is single-C structure.

(4) Neither condition 1 nor condition 2 is satisfied. Load network structure may be single R structure, RC series, RL series, LC series or RLC series. In both cases, when the measured impedance values do not change much, the load is a single R structure. The signal source outputs a 10MHz sinusoidal signal. If the measured impedance is less than 200\( \Omega \), then the load network structure is LC series. The signal source output sweep signal and record the impedance amplitude and phase of the load. The RL series without resonance and the impedance increases with frequency. The RC series without resonance and the impedance decreases with frequency. LC series with resonance point impedance close to 0 and RLC series with resonance point impedance greater than 200 \( \Omega \).

4.4. Program Design for Component Parameter Detection

Based on the obtained load network structure, display load element values are calculated when the load consists of only a single component. Set the reference resistance to \( R_1 \), \( U_A \) and \( U_B \) for A and B respectively. When the load is resistance, the resistance \( R \) to be measured

\[ R = \frac{U_A - U_B}{U_B} \cdot R_1 \]  

(4)

When the load is a capacitor, the capacitance \( C \) to be measured is calculated from the output signal at 1 kHz

\[ C = \frac{U_B}{R_1 \cdot (U_A - U_B) \cdot 2\pi f} \]  

(5)

When the load is an inductance, the capacitance \( L \) to be measured is calculated from the output signal at 1MHz

\[ L = \frac{(U_A - U_B)}{U_B} \cdot R_1 \cdot 2\pi f \]  

(6)
5. Test
The RLC series-parallel circuit parameter and fault location detection device is shown in Figure 13. The left side is the main body of the device and the right side is the load to be measured.

Figure 13. Circuit parameters and physical diagram of fault detection device

5.1. Measurement results of component parameters
When the circuit is connected, the download program starts testing, and the test results are as follows.

| Standard value /Ω | Measured value /Ω | relative error /% |
|-------------------|-------------------|-------------------|
| 430               | 378.86            | 11.89             |
| 1000              | 895.50            | 10.45             |
| 1500              | 1258.27           | 16.11             |

The measurement results from Table 1 require modification of the calculation method to fit the parameter values of the components due to some influence of the measurement environment. Select the ratio of the voltage at both ends of the load as the independent variable component value of the fitting data to fit the dependent variable.

The results of the resistance fitting are shown in the Figure 14. All data points are basically on a straight line. To ensure the accuracy of the final result, a second-order polynomial is used to predict the trend line, and the final expression is obtained:

\[ y = 3.7177x^2 + 113.09x - 3.0496 \]  \hspace{1cm} (7)

Figure 14. Diagram of the relationship between resistance values and fitting parameters

By returning the fitted expression to the program and modifying the calculation method, the calibrated resistance calculation results can be obtained, as shown in Table 2.
Table 2. Measurement results of resistance parameters after calibration

| Standard value /Ω | Measured value /Ω | relative error /% |
|-------------------|-------------------|-------------------|
| 220               | 218.59            | 0.68              |
| 240               | 238.65            | 0.56              |
| 750               | 740.68            | 0.44              |
| 1000              | 1003.57           | 0.36              |
| 1600              | 1588.66           | 0.71              |
| 2000              | 1995.24           | 0.23              |

From the measurement results in Table 2, it can be concluded that since the resistance is a linear element, the voltage at both ends of the resistor varies linearly in the linear circuit, so the relative error of the calculated results after fitting is very small and meets the design requirements.

The capacitance is fitted in the same way to get the data fit figure which are shown in Figure 15.

![Fitting Parameters](image)

Figure 15. Fitting diagram of capacitance data

The capacitance is also predicted by a second-order polynomial and the resulting expression is:

\[ y = -0.0013x^2 + 0.1116x - 0.1749 \]  

(8)

Return the expression to the program to modify the code and get the measurement results as shown in Table 3.

Table 3. Measurement results of capacitance parameters

| Standard value /nF | Measured value /nF | relative error /% |
|--------------------|--------------------|-------------------|
| 200                | 191.99             | 4.01              |
| 470                | 478.36             | 1.84              |
| 1000               | 963.52             | 3.65              |
| 2200               | 2103.97            | 4.37              |

From the measurement results in Table 3, it can be concluded that the error of capacitance measurement still exists. The mainly reasons are the use of less basic capacitance, less test data and uneven data arrangement. Capacitance is a non-linear device. The result of fitting is not good, but within the range of design requirements.

The inductance values are fitted and the fitted curve is shown in Figure 16.
Fitting Parameters

Figure 16. Fitting diagram of inductance data

The second-order polynomial is used to predict the trend line of inductance, and the final expression is:

\[ y = 657.94x^2 + 493.78x + 151 \]  \hspace{1cm} (9)

Return the expression to the program to modify the code and get the measurement results as shown in Table 4.

Table 4. Measurement results of inductance parameters

| Standard value /uH | Measured value /uH | relative error /% |
|--------------------|--------------------|------------------|
| 100                | 101.12             | 1.12             |
| 220                | 217.92             | 0.95             |
| 500                | 480.29             | 3.94             |
| 1000               | 957.27             | 4.27             |

From the measurement results in Table 4, it can be concluded that the error of capacitance measurement still exists. Error sources are similar to inductances: fewer test data, non-linear components, resulting in deviations in fitting and data points, but generally within range of the design requirements.

5.2. Load network structure detection

Using 1K resistance, 1uF capacitance and 1mH inductance as components of the load, the network structure is changed and then measure. The detected load network structure corresponds to the actual load network structure, and the result is correct. The device can complete the task of load network detection.

5.3. Load fault detection and short circuit location measurement

When the load is in open or short circuit state, the corresponding state can be detected. The measurement results are shown in Table 5.

Table 5. Short-circuit position measurement results

| Actual Distance /cm | Measure Distance /cm | relative error /cm |
|---------------------|----------------------|--------------------|
| 20.0                | 19.8                 | 0.2                |
| 25.0                | 24.2                 | 0.8                |
| 30.0                | 29.4                 | 0.6                |
| 35.0                | 34.6                 | 0.4                |
| 40.0                | 39.8                 | 0.2                |
| 45.0                | 44.9                 | 0.1                |
| 50.0                | 50.2                 | 0.2                |

According to the measurement results in Table 5, the output of constant current source is used for short-circuit point measurement, and to some extent the DC signal is easy to collect data. The
measurement of short-circuit point location is basically correct and meets the error requirements of design.

6. Conclusion
The high performance of STM32 is very convenient in collecting low-speed data and processing. It can easily amplify the signal acquisition of the circuit. By designing the signal processing module and analyzing the circuit principle, STM32 controls the direct digital frequency synthesis (DDS) module and the constant current source module as the excitation source. The voltage value at the load end is obtained through the RMS measurement module, the phase is obtained through Fourier transform, and then the load phase angle can be easily obtained. When the load works normally, the current will be calculated by the known reference resistance, then the impedance value of the load will also be calculated, and the phase value will be obtained. Finally, the network structure of the load will be conducted comprehensive analysis. An alarm will be given when the load is open or short circuited. The source AD9959 will be switched to the constant current source output when the load is short circuited. The voltage difference at both ends of the load will be amplified through the differential amplification module for measurement. After that the resistance of the short circuit will be calculated. Afterwards the position of the short circuit point will be measured according to the resistivity of the conductor. Finally, the results are comprehensively displayed on the LCD screen. The structure test shows that it can complete the above functions.

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