Timing constraints imposed by classical digital control systems on photonic implementations of measurement-based quantum computing

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Most of the architectural research on photonic implementations of measurement-based quantum computing (MBQC) has focused on the quantum resources involved in the problem with the implicit assumption that these will provide the main constraints on system scaling. However, the ‘flying-qubit’ architecture of photonic MBQC requires specific timing constraints that need to be met by the classical control system. This classical control includes, for example: the amplification of the signals from single-photon detectors to voltage levels compatible with digital systems; the implementation of a control system which converts measurement outcomes into basis settings for measuring subsequent cluster qubits, in accordance with the quantum algorithm being implemented; and the digital-to-analog converter (DAC) and amplifier systems required to set these measurement bases using a fast phase modulator. In this paper, we analyze the digital system needed to implement arbitrary one-qubit rotations and controlled-NOT (CNOT) gates in discrete-variable photonic MBQC, in the presence of an ideal cluster state generator, with the main aim of understanding the timing constraints imposed by the digital logic on the analog system and quantum hardware. We use static timing analysis of a Xilinx FPGA (7 series) to provide a practical upper bound on the speed at which the adaptive measurement processing can be performed, in turn constraining the photonic clock rate of the system. Our work points to the importance of co-designing the classical control system in tandem with the quantum system in order to meet the challenging specifications of a photonic quantum computer.

I. INTRODUCTION

Quantum computers are enjoying a period of intense research activity. This is due to the possibility of very large speed-ups in finding effective solutions for certain classes of problems which are hard or impossible to solve using classical computers. These include, in the near-term, the simulation of other quantum mechanical systems with applications in quantum chemistry [1], and in the longer term certain kinds of search-related problems [2].

Currently, only relatively small quantum computers have been built, containing less than one hundred qubits, in a multitude of competing technologies [3]. However, it is hoped that with increasing understanding over how to engineer and control quantum systems at scale, there will be a substantial increase in the computational power of quantum computers in the near future.

However, a few hurdles lie in the way of this scaling process. Often discussed are the characteristics of the qubits themselves: for example, the difficulty of achieving high enough fidelity gate operations on physical qubits [4], or how to fabricate devices at scale [5]. One aspect of the problem, which is discussed less often, is the classical electronic control requirements that need to be met for these machines.

At first glance, this is surprising since the common link between all the platforms for quantum computing is the need for traditional electronics to control them. However, there is a general tendency to view classical signal processing as a ‘solved problem’, at least in comparison to the difficulty of the quantum information processing, and assume that any requisite performance can be achieved using custom application-specific integrated circuits (ASICs). This is understandable, given the high-degree of performance and sophistication that modern (digital) CMOS electronics can routinely achieve. However, adapting and applying classical electronics to quantum control problems is not straightforward and is an active area of research across all quantum computing platforms. For example, in superconducting qubit based quantum computers, it is an open question how best to integrate the microwave control electronics close to the qubits in order to reduce the number of interfacing wires that prevent scalability in that architecture. Novel optical routes for microwave delivery are being investigated as a potential solution to this problem [6].

In addition, the flip-side to modern CMOS electronics having reached the great level of sophistication that it enjoys today is that there is not a great deal of room left for improvement in performance. For example, clock speeds in computers are plateauing [7], and transistor sizes are reaching their limits [8]. Quantum devices, on the other hand, being a relatively young technology, are expected to see a Moore’s law-like improvement in the future [9]. Consequently, it is critical to understand the limitations that classical electronics and control will impose on current quantum computing platforms.

The majority of the prior work discussing photonic MBQC has focused on the quantum resources required and the theoretical architecture of the system [9][13]. To our knowledge, the question of how far these schemes
can be successfully implemented using current electronic devices remains unaddressed. As a first step towards this problem, we analyse the timing constraints imposed by classical electronics on the operation of a photonic quantum computer based on an ideal cluster state generator. We focus on photonic MBQC because of its relative insensitivity to photon loss in contrast to the gate based models. In addition, it is the primary architecture of choice for most active large-scale implementations of photonic quantum computers [12, 13].

There are several important constraints the electronic control system may impose on the implementation of photonic MBQC. Firstly, the speed at which the electronics can be made to operate determines the maximum photon clock cycle of the system. In particular, the ‘flying-qubit’ architecture of photonic MBQC (discussed in Section III below) requires adaptive measurement settings to be worked out before the arrival of the next column of photons in the cluster state. Secondly, the complexity of the system – particularly the analog parts – determines how much on-chip area is taken up with classical processing. This is particularly important because the “unit cell” of the electronic system must be duplicated once per logical qubit in photonic MBQC, and signal routing becomes challenging as the system starts to scale. Thirdly, the noise that is introduced by the analog stages of the control system will potentially introduce logical errors that need to be accounted for.

In this work, we focus on the first of these questions: specifically, what timing constraints does the digital part of the system impose upon the analog and wider photonic systems, and how does that affect the overall photonic clock rate of the quantum computer? We perform the analysis for an idealized system with an ideal cluster state generator and consider the signal delay in the digital domain (after photon detection and logic-level amplification) to the input of the analog system which is needed to set the bases for the next measurement round; details in Figure 1 below).

The structure of this paper is as follows. In Section II, we provide a practical description of the parts of MBQC needed to understand the results of this paper. In Section III, we describe a simple model of photonic MBQC – based on an ideal cluster state source – showing the analog and digital systems which are necessary for a basic implementation of the system. In Section IV, we present an example design for the digital component of the classical processing, targeting a Xilinx 7-series FPGA. In Section V, we describe the functional verification of the design. In Section VI, we use static timing analysis of the implemented design to derive constraints on the analog parts of the system, and on the overall photonic clock frequency of the quantum computer. Section VII contains changes to the underlying model to make it more realistic, which would increase the complexity of the digital system. Finally, we discuss the wider implications of our results in Sections VIII and IX.

II. INTRODUCTION TO MEASUREMENT-BASED QUANTUM COMPUTING

Quantum computing in the gate-based model (see Appendix A for details) consists of the following steps:

1. An initial quantum state \( |\phi\rangle \) is prepared on \( N \) qubits;
2. Quantum gates are applied to the qubits;
3. The resulting state \( |\psi\rangle \) is measured, which constitutes the output from the quantum circuit.

MBQC is a different way to obtain the same resulting output state \( |\psi\rangle \), by performing single-qubit measurements on a more complicated initial state called a cluster state. It consists of the following steps:

1. Prepare a special quantum state, called a cluster state, on a larger number \( M > N \) of qubits. The main feature of the cluster state is that adjacent qubits are entangled together, which is represented using line segments in Figure 1;
2. Measure qubits from the cluster state one at a time, according to rules that correspond to the quantum circuit, until all but \( N \) have been measured;
3. Finally, the resulting state \( |\psi'\rangle \) on the \( N \) remaining qubits is measured in the computational basis, which constitutes the output from the circuit.

The initial state \( |\phi\rangle \) in the gate-based model is a matter of convention; if each qubit is initially prepared in the \( |+\rangle \) state, then the output states \( |\psi\rangle \) and \( |\psi'\rangle \) from the gate-based model and MBQC are the same, meaning that any algorithm expressed in the gate-based model can be equally well performed using MBQC.

For a comprehensive overview of MBQC, see [14]. A short pedagogical introduction is contained in [15]. What follows is a brief description of the main features of MBQC which are relevant to this paper.

1. Logical qubits and gates in MBQC

Each horizontal line of entanglement in the cluster state corresponds to a single qubit in the gate-based model, which we will call a logical qubit, to distinguish it from the cluster qubits that make up the cluster state. One-qubit gates in the gate-based model involve measurements of the cluster qubits along a logical qubit row according to rules that determine the basis settings of each measurement, and define what to do with the measurement outcomes. Two-qubit gates require vertical lines of entanglement which join the logical qubit rows together, as shown in Fig. 1b between the second and third row.
Entanglement between cluster qubits
No entanglement
Order of column measurements

FIG. 1. a) A cluster state is made from a rectangular array of qubits (the white dots), each of which may be entangled with its four nearest neighbours. When a computation is performed, a specific pattern of entanglement is required that matches the shape of the circuit. b) The quantum computation is performed by measuring the cluster qubits in bases derived from the measurement pattern. The shaded blue regions show which cluster qubits are involved in implementing which gates. The identity gate is included to pad the length of the one-qubit gate $U_1 = R_x(\xi)R_z(\eta)R_x(\xi)$ so it matches the CNOT. c) The quantum circuit that is performed by the measurement pattern in b).

2. Measurement patterns for gates

Each gate $G$ that is implemented in MBQC is defined by a measurement pattern, which is a set of rules describing:

- How many cluster qubits are needed to realise the gate $G$ and what pattern of entanglement is necessary between those cluster qubits;
- Which basis to use for each cluster qubit measurement;
- How to process the outcomes from the cluster qubit measurements.

A given computation involving multiple gates, such as the one shown in the gate-based model in Figure 1c, can be performed using MBQC by concatenating the measurement patterns for each gate (the blue shaded regions in Figure 1b). The resulting pattern contains one row for each qubit in the gate-based model (here, $N = 3$), and a number of columns defined by the length of the concatenated measurement patterns (the total number of cluster qubits is $M = 21$).

In making the measurements defined by the measurement patterns, each cluster qubit is removed one by one until only the rightmost column remains unmeasured. The final column of the cluster state is measured in the computational basis as shown in Figure 1b, which represents the output from the quantum circuit.

The arbitrary one-qubit gate $U$ in Figure 1c is realised using a measurement pattern of four cluster qubits in the top row of Figure 1b, and the CNOT gate is realised using a measurement pattern of 12 cluster qubits spanning the bottom two rows of Figure 1b (note the vertical entanglement link).

All measurements shown in green and purple boxes in the figure are performed along lines that lie in the equator of the Bloch sphere (Figure 2). Green boxes containing $X$ or $Y$ are measurements along the $x$- or $y$-axis, respectively. Purple boxes are measured along a line with an angle $\phi$ derived from the value in the box and measurement outcomes of other cluster qubits. The grey boxes represent computational basis measurements, which are made along the $z$-axis of the Bloch sphere.

3. Performing the cluster qubit measurements

As described in Appendix A, the only physical measurements that can be performed are computational basis measurements. All the other measurements (in the equator of the Bloch sphere) are performed by applying a one-qubit gate to the given cluster qubit and then measuring it in the computational basis.

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1 In [14], measurement patterns are taken to include the “output” qubits, which is the first column of qubits directly to the right of the measurement pattern. In this scheme, measurement patterns must overlap (because the output qubit column is also the input qubit column for the next gate pattern). In this paper, we associate the output qubit with the next measurement pattern, so that patterns can be simply concatenated.

2 The symbol for a CNOT gate shown in Figure 1 is the same as a classical XOR applied to the target qubit. This is because the CNOT gate can be thought of as adding the value of the control qubit to the target qubit modulo 2. We make extensive use of the classical XOR operation in subsequent figures in this paper. For clarity, we state here that all instances of the XOR symbol in this paper – apart from in Figure 1 – are classical XOR gates, not CNOT gates.
In MBQC, measurements in the purple and green boxes in Figure 1 point on the Bloch Sphere. A measurement of a single qubit in the equator of the Bloch sphere, as shown in Figure 2. It is therefore specified by a real angle $\theta$ and a sign bit $s$, such that $\phi = (-1)^s \theta$. The value of $\theta$ is shown in the purple boxes in Figure 1b. Note that $\theta$ may be negative.

For the green boxes in Figure 1, the value of $\theta$ is 0 for $X$ and $\pi/2$ for $Y$. In the first case, the value of $s$ does not affect the basis angle $\phi$ at all. In the second case, the roles of $|0\rangle'$ and $|1\rangle'$ are swapped because $L$ is reversed; however, since the outcome of the measurement is random, the swapped measurement outcomes can be corrected in the calculation of byproduct operators (see Section IV). Therefore, the $X$ and $Y$ measurements are not affected by the value of $s$.

The value of $\theta$ is a characteristic of the quantum circuit being implemented. The value $s$, however, depends on the outcomes of other (prior) measurements in the measurement pattern. The measurement bases in MBQC are therefore adaptive, because the basis in which a cluster qubit is measured may depend on the outcomes of measurements of other cluster qubits which have been measured before. We will refer to $s$ henceforth as the adaptive measurement setting.

Any measurement pattern, such as the CNOT gate, which contains only $X$ and $Y$ measurements, does not involve adaptive basis settings, because the value of $s$ has no effect. It can be shown that the set of gates implementable with these non-adaptive patterns is the Clifford gate set [14], which is not universal [16]. For universal quantum computing, it is necessary to include a gate such as the one-qubit gate which does require adaptive measurement settings.

In Figure 3b, the measurement pattern for the arbitrary one-qubit gate (corresponding to a rotation of the Bloch sphere) is shown in detail [14]. The shaded purple region (particularly the blue wires) shows how the adaptive measurement setting for each measurement is computed from previous measurement outcomes. The dependence between $s$ and measurement outcomes implies that the measurements must be made from left to right, which is also indicated by the arrow of time at the bottom of the figure.

The measurement pattern for the CNOT gate is shown in Figure 3. This is not the same pattern as that presented in the original MBQC paper [14], which uses three logical qubit rows. The derivation of the CNOT pattern in Figure 3 is contained in Appendix B. We use this modified CNOT measurement pattern because it considerably simplifies our example digital implementation in Section IV, which only supports nearest-neighbour connectivity of logical qubits.

4. Measurement basis angles and adaptive measurements

Every measurement that is part of a measurement pattern is measured along a line $L$ in the equator of the Bloch sphere, as shown in Figure 2. It is therefore specified by one real angle $\phi$. In MBQC measurement patterns, this angle is made up of a value $\theta$, and a sign bit $s$, such that $\phi = (-1)^s \theta$. The value of $\theta$ is shown in the purple boxes in Figure 1b. Note that $\theta$ may be negative.

5. Byproduct calculations

As the measurement pattern proceeds, the random outcomes of the measurements introduce correctable errors in the computation. These errors are known as byproduct operators, because they are unintended logical operations which occur as a byproduct of the MBQC measurements.

Specifically, after any $N$-qubit gate $G$ has been applied to a state $|\psi\rangle$ using its measurement pattern, the result-
b) Arbitrary one-qubit gate

The byproduct operator for the logical qubit $i$ is specified by two bits $x_i$ and $z_i$, which are updated as the computation proceeds. By an abuse of notation, we will refer to the pair $(x_i, z_i)$ as the byproduct operator as well. For $N$ logical qubits ($N$ rows of the cluster state), $2N$ bits are needed to store the byproduct operators. At the start of the computation, they are all initialised to zero, because no gate has been performed so no errors have been introduced. As the computation proceeds, the outcomes of the measurements in the pattern are XORed into the $x_i$ and $z_i$ according to prescribed rules, described below and shown in Figure 3.

For the one-qubit gate in Figure 3, the new byproduct operators $(x'_k, z'_k)$ and $(x'_4, z'_4)$ are calculated using
\begin{align}
    z'_c &= z_c \oplus m_0 \oplus m_2 \\
    x'_c &= x_c \oplus m_1 \oplus m_2 \oplus m_4 \oplus m_5,
\end{align}
\begin{align}
    z'_m &= z_m \oplus m_6 \oplus m_8 + 1 \\
    x'_m &= x_m \oplus m_1 \oplus m_2 \oplus m_7 + m_9 + m_{11}.
\end{align}

Unlike for the one-qubit gate, the byproduct operators for a given logical qubit row are calculated using measurements from other rows. Note the addition of the constant 1 in the control qubit byproduct operator.

On the face of it, byproduct operators appear to introduce errors into the computation, because the gate $BG$ is performed instead of the desired gate $G$. However, the effect of this error can be corrected after the final column of $Z$-measurements in the MBQC process has been performed: the outcome from any logical qubit row $i$ where $x_i = 1$ has its outcome flipped from a zero to a one or vice versa [13]. This action undoes the effect of the byproduct operators, leaving a circuit that effectively only implements the gate $G$ as desired. The $z_i$ components are not used because they correspond to a phase shift which does not affect the probability of measuring a zero or one in a computational basis measurement. However, as we describe in the next section, it is necessary to keep track of their values because they can affect the value of the $x_i$, through the process of commutation corrections.
6. Commutation corrections

The byproduct operators are used to correct the outcomes obtained after the MBQC circuit is finished. However, the correction only works if the byproduct operators are the last operation before the final column computational basis measurement, which is only the case if a single gate $G$ is performed.

If multiple gates $G_k$ are performed on a state $|\psi\rangle$, then the resulting state $|\phi\rangle$ will be

$$|\phi\rangle = (B_KG_K) \ldots (B_1G_1)(B_0G_0)|\psi\rangle. \quad (3)$$

These interleaved byproduct operators cannot be corrected at the end of the circuit. Instead, it is necessary to move all the byproduct operators to the left side of the equation. To do that, after each new gate $G_{k+1}$ is applied, it is necessary to commute the current byproduct operators $B_k$ and the gate $G_{k+1}$, so that the byproduct operators are always on the leftmost side of the equation. This is illustrated below for the application of the second gate $G_1$:

$$B_0G_0|\psi\rangle \mapsto B_1G_1B_0G_0|\psi\rangle \mapsto B_1B'_0G'_1G_0|\psi\rangle \mapsto B_1G'_1G_0. \quad (4)$$

where $G_1B_0 = B'_0G'_1$, and the prime indicates the change that may occur in either gate. The byproduct operators $B_1$ and $B'_0$ can be combined into a resulting byproduct operator $B_r$ by adding together the values of $(x_i, z_i)$ bitwise modulo 2 for each operator. The state on the right of Equation (4) is therefore transformed to the same form of the state on the left, so that on the application of the next gate $G_2$, the process can be repeated and the byproduct operators are always kept on the left. We will call the process of commuting $B$ through $G$ a commutation correction.

In practical terms, the commutation correction is an operation that is performed before a gate is applied, by manipulating the current value of the byproduct operators and the upcoming gate so as to have the effect of Equation (4). For the two measurement patterns we consider in Figure 3, the commutation corrections are quite simple. In the case of the CNOT gate $G = \text{CNOT}$, $G' = G$, and only the byproduct operator $B$ changes to $B'$, according to the rule

$$
\begin{align*}
    z'_c &= z_c \oplus z_t \\
    x'_c &= x_c \\
    z'_t &= z_t \\
    x'_t &= x_t \oplus x_c.
\end{align*} \quad (5)
$$

For the one-qubit gate $G = U$, the byproduct operators remain the same, $B' = B$, but the gate itself $G$ must be modified. The modification is made by using the values of the byproduct operators to affect the adaptive measurement settings, by XORing the byproduct operators with previous measurement outcomes to form the values of $s$ for each cluster qubit, as shown in Figure 3. The calculation of the adaptive measurement settings $s_j$ for each cluster qubit $j$ is shown in the following equations

$$
\begin{align*}
    s_0 &= 0 \\
    s_1 &= m_0 \oplus z \\
    s_2 &= m_1 \oplus x \\
    s_3 &= m_0 \oplus m_2 \oplus z.
\end{align*} \quad (6)
$$

It is necessary to make a copy of the byproduct operators $(x, z)$ before measuring the cluster qubits, because otherwise they will be overwritten during the calculations described in the previous paragraph. For example, after the measurement of cluster qubit 1 in the arbitrary one-qubit gate in Figure 3, both the $x$ and $z$ values have been updated by measurement outcomes from cluster qubits 0 and 1. However, the old values of $x$ and $z$ are necessary in the measurement settings for cluster qubits 2 and 3.

In addition to the timing constraints imposed by the calculation of the adaptive measurement settings, the need to track the byproduct operators and calculate commutation corrections leads to additional timing constraints on digital implementations of the system, because they must be tracked in real time, and may affect adaptive measurement settings.

7. Cutting out the right measurement pattern from the cluster state

In the measurement pattern for the CNOT gate in Figure 3, there are missing links between some of the cluster qubits. However, a fully connected cluster state does not contain missing links. In order for the CNOT measurement pattern to work, it is necessary to use an ideal cluster state generator, meaning one which can produce arbitrary patterns of nearest-neighbour entanglement in the cluster state.

In the more general approach to MBQC, the computation always begins from the full cluster state. The links around a cluster qubit can then be removed by performing a computational basis measurement on that qubit. Using this method, cluster states containing less entanglement can be obtained from fully connected cluster states.

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1 Some authors distinguish a fully connected cluster state from a partial cluster state, which is an example of the more general ‘graph state’, because it has vertices corresponding to cluster qubits and edges corresponding to entanglement links. In this terminology, a fully connected cluster state is a graph state whose graph is the fully connected 2D lattice. To simplify our discussion, we refer to all graph states of any entanglement pattern as cluster states.

4 This is one reason for using the three-row CNOT pattern, as in [13]: it is necessary to preserve a buffer row of cluster qubits be-
The computational basis measurement that cuts out a cluster qubit incurs an additional step in the calculation of basis angles for surrounding cluster qubits. If the outcome of this measurement is a one, then a rotation \( R_z(\pi) \) must be applied to the surrounding qubits, before they are measured according to any measurement pattern \([14]\). This gives rise to a more general form for the basis angle

\[
\phi = \pi c + (-1)^s \theta,
\]

where \( c \) is a single bit that is formed by XOR-ing the measurement outcomes from any cluster adjacent qubits which have been removed using computational basis measurements.

Since the cut-out correction caused by removing a given cluster qubit must be performed before making the measurement of that qubit, the cutting out of cluster qubits introduces a measurement dependency between the measurement outcome of the cut-out qubit and the measurement angle \( \phi \) of the qubits above and below it in the same column. This is different from our previous discussion on adaptive settings where the measurement outcomes had dependencies across columns in the cluster state and there was no intra-column dependence. This can only be handled by measuring each column in two rounds. First, the qubits that must be cut out are measured; then, the surrounding cluster qubits are measured using the modified basis angle \( \phi \) in Equation (7).

This aspect of cutting out the right shaped pattern from a fully connected cluster state can be avoided entirely if the right shaped cluster state is available from the beginning, using an ideal cluster state generator that can generate arbitrary patterns of entanglement. We assume the existence of such a cluster state generator for the purposes of this paper, and do not consider cut-out corrections any further.

III. SIMPLIFIED MODEL OF PHOTONIC QUANTUM COMPUTING

In this section we describe how to implement MBQC using photons as qubits. We do not consider the generation of photonic cluster states, which is a separate subject in its own right \([9, 12]\). Instead, we assume an ideal photonic cluster state generator, which can generate arbitrarily shaped rectangular cluster states, and describe how one can use it to perform photonic MBQC. We begin by describing how photons can be used as qubits.

## A. Quantum computing using photons as qubits

In photonic quantum computing, a qubit is realised using a single photon. In the dual-rail encoding considered in this paper, a single photon passes through one waveguide or another depending on whether the qubit it represents is in the state \(|0\rangle\) or \(|1\rangle\), as shown in Figure 4. A qubit encoded like this can be realised in the computational basis by placing a single-photon detector at the end of the pair of waveguides. It is important to realise that this process destroys the qubit (by absorbing the photon), unlike a matter-based qubit which can be re-used after measurement.

Modulators and beamsplitters can be used to realise an arbitrary one-qubit gate, as follows. First, a modulator in the \(|0\rangle\) waveguide realises an arbitrary \( z \)-rotation, shown in Figure 4. Then, the variable beamsplitter shown in Figure 5 realises an arbitrary \( z \)-rotation. Finally, a second modulator in the \(|1\rangle\) waveguide realises another arbitrary \( z \)-rotation, which completes the decomposition \( R_z(\alpha)R_z(\beta)R_z(\gamma) \).

In contrast to many other physical realisations of quantum computing, including superconducting qubits and trapped ions, that have a natural way to implement two-
qubit operations [17], there is no simple deterministic way to implement the CNOT gate, or any other two qubit entangling gate, in terms of passive linear optical elements (modulators and beamsplitters). This is mainly due to the weakness of the direct photon-photon interaction. While this might appear to be a key limitation for photonic quantum computing, it was shown that one can implement an artificial non-linear gate that works probabilistically by using additional auxiliary photons and photodetection [18]. By parallel multiplexing these entangling gates, one can overcome their inherently probabilistic operation [11].

One of the arguments in favour of photonic MBQC is the absence of two-qubit gates in the implementation of a quantum circuit [9]; after the cluster state has been generated, only one-qubit gates and computational basis measurements are necessary. Much of the complexity is pushed to the task of generating the cluster state [10], which is responsible for all the entanglement between the qubits. As we describe in the next section, it is possible to generate the cluster state one column at a time, so that each photon only has to travel through a fixed length of cluster state generating system, followed by a fixed length measurement system so that the overall photon loss can be bounded irrespective of the length of the equivalent quantum circuit (in the gate-based model) being implemented. Given photon loss is a primary source of error (and decoherence) for photonic quantum computing, this represents another important advantage of photonic MBQC [10].

B. Photonic measurement-based quantum computing

For matter-based implementations of MBQC, the grid of qubits directly corresponds to a two-dimensional physical array of atoms. However, for photonic quantum computing, it is not feasible to maintain a static array of qubits for long enough to perform the measurements. This is because a photon is always moving, so the only way to store it is to place it in a long waveguide, called a delay line, or keep it circulating in an on-chip cavity, such as a microring resonator. Both of these approaches eventually lead to photon decay, primarily due to scattering and absorption loss in the waveguide which is exacerbated in an integrated photonics platform (waveguide loss in a silicon platform is ≈ 1 dB cm⁻¹ [19] compared to ≈ 0.2 dB km⁻¹ for optical fibres [20]).

Instead, the cluster state can be generated one column at a time, and each column can be measured one after the other. This is opposite to the original presentation of MBQC [13], where the goal was to separate the processes of generating the cluster state and making the measurements. The motivation for generating the cluster state all at once was also due to physical considerations: a matter-based cluster state can be generated using a tunable Ising interaction that acts globally on the system [15]. However, it can be shown that in the two approaches are equivalent [14] Section II.D]: there, the successive column approach is used as tool for verifying measurement patterns.

When the cluster state generation and the photon measurement is alternated, a single photon only has to travel from its source, through the cluster state generator, through a fixed length waveguide, and finish at the measurement block.

For photonic MBQC, in Figure 3, the horizontal axis can therefore be interpreted as time, and the vertical axis as space. Each column of the cluster state is generated one at a time, progressing from left to right. Using this approach introduces a restriction which is not present in the matter-based realisation of MBQC. The scheme is only viable if the measurement settings for the currently measured block only depend on the outcomes of previously measured columns. This is quite a severe restriction, ruling out many of the measurement patterns originally proposed in [13] (for example the CPhase gate, a two-qubit gate that depends on a continuous parameter). However, this requirement is satisfied for the one-qubit gate and the CNOT gate described here. In the case of the CNOT gate, there are no measurement dependencies. For the one-qubit gate, all the measurement dependencies (the blue lines in Figure 3b) point from left to right.

C. Timing constraints on the cluster state

We do not consider the generation of the photonic cluster state, apart from making the following remark about the choice of time delay between the generation of columns, which is crucial for our timing analysis.

In order to entangle photons $P_n$ and $P_{n+1}$ from two adjacent columns $n$ and $n+1$ of the cluster state, they must be brought to the same location (for example, a beam splitter) at the same time. However, when performing the cluster qubit measurement for the MBQC measurement pattern, $P_n$ (from column $n$) must arrive at the detector a finite time before $P_{n+1}$ (from column $n + 1$), to allow time for the processing of measurement settings, byproduct operators and commutation corrections. Therefore, $P_{n+1}$ must experience a delay $T_p$ (realised using an on-chip delay line or optical fibre) after the entangling operation of adjacent columns and the measurement block. The inverse of this delay $X_p = 1/T_p$ is the photonic clock frequency, which is the rate at which columns are produced and measured, and which determines the speed at which the quantum computation progresses.

Two distinct physical mechanisms provide upper and lower bounds for this delay. An upper bound is given by...
by the loss of the on-chip delay line, optical fibre, or routing system involved in the delay of the photon. The lower bound is given by the time required to process the measurement outcomes. The object of our analysis is to estimate the lower bound.

D. The full MBQC system

Figure 6 shows the full system required for processing one row of the MBQC measurement pattern, which corresponds to one logical qubit. It consists of the following six parts:

- The cluster state generator, which outputs the dual-rail encoded photon in each column of the cluster state one after the other. The photon has been entangled with the previous photon in the same row, and with the photons in the rows above and below as necessary for the measurement pattern.
- The delay line, described in the previous section, which is necessary to temporally separate the photons in adjacent columns after they have been entangled.
- The measurement block, which consists of passive linear optical elements that apply a configurable one-qubit operation, followed by a computational basis measurement.
- The photon detector amplifier which converts the output from a single-photon detector to a logic level suitable for processing by a digital system.
- The digital system which processes measurement outcomes into adaptive measurement settings and keeps track of byproduct operators.
- The analog output system, controlled by the digital system, which produces the analog voltage levels needed to drive the modulators in the measurement block.

The job of the digital system is to convert the measurement results into adaptive measurement settings for future measurements, and byproduct operators for interpreting the final measured outcomes.

The input to the digital system is the output pulse from the photon detector amplifier. This may be, for example, a superconducting-nanowire single-photon detector (SNSPD) [21] followed by a low-noise amplifier [22].

The output from the digital system includes the digital form of the angle \( \theta \), the adaptive measurement setting output \( s \), and a signal \( z \) which determines whether the measurement is in the \( XY \)-plane of the Bloch sphere, or if it is a computational basis measurement.

The analog output system is responsible for generating the voltages that control the modulators in the measurement block. It may be implemented using a combination of fast DACs and modulator drivers. Two modulators are necessary: one (\( M_1 \) in Figure 6) chooses between an \( XY \)-measurement and a computational basis measurement; and another (\( M_2 \)) controls the basis angle \( \phi \) for the \( XY \)-measurement. They are controlled by the voltages \( \alpha \) and \( \beta \) respectively, defined as follows:

\[
\alpha = \frac{\pi}{2}, \quad \beta = \frac{\pi}{2} - \phi = \frac{\pi}{2} - (-1)^s \theta. \quad (8)
\]

These modulator voltages realise the one-qubit rotation \( R_x(\alpha)R_z(\beta), \) which sets the basis for the measurement. The one-qubit rotations are summarised in Table I.

The voltage \( \alpha \) controls the \( R_x \) rotation portion of the measurement setting, which determines whether the measurement is a computational basis measurement \( (z = 0) \) or an \( XY \)-measurement \( (z = 1) \). The voltage \( \beta \) controls the angle of the \( XY \)-plane measurement \( \phi \), which is itself determined by the fixed value \( \theta \) and the adaptive measurement setting \( s \).

In this paper, we focus on the digital control system, and present a simple reference design capable of performing the one-qubit gate and CNOT gate described in Section IV. We analyse the timing behaviour of this design by implementing it with an FPGA and performing static timing analysis. The main objective of this analysis is to place timing constraints on the input and output analog systems, and therefore on the overall quantum photonic clock rate of the system. In the interest of simplicity, we ignore the final computational basis measurement of MBQC, which can easily be incorporated by setting \( z = 0 \) for the final column of the pattern.

IV. DIGITAL SYSTEM DESIGN

In the following sections we describe an example digital system design for processing measurement outcomes

6 Voltagess are expressed in modulator-phase units, where \( V = 1 \) is chosen such that the modulator applies a 1 rad phase shift.

7 The design, along with other data used in the paper, is contained in the following repository: https://gitlab.com/johnrscott(mbqc-fpga)
A. Clock planning

We present a design that can process measurements within a single clock cycle, by using three out-of-phase clocks. We consider a system synchronous design, with the photonic clock \( X_p \) the common (master) clock in the system.

On the rising edge of \( X_p \), the photon arrives in the measurement block, causing a pulse at the output of the single-photon detector. This measurement outcome is amplified and triggers a latch which provides a constant digital signal to the digital system.

The other two clocks, \( X_s \) and \( X_r \), are internal to the digital system. On the rising edge of the measurement sample clock \( X_s \), the measurement latch is sampled by the digital system. The rising edge of \( X_s \) must be sufficiently offset from the rising edge of \( X_p \) so that the output from the latch has settled to a steady state. This delay must include the time required to amplify the photon detector output.

On the rising edge of the reset clock \( X_r \), the latch is reset ready for the next measurement round. This event must occur after the rising edge of \( X_s \), but before the rising edge of the next photon clock cycle \( X_p \), to satisfy the hold time requirement of the sampling logic.

The computation of the adaptive measurement setting is performed using combinatorial logic at the earliest possible time that the latch output is valid, on the rising edge of \( X_s \). The measurement setting for the next measurement is then computed and becomes available a short amount of time after the rising edge of \( X_s \), corresponding to the combinational logic delay.

In addition, the byproduct operators are also computed on the rising edge of \( X_s \) using combinatorial logic. The commutation correction, which must be applied at the boundary of a quantum gate, is then computed on the rising edge of \( X_r \), because it requires the value of the byproduct operators computed on \( X_s \). The program which controls the measurement pattern is loaded from memory on \( X_p \) so that it is ready for the computations that take place on \( X_s \) and \( X_r \).

The design of each computational subsystem is described in detail below.

B. Adaptive measurement setting generation

The most important feature of the adaptive measurement setting \( s \) is that it must be present as soon as possible, ready for the next measurement round. The earliest possible time that \( s \) can be computed is on the rising edge of \( X_s \). From Figure 3, the value of \( s \) can depend on previous measurement settings and stored byproduct operator values from the current qubit.

A shift register is used to store the past three measurement values \( m_0, m_1, m_2 \), where \( m_0 \) is the most

\footnote{For more complicated measurement patterns it may be necessary to store more than three measurements. However, for the arbitrary one-qubit gate and CNOT gate, three measurements are sufficient.}
FIG. 7. a) The digital system diagram for multiple qubits. The “unit cell” for each qubit (shaded green) has a measurement latch, a program memory, and a control system for calculating measurement settings and byproduct operators. b) The design of the control system. In the high level schematic diagram of the control system, buses are denoted with bold lines, and the bus width is written next to the wire. The circles apply bitwise operations between their inputs: the cross stands for XOR and the dot stands for AND. The right port of the circle is the output, and all other ports are inputs. The logic gates are multi-input, with inputs from all the buses and wires connected on their left (i.e. wires inside a bus will be combined in the logic operation). Each part of the diagram is shaded according to its function, using the same colouring as in Figure 3. Flip-flops are clocked on the rising edge of their clock input, and elements whose output is LUT represent combinational logic. Reset signalling is omitted from the diagram for simplicity.

recent measurement outcome. The shift register is loaded sequentially with the next measurement on the rising
edge of $X_s$. The output $s$ is then obtained using a combinational circuit from the shift register, so it is present soon after the rising edge of $X_s$.

The outputs from the shift register are combined bitwise with a 3-bit mask $A_m$ and XORed together to produce the measurement contribution to $s$. The stored byproduct operators $(x_s, z_s)$ are masked using a two-bit value $A_b$ and XORed to produce a second contribution to $s$. These two contributions are XORed to produce $s$ itself. Putting together these two contributions gives the following expression for $s$:

$$s = \left( \bigoplus_{i=0}^{2} A_m[i]m_i \right) \oplus (A_b[1]x_s \oplus A_b[0]z_s),$$

where square brackets denote bitwise access.

The masks $A_m$ and $A_b$ for each measurement round are chosen in such a way that they combine past measurement outcomes and byproduct operators correctly to realise the one-qubit gate, as shown in Figure 3. The CNOT gate has no adaptive measurement settings, so $A_m = A_b = 0$ in that case.

The mask $A_m$ must remain valid through the rising edge of $X_p$, so it is registered on the rising edge of $X_s$. The byproduct operator contribution due to $A_b$ is also registered on $X_s$, so that the byproduct term persists through $X_p$. These registers are necessary because the program word, which contains the masks (see Section IV C below), is updated on the rising edge $X_p$.

A disadvantage of this design is that the output $s$ may contain function hazards [23], due to the propagation delays from each of the flip-flops to the output $s$. These hazards do not affect the digital function of the (synchronous) digital system; however, they may contribute to the power dissipation of the system and/or noise in the analog output, depending on how it is implemented. In order to avoid the hazards, the output $s$ could be registered; however, this would require another clock edge soon after $X_s$ to preserve the setup time of the analog output stage.

The adaptive system is shaded in purple in Figure 7b.

### C. Byproduct operator calculation

The byproduct operators must be updated after each measurement round. Since they only depend on the measurement outcomes, they can also be computed on the rising edge of $X_s$.

The byproduct operators comprise two bits $(x, z)$, which are updated according to the measurement outcomes from the current logical qubit, $m_0^{(1)}$, and the two neighbouring logical qubits, $m_0^{(2)}$ above and $m_0^{(0)}$ below. Any of these three measurements may be XORed in any combination, together with the old byproduct operator values $(x, z)$, to produce new $(x', z')$. Two 3-bit masks $B_x$ and $B_z$ control which of the three measurements outcomes should be XORed together to produce the updated $x$ and $z$, so that the byproduct operators are obtained using the following equations:

$$x' = x \oplus \left( \bigoplus_{j=0}^{2} B_x[j]m_0^{(j)} \right)$$

$$z' = z \oplus \left( \bigoplus_{j=0}^{2} B_z[j]m_0^{(j)} \right).$$

The masks $B_x$ and $B_z$ for each measurement round are chosen in such a way that they combine measurement outcomes from the current and surrounding logical qubit rows to form the updates to the byproduct operators that are shown in Figure 3.

It is sometimes necessary to add a constant (the 1 in Equation (1) for $z'_i$) to the byproduct operators, as in the case of the CNOT pattern. This constant addition is controlled by the commutation correction program, as described in the section below.

The main byproduct operator calculation is shaded in purple in Figure 7b.

### D. Commutation corrections

For the CNOT gate, the commutation correction is performed by mixing the values of the byproduct operators between the control and target logical qubits, as described in Equation (1).

For an arbitrary one-qubit gate, the correction is more complicated, requiring the use of the byproduct operators in the calculation of the measurement settings. However, in order to avoid overwriting these correctional byproduct operators prematurely, it is necessary to store them in a separate register, called the stored byproduct operator register. The correction for the one-qubit gate then amounts to loading this register from the current byproduct operators.

Both these corrections, for the CNOT and the one-qubit gate, require the byproduct operator values and must therefore be calculated on the rising edge of $X_r$ rather than $X_s$. The behaviour of this correction is controlled by a 5-bit value $C$, whose interpretation is shown in Table II.

Most of the time $C = 0$ and the commutation correction does nothing. It is only directly before gate boundaries that a commutation correction must be performed.

The commutation corrections are shaded in orange in Figure 7b.

### E. Program word

The digital system is controlled using a 16-bit program word $P$ which is formed by concatenating the masks and control bits in the previous sections as follows:

$$P = CA_bA_mB_xB_z.$$  

(9)
TABLE II. The table contains the interpretation of the bit fields of \( C \), which controls the commutation correction for the arbitrary one-qubit gate and CNOT gate, and also controls the addition of constants to the byproduct operator. The meaning of bits 2 and 3 depend on whether bits 1 or 4 are set, which are mutually exclusive. If \( C = 0 \) then no operation is performed.

| Gate | Bit 0 | Bit 1 | Bit 2 | Bit 3 |
|------|------|------|------|------|
| \( U \) | 0    | 0    | 0302 | 0    |
|      | 1    | 1    | 0510 | -0.1 |
|      | 2    | 1    | 0342 | -0.2 |
|      | 3    | 0    | 3010 | -0.3 |
| CNOT | 4    | 1    | 0003 | 0    |
|      | 5    | 0    | 0010 | \( \pi/2 \) |
|      | 6    | 0    | a013 | \( \pi/2 \) |
|      | 7    | 1    | 0002 | 0    |
|      | 8    | 1    | 0012 | \( \pi/2 \) |
|      | 9    | 1    | 0010 | \( \pi/2 \) |

Each logical qubit requires its own set of program words, one per measurement round.

Table III shows an example calculation for the two qubit computation comprising a one-qubit gate \( U = R_x(0.3)R_y(0.2)R_z(0.1) \) on qubit 0, followed by a CNOT between qubits 0 and 1 (qubit 0 is the control). The program \( P_i \) (written in hexadecimal in the table) combines the measurement outcomes \( m_i \) (randomly generated) to produce the adaptive measurement setting \( s_i \) and the byproduct operators \( b_i \) (the least significant bit is \( z \)) for the \( i^{th} \) qubit. The basis measurement angles \( \theta_i \) are included for completeness (\( s_i \) is combined with \( \theta_i \) to produce the measurement angle \( \phi_i \)).

TABLE III. Example two-qubit computation comprising a one-qubit gate \( U = R_x(0.3)R_y(0.2)R_z(0.1) \) on qubit 0, followed by a CNOT between qubits 0 and 1 (qubit 0 is the control). The program \( P_i \) (written in hexadecimal in the table) combines the measurement outcomes \( m_i \) (randomly generated) to produce the adaptive measurement setting \( s_i \) and the byproduct operators \( b_i \) (the least significant bit is \( z \)) for the \( i^{th} \) qubit. The basis measurement angles \( \theta_i \) are included for completeness (\( s_i \) is combined with \( \theta_i \) to produce the measurement angle \( \phi_i \)).

| Gate | \( m_0 \) | \( P_0 \) | \( \theta_0 \) | \( s_0 \) | \( b_0 \) | \( m_1 \) | \( P_1 \) | \( \theta_1 \) | \( s_1 \) | \( b_1 \) |
|------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| \( U \) | 0      | 0      | 0302   | 0      | 0      | 0002   | 0      | 0      | 0      | 0      |
|      | 1      | 1      | 0510   | -0.1   | 1      | 10     | 0010   | 0      | 0      | 0      |
|      | 2      | 1      | 0342   | -0.2   | 1      | 11     | 0      | 0002   | 0      | 0      |
|      | 3      | 0      | 3010   | -0.3   | 0      | 11     | 1      | 5010   | 0      | 0      |
| CNOT | 4      | 1      | 0003   | 0      | 0      | 10     | 0      | 0002   | 0      | 0      |
|      | 5      | 0      | 0010   | \( \pi/2 \) | 0      | 10     | 0030   | 0      | 0      | 0      |
|      | 6      | 0      | a013   | \( \pi/2 \) | 0      | 10     | 0022   | 0      | 0      | 0      |
|      | 7      | 1      | 0002   | 0      | 0      | 10     | 0010   | 0      | 0      | 10     |
|      | 8      | 1      | 0012   | \( \pi/2 \) | 0      | 01     | 0      | 0002   | 0      | 0      |
|      | 9      | 1      | 0010   | \( \pi/2 \) | 0      | 11     | 0      | 0010   | 0      | 0      |

F. FPGA Implementation of the design

In order to analyse the timing characteristics of the system, we wrote an FPGA implementation of the design using VHDL, targeting a Xilinx Kintex-7 FPGA (part no. xc7k70tfbg484-2). We used the synthesis tool Xilinx Vivado 2020.2 to implement the design and perform static timing analysis.

We used the mixed-mode clock manager (MMCM) to generate the two out-of-phase clocks \( X_p \) and \( X_r \) from the (external) system clock \( X_s \). The program was stored in memory generated by an instance of the distributed memory generator IP [23], configured as ROM so that we could store the program in a coefficients file for the purpose of the verifying the design.

The use of logic and input/output (I/O) pads in the design is provided for 1 logical qubit and 20 logical qubits in Table IV. The data was obtained from the utilisation report generated by Vivado after implementing the system for each number of logical qubits. The number of logic elements scales more than linearly between 1 and 20 logical qubits because the synthesis tool optimises away logical qubit interconnects in the single logical qubit case. However, the overall utilisation of flip-flops and look-up tables in the design is very low (< 1% of device resources), because the calculations involved in the design are quite simple.

The use of I/O pads is quite high, due to the need for one measurement input \( m \), one adaptive measurement setting \( s \) and two byproduct operator lines per logical qubit. In our design, the total number of I/O pads required is

\[
K = 4N + 4,
\]

where \( N \) is the number of logical qubits. This includes four common signals: the input clock \( X_p \); the clock-islocked output signal from the MMCM; a reset signal; and an enable signal. By accessing the byproduct operators via a low speed serial interface, it would be possible to reduce this pin count to

\[
K \sim 2N,
\]

which includes only the measurement inputs \( m \) and adaptive measurement setting outputs \( s \). On the largest FPGA in the 7-series family [26], the Virtex-7 xc7v2000t device (which has 1200 user I/O pads), this provides an upper bound on the number of logical qubits (cluster state rows) of \( N \sim 600 \).

Input/output delays are also a bottleneck for performance in the FPGA design, as we show in Section VI. The Xilinx 7-series devices were chosen because they have a level-sensitive latch built into their input logic slice (LCDE) [27], which forms the first stage of the digital system.

A disadvantage of the design is that it is not possible to place the output \( s \) in the output logic slice, because there is combinational logic between the final register and
TABLE IV. Utilisation of flip-flops, look-up tables and input/output pads (I/O) in the design, for N=1 logical qubit and N=20 logical qubits, for the control system (CS) in Figure 7 and the full design. The proportion of device resources is included in the utilisation (Util.) columns.

| N     | Flip-flops | Look-up tables | Input/output |
|-------|------------|----------------|--------------|
|       | CS         | Full Util.     | CS           | Full Util.   | Full Util.   |
| 1     | 10         | 24 0.03%       | 5            | 11 0.03%     | 8 2.8%       |
| 20    | 237        | 476 0.89%      | 137          | 364 0.58%    | 84 29.5%     |

The state of the cluster state simulator at each measurement round is written to a file, which is used as the input to the hardware simulator. It contains the program word and the measurement outcomes, which are the inputs to the digital system. It also contains the value of the adaptive measurement settings, the byproduct operators and the stored byproduct operators, which are the outputs from the digital system.

B. VHDL testbenches

The function of the digital system was verified using testbenches written in VHDL. The testbenches read stimulus and output data from the simulation output file described in the previous section.

The output from the system, the adaptive measurement setting and the byproduct operators, are compared with the values from the simulation file. The simulation passes if all the values are equal, which is tested automatically. An example waveform output from the testbench, for a single logical qubit, is shown in Figure 8.

VI. TIMING ANALYSIS

We used static timing analysis to establish the maximum operating frequency of the design and to obtain the input/output delays associated with the system. The critical path is made up of two components:

- The path from the input port \( P \) (clocked on the rising edge of \( X_p \)) to the byproduct operator register (loaded on the rising edge of \( X_s \))
- The path from the shift register output (loaded on the rising edge of \( X_s \)) to the output port \( s \) (clocked on the rising edge of \( X_p \)).

By modifying the phase shift of \( X_s \) relative to \( X_p \), it is possible to allocate more time to one path or the other. The phase of \( X_r \) must also be adjusted to allow timing closure of paths between the \( X_s \) and \( X_r \) clock domains. We established the maximum operating frequency \( F_{\text{max}} \) of the system by manually adjusting the phase of \( X_s \) and \( X_r \) to balance the worst negative setup slack between the critical paths, while increasing the frequency of the design, until both paths fail to meet timing. Using this method, we obtained \( F_{\text{max}} = 190 \text{ MHz} \) using phase(\( X_s \)) = 220° and phase(\( X_r \)) = 300°. The phase difference 80° between \( X_s \) and \( X_r \) represents the amount of the time taken for the internal FPGA logic to process the latched measurement outcome before it is reset.

We then performed the timing analysis at each frequency between 10 MHz and 190 MHz, in steps of 10 MHz, to establish the most generous input and output constraints that still allow timing closure at each frequency. All input/output constraints are expressed with respect to the external clock \( X_p \) (the system clock).
The input constraint is specified by the clock-to-out time $t_{co}$ of the input signal $m$, which is equal to the time delay between the rising edge of $X_p$ and the pulse generated by the input analog system at $m$. This time constrains the analog characteristics of the single-photon detector amplifier.

The output constraint is the setup time $t_{su}$ of the output signal $s$ with respect to the system clock $X_p$, which is the delay between the time that $s$ transitions at the boundary of the FPGA and the next rising edge of $X_p$. This time determines the required operating speed of the output DAC system and modulator drivers, which must be able to set the voltages of the modulators before the next photon arrives on the rising edge of $X_p$.

The input/output timing constraints are plotted as a function of frequency in Figure 9. The input constraint is systematically more generous than the output constraint, because of the choice of phase of $X_s$. The sum of the input and output constraints must be less than the total input/output slack, also shown in the figure.

Figure 10 shows a graph of the proportion of the clock cycle $X_p$ taken up with digital processing, as a function of frequency. It is clear that at higher frequencies, the digital processing dominates the clock cycle, leaving very little time for the analog amplifier systems.

At a representative clock frequency of 150 MHz, the photons would need to be delayed for 6.67 ns in either an optical fibre or a waveguide delay line. Assuming a standard silicon-on-insulator (SOI) platform, the delay line must be approximately 83 cm, assuming a mode index of $\sim 2.4$ [19].

We re-implemented the design targeting a higher end FPGA (Xilinx Kintex Ultrascale+, part no. xcku5p-ffvd900-3-e), to see whether the maximum clock frequency could be improved. We found that the maximum clock frequency increased to $F_{\text{max}} = 220$ MHz using phase($X_s$) = 140° and phase($X_r$) = 230°. In this case, at the maximum clock frequency, less time is allocated to the input analog system compared to the 7-series FPGA. The phase difference of 90° between $X_s$ and $X_r$ indicates that approximately the same time (1.125 ns) is taken by the internal digital system compared to the 7-series FPGA (1.152 ns).

VII. EXTENDING THE DESIGN TO MORE REALISTIC SYSTEMS

The model of photonic quantum computing described here, with a deterministic cluster state generator, is a substantial simplification compared to what is required for a real photonic quantum computer. Firstly, we have ignored the question of cutting out the correct shaped cluster state for the given circuit. This would entail two rounds of measurement per column, because removing qubits causes measurement setting dependencies within
An important complication is the lack of a deterministic cluster state generator. There are schemes for generating probabilistic cluster states (i.e. cluster states that may contain missing edges); this non-determinism must be overcome by tracking the successfully generated cluster state edges in real time, and mapping the measurement pattern dynamically onto the resulting graph [25].

In this scheme, it would be necessary to hold many columns of the cluster state in delay lines at a time, rather than just one, in order to keep enough depth to correct for dead-ends in the partial cluster state. For a given delay line length, the photon clock frequency $X_p$ would have to be proportionally increased in order to fit multiple photons in the same length of delay line. At the same time, the algorithmic complexity of the digital system would increase substantially with the inclusion of a real-time algorithm to track the structure of the unfolding cluster state before the adaptive measurement calculation.

On the other hand, it is possible to optimise the measurement patterns for ease of implementation in a photonic setting. For example, by inserting the identity pattern ($I$ in Figure 1b) between the $X$ and $Z$ rotations in the arbitrary one-qubit gate [12], the timing requirements on the adaptive measurement setting could be significantly reduced, at the expense of longer measurement patterns. This approach is related to the percolation system described above, where logical qubit “wires” can be implemented using the identity pattern and the control system is responsible for placing measurement patterns on cluster qubits in real time.

Finally, if an SNSPD is used as the single-photon detector, the electronic control system may be required to operate at cryogenic temperatures so as to avoid data delays into and out of the cryostat. In this case, static timing analysis using a program such as Vivado is not valid. A 7-series FPGA has been found to operate at 4 K, with a slight performance increase across many metrics [29]. However, timing jitter inside the FPGA increases slightly, meaning that timing closure may not be achievable close to $F_{\text{max}}$.

The complex set of factors described above in a realistic photonic MBQC design makes it impossible to make general statements about the performance of classical control systems in this setting. In order to establish quantitative performance bounds, it is necessary to implement and analyse a simple example system incorporating these more realistic details.

VIII. DISCUSSION

In contrast to every other approach to building quantum computers, photonic MBQC relies on manipulating and measuring flying-qubit states. This means that the effective ‘lifetime’ of a qubit in these platforms is ultimately bounded by the length of time that photons can be kept circulating inside an optical delay line, either on or off-chip. The fact that the spatial and temporal properties of the system can not be decoupled is at the root of many of the unique timing constraints that photonic approaches need to satisfy. This is in contrast to other matter-based systems where the qubit lifetime is, for first
order, unrelated to its spatial footprint.

In an integrated photonic approach, the only way to get longer qubit lifetimes is by increasing the length of the on-chip delay line. Even with a high-index-contrast platform like SOI, which allows low-loss bend radii < 5 µm, getting realistic delays beyond 2 ns–3 ns is extremely challenging, both due to the increasing insertion loss (1 dB cm\(^{-1}\)–2 dB cm\(^{-1}\)) and the increasing on-chip footprint (spiral delay lines with lengths ∼10 cm) [19]. One solution to the timing constraints is to use an integrated photonic quantum memory [30] which would make photonic MBQC implementations closer to their matter-based counterparts by allowing one to map quantum information on to a long-lived spin / hyperfine transition.

Longer delays can be obtained in principle by using low-loss optical fibers off-chip, although this approach is not without its own trade-offs. Losses in the grating couplers involved in getting the light on and off the chip must be accounted for, in addition to losses involved in the optical switching network needed to get the cluster states to the grating couplers. These requirements can in principle be satisfied by state-of-the-art lithium niobate modulators, however the size and form factor are not really suitable for very large scale integration, which is a critical requirement from a systems perspective. State-of-the-art silicon modulators are very far from ideal, especially in terms of insertion loss (∼6 dB / device) [31]. It is likely that a performance improvement could be obtained by implementing the digital design using an ASIC. Critical path delays due to logic have been found to decrease by 3-4 times in standard-cell ASIC designs [32]. However, this may not translate to a performance improvement in this design because the majority of the critical path delays come from the input/output buffers, not the logic. To improve this, it may be possible to utilise very high speed latches and output buffer designs, with delays on the order of 100 ps [33]. A full analysis of the input/output buffer delays should be performed in tandem with the design of the input/output analog systems, to ensure compatibility between the two systems. At this point, the requirement for absolute synchronisation between the cluster state generator and the digital control system, using a system synchronous architecture [34] may become the bottleneck to the design. Such schemes are often limited to speeds up to 200 MHz–300 MHz, due to clock skew and data path delays [35].

**IX. CONCLUSION**

We have provided a practical description of the measurement patterns for one-qubit gates and the CNOT gate and shown in detail how to implement a digital control system for photonic MBQC, in the presence of an ideal path-encoded photonic cluster state generator. It is clear from the timing analysis of our FPGA implementation of this system that it places substantial constraints on the input and output analog systems needed at the interface between the classical and quantum subsystems. For example, at a photon clock frequency of 150 MHz, the total time available for the input and output analog processing is 1.59 ns out of the total period 6.67 ns. The remaining 5.08 ns is consumed by the logic delays inside the FPGA design. At the same time, a photon clock period of 6.67 ns corresponds to a long delay line (∼83 cm), that will occupy quite a large footprint in an integrated implementation of photonic MBQC.

While in this work we have implemented a proof-of-principle design to study the constraints, it is clear that the digital system and implementation can be further optimised. For example, since the maximum frequency of our design is less than 200 MHz and the maximum clock frequency of the target FPGA is greater than 600 MHz, it may be possible to create a multi-cycle digital design so as to properly register the inputs and outputs and place them in dedicated input/output slices. This would likely increase the maximum clock frequency somewhat while maintaining the input/output delay constraints.

Incorporating the features of a realistic photonic MBQC system, where the cluster state generator is probabilistic, adds an additional level of algorithmic complexity to the design. It is likely that analysis and implementation of a minimal system design is necessary to address the additional overheads that are involved in these settings.

We would like to emphasize that most of the constraints considered in this paper are practical, rather than fundamental in nature. We have shown that, for our reference design, the input and output analog systems must have a combined latency on the order of hundreds of picoseconds. While these specifications might be challenging, they also provide an exciting design opportunity for classical high-speed optoelectronics. In our view, the viability of photonic MBQC rests on the improvement of the classical subsystem just as much as it does on improving the quantum resources (cluster state generation). Understanding how these timing constraints can be relaxed to the point where they can be satisfied by existing circuit architectures/amplifier topologies is a necessary near-term goal. We believe this can be achieved by analysing ASIC implementations of the circuits discussed here, with a focus on reducing the input/output routing and buffer delays which limit the maximum operating frequency of the design. On the other hand, there is also a need to rethink the photonic MBQC architecture with latency as the primary constraint and explore the improvements that can be achieved through architectural changes in the design.

**Appendix A: Gate based quantum computing**

This appendix contains a brief overview of quantum computing in the gate-based model. The basic unit of quantum computation is the qubit, which is a two-state
system, analogous to a bit, except complex linear combinations of the zero-state (denoted $|0\rangle$) and the one-state (denoted $|1\rangle$) are also valid states. The states $|\psi\rangle$ of a qubit can be expressed as

$$|\psi\rangle = a|0\rangle + b|1\rangle, \quad a \in \mathbb{R}, b \in \mathbb{C}. \quad (A1)$$

The qubit can only ever be observed in the state $|0\rangle$ or $|1\rangle$, with probabilities given by the ratio of $|a|^2$ to $|b|^2$. The act of observing the qubit is called a measurement. The absolute values of $a$ and $b$ have no independent physical meaning, so the condition $|a|^2 + |b|^2 = 1$ is imposed so that the probabilities are equal to $|a|^2$ and $|b|^2$. Likewise, the arguments of the complex numbers $a$ and $b$ have no physical meaning, so it is possible to impose $a \in \mathbb{R}$ without loss of generality. The argument of $b$ is then the relative phase between $|0\rangle$ and $|1\rangle$.

The states of a single qubit can be identified with points on the surface of a sphere, called the Bloch sphere, as shown in Figure 2. The mapping between the $a$ and $b$ and the real number angles $\theta$ and $\phi$ is given by the identity:

$$a|0\rangle + b|1\rangle = \cos(\theta/2)|0\rangle + e^{i\phi} \sin(\theta/2)|1\rangle.$$

The angle $\phi$ in the equator of the Bloch sphere is the relative phase between $|0\rangle$ and $|1\rangle$, and the angle $\theta$ controls the probability of observing $|0\rangle$ or $|1\rangle$ upon measurement.

a. One-qubit gates

The state of the qubit can be changed by applying a quantum gate. The valid gates on a single qubit, called one-qubit gates, are those which correspond to a rotation of the points on the Bloch sphere about any axis, by any angle. The gates which perform rotations of the state about the $x$, $y$ and $z$ axes are denoted $R_x(\alpha)$, $R_y(\alpha)$ and $R_z(\alpha)$, where $\alpha$ is the angle of rotation according to the right-hand rule. An arbitrary one-qubit rotation can be formed by applying $x$- and $z$-rotations in sequence as $R_z(\zeta)R_x(\eta)R_z(\xi)$ (applied from right to left). This follows from the decomposition using Euler angles of an arbitrary rotation into $x$- and $z$-rotations.

b. Measurement

When a qubit is measured, it always collapses to either the state $|0\rangle$, with probability $|a|^2$, or the state $|1\rangle$, with probability $|b|^2$. This is called a computational basis measurement. However, it is possible to generalise the concept of measurement so that an “observation” causes the qubit to collapse into the state $|0\rangle$ or the state $|1\rangle$, which are any two antipodal points on the Bloch sphere, joined by a line $L$. This observation is made by using one-qubit gates to transform the line $L$ to the line through $|0\rangle$ and $|1\rangle$, and then making a computational basis measurement. For example, to measure along the line denoted $L$ in Figure 2 it is necessary to apply a $z$-rotation $R_z(-\phi + \pi/2)$ to align the state $|0\rangle$ with the positive $y$ axis, followed by an $x$-rotation $R_x(\pi/2)$ to obtain $|0\rangle$.

It is possible to measure along any line in this way by applying an arbitrary one-qubit gate $R_z(\alpha)R_x(\beta)R_z(\gamma)$ and then measuring in the computational basis. It is important to realise that general measurements involve the application of a one-qubit gate before making a computational basis measurement.

c. Two-qubit gates

The states of two qubits can be expressed analogously to Equation (A1) as

$$|\psi\rangle = a|00\rangle + b|01\rangle + c|10\rangle + d|11\rangle, \quad (A2)$$

where $a \in \mathbb{R}$ and $b, c, d \in \mathbb{C}$. The sum is over all the four possible states that the two qubits could be observed in. As with the single qubit case, $|a|^2 + |b|^2 + |c|^2 + |d|^2 = 1$ is imposed, and the probability of obtaining, for example, $|01\rangle$, is given by $|b|^2$.

There is no equivalent of the Bloch sphere for graphically presenting the states of two qubits. An example of a two-qubit gate is the CNOT gate. The action of this gate on the state (A2) above is

$$|\psi\rangle = a|00\rangle + b|01\rangle + c|10\rangle + d|11\rangle \quad \mapsto \quad |\psi\rangle = a|00\rangle + b|01\rangle + c|11\rangle + d|10\rangle, \quad (A3)$$

that is, the states $|10\rangle$ and $|11\rangle$ are reversed. The interpretation of this gate is that the first (leftmost) qubit controls whether a NOT gate is applied to the second (rightmost) qubit. The first qubit is called the control qubit, and the second qubit the target.

Analogously to the way that a NAND gate is universal for digital logic, the CNOT gate combined with the basic rotations $R_x(\alpha)$, $R_y(\alpha)$ and $R_z(\alpha)$ are universal for quantum computation. To build up any complicated computation, all that is required is to apply the correct string of one- and two-qubit gates, one after the other, to a set of qubits. For example, in Figure 1, an arbitrary one-qubit gate $U = R_z(\zeta)R_x(\eta)R_z(\xi)$ is applied to the top qubit, and a CNOT gate is applied between the bottom two qubits.

Appendix B: CNOT Measurement Pattern

We use a reduced measurement pattern for the CNOT gate that only uses two rows of cluster qubits, instead of the three row pattern in [13]. The pattern is derived using the same method outlined in Section II.G.7. of that paper for the calculation of the three-row CNOT gate. In order to explain the derivation, we begin by discussing some
INTERNAL

FIG. 11. The labelling of the cluster qubits for the purpose of deriving the CNOT measurement pattern. When a gate is realised in MBQC, the input state starts on the IN column and is teleported to the OUT column \( R \) and \( S \) by applying the measurement pattern. The black dots show the location of the correlation operators \( K_a \) in Equation (B8) below.

technical aspects of cluster states, and describe what it means for a measurement pattern to realise a gate.

A cluster state \( |\phi_C\rangle \) on \( N \) qubits is created by placing all the qubits in the \( |+\rangle \) state, and then applying CZ gates between each pair of qubits that should have an entanglement link (shown as red line segments in Figure 11). It can be shown [14] that cluster states satisfy the eigenvalue equations derived from Equation (B1) and a given measurement pattern, to the gate \( G \) which that measurement pattern realises. The content of the theorem is that it is only necessary to check how a cluster state \( |\phi_C\rangle \) is affected by the measurement pattern (where the state of qubits 0 and 6 are \( |+\rangle \)) in order to establish that the measurement pattern works for any other IN state \( |\phi\rangle \). In the interest of simplicity, We state the theorem for the case of a two-qubit gate \( G \) like the CNOT gate:

**Theorem 1.** Suppose that a cluster state \( |\phi_C\rangle \) is prepared on the pattern of 14 qubits shown in Figure 11 for the purpose of realising a two-qubit gate \( G \) acting on logical qubits labelled \( C \) and \( T \). Suppose that a set of measurements \( M \) is performed on the INTERNAL cluster qubits 1 to 5 and 7 to 11, resulting in a state \( |\psi_C\rangle \) on the remaining qubits (0, 6, \( R \) and \( S \)), which satisfies the following sets of eigenvalue equations:

\[
X_0 \left[ GX_CG^\dagger \right]_{R,S} |\psi_C\rangle = (-1)^{\lambda_x} |\psi_C\rangle \tag{B3}
\]

and

\[
X_6 \left[ GX_TG^\dagger \right]_{R,S} |\psi_C\rangle = (-1)^{\mu_x} |\psi_C\rangle \tag{B4}
\]

Then the measurement pattern in which the inner qubits are measured according to \( M \), and the IN cluster qubits 0 and 6 are measured in the \( X \)-basis, realises the gate \( GB \), where the byproduct operators \( B \) for the logical qubits \( C \) and \( T \) are given by

\[
(x_C, z_C) = (\lambda_z, m_0 + \lambda_x)
\]

\[
(x_T, z_T) = (\mu_z, m_6 + \mu_x), \tag{B5}
\]

where \( m_a \) is the outcome of the measurement of the \( a \)-th cluster qubit.

The square bracketed terms in Equations (B3) and (B4) are computed in terms of the logical qubits \( C \) and \( T \), without reference to cluster qubits. Any terms involving \( C \) and \( T \) are then interpreted as applying to the cluster qubits \( R \) and \( S \). For example, when \( G = \text{CNOT} \),

\[
[GX_TG^\dagger]_{R,S} = [X_CX_T]_{R,S} = X_RX_S.
\]

To apply the theorem to the CNOT gate, it is therefore necessary to obtain the following eigenvalue equations

\[
X_0 (X_RX_S) |\psi_C\rangle = (-1)^{\lambda_x} |\psi_C\rangle \tag{B6}
\]

and

\[
X_6 (X_S) |\psi_C\rangle = (-1)^{\mu_x} |\psi_C\rangle \tag{B7}
\]

To obtain these equations, begin with the cluster state \( |\phi_C\rangle \) on the two-row CNOT shape shown in Figure 11.
and multiply together the correlation operators in Equation (B1) so as to obtain the following four equations:

\[
|\phi_C\rangle = K_0 K_2 K_3 K_4 K_6 K_8 |\phi_C\rangle \\
= -X_0 Y_2 X_3 Y_4 X_R X_0 X_S |\phi_C\rangle \\
|\phi_C\rangle = K_1 K_2 K_4 K_5 |\phi_C\rangle \\
= Z_0 Y_1 Y_2 Y_3 Z_R |\phi_C\rangle \\
|\phi_C\rangle = K_6 K_3 K_10 K_8 |\phi_C\rangle \\
= X_0 X_8 X_10 X_S |\phi_C\rangle \\
|\phi_C\rangle = K_4 K_5 K_7 K_9 K_{11} |\phi_C\rangle \\
= Y_4 Y_5 Z_R Z_4 X_7 X_9 X_{11} Z_S |\phi_C\rangle. 
\] (B8)

The right hand sides are obtained by repeated application of the equation \(X_a Z_a = i Y_a = -Z_a X_a\). Note that Pauli operators on different qubits commute.

As with any pattern derived using this method, the choice of operators \(K_a\) in the above equations is motivated by two goals:

- The equations must contain the correct IN and OUT terms in Equations (B6) and (B7). These terms are coloured red in the equations;

- The Pauli operators on the INTERNAL cluster qubits agree between all the equations. That is, for each cluster qubit \(a\), only \(X_a\) or \(Y_a\) appears across all the equations. For example, when \(a = 4\), only \(Y_4\) appears (three times, shown in blue), and there are no instances of \(X_4\). It is these operators that define the measurement bases \(M\) for each qubit \(a\) in the INTERNAL group of cluster qubits.

When the INTERNAL qubits are measured according to \(M\), the Pauli terms disappear \[^{10}\] Section 10.5.3, and each one contributes a sign according to its measurement outcome \(m_a\), to give the following equations on the reduced state \(|\psi_C\rangle\):

\[
X_0 X_R X_S |\psi_C\rangle = (-1)^{m_2 + m_3 + m_4 + m_{10}} |\psi_C\rangle \\
Z_0 Z_R |\psi_C\rangle = (-1)^{m_1 + m_3 + m_4 + m_5} |\psi_C\rangle \\
X_6 X_S |\psi_C\rangle = (-1)^{m_8 + m_{10}} |\psi_C\rangle \\
Z_6 Z_R Z_S |\psi_C\rangle = (-1)^{m_4 + m_5 + m_7 + m_9 + m_{11}} |\psi_C\rangle. 
\]

These equations are in the form of Equations (B6) and (B7), and define the values of \(\lambda_x, \lambda_y, \mu_x, \mu_y\) in terms of the measurement outcomes \(m_a\). As a result, it follows from the theorem above that the measurement pattern consisting of \(M\), plus \(X\) measurements on the IN qubits, realises the gate \((\text{CNOT})_B\), where the byproduct operator \(B\) found using Equation (B5) to be

\[
(x_C, z_C) = (m_1 + m_2 + m_4 + m_5, 1 + m_0 + m_2 + m_3 + m_4 + m_{10}) \\
(x_T, z_T) = (m_4 + m_5 + m_7 + m_9 + m_{11}, m_6 + m_8 + m_{10}).
\] (B9)

Finally, the byproduct operator can be commuted past the CNOT gate to obtain

\[
(Z_C^{1+m_0+m_2+m_3+m_4+m_6+m_8} X_C^{m_1+m_2+m_4+m_5} Z_T^{m_6+m_8+m_{10}} X_T^{m_4+m_5+m_7+m_9+m_{11}})\text{CNOT}. 
\] (B10)

The contributions to the byproduct operators given in this formula are depicted in Figure 3 and stated in Equations (1) and (2).

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