Equivalent Circuit Models for Strained Si NMOSFET Using Verilog-A

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Abstract. Equivalent circuit models for strained Si NMOSFET at DC and AC working conditions are investigated in this article. The intrinsic region, source/drain parasitic regions, and substrate parasitic resistance are proposed respectively. The model admits analytical solution using the quasi-two-dimensional analysis and coherent smoothing functions, a unified drain current model is presented. We also present a unified charge model with the charge as the state variable. Model parameters are extracted from the experimental results by software. Furthermore, simulations for strained Si NMOSFETs are realized using Verilog-A.

Introduction

Strained Silicon (SSi) has been used to enhance mobility of carriers in the classical bulk MOSFET structures [1,2]. It has become an integral part of the CMOS process, especially for chips intended for RF applications [3]. Device structures and implementations of process for strained Si MOSFETs have been the focus of intense research in recent years [4]. However, equivalent circuits of strained Si for circuit simulators are not yet to be investigated in detail. There are few reports on model parameters, meanwhile, proposed model parameters have problems in the features of continuity and smooth I-V and C-V characteristics [5-10]. Recently we proposed equivalent circuits for strained Si NMOSFET at DC and AC working conditions. Smoothing functions and quasi-two-dimensional analysis have been used to meet requirements of continuities and accuracy for analog device model. Model parameters are extracted from the experimental results by software. Furthermore, simulations for strained Si NMOSFETs are realized using Verilog-A, which can be used in SPICE simulator.

Device Structure and Equivalent Circuit Model

As shown in Fig1.(a) the strained Si NMOSFET used in this letter were fabricated on a p-type Si substrate in our lab, next the graded SiGe buffers was grown on it. Following virtual substrate (relaxed SiGe) growth, the strained Si channel was pseudomorphically grown. The cross-sectional transmission electron micrograph (TEM) image of the strained Si NMOSFET is shows in Fig1.(b).
Figure 1. (a) Schematic diagram of a strained Si NMOSFET and (b) Cross-sectional TEM micrograph of Strained Si NMOSFET.

Based on the structure and working principle of strained Si NMOSFET, the equivalent circuit at DC operation condition is shown in Fig. 2 (a). In Fig. 2 (a) S and D are the source and drain nodes as specified in a SPICE input file; S’ and D’ are the corresponding internal node respectively representing channel portion of the device. $R_{S1}$ and $R_{D1}$ are conductance of the source and drain series resistance in the strained Si layer, and $R_{S2}$ and $R_{D2}$ are conductance of the source and drain series resistance in the relaxed SiGe layer, respectively. The gate and bulk nodes are represented by G and B, B’ is also the internal node. Since the gate is separated from the source and drain by an insulator, the gate is assumed to be a DC open circuit. The drain-source current is represented by a voltage controlled current source $I_{DS}$. $I_{\text{sub}}$ is a substrate current, which results from impact ionization. $D_{S1}$, $D_{S2}$, $D_{D1}$, and $D_{D2}$ are source/drain substrate parasitic diodes in strained Si layer and relaxed SiGe layer. $D_{SB1}$, $D_{SB2}$, $D_{DB1}$ and $D_{DB2}$ are the DC source/drain pn junction currents in strained Si layer and relaxed SiGe layer respectively. $D_B$ is parasitic strained Si-relaxed SiGe heterojunction diode in the channel. $R_B$ is terminal resistance at the bulk.

Fig. 2 (b) shows an AC equivalent circuit for strained Si NMOSFET. $C_{ij,t}$ is the total capacitance between terminal i and j:

$$C_{ij,t} = C_{ij} + C_{ij,p},$$  \hspace{1cm} (1)
Each element $C_{ij}$ of this capacitance describes the dependence of the charge at the terminal $i$ with respect to the voltage applied at the terminal $j$ with all other voltage held constant [11]: and $C_{ij,p}$ is the parasitic capacitance between terminal $i$ and $j$. The transcapacitances $C_m, C_{mb}, C_{mx}$ are defined as

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}, i \neq j$$

(2)

$$\begin{align*}
C_m &= C_{dg,t} - C_{gd,t} \\
C_{mb} &= C_{db,t} - C_{bd,t} \\
C_{mx} &= C_{bg,t} - C_{gb,t}
\end{align*}$$

(3)

**Model Parameters**

Recently, using the gradual channel approximation (GCA) and coherent quasi-two-dimensional (2D) analysis, as well as taking into account the effects of short channel effect (SCE), narrow channel effect (NCE), non-uniform doping effect, and drain-induced barrier lowering (DIBL) effect [11,12]. The threshold voltage $V_{TH}$ is:

$$V_{TH} = f_1(V_{GS}, V_{DS}, V_{BS}, SSi, SiGe)$$

(4)

Furthermore, according to Refs.[12,13], a unified drain current model can be expressed as:

$$I_{DS} = f_2(V_{GS}, V_{DS}, V_{BS}, SSi, SiGe)$$

(5)

The model describes current characteristics from subthreshold to strong inversion as well as from the linear to the saturation operating regions with a smoothing function, and guarantees the continuities of the drain current and its derivatives. The model accuracy is enhanced by including carrier velocity saturation and channel length modulation effects.

Using the charge as the state variable, unified charge models are:
\[ Q_I = f_3 (V_{GS}, V_{DS}, V_{BS}, SSi, SiGe) \]  
\[ Q_B = f_4 (V_{GS}, V_{DS}, V_{BS}, SSi, SiGe) \]
\[ Q_G = -Q_B - Q_I \]

where \( Q_G \) and \( Q_B \) are the charges in the gate and bulk respectively, \( Q_I \) is the channel charge. The model describes device characteristics from subthreshold to strong inversion as well as from the linear to the saturation operating regions using a smoothing function, and guarantees the continuities of charges and capacitances.

**Results and Discussion**

Model parameters of the strained Si NMOSFET are extracted from the experimental results by software. Furthermore, equivalent circuit models are presented using Verilog-A, a language to describe analog behavior. The evidence for the validity of equivalent circuit models and model parameters can be derived from the comparison of experimental results.

Fig. 3 (a) plots the output characteristics of the strained Si NMOSFET. The characteristics are quite similar to the conventional Si NMOSFET. The current drive of strained Si NMOSFET is 20-25% larger than classical bulk MOSFET, which fabricated using the same process conditions, due to the higher electron mobility of the strained Si channel. Fig. 3 (b) shows the measured bulk current of the strained silicon NMOSFET. The measured \( I_{sub} \) vs \( V_{gs} \) at a particular \( V_{ds} \) is bell-shape-like, indicating that for a given \( V_{ds} \), initially substrate current \( I_{sub} \) increases with increasing \( V_{gs} \) due to an increase in the drain current \( I_{DS} \). Further increase in \( V_{gs} \) eventually results in a decrease in due to the increase in \( V_{dsat} \), which in turn reduces the channel field.

Using Eq.(6c) in Eq.(2), we get a unified analytical model \( C_{gb} \), as shown in Fig.4(a). A “plateau” is obviously observed in the accumulation region, and the capacitance \( C_{gb} \) saturates to the oxide capacitance \( C_{OX} \) deep in accumulation. When applied voltage \( V_{gb} \) goes from negative to positive, the accumulated holes resided initially in the strained Si layer gradually transfer to SiGe layer, and the capacitance \( C_{gb} \) shifts from

\[ C_{gb} = \left[ C_{ox}^{-1} + C_C^{-1} \right]^{-1} \]

to

\[ C_{gb} = \left[ C_{ox,eff}^{-1} + C_{C,SiGe}^{-1} \right]^{-1} \]

giving rise to the plateau, \( C_C \) is the bulk capacitance, \( C_{ox,eff} \) is the effect oxide capacitance, and \( C_{C,SiGe} \) is the SiGe layer capacitance [10].
Figure 2. Measured and modeled (a) drain currents $I_{DS}$ as a function of $V_{ds}$ at different gate voltage $V_{gs}$, and (b) substrate currents $I_{sub}$ as a function of $V_{gs}$ for different drain voltage $V_{ds}$.

Fig.4 (b) shows normalized plots of measured and modeled $C_{GS}$, $C_{GD}$, and $C_{GB}$ as a function of $V_{gs}$. The model describes device characteristics from subthreshold to strong inversion as well as from the linear to the saturation operating regions using a smoothing function, and guarantees the continuities of charges and capacitances. $C_{GB}$ is much smaller in strong inversion than in weak inversion, because in strong inversion, with the formation of the inversion layer, the influence of the substrate potential on the gate charge is shielded; but in weak inversion, $Q_I$ increases with $V_{GS}$, and the control of $V_B$ on $Q_G$ is decreases. In addition, $C_{GS}$ is smaller in weak inversion than in strong inversion, because in weak inversion $Q_I = 0$, $Q_G = -Q_B$ according to Eq.(6c), $Q_B$ is mainly determined by the longitudinal electric potential, and the control of $V_S$ on $Q_B$ is week. With the increasing of $V_{gs}$ beyond saturation, the transistor enters the linear region. The shielding effect of the drain is released, its influence of channel charge is increasing. This means that the influence of the source to the channel charge is reduced, and the control of $V_S$ on $Q_G$ is decreases, $C_{GS}$ is decreased consequently. $C_{GD}$ is small both in weak inversion for the same reason as $C_{GS}$. In saturation region, the inversion layer is cut off, the control of $V_D$ on $Q_G$ is shielded, and therefore $C_{GD}$ is small. With the increasing of $V_{gs}$, the transistor enters the linear region. The shielding effect of the drain is released, its influence of channel charge is increasing, $C_{GD}$ increases continuously. The results from our model match the experimental data well, giving evidence for their validity.
Conclusion

In conclusion, we have successfully established equivalent circuits of strained silicon NMOSFETs at DC and AC working conditions. Model parameters are extracted from the experimental results by software, which have analytical and continuous I-V and C-V characteristics. Comparisons between the Verilog-A simulation results and measured dates show that equivalent circuits can describe the device characteristics well. It is believed that such equivalent circuits of strained Si are promising for integrated circuits design.

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Reference

[1] A.G. O’Neill, D.A. Antoniadis, Deep submicron CMOS based on silicon germanium technology IEEE Trans. Electron Devices., 43 (1996), 911-918.

[2] W.K. Sun, H.S. Shin, Optimization of Uniaxial Stress for High Electron Mobility on Biaxially strained n-MOSFETs, Solid-State Electronics, 94(2014), 23-27.

[3] C.H. Chou, W.S. Chan, I.C. Lee, C.L. Wang, C.Y. Wu, P.Y. Yang, C.Y. Liao, K.Y. Wang, and H.C. Cheng, High-Performance Single-Crystal-Like Strained-Silicon Nanowire Thin-Film Transistors via Continuous-Wave Laser Crystallization, IEEE Electron Device Lett., 36 (2015), 348-350.

[4] S.H. Olsen, A.G. O’Neil, L.S. Driscoll, S.K. Kwa, S. Chattopadhyay, A.M. Waite, Y.T. Tang, G.R. Evans, D.J. Norris, A.G. Cullis, D.J. Paul, and D.J. Robbins, N-MOSFET performance in single and dual channel strained Si/SiGe CMOS architectures, IEEE Trans. Electron Devices., 50(2003), 1961 -1967.
[5] B. Bindu, Nandita DasGupta, Amitava DasGupta, A Unified Model for Gate Capacitance-Voltage Characteristics and Extraction of Parameters of Si/SiGe Heterostructure pMOSFETs, IEEE Trans. Electron Devices., 53 (2006), 1411-1418.

[6] B. Bindu, Nandita DasGupta, and Amitava DasGupta, Analytical model of drain current of strained-Si/strained-Si$_{1-x}$Ge$_x$/relaxed-Si$_{1-x}$Ge$_x$ NMOSFETs and PMOSFETs for circuit simulation, Solid State Electron., 50(2006), 448-455.

[7] T. Tsunomura, A. Nishida, and T. Hiramoto, Analysis of NMOS and PMOS Difference in $V_T$ Variation With Large-Scale DMA-TEG, IEEE Trans. Electron Devices., 56 (2009), 2073-2080.

[8] H.M. Nayfeh, J.L. Hoyt, D.A. Antoniadis, A physically based analytical model for the threshold voltage of strained-Si n-MOSFETs, IEEE Trans. Electron Devices., 51(2004), 2069-2075.

[9] X. Zhou, S.B. Chiah, W.Z. Shangguan, H.S. Guan, L.K. Bera, N. Balasubramanian, and S.C. Rustagi, Physics-based single-piece charge model for strained-Si MOSFETs, IEEE Electron Device Lett., 27(2006), 62-65.

[10] B. Wang, H.M. Zhang, H.Y.Hu, B. Su, C.Y. Zhou, Y.C. Li, Analytical model for quasi-static C-V characteristics of strained-Si/SiGe pMOS capacitor, Solid State Electron, 79(2013), 258-263.

[11] N. Arora, MOSFET Modeling for VLSI Simulation, Singapore, 2007.

[12] C.Y. Zhou, H.M. Zhang, H.Y. Hu, Y.Q. Zhuang, B. Su, B. Wang, G.Y. Wang, Analytical modeling for drain current of strained Si NMOSFET, Acta Phys.Sin., 62(2013), 0771031-0771038.

[13] C.Y. Zhou, H.M. Zhang, H.Y. Hu, Y.Q. Zhuang, Y. Lv, B. Wang, Y.C. Li, Charge model of strained Si NMOSFET, Acta Phys.Sin., 62(2013), 2371031-2371038.