Design of an Ultrasonic Phased Array Launch System Based on Gigabit Ethernet Transmission

Weili Yu, Yonggang Cao and Huifeng Zheng
College of Metrology and Measurement Engineering, China Jiliang University, Zhejiang, Hangzhou 310018, China.
Email: 15A0202111@cjlu.edu.cn

Abstract. To better use ultrasonic phased array detection technology for underwater object detection and real-time imaging, an ultrasonic phased array launch system based on Gigabit Ethernet transmission was proposed in this work. The principle of phased focusing emission and the UDP communication protocol are analysed. Due to abundant I/O pin resources and internal logic resources, FPGA is used to excite the 32-channel ultrasonic phased array transducer, and the communication protocol is Gigabit Ethernet UDP. Generally, the delay parameters are sent to the FPGA in real-time and high-speed, and then transmitted to the pulse signals. By using an integrated chip Max4940, the pulse signals are amplified and delivered to the phased array transducers. According to experiment, it is conformed that this system can transmit a large amount of data in real time at high speed; realize phase-controlled focus transmission, and the delay precision reaches 2.5 ns. This study provides a good hardware foundation for underwater imaging systems.

1. Introduction
In recent years, with the gradual reduction of land resources, countries around the world are competing for the development of marine resources, which has led to the rapid development of underwater ultrasound imaging technology. Phased array ultrasonic imaging technology is a new type of underwater acoustic imaging technique. By controlling the array transducer arrays in the phase of emission signal and the received signal delay, the acoustic beam is focused and deflected. By this way the clear images are obtained [1].

The previous underwater ultrasonic detection usually uses a single channel transducer. In this paper, a novel ultrasonic phased array transmission system is designed using ultrasonic phased array detection technology. It uses a 32-element phase-contrast focusing ultrasonic transducer to realize the effect of focusing and deflecting the underwater ultrasonic transmitting beam, and adopts Gigabit Ethernet transmission technology to realize high-speed and real-time transmission of data. It provides technical support for subsequent underwater ultrasound experiments.

2. Theory
2.1. Phased Focus Emission Principle
The array elements of the phased array probe are arranged according to certain shape and size. By means of software electronic technology, the array elements can be controlled to trigger the excitation according to the set delay time, so that different array elements are excited at different times, and the generated ultrasonic coherent wavelet beams with different phases are superimposed in space, the resultant sound beam has the effect of deflecting or focusing. When the phase-controlled focusing transducer is transmitted, the excitation signal delay of each array element of the transducer gradually
increase from the both ends to the middle, and each independent wavefront engenders interference and points to a center of curvature to form a focused beam. The number of array elements of transducer is I, and the geometry of phase-controlled focusing sound beam is shown in Figure 1.

![Figure 1. Phased beam focusing principle](image)

According to Figure 1, the delay time of the ith array element of the transducer to the focus P is calculated as:

$$t_i = \frac{F}{c} \sqrt{1 + \frac{w}{F} \left(1 + \frac{i + 1}{2} \frac{d}{F}\right)^2}$$

Then, the delay difference between the ith array element and the array element with the largest sound path is:

$$\Delta t_i = \max \{t_1, t_2, \ldots, t_i \} - t_i$$

where, $i = 1, 2, \ldots, I$. $F$ is the focal length, $d$ is the center distance between adjacent elements, $w$ is the beam deflection displacement, and $c$ is the speed of sound.

2.2. UDP Communication Protocol

UDP is the English abbreviation of User Datagram Protocol. UDP user datagram protocol is a simple transmission protocol, which is mainly for the transport layer of datagrams. In the process of data transmission, each UDP data to be transmitted will have a corresponding UDP header, and then add the corresponding IP header, so as to form a complete IP datagram to be transmitted. UDP has no overhead such as establishing a connection, revoking a connection, confirming a message, and so on. Compared with TCP protocol, it has faster execution speed, stronger real-time performance, high data transmission efficiency and low load on the system[3]. The UDP datagram format is shown in Figure 2.

![Figure 2. UDP datagram format](image)

3. Ultrasonic Phased Array Transmission System Design

The ultrasonic phased Array Launch System based on Gigabit Ethernet transmission includes PC, power module, Gigabit Ethernet module, FPGA main control unit, high-voltage pulse signal
transmission circuit, and phase-controlled focused ultrasonic transducer. The FPGA is used as the main control unit and signal generation module of the system for generating 32 different delay waveform signals. The waveform signal is amplified by power amplification to excite the phase-controlled focused ultrasonic transducer. The overall block diagram of the system is shown in Figure 3.

3.1. Gigabit Ethernet Communications Design
This paper selects the Intel Cyclone IV series EP4CE30F23C7 chip as the FPGA controller hardware circuit, selects the Realtek company GPHY RTL8211EG Ethernet chip to achieve gigabit Ethernet data communication. The communication protocol adopts Ethernet UDP communication protocol. The FPGA controller communicates with the Gigabit Ethernet PHY chip on the circuit board through the GMII bus. The Gigabit PHY chip sends the data to the PC through the network cable [4]. The hardware connection of the entire system is shown in Figure 4.

According to the UDP communication controller, this paper sends three packets to the FPGA through the host computer system. The first packet is a 4-byte command control word, and the last two packets are instructions sent by the delay parameters of the array to be configured. Each delay parameter matrix takes up 2 bytes, so the configuration parameter matrix takes up a total of 2560 bytes. The 2560-byte delay data is sent in 2 packets, each packet has a data length of 1280 bytes, and each packet is added with a 4-byte data header and a 4-byte data tail, and a total of 1288 bytes are sent to the FPGA.

3.2. FPGA Master Control Module Design
The EP4CE30F23C7 chip of the FPGA main controller in this paper has a total of 484 pins. This model is FBGA package. The chip is highly integrated with 28848 logic units, 343 independent I/Os, four independent phase-locked loops (PLL) and up to 594Kbits of distributed RAM.
According to the focusing algorithm, the delay time of each element of the transducer is calculated, and then the delay parameter and the command control word are transmitted to the FPGA through the Gigabit Ethernet in the format of the packet. The focusing depth control and the automatic deflection Angle control of the transmitted beam of the transducer array are realized by using the abundant I/O pin resources of FPGA and the high-speed counting function.

The accuracy of phased array time delay is the most important parameter of phased array technology, which determines the imaging resolution of the system. The ratio of the phase-shifted delay root mean square (RMS) quantization error to the beam main lobe amplitude is:

\[
S = \left( \frac{1 - \sin(\frac{1}{N})}{N \cdot \sin(\frac{1}{N})} \right)^{\frac{1}{2}} \approx \frac{\pi}{\mu (6N)^{\frac{1}{2}}} \quad (\text{when } \mu \geq 1)
\]

Where, \( \sin(x) = \frac{\sin(\pi x)}{\pi x} \), \( N \) is the number of matrices, \( \mu \) is the ratio of the period corresponding to the center frequency to the minimum delay amount. From equation (3), it can be seen that under the condition that the number of transducer elements is not changed, the accuracy of the phased array time delay can be improved, the sidelobes of the main lobe suppression can be increased, and the imaging resolution can be effectively improved.

This paper uses the digital transmission delay method to realize the phased array transmission delay. Compared with the traditional analog delay line, the realization of the digital transmission delay has the advantages of high accuracy, good tuneability, and high stability. The digital delay can be divided into coarse delay and fine delay. The coarse delay is generally controlled by the sampling clock of the hardware system, and the delay value is an integral multiple of the sampling period. This paper, the 50MHz crystal perk is selected as the sampling clock of the system, and the delay precision is 2.5ns.

In order to reduce the complexity of the system and the number of components, and improve the system integration, this paper uses the basic module phase-locked loop (PLL) of the FPGA to divide, multiply, and shift the equalization technology. Firstly, four times for 50 MHz system clock frequency of 200 MHz signal, then take 200 MHz frequency signal and its reverse signals respectively in 2 frequency, have 4 road frequency is 100 MHz, phase according to the difference of 90° of the clock signal, which is realized the delay precision of 2.5 ns, achieving the target of minimum delay circuit. Verilog HDL language was used to write the simulation program, and Modelsim software was used for simulation, as shown in Figure 5.

3.3. High-Voltage Pulse Signal Transmission Circuit Design
The traditional underwater acoustic emission circuit is bulky and has low working efficiency, which limits the further improvement of the performance of the underwater ultrasonic phased array imaging system [7]. In this paper, aiming at the performance indexes of low power supply voltage, small volume, high frequency and high voltage of the underwater acoustic image system, and based on the requirements of the system's 32-channel ultrasonic phased-controlled transmission, a kind of high
integration transmission circuit using special integrated chip to realize strong ultrasonic signal transmission is proposed.

Since the digital pulse phase difference method is used to generate FPGA digital pulse signals with a delay accuracy of 2.5ns, the output voltage amplitude is only 3.3V(LVTTL), which is far from enough to stimulate the piezoelectric transducer. Therefore, the signal must be amplified in amplitude and power. This paper, the op amp chip uses an application-specific integrated circuit chip Max4940 four-channel high-voltage pulse signal transmitter. Its high voltage output has an output impedance of 8.5Ω, and the active clamp impedance is 21Ω. The high voltage output ensures 2.0A output current. Each channel of each device controls positive and negative pulses through two logic inputs. In this way, the amplitude of the excitation signal after the power amplifier module reaches plus or minus 24V. Part of the power amplifier circuit core design shown in Figure 6.

![Max4940 power amplifier core circuit](image)

**Figure 6.** Max4940 power amplifier core circuit

4. **System test**

In order to verify whether the above system can meet the requirements of phased-array emission, an experimental platform is set up to test and analyze the characteristics of phased-array ultrasonic emission signals and phased-control delay. A 32-channel FPGA ultrasonic phased array launching board is designed. The FPGA acts as the control center of the system, and generates a digital pulse waveform signal with a delay accuracy of 2.5 ns. It is connected with 8 high-voltage pulse transmitting boards, each of which has 4 channels and a total output of 32 channels.

This paper, the design goal is to be able to realize the underwater launch of phased array ultrasonic signal, so the phased focused ultrasound transducer is adopted in the experiment, the array element number 32, and center distance of 4 mm, center frequency of 500 kHz. An obstacle is placed at 80cm directly in front of the transducer array, with a phase-controlled focusing mode and a focal length of 80cm. The transducer transmits ultrasonic waves, which generate echo signals after meeting the target under test, and the hydrophone receives echo signals. The echo signals measured by the oscilloscope are shown in Figure 7.
Set the focal length of the phased focus to 80 cm, the number of emission channels to 32, and calculate the pulse time delay between 32 channels. FPGA configuration is performed according to the calculated delay value, and the 32-channel emission excitation pulse signals having different phase differences are set. The delay parameters set for each channel and the focus delay data of the experimental test are shown in Table 1.

### Table 1. Phased focus delay data

| Number of channels | Theoretical delay (ns) | Actual delay (ns) | Absolute error (ns) |
|--------------------|------------------------|-------------------|---------------------|
| 1/32               | 0                      | 0                 | 0                   |
| 2/31               | 113.8                  | 114.5             | 0.7                 |
| 3/30               | 220.1                  | 220.1             | 0                   |
| 4/29               | 317.6                  | 317.3             | -0.3                |
| 5/28               | 410.0                  | 410.5             | 0.5                 |
| 6/27               | 493.5                  | 493.5             | 0                   |
| 7/26               | 569.4                  | 569.6             | 0.2                 |
| 8/25               | 636.8                  | 636.8             | 0                   |
| 9/24               | 698.6                  | 698.5             | 0.1                 |
| 10/23              | 751.8                  | 751.8             | 0                   |
| 11/22              | 797.4                  | 797.2             | -0.2                |
| 12/21              | 853.4                  | 854.6             | 1.2                 |
| 13/20              | 865.8                  | 865.8             | 0                   |
| 14/19              | 888.6                  | 887.7             | 0.9                 |
| 15/18              | 906.8                  | 906.8             | 0                   |
| 16/17              | 911.5                  | 911.8             | 0.3                 |

Combining the experimental results with the data in Table 1, it can be seen that the error between the relative delay of each channel measured by the 32-channel phased focusing delay emission experiment and the theoretical delay calculated by the focusing algorithm is less than 2 ns, indicating that the system has reached 2.5 ns delay accuracy meets design requirements.

### 5. Conclusion

Compared with the original underwater ultrasonic detection system, this paper presents a multi-channel multi-array ultrasound phased array transmission system, which is realized through the design of FPGA main control module, Gigabit Ethernet communication module and high-voltage pulse transmission circuit. High-speed, real-time data transmission and high-frequency and high-voltage phased-array focused emission of ultrasonic signals. The experimental results show that the system can realize 32-channel phased array emission with phase-control delay accuracy of 2.5 ns, and the transmitted signal is stable, which provides the hardware basis for underwater ultrasound imaging experiments. This paper adopts a modular design, which facilitates large-scale multi-channel expansion and has a strong application value.
6. Acknowledgment
The authors gratefully acknowledge the financial support of The National Key Research and Development Program of China (Project Number: 2018YFC0114902, 2016YFF0201006), Zhejiang province University Student Research and Innovation Program of China (Project number: 2019R409042).

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