LightNorm: Area and Energy-Efficient Batch Normalization Hardware for On-Device DNN Training

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Abstract—When training early-stage deep neural networks (DNNs), generating intermediate features via convolution or linear layers occupied most of the execution time. Accordingly, extensive research has been done to reduce the computational burden of the convolution or linear layers. In recent mobile-friendly DNNs, however, the relative number of operations involved in processing these layers has significantly reduced. As a result, the proportion of the execution time of other layers, such as batch normalization layers, has increased. Thus, in this work, we conduct a detailed analysis of the batch normalization layer to efficiently reduce the runtime overhead in the batch normalization process. Backed up by the thorough analysis, we present an extremely efficient batch normalization, named LightNorm, and its associated hardware module. In more detail, we fuse three approximation techniques that are i) low bit-precision, ii) range batch normalization, and iii) block floating point. All these approximate techniques are carefully utilized not only to maintain the statistics of intermediate feature maps, but also to minimize the off-chip memory accesses. By using the proposed LightNorm hardware, we can achieve significant area and energy savings during the DNN training without hurting the training accuracy. This makes the proposed hardware a great candidate for the on-device training.

I. INTRODUCTION

Recently, deep learning has been applied in many fields of our daily life such as autonomous driving, computer vision and language modeling. Prior to the deployment of deep learning in these applications, training weight parameters of deep neural networks (DNNs) should be preceded. However, training DNNs is a computationally expensive task due to the large amount of weight parameters and thousands of training iterations on large datasets. It requires several days to train the large DNN models even if the training is done on state-of-the-art GPUs or custom NPsUs. For instance, training ResNet-50 takes 29 hours on 8 Tesla P100 GPUs [10] and training BERT requires 16 TPU-v3 chips for 3 days [6]. This prohibits the training at end devices thus the training is mostly done at much powerful cloud servers.

Generally, training DNN models is performed with a IEEE single precision format, i.e., FP32. However, training DNNs with the FP32 format on a large dataset accompanies excessive hardware costs in terms of energy consumption, memory capacity and communication cost. As a remedy for this challenge, reducing bit-width has been actively explored to effectively minimize the hardware cost. For instance, M. Paulius et al. have proposed a mixed-precision training method for the recent GPU to improve the training throughput [19]. With the mixed-precision training, multiplications are performed in FP16 while accumulations are performed in FP32. Unconventional data representations suited at DNN training, such as bfloat16 [11], [17] and block floating point (BFP) representation [7], [22], have been studied as well. To enable DNN training at much lower hardware cost, possibly at the edge, researchers have explored low-precision training using FP8 (i.e., 8-bit floating point) with the support of squeeze and shift operations [3] or exponent biases [8] to cover a wide dynamic range of the original data distribution. However, the prior work only allow low-precision operations on DNN layers, i.e., convolution (Conv) or fully-connected (FC) layers, leaving non-DNN layers including batch normalization to be processed with FP32.

However, as the DNN model evolves over time, the relative execution time of the previously time-consuming Conv/FC layers decreases. For example, early convolutional neural networks (CNNs), such as AlexNet and VGGNet, consume most of the training time (83.9%–95.1%) at Conv or FC layers [16]. Fig. 1 shows the relative execution time between the batch normalization (BN) layers and non-BN layers in three representative CNN benchmarks. Here, Conv/FC layers are included in the non-BN layers. Since the design of recent CNN models focuses on reducing the computational cost of Conv/FC layers, e.g., by reducing the kernel size [10] or introducing a new layer structure [13], [25], the relative execution time of non-BN layers significantly reduces on mobile-friendly CNNs. As shown in Fig. 1, only 39.2% of the total runtime is consumed by the non-BN layers for MobileNetV2 while 60.8% of the runtime is consumed by the BN layers. In other words, for training mobile-friendly CNN models, the runtime overhead of the overlooked BN layers becomes significant. Therefore, to enable on-device DNN training with limited hardware resources, we should explore reducing the complexity of not only the Conv/FC layers, but also the BN layers. Recently, a couple of research works have been presented that try to apply reduced precision on the BN layers, e.g., FP16 [12] or bfloat16 [17]. However, these previous works reduce the bit-width of data to store them in a smaller off-chip memory and to minimize the energy consumption of data accesses, while still limiting the computation to 16-bit multiplications with FP32 additions.

In this paper, we present an extremely compute- and memory-efficient BN process, named LightNorm, by fusing three approximation techniques, which are i) low bit-precision, ii) range batch normalization (RN), and iii) block floating point (BFP). By using
RN, the required dynamic range in representing the intermediate values during the BN process is constrained, which allows lower precision to work well on the BN layers. In addition, converting to a BFP representation prior to storing feature maps to DRAM helps minimize the communication cost incurred by expensive DRAM accesses. Then, we present a customized hardware for LightNorm which realizes area and energy-efficient BN hardware for on-device DNN training. By taking benefits of all these approaches, we were able to design an extremely lightweight BN hardware, which takes up 16.2x smaller area and consumes 15.4x lower power compared to the previous BN hardware designs.

The main contributions of our work are as follows:

1) **Hardware-friendly BN:** We explored the possible combinations of approximation techniques to design a low-complexity BN layer, named LightNorm, possibly realizing on-device training for recent mobile-friendly DNN models. We first utilize range batch normalization to push the quantization level down to FP10. Then, to further reduce the energy consumption, we group tensors so that exponents are shared.

2) **Hardware Implementation:** We designed LightNorm hardware and compared its efficiency to other BN methods. Moreover, we designed a training accelerator equipped with the LightNorm hardware to evaluate the system-level energy efficiency. Compared to training accelerators with different precision levels and BN types, the area reduces by 1.2~4.1x and the energy consumption decreases by 1.3~5.0x.

## II. BACKGROUNDS

### A. Batch Normalization

A batch normalization (BN) is an essential process in deep learning to adjust input distribution to allow faster convergence and improved training accuracy. The concept of the BN was first introduced in [14] to address the problem of internal covariate shift. For a mini-batch of input tensor per channel, i.e., \( X^{(c)} \in \mathbb{R}^{B \times H \times W} \), the BN is done by

\[
y_i = \gamma \cdot \frac{x_i - \mu}{\sqrt{\text{var}[X^{(c)}] + \epsilon}} + \beta, \tag{1}
\]

where \( c \) is the channel index, \( x_i \) is the \( i \)th element in \( X^{(c)} \), \( B \) is the mini-batch size, \( H \) and \( W \) are the height and width of a feature map, respectively, \( \mu \) is the expectation over \( X^{(c)} \), \( \text{var}[X^{(c)}] \) is the variance of \( X^{(c)} \), and \( \epsilon \) is the value to prevent the denominator from being zero. The \( \gamma \) and \( \beta \) are trainable parameters for each channel ‘\( c \)’ that improve the training accuracy. Due to the importance of the BN process for training a better DNN model, it is a common design strategy to add BN layers in the DNN model [2], [4], [26].

However, the computation of a conventional BN process in Eq. (1) requires complex arithmetic functions, i.e., square root and division, that incur considerable hardware overhead when designing a DNN accelerator [1]. To reduce the complexity of realizing the conventional BN computations, a range batch normalization (RN) has been proposed [1]. The main idea of the RN is to replace the denominator term in Eq. (1) to a range of input distribution. The RN is performed by

\[
\hat{y}_i = \gamma \cdot \frac{x_i - \mu}{C(B) \cdot \text{range}(x_i - \mu)} + \beta, \tag{2}
\]

where \( C(B) = 1/\sqrt{2 - \ln(B)} \) (e.g., 0.32 for \( B = 128 \)), \( \mu \) is the expectation over \( X^{(c)} \), and \( \text{range}(x) = \max(x) - \min(x) \). The constant \( C(B) \) is the key to the RN as it helps accurately approximate the standard deviation of \( X^{(c)} \). As feature maps in a DNN model are originated from a sum of many inputs, \( X^{(c)} \) naturally follows the Gaussian distribution [28]. Thus, the range of the input \( X^{(c)} \) is highly correlated with the standard deviation magnitude.

### B. Block Floating Point

A floating point number, which is generally used in the DNN training, is represented as

\[
x_i = (-1)^{s_i} \cdot (1.m_i) \cdot 2^{e_i},
\]

where \( s_i \) is the sign, \( m_i \) is the mantissa, and \( e_i \) is the exponent of the number \( x_i \). Block floating point (BFP) is a special form of representing a set of floating point numbers. In the BFP representation, multiple floating point numbers form a block, say \( \vec{x} = [x_1, x_2, ..., x_N] \), that will share an exponent value \( e_s \). Note that the shared exponent is obtained by \( e_s = \lceil \log_2(\max(|x_1|, ..., |x_N|)) \rceil \). Then, we shift the mantissa of all numbers in the block to the right by \( (e_s - e_i) \). As a result, we get a new block of floating point numbers that is

\[
\vec{x}_{\text{BFP}} = [x_1, x_2, ..., x_N] \cdot 2^{e_s} \approx [x_1, x_2, ..., x_N],
\]

where \( \vec{x} \) is the aligned number represented by only ‘sign + mantissa’.

The main advantage of BFP representation is that it becomes possible to perform a inner product between two floating point vectors with fixed-point arithmetic units [7]. Another important benefit of utilizing the BFP representation is reducing required memory footprint for storing tensors (thanks to the exponent sharing). In this work, we focus on the BN, which requires a considerable memory access [16], thus the purpose of utilizing the BFP format is to minimize the access energy of feature maps during the BN process by reducing the memory footprint.

## III. MOTIVATION

### A. Compute Units for BN Layers

The prior work on designing an energy-efficient DNN accelerator mostly focuses on Conv/FC operations [22], [23], [30], [32], while there is lack of research on making the BN hardware more efficient. One of the most effective ways of improving hardware efficiency of a processing unit is reducing the bit-precision. In this work, we extensively study the impact of reduced precision on computations involved in the BN layer. Prior to analyzing the impact of low-precision BN processing on DNN training accuracy, we performed a detailed analysis on compute units involved in the BN computation. There are four main compute units for the BN layer processing: i) adders, ii) multipliers, iii) dividers, and iv) square root units. We synthesized these compute units in a 45nm CMOS technology using DesignWare IPs supported by Synopsys [29]. Four different FP precisions were tested, i.e., FP32, FP16, bfloat16 and FP10. Since training DNNs with BN layers computed in FP8 failed, as discussed in Section IV, we report the hardware costs of compute units using FP10 as a lower bound. Two variants of FP10 are tested since forward and backward passes require different bit configurations to ensure training stability (refer to Section IV-B). One is FP10-A [1,5,4] and another is FP10-B [1,6,3]1. For the fair comparison, the synthesized clock frequency is set to that of FP32 for area and power reports (Fig. 2(a-b)). As a reference, we also report the maximum clock frequency that each compute unit for a given FP precision can operate at (Fig. 2(c)). As expected, the lower the FP precision, the lower the occupied area and power consumption. For instance, we can reduce the area and power consumption by 74.9% and 75.2% on average by using FP10 compared to FP32. By having more exponent bits

1The data format is represented by \{sign bit, exponent bits, mantissa bits\} throughout this paper.
and less mantissa bits in bfloat16, we can reduce the area and power consumption by 4.8% and 25.5% on average compared to FP16. This is because handling mantissa bits is more complex in floating point arithmetic [15].

B. Memory Requirement of BN Layers

When training CNNs, feature maps generated at each layer in forward pass are used during backward pass when computing gradients [16]. Thus, the feature maps generated in the forward pass need to be stored in DRAM for the later use. Fig. 3 shows a required memory footprint among the tested CNN models. This is because MobileNetV1 has the smallest number of layers and reduces the number of computations by using depthwise-separable convolutions. On the contrary, ResNet-50 requires the largest memory footprint. It requires 2.0× and 1.8× more memory capacity than MobileNetV2 and DenseNet-121. Since the training is an iterative process, accessing several or tens of GBs of data per epoch will consume significant amount of energy. Thus, minimizing the data travels from the processing core to DRAM is also an important thing to consider when dealing with BN layers.

IV. LIGHTNORM: LOW-PRECISION BLOCKED RANGE NORM

A. Low-Precision Batch Normalization

To perform BN, we first need to do a channel-wise feature map accumulation for a given mini-batch to compute μ in Eq. (1) or (2). Prior work on training DNNs perform BN with single precision (FP32) in order to extract the statistics of feature maps as accurate as possible to ensure the training convergence [3], [7], [8], [11], [17], [19]. In this section, we analyze the impact of the reduced precision on forward and backward passes at the BN layers to independently set the minimum bit-precision for each pass.

1) Floating Point Formats: In floating point representations, there are three bit components: a sign bit (s), mantissa bits (m) and exponent bits (e). Here, the length of mantissa bits determines the precision, and that of exponent bits determines the dynamic range. Table I summarizes the dynamic range and representable value range of various floating point formats, i.e., FP32, bfloat16, FP16, FP10 and FP8. The FP32 is the most precise representation with the widest dynamic range among the four. The bfloat16 is particularly designed for training DNNs with a wider dynamic range compared to FP16, while sacrificing the precision. Notably, the precision is less important than the dynamic range when considering the DNN training [9], [11]. The FP10-A and FP8 provide the same dynamic range with FP16, but with a significantly less precision (merely 4-bit and 2-bit is used as mantissa bits). With the use FP10-B, we slightly compromise precision for better dynamic range compared to FP10-A. As seen from Fig. 2, using FP10 results in the most efficient hardware implementation. Thus, our goal is to make full use of FP10 arithmetic units for BN processing to design an efficient DNN training accelerator without training accuracy loss.

2) Proper Length of Exponent Bits: The dynamic range has an important role in training accuracy. This is because values outside the representable range become zero. According to [19], the omitted values due to the limited dynamic range results in significant training accuracy drop. Therefore, we observed data distribution of both forward pass (i.e., activations) and backward pass (i.e., gradients) at BN layers in order to select a proper exponent bits for BN processing. Fig. 4 shows the dynamic range of feature maps (activations) and gradients at BN layers of ResNet-50 trained on CIFAR-100 dataset. The activations have a dynamic range of [\(-2.55, 4.31\)], which is safely covered by 5-bit exponent bits (i.e., FP16, FP10-A and FP8). However, gradients have a dynamic range of [\(-16.25, -8.97\)] which can be covered by 6-bit or higher exponent bits (i.e., FP32, bfloat16 and FP10-B). According to this data-driven analysis, we decided to select 6-bit or higher exponent bits for BN processing.

3) Proper Length of Mantissa Bits: Accumulation is a crucial operation to compute layer statistics (e.g., computing μ and Var[X^{(c)}]) in Eq. (1)). When performing a floating point addition, the maximum exponent among two numbers is extracted first, then a mantissa of...
TABLE II: Mean and standard deviation values of normalized feature maps at the 3rd layer of ResNet-50 at various training epochs with CIFAR-100. The precision of the BN layer for forward pass is only changed while bit widths of all other computations are kept at FP32.

| Epoch | FP32 / bfloat16 | FP16 / FP10-A / FP8 | FP16 / FP10-A / FP8 |
|-------|-----------------|---------------------|---------------------|
| Mean  | 3.958 E-08      | 1.263 E-09          | -2.462 E-06         |
| Stdev | 1.0000          | 1.0000              | 1.0000              |

| Epoch | FP32 / bfloat16 | FP16 / FP10-A / FP8 | FP16 / FP10-A / FP8 |
|-------|-----------------|---------------------|---------------------|
| Mean  | 1.195 E-09      | 1.263 E-09          | -2.462 E-06         |
| Stdev | 1.0000          | 1.0000              | 1.0000              |

| Epoch | FP32 / bfloat16 | FP16 / FP10-A / FP8 | FP16 / FP10-A / FP8 |
|-------|-----------------|---------------------|---------------------|
| Mean  | 1.263 E-09      | 1.263 E-09          | -2.462 E-06         |
| Stdev | 1.0000          | 1.0000              | 1.0000              |

B. Blocked Range Normalization

In addition to the reduced precision in the BN layers, we applied two more approximation techniques that mainly focus on reducing the number of DRAM accesses for higher energy-efficiency.

1) Utilizing Range Normalization: The range normalization (RN) presented in [1] has two important advantages which are essential to achieve lightweight BN layers. First, RN has a fewer number of operations to get layer statistics and significantly less DRAM accesses. Fig. 6 shows the computational flow to get statistics, i.e., and . The mean and standard deviation of normalized feature maps at various training epochs and data formats are analyzed in Table II. To look at the sole impact of the FP precision on BN layers during the forward pass, we kept all other computations at FP32. Due to extremely short mantissa bits in FP8, i.e., 2-bit, the normalized distribution is distorted deviating from zero-mean and unit-variance. By allowing two additional bits for mantissa, i.e., FP10-A, the computation errors of estimating and become much smaller than FP8.

4) Principle Behind Selection of BN Precision for DNN Training: Based on the analysis so far, we can conjecture that the length of mantissa bits is critical for the forward (FW) pass and that of exponent bits is more critical for the backward (BW) pass at BN layers. To verify this statement, we conducted a set of experiments on ResNet-50 with CIFAR-100 dataset. We selected different FP precisions for forward and backward passes to check the sensitivity of the length of mantissa bits or exponent bits at each pass on training accuracy. The training curves at various FP combinations are provided in Fig. 5. The baseline is using FP32 for both forward and backward passes. When using FP16 or bfloat16 for both forward and backward passes, the training accuracy degrades by ~2.5%. Instead, we used FP16 for the forward pass and bfloat16 for the backward pass based on our analysis. As a result, it was possible to reach similar training accuracy to the FP32 baseline. However, if we move from FP16 to FP8 for the forward pass while keeping bfloat16 for the backward pass, the training accuracy significantly degrades by 7.9% due to the insufficient mantissa bits. In this set of experiments, we used the conventional BN layers.

The number with a smaller exponent is shifted to the right by the shift amount, the smaller number becomes zero. This phenomenon is referred to as zero setting error (ZSE). Therefore, insufficient mantissa bits will cause errors when computing is referred to as zero setting error (ZSE). Therefore, insufficient mantissa bits. In this set of experiments, we used the conventional BN layers.

Fig. 4: Dynamic range of feature maps and gradients in BN layers. It is extracted by training ResNet-50 on CIFAR-100 over 160 epochs.

Fig. 5: Training results of various data formats on ResNet-50 with CIFAR-100 dataset.

TABLE III: Test accuracy when MobileNets are trained with four different combinations of FP10 formats on CIFAR-100 dataset using range normalization (RN) instead of the conventional BN.

| Data Format (FW / BW) | MobileNetV1 | MobileNetV2 |
|-----------------------|-------------|-------------|
| FP32 / FP32 (with BN; not RN) | 66.21% | 65.38% |
| FP16 / [1, 6, 3] / FP10-A / [1, 6, 3] | 75.68% | 72.53% |
| FP16 / [1, 6, 3] / FP10-A / [1, 6, 3] | 67.72% | 65.73% |
| FP10-B / [1, 6, 3] / FP10-A / [1, 6, 3] | 74.00% | 62.50% |
| FP32 / bfloat16 / [1, 6, 3] / FP10-A / [1, 6, 3] | 66.71% | 63.99% |
four CNN benchmarks, i.e., ResNet-50, MobileNetV1, MobileNetV2 and DenseNet-121, trained on CIFAR-100 dataset [18]. All training hyperparameters are kept the same as training the networks in FP32. Table IV summarizes the test accuracy of CNN benchmarks using LightNorm trained with various group sizes. We tested the group size of 4, 8 or 16 to group feature maps or gradients during the FW and BW passes. As shown in Table IV, allowing group size of 8 or larger results in a large amount of ZSEs significantly degrading the training accuracy. With the group size of four the test accuracy is similar to the FP32 baseline. The test accuracy only drops by 0.5% on average. Therefore, for the design of LightNorm hardware in the following section, we use BFP10 (FW: \{1,5,4\}, BW: \{1,6,3\}) as the BN precision using blocked range BN with the group size of 4.

V. DNN Accelerator with LightNorm

A. LightNorm Hardware

To support the end-to-end training, DNN training accelerators should be equipped with BN hardware. Fig. 8 shows the overall architecture of LightNorm hardware. It consists of one forward (FW) pass module and backward (BW) pass module to support hardware-accelerated training of BN layers, which processes 32 channels in parallel (directly connected to columns of a systolic array). Note that the systolic array is typically used at accelerating general matrix multiply (GEMM) operations [9]. In addition, LightNorm hardware has a control unit, a scalar unit and a lookup table (LUT). The scalar unit calculates \( \sigma = 1/\sqrt{2 \cdot \ln(B)} \) and \( (\sigma)^{-3/2} \cdot \gamma(C(B)) \) that are required in the backward pass of LightNorm. The LUT stores a pre-computed \( C(B) = 1/\sqrt{2 \cdot \ln(B)} \) for various \( B \) values, where \( B \) is the mini-batch size. In our design, it stores \( C(B) \) values when \( B = 16, 32, 64, 128, 256 \) and 1024. Note that LightNorm follows the RN computation given by Eq. (2) and channel-wise normalization is performed for a given mini-batch.

1) Forward Pass Module (LightNorm - FW): The forward pass module is dedicated to a forward pass of the LightNorm layer, which uses ‘FP10-A’ format. It has 32 FW blocks for parallel execution of BN for 32 output channels. The outputs from the training accelerator, i.e., a 32×32 systolic array in this paper, are streamed into 32 FW blocks. Each FW block has two forward pass units that are FWU0 and FWU1 (Fig. 9). The streamed \( x_i \)’s in FWU0 are accumulated by FP10-A adder to compute \( \mu \) of a particular output channel. At the same time, Max and Min units extract the maximum and minimum values of \( x_i \) for \( \sigma = C(B) \cdot (x_{\max} - x_{\min}) \) computation. Then,

![Fig. 8: Overall architecture of LightNorm hardware.](image-url)
computed $\mu$ and $\sigma$ are passed to FWU1 for the actual normalization on $x_i$. These two units are pipelined, which means that FWU0 takes inputs every clock cycle and FWU1 normalizes the feature map by using the pre-computed $\mu$ and $\sigma$.

2) Backward Pass Module (LightNorm - BW): The backward pass module backpropagates local gradients through the LightNorm layer, which uses ‘FP10-B’ format. Similar to the FW module, it consists of 32 BW blocks where each block consists of two backward pass units that are BWU0 and BWU1 (Fig. 10). The BWU0 computes the local gradient ($\partial L/\partial x_i$) through the denominator of Eq. (2), which can be defined as

$$\left(\frac{\partial L}{\partial x_i}\right)_1 = -\frac{\gamma}{\sigma + \epsilon} \cdot \left(\frac{1}{N} \cdot \sum_{i=1}^{N} \frac{\partial L}{\partial y_i} + \frac{\partial L}{\partial y_i}\right),$$

where $\partial L/\partial y_i$ is the gradient at the output of a LightNorm layer, $N$ is the number of elements in local gradients per channel, and $\gamma$ is the coefficient of the BN layer, $\sigma$ is the standard deviation, and $\epsilon$ is used to ensure stability. Another local gradient ($\partial L/\partial x_i$) through the numerator of Eq. (2), i.e., $\text{range}(x_i - \mu)$ function, can be obtained by

$$\left(\frac{\partial L}{\partial x_i}\right)_2 = \frac{\gamma \cdot C(B)}{2} \cdot (\sigma)^{-3/2} \cdot \left(\sum_{i=1}^{N} \frac{\partial L}{\partial y_i} \cdot (x_i - \mu)\right).$$

If $x_i = m_{min}$, the final local gradient at input ($x_i$) of the LightNorm layer is computed by ($\partial L/\partial x_i$)$_1 + (\partial L/\partial x_i)$$_2$. If $x_i = m_{max}$, the final local gradient at $x_i$ is computed by ($\partial L/\partial x_i$)$_1 - (\partial L/\partial x_i)$$_2$. Otherwise, the local gradient at $x_i$ simply equals to ($\partial L/\partial x_i$)$_1$. Since BWU1 computes Eq. (6), we need to selectively provide a positive or negative value of ($\partial L/\partial x_i$)$_2$. This is controlled by the multiplexer placed inside the BWU1 unit.

\[\text{TABLE V: Area and power breakdowns of LightNorm hardware.}\]

| Module          | Area [\mu m^2] | Power [\mu W] |
|-----------------|----------------|---------------|
| LightNorm - FW  | 6996.68 (74.82\%) | 1.184 (53.32\%) |
| LightNorm - BW  | 7015.31 (75.01\%) | 1.200 (53.59\%) |
| Scalar Unit     | 901 (14.19\%)  | 0.0515 (2.28\%) |
| Others          | 327.16 (0.55\%) | 0.0056 (0.15\%) |
| Total           | 8938.53 (100.00\%) | 1.2411 (100.00\%) |

B. Evaluation of LightNorm Hardware

1) Methodology and Baselines: In order to evaluate energy efficiency of LightNorm hardware, we implemented RTL and synthesized it at 150MHz with Synopsys Design Compiler using 45nm open cell library [27]. To compare LightNorm with other baselines, we designed BN hardware for the conventional BN [14] and restructured BN [16] with FP32 compute units. Then, they are synthesized at the same clock frequency using the same technology node. In the conventional BN, variance of a tensor $X$ is computed by

$$\text{Var}[X] = E[X^2] - E[X]^2,$$

where $X$ is the mini-batch of input tensor per channel. In the conventional BN, the variance can be calculated only after computing the mean $E[X]$. This temporal dependency results in two DRAM accesses for fetching the entire $X$’s for a given mini-batch size (bandwidth-limited). To reduce the overhead of excessive DRAM accesses, the restructured BN calculates the variance in a different manner, which is

$$\text{Var}[X] = E[X^2] - E[X]^2.$$

By simple restructuring of Eq. (7) to (8), the restructured BN computes the mean and variance in parallel. This effectively reduces the number of DRAM accesses by half. Meanwhile, local gradients at the conventional and restructured BN layers are calculated by the same equation [16], which is

$$\frac{\partial L}{\partial x_i} = \frac{\gamma}{\sqrt{\sigma^2 + \epsilon}} \cdot \left(\frac{1}{N} \cdot \sum_{i=1}^{N} \frac{\partial L}{\partial y_i} - \frac{1}{N} \cdot \frac{\partial L}{\partial y_i} \cdot \frac{\partial y_i}{\partial x_i} \cdot (x_i - \mu)\right),$$

where $\frac{\partial L}{\partial y_i}$ is the derivative of the local mean $\mu$ with respect to $x_i$, and $\frac{\partial y_i}{\partial x_i}$ is the derivative of the local variance $\sigma$ with respect to $x_i$. For the performance comparison, a cycle-approximate simulator was designed, which outputs the estimated clock cycles for three BN hardware modules (i.e., LightNorm and two baselines). The hardware evaluation was performed on four benchmarks, i.e., ResNet-50, MobileNetV1, MobileNetV2 and DenseNet-121, using CIFAR-100 dataset.

2) Area and Power Consumption: Table V shows area and power breakdowns of the LightNorm hardware. It reports the area and power consumption of all modules which are shown in Fig. 8. For the LUT and control unit, the area and power consumption are reported together as ‘Others’. In total, LightNorm hardware occupies about 0.09mm$^2$ of area and consumes 4.01mW of power. The areas of the (conventional) BN and restructured BN are 1.44mm$^2$ and 1.54mm$^2$, respectively. The power consumptions of the BN and restructured BN are 59.61mW and 63.53mW, respectively. For the precision independent comparison, we also designed the LightNorm hardware with FP32 compute units. Then, it occupies 0.99mm$^2$ of area and consumes 37.04mW of power. Thus, 1.5x smaller area and 1.7x lower power consumption on average are used by LightNorm hardware even with the same precision (FP32), thanks to the use of range BN. With the use of FP10-A for the forward pass and FP10-B for the backward pass, LightNorm takes up 16.2x smaller area and consumes 15.4x lower power on average. This benefit comes from the fused approximation schemes, i.e., reduced precision, range BN, and exponent sharing, presented in Section IV.
Restructured BN consumes lower energy than the conventional BN and restructured BN, $\mu_{FW}$, $\mu_{BW}$, and $\sigma_{FW}$ and $\sigma_{BW}$ in parallel, while the BN consumes lower energy in average compared to conventional BN for the FW and BW passes. Thanks to these approximation techniques, operations in the both FW and BW passes are simplified. This is obvious by comparing Eq. (5) to Eq. (9).

C. Training Accelerator with LightNorm

1) Methodology: To look at practical effectiveness of LightNorm, we designed a training accelerator that consists of data buffers, a $32 \times 32$ systolic array, and LightNorm hardware with BFP converters (Fig. 12). To perform a system-level analysis on the training accelerator, we also considered DRAM and SRAM accesses when estimating the performance and energy consumption. For as DRAM, 16Gb LPDDR3 was assumed and its associated timing specifications are used [20]. For the power and timing analysis of SRAM blocks, we used CACTI-6.0 [21]. The sizes of on-chip buffers are selected differently depending on the precision levels used by various training accelerators as summarized in Table VI. When deciding the on-chip buffer size, we also considered hiding the DRAM access latency to keep the systolic array busy as much as possible. To estimate the clock cycle consumed by the systolic array, we modified an open-source cycle-level simulator, i.e., Scale-Sim [24], to consider our SRAM and DRAM configurations. The number of clock cycles consumed by the LightNorm hardware is measured by the RTL simulation by assuming ImageNet-scale images [5] as inputs to the network for a more realistic analysis. The RTLs of all hardware configurations for the evaluation are synthesized at 150MHz with Synopsys Design Compiler using 45nm CMOS technology.

2) Hardware Configurations: Fig. 12 shows the overall architecture of a training accelerator equipped with LightNorm hardware. For the comparison, there are various hardware configurations that can affect the area and power consumption of the training accelerator. One configurable parameter is the bit-precision of the systolic array (SA). The systolic array processes Conv/FC layers and it has $32 \times 32$ multiply-accumulate (MAC) units. The precision for the multiplier at each MAC unit can be changed, i.e., FP32 for the high-performance training accelerators [14], [19] and FP8 for the energy-efficient training accelerators [30], [31]. Not to lose the training accuracy, we use the FP32 adder at each MAC unit for all hardware configurations. Another configurable parameter is the type of BN layer and its precision level (e.g., BFP10 for LightNorm). In Table VI, HW1~3 are high-performance training accelerators with different types of BN layers using FP32. HW4~6 are energy-efficient training accelerators with different BN modules using bfloat16, which is based on the recent studies possibly enabling on-device training [3], [17], [31]. There are three different BN types compared in this work, i.e., conventional BN [14], restructured BN [16], and range BN [1]. The BFP converter in Fig. 12 becomes simply a quantization unit for HW4~6 changing FP32 outputs to bfloat16 values for more efficient BN processing. HW7 is the proposed training accelerator using low-precision systolic array with LightNorm hardware. Note that BFP10 is used at the BN layers in LightNorm and BFP converters are used to quantize outputs to FP10 and store them in a more memory-efficient way, i.e., BFP10, as presented in Section IV.

3) Area Analysis: As expected, high-performance training accelerators, i.e., HW1~3, which use FP32 MAC units and FP32 BN modules occupy larger area (Fig. 13(a)). For instance, HW1 takes up $3.2 \times$ larger area than HW4 even though both use the same BN type. Despite of the identical precision level in HW1~3, different BN types lead to different chip areas. For example, HW3 using RN occupies 10.4% smaller area than HW2 using restructured BN. Since HW4~6 use lower precision in both SA and BN modules, they occupy 68.6% smaller area on average than the high-performance training accelerators (HW1~3). Note that the area of the BN module slightly reduces, this is because all adders in the BN hardware are still performed with FP32 as in [17]. The proposed training accelerator (HW7) occupies the smallest area thanks to the use of low-precision SA and LightNorm hardware. The area saving in the BN hardware comes from the reduced precision and more hardware-friendly RN computations. It occupies $4.0 \times$ and $1.2 \times$ smaller areas on average than HW1~HW3 and HW4~HW6, respectively.
### TABLE VI: Various hardware design configurations of a DNN training accelerator for the area and energy analysis.

| Hardware Configurations | HW1 | HW2 | HW3 | HW4 | HW5 | HW6 | HW7 (Proposed) |
|-------------------------|-----|-----|-----|-----|-----|-----|---------------|
| Precision in SA (Mul. / Add.) | FP32 / FP32 | FP32 / FP32 | FP32 / FP32 | FP32 / FP32 | FP32 / FP32 | FP32 / FP32 | FP32 / FP32 |
| Batch Norm Type | Conv. BN | Restructured Norm | Range Norm (BN) | Conv. BN | Restructured Norm | Range Norm (BN) | LightNorm |
| Memory size (I/W/O) | 128 / 128 / 64 | 128 / 128 / 64 | 128 / 128 / 64 | 32 / 32 / 32 | 32 / 32 / 32 | 32 / 32 / 32 |

**Fig. 13:** (a) Area and (b) energy breakdowns of various DNN training accelerators. High-performance training accelerators (HW1–3), energy-efficient training accelerators (HW4–6), and the proposed training accelerator are compared.

### 4) Energy Analysis: The analysis on energy consumption of each training accelerator is performed on one training epoch. Among HW1–3, a RN-based accelerator (HW3) shows the best energy-efficiency (11.6% better than HW1). HW4–6 show 3.4× lower energy consumption on average than HW1–3. This reduction is mainly due to i) low-precision multipliers in both SA and BN, and ii) reduction in the data access energy. The proposed accelerator (HW7) shows the minimum energy consumption, i.e., 1.3–5.0× lower energy than other accelerators. Compared to HW1–3 and HW4–6, HW7 saves the energy by 78.8% and 28.6%, respectively. This is due to the proposed LightNorm as BN processing, which minimizes both BN processing energy and memory access energy.

### VI. Conclusion

In recent DNNs, the relative importance in the execution time and energy consumption of the batch normalization (BN) process has been significantly increased. In this paper, therefore, we presented an extremely memory- and energy-efficient BN process, named LightNorm. To achieve this goal, we fused three approximation techniques, which are i) low bit-precision, ii) range batch normalization, and iii) block floating point. These techniques are carefully selected that help reducing the complexity of BN layers and improving its hardware efficiency without sacrificing the DNN training accuracy. To demonstrate the hardware efficiency, we designed a customized LightNorm hardware and compared with the other conventional BN hardware designs. Finally, we extended the hardware evaluation by integrating the LightNorm hardware to a real DNN training accelerator. In conclusion, LightNorm has improved the energy-efficiency by 1.3–5.0× compared to various configurations of DNN training accelerators.

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