Abstract—Virtual oscillator (VO) control is the latest and promising control technique for grid-forming inverters. VO controllers (VOCs) can simultaneously provide time-domain synchronization and steady-state droop functionalities. In recent developments, VOCs have been integrated into system-level control architecture to provide additional functionalities such as capacitor voltage regulation and overcurrent protection. This article has further refined the existing VO-based system-level grid-forming control architecture with two essential and specific research contributions. The first contribution is to improve the decoupling in control over individual phases, which is achieved by combining symmetrical-component-based VOC with nested voltage and current controls. The proposed phase decoupling control feature improves the grid-forming performance of existing VOCs in the presence of unbalanced grid voltages. The second contribution is to improve the fault ride-through performance under unbalanced faults by modifying the feedback of the existing VO. Systematic development of the proposed grid-forming control architecture with analytical reasoning is presented. The proposed controller is successfully validated using simulations and experiments.

Index Terms—Fault ride-through, grid forming (GFM), symmetrical component, unbalanced grid condition, virtual oscillator (VO).

I. INTRODUCTION

VIRTUAL oscillator (VO)-based grid forming (GFM) control strategy has gone through several major developments in recent years. The concept of decentralized communication-free control of inverters using nonlinear limit cycle oscillators was first proposed in [1], [2], [3]. It is followed by crucial component-level development and analysis. VO control provides all the steady-state functionalities of conventional droop control [4], [5]. At the same time, because of the time-domain implementation, the dynamic performance of VO control is better than conventional droop control [6], [7], [8]. Different oscillator models such as dead zone, Van-der-pol, Andronov-Hopf, and Dispatchable VO (d-VOC) are introduced in [5], [9], [10], [11], [12], [13]. Dead-zone and Van-der-Pol oscillators are unsuitable for three-phase operations because they cannot incorporate more than one input as feedback [14]. Dead-zone and Van-der-Pol oscillators are also unable to provide decoupled control over real and reactive power without additional control loops [5]. Van-der-Pol oscillators can achieve faster dynamics only at the expense of higher harmonic content at the output voltage [10]. A modification in the nonlinear current source of the Van-der-Pol oscillator is proposed in [11] to reduce the third harmonic component from the output voltage. Andronov–Hopf oscillator model has overcome the abovementioned limitations of dead-zone and Van-der-Pol oscillators [5]. A d-VOC and an Andronov–Hopf oscillator have a similar fundamental form [5].

The component-level development is followed by the system-level implementation of VO-based controllers (VOCs). VOC with additional control loops is used for grid-connected operation in [15] and [16]. A single VO is used for islanded and grid-connected operations of inverters with seamless transition using hierarchical and unified control structures in [17] and [18], respectively. The virtual impedance technique is integrated into VOC for selective harmonic current rejection and overcurrent protection in [19] and [20].

The system-level control architecture of VO-based grid-forming controllers can be divided into two broad categories. In the first category, as shown in Fig. 1(a), a VO generates the reference voltage for the inverter. The VO provides time-domain synchronization with the connected electrical network and droop functionalities. The cascaded control loops meet different objectives, such as limiting harmonic components from the output currents and overcurrent protection [19], [20]. The second category is more recent and advanced. In the second category, as shown in Fig. 1(b), a VOC is accompanied by nested
The trol to achieve active participation in mitigating grid voltage
unbalances. A voltage unbalance compensation method for droop control is presented in [31]. The negative sequence reactive power is fed to the compensator as the input through a lowpass filter with a corner frequency of 1.25 rad/s. The output voltage of the compensator is then added to the reference voltage generated by the droop controller. The lowpass filter acts as a major bottleneck to the overall control responsiveness. In [32], a centralized controller is used to collaborate among the grid-forming inverters of an ac microgrid for voltage unbalance compensation. The requirement of the communication link reduces the overall reliability of the proposed control architecture. Negative sequence voltage control techniques for virtual synchronous machine control are reported in [33] and [34] to mitigate the voltage unbalances of the connected electrical network. However, the proposed control technique suffers severely from active and reactive power oscillations. It is also crucial to mention that the implementation technique and inner working of the VO control are entirely different from the other two grid-forming control strategies, i.e., the droop control and the virtual synchronous machine control. As a result, although the final objectives are similar, the methods proposed in [31], [33], and [34] are not directly compatible with VOCs.

2) Riding through unbalanced low voltage faults: The fault ride-through requirements are becoming stricter for distributed renewable energy sources in recent grid codes [35]. GFM inverters must stay connected with the electrical network and inject reactive power to the network under balanced and unbalanced faults [35], [36]. Therefore, the performance under an unbalanced fault is vital for any grid-forming control strategy [37], [38]. During any unbalanced fault, the controller is expected to limit the output current and inject reactive power at the faulty phases [39], [40]. At the same time, the control over the healthy phases should be affected as minimum as possible [39], [40]. The existing VO-based grid-forming controllers, as presented in [21], [22], face great difficulty riding through unbalanced faults. The control over a healthy phase is severely affected by the feedback current from a faulty phase. The reason behind the mentioned issue faced by the existing VOC is as follows.

Any grid-forming controller must enter into the current control mode during a fault condition to limit the output currents [41], [42], [43]. However, for a VOC, only limiting the current output is not sufficient. Unlike droop control or virtual
synchronous machine control, the VO control technique uses the instantaneous output currents of the inverter explicitly for asymptotic synchronization with the connected electrical network. During an unbalanced fault, the time-domain implementation of the VO control technique becomes a disadvantage rather than an advantage. The current feedback from a faulty phase affects the overall effective synchronization of the controller and leaves adverse effects on the operation of a healthy phase.

The rest of the article is organized as follows. The overview of the explicit research contributions offered by this article is presented in Section II. Section III introduces the S-VOC-based system-level control architecture for grid-forming inverters. In Section IV, the performance of the proposed control strategy is evaluated using simulation results. Experimental results are presented in Section V to validate the proposed controller. Finally, the article is concluded in Section VI with a brief overview of how the present research work will be extended in the future.

II. OVERVIEW OF THE RESEARCH CONTRIBUTIONS

The explicit research contributions of this article are summarized as follows.

1) The main focus of the research work presented in this article is to improve further the existing VO-based system-level grid-forming control architecture, which is introduced in [21] and [22].

2) The concept of S-VOC from our previous work, [23], and the nested control loop architecture for VO-based grid-forming inverter from [21] and [22] are combined. As a result, the proposed controller has better decoupling in control over individual phases. At the same time, the proposed controller can meet the system-level requirements such as capacitor voltage regulation and overcurrent protection.

3) The ability of decoupled control over individual phases helps the proposed controller to achieve improved grid-forming performance over the existing VO Cs [21], [22] in the presence of unbalanced grid voltages.

4) This article has introduced a modification in the feedback of the existing VOC. The proposed feedback estimator is activated only during an unbalanced fault. It helps the proposed controller to retain effective synchronization with the connected electrical network under an unbalanced fault condition without requiring a PLL. As a result, the performance of a healthy phase gets affected to a lesser extent during an unbalanced fault.

5) The proposed controller has achieved the above improvements over the existing controllers without requiring any extra sensor.

III. PROPOSED CONTROL STRUCTURE

The schematic diagram of the proposed S-VOC-based system-level grid-forming controller architecture is illustrated in Fig. 2. The proposed controller consists of four main functional building blocks as follows:

1) The S-VOC

2) Instantaneous to synchronous reference frame transformation

3) Nested voltage and current control loops

4) Synchronous to instantaneous reference frame transformation

5) Feedback estimator to ride through an unbalanced fault

A. Symmetrical Component Based Virtual Oscillator Controller

The S-VOC provides time-domain synchronization with the positive, negative, and zero sequence voltages of a connected electrical network simultaneously. The S-VOC also provides positive, negative, and zero sequence droop functionalities. The systematic development and detailed mathematical modeling of an S-VOC are presented in our previous work, [23]. As shown in Fig. 3(a), the S-VOC produces reference voltages \( v_{xq}^* \), \( x \in \{a, b, c\} \) for the nested voltage controller in instantaneous reference frame. The lagging orthogonal components of the reference voltages, i.e., \( v_{xq}^* \), \( x \in \{a, b, c\} \) are also provided by the S-VOC.
B. Instantaneous to Synchronous Reference Frame Transformation

The nested voltage and current controllers work in the synchronous reference frame. Instantaneous parameters of an individual phase are converted to synchronous reference-frame-based parameters using the reference voltage of the same individual phase, as shown in Fig. 3(b). For three separate phases, separate reference frames are used. The reference voltage of an individual phase \((v^*_x); x \in \{a, b, c\}\) which is provided by the S-VOC is used as the direct axis for the same phase. The lagging orthogonal component of the reference voltage \((v^*_q); x \in \{a, b, c\}\) is used as the quadrature axis. Throughout this article, the instantaneous parameters are denoted by small letters, and the synchronous reference-frame-based parameters are denoted by capital letters.

In the synchronous reference frame, the output voltages of the S-VOC are denoted as \(V^*_x\) \((x \in \{a, b, c\})\) and derived as

\[
V^*_x = \sqrt{(v^*_x)^2 + (v^*_q)^2}; \quad V^*_x = 0; \quad (x \in \{a, b, c\}).
\]  

(1)

The voltages of the PCC and the inductor currents in the synchronous reference frame are denoted as \(V_{0xq}\) and \(I_{0xq}\), respectively, \((x \in \{a, b, c\})\) and derived as

\[
\begin{align*}
\dot{V}_{0xq} &:= \frac{v^*_x}{V^*_x}; \quad \dot{V}_{0xq} := \frac{v^*_q}{V^*_x}; \quad (x \in \{a, b, c\}) \\
\begin{bmatrix} V_{0xd} \\ V_{0xq} \end{bmatrix} &:= \begin{bmatrix} \dot{V}_{0xd} \\ \dot{V}_{0xq} \end{bmatrix}; \quad (x \in \{a, b, c\}) \\
\begin{bmatrix} I_{0xd} \\ I_{0xq} \end{bmatrix} &:= \begin{bmatrix} \dot{I}_{0xd} \\ \dot{I}_{0xq} \end{bmatrix}; \quad (x \in \{a, b, c\}).
\end{align*}
\]  

(2)

The variables \(v_{0abcd}\) and \(i_{0abcd}\) represents the instantaneous three-phase voltages of the PCC and the inductor currents of the inverter. The lagging orthogonal components of \(v_{0abcd}\) and \(i_{0abcd}\) are denoted by \(v_{0abcq}\) and \(i_{0abcq}\).

C. Nested Voltage and Current Control Loops

An individual nested control loop is dedicated to each phase to decouple control over the phases. Decoupling control is also included over the direct and quadrature axis. Proportional-integral (PI) controllers are used to regulate the voltages of the PCC (capacitor voltages) \(v_{0abc}\) and the inductor currents \(i_{0abc}\). The block diagram of a single nested control loop for an individual phase is illustrated in Fig. 4. Antiwindup function and a saturation block are included in the voltage controller to provide overcurrent protection.

The voltage controllers produce the reference inductor currents \(I^*_0; x \in \{a, b, c\}\) for the current controllers in the synchronous reference frame. The model of the voltage controller is presented in the s-domain as

\[
I^*_{0xd} = \left( K_{pi} + \frac{K_{ii}}{s} \right) \left( V^*_x - V_{0xd} \right) - \omega_n C_f V_{0xq}
\]  

(5)

\[
I^*_{0xq} = \left( K_{pi} + \frac{K_{ii}}{s} \right) \left( V^*_q - V_{0xq} \right) + \omega_n C_f V_{0xd}.
\]  

(6)

The proportional and integral gain of the voltage controller are denoted by \(K_{pi}\) and \(K_{ii}\), respectively. The variables \(\omega_n\) and \(C_f\) represent the value of the nominal frequency of the system and filter capacitor, respectively.

The current controllers produce the control voltages \(V^*_{invxd}, V^*_{invxq}; x \in \{a, b, c\}\) for the individual phases of the three-phase inverter in the synchronous reference frame.

The model of the current controller is presented in the s-domain as

\[
V^*_{invxd} = \left( K_{pi} + \frac{K_{ii}}{s} \right) \left( I^*_0 - I_{0xd} \right) + V_{0xd} - \omega_n L_f I_{0xq}
\]  

(7)

\[
V^*_{invxq} = \left( K_{pi} + \frac{K_{ii}}{s} \right) \left( I^*_0 - I_{0xq} \right) + V_{0xq} + \omega_n L_f I_{0xd}.
\]  

(8)

The variables \(K_{pi}\) and \(K_{ii}\) are the proportional and integral gain of the current controller, respectively. The value of the filter inductor is denoted by \(L_f\).

D. Synchronous to Instantaneous Reference Frame Transformation

The nested controller produces the reference voltages \(V^*_{inv}, V^*_{invxq}; x \in \{a, b, c\}\) for individual phases of the three-phase inverter in the synchronous reference frame. The instantaneous reference voltages \((v^*_{invxq}; x \in \{a, b, c\}\) are derived as

\[
\begin{bmatrix} v^*_{invx} \end{bmatrix} = \begin{bmatrix} \hat{v}^*_{xd} \\ \hat{v}^*_{xq} \end{bmatrix} = \begin{bmatrix} V^*_{invxd} \\ V^*_{invxq} \end{bmatrix}; \quad (x \in \{a, b, c\}).
\]  

(9)
E. Feedback Estimator to Ride Through an Unbalanced Fault

A VO uses the output currents of the inverter as feedback explicitly to achieve synchronization with a connected electrical network. During an unbalanced fault, the synchronization is severely affected because of the following reason.

During an unbalanced fault, for a healthy phase, the output current is the result of the interaction between the phase voltage of the VO and the connected network. At the same time, the output current of a faulty phase stays constant at the overcurrent limit due to the activation of the saturation block and the antiwindup function. The current at a faulty phase is no longer the result of the interaction between the phase voltage of the VO and the connected network. As a consequence, the output current of a faulty phase causes significant adverse effects on the grid-forming operation in a healthy phase by deteriorating the overall effective synchronization of the VO with the connected network.

During an unbalanced fault, a grid-forming inverter should meet three objectives simultaneously. The three objectives are as follows:

1. to limit the output current of a faulty phase;
2. to support the faulty phase with reactive power;
3. to maintain regular and unaffected operation at a healthy phase.

The proposed S-VO based grid-forming controller fulfills the above-mentioned objectives using a feedback estimator. As shown in Fig. 2., the feedback estimator is activated only during an unbalanced fault condition. The healthy phases are considered as the reference during an unbalanced fault to maintain effective synchronization between the S-VO and the connected network. The output currents of the healthy phases are used to derive the estimated current feedback for the faulty phases, as shown in Fig. 5.

The logic behind the estimation of the feedback is as follows.

Step 1: The fault detector, as shown in Fig. 2., detects the sequences of the faulty phases.

Step 2: The fault detector activates the “Feedback Estimator” block to derive the feedback for unbalanced fault conditions. The feedback for the faulty phases is estimated from the output currents of the healthy phases, as shown in Fig. 5. There are three phases, $P_1$, $P_2$, and $P_3$, where the sequence is predefined and given as

$$P_1 \angle 0^\circ = P_2 \angle 120^\circ = P_3 \angle 240^\circ.$$  \hspace{1cm} (10)

There are two different possible unbalanced fault conditions.

Condition 1- One phase is under fault: One of the three phases, i.e., $z$th ($z \in 1, 2, 3$) phase, $P_z$, is under fault. The feedback for the $z$th phase, $i_{P_z}$, is derived as

$$i_{P_z} = - \sum n_{iinv}P_j; (j \in 12, 3), (j \neq z)$$ \hspace{1cm} (11)

where $n_{iinv}P_j$ is the output current of phase $P_j$.

Condition 2- Two phases under fault: One of the three phases, i.e., $k$th ($k \in 1, 2, 3$) phase is healthy. The feedback for the faulty phases $i_{P(k+n)}$ and $i_{P(k-n)}$ are derived as

$$i_{P(k+n)} = i_{invP_k} \angle - (n \times 120^\circ); n \in 12$$ \hspace{1cm} (12)

$$i_{P(k-n)} = i_{invP_k} \angle (n \times 120^\circ); n \in 12$$ \hspace{1cm} (13)

$$(n + k) \in 12, 3$$ \hspace{1cm} (14)

where $i_{invP_k}$ is the output current of phase $P_k$.

Step 3: The feedback to the S-VO is replaced by the estimated feedback during an unbalanced fault, as shown in Fig. 2.

IV. SIMULATION STUDIES

The performance of the proposed controller is investigated using simulation studies in this section. The schematic diagram of the system considered for the simulation studies is presented in Fig. 2. The specification of the system is given in Table I.

The performance of the proposed controller is investigated thoroughly under the following conditions.

A. Tracking of the Active Power Reference

The three-phase active power reference, $P^*$, is set to 15 kW initially. The reference is then changed to 30 kW at $t = 50$ ms. The active power ($P_{abc}$) and current ($i_{invabc}$) outputs of the inverter are depicted in Fig. 6(a) and (b), respectively. The controller successfully tracks the active power reference.

B. Reactive Power Support During an Unbalanced Voltage Sag

The voltage amplitude of phase-a is lowered by 10% from the grid side at $t = 100$ ms while the active power reference, $P^*$, is...
Fig. 6. Tracking of the active power reference by the proposed controller. (a) Active power outputs of individual phases. (b) Output phase currents.

Fig. 7. Reactive power support by the proposed controller during an unbalanced voltage sag at phase-a. (a) Reactive power outputs of individual phases. (b) Individual phase currents.

Fig. 8. Reactive power support by the proposed controller during a balanced voltage sag. (a) Reactive power outputs of individual phases. (b) Individual phase currents of the voltage source.

set to 30 kW. The reactive power ($Q_{abc}$) and current ($i_{invabc}$) outputs of individual phases of the grid-forming voltage source are shown in Fig. 7(a) and (b), respectively. The voltage source successfully supports phase-a of the connected network with reactive power in the presence of the voltage sag.

C. Reactive Power Support During a Balanced Voltage Sag

A balanced 10% voltage sag is created at the PCC at $t = 100$ ms. The three-phase active power reference, $P^*$, is set to 30 kW. The reactive power outputs ($Q_{abc}$) and output currents ($i_{invabc}$) of individual phases of the voltage source are depicted in Fig. 8(a) and (b), respectively. As intended, all three phases of the connected network are supported by the voltage source with reactive power.

D. Riding Through a Single Line to Ground Fault

A single line to ground fault is created at phase-a near the PCC at $t = 1$ s while the three-phase active power reference, $P^*$, is set to 30 kW. As shown in Fig. 9(a) and (b), the voltage amplitude of phase-a of the PCC is reduced to 0.1 PU. The inductor currents ($i_{0abc}$) and the power outputs ($P_{abc}$ and $Q_{abc}$) of the individual phases of the voltage source are shown in Fig. 9(c)–(f). As intended, the inductor current of phase-a is restricted by the proposed controller to the overcurrent limit (50 A rms). The faulty phase (phase-a) is supported with reactive power. At the same time, the operation at phase-b and phase-c remain unaffected.

Next, a line-to-ground dead short circuit is created at phase-a of the PCC at $t = 1$ s. The active power reference, $P^*$, is set to 30 kW. The filter inductor is the only current limiting impedance between the terminal of the inverter and the ground during the fault. As illustrated in Fig. 10(a) and (b), the voltage amplitude of phase-a of the PCC is reduced to 0 PU. The inductor currents ($i_{0abc}$) and the power outputs ($P_{abc}$ and $Q_{abc}$) of the individual phases of the voltage source are shown in Fig. 10(c)–(f). The proposed controller restricts the inductor current of phase-a under the overcurrent limit (50 A rms) while the operation at phase-b and phase-c remains unaffected.
E. Ride Through a Double Line to Ground Fault

Next, a double line to ground fault is created near the PCC at \( t = 1 \) s. The voltage amplitude of phase-b and phase-c of the PCC is reduced to 0.1 PU, as seen in Fig. 11(a) and (b). As depicted in Fig. 11(c) and (d), the inductor currents of phase-b and phase-c are restricted by the proposed controller under the overcurrent limit (50 A rms). The voltage source also supports phase-b and phase-c with reactive power during the fault, while a normal operation, is maintained at phase-a.

F. Riding Through a Double Line (Line-to-Line) Fault

Finally, a line-to-line fault is created at the PCC at \( t = 1 \) s. Phase-b and phase-c are shorted at the PCC. The voltages of phase-b and phase-c of the PCC shift \(-60^\circ\) and \(+60^\circ\), respectively, as seen from Fig. 12(a) and (b). As depicted in Fig. 12(c) and (d), the controller successfully restricts the output currents of phase-b and phase-c under the overcurrent limit (50 A rms). The operation at the healthy phase (phase-a) remains unaffected.

V. EXPERIMENTAL RESULTS

This section presents the experimental validation of the proposed S-VOC-based grid-forming controller.

A. Tracking of Active Power Reference

The schematic diagram of the experimental setup is depicted in Fig. 13.

The three-phase inverter, \( \text{Inv}_1 \), is connected to the utility grid using the three-phase autotransformer, \( G_1 \). The dc-link \( V_{\text{dc,n}} \) of the three-phase inverter is energized using a three-phase rectifier, \( \text{Rec}_1 \). The autotransformer, \( G_2 \), connects the rectifier, \( \text{Rec}_1 \), to the utility grid. Table II contains the specifications of the experimental setup.

| Symbol | Description | Value |
|--------|-------------|-------|
| \( V_{\text{ng}} \) | Nominal voltage: grid emulator | 150 V |
| \( \omega_{\text{ng}} \) | Nominal frequency: grid emulator | 2\( \pi \)50 rad/s |
| \( L_p \) | Filter inductor: sources | 2 mH/Phase |
| \( C_p \) | Filter capacitor: sources | 20 \( \mu \)F/Phase |
| \( V_{\text{dc,p}}, V_{\text{dc,c}} \) | dc-link voltages (split Capacitor) | 250 V |
| \( I_{\text{max}} \) | Maximum output current (rms) | 13.5 A |
| \( f_{\text{sw}} \) | Switching frequency | 5 kHz |
| \( T_s \) | Sampling time of the controller | 50 \( \mu \)s |

The three-phase active power reference, \( P^* \), is initially set to 3000 W. As shown in Fig. 14, each phase of the three-phase inverter, \( \text{Inv}_1 \), initially injects 1000 W of active power into the grid. The active power reference, \( P^* \), is changed from 3000 to 4500 W at \( t = 120 \) ms. The controller successfully tracks the active power reference, as seen in Fig. 14.

B. Reactive Power Support During an Unbalanced Voltage Sag

A grid emulator is used, as illustrated in Fig. 15, to investigate the performance of the proposed controller in the presence of different voltage sags. The inverter, \( \text{Inv}_2 \), acts as a constant amplitude and constant frequency voltage source behind the inductance, \( L_g \). The voltage amplitudes of individual phases

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Fig. 12. Line-to-line fault ride-through. (a) Voltage profile of the PCC, \( v_{PCC} \). (b) Magnified view of \( v_{PCC} \). (c) Inductor currents of the voltage source, \( i_0 \). (d) Magnified view of \( i_0 \). (e) and (f) Active and reactive power outputs of the individual phases of the voltage source, respectively.

Fig. 13. Schematic diagram of the experimental setup used for validating the performance of the proposed controller under normal grid conditions.

Fig. 14. Tracking of active power reference by the grid-forming inverter. (a) Active power outputs of individual phases. (b) Individual phase currents of the inverter.

Fig. 15. Schematic diagram of the experimental setup used for validating the performance of the proposed controller in the presence of voltage sag and fault conditions.

Fig. 16. Reactive power support by the grid-forming inverter in the presence of voltage sags at phase-b and phase-c. (a) Reactive power outputs of individual phases. (b) Individual phase currents of the inverter.

The performance of the proposed controller is tested here in the presence of unbalanced voltage sag. The three-phase active power reference, \( P^* \), is set to 3000W. A 10% voltage sag is created at phase-b and phase-c of the PCC by the grid emulator. The voltage amplitude of phase-a is kept constant at the nominal value. The reactive power and current outputs of the inverter, \( \text{Inv}_1 \), are shown in Fig. 16. The inverter successfully supports phase-b and phase-c with reactive power in the presence of the voltage sag.

C. Fault Ride-Through Performance

The grid emulator, as depicted in Fig. 15, is used to investigate the performance of the proposed controller under two different fault conditions. The three-phase active power reference, \( P^* \), is set to 3000 W during the following experiments. At first, the voltage amplitude of phase-a of the grid emulator is lowered to 10% of the nominal voltage, \( V_{gn} \), from the grid emulator. The voltage amplitudes of phase-b and phase-c are kept constant at the nominal value. The voltage profile of the PCC during the fault is shown in Fig. 17(a). The current and power outputs of the inverter, \( \text{Inv}_1 \), are demonstrated in Fig. 17(b)–(d), respectively. The proposed controller successfully limits the output current of phase-a. The grid-forming inverter supports phase-a with reactive power during the fault condition. At the same time, the operation at phase-b and phase-c remains nearly unaffected.

Next, the voltage amplitude of phase-b and phase-c of the grid emulator is lowered to 10% of the nominal voltage, \( V_{gn} \). The voltage amplitude of phase-a is kept constant at \( V_{gn} \). The
The inverter supports phase-b and phase-c with reactive power max at phase-b and phase-c.

VI. CONCLUSION

VOC is the most advanced control technique for grid-forming inverters. However, the performance of an existing VOC deteriorates in the presence of unbalanced grid voltages or unbalanced fault conditions. This article has focused on addressing the mentioned issue by introducing an improved VO-based grid-forming control architecture. The proposed control architecture successfully integrates the S-VOC with nested control loops. As a result, the proposed controller has an improved decoupling in control over individual phases. The mentioned phase decoupling control feature helped the proposed controller to achieve superior grid-forming performance in unbalanced grid voltages. At the same time, the nested control loop helped to meet essential system-level functionalities such as capacitor voltage regulation and overcurrent protection. Next, an essential modification was introduced in the feedback of a VOC. The proposed feedback estimator was activated only in the presence of an unbalanced fault to retain effective synchronization with the connected network. As a result, the controller successfully maintains normal operation at a health phase while limiting the output current at a faulty phase.

The proposed control architecture improves the decoupling in control over individual phases without altering the existing general nested control loop structure. As a result, it becomes easier to include newer objective functions into a VO-based grid-forming controller. In the future, the authors will focus on incorporating additional functionalities, such as power quality improvement, into the proposed control architecture.

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