Parasitic-Based Active Gate Driver Improving the Turn-On Process of 1.7 kV SiC Power MOSFET

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Abstract: This article discusses an active gate driver for a 1.7 kV/325 A SiC MOSFET module. The main purpose of the driver is to adjust the gate voltage in specified moments to speed up the turn-on cycle and reduce the amount of dissipated energy. Moreover, an adequate manipulation of the gate voltage is necessary as the gate current should be reduced during the rise of the drain current to avoid overshoots and oscillations. The gate voltage is switched at the right moments on the basis of the feedback signal provided from a measurement of the voltage across the parasitic source inductance of the module. This approach simplifies the circuit and provides no additional power losses in the measuring circuit. The paper contains the theoretical background and detailed description of the active gate driver design. The model of the parasitic-based active gate driver was verified using the double-pulse procedure both in Saber simulations and laboratory experiments. The active gate driver decreases the turn-on energy of a 1.7 kV/325 A SiC MOSFET by 7% comparing to a conventional gate driver ($V_{DS} = 900$ V, $I_D = 270$ A, $R_C = 20$ Ω). Furthermore, the proposed active gate driver lowered the turn-on cycle time from 478 to 390 ns without any serious oscillations in the main circuit.

Keywords: active gate driver; medium voltage; power losses; SiC MOSFET

1. Introduction

Nowadays, medium-voltage (MV) silicon carbide (SiC) MOSFET power modules are used in a significant amount of power applications, including electric vehicle power systems and small renewable power plants based on photovoltaics [1]. Manufacturers of MV SiC MOSFETs provide new devices with short switching times counted in hundreds of nanoseconds which is related to low switching energies and power losses. On the other hand, high values of the drain current and drain-source voltages of those devices are the reason for significant $di/dt$ and $dv/dt$ ratios observed in power circuits. Parasitic elements under large $di/dt$ and $dv/dt$ ratios cause oscillations and overshoots [2–4]; thus, fast switching MV SiC MOSFETs are the source of EMI problems [5–7]. There are many ways to suppress these negative effects, for example, by decreasing the switching speed through an increase in the gate resistance, but the price is higher power loss. Another possibility is active gate driving, discussed in this paper. A conventional gate driver (CGD) with fixed gate voltage and resistances has no dynamic control of the gate current of the device. However, some drivers can manipulate the gate current in open loop by the change of the drain current and drain-source voltages of those devices. This approach simplifies the circuit and provides no additional power losses in the measuring circuit. The paper contains the theoretical background and detailed description of the active gate driver design. The model of the parasitic-based active gate driver was verified using the double-pulse procedure both in Saber simulations and laboratory experiments. The active gate driver decreases the turn-on energy of a 1.7 kV/325 A SiC MOSFET by 7% comparing to a conventional gate driver ($V_{DS} = 900$ V, $I_D = 270$ A, $R_C = 20$ Ω). Furthermore, the proposed active gate driver lowered the turn-on cycle time from 478 to 390 ns without any serious oscillations in the main circuit.

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protection, \( v_{DS} \) and \( i_D \) overshoot or oscillations caused by a short switching period due to parasitics. In [9], active control of the gate-source voltage was realized via voltage injection to the gate: at the turn-on cycle, the AGD pulls down the gate potential to the ground to slow down the \( di/dt \) ratio. The aim of this research was to reduce the switching speed of a 1.2 kV/33 A SiC MOSFET in order to suppress voltage and current overshoot at turn-off and turn-on, respectively. Both simulation and experimental results showed that the authors reduced those negative effects significantly. On the other hand, switching losses were increased, since \( di/dt \) and \( dv/dt \) ratios were reduced as well. Furthermore, the AGD proposed by the authors was designed for a low-power SiC MOSFET. The switching trajectory improvement of an AGD for a 1.2 kV/40 A SiC MOSFET was discussed in [10], where the feedback loop of the driver was based on the resistive measurement derived from the drain-source voltage \( v_{DS} \) and drain current \( i_D \). Then, the gate resistance was changed to manipulate the gate current and, in consequence, the AGD influenced the \( di/dt \) and \( dv/dt \) ratios. This type of measurement would be hard to implement in a MV SiC MOSFET since an auxiliary circuit is necessary. Furthermore, resistive measurements of the drain current and drain-source voltage generate additional power losses, which is undesirable in power electronic applications. The same type of the feedback signal was applied in an AGD where the purpose was to minimize the effects of parasitic inductances in a converter layout with a 1.2 kV/40 A discrete SiC MOSFET [11]. The authors used the same method as in [10] to modulate the gate current value in specified moments of the switching cycle. The researched AGD was experimentally validated by the authors with a double-pulse test and SiC MOSFET-based inverter with motor load. The AGD provided promising results in case of the turn-on and turn-off cycles. Unfortunately, the authors examined this solution only for low currents so it is not known if this approach could be used in high-power applications. The AGD can be also used as a short circuit protection of the device through the employment of a Rogowski coil to measure the current and use it as a feedback signal [12]. In this particular case, the AGD was designed for a 1.7 kV/325 A MV SiC MOSFET. Unfortunately, this solution generates additional expenses to the summary AGD cost as it needs an auxiliary circuit to be used in case of a feedback loop. In addition, the AGD can be used for voltage balancing in series connection of a 1.7 kV half-bridge SiC MOSFET module, which is the main topic in the paper [13]. As the closed-loop test results showed, the authors accomplished balancing of the drain-source voltage values in series connection in comparison to natural voltage sharing. In this case, the feedback signal of the AGD was acquired with a switch voltage sensor based on an RC branch connected to the drain of the SiC MOSFET. The main weakness of this solution was that the quantity of switching energy losses increased by less than 7.5%. Furthermore, the AGD can be used for SiC MOSFET oscillations damping [14] as well. In [14], the authors solved problems with overshoot and ringing in the body diode under inductive load. The subject of the experimental studies in this case was a 1.2 kV/36 A discrete SiC MOSFET which was tested with only a 400 V DC bus. The results indicated that the AGD had an impact on the oscillations and successfully suppressed them. However, in case of MV voltages, power modules are usually characterized by higher parasitic inductances and capacitances, and it is much more complicated to use closed-loop solutions due to disturbances in the feedback signals. Moreover, there are studies with an AGD for a 1.7 kV SiC MOSFET where the feedback loop is based on the parasitic inductances of the source and drain [15], and the multi-level gate voltage method is used for turn-on and turn-off cycle improvement. The application of the AGD reduced the turn-on energy by 30% for the 1.7 kV SiC MOSFET and showed a positive impact on EMI performance. To avoid high propagation delays, the main control unit of the AGD in this paper was based on a CPLD; alas, it made the whole device more complex. A multi-level gate voltage method for a 3.3 kV/450 A SiC MOSFET in open loop was described in [16]. This method was verified in a double-pulse test (DPT) and in a half-bridge inverter. The turn-on energy decreased by half through the manipulation of the gate driver supply. As a result, the PWM frequency of the inverter
can be doubled. However, the gate driver works in open loop which limits the system capabilities for variable drain currents.

According to the literature review, it can be seen that active gate drivers are discussed mostly for low-voltage and -current transistors, while those for 1.7 kV SiC MOSFET power modules are rare [12,13,15]. Moreover, a lot of the articles presented discrete 1.2 kV SiC MOSFETs [9–11,14]. Some of the AGDs proposed in the papers are for MV; however, they have limited drain current capabilities, thus excluding them from most high-power applications. Therefore, the subject of this paper is to show simulation results and experimental validation of an AGD for MV and a high-current SiC MOSFET based on a power module. The closed-loop AGD for a 1.7 kV/325 A SiC MOSFET proposed in this paper uses voltage measurement across the parasitic source inductance to simplify the measuring circuit. Unlike most of the presented AGDs in the literature, this kind of feedback loop does not generate any additional energy losses to the system. Additionally, the AGD improves the turn-on cycle of the device by manipulation of the gate voltage to decrease the dissipated energy by increasing the $dv_{DS}/dt$ ratio and suppressing the drain current oscillations. The proposed solution can be used in mostly all power SiC MOSFETs, affecting instant losses depletion without strengthening EMI. Modulation of the gate current is acquired by application of the multi-level gate voltage method. This approach allows having a constant value of the gate resistance, which optimizes the layout of the gate driver for the MV SiC MOSFET. The model of the proposed AGD was designed without any complex circuits such as CPLD as in [15] and is based on low-cost, high-speed, off-the-shelf integrated circuits. The main assumption was to improve the turn-on process with the proposed method since turn-on is usually the cause of much higher power losses in comparison to turn-off in the case of MV SiC MOSFETs in most hard switching applications [17]. The proposed AGD operates independently from the maximum drain current value in a range of operational conditions, which will be also discussed later in the paper. Thus, it can be used in highly efficient MV high-power electronic applications. The paper is organized as follows. The Section 2 of this paper provides a theoretical introduction of the methods used in the developed system. Then, the concept of the driver is verified in simulations in the Section 3. The experimental results and comparison of the AGD with CGD are shown in Section 4. Finally, the paper is concluded in Section 5.

2. The Active Gate Driver

Usually, the AGD input is connected to some feedback signal. A closed-loop signal can be obtained directly from the drain-source voltage, drain current or gate-source voltage [10,11]. However, all of those signals except the gate-source voltage are hard to be measured in case of MV SiC MOSFETs. For example, to measure the $v_{DS}$ voltage, the measuring resistance must be connected between the drain and the source, which makes the complete circuit more complicated and influences the main circuit performance [10]. An approach that is based on the feedback signal in the form of measurement of $i_D$ and $v_{DS}$ requires a complex subcircuit to be included in the AGD. In the proposed AGD, the closed loop is provided with the $V_{LS}$ voltage (1). In order to explain this more clearly, a SiC MOSFET connected in the double-pulse test, as presented in Figure 1, is considered. The SiC MOSFET active gate driver is connected to the gate of the transistor through $R_G$ and its reference ground is a Kelvin source ($S_{Kelvin}$). $S_{Kelvin}$ in SiC MOSFETs is terminal, placed as close as possible to the actual chip inside the module and used for driving purposes. If the device was driven in reference to the power source ($S$), the source parasitic inductance $L_S$ would have undesired effects on the gate current $i_G$. The existence of the parasitic inductance $L_S$ between $S_{Kelvin}$ and $S$ is naturally caused by internal connections of the SiC MOSFET. Dependence of the temperature for the value of $L_S$ is very limited, and it decreases slightly with rising temperature [18]; hence, temperature fluctuations can be omitted when considering this method. From (1), it can be considered that the value of $V_{LS}$ is proportional to the value of $L_S$ and $di_D/dt$. Thus, the value of $i_D$ and its dynamics can be estimated from $V_{LS}$. In an ideal case of the turn-on cycle, before $i_D$ starts to rise, the
$V_{Ls}$ value would be always 0 V; at the moment when $i_D$ begins to rise, it should have a constant value proportional to the slew rate of $i_D$. After the turn-on cycle, the value of $V_{Ls}$ should be 0 V. A feedback loop based on $V_{Ls}$ makes the AGD independent from the drain current values during the switching cycle because the drain current dynamic is defined by the changes in the $V_{Ls}$ value from 0 V to positive and negative values. Furthermore, $V_{Ls}$ peak values are not dependent on the maximal drain current values, but strictly on the $di_D/dt$ ratio (1) which is only reliant on the fixed values, thus making it an adequate signal to sense the individual stages of the turn-on cycle. Summarizing, the depicted closed-loop method simplifies the whole structure of the AGD and does not affect the power circuit of the SiC MOSFET.

$$V_{Ls} = L_s \frac{di_D(t)}{dt} \quad (1)$$

**Figure 1.** SiC MOSFET (DUT) in the double-pulse test (DPT) setup with the active gate driver (AGD) in which the feedback loop is based on the parasitic source inductance voltage ($V_{Ls}$). $V_{GG}$—gate voltage, $R_G$—gate resistance, $S_{Kelvin}$—Kevin source, $i_D$—drain current, $v_{DS}$—drain-source voltage, $L_s$—parasitic inductance, $v_{GS}$—gate-source voltage.

**Gate Voltage Manipulation for the Turn-On Cycle Improvement**

The measurement of the $V_{Ls}$ voltage can be used as a feedback loop for the method presented in Figure 2. The multi-level gate voltage ($V_{GG}$—see Figure 1) method’s purpose is to decrease power losses, drain current overshoot ($i_{rr}$) and oscillations of the drain current at the turn-on cycle of a SiC MOSFET by changing the $V_{GG}$ voltage from 15 V to higher at times specified by the regulation system. For the chosen device (CAS300M17BM2 [19]), the $V_{GG}$ value recommended by the manufacturers of SiC MOSFETs is 15 V; thus, such level was chosen. The second level of $V_{GG}$ may be selected between 15 and 30 V—the peak gate voltage allowed for this module; in this case, 30 V was chosen to obtain the maximum increase in the switching speed without damaging the gate oxide layer. Similar to other AGD methods for SiC MOSFET switching improvement, this approach is based on gate current manipulation of the device at the right moments of the switching transient. Thus, in that case, the aim is to improve the turn-on cycle without an unnecessary increase in $di_D/dt$ that would cause overshoot and oscillations of the drain current. What distinguishes this method from the many others is that the $R_G$ value is constant. Usually, the gate resistor

$R_G$ is placed as near as possible to the gate terminal of the SiC MOSFET to make the $i_G$ path as short as possible. The sequence of the proposed method appears as follows: at $t_0$, the driving signal (DS) is changing from the low state to the high state which begins the turn-on cycle of the SiC MOSFET. The $V_{GG}$ voltage at the same time is changing from $-5$ (low stage $V_{GG}$ level) to 30 V. The purpose of the first boost of $V_{GG}$ to the value of 30 V is to reduce the time delay between $DS$ and $v_{GS}$ reaching the threshold voltage $V_{Th}$. At $t_0$, the gate-source voltage $v_{GS}$ starts to rise from zero. After the $v_{GS}$ voltage crosses the threshold voltage $V_{Th}$ at $t_1$, the drain current $i_D$ starts to rise. The $V_{LS}$ voltage at $t_1$ will start to rise from 0 V to the value proportional to $di_D/dt$ and $L_S$; thus, the beginning of the rise of the current can be sensed. In order to decrease the $di_D/dt$ ratio during the interval between $t_1$ and $t_2$, $V_{GG}$ is reduced to 15 V at time $t_1$.

This gate current manipulation stage target is to not cause any serious oscillations of the drain current in the main power circuit. Then, the gate-source voltage is latched from

![Figure 2. The multi-level gate voltage method waveforms for the turn-on cycle improvement of the SiC MOSFET with an inductive load. DS—logical driving signal of the device, $V_{GG}$—gate voltage of the SiC MOSFET, $v_{GS}$—gate-source voltage, $v_{DS}$—drain-source voltage, $i_D$—drain current, $V_{DD}$—drain-source voltage before the turn-on of the MOSFET, $I_0$—drain current after switching on the device, $V_{Th}$—threshold voltage, $V_{Miller}$—Miller voltage, $I_{ir}$—drain current overshoot, $V_{LS}$—ideal source parasitic inductance voltage waveform.](image-url)
t_2 \text{ to } t_3 \text{ at Miller’s plateau. } t_2 \text{ is the moment when the drain-source voltage } V_{DS} \text{ is starting to decrease and when the } t_3 \text{ has reached its maximum value, which is sensed based on } V_{Ls} \text{ changes from positive to negative values as the drain current overshoot occurs. The } V_{GG} \text{ voltage is switched again to 30 V, which increases the } \frac{dV_{DS}}{dt} \text{ ratio and reduces the period between } t_2 \text{ and } t_3 \text{ which in fact decreases the turn-on power losses in the device and its switching period. Notice that } t_2 \text{ occurs when the drain current has reached its maximum value. In order to suppress further negative effects of } i_i \text{ overshoot, the gate current is increased through modification of the value of } V_{GG} \text{ to 30 V. To prevent damaging the gate of the device, } V_{GG} \text{ is again set to 15 V at } t_3. \text{ Finally, at } t_3, \text{ the gate-source voltage } V_{GS} \text{ reaches 15 V, equal to } V_{GG}. \text{ The feedback loop of the studied device is based on sensing the two from moments in the turn-on cycle occurring at } t_1 \text{ and } t_2, \text{ based on the } V_{Ls} \text{ measurements and thus responding with changes in the } V_{GG} \text{ values appropriately, as depicted in Figure 2.}

The multi-level gate voltage method impact can be theoretically explained using Equations (2)–(6) based on fundamental knowledge [20]. From Equation (2), it can be concluded that the higher the voltage } V_{GG} \text{ and the lower the resistance } R_G, \text{ the greater the gate current } i_G. \text{ However, the maximum } V_{GG} \text{ should be taken into consideration.}

\[ i_G(t) = \frac{V_{GG} - V_{GS}(t)}{R_G} \]  

(2)

In the proposed method, } R_G \text{ is fixed so the gate current is only dependent on the difference between } V_{GG} \text{ and } v_{GS}. \text{ The instantaneous gate-source voltage } v_{GS} \text{ in the switching transient (3) also mainly depends on the } V_{GG}, C_{GD} \text{ and } C_{GS} \text{ values. In the proposed method, the } V_{GG} \text{ voltage is set to 30 V from } I_0 \text{ to } t_1 \text{ to minimize the delay time between the } DS \text{ signal and the } t_1 \text{ moment where the } v_{GS} \text{ crosses the threshold value and the drain current starts to rise.}

\[ v_{GS}(t) = V_{GG} \left( 1 - e^{-\frac{t-t_0}{\tau}} \right), \tau = R_G(C_{GS} + C_{GD}) \]  

(3)

Delay time between } t_0 \text{ when } v_{GS} \text{ starts to rise and } t_1 \text{ when the MOSFET starts to conduct the drain current that is mainly dependent on the } V_{GG} \text{ voltage and constant values of the device, as shown in Equation (4). To compensate the delay between the rising edge of the } DS \text{ signal at } t_0 \text{ and } t_1 \text{ in } \Delta t_{10}. \text{ } V_{GG} \text{ is set to 30 V.}

\[ \Delta t_{10} = t_1 - t_0 = -\tau \ln \left( 1 - \frac{V_{Th}}{V_{GG}} \right) \]  

(4)

Another Equation (5) represents the rise time of the drain current from time } t_1 \text{ to } t_2, \text{ where } I_0 \text{ is the drain current in the steady state after the turn-on cycle (see Figure 2), } g_m \text{ is the transconductance and } V_{Th} \text{ is the threshold voltage at the turn-on cycle. A low value of } \Delta t_{21} \text{ leads to a high } \frac{dI_{DS}}{dt} \text{ ratio and, in consequence, current overshoot caused by the Schottky body diode (SBD) and the parasitic elements of the device. Thus, it is the reason for the } V_{GG} \text{ voltage depletion in } t_1 \text{ from 30 to 15 V.}

\[ \Delta t_{21} = t_2 - t_1 = \tau \ln \frac{g_m V_{GG}}{g_m(V_{GG} - V_{Th})} - I_0 \]  

(5)

The time of the drain-source voltage falling in the turn-on cycle can be presented by Equation (6), where } V_{DD} \text{ is the drain-source voltage in the time before } t_0 \text{ and } V_{DS(ON)} \text{ is the drain-source resistance of the SiC MOSFET. The value of the } \Delta t_{32} \text{ time should be as low as possible in order to increase the } \frac{dV_{DS}}{dt} \text{ ratio, which will finally decrease the turn-on energy of the MOSFET. Small values of } \Delta t_{32} \text{ do not have any undesirable effects on the switching transient. Therefore, equations show that } V_{GG} \text{ manipulation based on precise moments in the turn-on cycle can decrease } \Delta t_{32}, \text{ which in consequence reduces switching losses. Moreover, the proposed method does not generate drain current overshoot and provides the possibility to increase the switching frequency of the SiC MOSFET only by}
replacing the gate driver in any SiC MOSFET with a Kelvin source. The SiC MOSFET with an AGD using the multi-level gate voltage technique and feedback loop based on $V_{LS}$ can be switched at same frequency as in normal conditions. To provide an adequate feedback signal, the AGD response time must be shorter than the whole time of the turn-on cycle of the device; thus, the operating frequency of the power device is not constrained. Usually, the maximum switching frequency of an MV SiC MOSFET power module is limited by the thermal dependency of the device on power losses. In the case of a transistor in power modules, the switching frequency is much lower (100–500 times) than the sum frequency of the turn-on and turn-off cycles.

$$\Delta t_{32} = t_3 - t_2 = R_G C_{GD} \frac{(V_{DD} - IV_{DS(ON)})}{(V_{GG} - V_{Th})}$$

(6)

3. Simulation Study

The proposed AGD circuit in the DPT configuration is presented in Figure 3. The chosen device is a half-bridge module (CAS300M17BM2), so the AGD is controlling only transistor $T_2$ (see Figure 3) during the DPT. $T_2$’s gate current $i_G$ is actively controlled by the AGD with the previously described method and $T_1$’s gate is connected constantly to $-5$ V (in reference to its source). In this particular case, $L_S$ is equal to 15 nH based on the datasheet.

![Figure 3. The AGD in DPT setup with half-bridge module 1.7 kV/325 A SiC MOSFET CAS300M17BM2.](image)

Simulation verification of the proposed AGD multi-level gate voltage method based on the parasitic inductance voltage measurement was conducted in Saber RD software. The CAS300M17BM2 module simulation model was provided by the producer of the device. The first steps of the research were to observe the waveforms of $V_{LS}$ with CGD and, basing on this, conclude if the method can be used in all SiC MOSFETs. The purpose of the simulation study was to verify the assumptions about the decrease in the turn-on time and energy in the chosen method. Finally, the main aim of the simulation was to measure power losses of the CGD at the turn-on cycle and compare them with the AGD. In simulations, the SiC MOSFET half-bridge module was connected in the DPT setup (Figure 3). Transistor $T_1$ was turned off and $T_2$ was the DUT. The gate resistance $R_G$ of both the AGD and CGD was set to a fixed value of 20 Ω. The main assumption of the similar value of the $R_G$ in tests
of the AGD and CGD was to obtain the same \( \frac{di_D}{dt} \) ratio at the turn-on of the device for both cases. \( T_1 \) was connected in parallel to the inductor \( L = 110 \, \mu \text{H} \). The CGD gate voltage \( V_{GG} \) was fixed at a value of 15 V at the turn-on (according to datasheet recommendations). The AGD gate voltage \( V_{GG} \) (Figure 2) had a variable value of either 15 or 30 V. The AGD simulation was conducted using the feedback signal from \( V_{Ls} \), which was connected to the Saber RD logical and electrical elements to provide the active control of the \( V_{GG} \) voltage. Delays of the components were not considered in that stage of the research. The DPT was conducted for four operating conditions at the turn-on cycle for the \( V_{DD} \) voltages of 700 or 900 V and \( I_0 \) currents of 170 or 270 A. However, the observations of the response of the AGD on the increasing \( I_0 \) current had smaller step of change to verify that this solution is independent from the variation in the drain current. The turn-on cycle using the CGD for \( V_{DD} = 700 \, \text{V}, \, I_0 = 270 \, \text{A} \) is shown in Figure 4. In comparison, the turn-on cycle with the AGD for the very same conditions is shown in Figure 5, where the difference in the voltage falling time is visible. The \( \frac{v_{ds}}{dt} \) ratio increased without any serious oscillations of \( i_D \), thus shortening the turn-on cycle of the device. Notice that in Figures 4 and 5, the \( i_D \) rising time is marked, and in both simulated cases, the \( \frac{di_D}{dt} \) ratio was the same (1 kA/\( \mu \text{s} \)) due to identical \( R_G \) values and \( V_{GG} \) levels in \( \Delta t_{21} \) (see Figure 2). Additionally, the simulations show that the AGD compensates the delay between the rising of the \( v_{GS} \) voltage and the moment when the device starts to conduct the drain current.

![Figure 4](image_url)

**Figure 4.** The turn-on cycle of the SiC MOSFET from module CAS300M17BM2 using conventional gate driver (CGD). \( V_{DD} = 700 \, \text{V}, \, I_0 = 270 \, \text{A}, \, V_{GG} = 15 \, \text{V} \).

Table 1 presents the results of the previously mentioned simulation. The turn-on energy mostly decreased for \( V_{DD} = 900 \, \text{V}, \, I_0 = 270 \, \text{A} \). The turn-on energy settled at 65.5 mJ for the CGD, whereas for the AGD, it reached just 45.9 mJ, resulting in a difference of roughly 30%. The smallest percentage disparity was measured for \( V_{DD} = 900 \, \text{V}, \, I_0 = 170 \, \text{A} \), and it was equal to 15%.

Simulations of the AGD in Saber RD software confirmed that the multi-level \( V_{GG} \) method is able to decrease the turn-on energy of the transistor from the CAS300M17BM2 SiC MOSFET module, and there is the possibility to use the feedback signal from the \( V_{Ls} \) voltage measurement, thus confirming the presumptions.
Figure 5. The turn-on cycle of the SiC MOSFET from module CAS300M17BM2 using AGD. $V_{DD} = 700 \text{ V}, I_0 = 270 \text{ A}$.

Table 1. The turn-on energy losses of CGD and AGD comparison from the simulation study.

| $V_{DD}$ | $I_0$ | $E_{on \ CGD}$ | $E_{on \ AGD}$ |
|----------|-------|----------------|----------------|
| 700 V    | 170 A | 24.0 mJ        | 19.4 mJ        |
| 700 V    | 270 A | 46.2 mJ        | 36.5 mJ        |
| 900 V    | 170 A | 32.4 mJ        | 27.4 mJ        |
| 900 V    | 270 A | 65.5 mJ        | 45.9 mJ        |

4. Experimental Verification

After the simulation study, the proposed AGD was verified by means of experiments—the simplified main electrical circuit of the proposed AGD for the MV SiC MOSFET is presented in Figure 6. After the simulation research and datasheet-based calculations, it was concluded that the $V_{Ls}$ voltage will be in the operational range of the integrated electronic circuits ($0/5 \text{ V}$) after adequate signal conditioning. The AGD feedback loop is provided by the connection of the filtering circuit of the AGD to the power source $S$ of the DUT. All depicted voltage levels in Figure 6 are referenced to the potential of the Kelvin source $S_{Kelvin}$. During the short switching time of the chosen SiC MOSFET with high-level power turn-on conditions, $V_{Ls}$ is filtered by ferrite beads (FBD) from high-frequency noises to prevent damaging the vulnerable logical gates. The filtered signal is then delivered to the operational amplifiers circuit. In this particular case, two LM-7171 high-speed operational amplifiers were used in the differential configuration. The purpose of this stage is to separate the measuring signal into two independent measuring paths and to add the offset to both of them. Two measurement paths are the reason to have independent signal loops for sensing $t_1$ and $t_2$ (see Figure 2).

The outputs of the amplifiers are connected to low-propagation delay comparators, TLV3501 (4.5 ns), with the reference voltages $V_{ref1}$ and $V_{ref2}$. Values of $V_{ref1}$ and $V_{ref2}$ were obtained based on the datasheet of the device (switching speeds and $L_s = 15 \text{ nH}$). Note that these parameters may differ and the driver applied for different modules may need additional tuning. For the considered CAS300M17BM2, approximate maximum and minimum values of $V_{Ls}$ should be in the range $\pm 7.8 \text{ V}$ for $R_G = 20 \Omega$. However, this value is too high to be provided for the TLV3501 comparators ($0/5 \text{ V}$). Operational amplifiers suppressed this voltage and added offset, meaning that their output signals have maximum values of 5 V and minimum values of 0 V. It means that in steady state, where the device is not switching, the outputs of the amplifiers are 2.5 V. Thus, $V_{ref1}$ has a value of 2.5 V + 10%
of 2.5 V, which is 2.75 V, and its role is to identify when \( i_D \) starts to rise during the turn-on cycle. The 10% tolerance secures it from any inappropriate disturbances that could cause switching of the comparator due to the parasitic in the device. On other hand, the \( V_{\text{ref2}} \) role is to sense moment \( t_2 \) (see Figure 2). The value of this reference voltage was set to 4 V after approximated calculations of the expected \( V_{LS} \) value. \( t_2 \) is sensed based on the change in the operational amplifier output from a value above 2.5 to below 2.5 V, which corresponds to the \( V_{LS} \) change from positive to negative voltages. Comparators are responsible for sensing the \( t_1 \) and \( t_2 \) time moments (see Figure 2) of the \( V_{GG} \) voltage modification. Thus, one of the comparators detects the drain current rising moment \( t_1 \) which corresponds to \( V_{GG} \) depletion from 30 to 15 V. The role of the second comparator is to sense when \( i_D \) starts to fall, which is caused by the overshoot of current \( i_D \) at \( t_2 \) and it is responsible for the \( V_{GG} \) increase from 15 to 30 V. Since voltage \( V_{LS} \) represents the dynamics of the drain current \( V_{\text{ref1}} \) and \( V_{\text{ref2}} \) can be set to persistent values, the comparator answering to sense the \( t_2 \) role is not to define the exact value of \( V_{LS} \), but rather to sense the moment when \( di_D/dt \) begins to reach a negative value (see Figure 2). Subsequently, the signal is provided to the logical gate circuit and then connected to an X4340 high-speed driver. The logical subcircuit is based on high-speed logical gates, which are responsible for detecting the rising edge of the comparators’ outputs and for protecting the \( V_{GG} \) switching sequence. The purpose of that is so that \( V_{GG} \) would not set inappropriate values at unsuitable moments of the turn-on cycle. It is shown as a block to make the diagram more simplified and clearer. X4340 handles switching the voltage from 15 to 30 V dependently on the logical signal on its input with a low propagation delay. Voltage levels 15/−5 V are supplied by isolated DC/DC converters, MGJD241505. The supply voltage of 30 V is provided from the boost DC/DC converter TP61175. The last part of the circuit is the IXDN630 current amplifier whose role is to turn on or turn off the device according to the value of the \( DS \) signal. The gate resistance \( R_G \) of the AGD was constant and equal to 20 Ω. Summary propagation delays of the used components were calculated from the data provided from the manufacturers. The response times of the AGD were under consideration during the design stage of the research, in correspondence with the turn-on time of the studied SiC MOSFET. Even with the low switching period of the chosen device components, the AGD operated properly.

![Figure 6. Simplified diagram of the AGD.](image-url)
A photo of the designed AGD with the detailed marks of its visible components is shown in Figure 7. The AGD was optically isolated from the logical signal $DS$ using HFBR-2531 optical receivers. As it can be noticed, the AGD consists of two connected PCBs (Printed Circuit Boards). The role of the first two-layer PCB (blue) is to provide a power supply to all integrated circuits of the device, switch the voltage from 15 to 30 V and amplify the logical signal $DS$. The second subcircuit of the AGD is a four-layer PCB (black), and it is directly connected to the power source of the $T_2$ MOSFET. Filtering, conditioning and logical circuits were placed onto this board of the AGD. The main purpose of that was to suppress any disturbances in the $V_{LS}$ measurements.

![Figure 7. Photo of the designed AGD. 1—filtering and logical signal board (AGD input), 2—DC/DC boost converter 15/30 V, 3—isolated power supply, 4—optical receivers HFBR 2531-Z, 5—output of the AGD.](image)

The experimental setup with a half-bridge module (CAS300M17BM2) and a suitable inductor ($L = 110 \, \mu H$) connected in the DPT circuit is presented in Figure 8. Both the CGD and AGD were controlled by a microcontroller (uC) unit. Measurements were made using a Tektronix MSO56 scope with differential medium-voltage probes (P5205A) with a measurement tolerance of $\pm 2\%$ and a Rogowski coil (CWTMini HF3B) with a tolerance of $\pm 2\%$. Delay times of the probes were calculated from the datasheets and were further included in the measurements to provide correct results. The AGD and CGD were compared in the same experimental conditions. Thus, the tolerances of the used probes can be omitted when both devices are compared. The drain current $i_D$, drain-source voltage $v_{DS}$ and positive bus of the $V_{GG}$ voltage were measured. A 2 kV DC power supply was provided by a Magna Power TSD 2000-22.5/380 with the output connected in parallel to the energy storage ($C = 150 \, \mu F$). Next, Figure 9 presents the photo of the experimental setup in the DPT configuration during experiments.
Figure 8. Experimental setup of the DPT with a medium-voltage (MV) SiC MOSFET CAS300M17BM2 module.

Figure 9. Photo of the experimental setup. 1—CAS300M17BM2 module, 2—DC bus and blocking capacitors.

The first test was conducted with the CGD—Figure 10 ($V_{DD} = 700$ V, $I_0 = 270$ A) presents the turn-on cycle for a standard gate voltage of $V_{GG} = 15$ V. After the drain current overshoot, continuous, weakly damped oscillations can be observed, and they are continued after the end of the turn-on process where the impact on the drain-source voltage is also visible. The voltage fall time is slightly above 300 ns. Comparing it to the same turn-on cycle from Figure 11, the impact of the AGD on $i_D$ and $v_{DS}$ can be noticed. As expected, the AGD increased the speed of the $v_{DS}$ voltage decrease (<200 ns) and shortened the cycle without causing any negative effects on the transient. Individual influences of the AGD on the $di_D/dt$ and $dv_{DS}/dt$ ratios and drain current oscillations are marked on the waveforms.
Presented in the following Figure 12 ($V_{DD} = 900\, V$, $I_0 = 270\, A$). The shown voltage $V_{GG+}$ is the positive rail of the gate driver and, as it can be seen, the switching from a value of 15 to 30 V was obtained in proper moments of the cycle. The first decrease in the $V_{GG}$ voltage was delayed on purpose to increase the $di_D/dt$ ratio which occurs in the turn-on energy depletion without $i_D$ overshoot in crucial moments. The AGD had the most visible impact on the $dv_{DS}/dt$ ratio, decreasing ipso facto the falling time of $v_{DS}$. Moreover, the AGD delay between the ideal point of the switching $V_{GG+}$ voltage can be noticed in Figure 12. In addition, the response time of the AGD can be noticed, which is visible as a result of the summary delays of used electronic components and filtering subcircuits. Comparing both obtained waveforms for the AGD, the damping of the drain current oscillations is greater in the case with $V_{DD} = 900\, V$, contrary to the case with $V_{DD} = 700\, V$. However, in both shown AGD cases, the impact on the drain current oscillations can be seen.

![Figure 10](image1.jpg)

**Figure 10.** The turn-on cycle of the SiC MOSFET from module CAS300M17BM2 with CGD. $V_{DD} = 700\, V$, $I_0 = 270\, A$.

![Figure 11](image2.jpg)

**Figure 11.** The turn-on cycle of the SiC MOSFET from module CAS300M17BM2 with AGD. $V_{DD} = 700\, V$, $I_0 = 270\, A$. 
Figure 12. The turn-on cycle of the SiC MOSFET from module CAS300M17BM2 using AGD with the $V_{GG+}$ voltage waveform. $V_{DD} = 900$ V, $I_0 = 270$ A.

In summary, the experimental measurements of the turn-on energy $E_{on}$ of the AGD and CGD in the same switching conditions ($V_{DD}$, $I_0$ and probes’ tolerances) are shown in Table 2. The turn-on energy of the CAS300M17BM2 MV SiC MOSFET using the AGD was decreased in all of the measured conditions compared to the CGD. The turn-on energy was decreased even by 10.1%, with an average of 7% for all measured turn-on energies. Comparisons of the obtained results from experimental and simulation studies are presented in Figure 13.

Table 2. The turn-on energy losses of AGD and CGD comparisons from the experimental test.

| $V_{DD}$  | $I_0$    | $E_{on}$ CGD | $E_{on}$ AGD |
|-----------|----------|--------------|--------------|
| 700 (±14) V | 170 (±3.4) A  | 23.5 (±0.94) mJ | 21.5 (±0.86) mJ |
| 700 (±14) V | 270 (±5.4) A  | 37.9 (±1.52) mJ | 36.0 (±1.44) mJ |
| 900 (±18) V | 170 (±3.4) A  | 32.3 (±1.29) mJ | 29.0 (±1.16) mJ |
| 900 (±18) V | 270 (±5.4) A  | 53.9 (±2.16) mJ | 50.0 (±2.0) mJ |

Figure 13. Chart of the turn-on energy for CGD and AGD both in experimental and simulation conditions. 1—$V_{DD} = 700$ V, $I_0 = 170$ A, 2—$V_{DD} = 700$ V, $I_0 = 270$ A, 3—$V_{DD} = 900$ V, $I_0 = 170$ A, and 4—$V_{DD} = 900$ V, $I_0 = 270$ A.
5. Conclusions

In this paper, an AGD for a 1.7 kV/325A SiC MOSFET power module was proposed and validated via simulations and experiments. A mix of multi-level gate voltage and proper measurements of the voltage across the parasitic source inductance proved a positive impact on the turn-on process of the transistor. The AGD was able to deplete the turn-on energy of the power SiC MOSFET by 7% on average and shorten the turn-on cycle without interference in the main circuit. Furthermore, experimental validation showed a higher $dvds/dt$ rate and, subsequently, measurements confirmed that the chosen method has no negative effect on the drain current oscillations and even suppresses them. Moreover, the device shown in this paper was designed based on off-the-shelf integrated circuits, which makes it a low-cost solution. Additionally, due to use of an integrated boost converter, the AGD needs only one level of the positive supply voltage (15 V) which leads it to be less complex in terms of structure. Finally, the proposed driver can also be used in other models of MV SiC MOSFETs where the Kelvin source and the power source of the device are provided. Further research in the case of turn-off cycle improvement with the shown methods is under consideration.

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