Expressing Sparse Matrix Computations for Productive Performance on Spatial Architectures

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Abstract
This paper addresses spatial programming of sparse matrix computations for productive performance. The challenge is how to express an irregular computation and its optimizations in a regular way.

A sparse matrix has (non-zero) values and a structure. In this paper, we propose to classify the implementations of a computation on a sparse matrix into two categories: (1) structure-driven, or top-down, approach, which traverses the structure with given row and column indices and locates the corresponding values, and (2) values-driven, or bottom-up, approach, which loads and processes the values in parallel streams, and decodes the structure for the values’ corresponding row and column indices.

On a spatial architecture like FPGAs, the values-driven approach is the norm. We show how to express a sparse matrix computation and its optimizations for a values-driven implementation. A compiler automatically synthesizes a code to decode the structure. In this way, programmers focus on optimizing the processing of the values, using familiar optimizations for dense matrices, while leaving the complex, irregular structure traversal to an automatic compiler.

We also attempt to regularize the optimizations of the reduction for a dynamic number of values, which is common in a sparse matrix computation.

1. Introduction
This paper addresses high-performance high-productivity programming of sparse matrix computations on spatial architectures like FPGAs. Such computations are usually considered irregular in terms of memory access patterns and parallelism, etc. For productive performance, however, we should hide the irregularity and express the computations and their optimizations in a regular way. How to do so remains an open problem. There have been some efforts on CPUs [2][11], but no work has ever been done on spatial architectures, as far as we know.

A sparse matrix is a 2-dimensional storage with a lot of zeros in it. This storage is a unique dense representation, where every datum, zero or not, is stored, and is located by a unique row and column index.

However, a sparse matrix can have many sparse representations. A sparse representation has values and a structure, where the values include all the non-zeros, and the structure is a mapping from the row and column indices to the values. Popular sparse representations include CSR (Compressed Sparse Row), CSC (Compressed Sparse Column), and their blocked versions, etc [1][2].

Fig. 1 illustrates a few representations of a sparse matrix. Fig. 1(a) shows its dense representation. Fig. 1(b) is a sparse representation in a tree, where every dimension corresponds to a tree level, and the values are located at the leaf nodes. This is the way proposed in The Tensor Algebra Compiler (TACO) [11]. This tree representation is equivalent to a CSR representation(Fig. 1(c)).

In this paper, we propose to classify the implementations of a computation on a sparse matrix into two categories:

- Structure-driven, or top-down, approach, which traverses the structure with given row and column indices, and locates the corresponding values.

Take sparse-matrix dense-vector multiply (SpMV), an important kernel in sparse linear algebra, for example:

\[ y(i) = \sum_{\forall j, A(i, j) \neq 0} A(i, j) \cdot x(j), \quad (1) \]

Here \( y \) and \( x \) are dense column vectors, \( A \) is a sparse matrix, and \( A(i, j) \) refers to the value of matrix \( A \) with row index \( i \) and column index \( j \). In order to realize the computation, the structure of matrix \( A \) is traversed, and the corresponding values are located and loaded.

For the tree representation in Fig. 1(b), the tree is traversed top-down until a value is reached at the bottom. This structure-driven approach is commonly seen in CPU implementations [11] and sometimes on GPUs [6].

- Values-driven, or bottom-up, approach, which loads and processes the values in parallel streams, aiming to

1In TACO, a tree is used to conceptually illustrate how a tensor can be represented. The physical representation is in dense vectors. A tensor is a generalization of a matrix to higher dimensions.
maximize memory bandwidth, data locality and parallelism. The structure is decoded to locate the indices of the values $[7, 19, 9, 3, 4]$. The decoding of the structure is bottom-up: if we take the tree representation in Fig. 1(b) again, for a value, we need traverse the tree bottom-up so as to determine the indices of a value.

This values-driven approach particularly suits a spatial architecture: the key to get high performance there is to stream values in and consume the values in massive parallelism. It would be cumbersome if a structure has to be decoded first in order to load values.

For our purpose of high-performance high-productivity spatial programming, we need productively express values-driven implementations. As we said, a sparse matrix computation like that in Equation (3) is suitable for a structure-driven implementation. How could we re-express the computation to make it amenable to a values-driven implementation, instead?

We observe that a sparse matrix can be represented by a series of invertible transformations, including but not limited to, packing, blocking, and job scheduling. Packing puts the non-zeros of the matrix together along the rows or columns of the matrix. Blocking divides the non-zeros into blocks. Job scheduling schedules the non-zeros, in rows, columns, or blocks, as jobs to some “machines”, which are hardware units with identical logic and will process the non-zeros in parallel.

These transformations must be invertible: their resulting structure must encode the original row and column indices in some way so that the one-to-one correspondence between a value and its indices is still maintained.

Fig. 2 illustrates the observation with the same sparse matrix in Fig. 1. Starting from the dense representation, first pack the non-zeros in each row together, and we get the CSR sparse representation. Then we schedule the rows to 2 “machines” in ASAP (As Soon As Possible) policy, resulting another representation called CISR (Condensed Interleaved Sparse Representation). Because the job scheduling scheduled the jobs to 2 machines, in this final representation, there are 2 rows of values. The first (second) row of the values, along with related structure information, will be fed to the first (second) machine. Each machine accepts its inputs as a stream and processes the stream independently. This is essentially the SpMV design proposed by Fowers, et al. [7], where the machines processes the streams by multiply-add.

This is the first time that job scheduling is proposed as a primitive transformation for representing a sparse matrix: since we target a spatial architecture that allow many hardware units (i.e. machines) with the exactly the same circuit to perform computation in parallel, scheduling values to the machines is a natural abstraction.

The transformations can be applied more than once, but the last transformation should always be a job scheduling, for the same reason stated above. This last job scheduling gives a value two new indices: a machine identifier $i'$, and the position $j'$ of a value within the stream scheduled to that machine.

From now on, we will use $i$ and $j$ to represent the row and column index of a value in the dense representation, respectively, and $i'$ and $j'$ to represent the new indices in the final sparse representation, respectively. The two pairs of indices are 1-1 corresponding to each other. We call the mapping from $(i, j)$ to $(i', j')$ the forward mapping, and the mapping from $(i', j')$ to $(i, j)$ the inverse mapping.
With the inverse mapping, we can re-express a sparse matrix computation, e.g. SpMV in Equation[1], as follows:
\[ y((i', j') \rightarrow i) = \sum_{i', j'} A.\text{values}(i', j') \cdot x((i', j') \rightarrow j). \]  
(2)

Here \( A.\text{values}(i', j') \) represents the \( j'' \)th value to be processed by machine \( i' \), and \((i', j') \rightarrow i \) and \((i', j') \rightarrow j \) are the inverse mapping. For each machine \( i' \), we may increment \( j' \) so that effectively, each machine is loading a stream of data, without accessing the structure of the matrix. This is exactly what a high-performance implementation on a spatial hardware would behave. Therefore, the above equation enables a computation to be driven by values.

Remember that \( A.\text{values}, x \) and \( y \) are all densely stored. Thus one may apply the familiar dense-matrix/vector optimizations, such as tiling, unrolling, etc., in optimizing the computation in Equation[2].

The inverse mapping, \((i', j') \rightarrow i \) and \((i', j') \rightarrow j \), may be automatically generated by a compiler by inverting the high-level transformations used for a sparse representation like packing, etc. Usually, a traversal of a structure for either the forward mapping or the inverse mapping would require code to be written in an imperative language with complex array indirections and control flow, which is especially complicated when processing many values in parallel. The diverse representations a sparse matrix might have further increase the complexity. Now that the complex, irregular structure traversal is automatically handled by a compiler, programmers can be more productive and focus on optimizing the processing of values instead.

In this paper, we further propose how to regularize and optimize a reduction with dynamic number of values, which is common in a sparse matrix computation. We show how to partition a reduction into two levels of reductions, and specify useful properties that help a compiler to generate efficient reduction circuits.

Fig. 3 summarizes our approach how to, in general, efficiently implement a sparse matrix computation on a spatial hardware. Starting from the dense representation of the sparse matrix, a programmer specifies a sparse representation as a forward mapping, using a series of high-level transformations, including packing, blocking, and job scheduling, etc. A compiler automatically constructs an inverse mapping. The programmer specifies the optimizations of the matrix so that the values and the inverse mapping are fed into the machines that the last job scheduling targeted. Between the machines, there might be interactions, for example, reduction. Finally, the program specifies the results of the computation to be stored back to the external memory of the spatial architecture.

Our language is named T2S (Temporal To Spatial), which is an extension of the Halide language [14] to spatial architectures. Previously, we have proposed T2S in the context of dense matrices [15], where a sparse matrix cannot be directly represented unless it is pre-processed into a dense matrix on the host, and for an inverse-mapping, an external function written in an imperative language has to be introduced.

In this paper, we show how to further extend T2S to express and process sparse matrices directly. To the best of our knowledge, this is the first time a sparse computation can be specified in a productivity programming language so that its optimizations can also be specified in a way much like for a dense matrix computation.

Below we introduce the language extension of T2S for sparse matrices, and illustrate the approach with two high-performance SpMV designs on FPGAs. We skip a detailed description of the T2S language but introduce it briefly when explaining the examples. Then we discuss related work, point out future directions, and conclude the paper.

2. Language

We extend T2S in two aspects for sparse matrices. One aspect is how to specify forward and inverse mapping, the other is how to specify optimizations of reductions. The other optimizations like tiling, unrolling, buffering, etc. are the same as for dense matrices.

2.1 Forward and Inverse Mapping

We explicitly express a sparse matrix as the result of a series of invertible transformations. For example, the following specification expresses an input matrix \( A \) in CSR sparse representation:

1 Representation CSR;
2 Parameter \( A(\text{float}, 2, \text{CSR}); \)
3 Var col_idx;
4 CSR = \( A.\text{dense}() \)
5 .pack(Columns, Index(col_idx));

Here Line 1 declares a representation named CSR, but exactly what it is is not defined yet. Line 2 says that input parameter \( A \) is a 2-dimensional floating-point matrix in CSR representation. Line 3 declares a variable \( \text{col}_\text{idx} \), which will be used to refer to the column indices in the CSR representation. Then we define CSR: starting from the matrix’s dense representation (Line 4), pack the non-zeros along the column dimension (Line 5). The packed dimension is represented sparsely based on indices, referred to by the pre-declared variable \( \text{col}_\text{idx} \), which gives us a handle to access the indices later.

As illustrated in Fig. 1, the sparse representation of a sparse matrix can continuously evolve. Continue with the above example. There can be a subsequent statement

6 Representation CISR = \( A.\text{schedule}(\text{Rows}, 4, \text{ASAP, Zero}); \)

This statement further schedules the rows of matrix \( A \) to 4 machines in the ASAP policy, and pads the machines with zeros at the end if needed, so that every machine has the same number of values to process. At this moment, all we
need is only the total number of machines. Exactly how a machine behaves can be defined later.
Below we define the language elements:

- **Representation r**
  Declare a representation named as r.

- **Parameter matrix(type, total dimensions, r)**
  Declare an input matrix with the given type, number of dimensions, and representation r.

- **matrix.dense()**
  The dense representation of the sparse matrix.

- **matrix.pack(d, r)**
  Pack the matrix along dimension d, which is either Rows or Columns. The resulting representation r can be index-based, i.e. Index(idx), or with a length as well, i.e. Index(idx), Length(len), where idx and len are variables recording the indices and length of the values along the packed dimension.

- **matrix.block(d, f, padding policy, r)**
  Block dimension d with factor f, with the given padding policy. The resulting representation r is Length(b), where b is a variable for the number of blocks along the dimension.

- **matrix.schedule(d, m, scheduling policy, padding policy)**
  Schedule dimension d to m number of machines, with a given scheduling policy. At the end, balance the machines’ workloads in a given padding policy.

- **matrix.values(i′, j′)**
  After the above job scheduling, access one value of the sparse matrix by the machine identifier i′ and the position j′ of the value within the stream scheduled to machine i′.

- **matrix.inverse_map(i′, j′)**
  After the above job scheduling, for a value scheduled to machine i′ at position j′, return an expression that represent the row and column index in the corresponding dense representation of the sparse matrix. Let that expression be e, we can extract the row and column index by e[0] and e[1], respectively.

- **Func.load_structure(var1, var2, ...)**
  Load the structure information specifically referred to by var1, var2, ... These variables are those used in pack and block above.

2.2 Reduction

Reduction is a very common computation for sparse matrices. Unlike a reduction for a dense matrix or vector, one reduction for a sparse matrix usually has dynamic number of input values.

In this section, we will use the following conceptual example:

\[
y((i', j') \rightarrow i) = \text{initial value};
\]

\[
y((i', j') \rightarrow i) += f(A.values(i', j'));
\]

where f is an arbitrary function. The above two definitions of y, respectively, are an initial definition, directly referred to as y in a specification, and an update definition, referred to as y.update() in a specification.

Usually, it is unknown to the compiler how many \((i', j')\)'s are mapped to the same i, and whether these \((i', j')\)'s appear next to each other to a machine. To help compiler generate efficient reduction circuit, we can specify if the \((i', j')\)'s that are mapped to the same i appear continuously to a machine, and the maximum number of \((i', j')\)'s that are mapped to the same i to a machine. Further, if the number of \((i', j')\)'s that are mapped to the same i must be a multiple of some integer number, we can block these \((i', j')\)'s: reduce the corresponding values in each block to a local sum, then reduce the local sums of the blocks. This two-level reduction provides more optimization opportunities: the two reduction circuits can be optimized differently.

If several machines with different i' reduce to the same y(i), we may combine their reduction results and write into y(i) only once.

Below we describe the language features:

- **f.is_continuous_reduction(1)**
  For a specific iteration of loop 1 in function f, the function reduces to the same result location continuously before the function reduces to another result location.

- **f.is_distinct_reduction(1)**
  For two different iterations of loop 1 in function f, the function reduces to different result locations.

- **f.isolate_reduction(F)**
  Isolate out of function f the reduction of values into a separate function F. This creates a two-level reduction: F reduces the values, and f reduces the results of F.

For the above example, we can isolate out a new reduction Y in the following specification:

\[
\text{Func } Y;
\]
reduction(l, target info)

This produces the following:

\[
Y((i', j') \rightarrow i) = 0;
Y((i', j') \rightarrow i) += f(A.values(i', j'));
\]

\[
y(i) = \text{initial value};
\]

\[
y(i) += Y(i);
\]

Basically, \( Y(i) \) is a local sum. For the same \( i \), \( Y \) might reduce several values and send the local sum to \( y \), and then do the same for the next several values, and so on. Every time \( Y \) needs to send \( y \) a local sum, it also sends the current \( i \) to tell exactly which \( y(i) \) to reduce this local sum for. The sending of \( i \) can be added automatically by a compiler.

- \( f \).combine_reduction(l, target info)
  - Combine all the reductions of all the iterations of loop \( l \) into a single reduction with additional target information, which can be Same_Target or Maybe_different_Targets.

For the example at the beginning of Section 2.2, we can combine the reductions of the iterations of loop \( i' \) into a single reduction:

\[
y.update().combine_reduction(i', 
  \quad \text{Same}_\text{Targets});
\]

This transforms the original loop nest of the update definition of function \( y \):

\[
\begin{align*}
\text{for } & j' \\
\text{for } & i' \\
& y((i', j') \rightarrow i) += f(A.values(i', j'));
\end{align*}
\]

into the following:

\[
\begin{align*}
\text{for } & j' \\
& \quad \text{sum } = 0 \\
& \quad \text{for } i' \\
& \quad \quad \text{sum } += f(A.values(i', j'));
\end{align*}
\]

\[
y((0, j') \rightarrow i) = \text{sum};
\]

If, however, we specify

\[
y.update().combine_reduction(i', 
  \quad \text{Maybe}_\text{Different}_\text{Targets});
\]

the original loop nest will be transformed into the following instead:

\[
\begin{align*}
& \text{for } j' \\
& \quad \text{sum } = 0 \\
& \quad (0, j') \rightarrow \text{current}_i \\
& \quad \text{for } i' \\
& \quad \quad (i', j') \rightarrow i \\
& \quad \quad \text{if } (\text{current}_i == i) \\
& \quad \quad \quad \text{sum } += f(A.values(i', j'));
\end{align*}
\]

\[
\text{else} \\
\quad y(\text{current}_i) = \text{sum};
\]

\[
\text{sum } = f(A.values(i', j'));
\]

\[
\text{current}_i = i
\]

\[
y(\text{current}_i) = \text{sum};
\]

- \( f \).reduction_circuit(circuit structure, l)
  - The reduction function \( f \) is implemented in a circuit with a given structure, including Tree and Linear_Array. Usually, the reduction structure reduces the inputs level by level. The maximum number of levels in the circuit structure is \( l \).

3. Case Studies

In this section, we illustrate our approach with two high-performance designs of SpMV on FPGAs.

3.1 SpMV on an FPGA with High Memory Bandwidth

In an implementation of SpMV on an FPGA for the above Equation 2, \( j' \) is incremented by 1 every time such that the values for the same \( i' \) are loaded from memory into an FPGA sequentially, forming a stream. And several streams for different \( i' \)'s are formed in parallel. The final result, vector \( y \), is stored back to the memory also as a stream. This implementation is focusing on the values, and can be very efficient for spatial architectures with high memory bandwidth.

Fig. 4 illustrates the implementation. Starting from the dense representation of a sparse matrix, pack together all non-zeros in each row, we get the CSR sparse representation. Let us say the target FPGA has 4 memory channels. We would like the matrix to be read from the 4 memory channels in parallel for the maximal memory bandwidth. If we treat the 4 memory channels as 4 “machines”, and the compressed sparse rows as “jobs”, we can schedule the jobs one by one to the machines: a job is scheduled to the earliest available machine; the last job for a machine may be padded with zeros so that all the machines have the same number of values to process. The resulting sparse presentation is CISR [7]. A similar but trivial example has been described in Section 1 before.

Now with the CISR sparse representation, every memory channel of the FPGA can read the rows scheduled to it as a sequential stream, and all the memory channels read their streams in parallel. More specifically, this is done by a hardware unit, i.e. 4 _A_loaders_, in Fig. 4. The loaded contents include row lengths, column index \( j \) and values. A decoder figures out the row index \( i \) from the row lengths to each _A_loader_. This decoder is realizing an inverse mapping \( (i', j') \rightarrow i \) based on the row lengths. Vector \( x \) and \( y \) are buffered on the FPGA. Vector \( x \) is loaded into its buffer with _x_loader_ in the figure. Using the row index \( i \) and column index \( j \), \( x(j) \) and \( y(i) \) can be easily retrieved. Now all the necessary information are available for SpMV defined in Equation 2. The computation is straightforward: 4 multipliers work in parallel to compute 4 different _A.values(i', j') * x(j)_. The products are reduced.
by, say 2, adders. Each adder processes two streams alternatively. Finally, the resulting vector \( y \) is stored back to memory by a hardware unit, \( y_{\text{unloader}} \), in the figure.

Note that the entire hardware in the figure is a regular dataflow graph. All the hardware units are purely functional. The only exception is the decoder, which is stateful and the output of it depends on its previous output. Because it is not really functional, usually, one might have to write it in an imperative language, not a functional language. In our approach, however, a compiler should automatically generate such a decoder, i.e. generate the hardware for the inverse mapping \( (i', j') \rightarrow i \), automatically connecting the hardware with other hardware units in the figure based on the producer-consumer relationship.

Fig. 5 shows the T2S specification. There are 3 parts: sparse representation, temporal definition, and spatial mapping.

The sparse representation (Line 1-6) defines the sparse representation of the input matrix \( A \) as a series of transformations. Line 1 declares a sparse representation called CISR. Line 2 says that \( A \) is a 2-dimensional floating-point matrix with CISR sparse representation, and \( x \) is a floating-point vector. Line 3 declares two variables to be used next. Line 4-6 actually defines the sparse representation: starting
from the dense representation of the sparse matrix, first, pack
the nonzeros along the column dimension for each row, and
record the total number and the column indices of the non-
zeros in each row (row_len and col_idx). Then schedule
the rows to 4 machines in ASAP policy with zero-padding at
the end if needed.

The temporal definition (Line 7-16) defines what to com-
pute. Line 10-11 defines the row and column index as two
expressions based on an inverse mapping (Line 9). The ma-
chine identifier i' is declared as normal variable (Line 7).
while the position j' of a value scheduled to a machine is a
reduction variable whose range is from 0 to the last column
of A.values.

Line 14 defines the SpMV computation, according to
Equation 2. The result vector y is initialized as 0 beforehand
in Line 13. We know that vector y is equally long as the input
vector x. Thus instead of calculating every i from an inverse
mapping, we can simply iterate i over the same range as
vector x to initialize each y(i) directly (Line 15).

Line 16 says that the machine identifier i' is from 0 to
4 (not included), as there are 4 machines. Further, the loops
are ordered such that loop i' is the inner loop, and loop j' is
the outer loop.

Line 17-22 isolate the computation in Line 14 into multi-
ple pieces. Line 18-19 first isolate the expression in the right-
hand side of Line 14 into a function named multiplier,
and then isolate the saving of the result vector y into an-
other function y.unloader. Further, Line 21 isolates from
the multiplier the loading of the values of matrix A to a func-
tion A_loader. Then Line 22 isolates from the multiplier the
loading of vector x into a function x_loader, which trans-
fers the loaded values to another function x_feeder, which
transfers the values to function multiplier.

Line 23-31 specialize each function. In addition to load-
ing the values of A, A_loader is also specified to load
the structure information row_len and col_idx (Line 23). Further, we unroll loop \(i'\) in A_loader, which creates 4 instances of A_loader (Line 24). Line 25 lets x_feeder buffers the x values in an on-chip scratchpad memory, whose size will be automatically calculated by the compiler.

Line 26 fully unrolls loop \(i'\) in multiplier to create 4 instances of it. Line 28 says that the reduction for \(y\) is continuous for each iteration of loop \(i'\), and is distinct for different iterations of loop \(i'\). Then Line 29 splits loop \(i'\) by a factor of 2, and fully unrolls the newly created loop \(i''\) to create two reduction circuits (i.e. the two fused accumulators in Fig. 4). Line 30 buffers the entire result vector \(y\) before sending any data of it out. Line 31 says that in sending out the data of the buffered results of \(y\), we can directly iterate \(i\) with the same range as the input vector \(x\), instead of computing \(i\) indirectly from the inverse mapping \((i', j') \rightarrow i\).

The inverse mapping is specified as A.inverse_map() in Line 9. The mapping should be realized by a compiler automatically to generate the decoder in Fig. 4.

### 3.2 Illustration: Another SpMV design on FPGAs [19]

This design is very different from the previous one in how the data are represented and processed. Fig. 6 illustrates this design. After packing the columns along each row of the dense representation, we get the CSR sparse representation.

Each machine computes the sum of a block. For this purpose, it uses \(k/2\) multipliers, each for one of the values in the block. Each multiplier gets the values and their column indices from another hardware unit, A_loader. With a column index, the multiplier reads a value of \(x\) from a buffer, which was filled beforehand by a hardware unit, x_loader. Now with a value from the matrix \(A\) and the corresponding value from the vector, the multiplier can compute their product. For all the multipliers in the same machine, their results are added together in a tree of adders (For the particular case shown in Fig. 6 there is only 1 adder in the tree).

For the two machines, their corresponding blocks might be from the same row, or from two adjacent rows. A row_blocks_loader loads the structure information of the total blocks in each row, and sends the information to a decoder, which decides if the two blocks currently processed in the two machines belong to the same row or not. If yes, the decoder controls an adder to add together the two sums of the two blocks. Otherwise, the first sum is added with 0. The adder’s result and the row index is sent to a reduction circuit. The second sum and the corresponding row index is also sent to the reduction circuit but with some delay. The reduction circuit is accumulating the sums for all the blocks in the same row. It is composed of a linear arrays of small buffers and adders. With the row indices from the input, the reduction circuit knows when a row is completely reduced, and sends the results to another hardware unit, y_unloader, to save to memory.

Fig. 7 shows the T2S specification for the design. Line 1-8 describe the sparse representation of the input matrix \(A\). Line 2 says that \(A\) is a 2-dimensional floating-point sparse matrix in a representation called rep. How rep is defined? Starting from the dense representation of the matrix (Line 5), pack the non-zeros along the column dimension of each row and record the column indices of the non-zeros (col_idx) (Line 6). Then block the columns of each row into blocks with a length of \(k/2\) (Line 7), where \(k\) is a symbolic constant (Line 3). Then the last block with zeros if needed. The number of the blocks of a row is referred to by row_blocks. Finally, schedules the blocks to 2 machines in ASAP policy, padding the last machine with a zeroed block if needed (Line 8).

Line 9-18 defines the temporal computation. Not surprisingly, it is the same as the temporal definition in the previous example in Fig. 5 except the number of machines are changed from 4 to 2, the inner loop is \(j'\) and the out loop is \(i'\) (Line 18).

Line 19-27 builds a basic spatial layout. Line 20 isolates a y_unloader to store the final results of vector \(y\) to the external memory. Line 21 isolates the reduction of \(y\) so that the reduction is done in two levels: there is an additional reduction circuit \(Y\) to compute local sums at the first level, which are further reduced at the second level. Line 23 isolates out the loading of vector \(x\). Line 24 then unrolls loop \(i'\) to create 2 machines. Line 25-26 split loop \(j'\) by a factor of \(k/2\) and unroll the newly created loop \(j''\) so that each machine has \(k/2\) multipliers. Finally, Line 27 isolates the loading of matrix \(A\).

Line 28-35 specialize the individual computations. Line 28 buffers vector \(x\) for \(Y\). Then we combine the reductions in the same machine(Line 29). We also combine the results of the 2 machines, but they may be reduce to two different result locations (Line 30).

Line 31 says that the local sums sent from function \(Y\) to function \(y\) must be continuous for a row. The reduction circuit for function \(y\) is chosen to be implemented in a linear array with 4 levels.

In addition to loading of \(A\) values, A_loader also loads the structure information, col_idx (Line 33).

Line 34 declares a special function, row_block_loader, which is neither defined nor isolated. This is because it is to fetch a part of the sparse structure information, the number of blocks per row. We simply specify that functionality in Line 35.

The inverse mapping is specified as A.inverse_map() in Line 11. The mapping should be realized by a compiler automatically to generate the decoder in Fig. 6.
4. Related Work

We first discuss related work from the perspectives of implementing a sparse matrix computation, and then from the perspectives of languages.

4.1 Structure-Driven vs. Values-Driven Approach

In this paper, we classify algorithms for sparse matrix (or more generally, tensor) computations into two categories: the first is structure-driven, or top-down; the second is values-driven, or bottom-up.

Structure-driven algorithms are commonly seen for latency-oriented CPUs and sometimes for throughput-oriented GPUs. TACO \[11\] provides a unified and general way to represent all possible sparse tensors, including sparse matrices. Conceptually, every sparse tensor can be viewed as stored in a tree, with every tree level being a dense or sparse dimension of the tensor, and the leaves being the values of the tensor. The compiler will also automatically optimize the traversing of the structures of several related tensors. This traversal of the sparse structures is an efficient way of forward mapping, not the inverse mapping we propose in this paper. Thus the code generated by TACO is top-down, and is driven by structures.

In TACO, programmers control the representations of a sparse tensor, but have no control of subsequent optimizations so far. In contrast, we would like programmers have explicit control not only in the representations of sparse matrices, but also how to optimize them. Also we target FPGAs, while TACO targets CPUs so far.

Gustavson \[10\] proposed an algorithm for permuted transposition, and an algorithm for the multiplication of two sparse matrices (SpGEMM). Both algorithms follow the structure of a sparse matrix to get the values. Thus the algorithms are structure-driven. Based on Gustavson’s algorithm for SpGEMM, Deveci et al. \[6\] developed different parallel algorithms for portable performance across different CPUs and GPUs. They consider the trade-offs on parallelism (how to partition and parallelize a reduction across different compute units), how to determine the size of the result matrix, and efficient data structures of a reduction.

Values-driven approach seems to be the norm for sparse matrix computation on FPGAs. This is not surprising; due to the massive hardware parallelism of FPGAs, their slower frequencies relative to CPUs/GPUs, and their lack of hardware caches, a high-performance implementation on FPGAs would have to stream values in (maybe in several parallel streams) to avoid any random memory access, and process them in pipelines. Meanwhile, since FPGAs have abundant, programmable hardware resources, the implementation can use additional hardware resources to decode the structure of a sparse matrix for the indices of the values simultaneously.

Values-driven approach also appears in GPU implementations. Greathouse and Daga \[9\] map SpMV efficiently to a GPU by streaming the values of a sparse matrix into the local scratchpad memory of the GPU, and dynamically assigning rows to each parallel GPU compute unit. Bell et al. \[3\] show an SpGEMM algorithm based on COO (coordinate) representation. Bell and Garland \[4\] compare several SpMV implementations based on different representations including DIA (diagonal), ELL, CSR and COO. While there are no detailed algorithm descriptions, we believe their algorithms are driven by values, because they target to distribute fine-grain parallelism among thousands or tens of thousands of threads, which might be difficult for a structure-driven approach.

4.2 Languages

Our language, T2S, is an extension of Halide \[14\], a domain-specific language for image processing on CPUs/GPUs, to spatial architectures. Halide-HLS \[13\] is another spatial extension of Halide, where a dataflow graph of functions is specified to offload to an FPGA, with line buffers between functions to optimize their communication. As far as we know, sparse matrices are not expressible in the current Halide and Halide-HLS.

Spatial \[12\] is another domain-specific language for spatial architectures. Its syntax directly supports streaming, channels (i.e. pipes), reduction, finite state machine, loop parallelization, etc. There is no detail specific to sparse matrices, but it was evaluated with PageRank, a sparse matrix or graph algorithm. From its syntax, we believe that sparse matrices are not directly supported; instead, a values-driven approach might be implemented: the values of a sparse matrix may be streamed into a spatial hardware, and the structure of the matrix may be accessed with loops to build the inverse mapping. However, in this way, a programmer has to write in detail how to build the inverse mapping, while in our approach, we may have a compiler to automatically build it.

The Little Language (LL) \[2\] has also observed that a sparse matrix can be represented by a series of transformations. However, LL does not point out that the transformations are invertible, a simple yet critical fact that makes it possible for a compiler to automatically construct an inverse mapping. The usage of the LL language was for verification of sparse matrix codes, which is structure-driven. In addition, the transformations in LL have much lower abstraction level. For example, blocking and job-scheduling here would have to be expressed in other lower-level primitives in LL.

In our approach, we propose the transformations at a higher abstraction level in order to make it easy for a compiler to invert the transformations and automatically generate the inverse mapping, which is the key to enable a values-driven implementation.

5. Future Work

This paper is a first step to expressing and optimizing sparse matrix computations in a values-driven style on spatial architectures. There are many interesting questions left for future:
• **An algorithm for building an inverse mapping.** We reasonably assume that a compiler can automatically build an inverse mapping for a sparse matrix, as long as the matrix is represented in a series of invertible, high-level, transformations. In the next step, we will develop such a compiler algorithm.

• **Extension to sparse tensors.** While there are many (more than 50 in 2010 [2]) sparse representations for a sparse matrix, the possible representations for a sparse tensor can be overwhelming, since a sparse tensor can have many dimensions and any dimension can be dense or sparse. If a sparse tensor could be expressed in a similar way as a sparse matrix and for values-driven computations, programmers would be able to productively explore the design space, including not only the possible sparse tensor representations, but also their optimizations, for high performance.

• **More transformations.** While we have pointed out three high-level transformations, including packing, blocking, and job scheduling, it is possible to include more transformations to succinctly and precisely express the representations and optimizations of sparse matrices for various computations. There are known data parallel primitives that emerge in many computations [3][17], including reduction, scan (parallel prefix-sum), mapping, gathering, scattering, stream compaction, segmented reduction, and sorting [3]. They might be used as additional high-level transformations.

In this paper, the result of job scheduling is statically decidable with a sparse matrix. However, for GPUs and FPGAs, dynamic job scheduling is also common. It is useful if we could standardize dynamic job scheduling as a high-level transformation.

• **Optimizing across computations.** So far, we have focused on a single sparse matrix computation. In an iterative solver, there are multiple computations involved. Reordering [5][8] may improve data locality. Inspection/execution is a common strategy that examines the structures of sparse matrices, and transforms the computations at run-time for better performance. In our previous work [16], we have built a compiler and library to transparently optimize across computations with reordering and inspection/execution. Now that we can explicitly express a sparse representation, in future, we may leverage our previous work but further give programmers explicit control of reordering and inspection/execution.

• **More workloads and designs for FPGAs.** In this paper, we have studied two SpMV implementations on FPGAs, and from them extracted a general approach. We will study more workloads and their designs on FPGAs to validate and enrich this approach.

• **Workloads and designs for GPUs and CGRAs.** Similar to FPGAs, GPUs have massive resources and parallelism. CGRA (Coarse-Grain Reconfigurable Architecture) [18] is structurally similar to FPGAs except its resources have coarse granularity. It is interesting to see if our approach is applicable to workloads and designs on these architectures.

6. **Conclusion**

We have proposed a novel idea to productively expressing a sparse matrix for high-performance computing on a spatial architecture. We express the sparse representation of the matrix as a series of invertible transformations, and express the computation centering around values, aided by an inverse mapping automatically generated by a compiler. Then a programmer can specify optimizations of the computation in a way much like for a dense matrix computation.

This is a first step in addressing spatial programming of sparse matrix computations for productive performance. There are many interesting researches left for future.

**Acknowledgments**

The keen interest of Nitish Kumar Srivastava in sparse tensors has motivated me to think about the problem in this paper (productive, performant, spatial programming of sparse matrix computations). Zhiru Zhang, Nitish Kumar Srivastava, and Chris Hughes have provided valuable feedback on the solution.

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Schedule the blocks to 2 machines ASAP.

FPGA + y_unloader y(i)

buffer for x

buffer for x

buffer...

* 5

C F I L P

0 G J M

0

3 1 1 3 6

* 4 5 7 *

Conditionally combine reductions from two machines

Local sum and i

Machine 0

Machine 1

Combine reductions in the same machine

FPGA

Figure 6: Another SpMV design on FPGAs [19].
1 Representation rep;
2 Parameter A(float, 2, rep), x(float, 1);
3 Assumption symbolic_constants(k);
4 Var col_idx, row_blocks;
5 rep = A.dense()
6 .pack(Columns, Index(col_idx))
7 .block(Columns, k/2, Zero, Length(row_blocks))
8 .schedule(row_blocks, 2, ASAP, Zero);

9 Var i;
10 RDom j(0, A.values.extent(1));
11 Expr original_ij = A.inverse_map(i', j');
12 Expr i = original_ij[0];
13 Expr j = original_ij[1];
14 Func y;
15 y(i) = 0;
16 y(i) += A.values(i', j') * x(j); 
17 y.bound(i, 0, x.extent(0));
18 y.update().bound(i', 0, 2).reorder(j', i');

19 Func y_unloader, Y, x_loader, A_loader;
20 y.update().isolate_consumer(y, y_unloader)
21 .isolate_reduction(Y);
22 RDom j''(0, k/2);
23 Y.update().isolate_producer(x, x_loader)
24 .unroll(i')
25 .tile(j', j'', k/2)
26 .unroll(j'')
27 .isolate_producer(A, A_loader);

28 Y.update().buffer(x)
29 .combine_reduction(j'', Same_Target);
30 .combine_reduction(i', Maybe_Different_Target);
31 y.update().is_continuous_reduction(i)
32 .reduction_circuit(Linear_Array, 4);
33 A_loader.load_structure(col_idx);
34 Func row_blocks_loader;
35 row_blocks_loader.load_structure(row_blocks);

Figure 7: Specification for the SpMV design in Fig. 6