A fast X-ray detector using silicon avalanche photodiodes of 64-pixel linear array

S Kishimoto¹, H Yonemura¹, S Adachi¹, S Shimazaki², M Ikeno², M Saito², T Taniguchi² and M Tanaka²

¹Inst. of Materials Structure Science, High Energy Accelerator Research Organization, Oho 1-1, Tsukuba, 305-0801 Ibaraki, Japan
²Inst. of Particle and Nuclear Science, High Energy Accelerator Research Organization, Oho 1-1, Tsukuba, 305-0801 Ibaraki, Japan

E-mail: syunji.kishimoto@kek.jp

Abstract. We have developed a silicon avalanche-photodiode (Si-APD) array detector operated in the linear mode for time-resolved measurements using pulsed synchrotron X-rays. The Si-APD detector had 64 pixels of a linear array, where the pixel size was 100 μm by 200 μm with a 50-μm gap between pixels and a depleted thickness was 10 μm. A nanosecond response of the array detector is extremely valuable for time-resolved X-ray diffraction measurements in the multi-bunch mode operation of a 500M-Hz synchrotron ring. In order to apply the APD detector for the time-resolved diffraction measurements with 2-ns pulse-pair resolving time and a count rate of more than 10⁷ s⁻¹, an ultra fast ASIC has newly been developed for processing a nanosecond-width pulse from each pixel of the Si-APD array. A prototype system had a 10-ns time resolution and a high count-rate of more than 10⁷ s⁻¹/pixel in the first test measurement using synchrotron X-ray beam.

1. Introduction

We have developed a silicon avalanche photodiode (Si-APD) detector of 64-pixel linear array. The Si-APD operated in the linear mode provides a fast response of > 10⁸ s⁻¹ per one device and a good time resolution of sub-nanosecond by using fast pulse electronics and a time-to-amplitude converter as an X-ray detector [1]. A 100-μm order spatial resolution will be useful for the position-selective timing measurements. The nanosecond response of the array detector is extremely valuable for time-resolved X-ray diffraction measurements [2]. Synchrotron X-ray is a pulsed photon source generated by an accelerator and has the pulse interval decided by a n electron-filling pattern of the synchrotron ring. Our Photon Factory (PF) ring has the RF frequency of 500.1 MHz and the shortest X-ray pulse interval of ~2.0 ns in the multi-bunch mode [3]. If a detector system can count a pulse with each time interval of shorter than 2 ns, resolving a photon coming from a successive electron bunch, the detector system can be applied to a study for a laser-induced structure change of some molecules by recording a movie of X-ray diffraction images, without use of an electrical time gate. If adjusting a picosecond-order delay between a trigger signal and a signal caused by radiation from a sample, the 2-ns pulse-pair resolution will greatly improve efficiency of a measurement even in the picosecond time resolution without reducing input pulse rate.

We are now developing a linear array system of the Si-APD detector as the first step for a Si-APD pixel area detector. In order to take full advantage of the fast response of the Si-APD, development of an ultra-fast digital integrated circuit is essentially important. Here, we report on a prototype of 64-channel Si-APD linear array detector equipped with an ASIC frontend circuit and a digital system using conventional field programmable gate-arrays (FPGAs). As results of the first test measurement using the prototype, a count-rate of higher than 10⁷ s⁻¹ per pixel was obtained with 8-keV synchrotron X-ray beam. Due to use of a conventional FPGA, time resolution was limited to be 10 ns.
2. A linear array of Si-APD and a signal processing system

2.1. A 64-pixel linear array

We used an APD linear-array device of Hamamatsu S5343-9158, which had 64 pixels of 100 × 200 μm² with a 50-μm gap between pixels. The depletion layer was designed to be 10 μm thick. Sensitive area was 9.6 mm long and the capacitance of each pixel was 0.8-1.0 pF. The positive reverse-bias voltage was commonly applied to the n⁺-side of the APD device through a resistor and a capacitor mounted on a small circuit board. The output from each pixel was obtained from the p⁺-side of the Si-APD. Two micro-connectors, each of which had 37 contacts with a 0.30-mm interval, delivered the signals to a frontend board.

We investigated performance of pixels in the Si-APD linear array at beamline BL-14A of the PF ring. A fine X-ray beam of 8 keV was formed by a pinhole of 5 μm in diameter, which was made of iridium foil 50 μm thick. The beam diameter through the pinhole was 10 μm (FWHM) [4]. The intrinsic efficiency was measured at a bias voltage of +140 V using a charge-sensitive preamplifier (Canberra 2001A) at a gain of 17 ± 2 as 11% for 8-keV X-rays, which corresponded to absorption of 8-μm silicon. The relative difference of the efficiency between pixels was less than ±2%.

2.2. A frontend ASIC and a digital signal processing

As a frontend circuit of the linear array, an ultra-fast ASIC was designed by 0.8-μm BiCMOS process for processing a nanosecond-width pulse from each pixel of the Si-APD [5]. The frontend ASIC had four channels in 4×4 mm² and consisted of a preamplifier, a comparator, a current monitor, a feedback amplifier for baseline restoration, toggle flip-flops, and PECL drivers. The preamplifier gain was 5.5mV/fC. A threshold level of > 10 mV was commonly set externally by a potentiometer and was distributed to each of the comparators. A baseline restoration circuit, which was composed of a current monitor and a feedback amplifier, maintained the baseline of the preamplifier output level ~0 V from DC to 500MHz frequency. In order to adjust the maximum output frequency to that of CMOS circuits, outputs from the comparator were fed into two toggle flip-flops by reducing the output-frequency from 500MHz to 125MHz. The ASIC response was confirmed at input rates up to 540MHz using a pulse generator. A problem might be a large power consumption that reached 0.68 W per one ASIC chip [5]. After the frontend ASIC and the level converters from PECL to LV-CMOS, FPGAs (Xilinx Spartan3) were used to count pulses and to know a timing of the pulse with a duration along a series of 256 channels, where each channel had 36-bit counter-depth in the memory. The system can operate in the time course mode, which is a repetitive counting mode synchronized with a trigger input. We used a signal synchronized with a revolution of the storage ring as the trigger. Data of counts in the time course mode were acquired through the SiTCP that was a hardware-based TCP processor for Gigabit Ethernet [6]. The inside of the prototype detector is shown in a photograph of Fig. 1. Using a data acquisition program running on a Linux-based personal computer, we obtained X-ray counts of each pixel during a preset time between 2 μs and 4295 s. Counting data in the time course mode were available for each pixel as a series of 256 data with a time window of 10 ns to 167 ms width.
3. Test performance of the linear array system using synchrotron X-ray beam

3.1 Time-course counting with a 10-ns resolution at one pixel

Performance of each pixel of the detector was tested by the micro X-ray beam of 10-µm in diameter. The energy was 8 keV. After adjusting the detector position, counts just from one channel was measured in the time course mode. A bias voltage of > +150 V was applied to the Si-APD. Figure 2 shows the count distribution along time, obtained from channel 41. The time window was set to the minimum of 10 ns. As the electron-bunch filling consisted of four bunch-blocks of 126 ns plus 30-ns gap in the ring operation mode, gaps of 30 ns were observed in the count distribution with the 10-ns time resolution. A revolution period of 624 ns was just recorded in the data since a pulse having the revolution frequency from the RF cavity was used as the trigger signal of the detector system. The count-rate was about 1.0 k s⁻¹ at the pixel.

3.2 A beam profile without the pinhole obtained by scanning the linear array

By scanning a position of the detector itself, intensity profile of the X-ray beam without the pinhole was recorded. Figure 3 (a) shows a measured profile of 8-keV beam, roughly focused with a quasi-toroidal X-ray mirror, by scanning the detector position of every 0.1 mm along the vertical direction. The beam size was about 1 mm in diam. (FWHM). The measuring period was one second per position and an automatic stage mounting the detector was controlled, coinciding with a timing of data acquisition from the detector. Counts per channel of 1.2×10⁷ s⁻¹ were certainly recorded at channel 31, around the center of the linear array. Figure 3 (b) shows a time-course profile of the same X-ray beam. Similar to Fig. 2, the gap of 30 ns was seen in Fig. 3 (b). Unfortunately, since the beam intensity and the efficiency of the Si-APD array itself were not so high, they limited the maximum count-rate to be much less than 10⁸ s⁻¹. The efficiency obtained through each ASIC channel was limited to be low, about one third to one half of 11% measured with the charge-sensitive preamplifier.
The non-uniformity of the efficiency between channels reached ±50%. Since the non-uniformity between pixels was small of ±2% by the charge-sensitive preamplifier, as described in Section 2.1, the low efficiency and its large non-uniformity was probably due to a lack of gain in the ASIC preamplifier and due to a wide variation of threshold voltages at each comparator.

4. Conclusions
A Si-APD linear array detector was fabricated and tested for applications of the time-resolved diffraction experiments using pulsed synchrotron X-rays. The prototype had 64-pixel linear array of Si-APD. The outputs from each channel was processed by an ultra-fast frontend ASIC and a digital circuit using FPGAs. Data were acquired with the SiTCP through the Ethernet. The test results confirmed that the system had a 10-ns time resolution and a high count-rate of more than 10^7 s^-1. A frontend ASIC of the second version will be improved in the non-uniformity of the efficiency between the pixels. In the digital processing part, the next design will use a faster FPGA to obtain a 2-ns pulse-pair resolution.

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Figure 3. Beam profile of the mirror focused 8-keV X-rays: (a) count distribution obtained by scanning the detector position along the vertical direction and (b) count distribution in time course with each 10-ns time window.