B-DCGAN: Evaluation of Binarized DCGAN for FPGA

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Abstract. In this work, we demonstrate an implementation of Deep Convolution Generative Adversarial Network (DCGAN), into a Field Programmable Gate Array (FPGA). In order to implement the DCGAN, we modified the DCGAN model with binary weights and activations, and with using integer-valued operations in the forwarding path (train-time and run-time). We call the modified one as Binary-DCGAN (B-DCGAN) Using the B-DCGAN, we do a feasibility study of FPGA’s characteristics and performance for Deep Learning. Because the binarization and using integer-valued operation reduce the memory capacity and the number of the circuit gates, it is very effective for FPGA implementation. On the other hand, these reductions in the model might decrease the quality of the generated data. So we investigate the influence of these reductions.

1 Introduction

We try to implement a deep neural network in the edge computing environment for real-world applications such as the IoT (Internet of Things), the FinTech, to utilize the significant achievement of Deep Learning in recent years. Especially, we now focus on algorithm implementation on FPGA, because it is one of the promising devices for low-cost and low-power implementation in edge computing.

A well-known fact, Graphics Processing Unit (GPU) is now the most common computing resources for Deep Neural Networks (DNNs). GPU is one of the most useful devices to execute massive scale numerical operations such as DNNs. Furthermore, thanks to the effort of world-wide researchers and developers, now there are many software tools, libraries, and frameworks suitable for GPU, so it is easy to write the DNNs software for GPU. However, GPU has very high power consumption, so that it needs an abundant power supply and cooling equipment. Thus, it is hard to apply GPUs in the small edge machines for IoT.

As a way for low-power and low-cost dedicated computation, Field Programmable Gate Array (FPGA) is gathering attention recently again, since its cost performance has improved and the prices of related software tools have also declined.
While FPGA is user-programmable hardware, its development in the early times was pretty tricky and complicated, because the program requires ‘low-level’ notations such as Hardware Description Language(HDL) or schematic circuit diagrams, so the developers had to have these kinds of special skills.

However, nowadays, owing to the High-Level Synthesis(HLS) technique has been evolving, the developer programs the FPGA using a high-level programming language such as C/C++. It is a much easier way for the developer who is not an expert of hardware.

1.1 The Problem of Using FPGA for DNN

The algorithm development using FPGA has the following problems: First, the number of gates and the capacity of fast memory is much smaller than that of the GPU. While it is available to use either multi FPGAs, or FPGA with external memories, however, the processing speed will drop considerably because of the communication overheads. Second, the more the algorithm uses multiplication, division, or floating-point value of those operations, the much larger gates it will consume. Third, if the circuit is not optimized appropriately in the hardware-specific way, such as parallelizing or pipelining, the FPGA could get slower speed than a CPU with the same clock range.

As the solution for these problems, various researches make the circuit scale smaller for DNNs: Courbariaux et al. showed that image classification using the neural networks with binary weights and activations(BNN) is enough possible [4]. Moreover, they showed the method to train the BNN. Umuroglu et al. presented the FINN[9], a framework for building fast and flexible FPGA accelerators that enable efficient mapping of binarized neural networks to hardware. Adelouahab et al. published a good survey[1], which reports various types of implementation techniques of CNN on FPGA. Cheng et al. also published another good survey[3], in which they discussed the recent techniques for compacting and accelerating CNNs in detail.

1.2 Contributions

This work makes the following contributions:

– We introduce binarized & integer-valued deep convolutional conditional generative adversarial networks. Hereafter we call it as B-DCGAN.
– We show the quality change of output from B-DCGAN Generator when the extent of binarization was changed.

2 B-DCGAN: DCGAN With Binarized Generator

Binary Deep Convolutional & Conditional Generative Adversarial Networks(B-DCGAN) is a modified version of DCGAN [8]. In the B-DCGAN, the Discriminator network is a vanilla network as the normal DCGAN; that is, it uses real-valued operation. However, the Generator network adopts the binary weights, binary activations, and integer-valued operations.
2.1 Network Structure

Fig. 1 is a schematic diagram of the network structure of B-DCGAN Generator. The first half of the Generator is consist of full connection layers, which is called Encoder. The last half is named Decoder, is consist of deconvolution layers. We show the details of these layers in the following sections.

![Fig. 1. Schematic diagram of B-DCGAN Generator](image.png)

2.2 Integer-Valued Inputs

The Generator’s inputs are $z$ and $y$. In vanilla GAN, $z$ is 1D-vector of random floating point values in range $[-1.0 \sim +1.0]$. In B-DCGAN, we use integer value $z^i$ for input as follows:

$$z = (z_1, z_2, \cdots, z_n)$$  \hspace{1cm} (1)

$$z^i = (z^i_1, z^i_2, \cdots, z^i_n)$$  \hspace{1cm} (2)

$$z^i_k = \text{round}(A \cdot z_k) \hspace{0.5cm} (k = 1, 2, \cdots, n)$$  \hspace{1cm} (3)

$$A = 2^{h-1} - 1 \hspace{1cm} (h = 2, 3, 4, \cdots)$$  \hspace{1cm} (4)

The B-DCGAN treats the conditional input method like as CGAN[7]. The $y$ is one-hot vector representation of class label to be generated. It is also converted into integer value $y^i$:

$$y^i = A \cdot y = (y^i_1, y^i_2, \cdots, y^i_l, \cdots, y^i_c) \hspace{0.5cm} (l = 1, 2, \cdots, c),$$  \hspace{1cm} (5)

where the constant $A$ is a hyper-parameter of B-DCGAN. $z^i_k$ and $y^i_l$ is integer values represented by signed $k$ bits. The integer value is very advantageous from a hardware perspective because the number of circuit logics of integer process is much smaller than those of floating point in FPGA. We have investigated the influence of the value $A$ setting for quality of Generator’s output as we explain in Section 3.
2.3 Binarized Full Connection Layer (B-FC)

Implementation of Full Connection layer in B-DCGAN is based on those of BNN\cite{4}. During the backward pass (at train-time), its weight value is real-valued variable the same as the usual full connection. During the forward path calculation (both at run-time and train-time), we treat the weight as binary, that is, the value is constrained to either +1 or -1 as follows:

\[
x^b = \text{Sign}(x) = \begin{cases} 
+1, & \text{if } x \geq 0 \\
-1, & \text{otherwise}
\end{cases}
\]  

(6)

We have investigated the influence of this binarization for quality of Generator’s output as we explain in Section 3.

2.4 Binarized Batch Normalization + Activation Layer (B-BNA)

In our B-DCGAN structure, the batch normalization layer the non-linear activation layer, so we treat these two layers as one layer calculation. This consideration is based on the ‘Batchnorm-activation as Threshold’ in the FINN paper (Umuroglu et al. \cite{9}); that is, we have modified it as integer-valued version.

Let \(a_j\) is the output of \(j\)th neuron in the previous layer, and \(\Theta_j = (\gamma_j, \mu_j, \iota_j, B_j)\) is the batch normalization parameter set learned during the training phase. The output of this layer \(a_j^b\) in computed as:

\[
a_j^b = \begin{cases} 
+1, & \text{if } a_j \geq \tau_j^b \\
-1, & \text{otherwise}
\end{cases}
\]  

(7)

The threshold \(\tau_j^b\) is computed by solving \(\text{BatchNorm}(\tau_j, \Theta_j) = 0\) and rounding:

\[
\text{BatchNorm}(\tau_j, \Theta_j) = \gamma_j \cdot (\tau_j - \mu_j) \cdot \iota_j + B_j = 0 
\]  

(8)

\[
\therefore \tau_j = \mu_j - (B_j / (\gamma_j \cdot \iota_j)) 
\]  

(9)

\[
\tau_j^b = \text{round}(\tau_j) 
\]  

(10)

During the training phase, \(\tau_j^b\) value is always modified according to the change of \(\text{BatchNorm}\) parameters; however, in the run-time phase, the value can be treated as a fixed value.

2.5 Binarized Deconvolution Layer (B-Deconv)

The behavior of the binarized deconvolution layer (B-Deconv) is similar to those of the B-FC layer described at 2.3. That is, during the backward path calculation at the train-time, the weight values of filters are real-valued variable same as the normal deconvolution. However, in the forward path calculation both at the run-time and train-time, we treat the weight values as binarized to either +1 or -1 according to the equation (6).

We have also investigated the influence of using B-Deconv for output quality of the Generator (see 3.2).
3 Evaluation

3.1 Experimental Setup

**Scenario** To examine B-BDCGAN, we arranged several configurations of network binarization. We present a configuration as a set of flags and hyper-parameters described in Table 1. We call it ‘Scenario.’ The ‘Input as integer’ flag represents whether the input is integer-valued(Y) or real-valued(n). Other flags correspond with whether each layer is binarized(Y) or not(n). The ’A value’ is input scale value that is only effective when the ‘Input as integer’ is positive(Y), had explained in 2.2.

**Table 1.** Setup Scenario. ‘Y’ is positive, ‘n’ is negative.

| Scenario # | S0 | S1-1 | S1-2 | S2-1 | S2-2 | S3-1 | S3-2 |
|------------|----|------|------|------|------|------|------|
| Encoder    |    |      |      |      |      |      |      |
| Input as integer | n  | Y    | Y    | Y    | Y    | Y    | Y    |
| A value    | -  | 1    | 1    | 127  | 4095 | 1    | 1    |
| B-FC       | n  | Y    | Y    | Y    | Y    | Y    | Y    |
| B-BNA-1    | n  | n    | Y    | Y    | Y    | Y    | Y    |
| Decoder    |    |      |      |      |      |      |      |
| B-Deconv-1 | n  | n    | n    | n    | n    | Y    | Y    |
| B-BNA-2    | n  | n    | n    | n    | n    | Y    | Y    |
| B-Deconv-2 | n  | n    | n    | n    | n    | n    | Y    |

**Constant of Hyper-Parameters** We adopt the following constant as the hyper-parameters for the network: The number of units in Full Connection layer is 600. The Kernel sizes in Deconvolution layer-1, and -2 is 5 × 5. The number of filters of Deconvolution layer-1 is 64. Also, the number of filters of Deconvolution layer-2 is 1.

![Generator's output images in the middle of training](image)
Training We apply the MNIST\cite{6} dataset for training. We make the training program by python using Theano\cite{2} library and Lasagne\cite{5} library, and partially using BinaryNet\cite{4} code and DCGAN\cite{8} code. We run the program on Ubuntu Linux with NVIDIA Titan-X GPU. Our program code is available on-line\cite{3}.

We adopt a stochastic gradient descent (SGD) method as the training method, in which we set the number of mini-batches as 128, and the initial learning rate as 0.0001 that was linearly decreased down to 0 with the decay step of $0.0001/3000 = 3 \times 10^{-8}$.

We judge the finish of training of each Scenario through visual assessment for the quality of output images from the Generator. That is, at each training iteration, the program generates output image and current parameters from the Generator at that time to individual files, so we can examine these files in order to find when the quality reaches its peak. For example, Fig.\ref{fig:training} shows output images in the middle of training and the peak image. As this figure shows, the quality is rising according to the iterations of training.

\begin{figure}[h]
\centering
\includegraphics[width=0.3\textwidth]{fig3}
\caption{Fig. 3. peak image of S0 (baseline)\label{fig:fig3}}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=0.3\textwidth]{fig4}
\caption{Fig. 4. peak image of S1-1\label{fig:fig4}}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=0.3\textwidth]{fig5}
\caption{Fig. 5. peak image of S1-2\label{fig:fig5}}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=0.3\textwidth]{fig2}
\caption{Fig. 2. output image in middle of training and peak image\label{fig:training}}
\end{figure}

\textsuperscript{3} https://github.com/hterada/b-dcgan
After the training of the DCGAN network model, we extracted the set of model parameters of the peak quality. These parameters were written in python pickle formatted files with filename extension '.jl'. We made a dedicated python program called `model_to_ch.py`, which converts '.jl' file to C++ header files, where the model parameters are expressed as C++ constant variables. The building of the B-DCGAN Generator in Xilinx Vivado HLS for FPGA requires these header files.

A binarized parameter represented by +1 or -1 in training model should be represented by 1 or 0 (1-bit value) in FPGA, so the `model_to_ch.py` is converted ±1 parameters into such bit-mapped expression.

### 3.2 Training Results in Scenarios

**S0: Not Binarized (Vanilla) DCGAN** The Scenario S0 is the baseline of image quality. Figure 3 shows output image of peak quality (we call it 'peak image') from the trained model configured in S0.

**S1-1 vs S1-2: Encoder only binarization** The Scenario S1-1 and S1-2 are experiments to examine the influence of binarization of Encoder.

- The S1-1 makes input as integer and binarize only FC layer (see 2.3).
- The S1-2 makes input as integer and binarize FC and BNA layer (see 2.4).

Figure 4 shows peak of S1-1, and Figure 5 shows peak of S1-2.

**S2-1 vs S2-2: A value change** The Scenario S2-1 and the S2-2 are experiments to examine the influence of 'A' value of Encoder.

- In the S2-1, we set A value as 127.
- In the S2-2, we set A value to 4095.

Figure 6 and Figure 7 show the peak generations of the S2-1 and S2-2, respectively.
S3-1 vs S3-2: Encoder & Decoder binarization

The Scenario S3-1 and S3-2 are experiments to examine influence of Decoder binarization.

- The S3-1 adopts the binarize Encoder, B-Deconv-1 and B-BNA-2 in Decoder

- The S3-2 adopts the binarize Encoder, B-Deconv-1, B-BNA-2 and B-Deconv-2 in Decoder; that is all layers in Decoder

Figure 8 shows the peak of the S3-1. Figure 9 shows the results of candidates for peak of the S3-2. According to the training results, in the S3-2 Scenario, the quality of the output image looks very unstable. So we could not decide a single peak in clear. Therefore, we picked up some candidates for the peak.

![Fig. 8. peak image of S3-1](image)

![Fig. 9. peak candidates of S3-2](image)

4 Conclusion & Discussion

We have introduced B-DCGAN; that is DCGAN with binary weights and activations, and integer-valued input. We have conducted several scenarios of experiments on the Theano/Lasagne libraries, which show that it is possible to binarize
DCGAN model, moreover, show what extent is the binarization available with keeping output quality acceptable.

According to the results of these experiments, the last layer B-Deconv-2 mainly have the initiative for output image quality. So the last layer has to operate in the real-valued process. Except for the last layer, other layers can be fully binarized.

According to the results in each Scenario above, we conduct the following speculations:

1. The output quality is affected very few by only binarization of the Encoder(cf. S0, S1-1, S1-2).
2. No influence for quality appears when the $A$ value has changed(cf. S2-1, S2-2).
3. The output quality is somewhat degraded by binarization both the Encoder and partially of the Decoder(cf. S3-1)
4. The output quality is degraded seriously by full binarization of both the Encoder and the Decoder(cf. S3-2)
5. The output quality chiefly depends on the Deconv-2 layer because of the quality difference between S3-1 and S3-2.

At least on the MNIST dataset, we can select the S3-1 as the best Scenario for the B-DCGAN.

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