A Single- and Three-Phase Grid Compatible Converter for Electric Vehicle (EV) On-Board Chargers

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Abstract—This paper proposes a voltage-source converter for an on-board Electric Vehicle (EV) charger which is compatible with both the single- and three-phase (1-ϕ and 3-ϕ) grids. The classic 3-ϕ active AC-DC rectifier circuit is used for both the 1-ϕ and 3-ϕ connection, but a new control scheme and LCL filter are designed to address the double-line frequency power pulsation issue caused by a 1-ϕ grid without using bulky DC capacitors. The third leg of the circuit is utilized to control the power pulsation in conjunction with stored energy in the LCL filter between the grid and charger rectifier. Neither additional active nor passive components are required. For the 3-ϕ connection, the rectifier is under balanced operation; when connected with the 1-ϕ grid, all three legs are controlled cooperatively as a 3-ϕ rectifier but under unbalanced operation to recreate the 1-ϕ voltage. Hence advantages from the 3-ϕ rectifier such as space vector pulse width modulation (SVPWM) and Y/A transformation can be utilized to increase utilization of DC-link voltage and filter capacitance respectively. The operation principle, control, and LCL filter design are reported and validated by both simulation and experiments of a 3-kW prototype.

Index Terms—1-ϕ and 3-ϕ compatible rectifier, EV battery on-board charger, double-line frequency power pulsation, power decoupling.

I. INTRODUCTION

The on-board charger (OBC) for Electric vehicles (EVs) is attracting increasing attention [1-4] because of a rapid uptake of transport electrification [5, 6]. Major automobile production and consumption countries such as the U.S. and the U.K. have set ambitious EV development roadmaps in which the OBC has been defined as an important aspect [7, 8]. By 2035, the gravimetric and volumetric power densities of the OBC are expected to achieve 50 kW/kg and 60 kW/L according to the roadmap, which are approximately seven times higher than existing products [8].

The Level 2 charging in which an AC supply with the current up to 60 A is fed has been commonly considered as a mandatory requirement for OBCs in the domestic and street-side charging [9, 10]. The voltage of such AC supplies can be either single-phase (1-ϕ) or three-phase (3-ϕ). In fact, without additional upgrade on circuit breakers, 3-ϕ supplies can effectively increase the charging rate by three times, showing a sensible and affordable solution for EV charging. The 3-ϕ supply is commonly available in premises and thus it is commercially valuable to equip the EV OBCs with both 1-ϕ and 3-ϕ grid connections [11, 12]. Yet most of commercial OBCs are only compatible with a 1-ϕ supply and it is hardly seen literature on combined 1-ϕ and 3-ϕ OBCs. The potentials of such technology and solution have been overlooked by both the industry and academia.

However, the difference and challenge of combining single- and 3-ϕ OBCs are beyond only adding one more leg in the AC-DC rectifier of the OBC. When the OBC is connected to a 1-ϕ supply, a large power pulsation at double line frequency [13] is generated at the AC-DC rectifier, which would not appear when connecting to a 3-ϕ supply. In this paper, the AC-DC rectifier of the OBC as shown in Fig. 1 is focused to enable both single- and 3-ϕ OBC connection and achieve high power density.

TABLE I summarizes the techniques dealing with this double-line frequency power pulsation. Conventional techniques usually employ a bulk DC capacitor bank to reduce the voltage pulsation at the DC link of the rectifier. The power density is low due to the large number of capacitors at the DC-link output. For the 3-ϕ connection, DC voltage fluctuation is high. However, the difference and challenge of combining single- and 3-ϕ OBCs are beyond only adding one more leg in the AC-DC rectifier of the OBC. When the OBC is connected to a 1-ϕ supply, a large power pulsation at double line frequency [13] is generated at the AC-DC rectifier, which would not appear when connecting to a 3-ϕ supply. In this paper, the AC-DC rectifier of the OBC as shown in Fig. 1 is focused to enable both single- and 3-ϕ OBC connection and achieve high power density.

TABLE I COMPARISON AMONG DIFFERENT TECHNIQUES TO RESOLVE THE DOUBLE-LINE FREQUENCY POWER PULSATION

| Method          | DC link voltage | Charging current | Main issues                  |
|-----------------|-----------------|------------------|------------------------------|
| DC capacitor storage | vdc             | iusc             | Large DC capacitor           |
| Fluctuate charging current | vdc             | iusc             | Impairing battery           |
| Variable DC voltage | vdc             | iusc             | High voltage stress; Over modulation |
| Active power filter (APF) | vdc             | iusc             | Extra switching devices for control; Extra passive devices for energy storage |

Fig. 1. The diagram for EV chargers with a 1-ϕ grid.

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link. The reliability is also limited because the use of less reliable electrolytic capacitors is usually inevitable in this technique to achieve large capacitance.

To increase the power density, [14] boldly directs the low frequency power pulsation into the batteries so the capacitance of the DC-link can be significantly reduced but the DC current provided by the OBC contains a large AC ripple at the double-line frequency although the impact of the low frequency ripple current at to the battery is unclear. Some literature [15, 16] shows that the current pulsation will cause an adverse impact on the battery [17] such as the temperature increase, the capacity degradation, and the gassing.

Advanced control techniques can eliminate the current distortion caused by the double-line frequency power pulsation. [18] employs a repetitive algorithm and a feed-forward controller to eliminate the output current distortion. [19] applies a feedback controller to reduce the current pulsation. However, those special control techniques are based on using the inconstant DC-link voltage largely pulsating at the double-line frequency to smooth the output DC current and a high control bandwidth must be employed. The pulsating DC voltage will cause voltage stress and over-modulation of semiconductors at the peak and bottom of the pulsation respectively.

The active power filter (APF) can divert and store the double-line frequency power pulsation by using much smaller energy storage components. There are different APF circuit topologies depending on the location of the APF and the type of components used for energy storage in the APF [13, 19-30]. The APF can be implemented at the DC side [24, 25, 27] as shown in Fig. 2 (a) or AC side as shown in Fig. 2 (b) [13, 29, 31]; there are inductor-based APFs [24] and capacitor-based APFs [13, 20, 21, 27]. To identify the optimal location and the type of the energy storage components used in APFs, the unified equations among these techniques are necessary.

Reducing the cost and size of the APFs are important. [20] uses split-capacitors to control the current in both the rectifier and APF, and thus no extra switches are required. However, extra passive components are still needed to store the pulsating power. [30, 32] use novel topologies to reduce the capacitance but the voltage ratings of the capacitors and the semiconductor devices must be increased. Since the passive components storing the pulsating energy can dominate the volume and weight of the APF, it is important to investigate the volume/weight of the energy storage components.

This paper proposes a universal converter which is compatible with both a 1-ϕ and 3-ϕ supplies. Unlike some other chargers [11, 12] in which the third leg of the rectifier is redundant when connected to a 1-ϕ supply, the proposed technique utilizes the third leg as part of the AC side APF to address the double-line frequency power pulsation issue while the other two legs are connected to the 1-ϕ AC supply. Furthermore, the low frequency power pulsation is diverted into the LCL filter between grid and converter and the capacitor at the LCL filter is used to store the power pulsation. Therefore, neither extra semiconductor nor passive components are required. From control’s perspective, unlike the conventional APF technique, which decouples and separately controls the dc power and the double-line frequency power pulsation, the proposed control operates three legs as an unbalanced converter when connected with a 1-ϕ supply. Therefore, some benefits from 3-ϕ converters can be utilized, namely, the Y/Δ transformation and space vector pulse width modulation (SVPWM) can be applied to amplify the equivalent capacitance in LCL filters for APF power pulsation storage and achieve higher DC voltage utilization compared with sinusoidal pulse width modulation (SPWM), respectively. When connected with a 3-ϕ supply, the third leg is used with the other two legs like a normal 3-ϕ rectifier and no APF is needed because no double-line frequency power pulsation exists.

The paper is organized as follows: section II derives the universal equations to evaluate the optimal APF circuit. Section III proposes the circuit and discusses its operation principle. Section IV discusses the parameter design procedure of the LCL filter for this combined single- and 3-ϕ rectifiers along with the size and weight comparison with the conventional circuit. Section V presents simulations and experiments to verify the design.

II. EVALUATIONS OF DOUBLE LINE FREQUENCY APFS BASED ON UNIFIED EQUATIONS

Various APFs exist to filter the double line frequency power pulsation of a 1-ϕ rectifier. Fig. 2 (a) and (b) show the APF at the DC side AC side respectively. Either the inductor L or capacitor C or both can be used at the AC and DC side as energy storage components. Because both the topology and type of energy storage components can affect the current / voltage waveforms so does the power density of the APF, identifying the optimal circuit is complicated. A unified expression is derived to assess the performance of the different type of APFs as well as the volume expressions for the passive components are defined to support the selection of the APF in order to minimize the size of the passive components.

A. Evaluating the Size and Weight of Inductors and Capacitors as Energy Storage Devices for APFs
To discuss the relationship between the volume/weight versus the maximum stored energy, Fig. 3 (a) and (b) records 241 different capacitors and 121 different inductors from the market, including 49 inductors with silicon steel cores from the Hammond Manufacturing [33], 36 inductors with MPP power cores from the Magnetics Inc[34], 36 inductors with MPP power cores from ChangSung Corp [35], 19 inductor from Wurth Electronics’s HCFT series, 53 film capacitors from KEMET [36], 49 film capacitors from Vishay [37], and 139 film capacitors from TDK [38]. It should be noted that the weight information of 39 capacitors from C4AE series is not available in the datasheets so the Energy v.s Weight relationship shown in Fig. 3 (b) contains 199 capacitors while Fig. 3 (a) contains all 238 capacitors to illustrate the Energy v.s Volume relationship. Moreover, to calculate the size and volume of inductors with MPP cores, the maximum magnetic flux density is set as 0.1 T and the fill factor = 0.4 is used as a typical value suggested in Magnetics Inc’s design guides [39] in toroidal cores. The commercial inductors have two current limits: the suggested in Magnetics Inc’s design guides [39] in toroidal is set as 0.1 T and the fill factor = 0.4 is used as a typical value.

The solution of (3) is (4),
\[
\begin{align*}
    i_t(t) &= \pm \frac{P_{100}}{\omega_g L} \sqrt{K - \cos(2\omega_g t + \theta)} \\
    v_t(t) &= \pm \frac{P_{100} \omega_g L}{\sqrt{(K - \cos(2\omega_g t + \theta))}} \sin(2\omega_g t + \theta)
\end{align*}
\]

where \( K \) is the constant in general solutions of the differential equations, determined by \( i_t(0) \) as: \( K = i_t(0) \frac{\omega_g L}{P_{100}} + \cos(\theta) \).

Because \( i_t(0) \) can be controlled by setting specific value, \( K \) is determined by the control strategy. \( i_t(0) \) must be a real number so \( K \geq 1 \) is required. Specially, when \( K = 1 \), (4) can be further simplified as,
C. Volume/Weight Expressions of Passive Components

Based on the unified solution in (4), the magnitude of $i(t)$ for AC side APF and DC side APF has the same expression as shown in (6).

$$\text{mag}(i(t)) = \sqrt{\frac{P_{100}}{(\omega_L)}(K+1)}$$

From (6), it is obvious that the AC side inductor current equals to the smallest value of that in the DC side APF for storing the same amount of energy, i.e. $K=1$. The inductance $L$ and inductor current $i(t)$ determine the volume of inductors.

Substituting (6) into (1) yields (7):

$$\begin{align*}
VOL_{L} &= \left( \frac{1}{2} LI_{\text{rated}}^2 \right) K_{Y_L} = \frac{P_{100}}{2\omega_L K_{Y_L}}(K+1) \\
WET_{L} &= \left( \frac{1}{2} LI_{\text{rated}}^2 \right) K_{W_L} = \frac{P_{100}}{2\omega_L K_{W_L}}(K+1)
\end{align*}$$

Eq. (7) shows that the volume/weight of the required inductance is determined by the power pulsation ($P_{100}$), the material ($K_{Y_L}$ / $K_{W_L}$), and the control strategy (i.e. the value of $K$) from (6).

When a capacitor is applied as the energy storage device, similar to the derivation of using the inductor, the double-line power pulsation needs to satisfy (8), where $v_c$ and $i_c$ are the voltage and current of the capacitor used in APF respectively. The general solutions of (8) are given in (9) and the volume expressions are in (10). As aforementioned, the solution and
D. Optimal Circuit Selection

The instantaneous power \( p(t) \) can be written in the form of sequence network, where the subscripts 0, 1, 2 donate the zero sequence, positive sequence, and negative sequence respectively. If no zero-sequence current exists, the expression of \( p(t) \) is shown as (11):

\[
p(t) = v_0(t)i_0(t) + v_1(t)i_1(t) + v_2(t)i_2(t)
\]
TABLE II
THE DC POWER AND 100HZ POWER RIPPLE FROM THE SEQUENCE NETWORK

| V | I | P (dc) | \( \hat{P}_{00} \) (@100 Hz) |
|---|---|---|---|
| 1 | 1 | \( \frac{3}{2} V_I \cos(\theta_I - \theta_e) \) | 0 |
| 2 | 2 | \( \frac{3}{2} V_I \cos(\theta_I - \theta_e) \) | 0 |
| 2 | 1 | 0 | \(-j \frac{3}{2} V_I \) |
| 1 | 2 | 0 | \(-j \frac{3}{2} V_I \) |
| 0 | 1 | 0 | 0 |
| 2 | 0 | 0 | 0 |

\[
p(t) = \begin{bmatrix} v_a(t) & v_b(t) & v_c(t) \\
                        i_a(t) & i_b(t) & i_c(t) \\
\end{bmatrix}^T \begin{bmatrix} i_a(t) \\
                        i_b(t) \\
\end{bmatrix} \\
= V_a(t) I_a(t) + V_b(t) I_b(t) + V_c(t) I_c(t) + V_d(t) I_d(t) + V_e(t) I_e(t) (11)
\]

There are six components in (11), and their contributions can be summarized in TABLE II. TABLE II shows that \( \hat{P}_{00} \) is generated by coupling the positive and negative sequence. When connected with a balanced 3-ϕ supply, no negative-sequence voltage and current exist so \( \hat{P}_{00} \) is zero.

A 1-ϕ supply can be considered as an unbalanced 3-ϕ supply, whereas the 3-ϕ voltages and the 3-ϕ currents are as (12):

\[
\begin{bmatrix} \hat{V}_{a}, \hat{V}_{gb}, \hat{V}_{gc} \\
\hat{i}_{a}, \hat{i}_{b}, \hat{i}_{c} \end{bmatrix} = \begin{bmatrix} \hat{V}_a, 0, 0 \\
\hat{i}_a, \hat{i}_b, \hat{i}_c \end{bmatrix} (12)
\]

By using the abc/2pn transformation, the voltages and currents in the sequence network can be expressed as (13):

\[
\begin{bmatrix} \hat{V}_{a}, \hat{V}_{gb}, \hat{V}_{gc} \\
\hat{i}_{a}, \hat{i}_{b}, \hat{i}_{c} \end{bmatrix} = T_{abc2pn} \begin{bmatrix} \hat{V}_a, \hat{V}_b, \hat{V}_c \\
\hat{i}_a, \hat{i}_b, \hat{i}_c \end{bmatrix} = \begin{bmatrix} \frac{1}{3} \hat{V}_a, 1, 1 \\
\frac{1}{\sqrt{3}} \hat{i}_a, 0, 1 - 30^\circ, 1 - 30^\circ \end{bmatrix} (13)
\]

where \( T_{abc2pn} = \begin{bmatrix} 1 & 1 & 1 \\
1 & \alpha & \alpha^2 \\
1 & \alpha^2 & \alpha \end{bmatrix} \) is the matrix to compute the sequence components (positive, negative, and zero) from 3-ϕ abc system, and \( \alpha = 1 - 30^\circ \) is the complex operator for the 2\( \pi/3 \) rotation.

Substituting (13) into TABLE II derives (14) which is the expression of \( \hat{P}_{00-eg} \) (the phasor of the double-line frequency power pulsation generated by the grid) in form of sequence network:

\[
\hat{P}_{00-eg} = \frac{3}{2} V_{eg} I_{eg} = -j \frac{3}{2} V_{eg} I_{eg} (14)
\]

B. Operating Principles

As concluded in Section II, the AC side APF with capacitors is preferred. The Y/Δ transformation can amplify the equivalent capacitance provided by the LCL filter.

When connected with a 3-ϕ supply as shown in Fig. 6 (a), the 3-ϕ s of the converter are balanced. A 1-ϕ equivalent circuit is shown in Fig. 7 (a). Because \( \hat{P}_{00} = 0 \), there is no double-line frequency power pulsation. The voltage phasor of the rectifier is controlled as \( \hat{V}_{cvt} = \hat{V}_s + j \omega_L \left( L_s + L_c \right) I_g \). The subscript cvt donates the voltage generated by the converter (rectifier).

When connected with a 1-ϕ supply as shown in Fig. 6 (b), the equivalent circuit is shown in Fig. 7 (b) where \( v_{cvt}, v_{cvt} \), and \( v_{cvt} \) are the 3-ϕ voltages of the converter, and \( V_{cvt}, V_{cvt} \), and \( V_{cvt} \) are the 3-ϕ voltages across the \( C_f \). Both the power supply and impedance are asymmetrical, and the circuit needs to be simplified. By using the superposition theory, the unconnected terminal (Phase-C) is substituted by a current source with the current as zero, i.e. \( I_g = 0 \). The Phase-A and Phase-B form the line and neutral of the 1-ϕ where the current is \( I_g \) and \( -I_g \) respectively as shown in Fig. 8 (a). The sequence network circuits in terms of the forward and backward sequence are...
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shown in Fig. 8 (b) and (c) where the positive sequence current is \( I_g \) and the negative sequence current is \( I_g' \). The controlled voltage of the rectifier at each phase (\( V_{cmn}, V_{cvb}, \) and \( V_{cvm} \)) can be expressed in the positive sequence (i.e. \( \dot{V}_{ctrl} \)) and the negative sequence (i.e. \( \dot{V}_{ctrl}' \)) as shown in Fig. 8 (b) and (c).

Two requirements need to be satisfied: 1) the \( I_g \) needs to be controlled as (15), and 2) the capacitor \( \text{C}_f \) should store all double-line frequency power pulsation generated by the grid, \( \dot{P}_{100-CF} = \dot{P}_{100-vg} \) as (16).

\[
\begin{align*}
\dot{V}_g - (\dot{V}_{gb} - \dot{V}_{gb}') &= j\omega_g 2L_g I_g \\
\dot{P}_{100-CF} &= \dot{P}_{100-vg}
\end{align*}
\]

(15)

(16)

where \( \dot{P}_{100-CF} \) and \( \dot{P}_{100-vg} \) are the double-line frequency power generated by capacitors and the grid respectively.

The \( \dot{P}_{100-CF} \) is derived as (17) from TABLE II:

\[
\dot{P}_{100-CF} = -j\frac{3}{2} \dot{I}_{1-f} I_{1-f} - j\frac{3}{2} \dot{I}_{2-f} I_{2-f}
\]

\[
\begin{align*}
&= -j\frac{3}{2} \dot{V}_{1-f} j\omega_g (3\text{C}_f) \dot{V}_{2-f} \\
&= 9\omega_g \text{C}_f \dot{V}_{1-f} \dot{V}_{2-f}
\end{align*}
\]

(17)

Substituting \( \begin{bmatrix} \dot{V}_{gb} \\ \dot{V}_{gb}' \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} \dot{V}_{gb} \\ \dot{V}_{gb}' \end{bmatrix} \) into (15) derives (18),

\[
\dot{V}_{gb} = \frac{\dot{V}_{g} - \dot{V}_{gb} - \dot{V}_{gb}'}{1 + \alpha^2}
\]

and substituting (17) into (16) derives (19). Consequently, the two requirements are transformed in the form of sequence network:

\[
\begin{align*}
(1\angle 30') \dot{V}_{1-f} + (1\angle -30') \dot{V}_{2-f} &= \frac{1}{\sqrt{3}} \dot{V}_{REC} \\
\dot{V}_{1-f} \dot{V}_{2-f} &= \frac{1}{9\omega_g \text{C}_f} \left( \frac{1}{2} \dot{V}_{g} - \dot{P}_{100-vg} \right)
\end{align*}
\]

(18)

(19)

where \( \dot{V}_{REC} = \dot{V}_g - j\omega_g 2L_g I_g \) is a defined vector.

There are two variables ( \( \dot{V}_{1-f} \) and \( \dot{V}_{2-f} \)) in the two equations,(18) and (19). The solution can be derived as (20):

\[
\begin{align*}
\dot{V}_{1-f} &= \left( \frac{1}{\sqrt{3}} \dot{V}_{REC} + \Lambda \right) \left( \frac{1}{2} \angle -30' \right) \\
\dot{V}_{2-f} &= \left( \frac{1}{\sqrt{3}} \dot{V}_{REC} + \Lambda \right) \left( \frac{1}{2} \angle 30' \right)
\end{align*}
\]

(20)

where \( \Lambda = \sqrt{\frac{2}{3}} \dot{V}_{REC} - \frac{\dot{P}_{100-vg}}{9\omega_g \text{C}_f} \) is a defined vector.

From Fig. 8 (b) and (c), the rectifier voltage in the positive and negative sequences need to be controlled as:

\[
\begin{align*}
\dot{V}_{ctrl} &= \dot{V}_{ctrl} + \dot{V}_{ctrl} = \dot{V}_{ctrl} \\
\dot{V}_{ctrl}' &= \dot{V}_{ctrl}' + \dot{V}_{ctrl}' = \dot{V}_{ctrl}'
\end{align*}
\]

(21)

The \( \dot{V}_{ctrl} \) and \( \dot{V}_{ctrl}' \) are derived as (17) from TABLE II:

\[
\begin{align*}
\dot{V}_{ctrl} &= \dot{V}_{ctrl} + \dot{V}_{ctrl} = \dot{V}_{ctrl} \\
\dot{V}_{ctrl}' &= \dot{V}_{ctrl}' + \dot{V}_{ctrl}' = \dot{V}_{ctrl}'
\end{align*}
\]

(22)

where \( T_{abc2a0f} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{3}{2} \end{bmatrix} \) and \( T_{qpm2abc} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \) are the matrix to perform the \( zpm \) to \( abc \) transformation, and the \( abc \) to \( a0f \) transformation respectively.

Therefore, the open-loop control of this unbalanced operation for a \( 1-\phi \) connection can be illustrated in Fig. 9. With setting the complex power \( S \), the sequence network voltages on the \( \text{C}_f \), the sequence network voltages on the converter, and the converter voltage in the \( a0f \) axis are derived, and the switching signals are generated with SVPWM modulation block.

Fig. 10 shows the trajectory of the required rectifier voltage by using the technique in Fig. 9. Because the rectifier is operating in an unbalanced condition, the trajectory is not a circle but an ellipse. Because the SVPWM is applied, the
such as voltage fluctuation and reactive power provision. A useful margin for other possible grid connection requirements is the harmonic current injected to the grid. The closed-form expressions of the switching harmonic voltages are derived in [44], showing that the most significant harmonic in a half-bridge is:

\[ V_{har} = \frac{2V_{dc}}{\pi} \left( \frac{\pi}{2M} \right) \leq \frac{2V_{dc}}{\pi} \]

where \( V_{har} \) is the most significant harmonic’s magnitude, \( J_0 \) is the first-order Bessel function and is always smaller than 1. \( M \) is the modulation index within \([0, 1]\). When \( M = 0 \), \( V_{har} \) reaches its maximum value:

\[ I_{har} = V_{har} G_{LCL-har} (s = j\omega_{in}) \leq I_{std} \]
where $L_{\text{std}}$ is the maximum harmonic limit in the grid code. This paper applies IEEE Std 519 [42] as the grid limits in which $L_{\text{std}} = 0.3\% I_{\text{rated}}$ when $f_{\text{sw}} > 35 f_{\text{g}}$.

From (26) and (27), the minimum value of $L_g$ is derived as:

$$L_g = \frac{4 V_f}{\pi \omega_d L_c (3 C_f) I_{\text{std}}} \quad (28)$$

Fig. 11, (23) and (28) can be used to determine $C_f$, $L_c$, and $L_g$ respectively. The proposed technique requires larger $C_f$ than the existing design because the value of $C_f$ is determined by voltage modulation and energy storage given by Fig. 10 and Fig. 11. In this paper, the DC-link voltage needs to be regulated at 650 V which is commonly used in OBCs and the 1-6 power rating is set to be 10 kW, which covers the common 6.6 kW and 3.3 kW Level 2 and Level 1 charging standards.

The required $C_f$ is 14.3 $\mu$F obtained from Fig. 11, which is larger than 0.95 $\mu$F of the conventional method in [43]. However, (28) shows that the increase of $C_f$ can lead to a decrease of $L_g$. The total volume and weight of the $LCL$ filter need to be assessed.

Denoting $K_{C_f}$ as the coefficient of quantifying the increase of $C_f$, considering $L_g$ remains unchanged from (23), then $L_g$ is decreased by $K_{C_f}$ from (28). The volume and weight of the $LCL$ filter are functions of $K_{C_f}$, and can be expressed as (29) and (30) respectively:

$$VOL_{\text{TOT}}(K_{C_f}) = 3(K_{C_f} \cdot VOL_{Lc} + VOL_{Lg} + VOL_{C_f})$$
$$WET_{\text{TOT}}(K_{C_f}) = 3(K_{C_f} \cdot WET_{Lc} + WET_{Lg} + WET_{C_f})$$

where $VOL_{\text{TOT}}$, $VOL_{Lc}$, $VOL_{Lg}$ and $VOL_{C_f}$, $WET_{\text{TOT}}$, $WET_{Lc}$, $WET_{Lg}$ and $WET_{C_f}$ are the volume and weight of $LCL$ filter, $C_f$, $L_c$ and $L_g$ respectively.

In order to compare with the $LCL$ design from [43] which was for 200 kVA, the $LCL$ filter is recalculated by using the same method in [43] to compare with the filter used in this proposed method at 10 kVA, 650 V DC-link system. The $LCL$ parameters of the conventional method in [43] at 200 kVA and 10 kVA are shown in TABLE III, and its volume/weight can be evaluated with Fig. 12. For the 200 kVA system [43], $L_c = 100 \mu$H, $L_g = 270 \mu$H, $C_f = 10 \mu$F; the rated current and voltage are 240 A (rms) and 1200 V (peak). If a 30% margin is used for the inductor current and capacitor voltage, the required maximum energies stored in $L_c$, $L_g$, and $C_f$ are $Eng_{Lc} = 0.5 L_c (1.3 \sqrt{2} \times 240^2)$ J = 9.78 J, $Eng_{Lg} = 0.5 L_g (1.3 \sqrt{2} \times 240^2)$ J = 26.4 J and $Eng_{C_f} = 0.5 C_f (1.3 \times 1200^2)$ J = 12.2 J. Their volume and weight can be evaluated with the energy density equation in (1). In [43], $L_g$ used silicon steel inductors where $K_{Lg} = 10^4$ J/mm$^3$ and $K_{WLg} = 2 \times 10^4$ J/g, giving $VOL_{Lg} = Eng_{Lg} / K_{Lg} = 26.4 \times 10^4$ mm$^3$ and $WET_{Lg} = Eng_{Lg} / K_{WLg} = 132 \times 10^3$ g; $L_c$ used nanocrystalline based inductor, and the volume is given as $VOL_{Lc} = 6.78 \times 10^6$ mm$^3$ in [43], and $WET_{Lc} = VOL_{Lc} / \text{density} = 34 \times 10^3$ g when density $= K_{VLc} / K_{WLc} = 5.0$ g/cm$^3$; $C_f$ used film capacitors where $K_{VC} = 10^4$ J/mm$^3$, $K_{WC} = 0.1$ J/g, and $VOL_{C_f} = 121 \times 10^3$ mm$^3$, giving $WET_{C_f} = 121$ g. Therefore, the total volume and weight for the system with $K_{C_f} = 1$ can be derived as: $VOL_{\text{TOT}}(K_{C_f} = 1) = 9.99 \times 10^4$ mm$^3$; $WET_{\text{TOT}}(K_{C_f} = 1) = 4.98 \times 10^5$ g.

### TABLE IV

| Designed parameters | Selected devices | Energy capacity ($I_f$) ($\mu$F) | Evaluated volume ($\mu$m$^3$) | Evaluated weight ($g$) ($\mu$F) | Actual volume ($\mu$m$^3$) | Actual weight ($g$) |
|---------------------|-----------------|-------------------------------|-----------------------------|-----------------------------|---------------------|-------------------|
| $L_c$               | 336 $\mu$H @ 28 A | 744736540470 ($r_1$) x 7 | 0.3130 | 1.5180 | 2.62x10$^3$ | 1310 | 1720 | 3.62x10$^3$ | 1568 |
|                     | (329 $\mu$H, 31 A) |                               | 0.3130 | 1.5180 | 2.62x10$^3$ | 1310 | 1720 | 3.62x10$^3$ | 1568 |
| $L_g$               | 430 $\mu$H @ 28 A | 7447436540470 x 9 | 0.1673 | 0.2033 | 3.35x10$^4$ | 1670 | 2200 | 4.65x10$^4$ | 2016 |
|                     | (423 $\mu$H, 31 A) |                               | 0.1673 | 0.2033 | 3.35x10$^4$ | 1670 | 2200 | 4.65x10$^4$ | 2016 |
| $C_f$               | 0.9 $\mu$F @ 845V | MKP1848510094K2 ($r_2$) | 0.3418 | 0.4050 | 3418 | 3418 | 4050 | 4.1 | 5472 | 6.0 |

Fig. 12. The flow-chart to evaluate the volume/weight of the $LCL$ filter.
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From Fig. 13(a), the optimal volume can be achieved when $K_{Cf} = 15.25$. From (23), $L_c$ remains unchanged; from (29) and (30), $L_g$ is decreased to $270 \mu H / K_{Cf} = 17.7 \mu H$ and $C_f$ is increased to $(10 \mu F \times K_{Cf}) = 153 \mu F$. From (29) and (30), the total volume and weight are $VOL_{TOT}(K_{Cf} = 15.25) = 3.11 \times 10^7 \text{ mm}^3$ and $WET_{TOT}(K_{Cf} = 15.25) = 1.33 \times 10^7 \text{ g}$, respectively. Similarly, from Fig. 13(b), the optimal weight can be achieved when $K_{Cf} = 31.50$. From (23), $L_c$ remains unchanged; from (29) and (30), $L_g$ is decreased to $270 \mu H / K_{Cf} = 8.57 \mu H$ and $C_f$ is increased to $10 \mu F \times K_{Cf} = 315 \mu F$. According to (29) and (30), the total volume and weight are $VOL_{TOT}(K_{Cf} = 15.25) = 3.4 \times 10^7 \text{ mm}^3$ and $WET_{TOT}(K_{Cf} = 15.25) = 1.3 \times 10^7 \text{ g}$, respectively.

The total volume and weight of the $LCL$ filter can be plotted by using (28) and (29) as illustrated in Fig. 13. It is clearly shown that the design in [43] can be improved by increasing $K_{Cf}$ so the total volume and weight of the $LCL$ filter can be decreased. The optimal $K_{Cf}$ for the total volume and weight can be calculated by setting the first derivatives to be zero as $d(VOL_{TOT})/dK_{Cf} = 0$ and $d(WET_{TOT})/dK_{Cf} = 0$. The solutions are:

$$\begin{align*}
K_{Cf}^{\text{opt vol}} &= \frac{VOL_{le}}{VOL_{Cf}} \quad (31) \\
K_{Cf}^{\text{opt wet}} &= \frac{WET_{le}}{WET_{Cf}} \quad (32)
\end{align*}$$

where $K_{Cf}^{\text{opt vol}}$ and $K_{Cf}^{\text{opt wet}}$ are the $K_{Cf}$ for the optimal volume and the optimal weight respectively.

When (31) is met, $K_{Cf}VOL_{Cf} = VOL_{le} / K_{Cf}$, which means that the when $C_f$ and $L_g$ have the same volume, the optimal volume can be reached. Similarly, when the $C_f$ and $L_g$ have the same weight, (32) is met and the optimal weight can be reached. In the conventional design, both the volume and weight of $L_g$ is much larger than $C_f$ due to a small capacitance of $C_f$. However, in this proposed design, the increased capacitance $C_f$ will enable the volume and weight of the $C_f$ and $L_g$ become closer to each other, thus the total volume and weight of the filter will become closer to the optimum.

For $S = 10$ kVA with the $LCL$ designed technique in [43], the parameters can be derived as the marker 4 of Fig. 13(c): $L_c, L_g$, and $C_f$ are $336 \mu H$ at $21.5$ A, $420 \mu H$ at $21.5$ A and $0.96 \mu F$ at 650 V, respectively. If a 30% margin is used for the inductor current and capacitor voltage, the currents for both $L_c$ and $L_g$ are $28.0$ A, and the voltage for $C_f$ is 845 V. Thus, the energy stored in $L_c, L_g$, and $C_f$ are $Eng_{Lc} = 0.5 \times 336 \mu H \times 28^2 = 0.1311 \text{ J}$, $Eng_{Lg} = 0.5 \times 336 \mu H \times 28^2 = 0.1673 \text{ J}$, and $Eng_{Cf} = 0.5 \times 0.9 \mu F \times 845^2 = 0.3418 \text{ J}$, respectively. If both $L_c$ and $L_g$ use inductors with MPP cores with $K_{le} = 5 \times 10^{-7} \text{ J/mm}^3$, and $K_{wl} = 1 \times 10^4 \text{ J/g}$ as shown in Fig 1, the volume and weight are as follows: $VOL_{le} = 2.62 \times 10^5 \text{ mm}^3$, $WET_{le} = 1.31 \times 10^3 \text{ g}$, $VOL_{lg} = 3.34 \times 10^5 \text{ mm}^3$, $WET_{lg} = 1.67 \times 10^3 \text{ g}$. For $C_f, K_{Cf} = 1 \times 10^5 \text{ J/mm}^2, K_{Cf} = 0.1 \mu F$, $Eng_{Cf} = 0.5 CV^2 = 0.3418 \text{ J}$, therefore, $VOL_{Cf} = Eng_{Cf} / K_{Cf} = 0.3418 / 1 \times 10^4 = 3.42 \times 10^3 \text{ mm}^3$, and $WET_{Cf} = Eng_{Cf} / K_{Cf} = 0.3418 / 0.1 = 3.42 \text{ g}$.

To verify the designed effectiveness of the designed value, TABLE IV is added to compare the weight and volume between the designed parameters and the commercial devices. The evaluated volume and weight are $1.8 \times 10^6 \text{ mm}^3$ and $8.95 \times 10^3 \text{ g}$; the volume and weight of actual commercial components are $1.8 \times 10^6 \text{ mm}^3$ and $8.95 \times 10^3 \text{ g}$. The differences between evaluation and actual devices are small as shown in Table IV. It should be noted that the weight and volume differences on
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the capacitor $C_f$ between evaluation and actual device are more significant than that from the inductors. However, the capacitor is much smaller and lighter than the inductor thus this deviation between evaluation and actual commercial components can be neglected in the LCL filter design.

Fig. 13 clearly shows that volume and weight can be decreased with increased $K_C$. The LCL filter reaches the optimal volume and weight when $K_C = 10.28$ and 22.93 respectively. If $C_f$ is set as 16 $\mu$F in this proposed method, then $K_C = 16.67$, $V_{OLTOT} = 1.02\times10^6$ mm$^3$ and $WETTOT = 4406$ g, which are closer to the optimum. The volume and weight of the LCL filter with $K_C = 16.67$ (the marker 7 in Fig. 13) can be reduced by 76.47% and 103.4% respectively compared to the conventional design with $K_C = 1$ (the marker 4 in Fig. 13).

In conclusion, although the proposed technique requires that the LCL filter not only attenuates the harmonic current to the grid but also store the double-line frequency power pulsation, both the size/weight of the LCL filter can be reduced with the proposed technique because the increased capacitance $C_f$ for storage has moved the total volume and weight closer to the optimum as shown in Fig. 13.

B. Parameter Design for the DC-Link Capacitor

For the conventional 1-ϕ HB converter, the capacitance required to smooth the 100 Hz power pulsation is given as [45]:

$$C_{dc} > \frac{P_{dc}}{2\alpha_v V_{dc} \frac{1}{2} \Delta V_{dc}} = \frac{P_{dc}}{\alpha_v V_{dc} \Delta V_{dc}} \tag{33}$$

The proposed APF technique can eliminate the double-line frequency power pulsation. Therefore, the switching harmonics determine the DC capacitance.

The closed-form expressions of the switching harmonic voltages in [44] show that the most significant harmonics locates at the switching frequency $f_{sw}$.

$$V_{sw} = \frac{2V_{dc}}{\pi} J_0\left(\frac{\pi}{M}\right) \leq \frac{2V_{dc}}{\pi} \tag{34}$$

where $J_0$ is the Bessel function of the first kind, and $M$ is the modulation index. When $M = 0$, $V_{SW}$ reaches its maximum value.

If the AC output voltage and current are: $v_{sw}(t) = V_{sw}\sin(\omega_{sw} t + \theta_{sw})$ and $i_{sw}(t) = I_{sw}\sin(\omega_{sw} t + \theta_{sw})$, where $\omega_{sw}$ and $\theta_{sw}$ are the initial phase of $v_{sw}(t)$ and $i_{sw}(t)$. The instantaneous power at the AC output is $p(t) = (V_{sw}\sin(\omega_{sw} t) + V_{sw}\sin(\omega_{sw} t + \theta_{sw})) \times (I_{sw}\sin(\omega_{sw} t + \theta_{sw}) + I_{sw}\sin(\omega_{sw} t))$. Because $I_{sw}$ needs to be smaller than 4% of the grid current $I_{g}$ to comply with the grid code [42], it can be neglected. Therefore, the expression of $p_{sw}(t)$ and its magnitude $P_{SW}$ are:

$$p_{sw}(t) = V_{sw} I_{sw} \sin(\omega_{sw} t) \sin(\omega_{sw} t + \theta_{sw})$$

$$P_{SW} = \frac{1}{2} V_{sw} I_{sw} \tag{35}$$

Because the semiconductors do not store energy, $P_{SW}$ also donates the magnitude of the instantaneous power at the DC-link. The $P_{SW}$ for an unbalanced 3-ϕ converter is three times smaller than that in a half-bridge. The required capacitance needs to meet:

$$C_{dc} > \frac{3P_{sw}}{\omega_v V_{dc} \frac{1}{2} \Delta V_{dc}} = \frac{6P_{sw}}{\omega_v V_{dc} \Delta V_{dc}} \tag{36}$$

Fig. 14 shows the comparison of the required DC capacitance for the $P_{SW}$ at switching frequency and for the $p_{100}$ at the double-line frequency. The $C_{dc}$ for $P_{SW}$ is significantly smaller than the $C_{dc}$ for $p_{100}$, especially for the applications with a large $f_{sw}$. Because the proposed technique only needs $C_{dc}$ for $P_{SW}$, the size and volume can be greatly reduced. For $f_{sw} = 50$ kHz, $C_{dc} \geq 6.1$ $\mu$F, and a 10 $\mu$F capacitor is used for $C_{dc}$ in this paper.

V. SIMULATION AND EXPERIMENT RESULTS

A. Simulations

The proposed circuit is shown in Fig. 6, and the parameters are shown in TABLE V. Fig. 15 and Fig. 16 shows the simulation results of the rectifier fed by 1-ϕ supply at 3 kW and 3-ϕ supply at 10 kW respectively. The proposed OBC will have two connectors, the 1-ϕ connector (regulated by BS1336) and the 3-ϕ connector (regulated by IEC 62196), for users to select.
Once the corresponding plug has been connected, the OBC will work accordingly for that connection, either 1-ϕ or 3-ϕ. It is obvious that the charging voltage remains the same during each charging event, either 1-ϕ or 3-ϕ for each charging event thus there is no need for dynamic switching between 1-ϕ and 3-ϕ within one charging event. However, the additional 3-ϕ charging opportunity offered by the technology reported in this paper will benefit motorists by using 3-ϕ charging facility for three times higher charging rate by using the 1-ϕ and 3-ϕ compatible OBC.

Fig. 15 shows that both the DC-link voltage and the AC line current are smooth when connected with a 3-ϕ grid. The performance of the rectifier with a small DC capacitor and without using the APF is firstly assessed to highlight the significance of the distortion caused by the double-line power.

Fig. 16. The simulated waveforms of the conventional H-bridge (HB) with the LCL filter (all the parameters are as shown in TABLE V) connected to a 1-ϕ grid: (a) \( V_g = 230 \text{ V RMS}, \ P_o = 3 \text{ kW} \) and (b) \( V_g = 120 \text{ V}, \ P_o = 300 \text{ W} \).

\[
\begin{align*}
V_g(t) &\quad 230 \text{ V RMS} \\
325 \text{ V peak} \\
V_d(t) &\quad 995.1 \text{ V} \\
V_{\text{dmin}} &\quad 214.4 \text{ V} \\
V_{\text{dmax}} &\quad 651.6 \text{ V} \\
V_{\text{dmin}} &\quad 639.9 \text{ V} \\
I_g(t) &\quad i_{\text{max}} = 85.57 \text{ A} \\
I_{\text{max}} &\quad 19.78 \text{ A} \\
I_{\text{max}} &\quad 374.6 \text{ V} \\
I_{\text{max}} &\quad 203.4 \text{ V}
\end{align*}
\]

(a) (b) (c)

Fig. 17. The simulated waveforms of the proposed method of the converter connected to a 1-ϕ grid.

Fig. 18. Test set-up of (a) overall converter, (b) the capacitor bank for the dc capacitor storage technique, and (c) the film capacitor for the proposed technique.
When connected with a 1-ϕ grid using the conventional 1-ϕ converter (the HB circuit with the LCL filter in TABLE V, 10 μF dc capacitor, and the SPWM modulation technique) for the rated 3 kW operation, as shown in Fig. 16 (a), both the DC voltage and the AC current are greatly distorted due to the 100 Hz power pulsation. The voltage ripple is 780.7 V which was more than the nominal DC voltage of 650 V, and the maximum value reaches 95.1 V. The grid current is also significantly distorted because of the DC voltage ripple. Because the voltage and current stress are significantly higher than the nominal voltage and current and the magnitude of the over current and voltage depend on the power, it is impractical to verify the results with experiment at the rated power if using the same rating of the devices in the rectifier. Instead, a scaled-down test set-up with $V_g = 120$ V and $P_o = 300$ W is conducted experimentally thus a 300 W simulation as shown in Fig. 16(b) is also presented for comparison. If the proposed technique with $C_{dc} = 10$ μF is applied, the DC-link voltage ripple in Fig. 17 is 11.7 V; in comparison, if the conventional HB with $C_{dc} = 10$ μF is applied, the ripple voltage as shown in Fig. 16(b) is \((995.1 - 214.4) = 780.7\) V. The comparison between Fig. 16(b) and Fig. 17 shows that the proposed technique can greatly reduce the 2nd order DC harmonics. The conventional HB can also achieve small 2nd harmonic with bulk DC capacitors, and the required $C_{dc}$ can be calculated by using (33): to achieve $\Delta V_{dc} = 11.7$ V, the required $C_{dc}$ is $C_{dc} = 3000 / (314 \times 650 \times 11.7) F = 1.13$ mF; in comparison, to achieve $\Delta V_{dc} = 11.7$ V, Fig. 17 with the proposed technique only uses $C_{dc} = 10$ μF. Comparing 10 μF in the proposed technique and the 1.13 mF in the conventional H-bridge converter, it can be concluded that the proposed APF requires only less than 1% capacitance of the DC capacitor to achieve the same 2nd order DC harmonics.

B. Experiments

The experiment test set-up is shown in Fig. 18. The comparison between Fig. 18 (b) and (c) showed that the size reduction of the DC-link capacitor is significant. The significant reduction of the DC capacitance allows using the film capacitors at the DC-link, which improved the reliability and lifetime of the OBC due to higher robustness of the film capacitor than its electrolytic counterpart.
Fig. 19-Fig. 21 show the experiments with the proposed APF technique at 300 W, 500 W, and 3 kW rated power respectively. The waveforms in Fig. 19(a), Fig. 20(a) and Fig. 21(a) show that the DC-link voltage was smooth, and the grid current is sinusoidal with acceptable small distortions; the dc ripple spectrum in Fig. 19(b), Fig. 20(b), and Fig. 21(b) show that the 100 Hz voltage pulsations are small at various load conditions; the grid current spectrum show that at various load conditions, the grid current can satisfy the grid code in the IEEE 519. The experimental results in Fig. 21 match the simulations shown in Fig. 17 well. Fig. 22 shows that the proposed technique can
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Fig. 25. The 500 W experimental results of the conventional H-bridge converter with the 10 μF dc capacitor: (a) the waveforms of $V_{dc}$, $V_g$, and $I_g$, (b) the spectrum of the dc voltage $V_{dc}$, and (c) the spectrum of the grid current $I_g$ versus the IEEE 519 current limit.

Limit the magnitude of the 100 Hz voltage ripple with the various loads to less than 1.5% of the DC voltage (650V) from 300 W to 3000 W. Fig. 23 shows the efficiency comparison between the proposed technique with 10 μF dc capacitor and the conventional 1-ϕ converter (the HB circuit with the LCL filter in TABLE V, and the SPWM modulation technique) with 1.3 mF dc capacitors. The efficiency of the proposed technique decreases because the extra APF (the third leg) consumes power, and the peak efficiency is 97.6% at 3000 W.

Fig. 24(a) and Fig. 25(a) shows that the conventional 1-ϕ converter (which is a HB with the LCL filter) with 10 μF dc capacitance suffered great distortion from both the DC-link voltage and the grid current. When operating at 500W, the experiment of non-APF is conducted with reduced $V_g$ (120 V) and $V_{dc}$ (325 V) to avoid the over voltage / current failure caused by power pulsation. Fig. 24(b) and Fig. 25 (b) shows that the 100 Hz ripple was 49.97% (324.8 V) and 84.89% (275.8 V) respectively. The experiment matched the simulations shown in Fig. 16 (b) well.

VI. CONCLUSION

This paper proposes a voltage-source converter which is compatible with both 1-ϕ and 3-ϕ grids. The circuit is still the classic 3-ϕ converter, but the control strategy and the LCL filter are redesigned to address the issue of the power pulsation at double-line the grid frequency. When connected with a 1-ϕ grid, the power pulsation at double-line the grid frequency is diverted and stored into the LCL filter by utilizing the third leg of the rectifier circuit. Therefore, neither extra active switches nor passive components are required. The advantages of the proposed technology can be summarized as below:

1. Good compatibility: the charger can work with both 3-ϕ and 1-ϕ grids without changing the topology. When connected with a 1-ϕ grid, the third leg is used, and no extra active switches are required.
2. Simple circuit: $C_f$ in the LCL filter is utilized to store the pulsating power. $L_g$ and $L_c$ are utilized to damp the ripple current. Therefore, no extra passive components are required.
3. LCL filter’s size/volume reduction: Although the $C_f$ of the LCL filter is increased to store the pulsating power, the total volume and weight of the LCL filter can be reduced by 76.47% and 103.4% due to the reduction of the $L_g$.
4. DC-link capacitance reduction: The DC-link capacitance can be reduced by 130 times at the same switching frequency of the rectifier compared with the conventional DC capacitor storage techniques as mentioned in the experimental section.
5. Unified equations for size evaluation: the unified equations are obtained to identify the optimal circuit for AC/DC APFs with capacitors/inductors as energy storage devices and can be used to optimize the size/weight of the LCL filter.
6. High dc-voltage utilization: when connected with a 1-ϕ grid, the system operates in an unbalanced 3-ϕ condition. Therefore, the advantages of the 3-ϕ system can be utilized to increase the DC voltage utilization by 15% and increase the utilization of the LCL capacitor by three times because of applying the SVPWM and Y/Δ transformation provided by the 3-ϕ systems.

APPENDIX

GRID HARMONIC CURRENT WITH 1-ϕ GRID

When operating with under 1-ϕ voltage, the circuit is as shown in Fig. 26, which is a 4-node network. Write the nodal equations in the matrix format as follows:

$$\mathbf{Y} \begin{bmatrix} V_x \\ V_y \\ V_z \\ V_s \end{bmatrix} = \begin{bmatrix} V_{cxt} \\ V_{vth} \\ V_{vth} \\ V_{vth} \end{bmatrix}$$
Fig. 26. The equivalent circuit of proposed technique for 1-ϕ grid.

where \( Y \) is the bus admittance matrix and its value is:

\[
Y = \begin{bmatrix}
Y_{gg} + (0.5Y_{ lc} + Y_{ cf}) + Y_{ g},

Y_{ gc} - (0.5Y_{ lc} + Y_{ cf}) & -0.5Y_{ lc} + Y_{ cf}

Y_{ gc} + Y_{ cf} - (0.5Y_{ lc} + Y_{ cf}) & 0

Y_{ gc} & Y_{ gc} + Y_{ cf} - Y_{ cf}
\end{bmatrix}
\]

where \( Y_{ gg}, Y_{ gc}, \) and \( Y_{ cf} \) are the admittance of \( L_g, L_c, \) and \( C_f \) respectively.

Because \( I_g = (V_g - V_c) / (2sL_g) \), \( I_g \) can be derived in the matrix format as:

\[
I_g = \frac{1}{2sL_g} \begin{bmatrix}
1 & -1 & 0
\end{bmatrix} \begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix}
\]

and can be simplified as:

\[
I_g = \frac{V_{cva} - V_{cvt}}{s^2L_g} \begin{bmatrix}
1 & -1 & 0
\end{bmatrix} Y^{-1} \begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix}
\]

Because the most significant harmonic is \( V_{har} \), and \( V_{cva} \leq V_{har} \), \( V_{cvt} \leq V_{har} \). The maximum value of \( I_g \) is as (38),

\[
I_g = \frac{2V_{har}}{s^2L_g} (3C_f) + s(L_g + L_c)
\]

Define \( G_{LCL-har} \) as the maximum harmonic transfer function, then,

\[
G_{LCL-har} = \frac{I_g}{V_{cva}} = \frac{2}{s^2L_g} (3C_f) + s(L_g + L_c)
\]

With a balanced 3-ϕ system, the transfer function of the LCL filter is

\[
G_{LCL-har} = \frac{1}{s^2L_g} (3C_f) + s(L_g + L_c)
\]

and the maximum voltage harmonic remains unchanged as (26). Therefore, the worst scenario for \( I_g \) harmonics happens when connected to a 1-ϕ grid, and the LCL filter designed for the proposed 1-ϕ system can meet the grid current harmonic for the balanced 3-ϕ system.

Eq. (37) shows that \( V_{cvt} \) has no contribution to \( I_g \). To analyse the reason, the superposition theory is applied. Thus, all the voltage sources except \( V_{cva} \) are shorted as shown in Fig. 27. It is seen that Node 1 and Node 2 are in the equal voltage potential points of a balanced Wheatstone bridge when the only \( V_{cva} \) is applied. Therefore, \( I_g \) is independent of \( V_{cva} \).

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