Towards Practical Software Stack Decoding of Polar Codes
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ABSTRACT

The successive cancellation list decoding algorithm for polar codes yields near-optimal decoding performance at the cost of high implementation complexity. The successive cancellation stack algorithm has been shown to provide similar decoding performance at a much lower computational complexity, but software implementations report a sub-par T/P performance. In this technical report, the benefits of the fast simplified successive cancellation list decoder are extended to the stack algorithm, resulting in a throughput increase by two orders of magnitude over the traditional stack decoder.

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I Introduction

Polar codes were proposed by Erdal Arikan in 2008 [1] as the first set of linear block codes that have an explicit construction and provably achieve the symmetric capacity of a binary memoryless channel. Polar codes faced initial resistance due to the low throughput of the sequential successive cancellation (SC) decoding algorithm, as well as its mediocre error-correction performance at short code lengths. The successive cancellation list (SCL) algorithm [2] and its CRC-aided variant [3] enabled optimal decoding performance at short lengths, and fast simplified successive cancellation decoding [4–6] improved the throughput performance considerably, thereby deeming polar codes a viable candidate for practical applications. In 2016, polar codes were selected by 3GPP as one of the error-correcting codes to be used in the enhanced Mobile Broadband (eMBB) control channel [7, 8].

The successive cancellation stack (SCS) algorithm proposed in 2012 [9, 10] provides similar error-correcting performance as the SCL algorithm with a complexity that varies with the channel conditions. At high channel noise, SCS has the same complexity as SCL, and as channel noise decreases, the SCS complexity approaches that of SC, making it an attractive candidate. Although the SCS algorithm has an attractive complexity, software implementations report a mediocre T/P performance. This technical report outlines a method to apply the fast simplified decoding scheme in [4, 5] to the reduced memory stack decoder in [11], resulting in a software T/P improvement of over two orders of magnitude, from 9 Kbps to 930 Kbps.

This report is organized as follows: Section II provides relevant background information regarding polar codes and the pertinent decoding algorithms. Section III highlights key software implementation details of the decoders. Section IV describes the fast simplified scheme applied to stack decoding, and Section V presents and discusses the simulation results. Finally, Section VI concludes this report.
II Background

II-A Polar codes

Polar codes asymptotically achieve the symmetric channel capacity for a B-DMC $W$ by considering a set of $N$ independent copies of $W$ and recursively applying a polarizing transform $F = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$ to the inputs of the channels, resulting second set of $N$ channels $\{W_N^{(i)}\}$ that are said to be polarized in the sense that $K$ of the inputs are completely reliable, while the remaining $(N - K)$ inputs are completely unreliable, and as $N \to \infty$ the fraction $\frac{K}{N} \to I(W)$.

A polar code of length $N$ and message bit length $K$ shall be denoted by $PC(N, K)$. Given an information bit set $A$ of size $K$ and a corresponding frozen bit set $A^c$ of size $(N - K)$, the input $u_{0}^{N-1}$ to the polarized channels is constructed from a message bit sequence $m_{0}^{K-1}$ by placing the bits at the indices contained in a $A$, and setting the remaining indices to 0. The encoding step to generate the codeword $c_{0}^{N-1}$ can then be expressed as the matrix multiplication

$$c_{0}^{N-1} = u_{0}^{N-1} F^\otimes n,$$

where $n = \log_2 N$ and $F^\otimes n$ is the $n^{th}$ Kronecker power of the kernel $F$, and can be represented by the XOR tree shown in Figure 1. The tree has $n$ stages, and the variable $\lambda \in [0, n]$ is used to denote the current stage in the tree. Given a stage $\lambda$, there are $(n - \lambda + 1)$ branches denoted by $\phi \in [0, (n - \lambda)]$, and the size of each branch is $\Lambda = 2^\lambda$.

II-B Decoding algorithms

All decoding algorithms in this section are described in the LLR domain.

Successive cancellation

The successive cancellation (SC) decoding algorithm [1] operates on the encoding tree, propagating that channel values $LLR(y_i)$ from stage $n$ to produce $LLR\left(y_{0}^{N-1}, \hat{u}_{0}^{i-1}|\hat{u}^i\right)$
at stage 0, according to the min-sum approximation [12] in Figure 2 and Equation (2). The estimate $\hat{u}_i$ can then be made following Equation (3).

\begin{align*}
f(\alpha_0, \alpha_1) &= \text{sign}(\alpha_0) \text{sign}(\alpha_1) \min(|\alpha_0|, |\alpha_1|) \quad \alpha \in \mathbb{R} \quad (1) \\
g(\alpha_0, \alpha_1, \beta) &= \alpha_0 + (-1)^{\beta} \alpha_1 \quad \alpha \in \mathbb{R}, \beta \in [0, 1] \quad (2) \\
\hat{u}_i &= \begin{cases} 
  HD \left( LLR \left( y_0^{N-1}, \hat{u}_0^{i-1} | \hat{u}^i \right) \right) & \text{if } i \in A \\
  0 & \text{otherwise}
\end{cases} \quad (3)
\end{align*}

**Figure 1** – Encoding tree for $PC(8, 4)$ with $A = \{3, 5, 6, 7\}$.

**Figure 2** – Min-sum approximation over the polarizing kernel.
The XOR encoding tree in Figure 1 is reinterpreted as a binary tree as shown in Figure 3, and the stage $\lambda$ and branch $\phi$ is used to identify each node, denoted by $(\lambda, \phi)$. A node $v = (\lambda, \phi)$ has associated LLR values $\alpha_v[i]$ and bit estimates $\beta_v[i]$, where $i \in [0, \Lambda - 1]$. The LLR’s of the root node at $(n, 0)$ are obtained directly from the channel output, and the LLR’s of child nodes $v = (\lambda, \phi)$ are calculated from the parent node $p = (\lambda + 1, \lfloor \frac{\phi}{2} \rfloor)$ and previous branch $u = (\lambda, \phi - 1)$ according to Equation (4). The LLR $\alpha_{(0,i)}$ calculated for a leaf node is the desired $LLR(y_0^{N-1}, \hat{u}_{i-1} \mid \hat{u}^i)$.

$$\alpha_{(n,0)[i]} = LLR(y[i]), \quad i \in [0, N - 1]$$

$$\alpha_v[i] = \begin{cases} f(\alpha_p[i], \alpha_p[i + \Lambda]) & \text{if } \phi \text{ is even} \\ g(\alpha_p[i], \alpha_p[i + \Lambda], \beta_u[i]) & \text{if } \phi \text{ is odd} \end{cases}, \quad i \in [0, \Lambda - 1]$$

(4)

The bit estimates of the leaf nodes at $(0, i)$ correspond to $\hat{u}_i$, and are obtained via a
hard decision on its LLR. The bit estimates of parent nodes \( v = (\lambda, \phi) \) are calculated by propagating those of both the child nodes \( l = (\lambda - 1, 2\phi) \) and \( r = (\lambda - 1, 2\phi + 1) \), as shown in Equation (5).

\[
\beta_{(0,i)}[i] = \begin{cases} 
HD(\alpha_{(0,i)}[i]) & \text{if } i \in A, \ i \in [0, N - 1] \\
0 & \text{otherwise}
\end{cases}
\]

(5)

\[
\beta_v[i] = \beta_l[i] \oplus \beta_r[i], \quad i \in \left[0, \frac{\Lambda}{2} - 1\right]
\]

\[
\beta_v \left[ i + \frac{\Lambda}{2} \right] = \beta_r[i], \quad i \in \left[0, \frac{\Lambda}{2} - 1\right]
\]

**Fast simplified successive cancellation**

The fast simplified successive cancellation (FSSC) decoding algorithm [4] improves upon the computational complexity of the SC decoding algorithm by recognizing constituent codes in the SC decoding tree and pruning the nodes. The four nodes considered are:

- **Rate-0**

Rate-0 (R-0) nodes are the nodes in the SC tree below which all the leaf nodes correspond to frozen bits. For an R-0 node at \( v = (\lambda, \phi) \) in the decoding tree, no further traversal is needed and the bit estimates for the stage can be update as follows:

\[
\beta_v[i] = 0, \quad i \in [0, \Lambda - 1]
\]
• Repetition

Repetition (REP) nodes contain only a single information bit at the rightmost leaf node. The bit estimates for REP node at \( v = (\lambda, \phi) \) in the tree can therefore only be all 0’s or all 1’s, and the decision is made using an efficient ML decoding by:

\[
\beta_v[i] = HD \left( \sum_{k=0}^{\Lambda-1} \alpha_v[k] \right), \quad i \in [0, \Lambda - 1]
\]

• Rate-1

Rate-1 (R-1) nodes are the nodes in the SC tree below which all the leaf nodes correspond to information bits. Similar to R-0 nodes, an R-1 node at \( v = (\lambda, \phi) \) requires no further traversal and the bit estimates for the stage can be updated by taking a hard decision on the stage LLRs:

\[
\beta_v[i] = HD(\alpha_v[i]), \quad i \in [0, \Lambda - 1]
\]

• Single parity check

Single parity check (SPC) nodes contain only a single frozen bit at the leftmost leaf node. The bit estimates for REP node at \( v = (\lambda, \phi) \) in the tree therefore have to satisfy a parity constraint such that the XOR of all the estimates should be 0. This can be achieved by computing the parity of the hard decisions of the REP node LLRs, and then flipping the least reliable estimate if the parity is 1:

\[
\text{parity} = \bigoplus_{k=0}^{\Lambda-1} HD(\alpha_v[k])
\]

\[
j = \arg \min_i |\alpha_v[i]|, \quad i \in [0, \Lambda - 1]
\]

\[
\beta_v[i] = \begin{cases} 
HD(\alpha_v[i]) \oplus \text{parity} & \text{if } i = j \\
HD(\alpha_v[i]) & \text{otherwise}
\end{cases}, \quad i \in [0, \Lambda - 1]
\]
Since the FSSC scheme does not traverse the decoding tree till the leaf nodes, the bit estimates \( \hat{u}_i \) are not readily available. With non-systematic encoding, \( \hat{u}_i \) can be obtained by re-encoding the estimated codeword present in the bit estimates at the root node of the tree, \( \beta_{(n,0)}[i] \), \( i \in [0, N - 1] \). With systematic encoding \([13, 14]\), \( \hat{u}_i \) is directly available in \( \beta_{(n,0)}[i] \), \( i \in [0, N - 1] \).

**Successive cancellation list**

When the SC decoding algorithm encounters an information bit, an immediate decision is made and half the potential remaining paths are discarded from consideration. On the other hand, by considering both possibilities for information bits, ML decoding performance is achieved at the cost of searching through paths that grow exponentially in number. The successive cancellation list (SCL) decoding algorithm \([2, 3]\) is a trade-off between these two extremes in that it limits the number of paths under consideration to a fixed list size \( L \). At each information bit index, the number of paths is doubled. When the number of paths exceeds \( L \), the decoder only considers the \( L \) most reliable paths and discards the rest.

In order to ascertain which paths should remain in the list and which should be discarded, each path is associated with a path metric (PM) that is updated using the LLRs when a decision is made at the leaf nodes for bit index \( i \), as shown in (6) \([15]\).

\[
PM_l = \begin{cases} 
PM_l & \text{if } \hat{u}_i = HD(\alpha_{(0,i)}, l) \\
PM_l + |\alpha_{(0,i), l}| & \text{otherwise}
\end{cases}, \forall l \text{ paths in the list} \quad (6)
\]

After the SCL decoder has estimated all \( N \) bits, the path with the best PM is returned as the decoding output. Results in [3] show a significant improvement in error correction performance by appending a small cyclic redundancy check (CRC) code with the message bits to aid the SCL decoder in choosing the correct path from the final candidates in the list.
Fast simplified successive cancellation list

The FSSC scheme is applied to SCL decoding in [5], by defining the path creation and PM update for an FSSC node $v$ located at $(\lambda, \phi)$ as follows:

- **Rate-0**
  An R-0 node creates no new paths, and the PM’s and node bit estimates are updated according to:

  $$\beta_{v,l}[i] = 0, \ i \in [0, \Lambda - 1]$$
  $$PM_l = PM_l + \sum_{i=0}^{\Lambda-1} HD(\alpha_{v,l}[i]) |\alpha_v[i]|$$

  $\forall l$ paths in the list

- **Repetition**
  REP nodes create only two candidate paths for each path in the list, and the bit estimates and PM updates are given by:

  $$\beta_{v,l}^{(1)}[i] = 0, \ i \in [0, \Lambda - 1]$$
  $$PM_l^{(1)} = PM_l + \sum_{i=0}^{\Lambda-1} HD(\alpha_{v,l}[i]) |\alpha_v[i]|$$

  $\forall l$ paths in the list

  $$\beta_{v,l}^{(2)}[i] = 1, \ i \in [0, \Lambda - 1]$$
  $$PM_l^{(2)} = PM_l + \sum_{i=0}^{\Lambda-1} (1 - HD(\alpha_{v,l}[i])) |\alpha_v[i]|$$
• **Rate-1**

R-1 nodes are limited in the number of paths that are created following the Chase-II decoding algorithm. Each path in the list is extended with the four possible permutations of flipping the hard decisions of the bits at indices \( m_1 \) and \( m_2 \), corresponding to the two least reliable LLR’s. The 4\( L \) paths are then pruned back down to \( L \).

\[
\beta_{e,l}[i] = HD(\alpha_{e,l}[i]) \; , \; i \in [0, \Lambda - 1] \\
PM_l^{(1)} = PM_l
\]

\[
\beta_{e,l}^{(2)}[i] = \begin{cases} 
    HD(\alpha_{e,l}[i]) \oplus 1 & \text{if } i = m_1 \\
    HD(\alpha_{e,l}[i]) & \text{otherwise}
\end{cases} \; , \; i \in [0, \Lambda - 1] \\
PM_l^{(2)} = PM_l + |\alpha_e[m_1]|
\]

\[
\beta_{e,l}^{(3)}[i] = \begin{cases} 
    HD(\alpha_{e,l}[i]) \oplus 1 & \text{if } i = m_2 \\
    HD(\alpha_{e,l}[i]) & \text{otherwise}
\end{cases} \; , \; i \in [0, \Lambda - 1] \\
PM_l^{(3)} = PM_l + |\alpha_e[m_2]|
\]

\[
\beta_{e,l}^{(4)}[i] = \begin{cases} 
    HD(\alpha_{e,l}[i]) \oplus 1 & \text{if } i \in \{m_1, m_2\} \\
    HD(\alpha_{e,l}[i]) & \text{otherwise}
\end{cases} \; , \; i \in [0, \Lambda - 1] \\
PM_l^{(4)} = PM_l + |\alpha_e[m_1]| + |\alpha_e[m_2]|
\]

• **Single parity check**

SPC nodes are more complex than the preceding nodes discussed because all candidate paths created have to pass the parity check of the node. The number of candidate paths created in an SPC node are limited in a manner similar to R-1 nodes. Upon determining the indices \( m_1, m_2, m_3 \) and \( m_4 \) of the four least reliable
LLR’s, there are 16 possible permutations of flipping the hard decisions of the bits at these indices, of which, only the half that satisfy the parity constraint are considered. The SPC node thus creates 8 candidate paths from each path in the list, and the total of $8L$ paths are then pruned down to $L$. The bit estimates and PM update equations for the SPC node are omitted for the sake of brevity, and can be referenced from [5].

**Successive cancellation stack**

The SCL decoder considers $L$ candidate paths for each bit estimate in the codeword, resulting in a total search space of $LN$ paths. At this point, the term *iteration* is defined as a decoder making a leaf node bit estimate for a candidate path. The SC decoder therefore takes $N$ iterations to produce the decoding result, while the SCL decoder takes $NL$ iterations.

The successive cancellation stack (SCS) algorithm [9] is a sequential traversal through the same search space as the SCL decoder. The algorithm begins by extending an initial path following the SC procedure, and updating its PM following Equation (6). At the time of estimating information bits, both candidates are considered and the less reliable path is stored in a *stack* of size $D$ that is assumed to be sufficiently large. As the algorithm proceeds, the number of candidates in the stack grows, and in each iteration only the path with the winning PM is extended.

The stack contains candidates of different lengths, and over the course of decoding if $L$ paths of length $\Omega \in [1, N]$ have been extended, then all paths with length $\omega \leq \Omega$ are removed from the stack [10], thus ensuring the same search space as SCL.

If the winning path has a length of $N$, its bit estimates are returned as the decoding result and the algorithm terminates. Alternatively, the CRC-aided scheme in SCL can be applied to validate the decoded result [10]. If the CRC check fails, the path is removed from the stack and the algorithm continues. By nature of the algorithm, if $L$ paths fail the final CRC check, then all paths are removed from the stack and the algorithm terminates.
An upper bound on the size of the stack is $D = LN$ [10], which is the maximum number of paths the SCS algorithm can investigate. While results in [9, 10, 16–18] show that it is possible to achieve similar error correction performance with much smaller values of $D$ (especially at high SNR’s), there is no general approach to determining the smaller value of $D$ for different code parameters and channel conditions. In SCS implementations where $D$ is less than the upper bound and the stack is full, new candidate paths replace the path with the least reliable PM, and only if the PM of the new path is more reliable itself.

### III Implementation Details

This section introduces the memory layout and decoding schedule implementation for the successive cancellation family of polar decoders, which is then extended to incorporate list decoding. Finally, the stack decoder implementation is discussed.

#### III-A Successive cancellation decoders

The SC and FSSC algorithms make use of the $\alpha$ and $\beta$ memory tree structures shown in Figure 4 to store intermediate LLR calculations and bit propagations. The memory is structured according to the space efficient scheme outlined in [3], and has a spatial complexity $O(N)$ that scales linearly with the code length $N$.

Each stage $\lambda$ in the $\alpha$ memory is only given $\Lambda$ slots of memory - enough to store the LLR’s of a single branch $\phi$. This is possible because upon observing the SC schedule,
Algorithm 1: recursively_calc_α(λ, φ)

1 if \( \lambda = n \) then
2 return
3 if \( \phi \) is even then
4 recursively_calc_α(\( \lambda + 1, \lfloor \frac{\phi}{2} \rfloor \))
5 \( v = (\lambda, \phi) \)
6 \( u = (\lambda, \phi - 1) \)
7 \( p = (\lambda + 1, \lfloor \frac{\phi}{2} \rfloor) \)
8 \( \Lambda = 2^\lambda \)
9 for \( i = 0, 1, \ldots, \Lambda - 1 \) do
10 if \( \phi \) is even then
11 \( \alpha_v[i] = f(\alpha_p[i], \alpha_p[i + \Lambda]) \)
12 else
13 \( \alpha_v[i] = g(\alpha_p[i], \alpha_p[i + \Lambda], \beta_u[i]) \)

one can see that when calculating the LLR’s \( \alpha_v[i] \) at a node \( v = (\lambda, \phi) \), the LLR’s for all branches \( \phi' < \phi \) in the same stage \( \lambda \) will not be used again and can be safely overwritten.

Each stage in the \( \beta \) memory is given \( 2\Lambda \) slots of memory. This is because a stage must store the bit estimates from two child branches in order to update the parent node in the stage above. Once the bit estimates have been propagated, the values can be safely overwritten by subsequent nodes in the stage.

The schedule of operations in the SC decoder is realized at run time using the index \( i \) of the current bit \( \hat{u}_i \) being estimated, by implementing Equations (4) and (5) according to Algorithms 1 and 2 [3].

Computing the FSSC schedule at run time incurs a significant computational penalty since the entire decoding tree has to be traversed to identify the FSSC nodes. The FSSC schedule is therefore created and stored as the decoder is instantiated, which the decoder can then load and loop through for each decoding run. The schedule is stored as operations and the nodes in the tree at which they are performed. Figure 5 illustrates an example of an FSSC schedule created for the SC decoding tree in Figure 3. By abuse of notation, the operations that implement Equations (4) and (5) are denoted by \( \alpha \) and \( \beta \) respectively, and the operations R-0, R-1, REP and SPC implement the equation for the corresponding node.
Algorithm 2: recursively_update_β(λ, φ)

```
1 if φ is even then
2   return
3 v = (λ + 1, ⌊φ/2⌋)
4 l = (λ, φ − 1)
5 r = (λ, φ)
6 Λ = 2λ
7 for i = 0, 1, . . . , Λ − 1 do
8   βv[i] = βl[i] ⊕ βr[i]
9   βv[i + Λ] = βr[i]
10 recursively_update_β(λ + 1, ⌊φ/2⌋)
```

Operation: \quad α \quad \text{REP} \quad \text{α} \quad \text{SPC} \quad β

Node: \quad (2,0) \quad (2,0) \quad (2,1) \quad (2,1) \quad (2,1)

**Figure 5** – FSSC schedule for PC(8, 4) with A = 3, 5, 6, 7.

**III-B List decoders**

The SCL family of decoders extend up to L paths simultaneously, each of which have different values for intermediate LLR’s and bit estimates. The SCL and FSSCL therefore instantiate L copies of the α and a β memory trees from Section III-A, resulting in a spatial complexity of O(LN).

The naive approach to use these memory trees is to duplicate the α and β values for new candidate paths, which results in wasted memory operations for paths that are killed before the values are used.

The authors in [3] propose a lazy-copy scheme in which α and β memory is allocated stage by stage, rather than the tree as a whole, and new candidate paths point to the memory of the parent path that created them. Memory duplication now only occurs when a path needs to modify a stage in memory pointed to by multiple paths, and only that stage is duplicated. The SCL and FSSCL decoders in this work implement a minor modification to the lazy-copy scheme of [3] to support decoding in the LLR domain.
The decoding schedule for SCL and FSSCL is realized in the same manner as outlined for their counterparts SC and FSSC.

III-C Stack decoder

A candidate path that is placed on the stack must store its:

- path metric (PM)
- path length (PL)
- bit estimates \( \hat{u}_i, i \in [0, N - 1] \)
- intermediate \( \alpha \) and \( \beta \) values

The stack is implemented as \( D \) length arrays of these data-structures, and when a path is placed on the stack, it is assigned an index at which to store its values in these arrays. The winning path for each iteration is determined through a linear search on the PM arrays.

The PM and PL arrays are one-dimensional with a space complexity of \( O(D) \), while the bit estimates array is two dimensional with a complexity of \( O(DN) \). The data-structure for the \( \alpha \) and \( \beta \) values follows the same structure as in Figure 4, resulting in a memory complexity of \( O(DN) \). Its usage is also governed by the lazy copy scheme in [3]. Finally, the schedule for SCS is realized following the same Algorithms 1 and 2 as in the SC decoder.

Based on the observation that the SCS decoder extends only one path at a time, a reduced memory scheme (SCS-RM) is proposed in [11] in which only a single copy of the \( \alpha \) and \( \beta \) memory is instantiated. The initial path is created, and as long as there is no path switch, intermediate \( \alpha \) and \( \beta \) values remain valid and the path can continue to be extended. Potential candidates that are created store only their PM, PL and leaf node bit estimates \( \hat{u}_0^{i-1} \), where \( i \) is the current length of the path.
Algorithm 3: Populating $\beta$ memory with a new path $p$

1. for $i = 0, 1, \ldots, PL_p - 1$ do
2. \hspace{1em} $\beta_{0,i}[0] = \hat{u}_p[i]$ 
3. \hspace{1em} recursively_update_\beta(0, i)

Algorithm 4: recursively_calc_\alpha(\lambda, \phi) modified for SCS-RM

1. if $\lambda = n$ then
2. \hspace{1em} return
3. if $\phi$ is even or path has switched then
4. \hspace{1em} recursively_calc_\alpha(\lambda + 1, \psi)
5. \hspace{1em} $v = (\lambda, \phi)$
6. \hspace{1em} $u = (\lambda, \phi - 1)$
7. \hspace{1em} $p = (\lambda + 1, \lfloor \phi/2 \rfloor)$
8. \hspace{1em} $\Lambda = 2^\lambda$
9. for $\beta = 0, 1, \ldots, \Lambda$ do
10. \hspace{1em} if $\phi$ is even then
11. \hspace{2em} $\alpha_v[i] = f(\alpha_p[i], \alpha_p[i + \Lambda])$
12. \hspace{1em} else
13. \hspace{2em} $\alpha_v[i] = g(\alpha_p[i], \alpha_p[i + \Lambda], \beta_u[i])$

A path switch renders the $\alpha$ and $\beta$ memory values invalid, which now have to be recalculated for the new path. This is achieved by first populating the $\beta$ memory with the estimates $\hat{u}_{i-1}^i$, following which the $\alpha$ memory is updated by initiating the calculation of $LLR\left(y_0^{N-1}, \hat{u}_0^{i-1}|\hat{u}^i\right)$ from the channel values at the root node of the decoding tree, rather than from an intermediate stage as dictated by the standard SC decoding procedure. The $\alpha$ and $\beta$ memory can now be used following the traditional SC schedule until the next path switch is encountered, at which point the re-calculation is performed again.

Populating the $\beta$ memory for the newly switched path $p$ uses the same Algorithm 2 defined for the SC schedule. The procedure is highlighted in Algorithm 3, which is performed only once when the path is switched. Recalculating the $\alpha$ memory from the root node requires a minor modification to the SC Algorithm 1, as highlighted in Algorithm 4.
IV Fast simplified stack decoding

The FSSCL scheme of [5] can readily be applied to the SCS decoder. The key difference is that the FSSCL decoder has all candidate paths available at a given node, and is able to prune paths and pick the survivors immediately. In contrast, the FSSCS decoder creates all the candidate paths for the node and places them on the stack, and the paths are either further extended or killed at a later point following the SCS algorithm rules.

Two key implementational details are highlighted, the first of which is that the FSSCS decoder switches between paths at different points in the FSSC schedule. While the path length alone can be used to determine the coordinates of the current node \((\lambda, \phi)\) in the decoding tree, it is not sufficient to determine which FSSC operation \((\alpha, \beta, R-0, R-1, \text{REP or SPC})\) must be performed. To this end, when a path is placed on the stack, it stores an additional parameter - its current progress in the FSSC schedule.

The second detail involves applying the SCS-RM scheme of [11] to the FSSCS decoder, referred to as FSSCS-RM. Since the FSSC scheme does not necessarily traverse down to the root nodes to make bit estimates, it is impossible for the FSSCS-RM decoder to repopulate the \(\beta\) memory via the SCS-RM Algorithm 3. This hurdle is overcome by changing the structure of the \(\beta\) memory of the FSSCS-RM decoder. The work in [19] presents an efficient scheme to compute and store the \(\beta\) values in the context of VLSI design, which is adapted to software in this work.

The \(\beta\) memory is now organized as an array of \(N\) bits as shown in Figure 6a. When a node's bit estimates are made following the FSSCL equations, the estimates are stored directly in the \(\beta\) memory array beginning at the index corresponding to the length of the path. In the case of a \(\beta\) propagation operation, the bits are XOR-ed in place. Figure 6 shows the usage of the \(\beta\) memory for the FSSC schedule of Figure 5. In Figures 6b and 6c, the four bits corresponding to the REP and SPC node respectively are stored at the correct locations, following which Figure 6d shows the \(\beta\) operation performed in place.

The final content of the \(\beta\) memory is the estimated codeword at the root node of the tree, and by using systematic encoding, the estimated message bits are readily available.
Figure 6 – β memory structure and usage in the FSSCS-RM decoder for PC(8, 4).

This leads to the observation that each path on the stack can store the β array directly instead of the bit estimates ˆu_i. An additional advantage is that a path switch in the FSSCS-RM scheme does not need to re-populate the β array, since the propagations are already correctly stored in place.

V Results and discussion

Simulations are performed for PC(1024, 512), and the set of information bit indices A is obtained from the polar code sequence listed in the 3GPP technical specification for the 5G standard [7]. The CRC used in all variants of the SCL and SCS decoders is the 24-bit CRC-24C with a polynomial of 0xB2B117, also provided in [7]. The list parameter L is set to 8 and the stack size D is set to the maximum size NL = 8192 for all decoders.

All code is written in C language and compiled with GCC version 6.3.0 using the -Ofast, -march=native, -funroll-loops and -finline-functions compile flags. α and β values are implemented using 32-bit floating point numbers and 8-bit unsigned integers respectively. Simulations are run using 6 threads on an AMD Ryzen 5 1600 6-Core CPU clocked at 3.2 GHz. The T/P of the decoder is reported as an average per thread, and considering only information bits.

Figure 7a exhibits that the FER performance is maintained for all variants of the stack and list decoders. The slight FER performance degradation in the fast simplified decoders is attributed to the Chase-II approximation used [5].

Figure 7b shows that the baseline T/P of the SCS decoder is, at best, 9 Kbps at an E_b/N_o of 3 dB, which is more than an order of magnitude lower than the SCL T/P of
314 Kbps. The SCS-RM scheme is able to improve the SCS throughput by more than an order of magnitude to 232 Kbps. The FSSCL decoder reports a T/P of 1.22 Mbps, which is four times the T/P of SCL. Finally, applying the fast simplified scheme to SCS decoding results in similar throughput gains as observed with SCL. At an $E_b/N_o$ of 3 dB, FSSCS-RM provides a T/P of 930 Kbps, which is four times the T/P of SCS-RM and two orders of magnitude more than the T/P of the baseline SCS.
VI Conclusion

This report outlines a procedure for applying the fast simplified scheme [5] to the reduced memory stack decoder [11]. Results show that the T/P of the FSSCS-RM decoder is improved by two orders of magnitude over the baseline SCS decoder, from 9 Kbps to 930 Kbps. The FSSCS-RM decoder using the largest stack size achieves the T/P of the FSSCL decoder at practical SNR’s.
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