FPGA and ASIC implementation of reliable and effective architecture for a LTE downlink transmitter

Zhou Wang¹,²a), Bin Wu¹, and Tianchun Ye¹

1 Institute of Microelectronics of Chinese Academy of Sciences, Beijing, P. R. China
2 University of Chinese Academy of Sciences, Beijing, P. R. China
a) wangzhou@ime.ac.cn

Abstract: Hardware implementation of LTE-Advanced systems using FPGA and ASIC technology is a highly promising technology. This article proposed a reliable and effective architecture for a LTE downlink transmitter under different antenna configurations including SISO 1×1; MIMO 2×2. The design has been synthesized using Altera Quartus II 13.1.4 on Altera Stratix-V 5SGSD8K2F40I2. The parameter improving cost is introduced to evaluate the upgrading of resources caused by performance improvement. With this proposed structure, improving cost can be reduced compared with traditional method. The proposed plan is fabricated as an ASIC using SMIC 55-nm CMOS technology. Finally, the design is demonstrated in the test platform, showing a successful performance.

Keywords: LTE, FPGA, ASIC, transmitter

Classification: Integrated circuits

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1 Introduction

Long Term Evolution Advanced (LTE-A) is a useful broadband technology, which provides a reliable multimedia telecommunication link between base-stations and user equipment (UE). Generally, LTE-Advanced is developed so as to meet the diverse requirements of advanced applications designed to become common place of wireless services industry. All these features require performing fast processing and reliable delivery of data signals that brings the substance of data and control signals that specifies the format of the data and the location and timing of the radio resources allocated to the user. And the downlink transmitter is one of the most important part in LTE communication system. FPGA technology is a very usefull method of LTE applying and provide a realiable verifying way of ASIC implement. Besides, ASIC technology can provide the higher speed of calculating and lower power consume.

The growing use of LTE asks for a configurable downlink transmitter architecture that can easily be applied to different performance and complexity requirements. The current research is on the point of the realizing using FPGA. In most implementations, the transmitter processing is achieved on the basic of FPGA and with a low complexity of model which only consists of some parts of transmitter [2, 3]. And they also concentrate on the implementation of one of the channels like PDCCH [4, 5], PDSCH [6] and etc. [7, 8]. However, when updating from single antenna transmitter to two antennas transmitter or four antennas one, the cost of resources increases a lot in current implementation scheme, and it suffers from a lack of a design supporting all downlink channels which means practicability in the whole LTE system. Besides, almost no research has been done to offer details of a design using ASIC technology.

The proposed downlink transmitter using FPGA and ASIC technology is adapting to 3GPP LTE specification R10, which incorporates CRC (Cyclic Redundancy Check) attachment, channel coding, rate matching, scrambling, modulation, layer mapping, precoding, resource elements mapping, IFFT and CP insertion [9].
Besides, we also support all the downlink channels including PDSCH (Physical Downlink Shared Channel), PDCCH (Physical Downlink Control Channel), PCFICH (Physical Control Format Indicator Channel), PHICH (Physical Hybrid ARQ Indicator Channel), PBCH (Physical Broadcast Channel), CRS (Cell-specific Reference Signal), PSS (Primary Synchronization Signal) and SSS (Secondary Synchronization Signal) [10, 11]. What’s the most important, we proposed a structure of transmitter which can reduce the cost of increase of updating from single antenna to two antennas, and this structure can be adapted to multi antennas in LTE system or other communication system. The designs have been synthesized using Altera Quartus II 13.1.4 on Altera Stratix-V 5SGSMD8K2F40I2 and measured in whole platform. As a result, we will compare improved rate of resources with traditional methods. The proposed architecture is fabricated as an ASIC using SMIC 55-nm CMOS technology. Finally, a complete LTE system will be presented to test and verify. The design we proposed is applied to many segment market areas of LTE such as nano base station, IoTs and so on, in which the FPGA plan can provide functional customization services and the ASIC plan can offer lower power consumption, faster speed and smaller implementation area. Moreover, in the foreseeable future, 4G and 5G technologies will coexist for a long time, which means this scheme has a lot of application scene.

The remainder of this paper is organized as follows. Section II describes system design model and the function and VLSI architecture of different module. The corresponding implementation and test results are given in Section III, and we conclude in Section IV.

2 System design model

The LTE physical layer is an immensely efficient means of transmitting both data and control information between an enlarged based station and mobile user equipment. In LTE, two radio frame structures are supported including type1 and type2. Frame structure type 2 is applicable to TDD, and this design applies for TDD. Each radio frame of length $T_f = 307200 / C2$ and $T_s = 10$ ms consists of two half-frames of length $153600 / C2 = 5$ ms each. Each half-frame consists of five subframes of length $30720 \times T_s = 1$ ms.

The normal system model describing the transmitter are shown in Fig. 1. The transmitter will get control information for all the downlink channels in specified
format which will undergo a number of processing. Downlink transmitter incorporates CRC (Cyclic Redundancy Check) attachment, channel coding, rate matching, scrambling, modulation, layer mapping, precoding, resource elements mapping, IFFT and CP insertion.

This paper proposed a kind of system model describing the transmitter in Fig. 2. As for multi-antennas transmitter, this design can save a lot logic expenses in the part of below resource element mapper.

2.1 Cyclic redundancy check attachment

A Cyclic Redundancy Check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. Blocks of data entering these systems get a short check value attached, based on the remainder of a polynomial division of their contents. On retrieval, the calculation is repeated and, in the event the check values do not match, corrective action can be taken against data corruption. LTE defines four kinds of CRC including CRC8, CRC16, CRC24A and CRC24B.

2.2 Channel coding

The purpose of channel coding is to find codes which transmit quickly, contain many valid code words and can correct or at least detect many errors. LTE defines four ways of channel coding. Turbo coding applies for PDSCH, tail biting convolutional applies for PBCH and PDCCH, repeat coding applies for PHICH, scrambling coding applies for PCFICH.

2.3 Rate matching

Rate matching is to make sure coding rate at a low level. In LTE protocol, the input bit sequence to the code block segmentation is denoted by \( b_0, b_1, b_2, b_3, \ldots, b_{B-1} \), where \( B > 0 \). If \( B \) is larger than the maximum code block size 6144, segmentation of the input bit sequence is performed and an additional CRC sequence of \( L = 24 \) bits is attached to each code block. The code block concatenation consists of sequentially concatenating the rate matching outputs for the different code blocks.

2.4 Scrambling

One of the purposes of scrambling process is to reduce the length of strings of zeros and/or ones, which may take place in a transmitted signal, since a long string of 0 s
or a long string of 1 s may cause transmission synchronization problems, i.e. cause the clock regeneration at the receiver to be more difficult. Also, scrambling is done for making the transmitted signal more secured. That is a type of secure on the physical layer. To achieve this, pseudo random gold sequence is generated continuously at the transmitter. The incoming data and gold sequence are logically combined using XOR operation to generate the scrambled bits. Mathematically, it is given by special equation.

2.5 Modulation
For each codeword \( q \), the block of scrambled bits \( \tilde{b}^{(q)}(0), \ldots, \tilde{b}^{(q)}(M_{bit}^{(q)} - 1) \) shall be modulated using one of the modulation schemes in Table II, resulting in a block of complex-valued modulation symbols \( d^{(q)}(0), \ldots, d^{(q)}(M_{symb}^{(q)} - 1) \).

2.6 Layer mapping
The complex-valued modulation symbols for each of the codewords to be transmitted are mapped onto one or several layers. Complex-valued modulation symbols \( d^{(q)}(0), \ldots, d^{(q)}(M_{symb}^{(q)} - 1) \) for codeword \( q \) shall be mapped onto the layers \( x(i) = [x^{(0)}(i) \ldots x^{(v-1)}(i)]^T \), \( i = 0, 1, \ldots, M_{symb}^{layer} - 1 \) where \( v \) is the number of layers and \( M_{symb}^{layer} \) is the number of modulation symbols per layer. In the proposed design, layer mapping supports three types of transmission: single antenna, multiplexing and transmit diversity.

2.6.1 For single antenna transmission, a single layer is used, \( v = 1 \), and the mapping is defined by

\[
x^{(0)}(i) = d^{(0)}(i)
\]

with \( M_{symb}^{layer} = M_{symb}^{(0)} \).

2.6.2 For spatial multiplexing, the layer mapping shall work according to Table I.

| Number of layers | Number of codewords | Codeword-to-layer mapping |
|------------------|----------------------|---------------------------|
| 1                | 1                    | \( x^{(0)}(i) = d^{(0)}(i) \) |
|                  |                      | \( M_{symb}^{layer} = M_{symb}^{(0)} \) |
| 2                | 2                    | \( x^{(0)}(i) = d^{(0)}(i) \) \( x^{(1)}(i) = d^{(1)}(i) \) |
|                  |                      | \( M_{symb}^{layer} = M_{symb}^{(0)} = M_{symb}^{(1)} \) |
| 2                | 1                    | \( x^{(0)}(i) = d^{(0)}(2i) \) \( x^{(0)}(i) = d^{(0)}(2i + 1) \) |
|                  |                      | \( M_{symb}^{layer} = M_{symb}^{(0)}/2 \) |

2.6.3 For transmit diversity, the layer mapping shall be done according to Table II. There is only one codeword and the number of layers \( v \) is equal to the number of antenna ports \( P \) used for transmission of the physical channel.

| Number of layers | Number of codewords | Codeword-to-layer mapping |
|------------------|----------------------|---------------------------|
| 2                | 1                    | \( x^{(0)}(i) = d^{(0)}(2i) \) \( x^{(1)}(i) = d^{(0)}(2i + 1) \) |
|                  |                      | \( M_{symb}^{layer} = M_{symb}^{(0)}/2 \) |
In the proposed design, the codeword will be delivered by serial, so as to only one codeword come in layer mapping as input. The layer mapping for transmission on a single antenna port and spatial multiplexing can be regarded as the same situation. The structure of proposed layer mapping is shown in Fig. 3.

2.7 Precoding

The precoder takes as input a block of vectors $x(i) = [x^{(0)}(i) \ldots x^{(M_{\text{layer}} - 1)}(i)]^T$, $i = 0, 1, \ldots, M_{\text{layer}} - 1$ from the layer mapping and generates a block of vectors $y(i) = [\ldots y^{(i)}(i) \ldots]^T$, $i = 0, 1, \ldots, M_{\text{symb}} - 1$ to be mapped onto resources on each of the antenna ports, where $y^{(p)}(i)$ represents the signal for antenna port $p$.

2.7.1 For single antenna transmission, precoding is defined by

$$y^{(p)}(i) = x^{(0)}(i)$$

where $p \in \{0\}$ and $i = 0, 1, \ldots, M_{\text{symb}} - 1$, $M_{\text{symb}} = M_{\text{layer}}$.

2.7.2 For spatial multiplexing, precoding using antenna ports is only used in combination with layer mapping for spatial multiplexing as described in Table III. In this design, Spatial multiplexing supports two antenna ports and two types of transmission, without cyclic delay diversity (CDD) and large-delay CDD, and the set of antenna ports used is $p \in \{0, 1\}$, respectively.

For without CCD, precoding for spatial multiplexing is defined by

$$
\begin{bmatrix}
  y^{(0)}(i) \\
  \vdots \\
  y^{(P-1)}(i)
\end{bmatrix}
= W(i)
\begin{bmatrix}
  x^{(0)}(i) \\
  \vdots \\
  x^{(M_{\text{symb}} - 1)}(i)
\end{bmatrix}
$$

For large-delay CDD, precoding for spatial multiplexing is defined by

$$
\begin{bmatrix}
  y^{(0)}(i) \\
  \vdots \\
  y^{(P-1)}(i)
\end{bmatrix}
= W(i)D(i)U
\begin{bmatrix}
  x^{(0)}(i) \\
  \vdots \\
  x^{(M_{\text{symb}} - 1)}(i)
\end{bmatrix}
$$

where the precoding matrix $W(i)$ is of size $P \times v$ and $i = 0, 1, \ldots, M_{\text{symb}} - 1$, $M_{\text{symb}} = M_{\text{layer}}$. The values of $W(i)$ shall be selected among the precoder elements in the codebook configured in the eNodeB and the UE. The eNodeB can further confine the precoder selection in the UE to a subset of the elements in the codebook using codebook subset restrictions. The configured codebook shall be selected from Table III. The diagonal size-$v \times v$ matrix $D(i)$ and matrix $U$ are both given by Table IV. For different numbers of layers $v$. 

![Fig. 3. The structure of proposed layer mapping](image-url)
In the proposed precoder for spatial multiplexing, \( x(i) = \left[ x^{(0)}(i) \ldots x^{(u-1)}(i) \right]^T \) will get into by serial, the operation will conduct as follows:

For without CCD, precoding for spatial multiplexing is defined by

\[
y^{(0)}(i) \ldots y^{(P-1)}(i) = W(i) x^{(0)}(i) + \ldots + W(i) x^{(u-1)}(i)
\]

For large-delay CDD, precoding for spatial multiplexing is defined by

\[
y^{(0)}(i) \ldots y^{(P-1)}(i) = W(i) D(i) U x^{(0)}(i) + \ldots + W(i) D(i) U x^{(u-1)}(i)
\]

### Table III. Codebook for transmission on antenna ports \( \{0, 1\} \)

| Codebook index | Number of layers \( \nu \) |
|----------------|-----------------------------|
|                | 1                           | 2                           |
| 0              | \( \frac{1}{\sqrt{2}} \begin{bmatrix} 1 \\ 1 \end{bmatrix} \) | \( \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \) |
| 1              | \( \frac{1}{\sqrt{2}} \begin{bmatrix} 1 \\ -1 \end{bmatrix} \) | \( \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \) |
| 2              | \( \frac{1}{\sqrt{2}} \begin{bmatrix} 1 \\ j \end{bmatrix} \) | \( \frac{1}{2} \begin{bmatrix} 1 & 1 \\ j & -j \end{bmatrix} \) |
| 3              | \( \frac{1}{\sqrt{2}} \begin{bmatrix} 1 \\ -j \end{bmatrix} \) | - |

### Table IV. Large-delay cyclic delay diversity

| Number of layers \( \nu \) | \( U \) | \( D(i) \) |
|-----------------------------|--------|------------|
| 2                           | \( \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ e^{-i\pi/2} & e^{i\pi/2} \end{bmatrix} \) | \( \begin{bmatrix} 1 & 0 \\ 0 & e^{-i\pi/2} \end{bmatrix} \) |

2.7.3 Precoding for transmit diversity is only used in combination with layer mapping for transmit diversity as described in Table II. The precoding operation for transmit diversity is defined for two antenna ports.

For transmission on two antenna ports, \( P \in \{0, 1\} \), the output \( y(i) = [y^{(0)}(i) y^{(1)}(i)]^T \), \( i = 0, 1, \ldots, M^{up}_{\text{symb}} - 1 \) of the precoding operation is defined by

\[
y^{(0)}(2i) \quad y^{(1)}(2i) = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & j & 0 \\ 0 & -1 & 0 & j \end{bmatrix} \begin{bmatrix} \Re(x^{(0)}(i)) \\ \Re(x^{(1)}(i)) \\ \Im(x^{(0)}(i)) \\ \Im(x^{(1)}(i)) \end{bmatrix}
\]

for \( i = 0, 1, \ldots, M^{layer}_{\text{symb}} - 1 \) with \( M^{up}_{\text{symb}} = 2M^{layer}_{\text{symb}} \).
In the proposed precoder for spatial multiplexing, codeword will get into by serial, the independent codeword of spatial multiplexing will complete multiplication and then deliver to next module, and the add operation will be conducted in resource elements mapping. The structure of proposed precoder is shown in Fig. 4.

### 2.8 Resource elements mapping

For each of the antenna ports used for transmission of the physical channel, the block of complex-valued symbols \( y^{(p)}(0), \ldots, y^{(p)}(M_{\text{symb}}^{\text{map}} - 1) \) shall be mapped in sequence starting with \( y^{(p)}(0) \) to resource elements \((k, l)\) which meet differential criteria. The supposed design offers a support of eight physical channels downlink channels including PDSCH, PDCCH, PCFICH, PHICH, PBCH, CRS, PSS and SSS. The mapping to resource elements \((k, l)\) on antenna port \( p \) not reserved for other purposes shall be in increasing order of first the index \( k \) over the assigned physical resource blocks and then the index \( l \), starting with the first slot in a subframe.

In the proposed design, the codewords are delivered by serial will conduct the adding operation, and the intermediate variable and the final output will be stored in the same memory to deduce resource consume. For transmitter, the data of frame need to be prepared one frame in advance. When getting command of mapping over, the module will deliver the data to next processing. The structure of proposed resource elements mapping is shown in Fig. 5.
2.9 IFFT
A fast Fourier transform (FFT) is an algorithm that samples a signal over a period of time (or space) and divides it into its frequency components. IFFT is the reverse p of FFT. As for 20 Mhz LTE downlink transmitter, the point of IFFT is 2048. It needs to interpolate 848 zeros in the middle of the data.

2.10 CP insertion
CP insertion processing is to avoid ICI (Inter Carrier Interference). Besides, this module will rank the real part and imaginary part and then transmitter the data.

3 Results and discussion
Simulated programs are implemented on Altera Stratix-V 5SGSMD8K2F40I2 board using Quartus II 13.1.4 from Altera. This board is useful to estimate the register transfer level (RTL) design, resource utilization and FPGA editor. Here the logic, memory and routing resources available on the FPGA are assigned to the different circuits required for implementation of our design that has been synthesized using Altera synthesis technology tool. Finally, bitstream file is generated which is downloaded on the FPGA.

| Table V. Comparison between proposed design and previous design |
|---------------------------------------------------------------|
| Proposed Implementation | Previous Design [2] |
| Stratix-V 5SGSMD8K2F40I2 | Spartan-6 XC6SLX452CSG324 |
| Resource | | Virtex-5 XC5VLX220TFFF1738 |
| Single Antenna | Two Antennas | Improving cost | Single Antenna | Two Antennas | Improving cost | Single Antenna | Two Antennas | Improving cost |
| Registers | 28344 | 35608 | 125.63% | 1004 | 1469 | 146.31% | 880 | 1340 | 152.27% |
| LUTs | 35608 | 38905 | 109.26% | 777 | 1103 | 141.96% | 653 | 984 | 150.69% |
| RAM/ FIFO | 1844174 | 1854870 | 100.58% | 1 | 2 | 200% | 2 | 4 | 200% |
| DSP | 151 | 152 | 100.66% | 2 | 4 | 200% | 2 | 4 | 200% |
| Channels | PDCCH PCFICH PHICH PBCH PDSCH CRS PSS SSS | PDCCH | PDCCH |

The resource estimation of synthesizing presented designs using Altera synthesis technology tool on Stratix-V B board for transmitter with the two presented configurations: SISO: 1 x 1 and MIMO: 2 x 2 antennas are shown in the Table V.

It can be observed that the number of the used registers, LUTs, and DSP Arithmetic increased with increasing in the number of antennas. In Table IV, the proposed implementation is compared with previous downlink transmitter for LTE, i.e., the designs of M. A. Mohamed et al. [2]. The improving cost means the cost ratio of resources from single antenna transmitter to two antennas transmitter. As for the structure and implementation of single antenna transmitter, it is shown in Section II that we follow the principles of simple and efficient design as far as possible and the single antenna design can work successfully. We carefully compare the resource overhead of the single antenna and two antennas schemes based on the same principles of realization, and the precise data display results have very high logical consistency and accuracy with proposed scheme. As we can see,
by this reliable and effective architecture the proposed implementation has a lower improve rating. The improving cost of registers is 125.63% which is lower than 146.31% in Spartan-6 implementation and 152.27% in Virtex-5 implementation in [2]. And the improving cost of LUT is 125.63% comparing to 141.96% in Spartan-6 implementation and 150.69% in Virtex-5 implementation. The improving cost of RAM/FIFO and DSP is respectively 100.58% and 100.66% nearly invariant which is great lower than 200% both in Spartan-6 implementation and Virtex-5 implementation. The comparison shows the proposed design use less resources consume rate from one antenna updating to two antennas.

In this part, the test platform as shown in Fig. 6 is conducted to test and verify the LTE downlink transmitter. The independent RF module is produced to connect with FPGA to generate wireless signals. The FPGA can complete circuit operation, and the PCIe (Peripheral Component Interface Express) allows guest operating and delivering commands on PC. To validate the function of the downlink transmitter, we use ROHDE&SCHWARZ spectrum analyzer installing LTE kit to receive the signals. As a result, we can see the analyzer get the right data successfully.

The proposed architecture is fabricated as an ASIC using SMIC 55-nm CMOS technology, and the chip area. The Fig. 7 shows the ASIC physical design, and the Fig. 8 shows the entity of the chip. The whole chip area is $4.4 \times 4.3$ mm, and the part of transmitter is nearly $4.4 \times 1.5$ mm.
To validate the function of the downlink transmitter ASIC chip, we conduct the test platform. The independent RF module and MAC module are produced to connect with ASIC to generate whole LTE equipment as Fig. 9 shows. The signals and data can be proved by ROHDE&SCHWARZ spectrum analyzer installing LTE kit in Fig. 10.

4 Conclusion

Finally, the LTE downlink transmitter of the all channels under different antenna configurations using FPGA technology and ASIC technology were implemented successfully. The processing of downlink transmitter incorporates CRC attachment, channel coding, rate matching, scrambling, modulation, layer mapping, precoding, resource elements mapping, IFFT and CP insertion. Designs have been synthesized using Altera Quartus II 13.1.4 on Altera Stratix-V 5SGSMD8K2F40I2 and measured in whole platform. With the proposed structure, improved rate of resources can be reduced a lot compared with traditional method. The ASIC was fabricated in
55nm CMOS technology. In the end, the design is demonstrated in the test environment, showing a successful performance. This proposed structure can be adapted to multi antennas in LTE system or other communication system, which can lead to lower improving cost in diversified application scene.

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