Packing identical simple polygons is NP-hard

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Abstract
Given a small polygon $S$, a big simple polygon $B$ and a positive integer $k$, it is shown to be NP-hard to determine whether $k$ copies of the small polygon (allowing translation and rotation) can be placed in the big polygon without overlap. Previous NP-hardness results were only known in the case where the big polygon is allowed to be non-simple. A novel reduction from PLANAR-CIRCUIT-SAT is presented where a small polygon is constructed to encode the entire circuit.

1 Introduction

Packing is a fundamental problem in computational geometry. In this paper we study the problem of packing multiple copies of a small object inside a big object:

Problem 1 (Simple Polygon Packing). Given a small simple polygon $S$, a big simple polygon $B$, and a positive integer $k$, is it possible to place $k$ copies (allowing translation and rotation) of the small polygon inside the big polygon without overlap?

This problem was heretofore neither known to be in P, nor in NP, nor to be NP-hard. Here we show Problem 1 is NP-hard. Several results are known about closely related variants of Problem 1:

Multiple small polygons. If there is not one small polygon, but rather a set of multiple small polygons, the problem is trivially NP-hard, even in one dimension.

Big polygon is non-simple. If the big polygon is non-simple (i.e. it has holes), packing has been shown to be NP-hard even if the small polygon is a square [5].

Small polygon is a square. If the small polygon is a $2 \times 2$ square and all boundaries both the big and the small polygons in a packing are restricted to be on the unit grid, then the problem was shown to be in NP [4].

Orthogonal rotation. If orthogonal rotation is allowed, the problem is not known to be in NP, even if both the small and big polygons are rectangles. This is known as the pallet loading problem, and appears as problem 55 on the Open Problems Project [2].

Our result is the first to establish the hardness of packing of multiple copies of a simple polygon inside another simple polygon. Previous reductions for related problems fall into two categories. In the case of multiple small polygons, a reduction from KNAPSACK or PARTITION is easy. In the case of having a nonsimple big polygon, the reduction in [5] is from PLANAR-CIRCUIT-SAT. Such a reduction creates a big polygon which is essentially a drawing of the circuit, where the interior of the big polygon represents the wires and the gates, but where there are holes between all of the wires. Without the ability to literally create a big polygon that uses holes to create a circuit drawing, nothing was known. Our construction is also a reduction from PLANAR-CIRCUIT-SAT, but in a completely different manner. Previously the circuit was encoded in the big polygon; our big polygon is independent of all aspects of the circuit, other than the circuit size, while the circuit is encoded entirely in the small polygon.
However, because our construction creates a small polygon which is nonconvex and nonconstant in size (the size is polynomial), there remains a range of open problems relating to the packing of identical polygons. The simplest such variation (most likely to be in P) would be: given as the big polygon an orthogonally convex simple polygon drawn on a unit grid, how many grid-aligned $2 \times 2$ unit squares can be packed? (This is a slightly easier variant of problem 56 on the Open Problems Project [2]). The problem is known to be in P only if the big polygon is further restricted to be pyramidal [3]. Harder variants of what are unknown to be in P or NP-hard include limiting the inside or outside polygons to be convex or of constant complexity.

2 Planar circuit satisfiability on a grid

Our reduction is from a problem we call Planar-Grid-SAT: which is designed for the ease of presentation of the reduction of [3]

Problem 2 (Planar-Grid-SAT). The input is an integer $n$ and a classification of the edges on an $n \times m$ grid such that some of the edges of the grid are designated to be wires, other edges are designated to be inverters, and some pairs of adjacent horizontal edges where the rightmost vertex of the three has an odd $x$ coordinate are called AND gates. Those edges which are unclassified are referred to as don’t cares. The input is satisfiable if and only if there is an assignment of True or False to every vertex on the grid such that

- vertices connected by a wire have the same truth value,
- vertices connected by an inverter have different truth values,
- For three vertices connected by an AND gate, the truth value of the right vertex is the logical AND of the middle and left vertex, and
- The upper-left vertex has a truth value of True.

The NP-hardness of determining whether an instance of Planar-Grid-SAT is satisfiable follows from the NP-hardness of Planar-Circuit-SAT and the fact that any planar graph can be drawn on a polynomial size grid [1]; the location restriction of the AND gates is trivial to enforce through expansion of the grid size by a constant factor. Planar-Circuit-SAT itself is known to be NP-hard via a well-known reduction from Circuit-SAT, where overlapping wires in a non-planar drawing of a circuit can be implemented in an equivalent planar circuit through the appropriate use of three XOR gates (for an illustration of this construction see, for example, §3.2.3 of [6]).

3 Reduction

Due to the complexity of the reduction, it is presented in several phases of increasing complexity. In the first three phases (§3.1-3.3) we simply present big and small polygons, such that for a particular $k$ the packing of $k$ small polygons inside the big one is unique. In §3.4 we add a small degree of discrete flexibility to how the small polygons can be packed; each small polygon will represent a vertex in an instance of Planar-Grid-SAT, and this flexibility represents the truth value of that vertex. Finally, in §3.5 we restrict the flexibility of the positions of the small polygons granted in the previous phase to that which represents truth assignments to the vertices which are allowable in the given instance of Planar-Grid-Sat.

3.1 Squares in a rectangle

We begin with the obvious:

Fact 1. Given a $n \times m$ rectangle as the big polygon, and a unit square as the small polygon, there is a unique way to pack $nm$ copies of the small polygon in the big polygon.
Figure 1: Illustration of the graduated grid packing. The colored polygons are all identical, and the interior boundary of the black region is the big polygon. For a closeup of the horizontal protrusion, see Figure 3.1.
3.2 Protrusions, inclusions, and a progression of whitespace

In this phase we maintain the unique packing, but add some whitespace to the solution; see Figure 3.2. Additionally, the small polygon, while still roughly square-shaped has two protrusions, horizontal and vertical, and two matching inclusions. The big polygon also now has inclusions and protrusions which force the location of where each row and column of the squares line up. The whitespace is chosen so that the distance between each row and column increases linearly as one proceeds down and to the right. Additionally, the total whitespace is chosen to have a total area of less than 1, thus making it obvious that the packing of nm small polygons is unique.

Observe that each inclusion has n notches. Also observe that by construction, in a given small polygon, the vertical notch which the protrusion from above occupies is a graphical representation of the y coordinate of the small polygon in the grid of packed small polygons. Symmetrically, the horizontal notch occupied is a graphical representation of the horizontal position within the grid; see Figure 3.2.

This is a good first step of making a polygon “aware” of its location, however, we would like to be able to make the notch a neighboring protrusion occupies a function of the small polygon’s horizontal and vertical positions; currently the notch is a function of the horizontal or the vertical position.

3.3 The nailer

In this phase the location of each small polygon in a packing of nm of them remains exactly the same as in the previous one. The only change is that a protrusion (called the nail) is added heading down and to the right from the bottom right corner of each small polygon, and a matching inclusion (called the nailer) is built on the upper left portion of each polygon so that the nail never overlaps a neighboring small polygon. Observe that the nailer has nm notches, arranged in an m \times n grid, and for each small polygon’s nailer, the notch occupied by a neighboring polygon’s nail is unique for each small polygon and is a graphical representation of both the horizontal and vertical position of the small polygon in the grid of packed small polygons. Thus, we have for the first time have a local part of each small polygon’s packing which is uniquely determined by its position, both horizontal and vertical. This will be exploited further in the next step.

3.4 Refining the nailer—microshifts and subnotches

Recall that since § 3.2, the horizontal notch occupied is the horizontal position and the vertical notch occupied is the vertical position. In this phase we make several changes:

- We refine each of the n horizontal notches in the horizontal inclusion into m micronotches, where m represents the number of vertical notches. Thus the horizontal inclusion now has nm micronotches, which are arranged in n groups of m. See Figure 2 for an illustration of this and Figure 3.4 for a closeup of the nailer. Formerly, the occupied notch represented the horizontal location; now the micronotch group uniquely determines the horizontal coordinate, and the micronotch within the group will uniquely determine the vertical coordinate within the group. Symmetric changes are performed in the vertical protrusion and inclusions.

- We shrink the horizontal and vertical protrusions so that they fit in the micronotches.

- We make small shifts in the inclusions of the nailer, so that the horizontal and vertical probes uniquely fit in the appropriate micronotch. For an illustration of the resultant nailer see Figure 3.4.

The resulting packing of nm small polygons remains unique. The reason is that while the horizontal and vertical protrusions have more wiggle room than in the previous phases, this wiggle room is chosen to be less than the distance between the notches in the nailer, thus the nail is nailed in the nailer in a unique way which fixes the position uniquely and establishes the correct positioning of the protrusions in the micronotches.
Figure 2: Illustration of the nailer and the nail. Notice how in each small polygon the nail nails the nailer in a different notch. See Figure 3.4 for a closeup of the nailer. (Note that in a PDF viewer, the reader is encouraged to zoom in to explore the details)
Figure 3: Nailer closeup. The notch that the nail will end up in is uniquely determined by the position of the small polygon. Observe how the heights and horizontal alignment of each notch is different, this ensures the desired micronotch placement.

Figure 4: Horizontal inclusion closeup.

Figure 5: Horizontal inclusion closeup, showing the micronotches arranged in groups. Compare to Figure 3.4.
3.5 Adding states

The last phase left us with a construction whereby the packing of \(nm\) small polygons was unique, and that for each of the small polygons the micronotch occupied was unique. In order to implement a circuit, establishing this location awareness among identical objects is crucial, but now we must add a degree of flexibility which will allow a discrete degree of flexibility on the location where each small polygon is packed. The state of a small polygon in a packing will be represented by a vertical shift. The size of this shift is relatively small compared to the size of a unit square, and relatively large compared to the nailer. We modify the construction of the previous phase to create several vertically translated copies of the horizontal and vertical inclusions and nailer. This is illustrated in Figure 3.5.

To have a small polygon represent a node in the circuit in a given instance of PLANAR-GRID-SAT, we need to know if a given small polygon represents a true or a false state. For technical reasons explained below we also need to know if the polygon is currently in an even or odd numbered column. Finally, since the right node of an AND gate in an instance of PLANAR-GRID-SAT is a function of the truth states of not just the neighbor to the left, but two neighbors to the left we will need to encode in the state the truth value of the left neighbor; for simplicity we only encode this for even columns. This gives the six states listed in in Table 1. We assign each state a shift value according to an exponential progression, with the largest shift being 31 times the smallest. The reason this exponential progression is chosen is so that if two adjacent small polygons are in different states, the horizontal difference between them will uniquely determine their states. Observe that if there is no horizontal difference between adjacent small polygons, we know that they are in the same state, but we do not know which state that is; this is the reason for also encoding the columnar parity, as this means that having two horizontally adjacent small polygons in the same state is forbidden.

Thus, in a given small polygon, the horizontal protrusion from the left neighbor will go into a single micronotch (vertical coordinate) in a group of notches (horizontal coordinate) in a copy of the horizontal protrusion which indicates the shift difference between the given small polygon and the polygon to the left. As this shift difference encodes the states of both the given polygon and the polygon to the left, the exact micronotch occupied by the protrusion of the polygon to the left will be a unique function of the location of the given small polygon, its truth value, the truth value of the polygon to the left, and the truth value of the polygon two to the left (if the given polygon is in an odd column). Based on all of this information, it can be determined if the micronotch occupied represents a truth assignment that is consistent with the given instance of PLANAR-GRID-SAT. For example, if there were a wire connecting the node representing the current polygon to the node representing the one to the left, then we want to allow the grid packing of \(nm\) small polygons only if the two polygons have the same truth value. This can easily be done by removing the micronotches that do not correspond to this condition. Our construction ensures that by keeping or removing micronotches in the small polygon, we can allow a packing of \(nm\) small polygons if and only if the circuit is satisfied. Table 2 indicates how we can choose which horizontal micronotches to keep as a function of the circuit element being represented. Programming the vertical micronotches is slightly easier, since all AND gates are represented horizontally; Table 3 has the relevant information for vertical micronotch selection.

The large polygon is, in essence, created in the same manner as an enclosing ring of small polygons; the micronotches are encoded such that the interface between the big polygon and small polygons pack inside is a don’t care, except for at the upper-true where a TRUE condition is enforced. This corresponds to enforcing that the circuit be satisfied.

Thus we can summarize the result of the construction in this theorem:

**Theorem 1.** Given an instance of PLANAR-GRID-SAT on an \(n \times m\) circuit, the construction of this section yields a small polygon \(S\) and a large polygon \(B\) such that \(nm\) small polygons can be packed in the large polygon in a grid-like manner if and only if their shifts represent truth values which are consistent with the circuit diagram.
Table 1: Description of states

| Shift Amount | Abbreviation | Description of State |
|--------------|--------------|----------------------|
| 0            | OT           | Odd column, truth value of True |
| 1            | OF           | Odd column, truth value of False |
| 3            | ETT          | Even column, truth value of True, polygon to the left is True |
| 7            | ETF          | Even column, truth value of False, polygon to the left is True |
| 15           | EFT          | Even column, truth value of True, polygon to the left is False |
| 31           | EFF          | Even column, truth value of False, polygon to the left is False |

Table 2: Horizontal micronotch programming. This programs the relationship between horizontally adjacent blocks as a function of the parity of their column and the part of the circuit diagram they are representing. Only transitions from even to odd or vice-versa are allowed as the column parity of adjacent columns must be different. Micronotches should only be present when they represent a node in the circuit with the given difference which in the given instance of Planar-Grid-SAT has a logical element allowed by the programming function. Allowed micronotches are designated by a ◦ in the above table.
Figure 6: To introduce the concept of states, the horizontal and vertical inclusions as well as the nailer are copied several times. In this figure we illustrate three copies. We allow the small polygons to be packed either next to the polygon to their left, or above or below; this will determine which of the shifted inclusions is used. This is a simplification of the construction of the text, where the small polygons could be shifted in six ways, with a ratio of 31 between the large and the small shift, and the number copies of the inclusions being 63 instead of three. Also note that for ease of viewing the whitespace and other visual elements have been exaggerated dramatically; the total whitespace should be smaller than a single small polygon, and all inclusions should be much smaller and horizontally distant from the exterior of the small polygons.
### Vertical Micronotch Programming

| Difference | Transition | Even column | Odd column |
|------------|------------|-------------|------------|
|            | Wire       | Inverter    | Don’t care | Wire       | Inverter    | Don’t care |
| -28        | EFF → ETT  | o           | o          |            |             |            |
| -24        | EFF → ETF  | o           | o          |            |             |            |
| -16        | EFF → EFT  | o           | o          |            |             |            |
| -12        | EFT → ETT  | o           | o          |            |             |            |
| -8         | EFT → ETF  | o           | o          |            |             |            |
| -4         | ETF → ETT  | o           | o          |            |             |            |
| -1         | OF → OT    |             | o          | o          |             |            |
| 0          | EFT → EFT  | o           | o          | EFF → EFF  | o           | o          |
|            | ETF → EFT  | o           | o          | OF → OF    | o           | o          |
|            | ETT → ETT  | o           | o          | OF → OT    | o           | o          |
| 1          | OT → OF    | o           | o          |            |             |            |
| 4          | ETT → ETF  | o           | o          |            |             |            |
| 8          | ETF → EFT  | o           | o          |            |             |            |
| 12         | ETT → EFT  | o           | o          |            |             |            |
| 16         | EFT → EFF  | o           | o          |            |             |            |
| 24         | ETF → EFF  | o           | o          |            |             |            |
| 28         | ETT → EFF  | o           | o          |            |             |            |

Table 3: Vertical micronotch programming. This programs the relationship between vertically adjacent blocks as a function of the parity of their column and the part of the circuit diagram they are representing.

Figure 7: States. This closeup shows the middle polygon is in a different state from its neighbors.
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