Emerging Spintronics Phenomena and Applications

Rahul Mishra and Hyunsoo Yang

Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117576.

Development of future sensor, memory, and computing nanodevices based on novel physical concepts is one of the significant research endeavors in solid-state research. The field of spintronics is one such promising area of nanoelectronics which uses both the charge and spin of an electron for device operations. The advantage offered by the spin systems is in their non-volatility and low-power functionality. This article reviews the emerging spintronic phenomena and the research advancements in diverse spin-based applications. Spin devices and systems for logic, memories, emerging computing schemes, flexible electronics, and terahertz emitters are discussed in this report.

Index Terms—Magnetics, magnetic devices, magnetoelectronics, spintronics.

I. INTRODUCTION

CONVENTIONAL sensor, memory, and computing electronics exploit the charge of an electron for their operations. However, along with charge, an electron is also characterized by its spin angular momentum or spin. It is the spin of an electron that manifests in the form of magnetism that we see in magnetic objects of the macro world. In the information technology age, magnetism has found industry applications in the massive digital data storage. The field of spintronics is centered on the electron’s spin in conjunction with its charge. As we near the end of a several decade scaling of complementary metal–oxide–semiconductor (CMOS) technologies due to fundamental physical limitations, using the degree of spin freedom might be a natural choice for next-generation technologies. An external energy source is not required for maintaining a particular spin or magnetic state in a spintronic device. This property makes spintronic devices non-volatile and low power-consuming, and hence attractive for the emerging era of mobile, wireless, and scaled down electronic applications.

The validation of spintronics as an imperative field to pursue was propelled with the discoveries of giant magnetoresistance (GMR) [1], [2] and tunneling magnetoresistance (TMR) [3], [4]. In these findings, it was put forward that a thin magnetic multilayer has a higher (lower) resistance when the magnetization of individual layers is aligned anti-parallel (parallel) to each other. Eventually, these structures were incorporated in the read head of hard disks, where their scalability has resulted in ultrahigh storage density. Presently, the read heads are based on the magnetic tunnel junction (MTJ) in which the spacer layer between the two ferromagnetic layers is typically an oxide such as MgO. While in a magnetic disk storage the read-MTJ is toggled by the magnetic field emanating from the bits on the disk, a more efficient and scalable way to process the information. The information is transferred by the microprocessors. These computing units use miniaturized solid-state elements, that is, MOS to transfer and store the information. The information processing capacity of a typical processor has been continuously increasing since its inception in early 1970s. This has been majorly due to aggressive scaling of the underlying CMOS technology which resulted in packing numerous functions in a given processor area [11]. However, the processor performance improvement has recently plateaued, partially due to increasing power density. Spintronic devices offer a potential solution to this problem by offering reduced power consumption owing to their non-volatile nature [12]–[14].

The Datta and Das transistor is among the very first proposed spin logic device [15]. The suggested structure...
as illustrated in Fig. 1(a) consists of a spin polarizer and an analyzer (a magnet) connected by a non-magnet (NM) which has spin–orbit coupling (SOC). The application of an electric field on the SOC channel results in precession of spin of the electrons that are injected from the polarizer. The precession of spin is a consequence of the Rashba effect which dictates the manifestation of the electric field into the magnetic field in a moving electron’s frame of reference [16]. The phase of the injected spin can therefore be controlled by a gate voltage applied on top of the channel. On arrival at the analyzer, if the electron’s spin is in-phase (out-of-phase) with the analyzer’s magnetization, it will result in a low (high) channel resistance corresponding to the “ON (OFF)” state of the transistor. However, the use of phase makes it difficult for implementing logic circuits, because the phase is very sensitive to a continuous variable and not a discrete binary one. Therefore, phase information may be more suitable for sensors which deal with analog output values.

Till date, a fully functional spin field-effect transistor (spin-FET) has not been realized due to the non-ideality of the polarizer and analyzer layer and the scattering process in solids which randomizes the spins [17]. However, there have been few demonstrations of gate-induced spin precession and their subsequent detection in 2-D electron gas (2-DEG) systems. For example, Koo et al. [18] have detected spin precession in an InAs high-electron mobility channel. NiFe electrodes were used as the spin injector and detector in this configuration [see Fig. 1(b)]. As shown in Fig. 1(c), an oscillatory modulation of channel conduction was observed when the magnetization of the polarizer and analyzer was aligned along the channel direction (black curve). It should be noted that with the magnetization aligned along an in-plane direction transverse to the channel, there was no spin precession as the Rashba field and injected spins are collinear (red curve). It was later shown that spins injected using circularly polarized lights can also be modulated using a top gate and be detected using the spin Hall effect (SHE) [19]. Recently, spins injected electrically using a magnetic layer were detected in a similar way using the inverse spin Hall effect (ISHE) [20].

While the spin-FET emulates the functionality of a conventional MOSFET, numerous other spin logic devices which exploit alternate magnetic properties have been realized. One such scheme uses the magnetic domain wall (DW) and its motion to transfer information [21]–[24]. A magnetic DW is the interface between two oppositely aligned magnetic regions which moves either along or opposite to an applied magnetic field. The motion of DW around a corner in the presence of a rotating magnetic field has been used to implement the NOT gate as shown in Fig. 2(a) [25]. A nanowire is patterned in the form of a cusp with its either side serving as the input and output terminal of the NOT gate. The magnetization direction with respect to the DW motion direction represents the two logic states. A magnetic field is rotated in the anticlockwise direction as shown in Fig. 2(a). A DW that is present at a point P with the magnetization aligned along the +x-direction on its left side (representing input of logic “1”) moves along the first corner of the cusp to the point Q when the magnetic field is rotated from the +x-direction to the +y-direction. In the next cycle of magnetic field rotation from the +y-direction to the −x-direction, the DW moves to the point R. However, on arrival at the point R, the direction of the magnetization of the left of DW is now toward the −x-direction due to the continuity of the magnetization in the cusp. A logic “1” input is thereby converted to logic “0” in a half-cycle of magnetic field rotation. The rotating magnetic field in effect serves as a clock signal. The input and output traces of the NOT gate obtained using the magneto-optic Kerr effect (MOKE) are shown in Fig. 2(b). It should be noted that there is a propagation delay of half clock cycle from the input to the output as explained previously. Shift registers were also implemented by patterning many such cusps adjacent to each other. Several other nano-patterning schemes have been used to implement the NOT gate [23], AND gate [21], buffer [26], and SHIFT registers [24]. The DWs in these devices are either moved with the help of the magnetic field or using spin current. A big disadvantage of the DW-based logic is the need for an external magnetic field to move the DW, which also prevents individual controllability of each DW in a device with multiple DWs. This hinders their scaling for practical applications. Ideally, the DW-based logic gates can be designed such that the DWs can be moved by currents instead of the magnetic fields. Another drawback of the DW-based logic is the size of DW which can be anywhere between 7 and 100 nm. Therefore, the device containing these DW will be even larger. In comparison, the CMOS technology is already mass producing the 7 nm node technology and approaching the 5 nm node in the coming years. The DWs are also prone to
pinning due to inhomogeneity of the patterned channel, which can cause reliability issues.

Another scheme of implementing spintronic logic is via switching of the bistable magnetic element. The two stable states of a magnet represent binary information. Behin-Aein et al. [27] proposed one such implementation in which the spin information can be transferred using the spin current from one magnetic element to another. In their proposed scheme shown in Fig. 3(a), a voltage $V_{\text{supply}}$ is used to apply spin-torques to position the output magnetic bit in a neutral state (high-energy) which lies between the two stable states (low-energy). An application of a $V_{\text{bias}}$ signal which is relatively small compared with $V_{\text{supply}}$ transmits the information from the input magnet to the output magnet through the channel. A semiconductor spin channel can be used as an interconnect as it supports a longer spin coherence length. In the presence of both $V_{\text{supply}}$ and $V_{\text{bias}}$, the output magnet switches in either of the stable states depending on the state of the input bit. The information from few of these input magnets can be combined to implement logic functions like AND/OR.

While the scheme of magnetic logic was proposed almost a decade back, an experimental demonstration of such a device has not been shown yet. The proposal relies on ideal behaviors of the magnets, spin currents, and spin channels. While a metallic channel is an ideal choice for interconnect due to their low resistance, the small spin coherence length in metals will result in a loss of information before it is transferred from one magnet to another. Although a semiconducting channel supports a longer spin coherence length, the resistance mismatch between the ferromagnet (FM) and semiconductor makes the spin transfer efficiency very low. In addition, the superposition of spin currents coming from various inputs will highly depend on the interconnect length. Therefore, interconnects have to be designed precisely to obtain the desired functionality, which may lead to scalability issues for a large number of logic array operation.

Bhowmik et al. [28] demonstrated that the spin current generated using the SHE in a NM such as Ta and Pt can perform the clocking function. In their work, the magnetization state of an input magnet was used to control the final state of three nano-magnets as illustrated in Fig. 3(b). When the input magnet is set in the up (down) magnetization direction, the final state of the three bits stabilizes in the down–up–down (up–down–up) configuration. The three nano-magnets which have dipole coupling between them change their state only when a charge current is passed through the underlying Ta layer, hence the clocking function.

The current-induced magnetization switching using SOT (refer to Section III for details on SOTs) occurs above a certain threshold value of current density. This property has also been used to build the logic functions. An SOT device with two inputs in the form of current acts as an AND gate. The final magnetization state of the magnet represents the output. The individual value of each current input is maintained below the threshold switching current of the device to achieve the AND
functionality [29]. The direction and magnitude of the assist magnetic field were used to construct other logic functions such as OR, NAND, and NOR. For example, to implement an OR gate, the magnitude of the assist field was increased such that the threshold switching current decreases below the individual input current values. This results in switching of the magnetization for all the input values except when both the inputs are zero, thereby emulating an OR gate.

SOT devices which show a voltage control of magnetic anisotropy (VCMA) [30] have also been used to implement the spin logic. The VCMA in these devices modulates the threshold switching current of the magnet [31] (see Fig. 4). A multifunctional OR/AND gate was implemented using a single device depending on the initial magnetization states as shown in Fig. 4(c) and (d). The switching current and gate voltage act as the two input parameters, while the output was measured using the anomalous Hall resistance ($R_{xy}$). These logic devices, however, have limited fan-out as the readout is carried using the anomalous Hall resistance. Again, device-to-device variation normally results in different threshold currents for different devices. The proposed device also requires an assist magnetic field which makes scalability difficult.

Spin waves which represent propagating disturbance in a magnetic material have also been proposed as a viable means to construct the spin logic. The spin waves act as information carrier and their phase can be varied by a magnetic field produced by current passing through a waveguide [32], [33]. Spin waves from different sources add up constructively or destructively depending on the input current values to realize Boolean functionalities. However, since the phase of the spin wave is prone to disturbance from magnetic inhomogeneity and imperfections, it has been proposed to use the wave amplitude instead [34], [35]. The nonreciprocity of spin wave magnitude for the opposite propagation direction can be exploited to implement a simple inverter or pass gates [34]. A larger value of nonreciprocity corresponds to a larger readout margin. It was shown that a Ta/Pt bilayer system shows a giant nonreciprocity factor (the ratio of spin wave amplitude at positive and negative field) of $\sim 14$ (60 in the frequency domain) for the Ta thickness of 8.2 nm as shown in Fig. 5 [36]. The spin-wave-based logic is still in a very preliminary stage. In comparison to charge currents, spin waves are a very weak information carrier. Sustaining reliable and long-distance transfer of information using spin waves requires specific magnetic materials. The demonstration of the spin-wave-based logic network is yet to be seen due to these limitations and requirements.

Magnetic logic devices using skyrmions [37]–[39], which are topological spin states, have been proposed. Skyrmions can either be driven by the magnetic field or spin currents while they can be manipulated by dynamically modulating properties of the magnetic films using the electric field [40].
In one such scheme, this skyrmion behavior was used to simulate a skyrmion transistor. In the proposed transistor, the skyrmions were driven by a spin current from one end of the spin channel to another. A gate in between the channel was used to annihilate the skyrmion by modulating the anisotropy of the magnetic film under it, resulting in transistor “OFF” operation [41]. A hybrid structure based on skyrmion and DW has been put forward [42]. The DW and the skyrmion can be interconverted by designing magnetic channels of different widths. By designing specific nanostructures that duplicate, merge, or annihilate skyrmions logic gates functionalities can be achieved [43]. While the skyrmion logic devices are promising, they are still in a conceptual and simulation stage. An experimental demonstration of their functionality and scalability is awaited with interest.

As we see in this section, there have been multiple proposal and demonstration of spin logic devices and systems; however, these implementations still have a long way to go before they compete with CMOS logic. The normal propagation delay of any conventional CMOS logic gate is generally few picoseconds. In comparison, the delay or speed of typical spin devices is limited to nanoseconds or gigahertz, respectively. The advantage offered by spintronics is, however, their non-volatile nature which can save a tremendous amount of power during data processing, as circuit blocks in execution pipeline but not being executed can be switched off. Interconnects is a big issue in all spin logic circuits. An ideal interconnect should be able to transfer the spin information over long distances. However, in reality, the spin interconnects made up of metals have relatively short spin coherence lengths making them unsuitable for spin logic circuits. In contrast, the interconnects in current silicon logic circuits can even run from one end of the chip to another and over many layers. This is due to the fact that an electric charge is a conserved quantity, but a spin is not, and therefore it is not easy to transfer the spin information for a long distance. Scalability is another important feature for any logic device. While a MTJ which is the building block of the spintronic memory is highly scalable even comparable to CMOS gates. The spin logic devices that have been proposed and demonstrated till now fall short on this criterion. For example, the DW-based logic devices that rely on the presence of DWs have dimensions ranging from tens to hundreds of nanometers.

The majority of works on spin logic till now have been focused on single-device demonstrations. The performance of these devices is still limited in terms of the ON/OFF ratio, speed, and scalability in their present form. For example, the ON/OFF ratio of a thin-film-transistor panel is more than 100, which is regarded as a poor performance CMOS device. On the other hand, one of the best spin filters, an MgO barrier layer which separates the two magnetic elements a high-energy barrier between them. Ideally, it is desired to cross this energy barrier with a minimum input energy. At the same time, the energy barrier should not be too small so as to allow undesired magnetic switching due to the thermal energy from the surrounding. The MRAM research aims to develop device solutions that bring the balance between the conflicting requirements of a low switching energy and high thermal stability.

The first generation of MRAM also known as toggle MRAM used magnetic fields generated by the current in metal lines as shown in Fig. 6(a) to switch the MTJ. This writing method is both high-energy-consuming and non-scalable. The second-generation MRAM which is based on STT (STT-MRAM) [49] operates on the principle of the transfer of angular momentum from a spin-polarized electron to the atoms of the magnetic bit [5], [49], [50]. In an STT-MRAM illustrated in Fig. 6(b), the spin polarized current is generated by passing a charge current through a fixed magnetic layer. While offering tremendous advantage over the toggle MRAM, the STT-MRAM still requires a large write current and has a potential endurance issue due to the breakdown of the MgO barrier layer which separates the two magnetic elements (reference and free layer) of the MTJ. In 2010, Miron et al. [51] demonstrated that a spin current generated by passing charge currents through a heavy metal (HM) layer is capable of manipulating the magnetization of an adjacent magnet. Their work formed the basis of the spin–orbit torque MRAM (SOT-MRAM) [51]–[54]. For STT operation, a nanopillar-type MTJ is required to observe the current-induced switching effect, which is very challenging in a typical academic institute; however, SOT devices even with the width of micro-size can still demonstrate the current-induced effect due to a very thin-film thickness involved in lateral current injection. This relaxed device patterning requirement attracted various academic institutes to SOT research. However, the device size of the three-terminal SOT is larger than that of the two-terminal STT, but is still half size of the modern static random access memory.

### III. Spin Devices for Memories

The existing computing memory hierarchy has tremendous performance gaps in terms of the speed and density/cost which leaves abundant scopes for improvements. For example, the write speed of the cache, main, and eFLASH memory is around 5 ns, 30 ns, and 0.1 ms, respectively [44], [45]. The emerging memory technologies which have an intermediate speed between the cache and the main memory or that between the main memory and eFLASH are promising for bringing performance improvement in future computing systems. In addition, future applications like Internet of Things (IoT) demand for fast computing at the edge in an energy-efficient manner. Spintronic in the form of MRAM offers one such potential memory solution due to its non-volatility and high speed of operation [12], [13], [46].

The basic unit of an MRAM [47] is an MTJ [48] which stores digital information in the form of two bistable magnetization states of a thin magnetic layer. These magnetization states can be read-out using the resistance value of the MTJ. The writing of the MTJ involves switching the magnetization from one stable state to another by crossing a high-energy barrier between them. Ideally, it is desired to cross this energy barrier with a minimum input energy. At the same time, the energy barrier should not be too small so as to allow undesired magnetic switching due to the thermal energy from the surrounding. The MRAM research aims to develop device solutions that bring the balance between the conflicting requirements of a low switching energy and high thermal stability.

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(SRAM). The SOT device also has an advantage over the STT ones in terms of its speed. The incubation time in STT due to parallel alignments of the incoming spin and the magnetization of the free layer is absent in the perpendicular SOT devices. The SOT geometry offers another advantage; the spin currents in SOT devices can be very large, as the electron interacts with the FM many times taking advantage of lateral scattering in the SOT device. In fact, Yoda et al. [55] reported that the switching efficiency of SOT is 3–4 times higher than that of STT using an in-plane MTJ device. In the remaining part of this section, we will discuss about the major developments in SOT-MRAM devices. At first, we begin by giving a brief introduction on SOTs.

An SOT device heterostructure typically consists of an SOT source adjacent to a magnetic layer which is the data storage unit [56], [57] [see Fig. 6(c)]. The SOT source is a material with large SOC, for example, HMs such as Pt [56], [58]–[60], Ta [60]–[63], and W [64], [65]. The magnetic layer is typically a metallic FM such as NiFe and CoFeB. When a current is passed through the HM, spins accumulate at the interface of the HM and FM. The accumulated spins diffuse into the FM during which they transfer their angular momentum to the magnetic atoms. The overall result of this process is the manipulation of the FM magnetization and its eventual switching. The SOT research has been mostly focused on the understanding and exploiting the rich SOT physics to develop energy-efficient SOT heterostructures.

The spin accumulation and the subsequent spin current that are generated on passing a charge current through an SOT device are generally due to two physical mechanisms. The first mechanism is the SHE [66]–[72]. The SHE governs charge to spin conversion in a material with large SOC. Due to the SHE, the charge currents carrying electrons with opposite spins are separated into two opposite directions resulting in a spin current ($J_S$). The direction of $J_S$ is orthogonal to both the charge current ($J_C$) direction and the spin polarization ($\sigma$) direction as illustrated in Fig. 7(a). Although predicted long back in 1971 [72], the SHE was not observed until 2004 [73] when it was measured using magneto-optical Kerr microscopy.

It should be noted that the spin accumulation due to the SHE is a result of the charge currents flowing though the bulk of the HM. The spin separation in the SHE arises either from the band structure of the SOC source (intrinsic SHE) [71] or the asymmetric spin-dependent scattering of the electron with the impurities in the SOC source (extrinsic SHE) [66], [69]. The charge-to-spin conversion efficiency therefore depends on both the intrinsic and extrinsic factors, and it dictates the amount of spin current generated from a given charge current. The charge-to-spin conversion efficiency is called the effective spin Hall angle ($\theta_{SH}$). It should, however, be noted that in many of the reports $\theta_{SH}$ is a combined representation of the spin conversion factor from the SHE and other bulk spin current sources. Finally, an SOC source which exhibits the SHE also reciprocally converts a spin current to charge current through a process known as the ISHE [74], [75].

The second process of the spin-to-charge conversion is through the interfacial Rashba–Edelstein effect also referred to as the Rashba effect [16], [51], [60], [76], [77]. In a heterostructure with broken inversion symmetry, an electric field exists at the interface of two different layers. For example, in an SOT device an electric field ($E$) exists at the interface of the HM and FM. When an electron flows through this interface, the electron experiences an effective magnetic field in a direction given by $E \times p$, where $p$ is the electron’s momentum [see Fig. 7(b)]. Under the effect of this relativistic magnetic field, the electrons at the interface are polarized in...
Fig. 8. Current-induced spin accumulation visualized using helicity-dependent photoconductance (HDP) map for (a) Bi$_2$Se$_3$ and (b) Pt. Figures adapted from [85]. Note that there is out-of-plane spin accumulation on the top surface in Bi$_2$Se$_3$ due to hexagonal warping, which changes the sign with the current direction ($I$).

While most of the experimental works on evaluation of the SHE, Rashba effect, and SOTs involve their indirect measurements using an adjacent magnet, the first observation of SHE was a direct imaging in semiconductors GaAs and InGaAs using magneto-optical Kerr microscopy [73]. A similar examination of spin accumulation in metallic HM systems with Kerr microscopy has yielded controversial results. With some groups claiming to have observed the Kerr rotation in the presence of accumulated spins [80], [81], others suggest the SHE signal to be too weak to result in any Kerr rotation for these systems [82], [83]. It was suggested that the observed signal probably arises from the change in reflectivity of the metal due to heating. With the debate still open on the validity of MOKE to visualize the SHE in metals, an alternate method of photoconductance has been used recently to visualize the current-induced spin accumulation [84], [85]. In a photoconductance measurement, a circularly polarized laser is shone on the channel which results in a voltage difference across it. When a current is also passed through the channel, it was observed that the generated voltage has the helicity dependence due to magnetic circular dichroism. Fig. 8 shows the spatially resolved photovoltage map for Bi$_2$Se$_3$ [topological insulator (TI)] and Pt. The helicity-dependent photovoltage polarity is reversed on changing the current direction in the channel. This observation is in line with the reversal of the spin polarization direction due to the change in the electron’s momentum.

We will discuss the recent advances in the development of SOT devices. Sections III-A–III-D have been divided in terms of the approaches used for these developments.

### A. Novel SOC Source Materials

The most straightforward approach to developing devices with a high SOT efficiency is by replacing the underlying SOT/SOC source. Conventional SOT devices incorporate an HM layer as the source of SOTs. Typically, HMs such as Pt, Ta, W, and Hf are used in these devices which have $\theta_{SH}$ in the range of 0.05–0.5 [56], [61], [64], [86], [87] which makes these materials very efficient in the charge-to-spin conversion and subsequent magnetization switching. Alloys involving two different HMs [88], [89] (e.g., AuPt) and HM with a low SOC material like Cu have also been shown to exhibit a large value of $\theta_{SH}$ [90]–[96]. However, there has recently been an interest in exotic and novel materials such as TIs [97]–[106] and Weyl semimetal [107]–[120] due to their large charge-to-spin conversion efficiency.

TIs are materials with an insulating bulk and conducting surfaces (topological surface states, TSS) [121], [122]. Interestingly, the TSS exhibit spin-momentum locking in which the spin polarization direction of an electron on the TSS is fixed with respect to its momentum. This results in spin accumulation at TSS similar to the SHE and the Rashba effect observed in HMs. In spintronics, TI research has been pursued both for their interesting physics and practical applications in SOTs. In 2014, it was shown that current-induced spins
in TIs (Bi$_{0.5}$Sb$_{0.5}$)$_2$Te$_3$ can switch a magnetic element [100]. However, this experiment was performed at 5 K and a magnetic doped TI was used as the switching element instead of a metallic FM. The first room temperature magnetization switching using TI was performed on a ferrimagnet (FIM) [see Fig. 9(a)] [106] and on a metallic FM [103]. On the latter, the switching was observed using MOKE microscopy, and a TI thickness dependence study was also performed. The SOT efficiency in TI ($\theta$$_{\text{TSS}}$) as a function of its thickness. Figure adapted from [103]. (c) Out-of-plane spin canting angle as a function of the angle between the current and $\Gamma K$ axis of the TI. Figure adapted from [123].

Another exotic material system for SOT research is the Weyl semimetals [124]. They have been predicted to have large spin splitting, that is, Edelstein effect due to their non-trivial band structure [114]. Current Weyl semimetal SOT researches are largely focused on WTe$_2$. The crystal structure of a Weyl semimetal, WTe$_2$, has only one mirror plane and does not contain a twofold rotational invariance [see Fig. 10(a)]. Therefore, the current-induced spin accumulation response in WTe$_2$ is anisotropic. In fact, when the current is passed through a low-symmetry axis ($a$-axis), a sizable out-of-plane spin accumulation is detected [117], [118]. This behavior was evident from the angle-dependent second-harmonic measurement, which lacks symmetry [see Fig. 10(b)] [116]. This unique property of WTe$_2$ makes it ideal for use in SOT devices with perpendicular magnetic anisotropy (PMA), while a few other field-free SOT switching schemes were proposed [125]–[129]. Current-induced magnetization switching using WTe$_2$ has been recently demonstrated, as shown in Fig. 10(c) and (d), and an in-plane $\theta_{\text{TH}}$, which increases up to a maximum value of 0.8 with increasing the WTe$_2$ thickness, has been reported [118]. Interestingly, the required power to switch the magnetization was 19 times smaller in WTe$_2$/Py than that of Bi$_2$Se$_3$/Py and 350 times smaller than that of Pt/Py due to a high efficiency and low resistivity of WTe$_2$. Furthermore, a threefold reduction in the switching current is demonstrated using dumbbell-shaped magnetic elements in MoTe$_2$/Py heterostructures [130].

Transition metal dichalcogenides (TMDs), such as MoS$_2$ and WSe$_2$, have been also shown to have a moderate charge-to-spin conversion efficiency [131], [132]. The TMDs have also been predicted to induce a large current-driven spin polarization in a graphene layer placed on them [133]. Based on this prediction, an enhanced and tunable spin-to-charge conversion efficiency was demonstrated in a graphene layer placed in the proximity of WS$_2$ [134]. The 2-DEGs at the interface of LaAlO$_3$ and SrTiO$_3$ also support a giant charge-induced spin accumulation [135]–[139]. While the above-mentioned exotic materials have been promising in terms of their charge-to-spin conversion properties, the biggest hindrance toward their practical applications is the difficulty in their fabrication for a large and uniform area as well as their large resistivity leading to a current shunting issue. Single-crystal TIs, semimetals, and other layered materials in a majority of reports discussed above have been either exfoliated or fabricated using sophisticated molecular beam epitaxy (MBE). Only very recently sputter-deposited TIs have been shown to produce large SOTs capable of switching an adjacent magnet [105], [140]. While sputter-deposited exotic materials are expected to be more technologically relevant, it is still not clear whether topological features are present and what the role is in the structure with small crystalline clusters and non-stoichiometric inhomogeneous composition. Future research efforts should focus on the fabrication of these novel materials in a fast, efficient, and reliable way.
B. Engineering the Magnetic Layer

While the SOTs nominally arise from the SOC source such as HMs, the magnetic layer can also serve as a secondary source and modulator of the SOTs. Among the different types of magnetic materials, FMs which have positive exchange interaction between the individual atoms or layers have been widely explored for SOTs. However, there are also another class of magnetic materials such as antiferromagnets (AFMs) and FIMs. These materials typically consist of two different atomic sub-lattices that prefer to align their spins opposite to each other due to the negative exchange interaction between the two sub-lattices. While AFMs have net zero magnetization due to equal and opposite magnetization of the constituent sub-lattices [141], [142], FIMs have non-zero magnetization due to unequal magnetization of the constituent elements. The major advantage of AFMs and FIMs over FMs is their robustness against external magnetic fields. This makes them thermally very stable resulting in a longer retention time compared with FMs. The thermal stability in particular is a very important factor for scaling down the spintronics devices in the nanometer regime.

In 2016, it was first shown by passing a current through an AFM with locally broken inversion symmetry such as CuMnAs [143]; the antiferromagnetic domains can be switched [144]. The switching mechanism in CuMnAs is illustrated in Fig. 11(a). The current-induced local magnetic field is generated around individual Mn atoms due to the inverse spin galvanic effect [145], [146] which requires broken inversion symmetry in the given system. While the CuMnAs crystal as a whole has inversion symmetry, the local environment of two sub-lattices formed around Mn atoms has broken the inversion symmetry. This results in staggered magnetic field of...
Institute of Physics. (b) Measured transverse device resistances as current is applied. Reproduced from [221], with the permission of American

CuMnAs. Staggered magnetic field exists for the two Mn sub-lattices when a current pulses.

Fig. 11(b) shows the varying AMR signal on application of was detected using anisotropic magnetoresistance (AMR).

Néel vector as a whole. The switching of the Néel vector

opposite polarity around these atoms as shown in Fig. 11(a).

The staggered magnetic field results in switching of the AFM Néel vector as a whole. The switching of the Néel vector was detected using anisotropic magnetoresistance (AMR). Fig. 11(b) shows the varying AMR signal on application of current pulses.

Later, AFM switching was also demonstrated in Mn$_2$Au [147], [148]. Since a single current pulse moves the AFM domain only very slightly, multilevel memory cells were demonstrated with CuMnAs [149]. The ultrafast dynamic of AFMs allows their switching with picosecond current pulses [150]. The AFM domains have been imaged using X-ray magnetic linear dichroism-photoemission electron microscopy (XMLD-PEEM) as shown in Fig. 12(a)–(c) [151]. Chen et al. [152] have recently shown that the magnetic anisotropy of the Néel vector in Mn$_2$Au deposited on a ferroelectric substrate, lead magnesium niobate/lead titanate (PMN-PT), can be switched between two orthogonal directions. This results in a ratchet-like switching behavior [see Fig. 12(d)]. Apart from inducing switching, it has been also proposed that the staggered relativistic SOT fields can result in a very high DW velocity in these AFMs [153]. Other than AFMs with broken inversion symmetry, there have also been demonstration of Néel vector switching in insulating AFMs such as NiO [154]–[156]. In these works, the SOTs are generated from an adjacent HM instead from the AFMs themselves.

While the AFMs present an exciting and stable system for spintronic applications, the detection of their magnetization state remains challenging. Since the AFMs are read electrically using a small value of AMR rather than TMR, they are incompatible with an MTJ which is the standard readout device in the MRAM industry. For example, a TMR value of 150%–200% is required for a readout speed of 5–20 ns. In addition, a recent work by Chiang et al. [157] suggests that the AMR measurements in AFMs are complicated by the normal Seebeck effect and resistive switching. On the other hand, synthetic antiferromagnets (SAF) and FIMs offer a viable alternative to both the AFMs and FMs. Not only are they unperturbed against the external magnetic field similar to the AFMs but also their magnetization can be detected easily by anomalous Hall resistance ($R_{AHE}$) and TMR similar to the FMs.

Synthetic antiferromagnetism arises from the interlayer Ruderman–Kittel–Kasuya–Yosida (RKKY) coupling between two ferromagnetic layers separated by a spacer such as Ru [158]–[162]. Compared with AFMs such as CuMnAs, SAF are easier to fabricate and do not require special crystalline substrate. Fig. 13(a) shows a measurement of a very large DW velocity (750 m s$^{-1}$) obtained in an SAF formed by the Co/Ni/Co multilayers through a Ru spacer [163]. The negative exchange coupling results in this high domain velocity which increases with the amount of compensation [see Fig. 13(b)] between the two coupled layers. It was also found that the SOT switching efficiency in a completely compensated SAF made with the Co/Pd FM layers was significantly higher compared with the FMs [164]. Recently, it was shown that the SOT for the AFM coupling case is $\sim$15 times larger than without the AFM coupling in a Pt/Co/Ir-based SAF system [165]. This report suggests that the interface-induced phenomena apart from the negative exchange torque [163], [166] are possibly responsible for such a large SOT efficiency in the SAF.

The relatively weak exchange coupling in the SAFs leaves space for the exploitation of the FIMs. Rare-earth transition-metal (RE-TM) FIMs [167], [168] have been the material of choice in magneto-optical disks previously and FIM SOT devices recently. The magnetization in these RE-TM FIMs can be tuned by varying the relative composition of the RE and TE components or by adjusting the ambient temperature. The tunable characteristic of RE-TM FIMs provides a fertile ground for studying SOT in both the AFM and FM regimes. In CoGd-, CoTb-, and GdFeCo-based FIMs, it has been shown that the SOT efficiency or the SOT effective fields increase near the compensation point, that is, when the magnetization of the FIM is minimum [166], [169]–[174]. However, the amplification of SOT near compensation cannot be fully explained by the reduced magnetization. It has been proposed that apart from the reduction of the magnetization near compensation, the drastic amplification of SOTs in compensated FIMs has been attributed to the enhanced negative exchange torque [164]–[166]. The high efficiency of SOTs in the RE-TM FIMs and the fact that these materials derive perpendicular anisotropy from the bulk help in developing devices with a thick and thermally stable magnetic layer. Roschewsky et al. [174] have shown current-induced magnetization switching.
of 30 nm thick GdFeCo layer which has a thermal stability of \( \sim 100 \, k_B T \), where \( k_B \) is the Boltzmann’s constant and \( T \) is the temperature.

The faster intrinsic dynamics due to the negative exchange coupling also results in ultrafast switching in the FIMs. Fig. 13(c) shows the comparison of the switching energy and switching duration of the FIMs with the FMs [175] from which it can be seen that the FIMs are around 1–2 orders of magnitude better than FMs on both parameters. The ultrafast dynamics in FIMs [176], [177] also leads to a very high current-induced DW velocity up to 5.7 km/s [175] when compared with the FMs or even the SAFs [see Fig. 13(d)] [178], [179]. The high DW velocity finds applications in DW motion-based magnetic devices. It has also been reported that the FIMs and AFMs support longer spin coherence lengths [180], [181]. Fig. 14(a) illustrates the alternating spin alignment in an FIM that assists spin information transfer over a longer distance. Due to opposite exchange fields in alternating sublattices, spin dephasing is partially compensated. The SOTs therefore act over a larger thickness in the FIMs. Fig. 14(b) shows the bulk-like SOT [180] in the FIMs when compared with their limited penetration (< 1.2 nm) in the FMs [182], [183]. A disadvantage of RE-TM FIM is that the RE element is prone to oxidation. In the MRAM fabrication steps in which the die is exposed to different temperatures and chemicals, preventing oxidation of FIMs can be challenging. The temperature sensitivity of the magnetization of FIM and related properties should be considered while designing memories based on them. For example, the temperature sensitivity of FIM could be a critical issue involving varying temperature environment such as automotive applications. Considering that FIM has been successfully commercialized for magneto-optical disks, the above oxidation and temperature issues could also be addressed in magnetic memory applications.

While in this section we have mainly discussed the research works concerning the antiferromagnetically coupled materials, there are analogous efforts to exploit other interesting magnetic systems such as multilayers [184], [185] and magnetic insulators [186], [187]. Apart from a faster speed and lower power consumption, the integration of new magnetic systems in the MTJ-based MRAM architecture is a criterion that is important to meet for real applications.

### C. Engineering the SOT Heterostructure Stack

The simples SOT device consists of an SOC source neighboring a magnet. In this section, we will discuss about the alternative SOT heterostructures that enable an enhanced efficiency. In 2014, Woo et al. [188] demonstrated that by sandwiching the FM between SOC sources with opposite \( \theta_{SH} \), the overall SOT effective fields in the device can be enhanced. In their work, a thin Co layer was inserted between Pt and Ta which are the materials with opposite \( \theta_{SH} \). The maximum effective \( \theta_{SH} \) of the device was found to be around 0.35 for a Ta and Pt thickness of 4 and 3 nm, respectively. This value is larger than the individual \( \theta_{SH} \) of either Pt or Ta. Later in a detailed report, Yu et al. [189] compared the effective field among different material combinations (e.g., Pt, Cu, MgO, Ir, Ta, W, and Hf) with Pt as shown in Fig. 15(a). It was found that a combination of Pt and W results in the largest effective \( \theta_{SH} \) of 0.45. Additionally, it was suggested that the thicknesses...
Fig. 13. (a) DW velocity as a function of injected current for CoNiCo-based SAF stacks with different compensations. (b) Magnetic characterization of the SAF stack. The green curve is for a spacer (Ru) thickness that results in ferromagnetic coupling (SF—synthetic FM). Red, violet, and blue data points are for SAF with varying degrees of compensation achieved by changing the thickness of the top layer in the SAF. Reprinted figure with permission from [163], copyright 2015. (c) Comparison of the switching energy and time between SOT devices based on FIMs (CoGd) and FMs. Please note that the references cited in this figure are the ones listed in the original article. Figure adapted from [175]. (d) Current-induced DW velocity in a CoGd-based SOT device as a function of temperature. Reprinted figure with permission from [178], copyright 2018.

of the two HM layers are critical for obtaining the largest SOT efficiency, as it dictates the current shunting in the individual layer. It has also been shown that a bilayer of two HMs (Pt and Ta) can be used to continuously tune both the magnitude and direction of SOTs [190].

The interface between the HM and FM is critical in determining the magnitude of SOTs in a given device. The quality of this interface decides the amount of spin memory loss and spin transparency, and hence the magnitude of spin current experienced by the FM [191]–[193]. Due to the above reasons, the experimentally obtained SOT strengths (e.g., $\theta_{2\text{SH}}$) are the effective values including various bulk and interface effects. It was shown that by dusting a thin layer (~0.5 nm) of Hf at the Pt–CoFeB interface, the spin–torque efficiency could be enhanced up to 0.12, which is nearly double compared with the Pt/Py system [194]. An accompanied reduction of the magnetic damping, $\alpha = 0.012$, was also reported because of spin pumping suppression. The above approach was used to achieve a low switching current density of $5.4 \times 10^6$ A/cm² in an in-plane MTJ which had Hf dusting on both interfaces of the free layer [195]. An interfacial Ti layer (~1 nm) between Pt and CoFeB also helps in reducing the switching current density three times [196]. Recently, it has been suggested that a lower value of interfacial SOC at the HM–FM interface results in a lower attenuation of the spin currents by decreasing the spin memory loss [197].

Capping the HM/FM stack with the Ru layer has been shown to result in an enhanced value of SOTs [183]. This enhancement is attributed to the spin current absorption in the Ru layer as illustrated in the schematic of Fig. 15(b). The SOT effective field increases by a factor of 3 for a Ru thickness of 0.6 nm when compared with a Pt/Co/Ni/Co device without any Ru layer on top. In another variation of the SOT devices, it has been demonstrated that an in-plane magnetized FM layer [see Fig. 15(c)] can perform charge-to-spin conversion similar to an HM [198]–[200]. The resulting spin current in this heterostructure is capable of switching a perpendicular CoFeB layer without any assist in-plane magnetic field [see Fig. 15(d)] due to a slight out-of-plane alignment of the generated spins. However, in this heterostructure the
in-plane magnet should be immune against the external magnetic field. Therefore, an in-plane magnet with a high coercivity is required. Moreover, repeated switching events can perturb the magnetization direction of the in-plane magnet, and thus affecting the long-term stability of the memory device. Inadvertent switching of the in-plane magnet can result in opposite sense of switching loop and can lead to unreliable memory operations. We would like to bring to the reader’s attention that apart from the aforementioned works on engineering SOT heterostructures, there is a dedicated research effort on engineering SOT heterostructure for field-free SOT switching of the perpendicular magnetization, which is of significant importance for applications, the details of which can be found in a recent review [52]. Even though many different schemes were proposed for field-free switching, there is no clear avenue which can satisfy requirements of MTJ integration and large wafer size scaling with a homogeneous device-to-device uniformity, and further research is required to address this important issue.

**D. SOT Modulation by Oxygen Incorporation**

Oxygen plays an important role in determining many magnetic properties. For example, the incorporation of oxygen in metallic FMs such as Fe, Ni, and Co, induces negative exchange interaction resulting in the formation of AFMs such as Fe₂O₃, NiO, and CoO. For applications in nanodevices, a strong PMA which is vital for device scalability is derived from the orbital hybridization of magnetic atoms with the oxygen at the interface [201], [202]. As a result, the PMA has a strong correlation with the amount of oxygen at the magnetic interfaces. In fact, it was shown that by migrating the interfacial oxygen using the electric field, the PMA can be significantly altered in a non-volatile and reversibly way [203]–[205]. In the field of SOTs, it was found that the oxide capping layer plays a role in determining the magnitude of SOTs for a given device [206]. Both the field-like and damping-like torques were found to be 10 and 6 times larger, respectively, for a MgO capped Hf/CoFeB device compared with a TaOₓ capped one. The different interfacial electric field at the oxide interface and the resulting Rashba torque were attributed to this variation [86]. This suggests that not only the bottom HM–FM interface but also the top FM–capping interface should be considered to estimate the overall SOT effect in a given structure.

Incorporation of oxygen in the magnetic layer is another way of manipulating the SOTs. It was first shown when oxygen is dynamically introduced in the Co layer of a Pt/Co/GdOₓ device by the application of a gate voltage, the resultant SOT was an order of magnitude larger compared with the unmodified device [207]. While an enhancement of SOT on Co oxidation is expected due to the reduced Co magnetization, the observed amplification of SOT in this work was found to be disproportionately larger compared with the amount of reduction in the magnetization. This hints toward a role of oxygen in modifying the interfacial SOTs. A similar enhancement of SOTs was also reported on an HfOₓ capped device in which the gate voltage was applied using ionic liquid [208]. Hasegawa et al. [209] recently showed that on introducing an oxidized Co layer at the Pt–Co interface a fourfold and tenfold enhancement of the longitudinal SOT effective field (Hₓ) and transverse SOT effective field (Hᵧ), respectively, was achieved.

Apart from modulating the magnitude of SOTs, an oxidized Co or CoFeB layer on a thin Pt layer results in a reversal of the overall spin accumulation direction or the effective $\theta_{SH}$ polarity [210], [211]. It was shown by Qiu et al. [210] that in a series of Pt/CoFeB/MgO/SiO₂ devices with varying the SiO₂ capping thickness, devices with thin SiO₂ capping (<1.5 nm) have opposite SOT effective fields compared with the ones with thicker SiO₂ capping. Interestingly, the SiO₂ thickness of 1.5 nm corresponds to the native oxide thickness of SiO₂ when it is exposed to air. This opposite direction of SOT fields resulted in an opposite current-induced switching polarity as measured by the anomalous Hall resistance ($R_H$) in Fig. 16(a). It was found that the thickness of the SiO₂ capping determined the amount of oxygen in the magnetic layer, and hence the polarity of SOTs. Recently, it was shown that this SOT polarity control can be achieved dynamically and reversibly in a single Pt/Co/GdOₓ device using electric-field-assisted oxygen migration [211] as illustrated in Fig. 16(b), in which GdOₓ works as an oxygen reservoir sending and receiving oxygen ions depending on a negative and positive top gate bias voltage, respectively. The SOT polarity reversal has been attributed to competition between the bulk SHE and interfacial Rashba effect. An oxidized Pt–Co or CoFeB interface has a larger Rashba torque with an opposite polarity compared with a spin Hall torque, and therefore the device
has a negative SOT polarity. The critical level of oxidation of the Co layer is found to be $\sim 30\%–40\%$ to observe a SOT sign change; however, over-oxidation ($>50\%$) can cause an irreversible formation of CoO, which cannot be reduced back to Co by applying a gate bias. In addition, the oxygen at the interface was fine-tuned with the electric field to program the SOT device with a range of effective spin Hall angle as shown in Fig. 16(c). Such a sign change behavior with oxygen cannot be understood by the spin Hall physics. A recent work revealed that the experimentally reported oxygen-induced sign reversal of the SOT in Pt/Co bilayers is due to the significant reduction of the majority spin orbital moment accumulation on the interfacial HM atoms [212]. One of the drawbacks of oxygen migration-based spintronic devices is their slow speed of modulation. Unlike electrons, the oxygen ions migrate relatively slowly requiring between few milliseconds and tens of seconds to change the state of the given device. The optimization of the gate oxide thickness and material is essential to improve the performance of these devices. For example, recently yttria-stablized zirconia was used as a gate oxide to achieve anisotropy modulation in milliseconds, which is 100 times faster than any of the previously demonstrated magneto-ionic devices [213]. Due to a slow speed, these devices are not suitable for near-core memories, but can be exploited for flash replacement and field-programmable gate array (FPGA). In addition to the slow speed, the constant flux of oxygen ions inside these devices may result in a breakdown of the oxide or even the magnet after many cycles of operation. Since the process of oxygen migration is stochastic, there is cycle-to-cycle variability in the device operation. All the above concerns of oxygen migration based on spin devices need to be addressed before their practical applications, which share similar fundamental challenges with resistive random access memory (RRAM) due to the ionic migration nature.

The oxidation of the SOC source or the HM has been used in a few works to modulate the SOTs. A large $\theta_{\text{SH}}$ of $\sim -0.5$ was reported when 12% of oxygen was incorporated in tungsten [214]. $\theta_{\text{SH}}$ remains relatively insensitive with increasing the oxygen content [Fig. 17(a)] even though the material properties of W change with oxidation. The giant $\theta_{\text{SH}}$ was attributed to $\beta$-phase stabilization of W and an increase in the interfacial SOTs. However, the high resistivity of W which further increases with oxygen incorporation will result in large power consumption when these devices are used in memories. Recently, it was reported that an oxidized Pt, which is an insulator, shows $\theta_{\text{SH}}$ comparable to that of normal Pt, even capable of inducing efficient magnetization switching [215], [216]. While W and Pt are HMs with large SOC, a similar enhancement of SOTs on both surface and bulk oxidation of Cu was observed in a series of studies [217], [218]. Fig. 17(b) shows the spin torque ferromagnetic resonance (ST-FMR) measurement results for different degrees of Cu surface oxidation. A NiFe/Cu sample with a naturally oxidized Cu surface was found to have a larger spin–torque efficiency as evident from the symmetric ST-FMR component when compared with the SiO$_2$ capped un-oxidized Cu sample [217]. The SOTs in oxidized Cu were attributed to intrinsic Berry curvature and modification of orbital hybridization [218]. Overall, we see that oxygen in different layers and interfaces of an SOT device plays a vital role in enhancing and manipulating SOTs. Future research efforts should aim toward a more dynamic modulation of this oxygen content in a single device using gate biasing for applications.

Apart from the spin memory devices discussed in this section which are mainly based on switching of a magnetic element, there have been parallel efforts to enable magnetic memories using alternate schemes. One such methodology involves skyrmions on race tracks [219]. A race track is a
magnetic channel that can be used to store memory bits in the form of magnetic domains [220]. These bits or magnetic domains can be moved with the help of spin currents. In the skyrmion race track memory, these magnetic domains are replaced by skyrmions which have greater topological protection. In addition, the small size of skyrmion and the ease with which can be moved with a current holds promise toward developing a denser and low-energy storage. The spin current to move the skyrmions can be applied either using STT or SOT. However, there are many challenges that are currently being addressed in the field of skyrmion devices before a reliable memory can be realized. The corresponding research work primarily focuses on stabilization of skyrmion, their energy-efficient and linear movement on a magnetic track, and performing low-noise reading. More details of these works can be found in focused reviews [38], [39].

Spin devices are one of the most promising non-volatile memory candidates. Spintronics memories have evolved from a field-switching toggle MRAM to current-switching STT-MRAM and then recent active research topic of SOT-MRAM. There are still a few major challenges that need to be addressed before the practical implementation of SOT-MRAMs. First, the proposed material system and device structure should be compatible with the MTJ read-out scheme for fast read operations and a large size wafer scaling with a good uniformity should be guaranteed. External magnetic field-free switching of SOT devices without involving a complicated structure is another requirement for the adoption of SOT-MRAMs. Other challenges include a further reduction in the writing power and the switching time for SRAM replacement. Among the SOC candidates, it is desirable to have a good balance between the spin Hall efficiency and charge conductivity. While the
TI such as Bi$_2$Se$_3$ and HM such as W offer a large spin Hall angle, their large resistivity values will lead to large power consumption when used in memories. The switching endurance and read/write error rate evaluation also need to be carried out to meet the application requirements.

Among the explored physical mechanisms for non-volatile memory applications, spin memories hold competitive advantages in most of the performance parameters. The area of spintronic RAM is around 10–30 $F^2$ which is $\sim$5–10 times smaller than semiconductor SRAM and is comparable to other non-volatile candidates such as the RRAM, phase change memories (PCRAM), and ferroelectric RAM (FeRAM) [44]. The area per cell of RRAM can, however, be reduced by the 3-D architecture. The write voltage of STT-RAM of $\sim$1–1.5 V is the lowest among all the memories and is comparable to the SRAMs and DRAMs. For example, the write voltage for RRAM and PCRAM is greater than 3 V, while that of the FLASH memory is easily greater than 10 V. In terms of the write energy, all the non-volatile memories are more power-consuming (0.1–100 pJ) compared with the SRAM and DRAMs (1–10 fJ). However, STT-RAM falls at the lower end of this spectrum, consuming only 1 pJ during the write operation. In comparison, the eFLASH easily consumes around 100 pJ during writing. The lowest power of $\sim$0.1 pJ is consumed by FeRAM. With adoption of SOTs in the MRAM, the writing power can be even reduced further. The reading and writing speed of MRAM is also relatively high ($\sim$ a few to tens of ns). The writing time is in fact 5–6 order lower than the eFLASH. The endurance of STT-MRAM is predicted to be around $10^{15}$ cycles. RRAM which is based on the movement of ions and PCRAM which involves thermal treatment in every write cycle suffers from a relatively low endurance of $10^7$–$10^{12}$ cycles due to the nature of their operations. The endurance of MRAMs can be further improved by the SOT architecture which separates the read and write path.

IV. Spin Devices and Non-Von Neumann Computing

The present-day computing systems are based on the Von Neumann architecture in which the memory and processing units are separated and information processing is carried out serially. This architecture and computing methodology have fueled the information technology revolution for the past few decades. However, the massive increase in the amount of data with the recent rise of interconnected devices necessitates a new type of computing scheme that can efficiently interpret the data similar to a human brain. To this end, neuromorphic or brain-inspired computing aims at developing devices and circuits that can perform tasks involving learning, training, recognition, and cognitive ability. In addition, there is devoted research on alternate computing systems such as Ising machine and quantum computing, which can perform certain optimization tasks at a much faster speed compared with modern computers. In this section, we will discuss the recent progress in the spintronic devices and systems that have applications in the above-mentioned non-Von Neumann computing methodologies.

In the area of spin-based neuromorphic computing hardware, a variety of synapse and neuron models have been proposed based on a combination of magnetic DWs, MTJs, and SOTs [222]. The earliest proposal for spintronic synapse shown in Fig. 18(a) has a magnet with a DW acting as a synapse which is connected via an NM channel to the magnetic neuron [223]. The position of the DW in the synaptic-magnet determines the spin polarization of the current when a voltage is applied on this magnet. The spin polarization is therefore an analog function of the DW position, and thereby represents the synaptic weight. During the write operation, a current passed vertically through the synaptic-magnet will carry the weighted information in the form of degree of spin polarization. This spin-polarized current which represents a potential stimulus at the input of neuron can be used to switch an adjacent magnet that acts as a neuron. Many of these synaptic-magnets can be connected as fan-in to a single neuron which will receive weighted sum of spin currents from these inputs as shown in Fig. 18(b).

In a later proposal, Sengupta et al. [224] proposed a synaptic design which has a DW integrated with an MTJ as shown in Fig. 18(c). In this structure, the weight is written by SOT-induced DW motion. The DW moves transverse to the channel length when a current is passed from terminal C to D as illustrated in Fig. 18(c). The position of DW in the free layer of the MTJ determines its conductance which can be inferred as the synaptic weight. The parallel alignment of the free layer with respect to the reference layer results in a high conductance or maximum weight. On the other hand, an antiparallel alignment between two layers is a state of minimum weight due to a low conductance of the MTJ. The rest of the conductance states that lie in between these two states are determined by the DW position in the free layer. A similar device structure but without the extended free layer and HM channel [see Fig. 18(d)] was also proposed to perform identical synaptic functions [225]. In this design, the current is applied along the length of the MTJ and the DW moves along the current direction. The proposed device can emulate a neural transfer function as well when connected with a reference MTJ and a transistor as shown in Fig. 18(e). The reference MTJ in series with the synaptic or DW MTJ acts as a voltage divider between the supplied voltage and the ground. The position of DW in the synaptic MTJ determines the divided voltage at the input terminal of the transistor. The resulting transfer function of the complete device is in form of a sigmoid as shown in the inset of Fig. 18(e). It should be noted that a sigmoidal transfer function forms a building block of artificial neural network (ANN). Similar to the proposals of spin logic in Fig. 3(a), the above proposals are also based on ideal behaviors of the DW, the magnet, and the spin interconnects. The superposition of spin currents from different fan-ins as shown in Fig. 18(b) has not been demonstrated yet. Moreover, precise optimization of interconnect lengths and materials is also required to avoid spin decay. For DW-based synapse, the nanodimension of the future devices will result in very few analog states. For further details on a potential spin-based hardware solution for neuro-computing, we refer to the reader a focused review [222].
On the experimental side of spintronic neuromorphic hardware, Lequeux et al. [226] have demonstrated a DW-based synapse which has a large number of intermediate resistance states. This spintronic synapse consists of an MTJ with a single DW in the free layer. The DW can move back and forth with the aid of STT applied using a positive and negative current pulse. The pinning of the DW results in an intermediate domain configuration, hence in-between resistance states [see Fig. 19(a)]. A problem with this device is a reliable control of the DW. The motion of DW is not predictable due to the inhomogeneity of the material and thermal effects. While a linear weight tunability is desirable for synapse in ANNs, the DW synapse has a non-linear weight programming due to the arbitrary distribution of the pinning sites. A series of MTJs with moving DW under them have been used to implement precise and linear weight generator [227]. The schematic of this device and the corresponding scanning electron microscope image are shown in Fig. 19(b). The variation in the MTJ device areas produces a non-linear activation function as shown in Fig. 19(c). Borders et al. [228] have used an AFM-FM (PtMn-[Co/Ni]) bilayer SOT device which presents analog switching states like a biological synapse [see Fig. 19(d)]. The analog switching behavior is due to pinning of domains with AFM grains. In this work, the authors have demonstrated associative memory operation using 36 of these SOT devices integrated with an FPGA.

Recently, magnetic synapse has been demonstrated with a Pt/Co/GdO\textsubscript{x} SOT device [229]. Its working principle involves electric-field-induced reversible oxidation and reduction of the Co layer, thereby modulating its magnetization. The magnetization of the Co layer represents the synaptic weight measured using the anomalous Hall resistance ($R_{\text{AHE}}$) as shown in Fig. 19(e). Synaptic functionalities like potentiation, depression, spin-rate, and time-dependent plasticity were demonstrated on this device. Fig. 19(e) shows the effect of different stimulating pulse frequencies on the synaptic weight. Similar to a biological synapse, frequent stimulations result in a larger change in the synaptic weight when compared with sporadic stimulations. Since the device is based on oxygen migration, the speed of the synaptic update is quite slow. The read-out of the magnetization using the anomalous Hall resistance is also non-ideal for supporting a large number of fan-outs which are present in a typical neural network. Magnetic skyrmions have also been used to mimic the potentiation and depression function of the biological synapse [230]. The number of skyrmions in the magnetic channel determines the weight of the synapse which can be measured using the anomalous Hall resistance. Creation or annihilation of a single skyrmion in a ferrimagnetic film using a current pulse results in a quantum jump of the synaptic weight similar to the potentiation or depression of the biological synapse. Since the number of skyrmions in the channel can be effectively controlled using current pulses, the corresponding weight update is approximately linear. However, the skyrmion readout signal is generally very small, which poses a challenge in the readout operation and dynamic range of these synapses.

While the synaptic functionalities using spintronic elements have been implemented by a few groups, a hardware
realization of neuron has been rather challenging and limited. Few experiments have used MTJs to demonstrate a stochastic spiking neural function. A threshold current to drive the MTJ in an unstable state that results in stochastic current spikes was used in one of the schemes [231]. In a recent experiment, VCMA was used to enable a stochastic switching behavior of the free layer of the MTJ as shown in Fig. 20(a) [232]. In this work, the perpendicular anisotropy of the free layer was modified by an applied bias voltage to the MTJ. The bias voltage results in lowering the energy barrier leading to a stochastic switching of the free layer. The switching probability has therefore a sigmoidal relation with the applied bias field.

While a stochastic device with sigmoidal transfer function is suited for ANN, the leaky integrate-and-fire neuron is necessary to implement a spiking neural network. Thermally assisted current-induced SOT switching was exploited to enable this integrate and fire function [233]. Current pulses arriving at a high frequency integrate the temperature–current budget above the switching threshold of the SOT due to minimal leakage or less heat dissipation. This results in magnetization switching or neural firing (probability of switching, \( P_{sw} = 1 \)). For current pulses arriving far apart, the heat generated by the first pulse is dissipated by the time when the second pulse arrives, and therefore, the SOT device does not switch (\( P_{sw} = 0 \)). For pulses of intermediate frequency, \( 0 < P_{sw} < 1 \). Fig. 20(b) shows the distribution of the switching probability as a function of pulse frequency for the given SOT device. This behavior is similar to a biological neuron in which the incoming potential spikes to a neuron integrate in a leaky fashion resulting in neural firing when the membrane potential exceeds a pre-determined threshold. However, it should be noted that while the above SOT neuron can integrate and fire, it does not automatically reset like a biological neuron. This functionality is yet to be achieved using a spin device.

Apart from the research on spintronics counterpart for biological synapse and neuron, there are some interesting works on system-level implementation of spin devices for recognition and optimization tasks. Torrejon et al. [234] have used a spin-torque oscillator (STO) which converts an input dc current into voltage oscillation, for spoken vowel recognition. An STO is basically an MTJ in which the magnetization oscillates in a self-sustaining fashion around the effective magnetic field when a balance is achieved between the magnetic damping and the applied current-induced torque. The oscillation of the magnetization in effect results in an oscillating TMR signal. The frequency of these oscillations is a function of the effective magnetic field experienced by the magnet and its gyromagnetic ratio. Therefore, an STO is characterized by its oscillation frequency which can be tuned by varying the external magnetic field. An STO combines the non-linearity and memory in a single device [235]. The non-linear behavior is between the applied current and the amplitude of the generated voltage, while the memory function is achieved due to the dependence of the output on the past input currents. After pre-processing, the input speech signal was applied in the form of current to the STO, while the output was recorded.
in varying voltage signals. A comparison of the recognition performance with and without an oscillator in Fig. 21 shows clearly the improved performance of the STO-based system.

In a later work, four of these oscillators were electrically coupled for a vowel recognition task [236]. The electrical coupling was achieved by physically connecting these oscillators with wires. These oscillators were synchronized with two external microwaves as shown in Fig. 22(a). Each oscillator synchronizes itself with an external microwave frequency in a different range as shown in the right panel of Fig. 22(a). The range of synchronization can be tuned by varying the applied bias current to the individual oscillator. The spoken vowels were coded as a function of two external input microwave frequencies \( f_A \) and \( f_B \). The frequency distribution map of each vowel for different speakers overlapped on the oscillator synchronization map is shown in the left panel of Fig. 22(b). The color in the synchronization map represents the oscillator or oscillators synchronized with the two microwaves as shown in the legend bar to the right of Fig. 22(b). For example, (1A) represents the first oscillator synchronized with microwave source A, and (2A, 4B) represents the second and fourth oscillators synchronized with microwave source A and B, respectively. Since the goal of this work was to recognize vowel independent of the speaker, the learning involved adjusting the bias current through the oscillators so that the points for each vowel are contained in single synchronization region. The synchronization map after different training steps is shown in the middle and right panels of Fig. 22(b). Comparing the first and last panels of Fig. 22(b), it can be seen that after sufficient training, the spoken vowels which were initially distributed in more than one region on the synchronization map eventually reside in approximately a single synchronization region. A reasonable recognition rate of 89% was achieved after around 50 training steps. The disadvantage of using oscillators for neuromorphic computing is their limited scaling potential. In addition, the frequency spectrum of spintronic oscillators is not very sharp and has a large full width at half maximum which hinders their operational reliability.
Fig. 22. (a) Experimental setup of four electrically connected and coupled spin oscillators. Two external microwaves with frequencies $f_A$ and $f_B$ are applied to the coupled system. The microwave outputs from the oscillators without and with the external microwaves are shown by light blue and dark blue graphs, respectively. Synchronization of individual oscillator with external microwave (right). (b) Color code background in the figures shows the synchronization map of the oscillator as a function of $f_A$ and $f_B$. The color coding represents the oscillator or oscillators which are synchronized (see legend). The data points are frequency-coded representation of vowels spoken by different speakers. The evolution of the synchronization map after 15 and 86 training steps is shown in the middle and right panels, respectively. Reprinted figures with permission from [236], copyright 2018.

Very recently, the stochastic behavior of a thermally unstable MTJ has been used to develop a probabilistic-bit (p-bit) for integer factorization [237]. A p-bit is an entity that fluctuates between two binary states with a probability that can be controlled by an input [238], [239]. The relation between the input $I(t)$ and the output $m(t)$ of a p-bit is given by

$$m(t) = \text{sgn} \left[ \tanh(I(t)) - \text{rand}(-1, 1) \right]$$

(1)

where $\text{rand}(-1, 1)$ is a random number uniformly distributed between $-1$ and $1$ [238]. The stochastic nature of the p-bit finds applications in probabilistic computing. The MTJ for a spintronic p-bit is designed by optimizing its volume and free layer thickness so that the energy barrier between its two bistable states is low enough to be surpassed by ambient thermal energy. This results in the MTJ switching stochastically. Initially, current-controlled MTJ p-bits have been proposed [238], [240] as shown in Fig. 23(a). These three-terminal p-bits were driven by SHE torques induced by input currents flowing in the HM below the MTJ. The output can be read by passing a small read current through the MTJ which can be fed into a buffer stage. The CMOS buffer stage helps in providing a gain and isolation at the output. For the magnitude of input current greater than the threshold value, the MTJ free layer pins in one of the stable states resulting in an output of $+1$ or $-1$. However, for values of input current in between the MTJ behaves stochastically and the instantaneous value of the output can fluctuate between $-1$ and $1$ as determined by (1).

In a voltage-controlled scheme, the stochastic MTJ is connected to an n-type transistor (NMOS) as shown in Fig. 23(b) [237]. The transistor has also a resistance $R_{\text{source}}$ at its source terminal which limits the currents through the MTJ to a value at which its switching probability is 0.5 [237]. The output of the transistor is connected to a comparator which determines the final output ($V_{\text{OUT}}$) of the p-bit. While the instantaneous $V_{\text{OUT}}$ of the p-bit will be either of the rail-to-rail values, the time-averaged output (over 700 ms and 2000 sampling points) is a sigmoidal with respect to $V_{\text{IN}}$ as shown in Fig. 23(c). For performing factorization, these p-bits are interconnected (not physically) such that the input of each p-bit is a function of the output of all the other bits. In general, the input $I_i$ for the $i$th bit is determined by

$$-\delta E(m_1, m_2, \ldots)/\delta m_i.$$ Here, $m_i$ is the output of the $i$th bit and $E(m_1, m_2, \ldots)$ is the energy cost function. The inputs are calculated analytically from the outputs and the cost function ($E$) using a microcontroller. It should be noted that depending on the optimization problem, the associated cost function will be different. The p-bits frequently end up in configurations that minimize the cost function, $E$.

Fig. 23(d) shows a factorization result of number 35 obtained using four p-bits. The two factors in the binary form are represented by $(p_1, p_2, 1)$ and $(q_1, q_2, 1)$, where $p_i$ and $q_i$ are the four p-bits. The top panel of Fig. 23(d) shows an equal distribution between different states of the p-bits when they are uncorrelated, in this case their inputs
Fig. 23. (a) Current-controlled probabilistic or p-bit. MTJ has a low thermal barrier at room temperature which allows it to randomly switch between the two stable states. The stimulus is applied using the current-induced SHE. Adapted from [238]. (b) Voltage-controlled p-bit based on a stochastic MTJ, a transistor, and a comparator. (c) Time-averaged output and input voltage of the p-bit follows a sigmoid relationship. (d) Uncorrelated and correlated states of the four p-bit system are shown in the top and bottom panels, respectively. The correlate states are used to factorize the number 35. Reprinted figure with permission from [237], copyright 2019.

function being zero. When the p-bits are connected, their probability of settling in a configuration is highest for the values representing the numbers of (5, 7) and (7, 5), that is, factors of 35, as shown in the bottom panel of Fig. 23(d). Occasionally the p-bits end up in state representing the number (5, 5), (7, 7), and so on, although with a very less probability. In this work, spin-based probabilistic computing compared with the CMOS-based alternatives was suggested to offer an energy benefit of 10 times and an area advantage of 300 times. However, whether the proposed scheme can be scaled for a real application is questionable (e.g., the most common form of 256 bit encryption corresponds to 78 digits). It should also be noted that the network weights are still implemented in a microcontroller in this work. Going forward, these should also be implemented in hardware using memristors or capacitive network.

Other application of p-bit-enabled stochastic circuits includes machine-learning-inspired applications such as Bayesian inference and accelerating learning algorithms. Quantum-inspired applications such as inverted Boolean logic (e.g., finding input to a logic gate for a given output) and optimization problem like traveling salesman problem can also be solved using a network of p-bits [241]. Current-controlled p-bit can be used to implement binary activation function in a binary neural network (BNN) in combination with memristors that implement weights [242]. A more detailed review on these applications can be found in [241].

There are many other alternative computing methodologies and application-specific hardware that can be enabled in an energy- and area-efficient way with spin devices. BNNs, which use binary values of weights and activations, achieve the same degree of accuracy compared with the normal neural
networks while being more resource-efficient in terms of storage, speed, and power. During inference, the BNNs use the XNOR operation, which can be implemented using a single SOT device. The two inputs of the write driver of an SOT cell can serve as the inputs to the XNOR gate [243]. Non-volatile memories are also used for in-memory computations, which help in saving a large amount of power and time that is spent due to the separation of memory and computing units in a von Neumann architecture. The in-memory computing capability has been proposed to implement a two-bit AND gate used for performing the bit convolutions in BNNs [243], [244]. In this scheme, the row decoder is modified to turn on two read-word lines simultaneously. The sense current of the selected SOT bits flowing through the bitline determines the values stored in them. By appropriately setting the reference voltage in the sense amplifier circuit, logic AND can be implemented. Instead of using two bits, a single STT cell-based scheme was proposed for performing in-memory computation by fabricating two MTJs on top of one other [245]. Apart from the use in BNNs, the in-memory computing architecture using spin devices can be leveraged for bioinformatics (e.g., deoxyribonucleic acid (DNA) read alignment) [246], [247] and graph processing applications [248], [249].

The results discussed in this section demonstrate the viability of spintronics hardware for non-von Neumann computing systems. At present, the ANNs are implemented mostly in normal computers. Since the weights of the network are stored in memory and computing is performed in the processor, the flow of information between these two components is a speed and power bottleneck. Hardware implementations of ANNs have involved accelerators for matrix multiplication, for example, GPUs and in few cases using transistor circuits to implement weights. However, these efforts are not power- and area-efficient. The biggest stride in the use of alternative solid-state devices to build components of ANNs is using memristive technology [250], [251]. A single memristor incorporates most of the functionalities of a synapse that is used in both ANN and biological neural network. The most important feature of these functions is weight programmability in which the weights are represented by the conductance of the memristor. The simple device structure of a memristor, that is, an insulator between two metals, also enables 2-D and 3-D cross-point architecture that is very efficient in performing matrix multiplication (between inputs and weights) [252], [253]. However, the operation principal of memristive devices which is mostly based on the stochastic movement of ions exposes them to cycle-to-cycle variability. In addition, the memristor physics is still not well-understood and modeled, therefore there is device-to-device variation that makes the scaling of memristive architecture challenging. While the effort toward spin devices for neuromorphic computing is fairly recent and in an early stage, the well-established physics and fabrication process of spin devices gives a larger controllability when used in neuromorphic applications. The weight in a spin device is expressed in the form of its magnetization which is non-volatile and can assume analog values similar to memristive conductance. Since the process of weight modulation in different types of spin devices does not involve physical motion of ions (for most cases), spin devices have a high durability and endurance compared with the memristor counterparts. Future efforts involving spin devices in ANNs should focus on building memristor-like cross-point architectures to demonstrate its scalability.

Going forward, it is also necessary to integrate spin-based synapse and neurons for a complete neural architecture. To achieve general-purpose computation, we may need to mimic biological systems such as a human brain, in which one neuron has 10000 synaptic connections. Obviously, this requirement is beyond our capability using modern fabrication techniques. If we aim to solve a specific problem, however, a typical cross-point architecture can fulfill the job. For the time being, research activities will be focused on developing a particular recognition and optimization hardware such as the ones discussed in [234], [236], and [237] thereby accelerating the field toward real applications. The learning part of the recognition task which is still performed on conventional computer should also be enabled on spin architecture to realize a full spin-based non-Von Neumann computing system.

V. SPINTRONICS FOR FLEXIBLE ELECTRONICS

A huge segment of the future generation of consumer electronics such as wearables, medical implants, and displays depends on the fabrication of electronics components on flexible substrates. A key requirement is that the device performance should be comparable to that when they are fabricated on conventional rigid substrates. In the field of spintronics, the deposition of exchange-biased magnetic layers has been shown on free-standing organic films (e.g., mylar, Kapton, ultem) a few decades back [254]. Later, [Co/Cu]-based GMR multilayers deposited on plastic substrates with a photoresist buffer were shown to have two times larger GMR compared with the films deposited on bare silicon substrate [255]. The GMR value of these multilayers was unaffected by tensile deformation of up to 4.5% when grown on elastic poly (dimethylsiloxane) (PDMS) membranes [256]. These GMR layers were also made into printable ink by dissolving the multilayers deposited on photoresist-coated silicon films in acetone and subsequently mixing the dissolved flakes in a binder solution [257]. Ota et al. [258] have recently shown that GMR devices can even be used for sensing the direction of strain.

Since the MTJs form the backbone of modern spintronic applications, integrating them on flexible substrates has been a topic of active interest [259]–[262]. Co/Al2O3/NiFe MTJs have been fabricated on Kapton substrates which have a robust TMR with stress/bending as shown in Fig. 24(a) [261]. However, it has been shown that the TMR can in fact be engineered with strain for in-plane MTJs with an MgO barrier [259], [260], [263]. In a series of measurements on MTJs fabricated on silicon substrates, it was shown that increasing strain results in a twofold increase in the TMR [260]. The strain on the sample was applied through a clamp and screw setup, and the obtained results are shown in Fig. 24(b) and (c). It was elucidated that while the parallel resistance of the MTJ channel remains same under strain, the antiparallel resistance...
increases, resulting in a larger TMR. The TMR remained small and unperturbed by strain for a non-annealed sample, thereby establishing the sensitivity of quantum tunneling through an epitaxial MgO barrier to strain. In a later work, it has been shown that the MTJ stack when fabricated on a flexible polyethylene terephthalate (PET) substrate exhibits stable and reliable TMR values. In fact, the TMR of the MTJ on the PET was 50% higher when compared with the Si substrates [259]. The MTJs were fabricated by the transfer print process. In this process illustrated in Fig. 25, the MTJs were first fabricated on the Si substrate, and the substrate was etched using dry etching methods. The suspended MTJ stack was then transferred on the PET, glass, Al foil, PDMS, and nitrile glove [see Fig. 26(a)]. Fig. 26(b) shows that the TMR of the device is stable even after application of various degrees of stress over time.

Apart from the GMR and MTJ devices, other important spintronic phenomena and devices have been reliably demonstrated on flexible substrates. Vemulkar et al. [264] have shown successful fabrication of antiferromagnetic nanowires down to 210 nm width on flexible substrates. The switching characteristic of both the film and the fabricated device was as robust as the one grown on Si. Wang et al. [265] showed the voltage control of magnetic anisotropy through ionic liquid gating on Pt/Fe/Pt/Ta film on polyimide flexible substrates. Similarly, successful fabrication of Pt/Co SOT devices has been demonstrated on flexible plastic substrates [266]. The SOT devices on flexible substrates show a stable current-induced switching characteristic under both compressive and tensile bend conditions as shown in Fig. 27.

Strain engineering has been extensively applied to modern p-type field-effect transistors to improve the mobility and to optoelectronic devices to modify the effective hole mass, both of which improved the device performance significantly. In the future, flexible spintronics research should aim toward development of complex spintronic circuits on flexible wafers and integration of silicon components alongside the spintronics counterpart on these flexible wafers. More importantly, active strain engineering to enhance the device performance, detecting the amount of strain and even harvesting the energy, could be envisioned using flexible spintronics devices. A more cross-disciplinary approach which involves adopting learnings from efforts in other flexible electronics counterparts is essential for a faster implementation.

Fig. 24. (a) Measurement setup and the measured TMR for Al₂O₃-based MTJ on Kapton. Reprinted from [261], with the permission of AIP publishing. (b) TMR on MgO-based MTJ deposited on the Si/SiO₂ substrate. The substrate was clamped and bent using a screw underneath. Legend in the figure represents the amount by which screw was rotated to apply strain on the sample. (c) TMR value as a function of screw rotation or the amount of strain on sample. Adapted from [260].
VI. SPINTRONICS IN TERAHERTZ

The electromagnetic (EM) radiations with frequency in the range 100–300 GHz to 3–30 THz are termed as THz radiations, which find applications in spectroscopy, medical imaging, communication, and so on. A low-cost and energy-efficient THz source/emitter is desirable to fully develop these THz systems and further expand their applications. The currently used THz emitters based on photoconductive semiconductors, electrooptic crystals (e.g., ZnTe), air-plasma-based emitters, and so on have drawbacks in terms of narrow bandwidth, skipped bandwidth, or requisite of a high-energy laser pump. In view of these shortcomings, there has recently been wide-ranging research interest to explore spintronic-based THz emitters.

THz emission using spintronic devices is related to ultrafast spin dynamics which was at first revealed in sub-picosecond demagnetization in Ni using a femtosecond laser pulse [267]. It has been proposed that a superdiffusive transport of spin-polarized electron is responsible for this ultrafast demagnetization [268]. This mechanism was later confirmed by an experiment involving the Ni and Fe layer with the parallel and antiparallel alignment between them [269]. When the Ni layer was pumped with a femtosecond laser pulse, an increase (decrease) in the Fe magnetization was observed when the two layers were parallel (antiparallel) to each other. Soon after, Kampfrath et al. [270] used Fe/(Au or Ru) bilayers to detect the superdiffusive spin current.

The schematic of the scheme they used is shown in Fig. 28(a). The laser-induced superdiffusive spin current (\(J_s\)) on arrival in the metallic Au or Ru layer is converted to a charge current (\(J_c = \theta_{SH} J_s \times M/|M|\)) due to ISHE. The charge pulse is converted to an EM wave with a frequency in the THz spectrum, governed by Maxwell’s equation. The THz radiation was electro-optically sampled, the results of which are shown in Fig. 28(b). It can be seen that a reversal of the magnetization results in a corresponding reversal of the THz signal due to the reversal in the direction of \(J_s\). It should be noted that the emitted THz were polarized in the \(x\)-direction for the sample magnetization \(M\) along the \(y\)-direction in Fig. 28(a).

Since both Au and Ru are not the materials with large \(\theta_{SH}\), the emitted THz was of limited amplitude. Seifert et al. [271] and Wu et al. [272] have performed extensive studies about different NM and FM combinations to realize efficient, broadband, and high-performance spintronic THz emitters. Fig. 29(a) shows the comparison of the amplitude of the emitted THz for NMs adjacent to a Co FeB layer. A combination of Pt/CoFeB emits the strongest THz signal. For a W and Ta sample, the emitted THz is of opposite sign compared with others due to the opposite \(\theta_{SH}\) of these metals. The THz emitter optimized for the NM and FM thicknesses by Wu et al. [272] is shown in Fig. 29(b) and (c). An increase in the THz signal for increasing HM and FM thickness followed by its attenuation is a result of balance between the limited spin diffusion and THz absorption in the two layers. It has also been proposed that the
Multilayers of [Pt (2 nm)/Fe (1 nm)/MgO (2 nm)] onances), especially in terms of its broad frequency coverage. ters (showing limited frequency responses due to phonon res- the spintronic THz emitter outperforms these traditional emit- with other crystal and semiconductor-based emitters. Clearly, time- and frequency-domain spectra of this spintronic trilayer structure, optimized for individual layer thickness, emits a very peak THz signal for a particular thickness is possibly due to constructive Fabry–Pérot interference at this thickness [271]. Seifert et al. [271] showed that a Pt/CoFeB/W heterostructure, optimized for individual layer thickness, emits a very strong and broad THz. Fig. 30 shows the comparison of the time- and frequency-domain spectra of this spintronic trilayer with other crystal and semiconductor-based emitters. Clearly, the spintronic THz emitter outperforms these traditional emitters (showing limited frequency responses due to phonon resonances), especially in terms of its broad frequency coverage. Multilayers of [Pt (2 nm)/Fe (1 nm)/MgO (2 nm)]_n with different repetition numbers also serve as an excellent THz source [273]. A peak THz emission was found for three repetitions of these layers. Apart from conventional HMs, exotic materials such as a TI Bi2Se3 [274] and monolayer MoS2 [275] in combination with Co have been demonstrated to emit sizeable THz waves (see Fig. 31). Attachment of a collimating Si lens was proposed to collect most of the diverging THz to maximize the power output [276]. The THz can also be enhanced by passing currents through the heterostructure resulting in an additional photoconduction-related contribution to the total THz [277].

While the initial reports on THz generation assume an essential presence of net magnetization in the system for a finite THz generation, recent THz emitter reports based on nearly compensated FIMs have proved it otherwise. Chen et al. [278] have demonstrated emission of a finite THz signal from a nearly compensated Co1−xGdx/Pt-based heterostructure. The magnitude of this THz is comparable to the pure Co-based emitter. In fact, the polarity of the emitted THz reverses when the composition of Co1−xGdx traverses from a Co-rich to Gd-rich state as shown in Fig. 32(a) and (b). This behavior of RE-TM base THz emitter is due to the localized nature of the magnetic moment carrying f-shell electron in the RE metals. Therefore, the contribution to the superdiffusive spin current is only from the Co sub-lattice. Similar results were reported by Schneider et al. [279] for another RE-TM FIM, Fe1−xTbx. It was found that a CoGd heterostructure emits a stronger THz compared with the CoTb ones possibly due to a large out-of-plane anisotropy in CoTb [280]. The anomalous Hall effect (AHE) as a possible alternate mechanism of THz generation instead of ISHE has been put forward recently [281]. A single FeMnPt layer without an HM was found to generate considerable THz as shown in Fig. 32(c).

To summarize this section, magnetic heterostructures provide a cheap and efficient solution for THz generation. The peak intensity of the generated THz from an NM/FM structure exceeds compared with that from ZnTe- and GaP-based emitters (500 μm) which are conventionally used for THz generation. While the ZnTe and GaP THz spectrum shows considerable gaps, specifically between 3 and 13 THz, the spectrum of the spintronic THz emitter is wider and continuous. The THz amplitude for most of the spectral ranges from spintronic emitters exceeds that of the ZnTe- and the GaP-based emitters. When compared with a photoconductive switch, the spintronic emitter has a wider bandwidth with a larger intensity above 3 THz. For frequency below 3 THz, a photoconductive switch performs better [271]. A significant enhancement of the THz signals in a lower THz frequency range below 1 THz can be achieved by a novel ultra-broadband spintronic THz emitter enhanced by a current modulation through the semiconductor channel [277].

The spintronics THz emitter films are easy to fabricate and do not require any high-temperature deposition process or specific substrate. Future works on spintronic THz emitters should be focused on further improvement of the THz signal at lower laser fluence, removal of the external magnetic field, and enabling robustness to external temperature and magnetic fields.

VII. OUTLOOK

Ever since its use in the magnetic-core memory, spin devices have come a long way to be used in nanometer dimensioned STT memories. Apart from forming backbone of mass storage in the form of hard disk, almost all the modern-day devices and instruments are packed with magnetic sensors of various types. With the end of Moore’s law in sight, finding replacement of silicon logic devices is at the forefront of solid-state device research. While there is a continuous stride toward development of spin-based logic devices as discussed in this review, the spin logic research is still in a very preliminary
stage. Currently, most of these spin logic devices have been demonstrated in the form of stand-alone gates or logic elements. The viability of a complete spin logic architecture can only be ascertained if the individual spin elements are suitably integrated. The future direction of spin logic research should aim toward this assimilation. Apart from this, for all practical purposes any logic device should not only perform the said logic function but also be capable of meeting other important parameters such as low power, large fan-in, large fan-out, and high speed. Future efforts on spin logic devices should focus on developing devices that meet all these criteria. Overall, spin logic circuits require continuous research efforts to become practical in the distant future.

Spintronic memories or MRAM have proven to be one of the most successful spintronic applications. In fact, they are one of the most promising among all the non-volatile memory candidates currently being pursued. The second-generation MRAM, that is, STT-MRAM, is already mass produced and serving customer needs in companies such as Everspin, USA, GlobalFoundries, Singapore, and Samsung, South Korea, among those involved in its active production and development. The next iteration of MRAM involving the use of SOTs is a focus of major research in both academia and industry due to their promising high speed and large endurance. The MRAMs are currently developed as standalone memories and for embedded applications. One of the target applications of MRAM is in a form of cache to enable low-power computing. However, STT-MRAMs at their few to tens of nanoseconds read speed still fall short of the speed requirements of the L1/L2 cache. The promising high speed of SOT-MRAM due to low incubation times makes them a competitive candidate for L1/L2 cache. However, currently one hindrance toward practical applications of SOT-MRAM is the requirement of external magnetic field for their deterministic switching operation. While many device structures and engineering solutions have been proposed to overcome this problem, a full-scale integration of these SOT devices with CMOS-compatible process is yet to be seen. The future research work on MRAM should also focus on device scaling and development of a high-density MRAM architecture. MRAMs outperform both the conventional non-volatile solid-state storage like eFLASH and standalone memories, that is, DRAM in all performance aspects other than their storage density. This makes MRAMs cost-ineffective as of now. Future works toward improving their storage density will definitely make them a lot more competitive in a broader
range of memory pyramid. In addition, the potential of other magnetic memory candidates such as skyrmions should also be continuously evaluated.

The field of solid-state devices for non-von Neumann computing itself is in a very early stage with majority of success being shared by memristors. However, recently there have been continuous demonstrations of non-von Neumann systems using spin devices. This suggests the viability of spintronics as one of the promising approaches for pursuing alternative computing methodologies [234], [236], [237]. Being a field under development, alternative computing schemes do not yet have a coherently defined requirement from the devices and systems. In both memristor and spintronics, the researchers, with the tools in their hands, are proposing various standalone devices and architectures which although solving the specific problem in question fall short of marching toward a coherent and a general-purpose hardware for alternative computing needs. Since the viability of spintronic devices for ANNs, biological neural network, and other computing schemes has already been suggested, the next step should be toward a more joint effort between the device, circuits, and system architecture teams for obtaining tangible spin solutions. At present, the ANNs and ANN-like systems made from memristors and spintronics perform only the inference step, while learning and sometimes even weight storage are still carried out in conventional computers. Going forward, while it is desired to move the learning tasks to new solid-state devices, a hybrid
architecture can be a more practical option. Like spin logic, the real application of spins in unconventional computing will become clearer in the coming decade.

As detailed in this review, spintronics should not only be approached as a device candidate for computing applications but also its physics should be exploited for non-computing systems. In the form of a THz emitter, the spin devices have already proved themselves very competitive. A fast track development of THz systems based on these devices can be in fact applied to some applications in the coming few years. While in this review we have discussed some of the major emerging applications of spintronics, there are analogous ongoing research efforts for several other equally important applications, for example, spin-based electronic oscillators [282]–[284] which may find their use in both communication and computing. The low complexity and less stringent device requirement of non-computing systems should aid spintronics researches to quickly transfer a research device from an academic laboratory to industry, which requires not only a functionality testing of an individual device but also manufacturability and scalability aspects. Finally, flexible electronics will be playing a big role in the future, especially in consumer electronics. Works of any spin device on rigid wafers such as silicon for both computing and non-computing needs should have an analogous effort toward developing them on flexible substrates.

VIII. CONCLUSION

In this review, we have discussed the novel emerging areas of spintronic applications. Spin devices proposed for the logic
computation were discussed in Section II. The low static power consumption of spin elements makes them attractive for logical devices. However, full replication of the speed and versatility offered by the CMOS is one of the foremost challenges in this area of research. In Section III, spintronic memories were discussed with emphasis on the latest generation of spin memories, that is, SOT-MRAM. The SOT which requires a simpler device design promises larger endurance and smaller energy consumption when compared with the currently commercialized STT-MRAM. Current efforts to improve the energy efficiency of SOT devices involve engineering the SOC source, magnetic layer, and the heterostructure stack design itself. In addition, oxygen incorporation in various layers has proved to be an effective way to modulate and enhance the SOTs. Alternative computing methodologies not based on Von Neumann architecture are currently being pursued actively for their critical future importance. In Section IV, we discussed the recent research progress in this area with respect to the emerging spin devices that mimic the biological synapse and neuron functions. The optimization and recognition systems based on MTJs have been proposed to be both area- and energy-effective when compared with similar implementation using CMOS. The viability of spintronics devices for flexible electronics was discussed in Section V. Several spintronic devices such as GMR, TMR, SOT, and exchange devices have been shown to perform robustly on a variety of flexible substrates such as plastic, Kapton tape, PDMS, and PET. In Section VI, we detailed on the advancement of cost-effective THz emitter based on magnetic/NM heterostructures. The THz emitted from these spin devices are of equivalent strength and much broader bandwidth compared with the conventional crystal and semiconductor-based emitters.

Overall, we see that spintronics has emerged as a very promising and an actively pursued solid-state technology for meeting the future (opto)electronics needs in a wide variety of application areas. Future spintronic research should focus on improvement of spin device on all fronts that concern the stringent requirement of device practicality. In addition, research concerned toward system-level implementation of spintronics should also be pursued.

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