Seven-bit reconfigurable optical true time delay line based on silicon integration

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Abstract: We design, fabricate, and characterize a 7-bit reconfigurable optical true time delay line consisting of Mach-Zehnder interferometer (MZI) switches on the silicon photonics platform. Variable optical attenuators (VOAs) are embedded to suppress the inter-symbol crosstalk caused by the finite extinction ratio of switches. The device can provide a maximum of 1.27 ns delay with a 10 ps resolution over a wide wavelength range. Eye diagram measurement of a 25 Gbps 2^25−1 pseudo-random bit sequence (PRBS) signal reveals the power penalties only increase 0.17 dB and 0.77 dB after transmission through the shortest (reference) and the longest (1.27 ns delay) paths, respectively.

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1. Introduction

Optical delay lines provide a feasible solution for data synchronization, buffering in high capacity optical networks [1–4] and ultrahigh speed signal processing in radar systems [5]. Reconfigurability is required in practical applications. It is usually realized by switches connected with fibers or waveguides in different lengths, where the optical route is selected by changing the state of the switches, enabling discrete delay tuning [6]. Fiber based reconfigurable true time delay lines (RTTDL) using discrete components has been demonstrated [7]. Unfortunately, the inherent features of fiber optics, such as low insertion loss, are counteracted by the bulkiness and difficulty in implementation, e.g., fiber length precise control. A more attractive and practically feasible approach is to realize RTTDL on an integrated waveguide platform. Smaller footprint, higher delay accuracy and stability as well as lower cost can be expected. Up to date, RTTDLs integrated on different waveguide platforms have been successfully demonstrated, such as 4-bit RTTDL using polymer optical switches and waveguide delay lines [8, 9], silica-based RTTDL fabricated by the planar
lightwave circuit technique [10, 11], 4-bit RTTDL using thermo-optic switches based on Si$_3$N$_4$ planar platform [12].

Compared to the polymer, silica, and Si$_3$N$_4$ platforms, silicon platform with the key merits of high compactness and compatibility with complementary-metal-oxide-semiconductor (CMOS) technologies has been regarded as a promising solution for converging electrical and optical systems on a single chip [13, 14]. It can integrate $p-i-n$ diodes for nanosecond tuning, much faster than the thermal tuning method [15]. Multiple schemes to realize tunable delay lines on the silicon photonics platform have been reported, such as side-coupled integrated spaced sequence of resonators (SCISSORS) [16–20], coupled resonator optical waveguides (CROWs) [21–23], photonic crystal (PhC) waveguides [24], and gratings [25].

In our previous work, we proposed and theoretically analyzed the silicon based RTTDL [26]. In this paper, we experimentally demonstrate a 7-bit RTTDL on the silicon photonics platform. It can achieve the maximum delay of 1.27 ns with a 10 ps resolution. The transmission performance is tested and the measured results verify our design. In comparison with the slow light structures, although our RTTDL may not be so compact, it has a large delay tuning range over a broad spectral window with low loss and low group delay dispersion (GDD).

## 2. Device design and fabrication

![Fig. 1. (a) Topologic structure of the silicon N-bit RTTDL. (b) 3-D view of the single-arm-modulated MZI used as an optical switch. (c) Cross-sectional view of the $p-i-n$ diode for optical phase tuning and optical power attenuation.](image-url)

A schematic diagram illustrating the working principle of the silicon N-bit RTTDL is shown in Fig. 1(a). Our device consists of 8 cascaded $2 \times 2$ Mach-Zehnder interferometer (MZI) switches and 7 stages of waveguide pairs. Variable optical time delays are obtained upon selection of the long delay path or the short delay path (reference) in each stage by the MZI switches. Long waveguides are necessary to achieve a large delay and hence waveguide propagation loss has to be minimized in the design. The device is based on ridge-type waveguides with a height of 220 nm and a slab thickness of 60 nm. In order to reduce the sidewall scattering loss, wide waveguide delay lines of 3 $\mu$m in width are employed. The dispersion of our waveguide is $-1300$ ps/nm/km simulated by MODE SOLUTION package from Lumerical Corp. In the bending part, the waveguide width is thinned down to 0.5 $\mu$m.
using a 200-μm-long taper to avoid excitation of high-order modes. The short delay path in each stage has a length of ~4 mm. The delay step is designed to be Δt = 10 ps (corresponding to a waveguide length difference of ΔL = 808 μm). Compared with grating or photonic crystal waveguides, our waveguide is long for the same delay, but it has broad operation band, low loss, and low GDD. The delay difference of the waveguide pair in the Nth stage is 2^{N-1}Δt. Hence, the tuning range of our 7-bit RTTDL is from 0 to 1.27 ns relative to the reference path. Figure 1(b) shows the three-dimensional perspective view of the single-arm-modulated MZI used as an optical switch. The 2 × 2 multimode interference (MMI) couplers in the MZI switches are 5 μm wide and 31.5 μm long. The input and output waveguides of the MMI are 0.5 μm wide and 3 μm wide. They are connected through 200-μm-long tapers. To actively tune the optical phase, we embed a p-i-n diode across one waveguide arm as a phase shifter. Figure 1(c) shows the cross-sectional schematic of the p-i-n diode. The highly doped p⁺ and n⁺ regions are 600 nm away from the edges of the ridge waveguide to prevent absorption loss from the highly doped regions. When an external voltage is applied on the p-i-n junction, carriers are generated inside the waveguide. Hence, the refractive index of the waveguide changes due to the free carrier dispersion (FCD) effect of silicon. A long active arm of 5.27 mm is used in order to lower the π-phase shift voltage and thus alleviate the absorption loss upon turn-on. As we previously analyzed, VOAs are inserted in each waveguide as depicted in Fig. 1(a) to attenuate the undesired signal in the off-paths, so as to suppress the inter-symbol crosstalk arisen from the limited extinction ratio of MZIs [26]. In the VOAs, a 6 mm long p-i-n diode, with the same structure shown in Fig. 1(c), is used. High waveguide loss is induced by the free carrier absorption (FCA) effect when a positive voltage is applied.

The device was fabricated using the standard CMOS fabrication processes on a silicon-on-insulator (SOI) wafer. The top silicon layer has a resistivity of 10 to 15 ohm·cm (corresponding to a hole concentration of ~10^{15} cm⁻³). The device patterns were defined by 248-nm deep ultra-violet (DUV) photolithography and plasma dry etched with a depth of 160 nm to form a 60 nm slab. Boron and phosphorus ion implantations were used to achieve a doping concentration of ~10^{20} cm⁻³ for the p⁺ and n⁺ regions. A 1.5 μm thick silicon dioxide layer was deposited using plasma-enhanced chemical vapor deposition (PECVD). The contact holes were etched through before Aluminum (Al) layer was sputtered and patterned. Figures 2(a) and 2(b) shows the mask layout and optical microscope image of the fabricated device, respectively. The device has a footprint of 7.4 mm × 1.6 mm = 11.84 mm². The device is designed to operate in the transverse-electric (TE) polarization (electric-field parallel to the device plane). Light is coupled into and out of the device through on-chip grating couplers using an optical fiber array. A waveguide tap is added to each short waveguide segment with a power coupling ratio of 0.013 to facilitate the test of each switch. The input, output, and test ports are all routed to form an array with a pitch of 127 μm at the chip edge for convenient coupling with a fiber array. In order to apply voltages onto the p-i-n diodes, we used gold (Au) wire bonding to connect with a printed circuit board (PCB). Figure 2(c) illustrates the device after wire-bonding with the PCB. The dimension of the Al pads on chip is 120 × 150 μm². The diameter of the Au bonding wires is about 25 μm. The Au pads on the PCB have a dimension of 200 × 200 μm² separated by 200 μm. Figure 2(d) shows the Au wire-bonding between the device and the PCB.
3. Experimental results

We first characterize the MZI switch performance. The laser light at 1550 nm is coupled into the input port 1 and the polarization is optimized for TE mode via a polarization controller. The output optical power from the test port of the first stage is recorded. A voltage is then applied on the p-i-n diode of the MZI switch to induce a π-phase shift, leading to decreased optical power from the test port. The switch extinction ratio (ER) is measured to be around 13 dB. The limited ER is due to several factors including uneven power splitting of the MMIs and the unbalanced waveguide loss between MZI arms.

We then use the Agilent loss and dispersion analyzer (86038B) to measure the device transmission spectra. The input port is port 2 and the output port is port 4. As the MZI switches have a limited ER, light can also partially enter the off-paths. Therefore, light from all paths will interfere, giving rise to inter-symbol crosstalk and consequently deteriorating the output signal. Figures 3(a) and 3(b) show the transmission spectra after 0 and 1.27 ns delays without VOAs, respectively. Because of the interference, large power fluctuations are observable from the spectra. Figures 3(c) and 3(d) show the transmission spectra with 4 VOAs at the odd stages turned on with an attenuation of ~10 dB. It can be seen that the power fluctuation is greatly reduced to a magnitude of only about 4 dB after using VOAs.
Fig. 3. Measured transmission spectra of the device. (a) 0 delay without VOAs; (b) 1.27 ns delay without VOAs; (c) 0 delay with VOAs; (d) 1.27 ns delay with VOAs.

We next measure the optical signal delay after transmission through the device. Figure 4 shows the experimental setup. A continuous wave (CW) light at 1550 nm wavelength is generated by a tunable laser followed by a polarization controller. The light is modulated by an amplitude modulator driven by a non-return-to-zero (NRZ) $2^7-1$ pseudo-random bit sequence (PRBS) signal generated by a pulse pattern generator (PPG). The data bit rate is 25 Gbps (for delays of 10, 20 and 40 ps), 10 Gbps (for delays of 80, 160, 320, and 640 ps), and 3 Gbps (for delays of 1.27 ns). The modulated signal is amplified by an erbium-doped fiber amplifier (EDFA), followed by a band pass filter (BPF) to suppress the amplified spontaneous emission (ASE) noise. The optical signal is then coupled into the device and the output signal is amplified by another EDFA to compensate for the device insertion loss. A photodiode (PD) is used to convert the optical signal to the electrical domain and finally recorded by a 32 GHz bandwidth oscilloscope (OSC).

Fig. 4. Experimental setup for optical signal transmission experiment. PPG: pulse pattern generator; BPF: band-pass filter; PC: polarization controller; EDFA: erbium doped fiber amplifier; AM: amplitude modulator; PD: photodetector; DUT: device under test.

Figure 5 shows the measured output optical waveforms after transmission through the device with various delays. The reference output (blue lines) is obtained by configuring the
delay line into the shortest path. Then we change the switch state at each stage so that the longer waveguide segment is selected one by one to increase the optical delay (red lines). As the waveguide length difference doubles at the next stage, the relative delay is also doubled as shown by the first 7 panels in Fig. 5. If all the longer waveguide segments in the 7 stages are selected, the output signal experiences the maximum delay of 1.27 ns as shown by the bottom panel. A total number of $2^7 = 128$ different delays can be selected by flexible combination of switch states.

![Fig. 5. Measured optical output waveforms from the device showing 10 ps to 1.27 ns optical delays. The blue lines are the reference signals passing through the shortest path. The red lines represent various delayed signals upon reconfiguration of the delay line. The relative delay values are labeled on the graphs.](image)

Table 1 summarizes the performance of our RTTDL according to Fig. 5. The insertion loss of the reference path is 6.2 dB, mainly coming from the switch loss (0.38 dB per switch) and waveguide loss (3.15 dB). The 640 ps delay at the 7th stage only incurs an additional 4.8 dB loss comparing to the reference one, suggesting an average waveguide propagation loss of about 0.9 dB/cm. The average power consumption of MZI switches for inducing a $\pi$-phase shift is around 18 mW. Due to fabrication errors and thermal crosstalk, the initial state of each MZI switch might not be at the cross-state. Extra power consumption is needed to correct the phase errors, and therefore, the total switching power to set up a certain delay path is larger than the aggregate power required for $\pi$-phase shifts. The power consumption of each VOA when providing a 10 dB attenuation is 320 mW. Our measurement reveals that, in order to save the power, not all VOAs need to be turned on. The improved transmission spectra in Figs. 4(c) and 4(d) were obtained using 4 VOAs. It should be noted that the usage of VOAs is
due to the limited ER of switches. In principle, if the ER of switches increases to 24 dB which is feasible for MZI structures [27], no VOAs are needed. The delay line structure thus can be simplified and the power consumption can also be reduced considerably.

**Table 1. Summary of the RTTDL Performance**

| Stage | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | all |
|-------|---|---|---|---|---|---|---|---|-----|
| Delay (ps) | 0 | 10 | 20 | 40 | 80 | 160 | 320 | 640 | 1270 |
| IL (dB) | 6.2 | 6.3 | 6.4 | 6.5 | 7 | 7.5 | 9 | 11 | 16 |
| Switch power (mW) | 23.5 | 52.3 | 70.4 | 50.5 | 42.6 | 41.4 | 34.1 | 31.7 | 105 |

Lastly, we examine the quality of the delayed optical signal by measuring the eye diagrams. Figure 6(a) shows the system back-to-back (BtB) eye diagram of a 25 Gbps $2^{51} -1$ PRBS signal. The Q factor of the eye diagram is 9.68 and the jitter is 3.02 ps. Figures 6(b) and 6(c) show the eye diagrams of the optical signal passing through the shortest (reference) and the longest (1.27 ns delay) paths, respectively. The Q factors of these eye diagrams are reduced to 6.83 and 5.33 with the jitter increased to 3.41 ps and 3.91 ps, respectively. The degradation is primarily due to the increased insertion loss. We can deduce the power penalty from the measured eye diagrams. The power penalty $\delta$ in decibel (dB) unit is related to the signal extinction ratio $r_e$ as $\delta = 10\log_{10}(r_e + 1) / (r_e - 1)$ [28], where $r_e$ is defined as $r_e = p_1 / p_0$ with $p_0$ being the signal off-state power and $p_1$ on-state power. The power penalties only increase 0.17 dB and 0.77 dB after the shortest and longest paths, respectively. For the 25 Gbps optical signal (bit period 40 ps), our delay line can buffer 1270ps/(40ps/bit) = 31.75 bits. If a higher speed optical signal is used, it can buffer more bits without being bounded by the delay-bandwidth product as normally encountered in slow-light or resonance delay lines. The delay tuning resolution of our RTTDL is 10 ps, and hence for a 100 Gbps optical signal, our device can maximally buffer 127 bits with a single bit resolution.

As our device is a true time delay line, it should have time delay invariance to different RF frequencies. To verify this property, we measured the phase of the delayed optical signal as a function of frequency for the shortest (reference) and longest (1.27 ns) delay paths as shown in Figs. 6(d) and 6(e), respectively. The measurement was performed using an RF
vector network analyzer (Agilent PNA-X Network analyzer N5247A). Both of the phases have a linear response to the signal frequency, from which we can derive the group delay of the longest path relative to the shortest one as \( \tau_g = -d\phi/d\omega \approx 1.3 \text{ ns} \), consistent with our optical waveform measurement shown in Fig. 5.

Table 2 lists the comparison of our RTTDL with various state-of-the-art integrated tunable optical buffers including SCISSORs, CROWs, photonic crystal waveguides (PhCWs), Bragg gratings, MEMS actuated optical delay lines [18, 29–36]. It can be seen the key merits of RTTDLs are the large delay tuning range, broad operation window, and low loss.

Table 2. Comparison of Various Optical Delay Lines Obtained from Some Example Devices

| Device  | Delay range (ps) | Tuning resolution (ps) | Working bandwidth (nm) | Delay loss (dB/ps) | Power efficiency (mW/ps) | Device footprint (mm²) |
|---------|-----------------|------------------------|------------------------|-------------------|-------------------------|------------------------|
| SCISSORs [18,29,30] | 345 | 1.6 | >0.08 | 0.06 | 0.22 | 0.03 |
| CROWs [31] | 800 | 54 | 0.096 | 0.01 | 5 | 7 |
| PhCWs [32,33] | 54 | <1 | 3 | 0.3 | 11 | 16.48 |
| Grating [34] | 96 | small | 0.8 | 0.001 | 11 | 0.015 |
| 4-bit RTTDL [12] | 12350 | 850 | large | 0.001 | 0.02 | 3825 |
| MEMS [35,36] | 94 | small | 0.04 | 0.24 | - | 0.001 |
| Our work (7-bit RTTDL) | 1270 | 10 | large | 0.013 | 1.09 | 11.84 |

4. Conclusion

We demonstrated for the first time a compact silicon-based RTTDL achieving a maximum of 1.27 ns delay with a 10 ps resolution. The RTTDL is composed of 8 MZI switches and 7 waveguide pairs with an incremental length difference. The transmission spectra were measured and optical delay was characterized by transmission of PRBS signals. A major factor that affects the delayed optical signal is the inter-symbol crosstalk induced by the limited ER of MZI switches. To improve the signal quality, we used VOAs with 10 dB attenuation to reduce the residual signals in the off-paths. The transmission of a 25 Gbps 2^{21}-1 PRBS signal confirms the signal fidelity after the maximum delay of 1.27 ns. Due to its broad optical bandwidth, the RTTDL is insensitive to wavelength, which is desired in many practical applications.

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