A method to shorten the frequency hopping time of fractional-N phase-locked loop

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Abstract This paper proposes a frequency hopping method of multiple insertions of frequency points (MIFP) to shorten the lock time of fractional-N Phase-locked loop (PLL) in the large frequency hopping (FH) interval mode. Several frequency points between initial frequency and desired-frequency are inserted to steer the frequency up or down (multiple small FH step instead of direct large FH interval), which can ensure that the response processes are linear under-damped. The transient response process of PLL is theoretically analyzed and the feasibility of this method is verified by simulation. Moreover, this method is applied on radar local oscillators (LOs). Measurements show that 8us of the frequency hopping time can be reduced by using MIFP method compared with traditional direct frequency hopping from 2.0GHz to 2.8GHz with the loop bandwidth of 200kHz.

Keywords: phase locked loop, large hopping interval, nonlinear response, underdamped response, fast frequency hopping, MIFP

1. Introduction

With the development of wireless receivers and radar system, system performance is greatly determined by the hopping speed of LOs. The FH speed of Ultra-wideband (UWB) LOs is relatively low due to the large hopping interval and long tracking time. Therefore, it is meaningful to shorten the FH time of UWB PLL.

Many researches on FH time and FH speed have been carried out [1, 2, 3, 4, 5, 6, 7, 8, 9]. The circuit architectures to increase the hopping speed mainly include Direct Digital Synthesizer (DDS), DDS+PLL, dual-path PLL, etc [10, 11, 12, 13, 14]. DDS has short FH time, but poor spurious performance and low output frequency. DDS+PLL architecture has the advantages of high output frequency, but the FH time is relatively long due to the output frequency is achieved by PLL. The dual-path PLL structure can realizes fast switching between two frequency points by sacrificing volume and power consumption.

Compared with the above architectures, conventional fractional-N PLL has been more widely used due to its simple structure and low cost. Meanwhile, there are several methods [15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26] to further shorten the lock time of the fractional-N PLL. One of these methods uses dynamic loop bandwidth which can realize fast tracking with wide bandwidth at the state of out of lock. After lock-in, the diode is clamped to reduce the loop bandwidth and achieve good performance of out of band suppression [18, 19, 20, 21]. The method of adding fast capture circuit [22, 23, 24, 25, 26] is to transmit the tuning voltage of the next frequency point in advance so as to reduce the loop cycle process and accelerate the locking. However, loop design of the above two methods is more complex, which increases the difficulty of later circuit tuning.

This paper proposes a method of MIFP to shorten the FH time without adding hardware circuit on fractional-N PLL architecture. Several frequency points are successively inserted to accelerate the steering process of PLL towards lock-in. By analyzing the process of transient response, the effects of FH interval and loop bandwidth on lock time are demonstrated. This proposed method is verified by simulation and measurement.

2. Theoretical analysis

The transient response processes of PLL mainly have two stages including non-linear tracking response and linear response. As shown in Fig. 1, \( f_{\text{lock}} \) represents the FH interval boundary of linear response [27], which would present different transient response states. When the FH interval \( \Delta f < f_{\text{lock}} \), PLL directly work in the linear response state. The rising slope of transient process is large, and the lock time is short. When \( \Delta f > f_{\text{lock}} \), PLL enters the non-linear state followed by the linear state, which lead to the rising slope is small, and the lock time is longer.

2.1 Non-linear response

The transient processes of PLL are conventionally analyzed in linear model and ignore some non-ideal factors. When FH interval exceed linear response range, the frequency tracking behavior of fractional-N PLL are achieved by charge pump

![Fig. 1 The process of transient response with direct FH.](image-url)
(CP) and loop filter (LF). Therefore, nonlinear factors such as CP and Phase Detector (PD) play a role in the accuracy of modeling the non-linear stage.

When CP works, the frequency traction is realized by converting phase difference \( \Delta \phi \) between reference and desired-frequency into current. This conversion is transmitted in the form of current. The voltage expressed as a linear slope is formed through the nonlinear integration of the LF and then the VCO is tuned. The concept of voltage conversion rate can be proposed to approximate the process of charge pump tracking frequency. According to the closed loop transfer function model in Fig. 1, the voltage conversion rate \( V_{PLL} \) of PLL can be given by the following formula [27]:

\[
V_{PLL} = \frac{K_0K_d}{(C_1 + C_2)} \frac{H_z}{S}
\]

(1)

where \( K_0 \) is the gain of VCO, \( K_d \) is the gain of PD and charge pump.

For conventional fractional-N PLL, \( f_{\text{Delta}} \) is influenced by \( V_{PLL} \). PD dead time \( \tau \), and the value of loop capacitance [28, 29, 30]. \( f_{\text{Delta}} \) is determined by formula (2):

\[
|f_{\text{Delta}}| \leq \frac{1.25N(1 - \frac{2\tau}{T_{\text{ref}}})V_{PLL}RC_2}{2\pi}
\]

(2)

where \( T_{\text{ref}} \) is the cycle of the reference clock, \( \tau \) is a fixed value related to the design of the charge pump in the chip. A larger \( V_{PLL} \) leads to a larger \( f_{\text{Delta}} \) resulting in a greater FH interval \( \Delta f \) of the linear response. Since the CP gain does not exceed 5 mA for most PLLs, the max \( \Delta f \) of linear response would be limited.

The time of non-linear tracking stage can be approximately given by the following formula [28]:

\[
t_{\text{nonlinear}} = \frac{2(C_1 + C_2)}{K_0K_d} |\Delta f - f_{\text{Delta}}|
\]

(3)

According to the above formula, the time of nonlinear traction is prolonged when the frequency change distance is increased.

### 2.2 Linear response

The linear response stage can be approximated by continuous S-domain model. The third-order PLL with second-order passive LF is selected for modeling because the order of PLL does not affect the transient response characteristics. The closed loop model of PLL is shown in Fig. 2.

The open-loop transfer function of this system \( H_0(S) \) [31] is:

\[
H_0(S) = \frac{K_0K_dF(S)}{S}
\]

(4)

\( F(S) \) is the transfer function of the second-order LF with the following expression.

\[
F(S) = \frac{1 + SR_1C_2}{S(C_1 + C_2)(1 + \frac{SR_1C_2}{C_1 + C_2})}
\]

(5)

According to the feedback system theory, the closed-loop transfer function is:

\[
H(S) = \frac{\Phi_1(S)}{\Phi_0(S)} = \frac{H_0(S)G(S)}{1 + H_0(S)G(S)}
\]

(6)

Substituting \( F(S) \), \( G(S) \) into the above function \( H(S) \), the system function can be rewritten as:

\[
H(S) = \frac{S + 1/T}{A_0S^2 + A_1S + S + 1/T}
\]

(7)

where \( A_0 = C_1N/(K_0K_d) \), \( A_1 = (C_1 + C_2)N/(K_0K_dR_1C_2) \), \( T = R_1C_2 \).

Since the non-dominant poles and zeros of the closed loop model do not change the damping properties [32], the above formula can be simplified as follows:

\[
H(S) \approx \frac{\omega_n^2}{(S^2 + 2\xi\omega_nS + \omega_n^2)}
\]

(8)

where natural frequency \( \omega_n = \sqrt{\frac{K_0K_d}{N(C_1 + C_2)}} \), damping ratio \( \xi = \frac{\omega_nR_1}{2} \).

By inverting Laplace transform of \( H(S)U(S) \), the corresponding time-domain expression of step response can be obtained as follows:

While \( 0 < \xi < 1 \):

\[
S(t) = 1 - e^{-\xi\omega_n t}\cos(\omega_n\sqrt{1 - \xi^2}t) + \frac{\xi}{\sqrt{1 - \xi^2}}e^{-\xi\omega_n t}\sin(\omega_n\sqrt{1 - \xi^2}t), t > 0
\]

(9)

While \( \xi > 1 \):

\[
S(t) = 1 + A e^{\omega_n(\xi + \sqrt{\xi^2 - 1})t} + B e^{-\omega_n(\xi - \sqrt{\xi^2 - 1})t}
\]

(10)

where \( A = -\omega_n(\xi + \sqrt{\xi^2 - 1})/2\sqrt{\xi^2 - 1} \), \( B = \omega_n(\xi + \sqrt{\xi^2 - 1}) - 2\sqrt{\xi^2 - 1} \), \( 2\sqrt{\xi^2 - 1} \).

Response curve of \( S(t) \) versus \( t \) is shown in Fig. 3. With the decrease of damping factor \( \xi \), the response of the system is faster and the rise time is shorter, which means that the system is under-damped.

For the closed-loop system, the loop bandwidth \( \omega_{3dB} \) is the bandwidth when the amplitude drops to 3 dB below \( |H(j\omega)| \). Since the amplitude of unit step response \( |H(j\omega)| \) equal to 1, substituting \( |H(j\omega)|_{dB} \) into (8) the following equation can be obtained:

\[
\omega_{3dB} = \omega_n [1 - 2\xi^2 + \sqrt{(1 - 2\xi^2)^2 + 1}]^\frac{1}{2}
\]

(11)

Set \( A = \left(\frac{\omega_{3dB}}{\omega_n}\right)^2 \):

\[
dA = \frac{-4\xi}{\sqrt{(1 - 2\xi^2)^2 + 1} + (1 - 2\xi^2)^2}} < 0
\]

(12)

Therefore, \( A \) and \( \xi \) is inversely proportional. A wider \( \omega_{3dB} \) equal to a smaller damping factor \( \xi \) would lead to a faster response.
response.

3. Simulation verification of MIFP method

In this section, the FH processes are simulated and verified through ADIsimPLL software. The linear FH interval $\Delta f_{\text{lock}}$ is determined when PLL to be used is determined. The maximum FH distance is 2.0–2.8 GHz of the PLL designed in this paper, and the PD frequency is 10 MHz. Taking out-of-band spurious suppression into account, the loop bandwidth $\omega_{3\,\text{dB}}$ should be less than 1/50 of PD frequency at least. Therefore, $\omega_{3\,\text{dB}}$ is set to 200 kHz in simulator that is optimal value according to the above analysis.

Fig. 4 shows the simulation results of the direct FH process. The tracking time from 2.0 GHz to 2.8 GHz is about 9.8 us, and the final phase-locked time is 24.4 us within a given tolerance $5^\circ$ as the judgment. When the FH interval is relatively large, the tracking process of PLL is not a simple linear response but a transition from long-time nonlinear response to linear response which makes the overall lock time prolonged.

Based on the above analysis, a MIFP FH method is proposed as shown in Fig. 5. The large FH-distance is reasonably divided into multiple small interval to hop sequentially, $f_0, f_1$ to $f_{n-1}, f_n$ represent the initial frequency, inserted frequency, and the desired-frequency. The inserted frequency are determined by simulation, which ensures that the tracking process is linear underdamped response after inserting frequency; then the PLL is phase-locked at the desired frequency. $\Delta t$ (equal to $t_n - t_{n-2}$ in Fig. 5) is tracking time of the inserted frequency, which is determined by the latching time of the N register related to the next frequency. Meanwhile, the latching time is constantly adjusted to ensure the smooth completion of the linear under-damping process.

The above method is verified by ADIsimPLL software as well which can only simulate the transient process with the initial frequency and desired-frequency. Fig. 6 shows the FH time with two frequency points inserted while keeping the loop bandwidth, initial frequency and desired-frequency unchanged. The inserted frequency points are 2.3 GHz and 2.6 GHz. The total lock time which consist of tracking time of two inserted frequency and phase-locked time of desired frequency, are about 19.07 us (1.28 us+1.50 us+16.29 us). Due to the great improvement of tracking time, simulation results show that the total lock time is 5 us shorter than that the direct FH mode. Meanwhile, the last phased-locked process with the MIFP method is shorter which also contributes to time reduction due to the desired-frequency is steered from the nearby frequency [33].

4. Experimental verification of MIFP method

A broadband FH LOs on a certain type of radar is designed for verification of the above simulation results.

**PLL index:**

Reference input: 100 MHz;
Output frequency: 2.0G~2.8 GHz;
PN: $-105 \text{ dBc/Hz} @ 1 \text{ kHz}$; $-125 \text{ dBc/Hz} @ 300 \text{ kHz}$;
Lock Time: $\leq 35$ us;
Loop bandwidth: $\leq 200$ kHz;
Spurious: $\leq -70 \text{ dBc}$;
Considering the UWB characteristic of the LOs, a localized PLL with the external VCO and the active loop are selected. The operation frequency range of VCO is 2.0–3.0 GHz, and the max RF input frequency of PLL is 6 GHz, which can meet the requirements of LOs for output frequency. The design principle block diagram of LOs is shown in Fig. 7.

The setting of $\Delta t$ is important for shortening the FH time. If $\Delta t$ is prolonged, operating frequency of the PLL would exceed the desired inserted-frequency then the phase stabilization process would be implemented which will lead to extension of the total lock time. On the contrary, if $\Delta t$ is shortened, the PLL cannot approach the inserted frequency which would cause over damping or critical damping state in the latter tracking process. Therefore, the PLL can realize under-damped response at both inserted frequency points with appropriate $\Delta t$. The tracking time at the current frequency is equal to the latching time related to the next frequency point, that is, $\Delta t = T$ (latching time of N-register).

Two latches (48 bytes) related to the frequency need to be latched. Referring to the simulation results of the shortest tracking time (1.28 us) as shown in Fig. 6.(a), the clock rate ‘$r$’ of FPGA configuring PLL registers must exceed 37 MHz (1.28 us > 48*/$r$).

The Spartan-6 series FPGA of Xilinx company applied in this design adopts 50 MHz crystal oscillator as reference, and frequency doubling of reference is supported through internal integration PLL, which can meet the high-speed data transmission.

The measurement platform is shown in Fig. 8. Signal source analyzer (E5052B Keysight Technologies) is adopted for lock time test which is set to external trigger and rising edge capture mode. The LE pin of the PLL is connected to the external trigger input port of the instrument, and the VCO output port connected to the instrument input. The reference input port of the PLL is connected to the output of the signal-generator (SMW200A ROHDE&SCHWARZ).

The initial and desired-frequency of the test are 2.0 GHz and 2.8 GHz respectively. The LE pin of the PLL is connected to the external trigger input port of the instrument, and the VCO output port connected to the instrument input. The reference input port of the PLL is connected to the output of the signal-generator.

As shown in Fig. 9, the lock time of the last phase stabilization within 5° in the direct FH mode is about 38 us with the same lock-in criteria as simulation.

The PLL with MIFP FH method is tested and verified below. 2.3 GHz and 2.6 GHz are also set as the inserted frequency points during the measurement. Referring to the difference between Fig. 4 and Fig. 9, the lock time of test is much longer than the simulation, so the tracking time is also much longer than the simulation results in Fig. 5. Delay of software needs to be introduced before FPGA latching the N register of the next frequency.

Since the locking process cannot be interrupted to test the tracking time of inserted frequency, the only effective way to shorten FH time is to constantly adjust the tracking time which is equal to $\Delta t$ between two inserted frequency points and then to record the final minimum lock time. After much efforts of delay adjustment, the total FH time is the shortest, 30 us, when the first tracking time is 2.65 us and the second traction time is 3.1 us as shown in Fig. 10. It is shortened by 8us compared with direct FH in Fig. 9.

The above measured results of MIFP method are just under the condition of 0.8 GHz FH interval (2.0–2.8 GHz). What’s more, this method can also be applied to other LOs with different FH points and interval.
The shortening of PLL FH time is of great significance to communication and radar systems. In this paper, a MIFP technique has been applied to the communication systems and radar systems. In this paper, a MIFP method is proposed to shorten the FH time under the condition of large FH interval. The feasibility of this method is verified by theoretical analysis and simulation, and the technique has been applied to the communication systems and radar. Moreover, it can be applied to various UWB LOs circuits.

5. Conclusions

The shortening of PLL FH time is of great significance to communication and radar systems. In this paper, a MIFP method is proposed to shorten the FH time under the condition of large FH interval. The feasibility of this method is verified by theoretical analysis and simulation, and the technique has been applied to the communication systems and radar. Moreover, it can be applied to various UWB LOs circuits.

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