Comparison between CMOS full adder and PTL full adder

Amitha.M¹, Deepa²

¹Master of Technology in VLSI Design and Embedded Systems, Dept. of Electronics and Instrumentation Engineering, Siddaganga Institute of Technology, Tumakuru.
²Assistant Professor, Dept. of Electronics and Instrumentation Engineering, Siddaganga Institute of Technology, Tumakuru

Email.id: rmdeepa@yahoo.com

Abstract: In electronic industry the level of integration is an important aspect as makes the electronic device simpler and more reliable. The device density increases with the better level of integration. Power dissipation, area occupied and delay are some of the important factors that need to be considered. These parameters play a vital role in manufacturing portable electronic gadgets. Designing of full adder using conventional CMOS design and PTL has been shown in this paper. A comparison is made between the two designs with respect to power dissipation, delay and area (number of transistors). Mentor Graphics Tool is used in design and simulation of the full adder. The PTL full adder has a smaller number of transistors and lower power dissipation compared to CMOS full adder. With all the comparison made it will be concluded that the PTL full adder performance is better than the CMOS full adder.

Key words: Power dissipation, delay, area, PTL, mentor graphics, full adder.

1. Introduction

Full adder is a type of adder that adds three inputs and gives two outputs. Out of three, two will be the present inputs and the third input will be the carry from the previous stage. Full adder is shown in Fig 1, where ‘A’ and ‘B’ are the actual inputs, ‘C’ is the carry from the previous operation. SUM and CARRY OUT are the two outputs. The Truth Table shown in Table 1 gives an idea about outputs for various input combinations. For any arithmetic operations like multiplication, subtraction, division, DSP designs adders are the fundamental blocks. Many binary adders are formed using full adders. Hence, if any enhancements have to be made to improve the performance it can be made at the root i.e., adders. This in turn helps in bettering the performance of the electronics circuits which follow adder. The low power VLSI design is of great importance due to portable electronic products. Lowering the threshold voltage and the input voltages are some of the effective ways to reduce the power consumption. The adders are designed in various techniques and they all are concentrated on reducing the area, power dissipation and delay [1]. The area and complexity can be reduced by
decreasing the transistor count. The speed depends on transistor size, delay in the critical path and parasitic capacitance [4]. Although all the designs perform the similar function, each design has its own advantages and disadvantages. With a combination of one or more logic styles better result can be got.

Fig 1: Block diagram of full adder

| A | B | C | SUM | CARRY OUT |
|---|---|---|-----|-----------|
| 0 | 0 | 0 | 0   | 0         |
| 0 | 0 | 1 | 1   | 0         |
| 0 | 1 | 0 | 1   | 0         |
| 0 | 1 | 1 | 0   | 1         |
| 1 | 0 | 0 | 1   | 0         |
| 1 | 0 | 1 | 0   | 1         |
| 1 | 1 | 0 | 0   | 1         |
| 1 | 1 | 1 | 1   | 1         |

SUM = A^B^C = [A+B+C].[-CARRY OUT]+ABC --- (1) CARRY OUT= AB+BC+CA = AB+C [A+B] --- (2)

1.1. Mentor Graphics

Mentor graphics is a well-known technology provider in Electronics Design and Automation. This has built software and hardware solutions that help companies to make their quality electronic products at a higher production rate and also at lower cost. Mentor Graphics is used mainly to develop electronic devices that are fully customized [3]. One small flaw in the chip can ruin the entire system hence it is important to eliminate them at the initial stages. Mentor Graphics helps one to prepare the details related to design such as initial schematics, layout and physical design of the device; also verification of the circuit can be done before it is fabricated. At each stage, the design can be verified by simulating it and check whether the circuit is functioning properly.

Here is the 1bit full adder designed using both Complementary Metal Oxide Semiconductor (CMOS) design and also using Pass Transistor Logic (PTL). Both the designs are drawn using Mentor Graphics. The paper is organized in sections. The section 2 is about Conventional CMOS design. The section 3 is about the PTL full adder. In section 4 a comparison is made between both the designs.

2. Conventional CMOS design

Conventional CMOS design is based on normal complementary metal oxide semiconductor design with P-MOS acting as pull-up and N-MOS as pull-down transistor. This design requires 28 transistors, thus the silicon area and the complexity is more for larger designs. These are more immune to noise. The design and the simulation result for the 28T full adder is as shown in Fig 2. The schematics are drawn as per the equation (1) and (2). It is easy to analyse the conventional CMOS full adder by using the principle of mirror. In Fig 2(a) it can be seen that the NMOS network is identical to that of the PMOS network. This fully symmetric design reduces the complexity of the
layout design as it makes layout design, placement and routing easier. The main disadvantage of this configuration is that it has slower speed as it has to drive heavier load. Requirement of high input capacitance and buffer are also some of the disadvantages. High robustness against voltage scaling and transistor sizing are the advantages of CMOS full adder design.

Fig 2(a): Schematic of conventional CMOS full adder

Fig 2(b): Block diagram of Conventional CMOS Full adder
Fig 2(c): Waveforms showing inputs to full adder, sum and carry

Delay for sum=(τPHL+τPLH)/2 = (-3.289+138.59)ps/2 = 70.93psec
Delay for carry=(τPHL+τPLH)/2 = (-5.291+101.54)ps/2 = 53.4155psec
Power desipation=6.372 n watts

CMOS full adder has been designed, test schematic is drawn, and delay of 70.93psec for sum and 53.4155psec for carry and power dissipation of 6.372n watts has been obtained.

3. PTL Full Adder

The power dissipation is one of the main factors in VLSI circuits. The 1 bit CMOS 2T full adder was not efficient to build larger circuits with high performance as the complexity would increase. Hence, Pass Transistor Logic (PTL) adders were designed. This Logic helps us eliminate redundant transistors. The reduction in the transistor count in turn reduces the power dissipation of a device and at the same time maintains a proper throughput [2]. In 1 bit and 8 bit full adder, including of NMOS based PTL increases the performance as there will be more transistors in less area and hence proves itself to be an effective power handling logic.

Pass transistor Logic comes along with the advantages such as [5] high speed, low power dissipation and low interconnection effect. High speed results in lesser delay and the reason for this is small node capacitances. Lower power dissipation is due to less number of transistors. During the logic low the charge flowing through the transistor is drained. These charges are reused and given as input to control the transistor gates. This shows that there is no direct way to ground. Hence, the power dissipation is almost zero. The small area of circuit results in low interconnection effect. There are some disadvantages of PTL design techniques such as 1) threshold drop across the pass transistor 2) at the regenerative inverter the input voltage value is not Vdd. There will be multiple drops at the output as the NMOS can pass ‘0’ signal correctly but can never pass ‘1’ accurately. The threshold loss is always encountered. The below Fig 3 shows schematic of PTL full adder, its block diagram and waveforms related to input and output.
Fig 3(a): Schematic of PTL based Full adder

Fig 3(b): Block diagram of PTL full adder showing inputs and outputs
Fig 3(c): Waveforms of inputs, sum and carry

Delay = 100.0148ns
Power dissipation: 1.381nW
Advantage: Complexity reduces due to less number of transistors and delay reduces.
Disadvantage: NO full swing in the output voltages and leakage power is high.

4. Result and Conclusion
Fig 4: Comparison among PTL FA and CMOS FA. (a) No. of Transistors is the factor for comparison. (b) Delay is taken as the factor for comparison. (c) Power Dissipation is taken as the factor for comparison.

Table 2: Comparison between CMOS FA and PTL FA

| Parameter         | Conventional CMOS FA | PTL FA  |
|-------------------|-----------------------|---------|
| No. of transistors| 28                    | 10      |
| Delay             | 0.0793 ns             | 100.11 ns |
| Power Dissipation | 6.372nW               | 1.381nW |

Fig 4 has different graphs drawn for comparison between CMOS FA and PTL FA. Table 2 summarizes the practical values got by running the simulation of both the adders. By the above observations it can be concluded that the PTL full adder needs less area, less delay and also less power dissipation. Whereas the CMOS full adder requires many transistors hence occupies more area. More delay is encountered and also more power dissipation. Hence PTL full adder is far more advantageous than CMOS full adder.

References
[1] Mariano Aguirre-Hernandez, Monico Linares-Aranda, “CMOS Full-Adders for Energy Efficient Arithmetic Applications”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011
[2] Hamed Naseri; Somayeh Timarchi, “Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018
[3] T.K. Schneider, A.J. Schwab; J.H. Aylor, “A full custom VLSI design methodology using Mentor Graphics design software in an educational environs”, Sixth Annual IEEE International ASIC Conference and Exhibit 2018
[4] Mehedi Hasan, Md. Jobayer Hossein, Mainul Hossain; Hasan U. Zaman, Sharnali Islam, “Design of a Scalable Low-Power 1-Bit Hybrid Full Adder for Fast Computation”, IEEE Transactions on Circuits and Systems II: Express Briefs, 2020
[5] Jyoti Kandpal; Abhishek Tomar, Mayur Agarwal; K. K. Sharma, “High-Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR–XNOR Cell”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020