Implementing and Breaking Load-Link / Store-Conditional on an ARM-Based System

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Abstract—Manufacturers of modern electronic devices are constantly attempting to implement additional features into ever-increasingly complex and performance demanding systems. This race has been historically driven by improvements in the processor’s clock speed, but as power consumption and real estate concerns in the embedded space pose an growing challenge, multithreading approaches have become more prevalent and relied upon. Synchronization is essential to multithreading systems, as it ensures that threads do not interfere with each others’ operations and produce reliable and consistent outputs whilst maximizing performance and efficiency. One of the primary mechanisms guaranteeing synchronization in RISC architectures is the load-link/store conditional routine, which implements an atomic operation that allows a thread to obtain a lock. In this study, we implement, test, and manipulate an LL/SC routine in a multithreading environment using GDB. After examining the routine mechanics, we propose a concise implementation in ARMv7l, as well as demonstrate the importance of register integrity and vulnerabilities that occur when integrity is violated under a limited threat model. This work sheds light on LL/SC operations and related lock routines used for multithreading.

Index Terms—load-link/store-conditional, multithreading, synchronization, memory protection, security, register access, attacks, hardware

I. INTRODUCTION

Modern day computing systems rely heavily on multithreading to increase performance and resource utilization through improved responsiveness, resource sharing, economy and scalability. However, running multiple threads concurrently can become a complex challenge, with individual threads being capable of interfering with each other stochastically when sharing hardware resources. For instance, when multiple threads try to access a shared variable concurrently, the read and write operations can overlap in execution due to race conditions which can lead to unpredictable outputs depending on the order of access.

Thread interference errors can be corrected by ensuring synchronization, which is established by satisfying two conditions:

1) Only one thread can access a shared variable at a time, guaranteeing that the variable is atomic and other threads do not interfere with the operation.
2) Whenever a thread accesses a shared variable, it ensures that the changes are visible to other subsequent threads by establishing a happens-before relationship with ensuing accesses.

One method of addressing synchronization is load-linked/store-conditional (LL/SC), which refers to a pair of instructions that protect multithreaded accesses to memory by implementing a lock-free atomic read-modify-write (RMW) operation. The first instruction, LL or load-link, implements the read part of the atomic operation in two stages. First, LL reads from a memory location and puts the read value in a register. Second, the LL instruction appropriately updates the register, based on the address from which the value was loaded. The second instruction, SC or store-conditional, implements the write part of the atomic operation. The SC instruction attempts to store a value to an address in memory. If this store is permitted by the system (which is likely in the case that another thread hasn’t stored to the address and already obtained the lock), then the store will succeed (a 0 will be returned in the destination register in ARM). Otherwise, the store will fail (a 1 will be returned in the destination register in ARM). As such, the store is known as a conditional store, which is not guaranteed to succeed. The LL and SC operations work together with exclusive monitors in ARM architectures to provide atomic memory updates.

It is worth mentioning that LL/SC instructions are only compatible with RISC architectures such as ARM or MIPS. CISC architectures, like x86, implement a similar instruction called compare-and-swap (CAS), which has a slightly different functionality. Though implementation methods for LL/SC vary, some rely upon CAS. Specific syntax for LL/SC instructions varies across platforms.

Given the prevalence of LL/SC instructions, their functionality and potential vulnerabilities are of significant interest. This study aimed to illuminate LL/SC by implementing a lock scheme in ARMv7l using a Raspberry Pi through the supported LDREX and STREX instructions. We also subsequently explored the operation of these operations when executed by several threads and attempted to introduce unpredictable malicious behavior.

This paper overall makes the following contributions:

• Concise implementation of LL/SC in a multithreading environment on an ARM-based system

This work sheds light on LL/SC operations and related lock routines used for multithreading.
• Demonstration of the importance of register integrity during the LL/SC routine by highlighting the the impact an attacker can have by tampering with bits in key registers.
• Several implementation suggestions that may help protect register integrity

II. Key Idea

Synchronization is essential to various real-world use cases. Consider the example of a bank account’s details stored in memory, in which an accountBalance variable stores a numeric value for a given account (Fig. 1). Naturally, a synchronization failure could cause an error (or even a security breach), given that calling increaseBalance() as shown in Fig. 1 without appropriately-placed thread barriers may generate unexpected behavior which could be exploited by a malicious user. If two threads (access points) attempt to increment the account balance at the same time, they may each fetch the initial value and add to it, instead of waiting for the other thread to finish its execution and then adding to the resulting updated value. This means that the thread that concludes last will have effectively called increaseBalance(), but with no noticeable effect. Similar programs are commonly used to demonstrate the danger of sharing a global variable between threads.

```c
1 double accountBalance = 0;
2 void *increaseBalance(){
3   int i;
4   for (i = 0; i < 10000; i++){
5     accountBalance += 1;
6   }
7 }
```

Fig. 1. Simple code for increasing an account balance through incrementation

This idea of unexpected multithreading behavior serves as a source of motivation for a mechanism ensuring that only one thread is accessing a shared variable at a time. It is not difficult to imagine circumstances in which multiple threads executing privileged code in an uncoordinated manner could lead to catastrophe by modifying a critical variable in an unexpected way. It is also easy to conceive of why privileged code should not be accessed at the same time. Since tangible issues could arise from synchronization bugs, further research advancing knowledge on LL/SC instructions and lock sequences could be influential.

III. Methodology

A. Overview

We aimed to create a program capable of implementing and testing LL/SC in a multithread environment. This was achieved using ARMv7l on a Raspberry Pi through a C harness file with inline ASM code. In order to ensure synchronization of variables between different threads, we utilized GDB to step across multiple threads and ensure that the routine was working as expected. Finally, we attempted to break the LL/SC implementation by manipulating register values at runtime, and analyzing the results and their implications on the routine.

B. LL/SC Implementation

For the base LL/SC implementation, we relied upon supported inline ASM commands to create the lock routine. More specifically, our locking scheme utilized the LDREX and STREX instructions in combination with the BNE command to jump to the start of the program if a compare (CMP) operation failed. We kept track of the shared lock variable in the C harness code through lockVar.

```asm
1 lock:
2   retry:
3     LDR R10, =lockVar
4     LDREX R8, [R10]
5     CMP R8, #0
6     BNE retry
7     MOV R9, #1
8     STREX R2, R9, [R10]
9     CMP R2, #0
10    BNE retry
11   critical_section:
12     // critical shared variable
13     // changes could occur here
14   unlock:
15     MOV R5, #0
16     LDR R10, =lockVar
17     STR R5, [R10]
```

Fig. 2. Lock routine utilizing LDREX, STREX, and other built in operations for LL/SC in inline ASM

Our ASM code was modeled after prevailing LL/SC schemes in computer architecture. In the retry routine, a thread attempts to write to a lock. If the value loaded in through the LDREX instruction is 0 (i.e., no thread currently has the lock at the time the instruction was executed), the thread then attempts to write a value of 1 to the shared lock variable in the STREX instruction. If successful, the thread will then move on to the critical section.

After the critical section, the thread will release its hold on the lock by writing a value of 0 to lockVar, at which points other threads spinning in the retry routine can gain hold of the lock. The CMP BNE pair recursively calls retry, ensuring that a thread will repeatedly try to gain the lock if it is already taken. So long as there is at least one thread waiting for the lock, the thread giving up the lock will almost immediately yield it to another thread. LDREX and STREX rely on exclusive monitors, as specified by the ARM architecture.

C. Multithreading

Our ASM LL/SC routine was implemented with inline ASM in C, which allowed us to build out a more robust testing platform. The ASM code was wrapped in a void loadLinkRoutine function, which was then called by threads from a main function within the C program. The
main function also handled creating threads using the pthread library, allowing us to index threads and monitor access patterns, which was critical to keep track of “winning” and “losing” threads. A simple loop handled thread generation, so that it was possible to vary the number of threads throughout experimentation and observe resulting trends in race conditions and thread execution order.

```c
#include <string.h>

int main() {
    int i;
    pthread_t tid;
    for (i = 0; i < 10; i++) {
        pthread_create(&tid, NULL, loadLinkRoutine, NULL);
    }
    pthread_exit(NULL);
    return 0;
}
```

![Fig. 3. C code calling the lock routine and handling multithreading](image)

### D. Testing Challenges

The combination of C code and inline ASM proved to be a challenge when attempting to test the LL/SC routine. In particular it was difficult to directly observe outputs because even if the ASM routines are split up into several C functions which are chained together (allowing inter-routine printf calls to be execution), it is not possible to guarantee the order of the printf calls, as the threads are racing one another.

An alternative method of debugging would be to insert the printf statements directly into the ASM code. For instance, it is possible to take advantage of extended ASM to insert print statements as shown in Fig. 4.

```asm
MOV R0, #2
	 // stderr
MOV R1, [%toPrint]\n\t // message
MOV R2, [%length]\n\t // length
MOV R7, #4\n\t
SWI 0
:
[toPrint] "r" (str),
[length] "r" (len)
}
return 0;
```

![Fig. 4. Direct print statements from ASM](image)

Unfortunately, this approach was not effective given that if multiple threads cause a software interrupt at the same time, the output of one thread will overwrite the other. In certain scenarios, before the full string output of one thread can be printed out, another thread may make a software interrupt and prevent the former call from being fully executed. Without artificially guaranteeing the order of threads using barriers (and defeating the purpose of having multiple threads simultaneously accessing the same shared variable) a consistent output cannot be assured.

More advanced capabilities are required for lower level access, necessitating use of GDB to test the functionality of the routine in a more rigorous manner. This solution met the demands of our research objective while allowing us to retain an ASM and C code framework.

### E. GNU Debugger (GDB)

GNU Debugger, or GDB, is a portable debugger that is typically run from Unix-like systems. It grants access to registers and memory, and allows the programmer to insert breakpoints, pass commands at runtime, and inspect the functionality of code at a low level. GDB hence allowed us to probe and test the routine more precisely than print statements or other discussed modifications to the code. In order to understand and explore the behaviour of multiple threads racing against each other, we set a breakpoint at the start of the loadLinkRoutine function so that each thread will stop execution here and allow us to step through the following instructions one-by-one.

GDB cannot single-step all threads in lockstep [2], making analyzing the behaviour of multiple threads racing against each other difficult because, by default, other threads can execute more than one statement whilst the current thread only completes a single step. The Raspian OS, however, does support locking the OS scheduler so that a single thread can run at a time. This behavior can be achieved through GDB by executing the command:

```
set scheduler-locking step
```

This scheduler locking mechanism allowed us to manually stop each thread and have direct access to threads attempting to modify the same variable at once.

### F. Experimentation Model

Early versions of our LL/SC implementation and attack model did not produce the desired behavior, driving us to improve upon the lock routine and develop new methods of thread exploitation. We debugged and validated the functionality of LL/SC using GDB as described to ensure that the attack was independent of our implementation.

Prior to recording results and engineering our attack, we also dedicated a significant research effort towards LL/SC lock design. This experimentation involved introducing additional branch conditions (with BNE, LDREX without STREX (and vice versa), and misordered register accesses. The goal of this iterated testing was to fully determine LL/SC mechanics outside of traditional use before moving on to results.

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1. ![Fig. 5. Unconstrained behavior with incorrect threading implementation](image)

More advanced capabilities are required for lower level access, necessitating use of GDB to test the functionality of the routine in a more rigorous manner. This solution met the demands of our research objective while allowing us to retain an ASM and C code framework.

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The majority of errors we encountered with this experimentation were trivial and did not reveal any vulnerabilities related to LL/SC. Given the syntax and register usage of LDREX and STREX, there are limitations to the manner in which these instructions can viably be used. In some cases we reached segmentation faults and bus errors when LL/SC was improperly implemented. Still, this experimentation helped to narrow the scope of our attack and verify ways in which LL/SC was not prone to vulnerability.

IV. RESULTS

A. Lock Sequence

In order to ensure the functionality of our LL/SC routine, we followed a three part process:

1) Step the winner thread to the point where it had obtained the lock on the critical variable.
2) Step the remaining threads (the losers) to the LDREX instruction, and monitor their behavior.
3) Release the winner’s hold on the lock. Repeat.

This process verified that our LL/SC code was working properly. The winning thread maintained the lock when expected and executed the critical_section, while the losing threads looped in attempts to gain the lock. This was repeated for subsequent threads as described above.

While validating our lock sequence, we also used GDB to verify thread “locations” relative to the lock routine and register values as threads executed. This provided a low level view into memory without relying on the ASM or C code to examine program behavior.

B. Observations

After the LL/SC implementation was shown to be a functional lock routine, and prior to attempting to alter the lock or break LL/SC, we first conducted preliminary testing to determine areas of vulnerability for exploit. This allowed us to fine tune our attack on LL/SC based on thread execution.

One interesting discovery we made during this phase was that the instructions in between LDREX and STREX which proved to have important consequences when examining security vulnerabilities.

C. Breaking LL/SC

In order to attempt to break our implementation of LL/SC, and hence showcase the importance of LL/SC in synchronizing threads, we created numerous threads to attempt to access a memory address at the same time. More specifically, we created 3 threads, each of which added 5 to an initial accountBalance of 100 (representing a bank account).

To ensure that the resulting accountBalance could be correctly printed when the program terminated, we utilized pthread_barrier.

Given that each of the 3 threads added 5 to an initial balance of 100, the expected output of the program was 115. However, by modifying register values during runtime, we were able to break the locking mechanism and cause two threads to access the accountBalance variable at the same time, inducing the output to vary from expectation.

As we found in our observation period, it was not feasible to modify instructions that take place between the LDREX and STREX, due to the atomicity of this operation pair. Instead, we needed to modify the LL/SC routine slightly so that the CMP instruction compares two registers, as opposed to one register (the result of the LDREX/STREX) and a constant. This step would crucially allow us to modify the second register during runtime through the modified routine found in Fig. 8.

lock:
  LDR R10, =lockVar
  MOV R7, #0
  LDREX R8, [R10]
  CMP R8, R7 // updated comparison
  BNE retry
  MOV R9, #1
  STREX R2, R9, [R10]
  CMP R2, R7 // updated comparison
  BNE retry

critical_section:
  // critical shared variable changes would occur here

unlock:
  MOV R5, #0
  LDR R10, =lockVar
  STR R5, [R10]

Fig. 7. CMP statement that could not be reached by GDB due to atomic LDREX and STREX instructions

With this updated routine, we were able to successfully modify the value in R7 at runtime and produce an outcome that deviated from the expected 115 through pathological register manipulation and thread stepping.

lock:
  LDR R10, =lockVar
  LDREX R8, [R10]

retry:
  LDR R10, =lockVar
  MOV R7, #0
  LDREX R8, [R10]
  CMP R8, R7 // updated comparison
  BNE retry
  MOV R9, #1
  STREX R2, R9, [R10]
  CMP R2, R7 // updated comparison
  BNE retry

critical_section:
  // critical shared variable changes would occur here

unlock:
  MOV R5, #0
  LDR R10, =lockVar
  STR R5, [R10]

Fig. 8. Modified lock routine
To begin, we ran GDB using the described methodology, taking advantage of the step scheduler-locking mechanism to step through threads in place. Our three threads each started at the beginning of the loadLinkRoutine function. Utilizing GDB, Thread 1 first obtained the lock and added the value of five to accountBalance. Next, before Thread 1 had stored the value of 0 back to the lock (i.e., freed the lock), we switched to Thread 2. As expected, this thread was continually cycling between the three instructions detailed in Fig. 9.

![Fig. 9. Cycled instructions for Thread 2](image)

We then used GDB to change the value in the register R7 immediately after the MOV instruction. Since we could not modify R7 at any point in between the LDREX and STREX, we modified it before the LDREX instruction executed.

The instruction set $R7 += 1 was executed in GDB so that the comparison between R8 and R7 (which should return 0 under normal circumstances since Thread 1 has the lock and therefore the result of LDREX, stored in R8, will be 1) returned 1. This manipulation caused Thread 2 to make it past the STREX instruction. One instruction, however, still laid in the way: the CMP after STREX. This instruction compared R2 and R7. As a result, we needed to manipulate R7 once more for the line CMP R2, R7. This time, it was necessary to set R7 to 0, which would allow us the thread to move forward to the next instruction instead of continually spinning for the lock. This modification permitted Thread 2 to make it past the second CMP instruction, on the assumption that it now had the lock. Thread 1 also thought it had the lock.

It is deeply problematic that Thread 1 and Thread 2 simultaneously believed they each had the lock, as this allowed Thread 2 to read in the value of the accountBalance prior to update by Thread 1. Thread 2 read in an accountBalance value of 100, when it really should have read in a value of 105 (after it was updated by Thread 1). This meant that the base value of 100 was updated, not 105. After causing this crucial break in our LL/SC subroutine, we resumed normal operation by turning off the step mechanism via:

```
set scheduler-locking off.
```

After all threads finished running, we received the output shown in Fig. 10.

![Fig. 10. Thread output at conclusion of runtime](image)

This output of 110 instead of the expected 115 illustrated that it was possible to break our LL/SC routine and cause an unexpected result through runtime register manipulation.

### D. Implementation Suggestions

Based on our results, we suggest the following two measures to increase security in LL/SC implementations:

1. Ensure that the outputs of the LL and SC instructions are compared to constants, not registers.
2. Have a branch conditional both after the LL instruction and after the SC instruction.

The first recommendation is a direct result of the behavior observed through pathological register manipulation where we were able to modify the accountBalance variable in a manner different than what was presumably intended by the program(mer). The actual output of the LDREX and STREX instructions cannot be modified in between the LDREX and STREX instructions due to the atomic nature of LDREX and STREX working in conjunction. So, for instance, the code in Fig. 11 is safe because the R8 register cannot be modified, and neither can the constant value.

![Fig. 11. Thread output at conclusion of runtime](image)

The code in Fig. 12, however, is potentially unsafe because R7 can be modified before the LLSC routine occurs, as we demonstrated.

![Fig. 12. Thread output at conclusion of runtime](image)

The second recommendation relates to the number of modifications that must be made to corrupt the LLSC routine. Some implementations do not include a branch based on the result of LDREX, such as the implementation depicted in Figure 13. Thus, the only instruction standing in the way of LLSC corruption is the sole CMP instruction after STREX, as compared to our initial implementation with had a CMP instruction both after LDREX and STREX.

### V. RELATED WORK

#### A. Implementation and Optimization

A number of prior studies have explored the mechanics of LL/SC instructions, compared LL/SC to alternatives such as CAS, and explored the implications of LL/SC support across platforms. Notably, Alpha, PowerPC, MIPS, and ARM all provide LL/SC instructions, while x86 leverages CAS [3]. This means that depending on the hardware and CPU, LL/SC is sometimes infeasible. In our study, for instance, we initially approached x86 before opting for ARM. LL/SC differs from CAS in that it is more rigorous: an successful LL/SC...
lock:
  retry:  
    LDR R10, =lockVar
    LDREX R8, [R10]
    MOV R9, #1
    STREX R2, R9, [R10]
    CMP R2, #0
    BNE retry

critical_section:
  // critical shared variable
  // changes could occur here

unlock:
  MOV R5, #0
  LDR R10, =lockVar
  STR R5, [R10]

Fig. 13. Lock routine without branch depending on output of LDREX

programming pattern assures that the store-conditional will fail if any updates have occurred to the memory in question, while CAS solely verifies that the value is maintained. In practice, LL/SC guest instructions are often produced from host atomic CAS instructions, as is necessary in the case of x86 host systems [1], [4]. Though efficient, this has been shown to induce significant issues, which requires a new LL/SC emulation scheme [1]. Research has also investigated improving upon the implementation of CAS [5].

In the context of this work, our exploration of LL/SC routines and attacks helps to emphasize areas for future research. In implementing and optimizing LL/SC, it is critical that engineers bear security in mind, as synchronization could fail without the proper lock routine requirements. Improving upon existing LL/SC schemes must not sacrifice security for performance. Additionally, it is notable that lock register integrity remains incredibly important in terms of ensuring functional LL/SC instructions. Memory constraints (and which/how many registers are used in LL/SC implementations) must be prioritized.

B. LL/SC Usage

In addition to research investigating LL/SC directly, a large effort has been devoted to examining LL/SC in the context of related computing research. Given the pertinence of LL/SC operations in RMWs and the existence of supported open source standards (e.g. RISC-V), LL/SC is widely useful on RISC machines [6]. For instance, LL/SC operations are pivotal in generating atomic instructions in RISC machines for emulating multithreaded applications on multicore systems [7]. Instruction set extensions introduced in research sometimes share properties with LL/SC [5], meaning that the pattern of memory access is often similar. In such circumstances, LL/SC is conceptually linked as a blueprint for instruction dependency and memory maintenance. Novel primitive operations that are generalizations of the LDREX and STREX instructions have also been proposed for specific uses such as non-blocking data structures, further demonstrating the deployment of LL/SC-like instruction sequences [9]. It is possible that our work applies to LL/SC-like instruction routines, though this would likely depend on the mechanics of alternative operation pairs. In any case, our work is of interest to software and hardware researchers in fields wherein LL/SC is common, even if the immediate topic of interest is not lock routines.

VI. CONCLUSION

This paper examined a concise implementation of LL/SC on ARMv7l, demonstrated the importance of register integrity in a multithreading environment, and highlighted a few important security considerations to take into account when implementing LL/SC.

We built a C program to test the LL/SC routine under multithreading conditions, supervising its functioning using GDB and stepping through the instructions line by line. Based on our experimentation and results, we concluded that LL/SC can be exploited by an attacker with access to key individual registers, breaking synchronization and opening the door for vulnerabilities. Furthermore, we think that some of the assumptions of the threat model can be bypassed by combining our results with previously developed attacks. For instance, attacks like Row Hammer [10] are capable of flipping bits in registers, allowing for an attacker to modify the key register value that allows our exploit to succeed. Cloud computing companies may place increasing emphasis on the integrity of on-chip registers.

This finding demonstrates a broader principle for lock routines: a lock is only as strong as the registers storing essential values. LL/SC, for instance, relies on several aforementioned registers called during the lock routine. By modifying these registers, a malicious attacker might be able to undermine synchronization.

We hope that our findings serve as a stepping stone for further research into exploiting the built-in assumptions that go into the atomicity of the LL/SC routine, and that it can be combined with other attacks to strengthen the capabilities and versatility of the load-link/store-conditional mechanism.

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[2] R. Stallman, R. Pesch, and S. Shebs, “Stopping and starting multithread programs,” Debugging with GDB - thread stops, Jun-2002. [Online]. Available: https://ftp.gnu.org/old-gnu/Manuals/gdb/html_node/gdb_39.html.
While this appendix is not integral to understanding of our research, additional code is provided to facilitate replicability and make our approach more clear. The code that follows was used throughout the process of implementation, experimentation, and attacking LL/SC.

**Code Repository**

Our full code can be found on Github, including our final code and significant portions of experimentation, at the following repository:

https://github.com/evantilley/hardware_sec

**Code Description**

A brief video explaining our code can be found at the following link:

https://www.youtube.com/watch?v=b1YQl8vFc4

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**main.c**

```c
#include <stdio.h>
#include <string.h>
#include <stdlib.h>
#include <pthread.h>

int lockVar = 0;

void *loadLinkRoutine(){
    long threadID = (long) pthread_self();

    __asm__ volatile(
        "lock:
        try_again:
        // "MOV R3, %[lock]\n\t" // move lock variable into R3
        "LDR R10, =lockVar\n\t"
        "LDREX R8, [R10]\n\t" // load value stored at that address
        "CMP R8, #0\n\t"
        "BNE try_again\n\t"
        "MOV R9, #1\n\t"
        "STREX R2, R9, [R10]\n\t"
        "CMP R2, #0\n\t"
        "BNE try_again\n\t"
        // if we make it here, got the lock
        "MOV R5, #0\n\t"
        "LDR R10, =lockVar\n\t"
        "STREX R2, R9, [R10]\n\t"
        "CMP R2, #0\n\t"
        "BNE try_again\n\t"
        // [lock must be an address]
        : [lock] "r" (lockVar)
    );
}
```

---

**Fig. 14.** Beginning of main.c, the full normal functioning LL/SC

```c
int main(){
    int i;
    pthread_t tid;
    for (i = 0; i < 10; i++){
        pthread_create(&tid, NULL, loadLinkRoutine, NULL);
    }
    pthread_exit(NULL);
    return 0;
}
```

---

**Fig. 15.** Main function of main.c, the full normal functioning LL/SC
hacker.c:

```c
#include <stdio.h>
#include <string.h>
#include <stdlib.h>
#include <pthread.h>

int lockVar = 0;
int accountBalance = 100;
pthread_barrier_t barrier;

void *loadLinkRoutine(){
    long threadID = (long) pthread_self();
    int realBal = accountBalance;
    __asm__ volatile(
        "lock:\n"
        "try_again:\n"
        // "MOV R3, %[lock]\n"
        "LDR R10, =lockVar\n"
        "MOV R7, #0\n"
        "LDREX R8, [R10]\n"
        "NOP \n"
        "CMP R8, R7\n"
        "BNE try_again\n"
        // if we make it here, got the lock
        "NOP \n"
        "CMP R8, R7\n"
        "BNE try_again\n"
        // if we make it here, got the lock
        "MOV R4, #5\n"
        "add R4, [%DEST]\n"
        "add [%DEST], #5\n"
        // okay, shared variable has been modified
        // now, replace the lock
        "MOV R5, #0\n"
        "LDR R10, =lockVar\n"
        "STR R5, [R10]\n"
        : [DEST] "=r" (accountBalance)
        : [balRes] "=r" (accountBalance)
        : "[DEST]"
    );
    pthread_barrier_wait(&barrier);
}
```

Fig. 16. Beginning of hacker.c, the modified code that theoretically outputs an expected value of 115, which we successfully tampered with using GDB on registers to reach an output of 110

```c
int main(){
    int i;
    pthread_t t[3];
    pthread_barrier_init(&barrier, NULL, 4);
    pthread_create(&t[0], NULL, loadLinkRoutine, NULL);
    pthread_create(&t[1], NULL, loadLinkRoutine, NULL);
    pthread_create(&t[2], NULL, loadLinkRoutine, NULL);
    pthread_barrier_wait(&barrier);
    fprintf(stderr, "after all threads have run, the value of account balance is %d\n", accountBalance);
    pthread_barrier_destroy(&barrier);
    return 0;
}
```

Fig. 17. Beginning of hacker.c, the modified code that theoretically outputs an expected value of 115, which we successfully tampered with using GDB on registers to reach an output of 110