Numerical simulation of Gate shape effect on Self-Heating in nano-MOSFET Transistors with high-k dielectric

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Abstract:

The aim of the present work is to investigate numerically the self-heating effect (SHE) in MOSFET transistors based on high-k material taking into account the deformation of the gate under the SHE. The SHE inside the MOSFET transistor is calculated using the electrothermal model based on heat transfer equation coupled with semiconductor equations. The electrothermal model have been solved in 2D-dimension using the finite element method. The high-k dielectric HfO₂ have been used as gate oxide. Several gate shapes have been used to analyze their impact on SHE. It is observed that the reduction of equivalent oxide thickness (EOT) reduces the SHE in the MOSFET transistor based in high-k dielectric material. the temperature peak increases quadratically with drain voltage for all MOSFET structures. A decrease in self-heating effect is achieved using the square gate shape.

Key words: Gate shape, MOSFET, Finite element method, Numerical simulation, Self-heating effect (SHE).

1. Introduction:

The intensive scaling of MOSFET transistors requires the thinning of the SiO₂ gate oxide which induces significant gate tunnels leading to power loss, increased power consumption, and generation of excess heat [1-6]. The increase of drain current caused by the low dissipation capacity of the dioxide SiO₂ [7] results an increase in self-heating effect (SHE) [8]. Therefore, using high-k oxides than SiO₂ oxide can mitigate this issue. In our previous work [9], we have proved that the
fact of using a high-k material able to reduce the device temperature and then to mitigate the SHE. Otherwise, we have investigated the effect of different high-k materials such as ZrO₂, HfO₂, La₂O₃, and Al₂O₃ on SHE in PiFETs Structures [10]. An important reduction of SHE was obtained using these dielectric materials. Some other studies have demonstrated a decrease of gate tunneling current is obtained by using the high-k dielectric materials [11]. According to Yu et al.[12], a good enhancement in transfer and output characteristics is achieved in their experimental study of strained SiGe quantum well p-MOSFETs with higher-k dielectric. Evenly, Sharma et al. [13] have shown that the use of high k materials in JL-CSG MOSFET device contributes to the improvement of the electrical and thermal characteristics.

Pravin et al. [14] have studied the dual metal gate MOSFET transistor with with different h-k dielectric materials. The impact of high-k gate dielectric on electrical characteristics have been simulated in Karbalaei et al.[15] work. They have investigated the electric performance with varying angle of coverage in a circular cross-section of gate-all-around field-effect transistor (GAAFET). The simulation results revealed that the electrical control of the gate over the channel increase as HfO₂ cover more the channel.

In order to study the self-heating effect (SHE) in nano electronic components, several electrothermal models have been developed and used [5, 6, 9, 16-18]. Belkhiria et al. [16] have analyzed the SHE in the gate-all-around-Field-Effect Transistor (GAAFET) using on the Cattaneo and Vernotte (CV) heat conduction model. Echouchene et al.[5, 6] have investigated the entropy generation in MOSFET transistor using the dual-phase-lag (DPL) model. They have shown that the entropy generation cannot be described using the classical form of the equilibrium entropy production and an oscillatory behavior in transient entropy generation obtained using DPL model in a real MOSFET transistor.

In the other hand, the effect of gate shape on electrical and self-heating characteristics in nanowire transistor have been investigate by [19, 20].

In this paper we propose to study the gate shape effect on self-heating in MOSFET transistors based on HfO₂ as high-k gate dielectric instead of SiO₂. Several gate shapes have been used in this analysis such as curve, square and triangular gate shape. The results have been compared to conventional MOSFET structure with plane gate shape. In this investigation, the continuity and
Poisson equations coupled with the heat transfer equation have been solved based on the finite element method.

2. Electrothermal model for MOSFET transistor

2.1. Device structure

Figure 1 presents the geometry of typical transistor studied in this work. The thin layer of SiO2 insulator is placed above the channel and another layer of high-k dielectric located between the dioxide and the gate.

The high-k gate oxides are physically thicker layers than SiO2. This will retain the same capacity but decreases the tunnel current. Therefore, it is appropriate to define the equivalent oxide thickness (EOT) which is defined the SiO2 layer thickness that would be required to achieve the same capacitance density as the high-k material:

\[ EOT = \left( \frac{3.9}{\varepsilon_{H,K}} \right) \times t_{H,K} \]  

where 3.9 is the dielectric constant of the oxide, \( \varepsilon_{H,K} \) is the dielectric constant for high-k material, and \( t_{H,K} \) is its thickness. The geometric parameters are illustrated in Table 1.

2.2. Electrothermal model

The electrothermal model used in this work is given by [10]:

\[
\begin{align*}
\nabla (\varepsilon \nabla V) + q(p - n) &= q(N_A - N_D) \\
\frac{\partial p}{\partial t} + \nabla (p \vec{v}_p) &= \nabla (D_p \nabla p) - R_p \\
\frac{\partial n}{\partial t} + \nabla (n \vec{v}_n) &= -\nabla (D_n \nabla n) - R_n \\
C \frac{\partial T_L}{\partial t} &= \nabla (\lambda \nabla T_L) + H
\end{align*}
\]

where \( V, n, p \) and \( T_L \) are respectively, the electrostatic potential, the electron concentration, the hole concentration and the lattice temperature, \( N_D \) and \( N_A \) are the ionized donor and acceptor impurity concentrations, respectively. \( D_{n,p} \) present the diffusion coefficients of electron and hole, respectively. \( \lambda \) is the thermal conductivity, \( C \) is the specific heat, \( \varepsilon \) is the local permittivity, \( q \), is the magnitude of the charge on an electron, \( R_n \) and \( R_p \) are the electron and hole recombination rates,
respectively. \( H = \vec{J} \cdot \vec{E} \) is the heat generation rate, where \( E \) is the built-in electric field, \( J \) is the electric current density in the active zone.

2.3. Numerical method

The numerical solution of the transport equation (Eq.2) has been done using a finite element method. The approximation of function \( \Phi = [V, p, n, T_L] \) can be expanded in terms of the shape function as:

\[
\Phi(x, y, t) = \sum_{i=1}^{N} \Phi_i(t) \phi_i(x, y)
\]

In order to proceed we introduce a complete finite set of shape functions \( \phi_i(x, y) \): \( j=1,2,...,N \). The integral form is obtained by multiplying (2) by \( \phi_j \) and integrating over the region \( \Omega \) occupied by the device. After applying the divergence theorem we find:

\[
\int_{\Omega} \left[ \nabla \phi_j (\nabla \nabla \phi) - \oint_{\partial \Omega} \phi_j (\nabla \phi) \hat{n} \right] = \beta K_{ij} + \gamma L_{ij} \phi_j
\]

After development, Eq. 4 can be written as:

\[
\sum_{l} \left[ \alpha M_{ij} \phi_l + (\beta K_{ij} + \gamma L_{ij}) \phi_l \right] + F_j = 0 \quad l \leq j \leq M
\]

where

\[
M_{ij} = \int_{\Omega} \phi_i \phi_j \partial \Omega, \quad L_{ij} = \int_{\Omega} \phi_i \nabla \phi_j \nabla \phi \partial \Omega,
\]

\[
K_{ij} = \int_{\Omega} \nabla \phi_i \nabla \phi_j \partial \Omega \quad \text{and} \quad F_j = \int_{\Omega} \delta \phi_j \partial \Omega
\]

and
After assembling the elementary matrices, we obtain the global matrix form:

\[
\alpha = \begin{pmatrix}
0 \\
1 \\
1 \\
C
\end{pmatrix}, \quad \beta = \begin{pmatrix}
0 \\
D_p \\
-1 \\
-D_n \\
\lambda
\end{pmatrix}, \quad \gamma = \begin{pmatrix}
0 \\
-R \\
-R \\
0
\end{pmatrix}, \quad \delta = \begin{pmatrix}
\frac{q/\epsilon(N_D-N_A)}{-H}
\end{pmatrix}
\]  

(7)

After assembling the elementary matrices, we obtain the global matrix form:

\[
[M] \alpha \Phi + (\beta[K] + \gamma[L]) \Phi + [F] = 0
\]

(8)

where \( \Phi \) is the vector of unknown nodal transportable quantity, \([M]\) is the damping matrix, \((\beta[K] + \gamma[L])\) is the stiffness matrix, and \(F\) is the external flux vector.

The discretization of the ordinary differential equation Eq.8 gives

\[
\Phi_{n+1} = \Phi_{n-1} - \frac{2 \Delta t}{\alpha M} ([\beta[K] + \gamma[L]) \Phi_n + [F])
\]

(9)

where \( n \) is the time index and \( \Delta t \) is time discretisation step.

To carry out the thermal analysis of the proposed structures of MOSFET transistor, we adopted the following strategy for solving this problem:

- Poisson and continuity equations are solved iteratively, with a convergence achieved.
- Heat transfer equation is solved with an initial temperature 300 K assumed for the device so as to predict the local temperature.

The numerical code was validate with Rahiman and al.[21] results in a SOI MOSFET structure. Figure 2 presents \( I_D-V_D \) characteristics compared to the experimental data [21].

3. Results and discussion

Gate shape effect’s on the electro-thermal behavior have been investigated in MOSFET structure based on high-k material. HfO₂ has been chosen as a gate dielectric placed above the dioxide SiO₂ with an equivalent oxide thickness (EOT).

Figure 3 depicts the temperature distribution along X-Y plane for \( V_D=2 \) V and \( V_G=1.2 \) V. The results are calculated in MOSFET structure as shown in figure 1. The dielectric gate HfO₂ is placed above the dioxide SiO₂ with EOT. As it can be seen from figure 3, the temperature maximal
especially in the SiO₂-Si interface due to the low thermal conductivity of SiO₂ layer. The temperature decreases until the substrate temperature which is similar to the previous work [10].

Figure 4 present the electric potential distribution in MOSFET transistor for \( V_{G}=1.2 \) V and \( V_{D}=2 \) V. It's clear that the maximum value of electric potential is in the drain part.

The dielectric thickness effect on the SHE in MOSFET structure is studied for different EOT and for a variable drain voltage as shown in figure 5 at fixed \( V_{G}=1.2 \) V. The simulation results suggest that the highest temperature is obtained with the high value of \( V_{D} \) and the low of EOT. However, the peak temperature value proves that at this point the tunneling probability of the carrier to the gate terminal through the oxide is maximum. Therefore, we should choose the low EOT value in order to significantly reducing the impact ionization.

Subsequently, we propose to study the gate shape effect three different gate shape as shown in figure 1 (b-d) are chosen in order to analyze the SHE in these structures. Figure 6 shows the maximum temperature variation with the drain voltage for a constant \( V_{G}=1.2 \) V. This study exhibits a quadratic temperature increase with the drain voltage \( V_{D} \). It is clear from this figure that the gate shape affects the temperature variation. The lowest temperature is achieved with square gate shape. For example, for \( V_{D}=2 \) V the maximum temperature is 352.89 K, 323.94 K and 322.5 K in T-MOSFET, C-MOSFET and S-MOSFET, respectively.

Figure 7 shows the variation of the temperature profile along the y axis in the centerline at the hot spot location near the drain region. The results are shown for \( V_{D}=2 \) V and \( V_{G}=1.2 \) V. The peak temperature is located at \( y=0 \) in the Si-SiO₂ interface. This maximum decreases significantly up to the substrate temperature \( T=300 \) K and the temperature have the same trend in all devices with different gate shape.

The temperature profile along the x direction is presented in figure 8 at the Si-SiO₂ interface. It is clear from this figure that the SHE is located in the drain side channel for all structures. Also, the hot spot is located near the drain region and the maximum temperature reaches up to 325 K using the triangular gate shape. The results obtained with the S-MOSFET are slightly higher than T-MOSFET and C-MOSFET. It is found that the use of square gate shape can endure the increase of the temperature in nanodevices.
The transient temperature profile in normal MOSFET is shown in figure 9 for different drain voltage. The results show the maximum temperature, which is located near the drain region at the Si/SiO₂ interface for \( V_G = 1.2 \) V. The temperature profile increases rapidly for \( t < 100 \) ps and slightly for \( t > 100 \) ps until the steady state is reached at \( t = 500 \) ps for different \( V_D \). The same study has been made in C-MOSFET, S-MOSFET and T-MOSFET structures with the same values of \( V_D \) and for the same \( V_G \). The relevant results show the same form of temporal temperature evolution, obtained with different structures, with different amplitude. For examples, for \( V_D = 2 \) V and at \( t = 500 \) ps, \( T_{\text{max}} = 321 \) K, 319 K, 318 K and 322 K in normal MOSFET, C-MOSFET, S-MOSFET, and T-MOSFET, respectively. Furthermore, we noted from these figures that the steady state is reached at \( t = 500 \) ps for the C-MOSFET, while it is at \( t = 700 \) ps for the S-MOSFET and the T-MOSFET.

Figure 10 shows the comparison of the temporal evolution of the peak temperature rise in different devices for constant \( V_D = 2 \) V and \( V_G = 1.2 \) V. Our results are compared with BTE and BDE models. It is clear from this figure that the steady state in T-MOSFET structure is achieved earlier than the other structures. However, a significant temperature rise is obtained using the BTE and BDE models and the temperature achieve so fast the steady state.

**Conclusion**

On this work, the self-heating effect is analyzed in MOSFET transistor with different gate shapes. The heat transfer equation and the semiconductor equations have been used to investigate the temperature distribution along devices. The effect of drain voltage and EOT have been discussed. In addition, the special and temporal evolution have been analyzed. The obtained results show that using different gate shape able to mitigate the SHE. Especially, the square gate shape is more appropriate to reduce the temperature device.

**Declarations**

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Figure captions

Figure 1: 2D Normal MOSFET (a), MOSFET with curve gate shape (b), MOSFET with square gate shape (c) and MOSFET with triangular gate shape (d)

Figure 2: Comparison of the output characteristics of simulated results with experimental data[21]

Figure 3: Temperature distribution along X-Y plane

Figure 4: Electric potential distribution along X-Y plane

Figure 5: Temperature distribution for different EOT and variable drain voltage

Figure 6: Maximum temperature profile versus drain voltage in MOSFET structure with different gate shape

Figure 7: Temperature profile along the y axis in MOSFET structure with different gate shape

Figure 8: Temperature profile along the x axis in MOSFET structure with different gate shape

Figure 9: Transient temperature profile in MOSFETs for different drain voltages.

Figure 10: Comparison of Transient temperature profile in different structures
Table captions

Table 1: Device parameters of MOSFET transistor
Figure 1

(a) 

(b) 

(c) 

(d)
Figure 2

![Graph showing the relationship between drain current (A) and drain voltage (V). The graph includes a line representing simulation results and red dots indicating experimental data.](image-url)
Figure 3
Figure 5
Figure 6

![Graph showing the relationship between Vd (V) and maximum temperature (K) for different MOSFET types: C-MOSFET, S-MOSFET, and T-MOSFET. The graph illustrates how the temperature increases with Vd for each type.](Graph.png)
Figure 7
Figure 8

The figure shows the temperature distribution across different MOSFET types (C-MOSFET, S-MOSFET, T-MOSFET) along the x-axis (nm). The x-axis represents the position along the device, while the y-axis represents the temperature (K). The color gradient indicates the temperature, with higher temperatures shown in warmer colors. The shaded regions at the top indicate the cross-section of the MOSFETs, with the source and drain regions clearly marked. The graph illustrates how the temperature profiles differ across the different MOSFET types.
Figure 9

(a) 

(b) 

(c) 

(d)
Figure 10

[Graph showing peak temperature rise (K) over time (ps) for different MOSFET types: Normal MOSFET, C-MOSFET, S-MOSFET, T-MOSFET, BDE, BTE.]
| Parameter                                | Value     |
|-----------------------------------------|-----------|
| Channel length                          | 50 nm     |
| Substrate length                        | 250 nm    |
| Vertical spacing of the device          | 160 nm    |
| oxide thickness                         | 1 nm      |
| doping concentration in Source/drain    | $1 \times 10^{20} \text{ cm}^{-3}$ |
| Channel doping concentration            | $1 \times 10^{17} \text{ cm}^{-3}$ |