Topical Review

Lateral $\beta$-Ga$_2$O$_3$ field effect transistors

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Received 24 May 2019, revised 3 October 2019
Accepted for publication 6 November 2019
Published 28 November 2019

Abstract

Beta phase Gallium Oxide (BGO) is an emerging ultra-wide bandgap semiconductor with disruptive potential for ultra-low power loss, high-efficiency power applications. The critical field strength is the key enabling material parameter of BGO which allows sub-micrometer lateral transistor geometry. This property combined with ion-implantation technology and large area native substrates result in exceptionally low conduction power losses, faster power switching frequency and even radio frequency power. We present a review of BGO epitaxial materials and lateral field-effect transistors developments, highlight early achievements and discuss engineering solutions with power switching and radio frequency applications in mind.

Keywords: gallium oxide, lateral transistor, radio frequency transistor, power switch, power conversion, ultra-wide bandgap

(Some figures may appear in colour only in the online journal)

1. Introduction

Beta gallium oxide (BGO) is the only semiconductor with a bandgap ($E_G$) greater than SiC and GaN that can be made an insulator or conductor and be grown from a melt. Large BGO substrates offer low cost manufacturing solutions, with some orientations already shown to support sizes up to four-inches in diameter [1]. The main identified drawbacks of BGO are (1) lack of p-type material resulting from a heavy effective mass of holes combined with self-trapping effect [2] and (2) low thermal conductivity [3, 4]. The lack of p-type doping will present unique challenges to compete with multi-kilo-volt-class SiC electronics. However, in the sub-kV range, unipolar devices based on BGO are expected to compete well with Si and GaN-on-Si applications [5].

BGO device topologies can be scaled far more aggressively for a given operating voltage because of the critical field strength ($E_{crit}$) of BGO ($\sim$8 MV cm$^{-1}$) being >25x larger than Si and more than double that of GaN. A simple unipolar two-terminal device is shown in figure 1 to illustrate the scaling advantages of BGO. A one-sided abrupt junction approximation is ideally suited as an upper bound analysis for comparing the depletion width ($W_{D}$) formed in Si, 4H-SiC,
Figure 1. Comparison of depletion width formations in common power semiconductors doped n-type to achieve a target breakdown voltage based on the annotated $E_{crit}$.

GaN and BGO and assuming each semiconductor is doped n-type to achieve the same breakdown voltage ($V_{BK}$). The one-side abrupt junction approximation is given as:

$$W_D = \frac{2V_{BK}}{E_{crit}}$$

The $W_D$ is significantly smaller for BGO, and the contacts can be placed very close together compared to other doped semiconductors for the same target $V_{BK}$ resulting in ultra-low resistance.

This manuscript uniquely reviews materials and device developments targeted to relevant applications served by lateral BGO transistors. Other comprehensive literature can be found to supplement this review with focus on the BGO material system [6–9], epitaxial synthesis [10], processing [11], early power devices [1, 12–14] and technology perspectives [5]. We review the transport and doping trade space of BGO homoepitaxy as well as early attempts at heteroepitaxy. We present lateral BGO transistor results in the literature and identify promising trends and gaps. The review concludes with a summary of lateral BGO FETs for revolutionary ultra-low power loss switch devices and the importance of heat extraction and device topology effects.

2. Relevant figures of merit

A summary of notable unipolar figures of merit (FOM) normalized to Si is listed in table 1. The primary application for BGO is low-loss power switching. Baliga’s figure of merit (BFOM) describes how well a semiconductor conducts in the on-state for a particular $V_{BK}$ and is a cubic function of $E_{crit}$. During the on and off switching cycles, power switching loss is considered and will dominate at high switching frequency. Huang’s material figure of merit (HMFO) describes the total conduction and switch power losses of a semiconductor from a gate charge ($Q_g$) perspective [15]. For BGO, the conduction losses are exceptionally low; therefore, it will switch at faster frequencies and accept a higher power switch loss for a given total power loss target. The optimum chip area to achieve minimal power loss is a square function of $E_{crit}$ and referred to as Huang’s chip area figure of merit (HCAFOM). According to the FOMs in table 1, the conduction losses of BGO are $>2500$x superior than Si and $>3$x better than GaN while the chip area is $>250$x and $>3$x smaller than Si and GaN, respectively. Additional circuit-level size reduction for power conversion occurs because faster switching translates to smaller energy switched per period compared to a slower switch; this reduces energy storage requirements (and size) of capacitors and inductors.

BGO radio frequency (RF) transistors may also perform well according to the carrier velocity ($v_{sat}$)-$E_{crit}$ product defined by the Johnson figure of merit (JFOM) [16]. The $v_{sat}$ of BGO must be approximately 40% of GaN to have the same JFOM. And, indeed, Gosh and Singisetti modeled peak electron velocity values in BGO as high as $2.0 \times 10^7$ cm s$^{-1}$ [17]. Given the requirements for aggressive scaling to achieve the JFOM gain-bandwidth product, the target application for BGO RF devices will be higher voltage operation at a given frequency covered by the application space of GaN. The unique high-voltage properties of BGO in the low-GHz RF trade space may especially be interesting for very high-efficiency Class E and F switch-mode amplifiers which rely on ultra-low $R_{ON}$ and high $V_{bak}$ [18].

High-efficiency operation requires addressing the thermal conductivity challenges of BGO that will require a top or bottom-side engineering solution, or a combination of both. In fact, the thermal dissipation problems faced by all wide bandgap materials are all worse than Si because thermal conductivity must be normalized by the high energy density properties enabled by $E_{crit}$. Huang’s thermal figure of merit (HTFOM) describes the material’s temperature rise for the optimum chip area condition delivering minimal power loss [15].

Thermal management can be viewed as an engineering challenge as was the case in the development of GaAs. GaAs has a similar thermal conductivity to BGO; yet, GaAs saw great success as a power amplifier and managed heat through top-side thermal shunts combined with substrate thinning [19]. For BGO, more emphasis should be on top-side heat extraction because the drift region can be greatly scaled and combined with integrated heat spreaders to permit a thick metal drain contact in close proximity to the gate-drain peak field hot spot [20]. As an example of the efficacy of the combination of simultaneous front side and backside thermal dissipation, Flosfia has reported a thin-membrane $\alpha$-Ga$_2$O$_3$ diode packaged with a thermal resistance of 13.9 $\text{CW}^{-1}$ compared to 12.5 $\text{C W}^{-1}$ for a similar SiC diode [21].

3. BGO epitaxy

3.1. BGO homoepitaxy

To enable a viable semiconductor device technology, it is imperative to develop epitaxial growth for semiconductor electronic materials to achieve high crystallinity, low background impurity density, and doping density control. To
avoid structural defects such as dislocations and stacking faults, homoepitaxial growth or growth on lattice matched substrates is preferred. BGO, unlike other wide band gap semiconductors, has the advantage of large wafer sizes grown by melt techniques such as Czochralski (CZ), Bridgeman, and float zone. In this section, we will focus the discussion on BGO homoepitaxial growth, which has been demonstrated using molecular beam epitaxy (MBE), metal organic vapor phase epitaxy (MOVPE), halide vapor phase epitaxy (HVPE), low pressure chemical vapor deposition (LPCVD), and pulsed laser deposition (PLD).

3.1.1. MBE. MBE has been one of the most popular methods of BGO thin film growth due to the long history of oxide MBE development using oxygen plasma or ozone as the oxygen source, standard effusion cells are used to deliver Ga as well as dopants Sn, Si, and Ge. The first reported n-type homoepitaxial BGO films were demonstrated by Sasaki [22] using ozone MBE with Sn dopants spanning a carrier concentration of $2.6 \times 10^{16}$ to $1.3 \times 10^{19} \text{cm}^{-3}$ with a corresponding mobility range of 101 to 32 cm$^2$ V$^{-1}$s$^{-1}$. Film growth rates were found to be more than ten times higher on (010) compared to (100) substrate plane (figure 2) attributed to higher re-evaporation rates of depositing species on (100) planes associated with a lower adhesion energy from the cleavage plane surface. Growth on the (001) substrate plane has also been achieved with a growth rate slower than that on the (010) plane but faster than that of the (100) plane (see figure 2) [23]. A Si doping study utilizing an oxygen plasma source has shown that it is difficult to use Si to achieve controllable light doping ($<\text{low } 10^{18} \text{cm}^{-3}$) in oxide MBE due to the reactions of O$_2$ with the Si surface in the effusion cell [24]. However, it has been demonstrated that delta doping and modulation doping can be achieved using the Si high flux doping for devices such as MODFETs and MESFETs, which will be discussed in a later section [25, 26].

A Sn-doped MBE study with an O$_2$ plasma source rather than ozone showed comparable concentration and mobility of $1 \times 10^{17} \text{cm}^{-3}$ and 80 cm$^2$ V$^{-1}$s$^{-1}$, respectively, that degraded to $1 \times 10^{18} \text{cm}^{-3}$ and $12 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ [27]. Follow-on work from Ahmadi [28] also used O$_2$ plasma MBE to report $2.8 \times 10^{18}$ to $7.5 \times 10^{19} \text{cm}^{-3}$ and 80 to 40 cm$^2$ V$^{-1}$s$^{-1}$ with Ge as the dopant and $5 \times 10^{16}$ to $1 \times 10^{20} \text{cm}^{-3}$ and 120 to 39 cm$^2$ V$^{-1}$s$^{-1}$ with Sn as the dopant. Since Sn atoms tend to aggregate to the surface and cause doping non-uniformity and a narrow growth temperature window [12], a preliminary assessment is that Ge may be a preferred dopant to both Si and Sn. Recently, researchers reported successful growth of coherent $\beta$-(AlGa)$_3$O$_3$/Ga$_2$O$_3$ heterostructures using plasma assisted MBE [29] and demonstrated modulation doping with improved mobility [24, 25]. The demonstrated maximum Al content is approximately 0.2 since AlGaO goes through a phase transition with Al content above 0.2 at typical MBE growth temperatures. To further increase the Al content, the growth temperature must be raised while preventing Ga desorption.

3.1.2. MOVPE. Oxide MOVPE (or MOCVD) is a relatively new technique still under development but it holds great promise for scaling up to production considering the success of MOVPE in producing arsenide and nitride semiconductors. Baldini [31] used MOVPE for BGO homoepitaxial growth with Trimethylgallium (TMGa) or Triethylgallium (TEGa) and pure oxygen or water used as precursors for gallium and oxygen, respectively. On-axis growth of (100) substrates, two-dimensional (2D) islands can nucleate in a twinned orientation due to the limited diffusion length of the atomic species and lead to the formation of incoherent boundaries and stacking faults [10]. This results in charge carrier compensation and degradation of the electron mobility to a maximum of 40 cm$^2$ V$^{-1}$s$^{-1}$. On the other hand, when the adatom diffusion lengths were comparable to or longer than the substrate terrace width, which was demonstrated on off-cut (100) substrates [10], the step flow growth mode prevails instead of the 2D islandic growth, which reduces or eliminates the stacking faults. As a result, a carrier concentration range of $5 \times 10^{17} \text{cm}^{-3}$ to $7 \times 10^{18} \text{cm}^{-3}$ and improved mobilities were demonstrated by Baldini [10] with 4° and 6° miscut (100) IKZ CZ crystals. This initial work with miscut crystals delineates a critical development for all homoepitaxial growth regimes and merits significant further exploration as substrate crystal fabrication methods mature. Gogova [32] also utilized Sn-doped MOVPE on CZ (100) crystals from IKZ to achieve $7.1 \times 10^{17} \text{cm}^{-3}$ and 13.7 cm$^2$ V$^{-1}$s$^{-1}$. Du [33] reported Sn-doped MOCVD films with $9.54 \times 10^{17} \text{cm}^{-3}$ and 12 cm$^2$ V$^{-1}$s$^{-1}$ on (100) substrates from an unspecified source. The same IKZ group demonstrated MOVPE on on-axis (010) substrates from Tamura Corporation with the same growth condition as the (001) substrate growth for an almost identical growth rate [10]. In contrast, they did not observe stacking faults, dislocations, or any interfacial defects using MOVPE on
(010) substrates. Si and Sn were successfully incorporated as n-type donors to give a concentration range of $1.2 \times 10^{17}$ to $8.5 \times 10^{19} \text{cm}^{-3}$ and $2.1 \times 10^{17}$ to $1 \times 10^{19} \text{cm}^{-3}$, respectively, and the associated mobilities were 130 to 55 cm$^2$ V$^{-1}$s$^{-1}$ and 102 to 47 cm$^2$ V$^{-1}$s$^{-1}$, respectively. The narrower Sn doping range was attributed to chamber Sn precursors and molecular oxygen. They demonstrated growth rates up to 10 $\mu$m h$^{-1}$ using TMGa at a substrate temperature of 900 $^\circ$C clearly showing a much faster growth rate using the CCS approach compared to the conventional vertical rotation disc reactor design (see figure 3).

Capitalizing on a low impurity concentration, Zhang [35] deposited an unintentionally doped BGO epitaxial film by MOCVD with a room temperature mobility of 176 cm$^2$ V$^{-1}$s$^{-1}$ and electron concentration of $7.4 \times 10^{19} \text{cm}^{-3}$. To enable ohmic contact, a heavily Sn-doped contact layer was regrown by MBE on contact areas with an SiO$_2$ regrowth mask.

A variant of MOCVD known as MIST-CVD has been utilized by Lee [36] to demonstrate conductivity control with Sn-doped films on (010) BGO. A carrier concentration range of $1 \times 10^{18} \text{cm}^{-3}$ to $5 \times 10^{20} \text{cm}^{-3}$ was measured with corresponding mobilities from 45 cm$^2$ V$^{-1}$s$^{-1}$ to 15 cm$^2$ V$^{-1}$s$^{-1}$.

Compared to other growth techniques, the MIST-CVD approach is simple and economical. However, challenges remain to address lower electron concentrations and mitigate Sn chamber memory effects.

### 3.1.3 HVPE

HVPE is a growth method of very high growth rate (20 $\mu$m h$^{-1}$), which can generate BGO films with very low residual carrier density as low as $1 \times 10^{13} \text{cm}^{-3}$ [12]. Therefore, it is particularly suitable to use HVPE films for high breakdown voltage vertical devices based on thick films of low background donor density. Figure 4 shows a schematic diagram of atmospheric-pressure HVPE system for BGO growth.
of a HVPE chamber in which Cl₂ is used to react with high purity Ga metal to form GaCl. GaCl then reacts with O₂ to produce the Ga₂O₃ film. SiCl₄ is used as the molecule for silicon doping. The electron density is the same as the Si doping density and controllable in the range of 10¹⁵–10¹⁸ cm⁻³ with mobility values up to more than 100 cm² V⁻¹ s⁻¹ [12]. Leach [37] demonstrated an electron concentration range of 3 × 10¹⁶ to 2 × 10¹⁷ cm⁻³ and a maximum mobility of 123 cm² V⁻¹ s⁻¹ in unintentionally doped BGO films. Films with Si dopants exhibited concentrations of 2 × 10¹⁸ to 1 × 10¹⁹ cm⁻³. At present, the BGO (001) substrate is the most popular substrate for HVPE growth; however, whether the (001) orientation is the best substrate choice for HVPE growth is still under investigation.

3.1.4 LPCVD. Similar to HVPE, LPCVD is an effective growth method of high growth rate with a relatively simple and inexpensive chamber design, often a tube furnace. Unlike HVPE, LPCVD does not involve Cl based gases and only uses high-purity Ga metal and O₂ as the precursors with SiCl₄ and inexpensive chamber design, often a tube furnace. Unlike HVPE, LPCVD does not involve Cl based gases and only uses high-purity Ga metal and O₂ as the precursors with SiCl₄ as the Si doping molecule. Rafique [38] fabricated LPCVD Si doped films with a concentration of 1.4 × 10¹⁸ cm⁻³ and a mobility of 72 cm² V⁻¹ s⁻¹ on (010) substrates, and the group also demonstrated a carrier concentration of 9.5 × 10¹⁷ cm⁻³ and a mobility of 42 cm² V⁻¹ s⁻¹ on (001) substrates. The demonstrated deposition rate of ~1 μm h⁻¹ is attractive as vertical devices will require multiple μm-thick epitaxial films.

3.1.5 PLD. PLD is a physical vapor deposition method, of which a laser is used to ablate the target to deposit thin films. While PLD can deposit single crystal quality BGO film in homoepitaxy, it has, so far, been difficult to achieve accurate impurity doping control due to the lack of high-purity targets. The major strength of PLD is its ability to achieve high Si doping, as Si-doped PLD films from Leedy [39, 40] showed a high electron concentration of 1.74 × 10²⁰ cm⁻³ and a mobility of 26.5 cm² V⁻¹ s⁻¹. Combined with the fact that the deposition temperature of BGO film via PLD (~550 °C) is lower than most other techniques, PLD is a very attractive method for Ohmic contact regrowth for BGO-based heterostructures and delta-doped layers.

3.2. Survey of epitaxial sources

A wide range of n-type doping from 10¹⁶ to 10²⁰ cm⁻³ carriers in BGO thin films is evident in figure 5 where Hall effect data is shown for films with Si, Sn and Ge dopants from four deposition techniques, two substrate fabrication methods and three growth planes. Results from MBE, MOVPE, LPCVD, and PLD show a consistent relationship between mobility and concentration largely independent of deposition technique and dopant. A majority of the BGO substrates used for the deposited films in figure 5 were (010) Fe-compensation doped crystals fabricated by the edge-defined film fed growth (EFG) method from Tamura Corp. More limited homoepitaxial films were prepared on (100) crystals made by IKZ with the CZ method and (001) Fe-doped crystals made by Tamura with EFG.

Given the variety of deposition techniques and crystal orientations represented in figure 5, the consistency of the mobility data is encouraging for a technology in its infancy. The electron mobility decreases approximately as a power law with increasing carrier concentration, which is not unexpected given that donor ionized impurity scattering increases as a reciprocal of the donor concentration, 1/N_d. However, as we see in a comparison to the model of Ma et al [41], also plotted in figure 5, the power law decrease of mobility with carrier concentration is weaker than that expected from the combination of polar optical phonon scattering and donor ionized impurity scattering. At high doping levels, this deviation is not unexpected; the mobility is higher than indicated by the model due to the formation of donor impurity bands which merge with the conduction band at degenerate doping levels. At lower doping levels, the deviation of the experimentally measured mobility indicates scattering from additional sources such as energetically deep neutral impurities (e.g. oxygen vacancy deep donors [42]), compensating acceptors (e.g. gallium vacancies [43], Fe diffusion from semi-insulating substrate [44]) or extended defects (e.g. twin boundaries, stacking faults [10]). The polar optical phonon limited mobility could also be slightly lower than that estimated by Ma et al [41]. Nevertheless, it is clear that further improvement in Ga₂O₃ mobility is possible through the elimination of defects during material growth, including compensating acceptors and unintentional donors which will be discussed in the next section.

As far as the choice of substrate orientation, although early (001) growth efforts showed reduced mobilities and a narrower concentration range compared to results from (010) studies, continued studies with alternative growth planes to (010) are essential to fully assess the device capabilities of BGO. Last, with MBE successfully demonstrating modulation doping for MODFETs in the AlGaO/GaO heterostructure (highest Al content ∼0.2), it is natural to move this development forward with higher Al content, higher sheet carrier density (n_s), and more efficient doping. It is expected that other growth techniques will be used for this heterostructure, especially those with higher growth temperatures to achieve the goal of higher Al content.

To summarize, as a thermally stable material with the availability of native substrates, BGO is ready to be explored with various growth techniques. While each technique has its own strengths and weaknesses, in general it is feasible to grow BGO with single crystal quality, high mobility (>100 cm² V⁻¹ s⁻¹), and sufficiently low residual carrier density (<10¹⁷ cm⁻³) via homoepitaxy with each of these techniques.

4. BGO doping

To realize reliable and repeatable semiconductor material properties as a basis for electronic device technologies, precise control of carrier density in semiconductors is necessary
through intentional doping and the reduction of unintentional doping. The rapid pace of BGO device development can be attributed in part to the effective and controllable n-type doping of BGO as well as compensating acceptor doping to form semi-insulating substrates and current blocking layers. In this section, we give an overview of various intentional and unintentional dopants.

4.1. Donors

N-type doping has been achieved by using group IV elements such as tin (Sn) [31, 45–50], silicon (Si) [31, 51–54], and, more recently, germanium (Ge) [28, 55]. Details of each element in various growth methods were covered in the last section. In this section, we discuss two fundamentally related questions about these group IV donors, namely, (1) Are these group IV elements true shallow donors in BGO? and (2) Do they behave like negative-U centers (i.e., DX centers)? An early study by Varley [42] reported Si, Ge, and Sn as shallow donors based on the formation energy calculation using first-principle DFT modeling. More recently, Lany performed detailed DFT modeling including the $c(+/−)$ positive/negative charged donor transition energy calculation and concluded that only Si is a true shallow donor while Ge and Sn have delocalized impurity states near the conduction band minimum (CBM), which might be close enough for ionization at room temperature [56].

In the early history of semiconductor research, shallow donors were defined as electron donors possessing donor energy close to the room temperature thermal energy so that most of the extra electrons can be ionized into the conduction band by thermal activation. More advanced first-principle calculations reveal that not all shallow donors have delocalized resonance states, which can be more easily explained by the hydrogen model. This model is not complete since it gives the same donor energy to all donor impurities in a certain host semiconductor crystal. The true shallow donors have delocalized states close to CBM.

Recent DFT simulations raise questions about the functionality of Ge and Sn as shallow donors, because they would have the problem of self-compensation and/or the DX center behavior. Lany [56] considers those possibilities with regard to Ge and Sn and cites the recent electron paramagnetic resonance (EPR) study from Son [57] as a support claiming DX center behavior in unintentionally doped (UID) EFG substrates from Tamura Corp. In contrast, Son [57] attributes the DX center behavior to the Si donor, instead of Ge and Sn donors predicted by Lany as possible DX centers. Therefore, the calculation of Lany is not consistent with the EPR result from Son [57] for Si. On the other hand, Irmscher [58] performed an EPR study on Si doped Czochralski (CZ) substrates and claimed there is no observation of DX centers. It is noted that EFG substrates must undergo a thermal activation process to activate the Si donors while CZ substrates do not require this process, which might explain these discrepancies.

Neal et al [59] addresses some of these questions through Hall-effect transport studies of BGO grown by various methods. Through simultaneous fitting of the temperature dependent carrier density and mobility curves, they conclude that the Si and Ge donor energies are approximately the same, 30 meV at low doping density (see figure 6), consistent with the donor energy estimated by the hydrogen model. Furthermore, the result is not consistent with the electron distribution statistics of the DX centers. Despite all of this, from...
indicates that the simultaneous transition density, due to the onset of impurity band formation, drop in donor energy as the carrier density approaches the Mott are also included as indicated in the donor energy sensitive to changes as small as 5 meV.

donor concentration from.

Mobile shallow acceptors are not predicted in BGO due to the flat heavy-hole dispersion curve at around the Brillouin zone center with very high hole effective mass and the self-trapping nature of holes [2]. Experimentally, only deep acceptors such as Fe, Mg, N, and Zn have been verified; there are no reports of shallow acceptors in BGO. Even though hole transport is not predicted, deep acceptors are still important in creating semi-insulating substrates and current blocking layers/regions.

Fe is, perhaps, the most studied deep acceptor since it is used in the commercially available semi-insulating substrates produced by Tamura Corp. The Fe impurity state energy of 0.8 eV below the CBM is relatively well characterized by Ingebrigtsen [62] using deep level transient spectroscopy (DLTS) corroborated by secondary ion mass spectrometry (SIMS). The result is consistent with the high temperature Hall-effect transport measurement by Neal [59]. While it is well established that Fe acts as a compensation acceptor in BGO, the fact that the measured impurity state has the acceptor energy closer to CBM rather than the valence band maximum (VBM) makes the Fe-doped BGO an N-type semiconductor rather than P-type. Note that Fe is known for its multivalent nature in other semiconductors [63] and, therefore, there are likely other occupied Fe states below this 0.8 eV state.

Mg is another deep acceptor used to form semi-insulating substrates [64] and current blocking layers [65, 66]. The energy states of Mg in BGO are less clear. Neal [59] performed high temperature conductivity measurement of a Mg doped substrate provided by Northrop Grumman Synoptics and obtained an activation energy of 1.1 eV, consistent with a previous report on the activation energy of highly Mg doped BGO [67]. Because Si contamination is present in CZ grown samples, the activation energy of 1.1 eV is expected to be approximately equal to the acceptor energy for Mg. However, without Hall-effect measurements, it is not possible to determine the carrier type of the Mg doped sample because it is not known if the observed 1.1 eV activation energy is referenced to the CBM or VBM of BGO. Recent DFT calculations do indicate that the Mg acceptor level is closer the VBM [68]. More research needs to be conducted to understand the energy states of the Mg dopant in BGO. One common drawback of Fe and Mg is the high atomic diffusion length observed in BGO when implanted [44, 66]. Consequently, while it should be acceptable to use them as compensating acceptors to form semi-insulating substrates, this may present a challenge for current blocking layers/regions formed by ion implantation.

As an alternative, researchers have used nitrogen [69] in an attempt to replace Mg and Fe as a compensating acceptor in a current blocking layer due to the thermal stability with minimal diffusion. Although the location of N impurity levels in the BGO bandgap is not clear, early research on N-doped BGO nanowires [70] indicates it is a deep acceptor, consistent with DFT calculations [71, 72]. Similarly, an early study [73] also claims that Zn can induce p-type conductivity in BGO nanowires. Besides impurities, Chikoidze et al claimed to observe p-type conduction via Hall effect and Seebeck effect measurements on a PLD Ga2O3 film deposited on c-sapphire substrate at elevated temperatures [74]. The p-type conduction was tentatively attributed to gallium vacancies based on thermodynamic equilibrium calculations of the Ga2O3 crystal – O2 gas system [74].

While Fe and Mg are the easy choices for deep compensation acceptors in the BGO melt growth of semi-insulating substrates, more study is warranted to not only understand the nature of all varieties of compensating acceptors but also determine optimal solutions for the formation of current blocking layers.

4.3. Unintentional dopants

Unintentional doping is an important research topic for semiconductors because it sets the lower limit of the residual doping and carrier density, which in turn sets the upper limit on device breakdown voltages. Unintentional doping is also a source of additional scattering which degrades the carrier mobility. In MBE, theoretically unintentional doping is
generated mostly by intrinsic defects such as vacancies without cross contamination. A chemical deposition process generated mostly by intrinsic defects such as vacancies that can be incorporated unintentionally from the precursor molecules (e.g., H, C, Cl) and the growth chamber wall itself. An early first-principle calculation indicates that the Ga vacancy could be the main culprit for compensating acceptors while the O vacancy can be a neutral donor scattering center [42], and that the Ga vacancy is energetically more favorable than the oxygen vacancy even in a Ga-rich environment [75]. A positron annihilation study confirmed that the Ga vacancy is a deep acceptor [76].

Hydrogen is believed to be a shallow donor either as an interstitial or incorporated on the oxygen site [42], and hydrogen can passivate Ga vacancies according to first principles calculations [43, 77]. Theoretical, carbon is believed to be a deep DX center [56]. However, there is a contradictory theory that it can be a shallow donor [78]. Moreover, there are relatively shallow defects with energy about 100 to 200 meV reported by Neal [79] and Farzana [80], but there is no indication of their origin. Figure 7 shows the temperature dependent carrier density, normalized to room temperature, of two EFG grown samples measured via high temperature Hall effect measurement up to T = 1000 K. The increase in carrier density above room temperature indicates the existence of these defects and cannot be explained by unintentional Si donors alone. Fitting of the temperature dependent carrier density estimates a defect energy of 110 meV for these samples in addition to the Si shallow donor. In short, the study of unintentional dopants in Ga2O3 is still in its infancy where more studies are needed to confirm the properties and impacts of these unintentional donors. However, this is not an easy task, especially for native defects, considering most electronic characterization techniques (e.g., DLTS, Hall effect) only measure the energy level and the density of the defect, not their chemical nature. Techniques such as positron annihilation and EPR could determine the chemical nature of these defects but have their own limitations, such as limited sensitivity (mostly working only for thick samples such as substrates or high defect density samples). Correlation of all these techniques with growth experiments and reliable first-principle calculation is needed to identify and perhaps reduce the density of these unintentional dopants.

4.4. Doping by ion-implantation

Ion-implantation doping of n-type BGO has been reported and utilized for device engineering. The most studied implant species has been Si to achieve a wide range of conductivity from 1017 cm−3 to >1020 cm−3 with an activation temperature of 900 °C to 1000 °C with >60% activation efficiency [81]. The most common implant activation condition has been a furnace anneal for 30 min in Nitrogen. BGO substrates have retained sub-nanometer root mean square AFM surface roughness up to 1100 °C annealing temperature. However, at 1100 °C, the activation efficiency sharply decreased with observed Si diffusion to the regions with the most ion damage [81]. Ion damage in BGO was studied for Sn, Ar and P species [82], but ion-implantation doping with shallow Sn and Ge species has not yet been reported.

Tetzner et al found Nitrogen (N+) ion-implantation to be a good candidate for electrical isolation for BGO device applications [83]. The RsH for N+ implanted regions was as high as 1013 Ω/sq and was robust up to 600 °C with post-implantation anneal. Lattice recrystallization of the implant damage was observed at 800 °C with sharp reduction in RsH. Deep acceptor ion implantation with Mg and N+ species was recently reported by Wong et al [84]. N+ was found to be superior to Mg in terms of retaining the as-implanted depth profile and current blocking at the required activation temperature. Current blocking characteristics of N+ significantly improved at 1200 °C. Conversely, Mg leakage current increased as the annealing temperature approached the optimum activation point. This phenomena was shown using a vertical cavity BGO transistor with current blocking that greatly improved with N+ implant over Mg [85].

It is important to note that, at this time, BGO is the only semiconductor in the ultra-wide bandgap family of materials (those with Eg larger than GaN and SiC) that can be implanted. As a result, device engineering strategies such as self-aligned gate-source contacts are realizable to remove parasitic resistance that is critical for low power losses under power switching or RF operation.

5. Lateral BGO FETs

5.1. Early BGO FET device milestones

The first epitaxial BGO FETs were reported by NICT between 2012–2016. The first device structure was a ~300 nm Sn-doped MBE channel on (010) Fe-doped BGO substrate with a ring design to achieve electrical isolation [86]. A Schottky gate device achieved a Vbr = 257 V before a gate oxide was introduced to reduce gate leakage and obtain
higher $V_{RB} = 370$ V BGO MOSFET [45]. The MOSFET also had the first reported Si-ion implanted contacts [81]. An all-implanted BGO MOSFET was demonstrated in 2015 using Si species to vary the electron concentration from $\sim 3 \times 10^{15}$ cm$^{-3}$ in the channel to $> 1 \times 10^{19}$ cm$^{-3}$ for the ohmic contact regions [87]. A $V_{RB} = 415$ V was achieved with lower $R_{ON}$ and high $I_{ON}/I_{OFF} > 10^9$. In 2016, the device was field-plated (FP) using a T-shaped gate designed with 2.5 $\mu$m extension over the gate-drain access region with 0.4 $\mu$m SiO$_2$. The FP MOSFET demonstrated a $V_{RB}$ of 755 V and is among the highest measured $V_{RB}$ measured in air [88].

In 2016, the Air Force Research Laboratory (AFRL) reported a BGO MOSFET using an epitaxial channel layer grown with MOVPE by IKZ. A 200 nm Sn-doped homoepitaxial BGO film was grown directly on (100) Mg-doped BGO substrates. The mobility was limited to $\sim 20$ cm$^2$ V$^{-1}$s$^{-1}$ as a result of stacking faults later found to be resolved by implementing a slight mis-orientation of the substrate [12, 75]. A seminal result was obtained after blocking 230 V over a 0.6 $\mu$m gate-drain drift region and yielding an average $E_{crit} = 3.8$ MV cm$^{-1}$. This is the highest reported $E_{crit}$ ever obtained for a lateral transistor and surpassed the theoretical $E_{crit}$ values for GaN and SiC for the first time. Sentaurus modeling of this device indicated peak electric fields of 5.3 MV cm$^{-1}$ [89].

5.2. Depletion-mode BGO MOSFET studies

The first generation depletion-mode devices reported by AFRL were single layers of 200 nm Sn-doped homoepitaxial BGO grown by MOVPE directly on (100) Mg-doped BGO substrates [90]. The effects of channel thickness and doping concentration variations were studied, and the off-state voltage ($V_{OFF}$) behaved, as predicted, by the following relationship:

$$V_{OFF} = V_{FB} - \frac{qN_d d_{ch}}{C_{ox}} = \frac{qN_d d_{ch} 2}{2\varepsilon_b\varepsilon_o}$$  (2)

where $V_{FB}$, $d_{ch}$, and $C_{ox}$ are the flatband voltage, channel thickness and gate oxide capacitance, respectively.

Using Sn-doped BGO grown by MBE at Novel-Crystal Technology, Moser et al modeled the I-V effects of doping concentration in the range of $0.7 \times 10^{18}$ to $1.6 \times 10^{18}$ cm$^{-3}$ for a given channel thickness. Trapping and self-heating effects were suppressed by applying 200-ns pulses. Excellent agreement between modeled and measured I-V performance of each FET was accomplished by analyzing the C-V hysteresis effect as a function of $N_D$ and introducing an interface charge component to equation (2) [91]. The current density ($I_{DS}$) substantially increased to $>0.45$ A mm$^{-1}$ under pulsed operation; thus, the promise of pulsed power applications was highlighted as one solution to overcome BGO thermal limitations.

The first Ge-doped BGO MOSFET reported by AFRL and UCSB validated claims that Ge is a shallow donor alternative to Si and Sn [55]. The MOSFET channel was doped $\sim 4 \times 10^{17}$ cm$^{-3}$, and the measured room temperature Hall Effect mobility was 111 cm$^2$ V$^{-1}$s$^{-1}$ which is among the highest reported for BGO epitaxial films. The device achieved a $I_{DS} \sim 80$ mA mm$^{-1}$, $V_{RB} = 479$ V and performed similarly to previously reported BGO devices with a similar level of Sn or Si doping. Additional studies are required to determine the optimal BGO doping species.

Wong et al. studied the effects of incorporating a resistive buffer grown by MBE between the BGO substrate and channel layer [92]. One important finding was the suppression of leakage current formed by a Si accumulation layer at the buffer/substrate interface. This Si-rich layer has also been confirmed by SIMS on MOVPE BGO samples by Baldini [31]. By increasing the buffer epitaxial growth temperature, a compensating or Si-activation effect likely occurs which is evident in the sharp increase in on/off current ratio and $V_{TH}$ shift [92]. Joishi et al. found at least a 600 nm thick buffer was required to mitigate dc-to-RF dispersion caused by Fe-diffusion [93]. In the presence of Si-implant species, a thickness of about 1.2 $\mu$m was sufficient to fully suppress the anomalous diffusion of Fe from the substrate into the implant damaged regions [44]. Semi-insulating BGO buffer films and/or electrical isolation may be viable with N-doping in light of recent studies with BGO substrates indicating high resistivity of N implantation [83] and favorable thermal diffusivity properties of implanted N compared to Mg species [84].

Early radiation hardness of BGO FETs was evaluated by Wong et al using gamma-rays [94]. For up to 1.6 MGy(SiO$_2$) irradiation, less than 5% reduction in $R_{ON}$ and $I_{DS}$ resulted. The off-state current was the main limiting factor as a result of leakage caused by a degraded gate oxide and trapping that can be improved with future dielectric and interface optimization. Otherwise, intrinsically, BGO was unaffected by high-doses of gamma-rays which is promising for space applications.

5.3. Nano-membrane BGO MOSFETs

BGO can be mechanically exfoliated by cleaving multi-layered nano-membranes (NM) for rapid device demonstrations. The mechanism is unlike two-dimensional van der Waals materials and occurs because of the high anisotropy of the BGO unit cell. Cleavage planes occur along (001) and (100) where oxygen atoms share bonds differently with neighboring Ga atoms. The (100) is the lowest energy plane of the two and is noted as the easiest plane to cleave [6].

Hwang et al. was the first to demonstrate a BGO FET using a bulk-cleaved BGO NM in 2014 [95]. The ~100 nm BGO NM was cleaved from the (100) plane with $N_D = 5.5 \times 10^{17}$ cm$^{-3}$ and $\mu = 112$ cm$^2$ V$^{-1}$s$^{-1}$. The NM was transferred to a p-type Si wafer as a back-gate with 285 nm thermal oxide as the gate dielectric. Impressive early performance of a few mA/mm on-current, $I_{ON}/I_{OFF} > 10^9$ and high voltage operation up to 70 V was achieved leaving substantial room for optimization. The early demonstration was key to envisioning the use of high-thermal conductivity substrates with insulating behavior such as AlN, SiC or diamond as a solution to the low thermal conductivity challenges of BGO.

Several device demonstrations using multi-layered BGO NMs would soon follow as commercial availability of BGO.
substrates from Tamura Corp. increased. In 2016, bottom-gated BGO NM FETs were demonstrated as well as top-gated devices with ALD Al2O3 dielectric by cleaving from (-201) UID BGO substrates [96, 97]. Device engineering was demonstrated by tuning the BGO NM thickness by dry-etching [98] and wet-etching [99], BGO NM interface and processing observations [100–102] as well as radiation tolerance [103] were reported with FETs with reasonable performance. Integration with other exfoliated quasi-2D materials such as hexagonal BN [104, 105], WSe2 [106] and graphene [107] were all demonstrated.

Aggressive lateral and vertical scaling of MOSFETs formed by back gating BGO NMs on conductive substrates was reported by Purdue University. By tuning the thickness of exfoliated NMs, depletion and enhancement mode FETs were demonstrated with over 0.4 A mm⁻¹ current densities using sub-micrometer source-to-drain spacing [108]. By scaling the channel length to about 300 nm and using highly doped NMs, the devices were able to achieve a record high

\[
I_{DS} = 1.5 \text{ A mm}^{-1}\text{ with an } I_{ON}/I_{OFF} > 10^9 \quad [109].
\]

5.4. Enhancement-mode BGO FETs

Unipolar BGO MOSFETs are normally-on which is undesirable for fail-safe power electronic applications. Depletion-mode BGO transistors typically must sacrifice higher \(R_{ON}\) in exchange for a fully-depleted channel in the gated region. For example, implementing multiple gated fins, reducing doping concentration and gate-recessing can lead to normally-off operation.

The first reports of enhancement-mode operation were made using a resistive BGO channel with a high work function gate metal to deplete at \(V_{GS} = 0 \text{ V}\). Zeng \textit{et al} reported this device topology but high-voltage operation in the off-state was not achieved [110]. Chabak \textit{et al} used a multi-gate fin-array channel combined with lower doping and high work function metal to fully deplete the channel at \(V_{GS} = 0 \text{ V}\) and achieve over 600 V breakdown voltage [111]. The fin-array channels and high-contact resistance resulted in low on-current but an \(I_{ON}/I_{OFF} > 10^7\). Wong \textit{et al} used a UID channel with high resistance and self-aligned source and drain implanted contacts to demonstrate normally-off operation; though, without a drift region, high-voltage operation was not achieved [112].

A normally-off device can also be achieved by gate-recess to adjust the channel thickness within the depletion region width induced by the work function and surface states. The first report of this included a 200-nm channel with epitaxial cap to lower contact resistance. After removing the epitaxial ohmic cap layer, a second BCl3 ICP etch was used to remove BGO channel material under the gated region. A \(V_{TH}\) of about \(\sim 3 \text{ V}\) was extracted with nearly 200 V breakdown at \(V_{GS} = 0 \text{ V}\) with \(I_{ON}/I_{OFF} > 10^7\) [113]. Later, an improved version was reported with up to 40 mA mm⁻¹ and breakdown over 500 V using ALD SiO₂ with high conduction band offset to reduce gate leakage in the on-state [114]. For this device, the C-V results were integrated from the off-to-on-state to estimate \(Q_G\) and report the first \(R_{ON} Q_G\) figure of merit which has already exceeded the theoretical limit of Si.

5.5. Ohmic contacts to BGO

Metal compositions, mainly with a Ti layer in contact with a moderately doped BGO layer, have been used in conjunction with annealing to yield linear but high contact resistance, \(R_C\). Yao \textit{et al} experimented with several metals with work functions close to GaO (201); a preferred metal scheme of Ti/Au annealed at 400 °C for one minute resulted in good linear ohmic behavior [115]. A four-layer stack (Ti/Al/Ni/Au) utilized in GaN work has also been used to obtain ohmic contacts with rapid thermal annealing (RTA) in an N₂ atmosphere for one minute at 470 °C on BGO (100) and (010). This metal stack resulted in linear ohmic behavior with Sn-doped BGO [55, 89, 91, 114].

To obtain low \(R_C\), \textit{in-situ} deposition of a degenerately doped (\(\sim 1 \times 10^{19} \text{ cm}^{-3}\)) epitaxial layer is a viable approach. Green et. al fabricated a device using a thin \(\sim 25 \text{ nm}\) blanket cap layer of highly doped BGO grown \textit{in-situ} by MOVPE. The layer was patterned for the ohmic metallization and etched away from the channel region using a BCl₃ dry etch. An \(R_C \approx 3.3 \Omega \cdot \text{mm}\) was reported using TLM test structures [116].

Figures 8(a) and (b) show that selective area regrowth using PLD is a viable option to lower \(R_C\) for BGO FETs. PLD layers with Si concentration up to \(\sim 1.1 \times 10^{20} \text{ cm}^{-3}\) [39] were deposited on a patterned SiO₂ regrowth mask after performing a BGO recess etch to access the 2DEG sheet charge layer of a \(\beta-(\text{Al}_{1-x}\text{Ga}_{x})\text{O}_{2}\)/\(\text{Ga}_2\text{O}_3\) MODFET. A \(R_C \approx 1 \Omega \cdot \text{mm}\) was measured on TLM test structures without requiring an ohmic anneal and relying on a sidewall contact to the heterostructure. The low \(R_C\) results in \(R_{ON} = 40 \Omega \cdot \text{mm}\) as indicated in figure 9. With regrowths, the \(n++\) layer needs to have conformal sidewall coverage, as shown in figure 8, or additional interfacial resistance will develop. The \(n+\) junction has additional resistance that needs to be taken into consideration. Contact resistance calculations are also complicated by the high \(R_{SH}\) of the material processed.
can be removed in HF after diffusion and patterned with Ga2O3 MODFET regrowth structures.

As a result, the calculation errors could be of similar magnitude to the extracted contact resistance [117].

MBE has also been used for selective area regrowth of highly doped BGO. Zhang et al [25] used this method to obtain a contact resistance of 4.1 Ω·mm to a β-(Al,Ga,In)2O3/Ga2O3 heterostructure. Xia et al [26] obtained a contact resistance <1.5 Ω·mm on a BGO device sample. In this scheme, the contact areas were recess-etched and regrown with an n++ layer with a Si carrier density above 10^{20} cm^{-3}. Because these are MBE regrowths performed with a Si source cell, they are currently limited to delta-doped regrowth structures.

An example of Sn-diffusion to produce low R_C was demonstrated by Zeng et al [118]. A commercially available spin-on glass with Sn concentration exceeding 1 × 10^{21} cm^{-3} was deposited, and the diffusion process takes place in nitrogen for 5 min at ∼1200°C. The spin-on glass can be removed in HF after diffusion and patterned with fluorine-based RIE for device fabrication. A R_C of ∼3 Ω·mm was measured on a low-doped BGO epitaxial layer which would have otherwise been 1–2 orders of magnitude higher than a simple ohmic metal contact.

Si ion implantation has also been used to reduce R_C. Sasaki et al [81] first demonstrated Si-ion implantation using multiple energies and dose ratios to obtain a 150 nm deep box profile. The lowest R_C obtained through circular TLM test patterns was ∼0.21 Ω·mm for BGO after a 1000°C activation anneal. Both channel and ohmic contact regions were ion implanted.

5.6. Dielectric materials for BGO

Dielectric materials for gate insulator, passivation and/or field oxides are critical for high E_Crit operation of BGO FETs. Additionally, the dielectric/BGO interface must be optimized to reduce interface traps, leakage and surface depletion which degrade transistor performance. There is generally a tradeoff observed between E_Crit and the dielectric constant (κ), as depicted in figure 10, which are both desired for a large energy barrier to reduce leakage and increase electrostatic coupling under the gate. The most commonly studied dielectrics for BGO are Al2O3, SiO2 and HfO2.

The Al2O3/BGO interface has been the most studied since it is easy to deposit by ALD and possesses about the same κ as BGO and has a larger E_Crit. The band alignment was reported for plasma-enhanced Al2O3 on n-type (010) BGO, and MOSCAPS revealed long time constant, fixed charged border traps. The conduction band offset (∆E_C) was measured to be 1.5 ± 0.2 eV [119]. Carey et al reported a higher ∆E_C for the same interface with 2.2 ± 0.6 eV and 3.16 ± 0.8 eV for sputtered and plasma-enhanced ALD Al2O3, respectively [120]. The interface states (D_α) of Al2O3/BGO were reported lower on (010) BGO compared to (010) BGO as a result of a crystalline interlayer that forms on (010) BGO [121]. High-low C-V characterization revealed a D_α as low as 5.9 × 10^{10} cm^{-2}eV^{-1} for Al2O3 on (010) BGO. Zhou et al reported improvement of D_α down to ∼2.3 × 10^{11} cm^{-2}eV^{-1} using Piranha treatment for Al2O3 on (010) BGO by using photo-assisted C-V measurements [101]. The dominant leakage mechanism of the Al2O3/BGO MOSCAP under forward bias conditions is attributed to trap-assisted tunneling (for ∆E_C = 0.7 eV) [122].

The SiO2/BGO interface has the highest ∆E_C and is expected to reduce Fowler-Nordheim tunneling and operate better under high-temperature operation. Jia et al reported a large ∆E_C = 3.63 eV between plasma-enhanced ALD SiO2 and (010) BGO by XPS [123]. On (010) BGO, a ∆E_C = 3.1 eV was reported by Konishi with plasma CVD SiO2 [124]. Zeng et al studied the D_α of ALD SiO2 on (010) BGO and found no surface treatment resulted in the lowest D_α (∼6 × 10^{11} cm^{-2}eV^{-1}) compared to HF and HCl treatments [125]. The ALD SiO2/BGO interface was analyzed by C-V-T on (010), (010) and (001) oriented substrates with MOSCAPs; it was found (011) had the highest D_α at room temperature while (010) had the lowest. Though, for all three orientations, the D_α value decreased to <1 × 10^{12} cm^{-2}eV^{-1} when measured at 200°C or higher.

Figure 9. Transistor family of curves for a β(Al0.14Ga0.86)2O3/Ga2O3 MODFET 2 × 50 μm device with degenerately Si-doped BGO grown by PLD and resulting in low R_C and R_ON.

Figure 10. Dielectric constants of common semiconductors and insulators as a function of bandgap energy.
Other novel wide bandgap dielectrics have been investigated on BGO. The HfO2 on (201) BGO band alignment is reported to have a $\Delta E_C = 1.3$ eV extracted from electrical measurements [126] and XPS [127]. HfO2 is commonly reported to have a lower $\kappa$ than the predicted value of $\sim 30$ [91, 127]. Wheeler et al also extracted $\Delta E_C = 1.2$ eV for ZrO2 deposited by ALD on (201) BGO which possesses a good combination of large $E_G$ and high $\kappa$ [127]. Carey et al reported sputtered LaAlO3 with $E_G = 6.4$ eV and $\Delta E_C = 2.01 \pm 0.6$ eV with (201) BGO ($\kappa \sim 22$) [128]. Masten et al measured (Y0.5Sc0.5)2O3 on (010) BGO MOS-CAPS with $D_h < 1 \times 10^{12}$ cm$^{-2}$eV$^{-1}$ that is estimated to have a $\Delta E_C = 2.31$ eV and $\kappa = 9.6$ [129]. The AlN/BGO interface is also attractive as it could also have dual-use as a heat spreader on the BGO surface. AlN was found to have just 2.4% in-plane lattice mismatch to (201) BGO grown by PLD on sapphire substrate and $\Delta E_C = 1.75$ eV [130]. Interestingly, an AlN layer deposited by thermal and plasma-enhanced ALD was reported to have a $\Delta E_C = 1.39$ eV and $\Delta E_C = 0.58$ eV, respectively, with BGO (orientation unspecified). The origin of the different $\Delta E_C$ values is likely due to the Al-O bond formations between the two deposition techniques [131].

5.7. High power BGO MOSFETs

The University of Buffalo investigated the high-voltage performance of BGO FETs. A gate-connected field-plate design was employed with novel high-$\kappa$ and low-$\kappa$ field oxide layers to confine the peak fields in the high $E_{crit}$ dielectric layers. High-voltage performance was also enhanced by submerging in Fluorinert to suppress air breakdown. A BGO MOSFET with 20 $\mu$m gate-drain spacing and $\sim 1.5 \times 10^{16}$ cm$^{-3}$ Sn-doping achieved $V_{th} = 1.85$ kV—currently among the highest reported for lateral BGO MOSFETs [132]; and, a device with a 1.8 $\mu$m drift region achieved a peak $E_{crit} > 3$ MV/cm according to a device model.

In late 2018, a high BFOM surpassing 50 MW cm$^{-2}$ was reported by USTC for a depletion-mode BGO MOSFET with a FP structure [133]. The device was designed with Si-implanted ohmic contacts, a Si-doped BGO channel grown by MOVPE with $R_{th} = 3.6$ kΩ/sq, and a source-connected FP on a SIN field dielectric layer. The FP extended the breakdown of a $L_{SD} = 11$ $\mu$m device from 260 V to 480 V and a $L_{SD} = 18$ $\mu$m device from 310 V to 680 V. A record-high 155 MW cm$^{-2}$ BFOM was reported recently from Tetzner et al using a BGO MOSFET submerged in Fluorinert [134]. The device employed a gate-connected FP formed in SiN with $L_G = 0.7$ $\mu$m on a 200 nm Si-doped BGO channel grown by MOVPE using a (100) mis-oriented Mg-doped substrate. The carrier concentration and mobility were $2.3 \times 10^{17}$ cm$^{-3}$ and 128 cm$^2$ V$^{-1}$s$^{-1}$, respectively, from Hall measurements. The gate was recessed $\sim 100$ nm into the channel using BCl3 ICP etching. A three-terminal $V_{th}$ of 445 V and 1830 V was measured on a device with $L_{GD}$ of 2 $\mu$m and 10 $\mu$m, respectively.

The highest breakdown BGO FET was recently reported in 2019 by ETRI using a 150-nm Si-doped channel with a source-connected FP [135]. The $L_{GS}$, $L_G$ and $L_{GD}$ were 2 $\mu$m, 3 $\mu$m and 25 $\mu$m, respectively. The FP dielectric layer was 300-nm thick PECVD SiO2 and the FP extended 3 $\mu$m over the drift region. A $V_{th}$ of 2.3 kV was achieved at $V_{GS} = -10$ V while submerged in Fluorinert.

5.8. BGO MOSFET RF device scaling

RF transistors based on BGO, as well as other semiconductor material systems, achieve high-performance with lateral and vertical scaling coupled with high saturation velocity ($v_{sat}$). Ghosh et al report ab initio calculations for $v_{electron}$ in BGO with peak electron velocity as high as 2 $\times$ 10$^6$ cm s$^{-1}$ at 0.2 MV cm$^{-1}$—nearly double the 1.1 $\times$ 10$^5$ cm s$^{-1}$ value shown in table 1 and surpassing GaN [17]. The maximum oscillation frequency, $f_{max}$, is a strong function of the current-gain cutoff frequency, $f_T$, estimated by $v_{sat}/2\pi L_{th}$ in the short-channel limit. However, as $L_{th}$ decreases, the channel charge location must be closer to the gate contact to compensate for reduced gate-to-channel electrostatic coupling. To date, this has been accomplished primarily by gate-recess, delta-doping, or simply a thin-channel n-type epitaxial layer.

Green et al demonstrated the first BGO RF device in 2017. The device implemented a gate-recess to reduce the channel thickness from 180 nm to $\sim 90$ nm. The gate length was $\sim 0.7$ $\mu$m with a T-shaped cross-section for low $R_C$. An epitaxial ohmic contact layer lowered the $R_C$ to just over 3 $\Omega$-mm, and the $R_{th}$ was $< 5$ kΩ/sq before the recess etch. The combination of low $R_C$ and $R_{th}$ reduced source access resistance ($R_S$) and resulted in a higher transconductance, $G_M$, of $\sim 21$ mS mm$^{-1}$. Small-signal measurements at $V_{DS} = 40$ V resulted in $f_T$ and $f_{max}$ of $\sim 3$ and 13 GHz, respectively. Class-A, CW large-signal power measurements at 800 MHz with $V_{DS} = 25$ V showed $P_{max}$ = 0.23 W mm$^{-1}$ with a 6.3% PAE. The results were limited by severe heating which can be significantly improved with thermal shunting [116].

Scaling the bulk channel thickness and compensating with higher $N_D$ is another viable approach for increased RF device gain. Chabak et al reported this approach on a Si-doped BGO FET with 65 nm thin channel, $\sim 90$ cm$^2$/V$\cdot$s electron mobility and target $N_D \sim 2 \times 10^{15}$ cm$^{-3}$ grown by MOVPE at IKZ-Berlin directly on a (010) Fe-doped BGO substrate [136]. A T-shaped gate defined by electron beam lithography with $L_G = 140$ nm was formed by etching the gate length geometry in PECVD SiO2 and then realigning with a wider metal stripe to form the cap. Despite having high $R_C$, an $f_T$ and $f_{max}$ of 5 and 17 GHz, respectively, were measured. This is the first demonstration of a T-gated BGO device and has the highest measured $f_{max}$ reported to date.

Delta-doped transistors have been investigated in the past in different material systems for their vertical scaling advantage with high $n_{th}$ in confined channel near the surface [137]. Krishnamoorthy et al demonstrated the first delta-doped BGO FET with maximum $I_{DS} = 236$ mA mm$^{-1}$ and a $G_M$ of 26 mS mm$^{-1}$ [138]. Hall effect measurements indicated a mobility of 34 cm$^2$/V$\cdot$s and $n_{th} = 3.3 \times 10^{13}$ cm$^{-2}$. Later Xia et al improved the device characteristics by implementing MBE regrown ohmic contacts on a MESFET device [26].
With an estimated delta-doped layer thickness of 0.2 nm, they obtained a maximum $I_{DS} = 140$ mA mm$^{-1}$, $G_M = 34$ mS mm$^{-1}$ and $n_{sh} = 1.2 \times 10^{11}$ cm$^{-2}$. While the Hall effect mobility was not reported, the maximum extracted field effect mobility was 95 cm$^2$V$^{-1}$s$^{-1}$. The most recent delta-doped BGO FET combined the above with a 120 nm T-gate to extend $f_T$ to a record-high 27 GHz with high $G_M = 44$ mS mm$^{-1}$ [139].

5.8.1. MODFETs. An improvement over delta-doped FET is the MODFET (Modulation-Doped Field-Effect Transistor). In a MODFET, two semiconductors with different bandgaps are joined together. The discontinuity forms a potential well in the conduction band where electrons (holes) are quantum mechanically confined perpendicular to the growth direction forming a two-dimensional electron (hole) gas. This enables the device to have a higher mobility with reduced impurity scattering.

Early demonstrations of $\beta$(Al$_x$Ga$_{1-x}$)$_2$O$_3$/Ga$_2$O$_3$ MODFET structures suggest a path toward improved mobility and device performance. Ahmadi et al demonstrated a MODFET with a Ge delta-doped layer with $n_{sh} = 1.2 \times 10^{13}$ cm$^{-2}$ that obtained $I_{DS} = 20$ mA mm$^{-1}$ (mobility was not reported) [140]. Krishnamoorthy et al reported a Si delta-doped MODFET with $n_{sh} = 5 \times 10^{12}$ cm$^{-2}$ which achieved $I_{DS} = 5.5$ mA mm$^{-1}$ and a mobility of 74 cm$^2$V$^{-1}$s$^{-1}$ [24]. For these above results, the presence of a 2DEG was inferred using $C$-$V$ measurement though limitations occurred with non-optimal contact resistance.

Recently Zhang et al showed the first MODFET channel without parallel conduction in the barrier layer. Temperature-dependent Hall measurements and Shubnikov-de Haas oscillations indicated the presence of a 2DEG [25]. The sample was comprised of a UID BGO buffer/channel layer and a 27 nm $\beta$(Al$_x$Ga$_{1-x}$)$_2$O$_3$ (x $\sim 0.18$) barrier layer. A Si delta-doped layer was positioned 4.5 nm away from the BGO channel in the barrier layer. A device with $L_G = 0.7 \mu$m achieved $I_{DS} = 46$ mA mm$^{-1}$ with an electron mobility of 180 cm$^2$V$^{-1}$s$^{-1}$ and $n_{sh} = 2 \times 10^{13}$ cm$^{-2}$. The small signal measurements showed a $f_T$ of 3.1 GHz and $f_{max}$ of 13.1 GHz. The paper outlined maximum delta-doping limits for a given band offset and spacer layer thickness.

Zhang et al followed with a double heterostructure design with $n_{sh} = 3.85 \times 10^{12}$ cm$^{-2}$ which is larger than the single heterostructure design [141]. A mobility of 123 cm$^2$V$^{-1}$s$^{-1}$ was obtained despite contributions from a parallel parasitic channel. Impressive device performance consisting of $I_{DS} = 257$ mA mm$^{-1}$, $G_M = 39$ mS mm$^{-1}$, and $E_{crit}$ = 3.2 MV cm$^{-1}$ were demonstrated with $L_G = 0.6 \mu$m.

Impressive high-voltage performance was demonstrated with a $\beta$(Al$_x$Ga$_{1-x}$)$_2$O$_3$/Ga$_2$O$_3$ (x = 0.22) MODFET from Joishi et al [142]. The epitaxial design consisted of a 25 nm AlGaO barrier with Si-delta doping above a 5 nm AlGaO spacer which formed a 2DEG in the UID BGO channel/buffer with $n_{sh} = 3.4 \times 10^{12}$ cm$^{-2}$ electron concentration and 101 cm$^2$Vs mobility at room temperature. The device design consisted of a gate-connected FP with SiN field oxide layer. A device with $L_G = 1.3 \mu$m and $L_{GD} = 0.32 \mu$m recorded a $V_{BR} = 121$ V with $E_{crit} = 3.9$ MV cm$^{-1}$—among the highest $E_{crit}$ measured in a lateral transistor. A $V_{BR} = 1.37$ kV was measured in a device with $L_{GD} = 16 \mu$m. The $V_{BR}$ measurements were made under vacuum to avoid dielectric breakdown.

5.9. Summary of lateral BGO FETs

Important lateral BGO device milestones have been summarized in figure 11. Most notable are measuring record $E_{crit}$, obtaining enhancement-mode operation in the absence of a p-type inversion layer, and achieving RF performance. Important topics such as achieving a high-mobility 2DEG, semi-insulating layers for field management, ion-implantation and self-aligned transistor design are essential for ultra-low power losses in future BGO devices. There are also noteworthy literature results on vertical transistors—namely a vertical cavity BGO device with both shallow and semi-insulating ion-implantation [85], a vertical trench MOSFET [143] and a vertical fin-channel FET [144, 145]—the latter achieving $V_{BR} > 1$ kV. Vertical BGO FETs may be beneficial for high voltage operation while lateral ones target faster switching in the sub-kV range. Table 2 summarizes top device performance among lateral BGO FETs reported in literature.

6. Conduction losses in BGO FETs

Power switching is the primary target application for BGO. As a power MOSFET switches from the off to on state, it transitions from a high-voltage capacitor (depletion capacitance) to a low-loss conductor (contact and material sheet resistance). The dc conduction losses, defined by Baliga’s Figure of Merit (BFOM), are inversely proportional to $E_{crit}$, clearly illustrating the importance of BGO compared to GaN and Si [146]. The BFOM is a useful power switch device metric to compare power switching conduction losses in the on-state as a function of its $V_{BR}$ rating (in the limit of no dynamic switch losses). The BFOM can be expressed as

$$BFOM = \varepsilon \cdot \mu \cdot E_{crit}^3 = 4 \cdot V_{BR}^2 / R_{ON,sp}$$

For BGO, we must consider that devices are unipolar in the absence of p-type carriers. The n-type layer, or drift region, should only be thick enough to sustain the upper limit depletion width approximation calculated from the one-sided abrupt junction relationship re-written from equation (1) as:

$$W_D = \varepsilon_o \cdot \varepsilon_i \cdot E_{crit} / (q \cdot N_D)$$

Where $\varepsilon_o \cdot \varepsilon_i$ is the product of permittivity of free-space and BGO dielectric constant. Any drift region distance beyond $W_D$ translates to parasitic resistance leading to additional power loss and should be eliminated.

Figure 12 illustrates a three-terminal FET with $W_D$ shown in the drift region between gate and drain. The drift region should be engineered to be equal to the calculated $W_D$ without any additional parasitic resistance in the drain access region.
the peak $E_{crit}$ is always higher than the measured $E_{avg}$. FPs and engineered doping profiles are options to reduce the peak fields. Singisetti et al demonstrated both with ALD and PECVD SiO$_2$ as the field oxide layers and a gate-connected FP to extend $V_{BK}$ [132]. FPs and engineered doping profiles (in n-type only devices), however, come at some cost to other performance parameters such as $R_{ON}$ and gate voltage swing, $\Delta V_{G}$. 

Figure 13 shows the $R_{ON,SP}$ versus $V_{BK}$ trade space for all lateral BGO device results that report both $R_{ON}$ and $V_{BK}$ from the same BGO FET with an epitaxially grown channel. The theoretical lines for each semiconductor technology using equation (3) and values from table 1 are also displayed.

It should be noted that BFOM was originally derived for a one-sided junction where $R_{ON}$ is normalized to the area of the depletion region viewed in the direction of the applied field—for vertical devices this is simply the area of the anode contact. However, for a lateral device, the anode (gate) and the direction of the depletion toward the drain are normal to one another. For a uniformly doped channel, the $R_{ON}$ should be normalized to $d_{CH}$ · $W_G$ which is the area of the depletion region looking into the applied field along the channel. For heterostructure devices forming a 2DEG, the normalized $R_{ON}$ is usually overestimated using $W_G$ · $L_{SD}$ since $d_{CH}$ is negligible.

7. Dynamic switch losses in BGO FETs

7.1. Switching losses

The previous section discussed conduction losses, but dynamic losses related to power switch operation in the time domain should also be considered to capture the total power loss during device operation. The total switch power loss is given by equation (7),

$$ P_{loss} = I_{OUT}^2 R_{ON} + C_{IN} V_{G}^2 f $$

which is composed of the conduction losses, $I_{OUT}^2 R_{ON}$, and dynamic losses, $C_{IN} V_{G}^2 f$. The combination of the two is benchmarked by the $R_{ON}$ and $Q_G$ product for a given $V_{BK}$ [15]. The $R_{ON} \cdot Q_G$ figure of merit is a tradeoff between reducing resistance and increasing capacitance (hence $Q_G$.
Figure 14 shows the $\text{RON} \cdot \text{QG}$ theoretical material limits for common semiconductors as a function of $V_{BK}$.

### 7.2. Dynamic switch loss case study

In this section, we discuss the impact of gate design with respect to dynamic switch loss. Gate charge, $Q_G$, is calculated from measuring the input capacitance, $C_{ISS}$, expressed as

$$C_{ISS} = C_G + C_{GD} + C_{DS}$$

of the device where $C_G$, $C_{GD}$ and $C_{DS}$ are the device capacitances between the gate-source, gate-drain and drain-source contacts, respectively. To estimate $Q_G$, the source and drain electrodes are shunted, and the gate electrode bias is swept from $V_{GS,OFF}$ to $V_{GS,ON}$. The gate capacitance is measured and integrated with respect to voltage to calculate total $Q_G$ removed during the device turn on. This method provides an estimate of the total gate charge that is dependent only on the BGO channel design; and, although it is not equivalent to the $\text{RON} \cdot \text{QG}$ figure of merit, it does provide a starting point for estimating the advantages of the material system.

To examine gate geometry and its impact on gate capacitance, two device designs are compared. Both designs were fabricated on the same sample. The BGO channel ($65$ nm) was Si-doped and grown by MOVPE at IKZ on a $010$ Fe-doped BGO substrate purchased from Tamura. The donor concentration and mobility were measured to be $\sim 3 \times 10^{18} \text{cm}^{-3}$ and $\sim 80 \text{cm}^2/\text{V} \cdot \text{s}$, respectively. Mesa isolation was performed with a BCl$_3$ based ICP dry etch. Ohmic electrodes (Ti/Al/Ni/Au) were deposited by metal evaporation followed by a $470$ °C anneal. Next, $20$ nm of Al$_2$O$_3$ was deposited by ALD, and the sample was split into two process routes. One, seen in figure 15(a), shows an e-beam subtractively defined gate into SiO$_2$ field dielectric with a selective etch stop on the Al$_2$O$_3$ gate dielectric. On other parts of the sample, a standard T-gate was defined by liftoff directly on the Al$_2$O$_3$ (fabricated and tested prior to SiO$_2$ deposition) and can be seen in figure 15(b). For the last step for each sample was thick metal (Ti/Au) evaporation of source, gate, and drain interconnects.

Transfer characteristics can be seen below in figure 16(a). The maximum $I_{DSS}$ for the large gate head device (black) and

### Table 2. Record Device Performance Parameters for Epitaxially Grown Lateral BGO FETs.

| Parameter       | Units        | Depletion-Mode | Enhancement-Mode |
|-----------------|--------------|----------------|-----------------|
| Avg $E_{crit}$  | MV cm$^{-1}$ | $3.8, 3.9$ (V) | $\sim 1.0$      |
| Static $I_{DS,max}$ | mA mm$^{-1}$ | $275$          | $40$            |
| Pulsed $I_{DS,max}$ | mA mm$^{-1}$ | $478$          | —               |
| $G_m$           | mS mm$^{-1}$ | $44$           | $7.5$           |
| $R_{ON}$        | $\Omega \cdot$mm | $\sim 20$  | $215$           |
| $V_{BE}$        | kV           | $0.75, 2.32$ (F) | $0.61$        |
| BFOM            | MW cm$^{-2}$ | $50.4, 155$ (F) | $\sim 39$ |
| $f_T$           | GHz          | $27$           | —               |
| $f_{max}$       | GHz          | $17.1$         | —               |

* (F) denotes measurement was made in Fluorinert; (V) denotes measurement made under vacuum.
T-gate device (red) were 266 mA mm\(^{-1}\) and 253 mA mm\(^{-1}\) respectively with an \(I_{ON}/I_{OFF}\) ratio \(\geq 10^4\). Both devices had low leakage currents below 1 nA mm\(^{-1}\) after sharp pinch offs of about \(-20\) V. The \(G_M\) was measured to be 26 mS mm\(^{-1}\) and 30 mS mm\(^{-1}\) for the large gate head and T-gate, respectively.

Figure 16(b) shows \(C_{ISS}\) as a function of \(V_{GS}\). As expected, \(C_{ISS}\) in the off-state is significantly greater in the large gate head device due to extra parasitic capacitance. For each device type, the change in \(C_{ISS}\) from \(V_{GS,OFF}\) to \(V_{GS,ON}\) should be due to the depletion of the doped channel. The change in gate capacitance for the T-gate design is measured to be 15 fF whereas the large gate head measures a change in capacitance of about 50 fF. The capacitive ratio between the two device types closely matches the geometric ratio of the top of the T-shape. To estimate the gate charge portion of the device FOM from equation (8), \(C_{ISS}\) from figure 16(b) must be integrated from \(V_{GS,OFF}\) to \(V_{GS,ON}\). Additionally, the \(R_{ON}\) can be obtained by measuring the slope of the output curves in the linear region. The \(R_{ON}\) optimization product can then be plotted as a function of \(V_{GS}\) as seen in figure 16(c) where, this case, a minimum exists for optimal dynamic switch power loss. As the operational frequency increases, \(R_{ON}\) optimization becomes increasingly important. Other than the previously mentioned steps to minimize the drift region distance and maximize the doping, the gate geometry should be optimized to minimize the gate charge needed to turn the device off through reduction of parasitics.

8. Thermal considerations for BGO

8.1. Device modeling perspective

As processing and materials development matures, removal of parasitic components will allow the devices to operate closer to the fundamental limit set by the intrinsic material parameters. We expect BGO to follow a similar path to maturation, but with different materials level challenges driving device level mitigation strategies. For BGO, the benefits are clear; its \(E_{crit}\) is extremely high, the bulk defect density should be low due to melt-grown native substrate availability, the peak operating temperature is high, etc. The dominant materials-level challenges to design around will, instead, be the low bulk thermal conductivity (\(\lambda\)) of BGO which means wherever there is a large amount of power dissipation per unit volume there will be high temperature gradients and potentially high temperatures, if the proper device design is not employed. Here, we use device modeling to explore ways to design devices with thermal engineering solutions based on the following two focus areas:

1. How to optimize device design for optimal power density while not overheating the active region given the low bulk thermal conductivity of BGO.

2. The need to understand thermal aspects of very tightly scaled devices (e. g. for low-medium voltage applications with \(V_{BB} < 1.2\) kV).

8.2. A channel size case study

Figure 17(a) compares three hypothetical devices differing only in gate to drain spacing. In all cases the devices are biased in the on-state so that Joule heating is approximately uniform in the channel (with a slight skew toward the drain), and for comparative purposes the drain voltage is adjusted for the same 400 K temperature drop peak to ambient. While it is too early to predict the temperature at which mature devices will fail, this rather high value was chosen to represent a notional absolute maximum temperature for comparative purposes. In all cases, the model assumes the substrate is thinned to 20 \(\mu m\) on an ideal heat sink (not shown), such that (for gate pitch \(>20\) \(\mu m\)) the device periphery and layout is largely immaterial to the thermal analysis. The thermal conductivity of BGO was approximated as \(\lambda = 16 \times (T/300)^{1.135} \text{W/m/K}\).

Figure 17(b) shows plots of the depth profile of peak temperature (in all cases about the center of the depletion region). Because the channel dimensions vary, the thermal resistance of the three structures varies, from 79.8 K W\(^{-1}\) as removal of parasitic resistances and reducing \(L_{G}\) brings the projected \(R_{ON}Q_G\) within state-of-the-art GaN HEMT results. Additional optimization is possible with BGO epitaxial engineering towards quasi-2DEG transport; thus, allowing deep sub-micron lateral scaling of \(L_{G}\) towards unprecedented fast power switching and small die size for future integration.
(largest), 104.2 K W$^{-1}$ (middle), and 117.6 K W$^{-1}$ (smallest). Taking 20 K W$^{-1}$ as a rough goal for comparison with GaN [147], we see that the first 20 K W$^{-1}$ temperature drop is encountered in the first 1.69 μm, 0.53 μm and 0.15 μm below the hot spot, respectively, for largest to smallest channels. Approximately, this is the thickness required to reach this metric through substrate thinning. An exact determination would require a full thermal model of the package, the die attach solution, the thermal boundary resistances, an allowance for roughness and imperfections at the bottom of the die, etc., Regardless, any deviation from a perfect heat sink will affect the smaller channel proportionately more.

8.3. A top-side heat extraction case study

Figure 18(a) shows the thermal profile for a nominal structure with channel dimensions as reported in [89] but with an 816 μm periphery ring topology. As before, it is apparent that the bulk of the temperature drop is at the microscale. As a function of substrate thickness, we observe that thinning the substrate from 500 μm to 20 μm to 3 μm improved the thermal resistance from 190 K W$^{-1}$ to 90 K W$^{-1}$ to 53 K W$^{-1}$, all assuming an ideal bottom heatsink as a best-case scenario. In contrast, when topside heat extraction is modeled the thermal resistance can drop dramatically. Figure 18(b) shows the improvement when a 2 μm conformal heat spreader is placed on top of the 20 μm structure, plotted as a function of the thermal conductivity of this conformal layer. Here, the material is assumed to fill in the channel region and replacing or augmenting the passivation layer, and followed with a conformal coating of copper (or another material of similar thermal conductivity) over the entire device. With a much-improved heat path from the hot spot to the ohmic, even a modest 50 W/m/K thermal conductivity lowers thermal resistance from 90 K W$^{-1}$ to 26 K W$^{-1}$ and only 13 K W$^{-1}$ at the drain corner of the gate. Here, the gate temperature is plotted alongside the peak temperature because gate metals are likely to thermally fail before bulk Ga$_2$O$_3$, or barrier dielectrics in current use (Al$_2$O$_3$, HfO$_2$), even if the channel materials are hotter.

8.4. The thermal impact of nanoscale device design

Because a majority of the temperature drop is at the microscale, the size and location of the heat dissipating region matters far more in BGO than in competing materials (e.g.
SiC, GaN, Si. The percentage contribution of this ‘first micron’ to the total thermal resistance is much higher for a tightly scaled device. Specifically, the shape and composition of the channel, gate and drain matter greatly. As an example, figure 19 compares the impact of gate recess at the same steady-state power dissipation conditions. The right side shows a thinner and more highly doped channel, with the more tightly scaled depletion region driving the hot-spot thermal resistance from 22 (left) to 35 (right) K/W. Electrically, the device to the right is superior (e.g. lower on resistance from more highly doped channel), but the tighter confinement comes at a thermal cost. Both assume a 100 W/m/K topside layer for efficient heat extraction, corresponding to the third point to the left in figure 18 (b).

8.5. Summary

We have seen that the ideal thermal approach will be very different for a device optimized for sub-kV breakdown compared to one for tens of kV. Likewise, the ideal thermal approach will depend on what the most thermally susceptible material is; it is not necessarily sufficient to optimize based on the peak temperature. Additionally, the proper thermography techniques to quantify the peak temperature will need attention for tightly scaled devices. Last, we saw that the nanoscale device design affects peak temperature and must be considered for its thermal impact as well as for electrical reasons. In all cases, thermal resistances comparable to today’s GaN devices should be achievable with the right device fabrication approach. As a useful aside, it’s not the power passed through the device, it’s the power dissipated that matters. As discussed in previous sections, for a power switch this is combination of device-level loss factors such as ohmic resistance, channel

![Figure 17](image)

**Figure 17.** (a) An offset gate showing difference that channel scaling makes; all devices have a 0.25 μm source to gate channel, 0.5 μm gate length, and from top to bottom have 0.5, 2.5, and 12.5 μm gate to drain spacing. The hot spot is near the top of the 200 nm BGO channel, just under the barrier dielectric (not visible) and between the gate and drain (rightmost bi-layer). Black dotted lines are referenced in (b). (b) Depth profiles of temperature for the black dotted lines of (a). The smallest channel (bottom curve) has the quickest drop in temperature with depth. The vertical bars show the first 20 K W⁻¹ of thermal resistance.

![Figure 18](image)

**Figure 18.** (a) A centered gate showing the highly localized hot spot at 40 V bias, open channel. The hot spot is near the top of the 200 nm BGO channel, just under the barrier dielectric (not visible) and between the gate and drain (rightmost bi-layer). The model assumes the substrate is thinned to 20 μm. (b) When the topside is coated with a conformal dielectric heat spreader of varying thermal conductivity (not shown), in contact with a copper topside thermal shunt, modeled thermal resistance drops dramatically.

![Figure 19](image)

**Figure 19.** The legacy device (left) [89] compared to an improved device with a recessed gate (right). Only a portion of the gate (red and tan stack) and drain (black) are visible. Left and right plots are in all cases plotted on the same scale; 0 to 3 × 10¹⁸ cm⁻³, 0 to 1.7 × 10¹² W cm⁻³, 27 to 177 °C.
resistance and switching speed and system-level loss factors which are functions of circuit layout, switching frequency and more. As such, we note that as the materials system matures the ideal thermal approach will couple device-level modeling with a system-level model to optimize both.

9. Conclusions

This paper has reviewed BGO materials and device advancements toward power switching and radio frequency applications. The high $E_{\text{crit}}$ of BGO, its most coveted material property, was shown to have great promise for ultra-low total dynamic switch power losses, chip-size reduction and fast switching frequency with reduced passive energy storage requirements at the circuit level. Though BGO is still new, it is promising that over half of its predicted mobility and $E_{\text{crit}}$ has been achieved in short order along with availability of large native substrate sizes. The good news is, so far, an ∼1 MV cm$^{-1}$ has been achieved by multiple groups for lateral BGO FETs; this is compared to 211–26 typical achieved in lateral GaN HEMTs after several years of research.

Acknowledgments

The authors acknowledge scientists at IKZ-Berlin for their continued support and collaboration on a joint BGO materials and devices effort. We would also like to recognize the Air Force Office of Scientific Research for partially supporting this work under grant FA9550-17-1-0279.

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