INTERPLAY: An Intelligent Model for Predicting Performance Degradation due to Multi-cache Way-disabling

Panagiota Nikolaou*†, Yiannakis Sazeides†, Maria K. Michael*†

*Department of Electrical and Computer Engineering and KIOS Centre of Excellence, †University of Cyprus

Abstract—Modern and future processors need to remain functionally correct in the presence of permanent faults to sustain scaling benefits and limit field returns. This paper presents a combined analytical and microarchitectural simulation-based framework called INTERPLAY, that can rapidly predict, at design-time, the performance degradation expected from a processor employing way-disabling to handle permanent faults in caches while in-the-field. The proposed model can predict a processor’s performance with an accuracy of up to 98.40% for a processor with a two-level cache hierarchy, when multiple faults suffer from faults and need to disable one or more of their ways. INTERPLAY is 9.2x faster than an exhaustive simulation approach since it only needs the training simulation runs for the single-cache way-disabling configurations to predict the performance for any multi-cache, way-disabling configuration.

Index Terms—permanent faults, multi-cache way-disabling, graceful performance degradation, analytical predictive model

I. INTRODUCTION

Continued device miniaturization has enabled the integration of many cores and larger caches in processors. A modern processor contains multiple caches that take a large fraction of the total chip area (40%-60%) [1]. However, the scaling benefits for caches are confronted with reliability challenges caused by dynamic variations, e.g., aging [2], [3], and operation at low voltage levels [4]. To ensure reliable cache operation one can use spares to replace unreliable cache parts [5], however, this incurs high area costs [6].

One industry limits spare overheads is with in-the-field mechanisms for disabling cache segments that are detected to suffer from permanent (frequently repeating) faults [7]–[10]. Particularly, Intel processors use the Cache Safe Technology to dynamically disable cache lines and cache ways. As it is mentioned in [7], "...Up to 32 cache lines or up to 2 ways per set can be disabled on detection of post-production ECC corrections." Also, IBM’s POWER has in the field disabling capabilities for failing portions of the L1 D-cache and up to six lines in L2 [9]. When the disabled portion of a cache remains within pre-defined limit, set at design time by the hardware vendors, a processor remains in operation but its performance can be degraded due to the extra misses caused by the smaller cache capacity. Otherwise, when the disabled portion it exceeds the predefined-limits, the part is marked for field-return. Clearly, as it is mentioned for various real products, cache disabling can degrade performance or lead to a field return. Therefore, it is imperative to assess at design time the performance degradation caused by different cache-disabling configurations. For instance, hardware vendors need to provide an indication to their customers on the expected performance degradation when a processor activates way-disabling.

Performance degradation analysis can be done at design-time using simulation to determine field return policies (e.g., which cache-way disabling configurations should flag a field return), so that customers do not suffer from large or unknown performance degradation in-the-field. Thus, there is a need to quantify at design-time the performance impact when operating with different cache-disabling configurations to develop field return policies and to inform customers of the expected performance penalty when way-disabling is used. Cache-disabling can be applied at different granularities, by disabling the line or the entire cache-way that contains a fault [7]–[11]. Figure 1 shows a performance analysis of cache way-disabling for a processor with a two-level cache hierarchy, for 21 different applications and all possible cache-way disabling configurations. The processor has a 4-way IL1$ cache, a 4-way DL1$ and an 8-way L2$. Thus, the total number of way-disabling cache configurations of the processor are $4 \times 4 = 128$ (assuming there is at least one operational way in each cache) and are shown on the x-axis (denoted by L2$ _IL1S$). Configuration 8_4_4 is the baseline configuration with no disabling in any of the caches. Each configuration is evaluated for each of the 21 workloads (i.e., total $128 \times 21 = 2688$ data points, the methodology details are given in Section IV). The x-axis is sorted according the degradation suffered by any benchmark for a given way-disabling configuration.

It can be seen from Figure 1 that for 85 out of 128 (or 66.4%) of the configurations there is at least one benchmark that exceeds a hypothetical threshold of performance degradation of 20% (set by the manufacturer based on user requirements). When these way-disabling configurations occur in the field the processor can raise a flag for replacement [7], [9], [10]. One way to determine at design-time the performance degradation due to cache way-disabling, is to exhaustively evaluate, using micro-architectural simulators, all the possible combinations of way-disabling in one or more caches. However, this is, in general, non-practical as the time complexity...
grows as a product of the number of ways in the cache hierarchy. For example, for a processor with an 8-way IL1$, 8-way DL1$, 16-way L2$ and 20-way L3$, 20480 simulations are needed per application to cover all cache way-disabling configurations $(8 \times 8 \times 16 \times 20)$.

An alternative way, is to use analytical methods, in addition to simulation, to predict the performance degradation due to cache disabling. Unfortunately, most existing works predict performance degradation due to disabling in only a single cache [12]–[15]. Another related work [16], attempts to reduce power, given a performance constraint, using multi-cache way-power-gating. The work in [16] uses a greedy method to determine the best power-gating configuration. However, this method is only applicable during operation, it is heuristic-based and can suffer from a large performance degradation which needs to be detected and remedied on-line. In contrast to prior work, our paper aims to predict the performance degradation of all multi-cache way-disabling configurations at design-time in an accurate manner which requires, as we show later, to account for the interplay between caches at different levels.

This work proposes INTERPLAY, the first to our knowledge, efficient, design-time, framework capable of predicting in-the-field processor performance degradation due to multi-cache way-disabling. In particular, our main contributions are:

- The INTERPLAY framework that predicts the performance of any multi-cache way-disabling configuration based on a new performance-degradation analytical model that uses microarchitectural statistics from the simulation of single-cache way-disabling training runs. The number of simulations needed for each benchmark by INTERPLAY is proportional to the sum of the number of ways in the various caches instead of their product that is required by the exhaustive simulation approach.
- We validate INTERPLAY for a specific processor using 14 single-cache way-disabling combinations for training to predict the performance degradation of 114 multi-cache way-disabling configurations, for 21 benchmarks. The results show an average performance degradation prediction error of just 1.4% with more than 9x reduction in simulation time as compared to the exhaustive simulation approach.

The rest of the paper is organized as follows: Section II describes the INTERPLAY framework. Section III presents the proposed analytical prediction model. Section IV describes the evaluation setup, and Section V presents and discusses the results. Finally, Section VI concludes this paper and discusses some future directions.

II. INTERPLAY HIGH LEVEL FLOW AND USE

INTERPLAY combines simulation and an analytical model to quickly assess the performance of any multi-cache way-disabling configuration of a processor. It is based on an intelligent selection of a small subset of cache way-disabling configurations for which no benchmark incurs more than 20% performance degradation.

![Fig. 1: Performance Impact for each cache way-disabling configuration (x-axis does not show all points to be legible, inset shows x-axis for configurations for which no benchmark suffers more than 20% performance degradation).](image-url)
configurations that are simulated for an application and used as training dataset to derive the values for the microarchitectural parameters (e.g., cache misses) which are then used by an analytical model to predict the performance of the application for any of the remaining possible way-disabling configurations. Thus, this approach can reduce drastically the number of time-consuming simulations.

An overview of the proposed framework is given in Figure 2. A selection step divides the configurations into, i) those to will be simulated and used as training dataset to feed the analytical model, and ii) those to be predicted using the analytical model. The training configurations are simulated to collect different micro-architectural statistics that feed into the analytical-model which determines the performance impact for the remaining way-disabling configurations (predicted configurations). The computational benefits of INTERPLAY depend on the size of its training set. As we show next, it can be quite small which helps to drastically reduce the time spent on simulations.

At design-time, a designer can use INTERPLAY to quickly produce a similar analysis to that in Figure 1, to determine which way-disabling configurations can cause unacceptable large performance degradation (PD) and should flag a field return. The PD threshold can be defined by the designer, based on the application and its requirements. The effectiveness of INTERPLAY is shown in Figure 1 with red points that indicate the largest degradation predicted by INTERPLAY per way-disabling configuration: it is virtually an exact match with the actual simulation results. Below we explain the workings of INTERPLAY.

III. ANALYTICAL MODEL FOR PERFORMANCE DEGRADATION PREDICTION

This Section describes the models used by INTERPLAY to predict the performance degradation due to multi-cache way-disabling. An example cache hierarchy used to describe INTERPLAY’s models is shown in Figure 3(a). We use this example as a point of reference to present the proposed model, which can be generalized for other configurations and types of caches. In this specific case, the hierarchy has two-levels, the level-one or high-level caches consisting of a 4-way instruction cache (IL1$) and a 4-way data cache (DL1$), and the low-level cache, in this case, an 8-way unified cache (L2$). All caches are connected with their representative Miss Status Handling Register (mshr) to track outstanding cache misses.

A. Training Configurations Selection

One of the main contributions of this paper is the appropriate selection of the training configurations. We keep the set of training configurations small, to reduce the time complexity, but yet sufficient to predict accurately the performance degradation for all the remaining configurations. We select for training the baseline configuration (i.e., without any fault and disabled ways) and all the single-cache way-disabling configurations (i.e., with fault(s) in a single cache). All the remaining multi-cache way-disabling configurations can be predicted by our model. To illustrate, consider the processor in Figure 3(a) and assume we want to predict the performance of a multi-cache way-disabling configuration with remaining 3-way IL1$, 2-way DL1$ and 7-way L2$ shown in Figure 3(c). Our model will use statistics from the baseline simulation.
(Figure 3(a)) plus the three corresponding single-cache way-disabling simulations (Figure 3(b)), each having the same number of ways disabled as in the multi-cache way-disabling configuration but for a single-cache at a time i.e., remaining ways: (i) 4-way IL1$, 4-way DL1$ and 7-way L2$, (ii) 3-way IL1$, 4-way DL1$ and 8-way L2$ and (iii) 4-way IL1$, 2-way DL1$ and 8-way L2$.

As the example shows, INTERPLAY attempts to predict the performance of a multi-cache way-disabling in three caches, using the baseline configuration plus the three single-cache way-disabling configurations with the corresponding disabled ways for each individual cache. Consequently, the total number of training configurations that are needed to predict any multi-cache way-disabling configuration is equal to $1 + \sum (\#ways \text{ in cache}_i - 1), \forall \text{cache}_i$. Here, we assume that a functional processor needs to have at least one-way operational per cache. In an exhaustive simulation approach, the number of cache disabling configurations needed to be simulated in a multi-cache is equal to $\prod (\#ways\text{ in cache}_j), \forall \text{cache}_j$. Hence, our proposed framework can drastically reduce the simulation time. Note that, the exact location of disabled way(s) in a cache is irrelevant, only the # of ways disabled needs to be considered.

### B. Analytical Prediction Model

The selected training configurations are simulated for each benchmark to provide various micro-architectural statistics, such as cycles per instruction (CPI), cache misses and cache accesses, all used as input to the analytical model. Specifically, to formulate the CPI for each predicted configuration (multi-cache way-disabling configuration), we gather and use the statistics from their corresponding single-cache way-disabling training configurations and the baseline configuration. To determine the predicted CPI we combine, i) a linear CPI model ($CPI_L$) that sums the performance degradation, due to the extra cache misses, from all single-cache way-disabling configurations and ii) a CPI model ($CPI_{EM}$) that captures the degradation due to the extra cache misses in the lower-level cache (e.g L2$) as a result of the interplay between lower and higher level caches. We define the predicted CPI ($CPI_P$) for a multi-cache way-disabling configuration as:

$$CPI_P = CPI_L + CPI_{EM}$$  \hfill (1)

All the parameters used in the formulation throughout this Section are defined in Table I. Moreover, for simplicity, when we refer to misses or extra misses, we mean mshr–misses or extra mshr–misses, respectively.

### Linear CPI model ($CPI_L$):

The first objective, is to estimate $CPI_L$. Since the number of committed instructions of a benchmark run is the same for all the configurations, we replace $CPI$ with cycles $C$. Hence, we use:

$$C_L = (C_{DT} - C_B) + (C_{IT} - C_B) + (C_{L2T} - C_B) + C_B$$  \hfill (2)

This equation sums the extra cycles contributed from the three single-cache way-disabling training configurations ($C_{DT}, C_{IT}$ and $C_{L2T}$). To this end, we subtract from each training configuration cycles the cycles of the baseline configuration ($C_B$). At the end, we add to these differences the cycles of the baseline configuration to estimate the total cycles. For example, if we want to predict the CPI for a disabled L2$ with 1 remaining way, a DL1$ with 2 remaining ways and an IL1$ with 3 remaining ways, assuming a baseline configuration of L2$=8 ways, DL1$=4 ways and IL1$=4 ways, then equation(2) becomes:

$$C_L = (C_{8_2} - C_{8_4}) + (C_{8_4} - C_{8_4}) + (C_{8_4} - C_{8_4}) + C_{8_4}$$  \hfill (3)

where $8_2$ is the baseline configuration, $8_4$ is the D1 training configuration, $8_4$ is the L1 training configuration and $8_4$ is the L2 training configuration.

### CPI model due to extra cache misses in lower-level caches ($CPI_{EM}$):

The most challenging aspect of the problem we solve is capturing the interplay between the different caches in a multi-cache way-disabling configuration. Particularly, extra misses can occur in a multi-cache way-disabling configuration that do not occur either in the baseline or in the training single-cache way-disabling configurations. This is caused by the interactions between the higher-level and lower-level caches. For example, this happens when an L2$ hit in a single-cache training configuration becomes an L2$ miss in the predicted multi-cache way-disabling configuration. Such interplay is not captured by the $CPI_L$ model. Thus, we use $CPI_{EM}$ to encapsulate this behavior defined as follows: This model is defined as follows:

$$C_{EM} = EM_{L2} * Penalty_{L2}$$  \hfill (4)

, where $EM_{L2}$ are the extra misses in L2$ and $Penalty_{L2}$ is the cycle penalty per L2$ miss. $EM_{L2}$ can be estimated

| Parameters | Description |
|------------|-------------|
| $CPI_P$    | Predicted CPI |
| $CPI_{L,M}$ | CPI model for extra misses in lower-level caches |
| $C_l$      | Cycles for linear model |
| $C_{ij}$   | Cycles for a configuration $j$, where $i$ is: $B$: Baseline configuration (without disabling) $DT$: DL1S Training configuration $IT$: IL1S Training configuration $L2T$: L2S Training configuration |
| $EM_i$     | Extra misses for cache $i$, where $i$ is: $D8$: Data cache (DL1S) $I8$: Instruction cache (IL1S) $L2$: L2 cache ($L2S$) |
| $M_i$      | Misses for cache $i$ ($D8$, $I8$, $L2S$) in configuration $s$ ($D8$, $I8$, $L2S$) |
| $M_{i,j}$  | Misses for cache $i$ ($D8$, $I8$, $L2S$) derived from cache $m$ ($D8$, $I8$, $L2S$) accessses |
| $M_{i,m,j}$| Misses for cache $i$ ($D8$, $I8$, $L2S$) derived from cache $m$ ($D8$, $I8$, $L2S$) for configuration $j$ ($D8$, $I8$, $L2S$) |
| $T_M$      | Total Misses for cache $i$ ($D8$, $I8$, $L2S$) |
| $MR_{i,m}$ | Miss Rate for cache $i$ ($D8$, $I8$, $L2S$) derived from cache $m$ ($D8$, $I8$, $L2S$) accesses |
| $Penalty_{i,j}$ | Per miss penalty in cycles for cache $i$ ($D8$, $I8$, $L2S$) |
TABLE II: Processor Configuration

| Parameter description | Setting |
|-----------------------|---------|
| Pipeline depth         | 15 stages |
| Fetch/Decode/Issue/Commit | Up to 44/64/6 instructions per cycle |
| Line Predictor         | 4096 entries |
| RAS                    | 16 entries |
| Indirect Jump Predictor | 512 entries |
| Branch Predictor       | 8 KB gshare |
| Branch Resolution      | In-order |
| Prefetching            | Disabled |
| Issue Queue/Reorder buffer | 40 INT entries, 20 FP entries / 128 entries |
| L1 instruction cache (IL1S) | 4-way, 64 B blocks, LRU |
| L1 data cache (DL1S)   | 4-way, 64 B blocks, LRU |
| L2 unified cache (L2S) | 8-way, 64 B blocks, LRU |

TABLE III: Execution time in hours for the exhaustive simulation-based and INTERPLAY approaches

| Benchmark   | Simulation-Based Approach | INTERPLAY |
|-------------|---------------------------|-----------|
| astat       | 52.00                     | 5.75      |
| bwaes       | 16.00                     | 1.75      |
| bzip2       | 16.28                     | 1.78      |
| cactusADM   | 13.25                     | 1.45      |
| games       | 31.30                     | 3.42      |
| gcc         | 44.93                     | 4.91      |
| GnomeFZTD   | 27.02                     | 2.95      |
| gobmk       | 43.55                     | 4.76      |
| gromacs     | 16.02                     | 1.75      |
| lbm         | 18.33                     | 2.01      |
| leslie3d    | 12.50                     | 1.37      |
| libquantum  | 26.48                     | 2.89      |
| mcf         | 37.80                     | 4.13      |
| milc        | 25.67                     | 2.81      |
| namd        | 47.52                     | 5.19      |
| omnetpp     | 44.78                     | 4.89      |
| perlbench   | 33.12                     | 3.62      |
| sjeng       | 25.23                     | 2.76      |
| soplex      | 47.95                     | 5.24      |
| sphinx3     | 54.53                     | 5.96      |
| zeusmp      | 19.98                     | 2.19      |
| Total       | 654.85                    | 71.62     |

Using the following:

\[ EM_{L2S} = TM_{L2S} - M_{L2S} \]  \hspace{1cm} (5)

where the extra misses of L2S is the difference between the total expected L2S misses (\( TM_{L2S} \)) and the L2S misses from the training configurations for L2S (\( M_{L2S} \)). More specifically, \( TM_{L2S} \) is estimated by:

\[ TM_{L2S} = M_{L2S \rightarrow D} + M_{L2S \rightarrow I} \]  \hspace{1cm} (6)

Equation (6), aims to capture the total number of L2S misses of predicted configuration that mainly stem from two sources: 1) L2S misses caused by DL1S cache misses that access L2S (\( L2S \rightarrow D \)) and 2) L2S misses caused from IL1S cache misses that access L2S (\( L2S \rightarrow I \)). To do so, \( M_{L2S \rightarrow D} \) and \( M_{L2S \rightarrow I} \) are calculated as follows:

\[ M_{L2S \rightarrow D} = M_D * MR_{L2S \rightarrow D} \]  \hspace{1cm} (7)

where \( M_D \) are the total misses from DL1S and, \( MR_{L2S \rightarrow D} \) is the miss rate of the DL1S accesses in L2S.

\[ M_{L2S \rightarrow I} = M_I * MR_{L2S \rightarrow I} \]  \hspace{1cm} (8)

where \( M_I \) are the total misses from IL1S and, \( MR_{L2S \rightarrow I} \) is the miss rate of the IL1S accesses in L2S.

The L2S miss rates of the predicted configurations are determined from the training data provided by the simulated single-cache configuration as the ratio of the number of L2S accesses, due to higher-level cache misses, that cause miss in L2S, over the total number of L2S cache accesses due to the higher-level cache misses. Thus, the two miss rates are calculated using the following:

\[ MR_{L2S \rightarrow D} = \left\{ \begin{array}{ll} M_{L2S \rightarrow D} / M_D & \text{if } M_{L2S \rightarrow D} \geq M_{L2S \rightarrow D}, \\ M_{L2S \rightarrow D} / M_D & \text{if } M_{L2S \rightarrow D} < M_{L2S \rightarrow D}. \end{array} \right. \]  \hspace{1cm} (9)

\[ MR_{L2S \rightarrow I} = \left\{ \begin{array}{ll} M_{L2S \rightarrow I} / M_I & \text{if } M_{L2S \rightarrow I} \geq M_{L2S \rightarrow I}, \\ M_{L2S \rightarrow I} / M_I & \text{if } M_{L2S \rightarrow I} < M_{L2S \rightarrow I}. \end{array} \right. \]  \hspace{1cm} (10)

where \( M_{L2S \rightarrow D}, M_{L2S \rightarrow D} \geq M_{L2S \rightarrow D}, \text{and } M_{L2S \rightarrow D} < M_{L2S \rightarrow D}. \)

\[ M_{L2S} = (M_{L2S \rightarrow D} - M_{L2S \rightarrow D}) + (M_{L2S \rightarrow D} - M_{L2S \rightarrow D}) + (M_{L2S \rightarrow I} - M_{L2S \rightarrow I}) \]  \hspace{1cm} (11)

Finally, to estimate the miss penalty in cycles per L2S cache miss, needed in eq (4), we use the following:

\[ Penalty_{L2} = (C_{L2} - C_B) / M_{L2S \rightarrow L2T} \]  \hspace{1cm} (12)

which determines the per miss cycles in the L2S and represents the difference in clock cycles between the baseline and L2S training configurations, divided by the misses in L2S in the training configuration L2T.

IV. EXPERIMENTAL SETUP

The simulation experiments in this work were performed using the cycle accurate simulator sim-alpha for ALPHA processor [17]. The simulator is extended to support all the combinations of way disabling for all the cache levels (DL1S, IL1S, L2S) leaving at least one operational way in each cache, and to monitor all the related performance statistics. The key parameters of the simulated processor configuration are summarized in Table II. The experiments are conducted for 100M committed instructions of 21 SPEC CPU2006 benchmarks. An in-house SimPoint [18]-like tool is used to select the regions to simulate.

Two types of experimental results are reported: simulation and analytical based. The exhaustive simulation-based results are used to validate the accuracy of the proposed model. The validation compares the values obtained by simulations against the values predicted by the proposed model. The first set of results are for a processor with a 2MB L2 cache. To analyze further the model’s accuracy and highlight its generality, we have also experimented with a smaller L2 cache size of 256KB L2 that is still 8-way. For the training dataset
we use a set of 14 single-cache way-disabling configurations per benchmark and for the prediction dataset we use the set of all possible 114 multi-cache way-disabling configurations.

V. RESULTS

A. Execution time comparison of naive exhaustive simulation-based versus INTERPLAY

We first analyze the execution time for all 21 benchmarks for the two approaches, exhaustive simulation vs combined simulation and model based approach (INTERPLAY). The results are obtained when running the simulations on a Xeon server and are presented in Table III for each benchmark. The second and third column represent the execution time in hours for simulation-based approach and INTERPLAY approach, respectively. As it can be seen in Table III, INTERPLAY approach is around 9.2 times faster than the simulation approach. It is useful to note that this value matches the ratio 128/14 which corresponds to the total number of multi-cache way-disabling configurations over the INTERPLAY training configurations.

B. Model-Based Approach Accuracy Results

We evaluate the accuracy of the proposed predicting model for CPI_P, that includes both CPI_L and CPI_EM. We also present results for CPI_L alone, to highlight the need for both models. For these results we use CPI and we present the accuracy of the model in terms of percentage error. The error quantifies the difference of the proposed model with the actual exhaustive simulation results. Figures 4(a)-(b) show the CPI predicted (x-axis) versus the actual CPI (y-axis), as well as, the error in percentage (secondary y-axis) for CPI_L and CPI_P, respectively, per benchmark and cache way-disabling configuration. In order to quantify the accuracy of our model we set-up a 5% threshold as a maximum permissible error. Thus, error values that are above +5% or below -5% are considered as failed predictions. Consequently, the accuracy of CPI_L is 96.42% with an average error of 10% and a maximum error of 37%. On the other hand, considering the CPI_P model, as shown in Figure 4(b), we can see a prediction error decrease, giving an accuracy of 98.40% with an average error of 3% and a maximum error of 19%.

The accuracy of the performance prediction is correlated with the accuracy that L2$ misses are predicted, depicted in Figure 5 which shows the predicted L2$ misses (x-axis) estimated using eq. 7, the actual L2$ misses (y-axis) and the error on the secondary y-axis. Figure 5 clearly demonstrates that in most of the cases where we experience a larger prediction error, the actual number of L2$ misses is relatively small (see 0-100K misses in Figure 5), which means that the overall impact on performance will be negligible. Furthermore, we investigated the prediction accuracy using different thresholds and the results show an accuracy of 92.96% with 2% error threshold and 88.09% with 1% error threshold for the CPI_P model versus 89.88% with 2% error threshold and 81.13% with 1% error threshold for the CPI_L model. This clearly demonstrates the need for the CPI_P model, which considers the interplay between lower-level and higher-level caches.

To further demonstrate the effectiveness of the model we also analyze INTERPLAY with smaller L2$ cache which can cause a higher number of L2$ misses. Figures 6(a)-(b) show the CPI prediction with a 256KB L2$ for the CPI_L model and the CPI_P models, respectively. As it can be seen in Figure 6(a), the prediction error in model CPI_L increases considerably in the case of the smaller cache (compared with Figure 4(a)). However, when model CPI_P is used (Figure 6(b)), the prediction error remains small, similar to that in the
larger cache (Figure 4(b)). In particular, $CPI_P$ for the smaller cache provides an accuracy of 96.8%.

Finally, we investigated all the cases that have a prediction error above 5% and we determined that the $CPI_P$ fails when extra L2$S$ misses cause other misses. We call these secondary misses, and by analyzing them a bit further, we found out that when a benchmark has high reuseness on specific cache blocks and these cache blocks are replaced regularly by other blocks due to the small capacity of the cache (due to cache-way disabling), then this can result in secondary misses on the frequently accessed blocks, that our current approach cannot predict.

VI. CONCLUSIONS AND FUTURE WORK

This paper proposes INTERPLAY framework that uses a small set of single-cache way-disabling simulations as training configurations for an analytical model to predict the performance of multi-cache way-disabling configurations. Some key novelty of the work is the intelligent selection of the training configurations that consist of single-cache way disabling configurations and a model that predicts the extra misses caused by the interaction of higher and lower level caches when both caches, have some ways disabled. The framework has several uses. One of them is to use it at design time to help designers leverage trade-offs between performance degradation and number of field returns.

Future work will extend INTERPLAY to a three level cache hierarchy, multicore processors and other replacement policies. Moreover, we will quantify the performance degradation while taking into account lifetime reliability. Finally, we aspire to augment the proposed model to handle cache disabling at the finer granularity of a cache line.

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