Recent progress in CMOS RF circuit design

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Abstract: This paper reviews recent progress in CMOS RF circuits with respect to technology scaling. It turns out that RF transceivers almost ideally scale with technologies, even though some of RF circuits do not obey scaling law due to the noise, linearity, matching, and output power constraints. In order to overcome these constraints many design techniques including all digital approach, digital assisted approach, noise cancelling, non-linearity canceling, and RF filtering have been introduced. Also remaining challenges for the future is discussed.

Keywords: CMOS, RF, all-digital PLL, all-digital TX, noise cancelling, non-linearity cancelling

Classification: Integrated circuits

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1 Introduction

Since the invention of analog cellular in 1970’s, the market of wireless communication has developed rapidly mainly due to the ubiquitous nature of wireless devices [1]. The data rate has increased by more than thousand times during last 20 years, as shown in Fig. 1 [2, 3, 4, 5]. This is realized by increasing channel bandwidth and employing complex modulation scheme so as to increase the number of bits per symbol. In order to accomplish above, cost and power efficiency of both digital and RF/analog signal processing have been enhanced drastically.

Although many system and circuit level techniques have been developed for digital circuits, the benefit of CMOS technology scaling has given major part of its efficiency enhancement. Even though the performance of RF circuits can benefit from the technology scaling, RF circuits do not benefit as much as digital circuits do [6]. This is mainly because their area and power efficiency is limited by the noise, matching, and linearity of active and passive devices. Some of those factors, such as thermal noise, matching, and occupied area of active devices improve slightly with the technology scaling. However factors such as occupied area of passive device and linearity of the active device usually do not improve or even deteriorated with the technology scaling [6]. Also, the output power requirements, which apply to a power amplifier, make scaling difficult due to the smaller breakdown voltage in scaled technology. In order to bridge the gap of enhancements...
given by the technology scaling between digital and RF, many circuit design techniques have been developed. This paper reviews these CMOS RF circuit design techniques and how much performance improvement has been made. Circuit design techniques for very high frequency, such as millimeter wave (> 60 GHz) is the out of the scope of this paper, as they require different types of circuit design techniques.

This paper is organized as follows. In the next section, the performance trend of RF wireless transceivers is analyzed to see how much improvement has been achieved. In section three, RF circuit design techniques which tackled the above challenges such as noise, matching, occupied area, and linearity are explained. Then remaining challenges are discussed, which is followed by a conclusion.

2 Trends of RF transceiver performance

Cellular standards have the longest history, however its modulation scheme is so different between generations and it is very difficult to normalize the performance to see how overall performance has been improved. For this purpose IEEE 802.11 standards, which are known as wireless LAN (WLAN), are more suitable, since they have been using similar modulation schemes.

The trends of normalized area per transceiver (TRx) and technology node are shown in Fig. 2 [7, 8, 9, 10, 11, 12, 13, 14, 15, 16]. Please note that WLAN employs multiple-input multiple-output (MIMO) technology [13], and multiple transceivers are implemented in one chip. The normalized transceiver area stands for the estimated area per transceiver. As the technology scaled to almost one-fifth (from 250 nm to 45 nm) during last 12 years, the normalized area scaled to $1/22 = 1/4.7^2$. This is amazingly almost the same as the expected improvement of the scaling law. Moreover, considering the larger bandwidth is required for recent specifications and some of the building blocks such as analog-to-digital converter (ADC) and power amplifier are newly included in the transceiver, the effective improvement is perhaps more than expected by the scaling law.
Fig. 2. The trends of normalized transceiver die area, receiver power consumption and technology node

The trend of receiver power consumption is also shown in Fig. 2. Receivers are chosen for the comparison since transmitters have different output power level, which is the major factor for the transmitter’s power consumption. The receiver’s power consumption is scaled to about one tenth during last 8 years. We now understand that the tremendous efforts have been made so that the ratio between RF/analog and digital in terms of cost and power consumption is kept almost constant. This has been enabled the scaling of entire IC and system performance.

### 3 RF circuit design techniques

Before going into the detail of circuit design techniques, challenges for each circuit building block are explained. Fig. 3 shows a block diagram of a typical direct conversion transceiver, which is a cost-effective transceiver system and is often used in WLAN and cellular standards. The transceiver is consisted of three parts, which are transmitter (TX), receiver (RX), and local oscillator (LO). In the transmitter, digital data is converted to analog by digital-to-analog converters (DACs) (not shown in Fig. 3). The analog signal is applied from the digital baseband to low-pass filters (LPF) to reject aliasing
signals. Then, the LPF output or the baseband signal is up-converted to RF by mixers, which is followed by a driver amplifier (DA) and power amplifier (PA) in order to provide sufficient power to transmit signal to a distant receiver. In RX, signal received at antenna is first amplified by a low-noise amplifier (LNA), whose output is then down-converted by mixers. The signal goes through LPF and gain controlled amplifier in order to reject interferer and amplify signal to the input range of ADC. LO generates frequencies for down and up conversions.

In this paper, we focus on RF building blocks, which are challenging part of the transceiver and colored in blue in Fig. 3. The challenges in LO is that the die area for loop filter is huge. In addition, the phase noise of phase-locked loop (PLL)/oscillator is very important for entire transceiver performance and needs to be improved for higher data rates. Challenges for RF part of the receiver include noise and linearity. Also, matching is a critical issue to achieve better 2nd order input-referred intercept point (IIP2) [17], otherwise strong modulated interferer would desensitize the receiver. The Up-conversion mixers, driver amplifier, and power amplifier compose the transmitter, where linearity is the main challenge. Power consumption is a common issue for all building blocks. Among them, power amplifiers (PAs) must produce sufficient output power to transmit signals to a receiver. PAs generally consumes the largest power and reducing power consumption is a critical challenge. In addition to this, minimizing the occupied area for a PA is a difficult challenge, since high voltage devices to deal with high supply voltage are required for power efficient PA [18].

In the remaining part of this chapter, recent circuit techniques for these building blocks are introduced with the emphasis on how above challenges are tackled.
3.1 All-digital PLL (ADPLL)

The word of “all” in ADPLL is a little bit confusing as it is not truly “all” digital. Nevertheless, we see that almost all portion of the PLL is digitized when it is compared with the analog counterpart. Fig. 4 shows the block diagram of a conventional analog PLL and ADPLL [19]. The ADPLL takes advantage of the fast signal transition in a scaled CMOS technology. The phase data generator (PDG) detects the phase difference in digital domain. This can be done using time-to-digital converter (TDC) which converts the analog phase information into the digital information of the number of delay unit (e.g. inverter). The delay per a unit can be several tens of psec in sub-100 nm CMOS technology. The obtained phase information is compared with reference generated from frequency control word (FCW) and its output is applied to the digital loop filter. The usage of the digital loop filter is one of the largest advantages of this architecture, since its area and power are scaled with technology.

A digitally controlled oscillator (DCO) equips discrete variable capacitors so that the output of the filter directly controls the frequency as shown in Fig. 5 [19]. The number of the capacitor \( C_k \) connected to the oscillator core is controlled digitally through the switches \( S_k \). The frequency step,
which corresponds to the discrete capacitance, is designed to be small enough so that the quantization noise is smaller than the voltage controlled oscillator (VCO) noise and negligible. Finer resolution can be obtained with ΔΣ modulator [20]. Now the phase noise can be optimized regarding various parameters in ADPLL and VCO because phase difference in each comparison, which represents the phase noise, can be measured and recorded in the digital domain. Similarly, accurate optimization and calibration of performances, including loop bandwidth, and spurious is also possible [21].

3.2 Oscillators

LC-oscillators are often used in RF transceivers to satisfy stringent noise requirement. Recent progress in LC-oscillators is in its bias scheme, that is, the idea of class used in a power amplifier is now applied. Fig. 6 shows the schematics of conventional and class-C oscillator [22]. The conventional oscillator is biased such that the transistors are always on. This is similar to a class-A amplifier, where the transistor is on for its entire period. The classical classification of the amplifier class can be also applied to oscillators and class-C oscillator is introduced in [22] (Fig. 6 (b)). The transistor is on for less than its half of the period due to the reduced bias voltage. Smaller overlap between voltage across the transistor and drain current contributes to the better power-noise trade-off. Similarly, more efficient switching amplifiers of class-D and class-F are applied to oscillators in [23] and [24], respectively.

3.3 LNA and down-conversion mixer

One of the systematic approaches to greatly relax the linearity requirement for each building block is introducing RF channel selection, whose conceptual block diagram is shown in Fig. 7. Conventionally, channel selection is done in baseband (both in analog and digital) as it requires steep cutoff, and required Q for RF filtering is unfeasible. To overcome this issue, frequency translational loop is proposed as shown in Fig. 7 (b) [25]. Rejecting strong interferer
Fig. 7. (a) Simplified conceptual block diagram of RF channel selection and (b) its implementation

Fig. 8. (a) Noise cancelling LNA and (b) noise cancelling receiver

after the LNA relaxes the linearity requirements for mixer and succeeding blocks greatly, resulting in small occupied area and power consumption. In [26], same circuit topology is employed for the LNA and the feedback amplifier so that the non-linearity of LNA is partly canceled by the nonlinearity of the feedback amplifier. Note that the cancellation cannot be perfect since the operating frequency is different.

Another recent invention in the receiver side is the noise cancellation technique [27]. Fig. 8 (a) shows the principles. Input matching is realized by the input resistance (R_IN) of the common-gate (CG) transistor. The noise (V_N) of this resistance is amplified through the CG and common-source (CS) transistors. For the CG path, the noise current is negative and the CG does not change the polarity, therefore the resulting output noise of the CG path has negative polarity in terms of V_N. The output of the CS also has negative polarity since the CS is an inverting amplifier. As a result, if the gain between the CS path and the CG path matches, the noise of the input resistance R_IN is cancelled at the output. This idea is expanded such that the noise of a passive mixer and baseband is cancelled and is beautifully implemented in [28] (Fig. 8 (b)). Here, the noise V_N,main represents the noise at the input
Fig. 9. (a) Mixer with digital offset correction, (b) Offset cancelation for a simple differential pair

of the main path, including the mixer and baseband. Note that the noise of the mixer and baseband is up-converted by the passive mixer (the red arrow in Fig. 8 (b)). Considering the main and the AUX paths correspond to the CG and the CS paths in Fig. 8 (a), respectively, $V_{N,\text{main}}$ is cancelled if the gain of both paths are the same (shown in blue arrows in Fig. 8 (b)). The overall noise performance is dominated by the auxiliary path, which is small as there is a gain ($g_m$) in front. In addition to the noise cancellation, good linearity is achieved since there is no voltage gain before the trans-impedance amplifier (TIA). Note that after the TIA, interferer is filtered and the linearity requirement is relaxed.

The matching requirement was critical to RF transceivers since large device size and thus large area and cost are consumed to obtain better matching, since the matching performance is linearly related to the square root of the device area. This problem had to be solved, otherwise occupied area would not scale with the technology. Matching requirement is especially severe in RX mixers so as to achieve excellent IIP2 performance [18]. IQ mismatch and LO feed through are also issues for both RX and TX mixers. Fig. 9 (a) shows the mixer with digital offset correction. During the calibration, test tones are applied to mixers and resultant IIP2 product is detected after the ADC. The digital controller adjusts the input offsets of the mixer through the DACs so as to minimize the IIP2 product. For the case of simple differential pair, the DAC can be implemented as a current source of the differential pair, for example, as shown in Fig. 9 (b).

One more technique worth mentioning here is utilizing passive mixers for filtering and frequency conversion at the same time [29]. With a switched capacitor form shown in Fig. 10 (a), the mixer samples almost the same value in each LO cycle and does not produce output if the input frequency is close enough to the harmonics of the LO frequency. Also the passive mixers can up-convert or down-convert the input impedance from baseband (BB) to RF or from RF to BB as shown in Fig. 10 (b). This feature is utilized as an RF filtering functionality in [30]. The interferer rejection is so important and greatly improves the transceiver performance. Therefore these techniques are
3.4 Up-conversion mixer, driver amplifier (DA), and power amplifier (PA)

On the transmitter side, one of the progresses is to bring the amplifier chain into the digital domain. This idea is sometime called digital PA (DPA) or RF-DAC, contributing area efficient implementation especially the output power level is not so high (e.g. less than 10 dBm) [19]. The conceptual block diagram is shown in Fig. 11 (a). Similar to the DCO explained in section 3.1, the amplitude is represented by the number of activated amplifier unit, which is controlled by the amplitude code. The circuit implementation example is shown in Fig. 11 (b), where EN is activated depending on the amplitude code through a decoder. As in [19], the phase modulated signal generated by the ADPLL is applied to the DPA. Almost all building blocks belong to the digital domain, as shown in Fig. 12.

There are several issues in the all-digital approach. Since the input and output capacitance depends on the number of activated units, the output phase depends on the amplitude code and thus amplitude-to-phase (AM-PM) conversion is observed. In order to overcome the issue, phase constant DPA is proposed in [32]. When the output signal swing is large, output swing...
Fig. 13. Block diagram for digital pre-distortion (DPD)

is not proportional to the amplitude code. This problem can be alleviated by adopting digital pre-distortion (DPD) at the cost of power and die area [33]. The conceptual block diagram of the DPD is shown in Fig. 13. Note that Fig. 13 describes DPD for a conventional analog transmitter. However this concept can be applied to an all-digital TX by pre-distorting amplitude and frequency information in digital baseband. In the digital baseband, the pre-distorted signal is produced so that the linear response is obtained after the PA. In order to track the linearity drift due to the PVT variations, an adaptive feedback can be employed [34] (not shown in Fig. 13).

Other serious issues are the out-of-band noise and aliasing, which can be critical especially for cellular application. Employing high sampling frequency can reduce the effects at the cost of high power consumption. The modulation accuracy with small output power might be also an issue. Considering these trade-offs, the choice between the digital approach and conventional analog approach can be made. For example, wireless personal area network (WPAN) standards have relatively relaxed specification and smaller output power. Therefore the digital approach tends to be more cost effective. On the other hand, cellular standards have stringent requirements and the usage of digital approach can be limited.

3.5 High power amplifier (PA)

For a PA with more than +20 dBm output power, the power efficiency is critical to the entire transceiver and the battery life of a mobile device. The PA can also be implemented as an all-digital TX [33]. However it seems conventional analog approach is more suitable, since in addition to the trade-offs explained in section 3.3, there are issues for an all-digital TX to be applied to high power amplifier. Many long wires are required for the all-digital TX, as the total gate width can be larger than 10 mm. This can prevent from an optimal layout, which is very important for a high power amplifier. Also, mismatch in wire length can cause phase and amplitude mismatch between PA units, which deteriorates the quality of modulated signal and power efficiency. Instead of employing all-digital approach, a multi-band and multi-mode PA is developed in order to overcome the challenge of area reduction. Total occupied area for PAs has been reduced by sharing a PA with different frequency bands and standards. An octave range and multi-mode power amplifier is developed by employing transformer at the output [35].
In addition to the area reduction, many efficiency improvement techniques have been proposed. Many of techniques improve linearity, so that the operating point of a PA is close to its maximum output efficiency and maximum output power. One strong candidate is DPD with adaptive feedback [34], at the cost of area and power. PA-closed loop is proposed as an analog approach to improve linearity more efficiently [36]. A conventional feedback loops have large group delay and thus small loop bandwidth as shown in Fig. 14 (a). On the other hand, the polar loop within the PA has smaller group delay and its loop bandwidth is large enough for WCDMA standard (Fig. 14 (b)). Also additional die area and power consumption for the loop can be minimized. Please note that even with this analog approach, digital calibration is essential to the performance.

4 Challenges for the future

One obvious challenge is to keep up the scaling trend. Although the transistor will be faster, the supply will be less than 1 V and more RF and analog circuits have to be moved into the digital domain. Demands for low-power and low-supply operation are emerging for applications such as sensor network. The power has to be reduced down to $\mu$W level, which is more than thousand times smaller than the current major RF applications of cellular and WLAN. Although duty cycling technique is proposed to trade between data rate and power consumption, fundamental figure of merit such as energy per bit must be improved in $\mu$W-level systems [37]. Also, supply can be around 0.5 V for applications with solar cells. There are many researches for RF building blocks [38], however only few paper describes entire transceiver operating at $< 0.5$ V supply [39]. On the other hand, design of efficient power amplifier has been and will be challenging, as the complex modulation scheme will be used in the future.

Recently, many wireless standards including cellular, WLAN, Bluetooth, GPS, FM, TV, and NFC are integrated in a mobile device. Thanks to the technology scaling, multi-mode (2G/3G/4G) transceiver for cellular application [40] and combo-chip for WLAN/Bluetooth/GPS/FM [41] was commercialized to keep the device size small. However, RF front-end, such as PA, switches, filters and antennas are more difficult to scale. The circuit design techniques to make these devices smaller, shared, or unnecessary have been...
important and will be important in the future. For example, SAW filters in
the transceiver of 2G standard has been eliminated by improving the trans-
mitter noise performance. Non-linearity cancelling utilizing adaptive filter
lenders bulky surface acoustic wave (SAW) filter in the receiver unneces-
sary [42]. Another example is regarding an antenna. Recent antennas have
poor VSWR as they have to be wideband and they are designed as a part
of the mobile device to reduce size. Moreover, its performance drifts when
we hold the phone [43]. Antenna impedance control is now being adopted
in high performance smart phones. In the future more effective solution of
antenna impedance detection and tuning will be important to improve power
efficiency [44].

5 Conclusions

This paper reviewed the progress of CMOS RF transceivers and CMOS RF
circuit design techniques. RF circuits themselves do not scale as much as the
scaling law, due to the noise, linearity, matching, and output power require-
ments. However the occupied die area per RF transceiver is almost ideally
scaled with technology thanks to many newly proposed design techniques.
The all-digital approach is one of the most important techniques which con-
tributed the scaling. Also, the digital assisted approach including tuning and
 calibration is essential. We reviewed innovative techniques of noise and non-
linearity cancelling. The RF filtering with a passive mixer and a switched
 capacitor is so powerful and will be widely used in the future. Other than
keeping up with the technology scaling, future challenges exist in the area of
low-power and low-voltage transceivers. On the other hand, the efficiency im-
provement of power hungry high-power PAs will be also important for a long
battery life. Another challenge lies in the RF frontend. Circuit techniques
to reduce the role of RF frontend should be proposed, such that the RF
frontends can deal with many wireless standards within the limited mobile
device size.

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