Low Noise Amplifier Design and Performance Analysis of RF Front-End for Narrow Band Receivers

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Abstract: - This manuscript presents the low noise amplifier design and performance analysis of receiver RF front-end for narrowband wireless communications. The LNA is a central building block of the wireless receiver. A single-ended cascode CMOS LNA is purposeful for reconfigurable applications such as Wireless LAN. The scope of this manuscript is to design an LNA appropriate for wireless applications with improved performance metrics. The contributions of this paper are noise reduction and high gain using an inductive degeneration common source stage. The proposed LNA espouses the entire simulation results in the frequency band of 2.4 GHz. The excellent Noise Figure obtained as 0.95 dB; the preferable power gain (S21) is 17 dB, also the results of P-1dB of -17.3 dBm, IIP3 of -10.7 dBm at 2.44GHz, respectively. However, the perfect input and output matching network is achieved with proper reverse shielding and excellent stability.

Key words— CMOS, receiver RF front-end, LNA, narrow band, wireless LAN, common-source stage, inductive degeneration.

I. Introduction

In the simple front-end of radio-frequency (RF) receivers, the low-noise amplifier (LNA) is the critical discriminating component [1]. In radio communications systems, electronics equipment and medical instruments, LNAs are found. The primary function of LNA is to provide increased voltage gain, input output impedance matching with allowable noise figure and linearity of the receiver front-end. [2].

The wireless communication engineering is at this time experiencing remarkable expansion. Many exhaustive kinds of research on CMOS radiofrequency front-end circuits have been carried out in response to the requirements for a less expensive but high-performance device [3]. To design the circuit of RF front-end for high-speed wireless applications, different architectures of LNA have to be studied, keeping in view the following requirements [4]:

The LNA must be able to offer adequate amplification, but it should not be greater such that the next stages are saturated. It should introduce small amounts of external noise into the device. It should also be linear enough to conform to high-power interferences coming from the wireless interface. For communication systems, the LNA role is used to amplify poor signals received by an antenna. It is located far closer to the aerial, so that feed line losses are less critical [5].
II. Design consideration of LNA

A trade-off between design parameters is always available in analog circuits, such as conversion gain, noise, linearity, supply voltage, power consumption, etc. Degradation is observed in one parameter, while enhancement is bringing into being in another [9]. Therefore, we concentrate on the trade-off issues while retaining the optimum improvements in parameters by incorporating different technologies. The circuits proposed are designed for low noise, high linearity, increased conversion gain, low-power, depending on the context and application. Without fading specific parameters, including linearity and noise, increasing the changeable conversion gain enhances the multifunctionality of the device [10].

Any LNA circuit’s universal topology can consist of three stages shown in Fig. 1. These are an input side matching network, a central amplifier and a matching network at output [11]. This network will try to preserve resemblance in order to get better design results. The input reflection coefficient $S_{11}$ and output reflection coefficient $S_{22}$ are calculated by $s$-parameters [8].

![Fig. 1 The universal topology of LNA](image)

In this figure, the matching network of LNA are characterized by the means of lumped parameters (e.g., $Z_{in}$, $Z_{out}$, etc.) & $s$-parameters (e.g., $S_{11}$, $S_{12}$, $S_{21}$, and $S_{22}$) [6].

Using $s$-parameters, the reliability of the two-port network is examined. The Rollet factor $K_f > 1$ and alternate stability factor $B_{1f} < 1$ are necessary and adequate conditions for stability [7].

\[
K_f = \frac{(1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2)}{(2|S_{12}S_{21}|^2)}
\]

(1)

\[
|B_{1f}| = 1 + |S_{11}|^2 - |S_{22}|^2 - \Delta
\]

(2)

Where

\[
\Delta = (S_{11}S_{22} - S_{12}S_{21})
\]

If $K_f > 1$ & $B_{1f} < 1$, hence, it is unconditionally stable network.

We may describe the both transistor DC gains individually (respectively in common source and common gate configurations) as.

\[
A_o = -\frac{g_{meq}}{g_{oeq}} = -\frac{g_{m1}(g_{m2} + g_{o2})}{g_{o1} + g_{m2} + g_{o2}} \times \frac{g_{o1} + g_{m2} + g_{o2}}{g_{o1}g_{o2}}
\]

\[
A_o = -\frac{g_{m1}(g_{m2} + g_{o2})}{g_{o1}g_{o2}}
\]

\[
A_o = -\frac{g_{m1}}{g_{o1}} \quad \text{and} \quad A_o^2 = 1 + \frac{g_{m2}}{g_{o2}}
\]

\[
A_o = A_{o1} \times A_{o2}
\]

(3)
III. Design of Proposed LNA

The schematic of Inductor degenerate common source LNA topology and its test bench circuits are shown in Figure 2. Here, gate and source inductors are used to match the impedance at the desired frequency. First of all, the requirements for input matching are met by assigning an inductor $L_g$ at the gate of the MOS-FET transistor, which makes resonance at the center frequency [12]. An inductor $L_s$ is located at the source terminal to understand low NF in a given structure; it acts as source inductive degeneration. The components $L_g$, $C_{gd}$, and $L_s$ thereby afford the appropriate input network matching for narrow-band. The component $L_d$, and $C_d$ are required to resonating with a particular frequency at the output-side. The aspect ratio of MOSFET $M_1$ and $M_2$ decides the gain of the design. The value of drain inductor with a load capacitor is to set such that to resonance at desired frequency will improve gain and output matching. Here $C_{block}$ and $C_L$ are DC coupling capacitors at input and output, respectively [13].

The signal runs through the gate of the both $M_1$ transistor and $M_2$ transistor. Here, we set to $V_{ref}$ for biasing of $M_2$ transistor, so both transistors are operating in saturation mode. Hence, The $M_1$ transistor works as a common-source, while the $M_2$ transistor operates in the common-gate for isolating the output from input nodes [8].

![Fig. 2(a) proposed single-ended LNA design](image_url)
IV. Results and Discussions

The LNA circuit’s design parameters are evaluated with respect to the 2.44GHz operating frequency. Figure 3 to Figure 7 displays a plot of the s-parameters and necessary constraints. The S$_{21}$ plot is significant, as it gives the amplifier's gain. As shown in Figure 3, a gain of 17dB is achieved at 2.44GHz which falls true within our preferred range.

![Graph showing voltage gain versus frequency](image)

Fig. 3 The plot of voltage gain versus frequency is measured as 17dB at 2.44GHz.

Noise Figure is a measure of how much an amplifier degrades the signal-noise-ratio (SNR). The value of the noise figure is 0.95dB @ 2.44GHz which is a very good number shown in Figure 4.
Fig. 4 The plot of noise figure versus frequency is measured as 0.95dB at 2.44GHz.

Figure 5 shows a plot of the input output reflection coefficients $S_{11}$ and $S_{22}$. The values are -42.3 dB and –42.3dB respectively for the input and output sides.

Fig. 5: Simulated input return loss $S_{11} = -8.4\text{dB} @ 2.44\text{GHz}$ centre frequency

1-dB compression point is the input signal level that drives the small-signal gain to drop by 1dB. It is obtained as -17.3dBm at a 2.44GHz frequency as shown in Figure 6.

Fig. 6 The plot of 1-dB compression point measured as -17.3dBm

The corruption of signals relating to the intermodulation of two nearby interferers in the third order is so prevalent and so important that a performance metric was defined to characterise their behaviour called the 3rd order input intercept point (IIP3) which is shown in Fig. 7. It is obtained as -10.7dBm at a frequency of 2.44GHz.
A report on comparative studies taken in regards to directions for proposed work could tabulate in Table 1.

Table 1: Comparative analysis of proposed LNA to reported LNAs

| Parameters                  | This work   | (2)     | (4)     | (5)     |
|-----------------------------|-------------|---------|---------|---------|
| Center Frequency (GHz)      | 2.44GHz     | 2.4GHz  | 2GHz    | 2.4GHz  |
| CMOS Technology (nm)        | 180nm       | 180nm   | 180nm   | 180nm   |
| Voltage Gain (dB)           | 17dB        | 14.4dB  | 9.7dB   | 15.9dB  |
| Noise Figure (dB)           | 0.95dB      | 2.95dB  | 3.4dB   | 1.8dB   |
| $S_{11}$ (dB)               | -42.1       | -16     | -17     | -14     |
| $S_{22}$ (dB)               | -42.2       | -19     | -19     | -12.8   |
| $IIP_3$ (dBm)               | -10.7dBm    | 4.46dBm | -20dBm  | -30dBm  |
| $P_{1dB}$ (dBm)             | -17.3dBm    | --      | -6.22dBm| -12dBm  |
| Power supply                | 1.8V        | 1.8V    | 1.8V    | 1.8V    |

V. Conclusion

In the present scenario, the field of receiver for wireless communications has experienced tremendous progress, moving rapidly over a series of generations. The low-noise receiver architecture is a key design constraint. The architecture of the LNA for improved performance is of tremendous significance in this context. For this model, the inductive degeneration network has chosen a low NF of 0.95dB and a high power gain of 17dB and adequate linearity. This LNA designed can therefore be used at the center frequency of 2.44 GHz for wireless receiver applications such as wireless LAN.

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