Low latency protocol for transmission of measurement data from FPGA to Linux computer via 10 Gbps Ethernet link

Wojciech M. Zabolotny

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Institute of Electronic Systems, Warsaw University of Technology
ul. Nowowiejska 15/19, 00-665 Warszawa, Poland
E-mail: wzab@ise.pw.edu.pl

ABSTRACT: This paper presents FADE-10G – an integrated solution for modern multichannel measurement systems, aimed on low latency, reliable transmission of measurement data from FPGA based front-end electronic boards (FEBs) to computer based node in the Data Acquisition System (DAQ), using standard Ethernet 1 Gbps or 10 Gbps link. Additionally to transmission of data, the system allows to reliably send simple control commands from DAQ to FEB and receive responses. The aim of the work is to provide possibly simple base solution which can be adapted by the end user to his or her particular needs. Therefore emphasis is put on minimal consumption of FPGA resources in FEB and minimal CPU load in the DAQ computer. The open source implementation of the FPGA IP core and Linux kernel driver under permissive license facilitates modifications and reuse of the solution.

The system has been successfully tested in real hardware, both with 1 Gbps and 10 Gbps links.

KEYWORDS: FPGA, Ethernet, Ethernet Protocol, Data Acquisition, Measurement System.

*Corresponding author.
## 1. Introduction

In modern multichannel measurement systems it is often necessary to transfer multiple data streams from the detectors, to computers responsible for processing of data. Especially introduction of triggerless approach in the High Energy Physics (HEP) experiments ([1, 2, 3, 4]) increased demand on amount of data, which must be transferred to the Data Acquisition (DAQ) System, and therefore also number of links, which must be provided. The Front End Boards (FEB) are typically built using the FPGA chips, which nowadays are usually equipped with various high speed transceivers, allowing to implement broad range of different high speed interfaces [5, 6]. Selecting the appropriate solution, we must take into account additional requirements like length of the link, which in some experiments may reach even a few hundreds of meters (e.g. [7]) and electrical isolation (so optical fiber is preferred). To reduce the total cost of implementation of multiple links, it is
desirable to use a standard interface, with price reduced due to mass production of transceivers and other components of link infrastructure.

Considering the mentioned requirements, it seems, that the Ethernet link, using the SFP or SFP+ optical transceivers is the optimal solution. Broad use of Ethernet technology resulted in significant reduction of prices of components (namely SFP+ transceivers) needed to implement the 10 Gbps Ethernet link both on the computer side and on the FPGA side. The achievable price of optical 10 Gbps SFP+ transceiver is ca. $85 for single channel, and it can be further reduced when ordering a bigger batch, or when using 4 channel QSFP+ transceivers (price ca. $280 for four channels).

1.1 Required functionality of the transmission system

Because the aim of the work is to create a minimal, but extensible solution, an essential task is to define requirements, which should be fulfilled by such a system.

- Possibility to work with 1 Gbps (for price sensitive applications) and 10 Gbps (for typical applications) Ethernet links
- Reliable transport of data stream with maximal throughput and minimal latency (because the latency directly affects amount of memory needed to buffer transmitted but not confirmed yet data).
- Possibility to control FEBs and to check their status from the DAQ side of the link (even though in typical DAQ systems there is yet another, separate communication channel for configuration and diagnostics of FEBs).
- Open source implementation, which may be modified to suit needs of particular experiment.
- Ability to work with different PHY interfaces (copper, optical), depending on needs of the particular experiment.

2. State of the art

The standard solution for reliable transfer of data via Ethernet network is the TCP/IP protocol. Unfortunately this protocol has serious disadvantages, when used in FPGA. It has been optimized mainly for transport of data in wide area networks with multiple routers between communicating devices, so it contains many features related to routing of data packets, fragmenting the packets and with sharing the link bandwidth between multiple connections. The TCP/IP also assumes that data may be transported via untrusted networks, and therefore it implements sophisticated algorithms protecting the communication against malicious activity. The final result is that implementation of the full TCP/IP stack in FPGA is complex and resources hungry. Some implementations rely on a CPU implemented in FPGA or embedded in FPGA[8], but such solutions do not allow to fully utilize 10 Gbps link throughput. There are some commercial implementations of 10 Gbps hardware TCP/IP stacks for FPGA, but they are closed, and expensive solutions[8, 13].
2.1 Reduced TCP/IP developed in CERN

An interesting attempt to reduce resources consumption of the hardware based TCP/IP implementation is a solution developed in CERN and described in [11, 12]. Authors have reduced functionalities of the TCP/IP so, that it is possible to implement it in the FPGA without implementing any soft CPU core. The implementation provides only unidirectional transmission. Authors didn’t implement timestamps, selective acknowledgments and out of band data. Additionally certain mechanisms have been significantly simplified - e.g. the congestion management. This solution however still relies on the external DDR memory, used as a TCP socket buffer. Advantage of this solution is that the receiver may be a standard computer with TCP/IP stack provided by the operating system, however this solution also leads to significant CPU load – as authors state themselves “Running one 10 Gbps TCP stream can easily saturate one of the CPU cores”.

Another significant disadvantage is the closed source nature of this solution – no sources have been released, so it can not be a basis for an open, extensible solution.

2.2 Avoiding the TCP/IP complexity

To avoid implementation of complex TCP/IP stack in the FPGA and to reduce the CPU load in the receiving computer it is desirable to use a simpler protocol. Usage of the UDP protocol instead of the TCP is not optimal. The UDP protocol does not assure reliable transfer of data, so it is necessary to implement additional mechanisms ensuring reliability. At the same time the UDP protocol, and in fact all IP protocols still require significant overhead associated with routing of packets (datagrams). However the connection between FEBs and DAQ should not contain any routers, as they increase link latency, which in turn leads to increase of amount of memory needed to buffer the transmitted and not confirmed yet data.

There are two possible link topologies. In the case where Ethernet interfaces in both - FEBs and DAQ computers have the same speed, the point to point connections will be used (see Figure 1 a.). In the case where the Ethernet interface in the DAQ computer offers a higher speed (e.g. 40 Gbps), it is possible to connect a few FEBs to a single network card, via a 10 Gbps/40 Gbps switch (see Figure 1 b.). For such very simple networks, where Ethernet frames are passed either directly or via a layer 2 network switch, the best solution is to develop optimized Layer 3 protocol, using raw Ethernet frames.

2.3 Ethernet Proxy - EPRO as possible solution

The protocol and Linux kernel driver based on the above assumptions was developed in the AGH University of Science and Technology and described in [13, 14]. The proposed solution implements not only reliable transport of the data stream, but also some additional functions like different types and priorities of data, or possibility to send the same data to more than one destination. The protocol is implemented for 1 Gbps link and it uses the standard Xilinx MAC implementation. Unfortunately this solution, like the previous one, is not open. The authors did not publish sources, so it is not possible to modify it to work with higher speed 10 Gbps links, or to adjust it to the particular experiment requirements.
Figure 1. Possible topologies of Ethernet based data transmission from FEB to DAQ. a) The case where Ethernet interface speeds in FEBs and the computer are equal. b) The case where the computer offers a faster Ethernet interface.

2.4 First version of the FADE protocol

Yet another possible solution is the author’s open source FADE protocol described in [15]. This protocol provides reliable transmission of data from FPGA to a computer through 1 Gbps Ethernet links. The resources consumption in FPGA is kept at minimal level, and may be adjusted due to usage of parametrized VHDL code. Instead of complex standard MAC, simplified state machines are used to receive and send packets, which are sufficient for full duplex Ethernet links with granted link bandwidth. The initial version of the FADE protocol worked correctly with 1 Gbps links, but an attempt to simply modify the FPGA IP core for operation with 10 Gbps Ethernet PHY revealed problems with efficiency. Therefore the whole code was significantly modified. Modifications included simplification of the packets management (e.g. the concept of “sets of packets” described in [15] was dropped in favour of simple description of the data stream as a continuous sequence of packets). Another modification was addition of possibility to perform simple control and diagnostic operations via the Ethernet link, while the original FADE protocol allowed only to send START and STOP commands.

This article describes the implementation of the new version of the FADE protocol, named FADE-10G.
### Table 1. Structure of the Ethernet frames used by the FADE-10G transmission protocol.

| Source MAC | Destination MAC | Protocol version | Payload | Filler | Checksum |
|------------|-----------------|------------------|---------|--------|----------|
| 6 bytes    | 6 bytes          | 0xFADE           | 0x0100  | Payload bytes | N*0xa5   | FCS |

### 3. Implementation of the FADE-10G protocol

The FADE-10G protocol is oriented on transmission of the continuous data stream consisting of 64-bit words. To better utilize the link bandwidth, data are transmitted using the Ethernet jumbo frames in packets containing 1024 data words (8192 bytes) plus some additional information (MTU should be set to 9000 in the network interface configuration). The number of data words in a packet equal to power of two was chosen to simplify packet management both in the FPGA and in the receiving computer, as it is described later. When the transmission is stopped, the last packet may contain less data words. In such a case, the last data word contains the number of valid words in that packet (between 0 and 1023). Because the protocol is supposed to be used as the only protocol in private networks, a private, unofficial Ethertype 0xfade is used. To differentiate frames of the FADE-10G from the old FADE frames, and to allow further modifications of the protocol, the protocol version number is transmitted after the Ethertype field. This number is equal to 0x0100 in the current version\(^1\). Because the Ethernet link does not warrant reliable delivery of frames, it is necessary to implement a simple acknowledge/retransmission algorithm, which uses special shorter acknowledgement frames. Yet another short frames are necessary to allow transmission of simple control or diagnostic commands via Ethernet link. The general structure of the FADE-10G Ethernet frame is shown in Table 1 and the payload contained in frames of different types is shown in Table 2.

#### 3.1 Implementation of the protocol in the FPGA

As reliable transmission of data via an unreliable channel (like the Ethernet link) requires retransmission, it is necessary to buffer the data which have been transmitted, but are not confirmed yet by the receiving computer.

To keep the algorithm controlling the retransmission as simple as possible, the memory buffer in the FPGA has length of \( M = 2^{N_{FPGA}} \) data packets, where each data packet is 1024 words (8192 bytes) long. Thus the lower bits of the number of the data packet in the data stream may be directly used to define its position in the memory buffer. The length of this buffer also defines the transmission window of the protocol. In every moment in time only a packet from certain set of \( M \) consecutive packets may be transmitted via the link. The \( N_{FPGA} \) value may be configured before synthesis of the core and compilation of the protocol driver (described in Section 4).

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\(^1\)In the first version of the FADE protocol, this field contained type of the frame, and could be a value from the range 0x01 to 0x05, or the value 0xa5a5.
Table 2. Structure of the payload in different Ethernet frames used by the FADE-10G transmission protocol.

| Frame sequence number | Packet number in the data stream | Transmission delay | 
|-----------------------|----------------------------------|--------------------|
| 2 bytes               | 2 bytes                          | 4 bytes            |

b) User command request (from computer to FPGA)

| Command code | Command sequence number | Command argument |
|--------------|-------------------------|------------------|
| 2 bytes      | 2 bytes                 | 4 bytes          |

c) Standard data packet (from FPGA to computer)

| Frame sequence number | Packet number in data stream | Transmission delay | Command response | data |
|-----------------------|------------------------------|-------------------|------------------|------|
| 2 bytes               | 2 bytes                      | 4 bytes           | 12 bytes         | 8192 bytes |

d) Last data packet (from FPGA to computer)

| Frame sequence number | Packet number in data stream | Transmission delay | Command response | data |
|-----------------------|------------------------------|--------------------|------------------|------|
| 2 bytes               | 2 bytes                      | 4 bytes            | 12 bytes         | 8184 bytes, not all are valid |

| number of valid words |
|-----------------------|
| 8 bytes               |

e) Command response packet (from FPGA to computer)

| Filler | Command response * |
|--------|--------------------|
| 2 bytes| 12 bytes           |

* Command response field in the data packet or command response packet:

| Command code | Command sequence number | User defined return value |
|--------------|-------------------------|---------------------------|
| 2 bytes      | 2 bytes                 | 8 bytes                   |

Each packet is associated with its descriptor, shown in Figure 3.

The structure of the IP core implemented in the FPGA is shown in Figure 3. The Ethernet Receiver and Ethernet Sender blocks are simple state machines, replacing the standard Ethernet MAC. They are connected to the external Ethernet PHY or to the internal Ethernet PHY equivalent, implemented in the FPGA - like the Xilinx PCS/PMA core [16].

64-bit data words provided by the data source are written to the data packet pointed by the
Figure 2. Data packets in the FPGA memory and their descriptors shortly after start of transmission. Bit flags: V-Valid, S-Sent, C-Confirmed, F-Flushed (used when transmission is ended). The “Pkt” field - stores the 31-bit number of packet in the data stream. The “Seq” field - stores the 16-bit frame sequence number, used by the fast retransmission algorithm. The packets associated with descriptors 1 and 3 contain valid data, have been sent, but are not confirmed yet. Please note that sequence numbers are higher than packet numbers, because 3 packets were retransmitted before. The packet associated with descriptor 2 contains valid data, has been sent and is confirmed. The packet associated with descriptor 4 contains valid data, but has not been sent yet (therefore its sequence number is lower, as it is the sequence number of the packet which previously occupied this slot). Other descriptors are free, therefore their flags are cleared.

Figure 3. Structure of the FPGA IP core supporting the FADE-10G protocol.

Head pointer. When this packet is completely filled, it is marked as ready for transmission (V=1). Then the Descriptor Manager checks if it is possible to move the Head pointer to the next position. If the next position is the one pointed by the Tail pointer, it means, that the buffer is full. In this case the ready status of the core is deasserted, until the packet pointed by the Tail pointer is acknowledged, and the Tail pointer is moved to the next position.
The *Ethernet Receiver* block receives packets, checks their checksum, and writes information from correctly received packages to the *Acknowledgement and Commands FIFO* (*Ack & Cmd FIFO*). Additionally, the *Ethernet Receiver* itself executes a few high priority commands like START, STOP and RESET. The START and STOP commands are still written to the *Ack & Cmd FIFO* to ensure generation of their confirmation. The RESET command causes reset of the whole FADE-10G core, and therefore it is not confirmed at all.

The *Descriptor Manager* reads commands from the *Ack & Cmd FIFO*. If the received command is the packet acknowledge (ACK) or negative packet acknowledge (NACK) it handles it itself, as these commands are not confirmed. Other commands are passed to the *Command Processor*, which executes the command and generates their confirmation.

The packet acknowledge (ACK) command sets the C (Confirmed) flag in the descriptor of the acknowledged packet, if this packet is still kept in the buffer. If the received ACK packet contains the number of the packet bigger than the number of last transmitted packet, this situation is recognized as a protocol error.

After all commands available from the *Ack & Cmd FIFO* are executed, the *Ethernet Receiver* block tries to move the Tail pointer, freeing all packets which have the C flag set in their descriptor. All flags in descriptors of freed buffers are cleared. If after that operation there is a free place in the buffer, the ready status of the core is asserted again.

Another activity performed by the *Descriptor Manager* is the transmission and retransmission of packets. It continuously browses the packet buffer, and finds packets, which have set the V flag, but unset the C flag. Those packets are passed to the *Ethernet Sender* block for transmission or retransmission.

The last hardware block is the *Command Processor*, which may work in the same clock domain as the *Descriptor Manager*, but may also operate in another (even its own) clock domain. The *Command Processor* executes the received command, and after the result or status is ready, it builds the command response and passes it to the *Descriptor Manager*. The command response is then transmitted either in the nearest data packet, or in the dedicated command response packet, if no data packet is currently waiting for transmission or retransmission.

To avoid network congestion, the core counts transmitted data packets and retransmitted data packets and checks the ratio of those counts to verify if the network or receiving computer is not overloaded. If too high ratio of retransmitted packets is detected, which may be a symptom of overload, the delay between transmitted packets is increased. If the ratio of retransmitted packets is very low, this delay is decreased. Thresholds used by the delay adaptation algorithm are parametrized and may be changed before synthesis of the core. For debugging purposes, current transmission delay is included in packets sent from FPGA to the computer (field *Transmission Delay* in Table 2).

### 3.2 Early retransmission mechanism

The described retransmission algorithm has one significant disadvantage. If the packet pointed by the Tail pointer (or its acknowledge) is lost, the space in the packet buffer will not be freed, until

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2It is possible, that the core receives a delayed, duplicated acknowledge packet. In this case the buffer no longer contains the corresponding descriptor.

3The packet number wraps every $2^{32}$ packets. Therefore comparison of those numbers is defined as follows: $N_1 > N_2$ if $(N_1 - N_2) \pmod{2^{32}} \leq 2^{31}$.
Figure 4. Operation of the early retransmission mechanism: a) without sequence numbers, b) with sequence numbers. In both cases packet 2 gets lost, and the ACK for packet 4 gets lost. For time=7 packet 3 gets confirmed, but no ACK for packet 2 has been received earlier. Therefore packet 2 is scheduled for immediate retransmission. For time=9 the packet 5 gets confirmed, but neither packet 2 nor packet 4 have been confirmed yet. Therefore in case (a) both those packets are scheduled for immediate retransmission. In case (b) the sequence number is checked. In that moment the last sequence number for packet 2 is equal to 7, and for packet 4 to 4. As the received ACK for packet 5 has sequence number equal to 5, only packet 4 is scheduled for immediate retransmission.

this packet is retransmitted again and successfully confirmed. In the described implementation this packet will be retransmitted only after all other pending packets are transmitted or retransmitted. Therefore the core will not accept new data for significant amount of time.

The performance of the algorithm may be improved, if such a packet is retransmitted as soon, as its loss (or loss of its acknowledgement) is detected. The clear sign of such event is, when the core receives acknowledgement for the packet which was transmitted after that one. Such a solution is similar to the “Fast retransmit” used in the TCP protocol [17]. The simplest solution could be retransmission of all “earlier” unconfirmed packets after an acknowledgement of the “next” packet is received.

Unfortunately such a simple implementation, based only on the number of packet in the data stream is not optimal. If loss of yet another packet is detected before such “early retransmitted” packet is confirmed, this packet will be unnecessarily retransmitted once again (see Figure 4 a ). To prevent this, the data packets are labelled additionally with the frame sequence number which is incremented after every transmission. The last frame sequence number used to transmit the particular data packet is stored in packet’s descriptor (the “Seq” field in Figure 2). This frame
sequence number is copied to the acknowledgement packet. When loss of the packet is detected, it is possible to early retransmit only those packets which have the last frame sequence number smaller than the acknowledgement packet just received (see Figure 4 b).

3.3 Execution of user commands

To ensure that each command is reliably delivered, executed exactly once and the results are correctly delivered to the computer, the command sequence numbers (CSNs) are used.

Whenever a new command is sent to the FPGA core, the CSN is increased. This allows to discard possible duplicated responses to previous commands. After sending the new command, the computer waits for the response for certain configurable amount of time. If the computer doesn’t receive the command response packet in the declared time period, it states that either the command packet or the response packet got lost. In this case the computer resends the same command once again.

When the FPGA core correctly receives the command packet, it first checks its CSN. If it is the same as in the last serviced command (which means, that the response packet got lost, and command was resent), the core only resends the response for that last command. If the CSN is different, the core stores it, executes the command, and afterwards sends the response packet with the same CSN.

The command response is sent in the pending data frame, if it is available, or (when currently no data packet is waiting for transmission or retransmission) in the dedicated command response packet (see Table 2 c–e).

3.4 Resources consumption

In Kintex 7 xc7k325tfkg900-2 (both in KC705 and in AFCK) the core with $N_{FPGA} = 32$ occupies 801 slices (2107 slice LUTs and 1240 slice registers) and 65 BRAM tiles per link. With smaller memory buffer $N_{FPGA} = 16$ the core occupies 756 slices (2065 slice LUTs and 1234 slice registers) and 33 BRAM tiles per link.

In Spartan 6 xc6slx45csg324-2 in Atlys board the core with $N_{FPGA} = 16$ occupies 611 slices (1599 slice LUTs and 1227 slice registers) and 68 BRAM blocks (implementation of the core with $N_{FPGA} = 32$ was not possible due to too high BRAM consumption).

4. Linux driver

The GNU/Linux is widely used in modern data acquisition systems. It is free and open source, and therefore it is a perfect platform for such an open solution as the one proposed in this paper.

Because FADE-10G uses a non-standard Ethernet protocol, it is necessary to implement a dedicated kernel driver as a protocol handler responsible for reception of the Ethernet frames of 0xfade type. Similarly to solutions described in [3] and [13], the protocol handler is installed using the dev_add_pack function. Whenever the Ethernet frame with 0xfade type is received, the callback function in the driver is called.

The driver may service one or more FPGA based FEBs. They can be connected to separate Ethernet cards, or (via a switch) to the same Ethernet card (see Figure 1). Each connected FPGA based FEB is serviced via the dedicated character device /dev/l3_fpga%d, where %d is replaced.
with subsequent numbers, starting from 0). The maximum number of serviced FEBs is declared when loading the driver, using the `max_slaves` parameter. Whenever the particular character device is opened and configured for communication with the FPGA with given MAC address (slave), a `slave context` is created, describing the state of communication with that slave. One of components of the `slave context` is the `receiver packet buffer`, which stores received data. The amount of memory in the computer is significantly higher, than amount of internal memory in the FPGA. Therefore this buffer may be much longer than the memory buffer in the FPGA core (which has the length of $2^{N_{FPGA}}$ packets, as described in Section 3.1). Its length in bytes is chosen as $2^{N_{CPU}}$ packets, so that the lower bits of the packet number in the data stream may be directly used as a number of corresponding `packet slot` in the `receiver packet buffer`. This buffer is used as a circular buffer controlled with `Head pointer` and `Tail pointer`, pointing respectively to the next byte to be written, and to the last byte not read yet.

### 4.1 Packet reception routine

When the packet of `0xfade` type is received, the callback function `my_proto_rcv` is called. It first checks, if the packet arrived from the correct (“opened”) FEB. If not, the driver sends “reset” command to the misbehaving FEB. If the correct FEB slave is found, further operations are performed on the `slave context` of that FEB.

The function checks the protocol version. If it is incorrect, error flag is set and the packet is dropped. Then the type of the received packet is checked. If it is a command response packet, and if there is a thread waiting for completion of this command, the result is copied from the packet to the user space buffer, the waiting thread is woken up end the function returns. If the packet is neither a response packet nor a data packet, the error flag is set and the packet is dropped. Otherwise the packet is handled as a data packet. First the function checks the command response section, and if there is a thread waiting for the completion of corresponding command, it copies the result to the user space and wakes up this thread (like in the case of dedicated command response packet).

The `receiver packet buffer` stores the 32-bit `packet number` of the last received and confirmed packet for each `packet slot`. The number of the received packet in the data stream (see Table 2) is compared to `packet numbers` of packets currently stored in the `receiver packet buffer`. If the packet is already received and confirmed, or if the packet is “older”, than packets in the buffer, it is assumed that possibly the confirmation was lost, and the function simply marks, that the packet should be confirmed once again. If the packet is “newer” than packets in current `transmission window`, it means that the protocol error occurred - the function sets the error flag and drops the packet. If none of the above conditions applies, the packet contains new, unconfirmed data. The length of the packet is verified, and the function checks if there is enough free place in the `receiver packet buffer`. If not, it drops the packet (it will be retransmitted again by the FEB). If there is enough free place, data from the packet are copied to the corresponding `packet slot`.

If the received packet was the “last unconfirmed yet”, the routine updates the `Head pointer`. If it was the “last data packet” (see Table 2 d), additionally the last packet flag is set. If the amount of data available in the buffer is higher than the “receiver wake-up threshold” set by the

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4The “age” of packets is checked by subtracting their numbers modulo $2^{32}$, and result below $2^{31}$ is considered to be a positive number.
user application, the receiving thread is woken up. Additionally if the last packet flag is set and all packets are confirmed, the “end of transmission” flag is set and the receiving thread is also woken up. Finally, if required, the confirmation packet is prepared and scheduled for transmission.

4.2 Communication with the user application

To avoid conflicts when controlling different slaves, each character device (/dev/l3_fpga%d) may be open only once, by one application. However the user application may perform two different activities: reception of data and sending of control commands. Commands are serviced in synchronous way, and the thread sending the command is put on sleep until the command is executed and the response is received. When the data are transmitted at the high speed, it is unacceptable to stop data reception until the command is executed. Therefore the user application, after opening the device, should start an additional thread, so that data reception and processing and execution of control commands are handled in separate threads.

To avoid overhead associated with copying of data, the receiver packet buffer for each slave should be mapped into the appropriate application’s memory, using the drivers mmap function. Therefore the data are copied only once - from the socket buffer delivered by the Network Interface Card (NIC) driver to the shared kernel receiver packet buffer

5. Of course access to such shared memory must be appropriately synchronized. This is achieved using the ioctl function. The driver implements a set of ioctl commands, summarized in the table [3].

4.2.1 Reception of data

The user application may read current positions of the Head pointer and Tail pointer in its receiver packets buffer, using the L3_V1_IOC_READPTERS ioctl command. This command ensures appropriate synchronization, so that the stable Head pointer values are read. Additionally this command returns number of available bytes in the receiver packet buffer. To avoid active waiting for data, the application may define (with the L3_V1_IOC_SETWAKEUP ioctl command) how many bytes of data must be available in the receiver packet buffer before the receiver thread is woken up (the thread will be woken up also when the transmission finishes, even if the number of available bytes is below the defined threshold).

4.2.2 Sending the user commands

When sending the user command, the user fills the structure containing code of the command, its argument, number of retries and timeout for each retry. Those parameters allow the user to adjust behavior of the driver to the expected time of execution of the command. Pointer to this structure is used as the second argument to the ioctl call. When the ioctl L3_V1_IOC_USERCMD is executed, the current thread is put on sleep until the command response is received or until the timeout expires. In the latter case, the command is sent once again, until the given number of retries is reached. Together with the functionalities of the FPGA core described in the subsection 3.3, this

5Even though there are technologies offering the true zero copy handling of network data, like “Direct NIC Access” [3] or “PF_RING ZC” [19], it is not clear whether they can be used to create the continuous representation of the received data in the user application memory without additional copying. In fact the PF_RING ZC still requires single copying of the data, when used with standard NIC.
Table 3. The ioctl commands implemented in the kernel module to support communication with the user space application.

| IOCTL code                      | Description of the commands                                      |
|---------------------------------|------------------------------------------------------------------|
| L3_V1_IOC_SET_WAKEUP            | Sets the number of new data which must be present in the circular buffer, before the user space application will get woken up. |
| L3_V1_IOC_GET_BUFLEN            | Returns the length of the circular buffer associated with the particular FEB. |
| L3_V1_IOC_READ_PTRS             | Returns the number of the available data bytes and the positions of the Head pointer and Tail pointer in the circular buffer associated with the particular FEB. Provides necessary synchronization when accessing the pointers. |
| L3_V1_IOC_WRITE_PTRS            | Should be called with the number of bytes processed by the application. Provides necessary synchronization and updates the Tail pointer in the circular buffer associated with the particular FEB. |
| L3_V1_IOC_GET_MAC               | Associates the FEB identified by the given MAC, connected to the given network interface, with the particular character device. |
| L3_V1_IOC_START_MAC             | Starts the transmission from the previously associated FEB.       |
| L3_V1_IOC_STOP_MAC              | Stops the transmission from the FEB associated with the particular character device. |
| L3_V1_IOC_FREE_MAC              | Deassociates FEB from the particular character device.             |
| L3_V1_IOC_RESET_MAC             | Resets the FADE-10G core in the FEB associated with the particular character device. |
| L3_V1_IOC_USER_CMD              | Sends the user command to the FEB associated with the particular character device. This command sleeps the current thread until the command is executed and the result is sent back. |

The implementation ensures correct, single execution of command, even if either the command packet, or response packet gets lost.

5. Tests and results

The FADE-10G protocol was tested in different scenarios. The 1 Gbps operation was verified using the Atlys board [20] and Dell Vostro 3750 (Intel Core i7-2630QM CPU, 2.0 GHz clock). The 10 Gbps operation was verified using the KC705 board [21] and a computer equipped with Intel Core i5-4440 CPU, with 3.10 GHz clock. Additionally operation with 4 10 Gbps links was verified with the AFCK board [22], equipped with FMC board with 4 SFP+ cages and a computer equipped with Intel Xeon CPU E5-2630 v2, with 2.60 GHz.

Correctness of transmission was tested with the FPGA core sending the preprogrammed sequence of data, which was later on verified by the receiving computer. Transmissions up to 10 Tb were tested and no transmission errors occurred. The achievable transmission speed was equal to 990.34 Mbps with 1 Gbps interface in the Atlys board.

In tests of maximum transmission speed with 10 Gbps links, it was found, that verification of data leads to decrease of the achievable throughput, as the user application was not able to
process data at the full speed, which activated the congestion avoidance algorithm. Therefore the maximum throughput tests were performed without the full verification of data. Tests with 10 Gbps demonstrated 9.815 Gbps with 10 Gbps interface in the KC705 board, however to achieve such throughput it was necessary to decrease receive interrupt latency in the network adapter with the “-C rx-usecs 0” command of the *ethtool* program. With standard interrupt latency of 1 µs, the achievable throughput was equal only to 6.5 Gbps. The CPU load during the transmission (measured with *top*) didn’t exceed 5%.

Operation with 4 10 Gbps links in the AFCK board working simultaneously has shown limitations related to the computer speed. The achieved mean throughput was equal to 9.72 Gbps per link (with full data verification the throughput was further limited to 8.88 Gbps per link).

The protocol was also tested with the user application transmitting the data directly to the disk. In this setup the throughput was limited by the disk (achieved throughput was the same as with the application storing the pre-generated pseudorandom data to the disk). The congestion avoidance algorithm has correctly limited the transmission rate from the FPGA core. The data stored to the disk were later analyzed and no corrupted data were discovered.

The last series of tests verified transmission of the user commands in the worst conditions. The dedicated application transmitted user commands during reception of the continuous stream of data. In the 1 Gbps setup the FPGA core was able to execute 2870 commands per second (with data transmission speed unaffected). In the 10 Gbps setup the FPGA core was able to execute ca. 40000 commands per second (without impairing the transmission speed).

### 6. Conclusions

The presented FADE-10G system allows to reliably transmit measurement data from an FPGA via 1 Gbps or 10 Gbps interface to the computer running Linux OS. The system is able to almost fully utilize the link throughput. Except of transmission of data, the system implements simple control or diagnostic commands, which are reliably transmitted to the FPGA, and their results are reliable transferred to the computer. Even with fully occupied link, the system executes over 2800 commands per second with 1 Gbps link, and ca. 40000 commands per second with 10 Gbps link. The system minimizes packet acknowledge latency, which allows to reduce amount of memory needed in the FPGA to buffer the data. Additionally the system implements a special “early retransmission” mechanism, which reduces latency of data retransmission in case of lost packet. The data received by the computer are delivered to the user application using the memory mapped kernel buffer, which allows to avoid unnecessary data copying and reduces CPU load.

The FADE-10G system is implemented in possibly simple way and published under permissive license (most parts under BSD license, some under GPL license and some as public domain), therefore it can be a good base solution for further development of a transmission system suited for particular experiment. Sources of the FADE-10G project are available on the OpenCores website [23].

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