Surface preparation and patterning by nano imprint lithography for the selective area growth of GaAs nanowires on Si(111)

Hanno Küpers1, Abbes Tahraoui1, Ryan B Lewis1, Sander Rauwerdink1, Mathias Matalla2, Olaf Krüger2, Faebian Bastiman1, Henning Riechert1 and Lutz Geelhaar1

1 Paul-Drude-Institut für Festkörperelektronik, Hausvogteiplatz 5-7, D-10117 Berlin, Germany
2 Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik, Gustav-Kirchhoff-Strasse 4, D-12489 Berlin, Germany

E-mail: kuepers@pdi-berlin.de

Abstract

The selective area growth of Ga-assisted GaAs nanowires (NWs) with a high vertical yield on Si(111) substrates is still challenging. Here, we explore different surface preparations and their impact on NW growth by molecular beam epitaxy. We show that boiling the substrate in ultrapure water leads to a significant improvement in the vertical yield of NWs (realizing 80%) grown on substrates patterned by electron-beam lithography (EBL). Tentatively, we attribute this improvement to a reduction in atomic roughness of the substrate in the mask opening. On this basis, we transfer our growth results to substrates processed by a technique that enables the efficient patterning of large arrays, nano imprint lithography (NIL). In order to obtain hole sizes below 50 nm, we combine the conventional NIL process with an indirect pattern transfer (NIL-IPT) technique. Thereby, we achieve smaller hole sizes than previously reported for conventional NIL and growth results that are comparable to those achieved on EBL patterned substrates.

Keywords: selective-area-growth, vertical yield, mask processing

(Some figures may appear in colour only in the online journal)

1. Introduction

In recent years, numerous electronic and optoelectronic devices based on semiconductor nanowires (NWs) have been demonstrated, including LEDs, lasers, and photovoltaic cells [1]. Fairly independently of the material, these structures can be grown directly on Si substrates, allowing direct bandgap III–V devices to be integrated with Si technology. For many applications, controlling the position of the NWs on the chip is essential. One prominent approach is the selective area growth (SAG) in the holes of a patterned mask, which is defined in thermal silicon oxide layers using advanced lithography methods. Due to the low sticking on the oxide surface, growth is restricted to the nano-holes. In the case of Ga-assisted growth of GaAs NWs by molecular beam epitaxy (MBE), this approach has been of great interest in recent years [2–6].

Despite much progress, realizing a high vertical yield, i.e. ratio of vertical NWs to holes in the mask, remains challenging. Often, NWs form at the desired position but do not elongate perpendicular to the substrate or even crystallites form instead of NWs. Vertical yield values vary significantly among different studies [2, 7] because the yield depends not only on growth parameters [5, 7] but also critically on mask processing conditions [3, 4].

Additionally, in core–shell NW devices [8] it is desirable that the hole size is smaller than the NW diameter in order to minimize leakage currents between the substrate and the doped shells. Previously, two advanced lithography approaches have been used for the SAG of NWs: electron beam
lithography (EBL) [2–4, 6, 9–11] and nano imprint lithography (NIL) [5, 12, 13]. In principle, NIL is faster for large pattern sizes because EBL is a sequential process. However, so far the NIL approach could not realize feature sizes that are comparable to what was achieved with EBL (40 nm). Theoretically, the resolution limit of NIL depends mainly on the minimum feature size on the stamp, which can be fabricated by EBL. However, in practice, the precise pattern transfer into the mask layer with a high fidelity depends first on the thickness and the uniformity of the residual layer underneath the imprint pattern, and second on the optimization of the plasma etching parameters for each process step.

In this study, we explore different surface preparation treatments and the impact of this processing step on the vertical yield. We show that boiling the wafer in ultrapure water can increase the vertical yield from 5% to 65% on EBL patterned substrates, indicating that the surface preparation is of crucial importance for the nucleation of GaAs NWs in the vapor–liquid–solid (VLS) mode. Based on this surface preparation, we can achieve a vertical yield of 80% on EBL patterned substrates by further optimizing the growth parameters. In order to transfer this result to large arrays patterned by NIL, we establish a process to reach hole sizes that are comparable to what we achieve with EBL. Our approach combines the conventional ultraviolet-NIL (UV-NIL) technique with an inverse pattern transfer process (NIL-IPT) [14]. This novel combination enables the realization of holes with diameters below 50 nm, significantly smaller than values reported for the conventional NIL process with direct pattern transfer.

2. EBL processing and growth experiments

For the first part of this study, substrates were patterned by EBL. First, 100 nm of positive EBL resist was spin-coated on 2" and 3" Si(111) wafers covered with a 15–20 nm thick thermal silicon dioxide (SiO2) layer. Then, the pattern was written in an EBL system. The EBL pattern comprises fields with hexagonal arrays of holes with pitches ranging from 0.1 to 10 μm and minimum hole diameters of 40–50 nm. Subsequently, the resist was developed and the oxide mask was etched by reactive ion etching using CHF3 for an etching time of 10 minutes, after which the temperature was lowered to the growth temperature of 630 °C. Ga was pre-deposited at a flux of 0.5 ML s⁻¹ for 90 s. Subsequently, NW growth was initiated by supplying Ga and As2 simultaneously at a V/III ratio of 2.4. The growth time was 15–30 min, after which all sources were closed and the substrate was ramped to 100 °C. A more detailed description of the growth and related calibration routines can be found in our previous publication [15].

3. Surface preparation

One reason for the low reproducibility of the vertical yield of GaAs NWs in SAG by MBE is the limited understanding of the initial nucleation of NWs at the substrate-droplet interface. A way to change this interface is the exploration of different surface treatments of the Si(111) surface prior to growth. For the growth on unpatterned substrates the impact of surface preparations on the vertical yield has been explored previously, usually including re-growth of the native oxide [16]. In the case of SAG, this native oxide layer is unwanted and only changes of the bare Si surface are of interest. In general, fluoride acid solutions are employed to remove the native silicon oxide in the mask openings. Aqueous solutions of HF have been reported to produce atomically rough Si(111) surfaces [17, 18]. The surface is oxide free but small clusters are present with di- and trihydrides saturating the dangling bonds of the Si atoms at the edges. These edges are selectively etched in etching solutions with a higher pH value, as for example ammonium fluoride (NH4F), leading to an atomically flat surface [18]. A similar effect is achieved by boiling the sample in oxygen-free water for up to 10 min where OH⁺ ions attack the Si backbonds [19]: It was reported that this treatment leads to a Si(111) surface which is completely terminated by mono-hydrides [20], and the smoothness of the surface on an atomic scale was confirmed by scanning tunneling microscopy [21].

Figure 1 presents the surface topography of etched marker areas as measured by atomic force microscopy (AFM) on patterned substrates after etching in 1% HF solution for 60 s and rinsing with (a) cold (20 °C) water and (b) cold and subsequently boiling (100 °C) water. The root mean square roughness values are 0.19 nm and 0.17 nm, respectively. We
cannot assume this difference to be significant due to the resolution limit of the setup. Even though we cannot access the atomic roughness by AFM measurements, the sample with the boiling water rinse shows a larger feature size (average equivalent square size is 31.2 nm in (a) and 38.0 nm in (b) as calculated by a segmentation grain analysis using gwyddion). These larger islands are consistent with a smoother surface for the boiled sample.

In order to explore the impact of such surface treatments on NW growth, different treatments were carried out before loading the samples into the MBE system. Figure 2 shows scanning electron microscopy (SEM) images of samples after growth for substrates pre-treated with: (a) HF (1%) for 60 s with 3 min cold (20 °C) water rinse, (b) HF (1%) for 60 s with 3 min cold (20 °C) water rinse and 10 min hot (100 °C) water rinse, and (c) NH4F (40%) for 120 s with 3 min cold (20 °C) water rinse. The growth conditions were the same for all samples as described above. In figure 2(a), the vertical yield is below 5% with most holes occupied by tilted NWs or crystallites. However, the growth is restricted to the holes and the oxide surface seems to be free of residues. Figure 2(b) shows that adding a boiling water rinse in addition to the cold water rinse leads to a drastic increase in vertical yield to 65%. Figure 2(c) shows another sample which was grown on a wafer etched in NH4F instead of the HF dip (no boiling water). This sample also exhibits an increase in vertical yield to 25%. However, many droplets are present on the oxide surface indicating the presence of residues. Furthermore, the NWs of this sample have different lengths. Results from earlier experiments suggest that incompletely etched holes lead to the inhomogeneous length distribution. Here it may result from the low etching rate of the solution. The NH4F etching leads to a smoother surface but was reported to leave insoluble salt residues on the surface [22]. These residues may be the reason for the accumulation of material on the oxide surface as seen in figure 2(c).

Previously, it was reported that the contact angle of droplets on the substrate surface can have a significant impact on the nucleation and the corresponding vertical yield of NWs [16]. In order to check if the here presented surface treatment changes the contact angle we deposited Ga droplets on unpatterned Si(111) substrates in a similar fashion as has been done in the mentioned study. Even though we assume that the hole in the oxide mask has a significant impact on the shape of the Ga droplet, here, we are interested in the surface properties of the Si substrate. This effect will be similar on a bare substrate and in an etched hole and therefore we can use unpatterned substrates for this experiment. Figure 3 shows SEM top-view micrographs for samples with different surface treatments: (a) 1% HF for 60 s and rinsing in cold water and (b) 1% HF for 60 s and rinsing subsequently in cold and boiling water. The mean droplet diameter increases from 390 ± 50 nm to 620 ± 210 nm using boiling water and the density decreases from 0.92 to 0.21 μm⁻². The larger separation and size of the droplets indicate a longer surface diffusion length of Ga atoms on the Si surface for the substrate rinsed in boiling water, which is consistent with a smoother surface due to the hot water treatment. The insets of figure 3 show side-view micrographs of Ga droplets after the deposition. The contact angle is similar for the two samples (approximately 50° and 45°). These values are in agreement with the reported values for an oxide free surface [16]. Thus, the observed increase in vertical yield does not correlate with a significant change in contact angle. Consequently, NW nucleation cannot be understood by only investigating the contact angle and the underlying surface energies.

After further optimization of the growth parameters we could achieve a vertical yield of 80% as seen in figure 4. Our results underline the importance of the surface preparation for NW nucleation. Furthermore, our results are in agreement with the hypothesis that a smoother substrate surface leads to an improved vertical yield. We suppose that an atomically rough substrate surface may lead to a high density of initial nuclei at the droplet substrate interface leading to a rapid crystallization of the liquid Ga droplet into a GaAs crystallite.
HF + cold water
HF + boiling water

Figure 3. SEM top-view micrographs of Ga droplets deposited on unpatterned Si(111) substrates with different surface treatments: (a) HF and cold water and (b) HF, cold water and boiling water. Insets: SEM micrographs in side-view, showing a contact angle of 50° and 45°.

Figure 4. Micrograph of a NW sample grown on a substrate pre-patterned by EBL with optimized surface treatment and growth conditions. An overall vertical yield of 80% was achieved.

4. NIL with inverse pattern transfer

For the realization of large NW arrays, it is desirable to transfer the growth from EBL patterned substrates to substrates patterned by NIL-IPT. The complex process is depicted in figure 5(a). First, the Si(111) wafer with 20 nm thermal silicon oxide film is cleaned with oxygen plasma for 10 min in order to remove organic residue and enhance the hydrophilicity of the surface. Then, a 180 nm thick sacrificial resist layer UL3 is spin-coated (step 1 in figure 5), which is used for a lift-off process at the end of processing. Next, a thin film of adhesion promoter (mr-APS1) is spin coated and annealed at 150 °C for 1 min. Subsequently, the imprint resist ([mrUV-Cur21]) is spin-coated and the sample is soft baked for 1 min at 80 °C, in order to create a uniform layer and to remove solvent residues.

After coating the wafer with all resist layers, the NIL stamp is used to transfer the pattern into the UV-NIL resist layer (2). The total size of the imprinted structure is here 15 × 15 mm², but the method permits in general also the imprint of wafer scale patterns. The stamp is made out of UV-transparent quartz and consists of arrays of nanoholes. Such a stamp is more robust compared to a stamp containing nano-sized lamellas to directly imprint holes in the resist. Therefore, its life time is increased significantly, which helps prevent the creation of defects during the release of the stamp from the imprint sample and improves the cleaning process. Before the contact step, the surface of the UV-NIL stamp is treated with oxygen plasma for 10 min and coated with an anti-sticking solution. During the imprint process, the quartz stamp is horizontally levelled to the substrate-resist system and pressed onto the film with low pressure at room temperature. A helium gas flow is applied during the contact phase to avoid trapping of air bubbles between the stamp and the resist [23]. While the stamp and the substrate are in contact, the resist is exposed to UV light through the stamp, which promotes crosslinking in the resist. After having formed nanopillars in the resist layer, the mask is released (3) and a 200 nm thick hydrogen silsequioxane layer (HSQ) is deposited to planarize the sample surface (4). The final structure of the resist layers is depicted in figure 5(b).

The inverse pattern transfer consists of three different etching steps using plasma reactive ion etching. First, the HSQ layer is back etched under CHF3 gas down to the top of the nanopillars (5). In the second step, these pillars are selectively etched down to the SiO2 surface under oxygen plasma at −20 °C at a pressure of 0.8 Pa (6). In the third step, the pattern is transferred into the SiO2 layer by CHF3 plasma etching (7) for an etching time adjusted for each wafer according to its oxide thickness measured by ellipsometry. During this etching step the top HSQ layer is also partly etched but the etching of the SiO2 layer is not affected. As the last processing step, the resist layers are removed by a lift-off process using DI-water and the samples are cleaned by organic solvents, oxygen plasma and UV ozone (8). We want to mention that all resist materials used in the NIL-IPT process are purely organic provided by Microresist Technology. In combination with the lift-off process that is promoted by solution in DI-water, this feature assures the final surface cleanliness and the conservation of the underlying layer. Finally, these substrates are used for NW growth (9).

Figure 6(a) shows high resolution SEM images of the final pattern surface of substrates processed using the presented process. Hole diameters of below 50 nm could be realized with high fidelity. This result shows a clear improvement in the hole sizes of arrays used for NW growth compared to recent results using NIL with direct pattern transfer, showing hole diameters of 60 nm [13] and 100 nm [5]. In the direct approach holes are directly imprinted into the etching mask. During the etching of the thin residual layer that forms during imprint between stamp and substrate, the isotropic nature of the plasma etching leads to a widening of the hole size and inhomogeneities of the imprint pattern. This effect can be avoided by using the indirect pattern transfer, where the HSQ layer prevents hole widening during the second selective etching step. Even though our approach allows for smaller holes, we need to state that the complexity of the process makes it very sensitive to disturbances and it requires much time for process implementation and optimization.

Figure 6(b) shows a SEM image of a NW array grown on a substrate patterned by the presented NIL-IPT process. The same
growth conditions and surface treatment have been used that led to the optimized result for EBL patterned substrates as seen in figure 4. The vertical yield of the NIL-IPT patterned sample is comparable (above 80%) to what we obtained for EBL processed substrates, and to results on substrates patterned by NIL with direct transfer [5], displaying the efficacy of both processes for SAG of NWs. However, for the array grown on the NIL-IPT processed substrate a hole in the pattern is missing (blue circle in figure 6). This defect of the pattern regularly appears on NIL-IPT samples. It is caused by trapping of air bubbles between the stamp and the resist during the contact step, which results in missing pillars during the pattern transfer. One way to overcome this issue might be to use the step-and-flash imprint lithography approach [24], in which the exact amount of the dispensed droplets is controlled and optimized, which helps to reduce the thickness of the residual resist layer significantly after the separation step, leading to an imprint layer with improved homogeneity.

5. Conclusions

We improved the vertical yield of Ga-assisted GaAs NWs grown by MBE on pre-patterned substrates from 5% to 65% by following an improved substrate preparation procedure. The key process is rinsing in boiling water as the last step before loading the substrate into the MBE chamber. The origin for the improvement is not clear but we expect that it is...
related to the atomic scale roughness. These results will be important for understanding nucleation of VLS NWs and will help facilitate the reproducible and comparable SAG of VLS NWs.

Furthermore, using NIL with an inverse pattern transfer (NIL-IPT) we realized hole sizes smaller than those reported previously with NIL with direct pattern transfer, in particular below 50 nm. After optimization of the growth conditions we achieved vertical yield values of above 80% for substrates patterned by EBL and NIL-IPT. Therefore, this study presents the basis for the growth of NW samples on large-scale substrates and cost-effective patterns with a high vertical yield.

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ORCID IDs

Hanno Küpers @ https://orcid.org/0000-0001-8878-4644

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