A New Type of Right-leg-drive Circuit ECG Amplifier Using New Operational Amplifier

Wang Yang1, a
1Faculty of science and technology, University of Macau, Macau, China
*db72725@um.edu.mo

Abstract. The low-power consumption and low-noise sensor remain an important challenge in Electrocardiogram (ECG) sensor field. A new operational amplifier (op-amp) design is proposed in this study, and it is integrated into the traditional “right-leg-drive” circuit to cancel out the common-mode interference. Besides, the gain of this circuit can be controlled by adjusting the value of these resistors. Then, the traditional op-amp is redesigned to improve the performance of this circuit. Some improvements are made on the basis of the traditional sleeve-type cascade amplifier to obtain good gain and gain bandwidth. At the same time, power consumption is not too high. Meanwhile, to minimize the noise of the op-amp without using large value capacitors, pseudo-resistors are used. The right-leg-drive circuit is used in the overall process to ensure good common-mode rejection ratio (CMRR) performance. For the newly designed op-amp, its gain can reach 60db, and the operating frequency of the circuit is between 0.1HZ and 108HZ, and the error is no more than 10%. The differential mode gain of the overall circuit is 43.4db, and the error is within 5db. The total power consumption of the circuit is 3.17u watts, which is less than the specified maximum power consumption, and the total integrated input-referred noise is 3.786µVRMS, which is less than the specified maximum circuit noise. The total capacitor usage is 1nF, less than the specified maximum capacitor usage. To sum up, the ECG sensor is designed using the "right leg drive circuit" and a new type of amplifier is designed to eliminate common-mode interference and improve the performance of the amplifier.

1. Introduction
When the cardiomyocytes are depolarized, a tiny electrical signal is generated, and this signal is captured and amplified to become an Electrocardiogram (ECG) signal, which can be captured by electrodes placed on the surface of the human body. Because a large number of cells in the human body are conductive, and the current flow direction is not necessarily the same in the microscopic view, resulting in macroscopic measurements, only very low-amplitude signals can be observed. At the same time, other power sources outside the body, such as 50HZ AC power sources, can produce relatively large common-mode interference in the human body through electric field coupling [1, 2].

This coupled common-mode interference can be equivalent to the voltage generated by a displacement current flowing through a capacitor between the human body and the ground. This voltage can be broken down into two parts: the isolation mode voltage between the amplifier and ground, and the common-mode voltage generated by the human body at the common of the amplifier [3]. The isolation mode voltage obviously cannot be reduced, but there are many ways to reduce the common-mode voltage. And when the common mode is very low, there is no need to use a differential amplifier, which is also a significant advantage [4].
There are many ways to solve this common-mode interference, and the simpler one is to directly connect the electrode to the common of the amplifier. However, the impedance requirement of the electrode is relatively high. If the impedance is large when the electrode is in contact with the skin, it may have a huge impact on the performance of the amplifier.

Another method with more common and lower electrode requirements is to use the right-leg-drive circuit. It uses an inverting amplifier to collect the common-mode voltage from the right leg of the human body, farthest from the heart, to ensure the accuracy of the common-mode voltage. Then the obtained voltage is input into the common terminal of the two amplifiers, so as to cancel the positive common-mode voltage at the common terminal mentioned above [5].

Most calculations based on the right-leg-drive circuit rely on the characteristics of an op-amp, which has higher requirements on the various parameters of the op-amp used in this circuit. With the development of the portability of measurement equipment, this design requires more and more low power consumption and a high-performance op-amp. In the design, trade-offs need to be among speed, power and gain [6]. In order to solve this trade-off, a two-stage amplifier design can be used to take into account various data at the same time.

This article proposes a new type of operational amplifier design. This amplifier has a good frequency response, and the power consumption is not very high, and can be used to amplify ECG signals with very small amplitude. This article integrates this amplifier into the traditional right-foot drive circuit to eliminate common-mode interference. At the same time, the MOS tube forms a pseudo resistor to limit the operating frequency range of the circuit and reduce noise. The system will become a part of a wearable smart measurement device (such as a smartwatch) to achieve ECG signal measurement.

At the same time, for wearable devices, in order to ensure portability and practicability, the design should try to ensure a lower power supply voltage and lower power consumption. In terms of power supply, a boost circuit can be used to increase the power supply voltage, and the power consumption of the amplifier can be emphasized in the design [7, 8].

As for ECG measurement, how to suppress noise is also important. Since ECG signals are mainly low-frequency signals, noise will have a great influence on the measurement [9]. The noise is mainly flicker noise, so MOSFETs are used instead of resistors, which can greatly reduce the flicker noise caused by resistors [10].

In the first section, the design of op-amp and its theoretical calculation, frequency response and power consumption measurement will be introduced. The second section explains the design of the overall circuit and some other circuits. Finally, the measurement of some parameters of the overall circuit, including the measurement of the overall circuit frequency response, noise, and power consumption, is discussed.

2. Result and Discussion

2.1 Op-amp design

2.1.1 Overall schematic

![Figure 1. Overall schematic](image-url)
Figure 1 shows the overall design of the amplifier proposed in this article, which is composed of two stages and uses a current mirror to generate the bias current of the system. The first-stage amplifier mainly uses a cascode structure to obtain greater gain. The second one is mainly used to ensure that the system can have a large enough slew rate and other performance.

Through the schematic diagram of the transistor level shown in Figure 2, the structure of the entire amplifier can be clearly seen. The middle structure is the first-stage amplifier, which uses a sleeve-type cascode structure. This circuit has high speed, low power consumption and low noise, and the gain is also large. However, a single-stage amplifier is far from enough, because the small-signal current of the output tube of the single-stage amplifier directly flows through the output impedance. Therefore, the gain of the single-stage amplifier is limited to the product of the output tube transconductance and the output impedance. The use of a cascode structure can greatly increase the value of the output impedance and thus increase the gain, but it will inevitably lead to a reduction in the range of the output voltage, resulting in a reduction in the output swing.

In order to solve this contradiction, this paper adopts a two-stage operational amplifier design. The overall gain is obtained by cascading the two-stage amplifier, and the output swing is obtained by the second-stage common source amplifier.

### 2.1.2 Calculation

This section will do some calculations about the above two structures.

When only one layer of PMOS and one layer of NMOS are used, the small signal in Figure 3 can be used to do some calculations. From the structure, it can be known that the current $i_x$ is equal to $i_y$. According to the relationship of voltage, the following formulas can be obtained:

$$ (ix - gmnVin1) \cdot rON = VA - VP = ix \cdot (r_{OP}\|\frac{1}{\beta_{mp}}) $$

(1)
\(-iy + ix (r_{OP}||\frac{1}{g_{mp}})\) \(r_{OP} = V_{out}\)  
(\(iy - gmN\text{Vin}^2\)) \(r_{ON} = V_{out} - V_P\)  

Then from above three equations, the dc gain of this amplifier can be found as follows: 
\[
\frac{V_{out}}{V_{in1} - V_{in2}} = gmN(r_{ON}||r_{OP})
\]  

The \(r_{ON}\) and \(r_{OP}\) are the output resistances of the positive and negative sides. No matter how many the layers are, the output resistance can be calculated, and the final answer can be gotten. 

According to this structure, Figure 4 can be drawn. According to the small signal model, the following formula can be obtained: 
\[
V_{gs2} = -V_x
\]  
\[
i_{d2} = g_{m2}V_{gs2} = -g_{m2}V_x
\]  
\[
V_x = i_{test}r_{ds1}
\]  
\[
i_{test} = -g_{m2}V_x + \frac{v_{test} - V_x}{v_{ds2}}
\]

From the above four equations, the following equation can be gained: 
\[
\frac{v_{test}}{i_{test}} = r_{ds2} + r_{ds1}(1 + g_{m2}r_{ds2})
\]

Because \(g_{m2}r_{ds2}\) is much larger than 1, the equation is shown as: 
\[
r_{out} = g_{m2}r_{ds1}r_{ds2}
\]

And for the above part of the amplifier, the calculation procedure is quite similar to the downside. Therefore, if the values \(r_{ds}\) of the two transistors are the same, the output value of the upside should be: 
\[
r_{out} = g_{m2}r_{ds2}^2
\]

After simulation, this value is measured, and then the total output impedance can be calculated. Combined with the above analysis, the gain value can be obtained.

**Figure 4.** Small signal model of downside (a), and schematic of upside (b)

**Figure 5.** Common source amplifier
Stage 2 is a simple common source amplifier, as shown in Figure 5. Through calculation, its gain is expressed as the following formula:

\[
\frac{v_{out}}{v_{in1}-v_{in2}} = g_{mN}(r_{DN} || r_{OP})
\]  

(12)

2.1.3 Simulation result of op-amp

2.1.3.1 Parameters of transistors

| Table 1. Parameters in this design | \( g_m \) | \( V_{th} \) | \( r_{o} (\Omega) \) | \( i_d \) |
|-----------------------------------|---------|---------|----------------|--------|
| PMOS (up)                         | 795.1u  | -349.9m | 28058          | -41.43u |
| PMOS (down)                       | 849u    | -394.9m | 34473          | -41.43u |
| NMOS (up)                         | 400.7u  | 343.8m  | 20773          | 41.43u  |
| NMOS (down)                       | 805.8u  | 417.2m  | 7363           | 41.43u  |
| NMOS (stage 1 cm)                 | 1.032m  | 264.8m  | 29342          | 82.86u  |
| PMOS (down)                       | 3.124m  | -405.5m | 3454           | -632.8u |
| NMOS (stage 2 cm)                 | 7.645m  | 323.5m  | 3796           | 527.2u  |
| NMOS (cm)                         | 2.517m  | 325.4m  | 30788          | 200u    |

By bringing these data shown in Table 1 into the above calculations, the required values of various parameters can be obtained. \( v_{th} \) is the threshold voltage, which is the voltage between the minimum gate and source required to convert the MOSFET to the linear region and the saturation region. \( r_{o} \) is the drain output resistance in the MOSFET small signal model, and \( i_d \) is the drain current. Using these parameters, other parameters can also be calculated.

2.1.3.2 Simulations and calculations of dc gain

| Table 2. Calculation and simulation result of gain | Calculate | Simulate |
|--------------------------------------------------|-----------|----------|
| Stage 1                                          | 33.24db   | 38.49db  |
| Stage 2                                          | 20.66db   | 11.7db   |

This is the difference between the calculated gain value and the actual simulation result. It can be found that the calculated results are consistent with the simulation results.
2.1.3.3 Frequency response of circuit

![Figure 6. Frequency response; (a) magnitude frequency; (b) phase](image1)

After inputting a signal with constant amplitude and changing frequency to the system, and observing its output, some key parameters can be obtained.

In an electronic amplifier, the phase margin is the difference between the phase of the amplifier's output signal (relative to its input) and 180° at zero dB gain. From this figure we can clearly see the phase margin, for the frequency value which can make magnitude equal to 0. We can use following formula to calculate phase margin.

\[ PM = 180 - |\Delta \phi| \]  

So we can get the PM is 55.4 degree.

The phase margin is the phase change that can be increased before the system enters the unstable state. The larger it is, the slower the response speed is, but the more stable the system is. We can change it by changing the Miller compensation capacitor, which can lead the moving of poles, can change the phase margin. The design of this paper uses Miller compensation.

2.1.3.4 Power consumption

For current mirror

\[ P_{\text{current mirror}} = VDD \times \text{lin}_\text{cm} \]  

For amplifier 1:

\[ P_{\text{current mirror}} = VDD \times \text{lin}_\text{cm1} \]  

For amplifier 2:

\[ P_{\text{current mirror}} = VDD \times \text{lin}_\text{cm2} \]  

| Circuit     | Current(uA) | Power(mW) |
|-------------|-------------|-----------|
| Bias circuit| 200         | 0.24      |
| Stage 1     | 82.86       | 0.0994    |
| Stage 2     | 527.2       | 0.632064  |
| Total power |             | 0.97204 (mw) |

Power consumption is a very important indicator of the design in this article. Since the design is mainly used in wearable devices, the relevant power consumption must be small. After optimization, the design power consumption can be controlled within 1mw, which is suitable for wearable devices.
2.1.3.5 CMRR
CMRR expresses the ability to suppress common-mode signals, which are very large in human body, so in addition to the high gain and GBW, high CMRR is also needed. For the overall circuit, the right-leg-drive circuit is adopted to minimize common mode interference. For the amplifier itself, its two input terminals are connected together to measure the value of CMRR according to the following formula:

\[
CMRR = \frac{\mathcal{A}_d(j\omega)}{\mathcal{A}_c(j\omega)} = 50.19\text{db} - (-17.88\text{db}) = 68.07\text{db}
\] (17)

It can be seen that the value of CMRR is relatively large, which can cope with the huge common-mode interference of the human body.

2.1.3.6 Slew rate
Slew rate means the output voltage of the op-amp, which reflects the speed index of an op-amp. It indicates the ability of the op-amp to adapt to the speed of signal changes. It is also a measure of the operation of the op-amp when a large signal is applied. Since the rate of change of the ECG signal is not very large, the requirement for the slew rate is not very high, but we still measured it. It is found that this slew rate can basically meet all kinds of ECG measurement requirements.

The slew rate can be calculated by the following formula. However, because the maximum slope of the curve is difficult to calculate, the data are directly obtained through the computer.

\[
\text{Slew Rate} = \frac{dU}{dx}_{\text{max}} = 202.7 \text{ M}
\] (18)

2.1.4 Summery

| Table 4. Summary of amplifier performance |
|------------------------------------------|
| **value**                               |
| Gain                                    | 50.19db                                |
| GBW                                     | 570.6M                                  |
| PM                                      | 55.4 degree                             |
| DC output                               | 606 mv                                  |
| CMRR                                    | 68.07db                                 |
| Slew rate                               | 202.7M                                  |

Table 4 summarizes all the parameters of the amplifier structure of this article. It can be seen that its performance can fully meet the measurement requirements of the ECG signal.

2.2 Overall circuit design

2.2.1 Right-leg-drive circuit with a new op-amp
The amplitude of the ECG signal is between 0.5mv-0.8mv, and the common-mode interference of the human body can reach the V level, which has great interference to the measurement of the ECG signal. It would be difficult to improve only the structure of the operational amplifier, and even if it could, the cost of the operational amplifier would be relatively high. This can be done easily with the right-leg-drive circuit. The common-mode voltage of the human body on the right leg is collected, and its phase is flipped by 180 degrees through an inverting amplifier, and then it is input back to the common-mode point of the circuit to cancel common-mode interference. Common mode interference can be eliminated economically.

2.2.2 Electrode

In practical applications, signals from the human body need to be collected by electrodes. There will be some non-ideal effects during the acquisition process, and these effects will affect the measurement results to a certain extent. The structure shown in Figure 8 above is used to simulate the electrode that collects the signal, and one resistor in series is used with another resistor and capacitor in parallel. Because the electrode will generate coupling capacitance with the human body, the electrode itself and the human skin will generate resistance.

2.2.3 Pseudo resistor
Choosing suitable parameters can form a large resistance to reduce the capacitance value.

In actual circuits, it is difficult to make large capacitors, and it takes up space. In the design of this article, the performance of Miller compensation and filter part is affected by the product of capacitance and resistance, so the capacitance value can be reduced by increasing the resistance value. The MOSFETs shown in Figure 9 can be used as a pseudo resistor, and they are all diode-connected. By selecting appropriate parameters, their resistance can reach the T level, which greatly reduces the value of the capacitance. Therefore, the capacitance of the entire circuit can be controlled at the nF level.

2.3 Simulation result of overall circuit

2.3.1 Frequency response

![Frequency response graph](image1)

Figure 10. Frequency response

From the simulation results, it can be seen that the operating frequency of the circuit meets the requirements, and the error does not exceed 10%. The gain value has reached 43db overall, which meets the requirements of ECG signal measurement.

2.3.2 Input referred noise

![Input referred noise graph](image2)

Figure 11. Result of input referred noise simulation
Table 5. Performance summary of overall circuit

| Value                  | Value       |
|------------------------|-------------|
| Differential gain      | 43.4db      |
| Input referred noise   | 3.786 µVRMS |
| Total power consumption| 3mw         |

The input reference noise is the output noise of the circuit divided by the gain, which is used to determine the effect of noise on the output results of different circuits, that is, to what extent the circuit is damaged by noise. Figure 11 is the input reference noise simulation result of the circuit. It can be seen that the noise of the circuit does not exceed 5uVrms, which conforms to the ECG signal measurement standard, and the measurement effect is good.

3. Conclusion
In this study, a new amplifier structure is designed, which has the characteristics of high stability, high gain, and relatively low power consumption. Using this structure, combined with the traditional right leg drive circuit, a new type of amplifier is designed to eliminate common-mode interference and improve the performance of the amplifier. At the same time, pseudo-resistance is used to reduce the noise of the op-amp and limit the working frequency range of the circuit. It can be seen from the above data that the designed ECG sensor has the characteristics of low power consumption and low noise, and has a broad application prospect in the future ECG sensor field.

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