Stability Analysis for Fast Settling Switched DPLL
Pallavi Paliwal, Debasattam Pal, and Shalabh Gupta

Abstract—In current generation digital phase locked loop (DPLL) architectures, techniques like adaptive loop bandwidth with loop order switching and switched phase-detection are employed to achieve better lock time and jitter performance. This work derives stability conditions for such DPLL architectures using Multiple Lyapunov Functions (MLFs) for switched systems. The loop-parameters chosen on the basis of these stability conditions ensure that chattering phenomenon does not occur during switching between different subsystems. A 5 GHz fractional-N DPLL designed with these loop-parameter values is fabricated in CMOS65 nm-LT technology. The measured settling time of the implemented DPLL is within 1 μs. The efficiency of switching rule and stability conditions used for this DPLL is validated with the fast settling response, which is the best lock time reported until now for fractional-N DPLLs.

Index Terms—DPLL, Lyapunov theorem, switched system, Multiple Lyapunov Functions (MLFs), settling time.

I. INTRODUCTION

In PLLs employing LC oscillators, a trade-off between settling time and output jitter exists based on the loop bandwidth. For reducing both lock-time and jitter simultaneously, the concept of adaptive loop gain has been widely used in digital phase-locked loop (DPLL) architectures [1], [2], [3], [4]. Few DPLL designs also employ switching between linear and non-linear phase detection mechanism, to reduce high-resolution requirement on succeeding Time-to-Digital Converter (TDC) block. While design methodologies like adaptive gain mechanism and hybrid phase detection have been extensively explored for DPLLS, the stability analysis of these architectures has largely remained unexplored in literature.

For PLLs involving switched subsystems, linear and steady-state s-domain analysis is unable to predict nonlinear acquisition trajectory of a system. On the other hand, analysis techniques using difference equations and state-space model can define the functioning of both linear and non-linear PLL subsystems [5]. This work uses Lyapunov theory for analyzing stability conditions in switched-system DPLL.

In the available literature e.g. [6], [7], [8], [9], [10], the stability analysis using Lyapunov theorem has been done only for PLLs involving a single Linear-Time Invariant (LTI) system. This paper investigates global asymptotic stabilization of a hybrid DPLL architecture [2] (shown in Fig. 1), wherein the switching algorithm allows unstable states of non-linear time varying (NLTV) subsystem to work in coherence with linear-time invariant (LTI) subsystem. An exhaustive stability analysis becomes mandatory in this case with the architecture activating an unstable intermediate state in a bid to achieve a record-fast response time. As part of developing the stability criteria, this work verifies the loop parameter conditions to avoid chattering phenomenon while switching between different PLL subsystems. A similar analysis framework could be applied to other DPLL architectures as well.

As a case study, this work illustrates the stability analysis for adaptive DPLL with loop order switching as described in Section II. Section III gives an overview of the Lyapunov theorem approach for proving stability of the DPLL system with predefined switching rule. Sections IV and V derive Lyapunov functions for verifying the stability of DPLL with linear phase frequency detector (PFD) and non-linear bang-bang phase detector (BBPD). Section VI outlines the stability analysis of proportional-integral-derivative (PID) controller based switching algorithm in the DPLL, based on its known region of activation and deterministic state trajectory. Section VII highlights the overall DPLL stability with Lyapunov functions defined for individual subsystems. The measurement results in Section VIII provide the proof of DPLL stability with the loop gain conditions derived in this work.

II. DPLL SYSTEM OVERVIEW

We have proposed a fast settling DPLL in [2] which employs variable phase-detection and adaptive loop gain to achieve optimum lock time performance. This architecture involves switching between different subsystems based on the magnitude of phase error. Figure 2 shows that when the magnitude of phase error ($\phi_{err}$) is large, a linear PFD with digitally controlled oscillator (DCO) based counter is activated as the phase detection block (LTI-1 subsystem). With reduction in the phase-error below a single DCO clock period ($\phi_{err,1}$), an inverter based TDC is activated in the loop (LTI-2 subsystem). When the phase-error reduces below the delay corresponding to a single inverter ($\phi_{err,2}$), a BBPD is activated in the loop to keep the output jitter independent of the TDC resolution. Figure 3(a) highlights the phase-error state dependent switching in the DPLL across different subsystems.

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Fig. 1: Detailed block diagram of Hybrid DPLL architecture.
To improve the settling time with bang-bang phase detection, a finite state machine (FSM) shown in Fig. 3 is activated initially. This FSM emulates an additional PID controller in the loop. At the phase-error sign reversal, the FSM activates derivative gain for immediate phase correction. For a similar phase-error sign in consecutive cycles, the FSM activates derivative gain for immediate phase correction. When the derivative gain becomes 0, the FSM is removed from the loop to avoid chattering in the settled state. Therefore, the BBPD+FSM emulates a Non-Linear Time Varying (NLTV) subsystem, and the BBPD without FSM represents a Non-Linear Time Invariant (NLTI) subsystem.

![Fig. 2: Phase-error state dependent switching rule for DPLL toggling between different subsystems.](image)

Table I

| Parameter                        | Value               |
|----------------------------------|---------------------|
| Output Frequency                 | 4.8 GHz - 5.02 GHz  |
| Reference Clock ($f_{ref}$)      | 100 MHz             |
| DCO Gain ($K_DCO$)               | 10 KHz/LSB          |
| DCO Counter Resolution ($\phi_{err_1}$) | 1.67 ns           |
| Inverter Delay Line Resolution ($\phi_{err_2}$) | 20 ps            |
| DCO Jitter ($\sigma_{DCO}$)      | 0.2 ps              |

![Fig. 4: (a) I/O characteristics for PFD activated with DCO Counter for $|\phi_{err}| > |\phi_{err_1}|$, and inverter delay line for $|\phi_{err}| > |\phi_{err_2}|$; (b) I/O characteristics for BBPD+FSM.](image)

Table II

| Phase Error State | Phase Detection | Loop Type | Parameters |
|-------------------|-----------------|-----------|------------|
| $> \phi_{err_1}$  | PFD+            | LTI with  | PM ≈ 15°   |
| DCO Counter       | high loop gain  | B/W = 10 MHz |
| $> \phi_{err_2}$  | PFD+            | LTI with  | PM ≈ 35°   |
| Delay Line        | moderate loop gain | B/W = 7 MHz |
| $< \phi_{err_1}$  | BBPD+           | NLTV      | Unstable   |
| $(K_D > 0)$       |                 |           |            |
| $< \phi_{err_2}$  | BBPD            | NLTI with | B/W = 2 MHz |
| $(K_D = 0)$       |                 | low loop gain |            |

III. LYAPUNOV THEOREM OVERVIEW

Lyapunov theorem states that if a positive-definite storage function of the system could be found, which is decreasing with time along every possible trajectory of the system, then the equilibrium point is asymptotically stable. Thus, the system’s stability in Lyapunov sense is stated based on the storage function as follows:

Consider a discrete system described by $x_{k+1} = f(x_k)$, where $f(0) = 0$, $x_k \in R^n$, $k$ being the time index. The equilibrium state $x = 0$ is globally asymptotically stable if there exists a continuous scalar function $V_k = V(x_k)$, such that:

1. $V(0) = 0$
2. $V(x_k) > 0 \forall x \neq 0$
3. $\lim_{x_k \to \infty} V(x_k) = \infty$
4. $\Delta V_k \equiv V(x_{k+1}) - V(x_k) < 0 \forall x \neq 0$
Hence for a stable system, the design parameters are chosen such that the candidate Lyapunov function \(V(x_k)\) has a negative derivative along the trajectory of the system.

The DPLL in Fig. 1 is a state-dependent switched system. Though the subsystems of DPLL could be individually stable, the loop may still have divergent trajectories. On the other hand, it is also possible to make the loop switch between unstable subsystems such that the complete switched system becomes asymptotically stable \([11]\). Therefore, based on stability conditions, the DPLL parameters are derived such that the loop converges to its equilibrium point without cycling infinitely between two or more subsystems.

In a switched system, if there exists a Common Quadratic Lyapunov Function (CQLF) for certain subsystems, then the system is stable under arbitrary switching between those subsystems. Section VI discusses the stability of BBPD+FSM based DPLL, while switching between LTI-1 and LTI-2 subsystem.

The stability analysis of nonlinear-system is facilitated by the fact that Lyapunov function derivative only needs to be evaluated in the region where the system would be active \([11]\). Based on this clause, Section VI discusses the stability analysis of BBPD based DPLL, wherein a nonlinear function is replaced by different values it assumes in various regions of the phase plane. The state-space is thus partitioned into different regions based on the varying values of non-linear function. Consequently, the stability condition as per Lyapunov function is derived for these different cases of state-space equations.

With a suitable switching law in a switched subsystem, the trajectory can be brought to equilibrium even in the presence of an unstable subsystem. To achieve this, the stable subsystems are activated to compensate the state divergence caused by an unstable subsystem. Following this concept, Section VI verifies the stability of BBPD+FSM based DPLL which incorporates an unstable third-order integrator based subsystem. In this case, the energy functions of subsystems are analyzed at switching instants instead of consecutive cycles. Multiple Lyapunov Functions method \([12]\) states that for stability of system with difference equation \(x_{k+1} = f_j(x_k)\), the candidate Lyapunov function \(V_j\) corresponding to \(j\)th subsystem should satisfy condition in \([11]\), as shown in Fig. 5

\[
V_j(x_j(\bar{t}_j,k+1)) < V_j(x_j(\bar{t}_j,k)) (1)
\]

where, \(\bar{t}_{j,k}, \bar{t}_{j,k+1}\) are two consecutive switch-on instants of subsystem \(j\).

Fig. 5: Stability with multiple-Lyapunov functions is decided with decreasing value of \(V_j\), only at switching instants \([12]\). Thus, the multiple Lyapunov functions approach could be used to show stability for overall loop of DPLL incorporating subsystems with different storage functions.

IV. LINEAR DPLL STABILITY ANALYSIS

Consider that LTI-1/LTI-2 subsystem of DPLL, represented by Fig. 6 have initial phase and frequency error of \(\phi_0\) and \(\Delta f_0\). For evaluating PLL behaviour as an autonomous system, consider \(\phi_k\) and \(\Delta \phi_{f,k}\) as state variables representing phase error and additive phase due to frequency error in \(k\)th sampling instant.

With an ideal reference clock \((f_{ref})\) and a constant desired phase \((\theta_{k,des})\), the state-space equations for LTI-1/LTI-2 subsystems of DPLL are given as

\[
\phi_{k+1} = \phi_k + \Delta \phi_{f,k} - K'_P(\phi_k - \phi_{k-1}) - K'_I\phi_k,
\]

\[
\Delta \phi_{f,k+1} = \Delta \phi_{f,k} - K'_P(\phi_k - \phi_{k-1}) - K'_I\phi_k,
\]

where \(\phi_k = \theta_{k,des} - \theta_{k,fb}\), with \(\theta_{k,fb}\) being the feedback phase in the loop. The variables \(K'_P\) and \(K'_I\) denoting the proportional and integral gain in the loop, with \(K_{PF,DCO}\) being the TDC gain, are calculated as

\[
K'_P = \frac{K_{PF,DCO}K_{P,2\pi K_{DCO}}}{N_{div,ref}},
\]

\[
K'_I = \frac{K_{PF,DCO}K_{I,2\pi K_{DCO}}}{N_{div,ref}},
\]

\[
K_{PF,DCO} = \frac{T_{ref}}{2\pi \Delta t_{TDC}},
\]

where \(K_{DCO}\) is the DCO gain, \(N_{div}\) is the feedback division ratio, \(\Delta t_{TDC}\) is the TDC resolution, and \(T_{ref}\) is the reference clock period.

During locking process in PLL, the phase error \((\phi_k)\) is corrected by modulating the DCO frequency. Hence, the phase-error derivative is related to the incremental phase \((\Delta \phi_{f,k})\) from frequency error at the PLL output as

\[
\Delta \phi_{f,k} = \phi_k - \phi_{k-1}.
\]

The PLL is settled when the system’s trajectory reaches an equilibrium point of phase and frequency error \((\phi_k, \Delta \phi_{f,k})\) being \((0,0)\). From \([2] - [4]\), the state space equations used to prove stability in Lyapunov sense are derived as

\[
\phi_{k+1} = (1 - K'_I)\phi_k + (1 - K'_P)\Delta \phi_{f,k},
\]

\[
\Delta \phi_{f,k+1} = -K'_I\phi_k + (1 - K'_P)\Delta \phi_{f,k}.
\]

Representing the state-space equations in the form of matrices \([6]\), the system equation can be written as \([7]\).
\[
\begin{bmatrix}
\phi_{k+1} \\
\Delta \phi_{f,k+1}
\end{bmatrix} = 
\begin{bmatrix}
1 - K'_f & K \\
-K' & K
\end{bmatrix} 
\begin{bmatrix}
\phi_k \\
\Delta \phi_{f,k}
\end{bmatrix}
\]
where \( K = 1 - K'_p \)
\[ x_{k+1} = Ax_k \]

For stability analysis of this system, the candidate quadratic Lyapunov function is chosen as
\[ V_k = x_k^T P x_k, \]
where \( P = \begin{bmatrix} p_{11} & p_{12} \\ p_{12} & p_{22} \end{bmatrix} \).

To obtain \( V_k \) as a positive quantity, matrix P should be positive definite, which leads to the condition:
\[ p_{11}p_{22} > p_{12}^2, \quad p_{11} > 0, \quad p_{22} > 0. \]

Using the Lyapunov function \( V_k \), the change in energy of the system is given by
\[ \Delta V_k = x_k^T (A^T PA - P) x_k. \]

For the system to be stable in Lyapunov sense, \( (A^T PA - P) \) must be negative definite to have \( \Delta V_k < 0 \quad \forall \quad x_k \neq 0 \). Here, the discrete-time Lyapunov equation is \( A^T PA - P + Q = 0 \) with \( Q > 0 \), wherein for \( A^T PA \) being the energy function, \( A^T QA \) could be considered the associated dissipation.

Based on the required phase-margin and unity-gain bandwidth in the considered DPLL, loop-filter gain \( (K_{P_f} / K_I) \) for LTI-1 and LTI-2 subsystem is calculated using linear z-domain analysis presented in [13][2] as
\[
K_P = \frac{N}{K_{PFD}K_{DCO}} \frac{\omega_{UGBW}}{\sqrt{1 + \tan^2(\text{PM})}} \left( 1 - \frac{T_{\text{ref}}}{2} \right), \\
K_I = \frac{T_{\text{ref}}}{K_{PFD}K_{DCO}} \frac{N}{\omega_{UGBW}^2} \frac{\omega_{UGBW}}{\sqrt{1 + \tan^2(\text{PM})}},
\]

where \( T_{\text{ref}} \) is the reference clock period, \( N_{\text{div}} \) is the feedback divider, \( \omega_{UGBW} \) is the unity-gain bandwidth and \( \text{PM} \) is the phase-margin of the loop. Figure 7 shows the converging trajectory of DPLL in LTI-1 and LTI-2 mode, with loop-filter gain in Table III being derived from (10), based on the loop-bandwidth and phase-margin desired in each mode.

**TABLE III**

| Gain      | LTI-1 subsystem | LTI-2 subsystem |
|-----------|----------------|----------------|
| \( K_{PFD} \) | 6/2\pi          | 250/2\pi      |
| \( K_f \)   | 4096           | 128            |
| \( K_I \)   | 1024           | 8              |

Corresponding to the gain \( (K_{P_f} / K_I) \) in each subsystem, the matrix P could be found for common Lyapunov Function to have decreasing derivative under arbitrary switching between LTI-1 and LTI-2 subsystem. For instance, Fig. 8 shows the setting response of DPLL while switching between LTI-1 and LTI-2 subsystem with CQLF derived as
\[ V_{1,k} = \begin{bmatrix} \phi_k & \Delta \phi_{f,k} \end{bmatrix} \begin{bmatrix} 0.02 & 0.06 & 3 \end{bmatrix} \begin{bmatrix} \phi_k \\ \Delta \phi_{f,k} \end{bmatrix}. \]

Though the stability conditions in individual LTI-subsystem could be derived with linear z-domain analysis, the Lyapunov theorem aids in proving that the DPLL will be stable under arbitrary switching between LTI-1 and LTI-2 subsystem.

**V. BBPD BASED DPLL STABILITY**

Figure 9 shows the non-linear operation of BBPD based DPLL. In this case, the phase detector output \( \sigma(\phi_k) \) takes up the binary values of either +1 or -1, based on the sign of input phase error \( \phi_k \).
The DPLL state-space equations representing BBPD operation are
\[ \phi_{k+1} = \phi_k + \Delta \phi_{f,k} - K_{p3}' \sigma(\phi_k) - K_{i3}' \sigma(\phi_k), \]
\[ \Delta \phi_{f,k+1} = \Delta \phi_{f,k} - K_{p3}' \sigma(\phi_k) - K_{i3}' \sigma(\phi_k), \]
where \( K_{p3}' \) and \( K_{i3}' \) representing the proportional and integral gains in the feedforward path of BBPD based DPLL are given as
\[ K_{p3}' = \frac{K_{p3} 2\pi K_{DCO}}{N_{div} \cdot f_{ref}}, \]
\[ K_{i3}' = \frac{K_{i3} 2\pi K_{DCO}}{N_{div} \cdot f_{ref}}. \]

A. State-Space Partition

For simplified analysis, BBPD based nonlinear system can be modeled as a piecewise affine system of the form,
\[ x_{k+1} = A_i x_k + a_i \quad \text{for} \ x_k \in R_i \]
where \( R_i \)'s are polyhedral partitions of the state-space. The DPLL state-space can be thus partitioned into regions shown in Fig. [10] with the corresponding state-space equations derived from (12). Hence, based on the location of the state, the system’s settling trajectory is governed by (15) or (16), depending on whether the phase-error sign reverses or remains same in consecutive cycles.

\[ \phi_{k+1} = \phi_k + \Delta \phi_{f,k} - (2K_{p3}' + K_{i3}') \sigma(\phi_k), \]
\[ \Delta \phi_{f,k+1} = \Delta \phi_{f,k} - (2K_{p3}' + K_{i3}') \sigma(\phi_k) \]
\[ \phi_{k+1} = \phi_k + \Delta \phi_{f,k} - K_{i3}' \sigma(\phi_k), \]
\[ \Delta \phi_{f,k+1} = \Delta \phi_{f,k} - K_{i3}' \sigma(\phi_k) \]

B. State-Trajectory Direction

Equation (12) indicates that starting from an arbitrary \((\phi_0, \Delta \phi_0)\) point, the system’s trajectory moves in clockwise direction for \(K_{p3}' > 0\) and \(K_{i3}' > 0\). Also, (12) shows that the DPLL system enters into limit-cycle regime for \((\phi_k, \Delta \phi_k)\) satisfying condition \(\phi_k + \Delta \phi_k < (2K_{p3}' + K_{i3}') \sigma(\phi_k)\). Hence in succeeding sections, the Lyapunov function is discussed only for quadrant change by the DPLL trajectory in clockwise direction, outside the limit-cycle region. This knowledge of the state trajectory direction while passing through the partitioned state-space region aids in deriving the energy decreasing condition of the system.

C. Choice of Loop Filter Gain

Ideally, the lowest possible proportional gain \(K_{p3}'\) results in minimum jitter from BBPD limit cycles. With the lowest proportional gain \(K_{p3}'\) in the implemented DPLL, the DCO gain \(K_{DCO}\) of only 10 KHz/LSB corresponds to phase step \((\Delta \phi_{DCO, LSB})\) of only 15 fs in one DCO cycle. This low magnitude of phase step lies within the DCO’s random noise regime \((\sigma_{t,DCO} \approx 200 \text{ fs})\, as\, stated\, in\, Table II,\) and does not result in an immediate phase error correction. Thus, the decision of filter-proportional gain \((K_{p3}')\) value depends upon the jitter in the reference and feedback clocks. A lower proportional gain results in less noise contribution from BBPD limit cycles. However, a higher proportional gain ensures that a larger jitter in the feedback clock can be tolerated, without causing the DPLL to switch between different subsystems. In this design, the proportional gain \((K_{p3}')\) for final settling with BBPD is approximately kept as \(\sigma_{t,DCO} / \Delta \phi_{DCO, LSB} \approx 8\). Based on a fixed proportional gain \((K_{p3}')\), the integral gain \((K_{i3}')\) of loop filter is derived for stability as 1 using
\[ \frac{K_{p3}}{K_{i3}} \geq \tan(\omega_u T_{ref} D + P M), \]
where \(D\) refers to the loop delay [14].

D. Candidate Lyapunov Function

For analyzing stability in lyapunov sense, let BBPD based DPLL’s energy function be represented by (18), with energy function curve as shown in Fig. [11]
\[ V_{3,k} = x_k^T P x_k \]
where \(x_k = \begin{bmatrix} \phi_k \\ \Delta \phi_{f,k} \end{bmatrix}\) and \(P = \begin{bmatrix} 1 & 0 \\ 0 & 1000 \end{bmatrix} \).

Fig. 11: Candidate Lyapunov function for BBPD based DPLL.
In this case, the state-space matrix is modified as
\[
\Delta V_{k+1} = V_{k+1} - V_k,
\]
\[
= x_{k+1}^T P x_{k+1} - x_k^T P x_k,
\]
\[
= [Ax_k + a]^T P [Ax_k + a] - x_k^T P x_k,
\]
\[
= x_k^T [A^T P A - P] x_k + 2a^T P A x_k + a^T P a.
\] (19)

The energy change rate is evaluated for two different regions of DPLL phase plane as follows:

**Case I: Phase-error sign reversal**

In this case, the state-space matrix is modified as
\[
A = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}
\]
and \(a_1 = \begin{bmatrix} -(2(K'_{P3} + K'_{I3})\sigma(\phi_k)) \\ -(2(K'_{P3} + K'_{I3})\sigma(\phi_k)) \end{bmatrix}\).

Accordingly, the condition on loop-filter values for decreasing energy is derived as (20), using \(\Delta V_{k+1} \) expression from (19).
\[
\Delta V_{k+1} < 0
\]
\[
 \Rightarrow 1001(2K'_{P3} + K'_{I3})^2 - 2(\phi_k + 1001\Delta \phi_{f,k})(2K'_{P3} + K'_{I3}) + K'_{I3}\sigma(\phi_k) + (\phi_k^2 + \Delta \phi_{f,k}^2 + \phi_k \Delta \phi_{f,k}) < 0.
\] (20)

**Case II: Similar phase error sign in consecutive cycles**

Here, the state space matrix is modified as \(A = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}\) and \(a_2 = \begin{bmatrix} -K'_{I3}\sigma(\phi_k) \\ -K'_{I3}\sigma(\phi_k) \end{bmatrix}\). For these values of state matrix, the energy change rate, defined in (19), is obtained as
\[
\Delta V_{3,k+1} = 1001(K'_{I3})^2 - 2(\phi_k + 1001\Delta \phi_{f,k})K'_{I3}\sigma(\phi_k) + (\phi_k^2 + \Delta \phi_{f,k}^2 + \phi_k \Delta \phi_{f,k}).
\] (21)

Equation (21) indicates that the system’s energy decreases in Quadrants (I)/(III) but increases in Quadrants (II)/(IV) of the phase plane. The increase/decrease of energy in different quadrants, is of the same order \((2002K'_{I3})\Delta \phi_f - |\phi|\Delta \phi_f|\) for similar magnitude of \(|\phi|\Delta \phi_f|\).

Thus, from the above two cases, it is visible that the system’s energy function has oscillatory response in phase-plane regions excluding phase error switching axis. Since the energy function based on phase error is changing only on \(\Delta \phi_f\)-axis vicinity, the Lyapunov function is evaluated only at phase error switching instant, as per Case I.

**E. Loop Gain constraint from Lyapunov Function**

In the DPLL under consideration, BBPD based NLTI sub-system is activated only when the phase error goes below a value that could be detected by the inverter based TDC. In CMOS65nm-LL technology, a single inverter delay of 20 ps with reference clock of 100MHz, corresponds to the phase-error \((\phi_{err,x})\) of 0.01 radians. For BBPD based DPLL activated in region \((|\phi_k|, |\Delta \phi_k|) < (0.01\text{ rad},0.01\text{ rad})\), the stability condition is derived for \((|\phi_k|_{\text{max}},|\Delta \phi_k|_{\text{max}})\) in Quadrants (I)/(III) of the phase-plane. As stated earlier, the state-space equations (12) show that the system’s trajectory moves in clockwise direction and the phase error sign reversal occurs only in the quadrants where \(\phi_k\) and \(\Delta \phi_k\) have similar sign. Thus, the constraint on loop-gain \((K'_{P3},K'_{I3})\) is derived by replacing \((|\phi_k|_{\text{max}},|\Delta \phi_k|_{\text{max}})\) values in (19) with \((0.01\text{ rad},0.01\text{ rad})\) for this DPLL design, as shown in (22).
\[
1001(2K'_{P3} + K'_{I3})^2 - 20.02(2K'_{P3} + K'_{I3}) + 0.0003 < 0
\]
\[
\Rightarrow 0.00001 \text{ rad} < (2K'_{P3} + K'_{I3}) < 0.02 \text{ rad}
\] (22)

The stability condition is required to be satisfied only outside the limit-cycle region i.e. \((\phi_k_{\text{min}},|\Delta \phi_k|_{\text{min}}) \approx (2K'_{P3} + K'_{I3},2K'_{P3} + K'_{I3}).\) Hence, the loop-filter parameters can be derived from (22) as per chosen Lyapunov candidate function. The loop gain values \((K'_{P3},K'_{I3})\) calculated from the linearized approximation of BBPD based DPLL in (17) also satisfies the negative derivative condition on Lyapunov function.

The phase-portrait of BBPD based DPLL in Fig.12 shows that with the choice of loop gain \(K'_{P3}/K'_{I3}\), either settling time or jitter (from bang-bang operation) could be reduced at the expense of other. Figure 13 shows a decreasing energy plot for this subsystem, with Lyapunov function being calculated only on phase-error sign-reversal boundary.

![Phase-portrait of DPLL in BBPD mode with loop gains](image)

**F. Limit Cycle Stability**

Multiple Lyapunov functions are associated with the transitions in the hybrid system so that the trajectory is shown to converge to the switch points of the limit cycle. The multiple QLF aims to focus on a local behaviour of the system in each region. Construct a Lyapunov function outside the LaSalle’s invariant set. This approach only evaluates the global stability.
of the system, while neglects the detailed behaviour within the invariant set.

There exist a stable limit cycle to which the continuous trajectory converge.

For a standalone BBPD based DPLL, the stability analysis in [14] suffices to derive the loop filter gain from (17). However, for BBPD based DPLL incorporated in a switched system, its Lyapunov function search is still required to prove overall system’s stability using Multiple Lyapunov Functions approach.

VI. BBPD+FSM BASED DPLL STABILITY

During the locking process in the considered DPLL, when the phase error ($|\phi_k|$) reduces below $\phi_{err} (=0.01 \text{ rad})$ boundary, the system switches from LTI-subsystem to BBPD+FSM mode. With the activation of FSM, the derivative gain of Differentiator state is initialized with a value ($K_{D,I,init}$) required for the remaining phase error correction. For an immediate phase correction within bounds, the derivative gain is decremented ($K_{D,k}/\beta$) by FSM-Differentiator state, during each phase error sign-reversal. In this FSM, an additional accumulator ($K_{I,fsm}$) is activated for fast frequency tracking when consecutive cycles have same phase-error sign. The state switches from BBPD+FSM mode to BBPD based NLI subsystem, when the derivative gain ($K_{D,k}$) is reduced to a value of 1. The deactivation of FSM ensures that the limit-cycle region of DPLL doesn’t extend beyond the area due to BBPD operation, thus improving the PLL jitter performance. The state-space equation for FSM-Integrator stage and FSM-Differentiator stage is described in (23) and (24) respectively.

$$
\phi_{k+1} = \phi_k + \Delta \phi_{f,k} - K_{P3} \sigma(\phi_k) - K_{I3} K_{I,fsm} \sigma(\phi_k)
$$

$$
\Delta \phi_{f,k+1} = \Delta \phi_{f,k} - K_{P3} \sigma(\phi_k) - K_{I3} K_{I,fsm} \sigma(\phi_k)
$$

$$
K_{I,fsm,k+1} = K_{I,fsm,k} + 1
$$

$$
\phi_{k+1} = \phi_k + \Delta \phi_{f,k} - K_{D,k}(K'_{P3} + K'_{I3}) \sigma(\phi_k)
$$

$$
\Delta \phi_{f,k+1} = \Delta \phi_{f,k} - K_{D,k}(K'_{P3} + K'_{I3}) \sigma(\phi_k)
$$

Figure 14(a) shows the diverging trajectory of FSM-Integrator based DPLL governed by its state-space equations. Figure 14(b) shows the stability of FSM-Differentiator state with its negative energy-derivative rate calculated as per Lyapunov function defined in (18).

The presence of an additional integrator in the loop, as one of the FSM states, makes the system unstable during its activation period. Therefore, it is important to analyze the loop under this brief instability, with a fixed switching law defined by the FSM. With the FSM controlling the DPLL, unstable integrator state is either followed by LTI-subsystem activation (for $|\phi_k| > 0.01 \text{ rad}$) or with Differentiator-state activation (for $\phi_k$ sign-reversal). Accordingly, for stability analysis, Lyapunov function ($V_i$) is derived for (i) Integrator+LTI subsystem and (ii) Integrator+Differentiator subsystem, only in the suitable region of activation of each state. The overall system can then shown to be asymptotically stabilizable, if $V_i$ at the beginning of each interval on which the $j^{th}$ subsystem is active is not exceeding the value at the beginning of the previous such interval.

As discussed in Section V the system’s trajectory described by (23) moves in clockwise direction on the phase-plane. Thus, Integrator+LTI subsystem is evaluated in Quadrants III of phase-plane where $|\phi_k|$ increases, and Integrator+Differentiator subsystem is activated in Quadrants II/IV where $|\phi_k|$ decreases. Figure 15 shows the initial-point and end-point range along with the region of activation of each subsystem.

Following section discusses stability analysis of FSM-states for region having $|\phi_k|, |\Delta \phi_{f,k}| < 0.01 \text{ rad}, 0.01 \text{ rad}$, because beyond this region, correction ($K'_{P3}, K'_{I3}$) offered by the FSM-enabled subsystems is negligible in comparison to ($|\phi_k|, |\Delta \phi_{f,k}|$). Across this region, the loop trajectory is mainly governed by state-space equations of LTI subsystem.

A. Integrator+LTI subsystem stability

In Quadrants I-III, starting from any arbitrary point, system’s trajectory follows Integrator state-space equations defined in (23) for $|\phi_k| < 0.01 \text{ rad}$, and LTI state-space equations defined in (2) for $|\phi_k| > 0.01 \text{ rad}$. Based on the filter gain derived from Sections IV-V, the system trajectory could be predicted. Figure 16 shows that for $|\Delta \phi_{init}| < 0.001 \text{ rad}$, the loop does not switch to LTI-mode as phase error remains restricted below $|\phi_{err}|$. With the chosen filter gain values as in Table IV, the range of initial and terminating points for this subsystem’s trajectory are:

![Fig. 15: BBPD+FSM based DPLL phase plane divided into regions where (i) Integrator+LTI subsystem is active, or (ii) Integrator+Differentiator is active.](image-url)
\[ |\phi_{\text{init}}|_{\text{min}} \approx 0 \text{ rad}, |\phi_{\text{final}}|_{\text{max}} = 0.01 \text{ rad}, \\
0.001 \text{ rad} < |\Delta \phi_{\text{init}}| < 0.01 \text{ rad} \]

Consider the energy function \( V_{1,k} \) defined by (11) at switching-in point \((\phi_{\text{init}}, \Delta \phi_{\text{init}})\) and switching-out point \((\phi_{\text{final}}, \Delta \phi_{\text{final}})\) of this subsystem:

\[ V_{1,k} = 0.02 \phi_k^2 + 0.12 \phi_k \Delta \phi_{f,k} + 3 \Delta \phi_{f,k}^2. \]

For \(0.001 \text{ rad} < |\Delta \phi_{\text{init}}| < 0.01 \text{ rad}\), the system’s trajectory based on (23) converges to \(|\Delta \phi_{\text{final}}| < 0.002 \text{ rad}\), as shown in Fig. 17(a). Hence, for any arbitrary point in the above defined range, \(n^{th}\)-derivative of Lyapunov function \( \Delta V_{1,(k+n)-k} \) calculated as the energy difference at initial and terminating point of the subsystem is negative. This shows that energy increment in the loop caused by unstable integrator state is overcome by the large gain of LTI-subsystem. The energy decrement pattern across trajectory defined by Integrator+LTI subsystem is shown in Fig 17(b).

**B. Integrator+Differentiator subsystem stability**

With the phase-error decrease in Quadrants II-IV, the system’s trajectory follows Integrator state-space equation (23) for \(0 \text{ rad} < |\phi_{\text{err}}| < 0.01 \text{ rad}\), and Differentiator state-space equation defined by (24) on phase-error sign-reversal. Since BBPD+FSM mode is activated in the DPLL only for \( |\phi_{\text{err}}| < 0.01 \text{ rad}\), the initial derivative gain \((K_d,\text{init})\) stability is evaluated in this region. As per (24), FSM-Derivative state gives a constant correction of \( K_{D,\text{init}}(K_{P3}^r + K_{I3}^r) \) to the loop irrespective of whether the current point in state-space is near the equilibrium region or away from it. In case, the PLL is already near the locked region, a large derivative gain will increase the energy in the system instead of reducing it. Figure 17 highlight that the Integrator+LTI subsystem is able to reduce phase-error to a magnitude of 0.002 rad in the implemented DPLL. For providing further correction, the derivative gain is decided with condition as

\[ 0.002 \text{ rad} < K_{D,\text{init}}(K_{P3}^r + K_{I3}^r) < 0.01 \text{ rad}. \]  

For FSM based DPLL to have settling response analogous to binary-search algorithm, \( K_{D,\text{init}} \) is chosen as mid-point of the range defined by (25) i.e. \([K_{D,\text{init}}(K_{P3}^r + K_{I3}^r) \approx 0.005 \text{ rad}].\)

While BBPD+FSM mode is active, this derivative gain is reduced by a factor of \( \beta \) at each phase error sign-reversal instant to reduce the limit-cycle region in locked state. The derivative gain reduction factor is chosen as 2 in this design, so that the loop trajectory could be eventually placed in the bounded region of FSM-Integrator state, as shown in Fig. 16 and Fig 18(a). Within this bounded region of Integrator state, the phase error remains below 0.01 rad which ensures that the system doesn’t switch back to LTI-mode again. Figure 18 shows that with chosen \( K_{D,\text{init}} \), the phase or frequency error decreases at switching-out point in comparison to the switching-in point of this subsystem, with Lyapunov function being

\[ V_{1,k} = 0.02 \phi_k^2 + 0.12 \phi_k \Delta \phi_{f,k} + 3 \Delta \phi_{f,k}^2. \]

**VII. DPLL STABILITY AS SWITCHED SYSTEM**

Figure 2 shows that based on the magnitude of the phase-error \(|\phi_{\text{err}}|\) the system switches between PFD based LTI-mode, BBPD+FSM based NLTV-mode or standalone-BBPD based NLTI mode. Once the phase-error decreases below \(|\phi_{\text{err}}|\) boundary, the BBPD+FSM is activated introducing either Integrator+LTI subsystem or Integrator+Differentiator subsystem, based on the quadrant where current-state of system is positioned. Table IV highlights that PFD based LTI-systems with an adaptive loop bandwidth and BBPD based FSM could be designed with common Lyapunov function \( V_{1,k} \), thus assuring stability for arbitrary switching between these subsystems. The stability condition for BBPD based...
### TABLE IV

**Lyapunov Functions for DPLL subsystems mode**

| DPLL Subsystems          | Lyapunov Functions                                                                 | Activation Region | Loop Filter Gain |
|--------------------------|-------------------------------------------------------------------------------------|-------------------|------------------|
| LTI-1                    | \( V_{1,k} = 0.02\phi_k^2 + 0.12\phi_k \Delta \phi_{f_{c,k}} + 3\Delta \phi_{f_{c,k}}^2 \) | \( \phi_{err} > 1\text{rad} \) | \( K_{P1}' = 0.03\text{rad} \), \( K_{I1}' = 0.007\text{rad} \) |
| LTI-2                    | \( V_{1,k} = 0.02\phi_k^2 + 0.12\phi_k \Delta \phi_{f_{c,k}} + 3\Delta \phi_{f_{c,k}}^2 \) | \( 1\text{rad} > \phi_{err} > 0.01\text{rad} \) | \( K_{P2}' = 0.05\text{rad} \), \( K_{I2}' = 0.003\text{rad} \) |
| Integrator+LTI-2         | \( V_{1,k} = 0.02\phi_k^2 + 0.12\phi_k \Delta \phi_{f_{c,k}} + 3\Delta \phi_{f_{c,k}}^2 \) | \( \phi_{err} < 0.01\text{rad} \) | (Evaluated at switching-in and switching-out point) \( (K_D > 0, \text{Quadrant I/III}) \) |
| Integrator+Differentiator| \( V_{1,k} = 0.02\phi_k^2 + 0.12\phi_k \Delta \phi_{f_{c,k}} + 3\Delta \phi_{f_{c,k}}^2 \) | \( \phi_{err} < 0.01\text{rad} \) | \( K_{D,\text{init}} = 64 \) (Evaluated outside limit-cycle region) \( (K_D = 0) \) |
| BBPD based NLTI          | \( V_{3,k} = \phi_k^2 + 1000\Delta \phi_{f_{c,k}}^2 \) | \( \phi_{err} < 0.01\text{rad} \) | \( K_{P3}' = 0.00006\text{rad} \), \( K_{I3}' = 0.0000078\text{rad} \) |

DPLL is derived with Lyapunov function \( (V_{3,k}) \) defined in (18). The Integrator+Differentiator state ensures that the DPLL is placed in limit-cycle region, thus avoiding chattering phenomenon out of BBPD mode. Figure 19 shows the trajectory convergence of switched-DPLL system while traversing through phase-plane regions governed by different subsystems.

**VIII. Measurement Results**

The switched DPLL system, discussed in this work, is implemented in CMOS65nm-LL technology with chip micrograph as shown in Fig 20. Figure 22 highlights the settling response of the DPLL with loop gain parameters derived based on the stability analysis discussed in this work. Figure 23 shows that the DPLL achieves lock without chattering between different subsystems, thus constraining the output jitter only by the limit cycle region of BBPD based NLTI mode.

Figure 24 highlights a competitive Figure of Merit \( (\text{FoM}) \) [15] and best lock time being achieved by the fractional-N DPLL incorporating the switched loop technique in the feed-forward path. The Figure of Merit used for DPLL performance benchmarking is given as

\[
\text{FoM} = 10\log \left[ \frac{\sigma_t}{1s} \right]^2 \left[ \frac{t_s}{1s} \right]^2 \left[ \frac{P}{1\text{mW}} \right],
\]

(27)

where \( \sigma_t \) is the output jitter, \( t_s \) is the lock time and \( P \) is the power consumption of the DPLL.

**IX. Conclusion**

This work highlights the stability analysis using Lyapunov function towards deriving the loop parameters for a switched
DPLL system. The DPLL phase plane is partitioned into regions based on the phase-error state dependent switching across different subsystems. Multiple Lyapunov functions are used towards deriving the stability conditions for these subsystems. The measured fast settling response of the DPLL implemented with derived loop parameters, proves that the system achieves phase-lock without chattering phenomenon between different subsystems. The illustrated stability analysis for the DPLL unfurls the possibility of engaging an unstable integrator or an impulsive differentiator, without risking the convergence of the system.

The discussed stability analysis only verifies the loop convergence for a predefined switching rule and loop gain values obtained from first-order approximations. As a future scope to this work, an analysis could be developed to derive an optimum state-dependent switching rule and loop gain values for attaining maximum performance from the loop-order switching in a DPLL.

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