Drain Voltage Scaling in Carbon Nanotube Transistors

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While decreasing the oxide thickness in carbon nanotube field-effect transistors (CNFETs) improves the turn-on behavior, we demonstrate that this also requires scaling the range of the drain voltage. This scaling is needed to avoid an exponential increase in Off-current with drain voltage, due to modulation of the Schottky barriers at both the source and drain contact. We illustrate this with results for bottom-gated ambipolar CNFETs with oxides of 2 and 5 nm, and give an explicit scaling rule for the drain voltage. Above the drain voltage limit, the Off-current becomes large and has equal electron and hole contributions. This allows the recently reported light emission from appropriately biased CNFETs.

Recently, it has been shown experimentally [1,2] as well as theoretically [3,4] that typical carbon nanotube field-effect transistors (CNFETs) [5] operate by changing the transmissivity of the Schottky barrier (SB) at the contact between the metal electrode and the nanotube (NT). Due to the sharp edge at the metal-NT contact and the quasi 1D-channel of the NT, this barrier can be thinned sufficiently with gate voltage to allow thermally-assisted tunneling of electrons or holes. This working principle has important implications for device performance, e.g. it leads to a different scaling of the turn-on gate voltage with oxide thickness than for conventional transistors. [2,6]

Typically, CNFETs have had thick gate oxides, requiring large gate voltage for turn-on, and could be operated at drain voltages of 1 V or more. The performance of CNFETs can be systematically improved by reducing the thickness of the gate oxide. [2,6–8] However, we find that this places new constraints on the drain voltage. If the drain voltage is not scaled appropriately, reducing the oxide thickness can lead to minority-carrier injection at the drain, giving unacceptable Off-currents. The simultaneous electron and hole currents in this regime are of great interest for light-emission devices, [9] which have requirements opposite to SB-CNFETs. We derive explicit requirements for drain voltage scaling to obtain optimal device performance.

Our back-gated CNFET devices are produced using a two-step oxidation process which allows the formation of small ultra-thin oxide areas on which NTs are contacted, while keeping most of the substrate covered with thicker field oxide. The fabrication begins with 100 nm thick silicon nitride on top of a degenerately doped silicon wafer which serves as the backgate. Electron beam lithography (EBL) and reactive ion etching are used to pattern and remove the nitride except in micrometer-sized areas. The exposed silicon is covered by 120 nm thick, thermally grown field oxide. Silicon nitride is dissolved in phosphoric acid, and precisely controlled dry oxidation is used to deposit another 2 nm or 5 nm of silicon dioxide. Carbon nanotubes [10] are dispersed on these substrates, and source and drain connections to NTs located in areas of thin oxide are patterned using standard EBL and lift-off.

We focus on ambipolar devices, in particular those where the Fermi level at the metal-NT contact falls in the middle of the bandgap. Figure 1 shows typical transfer characteristics of current (I) vs. applied gate voltage (Vg) for different drain voltages (Vd) and oxide thicknesses (tox). All curves show the typical ambipolar characteristics, with hole current to the left of the minimum and electron current to the right. The gate voltage for minimum current shifts noticeably with drain voltage. Furthermore, we observe that at positive Vd the curves almost overlap for the electron current while they split for the hole current, and vice versa for negative Vd.

The minimum current as a function of Vg, i.e. the Off-
current ($I^{\text{Off}}$), rises steeply with increased absolute value of $V_d$. While the Off-current increase is clear in CNFETs with $t_{\text{ox}} = 5 \text{ nm}$, it is particularly worrisome for devices with $t_{\text{ox}} = 2 \text{ nm}$ where performance deteriorates already at $V_d \sim 0.6 \text{ V}$. (We note for comparison that the concurrently measured current leakage between the gate and source/drain electrodes are below 100 fA and 1 pA for CNFETs with $t_{\text{ox}} = 5 \text{ nm}$ and $2 \text{ nm}$, respectively.)

![Figure 2](image1.png)

**FIG. 2.** Effect of the drain field on the calculated $I$ vs. $V_g$ characteristics of a CNFET. (a) and (b) curves differ only by opposite sign of $V_d$. In (a), open and filled circles show current decomposed into hole and electron contributions, respectively, for $V_d = -0.8 \text{ V}$. Labeled points in (b) are discussed in text. The metal Fermi level is assumed to fall at midgap in the NT at the contact. The simulation parameters are: $t_{\text{ox}} = 2 \text{ nm}$, $L = 200 \text{ nm}$, the top gate is 120 nm from the NT, the contact thickness is 20 nm, and the contact has length 100 nm.

In order to understand these observations we use a semiclassical approach to calculate the total current through the device. For ballistic transport in the NT, [11] we can calculate the current with the Landauer-Büttiker formula:

$$I = \frac{4e}{h} \int \left[ F(E) - F(E - eV_d) \right] T(E) dE,$$

where $F(E)$ is the Fermi function. The energy-dependent transmission $T(E)$ through the device is controlled by the SBs at the source and drain contact. The transmission through the SBs are evaluated within the WKB approximation, using the idealized band structure [12] for a NT with $E_g = 0.6 \text{ eV}$ and diameter of 1.4 nm.

The shape of the SBs at the source and drain contact depend on the electrostatic potential along the NT. We calculate the potential by solving the Laplace equation for a device geometry with a bottom gate at $t_{\text{ox}}$ from the NT and a grounded top electrode which is far from the NT. Neglecting charge on the NT is a good approximation for the Off-state and the turn-on regime. [3,6]

Figure 2 shows the calculated transfer characteristics at various drain voltages, for a device geometry as in the experiment. The effect of drain voltage on the current characteristics for ideally ambipolar devices is clearly captured by the model. We see the splitting of the curves for the electron branch at negative $V_d$ and for the hole branch at positive $V_d$ as in the experiment. Moreover, in the model, the gate voltage giving minimum current is exactly half the applied drain voltage, and the current is symmetric about this gate voltage $V_g = V_d/2$. The shift of the current minimum in the experiment, Fig. 1, is in approximate agreement with this prediction. (The quantitative current is sensitive to details of the contact geometry, and the sharper turn-on in the theory may result from an assumed geometry more favorable than the actual one. [6])

![Figure 3](image2.png)

**FIG. 3.** Band diagrams for the simulations shown in Fig. 2, with $V_d = +0.8 \text{ V}$ and $V_g = +0.7 \text{ V}$ (solid line), +0.4 V (dashed), and +0.1 V (dotted), corresponding to points labelled A, B, C respectively.

Calculated band diagrams for different voltage regimes are displayed in Fig. 3. In the long channel limit ($L/t_{\text{ox}} \gg 1$) the electric field, as well as the transmissivity of the source and drain contacts, should only depend on the two potential differences $V_g$ and $V_d - V_g$. In a sense, the device acts as two SBs connected by a field-free region in the bulk of the nanotube. At large positive $V_g$, labeled by point A in Fig. 2(b) and the solid line in Fig. 3, the CNFET is in the On-state. Because $V_g \sim V_d$ at point A, the bending at the drain is insignificant, and the current is controlled by the source barrier. [3,4] As the gate voltage is decreased, the SB at the source becomes wider and thus the electron tunneling current is lowered. However, the potential drop at the drain electrode, $V_d - V_g$, increases. At $V_g = V_d/2$ (B) both SBs have the same shape and there is an equal contribution of electron and hole injection. If $V_d/2$ is close to or above the turn-on voltage, these currents can be significant and the device cannot be turned off. (In this regime, electron-hole recombination can lead to polarized light emission from an individual semiconducting nanotube. [9])

For symmetric source and drain contacts, as in the calculation, the electron current rises monotonically with $V_g$ exactly as the hole current increases monotonically with $V_d - V_g$, Fig. 2(a). Therefore, the total current becomes
minimal at $V_g = V_d/2$. As the gate voltage is further decreased (C) the hole current at the drain dominates the current through the device. This drain field induced current results in a severely deteriorated Off-current. We calculate that for $V_d = 1$ V, the On/Off ratio ($I_{On}/I_{Off}$) decreases from about $10^4$ at $t_{ox} = 50$ nm to less than $10^2$ at 2 nm.

However, for operation of the devices as transistors an On/Off ratio of about $10^4$ is desirable. Using an analytic model for the scaling of the current with $t_{ox}$ [6], we obtain an explicit rule for $V_d$ to meet this criterion. The upper limit is given by $V_d = 0.3 \sqrt{t_{ox}}$ nm V for the simulated bottom-gate devices. The scaling as $\sqrt{t_{ox}}$ is a consequence of the same scaling for the turn-on voltage. [6] (For experimental CNFETs the allowed $V_d$ may be a little larger due to a less favorable contact geometry, but the same scaling rule will still hold.) For $t_{ox} = 2$ nm, we find that to have an On/Off ratio of at least $10^4$ requires $V_d \leq 0.4$ V.

![FIG. 4. Output characteristic for devices with $t_{ox} = 2$ nm. (a) Experimental data for NT with $L = 60$ nm. Different regimes labelled C, D, and E correspond to those in Fig. 2. (b) Calculated output characteristic in the long channel limit. (c) Short-channel device with symmetric geometry. (d) Short-channel device with asymmetric geometry.](image)

The drain voltage induced minority carrier current also affects the device output characteristics ($I$ vs. $V_d$) as shown in Fig. 4(a). Instead of being Off near zero gate voltage [regimes D and E in Figs. 2 and 4(a)], a large potential difference at the drain induces an exponential increase of the current (regime C) in the device. This can result in crossing of $I$ vs. $V_d$ at different values of $V_g$, a behavior not observed in conventional transistors. The corresponding increase in Off-current puts an upper bound on the useable range of $V_d$ at about 0.5 V, in agreement with our estimate for the feasible On/Off ratio.

Figure 4(b) shows that the general crossover trend of $I$ vs. $V_d$ curves at different $V_g$ is captured by the simulations of a long channel device which mirrors the geometry of the measured CNFET. However, the experimental data more closely resembles the short-channel device obtained when the NT length is decreased (from 60 nm) to 20 nm [Fig. 4(e)]. Apparent short-channel effects in our devices occur at larger $L/t_{ox}$ ratios than in the simulations, perhaps due to differences in geometry, or to other unrecognized effects. The closest agreement [Fig. 4(d)] can be obtained by assuming that the impact of the gate is slightly better at the source than the drain, due to e.g. slight variations in oxide thickness or contact geometry. It is important to note that while these details of the geometry affect the output characteristics, they do not change our conclusions on the exponential increase in Off-current or the splitting of the $I$ vs. $V_g$ curves with $V_d$.

Our discussion has been limited to a midgap line-up of the metal Fermi energy with the NT bands, and a bandgap of 0.6 eV. However, we confirmed that the drain voltage induced current is a significant issue for ultra-thin oxide CNFETs even for asymmetric line-ups or different band gaps. Thus the limit in drain voltage will scale quite generally as the turn-on gate voltage, which gives a square-root scaling for the device geometries we have studied. [6] Above the drain voltage limit, the device can be used as a light source [9] by operating it at the Off-voltage ($V_g = V_d/2$) where the current consists of equal electron and hole contributions.

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