Comparison of Single-Event Transients of T-gate Core and IO device in 130 nm Partially Depleted Silicon-on-Insulator Technology

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Abstract: Many papers have confirmed that the single event vulnerability of semiconductor devices significantly increase with power supply voltage drop, rendering considerable challenges for the radiation harden design as per the development of Moore’s law. The higher the supply voltage of the chip scaling down, the greater severity of these problems. In this article, SET pulse widths induced by heavy ion of T-gate 1.2V Core and 3.3V IO devices fabricated by a 130nm partially depleted silicon-on-insulator technology were directly measured. We discovered that, by adjusting the design parameters and choosing an appropriate device W/L ratio, different power supply voltage SOI devices are able to achieve the same sensitivity for the single event, irrespective of supply voltage. The distribution of SET-pulse widths ranges from 210 to 735 ps under a constant LET of 37.6 MeV·cm²/kg, and the single event transient vulnerability of T-gate 1.2V Core and 3.3V IO devices is similar, which is instructive for the low-voltage and low-power circuit application.

Keywords: direct measurement, heavy ion irradiation, silicon on insulator technology, single event transient, MOSFET, radiation harden by design.

Classification: Electron devices, circuit, and systems

References

[1] P. E. Dodd, M. R. Shaneyfelt, J. A. Felix, and J. R. Schwank, “Production and propagation of single-event transients in high-speed digital logic ICs,”IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3278–3284, Dec.2004.
[2] O. Rozeau, J. Jomaah, J. Boussey, C. Raynaud, J. L. Pelloie, and F. Balestra,
“Impact of floating-body and BS-tied architectures on SOI MOSFETs radio-frequency,” in Proc. IEEE SOI Conf., 2000, pp. 124–125.

[3] J. B. Kuo and S.-C. Lin, Low-Voltage SOI CMOS VLSI Devices and Circuits. New York: Wiley, 2001, p. 339.

[4] N. K. Annamalat, “Leakage current in SOI MOSFETs,” IEEE Trans. Nuclear Sci., vol. 35, no. 6, pp. 1372–1378, Jun. 2004.

[5] P. Eaton, J. Benedetto, D. Mavis, K. Avery, M. Sibley, M. Gadlage, and T. Turflinger, “Single event transient pulsewidth measurements using a variable temporal latch technique,” IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3365–3368, Dec. 2004.

[6] Narasimham B, Ramachandran V, Bhuva B, et al. On-chip characterization of single-event transient pulse widths. IEEE Trans Device Mater Rel, 2006, 6(6):542

[7] P. Gouker, J. Brandt, P. Wyatt, B. Tyrrell, A. Soares, J. Knecht, C. Keast, D. McMorrow, B. Narasimham, M. Gadlage, and B. Bhuva, “Generation and Propagation of Single Event Transients in 0.18 μm Fully Depleted SOI,” IEEE Transactions on Nuclear Science, vol. 55, 2008, pp. 2854-2860.

[8] M. J. Gadlage et al., “Single Event Transient Pulse Width Measurements in a 65-nm Bulk CMOS Technology at Elevated Temperatures,” Proc. 48th Annu. IEEE International Reliability Physics Symp. (IRPS), pp. 763-767, May 2010.

[9] M. Gadlage, P. Gouker, B. Bhuva, B. Narasimham, and R. Schrimpf, “Heavy Ion Induced Digital Single Event Transients in a 180 nm Fully Depleted SOI Process,” IEEE Transactions on Nuclear Science, vol. 56, 2009, pp. 3483-3488.

[10] V. F. Cavrois et al., "Investigation of the Propagation Induced Pulse Broadening (PIPB) Effect on Single Event Transients in SOI and Bulk Inverter Chains," IEEE Transactions on Nuclear Science, vol. 55, no. 6, pp. 2842-2853, 2008.

[11] V. Ferlet-Cavrois, G. Gasiot, C. Marcandella, C. D’Hose, O. Flament, O. Faynot, J. du Port de Pontcharra, and C. Raynaud, “Insights on the transient response of fully and partially depleted SOI technologies under heavy-ion and dose-rate irradiations,” IEEE Trans. Nucl. Sci., vol. 49, no. 6, pp. 2948–2956, Dec. 2002.

[12] Christopher F. Edwards, William Redman-White, et al. The effect of body contact series resistance on SOI CMOS amplifier stages [J]. IEEE Transaction on Electron Devices, 1997,44(12):2290-2293.

1 Introduction

As a result of decreased cross section per transistor, higher operating speeds, and lower charge collection, the silicon-on-insulator (SOI) technology demonstrates inherent strengths over bulk technologies. Prior studies demonstrated that, in comparison to similar bulk technologies, SOI technologies generate sharper and shorter widths of single-event transient pulse [1]. Although SOI floating-body structures may be more effective as a result of the decreased source/gate capacitance [2], the contacts of body are required in order to cure physical instability in partially depleted (PD) SOI devices, particularly in reference to analog application [3]. The structures of physical contact, such as T-gate SOI MOSFET devices, are designed to restrain the parasitic bipolar transistor effects and the kink effects [4].
In this paper, the T-gate Core and IO device width-evaluation results of single-event transient (SET) pulses within a 130nm partially depleted silicon-on-insulator technology are reported. An on-chip self-triggering snapshot circuit has been developed to measure the T-gate device SET-pulse widths. In contrast to the variable temporal latch technique, it is then feasible to directly evaluate the SET-pulse widths and gain the corresponding distribution of histogram with no conversion of data [5]. The SET-pulse width histogram can be offered by means of the variable temporal latch technique through differentiation of the collected experimental data. However, the processing of this conversion would merely result in a lower statistical accuracy. A similar evaluation approach utilizing a self-triggering circuit has been employed [6]. However, the heavy-ion-induced SET-pulse evaluations in 130nm Partially Depleted SOI technology were not performed.

The experiment details, including test chip description, are introduced in Section 2. Discussions of Experimental results and TCAD simulation results are outlined in section 3. Finally, a conclusion is presented in Section 4.

2 Test chip and Experiment

130nm partially-depleted SOI CMOS devices with a T-shape gate are examined for SET sensitivity in this experiment. This high-performance technology features a 2nm gate oxide, with a 100nm silicon layer thickness thin-film SOI. Figure 1 illustrates the layout of a standard T-gate NMOS device. The devices are fabricated on Smart-Cut® Wafers, a 150nm buried oxide, 1.2V core device and 3.3V IO device.

![Fig. 1. Layout geometry for T-gate NMOSFET.](image)

![Fig. 2. Overall test circuit for T-gate 1.2V Core and 3.3V IO devices SET-pulse width measurement. The single-event transient pulse originating from under the test devices propagates through the entire test circuit and is finally captured by the circuits of Snapshot. The width of pulse is calculated as a bit affected sequence, for example “0...1101011...1”](image)
2.1. Test Circuit

Fig. 2 outlines the overall schematic of the test chip. It contains two circuit modules: one with an inverter chain of T-gate MOSFET devices under test (left side in Fig. 2), and another with a pulse snapshot circuit (right side in Fig. 2). The pulse snapshot circuit captures single-event transient pulses generated in the SOI MOSFET devices. In order to collect a sufficient amount of SET pulses in the irradiation experiment, we implemented 8 identical test circuits in parallel on the chip. More details of each of the circuit modules are presented as follows:

1) Devices Under Test: The under test target MOSFET devices consisted of a linear inverter chain in which the SETs are generated. The input port of every inverter cell is attached to the output port of the prior cell. As a result, the pulse of SET can diffuse via the chain. Similar to the first inverter cell input port, the input port of the inverter chain is grounded. We used two chips, T-gate 1.2V core devices and 3.3V IO devices, to compare the results. Both of them are minimally sized inverters, for 1.2V core devices, the NMOS and PMOS width of each inverter is 0.3um and 1um, the etched gate length is 130 nm; and for 3.3V IO devices, the NMOS and PMOS width is 0.3um to 0.75um for each inverter, the etched gate length of 350nm.

2) Snapshot Circuit: The Snapshot circuit is comprised of a triggering signal control Flip-Flops chain and a trigger circuit. The trigger signal control Flip-Flops (TCFF) chain is a 30-stage inverter with a radiation-hardened DFF chain, which is controlled by a Pass/Hold signal to propagate/save the SET pulse. In the initial state, the hold signal is OFF, whereas the pass signal of trigger circuit is ON (the circuit depicted in Fig. 2). Thus, every inverter output of the TCFF chain is attached to the subsequent phases, enabling the pulse of SET to diffuse via the pass gates and inverters. It stimulates an SR flip-flop, which subsequently turns off all pass gates by freezing the data. In addition, it inverts the pass signal of the chain by turning the hold signal on when the leading edge of the SET pulse reaches the trigger circuit. The width of the SET pulse is directly proportionate to the amount of D Flip-Flop whose output is influenced. When the outputs of DFF have been read out, a reset signal is utilized to hold the signals, initialize the pass and prepare the circuit for the measurement of the following pulse [2]. In regards to heavy ion tests, the SET pulse width and hit stage cannot be separated; hence, one cannot ascertain whether the hit stage has completely recovered. If the under test stage has not recovered and the TCFF chain is triggered, the charge collection may still continue and the chain inverter stage will not completely recover. Thus, the measured width of the pulse may be shorter than the actual pulse. To address this uncertainty, we introduced a delay in the trigger circuit that was long enough to ensure a full recovery of the inverter stage.

The width of SET-pulse could be evaluated in the units of TCFF chain stage delay. In a range between \((n-0.5) \times \text{stage delay}\) and \((n+0.5) \times \text{stage delay}\), for all of the pulse widths, n is the influenced TCFF stage count [2]. Therefore, the formula as below can be used to evaluate the single-event transient pulse width \((T_W)\):
\[ T_w = \Delta T \times N_{FF} \pm \frac{\Delta T}{2} \]  

(1)

\( \Delta T \) represents the delay time of two stages in the TCFF chain, while \( N_{FF} \) represents the number of DFF stages affected by the SET pulse. The SET pulse width is accurate to within one-half of the stage delay.

The test structure is dedicatedly designed to ensure that only the SET pulses stemming from the devices (T-gate MOSFET) are being examined. As a result, the TCFF chain output is not affected by a hit on the stage beyond point X (as depicted in Fig. 2). The trigger circuit and Flip-Flops were radiation hardened in order to remove the upsets of a single event in the entire snapshot circuit. Therefore, in the target device, only SET generated can be evaluated and in any other part of the circuit, the ion hits cannot be measured.

2.2. Irradiation Environment

We performed heavy ion tests at Heavy Ion Research Facility in Lanzhou (HIRFL). Irradiation conditions are summarized in Table I.

| Device       | Ion     | Energy [Mev] | LET [MeV·cm²/mg] | Flux (Averaged) [particles/(cm²·s)] |
|--------------|---------|--------------|------------------|-----------------------------------|
| T-gate MOSFET | ⁸⁶Kr    | 479.8        | 37.6             | \(1.0 \times 10^5\)                |

In order to measure the SET pulses in a space environment, we employed the constant LET of 37.6 MeV·cm²/mg. In order to reach the effective LET of 37.6 MeV·cm²/mg, at a 90° angle, ⁸⁶Kr was irradiated and we discontinued the irradiation when the fluence reached \(1.0 \times 10^7\) particles/cm² at the surface of the chip.

3 Results and discussion

3.1. Results of Heavy Ion Test

A heavy-ion broad beam testing of PDSOI T-gate device SET test chips was performed at the Heavy Ion Research Facility in Lanzhou (HIRFL), with the 479.8 MeV ion cocktail utilizing krypton (Kr) in air at a normal incidence. For all the findings delineated in this article, the particle energy and incident angle maintained stable. The irradiation environment and test set-up are illustrated in Fig.3. The system is predominantly composed of four parts: test chips, an FPGA control board, a logic analyzer and a terminal control computer.

Fig. 3. System of SET-pulse Measurement and Irradiation Environment.
30 inverter stages with D Flip-Flop are utilized by the pulse Snapshot Circuit in order to store the number of inverters affected by each SET. Hence, the SET width is assessed in the units of inverter & DFF chain delay. We calibrated the TCFF chain delay time prior to the irradiation test. To measure the chain individual stage delay $\Delta T$, a ring-oscillator testing circuit with the same 500-stage inverter & radiation-hardened DFF chain was created. Under the nominal operating voltage 1.2V, the chain delay time is approximately 105ps. This signifies that the test chip could measure single-event transient pulses ranging from 105ps to 3.15ns, with a 52.5ps (one-half of the chain individual stage delay) measurement resolution [6]. In addition, greater broadening effects of pulse for SOI and Bulk Inverter Chains have been demonstrated in prior works [7-10]. According to the statistics from the SOI process of 180 nm, the SET pulse and floating-body transistors will widen around 3 ps for each inverter. Therefore, we primarily use a 10-stage inverter and 30-stage TCFF chain to reduce the influence of Propagation Induced Pulse Broadening (PIPB) on the measurement accuracy.

Fig.4 demonstrates the histogram of the measured SET-pulse widths for two test chip devices. The counts of SET pulses collected in the 8 circuits of testing are plotted as a function of pulse width $T_W$. The width of SET-pulse can be found in a scope between 210 and 735ps, with a vertex around the distributing center. Take T-gate 1.2V core devices inverter chain for example; the peak can be inferred in the scope between 262.5 ps and 367.5 ps. According to the distribution, the SET pulse widths change under continuous LET ion irradiation. This is a reasonable finding, taking into consideration the completely random ion struck locations in the test of irradiation, as well as the response of transient current variations that are in accordance with the ion struck location of the transistor (for example, a gate hit and a drain hit [11]). Although a 3.3V IO device supply voltage is approximately three times that of the 1.2V core device, the channel length of the 3.3V IO device is also approximately three times that of the 1.2V core device (1.2V device channel length is 0.13um, 3.3V device channel length is 0.35um). Hence, the device electric field intensities of these channels are almost identical. Moreover, they have the same device structure, signifying that both devices have the same fundamental ability to collect charges induced by a single event, with a correspondingly similar distribution of pulse width.
Fig. 4. SET pulse histogram stems from T-gate 1.2V core devices (upper) and 3.3V IO devices (lower) chips. The SET pulse counts in the 8 circuits of testing are considered as an evaluated pulse width $T_W$ function.

3.2. TCAD Simulations

The simulations of mixed-mode technology computer aided design (TCAD) with 130nm PDSOI T-gate MOSFET devices have been conducted utilizing the Synopsys suite. The simulations aim to study the SET pulse width in response to heavy-ion strike on a single T-gate inverter, as compared to the chip measurement results.

![TCAD Simulations Diagram](image)

Fig 5. An illustration of the mixed-mode model used for the simulations. The second NMOS transistor in a four T-gate inverter chain is modeled in TCAD, while the remaining T-gate inverters are modeled in SPICE.
The PMOS and NMOS transistors were calibrated and modeled utilizing information collected during the process design kit (PDK) of 130nm PDSOI, SPICE model and I-V curves which were measured for the transistors fabricated within the technology of the 130nm PDSOI. According to Fig. 5, for the simulations, in a four minimally sized (1x) T-gate inverter chain, the off-state PMOS (or NMOS) transistor of the second inverter was modeled using TCAD. As for the strikes to the NMOS device, VIN was biased at VDD, prompting the second inverter NMOS to assume an OFF state. For strikes to the PMOS device, VIN was biased at GND, prompting the second inverter PMOS to assume an OFF state. We simulated SET pulse widths for the T-gate 1.2V core device and 3.3V IO device.

In order to trigger the T-gate body-contacted device, a contact resistance has been utilized to tie the body’s potential to the ground. The resistance of body contact is related to channel width and length, silicon thickness and silicon doping density. The device’s channel is in an “inversion state”. The following formula can be utilized to express the $V_{DS} = 0$V, the minimal body contact resistance $^{[12]}$

$$R_{body} = \frac{W_{eff}}{A_{eff}q\mu_pL_{eff} \left( t_{si} - \sqrt{\frac{4\epsilon_0\epsilon_{si}\phi_F}{qN_A}} \right)}$$

in which $t_{si}$ represents silicon thickness, $N_A$ refers to the doping density of the silicon body region, $\mu_p$ is indicative of the hole mobility, $\epsilon_0$ is vacuum dielectric constant, $\epsilon_{si}$ is Silicon relative permittivity, $q$ is the elementary charge, $\phi_F$ is Fermi potential and $L_{eff}$ and $W_{eff}$ refer to efficient channel length and width. It can be discerned that the 3.3V IO device has a relatively wide channel length, approximately 3 times wider than that of the 1.2V core device, and thus has a low body contact resistance.

![Fig 6. Simulated SET pulse widths under a constant LET of 37.6 MeV-cm$^2$/mg at the struck node for T-gate 1.2V Core and 3.3V IO devices. In the simulation, the ion hits at the gate center.](image)

The mixed-mode simulation results of the SET pulse are presented in Fig. 6. The ion hits at the gate center, with an LET of 37.6 MeV-cm$^2$/mg at normal
incidence. For an SOI device, this can be the most sensitive region. As evidenced in Fig. 6, the SET full-width half-rail (FWHR) pulse is approximately the same for both T-gate 1.2V core and 3.3V IO devices. The induced SET pulse width at this struck node in mixed mode simulation is about 300 ps. Although the evaluated width of SET is longer than the width of the simulated SET, the major objective of the simulation revealed in this part is to focus on the trends, as opposed to the actual width of SET pulse. Subsequently, it can be observed that the single event transient vulnerability of the T-gate 1.2V core device is similar to that of the 3.3V IO device. This simulation indicates that the SET pulse width is dependent upon the inverter PMOS and NMOS charge-discharge capacity, as well as the W/L ratio and load capacitance. It is affected less by power supply voltage.

![Fig 7](image-url)

**Fig 7.** Mixed-mode model simulated for the T-gate core and IO device, indicating the pulse width based on the location of the ion strike. The SET-pulse widths diminish rapidly with the strike location away from the gate center. At the center of the drain, no SET is generated at the ion hit. As for “Edge of the Gate” simulation, the location of ion strike is at the edge of the gate towards the drain regions.

In Fig. 7, the SET pulse widths are dependent upon the location of ion strike for the T-gate 1.2V core device and 3.3V IO device. The simulations are conducted under an LET of 37.6 MeV-cm$^2$/mg for the off-state transistor in a four minimally sized (1x) inverter chain. The pulse width, which can be considered as full-width half-rail (FWHR), is regarded as a location function. These simulations confirm that, due to ion strikes in the gate (body) regions, transients become wider than strikes in the drain region or around the edges of the gate. In the body region, the most sensitive regions (such as the region under the gate) induce the largest pulse widths in these SOI T-gate devices. These simulation results conform to the evaluated results, as evidenced in Fig. 4, which elucidates that the width of the SET-pulse can be distributed in a scope. The difference of the SET-pulse of core and IO devices, struck in closer proximity to the edges of the gate or in the drain region, may be due to the fact that the strike locations are not identical. Different device channel lengths result in different distances of strike position relative to the center (the coordinate system's origin). For the 1.2V device, the edge of the gate is 65nm from the center of the gate, and for the 3.3V device, the edge of the gate is
175nm from the center of the gate.

3.3. Circuit Verify
In order to examine SET-pulse widths distributed in a range of 210 ~735ps, we designed a verify chip using a T-gate MOSFET device. As depicted in Fig.8, the verify chip contains two different shift register chains, which are composed of 900 stages hardened DICE DFFs (DICE-FF) and hardened DICE DFF with 800ps delay filter (DFDICE-FF) respectively. We use hardened DICE-based DFFs to eliminate single event upset (SEU) in the DFF stages. The test structure is dedicatedly designed such that an SEU hit on any DFF stage storage nodes does not affect the shift register chain output, which ensures that the shift register chain output is solely affected by the SET-pulse. The delay filter is put on the D inputs in DFDICE-FF illustrated in Fig.8(c).

At normal incidence, the verify chip was performed with monoenergetic heavy ions collected from HIRFL, under identical irradiation conditions with the T-gate MOSFET device, as depicted in Table I. During testing, the shift register chains were clocked at 40MHz. As revealed in Fig.9, the results verify the effectiveness of the T-gate MOSFET SET-pulse width we measured in the article. The SET-pulse induced chain upset is less than 800ps, due to the delay filter, the DFDICE-FF has a lower amount of upsets than the DICE-FF for test chip. The DFDICE-FF reveals a 70% reduction in the cross section of single bit upsets, as compared to the DICE-FF chain at the LET of 37.6 Mev-cm²/mg. Nonetheless, according to Fig.9, DICEFFs suffer from SETs regardless of the fact that they are protected by the delay filters. This is a reasonable finding when taking into consideration the SET-vulnerability of the output in CK input and delay filter. As an ion strikes the output point of the delay filter, the data signal will be transformed and upset. While SET takes place on the input line of CK (presented in Fig.8(c)), a false rising edge can be generated and also can cause upsets.
4 Conclusion

The evaluation of heavy-ion-induced SET pulses of a T-gate Core and IO device in a 130nm partially depleted silicon-on-insulator process was compared in this article for the first time. By employing a self-triggering snapshot circuit, SET-pulse widths were evaluated directly. According to the results, the SET-pulse widths of T-gate devices were distributed in a scope between 210 and 735ps, with a peak around the distribution center. In addition, the single event transient sensitivities for the T-gate 1.2V Core and 3.3V IO devices are similar. The power supply voltage does not have a significant effect on the SET-pulse width. It was also indicated that the body region under the gate is the most sensitive region for the PDSOI T-gate device. We designed a validation chip shift register chain with the objective of verifying the SET-pulse measured results and validating the efficacy of the delay filter method for SET mitigation.

With the same Snapshot circuit employed in this paper, we are now testing other types of MOSFET devices under irradiation with various LETs. Variation in the pulse-width distribution, conditional upon device type or LET, will be reported in the future.