Abstract

We address the problem of optimizing mixed sparse and dense tensor algebra in a compiler. We show that standard loop transformations, such as strip-mining, tiling, collapsing, parallelization and vectorization, can be applied to irregular loops over sparse iteration spaces. We also show how these transformations can be applied to the contiguous value arrays of sparse tensor data structures, which we call their position space, to unlock load-balanced tiling and parallelism.

We have prototyped these concepts in the open-source TACO system, where they are exposed as a scheduling API similar to the Halide domain-specific language for dense computations. Using this scheduling API, we show how to optimize mixed sparse/dense tensor algebra expressions, how to generate load-balanced code by scheduling sparse tensor algebra in position space, and how to generate sparse tensor algebra GPU code. Our evaluation shows that our transformations let us generate good code that is competitive with many hand-optimized implementations from the literature.

Keywords Sparse Tensor Algebra, Optimization

1 Introduction

There has been a lot of interest in compilers for dense [3, 24, 29, 36, 40] and sparse [10, 17, 18] linear and tensor algebra. Dense tensor algebra compilers, such as TCE, TVM and Tensor Comprehensions, build on decades of research on loop transformations for affine loop nests [22, 44, 45]. Sparse tensor algebra compilers, on the other hand, suffer from a lack of analogous sparse loop transformation frameworks.

Without a loop transformation framework, sparse tensor algebra compilers leave several optimization opportunities on the table. First, sparse tensor algebra expressions are often really a mix of dense and sparse tensor algebra, where some operands are stored in sparse data structures and some in dense arrays. Examples include SpMV with a dense vector and (sparse matrix) × (dense matrix) multiplication (SpMM). Second, sparse tensors often have some dimensions that are dense, such as the blocked compressed sparse rows matrix format (BCSR) representing a sparse matrix that has dense blocks. Without a loop transformation framework, sparse tensor algebra compilers cannot optimize the dense loops in mixed sparse and dense expressions. Furthermore, current sparse tensor algebra compilers cannot apply loop transformations, such as strip-mine, reorder and collapse, to sparse loops. We will show that such transformations are possible and that they can be used to enable parallelization and make effective use of modern GPUs. Finally, we will show that by tiling the contiguous nonzero value arrays in sparse tensors, we can generate static load-balanced parallel code.

Applying loop transformations to sparse loops is challenging because they iterate over data structures. These data structures encode the coordinates of nonzero values and a single sparse loop may iterate over any number of them. In fact, the resulting imperative code may contain while loops, conditionals and indirect memory references. Furthermore, tiling loop transformations rely on the ability to jump around the iteration space, and sparse data structures may not support random access.

In this paper, we propose a unified loop transformation framework for loop nests with both dense and sparse loops that come from sparse tensor algebra. The loop transformations are applied to intermediate representations before generating imperative code. The transformations let us strip-mine, reorder, collapse, vectorize, and parallelize both dense and sparse loops subject to straightforward preconditions. Furthermore, our transformations enable sparse loops to be...
We show that our transformations let us generate good code analogous to the Halide scheduling language [29]. Unlike Halide, however, the transformations can apply to both sparse and dense loops from mixed sparse and dense tensor algebra expressions. We leave automatic scheduling—developing an optimization system to automatically decide loop transformations—as future work. Such systems can be built on top of the transformations we propose here. Finally, we show that our transformations let us generate good code that is competitive with hand-optimized kernels where these are available, that they let us target GPUs, and that they let us generate load-balanced kernels.

Our specific contributions are

1. position iteration spaces to complement the standard coordinate iteration spaces,
2. generalization of standard loop transformations to sparse loops,
3. dimension relationship graphs to track the dependencies between iteration spaces and data structures, and
4. a CUDA GPU backend for sparse tensor algebra enabled by sparse loop transformations.

## 2 SpMV Example

In this section, we demonstrate the capabilities of our loop transformation and code generation framework using a motivating example. Our main target is code expressing computations on mixed dense and sparse multidimensional tensors, but for simplicity we use the well-known example of matrix-vector multiplication: \( a = Bc \), in which a vector \( c \) (a one-dimensional tensor) is multiplied by a matrix \( B \) (a two-dimensional tensor).

When all operands are dense, the code is straightforward. Figure 2a shows matrix-vector multiplication with dense operands; the loops shown are easy to optimize, since they iterate over a regular data structure. However, when the matrix is sparse, as shown in Figure 2b, iterating through the entries of the matrix becomes more complex. This is due to the fact that sparse matrices are most often stored in compressed structures\(^1\), which avoid storing zero entries (more details about matrix storage are given in Section 3).

The combination of complex iteration and indirect storage, common to most sparse matrix formats, makes subsequent loop transformations more difficult for sparse matrix-vector multiplication (SpMV).

In the simplest case, shown in Figure 2c, it is possible to tile SpMV by tiling the outer dense loop. This code is suitable for further optimizations such as parallelizing the loop over \( i \). However, the resulting code can be load-imbalanced, because different rows may contain different numbers of entries. Logically, this approach tiles the \( i \) outer dimension of the matrix \( B \) while iterating through the \( i \) and \( j \) dimensions of the matrix. We refer to this approach as iterating through the coordinate space of \( B \).

The alternative approach is to instead iterate through the nonzeros of \( B \), which we call iterating through the position space. Code for computing SpMV by iterating through position space is shown in Figure 2d. This style of iteration is statically load-balanced and can be used as the basis for high performance implementations on GPUs. Figure 2e shows an optimized GPU implementation of SpMV, which iterates through position space. This code requires a number of further transformations, including further tiling for GPU blocks, warps, and threads, as well as loop unrolling and precomputation. Transforming SpMV to iterate through position space, however, is the basis on which the rest of the transformations are applied.

While the code in Figure 2a-b can be generated by TACO, the extensions in this work enable the compiler to automatically generate the optimized implementations shown in the rest of the figure. In the rest of the paper, we describe how we automate transforming code to iterate through position space for sparse tensors, and present a scheduling language users can use to explicitly apply this transformation along with others required to generate high performance sparse tensor code on CPUs and GPUs.

## 3 Coordinate & Position Iteration Spaces

There are two types of iteration spaces: coordinate spaces and position spaces. A coordinate space is a multi-dimensional Cartesian combination of coordinates that encode each dimension. Position spaces, on the other hand, are the positions along the space-filling curve created by imposing an ordering on these coordinates. We can imagine many different orderings, but in this paper we will limit ourselves to lexicographical orderings.

Dense coordinate spaces, such as those that arise from dense linear and tensor algebra, can be visualized as a multi-dimensional lattice (i.e., a grid). Figure 3a shows a dense matrix-vector multiplication example \( a = Bc \), and Figure 3b its two-dimensional \( m \times n \) coordinate space, lexicographically ordered with the \( i \) coordinates before the \( j \) coordinates. The resulting loop nest, shown in Figure 2a, iterates over \((i, j)\) coordinates and computes a position \( p \) to access the matrix using a strided formula \( i \times n + j \). Figure 3c shows the multiplication’s one-dimensional position space, consisting of the positions along the lexicographical ordering of the coordinate space. The resulting loop nest would iterate over these positions \( p \) and compute the coordinates with the formulas \( i = p/N \) and \( j = p\%N \). These would, of course, be

\(^1\)In this example, we use the ubiquitous compressed sparse rows storage.
for (int i = 0; i < M; i++) {
  for (int j = 0; j < N; j++) {
    int p = i * N + j;
    a[i] += B[p] * c[j];
  }
}

(a) Unscheduled GEMV

for (int i = 0; i < M; i++) {
  for (int j = 0; j < N; j++) {
    int p = i * N + j;
    a[i] += B[p] * c[j];
  }
}

(b) Unscheduled SpMV

// IndexVar i1, i2;
// return stmt.split(i, i1, i2, 4);
for (int i1 = 0; i1 < CEIL(M, 4); i1++) {
  for (int i2 = 0; i2 < 4; i2++) {
    int i = i1 * 4 + i2;
    if (i >= M) continue;
    for (int p = B_ptr[i]; p < B_ptr[i+1]; p++) {
      int j = B_crd[p];
      a[i] += B[p] * c[j];
    }
  }
}

(c) Strip-mined SpMV

// IndexVar f, p;
// return stmt.fuse(i, j, f)
//     .pos(f, p, B(i, j));
int i = 0;
for (int p = 0; p < B_nnz; p++) {
  int j = B_crd[p];
  while (p == B_ptr[i+1]) i++;
  a[i] += B[p] * c[j];
}

(d) Position Iterating SpMV

// IndexVar f, p, p1, p2, block, warp, thread, thread_nz, thread_nz_pre;
// TensorVar precomputed(Type(Float64, {Dimension(thread_nz)}), taco::dense);
// return stmt.fuse(i, j, f)
//     .split(p, block, p1, NZ_PER_THREAD * BLOCK_SIZE)
//     .split(p1, warp, p2, NZ_PER_THREAD * WARP_SIZE)
//     .split(p2, thread, thread_nz, NZ_PER_THREAD_THREADED)
//     .reorder(block, warp, thread, thread_nz)
//     .precompute(precomputedExpr, thread_nz, thread_nz_pre, precomputed)
//     .unroll(thread_nz_pre, NZ_PER_THREAD_THREADED)
//     .parallelize(block, ParallelUnit::GPUBlock, OutputRaceStrategy::IgnoreRaces)
//     .parallelize(warp, ParallelUnit::GPUWarp, OutputRaceStrategy::IgnoreRaces)
//     .parallelize(thread, ParallelUnit::GPUThread, OutputRaceStrategy::Atoms);

(e) GPU Optimized SpMV

Figure 2. Matrix-vector multiplication computed in several different ways, controlled by sparse iteration space transformations.

expensive to compute and position iteration over a dense matrix therefore primarily makes sense when the coordinates are not needed, such as when scaling a matrix.

Sparse iteration spaces appear when a loop iterates over one or more data structures that encode subsets of the coordinates in an iteration space dimension. In sparse tensor algebra, one or more tensors are stored in hierarchical compressed data structures. Figure 4a shows an example of a matrix $B$ whose coordinates are stored in a compressed hierarchy that contains only those coordinates that lead to a nonzero matrix value. Note that, although we chose to show the coordinate hierarchy abstractly as a forest, in computer memory it would be stored as a concrete data structure, such as compressed sparse rows (CSR) or doubly-compressed sparse rows (DCSR). See Kjolstad et al. [18] or Chou et al. [10] for in-depth descriptions of the relationships between coordinate hierarchies and concrete matrix/tensor data structures.

Sparse coordinate spaces can be visualized as a multi-dimensional lattice with holes. The holes appear because the coordinate hierarchy data structures compress out coordinates, and the sparse iteration space is described by the coordinates that are visited when loops iterate over these data structures. Figure 4b shows the sparse iteration space of the SpMV operation. The resulting loop nest that iterates over it is shown in Figure 2b. The outer loop iterates over the nonempty rows of $B$, stored as (coordinate, position) pairs. The positions are the locations of the coordinate at that level of the hierarchy, so the $i$ coordinate 2 is stored at the second position after coordinate 0. The inner loop iterates over the nonempty (nonzero) components of the current row in the outer loop. The loops together iterate over the coordinate hierarchy of $B$ and thus the sparse iteration space of $B_c$. (It is not necessary to iterate over $c$ as the intersection resulting from the multiplication makes it sufficient to iterate over the smaller operand.)
While loop to increment past empty rows. This increment which may be thought of as a sparse space-filling curve reaches the end of a row. The increment of i is placed in a coordinate j from the matrix B’s coordinate array. In addition, it keeps track of the current coordinate i by incrementing it every time it reaches the end of a row. The increment of i is placed in a while loop to increment past empty rows. This increment strategy requires that the coordinates are stored in order. If they are not, the increment of i would be replaced by a search. If there were more dimensions to the matrix B then the code would keep track of each coordinate above i using the same strategy.

We can tile the coordinate space or the position space of a sparse tensor algebra expression’s loop nest. Tiling its coordinate space is conceptually straightforward and similar to how tiling works for dense loops. We simply split the dimensions of the sparse space into coordinate sets that are assigned to separate tiles. The challenge with tiling a sparse iteration space is that the tiles may not have the same number of nonzeros and will therefore have different sizes in memory. This means that a potentially expensive search is required to determine the starting location of each tile when iterating over them. Furthermore, varying size blocks lead to different amounts of computation and thus load-imbalanced parallel execution. Figure 5 demonstrates the issue: although the cuts result in tiles with equal area, each tile contains very different numbers of points in its iteration space. We see this clearly when projecting the cut to the coordinate hierarchy data structure of B, where the number of values in each tile substantially differs.

Tiling the position space of a sparse tensor algebra expression opens up new and exciting opportunities. The key property of position spaces are that they, in contrast to coordinate spaces, are dense and contiguous. The tiles therefore have the same size and can easily be located. This lets us create statically load-balanced parallel code and makes it possible to generate code that is tuned for GPUs, which tend to benefit from more regular execution than CPUs. Figure 6 shows the effect of tiling the position space of the column coordinates. Figure 7 shows the position space of the row coordinates.

Sparse position spaces are the sequence of nonzero coordinates in the order they are stored in a coordinate hierarchy, which may be thought of as a sparse space-filling curve through nonzero values. Their main advantage is that, although the coordinate space of a sparse tensor expression is sparse and irregular, its position space is a dense one-dimensional space that can be effectively tiled into equal-size blocks. As we shall see, this makes it possible to transform tensor expressions into statically load-balanced parallel code and to make effective use of vectorization and GPUs. Figure 4c shows the position space of the SpMV expression as a sequence of positions with coordinates attached.

Figure 2d shows the single loop that iterates through the sparse position space of the SpMV operation. Like the dense position space, the loop increments a position variable p. Based on the position it retrieves the coordinate j from the matrix B’s coordinate array. In addition, it keeps track of the current coordinate i by incrementing it every time it reaches the end of a row. The increment of i is placed in a while loop to increment past empty rows. This increment strategy requires that the coordinates are stored in order. If they are not, the increment of i would be replaced by a search. If there were more dimensions to the matrix B then the code would keep track of each coordinate above i using the same strategy.
space introduces book-keeping code to track the coordinates above the cut (e.g., what row we are on in the SpMV example) and can lead to conflicting writes when a row spans two tiles. Furthermore, we can only cut the position space with respect to the data structure of one of the operands of the expression. The resulting code, as we will see in Section 6, iterates over this operand, computes coordinates, and then finds the position of those coordinates in the other operands. Despite these drawbacks, we find that position tiles are often crucial, especially on inflexible compute platforms such as GPUs. For example, they let us recreate important optimized GPU codes from the literature, while generalizing to many tensor algebra expressions not previously studied.

Finally, we can generalize position tiling to apply to any dimension of the iteration space, which corresponds to different levels of coordinate hierarchy in the data structure whose positions we are tiling. This lets us create tiles with a fixed number of coordinates in any dimensions. For example, we can tile a SpMV operation in the position space of the rows of matrix $B$. This creates tiles that have the same number of rows; however, the rows themselves may have different numbers of nonzeros. Figure 7 shows a position cut in the row dimension of the iteration space, which corresponds to the first level of the coordinate hierarchy. The cut evenly divides the rows, whereas the position cut in the lowest level of the hierarchy evenly divided the nonzero coordinates. The benefit of a cut in a higher level of the hierarchy is that the cut does not divide a row in two. This results in less bookkeeping code and avoids synchronization as the computation of two tiles do not write to the same locations in the result.

4 Intermediate Representation

In order to carry out the iteration space transformations in this paper, we extend the iteration graph intermediate representation of Kjolstad et al. [18] with the concepts of derived index variables, position index variables, and parallel index variables. Iteration graphs describe the lexicographically ordered sparse iteration space that results from iterating over coordinate hierarchy tensor data structures, and transformations on the graphs transform that space. Combined with iteration graph code generation, described in the next section, we can create loop nests that iterate over the space by coiterating over coordinate hierarchies.

4.1 Iteration Graph Background

We can symbolically describe an iteration space by a lexicographical ordering of index variables that represent dimensions, as in the polyhedral model. We extend this to a tree of such variables, where the concatenated ranges of the variables of each tree level together encode a dimension. This is analogous to an imperfect loop nest where an outer loop contains two or more sequenced loops. These index variable trees describe the full, or dense, iteration space of a tensor algebra expression.

Sparse iteration graphs extend iteration variable trees with paths through index variable nodes that each represent a coordinate tree hierarchy that encode a subset of the iteration space. In tensor algebra these coordinate hierarchies, as we saw in the previous section, come from the data structures that encode the nonzero values of tensors. Figure 8a shows two abstract coordinate hierarchies for the matrix-vector multiplication example. The expression has two index variables that we choose to lexicographically order $i$ before $j$. Figure 8b shows the two symbolic paths induced by these hierarchies. The matrix $B$ enumerates both $i$ and $j$ coordinates and therefore its path go through both variables, where the vector $c$ only enumerates $j$ coordinates. Finally, Figure 8c shows the iteration graph that contains both paths, since the whole expression must coiterate over both coordinate hierarchies. The graph is annotated with an intersection operation between the two paths incoming on $j$. Thus, the iteration space of $j$ is the intersection of each row of $B$ and the vector $c$. It is an intersection because multiplying any variable by zero yields a zero. It is therefore sufficient to iterate over those coordinates where both operands have a value in order to compute the output nonzeros. Conversely, a tensor addition would induce a union between incoming paths.

4.2 Derived Index Variables and Provenance Graphs

In this paper, we extend iteration graphs with the concept of derived index variables. These are new dimensions that are added to an expression’s iteration space by the split, fuse, and position iteration space transformations (described in Section 5) and can be in either coordinate space or position space. Figure 9 shows an iteration space before and after it has been tiled by splitting and reordering the index variables. The tiling increases the dimensionality from two dimensions to four. Since we cannot cleanly visualize a four-dimensional space, however, we visualize the tiled iteration space in terms of its iteration order when projected onto the original iteration space. The nested iteration diagrams show the iteration of each index variable as differently colored arrows. For example, in the original iteration space, the iteration proceeds...
The framework operates on the iteration graph intermedi-
ates variables that represent the dimensions of the final iteration
for sparse, dense, and mixed sparse/dense iteration spaces.

In this section, we will describe a transformation framework
through (transformations are described in the next section).

The original space through the transformations they went
space, p0 and p1, are tracked back to the index variables in

tiling the expression in the position space. The derived index
variables back to the original index variables.

Provenance graphs let us map between the transformed iter-
ation space and the original space, so that the code generator
can compute coordinates in the original space as needed to
iterate in the transformed space, while data structures must
be accessed by coordinates in the original space.

Index variable provenance graphs track the history of
derived index variables back to the original index variables. Provenance graphs let us map between the transformed iteration
space and the original space, so that the code generator
can compute coordinates in the original space as needed to
index into tensors data structures. Figure 10 shows the prove-

graph after creating a load-balanced SpMV kernel by

The transformations in this paper—coord, pos, reorder,
fuse, split, divide and parallelize—provide a comprehensive framework for controlling iteration order through sparse iteration spaces. Figure 11 shows the effect of the reorder, fuse and split transformations on an i, j iteration space. Although they are here shown separately, transformations are typically used together, with some adding or removing iteration space dimensions that other transformations reorder or tag for parallel execution. All transformations apply to index variables in both the coordinate space and the position
space and the coord and pos transformations transition index variables between these spaces.

Key to our approach is that the transformations operate on the iteration graph intermediate representation before sparse code is generated. This representation makes it possible to reason about sparse iteration spaces algebraically without the need for sophisticated dependency and control flow analysis of sparse code, which may contain while loops, conditionals and indirect accesses. The sparse code is then introduced when iteration graphs are lowered to code, as described in the next section.

Coordinate and Position Transformations The coord
and pos transformations create new index variables in the
coordinate and position spaces from index variables in the
position and coordinate spaces respectively. Specifically, the
pos transformation takes an index variable in the coordinate
space and replaces it with a new derived index variable that
operates over the same iteration range, but with respect to
one input’s position space. The coord transformation, on the
other hand, takes an index variable in position space and

Figure 9. Iteration graphs, nested iteration orderings, and
unrolled iteration orderings are shown for an untiled row-
major iteration (top) and a tiled iteration (bottom).

Figure 10. Index variable provenance graph after paralleliz-
ing SpMV in the CSR matrix’s position space. The graph
maps derived index variables back to the index variables
they derived from. Blue variables are in position space.

along the first blue arrow before it moves along the first red
arrow to the next row. The unrolled iteration space shows
the order of the overall iteration. Mapping between iteration
spaces is important for code generation, since emitted loops
iterate in the transformed space, while data structures must
be accessed by coordinates in the original space.

5 Transformations

In this section, we will describe a transformation framework
for sparse, dense, and mixed sparse/dense iteration spaces.
The framework operates on the iteration graph intermedi-
ate representation discussed in the previous section. These

transformations let us control the order of computation, so
that we can optimize data access locality and parallelism.

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one input’s position space. The coord transformation, on the
other hand, takes an index variable in position space and
replaces it with a new derived dimensional iterator that iterates over the corresponding iteration range in the coordinate iteration space.

**Reorder** The reorder transformation swaps two directly nested index variables in an iteration graph. This changes the order of iteration through the space and the order of tensor accesses. The precondition of a reorder transformation is that it must not hoist a tensor operation outside a reduction that it does not distribute over. Figure 11b shows the effect of the reorder transformation on a two-dimensional iteration space, in terms of iteration order on the original space. Whereas the original space was iterated through in row-major order, the reordering creates a new space that is equivalent to iterating through the original space in column-major order.

**Fuse** The fuse transformation collapses two directly nested index variables. It results in a new fused index variable that iterates over the product of the coordinates of the fused index variables. This transformation by itself does not change iteration order, but facilitates other transformations such as iterating over the position space of several variables and distributing a multi-dimensional loop nest across a thread array on GPUs. Figure 11c shows the iteration order of the fused space in terms of the original space. The fused space is a one-dimensional space that is equivalent to iterating over the original space in a linearized row-major order.

**Split** The split transformation splits (strip-mines) an index variable into two nested index variables, where the size of the inner index variable is constant. The size of the outer index variable is the size of the original index variable divided by the size of the inner index variable, and the product of the new index variables sizes therefore equals the size of the original index variable. Note that in the generated code, when the size of the inner index variable does not perfectly divide the original index variable, a *tail strategy* is employed such as emitting a variable sized loop that handles remaining iterations. Figure 11d shows the effect of the split transformation as an iteration order over the original space. The split creates a new inner loop that iterates over two iteration space points for each iteration of the outer loops.

**Divide** The divide transformation splits one index variable into two nested index variables, where the size of the outer index variable is constant. The size of the inner index variable is thus the size of the original index variable divided by the size of the outer index variable. The divide transformation is important in sparse codes because locating the starting point of a tile can require an $O(n)$ or $O(\log(n))$ search. Therefore, if we want to parallelize a blocked loop, then we want a fixed number of blocks and not a number proportional to the tensor size.

**Parallelize, Bound and Unroll** The parallelize, unroll and bound transformations apply to only one index variable and tag it with information telling the code generation machinery how to lower it to code. The parallelize transformation tags an index variable for parallel execution. The transformation takes as an argument the type of parallel hardware to execute on. The set of parallel hardware is extensible and our current code generation algorithm supports SIMD vector units, CPU threads, GPU thread blocks, GPU warps, and individual GPU threads. Parallelizing the iteration over an index variable changes the iteration order of the loop, and therefore requires reductions inside the iteration space described by the index variable’s sub-tree in the iteration graph to be associative. Furthermore, if the computation uses a reduction strategy that does not preserve the order, such as atomic instructions, then the reductions must also be commutative. The unroll transformation tags an index variable to result in an unrolled loop with a given unroll factor. This reduces the amount of control flow logic at the cost of increased code size. Finally, the bound transformation fixes the range of an index variable, which lets the code generator insert constants into the code and enables other transformations that require fixed size loops, such as vectorization.

## 6 Code Generation

We extend the sparse tensor algebra code generator described by Kjolstad et al. [18] to support iteration graphs with derived index variables. This is sufficient to lower transformed iteration spaces to efficient code and to generate parallel and GPU code.

The existing code generator operates on iteration graphs and generates loops to iterate over each index variable in turn, nested inside the loops generated for index variables above in the tree. For each index variable, one or more loops are generated to either iterate over a full dimension (a dense loop) or to coiterate over levels of one or more coordinate hierarchy data structures. Coiteration code is generated using a construct called a *merge lattice* that enumerates the intersections that must be covered to iterate over the sparse domain of the dimension. This may result in a single for loop, a single while loop, or multiple while loops.

To generate code for transformed sparse iteration spaces, we extended this code generator to

1. determine derived index variable bounds, generate loops over derived index variables, and generate iteration guards to implement a tail strategy,
2. generate code to recover coordinates in the original iteration space from coordinates in the transformed iteration space, and
3. generate SIMD vectorized, OpenMP CPU and CUDA GPU code with reductions.

Figure 12 provides an example of a generated SpMV implementation that highlights derived loop bounds (green), iteration guards (blue), and index variable recovery (red). The following sections describe each of these extensions.
#pragma omp parallel for schedule(runtime, 1)
for (int p0 = 0; p0 < CEIL(B2_pos[B1_dim],16); p0++) {
  int i = binary_search(B2_pos, 0, B1_dim, p0+16);
  double t = 0.0;
  for (int p1 = 0; p1 < 16; p1++) {
    int p = p0 * 16 + p1;
    if (p == B2_pos[i]) break;
    int j = B2_crd[p] / 2; // i++
    while (p == B2_pos[i]) i++;
    t += B[p] * c[j];
    if (p1 == B2_pos[i]) {
      #pragma omp atomic
      a[i] += t;
      t = 0.0;
    }
  }
  #pragma omp atomic
  a[i] += t;
}

Figure 12. Generated code for parallel sparse matrix-vector multiply. Red code recovers index variables, green code shows iteration bounds of derived index variables, and blue code depicts iteration guards.

6.1 Derived Iteration Code Generation
To generate loops that iterate, or coiterate, over derived index variables, the code generator must first compute their iteration domains. These domains are computed by an iteration domain propagation algorithm, and affect the bounds of generated loops (green in Figure 12). In cases where a fixed range index variable was split from another index variable, and its size does not evenly divide the original variable, the code generation algorithm also generates an iteration guard tail strategy (blue in Figure 12).

To determine the iteration domain of derived index variables, we propagate bounds through the index variable provenance graph (see Figure 10). We have defined propagation rules for each transformation and calculating the iteration domain of the derived index variables involves applying the propagation rules to each arrow in turn, from the original index variables to the derived index variables.

6.2 Coordinate Recovery
In a transformed iteration space dimensions are represented by derived index variables and the generated loops iterate over their coordinates. The coordinate hierarchy data structures of the tensors, however, contain and are accessed by coordinates in the original iteration space. The code generator must therefore emit code to map between these iteration spaces and we call this coordinate recovery.

It may be necessary to recover original or derived coordinates. Recovering original coordinates is required when these will be used to index into tensor data structures, which

Figure 13. An index variable provenance graph annotated with arrows that depict different ways that an unknown index variable’s coordinates can be recovered from known index variables. Red arrows depict original coordinate recovery and green arrows derived coordinate recovery.

are stored in the original coordinate space. It is necessary to recover derived coordinates, on the other hand, when a coordinate in the original coordinate space is loaded from a coordinate hierarchy, but a coordinate in the derived space is needed to determine iteration guard exit conditions.

The code generator defines two functions on the provenance graph to map coordinates between original and derived index variables, and vice versa. These are:

- **recover_original** which computes the coordinate of an index variable from its derived index variables in a provenance graph (red arrows in Figure 13), and
- **recover Derived** which computes the coordinate of an index variable from the variable it derives from and its siblings (green arrows in Figure 13).

Coordinate recovery may require an expensive search, so we define an optimization that computes the next coordinate faster than computing an arbitrary coordinate. Such tracking code implements a recurrence through coordinates and requires them to be stored in order in coordinate hierarchy data structures. The coordinate tracking code has two parts, an initialization that finds the first coordinate and tracking that advances it. The initialization is done with the following code generation function on provenance graphs:

- **recover_track** which computes the next coordinate (red stippled arrow in Figure 13).

Figure 12 uses the tracking optimization to track the i coordinate. It starts by finding the first i coordinate using a binary search, but then simply advances to the next i coordinate when it finds the end of a row segment.

6.3 Parallel and GPU Code Generation
Parallelization and vectorization are applied to the high-level iteration graph IR and their safety can therefore be assured without heavy analysis. A parallelization strategy is tagged onto an index variable and the code generator generates parallel constructs from it, whether SIMD vector instructions, a parallel OpenMP loop, or a GPU thread array. The parallelization command can easily be extended with other parallelization strategies and parallel code generators are easy to write as they only mechanically carry out orders from the higher levels.
It is the responsibility of the parallel code generators to emit code that safely manage parallel reductions. We have implemented two strategies. The first strategy is to detect data races, by inspecting whether a reduction is dominated by an index variable that is summed over, and insert an atomic instruction. A second strategy is to separate the loop into worker and a reduction loops that communicate through a workspace [17] (e.g., an array). The threads in the parallel loop reduce into separate parts of the workspace. When they finish, the second loop reduces across the workspace, either sequentially or in parallel. We have implemented this strategy on CPUs using SIMD instructions, and on GPUs with CUDA warp-level reduction primitives. It is also possible to control the reduction strategy at each level of parallelism to optimize for each level of parallel hardware. For example, on a GPU we can choose a loop separation strategy within a warp and atomics across warps.

7 Scheduling API

We expose the sparse transformation primitives as a scheduling interface in TACO, inspired by the Halide system for dense stencil computations [29]. The scheduling language is independent of both the algorithmic language (used to specify computations) and the format language (used to specify tensor data structures). This lets users schedule tensor computations independently of data structure choice, while ensuring correctness for the overall algorithm, and further enables efficient execution on different hardware without changing the algorithm. We add the following scheduling APIs to TACO:

IndexStmt reorder(vector<IndexVar> reorderedVars);
IndexStmt fuse(IndexVar i, IndexVar j, IndexVar f);
IndexStmt split(IndexVar i, IndexVar i1, IndexVar i2, size_t size);
IndexStmt divide(IndexVar i, IndexVar i1, IndexVar i2, size_t size);
IndexStmt pos(IndexVar i, IndexVar p, Access a);
IndexStmt coord[IndexVar p, IndexVar i];
IndexStmt parallelize(IndexVar i, ParallelUnit pu, 
OutputRaceStrategy rs);
IndexStmt unroll(IndexVar i, size_t unrollFactor);
IndexStmt bound(IndexVar i, BoundType type, 
size_t bound);
IndexStmt precompute(IndexExpr e, IndexVar i, 
IndexVar i_pre, Tensor w);

These primitives directly correspond to transformations described in Section 5. The split, divide, and fuse transformations follow the convention that, derived-from index variables precede newly-derived index variables in the list of arguments. reorder takes a new ordering for a set of index variables that are directly nested in the iteration order. bound specifies a compile-time constraint on an index variable’s iteration space that allows knowledge of the size or structured sparsity pattern of the inputs to be incorporated during bounds propagation. pos and coord create new index variables in their respective iteration spaces. pos requires a tensor access expression as input, that described the tensor whose coordinate hierarchy to perform a position cut with respect to. Specifically, the derived p variable will iterate over the tensors’ position space at the level that the i variable is used in the access expression. The precompute transformation is described in prior work [17], but composes with our set of transformations to allow us to leverage scratchpad memories and reorder computations to increase locality. The unroll primitive unrolls the corresponding loop by a statically-known integer number of iterations, and finally the parallelize primitive is as described in Section 6.3. An example schedule is shown in Figure 14. We first generate an iteration graph by using the concretize function and then apply successive transformations using scheduling language primitives.

8 Evaluation

We carry out experiments to compare the performance of code generated by our technique with different schedules to state-of-the-art library implementations of three important expressions: SpMV, SpMM, and MTTKRP. We chose these expressions because they have been heavily studied in the performance engineering literature. We stress, however, that the point of our experiments is not to demonstrate that our transformations produce kernels with the best possible performance for these specific expressions. Rather, the purpose of our transformations is to apply to any tensor algebra expression. These three expressions are therefore stand-ins for any expression, and we seek to demonstrate that our technique produces code with good performance that is competitive with hand-optimized kernels.

In addition, we carry out several studies to highlight situations where the best schedule differs depending on the situation. For example, the best CPU and GPU schedules differ, and the best GPU SpMV schedule depends on whether the computation is load-balanced or not. We carry out these studies on the simplest kernels that are sufficient to make
our point. For most studies this is the SpMV kernel, except for the locality study in Section 8.6 where we use the SpMM expression, since it has two dense loops we can tile over.

8.1 Methodology

We implement our transformation framework as an extension to the TACO compiler, which is freely available under the MIT license. To evaluate it, we compare the performance of code that has been optimized using our transformations accessed through the scheduling API to the original TACO system (commit 331188), Intel MKL [15], CSR5 [21], cuSPARSE [26], and hand-optimized GPU kernels presented by Nisa et al. [25]. For the comparative studies we use the 17 matrices from the SuiteSparse sparse matrix repository [11] used for targeted studies by Merrill and Garland [23] and Steinberger et al. [37], and the three tensors from the FROSTT sparse tensor repository [32] that were used by Kjolstad et al. [18]. We also carry out studies to evaluate the value of a scheduling language. Our load-balance study uses synthetic matrices designed to show at what load imbalance it makes sense to move to a statically load-balanced kernel. We have made all schedules available in the supplementary material.

All CPU experiments are run on a dual-socket, 12-core with 24 threads, 2.5 GHz Intel Xeon E5-2680 v3 machine with 30 MB of L3 cache per socket and 128 GB of main memory, running Ubuntu 18.04.3 LTS. We compile code that our technique generates using Intel icpc with -O3, -Ofast, and -mavx2. We run each experiment with a warm cache 16 times with 8 warm-up runs and report median serial execution times. All GPU experiments are run on an NVIDIA DGX system with 8 V100 GPUs with 32 GB of global memory, 6MB of L2 cache and 128KB of L1 cache per SM (80 SMs), and a bandwidth of 897 GB/s. We compile the CUDA code that our technique generates using NVCC v9.0 with -O3 and --use_fast_math.
8.2 Comparative Performance

Our first experiments validate that the performance of the code generated using our transformation framework performs well compared to other systems, and are shown in Figures 15–20. We evaluate three linear algebra and tensor algebra kernels that have received a lot of attention from researchers that study sparse linear and tensor algebra optimization. These are the ubiquitous SpMV operation on CSR matrices, the (sparse matrix) \( \times \) (dense matrix) (SpMM) operation, and the Matrizicated Tensor Times Khatri-Rao Product (MTTKRP) operation. We use our scheduling language to optimize each of these for our CPU and a GPU. On CPUs we compare the linear algebra kernels to the TACO Compiler [18], the Intel MKL library [15], and the CSR5 implementation of SpMV [21]. On GPUs we compare the SpMV kernel to cuSPARSE [26] using the CSR and hybrid format implementations of Bell and Garland [6], as well as the Merge-Based SpMV implementation of Merrill and Garland [23]. For the MTTKRP tensor kernel we compare to four hand-optimized GPU kernels presented in [25]. The Scheduled Taco results come from our system. The schedules are hand-written and included in the supplementary material. Scheduled TACO uses standard sparse data formats (CSR and CSF) instead of requiring preprocessing.

The results show the kernels generated by our transformations are competitive with hand-optimized library implementations in most cases. One exception is SpMM on GPUs where NVIDIA’s cuSPARSE library performs better. This library is closed source, however, so the exact reason is unknown to us. These results demonstrate the quality of code generated by our transformations. Since the code generator does nothing special for these expressions, it provides evidence for the performance we may see for other tensor algebra expressions that have no hand-optimized kernels.

8.3 Scheduling for GPUs

Good GPU schedules are different from good CPU schedules, and it is important to have transformations that let us order operations to fit the machine at hand. GPUs are sensitive to the order of loads and to thread divergence, and typically require more involved schedules to ensure operations are done in the right order. For instance, the best parallel CPU SpMV schedule compiled to and executed on a GPU performs 6.9x worse than the warp-per-row GPU schedule on a matrix with four million randomly allocated nonzeros.

The best CPU schedule for the SpMV operation when the matrix is load-balanced is a simple strip-mining of the outer dense loop to create parallel blocks, followed by parallelizing the outer loop. The resulting code assigns a set of rows to each CPU thread executing in parallel. The analogous schedule is a disaster on a GPU. Since threads in a warp execute separate rows, they cannot coalesce memory loads. This results in poor effective memory bandwidth and thus poor performance for the memory-bound SpMV kernel. Furthermore, if there are a different number of nonzeros on the rows executed by different threads in a warp, then they will experience thread divergence.

In contrast, more optimized GPU schedules are more carefully tiled. The warp-per-row schedule assigns an equal number of nonzero elements of the row to each thread and uses warp-level synchronization primitives to efficiently reduce these partial sums. The optimized SpMV schedule that we use in Figure 16 tiles the position space of the sparse matrix across threads. We also use a temporary to allow us to unroll the loop that performs loads and then later use atomic instructions to store the results in the output. This provides better memory access patterns and increased instruction-level parallelism, but makes hand-writing such a kernel difficult. On a matrix with four million randomly allocated nonzeros, this increased instruction-level parallelism provided a 36% speedup for our optimized schedule over the same schedule without the temporary or loop unrolling.

8.4 Scheduling for Load Balance

This study shows that the best GPU schedules differ for load-balanced and load-imbalanced computations. The SpMV computation demonstrates the issue, as it is sensitive to a skewed distribution of nonzeros in the matrix. The challenge, however, generalizes to any expression with a sparse tensor.

The previous section outlined an effective warp-per-row GPU SpMV schedule where threads in a warp collectively work on a matrix row at a time. If distribution of nonzeros across matrix rows is skewed, this kernel suffers from load imbalance. The optimized SpMV schedule used in Figure 16 where the two loops are fused and then split in the position space provides perfect static load balancing for loads of the sparse tensor at the cost of overhead from coordinate recovery. Figure 21 shows the performance of the warp-per-row schedule and the load-balanced position split schedule as the distribution of nonzeros per row becomes more skewed according to an exponential function. The number of nonzeros remains fixed and rows are randomly shuffled. As expected, the warp-per-thread schedule performs worse as skew increases, while the load-balanced schedule benefits from long rows and performs better with increased skew. The performance intersects just before the base of 1.00256. For skewed matrices, the load-balanced kernel is thus preferable.

8.5 Scheduling for Maximal Parallelism

Loop fusion to increase the amount of parallelism, despite higher overhead, can make sense in parallelism-constrained situations. The warp-per-row GPU SpMV schedule described in Section 8.3 assigns each row to be executed by a different warp. For matrices with few rows, however, this may result in too little parallelism to occupy the GPU. For such matrices, fusing before parallelizing the two loops creates more parallelism. For example, we executed the SpMV kernels generated
from both schedules on a short and wide $100 \times 100k$ matrix with 10k nonzeros per row. As expected from the experiment design, the warp-per-row kernel had too little parallelism and the fused kernel ran on average 4.5 times faster across 10 runs.

8.6 Scheduling for Locality
Sparse tensor algebra expressions can have dense loops that may be tiled for better temporal locality. We demonstrate this for the SpMM expression. Since a sparse matrix is multiplied by a sparse matrix, the resulting kernel has two dense loops that can be tiled. We implemented a tiled and an untiled schedule for this expression and ran the resulting kernels on a $100k \times 100k$ sparse matrix with an average of 1000 randomly distributed nonzeros per row multiplied by a $100k \times 32$ dense matrix. Not surprisingly, the tiled kernel performed 2x better.

9 Related Work
There is a long history of optimizations and transformations for sparse matrices [11, 14, 43] and tensors. We divide prior work into the categories described in the following sections.

Sparse compilation The work by Bik and Wijshoff [7, 8] was an early attempt to apply compiler techniques to sparse matrix codes. They use a technique called guard encapsulation to turn dense loops over dense arrays into sparse loops over nonzeros. The Bernouilli [19] system followed soon thereafter and lifted matrix codes to relational algebra, that was then optimized and emitted as sparse code. Most recent work on compiling and transforming sparse loops has been done in the context of the polyhedral model [4, 5, 38, 39]. These generally employ inspector-executor techniques, which combine run-time inspection of data with compile-time transformations. Venkat et al. [41] use the polyhedral model to turn dense loops with conditional guards into loops over a sparse matrix, enabling further optimizations including wavefront parallelism [42] and tiling of dense loops inside sparse codes [2]. Pugh et al. [28] designed SIPR, an intermediate representation for sparse compilation. Most recently, the TACO compiler generalizes sparse and dense tensor operations in a variety of formats, automatically generating code for any computation [10, 17, 18]. We build on TACO in this work, adding scheduling and GPU code generation.

Dense tensor compilation Recent work on dense tensor algebra has focused on two application areas: quantum chemistry and machine learning. While the two areas share some similarities, different types of tensors and operations are important in each domain. The Tensor Contraction Engine [3] automatically optimizes dense tensor contractions, and is developed primarily for chemistry applications. Libtensor [12] and CTF [35] are cast tensor contractions as matrix multiplication by transposing tensors. In machine learning, TensorFlow [1] and other frameworks [16, 27] combine tensor operations to efficiently apply gradient descent for learning, and are among the most popular packages used for deep learning. TVM [9] takes this further by adopting and modifying Halide’s scheduling language to make it possible for machine learning practitioners to control schedules for dense tensor computations. Tensor Comprehensions (TC) [40] is another framework for defining new deep learning building blocks over tensors, utilizing the polyhedral model.

Scheduling Halide [30, 31] is a widely used domain specific languages in industrial applications, partially due to its flexible scheduling language that lets users express how a high-level algorithm is executed. Many of our constructs are inspired by Halide, though we deal with sparse loops while Halide only considers dense loops. TVM uses a variant of Halide’s scheduling language, modified for deep learning applications. Most recently, GraphIt [46] and Taichi [13] built scheduling languages for graph algorithms and sparse irregular spatial data structures, respectively. In the polyhedral framework, CHiLL [41] allows users to specify sequences of loop transformations, similar to a scheduling language.

Hand-optimized sparse tensor code Finally, several researchers have studied how to manually optimize sparse linear and tensor algebra code for CPUs and GPUs. We will mention a few prominent examples. The Intel MKL library is a fast sparse linear algebra library for CPUs that employs some inspector-executor techniques to choose formats [15]. Bell and Garland describe a set of techniques for optimizing SpMV for several different data structures on GPUs, including the vectorized kernel we use in our evaluation [6]. Furthermore, Merrill and Garland showed how to develop a load-balanced SpMV implementation by generalizing a parallel merge algorithm [23]. The SPLATT library is an efficient implementation of the MTTKRP kernel [33] and HiCOO explores new coordinate-based formats that further improves performance [20]. Nisa et al. describe techniques for how to effectively parallelize the MTTKRP kernel for GPUs [25]. Finally, the Cyclops library shows how to scale sparse kernels to distributed machines [34].
10 Conclusion
This paper presented a comprehensive theory of transformations on sparse iteration spaces. The resulting transformation machinery and code generator can recreate tiled, vectorized, parallelized and load-balanced CPU and GPU codes from the literature, and generalizes to far more tensor algebra expressions and optimization combinations. Furthermore, as the sparse iteration space transformation machinery works on a high-level intermediate representation that is independent of target code generators, it points towards a portable sparse tensor algebra compilation. With this work, sparse tensor algebra is finally on the same optimization and code generation footing as dense tensor algebra and array codes.

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A Appendix

A.1 SPMV on a CPU (Figure 15)

IndexVar i("i"), j("j");
y(i) = A(i, j) * x(j);

IndexVar i0("i0"), i1("i1"), kpos("kpos"), kpos0("kpos0"), kpos1("kpos1");
IndexStmt stmt = y.getAssignment().concretize();
stmt = stmt.split(i, i0, i1, CHUNK_SIZE)
   .reorder({i0, i1, j})
   .parallelize(i0, ParallelUnit::CPUThread, OutputRaceStrategy::NoRaces);

A.2 SPMV on a GPU (Figure 16)

IndexVar i("i"), j("j");
IndexExpr precomputedExpr = A(i, j) * x(j);
y(i) = precomputedExpr;

IndexVar f("f"), fpos("fpos"), fpos1("fpos1"), fpos2("fpos2");
IndexVar block("block"), warp("warp"), thread("thread");
IndexVar thread_nz("thread_nz"), thread_nz_pre("thread_nz_pre");
TensorVar precomputed("precomputed",
   Type(Float64, {Dimension(thread_nz)}), taco::dense);
IndexStmt stmt = y.getAssignment().concretize();
stmt = stmt.fuse(i, j, f)
   .pos(f, fpos, A(i, j))
   .split(fpos, block, fpos1, NNZ_PER_TB)
   .split(fpos1, warp, fpos2, NNZ_PER_WARP)
   .split(fpos2, thread, thread_nz, NNZ_PER_THREAD)
   .reorder({block, warp, thread, thread_nz})
   .precompute(precomputedExpr, thread_nz, thread_nz_pre, precomputed)
   .unroll(thread_nz_pre, NNZ_PER_THREAD)
   .parallelize(block, ParallelUnit::GPUBlock, OutputRaceStrategy::IgnoreRaces)
   .parallelize(warp, ParallelUnit::GPUWarp, OutputRaceStrategy::IgnoreRaces)
   .parallelize(thread, ParallelUnit::GPUThread, OutputRaceStrategy::Atomics);

A.3 SPMM on a CPU (Figure 17)

IndexVar i("i"), j("j"), k("k");
C(i, k) = A(i, j) * B(j, k);

IndexVar i0("i0"), i1("i1"), kbounded("kbounded"), k0("k0"), k1("k1");
IndexVar jpos("jpos"), jpos0("jpos0"), jpos1("jpos1");
IndexStmt stmt = C.getAssignment().concretize();
stmt = stmt.split(i, i0, i1, CHUNK_SIZE)
   .pos(j, jpos, A(i, j))
   .split(jpos, jpos0, jpos1, UNROLL_FACTOR)
   .reorder({i0, i1, jpos0, k, jpos1})
   .parallelize(i0, ParallelUnit::CPUThread, OutputRaceStrategy::NoRaces)
   .parallelize(k, ParallelUnit::CPUVector, OutputRaceStrategy::IgnoreRaces);

A.4 SPMM on a GPU (Figure 18)
IndexVar i("i"), j("j") , k("k");
C(i, k) = A(i, j) * B(j, k);

IndexVar f("f") , fpos("fpos") , block("block") , fpos1("fpos1") , warp("warp");
IndexVar nnz_pre("nnz_pre") , nnz("nnz");
IndexVar dense_val_unbounded("dense_val_unbounded");
IndexVar dense_val("dense_val") , thread("thread") , thread_nz("thread_nz");
TensorVar precomputed("precomputed",
    Type(Float64, {Dimension(nnz)}) , taco::dense);
IndexStmt stmt = C.getAssignment().concretize();
stmt = stmt.reorder({i, j, k})
    .fuse(i, j, f)
    .split(fpos, block, fpos1, NNZ_PER_TB)
    .split(fpos1, warp, nnz, NNZ_PER_WARP)
    .split(k, dense_val_unbounded, thread, WARP_SIZE)
    .bound(dense_val_unbounded, dense_val, 1, BoundType::MaxExact)
    .reorder(block, warp, dense_val, thread, nnz)
    .parallelize(block, ParallelUnit::GPUBlock, OutputRaceStrategy::IgnoreRaces)
    .parallelize(warp, ParallelUnit::GPUWarp, OutputRaceStrategy::IgnoreRaces)
    .parallelize(thread, ParallelUnit::GPUThread, OutputRaceStrategy::Atomics);

A.5 MTTKRP on a CPU (Figure 19)
IndexVar i("i") , j("j") , k("k");
A(i,j) = B(i,k,l) * C(k,j) * D(l,j);

IndexVar ipos("ipos") , ipos0("ipos0") , ipos1("ipos1");
IndexStmt stmt = A.getAssignment().concretize();
stmt = stmt.pos(i, ipos, B(i, k, l))
    .split(ipos, ipos0, ipos1, CHUNK_SIZE)
    .reorder({ipos0, ipos1, k, l, j})
    .parallelize(ipos0, ParallelUnit::CPUThread, OutputRaceStrategy::NoRaces);

A.6 MTTKRP on a GPU (Figure 20)
IndexVar i("i") , j("j") , k("k");
A(i,j) = B(i,k,l) * C(k,j) * D(l,j);

IndexVar kl("kl") , f("f") , fpos("fpos") , block("block") , fpos1("fpos1");
IndexVar warp("warp") , nnz("nnz") , dense_val("dense_val");
IndexVar dense_val_unbounded("dense_val_unbounded") , thread("thread");
IndexStmt stmt = A.getAssignment().concretize();
stmt = stmt.reorder({i,k,l,j})
    .fuse(k, l, kl)
    .fuse(i, kl, f)
    .split(fpos, block, fpos1, NNZ_PER_TB)
    .split(fpos1, warp, nnz, NNZ_PER_WARP)
    .split(j, dense_val_unbounded, thread, WARP_SIZE)
    .bound(dense_val_unbounded, dense_val, 1, BoundType::MaxExact)
    .reorder((block, warp, dense_val, thread, nnz))
A.7 SpMV Thread per Row on GPU (Section 8.3)

IndexVar i("i"); j("j");
y(i) = A(i, j) * x(j);

IndexVar block("block"), warp("warp"), thread("thread");
IndexVar thread_nz("thread_nz"), i1("i1"), jpos("jpos");
IndexVar block_row("block_row"), warp_row("warp_row");
IndexStmt stmt = y.getAssignment().concretize();
stmt = stmt.parallelize(block, ParallelUnit::GPUBlock, OutputRaceStrategy::IgnoreRaces)
.parallelize(thread, ParallelUnit::GPUThread, OutputRaceStrategy::Atomics);

A.8 SpMV Warp per Row on GPU (Section 8.3)

IndexVar i("i"); j("j");
IndexExpr precomputedExpr = A(i, j) * x(j);
y(i) = precomputedExpr;

IndexVar block("block"), warp("warp"), thread("thread");
IndexVar i1("i1"), jpos("jpos"), block_row("block_row"), warp_row("warp_row");
TensorVar precomputed("precomputed",
Type(Float64, {Dimension(thread_nz)}), taco::dense);
IndexStmt stmt = y.getAssignment().concretize();
stmt = stmt.split(i, block, thread, ROWS_PER_TB)
.parallelize(block, ParallelUnit::GPUBlock, OutputRaceStrategy::NoRaces)
.parallelize(thread, ParallelUnit::GPUThread, OutputRaceStrategy::NoRaces);

A.9 SpMV on GPU with no Unrolling (Section 8.3)

IndexVar i("i"); j("j");
IndexExpr precomputedExpr = A(i, j) * x(j);
y(i) = precomputedExpr;

IndexVar f("f"), fpos("fpos"), fpos1("fpos1"), fpos2("fpos2");
IndexVar block("block"), warp("warp"), thread("thread"), thread_nz("thread_nz");
IndexStmt stmt = y.getAssignment().concretize();
stmt = stmt.fuse(i, j, f)
.parallelize(block, ParallelUnit::GPUBlock, OutputRaceStrategy::IgnoreRaces)
A.10 SpMM on CPU Tiled (Section 8.6)

IndexVar i("i"), j("j"), k("k");
C(i, k) = A(i, j) * B(j, k);

IndexVar i0("i0"), i1("i1");
IndexVar jpos("jpos"), jpos0("jpos0"), jpos1("jpos1");
IndexStmt stmt = C.getAssignment().concretize();
stmt = stmt.pos(j, jpos, A(i,j)).
    .split(jpos, jpos0, jpos1, UNROLL_FACTOR).reorder({i, jpos0, k, jpos1});

A.11 SpMM on CPU No Tiling (Section 8.6)

IndexVar i("i"), j("j"), k("k");
C(i, k) = A(i, j) * B(j, k);

IndexStmt stmt = C.getAssignment().concretize();