A Digital Calibration Method for a MEMS Accelerometer based on Harmonic Self-Test

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Abstract. This paper proposes a digital calibration method for electromechanical closed-loop MEMS accelerometer. The method based on a harmonic self-test mechanism, in which the MEMS structure is excited by an on-chip generated electrostatic force and the corresponding harmonic distortion could be captured and analysed as an indicator of structure mismatch. According the harmonic distortion level, the mismatch could be calibrated out by the electrical signal on-chip. The whole exciting and calibrating procedure is realized in digital domain. Thus, not only the area and power consumption are reduced, but also the flexibility and robustness of the procedure is enhanced.

1. The first section in our paper

As the improvement in process and the enhanced requirement in performance, MEMS accelerometers are not occupying a dominate share in consumer market, but also taking part into high-end inertial navigation area. When coming into the navigation area, the long-term stability is become a primary consideration [1]. However due to the high sensitivity to process and environment variation, the performance of MEMS structure exhibits a large fluctuation, which hindering its further development [2,3]. Thus, on one hand closed-loop architecture is used to reduce the output sensitivity to the fluctuation [4,5], on the other hand on-line self-calibration of the fluctuation out has attracted a lot of research attentions [6-9].

In this paper we concentrate in the self-calibration of sigma-delta closed-loop accelerometer. This architecture incorporates the MEMS sensing element into the sigma-delta modulation loop, thus not only the performance fluctuation of MEMS structure can be attenuated by the open loop gain, but also the digital interface and closed-loop configuration give facility to the implementation of self-test and calibration.

In this paper, we propose a digital self-calibration method to realize on-chip self-test and calibration of the front-end parasitic effect. And hence the linearity, stability and zero bias can be improved. The proposed method based on a principle that the parasitic effect will cause a consistent residue displacement of the proof mass, which cannot be rectified by the closed-loop gain, unlike displacement caused by the real input acceleration, and will induce a second harmonic distortion in proposed self-test experiment.
The proposed method uses an integrated high-precision digital resonator to excite the MEMS structure, and identifies the parasitic mismatch by observing the second harmonic distortion in output result. The identified mismatch can be further suppressed by the use of on-chip trimming circuit. The on-chip digital resonator is realized using 1-bit sigma-delta modulation which is coordinate to the electro-mechanical sigma-delta accelerometer, resulting an efficient low-cost high-precision solution. The open-loop gain of the system is enhanced by the use of PID control mechanism, ensuring the parasitic to input acceleration resolution.

2. MEMS Sensing Element and The Parasitic Effect
The sensing element is a critical part of the system which acts as both a capacitive sensor for external acceleration and an electrostatic actuator for the feedback force. As shown in Figure 1, it generally consists of a proof mass suspended by cantilever beams anchored to a fixed frame and accompanied by a couple of fixed plates located on each side.

![Figure 1. The structure diagram of the sensing element.](image)

The sensing characteristic can be described by the following second order transfer function:

$$H_{ms} = \frac{x}{a} = \frac{1}{s^2 + \frac{b}{m} s + \frac{k}{m}} = \frac{1}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}$$  \hspace{1cm} (1)

Where $x$ is the displacement, $m$ is the proof mass, $b$ is the damping factor, $k$ is the spring constant, $\omega_0$ is the intrinsic frequency of the structure, $Q$ is the quality factor.

The actuating characteristic can be described by the electrostatic force formula:

$$F_{elec} = \frac{C_0 d_0 V^2}{2(d_0 + x)^2}$$  \hspace{1cm} (2)

Where $C_0$ is the static capacitance, $d_0$ is the initial distance between the plates, and $x$ is the displacement of proof mass at real-time. Note that the electrostatic force has an inherent relationship with displacement $x$. This phenomenon needs to be carefully treated, since it will give rise to an adverse effect to the purity of the electrostatic excitation and the stability of the loop, which is left to discuss for subsequent section.

Besides the sensing capacitance, there are also parasitic effects which should be taken into consideration carefully. Parasitic effect includes the serial resistance and stray capacitors as shown in Figure 2.
The parasitic capacitors mainly come from the fringe capacitance of comb fingers the interconnect bonding pads and wires and the input equivalent capacitance of the interface circuit [10,11]. It may have a more detrimental effect on the MEMS accelerometer:

- introduce an inherent residue displacement;
- give rise to harmonic distortion;
- increase the loop instability;
- cause additional bandwidth requirement for the front-end amplifier
- add an uncertain and unstable factor to the bias instability.

**Figure 2.** The parasitic model of the sensing element

Part of the parasitic capacitors can be cancelled out by the correlated double sampling technique or chopping technique, as most of low-noise design used. However, there is another part which is equivalent to a differential change of sensing capacitor, having the same effect as the measurand, and is masked by unknown input acceleration in practical application. The latter part is a problem to which present method is inadequate and is which this paper aims to deal with.

### 3. System Architecture and Self-Test Mode

In this paper we proposed an on-chip self-test and calibrate method for suppressing the above-mentioned problem. The proposed method is accommodated to the Electro-Mechanical Sigma-Delta accelerometer (EM-ΣΔ) which is the most advanced detection method at present. The whole system architecture is shown in Figure 3.

**Figure 3.** The system architecture of EM-ΣΔ accelerometer with proposed self-test function

The main system includes the MEMS sensing element accompanying a pair of reference capacitance, configuring a fully-differential capacitance bridge. The differential change of this capacitance bridge is read out by a fully-differential pre-amplifier. As mentioned, the whole system
including mechanical part and electrical part is configuring a $\Sigma \Delta$ modulation loop, this is accomplished by a following 3-order electrical modulator and the electrostatic force effect. The MEMS sensing element is highly underdamped and the modulator is high order, these two effects mixed together resulting serious stability problem. Thus, a loop compensator is inserted between the preamplifier and the electrical modulator to provide additional phase compensation. Previous method resort to a phase-lead compensator to realize this section [9,10,12]. However, the trade-off between loop gain and compensation effectiveness made a sacrifice of open-loop gain. This problem not only give rise to nonideality to the closed-loop performance, but also may introduce instability due to the positive feedback effect of displacement to electrostatic force. Thus, in this paper, the traditional phase-lead compensator is replaced by a novel SC-PID compensator. The introduction of an additional integrating stage could effectively enhance the in-band loop gain, and at the same time the phase margin is retained by the phase lead introduced by the PD stage.

The self-test function is realized based on electrostatic force generated by an on-chip digital resonator. As mentioned, the EM-$\Sigma \Delta$ modulation loop is accommodated to 1-bit digital signal, thus giving facilities to the exerting of digital excitation. The digital resonator is $\Sigma \Delta$ modulated too, using the technique introduced in [13]. Due to the closed-loop working configuration, the digital excitation could be injected at proper inner node of the whole loop and transfer to the MEMS structure whereby the loop transfer function. This effect is another benefit for digital self-testing which the EM-$\Sigma \Delta$ architecture provides.

The most proper injecting node is the integrational stage of PID compensator. This is due to the fact that, at this node the digital excitation could excite a proper oscillation amplitude of the MEMS structure, and the quantization noise contained in the digital excitation could get pre-filtering to avoid saturating the electrical modulator.

According to the abstracted signal flow diagram as shown in Figure 4, the resulted system output voltage due to the excitation, can be obtained from (3-4):

\[
\begin{align*}
\left\{ \frac{-V_{\text{out}}}{V_s} K_{V-a} H_{ms}(z) K_{s-c} K_{C-PD} + V_T \right\} H_I(z) - \frac{V_{\text{out}}}{V_s} K_{V-a} H_{ms}(z) K_{s-c} K_{C-PD} H_{PD}(z) \right\} \frac{L_0(\xi)}{1 + L_I(\xi)} = V_{\text{out}} \\
V_{\text{out}} = \frac{H_I(z)}{1 + L(z)} + G_0(z)(H_{PD}(z) + H_I(z)) \approx \frac{1}{G_0(\xi)}
\end{align*}
\]
Where, \( G_0(z) = \frac{K_{V,\ldots}H_{ms}(z)K_{v,-c}K_{c,-V}}{V_S} \) \( (5) \)

As shown in equation (3), as long as the in-band loop gain is sufficiently large the self-test response is only determined by the forward gain expression \( G_0(z) \).

At this condition, the harmonic in self-test output can be calculated.

First, we consider the normal working condition (e.g. there is no \( C_p \) effect). At this time, the affect of residue displacement \( x \) should not be omitted, or else the harmonic terms cannot present.

The relationship between \( x \), \( V_T \), \( D_{out} \) can be expressed by (6-7)

\[
\frac{C_0d_0(V_F + V_S)^2}{4} \left[ \frac{1 + D_{out}}{(d_0 + x)^2} - \frac{1 - D_{out}}{(d_0 - x)^2} \right] H_{ms} = x
\] \( (7) \)

Expand expression (5) and (6), and use Taylor expansion omitting high-order terms we can get (7-9)

\[
x = \eta_0 V_T, \quad \eta_0 = \frac{C_f d_0}{4V_S C_0}
\] \( (8) \)

\[
D_{out} = \left[ \frac{1}{A_0} x (d_0^2 - x^2)^2 + 4d_0x \right] \frac{1}{2(d_0^2 + x^2)}
\]

\[
= \left[ \frac{d_0^4}{A_0} + 4d_0 \right] x - \frac{2d_0^2}{A_0} x^3 + \frac{1}{A_0} x^5 \right] \frac{1}{2d_0^2} \left( 1 - \left( \frac{x}{d_0} \right)^2 + \left( \frac{x}{d_0} \right)^4 \ldots (-1)^n \right) \left( \frac{x}{d_0} \right)^{2n}
\]

\[
\approx \alpha_0 + \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3 + \alpha_4 x^4 + \alpha_5 x^5
\]

\[
A_0 = \frac{1}{4} C_0 d_0 (V_F + V_S)^2 H_{ms}
\]

\[
\alpha_0 = \alpha_2 = \alpha_4 = 0, \quad \alpha_1 = \frac{d_0^2}{2A_0} + \frac{2}{d_0},
\]

Where,

\[
\alpha_3 = -\frac{3}{2A_0} - \frac{2}{d_0^3}, \quad \alpha_5 = \frac{1}{2A_0} + \frac{2}{d_0^3} + \frac{3}{2A_0 d_0^3}
\] \( (10) \)

From above deduction, we could find that if there is no parasitic capacitor there will be no even-order harmonics in the self-test.

On the contrary, if there is a parasitic capacitor \( C_p \), then it will introduce a constant term \( x_0 \) in residue displacement \( x \), then the displacement \( x' \) can be expressed as:

\[
x' = x_0 + x, \quad x_0 = \frac{C_p d_0}{C_0} \left( \frac{d_0}{2} \right)
\] \( (11) \)
When the in-band gain is sufficiently large, the expression (5) still holds. The harmonics can be obtained by substituting \( x \) in equation (9) by the \( x' \), and the new expression can be got:

\[
D_{\text{out}} = \alpha_0' + \alpha_1'(x + x_0) + \alpha_2'(x + x_0)^2 + \alpha_3'(x + x_0)^3 + \alpha_4'(x + x_0)^4 + \alpha_5'(x + x_0)^5
\]

\[
= \alpha_0' + \alpha_1'x + \alpha_2'x^2 + \alpha_3'x^3 + \alpha_4'x^4 + \alpha_5'x^5
\]

The new coefficient \( \alpha_0' \sim \alpha_5' \) can be obtained by rearrangement as:

\[
\alpha_i' = \sum_{n=0}^{5} C_n \alpha_n x_0^n, \quad i = 1, 2, 3, 4, 5
\]

From above analysis, we can find that when there is a parasitic capacitor, it will induce even-order harmonic terms in output expression. The amplitude of the even-order harmonic is proportional to the parasitic induced displacement \( x_0 \). Thus, the amplitude of even-order harmonic distortion is a representation of parasitic mismatch, by detecting those harmonics and making a calibration according to the detected level, the parasitic effect could get effectively suppressed.

4. Results and Discussions

The proposed system is implemented using 0.35 \( \mu \)m CMOS BCD process. The electromechanical sigma-delta read out interface is implemented by analog part. Besides that, the digital self-test and calibrate circuit is implemented by digital part. The photo diagram of the chip is shown in Figure 5. The total area of the ASIC is 13.2 mm\(^2\), the digital self-test part occupies less than 1/3 of the total area.

![Figure 5](image_url)

Figure 5. The photo diagram of the whole chip.

The spectrum of self-test excitation and the resultant output is shown in Figure 6. It can be seen that the digital excitation source is well performed, the achieved noise floor is less than -180dB far more less than that of the system under test whose noise floor is about -100dB. And the harmonic distortion of the self-test is well suppressed which is on the level of -170dB. Thus, the excitation source is well qualified for the self-test process. Besides in Figure 5, we could find that due to the existence of parasitic mismatch, there are obvious second order terms in the output spectrum, which is as high as -75dB.
Figure 6. The spectrum of self-test excitation resultant output.

By the self-test result, a calibration signal is generated on-chip and imposed on the auxiliary input pair of the front-end amplifier. As shown in Figure 7, after the adjustment of the calibration signal the second order harmonic of the system is well suppressed which means the parasitic mismatch is effectively calibrated out.

Figure 7. The output spectrum at self-test excitation before and after calibration.

5. Conclusions
This paper proposed a digital calibration method for the EM-ΣΔ MEMS accelerometer. The digital calibration method relies on the self-excitation of the MEMS element by an on-chip digital excitation source. The digital excitation method is well accommodated to the sigma-delta interface, and achieves a high-performance at a lower area cost. By analysis of the loop function, we point out that the detrimental parasitic mismatch is highly related to the even-harmonics of the self-test output. Further, by detecting the even-harmonics level and calibrating the system according it, the total parasitic mismatch could get well suppressed. And hence, the system linearity and stability could get enhancement.
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