DSA-aware multiple patterning for the manufacturing of vias: Connections to graph coloring problems, IP formulations, and numerical experiments

Dehia Ait-Ferhat, Vincent Juliard, Gautier Stauffer, and Juan Andres Torres

1Mentor Graphics Corporation. E-mail: {vincent.juliard@mentor.com, andres.torres@mentor.com}
2Center of Excellence in Supply Chain Innovation and Transportation (CESIT). Kedge Business School, Talence, France. E-mail: gautier.stauffer@kedgebs.com
3dehia.aitferhat@gmail.com

Abstract

In this paper, we investigate the manufacturing of vias in integrated circuits with a new technology combining lithography and Directed Self Assembly (DSA). Optimizing the production time and costs in this new process entails minimizing the number of lithography steps, which constitutes a generalization of graph coloring. We develop integer programming formulations for several variants of interest in the industry, and then study the computational performance of our formulations on true industrial instances. We show that the best integer programming formulation achieves good computational performance, and indicate potential directions to further speed-up computational time and develop exact approaches feasible for production.

1 Preliminaries

For the past decades, one of the main drivers of the explosion in the adoption of electronic components in our daily lives has been the addition of more functionality at a lower cost. This has traditionally been achieved by scaling down the geometries in the devices. At every technology node, new production methods allow devices to occupy less total space while at the same time enabling other properties, such as lower power consumption and faster switching.

However, in the last few years, the challenge of continuing on this rapid trajectory to ever-smaller feature sizes has increased: moving from 193nm lasers to a 13nm wavelength (in Extreme Ultra-Violet (EUV)) has required the complete redesign of lithography systems from optical diffraction to reflection projection systems. At 13nm, this radiation is mostly absorbed in the materials, rather than diffracted or reflected. Due to all the challenges associated with this technology, the industry has started using multiple patterning techniques where the design is separated into multiple patterning steps when a dense pattern in a single exposure is not possible. At and below 22nm technology nodes, it is impossible to reproduce the intended features using a single lithographic step, and the industry has thus resorted to using double, and in some cases triple, patterning.

However, the move to multiple patterning also has scaling implications. It reduces the total throughput of the system, and while a piece of equipment could previously process $N$ number of wafers, now the actual number is $N/i$ where $i$ is the number of patterning steps. So while denser patterns can be achieved, the process does not become immediately more cost-effective.

As a consequence, interest has grown in finding process technologies that cost-effectively reduce the total number of patterning steps. While EUV is one such technique, the investment in new lithography equipment, 13nm light sources, power requirements, and the development of new production materials has led to the search for alternatives. DSA (Directed Self Assembly), is one of these techniques that can in principle achieve finer feature sizes with a lower number of patterning steps.

---

1A technology node refers to a semiconductor manufacturing process. It usually takes the form of a distance, e.g., 193nm, 22nm, and is historically closely linked to chip density. [https://en.wikichip.org/wiki/technology_node](https://en.wikichip.org/wiki/technology_node)
The self-assembly process uses the thermodynamic properties of diblock copolymers to form lines or circles on a surface. These structures are randomly formed and controlled by the diblock copolymer architecture. The main idea is to chemically join two different types of polymers, such as polystyrene (PS) and poly(methyl methacrylate) (PMMA). Unless chemically bonded, they would separate at a macro level. However, when a molecule is composed of half PS and half PMMA, the molecules cannot macro separate, and therefore align in ways where PS attempts to surround itself with other PS segments, and PMMA with other PMMA segments.

As random micro-patterns are not very useful in semiconductor manufacturing, guiding patterns can be shaped that direct how the material alignment will take place. The idea is to exploit the diblock copolymers properties to achieve the necessary assembly to transfer the desired pattern onto a wafer. Ingeniously combining adequate guiding patterns with multiple patterning can then help reduce the number of patterning steps. This process is referred to as DSA-aware multiple patterning. In this paper, we investigate the corresponding process from an optimization point of view, starting with a gentle introduction for non-experts.

2 A gentle introduction to DSA-aware multiple patterning

During the fabrication of integrated circuits, a large number of transistors are etched over a silicon wafer (or silicon substrate). Then, a dense network of metal conductors is deposited on multiple layers within the dielectric material (non-conductive medium) on top of the transistors. The network provides the electrical current paths among the different components (see Fig. 1 for illustrations of integrated circuits). As illustrated in Fig. 1(a), the layers are typically of two kinds: either they contain (non-crossing) segments or snake-like shapes that somehow connect components horizontally - the corresponding metal shapes are called wires, and we refer to such layers as metal layers, or, they contain vertical square cylinders that allow connecting successive metal layers - the corresponding metal shapes are called vias and we refer to such layers as via layers. DSA-aware multiple patterning combines lithography and Directed Self-Assembly technologies. We now detail the two technologies and the corresponding process.

Figure 1: (a) a 3D view of an integrated circuit (source: https://commons.wikimedia.org/wiki/File:Silicon_chip_3d.png); (b) a cross-section of an integrated circuit: the first layers represent the substrate and the transistors, the dark red components represent metal ‘wires’, and the purple components represent vias.

Observe that we might superimpose several square cylinders in consecutive (metal and via) layers so that the corresponding metal component connects non-successive metal layers. The corresponding component is also referred to as a via in the industry.
Lithography

Lithography is typically used to ‘transfer’ geometrical features (vias, segments, or other objects) of the same layer from a mask to the wafer. This is achieved by exposing a light-sensitive chemical photoresist that is deposited on the wafer to a light source through the mask. This creates a ‘mold’ that can later be ‘filled’ with a conductive material through various chemical operations, a process called etching. The arrangement of features to be transferred is usually referred to as a layout. Fig. 2 shows two different examples of a layout (viewed from the top). Note that in our illustrations, we usually draw ‘idealized’ shapes for the features. In particular, we adopt the Electronic Design Automation (EDA) convention of representing vias as squares (we also assume that the squares are of equal size within a given via layer, which is also common practice). If the same shapes were used on the mask, the final shapes on the silicon wafer would differ due to optical distortions, which may depend on the technology used, but the transferred shapes are typically more rounded (see Fig. 3) so that a square on the mask generates a squircle (rounded square), or for a more advanced technology node, a circle on the wafer. As long as the network structure is preserved, the precise shape of the features on the wafer does not matter much. Optimal proximity correction (OPC) might be used to adjust the shapes on the mask upfront to ensure that the final arrangement is as close as possible to the targeted one. In addition, functional tests are performed on the final circuit to verify that manufacturing was successful. The reader can refer to [1] for a more detailed overview of the whole lithography process.

Optical distortions could induce network defects, such as the disruption of a wire or the ‘fusion’ of several wires (see Fig. 3). This occurs when the features are too close to each other. The minimum distance permitted between any two features to prevent defects is usually referred to as lithography distance (or resolution), which we denote with \( \text{Litho}_{\text{dist}} \) (note that the distance we consider between
two features \( f_1, f_2 \) is the Euclidean distance i.e., \( \min_{x \in f_1, y \in f_2} ||x - y||_2 \), that is, the distance border to border). For instance, 193 immersion technology has a resolution limit of 45nm \[11\], while the next generation of lithography, based on Extreme Ultra-Violet (EUV) light, allows lowering the resolution to 27nm \[24\]. As EUV is currently not used at a large production scale, and lithography technologies have tended to reach their limit, the industry is seeking other solutions to further lower the resolution (currently targeting sub-7 nm resolution). As pointed out in Section \[1\], multiple patterning is one such solution.

Multiple patterning is conceptually simple: the idea is to decompose the original layout into feasible sub-layouts that will be etched with different masks, one after the other, to produce the original arrangement. While multiple patterning may potentially decrease the minimum possible distance between the features within a layer, it substantially increases production costs and time. Indeed, masks are expensive, and given the fact that modern integrated circuits might contain fifteen to twenty layers (and typically involve around fifty rounds of lithography), the cost of all masks needed to manufacture an integrated circuit could reach millions of dollars. Furthermore, one of the main drawbacks of multiple patterning is alignment. For instance, in the case of double patterning, first, the features of the first sub-layout are etched on the silicon wafer. Then, the features of the second sub-layout have to be aligned with the first set of printed features and etched on the silicon wafer. When the number of patterning steps increases, the perfect alignment of features from different masks becomes challenging. Together with the reduction in the throughput discussed in Section \[1\], these are the main reasons why the number of patterning steps used in the industry is usually kept small.

The current standard in manufacturing is in fact to use double patterning (DP) in most cases, and then triple patterning (TP) or quadruple patterning (QP) when DP is not feasible. Quadruple patterning allows managing most (current) practical situations, but again, due to increased production costs and time, the industry is seeking solutions to minimize the number of patterning steps in the production of each layer. The corresponding problem readily translates into a graph coloring problem. Indeed, consider the graph whose node set are the features and where two nodes are adjacent if the distance between the corresponding features is below the lithography distance. This graph is usually called the conflict graph. Minimizing the number of patterning steps is equivalent to finding the chromatic number of this graph, that is, the minimum number of colors needed to color the vertices of the graph such that no pair of vertices within the same color are adjacent (a coloring with this latter property is usually called proper).

Proper (vertex) coloring is a notoriously NP-hard problem \[25\] and testing whether a graph can be colored with a fixed number \( k \geq 3 \) of colors is NP-complete \[40\]. The problem can be solved in polynomial time for some very specific classes of graphs, such as perfect graphs \[15\] or graphs with bounded tree-width \[8\] for instance, but usually remains hard even when additional assumptions are made on the graph structure (for a recent survey of complexity results and algorithms for graph coloring, see \[14\]). As conflict graphs arising from manufacturing an integrated circuit have some structure, it is natural to wonder whether this allows for polynomial time algorithms. For instance, as conflicts arise from proximity, when restricting to the manufacturing of vias, and if assuming that we are fine with producing (equal size) cylinders - and not squares - the corresponding graphs are unit disk graphs. Unfortunately, the problem remains hard in this class of graphs (even for planar unit disk graphs and also simply checking 3-colorability) \[30\]. Some authors have studied other types of structures that might be relevant \[17\]. Computational complexity and exact and heuristic approaches for proper vertex coloring have been surveyed in \[35\] and \[30\]. For additional references on exact approaches, see also \[9\] \[18\] \[31\] \[32\] \[16\] \[29\]. Furthermore, from the application side, several exact and heuristic approaches have been developed, see \[28\] for a survey.

There is strong industrial interest in new processes that can be used on top of multiple patterning to further reduce the number of patterning steps. Directed Self Assembly (DSA) has been identified as a promising solution in the manufacturing of vias, as other alternative techniques such as stitching are not applicable in this context \[27\].

**Directed Self Assembly (DSA)**

DSA is a chemical approach based on *block copolymers (BCP)* – a combination of two different structures (i.e., attraction between different molecules) – that works as follows: a region, called a *guiding pattern*, is filled with BCP in a ‘random’ state (i.e., an unorganized mixture of different blocks of

\[3\] This is usually the case.
Figure 4: Example of DSA-aware Triple Patterning. The layout is decomposed into three sub-layouts (red, blue, green). We detail the manufacturing of the red sub-layout using DSA: (i) there are two pairs of vias that are in conflict in the red sub-layout (we do not provide the resolution here but it can be selected as precisely the smaller distance between any two vias in the red sub-layout); (ii) the corresponding pairs are grouped into peanut-like guiding patterns that will be used to direct the assembly of the block copolymer; (iii) the associated mask is then created, taking into account optical distortion; (iv) the guiding patterns for the red sub-layout are then manufactured through one lithography step; (v) finally, the vias are etched through DSA.

molecules). After a certain chemical reaction is triggered (called a microphase separate anneal), the BCP assembles into a periodic arrangement of homopolymer structures: the periodic structures can be cylinders, lamella, or other geometric structures. These structures depend on the nature of the block copolymer and the volume fraction (the ratio of volume occupied by the two homopolymers). In this work, we are interested in the periodic cylinder structures as they might be used as vias. Indeed, one can combine microphase separate with additional chemical steps to retain the negative of cylinders.

Such a process can readily be combined with lithography to reduce the number of patterning steps in the manufacturing of vias. The whole idea in mixing DSA and lithography is to group some vias into guiding patterns that could otherwise not be assigned to the same mask. Lithography is then used to ‘mold’ the guiding patterns, and DSA is used to etch the vias that lie within these patterns (see Fig. 4 for an example). We distinguish two kinds of masks in this process: we call DSA mask a mask that involves a non-trivial guiding pattern (at least two vias are grouped in this mask), and Litho mask a mask that does not involve guiding patterns. Manufacturing constraints impose that a DSA mask can only use one block copolymer to etch vias within that mask: indeed all vias in the mask are etched through DSA after all guiding patterns have been printed through lithography (even single vias of this mask will be printed with DSA and will thus appear as cylinders on the wafer). In this study, we additionally assume that we only use one block copolymer for all masks. The production costs of this new process are again dominated by the cost of the masks, and production throughput is again limited by the number of patterning steps. Hence, it is still essential to minimize the number of lithography/patterning steps.
Heuristics and exact approaches for multiple patterning with DSA (and variants) have been investigated in [5, 12, 20, 37, 38, 43]. Note that in all studies, the number of patterning steps is fixed and the goal is to group vias into feasible guiding patterns so as to minimize the number of conflicts remaining (allowing sometimes for the insertion of redundant vias). In contrast, this work focuses on the “pure” coloring problem, that is, explicitly finding the minimum number of patterning steps needed for manufacturing with DSA (with no conflict allowed). This is motivated by two different goals: the first to formally demonstrate the potential benefits that DSA-aware multiple patterning could bring (over pure multiple patterning), and the second to allow assessing the quality of the heuristics developed in-house by Mentor Graphics.

In principle, it would be possible to use the exact methods developed in some prior studies in parallel: run the algorithm for a given number of patterning steps and then verify for which number of patterning steps zero coloring conflicts emerge. However, most of these methods either employ heuristics to accelerate finding a coloring solution at a large scale (and hence no longer guaranteeing optimality) [37, 43], propose formulations that do not work for any number of patterning steps [5, 20], or exploit additional structures and/or placement options [12, 20, 33]. In our case, given that the objective is to formally find the minimum number of patterning steps required for (large scale) layouts, we do not build on the methods developed in prior research.

Beyond the relevance from a practical point of view, we believe that our new models deserve additional attention from the combinatorial optimization community, as they are natural extensions of proper graph coloring and may find other applications beside integrated circuit manufacturing.

3 Relation to graph coloring and IP formulations

There are several natural ways of exploiting DSA within Multiple Patterning. We now detail a few variants that are of particular interest to the industry, their relation to graph coloring problems, and some ‘natural’ integer programming formulations. Note that we essentially extend the standard assignment-based integer programming formulations for vertex coloring (of course, the generalization brings other complications). We will now explain the rationale behind this choice. While it is known that the corresponding model contains color symmetries, and that the corresponding linear relaxation is weak [21, 30], it has the advantage of being easily implementable in modern solvers such as CPLEX or GUROBI. In our setting, because the upper bound on the number of colors is small, the color symmetries are limited, and therefore not very problematic (actually, we undertook some preliminary tests with column generation approaches in BaPCod [3], and the ‘assignment’ formulations implemented with Cplex 12.6.3 always performed better; indeed, experts of decomposition techniques [11] confirm that this is not surprising as the sub-problem is ‘as hard’ as the original one when the chromatic number is small). Furthermore, many specific cuts, such as clique inequalities for instance, are available in these solvers so we can also easily strengthen the formulation by simply activating well-known strong cuts for the problem (cliques, Chvatal-Gomory cuts, etc...).

3.1 Pairing vias

The first obvious idea to exploit DSA together with lithography is to attempt to group vias by pairs. As known [5], two vias can be grouped if they stand within a distance in a range of $[L_0, U_0]$ (center to center), which depends on the BCP, and if they satisfy additional constraints based the lithography technology (for instance, in 193 immersion, the contours of the guiding patterns have to be parallel to the x and y axis).

In this case, minimizing the number of patterning steps in DSA-aware Multiple Patterning is a simple variant of graph coloring. Let $G = (V,E)$ be the conflict graph associated with the chosen lithography technology. Let $F \subseteq E$ be the set of edges of $E$ whose extremities are within a distance between $L_0$ and $U_0$, and satisfy the additional lithography constraints associated with the technology (we sometimes call such edges DSA edges). The problem is coloring the vertices of $G$ with a minimum number of colors so that each color induces a disjoint union of nodes of $G$ and edges of $F$, or, alternatively, each color induces a graph where all nodes have at most 1 degree and all edges are in $F^\parallel$. When $F = E$ the problem is known as 1-improper coloring and is NP-hard [19]. In fact, according to the same authors, it is already hard to check whether a graph admits a 1-improper 2-coloring. To the best of our knowledge, the problem has not yet received much attention from the combinatorial

---

4This assumes that guiding patterns are in conflict with other guiding patterns if and only if some of the corresponding vias are in conflict, which is a reasonable assumption according to the industry given the typical values of $L_0, U_0$ and $\text{Litho}_{dist}$. 

6
We denote with $L$ the set 
\begin{align*}
\{1, \ldots, L\}
\end{align*}
because most designs can be solved with quadruple or quintuple patterning, $L$ can be set to 4 or 5, as a proper coloring is obviously 1-improper.\footnote{We denote with $[L]$ the set \{1, \ldots, L\} and with $N_F(u)$ the neighbors of $u$ in the subgraph $G_F := (V, F)$.}

\[
\min \sum_{i=1}^{L} \lambda^i 
\]

\[
\sum_{i=1}^{L} z^i_u = 1, \quad \forall i \in [L], \forall v \in V 
\]

\[
z^i_u + z^i_v - 1 \leq x^i_{(u,v)}, \quad \forall i \in [L], \forall (u,v) \in F 
\]

\[
\sum_{v \in N_F(u)} x^i_{(u,v)} \leq 1, \quad \forall i \in [L], \forall u \in V 
\]

\[
z^i_u + z^i_v \leq 1, \quad \forall i \in [L], \forall (u,v) \in E \setminus F 
\]

\[
z^i_u, x^i_{(u,v)} \leq \lambda^i, \quad \forall i \in [L], \forall u \in V, \forall (u,v) \in F 
\]

\[
z^i_u, x^i_{(u,v)}, \lambda^i \in \{0, 1\}, \quad \forall i \in [L], \forall u \in V, \forall (u,v) \in F 
\]

Variable $\lambda^i$ indicates whether color $i$ is used, $z^i_u$ indicates whether vertex $u$ is assigned color $i$, and $x^i_{(u,v)}$ indicates whether edge $(u, v)$ belongs to color $i$ (that is, with both extremities in color $i$). Constraint (2) ensures that each vertex is colored. Constraint (3) ensures that if an edge of $F$ is not selected within color $i$, then the extremities cannot both receive color $i$. Constraint (4) ensures that no vertex of color $i$ is adjacent to more than one other vertex within that color (through an edge of $F$). Constraint (5) ensures that there is no conflict within a color. Finally, (6) ensures that vertices and edges are assigned to a color only if the color is selected. The number of constraints and the number of variables in this formulation are in the order of $O(Ln^2)$, where $n$ is the number of nodes of the graph.

### 3.2 Small groups

In principle, it is possible to group more than two vias within guiding patterns. Indeed, design rules for guiding patterns have been investigated with explicit constraints on feasible groups in \cite{12} and \cite{10}. However, for the time being, there are only few specific shapes of guiding patterns that are validated. Furthermore, as the guiding patterns will have to be etched using lithography, the lithography technology will also have an impact on the feasible groups (as in the case of pairing, see above). The feasibility of guiding patterns can be verified through a procedure called DSA flow. If we assume that we are given a complete list $V \subseteq 2^U$ of all feasible groups (including singletons) and a complete list $E$ of all pairs of $V$ in conflict (in particular, two groups containing the same via will be in conflict), we can model the problem as another variant of graph coloring. Let $G$ be the graph with vertex set $V$ and edge set $E$. We want to find a subset $U$ of groups of $V$ satisfying $\bigcup_{g \in U} g = V$ with $\chi(G[U])$ (the chromatic number of $G[U]$) minimum.

Of course, we might consider variants of this problem where $V$ is a subfamily of feasible groups that have been validated, such as pairs of vias, for instance. In practice, a limited number of vias can be grouped due to manufacturing constraints. The maximum number of vias per group might evolve in the future, but with current technology is typically limited to two or three. This gives rise to the following mixed integer program ($L$ is again an upper bound on the number of colors):
Note that some authors use the same terminology for another variant of graph coloring, see for instance [13, 24, 34].

and instead build the optimal groups together with the coloring. To develop integer programming is tempting in this case to try to develop models that avoid the enumeration of the feasible groups.

When the maximum size $k$ of the groups increases (even if still bounded - consider $k = 6$ for instance), the previous model would quickly become too large to be handled by a modern solver for practical size instances, as the number of variables and the number of constraints grow exponentially in $k$. It is tempting in this case to try to develop models that avoid the enumeration of the feasible groups and instead build the optimal groups together with the coloring. To develop integer programming models in this case, we must understand and exploit the structure of the groups.

The main certified feasible groups put forth in [10, 7] concern ‘paths’ of vias. We focus on this special case, as this is what industrial companies are currently mainly interested in. We also assume that we have a bound $k$ on the number of vias in the paths (see the discussion in Section 3.2.

As discussed in Section 3.1, vias at distance in $[L_0, U_0]$ can be paired. In fact, under some additional conditions on the path obtained, they can be ‘chained’. More formally, let $G = (V, E)$ be the conflict graph associated with the chosen lithography technology. Let $F \subseteq E$ be the set of edges of $E$ whose extremities are at distance (center to center) in $[L_0, U_0]$. Manufacturing constraints allow associating feasible groups with induced paths of length $k - 1$ (the length of a path counts the number of edges) in the subgraph $G_F = (V, F)$ as long as it complies with the constraints associated with the lithography technology used. For instance, in 193 immersion, the paths have to be parallel to the x or y axis, and in EUV, the angle (degree) between any three consecutive vias in the paths should be in the range of $[135, 225]$.

If we ignore the lithography-specific restrictions (we can easily add the corresponding restrictions later in the integer programming model, see Section 3), the problem is yet another variant of graph coloring that can be described as follows. Given a graph $G = (V, E)$, $F \subseteq E$, and an integer $k \geq 1$, color the nodes of $G$ so that each color induces a disjoint union of paths of length at most $k - 1$, using only edges of $F$.

When $k = 1$, the problem is a standard graph coloring problem. When $k = 2$, the problem only allows pairs and is thus closely related to the 1-improper coloring problem. For larger values of $k$ and when $F = E$, the problem was introduced by Jinjiang proved that the $(2, 2)$-path coloring problem and the $(3, 3)$-path coloring problem are NP-complete [23, 22]. Thus, the $1$–path $2$–coloring and the $2$–path $3$–coloring problems are already NP-complete. We again develop a natural integer programming formulation for the problem when $k \geq 2$ (for $k = 1$, we can use the standard coloring formulation).

$\min \sum_{i=1}^{L} \lambda^i$ (8)

$\sum_{i=1}^{L} \sum_{g \in V} x^i_g = 1, \quad \forall v \in V$ (9)

$x^i_f + x^i_g \leq 1, \quad \forall i \in [L], \forall (f, g) \in E$ (10)

$x^i_f \leq \lambda^i, \quad \forall i \in [L], \forall g \in V$ (11)

$x^i_g, \lambda^i \in \{0, 1\}, \quad \forall i \in [L], \forall g \in V$ (12)

Variable $\lambda^i \in \{0, 1\}$ indicates whether color $i$ is chosen, and $x^i_g \in \{0, 1\}$ indicates whether a group $g \in V$ is colored with color $i$. Constraint (9) imposes that each node $v \in V$ is assigned to exactly one group and one color. Constraint (10) imposes that two groups $f$ and $g$ in conflict have to receive different colors.

In this case, such a naïve enumerative approach appears to perform pretty well, as we will see in Section 4.

### 3.3 Larger groups

When the maximum size $k$ of the groups increases (even if still bounded - consider $k = 6$ for instance), the previous model would quickly become too large to be handled by a modern solver for practical size instances, as the number of variables and the number of constraints grow exponentially in $k$. It is tempting in this case to try to develop models that avoid the enumeration of the feasible groups and instead build the optimal groups together with the coloring. To develop integer programming models in this case, we must understand and exploit the structure of the groups.

The main certified feasible groups put forth in [10, 7] concern ‘paths’ of vias. We focus on this special case, as this is what industrial companies are currently mainly interested in. We also assume that we have a bound $k$ on the number of vias in the paths (see the discussion in Section 3.2.

As discussed in Section 3.1, vias at distance in $[L_0, U_0]$ can be paired. In fact, under some additional conditions on the path obtained, they can be ‘chained’. More formally, let $G = (V, E)$ be the conflict graph associated with the chosen lithography technology. Let $F \subseteq E$ be the set of edges of $E$ whose extremities are at distance (center to center) in $[L_0, U_0]$. Manufacturing constraints allow associating feasible groups with induced paths of length $k - 1$ (the length of a path counts the number of edges) in the subgraph $G_F = (V, F)$ as long as it complies with the constraints associated with the lithography technology used. For instance, in 193 immersion, the paths have to be parallel to the x or y axis, and in EUV, the angle (degree) between any three consecutive vias in the paths should be in the range of $[135, 225]$.

If we ignore the lithography-specific restrictions (we can easily add the corresponding restrictions later in the integer programming model, see Section 3), the problem is yet another variant of graph coloring that can be described as follows. Given a graph $G = (V, E)$, $F \subseteq E$, and an integer $k \geq 1$, color the nodes of $G$ so that each color induces a disjoint union of paths of length at most $k - 1$, using only edges of $F$.

When $k = 1$, the problem is a standard graph coloring problem. When $k = 2$, the problem only allows pairs and is thus closely related to the 1-improper coloring problem. For larger values of $k$ and when $F = E$, the problem was introduced by Jinjiang proved that the $(2, 2)$-path coloring problem and the $(3, 3)$-path coloring problem are NP-complete [23, 22]. Thus, the $1$–path $2$–coloring and the $2$–path $3$–coloring problems are already NP-complete. We again develop a natural integer programming formulation for the problem when $k \geq 2$ (for $k = 1$, we can use the standard coloring formulation).

---

6Note that some authors use the same terminology for another variant of graph coloring, see for instance [13, 23, 44].
Variable $x'_{(u,v)} \in \{0,1\}$ indicates whether the edge $(u,v) \in F$ is assigned to color $i$. $x'_{(u,v)}$ and $x'_{(v,u)} \in \{0,1\}$ indicate whether the edge $e = (u, v) \in E$ is used as the $(k+1)$-th edge in the direction from $u$ to $v$ or $v$ to $u$ in one of the disjoint paths of color $i$ (explicitly giving an orientation to the path). $y_{i,v} \in \{0,1\}$ indicates whether there is a path that ‘starts’ from $v$ in color $i$ (it might be a path of length 0). $z_{i} \in \{0,1\}$ indicates whether a node $v \in V$ has color $i$ (hence $v$ is in a path of color $i$, possibly of length 0). Finally, $\lambda_{i} \in \{0,1\}$ indicates whether color $i$ is chosen.

Constraints (15) and (16) are ‘flow conservation constraints’ that impose that an edge leaving from $v$ (in color $i$) can be the $(k+1)$-th edge of a path only if there is an edge entering $v$ that is the $\kappa$-th, and that there cannot be a path starting with an edge from $v$ unless $v$ is the first node of the path. Constraint (17) imposes that $(u, v)$ is taken in color $i$ if and only if it is used in one direction or the other in a path. Constraint (18) ensures that a vertex $v$ in color $i$ is either the ‘starting’ extremity of a path of color $i$ or $u \in N_F(v)$ exists such that the edge $(u, v)$ is taken in a path of color $i$ in the direction from $u$ to $v$ (and vice versa). Constraint (19) guarantees that each vertex receives a color. Constraint (20) ensures that if an edge of $F$ is not selected within color $i$, then the extremities cannot both receive color $i$. Constraint (21) ensures that there is no conflict within a color. The number of constraints and the number of variables in this formulation are in the order of $O(L.k.n^3)$, and the number of constraints in the order of $O(L.n^2)$, where $n$ is the number of nodes of the graph and $k$ is the number of nodes in the path. One of the main advantages of this formulation is that it grows linearly in $k$, and could thus, in principle, be implemented in modern solvers for larger values of $k$ than the previous model. However, it is less flexible as it is limited to paths, and as we will see later, is much weaker.

### 3.4 Beyond induced paths

Requiring that paths be induced is somewhat conservative: for instance, three vias that are aligned, whose middle node is at a distance $L_0$ from each extremity, and where the two extremities are in conflict, might qualify for possible grouping (since the corresponding guiding pattern would in principle allow for the proper assembly of the three vias according to $\text{(10)}$). Hence, while induced paths are guaranteed to correspond to feasible groups, other paths might be allowed. However, in practice, it seems that the distances are often such that the situation described above for three vias does not emerge ($\text{Lith}0_{\text{uat}}$ is ‘not too big’ compared to $L_0$), and in the case of 193 immersion in particular, preventing this ‘three vias case’ is enough to ensure that all feasible paths (i.e., parallel to the x or y axis) are actually induced. When testing our model on true instances (see the next section), permitting non-induced paths did not allow better solutions. However, we believe that the relation between $L_0$ and $\text{Lith}0_{\text{uat}}$ might evolve in the future and that studying more general models makes sense.
A natural relaxed assumption is to require that a set $U \subseteq V$ with at most $k$ vias can be grouped if there is a Hamiltonian path in the subgraph $G(U, F)$. The existence of the Hamiltonian path ensures that we can create, in principle, a guiding pattern that closely follows the path that might assemble properly. Of course again, lithography might additionally impose some constraints on the guiding pattern. For instance, one might want to impose that, within a guiding pattern, there are no two vias $v_1$ and $v_2$ that are in conflict, and such that the segment linking these two is not ‘close’ to the path that links $v_1$ and $v_2$ in the Hamiltonian path (otherwise, the position of the vias would certainly differ from what is expected since the guiding pattern might itself differ substantially from the targeted one due to optical distortion): a natural measure of proximity might be to impose that each vertex of the path linking the two vias should be within a certain maximum Euclidean distance from the segment (see Fig. 5 for an example). For 193 immersion, this latter restriction is granted once we impose that the paths are parallel to the axis. For other technologies, such as EUV for instance, checking the corresponding constraints may be cumbersome.

The core problem, when we ignore restrictions arising from any specific lithography technology (again we can introduce the corresponding constraints later on), is a new interesting extension of graph coloring. Given a graph $G = (V, E)$, $F \subseteq E$, and an integer $k \geq 1$, color the nodes of $G$ so that the connected component induced by each color admits a Hamiltonian path of length at most $k - 1$. As $k$ grows, this seems to be a much more challenging problem to solve as it combines the difficulty of coloring with Hamiltonicity, as confirmed by our computational results (see Section 4). We again develop an integer model in the same vein as the previous one for $k \geq 2$. 

Figure 5: Assume that $\text{Litho}_\text{dist}$ is such that all vias within the green and the red guiding patterns are in conflict. The green guiding pattern would be fine, as it is ‘close’ enough to a straight line and would thus not be greatly affected by optical distortion, while the red guiding pattern would certainly induce defects.
min \sum_{i=1}^{L} \lambda^i \\
\sum_{u \in N_P(v)^{t}} x_{(u,v)}^{i,\kappa} \leq y_{v,v^t}^i \quad \text{if } \kappa = 0, \forall i \in [L], \forall v \in V \tag{25} \\
\sum_{u \in N_P(v)} x_{(u,v)}^{i,\kappa} - \sum_{u \in N_P(v)} x_{(u,v)}^{i,\kappa-1} \leq 0, \quad \forall \kappa : k - 2 \geq \kappa \geq 1, \forall i \in [L], \forall v \in V \tag{26} \\
\sum_{\kappa=0}^{k-2} (x_{(u,v)}^{i,\kappa} + x_{(v,u)}^{i,\kappa}) = x_{(u,v)}^{i}, \quad \forall i \in [L], \forall (u,v) \in F \tag{27} \\
y_{v,v^t} + \sum_{\kappa=0}^{k-2} \sum_{u \in N_P(v)} x_{(u,v)}^{i,\kappa} = z_{v^t}^i, \quad \forall i \in [L], \forall v \in V \tag{28} \\
y_{v,o}^i + x_{(u,v)}^{i} - 1 \leq y_{v,o}^i, \quad \forall i \in [L], \forall (u,v) \in F, \forall o \in V \tag{29} \\
y_{u,o}^i + x_{(u,v)}^{i} - 1 \leq y_{u,o}^i, \quad \forall i \in [L], \forall (u,v) \in F, \forall o \in V \tag{30} \\
\sum_{o \in V \setminus \{v\}} y_{v,o}^i = z_{v}^i, \quad \forall i \in [L], \forall v \in V \tag{31} \\
y_{v,v^t} + \sum_{o' \in V \setminus \{v\}} y_{v,o'}^i \leq 1, \quad \forall i \in [L], \forall (u,v) \in E, \forall o \in V \tag{32} \\
\sum_{i=1}^{L} z_{v}^i = 1, \quad \forall v \in V \tag{33} \\
\sum_{(u,v) \in F, (o,o') \in E} x_{(u,v)}^{i,\kappa}, y_{v,o}^i, x_{(u,v)}^{i,\kappa}, z_{v}^i \leq \lambda^i, \quad \forall i \in [L], \forall \kappa = 0, \ldots, k - 2, \forall (u,v) \in F, \forall o, u, v \in V \tag{34} \\
\sum_{(u,v) \in F, (o,o') \in E} x_{(u,v)}^{i,\kappa}, y_{v,o}^i, x_{(u,v)}^{i,\kappa}, z_{v}^i, \lambda^i \in \{0,1\}, \quad \forall i \in [L], \forall \kappa = 0, \ldots, k - 2, \forall (u,v) \in F, \forall o, u, v \in V \tag{35} 

Variable \( x_{(u,v)}^{i} \in \{0,1\} \) indicates whether an edge \((u,v) \in F \) is chosen in a path with color \( i \). \( x_{(u,v)}^{i,\kappa} \in \{0,1\} \) indicates whether an edge \((u,v) \in F \) is used as the \((\kappa+1)\)-th edge in the direction from \( u \) to \( v \) in one of the disjoint paths of color \( i \) (this again explicitly gives an orientation to the path). \( y_{v,o}^i \in \{0,1\} \) indicates whether a node \( v \in V \) is in a path starting in \( o \in V \) with color \( i \in [L] \). \( y_{v,v^t}^i \in \{0,1\} \) indicates whether a node \( v \in V \) is the first node of a path starting in \( v \in V \) with color \( i \in [L] \). \( z_{v}^i \in \{0,1\} \) indicates whether a node \( v \in V \) has color \( i \). \( \lambda^i \in \{0,1\} \) indicates whether a color \( i \) is chosen.

Constraints (25), (26), (27), and (28) have the same meaning as in the previous model. Constraints (29) and (30) identify the path each node belongs to by propagating connectivity, e.g., if \( u \) is in a path of color \( i \) starting in \( o \) and \((u,v) \) is taken in color \( i \) (in the direction from \( u \) to \( v \)), then \( v \) is in the path of color \( i \) starting in \( o \). Constraint (31) imposes consistency for the value taken by \( y_{v,o}^i \) (a vertex is in a path in color \( i \) if and only if it is in color \( i \)). Constraint (32) ensures that two adjacent nodes cannot belong to different paths of the same color. Finally, constraint (33) imposes that each node \( v \in V \) receives exactly one color, and constraint (34) imposes that vertices and paths can be assigned to a color only if the color is selected. The number of variables in the formulation is in the order of \( O(L,k,n^2) \), and the number of constraints is in the order of \( O(L,n^3) \), where \( n \) is the number of nodes of the (original) graph, and \( k \) is the maximum number of nodes in the paths.

4 Numerical experiments

In this section, we report on our computational experiments with the various models described in the previous sections. We tested our models on ten instances, named clip1, . . . , clip10 arising from true industrial layouts at Mentor Graphics (the corresponding layouts are available upon request). The number of vias for each instance are given in Table I.

We do not use the true values for LithoDistast, \( L_0 \), and \( U_0 \) for confidentiality reasons. Instead, following (26), (33), we use three different values of LithoDistast (31nm, 41nm, 49nm note that distance is border to border), and set \( L_0 = 20nm \) and \( U_0 = 40nm \) (note the distance is center to center here).

We re-scaled first the layout so that the minimum distance - border to border - between any two vias corresponds to a targeted pitch size of 10nm and so that the diameter of the vias is also 10nm, as
Table 1: Number of vias for each instance.

| Name  | Number of vias |
|-------|-----------------|
| clip1 | 200850          |
| clip2 | 173741          |
| clip3 | 236979          |
| clip4 | 184486          |
| clip5 | 214697          |
| clip6 | 248375          |
| clip7 | 225795          |
| clip8 | 126029          |
| clip9 | 200850          |
| clip10| 173741          |

Table 2: The number of nodes $|V|$, edges $|E|$, and DSA edges $|F|$ in the ten industrial instances when $\text{Litho}_\text{dist} = 31$ nm

| name  | $|V|$  | $|E|$  | $|F|$  | $|E|/|V|$ |
|-------|-------|-------|-------|---------|
| clip1 | 200850| 198199| 198199| 0,99    |
| clip2 | 173741| 166867| 166865| 0,96    |
| clip3 | 236979| 215657| 206185| 0,91    |
| clip4 | 184486| 154235| 147546| 0,84    |
| clip5 | 214697| 208971| 208970| 0,97    |
| clip6 | 248375| 248323| 248323| 1       |
| clip7 | 225795| 216105| 194251| 0,96    |
| clip8 | 126029| 112741| 111695| 0,89    |
| clip9 | 200850| 198199| 198199| 0,97    |
| clip10| 173741| 166867| 166865| 0,96    |

Table 3: The number of nodes $|V|$, edges $|E|$, and DSA edges $|F|$ in the ten industrial instances when $\text{Litho}_\text{dist} = 41$ nm

| name  | $|V|$  | $|E|$  | $|F|$  | $|E|/|V|$ |
|-------|-------|-------|-------|---------|
| clip1 | 200850| 389723| 198199| 1,94    |
| clip2 | 173741| 325605| 166867| 1,87    |
| clip3 | 236979| 370096| 215657| 1,56    |
| clip4 | 184486| 267536| 154235| 1,45    |
| clip5 | 214697| 430385| 208971| 2       |
| clip6 | 248375| 512810| 248323| 2,1     |
| clip7 | 225795| 371507| 216105| 1,65    |
| clip8 | 126029| 206612| 112741| 1,64    |
| clip9 | 200850| 389723| 198199| 1,94    |
| clip10| 173741| 325605| 166867| 1,87    |
Table 4: The number of nodes $|V|$, edges $|E|$, and DSA edges $|F|$ in the ten industrial instances when $\text{Litho}_{\text{dist}} = 49$ nm.

The density of the graph is reported as $|E|/|V|$, as in [26, 43]. Our industrial layouts actually exhibit a much larger density than the pseudo-industrial instances used in [26, 43]. This makes a huge difference from a computational point of view. Indeed, the computational time is somewhat dominated by the largest connected component (obviously we can parallelize the computation to solve the problem on each connected component independently). The size of the largest connected component for each instance is reported in Tables 5, 6, and 7 (clip1_31 represents the largest connected component of clip1 when $\text{Litho}_{\text{dist}} = 31$ nm, and so on). We do not have the figures for the instances used in [26, 43], however, what they consider as dense graphs are sparser than the sparsest graphs we consider here. This tends to indicate that the size of the largest and the average connected components in their benchmark are typically small, which explains why they have a computational time in the order of a few seconds for the overall instance without parallelization. In the following, we only document the characteristics and report the computational time on the largest connected component, as we believe this provides a better measure of the problem complexity. We also report the maximum clique size ($\omega$) and maximum degree ($\Delta$) of the corresponding instances.

Table 5: Largest connected components in each instance for $\text{Litho}_{\text{dist}}$=31 nm

4.1 $k=2$

In this subsection, we compare our models assuming we can only create groups of at most size two. In this case, we can compare the models from Section 3.1 and Section 3.2. We call pairing the model from Section 3.1 and naïve the model from Section 3.2. We also provide the computational time for proper coloring. ‘Best value’ indicates the best coloring found, ‘time to best’ the time (in seconds) to find the best solution, ‘time to certify’ the time (in seconds) to certify that the solution is optimal (the time limit when no certificate of optimality is obtained), and ‘cplex gap’ the percentage between the best value and the best lower bound. When not even a first feasible solution is found (either because of memory or cpu limits), we use a backslash sign ($\backslash$).

We can observe from our experiments that the naïve model outperforms the pairing model. Indeed,
while the computational times are similar on the sparsest instances ($\text{Litho}_{\text{dist}}=31\ \text{nm}$), the difference becomes more obvious as the density increases. It was quite surprising at first to see that the pairing model cannot solve half of the largest instances within the time limit of 1 hour, while the naïve model can solve all instances within a few minutes (8 minutes at most). However, this is not completely unexpected as the naïve model allows convexifying the integer hull of the paths (this is also true for longer paths) at a price that is not too high when $k$ is small. Furthermore, we believe that CPLEX
can better exploit the structure of the naïve model, as it combines the set partitioning and set packing constraints, both of which are well-studied, and many strong cuts for these problems are embedded in the CPLEX default settings. Interestingly, this analysis is also likely to explain the good performance of the naïve model when $k = 3$, as we will see in the next section.

### 4.2 $k=3$

In this subsection, we compare our models assuming we can only create groups of at most size three. We focus on paths. In this case, we can compare the models from Section 3.2, Section 3.3, and Section 3.4. To eliminate any confusion, we call naïve induced the naïve model instantiated by listing all induced paths of at most length two (i.e., groups of at most length three), naïve general the naïve model instantiated by listing all groups of at most length three that exhibit a Hamiltonian path of length two, induced the model from Section 3.3, and general the model from Section 3.4.

| Coloring | best value | time to best | time to certify | Cplex Gap | best value | time to best | time to certify | Cplex Gap | Instance | best value | time to best | time to certify | Cplex Gap | Instance | best value | time to best | time to certify | Cplex Gap | Instance | best value | time to best | time to certify | Cplex Gap |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| clip1_41 | 6 | 33.75 | 33.75 | 0% | 6 | 33.75 | 33.75 | 0% | 6 | clip2_41 | 6 | 25.31 | 25.31 | 0% | 6 | clip3_41 | 6 | 27.93 | 27.93 | 0% | 6 | clip4_41 | 6 | 21.56 | 21.56 | 0% | 6 |

Table 10: Comparison of the pairing and the naïve model for $k = 2$ and Litho$_{dist} = 49$nm.

| Coloring | best value | time to best | time to certify | Cplex Gap | best value | time to best | time to certify | Cplex Gap | Instance | best value | time to best | time to certify | Cplex Gap | Instance | best value | time to best | time to certify | Cplex Gap | Instance | best value | time to best | time to certify | Cplex Gap |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| clip1_41 | 6 | 33.75 | 33.75 | 0% | 6 | 33.75 | 33.75 | 0% | 6 | clip2_41 | 6 | 25.31 | 25.31 | 0% | 6 | clip3_41 | 6 | 27.93 | 27.93 | 0% | 6 | clip4_41 | 6 | 21.56 | 21.56 | 0% | 6 |

Table 11: Comparison of the naïve induced model and the induced model for $k = 3$ and Litho$_{dist} = 31$nm.

| Coloring | best value | time to best | time to certify | Cplex Gap | Instance | best value | time to best | time to certify | Cplex Gap | Instance | best value | time to best | time to certify | Cplex Gap |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| clip1_41 | 6 | 33.75 | 33.75 | 0% | 6 | 33.75 | 33.75 | 0% | 6 | clip2_41 | 6 | 25.31 | 25.31 | 0% | 6 | clip3_41 | 6 | 27.93 | 27.93 | 0% | 6 | clip4_41 | 6 | 21.56 | 21.56 | 0% | 6 |

Table 12: Comparison of the naïve induced model and the induced model for $k = 3$ and Litho$_{dist} = 41$nm.

We first focus on the case where the paths are induced and then move to the case where we allow for non-induced paths. Here again, the naïve induced model clearly outperforms the ad-hoc induced version. The results are somewhat surprising at first sight since while we would not expect the induced model to perform better than the naïve model on small graphs, we did not expect it to already reach its limits for $k = 3$ when the graphs are large. This calls into question the interest in such model and the existence of better models to cope with larger values of $k$. Indeed, we tried the models with $k = 5$ and observed very similar behavior (our instances are not that well-suited to testing larger values of $k$, as the number of feasible paths does not increase by much when going from $k = 3$ to $k = 5$ or larger, and hence the naïve model will always perform similarly while the induced model will run out of memory even faster). We believe that the clear advantage of the naïve model
Table 13: Comparison of the naïve induced model and the induced model for \( k = 3 \) and Litho\(_{dist} = 49\)nm.

again derives from the fact that CPLEX can exploit the set packing and set partitioning nature of the problem, and the fact that the formulation convexifies the path of length two.

In the case where we allow for non-induced paths, the results are even more in favor of the naïve model, as shown in the following tables. Observe that there is no difference on the optimal coloring whether we allow non-induced paths or not. As noted in the introduction, this has been anticipated by practitioners due to the structure of the industrial instances.

Table 14: Comparison of the naïve general model and the general model for \( k = 3 \) and Litho\(_{dist} = 31\)nm.

Table 15: Comparison of the naïve general model and the general model for \( k = 3 \) and Litho\(_{dist} = 41\)nm.

Table 16: Comparison of the naïve general model and the general model for \( k = 3 \) and Litho\(_{dist} = 49\)nm.

Clearly, the general model seems highly inappropriate. Indeed, for large instances, it cannot even load in memory. This raises the question of the existence of more appropriate models, in the original space for instance, which could compete with the naïve model for small groups and would also allow dealing with larger groups. Relevant models are likely to require exponentially many inequalities, and therefore, the use of cutting plane approaches. However, we leave the corresponding investigations for future research.
4.3 Toward a column-generation approach for the naïve model

One aspect that we have so far not really stressed is the fact that the naïve model relies on a complete enumeration of all feasible paths. Although we mentioned that we could enumerate the corresponding paths using the Networkx Python library, we have not commented on the time spent in this procedure, which, to be fair with respect to the other models, should be included in the computation time. In fact, including the pre-processing time (see Table 17) only marginally changes the conclusion. Nevertheless, it substantially increases the overall computation time.

| Instance | Pre-processing |
|----------|----------------|
|          | naïve induced  | naïve induced | naïve induced | naïve general | naïve general | naïve general |
| clip1    | 0.17 14.17     | 1197.48       | 0.17 15.68    | 1174.25       |
| clip2    | 0.99 14.53     | 1081.53       | 0.09 14.45    | 1050.28       |
| clip3    | 0.03 4.91      | 61.34         | 0.04 4.83     | 60.24         |
| clip4    | 0.12 2.92      | 8.6           | 0.13 2.82     | 8.48          |
| clip5    | 0.14 72.79     | 1308.79       | 0.14 71.22    | 1296.03       |
| clip6    | 0.17 60.53     | 1786.73       | 0.16 59.91    | 1786.39       |
| clip7    | 0.17 24.18     | 1190.55       | 0.17 23.67    | 1194.02       |
| clip8    | 0.09 4.68      | 66.42         | 0.09 4.57     | 66.17         |
| clip9    | 0.09 14.54     | 1099.01       | 0.1 14.33     | 1094.9        |
| clip10   | 0.09 7.39      | 1021.71       | 0.08 7.28     | 1016.18       |

Table 17: Preprocessing times

Given the encouraging performance of the naïve model, we investigate it further. In particular, we evaluate the potential of applying a column generation approach to avoid listing all the feasible paths upfront. For such an approach to be successful, we need to evaluate the quality of the linear relaxation. In so doing, some clique inequalities are easily identifiable for this model, and the model in Section 3.2 can easily be strengthened as follows.

\[
\text{min} \sum_{i=1}^{L} \lambda^i \quad (36)
\]

\[
\sum_{i=1}^{L} \sum_{g \in V: u \in g} x^i_u = 1, \quad \text{for each via } v \quad (37)
\]

\[
\sum_{f \in V: u \in f} x^i_f + \sum_{g \in V: v \in g} x^i_g \leq 1, \quad \forall i \in [L], \forall u, v: d(u, v) \leq L \quad (38)
\]

\[
x^i_g \leq \lambda^i, \quad \forall i \in [L], \forall g \in V \quad (39)
\]

\[
x^i_g, \lambda^i \in \{0, 1\}, \quad \forall i \in [L], \forall g \in V \quad (40)
\]

Variable \( \lambda^i \in \{0, 1\} \) indicates whether color \( i \) is chosen, and \( x^i_g \in \{0, 1\} \) indicates whether a group \( g \in V \) is colored with color \( i \). Constraint (37) imposes that each via is assigned to exactly one group and one color. Constraint (38) imposes that groups in conflict (for which there are two vias that are too close) have to receive different colors.

We compared the performance of this new naïve model when all cuts are deactivated in CPLEX with the original model, with the default cuts activated. We now report the results for the general case with \( k = 3 \) but a similar behavior is observed for the induced case and when \( k = 2 \). It would seem that the new model with no additional cuts performs even better than the original model (with cuts activated). Again this might seem strange at first sight, but can partly be explained by the fact that the clique constraints we identified are probably quite strong already. This is encouraging, as it tends to indicate that the corresponding linear relaxation is strong, and thus that a column-generation approach building on the later formulation might perform rather well, without requiring listing all paths upfront but instead generating the paths ‘on the fly’ by solving a pricing problem. The corresponding promising approach is far beyond the scope of the current study, and we hence leave it for future investigations.
Table 18: Comparison of the original model with the new model with no CPLEX cuts for $k = 3$ and $	ext{Litho}_{\text{dist}} = 31\text{nm}$.

| Instance | best value | time to best | time to certify | Cplex Gap | best value | time to best | time to certify | Cplex Gap |
|----------|------------|--------------|-----------------|-----------|------------|--------------|-----------------|-----------|
| clip1 \_31 | 2 | 3,03 | 3,04 | 0% | 2 | 1,57 | 1,58 | 0% |
| clip2 \_31 | 2 | 2,49 | 2,49 | 0% | 2 | 1,18 | 1,18 | 0% |
| clip3 \_31 | 2 | 0,28 | 0,29 | 0% | 2 | 0,21 | 0,33 | 0% |
| clip4 \_31 | 2 | 0,46 | 0,73 | 0% | 2 | 0,44 | 0,47 | 0% |
| clip5 \_31 | 2 | 1,37 | 1,38 | 0% | 2 | 1,72 | 1,72 | 0% |
| clip6 \_31 | 2 | 3,43 | 3,44 | 0% | 2 | 1,65 | 1,7 | 0% |
| clip7 \_31 | 2 | 0,77 | 1,16 | 0% | 2 | 0,75 | 0,87 | 0% |
| clip8 \_31 | 2 | 0,76 | 0,76 | 0% | 2 | 0,36 | 0,69 | 0% |
| clip9 \_31 | 2 | 1,51 | 1,52 | 0% | 2 | 1,47 | 1,55 | 0% |
| clip10 \_31 | 2 | 0,65 | 0,66 | 0% | 2 | 1,11 | 1,34 | 0% |

Table 19: Comparison of the original model with the new model with no CPLEX cuts for $k = 3$ and $	ext{Litho}_{\text{dist}} = 41\text{nm}$.

| Instance | best value | time to best | time to certify | Cplex Gap | best value | time to best | time to certify | Cplex Gap |
|----------|------------|--------------|-----------------|-----------|------------|--------------|-----------------|-----------|
| clip1 \_41 | 3 | 5,06 | 5,84 | 0% | 3 | 2,87 | 3,08 | 0% |
| clip2 \_41 | 3 | 6,27 | 6,75 | 0% | 3 | 3,21 | 4,05 | 0% |
| clip3 \_41 | 3 | 4,32 | 4,35 | 0% | 3 | 2,77 | 2,83 | 0% |
| clip4 \_41 | 3 | 2,66 | 2,76 | 0% | 3 | 1,94 | 1,95 | 0% |
| clip5 \_41 | 3 | 20,9 | 20,92 | 0% | 3 | 29,18 | 29,25 | 0% |
| clip6 \_41 | 3 | 13,04 | 13,08 | 0% | 3 | 24,6 | 25 | 0% |
| clip7 \_41 | 3 | 5,51 | 5,66 | 0% | 3 | 6,9 | 7,44 | 0% |
| clip8 \_41 | 3 | 3,84 | 4,06 | 0% | 3 | 1,59 | 1,69 | 0% |
| clip9 \_41 | 3 | 5,8 | 5,81 | 0% | 3 | 7,51 | 7,52 | 0% |
| clip10 \_41 | 3 | 7,83 | 7,84 | 0% | 3 | 2,08 | 2,17 | 0% |

Table 20: Comparison of the original model with the new model with no CPLEX cuts for $k = 3$ and $	ext{Litho}_{\text{dist}} = 49\text{nm}$.

| Instance | best value | time to best | time to certify | Cplex Gap | best value | time to best | time to certify | Cplex Gap |
|----------|------------|--------------|-----------------|-----------|------------|--------------|-----------------|-----------|
| clip1 \_49 | 4 | 430,59 | 435,33 | 0,00% | 4 | 289,18 | 289,8 | 0% |
| clip2 \_49 | 4 | 434,67 | 436,65 | 0,00% | 4 | 267,15 | 268,58 | 0% |
| clip3 \_49 | 3 | 24,74 | 24,74 | 0,00% | 3 | 45,83 | 47,85 | 0% |
| clip4 \_49 | 3 | 5,81 | 5,81 | 0,00% | 3 | 10,02 | 10,78 | 0% |
| clip5 \_49 | 4 | 532,91 | 533,12 | 0,00% | 4 | 244,73 | 247,65 | 0% |
| clip6 \_49 | 4 | 1648,19 | 1660,02 | 0,00% | 4 | 541,25 | 541,52 | 0% |
| clip7 \_49 | 4 | 372,98 | 374,51 | 0,00% | 4 | 227,56 | 227,76 | 0% |
| clip8 \_49 | 3 | 34,12 | 34,15 | 0,00% | 3 | 31,83 | 34,08 | 0% |
| clip9 \_49 | 4 | 731,56 | 731,79 | 0,00% | 4 | 196,84 | 197,1 | 0% |
| clip10 \_49 | 4 | 438,94 | 439,87 | 0,00% | 4 | 232,67 | 232,87 | 0% |

5 Conclusion and perspectives

In this study, we have developed several models for the manufacturing of vias through DSA-aware Multiple Patterning. Surprisingly, our computational experiments have shown that the most naïve models performed best on the industrial instances. Of course, this does not mean that other models should not be investigated further. Indeed, we only had access to a limited number of industrial cases that may not be representative of all possible instances. Furthermore, there might be other applications of our models beyond the manufacturing of vias. It would thus be interesting to develop new models that could scale better when $k$ increases. A possible line of research would be investigating models in the original space, which would certainly involve a large (exponential-size) number of constraints, and using such models in practice would therefore require cutting-plane approaches.
Although developing the corresponding models and investigating their performance is beyond the scope of this paper, it would offer fertile ground for polyhedral studies.

One of the main disadvantages of the naive models is that they rely on a complete enumeration of the feasible groups upfront. In our applications, this was not problematic as the number of feasible paths was limited (due to restriction in size but also manufacturing constraints). Nevertheless, our investigations on the quality of the linear relaxation of these models suggest that a column-generation approach might be worth pursuing. In fact, not only should generating the path on the fly reduce the pre-processing time, but it should also considerably decrease the size of the models, which in turn could lead to substantial computational improvements. For the largest instances, the computation times were in the order of 8 minutes in the worst case. We believe that a column generation approach could bring the computational time down to a few tens of seconds, which would then be much more appealing from an industrial point of view (the tools could then be used in real time to evaluate different designs before the production process begins, for instance).

In practice, while the computational time does not really allow using the corresponding models in production, Mentor Graphics used it to identify and improve weaknesses in their heuristics [1]. The heuristics that Mentor Graphics developed exploit the structure of the graphs arising from industrial applications. In this study, we have not attempted to exploit this line of research. Nevertheless, as the graphs are extremely sparse, there are many small cuts (isthmus, for instance) in connected components. Exploiting these structures by decomposing the problem further through Lagrangian relaxation and/or pure clustering ideas could significantly decrease the overall computation time by reducing the core problem to instances with only a few tens of vertices. This is certainly a direction worth investigating (an approach that has already been successfully investigated in [20] but on sparser instances). Moreover, there might be additional structures to explicitly exploit. We observed in many instances that the sparse graphs are ‘close to trees’, and deem that the case of graphs with small tree-width is particularly relevant from an application perspective. We are currently investigating algorithms that exploit such property. In particular, we may prove that the k-path coloring problem is polynomial in this case and develop efficient dynamic programming algorithms [1, 2]. Other structures such as those identified in [17] may be worth investigating.

A side benefit of the naive model is that it allows introducing additional ‘validated’ guiding patterns and easily adding other constraints. For instance, we have not considered constraints between groups in different masks. However, depending on the technology used, there might be additional constraints to take into account. For instance, two pairs of vias may lead to two guiding patterns that intersect, and this may be forbidden by the technology even if they belong to two different masks (see [3] for constraints of this type, called mutually exclusive). Although we have not considered such constraints thus far, they are easy to introduce in the naive model (but more difficult in others).

Finally, from a practical perspective, there might be relevant alternative models for the manufacturing of vias. We mentioned the industry’s interest in minimizing the number of conflicts when fixing the number of patterning steps (such conflict could then possibly be removed by slightly adjusting the layout, for instance). Another interesting option would be to consider the problem of maximizing the minimum distance between any two features within a mask when the number of patterning steps is again fixed. This would allow identifying which lithography technology is more appropriate for the corresponding design, and if no technology is feasible, again identify small adjustments in the layout that may result in a feasible solution.

6 Acknowledgment

We would like to thank François Clautiaux and Stéphane Dauzère-Peres for their very constructive comments and discussions on our work. This project has been partly supported by the Association Nationale de la Recherche et de la Technologie (Convention CIFRE 2015/0553).

References

[1] Ait-Ferhat, D. (2018). Conception de solutions exactes pour la fabrication de "vias" en utilisant la technologie DSA [Design of exact solutions for the manufacturing of ‘vias’ using DSA technology]. Doctoral Dissertation.

[2] Ait-Ferhat, D., Juliard, V., Stauffer, G., and Torres, J.A. (2018). DSA-aware multiple patterning for the manufacturing of vias: a dynamic programming approach. Technical Report.
[3] Akiyama, J., Era, H., Gervacio, S. V., and Watanabe, M. (1989). Path chromatic numbers of graphs. Journal of Graph Theory, 13(5), 571-573.

[4] Badr, Y. (2017). Co-optimization of Restrictive Patterning Technologies and Design. UCLA. ProQuest ID: Badr_ucla_0031D_10032. Merritt ID: ark:/13030/m5324r9m. Retrieved from https://escholarship.org/uc/item/6wz217k7

[5] Badr, Y., Torres, A., and Gupta, P. (2015, June). Mask assignment and synthesis of DSA-MP hybrid lithography for sub-7nm contacts/vias. In Proceedings of the 52nd Annual Design Automation Conference (p. 70). ACM.

[6] BaPCod: https://wiki.bordeaux.inria.fr/realopt/pmwiki.php/Project/BaPCod

[7] Bekaei, J., Doise, J., Gronheid, R., Ryckaert, J., Vandenberghhe, G., Fenger, G., ... and Cao, Y. (2015, July). N7 logic via patterning using templated DSA: implementation aspects. In Photomask Japan 2015: Photomask and Next-Generation Lithography Mask Technology XXII (Vol. 9658, p. 965804). International Society for Optics and Photonics.

[8] Bodlaender, H. L. (1988, July). Dynamic programming on graphs with bounded treewidth. In International Colloquium on Automata, Languages, and Programming (pp. 105-118). Springer, Berlin, Heidelberg.

[9] Camplo, M., Campos, V. A., and Corra, R. C. (2008). On the asymmetric representatives formulation for the vertex coloring problem. Discrete Applied Mathematics, 156(7), 1097-1111.

[10] Chang, L. W., Bao, X., Bencher, C., and Wong, H. S. P. (2010, December). Experimental demonstration of aperiodic patterns of directed self-assembly by block copolymer lithography for random logic circuit layout. In Electron Devices Meeting (IEDM), 2010 IEEE International (pp. 33-2). IEEE.

[11] F. Clautiaux, and R. Sadycov. Personal Communication.

[12] Fang, S.-Y., Hong, Y.-X., and Y.-Z. Lu. (2015). Simultaneous guiding template optimization and redundant via insertion for directed self-assembly. In ICCAD 15 Proceedings, pp. 410-417.

[13] Frick, M., and Bullock, F. (2001). Detour chromatic numbers. Discussiones Mathematicae Graph Theory, 21(2), 283-291.

[14] Golovach, P. A., Johnson, M., Paulusma, D., and Song, J. (2017). A survey on the computational complexity of coloring graphs with forbidden subgraphs. Journal of Graph Theory, 84(4), 331-363.

[15] Grtschel, M., Lovsz, L., and Schrijver, A. (2012). Geometric algorithms and combinatorial optimization (Vol. 2). Springer Science and Business Media.

[16] Guo, D., Zhang, H., and Wong, M. D. (2018, January). On coloring rectangular and diagonal grid graphs for multiple patterning lithography. In Proceedings of the 23rd Asia and South Pacific Design Automation Conference (pp. 387-392). IEEE Press.

[17] Hansen, P., Labb, M., and Schindl, D. (2009). Set covering and packing formulations of graph coloring: Algorithms and first polyhedral results. Discrete Optimization, 6(2), 135-147.

[18] Havet, F., Kang, R. J., and Sereni, J. S. (2009). Improper coloring of unit disk graphs. Networks: An International Journal, 54(3), 150-164.

[19] Held, S., Cook, W., and Sewell, E. C. (2012). Maximum-weight stable sets and safe lower bounds for graph coloring. Mathematical Programming Computation, 4(4), 363-381.

[20] Jabrayilov, A., and Mutzel, P. (2018, April). New Integer Linear Programming Models for the Vertex Coloring Problem. In Latin American Symposium on Theoretical Informatics (pp. 640-652). Springer, Cham.

[21] Jinjiang, Y. (1995). Computational complexity of (2, 2) path chromatic number problem. Applied Mathematics-A Journal of Chinese Universities, 10(1), 83-88.

[22] Jinjiang, Y., and Yixun, L. (1992). Some results about path chromatic numbers of graphs J. Zhengz. hou L m, 21(4), 1-8.

[23] Johns, G., and Saba, F. (1989). On the PathChromatic Number of a Graph. Annals of the New York Academy of Sciences, 576(1), 275-280.

[24] Karp, R. M. (1972). Reducibility among combinatorial problems. In Complexity of computer computations (pp. 85-103). Springer, Boston, MA.
[26] Kuang, J., Ye, J., and Young, E. F. (2018). STOMA: Simultaneous Template Optimization and Mask Assignment for Directed Self-Assembly Lithography With Multiple Patterning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 37(6), 1251-1264.

[27] Ma, Y., Torres, J. A., Fenger, G., Granik, Y., Ryckaert, J., Vanderberghe, G., ... and Word, J. (2014, October). Challenges and opportunities in applying grapho-epitaxy DSA lithography to metal cut and contact/via applications. In 30th European Mask and Lithography Conference (Vol. 9231, p. 92310T). International Society for Optics and Photonics.

[28] Ma, Y., Zeng, X., and Yu, B. (2017, October). Methodologies for layout decomposition and mask optimization: A systematic review. In Very Large Scale Integration (VLSI-SoC), 2017 IFIP/IEEE International Conference on (pp. 1-6). IEEE.

[29] Malaguti, E., Monaci, M., and Toth, P. (2011). An exact approach for the vertex coloring problem. Discrete Optimization, 8(2), 174-190.

[30] Malaguti, E., and Toth, P. (2010). A survey on vertex coloring problems. International transactions in operational research, 17(1), 1-34.

[31] I. Mndez-Daz, I., and Zabala, P. (2006). A branch-and-cut algorithm for graph coloring. Discrete Applied Mathematics, 154(5), 826-847.

[32] Mehrotra, A., and Trick, M. A. (1996). A column generation approach for graph coloring. informs Journal on Computing, 8(4), 344-354.

[33] Migura, S. (2018). Optics for EUV Lithography. 2018 EUVL Workshop, June 13th 2018 Berkeley CA. Retrieved from www.euvlitho.com/2018/P22.pdf.

[34] Mynhardt, C. M., and Broere, I. (1985, September). Generalized colorings of graphs. In Graph theory with applications to algorithms and computer science (pp. 583-594). John Wiley and Sons, Inc.

[35] Pardalos, P. M., Mavridou, T., and Xue, J. (1998). The graph coloring problem: A bibliographic survey. In Handbook of combinatorial optimization (pp. 1077-1141). Springer, Boston, MA.

[36] Peeters, R. (1991). On coloring j-unit sphere graphs. Tilburg, The Netherlands: Tilburg University.

[37] Ou, J., Yu, B., Gao, J. R., and Pan, D. Z. (2015). Directed self-assembly cut mask assignment for unidirectional design. Journal of Micro/Nanolithography, MEMS, and MOEMS, 14(3), 031211.

[38] Ou, J., Yu, B., and Pan, D. Z. (2016, April). Concurrent guiding template assignment and redundant via insertion for DSA-MP hybrid lithography. In Proceedings of the 2016 on International Symposium on Physical Design (pp. 39-46). ACM.

[39] Ruiz, R., Kang, H., Detcheverry, F. A., Dobisz, E., Kercher, D. S., Albrecht, T. R., ... and Nealey, P. F. (2008). Density multiplication and improved lithography by directed block copolymer assembly. Science, 321(5891), 936-939.

[40] Stockmeyer, L. (1973). Planar 3-colorability is polynomial complete. ACM Sigact News, 5(3), 19-25.

[41] Wei, Y., and Back, D. (2007). 193nm immersion lithography: Status and challenges. SPIE Newsroom.

[42] Xiao, Z., Du, Y., Tian, H., Wong, M. D., Yi, H., and Wong, H. S. P. (2014, March). DSA template optimization for contact layer in 1D standard cell design. In Alternative Lithographic Technologies VI (Vol. 9049, p. 904920). International Society for Optics and Photonics.

[43] Yang, Y., Luk, W. S., Zhou, H., Pan, D. Z., Zhou, D., Yan, C., and Zeng, X. (2017). An Effective Layout Decomposition Method for DSA with Multiple Patterning in Contact-Hole Generation. ACM Transactions on Design Automation of Electronic Systems (TODAES), 23(1), 11.

[44] Yu, B., Lin, Y. H., Luk-Pat, G., Ding, D., Lucas, K., and Pan, D. Z. (2013, November). A high-performance triple patterning layout decomposer with balanced density. In Proceedings of the International Conference on Computer-Aided Design (pp. 163-169). IEEE Press.