Memristors, Spintronics and 2D Materials for Future Computing Systems

D. Joksas\textsuperscript{1}, A. AlMutairi\textsuperscript{2}, O. Lee\textsuperscript{3}, M. Cubukcu\textsuperscript{3,4}, A. Lombardo\textsuperscript{3,1}, H. Kurebayashi\textsuperscript{3}, A. J. Kenyon\textsuperscript{1}, and A. Mehonic\textsuperscript{1}

\textsuperscript{1}Department of Electronic and Electrical Engineering, University College London, UK
\textsuperscript{2}Department of Engineering, University of Cambridge, UK
\textsuperscript{3}London Centre for Nanotechnology, University College London, UK
\textsuperscript{4}National Physical Laboratory, UK

Abstract

In a data-driven economy, virtually all industries benefit from advances in information technology—powerful computing systems are critically important for rapid technological progress. However, this progress might be at risk of slowing down if we do not address the discrepancy between our current computing power demands and what the existing technologies can offer. Key limitations to improving the energy efficiency are the excessive growth of data transfer costs associated with the von Neumann architecture and the fundamental limits of complementary metal–oxide–semiconductor (CMOS) technologies, such as transistors. In this perspective article, we discuss three technologies that will likely play an essential role in future computing systems: memristive electronics, spintronics, and electronics based on 2D materials. We present some representative applications for each and speculate how these could fit within future digital, quantum and neuromorphic systems.
1 Introduction

Computers have become an integral part of the modern world. Technologies from instant messaging to searches on the Internet to smart assistants are enabled by devices that perform logical operations and store information over time. With such an explosion of uses, it is not surprising that energy costs have been increasing too—some estimate that information and communications technology could constitute from 8% to 21% of the global electricity demand by the end of the decade [1]. Of course, some applications may contribute to this more than others.

Most notably, artificial intelligence (AI) and machine learning (ML) have become indispensable in a wide range of rapidly growing data-centric technologies, including the Internet of things (IoT), transport, medicine, security, and entertainment. It is now recognised that AI might have a hardware problem [2] associated with huge computational demands that are directly reflected in the energy consumption. This is not sustainable and is rapidly becoming a critical societal challenge. The soaring demand for computing power in ML vastly outpaces improvements made through Moore’s scaling or innovative architectural solutions. From 2012 to 2020, hardware performance of state-of-the-art AI has improved by a factor of 317 [3]; this is not enough to meet the growing computing demands of AI applications. The size of state-of-the-art AI models has been increasing exponentially, as have their training costs—from a few dollars in 2012 to millions of dollars in 2020 [4]. A pressing need to develop novel technologies to address this issue at the fundamental level and build efficient AI systems has recently become acute. More fundamentally, there is a great need for low-energy computing elements, including those based on different physical principles than complementary metal–oxide–semiconductor (CMOS) transistors implementing Boolean logic.

This perspective article will discuss memristors, spintronics, and 2D materials and devices, providing examples of possible applications in future computing, including digital, quantum and neuromorphic systems. We will present the main physical principles and the promise of these technologies, as well as some materials and engineering challenges that must be addressed before full adoption. This is by no means an exhaustive review and does not imply that other approaches and technologies are not going to play an important role; many alternatives will likely complement the systems we discuss here. Furthermore, the three approaches we present often overlap—at the extreme, we might even have spintronic memristors partially based on 2D materials [5].

1.1 Basic principles

1.1.1 Memristors

Memristor was formalised as a circuit element in 1971 [6]—an electrical property, called memristance, relating electric charge and magnetic flux was introduced. Memristor’s existence was motivated by the fact that this relation filled a gap in fundamental symmetries observed in circuit theory. Since late 2000s, there has been a rebirth of interest in memristors, followed by various physical implementations. The landscape of memristive technologies and the underpinning physical mechanisms is vast and still rapidly expanding [7].

Memristors, in most cases, are based on the concept of resistance switching. Resistance switching is a reversible process where a memristor changes its resistance with externally applied electrical stimuli. In most cases, resistance switching results in nonvolatile states with long retention times after the stimuli are removed—the memristive device “memorises” the resistance state. However, resistance switching can also be achieved by other types of stimuli (e.g. optical) and could lead to volatile switching, which benefits particular applications (e.g. neuronal spiking).

There exist many different memristive technologies, but most rely on similar physical principles. Three examples of such technologies—redox-based resistive random-access memory (ReRAM), phase-change memory (PCM), and magnetoresistive random-access memory (MRAM)—are shown in Figure 1(a). Memristors, including the ones mentioned, are typically implemented as simple two-terminal capacitor-like structures, where a switching layer is sandwiched between two electrodes. The resistance of the switching layer can be programmed to various resistance states with the application of voltage pulses.

Resistance switching manifests itself slightly differently in ReRAMs, PCMs, and MRAMs. In ReRAM technologies, resistance switching is based on the creation/dissolution of conductive filaments (intrinsic to the oxide layer or a result of metallic diffusion from electrodes); local nanoionic redox phenomena drive resistance switching in ReRAMs. There are different flavours of
Memristors

Figure 1: Overview of memristive devices and their potential uses in computing. (a) There exist multiple memristive technologies, including redox-based resistive random-access memory, phase-change memory and magnetoresistive random-access memory. (b) Common applications of memristive devices include embedded non-volatile memory, analog deep learning accelerators and bio-inspired systems implemented by memristor synapses and neurons.

ReRAM devices, but they can be broadly divided by the type of switching: (1) intrinsic switching that manifests itself as an intrinsic property of the switching material, and (2) extrinsic switching that is controlled by indiffusion (typically from metal electrons) and drift of metal ions extrinsic to the fabricated switching layer [8]. Alternatively, the devices may be classified by the dominant driving forces of the switching process; this would result in electrochemical metallization cells, valence change ReRAMs, and thermochemical ReRAMs [7]. In PCMs, the switching is governed by the reversible process of crystallisation and amorphisation of phase-change materials. Finally, the programmable relative spin orientation of two ferromagnetic layers is the basis of MRAM operation.

As shown in Figure 1(b), a wide range of memristor applications have been suggested, including embedded digital non-volatile memory, analogue deep learning accelerators and neuromorphic spiking systems [9]. We discuss these and other potential applications in more detail later in the text. We suggest consulting rich literature for details and descriptions of different physical mechanisms and many more types of memristive devices and technologies [7, 10, 11].

1.1.2 Spintronics

Conventional electronic systems rely on electron charges—these systems use voltage levels and currents to process information. But the electron has another intrinsic property, called “spin”, making it analogous to a tiny mag-
The core concept of spintronics is to use this degree of freedom to create functional electronic devices which cannot be achieved by conventional semiconductor technologies. Magnets can store digital information cheaply and reliably due to their excellent nonvolatile property and combining this with spin-dependent transport for efficient writing and read-out is a viable approach to making disruptive innovations in the electronic device market.

The quantum mechanical Pauli exclusion principle and the Coulomb interaction generate the so-called exchange coupling between spins, creating the magnetic orders of spin ensembles, with the order parameter of magnetization $M$. The central concept of spintronics is to store information bits in local $M$ which can be electrically written and read in an energy-efficient manner for data storage and processing [12–14]. The magnetic field $H$ is conventional way to control $M$ via the Zeeman interaction $(-M \cdot H)$, e.g. when the two vector are aligned in parallel, the free energy of the system becomes lower, hence stabilised. Magnetic moments are nonvolatile in general, meaning that when we switch off magnetic fields, the size and direction of the moments are unchanged. Why is that possible? This is due to the presence of the aforementioned exchange interaction and magnetic anisotropies.

In a ferromagnet, where the exchange interaction aligns individual moments along the same direction, flipping one of the magnetic moments against this direction requires large energy cost, thus maintaining the total moments along the favoured direction.\(^1\) The equilibrium direction of $M$ is determined by the magnetic free energy where—with zero external magnetic field—the magnetic anisotropy creates local minima as a function of angle, as shown in Fig-

\(^1\)There is an excitation state of this magnetically-ordered system (called magnons) that can be realized by tilting the moments; however, this results in a slight change of the total moments.
The energy barrier between the minima characterises the thermal stability of the moment orientation, directly relevant to the reliability for storing data in a magnetic cell. When the barrier height ($\Delta E$) is too small an accidental reversal of the magnetic moment takes place as data loss, whereas the data retention of ten years is generally guaranteed when $\Delta E/(k_B T) > 60$ in typical magnets. This mechanism is the origin of nonvolatility in magnetic materials and optimizing parameters such as $\Delta E$ (the size of magnetic anisotropy) is one of major topics in spintronic applications.

Another key ingredient for spintronic devices is that transport parameters (e.g. resistivity) can be controlled by $M$. In ferromagnets, the density of states at the Fermi level for up and down spin electrons are different due to the energy splitting by the exchange coupling (see Figure 2(b)). Magnetic tunnel junctions (MTJs) exploit this property as tunnel magnetoresistance (TMR) by having two magnetic layers with a tunnel barrier (Figure 2(b)) in which the tunnelling probability depends on the spin polarisation of electrons at the Fermi level for each electrode [15, 16]. TMR devices exhibit larger resistance changes than giant magnetoresistance (GMR) [17–19], in particular TMR devices with a MgO barrier [20, 21]. A high TMR value is critical for reliability of read-out of spintronic devices using MTJs as well as for reducing the read-out time since it realizes a faster rate of voltage changes during reading.

Normally we switch $M$ by applying $H$ greater than magnet’s anisotropy field, as shown in Figure 2(a). However, this writing method is not scalable with downsizing since $H$ produced by an electric current is proportional to the absolute value of the electric current, not current density. As a scalable magnetisation switching mechanism, the concept of spin transfer torque (STT) was proposed by Slonczewski [22] and Berger [23] independently. In this scheme (Figure 2(c)), spin-polarised currents injected into a magnetic layer can exert torques via angular momentum transfer between the conduction and localised electrons[24]. A electric current through an MTJ can switch magnetisation of one layer when the current size is sufficiently large. The size of this switching current density is directly relevant to power consumption of spintronic memories. Furthermore, it is also an important parameter for footprint (density) of spintronic arrays since each MRAM cell exploits powering from a CMOS transistor underneath and this element is so far the limiting factor of downsizing of MRAM. Since a high current requires a large CMOS transistor, a high-density MRAM can be achieved when the writing current is small. Other emerging magnetisation control mechanisms include spin-orbit torques (SOTs) and voltage-controlled magnetic anisotropy (VCMA), for which readers are invited to read [25–28] for more details.

1.1.3 2D materials

Adopting different computation variables (such as spin) and architectures (such as neuromorphic) leads to a demand for novel materials capable of supporting such technologies. In this perspective, we also explore two-dimensional layered materials, often simply referred as two-dimensional (2D) materials. We believe that 2D materials are among the most promising candidates for future computing due to large variety of properties they offer, the possibility of being easily combined into functional structures and the ease of integration with existing semiconductors and fabrication lines. 2D materials are a large class of materials consisting of stacks of individual layers held together by (typically) van der Waals forces. Each layer is formed by covalently-bonded atoms and exhibits fully-saturated surface bonds, resulting in crystals which are stable even in the form of a single layer, hence the name “2D” materials.

Figure 3(a) shows a list of the most common 2D materials grouped according to their structure. X-enes are materials consisting of a single element such as graphene and silicene, whereas X-anes and Fluoro-X-enes are their chemical derivatives, e.g. graphane refers to hydrogenated graphene and fluorographene—to fluorinated graphene. Transition metal dichalcogenides (TMDs) are a class of compounds formed by a transition metal element (M) mainly from IV, V or VI group and a chalcogen (X), with a generalized formula $MX_2$ [29]. These materials form layered structures of the form $XMX$, with the chalcogen atoms in two hexagonal planes separated by a plane of metal atoms [29]. Semimetal chalcogenides (SMCs) are similar to TMDs; they are formed by a semimetal and a chalcogen, usually occurring in $M_2X_2$ stoichiometry. MX-enes are ternary layered materials having occurring in the formula $M_{n+1}AX_n$ where $M$ is an early transition metal, $A$ is an element from group 13 or 14, $X$ is either carbon or nitrogen, and $n$ is an integer between 1 and 3. Finally, the 2D library includes insulators such as hexagonal boron nitride (hBN), an isomorph of graphene consisting of boron and nitrogen atoms.

Despite sharing a similar structure, the properties of
2D materials are very diverse—the “family” of 2D materials includes semimetals, direct and indirect bandgap semiconductors, insulators, metals, superconductors, topological and ferromagnetic insulators, as schematically illustrated in Figure 3(b). The lack of dangling bonds on the surface enables deterministic staking of different 2D materials to form heterostructure without lattice matching constrains, usually referred as van-der-Waals (vdW) heterostructures [30]. Such structures have atomically-precise control of the thicknesses of the different layers with abrupt interfaces, leading to an unprecedented flexibility in terms of combination of materials and properties available for device. Moreover, by controlling the angle between the layers, it is possible to define a Moiré superlattice, thus providing a further degree of freedom, leading to new phenomena (such as superconductivity in twisted bilayer graphene [31]) and enabling a novel approach to electronics, referred as “twistronics” [32].

With tens of materials experimentally available and over 2000 theoretically predicted [33], 2D materials represent one of the most promising material systems for future computing. From a manufacturing point of view, 2D materials also have significant advantages. Indeed, these materials are (sub)nanoscopic only in terms of thickness, whereas their lateral dimensions can be macroscopic, leading to a significant technological advantage over other nanomaterials, as they can be processed by using “conventional” semiconductor planar technology [34]. Combined with the ease of transfer them from one substrate to another, 2D materials can be easily integrated with existing technologies, particularly at the back-end of line in CMOS production lines [35]. Figure 3(c) shows the most promising devices based on 2D materials for applications in logic, neuromorphic and quantum computing.

### Figure 3: Overview of 2D materials and their applications.

(a) List of most common 2D materials. (b) The range of 2D materials electrical properties from zero bandgap semimetals such as graphene to wide band gap insulators such as hBN. (c) Devices based on 2D materials for applications in logic, neuromorphic and quantum computing.

#### 2 Digital Computing

Digital computers are the basis of our information and communication technologies. Logic gates, such as NAND or NOR, realized by digital CMOS circuits implement Boolean algebra that is used for all digital information processing. Field-effect transistors (FETs), fundamental building blocks of digital circuits, have followed Moore’s scaling law for more than 50 years. We are still managing to scale transistors; however, the scaling rate has slowed down over the last years [36]. There is a tremendous motivation to investigate post-CMOS technologies, starting from innovations in and understanding of materials and basic nanoscale devices that could be used either as digital memory or to construct logic gates. ReRAM, spintronics and 2D-based devices could all potentially offer better scaling prospects, as well as improved energy efficiency and speed.
2.1 Memory

ReRAM, PCM, MRAM devices can all be operated as binary memory with two well-defined nonvolatile memory states. Both ReRAM and MRAM devices compare favourably against currently used Flash technology, beating it in most performance metrics [37, 38]. Microcontroller units (MCUs) are the first and most attractive applications for these emerging nonvolatile memory technologies. Today’s MCUs use embedded NOR Flash that cannot be easily scaled beyond 28 nm node size; this represents a critical bottleneck, especially considering that more applications are becoming data-intensive (e.g. automotive MCU needs to operate on a significant amount of data collected by numerous sensors found in modern cars). Both ReRAM and MRAM present an attractive opportunity to replace NOR Flash in embedded memory applications offering better scaling (down to most aggressive nodes, <10nm) and faster programming/reading speeds (<5ns). Beyond embedded memory, ReRAM and MRAM are also considered as data storage, and thus as a replacement for NAND Flash. NAND Flash is scalable to most aggressive nodes; however, ReRAM and MRAM still offer better reading speed and lower energy. Another attractive potential application could replace or augment static random-access memory (SRAM) in edge AI applications [39, 40], where ReRAM/MRAM offer similar reading speeds but better scalability and energy efficiency.

In general, ReRAM—when used as nonvolatile digital memory—offers

- excellent scalability (e.g. 10 × 10 nm [41] and likely below [42]) that is highly competitive with current memory technologies, like SRAM and Flash
- large resistance ratio (>10 and much more) critical for fast sensing and reading speeds
- fast programming (typically <100 ns, although there are reports of 100 ps programming [43])
- excellent endurance (10^{12} switching cycles have been reported [44])
- small operational energy (e.g. sub pJ/bit [45])

In terms of commercialisation of ReRAM, in 2013 Panasonic released the first MCU with embedded ReRAM [46]. Many other companies are currently developing ReRAM technologies, including Rambus, 4DS, Dialog Semiconductor, Crossbar, Intrinsic Semiconductor Technologies, Weebit Nano, eMemory, and global foundries such as Taiwan Semiconductor Manufacturing Company (TSMC).

MRAM consists of an array of MTJs connected with read and write lines for its memory operation. Figure 4 displays three different types of individual MRAM cells with different writing mechanisms. In particular, the STT writing method has become ripe for industrial applications and two magnetic layers are magnetised along the perpendicular to the junction plane to minimise footprint. Non-volatility offers significant advantages in energy saving against volatile memories such as dynamic random-access memory (DRAM) which is volatile, requiring constant power to maintain their stored information as energy loss.

Major electronics companies have been focusing on MRAM development. Samsung and the partnership of Everspin and Global Foundaries announced their release of a 1 GB embedded MRAM on their 28/22 nm technology nodes [47, 48]. The write speed of their technology is orders of magnitude faster than eFlash (200 nanoseconds vs. 10s of microseconds), with comparable read speeds, providing a power advantage over eFlash in many applications. Intel announced they are embedding STT-MRAM into devices using its 22-nm FinFET process, with a bit yield rate of greater than 99.9% [49].

STT-MRAM are believed to be more suitable to embedded memory applications for industrial-grade MCUs, autonomous vehicles and various IoT devices [50]. Using its high-speed nature, STT-MRAM has been considered as an alternative of SRAM applications [51] as well as L3/L4 cache replacement, which requires high performance in terms of density, write efficiency, bandwidth, and endurance [52]. We point curious readers to more detailed review papers [53, 54] since there is an excellent summary table of STT-MRAM specs against other memory applications.

Emerging writing mechanisms of MRAM cells, such as SOT and VCMA, have been intensively studied for the next generation of MRAM [26, 50, 53, 54]. Wafer-scale SOT-MRAMs compatible with CMOS technologies have been demonstrated [55], together with fast switching demonstration (less than 400 ps) in a perpendicularly magnetised SOT-MRAM cell [56], show high-speed switching, as well as improved endurance for both standalone-memory and processing-in-memory (PIM) applications [57]. PIM refers to performing computational tasks within the memory units where the memory units within these applications need to have high endurance and fast writing/reading since data are more rapidly accessed inside [58]. Combining SOT and STT writing mechanisms
Figure 4: Schematics of different MRAM architectures. (a) Toggle-MRAM uses magnetic fields to switch magnetisation in an MTJ. (b) STT-MRAM directly passes an electric current through an MTJ to write their cells. (c) In SOT-MRAM, an electric current flows through the write line which generates magnetic torques on the layer above. Adapted from [50].

is expected to reduce the writing current down to a range of 10-100 fJ/bit [50, 59, 60].

2.2 Logic

2.2.1 Field-effect transistors based on 2D materials

Since the groundbreaking work of Geim and Novoselov that experimentally unveiled the electronic properties of graphene in 2004 [61], significant attention has been put into its use for transistors. That is due to graphene’s atomic thickness, extremely high room-temperature mobility, saturation velocity and thermal conductivity and the ambipolarity of its field effect. Because of the lack of bandgap, however, graphene field-effect transistors (GFETs) cannot be switched off. As a result, graphene exhibits a modest ON/OFF ratio of ~10, which is not suitable for transistor logic application, where current ratios in excess of $10^4$ are required [62]. Nevertheless, GFETs have been used in analog RF electronics, where switching off is not essential, achieving cut-off frequencies in excess of 400 GHz [63] and in application directly benefiting of the ambipolarity of the field effect, such as high-frequency mixers [64].

The possibility of isolating individual atomically-thin crystals demonstrated by graphene paved the way to the exploration of other 2D materials, in particular TMDs. Molybdenum and tungsten-based TMDs, such as MoS$_2$, WS$_2$ and WS$_2$, are of particular interest for future transistor logic application as they are atomically-thin semiconductors that can enable reduction of the characteristic length of FETs beyond the limit faced by silicon [65]. Scaling of body thickness by adopting ultrathin-body on insulator and fin field-effect transistor (FinFET) structures has indeed been key to reduce short-channel effects and extend Moore’s law [66]. However, the reduction of body thickness in bulk semiconductor below ~5 nm is accompanied by a rapid decrease of charge carrier mobility due to thickness variation, dangling bonds and roughness, resulting in a limit to further scaling [67]. Conversely, 2D semiconductors have thickness <1 nm (e.g. single layer MoS$_2$ ~0.65 nm) and mobility in excess of 100 cm$^2$/Vs, significantly higher than sub-5 nm silicon [65]. Moreover, in 3D semiconductor there is usually a tradeoff between bandgap and effective mass and therefore with mobility. Materials with higher bandgap normally show larger effective mass and lower mobility, imposing a compromise between performance and power consumption. This is not the case in 2D semiconductors, where the mobility is determined by phonon scattering [68], thus enabling materials combining large bandgap and high mobility. Saturation velocity also plays a very important role in ultrascaled devices, where the in-plane field is can easily exceed 1 kVcm$^{-1}$, however the data available for TMDs are somehow scattered and would require a more thorough investigation. TMDs are extremely interesting candidates for future multi-channel field-effect transistor (MCFET) to reduce the scaling length of FETs beyond the limits imposed by silicon.
2.2.2 Tunnelling field-effect transistors

One of the main figures of merit when assessing CMOS efficiency is the energy-delay product of its metal–oxide–semiconductor field-effect transistors (MOSFETs). One of the main factors governing the energy-delay product (EDP) is the subthreshold swing (SS), which is a measurement of the gate voltage required to change the drain current by a factor of ten. SS in MOSFETs, regardless of the channel material, is thermodynamically limited by the Boltzmann limit. In MOSFETs,

$$SS = k_B T \ln(10) \left( 1 + \frac{C_s}{C_{ox}} \right)$$

where $C_s$ and $C_{ox}$ are the semiconductor capacitance (or depletion layer capacitance) and the gate dielectric capacitance, respectively.

It is clear that even if $C_{ox} \gg C_s$, SS will never drop below $k_B T \ln(10)$ ($\approx 60 \text{mV/dec}$ at room temperature). Alternative to thermionic injections over an energy barrier, tunnelling field-effect transistors (TFETs) rely on band-to-band tunnelling (BTBT) which results in SS that is not limited to $60 \text{mV/dec}$. However, to achieve steep SS beyond the thermal limit, the energy window for tunnelling needs to be sharp which can only be attained with very abrupt interface. This has proven to be challenging in conventional planar homojunction TFETs because controlling the doping profile to the atomic level is extremely difficult. Bulk heterojunction TFETs, on the other hand, have been demonstrated to outperform their homojunction counterpart. Nevertheless, the fabrication of such sharp interface is still challenging.

2D materials, owing to their inherently atomically flat surfaces, are ideal for such applications as they can form a sharp interface ideal for tunnelling. Different material combinations have been explored, such as graphene/boron nitride/graphene [69], graphene/WS$_2$/graphene [70], MoS$_2$/WSe$_2$ [71], black phosphorus/SnS$_2$ [72] and SnS$_2$/WSe$_2$ [73]. More interestingly, heterostructures between a 2D materials and a 3D conventional one can bring the best of both worlds. In particular, MoS$_2$/germanium TFETs have been reported to achieve “record” SS of 3.9 mV/dec at room temperature, combined with higher current density compared to other sub-thermionic transistors [74].

2.2.3 Negative capacitance field-effect transistors

Steep SS can also be attained by modifying the gating mechanism in the MOSFET. In MOSFETs, the gate controls the channel through direct capacitive approach. Negative capacitance field-effect transistor (NCFET) utilizes ferroelectric materials (FE) that exhibits metastable spontaneous polarization which can be triggered through an external field from a low state to high state. NCFETs employ this abrupt change to switch the device from low (OFF) state to high (ON) state. However, it is important to note that an appropriate dielectric material (DE) needs to be connected in series with the FE layer to stabilize the NC state and reduce hysteresis [75, 76]. The aforementioned SS formula needs be changed to include the FE layer effect. Hence,

$$SS = k_B T \ln(10) \left( 1 + \frac{C_s}{C_{FE} + C_{ox}} \right) = k_B T \ln(10) \left( 1 - \frac{C_s}{|C_{FE} - C_{ox}|} \right)$$

where $C_{FE}$ is the capacitance of the FE layer [77].

It is clear that to achieve sub-60 mV/dec SS, $C_{ox}$ must be larger than $|C_{FE}|$ which adds another criterion for choosing the suitable dielectric. As was the case in MOSFETs, NCFETs benefits from improved gate control 2D materials exhibits duo to their thinness. Hence, SS as low as 25 mV/dec has been accomplished in MoS$_2$ NCFET with Hf$_{0.5}$Zr$_{0.5}$O$_2$ FE with low hysteresis (~28 mV) [78]. In addition, based on the industrial direction for MOSFETs, it is logical to assume that an all 2D stacked negative-conductance gate-all-around field-effect transistor (GAAFET) with its steep SS and high ON current is the way to go.

2.2.4 Memristor-based logic

There are several ways of using memristors for digital logic. For instance, memristors have been considered as programmable switches for field-programmable gate arrays (FPGAs) in the past [79, 80]. Although, currently, these switches are implemented using SRAM, memristor-based switches could lead to significantly improved energy efficiency, e.g. reducing cell area by 40% and energy-delay product by 28% [81]. Alternatively, memristors could be used to implement IMPLY$^2$ logic gates [82]. The interest comes from the fact that an IMPLY gate with the FALSE
operation\(^3\) comprises a complete logic structure. Memristive implementation of this fundamental logic element could lead to memristor-based logic circuits. More details and performance comparisons involving this approach can be found in [83].

3 Quantum Computing

Quantum computing holds potential to offer unique computational advantages (that cannot be otherwise achieved using classical computers [84–86]) by exploiting quantum-mechanical properties such as superposition, interference and entanglement. A quantum bit, or qubit, is used to store and process information in a quantum computer and unlike its counterpart in classical computers that only takes a definite binary value (0 or 1), a qubit can take any superposition of 0 and 1 prior to measurement. A quantum computer with \(n\) number of qubits can directly benefit from the superposition of \(2^n\) possible outcomes due to the large Hilbert space available, which can be an incredibly powerful approach to solving specific problems such as factorising a large number.

Making a large-scale quantum computer remains an immense challenge. DiVincenzo [87] explains the difficulty by laying the following quantum computing requirements:\(^4\):

- scalability
- initialisation
- long coherence length and fast gate operation
- universal gate set
- reliable qubit read-out

In addition to choosing appropriate materials, it is also important to establish reliable error correction protocols [89, 90].

Several physical systems have been significantly studied as qubit candidates. These include transmons in a superconducting circuit [91], isolated spins in solid states [92], trapped ions [93], single photons [94] and topological particles, such as Majorana fermions [95, 96], for different quantum computation schemes. Superconducting qubits designed for implementing quantum annealing [97] have been so far particularly successful for solving large-scale optimisation problems, by exploiting the adiabatic theorem of quantum mechanics [98]. For realising more universal quantum computing hardware suitable for a variety of different computational problems, the quest of discovering novel quantum systems that are more reliable and efficient should continue.

3.1 Quantum dots

As part of this quest to find the most promising hardware architectures for quantum computing, different type of devices with 2D materials have been explored starting with quantum dot (QD) qubits. In QD qubits, the spin states of trapped charges are exploited to perform computation.

Graphene has been predicted to be an excellent candidate for QD qubits. That is because of its electron spin g-factor being roughly 2 [99] and its weak spin orbit coupling which allows for a long spin decoherence time [100]. Moreover, while graphene-based QDs suffers from limitations due to fabrication challenges, it is possible to electrostatically define QDs in bilayer graphene (BLG) encapsulated in hBN. For instance, recently encapsulated BLG QDs, that utilize a back gate, two split gates, and two finger gates, have achieved high level of charge carrier number control (up to five charges) [101].

While graphene-based QDs have been flourishing, 2D semiconductor QDs such as the ones based on TMDs have been lagging. While being more promising due to the inherit band gap, issues arising from contact resistance and carrier mobility are limiting their application in quantum computing using QD. Material- and device-level engineering needs to be advanced before their potential is realized [102].

3.2 Josephson junctions

vdW heterostructure-based superconducting qubits, in the form of Josephson junctions (JJs), have been attracting more attention. 2D JJ utilizes a 2D insulator or semiconductor sandwich between two superconductor 2D materials, such as niobium diselenide (NbSe\(_2\)) and niobium nitride (NbN), through which supercurrent can pass. Vertically-stacked JJ has the advantage of wafer scale integrability; however, due to its structure, vertical JJ lacks tunability that gated devices offer. Alternative planar architectures with gate control have been demonstrated in magic-angle twisted BLG that was encapsulated in hBN with great level of success [103].

\(^3\)FALSE operation always yields a logical zero.
\(^4\)A similar summary was done in [88].
3.3 Single-photon emitters

2D materials, however, found their greatest success in photonic qubits in the form of single-photon emitters (SPEs). While not being physical qubits, SPEs are essential for node-to-node communication in quantum computing. To this end, capitalizing on deep defects in wide-bandgap hBN, several works were published demonstrating successful SPE in hBN [104–106].

4 Neuromorphic Computing

Neuromorphic computing mimics the structure and/or operation of the brain [107]. This paradigm aims to perform complex tasks, including recognition and classification, with little energy [108–110]. Neuromorphic implementations may involve well-established concepts like artificial neural networks (ANNs) which can be realised digitally but would benefit from more power-efficient and faster (neuromorphic) hardware. Other approaches, including spiking neural networks (SNNs) and reservoir computing, may require specialised hardware to even justify their use. Multiple emerging technologies hold promise of making neuromorphic computing a reality.

4.1 Artificial neural networks on crossbar arrays

The combination of (1) large amounts of data being processed, and (2) the nature of conventional computer architectures, is what makes ANNs so resource-intensive. Modern neural networks can often have billions of parameters [111], and von Neumann architecture, which most computers are built around, is not well suited to handle such large models. Time and energy is mostly spent not on performing computations, but on repeatedly moving data between memory and computing units [112].

Resistive crossbars may offer a solution to this problem. In these structures, resistive elements are arranged in an array, as seen in Figure 5(a). Ohm’s law achieves multiplication of voltages and conductances, while Kirchhoff’s current law achieves addition of currents. With the crossbar structure, these are combined, producing multiply-accumulate operations, or multiplication of vectors of voltage and matrices of conductance. By using pairs of devices [113], the principle can be easily extended to handle negative numbers, thus achieving in-memory multiplication of arbitrary vectors and matrices. Such crossbar are usually referred to as dot-product engines (DPEs).

Hardware acceleration of linear algebra operations is easily applicable to ML and ANNs in specific. Fully connected neural networks heavily rely on vector-matrix multiplication to compute outputs of the synaptic layers; this is demonstrated in Figure 5(b). During training, optimal weights \( W \) are determined; that is typically done using gradient descent [114]. After that, during a process called inference, only the inputs \( x \) change—with each new example, outputs \( y \) are either used for prediction directly or are passed along to the next synaptic layer. The fact that weights do not change during inference is one of the primary reasons why crossbars are an appealing candidate for their physical implementation. Inference can be accelerated by encoding weights into conductances and inputs—into voltages. The ability of DPEs to compute vector-matrix products means that, this way, the synaptic layers of ANNs can be implemented in memory, i.e. there is no need to transfer the weights during computation, only the inputs have to be applied in the form of voltage vectors.

Easily programmable resistive devices are perfect candidates for DPE implementations. Memristors are one example of such devices—one may encode matrix values into the conductances of memristors embedded in the crossbar array. Such programming can be done using voltage pulses that require very little energy [115]. Examples of such devices include Ta/HfO\(_2\) [113] and SiO\(_x\) [116] memristors. Spintronic devices can also be used to emulate synaptic behavior—MTJs can act as a local nonvolatile digital memory or as a continuously varying resistance [117–119]. For example, the conductance of a three-terminal MTJ device can be encoded by controlling the magnitude and the direction of the current flowing through the underlying heavy-metal layer [118]. Several neuromorphic proof-of-concept devices have also been realized using 2D materials. That includes atomically-thin MoS\(_2\) memristors having switching ratio >10\(^4\) and stable operation up to 50 GHz [120], memristors consisting of multilayer MoS\(_2\) encapsulated between graphene layers capable of high temperature (>300 °C) operation [121], synaptic transistors based on graphene [122], lithium-ion intercalated few-layer metal dichalcogenides and phosphorus trichalcogenides [123]. Different switching mechanisms have been

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\( ^5 \)One may also use crossbar arrays to train the ANNs, as will be explored later.
identified in 2D materials, including formation of conductive filaments [124], grain boundary migration [125], phase transition [126], oxygen migration [121], and graphene has been showed to improve the $I_{ON}/I_{OFF}$ ratio in tetrahedral amorphous carbon resistive MIMs [127].

Of course, with any of these technologies, due to the analogue nature of computations, the idealised vector-matrix computation in Figure 5(a) is often difficult to achieve. Firstly, it may be challenging to set devices to the desired values of conductances $G_{i,j}$. As an example, devices like memristors may get stuck in a certain conductance state [128] or even fail to electroform (i.e. become conductive) [129], experience random telegraph noise (RTN) [130, 131] or programming variability [132], or have their conductance state drift over time [133]. Even more difficult to tackle are nonidealities that result in deviations from the linear (with respect to conductance and/or voltage) behaviour that DPEs rely on; such nonidealities include $I$-$V$ nonlinearity [134, 135] and line resistance [136–138].

There are multiple ways of utilising DPEs for the implementation of ANNs. The most obvious one has been alluded to earlier—neural network weights may be mapped onto crossbar conductances after they have been trained on digital computers. However, it may also be possible to train ANNs directly on crossbar arrays, thus saving time, energy and even preventing unnecessary greenhouse gas emissions. That is attractive because training a large ANN on a conventional digital architecture may emit as much CO$_2$ as five cars throughout their lifetimes [139].

Ex-situ training is the most straightforward way of learning the weights of neural networks that are later implemented physically. Such ANNs can utilise a training process that is no different from the one used to train conventional networks. Training on a digital computer is the simplest approach, but it obviously has disadvantages due to the mismatch between well-behaved conventional electronic systems and crossbar arrays consisting of analog devices.

If one does not take nonidealities into account, networks trained ex situ may perform considerably worse on crossbar arrays, compared to their digital counterparts. For example, small number of achievable states, limited dynamic range, device-to-device (D2D) variability and $I$-$V$ nonlinearities may all contribute to higher error rate [140]. In addition, system-level issues, including the aforementioned line resistance [113, 141], may disturb the distribution of currents and increase the error further.

This may be partly addressed by modifying ex-situ training so that the nonidealities are considered before deploying ANNs onto DPEs. It is possible to model the behaviour of analog devices, like memristors, and adjust the expected outputs of the hardware neural network accordingly. Even for stochastic nonidealities, the nature of the stochasticity may inform the training process and make ANNs more robust. That is not unique to crossbar-based neural networks as noise can make even conventional

Figure 5: The computing principles behind crossbar-array-based dot-product engines and fully connected synaptic layers. (a) Using resistive devices in each of the vertical (bit) lines, crossbar arrays can compute dot products of voltages and conductances. When multiple of these bit lines are combined, one can compute products of voltage vectors $V$ and conductance matrices $G$. (b) Synapses in neural networks scale the incoming signals. Before nonlinear transformations, these scaled signals are added together by the postsynaptic neurons.
ANNs more robust [142].

There are multiple ways of taking nonidealities into account during training. For example, the cost function (which quantifies how close ANN outputs are to the expected ones) may be modified to incorporate the randomness associated with device behaviour [143]. Alternatively, network weights can be disturbed to represent nonidealities, like read and write noise [144]. Where the effects of nonidealities cannot be represented by injecting noise into the weights, their behaviour can be redefined to reflect, for example, \( I-V \) nonlinearities [135].

Although \textit{ex-situ} training can significantly improve the performance, it is important to consider that it relies on a number of assumptions. If the modeling of nonidealities is inaccurate, that will be reflected in the training on a digital computer and may result in deviations from intended behaviour when ANNs are implemented physically. However, this may be partly hedged against by including randomness in the modeling. Randomness may represent the uncertainty in not only the device behaviour, but also the designers’ understanding of how the devices behave. Therefore, it can improve the performance when the modelling is not perfectly accurate or even when different nonidealities manifest themselves [135].

Finally, one may employ \textit{in-situ} training which can refer to either full or partial training directly on crossbar arrays. Performing ANN training on real devices can help networks adapt to specific instantiations of nonideal behaviour—no two analogue are the same, but \textit{in-situ}, unlike \textit{ex-situ}, training can take individual variations into account without the need to model the behaviour. \textit{In-situ} approach makes networks more robust to nonidealities, like faulty devices and D2D variability [145]. One may even combine the two paradigms—conventional \textit{ex-situ} training can be used to produce ANN weights, after which \textit{in-situ} retraining is used to recover from defects, like stuck devices [146].

Unfortunately, training networks \textit{in situ} is challenging. Because conventional ML methods rely on incremental adjustments of synaptic weights, analogue devices may often be too unreliable for the task. For example, the training process can be negatively affected by the asymmetry and nonlinearity of conductance changes [145] which are both common in, for example, memristive devices. Approaches for dealing with this include adjusting the fabrication process [147, 148] and using digital electronic devices in conjunction with the analog ones [149].

4.2 Spiking neural networks

Although ANNs are loosely inspired by the brain, they are highly inefficient compared to biological systems. This is due to the fact that there are fundamental differences between the two systems. The adopted models of brain learning involve dynamic adjustment of synaptic strengths by the neuronal spiking activity. In comparison, learning in ANNs is based on gradient descent methods that adjust weights in order to optimise an objective function.

There is a significant research interest in developing SNNs as it is believed they could yield much better energy efficiency. The fundamental difference is that in SNNs, time is used directly to encode and process information—it is encoded in the time of arrival of binary events ("spikes"). Two main functional units needed for the implementation of SNNs are neurons and synapses. Neurons are typically implemented as simple leaky integrate-and-fire neurons that are capable of integrating signals over time and producing spikes when a certain threshold is reached. In terms of the synaptic functionalities, apart from adjustable strength, it is necessary to implement different local learning rules, such as spike-time-dependent plasticity, spike-rate-dependent plasticity, short-term plasticity, long-term potentiation, and long-term depression.

The energy efficiency argument relies on hopes of developing dedicated hardware platforms [150] because current von Neumann architectures are not best suited for the implementation of SNN algorithms. Although there exist many CMOS-based implementations of SNN hardware accelerators [151–160], these systems are still lacking in terms of the energy efficiency of biological counterparts. It is believed that emergent technologies will be able to directly implement critical functionalities using voltages and currents much lower than CMOS equivalents [161].

Memristive technology has been used to implement multiple elements of the SNN paradigm. Synaptic functionalities were implemented by incorporating temporal plasticity as well as particular local learning rules [162–164]. PCM memristors [165], ReRAMs [166, 167], and Mott-based memristors [168, 169] have all been used for emulating neuronal activity. For more details and a much more comprehensive overview of using memristors for SNNs, we refer readers to [161].

Spintronic devices, too, may be used for physical implementations of SNNs. The oscillatory behaviour of biological neurons can be emulated using spin-torque nano-
Figure 6: Spintronic approaches to spiking neural networks. (a) Schematic representation of p-bit computing scheme. Superparamagnetic tunnel junctions offer extremely low energy barriers that can be exploited to solve complex problems. The analogue input voltage to some junction, $I$, can cause a nonlinear response to the digital output voltages as shown in (b), and form random fluctuations analogous to ‘0’$s$ and ‘1’$s$ of a stochastic neuron at room-temperature. Adapted from [170]. (b) The control of bias voltages changes the relative energies of two states. Adapted from [171].

oscillators (STNOs) [172, 173]; the required power may be achieved when assisted by a microwatt nanosecond laser pulse [174]. When the system is configured towards the limit of super-paramagnetism, the random spiking of biological neurons can be emulated to perform population coding and probabilistic computing [171, 175]. Figure 6(a) shows a schematic of probabilistic computing with probabilistic-bits (p-bits), where the structural design of the MTJs benefits from the low-energy-barrier of the superparamagnetic tunnel junctions. The analogue input voltage, $I$, to some junction can cause a nonlinear response to the digital output voltage, $m$, (Fig 6(b)) and form random fluctuations analogous to ‘0’$s$ and ‘1’$s$ of a stochastic neuron at room temperature. Nevertheless, other systems such as memristors or nano-arrays or exploiting nonlinear dynamics in variant forms of magnetic spin textures like domain walls or skyrmions can also be engineered to facilitate such properties [176–180], demonstrating the potential of spintronic devices as artificial neuromorphic components.

4.3 Reservoir computing

In addition to the aforementioned fully connected ANNs, there also exist recurrent neural networks (RNNs). These networks contain recurrent connections and can be incredibly useful when dealing with time series data [185]. However, RNNs can suffer from vanishing and exploding gradients which makes their training especially difficult [186].

Given the challenges of RNNs, reservoir computing has been suggested as an alternative [187]. It relies on systems that exhibit rich dynamic behaviors to do the computations “for free”. Like activation functions in conventional ANNs may introduce nonlinearities, physical “reservoirs” that are complex, nonlinear, and have short-term memory properties, are able to map inputs to the nonlinear dynamics of a high-dimensional system. This enables to perform training only on the last synaptic—and usually linear—layer. The principles behind reservoir computing are visualized in Figure 7(a).

Many different kinds of memristors hold promise as potential mediums of reservoir computing. One of the factors enabling this is the fact that many memristors exhibit short-term memory properties. In the case of some memristors, repeatedly applying voltage pulses may gradually increase the response, while the absence of the pulses will make the devices decay toward their original resting state [190]. Additionally, nonlinear $I$-$V$ characteristics of memristive devices can be incredibly useful for reservoir
computing applications [188].

One may also use spintronic devices in reservoir computing applications. Figure 7(b) shows an experimental demonstration of using a single STNO facilitated with an MTJ as a reservoir. It exploited time multiplexing to emulate up to 400 neurons by tuning the state of each neurons by periodic time intervals. The relationships between the input current and the oscillation frequency can bring a nonlinear response, and the motion of spins in the free layer showed history dependence as a response to the amplitudes of analogue audio signals. Another example has been demonstrated by exploiting spinwaves in a three-dimensional space using small-sized metal electrodes to apply and detect the input and output voltages (currents) [191]. The system was configured as a stacked device consisting a thin yttrium iron garnet layer between the conductive substrate and magneto-electric coupling layer. The nonlinear effects and the history-dependent motion of the spinwaves were achieved by controlling the stability of the precession of the spins by reducing the applied bias DC magnetic field, allowing the device to satisfy the reservoir computation criteria. Yet another proposed medium for reservoir computing has been magnetic skyrmions due to their stability and controllable history-dependent nonlinear effects. In an example design by Jiang et al. (shown in Figure 7(c)), handwritten digits were converted into an input sequence of current pulses that was fed into a magnetic skyrmion memristor. The nonlinear relationship between the positions of the magnetic skyrmions allowed the system to be configured as a physical reservoir. In addition to this approach, a wide range of different systems have been proposed and investigated, including the manipulation of skyrmion fabrics, skyrmion position, and interaction of multiple skyrmions [192–194].

5 Outlook and Conclusion

Here we discuss the basics of three emerging nanoscale technologies with great potential for future computing systems. The landscape of future computing systems might get more diversified depending on particular applications. One plausible scenario includes a three-way synergy between digital, quantum and neuromorphic paradigms, each bringing benefits for specific applications. General-purpose computing will likely remain best implemented on digital systems that use Boolean logic and higher precision computing. The applications where quantum computing might provide decisive advantages include cryptography, quantum search and optimisation problems, and the scope will likely expand. Neuromorphic and analog systems that operate with lower precision and possibly utilise and/or tolerate stochasticity in data and hardware could be critical for energy-efficient AI systems. This is especially relevant for the rapidly expanding fields of IoT and edge computing.

Many systems would benefit from fast low-power memristive hardware but, at the same time, some are constrained by additional requirements. For example, memristive ANNs could in theory be used by autonomous driving companies; however, these companies often utilise...
driving data to improve their ML models and deploy the updated models continuously [195, 196]. Even if ANNs are trained ex situ and identical versions are deployed on memristive systems, each physical instantiation will be at least slightly different. This could affect not only the behaviour of individual vehicles, but also the ML pipeline, i.e. data that are collected and then used to improve the models [197] which are deployed to all cars. In general, we can identify multiple challenges of memristive systems that need to be addressed before wide-scale deployment in the real world:

- non-identical behaviour of identically designed systems [198]
- stochasticity, including possibly changing behaviour over time [199, 200]
- difficulty of reprogramming once deployed in the real world
- difficulty of identifying hardware faults [201, 202]

Where safety and behaviour reproducibility are key, special attention currently needs to be paid to the treatment of device stochasticity, variability and reliability. This is especially true when memristors are used unconventionally (i.e. not for digital nonvolatile memory, but as analogue memory and neuromorphic computational primitives). Similarly, applications where hardware needs to be constantly reconfigured (e.g. updating ML models in autonomous vehicles) would be challenging—even in controlled environments, programming memristive devices remains difficult [132, 203]. In addition, cycling endurance might need to be improved to match the endurance of volatile memory (e.g. $10^{16}$ cycles in SRAM).

We believe that memristors can be the most useful where computing needs to be fast, low-power and/or local (i.e. not in the cloud). The last possibility flows from the first two—data-intensive applications like ANNs consume a lot of power, thus the computing often takes place remotely; however, memristive technologies—due to their speed and power efficiency—can enable to perform the computations locally [204, 205]. We therefore believe that these devices are very well suited for applications like the IoT where potential violations of privacy remain a significant issue [206]. Memristive implementations of data-intensive tasks would not only eliminate the need to send data to the server, but also ensure low-power operation and high speed.

Spintronics is another promising approach that can advance the state-of-the-art in multiple paradigms of computing. Spintronic memory and logic circuits are expected to open a novel route to manipulate information more efficiently and their prototypes have been actively proposed [26, 50, 53, 54]. In the coming decade, we predict an increased dominance of hybrid CMOS-spintronic computing architectures based on MRAM techniques such as STT, SOT and VCMA. Moreover, the desired progress in speed, energy and scaling will also require the use of advanced materials such as antiferromagnets [207], 2D materials [208, 209], topological insulators [210]. Spintronic devices are also being employed in a new class of computer architecture such as all spin logic (ASL) [211] and logic-in-memory (LIM) [212]. LIM structures are hybrid in nature, combining contemporary spintronics components, such as MTJs, with current CMOS devices. Advancement in fabrication technology (e.g. 3D back-end process) enabled the growth of MTJs on the silicon layer without compromising the functionality of the circuit [213]. Circuits developed using LIM hold advantages over the conventional CMOS technologies due to their lower power dissipation, non-volatility, high density, fast reading capability, infinite endurance and 3D fabrication adaptability [214].

The properties of spintronic devices (e.g. high-speed dynamics of GHz to potentially THz ranges, nonvolatility, plasticity and nonlinearity) offer ample room for accessing numerous building blocks that can mimic the key features of biological synapses and neurons [117, 119, 176–180, 215]. In spintronic devices, the processing/transfer of information can be achieved via spin currents, spin waves, microwave signals, or magnetic spin textures such as domain walls and skyrmions. Such properties can potentially find their unique positions in the electronics market by offering a more compact and energy-efficient approaches, exploiting the spin degree of freedom.

While proof-of-concept spintronics-based neuromorphic computing implementations have been demonstrated [117, 170, 215, 216], there remain a number of key challenges. Although many creative and exciting ideas have been proposed, it is important to consider the viability of mass production and scalability when it comes to spintronics-based neuromorphic computing. Likewise, traditional algorithms used on CMOS technology require enhanced tuning to harness the maximum potential of such spintronic neuromorphic chips. Similar to von Neumann architecture for conventional computing, a dedicated architecture is a prerequisite for wide-scale implementation of neuromorphic computing [217]. Furthermore, additional research is required to increase the capability of the proposed devices.
For example, enhancing the coupling efficiency between the MTJ layers and the relatively low ratio of maximum to minimum resistance of the existing devices \[170\].

2D materials are yet another key enabler for future computing technologies. Taken individually, or in combination to form heterostructures with tailored properties, they offer an unprecedented playground for digital, neuromorphic and quantum computing. However, there are a number of challenges to overcome to realize their full potential.

The first is the doping because the ion implantation processes commonly used in semiconductor industry are not applicable to 2D materials due to their atomic-thickness \[218\]. Instead of replacing atoms in the crystal lattice (as in substitutional doping used for 3D semiconductors), doping in 2D materials is normally achieved either by physisorption or covalent bonding of impurities (chemical doping) or proximity with compounds which modifies the dielectric environment and leads to local gating effect (sometimes referred as solid-state doping) \[219\]. Unfortunately, to date, none of these methods fully satisfy the stringent requirement of ultra-scaled devices and more research effort should be devoted to identifying an industry-compatible, precise, stable and reproducible doping method.

The second challenge to overcome is related to the deposition of high-\(\kappa\) dielectrics. Indeed, the lack of dangling bonds in 2D materials’ surfaces complicates the growth of thin, uniform insulating layers by atomic layer deposition and often, “seed” layers are required to facilitate the growth. Dielectrics are not only important for the functionality of devices (e.g. as gate dielectric in MOSFETs) but also to encapsulate 2D materials, as their properties are often significantly degraded by substrate, contamination, roughness, and charged impurities. A promising alternative is represented by 2D dielectrics, which form atomically-sharp interfaces with other 2D materials. Hexagonal boron nitride (hBN) is by far the most explored 2D dielectric, which enabled experimental investigation of transport phenomena and proof-of-concept devices \[220\, 221\]. However, low dielectric constant (\(\sim 3\)) and difficulty in scalable production of multi-layer hBN limits its applicability in high-performance computing. A more promising option is represented by the possibility of oxidizing hafnium and zirconium-based multilayer TMDs to form high-\(\kappa\) dielectrics HfO\(_2\) and ZrO\(_2\) \[222\, 223\]. This approach is of particular interest as it is the equivalent to the oxidation of silicon and results in almost-perfect interfaces between the pristine semiconducting part and the oxidized surface.

The third challenge is represented by contacts. Contact resistance is usually high and cannot be reduced by ion implantation as in 3D semiconductors. Moreover, due to the Schottky junction formed when depositing metals on 2D semiconductor, contact resistance is also modified by applied gate voltage, introducing additional delays and complicating the analysis of devices \[218\]. Theoretical and experimental effort should be devoted towards this essential but often disregarded aspect of computing. Finally, scalable production of 2D materials should be optimized, in particular for what concerns reproducibility and control over defects and contaminations. Chemical vapor deposition (CVD) growth has made an impressive progress in the last ten years, however some fundamental challenges remains, such as the lack of a industrially-scalable, clean transfer of graphene. Our view is that 2D materials do not represent a replacement, but rather a complement to current bulk semiconductor technology. The relative ease of integrability of such materials into established semiconductor production lines will indeed be the key for a synergy between the two technologies and enable new, high performing computing.

Memristors, spintronics and 2D materials are rapidly developing and changing fields. New developments span materials, devices, circuit/system design and algorithmic approaches. This perspective article provides a basic introduction to central ideas, explores potential advantages over conventional CMOS technologies, and lists some pressing challenges that still need to be addressed. Memristors, spintronics and 2D-based electronics are among the most promising candidates for supporting future computing systems. There is a strong possibility they will co-exist and complement other emerging technologies and approaches, as well as conventional electronics systems.

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Conflict of Interest

A.M. and A.J.K. are co-founders of Intrinsic, a company developing memristor technology.

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