Recent achievements of the ATLAS upgrade Planar Pixel Sensors R&D project

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ABSTRACT: The ATLAS upgrade Planar Pixel Sensors (PPS) project aims to prove the suitability of silicon detectors processed with planar technology to equip all layers of the pixel vertex detector proposed for the upgrade of the ATLAS experiment for the future High Luminosity LHC at CERN (HL-LHC). The detectors need to be radiation tolerant to the extreme fluences expected to be received during the experimental lifetime, with optimised geometry for full coverage and high granularity and affordable in term of cost, due to the relatively large area of the upgraded ATLAS detector system. Here several solutions for the detector geometry and results with radiation hard technologies (n-in-n, n-in-p) are discussed.

KEYWORDS: Si microstrip and pad detectors; Particle tracking detectors; Radiation-hard detectors; Large detector systems for particle and astroparticle physics

1On behalf of the ATLAS Planar Pixel Sensors R&D Project.
1 Introduction

To extend the physics reach at the CERN Large Hadron Collider (LHC), upgrades to the accelerator are planned which will allow the ATLAS experiment to conclude a physics program integrating $\sim 3000 \text{fb}^{-1}$ of p-p interactions at 14 TeV centre of mass energy over about seven years. The machine will yield a levelled luminosity of $5 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ with up to 200 collisions per bunch crossing anticipated within the ATLAS detector. The resulting multiplicity of high energetic particles will impose severe challenges to the detector, especially to the pixel system that is the inner vertex detector located close to the beam line. The main constraints are the high granularity (small pixel size) required to keep the hit occupancy below the one per cent level (considered the limit for tracking efficiency and purity of the system) and the target radiation tolerance. The demanded radiation hardness for the pixel detector spans from about $3 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$ for the layers located further from the beam line to over $2 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ for the innermost pixels. Planar silicon pixel sensors are the baseline solution for instrumenting the vertex detector, provided that their performances are adequate to the requirements set by the experiment. This paper describes the activity of the planar pixel detector (PPS) groups to find optimised solutions for the above challenges.

2 The PPS project

The aim of the ATLAS PPS R&D project is to evaluate and improve the performance of planar pixel sensors for the final detector upgrade for the challenges mentioned. The present pixel system [1] consists of three barrel layers located at a distance of 50.5 mm, 88.5 mm and 122.5 mm from the nominal beam line. It includes 1744 modules for about 80 million readout channels. Each module is composed of a 250 $\mu$m thick planar n-in-n silicon sensors connected to 16 FE-I3 readout chips [2] by mean of solder bump bonding. The pixel unit dimensions are $50 \mu m \times 400 \mu m$. Sensor and readout chip are both qualified up to a fluence of $1 \times 10^{15}$ 1 MeV neutron equivalent ($\text{n}_{\text{eq}}$) cm$^{-2}$. The
Figure 1. Layout of the one half of the upgraded vertex and tracker ATLAS detector for the HL-LHC, with details of the pixel region.

Table 1. Main requirements for the inner, outer and barrel layer pixel detectors for the ATLAS prade at the High Luminosity LHC.

|                        | Inner barrel (two layers) | Outer barrel/disks |
|------------------------|---------------------------|--------------------|
| Sensor type and thickness | n-in-n or n-in-p, 100/150µm | n-in-p, 200/300µm |
| Pixel size             | 25 × 150µm²               | 50 × 250µm²       |
| ASIC’s thickness       | 150 µm                    | 150 µm (FE-I4 footprint) |
| TOT depth              | 0–8 bits                  | 4 bits            |
| ASIC/module            | 2 × 1, 2 × 2              | 2 × 2             |
| Data rate/module       | Up to 2 GBit/s            | 640 MBit/s        |

future system will be increased both in surface coverage and granularity (going from the current area of < 2 m² to about 10 m², and from 80 M to possibly over 600 M channels), comprising a four layer barrel and two end-cap disk regions (six disks deep), as shown in figure 1. The essential requirements for the sensors are defined in table 1.

ATLAS is currently upgrading the pixel system, for improved b-tagging capability, with the addition of a fourth innermost pixel layer at a radius of only 32 mm from the beam axis. This project is called the Insertable B-Layer (IBL) [3]. A dedicated ASIC [4] has been developed for this project, the FE-I4 which is a 2 × 1.9 cm² chip with 26880 pixels. This ASIC also satisfies the geometry and radiation tolerance requirements specified for the outer layers. This readout chip (ROC) is currently the main electronics tool used for evaluating the PPS sensors, although several studies have been performed with the legacy chip FE-I3, currently installed in the rest of the ATLAS pixel system. The results concerning the sensor performance are not depending on the particular readout ASIC employed. Table 1 indicates that n-side readout devices (n-in-n or n-in-p)
are chosen due to their superior radiation tolerance [5–7]. In particular, it shows that for the inner layers both option are possible, while for outer layers and disks the n-in-p diode configuration is preferred. The reason is that the cost for the n-in-p processing is sensibly lower (up to 40–50%) because it does not require double sided photo-lithography for sensor production. It is therefore preferred when large surfaces have to be covered. In n-in-p sensors the diode junction is on the readout (front) side, therefore the structures protecting the central sensitive active area from early breakdown (the guard-rings, GR) are on the same front side. This removes the need for placing the GRs on the back side of the pixel sensors (as opposite as for n-in-n pixel production) and the consequent more expensive double sided processing that this implies, reducing production costs and simplifying the handling and testing of the sensors. This geometry has a potential drawback when very high voltage has to be applied. The absence of GRs on the back (ohmic) size implies that a higher voltage is expected at the cut edge of the sensors (figure 2). The conductive edges bring the potential applied to the backside to the edge of the top surface. The separation of this edge from the readout ASIC bump bonded to the sensor and sitting at ground potential is only between 15–30 μm. This exposes the module to the risk of sparking discharges between these two surfaces [8]. These discharges, if happening, are potentially destructive and preventive methods should be implemented. In the n-in-n technology this problem would be mitigated (but not eliminated) by the presence of the GRs on the back side that reduces the edge potential. To prevent the discharges, three methods were investigated. The first is a 3 μm BenzoCycloButane (BCB) [9] passivation layer on the surface of the sensor. This method is applied at the end of the production process by the sensor manufacturer. Discharges are prevented up to an applied bias voltage of 1 kV [10]. Alternatively two post processing steps (therefore applicable by different vendors from the sensor manufacturer) were investigated. These approaches use silicon adhesive or Parylene-C. Both have been tested showing no discharges up to at least 1 kV [11].

The activity of the PPS groups is carried out with strong connection with silicon detector manufacturers, because non-standard design of the implant geometries offers better performances of the devices under the severe operation condition. The radiation hardness requirements impose the use of a n-side readout detector geometry and the ability to provide very high reverse bias voltage (up to 1000 V across a 200–300 μm thick sensor). A very close engineering collaboration has been established between the PPS institutes and a number of manufacturers, namely CiS [12], FBK [13], HPK [14], Micron [15], MPI-HLL [16] and VTT [17]. The sensors are designed in collaboration with the PPS institutes, also using advanced simulation method (with T-CAD simulation pack-
Figure 3. Collected charge with n-in-n CIS sensors irradiated to $2 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ compared with literature data from micro-strip sensors (left) [23]. Collected charge with pixel sensors irradiated at different fluences up to $1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ (right) [10]. In all cases the collected charge exceeds well the threshold (at bias voltages below 1 kV).

ages completed with radiation effects parameters) and their properties are tested before and after irradiation. Irradiations are performed with various particle types and energies to reproduce the realistic conditions in the experiment. Reactor neutrons (JSI) [18] and protons with different energies (26 MeV at KIT, [19], 800 MeV at LANSCE [20] and 24 GeV at CERN PS [21]) have been used. The samples were characterised in the laboratory with radioactive sources and in beam tests at CERN-SPS and DESY, using the EUDET telescope [22].

3 Status of radiation harness studies

As mentioned before, the radiation hardness of planar silicon sensors has been proven up to fluences exceeding $2 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ provided that high voltages can be applied to the segmented n-side readout sensors and that low noise electronics is used. The ability of hybrid pixel sensors to sustain high bias voltages has been briefly discussed above. In term of electronics noise, pixel sensors offer the best performance among the various hybrid segmented sensors geometries (e.g. micro-strips) in use thanks to the small size of individual readout channels. This reduces the capacitance load and the reverse current at the input of the front end amplifiers, reducing the two main contributions to the noise coming from the sensor itself, therefore making hybrid pixel the most radiation hard sensors available.

In fact, the high tolerance to hadron irradiation has been confirmed. Figure 3 shows just an example of the good signal measured after several doses up to $2 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ taken from the studies performed within the PPS community in an extensive irradiation programme involving detectors with different thicknesses (from 150 to 300 $\mu$m) and from various manufacturers [10, 23, 24].

4 Status of reduced edge distance studies

One of the aspects of geometry optimisation is the reduction of the distance between the outer edge of the active area (outer edge of the most external pixels) to the cut edge of the sensor. This distance includes the guard ring area and a bare silicon (silicon without electrically active structures) area. In current silicon detector technology this distance is just under 1 mm for silicon micro-strip detectors and 450 $\mu$m for the pixel sensors bolt for the ATLAS-IBL project. There is significant improvement
for the overall layout of the pixel modules in the various layers if the edge distance is reduced. Smaller inactive edge region would require small overlap between adjacent detectors to guarantee the full coverage of the acceptance volume of the experiment, with advantage in both reduced mass and simplicity of mechanics for the detector and layer supports. Besides, in the innermost one or two layers, the detectors can hardly be overlapped in the direction of the long side of the support (stave) and reduced edge is directly associated with reduced openings in the acceptance volume (inefficiency between neighbouring detectors). The edge reduction can be achieved in two different ways: making the edge part of the ohmic backplane contact (active edge) or passivating the edge to reduce its potential, so making the sensor more robust against voltage breakdown with a shorter distance of the active area from the cut line of the sensor (thin edge). Figure 4 shows a cartoon of these two concepts. In practice, reducing the edges aims to reduce the distance between edges and active area keeping the sensor able to sustain adequate bias voltage. A successful production of thin active edge pixel sensors has been done by VTT in collaboration with MPI [23] with the angular implantation technology. Deep Reactive Ion Etching (DRIE) is used to produce trenches around the sensor wide enough to allow doping implantation of the sensor sidewalls. P-type bulk sensors can be p-type side-implanted making the sensor walls an extension of the backplane ohmic contact. This determines an electric field in the region between the end of the pixel area and the cut edge allowing detection of ionising radiation also in this area, otherwise inactive in standard sensors. Only one guard ring is employed, therefore the edge distance can be as short as 50 µm. Sensors compatible with the ATLAS FE-I3 and FE-I4 readout chips were fabricated and tested in laboratory with radioactive sources and in beam tests, showing that the charge collection indeed extends practically to the detector edge with minimum charge losses [25].

A different method for producing active edge sensors is being tried currently by a collaboration between LPHNE Paris and FBK. The active edge is realised by etching a deep trench in correspondence with the detector edge, filled with doped polysilicon to provide the electrical continuity the detector backplane. The sensor thickness is between 200 and 300 µm and the edge distance is 100 and 200 µm.
Figure 5. Reverse current measured on a silicon detector before and after reducing the edge distance (down to 200 µm) with the SCP method [30].

In active edge, also charge generated between the outer pixels and the edge can be collected (by these corner pixels) because of a component of the electric field parallel to the surface place that drifts electrons from the edge to the active area. A relatively small distortion of the resolution is expected for the corner pixels, but the sensor can be active all the way to the edge.

Slim edges do not aim to make the area surrounding the sensitive part of the pixel sensor electrically active, but to develop methods for reducing this dead space. Three methods are being pursued by PPS groups. The first method can be used only with n-in-n sensors and exploits the fact that backplane GR are necessary with this geometry. In fact these GR can be implanted inside the projection onto the backplane, of the line that that limits the active area of the sensor (as shown in figure 2). In this way, the distance of the GR to the edge can still be the standard 450 µm but the distance of the corner pixels to the edge can be reduced (e.g. to < 150 µm). Good results are obtained with this method [26–28]. A further method is called scribe-cleave-passivate and it has been developed by SCIPP (Santa Cruz Institute for Particle Physics) in collaboration with the U.S. Naval Research laboratory [29, 30]. The sensors are scored very close to the active region (outside on of the GRs), then cleaved to obtain a very good cut on one of the crystal planes. The edge is then passivated using atom layer deposition techniques with aluminium oxide (alumina). Figure 5 shows the effectiveness of the method for achieving very good breakdown properties of sensors with reduced edge distances.

5 Status of varying pixel size studies

The floor-plan of the ROC determines the geometry of the pixel cell. The FE-I4 is designed to readout 80 columns by 336 rows of 50 × 250 µm² pixels. But, depending on the position of a given sensor on the general detector layout, the geometry determined by the floor-plan is not optimal. An example is given considering the sensors located at the end of the barrel region of figure 1, where the angle of incidence with the detector plane of the tracks coming from the interactions is very small. Figure 6 shows the response of an irradiated \(4 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}\) 150 µm thick detector
Figure 6. Response of an irradiated \((4 \times 10^{15} \text{ p}_{\text{eq}} \text{ cm}^{-2})\) 150 \(\mu\text{m}\) thick detector illuminated by relativistic pions at an angle of 85°. The seven hit pixels do not exhibit the same response, even when the path of the impinging particle in the cell has the same length.

Figure 7. Various pixel geometries compatible with bump-bonding connections to the FE-I4 readout ASIC. Some of the geometries only use a subset of the available readout connections.

illuminated at an angle of 85° (corresponding to \(\eta \sim 3.1\)). The number of hit pixels is seven (in the long side of the pixels, 250 \(\mu\text{m}\)). The charge generated deeper in the detector undergoes to higher charge trapping and contributes lower signal inducing a distortion on the resolution with irradiation (in the example of figure 6 the last hit pixels do not contribute to the signal). In such a case, a different geometry of the pixel cell, still compatible with the chosen ROC can be designed. For example the pixel could have \(25 \times 500 \mu\text{m}^2\) size, with the increased side in the \(z\)-direction does not degrade the resolution for shallow angle tracks, while the increased granularity in the other directions improves the resolution. In order to study the possibility of different pixel geometries compatible with the FE-I4, special detectors have been proposed and designed by the Liverpool group and produced in the U.K. by Micron. Figure 7 shows the cartoon of the various geometries considered. Some choice uses all the channels of the ROC, while other solutions are introduced to study the performance of larger pixel cells (bigger square pixels, very elongated pixels/stripes) using only a subset of the available channels.

The first test beam preliminary results show that one of the designs used to modify the shape of the sensitive channel with respect to the ROC \((25 \times 500 \mu\text{m}^2\)) does not introduce inefficiency
Figure 8. Comparison of the performance of a standard (50 × 250\,µm$^2$ pixel size) with a modified (25 × 500\,µm$^2$ pixel size) detectors coupled with a FE-I4 ASIC and measured in a testbeam at DESY with 6 GeV electrons. The top row shows the cluster size (number of hit pixels in a cluster) for the two geometries, which exhibits improved charge sharing in along the smaller size, while practically no difference is found along the longer direction. The middle row shows the expected residual distribution with the different geometries and the bottom row the comparison of the hit efficiency [31].

and performs as expected, namely with about half and double resolution in the perpendicular coordinates when compared with the standard pixel size. Figure 8 shows the cluster size, the residual distribution and the efficiency comparing the two different pixel shapes showing the expected performance with no loss of efficiency or degradation of resolution in the modified cell type. The sensors were characterized in a test beam at DESY with 6 GeV electrons [31].
6 Conclusions

The ATLAS Inner Tracker at the HL-LHC will require a whole new detector, with pixel sensors covering an area exceeding of about 10 m$^2$. Planar pixels are the obvious solution for most of the layers. The PPS project is making exciting progresses in the various issues posed by this extremely demanding detector, and namely qualifying the sensors in term of radiation hardness, studying the properties of the diode geometry (n- or p-type substrates) for radiation tolerance and reduced edges, studying different pixel geometries that could be used in different parts of the detector, trying solutions for more aggressively reduce the inactive peripheral areas (edges) and studying the quad detectors (sensors that cover the area of four FE-I4 ROCs) that are not mentioned here but are the most likely sensor configuration for the final layout.

References

[1] ATLAS collaboration, The ATLAS experiment at the CERN Large Hadron Collider, 2008 JINST 3 S08003.
[2] I. Peri´c et al., The FEI3 readout chip for the ATLAS pixel detector, Nucl. Instrum. Meth. A 565 (2006) 178.
[3] M. Capeans et al., ATLAS insertable B-layer technical design report, CERN-LHCC-2010-013 (2010).
[4] M. Garcia-Sciveres et al., The FE-I4 pixel readout integrated circuit, Nucl. Instrum. Meth. A 636 (2011) S155.
[5] G. Casse et al., First results on the charge collection properties of segmented detectors made with p-type bulk silicon, Nucl. Instrum. Meth. A 487 (2002) 465.
[6] G. Casse, P.P. Allport and A. Greenall, Response to minimum ionising particles of p-type substrate silicon microstrip detectors irradiated with neutrons to LHC upgrade doses, Nucl. Instrum. Meth. A 581 (2007) 318.
[7] T. Dubbs et al., Efficiency and noise measurements of non-uniformly irradiated double-sided silicon strip detectors, Nucl. Instrum. Meth. A 383 (1996) 174.
[8] T. Rohe, A. Bean, V. Radicci and J. Sibille, Planar sensors for the upgrade of the CMS pixel detector, Nucl. Instrum. Meth. A 650 (2011) 136.
[9] R. Kirchhoff, Polymers derived from poly(arylcyclobutenes), U.S. Patent 4540763 (1985).
[10] C. Gallrapp, Planar pixel sensors for the ATLAS tracker upgrade at HL-LHC, Nucl. Instrum. Meth. A 718 (2013) 323.
[11] Y. Unno et al., Development of novel n$^+$-in-p silicon planar pixel sensors for HL-LHC, Nucl. Instrum. Meth. A 699 (2013) 72.
[12] CiS Forschungsinstitut für Mikrosensorik und Photovoltaik, http://www.cismst.org.
[13] Fondazione Bruno Kessler, http://www.fbk.eu.
[14] Hamamatsu Photonics, http://www.hamamatsu.com.
[15] Micron Semiconductor, http://www.micronsemiconductor.co.uk.
[16] MAX-PLANCK-Institut Halbleiterlabor, http://www.hll.mpg.de.
[17] Valtion Tekniillisestä Tutkimuslaitoksesta, http://www.vtt.fi.
[18] L. Snoj, G. Žerovnik and A. Trkov, *Computational analysis of irradiation facilities at the JSI TRIGA reactor*, Appl. Radiat. Isotopes 70 (2012) 483.

[19] A. Dierlamm, *Untersuchung zur Strahlenhärte von Siliziumsensoren*, Ph.D. Thesis, Universität Karlsruhe, Karlsruhe Germany (2003).

[20] P. Lisowski, C.D. Bowman, G.J. Russell and S.A. Wender, *The Los Alamos National Laboratory spallation neutron sources*, Nucl. Sci. Eng. 106 (1990) 208.

[21] CERN Irradiation Facilities, https://irradiation.web.cern.ch.

[22] EUDET-JRA1 consortium, A. Bulgheroni, *Results from the EUDET telescope with high resolution planes*, Nucl. Instrum. Meth. A 623 (2010) 399.

[23] T. Wittig et al., *Radiation hardness and slim edge studies of planar n⁺-in-n ATLAS pixel sensors for HL-LHC*, talk given at PIXEL2012, Inawashiro Japan, 2–7 Sep 2012, http://indico.cern.ch/contributionDisplay.py?contribId=94&conId=137337.

[24] R. Nagai et al., *Evaluation of novel KEK/HPK n-in-p pixel sensors for ATLAS upgrade with testbeam*, Nucl. Instrum. Meth. A 699 (2013) 78.

[25] A. Macchiolo et al., *Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at HL-LHC*, Nucl. Instrum. Meth. A 731 (2013) 210 [arXiv:1210.7933].

[26] J. Weingarten et al., *Planar pixel sensors for the ATLAS upgrade: beam tests results*, 2012 JINST 7 P10028.

[27] M. Bomben et al., *Development of edgeless n-on-p planar pixel sensors for future ATLAS upgrades*, Nucl. Instrum. Meth. A 712 (2013) 41 [arXiv:1211.5229].

[28] S. Terzo et al., *Studies with irradiated thin n-in-p pixels at MPP*, talk given at the Planar Pixel Sensors Meeting, Paris France, 30 Sep 2013.

[29] M. Christophersen, V. Fadeyev, S. Ely, B.F. Phlips and H.F.-W. Sadrozinski, *The effect of different dicing methods on the leakage currents of n-type silicon diodes and strip sensors*, Solid State Electron. 81 (2013) 8.

[30] V. Fadeyev et al., *Scribe-cleave-passivate (SCP) slim edge technology for silicon sensors*, Nucl. Instrum. Meth. A 731 (2013) 260.

[31] H. Hayward et al., *Development of pixel sensors with 25 × 500 µm² pitch for the ATLAS HL-LHC upgrade*, talk given at the 9th International “Hiroshima” Symposium on the Development and Application of Semiconductor Tracking Detectors, Hiroshima Japan, 1–9 Sep 2013, https://indico.cern.ch/contributionDisplay.py?contribId=228876&conId=71.