Abstract—In this paper, we use modeling and prediction tool MuMMI (Multiple Metrics Modeling Infrastructure) and ten machine learning methods to model and predict performance and power and compare their prediction error rates. We use a fault-tolerant linear algebra code and a fault-tolerant heat distribution code to conduct our modeling and prediction study on the Cray XC40 Theta and IBM BG/Q Mira at Argonne National Laboratory and the Intel Haswell cluster Shepard at Sandia National Laboratories. Our experiment results show that the prediction error rates in performance and power using MuMMI are less than 10% for most cases. Based on the models for runtime, node power, CPU power, and memory power, we identify the most significant performance counters for potential optimization efforts associated with the application characteristics and the target architectures, and we predict theoretical outcomes of the potential optimizations. When we compare the prediction accuracy using MuMMI with that using 10 machine learning methods, we observe that MuMMI not only results in more accurate prediction in both performance and power but also presents how performance counters impact the performance and power models. This provides some insights about how to fine-tune the applications and/or systems for energy efficiency.

1. Introduction

Energy-efficient scientific applications require insight into how HPC system features impact the applications’ power and performance. This insight can result from the development of performance and power models. Dense matrix factorizations, such as LU, Cholesky, and QR, are widely used for scientific applications that require solving systems of linear equations, eigenvalues, and linear least squares problems [14] [6]. Such real-world scientific applications take a long time to execute on supercomputers, thereby relying on resilience techniques to successfully finish the long executions because of software and hardware failures. While reducing execution time is still a major objective for high-performance computing, future HPC systems and applications will have additional power and resilience requirements that represent a multidimensional tuning challenge. To embrace these key challenges, we must understand the complicated tradeoffs among runtime, power, and resilience. In this paper we explore performance and power modeling and prediction of an algorithm-based fault-tolerant linear algebra code (FTLA) [26] and a fault-tolerant heat distribution code (HDC) [25] using MuMMI (Multiple Metrics Modeling Infrastructure) [58] [59] and ten machine learning methods [32] [9].

In this work, we use FTLA and HDC to conduct our experiments on the Cray XC40 Theta [51] and IBM BG/Q Mira [40] at Argonne National Laboratory and on the Intel Haswell cluster Shepard [50] at Sandia National Laboratories. We analyze FTLA’s performance and power characteristics and use MuMMI and ten machine learning methods to model, predict and compare performance and power of FTLA and HDC. MuMMI [58] is a tool infrastructure that facilitates systematic measurement, modeling, and prediction of performance and power consumption, and performance-power tradeoffs and optimization for parallel systems. The ten machine learning methods from the R caret package [9] [32] are Random Forests [35], Gaussian Process with Radial Basis Function [31], eXtreme Gradient Boosting [12], Stochastic gradient boosting [18], Cubist [33], Ridge Regression [62], k-Nearest Neighbors [32], Support Vector Machines with Linear Kernel [31], Conditional Inference Tree [28], and Multivariate Adaptive Regression Spline [39].

Our experiment results show that the prediction error rates in performance and power using MuMMI are less than 10% for most cases. Based on the models for runtime, node power, CPU power, and memory power, we identify the most significant performance counters for potential optimization efforts associated with the application characteristics and the target architectures, and we predict theoretical outcomes of the potential optimizations. When we compare the prediction accuracy using MuMMI with that using 10 machine learning methods, we observe that MuMMI results in more accurate prediction in both performance and power.

The remainder of this paper is organized as follows. Section 2 discusses the FTLA and HDC. Section 3 briefly describes three architectures and their power profiling tools. Section 4 presents performance and power characteristics, modeling and prediction of FTLA using MuMMI. Section 5 discusses the modeling and prediction of FTLA and HDC using 10 machine learning methods and compares them with
MuMMI. Section 6 summarizes this work. Notice that we use the formula \((\text{prediction} - \text{baseline})/\text{baseline} \times 100\%\) to calculate the prediction error rate in this paper.

2. Fault-Tolerant Applications: FTLA and HDC

A number of resilience methods have been developed for preventing or mitigating failure impact. Existing resilience strategies can be broadly classified into four approaches: checkpoint based, redundancy based, proactive methods, and algorithm based. Checkpoint/restart is a long-standing fault tolerance technique to alleviate the impact of system failures, in which the applications save their state periodically, then restart from the last saved checkpoint in the event of a failure. Multilevel checkpointing is the state-of-the-art design of checkpointing, focusing on reducing checkpoint overhead to improve checkpoint efficiency. Such checkpointing libraries include FTI (Fault Tolerance Interface) \([7] [25]\), SCR (Scalable Checkpoint/Restart) \([48] [41]\), VeloC \([54]\), and diskless checkpointing \([44]\). Redundancy approaches improve resilience by replicating data or computation \([21] [22] [23]\). Proactive methods take preventive actions before failures, such as software rejuvenation and process or object migration \([42]\). Algorithm-based fault tolerance (ABFT) methods maintain consistency of the recovery data by applying appropriate mathematical operations on both the original and recovery data, and they adapt the algorithm so that the application dataset can be recovered at any moment \([30] [10] [5] [6]\). ABFT was applied to High Performance Linpack (HPL) \([13]\), to Cholesky factorization \([27]\), and to LU and QR factorizations \([14] [15] [6]\). The FTLA \([26]\) in particular was developed as an extension to ScaLAPACK \([42]\) that tolerates and recovers from fail-stop failures, which is defined as a process that completely stops responding, triggering the loss of a critical part of the global application state, and halts the application execution.

Matrix QR factorization decomposes a matrix \(A\) into a product \(A = QR\), where \(Q\) is an orthogonal matrix and \(R\) is an upper triangular matrix. The code ftla-rSC13 \([26]\) consists of two main components: one QR operation followed by a resilient QR (RQR) operation, where the RQR performs one QR, checkpointing, and repairing a failure until completing without a failure as shown in Figure 1. The structure of the block QR and LU is identical. We focus on the QR in this paper. The main loop is associated with the matrix sizes. For each matrix size, it performs one QR followed by one small loop. The small loop size is the number of error injections. For each error injection, it performs one RQR.

We remove all segments for error injections from ftla-rSC13 to create another code called \(ftla\). The main loop is associated with the matrix sizes. For each matrix size, it performs one QR followed by one RQR. The RQR performs one QR and checkpointing. Then we remove the checkpointing segments from \(ftla\) to get a code called \(la\), which is similar to ScaLAPACK QR. In this paper, we use the three codes \(ftla-rSC13\), \(ftla\), and \(la\) to conduct our experiments. They are strong scaling.

The other application used in this paper is an FTI version of MPI heat distribution benchmark code (HDC) \([25]\), which computes the heat distribution over time based on a set of initial heat sources. FTI \([7]\) leverages local storage, along with data replication and erasure codes, to provide several levels of reliability and performance. It provides four levels of checkpointing: local write (L1), Partner copy (L2), Reed-Solomon coding (L3), and PFS write (L4). The four checkpointing levels correspond to coping with the four types of failures: no hardware failure (software failure), single-node failure, multiple-node failure, and all other failures. The lower levels cannot take care of, respectively. The checkpointing file size is 2 MB per MPI process. HDC is a compute-intensive, weak scaling.

While fault tolerance methods and power-capping techniques continue to evolve, tradeoffs among execution time, power efficiency, and resilience strategies are still not well understood. Fault tolerance studies focus mainly on the tradeoffs between execution time, fault tolerance overhead, and resiliency, whereas most power management studies focus on the tradeoffs between execution time and power. Understanding the tradeoffs among all these factors is crucial because future HPC systems will be built under both reliability and power constraints. The previous work \([60]\) presented an empirical study evaluating the runtime and power requirements of multilevel checkpointing MPI applications using FTI on four different parallel architectures. Recent research has focused on a theoretical analysis of energy and runtime for fault tolerance protocols \([2] [38] [3] [19] [20] [52]\). In this paper, we use the FTLA and HDC to conduct our modeling and prediction study.

3. System Architectures and Environments

We conduct our experiments on three parallel systems with different architectures: the Cray XC40 Theta \([51]\) and IBM BG/Q Mira \([40]\) at Argonne National Laboratory and the Intel Haswell cluster Shepard \([50]\) at Sandia National Laboratories. Details about each system are given in Table 1. Each Cray XC40 node has 64 compute cores: one Intel Phi Knights Landing (KNL) 7230 with the thermal design power (TDP) of 215 W, 32 MB of L2 cache, 16 GB of
The power-sampling rate used is approximately 2 samples per second (default). On Mira, EMON API [7] provides monitoring capabilities with user access to a GPFS file system [40]. Shepard uses a Mellanox fourteen data rate InfiniBand network with a regular NFS file system [50].

Several vendor-specific power management tools exist, such as Cray’s CapMC and out-of-band and in-band power monitoring capabilities [57]. IBM EMON API on BG/Q [7], Intel RAPL [47], and NVIDIA’s power management library Intel RAPL [47], and NVIDIA’s power management library [43]. In this work, we use simplified PoLiMEr [36] to measure power consumption for the node, CPU, and memory at the node level on Theta; we use MonEQ [56] to collect power profiling data on Mira; and we use PowerInsight [58] to measure the power consumption for the node, CPU, memory, and hard disk at the node level on Shepard.

PoLiMEr uses Cray’s CapMC to obtain power and energy measurements of the node, CPU, and memory on Theta. The power-sampling rate used is approximately 2 samples per second (default). On Mira, EMON API [7] provides 7 power domains to measure the power consumption for the node, CPU, memory, and network at the node-card level. The power-sampling rate used is approximately 2 samples per second (default). Each node-card consists of 32 nodes. To obtain the power consumption at the node level, we calculate the average power by dividing by 32. So we conduct our experiments on multiple node-cards to obtain the power-profiling data. PowerInsight provides the measurement for 10 power rails for CPU, memory, disk, and motherboard on the Intel Haswell system Shepard. The power-sampling rate used is 1 sample per second (default).
Therefore, in the remainder of this section, we use the cache mode to conduct our experiments on Theta.

Figure 4 presents a performance comparison of the three codes on Theta, where ftla-1 stands for the code ftla-rSC13 with one error injection. We observe a proportional increase in application runtime with increasing numbers of error injections on up to 1,024 cores because of the proportional increase in the number of error injections.

Figure 5 shows the average node power consumption on Theta. The node power consumption decreases with increasing numbers of cores because of the strong scaling and dynamic power management support. Further, we compare power over time for the FTLA with one error injection and five error injections on 1,024 cores in Figure 6. We observe that the CPU power mainly affects the node power changes for both cases. Because of the dynamic power management on Theta, during each matrix loop the power adjusts dynamically, the power increases with the increase in the matrix size from 6,000 to 20,000. The runtime mainly results in the large energy increase.

To develop accurate models of runtime and power consumptions for the code ftla-rSC13, we use the power and performance modeling tool MuMII from our previous work [59] [58]. We collect 40 available performance counters on Theta with different system configurations (numbers of cores: 64, 128, 256, 512, and 1024) and the number of error injections (1, 2, and 3) as a training set. We then use a Spearman correlation and principal component analysis (PCA) to identify the major performance counters \( r_1, r_2, \ldots, r_n (n << 40) \), which are highly correlated with the metric: runtime, system power, CPU power, or memory power. Then we use a nonnegative multivariate regression analysis to generate our four models based on the small set of major counters and CPU frequency \( f \), as shown in Figure 7, where a numeric value is the coefficient for the counter in the corresponding model.

For the model of runtime \( T \), we develop the following equation:

\[
T = \beta_0 + \beta_1 * r_1 + \beta_2 * r_2 + \ldots + \beta_n * r_n + \beta * \frac{1}{f}. \tag{1}
\]

In this equation, \( T \) is the component predictor used to represent the value for runtime. The intercept is \( \beta_0 \); each \( \beta_n \) represents the regression coefficient for performance counter.
Figure 7. Four models for runtime, node power, CPU power, and memory power on Theta

TABLE 2. PREDICTION ERROR RATES ON THETA

| #Cores | fts-4 Runtime | fts-4 Node Power | fts-4 CPU Power | fts-4 Memory Power | fts-5 Runtime | fts-5 Node Power | fts-5 CPU Power | fts-5 Memory Power |
|--------|--------------|-----------------|---------------|------------------|--------------|-----------------|---------------|------------------|
| 64     | 0.99%        | -3.86%          | 2.51%         | 5.97%            | -0.54%       | -3.86%          | -3.86%        | -3.86%           |
| 128    | -2.21%       | 1.96%           | 0.16%         | -6.66%           | -3.21%       | -3.96%          | -2.71%        | -0.85%           |
| 256    | 0.75%        | 2.02%           | 3.13%         | -7.89%           | -1.32%       | -2.62%          | -3.07%        | -1.30%           |
| 512    | -0.49%       | -7.86%          | -1.50%        | -6.24%           | 0.74%        | -3.63%          | -6.86%        | -7.03%           |
| 1024   | -1.01%       | 2.85%           | 2.52%         | -3.86%           | -0.65%       | 8.89%           | 6.29%         | 7.74%            |

$\beta$ represents the coefficient for the CPU frequency. Equation 1 can be used to predict the runtime for the larger numbers of error injections (4 or 5 error injections).

Similarly, we can model CPU power consumption $P$ using the following equation:

$$P = \alpha_0 + \alpha_1 \times r_1 + \alpha_2 \times r_2 + \cdots + \alpha_n \times r_n + \alpha \times f^3. \quad (2)$$

In this equation, $P$ is the component predictor used to represent the value for the CPU power. The intercept is $\alpha_0$, and each $\alpha_n$ represents the regression coefficient for performance counter $r_n$, and $\alpha$ represents the coefficient for the CPU frequency. Equation 2 can be used to predict the CPU power on larger numbers of error injections. Similarly, a multivariate linear regression model is constructed for each metric (node power, memory power) of the same application.

Table 2 shows the prediction error rates for the runtime and power of the application with 4 and 5 error injections using Equations 1 and 2. Overall, the prediction error rates (absolute values) are less than 3.3% in runtime. This indicates our counter-based performance models are very accurate. The prediction error rates are less than 8.9% in node power, less than 6.3% in CPU power, and less than 7.9% in memory power. These performance and power models are generated from different system configurations and problem sizes, thus providing a broader understanding of the application’s usage of the underlying architectures. This in turn results in more knowledge about the application’s energy consumption on the given architecture.

Based on the models for runtime, node power, CPU power, and memory power, we identify the most significant performance counters for the application. Figure 8 shows the performance counter rankings of the four models using 12 different counters. We found that the L2_DCM (Level 2 data cache misses) and TLB_DM (Data translation lookaside buffer misses) contribute most in the runtime model; L2_DCM and L1_TCM (Level 1 cache misses) contribute most in the node power; TLB_DM and L1_TCM contributes most in CPU power models; and L2_STM (Level 2 store misses) contributes most in the memory power model. TLB_DM is correlated with L1_TCM. Therefore, the optimization efforts for the code should focus on the units associated with L2_DCM, TLB_DM, and L2_STM on Theta. For instance, as shown in Figure 9 we use our what-if prediction system based on the four model equations to predict the theoretical outcomes of the possible optimization by reducing L2_DCM by 30%, the other counters may be changed based on the correlation with this counter. The theoretical improvement percentage is 2.99% in runtime, 10.08% in node power, 7.44% in CPU power, and 7.10% in memory power. The default page size on Theta is 4 KB; but Theta supports several huge page sizes ranging from 2 MB to 2GB. In order to reduce the TLB miss (TLB_DM), the main kernel address space is mapped with huge pages—a single 2 MB huge page requires only a single TLB entry, while the same memory, in 4 KB pages, would need 512 TLB entries. Using the huge pages will result in the application performance improvement.

4.2. IBM Blue Gene/Q Mira

To develop accurate models for runtime and power consumptions on Mira, we collect 40 available performance counters with different system configurations (numbers of cores: 512, 1,024, 2,048, 4,096, 8,192, and 16,384) and the
number of error injections (1, 2, and 3) as a training set. We then use MuMMi to generate our four models based on the small set of major counters and CPU frequency (f), as shown in Figure 10, where a numeric value is the coefficient for the counter in the corresponding model.

Table 3 shows the prediction error rates for the runtime and power of the application with 4 and 5 error injections using Equations 1 and 2. Overall, the prediction error rates in runtime are less than 0.1%. This indicates that our counter-based performance models are accurate. The prediction error rates are less than 5% in node power and less than 8.7% in CPU power; and the error rates are less than 10% in memory power for most cases except 15.30% for f1la-4 on 2,048 cores.

Based on the models for runtime, node power, CPU power, and memory power, we identify the most significant performance counters for the application. Figure 11 shows the performance counter rankings of the four models using 9 different counters. We find that the BR_MSP (conditional branch instructions mispredicted) contributes most in the runtime model and is correlated with the counters SR_INS (Store instructions), BR_TKN (Conditional branch instructions taken), FP_INS (floating-point instructions), and RES_STL (Cycles stalled on any resource); VEC_INS (Vector/SIMD instructions (could include integer)) contributes most in the node power and CPU power models; and FML_INS (floating-point multiply instructions) contributes most in the memory power model. VEC_INS and FML_INS are not correlated with any other counters. Therefore, the optimization efforts for the code should focus on the units associated with BR_MSP, VEC_INS, and FML_INS on Mira. For instance, Mira features a quad floating-point unit that can be used to execute four-wide SIMD instructions or two-wide complex arithmetic SIMD instructions. In order to take advantage of vector instructions supported by BG/Q processors, the compiler options -qarch-qp and -qsimd=auto may be applied to compile the code to improve the energy efficiency. For instance, as shown in Figure 12, we use our what-if prediction system based on the four model equations to predict the theoretical outcomes of the possible optimization. By accelerating VEC_INS by 30%, the theoretical improvement percentage is 0.15% in runtime, 1.29% in node power, 2.49% in CPU power, and 1.79% in memory power.

### 4.3. Intel Haswell Shepard

To develop accurate models for runtime and power consumptions on Shepard, we use MuMMi to generate the four models based on the small set of major counters and CPU frequency (f), as shown in Figure 13, with the training dataset for different system configurations (numbers of cores: 32, 64, 128, 256, 512, and 1024) and the number of error injections (1, 2, and 3).

Table 4 shows the prediction error rates for the runtime and power of the application with 4 and 5 error injections using Equations 1 and 2. Overall, the prediction error rates (absolute values) are less than 0.25% for runtime. These results indicate that our counter-based performance models are accurate. The prediction error rates are less than 7.3% in node power, and less than 6.6% in CPU power; and the prediction error rates in memory power are less than 7.46% for most cases except 16.57% for f1la-4 and 12.88% for f1la-5 on 256 cores.

Based on the models for runtime, node power, CPU power, and memory power, we identify the most significant...
Figure 13. Four models for Runtime, node power, CPU power, and memory power on Shepard

TABLE 4. Prediction Error Rates on Shepard

| Cores | Flt-4 Runtime | Flt-4 Node Power | Flt-4 CPU Power | Flt-4 Memory Power | Flt-5 Runtime | Flt-5 Node Power | Flt-5 CPU Power | Flt-5 Memory Power |
|-------|---------------|-----------------|----------------|-------------------|---------------|-----------------|----------------|-------------------|
| 32    | -0.05%        | 7.25%           | 6.57%          | 7.45%             | -0.04%        | 1.44%           | 2.24%          | -0.06%            |
| 64    | 0.06%         | -3.07%          | -2.91%         | -6.05%            | 0.09%         | -4.86%          | -4.99%         | -5.72%            |
| 128   | 0.05%         | -0.48%          | -0.82%         | 0.10%             | -0.10%        | -1.71%          | -0.44%         | 0.92%             |
| 256   | 0.02%         | 2.21%           | 0.98%          | 16.57%            | 0.12%         | 3.12%           | 2.21%          | 12.88%            |
| 512   | -0.04%        | -0.27%          | -0.74%         | 6.42%             | 0.02%         | -0.71%          | -1.27%         | -1.87%            |
| 1024  | 0.19%         | -0.99%          | -2.16%         | 5.30%             | 0.24%         | -1.21%          | -1.58%         | -1.58%            |

performance counters for the application. Figure 14 shows the performance counter rankings of the four models using 13 different counters. We found that the L2_ICM (Level 2 instruction cache misses) and L1_DCM (Level 1 data cache misses) contribute most in the runtime model; L2_TCM (Level 2 cache misses) and L1_ICM (Level 1 instruction cache misses) contribute most in the node power; L2_TCM and L1_TCM contributes most in CPU power models; and L2_TCM and L1_ICM contribute most in memory power model. L2_ICM is correlated with L1_TCM, and L2_TCM is correlated with L1_ICM. Therefore, the optimization efforts for the code should focus on the units associated with L2 and L1 caches on Shepard. For instance, as shown in Figure 15 we use our what-if prediction system based on the four model equations to predict the theoretical outcomes of the possible optimization by reducing L2_TCM by 30%, the other counters may be changed based on the correlation with this counter. The theoretical improvement percentage is -0.02% in runtime, 7.02% in node power, 6.79% in CPU power, and 14% in memory power. For instance, loop optimization methods such as loop blocking and unrolling may help improve the cache locality.

5. Modeling and Prediction Using 10 Machine Learning Methods

In this section, we use 10 machine learning (ML) methods from the R caret package to model and predict performance and power of FTLa and HDC. Our methodology is as follows. First, we use the datasets for FTLa or HDC as input to split the data into the training and test datasets based on the 80/20% rule, and find out what the training and test datasets are by setting the seed 3456 of R’s random number generator set.seed() so that creating the random objects can be reproduced. Second, we apply the same training and test datasets to the 10 ML methods. Third, we use the same training and test datasets to build the performance and power models using MuMMI online. Finally, we compare the prediction error rates for these methods using violin plot from R violin package which is a combination of a box plot and a kernel density plot to visualize the distribution of the prediction error rates.

The 10 ML methods are Random Forest (RF), Gaussian Process with Radial Basis Function (GP), eXtreme Gradient Boosting (xGB), Stochastic gradient boosting (Sgb), Cubist (Cub), Ridge Regression (RR), k-Nearest Neighbors (kNN), Support Vector Machines with Linear Kernel (SVM), Conditional Inference Tree (CIT), and Multivariate Adaptive Regression Spline (MAR).

RF is short for random forests for regression or classification based on a forest of trees using random inputs, which was constructed in as a tree-based model. A random forest model achieves the variance reduction by selecting strong, complex learners that exhibit low bias. This ensemble of many independent, strong learners yields an improvement in error rates.

GP is short for Gaussian Process with Radial Basis Function, which is based on the prior assumption that adjacent observations should convey information about each other. It is assumed that the observed variables are normal, and that the coupling between them takes place by means of the covariance matrix of a normal distribution. Using the kernel matrix as the covariance matrix is a convenient
way of extending Bayesian modeling of linear estimators to nonlinear situations.

xGB is short for the eXtreme gradient boosting [12], which is an efficient implementation of the gradient boosting framework in [11]. It provides a sparsity aware algorithm for handling sparse data and a theoretically justified weighted quantile sketch for approximate learning.

Sgb is short for Stochastic gradient boosting [18], which is an implementation of extensions to AdaBoost algorithm [16] and gradient boosting machine [17]. It includes regression methods for least squares, absolute loss, t-distribution loss, quantile regression, logistic, multinomial logistic, Poisson, Cox proportional hazards partial likelihood, AdaBoost exponential loss, Huberized hinge loss, and Learning to Rank measures.

Cub is short for cubist [33] which is a regression modeling using rules with added instance-based corrections that combines the ideas in [45] and [46]. A cubist regression model is to fit for each rule based on the data subset defined by the rules. The set of rules are pruned or possibly combined, and the candidate variables for the linear regression models are the predictors that were used in the parts of the rule that were pruned away.

RR is short for Ridge Regression [62] [29], which adds a penalty on the sum of the squared regression parameters to create biased regression models. It reduces the impact of collinearity on model parameters. Combating collinearity by using biased models may result in regression models where the overall mean squared error is competitive.

kNN is short for k-Nearest Neighbors [32], which imply predicts a new sample using the k-closest samples from the training set. To predict a new sample for regression, it identifies that sample’s k-Nearest Neighbors in the predictor space. The predicted response for the new sample is then the mean of the k neighbors’ responses.

SVM is short for Support Vector Machines with Linear Kernel [31], which is the kernlab’s implementation of support vector machines [53]. It chooses a linear function in the feature space by optimizing some criterion over the sample.

CIT is short for the conditional inference tree [28], which embeds tree-structured regression models into a well defined theory of conditional inference procedures. This non-parametric class of regression trees is applicable to all kinds of regression problems, including nominal, ordinal, numeric, censored as well as multivariate response variables and arbitrary measurement scales of the covariates.

MAR is short for Multivariate Adaptive Regression Splines [39], which builds a regression model using the techniques in [24]. It is a form of regression analysis that is an extension to linear regression that captures nonlinearities and interactions between variables.

5.1. FTLA

For FTLA with the fixed problem size (matrix sizes from 6,000 to 20,000 with a stride of 2000 and a block size of 100, strong scaling), we ran the FTLA with five numbers of error injections (1, 2, 3, 4, and 5) on six different numbers of cores (32, 64, 128, 256, 512, and 1024) with five CPU frequency settings (1.2, 1.5, 1.8, 2.1 and 2.3 GHz) to collect the total 144 data samples on Shepard. Each data sample includes 53 variables such as application name, system name, number of cores, matrix sizes, stride size, block size, number of error injections, CPU frequency, 32 available performance counters, runtime, system power, CPU power, memory power, and so on. The 32 performance counters are TOT_CYC, TOT_INS, L1_TCM, L2_TCM, L3_TCM, CA_SHR, BR_CN, BR_TKN, BR_NTK, BR_MSP, CA_CLN, CA_ITV, RES_STL, L2_TCA, L1_STM, L2_TCW, L1_LDM, L2_DCA, L2_DCR, L2_DCW, L1_ICM, BR_INS, L1_DCM, L2_ICA, TLB_DM, TLB_IM, L2_DCM, L2_ICM, LD_INS, SR_INS, L2_LDM, L2_STM, then TOT_CYC is used to normalize all the performance counters. The metrics for performance and power are runtime, node power, CPU power and memory power. We split the data as training and test datasets with the 80/20% rule so that the training dataset consists of 116 samples, and the test dataset consists of 28 samples. For the fair comparison, we apply the same training and test datasets to all modeling methods.

Before we compare the prediction error rates for MuMMI with 10 ML methods, we look at MuMMI first. Figure 16 shows the prediction error rates for the models in runtime, node power, CPU power, and memory power using MuMMI. The prediction error rates are between -0.41% and 0.37% in runtime and between -6.31% and 6.06% in node power. The mean error rate is 0.03% in runtime, -0.26% in node power, 0.93% in CPU power, and 1.00% in memory power. Overall, this prediction is very accurate in runtime and power using MuMMI.

For the sake of simplicity, we use ML methods to model the performance and node power only in this paper. Figure 17 shows the performance prediction error rates using 10 ML methods and MuMMI (MuM). These violin plots visualize the distribution of the prediction error rates for each method. Based on these error rates, we observe that Cubist (Cub) and eXtreme Gradient Boosting (xGB) resulted in the lowest error rates in performance among 10 ML methods,
and for other ML methods, the maximum error rates are more than 50%. Overall, MuMMI outperformed all of them in performance prediction.

Figure 17 shows the node power prediction error rates using MuMMI and 10 ML methods. Based on these error rates, we observe that they are between -15% and 30%. Multivariate Adaptive Regression Spline (MAR), Cubist (Cub) and eXtreme Gradient Boosting (xGB) resulted in the lowest error rates in node power among 10 ML methods and outperformed MuMMI although the node power prediction error rates using MuMMI are between -6.31% and 6.06%.

For the sake of simplicity, we choose four ML methods: Cubist, eXtreme Gradient Boosting, Random Forests, and Multivariate Adaptive Regression Spline to do an in-depth analysis in performance and power modeling and prediction.

Figure 19 shows the prediction error rates for runtime and node power models using Cubist. The prediction error rates are between -33.35% and 44.38% in runtime, and between -5.71% and 2.85% in node power. The mean error rate is 0.27% in runtime and -1.32% in node power. Variable importance for boosting is a function of the reduction in squared error. Figure 20 shows the top 31 most important predictors for performance model of FTLA. We observe that the top 3 counters in performance model are TLB_DM, L2_TCW, and L2_DCA; the top 3 counters in power model are L2_TCM, L2_ICA, and L2_LDM. Overall, L2 cache and TLB mainly impact the performance and power by using Cubist, however, it is interesting to observe that the top 3 counters in performance model are in the bottom of the counter list in power model, and the top 3 counters in power model are in the bottom of the counter list in performance model.

Figure 22 shows the prediction error rates for runtime and node power models using eXtreme Gradient Boosting. The prediction error rates are between -33.35% and 44.38% in runtime, and between -5.71% and 2.85% in node power. The mean error rate is 0.27% in runtime and -1.32% in node power. Variable importance for boosting is a function of the reduction in squared error. Figure 23 shows the top 31 most important predictors for performance model of FTLA. We observe that the top 3 counters in performance model are TLB_DM, L2_TCW, and L2_DCA; the top 3 counters in power model are L2_TCM, L1_STM, and LD_INS. Overall, TLB, L2 cache and L1 cache mainly impact the performance and power by using eXtreme Gradient Boosting. Similarly, we observe that the top 3 counters...
in performance model are in the bottom of the counter list in power model, and the top 3 counters in power model are in the bottom of the counter list in performance model.

Contrasting the importance results to Cubist in Figure 20 and 21, we see that 2 of the top 5 counters are the same (L2_DCA and TLB_DM in performance model; L2_TCM and L1_STM in power model), however, the importance orderings are much different.

Figure 22 shows the prediction error rates for runtime and node power models using Random Forests. The prediction error rates are between -56.15% and 71.97% in runtime, and between -9.09% and 5.46% in node power. The mean error rate is 9.48% in runtime and -0.68% in node power. Figure 26 shows the variable importance for performance model of FTLA. Figure 27 shows the variable importance for node power model of FTLA. We observe that the top 3 counters in performance model are L2_DCA, TLB_DM, and L1_ICM; the top 3 counters in power model are L2_TCM, L1_STM, and L2_STM. Overall, L2 cache, TLB, and L1 cache mainly impact the performance and power by using Random Forests, however, it is interesting to observe that the top 3 counters in performance model are in the bottom of the counter list in power model, and the top 3 counters in power model are in the bottom of the counter list in performance model. The variable importance in random forest models is similar to that in cubist models, albeit in different order, because both are tree/rule-based models.

Figure 28 shows the prediction error rates using Multivariate Adaptive Regression Spline are between -56.15% and 71.97% in runtime, and between -9.09% and 5.46% in node power. The average error rate is 9.48% in runtime and -0.68% in node power. Figure 29 shows the variable importance with only 10 counters used in performance model of FTLA. Figure 30 shows the variable importance with only 4 counters used in node power model of FTLA. We observe
that the top 3 counters in performance model are TLB_DM, L1_ICM, and RES_STL; the top 3 counters in power model are L2_TCM, BR_CN, and BR_NTK. Overall, TLB and L2 cache mainly impact the performance and power by using Multivariate Adaptive Regression Spline.

In summary, for the four ML methods, we find that TLB_DM is one of the dominant factors in performance models, and L2_TCM is the dominant factor in power models. This validates that L2_TCM is the dominant factor in power models using MuMMI in Figure 14. Given the datasets, 10 ML models have been fit to the datasets. Since the ML methods have their own way of learning the relationship between the predictors and the target object and provide different variable importance, it is hard to identify which ML provides the robust variable importance.
5.2. HDC

For HDC with the checkpointing file size of 2MB per MPI process (weak scaling), we ran the HDC with ten different four-levels checkpointing configurations on eight distinct numbers of cores (32, 64, 128, 256, 512, 640, 960, and 1024) with the CPU frequency of 2.3 GHz to collect the total 80 data samples. Each data sample includes 54 variables such as application name, system name, number of cores, number of iterations, checkpointing file size, Level 1 checkpoint, Level 2 checkpoint, Level 3 checkpoint, Level 4 checkpoint, CPU frequency, 32 available performance counters, runtime, system power, CPU power, memory power, and so on. We split the data as training and test datasets with the 80/20% rule so that the training dataset consists of 64 samples, and the test dataset consists of 16 samples. For the fair comparison, we apply the same training and test datasets to all modeling methods.

Figure 31 shows the prediction error rates for the models in runtime, node power, CPU power, and memory power using MuMMI. The prediction error rates are between -9.07% and 3.60% in runtime and between -5.07% and 6.56% in node power. The mean error rate is -1.88% in runtime, 1.40% in node power, 1.28% in CPU power, and 1.55% in memory power. Overall, this prediction is very accurate in runtime and power using MuMMI.

Figure 32 shows the performance prediction error rates using 10 ML methods and MuMMI (MuM). Based on these error rates, we observe that eXtreme Gradient Boosting (xGB) resulted in the lowest error rates in performance models among 10 ML methods, and for other ML methods, the maximum error rates are more than 11%. Therefore, MuMMI outperformed all of them in performance prediction.

Figure 33 shows the node power prediction error rates using MuMMI and 10 ML methods. Based on these error rates, we observe that they are between -9% and 9%. k-Nearest Neighbors (kNN) and eXtreme Gradient Boosting (xGB) resulted in the lowest error rates in node power among 10 ML methods and outperformed MuMMI although the node power prediction error rates using MuMMI are between -5.07% and 6.56%.

Figure 34 shows that the prediction error rates using eXtreme Gradient Boosting are between -6.57% and 5.40% in runtime, and between -4.17% and 5.72% in node power. The mean error rate is -0.92% in runtime and 0.71% in node power. Figure 35 shows the variable importance for performance model of HDC. Figure 36 shows the variable importance for node power model of HDC. We observe that the top 3 counters in performance model are BR_INS, TLB_DM, and L2_TCW; the top 3 counters in power model are CA_ITV, L1_TCM, and L2_TCW. It is interesting to observe that the top counter BR_INS in performance model is in the bottom of the counter list in power model, and the top counter CA_ITV in power model are in the bottom of the counter list in performance model.

Figure 37 shows the prediction error rates using k-Nearest Neighbors are between -15.11% and 17.98% in runtime, and between -4.47% and 4.43% in node power. The mean error rate is -2.21% in runtime and 0.71% in node power. Figure 38 shows the variable importance for performance model of HDC. Figure 39 shows the variable importance for node power model of HDC.
importance for node power model of HDC. We observe that the top 3 counters in performance model are L2_DCR, L2_DCA, and TLB_DM; the top 3 counters in power model are TLB_IM, BR_CN, and L2_DCR. Contrasting the importance results to eXtreme Gradient Boosting in Figure 35 and 36 we see that 4 of the top 5 counters are the same in performance model and only 1 of the top 5 counters is the same in power model, and the importance orderings are much different.

6. Conclusions

In this paper, we used MuMMI and 10 ML methods to model, predict and compare the performance and power of the FTLA and HDC. Our experiment results show that the prediction error rates in performance and power using MuMMI are less than 10% for most cases. Based on the performance counters of these models, we identified the most significant performance counters for potential opti-
mization efforts associated with the application characteristics on these systems, and we used our what-if prediction system to predict the theoretical performance and power of a possible application optimization. These performance and power models were generated from different system configurations and problem sizes, thus providing a broader understanding of the application’s usage of the underlying architectures. This in turn resulted in more knowledge about the application’s energy consumption on a given architecture.

When we compare the prediction accuracy using MuMMI with that using 10 ML methods, we observe that MuMMI resulted in more accurate prediction in both performance and power. Since the 10 ML methods have their own way of learning the relationship between the predictors and the target object and provide different variable importance, it is hard to identify which ML provides the robust variable importance for potential improvements. To address the issue in our future work, we plan to utilize ensemble learning to combine several ML methods to result in more accurate models and provide the robust variable importance for the latent improvements. Performance and power modeling tools like MuMMI is able to aid in application optimizations for energy efficiency, power or energy-aware job schedulers, and system performance and power tuning. The general methodology presented in this paper can be applied to large scale scientific applications [59] and deep learning applications [61] on other parallel systems.

Acknowledgments

This work was supported in part by Laboratory Directed Research and Development (LDRD) funding from Argonne National Laboratory, provided by the Director, Office of Science, of the U.S. Department of Energy under contract DE-AC02-06CH11357, and in part by NSF grants CCF-1801856. We acknowledge Argonne Leadership Computing Facility for use of Cray XC40 Theta and BlueGene/Q Mira under the DOE INCITE project PEACES and ALCF project EE-ECFC, and Sandia National Laboratories for use of Intel Haswell Shepard testbed.

References

[1] C. Anfinson and F. Luk, A linear algebraic model of algorithm-based fault tolerance, IEEE Trans. on Computers, 37(12):1599–1604,1988.
[2] G. Aupy, A. Benoit, T. Herault, Y. Robert, and J. Dongarra, Optimal checkpointing period: Time vs Energy. In 4th International Workshop on Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems, 2013.
[3] P. Balaprakash, L. Bautista-Gomez, M. Bouguerra, S. M. Wild, F. Cappello and P. D. Hovland, Analysis of the tradeoffs between energy and run Time for multilevel checkpointing, the 5th International Workshop on Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems, 2014.
[4] L. Breiman, Random Forests, Machine Learning, 45, 532, 2001.
[5] G. Bosilca, R. Delmas, J. Dongarra, and J. Langou, Algorithm-based fault tolerance applied to high performance computing, J. Parallel Distributed Computing 69 (2009) 410–416.
[6] A. Bouteiller, T. Herault, G. Bosilca, P. Du, and J. Dongarra, Algorithm-based fault tolerance for dense matrix factorizations, multiple failures and accuracy, ACM Trans. Parallel Computing, Vol. 1, No. 2, January 2015.
[7] L. Bautista-Gomez, D. Komatitsch, N. Maruyama, S. Tsuboi, F. Cappello, and S. Matsuoka, FTI: High performance fault tolerance interface for hybrid systems, SC2011, Seattle, WA, 2011.
[8] R. Bertran, Y. Sugawara, H. Jacobson, A. Buyukkoseoglu, and P. Bose, Application-level power and performance characterization and optimization on IBM Blue Gene/Q systems, IBM Journal of Research and Development, 57(1), 2013.
[9] caret package: https://topepo.github.io/caret/index.html, https://cran.r-project.org/web/packages/caret/.
[10] Z. Chen and J. Dongarra, Algorithm-based checkpoint-free fault tolerance for parallel matrix computations on volatile resources, IPDPS’06.
[11] T. Chen and C. Guestrin, XGBoost: A Scalable Tree Boosting System, KDD’16, August 13-17, 2016.
[12] T. Chen, T. He, M. Benesty, et al., Extreme Gradient Boosting, Package “xgboost”, August 1, 2019.
[13] T. Davies, C. Karlsson, H. Liu, C. Ding, and Z. Chen, High performance linpack benchmark: A fault tolerant implementation without checkpointing, the International Conference on Supercomputing (ICS’11), 2011.
[14] P. Du, A. Bouteiller, G. Bosilca, T. Herault, J. Dongarra, Algorithm-Based Fault Tolerance for Dense Matrix Factorization, the 17th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, PPoPP 2012.
[15] P. Du, P. Luszczek, S. Tomov, J. Dongarra, Soft Error Resilient QR Factorization for Hybrid System with GPGPU, SC2011 Workshop on Latest Advances in Scalable Algorithms for Large-Scale Systems, 2011.
[16] Y. Freund and R. Schapire, Experiments with a New Boosting Algorithm, the thirteenth International Conference on Machine Learning, 1996.
[17] J. Friedman, Greedy Function Approximation: A Gradient Boosting Machine, Annals of Statistics, 29(5), 2001, 1189?1232.
[18] B. Greenwell, B. Boehmke, and J. Cunningham, Generalized Boosted Regression Models, Package “gbm”, January 14, 2019.
[19] M. el Mehdi Diouri, O. Gluck, L. Lefevre, and F. Cappello, Energy considerations in checkpointing and fault tolerance protocols, 2nd International Workshop on Fault Tolerance for HPC at eXtreme Scale (FTXS), 2012;
[20] M. el Mehdi Diouri, O. Gluck, L. Lefevre, and F. Cappello, ECOFIT: A framework to estimate energy consumption of fault tolerance protocols for HPC applications, 13th IEEE/ACM International Symp. Cluster, Cloud and Grid Computing, 2013.
[21] J. Elliott, K. Kharbas, D. Fiala, F. Mueller, K. Ferreira, and C. Engelmann, Combining partial redundancy and checkpointing for HPC, ICDCS’12, 2012.
[22] K. Ferreira, R. Riesen, P. Bridges, D. Arnold, J. Stearley, J. Laros, R. Oldfield, K. Pedretti, and R. Brightwell. Evaluating the viability of process replication reliability for exascale systems, SC2011, 2011.
[23] D. Fiala, F. Mueller, C. Engelmann, R. Riesen, K. Ferreira, and R. Brightwell, Detection and correction of silent data corruption for large-scale high performance computing, SC2012, 2012.
[24] J. H. Friedman, Multivariate Adaptive Regression Splines, The Annals of Statistics, 19(1), 1991.
[25] FTI: Fault tolerance interface, leobago.github.io/fti/.
[26] FTLA: Fault Tolerant Linear Algebra, http://icl.cs.utk.edu/fsla/software/index.html (ftla-rSC13.tgz).
[27] D. Hakkarinen and Z. Chen, Algorithmic Cholesky factorization fault recovery, the IEEE International Symposium on Parallel Distributed Processing (IPDPS’10), 2010.
[28] T. Hothorn, K. Hornik, C. Strobl, and A. Zeileis, A Laboratory for Recursive Partitioning, Package “party”, March 5, 2020.

[29] A. Hoerl, Ridge Regression: Biased Estimation for Nonorthogonal Problems, Technometrics, 12(1), 1970, 55-67.

[30] K. Huang and J. Abraham. Algorithm-based fault tolerance for matrix operations, IEEE Transactions on Computers, 33(6):518-528, 1984.

[31] A. Karatzoglou, A. Smola, and K. Hornik, kernlab – An S4 Package for Kernel Methods in R.

[32] M. Kuhn and K. Johnson, Applied Predictive Modeling, Springer, 2013.

[33] M. Kuhn, S. Weston, C. Keefer, N. Coulter, and R. Quinlan, Rule-And Instance-Based Regression Modeling, Package “Cubist”, January 10, 2020. https://topepo.github.io/Cubist.

[34] J. H. Laros III, P. Pokorny and D. DeBonis, PowerInsight — A commodity power measurement capability, International Green Computing Conference, 2013.

[35] A. Liaw and M. Wiener, Breiman and Cutler’s Random Forests for Classification and Regression, Package “randomForest”, March 25, 2018.

[36] S. Martin, D Rush, M Kappel, M Sandstedt, and J Williams. 2016. Cray XC40 Power Monitoring and Control for Knights Landing, 2016 Cray User Group Conference, 2016.

[37] E. Meneses, O. Sarood and L.V. Kale, Assessing energy efficiency of fault tolerance protocols for HPC systems, 24th IEEE Intern. Symp. on Computer Architecture and High Performance Computing, 2012.

[38] S. Milborrow, Multivariate Adaptive Regression Splines, Package “earth”, November 9, 2019.

[39] MIRA, IBM BlueGene/Q system, https://www.alcf.anl.gov/mira.

[40] A. Moody, G. Bronevetsky, K. Mohror, and B. R. de Supinski. Detailed modeling, design, and evaluation of a scalable multi-level checkpointing system, SC2010, 2010.

[41] A. Nagarajan, F. Mueller, C. Engelmann, and S. Scott. Proactive fault tolerance for HPC with Xen virtualization, ICS2006, June 2006.

[42] NVIDIA, NVML API Reference Manual, 2012.

[43] J. Plank, K. Li, and M. Puening. Diskless checkpointing, IEEE Trans. on Parallel and Distributed Systems, 9(10), 1998.

[44] R. Quinlan, Learning with continuous classes, the 5th Australian Joint Conference On Artificial Intelligence, 1992, pp. 343-348

[45] R. Quinlan, Combining instance-based and model-based learning, the Tenth International Conference on Machine Learning, 1993, pp. 236-243

[46] E. Rotem, A. Naveh, D. Rajwan, A. Ananthakrishnan, and E. Weissmann, Power-management architecture of the Intel microarchitecture code-named Sandy Bridge, IEEE Micro, 32(2), 2012.

[47] H. Zou and T. Hastie, Elastic-Net for Sparse Estimation and Sparse PCA, Package "elasticnet", August 31, 2018.

[48] VeloC: Very Low Overhead transparent multilevel Checkpoint/restart, http://www.mcs.anl.gov/project/veloc-very-low-overhead-transparent-multilevel-checkpointrestart.

[49] violin package: https://cran.r-project.org/web/packages/vioplot/index.html, https://www.data-to-viz.com/graph/violin.html.

[50] S. Wallace, V. Vishwanath, S. Coghlan, J. Tramm, Z. Lan, and M. E. Papka, Application power profiling on Blue Gene/Q, IEEE Conference on Cluster Computing, 2013.

[51] C. Williams and C. Rasmussen, Gaussian Processes for Regression, Advances in Neural Information Processing, Vol. 8, 1995. URL http://books.nips.cc/papers/files/nips08/0514.pdf.

[52] X. Wu, V. Taylor, C. Lively, H. Chang, B. Li, K. Cameron, D. Terpstra and S. Moore, MuMMI: Multiple Metrics Modeling Infrastructure (Book chapter), Tools for High Performance Computing, Springer, 2014.

[53] X. Wu, V. Taylor, J. Cook, and P. Mucci, Using performance-power modeling to improve energy efficiency of HPC applications, IEEE Computer, Vol. 49, No. 10, pp. 20-29, Oct. 2016.

[54] X. Wu, V. Taylor, and Z. Lan, Evaluating Runtime and Power Requirements of Multilevel Checkpointing MPI Applications on Four Different Parallel Architectures: An Empirical Study, 2018 Cray User Group Conference, Stockholm, Sweden, May 20-24, 2018.

[55] X. Wu, V. Taylor, J. M. Wozniak, R. Stevens, T. Brettin, and F. Xia, Performance, Energy, and Scalability Analysis and Improvement of Parallel Cancer Deep Learning CANDLE Benchmarks, the 48th International Conference on Parallel Processing, Kyoto, Japan, August 5-8, 2019.

[56] X. Wu, V. Taylor, J. M. Wozniak, R. Stevens, T. Brettin, and F. Xia, Performance, Energy, and Scalability Analysis and Improvement of Parallel Cancer Deep Learning CANDLE Benchmarks, the 48th International Conference on Parallel Processing, Kyoto, Japan, August 5-8, 2019.

[57] H. Zou and T. Hastie, Elastic-Net for Sparse Estimation and Sparse PCA, Package "elasticnet", August 31, 2018.

[58] V. Vapnik, Statistical Learning Theory, Wiley, New York, 1998.