µTiles: Efficient Intra-Process Privilege Enforcement of Memory Regions

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Abstract
With the alarming rate of security advisories and privacy concerns on connected devices, there is an urgent need for strong isolation guarantees in resource-constrained devices that demand very lightweight solutions. However, the status quo is that Unix-like operating systems do not offer privilege separation inside a process. Lack of practical fine-grained compartmentalization inside a shared address space leads to private data leakage through applications’ untrusted dependencies and compromised threads. To this end, we propose µTiles, a lightweight kernel abstraction and set of security primitives based on mutual distrust for intra-process privilege separation, memory protection, and secure multithreading. µTiles takes advantage of hardware support for virtual memory tagging (e.g., ARM memory domains) to achieve significant performance gain while eliminating various hardware limitations. Our results (based on OpenSSL, the Apache HTTP server, and LevelDB) show that µTiles is extremely lightweight (adds ≈ 10KB to kernel image) for IoT use cases. It adds negligible runtime overhead (≈ 0.5% – 3.5%) and is easy to integrate with existing applications for providing strong privilege separation.

1 Introduction

Many software attacks target sensitive content in an application’s address space, usually through remote exploits, malicious third-party libraries, or unsafe language vulnerabilities. Conventional operating systems consider processes as units of isolation. However, particularly in IoT use cases, most applications generate and analyze highly sensitive data in a single process for efficiency reasons. This leads to real threats (summarised in Table 1): (i) an application’s secret data (e.g., private keys or user passwords) can be leaked in the presence of compromised third-party libraries like OpenSSL [22]; (ii) privileged functions can be misused to access private content [21]; (iii) applications written in memory-safe languages such as Rust or OCaml are vulnerable via unsafe external libraries that jeopardizes all other safety guarantees [6,33]; and (iv) in multithreaded servers attackers can exploit vulnerabilities (e.g., buffer overflows) so the compromised thread can access sensitive data owned by other threads [2]. This whole class of attacks could be avoided by providing a practical way to enforce the least privilege within a shared address space.

Process-based isolation is the primary compartmentalization technique for security-sensitive applications such as OpenSSH to separate their components into different
Table 1: A representative selection of vulnerabilities that cause sensitive content leakage. The attacks with a tick can be mitigated by using \( \mu \text{Tiles} \) protection.

| CVE          | Description            | \( \mu \text{Tiles} \) |
|--------------|------------------------|------------------------|
| CVE-2019-9345 | Shared mapping bug     | ✓                      |
| CVE-2019-9423 | missing bounds check   | ✓                      |
| CVE-2019-15295| unsafe third party library | ✓                  |
| CVE-2019-1278 | unsafe third party library | ✓                  |
| CVE-2018-0487 | unsafe third party library | ✓                  |
| CVE-2017-1000376| unsafe native bindings | ✓                      |
| CVE-2014-0160 | Heartbleed bug         | ✓                      |
| CVE-2018-0497 | SW side-channels       | ✓                      |
| CVE-2017-5754 | HW side-channels       | ✓                      |

In this paper, we present \( \mu \text{Tiles} \), a new OS abstraction for enforcing least privilege between threads and on slabs of memory within the same address space. Unlike previous work, \( \mu \text{Tiles} \) security model allows each thread to selectively protect or share its memory compartments both from the untrusted code within itself as well as from any untrusted thread (see Figure 1). \( \mu \text{Tiles} \) access control layer maps threads’ security policies to \( \mu \text{Tiles} \) dedicated virtual memory (VM) abstraction. This VM manager provides an efficient memory tagging layer by bypassing most of the kernel’s paging abstraction. It utilizes hardware-enforced VMA tagging (e.g., ARM memory domains [11] or Intel MPK [29]) to achieve low overhead. It should be noted that these hardware features have various security and practicality limitations (§2) that are mitigated by \( \mu \text{Tiles} \) high-level abstraction. Our contributions can be summarised as follows:

- present a new kernel’s security primitives based on mutual-distrust for intra-process privilege separation. It provides strong protection of private content, a secure multithreading model, and guarded communication within a shared address space.
- describe how to utilize modern CPU facilities for efficient memory tagging to avoid the overhead of existing solutions (due to TLB flushes, per-thread page tables, or nested page table management) while relieving the hardware limitations.
- show that the solution is ultra-lightweight (≈ 5K LoC) to be practical for embedded devices with a minimal memory footprint.
- evaluate our implementation using real-world software such as Apache HTTP server, OpenSSL, and Google’s LevelDB, which shows \( \mu \text{Tiles} \) add negligible runtime overhead for lightly modified applications while significantly improve their security by strong compartmentalization.

The remainder of this paper elaborates on the hardware features we use (§2), describes the architecture (§3) and implementation of \( \mu \text{Tiles} \) (§4), presents an evaluation (§5) and finally the trade-offs of our approach (§6).
2 Goals & Assumptions

The µTiles abstraction aims to enforce thread-granularity least privilege for memory accesses via the following principles and assumptions on the underlying hardware.

2.1 Design Principles

Fine-grained strong isolation: All threads of execution should be able to define their security policies and trust models to selectively protect their sensitive resources. Current OS security models of sharing (“everything-or-nothing”) are not flexible enough for defining fine-grained trust boundaries within processes or threads (lightweight processes).

Performance: µTiles operations, including lunching, running, changing access permissions, and sharing across threads, should have minimal overhead. Moreover, untrusted (i.e., µTiles-independent) parts of applications should not suffer any overhead.

Efficiency: µTiles should be lightweight to be practical for embedded devices running on a few megabytes of memory and slow ARM CPUs.

Compatibility: It is difficult to provide strong security guarantees with no code modifications, and µTiles is no exception. We move most of these modifications into the Linux kernel (increasingly popular for embedded deployments [5]) and provide simple userspace interfaces. µTiles should be implemented without extensive changes to the Linux and not depend on a specific programming language, so existing applications can be ported easily.

To achieve effective isolation, we need a security model based on mutual-distrust that lets each thread protect its own µTiles from untrusted parts of the same thread as well as other threads and processes. Simply providing POSIX memory management within µTiles (e.g. malloc or mprotect) is inadequate. As a simple example, attackers can misuse the API for changing the memory layout of other threads’ µTiles or unauthorized memory accesses. The µTiles interface needs (i) to provide isolation within a single thread; (ii) to be flexible for sharing between threads, and (iii) to restrict all unauthorized permission changes or memory mappings modification of allocated µTiles. Previous work such as ERIM [47] or libMPK [40] does not offer such security guarantees since their focus is more on performance and virtualization of the hardware protection keys.

We derive inspiration from Decentralised Information Flow Control (DIFC) [32] but with a more constrained interface – by not supporting information flow within a program, we avoid the complexities and performance overheads that typically involves. Existing DIFC kernels such as HiStar [51] achieve our isolation goals, but requires a non-POSIX-based OS that makes it impractical for many applications, particularly IoT use cases. To have a practical and lightweight solution, we therefore built µTiles by modifying the Linux kernel and additionally utilizing modern hardware facilities for VMA tagging to deliver low overhead.

2.2 HW-enforced VMA Tagging

Modern CPUs have supported memory protection mechanisms that are more efficient than traditional paging. For example, VMA tagging features such as Intel Memory Protection Keys [29] and ARMv7 Memory Domains (MDs) [11] provide fast isolation by reducing page table walks and TLB flushes. Though the implementations across Intel and ARM vary considerably (see Table 3), µTiles high-level VM abstraction can securely utilize these efficient building blocks while hiding their limitations. In this paper, we primarily describe the design of µTiles for ARMv7-A that is a widely used CPU in IoT and mobile devices. Also, ARM-MD is a less flexible and more challenging interface to support (§2.3) that covers most MPK limitations as well.

As a summary of ARMv7-A memory management, page table entries consist of a virtual base address, a physical base address, Address Space Identifier (ASID) tags, domain IDs, and a set of flags for access control and other page attributes. It supports a two-level hierarchical page table when using a short-descriptor translation table format, and supports variable page sizes (1GB, 1MB, 64KB, and 4KB). ARM supports two page tables simultaneously, using the hardware registers TTBR0 and TTBR1. A virtual address is mapped to a physical address by the CPU, depending on settings in TTBRC. This control register has a field that sets a split point in the address space. Addresses below the cutoff value are mapped through the page tables pointed to by TTBR0 (used per process), and addresses above the cutoff value are mapped through TTBR1 (used by the kernel).

The translation tables hold a four-bits domain ID ranging from D0 to D15. Access control for each domain is handled by setting a domain access control register (DACR) in CP15, which is a 32-bit register only accessible in the privileged processor modes. Each domain is assigned two bits in DACR, which defines its access rights.

The four possible access rights for a domain are No Access, Manager, Client, and Reserved (see Table 4). Those fields let the processor (i) prohibit access to the domain mapped memory–No Access; (ii) allow unlimited ac-
Table 3: ARM memory domains vs Intel MPK: Despite being efficient building blocks of isolation, such features have various limitations that µTiles abstraction resolves to provide effective intra-process privilege separation.

| Feature                  | ARM Memory Domains | Intel MPK          |
|--------------------------|--------------------|--------------------|
| Per process domains      | 16                 | 16                 |
| Access control register  | DACR (2 bits per domain, privileged register) | PKRU (2 bits per domain, userspace register) |
| Access rights            | No-access, Full access, MMU default | No-access, write-disable, MMU default |
| Paging modes             | 2-level paging (bits 8:5, level 1 entries) | 4-level paging (bits 62:59 of PDPTE) |
| Address space privilege  | Privileged & userspace | Userspace only     |
| Specific page fault      | Domain fault       | PK fault           |
| Kernel virtual memory API| No support         | Limited support (pkey_mprotect, pkey_alloc, pkey_free, and mmap) |

Table 4: ARM memory domains access permissions

| Mode        | Bits | Description                                      |
|-------------|------|--------------------------------------------------|
| No Access   | 00   | Any access causes a domain fault.                |
| Manager     | 11   | Full accesses with no permissions check.         |
| Client      | 01   | Accesses are checked against the page tables     |
| Reserved    | 10   | Unknown behaviour                                |

though the DACR is only accessible in privileged mode, any syscall that changes this register is a potential breach that could cause the attacker to gain full control. Also, since only 16 domains are supported, it is trivial to guess other domains’ identifiers, making it essential to not expose these directly to application code.

3 µTiles

We now describe µTiles architecture, which is a kernel abstraction for intra-process privilege separation with an emphasis on strong isolation, performance, and practicality for IoT use cases. µTiles abstraction contains three primary kernel’s components for (1) access control and least privilege enforcement, (2) threading and task management, (3) and dedicated virtual memory manager.

3.1 Threat Model

This paper focuses on two types of threats. First, memory-corruption based threats inside a shared address space that lead to sensitive information leakage; these threats can be caused by bugs or malicious third-party libraries (see Table 1). Second, attacks from threads that could get compromised by exploiting logical bugs or vulnerabilities (e.g., buffer overflow attacks, code injection, or ROP attacks). We assume the attacker can control a thread in a vulnerable multithreaded application, allocate memory, and spawn more threads up to resource limits by the OS and hardware. The attacker will try to escalate privileges through the attacker-controlled threads or gain control of another thread, e.g., by manipulating another thread’s data or via code injection. The adversary may also bypass protection regions by exploiting race conditions between threads or by leveraging confused-deputy attacks. µTiles thus provides isolation in two stages: (1) within a

1An occasion that has happened once already through the misuse of the put_user/get_user kernel API (CVE-2013-6282)
single thread (through utile_lock/unlock calls), and (2) across threads in the same process. We consider threads to be security principals that define their security policies based on mutual-distrust within the shared address space. We protect each thread’s µTiles against unauthorized, accidental, and malicious access or disclosure. Therefore, the TCB consists of the OS kernel, which performs security policy enforcement. It also assumes developers correctly specify their policies through the userspace interface for managing µTiles.

µTiles are not protected against covert channels based on shared hardware resources (e.g., a cache). Systems such as Nickel [45] or hardware-assisted platforms such as Hyperflow [24] could be a helpful future addition for side-channel protection on µTiles.

3.2 Access Control Mechanism

Our modified Linux kernel enforces the principle of least privilege via a dynamic security policy based on DIFC [49,51] and a simpler version of the Flume [32] labeling with only two kernel objects that are thread and address space. Any thread \( t \) has one secrecy \( SL_t \) and integrity label \( IL_t \) that each is set of unique tags. µTile objects (e.g., contiguous units of memory) have only one secrecy label instead of both types. The integrity violations are restricted in the higher-level by controlling the flow of threads labels; this improves performance and reduces complexity.

Privileges are represented in forms of two capabilities \( \theta^+ \) and \( \theta^- \) per tag \( \theta \) for adding or removing tags to/from labels. These capabilities are stored in a capability list \( C_p \) per thread \( p \). Unique tags are assigned internally by the kernel by calling utile_create. For improving security, none of µTiles API propagates tags in the userspace; all APIs access control is done internally within the kernel. The kernel allows secrecy information flow from \( \alpha \) to \( \beta \) only if \( SL_\alpha \subseteq SL_\beta \), and integrity flow if \( IL_\beta \subseteq IL_\alpha \). Every thread \( p \) may change its label from \( L_i \) to \( L_j \) if it has the capability to add tags present in \( L_j \) but not in \( L_i \), and can drop the tags that are in \( L_i \) but not in \( L_j \). This is formally declared as \( (L_j - L_i \subseteq C_p^+) \lor (L_i - L_j \subseteq C_p^-) \).

When a thread has \( \theta^+ \) capability for µTile \( \theta \), it gains the privilege to only access µTile \( \theta \) with only the permission set by its owner (read/write/execute). The access privileges to each µTile can be different; hence, two threads can share a µTile, but the access privileges can differ. Having a \( \theta^- \) capability lets a thread to declassify µTile \( \theta \). The declassification allows the thread to modify the µTile memory layout (by adding/removing pages to it), changing permissions, or copying the content to untrusted sources. Unsafe operations like declassifying µTiles or by endorsing a µTile as high-integrity require the thread to be an owner or an authority (acts-for relationship); which can be managed by utile_grant and utile_revoke calls (see Table 5).

| syscall                  | Description                              |
|--------------------------|------------------------------------------|
| utile_transfer_caps      | passing only plus capabilities to thread  |
| utile_declassify          | thread declassification or endorsement   |
| utile_grant              | make an acts-for or a delegation link to another thread |
| utile_revoke_grant       | removes an acts-for or a delegation link  |
| utile_lock               | enables access to locked µTiles          |
| utile_unlock             | disables access to locked µTiles          |
| utile_clone              | creates a thread                         |

Table 5: µTiles access control system calls. \( tid \) represents a thread ID, struct u_info is the owner list of µTiles IDs and other fields for ownership management and capabilities per µTile. There is no direct propagation of labels that are security-critical data structures, and security policies are enforced within the kernel.

3.3 µTiles Threads

Each thread may have multiple µTiles attached to it. There is no concept of inheriting credentials and capabilities by default (e.g., in the style of fork) as this makes reasoning about security difficult [13]. For a µTile to propagate, it must be through transferring capabilities; this can be done directly by calling utile_transfer_caps for “plus” capabilities and utile_grant for declassification or endorsement. Both these operations are also possible via specific arguments of utile_clone syscall when creating a child thread. Figure 2 shows how each thread can use the µTiles API for creating tags, changing labels, and passing capabilities to other threads. For instance, thread 2 gains access to µTile 18 by directly getting the \( b^+ \) capability from thread 1. Since it does not have the \( b^- \) capability, it cannot change µTile 18 permissions or its memory mappings.

It should be noted that µTile ID is not the same as its label. All security-critical data structures for managing labels are stored inside the kernel, so they can not be modified by userspace attackers. Table 5 describes the userspace µTile API. Threads can lock access or permission changes of their µTiles via utile_lock, which temporarily change µTile tag to restrict any modifications of µTiles state. A locked µTile can only be accessed by calling utile_unlock.

A tagged thread can create a child by calling utile_clone; the child thread does not inherit any of its parent’s capabilities. However, the parent can create a child with a list of its µTiles and selected capabilities as an argument of utile_clone. For instance, in Figure 2,
thread 1 creates its child with only a “plus” capability to two of its µTiles (18, 46).

### 3.3.1 µTiles Memory Management

µTiles dedicated VM abstraction provides a familiar semantics for µTiles-aware memory management, VM tagging, mappings, protection, page faults handling, and least privilege enforcement. It bypasses most of the kernel’s paging abstraction. Hence, it does not require extensive modifications to the kernel memory management structures that might otherwise introduce security holes due to inevitable TLB and memory management bugs [53]. Threads’ security policy enforcement is done by adding custom security hooks in the VM interfaces that check the correct flow of labels (§3.3).

To improve performance (§2.1), the VM abstraction maps per thread’s high-level security policies and memory management interface to the underlying hardware domains that also hide its limitations(§2.3). Example code 1 shows a basic way of using µTiles to protect sensitive content in a single thread.

An application creates a new µTile by calling `utile_create`; the kernel creates a unique tag with both capabilities (since it is the owner) and adds it to the thread’s label and capability lists, and returns a unique ID. Then the owner thread maps pages to its µTile by calling `utile_mmap` that updates the µTile’s metadata with its address space ranges. The kernel allows mappings based on the thread’s labels and free hardware domains. If there is a free hardware domain, it maps pages to that domain and places it to µTiles cache. When the µTiles already exists in the cache, further access to it is fast. When there is no free hardware domain, we have to evict one of the µTiles from the cache and map the new µTile metadata to the freed hardware domain; this requires storing all the necessary information for restoring the evicted µTile, such as its permission, address space range, and label. The caching process can be further optimized by tuning the eviction rate and suitable caching policies similar to libMPK [40].

```c
/* create a utile */
int utile_id = utile_create();

/* map a memory region to the utile */
memblock = (char*) utile_mmap(utile_id,
addr, len, prot , 0, 0); //

// set permissions by utile_mprotect

/* allocate memory from utile */
private_blk = (char*) utile_malloc(
utile_id, priv_len);

/* make utile inaccessible */
lock_utile(utile_id);

/* cleanup utile */
utile_free(private_blk);
utile_munmap(utile_id, memblock,len);

Listing 1: Basic µTiles usage
```
Map a page group to a µTile
free memory from a µTile
Allocate memory within a µTile
Unmap all pages of a µTile
change an µTile’s pages permission
Get a µTile permission

The LSM initializes the required data structures, such as the labeling model we described (§3.3).

To mitigate attacks inside a single thread, unauthorized access to µTiles, by accident or other malicious code, are restricted once the owner calls utile_lock. Then application developer can allow only her trusted functions or necessary parts of the code to gain access by calling utile_unlock. For example, our single-threaded OpenSSL uses this mechanism for isolating private keys from vulnerabilities like Heartbleed bug §5.2).

The µTiles virtual memory abstraction is implemented as a set of kernel functions similar to their Linux equivalents (e.g., do_mmap, do_munmap and do_mprotect) with similar high-level semantics but replaces the pagining complexity with simpler hardware domain-based operations. When an application creates a µTile by calling utile_create and maps an address range to it via utile_mmap, The µTiles VM manager tags a 1MB aligned address space that covers the requested range, stores µTiles metadata, maps it to a free hardware domain and updates the µTiles cache. When µTiles are mapped to hardware domains, the exact physical domain number is hidden from the userspace code to avoid possible misuse of the API. The mappings between µTiles and hardware domains are maintained through a cache-like structure similar to libmpk [40]. A µTile is inside the cache if it is already associated with a hardware domain; otherwise, it evicts another µTile based on the least recently used (LRU) caching policy while saving all require metadata for restoring the µTile mapping and permission flags.

µTiles owners (or authorities) can change their µTiles’ permission via utile_mprotect. This operation is faster when the requested permission matches one of the domain’s supported options (Table 4) or undergo the overhead of effecting TLB. Any violation of µTiles permissions causes a µTiles fault that leads to the violating thread being terminated.

Userspace: To reduce the size of the TCB, we did not modify existing system libraries (e.g., glibc) and in-

Table 6: Some of userspace µTiles memory management API. Each µTile has an id and is a tagged kernel object internally. µTiles access control is checked within the kernel.

| Name                  | Description                                                                 |
|-----------------------|-----------------------------------------------------------------------------|
| utile_create(id)      | Create a new µTile                                                          |
| utile_destroy(id)     | Destroy a µTile                                                            |
| utile_malloc(id, size)→void* | Allocate memory within a µTile                                           |
| utile_free(id)        | free memory from a µTile                                                   |
| utile_mprotect(id, ...) | change an µTile’s pages permission                                         |
| utile_mmap(id, ...)+  | Map a page group to a µTile                                                |
| utile_munmap(id, ...)  | Unmap all pages of a µTile                                                |
| utile_get(id)→perms   | Get a µTiles permission                                                    |

The µTiles access control and the security model is implemented as a new Linux Security Module (LSM) [39] with only four custom hooks.

We modify the Linux task structure to store the metadata required to distinguish µTiles threads from regular ones. Specifically, we add fields for storing µTiles metadata, label/ownership as an array data structure holding its tags (each tag is a 32-bit identification whose upper 2 bits stores plus and minus capabilities), a capability list; all included as a specific task’s cred→security data structure. We implemented a hash table-based registry to make mostly used operations (e.g., store, set, get, remove) on these data structures more efficiently.

The LSM also provides custom security hooks for parsing userspace µTiles memory management API, labeling a task, checking whether the task is labeled, and checking if the information flow between two tasks is allowed. These security hooks are added in various places within the kernel to guard µTiles against unauthorized access or permission change by either the POSIX API (e.g., mmap, mprotect, fork) or the µTiles API. For example, forking a labeled task should not copy its labels and capability lists, and is enforced using these security hooks. As another example, µTiles-independent applications that using traditional POSIX APIs can not perform any unauthorized memory allocation from a random µTile or mapping pages to it; this is restricted via the security hooks that are placed in the kernel’s virtual memory management layer similar to the µTiles VM manager (Table 6).

The µTiles kernel modifications: The µTiles access control and the security model is implemented as a new Linux Security Module (LSM) [39] with only four custom hooks. The LSM initializes the required data structures, such as the label registry. Access control system calls (Table 5) for enforcing least privilege are implemented as a part of the LSM, including locking µTiles, transferring capabilities, authority operations, and declassification based on the labeling model we described (§3.3).

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The LSM also provides custom security hooks for parsing userspace µTiles memory management API, labeling a task (set_task_label), checking whether the task is labeled (is_task_labeled), and checking if the information flow between two tasks is allowed (check_labels_allowed). These security hooks are added in various places within the kernel to guard µTiles against unauthorized access or permission change by either the POSIX API (e.g., mmap, mprotect, fork) or the µTiles API. For example, forking a labeled task should not copy its labels and capability lists, and is enforced using these security hooks. As another example, µTiles-independent applications that using traditional POSIX APIs can not perform any unauthorized memory allocation from a random µTile or mapping pages to it; this is restricted via the security hooks that are placed in the kernel’s virtual memory management layer similar to the µTiles VM manager (Table 6).

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stead provided a small userspace library for µTiles operations that summarized in Tables 5 and 6. As demonstrated, the library supports a familiar API for memory management within a µTile, including `utile_malloc` and `utile_free` for memory management; which is implemented as a custom memory allocator similar to HeapLayer [15]. This allocates memory from an already mapped µTile. For each µTile, there is a memory domain in-kernel metadata structure that keeps essential information such as the µTile address space range (base and length) and the two lists of free blocks from the head and tails of the µTile region that is used when searching for free blocks of memory.

5 Evaluation

We evaluated our implementation of µTiles on a Raspberry Pi 3 Model B [4] that uses a Broadcom BCM2837 SoC with a 1.2 GHz 64-bit quad-core ARM Cortex-A53 processor with 32KB L1 and 512KB L2 cache memory, running a 32-bit unmodified Linux kernel version 4.19.42 and glibc version 2.28 as the baseline. We use microbenchmarks and compartmentalize real-world applications to evaluate µTiles in terms of performance and usability (§2.1 and §2.3) by answering the following questions:

- What is the initialization and runtime overhead of µTiles? How does utilizing hardware domains impact performance?
- Are µTiles practical and adaptable for real-world applications? How much application change and programming effort is required? What is the performance impact? How does it perform for hardening a multi-threaded environment?
- What is the memory footprint of µTiles? Is it suitable for small IoT devices? How much memory does it add (statically and dynamically) to both the kernel and userspace?

5.1 Microbenchmarks

Creating µTiles: Table 7 tests the cost of creating and mapping pages to µTiles using `utile_mmap` when µTiles are directly mapped to hardware domains, as compared to virtualized µTiles when there is no free hardware domain and requires evicting µTiles from the cache. The results show that when there is a free hardware domain, the performance improves by 4.9% compared to the virtualized one. Note that creating µTiles is usually a one-time operation at the initial phase of an application.

![Figure 3: Cost of µTiles memory allocation (malloc & free). On average `utile_malloc` outperforms `malloc` by a small rate (0.03%).](image)

| Operation                  | Overhead | stddev |
|----------------------------|----------|--------|
| Direct `utile_mmap/munmap` | 4.8%     | +0.17% |
| Virtualised `utile_mmap/munmap` | 10.01% | +0.15% |

Table 7: Cost of creating µTiles when directly mapped to hardware domains vs virtualized mapping that requires µTiles caching. The results show the average of 10000 runs.

Memory protection & allocation: Changing µTile permissions and memory allocation operations inside µTiles have the most impact on runtime overhead. We evaluated the performance comparison of `utile_mprotect` vs glibc `mprotect` based on permission flags. Since hardware memory domains do not have flexible access control options (§2.3), we cannot benefit from a control switch of domains using the DACR register for all possible permission flags such as the RO, WO, and EO variants. Our results show that on average `utile_mprotect` is 1.17x faster than `mprotect` for no access (PROT_NONE) or RW permissions (PROT_READ | PROT_WRITE), but 1.3x slower for read/write/execute-only options that are emulated.

Allocating memory using `utile_malloc` is on average 1.08x faster than glibc `malloc` for blocks ≤ 64KB and introduces a small overhead (8.3%) for larger blocks (> 64KB) as demonstrated in Figure 3. This cost can be optimized by using high-performance memory allocators [34]. We report the average of running microbenchmarks 20000 times and show how utilizing µTiles provides small overhead for memory allocation and permission changes.

Threading: We tested the cost of µTile threading operations (creating and joining) through `utile_clone` that creates µTile-aware threads; `utile_clone` internally uses the `clone` syscall with minor modifications...
to restrict any credential sharing with the child by default (instead it provides additional clone options for passing parent’s capabilities to its child). We implemented utile_clone similar to waitpid. Table 4 shows utile_clone outperforms pthread_create by 0.56% and fork by 83.01%. This gain is attributed to the utile_clone simply doing less sharing for initializing new threads.

**Codebase overhead:** Another factor towards the usability of µTiles is the codebase size, which is important both from a security perspective and the resource limitations of small IoT devices. We implemented µTiles as a Linux kernel patch with no dependency on any third-party library. As Table 8 shows, it adds less than 5.5K LoC in total to both the kernel (≈3K) and userspace (<2.5K). It adds 7KB to the kernel image size and adds 204KB for kernel slabs at runtime. The userspace library only needs ≈10KB of memory. These results show that the µTiles memory footprint is extremely low and suitable for many resource-constrained uses.

| Added LoC | Linux Kernel | Userspace |
|-----------|--------------|-----------|
| static(7KB) slab(204KB) | static(3023) | static(2405) |

Table 8: µTiles codebase size and Memory footprint in the Linux Kernel and userspace

## 5.2 OpenSSL

OpenSSL is a widely used open-source library implementing cryptography operations and the transport layer security (TLS) protocol. It handles sensitive content such as private keys and encrypted data. Hence it significantly benefits from isolating its sensitive content in separate compartments to mitigate information leakage attacks (e.g., Heartbleed). We modified OpenSSL to utilize µTiles for protecting private keys from potential information leakage by storing the keys in protected memory pages inside a single µTile or multiple µTiles assigned per private key. Using multiple µTiles provides stronger security while adding more overhead due to the cost of caching µTiles.

To enable µTiles inside OpenSSL, all the data structures that store private keys such as EVP_PKEY needed protected heap memory allocation. This meant replacing OpenSSL_malloc with utile_malloc and using utile_mmap at the initialization phase for creating one or multiple (per session) µTiles to store private keys. After storing the keys, access to µTiles is disabled by calling utile_lock. Only trusted functions that require access to private keys (e.g., EVP_EncryptUpdate or pkey_rsa_encrypt/decrypt) can access µTiles by calling utile_unlock. Modifying OpenSSL required fairly small code changes, and added only 281 LoC.

We measured the performance overhead of µTiles-enabled OpenSSL by evaluating it on the Apache HTTP server (httpd) that uses OpenSSL to implement HTTPS. Table 5 shows the overhead of ApacheBench httpd with both the original OpenSSL library and the secured one with µTiles. ApacheBench is launched 100 times with various request parameters. We choose the TLS1.2 DHE-RSA-AES256-GCM-SHA384 algorithm with 2048-bit keys as a cipher suite in the evaluation.

The results show that on average µTiles introduces 0.47% performance overhead in terms of latency when using a single µTile for protecting all keys, and 3.67% overhead when using a separate µTile per session key. In the single µTile case, the negligible overhead is mainly caused by in-kernel data structure maintenance for enforcing privilege separation and handling µTiles metadata. In the multiple-µTiles case, since httpd utilizes more than 16
µTiles (allocates a new µTile per session), it causes higher overhead due to the caching costs within the kernel.

5.3 LevelDB

To show how µTiles can be used for hardening multi-threaded applications, we modified Google’s LevelDB that is a fast key-value store and storage engine used by many applications as a backend database. It supports multithreading for both concurrent writers to insert data into the database as well as concurrent read to improve its performance. However, there is no privilege separation between threads, so threads can not communicate securely with the database and protect their private content from other threads. We modified LevelDB to evaluate performance overhead of using the µTiles secure threading model when each thread has its own private storage that cannot be accessed by other threads.

We replaced the LevelDB threading backend (env_posix) that uses pthreads with µTiles-aware threading, where each thread creates an isolated µTile to protect its private storage and sensitive computations. We used the LevelDB db_bench tool (without modification) for measuring the performance overhead of µTiles.

We generate a database with 400K records with 16-byte keys and 100-byte values (a raw size of 44.3MB). The number of reader threads is set to 1, 2, 4, 8, 16, and 32 threads for each successive run. The threads operate on randomly selected records in the database. The results in Figures 6 and 7 show how multithreading can improve the performance of LevelDB, and utilizing µTiles adds a small overhead on write (5%) and read (1.98%) throughput. As with OpenSSL previously, modifying LevelDB required only adding 157 lines-of-code around the codebase.

Figure 6: LevelDB: performance overhead of µTiles-based multithreading compare to pthread-based in terms of write throughput (5%).

Figure 7: LevelDB: performance overhead of µTiles-based multithreading compare to pthread-based in terms of read throughput (1.98%).

6 Discussion

We have shown that µTiles provides a practical and efficient mechanism for intra-process isolation and inter-thread privilege separation on data objects. However, the mechanism can still be taken further.

6.1 Address Space Protection Limitations

For single-threaded scenarios (e.g., event-driven servers), although µTiles can protect sensitive content from unsafe libraries or untrusted parts of the applications, it can be vulnerable if the untrusted modules are also µTiles-aware and already use the µTiles APIs. The untrusted library can use utile_get to query µTile IDs and use the API to reach them. It should be noted that this is not an issue for untrusted legacy libraries. Additionally, to remove the possibility of such attacks, it is better to run these unsafe libraries in a separate thread, which is isolated through µTiles abstraction.

Various covert attacks [45] and side-channel attacks such as Meltdown [35] and Spectre [30] demonstrate how hardware and kernel isolation can be bypassed [28]. µTiles are currently vulnerable to these class of attacks, although the existing countermeasures within the Linux kernel are sufficient protection. We believe these types of attacks are important security threats, and hardening µTiles against them could be significant future work.

6.2 Compatibility Limitations

Providing a solution that is compatible with various operating systems and heterogeneous hardware is challenging. Though we picked our base kernel on Linux and built the abstraction with minimal dependencies, some application
modification is still required. We believe that building more compatibility layers into our existing userspace implementation is possible. We are open-sourcing our code with further feedback and patches from the relevant upstream projects we have modified.

Although Linux is the most widespread general-purpose kernel for embedded devices, many even smaller devices depend on operating systems such as FreeRTOS. These often use ARM Cortex-M based hardware features for isolation (such as memory protection units (MPUs) [10, 46]), or more recent CPUs with memory tagging extension [9]. We plan to explore the implementation of the µTiles kernel memory management on these single-address space operating systems, as well as broadening the port to Intel architectures on Linux (where the memory domains support is generally simpler to use than on ARM).

7 Related work

There are many software or hardware-based techniques for providing process and intra-process memory protection.

**OS/hypervisor-based solutions:** Hardware virtualization features are used for in-process data encapsulation by Dune [14] by using the Intel VT-x virtualization extensions to isolate compartments within user processes. However, overall, the overheads of such hardware virtualization-based encapsulation are much more heavyweight than µTiles, and not practical for IoT applications.

ERIM [47], light-weight contexts (lwCs) [36] and secure memory views (SMVs) [27] all provide in-process memory isolation and have reduced the overhead of sensitive data encapsulation on x86 platforms. The µTiles abstraction provides stronger security guarantees and privilege separation. It allows more flexible ways of defining security policies for legacy code – e.g., within a single thread as in our OpenSSL example. Its small memory footprint makes it suitable for smaller devices, and it takes advantage of efficient virtual memory tagging by using hardware domains to reduce overhead.

Burow et al. [18] also leverage the Intel MPK and memory protection extensions (MPX) to isolate the shadow stack. Our efforts to provide an OS abstraction for in-process memory protection is orthogonal but more general than these studies, which all have potential use cases for µTiles. Our focus has also been on lowering the resource cost to work well on embedded and IoT devices, while these projects are also currently x86-only.

HiStar [51] is a DIFC-based OS that supports fine-grained in-process address space isolation. It influenced our work, but we focused on providing a more general-purpose solution for small devices by basing our work on the Linux kernel instead of a custom operating system. Other DIFC-based systems only support per-process protection with very large overhead [32, 49] or need specific programming language support [43].

**Compiler & Language Runtime:** Various compiler techniques introduce memory isolation as part of a memory-safe programming language. These approaches are fine-grained and efficient if the checks can be done statically [23]. However, such isolation is language-specific, relies on the compiler and runtime, and not effective when applications are co-linked with libraries written in unsafe languages and libraries. µTiles abstractions are fine-grained enough to be useful to these tools, for example, to isolate unsafe bindings.

Software fault isolation (SFI) [44, 48] uses runtime memory access checks inserted by the compiler or by rewriting binaries to provide memory isolation in unsafe languages with substantial overhead. Bounds checks impose overhead on the execution of all components (even untrusted ones), and additional overhead is required to prevent control-flow hijacks, which could bypass the bounds checks [31]. ARMLock [54] is an SFI-based solution that offers lower overhead utilizing ARM memory domains. Similarly, Shreds [19] provides new programming primitives for in-process private memory support. µTiles also uses ARM memory domains for improving the performance of intra-process memory protection, but is a more flexible solution for intra-process privilege separation; it provides a new threading model for dynamic fine-grained access control over the address space with no dependency on a binary rewriter, specific compiler or programming language (See Table 2).

**Hardware-enforced techniques:** A wide range of systems use hardware enclaves such as Intel’s SGX [7] or ARM’s TrustZone [8] to provide a trusted execution environment for applications that against malicious kernel or hypervisor [12, 25, 26].

The trust model exposed by these hardware features is very fixed, and usually results in porting monolithic codebases to execute within the enclaves. EnclaveDom [38] utilizes Intel MPK to provide in-enclave privilege separation. µTiles provide better performance and more general solutions with no dependency on these hardware features; hence it can be used for in-enclave isolation and secure multi-threading to improves both security and
performance of enclave-assisted applications.

Ultimately, dedicated hardware support for tagged memory and capabilities (e.g., ARM MTE [9]) would be the ideal platform to run μTiles on [52]. We are planning on building this support as future work, with a view to analyzing if the overall increase in hardware complexity offsets the resource usage in software for embedded systems.

8 Conclusions

We have presented μTiles – an OS abstraction, a set of security primitives and APIs for protecting data objects inside a shared address space, and providing flexible privileged separation for multithreaded applications. We designed μTiles to be extremely lightweight for IoT applications, with no programming language requirements, and with a small performance overhead by utilizing efficient hardware-based memory protection that makes it practical for a variety of uses cases and security-sensitive applications.

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