A Direct Modulation for Matrix Converters Based on the One-Cycle Atomic Operation Developed in Verilog HDL

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Abstract—This article presents a fast direct pulsewidth modulation (PWM) algorithm for the conventional matrix converters developed in Verilog hardware description language. All PWM duty cycle calculations are performed in one cycle by an atomic operation designed as a digital module using field-programmable gate array basic blocks. The algorithm can be extended to any number of output phases. The improved version of the discontinuous direct analytic voltage PWM (DAV-PWM) method is proposed, in which the use of trigonometry, angles, and program loops has been eliminated. The proposed DAV-PWM is equivalent to the space vector modulation; it can be applied during input asymmetry and also allows for the control of the displacement input angle. The proposal has been verified using the circuit simulation in PSIM, digital structure modeling in ModelSim, and finally through an experiment.

Index Terms—AC–AC converters, field-programmable gate array (FPGA) device, matrix converters, pulsewidth modulation (PWM).

NOMENCLATURE

\( T \)
Transposition of the matrix.

\( v_i \)
Measured input voltages \([v_{i1}, v_{i2}, v_{i3}]^T\).

\( v_o \)
Averaged output voltages \([v_{o1}, v_{o2}, v_{o3}]^T\).

\( i_i \)
Averaged input currents \([i_{i1}, i_{i2}, i_{i3}]^T\).

\( i_o \)
Measured output currents \([i_{o1}, i_{o2}, i_{o3}]^T\).

\( D \)
PWM duty cycle matrix with size \(3 \times 3\).

\( x \)
Real signal component.

\( y \)
Imaginary signal component.

\( v_{ix} \)
Matrix of \(v_i\) in-phase components.

\( v_{iy} \)
Matrix of \(v_i\) quadrature components.

\( v_{ox} \)
Real parts of reference voltages \([v_{o1x}, v_{o2x}, v_{o3x}]^T\).

\( v_{oy} \)
Imaginary parts of reference voltages \([v_{o1y}, v_{o2y}, v_{o3y}]^T\).

\( \phi_i \)
Input displacement angle.

\( s_i, s_o \)
Input and output voltage sectors.

\( \omega_i = 2\pi f_i \), where \( f_i \) is the input frequency.

\( \omega_o = 2\pi f_o \), where \( f_o \) is the output frequency.

\( q = V_o/V_i \), Voltage transfer ratio.

\( q_{\text{max}} = \sqrt{3}/2 \), Maximum value of \( q \).

\( T_{\text{PWM}} \)
Modulation period.

\( f_s = 1/T_{\text{PWM}} \) sampling frequency.

I. INTRODUCTION

CONVENTIONAL matrix converter (CMC), shown in Fig. 1, contains semiconductor switches arranged into a matrix configuration divided into three cells: \(\{h_{11}, h_{21}, h_{31}\}, \{h_{12}, h_{22}, h_{32}\}, \) and \(\{h_{13}, h_{23}, h_{33}\}\). Compared to ac–dc–ac back-to-back converters with large capacitors in the dc link, the CMC allows for direct ac–ac conversion using the small input filter, which is an advantage of these solutions [1]–[3]. The general motor drive application scheme with the matrix converter is illustrated in Fig. 1. Such a topology permits for regenerative power from the electrical motor with negligible input grid current harmonic content. An important feature of the CMC control is the possibility to adjust the input displacement angle to zero [4]–[6]. The single switch \(h\) can be built from two transistors with two diodes or two reverse-blocking insulated-gate bipolar transistor (RB-IGBT) devices [1], [7].

The single CMC’s cell is properly controlled to prevent line-to-line short circuits and to maintain a continuous waveform of the load current. Due to the safe commutation process requirement, the dead-time mechanism should be applied during the generation of switch control signals. The overvoltage upon the switch, caused by an interruption of the inductive current, has to be absorbed by a clamp circuit [8], [9]. The reduction of the scale of both the input filters and the clamp circuit can be reached by applying faster semiconductors with a high operation frequency; thus, a panel size of the CMC can be significantly reduced [10]. Attempts to integrate this panel with the electric motor have already taken place [11]. Gallium nitride (GaN) and silicon carbide (SiC) semiconductors offer fundamental advantages over silicon solutions [12]–[15]. The switch’s operation frequency can be very high compared to the silicon counterparts, which makes these devices great for high-frequency applications, which also include high-speed drives in compressors or high-speed generators in gas turbines [16]–[18]. Such applications require complex calculations within a short period of time.
This article presents an approach to computations performed in a field-programmable gate array (FPGA) in one step, during one cycle, without trigonometry and angles. Thus, the execution time of the PWM duty cycle calculation is atomic and limited only by the critical timing constraints of the FPGA device. The development of a digital structure that performs such an algorithm, in one clock cycle, requires the use of an appropriate modulation method that uses only simple arithmetic operations supported by Verilog HDL. Moreover, the proposed solution should allow us to obtain the maximum voltage transfer ratio and to adjust the angle at the input of the system, which is a characteristic feature of the PWM for the CMC [1].

PWM strategies for the CMC have been widely reported in the literature, such as the direct control by the Venturini approach [3], [19], [20], scalar control realized according to the Roy method [21], and the space vector modulation (SVM) [1], [22]. Other control methods, such as hysteresis and direct torque control, are interesting alternatives [23], [24]. However, the torque ripple in the low-speed region or switching frequency variations according to the change of the motor speed are drawbacks of these approaches. The aforementioned methods are not suitable for developing the simplest solution, which should be built from basic digital elements such as multiplexes, adders, and multipliers. A simplified carrier-based modulator based on the concept of a virtual matrix converter was presented in [25]. The proposed algorithm allows for obtaining the same instantaneous matrix states as the SVM method with a smaller number of calculations. Although the solution represents a more synthetic and systematic approach, this original approach has a major disadvantage. An input displacement angle is permanently equal to zero and cannot be adjusted.

The concept of simplifying and generalizing the PWM algorithm is also presented in [26] and [27]. As with the previous method, the proposal makes it possible to calculate PWM duty cycles without trigonometry with minimal computational effort. Moreover, the proposed computation scheme allows for the application of various methods of power factor control. Among the described modulation methods, the authors indicated that the direct analytic voltage pulsewidth modulation (DAV-PWM) is optimal because it allows reaching the maximum voltage transfer ratio equal to 0.866 with the same switch state collection as the SVM modulation. This algorithm has been developed as a sequential code, which contains a program loop for preselection input voltage vectors. Such a program loop has to be eliminated within the atomic and concurrent implementation based on an FPGA device. This article mainly addresses this issue and proposes certain improvements, which are clarified in Section II. The theoretical basis of an improved DAV-PWM algorithm, ready for the hardware description language (HDL) conversion, has been presented in the next section. Power electronics simulation, modeling based on the HDL, and hardware-in-the-loop (HIL) verification have been presented in Section IV. The conducted research path is summarized in Table I. Experimental results are presented in Section V. The Verilog HDL code of the improved DAV-PWM algorithm is available in an Appendix after the conclusion section.

### II. PROPOSAL FOR CHANGES IN THE DAV-PWM

The use of an FPGA chip offers new possibilities to design the computation structure with a short execution time, provided that these algorithms do not use advanced mathematical functions, such as trigonometric functions, and do not contain the program loops. Therefore, the computation scheme of the DAV-PWM should be optimized. The most important modifications of the DAV-PWM algorithm are explained in the following subsections.

#### A. Quadrature Component Generation of an Input Voltage

Each input voltage with the pulsation, \( \omega_i \), can be expressed as a rotating vector, as shown in Fig. 3. For pure sinusoidal input voltages with an amplitude \( V_i \), the imaginary coordinates are just...
If the input voltages are not perfectly sinusoidal, all coordinates should be determined using Hilbert filter or fast-Fourier-transform/discrete-Fourier-transform-based operation [28]–[30], which cannot be easily implemented in the FPGA without using an advanced intellectual property core. However, calculations using Clarke’s triple transforms, although simple, in the case of asymmetry cause a distortion of the input current [26]. In practice, error signals in the form of dc offsets, glitches, and momentary voltage sags may occur in measurements. Therefore, coordinates should be determined using Hilbert filter or quadrature components. Thus, the analytic signals corresponding to input voltages can be expressed as follows:

\[ V_1 = V \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \cos(\omega t - 2\pi/3) & \sin(\omega t - 2\pi/3) \\ \cos(\omega t + 2\pi/3) & \sin(\omega t + 2\pi/3) \end{bmatrix} \]  

(1)

To achieve the maximum voltage transfer ratio, the trajectory should be shifted to the nearest vertex of the triangle \( \Delta_{[1,2,3]} \). According to the original DAV-PWM algorithm, coordinates of the shift vector are designated by the program loop routine, in which the algorithm selects the best candidate among the input voltage vector set [26]. This solution can also be improved to meet the optimization requirements. The Gamma modification in (2) can be replaced by a formula containing a rotation matrix. Thus, the relation between input and output voltages in the CMC may be written in a following general form:

\[ V_o \cdot R = D \cdot V_i \]  

(4)

where

\[ R = \begin{bmatrix} \cos(\phi_1) & -\sin(\phi_1) \\ \sin(\phi_1) & \cos(\phi_1) \end{bmatrix} \]  

(5)

and \( D \) is a square matrix that contains all PWM duty cycles

\[ D = \begin{bmatrix} d_{11} & d_{12} & d_{13} \\ d_{21} & d_{22} & d_{23} \\ d_{31} & d_{32} & d_{33} \end{bmatrix} \]  

(6)

for switches \( h_{11} \)–\( h_{33} \). Taking into account the properties of the \( R \) matrix, (4) can be finally rewritten as

\[ V_o = D \cdot (V_i \cdot R^{-1}) = D \cdot V_{IR}. \]  

(7)

Now, the desired angle of displacement \( \phi_1 \) can be achieved by the angular displacement of the input vector collection (1). This result has a significant impact on the optimization of the original DAV-PWM algorithm because all calculations can be performed for reference voltage, which always has a zero imaginary component. Hence, the selection of the shift coordinates is simplified and is free from an undesired program loop. Reference to the new synthesis field \( \Delta_{R[1,2,3]} \) shown in Fig. 4, the shift vector always corresponds to an intermediate vertex between the top and the bottom vertex, which can be immediately selected in
a much simpler way using comparators instead of the program loop.

C. Simplification of the Reference Output Voltage Generation

The trajectory shift operation eliminates the common voltage from (2). Therefore, this component can be deleted in the proposed version of the DAV-PWM algorithm. As a consequence, only the sinusoidal voltage references can be applied in the algorithm.

III. IMPROVED DAV-PWM ALGORITHM

A schematic diagram of the improved DAV-PWM algorithm is presented in Fig. 5. The input voltage \( \{v_{i1}, v_{i2}, v_{i3}\} \) from measurements is converted into analytic signal pairs using the DSOGI-OSG or DSOGI-FLL structure. Next, all input vectors are multiplied by the rotation matrix \( R(5) \), which takes arguments—\( \cos \phi_i \) and \( \sin \phi_i \)—from the input power factor control routine. Three coordinates pairs for modulating signals \( v_o = \begin{bmatrix} v_{o1x} + v_{sx} v_{sy} \\ v_{o2x} + v_{sx} v_{sy} \\ v_{o3x} + v_{sx} v_{sy} \end{bmatrix} \) (8) are selected according to the input sector \( s_{IR} \) and the output sector \( s_o \). Both sectors are directly identified using comparators, as shown in Figs. 6 and 7.

Dependencies of the shift vector coordinates on the input and output sectors are referred to Table II. The collection of PWM duty cycles for switches \( h_{11} \), \( h_{21} \), and \( h_{31} \) can be calculated without trigonometry and angles using the following formulas:

\[
d_{21} = \xi \cdot \det \begin{bmatrix} v_{iR2x} - v_o(1,1) & v_{iR2y} - v_o(1,2) \\ v_{iR3x} - v_o(1,1) & v_{iR3y} - v_o(1,2) \end{bmatrix}
\]

\[
d_{31} = 1 - d_{11} - d_{21}
\]

where \( \det \) means the determinant of the 2 \( \times \) 2 matrix, and

\[
\xi = \det \begin{bmatrix} v_{iR2x} - v_{o(1,1)} & v_{iR2y} - v_o(1,2) \\ v_{iR3x} - v_{o(1,1)} & v_{iR3y} - v_o(1,2) \end{bmatrix}^{-1}
\]

Other PWM duty cycles, in the second and third rows of (8), can be computed analogously. The PWM duty cycle matrices \( D \) within an input and output voltage sectors in DAV-PWM are summarized in Table III. The \( D \) matrix consists of nine duty cycles \( d_{11} - d_{33} \), which are transformed into the sequence of logical signals for switch state control. These sequences are usually generated by the specialized digital structure based on counters and comparators according to the selected commutation strategy in the CMC [37]–[41]. The cyclic Venturini approach and the four-step commutation strategy have been chosen [5].

IV. POWER ELECTRONICS SIMULATION, HDL MODELING, AND HIL VERIFICATION

This section presents results obtained during the functional simulation in PSIM11 software, behavioral modeling of the HDL using ModelSim Intel FPGA environment, and the HIL
verification using Quartus Intel FPGA software with the signal-tap logic analyzer (STLA) tool.

A. Simulation and Switch State Sequences Comparison for DAV-PWM and SVM

The PSIM environment was used to simulate CMC control and verify the algorithm compiled as the user DLL block, which is written in C language. The proposed improved algorithm maintains the important properties of DAV-PWM proposed in [26]. The obtained sequences of switch states, including the waveforms of line-to-line voltages, remain unchanged. An input voltage amplitude asymmetry or phase angle disturbance change the shape and area of the synthesis field limiting the value of the voltage transfer ratio $q$. However, during operation with a unity power factor, currents on both sides of the converter are sinusoidal, as can be seen in Fig. 8, where three selected input conditions for $RL$ load type are presented. This article proposes a direct modulation algorithm, in which the switch states are not explicitly declared as in the conventional SVM modulation method. Table IV presents all switch states of the CMC. Black dots represent the active switches in the matrix panel. Several modulation techniques are compared in [42] and analyzed in [43]. Among the described switch state sequences, two of them can be distinguished: ten-switch double-sided sequence shown in Fig. 9 and low-distortion eight-switch sequence illustrated in Fig. 10. The switch states for DAV-PWM can be derived using the switch state parser connected with all nine control signals $h_{11} – h_{33}$. The state parser is a MATLAB script, which operates on the PSIM data saved in the CSV file format. Decoded SVM switching sequences for DAV-PWM with the cyclic Venturini scheme are collected in Table V.

The following major conclusions can be formulated based on the switch state sequence comparison.

1) Both the SVM method and DAV-PWM use the same active vectors in their input and output voltage sectors.
2) The construction of the switch state sequences in the DAV-PWM method is identical to that of sequences in SVM shown in Fig. 10.
3) The proposed DAV-PWM allows for reducing the harmonic distortion by having two zero vectors per period, as reported in [42], but only the approach illustrated in Fig. 9 permits for reduction of switch operation frequency.
4) Tabularizing the switch state sequences is not necessary for a carrier-based modulation such as DAV-PWM.

B. HDL Compilation

The ModelSim software was applied for modeling the digital module of the PWM duty cycle computation, in which the behavioral equivalent of the C-language-developed DAV-PWM
had been coded using Verilog HDL. The ModelSim-simplified simulation diagram is shown in Fig. 11. This software is usually dedicated for digital core or module simulation, but, here, that software has been used for developing the matrix converter control module. The fixed-point Q15 format arithmetic, in comparison with the single-precision format, often permits for developing very fast algorithms without pipelines and recursive operations. Continuous signals, such as input voltages, can be represented by the large tables of 16-bit values. The discrete sampling time was generated by the counter with auto-reload. An input displacement angle has been expressed as a sin–cos pair expressed by constant Q15 values. For simulation purpose only, the cyclic Venturini switching strategy was developed in Verilog HDL using nonsynthesizable modeling based on the signal delay command. This Verilog HDL piece of code is intentionally depicted in the drawing. Selected electrical waveforms, sectors, and PWM duty cycles in the analog form, modeled using ModelSim simulation environment, are shown in Fig. 12.

The load current was modeled using the first-order infinite impulse response (IIR) filter. All line-to-line load voltages were generated using the signal switching approach controlled by the input sector number.

C. HIL Verification

For early validation of the Verilog HDL project file synthesizability, the Quartus 18.1 with the STLA was used. An evaluation board DE10-Lite was used during the HIL test. Two debugging tools were used during the validation stage. As shown in Fig. 13, the In-System Sources and Probes tool was used to give phase and frequency of signals generated by CORDIC numerically controlled oscillators, while the STLA tool allowed to visualize and record the selected signals in real time. Fig. 14 shows improved DAV-PWM algorithm signals during the debug session using the STLA for $\omega_1/\omega_o = 2.67$, $f_s = 1$ MHz, and $q = 0.8$. The proposed PWM duty cycle computation module resource utilization is presented in Table VI.

![Fig. 11. 5-kW matrix converter with the DSP–FPGA control board.](image1)

![Fig. 12. Schematic diagram of the experiment configuration.](image2)

![Fig. 13. Block diagram of computation performed by the FPGA device during an experiment.](image3)

![Table VI](table1)
Fig. 14. Experimental results for $\omega_o/\omega_i = 0.5$ and symmetric input amplitudes for (a) unity power factor ($q = 0.86$ and $\phi_i = 0$) and (b) reactive power generation ($q = 0.6$ and $\phi_i = -\pi/4$).

Fig. 15. Output and input currents for asymmetrical input voltage source for DAV-PWM: $q = 0.55$ and $\omega_o/\omega_i = 0.5$.

Fig. 16. The schematic diagram of the experiment configuration.

V. EXPERIMENTAL RESULTS

A 5-kW CMC with the control board, shown in Fig. 15, based on the multicore ADSP-SC589 DSP from Analog Devices and the MAX10 Intel FPGA device was used during the experimental stage. The bidirectional power switch was built using two SiC transistors C3M0075120D. The schematic diagram of the experiment configuration is shown in Fig. 16. The block diagram of computation performed by the FPGA device during an experiment is presented in Fig. 17. The Q15 symbol indicates digital structures based on fixed-point arithmetic, while SP means the floating-point IP core used for time cycle scaling. This element is needed to preserve constant modulation frequency. The modulation period was 100 $\mu$s, while algorithm computation in Q15 blocks was accomplished through 100-ns positive clock pulse.

The waveforms for the normal operation with a zero displacement angle value $\phi_i$ and modulation with $\phi_i = -\pi/4$ are shown in Fig. 18. The proposed modulation method can be used in the case of supply voltage asymmetry. Despite such conditions, the input currents in each phase are sinusoidal. Experimental results for a significant asymmetry of input voltages ($V_{i1} = 75$ V, $V_{i2} = 100$ V, and $V_{i3} = 125$ V) are shown in Fig. 19.

VI. CONCLUSION

The proposed computation scheme of PWM duty cycles did not require trigonometry operation and angles resulting in a
TABLE VII

| Comparison of the SVM and the Improved DAV-PWM |
|------------------------------------------------|
| maximum voltage transfer ratio $q$ if $\cos(\phi_i) = 1$ | SVM       | DAV-PWM |
| 0.866            |             | 0.866   |
| an input angle control | yes       | yes     |
| the $q$ dependency from the input angle $\phi_i$ | $q = \frac{0.866 \cdot \cos(\phi_i)}{0.866}$ | $q = \frac{0.866 \cdot \cos(\phi_i)}{0.866}$ |
| integrative functions in the formulas for the PWM duty cycles | yes | no |
| implementation in FPGA using HDL | difficult | simple |
| execution time of the PWM duty cycles | several hundred clock cycles | one clock |
| switch states table | switch state sequences are pre-selected and placed in the look-up table | tabularization of the switch state sequences is not needed |
| ready for hybrid modulation | no - this algorithm is hermetic and the modulation can not be modulated in the fly during the device is running | yes - it is enough to modify the reference voltage waveform |
| ready for multiphase output (3 or more terminals) | no - both, the optimal switch state sequences and the PWM duty cycles formulas must be elaborated again | yes - a new output phase is represented by the same communication cell, an only new double multiplexer block is required for the PWM duty cycles computing |
| PLL requirements | yes - for the indication of the output voltage excitors and also the input current sources | no - there is no PLL needed |

Fig. 19. An output and input currents for asymmetrical input voltage source for DAV-PWM modulation: $q = 0.55, \omega_o/\omega_i = 0.5$.

TABLE VIII

| Comparison of the Previous [26] and the Improved DAV-PWM Algorithms |
|-------------------------------------------------------------------|
| previous | present |
| maximum voltage transfer ratio $q$ if $\cos(\phi_i) = 1$ | 0.866 | 0.866 |
| an input angle control method | the reference voltage's trajectory T'slope | based on the input voltage rotation matrix $R$ |
| the extraction method of the quadrature components of the input voltages | the Clarke transformation on each natural a-b-c | using the DSOGH-OGS structure |
| the occurrence of program loops in the algorithm | yes - for selection of the best reference voltage trajectory position inside the synthesis blocks | no program loop |
| ready to use in DSP and processors only using the C-code | C-code and HDL-code allow the use in both, DSP and FPGA based application |
| shortening the calculation time | $\approx 90\%$ in DSP one-cycle operation in the FPGA device |

APPENDIX

(The Verilog HDL code of the improved DAV-PWM algorithm.)

module ImprovedDAVPWM (parameter MSB = 33, LSB = 18);

input iCLK, signed [15:0] vi1x, vi2x, vi3x, vi1y, vi2y, vi3y;
output reg[15:0] d11, d21, d31, d12, d22, d32, d13, d23, d33, sum;
output reg [2:0] si, so;

reg signed [16:0] vi1x_vo1x, vi2x_vo1x, vi3x_vo1x;
reg signed [16:0] vi1y_vo1y, vi2y_vo1y, vi3y_vo1y;
reg signed [16:0] vi1x-vi2x, vi2x-vi3x, vi3x-vi1x;
reg signed [16:0] vi1y-vi2y, vi2y-vi3y, vi3y-vi1y;
reg signed [15:0] vi1xx, vi2xx, vi3xx, vi1yy, vi2yy, vi3yy;
reg signed [33:0] d11w, d21w, d31w, d12w, d22w, d32w, d13w, d23w, d33w, d00w;
reg signed [33:0] d11ww, d21ww, d31ww, d12ww, d22ww, d32ww, d13ww, d23ww, d33ww, d00ww;

//behavioral description
reg signed [15:0] vxx, vyy;
reg signed [31:0] vxx, vxx2, vxx3, vxx4, vxx5, vxx6, vxx7, vxx8, vxx9, vxx10;
reg signed [15:0] vyy, vyy2, vyy3, vyy4, vyy5, vyy6, vyy7, vyy8, vyy9, vyy10;
reg signed [15:0] vxx2, vxx3, vxx4, vxx5, vxx6, vxx7, vxx8, vxx9, vxx10;
reg signed [33:0] d11w, d12w, d13w, d21w, d22w, d23w, d31w, d32w, d33w, d00w;
reg signed [33:0] d11ww, d12ww, d13ww, d21ww, d22ww, d23ww, d31ww, d32ww, d33ww, d00ww;

The discussed approach was suitable and more robust for FPGA implementation than a conventional approach such as SVM. For a better understanding of the solution developing process, this article also briefly described the HDL project.

simplistic matrix converter control algorithm. All calculation was based on basic arithmetic operations that can be easily implemented in the FPGA within one clock tact. The proposed general direct modulation was an SVM equivalent when the low-distortion eight-switch double-sided modulator was applied. However, compared with SVM, the proposed DAV-PWM algorithm was much simpler. The comparison of the SVM and the improved DAV-PWM was presented in Table VII. With regard to the solution presented in [26], the following benefits were obtained, as presented in Table VIII.

Moreover, an early functional simulation of the CMC control can be performed using the ModelSim software. Finally, the solution can be represented only by one Verilog HDL file; thus, an export to another FPGA vendor platform is not complicated, and it is not necessary to explicitly predefine the semiconductor switch states as in the SVM methods. Each converter cell is controlled independently in a direct way. This is especially convenient when the number of outputs is greater than the standard three. Simulation files are provided in the IEEE DataPort portal to increase understanding of this article. The first file is a script for the MATLAB environment, which is a presentation of the proposed modulation. The second file contains the testbench of the proposed Verilog HDL modulator [44].
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