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Influence of a SiN Drift-Barrier on the Charge Decay in Parylene-C Electret Layers

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Abstract. This paper reports on the attempt to improve the charge carrier lifetime in Parylene-C electret layers by implementing a drift barrier layer close to the surface. The barrier layer is intended to avoid the rapid discharge by ionic drift through the electret layer. For this purpose, we fabricated test chips comprising silicon nitride drift barriers with thicknesses of 50 nm, 100 nm and 200 nm sandwiched between a 7.1-µm-thick Parylene-C base layer and capping Parylene-C electret layers of three thicknesses, charged using the corona discharge method. Experimentally, it turns out that there is no pronounced influence on the charging process due to the drift barrier. Surface potential measurements were repeated over a period of 20 days. Up to \( t = 10 \) days a weak improvement of the remaining surface potential can be interpreted into the data. However, thereafter the surface potentials decrease rapidly. Surface potential line scans over the samples show that the decreased width of the charge carrier distribution, likely due to an enhanced horizontal drift or diffusion, is the reason. This effect is not observed on charged Parylene-C layers without drift barrier.

1. Introduction
Recently, the development of micro energy harvesting devices transducing ambient energy into the electrical domain has received much attention [1, 2, 3, 4, 5]. These devices need no costly maintenance and thus are suitable for deployment in wireless sensor nodes and in medical implants such as cardiac pacemakers. They can contribute to extend the battery lifetime and may even avoid the use of dedicated batteries at all.

Vibrational energy can be harvested by electrostatic transduction relying on charged electret materials [6]. An electret material is able to store charge carriers quasi-permanently [7]. The stability of implanted ionic charge carriers is mandatory to guarantee the long-term functionality of the device. Among other materials such as silicon oxide and nitride and polymers like Cytop and Teflon, Parylene-C has been considered as a promising electret material [8, 9, 10]. Previously, the charge decay in simple Parylene-C layers with thicknesses up to 23 µm has been investigated [11]. The highest charge carrier stability was achieved using 11-µm-thick samples charged at 100°C with a decay of 20% after 140 days. However, the charge decay with time has to be further reduced for this material to be suitable for micro energy harvesters. An attempt to use a drift barrier layer close to the electret surface is described in this work.
2. Theory

2.1. Electret Charging

Various techniques to charge electret materials are available [7]. One of them is the corona discharge method, whereby an inhomogeneous electrical field between a sharp needle tip and a planar electrode generates a discharge in air at atmospheric pressure. A negative potential between the needle tip and the planar electrode accelerates the dominantly generated CO$_3^-$ ions towards the electret layer covering the planar electrode where they are implanted close to the surface [7, 12]. A grid-shaped electrode between the needle tip and the planar electrode serves to control the implanted charge carrier density. As the surface potential of the electret layer rises, the potential difference against the applied grid potential and thus the accelerating force on the ions decreases until the charging process finally stops.

2.2. Discharging

The distribution of the stored charges decays due to several mechanisms [7]. Electret materials are non-ideal insulators and thus resistive losses occur depending on the presence of positive and negative intrinsic charge carriers available in the valence or conduction bands, respectively. Second, the implanted electrical charges build up an electrical field within the electret layer which lets the stored charges drift towards the planar electrode where they are neutralized. A third phenomenon is diffusion. The initially pronounced concentration gradient of the charge carriers implanted close to surface progressively smoothes out with time. Finally, compensation charges are attracted from the environment and cause a further charge decay. The discharging effect in Parylene-C predominant over longer times has been identified to be ionic drift [7]. The implanted ionic charge carriers drift through the electret layer with the drift velocity $v_D = \mu I E(x, t)$ with the mobility $\mu$ under the self-induced electrical field $E(x, t)$ depending on the momentary charge carrier distribution $\rho_1(x, t)$. Thus, implementing a drift barrier layer close to the surface is conjectured to be a suitable approach to impede the charge carrier movement through the complete layer. Materials with low ionic mobilities and high dielectric constant such as silicon nitride or other ceramics are promising candidates. The lower electrical field within the barrier layer is expected to result in even lower drift velocities.

3. Test Chip Fabrication

To test this hypothesis, test chips implementing a silicon nitride (SiN) barrier layer were prepared. The test chips, schematically shown in Figure 1, were fabricated using four-inch Pyrex substrates with a thickness of 500 µm covered by a bottom electrode consisting of 20 nm of Cr, 300 nm of Au and 40 nm of Cr. Next, a Parylene-C layer with the thickness $d = 7.1 \pm 0.5$ µm is

![Figure 1](image1)

**Figure 1.** Schematic drawing of a cross-section of the test chip showing the composition of the stacked materials.

![Figure 2](image2)

**Figure 2.** Photograph of two fabricated test chips for the characterization of the charge stability.
deposited in a Labcoter 2 from SCS Coatings at a pressure of 22 mTorr. Then, SiN playing the role of a drift barrier is deposited by PECVD with thicknesses $d_{\text{SiN}}$ of 50 nm, 100 nm and 200 nm. In view of the wafer-to-wafer Parylene-C layer thickness variation, SiN is etched back on one half of each wafer using reactive ion etching (RIE) to obtain test chips with and without barrier layer on each wafer with matching Parylene-C thickness. Subsequently, capping Parylene-C layers with thicknesses $d_{\text{P}} = 0.3 \mu m$, $0.6 \mu m$ and $1.2 \mu m$ are deposited. The layer stack is structured using RIE to $8 \times 8 \text{ mm}^2$ squares. The exposed Cr layer is removed completely and the remaining Au and Cr layers are removed by wet etching except for a contact frame along the chip edges. Finally, the wafer is diced into $11.5 \times 11.5 \text{ mm}^2$ large chips as shown in Figure 2.

4. Experimental

4.1. Test Chip Charging

The fabricated test chips were charged using the custom-made corona discharge setup shown in Figure 3. The high potentials are generated by the two high-voltage sources LNC-10000-2 neg and LNC 1200-20 neg from Heinzinger, Germany. The potential $U_{\text{Needle}} = -8 \text{ kV}$ is applied between the sharp needle tip and the grounded electrode at the bottom of the electret layer on the test chip. At the same time the potential $U_{\text{Grid}}$ is applied to the grid-shaped electrode. For the experiments $U_{\text{Grid}}$ values ranging from $-200 \text{ V}$ to $-1000 \text{ V}$ in steps of 200 V and a charging duration of 3 min at room temperature (RT) were chosen.

4.2. Surface Potential Measurements

The measurement of the surface potential $U_S$ was first carried out directly after the charging process and repeated after increasing time spans. For this purpose the electrostatic voltmeter Isoprobe 279 from Monroe Electronics is used. The circular measurement spot of the probe has a diameter of $500 \mu m$. Thus, the measured value corresponds to an average within this area. As shown in Figure 4, the voltmeter probe is mounted above a chip carrier able to handle up to 16 chips at once. Using two LabView-controlled linear stages the voltmeter probe scans the electret surface with a horizontal step size of $200 \mu m$ to map the surface potential.

5. Results

5.1. Dependency of $U_S$ on $U_{\text{Grid}}$

To observe the influence of the drift barrier layer on the charging and discharging process the measured surface potential $U_S$ is repeatedly compared to identically charged test chips without drift barrier. In Figure 5 the dependency of the initial surface potential value, $U_{S,\text{initial}}$, on the
grid potential $U_{\text{Grid}}$ is shown for test chips with a $d_p = 0.3 \mu m$ thick capping Parylene-C layer and for the different $d_{\text{SiN}}$ values. No significant differences among three drift barrier thicknesses and the sample without drift barrier can be observed. Calculating the mean $U_{S,\text{initial}}$ for each $U_{\text{Grid}}$ value among all charged test chips and linearly fitting the dependency of $U_{S,\text{initial}}$ versus $U_{\text{Grid}}$ results in a slope of 683 V/kV and a standard deviation among the samples of 23.8 V. These results are in agreement with the charging behavior of test chips with pure Parylene-C electret layers [11]. Charging of the test chips with different $d_p$ values resulted in similar dependencies.

5.2. Influence of the Drift Barrier on the Charge Decay

The measurement of the surface potential $U_S$ was repeated over a time span of 20 days. In Figure 6, the discharging behavior for test chips charged at $U_{\text{Grid}} = -1000$ V at RT with a capping Parylene-C thickness $d_p = 0.3 \mu m$ and drift barrier thicknesses of 50 nm, 100 nm and 200 nm are shown exemplarily. Except for one measurement point, all chips seem to discharge at roughly the same rate for times below $t = 0.03$ days. This similar behavior is likely due to the thickness of the capping Parylene-C layer which has to be traversed and has the same thickness for all shown test chips. Later, the discharging curves spread. At $t = 10$ days, the test chips with SiN drift barriers show remaining surface potentials $U_S$ increased slightly by

![Figure 5](image_url)  
**Figure 5.** Measured initial surface potential $U_{S,\text{initial}}$ as a function of the grid potential $U_{\text{Grid}}$ for 7.1-µm-thick Parylene-C with different barrier thicknesses charged at RT.

![Figure 6](image_url)  
**Figure 6.** Measured maximum surface potential $U_S$ for samples without and with SiN thicknesses of 50 nm, 100 nm and 200 nm charged at RT at different time spans.

![Figure 7](image_url)  
**Figure 7.** Measured surface potential $U_S$ scanned over the electret layer on the test chips (a) with and (b) without SiN barrier at seven increasingly spaced times. The lateral extent of the charged electret is indicated by the dashed vertical lines.
5.2% ($d_{\text{SiN}} = 50 \text{ nm}$), 5.3% ($d_{\text{SiN}} = 100 \text{ nm}$) and 11.3% ($d_{\text{SiN}} = 200 \text{ nm}$) over those of the corresponding reference test chips without barriers. In the period between 11 days and 20 days, the surface potential of the sample with the 100 nm barrier begins to drop rapidly, reducing the remaining $U_S$ below that of the reference sample. This behavior was observed for other thicknesses $d_P$ and $d_{\text{SiN}}$, too. Among the reference test chips differences in discharging rates are observed as well. These are compatible with wafer-to-wafer thickness variations known to lead to different discharging rates [11]. Nevertheless, test chips with barrier and the corresponding references have the same Parylene-C thickness and can thus be directly compared.

Figure 7 (a) shows scans of the surface potential $U_S$ of a chip with a 50 nm barrier. Results at different times are shown. The potential profile is observed to progressively narrow with time. After $t = 20 \text{ days}$ the effective width of the profile has decreased to significantly below 4 mm. This behavior was observed for all test chips with a SiN drift barrier. In contrast, the width of the charge carrier profile of barrier-free reference test chips, as shown in Figure 7 (b), remains constant over time. We conjecture that the drift barrier offers a new, horizontal discharging path parallel to the electret.

6. Conclusion

In this work an approach to reduce the charge carrier decay in Parylene-C electret layers using SiN drift barriers was investigated. Test chips with different drift barrier thicknesses and different thicknesses of the capping Parylene-C layer were fabricated, charged and the surface potential $U_S$ was measured repeatedly. The drift barrier does not affect the charging process and $U_{S,\text{initial}}$ values are in agreement with those achieved for pure Parylene-C layers [11]. Comparing the discharging behavior of test chips with and without drift barrier, SiN layers as barrier provide a slightly higher stability of the charge carriers for short times. However, a horizontal discharge mechanism ruins this effect and decreases the long term stability dramatically.

Acknowledgments

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