Neuromorphic Processing: A Unifying Tutorial

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Abstract
All systolic or distributed neuromorphic architectures require power efficient processing nodes. In this paper, a unifying tutorial is presented which implements multiple neuromorphic processing elements using a systematic analog approach including synapse, neuron and astrocyte models. It is shown that the proposed approach can successfully synthesize multidimensional dynamical systems into analog circuitry with minimum effort.

1 Introduction
Given the application of the neuromorphic circuits, different approaches have been devised so far to mimic the biological behavior of the nervous system including special purpose computing architectures [1–5], digital [6–15], and analog platforms [16–24]. Although all these approaches have their own merits and purposes, the interest upon mimicking biological behavior in their natural form (analog) has always been pursued rigorously by researchers.

To this end, in this paper we apply a novel approach introduced in [25] to systematically synthesize different neuromorphic processing elements into CMOS circuitry operating in strong–inversion. Same approach has been applied to log–domain circuits presented in [16] with the purpose of achieving ultra–low power circuitry at the expense of slower time scales. In this tutorial, the application of the method is verified by synthesizing three different neuromorphic processing elements including synapse, neuron, and astrocyte models.

2 Method
In this section, the novel approach proposed in [25] is described which supports a systematic realization procedure of strong–inversion circuits capable of computing bilateral dynamical systems at higher speed compared to the previously proposed log–domain circuit [16]. The current relationship of an NMOS and PMOS transistor operating in strong–inversion saturation when $|V_{DS}| > |V_{GS} - V_{th}|$ can be expressed as follows:

\[ I_{Dn} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_n (V_{GS} - V_{th})^2 \]  
\[ I_{Dp} = \frac{1}{2} \mu_p C_{ox} \left( \frac{W}{L} \right)_p (V_{SG} - V_{th})^2 \]

where $\mu_n$ and $\mu_p$ are the charge–carrier effective mobility for NMOS and PMOS transistors, respectively; $W$ is the gate width, $L$ is the gate length, $C_{ox}$ is the gate oxide capacitance per unit area and $V_{th}$ is the threshold voltage of the device.

Setting $k_n = \frac{1}{2} \mu_n C_{ox} (\frac{W}{L})_n$ and $k_p = \frac{1}{2} \mu_p C_{ox} (\frac{W}{L})_p$ in (1) and (2) and differentiating with respect to time, the current expression for $I_A$ (see Figure [1]) yields:

\[ \dot{I}_A = \sqrt{k_n I_A} \dot{V}_{GS1} \]  
\[ \dot{I}_A = \sqrt{k_p I_A} \dot{V}_{SG2} \]  

(3) and (4) are equal, therefore:

\[ \dot{V}_{SG2} = \sqrt{\frac{k_n}{k_p}} \dot{V}_{GS1} = \beta \dot{V}_{GS1} \]  

(5)
Figure 1: The “main core” including the initialization circuit highlighted with red color.

Figure 2: (a) The “main block” including the main core and two current–mode root square blocks and a bilateral multiplier. (b) The final high speed circuit including the “main block” with several copied currents (the current mirrors are represented with double circle symbols)

where $\beta = \sqrt{\frac{k_n}{k_p}}$. Similarly, we can derive the following equation for transistors $M_3$ and $M_4$:

$$V_{SG_4} = \sqrt{\frac{k_n}{k_p}} V_{GS_3} = \beta V_{GS_3}. \quad (6)$$

The application of Kirchhoff’s Voltage Law (KVL) and applying the derivative function show the following relations:

$$\dot{V}_C = -(\dot{V}_{GS_1} + \dot{V}_{SG_2}) \quad (7)$$

$$\dot{V}_C = + (\dot{V}_{GS_3} + \dot{V}_{SG_4}) \quad (8)$$

where $V_C$ is the capacitor voltage and $V_b$ the bias voltage which is constant (see Figure 1). Substituting (5) and (6) into (7) and (8) respectively yields:

$$\dot{V}_C = -\dot{V}_{GS_1} \cdot (1 + \beta) \quad (9)$$

$$\dot{V}_C = +\dot{V}_{GS_3} \cdot (1 + \beta). \quad (10)$$

Setting the current $I_{out} = I_B - I_A$ in Figure 1 as the state variable of our system and using (3) and the corresponding equation for $I_B$, the following relation is derived:

$$\dot{I}_{out} = \dot{I}_B - \dot{I}_A = 2\sqrt{k_n I_B \dot{V}_{GS_3}} - 2\sqrt{k_p I_A \dot{V}_{GS_1}} \quad (11)$$
Figure 3: A block representation of the total circuit implementing the synapse model.

by substituting (9) and (10) in (11):

$$I_{out} = (\sqrt{I_A} + \sqrt{I_B}) \cdot \frac{2\sqrt{k_n}V_C}{2 + \beta}. \quad (12)$$

Bearing in mind that the capacitor current $I_{Cin}$ can be expressed as $CV_C$, relation (12) yields:

$$I_{out} = (\sqrt{I_A} + \sqrt{I_B}) \cdot \frac{2\sqrt{k_n}I_{Cin}}{(2 + \beta)C}. \quad (13)$$

One can show that:

$$\frac{(2 + \beta)C}{2\sqrt{k_n} \cdot I_{dc}} I_{out} = (\sqrt{I_A} + \sqrt{I_B}) \cdot I_{Cin}. \quad (14)$$

Equation (14) is the main core’s relation. In order for a high speed mathematical dynamical system with the following general form to be mapped to (14):

$$\tau I_{out} = F(I_{out}, I_{ext}) \quad (15)$$

where $I_{ext}$ and $I_{out}$ are the external and state variable currents, the quantities $\frac{C}{I_{dc}}$ and $I_{Cin}$ must be respectively equal to $\frac{2\sqrt{k_n}}{(2 + \beta)}$ and $\frac{F(I_{out}, I_{ext})}{\sqrt{I_A + \sqrt{I_B}}}$. Note that the ratio value $\frac{C}{I_{dc}}$ can be satisfied with different individual values for $C$ and $I_{dc}$. These values should be chosen appropriately according to practical considerations (see Section V.G). Since $F$ is a bilateral function, in general, it will hold:

$$I_{Cin}^+ = \frac{F^+(I_A, I_B, I_{ext}, I_{out})I_{dc}}{\sqrt{I_A + \sqrt{I_B}}} = \frac{I_{Cin}^-}{\sqrt{I_A + \sqrt{I_B}}} \quad (16)$$

where $I_{Cin}^+$ and $I_{Cin}^-$ are calculated respectively by a root square block (see Figure 2(a)) and $I_{ext}$ is separated to + and – signals by means of splitter blocks. Note that $I_{dc}$ is a scaling dc current and $\tau$ has dimensions of second(s). Since $I_{Cin}$ can be a complicated nonlinear function in dynamical systems, we need to provide copies of $I_{out}$ or equivalently of $I_A$ and $I_B$ to simplify the systematic computation at the circuit level. Therefore, the higher hierarchical block shown in Figure 2(b) is defined as the NBDS (Nonlinear Bilateral Dynamical System) circuit (16) (see Figure 2(b)) including the main block and associated current mirrors. The form of (15) is extracted for a 1–D dynamical system and can be extended to $N$ dimensions in a straightforward manner as follows:

$$\tau_N I_{out,N} = F_N(I_{out}, I_{ext}) \quad (17)$$

where $\frac{C_n}{I_{dc,N}} = \frac{2\sqrt{k_n}}{(2 + \beta)}$ and $I_{Cin,N} = \frac{F_N(I_{out}, I_{ext})I_{dc,N}}{\sqrt{I_{A,N} + \sqrt{I_{B,N}}}}$.

To realized the full potential of (14) and implement the aforementioned neuromorphic processing elements, some circuit blocks are required to perform basic operations including multiplication and division. The full description of these blocks can be found in [25]; however, in this paper we only employ them to implement the following case studies. In the following sections, multiple neuromorphic processing elements are implemented in which the feasibility of the above method is shown.
2.1 Synapse model

Synapses can be represented as low pass filters as the conductance and the capacitance of the post–synaptic cell are connected in parallel, forming a circuit in which the membrane’s capacitance takes time to charge. Therefore they function as low-pass filters attenuating the high frequency components of a pre–synaptic signals. The filtering characteristics including the time scale of a synapse can vary depending upon the membrane properties of the post-synaptic cell. Low pass filters can be generally represented as:

$$\tau \dot{s} = -s + I_{ext}$$  \hspace{1cm} (18)

where $\tau$ defines the response time scale of the synapse. We can start forming the electrical equivalent using [17]:

$$\left\{ \begin{array}{l}
\frac{(2+\beta)C}{2\sqrt{k_w}I_{dcw}} \dot{i}_{out_s} = F_s(i_{out_s}, I_{ext})
\end{array} \right.$$  \hspace{1cm} (19)

where $I_{dc} = I_{dcw}$, $F_s$ is function given by:

$$F_s(i_{out_s}, I_{ext}) = -i_{out_s} + I_{ext}$$  \hspace{1cm} (20)

It should be noted that the appropriate size of the capacitor $C$ can be defined based on the relative time scale of the model and $I_{dc}$. It was shown in [16] that there are some trade-offs between the size of the capacitor and $I_{dc}$, in terms of power, area and noise performance. Schematic diagrams for the synapse model is seen in Figure 3 including the symbolic representation of the basic electrical blocks introduced in [25]. According to these diagrams, it is observed how the mathematical model is mapped onto the proposed electrical circuit. The schematic contains only one NBDS circuit implementing the only dynamical variable and the necessary connections. As shown in the figure, according to the synapse model parameter, proper bias currents are selected and the correspondence between the biological voltage and electrical current is $V \iff \mu A$.

2.2 Neuron model

In this section, the application of the method is demonstrated by synthesizing the 2–D nonlinear FitzHugh–Nagumo neuron model. In the FHN neuron model [26] with the following representation:

$$\begin{align*}
\dot{v} &= v - \frac{v^3}{3} - w + I_{ext} \\
\dot{w} &= 0.18(v + 0.7 - 0.8w)
\end{align*}$$  \hspace{1cm} (21)

(describing the membrane potential’s and the recovery variable’s velocity. According to this biological dynamical system, we can start forming the electrical equivalent using [17]:

$$\left\{ \begin{array}{l}
\frac{(2+\beta)C}{2\sqrt{k_w}I_{dcw}} \dot{i}_{out_v} = F_v(i_{out_v}, i_{out_w}, I_{ext}) \\
\frac{(2+\beta)C}{2\sqrt{k_w}I_{dcw}} \dot{i}_{out_w} = F_w(i_{out_v}, i_{out_w})
\end{array} \right.$$  \hspace{1cm} (22)
where $\tau_v = 0.18\tau_w$, and $I_{dc_v} = 0.18I_{dc_w}$, $F_v$ and $F_w$ are functions given by:

$$
\begin{align*}
F_v(I_{out_v}, I_{out_w}, I_{ext}) &= I_{out_v} - \frac{I_{out_v}^2}{I_{ext} + I_{out_v}} - I_{out_w} + I_{ext} \\
F_w(I_{out_v}, I_{out_w}) &= (I_{out_v} + I_c - \frac{I_{out_w}}{I_{out_v}}).
\end{align*}
$$

(23)

It should be noted that the appropriate size of the capacitor $C$ can be defined based on the relative time scale of the model. Schematic diagrams for the FHN neuron model is seen in Figure 1 including the symbolic representation of the basic blocks introduced in [25]. According to these diagrams, it is observed how the dynamical functions. As shown in the figure, proper bias currents are selected implementing the two dynamical variables, followed by two MULT blocks and current mirrors realizing the electrical circuit. The schematic contains two NBDS circuits where $m$, $n$, and $p$ define the Hill coefficients, different degrees of cooperativity can be achieved. There are three different cases of Hill coefficients $(m = n = p = 1, m = n = p = 2)$ and $(m = n = 2, p = 4)$ which in this paper we only explore the $m = n = p = 1$ case and leave the rest to the interested readers. The electrical equivalent can be represented.

2.3 Astrocyte model

Astrocytes are part of the biological neural network that outnumber neurons by over a factor of five in the brain. They occur in the entire central nervous system (CNS) and perform many essential complex functions in the healthy CNS [27]. A reduced and an extended model, which accurately and efficiently describe $Ca^{2+}$ oscillations was presented in [28]. Relying on the fact that the amount of $Ca^{2+}$ released is controlled by the level of stimulus through modulation of the $IP_3$ level and by making the simplification that the level of stimulus-induced, $IP_3$-mediated $Ca^{2+}$ is a model parameter, the following 2-D model was presented:

$$
\begin{align*}
\dot{X} &= z_0 + z_1 \beta + z_2(X) + z_3(X, Y) + k_f Y - kX \\
\dot{Y} &= z_2(X) - z_3(X, Y) - k_f Y
\end{align*}
$$

(24)

where

$$
\begin{align*}
&z_2(X) = V_{M_2} \frac{X^n}{K_2^n + X^n} \\
&z_3(X, Y) = V_{M_3} \frac{X^m}{K_A^m + X^m}\frac{Y^p}{K_R^p + Y^p}
\end{align*}
$$

(25)

The parameters $V_{M_2}$, $V_{M_3}$, $K_2$, $K_R$, $K_A$, $k_f$ and $k$ are the maximum values of $z_2$ and $z_3$, threshold constants for pumping, release and activation and rate constants, respectively. Parameters $n$, $m$, and $p$ define the Hill coefficients characterizing the pumping, release and activation processes, respectively. Depending on the values of the Hill coefficients, different degrees of cooperativity can be achieved. There are three different cases of Hill coefficients $(m = n = p = 1, m = n = p = 2$ and $m = n = 2, p = 4)$ which in this paper we only explore the $m = n = p = 1$ case and leave the rest to the interested readers. The electrical equivalent can be represented.
as follows:

$$\begin{align*}
\begin{bmatrix}
\frac{(2+z)}{2\sqrt{z}}C
\frac{2+z}{2\sqrt{z}}C
\end{bmatrix}
\begin{bmatrix}
I_{outX}
\end{bmatrix}
= F_X(I_{outX}, I_{outY}, I_{ext})

\begin{bmatrix}
\frac{2+z}{2\sqrt{z}}C
\frac{2+z}{2\sqrt{z}}C
\end{bmatrix}
\begin{bmatrix}
I_{outY}
\end{bmatrix}
= F_Y(I_{outX}, I_{outY})
\end{align*}$$

(26)

where \( I_{ext} = z_0 + z_1 \beta \), \( F_X \) and \( F_Y \) are functions given by:

$$\begin{align*}
F_X(I_{outX}, I_{outY}, I_{ext}) &= \frac{I_{V Maint}_{outX}}{I_{R X} + I_{outX}} + \frac{I_{V Maint}_{outY}}{I_{R Y} + I_{outY}} - k I_{outX} + k f I_{outY} + I_{ext} \\
F_Y(I_{outX}, I_{outY}) &= \frac{I_{V Maint}_{outX}}{I_{R X} + I_{outX}} - \frac{I_{V Maint}_{outY}}{I_{R Y} + I_{outY}} - k f I_{outY}.
\end{align*}$$

(27)

It should be noted that the appropriate size of the capacitor \( C \) can be defined based on the relative time scale of the model. Schematic diagrams for the Astrocyte \( Ca^{2+} \) oscillations model is seen in Figure 5 including the symbolic representation of the basic blocks introduced in [25]. According to these diagrams, it is observed how the mathematical model is mapped onto the proposed electrical circuit. The schematic contains two NBDS circuits implementing the two dynamical variables, followed by three MULT blocks and current mirrors realizing the dynamical functions. As shown in the figure, according to the neuron model, proper bias currents are selected and the correspondence between the biological voltage and electrical current is \( V \Leftrightarrow uA \).

3 Discussion

In this paper, we demonstrated a unifying tutorial which synthesizes biological neuromorphic models into analog circuitry with the minimum effort. The validity of the approach was shown by implementing multiple neuromorphic processing elements including synapse, neuron and astrocyte models. As mentioned above there are multiple design trade-off aspects (including but not limited to the capacitor sizes and bias currents (\( I_{dc} \)) that interested readers should be aware of in order to design a power efficient circuitry.

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