A New SVPWM Strategy for Three-Phase Isolated Converter with Current Ripple Reduction

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Abstract: Three-phase isolated matrix converters enable bidirectional power conversion and galvanic isolation, and they are suitable for widespread applications in industry. However, excessive DC-link current ripple not only increases the inductor loss and switching loss but also causes more electromagnetic interference and grid current distortion. Traditionally, increasing DC-link inductance or switching frequency can reduce the current ripple to a certain extent, but it is not cost-effective due to the bulky size of the inductor and higher switching losses. To address the above issue, optimizing the modulation control strategy is more attractive. This paper proposes a new SVPWM strategy to reduce the current ripple. First, the inherent limitation of the conventional modulation scheme is revealed. Then, the new optimal modulation scheme is proposed for the isolated matrix converters to reduce the current ripple without increasing the DC-link inductor or switching frequency. Moreover, the power density of the system is effectively increased. Finally, simulation in a MATLAB environment and a laboratory prototype of the isolated matrix converter have been built to verify the effectiveness of the proposed strategy.

Keywords: three-phase isolated matrix converter; optimal SVPWM modulation; current ripple; power density

1. Introduction

With the development of power electronic technology, the requirements for power electronic conversion circuits are constantly increasing. Power converters are widely used in the applications of electric vehicle charging [1], photovoltaic systems [2,3], HVDC systems, and flexible ac transmission systems (FACTS) [4]. From the perspective of safety and reliability, it is usually required that the converter has the function of galvanic isolation. Therefore, the three-phase isolated matrix converters with a high-frequency transformer (HFT) have drawn lots of attention due to their superior performance, such as power factor correction [5–7], high power density, and low harmonic current distortion [8,9]. Therefore, three-phase isolated matrix converters have broad applications in the fields of electric vehicles, photovoltaic power generation systems, grid-connected converters [10], micro grids [11,12], fuel cell power systems, and battery chargers [13].

For three-phase isolated matrix converter circuits, the DC-link current ripple is one of the most important issues. Excessive DC-link current ripple not only increases the inductor loss and switching loss but also causes more electromagnetic interference and grid current distortion. In practice, the DC-link current ripple can be reduced by increasing the switching frequency or increasing the inductor size of the output filter [14]. However, a higher switching frequency will result in higher switching losses, and a larger output inductor will increase the size and cost of the converter. At present, there are several methods based on the SVPWM algorithm that can reduce dc ripple [15–17]. Additionally, therefore, optimizing the modulation control strategy is more attractive to address the above issue.
To deal with the problems caused by the DC-link current ripple, a method by setting the zero vector in a smart way is proposed for a three-phase converter in [16]. Though this method can reduce the current ripple, it suffers high switching losses due to the increasing switching actions. Another way is presented in [18,19] for the Z-source converter to reduce the DC-link current ripple, which is implemented by selecting the vectors and adjusting shoot-through time. In this way, the inductor current changes alternately in each switching cycle, which effectively suppresses the DC-link current ripple.

For a back-to-back current-source converter, another interesting solution is presented in [20] by coordinating the gating sequences of both the rectifier and inverter to reduce the current ripple. The idea is interesting, but it is only effective for the back-to-back current-source converters, which blocks its application.

The duty cycle loss and output current ripple of two different PWM schemes had been further studied and discussed in [21]. The proposed “six-segment” PWM scheme has the characteristics of small output current ripple and low duty cycle loss, which means that a smaller output inductance can be used. Besides, an optimized PWM scheme is proposed to reduce the current ripple in [22]. In addition, the proposed six-segment PWM scheme has lower switching loss and lower duty cycle loss, as well as a low THD with duty-cycle compensation.

In this paper, an optimized modulation control strategy for the three-phase isolated matrix converters is proposed to effectively reduce the DC-link current ripple. Moreover, the proposed scheme features potential benefits to increase power density. The rest of this paper is organized as below: in Section 2, the inherent limitation of the conventional modulation scheme is revealed. Then, in Section 3, the new optimal modulation scheme is proposed for the isolated matrix converters to reduce the current ripple by the optimal arrangement of vector sequences. Following that, the simulation and experiment results for three-phase isolated matrix converters are given to compare the performance of different SVPWM strategies in Sections 4 and 5. Finally, conclusions are drawn in Section 6.

2. DC-Link Current Ripple Analysis

2.1. System Configuration and Working Principle

The topology of the three-phase isolated matrix converter is shown in Figure 1. The converter contains a matrix converter (MC), high-frequency transformer (HFT), and uncontrolled rectifier bridge. The MC is composed of six bidirectional switches, which can realize bidirectional current flow. The HFT connects the MC and the uncontrolled rectifier bridge, which play the roles of electrical isolation and energy transfer. The diodes of the uncontrolled rectifier bridge can be replaced with controllable switches to achieve bi-directional power flow. The LC filter is used to filter high-frequency harmonics of the grid current. The inductor L and the capacitor C form an LC filter on the DC side.

![Figure 1](image-url). The schematic diagram of three-phase isolated matrix converter.
From Figure 1, the structure of the grid side MC is equivalent to a conventional current source rectifier, except that the MC uses the bidirectional switches, and therefore, the conventional SVPWM can be adopted to control this converter [23]. In general, the reference vector \( \vec{I}_{\text{ref}} \) is synthesized by two adjacent active vectors \( \vec{I}_x \), \( \vec{I}_y \) and one zero vector \( \vec{I}_0 \) (here \( \vec{I}_x = \vec{I}_1, \vec{I}_y = \vec{I}_2 \) as shown in Figure 2). In order to maintain the flux balanced in HFT [24], the average voltage vector over a switching cycle is zero. Therefore, the switching vectors should produce an alternating positive and negative primary voltage of the HFT. Consequently, two switching states depending on the direction of the primary side current \( I_p \) for each vector are required to correspond to the positive and negative current vector, respectively. The current space vector distribution in the two cases of \( I_p > 0 \) and \( I_p < 0 \) is shown in Figure 2, and the switching state and the corresponding output voltage are listed in Table 1.

![Figure 2. Current space vector. (a) \( I_p > 0 \) (b) \( I_p < 0 \).](image)

| Space Vector | Switch State | Output Voltage |
|--------------|--------------|----------------|
| \( I_1/14 \) | \( S_1 \) 1 0 0 1 0 0 | \( U_{AB} \) |
| \( I_2/15 \) | \( S_4 \) 1 0 0 0 0 1 | \( U_{AC} \) |
| \( I_3/16 \) | \( S_3 \) 0 0 1 0 1 0 | \( U_{BC} \) |
| \( I_4/11 \) | \( S_6 \) 0 1 1 0 0 0 | \( U_{BA} \) |
| \( I_5/12 \) | \( S_5 \) 0 1 0 0 1 0 | \( U_{CA} \) |
| \( I_6/13 \) | \( S_2 \) 0 0 0 0 1 1 | \( U_{CB} \) |
| \( I_7 \) | 1 1 0 0 0 0 | 0 |
| \( I_8 \) | 0 0 0 0 1 1 | 0 |
| \( I_9 \) | 0 0 0 1 1 0 | 0 |

2.2. DC-Link Current Ripple Analysis of Traditional Scheme

According to the formula \( U_L = L \left( \frac{di}{dt} \right) \), the expression of DC-link inductor current ripple can be expressed as:

\[
\Delta i = \frac{U_L}{L} \Delta t = \frac{U_{dc} - U_o}{L} \Delta t
\]

where \( U_{dc} \) is the bridge output voltage, \( U_o \) is the output voltage, and \( \Delta t \) is the charging/discharging time of inductor current.

From (1), it can be observed that the DC-link current ripple depends on the variable of \( U_{dc} \), which is associated with the switching states of the MC. Therefore, the inductor current ripple can be optimized through the above formula.

Take Sector I for example: \( \vec{I}_{\text{ref}} \) can be represented by \( \vec{I}_1, \vec{I}_2, \) and \( \vec{I}_0 \), as shown in Figure 3.
According to the ampere-balance principle in (2), the dwell times for three vectors can be obtained as (3)

\[ T_x = T_1 = m_a T_s \sin(\frac{\pi}{6} - \theta) \]
\[ T_y = T_2 = m_a T_s \sin(\frac{\pi}{6} + \theta) \]
\[ T_0 = T_s - T_1 - T_2 \]

where \( T_s \) is the sampling period, \( m_a \) is the modulation index, and \( \theta \) denotes the vector angle \((-\frac{\pi}{6} \leq \theta \leq \frac{\pi}{6})

The different vector sequence arrangements are well described in [22]. For the analysis in this paper, in order to avoid magnetic saturation caused by dc component, the transformer of the current mode matrix converter should ensure that the current with equal size and opposite phase passes through the primary side of the transformer in one cycle. In the positive half-cycle, \( I_1 \) and \( I_2 \) act, and the primary side output voltage of the transformer is \( V_{AB} \) and \( V_{AC} \), respectively. In order to ensure that in the negative half-cycle, the action time of \( I_4 \) is the same as \( I_1 \), and the action time of \( I_5 \) is the same as \( I_2 \), the primary side voltage of the transformer is \( V_{BA} \) and \( V_{CA} \), respectively. The traditional six-segment SVPWM scheme with a step change in the primary voltage of the HFT from a higher voltage amplitude to a lower one (HTL) is adopted. The output voltage of the primary side of the transformer and the corresponding switching states are shown in Figure 4.

According to the above analysis, when the reference vector is located in Sector 1, the time-domain expression of DC-link current ripple can be calculated as (4).

\[
\begin{align*}
\Delta I_{L1} &= \frac{U_o - U_i}{L} T_1 \frac{T_s}{2} = \frac{U_o \cos(\frac{\pi}{6} + \theta) - U_i}{L} mT \sin\left(\frac{\pi}{6} - \theta\right) \\
\Delta I_{L2} &= \frac{U_o - U_i}{L} T_2 \frac{T_s}{2} = \frac{U_o \cos\left(\frac{\pi}{6} - \theta\right) - U_i}{L} mT \sin\left(\theta + \frac{\pi}{6}\right) \\
\Delta I_{L3} &= 0 - \frac{U_o}{L} T_0 \frac{T_s}{2} = -\frac{U_o}{L} T - T_1 - T_2 
\end{align*}
\]

From (4), the increasing/decreasing trend of the current ripple can be drawn in Figure 5a, where the traditional scheme is used, and this methodology is highlighted on page 4. Note that (4) is monotonic, and the peak-peak value of the DC-link current ripple is determined by \( \Delta I_{L3} \), which can be defined as

\[ \Delta I_{L_m} = \left| \frac{U_o}{L} \frac{2T - \sqrt{3}mT}{4} \right| \]
Figure 4. Waveforms of the transformer primary voltage and switching states.

Figure 5. Waveforms of the inductor current ripple. (a) Traditional scheme (b) Proposed scheme.

As shown in the previous analysis, the current ripple of the traditional six-segment SVPWM scheme with HTL is not optimized.

3. Proposed Solution

As shown in the previous section, it is hard to reduce the DC-link current ripple with conventional SVPWM by synthesizing the reference vector with two adjacent active vectors \( \vec{I}_x, \vec{I}_y \), and one zero vector. In order to reduce the DC-link current ripple effectively, the space vector is divided into 12 sectors, as shown in Figure 6. In this section, an optimal scheme is proposed by employing six non-nearest vectors in each sector to synthesize the reference vector to solve the above problem.
Table 2 shows the current vectors, switching sequence, and the corresponding primary side voltage of the HFT. It indicates that the primary side voltage is determined by the current vectors and line voltage. Figure 7 shows the relationship of the bridge output voltage $U_{dc}$, the amplitude of line–line voltage $V_i$, and the vector angle $\theta$ of the reference vector. From Figure 7, the line–line voltage in each sector is monotonic. From (1), the DC-link current ripple $\Delta i$ can be optimized depending on the bridge output voltage $U_{dc}$, which is determined by the switching states, as shown in Table 2; that is, the DC-link current ripple would be high if $U_{dc}$ steps from the highest to lowest one depending on the vector sequence.

Table 2. The corresponding switching sequence and the output voltage.

| Vector | Switches | Line Voltage | Vector | Switches | Line Voltage |
|--------|----------|--------------|--------|----------|--------------|
| $I_1$  | $(S_{11},S_{21})(S_{16},S_{26})$ | $U_{ab}$  | $I_1$  | $(S_{13},S_{23})(S_{14},S_{24})$ | $-U_{ab}$  |
| $I_2$  | $(S_{11},S_{21})(S_{12},S_{22})$ | $U_{ac}$  | $I_2$  | $(S_{14},S_{24})(S_{15},S_{25})$ | $-U_{ac}$  |
| $I_3$  | $(S_{12},S_{22})(S_{13},S_{23})$ | $U_{bc}$  | $I_3$  | $(S_{15},S_{25})(S_{16},S_{26})$ | $-U_{bc}$  |
| $I_4$  | $(S_{13},S_{23})(S_{14},S_{24})$ | $-U_{ab}$ | $I_4$  | $(S_{11},S_{21})(S_{16},S_{26})$ | $U_{ab}$   |
| $I_5$  | $(S_{14},S_{24})(S_{15},S_{25})$ | $-U_{ac}$ | $I_5$  | $(S_{11},S_{21})(S_{12},S_{22})$ | $U_{ac}$   |
| $I_6$  | $(S_{15},S_{25})(S_{16},S_{26})$ | $-U_{bc}$ | $I_6$  | $(S_{12},S_{22})(S_{13},S_{23})$ | $U_{bc}$   |

Figure 6. New current space vector diagram.

Figure 7. Line voltage and sector division.
Taking the range of $-30^\circ$ to $30^\circ$ as an example, and assuming that the current reference is located in sector 1, which is shown in Figure 8, the DC-link current ripple would be decided by the vector sequence. The vector sequence of the traditional modulation scheme is $I_1 \rightarrow I_2 \rightarrow I_0$, and the corresponding $U_{dc}$ would be $V_{ab}$, $V_{ac}$, 0 and $V_{ac} > V_{ab} > 0$; consequently, the high current ripple would be caused by $U_{dc}$ steps from the highest line-line voltage to 0 when $I_2 \rightarrow I_0$. In order to solve the problem, an optimum scheme with the main idea to synthesize the current reference vector with available non-nearest vectors is proposed. Instead of using zero vector and guaranteeing only one switch action when the vector changes, the proposed solution used the optimum vector sequence $I_1 \rightarrow I_2 \rightarrow I_3 \rightarrow I_2$, and the maximum step change of $U_{dc}$ can be avoided. Therefore, compared with the conventional solution, the proposed scheme can significantly reduce the DC-link current ripple. Next, a detailed theoretical analysis will be derived.

![Figure 8. Relationship of variables in sector 12 and sector 1.](image)

Different from the conventional current source rectifier, the primary side voltage of the HFT must be alternating positive and negative to maintain the volt-sec balance. Therefore, taking reference vector located in sector 1, for example, three active vectors $I_1$, $I_2$, and $I_3$ are used in the positive half-cycle, and the active vectors $I_4$, $I_5$, and $I_6$ are used in the negative half-cycle. Based on the above analysis, Table 3 shows the corresponding relationship between the 12 sectors and the vector sequence.

| Sector | Vector Action Sequence |
|--------|-----------------------|
| 1      | $I_1-I_2-I_3-I_4-I_5-I_6-I_3$ |
| 2      | $I_3-I_2-I_1-I_6-I_5-I_4-I_3$ |
| 3      | $I_2-I_3-I_4-I_5-I_6-I_4-I_6$ |
| 4      | $I_4-I_3-I_2-I_1-I_6-I_5-I_6$ |
| 5      | $I_5-I_4-I_3-I_2-I_1-I_6-I_6$ |
| 6      | $I_6-I_5-I_4-I_3-I_2-I_1-I_6$ |
| 7      | $I_5-I_4-I_3-I_2-I_1-I_6-I_5$ |
| 8      | $I_4-I_3-I_2-I_1-I_6-I_5-I_5$ |
| 9      | $I_5-I_4-I_3-I_2-I_1-I_6-I_5$ |
| 10     | $I_6-I_5-I_4-I_3-I_2-I_1-I_6$ |
| 11     | $I_5-I_4-I_3-I_2-I_1-I_6-I_5$ |
| 12     | $I_1-I_6-I_5-I_4-I_3-I_2-I_1$ |
When the reference vector is located in the odd sector (1, 3, 5, 7, 9, 11), the dwell times of each vector can be calculated by

\[
\begin{align*}
T_n &= T_s - mT_s \sin (\frac{\pi}{6} + \theta) \\
T_{n+1} &= \sqrt{3} mT_s \sin (\frac{\pi}{3} + \theta) - T_s \\
T_{n+2} &= T_s - T_1 - T_2 
\end{align*}
\]

(6)

When the reference vector is located in the odd sector (2, 4, 6, 8, 10, 12), the dwell times of each vector can be calculated by

\[
\begin{align*}
T_n &= \sqrt{3} mT_s \sin (\frac{\pi}{3} - \theta) - T_s \\
T_{n+1} &= mT_s \sin (\theta - \frac{\pi}{6}) + T_s \\
T_{n+2} &= T_s - T_1 - T_2 
\end{align*}
\]

(7)

By combining (1) and (6)–(7), the DC-link current ripple can therefore be calculated in (8). Additionally, Figure 5b shows the increasing/decreasing trend of the current ripple of the proposed scheme.

\[
\begin{align*}
\Delta I_{L1} &= \frac{U_{ab} - U_o}{L} T_1 = \frac{U_i \cos (\frac{\pi}{3} + \theta) - U_o [T - mT \sin (\theta + \frac{\pi}{6})]}{2} \\
\Delta I_{L2} &= \frac{U_{ac} - U_o}{L} T_2 = \frac{U_i \cos (\frac{\pi}{3} - \theta) - U_o \sqrt{3} mT \sin (\theta + \frac{\pi}{3}) - T}{4} \\
\Delta I_{L3} &= \frac{U_{bc} - U_o}{L} T_3 = \frac{U_i \cos (\theta - \frac{\pi}{6}) - U_o T - T_1 - T_2}{2} \\
\Delta I_{L4} &= \frac{U_{ac} - U_o}{L} T_4 = \frac{U_i \cos (\theta - \frac{\pi}{3}) - U_o \sqrt{3} mT \sin (\theta + \frac{\pi}{3}) - T}{4}
\end{align*}
\]

(8)

From (8) and Figure 5b, the peak–peak value of the DC-link current ripple of the proposed scheme can be defined as

\[
\Delta I_{Lm} = \left| \frac{U_i \cos (-60^\circ) - U_o}{L} \cdot T - T_1 - T_2 \right| = \left| \frac{U_i - 2U_o}{2L} \cdot 2T - \sqrt{3} mT \right|
\]

(9)

As shown in Figure 5, it can be observed that the proposed solution can effectively mitigate the DC-link current ripple compared with the conventional solution.

Figure 9 shows the control algorithm, which can be summarized into the following seven steps:
4. Simulation Results

In order to verify the effectiveness of the theoretical analysis, comparative simulations in MATLAB/Simulink with the proposed SVPWM strategy and the conventional scheme for the three-phase isolated matrix converter are carried out. The MATLAB/Simulink model consists of the main circuit and control module, where the IGBT is used for the main circuit of matrix converter, and the S-function is used to implement the control module of space vector modulation algorithm, as shown in Figure 10. The simulation parameters are listed in Table 4.

Table 4. Parameters of simulation model.

| Parameters                  | Value  |
|-----------------------------|--------|
| Power voltage $U_{ref}$     | 380 V  |
| AC inductance $L_i$         | 2.5 mH |
| AC capacitance $C_f$        | 10 µF  |
| Switching frequency $f_s$   | 20 kHz |
| DC inductance $L_{dc}$      | 1 mH   |
| DC capacitance $C_{dc}$     | 940 µF |
| Load resistance $R$         | 50 Ω   |
| Transformer leakage inductance $L_{lk}$ | 3.6 µH |

Figure 11 shows the rectifier bridge output voltage and DC-link current ripple waveforms under the different inductance values. It can be observed that the traditional modulation scheme produces a large DC-link current ripple when $U_{dc}$ steps from the highest line voltage to 0. On the contrary, the proposed solution employs the optimum vector sequence, which can effectively avoid the maximum step change of $U_{dc}$. As a consequence, the DC-link ripple of the proposed solution is much lower than that of the conventional one.
Figure 10. MATLAB/Simulink model. (a) Main circuit and control module. (b) S-function of SVPWM.

Figure 11. Rectifier bridge output voltage and inductor current ripple. (a) Inductance with 2 mH (b) Inductance with 1.5 mH (c) Inductance with 1 mH.
Figure 12 shows the filter inductor current waveforms under the different inductance values. It can be clearly seen that the peak-to-peak current ripples of the traditional scheme are 2.07 A, 1.32 A, and 1 A at 1 mH, 1.5 mH, and 2 mH inductance values, respectively. From Figure 12b, the peak-to-peak current ripple of the proposed scheme are 1.36 A, 0.9 A, and 0.68 A with corresponding inductance values; that is to say, the maximum DC-link ripple of the proposed scheme is much lower than that of the conventional one. It is also noted that the smaller the inductance, the better the current ripple reduction.

![DC output filter inductor current waveform](image)

**Figure 12.** DC output filter inductor current waveform. (a) Inductance with 2 mH (b) Inductance with 1.5 mH (c) Inductance with 1 mH.

For analysis of simulation, it can be seen that compared with the traditional scheme, the new scheme can reduce the DC-side inductance current ripple only by changing the modulation strategy without increasing the inductance value and switching frequency.

For easier viewing, the peak-to-peak current ripple of the traditional scheme and the proposed scheme with different inductance values are summarized in Figure 13. It can be observed that the proposed scheme can effectively reduce peak-to-peak current ripple compared with the conventional solution. In other words, for a given current ripple requirement, the DC-link inductor can be designed as a smaller size and lower inductance and cost.
5. Experimental Results

To verify the proposed SVPWM strategy for the three-phase isolated matrix converter, a lab prototype is built, as shown in Figure 14. Texas Instruments DSP TMS320F28335 and FPGA XC6SLX9-2TQG144C are used to implement the control algorithm. Detailed parameters of the experiment are listed in Table 5.

![Experimental setup](image)

**Table 5. Experimental parameters.**

| Parameters         | Value  |
|--------------------|--------|
| Power voltage $U_{ref}$ | 50 V   |
| AC inductance $L_f$      | 2.5 mH |
| AC capacitance $C_f$     | 10 μF  |
| Switching frequency $f_s$ | 10 kHz |
| DC inductance $L_{dc}$   | 1 mH   |
| DC capacitance $C_{dc}$  | 940 μF |
| Load $R_{dc}$            | 30 Ω   |

Figures 15 and 16 show the experimental waveforms of the conventional SVPWM. The overall and detailed enlarged waveforms of the primary and secondary voltages of the transformer are shown in Figure 15, and it can be seen that the measured waveforms of the primary and secondary voltages of the transformer step from a higher voltage amplitude to a lower one and they are characterized by the alternatively positive and negative variations. It is also noted that the voltage amplitudes of the primary and secondary sides
are approximately the same since the transformer ratio is designed to be 1:1. Figure 16 shows the experimental waveforms of the output voltage and DC-link inductor current with the conventional solution. The current ripple is large since the SVPWM modulation is not optimized.

![Figure 15. Experimental results with conventional solution. (a) Overall waveform (b) Detail waveform.](image)

![Figure 16. Output voltage and inductor current with conventional solution.](image)

Figure 17 shows the experimental comparison of the conventional and proposed solutions from the viewpoint of the rectifier bridge output voltage and DC-link current ripple. The experimental parameters are listed in Table 5. It can be seen that the DC-link current ripple has been reduced from 0.5 A (conventional scheme) to 0.3 A (proposed scheme), and the corresponding current ripple factors are 45.4% and 27.3%, respectively. Consequently, the experimental results verify the effectiveness of the proposed strategy that can significantly reduce the DC-link current ripple, which is in agreement with the theoretical analysis in Figure 12.

![Figure 17. Comparison waveforms of conventional and proposed schemes. (a) Traditional scheme (b) Proposed scheme.](image)
6. Conclusions

This paper presented an optimized SVPWM by using the active vector instead of the zero vector to reduce the DC-side inductor current ripple for the three-phase isolated converter. After theoretical analysis, simulation, and experimental verification, the following conclusions are obtained. Different from the traditional modulation schemes, the proposed solution can effectively reduce the current ripple. On the other hand, the application of large filter inductance is avoided. Aside from that, the proposed scheme can be easily implemented without increasing the switching frequency or adding any other hardware. Therefore, the proposed scheme is attractive for three-phase isolated converter applications.

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Nomenclature

SVPWM  Space vector pulse width modulation
FACTS  Flexible ac transmission system
FPGA  Field-programmable gate array
IGBT  Insulated gate bipolar transistor
HVDC  High voltage direct current
HFT  High-frequency transformer
THD  Total harmonic distortion
DSP  Digital signal processor
MC  Matrix converter

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