To Analyze Energy Band Diagram of N-Tunnel Field Effect Transistors (NTFET)

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Abstract. In low power consumption devices an emerging device of transistor is Tunnel Field Effect Transistors (TFET). Although MOSFET (Metal Oxide Field Effect Transistors) having applications based on low energy usable electronics devices the power is reduced by reducing supply voltage but by decreasing supply voltage slow down the sub threshold swing. By the down scaling of MOSFET static power become high. As TFET having structure closer to MOSFET and working of TFET is based on p-i-n diode in which tunnel current flows between the source and channel bands. The low value of leakage current and sub threshold swing in TFET is used for low power applications as the switching in TFET is on the principle of modulating quantum tunneling through a barrier instead of modulating thermionic emission over a barrier as in MOSFET. The analysis on Energy band diagram of NTFET discussed in this paper.

Keywords: MOSFET, TFET, SG-TFETDG-TFET, NTFET

1. Introduction

An important area under consideration in semiconductor field, specifically in devices, is the continual scaling down of device measurements. In the past, we came across large vacuum tubes to first MOSFET with a Channel length of 300 μm to transistors with Channel lengths of 14 nm or less. This leads to integration of circuits with billion of transistors on a single VLSI chip. By Scaling the length of a MOSFET i.e. by reducing the Channel length, we can increase the number of transistors which leads to an increased Gate capacitance, increased switching speed of VLSI circuit. Additionally, the voltage scaling that is an essential part of a device likewise causes decrease in the power utilization of the device.

A comparison of SGTFET and DGTFET is done and a novel design for DGTFET with significant improvements is proposed. It is also shown that current associated to the device is not confined to Gate-Dielectric surface [1]. A complete survey on TFET with various structures available for its design and also with variation in various parameters was done [2]. The Dual Modulation effects on Surface potential of Channel i.e. Channel is controlled by Gate supply and Drain supply voltage in different operating regimes. [3]. In pseudo-2-D analytical model to analyze the electrostatics of Multiple Gates TFETs, with convenient set of equations to describe and compare SOI, DGTFET and Cylindrical Nano wire devices simultaneously on the basis of numerical simulations [4]. Two dimensional analytical models were analyzed for Surface potential, Electric Field, Iₐ₅, Subthreshold Swing and Vₜ. In the proposed model, Dual Material Double Gate TFET with stacked SiO₂/HfO₂ is analyzed. All the simulations are carried out on Silvaco ATLAS TCAD [5]. Ambipolar conduction in tunnel field-effect transistors (TFETs) occurred due to drain-channel tunneling [6]-[7]. The model describes the impact of device design parameters on the electrical performance of the device [10]. An N-channel tunnel field effect transistor (TFET) i.e. double gate N-TFET for improved subthreshold slope (SS) and OFF-state leakage current (Iₐ₅) with reference to drain bias (VDS), and body thickness (TSI) [11].

2. Research Methodology

2.1 Problem Definition:

In this segment, the procedure used to do this research work has been talked about which is utilized to structure DGTFET. The essential point of this research work is to consider the performance analysis of
the structure. This work is accomplished with the assistance of tool Cogenda TCAD version 1.9.2. The designing of the device, simulation and correlation of results have been gotten on this tool. The section gives the stream of Research Methodology and clarifies the footsteps for Design and Simulation of Double Gate Tunnel Field Effect Transistor.

![Flowchart of Proposed Work](image)

**Figure 1.** Flowchart of Proposed Work

### 2.2 Device Design in Genius Device Simulator
The device is outlined by Cogenda Semiconductors. This tool is used for Device Modeling, Device Simulation and Classification of devices i.e. Transistors and diodes are finished utilizing different techniques. The Closed Form Equations contained in Analytical Technique is used for modeling using SPICE. Experimental Techniques are used for Classification or Characterization of devices. 2D and 3D meshing which are included in Numerical techniques are used for Simulations for which TCAD is required.

The simulator used in Cogenda TCAD is Genius which is very powerful simulator. Cogenda Visual TCAD contains GUI (Graphical User Interface) which is used for creating 2D and 3D structures. Circuit simulation is also possible in Cogenda TCAD with some basic features like Advanced Device...
Modeling specification, Visualization, Syntax Text Editor, Spreadsheets, X-Y plot for 2D models etc. Various analysis methods like Optical Simulation, DC analysis, AC analysis and Simulation etc. Advanced features like Boundary Conditions, Physical models etc are also available. By using Visual TCAD we get a clear image of physics behind every Semiconductor device at Microelectronics level.

There are different steps for Device Simulation is:

1. Characterize X, Y and Z mesh.
2. Characterize Region and Relating Materials.
3. Characterize Doping Profile.
4. Apply the available Models.
5. Apply Supply Voltage or Voltage Bias.
6. Export File.

The Diagram shown in Figure 2 is the Structure of Two Dimensional Double Gate TFET drawn in the Device Drawing Window with X-Y axis with various regions labeled with it.

![Figure 2. Schematic Diagram of Double Gate TFET](image)

| S.NO | PARAMTRES             | SIZE  |
|------|-----------------------|-------|
| 1.   | Channel Length        | 30nm  |
| 2.   | Oxide Thickness       | 3nm   |
| 3.   | Body Thickness        | 10nm  |
| 4.   | Source/Drain Length   | 10nm  |
5. Work Function of metal contact  
   Work Function 4.5 eV

6. Source Concentration  
   Source Concentration $10^{17}$/cm$^3$

7. Drain Concentration  
   Drain Concentration $5 \times 10^{18}$/cm$^3$

8. Intrinsic Channel Concentration  
   Intrinsic Channel Concentration $10^{20}$/cm$^3$

The Table 1 above shows the various specifications associated with the Double Gate TFET. Various parameters are considered like Doping concentrations, dimensions and materials used. The Tunneling model is used is Non Local BTBT model used extensively for simulation of ON Current i.e. to study the Charge Transfer through the Potential barrier by taking into consideration the Potential profile in the region of Tunneling.

2.3 Doping in Different Regions

The next step after drawing device and defining various regions of Double Gate TFET i.e. Source, Drain and Dual Gates (Gate1 and Gate2) and contact terminals and defining materials of different regions, the next step will be Doping different regions. In DGTET, Uniform doping is done in Source, Drain and Intrinsic Channel region. In NTFET, Source side is highly doped with Donor type, Drain side is highly doped with Acceptor type and intrinsic region is lightly doped with Donor type of impurity.

![Figure 3. Doping Profile Window](image_url)
2.4 Meshing of Device Structure

The next step is to apply mesh. Firstly, option 'Do mesh' is selected from the Terminal bar. After that, save the Device Window to mesh file. The mesh file is saved with file name (.drw). The mesh structure of DGTFET is shown in Figure 4. In Tunnel Field Effect Transistors, the tunneling occurs at the Source to Channel junction and Tunneling is main principle of TFET. So, finest mesh must be done at the both the junctions i.e. Source-Channel region and the Channel-Drain region as we know the leakage current in TFET is due to Tunneling at the Channel-Drain region.

![Figure 4. Mesh Structure of DGTFET](image)

![Figure 5. Mesh Window of Visual TCAD](image)
2.5 Loading Files:

After completing procedure of meshing, save this file to (.tif) file using Device option of Menu bar in which we get option "Save Mesh to file". After the file is saved go to File option and open the Device Simulation. The folder below the Setup, open the (.tif) file and after taking little time structure will be loaded from (.tif) file with contacts in the centre of Electrode Work Area e.g. Gate1, Gate2. Source and Drain.

![Figure 6. Loading File for Device Simulation](image)

The next step is to connect both the Gate terminals i.e. Gate1 and Gate2. Go to Boundary Conditions -> Interconnections and then connect both the terminals and name it as GATE. All the steps are shown in Figure 7.
After this step provide Supply voltage at various terminals i.e. Gate, Drain and Source. Provide **Constant Voltage** to the Drain side and **Voltage Sweep** to the **Gate** from 0V to 2V. Now **save** all the changes with some name with the help of **Run** optionsavethe file in (.sim) format.

The next step is to create a Folder and give it a name after choosing the particular folder where all the data is saved with the particular device structure. The file is saved in (.dat) format in the folder which is selected for simulation.

### 2.6 Simulation of $I_D$-$V_{GS}$ Characteristics:

After completing the Device Design, the next procedure is Simlation phase. For simulation of Device designed in the foregoing step, open the Simlulation terminal and then load the file of that particular device design in the simlation terminal as shown in Figure 8. In the figure below, it is shown that the file of Device Design is loading in the Simlation window.
3. Results and Discussion

Energy Band Diagrams

The various states in energy band are as follows

3.1 Equilibrium State

The Equilibrium state is when, there is no external bias applied i.e. $V_G = V_S = V_D = 0$. The Band diagram at equilibrium state is shown below. In this state, there are two depletion region formed, one at Source-Channel junction and other region is formed at Channel-Drain region. The Energy Band diagram for equilibrium state is shown in Figure 9.

3.2 OFF State

OFF State is when $V_{DS} > 0$ and no bias is applied at the Gate terminal i.e. $V_{GS} = 0$. This state is similar to MOSFET. The Band diagram is shown in Figure 9 below. In this state, any Charge carrier present in the Conduction Band of Channel have a possibility to drift to Drain side and generate small amount of leakage current. The electrons in the Valence band of Source side do not have vitality states available into which they can tunnel. Now, as the Source is $p^+$, there are very less number of electrons.
Figure 9. Energy Band diagram of TFET in Equilibrium Condition [2]

Very few electrons are injected into Drain side and hence lead to negligible current in OFF state. In OFF state, TFET has least leakage current as compared to MOSFET in which electrons are injected from n-type Source (electrons in majority) to Channel region by thermionic emission and leads to high OFF-state current.

3.3 ON State
Current will flow when Charge carriers tunnel from Valence band in Source side to Conduction band in Channel region. In case of N-TFET, Source side is P+ doped, so there are negligible electrons in Conduction band in Source side. Hence, the Charge carriers i.e. the electrons start to tunnel when Gate voltage applied is as shown in Fig.10. For the definite value of Gate supply $V_{GS}$, the Valence Band in Source side get just aligned to the Conduction Band in Channel side and electrons can tunnel to the Channel side as now they have available energy states in the Channel's Conduction Band through potential barrier $E_C$ (dashed shape in Figure 11).

As the $V_{GS}$ is further increased, there will be more Band bending in Channel region and more and more Electrons tunnel from Valence band edge of Source ($E_{V(source)}$) to Conduction band edge of Channel ($E_{C(Channel)}$) and generates steep increment in current because of decrease in Tunneling barrier. Due to this steep increase in current, Subthreshold Swing decreases.
The amount of tunneling depends on the height barrier i.e. on Band-gap of the material used) and length of the potential barrier (depends on the steepness of the energy Bands). Higher the slope shorter will be the tunneling length. The maximum slope lies at the junction from the knowledge of p-n junction diode. In TFET, this junction lies almost at the edge of Source side. The Source side is heavily doped so electrons from Valence band of Source tunnel through shorter tunneling length in comparison with the electrons from Conduction band of Channel side. Hence, tunneling probability at Source is more than the Channel side.

**Figure 10.** Energy Band Diagram of TFET in OFF state [2]

**Figure 11.** Energy Band Diagram in ON state
3.4 Pinning of Channel
As Gate voltage increases, energy Band in Channel side further lowers and an Inversion layer (containing electrons) starts forming in the Channel as the Gate applied bias is positive. At enough Gate voltage above Drain voltage ($V_{GS}>V_{DS}$), Inversion Charge layer containing electrons becomes comparable to electron density in the Drain region and hence Channel is "shorted" to Drain. The Energy Bands in the Channel do not change notably with increase in Gate bias and the Channel potential becomes approximately equal to the potential. This phenomenon is called Pinning of Channel as the Channel potential is "pinned" to the Drain Potential [2]. Pinning do not occur notably when $V_{GS}>V_{DS}$ (not when $V_{GS}=V_{DS}$).

There is an increase in ON current due to high Electric Field at Source-Channel region and increase in the number of energy levels of Source Valence Band from where tunneling occurs. It is depicted from the Figure 12 that at Source Channel junction, Electric Field increases even when the Channel potential is pinned to Drain potential. When $V_{GS}>V_{DS}$ ON current increases with Gate bias but at a lower rate than in case of $V_{GS}<V_{DS}$.

![Energy Band Diagram for Different $V_{GS}$ and $V_{DS}$](image)

**Figure 12.** Energy Band Diagram for Different $V_{GS}$ and $V_{DS}$

4. CONCLUSION
Double Gate TFET structure is like that of MOSFET aside from that Source and drain are doped with dopants of opposite polarity and Channel is intrinsic or uniformly doped [28]. Figure 13 shows N-TFET in which drain side is doped with donor type of impurities (n+) , Source side is doped with acceptor type impurities (p+) and Channel is n-type intrinsic region and TFET forms a gate PIN diode in which drain is applied positive with respect to Source and works under reverse biased condition. The Tunneling occurs between Source and Channel region, so Channel region is to be made of n-type material to further cause the bending of Conduction band in the Channel region than p-type material.
The Energy band diagram of N-TFET is as shown Figure 14 for $V_{GS}=0$V and 2V. The Tunneling procedure can be comprehended by Energy band diagrams. It depicts that when gate voltage is zero, band is not bending in the Channel. The width of the band barrier is greater than 10nm. At the point when the gate supply is increased the band in the Channel region start bending downward i.e. the filled valence band of Source side is parallel to the unfilled Conduction band of Channel region and hence the electrons start tunneling due to band bending, the barrier width is reduced and electrons tunnel from Source to Drain. As a result, the drain current increases.

Tunneling can be enhanced by increasing the doping concentration of the Source side up to some optimized value, as more charge carriers are available to tunnel and also the depletion region is also decreased and hence the ON-current is improved while keeping the OFF current small.

**Figure 13.** Schematic Diagram of Double Gate TFET

**Figure 14.** Energy Band Diagram of Double Gate TFET, (a) At $V_g=0$V, (b) At $V_g=2$V

The performance and Simulation analysis of Double Gate Tunnel Field Effect Transistor observed. The device structure of Double Gate TFET optimize by varying different parameters.
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