Digital Error Correction Logic for Pipelined ADC Using 1.5Bits/ Stage

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Abstract: Low power, high resolution and high-speed ADCs are becoming increasingly important with advancements in portable electronics, from mobile phones and pagers to CD players and MP3 players. This is certainly not feasible on a handheld device which is why new ADC techniques must be developed. They are becoming increasingly attractive to major data converter manufacturers and their designers because pipeline ADCs provide an optimal balance of scale, speed, resolution, power dissipation and analogue design effort. Because of latency and errors in comparators & gain stages in pipelined ADCs, the need arises for digital error correction mechanism. The digital error correction logic will be implemented for 8-bit ADC using 1.5 bits per stage. While designing we are considering important parameters of CMOS like propagation delay performance and power dissipation. The VLSI realization of digital arithmetic is implemented using TANNER EDA software tool using 0.18µm CMOS process.

Key words: Digital error correction, pipeline ADC, 1.5 bit stages

1. Introduction

Pipelined analog to digital converters (ADCs) are generally used in Nyquist sampling applications that provide a combination of high resolution and high velocity. An integral component in the low cost highly integrated chip system (SoC) was a low power low voltage ADC with high signal bandwidth. [1]. The implementation of digital error correction logic for pipeline ADCs is described in this paper. To reduce cost and increase bandwidth 1.5 bit stages are used in pipelined ADC architecture.

2. 1.5-BIT STAGES

The minimum stage resolution is an advantage for high speed converters. It mitigates the interstate gain necessary, which in gains bandwidth, because for a given technology, gain-bandwidth is a constant. Parts produced using a cost-effective CMOS wafer production process for commodities, this factor is especially significant, as highest possible velocity needed as of vital circuit blocks such as operational amplifiers. Imagine the ±Vref symmetric reference voltages.

An analog decision level will be positioned halfway between the reference voltages, which is, at ground level, with a least probable stage resolution of one bit. For the amplifier, there will be a gain of 2. A 1.5 bit stage is a one-bit stage in which some precision has been designed to have wide resistance to imperfections and part tolerances. The consistency is later removed by a digital correcting algorithm. In fact, a 1.5 bit stage is representing more or less 1.5 bits.
Instead of one, the 1.5 bit stage uses 2 equal analog assessment stages, $V_H$ and $V_L$, as shown in figure 1(a). There is a gain of 2 in the amplifier. The option of VH and VL voltage levels is not important, but they must be positioned between the range of $+V_{ref}/2$ and $-V_{ref}/2$ because of the following gain of 2.

$V_H$ is usually in the $0.2V_{REF}$ less than $V_H$ less than $0.4V_{ref}$ range, allowing the digital correction algorithm to correct circuit imperfections. $V_{HI}=0.25V_{ref}$ is a common option and $V_{LV}=-0.25V_{ref}$. 1.5 bit design has an benefit in that at mid-range, there is no analog deciding level or trip point, which benefits operation at low signal level. The operating voltage spectrum comprises three parts: High means $>V_H$, Mid means in between $V_H$ and $V_L$, and Low means $-V_L$. This process is called Redundant Signed Digit because +1, mid value as 0, and low value as -1 were originally tagged as the High range. Table 1 summarizes the 1.5-bit stage configuration overview information.

### Table 1 1.5 bit stage summary information

| VIN   | Range | B1 | B0 | DAC/OP  | Residue  |
|-------|-------|----|----|---------|----------|
| VIN-$>$VH | H     | 1  | 0  | +VREF   | 2VIN-VREF|
| VL-$<$VH | M     | 0  | 1  | 0       | 2VIN     |
| VIN-$<$VL | L     | 0  | 0  | -VREF   | 2VIN-VREF|

Two comparators plus some basic encoding are included in the stage low-resolution ADC. Two bits B1 and B0 are the ADC output. The starting digital output, prior to code conversion and error correction. In the L, M, and H input ranges, the output codes are 00, 01, and 10 for Vin, correspondingly. The digital to analog converter outputs from -$V_{ref}$ to 0 to $+V_{ref}$ for input voltage $V_{in}$ in the L, M, and H range. After subtraction, the analog remains voltages outside the stage are

| Table 2 Transfer function, different $V_H$ and $V_L$ values |
|-------------------------------------------------------------|
| Designed for | Remains  |
| $V_{IN}$ is greater than $V_H$ | $2V_{IN}-V_{ref}$ |
| $V_L$ less than $V_{IN}$ less than $V_H$ | $2V_{IN}$ |
| $V_{IN}$ less than $L$ | $2V_{IN} + V_{REF}$ |

3. **Code conversion and error correction**

As stated earlier, every 1.5 bit pipelined analog to digital converter stage produces a two bit message. This is decreased to the final one bit per stage code when the error correction algorithm is applied. The two bit per stage code must be converted to one bit per stage, except in the absent of any errors at all. In the involved circuitry, several sources of potential error exist. These include comparator and amplifier offset voltages, x2 amplifier gain error, time settling amplifier, converter nonlinearity, voltages of capacitor dependence, and others. These entire transform Table 2 perfect stage transfer function in a few quantity and path. Most of these are corrected by the error correction process or, at a minimum, substantially modified. Offset voltage effects are completely checked, such as
An uncorrected source of error is the x2 amplifier gain error. It is mainly a critical problem in 1.5 bit phases due to an error in the 2:1 capacitor ratio. The 1st stage capacitor ratio is most significant part, because the error occurs in output stage is multiply by the gains of all phases. An occasion demonstrates problems, including translation of error-correction code, followed by Table 3, are shown in Figure 2.

As the resolution is 3 bits, as shown in the first column of Table 3, the applied voltage of ±2V is split into 8 equal sectors. As see in the 2nd column, it is called DOC (design output code), the proposed output code binary increases from –ve to +ve.

Table 3 shows third column lists the input voltages selected randomly, in every of the 8 sectors of equivalent input voltage, one. Like the 3 sets of 2 digit uncorrected output codes from each of the three stages, the remaining voltages of the first 2 stages are shown.

In order to generate the converted finishing data and error corrected 3 bit output data from the three 2 bit stage codes, 2 bit digital outputs from each stage are collectively added with 1 bit superimposed between nearby stages. The definitive code is the three MSBs. If \( V_{in} = 0.79 \)V case, the output code as of the 3 steps are 10, 01, 00. As follows, it gets the final 3 bit output code.

The final output code, ignoring the far right digit, is 1 0 1. In the same way, the complete set of final output codes in Table 3 is obtained. It is possible to enforce this error correction algorithm by linking a collection of adders, or by using logic as an alternative. Table 3 Development of error corrected output code.

1.5 bit phases have been developed as together presentation and cost effective circuits in high speed pipelined ADCs. At least in terms of their basic process, they’re clear in principle.

4. Data Latency
Data latency is associated with pipelined ADCs since each sample must propagate through the entire pipeline until all its associated bits are available for combination in the digital error correction logic. This latency is around three cycles in Figure 3, where the analogue input at point N is obtained after three cycles of the clock. The latency here consists of three clock cycles.
Since the pipeline phases are interleaving (meaning when odd phases are sampled and even phases are evaluated), the outputs are present at a 1/2 clock cycle interval for a given input sample and proceed down the pipeline. So all the digital outputs are not available simultaneously. The output from the second stage would only be ready after half a clock cycle if the output from the first stage is ready. Therefore, once the last stage has finished the conversion, the sampled input signal can not be corrected.

So in order to obtain all the bits simultaneously we need to time shift the digital outputs obtained from the earlier stages accordingly. D flip-flops are used to shift the outputs. Here we use both positive and negative edge triggered D flip flops. As the stages proceed the number of flip flops gets reduced. For example if the first stage uses 5 flip flops the second stage uses only four.

Here we are using 1.5 bit per stage pipelined ADC which outputs 2 bits. So each stage outputs are given to a pair of flip flops. The ADC for which we are building digital error correction logic consists of eight 1.5 bit stages. So, in all there are 16 output bits from the 8 stages. The bits obtained after passing through digital error correction logic are 8 in number. The outputs from the comparators of the different ADC stages are given to the shifters or D flip flops before being fed to the adders. The waveforms shown in the figure 4 describe the requirements of shifters. Here’s ‘’ indicates sampling stage and ‘‘h’’ indicates hold stage. Due to concurrent operation while one stage samples the stage next to it holds the input obtained from previous stage.

One set of alternate stages sample the input(if it is the first stage) or the residues obtained from previous stages while the other set of alternate stages hold the output obtained from previous stages. The LSB or the final stage output is not obtained until 4 and 1/2 clock cycles after the inputs are given. The outputs are obtained during hold stage. The output of the first stage should be shifted by four and half clock cycles, the second stage output by four clock cycles, the third by 3 and 1/2 cycles and so on. The last stage is shifted by only one cycle.
Only adding is necessary in the digital correction due to changed coding. A conceptual diagram of the digital correction is shown in figure 5. The output from stage N is delayed by clock cycles of \( \lceil (8-N)/2 \rceil + 1 \) until it is corrected. The correction is achieved by taking the output of \((N+1)\)th stage and adding one bit overlap from the LSB to the Nth stage output. The carrier will spread in the MSB direction.

5. Experimental Results

Figure 6. Digital error correction logic

Figure 7. Layout of Digital error correction logic

The figure 6 and 7 gives the digital error correction logic circuit schematic and layout. Here after shifting the outputs they are given to the full adders to perform the digital error correction. Here in all we use 48 D flip flops of which 8 are positive edge triggered and the remanant negative edge triggered. After shifting the 16 input bits they are given to 9 full adders which finally produce the digital error corrected code of 8 bits.

Here we use 0.18 micron technology and accordingly set L to 0.18 micron technology and W is set to 0.27 micron technology.

\[ I_{ds} = kW/L \left[ \frac{(V_{gs}-V_{t})^2}{2} \right] \]

The high and low voltage levels are set to 3 volts and 0 volts respectively. Here when \( V_{gs} \) is set to 3 volts the circuit operates in saturation and when 0 volts is applied it perates in cutoff fulfilling the requirement of CMOS operation.
The digital error correction logic was successfully implemented for 8-bit ADC using 1.5 bits per stage. Here we used 0.18 micron technology. We have verified the functionality by simulating the results of individual blocks and overall digital error correction logic in schematic design and layout design. The digital error correction logic is tested to work at a clock speed of 100 mega samples per second.

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