A Zero-Sequence Steerable CBPWM Strategy for Eliminating Zero-Sequence Current of Dual-Inverter Fed Open-End Winding Transformer Based PV Grid-Tied System With Common DC Bus

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ABSTRACT Aiming at the issue of zero-sequence current (ZSC) in the dual-inverter fed open-end winding transformer (OEWT-DI) based photovoltaic (PV) grid-tied system with common DC bus, a carrier-based pulse width modulation (CBPWM) strategy with steerable zero-sequence is proposed. The modulation wave of the dual-inverter is decomposed into two modulation waves with same amplitude and 120° phase difference, and each of the modulation waves is modified through adding steerable zero-sequence component. The zero-sequence component is regulated by the ZSC control loop based on a quasi-proportional resonant regulator, which is designed to suppress the ZSC caused by the dead-time effect and other nonlinear factors. Meanwhile, the effective modulation range is also analyzed. The proposed strategy is an alternative approach to the conventional zero-sequence steerable phase shift based space vector pulse width modulation (SVPWM) strategy, but has the advantage of easy implementing and low computation cost. With the proposed strategy, both the high-frequency and low-frequency ZSC in the system can be effectively suppressed. Effectiveness of the proposed strategy is validated by experimental results on a 30-kW OEWT-DI experimental platform.

INDEX TERMS Dual-inverter, open-end winding transformer, zero-sequence current, carrier-based pulse width modulation (CBPWM).

I. INTRODUCTION
In recent years, multilevel inverters have been widely used in medium and high power applications, due to the advantage of low output voltage harmonics, high efficiency, and large capacity [1]. Compared with other types of multilevel inverters (flying-capacitor, neutral-point clamped and cascaded inverters), the dual-inverter topology based on open-end winding configuration has many advantages, such as high DC voltage utilization, high modulation freedom, and easy to realize fault-tolerant operation [2]. Since the topology was proposed [3], it has been extended to a variety of applications, for instance, dynamic voltage restorer [4], STATCOM [5], motor drive [6], wind and photovoltaic (PV) power generation [8]–[12], etc.

When the topology was adopted in PV grid-tied system, it is more suitable to be used in the high power medium-voltage (MV) PV systems, where the step-up transformer is used to match the voltage levels between the inverter and the MV grid [13]. In this case, the topology is configured as dual-inverter fed open-end winding transformer (OEWT-DI) scheme, in which two voltage source inverters (VSIs) are connected to the open-end primary windings of the transformer from both the terminals, and the secondary windings of the transformer are connected to the grid via a delta or star connection. In this OEWT-DI based PV grid-tied system,
the two inverters can be designed with independent DC buses, that two inverters are connected with separate PV arrays [8]–[11], or a common DC bus, that two inverters are connected with a common PV array [12]. The system configuration with separate PV arrays has higher conversion efficiency owing to that it can achieve two separate maximum power point trackings (MPPTs). But due to the parasitic capacitances existing between the PV modules and the ground [10], the DC sides of the two inverters are connected indirectly, providing a zero-sequence path which enables the zero-sequence current (ZSC) flowing. The ZSC may increase the system losses, switch device stress and cause safety concerns. Therefore, suppressing the ZSC is necessary for such system. However, since the DC voltages and the modulation indexes of the two inverters are usually different when performing separate MPPTs, the modulation freedom of the dual-inverter is significantly reduced, leading to that it is hardly to suppress the ZSC by neither modulation nor control method. As a result, the application of this configuration is limited. The system configuration with a common PV array also faces the ZSC problem, but has the possibility to be suppressed by appropriate modulation and control strategy [12], which has a certain application prospect.

In current research, the ZSC suppression methods of the dual-inverter with common DC bus mainly focus on the topology used in open-end winding induction motor [14]–[19] or permanent magnet synchronous machine (PMSG) systems [20]–[30]. Whether these methods are suitable for the OEWT-DI based PV grid-tied system is worth discussing.

The zero-sequence voltage (ZSV) of the OEWT-DI based system, which is the source of the ZSC, is mainly caused by pulse width modulation (PWM), dead-time effect and other nonlinear factors. Therefore, only using modulation strategy to suppress the ZSC, such as the “zero vector placement” modulation strategy [14]–[16] or the zero ZSV modulation strategy [17]–[24], is not sufficient. In order to improve the ZSC suppression effect, modulation strategies should be implemented in conjunction with corresponding control methods. In [25], a ZSC suppression method based on PI regulator and ZSV controllable space vector PWM (SVPWM) strategy was introduced. In [26], a proportional resonant (PR) regulator and zero vector redistribution (ZVR) SVPWM strategy based ZSC suppression method was proposed. In [27], a novel ZSC suppression method with a PR regulator and a reduced switching frequency modulation strategy was presented. All [25], [26] and [27] achieved good ZSC suppression effect in the open-end winding PMSG system with the corresponding method. However, it should be noted that these methods mainly consider the suppression of low-frequency ZSC, the high-frequency ZSC is generally suppressed by the motor stator inductance. For the OEWT-DI based PV inverters, the three-phase three-limb inductors are usually used as the filter inductors for the purpose of cost and size reduction. But this kind of inductor has the characteristic that the zero-sequence inductance is relatively small owing to the lack of independent flux return paths [31], so the adoption of these methods [25]–[27] will inevitably result in excessive high-frequency ZSC, which is unacceptable. In [28], a PR regulator and a switching signal phase shift based sinusoidal PWM strategy was proposed to suppress the ZSC, both the high- and low-frequency ZSC were effectively suppressed. However, the phase shift of the switching signal will cause half-wave asymmetry problem, and even-order harmonics will be existed in the inverter output phase current, especially when considering the dead-time effect. In [29] and [30], a ZSC suppression method based on zero sequence steerable SVPWM (ZSS-SVPWM) strategy was proposed. In the method, the 120° phase shift based SVPWM strategy is used, and a ZSC control loop is added to steer the zero sequence component by adjusting the dwell time of the zero-vector. The method can effectively reduce the ZSV caused by modulation and counteract the ZSV caused by other disturbance sources. Thus, it can be used in the OEWT-DI based PV grid-tied system. However, the effect mechanism of changing the zero-vectors’ dwell time on the ZSV and the effective modulation range of the strategy were not analyzed in the literature. What’s more, the implementation of the modulation strategy is complicated due to the need of sector identification, switching time calculation and lookup tables, etc.

In light of the above, for suppressing the ZSC of the OEWT-DI based PV grid-tied system, a zero sequence steerable carrier-based PWM (ZSS-CBPWM) strategy is proposed in this paper. The proposed ZSS-CBPWM strategy is actually a carrier based equivalent implementation of the conventional ZSS-SVPWM strategy, which has the advantage that easier to implement and less calculation required. The remainder contents of this paper are as follows. In Section II, the mathematical model including the ZSC model of the OEWT-DI based PV grid-tied system is established. In Section III, a further research on the conventional 120° phase shift based SVPWM strategy is made. This strategy is the fundamental of the proposed ZSS-CBPWM strategy, which has also been widely used in the current research. However, the strategy has not been analyzed in depth so far, so this paper will complement it. In Section IV, the principle of the proposed ZSS-CBPWM strategy is presented, the effect mechanism of adjusting the zero-vectors’ dwell time on ZSV is analyzed, and the effective modulation range of the proposed strategy is also investigated. In Section V, the overall control scheme based on the ZSS-CBPWM strategy is presented. In Section VI, the proposed scheme is tested on a 30-kW OEWT-DI experimental platform. Finally, conclusions of this paper are made in Section VII.

II. MATHEMATICAL MODEL OF OEWT-DI BASED PV GRID-TIED SYSTEM WITH COMMON DC BUS

Fig. 1 shows the structure of the OEWT-DI based PV grid-tied system with common DC bus. The dual two-level (D2L) inverter, which was composed of two two-level VSIs, named VSI-1 and VSI-2, is adopted as the main circuit topology. The DC sides of the two VSIs are connected in parallel and
supplied by a common PV array. An LC filter is set between the inverter output and the primary winding of the open-end winding (OEW) transformer, where inverter-side inductor $L_i$ is a three-phase three-limb inductor for cost savings. The leakage inductance of the OEW transformer is used as the grid-side inductor, which together with the LC filter forms an LCL filter structure.

### A. BASIC MATHEMATIC MODEL OF OEWT-DI

The mathematic model of the OEWT-DI based PV grid-tied system includes the basic mathematic model and the ZSC model. For the basic mathematic model, in order to facilitate the analysis, the filter capacitor $C$ is ignored, and all the parameters are referred to the primary side of the transformer. According to Kirchhoff’s voltage law (KVL), the phase voltage expressions of the system can be expressed as

$$\begin{align*}
v_a &= v_{ga} + L \frac{di_a}{dt} = v_{a1n} - v_{a2n} \\
v_b &= v_{gb} + L \frac{di_b}{dt} = v_{b1n} - v_{b2n} \\
v_c &= v_{gc} + L \frac{di_c}{dt} = v_{c1n} - v_{c2n}
\end{align*}$$

where $v_k$ and $i_k$ are the phase-$k$ synthesized output voltage and inverter-side current of OEWT-DI, respectively; $v_{gk}$ is phase-$k$ grid voltage; $v_{k1n}, v_{k2n}$ are the phase-$k$ pole voltage of VSI-1 and VSI-2, respectively; $k = a, b, c$; $L$ is the total inductance of the filter.

Performing Clarke and Park transformation on (1), the system expressions in the $dq$ synchronous rotation coordinate frame can be obtained as

$$\begin{align*}
v_d &= v_{gd} - \omega Li_d + L \frac{di_d}{dt} = v_{d1} - v_{d2} \\
v_q &= v_{gq} + \omega Li_q + L \frac{di_q}{dt} = v_{q1} - v_{q2}
\end{align*}$$

where $v_d$, $v_q$ and $i_d$, $i_q$ are the $dq$ coordinate components of the synthesized output voltage and inverter-side current of OEWT-DI, respectively; $v_{gd}$, $v_{gq}$ are the $dq$ coordinate components of grid voltage; $v_{d1}$, $v_{q1}$ and $v_{d2}$, $v_{q2}$ are the $dq$ coordinate components of the VSI-1 and VSI-2 output voltage, respectively; $\omega$ is the grid angular frequency.

### B. ZSC MODEL OF OEWT-DI

For the ZSC model, the filter capacitor $C$ can affect the model characteristic and cannot be ignored. Taking the negative terminal (point n) of the DC bus as the reference point, with considering the ZSV disturbance caused by dead-time effect and other nonlinear factors, the three-phase zero-sequence equivalent circuit model of OEWT-DI with common DC bus can be established as shown in Fig. 2.

In Fig. 2, $v_{D0}$ is the ZSV disturbance caused by dead-time effect and other nonlinear factors; $L_{i,0}$ is the zero-sequence inductance of inverter-side inductor; $L_{i}$ is the leakage inductance of the OEW transformer. According to KVL, the three-phase loop equations in the complex frequency domain can be written as

$$\begin{align*}
v_{a2n}(s) - v_{a1n}(s) - v_{D0}(s) + i_0(s) \left( L_{i,0}s + L_{i} \right) \frac{1}{Cs} &= 0 \\
v_{b2n}(s) - v_{b1n}(s) - v_{D0}(s) + i_0(s) \left( L_{i,0}s + L_{i} \right) \frac{1}{Cs} &= 0 \\
v_{c2n}(s) - v_{c1n}(s) - v_{D0}(s) + i_0(s) \left( L_{i,0}s + L_{i} \right) \frac{1}{Cs} &= 0
\end{align*}$$

(3)

Summing up the equations in (3), we can get the expression of ZSC $i_0(s)$ as follows

$$i_0(s) = \frac{[v_{cm1}(s) - v_{cm2}(s) + v_{D0}(s)]}{H(s)}$$

where $i_0 = (i_a + i_b + i_c)/3$; $H(s)$ is the transfer function of the zero-sequence impedance (ZSI); $v_{cm1}$ is the common-mode voltage (CMV) generated by VSI-1; $v_{cm2}$ is the CMV generated by VSI-2; and

$$\begin{align*}
v_{cm1}(s) &= \frac{1}{3} \left[ v_{a1n}(s) + v_{b1n}(s) + v_{c1n}(s) \right] \\
v_{cm2}(s) &= \frac{1}{3} \left[ v_{a2n}(s) + v_{b2n}(s) + v_{c2n}(s) \right] \\
H(s) &= \frac{L_{i,0}L_{i}Cs^3 + (L_{i,0} + L_{i})s}{L_{i}Cs^2 + 1}
\end{align*}$$

According to (4) and (5), the single-phase zero-sequence equivalent circuit model of OEWT-DI can be drawn as shown.
in Fig. 3. From the figure, it can be seen that the ZSV sources mainly include \(v_{pwm0}\) (\(v_{pwm0} = v_{cm1} - v_{cm2}\)) and \(v_{D0}\), the ZSI is a filter network composed of \(L_{i,0}\) and \(L_i\). In the tested system, the values of \(L_{i,0}\), \(C\) and \(L_i\) are 0.36mH (\(L_i\) is 3.6mH and \(L_{i,0}\) is about 10% of \(L_i\)), 11µF and 1mH, respectively. With the adopted value, the Bode plot of the ZSI transfer function \(H(s)\) is drawn and shown in Fig. 4. It can be seen that in the low-frequency region, the ZSC is mainly suppressed by \(L_{i,0}\) and \(L_i\), while in the high-frequency region, the ZSC is mainly suppressed by \(L_{i,0}\). \(L_{i,0}\) is a relatively small value due to the lack of independent flux return paths in the three-phase three-limb inductor \(L_i\). Hence, if using the ZSC suppression method which only considering the elimination of low-frequency ZSV [25]–[27], the excessive high-frequency ZSC can be easily induced by the high-frequency ZSV disturbance. Therefore, in order to suppress the ZSC effectively, both the low-frequency and high-frequency ZSV need to be reduced to a promising value.

For the two ZSV sources described above, the value of \(v_{pwm0}\) can be controlled by modulating the D2L inverter, while \(v_{D0}\) is uncontrollable. But fortunately, the amplitude of \(v_{D0}\) is within a certain range, it can be counteract by controlling the \(v_{pwm0}\). Therefore, the basic methodology to reduce the ZSV is as follows. First, modulating \(v_{pwm0}\) to zero through proper modulation strategies. Then, tuning the value of \(v_{pwm0}\) to counteract the influence of \(v_{D0}\) by designing a closed-loop control of the ZSC.

### III. CONVENTIONAL 120° PHASE-SHIFT BASED SVPWM STRATEGY

The conventional 120° phase-shift based SVPWM strategy is widely used in current research for suppressing the ZSC of the open-end winding topology [22]–[24]. It is also the fundamental of the proposed strategy in this paper. However, the principle of this strategy has not been well studied in the existing literatures. So, in this section, a further research on the conventional 120° phase-shift based SVPWM strategy is given first.

For the D2L inverter, the voltage vector of the sub-inverters VSI-1 and VSI-2 can be, respectively, defined as

\[
\begin{align*}
V_{s1} &= \frac{2}{3} (v_{a1n} + v_{b1n}e^{j2\pi/3} + v_{c1n}e^{-j2\pi/3}) \\
V_{s2} &= \frac{2}{3} (v_{a2n} + v_{b2n}e^{j2\pi/3} + v_{c2n}e^{-j2\pi/3})
\end{align*}
\]

where \(V_{s1}\) is the voltage vector produced by VSI-1, \(V_{s2}\) is the voltage vector produced by VSI-2.

The basic voltage vectors of VSI-1 and VSI-2 are shown in Fig.5 (a) and (b), respectively. The corresponding switching states are shown in the brackets, where “1” means the upper switch of a leg is switched on and the lower one is switched off, while “0” means the opposite state. According to (1) and (6), the voltage vector \(V_s\) produced by the D2L inverter can be calculated as

\[
V_s = V_{s1} - V_{s2}
\]

Consequently, 64 switching combinations can be generated by the D2L inverter. Specially, 20 of them have the characteristic that the D2L inverter generates null ZSV with these switching combinations [17]. The voltage vectors of these switching combinations, including 12 active vectors and 8 zero vectors, are marked as \(V_{mn}'\) (\(m, n = 0\sim7\)) as shown in Fig. 6, where \(V_{mn}'\) is a combination voltage vector of \(V_m\) of

![FIGURE 4. Bode plot of the ZSI transfer function \(H(s)\).](image)

![FIGURE 5. Voltage vectors generated by VSI-1 and VSI-2. (a) VSI-1. (b) VSI-2.](image)

![FIGURE 6. Zero ZSV voltage vectors of the D2L inverter.](image)
VSI-1 and $V_{0}'$ of VSI-2. Therefore, in the ideal case, the ZSV can be eliminated by employing these special voltage vectors to implement SVPWM.

As to the conventional zero ZSV SVPWM strategy [20], there are two possible voltage vector sequence to synthesize the reference voltage vector. One is $(V_{00}', V_{15}', V_{26}', V_{31}', V_{42}', V_{53}', V_{64}', V_{77}')$ (Sequence-1), the other is $(V_{00}', V_{24}', V_{35}', V_{46}', V_{51}', V_{62}', V_{13}', V_{77}')$ (Sequence-2). The chosen voltage vectors of the D2L inverter and the relationship to the sub-inverters’ voltage vectors for the two sequences are shown in Fig. 7 (a) and (b), respectively. From Fig. 7, it can be found that each of the sectors in D2L inverter can be mapped to a sector in the individual sub-inverters. For instance, in Sequence-1, Sector II of the D2L inverter is formed by $V_{00}', V_{15}', V_{26}$ and $V_{77}'$, it can be mapped to Sector I of VSI-1 (which is formed by $V_0, V_1, V_2$ and $V_7$) and Sector V of VSI-2 (which is formed by $V_0', V_5', V_6$ and $V_7'$). The concrete of the sector mapping in the two sequences are listed in Table 1 and Table 2, respectively. Consequently, the reference voltage vector of the D2L inverter can also be mapped to a pair of reference voltage vectors of the individual sub-inverters. Hence, the modulation process of the D2L inverter can be simplified. The reference voltage vector of the D2L inverter $V_{ref}$ can be decomposed into two reference voltage vectors of VSI-1 and VSI-2 (named $V_{1\_ref}$ and $V_{2\_ref}$) first, and then each of the sub-inverter implements SVPWM with their respective reference voltage vectors.

Before decomposing $V_{ref}$, the magnitude and phase relationship between the $V_{1\_ref}, V_{2\_ref}$ and $V_{ref}$ should be derived first. For the conventional zero ZSV SVPWM strategy, the seven-segment modulation is usually utilized [20]. Taking Sector II in Fig. 7 as example, the seven-segment switching sequence of the two voltage vector sequences are $V_{00}' - V_{35}' - V_{24}' - V_{77}' - V_{35}' - V_{00}'$ (in Sequence-1) and $V_{00}' - V_{15}' - V_{26}' - V_{77}' - V_{26}' - V_{15}' - V_{00}'$ (in Sequence-2), respectively. The switching waveforms of these two sequences are shown in Fig. 8. In the figure, $S_{a1}$, $S_{b1}$, $S_{c1}$ and $S_{a2}$, $S_{b2}$, $S_{c2}$ represent the three-phase switching signals of VSI-1 and VSI-2, respectively; $T_{s}$ represents the switching period; $T_{1}$ represents the dwell time of $V_{15}'$ and $V_{35}'$; $T_{2}$ represents the dwell time of $V_{24}'$ and $V_{26}'$; $T_{0}$ represents the dwell time of the zero vectors; $k_{0}$ is the distribution coefficient of the zero vectors’ dwell time, in which $V_{77}'$ is applied for time $k_{0}T_{0}$, $V_{00}'$ is applied for time $(1-k_{0})T_{0}$, $0 \leq k_{0} \leq 1$. In the conventional zero ZSV SVPWM strategy [20], the dwell time of both the $V_{77}'$ and $V_{00}'$ are equal to $T_{0}/2$ (i.e., $k_{0} = 0.5$). Observing the switching waveforms in Fig. 8, we can find that the switching signals between the two sub-inverters in Sector II satisfy the following relationship

$$S_{a1} = S_{c2}, S_{b1} = S_{a2}, S_{c1} = S_{b2} \text{(Sequence-1)}$$

$$S_{a1} = S_{b2}, S_{b1} = S_{a2}, S_{c1} = S_{a2} \text{(Sequence-2)}$$

(8)
The switching signals in other sectors also satisfy the above relationship, and are not repeated here. Therefore, based on (8), the pole voltages of the two sub-inverters satisfy the following equations:

\[
\begin{align*}
&v_{a1n} = v_{c2n}, v_{b1n} = v_{a2n}, v_{c1n} = v_{b2n} \quad \text{(Sequence-1)} \\
&v_{a1n} = v_{b2n}, v_{b1n} = v_{a2n}, v_{c1n} = v_{b2n} \quad \text{(Sequence-2)}
\end{align*}
\]

(9)

According to (6), (7) and (9), the magnitude and phase relationship between the reference voltage vector \(v_{1\_ref}\), \(v_{2\_ref}\) and \(v_{ref}\) can be deduced and expressed as follows:

\[
\begin{align*}
&V_{1\_ref} = V_{2\_ref}e^{j2\pi/3} \quad \text{(Sequence-1)} \\
&V_{1\_ref} = V_{2\_ref}e^{-j2\pi/3} \quad \text{(Sequence-2)} \\
&V_{1\_ref} = \frac{1}{\sqrt{3}}V_{ref}e^{-j\pi/6} \quad \text{(Sequence-1)} \\
&V_{2\_ref} = \frac{1}{\sqrt{3}}V_{ref}e^{-j5\pi/6} \quad \text{(Sequence-1)} \\
&V_{1\_ref} = \frac{1}{\sqrt{3}}V_{ref}e^{j\pi/6} \quad \text{(Sequence-2)} \\
&V_{2\_ref} = \frac{1}{\sqrt{3}}V_{ref}e^{j5\pi/6} \quad \text{(Sequence-2)}
\end{align*}
\]

(10)

(11)

For the purpose of showing the relationship between \(V_{1\_ref}\), \(V_{2\_ref}\) and \(V_{ref}\) more intuitively, the diagram representation of these three reference voltage vectors based on (10) and (11) are shown in Fig.7. It can be seen that, for the two sequences, the magnitudes of \(V_{1\_ref}\) and \(V_{2\_ref}\) are all equal to the \(1/\sqrt{3}\) times of \(V_{ref}\), and the phase angles between \(V_{1\_ref}\) and \(V_{2\_ref}\) are all 120°. The difference is that \(V_{1\_ref}\) leads \(V_{2\_ref}\) with 120° in Sequence-1, while \(V_{1\_ref}\) lags \(V_{2\_ref}\) with 120° in Sequence-2. In addition, \(V_{ref}\) leads \(V_{1\_ref}\) with 30° and \(V_{2\_ref}\) with 150° in Sequence-1, while \(V_{ref}\) lags \(V_{1\_ref}\) with 30° and \(V_{2\_ref}\) with 150° in Sequence-2.

Assuming that \(v_{d\_ref}\), \(v_{q\_ref}\), \(v_{d1\_ref}\), \(v_{q1\_ref}\) and \(v_{d2\_ref}\), \(v_{q2\_ref}\) are the reference voltage of the D2L inverter, VSI-1 and VSI-2 in dq coordinate, respectively, then:

\[
\begin{align*}
&V_{ref} = v_{d\_ref} + jv_{q\_ref} \\
&V_{1\_ref} = v_{d1\_ref} + jv_{q1\_ref} \\
&V_{2\_ref} = v_{d2\_ref} + jv_{q2\_ref}
\end{align*}
\]

(12)

According to (11), (12) and the Euler formula \(e^{jx} = \cos x + j\sin x\), the decomposition equation from \(v_{d\_ref}\), \(v_{q\_ref}\) to \(v_{d1\_ref}\), \(v_{q1\_ref}\) and \(v_{d2\_ref}\), \(v_{q2\_ref}\) can be derived as:

\[
\begin{align*}
&\begin{bmatrix} v_{d1\_ref} \\ v_{q1\_ref} \\ v_{d2\_ref} \\ v_{q2\_ref} \end{bmatrix} = \begin{bmatrix} 1/2 & -\sqrt{3}/6 & -\sqrt{3}/6 & 1/2 \\ -\sqrt{3}/6 & 1/2 & -\sqrt{3}/6 & 1/2 \\ -\sqrt{3}/6 & -1/2 & -\sqrt{3}/6 & -1/2 \end{bmatrix} \begin{bmatrix} v_{d\_ref} \\ v_{q\_ref} \end{bmatrix} \quad \text{(Sequence-1)} \\
&\begin{bmatrix} v_{d1\_ref} \\ v_{q1\_ref} \\ v_{d2\_ref} \\ v_{q2\_ref} \end{bmatrix} = \begin{bmatrix} 1/2 & -\sqrt{3}/6 & -\sqrt{3}/6 & 1/2 \\ -\sqrt{3}/6 & 1/2 & -\sqrt{3}/6 & 1/2 \\ -\sqrt{3}/6 & -1/2 & -\sqrt{3}/6 & -1/2 \end{bmatrix} \begin{bmatrix} v_{d\_ref} \\ v_{q\_ref} \end{bmatrix} \quad \text{(Sequence-2)}
\end{align*}
\]

(13)

(14)

Therefore, the implementation of the conventional zero ZSV SVPWM can be simplified as follows. First, decomposing the reference voltage of the D2L inverter into two parts of reference voltages with same amplitude and 120° phase difference using (13) or (14). Then, each of the sub-inverters implements the classic SVPWM with one of the obtained two parts of reference voltages. Since the phase difference between the two sub-inverters’ reference voltages is 120°, so the strategy is called 120° phase-shift based SVPWM (PS-SVPWM) strategy.

IV. PROPOSED ZERO-SEQUENCE STEERABLE CBPWM STRATEGY

A. PRINCIPLE OF THE 120° PHASE-SHIFT BASED CBPWM STRATEGY

It is generally known that the classic two-level SVPWM strategy can be equivalently implemented by a carrier-based PWM method [32], [33]. Owing to omitting the complicated sector identification, switching time calculation and lookup table processes, the carrier-based PWM method can reduce the processing time and implement conveniently in engineering. For the PS-SVPWM strategy, since the two sub-inverters still use the classic two-level SVPWM strategy, this modulation strategy can also be implemented equivalently by the carrier-based PWM method. With reference to the methodology proposed in [32], the carrier-based implementation method of the PS-SVPWM strategy, here call it the PS-CBPWM strategy, can be shown as follows.

Step 1: normalizing the \(dq\) reference voltage \(v_{d\_ref}\) and \(v_{q\_ref}\) of the D2L inverter with 0.5\(V_{dc}\) as the base value:

\[
\begin{align*}
&v_{d\_ref} = v_{d\_ref}/(0.5V_{dc}) \\
&q_{q\_ref} = v_{q\_ref}/(0.5V_{dc})
\end{align*}
\]

(15)

where \(v_{d\_ref}\) and \(v_{q\_ref}\) are the normalized \(dq\) reference voltage of the D2L inverter.

Step 2: calculating the normalized \(dq\) reference voltage \(v_{d\_ref}^*\) and \(v_{q\_ref}^*\) of VSI-\(j\) (\(j = 1, 2\)) according to (13) or (14). After that, performing inverse Park and inverse Clarke transformation on \(v_{d\_ref}^*\) and \(v_{q\_ref}^*\), the normalized three-phase reference voltage \(v_{d\_ref}^*\), \(v_{q\_ref}^*\) and \(v_{d\_ref}^*\), \(v_{q\_ref}^*\) of VSI-\(j\) can be obtained.

Step 3: calculating the zero-sequence component \(v_{zsj}\) of VSI-\(j\):

\[
\begin{align*}
&v_{zsj} = -(1 - 2k_0)v_{max} + (1 - k_0)v_{min} \quad \text{(16)} \\
&v_{zsj} = -0.5(v_{max} + v_{min}) \quad k_0 = 0.5 \quad \text{(17)}
\end{align*}
\]

where \(v_{max}\) and \(v_{min}\) are, respectively, the maximum and minimum values among \(v_{d\_ref}^*, v_{q\_ref}^*, v_{max}\) and \(v_{min}\); \(k_0\) is the distribution coefficient of the zero vectors’ dwell time as introduced in Fig. 8, 0 ≤ \(k_0\) ≤ 1.

Step 4: calculating the three-phase modulation signals \(m_{dj}\), \(m_{bj}\) and \(m_{cj}\) of VSI-\(j\) through adding the zero-sequence component \(v_{zsj}\) to the original normalized three-phase reference
vectors \( v_{aj, \text{ref}}^*, v_{bj, \text{ref}}^* \) and \( v_{cj, \text{ref}}^* \):

\[
\begin{align*}
  m_{aj} &= v_{aj, \text{ref}}^* + v_{szj}^* \\
  m_{bj} &= v_{bj, \text{ref}}^* + v_{szj}^* \\
  m_{cj} &= v_{cj, \text{ref}}^* + v_{szj}^* 
\end{align*}
\] (18)

Step 5: comparing the three-phase modulation signals with the triangle-carrier waves, the switching signals of VSI-\( j \) can be obtained.

With the above steps, the PS-CBPWM strategy is implemented.

**B. PRINCIPLE OF THE ZERO-SEQUENCE STEERABLE CBPWM STRATEGY**

In the ideal case, the ZSV caused by modulation can be eliminated with the above PS-CBPWM strategy. But when considering the ZSV caused by the nonlinear factors, such as the dead-time effect, it is not enough to just adopt the above modulation strategy to suppress the ZSC. Thus, modification should be made for the PS-CBPWM strategy.

As mentioned in Section II, the D2L inverter need to generate a certain amount of ZSV to counteract the influence of the nonlinear ZSV disturbance. Generally, the generated ZSV can be controlled by adjusting the dwell time of the zero vectors when modulating the two sub-inverters [22], [26]. Take the situation shown in Fig. 7(a) and Fig. 8(a) (\( V_{\text{ref}} \) is located in Sector II and synthesized by Sequence-1) as example. Assuming that the adjusted dwell times of the zero vectors \( V_0, V_7, V_0' \) and \( V_7' \) are \( t_0, t_7, t_0' \) and \( t_7' \), respectively. According to the volt-second equivalent principle, the CMV generated by VSI-1 and VSI-2 can be expressed as

\[
\begin{align*}
  v_{cm1} T_s &= v_{dc} T_1 + 2 v_{dc} T_2 + v_{dc} T' \\
  v_{cm2} T_s &= v_{dc} T_1 + 2 v_{dc} T_2 + v_{dc} T'
\end{align*}
\] (19)

Subtracting (20) from (19), the ZSV generated by the D2L inverter satisfies the following equation:

\[
v_{\text{pw}0} T_s = (v_{cm1} - v_{cm2}) T_s = v_{dc} (t_7 - t'_7)
\] (21)

The above relationship still holds in other sectors and sequences, and no more expatiation here. It can be seen from (21) that, in order to obtain the desired ZSV, the dwell times between \( V_7 \) and \( V'_7 \) need to maintain a certain difference. Let \( \Delta T = t_7 - t'_7 \), then, with considering that making the two sub-inverters work in the symmetrical state, the adjusted zero vectors’ dwell times \( t_0, t_7, t_0', \) and \( t_7' \) can be expressed as

\[
\begin{align*}
  t'_0 &= t_7 = T_0/2 + \Delta T/2 \\
  t_0 &= t'_7 = T_0/2 - \Delta T/2
\end{align*}
\] (22)

Define \( \Delta k \) as the zero-sequence component adjustment coefficient, and \( \Delta k = \Delta T/T_0 \), then (22) can be rewritten as

\[
\begin{align*}
  t'_0 &= t_7 = 0.5(1 + \Delta k)T_0 \\
  t_0 &= t'_7 = 0.5(1 - \Delta k)T_0
\end{align*}
\] (23)

According to (23), the distribution coefficient of the zero vectors’ dwell time \( k_0 \) for VSI-1 and VSI-2 are adjusted as

\[
\begin{align*}
  k_0 &= 0.5(1 + \Delta k) \quad \text{for VSI-1} \\
  k_0 &= 0.5(1 - \Delta k) \quad \text{for VSI-2}
\end{align*}
\] (24)

Then, the zero-sequence component \( v_{sz}^* \) of VSI-\( j \) expressed in (16) should be modified as

\[
\begin{align*}
  v_{sz1}^* &= \Delta k - 0.5(1 + \Delta k)v_{\max 1}^* - 0.5(1 - \Delta k)v_{\min 1}^* \\
  v_{sz2}^* &= -\Delta k - 0.5(1 - \Delta k)v_{\max 2}^* - 0.5(1 + \Delta k)v_{\min 2}^*
\end{align*}
\] (25)

Similarly, take the case that \( V_{\text{ref}} \) is located in Sector II and synthesized by Sequence-1 for example, the effect of adjusting the zero vectors’ dwell time (or \( \Delta k \)) for the proposed ZSS-CBPWM. (a) Increasing the dwell time of \( V_j \) by 0.5\( \Delta k T_0 \) for VSI-1. (b) Decreasing the dwell time of \( V_j \) by 0.5\( \Delta k T_0 \) for VSI-2. (c) The ZSV generated by the D2L inverter.
and same amplitude of $v_{dc}/3$ for each pulse in one switching period. The mean of the ZSV in one switching period is $[6 \times (v_{dc}/3) \times 0.5 \Delta k T_0]/T_s = \Delta k T_0 v_{dc}/T_s$, which is consistent with (21).

Therefore, with the above modifications, the zero-sequence component of the PS-CBPWM strategy is steerable. It can be steered by adjusting $\Delta k$ to obtain a desired ZSV. According to this characteristic, the modified scheme can be called as zero-sequence steerable PS-CBPWM strategy, or ZSS-CBPWM strategy for short. Synthesize the above analysis, it is easy to see that the proposed ZSS-CBPWM strategy is actually a carrier based equivalent implementation of the conventional ZSS-SVPWM strategy proposed in [22], [29], [30]. The realization process of the proposed ZSS-CBPWM strategy can be drawn and shown in Fig. 10. Obviously, the required operations of the PS-CBPWM strategy are simple and easy to be implemented than the ZSS-SVPWM strategy.

![ZSS-CBPWM Strategy](image)

**FIGURE 10.** Realization process of the proposed ZSS-CBPWM strategy.

### C. EFFECTIVE MODULATION RANGE ANALYSIS

Similar to other ZSC suppression modulation strategies [26], [28], the proposed ZSS-CBPWM strategy also has an effective modulation range. The ZSC can only be suppressed completely when the modulation index of the D2L inverter is within a certain range. This modulation index range need to be identified because it determines the range of the inverter DC voltage, which is also the MPPT operation voltage range of the OEWT-DI based PV grid-tied system.

According to (21), the effective range (represented by maximum and minimum value) of the ZSV generated by the D2L inverter can be deduced as

$$(v_{pwm})_{\text{max}} | (t_1 = T_0, \ t_0 = 0) = \frac{1}{T_s} v_{dc}(t_1 - t_0) = \frac{T_0}{T_s} v_{dc} \tag{27}$$

$$(v_{pwm})_{\text{min}} | (t_1 = 0, \ t_0 = T_0) = \frac{1}{T_s} v_{dc}(t_1 - t_0) = -\frac{T_0}{T_s} v_{dc} \tag{28}$$

It can be found from (27) and (28) that, if the switching frequency is selected, the generated ZSV range is proportional to the zero vector’s dwell time $T_0$ and the DC voltage $v_{dc}$. Obviously, if $T_0$ is equal to zero, there is no adjustment margin for generating the desired ZSV and the ZSC will exist inevitably.

Define the D2L inverter’s modulation index $m$ as $m = V_{\text{ref}} / ((2\sqrt{3}/3)v_{dc}) [26]$, the situation that $T_0$ has the minimum value (referred as $T_{0, \text{min}}$) occurs when $V_{\text{ref}}$ is in the middle of each sector, and when $T_{0, \text{min}} = 0$, the modulation index has the maximum value and equals to 0.866. Then the modulation index $m$ can also be expressed as

$$m = 0.866(1 - T_{0, \text{min}}/T_s) \tag{29}$$

So $m$ must be less than a certain value to make the value of $T_{0, \text{min}}$ sufficient to generate the desired ZSV. To derive the maximum value of $m$, the minimum value of $T_{0, \text{min}}$ should be derived first. In the OEWT-DI based PV grid-tied system, the dominate nonlinear ZSV disturbance is the ZSV caused by dead-time effect. The value of this ZSV has been derived in detail in [25] and the mean of the ZSV in each switching period (named as $v_{0, dt}$) is expressed as

$$v_{0, dt} = \begin{cases} \frac{2v_{dc}T_d}{3T_s} - \frac{2v_{dc}T_d}{3T_s} \\ \frac{2v_{dc}T_d}{3T_s} \end{cases} \tag{30}$$

where $T_d$ is the dead-time of the D2L inverter. $v_{0, dt}$ has two different values, which is related to the three-phase current mode [25].

Thus, in order for the D2L inverter to generate enough ZSV to counteract the ZSV caused by dead-time effect, $T_{0, \text{min}}$ should satisfies the following relationship:

$$\frac{T_{0, \text{min}}}{T_s} v_{dc} \geq \frac{2v_{dc}T_d}{3T_s} \tag{31}$$

Then

$$T_{0, \text{min}} \geq \frac{2T_d}{3} \tag{32}$$

Accordingly, the effective modulation range of the proposed ZSS-CBPWM strategy can be deduced as

$$m \leq 0.866 \left[ 1 - \frac{2T_d}{3T_s} \right] \tag{33}$$

From (33), it can be seen that the effective maximum modulation index of the proposed ZSS-CBPWM is 0.866 $[1 - 2T_d/(3T_s)]$. Therefore, for a specific OEWT-DI based PV grid-tied system, when the switching frequency and the dead-time are selected, the effective maximum $m$, under which the ZSC can be completely suppressed, is then determined. As a result, the minimum DC voltage (or the lower limit value of the MPPT operation voltage) of the D2L inverter is also determined. In addition, it’s worth noting that the dead-time effect also cause voltage deviation effect on the inverter output fundamental voltage [34]. So for compensating this deviation effect, the lower limit value of the DC voltage need to choose slightly larger than the value calculated by (33).
B. Wang et al.: Zero-Sequence Steerable CBPWM Strategy for Eliminating ZSC of OEWT-DI Based PV Grid-Tied System

V. OEWT-DI CONTROL METHOD BASED ON THE ZSS-CBPWM STRATEGY

In the OEWT-DI control system, for suppressing the ZSC, a ZSC control loop should be added to regulate the zero-sequence component adjustment coefficient $\Delta k$. The reference $i_{0,\text{ref}}$ of the ZSC control loop is set as zero, and the feedback $i_0$ is calculated as one third of the sum of sampled three-phase inverter-side currents. Considering that the major component of the ZSC is third-order harmonic and its frequency usually fluctuates with the fluctuation of the grid frequency, the quasi-PR regulator is more suitable to be used to eliminate the control loop tracking error. Therefore, the control function of the ZSC control loop can be expressed as

$$\Delta k = \left( K_p + \frac{K_i \omega_c s}{s^2 + 2\omega_c s + \omega^2_r} \right) (i_{0,\text{ref}} - i_0) \quad (34)$$

where $K_p$ and $K_i$ are the proportional and resonant gains of the quasi-PR regulator, respectively; $\omega_c$ is the resonant frequency and selected as the three times of the grid frequency; $\omega_r$ is the cutoff frequency which determines the control bandwidth of the regulator, and can be selected as 2–5 rad/s [26].

With the above ZSC suppression method, the proposed overall control scheme for the OEWT-DI based PV grid-tied system is shown in Fig. 11. The control scheme consists of four parts: DC voltage control loop, phase lock loop (PLL), current control loop and the ZSS-CBPWM strategy. The DC voltage loop aims at regulating the DC voltage to the MPP voltage and generate the reference active current $i_{d,\text{ref}}$. Due to the presence of step-up transformer in the system, the three-phase capacitor voltage $v_{ca}$, $v_{cb}$ and $v_{cc}$ are easier to be sampled than the grid voltage, so they are used to implement the PLL to get the system angle $\theta$. The current control loop includes the active current control loop, reactive current control loop and the aforementioned ZSC control loop, which are used to achieve the active and reactive power control as well as the ZSC suppression for the system. The ZSS-CBPWM strategy is implemented to generate the inverter switch signals.

VI. EXPERIMENTAL RESULTS

A. EXPERIMENTAL SYSTEM DESCRIPTION

The experimental platform based on a 30kW OEWT-DI prototype is shown in Fig. 12. The control algorithm is implemented on a control board based on a TMS320F28377 DSP processor. The PV array is simulated by a DC source (650V) with a 0.8 series resistor. For the OEWT transformer, the primary side is configured as open-end and the secondary side is connected in delta, the phase voltage ratio is 364V/380V, and the impedance voltage is about 2.5%, which equivalent to 1mH leakage inductance. Other system parameters are given in Table 3. In addition, the experimental waveforms are measured by the FLUKE i400s current probe and displayed on the Yokogawa DLM2024 oscilloscope.

TABLE 3. System parameters.

| Symbol | Parameter | Value |
|--------|-----------|-------|
| $i_{nv}$ | Rated inverter-side current | 27.5A |
| $i_i$ | Rated grid-side current | 45.5A |
| $v_3$ | Grid voltage | 380V |
| $f_s$ | Grid frequency | 50Hz |
| $f_i$ | Switching frequency | 5kHz |
| $f_{imp}$ | Sampling frequency | 10kHz |
| $T_d$ | Dead time | 3μs |
| $L_i$ | Inverter-side inductance | 3.6mH |
| $L_t$ | Transformer leakage inductance | 1mH |
| $C$ | Filter capacitance | 11μF |

B. EXPERIMENTAL RESULTS

To validate the performance of the proposed strategy, both the steady-state and dynamic experiments are performed on the above experimental platform. For the steady-state performance, as a comparison with the proposed strategy, the PS-CBPWM strategy and the ZVR SVPWM strategy (with a ZSC PR controller) [26] are also tested on the experimental system. The experimental three-phase inverter-side current ($i_a$, $i_b$, $i_c$) and ZSC ($i_0$) waveforms at rated power for the three strategies are, respectively, shown in Fig. 13(a)–15(a), and the corresponding fast Fourier transform (FFT) analysis

FIGURE 11. Overall control scheme for the OEWT-DI based PV grid-tied system with common DC bus.
results of the inverter-side current are, respectively, shown in Fig. 13(b)–15(b).

From Fig. 13(a) and (b), it can be seen that a rich low-frequency ZSC harmonics (mainly the triple harmonics) are exist in the inverter-side current as controlled with the PS-CBPWM strategy. For instance, the 3th harmonic accounts for up to 9% of the fundamental component, which seriously affected the current quality. The experimental results verify that using the modulation strategy, which can only eliminate the ZSV produced by modulation, cannot suppress the ZSC effectively.

As controlled with the ZVR SVPWM strategy, it can be found from Fig. 14(a) and (b) that the inverter-side current contains a large amount of high-frequency ZSC harmonic. The amplitude of the ZSC is up to about 10A (25% of the fundamental amplitude). The experimental results show that due to the low zero-sequence inductance in the OEWT-DI system, the adoption of the strategy which mainly consider the suppression of low-frequency ZSV cannot effectively suppress the ZSC as well.

With the experiment results shown in Fig. 15(a) and (b), it comes to that both the low- and high-frequency ZSC are effectively suppressed when using the proposed ZSS-CBPWM strategy. Compared with the PS-CBPWM strategy, the 3th harmonic content is reduced from 9% to about 0.33%, which is a very low value. Compared with the ZVR SVPWM strategy, the amplitude of the ZSC is reduced from 10A to about 2A, a decrease of nearly 80%. The above experiments show the better stead-state performance of the proposed ZSS-CBPWM strategy than the other strategies.

Actually, the experiment with the conventional ZSS-SVPWM strategy is also made in the laboratory, they are not presented in the paper because the experiment results show no notable difference with using ZSS-CBPWM strategy. The difference between these two strategies is the ZSS-CBPWM strategy requires less program processing time than the ZSS-SVPWM strategy.

For researching the dynamic performance of the proposed strategy, the step-response experiments are made. Fig. 16 shows the experimental results before and after
enabling the ZSC controller of the ZSS-CBPWM strategy. It can be seen that the ZSC is effectively suppressed when enabling the ZSC controller. Fig. 17 shows the dynamic experimental results from half rated power to rated power (50% step rated power change) with the ZSS-CBPWM strategy. One can find that the inverter-side current can follow the reference well, and the ZSC can keep in a satisfactory range with the power step change. The experiment results prove good dynamic performance of the proposed strategy.

VII. CONCLUSION

To suppress the ZSC in the OEWT-DI based PV grid-tied system, this paper first established the ZSC model of the system and analyzed the characteristics of the zero-sequence equivalent circuit. With consideration that the three-phase three-limb inductor, which has a small zero-sequence inductance, is usually adopted as the filter inductor in the selected PV system, the analysis shows that both the low- and high-frequency ZSV should be reduced for suppressing the ZSC. For this reason, a ZSS-CBPWM strategy is proposed in the paper. The strategy using the 120° phase-shift based PWM method to eliminate the major ZSV disturbance caused by the modulation, then introduces a coefficient $\Delta k$ to adjust the output ZSV of dual-inverter to counteract other ZSV disturbances. The strategy can be regarded as a carrier equivalent implementation of the conventional ZSS-SVPWM strategy, but it is easier to be implemented in the DSP controller.

Furthermore, the effective modulation range of the proposed strategy, which determines the lower limit of the DC voltage, is also investigated. This range is related to the system switching frequency as well as the dead-time, and the ZSC can only be effectively suppressed when the modulation index is within the range.

The steady-state and dynamic experimental results show the effectiveness of the proposed strategy, what’s more, it has better steady-state performance compared to the PS-CBPWM and ZVR SVPWM strategy.

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