MPNA: A Massively-Parallel Neural Array Accelerator with Dataflow Optimization for Convolutional Neural Networks

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Abstract—The state-of-the-art accelerators for Convolutional Neural Networks (CNNs) typically focus on accelerating only the convolutional layers, but do not prioritize the fully-connected layers much. Hence, they lack a synergistic optimization of the hardware architecture and diverse dataflows for the complete CNN design, which can provide a higher potential for performance/energy efficiency. Towards this, we propose a novel Massively-Parallel Neural Array (MPNA) accelerator that integrates two heterogeneous systolic arrays and respective highly-optimized dataflow patterns to jointly accelerate the convolutional (CONV) and the fully-connected (FC) layers. Besides fully-exploiting the available off-chip memory bandwidth, these optimized dataflows enable high data-reuse of all the data types (i.e., weights, input and output activations), and thereby enable our MPNA to achieve high energy savings. We synthesized our MPNA architecture using the ASIC design flow for a 28 nm technology, and performed functional and timing validation using multiple real-world complex CNNs. MPNA achieves 149.7 GOPS/W at 280 MHz and consumes 230 mW. Experimental results show that our MPNA architecture provides 1.7× overall performance improvement compared to state-of-the-art accelerator, and 51% energy saving compared to the baseline architecture.

I. INTRODUCTION

Machine learning has rapidly proliferated into different field of life ranging from automotive and smart environments to medicine. Due to their high accuracy, larger and deeper Convolutional Neural Networks (CNNs) have become the key technology for many applications like advanced vision processing. However, it comes at the cost of significant computational and energy requirements, and thus, requiring specialized accelerator-based architectures.

A. State-of-the-Art and Their Limitations

Plenty of work has been carried out in designing CNN accelerators [1], which mostly focus on un-structurally sparse neural networks like EIE [2], SCNN [3] and Convlin [4]. The EIE and SCNN architectures make use of both sparsity in weights and activations for accelerating the networks, while Convlin exploits sparsity in activations only. The sparsity in activations usually comes from converting all the negative activations to zeros in the Rectified Linear Unit (ReLU), as used in these designs. However, the above accelerators cannot efficiently handle advanced activation functions like Leaky-ReLU that do not result in high sparsity to help the training process [5]. Tensor Processing Unit (TPU) [6], DaDian-Nao [7] and Eyeriss [8] architectures accelerate dense neural networks, and can also be modified to provide support for structurally sparse networks [9]. Although these architectures show good performance in terms of latency for the convolutional (CONV) layers, they offer very limited acceleration for the fully-connected (FC) layers, as we will show with the help of a motivational case study in the following.

B. Motivational Case-Study

To achieve high performance and power/energy efficiency, state-of-the-art CNN accelerators exploit the reuse of activations, weights and partial sums, thereby increasing the data locality and reducing the number of off-chip memory accesses [9]. In this respect, the conventional systolic array-based designs (like Google’s TPU [6]) render very effective, because each Processing Element (PE) in the Systolic Array (SA) performs three key tasks. (1) It receives data from their upstream neighbor(s). (2) It performs the basic multiply-and-accumulate (MAC) operation(s). (3) It passes the data along with the partial result(s) to their downstream neighbor(s). Hence, for computations that involve both activation and weight reuse (i.e., CONV layer), the overall speedup of these systolic arrays is significant as shown in Fig. 1 for AlexNet [10]. However, in case of only activation reuse — i.e., where one single input...
A Convolutional layer receives the data from the inputs or the preceding layer, and performs the convolution operation on each input and a filter to generate the output feature map. A CNN mainly consists of these sections: (1) Convolutional, for extracting features; (2) Fully-Connected, for classification; (3) Activation, for introducing non-linearity; and (4) Pooling, for sub-sampling. Among these layers, the convolutional (CONV) layers are the most computationally intensive, while the fully-connected (FC) layers are the most memory intensive ones. Fig. 3 shows this observation using the percentage of weights and MAC operations required for the CONV and FC layers in the AlexNet and VGG-16 networks.

A convolutional layer can accelerate both CONV and FC layers without incurring significant area and power/energy overheads compared to the baseline architecture. MPNA achieves 149.7 GOPS/W performance efficiency at 280 MHz and consumes 239 mW.

II. PRELIMINARIES

Before proceeding further, first, we present basics of CNNs, which are necessary to understand the contributions in the later sections.

Neural networks are composed of various layers, which are connected in cascade. Each layer receives some input from the preceding layer, performs certain operations, and forwards the result to the succeeding layer. A CNN mainly consists of these layers: (1) Convolutional, for extracting features; (2) Fully-Connected, for classification; (3) Activation, for introducing non-linearity; and (4) Pooling, for sub-sampling. Among these layers, the convolutional (CONV) layers are the most computationally intensive, while the fully-connected (FC) layers are the most memory intensive ones.

A convolutional layer receives the data from the inputs or the preceding layer, and performs the convolution operation.
using several filters to obtain several output feature maps, each corresponding to the output of one filter. Fig. 3 shows a detailed illustration of a single convolutional layer. Here, $IF^j$ is the $i^{th}$ 2D input feature map, $OF^j$ is the $j^{th}$ 2D output feature map, $F_{ij}$ is the 2D kernel of a filter between $IF^i$ and $OF^j$. The term $OF^j(m,n)$ denotes the activation at location $(m,n)$ of the $j^{th}$ output feature map, i.e., $OF^j$. Similarly, $F_{ij}(p,q)$ denotes the weight/synapse at location $(p,q)$ in the 2D filter kernel between $IF^i$ and $OF^j$. Let’s consider convolutional stride = 1, unless stated otherwise. The FC layers can be considered as a special case of CONV layers where the input and output is a 1D array and, therefore, can be represented by the above terminologies.

III. METHODOLOGY FOR DESIGNING DNN ACCELERATORS

Our methodology for designing optimized DNN accelerator-based architectures is shown in Fig. 4. It consists of the following key steps, which are explained in detail in the subsequent sections.

![Diagram of DNN Accelerator Methodology](image)

**Fig. 4:** Overview of our MPNA design methodology showing key steps.

1) Analyze different data-reuse techniques, which can be exploited for energy- and performance-efficient execution of a given DNN on the hardware accelerator.

2) Design and optimize individual hardware components for all the elementary functions required for the DNN execution.

3) Design area and power/energy-efficient processing arrays as key accelerator units, which can support the most effective types of dataflow/parallelism for high-performance execution of all the computational layers of a given DNN.

4) Devise an optimized hardware configuration considering key architectural parameters like the size and number of processing arrays, interconnect of components affecting the supported dataflows, on-chip buffers, data reuse and memory organization considering the available DRAM bandwidth.

5) Define highly efficient dataflows for reducing the total number of DRAM accesses required for the DNN inference.

6) Synthesis of the complete hardware architecture for detailed benchmarking for area, performance/throughput, and power/energy consumption considering different DNN configurations.

A. Computational Complexity and Data-Reuse Analysis

The CNN complexity can be estimated by analyzing the number of computations required for the CONV and FC layers. Fig. 5 illustrates the pseudocode of the CNN layer execution. Here, $I$ and $J$ define the number of input and output feature maps; $M$ and $N$ define the number of rows and columns in the output feature maps; and $P$ and $Q$ define the number of rows and columns in filter kernels. These parameters can be used to define other parameters, like the number of filters can be derived from $J$.

![Pseudocode of CNN Layer Execution](image)

**Fig. 5:** Pseudocode for the processing of CONV layers.

Table 1 shows the number of MAC operations required for each CONV and FC layer of the AlexNet and VGG-16 networks. Fig. 6a and c show the weights-, input activations-, and output activations-reuse factor for the AlexNet and VGG-16, respectively. The **data-reuse factor** defines the number of MAC operations in which a specific data is used. It can be observed form the figures that the data reuse pattern can mainly be classified into two main categories: (1) CONV layers, where all types of data has significant reuse factor, and (2) FC layers, where per sample weight-reuse is 1. This classification is also supported by the fact that the CONV layers are more computationally intensive and the FC layers are more memory intensive, as shown in Fig. 6b. These observations along with the data-reuse pattern is exploited in section IV and VI for designing a novel architecture that can maximally benefit from the data-reuse and a dataflow to reduce the number of off-chip memory accesses, respectively.

**TABLE I: Number of MACs per input sample and weights in the AlexNet and VGG-16.**

| Observation | # of MACs/Sample | # of Weights |
|-------------|------------------|--------------|
| CONV        | 58,623M          | 58,623M      |
| FC          | 123,632M         | 123,632M     |

IV. THE MPNA ARCHITECTURE

Fig. 7 presents the top-level view of our MPNA architecture with detailed components, as discussed in the subsequent subsections.

A. Overview of our MPNA Architecture (Fig. 7A)

The MPNA architecture is composed of two heterogeneous systolic arrays, an accumulation unit, a pooling & activation unit, on-chip data and weight buffers, a control unit, and connectivity to DRAM. Each systolic array is specialized to support specific types of data parallelism for accelerating a specific set of configurations of computational layers while incurring minimum overheads. The systolic arrays receive data and weights from on-chip buffers, perform MAC operation,
and forward the resultant partial sums to the accumulation block. The accumulation block is meant to hold the partial outputs while rest of their corresponding partial outputs are being computed, which are also then accumulated together inside the accumulator block. Once the output is complete, the accumulator block forwards the output(s) to the subsequent block for pooling and activation operation, or sends it back to the on-chip data buffer. The data is then either used for the next layer or is moved to the DRAM until rest of the intermediate operations are completed.

### B. Heterogeneous Systolic Arrays (Fig. 7B-D)

Based on the observations of Fig. 6 in Section III-A, we conclude that there is a need for two heterogeneous systolic arrays for processing different types of layers in a given CNN.

**Systolic Array for the Convolutional Layers (SA-CONV, Fig. 7B-C):** Following the advanced architectural trends in DNN systolic arrays like [6], we design the CONV systolic array that can also exploit the activation (input data), weight, and partial sum reuse. Our SA-CONV integrates a massively parallel array of Processing Elements (PEs) for dense MAC processing. Each PE receives the activations (input data) from its neighboring-left PE, and weights and partial sum from the neighboring-top PE, and passes the output to its downstream neighbor. The left-most PEs in the array receive data from the input buffers and the top-most PEs receive weights from the weight buffer. The processed data is then forwarded to the accumulation block by the bottom-most PEs. Such a systolic array enforces to have weights from the same filter/neuron to be mapped on the same column of the array, while the weights that are to be multiplied with the same input activations to be mapped on parallel columns. This enables high activation and weight reuse.

To support parallel weight movement during computation, we proposed to include an additional register that can hold the weight values while the values which are to be used in the next iteration can be moved to their respective locations. This significantly reduces the initialization time of the systolic array.

**Systolic Array for the Fully-Connected Layers (SA-FC, Fig. 7C-D):** As also supported by the studies of [6] for convolutional accelerators, the SA-CONV can provide significant throughput for multi-batch processing (with larger batch sizes), provided a reasonable size of on-chip memory. However, this can significantly affect the latency of DNN inference which is an important parameter for almost all the real-world applications. To support such scenarios, we propose a novel systolic array architecture (SA-FC), which can accelerate both the CONV and the FC layers for **smaller batch sizes** as well. The design is based on the observation that the weight reuse factor-per-sample in all the FC layers is 1, as shown in Fig. 6b and c. This makes the SA-CONV ineffective as highlighted in Section III-A. However, the overall bandwidth required for such cases is huge, especially for larger DNNs. Therefore, our proposed systolic array SA-FC can be time-multiplexed for processing bandwidth intensive FC and computational intensive CONV layers. Towards generalization, it can also be effectively used for multi-batch processing while incurring minimum area and power overheads when compared to SA-CONV. However, integrating both SA-FA and SA-CONV is a better design option w.r.t. the area, performance, and power/energy efficiency as we will show in the results section. Fig. 7D shows that, unlike in SA-CONV, the SA-FC has dedicated connections from the weight buffer to each individual PE. This enables the system to update the weights in PEs at every clock cycle, and thereby providing the capability to support high-performance execution of the FC layers. The supporting dataflow for the SA-FC is illustrated in Fig. 8.

### C. Accumulation Unit (Fig. 7E)

It is composed of several sub-units (equal to the total number of columns in SA-CONV and SA-FC) to support parallel processing. Each sub-unit is composed of a Scratch-Pad-Memory (SPM) for storing the partial output activations generated by the systolic arrays, and an adder for the accumulation of incoming partial sums with the stored values. Once the output activations are complete, the values are forwarded to the succeeding pooling and activation block for further processing.

### D. Pooling and Activation Unit (Fig. 7F-I)

After the CONV and FC layers, the activation function is employed followed by a pooling layer that reduces the size of the feature maps for subsequent layers. The MPNA provides support for the state-of-the-art MaxPooling, which is deployed in almost all the modern DNNs. Since the activation functions are typically monotonically increasing functions, they can be moved after the pooling operation to curtail the number activation functions to be performed and to reduce the hardware complexity. Figs. 7F-H show that this block consists of an SPM to hold the intermediate pooling results, and a pooling and activation computation module. The MPNA architecture currently supports two of best activation functions.

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**Fig. 6:** Computing and Data-reuse statistics of the AlexNet and VGG-16.

| Layer       | # of MACs | # of Weights | Percentage |
|-------------|-----------|--------------|------------|
| CONV        | 50176     | 2305         | 100%       |
| FC          | 50176     | 2305         | 100%       |
| CONV        | 12544     | 2305         | 100%       |
| FC          | 1152      | 2305         | 100%       |
| CONV        | 3136      | 2305         | 100%       |
| FC          | 784       | 2305         | 100%       |
| CONV        | 4608      | 2305         | 100%       |
| FC          | 4609      | 2305         | 100%       |

**Fig. 7B:** Systolic Array for the Convolutional Layers (SA-CONV).

**Fig. 7C:** Systolic Array for the Fully-Connected Layers (SA-FC).

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This significantly reduces the initialization time of the systolic array.
which are commonly used in DNNs (i.e., ReLU and Leaky-ReLU [11]).

V. DATAFLOW OPTIMIZATION

To effectively use the memory (both on-chip and off-chip) and the compute capabilities of our architecture, we propose a set of dataflows (Fig. 9) that can be employed depending on the configuration of the CONV and FC layers. To explain this, we first present the types of data-reuse and their dependencies on different data.

A. Data-reuse and Their Dependencies

- **Input Activation-Reuse** is the number of times an input activation is used by the same filter multiplied by the number of filters in a layer. To fully exploit this reuse, all the weights (i.e., $F^i_j$ where $i$ represents the feature map index of the input activation) and the corresponding output activations should be available for each available input sample.
- **Output Activation-Reuse** is defined by the number of times partial sums are added into an output activation which are determined by the size of the filters in a layer. To fully exploit this reuse, all the input activations and weight values corresponding to the output activation should be available.
- **Weight-Reuse** is given as the number of times a weight value is used in the computation of a layer which equals the size of $OF_j$. To exploit this completely, all the input activations and the corresponding $OF^j$ map should be available on chip.

B. Possible Scenarios and Corresponding Dataflows (Fig. 9)

Case 1: All input and output activations, and a set of weights ($K \times L$) that has to be uploaded in the processing array in the next stage can be stored on-chip. Here, $K$
and $L$ represents the number of rows and columns in the systolic array. Also, the output activations in one OF can be accommodated in the SPM of a single accumulation sub-unit. In this case, we can avoid input and output activation movement to DRAM and will fetch the weights once only. This is very effective for the later CONV layers where the total size of the input and output activation maps is small, and the number of filter parameters is huge.

**Case 2:** All input and output activations can be completely stored in on-chip data buffer. The output activations in one OF cannot be accommodated in the SPM of a single accumulation sub-unit. In this case, if the overall weight buffer allows to accommodate $L$ (or $2\times L$) complete filters, we partition the input feature maps into multiple blocks to fit the output channels in SPMs, as shown in Fig.9.

**Case 3:** The Input and output activations cannot be completely stored on-chip. In this case, we give preference to input activations if they can be completely stored, and hence the Case 1 can be used while moving the resultant outputs to off-chip memory.

**Case 4:** For all other cases, the best-possible configuration for partitioning data is selected using the methodology proposed in [15] with following constraints: (1) The set of filters being processed together should be a multiple of $L$. (2) The number of weights selected from each filter at one time should be a multiple of $K$.

**C. Observations and Hardware Configurations**

We analyzed the configuration of the AlexNet [10] and defined our hardware configuration (shown in Table II) on the following observations.

- The OF of CONV3 till CONV5 (i.e., last three CONV layers) should fit in SPM of the accumulation, and the pooling and activation units. Since the size of OFs in these layers is $13\times13$, we selected SPM which can hold up to 256 elements.
- For holding the input & output activations of CONV3 till CONV5 layers of the AlexNet on-chip, we selected a 256KB data buffer for two systolic arrays, i.e., greater than four times $13\times13\times384$ which is the size of the activation maps of CONV4.
- Systolic array of size $8\times8$, which provides significant parallelism while not requiring much off-chip memory bandwidth.

**TABLE II: MPNA Hardware Configurations.**

| Module | Description |
|--------|-------------|
| Systolic Arrays | Size of SA-CONV = 8x8 of PEs |
| Systolic Arrays | Size of SA-FC = 8x8 of PEs |
| SPM | Size of SPM in each sub-unit of Accumulation block and Pooling & Activation block = 256B |
| Weight Buffer | Size of weight buffer = 256KB |
| Data Buffer | Size of weight buffer = 256KB |
| DRAM | Bandwidth of DRAM = 12.8GB/s |

**VI. Evaluation Methodology (Fig. 10)**

We developed a fully functional simulator to model the behavior of the MPNA. It is integrated with CACTI 7.0 [12] for memory models and respective area, power, and energy estimation. The complete MPNA architecture is also designed in RTL and synthesized for a 28nm technology using Synopsys design tools. We used ModelSim for logic simulation for functional and timing validations, and obtained the critical path delay, area, and power afterwards. We compared our SA-FC architecture with SA-CONV, and our MPNA with conventional systolic array based accelerators (as baselines), for size of $2\times2$, $4\times4$, and $8\times8$ using AlexNet. We also compared our MPNA with several state-of-the-art accelerators such as Eyeriss [13], SCNN [3], and FlexFlow [14].

**VII. Experimental Results and Discussion**

**Systolic Array:** We compared our SA-FC and SA-CONV to get the profile of the proposed SA-FC in terms of area and power. Fig.11 shows that the SA-FC incurs insignificant area and power overhead (2.1% and 4.4%, respectively) compared...
to SA-CONV. Fig. [12] shows that SA-FC achieves 8.1× speed-up, compared to when only using the SA-CONV for FC layers, due to its microarchitectural enhancements that can provide the data timely to PEs for generating results each clock cycle.

Key Observations for Performance Evaluation (Figs. [12]-d):

- Our MPNA achieves 1.4× – 7.2× higher speed-up for AlexNet compared to the conventional systolic array-based architectures. These improvements come from the parallelism of heterogeneous computing arrays and efficient dataflows.
- Compared to FlexFlow [14], our MPNA requires 53% less number of memory accesses (Fig. [12]-d) due to our optimized dataflows, leading to significant performance and energy improvements.
- Compared to Eyeriss [8], our MPNA achieves 1.7× better latency for CONV layers, as well as significant speedup for FC layers (see Fig. [12]-d), while Eyeriss does not disclose their latency results for the FC layers.
- Further comparison of MPNA with the state-of-the-art accelerators is summarized in Table III showing competitive characteristics of our MPNA for full CNN acceleration.

Key Observations for Power/Energy Evaluation (Figs. [12]-g):

- MPNA consumes 239mW average power, which is dominated by pooling and activation unit due to its local memories and activation function processing.
- MPNA achieves overall 51% of energy reduction compared to baseline architecture (Fig. [12]-d) due to reduced memory access and maximal data-reuse as a result of optimized dataflows.

Key Observations for Area Evaluation (Figs. [12]): The area of MPNA (2.34mm²) is occupied by computational parts (1.38mm²) and on-chip memories (0.96mm²) comprising data and weights buffers. Table III shows that our MPNA consumes a competitively small area compared to other state-of-the-art accelerators.

VIII. CONCLUSION

In this work, we demonstrate that a significant speedup for both CONV and FC layers can be achieved by a synergistic design methodology encompassing dataflow optimization, diverse types of data-reuse and the MPNA architecture with heterogeneous systolic arrays and specialized buffers. The complete architecture is synthesized in a 28nm technology with ASIC design flow, and a comprehensive evaluation is done for area, performance, power, and energy, showing significant gains of our approach over various state-of-the-art. Our novel concepts and open-source hardware would enable further research on accelerating emerging DNNs (like Capsule neural networks).

**TABLE III: Comparison of the state-of-the-art accelerators.**

| Reference | Eyeriss [8] | SCN [1] | FlexFlow [14] | MPNA (this work) |
|-----------|-------------|---------|---------------|-----------------|
| Technology (nm) | 65 | 16 | 65 | 28 |
| Precision (fixed-point) | 16-bit | 16-bit | 16-bit | 8-bit |
| # PEs | 168 | 64 | 256 | 128 |
| On-chip Memory (KB) | 181.3 | 1024 | 84 | 288 |
| Area (mm²) | 12.25 | 7.9 | 3.89 | 2.34 |
| Power (mW) | 27.8 | NA | ∼1000 | 239 |
| Frequency (MHz) | 100-250 | 1000 | 1000 | 280 |
| Performance (GOPS) | 23.1 | NA | 420 | 35.8 |
| Efficiency (GOPS/W) | 83.1 | NA | 305-500 | 149.7 |
| Acceleration Target | CONV | CONV | CONV+FC | CONV |

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