Energy-Efficient Accelerator Design for Deformable Convolution Networks

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Abstract—Deformable convolution networks (DCNs) proposed to address the image recognition with geometric or photometric variations typically involve deformable convolution that convolves on arbitrary locations of input features. The locations change with different inputs and induce considerable dynamic and irregular memory accesses which cannot be handled by classic neural network accelerators (NNAs). Moreover, bilinear interpolation (BLI) operation that is required to obtain deformed features in DCNs also cannot be deployed on existing NNAs directly. Although a general purpose processor (GPP) seated along with classic NNAs can process the deformable convolution, the processing on GPP can be extremely slow due to the lack of parallel computing capability.

To address the problem, we develop a DCN accelerator on existing NNAs to support both the standard convolution and deformable convolution. Specifically, for the dynamic and irregular accesses in DCNs, we have both the input and output features divided into tiles and build a tile dependency table (TDT) to track the irregular tile dependency at runtime. With the TDT, we further develop an on-chip tile scheduler to handle the dynamic and irregular accesses efficiently. In addition, we propose a novel mapping strategy to enable parallel BLI processing on NNAs and apply layer fusion techniques for more energy-efficient DCN processing. According to our experiments, the proposed accelerator achieves orders of magnitude higher performance and energy efficiency compared to the typical computing architectures including ARM, ARM+TPU, and GPU with 6.6% chip area penalty to a classic NNA.

Index Terms—Deformable Convolution Network, Neural Network Accelerator, Irregular Memory Access, Runtime Tile Scheduling

I. INTRODUCTION

Deformable convolution network (DCN) [1], a new category of neural networks, is proposed to address the neural network model accuracy degradation caused by geometric and photometric variations such as lighting and rotation occurred in many practical applications like medical imaging. DCNs typically sample arbitrary locations of the input features for the convolution such that the objects with different scales or deformation can be captured. The sampling patterns of deformable convolution can be learned and calculated using an additional convolution layer. With the unique deformable convolution, DCNs have shown superior performance on many vision tasks such as object detection [1], instance segmentation [1] [5] [6] [7] and classification [8] [9] [10]. For instance, the authors in [1] demonstrated that the prediction accuracy of the proposed DCN increases from 70% to 75% on the image semantic segmentation dataset (CityScapes). Significant prediction accuracy improvement is also observed in human motion recognition task [11] [12], action detection task [13] [14] and intelligent medical monitoring and treatment [15] [16].

Despite the great advantages, each deformable convolution operation in DCNs needs additional convolution-based index calculation and bilinear interpolation (BLI) to obtain deformed features other than a standard convolution, so it is both computing- and memory-intensive and requires intensive acceleration for widespread deployment. Nevertheless, DCNs can not be deployed on conventional neural network accelerators mainly from the following two aspects. First, it convolves on arbitrary locations of the input features instead of fixed sliding windows as depicted in Figure 1. The locations i.e. the indices to the input features are generated at runtime and they will cause both dynamic and irregular accesses to the memory, which can not be fitted to conventional neural network accelerators targeting at regular memory accesses and data flows. Second, DCNs have a standard convolution to calculate the indices, but the calculated indices are usually not integers and can not be used to retrieve the feature data directly. Typically, BLI algorithm is utilized to approximate the features with the nearest original input features. This step is also not supported in conventional neural network accelerators. An intuitive solution to execute DCNs is to conduct the deformable convolution on a general purpose processor (GPP) which is usually seated with a neural network accelerator while deploying the rest of the normal neural network operations in DCNs on a neural network accelerator. However, GPPs especially the embedded processors with limited parallel processing capability is inefficient for the bilinear interpolation, and a large number of irregular memory accesses and data transfers between the GPPs and the neural network accelerator also inhibit the DCN execution efficiency.
Recently, there are also works proposed to revise the DCN models to fit existing neural network accelerators. The authors in [17] proposed to replace the bilinear interpolation algorithm with a simple rounding strategy and restrict the sampling locations to avoid dynamic memory access induced buffering problems. Similarly, the authors in [18] also proposed to modify the DCN models to reduce the receptive field size substantially so that the sampling locations are limited to a small region, which avoids the dynamic memory accesses across the whole input feature map. Although these approaches are demonstrated to be effective on existing neural network accelerators with minor model accuracy, it essentially poses hardware constraints to the model design and particularly limits its use on scenarios that are sensitive to the model accuracy loss. In addition, it requires time-consuming retraining and training data that may not be applicable to the end users. Thereby, we investigate the computing of the DCNs and seek to implement the entire unmodified deformable convolution on top of a unified neural network accelerator directly.

To implement the entire DCNs on a unified accelerator and reuse the conventional neural network accelerator as much as possible, we revisit a typical neural network accelerator architecture mainly for the new irregular feature sampling and the BLI required by DCNs. For the dynamic and irregular feature accesses, we observe that the input data required by the deformable convolutional output is imbalanced and some of the input features are utilized more than the others. More details can be found in Section III. With this observation, we propose to divide the input and output features into smaller tiles and build a tile dependency table (TDT) that keeps a record of all the required input tile IDs of each output tile with runtime tracking. On top of the TDT, we further schedule the output tile execution such that the buffered tiles are reused as much as possible and the overall memory access efficiency can be improved. For the BLI, we convert it to multiple small vector-based dot production which can be mapped in parallel to the 2D computing array in typical neural network accelerators efficiently with a weight stationary data flow [19]. In addition, we fuse the BLI and the following convolution to further reduce the intermediate data transmission between on-chip buffers and the external memory. With the proposed re-designing on top of a conventional neural network accelerator, the entire deformable convolution can be implemented on the revisited accelerator efficiently. According to our experiments on a set of DCNs, it achieves orders of magnitude higher performance and energy efficiency when compared to typical computing architectures including ARM, ARM+TPU, and GPU while it incurs only minor hardware resource consumption compared to a conventional neural network accelerator.

The rest of the paper is organized as follows. In Section II we introduce the typical deformable convolutional networks and formulate them into a unified computing model. Meanwhile, we briefly prior works about neural network accelerator redesigning for new types of neural network models. In Section III we characterize the computing patterns and memory accesses of deformable convolution. In Section IV we show the detailed design and optimizations of an accelerator for DCNs on top of a classical neural network accelerator. In Section V we evaluate the performance and energy efficiency of the accelerator and compare it with typical embedded computing platforms. In Section VI we conclude this work.

II. BACKGROUND AND RELATED WORK

A. Deformable convolutional networks

Deformable convolution may sample arbitrary locations of the input features for convolution such that it can capture the objects with scale or transformation. The unique feature makes it attractive in visual recognition tasks with geometric variations such as lighting and rotation. There have been many deformable convolution architectures proposed recently [1], [14]. They typically include two standard convolution operations. The first convolution calculates the indices for the input feature sampling while the second convolution convolves on the sampled features. Usually, a BLI operation is used to bridge the two convolution operations. It approximates the input features based on the non-integer indices generated by the first convolution and provides the features as inputs to the second convolution. The structures of DCNs mainly differ on the index reuse and can be roughly divided into two categories. The first category of DCNs has a unique index for each data in the feature plane and the indices are reused across the different channels [14]. The second category of DCNs also has the indices shared across the feature channels, but it has a unique index for each data in each convolution window [1]. Basically, the same data in the feature plane has different indices when it is located in different convolution windows. The second category of DCNs requires a larger convolution to calculate more sampling indices and produces more deformed features.
than the first category of DCNs. The two categories of DCNs are abbreviated as DCN-I and DCN-II respectively.

B. Unified deformable convolution model

The different deformable convolution can be represented in a unified model as formulated in Equation (1). Basically, it has a convolution to determine the deformed locations or indices of the input features in the first step. This step is formulated in Equation (1) where \(c, l, i, j\) refer to input channel index, output channel index, kernel offset in \(X\) dimension and kernel offset in \(Y\) dimension respectively. Since the indices can be different when the feature data is in different positions of the convolution kernel, we have \(y_L\), a vector of planar coordinates with length \(L = 2 \times K \times K\) where \(K\) is the kernel size to represent the indices. Suppose \(\alpha_m\) and \(\beta_n\) are the corresponding coordinates in \(X\) axis and \(Y\) axis respectively. \(\alpha_m\) and \(\beta_n\) are not integers, so they can not be used to retrieve the input features directly for the deformable convolution.

To that end, a bilinear interpolation approach is utilized to calculate the deformed features using the neighboring features around the location \((\alpha_m, \beta_n)\) in the second step. The calculated feature \(x_{c,\alpha_m,\beta_n}\) can be obtained using Equation (2) where \(BLI(\cdot)\) refers to the bilinear interpolation function, \(\Delta\alpha_m = \alpha_m - \lceil \alpha_m \rceil\) and \(\Delta\beta_n = \beta_n - \lfloor \beta_n \rfloor\). A vivid description of the BLI function can be found in Figure 2.

When the input features are retrieved and organized according to the deformed indices, the deformable convolution can be obtained using a standard convolution over the reorganized features as shown in Equation (3) in the third step.

\[
y_L = \sum_c \sum_{i,j} w_{c,i,j} \cdot x_{c,i,j} + b_l
\]

\[
x'_{c,\alpha_m,\beta_n} = F_{BLI}(x_{\lceil \alpha_m \rceil,\lfloor \beta_n \rfloor} \cdot x_{\lceil \alpha_m \rceil,\lceil \beta_n \rceil} \cdot x_{\lfloor \alpha_m \rceil,\lfloor \beta_n \rfloor} ;
\]

\[
x_{\lceil \alpha_m \rceil,\lfloor \beta_n \rfloor} ; \Delta\alpha_m ; \Delta\beta_n)
\]

\[
= (1 - \Delta\alpha_m) (1 - \Delta\beta_n) x_{\lceil \alpha_m \rceil,\lceil \beta_n \rceil} + (1 - \Delta\alpha_m) \Delta\beta_n x_{\lceil \alpha_m \rceil,\lceil \beta_n \rceil} + \Delta\alpha_m (1 - \Delta\beta_n) x_{\lfloor \alpha_m \rceil,\lceil \beta_n \rceil} + \Delta\alpha_m \Delta\beta_n x_{\lfloor \alpha_m \rceil,\lfloor \beta_n \rfloor}
\]

\[
y'_L = \sum_c \sum_{m,n} w'_{c,m,n} \cdot x'_{c,m,n} + b'_l
\]

C. Neural Network Accelerator Redesigning

The great success of neural networks in massive domains of applications inspires considerable efforts devoted to developing neural network accelerators [20] [21] [22] [23] [24] [25]. In spite of the notable efforts, newer network operations proposed for higher performance may go beyond the capability of the existing neural network accelerators. Although it is usually possible to offload the unsupported operations to the attached GPPs while leaving the rest of the conventional neural network operations on the accelerator, the performance of the co-designed implementation may drop dramatically due to the massive data communication between GPP and the accelerator. Also complex operations offloaded to GPPs may still become the performance bottleneck due to the insufficient computing capability of GPP and degrade the overall neural network execution. Thereby, the neural network accelerators are usually redesigned to meet the requirements of the new neural network operations on top of the existing neural network accelerators. For instance, unified neural network accelerators are also proposed to perform deconvolution used in generative adversarial neural networks other than the conventional convolution [26] [27] [28] [29]. A novel accelerator is developed to support 3D neural networks in [30] [31] [32]. The authors in [33] proposed to add a bilinear interpolation calculation module to an existing ReRAM neural network accelerator to enable in-situ DCN calculation. Inspired by prior works, we also try to convert the deformable convolution to operations that can be mapped to the neural network accelerator efficiently with minor hardware modification such that the whole deformable convolution can be executed on the neural network accelerator efficiently.

III. Observation

Since deformable convolution has many irregular memory accesses involved which dramatically affect the processing efficiency, we investigate the memory accesses of a typical deformable convolution in this section. We take the third convolution layer of VGG16 as the basis of a typical deformable convolution operation. As the memory accesses vary on different inputs, we randomly selected 2000 images from ImageNet and averaged the memory accesses for the investigation.

Figure 3 (a) shows the distribution of the input feature accesses. Unlike standard convolution that usually has nearly uniform utilization of the input features, deformable convolution has distinct utilization of the different input features. With the \(3 \times 3\) kernel used in the convolution, each input feature will be utilized around 9 times. For the corresponding deformable convolution, the access distribution shows dramatic difference. Around 15\% of the features will be utilized by more than 12 times, which take up around 25\% of the feature accesses. In contrast, more than 22\% of the features are utilized less than 6 times. While the neural networks can usually be tiled and the memory accesses can be performed in the granularity of a tile, we further analyze the input feature tile access distribution. In this experiment, we had both the input feature map and the output feature map divided into 25 tiles as an example. The tile access distribution is shown in Figure 3 (b). It can be observed that the input tile reuse still shows notable variation.
In summary, the input features are not evenly accessed, so some of the input features are more likely to be reused than the other. Given limited on-chip buffers, scheduling the order of the output feature calculation and optimizing the order of the input feature accesses can potentially improve the on-chip buffer utilization and remains demanded for higher performance and energy efficiency of the DCN processing.

IV. DCN ACCELERATOR ARCHITECTURE

A. Overall Accelerator Architecture

Deformable convolution is the major barrier that hinders the deployment of DCNs on existing neural network accelerators. Thereby, taming the deformable convolution to the existing neural network accelerators is key to accelerate DCNs. As formulated in Section II-B, deformable convolution consists of three processing stages including convolution, BLI, and convolution. Since the convolution operations in DCNs can be deployed on existing neural network accelerators directly, the major challenge of DCN acceleration is to optimize the BLI operation that samples the input features according to the irregular indices calculated with the first convolution in DCNs and conducts the BLI calculation based on the sampled input features. Since the indices depend on the input features and thus change at runtime, the BLI sampling leads to complicated memory accesses. To address this dynamic and irregular memory access problem, we have BLI divided into tiles and track the tile dependency at runtime with a tile dependency table (TDT). On top of the TDT, we have a tile scheduler to decide the order of the output tile execution and the input tile loading at the same time such that the tiles loaded to the on-chip buffers can be fully utilized and the memory accesses to the external memory can be reduced. As for the BLI calculation, we reorganize it to multiple small vector-based dot production and have the processing performed in parallel on top of the 2D computing array in the neural network accelerator for the sake of higher performance.

The proposed DCN accelerator architecture is shown in Figure 4. The components without filling any color belong to a classic neural network accelerator while the rest of the components filled with grey are designed specially for the deformable convolution. The entire accelerator is generally controlled with a sequence of instructions compiled from the target neural networks. The instructions are stored in the instruction buffer and decoded at runtime to generate control signals for the entire accelerator. With the controlling, neural network operations are mapped and executed on the regular 2D computing array. For the convolution operations, weights from different filters are streamed to the different columns of the computing array from top to bottom in parallel while input features are streamed from left to right in different rows according to the output stationary data flow proposed in [19].

For the deformable convolution, it is divided into three dependent operations. The first convolution operation starts when inputs and weights are ready in the on-chip buffers. The outputs of the first convolution are indices and will be utilized to sample from the input features. Since they are not integers and cannot be utilized to retrieve the input features directly, we have them stored in an index buffer and have an address converter to obtain the four neighboring integer indices. Meanwhile, BLI coefficients as proposed in Section II-B are generated with a coefficient calculation block at the same time. To this end, we can start the BLI calculation with the retrieved input features and BLI coefficients by taking advantage of the 2D computing array of the accelerator. The output of the BLI are essentially deformed features and will be utilized as inputs of the second convolution. While the address conversion and the BLI calculation are conducted in pipeline manner, the output buffer and the index buffer are separated in case of conflicts. After the BLI calculation, the deformed features will be stored and swapped as inputs of the computing array for the second convolution. When the features or weights exceed the on-chip buffers, BLI and the second convolution need to be tiled and fused to avoid intermediate data exchange through the external memory. In addition, we have a TDT to

![Fig. 3. Memory access characterization of the deformable convolution](image)

![Fig. 4. DCN accelerator overview. The blocks filled with grey are added specifically for the deformable convolution processing while the rest of the blocks remain the same with a conventional neural network accelerator with 2D computing array.](image)
keep a record of the tile dependency based on the generated indices and have a runtime tile scheduler to optimize the output tile execution and input tile loading ordering based on the TDT to enhance the on-chip data reuse and memory access efficiency.

B. BLI Implementation

To implement BLI, we have an address converter module to convert the original non-integer indices to neighboring integer addresses of the input feature buffer and a coefficient calculation block to produce the BLI coefficients at the same time. Each feature requires four coefficients $\eta, \mu, \theta, \gamma$ and they can be calculated with Equation 2. The BLI coefficients are stored in the weight buffer while the converted buffer addresses are used to retrieve features from the input buffer directly. The retrieved features and coefficients read from the weight buffer will then be fed to the 2D computing array following a standard weight stationary data flow  [19] for the BLI computing. Details of the processing will be illustrated in the rest of this section.

BLI Mapping Each deformed feature depends on four neighboring input features and it can be viewed as a vector-based dot production. One of the vector includes four BLI coefficients and the other vector includes four neighboring input features as shown in Figure 5. Each deformed feature processing can be mapped to four neighboring PEs organized as a cluster with a weight-stationary data flow. Since weights of the BLI are shared among the different input feature channels, they can be distributed to the PEs in the same cluster and broadcast to different clusters. The corresponding four input features in the same channel will be streamed in parallel for the multiplication among PEs in the same cluster. Features from different channels will be distributed to the different clusters of the computing array for higher throughput, but additional wires from wide input feature buffers to the PEs across the computing array are required accordingly. The clustered computing array on top of the original 2D regular computing array is shown in Fig 6. Unlike the output of the conventional computing array that are aligned in column, the clustered computing array output are extracted and aligned in cluster. Thereby, a MUX is added to the output port of each PE cluster to extract the output from the computing array when BLI is mapped.

Input Feature Layout To make best use of the entire computing array, the neighboring input features must be fed to the computing array continuously. However, when the input features are sequentially stored in a single port buffer, it can not load the four features in different rows and columns of the input features from the on-chip buffer in a single cycle simply with wider read port. A four-port on-chip buffer can meet the computing requirement, but it is extremely resource-consuming in terms of both power and chip area. To address the problem, we modify both the input feature layout and the structure of the input buffer as shown in Figure 7. Since the four features for each BLI processing of a deformed output feature are located in adjacent rows and columns, we separate the input features into four partitions based on the feature coordinate parity in the feature map and the four features will always be located in different partitions. Accordingly, we have the buffer divided into four banks and each bank accommodate an input feature partition. Four features required by the BLI processing of any feature can be loaded in a single cycle. In addition, we have the input features stored in channel-major order and widen the port of the buffer bank such that features of multiple channels are read at the same time for all the different PE clusters.

Address Converter: In order to fetch neighboring features for the BLI, we need to calculate the buffer addresses of the

Fig. 5. BLI mapping strategy

Fig. 6. Clustered PE array for parallel BLI calculation. The design is built on top of a conventional 2-D computing array in typical neural network accelerators. When the MUXes select 0, it is configured to be a normal 2-D computing array and can be used for standard convolution. When the MUXes select 1, each PE cluster in the design can be used for an BLI output calculation.

Fig. 7. Input feature layout and input buffer organization
four input features based on the non-integer indices. The basic idea is to obtain the four neighboring integers of the non-integer feature indices first and then deduct the base index of the four features to calculate the on-chip buffer addresses of the required features. Essentially, it is a conversion from 3-D feature map indices to the 1-D on-chip buffer indices and the higher dimension indices including the channel index and the height index need to be scaled accordingly as formulated in Equation 5 according to Equation 2. The four coefficients are required by all the four coefficient calculation, so it is formulated in Equation 4.

\[ \alpha_m = \left( 1 - \Delta \alpha_m \right) \Delta_n \]
\[ \beta_n = \left( 1 - \Delta \beta_n \right) \Delta_m \]
\[ \eta = \left( 1 - \Delta \alpha_m \right) \Delta_n \]
\[ \mu = \left( 1 - \Delta \beta_n \right) \Delta_m \]

C. Runtime Tile Scheduling

In order to address the dynamic and irregular memory access problem in deformable convolution, we propose to track the data dependency at runtime and optimize the execution with runtime scheduling based on the tracked data dependency. The dependency tracking and scheduling optimization will be illustrated in the rest of this sub-section.

Tile Dependency Tracking: To track the dynamic memory accesses, we need a dependency table to record all the required input features for each deformable convolution output feature. Due to the limited on-chip buffer in the accelerator, the neural network processing is usually tiled and the dependency table is constructed in the granularity of a tile accordingly. The tile dependency table is abbreviated as TDT. The dependency of the deformable convolution output tile to the input feature tile can be inspected with the deformed feature indices as described in Figure 9. Assume both the input and output features are divided into fixed 5 x 5 tiles. The feature indices i.e. \( \alpha_m \) and \( \beta_n \) are compared to the different boundary indices and the comparison result vectors can be used to determine the row index and the column index of the tile. As shown in Figure 9 the comparison result vector for \( \alpha_m \) is \((1,1,0,0)\) and it means \( \alpha_m \) is between 0.4H and 0.6H. With a decoder, we can obtain the row index of the dependent input tile. In this example, the row index is 2. Similarly, we can also obtain the column index of the dependent input tile and it is 1 in this example. Given the row index and the column index, we can decide the dependent input tile index and it is 11 in this example. Given the tracked data dependency, the dependent bit vector of which each bit refers to the dependency of the indexed input tile. If the corresponding input tile is dependent, it will be set to be 1 while the rest bits are set to be 0. By continuously inspecting all the deformed features required by an output tile and conducting OR operation with the bit vectors, we can obtain the entire tile dependency vector of an output tile. The tile dependency table is constructed right after the first convolution of the deformable convolution.
**Tile Scheduling**: Input tiles loaded to the on-chip buffers can be reused among the different output tile calculation, but the ordering of the input tile loading and output tile execution can both affect the reuse especially when the input buffer is limited and some of the input tiles have to be replaced. The input tile utilization varies greatly during the DCN processing as observed in the motivation section, which further aggravates the influence of the ordering of the input tile loading and the output tile execution. To address the above problem, we propose a unified tile scheduling algorithm that handles both the output tile scheduling and input tile scheduling based on the TDT that is updated at runtime.

The proposed scheduling algorithm is presented in Algorithm 1. It includes an output tile scheduling procedure and an input tile scheduling procedure based on the output tile scheduling result. For the output tile scheduling, it essentially selects an output tile that can reuse the input tiles that are already loaded and stored in the on-chip buffer. When the on-chip buffer is empty, it simply selects the output tile that requires the most input tiles which are more likely to be reused. When the output tile is selected, we need to determine the loading order of the dependent input tiles of the selected output tile. Although it is possible to sort all the dependent input tiles based on its potential reuse, but the input tile reuse is expensive to estimate at runtime. In this work, we have the dependent input tiles divided into three parts as illustrated in the input_tile_scheduling( ) function. The first part is the input tiles that are already stored in on-chip buffers. They will be scheduled first to ensure the on-chip data reuse. It can be determined by comparing the tile on-chip status bit vector OC and the dependency bit vector B[nextID]. The second part is the tiles that will be reused by the next output tile calculation. They will be loaded at last such that they can reside in the on-chip buffer for reuse. The next output tile calculation is obtained with the procedure output_tile_scheduling ( ). By comparing the current output tile dependency bit vector and the next output tile dependency bit vector, we can determine the overlapped input tiles that can be reused, but the tiles that are already stored in the on-chip buffer will be removed. The rest of the input tiles will be scheduled between the first part and the second part. As the input tile reuse are already considered in the scheduling, An FIFO (first in first out) strategy is used for the input tile replacement for efficient hardware implementation.

The proposed tile scheduling is implemented with customized hardware rather than a software scheduling algorithm on CPUs to ensure efficient tile-based execution. The tile scheduling module is shown in Figure 9. It mainly depends on the TDT to select the next output tile for execution on the computing array in the accelerator. The basic idea is to choose the output tile that has the most dependent input tiles overlapped with that of the scheduled current output tile. Thus, we have the dependency bit vector of current output tile AND with the bit vectors of all the un-executed output tiles. The AND result will be sent to an non-zero (NZ) bit counter module that mainly consists of an adder tree to count the number of the non-zero bits. The number will pass through a pipelined comparator to determine the maximum value. The corresponding output tile has the most input tiles overlapped with that of the current output tile, so it will be scheduled for the execution next. Instead of having the output tile scheduling and the execution conducted sequentially, we adopt a pre-scheduling strategy that performs the next output tile scheduling in parallel with the current output tile execution. Since the execution does not have to wait for the immediate scheduling result, more complex scheduling algorithm can be implemented. When the next output tile is selected, we will schedule the dependent input tiles. The input tile scheduling mainly depends on three hardware-friendly bitwise operations which divide the input tiles into three parts as already discussed in Algorithm 1. By inspecting the non-zero bit number of the three resulting bit vectors with corresponding NZ bit counters, we can determine the IDs of the input tiles in each partition and push them into three independent queues. As each queue belongs to different scheduling priorities, they can be scheduled sequentially and the input tile scheduling is

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**Algorithm 1 Bit vector based tile scheduling**

**Input:**
- \( N \): the number of tiles per feature map.
- \( B[N][N] \): bit vector of the output tile dependency, each vector \( B[i] \) \((1 \leq i \leq N)\) denotes it if it is dependent on the corresponding input tiles.
- \( M \): the total number of tiles that can be stored in the on-chip buffer.
- \( OS[N] \): bit vector of the output tiles, each bit denotes if a tile is executed.
- \( OC[N] \): bit vector of the input tiles, each bit denotes if a tile is in the on-chip buffer.

**Output:**
- \( OID[N] \): output tile IDs of the execution order.
- \( IID[N][N] \): input tile IDs of the loading order for each output tile.

1. \( it \leftarrow 1 \)
2. \( OID[it] \leftarrow \) ID of the output tile that requires the most input tiles.
3. \( while \ OS \neq \{0,0,\ldots,0\} \) do
4. \( it \leftarrow it + 1 \)
5. \( OID[it] \leftarrow \) output_tile_scheduling \((OS,OC)\)
6. \( IID[it] \leftarrow \) input_tile_scheduling \((OID,it,OS,OC)\)
7. \( OS[OID[it-1]] \leftarrow 0 \)
8. end while
9. procedure output_tile_scheduling \((OS, it)\)
10. \( TR[N] \): # of reused tiles when an output tile is scheduled.
11. \( currID \leftarrow OID[it-1] \)
12. \( for \ i = 1 \rightarrow N \) do
13. \( if \ OS[i] \neq 0 \) then
14. \( tmpID \leftarrow \) output_tile_scheduling \((OS,it)\)
15. \( else \)
16. \( TR[i] \leftarrow 0 \)
17. end if
18. \( end for \)
19. \( find \ output \ tile \ ID \ that \ TR[i] = \text{max}(TR) \)
20. return \( ID \)
21. end procedure
22. procedure input_tile_scheduling \((OID, it, OS, OC)\)
23. \( for \ i = 1 \rightarrow N \) do
24. \( if \ OS[i] = 0 \) then
25. \( nextID \leftarrow OID[it-1] \)
26. \(OiD[it] \leftarrow nextID \)
27. \( loadedVec \leftarrow OC & !B[nextID] \)
28. \( loadedVec \leftarrow B[currID] & B[nextID] \)
29. \( push \ the \ non-zero \ IDs \ of \ loadedVec \ to \ tmpID \)
30. \( push \ the \ non-zero \ IDs \ of \ tmpLoadVec \ to \ tmpID \)
31. \( return \ tmpID \)
32. end procedure

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A. Experiment setup

and fused in practice. The second processing stage and the third processing stage tile data and can be buffered on-chip directly, we mainly have the deformed indices is usually small compared to the feature back from the external memory, which is beneficial to both of the tiling avoids transferring the intermediate data to and from the external memory, which is beneficial to both the performance and energy efficiency. While the amount of the deformed indices is usually small compared to the feature data and can be buffered on-chip directly, we mainly have the second processing stage and the third processing stage tiled and fused in practice.

V. EXPERIMENT

A. Experiment setup

Hardware Platforms: The proposed DCN accelerator is implemented with Verilog and synthesized with Synopsys Design Compiler under TSMC 40nm library. It works at 800 MHz. The configurations of the DCN accelerator are shown in Table I. Processing elements in the accelerator adopt 8-bit fixed point. We also have DCN implemented on four typical architectures including an ARM processor (ARM), ARM+TPU, GPU, and DCN Accelerator (DCNA) for comparison. The ARM processor is ARM-A7@900MHz equipped with 1GB DRAM (DDR3) which is the core of Raspberry Pi 3. The GPU is 256-core NVIDIA Pascal GPU with 8GB GDDR5 memory and it is the core of Nvidia TX2. Experiments on the ARM processor and the GPU were implemented with PyTorch 1.3 on real platforms i.e. Raspberry Pi and TX2 respectively. Experiments for ARM+TPU were conducted in a mixed manner. The second stage of the deformable convolution is not supported by TPU and it was performed on the ARM processor instead, while the rest of the neural networks was performed on TPU and evaluated with Scale-Sim [35]. The configurations of the TPU architecture are the same with that used in the DCN accelerator. In addition, both the ARM processor and TPU have 1GB DRAM equipped. The average power of the ARM processor is 1.3W and its idle power is 0.3W. In order to evaluate the power consumption of DRAM, we accumulate the power consumption of the different memory operations such as Activation (ACT), Read (RD), Write (WR), and Background (BG) power based on Table II according to Micron’s power calculators [36].

Neural Network Benchmark: In order to evaluate the proposed DCNA, we have two typical neural network models including VGG19 [37] and SegNet [38] used as our benchmark. Deformable convolution can be used to replace any convolution in neural networks, but the replacement configurations can lead to different trade-offs between computation and model accuracy. In this case, we have three typical deformable convolution configurations set for each model and they are denoted as VGG19/SegNet-3, VGG19/SegNet-8, and VGG19/SegNet-16. As the convolution layers close to the output layer are usually smaller, we have deformable convolution placed from the output layer to input layer of the neural networks to minimize the deformable convolution induced computation. VGG19/SegNet-3 and VGG19/SegNet-8 represents that the last three convolution layers and the last eight convolution layers of VGG19/SegNet are replaced with the deformable convolution layers respectively. VGG19/SegNet-F represents that all the convolution layers are replaced with deformable convolution layers. Details of the benchmarks are summarized in Table III.

B. Performance Evaluation

The performance of the DCN execution on the different computing architectures is normalized to that on an ARM processor. As shown in Figure 10, DCNA achieves 515× and 621× higher performance on DCN-I and DCN-II respectively on average compared to a general ARM processor. DCN-II requires more sampling locations in deformable convolution operations of DCNs, so it has more computation and random...
TABLE III
NEURAL NETWORK BENCHMARK

| Network | # of deformable Conv | # of Conv | Kernel types |
|---------|----------------------|-----------|--------------|
| VGG19-3| 3                    | 13        | 3            |
| VGG19-8| 8                    | 8         | 3            |
| VGG19-F| 19                   | 0         | 3            |
| SegNet-3| 3                | 13        | 3            |
| SegNet-8| 8                   | 8         | 3            |
| SegNet-F| 16                 | 0         | 3            |

Fig. 11. Normalized (to ARM) performance of DCNs on different computing architectures.

accesses involved, which leads to larger execution time. Accordingly, higher performance speedup is achieved for DCN-II on DCNA. On the other hand, we notice that DCNA achieves much higher performance speedup on VGG19/SegNet-F compared to the other two configurations (i.e. VGG19/SegNet-3 and VGG19/SegNet-8) with less deformable convolution operations in the neural networks. The main reason is that the deformable convolution is rather challenging for the ARM processor due to the irregular memory accesses. The execution of deformable convolution operations on an ARM processor dominates the total DCN execution time and becomes the performance bottleneck of DCNs. In contrast, convolution with regular memory accesses is usually intensively optimized on ARM processors in PyTorch and the performance speedup achieved on customized accelerators is relatively lower. When DCNs are deployed on the ARM+TPU architecture, we can only have the convolution operations accelerated with TPU while the deformable convolution is still executed on the ARM processor. According to Amdahl’s law, the deformable convolution remains the performance bottleneck. Thereby, the performance speedup of the ARM+TPU architecture to the ARM processor is rather low especially for VGG19/SegNet-F. Unlike the ARM+TPU architecture, GPU in TX2 can have the entire DCNs implemented and the deformable convolution operations can also benefit from the GPU parallel processing due to its powerful support on general tensor operations. Thus, significant performance speedup is achieved compared to the ARM+TPU architecture. DCNA that is built on top of a conventional neural network accelerator has customized circuit design for both the standard convolution and the new deformable convolution outperforms GPU and exhibits 2.21× performance speedup on average.

C. Energy Consumption Evaluation

The energy consumption of DCNs on the four computing architectures is presented in Figure 12. It shows both the total energy consumption and the energy consumption distribution. Generally, DCNA with customized hardware acceleration shows the lowest energy and it is 612× less than the ARM processor. The energy consumption benefit is attributed to both the much smaller execution time brought by the performance acceleration as illustrated in Figure 11 and the lower power consumption. For the ARM+TPU architecture, although TPU can accelerate the convolution operations and consumes little energy, it still consumes considerable time and energy for the deformable convolution operations on the ARM processor. GPU on Nvidia Jetson TX2 can have both the convolution and deformable convolution accelerated, so it greatly reduces the execution time but its energy consumption remains 9× higher on average than DCNA due to the much higher power consumption. Moreover, we notice that the percentage of the DRAM energy consumption on VGG19/SegNet-F is larger than that on VGG19/SegNet-3 on DCNA. The main reason is that VGG19/SegNet-F with more deformable convolution involves many irregular memory accesses and lowers the memory access efficiency. Particularly, DCNA handles the irregular memory accesses with the granularity of a tile. Usually only a portion of the data in a tile is required and many of the data remain unused though the dependency is considered by the on-chip tile scheduler. In addition, some of the tiles may have to be repeatedly loaded due to the limited on-chip buffer and irregular data reuse. Thereby, the memory access efficiency is much lower than that of a standard convolution with regular memory access patterns. The lower memory accesses eventually lead to higher DRAM energy consumption.

D. Chip Area Evaluation

The baseline neural network accelerator can be roughly divided into on-chip Data Buffer (input feature/ output feature/ weight/ bias buffer), PE Array, and the Original Control Logic while DCNA requires additional components including Index Buffer, Tile Dependency Table, and the Added Control Logic. The chip area of the different components is presented in Figure 13. It can be seen that DCNA induces only 6.6% chip area compared to the baseline design. Among the added hardware blocks, index buffer that usually needs to store the generated feature indices in a deformable convolution operation takes up the most chip area. In contrast, the additional control logic and the tile dependency table consume negligible chip area. Since the feature indices generated in deformable convolution is usually reused among the different channels, it is much less than the input/output features and weights. Hence, the index buffer size is much smaller compared to the data buffer in the baseline neural network accelerator.
formable convolution exhibits marginal performance speedup. It is mainly caused by two reasons. First, the computation of the deformable convolution operations takes up only a small portion of the entire neural network computation, there is little space left for the performance improvement. Second, the sizes of the deformable convolution operations are small and the data including the input features, the weights, and the output features can be mostly fully buffered. Hence, the tiles can be reused without any scheduling and the proposed tile scheduling shows no performance improvement in this case. The performance improvement on DCN-I and DCN-II also differs. This is mainly caused by the fact that DCN-II involves more random sampling and thus benefits more from the DCNA acceleration.

On top of the performance improvement, we also evaluate the influence of the tile scheduling on the energy consumption of the DCN execution. The experiment result is shown in Figure 15. Again, it can be seen that VGG19/SegNet-F with most deformable convolution operations benefits most and shows the least energy consumption while VGG19/SegNet-3 with small deformable convolution operations has little optimization space for the tile scheduling. Generally, the energy reduction is mainly attributed to both the reduced execution time according to Figure 14 and the lower power consumption brought by the reduced memory accesses. As the performance improvement is already discussed in prior subsection, we mainly investigate the memory access reduction in this subsection. The total memory accesses issued by DCNA during the DCN processing is shown in Figure 16. By comparing the implementation without bit vector based dependency tracking and the implementation with bit vector but no scheduling, we observe that the bit vector based tile dependency tracking removes substantial memory accesses. It is mainly achieved by avoiding repeatedly loading the same input tiles required by the calculation of different output features in the same output tile. The scheduling further reduces the memory accesses by inspecting the input tile reuse among the different output tiles according to the tile dependency table. The experiment shows that the proposed scheduling
reduces the memory accesses by 40.7% on VGG19/SegNet-F on average compared to the implementation with only bit vector based dependency tracking.

**Tile Sizing**: Tile size is an important design parameter and it determines the granularity of the tile dependency tracking and scheduling. Since most of the memory access latency in DCNA can be overlapped by the computing latency, tile size mainly affects the memory access efficiency and the DRAM energy consumption eventually, and has little influence on the performance. We take VGG19/SegNet-F with most deformable convolution operations as an example and analyzed the DRAM energy consumption under different tile sizes. The experiment result is shown in Figure 17. It can be seen that the DCN processing with smaller tile size benefits most from DCNA and consumes the least DRAM energy. The main reason is that smaller tile size allows more efficient tile dependency tracking and scheduling. Thus, the on-chip buffer utilization and DRAM memory access efficiency can be improved. In contrast, when the tile size is large, the dependent input features of each output tile can spread across all the input tiles. In this case, all the input tiles have to be repeatedly loaded for each output tile calculation, leaving little optimization space for the proposed tile dependency tracking and scheduling.

**Layer Fusion**: In order to reduce the intermediate data transmission to and from DRAM, we propose to fuse the processing stages in each deformable convolution operation. The influence of the layer fusion on the energy consumption is shown in Figure 18. It can be seen that the fusion reduces the energy consumption by more than 20% on VGG19/SegNet-F with DCN-II structure. The main reason is that the memory access time in the two DCNs cannot be fully overlapped by the computation time due to the involved large deformable convolution operations and the fusion that avoids large intermediate data transmission improves the DCN performance other than the memory access efficiency. Unlike VGG19/SegNet-F, the deformable convolution operations in the rest scenarios are relatively small and the fusion only reduces the memory accesses while the performance has little improvement. As the DRAM energy consumption takes up only around 20% of the entire DCN energy consumption according to Figure 12, the energy reduction brought by the memory reduction is limited. Particularly, for VGG19/SegNet-3, the entire intermediate data can be mostly fully buffered and there is even little memory access optimization space left for the fusion. Thereby, the fusion shows little energy reduction.

**VI. Conclusion**

DCNs that have been demonstrated to be effective in many practical scenarios with image geometric or photometric variations include new deformable convolution operations other than the conventional neural network operations. The deformable convolution operations that require random sampling over the entire input feature maps incur considerable irregular memory accesses and bilinear interpolation (BLI) operations, which can not be fitted to the existing neural network accelerator architecture. In this work, we revisit the conventional neural network architecture by introducing a runtime tile-based data dependency tracking and scheduling mechanism.
to address the irregular memory accesses and optimize the data reuse in DCNs. At the same time, we reorganize the BLI operations to fit them to the 2D computing array for parallel processing. Finally, we also fuse the different processing stages in each deformable convolution operation to enable on-chip data reuse and reduce the intermediate data transmission via DRAM. According to our experiments on representative neural networks with different deformable convolution configurations, the proposed DCNA that supports both the convolution and deformable convolution achieves 45×-546× performance speedup over the ARM+TPU architecture that relies on the ARM processor to handle the deformable convolution. When compared to GPU that can execute the entire DCNs, DCNA shows 3× performance speedup and 18.6× energy reduction.

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