Accelerating Neural Network Inference with Processing-in-DRAM: From the Edge to the Cloud

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Abstract—Neural networks (NNs) are growing in importance and complexity. A neural network’s performance (and energy efficiency) can be bound either by computation or memory resources. The processing-in-memory (PIM) paradigm, where computation is placed near or within memory arrays, is a viable solution to accelerate memory-bound NNs. However, PIM architectures vary in form, where different PIM approaches lead to different trade-offs. Our goal is to analyze, discuss, and contrast DRAM-based PIM architectures for NN performance and energy efficiency. To do so, we analyze three state-of-the-art PIM architectures: (1) UPMEM, which integrates processors and DRAM arrays into a single 2D chip; (2) Mensa, a 3D-stack-based PIM architecture tailored for edge devices; and (3) SIMDRAM, which uses the analog principles of DRAM to execute bit-serial operations. Our analysis reveals that PIM greatly benefits memory-bound NNs: (1) UPMEM provides $23 \times$ the performance of a high-end GPU when the GPU requires memory oversubscription for a general matrix–vector multiplication kernel; (2) Mensa improves energy efficiency and throughput by $3.0 \times$ and $3.1 \times$ over the Google Edge TPU for 24 Google edge NN models; and (3) SIMDRAM outperforms a CPU/GPU by $16.7 \times / 1.4 \times$ for three binary NNs. We conclude that the ideal PIM architecture for NN models depends on a model’s distinct attributes, due to the inherent architectural design choices.

Introduction

Neural networks (NNs) [1–3] are becoming increasingly important for many daily activities, from routine tasks such as commute traffic estimation [4] to critical tasks such as medical diagnosis [5]. NN algorithms are rapidly evolving, which has led to many different types of NN models [6–41]. Such NN algorithms behave as either compute-bound workloads (i.e., when computing resources are the main performance bottleneck) or as memory-bound workloads (i.e., when memory resources are the main performance bottleneck) depending on the NN model [42–51].
A common approach to improve the performance of compute-bound NNs is to design compute-centric accelerators [6, 42, 46, 48, 52–62], where a significant portion of hardware resources are dedicated to the processing elements of the accelerator. Compute-centric NN accelerators aim to speed up two main operations that many NN models rely on [44]: multiply-and-accumulate (MAC), largely used for convolutions; and matrix-vector multiplications (MVMs). Similarly, various approaches to improve the performance of memory-bound NNs have been proposed [45, 63–73]. One such approach is processing-in-memory (PIM) [74–85], where computation is (1) placed near 2D [69, 86–110] or 3D [45, 63, 64, 67, 111–166] memory arrays (processing-near-memory, PNM) or (2) performed using the memory arrays themselves (processing-using-memory, PUM) [65, 70–72, 135, 167–203].1 PN Mand PUM can be implemented using different memory technologies [75], including SRAM [71, 99, 107, 110, 177, 178], DRAM [45, 64, 87, 100, 111, 123, 125, 128, 131–135, 142, 143, 146, 152, 157, 193, 195, 196], and resistive RAM (ReRAM) [65, 70, 121, 174, 175, 183, 188, 189, 199, 200, 202]. Independent of the memory technology, PIM allows NNs to enjoy higher memory bandwidth, shorter memory access latency, and lower energy per bit [75].

Our goal is to analyze, discuss, and contrast the benefits and drawbacks of different PIM architectures for NN performance and energy efficiency in different computing environments (i.e., edge devices and cloud servers). In this work, we focus on DRAM-based PIM, and NN inference in three different DRAM-based PIM architectures: (1) UPMEM [88, 90–92, 204, 205], a large-scale 2D-based PNM architecture, which integrates several simple general-purpose processing cores near DRAM arrays (inside a DRAM chip); (2) Mensa [45], a heterogeneous edge NN inference accelerator, which uses 3D-stack-based PNM to speed up memory-bound NN models; and (3) SIMDRAM [206], a PUM architecture, which uses the analog properties of DRAM to execute bit-serial operations. These three state-of-the-art PIM architectures broadly cover the design space for PIM designs since (1) UPMEM represents the design of 2D-based PNM systems, (2) Mensa represents the design of a PNM system that leverages 3D-stacked integration to add specialized hardware units near DRAM, and (3) SIMDRAM represents the design of PUM systems.

We draw three key takeaways from our analysis. First, the evaluated PIM architectures provide significant performance improvement and energy savings for NN inference when compared against compute-centric architectures (i.e., CPUs, GPUs, and compute-centric edge TPUs). Second, there is no holy grail PIM architecture that can broadly accelerate all different types of NN models. This happens because different PIM architectures come with different trade-offs (e.g., limited memory capacity, high cost, high complexity of mapping workloads to the PIM substrate, lack of support for key operations in NN inference). However, regardless of the underlying operating principles of our three state-of-the-art PIM architectures, they all can alleviate the memory bottlenecks our evaluated NN models suffer from by leveraging the internal memory bandwidth and abundant parallelism available inside DRAM.

Third, there is a need for programming models and frameworks that can unify the benefits of the different PIM architectures into a single heterogeneous system. Such solutions need to map, schedule, and control the execution of NN models on the most appropriate PIM architecture. Thus, they can enable a workload to leverage the benefits of PIM while avoiding particular drawbacks related to a given PIM architecture. We conclude that PIM is a promising solution to improve the performance and energy efficiency of several NN models.

We make the following key contributions:

- We investigate how three PIM architectures can be used to improve the performance and energy efficiency of different NN models.
- We observe that the fundamental properties of the target PIM architecture define the most suitable type of NN model for the underlying architecture.
Drawbacks of Compute-Centric NN Accelerators

We analyze the performance and energy of executing NN models using a commercial state-of-the-art compute-centric NN accelerator, called the Google Edge TPU [52], as our baseline accelerator. The Edge TPU has a generic tiled architecture, similar to other state-of-the-art accelerators [6, 63]. It includes a 64×64 2D array of floating-point multiply-and-accumulate processing elements (PEs), where each PE has a small register file to hold intermediate results. The accelerator has two large SRAM-based on-chip buffers to hold model parameters (4 MB parameter buffer) and activations (2 MB activation buffer). We analyze 24 Google edge NN models, including convolutional neural networks (CNNs) [7–11], long short-term memory (LSTM) networks [19–21], transducers [36, 37], and recurrent convolutional neural networks (RCNNs) [26, 38, 39]. Based on our analysis, we find that the accelerator suffers from three key shortcomings.

1. The accelerator often suffers from extreme underutilization of the PEs. The Edge TPU has a theoretical peak throughput of 2 TFLOP/s. However, the accelerator operates at a throughput much lower than its peak throughput during inference execution (75.6% lower on average). Figure 1 (left) shows the throughput roofline model [207] for the Edge TPU, along with the measured throughput of all of our edge models. We observe that the PE utilization is low across all models. Transducer and LSTM models have the highest underutilization, with both achieving less than 1% of peak throughput. While CNN and RCNN models do somewhat better, they achieve only 40.7% of peak utilization on average (with a minimum of only 10.2% of peak utilization). We identify two main reasons why the actual throughput of the Edge TPU falls significantly below its peak.

First, while some layers have high parameter reuse (1200 FLOP/B ratio), other layers exhibit very low reuse (1–64 FLOP/B) while at the same time having large parameter footprints (0.5–5 MB). Layers with low reuse yet large parameter footprints are memory-bound and often leave PEs idle, as the parameters incur long-latency cache misses to DRAM.

Second, the Edge TPU does not provide a custom dataflow optimized for each layer. From our analysis, we observe that layers both across and within models exhibit high variation in terms of data reuse patterns and computational intensity. This variation necessitates the need for different dataflows for different layers, where each dataflow exposes a different set of reuse opportunities for parameters and activations.

2. The Edge TPU operates far below its theoretical maximum energy efficiency. Figure 1 (right) shows the energy efficiency roofline [208] for the Edge TPU, along with the energy efficiency achieved for each model. On average across all models, the Edge TPU achieves only 37.2% of its maximum possible energy efficiency. The energy efficiency is particularly low (33.8% of the maximum) for LSTM and Transducer models, but even the best CNN model achieves only 50.7% of the maximum energy efficiency. To understand the accelerator’s low energy efficiency, we analyze (in Figure 2) the energy breakdown during inference execution across different models. We make three key observations.

First, the on-chip buffers (the activation buffer and the parameter buffer) account for a significant portion of both static and dynamic energy across all models. Second, averaged across all models, the Edge TPU spends 50.3% of its total energy on off-chip memory accesses. Third, for LSTMs and Transducers, the Edge TPU spends approximately three quarters of its total energy on DRAM accesses. This is because while the buffers consume...
a significant amount of area in the Edge TPU (79.4% of the total area), they are ineffective at reducing off-chip memory accesses.

3. The accelerator’s memory system design is neither effective nor efficient. The Edge TPU memory system, which includes both on-chip buffers and off-chip memory, is highly inefficient, and results in significant energy consumption.

Key Takeaways. Our analysis provides two key insights: (1) there is significant variation in terms of layer characteristics across and within edge NN models, where models vary from being compute-bound and memory-bound; (2) the monolithic design of state-of-the-art NN accelerators mainly caters for compute-bound NN models, which leads to high underutilization and low energy efficiency of memory-bound NN models.

PIM Architectures for NN Inference

The goal of our work is to explore how different state-of-the-art PIM architectures overcome the memory bottlenecks caused by data movement in NN inference in different environments (i.e., from edge devices to cloud servers).

We conduct our analysis in three steps. First, we evaluate the performance of a key primitive in NN inference (i.e., general matrix–vector multiplication, GEMV) on the first commercial server-based PIM architecture (UPMEM [88, 90–92, 204, 205]), which is a 2D general-purpose PNM architecture. Second, we design specialized NN inference accelerators for 24 different edge NN models in a 3D-stacked memory using the Mensa framework [45]. Since Mensa relies on the 3D integration of logic and memory, the microarchitecture for the PIM accelerators can consist of an extensive range of processing elements, including costly floating-point MAC units. Third, we map three different binary neural networks (BNNs) [41, 209–212] to a PUM substrate called SIMDRAM [206], which is a promising solution for both edge-based and cloud-based systems since it operates using standard 2D DDRx DRAM chips. We conclude by drawing key takeaways from our analyses, and based on them, we provide some guidelines for future PIM systems targeting NN inference.

These three state-of-the-art PIM architectures broadly cover the design space for general-purpose 2D PNM (UPMEM), specialized 3D PNM (Mensa), and DRAM-based PUM (SIMDRAM) proposals. Regardless of the underlying operating principles of our three state-of-the-art PIM architectures, they all leverage DRAM’s abundant internal parallelism and internal memory bandwidth to alleviate memory bottlenecks.

NN Inference on General-Purpose 2D-Based Processing-near-Memory

We conduct a preliminary analysis of the potential of the first commercially-available server-based PIM system, called UPMEM [88, 90–92, 204, 205], for NN inference. Many NN inference workloads (e.g., CNN, LSTM) use matrix–vector multiplication (GEMV) as a key operation. GEMV is characterized as memory-bound in compute-centric architectures (i.e., CPU, GPU) [76, 92]. As a result, GEMV is a suitable candidate to be mapped onto the UPMEM architecture. We compare quantitatively and qualitatively our PIM implementation of GEMV to its state-of-the-art GPU counterpart.

UPMEM PIM Architecture

Figure 3 (left) depicts an UPMEM-based PIM system with (1) a host CPU, (2) standard main memory (DRAM modules), and (3) PIM-enabled memory (UPMEM modules) [88]. An UPMEM module is a standard DDR4-2400 DIMM module with 16 PIM chips.

We show GEMV performance in our UPMEM experiments as a preliminary evaluation of the benefits the UPMEM system can provide for NN inference. Implementing an end-to-end NN inference model using the UPMEM system requires non-trivial effort, which we leave for future work.

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2We refer the reader to the sidebar for a brief discussion of several other related works.
MRAM is accessible by the host CPU (Figure 3, left) for copying input data (from main memory to MRAM) and retrieving results (from MRAM to main memory). In UPMEM, data is explicitly copied from a CPU to DPUs, and from MRAM to WRAM using CPU instructions. The UPMEM runtime system transposes DPU data using software libraries so that a 64-bit word is placed inside a single DPU. There is no communication path across DPUs: all inter-DPU communication happens through the CPU. In current UPMEM-based PIM systems, the maximum number of UPMEM DIMMs is 20. Thus, the PIM system contains up to 2,560 DPUs which amounts to 160 GB of PIM-capable memory.

Evaluation Methodology

We evaluate GEMV on a real UPMEM-based PIM cloud system with 2048 DPUs and on a state-of-the-art NVIDIA A100 GPU [213, 214]. We use an open-source implementation of GEMV for UPMEM [90–92] and the cuBLAS library [215] for the GPU. DPUs run at 428 MHz. The maximum aggregated memory bandwidth for 2048 DPUs is 1.7 TB/s for a memory capacity of 128 GB. The A100 GPU runs at 1.4 GHz. The A100 GPU features 40 GB of HBM2 memory [216] with a bandwidth of 1.5 TB/s.

We perform two experiments. First, we evaluate performance and scalability characteristics of GEMV on the UPMEM system. Second, we compare the performance of GEMV on 2048 DPUs with that on the GPU. Since the amount of memory of the GPU is relatively small, we evaluate one version with regular memory allocation and another version with unified memory allocation, which allows memory oversubscription.

Results

Figure 4 shows strong scaling results of GEMV for four different matrix sizes on the UPMEM system. The matrices have 32-bit floating-point or integer values. The experiment uses 256, 512, 1024, and 2048 DPUs. Inside each DPU, we execute 16 software threads.

We make two observations. First, the execution with floating-point values takes one order of magnitude more time than the execution with integers. The reason is that the UPMEM DPUs do not have native support for floating-point operations. This is a limitation that comes from the difficulty of integrating logic into DRAM chips [217]. As a result, floating-point operations are emulated [92]. Second, the kernel execution time of GEMV (both floating-point and integer values) scales linearly on the UPMEM system. The DPU kernel execution time reduces by nearly $2 \times$ when we double the number of DPUs.

Figure 5 shows the comparison of GEMV (integer values) on the PIM system with 2048 DPUs to the A100 GPU. We observe that the GEMV kernel execution time on the 2048-DPU UPMEM system and on the GPU (without unified memory) is in the same order of magnitude, with the GPU being 4–5 $\times$ faster than the UPMEM system. This is because (1) the peak compute throughput of the A100 GPU is orders of magnitude higher (TFLOPs vs. GOPs) even though the UPMEM system and the A100 GPU have similar memory bandwidth [92], and (2) 32-bit integer multiplication is emulated on the UPMEM DPUs (there is no 32-bit multiplier [88]).

![Figure 4: Execution time (ms) of GEMV for 32-bit floating-point (left) and 32-bit integer (right) on 256, 512, 1024, and 2048 DPUs.](image)

![Figure 5: Normalized execution time of GEMV for 32-bit integer values on 2048 DPUs and A100 GPU with unified memory (GPU-UM). Values are normalized to an A100 GPU without unified memory.](image)

There are three key takeaways from this comparison. First, the GPU has significant compute resources (including hardware multipliers), which leads to its higher performance. As future PIM systems integrate better (e.g., higher precision)
multipliers and more compute resources as GPUs have done, we expect their performance to get significantly higher. Second, the GEMV kernel is very memory-bound on GPU for large matrix sizes. In contrast, the UPMEM system balances GEMV’s compute and memory requirements better. Third, when employing a unified memory allocation in the GPU system, the GEMV kernel’s execution time increases significantly. In this case, both the 2048-DPU system and the GPU without unified memory greatly outperform the GPU with unified memory. Allowing memory oversubscription in the GPU has a large performance cost due to overheads related to address translation and page swapping between the CPU and GPU memories [218–220]. The UPMEM system avoids the need for a unified memory space, since it provides higher memory capacity and better scalability of computing throughput and memory size compared to the GPU.

We run one final experiment (not shown in the figure) where we compare GEMV on the UPMEM system for 32-, 16-, and 8-bit integers. The DPU contains an 8-bit multiplier [88], which allows the 16-bit and the 8-bit versions to be $1.75 \times$ and $2.17 \times$ faster than the 32-bit version, respectively. These results demonstrate the potential of the UPMEM system for NN inference in cases where fixed-point computation and quantization are feasible, despite the inherent limitations derived from the integration of logic units inside the 2D DRAM chip.

**NN Inference on Specialized 3D-Based Processing-near-Memory**

Modern 3D-stacked memories [221–223] such as High Bandwidth Memory [221] and the Hybrid Memory Cube [222] include logic layers that have access to the high memory bandwidth available within a 3D-stacked memory chip [75]. We evaluate the opportunities a 3D-stack-based PNM architecture provides for NN inference. To do so, we use Mensa [45], a new machine learning accelerator design framework that distributes the layers from an NN model across a collection of smaller memory- and compute-centric hardware accelerators that are specialized to the properties of different NN layer types. By specializing each accelerator to a subset of NN layers, Mensa avoids the shortcomings of monolithic edge NN accelerators, resulting in a highly-efficient and high-performance heterogeneous accelerator with a much smaller area footprint.

We employ Mensa’s methodology to design a specialized NN inference system for the Google edge NN models discussed in our motivation. For each layer, we study the correlation between different characteristics. These characteristics include (1) parameter reuse (FLOP/B), (2) parameter footprint (MB), and (3) MAC intensity (defined by the number of MAC operations). Based on all of the layer characteristics that we analyze, we observe across all layers from all models that 97% of the layers group into one of five layer families. We design different accelerators to cater to the properties of each layer family.

We identify that (a) layers in Families 1 and 2 share a high MAC intensity (20M–20M), small parameter footprint (1–500 kB), and moderate-to-high parameter reuse (81–20K FLOP/B); while (b) layers in Families 3 and 4 share a low MAC intensity (0.1M–25M), large parameter footprint (0.5–18 MB), and low parameter reuse (1–64 FLOP/B). Thus, we need at least two different accelerator designs: one that caters to the compute-centric behavior of Families 1/2, and one that caters to the data-centric behavior of Families 3/4. Given our resource-constrained edge environment, we look to see if layers in Family 5, which have a low MAC intensity (similar to Families 3 and 4) but a relatively small parameter footprint (similar to Families 1 and 2), can benefit from one of these two approaches. We find that the low MAC intensity, along with the low parameter reuse by many Family 5 layers, allow the layers to benefit from many of the data-centric optimizations that benefit Families 3 and 4, so we study Families 3/4/5 collectively as we design the data-centric accelerators.

Figure 6 shows the design of the three Mensa accelerators, called Pascal, Pavlov, and Jacquard, which we collectively refer to as Mensa-G. We tailor the hardware components (i.e., PE array size, on-chip parameter and activation buffers size, accelerator placement) and dataflow for each accelerator based on the properties of the layer families it targets. We briefly describe the hardware components of each accelerator next. We refer the reader to the full Mensa paper [45] for a detailed description of each accelerator.
Figure 6: Mensa-G accelerator design.

**Pascal: Compute-Centric Accelerator Design.** Pascal caters to layers in Families 1 and 2, which are compute-centric. We design Pascal as shown in Figure 6a. First, the PE array in Pascal needs to have enough PEs to accommodate the high MAC intensity exhibited by layers in Families 1 and 2. Thus, we profile the performance of Family 1/2 layers on different PE sizes and empirically choose a $32 \times 32$ PE array, which lets Pascal achieve a 2 TFLOP/s peak throughput. Second, we reduce the size of the activation buffer from 2 MB in the Edge TPU to 256 kB (i.e., by $8 \times$) in Pascal, because Pascal’s dataflow exploits temporal reduction for the output activations using the internal PE registers, and no longer needs to store the large footprint of the output activations in the activation buffer. We reduce the size of the parameter buffer from 4 MB in the Edge TPU to 128 kB in Pascal, because layers in Families 1 and 2 have small parameter footprints. Given the low off-chip memory bandwidth requirements of Pascal, we keep the accelerator on the CPU die.

Pascal’s dataflow reduces memory traffic by enabling two types of reuse. First, the dataflow uses temporal reduction [224] for each output activation element, by having a single PE accumulate the entire sum of the elements across multiple cycles in the PE’s register file. Second, the dataflow uses spatial multicasting [224] for each parameter, by ensuring that all PEs work on the same image channel\(^4\) in the same cycle.

**Pavlov: Data-Centric Accelerator Design for (Mainly) LSTM.** Pavlov caters to layers in Family 3, which are data-centric and predominantly consist of LSTM layers. We design Pavlov as shown in Figure 6b. First, because Family 3 layers have low MAC intensity, we empirically choose a small $8 \times 8$ PE array for Pavlov. This allows Pavlov to achieve 128 GFLOP/s peak throughput. Second, we place Pavlov inside memory to accommodate the significant off-chip memory bandwidth requirements of Family 3 layers. Given that parameters and activations from Family 3 layers exhibit different characteristics, for parameters, we use only one level of memory hierarchy (512 B of private registers per PE), eliminating the parameter buffer, and streaming parameters directly from DRAM. The per-PE registers provide enough space to cache the temporally-multicasted parameters, and there are no other reuse opportunities that the parameter buffer could exploit. Thanks to the small activation footprint of Family 3 layers, we use a 128 kB buffer for activations ($16 \times$ reduction over the Edge TPU’s activation buffer).

Pavlov’s dataflow reduces memory traffic by enabling two types of reuse. First, the dataflow temporally reuses a weight by allowing the PEs to store the weight and partial sums in one of their private registers. Second, the dataflow uses spatial multicasting for each input activation, as the same activation is multiplied across all columns for a given row of a parameter matrix.

**Jacquard: Data-Centric Accelerator Design for (Mainly) Non-LSTM NNs.** Jacquard caters to layers in Families 4 and 5, which primarily consist of non-LSTM data-centric layers. We design Jacquard as shown in Figure 6c. First, while layers in Families 4 and 5 have low MAC intensity, they perform more MAC operations on average than Family 3 layers. Thus, we empirically select a $16 \times 16$ PE array for Jacquard. This allows Jacquard to achieve a peak throughput of 512 GFLOP/s. Second, similar to Pavlov, we place Jacquard inside the logic layer of 3D-stacked memory. Doing so enables high memory bandwidth for the large parameter footprints of Family 4 layers. Given the small activation footprints, we use a small 128 kB buffer for them ($16 \times$ reduction compared to the Google Edge TPU). Thanks to the temporal parameter reuse that Jacquard’s dataflow enables, we reduce the parameter buffer to 128 kB ($32 \times$ reduction compared to the Google Edge TPU).

Jacquard’s dataflow reduces memory traffic by enabling two types of reuse. First, the dataflow temporally reuses parameters. As in Pavlov, a parameter is stored in a PE register and reused over

\(^4\)A layer in a CNN can sometimes break down an input into multiple filtered channels (e.g., breaking an image down into red, green, and blue colors).
multiple cycles to reduce the number of times the parameter is fetched from memory. By increasing the reuse of the parameter, the dataflow hides the off-chip memory access latency by overlapping it with PE computation. Second, the dataflow uses spatial multicasting for each input activation. To enable spatial multicasting for Families 4 and 5, the dataflow enables all PEs to collectively compute a single output activation in two steps. In the first step, each PE computes a partial sum. In the second step, the on-chip interconnect is used to gather partial sums from all PEs and produce the final output activation.

Layer-to-Accelerator Mapping. We design a software runtime scheduler to identify which accelerator each layer in an NN model should run on. When an NN model runs on Mensa, the scheduler maps each NN layer to different accelerators. The scheduler uses the NN model (including a directed acyclic graph representing communication across model layers) and the configuration information in the accelerator hardware driver to determine this mapping.

Execution and Communication. Once the layer-to-accelerator mapping is complete, Mensa begins model execution. During execution, destination layer $i$ placed in accelerator $j$ needs to read (1) any unbuffered parameters (i.e., weights) from DRAM; and (2) input activations (i.e., input data) produced by layer $i-1$, when layer $i$ is run on a different accelerator than $j$. In order to simplify communication between accelerators, Mensa accelerators transfer activations to another accelerator through DRAM, avoiding the need to keep on-chip data coherent across accelerators (or, when some of the Mensa accelerators are placed near memory, to keep on-chip and near-data accelerators coherent [45, 64, 123, 134]).

Evaluation Methodology

We evaluate end-to-end inference energy (using an energy model based on prior works [63, 64]), hardware utilization, and throughput (using an in-house simulator) of three configurations: (1) Baseline, the Google Edge TPU [52]; (2) Base+HB, a hypothetical version of Baseline with $8 \times$ the memory bandwidth (256 GB/s), similar to monolithic 3D-stack-based PNM inference accelerators [63]; and (3) Mensa-G with all three accelerators (Pascal, Pavlov, Jacquard).

Results

Energy Analysis. Figure 7 shows the total inference energy consumed by the three systems we evaluate across different NN models. We report results for representative LSTM, Transducers, CNNs, and RCNNs to improve the figure’s clarity. We report average energy values for all 24 Google edge NN models. We make two observations.

![Figure 7: Inference energy across different models normalized to Baseline.](image)

First, providing high memory bandwidth to Baseline (Base+HB) results in only a small reduction in energy (7.5% on average). This is because Base+HB still incurs a high energy cost due to (1) on-chip buffers that are overprovisioned for many layers, and (2) off-chip traffic to DRAM. Second, Mensa-G significantly reduces energy across all models. The reduction primarily comes from three sources. (1) Mensa-G lowers the energy spent on on-chip and off-chip parameter traffic by $15.3 \times$ over Baseline, by scheduling each layer on the accelerator with the most appropriate design and dataflow for that layer. LSTMs and Transducers benefit the most, as their energy in Base+HB is dominated by off-chip parameter traffic, which Pavlov and Jacquard drastically reduce by being placed inside memory. (2) Mensa-G reduces the dynamic energy of the on-chip buffer and on-chip network (NoC) by $49.8 \times$ over Base+HB by avoiding overprovisioning and catering to specialized dataflows. This is most beneficial for CNN and RCNN models. (3) Mensa-G reduces static energy by $3.6 \times$ over Base+HB thanks to using significantly smaller PE arrays that avoid underutilization, significantly smaller on-chip buffers, and dataflows that reduce inference latency.

\footnote{We implement Mensa using Google’s Edge TPU in-house simulator as a base, which faithfully models all major components of the Google Edge TPU, including the PE array, memory system, on-chip network, and dataflow. In our in-house simulator, the logic layer of 3D-stacked memory accelerators has access to the 256 GB/s internal bandwidth of High Bandwidth Memory (HBM) [221], which is $8 \times$ the external memory bandwidth of accelerators that sit outside of memory.}
Utilization and Throughput Analyses. Figure 8 shows the raw PE utilization (top) and Baseline-normalized throughput (bottom) for our three configurations. Mensa-G’s utilization is calculated by computing the average utilization across its three accelerators (Pascal, Pavlov, and Jacquard). We make two observations.

![Figure 8: PE utilization (top) and Baseline-normalized throughput (bottom).](image)

First, Baseline suffers from low PE array utilization (on average 27.3%). The higher memory bandwidth in Base+HB increases the average PE utilization to 34.0%, and improves throughput by 2.5×. Overall, Base+HB still has very low utilization, as many layers (those from Families 3, 4, and 5) do not need the large number of PEs in the accelerator. Second, Mensa-G significantly increases both average utilization (by 2.5×/2.0×) and throughput (by 3.1×/1.3×) over Baseline/Base+HB. The large utilization improvements are a result of (1) properly-provisioned PE arrays for each layer, (2) customized dataflows that exploit reuse and opportunities for parallelization, and (3) the movement of large-footprint layer computation into 3D-stacked memory (which eliminates off-chip traffic for their DRAM requests).

**NN Inference on Processing-using-Memory**

A common approach for PUM architectures is to make use of bulk bitwise computation. Ambit [167, 168, 171, 179, 180, 182], a DRAM-based PUM architecture, was the first work to propose exploiting DRAM’s analog operation to perform bulk bitwise AND, OR, and NOT logic operations. Ambit leverages the fact that by simultaneously accessing three DRAM rows, the DRAM row sensing circuitry pulls its output voltage level to the majority voltage level among the three accessed rows, performing a majority-of-three (MAJ) operation. AND and OR logic operations can be performed by setting one of the three simultaneously accessed DRAM rows to either ‘1’ (for an OR) or ‘0’ (for an AND). To implement NOT, Ambit uses and feeds into a DRAM array the complemented value of a cell that already exists after sensing in the sense amplifier. SIMDRA M [206] builds on top of Ambit to implement complex operations efficiently in DRAM using an end-to-end framework. Such a framework efficiently implements arbitrary in-DRAM operations by (1) leveraging MAJ/NOT-based computation (instead of Ambit’s focus on AND/OR/NOT-based computation) and (2) by employing a bit-serial execution model.

SIMDRAM consists of three key steps to enable any desired operation in DRAM: (1) building an efficient MAJ/NOT-based representation of the desired operation, (2) mapping the operation’s input and output operands to DRAM rows and to the required DRAM commands that produce the desired operation, and (3) executing the operation. These three steps ensure efficient computation of a wide range of arbitrary and complex operations in DRAM. The first two steps give users the flexibility to efficiently implement and compute any desired operation in DRAM. The third step controls the execution flow of the in-DRAM computation, transparently from the user.

For a desired computation, the first step derives its optimized MAJ/NOT-based implementation from its AND/OR/NOT-based implementation. The second step translates the MAJ/NOT-based implementation into DRAM row activations. This step includes (1) mapping the operands to the designated rows in DRAM, and (2) defining the sequence of DRAM row activations that are required to perform the computation. SIMDRA M chooses the operand-to-row mapping and the sequence of DRAM row activations to minimize the number of DRAM row activations required for a specific operation. To this end, we present a new row allocation algorithm inspired by the linear scan register allocation algorithm [225]. However, unlike register allocation algorithms, our row allocation algorithm considers two extra constraints that are specific to processing-using-DRAM: (1) performing MAJ in DRAM has destructive behavior; and (2) the number of DRAM rows that are designated to perform bitwise operations is limited. The third
step programs the memory controller to issue the sequence of DRAM row activations to the appropriate rows in DRAM to perform the computation specified by the operation. To this end, SIMDRAIN uses a control unit in the memory controller that user-transparently executes the sequence of DRAM row activations for each specific operation.

We use SIMDRAIN to efficiently support a wide range of operations of different types. We implement a set of 16 SIMDRAIN operations of five different types for \( n \)-bit data elements: (1) \( N \)-input logic operations (OR-/AND-/XOR-reduction across \( N \) inputs); (2) relational operations (equality/inequality check, greater-/less-than check, greater-than-or-equal-to check, and maximum/minimum element in a set); (3) arithmetic operations (addition, subtraction, multiplication, division, and absolute value); (4) predication (if-then-else); and (5) other complex operations (bitcount, and ReLU [226]). We support four element sizes that correspond to data type sizes in popular programming languages (8-/16-/32-/64-bit integers).

System Integration

A program in a SIMDRAIN-enabled system can have a combination of CPU and SIMDRAIN instructions, with possible data sharing between the two. This leads to several challenges in integrating SIMDRAIN into a real system. We discuss two system integration challenges related to data mapping and internal memory communication. The full SIMDRAIN paper [206] contains further discussion about other system integration challenges and how we address them, including (1) data layout and how SIMDRAIN stores the data required for in-DRAM computation in a vertical layout and transposes such data when it is needed in a horizontal layout; (2) ISA extensions for and programming interface of SIMDRAIN; (3) how SIMDRAIN handles page faults, address translation, coherence, and interrupts; (4) how SIMDRAIN manages computation on large amounts of data; (5) security implications of SIMDRAIN; and (6) current limitations of SIMDRAIN.

Data Mapping. SIMDRAIN uses a special ISA instruction (bbop_trsp_init) to inform the operating system (OS) that a memory location is a SIMDRAIN object. This allows the OS to perform virtual-to-physical memory mapping optimizations for the SIMDRAIN object before the allocation starts (e.g., mapping the arguments of an operation to the same row/column in physical memory).

Internal Communication. SIMDRAIN does not support communication across different in-DRAM SIMD lanes (i.e., there is no communication across DRAM bitlines). Communication across subarrays and banks can be performed using prior works (i.e., LISA [227] and RowClone [170], respectively).

Evaluation Methodology

We map three different binary neural networks (BNNs) [41, 209–212] to our PUM substrate since SIMDRAIN operates in a bit-serial model and only supports integer operations. BNNs are CNNs whose activations and weights are represented with 1-bit values, enabling convolutions by executing bit-serial bitcount, shift, and addition operations [186]. We use the XNOR-NET [41] implementations of VGG-13, VGG-16, and LeNET provided by [186], to evaluate the functionality of SIMDRAIN. We modify these implementations to make use of SIMDRAIN’s bitcount, addition, shift, and XNOR operations. We evaluate all three networks for inference using two different datasets: CIFAR-10 [228] (for VGG-13 and VGG-16), and MNIST [229] (for LeNet-5). We evaluate BNN inference time in SIMDRAIN by isolating the main kernel that SIMDRAIN executes (i.e., bitwise convolution) and evaluating its performance. We estimate the end-to-end speedup SIMDRAIN provides for each BNN by applying Amdahl’s law [230]. Thus, SIMDRAIN’s end-to-end speedup is given by: 

\[
\text{SIMDRAM speedup} = \frac{1}{(1 - \text{conv\_time}) + \text{conv\_time}}
\]

where \( \text{SIMDRAM speedup} \) is the speedup SIMDRAIN provides for the main kernel compared to the CPU execution, and \( \text{conv\_time} \) is the percentage of the total execution time the main kernel represents when executing BNN inference on the baseline CPU.

We implement SIMDRAIN using the gem5 simulator [231] and compare it to a real multicore CPU (Intel Skylake [232]), a real high-end GPU (NVIDIA Titan V [233]), and a state-of-the-art processing-using-DRAM mecha-
nism (Ambit [167, 168, 171, 179, 180, 182]). We validate our Ambit and SIMDRAM gem5 implementations rigorously with the results reported in the original Ambit paper. We evaluate three different configurations of SIMDRAM where 1 (SIMDRAM:1), 4 (SIMDRAM:4), and 16 (SIMDRAM:16) DRAM banks out of all the 16 banks in one channel have SIMDRAM computation capability. SIMDRAM:1’s throughput for bitcount, addition, shift, and XNOR operations used during BNN inference are 24.3 GOPs/s, 20.1 GOPs/s, 1337.5 GOPs/s, and 51.4 GOPs/s, respectively, and this throughput scales linearly with the number of DRAM banks.

Results

Figure 9 shows the performance of SIMDRAM, the GPU, and Ambit for each BNN, normalized to that of the multicore CPU. We make two observations.

First, SIMDRAM:16 greatly outperforms the CPU and GPU baselines, providing 16.7× and 1.4× the performance of the CPU and GPU, respectively, on average across all three NNs. SIMDRAM has a maximum performance of 31× and 1.7× that of the CPU and GPU, respectively (for VGG-13 in both cases). Similarly, SIMDRAM:1 provides 1.9× the performance of Ambit (which also uses a single bank for DRAM computation), on average across all three NNs, with a maximum of 2× the performance of Ambit for VGG-13. Second, even with a single DRAM bank, SIMDRAM always outperforms the CPU baseline, providing 3× the performance of the CPU on average across all NNs. We conclude that SIMDRAM is an effective and efficient substrate to accelerate NN inference.

Key Takeaways and Future Opportunities

This article investigates the benefits of state-of-the-art PIM architectures in mitigating memory bottlenecks during NN inference. We identify the key opportunities and challenges for three PIM solutions that can be employed in edge or cloud environments. We summarize the key takeaways from our analysis as follows.

First, we evaluate the performance of the GEMV primitive, which is a key operation for NN inference, on a commercial general-purpose server-scale PNM architecture (UPMEM) using 32-bit floating-point and integer data types. Our experiments allow us to gain insights on the benefits a real PIM architecture can provide for NN inference. We observe that while GEMV using floating point takes one order of magnitude more time than using integers, the kernel execution time scales linearly with the number of UPMEM processing cores employed. When considering the 32-bit integer GEMV implementation, the UPMEM system provides similar performance to a high-end GPU, even outperforming the GPU when the GPU requires memory oversubscription.

There are two key benefits of the UPMEM system compared to the other two PIM systems. (1) It is relatively easy to scale the UPMEM system to higher memory capacities and computational power by simply adding more UPMEM modules to a system. In contrast, scaling the 3D-stack-based PIM systems requires non-trivial engineering since 3D memory cubes need to be connected using specialized interconnection network. (2) It is relatively easy to program the UPMEM system since UPMEM provides a complete programming toolkit and a C-based programming model for their system. In contrast, for the PUM architecture, the programmer needs to manually map a workload to the underlying substrate, which is an arduous task.

Second, Mensa, a heterogeneous architecture for Google edge NN models that employs 3D-based PNM, greatly benefits many NN models, improving performance (throughput and utilization) and energy efficiency, while at the same time reducing the area footprint of the monolithic Google Edge TPU. The key benefit of Mensa’s 3D-based PNM accelerator compared to the 2D-based PIM designs we evaluate (SIMDRAM and UPMEM) is its flexibility. Since the logic and memory components of a 3D-based architecture are separately manufactured, the design of a near-memory accelerator has no constraints other than the area and power constraints of the logic layer.
This means that, in practice, the 3D-based architecture can accelerate many NN types relatively flexibly. In contrast, 2D PNM and PUM have natural limitations that make them infeasible or unsuitable to support floating-point computation, which is standard for most NN operations. The key drawback of PNM solutions that rely on 3D-stacked memories is the high cost and limited memory capacity associated with 3D memories. This can be a limiting factor in edge environments (since edge devices are often cost-sensitive) and future NN models (since NN model sizes are increasing significantly).

Third, SIMDRA, a 2D-based PUM architecture, provides significant performance improvements for binary neural networks compared to high-end CPUs and GPUs. The key benefit of employing a PUM architecture for NN inference is the massive parallelism available inside DRAM. SIMDRA’s throughput for a 32-bit addition using a single DRAM bank is 2.3× that of a CPU [206] and scales linearly with the number of DRAM banks (up to 36.8× the CPU throughput using all 16 DRAM banks in a DRAM chip [206]) with relatively low area cost (i.e., only 0.2% area overhead in a high-end CPU). SIMDRA is suitable for edge-based and cloud-based environments since it leverages the operating principles of standard DRAM DDRx memories. The key drawback of SIMDRA is its limited applicability for NN models due to the lack of (1) support for floating-point operations and (2) tools (e.g., compilers, programming models) to map NN execution to the underlying hardware substrate.

We believe that there are many opportunities to improve the design of PIM architectures (both 2D and 3D) targeting NN inference, including better manufacturing processes that can seamlessly integrate logic and memory units, cheaper and efficient interconnection networks that can be used to scale up the capacity of 3D-based DRAM systems, and programming support to ease the deployment of PUM approaches. Also, there is a need for programming models and frameworks that can unify the benefits of the different PIM architectures into a single heterogeneous system. Such solutions need to map, schedule, and control the execution of different NNs onto the most appropriate PIM architecture, thereby enabling a

**Sidebar: Related Works on Accelerating NN Inference with Processing-in-DRAM**

**2D PNM.** Beyond UPMEM, other memory manufacturers have announced PNM prototypes using 2D DRAM. Samsung’s AxDIMM [1] integrates reconfigurable logic to DDR4 modules to accelerate recommendation systems. SK Hynix’s GDDR6-based PIM [2] adds MAC units near DRAM banks to accelerate NN inference. Both solutions are not yet available on the market.

**3D PNM.** There is extensive literature on accelerating NN inference using 3D-stack-based PNM [3]. We highlight Samsung’s FIMDRAM [4], an industry proposal (not yet available on the market) that adds MAC units near DRAM banks in an HBM2 device. A common drawback of prior 3D PNM NN accelerators is that they use a monolithic accelerator design, which cannot efficiently accommodate diverse types of NNs. Mensa avoids such issues by tailoring NN accelerators for the needs of different NN models.

**PUM.** DRISA [5] executes bulk operations in DRAM by adding logic elements inside DRAM arrays, providing speedups for binary neural networks. However, adding such logic to the DRAM array incurs large overheads. DrAcc [6] implements in-DRAM addition operations using AND/OR/NOT logic primitives, targeting ternary neural networks. SIMDRA supports a wider range of operations (compared to DrAcc) at lower area overhead (compared to DRISA).

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workload to leverage the benefits of PIM while avoiding particular drawbacks related to a given PIM architecture. We hope that our work brings attention to such challenges and can inspire future PIM system designs.

Conclusion

We analyze, discuss, and contrast the benefits and drawbacks that different DRAM-based PIM architectures provide for NN performance and energy efficiency. To do so, we analyze three state-of-the-art PIM architectures, which broadly cover the PIM design space. Our comprehensive analysis provides several key takeaways. We conclude that while different PIM architectures provide greater performance and energy benefits than compute-centric solutions, different PIM architectures impose different limitations for NN workloads. We hope that our analysis can highlight the opportunities and drawbacks of state-of-the-art PIM solutions and inspire future designs.

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