A self-clocked binary-searching digital low-dropout regulator with fast transient response

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Abstract A self-clocked binary-searching (SCBS) digital low-dropout (DLDO) regulator with fast transient response is proposed. The SCBS controller employed in the DLDO achieves fast transient response and eliminates the need for an external high-speed clock. A transient enhancement unit (TEU) is proposed to reduce the undershoot of the output voltage. The proposed DLDO is simulated in a 40-nm CMOS process with an active area of 0.015 mm\textsuperscript{2}. The simulation results show that with a 15.5 mA/2 ns load step, it shows a setting time of 28 ns with a voltage undershoot of 93 mV, and it achieves a peak current efficiency of 99.87\% by consuming a 19.4-μA quiescent current. Thus, the resulting FOM\textsubscript{1} is 0.379 ps and FOM\textsubscript{2} is 5 ps.

key words: digital low-dropout (DLDO) regulator, fast transient response, self-clocked, binary-searching

Classification: Integrated circuits

1. Introduction

The low-dropout regulator has been widely applied in the system-on-chip to provide power supply for various intellectual properties. The analog LDO (ALDO) can achieve fast transient response and good power supply ripple rejection \cite{1, 2, 3, 4}. With the supply voltage scaling down to the near-threshold or the subthreshold regions, it is hard to implement a high loop gain for the error amplifier of ALDO. The DLDO gains more attention due to its low voltage operation capability and process scalability \cite{5}. In the conventional synchronous DLDO, bidirectional shift resistors are extensively used as control logic to achieve voltage regulation \cite{6, 7}. However, due to only one MOS device is tuned per clock cycle for the operation, the transient response of the DLDO is mainly determined by its sampling frequency. Although increasing sampling frequency can improve transient response, it comes at a large cost in power consumption \cite{8}.

To advance the transient response and power consumption tradeoff, different design techniques are introduced. Asynchronous circuits were proposed in \cite{9, 10, 11, 12, 13, 14} to improve the transient response time without increasing power consumption. However, the delay of asynchronous circuit is sensitive to process, voltage, and temperature variations, which degrades the design robustness \cite{15}. The study from \cite{16, 17} proposed event-driven DLDOs with a proportional-integral controller to shorten the loop latency. \cite{7} employed an analog-assisted loop to enhance the transient response, but the effectiveness is proportional to the turned-on MOS devices. The hybrid synchronous-asynchronous architecture was employed in \cite{18, 19, 20} to improve the transient response and regulation precision. The self-clocked technique was employed in \cite{21, 22}, which eliminates the need for an external high-speed clock and achieves fast transient response. A hybrid LDO is proposed in \cite{23, 24, 25, 26} to achieve fast setting time and good power supply ripple rejection.

In this paper, a self-clocked DLDO employing binary search algorithm is proposed to achieve fast transient response and eliminates the need for an external high-speed clock. In addition, A transient enhancement unit (TEU) is added to reduce the undershoot of the output voltage. This paper is organized as follows. The implementation and design considerations of the proposed DLDO is illustrated in Section 2. Simulation results are shown in Section 3. Finally, Section 4 draws the conclusion.

2. Implementation and design considerations

2.1 Architecture of the proposed DLDO

Fig.1 shows the architecture of the proposed DLDO, which comprises an asynchronous comparator, a transient detection, a self-clocked binary-searching (SCBS) controller, a transient enhancement unit (TEU), and a binary-weighted PMOS switch array. The asynchronous comparator compares the output voltage \( V_{\text{OUT}} \) and the reference voltage \( V_{\text{REF}} \), and defines the value of the signal DIR determines the regulation direction of SCBS controller. High threshold voltage \( V_{\text{REFH}} \) and low threshold voltage \( V_{\text{REFL}} \) set the upper and lower thresholds around \( V_{\text{REF}} \). If \( V_{\text{OUT}} \) is higher than \( V_{\text{REFH}} \) or lower than \( V_{\text{REFL}} \), the output signal RST_N of the
transient detection pulls down, which resets the SCBS controller and triggers the internal self-clocked logic. For the \(N\)-bit SCBS controller, it only takes up to \(N\) cycles, enabling a much smaller setting time. To reduce the undershoot of output voltage, a TEU is employed in the DLDO. After the transient detection detects the increase of load current, the signal RST_N pulls down, resulting in the signal CTRL[5:0] becomes “0111111”. The output signal Droop of the TEU pulls down before the signal CTRL[5] of the SCBS controller, thus increase the response speed of the DLDO and reduce the output voltage’s undershoot. There are six PMOS power transistors in the switch array and the unit current relationship between the PMOS power transistors is that \(I_N=2I_{N-1}\) (1 \(\leq N \leq 5\).

![Fig. 1 Overall architecture of the proposed DLDO](image)

2.2 Self-clocked binary-searching (SCBS) controller  
Fig.2 shows the block diagram of the SCBS controller. The SCBS controller consists of a binary-searching controller and a self-clocked logic. The operation principle of the binary-searching controller is given in Fig.3. Once reset the binary-searching controller, the control word CTRL[5:0] becomes “011111” and hence the most significant bit of switch array turns on. If \(V_{OUT}\) falls below \(V_{REF}\) at the first positive edge of the clock, DIR is set to “High”, and the control word CTRL[5:0] becomes “001111”. Otherwise, if \(V_{OUT}\) exceeds \(V_{REF}\), DIR is set to “Low”, and the control word CTRL[5:0] becomes “101111”. After certain clock cycles, all the bits in the switch array are determined, resulting in the \(V_{OUT}\) reach to the desired voltage level. Consider a situation in which a sudden load transient occurs during conversion steps that results in \(V_{OUT}\) exceed outside the voltage range defined by \(V_{REFH}\) and \(V_{REFL}\), the transient detection will restart the SCBS controller.

The self-clocked logic is composed of an encoder, a frequency doubler[21], an inverter, and a delay cell. The encoder is the core of the self-clocked logic, which needs to generate the flip signal CLK_GEN according to the change rule of the control word CTRL[5:0]. Therefore, the encoder can be implemented by a lookup table shown in Table I. Fig.4 shows the operational waveforms of the self-clocked logic. Once the transient detector detects a load transient event, the signal RST_N is valid, which resets the SCBS controller, and the control word CTRL[5:0] becomes “0111111”, hence the output signal CLK_GEN of the encoder becomes “0”. After the signal CLK_GEN passes through the frequency doubler, the inverter, and the delay cell, the first positive edge of the clock signal CLK is generated. The SCBS controller performs the first search process, and the control word CTRL[5:0] becomes “001111” or “101111”. Regardless of how CTRL[5:0] changes at the positive edge of the clock signal CLK, the output of the encoder will display “1” and trigger the generation of the second positive edge of the clock. The generation process of the subsequent clock is the same as described above.

After certain clock cycles, all the bits in the switch array are determined, resulting in the \(V_{OUT}\) reach to the desired voltage. Due to the output of the SCBS controller is not change until a new load transient event occurs, the output of the self-clocked logic stops toggling and fixes at “high”. The self-clocked logic eliminates the dependence of an external high-speed clock, and no clock signal is generated in the steady state, which reduces the dynamic power consumption of the design.

![Fig. 3 Operation principle of the binary-searching controller](image)
to compare the $V_{OUT}$ with $V_{REF}$, its schematic is shown in Fig.6. The first stage of the asynchronous comparator is a self-biased differential amplifier that performs the comparison between the $V_{OUT}$ and the $V_{REF}$. The complementary self-biased second stage of the asynchronous comparator is to amplify the compared signal $V_X$. The comparison result DIR of asynchronous comparator determines the regulate direction of the SCBS controller.

The architecture of the transient detection is shown in Fig.7. It consists of two asynchronous comparators, an XOR gate, and an edge detection. Fig.8 presents the operational waveforms of the transient detection. A pair of asynchronous comparators sets the upper and lower thresholds around $V_{REF}$. When $V_{OUT}$ higher than $V_{REFH}$ or lower than $V_{REFL}$, the comparison results of the two asynchronous comparators are the same, and the output of the XOR gate is pulled low, hence a narrow low pulse signal RST_N is obtained through the edge detector, which resets the SCBS controller.

2.3 Transient enhancement unit
To reduce the undershoot of the output voltage, a transient enhancement unit (TEU) inspired by the scheme in [27,28] is proposed, as given in Fig.5. The TEU is composed of a high-pass network constructed by a 500F coupling capacitor $C_C$ and an regular-threshold (RVT) inverter with all ports connected, and two low-threshold (LVT) inverters. Since the steady-state voltage of node $V_P$ is larger than the threshold voltage of LVT inverter, the output signal Droop of the TEU is “High” in the steady state. When the undershoot of the output voltage $V_{OUT}$ occurs, $\Delta V_{OUT}$ is coupled to the node $V_P$ through the high-pass network. When $V_P$ dropped lower than the threshold voltage of LVT inverter, the signal Droop pulls down, and the most significant bit of switch array turns on. The signal Droop pulls down before the SCBS controller can respond, thus increase the response speed of the DLDO and reduce the output voltage’s undershoot.

2.4 Asynchronous comparator and transient detection
In this design, an asynchronous comparator [29] is used

### Table I. Lookup table constituting the encoder

| Input:CTRL[5:0] | Output:CLK_GEN |
|-----------------|----------------|
| 6’B011111       | 0              |
| 6’B001111,6’B011111 | 1            |
| 6’B000111,6’B0101116’B100111,6’B110111 | 0        |
| 6’B000011,6’B010011,6’B100011,6’B110011 | 1      |
| 6’B000001,6’B000101,6’B111001,6’B111101 | 0      |
| 6’B000000,6’B000010,...,6’B111100,6’B111110 | 1    |

![Fig. 4 Operational waveforms of the self-clocked logic](image)

![Fig. 5 Schematic of the transient enhancement unit](image)

![Fig. 6 Schematic of the asynchronous comparator](image)

![Fig. 7 Architecture of the transient detection](image)

![Fig. 8 Operational waveforms of the transient detection](image)
3. Simulation results

The proposed DLDO is designed in a 40-nm CMOS process and the layout is shown in Fig.9, where only 50.5-pF total capacitor (C_{OUT} + C_C) is used, and the active area is approximately 0.015 mm² (196 μm × 75 μm). The post-layout simulation results at the input voltage of 0.7 V with a 50-mV dropout voltage are as follows.

![Fig. 9 Layout of proposed digital LDO](image)

Fig.10 shows the simulated transient response when load current changes from 0.25 mA to 15.75 mA within a 2-ns transition edge time (T_{EDGE}). A 93-mV undershoot and a 49-mV overshoot are achieved and the settling time are simulated as 28 ns and 75 ns, respectively. When applying the TEU, the undershoot is reduce from 245 mV to 93 mV (more than 62% reduction), which verifies the proposed TEU scheme.

The current efficiency of the proposed DLDO is depicted in Fig.11, where a current efficiency > 98% is achieved over a range from 1 mA to 15 mA for dc loading conditions. Since the quiescent current of DLDO is independent of the load current, a peak current efficiency of 99.87% is achieved by consuming a 19.4-μA quiescent current.

The simulated load regulation is given in Fig 12. With load current ranging from 1 mA to 15 mA at 0.7-V input voltage, 0.13 mV/mA is obtained.

![Fig.10 Simulated load transient response when load current change](image)

![Fig.11 Simulated current efficiency](image)

![Fig. 12 Simulated load regulation](image)

Table II summarizes the simulated performance in comparison with other recent works. The maximum output current is 15.75 mA, and the simulated quiescent efficiency is 19.4 μA, hence the calculated maximum current efficiency is 99.87%. In the table, two figures of merit (FOM), FOM₁[30] and FOM₂[21] are used, and those are defined by

\[
FOM_1 = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} \times \frac{I_0}{I_Q} \times C_{TOTAL} \quad (1)
\]

\[
FOM_2 = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} \times \frac{I_0}{I_Q} \times T_{SET} \quad (2)
\]

It is observed that the proposed DLDO achieves minimized settling time and small on-chip capacitor. According to the comparison, the proposed DLDO achieves comparable or better performances than the state-of-the-art works.
| Design | Architecture | Process[nnm] | $V_{DD}[\text{V}]$ | $I_{DD}[\mu A]$ | Current Eff [%] | $\Delta V_{OUT}$ | $T_{text}$ | $\Delta I_{LOAD}$ | $FOM_1[\text{ps}]$ | $FOM_2[\text{ps}]$ |
|--------|--------------|--------------|-------------------|-----------------|-----------------|----------------|-----------|-----------------|-----------------|-----------------|
| This Work | SR/AA | ABS/SL/S | SAR/PD | 5C/BS | 65 | 0.5-1 | 0.5-1 | 0.5-1 | 0.7 | 0.45-0.95 | 0.4-0.95 | 0.3-0.45 | 0.65 | 99.97 | 99.99 | 99.8 | 99.87 | 100 | 100000 | 400 | 50.5 |
| | | | | | | 105mV | 25us | 2.5us | 4.3us | 100ns | 0.27mA | 48us | 100ns | 28ns | 168 | 23 | 117 | 5 |

4. Conclusion

A self-clocked binary-searching DLDO with fast transient response has been proposed and demonstrated in a 40-nm CMOS process. Simulation results show that the proposed DLDO achieves an undershoot of 93 mV and a setting time of 28 ns for a load change between 0.25 mA to 15.75 mA within a 2-ns transition edge time. With the proposed TEU scheme, the undershoot of output voltage is reduced by 62%. The quiescent current is 19.4 µA and the peak current efficiency is 99.87%. The proposed DLDO achieves a 0.379-ps FOM$_1$ and a 5-ps FOM$_2$, which is comparable with the state-of-the-art works.

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