Central span switching structure for SAR ADC with improved linearity and reduced DAC power

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Abstract: Zero switching point effect for successive-approximation-register (SAR) analog-to-digital converters (ADCs) is analyzed in this paper. Central span switching procedures are presented based on shifting zero switching points of digital-to-analog converter (DAC) to improve the linearity of SAR ADC and reduce DAC energy. Several central span switching procedures modified from previous merged-capacitor-switching (MCS) and monotonic switching schemes are analyzed, which is central span MCS (CS-MCS) and central span monotonic (CS-MON). By splitting most-significant-bit (MSB) capacitors, CS-MCS and CS-MON have linearity error reduction by a factor of 2 and \( \sqrt{2} \). The DAC switching energy is reduced by 92.2% and 84.4% relative to conventional SAR ADC. With \( V_{cm} \) applied as reference voltage at LSB conversion, the energy reduction can be increased to 96.1% and 92.17%. Moreover, with comparator input transistors split into two parts, the energy reduction of CS-MCS switching procedure can be 95.3% and 97.6% with \( V_{cm} \) reference at LSB conversion. These central span switching procedures are not sensitive to \( V_{cm} \) accuracy since it is the reference only at least-significant-bit (LSB) conversions.

Keywords: SAR ADC, low power, DAC switching procedure

Classification: Integrated circuits

References

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1 Introduction

The popular applications of mobile terminals and devices require low power robust analog-to-digital converters (ADCs) in analog front-end to convert information from the real world into digital data. Among many ADC architectures, successive-approximation-register (SAR) ADCs have higher potential usage under such requirements thanks to advantages of high power efficiency, low complexity, small silicon area and low cost. The switched capacitors with charge redistribution architecture and opamp-less structure with digital control logics of SAR ADCs render them more adaptable to the technology and power supply scaling down, which enable them to achieve higher conversion speed and power efficiency. Numeric works have been done to improve the power efficiency and linearity of SAR ADCs, many of which [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11] focus on switching methods of redistribution digital-to-analog converter (DAC) to reduce the power consumption.

Thanks to the single-end switching method, monotonic switching procedure in [2] achieves both less power and complexity in DAC and control logic. But common-mode induced error in comparator design has to be taken special consideration. Merged-capacitor-switching (MCS) and $V_{cm}$-based switching procedures [3, 4] introduces more energy efficiency by involving extra common-mode voltage. These two switching procedures also have stable common-mode voltage which introduces less dynamic offset and error. Early reset merged capacitor switching (EMCS) method in [6] demonstrates 50% linearity improvement and 41.5% DAC power reduction compared to monotonic switching procedure, which is similar in binary-window structure [7]. Recently, several works [8, 9, 10, 11] propose new switching methods with much less DAC power by adopting $V_{cm} = V_{ref}/2$ as extra reference voltage. Compared to monotonic switching procedure, these works can save more than 90% DAC power. However, since $V_{cm}$ is also the reference for MSB decisions, the linearity are sensitive to $V_{cm}$ accuracy. Therefore, $V_{cm}$ is avoided to be reference or only applied in LSB conversion as reference in switching procedures proposed by this paper. Also, this paper presents several new DAC switching procedures and compares them to other presented switching procedures with linearity enhancement and 50% DAC power efficiency relative to monotonic switching procedure based on zero switching point shift.
This paper is organized as follows. The DAC switching procedure is analyzed in section 2. Simulation results are compared in section 3. The paper is concluded in section 4.

2 Structural analysis

2.1 Zero switching point shift
For any switching methods, if a capacitor is not switched to another reference voltage during conversion, then it is a zero switching point for this capacitor. If comparator decisions are decided by redistribution capacitance of un-switched capacitors, the nonlinearity of those capacitors are not calculated into SAR ADC performance. As a result, zero switching points of capacitors can lead to smaller differential nonlinearity (DNL) and integral nonlinearity (INL).

For conventional switching procedure, zero switching points of all capacitors are placed at differential input of $-V_{ref}$, which is in nature 0 for DNL and INL definitions. But the largest error occurs at 0 differential input or the middle code from 100⋯0 to 011⋯1, where all capacitors are switched to opposite reference voltage and nonlinearity of all capacitors are included. However, in EMCS and binary-window switching procedures, linearity improvement is witnessed by introducing the voltage continuity of DAC and zero switching points at 0 differential input. Compared to conventional switching procedure, EMCS and binary-window switching procedures are applied with different zero switching points to obtain better linearity. The structure and comparison is demonstrated in Fig. 1 with unit capacitance $C$ and $V_{cm} = V_{ref}/2$. To shift zero switching points of capacitors from $-V_{ref}$ to 0 differential input, capacitors have to be switched back after previous conversions. DAC power efficiency can also be extra advantages by shifting zero switching points. But, the complexity of control logic has to be limited in practical applications to suppress unnecessary power consumption and speed penalty on logic circuits. Binary window in [4] is the special case when first four capacitors are un-switched.
Fig. 2. The structure of CS-MCS (with $V_{cm}$) and CS-MON (without $V_{cm}$) switching SAR ADC.

Fig. 3. The example of CS-MCS for a 3b SAR ADC.
2.2 Central span MCS
Based on zero switching point shift, a central span MCS (CS-MCS) for N-bit SAR ADC is proposed in Fig. 2, which is modified from MCS switching procedure. To achieve zero switching point shift, CS-MCS switching procedure splits the most-significant-bit (MSB) capacitor into N-1 capacitors ($C_{k,p}$ and $C_{k,n}$, $k = 1, 2, \ldots, N - 1$) with the same capacitance as following N-1 capacitors ($C_{k+1,p}$ and $C_{k+1,n}$)

$$C_{k,p} = C_{k,n} = 2^{N-2-k} C, \quad k = 1, 2, \ldots, N - 2$$

and

$$C_{N,p} = C_{N,n} = C_{N-1,p} = C_{N-1,n} = C.$$ (di, i = 1, 2, \ldots, N are comparator decisions.) Taking positive DAC as example (negative DAC operates in the opposite switching direction), all MSB capacitors are switched to $V_{\text{ref}}$ and GND according to MCS ($d_1 = 1$ is down to GND and $d_1 = 0$ is up to $V_{\text{ref}}$) after MSB conversion. From the 2nd cycle, if $d_1 \oplus d_k = 1$, $k = 2, 3, \ldots, N - 1$ ($\oplus$ means EOR), then MSB capacitor $C_{k-1,p}$ is switched back to $V_{\text{ref}}$ while capacitor $C_{k,p}$ keeps the previous connection to $V_{\text{cm}}$. If $d_1 \oplus d_k = 0$, $k = 2, 3, \ldots, N - 1$, then capacitor $C_{k,p}$ is switched to $(1 - d_1)V_{\text{ref}}$ and MSB capacitor $C_{k-1,p}$ is un-switched. Fig. 3 illustrates a CS-MCS switching example of 3b SAR ADC. Due to switching circuits of $V_{\text{cm}}$ voltage, control logic for CS-MCS switching procedure is more complex than MCS. But DAC energy reduction and linearity improvement can be obtained, which is analyzed in section 3.

If $V_{\text{cm}}$ is applied as reference voltage at least-significant-bit (LSB) conversion, the total DAC capacitance can be halved so that more DAC switching energy and layout area are saved. Speed benefit can also be obtained from smaller DAC capacitance. The linearity performance is only affected by smaller DAC capacitance, which is not sensitive to the accuracy of $V_{\text{cm}}$ reference at LSB.

2.3 Central span monotonic
Similar to CS-MCS switching procedure, shown in Fig. 2 (without $V_{\text{cm}}$ connection), monotonic switching procedure can be replaced by central span monotonic (CS-MON) switching procedure based on zero switching point shift to provide better static performance. The operation of CS-MON switching procedure is similar to CS-MCS except that it is switched between $V_{\text{ref}}$ and GND. Capacitors are switched back to $V_{\text{ref}}$ to implement zero switching point. Fig. 4 illustrates a CS-MON switching example of 3b SAR ADC.

Also, with $V_{\text{cm}}$ as reference voltage at LSB conversion, CS-MON switching procedure can save more DAC switching energy and layout area. But the linearity performance may be affected by smaller DAC capacitance.

2.4 Central span MCS with comparator input transistors split
Thanks to the introduction of $V_{\text{cm}}$ voltage, CS-MCS switching procedure can save more DAC switching energy by split DAC and comparator input transistors into two parts. Shown in Fig. 5, MSB and rest capacitors are split into two DACs which are connected to different comparator input transistors with the same size. The comparator can be fully dynamic pre-amplifier with a latch, with the gates of input transistors connected to different split DAC. Same switching logic is adopted, so that the linearity performance is unchanged. But the MSB switching cycle consumes 0 DAC switching energy compared to $0.5CV_{\text{ref}}^2$ in previous CS-MCS.
switching procedure. However, CS-MON switching procedure cannot adopt such structure due to $-V_{ref}$ redistribution voltage in MSB switching cycle which will be below GND and affect transistor performance.

Fig. 4. The example of CS-MON for a 3b SAR ADC.

Fig. 5. The structure of CS-MCS with comparator input transistors split into two parts.
3 Simulation results

3.1 Switching energy

As discussed in [1], the switching energy consumed on DAC can be calculated from current flowing through reference voltage $V_{ref}$ and $V_{cm}$. The current is calculated from by the redistribution charge on each capacitor. The switching energy for each cycle is given by equation (1). $t_0$ and $t_1$ are the time before and after redistribution. $Q_C$ is the charge on capacitors which are connected to $V_{ref}$ after DAC switching.

$$E = \int_{t_0}^{t_1} i_{ref}(t)V_{ref}dt = -V_{ref} \int_{Q_{C}(t_0)}^{Q_{C}(t_1)} dQ_C$$

Assuming $V_{cm} = V_{ref}/2$, the DAC energy of MSB cycle for CS-MCS switching procedure is given by equation (2), which equals to DAC energy for MCS switching procedure. For other cycles in CS-MCS switching procedure, DAC energy can be presented by equation (3), which is less than DAC energy for MCS switching procedure. Assuming $v_{p_k}$ and $v_{n_k}$ ($k = 1, 2, \ldots, N-1$, $v_{p_1} = V_{inp}$ and $v_{n_1} = V_{inn}$) are DAC voltages during $k^{th}$ switching cycle. $sp_{1,k,i}$, $sp_{2,k,i}$, $sn_{1,k,i}$, and $sn_{2,k,i}$ represent the connection status of each capacitor $C_i$ at the $k^{th}$ cycle. Connection status equals 1, 0, and 0.5, which means capacitors connected to $V_{ref}$, GND, and $V_{cm}$. $sp_{1,k,i} = sp_{2,k,i} = 1 - d_i/2 - d_k/2$ and $sn_{1,k,i} = sn_{2,k,i} = d_i/2 + d_k/2$ are updated during each cycle. Thanks to differential switching structure of capacitors on $V_{cm}$, it consumes no switching energy. The average DAC energy of CS-MCS switching procedure is $E_{avg} \approx (2^{N-3} - 2^{N-6} - 2^{N-8} - 2^{N-10})CV_{ref}^2$.

$$E_1 = -V_{ref} \sum_{i=1}^{N-1} (C_{1,p}(1-d_i)((v_{p_2} - V_{ref}) - (v_{p_1} - V_{cm}))$$

$$+ C_{1,n}d_i((v_{n_2} - V_{ref}) - (v_{n_1} - V_{cm})))$$

$$= 2^{N-4}CV_{ref}^2$$

Fig. 6. The DAC switching energy of each code of 10b SAR ADC (*comparator input transistors split into two parts).
$E_{k+1} = -V_{ref} \sum_{i=1}^{N-1} (C_{i,p}sp_{k+1,i}(vp_k - V_{ref}sp_{k,i} - vp_{k+1} + V_{ref}sp_{k+1,i})$

$+ (C_{i,p}sp_{k+1,i}(vp_k - V_{ref}sp_{k,i} - vp_{k+1} + V_{ref}sp_{k+1,i})$

$+ (C_{i,n}sn_{k+1,i}(vn_k - V_{ref}sn_{k,i} - vn_{k+1} + V_{ref}sn_{k+1,i})$

$+ (C_{i,n}sn_{k+1,i}(vn_k - V_{ref}sn_{k,i} - vn_{k+1} + V_{ref}sn_{k+1,i})))$

For CS-MON switching procedure, the DAC energy can be calculated through the same method. But the update methods of connection status is different from the MSB-1 cycle, which is $sp_{1,i} = sp_{2,i} = 1 - d_1d_k$ and $sn_{1,i} = sn_{2,i} = 1 - (1 - d_1)(1 - d_k)$.

Since many capacitors are switched back during conversion and MSB capacitors are split to further avoid unnecessary switchings, the DAC energy of CS-MCS and CS-MON switching procedures are reduced by 92.2% and 84.4% relative to conventional SAR ADC. The energy comparison of each code is shown in Fig. 6 for 10b SAR ADC. Note that CS-MON consumes twice the energy of CS-MCS because the switching voltage of each capacitor is $V_{ref}$ not $V_{ref}/2$. If $V_{cm}$ is applied as reference voltage at LSB conversion, DAC energy reduction is 96.1% and 92.17% for CS-MCS and CS-MON switching procedures. With comparator input transistors split into two parts, CS-MCS switching procedure has even better DAC energy performance. The DAC energy reduction is 95.3% and 97.6% if $V_{cm}$ is reference at LSB conversion. The detailed DAC switching energy of different switching procedures are listed in Table I.

| Switching procedure | Average switching energy ($CV_{ref}^2$) | Energy saving | $V_{cm}$ accuracy | INL (same unit capacitance) |
|---------------------|--------------------------------------|--------------|------------------|-----------------------------|
| Conventional        | 1362.3                               | Reference    | unrelated        | Reference                   |
| monotonic [2]       | 255.5                                | 81.25%       | unrelated        | 1                           |
| MCS [3, 4]          | 170.2                                | 87.51%       | unrelated        | 1                           |
| Tri-level [5]       | 42.42                                | 96.89%       | $< V_{cm}/2^N$  | $\sqrt{2}$                  |
| VMS [10]            | 31.88                                | 97.66%       | $< V_{cm}/2^N$  | $\sqrt{2}$                  |
| Sanyal [9]          | 21.33*                               | 98.43%       | $< V_{cm}/2^N$  | $\sqrt{2}$                  |
| HCS [11]            | 15.88*                               | 98.83%       | $< V_{cm}/2^N$  | $\sqrt{2}$                  |
| CS-MCS              | 106.42                               | 92.19%       | unrelated        | 1/2                         |
| CS-MON              | 212.84                               | 84.38%       | unrelated        | $1/\sqrt{2}$                |
| CS-MCS+             | 53.08                                | 96.10%       | unrelated        | 1/2                         |
| CS-MON+             | 106.67                               | 92.17%       | unrelated        | 1                           |
| CS-MCS#             | 63.75                                | 95.32%       | unrelated        | 1/2                         |
| CS-MCS##            | 31.99                                | 97.65%       | unrelated        | 1/\sqrt{2}                  |

*16CV_{ref} reset energy from comparison to sampling is not calculated
+V_{cm} applied as reference voltage at LSB conversion
#comparator input transistors split into two parts
3.2 Linearity

Linearity of SAR ADC can be analyzed by static performance. Thanks to zero switching point shift, the middle code of CS-MCS switching procedure preserves the continuity of capacitors and the INL RMS value is reduced by a factor of 2. This result is demonstrated in Fig. 7 for 10b SAR ADC under 1000 simulations with 3σ capacitor mismatch of σ = 1.6%.

The INL RMS value of CS-MON switching procedure is demonstrated in Fig. 8 under 1000 simulations with the same capacitor mismatch as previous. Compared to monotonic, only half of capacitors are switched for each code, so that a gain of \( \sqrt{2} \) in INL RMS value can be witnessed between monotonic and CS-MON. Also, it is witnessed that monotonic and MCS have similar static performance with same capacitor mismatch. The performance of different DAC switching procedures are summarized and compared in Table I. Due to adopting \( V_{cm} \) as reference voltage at MSB, Tri-level, VMS, and HCS switching procedures are more sensitive to \( V_{cm} \) accuracy, which requires \( V_{cm} \) to be exactly half of \( V_{ref} \). To guarantee \( DNL < 0.5\text{LSB} \), \( V_{cm} \) accuracy has to satisfy \( \Delta V_{cm} < V_{cm}/2^N \). But, if \( V_{cm} \) is applied as reference voltage at LSB, the linearity of SAR ADC cannot be affected by \( V_{cm} \) accuracy. Also, similar to monotonic switching procedure, comparators of

![Fig. 7. The RMS value of INL of CS-MCS for 10b SAR ADC under 1000 simulations.](image1)

![Fig. 8. The RMS value of INL of CS-MON for 10b SAR ADC under 1000 simulations.](image2)
Tri-level, VMS, HCS, and CS-MON switching procedures have to be carefully designed to avoid dynamic offset and extra noise due to common-mode voltage variation during each conversion cycle.

4 Conclusions

In this paper, the effect of zero switching point for capacitors is analyzed, which can improve the linearity of SAR ADC. Several central span switching procedures modified from previous switching schemes applied with zero switching point shift structure are proposed. They can enhance the static performance of SAR ADC while achieve much less DAC energy consumption compared to conventional SAR ADC. Compared to newest switching procedures with $V_{cm}$ as extra reference voltage, central-span switching procedures have better linearity and they are not sensitive to $V_{cm}$ accuracy.

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