PERFORMANCE ESTIMATION OF O-IDMA WITH OPTIMUM DESIGN
CONVOLUTIONAL CODES USING PRIME INTER-LEAVERS

Ravi Prakash¹, Nitant Saubagya², Ajay Kumar Maurya³ and B. B. Tiwari⁴
¹Department of Electronics and communication Engineering university of Allahabad, Allahabad
²,³,⁴Department of Electronics Engineering U.N.S.I.E.T. Purvanchal University Jaunpur

Abstract- Convolutional codes are mainly used in communication systems for error correction purpose. The coded bits depend on design of convolutional coder circuit elements which are basically shift registers and adders. By varying the possible feedback connection of convolutional encoder hardware design, various design topologies are generated which produces different code-words according to design topology. In present article O-IDMA which is supreme technology for mobile communications has been observed qualitatively in terms of BER for different design topologies of encoder. For analysis purpose prime inter-leaver is taken into consideration.

Keywords- O-IDMA, Network topology, Hamming distance, Prime Inter-leaver, LLR (Long likely hood ratio)

I. INTRODUCTION

The multiple access methods are an essential communicational requirements in a multi-user environment. Multiple access techniques are required to meet the demand for high speed and large user handling capability of communication optical networks, which permit multiple user to share the fiber bandwidth. O-IDMA (optical interleave division multiple access) made its attention due to its probable applications for LAN optical networks [1-3]. Inter-leaver is usually working a key component in turbo codes, due to the fact that iterative method of the turbo coding will use interleaved version of information iteratively to produce high coding gain.

A very powerful and widely used a variety of codes, called convolutional codes, which are used in a variety of system including today’s standard wireless, optical and in satellite communication. Convolutional error correcting or channel coding is used to improve the efficiency and accuracy of information transmitted. Convolutional codes are beautiful because they are intuitive, one can know them in many different ways, and there is a way to decode them so as to recover the mathematically most possible message from among the set of all possible transmitted message [4-5]. Other major reason for this is the possibility of achieving real time decoding without visible information losses thanks to the well known soft input Viterbi Algorithm.

In present paper, the convolutional coder of fixed constraint lengths with varying network topology is designed and connected in the IDMA system [6]. Varying the network topology specifies that different possible combinations of shift registers and adders are used in encoder to generate more number of uncorrelated code words and produces larger hamming distance, which increases the error detection and correction ability of codes. Constraint length and network topology are the important parameter of the convolutional encoder. The longer the constraint length, the larger the number of parity bits that are subjective by any given message bit. Because the parity bits are the only bits sent over the channel, a larger constraint length generally implies a greater flexibility to bit errors [7]. The trade – off, though, is that it will take significantly larger to decode codes of long constraint length. So one can not
increase the constraint length at random and expect fast decoding. In this article, varying the network topology and fixed the constraint length makes system more efficient agains the larger number of users and we get reduction in bit error rate (BER).

II. OPTICAL IDMA SYSTEM

The block diagram of optical IDMA system shown in figure-1, having k different users, proposing single path of optical window 1550 nm. It all users having converted in fixed code length, which is assumed to be low rate [8-9]. The chip is interleaved by a chip level inter-leaver. After transmitting through the channel, the bits are seen at the receiver side.

In receiver section, after chip matched filtering, the received signal from the k users are observed. In the receiver side for multiuser detection we have used elementary signal estimator, APP and SDECs having variable iterative mechanisms. The produced LLR are further classified in two ways, one which is produced by PSE and another which is generated by DEC. The concept and ethics involved in CBC has shown in, the function of ESEB and APP decoders are based on users.

![Optical IDMA Transmitter and Receiver Structure](image)

**Figure -1: Optical IDMA Transmitter and Receiver Structure.**

III. PRIME INTER-LEAVER

Random inter-leaver consumes huge memory. This is the drawback of random inter-leaver. To reduce the huge memory space in random inter-leavers a special type of inter-leaver is created that is totally based on prime numbers [9-10]. It provides better performance in comparison to random and tree inter-leaver. The generation number based on seeds, where seeds are only prime number that why it is called prime inter-leaver. separation between interleaved bits on G[N].

Let us assume G [N] = {1, 2, 3, 4, 8………N}
For sake to simplicity let N = 8.
Our aim is to interleave N bits with seed 5 then the generated interleaved bits are as follows.

1——> 1
2——> (1+1x5) mod 8——>6
3——> (1+2 x 5) mod 8——>3
4 ===> (1+3 x 5) mod 8 ===> 8
5 ===> (1+4 x 5) mod 8 ===> 5
6 ===> (1+5 x 5) mod 8 ===> 2
7 ===> (1+6 x 5) mod 8 ===> 7
8 ===> (1+7 x 5) mod 8 ===> 4

So the generated interleaved sequence for G [8]
[1, 2, 3, 4, 5, 6, 7, 8] original sequence
[1, 6, 3, 8, 5, 2, 7, 4] interleaved sequence

The generated interleaved sequence differs each bit by prime length 5. Applying this logic in hardware design, we can generate prime interleaving. This curtails a lot of memory space. By using prime inter-leaver the complex structure of random inter-leavers is simplified and which reduce the size, cost as well as power consumption.

IV. CONVOLUTIONAL CODING

Convolutional codes cares for information by adding redundant bits to any binary data. The convolutional encoder calculates each n-bit symbol (n > k) of the output sequence from linear operations on the current input k-bit symbol and the contents of the shift register(s) [11-12]. Thus, a rate k/n convolutional encoder processes a k-bit input symbol and computes an n-bit output symbol with every shift register update. Convolutional codes are commonly specified by three parameters; (n, k, m).

n = number of output bits
k = number of input bits
m = number of memory registers

The amount k/n is called as code rate. It is a measure of the efficiency of the code. Generally, k and n parameters range from 1 to 8, m from 2 to 10 and the code rate from 1/8 to 7/8 except for deep space applications where code rates as low as 1/100 or even longer have been in employment. Here, the quantity, L is called the constraint length of the coder.

The constraint length L denotes the number of bits in the encoder memory that affect the generation of the n output bits. The constraint length L is also referred to by the capital letter K, which can be confusing with the lower case k, which represents the number of input bits.

4.1 Design of Convolutional Encoder

In designing of convolutional encoder there are two prime constraints. First one is number of shift register and another one is number of Ex-OR gates used in encoder circuit. The constraint length L of a encoder is well-defined as number of shift registers where only one message bit can effect the encoder output, designed as L = m+1, where m represents number of memory elements or shift registers used. As more numbers of shift registers are used in encoder more number of output bits are influenced by single bit, which reduces the chance of error in deciding input bits at receiving side. If we increase the number of adders at output then more number of uncorrelated bits as well as code words produces at output, which increases the d_min (minimum hamming distance) between code wards and increases the error correcting capability of encoder.

4.2 Network Topology Variation of Coders

Network topology is the schematic description of a network arrangement connecting various nodes (Sender & Receiver) through lines of connection. In other words, network topology is the
arrangement of various network elements used in data transmission and formations of interconnection like node and link with each other.

Variation of network topology means changing the different connections from the input to output and changing the feedback path from fixed hardware component of a convolution encoder. By altering the different possible connection from the shift register and adders used in convolutional encoder, the number of loops in network topologies are changed. by using different connections and feedbacks in all possible combinations of network topologies the node and loops and possible signal flow graph is changed. In present example of (1,2) convolutional encoder with two shift register and two adder (fixed), one can draw all possible network topology combinations like (7,1) (7,2) up to (7,7) shown in fig. By adding or deleting various paths from input to output these possible topologies are deduced. We have used all these different network topologies in OIDMA system and calculated BER for each case. By finding the result of BER in each cases., we have derived the optimum network topologies which will give the best result i.e. minimum value of BER, among all.

Network topology -1. Convolutional Encoder- (7, 1).

Network topology -2. Convolutional Encoder- (7,2).

Network topology -3. Convolutional Encoder- (7,3).

Network topology -4. Convolutional Encoder- (7,4).
V. SIMULATION RESULT AND DISCUSSION

The O-IDMA has been implemented on MATLAB programming. The various blocks like
encoder, spreader, inter-leavers and optical channels receiver, de-inter-leaver and decoder blocks are programmed collectively to implement whole IDMA system. The input parameters are being fixed as spread length = 16, data length = 512, constraint length L = 3 and block = 50 for fixed users = 100, inter-leaver is prime and channel is optical having source wavelength 1330nm.

In table – 1, BER performance for block = 50 with all possible seven network topologies of convolutional encoder has been shown. The results show that network topologies 4 and 5 having better result comparative to all topologies. The network topology 4 has the best result that is $7.4219 \times 10^{-6}$ but it is not considered because it avoids the ethos of hardware design since adders $V_2$ has no connection to shift register $Z_2$. The topology 5 having result $9.7656 \times 10^{-6}$ is best and optimum one since it satisfies all the design parameter of encoder. So optimum network topology which is considered for design is (7, 5).

The result for table – 2 which is measured for all the same input parameters as in table – 1 but having block is doubled that is 100. The results also suggest the same trend as in table – 1 that is minimum result of BER for topology 4 and 5 where 4 is discarded due to its design constraints and 5 will be treated as optimum one with BER $6.6406 \times 10^{-6}$. If we compare this result with [ table – 1, BER for topology 5 ($9.7656 \times 10^{-6}$)] it show improvements which clearly correlates the theoretical aspects that is increasing the block produces more number of uncorrelated words and reduces the BER significantly.

Table 1

| Network Topology | Generator $G_1$ | $G_2$ | Generator $G_1$ | $G_2$ | B.E.R. |
|------------------|----------------|------|----------------|------|--------|
| 1                | (7,1)          | 111  | 001            |      | 1.8438×10^{-4} |
| 2                | (7,2)          | 111  | 010            |      | 8.0078×10^{-5}  |
| 3                | (7,3)          | 111  | 011            |      | 2.0391×10^{-4}  |
| 4                | (7,4)          | 111  | 100            |      | 7.4219×10^{-6}  |
| 5                | (7,5)          | 111  | 101            |      | 9.7656×10^{-6}  |
| 6                | (7,6)          | 111  | 110            |      | 9.6094×10^{-5}  |
| 7                | (7,7)          | 111  | 111            |      | 0.0172          |

Table 2

| Network Topology | Generator $G_1$ | $G_2$ | Generator $G_1$ | $G_2$ | B.E.R. |
|------------------|----------------|------|----------------|------|--------|
| 1                | (7,1)          | 111  | 001            |      | 1.7500×10^{-4} |
| 2                | (7,2)          | 111  | 010            |      | 7.8516×10^{-5}  |
| 3                | (7,3)          | 111  | 011            |      | 1.7344×10^{-4}  |
VI. CONCLUSION

The observed results discussed earlier implies the optimum hardware design topology of convolutional codes which suits best for O-IDMA system. Though there are a lot of possible combinations has been designed for varying the connection at adder $V_1$ also. If simultaneously $V_1$ and $V_2$ are varying results should be probably more improved. But overall we conclude that by fixing $V_1$ and varying all possible combinations of $V_2$, we have found best topology with minimum BER is (7,5), network topology 5. If such type of design of convolutional encoder is used in O-IDMA with prime inter-leavers, this O-IDMA may be prominently better alternative for future wireless network and mobile network.

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