1553B self-check abnormal analysis of a certain computer

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Abstract. During the factory test of a certain computer, the 1553B self-test is abnormal. Through the analysis, it is found that the RAMLB signal pin constraint error in the FPGA firmware caused the failure. In the case of a certain difference in the characteristics of the chip, the 1553B extended SRAM storage function is unstable, and the existing drivers and applications use the extended storage area, which eventually leads to unstable communication. This problem was solved by modifying the 1553B driver. The research in this paper enriches the research of computer 1553B communication and provides theoretical support and basis for subsequent development, design, and solving practical problems.

1. Introduction

The data transmission rate of the 1553B bus is 1 Mbps, and 32 words are included in the information. The time is very high, and there is no delay. When the input message is specified and unchanged, the time required is very short. Compared with the general communication network, the data transmission rate is much higher. You can judge whether the message is valid through the report. When RT receives a command from BC or receives a message, the terminal will feedback a status word within a certain time. When the terminal does not feedback the status word, it means that the transmitted message is wrong. This transmission is invalid. The 1553B bus [1-5] is widely used in the field of aerospace and shipping, and many research institutions have studied it.

When a certain type of computer[6-10] was shipped from the factory, the 1553B self-test was abnormal. Read the computer's communication data through the 1553B bus tester and find data errors; at this time, keep the peripheral connection relationship unchanged, and use the 1553B test software to find that it can communicate with the bus tester normally.

2. Problem location

The 1553B chip has only 4K words on-chip storage, of which 0X0400 ~ 0X0FFF can be used as a data buffer, only 96 blocks (Data block5 ~ Data block100, 32 words per block) are used, a total of 3K words, cannot meet the system requirements. Therefore, it is necessary to use an external SRAM to expand the cache storage area. 1553B driver software design corresponding address mapping relationship of receiving and sending buffer as shown in Table 1.

| Subaddress | Mapped address | Remarks |
|------------|----------------|---------|
| 0 (receive)| 0x400          |         |
| 1 (receive)| 0x440          |         |
| 2 (receive)| 0x480          |         |
| ....       | ....           |         |
Further analysis of the fault phenomenon found that: under the operating system shell, manually check the data in the RAM of 1553B, and found that the content of the data to be sent in the test software is inconsistent with the data content in the send buffer written in the SRAM of 1553B. And the test of sub-address 1 ~ 15 is normal, the test data of 16-30 is abnormal, and the abnormal probability is 100%. And when abnormality is found, the upper 8 bits of the data are normal, and the lower 8 bits are abnormal. For the abnormal data transmission and reception, see Table 2. The data content of the board without failure phenomenon is consistent and the probability is 100%.

By looking at the sub-address lookup table and the mapping address of the sending and receiving buffer of each sub-address of RT, it is found that the space of the sending sub-address 16 and above is mapped in the off-chip extended SRAM storage area. Through the investigation, when the 1553B communication self-test accesses the extended SRAM with words, the upper 8-bit data is normal and the lower 8-bit data is abnormal.

### Table 2 Test software to send data and 1553B off-chip SRAM send buffer data comparison

| To send data | Send buffer data |
|--------------|------------------|
| 0x03aa       | 0x03ff           |
| 0x0000       | 0x00ff           |
| 0x0000       | 0x00ff           |
| 0x0000       | 0x00ff           |
| 0x0000       | 0x00ff           |
| 0x552f       | 0x55ff           |
| 0x315a       | 0x31ff           |
| 0x2d34       | 0x2dff           |
| ...          | ...              |

The SRAM chip is a 16-bit memory chip with 18 address lines (SA 0-SA17), 16 data lines (LD0-LD15) and 5 control signals (including / RAMCS, / RAMLB, / RAMUB, / RAMOE, / RAMWE). The control signals are all active low. All control signals and address signals are output through the FPGA. Among them / RAMCS is the chip selection signal, / RAMOE is the output enable signal, / RAMWE is the read-write control signal, / RAMLB is the low 8-bit enable signal, and / RAMUB is the high 8-bit enable signal. According to the design, the SRAM space can be accessed by both the CPU and the 1553B; all accesses are accessed by words (16 bits). According to the above module principle, the fault tree of 1553B extended SRAM storage space lower 8-bit data access exception is shown in Figure 1.
Checking this part of the circuit, the main chips involved include: 1553B protocol chip, SRAM chip, FPGA chip, etc. The above integrated circuit chip procurement channels are normal, the chip quality is guaranteed, and the above chips are also widely used in other modules. Troubleshoot A1 equipment problems. Check the solder joints of the relevant circuits around the external memory of the module under a magnifying glass. The soldering is normal, the solder joints are full, and the same phenomenon occurs in multiple modules and can appear steadily. The possibility of virtual soldering is extremely low. Check the schematic diagram and PCB, the design is based on the chip manual, the chip is used in the correct way, and this part of the circuit is used in other modules. It is a mature circuit and has been used in many projects. Eliminate the design problem of B1 principle. A static code walk through the FPGA code and no abnormalities were found. At the same time, carefully check the timing diagram of the control bridge chip, SRAM access timing diagram, and the timing simulation. The timing relationship was not found abnormal, the FPGA code was normal, and the corresponding logic code was The other modules have been extensively verified and no similar problems have occurred, so FPGA code design issues are excluded.

Look for the FPGA pin constraint file, and find that the low 8-bit chip select signal RAMLB pin of the external expansion SRAM should be PIN_20 pin on the FPGA, but it is actually set to PIN_23 pin in the FPGA pin constraint file, FPGA pin constraint The error is shown in Figure 2, while checking other constraint pins and constraint files, no errors were found. By modifying the pin constraint file in the FPGA, the lower 8-bit chip select signal RAMLB is assigned to the PIN_20 pin on the FPGA. The modified FPGA pin constraints are shown in Figure 3 below.
After modifying the FPGA pin constraints, test in the original fault module, use manual mode to read and write off-chip extended SRAM space, each test 50 times, the result is normal; run 1553B test software, all can work normally, each test 50 times, 1553 Communication is also normal. Therefore, the wrong RAMLB signal pin constraint in the FPGA firmware is the cause of the failure.

3. Mechanism analysis and measures verification

Under the correct constraints of the FPGA pins, the resulting functional diagram is shown in Figure 4. In the FPGA, RAMLB is assigned to zero, that is, the 20th pin of the FPGA is set to output, and the output is logic 0, which is routed through the printed board. The 39 pin LB # signal of the control SRAM is enabled as the lower 8 bits, so that the 39 pin LB # signal of the SRAM chip is always valid.

Under the constraints of FPGA pin errors, the resulting functional diagram is shown in Figure 5. Although the value of RAMLB is assigned to zero in the FPGA, due to the incorrect allocation of RAMLB to 23 pins, the 23rd pin of the FPGA is set as an output and the output is a logic 0, while the 20th pin of the FPGA is used as an unused The pin (Unused pin) is uniformly configured as a three-state input, and is connected to the 39 pin LB # signal of the SRAM through the printed circuit board trace.
As shown in Figure 5, due to an incorrect constraint on the lower 8-bit enable signal pin (RAMLB) in the FPGA firmware design, the LB # pin of SRAM is not properly driven, resulting in the inability to effectively operate the lower 8-bit data line. Leading to the exception of the lower 8-bit data and the higher 8-bit data when accessing the external RAM space in word mode.

According to the setting of double buffer allocation in the driver software, when the device subaddress is 0-15, the 1553B communication only uses the on-chip 4K word storage space of the chip, and the communication is normal at this time; when the device subaddress is 16-31, the The 4K RAM space address cannot meet the buffer requirements, and an externally expanded SRAM space needs to be used. When the device subaddress is 0-15, when the module only uses the internal 4K RAM space, it will not use the external SRAM space, even if the RAMLB constraint is wrong, it will not affect it. When the device sends a sub-address of 16-31, in addition to the internal 4K RAM space, it also needs to use the external expansion SRAM space. The user application uses the sending sub-address 30 as the information channel for self-test information reporting, which results in the correct 8-bit high and low 8-bit errors of all data received by the BC terminal, resulting in an abnormal self-test of a certain type of computer.

Modify the 1553B driver, only allocate the corresponding on-chip storage space of the 1553B chip to the sub-addresses (7-23, 29, 30) used by the system, and the remaining sub-addresses are mapped to 0x400, and the 1553B external storage space is no longer used. See Table 1 for specific sub-address allocation. Use the modified driver software to test and verify the 7-23, 29, 30 sub-addresses in the computer, and the communication is normal.

4. Conclusion
Through the above analysis, the computer 1553B self-test abnormality problem (1553B off-chip RAM read and write data error) is the low 8-bit select enable signal in the FPGA / RAMLB pin constraint error, resulting in 1553B when the chip has certain characteristics differences The extended SRAM storage function is unstable, and existing drivers and applications use the extended storage area, which eventually leads to unstable communication. The problem is accurately located, the mechanism is clear, the problem can be reproduced, and feasible corrective measures are proposed, which are effective.

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