Ultra-low jitter clock distribution for the trigger electronics of the New Small Wheel for the ATLAS experiment

T. Alexopoulos\textsuperscript{a} T. Geralis\textsuperscript{b} P. Gkountoumis\textsuperscript{c,1} L. Levinson\textsuperscript{d} I. Mesolongitis\textsuperscript{e} O. Zormpa\textsuperscript{b}

\textsuperscript{a}National Technical University of Athens, 9, Iroon Polytechniou St., Zografou, Greece
\textsuperscript{b}National Centre for Scientific Research “Demokritos”, Patr. Gregoriou E & 27 Neapoleos Str, Agia Paraskevi, Greece
\textsuperscript{c}CERN, Geneva 23, Meyrin, Switzerland
\textsuperscript{d}Weizmann Institute of Science, 234 Herzl St., Rehovot, Israel
\textsuperscript{e}University of West Attica, 250 Thivon & P. Ralli St., Egaleo, Athens

E-mail: panagiotis.gkountoumis@cern.ch

ABSTRACT: The Large Hadron Collider (LHC) at CERN plans to have a series of upgrades to increase its instantaneous luminosity to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. The increased luminosity drastically impacts the ATLAS trigger and readout data rates. The inner-most station of the ATLAS muon spectrometer, the so-called Small Wheels is being replaced with a New Small Wheel (NSW) system, consisting of Micromegas and small-strip Thin Gap Chambers (sTGC) detectors. The on-detector radiation levels required radiation tolerant electronics. The lower radiation levels on the rim of the NSW allowed utilizing commercial electronic chips, such as Field Programmable Gate Arrays (FPGAs), in the trigger chain of the sTGC detectors. Those FPGAs require an ultra-low jitter clock for the proper operation of their Gigabit transceivers ($4.8 \text{ Gb/s}$ serial links). The initial design was based on a clock provided by a radiation tolerant ASIC designed at CERN, but due to its intrinsic jitter and consequent marginal error rate on the transmission lines, a different approach had to be chosen. An additional clock source based on commercial jitter cleaners, fanout chips and optical transmitters driving dedicated fibers was built. The new scheme provides 64 low-jitter clocks (32 main and 32 redundant) from the radiation-protected area (USA15) to the trigger electronics over 60 m of OM3 fiber.

KEYWORDS: Digital electronic circuits, Radiation-hard electronics, low jitter clock, Trigger concepts and systems (hardware and software)

\textsuperscript{1}Corresponding author.
1 Introduction

The sTGC trigger electronics are placed in an accessible position on the rim of the NSW about 5 m away from the interaction point. The low radiation levels at this point gave the opportunity to utilize commercial devices for the trigger electronics. The simulated radiation levels for the Total Ionizing Dose (TID), Non-Ionizing Energy Loss (NIEL), Single Event Effects (SEE) and magnetic field are presented in Table 1. To transfer the high amount of sTGC trigger data from the on-detector Front-end boards and to perform multiple calculations on the coincidence logic, FPGAs and high bandwidth serial links at 4.8 Gb/s were utilized[1].

For the serialization and data transmission from the front-end boards to the trigger electronics the Trigger Data Serializer (TDS)[2] ASIC was utilized. The later receives the 40 MHz LHC clock by the GigaBit Transceiver (GBTX)[3] ASIC from CERN (housed on the sTGC-Level-1 Data Driver Card (L1DDC)[4] board) and generates a 160 MHz reference clock using an internal PLL. The output data use the Low Voltage Signalling (SLVS) standard.

### Table 1. Simulated Radiation Loads and Magnetic Fields, from[5] for the NSW after 10 years at high luminosity LHC.

|                  | Inner radius (R=1 m)                  | Outer Rim (R=5 m)                  |
|------------------|----------------------------------------|------------------------------------|
| TID ($\gamma$)   | 400 Gy                                 | 16 Gy                             |
| NIEL (fast neutrons) | $2.3 \times 10^{13}$ n/cm$^2$ | $7.3 \times 10^{11}$ n/cm$^2$  |
| SEE (protons)     | $4.2 \times 10^{13}$ p/cm$^2$         | $1.3 \times 10^{11}$ p/cm$^2$  |
| B field          | $\leq 1$ kG                           | 5 kG                               |

The FPGA transceivers require an extra low jitter reference clock to ensure the signal integrity of the transmitting and receiving data. Furthermore, due to the attenuation of the high speed signals over the long twinaxial cables (up to 6 m) repeater chips were also utilized. The attenuation of tin and silver cables is presented in Table 2.
Initially the E-Link and programmable clocks of the GBTX ASIC were used as reference clocks but they proved to be marginal during the data integrity tests due to their high jitter of about 4.3 ps and 10 ps respectively. For this purpose a new clock distribution scheme was designed to deliver a direct low jitter clock to the 288 trigger boards of the NSW over 63 m fibers, but also to preserve the E-Link clocks as a selectable option. This scheme is based on the Si5345 jitter cleaner by Silicon labs and a fanout network. The overall scheme, presented in Figure 1, can be divided into two categories: the on-detector electronics Rim-L1DDC[5]) comprised mainly of radiation tolerant components and the off-detector electronics (ALTI, FELIX and clock distributor board) housed in the radiation-protected area (USA15) consisting of Commercial-Off-The-Shelf (COTS) components. The clock distributor board receives the timing, trigger and control (TTC) stream from the ALTI module and recovers the LHC clock by using a Clock and Data Recovery (CDR) chip (AD2814) from Analog Devices. Then, with the help of a 1:4 fanout buffer (Si53306) from Silicon Labs with an Ultra-low additive jitter of 50 fs the clock is fed to four Si5345 jitter cleaners. Each board provides 32 clocks that are distributed to the on-detector electronics via three 12-channel micro-POD optical transmitter modules and MTP fibers. One distributor board will be used for each wheel providing in total 64 clocks (32 main and 32 redundant). The L1DDC board is equipped with the CERN GBTX and Slow Control Adapter Adapter (SCA) ASICs. The output clock can be selected to be either the GBTX E-Link or the direct clock with the fanout network. The fanout network consists of 1:2 and 2:12 fanout buffers from Texas Instruments with less than 300 fs additive jitter (part numbers CDCLVD2102RGTT and CDCLVD1212RHAT respectively) and a 4:1 fanout buffer from IDT with less than 65 fs additive jitter (part number 854S057BGILF).

**Table 2.** Twinax cable attenuation for tin and silver-plated cables.

| Frequency (GHz) | 0.5 | 1.0 | 2.0 | 5.0 | 10.0 | 15.0 | 20.0 |
|----------------|-----|-----|-----|-----|------|------|------|
| Tin Plating (dB/m) | -0.90 | -1.4 | -2.2 | -4.0 | -7.5 | -10.9 | -14.6 |
| Silver Plating (dB/m) | -0.85 | -1.2 | -1.7 | -3.2 | -4.9 | -6.8 | -8.8 |

![Figure 1. Clock distribution for the NSW trigger electronics.](image-url)
2 The clock distributor board

The clock distributor board is a VME 6U blade that receives the TTC stream from ALTI module over a fiber with an ST connector. An additional LVDS input over SMA connectors bypassing the clock and data recovery chip is also available. Specific layout rules were incorporated to reduce any potential noise that could increase the output jitter. Those rules include specific component placement, shielding of the differential pairs in the internal layers, utilizing dedicated LDOs for each Si5345 channel, use of low ESR capacitors and passive filtering on the input power rail. The Si5345 and microPODs are configured via a commercial Ethernet-to-I2C module running at 10 Mb/s. The Ethernet connection obviates the need for a VME single board computer to configure the board. The clock distributor board is presented in Figure 2.

![Clock Distributor Board](image)

**Figure 2.** The clock distributor board.

3 Radiation tests

The 4:1 fanout chip of the L1DDC board was irradiated with a total dose of $6.54 \times 10^{10}$ n/cm$^2$ and maximum flux of $4.6 \times 10^6$ n/cm$^2$/s at the 5.5 MV HV TN-11 TANDEM Van De Graaff accelerator of NCSR “Demokritos” in Athens. The 2:4 fanout chip with part number CDCLVD1204 which is the same family and technology (CMOS) with the 1:2 and 2:12 fanout chips of the L1DDC was also validated under radiation at Demokritos with a $4.82 \times 10^{10}$ n/cm$^2$ (maximum flux of $2.82 \times 10^6$ n/cm$^2$/s) and $^{60}$Co facility at CERN with a TID of 670 Gy (13.14 Gy/H). In both cases the clock generated by a synthesizer was fed to the PLL of the FPGA via the fanout chips where the lock signal was monitored and a counter based on the received clock was compared to a local one. In all cases no errors or failures were observed during the irradiation period.

4 Results

The whole scheme was evaluated by using the clock distributor with a Si5345 evaluation board as a clock source over the LVDS input and total 110 m ($2 \times 50$ m + 60 m with couplers) fiber cables. The
output of the Rim-L1DDC board was driven to a signal source analyzer with the use of a mini Serial Attached SCSI mini-SAS to SMA adapter. The maximum phase noise jitter was measured to be 1 ps with an integrated bandwidth from 1 kHz to 30 MHz. Xilinx® provides the phase noise mask of their 7-series GTX/GTH/GTP transceivers for 156.25 MHz and therefore a correction factor to the mask point according to the equation shown below was applied.

\[ \text{PhaseNoiseAt}(X) \text{MHz} = \text{PhaseNoPhaseNoiseAt}(Y) \text{MHz} + 20 \times \log \frac{X}{Y} \]

The Phase noise jitter of the GBTX E-Link clock, the GBTX programmable-phase clock and the direct clock of the clock distributor described here compared to Xilinx®’s phase noise mask for CPLL and QPLL are presented in Figure 3.

![Figure 3](image)

**Figure 3.** Phase noise jitter of the direct and GBTX clocks compared to Xilinx®’s phase noise mask.

The eye diagram comparison between the GBTX and direct clock for different links at 4.8 Gb/s using the SLVS standard is presented in Figure 4. The direct clock can increase the open area up to 18% and the UI up to 33% more.

![Figure 4](image)

**Figure 4.** Eye diagram comparison of the 4.8 Gb/s links for both GBTX and direct clocks using IBERT at the router boards.
The 4.8 Gb/s links were also evaluated with the use of a 12 GHz high performance oscilloscope (DSA91204A by Infinium). The eye diagram of the SLVS signal over 8 m silver-plated cable, a repeater and 0.5 m tin-plated cable is presented in Figure 5.

![Eye Diagram of SLVS Signal](image)

**Figure 5.** The 4.8 Gb/s serial links were assessed also with the eye diagram by using a high bandwidth oscilloscope.

### 5 Conclusions

A new scheme using COTS components was developed for the distribution of a low-jitter clock to the FPGA transceivers of the NSW sTGC trigger electronics. This scheme can achieve a maximum of 1 ps jitter measured at the output of the Rim-L1DDC board over 110 m cables (almost double the required length) and the phase noise remains in general below the mask provided by Xilinx®. In total 64 clocks can be distributed by the two clock distributor boards to the L1DDC and from there to the 288 trigger boards with the use of fanout chips. The low jitter clocks with the combination of the repeater chips provide a robust solution for the transmission of the trigger data over long cables using the SLVS standard. IBERT tests on the 4.8 Gb/s links over 5 m twinax cables with a BER of $10^{-14}$ and zero errors, but also eye diagrams on the high speed serial links proved that the new scheme can work reliably. Finally, by using the final NSW electronics and infrastructure it was proved that the direct clock can improve the signal quality of the high speed signals compared to the GBTX clock.

### Acknowledgments

We acknowledge support of this work by the project “DeTAnet: Detector Development and Technologies for High Energy Physics” (MIS 5029538) which is implemented under the action “Reinforcement of the Research and Innovation Infrastructure” funded by the Operational Programme “Competitiveness, Entrepreneurship and Innovation” (NSRF 2014–2020) and co-financed by Greece and the European Union (European Regional Development Fund).
References

[1] P. Gkountoumis, *Electronics design and system integration of the ATLAS New Small Wheels*, 2017 *JINST* 12, DOI: 10.1088/1748-0221/12/01/C01088

[2] J. Wang et al, *Design of a Trigger Data Serializer ASIC for the Upgrade of the ATLAS Forward Muon Spectrometer*, 2017 *IEEE* 64, DOI: 10.1109/TNS.2017.2771266

[3] GBT Project, *GBTX Manual*, 2016 vol. 0.15, private communication

[4] P. Gkountoumis, *LEVEL-1 DATA DRIVER CARD - A high bandwidth radiation tolerant aggregator board for detectors*, *PoS* MPGD2017 (2019), DOI: 10.22323/1.322.0036

[5] R. Edgar et al, *Radiation and Magnetic Field Environment for NSW Electronics*, 2017 v.3, 1470513 | ATL-M-NG-0014