Advances In Vertical Solid-State Current Limiters For Individual Field Emitter Regulation In High-Density Arrays

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Abstract. We report the design, fabrication, and characterization of improved solid-state elements intended for individual regulation of field emitters part of high-density arrays. We demonstrate a high-yield, CMOS compatible fabrication process of single-crystal, vertical, ungated, n-type silicon field-effect transistors (FETs); each device behaves as a current source when is biased at a voltage larger than its drain-source saturation voltage. An ungated FET in saturation connected in series to a field emitter can compensate for the wide variation in current-voltage characteristics of the field emitters due to the tip radii spread present in any field emitter array, which should result in emitter burn-out protection, larger array utilization, and smaller array emission non-uniformity. Using 1-2 Ω·cm single-crystal n-Si wafers, we fabricated arrays of 25 μm tall vertical ungated FETs with 0.5 μm diameter that span two orders of magnitude of array size. Experimental characterization of the arrays demonstrates that the current is limited with > 3.5 V bias voltage to the same ~6 μA (6 A.cm⁻²) per-FET value. Finite element simulations of the device predict a saturation voltage close to the experimental value and a saturation current within a factor of two of the experimental value.

1. Introduction

Field emission is the quantum tunneling of electrons into vacuum from the surface of metallic or semiconducting materials due to the presence of a high electrostatic field (> 3x10⁷ V/cm) that narrows the potential barrier that traps the electrons within the material, i.e., workfunction [1]; a field emitter with a nanoscaled tip radius is capable of generating such electrostatic fields at a low (< 100 V) voltage [2],[3]. Field emitter electron sources are an attractive alternative to thermionic cathodes because they can be switched faster [4], work at a lower vacuum [5], consume less power, and produce electron beams with lower energy spread and higher brightness. Field emitter arrays (FEAs) are implemented to increase the total current from a field emission cathode and have been used in field emission displays [6], high-frequency amplifiers, gas ionizers [7],[8], X-ray sources [9],[10], multi-electron beam lithography, and other vacuum microelectronic and nanoelectronic devices. However, field emission current has an exponential dependence on the emitter tip radius, and, unfortunately, arrays of nano-sharp emitters can have associated tip diameter distributions with long tails [11]. Variations of tip diameters across an array of emitters lead to non-uniform emission. At a given bias voltage the duller tips might not be active while the sharper tips are already burned-out, which can cause severe array subutilization.

Researchers have proposed technologies to regulate the current emitted by FEAs, including p-n junction diodes operated in reverse bias [12], linear resistors [14], and CMOS transistors [15].
However, these approaches are not ideal because they cannot attain high enough current per tip, are not power efficient, or only regulate clusters of emitters that still present emission non-uniformity within the cluster. Our group pioneered the use of vertical ungated field-effect transistors (FETs), i.e., high aspect-ratio, single-crystal, n-type silicon columns, that are operated in saturation to limit the current of each field emitter [16]. The technology takes advantage of velocity saturation of carriers and channel pinch-off in a semiconductor to implement a current source-like ballast component that occupies the footprint of the emitter, leaving unaltered the emitter density of the FEA [17]. We previously demonstrated FEAs with 1 µA per emitter and 1 A.cm⁻² current density with this structure [18]; more recently, we reported characterization of a scaled-down version of the vertical limiters with per-emitter saturation currents up to 0.1 µA [19]. In this work, we report ungated FETs that achieve current saturation with ~3.5 V bias voltage and that limit the current to ~ 6 µA (6 A.cm⁻²).

2. Device Design and Modeling

Extensive axisymmetric process simulations of high aspect-ratio, single-crystal silicon columns were conducted using the SILVACO software (Silvaco International, Santa Clara, CA). Using the process simulation results, the electrical response of the devices was simulated and the parameters of the transistor, i.e., drain-source saturation current $I_{ds}$, drain-source saturation voltage $V_{ds}$, linear conductance $g_{lin}$ (inverse of the drain-source resistance for bias voltages significantly lower than $V_{ds}$), and output conductance $g_{out}$ (inverse of the drain-source resistance for bias voltages significantly higher than $V_{ds}$) were obtained.

In a first set of simulations, the cross-section of the device is circular with a 0.5 µm diameter, the channel length was set at 25 µm, and the doping concentration was varied between $10^{12}$ and $10^{16}$ cm⁻³; the transistor parameters obtained are shown in Figure 1. Through variation of the doping concentration only, the same structure can deliver a saturation current between 20 µA and 14 µA with a saturation voltage between 0.06 V and 7.15 V. In addition, the output resistance is at least two orders of magnitude larger than the linear resistance, evidencing the current source-like behavior of the ungated FET when biased at voltages larger than $V_{ds}$, which results in a better capability of the ungated FET to regulate current compared to a linear resistor. For a doping concentration of $4 \times 10^{16}$ cm⁻³ (resistivity ~ 1-2 Ω.cm), $I_{ds}$ is equal to 3.0 µA and $V_{ds}$ is equal to 3.7 V.

![Figure 1](image)

**Figure 1.** Finite element modeling results of the saturation current vs. doping (left), saturation voltage versus doping (center), and linear/output conductance vs. doping (right) for an ungated FET with a 0.5 µm diameter cross-section and channel length equal to 25 µm.

In a second series of simulations, we varied the channel length between 10 µm and 80 µm for an ungated FET with a 0.5 µm diameter cross-section made of n-Si with a doping concentration equal to $2 \times 10^{15}$ cm⁻³; the transistor parameters obtained are shown in Figure 2. There is great modulation in the saturation current for variation on the channel length, but there is only a moderate variation in the saturation voltage of the transistor, with minimal changes in $V_{ds}$ for channel length above 40 µm.
3. Device Fabrication

Arrays of vertical ungated FETs were made using single-crystal, n-type, silicon wafers with a resistivity equal to 1-2 $\Omega \cdot \text{cm}$. First, 25 $\mu$m-tall columns with 1 $\mu$m diameter cross-section are patterned on the substrate with deep reactive-ion etching, and the silicon around the columns is recessed by 2 $\mu$m so that the tops of the columns are taller than the surrounding silicon (Figure 3(a)). The columns are then thinned to a 0.5 $\mu$m diameter cross-section using wet oxidation (Figure 3(b)). Next, the gaps around the columns are filled-in with a 1.5 $\mu$m thick TEOS film (Figure 3(c)). After that, the oxide on the tops of the columns is etched back using plasma etching, which exposes the silicon core (Figure 3(d)). Finally, a 1.5 $\mu$m-thick aluminium film on top of a 10 nm-thick titanium film is sputtered on the top surface of the wafer, patterned, and sintered to form ohmic contacts (Figure 3(e)). Scanning electron microscope (SEM) images of the fabricated chip with a close-up of array of a 11 by 11 ungated FET array are shown in Figure 4.

![Figure 3](image)

Figure 3. Selected SEM images of the fabrication process: (a) cross-section of an array of 11 high aspect-ratio silicon columns, each of which will form the channel of an ungated FET; (b) close-up of a silicon column after thinning; (c) close-up of a silicon column after the cavity filling-in; (d) close-up of a silicon column after the oxide on top has been removed, leaving the silicon intact; (e) metallized top.
4. Device Characterization

Current-voltage ($I-V$) characteristics of arrays of ungated FETs with different array size were obtained using a probe station using an Agilent 4156C semiconductor parameter analyser; arrays of 1, 4, 16, 64 and 121 ungated FETs were characterized. During the measurements, the substrate (hence the source end of the channel) was held at 0 V, and a positive voltage $V_{ds}$ was applied to the drain contact (the top of the structure). The results of the experiments are shown in Figure 5; in the figure, we assumed that the FETs part of the same array operated uniformly, that is, we divided the measured current by the number of FETs present in the array to calculate the per-ungated FET current-voltage characteristics. For $V_{ds} < 0.5$ V, the characteristics of the ungated FETs are linear; for $V_{ds}$ between 0.5 V and about 3.5 V, there is a transition regime between the linear operation (no channel pinch-off) and saturated operation (channel pinched-off); for $V_{ds} > 3.5$ V, the ungated FET behaves like a current source, that is, it delivers a certain current while having associated a high impedance, resulting in small variation in the current for a significant variation in $V_{ds}$. The average saturation voltage is ~3.5 V, which is very close to the expected value from the finite element simulations; the average saturation current per ungated FET is 6 $\mu$A, which is within a factor of two from the value predicted by the finite element simulations.

![Figure 4](image1.png)

**Figure 4.** Fabricated chip (left) and close-up of an 11 by 11 array pad (right).

![Figure 5](image2.png)

**Figure 5.** Per-ungated FET current-voltage characteristics from arrays of ungated FETs spanning a range of between 1 and 121 elements. The data demonstrates uniform array operation.
5. Conclusions
We demonstrated improved solid-state ballasting elements intended for individual regulation of field emitters part of high-density arrays. The devices are single-crystal, vertical, ungated, n-type silicon FETs that behave as current sources when biased at a voltage larger than their drain-source saturation voltage. Using 1-2 Ω·cm single-crystal n-Si wafers, we fabricated arrays of 25 μm tall vertical ungated FETs with 0.5 μm diameter cross-section that spanned two orders of magnitude of array size. Experimental characterization of the arrays demonstrates that the current is limited with > 3.5 V bias voltage to the same ~6 μA (6 A·cm⁻²) per-FET value. Finite element simulations of the device predict a saturation voltage close to the experimental value and a saturation current within a factor of two of the experimental value.

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