A Study and Analysis of High Efficiency CMOS Power Amplifier for IoT Applications

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Abstract. This paper presents a study and analysis of high efficiency CMOS power amplifier (PA) for Internet of Thing (IoT) application. The studied mainly focused on the topology employed in designing high efficiency PA in gigahertz range frequencies. This study covers the basic class-E PA and the topologies in designing class-E PA such as single-stage, two-stage, multistage and differential. The circuits structure and the performances of class-E PA is discussed. The analysis is focusing on the efficiency of the proposed PA. The latest CMOS PAs developments have been studied and a summarization of the performance specification for different topologies are elaborated.

1. Introduction

The number of internet-connected devices is expected to increase rapidly in the near future. The different electronic devices such as laptops, mobile phones, cameras, game consoles, printers, etcetera, are most commonly utilized wireless communication systems [1]. Moreover, the Internet of Things (IoT) has received considerable attention in recent years for low-power applications. Low power and low-cost wireless connectivity are becoming a necessary and highly demanding. Prolonging battery life and improving the sensitivity of the front-end of devices are the major concerns of such applications [2].

The main part of the IoT devices is transceiver, which consists of some blocks, such as low noise amplifier (LNA), mixer, analog to digital converter (ADC), power amplifier (PA), etc. The PA plays an important role in RF transceivers due to it consumes high power [2]. Besides, the efficiency will reduce while the power consumption will increase when using inductors and large size transistors in PA. Therefore, efficient and low power consumption power amplifiers are necessary for IoT applications [3].

Figure 1 shows the typical radio frequency (RF) transceiver structure consist of mixer, LNA, phase locking loop (PLL), voltage controlled oscillator (VCO) and PA [4]. The upper part of the structure is receiver. As signal is received by the antenna and is preprocessed by the filters and the LNA. After that, the mixer and the local oscillator (LO) will perform frequency down-conversion with a low intermediate frequency (IF). The filter and the IF amplifier are designed to achieve output suitable baseband signal for the ADC. On the other hand, the bottom part is the transmitter. Mixer and LO are used to perform frequency up-conversion with baseband signal outputting by digital to analog convertor (DAC). The next filter will extract the useful signal and transfer to PA. Lastly, the RF signal
can obtain sufficient power from PA and emit out via antenna. The radiation output power mostly supplied by PA. Hence, the ability of radiation output is mainly identified by PA. In wireless transceivers, greatest power budgets are required for PA. The PA usually works at final phase in a RF transceiver system as shown in Figure 1. Moreover, PA supply sufficient output power to resolve transmitter’s path loss in the RF transceiver system. Hence, a high efficiency PA plays an important role to enhance the RF transceivers performance [5].

The aim of this paper is to study and analysis the topologies of highly efficient CMOS PA for IoT’s transceiver. Its focuses on identifying the various topologies of the PAs design in the transceiver structure. This study will be started by briefly explain the basic class-E PA, further, the various topologies for designing highly efficient PAs, such as class-E PA, single-stage and two-stage PA, multistage PA and differential PA is analysed. The performance and topology used of the studied references will be analysed and summarised in a table for comparison. At the end of this research, the best topology with high efficiency, low power consumption and simpler circuitry will be identified.

2. CMOS PA Design Topologies

The various topologies of the PAs have been proposed in the previous works. The topologies can be classified into single-stage, two-stage, multi-stage and differential.

2.1. Single-stage and Two-stage PA

Power efficiency in switched common source class-E PAs is commonly obtained at the expense of device stress [7], [8]. The long-term reliability can be improved, and the voltage drops across a single device can be reduced by implementing device stacking. In [9], this paper discussed about the cascode-based topologies, introduced ways for design optimization and analyzing the loss mechanisms as shown in Figure 2. A circuit solution to reduce the effect and a new dissipative mechanism using specification of the cascode topology have been proposed. The proposed design using 0.13 μm CMOS technology achieve 67 % power-added efficiency (PAE) and 23 dBm peak power at 1.7 GHz frequency [9]. In addition, the proposed PA also shows that, at 1.4 - 2 GHz frequency range, PAE is more than 60 % is achieved [9].

In [10], a common source class-E PA using cascode topology at driver stage is presented. The biasing is implemented using current mirrors. Four transistors with 61 fingers are used for the power stage. In addition, low pass resonant (LC) circuit is applied with surface mounted capacitor and
external microstrip. The schematic of proposed two-stage class-E PA is shown in Figure 3 [10]. The proposed design obtained 40% PAE and 21.3 dBm output power at supply voltage 3.3 V. The weakness of this proposed PA is the implementation of microstrip lines as a matching circuit and applied off-chip inductors, capacitors [10].

![Figure 3. Two-stage class-E power amplifier schematic [10].](image)

Next, in [11], a two-stage CMOS PA is implemented using ADS tool with 0.13 μm RF CMOS technology, at 2.4 GHz with DC supply 2.5 V. The proposed design obtained 20.03 dBm output power at 1 dB compression point and 22.00 dBm maximum output power. In addition, 44.67% PAE at 1 dB compression point and 70.20% maximum PAE are obtained for the proposed design. The input return and output return losses are -11.13 dB and -12.47 dB respectively. Small signal gain and isolation loss are 43.75 dB and -61.89 dB respectively. This proposed circuit obtain 42.73 dB power gain at 1 dB compression point. Moreover, 0.0901 A total DC current flowing via this circuit [11]. To minimize total DC current, MOSFET only bias circuits are implemented. The proposed design is for WLAN applications. Figure 4 shows the complete two-stage CMOS PA schematic [11].

![Figure 4. Two-stage CMOS power amplifier schematic [11].](image)

In [12], cascode driver stage is implemented to obtain high output gain ability. Figure 5 presents the proposed two-stage PA schematic [12]. The class-A PA is implemented at output stage to achieve high linearity level for the proposed PA. The implementation of cascade driver stage in the proposed design provides high gain signal. Thus, the proposed PA performed higher gain as compared to traditional two-stage PAs. The independent bias supply provides more constant DC power than simple bias circuit structure. The proposed two-stage PA obtained 12.6 dB output gain and 31.2% PAE, working at 4 GHz [12]. The experimental results identified that the proposed design consumed less than 37 mW power [12].
A low-power CMOS class-E Chireix RF out-phasing PA has been proposed in [13]. The proposed design is suitable for WLAN applications. This proposed design using cascode class-E topology with Chireix power combiner with a floating load and two-stage configuration. Figure 5 shows the schematic of the out-phasing PA [13]. The Chireix combiner consists of two residual inductances (LA, LB). The class-E topology using the current-reused and self-biased technique to prevent the use of thick-oxide transistors and improve the power gain and driving ability. In addition, by preventing the implementation of isolation resistance, the Chireix combiner able to enhance efficiency and minimize power loss. The proposed design obtained 29.9 % average PAE and 21.4 dBm maximum output power at 2.4 GHz with power supply 2.5 V. The proposed design obtained 38.8 dB power gain when worked for minimum input levels at 2.5 V. 3 % of error vector magnitude and 62 % peak drain efficiency are obtained for WLAN OFDM signal with 20 MHz. Furthermore, the out-phasing PA is integrated with TSMC 0.18-μm CMOS technology. The chip area of the design involving testing pads is 1.07 x 1.17 mm² [13].

Next, a single-stage PA and two-stage PA, working at 2.4 GHz are presented in [14]. By implementing optimized impedance matching and harmonic suppression technologies, the proposed PAs can obtain high efficiency and high gain. There have two harmonic suppression circuits implemented in this design, 2 inductors and 2 capacitors are added at each stage of the PA [14]. Therefore, this can inhibit the harmonic frequency at 2.4 GHz. The overall efficiency of the PAs can be improved by implementing the suppression circuits. The proposed single-stage and two-stage PA
are connected with 4.2V VCC supply. Input and output impedances are matched to 50 ohms. The simulation result and experimental results are introduced. For the proposed single-stage PA, the simulated PAE is 53 % and the simulated gain is 17.58 dB, while the experimental PAE is 49.5 % and the experimental gain is 16.7 dB [14]. Besides, for the proposed two-stage PA, the simulated PAE is 55 % and the simulated gain is 34.6 dB, while the experimental PAE is 53.1 % and the experimental gain is 30.5 dB. Figure 7 shows the proposed two-stage class-E PA schematic [14].

![Figure 7](image1.png)

**Figure 7.** Two-stage class-E power amplifier schematic [14].

### 2.2. Multistage PA

In [15], a multistage class-AB PA with high PAE and appropriate linearity for WLAN applications is presented. Figure 8 shows the schematic of optimized PA [15]. The open-circuited third harmonic control circuit improves the PA efficiency without affecting the class-AB mode linearity. The voltage and current waveforms are simulated to assess the suitable operation for the modes. The efficiency of the proposed controller has been proved by comparing proposed technique with another techniques using simulation study under different conditions. The proposed design obtained 31.6 dBm output power, 37.6 % PAE and dissipated 34.61 mA with 1.8V supply [15].

![Figure 8](image2.png)

**Figure 8.** Optimized power amplifier schematic [15].

In [16], a dual-level and dual-band Class-D CMOS PA have been successfully designed with standard 0.18-μm CMOS process for IoT applications. Figure 9 shows the proposed Class-D PA schematic [16]. The proposed PA can work in dual-level mode, which are low and high output power modes by implementing a tunable PA stages which controlled by a single bit switch. All the stages are turned on at high-level mode, while the stages are scaled at low-level output power mode, only certain part of PAs work, so that the performance of PAE over a wide range of output power levels can be maintain. In addition, the PA can also work in dual-band mode by utilizing a tunable band matching circuit. The proposed PA obtained 16–19 dBm output power and more than 20 dB gain at the 600/780 MHz bands [16]. The maximum efficiency of dual-band PA for the low output power mode is 36.6 %, while high output power mode is 46.66 % [16].
In [17], a design of linear PA with low power consumption and high gain for IoT applications is presented. Integration of driver stage boosted the gain of the PA. A passive linearizer is used to reduce the effect of Cgs capacitance. This enhances the efficiency and linearity of the PA while obtain 19 dB of gain between 2.4 to 2.5 GHz. The designed PA obtained 19.6 dB power gain and 29.71 % PAE at 15.9 dBm maximum output power. The OIP3 is 21 dBm at 18.0 V drain voltage [17]. The designed multistage PA with passive linearizer is a technique to enhance the gain and linearity of the 180nm CMOS PA without affecting the efficiency and maximum output power at the operating frequency. The proposed high gain multistage PA schematic design is showed in Figure 10 [17].

2.3. Differential PA

In [18], a transformer-based differential fully integrated CMOS class-E PA working at 1.8 GHz is designed. The designed PA obtains 29dBm output power and 38.7 % PAE [18]. In the designed architecture, a new output circuit is designed to function as waveform-shaping network and power combining device. Thus, the proposed PA can minimize power loss and smaller footprint. The designed PA implemented with 0.35-µm CMOS technology. The schematic of differential Class-E PA with proposed balun power combination is showed in Figure 11 [18].
In [19], a novel mode-locking differential cascode PA has been designed to increase power gain and reduce time delay. **Figure 12** shows the proposed PA schematic [19]. The drain voltage of the CS transistor was connected to the input of the cross-coupled transistor. Hence, this can increase the breakdown voltage for CMOS devices. By implementing this technique, the time delay between the cross-coupled transistors and CS was minimized. Therefore, the harmonics can be reduced while the benefit of mode-locking technique maximized. The signal was distorted by harmonics generated from excessive time delay. The proposed design obtained 13.2 dB power gain, 34.9 % PAE and 23.32 dBm saturated output power [19].

**Figure 12.** Mode-locking technique power amplifier [19].

A new differential class-E PA with complementary CMOS cross-pair and capacitive cross-coupling neutralization has been successfully designed in [20]. The proposed PA can obtain high PAE, gain and output power for IoT applications. **Figure 13** shows the proposed PA schematic [20]. The proposed PA obtained high power gain, high PAE and greater reverse isolation by implementing fully differential and cross coupling neutralization topology in class-E PA. Power consumption and THD can be reduced by implementing tuning LC tank oscillator and cross coupled pair structure. Besides, cross coupled capacitor able to enhance the design performance. In addition, differential topology led to high PAE, however cross coupled neutralization led to high power gain and PAE. The advantage of the design is implementing cross capacitor wisely. Hence, the capacitor applied can minimize the die size and provide stability enhancement. The proposed Class-E PA obtained 36 dB power gain, 43.5 % PAE and 29.5 dBm output power at 2.4 GHz [20]. Moreover, 0.9 W of power has been transmitted to load in the proposed PA. Post layout is simulated to verify the results of the proposed PA, which implementing 0.18-μm standard CMOS technology [20].

**Figure 13.** Differential class-E power amplifier with complementary CMOS cross-pair and capacitive cross-coupling neutralization [20].

3. Summary of Findings
Generally, the PAE of PA decreases as the frequency increases due to an increment in the parasitic losses. There are many proposed PAs were designed in cascode topology to relieve the device stress. Meanwhile, the inductors have been implemented by utilizing bond wire to achieve high Q factor, thereby leading to higher efficiency. In order to minimize the losses in $R_{on}$ resistance, a larger size
transistor or multiple transistors in parallel was implemented in the amplifier stage. In addition, the supply voltage is proportional to the output power.

From this studied, a comparison of CMOS PA is summarized in Table 1. As can be seen, a class-E PA at 2.4 GHz is the best candidate of power amplifier for IoT applications as proposed by the previously published works. The class-E PA has advantage of achieving higher efficiency. In addition, the two-stage topology with simpler PA circuitry able to attain highest PAE approximately 55 % [14]. Besides, there are also some proposed PAs have been conducted on multistage topology. However, the PAE obtained was less than 50 %. On the other hand, the fully differential topology PAs can deliver high PAE and high output power simultaneously. The highest PAE and output power were obtained from this studied is about 43.5 % and 29.5 dBm, respectively at 2.4 GHz [20].

This studied shows that the most desirable topologies for high efficiency CMOS PA for IoT applications are class-E topology with two-stage or cascode structure due to their high PAE, high gain and high output power performance.

4. Conclusion
A high efficiency CMOS PA for IoT applications has been studied. Based on previously published works, the higher PAE can be achieved by CMOS PA is approximately 55 % only. The PAE of PA still unable to obtain theoretically 100 % PAE, even technology scaling down, device stress, driver stage and inductors losses have been studied in PA design. The CMOS PA for IoT applications was found that facing difficulty to attain high efficiency as the frequency increasing, but the output power limited approximately range of 1 W only. As up to year 2018, most of the proposed PA design still using 0.18-μm CMOS process for CMOS PA design, this proves that selection of technology can be said that not the main focus on designing high efficiency CMOS PA. Authors trust that, in the near future, a new technique which can improve PA efficiency could be found.
## Table 1: Comparison of CMOS power amplifier

| Tech. (um) | Freq. (GHz) | Vdd (V) | Pout (dBm) | Gain (dB) | PAE (%) | Area (mm²) | Technique | Weakness | Application |
|------------|-------------|---------|------------|-----------|---------|------------|-----------|----------|-------------|
| [9]        | 0.13        | 1.7     | 2.5        | 23        | -       | 67         | - Cascade topology - Class-E PA | - Low frequency - High voltage supply | Portable wireless |
| [14]       | 0.18        | 2.4     | 4.2        | -         | 34.6    | 55         | - Two-stage PA - Class-E PA | - Poor linearity - Cost more input DC power - Transmit signals-longer distance (security & privacy) - High voltage supply | IoT |
| [16]       | 0.18        | 2.4     | 3.3        | 19        | 20      | 46.66      | - Dual-level & dual-band Class-D PA | - High voltage supply | IoT |
| [11]       | 0.13        | 2.4     | 2.5        | 20.03     | 42.73   | 44.67      | - Two-stage PA - Cascade topology | - More complex circuit design - Quite less PAE - Average output power | WLAN |
| [20]       | 0.18        | 2.4     | 1.8        | 29.5      | 36      | 43.5 0.47  | - Cross coupling neutralization - Differential topology - Class-E PA | - Implemented off-chip inductors & capacitors - Implemented microstrip lines as matching network - High voltage supply | IoT |
| [10]       | 0.18        | 2.4     | 3.3        | 21.3      | 14.3    | 40 0.43    | - Two-stage PA - Cascade topology - Class-E PA | - Implemented off-chip inductors & capacitors - Implemented microstrip lines as matching network - High voltage supply | WLAN |
| [18]       | 0.35        | 1.8     | 3.3        | 29        | -       | 38.7 1.53  | - Transformer-based - Differential topology - Class-E PA | - Low frequency - High voltage supply | - |
| [15]       | -           | 2.4     | 1.8        | 31.6      | -       | 37.6       | - Multistage class-AB PA | - | WLAN |
| [19]       | 0.18        | 2.4     | 3.3        | 23.3      | 13.2    | 34.9       | - Differential topology - Cascade topology | - More complex circuit design - Quite less PAE - Average output power - High voltage supply | IoT |
| [12]       | 0.18        | 4       | 1.8        | -         | 12.6    | 31.2       | - Two-stage PA - Cascade driver stage - Output stage: Class-A PA | - High power consumption | RFID & IoT |
| [13]       | 0.18        | 2.4     | 2.5        | 21.4      | 38.8    | 29.9 1.25  | - Two-stage PA - Cascade topology - Class-E PA - Chireix RF out phasing PA | - High voltage supply | WLAN |
| [17]       | 0.18        | 2.5     | 1.8        | 15.9      | 19.6    | 29.71      | - Multistage PA | - | IoT |

### Acknowledgment

The author would like to acknowledge the support from the Fundamental Research Grant Scheme (FRGS) under a grant number of FRGS/1/2018/TK04/UNIMAP/02/8 from the Ministry of Education Malaysia.
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