BaPipe: Exploration of Balanced Pipeline Parallelism for DNN Training

Letian Zhao†, Rui Xu†, Tianqi Wang†, Teng Tian†, Xiaotian Wang†, Wei Wu†, Chio-In IEONG‡, and Xi Jin∗†§

∗State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei, China
†Institute of Microelectronics, Department of Physics, University of Science and Technology of China, Hefei, China
‡Huawei Technologies, Shenzhen, China

Emails: {zhaolt, xray, tqwang, tianteng, wxtdsg, wuw1993}@mail.ustc.edu.cn,
ieong.chio.in@huawei.com, jinxi@ustc.edu.cn

Abstract—The size of deep neural networks (DNNs) grows rapidly as the complexity of the machine learning algorithm increases. To satisfy the requirement of computation and memory of DNN training, distributed deep learning based on model parallelism has been widely recognized. We propose a new pipeline parallelism training framework, BaPipe, which can automatically explore pipeline parallelism training methods and balanced partition strategies for DNN distributed training. In BaPipe, each accelerator calculates the forward propagation and backward propagation of different parts of networks to implement the intra-batch pipeline parallelism strategy. BaPipe uses a new load balancing automatic exploration strategy that considers the parameters of DNN models and the computation, memory, and communication resources of accelerator clusters. We have trained different DNNs such as VGG-16, ResNet-50, and GNMT on GPU clusters and simulated the performance of different FPGA clusters. Compared with state-of-the-art data parallelism and pipeline parallelism frameworks, BaPipe provides up to 3.2x speedup and 4x memory reduction in various platforms.

Index Terms—DNN training, pipeline parallelism, load balancing, parallel and distributed systems

1. Introduction

In recent years, deep neural networks (DNNs) have made great progress in a variety of applications such as image classification [1]–[4] and natural language processing (NLP) [5]–[7]. As the effect of DNNs has been improved, the size of DNNs has become bigger and bigger, making DNNs more computationally intensive and memory intensive. The adoption of a single accelerator for DNN training will face the memory bottleneck and cost unaffordable training time. Therefore, DNN training usually deploys distributed computing systems which consist of multiple accelerators such as GPUs, FPGAs, and ASICs. GPU clusters have been used most for DNN training [9]–[12] as they are easy to implement and have high computing power. FPGA clusters have become a popular option due to the advantages of energy efficiency and flexibility [13]–[16]. ASIC clusters are developed by many companies [9], [17] for the most energy efficiency but the highest development cost at the same time. And heterogeneous clusters, such as clusters consisting of mixed models of GPUs, are commonly employed in realistic scenarios [18]–[22].

Nowadays most accelerator clusters for DNN training work in Data Parallelism [23], [24]. As shown in Fig. 1(a), each accelerator in distributed systems with Data Parallelism computes the whole layers of DNN with a different part of training data concurrently. In the meantime, all the weights and intermediate features of DNN must be stored locally by each accelerator in Data Parallel systems. Therefore, the capacity of higher bandwidth memory of accelerators maybe not enough for big DNN training which will consequently decrease the parallel performance. The higher bandwidth memory is compared with low bandwidth memory in distributed systems. For example, the bandwidth of on-chip memory is higher than off-chip memory in FPGA clusters. And graphic memory is higher bandwidth memory compared with host memory in GPU clusters. Distributed data parallel systems even cannot training larger DNN models when the memory consumption of deep learning is much larger than the memory capacity of accelerators. Thus, Model Parallelism has been used in DNN training. Large DNN models have been divided into partitions. Different accelerators execute different partitions, and store different parts of weights and intermediate features as shown in Fig. 1(b)(c). Hence, distributed systems with Model Parallelism can train larger models and increase training speed.

There are two types of Model Parallelism, which we called Tensor Slicing and Pipeline Parallelism. As shown in Fig. 1(b), Tensor Slicing splits each layer of the DNN model horizontally across accelerators, i.e. workers in Fig. 1 without pipeline. And there will be lots of All-Reduce operations among workers after every layer, which will lead to high communication overhead across workers. On the other hand, Pipeline Parallelism splits the DNN model vertically into different subsets of neural network layers, as shown in Fig. 1(c). And each worker computes different partition in the pipeline, which increases parallel efficiency. There are also two approaches of Pipeline Parallelism: inter-
batch and intra-batch pipeline parallelism. As shown in Fig. 2(b), the inter-batch parallelism sets one mini-batch of training data as a primitive element in the pipeline. Consequently, the weights used for backward propagation (BP) of DNN training are not the same version of weights in forward propagation (FP). Thus, it prolongs the convergent rate of a DNN model and even diverges the training of the model. In contrast, intra-batch parallelism, as shown in Fig. 2(a), divides a mini-batch into micro-batches for pipeline parallelism to achieve the high accuracy results in DNN training without inconsistent weights.

However, intra-batch pipeline parallelism still faces two major challenges. First, the computation for DNN training is consistent with forward propagation (FP) and backward propagation (BP). And BP should be executed after FP with the same micro-batch of intermediate features. Thus, there are various scheduling methods of the pipeline consisting of different FP and BP from different micro-batches. The different pipeline scheduling will generate varying memory requirements to store the different sizes of intermediate features, and affect parallel performance due to the different rate of pipeline bubbles. Second, the efficiency of pipeline parallelism is determined by the bottleneck of distributed training systems. That means the partition of DNN training should make the load across accelerators as balanced as possible. Communication between accelerators, including both intermediate feature maps in FP and errors in BP, and computation costs constitute the executing time of each accelerator. In addition, the overlap of communication and computation will also have a significant impact on parallel efficiency.

To solve the challenges described above, we propose BaPipe, a novel distributed DNN training framework with intra-batch Pipeline Parallelism. BaPipe can improve DNN training performance and reduce memory consumption by automatically exploring pipeline scheduling and load balanced partition strategies. The main contributions of this work are as follows:

- We present an automatic exploration method of the scheduling of pipeline parallelism which can select the most suitable scheduling method according to hardware resources of accelerator clusters and structure of DNNs.
- We propose a partitioning strategy suitable for a variety of DNNs. The DNN model is specified as consecutive layers to balance the computational load, communication cost, and memory consumption among accelerator clusters. And the partitioning strategy also applies to distributed systems in heterogeneous environments, where the clusters consist of mixed models of hardware, including GPU clusters and FPGA clusters.
- We evaluate BaPipe by training different DNN models such as VGG-16, ResNet-50, and GNMT on various GPU clusters and simulating the performance of both homogeneous and heterogeneous FPGA clusters. Compared with state-of-the-art data parallelism and pipeline parallelism frameworks, BaPipe provides 3.2x speedup and 4x memory reduction on various platforms.

The rest of this paper is organized as follows: Section II discusses background and related work. Section III presents the framework of BaPipe. BaPipe is evaluated in Section IV and Section V concludes this paper.

2. Background and Related Work

Many works focus on parallel DNN training in recent years which can be classified into Data Parallelism, Model Parallelism, and Hybrid Parallelism.
2.1. Data Parallelism

The whole DNN model weights are replicated on each accelerator and input data of mini-batches are partitioned evenly across accelerators in Data Parallelism, as shown in Fig. 1(a), thus each accelerator synchronizes updates weights after backward propagation. A popular data parallel DNN training method for large-scale distributed systems is the parameter server framework \([25], [26]\). To decrease communication costs between the parameter server and other accelerators, Ring All-Reduce options are used commonly nowadays \([12], [27]\). In this paper, we use synchronized All-Reduce Data Parallelism as a baseline.

2.2. Model Parallelism

In Model Parallelism, the DNN model is divided into partitions mapping to accelerators, thus clusters can be used in larger DNN training. There are also two ways for Model Parallelism: Tensor Slicing and Pipeline Parallelism, as shown in Fig. 1(b)(c), which respectively partition models horizontally and vertically. Mesh-Tensorflow \([28]\) and Megatron-LM \([29]\) both implemented large NLP models by Tensor Slicing. However, accelerators in Tensor Slicing have to communicate intermediate features after each layer which will degrade training efficiency a lot.

2.2.1. Pipeline Parallelism. Pipeline Parallelism can be divided into two paradigms according to the primitive element in the pipeline: inter-batch pipeline parallelism and intra-batch pipeline parallelism, as shown in Fig. 2(a)(b), which updates weights after each mini-batch asynchronously and synchronously, respectively. That means each accelerator in an intra-batch pipeline parallel cluster has the same fresh version of weights, at the same time, the weights of accelerators in inter-batch pipeline parallelism may be delayed or in different versions.

PipeDream \([8]\) is the most cited inter-batch pipeline parallelism technique in GPU clusters. The main contribution of PipeDream is weight stashing which keeps multiple versions of weights to solve the weight inconsistency problem of inter-batch pipeline parallelism. However, more memory requirements are generated by weight stashing thus larger DNN cannot train with PipeDream while the weight staleness issue still exists which impacts the convergence and accuracy of DNNs. PipeDream also presents a dynamic programming algorithm to balance computational load and communication costs across layers but ignore memory requirements. GPipe \([9]\) and FPDeep \([13], [14]\) are popular intra-batch pipeline parallelism approaches. GPipe split each mini-batch into micro-batches to increase pipeline training efficiency with GPUs or TPUs while backward propagation is computed after the whole forward propagation of each mini-batch being completed which leads to significant memory requirement for intermediate features of all micro-batches in one mini-batch. So GPipe sacrifices performance to reduce memory cost by recomputing forward propagation. Moreover, GPipe has not proposed a partitioning strategy to balance the load. FPDeep presents a fine-grained pipeline for FPGA clusters which partitions model intra-layer to implement high parallelism and utilization. Meanwhile, FPDeep proposes a novel workload and weight partitioning schemes but has not addressed the communication bottleneck.

2.3. Hybrid Parallelism

As model parallelism and data parallelism are orthogonal, there are various works used hybrid parallelism \([30]\), for example, FlexFlow \([31], [32]\) automatically optimizes parallelism across the sample, operation, attribute, and parameter dimension. Megatron-LM \([29]\) and PipeDream \([8]\) also use hybrid parallelism. However hybrid parallelism with automatic partition has much more requirements on the topology of clusters in which arbitrary accelerators may need to be
connected. Our design, BaPipe, is suitable for accelerator clusters in 1D daisy chain topology and orthogonal to data parallelism.

3. BaPipe Framework

3.1. Overview

In this section, we present BaPipe, a novel distributed DNN training framework with intra-batch pipeline parallelism. And BaPipe is adaptive to various hardware architectures, including GPU clusters and FPGA clusters in both homogeneous and heterogeneous environment. As shown in Fig. 3, the BaPipe framework has two sets of inputs: the DNN configurations and the hardware constraints. The hyper-parameters of DNN to describe network structures form the DNN configurations. The hardware constraints involve computing power, memory bandwidth, memory capacity, and communication bandwidth of each accelerator in the cluster.

There are mainly three parts in the BaPipe framework: DNN profile, automatic exploration of pipeline scheduling, and automatic exploration of balanced partition. BaPipe profiles the DNN first to get computing time for FP and BP, weights size, and features size of every layer in the network. For heterogeneous GPU clusters, BaPipe records the measurement through a short profiling run of 1000 mini-batches on each different type of GPU. For FPGA clusters, BaPipe simulates the DNN profile according to DNN configurations and hardware constraints include computing power and memory bandwidth of each different model of FPGA. And the simulation is based on the hardware accelerator architecture of FPDeep [13], [14], [16]. Then the results of profiling, the number of accelerators, and memory capacity and communication bandwidth of each accelerator are used as the input of both auto exploration methodologies. The partition algorithm partitions the network into several stages across accelerators to balance the computational load, communication cost, and memory consumption. Thus, according to hardware constraints and the results of DNN profiling and partitioning, the pipeline scheduling strategy automatically explores the most suitable sequence of the pipeline. Finally, BaPipe exports the results of pipeline scheduling and balanced partition to deploy the accelerator cluster for parallel DNN training.

3.2. Pipeline Scheduling

As shown in Fig. 4, there are two execution orders of accelerators for computation and communication: asynchronous execution and synchronous execution. In Fig. 4, mFn means computation time for FP of the m-th batch at accelerator n while mFS/mFR refers to the time to send/receive forward activations of m-th batch between 2 accelerators. GPUs have to compute and communicate synchronously which means the outputs of computation should be sent after the whole computation. Meanwhile, asynchronous execution can be used in FPGAs, thus communication can start after the part of outputs being done. So the overlap of communication and computation is different between the two execution methods.

3.2.1. Asynchronous Execution. BaPipe provides two options for automatic exploration of pipeline scheduling with asynchronous execution: 1F1B-AS and FBP-AS (Fig. 5). In Fig. 5, mFn/mBn denotes forward/backward propagation of m-th batch at accelerator n. Moreover, send and receive are omitted due to the complete overlap by asynchronous execution.

![Figure 3. Overview of BaPipe framework.](image)

![Figure 4. The timeline of a 2-accelerator cluster for DNN inference showing the order of computation and communication: (a) Asynchronous Execution; (b) Synchronous Execution.](image)
1F1B is first proposed by PipeDream \cite{8} which means each accelerator alternately executes forward and backward propagation for its stage in a steady pipeline state. BaPipe modifies it to 1F1B-AS for intra-batch pipeline parallelism with asynchronous scheduling which partitions each mini-batch in several micro-batches, such as 8 micro-batches in Fig. 5, and updates weights after backward propagation of each mini-batch to ensure the convergence of training and decrease memory requirement of weight stashing. FBP-AS is first used by FPDeep \cite{13} which means each accelerator executes forward and backward propagation in parallel with asynchronous scheduling in a steady pipeline state.

The comparison of theoretical performance between 1F1B-AS and FBP-AS is shown in TABLE 1 where \( M \) is the number of micro-batches in each mini-batch, \( N \) is the number of accelerators in the cluster, \( F/B \) is the computation time of FP/BP which are assumed the same in each stage by the balanced partition, \( i \) is the \( i \)-th accelerator across 1 to \( N \), and \( a/w \) is the size of activation/weights in each stage. As we can see, the training time and bubble overhead of each mini-batch, and memory requirements for weights and weights gradient of each stage are the same between 1F1B-AS and FBP-AS when the partition of DNN is the same too. Meanwhile, the activation memory requirement of FBP-AS is twice as much as 1F1B-AS, as the number of micro-batches for FP before the first BP of 1F1B-AS is half of FBP-AS. Besides, the demand bandwidth to overlap communication and computation of 1F1B-AS is more than FBP-AS, since \( a \) is the same that send/receive time is the same but the calculation to overlap is different between FP and parallel FP/BP.

3.2.2. Synchronous Execution. Different tasks such as FP and BP cannot be calculated in parallel by GPU with current machine learning frameworks such as PyTorch \cite{33}, TensorFlow \cite{34}, and Caffe \cite{35} due to their sequential instructions. Thus FBP cannot be used by GPUs while 1F1B-AS cannot be used either because of the synchronous execution of GPUs. As shown in Fig. 6(a), the naive 1F1B (called 1F1B-SNO in BaPipe) suffers non-overlapping of communication and computation because there are not enough warm-up micro-batches in the set-up pipeline state to completely receive the inputs of each mini-batch before the related computation in each accelerator. In Fig. 6(b), BS/BR denotes the time to send/receive outputs/inputs features in FP while FS/FR denotes the time to send/receive outputs/inputs error in BP. Also, we assume all input/output activation/error of each stage is the same so that the FS, FR, BS, and BR of each accelerator are all same.

![Figure 5. The timeline of a 3 accelerator cluster for DNN training showing the pipeline scheduling methodologies with asynchronous execution: (a) 1F1B-AS; (b) FBP-AS.](image)
TABLE 2. COMPARISON BETWEEN 1F1B-SNO AND 1F1B-SO

|                  | 1F1B-SNO                                                                 | 1F1B-SO                                                                 |
|------------------|---------------------------------------------------------------------------|---------------------------------------------------------------------------|
| Mini-batch time  | $(M + N - 1) \times (F + B) + $                                            | $(M + N - 1) \times (F + B) + $                                            |
|                  | $(N + M - 2 - \lceil \frac{M-1}{N} \rceil) \times 2 \times SR$            | $(M - 1) \times 2 \times SR$                                              |
|                  | $(N - 1) \times (F + B + 2 \times SR) + (M - 1 - \lceil \frac{M-1}{N} \rceil) \times 2 \times SR$ | $(N - 1) \times (F + B + 2 \times SR)$                                    |
|                  | $(M + N - 1) \times (F + B) + (N + M - 2 - \lceil \frac{M-1}{N} \rceil) \times 2 \times SR$ | $(M + N - 1) \times (F + B) + (N - 1) \times 2 \times SR$                |
| Features memory  | $(N - i + 1) \times a$                                                    | $2 \times a$                                                            |
| Weights memory   | $2 \times w$                                                              | $2 \times w$                                                            |
| Bandwidth        | $\alpha/F$                                                                | $\alpha/F$                                                              |

Thus we present 1F1B-SO to overlap the communication and computation of each stage for synchronous pipeline scheduling used in GPU cluster by double the warm-up micro-batches as shown in Fig. (b). TABLE 2 shows the comparison of theoretical performance between 1F1B-SNO and 1F1B-SO in which SR denotes the time for send/receive features/errors while other abbreviations are the same as TABLE 1. As we can see, the training time and bubble overhead of each mini-batch of 1F1B-SO are much better than 1F1B-SNO when the partition of DNN is the same. The extra bubble of 1F1B-SNO consists of non-overlapping communications that are proportional to M. However, the cost of higher performance is double the memory requirements for intermediate features which leads to a decrease of micro-batch size. Moreover, the throughput of training with small batch sizes may be lower when the utilization of GPU is not high enough. Thus the profile of DNN should consider batch size as a variation for GPU clusters by profiling run on each different GPU. After that, BaPipe also automatically explores the better synchronous pipeline scheduling methods for GPU clusters according to hardware constraints, DNN profile, and DNN partitions.

3.3. Balanced Partition

To balance the computational load, communication cost, and memory consumption of each accelerator, BaPipe automatically explores the DNN partitioning method by the inter-layer partition with intra-layer partition, coarse-grained partition based on communication bandwidth, and fine-tune partition based on memory capacity, respectively.

The partition algorithm first executes inter-layer partition, assuming that communication and computation are overlap. Second, BaPipe judges whether the communication is the bottleneck, that is, whether the communication time of each stage is longer than the computation time. And if so, BaPipe partitions layers in a coarse-grained manner to overlap communication. Then, BaPipe tunes layer partition if memory capacity is not enough until the bottleneck is resolved. Thus, we can skip the later steps and output the result of DNN partitions. In contrast, if the communication is not the bottleneck, BaPipe skip to the next step. Third, the intra-layer partition is used to make the workload more
balanced. Finally, BaPipe judges whether the memory capacity of each accelerator is enough for the requirements of each stage, and if not, finely tunes layer partition until memory requirements are satisfied and communication is not the bottleneck, thus the balanced partition strategy can be output.

3.3.1. Inter-layer partition. The input of inter-layer partition for pipeline parallelism is the number of accelerators and computing time for FP and BP of every layer in the network over each different type of accelerator from profiling results. And the inter-layer partition algorithm outputs the DNN partition strategy without considering communication and memory.

Let \( T_n \) denote the training time of one micro-batch for the whole network used in accelerator \( n \), \( l_n \) denotes the part of the network on stage \( n \) with the ideal partition so that \( L = \sum_{n=1}^{N} l_n \), where \( L \) is the number of layers in the network. If we assume that DNN is uniform across all layers, the ideal training time of each stage is \( T = \frac{L}{N} T_1 = \frac{L}{N} T_2 = \cdots = \frac{L}{N} T_N \), and can be solved as:

\[
T = \frac{1}{\sum_{n=1}^{N} \frac{1}{l_n}}
\]

Therefore, BaPipe partitions DNN according to \( T \) firstly, and then iterates to load balancing with inter-layer partition.

3.3.2. Intra-layer partition. The intra-layer partition for pipeline parallelism is first proposed by FPDeep [13]. However, FPDeep is used for FPGA clusters in which every FPGA is the same, while we present BaPipe for heterogeneous accelerator clusters (e.g. heterogeneous GPU clusters, heterogeneous FPGA clusters) in which each accelerator can be different. Thus the balanced workload cannot be divided by \( N \) directly. The input of intra-layer partition for pipeline parallelism is both the input and output of inter-layer partition. Moreover, the intra-layer partition will be employed only when the communication is not the bottleneck, because intra-layer partition will increase the communication time. BaPipe partitions DNN according inter-layer partition firstly and then iterates to load balancing with intra-layer partition by fine-tuning part of the boundary layer between accelerators.

3.3.3. Coarse-grained partition based on communication. When the send/receive time of intermediate activation/error across accelerators is longer than the computation time of each stage, the communication becomes the bottleneck for the pipeline. Since the bandwidth across accelerators is fixed, we can set the feature threshold \( \alpha_{th} \) for transmission when the communication time threshold is determined such as \( T \). Thus the DNN can be set to a coarse-grained network in which each layer is consists of consecutive layers in the original DNN between two adjacent layers that the size of their output features both are below \( \alpha_{th} \). Therefore, the balanced partition used in the coarse-grained network no longer suffers from a communication bottleneck.

4. Evaluation

In this section, we evaluate the efficiency of BaPipe with two kinds of DNNs on different accelerator clusters. First, we have trained several small models on GPU clusters to prove performance improvement. And we also evaluate the memory demand with giant models on GPU clusters. Besides, we have simulated the performance of BaPipe on FPGA clusters.

4.1. Experimental Setup

We use two representative types of DNN models in our experiments: convolutional model such as VGG-16 [4], ResNet-50 [1] and sequence-to-sequence model such as Google’s Neural Machine Translation(GNMT) [5] with different number of LSTM layers. The GPU cluster we used has 8 NVIDIA V100 GPUs, with 16GB of GPU device memory, and PCIe Gen3 x16 interconnections between GPUs. The FPGA clusters we used in the simulator have 4 Xilinx VCU118 boards and 4 Xilinx VCU129 boards as shown in TABLE 5.

4.2. Experimental Results on GPU clusters

4.2.1. Small DNN models experiments. TABLE 3 compares several DNN models training epoch time among DP, PipeDream [8], GPipe [9] and our work. We use the GLOO [36] communication backend for all parallel training as the NCCL does not currently support multi-threads communication in safety, and we set DP as a baseline for all parallel training. In TABLE 3 B means the amount of batch size per GPU, and to improve performance we set B as much as possible under the constraint of GPU memory. As we can see, the throughput of DNN training has reduced when B has decreased in DP and PipeDream. For GPipe and BaPipe, M means the number of micro-batches in each mini-batch, and we also set M large enough to ignore the pipeline bubble. But the number of micro-batches is still limited by the GPU memory for GPipe, as the accelerator in GPipe has to store all activation of a whole mini-batch. So GPipe selects to recompute forward propagation for memory reduction, and in our experiments, we didn’t use recomputation for fairness. Also, we use the same partitions as BaPipe in GPipe, since GPipe doesn’t have a load balancing algorithm, and PipeDream uses its strategy to partition training load.

As TABLE 3 shown, BaPipe has up to 3.2x faster than DP, 1.4x faster than state-of-the-art pipeline parallelism in DNN training. And except for VGG-16 on 8 V100, the pipeline scheduling of BaPipe automatically chose 1F1B-SNO, to overlap communication and computation for more performance improvement than the utilization reduction caused by mini-batch decreased in other situations. For ResNet-50, both BaPipe and PipeDream have explored that the best partition is DP on our GPU cluster, as the communication consumption for activation between GPUs in the pipeline is larger than the amount of communication for weights gradient among GPUs in DP.
### TABLE 3. COMPARISON OF EPOCH TIME AMONG DP, PipeDream, GPipe and BaPipe

| Model       | Cluster | Epoch time(Speedup over DP) |  |
|-------------|---------|-----------------------------|---|
|             |         | DP | PipeDream | GPipe | BaPipe |
| VGG-16 [4]  | 4 V100  | B=32 0.62x | 1.97x | M=8 B=32 1.95x | 1F1B-SO M=32 B=32 2.61x |
|             | 8 V100  | B=32 0.55x | 2.33x | M=8 B=32 1.77x | 1F1B-SNO M=64 B=64 2.97x |
| ResNet-50 [1] | 4 V100 | 1x | 1x | 1x | 1x |
|             | 8 V100  | 1x | 1x | 1x | 1x |
| GNMT-8 [5]  | 4 V100  | B=64 1x | 2.75x | M=8 B=64 2.93x | 1F1B-SO M=32 B=64 3.90x |
|             | 8 V100  | B=64 1x | 2.37x | M=12 B=64 2.05x | 1F1B-SO M=64 B=64 3.21x |

### TABLE 4. COMPARISON OF MAXIMUM (L, W) OF GNMT WITH OTHER PARALLELISM

| GPU Cluster(16GB each) | 1 V100 | 2 V100 | 4 V100 | 8 V100 |
|------------------------|--------|--------|--------|--------|
| DP                     | (32, 445.6M) | (32, 445.6M) | (32, 445.6M) | (32, 445.6M) |
| PipeDream              | (32, 445.6M) | (32, 445.6M) | (32, 445.6M) | (32, 445.6M) |
| GPipe                  | (32, 445.6M) | (42, 550.6M) | (60, 739.5M) | (74, 886.4M) |
| BaPipe                 | (32, 445.6M) | (74, 886.4M) | (118, 1.35B) | (158, 1.78B) |

### TABLE 5. FPGA PLATFORM PARAMETERS

| Platform  | Xilinx VCU118 | Xilinx VCU129 |
|-----------|---------------|---------------|
| DSP Slices | 6840          | 12288         |
| On-chip RAM(Mb) | 345.9        | 454.9        |
| GTY/GTM Transceivers | 120/0     | 32/48        |
| DDR4 Throughput(GB/s) | ~40        | ~40           |

### TABLE 6. COMPARISON BETWEEN BaPipe AND DP ON FPGA CLUSTERS

| ResNet-50 | 4 VCU118 | 2 VCU129, 2 VCU118 | 4 VCU129 |
|-----------|-----------|-------------------|----------|
| Batch time (Speedup over DP) | 1x | 1.05x | 1.14x |

4.2.2. Giant DNN models experiments. TABLE 4 compares the maximum model size which DP, PipeDream, GPipe, and BaPipe can support on different GPU clusters. We use the GNMT-L model to evaluate memory consumption. GNMT-L is based on GNMT [5] which consists of an LSTM model. Thus, we have stacked the GNMT-L by L/2 encoder and L/2 decoder layers, and W presents the number of parameters. We set the batch size per GPU is 32, and the number of micro-batches in each mini-batch for GPipe and BaPipe both are two times the number of pipeline stages. As mentioned in Section 4.2.1, the GPipe in our evaluation does not support recomputation. And BaPipe has used 1F1B-SNO to fit the biggest model size for DNN training on clusters.

As shown in TABLE 4, the model size is constrained by single GPU memory limits with DP and PipeDream because of weight stashing for convergence. On the other hand, GPipe and BaPipe both can scale DNN model size with the number of accelerators increased. BaPipe can train up to 4x larger models than DP and 2x larger models than state-of-the-art pipeline parallelism.

4.3. Experimental Results on FPGA clusters

TABLE 5 compares the simulation result of ResNet-50 training on different FPGA clusters between DP and BaPipe, and the parameters of FPGA boards are shown as TABLE 6. We set 1 as the micro-batch size for BaPipe and 128 as the mini-batch size for both BaPipe and DP. We use fp16 precision for memory optimizer, and guarantee weights of each stage are stored in on-chip memory as much as possible for BaPipe. At the same time, DP has to store weights in DDR due to the size limits, so there has speedup over DP compared with TABLE 3. However, the computation resources of FPGAs are not enough to take advantage of on-chip memory, thus, the speedup is only 1.14x. Also, BaPipe automatically chooses FBP-AS to increase accelerator utilization for clusters in the simulator.

5. Conclusion

This paper presents BaPipe, a pipeline parallelism training framework, which explores the design space of pipeline scheduling methods and balanced partition strategies for DNN training on accelerator clusters. Compared to state-of-the-art parallelism frameworks, BaPipe provides up to 3.2x speedup and 4x memory reduction in various platforms. Consequently, BaPipe can train small DNN models more efficiently and train far larger DNN models.

Acknowledgment

This research was sponsored by Huawei Innovation Research Program. The numerical calculations in this paper
have been done on the supercomputing system in the Supercomputing Center of University of Science and Technology of China. Supports from Chio-In IEONG are gratefully acknowledged.

References

[1] K. He, X. Zhang, S. Ren, and J. Sun, “Deep residual learning for image recognition,” in Proceedings of the IEEE conference on computer vision and pattern recognition, 2016, pp. 770–778.

[2] A. Krizhevsky, I. Sutskever, and G. E. Hinton, “Imagenet classification with deep convolutional neural networks,” Communications of the ACM, vol. 60, no. 6, pp. 84–90, 2017.

[3] K. He, X. Zhang, S. Ren, and J. Sun, “Identity mappings in deep residual networks,” in European conference on computer vision, Springer, 2016, pp. 630–645.

[4] K. Simonyan and A. Zisserman, “Very deep convolutional networks for large-scale image recognition,” arXiv preprint arXiv:1409.1556, 2014.

[5] Y. Wu, M. Schuster, Z. Chen, Q. V. Le, M. Norouzi, W. Macherey, M. Krikun, Y. Cao, Q. Gao, K. Macherey et al., “Google’s neural machine translation system: Bridging the gap between human and machine translation,” arXiv preprint arXiv:1609.08144, 2016.

[6] A. Vaswani, N. Shazeer, N. Parmar, J. Uszkoreit, L. Jones, A. N. Gomez, L. Kaiser, and I. Polosukhin, “Attention is all you need,” in Advances in neural information processing systems, 2017, pp. 5998–6008.

[7] J. Devlin, M.-W. Chang, K. Lee, and K. Toutanova, “Bert: Pre-training of deep bidirectional transformers for language understanding,” in Proceedings of the 2019 Conference of the North American Chapter of the Association for Computational Linguistics: Human Language Technologies: Volume 1 (Long and Short Papers), 2019, pp. 4171–4186.

[8] D. Narayanan, A. Harlap, A. Phanishayee, V. Seshadri, N. R. Devanur, G. R. Ganger, P. B. Gibbons, and M. Zaharia, “Pipedream: generalized pipeline parallelism for dnn training,” in Proceedings of the 27th ACM Symposium on Operating Systems Principles, 2019, pp. 1–15.

[9] Y. Huang, Y. Cheng, A. Bapna, O. Firat, D. Chen, M. Chen, H. Lee, J. Ngiam, Q. V. Le, Y. Wu et al., “Gpipe: Efficient training of giant neural networks using pipeline parallelism,” in Advances in neural information processing systems, 2019, pp. 103–112.

[10] S. Pal, E. Brejnh, A. Zulfiquar, Y. Fu, V. Zhang, S. Migacz, D. Nellans, and P. Gupta, “Optimizing multi-gpu parallelization strategies for deep learning training,” IEEE Micro, vol. 39, no. 5, pp. 91–101, 2019.

[11] S. Li, R. J. Walls, L. Xu, and T. Guo, “Speeding up deep learning with transient servers,” in 2019 IEEE International Conference on Autonomic Computing (ICAC), 2019, pp. 125–135.

[12] T. Capes, V. Raheja, M. Kemertas, and I. Mohomed, “Dynamic scheduling of mpi-based distributed deep learning training jobs,” 2019.

[13] T. Geng, T. Wang, A. Sanaullah, C. Yang, R. Xu, R. Patel, and M. Herbordt, “Fpdeep: Acceleration and load balancing of cnn training on fpga clusters,” in 2018 IEEE 26th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM). IEEE, 2018, pp. 81–84.

[14] T. Wang, T. Geng, A. Li, X. Jin, and M. Herbordt, “Fpdeep: Scalable acceleration of cnn training on deeply-pipelined fpga clusters,” IEEE Transactions on Computers, vol. 69, no. 8, pp. 1143–1158, 2020.

[15] S. Venkataramani, A. Ranjan, S. Banerjee, D. Das, S. Avancha, A. Jagannathan, A. Durg, D. Nagaraj, B. Kaul, P. Dubey et al., “Scaledep: A scalable compute architecture for learning and evaluating deep networks,” in Proceedings of the 44th Annual International Symposium on Computer Architecture, 2017, pp. 13–26.

[16] T. Geng, T. Wang, A. Sanaullah, C. Yang, R. Patel, and M. Herbordt, “A framework for acceleration of cnn training on deeply-pipelined fpga clusters with work and weight loading balancing,” in 2018 28th International Conference on Field Programmable Logic and Applications (FPL). IEEE, 2018, pp. 394–394.

[17] W. Fedus, B. Zoph, and N. Shazeer, “Switch transformers: Scaling to trillion parameter models with simple and efficient sparsity,” 2021.

[18] S. Li, R. J. Walls, and T. Guo, “Characterizing and modeling distributed training with transient cloud gpu servers,” 2020.

[19] D. Li, Z. Lai, K. Ge, Y. Zhang, Z. Zhang, Q. Wang, and H. Wang, “Hpdi: Towards a general framework for high-performance distributed deep learning,” in 2019 IEEE 39th International Conference on Distributed Computing Systems (ICDCS), 2019, pp. 1742–1753.

[20] X. Zhao, A. An, J. Liu, and B. X. Chen, “Dynamic stale synchronous parallel distributed training for deep learning,” in 2019 IEEE 39th International Conference on Distributed Computing Systems (ICDCS). IEEE, 2019, pp. 1507–1517.

[21] Q. Zhou, K. Wang, S. Guo, H. Lu, L. Li, M. Guo, and Y. Sun, “Falcon: Towards computation-parallel deep learning in heterogeneous parameter server,” in 2019 IEEE 39th International Conference on Distributed Computing Systems (ICDCS), 2019, pp. 196–206.

[22] W. Lee, Y. Lee, J. S. Jeong, G. Yu, J. Y. Kim, H. J. Park, B. Jeon, W. Song, G. Kim, M. Weimer, B. Cho, and B. Chun, “Automating system configuration of distributed machine learning,” in 2019 IEEE 39th International Conference on Distributed Computing Systems (ICDCS), 2019, pp. 2057–2067.

[23] T. Ben-Nun and T. Hoefler, “Demystifying parallel and distributed deep learning: An in-depth concurrency analysis,” ACM Computing Surveys (CSUR), vol. 52, no. 4, pp. 1–43, 2019.

[24] R. Mayer and H.-A. Jacobsen, “Scalable deep learning on distributed infrastructures: Challenges, techniques, and tools,” ACM Computing Surveys (CSUR), vol. 53, no. 1, pp. 1–37, 2020.

[25] C. Zhang, H. Tian, W. Wang, and F. Yan, “Stay fresh: Speculative synchronization for fast distributed machine learning,” in 2018 IEEE 56th International Conference on Distributed Computing Systems (ICDCS), 2018, pp. 99–109.

[26] S. Ahn, J. Kim, E. Lim, W. Choi, A. Mohaisen, and S. Kang, “Shmcaffe: A distributed deep learning platform with shared memory buffer for hpc architecture,” in 2018 IEEE 38th International Conference on Distributed Computing Systems (ICDCS), 2018, pp. 1118–1128.

[27] P. Goyal, P. Dollár, R. Girshick, P. Noordhuis, L. Wesolowski, A. Kyrola, A. Tulloch, Y. Jia, and K. He, “Accurate, large minibatch sgd: Training imagenet in 1 hour,” arXiv preprint arXiv:1706.02677, 2017.

[28] N. Shazeer, Y. Cheng, N. Parmar, D. Tran, A. Vaswani, P. Koanantakool, P. Hawkins, H. Lee, M. Hong, C. Young et al., “Mesh-tensorflow: Deep learning for supercomputers,” in Advances in Neural Information Processing Systems, 2018, pp. 10.414–10.423.

[29] M. Shoeybi, M. Patwary, R. Puri, P. LeGresley, J. Casper, and B. Catanzaro, “Megatron-lm: Training multi-billion parameter language models using gpu model parallelism,” arXiv preprint arXiv:1909.08053, 2019.

[30] J. Geng, D. Li, and S. Wang, “Horizontal or vertical? a hybrid approach to large-scale distributed machine learning,” in Proceedings of the 10th Workshop on Scientific Cloud Computing; 2019, pp. 1–4.

[31] Z. Jia, M. Zaharia, and A. Aiken, “Beyond data and model parallelism for deep neural networks,” SYSL 2019, 2019.

[32] Z. Jia, S. Lin, C. R. Qi, and A. Aiken, “Exploring hidden dimensions in parallelizing convolutional neural networks,” arXiv preprint arXiv:1802.04924, 2018.

[33] A. Paszke, S. Gross, F. Massa, A. Lerer, J. Bradbury, G. Chanan, T. Killeen, Z. Lin, N. Gimelshein, L. Antiga et al., “Pytorch: An imperative style, high-performance deep learning library,” in Advances in neural information processing systems, 2019, pp. 8026–8037.
[34] M. Abadi, P. Barham, J. Chen, Z. Chen, A. Davis, J. Dean, M. Devin, S. Ghemawat, G. Irving, M. Isard et al., “Tensorflow: A system for large-scale machine learning,” in 12th {USENIX} symposium on operating systems design and implementation ({OSDI} 16), 2016, pp. 265–283.

[35] Y. Jia, E. Shelhamer, J. Donahue, S. Karayev, J. Long, R. Girshick, S. Guadarrama, and T. Darrell, “Caffe: Convolutional architecture for fast feature embedding,” in Proceedings of the 22nd ACM international conference on Multimedia, 2014, pp. 675–678.

[36] “Gloo,” https://github.com/facebookincubator/gloo, 2020.