Epitaxial Growth of Si and SiGe Using High-Order Silanes without a Carrier Gas at Low Temperatures via UHVCVD and LPCVD

Dae-Seop Byeon, Choonghee Cho, Dongmin Yoon, Yongjoon Choi, Kiseok Lee, Seunghyun Baik and Dae-Hong Ko *

Abstract: Conventional Si or SiGe epitaxy via chemical vapor deposition is performed at high temperatures with a large amount of hydrogen gas using silane (SiH₄) or dichlorosilane (SiCl₂H₂) precursors. These conventional precursors show low growth rates at low temperatures, particularly below 500 °C although a low thermal budget becomes more important for modern fabrication techniques. High-order silane precursors, such as disilane, trisilane, and tetrasilane, are candidates for low-temperature epitaxy due to the lower strength of the Si-Si bonds compared to that of the Si-H bonds. In addition, the consumption of vast amounts of hydrogen gas is an additional burden of the low-temperature process due to its low throughput. In this study, we explored Si and SiGe epitaxial growth behaviors using several high-order silanes under ultra-high vacuum chemical vapor deposition (UHVCVD) and low-pressure chemical vapor deposition (LPCVD) conditions without a carrier gas. Disilane showed high-quality epi-growth under both pressure conditions, whereas trisilane and tetrasilane showed enhanced growth rates and lower quality.

Keywords: Si epitaxy; SiGe epitaxy; high-order silane; ultra-high vacuum chemical vapor deposition (UHVCVD); low-pressure chemical vapor deposition (LPCVD)

1. Introduction

Si and SiGe epitaxy can be performed using various techniques such as molecular beam epitaxy, low-pressure chemical vapor deposition (LPCVD), reduced-pressure chemical vapor deposition (RPCVD), and ultra-high vacuum chemical vapor deposition (UHVCVD). Currently, RPCVD is the most popular technique for Si and SiGe epitaxy; however, it requires a large amount of H₂ gas as the carrier gas. On the other hand, the epitaxial growth via UHVCVD is performed without a carrier gas, but the growth rate is limited, particularly at low temperatures, because the pressure is too low. High-order silanes are candidate Si precursors for low-temperature Si epitaxy due to the lower strength of the Si-Si bonds compared to the Si-H bonds. Previous studies have been conducted on high-order silane-based Si or SiGe epitaxy utilizing disilane [1,2], trisilane [3–6], tetrasilane [7,8], or neopentasilane [9,10]. However, these studies have focused on one or two high-order silanes compared to conventional precursors (silane; SiH₄ or dichlorosilane; SiCl₂H₂), and most were performed in RPCVD or LPCVD chambers with an abundance of ambient H₂ or N₂. Silane-based low-temperature CVD may also be applicable to the coating of sensing devices. For example, alkylsilane-based self-assembled monolayers (SAMs) deposited on metal oxides were suggested to replace expensive gold electrodes [11]. Gabriunaite et al. demonstrated a transparent electrode system of octadecyltrichlorosilane-based SAM on fluorine-doped tin oxide (FTO) for biosensors [12]; FTO can also be formed by using CVD techniques [13]. In this study, we performed Si and SiGe epitaxy under UHVCVD (working
pressure <0.1 mTorr) and LPCVD (working pressure 80 mTorr) conditions without a carrier gas. Various temperatures ranging from 400 to 650 °C were investigated using disilane, trisilane, and tetrasilane.

2. Experimental Procedure

First, we performed Si and SiGe epitaxy at 450 to 650 °C under UHVCVD conditions (<0.1 mTorr) on blanket Si (100) coupon wafers using a UHVCVD chamber (EURECA 3000, Jusung Engineering, Gwangju-si, Gyeonggi-do, Korea). The base pressure was maintained at a 5 × 10^{-8} torr using a turbo-molecular pump (TMP) (Leybold, Köln, Germany). Graphite heaters were used to control the temperature. The working pressure was not identified precisely in these experiments due to the absence of a pressure controller, and the cold cathode gauge was automatically isolated during the process. However, the working pressure did not exceed 0.1 mTorr, which was the lower limit of the convectron gauge. All samples were dipped in dilute HF (1:100) for 1 min to remove the native oxides. Then, they were rinsed with deionized water prior to loading. Subsequently, the samples were loaded into the CVD chamber within 3 min to inhibit native oxide regrowth. In situ plasma cleaning was performed before the epitaxial growth process. SF₆ and Cl₂ gases were then used with Ar plasma for 60 s each. High-order silane and germane precursors were supplied during this process without a carrier gas. Trisilane and tetrasilane are liquid precursors at room temperature unlike disilane. However, their vapor pressures are sufficiently high for the use of a conventional gas delivery system with a heated gas line, even though the flow rate is limited to either tens of standard cubic centimeters per minute (sccm; for trisilane) or a few sccm (for tetrasilane). A similar delivery system was demonstrated by Hazbun [7]. In the case of Si epitaxy, the deposition of the SiGe marker layer was preceded by Si epitaxial growth. This was used to easily determine the resulting thickness.

Si epitaxy was also carried out at a higher pressure of approximately 100 mTorr and temperatures below 500 °C. The sample preparation and in situ cleaning methods were the same as those mentioned above unless otherwise stated. After in situ plasma cleaning, TMP was turned down for 10 min and the epitaxial growth process was conducted. No carrier gas was used during this process.

The epilayers were evaluated using various analysis techniques. The thicknesses of the epilayers were measured using transmission electron microscopy (TEM) (JEOL, Tokyo, Japan). The Ge concentrations were extracted using high-resolution x-ray diffraction (HR-XRD) (Rigaku, Tokyo, Japan) and the results were confirmed by energy-dispersive X-ray spectroscopy (EDS) (JEOL, Tokyo, Japan) and spectroscopic ellipsometry (SE) (J.A. Woollam, Lincoln, NE, USA). We note that the Ge concentration calculated via XRD is incorrect when strain relaxation occurs. Therefore, the crystal quality was confirmed upon the evaluation of the Ge concentration using HR-XRD. The crystal quality was analyzed via TEM, and the surface roughness was measured using atomic force microscopy (AFM) (Park Systems, Suwon, Korea).

3. Results and Discussion

Disilane- and trisilane-based Si epitaxy were carried out at 500 to 650 °C under UHVCVD conditions below 0.1 mTorr. Tetrasilane was excluded due to the limitation of its low flow rate. SiGe marker layers of approximately 5 nm were inserted between the Si epilayers and the substrates because the epilayers may be indistinguishable from the substrate. The Si growth rate can be increased, particularly in thin films, if the Ge concentration of the marker layer is adequately high. This phenomenon occurs because surface Ge atoms can act as hydrogen desorption centers due to the lower strength of the Ge–H bond compared to that of the Si–H bond [14]. Therefore, the Ge concentration of the SiGe marker should be sufficiently low and should be targeted at 10%. The growth rates of these epitaxial layers were similar regardless of the existence of the marker layer, as shown in Supplementary Materials Figure S1. The difference in the growth rate was less than 3%. There were no evident defects such as stacking faults at the interface between the
SiGe marker layer and the Si epilayer or substrate as shown in Supplementary Materials Figure S2. Therefore, all Si epitaxy experiments were performed using SiGe marker layers for ease of evaluation.

The flow rates of the Si precursors (disilane and trisilane) were fixed at 20 sccm. The growth time was 1000 s at $\geq 550 \, ^\circ\text{C}$ and 4000 s below $550 \, ^\circ\text{C}$. Figures 1 and 2 show the cross-sectional TEM images of the Si epilayers grown using disilane and trisilane, respectively. All epilayers were successfully grown epitaxially, and no defects such as stacking faults or contamination were found. The activation energies extracted from these experiments at low temperatures (reaction rate limited regime) are 2.1 eV, which is well consistent with the values reported by Hartmann et al. [2] and Chung et al. [9]. The growth rate in this study was the lowest because the partial pressure of the silane precursor was the lowest. Trisilane-based Si epitaxy also showed similar growth kinetics. Solid symbols and lines in Figure 3 show the above-described UHVCVD results.

![Cross-sectional TEM images](image_url)

**Figure 1.** Cross-sectional TEM images of the Si layers grown using disilane at 550–650 °C with a SiGe marker layer. High-resolution TEM images of the interface are also shown.
Figure 2. Cross-sectional TEM images of the Si layers grown using trisilane at 500–650 °C with a SiGe marker layer. High-resolution TEM images of the interface are also shown.

Figure 3. Arrhenius plot of high-order, silane-based Si epitaxy under UHVCVD and LPCVD conditions. The solid symbols and lines represent UHVCVD conditions, while the open symbols and dotted lines represent LPCVD conditions. The black squares, red circles, and blue triangles represent disilane, trisilane, and tetrasilane, respectively.
The high-order silane-based Si epitaxy at temperatures below 500 °C was also examined under LPCVD conditions. The Arrhenius plot of the Si epitaxial growth is shown in Figure 3. The closed and open symbols represent the Si epilayers grown under UHVCVD and LPCVD conditions, respectively. Surprisingly, the growth rates of disilane for the two process conditions are the same. Conversely, the growth rate of trisilane under LPCVD conditions was three times higher than that under UHVCVD conditions. The same growth rate of disilane being achieved in both conditions indicates the saturation of the surface reactions with increasing gas flow. The increased growth rate of trisilane is assumed to originate from gas-phase reactions. Figure 4 shows the AFM measurements and the root mean square (RMS) surface roughness (Rq) of the Si epilayers grown using disilane and trisilane under UHVCVD conditions at 550 and 600 °C. No particles were found in either case, while the RMS surface roughness of the trisilane samples was higher than that of the disilane samples due to the high growth rate. However, the Si epilayer grown using trisilane at a low pressure demonstrated island formation phenomena, whereas no such phenomena were found for disilane or when using UHVCVD conditions, as shown in Figure 5.

![AFM measurements and RMS surface roughness (Rq) values of the Si epilayers grown under UHVCVD conditions at 550 and 600 °C using disilane (DS) and trisilane (TS). The red lines represent the results of the line scans and their positions. All line scans were performed at the same position.](image)

In the case of silane or dichlorosilane, it is well known that the epitaxial growth behaviors can be simply divided into two regimes: the mass flow limited regime at high temperatures and the reaction rate limited regime at low temperatures. On the other hand, high-order silanes have complicated behaviors depending on the temperature; there are intermediate regions, called plateaus, between the mass flow limited regime and the reaction limited regime [2,4]. The growth rate in the intermediate region is relatively independent of the temperature or even increases slightly despite decreasing temperature.
This region appears clearly in RPCVD, particularly in H\textsubscript{2} ambient conditions, whereas does not appear in UHVCVD as shown in Figure 3 (solid line), also reported by Adam et al. [1]. Hartmann suggested an alternative reaction pathway at the intermediate region, such as Si\textsubscript{2}H\textsubscript{6}(g) + 2SiH(a) → 2SiH\textsubscript{4}(g) + 2Si(s) [2], and Gouyé suggested similar reactions of trisilane [4]. However, the intermediate region did not appear in our disilane experiments and appeared very slightly in trisilane and tetrasilane under LPCVD conditions, although the partial pressure of high-order silane of approximately 80 mTorr is similar to the RPCVD studies. This result indicates that the carrier gas plays an important role in the enhancement of growth rates at low temperatures.

![Figure 5](image_url)

**Figure 5.** Si epilayers grown at 500 °C using disilane and trisilane under LPCVD and UHVCVD conditions. Islands appear only in trisilane under the LPCVD condition.

Next, disilane- and trisilane-based SiGe epitaxy processes were carried out at 550–650 °C under UHVCVD conditions below 0.1 mTorr. The flow rate of disilane was fixed at 20 sccm, that of trisilane was 5 sccm, and the flow rate of germane varied from 5 to 30 sccm. The growth time was 500 s for all splits. All SiGe epilayers were grown epitaxially, but relaxation occurred in some of the samples because the thickness exceeded the critical thickness. Ge concentrations were measured by HR-XRD, EDS, and SE, as shown in Table S1. HR-XRD curves are presented in Figure S3. The results are well-matched except for disilane at 550 °C. The HR-XRD results were used because EDS measures only significantly small regions while HR-XRD is more reproducible than SE. However, when relaxation was observed in TEM images, the Ge concentrations extracted by the HR-XRD curves were considerably smaller than those of EDS and SE. Thus, the Ge concentrations of the highest GeH\textsubscript{4} flow rate at 600 °C were obtained from EDS. Hereafter, the Ge concentration mentioned was obtained from HR-XRD, unless otherwise stated. We note that the Ge concentrations of the SiGe epilayers grown using trisilane are comparable to those grown using disilane even though the flow rate of trisilane is four times lower than that of disilane. This indicates that the Si incorporation of trisilane is four times more effective than that of disilane even though the growth rate of Si epitaxy using trisilane was only two times higher than that of disilane.

The growth rate and Ge concentration versus the Ge flow rate are shown in Figure 6. The growth rate was proportional to the germane flow rate due to the weaker strength of the Ge–H bond compared to the Si–H bond. When silane is used for SiGe epitaxy at temperatures below 650 °C, the growth rate is highest at a Ge concentration of approximately 10% [15]. The monotonic increase in the growth rate at a low Ge content is due to the weak
strength of the Ge-H bond, as mentioned above. Conversely, the monotonic decrease of the growth rate at high Ge content, particularly at high temperatures, is due to the decrease in the sticking coefficient of silane with increasing Ge content [15]. However, disilane and trisilane demonstrated a linearly increasing growth rate until the Ge content reached 22% (disilane) or 25% (trisilane) because the sticking coefficient of high-order silane is higher than that of silane. Therefore, high-order silane has the advantage of having a higher growth rate of SiGe epilayers than silane at the same Ge content. The Ge concentration of the SiGe epilayers grown by disilane did not change with increasing temperature, whereas that of trisilane grown at 600 °C was slightly higher than that obtained at 550 °C, as shown in Figure 6. Gouyé et al. reported the same trend for trisilane in terms of the Ge content in SiGe epitaxy [4]. However, silane exhibits the opposite characteristics, with the Ge concentration decreasing with increasing temperature [16]. This phenomenon occurs because the sticking coefficient varies depending on the temperature. Buss et al. reported that the sticking coefficient of disilane is less dependent on the temperature than that of silane [17]. They fitted the reactive sticking coefficient to the Arrhenius plot for these substances, and the activation energies of silane and disilane at temperatures below 800 °C were calculated to be 55–60 and 35 kJ/mol, respectively. Therefore, the higher-order silane showed a lower dependence of the Ge content on the process temperature.

![Figure 6](image_url)

**Figure 6.** Growth rate and Ge concentration versus the Ge flow rate of the SiGe epilayers grown using disilane and trisilane at 550 and 600 °C. The flow rates of disilane and trisilane were 20 and 5 sccm, respectively.

The RMS surface roughness values of the SiGe epilayers grown by disilane and trisilane at 550 °C were 0.105 and 0.104 nm, respectively, as shown in Figure 7. These values are below the limitations of the AFM measurements. Conversely, the RMS surface roughness values of the SiGe epilayers grown at 600 °C were 0.386 and 0.736 nm as shown in Figure 7. These values are slightly higher than those obtained at 550 °C because of the higher obtained growth rate. Similar to Si epitaxy, the surface roughness values of the SiGe
epilayers grown under UHVCVD conditions were only affected by the growth rate and not by the precursor species.

![AFM measurements and RMS surface roughness (Rq) values of the SiGe epilayers grown under UHVCVD conditions at 550 and 600 °C using disilane (DS) and trisilane (TS). The flow rates of disilane, trisilane, and germane are 20, 5, and 30 sccm, respectively. The red lines represent the results of the line scans and their positions. All line scans were performed at the same position.](image)

SiGe epitaxial growth at 450 °C under UHVCVD conditions was attempted using trisilane; however, epitaxial growth did not occur. Subsequently, high-order silane-based SiGe epitaxy at temperatures below 500 °C was examined under LPCVD conditions. First, various high-order silane and germane ratios were examined. The lack of adequate surface diffusion length is critical for epitaxial growth at low temperatures. If the Ge concentration of a SiGe layer is low, the surface diffusion of an adatom is more difficult to achieve because of the high hydrogen coverage and high strength of the Si-Si and Si-H bonds. Therefore, tetrasilane was first tested because the lowest Ge concentration was expected to be obtained using this compound. Figure 8 shows the SiGe epilayers grown using tetrasilane at 450 °C. The tetrasilane and germane ratios were 2:1, 1:1, and 1:2. High-quality SiGe layers were obtained at the ratio of 1:2. Consequently, disilane and trisilane were also utilized at the
1:2 ratio. Ge concentrations of the 2:1 ratio samples were lower than those of the other samples; however, most SiGe epilayers grown at 450 °C were too thin to determine the Ge concentration precisely, as shown in Figure S4. Figure 9 shows the Ge flow rate plotted versus the Ge concentration of the SiGe epilayers grown at 500 °C as the Si precursors. The order of silane was increased while the Ge concentration of the SiGe epilayer was lowered, as expected. The Arrhenius plot for the SiGe epilayers as the Si precursors grown at 410–500 °C is shown in Figure 10. Trisilane showed the highest growth rate while disilane demonstrated the lowest; however, these rates should not be directly compared due to the different Ge contents. The activation energy was 1.5 eV at 410–450 °C regardless of either the precursor species or the Ge content in the SiGe layer. This is consistent with the values previously reported by Hart et al. for tetrasilane and digermane [8]. The surface morphology of epitaxial SiGe grown at 500 °C was reported in our previous study [18]. Similar to Si epitaxy, good morphology was obtained when disilane was used, whereas particle formation was observed when trisilane or tetrasilane was used.

![Cross-sectional TEM images of the SiGe epilayers grown using tetrasilane at 450 °C. The tetrasilane and germane ratios were 2:1, 1:1, and 1:2.](image1)

**Figure 8.** Cross-sectional TEM images of the SiGe epilayers grown using tetrasilane at 450 °C. The tetrasilane and germane ratios were 2:1, 1:1, and 1:2.

![Graph showing Ge concentration of the SiGe epilayers as a proportion of the Ge flow rate.](image2)

**Figure 9.** Ge concentration of the SiGe epilayers as a proportion of the Ge flow rate.
4. Conclusions

We demonstrated fairly good Si epitaxial growth without a carrier gas at low temperatures. This hydrogen-free process can be cost-effective, but the crystal quality should be controlled carefully. The Si epitaxial growth characteristics achieved using disilane under both conditions resulted in high crystal quality and the same growth rate despite the large difference in the pressure. Trisilane demonstrated growth rates that were two and six times higher than that of disilane under UHVCVD and LPCVD conditions, respectively. High-quality Si epilayers were grown using trisilane under UHVCVD conditions, whereas their surface roughness was higher than that achieved using disilane due to the high growth rate of this compound. However, particle formation was observed under LPCVD conditions. Particles are generally regarded as a result of gas-phase reactions; therefore, the increase in the growth rate at temperatures below 500 °C likely originated from gas-phase reactions. Tetrasilane shows similar characteristics to trisilane. These results indicate that disilane is highly advantageous for quality control, and trisilane and tetrasilane are advantageous for obtaining a higher growth rate. SiGe epitaxial growth was also carried out under UHVCVD and LPCVD conditions without a carrier gas. SiGe epitaxial growth was achieved at the lowest temperature of 410 °C under LPCVD conditions but failed under UHVCVD conditions at the same temperature. Disilane shows better quality, higher Ge content, and less growth rate of the epitaxial layers whereas trisilane and tetrasilane show particle formation, less Ge content, and higher growth rate. The Ge content decreased with increasing order of the silane precursor. The activation energy was the same regardless of the Si precursor used.

Supplementary Materials: The following are available online at https://www.mdpi.com/article/10.3390/coatings11050568/s1, Figure S1: Cross-sectional TEM images of the Si layers grown using disilane at 600 °C with and without an SiGe marker layer. The difference in the growth rate is less than 3%, Figure S2: High-resolution TEM images of the Si epilayers and SiGe marker layers grown by disilane, Figure S3: HR-XRD curves of SiGe epilayers grown by disilane and trisilane at 550–600 °C, Figure S4: HR-XRD curves of SiGe epilayers grown by tetrasilane and germane at 450 °C. The flow rate of tetrasilane are 2 sccm and those of germane were 1, 2, and 4 sccm. The SiGe epilayer of the lowest germane flow rate shows the lowest Ge concentration of 14.1%; however, the others are too thin to confirm the Ge concentration correctly, Table S1: Ge concentration of SiGe epilayers grown at 550–600 °C, measured by HR-XRD, SE, and EDS.

Author Contributions: Funding acquisition, D.-H.K.; Investigation, D.-S.B., C.C., D.Y., Y.C., K.L., and S.B.; Supervision, D.-H.K.; Writing—original draft, D.-S.B. All authors have read and agreed to the published version of the manuscript.
**Funding:** This work was supported by the Technology Innovation Program (20010598) funded by the Ministry of Trade, Industry & Energy (MOTIE), and the Future Semiconductor Device Technology Development Program (20004274) funded by MOTIE and Korea Semiconductor Research Consortium (KSRC).

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** All the original data generated in this research are available.

**Acknowledgments:** The authors thank SK Materials for providing the high-order silane precursors.

**Conflicts of Interest:** The authors declare no conflict of interest.

**References**

1. Adam, T.N.; Bedell, S.; Reznicek, A.; Sadana, D.K.; Venkateshan, A.; Tsunoda, T.; Seino, T.; Nakatsuru, J.; Shinde, S.R. Low-temperature growth of epitaxial silicon on silane and disilane in a 300 mm UHV/CVD cold-wall reactor. *J. Cryst. Growth* 2010, 312, 3473–3478. [CrossRef]

2. Hartmann, J.M.; Benevent, V.; Damencourt, J.F.; Billon, T. A benchmarking of silane, disilane and dichlorosilane for the low temperature growth of group IV layers. *Thin Solid Films* 2012, 520, 3185–3189. [CrossRef]

3. Fischer, P.R.; Bauer, M.; Van Aerde, S.R.A.; Oosterlaken, T.G.M.; Yan, M.; Verweij, W.A.; Bozon, B.W.M.; Zagwijn, P.M. Low temperature Silcore® deposition of undoped and doped silicon films. *ECS Trans.* 2006, 3, 203. [CrossRef]

4. Gouyé, A.; Kermarrec, O.; Halimouaï, A.; Campidieli, Y.; Rouchon, D.; Burdin, M.; Holliger, P.; Bensahel, D. Low-temperature RPCVD of Si, SiGe alloy, and Si1–yCy films on Si substrates using trisilane (Silcore®). *J. Cryst. Growth* 2009, 311, 3522–3527. [CrossRef]

5. Vincent, B.; Loo, R.; Vandervorst, W.; Brammertz, G.; Caymax, M. Low temperature Si homo-epitaxy by reduced pressure chemical vapor deposition using dichlorosilane, silane, and trisilane. *J. Cryst. Growth* 2010, 312, 2671–2676. [CrossRef]

6. Shinriki, M.; Chung, K.; Hasaka, S.; Brabant, P.; He, H.; Adam, T.N.; Sadana, D. Gas phase particle formation and elimination on Si (100) in low temperature reduced pressure chemical vapor deposition silicon-based epitaxial layers. *Thin Solid Films* 2012, 520, 3190–3194. [CrossRef]

7. Hazbun, R.; Hart, J.; Hickey, R.; Ghosh, A.; Fernando, N.; Zollner, S.; Adam, T.N.; Kolodzey, J. Silicon epitaxy using tetrasilane at low temperatures in ultra-high vacuum chemical vapor deposition. *J. Cryst. Growth* 2016, 444, 21–27. [CrossRef]

8. Hart, J.; Hazbun, R.; Eldridge, D.; Hickey, R.; Fernando, N.; Adam, T.N.; Zollner, S.; Kolodzey, J. Tetrasilane and digermane for the ultra-high vacuum chemical vapor deposition of SiGe alloys. *Thin Solid Films* 2016, 604, 23–27. [CrossRef]

9. Chung, K.H.; Yao, N.; Benziger, J.; Sturm, J.C.; Singh, K.K.; Carlson, D.; Kuppurao, S. Ultrahigh growth rate of epitaxial silicon by chemical vapor deposition at low temperature with neopentasilane. *Appl. Phys. Lett.* 2008, 92, 113506. [CrossRef]

10. Sturm, J.C.; Chung, K.H. Chemical vapor deposition epitaxy of silicon-based materials using Neopentasilane. *ECS Trans.* 2008, 16, 799. [CrossRef]

11. Garbiunaite, I.; Valiūniénė, A.; Valincius, G. Formation and properties of phospholipid bilayers on fluorine doped tin oxide electrodes. *Electrochim. Acta* 2018, 283, 1351–1358. [CrossRef]

12. Garbiunaite, I.; Valiūniénė, A.; Poderyte, M.; Ramanavicius, A. Silane-based self-assembled monolayer deposited on fluorine doped tin oxide as model system for pharmaceutical and biomedical analysis. *J. Pharm. Biomed. Anal.* 2020, 177, 112832. [CrossRef] [PubMed]

13. Yang, J.K.; Liang, B.; Zhao, M.J.; Gao, Y.; Zhang, F.C.; Zhao, H.L. Reference of temperature and time during tempering process for non-stoichiometric FTO films. *Sci. Rep.* 2015, 5, 15001. [CrossRef] [PubMed]

14. Garone, P.M.; Sturm, J.C.; Schwartz, P.V.; Schwarz, S.A.; Wilkens, B.J. Silicon vapor phase epitaxial growth catalysis by the presence of germane. *Appl. Phys. Lett.* 1990, 56, 1275. [CrossRef]

15. Greve, D.W. Growth of epitaxial germanium-silicon heterostructures by chemical vapour deposition. *Mater. Sci. Eng.* 1993, B18, 22–51. [CrossRef]

16. Tillack, B.; Murota, J. *Silicon-Germanium (SiGe) Nanostructures*; Shiraki, Y., Usami, N., Eds.; Woodhead Publishing: Sawston, UK, 2011; Chapter 6; p. 117.

17. Buss, R.J.; Ho, P.; Breiland, W.G.; Coltrin, M.E. Reactive sticking coefficients for silane and disilane on polycrystalline silicon. *J. Appl. Phys.* 1988, 63, 2808. [CrossRef]

18. Byeon, D.-S.; Choi, Y.; Cho, C.; Yoon, D.; Lee, K.; Baik, S.; Ko, D.-H. Comparison of high-order silanes and island formation phenomena during SiGe epitaxy at 500 °C. *J. Korean Phys. Soc.* 2021, 78, 712–718. [CrossRef]