HiKonv: High Throughput Quantized Convolution With Novel Bit-wise Management and Computation

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Abstract— Quantization for Convolutional Neural Network (CNN) has shown significant progress with the intention of reducing the cost of computation and storage with low-bitwidth data inputs. There are, however, no systematic studies on how an existing full-bitwidth processing unit, such as CPUs and DSPs, can be better utilized to carry out significantly higher computation throughput for convolution under various quantized bitwidths. In this study, we propose HiKonv, a unified solution that maximizes the compute throughput of a given underlying processing unit to process low-bitwidth quantized data inputs through novel bit-wise parallel computation. We establish theoretical performance bounds using a full-bitwidth multiplier for highly parallelized low-bitwidth convolution, and demonstrate new breakthroughs for high-performance computing in this critical domain. For example, a single 32-bit processing unit can deliver 128 binarized convolution operations (multiplications and additions) under one CPU instruction, and a single 27×18 DSP core can deliver eight convolution operations with 4-bit inputs in one cycle. We demonstrate the effectiveness of HiKonv on CPU and FPGA for both convolutional layers or a complete DNN model. For a convolutional layer quantized to 4-bit, HiKonv achieves a 3.17× latency improvement over the baseline implementation using C++ on CPU. Compared to the DAC-SDC 2020 champion model for FPGA, HiKonv achieves a 2.37× throughput improvement and 2.61× DSP efficiency improvement, respectively.

I. INTRODUCTION

Quantization is a frequently used technique in hardware implementation of Deep Neural Network (DNN) models in order to reduce both the memory consumption and execution time [1]–[6]. It is typically done by approximating high-precision floating point numbers to low-bitwidth integers or fixed-point numbers. This is particularly important for modern DNN models as many of them employ convolutional layers, which contain intensive multiplication and accumulation (MAC) operations [5]–[8]. Therefore, many novel quantization methods have been proposed in the literature to reduce the precision of weights, activations, and even gradients for DNNs while retaining their high accuracy [2], [3], [6], [9].

The current hardware implementation of quantized DNNs is, however, not ideal as there is no general support for quantized MACs without changing the underlying hardware [10]–[15]. Most hardware units have a high-bitwidth (such as 32 or 64 bits) MAC for either floating point numbers or integers [16]. When they are used for quantized MACs, most of the bitwidths are left underutilized, wasting precious computing resources. Even with the 8-bit multi-data processing of the Advanced Vector Extensions (AVX) support in X86_64 architecture, processing a single 4-bit multiplication would still occupy the 8-bit data width with the remaining 4 bits simply wasted [17]. The waste becomes even more severe when either processing lower bitwidth (such as binary) data or utilizing a hardware unit with higher built-in bitwidths.

Reconfigurable hardware such as FPGA may alleviate some of the waste because of its bit-level flexibility for configuration, but it exhibits similar drawbacks, especially for FPGAs with high-precision Digital Signal Processing (DSP) units [8], [16], [18]. Without a careful bit-wise management of inputs and outputs, deploying quantized DNNs onto FPGAs with the given DSPs would still waste much of their computation capacity.

In this paper, we propose a novel solution, HiKonv, that can significantly improve the existing arithmetic units’ utilization efficiency when conducting quantized convolution, thus improving throughput for convolution and reducing end-to-end DNN computation latency. Our solution is based on a careful management of bitwidths used for quantized MACs and novel mapping of multiple parallelized MACs onto an existing arithmetic unit, such that the arithmetic unit’s computation capacity is fully utilized. We further show theoretically that such a management and mapping strategy is universal in the sense that it can be applied to arbitrarily quantized bitwidths and high-bitwidth arithmetic units. For example, a single 32-bit processing unit can deliver 128 binarized convolution operations using one instruction for CPU, and a single 27×18 DSP core can deliver eight convolution operations with 4-bit inputs in one cycle. Based on such a theoretical analysis, we show that there are different optimal design points in choosing the quantization bitwidth for a given arithmetic processing unit. Our experimental results further validate our analysis and HiKonv’s general applicability. For example, our CPU-based implementation of HiKonv achieves up to 3.17× latency improvement for quantized convolution over existing methods on the same CPU. We also apply HiKonv to an end-to-end quantized DNN model, UltraNet [19], in an FPGA setting, and the measured on-board result outperforms the state-of-the-art in terms of throughput and DSP efficiency by 2.37× and 2.61×, respectively.

Because of its generality, we believe HiKonv opens up a new venue for further improving the hardware efficiency of

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DNN based inferences. It not only improves the throughput and latency for existing quantized DNN models on existing hardware, but also offers new opportunities for designing new hardware-friendly quantized DNN models or co-designing both the hardware and quantized DNN models.

II. PRELIMINARY

Before we present our proposed HiKonv solution, we first review 1) input slicing and data packing for concurrency improvement and 2) 1-D convolution.

A. Input-Slicing for Concurrency Improvement

Input slicing and data packing are generally used by the current hardware units to process low-bitwidth inputs [17], [20], [21]. The input bitwidth is split into different pieces, each of which is called a slice to hold a low-bitwidth data. It uses the available bitwidth space to hold a number of data slices to improve the parallelism while still preserving the correct output. An example of INT4 optimization for Xilinx DSP48E2 unit is shown in Figure 1 each of the input contains two slices. It takes advantage of the multiple input ports and the internal addition operation of the DSP to enable four multiplications of data slices simultaneously. Since an INT4 × UINT4 multiplication generates a result that needs at least an 8-bit space, guard bits are added during the packing of the low-bitwidth data to guarantee the correctness of the result. Here, we define the term guard bit as the filling 1s or 0s between the packed data in the multiplicant for the purpose of preventing convolution overflow. The multiplication with the sliced and packed inputs is represented as:

\[(A_2 \cdot 2^{11} + A_1) \cdot (W_2 \cdot 2^{22} + W_1)\]  
\[= A_2W_2 \cdot 2^{33} + A_1W_2 \cdot 2^{22} + A_2W_1 \cdot 2^{11} + A_1W_1\]  

Equation (1)

The output of Equation (1) is the concatenation of four multiplication results with zeros between them due to the guard bits. This process accomplishes four multiplications within one operation cycle.

B. 1-D Convolution

The conventional 1-D discrete convolution between an \(N\)-element sequence \(f\) and a \(K\)-element kernel \(g\) (denoted as \(F_{N,K}(f,g)\)) can be represented as Equation 3. Here, we define the infinite length sequence \(h\) as the zero extension of \(f\) with the index range of \((-\infty, \infty)\). Meanwhile, \(y\) is the output with \(N+K-1\) non-zero elements.

\[h[n] = \begin{cases} 
  f[n], & 0 \leq n < N \\
  0, & n < 0 \text{ or } n \geq N
\end{cases}\]  

Equation (2)

\[y[m] = (h * g)[m] = \sum_{k=0}^{K-1} h[m-k]g[k]\]  

Equation (3)

Alternatively, \(y\) can be represented as an \((N+K-1)\)-element sequence with Equation 4. Each of the \(y[n]\) elements involves a sequence of multiplication and addition operations.

\[y[m] = \sum_{k=0}^{K-1} h[n]g[k]\]  

Equation (4)

III. MULTIPLIER FOR CONVOLUTION

Inspired by input slicing and data packing for novel bit management and high processing concurrency, we generalize the solution for using a given hardware unit to process the maximum amount of low-bitwidth convolution operations concurrently with theoretical guarantees.

We first define the variables related to our exploration. As shown in Figure 2, we assume a given high-precision hardware unit that can multiply \(Bit_A\)-bit integer input \(A\) with \(Bit_B\)-bit integer input \(B\) and generate the product Prod. The bitwidths of \(A\) and \(B\) define the computation capability of the hardware unit, or more specifically, the multiplier, and thus determine the design setting of HiKonv specific to this unit. Convolution input \(f\) and kernel \(g\) are the two sequences of low-bitwidth integer values quantized to \(p\) and \(q\) bits, respectively.

To determine how to load \(A\) and \(B\) with multiple convolution operands from \(f\) and \(g\) and perform the convolution between these operands, we define an additional variable \(S\) to be the size of a slice of inputs for both \(A\) and \(B\) as demonstrated on the left in Figure 2. The lower bits of each slice contain one operand from \(f\) or \(g\). To simplify the problem, we assume the \(N\) and \(K\) are the maximum numbers of operands from \(f\) and \(g\) that can fit into \(A\) and \(B\), respectively. Hence, the polynomial representations of \(A\) and \(B\) are:

\[A = \sum_{n=0}^{N-1} f[n] \cdot 2^{S \cdot n}, \quad B = \sum_{k=0}^{K-1} g[k] \cdot 2^{S \cdot k}\]  

Equation (5)

Although the intermediate results of the multiplication are invisible to us, we assume the processing unit takes the most ideal way for the multiplication of two inputs, as shown in Figure 2. The entire multiplication is treated as the multiplication of slices in \(A\) with the corresponding slices in \(B\) followed by shifting the product left by \(S\) bits and accumulating the shifted results to the previous result. There are always \(N \times K\) products between elements from \(f\) and \(g\) that are computed and accumulated to form the output Prod.

A. From Multiplication To Convolution

To use the product Prod = \(A \times B\), we need to segment the output into an effective format for convolution during the process. In order to segment the intermediate results, we extend the guard bits \(G_b\) in [20]. The guard bits are not only to prevent overlaps between the effective product of two adjacent intermediate partial products but also to segment out the partial accumulations of vertically stacked segments. Its length varies according to the maximum number of multiplication terms \(f[n]g[k]\) that are summed together. According to our settings for \(A\) and \(B\), a maximum of \(\min(K, N)\) terms are summed together for each output segments. Therefore, to ensure the correctness of the final result, each of the slicing should contain both the guard bits and the bits of the \(p\)-bit and \(q\)-bit inputs for the production, respectively.
Theorem 1. Assuming guard bits, $G_s$, are properly decided according to the specific multiplier setting, with given $A$ and $B$ constructed from $N$-element sequence $f$ and $K$-element sequence $g$, where $f$ and $g$ are quantized respectively to $p$ and $q$ bits, we can obtain $N + K - 1$ segments from the product $Prod = A \times B$ which are all short partial convolutions in the form of 1-D convolution.

Proof. Considering the guard bits, we can obtain:

$$S = \begin{cases} 
q + G_s, & p = 1, q \geq 1 \\
p + G_s, & q = 1, p \geq 1 \\
p + q + G_s, & \text{otherwise} 
\end{cases}$$

(6)

$$p + (N - 1)S \leq \text{Bit}_A$$

(7)

$$q + (K - 1)S \leq \text{Bit}_B$$

(8)

Thereby, the intermediate stages are shifted left by $S$ bits for every stage, and the effective vertical accumulation of the partial products in the segments from all the stages stacked together would not exceed the length of $S$ bits, as shown in Figure 2. Then, the multiplication is represented as:

$$Prod = A \times B = \left( \sum_{n=0}^{N-1} f[n] \cdot 2^{Sn} \right) \left( \sum_{k=0}^{K-1} g[k] \cdot 2^{Sk} \right)$$

$$= \sum_{m=0}^{N-K-2} \left( \sum_{n+k=m} f[n] \cdot 2^{Sn} \cdot g[k] \cdot 2^{Sk} \right)$$

(9)

$$= \sum_{m=0}^{N-K-2} \left( \sum_{n+k=m} f[n] \cdot g[k] \cdot 2^{Sm} \right)$$

Different from general multiplications, convolution consists of a sequence of multiplications and accumulations. Referring to the form of 1-D convolution in Equation 4, the result of $Prod$ can be represented as:

$$Prod = \sum_{m=0}^{N+K-2} y[m] \cdot 2^{Sm}$$

(10)

where the intermediate accumulations form a 1-D convolution of two sequences in each of the output segments, and the total number of convolution segments is $N + K - 1$.

Per the above, we can use a high-bitwidth multiplier to process two integers $A$ and $B$ to form $N + K - 1$ convolutions of short sequences. However, due to the two’s complement representation of signed values, directly packing negative values into $A$ or $B$ leads to wrong results for the intermediate products. To guarantee the correctness of the products as the intermediate results, we must consider the sign bit during the packing of the elements from $f$ and $g$ into $A$ and $B$ as well as segmenting the result $Prod$.

If $f$ and $g$ are all unsigned integers, we can construct $A$ and $B$ as integers with bit-wise assignments and the zero extension without additional operations:

$$A[S(n+1)-1:Sn] = f[n]$$

$$B[S(k+1)-1:Sk] = g[k]$$

(11)

Meanwhile, each $y[m]$ can be segmented out from $Prod$ with:

$$y[m] = Prod[S(m+1)-1:Sm]$$

(12)

However, if $f$ and $g$ contain signed integers, we need additional bit management.

$$A = 2^{2f[3]} + 2^{2f[2]} + 2^{f[1]} + f[0]$$

$$A[25:1-5] = f[1]+f[0]=f[1]$$

$$f[0]<0$$

$$A[25:1-5] = 0$$

$$A[25-1:5] = f[1]-\text{MSB}[0] = f[1]-1$$

Figure 3 shows the packing of four elements of $f$ into multiplicand $A$. Taking the second $S$-bit segment as an instance, in 2’s complement expression, if $f[0]$ is positive, the MSB is 0, and the sign extension part are all zeros. On the other hand, if $f[0]$ is negative, the sign extension part are all 1s in binary expression and represents -1 in 2’s complementary representation. In such condition, we decrement 1 from $f[1]$ to form the second $S$-bit and perform the packing process with concatenation and 1-bit incremener instead of using a larger bitwidth adder. The packing process works recursively for all the slices while slicing of the output works in a reversed manner. Equation 13 shows the packing and slicing formula for signed integer $f$ and $g$. With this bit management technique, we obtain $N + K - 1$ partial convolutions from $N \times K$ segments of intermediate results for a single multiplier to process signed input data.

$$A[S(n+1)-1:Sn] = \begin{cases} 
  f[0], & n = 0 \\
  f[n]-A[Sn-1], & n > 0 
\end{cases}$$

$$B[S(k+1)-1:Sk] = \begin{cases} 
  g[0], & k = 0 \\
  g[k]-B[Sk-1], & k > 0 
\end{cases}$$

(13)

$$y[m] = \begin{cases} 
  Prod[S-1:0], & m = 0 \\
  Prod[S(m+1)-1:Sm]+Prod[Sm-1], & m > 0 
\end{cases}$$
B. Convolution Extension

Now we have presented an efficient algorithm to use the multiplication unit on a hardware platform to perform the \( F_{N,K} \) 1-D convolution. However, the size of \( N \) are limited by the bitwidth of the hardware multiplier whereas most real-world applications have much larger input sizes. Moreover, the \( F_{N,K} \) 1-D convolution is often used as a unit building block for other larger-scale convolution operations. Thus, we design a new algorithm to use the \( F_{N,K} \) 1-D convolution to complete arbitrarily large size 1-D convolutions and any arbitrary convolutions. As shown in Figure 2, the order of the elements for these intermediate production is controlled by the order of elements packed into the slices in \( A \) and \( B \); it allows us to devise different accumulation methods to provide flexibility to construct different convolutions beyond 1-D convolution.

a) 1-D Convolution Extension: Regarding the \( F_{N,K} \) as a basic operation, we extend it to \( F_{X \cdot N,K} \) convolution of a longer sequence by summing up the elements in output sequences of different \( F_{N,K} \) convolutions.

**Theorem 2.** The output sequence \( y = X \cdot N \) of a 1-D convolution between an \((X \cdot N)\)-element sequence \( f \) and a \( K \)-element filter \( g \) can be represented as the sum of index-shifted output sequences \( y_x = F_{N,K}(f_x, g) \), as shown in Equation (16). Here, \( f_x = f[xN:(x+1)N-1] \) (\( x \in [0, X - 1] \)).

**Proof.** Following Equation 16, we extend \( f \) and \( g \) sequences into zero extension sequences \( h \) and \( h_x \). Then \( h \) is represented as the sum of the shift indices \( h \) itself:

\[
h[n] = \sum_{x=0}^{X-1} h_x[n-xN]
\]

According to Equation 5, the convolution output \( y \) is calculated with:

\[
y[n] = \sum_{k=0}^{K-1} h[n-k]g[k]
\]

\[
y[n] = \sum_{k=0}^{K-1} \sum_{x=0}^{X-1} h_x[n-xN-k]g[k]
\]

\[
y[n] = \sum_{k=0}^{X-1} \sum_{x=0}^{K-1} h_x[n-xN-k]g[k]
\]

Equation 16 reveals that the extended \( F_{X \cdot N,K} \) 1-D convolution is computed by a shift-accumulation pattern with \( F_{N,K} \) base operation results. Figure 4 demonstrates how the elements in different \( y_x \) sum up to the elements in \( y \). Each computed \( y_x \) sequence is shifted \( Z \) indices and then summed up to form the element of \( y \), which is marked by the red square. Still, we use existing adder unit of the given platform to complete multiple additions by adding the bit slices from the product \( Prod \) as mentioned in Section III-A as marked by the blue square. In such a case, the guard bit of \( G_b = \lceil \log_2 K \rceil \) is also adjusted with additional bits to prevent the partial results from overflow.

**Figure 4: Computation of \( F_{X \cdot N,K} \) 1-D convolution**

b) DNN Convolution: The convolution layer in DNN computes a feature-map array \( I[C_0][H_0][W_0] \) and a kernel array \( W[C_0][C_1][K] \) for output feature-map array \( O[C_0][H_1][W_1] \) (assuming \( H_1 = H_0 + K - 1 \) and \( W_1 = W_0 + K - 1 \)) which can be represented as:

\[
O[c_0][h][w] = \sum_{c_o=0}^{C_o-1} \sum_{h_o=0}^{K-1} \sum_{k=0}^{K-1} I[c_0][h+k_h][w+k_w] W[c_o][c_1][h_o][k_w]
\]

With the inherent convolution computation pattern, we may also compute a DNN convolution layer with \( F_{N,K} \) 1-D convolution as the base operation, as shown in Theorem 3.

**Theorem 3.** For a DNN convolution, the output feature-map can be computed by \( F_{X \cdot N,K} \) 1-D convolution with the following equation:

\[
O[c_o][h][w] = \sum_{c_i=0}^{C_i-1} \sum_{h_i=0}^{K-1} \sum_{k=0}^{K-1} y[c_i,c_o,h,k] [w+K-1]
\]

Where the term \( y[c_i,c_o,h,k] \) is a 1-D convolution result with \( X = \lceil \frac{W_i}{N} \rceil - 1 \):

\[
y[c_i,c_o,h,k] = F_{X \cdot N,K}(f, g)
\]

**Proof.** For abbreviation, we denote sequence \( y[c_i,c_o,h,k] \) as \( y' \). According to the definition of 1-D convolution, sequence \( y' \) can be computed by following equation:

\[
y'[n] = \sum_{k=0}^{K-1} f[n-k] g[k]
\]

\[
y'[n] = \sum_{k=0}^{K-1-i} I[c_i][h+k_h][n-k] W[c_o][c_1][h_o][k-1-k]
\]

\[
y'[n] = \sum_{k=0}^{K-1} I[c_i][h+k_h][n+k-K+1] W[c_o][c_1][h_o][k]
\]

Then we have

\[
y[c_i,c_o,h,k][n+K-1] = \sum_{k=0}^{K-1} I[c_i][h+k_h][n+k] W[c_o][c_1][h_o][k]
\]

With Equation 22, Equation 17 could be represented as:
A convolution layer in DNN has multiple input and output channels, which require accumulation of channel-wise features to form the final output. By grouping the \( F_{N,K} \) output sequences with different \( c_i \) but same \( c_o, h, k_h, x \) and indices, and accumulating the corresponding product \( Prod \) with adders, we can perform the channel-wise accumulation of the feature maps. In this case, the required number of guard bits is \( G_b = \lfloor \log_2(M \cdot \min(K, N)) \rfloor \) for the accumulation of \( M \) feature maps along input channel in a convolution.

### C. Throughput Analysis

Based on the above discussions, the equivalent achievable throughput for convolution of inputs with \( p \) and \( q \) bits quantized by a given processing unit is a function of both the supported bitwidth of \( A \) and \( B \) by the hardware and the given bitwidth of the elements in \( f \) and \( g \). It can be represented by the number of multiplication and accumulation operations (\( \# \) ops) that one multiplier can perform for the low-bitwidth data in every cycle, which is \( N \times K + (N - 1) \times (K - 1) \).

Figure 5 shows two examples of multipliers with different bitwidth configurations. For a given high bitwidth processing unit, the maximum supported throughput (multiplication and addition) of a given processing unit varies with \( N \) and \( K \) which are determined by the values of \( p \) and \( q \). For instance, when the input bitwidths of the two inputs of a multiplier are 27 and 18 bits (Figure 5a), according to Equation (5) and (8) and the required guard bits, we could obtain \( S = 4, N = 9, K = 4 \) when the \( p \) and \( q \) are both 1-bit binary values. The maximum supported throughput of this specific multiplier is equivalent to 60 ops per cycle, which are 36 multiplications and 24 additions that are required operations for computing the convolution if all the computation is carried out in a conventional way following the 1-D convolution algorithm without HiKonv. Here, with HiKonv, all we need is one multiplication of high bitwidth multiplier with our specific slicing/packing solution. In addition, when the \( p \) and \( q \) are both 4 bits, the multiplier provides 8 equivalent ops per cycle (6 multiplication and 2 addition). In Figure 5a, we show the configurations for \( p \) and \( q \) from 1-bit to 8-bit, which are the common bitwidths of low-precision quantization. The principle generally applies to all bitwidths. When the inputs for the multiplier are both 32 bits, these values are further increased to 128 ops per cycle and 13 ops per cycle for 1-bit and 4-bit \( p \) and \( q \), as shown in the Figure 5b.

### IV. Evaluations

HiKonv is a general technique that can be adopted for both the general purpose processor and reconfigurable hardware platform. We demonstrate its efficacy on both platforms.

#### A. General Purpose Processors

We first evaluate HiKonv on both CPU-based desktop and mobile platforms with an Intel Core i7-10700K CPU and i7-10710U CPU, respectively. We measure the performance of both 1-D convolution and a DNN convolution layer.

For 1-D convolution, the baseline implementation has 2-level nested loops. The outer loop scans through the input vector, whereas the inner loop scans through the kernel vector. We adopt the horizontal stacking strategy proposed by HiKonv 1-D convolution. The features are packed during runtime, and kernels are packed offline before the processing starts. For the output, we first shift the previous partial result to the right by \( S \times 2 \) bits and the current partial result to the left by \( S \times (N - 2) \) bits. Then, we add them together to form the whole result for this loop. In the end, we take the last \( S \times N \) bits as the \( N \) outputs with the corresponding indices.

For a quantified analysis with a DNN layer, we pick the final layer of UltraNet [19], which is the champion model for the DAC-SDC contest 2020 and randomly generate feature and kernel vectors. We implement the DNN layer by embedding the 1-D convolution algorithm into the 6-level nested loops that scan through the input channel, output channel, output height, output width, kernel height, and kernel width according to Theorem 3. Since CPU hardware lacks bit-wise management capability, dealing with signed values can cause unnecessary overhead from intricate bit operations. While we can deploy the HiKonv solution with signed values, the hardware constraint makes such optimization less efficient than unsigned values. Since modern CPUs are equipped with 32-bit multipliers, without loss of generality, we use \( A = B = 32 \) bits as the multiplication bitwidth, and pack \( p = q = 4 \)-bit unsigned values in each of the operands. According to Theorem 2 we obtain \( N = 3, K = 3, G_b = 2 \), and \( S = 10 \) bits. Figures 6a and 6b show the 1-D and 2-D convolution latency results, respectively. Both are compared to the baseline implementation with nested loops without our HiKonv solution.

It is clear that our HiKonv solution is about three times faster than the baseline implementations under all four com-
 combinates. The experimental results are slightly slower than
the theoretical speed-up shown in Section III because of the
processing overhead. Despite the reduction in loop counts and
thus the total number of multiplications to generate all outputs,
HiKonv has additional bit-shifting and gating operations to
prepare the operands and segment the output. Since the
ALU handles both multiplications and bit-wise operations,
the latency of bit-wise operations are not much faster than
the DSP48E2 has one 27-bit, one 18-bit and one 45-bit input
port. It can perform one MAC in one clock cycle, where
M × M + Acc are the inputs at the 27-bit, 18-bit, and 45-bit port, respectively. Different from software implementation of HiKonv for general-purpose processors, with reconfigurable hardware, the input packing is conducted with small adders for each of the slices, and output segmentation is conducted by bit-wise operations. These advantages on the hardware can fully benefit the performance of our HiKonv solution.

B. Reconfigurable Hardware

We also conduct the evaluation of our HiKonv solution on
the Xilinx Ultra96 MPSoC platform, which is equipped with
360 DSP48E2 units and a quad-core ARM processor. Each of the DSP48E2 has one 27-bit, one 18-bit and one 45-bit input port. It can perform one (M × M + Acc) MAC operation in one clock cycle, where M, M, Acc are the inputs at the 27-bit, 18-bit, and 45-bit port, respectively. Different from software implementation of HiKonv for general-purpose processors, with reconfigurable hardware, the input packing is conducted with small adders for each of the slices, and output segmentation is conducted by bit-wise operations. These advantages on the hardware can fully benefit the performance of our HiKonv solution.

a) Binary convolution layer: We first evaluate the extreme case of quantized convolution which is the Binary Neural Networks (BNN). A convolutional layer in a BNN takes the binary inputs for both feature maps and kernel weights, processes the convolution between them, and generates the outputs. Note that the outputs may not be binary due to the channel-wise accumulation. We first implement a binary convolution layer with 4-bit outputs without using the DSP resources, denoted as BNN-LUT; we then replace the binary computations with our HiKonv solution with DSP, denoted as BNN-HiKonv. In comparison, we evaluate the resource utilization of these two designs under the setting of the same concurrency and same clock frequency, as shown in Table I.

Table I: Comparison of Resource util. of binary convolution

| # of Concurrent MACs | BNN-LUT | BNN-HiKonv |
|----------------------|---------|------------|
| LUT                  | 3371    | 3537       |
| DSP                  | 2672    | 3608       |
| LUT/DSP              | 21/18   | 15/12      |
| LUT/DSP              | 43.7    | 67.6       |

Clearly, compared to BNN-LUT, the LUT usage of BNN-
HiKonv is reduced. However, the throughput for each DSP reduces when the concurrency increases due to the reason that there is more vertical stacking, and it takes more guard bits when the concurrency increases. The equivalent number of LUTs replaced by one DSP (LUT/DSP) varies from 43.7 to 76.6 due to the accumulation logic in the convolution operation. HiKonv creates opportunities to leverage DSPs for high-throughput BNN (or other low-bitwidth models) convolution computations that would help map a larger BNN with high concurrency into the same FPGA. It can also potentially increase the design’s clock frequency since DSPs can run at a higher frequency than LUTs.

b) Complete model: We apply our HiKonv solution to the entire UltraNet model [19] on the Xilinx Ultra96 MPSoC FPGA. The weight and activation of this model are quantized to 4-bit. We execute all the convolution layers on the reconfigurable logic and the other layers on the ARM processor in the FPGA platform. We follow the same layer architecture and system architecture as the original UltraNet design and only change the computation for convolution with our HiKonv solution. Besides using DSPs, we also use small adders and shifters constructed by LUTs, taking advantage of the flexible configuration features of the FPGA.

In addition to resources utilization, we also measure the throughput in frame-per-second (fps) and calculate the DSP efficiency in terms of Giga-operations-per-second-per-DSP (Gops/DSP) for comparison as shown in Table II.

Table II: UltraNet resource and performance

|                      | UltraNet | UltraNet-HiKonv |
|----------------------|----------|-----------------|
| LUT                  | 360      | 327             |
| DSP                  | 248      | 401/588         |
| LUT/DSP              | 0.289    | 0.514/0.753     |

UltraNet-HiKonv uses more LUT resources than the original implementation due to the shifting and adding logic; however, it reduces the DSP utilization thanks to the dramatic improvements of the efficiency and the throughput of the DSPs. The original implementation of the UltraNet uses one DSP for two 4-bit MACs that is natively supported by the synthesis tool. It only achieves 248 fps with a 0.289 Gops/DSP efficiency. With our HiKonv solution, the on-board implementation of UltraNet achieves 401 fps with a 0.514 Gops/DSP DSP efficiency. This significant improvement is achieved under the constraint that the software execution on the ARM core is not fast enough to feed the input data to the FPGA accelerator to process, even with our best software optimization of multi-threading and data buffering. If this ARM core bottleneck is removed, the UltraNet-HiKonv
accelerator can reach an even higher performance of 588 fps with the DSP efficiency of 0.753 Gops/DSP.

V. RELATED WORKS

Existing solutions for low-bitwidth arithmetic [22] build their own computation units based on the inputs [10]–[15] and benefit from the control flexibility down to a single bit. Prior work for accelerating DNN inference has also incorporated low-bitwidth computations. Tensor processing units (TPUs) introduce 16-bit bfloats [23], and mobile GPUs and other edge devices now support 8-bit computations. However, these improvements focus only on homogeneous arithmetic requirements and do not allow flexible arithmetic computations with varied bitwidths. Therefore, when processing data with a bitwidth different from its targeted bitwidth, it either leaves some precision unused with wasted resources or hurts the efficiency of the overall process.

There are methods that simply pack short bitwidth values into longer words and attempt to incorporate additional computations using the existing unit through bit shifting and packing [17], [20], [24]–[26] to further improve processing efficiency. However, these studies are ad-hoc and do not fully leverage the hardware’s capability as HiKonv does. Moreover, there are no theoretical studies to guide the flexible management of low-bitwidth quantized data. Our work fills the gap of processing low-bitwidth data under theoretical guidance for the best computation efficiency and throughput on either existing hardware architecture or any bit-efficient processing units in the future.

VI. CONCLUSION AND DISCUSSION

In this paper, we present HiKonv, a general technique with theoretical guarantees for using a single multiplier unit to process multiple low-bitwidth convolution operations in parallel for significantly higher computation throughput with flexible bitwidths. It is able to support convolutions in DNNs and achieves the highest possible throughput for quantized convolution with novel bit-wise management and computation. As a demonstration of its general applicability and benefits, we show that HiKonv has achieved 3.17× throughput improvement on CPU and 2.37× and 2.61× throughput and DSP efficiency improvements for the DAC-SDC 2020 champion model on FPGA. HiKonv suits for both software and hardware optimizations and provides new opportunities for future hardware designs for efficient DNN processing.

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