Quad-Level Cell Switching with Excellent Reliability in TiN/AlOx:Ti/TaOx/TiN Memory Device

Hee Ju Shin 1,2,†, Hyun Kyu Seo 1,†, Su Yeon Lee 1, Minsoo Park 1, Seong-Geon Park 2 and Min Kyu Yang 1,*

Abstract: TiN/AlOx:Ti/TaOx/TiN memory devices using bilayer resistive switching memory demonstrated excellent durability and capability of QLC (quad-level cell) memory devices. The best nonvolatile memory characteristics with the lowest operation current and optimized 4 bit/cell states were obtained using the Incremental Step Pulse Programming (ISPP) algorithm in array. As a result, a superior QLC reliability (cycle endurance > 1 k at each level of the QLC, data retention > 2 h at 125 °C) for all the 4 bits/cell operations was achieved in sub-µm scaled RRAM (resistive random access memory) devices.

Keywords: ReRAM; resistive switching; ISPP; QLC

1. Introduction

The paradigm shift from a planar to vertical 3D structure of modern electronic devices is not a choice anymore. In the nonvolatile memory field, a 3D stackable crossbar-type ReRAM (resistive switching random access memory) device has been considered as the next-generation stand-alone memory device due to its simple structure, wide range of operational currents and fast write/erase speed. However, manufacturing high-density crossbar resistive memory cannot be realized simply by stacking multi floors or the scaling of device technology because the technology enablement unavoidably results in a rapid increase in the cost of device fabrication [1]. In this context, its main advantage over flash is that it is both more durable and requires far less energy per write. At present, long-term NAND flash scaling faces a number of problems, such as a flash built on smaller process nodes being less durable. An extension from MLC (multi-level cell) to TLC (triple level cell) has only been acceptable to a few limited applications due to the drastically reduced number of write cycles that a TLC flash can perform [2–4]. The QLC (quad levelcell) is still questionable. In theory, a resistance switching memory could solve a number of these problems. In this research, highly reliable ReRAM cells with QLC characteristics were fabricated using a bilayer structure for cross-point memory applications. Reproducible QLC behavior was successfully observed and elucidated by an oxygen ion migration model. Moreover, a new programming algorithm was developed for a more reliable and uniform QLC operation [5–9]. Recently, in-memory processing applications have attracted attention as cutting-edge chip technology that not only stores data in memory, but can also perform data operations. Accordingly, there is high interest in the resistive switching (RS) of various metal oxide materials for use in the implementation of in-memory computing utilizing next-generation, nonvolatile memory [10–24]. In this situation, as the amount of user data grows exponentially, low-energy operation is essential. To this end, new devices must meet high operating speeds, low operating voltages and high reliability.
As a candidate to meet these requirements, RS random access memory (RRAM) shows excellent performance in terms of speed and reliability [25,26]. However, many RRAM studies conducted so far have been conducted in the high-current region (over 10 µA), making them unsuitable for future demanding electronic device applications [27–29]. The reason is that the reliability of the RRAM resistance state becomes difficult to achieve as the operating current decreases [30–33]. Approaches are being undertaken to overcome the reliability issue by adopting several types of electrodes or by changing the stacked structure [34,35], but there are still difficulties. In this study, we used Ti-doped alumina (Ti: Al$_2$O$_3$, TAO) and TaO$_x$ as the RS and oxygen reservoir, respectively. Our device showed 4-bit characteristics and stable retention characteristics (125 °C, 2 h) at a low operating current (<1 µA). Ti doped into the RS layer played a central role in the generation of oxygen vacancies, resulting in excellent and gradual RS behavior. TaO$_x$, used as an oxygen storage layer, also acts as an external load resistor to help achieve multibit operation and reliable retention characteristics.

2. Materials and Methods

The manufactured RS devices had a crossbar structure, and the cell size was 100 nm$^2$. We patterned TiN (Pioneer Materials, Chongqing, China) as the bottom electrode (BE) by e-beam lithography and photolithography. TAO layer was deposited by the atomic layer deposition (ALD) technique while maintaining a temperature of 200 °C. Trimethyl aluminum (TMA, Merck, Darmstadt, Germany), titanium isopropoxide (TTIP, Merck, Darmstadt, Germany) and H$_2$O were used as sources of Al, Ti and O, respectively. TiO$_2$ and Al$_2$O$_3$ were alternately deposited in super cycle ALD to form a 5 nm thick TAO layer. A 20 nm thick TaO$_x$ layer was deposited using a radio-frequency (RF) reactive sputtering method, of which the oxygen flow rate was 5 sccm. The base pressure for sputtering was 5 × 10$^{-7}$ torr, and the working pressure was 1 × 10$^{-3}$ torr. After TaO$_x$ layer formation, TiN top electrodes (TE) were patterned using the same process as used for the BE, and the TE and BE were crossed perpendicularly to make the crossbar-type device. The thermal annealing test was conducted using furnace equipment to check retention performance by baking at 125 °C for 2 h. To check the amount of Ti in AlO$_x$, compositional analyses of the TiN/AlO$_x$:Ti structure were performed based on the depth profile obtained via Auger electron spectroscopy (AES, PHI-700 ULVAC-PHI, Kanagawa, Japan). The electrical properties of our RS devices were tested using a semiconductor parameter analyzer (SPA, Keithley 4200 SCS, Beaverton, OR, USA) and arbitrary function generator (AFG, Agilent 81150A, Beaverton, OR, USA). The RF circuit-switching module accessed the two-terminal electric circuits between the SPA and the AFG, alternately. During all measurements, the TE was biased, while the BE was grounded. During multibit measurement, we used ISPP and the error check and correction (ECC) method (details concerning these methodologies available elsewhere).

3. Results

Figure 1a,b shows the SEM (ZEISS, Jena, Germany) and TEM (JEOL, Akishima, Japan) image of TiN/AlO$_x$:Ti/TaO$_x$/TiN memory devices. The thickness of the AlO$_x$ film was approximately 5 nm and the thickness of the TAO was confirmed to be 20 nm, respectively. Figure 2a,b shows the I–V characteristics according to the Ti 0% and 10% doping of Al$_2$O$_3$, which was the RS layer, respectively. To prevent a permanent dielectric breakdown, the compliance current (CC) was set to 1 uA during the ‘SET’ (resistance change from high-resistance state (HRS) to the low-resistance state (LRS) by external bias) measurement. The Ti 10%-doped Al$_2$O$_3$ device showed a very uniform distribution of the SET operating voltage at ~6 V and a RESET (resistance change from LRS to HRS) voltage distribution between −2.5 V and −3 V. Figure 2c,d shows the depth profile of AES to analyze the amount of Ti inside the AlO$_x$ thin film of both devices. As a result of the analysis, it was confirmed that about 10% of Ti was doped inside AlO$_x$, which would have improved the RS curve as well as other properties.
was confirmed that about 10% of Ti was doped inside AlO$_x$, which would have improved the RS curve as well as other properties.

Figure 1. (a) SEM image from the top of TiN/AlO$_x$:Ti/TaO$_x$/TiN device. (b) TEM image of TiN/AlO$_x$:Ti/TaO$_x$/TiN.

Figure 2. (a,b) show the DC I–V characteristics of the Ti 0% and 10% RRAM devices, respectively. (c,d) show the AES depth profile of devices.

Figure 3a,b compares the retention of RRAM devices doped with Ti 0% and Ti 10%, respectively. They were baked at 125 °C for 2 h and, as a result of the before and after comparison, it was observed that the retention of the LRS of the device doped with Ti 0%
was deteriorated. However, in the device doped with Ti 10%, it was observed that the LRS was stably maintained after 6 h. As a result, the Ti in AlO\(_x\) strengthened the retention of the device. Figure 3c,d schematically shows the mechanism of the RRAM device. The RS cycle started in the initial state. When a positive voltage was applied to the upper electrode (TE), oxygen ions moved from the resistive switching layer (Ti:AlO\(_x\)) to the oxygen ion reservoir layer (TaO\(_x\)) in Figure 3c. As a result, conduction paths were formed, resulting in an LRS state. The device then transitioned to HRS (Figure 3d) via a RESET operation. Then, the oxygen ions came out of the reservoir layer and the conduction paths were broken. However, the initial resistance of the primordial device was not fully recovered in HRS, indicating that some of the metal phase connections may have been lost and the electrically conductive paths may have been completely blocked by recombination with oxygen during RESET.

![Figure 3. (a,b) show the retention characteristics of the Ti 0% and 10% RRAM devices, respectively. The schematic figures for a sequential RS cycle. (c,d) show the LRS the HRS of the RRAM device, respectively.](image)

As shown in Figure 4, the cells subjected to the ISPP pre-cyclic pulse had a narrower distribution of resistance states. Compared to the initial state cells that did not use the ISPP pre-cycling method, cells to which ISPP pre-cycling was applied were highly likely to show an improved performance of the 4-bit/cell operation. A uniformly formed microresistive switching region in a cell could be considered to benefit from a uniform and stable performance.
As shown in Figure 4, the cells subjected to the ISPP pre-cyclic pulse had a ... overlap in the worst case overlap probability (SOP) between the resistance states, we assumed that the obtained resistance values obeyed a Gaussian distribution, and evaluated the SOP values using the equation $\sigma = \frac{m_2 - m_1}{\mu_2 - \mu_1}$, where $m_2$, $m_1$, $\mu_2$, and $\mu_1$ represent the average and standard deviations between neighboring resistance states, respectively. This equation implies that the larger the value of $\sigma$, the smaller the SOP. The distribution of each state was distinguishable from one another (lower than $2.45\sigma$ (0.71%) overlap in the worst case of the 4 bits/cell). The data indicated an excellent reliability performance in the 4 bits/cell RRAM devices.
Figure 5. (a) Shows the self-compliance effect and the BV. (b) Endurance of the initial cell and the cell to which ISPP algorithm was applied. (c) Retention of Level 1 and Level 15 of the LRS state. (d) Current range per bit. (e) Shows the endurance of 1 k cycle for each level. (f) Distributions of the 4 bits/cell operation using the ISPP in array.

4. Conclusions

By using the ISPP algorithm, we successfully achieved a 4 bits/cell approach in the sub-μm scaled RRAM devices in array. The sub-μm scaled RRAM devices exhibited a superior QLC reliability (cycle endurance > 1 k at each level, data retention > 2 h at 125 °C). Higher Ti concentrations in the TAO layer generated more leakage current characteristics and were not suitable for a stable RS operation. The SET and RESET operating voltages must still be high to facilitate a low-power RS operation depending on energy dependency. However, the QLC properties achieved in nonvolatile memory may provide guidance for the resistive switching of various metal oxide materials to be used in the implementation of in-memory computing utilizing next-generation, non-volatile memory in the future.

Author Contributions: H.J.S. and H.K.S. contributed equally to this work. Conceptualization, H.J.S. and H.K.S.; methodology, H.K.S., S.Y.L., M.P. and S.-G.P.; investigation, H.J.S., S.-G.P. and M.K.Y.; resources, S.Y.L. and M.P.; writing, H.J.S. and H.K.S.; funding acquisition, M.K.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This paper was supported by the Academic Research Fund of Myung Ki (MIKE) Hong in 2021.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-Based Resistive Switching Memories—Nanoionic Mechanisms Prospects, and Challenges. Adv. Mater. 2009, 21, 2632. [CrossRef]
2. Ahn, S.-E.; Lee, M.-J.; Park, Y.; Kang, B.S.; Lee, C.B.; Kim, K.H.; Seo, S.; Suh, D.-S.; Kim, D.-C.; Hur, J.; et al. Write current reduction in transition metal oxide based resistance change memory. Adv. Mater. 2008, 20, 924. [CrossRef]
3. Strukov, D.B.; Snider, G.S.; Stewart, D.R.; Williams, R.S. The fourth circuit element. Nature 2008, 453, 80. [CrossRef] [PubMed]
4. Mikolajick, T.; Salinga, M.; Kund, M.; Kever, T. Nonvolatile Memory Concepts Based on Resistive Switching in Inorganic Materials. *Adv. Eng. Mater.* 2009, 11, 235. [CrossRef]

5. Liu, J.-C.; Wu, T.-Y.; Hou, T.-H. Optimizing Incremental Step Pulse Programming for RRAM through Device-Circuit Co-Design. *IEEE Trans. Circuits Syst. II Express Briefs* 2018, 65, 617–621. [CrossRef]

6. Suh, K.; Suh, B.; Um, Y.; Kim, J.; Choi, Y.; Kob, Y.; Lee, S.; Kwon, S.; Choi, B.; Yun, J.; et al. A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme. *IEEE ISSCC Dig. Tech. Pap.* 1995, 30, 128–129.

7. Gao, L.; Chen, P.-Y.; Yu, S. Programming protocol optimization for analog weight tuning in resistive memories. *IEEE Electron Device Lett.* 2015, 36, 1157–1159. [CrossRef]

8. Liu, S.; Zou, X. QLC NAND study and enhanced Gray coding methods for sixteen-level-based program algorithms. *Microelectron. J.* 2017, 66, 58–66. [CrossRef]

9. Jeong, G.I.; You, S.W.; Hyun, C.S.; Lee, D.H. Evaluation of Data Encoding Method Enhancing Program Performance of NAND Flash Memory. In Proceedings of the Korea Information Processing Society Conference, Seoul, Korea, 14–15 May 2021; pp. 43–46.

10. Jeong, D.S.; Thomas, R.; Katiyar, R.S.; Scott, J.F.; Kohlstedt, H.; Petraru, A.; Hwang, C.S. Emerging memories: Resistive switching mechanisms and current status. *Rep. Prog. Phys.* 2012, 75, 076502. [CrossRef]

11. Chang, T.-C.; Chang, K.-C.; Tsai, T.-M.; Chu, T.-J.; Sze, S.M. Resistance random access memory Mater. *Today 2016*, 19, 254.

12. Linn, E.; Rosezin, R.; Kugeler, C.; Waser, R. Memory window engineering of TaOx memristive devices. *Appl. Phys. Lett.* 2010, 97, 232102. [CrossRef]

13. Lee, M.; Lee, C.B.; Lee, D.; Lee, S.R.; Chang, M.; Hur, J.H.; Kim, Y.; Kim, C.; Seo, D.H.; Seo, S.; et al. A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5(5-x)/TaO2(2-x) bilayer structures. *Nat. Mater.* 2011, 10, 625. [CrossRef] [PubMed]

14. Yang, J.J.; Zhang, M.-X.; Strachan, J.P.; Miao, F.M.; Pickett, M.D.; Kelley, R.D.; Ribeiro, G.M.; Williams, R.S. High switching endurance in TaOx memristive devices. *Appl. Phys. Lett.* 2013, 102, 063002. [CrossRef]

15. Kim, G.H.; Lee, J.H.; Seok, J.Y.; Song, S.J.; Yoon, J.H.; Yoon, K.J.; Lee, M.H.; Kim, K.M.; Lee, H.D.; Ryu, S.W.; et al. Improved endurance of resistive switching TiO2 thin film by hourglass shaped Magnéli filaments. *Appl. Phys. Lett.* 2011, 98, 262901.

16. Yang, Y.; Sheridan, P.; Lu, W. Complementary resistive switching in tantalum oxide-based resistive memory devices. *Appl. Phys. Lett.* 2012, 100, 203112. [CrossRef]

17. Torrezan, A.C.; Strachan, J.P.; Medeiros-Ribeiro, G.; Williams, R.S. Sub-nanosecond switching of a tantalum oxide memristor. *Nanotechnology* 2011, 22, 485203. [CrossRef]

18. Jo, S.H.; Kim, K.-H.; Lu, W. High-Density Crossbar Arrays Based on a Si Memristive System. *Nano Lett.* 2009, 9, 870. [CrossRef]

19. Linn, E.; Rosezin, R.; Kugeler, C.; Waser, R. Memory window engineering of Ta2O5-x oxide-based resistive switches via incorporation of various insulating frames. *Nat. Mater.* 2010, 9, 403. [CrossRef]

20. Waser, R.; Aono, M. Nanoinionics-based resistive switching memories. *Nat Mater.* 2007, 6, 833–840. [CrossRef]

21. Yanagida, T.; Nagashima, K.; Oka, K.; Kanai, M.; Klamchuen, A.; Park, B.H.; Kawase, T. Scaling effect on unipolar and bipolar resistive switching of metal oxides. *Sci. Rep.* 2013, 3, 1–6. [CrossRef]

22. Lee, M.J.; Park, Y.D.; Suh, D.; Lee, E.H.; Seo, S.; Kim, D.-C.; Jung, R.J.; Kang, B.-S.; Ahn, S.-E.; Lee, C.B.; et al. Two Series Oxide Resistors Applicable to High Speed and High Density Nonvolatile Memory. *Adv. Mater.* 2007, 19, 3919–3923. [CrossRef]

23. Yang, J.J.; Pickett, M.D.; Li, X.; Ohlberg, D.A.A.; Stewart, D.R.; Williams, R.S. Memristive switching mechanism for metal/oxide/metal nanodevices. *Nat. Nanotechnol.* 2008, 3, 429–433. [CrossRef] [PubMed]

24. Sawa, A. Resistive switching in transition metal oxides. *Mater. Today.* 2008, 11, 28–36. [CrossRef]

25. Nair, C.; Molas, G.; Blaise, P.; Piccolboni, G.; Sklenard, B.; Cagli, C.; Bernard, M.; Roule, A.; Azzaz, M.; Vianello, E.; et al. Understanding RRAM endurance, retention and window margin trade-off using experimental results and simulations. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016.

26. Wei, Z.; Takagi, T.; Kanzawa, Y.; Katoh, Y.; Ninomiya, T.; Kawai, K.; Muraoka, S.; Mitani, S.; Katayama, K.; Fujii, S.; et al. Retention Model for High-Density ReRAM. In Proceedings of the 2012 4th IEEE International Memory Workshop, Milan, Italy, 20–23 May 2012.

27. Ielmini, D. Resistive switching memories based on metal oxides: Mechanisms, reliability and scaling. *Semicond. Sci. Technol.* 2016, 31, 063002. [CrossRef]

28. Clima, S.; Chen, Y.Y.; Chen, C.Y.; Goux, L.; Govoreanu, B.; Degraeve, R.; Fantini, A.; Jurczak, M.; Pourtois, G. First-principles thermodynamics and defect kinetics guidelines for engineering a tailored RRAM device. *J. Appl. Phys.* 2016, 119, 225107. [CrossRef]

29. Chen, Y.Y.; Komura, M.; Degraeve, R.; Govoreanu, B.; Goux, L.; Fantini, A.; Raghavan, N.; Clima, S.; Zhang, L.; Belmonte, A.; et al. Improvement of data retention in HfO2/Hf ITIR RRAM cell under low operating current. In Proceedings of the 2013 IEEE International Electron Devices Meeting, Washington, DC, USA, 9–11 December 2013.

30. Lee, D.K.; Kim, G.H.; Shon, S.; Yang, M.K. Role of an Interfacial Layer in Ta2O5-Based Resistive Switching Devices for Improved Endurance and Reliable Multibit Operation. *Phys. Status Solidi RRL* 2020, 14, 1900646. [CrossRef]

31. Zhao, L.; Clima, S.; Magyari-Köpe, B.; Jurczak, M.; Nishi, Y. Ab initio modeling of oxygen-vacancy formation in doped-HfOx RRAM: Effects of oxide phases, stoichiometry, and dopant concentrations. *Appl. Phys. Lett.* 2015, 107, 013504. [CrossRef]

32. Park, S.G.; Yang, M.; Ju, H.; Seong, D.; Lee, J.M.; Kim, E.; Jung, S.; Zhang, L.; Shin, Y.; Baek, I.; et al. A non-linear ReRAM cell with sub-1Ua ultralow operating current for high density vertical resistive memory (VRRAM). In Proceedings of the IEEE Int. Electron Devices Meeting (IEDM), San Francisco, CA, USA, 10–13 December 2012.
33. Crowley, M.; Al-Shamma, A.; Bosch, D.; Farmwald, M.; Fasoli, L.; Ilkbahar, A.; Johnson, M.; Kleveland, B.; Lee, T.; Liu, T.-Y.; et al. 512 Mb PROM with 8 Layers of Antifuses/Diode Cells. In Proceedings of the 2003 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 13 February 2003; pp. 284–285.

34. Kawahara, A.; Azuma, R.; Ikeda, Y.; Kawai, K.; Kato, Y.; Hayakawa, Y.; Tsuji, K.; Yoneda, S.; Himeno, A.; Shimakawa, K.; et al. An 8 Mb Multi-Layered Cross-Point ReRAM Macro with 443 MB/s Write Throughput. *IEEE J. Solid-State Circuits* **2012**, *48*, 432–433. [CrossRef]

35. Chevallier, C.J.; Siau, C.H.; Lim, S.F.; Namala, S.R.; Matsuoka, M.; Bateman, B.L.; Rinerson, D. A 0.13 µm 64 Mb Multi-Layered Conductive Metal-Oxide Memories. In Proceedings of the 2010 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 7–11 February 2010; pp. 260–261.