Predictable Sharing of Last-level Cache Partitions for Multi-core Safety-critical Systems

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ABSTRACT
Last-level cache (LLC) partitioning is a technique to provide temporal isolation and low worst-case latency (WCL) bounds when cores access the shared LLC in multicore safety-critical systems. A typical approach to cache partitioning involves allocating a separate partition to a distinct core. A central criticism of this approach is its poor utilization of cache storage. Today’s trend of integrating a larger number of cores exacerbates this issue such that we are forced to consider shared LLC partitions for effective deployments. This work presents an approach to share LLC partitions among multiple cores while being able to provide low WCL bounds.

KEYWORDS
Last-level cache, Predictability, Cache partitioning

1 INTRODUCTION
The use of multicores in safety-critical systems offers an attractive opportunity to consolidate several functionalities onto a single platform with the benefits of reducing cost, size, weight, and power while delivering high performance. Although multicores are mainstay in general-purpose computing, their use in safety-critical systems is approached with caution. This is because multicores often share hardware resources to deliver their high performance, but since safety-critical systems must be certified, this makes guaranteeing compliance with safety standards increasingly challenging. The central reason behind this difficulty is that shared resources complicate worst-case timing analysis necessary for applications deemed to be of high criticality. For instance, the automotive domain uses the ISO-26262 [6] standard, which identifies ASIL-D as the highest criticality application where a violation of its temporal behaviours may result in a significant loss of lives or injury.

One such shared hardware resource is the shared last-level cache (LLC) that multiple cores access when they experience misses in their private caches. For example, the Kalray MPPA 3 [3] features an 80-core architecture with 16 cores in a cluster that share 4MB of LLC. LLCs are an important component of the memory hierarchy to deliver high performance [2]. However, multiple cores accessing the LLC can introduce inter-core temporal interferences where one core evicts the data of another’s resulting in large variations in execution times. These interferences complicate worst-case latency (WCL) analysis, and often result in overly pessimistic worst-case bounds. LLC partitioning has been proposed as a countermeasure to address these difficulties in using LLCs with multicores [4, 8, 9]. LLC partitioning allocates a part of the LLC to each core that it can use. This provides temporal isolation to tasks executing on a core from other tasks executing on another core. However, there are multiple downsides to LLC partitioning: (1) it can significantly affect average-case performance, (2) it can lead to underutilization of cache capacity, and (3) prevent coherent data sharing [1]. Downside (1) is a result of each core having a smaller part of the LLC. (2) happens when a core gets allocated a partition that it doesn’t effectively use. Lastly, for (3), conventional LLC partitioning disallows one core to access a partition of another core; thus, accessing shared data between cores in the LLC is prohibited. This prevents LLC caching of coherent data across multiple cores. With the continued increase in demand for functionalities, and their consolidation onto a multicore platform, we expect these downsides to overwhelm the benefits of LLC partitioning, and force us to seriously consider sharing LLC partitions in the near future.

As a cautious step towards addressing these downsides, and possibly a refreshing alternative to traditional LLC partitioning approaches, we allow multiple cores to share partitions. This requires us to determine the WCL of memory accesses from cores that miss in their private caches, and access the shared partition. In this paper, we develop such a WCL analysis. In doing so, we show that naively arbitrating cores’ accesses to the shared LLC partitions results in a scenario where the WCL is unbounded. We correct this unbounded scenario by showing that a restricted version of time-division multiplexing (TDM) policy called 1S-TDM can result in a WCL bound. However, the resulting WCL bound is grossly pessimistic; it is proportional to the minimum of the cache capacity and LLC partition size of a given core and cube of the number of cores. By methodically analyzing the critical instance that renders the WCL bound, we intuit a technique to significantly lower the WCL. This technique yields a WCL that eliminates the dependency on the cache and partition sizes. For a 4-core setup with a 16-way LLC with 128 cache lines, our approach results in a WCL that is 2048 times lower. We implement this technique in a hardware structure called the set sequencer. We also show that careful sharing of cache partitions not only allows for a low WCL, but possibly higher average-case performance. We envision the proposed work to complement existing efforts on LLC partitioning where certain tasks have their own partitions, but others share partitions; all of which depends on their performance and real-time requirements. The following are our main contributions.

- We identify that naively using TDM to arbitrate accesses to the shared LLC partitions can result in an unbounded WCL. We resolve this by showing that a 1S-TDM schedule prohibits this scenario.
- We develop a WCL analysis for a memory access to a shared LLC partition using the 1S-TDM arbitration policy.
- We propose a micro-architectural extension called the set sequencer that significantly lowers the WCL when sharing a LLC partition.
- We evaluate the proposed approach by implementing a simulation of the set sequencer.
2 RELATED WORKS

Cache partitioning [4] reserves a portion of the cache to a task or a core either via hardware or software techniques [12]. The key role of cache partitioning is to improve temporal isolation to simplify the WCL analysis. However, as the number of cores increase, allocating distinct partitions to each core or each task can affect average-case performance and cache under-utilization. Moreover, this prohibits deploying a large number of functionalities on the multi-core as it may result in extremely small partitions to each functionality, which would adversely affect performance. The proposed work seeks a middle ground where designers can judiciously share partitions with a subset of cores, and isolate others. Prior works identified that accurately capturing the contention of multiple cores sharing the LLC is difficult [10], and attempts exist for shared cache for dual-core processor relying on knowledge of the application [11]. Our work does not rely on application-specific knowledge and does not constraint the number of cores.

Authors in [7] noticed that interference between tasks exists when multiple tasks or cores share the LLC. They proposed a time analysable shared LLC where the inter-task interference is bounded probabilistically. Given their proposed technique, the exact worst-case interference in the LLC and the exact worst-case latency is not discernible. Compared to [7], our analysis provides an exact (non-probabilistic) bound of a memory access in the LLC, and does not rely on MBPTA. Our work assumes that a TDM bus arbitration has one slot in each period, which is common in controlling access to resources in safety-critical systems [1, 5]. We also identified the worst-case scenario for the LLC evictions, and that in the worst-case the latency can be unbounded if the arbitration has no constraint. Moreover, our analysis does not rely on certain type of address mapping or replacement policy.

3 SYSTEM MODEL

System hierarchy. We assume a system with $N$ cores and three levels of cache in the memory hierarchy (Figure 1). Each core has a private L1 instruction cache (L1I*) and a private L1 data cache (L1D*). The private L1 caches of a core are connected to a L2 cache (L2*). A set-associative last-level cache (LLC), or the L3 cache (L3*), connects to all L2 caches, and interfaces with a DRAM directly. The accesses from L2 to L3 is controlled by a shared bus. The shared bus implements a time-division multiplexing (TDM) arbitration where equally sized slots are allocated to cores. The L2 cache controller of each core only accesses the LLC in the core’s allocated slot, and the LLC only responds to the L2 within the core’s slot. Since the L2 cache is private to each core, a core accessing the bus implies that the core’s L2 cache controller access the bus. An LLC partition isolates a part of the LLC for a specific core. We assume one task can be mapped to one core.

Similar to prior works [1], we assume each core has at most one outstanding memory request. Before a core’s request or write-back is placed on the bus, we assume that the request is buffered in a structure named pending request buffer (PRB), and the write-backs are buffered in a structure named pending write-back buffer (PWB). There is a predictable arbitration such as round-robin between PRB and PWB to choose from a request or a write-back to send on the bus at the beginning of the core’s slot.

Cache inclusion policy. We assume that the LLC is inclusive of L2. This is a common setup in existing platforms. Suppose that core $c_i$’s request to the cache line at address $X$ is a miss in all its private caches, and the LLC. Then, for the LLC to respond with the provided data for $X$, the LLC must ensure the following: (1) that there is an empty line in the set that cache line $X$ maps to, (2) the cache line from a lower level memory in the memory hierarchy is fetched, and (3) the response to $c_i$ is sent in $c_i$’s slot. An important property of inclusive caches is that an eviction of a cache line in the lower-level cache requires eviction of cache lines for the same address in upper-level caches. For our setup, an eviction in the LLC, would force evictions in both the L1 and L2 private caches that have the data.

4 WCL WITH SHARED PARTITIONS

4.1 An unbounded WCL scenario

We show that an undesired consequence of the inclusive property, and multiple cores making accesses to the LLC is a situation where the WCL is unbounded. Using Figure 2, we illustrate this scenario. We assume a TDM arbitration policy with one slot for $c_{ua}$ and two slots for $c_i$. We use $s_{t, i}$ to denote the starting time of the $t$-th slot of core $c_i$. Unambiguously, $s_{t, i}$ also refers to the $t$-th slot of $c_i$. At $s_{t, ua}$, in Figure 2, $c_{ua}$’s request to a cache line $X$ misses in the private caches and the LLC. Cache line $X$ is mapped to a full cache set $set_{LLC}(X)$ in the LLC; thus, the LLC evicts a cache line $i_1$ in $set_{LLC}(X)$, which is also privately cached by $c_i$ denoted by $i_1 : c_i$. Note that a full cache set means that there are no empty cache lines in the set. In Figure 2, $c_i$ writes back $i_1$, and frees an entry in $set_{LLC}(X)$. Then, in Figure 2, $c_i$ requests a cache line mapped to $set_{LLC}(X)$, and gets the response within its slot because $i_1$ is available. In $c_{ua}$’s next slot $s_{t+1, ua}$, $set_{LLC}(X)$ is full again preventing $c_{ua}$ from completing its request. This behavior can potentially repeat indefinitely, which shows that the interference at the LLC from other cores can cause unbounded WCL for the core under analysis.
4.2 One-slot TDM schedule

The scenario where $c_{ua}$ experiences unbounded latency happens when a core other than $c_{ua}$ is allowed to access the LLC multiple times before $c_{ua}$ can access the bus again. An effective solution to prevent another core from occupying a free entry in $set_{LLC}(X)$ is to constrain the TDM schedule to allocate only one slot per core in a period (Definition 4.1). Note that the crux of the issue is that an entry freed by $c_{i}$ due to the eviction of cache line $l_{1}$ is occupied again by $c_{i}$ again before $c_{ua}$ can access the LLC. With 1S-TDM, we only allow one core to perform one access to the bus in a period.

Definition 4.1. A one-slot TDM schedule (1S-TDM) is a TDM schedule that has exactly one slot allocated to each core in every period.

4.3 Key observations

Although a 1S-TDM schedule guarantees a WCL bound for $c_{ua}$, we show that the WCL is proportional to the minimum of the cache capacity of $c_{ua}$ and $c_{ua'}$’s LLC partition size $M$, and cube of the number of cores. This results in a significantly large WCL. We illustrate this by making observations from two examples.

Consider the example in Figure 3 that has four cores, and a two-way set-associative LLC. The 1S-TDM schedule is $\{c_{ua}, c_{2}, c_{3}, c_{4}\}$. In Figure 3, $c_{ua}$ requests cache line $X$, which is not privately cached by $c_{ua}$. Hence, its L2 cache controller issues request for $X$ at the beginning of $s_{tua}^{f}$ to the LLC. Cache line $X$ maps to a cache set $set_{LLC}(X)$ in the LLC, and it also experiences a miss in the LLC. Since $set_{LLC}(X)$ has no empty lines, it must evict one cache line in $set_{LLC}(X)$. Suppose that $l_{1} \in set_{LLC}(X)$ is selected for eviction. Note that $l_{1}$ is privately cached in $c_{3}$ denoted by $l_{1} : c_{3}$. Hence, $c_{3}$ must also evict $l_{1}$ from its private caches in Figure 3, resulting in a free entry in $set_{LLC}(X)$, denoted as $l_{1} : \_$. Clearly, the cache line to replace depends on the replacement policy. In this work, we assume a replacement policy that can select any of the cache lines. Even though we select $l_{1}$ in this example, our observation is agnostic of replacement policy. As a result, the observation applies to any replacement policy, including least-recently used (LRU).

Next, in Figure 4, $c_{4}$’s L2 cache controller issues a request, and occupies the free entry, preventing $c_{ua}$ from obtaining its response in slot $s_{tua}^{e+1}$. As a result, the LLC must evict a cache line in $set_{LLC}(X)$ to make space for $c_{ua}$, and the LLC evicts $l_{2}$ in slot $s_{tua}^{e+2}$ which is privately cached by $c_{3}$. As before, $c_{3}$ evicts $l_{2}$ in Figure 4, but it is occupied by $c_{4}$ in Figure 3. Note that in the period starting at $s_{tua}^{e+2}$, this pattern of interfering $c_{ua}$ from receiving its response cannot continue. When $c_{4}$ evicts $l_{1}$ in Figure 3, there is no other core that can occupy the free entry; thus, $c_{ua}$ will get its response in $s_{tua}^{e+3}$ at Figure 3. This is guaranteed to occur because whenever any core other than $c_{ua}$ occupies a free entry in $set_{LLC}(X)$, $c_{ua}$ gets closer to being able to occupy a free entry in $set_{LLC}(X)$. For example, in Figure 3, both cache lines are privately cached by $c_{4}$, and any core making a request to $set_{LLC}(X)$ resulting in a miss requires $c_{4}$ to evict it from its private caches as well. Since, $c_{ua}$’s slot comes after $c_{4}$’s, it is guaranteed to occupy the free cache line entry due to $c_{4}$’s eviction. We characterize this closer effect by introducing a notion of distance (Definition 4.2).

Definition 4.2. For a 1S-TDM schedule $S$, the distance between two cores $c_{i}$ and $c_{j}$, $d_{ci}^{S}$, is the number of slots between the start of slot of $c_{i}$, and the start of $c_{j}$’s next slot.

Corollary 4.3. Given a 1S-TDM schedule $S$ with $N$ cores, the distance between any two cores $c_{i}$ and $c_{j}$, $d_{ci}^{S}$, $1 \leq d_{ci}^{S} \leq N$.

Given a cache line $l_{i}$, we will use $d_{ci}^{(l)}(x)$ as a convenience to return the distance between the core that has privately cached $l_{i}$, and $c_{i}$ at $x$. Using Figure 3, with a TDM schedule of $\{c_{ua}, c_{2}, c_{3}, c_{4}\}$, $d_{c4}^{c2} = 2$ and $d_{c4}^{c3} = 1$. With Definition 4.2, the example in Figure 3 can be interpreted in terms of distance: the core that caches $l_{1}$ changes from $c_{3}$ in slot 1, with a distance of $d_{c3}^{c1} = 2$, to $c_{4}$ in slot 4, with a distance of $d_{c4}^{c1} = 1$, and finally freed in slot 5. Similarly, the core that caches $l_{2}$ changes from $c_{3}$ in slot 1 to $c_{4}$ in slot 1, and thus the distance of the core that caches $l_{2}$ decreases from 2 to 1. These example scenarios highlight the following key observations.

Observation 1. Given a 1S-TDM schedule $S$, the distance of cache lines in $set_{LLC}(X)$ decrease when $c_{ua}$ does not perform write-backs after issuing its request to cache line $X$ and before receiving its response for $X$.

The decreasing distance articulates the effect of the core under analysis getting closer to occupying a freed cache line entry in $set_{LLC}(X)$. A direct consequence of observation 1 is that $c_{ua}$’s request will eventually complete as described in observation 2.

Observation 2. $c_{ua}$’s request will eventually complete.

The main intuition behind this observation is that once the lines in $set_{LLC}(X)$ are privately cached by $c_{4}$, a request for $X$ by $c_{ua}$ will succeed in the following period (Figure 3). This is because $c_{4}$ must evict the privately cached line due to inclusive property, which results in a free entry in $set_{LLC}(X)$ that $c_{ua}$ can occupy. When $n \leq N$ cores share a partition with a 1S-TDM schedule and there are $w$ ways in $set_{LLC}(X)$, for $c_{ua}$ to occupy an entry in $set_{LLC}(X)$ in the worst-case, the distance of all $w$ cache lines must experience the largest decrements. Since the maximum distance is $n$ when $c_{ua}$ caches a cache line, and the minimal distance is 1, $c_{ua}$ must wait for the distance of all $w$ cache lines to decrease from $n$ to 1, accounting for $w(n - 1)$ decrements in the worst-case.

Note that we have not considered scenarios where $c_{ua}$ performs write-backs before receiving the response for its request. When a core other than $c_{ua}$ requests a cache line that is privately cached by $c_{ua}$, then $c_{ua}$ would also need to perform write-backs due to inclusivity. The effect of write-backs on the distance is summarized in observation 3. After a write-back by $c_{ua}$, cache lines in $set_{LLC}(X)$ can be privately cached by a core with a larger distance compared to before $c_{ua}$ performs the write-back.

Figure 3: $c_{ua}$’s request to cache line $X$ eventually is completed.
Observation 3. Given a 1S-TDM, when \( c_{uu} \) performs a write-back after issuing its request to a cache line \( X \) and before receiving the response, the distance of cache lines in \( set_{LLC}(X) \) increases.

Figure 4 shows a scenario with \( c_{uu} \) performing write-backs. There are four cores with 1S-TDM schedule of \( \{c_{uu},c_2,c_3,c_4\} \). Cache lines \( l_1 \) and \( l_2 \) are in \( set_{LLC}(X) \), and are initially privately cached by \( c_4 \). In \( \Box \), \( c_{uu} \) issues a request to cache line \( X \) that misses in the private caches and LLC. This is followed by \( c_2 \) issuing a request to cache line \( Y \) such that \( Y \in set_{LLC}(X) \) in \( \Box \), and it also misses in the private caches and LLC. The LLC selects to evict another line \( l_2 \), which needs to be evicted by \( c_4 \). In \( \Box \), \( c_3 \) issues a request to cache line \( A \) that causes \( c_1 \) to evict a cache line \( l \). In \( \Box \), \( c_4 \) writes back \( l_1 \) freeing up an entry in \( set_{LLC}(X) \). In the write-back slot of \( s_{uu}^{t+1} \) \( \Box \), \( c_1 \)’s request to \( X \) cannot be satisfied because \( c_1 \) has to perform an eviction. The free entry is thus occupied by \( c_2 \). Note that the core that is caching \( l_1 \) has changed from \( c_4 \) to \( c_2 \) and thus the distance of the core caching \( l_1 \) increased from \( d_{c_1}^4 = 1 \) to \( d_{c_2}^4 = 3 \). In general, write-backs from \( c_{uu} \) allow a core with a larger distance to occupy a free entry in \( set_{LLC}(X) \) that would have satisfied \( c_{uu} \)’s request; thus, the distance of cores caching cache lines in \( set_{LLC}(X) \) does not always decrease as in the case of Observation 1 when \( c_{uu} \) performs write-backs. Combining these two observations, we develop an analysis that bounds the worst-case latency of a request.

4.4 WCL analysis for 1S-TDM schedule

We first prove that the distance in \( set_{LLC}(X) \) only decreases when no write-back by \( c_{uu} \) is involved with Corollary 4.5 (Observation 1). Then, we bound the latency required for the distance to decrease. Next, in Lemma 4.6, we show that distance increases when \( c_{uu} \) writes back cache lines (Observation 2). Hence, when \( c_{uu} \) waits for its response, the distance in \( set_{LLC}(X) \) shows an alternating pattern of decreasing and increasing. Finally, Theorem 4.7 combines Corollary 4.5 and Lemma 4.6 to express the WCL of \( c_{uu} \)’s request.

We use our key observations to formulate an analysis to compute the WCL. Consider a multicore configuration with \( N \) cores interacting over the shared bus using a 1S-TDM schedule \( S \), and \( n \) cores sharing a partition \( P \) in the LLC (\( n \leq N \)) with \( c_{uu} \) being one of the \( n \) cores. Throughout the analysis, we assume that \( c_{uu} \)’s request for cache line \( X \) misses in its private caches and the LLC, and \( set_{LLC}(X) \) is full before \( c_{uu} \)’s request to cache line \( X \) is completed.

**Figure 4: Distance of core caching \( l_1 \) increases after \( s_{uu}^{t+1} \).**

**Lemma 4.4.** If \( c_{uu} \)’s request is not completed at slot \( s_{uu}^{t+T} \), \( c_{uu} \) does not perform any write-backs, and \( l_x \in set_{LLC}(X) \) is evicted in response to \( c_{uu} \)’s request in \( s_{uu}^{t} \), then

\[
\forall l \in set_{LLC}(X) : d_{c_{uu}}^{t}(s_{uu}^{t+T}) \leq d_{c_{uu}}^{t}(s_{uu}^{t})
\]

**Proof.** We prove the lemma by contradiction and assume that \( \exists l \in set_{LLC}(X) : d_{c_{uu}}^{t}(s_{uu}^{t+T}) > d_{c_{uu}}^{t}(s_{uu}^{t}) \). Then, before \( s_{uu}^{t+T} \), there must exist two cores \( c_i \) and \( c_j \) such that \( c_i \) frees the entry \( l \) and \( c_j \) occupies \( l \) after \( c_i \) frees \( l \). The freeing-then-occupying by \( c_i \) and \( c_j \) increases the distance of \( l \) to be greater than \( d_{c_{uu}}^{t}(s_{uu}^{t}) \), that is, \( d_{c_{uu}}^{t} \leq d_{c_{uu}}^{t}(s_{uu}^{t}) < d_{c_{uu}}^{t}(s_{uu}^{t+T}) \). Assume that \( l_i \) frees \( l \) in \( s_{uu}^{t} \) and \( c_j \) occupies \( l \) in \( s_{uu}^{t+T} \), then \( s_{uu}^{t} < s_{uu}^{t+T} \). Furthermore, because \( d_{c_{uu}}^{t} < d_{c_{uu}}^{t+T} \) and 1S-TDM is deployed, \( s_{uu}^{t} \) must be in the next period of \( s_{uu}^{t+T} \). There must be a slot of \( c_{uu} \)-write-backs, such that \( s_{uu}^{t} < s_{uu}^{t+1} < s_{uu}^{t+T} \). Consequently, there is a free entry in \( set_{LLC}(X) \) in slot \( d_{c_{uu}}^{t+1} \). Because \( c_{uu} \)’s request is not completed in slot \( s_{uu}^{t+T} \), it is not completed in slot \( d_{c_{uu}}^{t+1} \). The only reason that \( c_{uu} \)’s request is not completed in its slot when there is a free entry is that \( c_{uu} \) is performing a write-back, which contradicts the hypothesis that \( c_{uu} \) does not perform any write-backs.

**Corollary 4.5.** If \( c_{uu} \) does not perform any write-backs, \( l_x \in set_{LLC}(X) \) is evicted in response to \( c_{uu} \)’s request in \( s_{uu}^{t} \) and \( c_{uu} \)’s request is not completed in \( s_{uu}^{t+2(2n-1)} \), then

\[
d_{c_{uu}}^{t}(s_{uu}^{t+2(2n-1)}) < d_{c_{uu}}^{t}(s_{uu}^{t})
\]

**Proof.** Assume that at \( s_{uu}^{t} \), cache line \( l_x \) is evicted, but it is also privately cached by \( c_j \) such that \( d_{c_{uu}}^{t} = d_{c_{uu}}^{t}(s_{uu}^{t}) \). At a later slot for \( c_j \), \( s_{uu}^{t+q} \), where \( l_x \) is written back, \( q \leq t + 2(n - 2) + 1 < t + 2(n - 1) \). This is because there can be at most \((n - 1)\) pending write-backs in \( c_j \)’s WBV including the write-back for \( l_x \). Before \( c_{uu} \)’s next slot, another core \( c_j \) must occupy \( l_x \) so that \( c_{uu} \)’s request is not completed. Due to 1S-TDM, if \( c_j \) occupies \( l_x \), \( d_{c_{uu}}^{t+T} < d_{c_{uu}}^{t}(s_{uu}^{t}) \). Applying Lemma 4.4, \( s_{uu}^{t+2(2n-1)} \leq d_{c_{uu}}^{t} < d_{c_{uu}}^{t}(s_{uu}^{t}) \).

**Lemma 4.6.** Given a slot \( s_{uu}^{t+1} \) where \( c_{uu} \) performs write-back, then there exists an execution such that

\[
\forall l \in set_{LLC}(X) : d_{c_{uu}}^{t}(s_{uu}^{t+1}) \geq d_{c_{uu}}^{t}(s_{uu}^{t})
\]

**Proof.** In \( s_{uu}^{t+1} \), let us assume that \( c_{uu} \) writes back a cache line as a response to an eviction caused by another core. Since \( c_{uu} \) is performing a write-back, it cannot issue a request; thus, its request cannot complete. Hence, for each of the free cache line entry \( l \) in \( set_{LLC}(X) \) at \( s_{uu}^{t+1} \), a core \( c_j \) can make a request to \( l \) after \( s_{uu}^{t+1} \) which completes within one slot. Then, \( d_{c_{uu}}^{t}(s_{uu}^{t+1}) = d_{c_{uu}}^{t+1} > d_{c_{uu}}^{t}(s_{uu}^{t+1}) \). For other cache lines \( l' \in set_{LLC}(X) \) that are privately cached by other cores that are not evicted due to accesses made by some other cores, \( d_{c_{uu}}^{t}(s_{uu}^{t+1}) = d_{c_{uu}}^{t}(s_{uu}^{t+1}) \) holds trivially.

Corollary 4.5 and Lemma 4.6 provide the cornerstone to derive the worst-case latency for \( c_{uu} \) in Theorem 4.7.
Theorem 4.7. Let \( m = \min(m_{\text{ena}}, M) \), where \( m_{\text{ena}} \) is the cache capacity of \( e_{\text{ena}} \). The worst-case latency in number of slots of the request of the core under analysis \( e_{\text{ena}} \), \( \text{WCL} \), is given by:

\[
\text{WCL} = ((m + 1) \cdot A \cdot N + 1) \cdot SW,
\]

where \( A = 2(n - 1) \cdot w \cdot (n - 1) \).

Proof. The critical instance has \( e_{\text{ena}} \) making a request and receiving a response with the possibility of multiple write-backs from any core in between as shown in Figure 5. We split this critical instance into four parts. (1) The number of write-backs \( e_{\text{ena}} \) can perform in the worst-case. (2) The worst-case latency between two write-backs by \( e_{\text{ena}} \). (3) The worst-case latency before the first write-back of \( e_{\text{ena}} \). (4) The worst-case latency after the last write-back of \( e_{\text{ena}} \) until it receives its response. For (1), in the worst-case, other cores cause \( m = \min(m_{\text{ena}}, M) \) write-backs on \( e_{\text{ena}} \), which is the maximal number of cache lines \( e_{\text{ena}} \) can cache with partition \( P \). For (2), we showed that the distance for a given cache line can both increase and decrease under certain situations. According to Lemma 4.6, after a write-back, \( d_{\text{ena}}^{(l)} \) can increase from 1 to \( n \) in the worst-case for all \( l \in \text{set}_{\text{LLC}}(X) \). Note that the distance would be \( n \) if the core just after \( e_{\text{ena}} \) was to privately cache the requested line. From Corollary 4.3, \( d_{\text{ena}}^{(l)} \) ranges from 1 to \( n \) and in the worst-case, \( d_{\text{ena}}^{(l)} \) can decrease from \( n \) to 1 for each of the \( w \) cache lines \( l \in \text{set}_{\text{LLC}}(X) \) before encountering the next write-back in the worst-case. Corollary 4.5 shows that it takes \( 2(n - 1) \) periods in the worst case to strictly decrease \( d_{\text{ena}}^{(l)} \), and the worst-case decrement of distance is by 1. Hence, for all \( w \) cache lines to decrease from \( n \) down to 1, it takes \( A = 2(n - 1) \cdot w(n - 1) \) periods, or \( A \cdot N \) slots. For (3), in the worst-case, the distance of all \( w \) cache line entries in \( \text{set}_{\text{LLC}}(X) \) decreases from \( n \) down 1 before the first write-back. Following a similar argument as in (2), the WCL in (3) is hence \( A \) periods or \( A \cdot N \) slots. Similar to (3), for (4), after the last write-back, the distance of all \( w \) cache line entries in \( \text{set}_{\text{LLC}}(X) \) decreases from \( n \) down 1 before \( e_{\text{ena}} \) receives its response, and finally, one slot is required for \( e_{\text{ena}} \) to receive its response, which translates to a worst-case latency of \( A \cdot N + 1 \) slots. Combining (1), (2), (3) and (4), \( \text{WCL} = ((m + 1) \cdot (A \cdot N) + (A \cdot N + 1)) \cdot \text{SW} = ((m + 1) \cdot (A \cdot N + 1)) \cdot \text{SW} \)

\[ \text{WCL}_{\text{ena}} = (2(n - 1) \cdot n + 1) \cdot N \cdot \text{SW}. \]

\[ \text{WCL}_{\text{ena}} = (2(n - 1) \cdot n + 1) \cdot N \cdot \text{SW}. \]

Proof. In the worst-case, all other \( (n - 1) \) cores issue their request before \( e_{\text{ena}} \) sends its request to cache line \( X \) to the LLC, and it is the last request in the set sequence for a full set \( \text{set}_{\text{LLC}}(X) \). For each request in the set sequencer, including \( e_{\text{ena}} \), it takes \( 2(n - 1) \)

4.5 Set sequencer: Lowering the WCL

We propose a hardware extension called a set sequencer that enables us to significantly lower the WCL. Recall that the WCL analysis yields a WCL for a core under analysis \( e_{\text{ena}} \) to be proportional to the minimum of either the cache capacity or \( e_{\text{ena}} \)’s LLC partition size, and cube of the number of cores. This bound is clearly large making it difficult to allow cores to share partitions in the LLC. When using the set sequencer, the WCL bound ends up being independent of the minimum of the cache capacity of \( e_{\text{ena}} \) and \( e_{\text{ena}} \)’s LLC partition size.

![Figure 5: An illustration that shows the WCL of e_{ena}](image)

**Figure 6: An illustration of set sequencer.**

M. We illustrate the main idea behind set sequencer using Figure 6, which contains two structures, a Queue Lookup Table (QLT) \( (\mathcal{Q}) \) and a Sequencer (SQ) \( (\mathcal{S}) \). The set sequencer contains one entry in the QLT for each set in the partition that has at least one pending LLC request. The entry maps the set to a queue in SQ. For example, \( c_1 \) has requested for set 3, but \( c_1 \) has yet to occupy a free cache line in that set. This may be because another core may still have to evict a cache line from their private caches before set 3 has a free cache line. When there are multiple cores requesting a cache line from the same set, such as set 5, which maps to queue 2 in SQ, then set sequencer stores the order in which the requests arrived at the LLC (broadcast order on the shared bus). For this set, core \( c_2 \) would occupy a free cache line in set 5 before \( c_3 \), and so on. Our key observations and the WCL analysis revealed that the distance increases whenever \( e_{\text{ena}} \) is prevented from occupying a free cache line entry due to another core intercepting it. By maintaining order using set sequencer, we can guarantee that does not happen. We present the WCL when using the set sequencer in Theorem 4.8.

**Theorem 4.8. The WCL of a request of the core under analysis e_{ena} when using the set sequencer, \( \text{WCL}_{\text{ena}} \), is given by:**

\[ \text{WCL}_{\text{ena}} = (2(n - 1) \cdot n + 1) \cdot N \cdot \text{SW}. \]

Proof. In the worst-case, all other \( (n - 1) \) cores issue their request before \( e_{\text{ena}} \) sends its request to cache line \( X \) to the LLC, and it is the last request in the set sequence for a full set \( \text{set}_{\text{LLC}}(X) \). For each request in the set sequencer, including \( e_{\text{ena}} \), it takes \( 2(n - 1) \)

![Figure 7: The observed WCL of SS, NSS and P.](image)
slots for the core caching cache lines in set
LLC(X) to write back a cache line and free an entry as a core performs (n − 1) write-backs in the worst-case, and the evicted cache line is written-back last. Note that each such slot accounts for one period, which is N · SW. Finally, casl requires one slot SW to receive its response, which accounts for another period.

5 EVALUATION

Our empirical evaluation is performed with an in-house trace simulator that simulates the cache subsystem of a four-core system with the memory hierarchy as described in section 3. The L2 cache is a 4-way set-associative cache with 16 sets and the L3 cache is a 16-way set-associative cache with 32 sets that can be partitioned across the four cores. The cache line size is 64-byte.

Workload generation. We use synthetic workloads consisting of memory requests to random addresses within various address ranges. We enforce disjoint address ranges for each core to guarantee that accesses to shared data does not occur. For a certain address range, a core issues the same memory addresses across different partitioned configurations.

Notation. We use the following syntax to express partitioned configurations. (1) SS(s, w, n): a partition shared among n cores with s sets and w ways with set sequencer, (2) NSS(s, w, n): a partition shared among n cores with s sets and w ways and LLC services contending requests with best effort, and (3) P(s, w): a partition with s sets and w ways that is uniquely occupied by a core. For P(s, w), each core is assigned equally-sized partition.

5.1 Worst-case latency

Workload setup. To exercise the worst-case, we enforce a partition size of one set for all configurations. This is done to force as many conflicts as possible.

Results. Figure 7 confirms that the observed WCL of all configurations are within the analytical WCLs, which are 5000 cycles for SS, 979250 cycles for NSS, and 450 cycles for P. Although a distinct partition P yields the lowest WCL, recall that we wish to share partitions for cores whose real-time requirements are met with sharing. However, there might be others that need distinct partitions P, which do indeed provide the lowest WCL. This is essential when the number of required functionalities deployed onto a single multicore increases. In the case of cores sharing a partition, the bound for SS can be employed. NSS shows a higher observed WCL compared to SS across all address ranges because distance can increase as mentioned in Observation 3.

5.2 Partition sharing and utilization

We next investigate the the impact of partitioning when cores are forced to share a partition.

Workload setup. We conduct the experiment with 2-core and 4-core setups, each with a fixed cache capacity that is then partitioned. In SS and NSS, all cores share the same partition while in P, the fixed cache capacity is divided equally between all cores, and the set-associativity is fixed. Figure 8a shows that when the address range is 1024-byte or 2048-byte, the execution time is the same across SS, NSS and P. This is because the address range is less than or equal to the partition size.

When the address range exceeds the partition size, SS exhibits improved performance when compared to both NSS and P. In the 2-core setup with 4096-byte of partition size, SS achieves an average speedup of 1.34× as is shown in Figure 8a. When the capacity is 8192-byte, SS achieves an average speedup of 2.13× (Figure 8b). Such performance persists in the 4-core setup where SS features an average speedup of 1.10× for 4096-byte partition size (Figure 8c) and an average speedup of 1.02× for 8192-byte partition size (Figure 8d).

6 CONCLUSION

This paper provides a complementary approach to strictly partitioning the LLC where cores can share LLC partitions. We expect sharing of partitions to be important as the demands for consolidating a large number of safety-critical functionalities onto a single multicore are accelerating. Using a constrained TDM policy, multiple cores can predictably share the LLC. However, the resultant WCL is grossly pessimistic. We introduced the set sequencer hardware structure that reduced the WCL by 2048 times, and empirically evaluated that the WCL bounds hold.

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