ABSTRACT  This paper proposes the circuit structure, topological family and energy management control strategy (EMCS) of a Buck type multi-input distributed generation system (DGS) with parallel-timesharing power supply. Also, the power supply modes (PSMs) and their smooth transition, as well as the control loops and multiple duty cycles expression are studied. The circuit structure is composed of a Buck type single-stage multi-input inverter and a single-stage isolated battery charging/discharging converter, with their outputs parallel-connected on the AC side. The topological family includes full-bridge etc. 3 types of circuit. By comparing the load power and the total generated multi-input sources power, the proposed EMCS achieves real-time control of charging/discharging converter’s power flow and the system’s smooth transition among different PSMs. The proposed “variable inductances equivalent method” regards the output filter inductor as the parallel connection of two virtual inductances, based on which the small signal model of multi-input inverter is established and the corresponding control loops are designed. Experimental results of a 3kVA laboratory prototype have shown that the proposed circuit topology has a good performance of high conversion efficiency, low distortion of output voltage, and galvanic isolation among load, multi-input sources and battery, etc.

INDEX TERMS  Buck type, distributed generation system (DGS), multi-input, energy management control strategy (EMCS), parallel-timesharing power supply.

I. INTRODUCTION  Due to the increasing shortage of traditional fossil energy, new energies such as photovoltaic (PV) cells, wind power possess a high level of penetration as they are clean, pollution-free and abundant. However, the periodic nature of the generated power and the intermittent characteristics of single new energy introduce adverse impacts on the power system performance [1]–[3]. In order to become independent as much as possible from these impacts, and improve the stability of new energy power generation system, the DGSs that combines multiple new energies have been implemented [4]–[8].

A two-stage multiple single-input DC-DC converters type DGS was proposed in [9]–[11], which was constructed by multiple single-input DC-DC converters and a cascaded Buck type inverter. The outputs of the single-input DC-DC converters were connected in serial or in parallel. This kind of DGS has deficiencies of two-stage power conversion, bulky size and high cost.

When replacing the multiple single-input DC-DC converters with one multi-input DC-DC converter, the two-stage multi-input DC-DC converter type DGS was formed in [12]–[18]. A two-stage integrated Boost/dual half-bridge DC-DC converter type DGS was presented in [12]. The two input sources of PV and wind power adopted MPPT control. The battery was current-limited charged during grid-connected operation, and complemented the load power or absorbed the surplus power during island operation. This DGS was single-stage power conversion when the battery was charged but three-stage conversion when discharged. Also, control of the system was complicated and not available to extend to n-sources. A two-stage combined Buck/Boost multi-input DC-DC converter type DGS was discussed in [13]. The PV and wind power adopted MPPT control, and Buck inverter adopted DC bus voltage outer loop, grid-connected current inner loop control. A two-stage combined Buck/Boost/Buck-Boost multi-input DC-DC converter type
DGS was presented in [14], in which the multi-input DC-DC converter can operate in Buck, Boost, and Buck-Boost modes. However, the EMCS of the system was not mentioned. A two-stage LCC resonant multi-input DC-DC converter type DGS was proposed in [15]. The multi-input DC-DC converter was composed of multiple LCC resonant charger units and a DC filter. The charger units were connected in serial on the secondary side of high-frequency (HF) transformer, yet the EMCS of the system was not discussed either. The DGSs in [13]–[15] have the features of multi-input sources supplying power at the same time, a wide range of duty cycle adjustment, but requiring multiple free-wheeling diodes, and hard to extend to n-sources. A two-stage multi-winding Boost DC-DC converter type DGS was proposed in [16]. The former stage adopted the maximum power phase-shift PWM control strategy, and the latter stage used the DC bus voltage outer loop, grid-connected current inner loop unipolar SPWM control strategy. A two-stage multi-winding Buck DC-DC converter type DGS was presented in [17], in which the former stage adopted PWM phase-shift control strategy, but the EMCS of the system was not discussed. All the inputs and output in [16], [17] were HF isolated, and could supply power simultaneously or in timesharing. However, there were too many power switches in the circuits, and both the HF transformer’s structure and control strategy were complicated. A two-stage Buck-Boost multi-input DC-DC converter type DGS was proposed in [18]. The fuel cell adopted peak current control to achieve constant output current, and the wind power was controlled by DC bus voltage regulation. It has simple circuit structure and control strategy, low voltage stress over power switches, well integrated and easy to extend to n-sources, despite of a small range of duty cycle adjustment.

In conclusion, two-stage multi-input DC-DC converter type DGS simplifies the circuit structure and reduces the cost. However, it still has a two-stage circuit structure, thus the conversion efficiency and power density are not satisfactory. Besides, when a battery charging/discharging converter is connected with the DC bus, it is two-stage power conversion whether the battery is charged by multi-input sources or discharges to the AC load. Consequently, the conversion efficiency is still not ideal.

In order to further simplify the circuit structure and reduce power conversion stage, it is necessary to seek a multi-input inverter with a single-stage circuit structure and its DGS. This paper proposes the circuit structure, topological family and EMCS of a Buck type multi-input DGS with parallel-timesharing power supply. Theoretical analysis and experimental results indicate that the proposed multi-input DGS possesses some distinct advantages as follows.

(i) The multi-input inverter directly converts the total multi-input sources power into LF alternating current, exhibiting a simple circuit structure.

(ii) Single-stage power conversion during battery discharge, and single-stage or two-stage conversion during battery charge, which is favorable for conversion efficiency.

(iii) The proposed EMCS achieves real-time control of charging/discharging converter’s power flow and the stability of output voltage as well as smooth transition among different PSMs.

(iv) The proposed \( L_f-C_f \) parallel-resonant circuit effectively suppresses the low-frequency current ripple on battery side, which is favorable for interfacing the battery and its single-stage converter.

(v) Galvanic isolation between any two of the load, multi-input sources and battery.

The rest of this paper is organized as follows: Section II illustrates the circuit structure and topological family. The EMCS, PSMs of the proposed DGS and the mechanism of their smooth transition are elaborated in Section III. Section IV sheds light on the design of the system’s control loops. Analysis on key issues, e.g., derivation of multiple duty cycles expression, is given in Section V. Section VI depicts the prototype experimental verification of the proposed DGS and its EMCS, followed by the drawn conclusion in Section VII.

II. CIRCUIT STRUCTURE AND TOPOLOGICAL FAMILY

The circuit structure and topological family of the proposed Buck type multi-input DGS are shown in Fig. 1. The DGS is composed of a Buck type single-stage multi-input inverter with external parallel-timesharing selection switches and a single-stage isolated battery charging/discharging converter, with their outputs connected in parallel on the AC side.

The multi-input inverter is cascaded by the input filter capacitors \( C_{i1} \sim C_{in} \), the external parallel-timesharing bi-directional selection switches \( S_{s1} \sim S_{sn} \), HF inverting bridge, output filter inductor \( L_{f1} \), line-frequency (LF) transformer \( T_1 \) and output filter capacitor \( C_f \). “Timesharing” denotes that each parallel-connected input source separately delivers energy through its selection switch \( (S_{s1} \sim S_{sn}) \) at a time during a single high-frequency switching period. Using four quadrant switches \( S_{s1} \sim S_{sn} \) could prevent the short circuit among different inputs, because \( S_{s1} \sim S_{sn} \) conduct in timesharing, there’s no current flow path between any inputs. The \( L_f-C_f \) parallel-resonant circuit is designed to suppress the low-frequency current ripple on the battery side.

For half-bridge topologies shown in Fig. 1(c), the multi-input sources voltage are imposed in timesharing on the bridge-arm capacitors \( C_1, C_2 \) in a HF switching period, thus the sources voltage should be approximately the same, which restricts the practicability to a great extent. However, for push-pull and full-bridge topologies shown in Fig. 1(b), (d), the input sources voltage allows differences. Variation in input sources voltage reflects on the voltage across its own capacitor \( C_{i1} \sim C_{in} \) and the rising slope of inductor current \( i_{L1} \). Compared the proposed DGS with the entire two-stage parallel-timesharing multi-input DC-DC converter type DGS in [18], the proposed DGS has less power switches and only one filter inductor.

The connection of the HF transformer \( T_2 \)’s secondary winding and cycloconverter is adjusted from the collectors of
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It can be seen that the proposed DGS has the following features: (1) the multi-input inverter directly converts the total multi-input sources power into LF alternating current, exhibiting a simple circuit structure; (2) single-stage power conversion during battery discharge, single-stage or two-stage conversion during battery charge, and small low-frequency current ripple on battery side; (3) galvanic isolation among AC load, multi-input sources and battery; (4) the primary leakage inductance of transformer $T_1$ can be used as the filter inductor for half-bridge and full-bridge circuits in Fig. 1(c), (d).

III. EMCS OF PROPOSED DGS

A. MAXIMUM POWER EMCS

Major concerns of EMCS for DGSs are: (1) energy management of multi-input sources; (2) MPPT control of new energy equipment such as PV, wind power and (3) stability of output voltage. Take full-bridge topology shown in Fig.1(d) and PV, wind power two inputs as an example (the same below), the maximum power EMCS with analogous-rectifying unipolar phase shift of the proposed DGS is illustrated in Fig. 2.

The single-stage multi-input inverter employs maximum power energy management SPWM control strategy, which consists of PV, wind power MPPT voltage outer loops and inductor current inner loops. By sampling the voltage and current of the two input sources, the MPP voltage $U_{i1}^*$ and $U_{i2}^*$ can be obtained through MPPT algorithm. $I_{1r}$, $I_{2r}$, as the product of PV, wind power MPPT voltage outer loop signals $I_{1r}$, $I_{2r}$ and AC voltage synchronous signal $\sin(\omega t)$, are the references of each inductor current inner loop, and $I_{1r}I_{1r}/(I_{1r} + I_{2r})$, $I_{2r}I_{2r}/(I_{1r} + I_{2r})$ are the corresponding feedback signals of inductor current. Their error amplifying signals and the output voltage feedforward subjects $u_0U_{clm}N_{11}/[N_{12}U_{i1}(1 + I_{2r}/I_{1r})]$, $u_0U_{clm}N_{11}/[N_{12}U_{i2}(1 + I_{1r}/I_{2r})]$ are respectively summed up to obtain the driving signals of $S_{s1} \sim S_{s2}$ and $S_1 \sim S_4$.

As is shown in Fig. 2(a), driving signal of $S_{s1}$ is obtained right from its regulated signal $i_{e1}$. However, as the two inputs are parallel-connected, driving signal of $S_{s2}$ cannot be obtained right from $i_{e2}$ as to prevent short-circuit case between the two inputs. Regulated signals $i_{e1}$ and $i_{e2}$ are summed up by a summator to generate the total duty cycle of two inputs. By deducing the duty cycle of $S_{s1}$, driving signal of $S_{s2}$ is obtained. Therefore, $S_{s2}$ is turned on only after $S_{s1}$ turned off, and the two inputs supply power in a parallel-timesharing way in a HF switching period, as shown from waveforms of $S_{s1}$ and $S_{s2}$ in Fig. 2(b).

It should be noted that as the two inputs are parallel-connected through $S_{s1}$, $S_{s2}$, a dead-time interval is mandatory link in other multi-input converters, this paper proposes an AC link topology which incorporates the new energy sources and a battery. Therefore, the input sources intermittency could be taken care of by the battery through charging/discharging converter, and the output voltage of the system is maintained stable.
between $S_{s1}$ and $S_{s2}$. Nevertheless, it arises a turnoff voltage spike over selection switches because of no feedback path for $i_{L1}$ while $u_{o}\cdot i_{L1} < 0$. In order to restrain the voltage spike, drive signals of $S_{s12}$, $S_{s22}$ need to be adjusted from the original ones which is the same as $S_{s11}$, $S_{s21}$ respectively to the reversed signals of $S_{s21}$, $S_{s11}$, respectively, so that an overlap time between $S_{s12}$ and $S_{s22}$ is generated. As the feedback path is ensured, the turnoff voltage spike is intrinsically restrained. The battery charging/discharging converter adopts analogous-rectifying unipolar phase-shifted control strategy. It implies that (1) a phase-shifted angle $\delta$ between the right and left bridge legs of HF inverting bridge, and the front-end voltage of the output filter $u_{EF}$ is an unipolar SPWM wave; (2) during the positive half cycle of output voltage, $S_{b6}$ ($S'_{b6}$) and $S_{b7}$ ($S'_{b7}$) are turned on, the rectification circuit composed of $S_{b5}$ ($S'_{b5}$) and $S_{b8}$ ($S'_{b8}$) rectifies the secondary side voltage $u_{CD}$ into positive half cycle SPWM wave, while during the negative half cycle, $S_{b5}$ ($S'_{b5}$) and $S_{b8}$ ($S'_{b8}$) are turned on, the rectification circuit composed of $S_{b6}$ ($S'_{b6}$) and $S_{b7}$ ($S'_{b7}$) rectifies $u_{CD}$ into negative half cycle SPWM wave, therefore it is called analogous-rectifying control. By adding an overlap time to rectification power switches, energy could be backward transferred to the battery side.

Features of the proposed EMCS are: (1) direct control of $i_{L1}$ is realized by decomposing $i_{L1}$; (2) the cycloconverter switches are ON in half cycle and zero-voltage turnoff HF operation in another half cycle, hence reduces the switching losses; (3) soft commutation of leakage inductance and filter inductor current is realized without judging the polarity of $i_{L2}$.

B. PSMs

Comparing the load power $P_o$ and the total input power $P_{1max} + P_{2max}$, the proposed DGS has three PSMs.

Mode I: $P_{1max} + P_{2max} > P_o$, two inputs supply the load and battery simultaneously, and the system is equivalent to a single-stage multi-input inverter and a single-stage
Boost-type HF rectifier, with the battery output power $P_o - (P_{1\text{max}} + P_{2\text{max}}) < 0$.

Mode II: $P_{1\text{max}} + P_{2\text{max}} < P_o$, two inputs and the battery supply the load at the same time, while the system is equivalent to a single-stage multi-input inverter and a single-stage Buck-type HF inverter parallel-connected in their outputs, with the battery output power $P_o - (P_{1\text{max}} + P_{2\text{max}}) > 0$.

Mode III: $P_{1\text{max}} + P_{2\text{max}} = P_o$, the two inputs only supply power to the load, while the battery output power is 0 (the charging/discharging converter operating in no-load condition). However, in the extreme case while neither the 1st nor the 2nd input supplies power, that is, $P_{1\text{max}} + P_{2\text{max}} = 0$, the load power is totally provided by the battery, which is an exceptional case of Mode II.

Usually, the capacities of multi-input sources, battery and load are configured in a certain proportion. In the proposed DGS, the capacities of multi-input sources, battery and load are configured equally to verify the maximum power EMCS. Therefore, the PV cells and wind generator normally work at their MPPs. On the other hand, when adding battery voltage loops to the MPPT voltage outer loops of PV and wind generator, making PV or wind generator not work at their MPPs, overcharge of battery can be avoided.

### C. MECHANISM OF SMOOTH TRANSITION AMONG DIFFERENT PSMs

For output filter capacitor $C_f$ and load $Z_o$, the parallel connect of multi-input inverter and charging/discharging converter is equivalent to the parallel superposition of two current sources. From Fig. 2 (a) the EMCS indicates that inductor current $i_{L1}$ (or $i_{N12}/N_{12}/N_{11}$) is in phase with output voltage $u_o$, providing the active power; the phase difference $\theta$ between charging/discharging converter’s inductor current $i_{L1}$ and $u_o$ differs by the amount and direction of active power for the converter. In this regard, the phasor diagram of output fundamental component on AC side under three PSMs and different load properties, can therefore be drawn in Table 1, where $\phi$ is the power factor angle of the load.

When $P_{1\text{max}} + P_{2\text{max}} = P_o$, namely, $I_{N12} = I_o\cos\phi$, the phase difference $|\theta| = 90^\circ$, and the active power of charging/discharging converter is 0, thus the battery output power $P_b = 0$ (no-load condition)–Mode III. When the load power increases, making $P_{1\text{max}} + P_{2\text{max}} < P_o$, that is, $I_{N12} < I_o\cos\phi$, $u_o$ decreases and the phase-shifted angle $\delta$ decreases too, while the phase difference spontaneously adjusts to $0 < |\theta| < 90^\circ$; the charging/discharging converter delivers active power, thus battery complements the load power at $P_b = P_o - (P_{1\text{max}} + P_{2\text{max}}) > 0$–Mode II. When the load power decreases, making $P_{1\text{max}} + P_{2\text{max}} > P_o$, that is, $I_{N12} > I_o\cos\phi$, $u_o$ increases and the phase-shifted angle $\delta$ increases too, while the phase difference becomes $90^\circ < |\theta| < 180^\circ$; the charging/discharging converter absorbs active power, thus surplus power from the 1st and 2nd input charges the battery at $P_b = P_o - (P_{1\text{max}} + P_{2\text{max}}) < 0$–Mode I. Hence, by comparing the load power $P_o$ and the total generated multi-input sources power $P_{1\text{max}} + P_{2\text{max}}$, the proposed EMCS achieves real-time control of charging/discharging converter’s power flow and stability of output voltage, as well as the smooth transition among different PSMs.

### IV. DESIGN OF CONTROL LOOPS

The output voltage of the proposed DGS is regulated stable by the battery charging/discharging converter, which can be metaphorically regarded as a “grid-connected voltage” for the single-stage multi-input inverter. Therefore, the control loops include 2 current loops for the multi-input inverter and a voltage loop for the charging/discharging converter, which are independent of each other and therefore can be designed.
separately. This section focuses on the analysis of the current loops design.

**A. VARIABLE INDUCTANCES EQUIVALENT METHOD AND SMALL SIGNAL MODELING**

Since the two input sources share a common output filter inductor $L_{f1}$, it can be equivalent to the parallel connection of two inductances $L_{f11}$ and $L_{f12}$. Consequently, $i_{f11}$ can be regarded as the sum of corresponding inductor current $i_{f11}$ for 1st input source power and $i_{f12}$ for 2nd source power, as shown in Fig. 3.

![Figure 3: The proposed “variable inductances equivalent method.”](image)

\[
\begin{align*}
L_{f11} \text{ and } L_{f12} \text{ fulfill} \\
\begin{cases}
L_{f11} \cdot L_{f12} & = L_{f1} \\
L_{f11} + L_{f12} & = L_{f1} \\
i_{f1} & = i_{f11} + i_{f12} \\
i_{f11} & = i_{f1} \\
i_{f12} & = i_{f1} \\
1 & = i_{f1} \\
L_{f11} & = L_{f1} \\
L_{f12} & = L_{f1}
\end{cases}
\]

\[\text{(1)}\]

\[\text{(2)}\]

$I_{f1}$, $I_{f2}$ are the MPPT voltage outer loop signals of PV, wind power, respectively.

Therefore $L_{f11}$ and $L_{f12}$ can be derived as

\[
\begin{align*}
L_{f11} & = \frac{i_{f1} + i_{f2}}{i_{f1}} \\
L_{f12} & = \frac{i_{f1} + i_{f2}}{i_{f2}} \\
L_{f11} \text{, } L_{f12} & \text{ changes with the value of } I_{f1} \text{ and } I_{f2}, \text{ hence it is called “variable inductances equivalent method”}. \text{ When only the 1st input source works, } I_{f2} = 0, L_{f11} = L_{f1}, L_{f12} = \infty; \text{ when only the 2nd input source works, } I_{f1} = 0, L_{f12} = L_{f1}, \text{ and } L_{f11} = \infty.
\end{align*}
\]

Combining the “variable inductances equivalent method” and the “state-space average method” to obtain the small signal model of three working cases for multi-input inverter, as shown in Fig. 4. $G_{cel1}(s)$ and $G_{cel2}(s)$ are the compensation functions of two current loops, $G_{op}(s) = k_p1 + k_i/s (j = 1, 2); G_{PWM}(s)$ is the transfer function of PWM comparator, $G_{PWM}(s) = 1/[(T_5s + 1) \cdot U_{clim}]; U_{clim}$ is the amplitude of sawtooth wave $u_{cl1}; G_{i1}(s), G_{i2}(s), G_{i12}(s), G_{i122}(s)$ are the control-output transfer functions, $G_{i1}(s) = U_{cl1}(sL_{f11} + r_1), G_{i2}(s) = U_{cl2}(sL_{f12} + r_2), G_{i12}(s) = U_{cl1}(sL_{f112} + r_1), G_{i122}(s) = U_{cl2}(sL_{f122} + r_2); r_1, r_2$ are the equivalent serial resistance of $L_{f11}, L_{f12}$.

When the two input sources jointly work, variations of $\hat{d}_1(s), \hat{d}_2(s)$ affect $\hat{i}_{f11}(s), \hat{i}_{f12}(s)$ due to $G_{i12}(s), G_{i21}(s)$. In other words, single-stage multiple-input inverter is a strong coupling multiple-input multiple-output control system, thus the current regulator design in control loops is complicated. However, when only the 1st or 2nd input source works, there’s only one current loop for the inverter, in this case $L_{f11} = L_{f12} = L_{f1}$.

![Figure 4: Small signal model of three working cases for multi-input inverter: (a) Two input sources jointly work, (b) Only the 1st input source works, (c) Only the 2nd input source works.](image)

**B. CURRENT REGULATORS DESIGN**

From the small signal model shown in Fig. 4(b), the loop gain when only the 1st input source works is:

\[
H_{i1}(s) = G_{cel1}(s) \cdot G_{PWM}(s) \cdot G_{i1}(s) = \frac{U_{cl1}(k_p1 + k_i/s)}{U_{clim}(T_5s + 1) (sL_{f1} + r_1)}
\]

(3)

From Fig. 4(c), the loop gain when only the 2nd input source works is:

\[
H_{i2}(s) = G_{cel2}(s) \cdot G_{PWM}(s) \cdot G_{i2}(s) = \frac{U_{cl1}(k_p2 + k_i2/s)}{U_{clim}(T_5s + 1) (sL_{f2} + r_2)}
\]

(4)

When the two input sources jointly work, $\hat{i}_{f12}(s)$ in Fig. 4(a) is considered “0” to derive the 1st current loop gain. Therefore, the 1st current loop gain under two input sources joint work is

\[
H_{i1}(s) = H_{i1 \cdot 1}(s) + H_{i1 \cdot 2}(s) = G_{cel1}(s) \cdot G_{PWM}(s) \cdot \left( \frac{G_{i1}(s) - G_{i2}(s) \cdot G_{cel2}(s) \cdot G_{PWM}(s) \cdot G_{i12}(s)}{1 + G_{cel2}(s) \cdot G_{PWM}(s) \cdot G_{i12}(s)} \right) + G_{cel1}(s) \cdot G_{PWM}(s) \cdot \left( \frac{G_{i1}(s) + G_{i2}(s) \cdot G_{cel2}(s)}{G_{cel1}(s) \cdot G_{i12}(s)} \right) \cdot G_{i12}(s) + G_{i21}(s)
\]

and the 2nd current loop gain under two input sources joint work can be deduced as

\[
H_{i2}(s) = H_{i2 \cdot 2}(s) + H_{i2 \cdot 1}(s)
\]
If the parameters of the two current regulators from (3), (4) are taken into (5), (6), and the two current loop gains meet the stability and rapidity requirements, then the design process is completed; otherwise, the parameters of the two current regulators need to be readjusted and substituted into (5) and (6) to verify the stability and rapidity again. Here, it is considered that when the phase margin of the loop gain is higher than 45° and the cut-off frequency $f_c$ satisfies $f_c/20 < f_c < f_c/5$, the system meets the stability and rapidity requirements.

Switching frequency of multi-input inverter $f_s = 30$ kHz, take $f_c = 3$ kHz as the cut-off frequency of the current loop. Other parameters are: $U_{i1} = 288$ V, $U_{i2} = 250$ V, $U_{clm} = 2499$, $L_{f1} = 1.0$ mH, $r_1 = r_2 = 0.01$ $\Omega$, $P_1; P_2 \approx 1.4:1$, so $L_{i11} = 1.714$ mH, $L_{i12} = 2.4$ mH. Substituting $k_{p1} = 150$, $k_{i1} = 300$, $k_{i2} = 170$, $k_{i2} = 300$ into (5) and (6), the frequency characteristics of the two current loop gains under two input sources joint work can be drawn in Fig. 5.

It can be seen from Fig. 5 that the cut-off frequency of the $1^{st}$ current loop gain is 3.85 kHz, the amplitude at 50 Hz is 52.3 dB and the phase margin is 49.7°; for the $2^{nd}$ current loop gain, the cut-off frequency is 3.85 kHz, the amplitude at 50 Hz is 53.4 dB and the phase margin is 50.1°. Therefore, the design of the two current regulators meets the stability and rapidity requirements under three working cases.

$$u_o = \frac{N_{i2}}{N_{i1}} (d_1 U_{i1} + d_2 U_{i2})$$

(7)

**FIGURE 5.** Frequency characteristics of the two current loop gains under two input sources joint work.

**V. ANALYSIS ON KEY ISSUES**

**A. DERIVATION OF MULTIPLE DUTY CYCLES EXPRESSION**

The output AC voltage can be described as

$$u_o = \frac{N_{i2}}{N_{i1}} d_1 U_{i1} + \frac{N_{i2}}{N_{i1}} d_2 U_{i2}$$

(8)

where $d_1$, $d_2$ are the multiple duty cycles of multi-input inverter, $d_0$ is the duty cycle of the charging/discharging converter. Assuming that $L_{f1}$ is large enough, current ripple of $i_{f1}$ can be neglected. The average value of inductor current $i_{f1}$ in a HF switching period $T_s$ is $I_{f1avg}$; the average values of each inner current loop reference for the $1^{st}$ and $2^{nd}$ input sources are $I_{avg1}$, $I_{avg2}$, respectively; $u_0$ can be regarded as a constant value $U_{oavg}$ in a switching period. Therefore, in a $T_s$, the average output power of $1^{st}$, $2^{nd}$ input and the primary-winding port of $T_1$ is

$$P_{avg1} = \frac{N_{i1}}{N_{i2}} U_{oavg} I_{avg1} \approx \frac{d_1}{N_{i1}} U_{i1} I_{f1avg}$$

(9)

$$P_{avg2} = \frac{N_{i1}}{N_{i2}} U_{oavg} I_{avg2} \approx \frac{d_2}{N_{i1}} U_{i2} I_{f1avg}$$

(10)

$$P_{avg1} + P_{avg2} = \frac{N_{i1}}{N_{i2}} U_{oavg} I_{f1avg}$$

(11)

From power balance and (9)-(11), there is

$$I_{f1avg} = I_{avg1} + I_{avg2}$$

(12)

d_1, d_2 can be derived from (7), (9), (10) as:

$$d_1 \approx \frac{N_{i1}}{N_{i2}} \frac{U_{oavg}}{U_{i1}} \left[ U_{i1} \left( 1 + \frac{I_{avg1}}{I_{f1avg}} \right) \right]$$

(13)

$$d_2 \approx \frac{N_{i1}}{N_{i2}} \frac{U_{oavg}}{U_{i2}} \left[ U_{i2} \left( 1 + \frac{I_{avg2}}{I_{f1avg}} \right) \right]$$

(14)

Taking $d_1$ and $d_2$ in (14) as the feedforward subjects in respective current loops, to ensure that $I_{f1}/I_{f2} = P_1/P_2$ ($P_1$ and $P_2$ are the average power in a line cycle of the $1^{st}$ and $2^{nd}$ input, respectively).

**B. LOW-FREQUENCY CURRENT RIPPLE SUPPRESSION**

The $L_f C_f$ parallel-resonant circuit is added to suppress the low-frequency current ripple on battery side. Assuming that the conversion efficiency of charging/discharging converter is $\eta$, the voltage variation across $C_b$ is

$$\Delta U_{Cb} = 2 \cdot I_{DC} \cdot \frac{1}{2 \eta C_b} \cdot U_0 I_o = \eta U_o \cdot \frac{1}{\omega C_b}$$

(15)

From (15) we obtain

$$C_b = \frac{U_0 I_o}{\eta \omega U_b \Delta U_{Cb}}$$

(16)

and the voltage variation is taken $\Delta U_{Cb} = 10\% U_b$.

The voltage across $C_f$

$$U_{Cf} = \frac{1}{2} \Delta U_{Cb} \cdot U_0 I_o = \frac{1}{2 \eta U_b} \cdot 1 \omega C_b = 5\% U_b$$

(17)
and the current through $L_r$

$$I_{L_r} = I_b + U_{C_r} \cdot 2\omega C_r = \frac{U_o I_o}{\eta U_b} + \frac{U_o I_o}{2\eta U_b} \cdot 2\omega C_r$$

$$= \frac{U_o I_o}{\eta U_b} \left(1 + \frac{C_r}{C_b}\right)$$

(18)

In addition, $L_r$, $C_r$ is restricted by

$$f_t = \frac{1}{2\pi \sqrt{L_r C_r}} = \frac{2\omega}{2\pi} = 100\text{Hz}$$

(19)

VI. EXPERIMENTAL VERIFICATION

Taking full-bridge topology in Fig.1(d) as an example, to verify the effectiveness of the proposed circuit topology and EMCS. Key parameters are listed as follows: rated capacity 3kVA, the PV and wind power in the experiment are both simulated by TopCon programmable DC power supply TC.P.16.800.400.S, which exhibits the same characteristics as PV cells; the 1st input MPP is set at (1275W/288V/4.43A) and the 2nd input MPP is set at (915W/250V/3.66A), both under room temperature 25°C and light intensity 1000W/m²; battery voltage $U_b = 96V$, output voltage $u_o = 220V/50Hz$, switching frequency $f_s = 30kHz$, input filter capacitors $C_1 = C_2 = 4000\mu F$, $C_b = 14.1mF$, resonant circuit $L_r = 1.1mH$, $C_r = 2300\mu F$, $L_d1 = 1.0mH$, $L_d2 = 1.2mH$, turns ratio $N_{11}/N_{12}$ of $T_1$ is 57/80, for $T_2$ $N_{21}/N_{22} = 9/40$, IGBT IXH50N60B3D1 for power switches $S_{s11}$ $\sim S_{s12}$ and $S_1$ $\sim S_4$, MOSFET IXXH150N20T for $S_{b1}$ $\sim S_{b4}$, IGBT IXH40N65B4H1 for $S_{b3}(S_{b3}')$ $\sim S_{b8}(S_{b8}')$, DSP TMS320F28335 for control circuit chip, and the MPPT algorithm employs open-circuit voltage and disturbance observation methods.

Steady-state experimental waveforms of the proposed topology at $U_{i1}/U_{i2} = 288V/250V$, rated resistive load and PSM II are illustrated in Fig. 6.

It can be seen that: (1) The 1st and 2nd inputs operate at their MPPs (1275W/288V/4.43A), (915W/250V/3.66A), as shown in Fig. 6(a); (2) $S_{s11}$, $S_{s21}$ conduct in timesharing, while the voltage across $S_{s11}$, $S_{s21}$ during dead time is constantly $U_{i1}$, $U_{i2}$ (as marked with arrows), as shown in Fig. 6(b); (3) $u_{AB}$ is an unipolar SPWM wave with the amplitude of $U_{i1}$, $U_{i2}$, while the slopes of $i_{L1}$ are $(U_{i1} - U_o N_{11}/N_{12})/L_{d1}$, $(U_{i2} - U_o N_{11}/N_{12})/L_{d1}$, as shown in Fig. 6(c); (4) $P_{1_{\text{max}}} + P_{2_{\text{max}}} \approx 2kW$, the battery discharges to complement the rated resistive load power with the phase difference $\theta \approx 3^\circ$ and the total harmonic distortion (THD) of $u_o$ is 1.08%, as shown in Fig. 6(d).

Steady-state experimental waveforms of the charging/discharging converter at $U_{i1}/U_{i2} = 288V/250V$, rated resistive load and PSM II are illustrated in Fig. 7. It can be seen that: (1) $L_r - C_r$ parallel-resonant circuit effectively suppresses the low-frequency current ripple on battery side, as shown in Fig. 7(a), (b); (2) both the leading and lagging leg switches $S_{b3}$ and $S_{b4}$ achieve zero voltage switching (ZVS) turn-on, as shown in Fig. 7(c); (3) the cycloconverter switches work at half cycle HF square wave and half cycle high level, and also achieve ZVS turn-off, as shown in Fig. 7(d).

FIGURE 6. Steady-state experimental waveforms of the proposed topology at $U_{i1}/U_{i2} = 288V/250V$, rated resistive load and PSM II: (a) 1st and 2nd input voltage, current, (b) GE, CE voltage of $S_{s11}$, $S_{s21}$, (c) front-end voltage $u_{AB}$, current $i_{L1}$, (d) Mode II ($\cos\theta = 1$).

Steady-state experimental waveforms of the proposed topology at $U_{i1}/U_{i2} = 288V/250V$, different load properties and PSMs are depicted in Fig. 8.

In Fig. 8(a), $P_{1_{\text{max}}} + P_{2_{\text{max}}} \approx 2kW$, inductive load power $P_{S} \approx 1kVA$, the surplus power charges the battery with the phase difference $90^\circ < |\theta| < 180^\circ$ and the system operates in Mode I; in Fig. 8(b), $P_{1_{\text{max}}} + P_{2_{\text{max}}} \approx 2.25kW$, capacitive load power $P_{S} \approx 3kVA$, and battery output power $P_{b} \approx 0$ with the phase difference $|\theta| \approx 90^\circ$, the system operates in Mode III; Fig. 8(c) shows the 1st, 2nd inputs and battery supplying the rectifier type load at the same time.
Fig. 9 depicts the different modes switching waveforms under load power and light intensity change. In Fig. 9 (a), the 1st and 2nd inputs work at MPPs (1275W/288V/4.43A), (915W/250V/3.66A) throughout the operation, $P_o$ in Stage 1, 3 is 1kW while in Stage 2 is changed to 3kW. During Stage 1, 3, $P_{1\text{max}} + P_{2\text{max}} > P_o$, $i_b < 0$, the system works in Mode I; during Stage 2, the light intensity of two inputs suddenly drops to 500W/m$^2$, resulting in $P_{1\text{max}} + P_{2\text{max}} = P_o$, $i_b = 0$, the system switches to Mode III; during Stage 3, the light intensity decreases to zero and the two inputs stop working; $I_{i1}$, $I_{i2}$ decreases to 0 and $U_{i1}$, $U_{i2}$ rapidly rise to their respective open-circuit voltage, resulting in $P_{1\text{max}} + P_{2\text{max}} < P_o$, $i_b > 0$, the system switches to Mode II. Therefore, the proposed DGS exhibits smooth transition among different PSMs under sudden change of load power and light intensity.

The conversion efficiencies of the proposed single-stage multi-input inverter and its DGS are shown in Fig. 10, wherein the efficiency of transformer $T_1$ at 3kVA is 97.2%. In Fig. 10(a), switching loss and core loss of $T_1$ and $L_{f1}$ possess a high proportion, resulting in a lower efficiency under light load; while under heavy load, the conduction loss 1000W/m$^2$ are (1275W/288V/4.43A), (915W/250V/3.66A), while $P_o$ keeps constant in 1kW. During Stage 1, $P_{1\text{max}} + P_{2\text{max}} > P_o$, $i_b < 0$, the system works in Mode I; during Stage 2, the light intensity of two inputs suddenly drops to 500W/m$^2$, resulting in $P_{1\text{max}} + P_{2\text{max}} = P_o$, $i_b = 0$, the system switches to Mode III; during Stage 3, the light intensity decreases to zero and the two inputs stop working; $I_{i1}$, $I_{i2}$ decreases to 0 and $U_{i1}$, $U_{i2}$ rapidly rise to their respective open-circuit voltage, resulting in $P_{1\text{max}} + P_{2\text{max}} < P_o$, $i_b > 0$, the system switches to Mode II. Therefore, the proposed DGS exhibits smooth transition among different PSMs under sudden change of load power and light intensity.
FIGURE 9. Modes switching waveforms under load power and light intensity change; (a) Load power change, (b) Light intensity change.

and the copper loss of $T_1$ and $L_{11}$ are in proportion to the square of current RMS value, thus the conversion efficiency increases and then decreases, with an efficiency of 92.5% at full load of 3kW and a maximum efficiency 93.2% at 1.7kW. In Fig. 10(b), the full-load conversion efficiencies when $P_{1\text{max}} + P_{2\text{max}}$ is 1kW and 2kW are 91.0% and 92.4%, respectively. Conversion efficiency at $P_o = 3kW$ under $P_{1\text{max}} + P_{2\text{max}} = 2kW$ is higher than 1kW, because the inverter reaches its highest efficiency at 1.7kW, while charging/discharging converter has its highest efficiency of 92.2% at 1.3kW. In addition, resonant inductor $L_r$ on the battery side occupies copper loss too.

Compared the proposed topology with [9-18], conversion efficiency of the two-stage single-input Buck-Boost DC-DC converter type DGS described in [11] was only 81% at input voltage 18V, output voltage 30V50Hz, and output power 43.2W, THD of grid-connected current was 1.6%; in [13], THD of grid-connected current was 4.5% at input voltage 360V/120V, output voltage 110V60Hz, and rated power 1kW, with no conversion efficiency given; in [16], THD of grid-connected current was 1.32% at input voltage 48V/48V, output voltage 220V50Hz and rated power 1kW, with no conversion efficiency given either. Conversion efficiencies and THD of output waveform in other two-stage DGSs mentioned were not given, unfortunately. It is thus evident that the single-stage multi-input inverter and its DGS proposed in this paper exhibit a good performance of simple circuit structure, single-stage power conversion in discharging state, high conversion efficiency and low distortion of output voltage, galvanic isolation among AC load, multi-input sources and battery, 

FIGURE 10. Conversion efficiencies of the proposed single-stage multi-input inverter and its DGS; (a) Single-stage multi-input inverter, (b) its DGS.
which possesses a certain theoretical and applicable value in multiple new energies distributed generation occasions.

VII. CONCLUSION

The circuit structure, topological family and EMCS of a Buck type multi-input DGS with parallel-timesharing power supply have been proposed in this paper. The proposed maximum power EMCS achieves real-time control of charging/discharging converter’s power flow and the stability of output voltage as well as smooth transition among different PSMs. Also, the “variable inductance equivalent method” has been proposed to establish the small signal model of multi-input inverter and corresponding control loops. The proposed buck-boost parallel-resonant circuit effectively suppresses the low-frequency current ripple on battery side, which is favorable for interfacing the battery and its single-stage converter. These features, effectiveness, and feasibility of the proposed topology have been evaluated and verified by experimental results of a 3kVA 240-360VDC/220V50Hz AC laboratory prototype.

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