A new trench gate field stop insulated gate bipolar transistor (IGBT) with a significant reduction in Miller capacitance

1 Introduction

Insulated gate bipolar transistor (IGBT) is the key component utilized for all kinds of power switching applications in the middle voltage range, such as in automobiles, motor drive and uninterruptible power supplies (UPS) and so on [1–3]. Over the past decades, numerous studies on the improvement the performances of IGBTs, mainly including the on-state voltage drop [4–16] and turn-off loss [11–18] have been conducted. This includes the utilization of the trench gate [5] and field stop structures [19] resulting in dramatic improvement in the trade-off relationship between the on-state voltage drop and the turn-off loss. However, comparison with the planar gate structure [20, 21] shows that trench gate based structures have larger gate-collector overlap area, causing a larger gate-collector parasitic capacitance (as called Miller capacitance) and gate-collector charge, which has significant influence on the loss, size and cost of the gate driving circuit. This is despite the fact that the trench gate structure could obtain lower on-state voltage drop and much better endurance property for latch-up effect. While several research efforts have been directed towards understanding ways to improve the trade-off relationship between the on-state voltage drop and the turn-off loss, very less work has been done on understanding ways to reduce the Miller capacitance (C_{\text{gc}}) and gate-collector charge (Q_{\text{gc}}) [22–24]. A common approach to reduce the Miller capacitance is through the utilization of the split-gate [22] or shielded-gate concept [23], even though these two structures require more complex processing and structure design. Since a lower Miller capacitance value is very important for the working of IGBT devices, especially used for the motor drive application of lower switching frequency, it is necessary to reduce the IGBTs’ Miller capacitance even further. In addition, with the deep trenches and narrow mesas, these transistors can achieve excellent injection enhancement (IE) effect and a lower on-state voltage drop can be realized without incurring a penalty in the turn-off loss increase. However, a large area of the trench gate is facing the collector side, which causes the formation of a large Miller capacitance. Therefore, it is required to develop a new structure which can realize the high IE effect and the low Miller capacitance of the IGBT.

In this paper, a new IGBT device incorporated with an n-p-n structure in the gate trench is proposed to reduce the Miller capacitance as well as the gate-collector charge and the same is investigated through numerical simulation [25]. The simulation results prove that the proposed structure has a lower Miller capacitance and gate-collector charge. One feature of this proposed structure is that its structure and the associated processing are simpler than the split-gate and shielded-gate structure. The other feature is the introduction of an n-p-n structure in the gate-trench, which involves two reverse biased diodes and two series diode capacitances, resulting in the remarkable reductions of the Miller capacitance and gate-collector charge, without degrading the others electrical characteristics (threshold voltage \( V_{\text{th}} \), breakdown voltage \( B\text{V} \), on-state voltage drop and turn-off loss \( E_{\text{off}} \)).

This paper is organized in the following way. The simulation models and device parameters are described in Section 2. While Section 3 presents, discusses and analyses the simulation results. A final conclusion is made and discussed in the Section 4.

2 Description of device parameters and simulation models

A schematic cross-section of the simulated device structures have been presented in Figure 1, where in the proposed structure has an n-p-n configuration in the gate trench (nnp-FS-TIGBT) and Figure 1(b) depicts the conventional structure (C-FS-TIGBT). The only structural difference between the nnp-FS-TIGBT and the C-TS-TIGBT is whether an npn structure exists in the gate trench or not. For the sake of simplicity, the all structural parameters are kept as same except the parameter of the gate. The thickness of the gate oxide is 100 nm and for the C-FS-TIGBT an n-type poly-silicon, with a doping of \( 1 \times 10^{19} \) cm\(^{-3} \) has been used. The gate of the nnp-FS-TIGBT is composed by an n-poly1, p-poly and n-poly2 layers, in which the dopant concentration of n-poly1, p-poly and n-poly2 are \( 1 \times 10^{19} \), \( 1 \times 10^{16} \) and \( 1 \times 10^{14} \) cm\(^{-3} \), respectively. The other structural parameters of the simulated devices are presented in Table 1.

A possible fabrication process for the n-p-n poly gate structure is depicted in Figure 2. This demonstrates the feasibility of the proposed structure in terms of fabrication, a probable...
TABLE 1 Structural parameter for the simulated devices

| Structural parameters                  | npn-FS-TIGBT | C-FS-TIGBT |
|---------------------------------------|--------------|------------|
| Concentration of P⁺ contact region    | 1.0 X 10¹⁰ cm⁻³ | 1.0 X 10¹⁰ cm⁻³ |
| Thickness of P⁺ contact region        | 0.5 μm       | 0.5 μm     |
| Concentration of N⁺ source region     | 2.0 X 10¹⁰ cm⁻³ | 2.0 X 10¹⁰ cm⁻³ |
| Concentration of N-drift              | 2.3 X 10¹⁳ cm⁻³ | 2.3 X 10¹³ cm⁻³ |
| Thickness of N⁺ buffer                | 2.0 μm       | 2.0 μm     |
| Concentration of N⁺ buffer            | 2.0 X 10¹⁶ cm⁻³ | 2.0 X 10¹⁶ cm⁻³ |
| Thickness of P⁺ collector              | 0.3 μm       | 0.3 μm     |
| Gauss peak concentration of P⁺ collector | 1.0 X 10¹⁸ cm⁻³ | 1.0 X 10¹⁸ cm⁻³ |
| Depth of the gate trench              | 6.0 μm       | 6.0 μm     |
| Width of the gate trench              | 0.5 μm       | 0.5 μm     |
| Concentration of n-poly               | --           | 1.0 X 10¹⁹ cm⁻³ |
| Concentration of n-poly1              | 1.0 X 10¹⁹ cm⁻³ | --         |
| Concentration of n-poly2              | 1.0 X 10¹⁴ cm⁻³ | --         |
| Concentration of p-poly               | 1.0 X 10¹⁶ cm⁻³ | --         |
| Doping of p-body                      | 1.0 X 10¹⁷ cm⁻³ | 1.0 X 10¹⁷ cm⁻³ |
| Length of channel                     | 1.0 μm       | 1.0 μm     |
| Concentration of P⁺ contact region    | 1.0 X 10²⁰ cm⁻³ | 1.0 X 10²⁰ cm⁻³ |
| Thickness of gate oxide               | 0.1 μm       | 0.1 μm     |

process flow is illustrated, and shown in Figure 2. Beginning with an n-type substrate, the surface p-body, n⁺ and p⁺ regions are formed as shown in Figure 2(a). Next, inductively coupled plasma reactive-ion etching (ICP-RIE) is recommended to form the trench as shown in Figure 2(b). The gate oxide with a thickness of ≈100 nm is formed by thermal oxidation, where an n-type polysilicon is deposited by the LPCVD process and subsequently etched back to form the n-poly2 in the trench. Afterwards, the p-type polysilicon is used to refill the trench and etched back to form the p-poly. And an n-type polysilicon is used to refill the trench and etch back to form the layer of n-poly1. Finally, the source contact is formed after isolating the gate and the source.

3 | ANALYSIS AND DISCUSSION

The static and dynamic performances of the npn-FS-TIGBT and the C-FS-TIGBT have been examined and compared through extensive numerical simulations. The compared electrical performances mainly include static behaviours (transfer characteristic, $I-V$ breakdown voltage and parasitic capacitance) and dynamic behaviour (gate-collector charge and turn-off performance).

3.1 | The static state characteristics

Figure 3 shows the comparison of the transfer characteristic curves of the npn-FS-TIGBT and the C-FS-TIGBT, indicating that these two device structures have a similar threshold voltage, of about 4.5 V. The simulation breakdown curve at the avalanche breakdown is also shown in Figure 3, and from which, it can be seen that the value of breakdown voltage is identical for the npn-FS-TIGBT and the C-FS-TIGBT devices, and is about 1200 V. And the comparison between the output $I-V$ curves is given in Figure 4, demonstrating that the two structures have almost the same value of on-state voltage drop ($V_{on} = 2.85 V \text{ at } j_{ce} = 100 A/cm^2 \text{ and } V_{ge} = 10 V$) and have almost identical current driving capability. Since the npn-FS-TIGBT has the same channel, blocking layer parameters as the C-FS-TIGBT, ensure that these two structures have almost identical values of threshold voltage, breakdown voltage and on-state voltage drop.

However, it can be obtained from Figure 5, that by plotting the parasitic capacitance performance (input capacitance $C_{iss}$, output capacitance $C_{oss}$ and reverse transfer capacitance $C_{res}$), that the proposed structure of npn-FS-TIGBT has a superior capacitance performance compared to the C-FS-TIGBT. The values of $C_{iss}$, $C_{oss}$ and $C_{res}$ are summarized in Table 2. From this table, it can be concluded that the $C_{res}$ of the proposed structure is reduced by 92.0% and 48.3% compared to the conventional structure at $V_{ce} = 0 V$ and $V_{ce} = 20 V$, respectively. The input capacitance and output capacitances are also reduced, to one degree or another. The main factor responsible for this is the series attachment of the two diode capacitances ($C_{d1}$ and $C_{d2}$ as shown in the Figure 1(a)) between the gate and the collector electrodes compared to the conventional structure. Thus,
FIGURE 2  Major front-side process flow for the proposed structure. (a) Form the p-body, N+ and P+ region. (b) Form the trench by ICP-RIE. (c) Form the gate oxide by thermal oxidation and n-type polysilicon (n-poly2) is deposited by LPVCD. (d) Etch back the n-type polysilicon and refill the trench with p-type polysilicon. (e) Etch back the p-type polysilicon and refill the trench with n-type polysilicon (n-poly1). (f) Etch back the n-type polysilicon, isolation and form the electrode.

FIGURE 3  Transfer and breakdown characteristics of npn-FS-TIGBT and C-FS-TIGBT

FIGURE 4  Forward $I-V$ characteristic of npn-FS-TIGBT and C-FS-TIGBT

FIGURE 5  Comparison of the capacitance performance between npn-FS-TIGBT and C-FS-TIGBT

the capacitive performance shows remarkable improvement and the parasitic capacitance is significantly reduced. In order to further indicate the role of the npn structure in the gate trench on the capacitance characteristics, the distribution of the potential at $V_{gc} = 0$ V and depletion edge at $V_{ce} = 0$ V is investigated and compared as shown in Figures 6 and 7, respectively. From the Figure 5, we can obtain that there exists two reverse biased diodes, comprising of p-poly, n-poly1 and n-poly2, which explains why two depletion capacitances $C_{d1}$ and $C_{d2}$ as shown in the Figure 6 have been introduced. The depletion capacitance $C_{d1}$ and $C_{d2}$ is in series with the gate-collector capacitance, leading to the reduction in total gate-collector capacitance ($C_{res}$). Thus, the utilization of the npn structure in the gate trench plays an important role in reducing the Miller capacitance, and simul-
TABLE 2 Capacitance performance comparison

|                        | \( V_{ce} = 0 \text{ V} \) | \( V_{ce} = 20 \text{ V} \) |
|------------------------|-----------------------------|-----------------------------|
|                        | npn-FS-TIGBT                | C-FS-TIGBT                  | ImP\%       | npn-FS-TIGBT                | C-FS-TIGBT                  | ImP\%       |
| Input capacitance \( C_{iss} \) (nF/cm\(^2\)) | 16.5                        | 34.0                        | 51.5%       | 15.75                       | 17.5                        | 10.0%       |
| Output capacitance \( C_{oss} \) (pF/cm\(^2\)) | 3250                        | 20,500                      | 84.1%       | 375                         | 472.5                       | 20.6%       |
| Reverse transfer capacitance \( C_{res} \) (or Miller capacitance (pF/cm\(^2\)) | 1450                        | 18,200                      | 92.0%       | 362.5                       | 187.5                       | 48.3%       |

FIGURE 6 Potential distribution of npn-FS-TIGBT and C-FS-TIGBT in the trench gate

FIGURE 7 Depletion edge in npn-FS-TIGBT in the gate trench

FIGURE 8 Gate-collector charge curve of npn-FS-TIGBT and C-FS-TIGBT

3.2 Dynamic state performances

Since that the gate-collector charge has a significant effect on the switching speed and loss of the transistor device, the gate-collector charge characteristic and the turn-off behaviour are simultaneously resulting in a reduction in the gate-collector charge which will be investigated in the next section.

The simulated gate-collector charge curve is plotted in Figure 8. As shown, the npn-FS-TIGBT exhibits a lower gate-collector charge \( Q_{gc} = 187.5 \text{ nC/cm}^2 \) than the C-FS-TIGBT \( Q_{gc} = 562.5 \text{ nC/cm}^2 \), in which the gate-collector charge \( Q_{gc} \) of the proposed device is reduced by \( \approx 66.7\% \) as compared to the conventional structure. The main factor causing this is the existence of the npn structure in the gate trench of the proposed transistor structure introducing two diode capacitances in series with the parasitic gate-collector capacitance, leading to a lower total gate-collector capacitance and a further lower gate-collector charge. That is to say, the improvement in the Miller capacitance \( C_{res} \) results in a remarkable reduction in the gate-collector charge.
TABLE 3 Devices performance comparison

| Device types  | BV (V) | $C_{res}$ (pF/cm²) @ $V_{ce} = 15$ V | $Q_{gc}$ (nC/cm²) |
|---------------|--------|------------------------------------|-------------------|
| npn-FS-TIGBT  | 1200   | 210.5                              | 187.5             |
| Ref. [24]     | 1200   | 251.11                             | 328.36            |

FIGURE 9 Turn-off waveform of the two structures

In order to prove the advantages of the proposed structure, the Miller capacitance and gate-collector charge of the proposed structure are compared with the split gate structure having a breakdown voltage of 1200 V, shown in reference [24], under the same test conditions. The comparative results have been presented in Table 3. It can be seen from the comparison that the npn-FS-TIGBT has a lower Miller capacitance and gate-collector charge, compared with the split gate trench type IGBT. Hence, the proposed structure can realize the high IE effect and low Miller capacitance.

The turn-off waveform is shown in Figure 9, depicting that the proposed structure has a slight improvement than the conventional structure in the turn-off loss. Through integration of the time by the product of the collector voltage and collector current, the turn-off loss is obtained to be 0.102 and 0.104 mJ for the proposed structure and conventional structure, respectively. The reduction in the turn-off loss is 2.0%, which can be omitted. Hence, the npn-FS-TIGBT and C-FS-TIGBT has almost same turn-off speed and loss.

A comparative study of the proposed structure and the split gate structure [24] is performed on the Miller capacitance and gate-collector charge, which have the same breakdown voltage of 1200 V. The comparison results have been presented in Table 3. It is can be seen that the npn-FS-TIGBT has a lower Miller capacitance and gate-collector charge, compared with the split gate trench IGBT. Hence, the proposed structure can realize the high IE effect and low Miller capacitance.

The effect of $N_{n-poly2}$ and $T_{n-poly2}$ on the $C_{res}$ is presented in Figure 10 and 11, showing that the $C_{res}$ is almost unchanged when the $N_{n-poly2}$ and $T_{n-poly2}$ changes. From the Figure 12, it is can be seen that the value of $C_{res}$ reaches a minimum when the doping of p-poly is $1 \times 10^{16}$ cm$^{-3}$. This is due to the maximum diode capacitance at this time.

4 CONCLUSIONS

In this paper, we investigate a new trench field-stop IGBT incorporated with an npn structure in the gate trench (npn-FS-TIGBT) and compare its characteristics with the conventional trench field-stop IGBT (C-FS-TIGBT) using a two-dimensional semiconductor simulator software—ATLAS. The new IGBT structure (npn-FS-TIGBT) is proposed in order to reduce the Miller capacitance and gate-collector charge with the introduction of the diode capacitance. Through the simulation investigation, the npn-FS-TIGBT structure exhibits significant reduction in the Miller capacitance and gate-collector capacitance. The former is reduced by 92.0% at $V_{ce} = 0$ V and 48.3% at $V_{ce} = 20$ V. The latter is reduced by 66.7%, without degrading the other performances, including transfer characteristic, $I-V$ curve, breakdown voltage and turn-off speed and loss.
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