Analysis of Noise in Current Mirrors with memristive Device

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Abstract—This work presents an analysis of noise in a cascode current mirror with CMOS-memristive device done by comparison with the basic current mirror. The analysis is completed based on THD for different frequency and channel length values by means of computer-aided design. AC and DC analyses are presented for both balanced and unbalanced current mirrors. While the change in the channel length has similar effect in both circuits, at high frequencies the memristive circuit is less susceptible to noise.

Index Terms—Analog Circuits Design, Memristor, Current Mirrors, LTSpice, Noise Analysis.

I. INTRODUCTION

A. Current Mirror types

Current mirrors (CM) are widely used circuits that allow to copy a reference current level and, thus, control the current through the other device. It is widely used in operational amplifiers and integrated circuits [1]. Current mirror eliminates a need to establish a current source with specific characteristics multiple times which is a very complex procedure. Instead, similar result is achieved by using only two transistors. It is also used in most operational amplifier circuits, and is among the building blocks of the integrated circuits [2]. The simplest current mirror consists of two transistors as presented in the Fig. 1. It can be further improved to enhance the performance. Thus, there are a lot of variations of current mirrors. The most popular ones are Wilson and cascode current mirror, which are presented in the Fig. 2. They provide a much better performance than a basic CM with minimum increase in complexity.

B. Noise in Current Mirrors

Main noise types in current mirrors include Flicker, Burst, Thermal and Shot noises. According to Bilotti and Mariani [3], Cascode, Wilson CMs and their main variations demonstrate similar noise tolerance with slight discrepancies at low and high frequencies. In particular, Cascode CM exhibits a consistent performance throughout the whole range of frequencies, while Wilson CM performed better at high frequencies. Another parameter that affects the noise in CMs is channel length. The same study [3] suggests that when it is lower than 1.6 μm Wilson CM is more tolerant to noise than other configurations, but there is no notable difference for greater channel length values. Thus, modifications of CM provide better performance, however the major decrease in noise can be provided by resistors. Use of resistors is not justified in the CMs because they are mostly used in IC chips where the area is limited. Memristors are proposed as a possible device that would provide a better noise tolerance while not taking too much area.

C. Memristors

Memristor is a promising device that is gaining popularity as more and more applications of its memory effect are being discovered [4]. Its existence was first predicted mathematically by Leon Chua in 1971 based on the relationship between fundamental circuit variables [5]. The first experimental memristor was built in Hewlett-Packard laboratories in 2007 [6]. It was based on two-layered titanium dioxide film that was placed between platinum and titanium films. One of the film had oxygen vacancies that created a low and high resistance.
layers. Depending on the amount of current that had passed through it previously, the oxide layer shifts towards low or high resistance sides [6]. When current is no longer applied its oxide layer remains on that particular level and resistance stays fixed at a new value [7]. This effect can be used for non-volatile memory and neuromorphic circuits [8]. A memristor based hardware is able to mimic brain synapses and much more efficiently mimics neural networks than software based algorithms [9].

D. Memristor model for simulation

In software memristor models are simulated mostly by utilizing a concept of parallel switching channels that can have on and off states [10], [11]. Depending on an applied voltage levels, channels switch ON or OFF and change the overall conductance of the device. This switch-based conductance change is represented as follows in Eq. 1.

\[
G = \frac{X}{R_{ON}} + \frac{1 - X}{R_{OFF}} \quad (1)
\]

Where X is the number of metastable switches in ON state, which can be calculated by:

\[
X = \frac{R_{ON}(R_{inst} - R_{OFF})}{R_{inst}(R_{ON} - R_{OFF})} \quad (2)
\]

Thus, oxide level in memristor is represented by a number of conducting channels in the model. This method is described in [12] and provides a suitable simulation model of memrsitor. However, memristor models available do not take into account any noise types. Nevertheless, noise in memristor was found to be equivalent to the resistor noise and, thus, have much smaller effect on a circuit than the noise in transistors, and is of no interest.

In this paper, we provide a noise analysis of the cascode current mirror, and investigate the dependence between the noise level and frequency, transistor channel length, memristor resistance. Also, a practical case of a circuit with unbalanced values of channel length and memristor resistance is evaluated.

II. SMALL-SIGNAL MODEL ANALYSIS

A. Basic Current Mirror

For a basic transistor-based current mirror as in Fig. 1, a small-signal model will be as presented in the Fig. 3. Main equations describing its operation are as follows, [13], [14]:

\[
v_1 = h_{11}i_1 + h_{12}v_2 \\
i_2 = h_{21}i_1 + h_{22}v_2
\]

h-parameters can be found from the model by setting corresponding voltage and current values to 0;

\[
h_{11} = \frac{v_2}{i_2} = \frac{1}{g_{m1} + g_{m2} + (1 + \frac{g_{m1}}{g_{m2}})}  \\
h_{12} = 0 \\
h_{21} = \frac{i_2}{i_1} = \frac{g_{m2}}{g_{m1} + g_{m2}}  \\
h_{22} = \frac{i_2}{v_2} = \frac{1}{r_{o2}}
\]

For MOSFET specifically the result will be:

\[
h_{11} = \frac{1}{g_{m1}} \\
h_{12} = 0 \\
h_{21} = g_{m2} \frac{g_{m2}}{g_{m1}} \approx \frac{g_{m2}}{g_{m1}} = \frac{I_{C2}}{I_{C1}} \approx n \\
h_{22} = \frac{1}{r_{o2}}
\]

From the equations above, the values of input and output resistances will be \(\frac{1}{g_{m1}}\) and \(\frac{1}{r_{o2}}\) respectively. It can be seen that the output/input ratio is largely determined by geometry of transistors along with the output voltage level.

B. Current Mirror with Memristor

In the cascode CM two transistors are substituted by memristors. This causes a circuit to be simplified into a basic current mirror with, essentially, non-linear resistors as in Fig. 4. Memristors in the small-signal model are represented as additional resistances in series with existing ones. Thus, the
overall operation of the circuit will not change. Input and output resistances become as follows:
\[
\begin{align*}
  r_{in} &= \frac{1}{g_{m1} + r_{mem1}} \\
  r_{out} &= \frac{1}{r_{a2} + r_{mem2}}
\end{align*}
\]

Where \( R_{mem1} \) and \( R_{mem2} \) are memristor resistance values at input and output sides of current mirrors respectively. When these memristors are identical their resistance expressions are the same. Mathematically these resistances can be expressed through a state variable \( w(t) \) with range from 0 to 1 as presented by Z. Biolek [15]:
\[
\begin{align*}
  V(t) &= \frac{R_{ON} w(t)}{D} + R_{OFF}(1 - \frac{w(t)}{D})I(t) \\
  v_D &= \frac{dw(t)}{dt} = \frac{\mu_D R_{ON}}{D} I(t) \\
  w(t) &= \frac{\mu_D R_{ON}}{D} q(t)
\end{align*}
\]

Where \( v_D \) is a drift velocity of oxygen deficiencies. A windowing function can be added to ensure that the value of \( w(t) \) does not exceed the range from 0 to 1. Then, by equating \( \frac{w(t)}{D} \) to \( x(t) \):
\[
\begin{align*}
  x(t) &= \frac{w(t)}{D} \\
  \frac{dx}{dt} &= \frac{\mu_D R_{ON}}{D^2} I(t) F(x(t))
\end{align*}
\]
a windowing function will be
\[
F(x(t)) = 1 - (2x(t) - 1)^2 p
\]

When value of the state variable is 0 memristor is operating at the lowest resistance \( R_{ON} \), and 1 stands for the maximum resistance state \( R_{OFF} \). Parameter \( p \) defines a sharpness of a window boundary - lower values will provide a smoother transition, while higher values will give an almost rectangular function. This mathematical representation was used in memristor Spice model proposed by HP lab [12], and all other models are largely based on it.

### III. Simulation Parameters

In the simulation of the circuit presented in the Fig. 4 the BSIM 3.1 MOSFET model provided by MOSIS [16] is used. The Length of the channel is 180nm. A memristor model added in the circuit was developed by Knownm organization [10]. Its initial major parameters are \( R_{on} 5000 \Omega \), \( R_{off} 15000 \Omega \) and threshold voltage 0.27V.

For an AC analysis because the .noise command in LTSpice does not take into account the effect of memristor in the circuit, a Fourier coefficients are evaluated instead. A comparison is made on the basis of total harmonic distortion. A major problem of the Fourier analysis is that its accuracy is heavily dependent on the resolution of a data sample and its size [17]. However, eliminating this problem by setting a resolution and length of the simulation high is not feasible as it takes too long for the software to evaluate it. So, this calculation error is instead kept constant throughout the simulation by providing the same number of evaluation points and periods for estimation. Thus, for different frequencies appropriate total time and maximum time step are set to keep the number of evaluation points constant.

For the DC analysis cases of imbalanced transistor lengths and imbalanced memristor resistances are considered. The channel lengths of both transistors M1 and M2, from the Fig. 4, are varied to observe the dependence between the current and channel length difference. The parameter LINT in the model file was changed for that [18]. For the case of imbalanced memristor resistance values, the memristor in series with the output is varied. The values considered are in the range of 10% from the original value.

### IV. Results

#### A. Frequency Dependence

In the simulation THD for six different frequencies from 1Hz to 10GHz with logarithmic step of 100 in circuits with and without memristor was observed. The circuit without memristor shows approximately constant noise for the whole range with abrupt fall at 0.1GHz which is caused by a decrease in noise of the main transistor and not yet coming into picture effect of the other transistor. In contrast, the circuit with memristor exhibits a clear decline in noise at higher frequencies. In particular, it becomes 0.03% when frequency is lower than 10KHz, 0.009% at 100MHz and 0.000122% at 10GHz as can be seen in the Fig. 6.

#### B. Channel length dependence

The same procedure is done for different channel length values. The values considered were \( 1.7 \cdot 10^{-8}, 2.0 \cdot 10^{-8}, 2.5 \cdot 10^{-8} \) and \( 3.0 \cdot 10^{-8} \)m. The resultant change in the total harmonic distortion is very small, in the order of \( 10^{-6} \). This change is irrespective of frequency as can be seen in the Fig. 7 and 8. The average slope for six frequencies of the CM with
C. Channel length dependence for the DC source

When the channel length of the transistor which is in series with the output is changed the reference current does not change, but some discrepancy occurs between it and the output current that previously was not observed. Thus, for the source voltage amplitude equal to 3V, the current changes by 74.9μA per nm change of the length; for 5V source this value becomes 146μA per nm; and 229μA per nm for 8V supply voltage. For the basic current mirror without memristors, the current on channel length dependence is higher, namely 86μA per nm change of the length for a 3V source as shown in Fig. 9.

When the length of another transistor, M1, is increased it affects both current values. In particular, the reference current increases, and the output current decreases, though much slower. Notably, the discrepancy between two currents in both cases is the same. Thus, for the 3V source voltage the difference between reference current and output current

memristor is calculated to be $6.271.7 \cdot 10^{-8}$ per μm and for the CM without it 1.95e-5 per μm.
increased by 74.9 μA per nm change in the length of M1 as well.

D. Memristor resistance dependence for the DC source

Similar procedure is performed for the ON resistance of memristor. The variation is set to 10% of the initial value. As expected, the current is decreasing as the resistance value increases linearly. For the source voltage value equal to 3V the difference between the reference and the output currents rises by 13 μA/Ω, for 5V by 11.4 μA/Ω and for 8V by 2.67 μA/Ω.

V. DISCUSSION

The AC analysis results suggest that for a wide range of frequencies the CM with memristor has higher THD level than the basic CM. However, at high frequencies the THD value of the circuit with memristor goes to almost zero. In addition, the change in transistor channel length affects the proposed circuit less, which can be useful in minimizing the effect of inaccuracies that frequently occur in manufacturing process.

The DC analysis of the circuit also shows that the discrepancy that occurs because of the channel length imbalance is less for the CM with memristor when compared to the basic CM. Also, when memristor resistance variations are considered and changed from 500 Ω to 550 Ω the discrepancy between the output current and the reference current is much smaller for memristor resistance variations when compared to the transistor channel length imbalance.

This analysis is limited to the comparison of the basic CMs with and without memristor. Similar comparison can be drawn between the cascode CM and a basic CM with memristor. Also, a basic CM with resistors instead of memristors could be considered. Memristor in this circuit does not really utilize its memory effect, so the main reason for its introduction into the circuit is to save area. However, in this paper the case when the voltage level of the source is close to the threshold voltage of memristor were not considered. So, other possible advantageous properties could be observed in that case. Moreover, a more complete analysis could be performed by introducing the noise of memristor and using a more practical transistor models.

VI. CONCLUSION

In conclusion, the analysis of noise in the CM with memristor is presented in this paper. Both AC and DC cases are considered for transistor channel length and memristor resistance variations. The results show that memristor in the basic current mirror makes its noise level less at high frequencies, and also decreases the dependence on channel length variations significantly. Small area of memristor makes the proposed circuit a viable option when high transistor variation tolerance or low noise at high frequencies is required. The analysis,
however, is limited to the comparison with the basic CM. It can be further extended by comparing the circuit with the other configurations. In addition, transistor and memristor models do not exhibit real-life properties of the devices, which puts a limitation to the viability of results obtained.

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