Persistent Josephson Phase-Slip Memory with Topological Protection

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Superconducting computing promises enhanced computational power in both classical and quantum approaches. Yet, efficient schemes for scalable and fast superconducting memories are still missing. On the one hand, the large inductance required in magnetic flux-controlled Josephson memories [1, 2] impedes device miniaturization. On the other hand, the use of ferromagnetic order to store information [3–8] often degrades superconductivity, and limits the operation speed to the magnetization switching rate of a few GHz. Here, we overcome the above limitations through a fully superconducting memory cell based on the topological transition driven by hysteretic phase slips [9, 10] existing in aluminum nanowire Josephson junctions [11, 12]. Our direct and non-destructive read-out scheme, based on local tunneling spectroscopy, ensures reduced dissipation (∼40 fW) and estimated response time below ∼30 ps thereby yielding a maximum energy per bit consumption as low as ∼10⁻²⁴ J. In addition, the memory topological index can be directly read by robust phase measurements thus further lowering dissipation whilst maximizing the stability against magnetic noise. The memory, measured over several days, showed no evidence of information degradation up to ∼1.1 K, i.e., ∼85% of the critical temperature of aluminum. The ease of operation combined with remarkable performance elects the Josephson phase-slip memory as an attractive storage cell to be exploited in advanced superconducting logic architectures.

A Josephson junction (JJ) consists of a localized discontinuity (weak link) in the order parameter of two superconducting electrodes [13], where the Cooper pairs transport is ruled by the macroscopic quantum phase difference (ϕ) across the junction. Weak links are typically realized in the form of a thin insulator, a normal metal wire or a narrow superconducting constriction [11, 13]. The junction current-phase relation (CPR) strongly depends on the structural attributes of the constriction, i.e., on how its effective length (d), i.e., the distance between the superconducting leads), width (w), and thickness (t) compare to the superconducting coherence length (ξw) [11]. In a fully superconducting one-dimensional JJ (w, t ≪ ξw) the CPR evolves from the single-valued distorted sinusoidal characteristic, typical of the short-junction limit (d ≪ ξw, Fig. 1a), to the multi-valued function obtained in the long regime (d ≫ ξw, Fig. 1b) [11]. In the latter scenario, the Josephson current (Ij) flowing through the junction follows a hysteretic evolution in ϕ due to the presence of two energetically-stable states (corresponding to even and odd topological index) well separated by a strong phase-slip energy barrier [9], and accessible by going through the phase contour in the forward or backward direction (see Fig. 1b). These two states are topologically discriminated by the parity of the winding number of the superconducting phase along the wire [9, 14] which reflects into opposite directions of the supercurrent flow [10], as shown in Fig. 1b. The transition between the even and odd state requires to pass through a gapless condition via a 2π phase-slip occurring in the superconducting nanowire [11, 12]. We therefore take advantage of this topologically-protected hysteresis loop and well defined parity states to implement a robust and permanent superconducting memory: the Josephson phase-slip memory (PSM).

The design of a proof-of-concept PSM requires an architecture enabling the tuning of the phase ϕ, and the definition of an efficient readout scheme. The most effective way to finely control ϕ is by inserting the JJ in a superconducting loop, where an external magnetic field gives rise to a total flux Φ piercing the ring area. Stemming from fluidic quantization [16], the superconducting phase difference across the weak link is given by ϕ = 2πΦ/Φ0 (where Φ0 ≃ 2.067 × 10⁻¹⁵ Wb is the flux-quantum). The phase together with the topological index determines the amplitude of the gap in the local density of states (DOS) of the wire [12] which can be probed with a metallic electrode tunnel-coupled to the middle of the junction (see the sketch on top of Fig. 1c), thereby implementing a superconducting quantum interference proximity transistor (SQUIPT) [17]. The DOS determines the tunneling current (I) flowing through the probing electrode which can vary from a continuous function of Φ for a short junction (Fig. 1c) to a discontinuous characteristic reflecting the hysteresis in the long regime (Fig. 1d). The parity of the topological index and Φ then determines the amplitude of the tunneling current that can read the logic [0] and [1] states of the PSM cell (see Fig. 1d).

Figure 1-e shows the scanning electron micrograph (SEM) of a representative PSM cell realized through a suspended-mask lithography technique (see Methods for fabrication details). The weak link consists of a one-dimensional Al nanowire (green, t = 25 nm and w = 90

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FIG. 1. PSM working principle and structure. Sketch of the current-phase relation (\(I_s\) vs \(\varphi\)) of a S-S’-S weak link in the short (a) and long (b) junction regime. The CPR evolves from a deformed sinuous to a multi-valued function as the junction length increases. The transition between the two topologically-protected states (corresponding to even and odd topological index) \([9]\) is due to phase-slips occurring in the wire \([11, 15]\), and corresponds to a vertical jump between the two current branches (indicated by coloured arrows). Dependence of the tunnel current on the normalised applied magnetic flux \(\Phi/\Phi_0\) for a SQUID in the short (c) and long (d) junction regime. In the latter case, the current evolution shows a hysteretical profile, which stems from the multi-valued CPR. Top: scheme of a voltage-biased DC SQUID in a two-wire configuration. \(\Phi\) is the magnetic flux piercing the ring. Pseudo-colour scanning electron micrograph of a typical PSM. An Al nanowire (green) is inserted in a micron-size Al ring (yellow), whereas an \(Al_{0.98}Mn_{0.02}\) probing electrode (red) is tunnel-coupled to the middle of the nanowire and to a second Al electrode (green) to allow the memory operation. Inset: blow-up of the weak-link region. The passive replicas due to the three-angle shadow-mask metal depositions are visible.
FIG. 2. PSM magneto-electric response. a Current vs voltage characteristics acquired at Φ = 0 (black trace) and Φ = 0.5Φ₀ (orange trace). The magnetic flux modulates Δφ and, therefore, the I–V tunnel characteristics. b Current modulation I(Φ) of a typical PSM cell biased at V = 300 μV. The purple and green arrows indicate the magnetic flux sweep directions. The width of the hysteretic loop (δΦ), the current drop (δI), and the current at the hysteresis crossing-point [I₀ = I(0.5Φ₀)], are also indicated. c Evolution of I(Φ) acquired for selected values of V, as indicated by the coloured arrows in panel a. I₀ increases by rising V. d Dependence of the hysteretic width (δΦ) on V. δΦ monotonically drops by increasing V. e Relative variation of the tunneling current (ζ = δI/I₀) vs V. All these measurements were taken at T = 25 mK.

perconducting loop with a flux (Φₔ) comprised within the hysteretic domain (Φₐₘᵢₜ, Φₐₗₘₚₖ). Writing (erasing) operations are performed by lowering (increasing) the total flux below (above) the hysteretic domain, as sketched in Fig. 3a. The two logic states [1] and [0] encoded in the topological index of the PSM (odd or even) can be simply read through the amplitude of the tunneling current measured with a low-power non-destructive scheme.

Figure 3b shows the writing/erasing operations in the continuous read-mode, i.e., when a bias voltage V = 300 μV is permanently applied. The bias flux is set at 0.54Φ₀, i.e., just above the crossing-point of the hysteresis (see Fig. 2c). The memory is initialized in the [0] state corresponding to a low current of I ≃ 43 pA. By applying a negative flux pulse down to Φₔ = 0.33Φ₀, the PSM logic state suddenly jumps to [1] as detected by the current jump to I ≃ 90 pA. Conversely, the logic state [0] is recovered via a positive erase pulse up to Φₔ = 0.75Φ₀. The device unequivocally shows the typical behavior of a memory cell upon many erasing/writing cycles.

The ability of the PSM to retain the data even when the bias voltage is temporarily turned off (non-volatile memory) is displayed in Fig. 3c. Here, the reading voltage is set to V only during the readout operation. Non-volatility is a fundamental requirement for energy saving since power is dissipated only during the readout procedure without losing the stored information. The readout dissipation obtains values as low as P₀ ≃ 25 fW for logic state [0], and P₁ ≃ 40 fW for logic state [1]. Moreover, the operations have been performed several times always with comparable results, highlighting the relevant endurance of the device.

The intrinsic bandwidth limits of the PSM read and write operations were not achieved due to the strong cut-off (≈ 800 Hz) of our cryogenic filters and the large inductance of the superconducting coil used for the writing/erasing operations. However, a switching time of ≃ 1 ps for the writing/erasing process is expected, which is typical for small superconducting loops, while a readout time of τₐ = 30 ps can be estimated from the charging time of the tunnel junctions (see Methods for details). The PSM speed is therefore expected to be on par with current state-of-the-art superconducting memories [2, 4, 6–8].

The combination of low power dissipation and fast access time yields tiny energy required per bit J₀ = P₀τₐ ≃ 0.8 yJ and J₁ = P¹τₐ ≃ 1.3 yJ for the readout operation of state [0] and [1], respectively. Notably, these values are several orders of magnitude smaller than any superconducting memory reported so far, and well
FIG. 3. Performance of the PSM with DC read-out. a Sketch of the PSM operation principle at a constant voltage bias ($V$). Low (blue, $I_{[0]}$) and high (red, $I_{[1]}$) current branches at the bias flux [$\Phi_B \in (0.5\Phi_0, \Phi_{B,\max})$] encode the [0] and [1] logic states, respectively. The erase (write) operation is performed by applying a flux pulse with amplitude $\Phi_B > \Phi_{B,\max}$ ($\Phi_B < \Phi_{B,\min}$). The PSM can also be operated in the complementary part of the hysteresis at $\Phi_B \in (\Phi_{B,\min}, 0.5\Phi_0)$ by exchanging the erase and write fluxes. b Evolution of the read-out tunneling current (top panel) measured at $V = 300 \, \mu V$ for $\Phi$ composed by a bias flux $\Phi_B = 0.54\Phi_0$ interrupted by write ($\Phi_W = 0.33\Phi_0$) and erase ($\Phi_E = 0.75\Phi_0$) pulses (bottom panel). c Same as b but now the voltage bias (central panel) is applied only during the read-out operation to minimize power consumption and demonstrate the non-volatility of the PSM. All the measurements were taken at $T = 25 \, \text{mK}$. 

below the requirements of rapid single flux quantum (RSFQ) logic [2, 3, 6].

The robustness of the PSM against flux fluctuations is tested by superimposing to the working biasing flux a sizable sinusoidal signal ($\Phi_{AC}$, see Fig. 4a). The PSM shows optimal stability with respect to flux oscillations, as shown in Fig. 4b for $V = 300 \, \mu V$ and $\Phi_B = 0.56\Phi_0$. The memory preserves the stored state, and keeps the readout of the two logic states well separated for $\Phi_{AC} \simeq 0.04\Phi_0$, that is $\sim 80\%$ of the separation between the working and the minimum erasing flux. Interestingly, thanks to the opposite magnetococonductance of the tunnel barrier in the two topological states, the AC flux modulation reflects in the AC response of the tunneling current that acquires a phase shift of $\pi$ between the two logic states [0] and [1]. This phase shift provides an alternative and efficient method to probe the parity of the JJ winding number, which is not affected by the position of $\Phi_B$ within the hysteretic domain, or by the low visibility of the DC readout signal (see Figs. 9 and 10 for more details).

Figure 4c displays a persistency test of the PSM realized with the phase-based readout. The memory is initialized to logic state [1], and the readout is performed every 4 hours. No sign of signal degradation has been observed even after $\sim 3$ days of measurement. This confirms the stability of the PSM as a permanent memory, which is guaranteed by the vanishing phase-slip rate ($\sim e^{-10^{17} s^{-1}}$) expected at low temperature [12, 20].

High temperature can degrade, in principle, the performance of PSM by increasing $\xi_w$ [13] thereby lowering the JJ effective length, and driving the nanowire junction towards the non-hysteretic single-valued CPR which is expected to occur for $d \lesssim 3.5\xi_w$ [11, 15]. In addition, thermal activation can substantially increase the phase-slip rate [12]. Figure 5a shows the evolution of the hysteresis loop at several bath temperatures ($T$). The hysteresis progressively fades out by increasing $T$ and persist up to 1.1 K, which corresponds to $\sim 85\%$ of the nanowire critical temperature, with $d\Phi$ reduced to $\sim 12\%$ with respect to base temperature (see Fig. 5b). Figure 5c shows $\zeta$ vs $T$ for different values of bias voltage, and highlights the drop of $\zeta$ by increasing $T$. The observed high-temperature operation of the PSM indicates a substantial protection of the topological state even in the presence of a sizable amount of hot quasiparticles [9].

In summary, we have envisioned and demonstrated an original persistent Josephson phase-slip memory cell which takes advantage of fluxoid quantization to codify two logic states in the topological index of the system, i.e., the superconducting winding number [14]. Differing from conventional superconducting loops, here the separation between the two topological states is provided by the large phase-slip barrier, which is unique to long superconducting JJs [9, 12]. The memory exploits conventional superconductors thereby avoiding the use of complex ferromagnetic metals typical of present superconducting memories [3–8]. Notably, the PSM is characterized by reduced readout dissipation ($\lesssim 40 \, \text{fW}$), short estimated response time ($\lesssim 30 \, \text{ps}$), and ultralow energy per bit ($\sim 10^{-24} \, \text{J}$). Moreover, the PSM state shows endurance, persistence, and high-temperature operation (up to $\sim 1.1 \, \text{K}$), only limited by the Al critical temperature. The use of vanadium [19] or niobium [21], therefore, could push memory operation above liquid He temperature, and further improve miniaturization thanks to the low coherence length of these metals. In addition, our phase-based read-out scheme ensures stark protection against magnetic flux fluctuations, and provides ideal visibility in all the operation ranges. This makes the PSM a suitable candidate for the implementation of industrially-scalable classical memory cells in actual superconducting electronics technologies, such as rapid single flux quantum (RSFQ) [22], reciprocal quan-
FIG. 4. Performance of the PSM with AC read-out. a Sketch of PSM operation in the presence of a sinusoidal flux oscillation ($\Phi_{\text{AC}}$) around $\Phi_{\text{B}} \in (0.5\Phi_0, \Phi_{\text{B,max}})$. b Evolution of the read-out current (top) measured at $V = 300 \mu$V and $/Phi$ composed by a flux bias ($\Phi_{\text{B}} = 0.56\Phi_0$) superimposed with a sinusoidal fluctuation $\Phi_{\text{AC}} = \pm 0.04\Phi_0$ (bottom). Write ($\Phi_{\text{W}} = 0.32\Phi_0$) and erase ($\Phi_{\text{E}} = 0.81\Phi_0$) flux pulses are applied to switch the logic state of the PSM. Notice that the two current signals oscillate with $180^\circ$ phase shift making the phase of the AC signal a very sensitive read-out observable. Vertical dashed lines highlight the signals phase shift with respect to the magnetic flux. c Demonstration of persistent PSM operation at $\Phi = 0.5\Phi_0$ obtained by measuring the signal phase with a lockin amplifier (top) every 4 hours and only when the read-out voltage is turned on ($V = 300 \mu$V, bottom). State [1] was measured for almost 3 days without showing any sign of degradation and low dissipation being $V = 0$ for most of the time. All the data were recorded at $T = 25$ mK.

quantum logic (RQL) [23], quantum flux parametrons (QFPs) [24], Josephson field-effect transistors (JoFETs) [25], and gate-controlled cryotrons (EF-trons) [26, 27]. Yet, the strong topological protection and stability observed in the PSM make our approach promising in light of the implementation of phase-slip flux qubits[28] and quantum memories.

METHODS

Device fabrication details. The hybrid memory cells were realized by shadow-mask lithography technique. The suspended resist-mask was defined by electron-beam lithography (EBL) onto a SiO$_2$ wafer. All metal-to-metal clean interfaces, and metal-to-oxide barriers were realized in an ultra-high vacuum (UHV) electron-beam evaporator (EBE) with a base pressure of $10^{-11}$ Torr equipped with a tiltable sample holder suitable for multi-directional depositions. In order to obtain wire/ring transparent interfaces, which is crucial for the device operation, the use of the same material is strongly recommended [18]. Therefore, the nanowire and the ring of the PSM were realized with aluminum. Furthermore, the Al film evaporation is relatively simple, and its high-quality native oxide allows the realization of good tunnel barriers through oxygen exposure at room temperature. At first, 15 nm of Al$_{0.98}$Mn$_{0.02}$ were evaporated at an angle of -18$^\circ$ to realize the normal metal electrode. Subsequently, the sample was exposed to 60 mTorr of O$_2$ for 5 min in order to form the thin insulating AlMnO$_x$ layer. Next, the sample holder was tilted to 10$^\circ$ for the deposition of 20 nm of Al realizing the SQUIPT nanowire (length $d = 400$ nm, width $w = 90$ nm) and the superconducting electrodes. Finally, a thicker layer of Al ($t_R = 70$ nm) was evaporated at 0$^\circ$ to realize the superconducting loop of circumference $\sim 7.6 \mu$m, and average width $w_{R,\text{ave}} \simeq 600$ nm.

Magneto-electrical characterization. The magneto-electric characterization of the samples was performed at cryogenic temperatures in a $^3$He-$^4$He dilution refrigerator (Triton 200, Oxford Instruments) equipped with RC-filters of resistance $\sim 2k\Omega$. The out-of-plane magnetic field was applied via a superconducting magnet driven by a low-noise current source (Series 2600, Keithley Instruments). The DC measurements were performed in a two-wire voltage-bias...
for ξ_{w,short} ≥ d/3.5 ∼ 114 nm [11] is reached at temperature T_{short} = T_{C,w}(1 − 0.852ξ_{w,0}/ξ_{w,short}) ∼ 1.3 K [11, 13], where l = 3D/υ_F ∼ 3.3 nm is the nanowire free path, and υ_F = 2.03 × 10^6 m/s is the Fermi velocity of Al.

The kinetic inductance (L_K) of a long JJ depends on the geometry and superconducting properties of the nanowire [12]. In our case, at 25 mK it takes the value L_K = R_Nℏ/ 2πl/ξ ∼ 15 pH [29]. The nanowire normal-state resistance is given by R_N = d/υ_F ∼ 14 Ω, where σ = DN_f e^2 = 1.24 × 10^7 S is the Al film conductance (with N_f = 2.15 × 10^{27} J^{-1} m^{-3} the density of states at the Fermi energy of Al). Analogously, the ring total inductance takes the value L_R ∼ 1.5 pH (with normal-state resistance R_R ∼ 1.4 Ω). The contribution of the ring to the total inductance of the SQUIPT yields a screening parameter β = 2πL_RI_C/Φ_0 ∼ 0.1, where I_C ∼ 20 μA is the low-temperature nanowire critical current deduced from the weak link geometry [18]. The small β cannot account for the hysteretic behavior of the PSM, which stems, differently, from the long-junction regime of the Josephson nanowire [12, 18].

The writing/erasing time (τ_{W,E}) is mainly due to the time required to polarize the SQUIPT with the external flux. It is given by τ_{W,E} = L_{SQUIPT}/R_{SQUIPT} ∼ 1.1 ps, where L_{SQUIPT} = L_K + L_R and R_{SQUIPT} = R_N + R_R are the total inductance and resistance of the SQUIPT, respectively. The read out time (τ_R) is predominantly limited by the characteristic time of the two tunnel barriers, τ_R = τ_{11} + τ_{12} ∼ 31 ps, where τ_{11} = R_{11}C_{11} ∼ 19.5 ps is the characteristic time of the first tunnel junction, and τ_{12} = R_{22}C_{12} ∼ 11.5 ps is the time constant of the second junction. The junctions capacitances (C_{11} ∼ 0.3 ff and C_{12} ∼ 0.13 ff) are estimated from the area and the typical specific capacitance of AlOx tunnel barriers ∼ 50 ff/μm^2 [30].

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AUTHOR CONTRIBUTIONS

E.S. and F.G. conceived the experiment. N.L. fabricated the samples with inputs from F.P., N.L. and E.S. performed the measurements. N.L. analysed the experimental data with inputs from E.S. and F.G. N.L and F.P. wrote the manuscript with inputs from all the authors. All the authors discussed the results and their implications equally at all stages.

ADDITIONAL INFORMATION

The authors declare no competing financial interests.
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FIG. 6. Hysteresis in the current vs voltage characteristics - Current ($I$) vs voltage ($V$) curves measured at different values of magnetic flux ($\Phi$). Left panel: $I(V)$ recorded while increasing $\Phi$ (forward). Right panel: $I(V)$ recorded while decreasing $\Phi$ (backward). The tunnel $I(V)$ characteristics reveal a hysteric behavior with $\Phi$, showing a maximum reduction of the Al nanowire gap ($\Delta w$) at $\Phi = 0.54\Phi_0$ and $\Phi = 0.45\Phi_0$ for the forward and backward traces, respectively. All data were recorded at $T = 25\,\text{mK}$.

FIG. 7. PSM in continuous read-out configuration for several applied voltage biases - Writing/erasing operations in the continuous read-out mode performed for different values of permanently applied voltage bias ($V$). Bottom: write ($\Phi_W = 0.33\Phi_0$) and erase ($\Phi_E = 0.75\Phi_0$) magnetic fluxes applied around the read-out flux ($\Phi_R = 0.54\Phi_0$). Top: the read-out current ($I$) measured for different values of voltage bias ($V$). The higher (lower) current value $I_{[1]}$ ($I_{[0]}$) acquired for a fixed $V_b$ corresponds to logic state $[1]$ ($[0]$). $I_{[1]}$ and $I_{[0]}$ are negligible for $V < 300\,\mu\text{V}$, therefore the PSM cannot be biased in that voltage range. Note that the memory works properly also applying multiple times the voltage bias, confirming the endurance of the PSM cell. All data were acquired at $T = 25\,\text{mK}$. 
FIG. 8. Non-volatility of the PSM measured at different $V$ - Writing/erasing operations performed for different values of a pulsed readout voltage bias ($V$). The values of $V$ ranges form: 400 $\mu$V (a), 450 $\mu$V (b), 500 $\mu$V (c) and 550 $\mu$V (d). For each panel is shown the temporal evolution of the magnetic flux applied to the PSM (bottom) together with the bias voltage pulses (center) and the resulting tunnel current (top) used for the state readout. The flux was biased at $\Phi_B = 0.54 \Phi_0$ while flux pulses of $\Phi_W = 0.33 \Phi_0$ and $\Phi_E = 0.75 \Phi_0$ were used for write and erase operations, respectively. The permanency of the memory state before and after the application of the readout bias demonstrate the persistency and non-volatility of the PSM. Note that the PSM works properly during the operation of the device for a wide range of applied voltage biases. All measurements were performed at $T = 25$ mK.
FIG. 9. PSM operation at the degenerate flux $\Phi_B = 0.5\Phi_0$ with a sinusoidal noise ($\Phi_{AC}$) superimposed. Writing/erasing operations performed at the degenerate point $\Phi_B = 0.5\Phi_0$. Bottom: Temporal evolution of the total flux applied to the PSM and composed by a bias $\Phi_B = 0.5\Phi_0$ superimposed to a low frequency sinusoidal fluctuation with amplitude $\Phi_{AC} = \pm 0.04\Phi_0$. Write ($\Phi_W = 0.30\Phi_0$) and erase ($\Phi_E = 0.80\Phi_0$) pulses are applied to switch the memory state. Top: read-out current acquired at different voltage bias ($V$). Notice that at the degeneracy point the average values of $I_0$ and $I_1$ are indistinguishable while information of the memory state is stored in the phase of the signal. $I_0$ and $I_1$ show a $180^\circ$ phase shift. All measurements were performed at $T = 25$ mK.

FIG. 10. Phase-dependent read-out scheme - Read-out of the PSM by lock-in phase measurements. a Scheme of the PSM, where the Al ring (yellow), the Al nanowire (green) and the normal metal tunnel probe (red) are presented together with the complete electrical set-up. The PSM is biased with a DC constant voltage $V = 400 \mu V$. The magnetic flux piercing the superconducting ring is $\Phi_B + \Phi_{AC}$, where $\Phi_B = 0.5\Phi_0$ is the flux corresponding to the crossing point of the two current branches and $\Phi_{AC}$ is a small sinusoidal component superimpose with a lock-in source. The variations of the read-out current with the flux oscillations are recorded with standard lock-in technique. b Time dependence of the phase of the readout current while write and erase operations are performed. $I_1$ oscillates in phase with the magnetic flux (phase=0), while $I_0$ has the opposite dependence (phase=180°) allowing the acquisition of the two distinguishable signals of phase. All data were recorded at $T = 25$ mK.