Wearable ECG calculation system based on microprocessor cluster

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Abstract. This article introduced a wearable ECG calculation system based on microprocessor cluster. The microprocessor cluster has the characteristics of low cost and low power consumption. This article proposes special hardware and software design methods for ECG calculation. In the experiment, a cluster of 48 Nuvoton nano120 processors was used to implement the computational tasks equivalent to the Intel i5-3317 single-core level. This cluster hardware requires only the size of a bank card in terms of volume and can be used for wearable devices.

1. Introduction

Traditional health monitoring devices have a number of shortcomings and problems. The main problem is that the potential changes in health cannot be predicted. Under normal circumstances, monitoring equipment is used only when the user feels abnormal health. Although the wearable devices that have emerged in recent years are capable of continuous detection of the user's vital signs data, due to factors such as insufficient battery life and weak computing power, it is impossible to monitor complex vital signs such as multi-lead electrocardiograms. Currently used solutions will also bring some new problems.

• Occupation of communication traffic resources. A common method used by existing wearable devices is to upload complex data to a server for solving. Due to the high sampling accuracy of complex data, the acquisition frequency is dense, and it is difficult to compress, resulting in a large amount of communication bandwidth occupied by data transmission and affecting the performance of the wireless network system.

• Heavy burden on computing servers. Since the user data is concentratedly calculated on the calculation server, when multiple users are used at the same time, the server-side communication burden, storage load, and especially the computational burden are heavy. The server is powerful and fast, but its high performance is obtained at the expense of high power consumption, high attrition, high maintenance, and high operating costs.

• 90% of simple cases do not need to be resolved by the server. Since the wearability of the wearable device is too weak and the algorithm is lacking, a large number of simple calculation tasks are also delivered to the server for calculation, causing unnecessary waste of communication resources and computing resources. If simple cases can be solved on the wearable device side, it can save a lot of communication bandwidth and server time.
• Leak of real-time performance. For severe sudden changes in vital signs, such as cardiac arrest, polarity-reversed ventricular tachycardia, if you wait for the server to return to the calculation results, you may miss the opportunity for self-aid and call for help. If device-side computing is used, a powerful processor and a large-capacity battery are required, which will affect the device's wearability. In short, there is a conflict between wearability and computational performance.

In terms of ECG equipment hardware, a conventional acquisition device requires a dedicated signal line of 10 cables, which affects wearable performance. Geng Yang et al. [1] proposed a serial bus sensor that simplifies the cable structure. G.Kavya and V.ThulasiBai [3] used an Altera FPGA chip to create a dedicated system with dual processor cores that can process ECG signal acquisition and analysis tasks in parallel. Jia-Hua Hong et al. [2] designed two dedicated low-power chips, one for collecting and wirelessly transmitting ECG signals, the other for receiving wireless signals, and integrating DSP units for the data-analysis task. Shih-Lun Chen [7] designed a dedicated chip that uses fewer logical-gates and reduces chip area for a higher price-performance ratio.

Based on the conclusions of the above researchers, it can be seen that the highly integrated custom chip has an overwhelming advantage in both power consumption and performance. However, the cost of custom chips is extremely expensive, and custom chips are difficult to be versatile. Although the traditional general-purpose microprocessor has relatively large volume and power consumption, it has undergone a large number of application tests, mature technology, low risk and low cost. The design concept of the microprocessor clustering scheme proposed in this paper is to spread the data processing algorithm to dozens of single-chip microprocessors to form a mini-cluster. With the right software design approach, this cluster can fully perform as well as the performance of a single highly integrated microprocessor, and there will be no significant difficulties in software development.

2. ECG Calculation Cluster Design

ECG automatic analysis tasks consist of a series of complex calculations. The calculation principle is shown in Figure 2. The input object of this task is the ECG data stream. First, the data must be filtered to remove noise. Then the data is scaled by a certain proportion. Afterwards the data is segmented and calculate the similarity to the preset ECG templates. Finally the similarity values trigger the activation function to get the result output.

![Figure 1. The structure of the ECG calculation task.](image_url)
In the original computational structure, Sliding Window Operations are usually performed directly on the data stream, so no Copy Operation is required. If the time required to copy the data is much longer than the data processing time, the benefit of parallel computing will be greatly reduced. If a computational task is suitable for transformation into a parallel computational structure, it should meet the requirements of formula 1 and formula 2.

$$\sum \Delta T + TTS < TSO$$  \hspace{1cm} (1)
$$\sum DCBW < CBW$$  \hspace{1cm} (2)

TTS: Parallel Unit Task Time Span  
TSO: Time Span of the Original Task  
DCBW: Data Copy Bandwidth  
CBW: Communication Bandwidth

The purpose of parallel computing is to get results faster. Formula 1 points out that the time from the beginning of the first task to the end of the last task must be less than the execution time of the original task. Otherwise, parallel calculations have no benefit. The key technique of this step is to try to reduce $\Delta T$. Formula 2 indicates that the bandwidth of all data copies cannot exceed the upper limit of the bandwidth that the communication bus can tolerate.

2.1. Cluster Hardware Design

The hardware block diagram of the ECG calculation cluster is shown in Figure 3.

$$\sum \Delta T + TTS < TSO$$  \hspace{1cm} (1)
$$\sum DCBW < CBW$$  \hspace{1cm} (2)

The main control chip is the nuvoton M472 processor (abbreviated as M472) produced by Nuvoton Technology Corporation in Taiwan, China, and the computing node uses another processor of Nuvoton, the nuvoton nano120 (abbreviated as nano120). The M472 communicates with computing nodes 1-6 through six full-duplex UART serial ports; each computing node then serially connects 7...
other computing nodes through the UART. The entire network consists of a total of 48 nano120 processors. In addition, the M472 performs broadcast functions through a simplex UART serial port. The TXD signal line of the serial port enhances the driving ability through a triode buffer circuit, and then directly connects to the RXD2 signal line of the 48 nano120 processors. All serial communication baud rates are set to 115200.

2.2. Cluster Software Design
On this cluster, one nano120 chip has a storage space of 128K and the actual available space is about 110K. Due to memory limitations, data resolution and calculation accuracy need to be properly reduced. The software process design is shown in Figure 4.

![Figure 4. ECG calculation tasks collaboration diagram.](image)

If we ignore some technical details, we can think of this system approximation as two main processes: the data broadcast process and the computation process. The data broadcast process is shown in Figure 5.

![Figure 5. Data Broadcast Process.](image)

3. Experiment
In theory, the system hardware can be completely fabricated on a bank card size double-sided circuit board as shown in Fig6. Since our goal is only to validate the method, we just use now available
development boards to build the verification system as shown in Fig7. The circuit principle of the two is exactly the same.

![Image](image1.png)

**Figure 6.** The ideal wearable ECG calculation cluster.

![Image](image2.png)

**Figure 7.** The verification machine.

The comparison system is a laptop computer with Intel i5-3317 processor. In this experiment, the laptop used only one single-threaded task to participate in ECG calculations. The performance of the two is shown in Table 1.

| Compare items          | i5-3317                      | nano120                     | nano120×48 cluster  |
|------------------------|------------------------------|-----------------------------|---------------------|
| Frequency              | 1700MHz                      | 100MHz                      | 1152MByte           |
| Bus bandwidth          | 1600MByte                    | 50MByte                     | 1152MByte           |
| Floating point capability | 95,000Mflops                 | about 200Kflops             | 4.8Mflops           |
| Threads                | 1                            | 1                           | 48                  |
| Task switching         | Time-sharing                 | Interrupt routine           | Parallel            |
| Software structure     | Sequence                     | Sequence                    | Parallel            |

It can be seen that the advantages of the cluster are in the number of threads and parallel structure. The parallel structure can really achieve simultaneous multi-task promotion. In the parallel structure, the cost of switching between tasks is only 10 to 100 machine cycles. It occupy only a few microseconds on the 100MHz frequency processor and tasks can be switched at any time. While the Windows operating system allocates task time slices in units of 1 millisecond, it takes at least 1 millisecond for one task to wait for signals of another task without blocking. If the computer
frequently switch blocking tasks (for example, using pipes or semaphores), it will increase processor spending for thread context switching. For a 100MHz nano120 processor, 1 millisecond is sufficient to complete 100,000 single-cycle arithmetic instructions. Therefore, the cluster can achieve high task interaction efficiency and extremely high task intensiveness, which is unmatched by single-processor systems.

The experimental environment is shown in Fig8. The signal is instructed by the host to randomly select the ECG data in the database, and then send it to the laptop and the microprocessor cluster through the network and the USB interface respectively for calculation. After the calculation is completed, the completion time and calculation accuracy of each task are counted. A total of 1000 sets of ECG data tests were performed. Count the completion time of each task in each of the two systems and plot them as scatter plots as shown in Fig9. The total task completion time and accuracy are shown in Table 2.

![Figure 8. Performance Comparison Test Environment.](image)

![Figure 9. Task Completion Time.](image)

It can be seen from Fig9 that due to the high degree of parallelism of computing tasks in the microprocessor cluster, the main control processor can terminate the calculation processes that will inevitably fail to obtain the optimal solution. Therefore, the time distribution of the calculation process is very large. In the laptop computer, due to its sequential calculation structure, the probability of interrupting the calculation halfway is much less. From Table 2, it can be seen that the nano120 clusters uses 15% less time than the i5-3317 processor.

| Compare items         | i5-3317 | Nano120 × 48 Clusters |
|-----------------------|---------|-----------------------|
| Total time            | 5257.9 S| 4469.2 S              |
| Average accuracy      | 76.17%  | 71.25%                |

Table 2. Total task completion time and accuracy statistics.

If we further compare the power consumption and hardware cost of the two, as shown in Table 3, we can see that the nano120 cluster has great advantages in cost and power consumption. In contrast, the price paid for software modification is worth it.
4. Conclusion
The microprocessor cluster introduced in this paper has a good price-performance ratio. With the development of wearable technologies, such microprocessors will become cheaper, more power-efficient, smaller, and even can be embeded into sensors and signal cables and will become the mainstream hardware platform for wearable devices. This article introduces the hardware and software design method of the microprocessor cluster and proves that the cluster has good performance in ECG calculation tasks.

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