Interface properties study on SiC MOS with high-k hafnium silicate gate dielectric
Lin Liang, Wei Li, Sichao Li, Xuefei Li, and Yanqing Wu

Citation: AIP Advances 8, 125314 (2018); doi: 10.1063/1.5051615
View online: https://doi.org/10.1063/1.5051615
View Table of Contents: http://aip.scitation.org/toc/adv/8/12
Published by the American Institute of Physics

Articles you may be interested in
High-performance transistors based on monolayer CVD MoS2 grown on molten glass
Applied Physics Letters 113, 202103 (2018); 10.1063/1.5051781
Interface properties study on SiC MOS with high-κ hafnium silicate gate dielectric

Lin Liang, 1 Wei Li, 2 Sichao Li, 1 Xuefei Li, 1 and Yanqing Wu 1,a

State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China

School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, China

(Received 10 August 2018; accepted 16 November 2018; published online 6 December 2018)

High κ dielectrics, such as Al₂O₃, has attracted increasing research attention for its use as the gate dielectric of 4H-SiC MOS capacitors. Since the dielectric constant of Al₂O₃ is not high enough, many other high-κ dielectrics are actively explored. In this letter, a report of the interface properties of 4H-SiC MOS capacitors with Hafnium silicate (HfSiOₓ) dielectric is presented. The HfSiOₓ dielectric was deposited by thermal atomic layer deposition. A systematic study of I-V and multi-frequency C-V characteristics were carried out and the results showed HfSiOₓ gate dielectric could effectively increase dielectric constant. A thin layer of SiO₂ in between SiC and high κ dielectric can further improve interface properties. These results indicate that HfSiOₓ could be a promising candidate as suitable gate dielectric material for future 4H-SiC MOS capacitors and MOSFETs. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).

Silicon carbide (SiC) is a wide bandgap semiconductor which holds great promise for next-generation power devices. Due to its wide bandgap, high breakdown field strength and high thermal conductivity properties, 4H-SiC has a great advantage compared with conventional silicon on power electronics targeting high power, high temperature and high working frequency applications. However, there is a severe problem with the dielectric stability at high electric field. Since the dielectric constant of SiC is much higher than that of SiO₂, the electric field in SiO₂ is always much higher than that of SiC, especially when it reaches the critical field of SiC at 3 MV/cm, which will lead to a severe reliability problem for the SiO₂ dielectric. High κ dielectrics can be applied on SiC to alleviate the electric field in the gate dielectric and some example high κ materials are Al₂O₃, HfO₂, AlON and La₂O₃. A study with Al₂O₃ as the gate dielectrics was taken and it showed using Al₂O₃ could increase the dielectric constant, thus improving the stabilities of the gate dielectric of SiC MOS capacitors. Gate dielectric with even higher dielectric constant such as Hf-based HfSiOₓ is expected to improve the performance further.

In this letter, all the MOS capacitors were fabricated by using a commercial n-type 4H-SiC (0001) substrate (4° off-axis) with an n-type doping level of 8×10¹⁵ cm⁻³. Each sample was cleaned by a standard RCA cleaning process, followed by a dip of 60s in diluted BOE to remove the native oxide. After the cleaning, 20nm HfSiOₓ was deposited by atomic layer deposition (ALD). HfSiOₓ dielectric was deposited at 300 °C with Tetrakis (dimethylamino) hafnium, Tris (dimethylamino) silane and ozone as precursors. The XPS and X-ray powder diffraction (XRD) data of the film are shown in Figure 1. The molar concentration of SiO₂ within the HfO₂ host lattice is ~ 4 %. Then these samples were thermally annealed in oxygen atmosphere at various temperatures for 30 minutes. After that, 20 nm Ni and 50 nm Au layers were deposited by e-beam evaporation as contact pads as shown in Figure 2. Finally, electrical measurement of C-V and I-V characteristics of these devices was carried out by using the Agilent B1505.
As can be seen from Figure 3, it could be found that the annealing temperature affects not only the flatband voltage shift, but also the threshold voltage. It is clear to see the $900^\circ C$ to $950^\circ C$ is the optimized temperature range for annealing from the flatband voltage shift. The $k$ can be calculated by the equation

$$C = \frac{k\varepsilon_0S}{t_{ox}}$$

where $C$ is the gate oxide capacitance of C-V curves measured at 1 MHz, $t_{ox}$ is the thickness of gate dielectric (20 nm), and $S$ is the area of MOS capacitor. As shown in Figure 4(a), the dielectric constant changes with different annealing temperature, and reaches the peak values at around $850^\circ C$. Figure 4(b) shows the flatband voltage shift at different annealing temperatures. It could be clearly found that the devices annealed at temperature from $900^\circ C$ to $950^\circ C$ in oxidation atmosphere have the lowest flatband voltage shift. High temperature annealing can significantly reduce the negative
charges located at near interfaces and in the oxides. Therefore, the flatband voltage decreases from 800 to 950 °C. The higher temperature could cause the formation of SiO$_x$ interfacial layer, resulting in the increase in the flatband voltage.

The effective trapped charge density $N_{it}$ is defined by the equation\textsuperscript{12}

$$N_{it} = \frac{\Delta V_{fb} \times C_{ox}}{q} \quad (2)$$

where $C_{ox}$ is the gate dielectric capacitance per unit area. The devices annealed at 925°C exhibit a very low trapped charge density of $4.26 \times 10^{10} \text{ cm}^{-2}$. Figure 4(c) shows the frequency dispersion $H_{fd}$ reduced drastically from 850 °C and above, also indicating a low density of interface trap.

Taking into all the factors including $k$, $\Delta V_{fb}$, $N_{it}$ and frequency dispersion, the overall optimized performance can be obtained at around 925°C annealing temperature for the HfSiO$_x$/4H-SiC MOS capacitors. All the results were shown in Table I.

However, it is noted that there is still room for further improvement in frequency dispersion. Previous studies show that a thin layer of SiO$_2$ deposited between 4H-SiC and high $k$ dielectric can improve the interface quality, compensate the low band offset and block the electron injection into SiC layer, decreasing the leakage current and interface trap density.\textsuperscript{13,14} Therefore, some supplemental experiments were carried out.

After cleaning the 4H-SiC epi wafers, a thin SiO$_2$ layer with the thickness of 5 nm was grown at 1050°C in thermal dry oxidation atmosphere. Then 20 nm HfSiO$_x$ layer was deposited on SiO$_2$. 

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|}
\hline
Dielectric material & $k$ & $\Delta V_{fb}$ (V) & $H_{fd}$ (%) \\
\hline
HfSiO$_x$ & 12.8 & 0.12 & 3.87 \\
\hline
\end{tabular}
\caption{The properties of SiC MOS capacitors with HfSiO$_x$ dielectric annealed.}
\end{table}
layer at 300°C by ALD. After that, the samples with HfSiO<sub>x</sub>/SiO<sub>2</sub> dielectrics were annealed in dry oxidation atmosphere. Finally, 20 nm Ni and 50 nm Au layer were deposited on these caps.

Figure 5(a) shows the frequency dispersion of SiC MOS capacitors with HfSiO<sub>x</sub>/SiO<sub>2</sub> dielectric annealed at different temperature. Again, the annealing temperature of 925°C shows the best performance. It acquires the lowest frequency dispersion and the best uniformity. The calculated result of
frequency dispersion is 1.58%, which is lower than half of the value for the sample without SiO$_2$ layer, as shown in Table I. Figure 5(b) shows the C-V curves of the SiC MOS capacitors with HfSiO$_x$/SiO$_2$ dielectric annealed at 925 °C. As expected, the calculated result of $k$ of this composition layer is around 10, lower than the value with HfSiO$_x$ single layer. The I-V characteristics were also tested for comparison, as shown in Figure 6(a). It can be seen that the gate leakage current density is much lower with the thin layer of SiO$_2$ in between. The curve of current density vs electric field (J-E) was also plotted in Figure 6(b). A transmission electron microscope (TEM) image is taken in Figure 7 to show the interface of the HfSiO$_x$/SiO$_2$/SiC structure.

In summary, we have reported the interface properties of SiC MOS with HfSiO$_x$ gate dielectric. The high $k$ material HfSiO$_x$ has enhanced the gate dielectric constant dramatically, and therefore lower electric field could be acquired in the dielectric layer and higher long-term reliability for the SiC MOSFET could be expected. In order to improve the interface quality in further, a thin layer of SiO$_2$ with about several nanometers is proved to be necessary by experiment.

This work was supported by State Key Laboratory of Advanced Electromagnetic Engineering and Technology (Huazhong University of Science and Technology) (2016KF004) and the Key Basic Research Program of Hubei Province under Grant 2017AAA127.

1 C. E. Weitzel, J. W. Pulmour, C. H. Carter, K. Moore, K. J. Nordquist, S. Allen, C. Thero, and M. Bhatnagar, IEEE Trans. Electron Devices 43, 1732 (1996).
2 L. M. Lin and P. T. Lai, J. Appl. Phys. 102, 054515 (2007).
3 W. Yi-Yu, S. Hua-Jun, B. Yun, T. Yi-Dan, L. Ke-An, L. Cheng-Zhan, and L. Xin-Yu, Chin. Phys. B. 22, 078102 (2013).
4 C. M. Tanner, Y. C. Perng, C. Frewin, S. E. Saddow, and J. P. Chang, Appl. Phys. Lett. 91, 203510 (2007).
5 V. V. Afanas’ev, A. Stesmans, F. Chen, S. A. Campbell, and R. Smith, Appl. Phys. Lett. 82, 922 (2003).
6 P. M. Gammon, A. Pérez-Tomás, M. R. Jennings, O. J. Gay, N. Rimmer, J. Llobet, N. Mestres, P. Godignon, M. Placidi, M. Zabala, J. A. Covington, and P. A. Mawby, Appl. Phys. Lett. 97, 013506 (2010).
7 Q. Chen, Y. P. Feng, J. W. Chai, Z. Zhang, J. S. Pan, and S. J. Wang, Appl. Phys. Lett. 93, 052104 (2008).
8 H. Watanebe, T. Kirino, Y. Uenishi, A. Chanthaphan, A. Yoshigoe, Y. Teraoka, S. Mitani, T. Nakamura, T. Hosoii, and T. Shimura, ECS Trans 35, 265 (2011).
9 B. Lee, S. R. Novak, D. J. Lichtenwalner, X. Yang, and V. Misra, IEEE Trans. Electron Devices 58, 3106 (2011).
10 X. Yang, B. Lee, and V. Misra, IEEE Electron Device Lett. 36, 312 (2015).
11 L. Liang, W. Li, S. Li, X. Li, and Y. Wu, ICSICT, 2016 13th IEEE International Conference on. IEEE, 1378 (2016).
12 R. Mahapatra, A. K. Chakraborty, A. B. Horsfall, S. Chattopadhyay, N. G. Wright, and K. S. Coleman, Appl. Phys. Lett. 102, 024105 (2007).
13 R. Mahapatra, N. Poolamai, S. Chattopadhyay, N. G. Wright, A. K. Chakraborty, K. S. Coleman, P. G. Coleman, and C. P. Burrows, Appl. Phys. Lett. 88, 072910 (2006).
14 L. M. Lin and P. T. Lai, J. Mater. Sci.: Mater. Electron. 19, 894 (2008).