Abstract—Guessing Random Additive Noise Decoding (GRAND) is a recently proposed universal decoding algorithm for linear error correcting codes. Since GRAND does not depend on the structure of the code, it can be used for any code encountered in contemporary communication standards or may even be used for random linear network coding. This property makes this new algorithm particularly appealing. Instead of trying to decode the received vector, GRAND attempts to identify the noise that corrupted the codeword. To that end, GRAND relies on the generation of test error patterns that are successively applied to the received vector. In this paper, we propose the first hardware architecture for the GRAND algorithm. Considering GRAND with ABandonment (GRANDAB) that limits the number of test patterns, the proposed architecture only needs $2 + \sum_{i=2}^{n} \left\lfloor \frac{i}{2} \right\rfloor$ time steps to perform the $\sum_{i=1}^{n} \binom{n}{i}$ queries required when $AB = 3$. For a code length of 128, our proposed hardware architecture demonstrates only a fraction (1.2%) of the total number of performed queries as time steps. Synthesis result using TSMC 65nm CMOS technology shows that average throughputs of 32 Gbps to 64 Gbps can be achieved at an SNR of 10 dB for a code length of 128 and code rates rate higher than 0.75, transmitted over an AWGN channel. Comparisons with a decoder tailored for a (79,64) BCH code show that the proposed architecture can achieve a slightly higher average throughput at high SNRs, while obtaining the same decoding performance.

Index Terms—Error correcting code (ECC), guessing random additive noise decoding (GRAND), maximum likelihood decoding (MLD), VLSI architecture.

I. INTRODUCTION

Since the landmark paper by Shannon [1] in 1948, one of the goal of researchers in the field of information theory was to find good error correcting codes that can be efficiently decoded. As soon as 1950, Hamming proposed his eponymous codes that can always correct one error [2]. Ten years later, BoseChaudhuriHocquenghem (BCH) codes [3], [4] were discovered. They have the pleasant property that the number of correctable errors is chosen by design. To find the locations of the errors, two main algorithms can be considered: the BerlekampMassey algorithm [5], [6] or the Peterson-GorensteinZierler (PGZ) algorithm [7]. After major advances and rediscoveries in the 90’s, polar codes were proposed in 2008 along with their decoding algorithm called successive cancellation (SC) algorithm [8]. This is the first proven class of codes that asymptotically reaches the Shannon limit. Serially concatenated with an outer cyclic redundancy check (CRC) code [9], polar codes have been selected as part of the 5G New Radio (NR) standard [10]. All of these algorithms require devoted decoding techniques, and a decoder tailored for a decoding algorithm cannot be directly utilized for another one.

Recently, a universal decoding algorithm for linear codes has been proposed [11]. Named Guessing Random Additive Noise Decoding (GRAND), the algorithm does not rely on the underlying channel code. Instead of using the properties and the structure of the code to identify the errors that may occur at the reception due to the channel noise, GRAND guesses the noise present in the received vector. In other words, GRAND is noise-centric rather than being code-centric and is able to tackle any aforementioned coding schemes that have been developed over the course of information theory. GRAND is not the only decoding algorithm that is code agnostic. However, considering high rate codes, GRAND has a lower computational complexity than a brute-force search [11], or does not require the costly Gaussian elimination required for information set decoding [12]. The Gaussian elimination is also required for random linear network coding [13] and GRAND could be an efficient way to reduce the computational complexity of this powerful encoding scheme. In addition, an approach similar to GRAND has been used to lower the error floor of turbo codes in [14], which could lead to the use of GRAND in conjunction with usual decoding techniques.

To identify the noise, GRAND has three main steps. First, error patterns are generated in a specific order. Then, the error patterns are combined with the received vector, and finally, queries for codebook membership on the resulting words are realized. Generating all the possible error patterns is impractical and unwanted. Thus, GRAND with ABandonment (GRANDAB) has been also proposed to limit the number of queries performed during the process [11].

In [15], the application of GRANDAB for short length and high rate CRC-polar codes encountered in the 5G NR standard has been demonstrated. Considering a code of length 128 and up to 3 errors, a maximum number of 349,632 queries may be required. However, it has been observed that the average number of queries are much smaller than the worst-case scenario for practical signal-to-noise ratio (SNR) conditions. Thus, GRANDAB offers a high throughput with an average low latency at moderate-to-high SNR regimes, and tailored for high code rates, both of which are particularly crucial for ECC storage applications.

In [16] and in [17], GRAND is enhanced to consider soft-information at its input. Impressively decoding performance is achieved, where substantial gains over the SC-List [18] are presented. However, we limit the scope of this work to hard
input decoding.

In this paper, we propose a high throughput hardware architecture for GRANDAB. To this end, we first show how to share computations required by the GRAND algorithm, using basic linear algebra. Then we propose an efficient hardware exploiting the proposed sharings. To the best of our knowledge, this is the first hardware architecture implementing the GRAND algorithm. Considering a code of length 128, and with a correction capability of up to three errors, the proposed architecture can achieve an average coded throughput of up to 64 Gbps. Moreover, the proposed architecture can achieve the same average throughput as a recently proposed decoder that can only consider a (79, 64) BCH code.

The rest of this work is organized as follows: In Section II, preliminaries regarding linear codes and GRAND algorithms are given. In Section III, the proposed hardware architecture is detailed. Synthesis results and comparison with a state-of-the-art decoder for BCH code are given. Finally, concluding remarks are drawn in Section V.

II. PRELIMINARIES

A. Notations

Matrices are denoted by a bold upper-case letter \( (M) \), while vectors are denoted with bold lower-case letters \( (v) \). The transpose operator is represented by \(^\top\). The number of \( k \)-combinations from a given set of \( n \) elements is noted by \( \binom{n}{k} \). \( \mathbf{1}_n \) is the indicator vector where all locations except the \( n^{th} \) are 0 and the the \( n^{th} \) is 1. All the indices start at 1.

B. Linear block codes

Due to their convenient representations, linear block codes are a class of error-correcting codes widely adopted by communication standards. In the following, we restrict ourselves with operations in the Galois field with 2 elements, noted \( \mathbb{F}_2 \). A block code is a mapping \( g : \mathbb{F}_2^k \rightarrow \mathbb{F}_2^n \), where \( k < n \). This way, a vector \( u \) of size \( k \) maps to a vector \( c \) of size \( n \). The set of the \( 2^k \) vectors \( c \) is called a code \( C \), whose elements \( c \) are called codewords. The ratio \( R \triangleq \frac{k}{n} \) is the code rate. If \( g \) is a linear mapping, then \( C \) is a linear block code. Thus, there exists a \( k \times n \) matrix \( G \) called generator matrix of the code \( C \). Then, the encoding process can be realized as a vector-matrix product: \( c = u \cdot G \). We can define \( H \), the \( (n-k) \times n \) generator matrix of the dual code of \( C \). \( H \) is also called the parity-check matrix of \( C \) and verifies the following property:

\[
\forall \ c \in C, \ H \cdot c^\top = 0. \tag{1}
\]

Consider that \( e \) has been transmitted over a noisy channel and that \( r \) is received at the output of the channel. Because of the channel noise, \( r \) can differ from \( c \). Therefore, we can establish the relationship between \( r \) and \( c \) as: \( r = c \oplus e \), where \( e \) is the error pattern caused by the channel noise. The syndrome is defined by \( s \triangleq H \cdot r^\top \). According to (1), \( s \) is zero if and only if \( r \) is a codeword. Thus, if \( s \) is zero either there is no error or the error pattern is itself a codeword. This is the basic principle for standard array decoding [19], and also for GRAND.

Algorithm 1: GRAND for linear codes

| Input: \( H \), \( G^{-1} \), \( r \) |
| Output: \( \hat{u} \) |
| 1 \( e \leftarrow 0 \) |
| 2 while \( H \cdot (r \oplus e)^\top \neq 0 \) do |
| 3 \( e \leftarrow \text{generateNewErrorPattern()} \) |
| 4 \( \hat{u} \leftarrow (r \oplus e) \cdot G^{-1} \) |
| 5 return \( \hat{u} \) |

C. Maximum Likelihood Decoding via GRAND

Guessing Random Additive Noise Decoding (GRAND) is a recently proposed hard detection decoder that has been proven to be a maximum likelihood (ML) decoder [11]. Algorithm 1 summarizes the steps of the GRAND procedure. The principle of GRAND is to generate test error patterns, to apply them to the received vector, and to check if the generated candidate is a codeword by verifying that

\[
H \cdot (r \oplus e)^\top = 0 \tag{2}
\]

is equal to zero. If so, \( \hat{c} \triangleq r \oplus e \) is the estimated codeword. To perform a proper decoding, \( \hat{c} \) has to be converted into the estimated message: \( \hat{u} \triangleq \hat{c} \cdot G^{-1} \), where \( G^{-1} \) is the \( n \times k \) matrix such that \( G \cdot G^{-1} \) is the identity matrix of size \( k \). Note that this step is not required for systematic codes, since the message bits directly appear in the codeword.

The most important property of GRAND is that it requires no other condition on the code except the linearity. Thus, GRAND can be considered for any linear code if only the parity check matrix \( (H) \) is provided. To the best of our knowledge, the only other decoders that can decode any linear code are the brute-force ML decoder and the information set decoding [12], or its more recent version known as ordered statistic decoding [20]. However, the ML decoder is impractical for high-rates codes since the \( 2^k \) codewords have to be evaluated, while the two others require Gaussian elimination, which is challenging to efficiently implement in hardware [21].

D. GRAND with Abandonment

To limit the computational complexity of the GRAND algorithm, GRAND with ABandonment (GRANDAB) is also proposed in [11]. In that case, the decoder abandons the search for the error pattern after a fixed number of queries is reached. Therefore, GRANDAB results in an approximated ML decoding. The notation GRANDAB with \( AB = t \), means that the Hamming weight of the considered error patterns do not exceed \( t \). As a result, the maximum number of queries for a code of length \( n \) is given by

\[
\sum_{i=1}^{t} \binom{n}{i}. \tag{3}
\]

For an illustrative purpose, Fig. 1 compares the frame error rate (FER) performance obtained with GRANDAB \( AB = 3 \), using CRC codes with different rates \( (R \geq 0.75) \). All
codes have a length $n$ of 128. The generator polynomials are 0x04c11db7, 0xb2b117, 0x1021, and 0xd5 for $k = 96$, $k = 104$, $k = 112$, and $k = 120$, respectively. A BPSK modulation and an AWGN channel with variance $\sigma^2$ are considered. The SNR in dB is defined as $\text{SNR} = -10 \log_{10} \sigma^2$. The demodulator provides hard decisions to the GRANDAB decoder. Observe that the FER performance improves with the number of redundancy bits, up to the case CRC(128,104). Considering more redundancy bits does not improve the decoding performance since the considered version of GRANDAB cannot correct more than 3 errors. Nevertheless, GRANDAB is an effective way for decoding any code, especially compared to its high-complexity agnostic hard decoder counterparts, for which an impractical number of computations are required. With $n = 128$ and $AB = 3$, a total number of 349,632 queries are required. Despite this large number of queries, targeting a FER of $10^{-4}$, the average number of queries become 445, 412, 4.58, and 1.01 for $k = 96$, $k = 104$, $k = 112$, and $k = 120$, respectively. This is another advantage of GRAND: the average computational complexity decreases sharply as channel conditions improve.

III. VLSI ARCHITECTURE FOR GRAND

In this section, we provide details of the proposed VLSI architecture for GRANDAB ($AB = 3$) decoding of linear codes. Since GRAND decoding is agnostic to the underlying channel code, the proposed VLSI architecture can be used to decode any linear block code conforming with the length and rate constraints, given the parity check matrix ($H$) of that code. Before presenting the details of our proposed VLSI architecture, we provide a minimal mathematical background—exploiting the linearity of the considered codes—required to simplify the problem.

A. Computations reformulation

For the one bit-flip error patterns $\mathbb{1}_i$, with $i \in [1 \ldots n]$ using the distributivity rule, (2) can be written as

$$H \cdot (r \oplus \mathbb{1}_i)^\top = H \cdot r^\top + H \cdot \mathbb{1}_i^\top,$$  

(4)

where $H \cdot r^\top$ is the $(n-k)$-bits syndrome associated with the received vector $r$ and $H \cdot \mathbb{1}_i^\top$ is the $(n-k)$-bits syndrome associated with the one bit-flip error pattern $\mathbb{1}_i$.

Noticing that the two bit-flips noise sequences $\mathbb{1}_{i,j}$, with $i \in [1 \ldots n]$, $j \in [1 \ldots n]$ and $i \neq j$, can be written as $\mathbb{1}_{i,j} = \mathbb{1}_i \oplus \mathbb{1}_j$, (2) can be expressed as

$$H \cdot (r \oplus \mathbb{1}_{i,j})^\top = H \cdot r^\top \oplus H \cdot \mathbb{1}_i^\top \oplus H \cdot \mathbb{1}_j^\top,$$  

(5)

for the two bit-flips case. Similarly, the three-bit-flips noise sequences $\mathbb{1}_{i,j,k}$, where $i$, $j$ and $k$ are the flipped bit positions, can be checked for code membership with

$$H \cdot (r \oplus \mathbb{1}_{i,j,k})^\top = H \cdot r^\top \oplus H \cdot \mathbb{1}_i^\top \oplus H \cdot \mathbb{1}_j^\top \oplus H \cdot \mathbb{1}_k^\top.$$  

(6)

Equations (4)-(6) are the core of the proposed VLSI architecture. By combining several different one bit-flip noise sequence syndromes, it is possible to compute all the queries corresponding to several bit-flips. In the following, we denote by $s_i$ the syndrome corresponding to the one-bit-flip error pattern at location $i$: $s_i = H \cdot \mathbb{1}_i^\top$, which also corresponds to the $i^{th}$ column of the parity check matrix.

B. Principle, Details and Scheduling

The scheduling of the proposed architecture comprises four fundamental decoding steps. In the first one, the syndrome of the received word is computed ($H \cdot r^\top$). In the second step, all the error patterns with a Hamming weight of 1 are independently combined with the syndrome of the received word. In the third and fourth steps, Hamming weights of 2 and 3 are considered, respectively. During the iterations of any of the described steps, when (2) results in a zero, the corresponding estimated word is the output and the procedure is terminated. To efficiently generate the different error patterns, the proposed architecture is based on what we call **dials**.

A dial is a $n \times (n-k)$-bit register file which stores all the $n$ syndromes associated with the one-bit-flip error patterns ($s_i$). The dial has the ability to shift its content in a cyclic manner at each time step; i.e. when the content of the second row is shifted to the first row, the content of the first row is shifted to the last row. Moreover, during a cyclic shift, the content of the last row may be replaced by the $(n-k)$-bit wide null vector. This operation is called **shift-up**. After a shift-up operation has taken place, the following cyclic shifts
exclude rows containing null vectors. Note that a dial works in conjunction with an index dial, a \( n \times \log_2 n \)-bit cyclic shift register file, which performs the same operations (cyclic shift or shift-up) to keep track of the indices \( i \) in \( s_i \). As explained later, only 2 dials are used in the proposed architecture.

For checking the one-bit-flip error patterns, the content of the dials is depicted in Fig. 2. By combining each row of the dials with the syndrome of the received vector, we can compute (4) in one time step. Fig. 3(a) shows the content of the dials at the first time step when checking for the two-bit-flips error patterns: the content of the dial 2 is the image of dial 1 cyclically shifted by one. By combining each row of the dials with the syndrome of the received vector, we can compute (4) in one time step. At the next time step, the content of the dial 2 is cyclically shifted by one as shown in Fig. 3(b). Observing that \( \mathbb{I}_{i,j} = \mathbb{I}_{j,i} \), all the \( \binom{n}{2} \) two-bit-flips error patterns are tested for code membership after a total of \( \lfloor \frac{n}{2} \rfloor - 1 \) cyclic shifts from the original setting (Fig. 3(a)). Hence, a total of \( \lfloor \frac{n}{2} \rfloor \) time steps are required to compute (5). Note that to keep track of the indexes, whenever a dial is rotated, its corresponding index shift register (index dial) is also rotated.

Regarding the three-bit-flips error patterns, we show that only two dials can be used. Indeed, if three dials are considered, the scheduling and the associated hardware become more complex to avoid error pattern duplications. Instead, a controller is used in conjunction with the dials to generate the test patterns. The controller takes care of the first bit-flip, while the dials are responsible for considering the other bit-flips. Fig. 4(a) shows the content of the dials and the syndrome output by the controller to generate \( n - 1 \) three-bit-flips error patterns at time step 1. To do so, the dial 1 is shifted-up by 1, while the dial 2 is shifted-up by 1 and cyclically shifted by 1 at the initialization. In the next time step, the dial 2 is cyclically shifted by 1 to generate the next \( n - 1 \) three-bit-flips noise sequences as shown in Fig. 4(b). After \( \lfloor \frac{n-1}{2} \rfloor \) time steps all the \( \binom{n-1}{3} \) three-bit-flips error patterns with \( s_1 \) are generated. In the next time step, the controller outputs \( s_2 \) while the dial 1 is shifted-up by 1 and the dial 2 is reset, shifted-up by 2 and cyclically shifted by 1. This generates \( n - 2 \) three-bit-flips error patterns, as shown in Fig. 4(c). In the next time step, the dial 2 is cyclically shifted by 1, allowing to generate the next \( n - 2 \) three-bit-flips error patterns as shown in Fig. 4(d). Hence, \( \lfloor \frac{n-2}{2} \rfloor \) time steps are used to generate all the \( \binom{n-2}{3} \) three-bit-flips error patterns with \( s_2 \) set and \( s_1 \) excluded. Similarly, this process is repeated until \( s_{n-2} \) is output by the controller, where only one three-bit-flips error pattern is generated: \( H \cdot r^\top \oplus H \cdot s_{n-2} \oplus H \cdot s_{n-1} \oplus H \cdot s_n \). Finally, checking all the three-bit-flips error patterns requires \( \sum_{i=2}^{n-1} \lfloor \frac{i-1}{2} \rfloor \) time steps.

In summary, the number of required time steps to check all the error patterns with Hamming weights of 3 or less is given by:

\[
2 + \sum_{i=2}^{n} \left\lfloor \frac{i}{2} \right\rfloor.
\] (7)

Using some mathematical manipulation, the ratio between (3) and (7) – that expresses the parallelization factor – can be approximated by \( \frac{\log_2 n}{\log_2 (n/2)} \). Thus, the longer the code, the higher the savings compared with a conventional and serial approach.

The proposed hardware architecture for the GRANDAB algorithm with \( AB = 3 \) is shown in Fig. 5. Its input is the hard decision vector \( r \) of length \( n \) and its output is the estimated word \( \hat{u} \), padded with zeros to match the length of \( n \). For the sake of clarity, the control and clock signals are omitted in the Figure. At any time, to support any code given the length and rate constraints, an \( H \) matrix can be loaded. The data path consists essentially of the interconnection through \( 2 \times n + 1 \).
(n – k)-bit-wide XOR gates of the dials, the syndrome of the received word, and the syndrome provided by the controller (2 x n for the dials and 1 for the controller), as described in the previous paragraphs. Each of the n test syndromes is NOR-reduced, to feed an n-to-log2 n priority encoder. The output of each NOR-reduce is 1 if and only if all the bits of the syndrome computed by (2) are 0. The output of the priority encoder controls two multiplexers, used to forward the indices associated with the valid syndrome to the word generator. Finally, the word generator combines the hard decision vector r and the three indices to produce the estimated codeword, which is translated into the estimated word and outputted.

IV. IMPLEMENTATION RESULTS

The proposed architecture has been implemented in Verilog HDL and synthesized using the Synopsys Design Compiler version P-2019.03 with TSMC 65nm CMOS technology. The design has been verified using test benches generated via the bit-true C model of the proposed hardware.

Table I presents the synthesis results for the proposed decoder with n = 128, AB = 3 and a code rate between 0.75 and 1. Thus, the length of the syndromes is constrained to the interval [0 .. 32]. The implementation can support a maximum frequency of 500 MHz. No pipelining strategy is used, therefore one clock cycle corresponds to one time step. Using (7), 4098 cycles are required in the worst-case (W.C.) for decoding a 128-length code. Recall that GRANDAB (AB = 3) requires a total number of 349 632 queries for decoding any code of length 128. Hence, our proposed VLSI architecture demonstrates only a fraction (1.2%) of the total number of performed queries as latency. With a frequency of 500 MHz, the proposed architecture results in a worst-case information throughput (W.C. T/P) of 11.71 to 14.64 Mbps for the CRC codes considered in Section II-D. However, the average latency is much shorter than the worst-case latency, especially in the mid-to-high SNR region. Using the bit-true model, the average latency is computed after considering at least 100 frames in error for each SNR points. Fig. 6(a) depicts the average latency for the considered codes. Irrespective of the code rate, we can see that the average latency reduces when the channel condition becomes better, up to the point where the average latency reach only 1 cycle per decoded codeword. The counterpart of the latency, the throughput, is given in Fig. 6(b). Observe that the information throughput grows with the SNR up to reaching the values of 48 Gbps to 60 Gbps, according to the code rate. In addition, considering an FER of 10^-4, average information throughputs of 9 Gbps, 9 Gbps, 56 Gbps and 60 Gbps are obtained for the information lengths of 96, 104, 112, and 120, respectively.

To the best of our knowledge, there is no hardware implementation of a hard detection decoder in the literature that achieves the same code flexibility as our proposed architecture. Thus, performing a fair comparison is difficult. However, we propose to compare it with a state-of-the-art hard decision algebraic decoder. Recently, a high throughput VLSI architecture based on the PGZ algorithm for a (79, 64) BCH code decoder has been proposed [22]. Since up to 2 errors can be corrected with this decoder, GRANDAB with AB = 2 is enough to achieve the same decoding performance. Therefore, we re-synthesized our architecture by limiting n to 79 and by setting AB = 2. Hence, a total of 1+1+[79/2] = 41 time steps are required to decode any code of length 79 with at most 2 errors.

Table II compares the implementation results of the GRANDAB (AB = 2) decoder and the BCH decoder in [22]. The proposed decoder is 41 x larger and has 13.6 x higher worst-case latency. On the other hand, the average latency of the two decoders are equivalent at an SNR of 10 dB. At higher SNRs, the proposed decoder exhibits a slightly better minimum latency and achieves an information throughput of 64 Gbps, while the BCH decoder is limited to 58 Gbps. Finally, while [22] can only decode the (79, 64) BCH code, the proposed GRANDAB (AB = 2) can decode any code with n = 79 and R ≥ 0.75.

V. CONCLUSION

In this paper, we proposed the first hardware architecture for the GRANDAB algorithm. The decoding algorithm has the uncommon property of being able to decode any linear code. By using linear algebra basics, we were able to decompose the computations of the GRAND algorithm to improve the inherent parallelism. By doing so, the proposed hardware architecture can accomplish 349 632 queries in 4098 time steps. ASIC synthesis results showed that an average information throughput of at least 9 Gbps can be achieved with a block length of 128 when a FER of 10^-4 is targeted. Moreover, the average throughput increases when the channel conditions be-
come better. Hence, the average coded throughput for the same parameters can reach up to 64 Gbps. Finally, the architecture can achieve the same average throughput as a BCH decoder tailored for a (79, 64) code. The proposed architecture paves the way for future implementation of the GRAND algorithm that can consider soft information as their inputs.

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