Understanding the Limits of Conventional Hardware Architectures for Deep-Learning

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Abstract—Deep learning and hardware for it has garnered immense academic and industry interest in the past 5 years – including almost 100 startups, more than $5B of VC investment – and a re-relevance of the role of architecture. However, the state-of-art remains NVIDIA's TensorCore-based systems that provide i) top-of-line performance, ii) turnkey software stack, and iii) coverage across a wide-spectrum of DL network styles (DL-architecture in AI parlance). Other academic and industry efforts have included novel approaches like spatial dataflow, CGRAs, systolic arrays, blended FPGA LUTs with fixed function units and more. These have all necessitated their own innovations in architecture, compiler, and software stack integration. However, none of these have yet satisfied all the 3 metrics that NVIDIA's TensorCore and software stack provides, and generally seem to perform worse. In this paper, we systematically investigate the behavior of DL workloads and imputed needs on hardware/compiler/software. We show that SIMD/short-vector, caching, and synchronization in a fairly well-understood multicore chip organization we call UPCYCLE can achieve day-zero software maturity, and provide big integer factor speedups over the state-of-art NVIDIA solutions. Compared to an A100, UPCYCLE at small-batch size is geo-mean 7.7X faster for inference, geo-mean 11.7X faster at training, while consuming only half the power. Second, the UPCYCLE architecture requires no new compiler or software stack innovation. Third, it provides full DL-architecture coverage, and can be instantiated to provide training-optimized, inference-optimized, or balanced training and inference systems. Overall, this paper motivates the treatment of software maturity as a first class design constraint in developing new architectures for DL.

I. INTRODUCTION

Deep Learning (DL) is one of the hottest topics in computing today, and its need for compute is insatiable. Many chips are being built to meet this need: most cloud-service providers are building their own chips, as are companies like Tesla and GM/Cruise for their vertical uses, and over 100 startups.

Many styles of architecture are being explored: GEMM acceleration (TensorCore from NVIDIA, Matrix Core from AMD, CGRA (many startups), systolic arrays (Google TPU), dataflow (Wave, Blaize, Graphcore and other startups), FPGA (LUT-based Xilinx, Versal, Systolic-array-based Lattice), spatial dataflow (SambaNova, Groq), other (Qualcomm AI-100, Inferentia - design details sparse) including some delineating of training vs inference, and within that support for particular types of DNNs (CNN, LSTM, GNNS etc.). All but NVIDIA and Google TPU lack software maturity or usable software. This is evidenced by their inability (unwillingness) to run the MLPerf benchmark suite. While NVIDIA is able to run the entire MLPerf suite and much more, other companies have reported results only for Resnet. When results are reported, they far worse than NVIDIA’s A100 as shown in Table I. Another cohort of candidates are inference optimized chips (with some architectural handicaps hampering training capability) like Tenstorrent (some form of spatial dataflow) [19]; Groq (extreme slice-oriented spatial architecture, require extensive static scheduling) [17]; Qualcomm AI-100 (8-core DSP with very wide vectors per core) [18]; Baidu Kunlun [24]; Xilinx Versal (wide vectors added to FPGA), and Alibaba’s HanGuang [10]. Again, none of these have wide MLPerf coverage, largely run “just” Resnet50, and run at low chip utilization. An industry white-paper includes a summary assessment, “Challengers Struggle to Match Nvidia” and also comments on the need for mature software for architectures to be practical, which has proved a hindrance for these novel chip designs [20].

In summary, there are two glaring problems facing our community: i) lack of software maturity and ii) inefficiency of the current set of novel alternatives compared to GEMM acceleration.

On the purely academic side, full fledged ISAs and novel dataflow designs have been proposed. Examples of reconfigurable dataflow accelerators include [34], [38], Fused-layer CNN accelerator exploits fine-grained pipelined layer parallelism to minimize data movement of activations [12]. Kwon et al. describe heterogeneous dataflow accelerators [33]. All of these works sidestep the role of software and compiler, or require a new compiler. Typically a python graph to bare-metal object code flow is not demonstrated conceptually or in implementation. Further, none have demonstrated end-to-end application across the diverse MLPerf suite showing software readiness. This hardware-heavy and software-lite approach exacerbates industry’s lack of software readiness for AI hardware. Many modeling works have been published as well, including Timeloop [45] and Accelergy [59], which don’t focus on the role of architecture or explore the design space of uncore, memory bandwidth, application coverage, and software readiness. Other modeling works include SMAUG [60], DNNWeaver [51], DNNBuilder [62], MAGNet [50], Scale-SIM [49], HSIM-DNN [55], and MAESTRO [32]. SMAUG provides a detailed treatment on the differences between them.

In this work we focus on a key metric for accelerator platforms, software maturity, which we define as the existence of a mature software stack for a given platform which can

1In later Sections we delve into the details of A100 chip utilization showing an opportunity to substantially improve on it’s performance and energy efficiency, by improving utilization.
consume applications and produce high performance target code. NVIDIA's A100 GPU can be thought of as a canonical example of a DL accelerator which achieves software maturity. It is to be noted that libraries like cuDNN are over 10 years old, and NVIDIA has spent hundreds of millions of dollars, and hence many person-hours of engineering on CUDA during its lifetime [10]. No other academic example exists that is software mature. In this work, we investigate the following primary question: if software-maturity was considered the most important design constraint for a new accelerator, what does this imply about the architecture, microarchitecture, and achievable performance, power, and area across the space of DL applications. A secondary question is can we develop an architecture that is SW mature and substantially better than state-of-art DL hardware like NVIDIA A100. In particular, our goal is to explore an architecture for which additional compiler research or compiler development is not necessary. Whether or not a novel architecture can be made software mature in the future is orthogonal to this work.

Software maturity as a guiding principle is important for several reasons. First and foremost, without software, chips and hardware are useless and cannot be used by end users. Second, the hardware design cycle has become quite fast with chip-development cycles becoming more optimized – Google’s TPU [28] was built in 18 months from architecture concept/definition to silicon, Tesla’s FSD [3] took 14 months, and Google’s video coding unit (VCU) took just weeks before design verification was underway [47]. As the chip-development cycle tightens, the time pressure on developing software for these chips increases. Third, usable software/hardware combinations are necessary to amplify the effectiveness of systems as expounded by Hooker [22].

When examined through this lens, we find an intuitive and surprising result. Intuitively, a combination of short-vector processing, traditional caching and synchronization is sufficient for achieving software maturity, and high DL coverage. Surprisingly, this provides very high performance when compared to state-of-art software mature accelerators such as Nvidia’s A100 GPU (7.7X/11.7X speedup on small batch inference/training). Second, we are able to exceed the energy efficiency of GPUs by almost an order of magnitude. Finally, we uncover and plug the hole of very low utilization of GPUs. By revisiting and “upcycling” these old ideas, we construct UPCYCLE, an architecture designed specifically with software maturity in mind, and achieving this through composing well known architectural features for which decades of software and compiler work already exists. This paper is the first to systematically explore the different building blocks of compute, architectural storage/operand storage, memory hierarchy and bandwidth, communication primitives and interplay with parallelism in DL algorithms. While many novel micro/architecture investigations have been undertaken, such a treatment is surprisingly missing.

What’s not a focus of this work: For this work, we leave out other AI workloads like reinforcement learning, regression trees etc - although we hypothesize based on prior works in this area, the mechanisms and results in this work should generalize. Finally, the nature of the architecture allows us to naturally support traditional dense HPC and sparse HPC using techniques that have recently been developed by the GPU community [47].

The particular contributions of this paper are:

- A detailed qualitative and quantitative characterization of a broad set of DL applications and their imputed needs on the hardware/architecture. We evaluate 600+ different shapes of operators, across CNNs, Transformers, and LSTMs which as far as we know is the widest such study.
- A realizable architecture, UPCYCLE, designed from first principles and composed from well-known architectural features to be software mature for DL applications.
- A demonstration of how UPCYCLE can achieve software maturity through an in-depth exploration of DL algorithm mapping, focusing on the interplay between system design choices, and the precise mapping strategy needed to achieve high performance and utilization.
- An analysis across DL applications, comparing UPCYCLE to the NVIDIA A100 GPU which shows UPCYCLE achieves 7.7X/11.7X better performance for low batch size with 23X/35X better power efficiency for inference/training. Excluding the software-maturity framing, UPCYCLE is the best design for broad DL coverage.
- A systematic sensitivity study of performance on UPCYCLE to various design variables, which demonstrates balancing compute and memory hierarchy is important for end-to-end application gains.

The rest of this paper is organized as follows. Section II

### Table I

| Chip          | Resnet | Bert |
|---------------|--------|------|
| NVIDIA A100   | 1X     | 1X   |
| Google TPU    | 0.85X  | 0.65X|
| Habana        | 0.45X  | 0.25X|
| Huawei Ascend | 0.5X   | 0.35X|
| Xeon 8380H    | 0.05X  | -    |

All chips are roughly 300W. Data from MLPerf extracted as performance per-chip from an 8-chip system training time. For Google-TPU and Ascend data per chip is based on 64-chip system data reported.
provides a brief background and overview of deep-learning applications with a particular focus on distilling the differences and similarities between different DNNs, the role of “dense” layers, role of element-wise operators, training vs inference, and imputed needs on the architecture. Section III introduces the UPCYCLE architecture and describes the design space. Section IV describes software mapping, Section V describes our methodology for evaluation. Section VI presents results. Section VIII provides concluding thoughts.

II. BACKGROUND OF DEEP LEARNING APPLICATIONS

This section provides an overview of deep-learning applications with a particular focus on distilling the program behaviors and the imputed needs on the architecture.

A. A Deep Learning App (An Architect’s Perspective)

Most common deep learning applications are realized as a compute graph (Shown in Figure 2) consisting of nodes corresponding to well known operators and edges corresponding to operands between them, which are Tensors (with a shape and datatype). Operators combine learned variables with incoming data based on some mathematical operations. Examples include Matrix Multiply, Convolution, and Activation (Element-wise) functions. Nearly all DL apps today (including the ones in MLPerf) are implemented using frameworks such as Tensorflow, PyTorch and ONNX. These frameworks, in addition to providing implementations for operators, also provide automatic differentiation, which is used to compute gradients to each learned variable during training.

Tensor shape (dimensions), layout and datatype factor into the performance and efficiency of the application. Layout can be optimized with techniques presented in [45]. Datatype has some implications for the computer arithmetic portion of the architecture. For integer types, multiplication produces wider output than its input operands. For example, Intel’s recent AVX extensions support an Int8 to Int32 multiply-accumulate [11]. This impacts the design of an algorithm implementing a given operator since it has to be aware of this “wide-accumulate” detail. In short, it commonly amounts to tuning the tiling factors in a way that’s amenable to the input to accumulator size ratio and providing hardware support for accumulating and maintaining intermediates at a higher bit-widths than the inputs. On the hardware side Int8 to FP16 costs 3X in area, up to 5X in power, while Int8 to FP32 costs 10X to 20X in area and power [1], [14], [26], [61].

Execution. Often these applications exhibit statically determine dependencies between nodes of the graph, so graph nodes can simply be executed in topological order. Some applications, such as RNN-T, have dynamic control flow, which we discuss later. For inference, batching of multiple inputs provides higher reuse and more embarrassing parallelism, with almost no additional pressure on the hardware. Training with large batches, provides the same, but a linear increase in the amount of intermediates that need to be kept-around, before the backward pass can commence. To support distributed training, which is often needed, an intermittent All-Reduce phase allows exchanging of gradients across all of the systems: creating the illusion of all systems having learned from all of the samples. Klenk et al. show that perfect all-reduce improves performance by 10% to 40% [30].

B. Workload Characterization

Figure 2 shows a snippet that is representative of each of the applications at the graph-level. We characterize the entire MLPerf suite (including MaskRCNN, removed in the latest version of MLPerf). Table II summarizes the quantitative features of each of the applications. Based on qualitative understanding of the applications and detailed quantitative profiling (methodology explained in Section VII), our general findings are below.

Program Behavior. The basic program behaviors are:

- Because of the topological order imposed by the compute graph, it is often the case that an operator consumes a tensor produced by the directly preceding operator (in execution order). This “tensor-reuse” is an easy target for performance optimization (e.g. via caching). A framework can tune its topological sort to further optimize for operand locality. Memory reuse and access behaviors can be often statically determined.
- Datatype implications of wide-accumulate to operators like Matrix Multiply and Convolution are contained to computer arithmetic responsibility of the hardware, and can be handled with the abstraction of a requantize node prior to the successor operator.
- For this diverse DL application set we analyze, three broad operators (and their backward counterparts) dominate: Convolution, Matrix Multiply and Element-wise operations. But ignoring the others quickly curtails performance because of Amdahl’s law effects. The last column shows the percentage of network ops that are accounted for by these primary op types.
- There is a generally scalable parallel algorithm for MatMul, Conv, Element-wise, and their backward operations, for the shapes in typical DL applications, without needing large batch size.

Hardware needs. These program behaviors can be distilled into the following needs from the hardware.

- A memory hierarchy that is capable of supporting data-reuse, most or all of which can be statically inferred and communicated by the software. Mechanisms like
TABLE II
SUMMARY OF DIFFERENT PROPERTIES OF WORKLOADS

| Network       | Mode  | GOPs / Sample | # Shapes | Static/Dyn. | Primary Op Types | % Primary |
|---------------|-------|---------------|----------|-------------|------------------|-----------|
| Resnet50      |       | 7.8           | 30       | Static      | Conv2D, MatMul   | 98.41%    |
| SSD Resnet34  |       | 35            | 43       | Static      | Conv2D, MatMul, Relu | 99.82%   |
| Yolo V4       |       | 98.9          | 54       | Static      | Conv2D, Tanh, Sigmoild | 93.92%   |
| MaskRCNN      |       | 780.9         | 60       | Static      | Conv2D, MatMul, Sigmoild, Relu | 99.85%   |
| RNN-T         |       | 12.8          | 16       | Dynamic     | MatMul, Tanh, Sigmoild | 99.92%   |
| Bert Base 128 | Inference | 23.0           | 8       | Static      | MatMul, Tanh    | 97.67%   |
| Bert Base 384 |       | 72.1          | 8        | Static      | MatMul, Tanh    | 98.35%   |
| Bert Large 128|       | 81.1          | 8        | Static      | MatMul, Tanh    | 98.05%   |
| Bert Large 384|       | 251.7         | 8        | Static      | MatMul, Tanh    | 98.68%   |
| Resnet50      |       | 23.6          | 81       | Static      | Conv2D, MatMul   | 98.11%   |
| SSD Resnet34  |       | 39.5          | 116      | Static      | Conv2D, MatMul, Relu | 99.70%   |
| Yolo V4       |       | 285.6         | 156      | Static      | Conv2D, Tanh, Sigmoild | 97.19%   |
| MaskRCNN      |       | 2,591.6       | 175      | Static      | Conv2D, MatMul, Sigmoild, Relu | 99.81%   |
| Bert Base 128 | Training  | 73.3           | 32       | Static      | MatMul, Tanh    | 95.55%   |
| Bert Base 384 |       | 219.5         | 32       | Static      | MatMul, Tanh    | 98.03%   |
| Bert Large 128|       | 251.1         | 32       | Static      | MatMul, Tanh    | 95.99%   |
| Bert Large 384|       | 757.0         | 32       | Static      | MatMul, Tanh    | 98.30%   |
| Bert Base 384 |       | 217.4         | 8        | Static      | MatMul, Tanh    | 98.10%   |
| Bert Large 384|       | 755.6         | 17       | Static      | MatMul, Tanh    | 98.37%   |

We do not cover DLRM in this work because of its over-reliance on large embedding tables. The MLPerf version of DLRM is a very simple MLP with just 5 MOPs per item. Most of the inefficiency for hardware execution comes from looking up a 96GB table (with FP32 features) into which the lookups are sparse; 5 tables account for 98% of total capacity. From the perspective of a DL accelerator, the design principles focus on memory system optimizations on page/bank policies, or split work between CPU and accelerator, where the CPU does the rare lookup, keeping the entire table in memory, with an accelerator doing the frequent ones only. Doing this detailed system-level tuning is beyond the scope of this work, and is necessary for fair evaluation of performance, and such table/data-structure optimizations are part of NVIDIA’s implementation. A blind implementation of DLRM becomes purely memory accelerator doing the frequent ones only. Doing this detailed system-level tuning is beyond the scope of this work, and is necessary for fair evaluation of performance, and such table/data-structure optimizations are part of NVIDIA’s implementation. A blind implementation of DLRM becomes purely memory latency bound and heavily skewed for memory capacity.

hardware managed caching, hardware-learned prefetching, memory disambiguation, out-of-order execution of memory accesses are all superfluous or unnecessary.

- The hardware must support lots of parallelism and fast synchronization, without necessarily needing support for frequent / fast fine-grained operand communication.
- Power efficient high-density computation to exploit the available parallelism.
- Enable overlapping of memory reads with computation in order to achieve full utilization of compute resources.

III. ARCHITECTURE AND DESIGN SPACE

Abstractions. As outlined above, for DL, a set of higher level of abstractions exist that are quite naturally aligned to the algorithm developer’s view of the world. These are Tensors (with datatype and layout), Operators, and explicit dependence between tensors providing a graph of computation. Hardware designers are used to architectural abstractions being instructions, primitive operands, register-file, and memory. Our intuitive observation is that it is possible to lower these high-level abstractions down to the architectural abstractions with established compiler techniques, and established microarchitectures can be upcycled to provide efficient support for these high-level abstractions.

Principles. Before we describe the architecture, we first outline our guiding principles. The principles are disconnected from the program behaviors, or the architectural solutions themselves. Instead they are inspired by the problem definition and help focus our contribution and novelty. They are:

- Adhere to established SIMD CMP design as much as possible. This is so we can show how a software architecture as well as non-exotic architecture can achieve high performance of DL workloads.
- Be able to take advantage of decades worth of compiler and software-stack optimizations that target this type of architecture such as loop unrolling, instruction scheduling, vectorization, and tiling. This is to demonstrate the advantage (and feasibility) of building a competitive architecture that has a software stack immediately available.
- Target state-of-art technology node, focusing on conventional transistors and circuits, to study the limits of architectures. We explicitly avoid packaging, circuits, and in-memory ideas for this work. This enables a fair comparison to current industry state-of-art DL accelerators and allows us to study the limits of architecture using conventional and production transistor technology.

The rest of this section describes the architecture, execution model, programmer view and concludes with the implementation decisions to instantiate one instance of this architecture. We call this the UPCYCLE architecture.

A. High Level Organization

UPCYCLE, shown in detail in Figure 1 and Figure 2 consists of three main components: 1) Parallel processing elements 2) An interconnection network and 3) A memory system. UPCYCLE is a mesh of identical tiles containing the processing elements and slices of the memory hierarchy. The hardware includes a global thread scheduler (that could be just a programmable core or fixed state machine) that allocates work to cores. It also includes a host interface controller.
(PCIe-like interface) to provide high bandwidth, low latency communication to a general purpose host computer that runs the system-level portions of the DL stack. Finally, one or more memory controllers and PHY on chip (HBM from a implementation standpoint is preferred) feed the LLC. The physical organization of the LLC is straightforward: slices distributed across the chip with static address mapping. A 2D-mesh interconnection network transmits cache lines between tiles and to and from memory.

B. Tile Organization

Each tile contains a pseudo-dual-issue in-order core coupled with a wide SIMD/short-vector datapath including register file and arithmetic units organized as lanes. We find the mechanics of the ISA are unimportant as suggested by Blem et al. For the SIMD datapath, a narrow subset of AVX suffices. This consists of add, multiply, multiply-accumulate, vector load/store (with broadcast & stride), and wide-accumulate instructions. In addition we also add a small number of custom vector load instructions such as multi-broadcast (i.e. load several elements from memory and broadcast each to their own SIMD register). We choose a dual-issue design in order to allow overlapping vector loads with computation (Executing two vector loads in one cycle is not necessary). We discuss more details of custom loads and dual-issue in Section IV-A.

One SIMD lane supports two Int8 and one FP16 multiply-accumulate operation per cycle. It allows internal accumulation in 32-bits. A private cache is also included in each tile. We choose our private cache to be 16 KB as a staging area for data. In the next section, we explain why this choice of small private cache is sufficient. The private cache is built with a scratchpad mode and HW-managed cache mode. The scratchpad mode minimizes the pollution from aliasing caused by prefetching. As noted by others, caching and streaming are of similar effectiveness with the scratchpad mode reducing

\[ \text{Prefetch I} \rightarrow \text{LLC} \]
\[ \text{Prefetch W} \rightarrow \text{LLC} \]

1. Original Graph
2. Optimize + Order
3. Threads + Sync.
4. Object Code

Execution model and lower of graph to hardware primitives.

For the sake of hardware simplicity, we assume software configuration of the mode. The size of the architectural register file and SIMD lanes is a first-order determinant of performance, since it dictates how much parallel work can be done before hitting WAW hazards. We found that with 32 registers, the shapes in MLPerf can be supported without the core becoming the bottleneck.

One important requirement to effectively exploit the abundantly available data reuse and embarrassing parallelism in the presence of large data sets is prefetching. To efficiently support prefetch on a simple scalar core, we allow prefetch instructions to skip the scoreboard logic, avoiding them blocking future instructions. To simplify the core, we use software assisted compiler instruction scheduling to promote prefetch instructions before their use. The rich information in DL stacks allow such static analysis to be effective and straightforward (unlike codebases like SpecINT, SpecFP etc.). An SMT scalar core could reduce these burdens on software.

C. Programmer’s view and Execution Model

The abstract model of UPCYCLE is a parallel thread array with one thread per core. Figure 4 provides a pictorial representation of the execution model and how the DL-stack abstractions are lowered down to low-level primitives. Programmers divide up work into individual tasks each of which run on one logical thread, inserting necessary synchronization instructions to support inter-thread dependencies. For DL applications, the DL-stack serves as a high-level abstraction hiding all of this from the programmer, where the programmer’s view is straight-line code in a framework like Tensorflow, Pytorch, Keras etc. The middleware that translates from the framework to the “programmer-view” is responsible for creating threads, inserting synchronization instructions for enforcing barriers between one operator and another. This middleware is also responsible for mechanical code-generation tasks of a preamble code to communicate

\[ \text{Vmovps } \text{zmm1}, \{ \text{ll} \} \]
\[ \text{Vmovps } \text{zmm2}, \{ \text{ll} \} \]
\[ \text{Vbroadcastss } \text{zmm3}, \{ \text{Wll} \} \]
\[ \text{Vmovaps } \text{zmm4}, \text{zmm1}, \text{zmm3} \]
D. Machine Parameters

There are ultimately 4 machine parameters to instantiate a version of UPCYCLE: number of tiles, SIMD width, cache sizes (L1, LLC), and memory system bandwidth hierarchy (LLC → L1, L1 → VRF). These parameters are inter-related to create a balanced design and some are influenced by performance cliffs in terms of supporting applications. The number of tiles is dictated by available chip area and power which, coupled with performance needed, dictates the LLC size and memory system bandwidth (we explore this sensitivity in the results section). Finally the SIMD width intimately dictates the L1 and LLC fill-rates and sizes. To avoid an over-provisioned core, cache fill-rate must match the SIMD width.

One of the main takeaways is UPCYCLE is a fairly straightforward composition of known ideas, allowing easy mapping of applications to hardware, easy compiler (re)targeting and SW stack development which we discuss next.

IV. ACHIEVING SOFTWARE MATURITY

UPCYCLE is intentionally designed to eliminate the need for novelty needed in the compiler\textsuperscript{6} With a manually designed operator library where parallelization and vectorization is explicitly done by the DL-framework developer (not DL programmer/chip user), the compiler is simply responsible for lowering low-level intrinsics into object code. This stage of code-development includes reasoning of private cache sizes, available architectural registers to create the optimal micro-kernel, which we discuss in Section IV-A 4.6. The compiler also inserts some of the primitives from the standard library for orchestrating communication with the global thread scheduler. The compiler’s instruction scheduler’s responsibility is to promote prefetch instructions ahead of their usage.

Software Stack. Our software stack is built by composing known components. We employ Tensorflow, which exposes the compute graph as a user-facing abstraction. Referring back to Figure 3 the framework parses (runs) user code to build the compute graph which then feeds into a graph optimizer, which handles operator fusion, and optionally quantization. A library mapper then chooses operator implementations based on our mapping in the previous section and then performs additional optimization over tensor shape and layout. Once operator implementations are chosen, our compiler does the final step of lowering and packaging the program object code. Inference vs Training. A datatype such as signed 8-bit (Int8) is popular for inference since Int8 arithmetic units are smaller, faster and more efficient compared to floating-point units. Training still often uses floating point formats such as FP32, FP16 or newer types such as NVIDIA’s TF32 or BF16, and once training is completed a network’s weights are “quantized” into a lower-precision integer format (e.g. Int8) for inference. Standard workflows exist for quantizing networks post-training \cite{31, 58}. We use a TF-based flow for such quantization to perform inference in integer datatypes.

Supporting a new operator. Supporting a new operator is very easy. An SDK developer simply authors the implementation and metadata for the operator in the framework. The DL framework developer is responsible for a high-performance back-end library function implementation for the operator. This approach requires virtually no effort on the part of the compiler developer or application developer. If the compiler is able to have more responsibility for code-generation, back-end library function development becomes unnecessary.

A. Algorithm Mapping

First, we provide a summary of the general approach of mapping an application (decomposed into a graph of operators) onto the architecture. In this paper, we primarily focus on an execution model of one operator active at a time, with the exception of RNN-T, which we will address specifically. Nothing in the architecture precludes mapping multiple operators and pipelined communication between operators. As described in the results, this simpler approach provides substantial efficiency already. And we leave pipelined multi-operator execution as future work, and acknowledge production/commercial uses cases of this exist \cite{12}. For training, we use the same sequential-operator execution model. For this work, we focus on single-node training. Other ideas optimized for distributed training can be layered on top.

We choose output-splitting as the default parallelization strategy. This lends itself to the easiest parallel algorithm in that it minimizes the amount of synchronization and inter-core communication needed. Chunks are made as small as possible without affecting SIMD efficiency to expose ample parallelism. For each operator, we develop a micro-kernel which handles a single output chunk.

Figure 5 shows an overview of algorithm mapping for 2 representative operators. It shows the highest level operations in terms of the two tensors, the chunking to achieve parallelism, reuse available, and the lowest-level code snippet. Now we detail how each operator is lowered to our architecture.

Matrix Multiply. Two input matrices $A$ and $B$ have shapes $A[M, K]$ and $B[K, N]$. Our approach for matrix multiply is based on NGemm \cite{4}, taking into account the effects of wide-accumulation for integer data types. The micro-kernel used to compute output chunks in parallel is a sub-matrix multiply. We choose to vectorize along $M$ for matrix multiply, since most applications fill this dimension to at least the vector width. If $M = 1$, which occasionally appears, we vectorize along $K$ instead and incur the cost of an add-reduction across the vector width.

Based on tensor layout, we face a few challenges. For example, for a layout of MKKN (That is, $A$ is major in $M$, $B$ is major in $K$) we observe that the tiling in the $N$ dimension must be at least the vector width, or the microkernel will end.
up loading more data into the private cache than is necessary for computing the output. To overcome this, we simply enforce a minimum tiling factor so in the common case, memory bandwidth is used efficiently.

In addition to this, loads into the vector register file need to amortize to one vector per op to maintain peak throughput due to cache bandwidth and issue width constraints. To achieve this for layouts like M2KN, we introduce custom load instructions. For a MatMul microkernel, we load $TM \times TK$ chunks from $A$, and $TN \times TK$ chunks from $B$. Elements from $B$ undergo a “multi-broadcast” operation, where sequential (and contiguous) elements along the $N$ dimension are loaded as a whole cache line, and each element is then broadcast to its own vector in the VRF. This effectively enables one memory instruction to fill $TN$ of the operands for computation. Elements of $A$ are loaded in a strided fashion, where the number of cachelines loaded is the vector width divided by the ratio of the accumulator to the input data type. Again, excess data is loaded to fill additional vector registers to fully utilize peak bandwidth. This allows $TM$ load from $A$ and $TK$ loads from $B$ to satisfy (amortized) $TM \times TK$ vector FMA operations, which, when sized properly, allow memory operations to be completely hidden behind computation.

2D Convolution. We implement Conv2D based on Intel’s high-performance convolution approach [15]. In this approach, input and output channel blocking are applied to the tensor shape to enable vectorization. Independent output chunks are computed as independent tasks in parallel. Also in line with Intel’s approach, each output block is computed by invoking a small GEMM kernel over the input and filter. Similar to MatMul, convolution microkernel invocations use tiling factors to achieve a similar effect where we can amortize loads to hide behind vector operations. To provide insight into the workings of the architecture, Figure 5 presents the timeline of operations, the spreading of work across the chip, and how the transfer rates between portions of the chip allow execution of the first Conv2D in Resnet-50.

2D Convolution Back-Propagation. We build our own approach for computing Conv2D input backpropagation (dl) and weight backpropagation (dw). In order to enable compatibility with the shapes and layouts used in the backward pass of convolution, we assume the same tensor shape and layout as for forward. For dl, the micro-kernel computes a dl chunk of size $w \times h \times C_b$ with $w = h = \text{stride}$. For dw, our micro-kernel computes a single filter pixel (spatially).

Element-wise operators. Element-wise operations are computed in an embarrassingly parallel manner. We simply divide evenly the number of elements to compute across the available cores (respecting some minimum block size to ensure SIMD efficiency is maintained). Backpropagation for these operators is conceptually simple and themselves are just element-wise operations. Some backprop operators, such as TanhGrad, require two inputs (the original computed output and the output gradient) to compute the input gradient.

RNN-T Considerations. RNN-T operators are small enough that our execution model cannot achieve high-performance without also considering inter-operator parallelism. For RNN-T we enable this in our operator implementation and execution model so that operations with no order dependence can be executed in parallel. This boils down to computing all of the input-weight products across an LSTM sequence in parallel, then propagating a sequential “hidden-chain” though. Similarly, for backpropagation, we compute the backward pass through the hidden chain sequentially, then the backward pass
of the input and weights as large matrix multiplies with the sequence length as one of the dimensions.

V. METHODOLOGY

We now detail our evaluation methodology of end-to-end DL applications implemented in TensorFlow/PyTorch.

Extracting Traces. We use PIN [39] to implement a tool for capturing instruction mix and flop count over a region of interest. We insert region markers into Tensorflow at the operator boundary, and capture metadata, such as input/output tensor shapes, operator parameters, op-counts, and instruction-mix. We run an app with our instrumented Tensorflow on PIN, producing an op trace. We also obtain hardware performance counter statistics to validate the PIN data.

Performance Modeling. For performance evaluation, we build a Zsim-like performance simulator/model that uses the DL operator trace, and a memory system model, accounting for the effects of the vector instructions, and access rates to model memory bandwidth. We do not model the details of memory bank conflicts, page policy etc. and instead assume 60% of available memory bandwidth is used. The simulator accounts for the cycles taken by the computation core, and the execution timeline of events shown in Figure 6.

Power and Area Estimation. Our tile design consists of a SIMD MAC, SIMD NLOp, SIMD register file, processing core, and private cache which is replicated across the chip and then combined with a distributed last level cache (LLC). We used the methodology in Accelergy [59] and Timeloop for our area and power modeling. We use the LX3 processor core mentioned in [21], [44] as a reference for the power and area of a lightweight, in-order core. Ara [6] provides an estimate of SIMD area and power. We use the arithmetic units from [26] as a reference for the SIMD MAC unit. Finally, Cacti is used for power and area estimates of the last level cache. All of these components are normalized to 7nm power and area using the methods from [54]. The power consumption of the memory controllers, PHY and HBM stacks is 6 Watts per stack (24W for entire chip) based on data sheets for HBM2. For the frequency scaling experiments, we make use of work presented by ARM on their Neoverse N1 CPU, which presents power scaling for 3 GHz to 1.2 GHz [2].

Baseline and Comparing Performance. To report our results, we obtained published performance results of the NVIDIA A100 system. We paid close attention to ensure that we were using the exact same DL-model as the NVIDIA system. For some applications, we used NVIDIA’s code published through MLPerf to replicate performance results and obtain results for different batch sizes. For Bert Large pretraining, we were unable to run NVIDIA’s official code on a single GPU so we used the ratio of large batch inference to small batch inference to estimate small batch pretraining.

VI. RESULTS

A. Overall performance

To evaluate UPCYCLE, we first examine our default configuration, UPCYCLE$_{Base}$, against an A100 – A state-of-art software mature DL accelerator – separating out performance on inference and training. For both we consider performance at small batch-size and large-batch size, on the MLPerf benchmark suite to stress DL coverage.

Before we present the performance results, Table III summarizes other high-level specs. Our area is much smaller than an A100 because of the lack of any FP64 support, and because of the other cache right-sizing we have done. It is likely that our chip configuration is over-fitted to the MLPerf applications resulting in smaller cache sizes. Also, UPCYCLE is over-fitted to DL, where the A100 needs to support general purpose HPC, leading to larger structures.

Figure 7 shows our performance and power efficiency. We cover two broad scenarios for these applications: small batch (1 for both UPCYCLE and A100) and large batch (64-128 for UPCYCLE and A100; whichever yields highest performance). Table IV accompanies this by providing the compute resource utilization of UPCYCLE and A100 for each of these applications for both small and large batch execution.

High level comparison. At large batch, UPCYCLE provides modest performance improvements over A100 – geo-mean 2.2X and 2.3X for inference and training performance respectively – as well as 6X power efficiency improvement in both cases. At small batch, UPCYCLE’s improvements are much larger, providing 7.7X and 11.7X geo-mean performance for inference and training, and 23X and 35X power efficiency gains. Broadly, this shows that UPCYCLE is better suited than A100 to take advantage of abundant intra-operator parallelism at small batch sizes where embarrassing parallelism afforded by batching is not present – which is a product of the architecture and algorithm mapping. We also observe that UPCYCLE is able to achieve this performance advantage at a lower peak performance rating and less than half the power of A100, validated by the relatively high utilization numbers UPCYCLE achieves compared to A100.

We now look at the applications using the compute resource utilization shown in Table IV as a guide explaining the performance and efficiency trends in Figure 7.

Analysis of CNNs. Across the applications we notice interesting performance and efficiency characteristics. For convolution based networks (CNNs), we notice on Resnet50, both UPCYCLE and A100 observe a decrease in utilization when switching from inference to training. To maintain efficiency, the backpropagation to inputs for Conv2D must be computed in chunks of $(R, S)$ (Stride size) over the input feature map. This causes scalability to be limited when compared to the forward pass which ultimately leads to utilization suffering on UPCYCLE since not all cores can be filled with useful
work. For UPCYCLE, this trend holds for all convolution based networks. For A100 utilization actually improves for MaskRCNN training, and also SSD large batch. This suggests A100’s mapping strategy is able to overcome this problem for the shapes in these networks.

**Analysis of Transformers.** For transformer networks, we notice that A100 achieves its highest utilization on Bert compared to the other applications we evaluate. This makes sense since the attention mechanism in transformers are dominated by large matrix multiplies, which allow the A100’s TensorCores to shine. Interestingly, the A100 achieves lower utilization when training transformer models, where UPCYCLE actually improves. For UPCYCLE, this improvement is due to the careful consideration given to mapping transposed forms of tensor layouts. We hypothesize the fixed layout of the TensorCore’s MAC array and its requirements on memory layout are what cause it to suffer for alternative tensor layouts.

**Analysis of RNN-T.** For RNN-T, we observe UPCYCLE’s largest performance and efficiency wins – 25X and 22X performance and 62X and 72X efficiency for small batch inference and training. This gap diminishes dramatically in a large batch scenario. Matrix-vector operations are at the heart of LSTM based networks such as RNN-T, which leads us to hypothesize that Nvidia performs so poorly at low batch execution because these types of operations don’t map efficiently to the TensorCore’s layout. Further, we believe this gap closes so dramatically at large batch because Nvidia makes up for the sub-optimal utilization by exploiting embarrassingly parallelism.

**Take away 1:** UPCYCLE is able to exploit the abundant parallelism in small batch execution much more efficiently than the GPU’s TensorCore approach, by leveraging prefetch and fast synchronization.

**Take away 2:** UPCYCLE is also able run training more efficiently, without needing very large minibatches. This opens up the opportunity for different AI algorithms and training much larger models with the same amount of system memory.

**B. Design space exploration**

Next, we explore the design space of UPCYCLE. For this, we computed the area and power efficiency of different UPCYCLE configurations (SIMD width, number of cores, frequency) in terms of TOP/s per mm² and pJ/op for each of the applications of interest. Figure 8 shows these values plotted for each application for inference and training.

These results reveal a lot of interesting features of the UPCYCLE design space: (a) UPCYCLEBase is quite optimal; (b) RNN-T’s application idiosyncrasies impute different needs on hardware; (c) parameter choice have a massive impact on performance/efficiency. We elaborate further on these. (a) We find that when considering power efficiency alone (pJ/op), UPCYCLEBase comes within a geometric 17% of the optimal application specific UPCYCLE configuration we might pick. (b) For RNN-T, compared to UPCYCLEBase, UPCYCLE 4096c/256v is 28% better for training, but roughly 40% worse for Bert, MaskRCNN, and SSD-Resnet34 (training).

We hypothesize RNN-T benefits from the larger core count since there is more parallelism available due to the tuned mapping we use for this application alone (as described in Section IV-A), and also note that vector length appears not to play a role in RNN-T’s performance characteristics, likely due to how easy it is to achieve high SIMD-efficiency on matrix-vector operations. For the other application, decreasing vector-width while trading core count likely doesn’t affect SIMD efficiency quite as much, but does add the overhead of many more cores, which is what likely accounts for the lower energy efficiency. (c) Finally, a poor implementation choice (256-bit, 192-bit...
1k cores, 1GHz) is over 200% worse in performance efficiency compared to UPCYCLE\textsubscript{Base} but still beats the A100 on power efficiency for every application except Resnet50 Inference.

Figure 9 shows a scatter plot of all the operator shapes we perform on UPCYCLE across the MLPerf applications. The spread of this chart suggests a wide diversity in the performance characteristics of this collection of shapes. UPCYCLE, being purposefully designed for generality across the applications achieves good end-to-end performance despite this diversity, and its SW maturity allows full-mapping/execution of this diverse space.

Take away 3: Though UPCYCLE’s parameters expose a diverse design space of architectures which have varying performance across our target applications, we find our intuitive choice of UPCYCLE\textsubscript{Base} has proven to perform well.

C. Comparison with EyerissV2

To answer how our solution stacks up to state-of-art novel microarchitecture, we investigate the power efficiency of UPCYCLE compared to the popular EyerissV2 accelerator \cite{8}. EyerissV2 is an inference only accelerator which reports performance results for two convolution networks: MobileNet and Alexnet. To make a fair comparison, we define a configuration of UPCYCLE, called UPCYCLE\textsubscript{Riss}, which contains a single core with a 512-bit SIMD unit running at 1.2 GHz to match the theoretical peak compute of EyerissV2. We also size the last level cache of UPCYCLE to 192 KB to match EyerissV2.

Table V shows this comparison. We use the predicted performance of Alexnet and MobileNet on UPCYCLE, coupled with our power estimate to derive average energy per operation (pJ/Op). We scale this metric for UPCYCLE to 65nm equivalent to compare with EyerissV2 using the methodology in \cite{54}.

Unsurprisingly, we see that EyerissV2, being an accelerator design aggressively tuned for CNN inference in low power scenarios, achieves a higher energy efficiency than UPCYCLE. This difference is explained by compute utilization: according to their paper, EyerissV2 achieves 100% utilization of its compute resources, where UPCYCLE achieves roughly 60-80% for the same workloads.

Despite this, EyerissV2 has several shortcomings. First, it has not been demonstrated to run post-resnet CNNs such as MaskRCNN and SSD-Resnet34, as well as modern DL applications such as transformers. Next, it does not show how one can achieve high performance on matrix-vector operations, which are at the heart of LSTM-based applications like RNN-T. EyerissV2’s core alone does not offer techniques for dealing with dynamic memory latency in a larger memory

\begin{table}[h]
\centering
\begin{tabular}{ |c|c|c| } 
\hline
 & Alexnet & Mobilenet \\
\hline
EyerissV2 & 3.95 & 5.16 \\
UPCYCLE\textsubscript{Riss} & 4.92 & 6.72 \\
\hline
\end{tabular}
\caption{Power Efficiency (pJ/Op) of UPCYCLE compared to EyerissV2.}
\end{table}
hierarchy which would be needed to build a tera-op scale chip. For UPCYCLE, this is overcome through leveraging hardware caching and prefetch. As a result of the software maturity of UPCYCLE, other DL applications such as graph algorithms, regression trees for which SIMD mappings exist can be brought up with little to no effort on UPCYCLE where additional hardware work would be needed for EyerissV2.

Take away 4: UPCYCLE is tuned to achieve high reuse, the LLC is sized to capture decent amount of the working set, and the LLC-L1-register file fill rates are balance to avoid the core from being starved. This study shows other memory systems like GDDR6, LPDDR5 could provide graceful performance/power/cost points with UPCYCLE.

Core. To isolate, the effects of the core, we simulate some abstract configurations, where the performance of the core is improved by 2X, 10X, and 100X, with a related increase in the fill-rate of LLC → L1 → RF. Without increasing the fill-rates, the core becomes starved for memory. This study also captures the upper-bound contribution of data-type/datapath optimization of functional units and change the mix of int8/fp16/fp32 etc. Figure 10 shows the results of this experiment. Again the speedup is relative to UPCYCLEBase. Note here that we are ignoring any additional power consumption that might be necessary to achieve this.

Take away 5: Just improving performance and efficiency of the compute core by a lot, can provide limited end-application performance: 100X free core speedup provides only geomean 3.5X application speedup, while a 2X free speedup provides a 1.7X application speedup. Small improvements across the core, uncore, and memory are more impactful.

E. Limitations

Our study includes the following limitations. We don’t believe these have a first-order impact on the qualitative or quantitative findings. First, we are comparing a simulated system to production silicon. To address this, we have made mostly conservative assumptions on performance, power, and area. Second, for training we are not running full training to completion. As explained this is impossible for a simulated system, and we compared training throughput which isolates the effect of the hardware from other algorithmic and system level optimizations. Third, we have not evaluated DLRM and Mini-GO from MLPerf. The latter has been addressed before. Mini-GO does not naturally lend itself to our simulation and evaluation flow since it is a native python code.

VII. RELATED WORK

Verma et al. present a workload characterization of MLPerf Training [57]. Cross-layer approaches related to our work include high-level code generation techniques, and also memory management [23] and memory partitioning techniques [25], [35], [53]. There have been some recent works on SIMD and in particular looking at AVX extensions. These include REDUCT [43], analysis of convolution performance [15], and analysis of inference on CPUs [57]. Mittal et al. [42] presents a survey of deep-learning on CPUs and focus on some of the issues of memory hierarchy and datapath. Domke et al. [13] present a thoughtful case to understand and revisit the role of Matrix Engines for HPC. Reuther et al. present a survey on DL accelerators [48]. These works do not look at the details of program behavior, distilling out the contribution of architecture, or DL coverage. Google has published an extensive set of papers on TPU including [27], which have included treatment on the importance of the software stack, and role of the systolic array architecture, and data-types. Our introduction covered other related work.

VIII. DISCUSSION AND CONCLUSION

This paper observes the importance of SW maturity, revisits old-school architecture ideas of vector, caching, and synchronization coupled with a detailed analysis of program behavior from MLPerf. The UPCYCLE architecture we have defined shows order-of-magnitude speedups and energy efficiency from architectural innovation. The small-batch performance further opens up avenues and impact on the DL space outside of hardware.
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