A Novel Software-based Multi-path RDMA Solution for Data Center Networks

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ABSTRACT
In this paper we propose Virtuoso, a purely software-based multi-path RDMA solution for data center networks (DCNs) to effectively utilize the rich multi-path topology for load balancing and reliability. As a “middleware” library operating at the user space, Virtuoso employs three innovative mechanisms to achieve its goal. In contrast to existing hardware based MP-RDMA solution, Virtuoso can be readily deployed in DCNs with existing RDMA NICs. It also decouples path selection and load balancing mechanisms from hardware features, allowing DCN operators and applications to make flexible decisions by employing best mechanisms (as “plug-in” software library modules) as needed. Our experiments show that Virtuoso is capable of fully utilizing multiple paths with negligible CPU overheads.

KEYWORDS
Data Center Networks, RDMA, Software-based Multi-Path

1 INTRODUCTION
Remote Direct Memory Access (RDMA) introduces the capability of directly accessing the memory of a remote server by implementing the transport logic in hardware network interface cards and bypassing CPU and kernel network stacks, thereby offering high bandwidth and low latency. Nowadays, RDMA is widely deployed over “Converged” Ethernet via RoCEv2 in modern data centers [12, 16, 26] to support machine learning and other data intensive applications. By design, RDMA is a point-to-point transport, where each RDMA connection is mapped onto a single network path. More specifically, RDMA operations (verbs) of an RDMA connection are transported along the same network path via single Queue Pair (QP); each message of an RDMA verb such as SEND, RECV, READ, WRITE is divided in segments of equal size and encapsulated in UDP packets, where the source and destination IP addresses of the UDP packets are set to those of the two communicating servers, the destination port fixed at 4791 and the source port arbitrarily chosen. These are all done automatically by the RDMA NICs (or RNICs in short), which makes port number based path control mechanism as in MPTCP [7] difficult in user space.

Data center networks (DCNs) are typically built using a “spine-leaf” topological structure with rich multiple paths, especially between spine routers, for load balancing and reliability [1, 9]. As a point-to-point transport, RDMA does not take advantage of multiple paths in the underlying networks for load balancing and reliability [11, 22, 24]. For machine learning and other data intensive applications, an RDMA read/write operation may involve remote transfer of a big chunk of data (“elephant flows”), which may not only take some time to deliver along a single path, but also cause congestion that can potentially affect “mice flows” from other applications, especially interactive applications with stringent latency requirements. MP-RDMA [17] is the first work that attempts to address this limitation of existing RDMA (or rather, RoCEv2). It focuses on the challenges in implementing a multi-path RDMA solution in hardware, in particular, the limited memory resource in RNICs. By using source port to encode “virtual path” id (VP id) and influencing the path traversed by the RDMA UDP packets, it assumes and heavily relies on the underlying routers’ ECMP mechanisms for load balancing among multiple paths. The proposed solution is emulated/prototyped using FPGA. As MP-RDMA requires replacing existing RNICs to new MP-RDMA capable NICs, it cannot be readily deployed in DCNs.

In this work, we propose and develop a purely software-based multi-path RDMA solution, dubbed Virtuoso. Our solution employs three key innovations. First, we create multiple virtual interfaces – each with a different (virtual) IP address of our choice – and bind them to the same physical NIC (effectively creating multiple virtual RNICs). Hence unlike MP-RDMA which manipulates the source port only, we control and manipulate source IP addresses of the RDMA UDP packets for load balancing and reliability. Second, we develop a user-space middleware layer which intercepts and split (large) messages of RDMA operations into multiple
(smaller) messages, and dynamically maps them onto different paths at the sender side, and judiciously merge them together at the receiver side by passing them to the applications. Performing these operations correctly and incurring as little overheads as possible (especially, maintaining zero-copy) is nontrivial; it involves careful design and some clever tricks (see Section 3). Third, we also implemented a user-space load balancer that consists of a congestion avoidance (for lossy network) and path probing component mechanism, to do a application aware load balancing.

Virtuoso offers several advantages over existing hardware-based multi-path RDMA solutions. As a purely software-based solution, it can be readily deployed in DCNs at scale with existing RDMA NICs and works regardless of the number of physical RNICs installed on servers. In contrast to MP-RDMA which implements “built-in” path selection, congestion control and traffic distribution mechanisms in hardware and hinges on ECMP to perform multi-path routing, Virtuoso decouples these mechanisms from hardware features, and allows DCN operators/applications to make flexible decisions by employing best mechanisms (as “plug-in” software library modules) as needed. For example, one can explicitly manage multi-path routing by setting appropriate forwarding rules (based on source and destination IP addresses), e.g., through an SDN controller. Virtuoso allows them to guide traffic distribution decisions. Our experiments show that Virtuoso can fully utilize multiple paths with negligible CPU overheads.

2 MOTIVATION & RELATED WORK

2.1 RDMA/RoCE Basics

RDMA allows applications to directly access remote memory with zero-copying and low CPU involvement by implementing the transport logic in hardware RNICs. RDMA over Converged Ethernet v2 (RoCEv2) has been widely deployed in data center networks to support compute- & data-intensive applications such as machine learning, as it provides low latency and high bandwidth with little CPU overheads. Normally, RDMA requires a lossless network where Priority-based Flow Control (PFC) and Explicit Congestion Notification (ECN) are usually configured to prevent packet losses by pausing traffic and throttle packets at the source.

RDMA is a message based, point-to-point transport, where RDMA messages are divided into segments and encapsulated in UDP packets that are transported along a single path. Applications connect with each other using send and receive Queue Pairs (QP). An application initiates RDMA operations (or verbs) by posting Work Requests (WRs) (or Work Queue Element (WQE)), e.g., SEND/RECV or WRITE/READ to the QP, which commands the RNIC to transfer data to the memory of a remote host. For each application, there is also one (or more) completion queue (CQ); upon completing a WR, a completion queue element (CQE) is delivered to CQ.

2.2 Multi-paths in Data Centers & RDMA

The “leaf-spine” topology in modern Data Center Networks (DCNs) offers rich path diversity [1, 5, 9]. Switches and routers employ built-in Equal-Cost Multi-path (ECMP) for routing based on hashes of 5-tuple packet/flow headers (⟨src IP, dst IP, src port, dst port, protocol number⟩). ECMP suffers several issues in practice [1, 3], e.g., it is less effective when the number of paths is large, and it cannot perform intra-flow load balancing for large elephant flows. Other (software-based) solutions such as Valiant Load Balancing and “customized” multi-path routing algorithms (e.g., by setting up explicit flow rules [1, 9, 19]) provide DCN operators and applications more control over multi-path routing and load balancing. We remark that congestion often occurs at the core layer of a DCN [2]; large “elephant” flows generated by data-intensive machine learning applications further contribute to this problem. They not only prolong their own flow completion times (FCTs), but also adversely affect other applications. It is therefore desirable to split such “elephant” flows to enable “intra-flow” load balancing across multiple (core) paths [2, 25].

MP-RDMA [17] is the first to address the challenge that RDMA/RoCE v2 cannot effectively take advantage of rich multiple paths in DCNs [11, 22, 24]. It proposes a hardware-based solution with “built-in” path selection and congestion avoidance mechanisms. The key challenge it focuses on is the limited memory in RNICs (see also FaRM [6], LITE [27] and INFINISWAP [10] that tackle similar hardware constraints). As a hardware-based solution, it cannot be readily deployed without upgrading RNIC. It also heavily relies on ECMP for multi-path routing and load balancing.

We therefore seek a purely software-based multi-path RDMA solution operating in the user space that works with existing RNICs while maintaining zero-copying and incurring as little CPU overheads as possible. A key enabling idea of our proposed solution is to create multiple virtual NICs (vNICs) and bind them to the same hardware RNIC, thereby allowing multiple IP addresses to be assigned to the same RNIC. Our solution allows a single RDMA application to create multiple virtual RDMA connections that are mapped to different paths. This is different from existing efforts in virtualizing RNICs [4, 13, 15, 21] with the goal to allow multiple VMs/containers to share the same RNIC with some level of isolation. Compared with “built-in” multi-path routing and load balancing mechanisms, we also believe that it is imperative to provide DCN operators and applications with flexibility in multi-path routing and load balancing decisions. For example, it has been shown that global congestion avoidance and traffic scheduling [8, 18, 20] are essential in DCNs,
and applications are best aware of traffic load distribution for adaptive load balancing [14]. Similarly, Avatar [23] aims at making RDMA transport on a single NIC to be efficiently shared by eliminating lock contention and providing fair data scheduling via WR multiplexing.

3 VIRTUOSO DESIGN

3.1 Overview

Virtuoso is a software-based, modular multi-path RDMA framework. Virtuoso sets up multiple virtual NICs (vNICs) on each physical RNIC using IP alias, each assigned with a distinct IP address (see Fig. 1(a)). In practice, RDMA uses a Global ID (GID) to identify each host, and RoCEv2 binds GIDs to the IP addresses of the interfaces using the IP table. Using vNICs, Virtuoso is able to create multiple QPs using the standard RDMP libraries rdma_cm and ibv_verb.

![Diagram of Virtuoso](image)

(a) Virtuoso Overview

(b) System Design

Figure 1: Virtuoso: Software Multi-path RDMA Solution

Virtuoso maps each QP to a distinct virtual path (VP), and using the IP address associated with each vNIC as a VP id. As a middleware operating at the user space, Virtuoso provides the same APIs (and RDMA verbs) as in the standard RDMA libraries, but prefixes them with the keyword MP as shown in Table 1. For example, an application invokes MP_connect() to set up a Virtuoso multi-path (logical) connection, and uses MP_READ/SEND and MP_WRITE/RECV to post Virtuoso work requests (WRs), MP_WRs. On the sender side, Virtuoso decomposes a large RDMA message (thereafter simply a “flow”) contained in an MP_WR into smaller “sub-flows”, and distribute them to different QP’s by generating the corresponding constituent WRs using the standard RDMA verbs. The sub-flows are “merged” at the receiver side. These are illustrated in the right portion of Fig. 1(b). Virtuoso consists four major components, QP Manager, Decomposer (on the sender side), Reassembler (on the receiver side), and Path Monitor & Load Balancer.

| Standard RDMA API & Verbs | Virtuoso Version |
|---------------------------|------------------|
| rdma_connect()            | MP_rdma_connect()|
| rdma_disconnect()         | MP_rdma_disconnect()|
| ibv_post_send()           | MP_ibv_post_send()|
| WRITE/READ                | MP_WRITE/READ    |
| SEND/RECV                 | MP_SEND/RECV     |

Table 1: Interface & Verb Design

Virtuoso assumes that there is only one single port connection between ToR switch (but can also work with multiple ports) and RNIC while have multiple paths in the core layer of data center networks. The load balancing mechanism can be either ECMP (with known hash function) or static routing.

3.2 Virtuoso QP Manager

3.2.1 Transmission via Multiple QPs. As discussed above, an RDMA application creates a (logical) multi-path connection using Virtuoso APIs. Virtuoso maps this logical connection to multiple (virtual) paths by automatically setting up the corresponding QPs, one per path. To set up these QPs to work with the same application, we take advantage of several key features of RDMA. Recall that in RDMA, memory must be registered before any RDMA verb can be post. The sender and receiver communicate and negotiate the address locations of the respective memory. Each RDMA transport context (registered memory, QP) is maintained inside a Protect Domain (PD). Inside this PD, these contexts can be shared and accessed by multiple QPs who within the same PD.

In order to associate the multiple QPs created by Virtuoso with the same application, the QP manager create them within the same PD. Furthermore, the same target memory region as specified by an RDMA application is also registered to this PD. This way the message in an MP_WRITE or MP_SEND can be transported through any of the QPs; in particular, for a large message, it can be divided into smaller chunks and transported via multiple QPs for load balancing.

The advantage of this design is efficiency and flexibility: the QPs can concurrently manage the same memory region without memory copying and state transfer between PDs. This, however, creates a challenge at the receiver side when the two-sided MP_SEND and MP_RECV verbs are used: the receiver will not know in advance which QP the data will be arriving, thus which QP to post the corresponding RECV WR. We will discuss how this challenge is addressed in Reassembler of Virtuoso, as well as how out-of-order (OOO) data is handled in Section 3.4. QP manager also creates a shared Completion Queue (CQ) for these QPs, so that it can poll this queue to query the CQEs of the WRs posted to any of these QPs. Note that each CQE has the corresponding WR information (e.g., WR id). Hence for each MP_WR (a “flow”) submitted by an application, Virtuoso can determine
3.2.2 MP_connection & MP_disconnect. In terms of connections between queue pair, it requires a transmission parameter (e.g., queue pair type & queue pair capabilities) exchange process, which involves several functions provided by standard RDMA libraries. This procedure works as the three-way hand shake procedure in TCP/IP. However, this procedure is handled in user space by application instead of the driver in kernel. Thus, Virtuoso should handle all the parameter exchange tasks for multiple QPs. To simplify the connection procedure, Virtuoso provides an uniformed interface, 'MP_rdma_connect()', for multi-path connection which takes over the whole connecting procedure from application. Moreover, application can also configure these parameters by submitting configurations to Virtuoso. The disconnection procedure of QPs is similar and requires extra negotiation between two remote sides. Thus, Virtuoso also provides an uniformed interface, 'MP_rdma_disconnect()', for applications.

3.3 Virtuoso Decomposer

The Decomposer component is responsible for WR generating, memory mapping and MP_CQE generating. As the same as RDMA verbs, each MP_WR (multi-path work request) contains the relevant metadata (memory location, size) regarding the target memory blocks it wants to access. At the sender side, the main task of Decomposer is to divide a large message ("flow") contained in a MP_WRITE or MP_SEND multi-path work request into smaller data chunks ("sub-flows"), and generate the corresponding WRs (WRITE or SEND) for each sub-flow using the standard verb (WRITE or SEND). Likewise, a MP_READ WR that wants to access a large remote memory region ("flows") will be divided at the sender side into multiple READ WRs, each accessing a smaller part of the target memory region ("sub-flows"). To facilitate the memory location and size matching between the sender and receiver, Virtuoso divides the whole (application) memory space into blocks (this parameter is configurable).

To decide the size of each sub-flow, the Decomposer will query the Path Monitor & Load Balancer. Based on the path status, bandwidth and congestion information, Path Monitor & Load Balancer provides a decision about the memory message and WR mapping where load balancing and congestion avoidance are considered (in section 3.5). Then, the Decomposer will generate WRs that maps different blocks of the memory, and pass them to QP Manager. After these WRs are successfully posted and completed, the Decomposer will be notified. Then it generates a corresponding MP_CQE for entire message to notify the application of the completion.

3.4 Virtuoso Reassembler

We first remark that while Virtuoso performs the additional tasks of dividing a large message ("flow") contained in an MP_READ, MP_WRITE or MP_SEND into smaller messages ("sub-flows") by generating a sequence of WRs. These WRs are distributed across multiple QPs, and are performed using the standard RDMA verbs (READ, WRITE or SEND). In other words, the RNIC will directly read/write the corresponding data from or into the remote memory area in application’s memory region as indicated by the verbs. Hence, Virtuoso incurs no additional memory copying.

Out-of-Order (OOO) is a common issue in multi-path transport, due to parallel transmission and variant delay on multiple paths. Virtuoso leverages the benefit of direct memory wiring to resolve the OOO issue by buffering correctly received data into application memory. Once the data traffic arrived on the remote side, we have to merge sub-flows to reconstruct original memory region for receiver application. Since sub-flow traffic pay-loads are written to the memory directly by NIC hardware. The data flow will be composed correctly directly in the user space memory once we post the correct WR into the receive queue of MP_SEND/RECV case (to identify the target memory addresses for each sub-flow); into the send queue of MP_SEND/MP_WRITE/MP_READ case (where the receiver side is totally passive). When Virtuoso uses MP_WRITE verbs as instructed by application submitted MP_WR, the receiver side is totally passive (which means receiver requires no action after memory registration). Once the access key of remote memory is acquired by sender side, Virtuoso can treat remote target memory as its own memory space without receiver’s reaction for any transmission.

**Figure 2: SEND/RECV & Out-of-Order**

MP_SEND/RECV verbs is a special case of OOO. Originally in RDMA, each SEND consumes a RECV in receive queue. Moreover, RECV (who instructs RNIC to write data to the target memory address) is supposed to be posted before SEND’s arriving, which means the target addresses need to be determined in advance. However, the arriving order and data size of each sub-flow is unpredictable. So we cannot simply generate multiple SEND/RECV WRs as in MP_WRITE case. So we propose a hybrid solution by combining SEND/RECV and WRITE. As illustrated in Fig 2, WRITE verbs who requires no RECV, are used to avoid beforehand memory address determination on receiver side. Additionally, two-sided SEND/RECV needs to notify the application of accomplishment by posting a CQE into CQ
(MP_CQE in our case). However, one-sided WRITE verb cannot generate CQEs on receiver side. To this end, Virtuoso posts an extra RECv to the receiving queue for receiver notification purpose. And also Virtuoso appends an extra SEND after WRITE WRs to consume this RECv. Both the RECv and SEND are empty WRs (did not map any memory). As a result, when all the WRITE and SEND/RECv WRs are accomplished, CQEs will be posted to CQs on both sender and receiver sides. After polling the CQ, Virtuoso can post a MP_CQE to notify application using the metadata in CQE.

For efficiency, we classify the MP_SEND into two categories, small message and large message. For small message, a single SEND is used to send entire small message via arbitrary single path; for large message, the hybrid solution is used to load balance the elephant flow of the message onto multiple paths.

3.5 Virtuoso Path Monitor & Load Balancer

Load Balancing is an essential task in multi-path transmission. Virtuoso employs a pre-allocation mechanism to fit the RDMA verbs scenario. First, Virtuoso probes the path capacity (e.g., bandwidth) using historical information (or other performance tools such as iPerf). In current implementation, Virtuoso initiates multiple probing flows (at least 512 KB) to estimate the capacity of each path by monitoring the flow completion times. Second, Virtuoso distributes the incoming large data traffic into multiple sub-flows as follows.

$$\begin{align*}
\sum_{i=0}^{n} data_{path_i} = data_{total} \quad \text{cap}_{path_i} = data_{path_i} / cap_{path_n}
\end{align*}$$

Here cap_{path}, and data_{path}, denote the estimated bandwidth and allocated data size for path i respectively. Then Virtuoso maps the memory into WRs and submits them to QPs in Round-Robin scheduling as shown in Fig. 3(a). Current design is based on the assumption that the status of core paths are stable in short period. Since load balancing is totally decoupled from other components, more real-time and fine-grain load balancing mechanisms in user space will be explored in the future work.

![Figure 3: User-space Load Balancing](image)

Congestion Avoidance is also required in per sub-flow transmission. For instance, if the RNIC has insufficient resilient capability (e.g., Mellanox ConnectX-3 Pro) while the network is not well configured (lossy), mapping a large amount memory into a single WR (where RNIC transmits the data too fast) will cause packet loss in core switches (where the network bottleneck locates at). To resolve this, Virtuoso limits the maximum trunk size of each WR using a congestion window based mechanism. Initially, Virtuoso probes the threshold value of the trunk size of each sub-flow by binary increasing the chunk size while monitoring the shared CQ. If a congestion happens (usually indicated by a CQE with IBV_NC_RETRY_EXC_ERR error code). Virtuoso will decrease the chunk size to previous value and to find a maximum threshold in linear increasing. Moreover, WR construction and posting is also slightly different in lossy network. To avoid packet loss, Virtuoso uses multiple WRs to map the sub-flow message of each path. The maximum chunk size value is used to determine the number of WRs. And also, these WRs will be posted in turns followed by success CQEs as shown in Fig. 3(b).

4 EVALUATION

In this section, we introduce the implementation and evaluation of Virtuoso. We evaluate the performance of Virtuoso, and validate that Virtuoso can fully utilize multiple paths in the core of DCN with minimal CPU overhead.

4.1 Implementation

Virtuoso is implemented as a user space “middleware” library on top of the standard RDMA libraries, ib_verbs and rdma_cm. Virtuoso contains approximately 1500 lines of code (LoC) in C language. Virtuoso uses a thread-free method and event based mechanism to handle multiple QPs establishment and data transmission. An RDMA applications invokes MP_connect() to create QP connections, and use MP_WRITE()/SEND() to initiate a multipath data transmission. Additionally, we implemented two basic modules for congestion control and load balancing. However, they could be replaced easily for apps’ own design.

4.2 Testbed Setup

Our testbed consists of two servers connected to two Top of Rack (ToR) switches with multiple links between them to emulate the multipath scenario in spine-leaf DCN topology. The end-host server is Dell PowerEdge R430 with Intel Xeon CPU E5-2620v3@2.40GHz CPUs and 64GB RAM. They are equipped with Mellanox ConnectX-3 40Gbps RNICs with the MLNX_OFED_LINUX-4.6-1.0.1.1 driver with 10GB port enabled. The ToR switches are QuantaMesh T1048 LB9A (SDN switch) to perform an ip based path mapping as shown in Fig. 4.
4.3 Multi-Path Utilization

In this experiment, we evaluate the capability of Virtuoso in path utilization. We can proof that Virtuoso can fully utilize multiple paths to improve bandwidth in the network between ToR switches (core portion).

Flow Completion Time is the matrix that we are using to evaluate the performance of Virtuoso in using different number of paths (1, 2, 4, 6, 8 and 10). For each link between ToR switches, we limited the speed to 1GB/s while links between ToRs and servers are 10GB/s which introduces a bottleneck in core portion. As shown in Fig. 5, with the increasing of the number of used paths, the FCT will decrease obviously. And also, the benefit of using more paths can be leveraged under different sizes (from 10 MBytes to 100GBytes) of message size scenarios as shown in Fig. 7, which means Virtuoso can utilize multiple paths for better transport.

4.4 Trunk Size & Congestion Avoidance

As in congestion control, if a WR submitted too much data at once, congestion will happen in bottleneck core network. Thus, utilizing multiple paths will potentially increase the trunk size that a WR can submit. As shown in Table. 2, by using more paths, the trunk size can also increase. As a result, for a fixed size of data flow, we could save more CPU time by sending more data each single iteration.

Moreover, as shown in Table. 2, using 2 or 4 paths can cause a decreasing of average trunk size compared with single path scenario. The reason is that the capabilities of limited number of extra paths still cannot patch the gap between core networks and RNIC. However, with more paths are used, the average trunk size of each can also be increase with less data allocated on each path in each iteration.

4.5 Multiple Flow & Load Balancing

As discussed in Section 3, multi-path transport can also increase the fairness by avoiding elephant flows blocking the mice ones. To validate that, we generate consistent data flow as background traffic while a mice flow (256 KBybe) is initiated in every 2 seconds. Virtuoso splits the background elephant flow among 10 paths to avoid its blocking on single path. In comparative situation, Virtuoso does not split the elephant flow, while mice flows are sharing the same path used by the elephant flow. Then, we compare the FCT of mice flows with/without load balancing of Virtuoso.

As shown in Fig. 7, with Virtuoso splitting the elephant flow on multiple paths, the FCT of these mice flow will decrease due to extra bandwidth. In single path scenario, which is also the case without Virtuoso’s load balancing, the background traffic occupies the shared single path and blocks the mice flows. As a result, the FCT of mice flows are increased.

4.6 CPU Overhead

We use CPU usage time (CPU cycles) to evaluate the CPU overhead of Virtuoso. In this experiment, we tag the code in different points (e.g., the end of the MP_rdma_connect() function) to measure the CPU cycles used by different parts. The standard C library time is used to log the CPU clock of a specific time.

Moreover, to avoid CQ polling caused extra CPU usage, we use event based completion queue polling (ibv_get_cq_event())
where the application will be blocked during data transmission). In this way, we could avoid the deviation caused by unnecessary CPU usage and measure only critical CPU overhead.

Virtuoso can improve the bandwidth in core of DCNs by utilizing multiple paths but introduces negligible CPU overhead.

Virtuoso is presented to bring inspirations for the community to leverage the flexibility of software visualization techniques. We plan to further i) provide a fine-grained yet efficient congestion control mechanism to achieve fast and dynamic load balance reaction and ii) migrate real-world applications, like distributed TensorFlow [12], to evaluate the benefits of Virtuoso, and to benefit the machine learning community.

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5 CONCLUSION & FUTURE WORK

This paper presents Virtuoso, a purely software-based multipath RDMA solution for data center networks which effectively utilizes multiple paths for load balancing and reliability. Virtuoso employs VNICS to help RDMA applications split large flows into multiple smaller sub-flows and dispatch them among multiple paths to achieve user space load balancing.

Figure 7: Multiple Flows Interactions with Virtuoso

As shown in Fig 8, with increasing the number of used paths especially in small message size scenarios, more CPU cycles are used in user space computation. However, large data size actually eliminates this side effects by increasing both bandwidth and trunk size to decrease the iterations for transmitting the same amount of data. Hence as a comprehensive conclusion, large data message should always leverage multiple paths while small data messages can use Virtuoso to steer the flows to avoid congested paths.

Figure 8: CPU Usage Overhead Comparison
