A low-voltage with high pumping efficiency charge pump for flash memory

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Abstract. This paper proposed a high efficiency of power conversion and high pumping gain charge pump applied to the field of low power consumption like flash memory. The threshold voltage drop, body effect and the undesired charge transfer are three significant factors limiting the pumping gain and power conversion efficiency. In order to solve the threshold voltage drop and body effect, the charge transfer switches (CTS) are utilized in the proposed charge pump. What’s more, an optimized substrate control strategy and body-source diode are applied to eliminate undesired charge transfer for improving power efficiency. And a complementary branch scheme is employed to reduce the output voltage ripple. The proposed charge pump is implemented in SMIC 0.18 um standard technology and the simulation results indicate better performance and high efficiency of power conversion. The proposed charge pump satisfies the relevant specifications of the charge pump applied to flash memory.

1. Introduction
As we all know, charge pump offering different output voltage to circuit system is a kind of switched-capacitor DC-DC convertor through transferring charge among capacitor networks with multiphase clock [1]. The charge pump is an integral part of the flash memory module, which uses an external power supply to generate the programming voltage required for the flash memory to operate, with a voltage range of approximately 1-7 V [2]. As the supply voltages available in flash memory systems continue to drop, the design of charge pumps for flash memory becomes more challenging. In the case of a charge pump that is inefficient at low supply voltages, conventional charge pump circuit implementations are no longer suitable for modern flash memory systems that can operate at supply voltages as low as 1.2V. Furthermore, as the ratio between the write/erase voltage and the CMOS supply voltage increases, more stages need to be cascaded to produce the desired voltage. This trend greatly increases the silicon area occupied by the charge pump, which greatly increases the size of the entire chip. Therefore, how to improve the pump gain and power efficiency of the charge pump at low input voltage has become the focus of this paper.

Most of the charge pumps are based on the circuit proposed by Dickson [3]. Figure 1 depicts the basic five-stage NMOS Dickson charge pump. The NMOS transistors are linked by diode connection so that the charge can only be transferred along the source-load direction. Analysis of Fig.1 shows that there is a threshold voltage drop loss at each stage in the Dickson charge pump. Additionally, the threshold voltage of each NMOS transistor will increase as the voltage of the source terminal increase because of the body-effect.
For low voltage systems, the conventional Dickson charge pump is not suitable due to the threshold voltage drop and body-effect, so many scholars choose the charge transfer switches (CTS) which can be turned on and off completely to take place of the diode connection NMOS [4-5]. The charge pump topology presented in Figure 2 is proposed in [5]. In this circuit, PMOS transistors are utilized as CTS to lead the charge to the load. Moreover, the floating well structure can effectively eliminate the body effect of PMOS CTSs and the gate terminal of each CTS is controlled by a CMOS inverter composed of MNi and MPi. The strategy is utilizing voltages from previous stage and next stage to turn on and off the CTSs completely which can solve the problem of threshold voltage drop effectively.

In the case where the conduction loss is kept low, the conventional CTSs charge pump circuit shown in Figure 2 has the inherent undesired charge transfer phenomenon caused by the simultaneous conduction of the auxiliary transistor and the delayed turn-off of the CTSs. Reverse charge transfer is a significant factor affecting pumping gain and power conversion efficiency. Therefore, we hope to develop a charge pump for flash memory that has a high voltage pumping gain at low input voltages, thereby eliminating poor charge transfer while maintaining conduction losses at a low level.

2. Proposed charge pump

As is shown in Figure 3, it is the proposed charge pump composed of two complementary branches with the same circuit working in completely inverted clock. An optimized gate terminal control strategy is applied to the proposed circuit. In addition to the first stage, a PMOS transistor is used as the CTS, and the body effect problem can be solved by a body-source diode connection where the drain and the body of the transistor are connected together [6]. Figure 4 is a schematic diagram of a body-source diode connection. Meanwhile, with this connection, when the CTS turns off, the CTS in a charge pump circuit can be completely shut down and prevent undesired charge transfer caused by CTS delayed turn-off. When the CTS turns on, the body-source junction diode can increase the on-time of the CTS and reduce the on-resistance. Moreover, the reverse charge transfer caused by simultaneous conduction of the auxiliary transistors can be restrained due to the gate control strategy offering completely control signal. The detailed operation is explained as follows.

2.1. First Stage
As is seen from Fig 3, there is a NMOS transistor in each branch at the first stage to transfer charge. Take the transistor MA1 as an example. During T1, the voltage of node A1 is VDD, and the voltage of node B1 is 2VDD. V_{GS} (gate-source voltage) of MA1 is greater than V_{THN}, so MA1 can be effectively turned on, and its voltage drop from drain to source is much lower than V_{THN}, effectively eliminating the threshold impact of voltage drop.

![Figure 3. Proposed charge pump circuit](image)

2.2. Middle Stages
The two auxiliary transistors at each stage are controlled by two clocks with the same phase and different amplitude generated in the circuit presented in Fig.3. Each of the middle stages have the same operating mechanism, so the third stage is chosen as an example to explain the principle. During time interval T1, both V_{A2} and V_{A3} are approximately 3VDD. V_{B2} and V_{B3} generated in branch B are about 2VDD and 4VDD, respectively. As a result, the auxiliary transfer transistor MNA3 is turned on when the gate-source voltage is VDD, and MPA3 is turned off when the gate - source voltage is -VDD. The ON state of MNA3 leads to the gate terminal MA3 of CTS connected to node B2 (VB2 is about 2VDD), and its gate drive voltage VDD turns on MA3, thereby allowing charge to be transferred from capacitor CA2 to capacitor CA3. During the time interval T2, the auxiliary transfer transistor MPA3 is turned on and MNA3 is turned off. Because the gate and source terminals of CTS MA3 are connected together through MPA3, CTS MA3 is closed, thereby cutting off the path from node A3 to node A2. Branch B, on the other hand, operates in a complementary manner.

2.3. Output Stage
The output stage operates similarly to the input stage. Each branch uses a PMOS transistor instead of an NMOS transistor. The two CTSs are turned on to charge Cout alternately, so that, in whatever charging phase and discharging phase, the current can still float into the load. In this manner, the output voltage ripple can be reduced greatly.

3. Power loss analysis
As shown in Figure 5(a), in the proposed charge pump circuit, since the two auxiliary transistors each employ a separate control signal, the reverse current due to the simultaneous conduction of the auxiliary transistors during T1 is eliminated. In Figure 5(b), in the T2 interval, as with T1, the reverse current as a result of simultaneous conduction of the auxiliary transistors can be contained, and the delay of the transfer transistor CTS is turned off due to the body-source junction diode reverse bias. The resulting undesired charge transfer is eliminated. Therefore, the proposed charge pump can cancelate the reverse charge transfer.
Figure 4. Schematic diagram of body-source diode connection

Figure 5. The voltage waveform across the CTS of the charge pump circuit. (a) Φ1: VDD ⇒ 0 Φ2: 0 ⇒ VDD (b) Φ1: 0 ⇒ VDD Φ2: VDD ⇒ 0.

4. Simulation Results
The proposed circuit of 5-stage charge pump was implemented in SMIC 0.18um standard CMOS technology and simulated in Spectre—a circuit simulation software designed by Cadence. The conventional charge pumps used for comparing performance are also implemented in this process. The frequency of the clock in the circuit is 100 MHz enabling the charge pump to drive 300uA current load. All the capacitors in the circuit with the capacitance of 12 pF are MIM-capacitors. Since the body-source diode connection is used for the substrate, all NMOS transistors are implemented using a triple well structure. All CTSs have the same size and all auxiliary transistors have the same size but smaller than CTSs in the proposed circuit. The all chip area is determined by the on-chip MIM-capacitors significantly, and the other area introduced by the circuit including CTSs and auxiliary transistors can be ignored.

Figure 6 demonstrates the output voltage and power efficient versus load current ranging from 0A to 300uA of the proposed 5-stage charge pump in 0.8V to 1.2V supply voltage. According to Figure 6(a), the output voltage reaches 7.097 V at no-load and 1.2 V supply voltage. With the increase of load current, the output voltage is reduced because of the decreased load resistance. It is shown in Figure 6(a) that the output voltage of the proposed 5-stage charge pump circuit still remains over 6 V (6.129 V) at the load current of 300 μA. Furthermore, according to Figure 6(b), under the conditions of 300uA load current and 1.2V supply voltage, the power efficiency of the proposed 5-stage charge pump can reach 77.44%. And the power efficiency still maintains over 40% while load current ranges from 25uA to 300uA. Above all, in order to keep the high efficiency of power conversion and output voltage gain, sufficient supply voltage is need to support the load current drivability. As the supply voltage drops, the performance of the circuit decreases.

Simulated output voltages versus load current of other previous works [7], [8], [9], and the proposed 5-stage charge pump at 1.2V supply voltage are revealed in Figure 7. What can be seen from the five curves is that the voltage generated by the proposed 5-stage charge pump is higher than that of
the previous works with the load current ranging from 0A to 300μA. The output voltage of Dickson charge pump is lowest as the existence of the threshold voltage drop with the same load current. The purpose of the proposed circuit is to cancel the reverse current to improving the power efficiency, but it can also reduce the conduction loss with one pumping switch used at each stage by the body-source diode connection. We can conclude from Figure 7 is that the current driving capability and output voltage is better than that of the other charge pump.

![Figure 6. Simulated output voltage (a) and power efficiency (b) of the proposed circuit with 5 stages for various load current under different supply voltages.](image)

![Figure 7. Comparison of simulated output voltage of Dickson, [7], [8], [9] and proposed charge pump circuit with 5 stages when driving a 300 μA current load with 1.2V supply voltage.](image)

Table 1. Comparison of different charge pump circuits on output voltage performance.

| Parameter                          | Dickson | [7]  | [8]  | [9]  | This work |
|------------------------------------|---------|------|------|------|-----------|
| Year                               | 1976    | 2013 | 2018 | 2018 | 2019      |
| Load current (μA)                  |         |      |      |      | 300       |
| Number of stages                   |         |      |      |      | 5         |
| Supply voltage (V)                 |         |      |      |      | 1.2       |
| Output voltage (V)                 | 1.837   | 5.295| 5.995| 5.937| 6.129     |
| Voltage gain                       | 1.53    | 4.41 | 4.99 | 4.95 | 5.12      |
| Output voltage Ripple ΔV (mV)     | 152.32  | 168.78| 19.52| 17.63| 14.04     |
| Output voltage ripple percentage ΔV/ V (%) | 8.29  | 3.19 | 0.33 | 0.29 | 0.23      |
| Start-up response time (μs)        | 0.47    | 7.23 | 1.35 | 1.47 | 1.12      |
Table 1 shows the comparison of the output voltage performance of different charge pump circuits. From this we can see that when VDD = 1.2V and the load current is 300μA, the proposed charge pump circuit is compared with Dickson, [7], [8] and [9] have higher voltage pumping gain and smaller output voltage ripple (only 14.04mV), and have the fastest response time (only 1.12μs) in addition to the Dickson charge pump.

5. Conclusion
An optimized charge pump circuit with two-phase clock scheme generated in circuit internally for reducing circuit complexity and two complementary branches for decreasing the output voltage ripple is proposed in this paper. The new gate terminal control signal generated by the two complementary branches can eliminate the undesired charge transfer caused by the simultaneous conduction of the auxiliary transistors. The reverse current floating from the CTSs is also reduced due to the delayed on or off control signal and the P-N junction of body-source diode connection. Simulation results show that the proposed charge pump circuit has an output voltage of 6.129V, a power efficiency of 77.44% when the input voltage is 1.2V and the load current is 300μA, and has faster settling time and output voltage ripple. Though the area of the on-chip MIM-capacitors accounts for the major proportions of all chip area, the shortcoming of the proposed circuit is that additional area is introduced by the two complementary branches.

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