Simple coplanar waveguide resonator mask targeting metal-substrate interface

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April 18, 2022

Abstract

This white paper presents a single-layer mask, found in Ref. [1], designed for fabrication of superconducting microwave resonators towards 1:1 comparisons of dielectric losses from the metal-substrate interface. Finite-element electromagnetic simulations are used to determine participation ratios of the four major regions of the on-chip devices, as well as to confirm lack of crosstalk between neighboring devices and demonstrate coupling tunability over three orders of magnitude. This mask is intended as an open-source community resource for facilitating precise and accurate comparisons of materials in the single-photon, millikelvin regime.

1 Introduction

Superconducting microwave resonators are a critical tool for materials loss characterization in superconducting quantum computing [2]. Resonator measurements allow us to distinguish between sources of loss impacting device performance as well as to compare losses from a variety of materials growth and fabrication processes including surface treatments and interface engineering methods.

¹https://github.com/Boulder-Cryogenic-Quantum-Testbed/simple-resonator-mask
Coplanar waveguide (CPW) resonators are commonly implemented in multi-qubit circuits for qubit control, readout, and qubit-qubit coupling. As they are generally patterned from the same single superconducting thin film that makes up the qubit capacitor pads, they are ideal for measuring losses of materials and interfaces that dominate qubit relaxation.

At power levels near a single photon of average power and temperatures in the tens of mK, superconducting CPW resonators are sensitive to materials losses due to spurious two-level states (TLS) in on-chip amorphous dielectrics, crystal defects and impurities, and contaminants within regions in the device such as the substrate, the metal-substrate (MS) interface, the substrate-air (SA) interface, and the metal-air (MA) interface [3].

The total loss induced in a resonator is equivalent to the inverse of the internal quality factor, \( Q_i = 1/\delta \). Further, the loss angle induced in a resonator due to TLS can be broken down as:

\[
\delta_{TLS} = \sum_j p_j \delta_j, \tag{1}
\]

where \( p_j \) is the participation ratio of the \( j \)-th device region, and \( \delta_j \) is the TLS loss of the \( j \)-th region. Assuming each region of interest is thin enough that the electric field changes only across the surface, the participation ratio for region \( j \) of surface area \( S \) and thickness \( t_j \) can be further expressed in terms of the electric field as:

\[
p_j \approx t_j \int_S \frac{\bar{E}^{(j)} \cdot \bar{E}^*(j) \, dS}{U_{tot}}, \tag{2}
\]

where \( \bar{E}^{(j)} \) is the electric field in this region, \( \epsilon_j \) is its relative permittivity, and \( U_{tot} \) is the total energy density. This can be solved using finite-element full-wave driven electromagnetic simulations. The level of sensitivity to regions in the device can be tuned to an extent by modifying device geometry. Changes in the CPW gap width \( g \), conductor width \( s \), and trench depth and geometry determine TLS participation ratios.

The gold standard for dielectric loss measurement of individual materials within a superconducting quantum device is outlined in Refs. [4] and [5]. This method allows the identification of loss for each individual interface in the device as well as the bulk dielectric, at the cost of requiring the measurement of 120 devices across four geometrically extreme CPW designs. For the majority of materials experiments, this precision is both unnecessary and experimentally infeasible, and the knowledge of comparative performance is sufficient. For these types of experiments, it is beneficial to have a simple mask set with many devices per chip and a high sensitivity to the device region of interest, while maintaining ease of fabrication.

For experiments varying the MS interface, such as those focused on substrate cleaning [6–9], resonators with a strong sensitivity to this interface allow higher-precision loss comparisons, and may even allow the identification of performance-improving techniques that would otherwise be obscured. In this white paper, we present a mask set designed to have an increased participation
Table 1: High-level chip design specifications.

| Specification          | Value       |
|------------------------|-------------|
| Chip dimensions        | 7.5 mm x 7.5 mm |
| CPW trace width s      | 6 µm        |
| CPW gap width g        | 3 µm        |
| Feedline impedance     | 50 Ω        |
| Resonators per chip    | 10          |
| Frequency range        | 4.6 - 7.4 GHz |
| Substrate ϵ_r          | 11.45       |
| Smallest feature size  | 3 µm        |

ratio of the MS interface as described in Ref.[5], while avoiding confounding experimental factors by maintaining simplicity in device design and associated fabrication procedures. This single-layer mask provides other features such as ~50 Ω matching on both silicon and sapphire substrates, eight resonators per chip to lend itself to statistical analysis, and tapered bond pads to reduce reflections. We also provide participation values for each device region, as well as simulations of coupler arm lengths ℓ_c to reach coupling quality factors (Q_c) spanning three orders of magnitude.

We hope this open-source mask[1] will be adopted as a standard across the burgeoning field of materials investigations for superconducting quantum computing. This design is intended to facilitate interlaboratory 1:1 comparisons between materials sets, opening the door for a higher level of device optimization than is currently possible in the field.

2 Chip design

This simple mask is a single-layer 7.5 mm x 7.5 mm chip design composed of eight quarter wave CPW resonators inductively coupled to a single feedline (Fig. 1). The feedline is connected to wirebonding pads on either side of the chip. Each chip contains resonator, feedline, and design name labels. Dicing alignment marks are not included. Individual resonator parameters from simulation are included in Table 1.

A higher-resolution image of a single quarter wave resonator is shown in Fig. 2. The top end of the resonator far from the feedline is open, whereas the end close to the feedline is shorted to ground, forming a voltage node. This induces inductance-dominated coupling between the resonator and the feedline. Both ends of the resonator are filleted to remove field singularities and corresponding losses that could arise from sharp corners.
Figure 1: Two-port single-layer chip design with overall chip dimensions of 7.5 mm x 7.5 mm. Eight multiplexed quarter wave resonators are coupled to a single common feedline, and tapered, 50 Ω-matched bond pads can be seen at the left and right of the chip.

Table 2: Simulated resonator parameters.

| Resonator label | Simulated $f_0$ [MHz] | Simulated decay rate [MHz] | Simulated $Q_c$ |
|-----------------|------------------------|-----------------------------|-----------------|
| r0              | 4600                   | 0.0094                      | 495k            |
| r1              | 5000                   | 0.0102                      | 496k            |
| r2              | 5400                   | 0.0110                      | 497k            |
| r3              | 5800                   | 0.0118                      | 499k            |
| r4              | 6200                   | 0.0126                      | 497k            |
| r5              | 6600                   | 0.0134                      | 498k            |
| r6              | 7000                   | 0.0142                      | 499k            |
| r7              | 7400                   | 0.0146                      | 512k            |
Figure 2: Graphic of a single resonator with gap width $g$ and conductor width $s$ coupled to the feedline by an inductive coupling arm of length $\ell_c$. Areas where the metallic layer is removed are shown in black, and metallized areas are shown in white.
Figure 3: Resonator coupling quality factor $Q_c$ as a function of coupler length $\ell_c$ for resonators r0 to r7. $Q_c$ is tunable by more than three orders of magnitude upon varying the length of the resonator arm parallel to the feedline (the coupler). Color curves correspond to different resonators on the chip.

3 Device simulation

Table 2 summarizes resonator parameters determined by full-wave finite element electromagnetic simulations. Resonance frequencies $f_0$ are expected to vary from simulation by up to 50 MHz due to variation in propagation speed. Here, the characteristic impedance $Z_0$ of the resonator is $\sim 50$ Ω assuming a silicon substrate ($\varepsilon_r = 11.45$), but will not deviate significantly from 50 Ω for the implementation of a sapphire substrate.

The inductive coupling strength is controlled by the length of the arm parallel to the feedline (the coupler). In this mask [1], the coupler is designed such that $Q_c \sim 500,000$. Since critical coupling is optimal for accurate fitting of $Q_i$ from the Lorentzian resonator transmission model [2], this mask is well-designed for accurate measurements of materials which induce a resonator performance of $Q_i \sim 500,000$. Materials systems with higher or lower loss can be accurately measured by lengthening or shortening the coupling arm. Fig. 3 shows $Q_c$ as a function of coupler length for all eight designed resonators, where the coupler length is defined as the portion of the resonator arm that runs parallel to the feedline. Here, $Q_c$ decreases by more than three orders of magnitude as the coupler length increases.

Fig. 3 demonstrates that resonator eigenmodes are strongly localized in this
Table 3: Participation of resonator regions determined by simulation of a 3\(\mu\)m gap CPW resonator with 100 nm of isotropic trenching.

| Region   | Participation | C (fF/\(\mu\)m) |
|----------|---------------|-----------------|
| MS       | 0.26          | 0.147           |
| SA       | 0.13          |                 |
| MA       | 0.008         |                 |
| Substrate| 89            |                 |

design, with minimal field leaking into the neighboring resonators or the feedline, so crosstalk is not anticipated to be a significant loss channel.

4 Participation of interfaces

The participation ratios of the MS, SA, MA, and substrate regions of a 3\(\mu\)m gap CPW resonator with 100 nm of isotropic trenching (as shown in Fig. 4) are reported in Table 3. Assuming interface and surface losses are around three orders of magnitude higher than substrate loss as in Ref. [4], the devices on this mask will be dominated by interface losses, with the MS interface having the largest participation by a factor of two.

5 Wirebonding

A suggested map for wirebond location and density in presented in Fig. 6. Wide resonators meanders allow wirebonding between meanders, connecting otherwise disconnected ground planes and suppressing slotline modes [10].

6 Acknowledgements

This material is based upon work supported by the U.S. Department of Energy, Office of Science, National Quantum Information Science Research Centers, Superconducting Quantum Materials and Systems Center (SQMS) under the Contract No. DE-AC02-07CH11359.

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Figure 4: Details of the finite-element electromagnetic simulation of the participation of regions within a 3 µm gap CPW resonator with 100 nm of isotropic trenching. Top: Cross-section of simulated gap region, with metal shown as blue and substrate shown as grey. Middle: Electric field diagram. Bottom: Mesh density.
Figure 5: Eigenmode of one of the resonators. Modes are strongly localized around resonators with minimal leakage.

Figure 6: Recommended internal wirebonding schematic, with isolation bonds over the resonators and feedline marked in red.
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