OPTIMIZATION OF CODE IDENTIFIER USING TGL AND DVL

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Abstract: The design of 2:4 and 4:16 decoder using 14 multiple logics is proposed. As the power is very important key role in IC. Also to provide lower power consumption with high performance is challenging task. To provide such a performance the design of low power high performance is discussed. The decoder is designed based on TGL, DVL and complementary metal oxide semiconductor (CMOS). The decoder is discussed with low power scheme. The design is implemented on tanner tool. The comparative analysis of static current and power dissipation are calculated.

Keywords: Power consumption, decoder, CMOS.

1. Introduction

In today’s era optimization in power of a circuit is very important concern to design a circuit. Design of low power circuit it is very challenging battery backup. It is problem for the high performance design circuit. The size of the chip should be small and for faster operation the requirement of high frequency of operation. The design of low energy design is needed. As this specification are useful in every electronic gadget. Decoder is a combinational circuit which consist of m input and $2^m$ output. It consists of select line also known as enable. Whenever the enable is one the input is attached to the output. The decoder is used in mux, selecting row or column for memory address.7 segment display, etc.

In the field of VLSI battery would worked last long necessity of versatile and convenient gadgets also it is because of expanding increase of semiconductors on a solitary chip. The min. force necessities of current computerized frameworks required the investigation of innovative, structural and circuitual arrangements that permit a decrease of the energy dispersed by an mos. Most of the fundamental driver of energy dispersal in CMOS circuits is because of the switching of transistor. The transistor count is also important if the circuit reduces the number of transistor the power dissipation automatically reduces. Some of the techniques are discussed with their circuit to design 2:4 decoder.

2. Existing System

Cmos are used in various types of logic gates in Ic’s. It consists of pmos pullup and nmos pulldown mos which result in good performance. Along these lines, CMOS rationale is portrayed by toughness opposes voltage variation and semiconductor electronic semiconductor size and accordingly dependable activity at low voltages and little semiconductor sizes. Information signals are associated with semiconductor unit entryways exclusively, giving diminished style quality and assistance of cell based generally rationale combination and tastefulness. Pass-semiconductor rationale was mainly evolved among the Nineties, when various style plans were presented, advancing to offer a reasonable distinctive to MOS rational and enhances speed, force and space. Its principle style qualification is that inputs ar given to each the entryways also the diffusion terminals of transistors i.e source/drain. Pass semiconductor unit circuits ar enforced by single nMOS/pMOS pass semiconductor or parallel pairs referred to as transmission gates. The use of these circuit makes a combined-logic style method for line decoder (LD), combining gates of assorted logic to the identical circuit, in an endeavor to induce enhances performance over a single vogue style. LD are basic circuits, wide used within the electronic equipment of memory (e.g. SRAM), mux, design of logic functions, etc.

3. Design Methodology

3.1. 2-4 Line Decoder

This decoder takes n bit binary no. and change to $2^n$ o/p lines. grab an n-digit binary number and converts it into 2n data lines. The basic decoder is 1:2.

Figure: 1 Blok diagram of basicDecoder
2-4 NAND decoder consist of 2 input and 4 outputs. Table 1 shows the complete functionality of decoder. Based on two input output are selected but the select line must be high. Table 2 shows the Inverted (I) decoder where the selected output gives low and rest of the output gives high. It is also called as code identifier.

| A | B | D0 | D1 | D2 | D3 |
|---|---|----|----|----|----|
| 0 | 0 | 1  | 0  | 0  | 0  |
| 0 | 1 | 0  | 1  | 0  | 0  |
| 1 | 0 | 0  | 0  | 1  | 0  |
| 1 | 1 | 0  | 0  | 0  | 1  |

Table 1: 2-4 decoder Truth Value

| A | B | I0 | I1 | I2 | I3 |
|---|---|----|----|----|----|
| 0 | 0 | 0  | 1  | 1  | 1  |
| 0 | 1 | 1  | 0  | 1  | 1  |
| 1 | 0 | 1  | 1  | 0  | 0  |
| 1 | 1 | 1  | 1  | 0  | 0  |

Table 2: 2-4 Inverted decoder Truth Value

3.3 NEW MIXED-LOGIC DESIGNS

2-4 LD designed by TGL or DVL gates. It requires sixteen transistors. By mixture each gate varieties into a similar topography and victimization correct signal structure, it’s attainable to wipe out one in all the two invertors, so decreasing the whole semiconductor device no. to fourteen. A 14-transistor topology (9 nMOS, 5pMOS). The close setting with OR gates, a 2:4 I LD square measure usually enforced with fourteen transistors (5nMOS, 9pMOS), I0, I2 square measure enforced with TGL (B as propagating signal) and I1, I3 square measure enforced with DVL (A as propagate signal). The B electrical converter will another time be eliminated. The electrical converter elimination reduces semiconductor device no., logical style and complete change scheme of the circuits, thus cut down power drain. fourteen is that the lower range of transistors needed to understand a full-swinging 2-4line code identifier with static logic. The 2 new scheme square measure named ‘2-

4 LP’ and ‘2-4LP’ (I: inverting LP: low power). Their design shown in fig four and fig five.

3.2. 4-16 LD with 2-4 Pre decoders

Fig. 3. CMOS based 4–16 decoder using 104 transistor
(a) NI code identifier implemented with Pre decoders and NOR-based post decoder.
(b) I code identifier implemented with 2-4 noninverting pre-decoder

Fig. 4. 14-transistor 2–4 LD. (a) 2–4LP. (b) 2–4LPI.
1. Design Implementation:

Design of 2:4 LP and LPI as well as 2:4 HP and HPI are implemented in Tanner tool. The schematic and their simulation result are shown below.
4. Conclusion

The design of 2:4 decoders with and low power inverted is successfully design and implemented in 180nm technology file. The design of 2:4 LPI and HPI are having lower static current and power dissipation. In future scope the design can be implemented in 90nm as well as 50nm technology file to reduce more static current and power consumption.

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