A Discuss on a Thermal Conductive Panel of FPGA

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Keywords: Thermal analysis, CAE, Finite element analysis, Contact thermal resistance.

Abstract. In this paper a mounted problem about a thermal conductive panel which is used for a FPGA chip being used on satellite and in vacuum environment is discussed. In order to decide whether the panel could be un-mounted when carrying electronic testing in air condition under high and low temperature environment, a simulation analysis is done and the different of convection for the air condition and the thermal contact resistance is considered. The analysis results showed that the temperature of FPGA un-mounting the thermal conductive panel is within the permitted temperature and the final testing have been done in which the box work well. Through the efficiency analysis the time cost and project cost are all saved.

Introduction

Usually the heat conductive way is different in air and in vacuum. In our project a satellite electric box will be test in high and low temperature environment in air condition before it is equipped in the following procedures. The problem is that one of the thermal conductive panel was hoped not to be mounted on the surface of the heat component when in the testing because in one of the following procedures the panel is still need to been removed and this maybe take new problems. So in this paper the analysis was done to find whether the heat conductive panel could be un-mounted on the component when in the high and low temperature testing.

Methods and Analysis Procedure

Information and Structure of the Electric Box

The box is one part of an electric equipment on satellite which will work in vacuum environment. The basic material is aluminum and the most high heat component is a FPGA chip. The heat power consumption of FPGA in this box is 3.625 W\textit{att} and in order to avoid too high temperature the heat should be conducted to the outer of the box and then to the satellite. In vacuum the heat in the inner of the box need be conducted mostly through heat conductivity because the convection could not be functional without air and the radiation is functional little in the inner of the box. The conductivity of the PCB is not enough to dissipate the heat, so a thermal copper conductive panel is used in this box which one end is connected with the aluminum structure and the other end is connected with the top surface of chip (as shown in Fig.1).

And the total structure is shown in Figure.2.
Change of Thermal Resistance. Contact thermal resistance $R_c$ could be computed refer with Eq.1 and the temperature improvement for the contact $\Delta T_c$ could be computed refer with Eq.2

$$R_c = \frac{1}{h_c A_c}$$ (1)

$$\Delta T_c = R_c \cdot Q$$ (2)

Where $A_c$ is contact area, $h_c$ is the contact heat conductivity and $Q$ is heat power consumption.

The convection thermal resistance $R_a$ and the temperature improvement could be computed refer with Eq.3 and Eq.4,

$$R_a = \frac{1}{h_a A_a}$$ (3)

$$\Delta T_a = R_a \cdot Q$$ (4)

Where $A_a$ is convection area and $h_a$ is the convection heat conductivity.

The most important changes of heat transfer when changing the box from vacuum to air environment is that the contact thermal resistance and convection. The reason why the contact thermal resistances change is that the contact heat conductivity will change, for the air will fill in little crevices of the contact interface so more heat could be conduct through the interface. Usually the value of contact thermal conductivity could be improved one or two order higher in air condition [1-3]. The convection changes obviously because there is no convection heat transfer in vacuum.

The changes that there add the convection heat transfer and the contact thermal resistance improved one or two order make it possible to un-mount the heat conductivity panel of FPGA for the heat dissipation condition become better.
**Equations of Temperature.** The junction temperature of chip could be computed refer with Eq. 5,

\[ T_j = T_c + Q \cdot R_{jc} \]  \hspace{1cm} (5)

Where \( T_c \) is the case temperature of chip and \( R_{jc} \) is the thermal resistance from case to junction.

**Simulation Model.** A finite element model is built in order to do the simulation analysis (refer with Fig.3).

![Finite element model of thermal analysis.](image)

**Computing Parameter.** The contact thermal conductivity is valued in the scope of 800 to 3000 W/(m\(^2\)K) when have some heat filling filled in the contact interface in vacuum and in the scope of 8000 to 12000 W/(m\(^2\)K) when in air condition. The convection heat conductivity is valued 5 when in natural convection and 25 W/(m\(^2\)K) when in forced convection.

**Results and Discussion**

The permitted derated case temperature of the FPGA chip is 70 °C according the Eq.5. The case temperature of the chip is 67.9 °C (refer with Fig.4 a) in vacuum and when the thermal conductivity panel is removed the temperature changed to 75.8 °C (refer with Fig.4 b) which is over the permitted temperature.

![Temperature change of the chip after un-mounting the thermal conductivity panel in vacuum environment.](image)

(a) Mount thermal conductivity panel  
Case temperature of FPGA chip is 67.9°C  
(b) Un-mount thermal conductivity panel  
Case temperature of FPGA chip is 75.8°C

When only considering contact thermal conductivity change or only considering convection change the case temperature of FPGA chip is 70.5°C and 75.0°C respectively, and 5.6°C and 0.8°C drop contract to result in vacuum (refer with Fig. 5). When considering both these two factors the case temperature of chip is 70.0°C (refer with Fig. 6) which satisfy the permitted temperature, and because the permitted temperature has leave enough tolerance to the most maximum temperature so it could be decided that the experiment is safe when the thermal conductivity panel is un-mounted for this project.

The electrical test experiment has been done after the decision and the equipment work well.
Summary

1. For the box in this paper the thermal conductivity panel could be un-mounted when carrying electrical testing in high and low temperature environment through the temperature analysis.

2. It is found during the analysis that when change from vacuum environment to air environment the change for contact thermal resistance helps to dissipate heat and decease temperature of chip more than the convection of the outer of the structure.

Acknowledgement

This paper is supported by Youth Innovation Promotion Association, Chinese Academy of Sciences and the Knowledge Innovation Program of the Chinese Academy of Sciences.

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