Research Article

A 0.8–6 GHz Wideband Receiver Front-End for Software-Defined Radio

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A wideband (0.8–6 GHz) receiver front-end (RFE) utilizing a shunt resistive feedback low-noise amplifier (LNA) and a micromixer is realized in 90 nm CMOS technology for software-defined radio (SDR) applications. With the shunt resistive feedback and series inductive peaking, the proposed LNA is able to achieve a wideband frequency response in input matching, power gain and noise figure (NF). A micromixer down converts the radio signal and performs single-to-differential transition. Measurements show the conversion gain higher than 17 dB and input matching (S11) better than \(-7.3\) dB from 0.8 to 6 GHz. The IIP3 ranges from \(-7\) to \(-10\) dBm, and the NF from 4.5 to 5.9 dB. This wideband receiver occupies 0.48 mm\(^2\) and consumes 13 mW.

1. Introduction

Software-defined radio was designed to process any signal within a certain bandwidth [1]. For an SDR in 0.8–6 GHz region, it includes signals of GSM, 3G, WLAN, Bluetooth, WiMAX, and GPS applications. Such an idea can be realized by using an ultra-high speed ADC for direct sampling, but the power consumption of the high speed ADC is too large to accept. Relatively, a SDR receiver that down-converts signals before ADC appears to be a more practical approach.

The intuitive SDR receiver topology is to connect front-ends of different standards in parallel as shown in Figure 1(a); nevertheless, the chip size of such topology would be too large. A wideband radio [2–6] and a tunable-band radio [7–9] (see Figure 1(b)) are good candidates for this purpose. The most challenging problem is how to design an LNA and a mixer that meet all the requirements in such a wideband from 800 MHz to 6 GHz.

A wideband RFE can be implemented by several circuit structures. Conventional common-gate LNAs feature wide input matching and gain bandwidths [4]. However, the multiple stages required by such circuits for gain and noise flatness can be power hungry. A shunt-shunt feedback LNA followed by a passive mixer [2, 5, 6] can be an option, but its gain degrades at high frequency due to the large capacitance at its input and output stages. Besides, the trade-off between noise figure and bandwidth remains an issue. Tunable-band receivers switching its frequency with tunable passive devices [7–9] would be promising, except that the size of passive devices is too costly to accept. Designs of mixers can be also challenging for SDR. Passive mixers are widely used for frequency down-conversion. Very large power is needed for LO input to drive these passive mixers which results in power consumption and interference problems.

In order to solve the above issues, a wideband RFE utilizing a resistive feedback LNA and a micromixer is proposed. This LNA adopts the resistive feedback technique and inductive peaking to extend the bandwidth [10, 11]. The micromixer [12–14] topology is used for down-conversion as well as single-to-differential transition in a wide frequency range without the high LO signal power requirement. As a result, this RFE accomplishes the wideband, low power, and small size criteria of SDR applications.

2. Receiver Architecture

Figure 2 shows the block diagram of the proposed SDR system. The receiver comprises a 0.8–6 GHz wideband LNA, two micromixers, baseband blocks, a frequency divider, and
an LO signal generator. Requirements of the LNA include flat frequency responses of high gain and low NF, wideband matching, and good phase linearity (i.e., small group delay variation). After LNA, the I/Q micromixers downconvert signal frequency to a lower band for baseband signal processing. In addition, the frequency divider can generate differential I/Q LO signals.

3. Design of Wideband Receiver Front-End

Figure 3 shows the schematic of the proposed RFE. Resistive feedback and inductive peaking technique are adopted in the LNA. The amplified signal is coupled through a capacitor $C_C$ to a micromixer. Design principles of each stage are described as follows.

### 3.1. Wideband LNA

The small-signal model of the proposed LNA is shown in Figure 4, where the $R_f$ equal to $(R_{FB} + R_M)/(1 + g_m R_M)$ is the impedance looking into the input of the LNA after the gate inductor $L_g$, and $R_M$ equal to $(1/g_{mM1}/1/g_{mM2})$ is the input impedance of the micromixer. The input impedance is expressed by (1) with parameters mapping onto Figure 3. Note that $C_p$ represents parasitic capacitance at the input node, and $C_{in}$ represents the input dc blocking capacitor,

$$Z_{in} = \frac{1}{s C_{in}} + \frac{s^2 R_f C_{gs1} L_g + s L_g + R_f}{s^3 R_f C_{gs1} C_p L_g + s^2 L_g C_p + s R_f (C_{gs1} + C_p) + 1}.$$  \hspace{1cm} (1)

As the input impedance of the conventional resistive shunt-shunt feedback amplifier, $R_f$ provides 50 Ω input matching. Since $C_{in}$ and $C_{FB}$ will affect the low frequency matching, they are chosen to be as large as possible (7 pF and 3 pF, resp.). In order to extend the matching range to higher frequencies, a series inductor $L_g$ is added to generate a dip in the frequency response of input matching ($S_{11}$). The dip frequency is determined by $L_g$ and $C_{gs1}$ values, which are 1.2 nH and 257 fF, respectively. The input matching of the LNA can be calculated by substituting (1) into (2),

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}.$$  \hspace{1cm} (2)

The voltage gain of the LNA, $A_v$, can be derived and separated by $A_u$ and $A_{vc}$ expressions as illustrated in (3)–(5),

$$A_v = A_u \times A_{vc},$$  \hspace{1cm} (3)

$$A_u = s R_f C_{in} \left( s^3 L_g C_{gs1} C_{in} R_f + s^2 (L_g C_{in} + R_f R_S C_{gs1} C_{in}) \right. \left. + s \left( R_f C_{in} + R_f C_{gs1} + R_S C_{in} \right) + 1 \right)^{-1},$$  \hspace{1cm} (4)
Figure 3: Schematic of proposed receiver front-end.

Figure 4: Small-signal model of wideband LNA.

\[
A_{\text{lc}} = \frac{(1/C_{d2}L_p) (R_{FB}/R_M) ((1/R_{FB}) - g_{m1})}{s^2 + s (\omega_{lb}/Q_c) + \omega_{0c}^2},
\]

where

\[
\omega_{lb} = \sqrt{\frac{1}{C_{d2}L_p}},
\]

\[
Q_c = \frac{1}{R_{FB}/R_M} \sqrt{\frac{L_p}{C_{d2}}}.
\]

\[C_{d2}\] is the capacitance looking into the drain of \(M2\) and \(L_p\) is the peaking inductor. Since gain starts decreasing at the frequency \(1/2\pi (R_{FB}/R_M) C_{d2}\) and the degradation becomes even more serious due to the large size of transistors \(M1\) and \(M2\), \(L_p\) is used to resonate out \(C_{d2}\) and extend the bandwidth. The sizes of \(M1\) and \(M2\) are of the same size: 32 fingers with a \(W/L\) ratio of 8 \(\mu m/90\ nm\) per finger. The inductance of \(L_p\) is 0.55 nH.

The noise figure of the LNA is derived according to [11]:

\[F_{\text{LNA}} = 1 + \frac{R_g + R_{sg} + R_{ss}}{R_s} + \frac{\alpha \delta \omega^2 C_{g_{m1}}}{5g_{m1} R_s} \times \left( R_s - \omega^2 L_g R_s C_p \right)^2 + \omega^2 L_g^2 \]

\[\times \left[ \frac{R_{FB}}{R_s} \right]^2 + \frac{R_{FB}}{R_s} \left( \frac{L_g}{R_{FB}} + \frac{C_{g_{m1}}}{R_{FB}} \right) + \left( \frac{R_s}{R_{FB}} \right) + 1 \right]^2 + \gamma R_{m1} R_{FB} \]

\[\times \left( g_{m1} - \frac{1}{m R_{FB}} \right)^{-1} \right]^2,
\]

where

\[m = \frac{1}{1 + s^2 C_{d2} L_p}.
\]

\(R_s\) represents the source resistance, \(R_g\) represents the gate resistance of \(M1\), \(R_{sg}\) represents the source resistance of \(M1\), \(R_{ss}\) represents the series resistance of the gate inductor, \(\delta\) and \(\gamma\) are the coefficients of gate noise and channel noise, and \(\alpha\) is the ratio of \(g_{m1}\) to zero-bias drain conductance \(g_{d0}\).

Note that \(R_{FB}\) affects the input matching, gain, and noise figure. A large \(R_{FB}\) improves the gain and noise performance but results in significant variation across the frequency band. To perform the maximum flat frequency response, a resistance of 340 \(\Omega\) is used.

Apart from bandwidth extension, the resistive feedback topology improves the linearity of the amplifier [15]. However, the improvement can be observed only in the lower frequency range because of the limited feedback loop bandwidth, as will be seen in the measurement results.

3.2. Micromixer. A micromixer possesses wideband input matching, high linearity, and single-to-differential conversion ability, which makes this topology suitable for the proposed SDR application.
Single-to-differential conversion is accomplished by injecting the signal current into the source of transistor M3, and replicating this current to M5 with the opposite current direction. The sizes of transistors M1–M4 are the same and equals to 48 μm/90 nm to balance both paths. Frequency down-conversion is completed by the switching core M5–M8 whose sizes are 90 μm/90 nm. The output load resistor R_L is parallel with C_L to filter out high frequency noise and harmonics. C_L (10.8 pF) and R_L (500 Ω) generate a pole at 29.5 MHz for sufficient IF bandwidth. To ensure the single-to-differential conversion, the operation frequency of the micromixer should be well below the dominant pole frequency, which is ω_L/2 contributed by 1/g_m from M1 and 2C_gsi from M3 and M4. For a 90 nm CMOS technology, the cut-off frequency f_T is as high as 80 GHz; therefore, such topology remains suitable in the interested frequency range.

The conversion gain of the micromixer can be derived as (9), assuming the switching pair operates ideally,

\[ A_{vm} = \frac{2}{\pi} (g_{mM2} + g_{mM3}) R_L. \quad (9) \]

The noise factor of the mixer can be obtained by [16] and expressed as follows:

\[ F_{Mixer} = \frac{\beta}{c^2} + \left( 2 \left( \gamma_{M3} + r_gM3g_m \right) \beta g_m + 4Y_{M5} \overline{\gamma} \right) + 4r_gM5 \overline{\gamma} + \frac{1}{R_L} \right) \left( c^2 \frac{g_m^2 R_s}{A} \right)^{-1}, \quad (10) \]

where

\[ \frac{2I}{\pi A} \], \quad (11) \]

\[ \beta \] and \( c \) are evaluated with the bias current of each switching pair; \( \gamma \) and \( r_g \) are the noise factor and gate resistance of each transistor; \( g_m \) the transconductance of the \( g_m \) stage \( (g_m = g_{mM2} + g_{mM3}) \), and \( I \) the current passing through M1 and M3. \( A \) is the amplitude of the LO signal and \( R_L \) is the load resistance of the micromixer. When LO amplitude becomes large enough, \( \beta \) and \( c \) start to approach 1 and 2/π, respectively. The effect of the LO port and gate resistance in \( g_m \) stage is so small that the noise factor can be reduced as (12):

\[ F_{Mixer} \approx \frac{\beta}{c^2} + \frac{2Y_M g_m + 4Y_{M5} \overline{\gamma} + (1/R_L)}{c^2 g_m^2 R_s}. \quad (12) \]

The conversion gain of the RFE can be expressed by the product of (3) and (9) and used in the following discussions. Similarly, the noise performance, dominated by LNA, is derived as (14) according to Friis noise formula for further comparisons,

\[ A_{vRX} = A_{vL} \times A_{vC} \times A_{vm}, \quad (13) \]

\[ F_{RX} = F_{LNA} + \frac{(F_{Mixer} - 1)}{A_v}. \quad (14) \]

4. Measurement Results and Discussion

The RFE was realized in 1P9M 90 nm CMOS technology. On-wafer measurement was performed by using an Agilent 8722ES network analyzer for input matching measurements. Signal generators Agilent E8257D and Agilent E4438C are used to provide LO and RF signals, respectively. Spectrum analyzer Agilent E4440A is used for IF spectrum and noise figure measurements.

Figure 5 shows the measured, calculated, and simulated input matching versus frequency characteristics of the RFE. The S11 is below –10 dB in 1.2–8.9 GHz and –7.3 dB in 0.8–1.2 GHz, respectively. The first dip is determined by \( R_f \) and \( C_{in} \) at low frequency. The second dip is located by \( L_g \) and \( C_{gr} \) at high frequency. Figure 6 shows the measured, calculated, and simulated conversion gain versus frequency characteristics of the RFE. The measured conversion gain is larger than 17 dB from 0.8 to 6 GHz owing to the peaking.
Table 1: Summary of the implemented and recently reported state-of-the-art CMOS wideband and tunable-band receiver front-ends.

| Frequency (GHz) | $S_{11}$ (dB) | $\gamma$ Conversion gain (dB) | Noise figure (dB) | IIP3 (dBm) | Supply voltage (V) | Power (mW) | Area (mm$^2$) | Technology |
|----------------|---------------|-------------------------------|------------------|------------|-------------------|------------|--------------|------------|
| This work      | 0.8–6         | -7.6                          | 17–20*           | -10–7.3   | 1                 | 15*        | 0.48*        | 90 nm CMOS |
| [2] 2008 ISSCC | 0.6–10        | < -10                         | 14*              | 0          | 1.2               | 30*        | 1*           | 45 nm CMOS |
| [3] 2007 ISSCC | 2–8           | -8                            | 23*              | -7         | 1.2               | 27.8*      | 0.48*        | 65 nm CMOS |
| [4] 2006 JSSC  | 0.8–6         | N/A                           | 18–20*           | -3.5       | 2.5               | 28.5*      | 3.8*         | 90 nm CMOS |
| [5] 2012 TMTT  | 0.6–3         | -<8                           | 42–48*           | -14        | 1.2               | 30*        | 1.5*         | 130 nm CMOS|
| [6] 2011 RFIC  | 0.1–3         | N/A                           | 33–55*           | N/A        | 1.2               | 14.5–48.5* | 2.2*         | 130 nm CMOS|
| [7] 2009 JSSC  | 0.1–5         | N/A                           | -2–82*           | -10–3     | 1.1               | 59–115*    | 2*           | 45 nm CMOS |
| [8] 2008 MWCL  | 3–5           | -<7.6                         | 19.8–24.6*       | > -6       | 2                 | 16*        | 1.14*        | 0.18 um CMOS|
| [9] 2006 ISSCC | 3–8           | N/A                           | 15–21*           | 5–6.5     | 2.3               | 44.9*      | 0.35*        | 0.18 um CMOS|

*Front-end; LNA only; Whole receiver; active area only.

inductor $L_p$ technique. The declining response at lower frequency is due to the finite value of blocking capacitance $C_{\text{in}}$. Figure 7 shows the measured, calculated, and simulated noise figure versus frequency characteristics of the RFE. The noise figure varies within 5.2 ± 0.7 dB in the covered frequency range.

The input third intercept points (IIP3) are in the range from −10 to −7 dBm over the frequency of interest as shown in Figure 8. As aforementioned, the IIP3 rolls off at higher frequency due to the limited bandwidth of the feedback loop. The power consumption of the LNA and micromixer are 11.5 and 1.5 mW, respectively, under the supply voltage of 1 V. A summary of the implemented and recently reported CMOS wideband and tunable-band RFEs is given in Table 1.

The chip area is 0.48 mm$^2$ including testing pads as shown in Figure 9. The off-chip choke inductor $L_C$ can be implemented by integrated passive device (IPD) technique [17] for future integration. In this work, the inductor $L_C$ is replaced by a bias-T to demonstrate the RFE performance.

5. Conclusion

A wideband RFE from 0.8 to 6 GHz is proposed by using a resistive feedback amplifier and a micromixer. The measurement results show a flat and wideband feature in input matching, gain, and noise performance. The proposed RFE
features the lowest power consumption (13mW) among recently reported silicon-based RFES in 0.8–6 GHz range.

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