ZCSD: a Computational Storage Device over Zoned Namespaces (ZNS) SSDs

Corne Lukken, Giulia Frascaria, and Animesh Trivedi
Vrije Universiteit Amsterdam

Abstract

The Big Data trend is putting strain on modern storage systems, which have to support high-performance I/O accesses for the large quantities of data. With the prevalent Von Neumann computing architecture, this data is constantly moved back and forth between the computing (i.e., CPU) and storage entities (DRAM, Non-Volatile Memory NVM storage). Hence, as the data volume grows, this constant data movement between the CPU and storage devices has emerged as a key performance bottleneck. To improve the situation, researchers have advocated to leverage computational storage devices (CSDs), which offer a programmable interface to run user-defined data processing operations close to the storage without excessive data movement, thus offering performance improvements. However, despite its potential, building CSD-aware applications remains a challenging task due to the lack of exploration and experimentations with the right API and abstraction. This is due to the limited accessibility to latest CSD/NVM devices, emerging device interfaces, and closed-source software internals of the devices. To remedy the situation, in this work we present an open-source CSD prototype over emerging NVMe Zoned Namespaces (ZNS) SSDs and an interface that can be used to explore application designs for CSD/NVM storage devices. In this paper we summarize the current state of the practice with CSD devices, make a case for designing a CSD prototype with the ZNS interface and eBPF (ZCSD), and present our initial findings. The prototype is available at https://github.com/Dantali0n/qemu-csd.

1 Introduction

In the age of Big Data, every day we generate 2.5 Exabytes (10^{18}) of data, and by 2025 this rate will grow to 480 Exabytes/day (a 192-fold increase) to generate 175 Zettabytes of data per year [25]. With the prevalent Von Neumann computing architecture, this vast amount of data is stored and processed in separate architectural entities, with storage devices such as hard-disk drives (HDDs) or solid state drives (SSDs) only passively storing data [42]. When needed, data is moved between storage devices and DRAM to be processed by the CPU. However, while the data growth is exploding, the CPU performance improvements and link speeds (over which data movement happens, e.g., PCIe or Ethernet) are not projected to improve at the same rate over the next 5 years. Consequently, the excessive data movement with a system for CPU-driven data processing has become the key performance bottleneck for data-intensive workloads [6].

One promising avenue to solve the challenges associated with excessive data movement is to push compute to storage, rather than pull data from storage to compute (i.e., the CPU). Today researchers are actively exploring the possibility of “Programmable Storage” or “Computational Storage” devices (CSD) [7,14,16,17,24,27,28,30,34,41,44,46,50,51]. The idea of programmable storage is not new, and has been explored previously with HDDs [5, 22, 31, 43], though the low disk bandwidths dominated the data processing costs. With the rise of Non-Volatile Memory (NVM) storage the idea is being revisited as NVM SSDs offer significant device-internal bandwidths [18], and already have an element of programmability to run management code like Flash Translation Layer (FTL) for NAND flash chips. The elimination (or reduction) of data movement due to storage programmability offers energy, cost, and performance benefits.

Despite its potential, building applications for programmable storage remains challenging due to multiple reasons [8]. First, there is no de-facto device design for CSD devices. Previous efforts have explored delivering programmability with the use of embedded CPUs [46], FGPA [44, 51], ASICs/ARM cores [16, 17], and there are on-going efforts to work on standardization from SNIA [47]. A few closed-source CSD devices are available in the market now, albeit with limited availability [19,39,45]. Due to the complexity and limited accessibility to the device internals, it is challenging to explore the right computational hardware model (ISA, microarchitectural properties), and its host integration interface. Second,
| Hardware                     | Software API                  | Open | Comments                                                                                                                                 |
|------------------------------|-------------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------|
| Smart SSDs [30]              | RISC processor                | MapReduce | use an object-based communication protocol, OS/application transparent analysis functions fused with the FTL, not possible to change them |
| Active Flash [50]            | ARM SATA controller           | Statistical analysis functions | analytics, statistical and database scan and filter operators implemented |
| Intelligent SSDs [14]        | ASICs, reconfigurable stream processors | Map-Reduce, OpenCL | Pre-compiled selection and aggregation operators into the SSD FTL Supports arbitrary user code and integration with the host file system |
| SmartSSD [17]               | Embedded SSD CPU             | 3 new commands for a session-based protocol | FPGA as implicit co-processor, groupby and filter offload to an FPGA Supports C++11, I/O queues, multithreading, and dynamic memory in an SSD |
| Willow [46]                  | RISC processor                | RPC / Client-server            | supports opportunistic offloading of code to SSDs, no file system integration focus on key-value store operations (get, put, delete, scan) only full database integration with MariaDB query plans for query offloading supports opportunistic offloading of code to SSDs, no file system integration |
| Ibex [51]                    | FPGA                          | MySQL storage engine          | workload-specific acceleration (regex only)                                                                                                                     |
| Biscuit [24]                 | ARM Cortex R7 cores           | Dataflow operators            | Full integration with the host file system, virtual file abstraction, requires FPGA knowhow workload-specific (feature extraction, deep-learning, and graph search) offloading general-purpose, enterprise-grade, CSDs appear as a networked machine with attached storage supports general-purpose eBPF code execution on (read/write/transform) files inside a SSD |
| Caribou (also [54])          | FPGA                          | Key-Value operations          | Yes                                                                                         |
| Caribou [27]                 | ARM Cortex R7 cores           | Database query offloading user functions on flash pages | No                                                                                         |
| Summarizer [34]              | ARM cores/FPGA                | specific calls to process files | No                                                                                         |
| Registor [41]                | FPGA with RegEx IC modules    | specific r/w calls on flash PBAs | Yes                                                                                         |
| INSIDER [44]                 | FPGA                          | RPC/Client-server             | Yes                                                                                         |
| CognitiveSSD [37]            | (FPGA with ARM Cortex-A9 cores) | OpenSSD [4]                  | supports opportunistic offloading of code to SSDs, no file system integration focus on key-value store operations (get, put, delete, scan) only full database integration with MariaDB query plans for query offloading supports opportunistic offloading of code to SSDs, no file system integration workload-specific acceleration (regex only) Full integration with the host file system, virtual file abstraction, requires FPGA knowhow workload-specific (feature extraction, deep-learning, and graph search) offloading general-purpose, enterprise-grade, CSDs appear as a networked machine with attached storage supports general-purpose eBPF code execution on (read/write/transform) files inside a SSD |
| NGD Newport [16]             | ARM cortex A53 (64-bits)      | RPC / Client-server           | No                                                                                         |
| blockNDP [7]                 | OpenSSD [4]                   | eBPF code, shared memory      | Not yet supports general-purpose eBPF code execution on (read/write/transform) files inside a SSD |
| ZCSD (work-in-progress)      | Any (eBPF-supported), QEMU host CPU | eBPF code, shared memory      | Yes Supports ZNS NVMe devices, integration with files/SPDK, uses NVMe command set |

Table 1: Related work and comparison of recent CSD projects including work-in-progress ZCSD prototype (this work).
there are no standard CSD programming abstractions, APIs, or programming models (dataflow, client-server, and shared memory) [8]. Often the device manufacturers select the programming model, rather than letting developers choose the one that is the most suitable for their workload. Choosing an appropriate programming model necessitates an end-to-end visibility in the application design, host storage stack, and CSD internals due to the closed-nature of devices, and the semantic gap between these components. A CSD device has limited visibility into application-level data structures and file system data layouts. Likewise, the application is oblivious to CSD internal FTL and GC operations that can potentially change the data location. Lastly, due to the shared and multi-tenant nature of storage devices, CSD prototypes dedicated to one client or application [17,41] without security and privacy mechanisms are of limited usability. As a result, there is a need for a systematic evaluation of design choices for a data-intensive application (e.g., databases, analytics, AI/ML, searching and indexing) for programmable storage devices.

To facilitate such exploration, we present a Zoned Computation Storage Device (ZCSD) software prototype in QEMU [10]. Two key decisions shape the ZCSD design:

1.1 Why Zoned Namespaces (ZNS) Devices

The ZNS interface is the emerging standard (ratified by the NVM Express consortium as of June 2020) that allows host applications to have visibility and control over data placement and garbage collection operations in SSDs [1,48]. It is a standardized, technical successor of Open-Channel [12], streaming [29], and Software-defined SSDs [40]. The key features of the ZNS interface are (i) it does not allow in-place updates to written data; and (ii) zone reset and garbage cleaning must be done by the host software. As a result, the host software (including file systems) must become aware of append-only properties of data stored on ZNS devices. Such append-only properties with visibility and control over SSD devices are very attractive to design a clear end-to-end APIs, and programming models with data consistency models, which was not possible before. We currently lack such end-to-end consistency models [8]. For example, multiple versions of data inside a log-structured file systems (e.g., F2FS) and ZNS can be trivially used to build a write-once data semantics model with shared memory.

1.2 Why eBPF for programmability

With the notion of programmability we mean ability to run user-provided code in a dynamic and safe manner. Programmability can be supported by different software (kernel [kernel modules], file system [integration with the VFS], runtime and languages [Webssembly, Rust]) and hardware (FPGAs, ASICs, embedded CPUs) targets in the storage stack. Diverse user requirements for open CSD exploration necessitate not being limited by restrictions from one particular “programmability” implementation. Naturally, the closer to storage that we can run the code (Near-Data Processing) the better it is for performance. In this work, we advocate to use eBPF (extended Berkeley Packet Filter) language and toolchain [15,38] for three key reasons. First, eBPF instructed set is not tied to an application-domain like databases and it has already been used in networking [53], tracing [23], security [32], and even storage [7,9,11,35,52]. Second, due to the simplified nature of the eBPF instruction set, it is possible to verify for correctness and bounded execution of extensions. The Linux kernel already ships with an eBPF verifier [49], and multiple other prototypes are available [2,21]. Lastly, eBPF can support highly efficient code generation (via JITing) for multiple hardware devices such as x86, ARM, or FPGAs (the popular choices with CSDs), and has been positioned as the unified ISA for heterogeneous computing [13,33]. Hence, we choose to use eBPF to support programmability with ZNS SSDs.

Our key contributions in this work are:

- An analysis of current CSD state of the research and practices, and making a case for Zoned Computational Storage Devices (ZCSD);
- A flexible open-source implementation of a ZCSD device in QEMU, https://github.com/Dantali0n/qemu-csd.
- An initial prototype evaluation for (i) performance of the prototype; and (ii) performance of the toolchain.

2 Current State-of-the-Art in CSD Research

To the best of our knowledge, there are no open prototypes available for CSD at this moment that let users explore design choices without significant hardware or software development efforts (see Table 1). For example, FPGA related projects [44,51] require deep FPGA expertise to design and develop applications to run inside a CSD device. Many other CPU-driven prototypes are either not openly available, or are closely integrated with a specific-application domain like databases, thus, reducing the possibility for exploration. NGD Newport [16], a enterprise-grade CSD device, offers a true general-purpose CSD design where the device run a full-fledged Linux environment on the CSD. blockNDP is the closest work to ZCSD, which uses eBPF to offer general-purpose programmability to CSD, but as of this writing it is not yet open-source1. Moreover, none of the aforementioned prototypes offer support for new SSD interfaces such as Zoned

1https://github.com/systems-nuts/blockNDP, promised to be since December 2020. One part of the code (released as of Oct 17th, 2021) "developed outside Huawei are already available, but may contain bugs and insufficient instructions".
Namespaces (ZNS) that can help to reduce the semantic gap between an application and the CSD device.

3 The ZCSD Prototype

In this section we present the design and implementation details of an open-sourced, Zoned Computation Storage Device (ZCSD). ZCSD is designed for (i) easy programmability to present users a familiar language, runtime, and toolchain; (ii) easy extensibility of the prototype to allow users to extend and define new NVMe command sets, type of code to run in CSD, and work split between the host application and ZCSD device; (iii) easy analysis to collect data about the execution of a prototype and reason about the design efficiency. ZCSD uses a NVMe Zoned SSD device in QEMU, and enhances it with an eBPF toolchain to support easy programmability and extensibility. The whole prototype is written in C/C++, thus providing a familiar user language and toolchain. ZCSD uses an Userspace eBPF VM (uBPF) [2], which allows us to JIT and run general-purpose eBPF code in ZCSD. An alternative would have been to choose the kernel eBPF infrastructure, but it is known to be restrictive in multiple ways such as restrictions on the number of instructions, absence of accesses to user data structures, and limited execution environment (access to function hooks, parameters and return codes) [20]. To support analysis, the whole prototype collects multiple performance statistics such as runtime, number of instructions executed, JITing time, amount of data movement saved, etc. that can help user to reason about their design.

The workflow life cycle: Figure 1 shows the overall steps in the process. A CSD application interacts with the ZCSD device using a user-defined ZCSD API (step 1, discussed in the next paragraph). The API allows the application to identify the data and associated eBPF program that should execute on the data. ZCSD prototype then reads the necessary data from the ZNS SSD in the userspace (step 2 and 3). Currently, we use SPDK/UIO to directly access the device using the ZNS NVMe command set, but integration with other access mechanisms such as libnvme or libzbd are also possible. After accessing the data, the user provided eBPF program is checked and JITed using uBPF (step 4 and 5) on the read data. The final result of executing the eBPF program on the data is returned to the user in the step 6. An important note here is that, in its current incarnation without any hardware offloading, ZCSD can not eliminate data movement from the storage device to the application. However, with the prototype a developer can measure the extent of the data reduction possible with and without ZCSD support, thus, making it possible to reason about viability of using CSD in their application.

ZCSD API: The ZCSD API allows developers to define (part-i) the nature of interaction with ZCSD device and application; (part-ii) what should be offloaded in ZCSD using eBPF. The two parts of the APIs are defined in the NvmCsd class (can be extended by user by C++ inheritance) and shown in listing 17. The part-i of the API (ZSCD-app) allows a user to attach an eBPF program, by including a eBPF-program ELF header at the compile time, running it synchronously (line 7), and getting results (line 8). In the future we wish to extend this to allow asynchronous execution, with a dynamic runtime compilation support as done with the Linux/BCC framework [3]. The eBPF API part (also defined and extensible by the user) allows the eBPF program to read and process data from any offset from the ZNS SSD (lines 11-14). The result of eBPF processing is returned to the user by calling bpf_return_data. The current prototype is focused on defining these extensible hooks that can be used by developers to control the nature of interaction with a ZCSD device.

Listing 1: The two parts user-extensible ZCSD API.

Listing 1: The two parts user-extensible ZCSD API.

```c
namespace qemu::nvm_csd {
public:
  NvmCsd(struct arguments::options*, struct spdk_init::ns_entry*);
  ~NvmCsd();
  // part-i of the API between app and ZCSD
  uint64_t nvm_cmd_bpf_run(void *bpf_elf,
                           uint64_t bpf_elf_size);
  void nvm_cmd_bpf_result(void *data);
  // part-2 of the API to define the eBPF interface
  static void bpf_return_data(void *data,
                             uint64_t size);
  static void bpf_read(uint64_t lba, uint64_t offset,
                      uint64_t limit, void *data);
  static uint64_t bpf_get_lba_size(void);
  static void bpf_get_mem_info(void **mem_ptr,
                            uint64_t *mem_size);
};
```
The primary goal of our current evaluation is to demonstrate that the footprint of the prototype is low and that it can yield performance gains with low software overhead. The reported numbers are the averages of 5 runs, with the whiskers showing the min and max runtimes. The key takeaway message from the graph is that our ZCSD prototype performs comparable to a native SPDK implementation in the JITed mode. As expected, the time for initialization and filling is the same in all scenarios as only the filtering is offloaded to uBPF. The execution of the filter code is different, with the ZCSD implementation without JIT (configuration #2) being the slowest due to its stack machine implementation and memory-bound checking. When used with JIT (takes 152 µseconds) the performance is within 1% of the SPDK performance. Nonetheless we are aware that a more complex application with checks and verification will add overheads to our toolchain.

5 Conclusion and On-Going Work

In this paper we made a case and presented an open-sourced computational storage device prototype with zoned namespace SSDs and eBPF language. Our evaluation on the initial prototype, ZCSD, demonstrates minimum overheads from the toolchain and implementation. While the prototype is functional and allows to experiment with CSD capabilities, we are working to expand its capabilities to: (i) integrate lightweight NVMe device access using libnvme; (ii) integrate ZCSD with a zoned-enabled file system for Flash storage like F2FS [36] to design a unified end-to-end data consistency model between an application, the file system, and a CSD; (iii) support for additional hardware backends such as ARM and FPGA, with a fast and efficient eBPF code verifiers [21]; (iv) offer built-in support for popular application-level data structures like B+-trees, hash tables, and LSM trees for data processing inside ZCSD. These efforts will further improve the support for research experiments and more complex data processing workloads on the programmable storage device. ZCSD prototype is open-sourced and publicly available at https://github.com/Dantali0n/qemu-csd.

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