High current efficiency class-AB OTA with high open loop gain and enhanced bandwidth

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Abstract: An efficient class-AB OTA with enhanced output current, slew rate, open loop gain, and gain bandwidth is presented. The circuit is based on a class-AB input stage with adaptive biasing, and an output stage with dynamically biased cascode transistors. It can deliver output currents 100 times larger than the bias current with a total quiescent power dissipation of 72 µW. Measurement results of a 180 nm CMOS test chip prototype show slew rate, gain bandwidth, and open loop gain enhancement.

Keywords: Class-AB, OTA, current efficiency

Classification: Integrated circuits

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1 Introduction

Fig. 1 shows the scheme of conventional current mirror class-A OTA. It has an open loop gain $A_{OL}$=$A_i^2/2$, where $A_i$ is the transistor’s intrinsic gain. Its maximum positive and negative output currents ($I_{out\text{MAX}}$) are limited by the total quiescent current ($I_Q$) to a value $I_{out\text{MAX}}=0.5I_Q$. Class-AB OTAs [1]-[11] overcome this limitation and generate $I_{out\text{MAX}}>I_Q$. Super class-AB schemes [4] and [6] have remarkably large output Current Enhancement (CE two decades or higher) factors $I_{out\text{MAX}}=CE\cdot I_Q$, while suffering from low open loop gain ($A_{OL}$=$A_i/2$) which is of special concern in deep sub-micron technologies characterized by low $A_i$ values ($A_i<20$ V/V). On the other hand, class-AB OTAs with high open loop gain have only modest output current enhancement factors, i.e. in [7] and [8] $I_{out\text{MAX}}=2.24I_Q$, and $I_{out\text{MAX}}=5.55I_Q$ respectively. In this letter, we discuss the implementation and experimental verification of a class-AB OTA that has simultaneously very high current enhancement factor and even higher open loop gain and bandwidth than the conventional class-A OTA of Fig. 1.

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2 Proposed scheme
The proposed class-AB OTA is shown in Fig. 2. It has a class-AB input stage [12] implemented with Cascoded Flipped Voltage Followers (CFVF s shown in blue color) [13] with an adaptive biased load (Mp, Mcp) [6] and an adaptive biased tail transistor (Mnt’, Mcnt). The class-AB differential pair generates transient currents $i_1, i_2$ with peak values much higher than $I_{bias}$.
The utilization of adaptive biasing in the load \((V_{cp})\) and tail transistors \((V_{cn})\) causes magnified replicas \(i_1', i_2'\) of \(i_1, i_2\) to appear in the output branch. This leads to an output current that can be much larger than \(I_{bias}\).

In [4] and [6] cascode transistors in the output branches could not be used to achieve high open loop gain because the increasing gate-source voltage \((V_{GS})\) with very large currents causes output branch mirroring transistors to enter triode mode which limits the output current. In order to mitigate this problem, in the proposed circuit, cascode voltages \(V_{cp}', V_{cn}'\) adapt dynamically to the output current. This is achieved using large time constant \(RC\) networks formed by \(C_{bat} (~pF)\) and a large resistance \(R_{large} (~100,000 \Omega)\). Under quiescent conditions the PMOS and NMOS cascode voltages have values \(V_{cp} = V_{cp}'\) and \(V_{cn} = V_{cn}'\). For large dynamic currents, variations \(\Delta V_X, \Delta V_Y\) in nodes \(X, Y\) are transferred to \(V_{cn}'\) and \(V_{cp}'\) respectively. This provides more headroom for the drain-source voltage \(M_{no}\) and \(M_{po}\) and allows simultaneously large output currents and high open loop gain.

3 Measurement results

A test chip with the proposed circuit and a conventional current mirror class-A OTA were fabricated in 0.18 µm CMOS technology (Fig. 3). The proposed circuits occupied 0.15 m × 0.046 m (0.007 mm²) of silicon. The sizes (in µm) of unit NMOS and PMOS transistors were \((W/L)_N=(4/0.7)\) and \((W/L)_P=(16/0.7)\) respectively. Values \(R_{large}=100 \Omega\), \(C_{bat}=1 \mu F\), \(C_L=25 \mu F\), \(V_{DD}=0.9 \text{ V}\), \(V_{SS}=-0.9 \text{ V}\), and a bias current \(I_{bias}=5 \mu A\) were used for testing purposes.

![Fig. 3.](image)

![Micrograph of a test chip including the proposed circuit fabricated in 0.18 µm CMOS technology occupying 0.007 mm² of silicon.](image)

The experimental output waveforms of the proposed and the conventional class-A OTA connected in unity gain configuration are shown in Fig. 4. The input is a 1 MHz square wave with amplitude of 0.8 Vpp. The proposed scheme has an experimental \(SR=43.1 \text{ V/µs}\), \(GB=2.65 \text{ MHz}\), and \(A_{OL}=77 \text{ dB}\) while the conventional class-A scheme has \(SR=0.44 \text{ V/µs}\), \(GB=1 \text{ MHz}\), and \(A_{OL}=71 \text{ dB}\). It can be seen that: a) the \(SR\) is improved by a factor 100 and b) the open loop gain
and bandwidth of the proposed circuit have values approximately twice as large as the conventional class-A OTA with equal $I_{\text{bias}}$.

![Fig. 4](image)

**Fig. 4.** Experimental results: (a) 1 MHz 0.8 $V_{\text{pp}}$ square wave input signal. (b) Proposed Class-AB OTA output waveform. (c) Conventional class-A OTA output waveform.

The $GB$, $A_{OL}$ enhancement is expected from the utilization of the class-AB input stage [4] and [6]. The performance of class-AB circuits can be compared using the current enhancement figure of merit $FOM_{CE} = \frac{SR \cdot C_L}{P_Q}$ where $P_Q$ is the total quiescent power dissipation. It can be seen that the proposed circuit has a higher $FOM_{CE}$ than all OTAs with high open loop gain and high phase margin (~90°) reported in literature. The performance comparison between experimental results of the proposed OTA and some other references is summarized in Table I.

**Table I.** The performance comparison between experimental results of the proposed OTA and some other references.

| Parameters          | Class-A OTA | Fig. 1 | [4] 2005 | [9] 2013 | [7] 2016 | [8] 2015 | This work | Fig. 2 |
|---------------------|-------------|--------|---------|---------|---------|---------|-----------|--------|
| CMOS Technology ($\mu$m) | 0.18        | 0.5    | 0.18    | 0.18    | 0.5     |         | 0.18      |        |
| Results*            | Ex          | Ex     | Sim     | Ex      | Ex      | Ex      | Ex        |        |
| Supply (V)          | 1.8         | 2      | 3       | 1.8     | 5       |         | 1.8       | 1.8    |
| $I_{\text{bias}}$ (µA) | 5           | 10     | -       | -       | 25      | 5       | 5         | 5      |
| Power (µW)          | 36          | 120    | 750     | 11900   | 612.5   |         | 72        | 72     |
| SR (V/µs)           | 0.44        | 89     | 7.43    | 74.1    | 23.2    | 43.1    |           | 43.1   |
| $FOM_{CE}$ [V/µs]-[pF/µW] | 0.3  | 59.33  | 0.3     | 1.25    | 0.76    | 15      |           | 15     |
| $A_{OLDC}$ (dB)     | 71          | 43     | 64.1    | 72      | 71.8    | 77      |           | 77     |
| $C_L$ (pF)          | 25          | 80     | 30      | 200     | 20      | 25      |           | 25     |
| GB (MHz)            | 1           | 0.725  | 7.64    | 86.5    | 6.3     | 2.65    |           | 2.65   |
| PM (°)              | 89          | 89.5   | 83      | 50      | 82      | 86      |           | 86     |
| Die Area (mm²)      | 0.001       | 0.024  | -       | 0.07    | -       | 0.007   |           |        |

* Ex: Experimental results, Sim: Simulation results
6 Conclusion

An implementation of a class-AB OTA using a class-AB input stage with CFVFs, and dynamically biased cascode transistors is presented. Compared to the conventional OTA, the proposed scheme shows a very large enhancement factor of 100 in both $SR$ and $I_{\text{outMAX}}$ without degradation in the open loop gain $A_{OL}=77$ dB. Both $A_{OL}$ and $GB$ are approximately a factor two higher than for a conventional current mirror OTA. A fabricated chip in 0.18 µm CMOS technology is used to verify experimentally theoretical predictions.