Mixed-precision training of deep neural networks using computational memory

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Deep neural networks have revolutionized the field of machine learning by providing unprecedented human-like performance in solving many real-world problems such as image and speech recognition. Training of large DNNs, however, is a computationally intensive task, and this necessitates the development of novel computing architectures targeting this application. A computational memory unit where resistive memory devices are organized in crossbar arrays can be used to locally store the synaptic weights in their conductance states. The expensive multiply accumulate operations can be performed in place using Kirchhoff’s circuit laws in a non-von Neumann manner. However, a key challenge remains the inability to alter the conductance states of the devices in a reliable manner during the weight update process. We propose a mixed-precision architecture that combines a computational memory unit storing the synaptic weights with a digital processing unit and an additional memory unit accumulating weight updates in high precision. The new architecture delivers classification accuracies comparable to those of floating-point implementations without being constrained by challenges associated with the non-ideal weight update characteristics of emerging resistive memories. A two layer neural network in which the computational memory unit is realized using non-linear stochastic models of phase-change memory devices achieves a test accuracy of 97.40% on the MNIST handwritten digit classification problem.

I. INTRODUCTION

Deep neural networks (DNN) including multilayer perceptrons, convolutional neural networks, deep belief networks, and Long-Short-Term-Memories are loosely inspired by biological neural networks in which parallel processing units named neurons are interconnected by plastic synapses. By tuning the weights of the interconnections these networks are able to solve problems which are intractable by conventional algorithms. Through a combination of factors, such as the availability of massive labeled datasets and the highly parallel matrix manipulations offered by modern GPUs, these networks have recently achieved considerable success in numerous applications.¹

A DNN comprises multiple layers of neurons interconnected by synapses. Training of DNNs refers to the process of finding appropriate synaptic weights such that after the training process, the network is able to perform various classification tasks with sufficient accuracy. Typically, this is achieved by a supervised training algorithm known as backpropagation. During the training phase, the input data is forward-propagated through the neuron layers with the synaptic network performing a multiply-accumulate operation. The final layer responses are compared with input data labels and the errors are back-propagated. All the synaptic weights are updated to reduce the error. This forward-backward data propagations and weight updates are repeated several times over the entire training data set. This brute force approach to training neural networks is computationally intense and, in spite of the availability of computing resources such as the GPUs, is very time-consuming. Also, the high power consumption of this training approach makes its application prohibitive in several emerging domains such as internet of things and edge computing. Much of the inefficiency arises from the fact that the DNNs are trained using conventional von Neumann computing systems where the physical separation between the memory and processing units leads to constant shuttling of data back-and-forth between them.

Recently, there is a significant interest in designing non-von Neumann co-processors for training DNNs. A system comprising dense crossbar arrays of resistive memory devices has been proposed to perform the various steps involved in training of DNN.² The devices, also referred to as memristive devices, store information in their conductance state and can be used to represent the synaptic weights. The matrix-vector multiplications needed during the propagation of data in the network can then be computed as a result of Kirchhoff’s circuit laws. Weight updates can be applied by modifying the conductance levels of the resistive memory devices by applying appropriate electrical pulses. However, this approach can achieve satisfactory training accuracy only with ideal, not-yet-available resistive memory devices. The experimental demonstrations based on existing resistive memory devices have achieved reduced classification accuracies owing to the inability to achieve precise conductance changes in the memristive devices.³

A related research area that is gaining a lot of traction is in-memory computing or computational memory. Here, physical attributes of the memory devices are exploited to perform computations in a non-von Neumann manner. There are recent demonstrations of performing bulk bit-wise operations,⁴ matrix-vector multiplications,⁵ and finding temporal correlations using such a memory unit.⁶ One major issue in
this field is the limited precision of the individual units of the computational memory. Recently, we proposed the concept of mixed-precision in-memory computing to counter this challenge. The essential idea here is to use the low-precision computational memory unit in conjunction with a precise computing unit. The benefits of area/energy/speed improvements arising from computational memory are retained while addressing the key challenge of inexactness associated with computational memory. As an example, we presented an iterative solver for systems of linear equations.

Meanwhile, there are some key developments taking place at the algorithmic front with respect to training DNNs using digital arithmetic with reduced precision. Recent work shows that it is possible to have binary precision for the weights used in the multiply-accumulate operations (during the forward and backward propagations) as long as the precision of the stored weights in which gradients are accumulated is retained. This indicates the possibility of accelerating the DNN training using programable low precision computational memory, provided we address the challenge of reliably transferring the high precision gradient to them.

In this article, we present a mixed-precision architecture based on computational memory to train DNNs. We investigate various undesirable attributes of the constituent devices in such a computational memory unit and show how the proposed architecture is designed to cope with them. Finally, the DNN training performance of the mixed-precision scheme is evaluated where computational memory devices are realized using stochastic models based on 90nm phase-change memory characterization.

II. COMPUTATIONAL MEMORY: THE KEY CHALLENGES

Non-volatile resistive memory devices have several attributes making them suitable candidates for building computational memory elements. These devices operate based on a variety of physical mechanisms such as field driven atomic rearrangement (metal-oxide based resistive memory (ReRAM)), conductive bridge memory (CBRAM), spintronic effects (spin transfer torque based magnetic memory (STT-MRAM)) and phase transition (phase-change memory (PCM)). Irrespective of the underlying physical mechanism, all these devices store information in their resistance or conductance states which are programmed by the application of suitable electrical pulses. However, there are many challenges associated with programming a desired conductance change in these devices. First, there are limitations on the minimum conductance change that can be reliably induced. For example in STT-MRAM, it is very difficult to achieve more than two conductance levels due to the underlying physical mechanism. Similarly in filamentary resistive memory devices such as CBRAM, the positive feedback mechanism involved in the filament growth process makes it difficult to control the process and to achieve intermediate states. This inability to achieve a sufficiently small conductance change also limits the storage resolution. Another major challenge arises from stochasticity associated with the device programing. In these nanoscale devices, slight changes in atomic configurations can lead to significantly different conductance values. Asymmetry in the conductance change, i.e., the average increment (potentiation) and decrement (depression) in conductance that can be reliably realized in a device is also an important challenge. Some devices also show significant state dependence where the conductance update depends on the current state of the device. For instance, this makes potentiation progressively harder with increasing conductance values. We refer to this as non-linear conductance response. In addition to weight update challenges, random volatile conductance fluctuations in the constituent elements of the computational memory and the finite resolution of the data converters used to interface them with the processing units could significantly impact the accuracy of the computations performed.

In Fig. 1 we introduce the mixed-precision computational memory approach for training DNNs. The most expensive operation during the forward and backward propagation is determining the weighted sum, which are matrix-vector multiplications. A computational memory unit which has resistive memory devices organized in a crossbar array is ideally suited to perform these matrix-vector operations with constant computational time complexity. The neuron activations of a layer, $x_i$, are applied as voltages to the word lines using digital-to-
Mixed-precision architecture based on computational memory: The synaptic weights are stored in a computational memory unit as conductance states of resistive memory devices organized in crossbar arrays. The matrix-vector multiplications associated with the forward and the backward propagation are performed in place in the memory arrays. The weight updates are accumulated in a volatile memory, χ, in high precision until they become comparable to the update granularity (ε) of the memory devices. The device updates are integer multiples of ε and the same quantity will be subtracted from χ.

The desired weight updates are determined as the product of the back-propagated error and the neuron activation, \( ΔW_{ji} = η \delta_j x_i \), where η is the learning rate. Even though the computational memory unit can accelerate the forward and the backward propagation significantly, updating the synaptic weights with the desired precision is very challenging. Often, the devices representing the synaptic weights have a conductance update granularity dictated by the physical mechanism behind it. Let ε be the absolute value of the smallest conductance change that can be reliably achieved. Attempts to program weight updates which are much smaller could induce significant error in the training. In the proposed approach, the weight updates are accumulated in high precision in a variable χ. The device conductance will be updated only if the magnitude of the accumulated weight update becomes greater than or equal to an integer multiple of ε. The number of programming pulses, p, to be applied to the resistive memory device is determined by flooring \( χ/ε \) toward zero, and the same number of εs is subtracted from the χ. Depending on the sign of p, the conductance value of the corresponding device will be increased or decreased. Note that, the actual conductance state of the devices are never read back, and hence we will never be able to confirm whether the requested weight updates are accurately attained as equivalent conductance changes in the devices. In spite of this, we show that this scheme works remarkably well and that the performance is often comparable to those of floating-point implementations. This single-shot programming method, which avoids verification and iterative programming steps, enables the acceleration of the training process. In subsequent sections, we will present a detailed evaluation of this methodology under various scenarios of device-level non-ideal behavior.

IV. EVALUATION OF THE MIXED-PRECISION ARCHITECTURE

A. The simulation framework

![Diagram of the mixed-precision architecture](image)

FIG. 2. Neural network for digit classification: The neural network used to evaluate the mixed-precision architecture. The objective is handwritten digit classification based on the MNIST data set. There are 784 input neurons, 250 hidden sigmoid neurons, and 10 output sigmoid neurons. The network weights are trained by optimizing a quadratic objective function using gradient descent. All the 60,000 images in the dataset are used in one epoch of training and 10,000 images for testing.

The performance of the mixed-precision architecture is analyzed based on its classification accuracy on the MNIST handwritten digit dataset using a neural network as shown schematically in Fig. 2. The number of neurons in the input, the hidden and the output layer is 784, 250, and 10 respectively. The hidden and output neurons are sigmoid. The network is trained using the entire training set of 60,000 images for ten epochs, and a test accuracy is reported based on 10,000 test images. The pixel values of the 28 × 28 gray-scale images are normalized between 0 and 1 before they are supplied as input to the network. No other preprocessing is performed on the
images. We used the quadratic objective function for the backpropagation-based training and used a fixed learning rate. The network gave 98% floating point (64-bit) test accuracy when trained using stochastic gradient descent. This classification result is used as reference to evaluate the performance of our mixed-precision approach. The final weight distribution from this high-precision training was approximately in the range [-1 1].

B. Inaccuracies arising from weight-updates

In this section, we will evaluate how the proposed architecture copes with the issues associated with weight updates. We assume a hypothetical linear device with a conductance range of [-1 1] similar to the floating-point trained weight distribution. The device is assumed to have \( n \)-bit update granularity such that it covers its conductance range in \( 2^n - 2 \) steps and hence it will have \( 2^n - 1 \) possible levels in the absence of conductance change stochasticity. An odd number of levels was chosen to include zero. Therefore, in our mixed-precision training approach, we will update the device when the weight-update accumulation exceed the conductance change step size, \( \varepsilon = 2 / (2^n - 2) \). In subsequent discussions, we will use both \( \varepsilon \) and \( n \) interchangeably to indicate the granularity associated with the weight-updates.

The conductance updates in the non-volatile devices are often stochastic. Even though it is desirable to induce a change in conductance corresponding to an integer multiple of \( \varepsilon \), the observed change is often quite different from the desired one. Therefore, the actual weight update from the device, denoted by \( \Delta W \), is modeled as a Gaussian random variable whose mean is \( \varepsilon \) and whose standard deviation (\( \sigma \)) is a fractional multiple of \( \varepsilon \). This device model is used as the computational memory elements representing the neural network synapses during its training using the mixed precision scheme. The devices are initialized to \{-1, 0, 1\} states with a discrete distribution whose variance is normalized by the number of neurons in the pre- and post-synaptic layers. Device read noise and analog-digital converters are ignored at this stage. The simulated classification accuracies with limited granularity and with different amounts of stochasticity in the updates is shown in Fig. 3. In the case where the weight updates are non-stochastic the test accuracy drop is only 1% for 2-bit, and with 3-bit granularity the accuracy is very close to that obtained in the floating-point simulation (reference). As the stochasticity increases, the performance degrades with reducing number of bits. However, it is remarkable that even though the standard deviation of the weight update is equal to or greater than the mean weight update granularity itself, drop in the test accuracy is still within approximately 4% for 2-bit granularity. The test accuracy becomes closer to the reference floating-point

![FIG. 3. Effect of granularity and stochasticity associated with weight-updates](image)

Linear devices with symmetric potentiation and depression granularity are assumed as computational memory elements. The standard deviation of the weight-update randomness, \( \sigma(\Delta W) \), is taken as a multiple of the weight-update granularity, \( \varepsilon \). The error-bars indicate the standard deviation corresponding to five repetitions of the simulation. It can be seen that even in the extreme cases of highly coarse and random weight-updates, drop in the test accuracy is still within approximately 4% for 2-bit granularity.

![FIG. 4. Discrete weight solutions](image)

(a) Initial weight distribution

(b) 2-bit update granularity (\( \sigma(\Delta W)=0 \))

(c) 3-bit update granularity (\( \sigma(\Delta W)=0 \))

FIG. 4. Discrete weight solutions: (a) In the linear device simulations, the weights are initialized to a set of states -1, 0, and 1. (b) In non-stochastic two bit granular updates the devices go through only these discrete states and hence the update granularity also becomes the device resolution. This discrete weight solution gave a test accuracy of approximately 97%. However, in case of stochastic programming, the devices can achieve intermediate states. (c) The final weight distribution from the 3-bit update granularity simulation is also shown. The higher weight resolution improved the test accuracy by approximately 1%.
accuracy as the device granularity is further reduced.

The distributions of the initial and trained weights in the two layers of the neural network for the 2-bit and 3-bit update granularity are shown in Fig. 4. The distributions are shown for non-stochastic device programming and hence the final weights are also discrete and the number of levels correspond to the update granularity. We observe that increasing the number of levels improved the classification performance until an update granularity of 4-bit beyond which the test accuracies remained approximately constant. The stochasticity associated with conductance updates helps to create a non-discrete weight distribution. However, we found this to have no significant advantage and we typically observe a decrease in the classification performance with increasing stochasticity (Fig. 5).

From the previous discussion, it can be seen that increasing the resolution of conductance change beyond a certain value does not necessarily improve the network performance. Moreover, in the mixed precision scheme, there is a significant reduction in the device programming cost with the use of larger $\epsilon$s. In Fig. 5, we show the number of device updates during each epoch of training. The maximum number of device updates, calculated as the product of the synapse count and the training image count, assuming all the weights are updated after each image presentation, is indicated as reference. However, in the mixed precision approach, we accumulate the updates in high precision. As a result, the smaller updates are combined and delivered together to the device. Hence, as the device update granularity ($\epsilon$) increases, the devices need to be programmed less often, resulting in eventual energy savings. Programming resistive memory devices incurs significant time and power penalty and hence it is desirable to reduce the number of such programming instances, without compromising the network performance. For the chosen network architecture and classification problem, 4-bit update granularity seems to offer the best case scenario of highest test accuracy with reduced programming expense.

Next, we study the influence of asymmetric conductance update response. We assume a device with fixed but unequal potentiation and depression granularity. The mixed-precision method can cope with this behavior by using different thresholds, $\epsilon_P$ for conductance increment and $\epsilon_D$ for conductance decrement. For example, in Fig. 6 we assume an 8-bit potentiation granularity and 6-bit depression granularity is varied. The one bit depression in the figure correspond to a situation where the update granularity, $\epsilon_D$, equals the entire weight range in contrast to the previous definition. The weight updates are assumed to be deterministic. The resulting test accuracies show less than 1% drop even for the maximum asymmetric case tested, demonstrating the efficacy of the proposed scheme to tolerate device update asymmetry effectively.

Subsequently, we investigate the influence of non-linear conductance response. To analyze this, we simulated the training problem using a device model whose non-linearity could be tuned. We chose an exponential function to model the potentiation and depression granularity. The mixed-precision method can cope with this behavior by using different thresholds, $\epsilon_P$ for conductance increment and $\epsilon_D$ for conductance decrement. For example, in Fig. 6 we assume an 8-bit potentiation granularity and 6-bit depression granularity is varied. The one bit depression in the figure correspond to a situation where the update granularity, $\epsilon_D$, equals the entire weight range in contrast to the previous definition. The weight updates are assumed to be deterministic. The resulting test accuracies show less than 1% drop even for the maximum asymmetric case tested, demonstrating the efficacy of the proposed scheme to tolerate device update asymmetry effectively.

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\[
\Delta \tilde{W}_P = \alpha e^{-\beta \frac{W - W_{\min}}{W_{\max} - W_{\min}}} \\
\Delta \tilde{W}_D = \alpha e^{-\beta \frac{W_{\max} - W}{W_{\max} - W_{\min}}}
\]

Here, $\Delta \tilde{W}_P$ and $\Delta \tilde{W}_D$ model the potentiation and depression respectively for a device at a conductance of $W$. $W_{\min}$ and $W_{\max}$ represent the limits of the device conductance. We used the parameter $\beta$ to tune the amount of non-linearity and $\alpha$ to adjust the update granularity. To make a reasonable comparison in training performance using models of different amount of non-linearity, we assume that two criteria have to be satisfied: the device models must have the same on-off ratio and
FIG. 7. Effect of non-linear conductance response: (a) Non-linear device model: the weight update ($\Delta W$) is modeled as exponentially dependent on the current state, $W$. The exponential function for different amount of non-linearity is plotted. (b) Corresponding device model pulse response, where 14 potentiation pulses followed by the same number of depression pulses are applied to the device. (c) Non-linear device model as synapse for DNN training. $\beta = 0$ corresponds to a symmetric linear device and higher $\beta$ values indicate increasing amount of non-linearity. Approximately 4-bit weight update granularity is assumed for the device model and mixed precision training. Weight updates were non-stochastic. The result shows that there is no significant degradation in the test accuracy even for $\beta = 5$ that corresponds to a highly non-linear conductance response.

they must take the same number of programming steps to span the whole conductance range, irrespective of the non-linearity. The $\Delta W$ versus $W$, and $W$ versus pulse number responses satisfying these conditions for different values of $\beta$ are shown in (a) and (b). Here, $\beta = 0$ correspond to a linear device. The number of pulses for full range potentiation or depression is assumed to be corresponding to that of a 4-bit update granularity. The same update granularity is assumed to determine the $\varepsilon$ for the mixed precision scheme for varying amount of non-linearity. The resulting test accuracies are plotted as a function of $\beta$ in Fig. 7(c). It can be seen that there is no significant degradation in the test accuracy even for $\beta = 5$, which is very close to the behavior of a binary device.

C. Inaccuracies arising from matrix-vector multiplication

In this section, we analyze the influence of conductance fluctuations and finite resolution of data converters. Resistive memory devices typically exhibit fluctuations in conductance arising from trapping/detrapping processes. The effect of this read noise in the DNN training using the proposed scheme is tested by adding a zero mean white Gaussian noise to a linear device model. The noise is added to the weights whenever it is used in the matrix multiplication in the forward and the backward propagation. It is also incorporated during the testing phase (only forward propagation). The standard deviation of the noise is varied as a fraction of the total weight range. The resulting test accuracies are shown in Fig. 8a. It can be seen that the methodology is quite robust to up to 5% read noise.

An additional source of error in the matrix-vector multiplication is due to quantization from the DACs and ADCs. During forward propagation, the neuron activations evaluated in the digital domain are converted to analog voltages using DACs before they are applied to the word lines of the crossbar array. The weighted sum obtained as currents in the bit lines are read back using ADCs. Similarly, the back-propagated errors are converted to analog voltages when applied to the cross-bar array matrices. The range for the digital to analog converters are fixed for sigmoid and tanh neuron activations, whereas for the ReLu neurons this could be a challenge as
their range dependents on the data and weight distribution. Here, we chose sigmoid neurons for our network, which fixed the DAC range in the forward propagation. Furthermore, we normalized the back-propagated errors to fix the range for its interface converters to analog voltages. The normalization factor is multiplied with the learning rate during the weight update calculation. However, the input for the analog to digital converters is results from matrix-vector multiplications and their distribution is dependent on the number of neurons and the weight distribution in the layer. In this work, the range for ADC was determined by observing the distribution of corresponding variables representing the weighted sums. To study the effect of DACs and ADCs separately, the bit precision of one of them is varied, whereas the other variables are represented in floating-point precision. Fig. 8 shows that 8-bit resolution is sufficient to avoid a noticeable degradation in test accuracy.

D. Phase-change memory synapses

Phase-change memory is a relatively mature resistive memory technology that has found applications in the space of storage-class memory and novel computing paradigms such as neuromorphic computing and computational memory. It is based on the property of chalcogenide alloys, typically compounds of Ge, Sb and Te, which exhibit drastically different electrical resistivity depending on whether they are in the ordered crystalline phase or in the disordered amorphous phase. The crystalline phase of the Ge$_2$Sb$_2$Te$_5$ (GST) alloy is orders of magnitude more conductive than the amorphous phase. If this material is sandwiched between two metal electrodes, the phase-configuration of the material and thus the conductance of the device can be reversibly changed by applying suitable electrical pulses. The crystalline to amorphous phase transition is accomplished by a melt-quench process and the reverse transition is governed by temperature accelerated nucleation and crystal growth. It is possible to achieve a continuum of conductance values by partial crystallization or amorphization in these devices. This analog storage capability makes PCM particularly suited for applications in the space of computational memory.

The PCM devices exhibit most of the non-idealities we described earlier, such as limited granularity, non-linear and asymmetric conductance update, and programming stochasticity. There is also substantial read noise associated with these devices. To evaluate the suitability of PCM devices for the mixed-precision approach to train DNNs, we developed a model that captures the essential physical attributes of PCM devices. The model is created based on characterization data from approximately 10,000 devices integrated in 90nm CMOS technology. The devices are subjected to 20 programming pulses of fixed amplitude and each state is read 50 times to eliminate read noise. The mean and standard deviation of the extracted conductance change ($\Delta G$) versus the average initial conductance for each programming pulse are fitted using piece-wise linear models as shown in the Fig. 9a, b. Assuming the $\Delta G$ to be a Gaussian random variable, the device cumulative pulse response is simulated, and the statistical plot of the resulting stochastic model behavior is plotted in Fig. 9c.

This device model was used to emulate the synapses in the crossbar array to study its influence on training DNNs. Two PCM devices in differential configuration with weight refresh are used. The conductance values are initialized to a normal distribution around 2$\mu$A whose standard deviation is normalized based on the number of neurons in the pre- and post-synaptic layers. Resulting test accuracy after 10 epochs of training was 97.78% (Fig. 9d). Incorporating a fixed read noise (zero mean Gaussian noise with experimentally measured average standard deviation) and 8-bit analog-digital converters during training and testing resulted in an additional 0.38% drop in accuracy. We also tested the training performance where each synapse is realized using a single PCM device model at the crosspoint, exploiting the capability of the scheme to cope with the strongly asymmetric conductance response. The final test accuracy for the MNIST dataset classification was 96.5%, indicating the robustness of our scheme.

V. DISCUSSION

The non-volatile memory crossbar array based computational memory unit is ideally suited to perform matrix-vector
multiplications. By utilizing the computational memory to perform those operations when training DNNs, the forward and the backward propagation of data can be significantly accelerated. Also, the processor-memory bottleneck is reduced as the synaptic weights are not transferred during the propagations. However, the necessity to frequently update the memory devices poses an additional challenge compared to applications of computational memory where the matrix does not change. In back-propagation based training algorithm it is desirable to update the weight matrix after the presentation of each training instances. Using devices like PCM, which can attain a continuum of conductance states, it is possible to iteratively program the devices to the desired conductance states accurately. However, this involves repeated read/write cycles and incur significant time/power penalty. The necessity to program a large number of devices very often could overshadow the performance gain that we obtain from the in-place matrix-vector multiplication in the crossbar array.

On the other end of the spectrum lies the non-von Neumann coprocessor approach proposed recently. As before, the synaptic weights are stored in resistive memory devices organized in crossbar arrays and the matrix-vector multiplications during forward and backward propagation are realized in place using these arrays. However, they suggest a fully parallel conductance update by overlapping pulses from the pre- and post-synaptic neuron layers. By realizing the neurons and associated circuits in place, this offers the possibility of a fully parallel non-von Neumann system. By accelerating all the three components of training DNNs, namely forward propagation, backward propagation, and weight update, this approach could be the fastest and most energy-efficient compared to alternate approaches. However, the non-idealities associated with programming the memory devices will pose significant challenges in realizing state-of the art classification accuracies. An ideal device is expected to have a symmetric weight update granularity of 10 bits. Experimental demonstrations using more realistic phase change memory devices have shown a limited test accuracy of less than 83%.

Our mixed precision approach is designed to take into account the limited device update granularity seen in experimental devices today. The proposed architecture is significantly tolerant to conductance programming asymmetry and update non-linearity. In contrast to the above discussed methods, we deliver the conductance updates only when weight updates accumulated in high precision become comparable to the device update size. As a result, the number of device programming instances are reduced by several orders of magnitude as the update size increases. As a result, the advantage of matrix-vector multiplication acceleration in the data propagation stages is preserved without significant device programming overhead. We follow a blind single pulse programming approach without read-back to deliver an \( \epsilon \) amount of update. The value of \( \epsilon \) is chosen based on the device dynamics. The simulations show that the resulting sparse weight updates training are able to achieve classification accuracies comparable to those from the floating-point simulations in similar number of training epochs. Further, the high precision accumulation and less frequent weight-updates combined with the inherent error tolerance of neural network training enable the architecture to cope with the high device programming stochasticity.

We believe that the weight update and accumulation overhead associated with this mixed precision architecture is significantly less compared to the training acceleration we obtain. The training acceleration is achieved by computing the multiply-accumulate operation of approximately \( O(N^2) \) complexity in fixed time for each \( N \times N \) neural network layer. The device updates are sparse and the weight update accumulation in high precision is equivalent to the weight update scheme in standard stochastic gradient decent except that the memory is initialized to zero here. The additional thresholding/flooring and subtraction operations are computationally simple and do not incur additional memory read/write operations as they can be preformed concurrently with the weight-update accumulation. Still, it is desirable to further accelerate the weight update stage of DNN training as the weight-update determination is an \( O(N^2) \) operation.

VI. CONCLUSION

In this work, we presented a mixed precision computing architecture to train deep neural networks. The essential idea is to use a computational memory unit in conjunction with a high precision processing unit. The computational memory unit comprises of resistive memory devices that are organized in a crossbar array. The synaptic weights are stored as conductance states of these memory devices. The computational-expensive matrix-vector multiplications arising during the forward and backward propagation stages of the backpropagation algorithm can be realized in a highly efficient manner using this computational memory unit. However, the weight updates are accumulated in high precision and are only sporadically transferred to the device array. This mixed-precision approach is shown to overcome the non-ideal behavior related to resistive memory devices such as limited granularity and stochasticity associated with their programming as well as asymmetric and non-linear conductance response. In spite of the added complexity arising from the high precision unit, we still gain in overall performance due to the substantial gain in time/power efficiency associated with the forward and backward propagation steps. Moreover, the weight updates are sparse enough to not incur a significant time/power penalty arising from the need to program the memory devices. This approach was tested using the MNIST handwritten digit classification problem and is shown to achieve remarkably high classification accuracies even with computational memory units comprising single phase-change memory devices. Realistic models of PCM devices fabricated in 90nm technology node were used for this evaluation.

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