Edge-Contact MoS$_2$ Transistors Fabricated Using Thermal Scanning Probe Lithography

Ana Conde-Rubio,* Xia Liu, Giovanni Boero, and Jürgen Brugger

ABSTRACT: The science and engineering of two-dimensional materials (2DMs), in particular, of 2D semiconductors, is advancing at a thriving pace. It is well known that these delicate few-atoms thick materials can be damaged during the processing toward their integration into final devices. Thermal scanning probe lithography (t-SPL) is a gentle alternative to the typically used electron beam lithography to fabricate these devices avoiding the use of electrons, which are well known to deteriorate the 2DMs’ properties. Here, t-SPL is used for the fabrication of MoS$_2$-based field effect transistors (FETs). In particular, the use of t-SPL is demonstrated for the first time for the fabrication of edge-contact MoS$_2$ FETs, combining the hot-tip patterning and Ar$^+$ milling to etch the 2DM. To avoid contamination of the contact interface by atmospheric gas molecules, etching and metal deposition are performed without breaking the vacuum conditions in between. With this process, edge-contact MoS$_2$ FETs are successfully fabricated and characterized. On/off ratios up to 10$^8$ and 10$^9$ are obtained at room temperature in air and vacuum, respectively, i.e., comparable with the best values reported in the literature.

KEYWORDS: 2D materials, TMDCs, MoS$_2$, FET, edge contact, lithography, thermal scanning probe

INTRODUCTION

Two-dimensional materials (2DMs) have emerged as potential candidates for future electronic and optoelectronic devices. Not only their ultrathin nature but also the possibility of tuning their properties by, for example, modifying the dimensionality$^{1,2}$ or by applying strain,$^{3,4}$ have put 2DMs in the spotlight. As compared to silicon technologies, transition metal dichalcogenides (TMDCs) overcome short-channel effects even in multilayered devices$^5$ which makes them good candidates for miniaturization of low-power electronics. However, 2DMs are also extremely delicate, and their properties can be significantly affected by chemical and physical fabrication processes. Conventional lithography methods like UV photolithography and electron beam lithography (EBL) have been shown to produce detrimental effects in 2DM devices.$^6,7$ In particular, it has been reported that UV radiation can affect the interface between graphene and SiO$_2$, induce hysteresis in the electronic characteristics, and reduce the charge carriers’ mobility.$^7$ Electron and ion radiation can result in local band-gap modification, nanoscale domain formation, and vacancy creation.$^5,8$ The exposure to ion beams, even for short times at relatively low energies, can cause serious alterations to 2DMs that are reflected as a decreased photoluminescence.$^8$ Besides, it has been reported that both PMMA and photoresist leave residues that also deteriorate the device performance.$^9,10$ It is clear that this effect is more relevant in the case of top-contact devices. However, when EBL is used, the incoming electrons interact along their path, resulting in forward scattering and secondary electrons. This results in an interaction volume that goes beyond the desired aperture, causing the well-known proximity effects of EBL. For the same reason, the scattered electrons and secondary electrons generated could affect the 2DM located close to the patterned areas (with an extension of a few nanometers). Hence, for miniaturized devices, not only the contacts but also a significant part of the channel could be affected.

Another recurring challenge in the fabrication of 2DM devices is their contact to metals. The characteristic Schottky barrier appearing at the junction between 2DMs and metallic contacts remains a limiting factor in the performance of 2DM-based electronic devices.$^{11,12}$ There are two main configurations to contact metallic electrodes to 2DMs (Figure 1a): top contact, in which the metal is deposited on top of the 2DM uppermost layer (basal plane), and edge contact, when the metal contacts every layer of the 2DM through the side (edge plane). When 2DMs are exposed to air, molecules such as

Received: June 7, 2022
Accepted: August 16, 2022
Published: September 7, 2022

https://doi.org/10.1021/acsami.2c10150
ACS Appl. Mater. Interfaces 2022, 14, 42328−42336

© 2022 The Authors. Published by American Chemical Society
water or hydrocarbons adhere to the surface, forming layers with a thickness that can be of the same order of the 2DM itself. As a consequence, in the case of top-contact devices, these molecules directly affect the 2D semiconductor−metal interface and could result in Fermi level pinning and increased contact resistance. Besides, 2DMs have a large conductivity anisotropy between the in- and out-of-plane directions. This means that, in multilayer devices, when a top-contact configuration is used, each interface between two layers acts as a tunneling barrier, decreasing the final performance of top-contacted devices, while in the case of edge contact, every single layer is contacted. The lack of reactivity of the basal planes in 2DMs also complicates an efficient bonding to the metal electrode in top-contact configuration. Density functional theory (DFT) calculations for graphene have shown that the shorter bonding distance in edge-contacted devices reduces significantly the contact resistance. Many studies have focused on TMDCs and, in particular, on MoS$_2$, a 2D material with a direct band gap for a monolayer and decent charge-carrier mobility, mechanical flexibility, and optical transparency, making it a good candidate for flexible devices, low-power electronics, photodetectors, and gas sensing. Here, we report on the fabrication of edge-contacted MoS$_2$ field effect transistors (FETs) where the lithography is performed by a combination of thermal scanning probe lithography (t-SPL) and direct laser writing (DLW) to avoid the exposure of the 2DM channel to energetic charged particles (ions and electrons) and UV radiation (see Supporting Information, section S1). As already proven in earlier work, t-SPL is well suited for these delicate materials: free from UV radiation or electrons, t-SPL uses a heated tip to locally create patterns reaching a resolution better than 10 nm. Typically, polyphthalaldehyde (PPA) is used as resist, as it thermally decomposes into volatile monomers above 150 °C. A direct laser write add-on incorporated within the t-SPL tool allows for a seamless combination of both micro- and nanopatterning processes to increase the patterning throughput. This method overcomes the problems of the other
approaches by substituting electrons, ions, and photons for patterning with a hot tip where only the upper part of the resist is exposed to heat and using the laser for the large pads located far away from the 2DM. Moreover, to avoid possible atmospheric contamination of the contacts, the etching of the 2DM and deposition of metallic contacts are performed in the same process chamber without breaking the vacuum.

Following this approach, we demonstrate the fabrication of top- and edge-contact MoS$_2$ FETs with a global silicon back gate (Figure 1b) and study systematically the performance of 29 devices. We show that the best performance is achieved with edge-contacted few-layer (FL) MoS$_2$ FETs, reaching a mobility of 38 cm$^2$ V$^{-1}$ s$^{-1}$ and an on/off ratio of $1 \times 10^8$ (air)/$1 \times 10^9$ (vacuum), while for monolayer (1L) devices, the highest achieved mobility is 7 cm$^2$ V$^{-1}$ s$^{-1}$ and the best on/off ratio is $7 \times 10^7$, also with edge-contact configuration. Besides, thanks to the freshly created edge surfaces on MoS$_2$, edge-contact FETs, both 1L and FL devices, show, in general, better electrical performance (higher mobility, higher on-state current, and lower contact resistance) than similar top-contacted devices.

### RESULTS AND DISCUSSION

**Fabrication Process.** In the following, the fabrication process of edge-contact MoS$_2$ shown in Figure 1c will be discussed (see Experimental Section for further information). MoS$_2$ flakes were exfoliated onto polymer films (X4 PF films, Gel-Pak). Upon inspection under an optical microscope, flakes of different thicknesses, ranging from monolayer to 8 nm, were chosen and transferred to the substrate consisting of 500 μm thick doped Si with a 200 nm thick layer of thermally grown SiO$_2$. The 2DM thickness was confirmed by Raman spectroscopy and/or atomic force microscopy (AFM).

For the fabrication of the contacts, a bilayer stack of 90 nm of polydimethylglutarimide (PMGI) and 30 nm of PPA was used. Contacts were patterned by a mix-and-match approach combining t-SPL for the small features on top of the semiconductor channel and DLW for larger features far away from the 2DM. Prior to patterning, the surface of the sample was imaged using the thermal-based readout of the t-SPL tool to find the area of interest. Then, the surface was scanned setting a target patterning depth equal to the thickness of PPA, creating the desired patterns with a markerless overlay accuracy of around 20 nm. Thanks to the closed-loop algorithm linking the thermal lithography and the reading, the system adjusts the voltage to correct for deviations in the target depth, which is required for successful lift-off processes as any residual PPA would prevent the opening of the PMGI in the following step. For the pads and other large features, the DLW system was adopted. In this case, a 405 nm laser was used, resulting also in the direct sublimation of PPA. Then, wet etching in diluted TMAH for 2 min was used to open the PMGI, controlling the undercut for the subsequent lift-off. TMAH can fully remove PMGI without deteriorating the 2DM, as reported in previous studies.

Previous studies have shown that even though MoS$_2$ is chemically very inert on its basal planes, the edges are much more reactive and can adsorb molecules when exposed to air. In particular, Ar milling was used to create Mo and S vacancies in MoS$_2$ and to fully etch the 2DM. In both cases, the newly created sites were much more reactive to molecules such as O$_2$. It has also been shown that edge-contact configurations can...
improve the contact to metals such as In, Au, Pd, and Ti by lowering tunnel barriers and strengthening the orbital overlaps.\textsuperscript{28} Hence, to create the contact through the edge, the flakes were milled using an Ar\textsuperscript{+} ion source in the same vacuum chamber in which the contacts were subsequently deposited, resulting in a complete etch of the MoS\textsubscript{2} in the patterned area without destroying the undercut needed in the resist for the subsequent lift-off. In this way, the dangling bonds from the just created edge can efficiently bond to the metal contacts. It has been previously reported that 2DM can be affected by chemical changes or kinetic energy transfer during metal deposition.\textsuperscript{11,29} For top contact, the evaporated materials would directly impinge the contact area affecting the contact area,\textsuperscript{29,30} whereas in the case of edge contact, the 2DM is presumably less affected due to the lower energy involved in the lateral diffusion of the deposited atoms to the 2DM edge.

The ion source milling process is 5 min long for all devices, meaning that for thinner ones there will be more etching of the SiO\textsubscript{2} underneath but always ensuring complete removal of the 2DM. To check the milling step, the same process was done without the metal evaporation step and the samples were characterized using optical microscopy, AFM, and Raman spectroscopy. All techniques showed that even the thicker parts of MoS\textsubscript{2} (>15 nm, thicker than those used for devices) were completely etched away (Supporting Information, Figure S2).

Regarding the selection of the contact electrode material, previous studies showed that Cr results in a shorter bonding length, lower potential barrier, and higher density of states at the Fermi level in top-contact FETs than other alternative metals for MoS\textsubscript{2}.\textsuperscript{31} For this reason, we opted for Cr as the electrode material for our initial devices. Given the fact that the ion-milling time is always the same and that our devices vary in thickness from 1L to FL devices of up to 8 nm, 20 nm of Cr were deposited by electron beam-induced physical vapor deposition (PVD) to ensure the edge contact is defined only through the Cr (only the sample used for TEM inspection has a thinner Cr layer, but it is not part of the devices analyzed within this paper). Then, a Au layer was deposited to protect the Cr from oxidation. However, the deposition of a 20 nm thick layer of Cr caused cracks in the film due to stress, inducing leakage of metal through the cracks that resulted in short circuits in some of the devices (Supporting Information, Figure S3). For this reason, Ti/Au was used in a second set of devices, showing a better fabrication yield but lower device performance (see Supporting Information, Table S1).

**TEM Characterization.** Cross-sectional scanning transmission electron microscopy (STEM) studies were carried out to have a closer insight into the nature of the 2DM—metal contact in one of our preliminary devices. For this experiment, a 6L MoS\textsubscript{2} flake was chosen. In this case, 5 nm of Cr and 25 nm of Au were used in the metallic side of the contact (note that all devices characterized in the rest of the manuscript are consistent in metal thickness with 20 nm of Cr or Ti and 5 nm of Au). Figure 2 shows a STEM image and the corresponding EDX map of an edge contact. In our PVD setup, the angle
between the samples and the evaporation source is around 7°; for this reason, some material is deposited laterally, resulting in “ears” that appear after lift-off (Figure 2a and 2b). This overhanging metal part appearing after lift-off from the lateral deposition of metals in the PMGI cavity protected the edge contact from the carbon deposited for the lamella preparation, allowing us to see the 6 layers of the MoS\(_2\) flake. This overhanging metal part does not affect the performance of the device as this part is not contacted to the 2DM. EDX experiments (Figure 2c and 2d and Figure S4) show the complete milling of the flake by the ion source. However, it is difficult to say if there is an oxidation of the MoS\(_2\) as the Cr-L line is superimposed on the O-K\(_\alpha\) line. It is worth noting that previous publications reported the need for tilted evaporation both for the ion source milling (to expose pristine MoS\(_2\)) and for the metal deposition (to achieve a successful contact).\(^{32}\)

However, due to the inherent angle between the metal source and the sample in our setup, we found that the contact is successful without specifically adding more tilting.

**Electrical Performance of MoS\(_2\) Transistors.** Previous reports show that for top contact, the performance of the devices, in particular, the mobility, is highly dependent on the number of layers.\(^5,33,34\) In top-contact configuration, the metal is in direct contact only with the topmost layer of the 2DM flake, and hence, the charge carriers need to overcome tunneling gaps to reach lower layers. Scattering from the MoS\(_2\)−SiO\(_2\) interface will affect the bottom layers of the device, and thinner flakes will be more affected by the substrate interface than thicker ones, where this effect will be partially screened.\(^5\) In the case of edge contact, we expect the influence of the substrate to have the same effect but with the benefit of having a contact to each single layer of the flake and, in turn, direct access for the current to be injected.

A set of 29 MoS\(_2\) devices with different channel thicknesses, lengths, and widths have been fabricated. For the sake of comparison, both edge- and top-contact configurations have been implemented. The fabrication process for both configurations is the same except that the ion source milling step (see Figure 1c, step 6) is not done in the case of top-contact devices. Table S1 in the Supporting Information shows the list of devices fabricated within this study, including Cr/Au and Ti/Au contacts and top- and edge-contact configurations. Here, we have chosen 3 representative devices to analyze them in more detail.

Figure 3 shows the transfer characteristics before and after thermal annealing (dashed and solid lines, respectively) for two edge-contact transistors using Cr as the contact metal: 1L MoS\(_2\) (Figure 3a and 3b, \(w_c = 7.7 \mu m; l_c = 2.4 \mu m\)) and FL MoS\(_2\) (Figure 3c and 3d, \(w_c = 4.5 \mu m; l_c = 4.9 \mu m, t_c = 6 \text{ nm}\)), where \(w_c\), \(l_c\), and \(t_c\) are the width, length, and thickness of the transistor channel, respectively. Figure 3a and 3c shows the drain current (\(I_{ds}\)) as a function of the back-gate voltage (\(V_{gb}\)) for various drain voltages (\(V_{ds}\)) measured in ambient conditions. As shown, the as-fabricated edge-contact FETs exhibit electron conduction behavior (n-type transport) and on/off ratios of about \(3 \times 10^6\) (1L) and \(6 \times 10^7\) (FL) with on-state currents of 2 and 19 \(\mu A\), respectively, at \(V_{ds} = 1 \text{ V}\). The electron field effect mobility can be extracted from the linear...
dependence of $I_n(V_{gs})$ in the strong inversion regime (see Supporting Information, section S5). As a result, mobilities of 1 and 20 cm$^2$ V$^{-1}$ s$^{-1}$ are calculated for the 1L and FL FETs, respectively. For the sake of comparison, the mobility has also been estimated with the Y-function method (see Supporting Information, section S5). In this case, we obtain electron mobilities of 0.2 and 36 cm$^2$ V$^{-1}$ s$^{-1}$ for the 1L and FL devices, respectively. For the monolayer, $I_n(V_{gs})$ shows a nonlinear response (see Figure 3b) that could originate from the Schottky barrier between the metal and the semiconductor. The asymmetry in these curves is a sign of different Schottky barrier heights (SBHs) in the two electrodes.

Previous studies have shown that annealing the devices in an inert atmosphere or vacuum can induce atomic rearrangement and improve bonding. As a result, annealing can reduce the contact resistance, increase mobility, and reduce hysteresis. Hence, we measured the electrical characteristics of the same devices before and after annealing at 250 °C for 3 h in N$_2$ atmosphere. We observe an increase in the mobility ($\mu_{slope}/\mu_s$), reaching values of $2/1$ and $31/38$ cm$^2$ V$^{-1}$ s$^{-1}$ for the 1L and FL FETs, respectively. The on-state currents and the on/off ratio also increased, reaching $I_{on} = 6$ (1L) and 28 (FL) μA (at $V_{ds} = 1$ V) and $I_{on}/I_{off} = 4 \times 10^7$ (1L) and $1 \times 10^8$ (FL).

Figure 4a–c shows the FL top-contact transistor ($w_1 = 4.4$ μm, $l_1 = 2.8$ μm, $t_1 = 4$ nm, Cr contacts) having the best performance among the fabricated ones. Figure 4a and 4c shows the corresponding $I_n(V_{gs})$ characteristics measured in air and vacuum, respectively. From the data in vacuum, at $V_{ds} = 1$ V, mobility values of 9 and 3 cm$^2$ V$^{-1}$ s$^{-1}$ were extracted with the slope and Y-function methods, respectively. The on/off ratio in this case was $1 \times 10^6$ and $I_{on} = 4$ μA. The $I_n(V_{gs})$ curve at $V_{ds} = 1$ V for the FL edge-contact device shown in Figure 3c and 3d is plotted in Figure 4d for the sake of comparison. It is worth noting that the $I_n(V_{gs})$ characteristics present a linear response in the range between $-1$ and $1$ V in vacuum, which was not the case for the response in air (see Figure 4b). This cannot be attributed to the SBH as we should not observe a variation between air and vacuum. As compared to the edge-contact FL device, the performance of the top-contact is worse, presumably due to the tunneling barriers from layer to layer and the possible contamination of the 2DM surface where the electrode is fabricated, as discussed also in previous works.

The Y-function method was also used to obtain the contact resistance, $R_c$ (see Supporting Information, section S5). The results of a representative set of samples are displayed in the Supporting Information in Table S1. In the case of Cr/Au contacts, a clear trend shows that top-contact devices present the highest contact resistance independently of the number of layers, which is most likely due to contamination between the electrode metal and the 2DM. Edge-contact devices show clear differences between 1L and FL, where the contact resistance of the later is at least one order of magnitude lower. In the case of Ti/Au, determining a clear trend is less obvious and the contact resistance is, in general, higher than that of Cr/Au contacts.

To determine the effect of temperature in the electrical response of the devices, additional $I_n(V_{ds})$ and $I_n(V_{gs})$ measurements were carried out with temperatures starting from 80 K until room temperature (see Supporting Information, section S6). For low temperatures, the response is less linear and $I_{on}$ is slightly lower, in accordance with previous studies. The variation in the electrical performance is more noticeable for devices where the performance is lower, which we attribute to a worse contact between the 2DM and the metallic electrode. This set of measurements was also used to obtain the SBH in the thermionic regime, leading to values of 68 and 87 meV for the edge- and top-contact FL devices, respectively (see Figure 5).

2DM devices are typically characterized by their variability due to the quality of the exfoliated flakes themselves, defects introduced during the fabrication process, and effects of the environment. In this paper, we present 29 devices, which helps to see some trends but underlines also the large variability among nominally similar devices. The fabricated devices are compared in terms of mobility, contact resistance, on/off ratio, and on-state current (Figure S10, Supporting Information). According to previous studies, mobility should be higher for 1L MoS$_2$ FETs than for that 2L or 3L devices. Despite a broad variation in the measured values, mobility clearly tends to increase with thickness, which was also reported in the past by different groups. This effect is most probably due to the molecules adsorbed on the channel upon exposure to air, which Lembke and co-workers avoided by doing the measurements in high vacuum and annealing the samples in situ to have a clean semiconductor channel. This effect is clearly more important for 1L FETs. Besides, the effect of the substrate has also an important contribution. It has been reported that the contribution of the scattering from the interface between SiO$_2$ and MoS$_2$ is critical for the degradation of mobility in monolayer devices, which is reduced with an.
also effective in preserving the performance of the FETs. Hence, adding an encapsulation step to our process might be necessary to protect the channel has been reported in several studies. In previous studies, the contact resistance is reduced and the hysteresis is observed that in most cases the electrical performance which we attribute to a mechanism of self-annealing through current (see Table S1 in Supporting Information). However, from day to day, there are variations in the device. We measured the $I_d(V_d)$ characteristics of some of our devices several months after their fabrication, and we observed that in most cases the performance decreased (Supporting Information, Figure S12). Some of them, especially monolayer devices, were no longer measurable after some months exposed to air. Encapsulating MoS$_2$ FETs with hBN$^{11,35}$ or a top layer deposited by ALD$^{44}$ to protect the channel has been reported in several studies. Hence, adding an encapsulation step to our process might be also effective in preserving the performance of the FETs.

Finally, the devices were electrically characterized in vacuum and compared to the measurements performed in air. We observe that in all cases, the hysteresis is reduced and the mobility and on current tend to be improved when measured in vacuum (see Supporting Information, Figure S13). This is in agreement with previous reports$^{34,42}$ and attributed to the adsorbed molecules in the MoS$_2$ surface (and water in particular), which are partially removed in the vacuum chamber. In vacuum, we achieved a maximum on/off ratio of 10$^9$.

**CONCLUSION**

In this work, we demonstrate a combination of t-SPL and DLW to fabricate edge-contact MoS$_2$ FETs in a gentle and clean manner. Neither energetic electrons nor UV photons are used near the semiconductor channel during lithography, avoiding the risk of deteriorating the properties of MoS$_2$. In addition, the edge-dangling bonds created by Ar$^+$ milling are kept in vacuum until the PVD deposition of the contact is performed. This fabrication method resulted in edge-contact FETs comparable to the state-of-the-art and with better performance than top-contact devices of similar characteristics fabricated following an analog approach. This is attributed to the cleaner interface between the 2DM and the metal. Both Ti and Cr were studied as possible contact metals. In spite of the cracks induced in Cr due to stress, this type of contact seems to result in lower contact resistance, higher performance, and less variability. For implementation in devices, FL FETs seem more promising than 1L devices as they present higher mobility, higher on-state currents, lower contact resistance, and less degradation.

**EXPERIMENTAL SECTION**

**Preparation of MoS$_2$ Flakes.** MoS$_2$ flakes were exfoliated from MoS$_2$ bulk (HQ_Graphene) onto PF films (Gel-Pack) glued on a glass slide and then transferred to the substrate consisting of 500 µm thick doped Si with a 200 nm thick layer of SiO$_2$.

**Fabrication of Edge-Contact MoS$_2$ Transistors.** The process flow for the fabrication of edge-contact MoS$_2$ transistors is shown in Figure 1c. The MoS$_2$/SiO$_2$/Si samples were dehydrated for 5 min at 190 °C in air. Then, PMGI SF25 (Microchem) was spin coated at 1000 rpm, followed by a bake of 3 min at 190 °C. A 1.3% solution of polyphthalaldehyde (PPA, Allresist) in anisole (abcr GmbH) was prepared and spin coated at 2000 rpm with a subsequent soft bake at 90 °C for 3 min. A commercial t-SPL system (Nanofrazor, Heidelberg Instruments) was used to pattern the contacts. A combination of t-SPL and DLW was used for smaller and bigger features, respectively. For t-SPL, the heater temperature was set to 950 °C and the step size and depth were fixed to 30 nm. For DLW, the step size was 50–100 nm, the pixel time was 70 µs, and the power was varied from 150 to 300 mW. Then, the pattern was transferred to the substrate by dipping the sample in AZ 726 MIF (2.38% TMAH in H$_2$O) for 120 s and then rinsing in DI water and isopropanol. For the milling of the flakes and the metal deposition, LAB600H (Leybold Optics) was used. The milling was performed using an end-Hall ion source (Kaufmann Robinson, Inc., KRI EH1000 equipped with a hollow cathode electron source KRI SHC-1000) for 300 s, and in the same chamber, the metals for the contacts were evaporated. A voltage of 160 V and a current of 3.5 A were used, resulting in a current density of around 0.5 mA/cm$^2$. Finally, lift off was performed in Remover 1165, followed by soft ultrasounds when needed.

**Fabrication of Top-Contact MoS$_2$ Transistors.** The MoS$_2$/SiO$_2$/Si samples were dehydrated for 5 min at 190 °C in air. Then, PMGI SF25 (Microchem) was spin coated at 1000 rpm, followed by a bake for 3 min at 190 °C. A 1.3% solution of polyphthalaldehyde (PPA, Allresist) in anisole (abcr GmbH) was prepared and spin coated at 2000 rpm with a subsequent soft bake at 90 °C for 3 min. A commercial t-SPL system (Nanofrazor, Heidelberg Instruments) was used to pattern the contacts. A combination of t-SPL and direct laser writing was used for smaller and bigger features, respectively. For t-SPL, the heater temperature was set to 950 °C and the step size and depth were fixed to 30 nm. For DLW, the step size was 50–100 nm, the pixel time was 70 µs, and the power was varied from 150 to 300 mW. The pattern was transferred to the substrate by dipping the sample in AZ 726 MIF (2.38% TMAH in H$_2$O) for 120 s and then rinsing in DI water and isopropanol. For the metal deposition of the electrodes, LAB600H (Leybold Optics) was used and the process finished with a lift off using Remover 1165, followed by soft ultrasounds when needed.

**Lamella Preparation and Cross-Sectional STEM.** A carbon layer was deposited on the sample to protect it from the focused ion beam (FIB). First, electron beam-assisted deposition at 5 kV was used to protect MoS$_2$ from ion implantation and surface damage. Then, a second carbon layer of around 1.3 µm was deposited using ion beam-assisted deposition at 30 kV and 150 pA. A lamella was cut perpendicular to one of the contacts to observe the interface between...
the edge of MoS₂ and the contact. A Thermo Fisher Tecnai Osiris transmission electron microscope was used to study the interface between the electrode and the 2DM. The HAADF STEM detector was used to image the contact, and EDX was performed to analyze the material composition of the interface.

**Electrical Measurements.** Electrical measurements of all devices were performed at room temperature and ambient conditions. Some devices were also characterized in vacuum (4 × 10⁻⁶ mbar). For the Schottky barrier height extraction, some of the best devices were measured for a set of temperatures ranging from 80 to 300 K, also in vacuum. The standard DC measurements were performed using a HP4156A Semiconductor Parameter Analyzer and a Cascade Summit probe station.

**ASSOCIATED CONTENT**

**Supporting Information**

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.2c10150. The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.2c10150.

Thermal scanning probe, Ar⁺ milling, cracks in the Cr layer, TEM characterization, fabricated devices, low-temperature measurements, effect of thickness, configuration and electrode material in the performance of the device, reproducibility of the measurements, stability of the devices over time, and effect of ambient atmosphere in the device performance (PDF)

**AUTHOR INFORMATION**

**Corresponding Author**
Ana Conde-Rubio — Microsystems Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland; Present Address: Institute of Materials Science of Barcelona (ICMAB-CSIC), Campus de la UAB, 08193 Bellaterra, Catalonia, Spain; orcid.org/0000-0001-5739-2189; Phone: +34 93 255 73; Email: aconde@icmab.es

**Authors**
Xia Liu — Microsystems Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland; orcid.org/0000-0003-1886-6825
Giovanni Boero — Microsystems Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland
Jürgen Brugger — Microsystems Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland; orcid.org/0000-0002-7710-5930

Complete contact information is available at: https://pubs.acs.org/10.1021/acsami.2c10150

**Notes**

The authors declare no competing financial interest.

**ACKNOWLEDGMENTS**

The authors thank the Center of Micro/Nanotechnology (CMi) of EPFL. We also thank Sadegh Kamaei, Teodor Rosca, and Prof. A. M. Ionescu for their help with the electrical measurement set-up and access to their instruments. This work received funding from the European Research Council (ERC) under the European Union’s Horizon 2020 Research and Innovation Program (Project “MEMS 4.0”, ERC-2016-ADG, grant agreement no. 742685).

**REFERENCES**

(1) Pezo, A.; Lima, M. P.; Costa, M.; Fazzio, A. Electronic transport properties of MoS₂ nanoribbons embedded in butadiene solvent. *Phys. Chem. Chem. Phys.*, 2019, 21, 11359–11366.
(2) Son, Y.; Wang, Q. H.; Paulson, J. A.; Shih, C.-J.; Rajan, A. G.; Tvdry, K.; Kim, S.; Alfeeli, B.; Braatz, R. D.; Strano, M. S. Layer Number Dependence of MoS₂ Photoconductivity Using Photocurrent Spectral Atomic Force Microscopic Imaging. *ACS Nano* 2015, 9, 2843–2855.
(3) Conley, H. J.; Wang, B.; Ziegler, J. I.; Haglund, R. F.; Pantelides, S. T.; Bolotin, K. I. Bandgap Engineering of Strained Monolayer and Bilayer MoS₂. *Nano Lett.* 2013, 13, 3626–3630.
(4) Liu, X.; Sachan, A. K.; Howell, S. T.; Conde-Rubio, A.; Knoll, A. W.; Boero, G.; Zenobi, R.; Brugger, J. Thermomechanical Nanoraming of Two-Dimensional Materials. *Nano Lett.* 2020, 20, 8250–8257.
(5) Liu, W.; Kang, J.; Cao, W.; Sarkar, D.; Khatami, Y.; Jena, D.; Banerjee, K. High-performance few-layer-MoS₂ field-effect-transistor with record low contact-resistance. 2013 IEEE International Electron Devices Meeting; IEEE, 2013; pp 1–19.
(6) Matsunaga, M.; Higuchi, A.; He, G.; Yamada, T.; Krüger, P.; Ochiya, Y.; Gong, Y.; Vajtai, R.; Ajayan, P. M.; Bird, J. P.; Aoki, N. Nanoscale-Buffer Formation Induced by Low-Dose Electron-Beam Exposure in Ultrathin MoS₂ Transistors. *ACS Nano* 2016, 10, 9730–9737.
(7) Imamura, G.; Sakki, K. Modification of Graphene/SiO₂ Interface by UV-Irradiation: Effect on Electrical Characteristics. *ACS Appl. Mater. Interfaces* 2015, 7, 2439–2443.
(8) Cheng, Z.; Abuzaid, H.; Yu, Y.; Zhang, F.; Li, Y.; Noyce, S. G.; Williams, N. X.; Lin, T.-C.; Doherty, J. L.; Tao, C.; Cao, L.; Franklin, A. D. Convergent ion beam alteration of 2D materials and metal-2D interfaces. *2D Materials* 2019, 6, 034005.
(9) Cheng, X.; Calò, A.; Albisetti, M.; Liu, X.; Alharbi, A. S. M.; Arefe, G.; Liu, X.; Spiezer, M.; Yoo, W. J.; Taniguchi, T.; Watanabe, K.; Aruta, C.; Ciarrocchi, A.; Kis, A.; Lee, B. S.; Lipson, M.; Hone, J.; Shahjerdi, D.; Riedo, E. Patterned metal contacts on monolayer MoS₂ with vanishing Schottky barriers using thermal nanolithography. Nat. Electron. 2019, 2, 17–25.
(10) Yan, X.; Jia, K.; Su, Y.; Ma, Y.; Luo, J.; Zhu, H.; Wei, Y. Edge-Contact Formed by Oxygen Plasma and Rapid Thermal Annealing to Improve Metal-Graphene Contact Resistance. *ECS Journal of Solid State Science and Technology* 2018, 7, M11–M15.
(11) Wang, Y.; Kim, J. C.; Wu, R. J.; Martinez, J.; Song, X.; Yang, J.; Zhao, F.; Mikhoyan, A.; Jeong, H. Y.; Chihowlalla, M.; Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature* 2019, 568, 70–74.
(12) Allain, A.; Kang, J.; Banerjee, K.; Kis, A. Electrical contacts to two-dimensional semiconductors. *Nat. Mater.* 2015, 14, 1195–1205.
(13) Yang, Z.; Kim, C.; Lee, K. Y.; Lee, M.; Appalakondaiah, S.; Ra, C.; Watanabe, K.; Taniguchi, T.; Cho, K.; Hwang, E.; Hone, J.; Yoo, W. J. A Fermi-Level-Pinning-Free 1D Electrical Contact at the Intrinsic 2D MoS₂–Metal Junction. *Adv. Mater.* 2019, 31, 1808231.
(14) Cheng, Z.; Yu, Y.; Singh, S.; Price, K.; Noyce, S. G.; Lin, Y.-C.; Cao, L.; Franklin, A. D. Immunity to Contact Scaling in MoS₂ Transistors Using in Situ Edge Contacts. *Nano Lett.* 2019, 19, 5077–5085.
(15) Chu, T.; Chen, Z. Understanding the Electrical Impact of Edge Contacts in Few-Layer Graphene. *ACS Nano* 2014, 8, 3584–3589.
(16) Matsuda, Y.; Deng, W.-Q.; Goddard, W. A. Contact Resistance for “End-Contacted” MetalGraphene and MetalNanotube Interfaces from Quantum Mechanics. *J. Phys. Chem. C* 2010, 114, 17845–17850.
(17) Manzeli, S.; Ovchinnikov, D.; Pasquier, D.; Yazeyev, O. V.; Kis, A. 2D transition metal dichalcogenides. *Nat. Rev. Mater.* 2017, 2, 17033.
(18) Singh, E.; Singh, P.; Kim, K. S.; Yeom, G. Y.; Nalwa, H. S. Flexible Molybdenum Disulphide (MoS₂) Atomic Layers for Wearable Electronics and Optoelectronics. *ACS Appl. Mater. Interfaces* 2019, 11, 11061–11105.
(19) Zhang, H.; Shi, B.; Xu, L.; Yan, J.; Zhao, W.; Zhang, Z.; Zhang, Z.; Lu, J. Sub-5 nm Monolayer MoS₂ Transistors toward Low-Power Devices. *ACS Appl. Electron. Mater.* 2021, 3, 1560–1571.

(20) Lopez-Sanchez, O.; Lemke, D.; Kayci, M.; Radenovic, A.; Kis, A. Ultrasonic photodetectors based on monolayer MoS₂. *Nat. Nanotechnol.* 2013, 8, 497–501.

(21) Late, D. J.; Huang, Y.-K.; Liu, B.; Acharya, J.; Shirodkar, S. N.; Luo, J.; Yan, A.; Charles, D.; Waghmare, U. V.; Dravid, V. P.; Rao, C. N. R. Sensing Behavior of Atomically Thin-Layered MoS₂ Transistors. *ACS Nano* 2013, 7, 4879–4891.

(22) Liu, X.; Howell, S. T.; Conde-Rubio, A.; Boero, G.; Brugger, J. Thermomechanical Nanocutting of 2D Materials. *Adv. Mater.* 2020, 32, 2001232.

(23) Howell, S. T.; Grushina, A.; Holzner, F.; Brugger, J. Thermal scanning probe lithography—a review. *Microsyst. Nanoeng.* 2020, 6, 21.

(24) Coulembier, O.; Knoll, A.; Pires, D.; Gotsmann, B.; Duerig, U.; Frommer, J.; Miller, R. D.; Dubois, P.; Hedrick, J. L. Probe-based nanolithography: Self-amplified depolymerization media for dry lithography. *Macromolecules* 2010, 43, 572–574.

(25) Rawlings, C.; Ryu, Y. K.; Rüegg, M.; Lassaline, N.; Schwemmer, C.; Duerig, U.; Knoll, A. W.; Durrani, Z.; Wang, C.; Liu, D.; Jones, M. E. Fast turnaround fabrication of silicon point-contact quantum-dot transistors using combined thermal scanning probe lithography and laser writing. *NanoTechnology* 2018, 29, 505302.

(26) Ashokhbai Patel, K.; Grady, R. W.; Smither, K. K. H.; Pop, E.; Sordan, R. Ultra-scaled MoS₂ transistors and circuits fabricated without nanolithography. *2D Mater.* 2020, 7, 015008.

(27) Cheng, Z.; Cardenas, J. A.; McGuire, F.; Najmaei, S.; Franklin, A. D. Modifying the Ni-MoS₂ Contact Interface Using a Broad-Beam Ion Source. *IEEE Electron Device Lett.* 2016, 37, 1234–1237.

(28) Kang, J.; Liu, W.; Sarkar, D.; Jena, D.; Banerjee, K. Computational Study of Metal Contacts to Monolayer Transition-Metal Dichalcogenide Semiconductors. *Physical Review X* 2014, 4, 031005.

(29) Liu, Y.; Guo, J.; Zhu, E.; Liao, L.; Lee, S.-J.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X. Approaching the Schottky—Mott limit in van der Waals metal—semiconductor junctions. *Nature* 2018, 557, 696–700.

(30) Kim, C.; Moon, I.; Lee, D.; Choi, M. S.; Ahmed, F.; Nam, S.; Cho, Y.; Shin, H.-J.; Park, S.; Yoo, W. J. Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides. *ACS Nano* 2017, 11, 1588–1596.

(31) Luo, B.; Liu, J.; Zhu, S. C.; Yi, L. Chromium is proposed as an ideal metal to form contacts with monolayer MoS₂ and WS₂. *Materials Research Express* 2015, 2, 106501.

(32) Jain, A.; Szabó, r; Parzefall, M.; Bonvin, E.; Taniguchi, T.; Watanabe, K.; Bhuradwaj, P.; Lusier, M.; Novotny, L. One-Dimensional Edge Contacts to a Monolayer Semiconductor. *Nano Lett.* 2019, 19, 6914–6923.

(33) Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS₂ Transistors with Scandium Contacts. *Nano Lett.* 2013, 13, 100–105.

(34) Lemke, D.; Allain, A.; Kis, A. Thickness-dependent mobility in two-dimensional MoS₂ transistors. *Nanoscale* 2015, 7, 6255–6260.

(35) Chang, H.-Y.; Zhu, W.; Akinwande, D. On the mobility and contact resistance evaluation for transistors based on MoS₂ or two-dimensional semiconducting atomic crystals. *Appl. Phys. Lett.* 2014, 104, 113504.

(36) Cai, F.; Deng, G.; Li, X.; Lin, F. Contact Resistance Parallel Model for Edge-Contacted 2D Material Back-Gate FET. *Electronics* 2020, 9, 2110.

(37) Sangwan, V. K.; Hersam, M. C. Electronic Transport in Two-Dimensional Materials. *Annu. Rev. Phys. Chem.* 2018, 69, 299–325.

(38) Gupta, S.; Rortais, F.; Ohshima, R.; Ando, Y.; Endo, T.; Miyata, Y.; Shiraishi, M. Monolayer MoS₂ field effect transistor with low Schottky barrier height with ferromagnetic metal contacts. *Sci. Rep.* 2019, 9, 17032.