A single event upset tolerant latch with parallel nodes

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Abstract A single event upset (SEU) tolerant latch has been put forward in the current paper. By means of the parallel nodes structure design together with the layout-level optimization design, the proposed design is capable of substantially improving the immunity to SEU. In comparison with the conventional latch, the stacked latch with isolation and the dual-modular-redundancy (DMR) latch with C-element, the simulation results based on the 65 nm CMOS process demonstrate that the proposed latch performs much better in SEU mitigation. For P-hit simulation, the proposed latch can achieve a correct output in the end, no matter the struck PMOS is at OFF state or ON state. For N-hit simulation, the proposed latch is also capable of mitigating the voltage transient and recovering to original state eventually.

Keywords: latch, N-hit, P-hit, single event upset

Classification: Integrated circuits

1. Introduction

Radiation striking in integrated circuits (ICs) is likely to result in soft errors \cite{s1, s2, s3, s4, s5, s6, s7}. For the ICs in spaceflight systems, when semi-conductor material is struck by the highly energetic particles that existing in the outer space, the generated carriers are likely to be gathered by the sensitive nodes. It is likely to cause voltage transients at the nodes \cite{s8, s9, s10, s11, s12, s13}. If the voltage transients occur at the storage nodes of latches, the data stored might be flipped \cite{s7, s14, s15, s16, s17, s18}.

The stacked latch with isolation technique put forward in reference \cite{s19} can lower the SEU sensitivity of latch effectively. Through the division of a PMOS into two serial PMOSs and then making use of shallow trench isolation (STI) to isolate the two PMOSs, the radiation immunity can be substantially enhanced in a case where the struck PMOS is at OFF state \cite{s19, s20}. But if an ion hits at the drain of the ON PMOS, the potential of the drain might drop to low level \cite{s21, s22}. As we know, there are numerous electrons as well as holes will be generated along the penetration path subsequent to an ion striking. The N-well will constrain the electrons, which will cause the dropping of N-well potential. Close to the P-N junction that is caused by the drain of the struck PMOS and N-well, the built-in electric field will drive electrons in N-well to the drain. Accordingly, the potential of the drain will decrease to even logic “0”. In a case where the energy of the ion striking is large enough, the data stored in latch is likely to be altered.

The DMR latch with C-element is a typical way to achieve radiation hardening \cite{s23, s24, s25}. However, it can only rectify one upset of the original latch or the duplicated latch. If the ion striking disturbs the data of the two latches and causes upset among the two latches, the final output of the DMR latch will also be upset \cite{s14}.

In the current paper, we put forward a SEU hardened latch with structure of parallel nodes, and combined with the layout-level design, the proposed approach is capable of mitigating the SEU effectively.

2. The proposed latch

Fig. 1 presents the schematic of the proposed latch. D represents the input signal. In addition to that, the system clock and negative system clock are CLK and CLKB, correspondingly. Signal D is divided into signals n0 and n1 by the transmission gates T0 and T1. Signals n0 and n1 connect to the gates of the PMOSs and the NMOSs of INV1, respectively. The outputs of INV1 are n2 and n3. Signal n2 connects to the gate of P8 together with gates of PMOSs at INV2. And signal n3 connects to the gate of N8 together with the gates of NMOs at INV2. Signals n4 and n5 are the outputs of INV2, and they feedback signals n0 and n1 by the transmission gates T2 and T3, respectively. The final output signal is marked as Q. INV1 and INV2 constitute the storage structure of the latch, and the placement of the MOSFETs of the storage structure of the proposed latch has been presented in Fig. 2. The x-z plain and the +y-axis are parallel and vertical to the surface of the cell, correspondingly.

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{fig1.png}
\caption{The schematic of the proposed latch.}
\end{figure}
When CLK = “1” and CLKB = “0”, T₀ and T₁ will be turned on, and T₂ and T₃ will be turned off. Accordingly, the latch will work in the transparent mode of operation. When CLK = “0” and CLKB = “1”, T₀ and T₁ will be turned off, and T₂ and T₃ will be turned on. Accordingly, the latch will work in the latching mode of operation. We mainly discuss the situation that the latch works in the latching mode while being hit by an ion.

Case 1: P-hit

1) We assume that the signals n₀, n₁, n₄ and n₅ are “1”, and the signals n₂ and n₃ are “0”.

If the drain of P₁ gets struck by an ion, the voltage of n₂ might raise to high level. Thus, P₄, P₅, P₆, P₇ and P₈ will be turned off. Nevertheless, the voltage of n₃ is still logic “0”, so N₄, N₅, N₆, N₇ and N₈ will keep at OFF state. Therefore, the nodes n₄, n₅ and Q will not be discharged, and their states can be held. Besides that, the signal n₂ will recover from the transient voltage pulse eventually. The data stored in the proposed latch will not upset.

If the drain of P₁ gets struck by an ion, the voltage variation might occur at signal n₃, but the logic level of n₃ will not change. This is owing to the fact that we make use of the isolation approach in the layout. Just as evident from Fig. 2, P₂ is isolated from P₃ by STI. In this way, the bipolar effect can be weakened significantly. Therefore, the amplitude of voltage variation can be lowered substantially. Moreover, N₂ is at ON state, which will discharge the source of N₁, so the voltage variation that is caused by the ion striking can be mitigated further. As a result, the ion striking at the drain of P₁ will not change the logic level of n₃. And the proposed latch is capable of holding the data.

2) We assume that the signals n₀, n₁, n₄ and n₅ are “0”, and the signals n₂ and n₃ are “1”.

If the drain of P₁ is hit by an ion, the voltage of n₂ will stay at high level because the source of P₁ is connected to VDD and P₁ is conducted on. The ion striking has little impact on the node n₂ as well as other storage nodes, and the final output will be correct steadily.

If the drain of P₁ is hit by an ion, the voltage of n₃ might decrease owing to the drawback of using isolation approach. We make an assumption that the voltage of n₃ decreases to low level, which turns on N₄, N₅, N₆, N₇ and N₈. But the signal n₂ remains at high level, so P₄, P₅, P₆, P₇ and P₈ will not be conducted on, and the logic levels of n₄, n₅ as well as Q will not change. And the voltage of n₃ will recover to the original value in the end.

Case 2: N-hit

As we know, the ion striking at the drain of NMOS will cause the dropping of the potential of the drain [26]. If the potential of the drain is low, the potential will decrease further after ion striking, but the logic level of the drain will still be logic “0”. If the potential of the drain is high, the potential is likely to decrease to low level after ion striking. So, this is the main situation that we should consider.

We assume that the signals n₀, n₁, n₄ and n₅ are “0”, and the signals n₂ and n₃ are “1”.

If the drain of N₁ gets struck by an ion, the voltage of n₂ may decrease. But P₀ is at ON state, so the source of N₁ will be charged by P₀. It will mitigate the dropping of voltage of n₂. We develop an assumption that the voltage of n₂ decreases to low level, which turns on P₄, P₅, P₆, P₇ and P₈. Nevertheless, the voltage of n₃ is still logic “1”, so N₄, N₅, N₆, N₇ and N₈ will keep at ON state, the ion striking will not cause a full-swing transient at the nodes n₄, n₅ and Q. Additionally, as evident from Fig. 2, in the layout we place the drain of N₄ close to the drain of N₁. Thus, the charge that is generated owing to the ion striking can be also gathered by the drain of N₄, which can reduce the quantity of the charge that is collected by the drain of N₁. In addition, the drain of N₄ collecting charge can suppress the rising of voltage of node n₄ that is caused by the voltage variation at node n₂. Thus, the impact of ion striking at the drain of N₁ will be mitigated further. The storage nodes of the proposed latch will recover to their original states at last.

If the drain of N₁ gets struck by an ion, the voltage of n₃ may decrease. Fig. 2 shows that the drain of N₀ is placed close to the drain of N₁, so the drain of N₀ can share the charge that is generated because of the ion striking, which will reduce the quantity of the charge that is collected by the drain of N₁ and weaken the voltage variation. We assume that the voltage of n₃ drops to logic “0”, N₄, N₅, N₆, N₇ and N₈ are turned off accordingly. Nonetheless, the voltage of n₂ remains being logic “1”, which will keep P₄, P₅, P₆, P₇ and P₈ at OFF state. The nodes n₄, n₅ and Q will not be charged, and the voltage of node n₃ will recover to high level eventually, which implies that the storage data of the proposed latch can be held.

Based on the above analysis, we can find out that the proposed design is capable of improving the immunity to SEU significantly. For P-hit, the nodes n₂ and n₃ are not sensitive to ion striking simultaneously, so the proposed latch can recover to the correct state in the end. For N-hit, the proposed design can also prevent the ion striking from causing upset of the storage data.

3. Simulations and analysis

Simulations are performed for different latches, which are the conventional latch, the stacked latch with isolation, the DMR latch with C-element and the proposed latch. All circuits are simulated in 65 nm CMOS technology with a supply voltage of 1.2 V. The gate lengths and widths of all transistors are set to 65 nm and 140 nm, correspondingly.

3.1 Circuit-level performance

The simulation results of circuit-level performance including area, delay, and power consumption. According to references [10, 14], we use the number of the transistors in the latch to represent the area of the latch. The delay is measured through calculating the delay from the input D to
the output Q when the latch works in the transparent mode of operation. And the delay as well as the power consumption of each latch is normalized to which of the conventional latch in order to clearly demonstrate the differences.

The comparisons of different latches have been presented in Table I. The transistors in the proposed latch is a few more than that in the DMR latch with C-element. It can be observed that the delay of the proposed latch is smaller than the stacked latch with isolation. Moreover, the power consumption of the proposed latch is lower as compared with the DMR latch with C-element. Thus, the cost of circuit-level performance of the proposed design is acceptable. In addition, the proposed latch has much better SEU immunity compared with the existing latches.

### Table I. Circuit-level performance comparisons between different latches.

|                | Number of transistors | Delay (ns) | Power (mW) |
|----------------|-----------------------|------------|------------|
| Conventional   | 10                    | 1          | 1          |
| Stacked        | 14                    | 2.1288     | 0.7791     |
| DMR            | 20                    | 1.3042     | 1.9394     |
| Proposed       | 26                    | 1.9568     | 1.5152     |

#### 3.2 SEU Tolerance

Three-dimensional mixed-mode (TCAD) simulation is adopted in this paper, which has been proven to be a useful means of investigating single-event effects (SEEs) in ICs [20, 27, 28, 29, 30]. The MOSFETs used in storage structures of these latches are built with the use of TCAD numerical models, and the others employ the SPICE models. As shown in Fig. 3, for well matched electrical characteristics, the TCAD models of the MOSFETs that are used in simulations are calibrated to the commercial 65 nm bulk CMOS process design kit (PDK). Vd and Vg represent the voltage of the drain and gate, respectively, and Id means the current of the drain.

In the simulation, the transistors are made on a $20 \times 20 \times 20 \mu m^3$ P-substrate with a constant doping of $1 \times 10^{18} \text{cm}^{-3}$. Also, the backside of the substrate contact is utilized along the bottom surface. Meanwhile, the N-well, P-well and P+ deep well are made with Gaussian doping profiles with the peak value of $1 \times 10^{17} \text{cm}^{-3}$, $1 \times 10^{18} \text{cm}^{-3}$ and $1 \times 10^{19} \text{cm}^{-3}$, respectively. The heavy ion striking is modeled with charge-track length and radius of 10 µm and 50 nm, respectively. In addition, the ion strikes at the center of the drain and proceeds through the device, and the LET value is kept constant along the heavy ion track. The spatial and temporal distributions of charge around the ions track are modeled using the Gaussian radial profile [20, 27]. In addition, according to the references [20, 27], we assume that the ion strikes the proposed latch with the LET values at 10, 30, 50, 70, and 90 MeV·cm$^2$/mg. Moreover, we assume that the latches work in the latching mode.

**Case 1: P-hit**

1) In a case where the storage data of the latch is “0”, i.e., the voltage of storage node ($V_{sn}$) is at low level, and the voltage of output node Q ($V_Q$) is high.

As for the conventional latch, if an ion strikes at the drain of the storage PMOS, the data is likely to upset. As shown in Fig. 4, when the ion strikes vertically, the SEU threshold of it is between 1.0 MeV·cm$^2$/mg and 1.1 MeV·cm$^2$/mg.

As for the proposed latch, if the ion hits at the drain of P1 vertically, the simulation results are shown in Fig. 5(a). We can see that the voltage of node n2 ($V_{n2}$) rises to high level rapidly after the ion striking, and the transient pulse that occurs at node n2 becomes wider with the increase of LET value. The high level n2 turns off P8 and the PMOSs in INV2. Nonetheless, the voltage of node n3 ($V_{n3}$) remains at low level. Accordingly, n8 and the NMOSs in INV2 keep at OFF state. Thus, the final output Q can stay at high level. And the nodes n4 and n5 can hold their states, so the signal n2 recovers from the transient pulse at last.

![Fig. 3. Id-Vg and Id-Vd curves of PDK and TCAD.](image)

![Fig. 4. The simulation results of conventional latch when the ion strikes at the drain of the OFF PMOS vertically.](image)

![Fig. 5. The simulation results of proposed latch when the ion strikes at the drain of the OFF PMOS vertically.](image)

If the ion hits at the drain of P3 vertically, the simulation results are shown in Fig. 5(b). As discussed in section 2, the voltage variation still occurs at the node n3, but the logic level does not change. The internal nodes of the proposed latch are able to keep at their original logic levels, and the proposed latch can keep a correct output steadily.

The angle striking of heavy ion has been investigated in the current paper as well. Angle 60° is widely adopted in simulations to perform the influence of the ion striking angle on device [27, 28, 29, 30]. Thus, we set the angle between the $+y$-axis and the direction of the ion striking to 60°.

With regard to the DMR latch with C-element, if the ion strikes with the projection direction from the drain of PMOS at the original latch towards the drain of PMOS at the duplicated latch, and the voltage of the storage node of the original latch ($V_{sn0}$) and the voltage of the storage node of the duplicated latch ($V_{sn1}$) are both disturbed, then the
final output of this latch is likely to turn over. As shown in Fig. 6, its SEU threshold is between 12 to 13 MeV·cm²/mg.

As for the proposed design, the projection directions of ion striking in the x-z plane are present in Fig. 7. Direction (1), direction (2) and direction (3) represent that the projection directions of ion striking in the x-z plane are from the drain of P₁ towards the drain of P₃, the drain of P₅ and the drain of P₇, correspondingly. Direction (4), direction (5) and direction (6) imply that the projection directions of ion striking in the x-z plane are from the drain of P₃ towards the drain of P₁, the drain of P₇ and the drain of P₅, correspondingly.

The simulation results of ion striking with angle 60° of the proposed latch are presented in Fig. 8. When the ion strikes the proposed latch with angle 60°, the proposed latch can also mitigate the impact of ion striking. The proposed design can remain the original output even under an ion striking that has the LET value equivalent to 90 MeV·cm²/mg, which performs better than the DMR latch with C-element.

2) In a case where the storage data of the latch is "1", i.e., \( V_{sn} \) is at high level, and the output Q is low.

The simulation results of ion striking with angle 60° of the proposed latch are presented in Fig. 8. When the ion strikes the proposed latch with angle 60°, the proposed latch can also mitigate the impact of ion striking. The proposed design can remain the original output even under an ion striking that has the LET value equivalent to 90 MeV·cm²/mg, which performs better than the DMR latch with C-element.

As for the stacked latch with isolation technique, as discussed in section 1, if an ion strikes at the drain of the ON PMOS, the potential of the drain will decrease even to logic "0", which is likely to change the data that is stored in latch. As evident from Fig. 9, when the ion strikes vertically, the voltage of storage node decreases sharply, and the SEU threshold of the stacked latch is between 72 to 73 MeV·cm²/mg.

As mentioned in section 2, we mainly discuss the situation that the potential of the drain of NMOS is logic "1". We assume that the storage data of the latch is "1", i.e., \( V_{sn} \) is at high level, and the output Q is low.

Fig. 12(a) and Fig. 12(b) present the simulation results of the conventional latch and the stacked latch with isolation technique, respectively. We can observe that the voltage of the storage node decrease rapidly subsequent to the ion striking at the NMOS. The SEU thresholds of the conventional latch and the stacked latch are between 0.5 to 0.6 MeV·cm²/mg and between 0.7 to 0.8 MeV·cm²/mg, respectively.

As for the proposed latch, when the ion hits at the drain of \( N₁ \) vertically, Fig. 13(a) presents the simulation results.

As for the proposed design, if the ion hits at the drain of \( P₁ \) vertically, the simulation results are shown in Fig. 10(a). After ion striking, the voltage of n2 is disturbed, but its logic level still keeps at "1". The ion striking has little impact on the final output Q. The output node Q can hold the state steadily, as well as the internal nodes of the proposed latch.

If the ion hits at the drain of \( P₃ \) vertically, the simulation results are shown in Fig. 10(b). The negative voltage pulse occurs at the signal n3, and the width of the pulse gets larger with the increase in the LET value. The NMOSs at INV2 and N₈ will change to OFF state, if the voltage of n3 is sufficiently low. However, the signal n2 remains at high level, which can keep \( P₈ \) at OFF state. Thus, the node Q can stay at low level. In the same manner, the PMOSs at INV2 also keep at OFF state, so the nodes n4 and n5 can hold their states. And the signal n3 can recover to "1" in the end.

The simulation results of ion striking at the ON PMOS with angle 60° are shown in Fig. 11. When the drain of \( P₁ \) is hit by an ion, the voltage variation that caused by ion striking can not change the logic level of node n2. The proposed latch can maintain a correct output all along, which has been presented in Fig. 11(a), (b) and (c). When the drain of \( P₃ \) gets hit by an ion, it still causes voltage variation at the struck node. Nevertheless, the proposed latch can mitigate the variation and achieve a correct output as might be expected.

Case 2: N-hit

As the proposed design, if the ion hits at the drain of \( P₁ \) vertically, the simulation results are shown in Fig. 10(a). After ion striking, the voltage of n2 is disturbed, but its logic level still keeps at "1". The ion striking has little impact on the final output Q. The output node Q can hold the state steadily, as well as the internal nodes of the proposed latch.

As for the proposed design, if the ion hits at the drain of \( P₃ \) vertically, the simulation results are shown in Fig. 10(b). The negative voltage pulse occurs at the signal n3, and the width of the pulse gets larger with the increase in the LET value. The NMOSs at INV2 and N₈ will change to OFF state, if the voltage of n3 is sufficiently low. However, the signal n2 remains at high level, which can keep \( P₈ \) at OFF state. Thus, the node Q can stay at low level. In the same manner, the PMOSs at INV2 also keep at OFF state, so the nodes n4 and n5 can hold their states. And the signal n3 can recover to "1" in the end.

The simulation results of ion striking at the ON PMOS with angle 60° are shown in Fig. 11. When the drain of \( P₁ \) is hit by an ion, the voltage variation that caused by ion striking can not change the logic level of node n2. The proposed latch can maintain a correct output all along, which has been presented in Fig. 11(a), (b) and (c). When the drain of \( P₃ \) gets hit by an ion, it still causes voltage variation at the struck node. Nevertheless, the proposed latch can mitigate the variation and achieve a correct output as might be expected.
The voltage of n2 decreases to logic “0” after striking, which conducts on P8 and the PMOSs at INV2. Nonetheless, the high level n3 can keep the corresponding pull down NMOSs at ON state. In this way, the transient at n2 can not cause a full-swing voltage pulse at the final output. And as discussed in section 2, the output node Q together with the storage nodes can recover to correct states eventually.

When the ion strikes at the drain of N3 vertically, Fig. 13(b) presents the simulation results. The voltage of node n3 changes to logic “0” subsequent to ion striking. The NMOSs at INV2 as well as N8 are turned off because of the low level n3. Nonetheless, the voltage of node n2 keeps at logic “1”, so the PMOSs at INV2 together with P8 can stay at OFF state. Thus, the states of n4, n5 and Q can be held, and the node n3 can recover to its original state at last.

If the ion hits at the drain of NMOS with angle 60°, the simulation results of the DMR latch with C-element are disappointing. We assume that the projection direction of the ion striking is from the drain of NMOS at the original latch towards the drain of NMOS at the duplicated latch, the simulation results are shown in Fig. 14. When the voltage of the storage node at the original latch and the voltage of the storage node at the duplicated latch are both disturbed by the incident ion, the final output Q will be upset unquestionably. And its SEU threshold is between 35 to 36 MeV·cm²/mg.

With regard to the proposed latch, the projection directions of N-hit in the x-z plane are presented in Fig. 15. Direction (1) and direction (2) imply that the projection directions of ion striking in the x-z plane are along with the −x-axis and +x-axis, respectively. Direction (4) and direction (5) have the same meanings. Direction (3) and direction (6) represent that the projection directions of ion striking in the x-z plane are from the drain of N1 towards the drain of N3 and from the drain of N3 towards the drain of N1, correspondingly.

Fig. 16 presents the simulation results of N-hit with angle 60° of the proposed latch. As evident to us, the proposed latch displays a good performance in SEU mitigation. Although the voltage variation occurs at the struck node, the nodes n2, n3 and Q can recover to the original states at last.

4. Conclusion

In this paper, we put forward a radiation hardened latch, which is investigated in 65 nm CMOS process. The parallel nodes structure design in combination with the layout placement optimization can enhance the SEU immunity of the proposed latch significantly. In comparison with the conventional latch, the stacked latch with isolation and the DMR latch with C-element, with regard to P-hit simulations, the proposed latch can achieve the SEU mitigation effectively, no matter the struck PMOS is at OFF state or ON state. With regard to N-hit simulations, the proposed latch also performs better as compared with the existing latches in tolerating the SEU. Meanwhile, the cost of circuit-level performance of the proposed design is acceptable.
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