Design and Analysis of CMOS and CNTFET based Ternary Operators for Scrambling

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1. Introduction

Scrambling is widely used in digital communication systems consisting of transmitting and receiving terminals, and a transmission media. The main target is to encode digital signals by using a scrambler at the transmitter side and decode them by a descrambler at the receiver side. In today’s VLSI design, interconnects complexity became a serious issue. MVL is an alternative to this solution [1]. Ternary logic surpasses binary in terms of higher computational speed since ternary digit (trit) has more information than a binary digit (bit). Now-a-days, ternary logic (or three-valued logic) has attracted due to its advantages over binary logic for designing digital systems. Simple and efficient design, less memory requirement, reduced interconnection complexity, and low product cost [2], reduction in chip area, and implementation of arithmetic and logic functions in a single IC are some of the advantages of MVL. Ternary logic is radix-3 number system which has three logic states, 0, 1 and 2 representing false, intermediate and true, respectively. Many ternary logic circuit models exist in the literature for CMOS technology but are not effective for present high-performance applications. Hence, a new technology (CNTFET) came into existence with better parametric results with low power, delay, and area. Over the past few decades, carbon nanotubes (CNTs) have drawn significant attention in the field of electronics, due to their unique structure and excellent physical properties. In this paper, the comparative analysis between CNTFET and CMOS designs are discussed.

Cryptography plays an important role in telecommunication systems. The general method used to scramble a data stream is the symmetric encryption where the original data stream called plaintext is combined with a keystream to generate an encrypted data, known as ciphertext at the transmitter side. Exclusive-OR (XOR) equivalent to modulo-2 addition is the operator used in binary logic to generate ciphertext.

\[ \text{Plaintext} \oplus \text{keystream} = \text{Ciphertext} \] (1)
\[ \text{Ciphertext} \oplus \text{keystream} = \text{Plaintext} \] (2)

While at the receiver side, the ciphertext is combined with the same key stream using the XOR operator to get plaintext back. All the data streams namely plaintext, keystream, and ciphertext are consequently a sequence of trits \( \epsilon\{0,1,2\} \), (for example, 01221121). A general architecture for cryptography with encryption and decryption steps is shown in Fig. 1 for binary logic.

Moreover, in ternary logic, the operator \( \oplus \) represents mod-3 addition or SUM function in a ternary adder, follows the architecture shown in Fig. 2. The SUM operator is utilized twice to retrieve the original message sent by the sender as shown in Fig. 2. Because of more decoding steps, SUM is not an efficient ternary operator to use in cryptography.

Hence, two scrambling operators (SOP1 and SOP2) are designed in 32-nm Bulk CMOS technology [3] such that they follow the architecture shown in Fig. 1. The operators SOP1 and SOP2 have single encoding and decoding step. For better performance, the operators are proposed in 32-nm CNTFET Technology.
2. Ternary Operators in CNTFET Technology

CNTFET is a three terminal device like MOS, where the semiconducting channel between the two contacts called Source and Drain consists of a Nanotube. Because of high electron mobility, high mechanical and thermal stability of CNTs, CNTFETs are being considered as one of the most promising ones. The representation of voltage levels in unbalanced ternary logic is 0, Vdd/2, Vdd for logic values 0, 1, 2, respectively. There are three representations of ternary inverter namely Negative (-), Positive (+) and Standard and its truth table is mentioned [4]. The positive (negative) ternary inverter takes a path to Vdd (Gnd) when the input is logic ‘1’ where e Vdd and Gnd represent logic ‘2’ and ‘0’, respectively. Let p, q and C be the plaintext, keystream, and Cipher text which consists of trits e{0(1, 2). The CPT1 and SOP2 operators are designed such that they satisfy Eqs. (3) and (4). Moreover, the same is not possible for SUM Eq(5) but it can be applied to cryptography by using operator three times Eq(6) as shown in Table 1. The truth table for a two input ternary function (p, q) for SUM, SOP1 and SOP2 are summarized in Table 2 [3].

\[ \text{SO}_P1(p, q) = C \text{ and } \text{SO}_P1(C, q) = p \]  
\[ \text{SO}_P2(p, q) = C \text{ and } \text{SO}_P2(C, q) = p \]  
\[ \text{SUM}(p, q) = C \text{ and } \text{SUM}(C, q) \neq p \]  
\[ \text{SUM}(p, q) = C \text{ and } \text{SUM}[(\text{SUM}(C, q)), q] = p \]  

| Table 1 Truth table for SUM in Cryptography |
|---------------------------------------------|
| p | q | SUM(p,q) (C) | SUM(C,q) (x) | SUM(x,q) (p) |
|----|----|--------------|---------------|---------------|
| 0  | 0  | 0            | 0             | 0             |
| 0  | 1  | 1            | 2             | 0             |
| 0  | 2  | 2            | 1             | 0             |
| 1  | 0  | 1            | 1             | 1             |
| 1  | 1  | 0            | 2             | 1             |
| 1  | 2  | 0            | 2             | 2             |
| 2  | 0  | 2            | 2             | 2             |
| 2  | 1  | 0            | 1             | 2             |
| 2  | 2  | 1            | 0             | 2             |

| Table 2 Truth table for SUM, SOP1 and SOP2 operators |
|-----------------------------------------------------|
| p | q | SUM | SO_P1 | SO_P2 |
|----|----|-----|-------|-------|
| 0  | 0  | 0   | 0     | 1     |
| 0  | 1  | 1   | 2     | 1     |
| 0  | 2  | 2   | 1     | 0     |
| 1  | 0  | 1   | 1     | 0     |
| 1  | 1  | 0   | 2     | 1     |
| 1  | 2  | 0   | 2     | 2     |
| 2  | 0  | 2   | 2     | 2     |
| 2  | 1  | 0   | 1     | 2     |
| 2  | 2  | 1   | 0     | 2     |

2.1 Transistor-Level Implementation of Ternary Operators

There are several ternary adder designs exists in literature survey [5-8]. The method of ternary circuitry in [7] is used to implement ternary operators in transistor level where the average of (Out +) and (Out –) generates the standard ternary function ‘Out’. The sub-circuits has CMOS binary structures consists of PMOS transistors in Pull-up and NMOS transistors in Pull-down networks that generate the mid-outputs values at Out+ and Out-.

![Fig. 3 Method of ternary circuitry used to design CNTFET [7]](image)

As CNTFET has an excellent current driving capability, a single inverting buffer is enough to strengthen the signal and converts mid-outputs into (Out +) and (Out –). Then, the voltage division takes place to generate the standard ternary function Out as shown in Eq.(7). The fewer times the voltage division, less power dissipates [7]. The method of ternary circuitry used to design CNTFET based ternary operators is shown in Fig. 3.

\[ \text{Out} = \frac{(\text{Out} +) + (\text{Out} -)}{2} \]  

The transistor-level implementation of CNTFET based SUM, SOP1, and SOP2 are depicted in Figs. 6-8. The ternary inputs in Fig. 3 can be Positive Ternary Inverters (PTI) and Negative Ternary Inverters (NTI), used to complement the input variables (p, q). Two Logic One Detectors [8] are also needed to check whether the input variables p, q are ‘1’ or not.

![Fig. 4 Transistor-level and Gate-level implementations of PTI, NTI and Logic One Detector](image)
1 or 2. The mid-outs (for example, \( \text{SUM}^+ \)) and \( \text{SUM}^- \) are binary functions resulting in logic 2 (logic 0), whenever they take a path to the power supply (ground), through a pull-up network (pull-down network).

The ternary expressions are simplified by unifying the literals wherever possible. The terms \( (p^1 + p^2) \) and \( (p^3 + p^4) \) can be replaced by a single transistor \( p^{12} \), respectively. The same unification is not possible for the term \( (p^5 + p^6) \). For \( t^{12} \) \((t^{12}) \), \( t(p,q) \), is represented by a pmnFET (nFET) whose threshold voltage is set properly so that the transistor switches off (switches on) above \( 2V_{dd}/3 \). The ternary expressions are shown in Eqs. (10–21) for SOP1, SOP2 and SUM operators.

For example, in Eq. \((18) \), \( (\text{SUM}^+) \) represents the active paths of replacing inputs with transistors in Fig. 5 with its mid numbers highlighted with red color represents the active paths of replacing inputs with transistors in Fig. 5.

\[
\text{SUM}^+ = p^0q^0 + p^1q^1 + p^2q^2 + p^3q^3 + p^{12},
\]

For the term \( (\text{SUM}^-) \), \( t(p,q) \), is represented by a pmnFET (nFET) whose threshold voltage is set properly so that the transistor switches off (switches on) above \( 2V_{dd}/3 \). The ternary expressions are shown in Eqs. (10–21) for SOP1, SOP2 and SUM operators. 

For example, in Eq. \((18) \), \( (\text{SUM}^+) \) represents the active paths of replacing inputs with transistors in Fig. 5 with its mid numbers highlighted with red color represents the active paths of replacing inputs with transistors in Fig. 5.

\[
\text{SUM}^- = p^0q^0 + p^1q^1 + p^2q^2 + p^3q^3 + p^{12},
\]

Table 3 Truth table of SUM with its mid output values

| p | q | SUM | SUM+ | SUM– |
|---|---|-----|------|------|
| 0 | 0 | 0   | 2    | 0    |
| 0 | 1 | 1   | 2    | 0    |
| 1 | 0 | 1   | 2    | 0    |
| 1 | 1 | 2   | 2    | 2    |
| 0 | 2 | 0   | 2    | 0    |
| 2 | 0 | 2   | 2    | 2    |
| 2 | 1 | 0   | 2    | 2    |
| 2 | 2 | 1   | 2    | 0    |
To provide a comparison between CMOS and CNTFET technologies, the transistor-level implementation of ternary operators in CMOS [3] are simulated with 32 nm bulk CMOS technology at 0.9 V supply voltage. The parameters given in table 6 are utilized to define model files in Predictive technology model [10] for simulation. As the current driving capability of CMOS is weaker, Buffers are supplemented to drive the current. For CNTFET, two buffers are eliminated due to its high current driving capability which leads to a reduction in transistors. The transient response for SOP1 in CMOS and CNTFET is shown in Figs. 9 and 10, with 58 and 50 transistors, respectively.

3. Results and Discussion

All CNTFET circuits are simulated with CNFET compact model [9]. The model parameters for CNFET are provided [7]. The performance parameters are measured in Synopsys HSPICE tool at 0.9 V power supply. The average power for all possible transitions is measured for all circuits. For measuring delay, the fan-out of 4 ternary inverters (TFO4) is considered as output load. The complete input pattern that covers all possible transitions 0 to 1, 1 to 2, 0 to 2, 2 to 1, 1 to 0 and 2 to 0 is fed to the circuit and the maximum is reported as delay value. For a two-input function \((p, q)\) with 9 minterms, there are \(9^2=81\) possible transitions since every single minterm can change into the eight other minterms. For example, the minterm 00 can change into 01, 02, 10, 11, 12, 20, 21, 22. The Power-delay product is the balance between maximum delay and average power calculated (2.2).

\[
\text{Power – Delay Product (PDP)} = \text{Average power} \times \text{Max. Delay (22)}
\]

| \(p\) | \(q\) | \(p\) \(q\) | \(p\) \(q\) | \(p\) \(q\) | \(p\) \(q\) | SOP2+ and its Path(s) | SOP2− and its Path(s) |
|-----|-----|-------|-------|-------|-------|----------------|----------------|
| 0   | 0   | 0     | 0     | 0     | 0     | 2 1 0 8       | 2 1 0 8       |
| 0   | 2   | 2     | 2     | 2     | 2     | 0 2 1 8       | 0 2 1 8       |
| 0   | 2   | 2     | 2     | 2     | 2     | 0 2 1 8       | 0 2 1 8       |
| 1   | 0   | 2     | 0     | 2     | 2     | 2 2 2 6       | 2 2 2 6       |
| 1   | 2   | 2     | 0     | 2     | 2     | 2 2 2 6       | 2 2 2 6       |
| 2   | 0   | 0     | 0     | 2     | 2     | 2 2 2 6       | 2 2 2 6       |
| 2   | 2   | 0     | 0     | 2     | 2     | 2 2 2 6       | 2 2 2 6       |

Fig. 7 Transistor-level implementation of CNTFET based SOP1

Fig. 8 Transistor-level implementation of CNTFET based SOP2

Fig. 9 Transient response of SOP1 in CMOS technology

Fig. 10 Transient response of SOP1 in CNTFET technology

Fig. 11 Transient response of SOP2 in CMOS technology

Fig. 12 Transient response of SOP2 in CNTFET technology

Table 8 Truth table for SOP2 with mid-output values and active path numbers

The transient response for SOP2 in both technologies is shown in Figs. 11 and 12. SOP2 in CMOS [3] design has 52 transistors whereas CNFET design for SOP2 has 44 transistors. Figs. 13 and 14 show the transient response of SUM in CMOS and CNFET designs that has 60 and 52 transistors, respectively.
The average power, delay, PDP, transistor count, total cell width of all operators are compared for CMOS and CNTFET designs as reported in Table 9. By comparing each ternary operator designed with CMOS and CNTFET, the CNTFET designs have better performance. For operators SUM, SOP1 and SOP2, the CNTFET designs have lower power-delay product (PDP) than the operators designed in CMOS. The CNTFET based SOP2 has the least PDP and also it has the lower transistor count and lower cell width. Hence, CNTFET based SOP2 occupies less area in a chip. As it has lower PDP, it is a high-energy efficient ternary operator for scrambling. The total cell width of CNTFET circuit is calculated by considering the sum of each transistor width Eq.(24). The transistor width is calculated by Eq.(23) [7] where \( W_{\text{min}} \) is the minimum width of the gate and \( N \) is the number of nanotubes placed under the transistor gate \( (N = 3) \). By considering Eq.(23), the cell width for each transistor is 60nm. The SOP2 design has the least cell width which intends to decrease in the area of a chip.

\[
W_g = \text{Min}(W_{\text{min}} \times \text{Pitch}) \tag{23}
\]

\[
\text{Total cell width} = \sum \text{width of transistors} \ (W_g) \tag{24}
\]

Fig. 13 Transient response of SUM in CMOS technology

Fig. 14 Transient response of SUM in CNTFET technology

### Table 9

| Operator | Design | Average Power (\( \mu W \)) | Maximum Delay (\( \mu s \)) | PDP (\( fJ \)) | Transistor Count | Total cell width (\( \text{nm} \)) |
|----------|--------|-----------------------------|----------------------------|---------------|-----------------|-------------------|
| SUM      | CMOS   | 1.9659                      | 0.5680                     | 1.1166        | 60              | 7900              |
| SUM      | CNTFET | 0.28458                     | 0.0465845                 | 0.013245      | 52              | 3120              |
| SOP1     | CMOS   | 1.9457                      | 0.4916                     | 0.95655       | 58              | 7824              |
| SOP1     | CNTFET | 0.28203                     | 0.0444696                 | 0.012541      | 50              | 3000              |
| SOP2     | CMOS   | 1.8631                      | 0.5016                     | 0.9345        | 52              | 7232              |
| SOP2     | CNTFET | 0.25039                     | 0.046436                  | 0.011627      | 44              | 2640              |

### 4. Conclusion

The transistor-level designs for CNTFET based Ternary operators, SOP1, SOP2, and SUM, have been proposed in this paper which optimizes the performance metrics with lower power consumption, lesser PDP, reduced transistor count and occupying less area in a chip. They can be used in digital coding in communication systems. A comparative analysis is performed for ternary operators designed with CMOS and CNTFET in 32 nm technology, to conclude the superior technology for ternary circuitry in scrambling applications. In comparison with CMOS, the proposed CNTFET based ternary operators benefit from low power consumption, reduced transistor count and less area. The performance is enhanced because of its excellent current driving capability. The results show that the Power delay product of CNTFETs is less when compared to CMOS designs. The transistor count is reduced from 52 in CMOS to 44 in CNTFET based SOP2. Hence, SOP2 consumes the least area in a chip. CNTFETs are more flexible in adjusting the threshold voltage of transistors by varying the diameter of CNT. This feature makes CNTFET highly appropriate for multi threshold voltage circuitry. The current driving capability of CNTFETs is higher than CMOS. Hence, CNTFETs are the most promising ones in designing the ternary operators for scrambling.

### References

[1] E. Dubrova, Multiple-valued logic in VLSI: Challenges and opportunities, Proc. NORCHIP Conf. 1 (1999) 340-350.
[2] S.L. Hurst, Multiple-valued logic – its status and its future, IEEE Trans. Comput. C 33(2) (1984) 1160-1179.
[3] M.S. Daliri, R. Faghii Mirzaee, K. Navi, N. Bagherzadeh, High-performance ternary operators for scrambling, integration, VLSI Journal 59 (2017) 1-9.
[4] M.H. Moaiyeri, A. Doostaregan, K. Navi, Design of energy-efficient and robust ternary circuits for nanotechnology, IET Circ. Device. Syst. 5(4) (2011) 205-216.
[5] R.F. Mirzaee, M.H. Moaiyeri, M. Maleknejad, K. Navi, O. Hashemipour, Dramatically low-transistor-count high-speed ternary adders, IEEE 43rd Int. Symp. Multiple-Valued Logic 1 (2013) 170-175.
[6] R. Faghii Mirzaee, K. Navi, Optimized adder cells for ternary ripple-carry addition, ICICE Trans. Inf. Syst. E97-D(9) (2014) 2312-2319.
[7] R. Faghii Mirzaee, K. Navi, N. Bagherzadeh, High-efficient circuits for ternary addition, VLSI Des. 2014 1 (2014) 1-15.
[8] S. Rezaie, R. Faghii Mirzaee, K. Navi, O. Hashemipour, From static ternary adders to high-performance race-free dynamic ones, J. Eng. S 2015 1-12.
[9] CNTFET Compact Model, https://nano.standard.edu/Stanford-cntfet-model (Accessed on: 10.05.2018)
[10] Predictive Technology Model (PTM), http://ptm.asu.edu (Accessed on: 10.05.2018).