PERFORMANCE EVALUATION OF SYMMETRICAL AND ASYMMETRICAL CASCADED H – BRIDGES OPERATED WITH MULTICARRIER SINUSOIDAL PWM AND NEAREST LEVEL CONTROL (NLC) TECHNIQUE

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Abstract
Cascaded H – Bridge (CHB) is one of the multilevel inverter topologies which is most used in the medium and high-power applications. To increase the output power and the voltage levels hybrid cascaded H bridges with unequal input voltages have been proposed in the various publications. The number of stages i.e. series connected H -bridges are reduced. It also reduces the distortion and the Electromagnetic Interferences (EMI). The analysis of the hybrid Cascaded H bridges operated with level Shifted (LSPWM), Phase shifted (PSPWM) and Nearest Level Control (NLC) have been studied. Total Harmonic Distortion (THD), fundamental output voltage and the first harmonic spectrum are the performance parameters considered. The comprehensive simulations of three stage CHB, and new hybrid multi-level inverter topologies have been carried out in MATLAB/SIMULINK software.

Keywords
Cascaded H – Bridge (CHB), Hybrid Cascaded Bridge, Sinusoidal Pulse Width Modulation (SPWM), Level Shifted PWM(LSPWM), Phase – Shifted PWM (PSPWM), Nearest Level Control (NLC)

1. Introduction
Multilevel inverters have been established their place in various applications such as HVDC, drives and FACTS controllers etc. They have the advantages such as low THD, low EMI, and reduction in rating of the semiconductor devices over the two – level inverter. The various multilevel inverter topologies have been proposed and discussed in the publications. But very few of them have gained commercial status. The topologies which have been found in commercial use are Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-Bridge (CHB) inverters. The NPC inverter requires more number of diodes for increased levels and the capacitor voltage of NPC inverter cannot be balanced easily. For FC inverter large number of capacitors are required and also balancing of them is critical. The CHB inverter requires a smaller number of components to get the same number of levels in the output voltage as compared to the NPC and FC. And because of its structure it is more suitable to medium and high voltage applications especially high – power medium voltage (MV) drives. It is basically a series connection of the multiple units of H – bridges. And in practice the selection of the number of H -bridges depend on operating voltage and the manufacturing cost. The symmetric and asymmetric hybrid CHB are having equal and unequal input voltages to the series - connected H – bridges [1-2].

The modulation techniques play an important role in the dynamics of CHB inverters. The SPWM voltage applications especially high – power medium voltage (MV) drives. It is basically a series connection of the multiple units of H – bridges. And in practice the selection of the number of H -bridges depend on operating voltage and the manufacturing cost. The symmetric and asymmetric hybrid CHB are having equal and unequal input voltages to the series - connected H – bridges [1-2].

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Elimination (SHE), SHE PWM and space vector etc. have been found in various research publications. The LSPWM, PSPWM and carrier based high switching frequency modulations methods. They are suitable for low and medium power applications [3-4]. The SHE and SHE-PWM can be used for the high-power applications because of having the low switching frequency. But calculations of the switching angles at which the gate pulses are generated of the non linear equations are cumbersome and tedious [5].

Due large switching states space vector , the application of it is limited to the low voltage level [6-7]. Recently, introduced Nearest Level Control (NLC) does not require carrier signals and it is low switching frequency method [8]. Therefore, it is most suitable for high power applications. The application of NLC to the Modular Multilevel Converter (MMC) has been found in publications [9]. But as per best of author’s knowledge, the analysis and applications of LSPWM, PSPWM & NLC to symmetrical and asymmetrical CHB have so far not been found in the existing literature. In this paper, the comprehensive analysis of their applications to the symmetrical and asymmetrical CHB have been carried out.

2. Symmetric H- Bridge
The symmetric topology having the equal input voltages and is called CHB. The fundamental circuit of H-bridge is shown in Fig.1(a) in which the two switches ($S_1$,$S_2$ & $S_3$,$S_4$) of the cross arm are ON at a time gives two levels of the output voltage $+V_{DC}$ and $-V_{DC}$. Redundancy is available for the zero level i.e. it can be generated by switching $S_1$$S_3$ or $S_2$$S_4$ as given in Table 1. The gate pulses for corresponding switches are shown in Fig.1(b). The switches $S_2$ and $S_4$ in the Fig.1(a) are complementary to $S_1$ and $S_3$. The switches can be IGBT, IGCT, which can be turned ON or turned OFF by gate pulse.

A. Cascaded H- Bridge (CHB) [10-11]

Fig. 2 shows the structure of the Cascaded H – bridge. $p$ is the number of stages i.e. number of series connected H – bridges and the associated number of levels in the output phase voltage is $p+1$. In this topology the input voltages of the series connected bridges are equal and is $V_{DC}$. For $p =2$ and $p = 3$ the voltage levels in the output voltage are five and seven levels. Redundancies in the switching sates are available for achieving the different voltage levels. For three stage CHB, three switching combinations for $\pm 2V_{DC}$, six and seven combinations for $\pm V_{DC}$ and 0 levels are available. The redundancies are not shown in the switching tables.

3. Asymmetric cascaded topologies
The input voltages in the asymmetric topologies are unequal. Hybrid, quasi-linear and new hybrid multilevel inverter are considered for the analysis. The number of stages(\(p\)) is the number of H – bridge connected in series. Two H – bridges are connected in series for $p = 2$. Similarly, for three stages $p = 3$ three H -bridge are connected in series.
A. Hybrid multilevel inverters [12-13]

In this topology shown in Fig. 2(b), the input voltages are asymmetrical. For \( p = 2 \) the two input voltages are \( V_{DC} \) and \( 2V_{DC} \). The output phase voltage \( v_{an} \) is \( 3V_{DC} (V_{DC}+2V_{DC}) \). For \( p = 3 \) the output phase voltage is \( 7V_{DC}(V_{DC}+2V_{DC}+4V_{DC}) \). The output phase voltage is having 15 – levels. For \( p = 4 \) stages the output voltage is \( 21V_{DC} \). Table 2 & 3 for \( p = 2 \) & 3.

B. Quasilinear multilevel inverters [14]

Fig. 2(c) show the quasilinear multilevel inverter topology. The input voltages are \( V_{DC} \) and \( 2V_{DC} \) for two stages i.e. \( p = 2 \). The corresponding phase voltage levels 7 - levels. For \( p = 3 \), \( V_{DC}, 2V_{DC} \) & \( 4V_{DC} \) are the input voltages and the corresponding phase voltage are 19 – levels and those are \( \pm 9V_{DC}, \pm 8V_{DC}, \pm 7V_{DC}, \pm 6V_{DC}, \pm 5V_{DC}, \pm 4V_{DC}, \pm 3V_{DC}, \pm 2V_{DC}, \pm V_{DC} \) and 0. For \( p = 4 \) stages the corresponding generated phase voltage levels are \( 2*3^{p-2}V_{DC} \). The switching combinations to generate the particular positive output voltage level is given in Table 2 & 3 for \( p = 2 & 3 \).

C. New hybrid multilevel inverters [15]

New hybrid multilevel inverter topology for the \( p^{th} \) stages is shown in Fig. 2(d). For two stages \( p = 2, V_{DC} \) and \( 3V_{DC} \) are the input voltages to the series connected H – bridges. Similarly, \( V_{DC}, 3V_{DC} \) & \( 9V_{DC} \) are the input voltages to three stages (\( p = 3 \)) circuit and the corresponding phase voltage levels are \( \pm 13V_{DC}, \pm 12V_{DC}, \pm 11V_{DC}, \pm 10V_{DC}, \pm 9V_{DC}, \pm 8V_{DC}, \pm 7V_{DC}, \pm 6V_{DC}, \pm 5V_{DC}, \pm 4V_{DC}, \pm 3V_{DC}, \pm 2V_{DC}, \pm V_{DC}, 0 \). Various switching combinations to generate the particular positive output voltage levels can be found for two and three stages in Table II & III.

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### Table II Switching Combinations for two stages

| Multilevel inverter topology | Input DC voltages | H-bridge output | Output phase voltage | Output levels |
|-----------------------------|-------------------|----------------|---------------------|--------------|
| Cascaded H - Bbridge        | \( V_{DC} \)     | \( V_{DC} \)  | \( 2V_{DC} \)       | 5 - Levels   |
|                             | 0                 | 0              | 0                   |              |
| Hybrid Multilevel inverter  | \( V_{DC} \)     | \( V_{DC} \)  | \( 2V_{DC} \)       | 7 - Levels   |
|                             | 0                 | \( V_{DC} \)  | \( V_{DC} \)       |              |
|                             | \( V_{DC} \)     | 0              | \( V_{DC} \)       |              |
|                             | 0                 | 0              | 0                   |              |
| Quasilinear Multilevel inverter | \( V_{DC} \) | \( V_{DC} \)  | \( 2V_{DC} \)       | 7 - Levels   |
|                             | \( V_{DC} \)     | 0              | \( V_{DC} \)       |              |
|                             | 0                 | \( V_{DC} \)  | \( V_{DC} \)       |              |
| New Hybrid Multilevel inverter | \( V_{DC} \) | \( 3V_{DC} \) | \( 4V_{DC} \)       | 9 - Levels   |
|                             | \( V_{DC} \)     | \( 3V_{DC} \) | \( 4V_{DC} \)       |              |
|                             | 0                 | 0              | 0                   |              |

### Table II Switching Combinations for three stages

| Multilevel inverter topology | Input DC voltages | H-bridge output | Output phase voltage | Output levels |
|-----------------------------|-------------------|----------------|---------------------|--------------|
| Cascaded H - Bbridge        | \( V_{DC} \)     | \( V_{DC} \)  | \( 2V_{DC} \)       | 7 - Levels   |
|                             | \( V_{DC} \)     | 0              | \( V_{DC} \)       |              |
|                             | \( V_{DC} \)     | \( V_{DC} \)  | \( 2V_{DC} \)       |              |
| Hybrid Multilevel inverter  | \( V_{DC} \)     | \( 2V_{DC} \) | \( 4V_{DC} \)       | 15 - Levels  |
|                             | \( V_{DC} \)     | \( 2V_{DC} \) | \( 4V_{DC} \)       |              |
|                             | \( V_{DC} \)     | 0              | \( 4V_{DC} \)       |              |
|                             | \( V_{DC} \)     | \( 2V_{DC} \) | \( 4V_{DC} \)       |              |
|                             | \( V_{DC} \)     | \( 2V_{DC} \) | \( 4V_{DC} \)       |              |
| Quasilinear Multilevel inverter | \( V_{DC} \) | \( 2V_{DC} \) | \( 6V_{DC} \)       | 19 - Levels  |
|                             | \( V_{DC} \)     | \( 2V_{DC} \) | \( 6V_{DC} \)       |              |
|                             | \( V_{DC} \)     | \( 2V_{DC} \) | \( 6V_{DC} \)       |              |
|                             | \( V_{DC} \)     | \( 2V_{DC} \) | \( 6V_{DC} \)       |              |
| New Hybrid Multilevel inverter | \( V_{DC} \) | \( 3V_{DC} \) | \( 9V_{DC} \)       | 27 - Levels  |
|                             | \( V_{DC} \)     | \( 3V_{DC} \) | \( 9V_{DC} \)       |              |
|                             | \( V_{DC} \)     | \( 3V_{DC} \) | \( 9V_{DC} \)       |              |
|                             | \( V_{DC} \)     | \( 3V_{DC} \) | \( 9V_{DC} \)       |              |

**Table IV. Simulation Parameters**

| Parameters                  | LSPWM & PSPWM | NLC |
|-----------------------------|---------------|-----|
| Input DC voltage \( V_{DC} \) | \( 11/2kV \) | \( 11/2kV \) |
| Line frequency \( f_{r} \)   | \( 50Hz \)   | \( 50Hz \)   |
| Carrier frequency \( f_{c} \) | \( 1550Hz \) | NA    |
| Sampling frequency \( f_{s} \) | \( 100kHz \) | \( 100kHz \) |
| Load resistance \( R_{L} \)   | \( 22.1\Omega \) | \( 22.1\Omega \) |
| Load inductance \( L \)       | \( 79.53\,mH \) | \( 79.53\,mH \) |
| Power factor \( \cos(\phi) \) | 0.9 lag       | 0.9 lag   |

**NA – Not applicable**

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4. Level Shifted PWM (LSPWM)

In this modulation method the carrier and the modulation or reference waveforms are required. Carriers are shifted by the amplitude determined by the number of levels. \( N \) is the number of voltage levels. Total \( N-1 \) carriers are required with same amplitude and frequency. The modulating or reference waveform is a sinusoidal waveform with the fundamental frequency 50Hz. The gate pulses are generated by comparing the modulating with the carrier waveforms. The amplitude of the carrier and the modulating waveform are determined from the modulation index which are defined by Table III. The principle is explained in the Fig. 3(a). If all the carriers are in phase is called the phase disposition (PD). In Phase Opposition Disposition (POD) all the carriers above the zero are in phase and in opposition with the carriers below the zero. If all the carriers are alternatively in opposition is called the Alternate Phase Opposition Disposition (APOD) [3]. Fig. 3 (b), (c) & (d) show the PD, POD and APOD schemes. The inverter switching frequency is given as

\[
f_{\text{inv}} = f_c
\]

And the device switching frequency is as follows

\[
f_d = \frac{f_c}{m-1}
\]

![Fig. 3 LSPWM (a) Principle (b) PD (c) POD (d) APOD](image)

![Fig. 4 Principle of PSPWM](image)

![Fig. 5 Principle of NLC](image)
5. Phase Shifted PWM (PSPWM)

Here the carriers are shifted by the phase angle. The principle is shown in the Fig. 4. The phase shift between any two carriers is \( \frac{360^\circ}{(N-1)} \). The amplitude of the carrier and the modulating waveform is same i.e. between the +1 and -1. The gate pulses are generated by comparing the modulating with the carrier waveforms. The modulation index is given in the Table I. The switching frequency of the inverter is given by [7]

\[
 f_{\text{inv}} = (N-1)f_d = (N-1)m_f \times f_m
\]

And the device switching frequency is as follows

\[
 f_d = f_c = m_f \times f_m
\]

6. Simulation results

Simulation parameters are listed in the Table IV. Fig.6 & 7 show the phase voltages \( v_{an} \) and the corresponding harmonic spectrum for the CHB, and new hybrid multilevel inverters. The three stage, \( p = 3 \) are taken for simulation. In CHB the three inputs are equal i.e. \( V_{DC} = 11/\sqrt{2} = 7.78 \text{kV} \). The peak output is expected at \( (V_{DC} + V_{DC} + V_{DC}) = 23.34 \text{kV} \) and is shown in the Fig. 6(a), (c), & (e). Fig. 7 shows the output voltage for new hybrid multilevel inverter topology with \( p = 3 \) modulated by LSPWM, PSPWM, & NLC. The three input voltages are \( V_{DC} \), \( 3V_{DC} \) & \( 9V_{DC} \). The peak output voltage is \( 13V_{DC} \) i.e. 101.14 kV and is shown in the Fig. 6(a), (c), & (e).

Nearest Level Control (NLC)

NLC is also known as round method. The three phases are controlled independently by having 120° phase differences in the reference waveforms. The closest voltage level is used to normalise the reference waveform \( v_r \) and is given by

\[
 \text{Closest voltage level} = v_{an} = V_{DC} \times \text{round}\[
\]

Where \( V_{DC} \) is difference between the two levels. The
Fig. 7 & 8 show the total harmonics distortion of phase voltage and current for CHB and the new hybrid multilevel inverter for 7 & 27 levels. It also shows the peak fundamental voltage. The THD is less for the greater number of levels. For higher modulation index, the THD of voltage and current are less. In NLC technique the harmonic spectrum is not defined and low order harmonics appear with large amplitudes.

7. Conclusion

Three stage CHB and new hybrid multilevel inverter operated with LSPWM, PSPWM and NLC have been simulated comprehensively in MATLAB/SIMULINK software. The effective frequency of the inverter in the LSPWM is equal to the carrier frequency while it is depended on voltage levels in the PSPWM. Therefore, the first harmonic in the PSPWM for the same frequency is shifted to high order. NLC does not have the defined harmonic spectrum and hence low order harmonics present in the output voltage and current. In new hybrid multilevel inverter, the output voltage levels are highest compared to the CHB, quasilinear and hybrid multilevel inverter topologies. This paper may find useful in knowing the modulations methods for low, medium and high-power cascaded bridge applications.

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