Util::Lookup: Exploiting key decoding in cryptographic libraries

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ABSTRACT
Implementations of cryptographic libraries have been scrutinized for secret-dependent execution behavior exploitable by microarchitectural side-channel attacks. To prevent unintended leakages, most libraries moved to constant-time implementations of cryptographic primitives. There have also been efforts to certify libraries for use in sensitive areas, like Microsoft CNG and Botan, with specific attention to leakage behavior.

In this work, we show that a common oversight in these libraries is the existence of utility functions, which handle and thus possibly leak confidential information. We analyze the exploitability of base64 decoding functions across several widely used cryptographic libraries. Base64 decoding is used when loading keys stored in PEM format. We show that these functions by themselves leak sufficient information even if libraries are executed in trusted execution environments. In fact, we show that recent countermeasures to transient execution attacks such as LVI ease the exploitability of the observed faint leakages, allowing us to robustly infer sufficient information about RSA private keys with a single trace. We present a complete attack, including a broad library analysis, a high-resolution last level cache attack on SGX enclaves, and a fully parallelized implementation of the extend-and-prune approach that allows a complete key recovery at medium costs.

1 INTRODUCTION
Due to the widespread adoption of cloud-computing and virtual machines, architectural and microarchitectural attacks exploiting shared resources have become a major concern for security-critical applications [1–3]. Within the last decade, these attacks have seen great advances [4–7], culminating in jeopardizing the security of trusted execution environments, cloud computing, and finally revealing transient execution bugs in all modern processors [8–11].

A popular target of these attacks are cryptographic implementations, as they contain critical information that is both compact and used for extensive and often highly optimized computations. As a result, cryptographic implementations have been analyzed for exploitable code behavior that leaks information in great detail. This task has been significantly eased by the development of more automated analysis techniques, which are offered by tools like CacheAudit [12], DATA [13] or Microwalk [14]. In fact, recent studies have identified remaining exploitable code sections in cryptographic implementations, with increasingly small leakages [7, 15–17] and have resulted in a long stream of CVEs for these libraries. These remaining leakages are getting smaller and more difficult to find due to the vast effort that went into the analysis. Some libraries have even been certified for secure implementation and design: Microsoft Cryptography API: Next Generation (CNG) is periodically FIPS-validated [18]; Botan has been extensively audited to be resistant against common side-channel attacks, and is thus authorized for use in sensitive applications [19].

At the same time, Intel has released numerous mitigations for transient execution bugs which significantly altered the efficacy of microarchitectural attacks, in particular in highly protected environments such as Intel Software Guard Extensions (SGX). Countermeasures to Foreshadow [10], also known as L1 Terminal Fault, now prevent L1 Cache attacks on SGX [20], while attacks exploiting Simultaneous Multithreading (SMT) should be prevented by enclave developers ensuring operation on private cores.

1.1 Our Contribution
In this work, we show that despite the increasingly rigorous analysis of cryptographic libraries, microarchitectural attacks are still a threat. Our analysis finds that remaining issues are not in the cryptographic routines that have been extensively analyzed by other publications. Instead, we investigate utility functions, which are a vital part of cryptographic libraries, but have thus far been ignored in most studies. Clearly, these functions compute on sensitive data and are thus potential subject to information leakage.

In particular, we focus on functionality that decodes secret keys from a format suitable for storage and converts them into binary data used at runtime. We show how such a functionality can be exploited via a faint last level cache (LLC) leakage.

More concretely, we investigate RSA keys that are stored in the popular PEM format, which uses base64 to encode binary data in printable characters. The decoded information is later processed in the constant-time cryptographic implementations of the library.

Usually, the leakage of the decoding process is quite faint and extremely difficult to exploit: Subsequent table accesses during decoding are only few instructions apart and will be executed out-of-order, resulting in extremely high noise, while featuring only minimal leakage to begin with. In fact, even a powerful attack that combines
three different microarchitectural attack techniques, the page fault side channel [21], the single-stepping of SGX-step [22], and a last-level cache attack for spatial resolution of cache accesses [2] has problems to distinguish two close cache hits in the LLC due to the noise. Thus, other studies which already noticed such leakages in key decoding [13] ignored these findings, likely because they were not deemed exploitable, and the vulnerable code remained unfixed.

Many of the recent microcode updates render side-channel attacks on SGX more difficult, in particular by flushing the L1 data cache and reflecting the SMT state in the attestation. However, it turns out that the recent mitigation against Load Value Injection (LVI) and the resulting serialization of memory accesses in SGX enclaves enables us to sample the decoding with significantly reduced noise and to obtain almost error-free leakage, even from a single key loading event. To practically exploit the observed leakages, we make use of state-of-the-art cryptanalytic methods.

In summary our contributions are:

- Fine-grained leakage analysis of the base64 decoding functions for several common crypto libraries, including the certified Botan library.
- A sophisticated microarchitectural attack that manages to extract the observed leakages from SGX enclaves with a single observation, in spite of and because of the microcode and countermeasures introduced by Intel in response to transient execution attacks.
- An optimized RSA key recovery method including a highly scalable implementation that, given medium resources, allows to reconstruct the key from very weak leakages of 5 of the 6 redundant key parameters commonly used for RSA key storage, as well as a thorough performance analysis.

We plan to publish the complete code of our attack.

1.2 Responsible Disclosure

We have informed the maintainers of all studied libraries about our findings in December 2020.

- Botan: CVE-2021-24115, fixed with version 2.17.3
- GNU Nettle: No response, not yet fixed
- mbedTLS: CVE-2021-24119, fixed with version 2.26.0
- MS CryptoAPI: Declared as not urgent
- NSS: Not yet fixed
- OpenSSL: No response, not yet fixed
- RustSGX: CVE-2021-24117, pending fix
- wolfSSL: CVE-2021-24116, fixed with version 4.6.0

2 BACKGROUND

2.1 Microarchitectural Attacks

A common approach in microarchitectural attacks is the exploitation of contention in microarchitectural buffers within the CPU, which are intended to improve performance. The usually unprivileged attacker manipulates the content of a buffer or cache to provoke abnormal behavior, which can be measured as side-channel information like timing behavior, and leak secrets partially.

2.1.1 Cache attacks. A frequent target are CPU caches, from the core-specific L1 caches [4, 23], to the unified, inclusive and shared L3 caches [2, 5]. Many techniques evolved, allowing the adversary to measure timing differences regarding data or instruction accesses [6, 24–26], in order to determine whether the victim code accessed a certain cache line.

Intel’s processors have a set-associative cache layout, where each 64-byte cache line maps into a specific cache set. Each cache set has a limited number of ways, which is the number of cache lines it can contain at any time. The cache sets of the L3 cache are divided into slices, where the number of slices usually corresponds to the number of logical cores. The mapping of physical address to slices is computed by an undocumented hash function.

Prime+Probe [24] determines a victim’s cache access by first priming a complete cache set with attacker values, the so-called eviction set, then waiting on the victim’s code execution and finally probing the complete cache set with the same attacker values. If the probing access time is below a threshold, all attacker values were served from the cache and the victim did not access the data of interest. Otherwise, if the access time is above that threshold, the victim accessed data that was mapped to the same cache set and thus evicted some of the attacker’s values. Unlike Flush+Reload [6], this procedure does not require any shared memory, but it is less precise and prone to noise, since a complete set is probed instead of a single cache line. When attacking the sliced L3 cache, it is advisable to use one eviction set per slice, to reduce noise caused by the remaining system and its processes. Prime+Probe first requires to construct eviction set(s), meaning finding csize addresses which map to the cache set that is to be primed, where csize specifies the size of a cache set. Depending on the attacker model, this can be done using virtual to physical address translation, or through huge pages usually giving the attacker control over the cache set index bits [2, 27]. Constructing eviction sets per slice does not require the knowledge of the address to slice mapping. Instead they can be derived incrementally from the cache set’s eviction set [2].

2.1.2 Vulnerability Detection. Finding side-channel vulnerabilities in programs by manually inspecting high level and assembly code is a cumbersome task and will reveal only a small portion of vulnerabilities, and has to be repeated each time the code was changed.

Automated vulnerability finding can assist in this endeavor. One approach to this end is to leverage dynamic binary instrumentation and analysis combined with input fuzzing, as done by DATA [13] and Microwalk [14]. These frameworks find non-constant-time behavior by instrumenting a piece of code under test and executing it multiple times with different inputs (secrets), while recording the execution traces. Deviations between traces suggest secret dependent behavior. The tools quantify the leakages by calculating the mutual information between input and observed traces.

There also are different approaches like e. g. CacheAudit [12], which applies static analysis to find cache side channels.

2.2 Intel SGX

Running security relevant software or algorithms processing confidential data in untrusted environments has become quite common. Intel Software Guard Extensions (SGX) aims to provide a hardware root of trust, enabling users to run software in isolated environments, called enclaves, which can perform confidential computations in the presence of an untrusted operating system (OS) without
leaking secret information [28, 29]. To allow the application developer to verify the integrity and security of their application, Intel SGX supports two remote attestation schemes [30, 31].

2.2.1 Memory management. Intel SGX leaves the memory management to the OS, which is responsible for allocating memory and mapping physical to virtual memory addresses. This allows untrusted software to tamper with page table entry (PTE) meta information like the PTE accessed bit [22]. However, Intel SGX specifically guarantees integrity and confidentiality of the data in RAM. All data in RAM is protected by memory encryption [32] and kept in the Enclave Page Cache Map (EPCM), which is inaccessible from outside SGX. To counteract manipulations of the address translation, SGX keeps track of all EPC memory pages including their expected virtual address in the Enclave Page Cache Map (EPCM) [33].

2.2.2 Context switches. Programs running in Intel SGX are subject to context switches as any other process. Since enclaves are isolated from the remaining system, context switch require dedicated instructions provided by SGX [29, 33]. After an enclave was created with the ECREATE instruction, it can be entered with EENTER. In case the processor is interrupted while in enclave mode, SGX ensures that Asynchronous Enclave Exit (AEX) is executed, storing the execution state to a secure area and cleaning up the registers. Additionally, the instruction pointer is set to the Asynchronous Exit handler Pointer (AEP), causing the system’s interrupt handler to return to AEP when it finishes. Finally, ERESUME can be called from the asynchronous exit handler to resume execution of the enclave.

2.2.3 Attacks on Intel SGX. Trusted execution environments like Intel SGX feature an attacker model which assumes an untrusted OS, and thus enables adversaries to tamper with all system resources to extract information from isolated enclaves.

Amplifying side-channels with control over system events and resources, such as page faults or interrupts, and using this to reduce noise, is called a controlled-channel attack [21].

SGX-Step [22] introduced a framework for controlled-channel attacks on SGX, which was used in many subsequent attacks [7, 11, 34, 35]. It enables the attacker to single step enclaves and to manipulate page table entries in order to get insight into the control flow.

Transient execution attacks on SGX [10, 11, 36–38] have forced Intel to publish microcode and software mitigations. One countermeasure pushed via microcode updates is to flush microarchitectural buffers such as the L1 data cache upon enclave exit [20]. In addition, compilers now insert fences in enclave code to prevent Spectre-like attacks. Furthermore, disabling simultaneous multithreading is recommended when executing enclaves. In addition to transient execution attacks and controlled-channel attacks, other vulnerabilities were found targeting e.g. the cache [39, 40] or the branch history [41].

2.3 RSA Key recovery

Recovering the complete RSA key from partial information has been studied in numerous settings. In theory, it is sufficient to store only one of the primes \( p \) or \( q \) as private key, but this is very inefficient. To speed up the decryption of messages via the Chinese Remainder Theorem (CRT), \( all \) of the values \( (p, q, d, d_p, d_q, q_p^{-1}) \) are stored, where \( d_p := d \mod p - 1 \), \( d_q := d \mod q - 1 \), and \( (q_p^{-1} - q) \mod p = 1 \). Note that the knowledge of any single of these variables is sufficient to reconstruct all other variables, given the public key \((N, e)\) [42].

There are roughly two kinds of partial information that are obtained by side-channel attacks: consecutive information and non-consecutive information. In the consecutive case, the attacker obtains a number of consecutive blocks of information about some of the variables, e.g. the \( (p) \) or \( q \) most significant bits of \( p \), where \( (p) \) is the encoding length of \( p \), i.e. \( (p) := \lceil \log_2(p + 1) \rceil \) or the \( (p) \) least significant bits of \( p \) and the \( (q) \) least significant bits of \( q \). This continuity gives a high amount of structured information, which allows an attacker to mount attacks based on lattices. For the many applications of this technique to reconstruct parts of the private key, we refer to the surveys [43–45]. This technique was also used in a recent work to recover RSA keys [46], where the authors were able to obtain partial leakages of \( q \) on consecutive positions and could use this information to derive \( q \) completely.

In the non-consecutive case, the information is widely spread over the variables.

A widely used algorithm for this case was presented by Heninger and Shacham and subsequently generalized by Henecka et al. and Paterson et al. [42, 47, 48]. In a naive fashion, one could try to construct a search tree that aims to test all possibilities for the different unknown variables, which gives a solution space of \( 2^m \). Whenever a candidate is encountered that does not fit to the partial known information, we can prune this candidate. The main idea of Heninger and Shacham is to use the different dependencies between the variables to set up an equation system containing \( 4 \) equations and \( 5 \) variables, which drastically reduces the solution space to \( 2^m \).

Given sufficient information from side-channel attacks can then be used to further reduce this space. This approach was used for many attacks, e.g. [49–52]. In all variations of the algorithm, the partial information contains information on a bit-wise level, while our attack works on information about blocks of bits. We thus adapt the algorithm of Heninger and Shacham to this setting in Section 5.

3 EXPLOITING KEY DECODING

In this section we analyze possible leakages in the key decoding routines of various cryptographic libraries. First, we describe the Privacy-enhanced Electronic Mail (PEM) format, which is used for storing and exchanging cryptographic material, and is supported by many common cryptographic implementations. We use the Microwalk [14] framework to conduct a broad analysis of several popular libraries, including OpenSSL [53], wolfSSL [54], NSS [55], and Botan [56] in order to find and assess possible leakages in key decoding. Microsoft CNG itself does not offer native key decoding, and offloads this onto the user; however, its largely deprecated predecessor Microsoft Crypto API [57] is still included in recent Windows versions, and supports loading and storing PEM formatted keys. WolfSSL, RustSGX [58] and mbedTLS [59] offer native SGX support, and with TaLoS [60] there also is an SGX mode for OpenSSL. Finally, we analyze Microwalk’s findings and show that lookup table (LUT)-based base64 decoding poses a significant and widespread source of leakage, which we exploit to infer the entire private key in Sections 4 and 5.
3.1 Storing Cryptographic Material

Storage formats for cryptographic data face several challenges: The format should be standardized, such that it can be exchanged between different implementations without compatibility issues. Then, fingerprints of keys and certificates should be unambiguous, i.e., there shouldn’t be two equivalent representations of the same cryptographic entity. Finally, while not a hard requirement, the format should be easily usable in practice, to allow transferring cryptographic data without worrying about encoding issues.

3.1.1 PEM Format. To accomplish this, RSA private keys are commonly stored in PKCS #8 format [61], which is specified in Abstract Syntax Notation One (ASN.1) interface description language [62] and uses the Distinguished Encoding Rules (DER) encoding to generate a unique binary representation for cryptographic data. This encoding is defined in such a way that it is ensured that the same key material always yields the same binary data. Listing 9 in the appendix shows an example 1024-bit RSA private key in ASN.1 format, encoded with DER. Data encoded with DER can be encrypted using a symmetric algorithm and wrapped into another DER layer, to protect it in case the key file gets stolen; however, for server deployments, the same applies for the used passphrase, which usually is stored next to the encrypted key file, limiting the security benefit. For this reason, unencrypted key files are still prevalent.

Finally, in order to allow easy handling and transmission over non-binary channels, the binary DER data is base64 encoded and complemented with start and end markers, which denote the semantics of the base64-encoded payload, and allow implementations to easily determine the correct decoding technique. These markers also allow to store multiple entities in one file, e.g., certificate files, containing certificates of an entire chain. These files are usually referred to as PEM format.

3.1.2 Encoded RSA Private Keys: An RSA private key typically consists of the public parameters $N$ and $e$, as well as the private parameter $d$. These values are sufficient for decrypting and signing messages. For better performance, many implementations utilize the CRT, which additionally requires the primes $p$ and $q$, and three parameters $d_p = d \mod (p - 1)$, $d_q = d \mod (q - 1)$ and $q_{\text{inv}} = q^{-1} \mod p$.

3.2 Finding Leaks

3.2.1 Leakage Detection. In order to avoid time-consuming and error-prone manual analysis, we utilized the Microwalk [14] framework to automatically analyze the key decoding of several major cryptographic libraries, and infer possibly interesting leakages. This approach has the advantage that we can focus on the code sections which actually do behave differently depending on the secret input (and thus may leak), and it also finds very subtle leakages often missed when doing manual analysis, but exploitable nonetheless.

Since Microwalk relies on dynamic instrumentation, we randomly generated a set of 4,096 private key PEM files with slightly varying parameter sizes, and traced the key decoding of each library. We then instructed the analysis module to compute the amount of leaked bits per memory accessing instruction. After Microwalk had generated and analyzed the traces for each test case, we manually removed false positives like subtle variations in the memory allocator and reports relating to cryptographic operations, and sorted the results by their estimated severity.

For OpenSSL, the resulting leakage candidates were all related to decoding the private key. Functions prefixed with the string EVP were assigned the highest possible leakage estimation: The EVP_DecodeUpdate method does an initial scan of the entire input string, in order to determine its length and remove invalid characters, and then passes it to the EVP_DecodeBlock method, which performs a LUT-based base64 decoding of the input. Another notable leakage is the Bn_bin2bn function, which converts the decoded key parameters into big number objects: It loops over the currently processed parameter, and thus leaks its length. Detailed analysis results for OpenSSL are listed in Table 5 in the appendix. We continue with explaining and discussing these leakages in detail.

3.3 Analysis of Key Decoding Techniques

3.3.1 Decoding of PEM Files. When loading the private key, cryptographic libraries parse the PEM file, decode the base64 DER, and convert the binary DER representation into an internal format. For those libraries that employ a lookup table (LUT)-based approach, we found that in each analyzed library this process leaks key information for every base64 character, and thus every parameter stored in the key file.

All libraries roughly follow the same high-level approach: First, they parse the start/end markers to locate the base64-encoded payload. Then, they decode each base64-character and reconstruct the underlying binary data, while skipping invalid characters like line breaks and spaces. Finally, the DER container is handed to the next decoder stage, which parses the DER blocks following the ASN.1 specification, and initializes a corresponding private key object.

3.3.2 Leaks in base64 Decoding. In base64 encoding, the binary data is divided into 6-bit chunks, interpreted as alphanumeric characters, the plus sign or the slash, making up 64 distinct characters, all from the ASCII character set.

For decoding, these characters are converted back into 6-bit chunks, where each group of four chunks corresponds to 3 bytes of binary data. While this conversion can be realized as a case decision, most implementations rely on LUTs, where each ASCII character maps to the corresponding 6-bit chunk (or an invalid value). Since an ASCII-encoded character takes up 7 bits, the LUTs need to have at least 128 entries. Listing 1 shows the decoding table used by OpenSSL. Note that due to its length, the table takes up at least two 64-byte cache lines, which allows an attacker to infer a part of the table index through a cache attack, as we will show in Section 4. While all analyzed libraries use a LUT-based base64-decoding, the exact implementations vary in detail: For example, OpenSSL and NSS parse the base64 string twice, to handle invalid or white space characters, and determine the length of the resulting decoded binary string. This allows the attacker to do multiple measurements per input, which reduces the measurement error.

Another difference between the libraries and even between different configurations of a single library is the alignment of the base64 LUT. If a 128-byte LUT is aligned at a cache line boundary
Due to the memory constraints, the standard 64-byte and 32-byte alignments, except for libraries compiled with potentially higher leakage. In our experiments, we mostly observed alignment is not at a cache line boundary, but within a cache line, cache line increases, making up for an overall smaller leakage. If the character; however, at the same time, the entropy for the denser cache line decreases, making it easier to infer the respective base64 one bit of each base64 character by observing the accessed cache line. Finally, the cache lines which contain a part of the LUT. The probability for base64 decoding.

| 0x08 | ff000000 00000000 | # TAB LF CR |
| 0x10 | ff000000 00000000 | |
| 0x18 | ff000000 00000000 | |
| 0x28 | 00000000 00000000 | # SPACE |
| 0x28 | ff000000 00000000 | |
| 0x30 | 32222222 22222222 | # + - / |
| 0x38 | 11111111 11111111 | # TAB LF CR |
| 0x40 | ff000000 00000000 | |
| 0x48 | 00000000 00000000 | |
| 0x50 | 00000000 00000000 | |
| 0x58 | 00000000 00000000 | |
| 0x60 | 00000000 00000000 | |
| 0x68 | 00000000 00000000 | |
| 0x70 | 00000000 00000000 | |
| 0x78 | 00000000 00000000 | |

Figure 1: base64-decoding lookup table as present in the OpenSSL binary. The comment column on the right lists the ASCII representations of valid code points (non-0xFF bytes).

(64 bytes), it takes up exactly two cache lines. As depicted in Listing 1, the LUT entries are not evenly distributed: Considering only the base64 character set, the first half has 12 entries, while the second half has 52, so observing an access to the first cache line yields more information than an access to the second one. However, if the LUT is aligned at 32 bytes, the entries are split over three cache lines: The first one does not have any base64 entry, the second has 38, and the third has 26.

To measure the average information that is leaked by a LUT access when observed at cache line level, we compare the number of base64 entries per cache line. Let random variable $B$ denote the 64 possible base64 characters, where each character $b$ has the same probability: $Pr[B = b] = \frac{1}{64}$. Also, let random variable $C$ denote the cache lines which contain a part of the LUT. The probability that we observe a certain cache line $c$ is thus $Pr[C = c]$, which equals the fraction of base64 characters which map to this cache line. Finally, $Pr[B = b | C = c]$ denotes the probability of a certain base64 character $b$ if we observed cache line $c$.

We can then compute the average information $I(B,C) = H(B) - H(B | C)$ leaked by observing a cache line, where $H$ denotes the Shannon-entropy.

Table 1 shows the investigated libraries and the expected leakage for base64 decoding.

Note that the amount of leaked information depends on the structure and the alignment of the LUT: If the LUT takes up two cache lines and the base64 character entries are distributed evenly, so $Pr[C = c] = \frac{1}{3}$ and $Pr[B = b | C = c] = \frac{1}{64}$, we see the maximum possible leakage value of $I(B,C) = 1$, which means that we learn one bit of each base64 character by observing the accessed cache line. If the table is not evenly distributed, the entropy for the sparser cache line decreases, making it easier to infer the respective base64 character; however, at the same time, the entropy for the denser cache line increases, making up for an overall smaller leakage. If the alignment is not at a cache line boundary, but within a cache line, the table may spread over more than two cache lines, leading to a potentially higher leakage. In our experiments, we mostly observed 64 byte and 32 byte alignments, except for libraries compiled with the SGX framework: Due to the memory constraints, the standard Makefiles enable optimization for space (~0s in GCC), which reduces the table alignment down to 1 byte. While the leaked information per base64 character is rather small and capped at one bit, the redundancy imposed by storing multiple secret key parameters makes up for this, as we show in Section 5.

Non-LUT-based base64 decoding: Another approach for base64 decoding is treating each case separately: Most characters (letters and numbers) are ASCII-encoded in contiguous chunks, with only few exceptions. Thus, one can test whether the current character is in a specific interval, and then simply add/subtract a certain constant which then yields the associated 6-bit value. This approach has, e.g., been used by BoringSSL [64] and the Rust base64 package, although the latter has since moved to a LUT-based implementation.

Depending on the binary layout of the code handling each case, an attacker may be able to acquire much more fine-grained information about each character than in a LUT-based attack: If they can distinguish each case, which may be possible by counting the number of executed instructions per loop iteration, they learn whether the current character is an upper- or lower-case letter, a number, or a special symbol. This corresponds to more than 1 bit of information, even higher than the leakage induced by LUT-based decoding.

3.3.3 Exploiting the DER Format. Even though the majority of the detected leakages are found in the base64 decoder, we also identified subtle secret-dependent computations in the DER decoder and the big number initialization. In DER, the parameters are not stored directly next to each other, but have a prefix denoting their type (integer, 02) and byte length (see Listing 9 in the appendix). Since base64 encoding divides the payload into 6-bit chunks, some chunks may contain bits from both a secret parameter and a byte belonging to DER formatting. If this DER byte is known to an attacker, they can reduce the remaining uncertainty from detecting the corresponding LUT cache line, and infer up to 4 bits of the first or last secret parameter byte. While the parameter type byte is constant, the length byte is not; however, an attacker can learn the length of the parameter through other leakages, like in cases where a parameter is copied when initializing a big number object: In order to speed up arithmetic operations, many big number implementations divide their state into 64-bit integer chunks, which are initialized by copying the number bytes using bitwise operations like shifts and OR. The attacker can then simply count the number of loop iterations and thus learn the parameter length, if the loop is not constant-time.

4 CACHE ATTACK ON INTEL SGX ENCLAVE

Attacking a simple lookup procedure, which mainly involves memory loads executed in a very short time frame, requires a high temporal attack resolution or a slowed down victim process. Thus, we attack the base64 decoding process of RSA keys in an Intel SGX enclave, which allows us to analyze the decoding process on a per-instruction basis. The attack we implemented is specific to the way OpenSSL implements the decoding of base64 keys into its internal data format, especially the offline analysis part which leverages OpenSSL’s access pattern to the LUT. However, the translation from base64 to binary by means of a LUT is a recurring pattern
in all of the libraries shown in Table 1. Thus, the general attack scheme is applicable to other libraries as well.

In short, our attack on the base64 LUT-based decoding process of RSA keys consists of several steps. First, we run OpenSSL’s key decoding in an SGX enclave and execute it in a controlled, single-stepped fashion, where the corresponding memory page accesses to the LUT and decoding function are tracked. We combine the page access monitoring with a classic Prime+Probe attack on the LLC to track which cache line of the decoding table is accessed when the investigated code is executed. The resulting trace is then processed during an offline analysis step, which outputs a cache line access pattern with the same length as the original base64 string in the PEM file holding the private key.

We first run the attack without mitigation against recent transient execution attacks like LVI [11] and obtain mostly negative results. However, as we show in this section, running the same experiments with enabled mitigation drastically reduces noise in the measurements, which allows to reliably extract all information introduced by non-constant time behavior in the base64 decoding.

4.1 Attack description

4.1.1 Attacker model. Intel SGX aims to protect programs by running them in enclaves isolated by special hardware mechanisms. Ultimately, it allows enclaves to be guarded from a malicious OS and otherwise rogue software environments and system administrators as long as the authenticity and integrity of the enclave and SGX instance are verified by attestation [29, 30, 33]. Consequently, attacking a process running in a protected enclave assumes an attacker with system level privileges having full control over the OS kernel and the system BIOS. They are capable of translating virtual to physical addresses, manipulating page access bits and setting timed interrupts using the APIC timer. Additionally, they have access to the program’s binary and control the unprotected application part. By using the SGX-Step framework [22], the enclave can be single-stepped.

4.1.2 Cache Attack. For our cache attack, we use Prime+Probe with eviction sets. After the discovery of Foreshadow [10], Intel published a microcode fix which conducts an L1 cache flush on every enclave exit, so we are restricted to attacking the L3 cache.

4.1.3 Attack process. Figure 2 shows an overview of the attack process on base64 decoding in Intel SGX. We start with initializing the victim’s enclave (#1) and constructing eviction sets (#2) for every cache set possibly containing the cache lines holding the lookup table. Since the last level cache is divided into slices, the number of required eviction sets is determined by the number of cache lines occupied by the LUT times the number of slices. To construct the eviction sets, we implement an algorithm similar to the procedure presented by Liu et al. [2] using virtual to physical address translation. After constructing the eviction sets, we use SGX-Step to configure APIC timer interrupts which allow us to single step code running in the enclave (#3) and subsequently trigger the base64 decoding (#4).

Next, we enter the enclave with the EENTER instruction and execute one instruction (#5) during which the APIC timer interrupt arrives. The interrupt causes an EEXIT, which is followed by the

Table 1: LUT properties and expected leakage of base64 decoding implementations of several standard and SGX crypto libraries. The observed LUT alignment is taken from our test system and may vary between systems and package sources. The estimated leakage $I(B, C)$ depends on the LUT size, its observed alignment and the distribution of relevant entries over cache lines.

| Library      | Version | Decode iterations | LUT size | LUT alignment (observed) | # Cache Lines | $I(B, C)$  |
|--------------|---------|-------------------|----------|--------------------------|--------------|------------|
| Botan [56]   | 2.17.0  | 1                 | 256 byte | variable (32 byte)       | 5            | 0.974 bit  |
| GNU Nettle [63] | 3.6     | 1                 | 256 byte | variable (32 byte)       | 5            | 0.974 bit  |
| mbedTLS [59] | 2.24.0  | 2                 | 128 byte | variable (32 byte)       | 3            | 0.974 bit  |
| MS CryptoAPI [57] | 10.0.18362.476 | 1 | 80 byte | unknown\(^1\) (64 byte) | 2            | 0.811 bit  |
| NSS [55]     | 3.58    | 1                 | 256 byte | variable (64 byte)       | 4            | 0.696 bit  |
| OpenSSL [53] | 1.1.1h  | 2                 | 128 byte | variable (32 byte)       | 3            | 0.974 bit  |
| RustSGX [58] | 1.1.3\(^2\) | 1 | 256 byte | variable (20 byte)       | 5            | 0.564 bit  |
| wolfSSL [54] | 4.5.0   | 1                 | 80 byte  | variable (64 byte)       | 2            | 0.811 bit  |

\(^1\) The source code is not publicly available, so we could not determine whether Microsoft uses a fixed or a variable alignment.
\(^2\) The base64 decoder itself is included in a separate package (version 0.13.0), which gets pulled into the SGX enclave.
In order to extract each key parameter, the trace needs to be partitioned according to the DER format, by identifying parameter lengths and removing meta data: As mentioned in Section 3.3.3, OpenSSL leaks the parameter length information in the _B Nh b2b n_ method, which iterates over every byte in the DER binary, and converts the data to an internal array representation. It can be attacked in a similar manner as the lookup operation, except that the single-stepped Prime+Probe attack must be run against the cache line holding the instruction which loads the next key byte. Counting the number of evictions and translating them to the iteration count determines the length of each parameter easily.

### 4.2 Experimental Evaluation

In the following, we describe the experimental setup to conduct the single-stepped cache attack against base64 decoding, and discuss our observed results. We show that a mitigation against an attack in the transient domain greatly simplifies the process of leaking information from the decoding operation.

#### 4.2.1 Setup

For the evaluation of the attack and leakage extraction, we evaluated two different enclaves and took measurements on three different CPUs. First, we crafted an enclave containing the relevant code parts for base64 decoding from OpenSSL and ran experiments on an Intel i5-8259U processor with an 6144 kB inclusive L3 cache and 4 GB main memory. The cache has 12 ways and, as assessed in our experiments, 8 slices with 1024 sets each.

Second, we conducted the same measurements on an enclave which decodes a base64 encoded private key using the intel-sgx-ssl [65] library in version 1.1.1k, compiled with default settings. The intel-sgx-ssl project compiles and installs the trusted OpenSSL libraries with and without mitigation by default. We linked our enclave against intel-sgx-ssl with MITIGATION-CVE-2020-0551 set to LOAD, CF and no mitigation and compared the results. The measurements with intel-sgx-ssl were run on an Intel Xeon E-2286M with 16384 kB inclusive L3 cache and 16 GB main memory and on an Intel i5-6400 with an 6144 kB inclusive L3 cache and 4 GB main memory.

All CPUs used the latest stable microcode patches. For compatibility with SGX-Step, we used Intel SGX SDK version 2.11. We disabled hardware prefetching for the L1 and L2 caches on each core. Additionally, the CPU frequency was fixed to the processor’s base frequency on all cores, Intel Speedstep was disabled and the maximal C-State was set to 0 in order to decrease variability in the measurements. Finally, we assigned the enclave and its host application to a specific logical core, which was removed from the OS scheduler.

#### 4.2.2 Results

The first experiments were run without configuring the make process to apply mitigations against LVI [11], which are available since the Intel SGX Platform Software (PSW) and Software Development Kit (SDK) version 2.9.100.2.

The results are very noisy and hardly exploitable, in fact most measurement runs are not usable at all, as the eviction time measurements of the Prime+Probe attack are inconclusive: Extracting the sequence of lookups of base64 symbols is not possible, as both monitored sets were accessed, even though we performed a single-stepping attack. Simultaneous accesses are likely caused by speculative or out-of-order accesses of the lookups, as subsequent lookups are only few instructions apart. While single-stepped execution
ensures that only one instruction commits between interrupts, several are issued in parallel in that time window. We further suspect that this transient effect is amplified by resetting the page accessed bits, which increases the out-of-order window. The measurements for this experiment without the LVI mitigation reveal that most of the time, evictions are observed for both investigated cache sets, which renders a distinction infeasible. Table 2 shows a few example measurements for both cache sets without mitigation.

Next, we repeated the measurements with MITIGATION-CVE-2020-0551 set to LOAD [66]. This LVI mitigation places load fences after every instruction which has a load micro-op [11, 67]. Consequently, it prohibits out-of-order execution of instructions after the traced load instruction, which otherwise might have accessed further cache lines in the LLC. Figure 3 depicts a comparison of eviction times for measurements with and without LVI mitigation. It is observable that with the LVI countermeasure, only one of the two monitored cache lines is accessed, while both are accessed when the countermeasure is turned off. We thus conclude that the LVI countermeasure greatly enhances granularity of cache attacks.

The attack we ran against base64 decoding in Intel SGX requires only one execution to create a trace, which leaks all information we can obtain from priming and probing the cache sets holding the LUT. In order to determine the reliability of the measurements, we ran the attack 100 times against the same key and tried to extract the respective cache line access trace. For our experiments, we aligned the lookup table on a 64 byte boundary, such that the LUT used in OpenSSL spread over exactly 2 cache lines. The cache access trace created by the offline analysis is a string with elements from \{1, 2, x\}, where x means that no clear distinction can be made and 1 and 2 identify the accessed cache lines.

Finally, each of the extracted traces is checked for the correct length and compared against the actual key, by checking for each base64 symbol whether it matches the cache line access. The PEM file holding the 1024 bit test key has a length of 848 base64 symbols, thus requiring the same length for the measured cache access trace.

Figure 4 depicts the eviction time measurements for all sets over all slices possibly holding cache line 2 of the LUT when probing the corresponding eviction sets.

The sets in all slices but slice 8 reveal the same spectrum of eviction times for measurements with and without observed page accesses. However, for slice 8, a clear deviation in eviction time measurements can be observed, which allows the detection of LUT accesses.

**Self-Crafted Enclave.** The histogram in Figure 5 shows the number of trace elements which could not be classified (x) or which received a wrong classification per execution. The measurement was taken on the Intel i5-8259U with the “self-crafted” enclave and LVI mitigation level set to LOAD.

The data shows that the attack runs stable in most cases. In 93 of the measurements the automated offline analysis is able to extract a sequence of correct length, and in 62 the number of cache line accesses which could not be classified is less than 10, which is only 1.2% of the full trace. Figure 5 shows that there are only few measurements with more than 30 ambiguous or wrong cache line classifications. Additionally, in none of the 93 measurements, for which extracting the sequence was feasible, a cache line hit was detected for the wrong cache line. This very reliable classification can partially be attributed to OpenSSL looking up each symbol twice.

For the key reconstruction, we are only interested in the lower half (least significant part) of bits of every parameter, as explained in Section 5. This reduces the number of relevant missing cache line classifications to about the half. Moreover, due to a random distribution of missing information, running the attack twice is sufficient to obtain a (near) complete trace.

**Enclave with intel-sgx-ssl.** In Figure 6, the measurement results on the Intel Xeon E-2286M with an enclave using intel-sgx-ssl to decode the base64 encoded key are depicted. The measurement was taken with MITIGATION-CVE-2020-0551 set to LOAD, CF and without mitigation. The results with the mitigation level set to LOAD show that 14 of 100 traces don’t have any errors and 42% of the automatically extracted traces have less than 1.2% of errors (10/848). The attack also works when no mitigations are applied, but significantly worse: On the Xeon, only about 7% of the observed traces have less than 10 missing classifications and there is none without wrong or ambiguous trace elements. As leakage is already quite low, errors must be avoided at all cost, so many traces are required to obtain a reliable trace with no mitigations. The CF mitigation is comparable to no mitigations, as it does not inject fences after load instructions in the decoding routine, but only for control flow related instructions.
Figure 3: Eviction set measurements with and without LVI mitigations enabled. The blue and orange lines correspond to the eviction times of the cache sets holding the LUT. To level both graphs, the respective mean measurement time has been subtracted, resulting in an expected value of 0 when the corresponding set has not been accessed. In the upper plot, with enabled LVI mitigations, we see a clear separation of both sets: If the orange graph is positive, the blue one is 0, and vice versa. Note that the LUT entries are not evenly distributed, leading to a bias towards the orange set. In the lower plot, without LVI mitigations, we see that most of the time both sets are hit, so a clear separation is impossible.

Figure 4: Eviction times measured after every instruction during the decoding process for all cache sets over all slices possibly holding cache line 2 of the LUT. Violet boxes and whiskers show the eviction time of all measurements in which the memory pages of the lookup table and decoding function were not accessed. Green shows the measurements for which the observed pages were accessed. Since no knowledge of the slice mapping is assumed, the slice numbers cannot be matched to a logical CPU core and will be assigned differently in every execution. In the depicted case, the victim’s accesses map to slice 8.

On the Intel i5-6400, the results with no mitigations applied are better, but still clearly worse than with LOAD mitigations enabled.

4.2.3 Practical relevance of LVI mitigations. Setting MITIGATION-CVE-2020-0551 to LOAD has a high performance impact. In general, it is hard to say whether this mitigation is applied in commercial enclaves; that also holds for open source software, since the mitigations are activated by explicitly setting an environment variable. However, we believe that this mitigation has its value in practical applications and that should be applied to secret-dependent workloads like key loading procedures and cryptographic operations.

In general, Intel recommends applying the MITIGATION-CVE-2020-0551 on LVI-affected platforms [68]: “Intel SGX Attestation Service will report a new status code, SW_HARDENING_NEEDED, to indicate the platform is affected by a security advisory for which software hardening is recommended”. Intel recommends enclave developers to “determine the level of software hardening that their environment requires, based on risk analysis and an evaluation of the performance impacts of mitigation”.

The CF (Control-Flow-Mitigation) mitigation level will only protect against LVI gadgets which use control-flow instructions for secret transmission. However, secret transmissions with LVI can also be encoded into the data flow [11], so memory load instructions have to be protected with LFENCEs as well. Since this is rather important in secret-dependent algorithms, there is a practical relevance for the LOAD mitigation level in this case.

We found several concrete applications using these mitigations by default or offering a version with mitigations applied:

- Inclavare Containers [69] and the RUST SGX SDK [58] enable their users to apply the mitigations. For the enclave-tls module of the former, it is even stated in the documentation that the SGX LVI mitigation is enabled by default, but not which level [70]. Both frameworks consider both levels.
- SecretNetwork [71] enables the LOAD mitigation level in their deployment / Docker files [72].
- According to a GitHub issue [73], Asylo [74] uses MITIGATION-CVE-2020-0551 set to LOAD by default since May 2020.
were able to recover the full trace. The histogram shows that the majority of executions had less than 10 measurements where the classification was wrong or ambiguous. This corresponds to around 1.2% of the full trace. The measurements were performed on an Intel Xeon E-2286M against our OpenSSL-based enclave.

Figure 5: Number of ambiguous or wrong cache access measurements for 93 executions of the experiment, where we were able to recover the full trace. The histogram shows that the majority of executions had less than 10 measurements where the classification was wrong or ambiguous. This corresponds to around 1.2% of the full trace. The measurements were performed on an Intel Xeon E-2286M against our OpenSSL-based enclave.

![Histogram of cache access errors](image)

Figure 6: Number of ambiguous or wrong cache access measurements across different mitigation levels. Traces with LOAD mitigation level contain considerably less errors. The measurements were performed on an Intel Xeon E-2286M against the intel-sgx-ssl enclave.

5 RSA KEY RECOVERY

In the following, we will adapt the algorithm of Heninger and Shacham [42] to the setting, where only information about certain blocks of bits is known. Here, we only give a high-level overview and refer the reader to the appendix, which contains a complete formal description of both the setting and the algorithm.

We first formalize the setting, describe the adapted algorithm, and analyze its running time. Finally, we discuss optimizations used in our implementation.

**Blockwise Knowledge.** We consider the situation that some blockwise knowledge about the secret key $sk^*$ was obtained. In the following, we focus on the first five variables and treat $sk^*$ as a quintuple on the variables $Vars = \{p, q, d, p_1, q_1\}$. To simplify the notation, for $v \in Vars$, we denote the corresponding entry in some key $sk$ by $sk[v]$. We show in Sec. A.1 that integrating the last variable $q_1^{-1}$ into the key-recovery approach does not directly give a usable linear equation to contrast in the other variables.

From a high-level perspective, our attack gives us the following information: For each 6-bit block of a variable $v \in Vars$, we know that this block belongs to a certain cache line. This knowledge allows us to rule out the values of the other cache lines for this block. For example, we might know that the first 6 bits of $p^*$ belong to cache line $i$. As we also know the content $C_i \subseteq \{0, \ldots, 2^6-1\}$ of cache line $i$, we can reduce our search space for these 6 bits from the complete space $\{0, \ldots, 2^6-1\}$ down to $C_i$, but we still have a remaining uncertainty about which concrete value in $C_i$ was used. In contrast, in the scenarios studied in [42, 47, 48], the knowledge always was about single bits. Hence, the attacks here might have given the information that the fifth bit of $p$ equals 0. The uncertainty in this scenario comes from the fact that this information could potentially be wrong (e.g., due to a bit-flip in the cold-boot scenario).

**Modeling the Scenario.** As described above, in the situation given by our attack, we do not have observations on single bits, but on blocks consisting of 6 bits, the length of a base64 symbol. To generalize this knowledge, we let $b \in \mathbb{Z}_{>0}$ be the blocksize, i.e., the length of the block on which we have obtained our knowledge. For a variable $v$, we denote the $j$-th block of length $b$ as block$_j(v)$, e.g., the six least significant bits of $p$ are denoted as block$_0(p)$. In our attack, we make use of the fact that the possible values for block$_j(v)$ are partitioned into different sets to model the different cache lines used in our attack. To formalize this, we consider a partition $\text{PART} = (\text{PART}_1, \ldots, \text{PART}_{|\text{PART}|})$ of all possible $b$-bit values $\{0, \ldots, 2^b-1\}$. The set $\text{PART}_i$ would thus correspond to the content of $C_i$ of cache line $i$. Our algorithm is now given an observation about a certain key $sk^*$ stating that for each variable $v \in Vars$, the block block$_j(v)$ belongs to $\text{PART}_i$. In our concrete application, this translates to the knowledge that the $j$-th base64 symbol of variable $v$ belongs to cache line $i$.

5.1 Recovery Algorithm

The main idea of the algorithm is to reconstruct the different bits of the secret key $sk^*$ iteratively. We build up a set of candidates iteratively. Each such candidate is a guess for the least significant bits of the true secret key $sk^*$ compatible with our observation and the RSA equations. We start our algorithm by producing a single candidate $\hat{sk}$ of depth 1, i.e., each variable only consists of a single bit. Informally, the depth of a candidate is the number of bits each variable has. We then apply the expand operation on $\hat{sk}$ to obtain two candidates $\hat{sk}_1$ and $\hat{sk}_2$ of depth 2 by using the RSA
equations described by Heninger and Shacham [42]. Whenever a candidate has reached depth of a multiple of $b$, i.e., $j \cdot b$ for some $j$, we apply the check operation on this candidate to verify that the last produced block $\text{block}_j(v)$ of each variable $v$ is possible under our observation. If this candidate does not fit to our observation, we prune it. We repeat these operations until a target depth $D$ is reached. All produced candidates of depth $D$ are output. This target depth is chosen such that the remaining bits can be reconstructed via the Coppersmith method [76–78].

Our algorithm first performs these operations in a breadth-first fashion to utilize parallelisation and then in a depth-first fashion (see Figure 7). The expand operation uses a set of 4 modular equations on 5 variables and the check operation compares the generated candidates to our observations.

### Pseudocode of the key-reconstruction algorithm

```plaintext
Input: Observation \( \text{obs}(\text{part}) \), target depth \( D \)
1:  find valid triples \((k, kp, kq)\)
2:  for each possible triple \((k, kp, kq)\):
3:     initialize empty stack \( S \)
4:     add initial candidate \( \tilde{sk}(k, kp, kq) \) to \( S \)
5:     while \( S \) is not empty:
6:         let \( \tilde{sk} = S\).pop()
7:         let \( \tilde{sk}_1, \tilde{sk}_2 = \text{expand}(\tilde{sk}) \)
8:         for \( \beta \in \{1, 2\} \):
9:             if depth(\( \tilde{sk}_\beta \)) ≥ \( D \): \textbf{output} \( \tilde{sk}_\beta \)
10:        if depth(\( \tilde{sk}_\beta \)) mod \( b = 0 \) and \( \text{check}(\text{obs}, \tilde{sk}_\beta) \):
11:            S.push(\( \tilde{sk}_\beta \))
12:        else: S.push(\( \tilde{sk}_\beta \))
```

Figure 7: Concise description of our adapted key-reconstruction algorithm

### 5.2 Analyzing the Algorithm

In the following, we analyze the number of candidates of depth \( i \) produced by the algorithm. To do so, we need some probability notions. Let \( pr = (pr[1], \ldots, pr[k]) \) be a probability vector of length \( k \), i.e., \( pr \in [0, 1]^k \) with \( \sum_{i=1}^{k} pr[i] = 1 \). For \( \alpha \geq 0 \) with \( \alpha \neq 1 \), the Rényi entropy \( H_{\alpha}(pr) \) measures the amount of information given by \( pr \) and is defined as \( H_{\alpha}(pr) = \frac{1}{1-\alpha} \log \left( \sum_{i=1}^{k} pr[i]^\alpha \right) \).

The special case for \( \alpha = 2 \) is called the collision entropy, which we will need in the run time analysis of our algorithm, similar to [49]. Intuitively, the usual Shannon-entropy used in Table 1 gives the complete amount of information available, but we can only use certain events to discard candidates not belonging to the observed cache line, namely non-collision events.

To simplify the analysis of our algorithm, we use the heuristic assumptions of [42, 49], namely

**Assumption.**

### Table 3: Overview on the number of calls to the lattice algorithm for blocksize \( b = 6 \) compared with the security level of the key length. Here, \( B \) denotes bits and \( L \) the number of calls to the lattice algorithm.

| Key (B) | level (B) | \( H_2 = 1 \) (L) | \( H_2 = 1.1 \) (L) | \( H_2 = 1.15 \) (L) |
|--------|----------|------------------|------------------|------------------|
| 1024   | 2^{80}   | 2^{49}           | 2^{29}           | 2^{19}           |
| 2048   | 2^{112}  | 2^{92}           | 2^{50}           | 2^{29}           |

(1) Upon random choice of \( sk^* \), for each \( v \in \{p, q, d_p, d_q\} \) and each block \( \text{block}_j(v) \), we have \( \text{Pr}(\text{block}_j(v) \in \text{PART}) = |\text{PART}|/2^b \) and these probabilities are independent.

(2) Once a bit in a candidate \( \tilde{sk} \) is set incorrectly (w.r.t. \( sk^* \)), the set of satisfying solutions to the four congruences behaves randomly and independently.

Using these, we can bound the expected number of candidates.

**Theorem 1.** Let \( C \) be a set of incorrect candidates with depth \( j \cdot b \). After expanding these candidates \( b \) times, the expected number of incorrect candidates after pruning is \( |C| \cdot 2^{b-5} \cdot H_2(pr) + 2^b - 1 \), where \( pr[i] = |\text{PART}|/2^b \).

It is easy to see that we have exactly \( 2^{b-1} \) initial candidates of depth \( b \). We can thus conclude the following theorem about the expected number of candidates.

**Theorem 2.** The expected number of incorrect candidates with depth \( j \cdot b \) is at most \( 2^b \cdot \sum_{i=0}^{j} \left( 2^{b-5} \cdot H_2(pr) \right)^i \frac{2^b}{2^b - 2^{b-5} \cdot H_2(pr) - 1} \).

### 5.3 Termination of the Algorithm

Finally, we need to describe how to set the target depth \( D \) of our algorithm. In a naive approach, we could set \( D = |sk^*[p]| \) and then test for all candidates \( sk \) of depth \( D \), whether \( \tilde{sk} \) is a factor of \( N \). But using a lattice-based approach, we can factor \( N \) much faster. The algorithm of Boneh, Durfee, and Frankel shows that it is sufficient to obtain \( |sk^*[p]|/2 \) bits of \( p \) to factor \( N \) in polynomial time [79, Corollary 1]. By setting our target depth \( D = |N|/4 \) and using the algorithm of Boneh, Durfee, and Frankel on all candidates \( sk[p] \) output by our algorithm, we can reconstruct the correct secret key \( sk^* \). Together with Theorem 2, this shows that \( (2^{b-5} \cdot H_2(pr))^{|N|/4b} \) calls to the lattice algorithm are sufficient to reconstruct \( sk^* \). Table 3 contains the total number of calls to the lattice algorithms for different collision entropies for blocksize \( b = 6 \) (as in our attack), compared with the security level in bits.

### 5.4 Experimental Evaluation

To make the connection between the algorithm described above and our attack more explicit, the partition \( \text{PART} \) corresponds to the (usually two) different cache lines and the block length \( b = 6 \) due to the base64 encoding. To reconstruct the RSA key completely, we implemented the adapted algorithm in C++ and implemented the final reconstruction step via the lattice algorithm small roots in SageMath 9.0. Note that, due to the depth-first approach used in the algorithm, it is highly parallelizable: if we are given \( K + L \) processors, we can compute the first \( K \) candidates in a breadth-first
fashion, distribute them across the processors, and run them in depth-first fashion. The remaining $L$ processors can then be used to apply the lattice algorithm on all candidates of length $D$.

Table 4 contains the experimental results of our algorithm for different key lengths. In order to obtain these experimental results, we used idealized inputs to our algorithm, which were generated by hand, and represent a separate trace for every parameter. Our experimental results showed that the running time of genCands and testCand is relatively stable per candidate with at most 0.0006 seconds for genCands and at most 0.07 seconds for testCand. An extrapolation shows that such a non-optimized implementation does not yet give an algorithm that reconstructs the complete 1024-RSA key within a week: The generation of all candidates via testCand would take about 60 CPU years and the reconstruction via testCand would take about 6,000 CPU years. We estimate a cost of about 1,000,000 dollars on AWS and accordingly a few 100,000 dollars on cheaper bare-bone clouds if we simply use many copies of small roots. But, as shown by the evolution around the Data Encryption Standard (DES), the time to brute-force over a search space of $2^{64}$ (as given in our case for 1024-RSA) can be drastically reduced by more specialized hardware. More concretely, [80] uses 120 low-cost FPGAs and can make about $5 \cdot 10^{10}$ DES calls per second allowing to break DES within two weeks. We thus expect more specialized hardware will lead to a reconstruction time of a few weeks.

6 MITIGATIONS

The demonstrated attack and library analysis show that not only cryptographic implementations themselves need to be protected against attacks, but that it is equally important to shield utility functions from side- and controlled-channel attacks, if they process secret data. We propose two mitigations for the base64 attacks described in this work: First, we describe a constant-time variant of the original lookup table-based decoding algorithm, and discuss the constant-time case decision approach from BoringSSL [64]. Additionally, we highlight how adjusting existing best practices for key storage can help to reduce the surface for attacks on utility functions in general.

6.1 Constant-time decoding

6.1.1 LUT-based. A naive mitigation to our attack on the lookup table would work as follows: In order to make sure that the decoding of each symbol happens in constant time, each entry of the lookup table is accessed for each decoded symbol, and the correct symbol is selected using a mask. This approach will decrease decoding performance drastically, since decoding of each symbol does require 128 lookups (the size of the LUT in bytes), instead of only one.

Table 4: Experimental Evaluation of our implementation on different key lengths and different cache distributions.

| Length | Cache Dist. | genCands \[s\] | testCand \[s\] |
|--------|-------------|----------------|----------------|
| 256    | 38/26       | 795.712        | 31             |
| 256    | 32/32       | 31.760         | 2              |
| 512    | 32/32       | 2.08·10^3     | 1.30·10^3      |


Figure 8: Optimized constant-time decoding of a single base64 character, with a 64-byte aligned lookup table. Note that the LUT only spans two cache lines, so two accesses are sufficient in our leakage model.

To improve the performance of our naive mitigation, we add a constraint on the memory alignment as shown in Listing 8. By instructing the compiler to align the LUT to 64 byte, it is only necessary to access each line once per symbol, which ensures that a controlled-channel attacker cannot determine the correct access in our leakage model. Therefore, we always access the LUT at $b64ch \mod 64 + 64$ and select the correct lookup with a mask as before. In case the current index is smaller than 64, the first access correctly decodes the symbol, otherwise the second. The overhead of the LUT dummy access should be negligible, compared to operations like asymmetric decryption.

6.1.2 Case decision-based. Google’s BoringSSL [64] already implements a constant-time base64 decoding approach.

Constant-time behavior in base64 decoding is achieved by a LUT-free implementation. In a first step, it is determined to which part of the ASCII table the currently decoded symbol belongs. Then, the corresponding binary value is selected using a mask. Listing 10 in the appendix shows the relevant part of the decoding routine from BoringSSL. Other examples for constant-time case decision-based base64 decoding are libodium [81] and Nimbus-JOSE-JWT [82].

We believe that using a case decision-based approach has some advantages over using a LUT: Most cryptographic libraries already offer well-tested and portable macros for constant-time comparison and selection, so employing a separate technique in utility functions does not make much sense. Also, the LUT-based technique highlighted in Listing 8 still makes certain assumptions on the underlying hardware and leakage behavior, which may not apply when compiling the same code for different target platforms. Finally, due to the relatively few calls the performance difference is negligible. We thus recommend to consider replacing LUT-based decoding functions by case decision-based implementations.

6.2 Key Storage Practices

Our base64 decoding attack against RSA keys can also be mitigated by using encrypted PEM files: In this case, the attacker would only learn parts of the ciphertext, and is not able to derive the contained key. After base64 decoding, the DER-encoded key is decrypted and decoded. Assuming that the key loading routine uses the same
We leverage techniques common in the microarchitectural attack which an observation on the variables of the square-and-multiply with a malicious process. Intel advises against such operations [84]. When doing automated replacement of keys and certificates (e.g., Let’s Encrypt), if those private key files are not intended to be transmitted over the network or stored in text-based configuration files, there is no real benefit in using base64 at all, since it just adds overhead and increases the attack surface: In such cases, simply storing the binary DER data would be sufficient.

7 RELATED WORK
In general, leakage in key decoding is not a new concept: The authors of DATA [13] briefly mention true positives in OpenSSL’s key loading functionality, but did not further investigate the issue. In [83], the authors use alternative, but mathematically equivalent key representations to trigger specific non-hardened branches of the decoding routines, which deal with less common key formats and have thus been overlooked in prior research. However, they do not target generic utility functions, but arithmetic aspects of key decoding. To the best of our knowledge, the only other attack targeting utility functions is Medusa [46]. Medusa is an attack which leaks key information during base64 decoding in OpenSSL. However, their focus is on extracting information from the transient domain and attacking the associated rep mov instruction. Such attacks are only possible if SMT is enabled and if the SGX enclave shares the core with a malicious process. Intel advises against such operations [84].

Our attack, however, does not need simultaneous access to the neighboring vCores and works fine on enclaves with disabled hyperthreading. Furthermore, we do not only concentrate on a single instruction, but present a systematic analysis of key decoding functionality in several widely used cryptographic libraries and show that these utility functions leak sensitive information despite and because of the mitigation introduced by other microarchitectural attacks on SGX and through the transient domain [8–11, 36]. We leverage techniques common in the microarchitectural attack domain like Prime+Probe and combine them with a recent attack framework [22] to extract all available leakage introduced through non-constant time behaviour of the base64 decoding process and analyze the leakage with an adapted and generalized version of the Heninger and Shacham key reconstruction algorithm [42].

The algorithm of Heninger and Shacham was already generalized by Bernstein et al. [49], but only to their special scenario, in which an observation on the variables of the square-and-multiply algorithm was used. Our approach is more generic and general. In the setting of cold-boot attacks, the generalizations by Henecka et al. and Paterson et al. [47, 48] outperform the algorithm of Heninger and Shacham [42]. The main reason for this is that, given some partial information, there are some candidates compatible with this observation that are much more likely than other candidates. One can thus prune these unlikely candidates and only introduce a negligible error probability. In contrast, in our scenario all of the candidates compatible with our observation are equally likely and no probabilistic pruning is possible.

8 CONCLUSION
We showed that side-channel resistance is not only relevant for cryptographic routines, but also for utility functions responsible for encoding and decoding secret data. Nearly all of the major cryptographic libraries used lookup tables for these decoding purposes, allowing us to mount a high-resolution cache attack to significantly weaken the security guarantees provided by the underlying encryption schemes. We thus believe that it is important to check all parts of a cryptographic library for side-channel vulnerabilities, e.g., by using automated analysis tools, especially for the case of strong attacker models enabled by trusted execution environments.

There are two important parameters making our attack feasible: First, the high resolution of our attack is possible only due to a security fix for transient execution attacks, as the serialization of memory loads greatly improves the signal-to-noise ratio. Second, while the resulting leakage is quite small, the redundancy in the storage of the RSA keys allows us to achieve a significant drop in the security level of the secret key. Both improvements, one which is intended to mitigate newly emerged attacks and the other targeting at speeding up RSA computations, come at the cost of security and in their combination render our attack possible. We thus believe that studying performance optimizations, security patches and other improvements for their side effects is a crucial task and should be conducted continuously and across all functions which process sensitive data. We also propose to add side-channel analysis to the continuous integration pipelines, such that existing and newly introduced vulnerabilities are identified automatically, and known but minor leakages are re-evaluated depending on new developments in attack accuracy.

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A MISSING PARTS FROM SECTION 5

Blockwise Knowledge. We consider the situation that some blockwise knowledge about the secret key $\text{sk}^*$ obtained. In the following, we focus on the first five variables and treat $\text{sk}^*$ as a quintuple on the variables $\text{Vars} = \{p, q, d, dp, dq\}$. To simplify notation, for $v \in \text{Vars}$, we denote the corresponding entry in some key $\text{sk}[v]$. We show in Sec. A.1 that the last variable $q_p^*$ in the key-recovery approach does not directly give a usable linear equation in contrast to the other variables.

In the situation given by our attack, we do not have observations on single bits, but on blocks consisting of 6 bits, the length of a base64 symbol. In our model, we let $b \in \mathbb{Z}_{>0}$ be the block-size. Without loss of generality, we assume that for each $v \in \text{Vars}$, we have $b(\text{sk}^*[v])$ by zero-padding all variables, i.e. the length $\langle \text{sk}^*[v] \rangle$ of each variable $v$ in our secret key $\text{sk}^*$ is a multiple of $b$. We denote the $i$-th bit of a bit-string $x$ by $x[i]$, i.e. the numerical value of $x$ is given by $\sum_{j=0}^{b-1} x[j] 2^j$. The $j$-th block $\text{block}_j(x)$ in $\{0, \ldots , 2^b-1 \}$ of $x$ is defined as the value of the bitstring in the $j$-th block of $x$, i.e. $\text{block}_j(x) = \sum_{i=j b}^{(j+1)b-1} x[i] 2^{i-j b}$. In our attack, we make use of the fact that the possible values for $\text{block}_j(x)$ are partitioned into different sets to model the different cache lines used in our attack. We consider a partition $\text{PART}_{v}$ of the set $\{0, \ldots, 2^b-1 \}$, i.e. $\text{PART}_{v}$ is a set of sets $\text{PART}_{1}, \ldots, \text{PART}_{t}$ such that $\bigcup_{j \in \text{PART}_{v}} \{0, \ldots, 2^b-1 \}$ and $\text{PART}_{1} \cap \text{PART}_{2} = \emptyset$ for all $i \neq i'$. An observation $\text{obs}(\text{PART}_{v})$ with regard to this partition $\text{PART}_{v}$ is a quintuple that contains for each variable $v \in \text{Vars}$ a vector in $\{1, \ldots, |\text{PART}_{v}|\} \langle \text{sk}^*[v] \rangle / b$. We denote the $j$-th entry of this vector by $\text{obs}(\text{PART}_{v})[\text{sk}^*[v]] / b$. We say that an observation $\text{obs}(\text{PART}_{v})$ is correct for a secret key $\text{sk}^*$ if for all $v \in \text{Vars}$ and all $j \in \{0, \ldots, |\text{PART}_{v}| / b - 1 \}$, we have $\text{block}_j(\text{sk}^*[v]) \in \text{PART}_{v}$ with $j' = \text{obs}(\text{PART}_{v})[\text{sk}^*[v]] / b$ and only if $\text{block}_j(\text{sk}^*[v]) \in \text{PART}_{v}$.

A.1 Adapting the Algorithm

The main idea of the algorithm is to reconstruct the different bits of the secret key $\text{sk}^*$ iteratively. We build up a set of candidates. Each candidate is a guess for the least significant bits of the true secret key $\text{sk}^*$ compatible with our observation and the RSA equations. We start our algorithm by producing a single candidate $\text{sk}$ of depth 1, i.e. each variable only consists of a single bit. We then apply the expand operation on $\text{sk}$ to obtain two candidates $\text{sk}_1$ and $\text{sk}_2$ of depth 2 by using the RSA equations described by Heninger and Shacham [42]. Whenever a candidate has reached depth of a multiple of $b$, i.e., $j \cdot b$ for some $j$, we apply the check operation on this candidate to verify that the last produced block $\text{block}_j(\text{sk})$ of each variable $v$ is feasible under our observation. If this candidate does not fit to our observation, we prune it. We repeat these operations until a target depth $D$ is reached. All produced candidates of depth $D$ are output. This target depth will be sufficient to reconstruct the remaining bits via the Coppersmith method [76–78]. Informally, the depth of a candidate is the number of bits each variable has (see below for details). Our algorithm performs these operations in a depth-first fashion (see Figure 7 in Sec. 5). We now
give a more formal description of our algorithm. The expand operation uses a set of 4 modular equations on 5 variables and the check operation compares the generated candidates to our observations.

(1) As a first step to set up our modular equations, we need to determine values $k, k_p$, and $k_q$ such that

\[ e \cdot s_k^*[d] = k(N - s_k^*[p] - s_k^*[q] + 1) + 1, \]

\[ e \cdot s_k^*[d_p] = k_p(s_k^*[p] - 1) + 1, \]

and $d_q[i + \tau(k_q)]$. Note that a trivial approach would continue the algorithm with all possible $2^b = 32$ assignments, but the partial knowledge given by our candidate allows us to drastically shrink the number of possibilities down to 2.

Therefore, we set up the following system of congruencies derived from the relations between the variables. This is a system with 5 variables and 4 constraints and thus has exactly 2 solutions.

\[ p[i] + q[i] \equiv r_{hs1}[i] \pmod{2} \]

\[ d[i + \tau(k)] + p[i] + q[i] \equiv r_{hs2}[i + \tau(k)] \pmod{2} \]

\[ d_p[i + \tau(k_p)] + p[i] + q[i] \equiv r_{hs3}[i + \tau(k_p)] \pmod{2} \]

\[ d_q[i + \tau(k_q)] + q[i] \equiv r_{hs4}[i + \tau(k_q)] \pmod{2} \]

Here, the right-hand sides are given as

\[ r_{hs1} = (N - 3k[p] \cdot 3k[q]) \]

\[ r_{hs2} = (k(N + 1) + 1 - k(3k[p] + 3k[q]) - e \cdot 3k[d]) \]

\[ r_{hs3} = (k_p(3k[p] + 1) + 1 - e \cdot 3k[d_p]) \]

\[ r_{hs4} = (k_q(3k[q] + 1) + 1 - e \cdot 3k[d_q]). \]

Let $sk_1$ and $sk_2$ be the solutions of depth $i + 1$ obtained by setting the position $i$ (resp. $i + \tau(k)$, $i + \tau(k_p)$, and $i + \tau(k_q)$) of $sk$ to the solutions of the system. For example, if $p[i]$ is part of the first solution, the candidate $sk_1[p]$ for $p$ in $sk_1$ would be given by $sk_1[p] = 3k[p] + 2^i \cdot p[i]$. (4)

(4) Now, whenever a candidate $sk$ of depth $j + b + b$ is reached, we can check, whether the $j$-th block $block_j(v)$ of each variable $v$ is feasible under our observation obs. We therefore check for each $v \in Vars$, whether we have $block_j(sk[v]) \in PART$, with $j = obs(part)(s_k^*[v])$. If this assignment is not possible, we prune the solution. We denote this check against our observation obs as check(obs, sk).

(5) Finally, whenever we find a candidate with our target depth $D$, we output this candidate.

We say that a candidate $sk$ of depth $i$ is compatible with a secret key $s_k^*$ if the $i$ (resp. $i + \tau(k)$, $i + \tau(k_p)$, and $i + \tau(k_q)$) least significant bits of $sk^*[v]$ are identical to $sk[v]$ for all $v \in Vars$. The correctness of the algorithm is easily seen by the following lemma.

**Lemma 3.** Let $sk^*$ be the correct secret key and $sk$ be a candidate of depth $i$ that is compatible with $sk^*$.

- If $i = j \cdot b$ and obs is correct, check(obs, sk) will never prune $sk$.
- Let $sk_1$ and $sk_2$ be the output of expand(sk). Then, either $sk_1$ or $sk_2$ are compatible with $sk^*$.
- The initial candidate of depth 1 produced by the algorithm is compatible with $sk^*$.

**Proof of Theorem 1**

**Proof.** Expanding all of the candidates in $C$ with $b$ bits gives us exactly $2^b \cdot |C|$ incorrect candidates. If we expand any incorrect candidate by $b$ bits, our assumption says that the blocks $j + 1$ of these candidates behave like random $b$-bit strings. Fix one of these candidates $sk$. Now, $sk$ is not pruned, if $block_j(s_k^*[v]) \in PART$ with $j = obs(part)(s_k^*[v])$. For all $v \in Vars$. By our assumption, for each block, this happens with probability $\sum_{i=1}^{2^b} |PART_i|^2/2^{2b} = 2^{-H_2(p)}$, where $pr[i] = |PART_i|/2^b$. As these are independent, the
probability that such an incorrect \( \overline{x} \) is not pruned, is \( 2^{-5H_2(pr)} \). Hence, the expected number of non-pruned candidates where each block behaves like a random \( b \)-bit-string is exactly \(|C| = 2^{b-5-H_2(pr)} \). Furthermore, the expansion of the correct candidate gives us an additional \( 2^b - 1 \) incorrect candidates.

**Proof of Theorem 2**

Proof. As noted above, we have \( 2^{b-1} \leq 2^b \) candidates of depth \( b \). A simple induction combined with Theorem 1 shows that the number of incorrect candidates with depth \( j \cdot b \) is at most \( 2^b \cdot (2^{b-5-H_2(pr)} - 1)^j \). Hence, the expected number of non-pruned candidates where each additional \( b \)-bit-string is exactly \( |C| = 2^{b-5-H_2(pr)} \). □

**THE LAST PARAMETER** \( q_{p}^{-1} \)

The attentive reader might have noticed that we obtain information about six parts of the secret key \( p, q, d, d_p, d_q, \) and \( q_{p}^{-1} \), but do not use the information about \( q_{p}^{-1} \) in our key reconstruction algorithm.

In the following, we will shortly illustrate the problems of integrating \( q_{p}^{-1} \) into the key-reconstruction algorithm. First, note that, similar to the other variables of the secret key, one can easily conclude that there is some value \( k' \) such that \( q \cdot q_{p}^{-1} = k' \cdot p + 1 \). But the following adaption of an argument of Nguyen (described in [42]) shows that knowing \( k' \) already reveals the factorization of \( N \). As \( q \cdot q_{p}^{-1} = k' \cdot p + 1 \), multiplying both sides of the equation by \( p \) gives the equation \( N \cdot q_{p}^{-1} = k' \cdot p^2 + p \). Defining the polynomial \( f(x) = k' \cdot x^2 + x \) shows that \( f(p) \mod N = 0 \). Hence, \( p \) is a small root of a known polynomial (if \( k' \) is known) and can thus be found by the method of Coppersmith [76–78].

**B AN EXAMPLE KEY IN DER ENCODING**

![Figure 9: 1024-bit RSA private key, DER encoded according to PKCS #8, in hexadecimal format.](image)

**C LEAKAGE ESTIMATION WITH MICROWALK**

Table 5: The leakage estimation from Microwalk for OpenSSL, generated from 4,096 test cases. For each instruction, Microwalk computes the Mutual Information (MI) between the memory access traces and the test case IDs, which measures the ability of an attacker to infer the input from an observed trace. Note that the leakage is upper bounded by the logarithm of the number of test cases (12).

| Instruction                        | Avg. leakage (bits) |
|------------------------------------|---------------------|
| EVP_DecodeUpdate+1D5               | 12                  |
| EVP_DecodeBlock+E                  | 12                  |
| EVP_DecodeBlock+59                 | 12                  |
| EVP_DecodeBlock+C8                 | 12                  |
| EVP_DecodeBlock+D4                 | 12                  |
| EVP_DecodeBlock+EA                 | 12                  |
| EVP_DecodeBlock+F8                 | 12                  |
| EVP_DecodeBlock+G9                 | 12                  |
| EVP_DecodeBlock+14D                | 12                  |
| EVP_DecodeBlock+C8                 | 12                  |
| EVP_DecodeBlock+D9                 | 12                  |
| EVP_DecodeBlock+EE                 | 12                  |
| EVP_DecodeBlock+13B                | 12                  |
| EVP_DecodeBlock+142                | 12                  |
| PEM_read_bio+1D0                    | 1.009               |
| PEM_read_bio+1ED                    | 1.009               |
| PEM_read_bio+1F2                    | 1.009               |
D BORINGSSL’S BASE64 DECODING

```c
static uint8_t base64_ascii_to_bin(uint8_t a) {
    // Since PEM is sometimes used to carry private keys, we decode base64 data
    // itself in constant-time.
    const uint8_t is_upper = constant_time_in_range_8(a, 'A', 'Z');
    const uint8_t is_lower = constant_time_in_range_8(a, 'a', 'Z');
    const uint8_t is_digit = constant_time_in_range_8(a, '0', '9');
    const uint8_t is_plus = constant_time_eq_8(a, '+');
    const uint8_t is_slash = constant_time_eq_8(a, '/');
    const uint8_t is_equals = constant_time_eq_8(a, '=');
    uint8_t ret = 0xff; // 0xff signals invalid.
    ret = constant_time_select_8(is_upper, a - 'A', ret); // [0,26)
    ret = constant_time_select_8(is_lower, a - 'a' + 26, ret); // [26,52)
    ret = constant_time_select_8(is_digit, a - '0' + 52, ret); // [52,62)
    ret = constant_time_select_8(is_plus, 62, ret);
    ret = constant_time_select_8(is_slash, 63, ret);
    // Padding maps to zero, to be further handled by the caller.
    ret = constant_time_select_8(is_equals, 0, ret);
    return ret;
}
```

Figure 10: Base64 decoding constant-time implementation in Google’s BoringSSL [64] (crypto/base64/base64.c)