More and more industrial devices are connected to IP-based networks, as this is essential for the success of Industry 4.0. However, this interconnection also results in an increased attack surface for various network-based attacks. One of the easiest attacks to carry out are DoS attacks, in which the attacked target is overloaded due to high network traffic and corresponding CPU load. Therefore, the attacked device can no longer provide its regular services. This is especially critical for devices, which perform Real-Time (RT) operations in industrial processes. To protect against DoS attacks, there is the possibility of throttling network traffic at the perimeter, e.g. by a firewall, to develop robust device architectures. In this paper, we analyze various concepts for secure device architectures and compare them with regard to their robustness against DoS attacks. Here, special attention is paid to how the control process of an industrial controller behaves during the attack. For this purpose, we compare different schedulers on single-core and dual-core Linux-based systems, as well as a heterogeneous multi-core architecture under various network loads and additional system stress.

**Keywords**
Industrial Control Systems · Real-Time · Denial of Service · Network-based Attack · Flooding

1 Introduction

Modern industrial devices, like Programmable Logic Controllers (PLCs), are more and more connected to IP-based network structures due to the trend of Industry 4.0, which is based on network-enabled machines, actuators and sensors. In addition to controlling a Cyber Physical System (CPS), the connectivity enables features, like easy configuration, remote data collection, web services, updating of firmware or uploading of control programs. These features increase the productivity and comfort of use, but the wide accessibility also enlarges the attack surface of the industrial controllers through various network-based attack vectors [1]. Furthermore, the historical network isolation by air gaps no longer applies, making components a possible target for network-based attacks.

The third industrial revolution was founded on the use of PLCs, first introduced by Modicon 1969, which automate the manufacturing process by digital programming and provided a huge gain of productivity [2]. These devices were designed without considering any security aspects for their connectivity, since the devices were separated from...
Analysis of Industrial Device Architectures for Real-Time Operations under Denial of Service Attacks

IT network infrastructures by the concept of air gap. This means a physical segregation of the Industrial Control System (ICS) network from other networks. As a consequence, the air gap for the industrial processes is nowadays not always guaranteed and other mechanisms are required, since the communication between IT and OT networks arises due to Industry 4.0.

Many processes in the industrial context require a control loop, that must react fast and within a certain time, e.g. the fill up process in a bottling plant. The PLCs, which control the processes, are working in a cyclic manner, i.e. they repeatedly execute a control program e.g. every 1 ms. Deviation of this cyclic execution of the process control program can lead to bad consequences, like too much or too little fill quantity. These systems must provide a deterministic behavior, i.e. a known latency jitter from stimulus to response within the industrial control program. This deterministic control can be provided by Real-Time (RT) capable devices.

Recent research shows, that the cyclic operations of several commercial control devices can be influenced by network-based attacks. Niedermaier et al. presented, that high network traffic loads can affect the cyclic execution of common PLC devices up to complete system failures \[3\]. These kind of flooding attacks enable even less experienced attackers with access to the industrial network to influence the cyclic execution of control programs and can thereby cause disturbance to controlled physical processes. Two different types of attackers are considered, as shown in Fig. 1. For instance an external attacker \(1\) can perform a Denial of Service (DoS) attack on a service, that is accessible from external networks, like the Internet. The second attacker type is an internal attacker \(2\) who, in addition to an intended attack with flooding, could also trigger an DoS attack unintentionally e.g. by executing a network scan. This attacker type differentiation assumes proper firewall configuration, so no flooding attack or scanning, e.g. for asset management, is possible from external networks.

![Diagram](image)

Figure 1: DoS attack scenarios on PLCs addressed in this work.

Vendors of industrial components have to make decisions about the underlying architecture design in an early development state. This early decision must already consider proper protection against DoS attacks. The recent industrial security standard IEC 62443-4-2 requires DoS Protection from secure industrial devices. Therefore a Security-by-Design approach for modern industrial control devices is obligatory, to achieve robust regular execution of a control task, when network connectivity is necessary. A secure architecture for industrial control devices is required, which is also robust against various kinds of network flooding attacks and under certain system loads. To evaluate suitable system architectures for future PLC designs, influences of certain stress factors on RT execution must be considered.

The General Purpose Operating System (GPOS) Linux is a common choice for industrial components, due to need of implementing demanding Graphical User Interfaces (GUIs) or the possibility, to use open source libraries. In addition Linux can be used for commercial products and supports multiple hardware architectures. The implementation of features is commonly less costly on fully featured operating systems, like Linux, and therefore development duration and costs are far less, than on systems, based on bare metal or Real Time Operating System (RTOS) \[4\]. Linux is a GPOS, but by applying the `preempt_rt` patch, it becomes RT capabilities \[5\]. This combination addresses the requirement for a fully fledged Operating System (OS) and the real-time needs for demanding industrial control processes.

The contribution of this paper is the systematic measurement of influences on a control program under network load and CPU stress scenarios, executed on different device architectures. Further, we discuss the measurement results and the consequences of architectural choices on the robustness of industrial components against DoS attacks.

The paper is organized as follows. First we provide a summary of related work in Section 2, followed by the presentation of technical background about RT systems, PLCs and network-based attacks in Section 3. We present the selection of architectures in Section 4. Section 5 describes the method of our measurements and the measurement setup. Further, the test cases and the results are shown in Section 6 followed by a discussion in Section 7. A final conclusion is provided in Section 8.
2 Related Work

Influences of DoS attacks on ICS components are still a topic in research and were investigated in previous works. Long et al. analyzed DoS attacks on network-based control systems and how this degrades their performance almost two decades ago [6]. Although this work discusses DoS attacks on PLCs, the results are based on simulation data and no investigations of real devices is done. This theoretic work handles effects of delay on communication between PLC and remote devices and not the effects in connection with system load, produced by receiving many packets.

Markovic et al. also provide measurements of performance degradation under Distributed Denial of Service (DDoS) attacks, based on simulation data [7]. In comparison to these works, we want to provide realistic measurement data by investigating influences on electrical controls of real devices.

Niedermaier et al. presented measurement of common of the shelf PLCs under certain network loads [3]. The measurements aim for physical influences of network-based flooding attacks, but lacks architecture comparison to provide a robust network-enabled PLC design. We use similar measurement routines, but also discuss architecture approaches and their suitability for future robust PLCs.

Recent research already discusses robust hardware architecture for ICS. Niedermaier et al. presents a dual controller setup, which separates the control task and the communication part by hardware [8]. This architecture design requires implementation of a custom dual controller setup and lacks the capability to run a full fledged OS, like Linux. This concept is not comparable to architectures, which provide the features of a full OS for functionality next to the process control, like in the architecture designs within our work.

Lelli et al. discuss the deadline scheduler under Linux and compare the percentage of missed deadlines with SCHED_FIFO and SCHED_OTHER under certain system load scenarios [9]. They come to the conclusion, that SCHED_DEADLINE is suitable for hard RT tasks, if the taskset can be partitioned and the per-core load is <1. However no results for full system utilization and other sources of load, e.g. network traffic, are discussed within their work. This worst case scenario for RT execution is analyzed by our measurements.

On Linux-based RT systems the measurement tool cyclicstress is a common method to determine the kernel latency on all cores of a Device under Test (DuT) [10]. Linutronix runs continuous tests on multiple hardware platforms with this tool and applies a defined load during the tests [11]. The test routines contains certain network communication load, but lack investigation of influences during network-based attacks, like flooding.

In further work there is already investigation of jitter on RT patched Linux systems, measured on digital outputs [12][13][14], but none covers external influences, like high network loads to these systems.

In summary, related work does not cover demanding cyclic execution under heavy network-based attacks. Therefore we focused our work on creating a test methodology, which covers these scenarios.

3 Technical Background

This section discusses the topics RT, PLCs and network-based attacks.

3.1 Real Time

To control a CPS, control devices need to provide RT operations. RT by far does not mean fast processing, but deterministic and in-time execution of a certain task. A specific process has to complete and provide its results within a time mark, known as deadline. RT systems can be classified in the categories soft, firm and hard [15]. This classification is done by the consequences accompanied with the miss of a RT system deadline. Deadline misses on soft RT systems lead to a degradation of the event value after the deadline. Misses on a firm RT system degrade the value of the event to zero after the deadline. A single deadline miss on a hard RT system can lead to a complete fault of the controlled process. This can cause catastrophic consequences, like out-of-control production processes, destruction of production environment and gear or even hazard to human beings.

3.2 Programmable Logic Controllers (PLC)

PLCs nowadays are the main devices to control ICS and therefore have to provide RT capability. The conditions, that must be met are highly depending on the physical process, controlled by the device. Therefore control devices must be prepared, to provide the required RT capability even in worst case scenarios, like high system load or during a network-based attack. A control program is executed on PLCs in a cyclic manner and processes the four steps illustrated in Fig. 2.
Figure 2: Program execution on a cycle orientated PLC.

The read inputs stage \( \text{1} \) handles the read of digital or analog inputs on the PLC. The program execution stage \( \text{2} \) handles the execution of the cyclic control program. The housekeeping part \( \text{3} \) can service communication requests, internal checks or diagnostic functionality. The write outputs stage \( \text{4} \) handles the writing of the logic values back to the electric analog or digital output pins of the PLC. This control program is executed periodically within the configured cycle time. Deviation of this cycle time can cause a delayed response on stimuli from the CPS and therefore disturb the RT controlling.

3.3 Network-based Attacks

A known method to achieve deviation on RT devices is network flooding. Network packets produce certain system load at the receiving device on arrival, even if no payload is handled, since information of the underlying protocols from some message types are still processed. Parsing and interpreting this information already consumes CPU time, even if the receiver has no listening service running and is not awaiting certain packets. Flooding massive amount of packets containing Transmission Control Protocol (TCP), synchronize (SYN) packets or Address Resolution Protocol (ARP) requests for instance are producing high amount of system load and aim for DoS on the device. This externally triggered system load can be used to disturb the regular execution of the receiving device. Filtering and blocking of certain network packets e.g. with firewall rules can mitigate these influences, but degrades also the throughput of the network traffic, e.g. by limiting the SYN packet rate.

4 Architectures

Robust and distortion free execution of the cyclic industrial control program is an essential feature of PLCs. For this reason, this work analyzes and compares the influences of flooding attacks on different device architectures.

The implementation of RT capable devices can be based on various design approaches. The focus in this paper is on full open source implementations and therefore the considered solutions lack proprietary concepts and software. In the following the architecture concepts, which are used as the DuTs within the measurement procedure, are introduced.

Two architectures, which execute the critical task on a preemption patched Linux are defined: (S) a single-core system and (D) a dual-core system. We configure these architectures to use the real time schedulers SCHED_FIFO (First-In-First-Out), SCHED_RR (Round Robin) and SCHED_DEADLINE. In addition (D) also pins the critical process to CPU2, while the network kernel process runs on CPU1.

The third variant (C) is a special architecture design, based on a dual-core Linux system and a co-processor. This co-processor handles the critical control task, while network communication is handled on the Linux system.

These architecture concepts result in the following test cases:

(S) Single-core system running Linux
   (SF) using SCHED_FIFO
   (SR) using SCHED_RR
   (SD) using SCHED_DEADLINE

(D) Dual-core system running Linux
(DF) using SCHED_FIFO and pinned execution on CPU2  
(DR) using SCHED_RR and pinned execution on CPU2  
(DD) using SCHED_DEADLINE and pinned execution on CPU2  
(C) Dual-core system running Linux with additional co-processor

For single-core (S) and dual-core (D) test cases a Raspberry Pi 4 is used. The Linux image is created with the buildroot environment [16] and enabled `preempt_rt` patch on Kernel Version 4.19.113. Since the background processes have influence on process latencies, this minimal setup is used. On the Linux-based DuT, the static priority schedulers SCHED_FIFO and SCHED_RR are configured with the highest possible priority of 99. The SCHED_DEADLINE configures its three parameters the following. Runtime is set to 100 000 ns, which is the execution time assigned to the task within a period, while its deadline and period are set to 1 000 000 ns.

For the co-processor test case (C), a development board with the STM32MP1 Microcontroller Unit (MCU) from ST Microelectronics is used [17]. The MCU consists of a dual-core Cortex A7 CPU with additional Cortex M4 co-processor. This device provides a test case for hardware separated execution.

5 Methodology and Measurement Parameters

The architectures selected for this work are used to implement a minimal RT industrial process. Thereby, we want to provide measurements and comparison of influences on the regular execution of a task on these architectures during network-based attacks and additional synthetic system loads. The results can give advice for future designs of robust PLCs.

To represent a common cyclic execution of industrial control programs, a elementary periodical program, that inverts the logic level of a physical output within every cycle, is used. So the stages program execution @ and write outputs # are present. Other execution stages, like reading inputs $ or housekeeping % are not necessary and thus omitted within our analysis. The minimal control program is provided for the Linux-based systems (S) and (D), as well as on the bare metal system (C). The cycle time within our control program is set to 1 ms in all configured test cases, as this is a common minimal cycle time for off-the-shelf PLCs. This results in a digital output signal, as illustrated in Fig. 3.

The regular signal is a square wave signal, which changes the output state every 1 ms. If no influence occurs, the square wave signal is continuing as expected. In contrast to this, the square wave signal delays or keeps the current output value, when network flooding influences the control program.

![Figure 3: Impacts on cycle time and output signal.](image)

5.1 Setup

To measure the output signal of the DuT, the Saleae Logic Pro logic analyzer is used [18], to capture the temporal progression of this signal during the test scenarios. Fig. 4 shows a schematic of the measurement setup. The sample rate is configured to 250 Megasamples per second. This device is connected to a computer, which is also executing the network stress tests via a direct Gigabit Ethernet connection to the DuT. Network hops in between might decrease the packet rate during a full load network attack, therefore we used a direct connection to simulate the worst case scenario, where the attacker has unlimited access without any bandwidth limitations.

5.2 Attacking Tools

Network flooding with SYN and ARP packets and network scanning are carried out on the DuT to disturb the regular execution.

For the first attack, a SYN flood test generates a large amount of SYN packets, without handling the resulting responses from the DuT. The second attack is an ARP flood program, which generates gratuitous ARP requests, which are sent to the DuT.

---

(C) ---

Analysis of Industrial Device Architectures for Real-Time Operations under Denial of Service Attacks
We also measure the impact of the common network scanning tool nmap [19]. The tool is used to detect configurations of the network connection, e.g. for asset management in the industrial network. Without rate limitation this tool also generates massive network load for the DuT. In our test cases a full SYN scan for all 65535 ports is executed. The use of this tool is not intended to disturb the receiver device, but since the scan of open ports without scan rate limitation can generate high network traffic, similar to the SYN flood tool, consequences for the cyclic control program under this network load were measured. The measurement period is set to ten seconds for the idle and the attack measurements, due to the fact, that a full nmap scan on the DuT takes around three to eight seconds in our setup.

Additional CPU load is generated to simulate high system utilization, e.g. brought by regular execution, demanding tasks or further attacks, which aim for high load generation on the device.

This system load is created with the common command line tool stress-ng and combined with the SYN and ARP flooding attacks and nmap network scanning. Within this test run, we set one Central Processing Unit (CPU) load process for single-core systems and two CPU load processes for the dual-core systems, which get pinned to a CPU each. This results in a user-space process, which consumes 100 percent CPU time on all available cores. Additional CPU load is intended to simulate high system utilization. This is common for demanding industrial use cases, which require much processing time, at least for certain time.

5.3 Measurement Procedure

A measurement procedure consists out of three measurements, with a duration of five minutes each. While one measurement is taken during network attack, the other two capture the device in idle, before and after the attack. A five seconds break is implemented between these three captures. The measurement during the attack gives information about expectable consequences of the attack scenario, while the measurement before and after the attack is used for comparison to the regular execution and the idle jitter. The capture after the attack also reveals information, if the influences of the attack are persistent, e.g. if the system crashed under the attack load.

6 Results

In this section the measurement results of our setup are presented and outcomings are discussed.

6.1 DoS with Flooding for Single and Dual-core

The analysis with SYN and ARP based network attacks showed, that single-core configurations, like (SF), (SR) and (SD), have high outliers of their periodic toggle frequency during attack, in comparison to their idle measurement before and after. The single-core setups do not show any deviation of mean cycle time, but have outliers multiple times higher and lower than the mean value. There are outliers observed, which are multiple times the common cycle time of one millisecond, while the highest outliers can be found in the single-core setup with deadline scheduler (SD). These high outliers get compensated by lower outliers, up to 62 times smaller, than the mean value. This results in a mean cycle time without deviation, like the idle mean. While faster cyclic execution should work well for most use cases, the higher outliers conditions delayed execution within the CPS. This behavior can cause severe disturbance to the controlled physical process. Both network attacks result in comparable disturbance to the signal, especially for (SF) and (SR) the distribution differs and more cycles are found around the mean cycle time of 1 ms. The results for SYN flooding attack on (SD), (SF) and (SR) are depicted in Fig. 5. Our measurement for ARP flooding for the single-core test cases is shown in Fig. 6.
In the dual-core scenario with pinning the toggle process to CPU2, an impact on cycle time during the SYN flood attack is not recognizable for all three test cases (DD), (DF) and (DR). There are outliers measured during idle and attack, which jitter a few thousandths around the mean. Fig. 7 shows the dual-core test cases during SYN flooding. The dual-core test cases show minimal higher outliers during the ARP flooding attack, but the deviation stays around one percent. ARP flooding for all dual-core test cases is depicted in Fig. 8. Since the choice for a Linux-based system for RT demands, presupposes the acceptance of some jitter during the execution of the control process, the measured dual-core systems provide a low jitter, even under network attack, for the configured cycle time.

In addition to network flooding, synthetic CPU load is generated during the measurement on the DuT, to simulate high system utilization.

The single-core configurations (SD), (SF) and (SR) with stress show comparable distribution but higher outliers during ARP and SYN flooding, in comparison to the measurement without additional CPU load. SYN flooding with stress is depicted in Fig. 9. ARP flooding with stress is shown in Fig. 10.

The dual-core setups with additional stress now have higher outliers during SYN and ARP flooding. This differs from the measurement of these systems without additional load, where only ARP resulted minor outliers during attack. The setups (DF) and (DR) now show higher and lower outliers during network attack, which results in a jitter around 11-13 percent.

(DD) with full CPU utilization, shows high outliers even in the idle measurements. These outliers are two times the common cycle time and do not get worse under attack. So a fully utilized dual-core system, using deadline scheduler shows very high jitter, even without additional network load. A fully utilized system using the deadline scheduler with our tested configuration does not provide a low jitter system, which seems usable for RT controlling needs. This odd behavior requires further investigation with this test case in addition to a fully loaded system.

6.2 DoS with Flooding for Single and Dual-core and CPU Load

In addition to network flooding, synthetic CPU load is generated during the measurement on the DuT, to simulate high system utilization.

The single-core configurations (SD), (SF) and (SR) with stress show comparable distribution but higher outliers during ARP and SYN flooding, in comparison to the measurement without additional CPU load. SYN flooding with stress is depicted in Fig. 9. ARP flooding with stress is shown in Fig. 10.

The dual-core setups with additional stress now have higher outliers during SYN and ARP flooding. This differs from the measurement of these systems without additional load, where only ARP resulted minor outliers during attack. The setups (DF) and (DR) now show higher and lower outliers during network attack, which results in a jitter around 11-13 percent.

(DD) with full CPU utilization, shows high outliers even in the idle measurements. These outliers are two times the common cycle time and do not get worse under attack. So a fully utilized dual-core system, using deadline scheduler shows very high jitter, even without additional network load. A fully utilized system using the deadline scheduler with our tested configuration does not provide a low jitter system, which seems usable for RT controlling needs. This odd behavior requires further investigation with this test case in addition to a fully loaded system.
Analysis of Industrial Device Architectures for Real-Time Operations under Denial of Service Attacks

Figure 9: Single-core 5 min SYN flood test for (SD), (SF) and (SR) with CPU load

Figure 10: Single-core 5 min ARP flood test for (SD), (SF) and (SR) with CPU load

SYN flooding on the dual-core test cases with additional CPU load is depicted in Fig. 11 and for ARP flooding in Fig. 12. This shows also the odd behavior of (DD) under attack, which is similar in the pre and post idle.

6.3 Impacts of Network Scanning

The previously shown scenarios are intended to provoke a DoS of the DuT intentionally. However, network load is not just caused by offensive network traffic, but also by intentional network services, like scans. Hence, this scenario shows the effects of a conventional network scanner (nmap) on the different architecture configurations.

The test cases (SD), (SF) and (SR) have similar outliers than under ARP and SYN flooding, while there is again no deviation from the mean cycle time. Dual-core setups (DD), (DF) and (DR) do not show additional outliers during the nmap scan. Resulting influences during nmap scanning is depicted in Fig. 13.

6.4 Impacts on Co-Processor Architecture (C)

The measurement of the co-processor test case showed no measurable deviation during all attacks, compared to idle. All measured outliers in the measurements are within a very low jitter of a view nanoseconds. This is conditioned by the strict separation between co-processor executing the cyclic program and the Linux system, which results in a near perfect cyclic signal. Fig. 14 depicts test case (C) under SYN flooding attack, while the other attacks show similar results.
6.5 Network Packets and CPU Load

During the flooding attacks, the attacker sends about 100,000 SYN packets/s to the DuT. The DuT answers these packets with around 10,000 SYN/ACK and SYN/RST packets/s.

This indicates that not all network packets can be processed. The flooding attack does not crash the network communication, since the DuT constantly sends packets back to the sender device over the complete measurement period.

To determine the cause of disturbance under network-based attacks, CPU usage is analyzed for a single-core test case. The CPU load distribution during a SYN flooding attack is shown in Fig. 15. It can be observed that during the attack the software IRQ increases to almost 100% CPU utilization. This high utilization has an impact on the lower priority user tasks, e.g., the cyclic toggle program.
7 Discussion

During our measurements the different architecture designs showed very different impacts to the different network-based and CPU-based loads. Table 1 and Table 2 show the highest measured outliers with and without additional CPU load. For future PLC designs, the results can be a reference for the requirement of robustness. The measured influences on the control process during network and system load determine the choice of the underlying architecture, therefore the measurement outcome gets summarized to give recommendations.

The introduced hardware separation with a co-processor provides best results in latency jitter, already in the idle state. But the implementation of such an architecture requires low-level programming and software development skills. To provide a deterministic and jitter free controller for CPS, the co-processor solution is the only acceptable architecture from the measured test cases. This makes the co-processor architecture the best choice for hard RT demands, which can not accept single outliers during regular execution. However, already dual-core systems, with additional task pinning, provide a robust setup for RT demanding industrial control processes. Even if there are influences measurable during attack or network scans, the measured dual-core setups provide overall a low jitter. If little deviation from expected execution is tolerable for the control task, multi-core systems, running Linux `preempt_rt` can offer a viable architecture for executing ICS tasks. Our measurements show, that task pinning in multi-core systems - (DD), (DF) and (DR) - provide robustness from network flooding attacks, since without additional load, no impact during attack can be measured. Even in combination with CPU load, (DF) and (DR) provide low cycle time delay, around 11-13 percent, while (DD) suffers from full utilization. This architecture suits firm real-time needs, were some missed deadlines are tolerable and do not disturb regular execution.

|          | Idle       | SYN flooding | ARP flooding | Nmap       |
|----------|------------|---------------|--------------|------------|
| **SD**   | 1.008 ms   | 27.852 ms     | 25.685 ms    | 21.678 ms  |
| **SF**   | 1.013 ms   | 3.438 ms      | 3.331 ms     | 2.560 ms   |
| **SR**   | 1.008 ms   | 4.213 ms      | 3.200 ms     | 2.603 ms   |
| **DD**   | 1.007 ms   | 1.008 ms      | 1.011 ms     | 1.005 ms   |
| **DF**   | 1.005 ms   | 1.006 ms      | 1.007 ms     | 1.005 ms   |
| **DR**   | 1.006 ms   | 1.006 ms      | 1.010 ms     | 1.005 ms   |
| **C**    | 1.000 ms   | 1.000 ms      | 1.000 ms     | 1.000 ms   |

Table 1: Overview of maximum cycle time, without additional CPU load

|          | Idle       | SYN flooding | ARP flooding | Nmap       |
|----------|------------|---------------|--------------|------------|
| **SD**   | 1.018 ms   | 30.681 ms     | 69.619 ms    | 22.143 ms  |
| **SF**   | 1.014 ms   | 4.282 ms      | 21.389 ms    | 2.661 ms   |
| **SR**   | 1.014 ms   | 4.438 ms      | 21.697 ms    | 2.769 ms   |
| **DD**   | 2.043 ms   | 2.016 ms      | 2.022 ms     | 2.027 ms   |
| **DF**   | 1.039 ms   | 1.111 ms      | 1.113 ms     | 1.070 ms   |
| **DR**   | 1.052 ms   | 1.122 ms      | 1.130 ms     | 1.082 ms   |
| **C**    | 1.000 ms   | 1.000 ms      | 1.000 ms     | 1.000 ms   |

Table 2: Overview of maximum cycle time, with additional CPU load

Single-core solutions - (SD), (SF) and (SR) show high outliers during network-based attacks. The cyclic execution shows outliers, which are multiple times higher, than the mean cycle time. There are also outliers, which are multiple times smaller than this mean time. While the higher outliers can cause massive delay in process execution, faster cycles are tolerable for most scenarios. In addition, it should be mentioned, that the single-core test cases do not show any deviation in the mean value of the cycle time. Therefore this architecture could be the correct choice for soft real-time control systems, if some high outliers of regular cyclic execution are neglectable.

8 Conclusion

In this work, we discussed how different configurations of schedulers and CPU architectures influence the robustness of ICS devices against high network communication loads. For real-time control processes, a `preempt_rt` patched Linux is a complex underlying system. This results in a general higher jitter, due to kernel and scheduling latencies. The use of multi-core systems with real-time patched Linux and pinning the critical process to a different CPU provides already good robustness for network flooding attacks, even in combination with high CPU utilization.

Physical processes, which are controlled by such devices, have specific but various demands on the RT capabilities of the controlling device. For these reasons, a general recommendation for a RT capable industrial control device
architecture is hard to define, since this choice also depends on factors, like development and hardware costs, required features of the underlying system and many more.

The outcome of this work can act as a reference to determine the choice of robust architectures for future PLCs. Robustness of future PLCs against network-based attacks is essential, due to the increase of connectivity. Therefore our measurement methodology and results should be considered for the selection of future architecture for RT industrial devices. If single deadline misses lead to catastrophic consequences for the control process, developers should reconsider the usage of Linux preempt RT, since our measurement shows high impact on single-core and measurable impact on multi-core test cases on the cycle time. If this jitter is not tolerable for the control process or the controlled CPS has hard RT requirements, the execution of the control process on a dedicated CPU is the only feasible solution within our measurements.

The measured heterogeneous multi-CPU architecture, provides Linux features and also a co-processor, which creates a predictable and robust RT system. But even multi-core Linux systems showed very little jitter, even under worst case network loads, which makes them suitable for multiple use cases. If Linux-based systems are used for RT process control, further additional mitigation strategies e.g. firewall rules must be considered and therefore can be part of future investigation and measurement.

Acknowledgments

This work was partly funded by the Bavarian Ministry of Economic Affairs, Regional Development and Energy in the project ProLogCloud through grant number ESB066/003.

References

[1] Juan Enrique Rubio, Cristina Alcaraz, Rodrigo Roman, and Javier Lopez. Current cyber-defense trends in industrial control systems. Computers & Security, 87, 2019.
[2] Rainer Drath and Alexander Horch. Industrie 4.0: Hit or Hype? [Industry Forum]. IEEE Industrial Electronics Magazine, 8(2):56–58, 2014.
[3] Matthias Niedermaier, Jan-Ole Malchow, Florian Fischer, Daniel Marzin, Dominik Merli, Volker Roth, and Alexander von Bodisco. You Snooze, You Lose: Measuring PLC Cycle Times under Attacks. 12th USENIX Workshop on Offensive Technologies (WOOT 18), 2018.
[4] Federico Reghenzani, Giuseppe Massari, and William Fornaciari. The Real-Time Linux Kernel: A Survey on PREEMPT_RT. ACM Computing Surveys, 52(1):1–36, 2019.
[5] Daniel Bristot De Oliveira and Romulo Silva De Oliveira. Timing analysis of the PREEMPT RT Linux kernel. Software: Practice and Experience, 46(6):789–819, 2015.
[6] M. Long, C.-H. Wu, and J.y. Hung. Denial of Service Attacks on Network-Based Control Systems: Impact and Mitigation. IEEE Transactions on Industrial Informatics, 1(2):85–96, 2005.
[7] Jasna D. Markovic-Petrovic and Mirjana D. Stojanovic. Analysis of SCADA system vulnerabilities to DDoS attacks. 2013 11th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services (TELSIKS), 2013.
[8] Matthias Niedermaier, Dominik Merli, and Georg Sigl. A Secure Dual-MCU Architecture for Robust Communication of IoT Devices. 2019 8th Mediterranean Conference on Embedded Computing (MECO), 2019.
[9] Jurij Lelli, Claudio Scordino, Luca Abeni, and Dario Faggioli. Deadline scheduling in the Linux kernel. Software: Practice and Experience, 46(6):821–839, 2015.
[10] Thomas Gleixner, Clark Williams, and John Kacur. CyclicTest, 2020.
[11] Linutronix. Real-Time Linux Continuous Integration, 2019.
[12] Siro Arthur and Nicholas Guire. Assessment of the Realtime Preemption Patches (RT-Preempt) and their impact on the general purpose performance of the system. 9th OSADL Real-Time Linux Workshop, 01 2007.
[13] Jeremy Brown and Brad Martin. How fast is fast enough? Choosing between Xenomai and Linux for real-time applications. 12th OSADL Real-Time Linux Workshop, 2010.
[14] Morten Mossige, Pradyumna Sampath, and Rachana Rao. Evaluation of Linux rt-preempt for embedded industrial devices for Automation and Power Technologies - A Case Study. 9th RTL Workshop, 01 2007.
[15] Hermann Kopetz. *Real-time Sytems: Design Principles for Distributed Embedded Applications*. Springer US, 2011.

[16] Buildroot. Buildroot, 2019.

[17] STMicroelectronics. STM32MP157C-DK2 Discovery kit with STM32MP157C MPU, 2020.

[18] Saleae Inc. Saleae logic analyzer, 2020.

[19] Gordon Lyon. Nmap.