Mitigate Parasitic Resistance in Resistive Crossbar-based Convolutional Neural Networks

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Traditional computing hardware often encounters on-chip memory bottleneck on large-scale Convolution Neural Networks (CNN) applications. With its unique in-memory computing feature, resistive crossbar-based computing attracts researchers’ attention as a promising solution to the memory bottleneck issue in von Neumann architectures. However, the parasitic resistances in crossbar deviate its behavior from the ideal weighted summation operation. In large-scale implementations, the impact of parasitic resistances must be carefully considered and mitigated to ensure circuits’ functionality. In this work, we implemented and simulated CNNs on resistive crossbar circuits with consideration of parasitic resistances. Moreover, we carried out a new mapping scheme for high utilization of crossbar arrays on convolution, and a mitigation algorithm to mitigate parasitic resistances in CNN applications. We demonstrated the proposed methods with implementations of a 4-layer CNN on MNIST, and residual neural network (ResNet) (20, 32, and 56) on CIFAR-10. Simulation results show the proposed methods well mitigate the parasitic resistances in crossbars. With our methods, modern CNNs on crossbars can preserve ideal (software) level classification accuracy with 6-bit ADCs and DACs implementation.

CCS Concepts: • Computing methodologies → Neural networks; • Hardware → Emerging simulation;

Additional Key Words and Phrases: Resistive crossbar, convolutional neural network, parasitic resistance

1 INTRODUCTION

Convolutional Neural Networks (CNN) have led to many performance breakthroughs in image classification, video object tracking, and audio processing applications [19]. Since AlexNet won the Large Scale Visual Recognition Challenge (ILSVRC) 2012 [18], CNNs have evolved into many different models, such as GoogLeNet [32], VGG [30], and residual neural network (ResNet) [11]. Using Graphics Processing Units (GPUs) and specific accelerators to accelerate convolutions play an important role in CNNs’ success, since convolutions dominate the overall computation.
Interestingly, in many machine learning applications, throughput of convolutions comes prior to computing accuracy, especially on inference functions [9]. Inspired by this feature, Nvidia’s recent GPUs [13], Cambricon-X [43], and many other accelerators (such as Cambricon MLU100 [34], Xilinx FPGA-based accelerator [26]) start supporting half-floating point or even 8-bit integer precision to accelerate convolutions without performance degradation in many neural networks.

However, modern computing hardware often encounters an on-chip memory bottleneck when dealing with high volume convolutions in large-scale CNNs [3, 28]. State-of-the-art convolution neural networks require a tremendous amount of parameters to handle complex tasks. For example, AlexNet has 2.3 million parameters, VGG has 14.7 million parameters, and ResNet-152 has 25.5 million parameters [3]. Storing such an amount of parameters into limited caches is impossible. Therefore, frequent cache flushing and weight loading from off-chip memory (usually DRAM) are usually inevitable, which leads to significant delay and energy cost.

To overcome the memory bottleneck, many researchers show interest in resistive crossbar arrays for the computing-in-memory feature [1, 8, 14, 21, 25, 41]. The resistive crossbar is defined as a circuit structure with vertical and horizontal metal lines sandwiching a resistive switching material at their intersection. The cross-point material could be memristor [31], phase change memory (PCM) devices [37], floating gates [4], spintronic devices [35], Resistive random-access memory (ReRAM) [36], Static random-access memory (SRAM) [27], or any other devices with programmable resistance. By utilizing Kirchhoff’s current law (KCL) and Ohm’s law, an ideal resistive crossbar array can carry out analog vector-matrix-multiplication (VMM). The outputs of analog VMMs are represented as the analog output currents from columns of the crossbar, with input voltage signals flowing through rows, and weights are stored non-volatility as conductance in cross-point. In the inference stage, any size of VMMs can be easily done in a single step. Moreover, since weight storage and weighted multiplication/summation both happen at the same place—the crossbar array—it enables ultra-high computing efficiency on multiplications between changing vectors (data) and fixed matrices (weight), which is ideal for implementing ultra-low power inference functions of neural networks.

However, as the array scales up, circuit parasitics deviate the crossbar from its ideal linear behavior and bring the non-negligible error to the computing result. The impact of circuit parasitics, especially parasitic resistances such as wire resistance and interconnect resistance, have been observed and analyzed in many simulations and experiments [2, 6, 15]. Currently, the impact of parasitic capacitance and inductance can be ignored since they mainly affect transient behavior of the crossbar, while in-memory computing mainly depends on crossbars’ DC behavior. It is important to consider parasitic resistance in circuit simulations for practical and functional implementations, especially for neural network applications where many large-scale crossbars are used.

In this article, we investigate crossbar-based large-scale CNN implementation with consideration of parasitic resistances and provide methods to mitigate its impact on convolution accuracy as well as CNN classification accuracy. Our major contributions include:

— First, we invent an efficient implementation method to densely map high-dimension 4-D kernels to 2-D crossbar arrays. Using this method, a crossbar designed for vector-matrix multiplication can be easily adapted for convolution with near-zero hardware overhead.
— Second, we model a resistive crossbar array with consideration of parasitic resistances and realistic device models. The simulation result is also verified with experiment data up to a 128×64 crossbar size.
— Third, we study the impact of parasitic resistances and provide a mitigation method to minimize computing error due to parasitic resistances as well as data/kernel patterns in CNNs without re-training.
Last, but not least, we demonstrate our methods for a 4-layer CNN on MNIST, and Resnet-20, 32, and 56 on CIFAR-10.

Compared to other state-of-the-art crossbar simulators, our work conducts the end-to-end full circuit simulation on modern CNN models and large datasets with the consideration of circuit parasitics and realistic memristor models. Our work firstly shows that with realistic crossbars and other peripheral circuits (DAC+ADC), errors will propagate in deep CNNs due to mixed signal processing and nonlinear activations (ReLU).

Our result shows that, with the proposed implementation and mitigation methods, 8-bit ADC/DAC resolution may be good enough to preserve the software-level classification accuracy in deep CNNs.

The rest of article is organized as follows: Section II covers the background. Section III details the methodology of the implementation and mitigation methods. Section IV gives simulation result on single crossbar as well as crossbar-based CNNs. Section V concludes the article.

2 PRELIMINARY

2.1 Convolutional Neural Network

Figure 1 shows a typical structure of CNN models. It has three key components: convolutional layers, pooling layers, and fully connected layers [19]. Each convolutional layer consists of a set of kernels that have identical sizes. It can be used to detect the local spatial correlation in input patterns. The output of convolution is passed to a non-linear activation function such as ReLU or sigmoid to form new feature maps. A pooling layer acts as a down-sampling filter for the output of the activation function. A pooling layer not only reduces the size of the feature map but also merges similar features. As a result, it helps to reduce the number of parameters as well as alleviate over-fitting. The output from the pooling layer then feeds into the next convolution layer. Fully connected (FC) layers usually appeared at the last few layers of CNNs as the classifier. They weight every point in the high-level feature maps and generate the final classification result.

In this work, we are targeting deep ResNet on resistive crossbar arrays, as it is one of the state-of-the-art CNNs on image classification problems. ResNet was firstly introduced in ILSVRC 2015 [11]. It keeps the benefit of deeper layers while addressing the degradation issue by optimizing the residual mapping with shortcut connections between layers. An ensemble of residual nets up to 152 layers has achieved 3.57% error on the ImageNet test set and won first place at the ILSVRC 2015 classification competition. Figure 2 shows the basic block diagram of ResNet. It combines multiple convolutions, batch normalizations, and rectified linear units (ReLU) together as its basic building block. Different from other CNNs, ResNet uses a shortcut to directly add input data to the output result of a block. Since two data inputs may have different dimensions at the summation stage, a $1 \times 1$ convolution layer is introduced in the shortcut to match the dimensions of two inputs. The summation result is fed to ReLU and passes to the next Block. At the end of...
ResNet, the pooling layer, one or more FC layers, and a softmax layer are used in sequence to generate the final classification result. By studying and optimizing resistive crossbars for ResNet, we can get more insight into the performance of resistive crossbar-based computing on modern CNNs.

2.2 Resistive Crossbar Circuit for VMM Computing

Figure 3 illustrates the general structure of resistive crossbar array for VMM computing. In an ideal crossbar, when applying voltage inputs $V$ at the rows simultaneously and reading current outputs $I$ from the columns, the input-output relationship of the crossbar can be represented as below:

$$I = VG$$

In this way, the analog weighted summation is achieved through Kirchhoff’s Current Law and Ohm’s Law. By mapping input vector $X$ to input voltage $V$, positive matrix $A$ to conductance $G$, and output current $I$ back to output result $Y$, a memristor crossbar can be regarded as an analog VMM module to realize $Y = XA$ in one step. Note that $I = VG$ is only valid for ideal crossbar where parasitic resistances can be ignored, and device conductance is independent of the voltage/current.

In realistic crossbar arrays, circuit parasitics, including wire resistance, input/output resistance, device I-V non-linearity, and parasitic capacitance, deviate crossbar’s behavior from ideal vector-matrix multiplication. For instance, the wire resistance degrades the signal along the row and column wire, so the device on the further corner will receive signal less than expected due to increased wire resistance. Input/Output resistance act similarly as wire resistance, but they could cause even larger signal degradation since they are usually caused by pass transistors and more resistive than wires. Meanwhile, cross-point device I-V non-linearity affects its multiplication accuracy, as its conductance is no longer independent of voltage or current. The impact of capacitance and inductance can be ignored at the current stage since they mainly affect the transient behavior of the crossbar while we are using the crossbar’s DC behavior to realize analog VMM at a relatively low frequency (10M to 100MHz).

2.3 Mapping Algorithms for Crossbar Array

When using the crossbar array as the VMM circuit, the first problem is how to map the matrix onto the crossbar. Since the intersection conductance and column output current cannot be the negative value, the mapping method needs to be able to address the negative issue. One common way is using the positive and negative power supply, and matrices are mapped on crossbar array in absolute form. For the negative element in the matrix, the negative input voltage is applied to the corresponding position. Recently, Chris Yakopcic et al. have proposed a way to implement convolution and CNN on memristor-based crossbar [39, 40]. In their ex-suit process, convolutional...
Table 1. Crossbar-based NN Simulator Comparison

| Simulator | Experiment-verified | Full circuit simulation | MNIST | CIFAR-10 | NN type | Non-ideal effects | Method to rescue IR-Drop |
|-----------|---------------------|-------------------------|-------|----------|---------|------------------|--------------------------|
| MNSIM [38] | x | x | x | x | MLP,CNN | Consider wire resistance into simplified parallel resistance | x |
| NeuroSim [5] | x | x | ✓ | x | MLP | Wire RC considered in nearby synaptic cell | Setting a small IR_DROP_TOL |
| PytoX [12] | x | x | x | ✓ | CNN | Simplified nodal analysis for wire resistance, stuck-at-fault, thermal & shot noise | Re-training with IR-drop consideration |
| FNNNA [24] | x | x | ✓ | ✓ | CNN | Programming error, stuck-at-fault | Retraining with error correction output code |
| DPE [15] | ✓ | ✓ | ✓ | x | MLP | SPICE-level analysis with transistor models, circuit parasitics, and actual memristor models | Conversion |
| Our simulator | ✓ | ✓ | ✓ | ✓ | CNN | SPICE-level analysis with transistor models, circuit parasitics, and actual memristor models | Conversion and Calibration |

Kernel G has to be divided into two parts, positive $G^+$ and negative $G^-$. All negative values in $G^+$ have been replaced by zero. And those negative values have been mapped in $G^-$ as positive conductance. By providing $G^-$ the identical inputs to $G^+$ but with reversed sign, the memristor-based crossbar can deal with the matrix, which contains negative values.

Reference [7] also maps the absolute value of the matrix on the crossbar array. However, it needs two adjacent columns of the crossbar to represent a single column of that matrix. One represents the positive part, and another represents the negative part. Then, the two columns have output currents $I^+$ and $I^-$, respectively. Final output $= I^+ - I^-$. Reference [16] uses another way to solve this negative issue in their ReRAM crossbar-based processing element (PE). The positive and negative parts of the matrix are still mapped on two adjacent columns of a crossbar. But the negative voltage input is unnecessary in this design. Instead, an extra subtracter component is needed for every pair of positive and negative columns. Another change in this design is that it uses spiking schema to improve the output precision. $2^n$ spikes are used to represent a number of $n$ bits.

In the above mapping schemes, either extra overheads or redundant crossbar areas are needed. Moreover, for all above implements, a rigorous full circuit simulation with consideration of parasitic resistances on a large enough CNN is still missing.

### 2.4 Crossbar-based Neural Network Simulator

There exist a lot of crossbar-based simulators for neural network applications with the consideration of parasitic-effect, stuck-at-fault, thermal noise, and more. However, most of those simulators are not experiment-verified and even over-simplified for the non-ideal effects. Table 1 compares state-of-the-art crossbar-based NN simulators. Our simulator is the only circuit simulator that is experimentally verified and works on a large-scale dataset and NN models.

MNSIM [38] and NeuroSim [5] are two famous ReRAM crossbar simulators. They count many non-ideal effects into consideration, but they do not focus on accurate crossbar computation output due to lack of full analog circuit simulation. However, they could give a reasonable power/area estimation for crossbar-based design. Moreover, they are designed for general crossbar-based neural networks not optimized for convolution neural networks.
PytorX [12] and FTNNA [24] are designed for neural network applications with the consideration of non-ideal effects. They also have the ability to alleviate the impact of those non-ideal effects and have been demonstrated on large datasets. However, such rescue ability is given by the error tolerance of NN models rather than the optimization of simulators, since both need to re-train the model to assuage the non-ideal effects. Practically, we cannot guarantee that all crossbars have the same non-ideal effects, and those effects may vary because of different crossbar size, stored conductance matrix, wire resistance, and so on. Re-training for every crossbar device is a plausible way to solve such non-ideal effects, but they may not always be practical due to time/energy limitation. Moreover, online training for large-scale NNs requires deep understanding and very accurate modeling of memristor dynamic behaviors, which is still far from enough at this moment. Even if we do training with existing memristor models, the learning we can get from it is questionable because the model is still very different from realistic device behaviors and does not account the impact of realistic process variations and noises.

In this work, we developed an experiment-verified simulator to conduct the end-to-end SPICE-level analog crossbar circuit simulation with the consideration of circuit parasitics and realistic memristor models. Conversion and calibration methods are used to mitigate the parasitic effects in crossbar-based computing. Compared to other simulators, our work not only shows the impact of non-ideal effects on NN model accuracy, but also explains the reasons behind such accuracy degradation by investigating the error propagation in crossbar-based deep CNNs. In this way, our work provides a more solid upper-bound for the inference performance of crossbar-based CNNs respecting different design parameters.

3 METHODOLOGY

There are two challenges ahead of using resistive crossbars for convolution operations. The first challenge is how to transform high dimensional convolution kernels to 2-D matrices for resistive crossbars. The most straightforward way converts convolution kernels to Toeplitz matrices. However, the Toeplitz matrix is sparse, and its sparsity significantly grows with larger kernels. Directly mapping this sparse matrix to resistive crossbars will cause large hardware overhead as well as computing accuracy concerns. The second challenge is how to mitigate parasitic resistances in crossbar-based computing. As introduced before, parasitic resistances in the crossbar will cause nonlinear signal degradation at each cross-point device; a lack of considering its impact will cause unacceptable errors in computing the results of large crossbar arrays. To solve both challenges, we present the dense mapping as the new mapping method to fully unitize crossbar arrays with near zero hardware overhead, and the mitigation algorithm to compensate parasitic resistance in large-scale crossbars.

3.1 Dense Mapping for Crossbar-based Convolution

The critical step of mapping an arbitrary matrix \(A\) on a crossbar is how to deal with negative values in \(A\), as conductance cannot be negative. We first shift all elements in \(A\) by a constant \(A_{\text{Shift}}\) to make sure of no negative value in \(A\). Such a shift can be easily removed at the final step by subtracting \(A_{\text{Shift}} \times \text{sum}(X)\) where \(\text{sum}(X)\) is the summation of the input. By doing so, we do not need to part the matrix into positive and negative sub-matrices, and any VMM can be performed on the crossbar with much less overhead.

When we use a crossbar for VMM computing in a digital circuit environment, ADC/DAC are necessary to convert input data to analog voltage and output current to digital form. This process usually assumes to be 10ns to 100ns, which is usually limited by the ADC speed. To get \(\text{sum}(X)\), an accumulator works in parallel with the DAC->crossbar->ADC system with similar speed. For small or medium size crossbars, a digital accumulator would be more efficient to calculate the
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Fig. 4. Dense mapping for input data size (j,k,p), where j,k,p means data height, width, and channel, respectively. The circuit needs j*k iterations to process the input data.

summation of input vectors; For large crossbars, an analog accumulator can be implemented by using an additional column in the crossbar array where its devices are programmed to the same conductance, and it is sensed by an additional ADC. With either method of accumulator design, the cost and hardware overhead on calculating sum(X) is much lower than using two crossbars or two devices to track negative values.

In CNN, each convolution layer has a 4-D kernel. For example, a 3*3*3*16 kernel means it has 16 sets of 3*3*3 3-D kernels, and each 3-D kernel contains three 2-D kernels for the three channels (RGB) of color images. To perform convolution on the memristor crossbar, we need to convert high-dimensional convolution into 2-D VMM. It is well known that 2D convolution can be implemented using matrix multiplication by converting kernel to a Toeplitz matrix. Toeplitz matrices are sparse matrices that contain many zeros, so we named this method sparse mapping.

However, sparse mapping has three major issues: First, memristor crossbar is by nature a dense array structure with positive values, not efficient for sparse matrix implementation. Mapping a sparse matrix to crossbar means that those memristors assigned with zero would do nothing but add error to the final result due to the leakage current, as well as waste circuit area. Second, sparse mapping requires a huge crossbar array, which is not always feasible, and vulnerable to noise and defects. Third, sparse mapping requires a sizeable peripheral circuit to support the enormous array. Since the peripheral circuit dominates the total power/area, the hardware implementation of sparse mapping would be too costly to afford.

In contrast to sparse mapping, we developed a new method, named as dense mapping, targeting on using small and dense memristor crossbars to implement convolutions efficiently. Figure 4 illustrates the concept of dense mapping. Each 2-D kernel is unrolled to a vector and mapped to one column of crossbar so that one crossbar can implement multiple 2-D kernels as long as it has enough columns. For input signal, only data within the convolution window are fed to the row inputs of crossbar arrays. When input data has multiple feature channels, each output feature channel needs a 3-D convolution kernel. A 3-D convolution kernel can be treated as many 2-D kernels. Every 2-D kernel corresponds to one input channel. The output of 3-D convolution is given by performing convolution on all 2-D input channels and adding them together. Thus, we can unroll every 2-D kernel in the 3-D kernel as the same order. It is then cascading all vectors together to form a single column on a crossbar. An input shift register stores the unrolled input data within the convolution window (multiple input channels cascaded like the kernel on a crossbar) at the current iteration to feed to the crossbar, then updating its storage as the window moves through the entire data space. The convolution results for data within the convolution window are collected at the column outputs of the crossbar. In this way, a single convolution kernel with
Table 2. Overhead Comparison for Dense and Sparse Mapping

| Kernel Size         | xbar size (dense&sparse) | xbar power (mW) | xbar area (mm²) | ADC number | DAC number | Total power (mW) | Total area (mm²) |
|---------------------|--------------------------|-----------------|-----------------|------------|------------|-----------------|-----------------|
| 3x3x3x16            | 27 x 16                  | 0.06            | 0.000005        | 1          | 27         | 29.06           | 0.001           |
|                     | 3,072 x 14,400           | 6,480           | 0.54            | 113        | 3,072      | 9,778           | 0.806           |
| 3x3x16x16           | 144 x 16                 | 0.34            | 0.000028        | 1          | 144        | 146.34          | 0.007           |
|                     | 16,384 x 14,400          | 34,560          | 2.88            | 113        | 16,384     | 51,170          | 3.712           |
| 3x3x32x32           | 288 x 32                 | 1.35            | 0.000113        | 1          | 288        | 291.35          | 0.014           |
|                     | 8,192 x 6,272            | 7,526.4         | 0.6272          | 49         | 8,192      | 15,816.4        | 1.034           |
| 3x3x64x64           | 576 x 64                 | 5.4             | 0.00045         | 1          | 576        | 583.4           | 0.026           |
|                     | 4,096 x 2,304            | 1,382.4         | 0.1152          | 18         | 4,096      | 5,514.4         | 0.311           |

one stride on both horizontal and vertical direction needs \((j - m + 1) \times (k - n + 1)\) iterations where \(j, k / m, n\) are data/kernel height and width, respectively. Since multiple input channels have been compressed in a single column on a crossbar, the input channel number doesn’t impact the iteration time.

Comparing dense mapping to sparse mapping, it is a tradeoff between time complexity and space complexity. Sparse mapping uses much more extra hardware to produce the result in parallel without iteration. From the data movement aspect, the least movement mapping method is sparse mapping. It uses extra space in crossbar to not only store weight in there but also perform the kernel window movement. However, its efficiency exponentially drops as data/kernel size scales up because more devices in a rectangular crossbar are unused for increasing data/kernel size.

And much larger crossbar and more ADC/DACs are required for sparse mapping a large data/kernel. Table 2 compares the overhead of dense and sparse mapping on common used data/kernel sizes from ResNet. In Table 2, crossbar and ADC/DAC parameters are adopted from ISAAC [29]. We exponentially scaled the DAC to 8-bit, then proportionally scaled the area and power for crossbar, ADC, and DAC, respectively. Although we could partition a huge matrix into multiple small matrices [23], sparse mapping still needs 100x more numbers of DACs and ADCs than dense mapping.

Therefore, dense mapping is an adequate and more practical method compared to sparse mapping. It not only achieves 100% usage of devices, but is also easy to implement and provide sufficient performance in speed for CNN applications. From Figure 5, one classification inference in ResNet-20 needs 9,089 iterations in sequential order, if no parallel copies of hardware are used. Note that summation (sum#) is in parallel of convolutions, so it’s not counted in total iterations. Assuming a crossbar runs at 100 MHz [15], for each classification, the convolution part takes only 0.09 ms, which is fast enough for a real-time classification requirement.

3.2 Crossbar Simulation with Parasitic Resistances

Figure 6 shows the circuit structure of one-transistor-one-memristor (1T1M) crossbar for vector matrix multiplication (VMM). In this structure, memristor crossbar is the core component as it enables analog current weighted summation, which leads to ultra-efficient VMM operation. A \(m \times n\) memristor crossbar is made by \(m\) row and \(n\) column metal wires where memristors are formed at intersecting points. Each memristor can be tuned to arbitrary conductance within its programmable range. To enable precise, non-disturbing tuning in large crossbar arrays, the 1T1M cell is necessary to program the entire array with arbitrary conductance matrix \(G\).
Fig. 5. Flowchart of a 32 by 32 image in ResNet20.

Besides memristor crossbars, DACs/ADCs are also essential to ensure accurate VMM operation. First, they are necessary to integrate a memristor-based analog VMM module into the digital environment, as functions like pooling, ReLU, and normalization still need digital implementation. Second, the calibration step can be performed at the ADC/DAC stage to improve crossbar results further. Last but not least, ADC provides quantization, which is helpful in filtering out the output error of memristor-based analog VMM modules, to prevent the error accumulation of inter- and intra-layers in CNNs.

Compared to previous simulation work on memristor crossbar arrays, we considered parasitic resistances including wire resistances, input/output resistances, and intersection resistances in our simulation model. With consideration of parasitic resistances, we can observe the signal degradation along rows and columns in the array, as shown in Figure 8. The low input signals applied on further corner memristors also make the column current output lower than expectation. To guarantee the actual output close to the ideal output, we adopt an experiment verified method [14]. Instead of mapping conductance $G$ to a crossbar, we map a tweaked conductance matrix $G'$ with consideration of parasitic resistances in the crossbar. To find $G'$ for a $m \times n$ crossbar, we first need to formulate all $3m \cdot n + 2m + 2n$ KCL equations from the crossbar circuit model to solve all node voltages, including $m \cdot n$ cross-point top nodes, cross-point middle nodes (between memristor and access transistor), cross-point bottom nodes, and $2m + 2n$ boundary nodes on both ends of horizontal and vertical lines. Then, as conductance $G'$ has $m \cdot n$ unknown variables, we add $m \cdot n$ new equations $I_m = V \odot G$ as new limitations to force each cross-point to pass the ideal current. Where $I_m$ is the cross-point current for each memristor, $V$ is the ideal cross-point voltage between top nodes and bottom nodes, and $\odot$ denotes Hadamard product, or say element-wise multiplication. Finally, with $4m \cdot n + 2m + 2n$ nonlinear equations, $G'$ can be solved with HSPICE or any nonlinear equation solver. As shown in Figure 7, the simulation result well matches the experiment result of a 128×64 array.

3.3 Mitigation Algorithm for Parasitic Resistance

Algorithm 1 summarizes the flow of crossbar-based convolution with the mitigation algorithm. Table 3 explains the important functions in the algorithm. After initialization, if the kernel is already mapped and converted onto crossbars, it will directly jump to the computing step to simulate crossbar-based convolution. So, we only need to map the conductance matrix once for CNN inference.
Fig. 6. Crossbar model with consideration of parasitic resistance.

Fig. 7. 1T1M simulation and experiment result [14]. Wire segment resistance is calibrated to 1Ω; transistor and memristor models are calibrated with in-array device test.

Fig. 8. Signal degradation along rows and columns in crossbar. (a) 0.2V signal imported into crossbar from the very left point on each row. (b) Current degradation along columns in crossbar. Due to parasitic resistance, the further column has lower voltage and current than what is ideal.

Table 3. Explanations for Functions in Algorithm 1

| Function     | Explanation                                                                 |
|--------------|-----------------------------------------------------------------------------|
| CrossbarSim  | Experiment verified crossbar simulator from Ref. [14]                      |
| Conversion   | Solve $V_{\text{conv}} \cdot G = \text{CrossbarSim}(V_{\text{conv}}, G')$ to get $G'$. |
| GetCaliPara  | Get first-order poly-fitting result $P$ by fitting crossbar output to ideal output of calibration samples. |
| Calibration  | Use $P$ and $\text{InputVector}[i]$ to map $I_{\text{out}}[i]$ to $\text{Output}[i]$. Here, $\text{InputVector}[i]$ is needed because in VMM $Y = XA$, if $A$ contains negative values, $Y$ can be calculated by $Y = X(A + c) - c \cdot \text{sum}(X)$, while $c$ is a large enough scalar to shift $A$ to all positive. |

3.3.1 Data and Kernel Pattern. Input data has high sparsity after the ReLU layer. Figure 9 shows the data sparsity at each convolution layer of ResNet-20. The impact of data sparsity should be considered when choosing the conversion signal as well as gathering calibration samples.

Similarly, we found that kernels in CNN have different distributions. In Figure 10, we list three typical kernel types regarding their weight value distributions. Kernel type 1 refers to a weight...
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3.3.2 Optimize Conversion Signal. To better quantify the computing accuracy, we define Output Error and Relative Error as below:

\[
\text{Output Error} = \frac{\text{ActualOutput} - \text{IdealOutput}}{\text{Output Range}}
\]

\[
\text{Relative Error} = \text{abs}(\text{Output Error})
\]

while ActualOutput is the crossbar output in our simulator. IdealOutput is the expected correct result of the same kernel and input data. Output Range is the ideal convolution output range for each kernel. Relative error is the absolute value of output error, and it can be converted to output bit accuracy as below:

\[
\text{Bit Accuracy} = \log_2(1/\text{Relative Error} + 1)
\]

The conversion step is fine-tuning crossbar conductance from \( G \) to \( G' \) to compensate the parasitic resistances. The original conversion algorithm \([15]\) takes the maximum input vector as its conversion signal, which works well with dense matrix and dense input signals. However, in CNN, we need to consider the sparsity of data/kernel to optimize the conversion signal. By testing different conversion signals across different kernels, we notice that the amplitude of conversion signal is critical, while the sparsity of the conversion signal is not as important. Figure 11 shows the relative distribution close to Gaussian. Usually, it happens when training algorithms put no particular limitation on weight values, such as ResNet. Kernel type 2 refers to the training algorithm that prevents weight values from going near zero \([10]\). Kernel type 3 refers to Ternary Neural Networks where weights can only be -1, 0 (sparse), or 1 \([22]\). It’s worth investigating how different kernel types in CNN impact the quality/precision of crossbar-based convolution.
error distribution with different conversion signal amplitudes in crossbar with size $144 \times 16$. We found that a conversion signal with too large amplitude (all 1) will cause overcompensation for crossbar conductance matrix due to circuit parasitic, and a too-small conversion signal (all 0.001) does not have enough compensation, and both of them result in obvious output error. A bad conversion signal may cause hundreds of times of error than a good conversion signal ($\pm 20\%$ in all 1 signal versus $\pm 0.2\%$ in all 0.1 signal). So, for crossbar size $144 \times 16$, all 0.1 signal appears to be the best conversion signal, and other conversion signals close to it generate similar error distribution.

3.3.3 Calibration. In addition to the original conversion algorithm, we add a calibration stage to improve the result further. It randomly picks 10 samples from the input dataset and runs a first-order polynomial fit to fit the crossbar output to the ideal output. The generated fitting vector $P$ is fixed per crossbar and can be easily embedded in ADC/DAC configurations. Figure 12 shows the
relative error with different calibration signals, and shuffled input patterns achieve the best result in all four sets of different calibration signals.

4 RESULT
4.1 Simulation Setup
In this work, convolution and fully-connected (FC) layers are implemented by analog crossbars with the digital interface. Other functions, such as pooling, ReLU, batch normalization, and so on, are processed by digital circuits. The CNN is offline-trained; then, its kernels are converted to the conductance of crossbar for inference. Similar to our previous work [42], our crossbar parameters are listed below: lowest resistance $R_{on} = 15k\Omega$, highest resistance $R_{off} = 300k\Omega$, wire resistance per segment is set to 1\(\Omega\), input/output resistance of crossbar is set to 1\(\Omega\). Input voltage range is [0, 0.4V]. The sensing voltage for device conductance is 0.2V. The CNN framework used in this work is MatConvNet [33].

4.2 Individual Convolution Layer Simulation
We first run circuit simulation at the individual convolution layer to study the impact of input data sparsity, kernel type, and crossbar size on convolution accuracy.

Figure 13 shows the output distribution with different input sparsity and different mapping algorithms in a 144 × 16 crossbar, which stores a 3*3*16*16 convolution kernel. If just using linear mapping without any consideration of circuit parasitics, the crossbar result deviates far away from the ideal outcome. Our mitigation algorithm demonstrates better performance compared to the original conversion algorithm in all cases. The result overlaps well on the y = x trend-line with different input sparsity. The original conversion algorithm can force the output to get close to the ideal output. But as the sparsity goes up, the original conversion algorithm loses its ability to amend the result.

Figures 14–17 illustrate the impact of input data sparsity on different sizes of crossbars. There are three observations: first, our method provides ~50% better overall accuracy than the original conversion algorithm. Second, our method gives a lower mean relative error when the ideal value is small. Third, our method minimizes the impact of data sparsity comparing to the original conversion algorithm. Figure 18 summarizes the mean/worst relative error across the aforementioned
three kernel types with different input sparsity and crossbar sizes. In short, the result shows that our method is independent of kernel types and data sparsity, and achieves the best accuracy overall.

### 4.3 End-to-end CNN Circuit Simulation

CNN contains more than one layer, any error in one layer will propagate and accumulate to the next layer. It is essential to analyze how error propagates and accumulates in deep neural networks, and evaluate their impact on the final classification result. For MNIST [20], we trained a CNN with four convolution layers. Table 4 summarizes the kernel information, corresponding crossbar sizes, and the conversion signal for each layer. Note that for larger crossbars, a conversion signal with smaller amplitude tends to ease the calculation of $G'$, and provides $G'$ with better quality (higher VMM accuracy). It is because, in the conversion process, conversion signals are used for the initialization of node states in crossbar simulation. For example, we initialize all top voltage nodes to be its row input voltages. Large conversion signal is okay for small- to medium-sized crossbar arrays since the signal degradation along wires is not too significant. However, in large crossbar arrays, the node voltage of devices in further corners are significantly different from the ideal values due to notable parasitic resistance. Initializing these nodes with ideal values not only makes the solver take more iteration to complete, but also may lead to non-convergence issues due to lousy initialization, observed as extremely large or even negative values in $G'$. In practice, we found that as the crossbar size goes up, the lower conversion signal helps the algorithm to compute the $G'$ quickly in the appropriate range.
Fig. 18. Mean/worst relative error with different kernel types, data sparsities, and crossbar sizes.

Table 4. Simple CNN Convolution Layer Kernel Size, Crossbar Size, and Corresponding Conversion Signal Amplitude

| Layer | Kernel Size   | Crossbar Size | Conversion signal |
|-------|---------------|---------------|-------------------|
| Conv1 | 5*5*1*20      | 25 * 20       | 0.1               |
| Conv2 | 5*5*20*50     | 500 * 50      | 0.01              |
| Conv3 | 4*4*50*500    | 800 * 500     | 0.001             |
| Conv4 | 1*1*500*10    | 500 * 10      | 0.01              |

Fig. 19. Error propagation along layers in a simple neural network (four convolution layers) with the MNIST dataset, solid lines represent mean error, dash lines represent worst error.
Figure 19 shows the error propagation at each convolution layer for MNIST. Different ADC/DAC quantization bit-resolutions are applied to restrict error propagation. As a result, we can see that 6- and 8-bit quantization both can prevent error accumulation after the third layer. Another observation is that non-quantization (direct analog forwarding) makes the error even lower than 8-bit.

We further tested 4,000 images from MNIST validation dataset with a different quantization setting. The testing results are given in Table 6. With 8-bit quantization, final classification accuracy is remaining at 98.8%, which is less than 1% difference than the ideal (software) result (99.1%).

We further implement the state-of-the-art CNN, ResNet on CIFAR-10 [17] to explore the impact of error propagation in modern deep neural networks. ResNet-20, 32, and 56 all consist by following types of convolution layers: first a convolution layer connected with input has convolution kernel size $3\times3\times16$, then a bunch of layers followed with kernel size $3\times3\times16, 3\times3\times32, 3\times3\times64$, respectively. Second, an additional convolution layer is added between different kernel sizes to match the matrix dimension. Its size depends on nearby convolution layers but with a fixed convolution window (1 by 1) on the feature map. The last convolution layer is the fully connected layer that has the kernel size $1\times1\times64\times10$. Besides the last FC layer and dimension matching layer, convolution layers in ResNet use the same $3\times3$ convolution window in their every channel. It means for each channel, only nine memristors in the same column are needed to perform the convolution operation. Due to such small convolution kernels and few feature channels in ResNet, even in 56 layers, the largest crossbar needed is still the same in ResNet-20 ($576\times64$).

In Table 5, we give the convolution kernel sizes, corresponding crossbar sizes, and the calibration signal amplitude for ResNets. In ResNet, some bypass branches use $1\times1$ convolution to match the matrix dimension. For those dimension matching layers, since kernels are tiny, we use the 0.1 calibration signal for all cases. Although the crossbar size in ResNet is much smaller than the CNN we used with the MNIST dataset, extra layers make it need more crossbars for inference. Circuit simulation for ResNet is slower than the CNN mentioned above for MNIST.
Table 5. ResNet Kernel, Crossbar Size, and Convolutional Signal Setting

| ResNet-20 | ResNet-32 | ResNet-56 | Kernel Size | Xbar Size | Conv. Signal |
|-----------|-----------|-----------|-------------|-----------|--------------|
| Conv1     | Conv1     | Conv1     | 3*3*3*16   | 27*16    | 0.1          |
| Conv2-7   | Conv2-11  | Conv2-19  | 3*3*16*16  | 144*16   | 0.1          |
| Conv8     | Conv12    | Conv20    | 3*3*16*32  | 144*32   | 0.1          |
| Conv9-13  | Conv13-21 | Conv21-37 | 3*3*32*32  | 288*32   | 0.05         |
| Conv14    | Conv22    | Conv38    | 3*3*32*64  | 288*64   | 0.05         |
| Conv15-19 | Conv23-31 | Conv37-55 | 3*3*64*64  | 576*64   | 0.01         |
| FC        | FC        | FC        | 1*1*64*10  | 64*10    | 0.1          |

Table 6. Classification Accuracy with Different Quantization Levels

| Network             | Software | non quantization | 4-bit | 6-bit | 8-bit |
|---------------------|----------|------------------|-------|-------|-------|
| ResNet-20 (CIFAR-10)| 89.3%    | 88.7%            | 11.3% | 82.7% | 90.7% |
| ResNet-32 (CIFAR-10)| 89.3%    | 89.3%            | N/A   | 82%   | 90%   |
| ResNet-56 (CIFAR-10)| 90%      | 88%              | N/A   | 88%   | 89.3% |
| LeNet (MNIST)       | 99.1%    | 98.9%            | 79.2% | 88.6% | 88.8% |

Limited by long circuit simulation time (each test image takes about 5 minutes), we use a subset of CIFAR-10, which contains 150 images as our test set. In Table 6, our experiments show that 8-bit quantization is a good balance between error suppression and information preservation, as it achieves even a slightly better classification result than software. A 4-bit quantization causes the error to accumulate through all layers and leads to a significant drop in final classification accuracy.

4.4 Impact of Programming Error

We modeled the programming error as conductance variations following zero-mean Gaussian distributions with sigma ranges from 0 to 1 $\mu S$ [14]. The devices’ conductance ranges from 3.3 $\mu S$ (300k ohm) to 66.7 $\mu S$ (15k ohm). We would like to emphasize that since crossbar-based computing is based on Ohm’s law and KCLs, computing results are carried by current. The error current is linearly proportional to the error in conductance rather than the error in resistance. Thus, a large resistance variation at a high resistance state may not cause a large computing error because the relative error in conductance is small. Figure 21 shows how a programming error affects the final classification accuracy of ResNet-20 on CIFAR-10 with different quantization levels. To conduct the simulation, we generate the programming error pattern with different sigma settings and add them to the conductance matrices. The calibration step is then performed on the programming error noise contaminated conductance matrix to update the fitting parameter P. The above configurations are stored for all input test data to make sure they all use the same crossbar setting.

When the programming error sigma $<0.4 \mu S$, ResNet-20 could still maintain the accuracy higher than 80%. Since the 0.4$\mu S$ is less than the 6-bit resolution under our configuration, the 6-bit quantization has minimal impact. While the non-quantization setting has the maximum accuracy degradation. As the programming error sigma increases, the quantization step could not prevent such error propagating between layers, and the classification accuracy drops dramatically.
5 CONCLUSIONS

In this work, we investigate how modern CNN performs on crossbar-based architecture with end-to-end circuit simulations with careful consideration of parasitic resistances. By studying CNN layer by layer, we find CNN’s characteristics, like data sparsity, cause existing crossbar-based optimization algorithms to be invalid. We propose dense mapping to achieve efficient convolution kernels to crossbar mapping. And we adapted and improved the original conversion algorithm for CNNs, which enables 0.25% mean relative error ($\sim 8.6$ bits) or 1.2% worst relative error ($\sim 6.4$ bits) for crossbar size $576 \times 64$. We performed a rigorous end-to-end circuit simulation for every convolution layer to give an accurate prediction of error propagation due to analog circuit errors. We find that 8-bit or even 6-bit ADC/DAC is necessary to prevent error accumulation in deep CNNs up to 50 layers, and they maintain the final classification accuracy. Simulation results also shows that our method is independent of input data sparsity and kernel type. It would be applied to general CNNs to improve their accuracy performance on crossbar-based architecture.

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