Abstract—Graph neural networks (GNN) analysis engines are vital for real-world problems that use large graph models. Challenges for a GNN hardware platform include the ability to (a) host a variety of GNNs, (b) handle high sparsity in input vertex feature vectors and the graph adjacency matrix and the accompanying random memory access patterns, and (c) maintain load-balanced computation in the face of uneven workloads, induced by high sparsity and power-law vertex degree distributions. This paper proposes GNNIE, an accelerator designed to run a broad range of GNNs. It tackles workload imbalance by (i) splitting vertex feature operands into blocks, (ii) reordering and redistributing computations, (iii) using a novel flexible MAC architecture. It adopts a graph-specific, degree-aware caching policy that is well suited to real-world graph characteristics. The policy enhances on-chip data reuse and avoids random memory access to DRAM.

GNNIE achieves average speedups of 21233 over a CPU and 699 over a GPU over multiple datasets on graph attention networks (GATs), graph convolutional networks (GCNs), GraphSAGE, GINConv, and DiffPool. Compared to prior approaches, GNNIE achieves an average speedup of 35 over HyGCN (which cannot implement GATs) for GCN, GraphSAGE, and GINConv, and, using 3.4 fewer processing units, an average speedup of 2.1 over AWB-GCN (which runs only GCNs).

I. INTRODUCTION

Deep learning accelerators have largely focused on data with Euclidean embeddings, e.g., audio/video/images/speech. Many real-world problems (e.g., network analysis, embedded sensing, e-commerce, drug interactions) use graphs to model relationships. Inferencing on large, unstructured, and sparse graphs with non-Euclidean embeddings requires specialized graph neural networks (GNNs). Today’s GNNs [14], [21], [33], [37] are based on nearest-neighbor operations, with lower computation cost than early approaches [5], [9], [21]. Though GNNs can be run on software platforms [1], [34], [39], high performance requires hardware acceleration platforms.

Multilayer GNNs perform two computation steps per layer: (a) Weighting performs a linear transform of vertex feature vectors through multiplication by a weight matrix. (b) Aggregation consolidates information from the neighbors of a vertex to compute the feature vectors for the next layer. The challenges in building GNN accelerators are as follows: (1) Versatility An accelerator should be able to handle a diverse set of GNNs to cover a wide range of GNN architectures to provide appropriate computation/accuracy tradeoff points for various applications. The achievable accuracy depends on the GNN: graph attention networks (GATs) achieve higher accuracy than other GNNs, but with more computation (Fig. 1). (2) Adjacency matrix sparsity The graph adjacency matrix encodes vertex neighborhood information required for Aggregation. The adjacency matrix is highly sparse (> 99.8% for all datasets in this paper; in contrast, DNN data shows 10%–50% sparsity). Unlike image/video data, adjacency matrix sparsity patterns typically exhibit power-law behavior, with vertex degrees ranging from very low (for most vertices) to extremely high (for very few vertices): in the Reddit dataset, 11% of the vertices cover 88% of all edges.

(3) Input feature vector sparsity The vertex input feature vectors are highly sparse, e.g., the 2708 input vertex feature vectors of the Cora dataset have 98.73% average sparsity. In Fig. 2 Region A is sparser than B and requires less computation, leading to load balancing issues during Weighting.

(4) Memory footprint and random-access patterns Real-world graphs have a large number of vertices and a massive memory footprint (Reddit: 2.3Gb in sparse format). High sparsity and power-law distributions can lead to random memory access patterns and poor data access locality in Aggregation.

Therefore, GNN-specific accelerators must address: (a) load balancing during Weighting, due to the sparsity variations in Fig. 2 and during Aggregation, due to the imbalance of computations for high- and low-degree vertices. (b) lightweight graph-specific caching of the adjacency matrix for high data access locality and maximal reuse of cached data.

Relation to other acceleration engines: The Weighting step performs matrix-vector multiplication which resembles convolutional neural network (CNN) computations, but CNN accelerators [2], [7], [15], [17], [18], [27], [30] are inefficient at handling graph data. Aggregation operates on graph neighborhoods and resembles graph analytics, but graph processing accelerators [8], [13], [19] are designed to perform lightweight computations, significantly lower than the needs of a GNN. Extensions of CNN/graph processing engines are inadequate.
An early GNN accelerator, HyGCN [38], bridges the divide by using two pipelined engines: an Aggregation engine that operates on graph data and consolidates vertex feature vectors from the neighborhood of each vertex, followed by a Combination engine, which uses a multilevel perceptron to weight the aggregated features with the weight matrix. The disparity between engines raises challenges in providing a steady stream of data to keep the Aggregation/Combination engine pipeline busy. The Aggregation engine does not account for power-law behavior while caching partial results, and high-degree vertices may create stalls due to the limited size of on-chip buffers. In the Combination engine, the aggregated feature vectors are both sparse and show high sparsity variations (Fig. 2). Consequently, stalls are required, leading to inefficiency.

AWB-GCN [12] views the GNN computation as two consecutive sparse-dense matrix multiplications (SpMMs). During Weighting, the method is targeted to moderate sparsity of 75% — but input layer vertex feature vectors are ultra-sparse (Fig. 2). During Aggregation, the graph-agnostic SpMM view necessitates numerous expensive off-chip accesses to the adjacency matrix. AWB-GCN addresses workload imbalances issues through multiple rounds of runtime load-rebalancing, but this leads to high inter-PE communication. Finally, SpMM-based approaches face more severe load imbalances for implementing GNNs that involve additional complex computations before Aggregation (e.g., softmax in GATs and DiffPool). In fact, AWB-GCN targets only GCNs and not general GNNs.

**Novelty of this work:** We propose the GNNIE (pronounced “genie”) architecture that uses a single engine that efficiently performs both Weighting and Aggregation. The GNNIE framework handles high levels of sparsity in the input vertex feature vectors and the adjacency matrix, with novel approaches for load balancing and graph-specific caching. It covers a number of GNN topologies, from lower accuracy/lower computation (e.g., GCN, GraphSAGE) higher accuracy/higher computation (e.g., GATs), as motivated in Fig. 1, and is more versatile than previous methods in handling functions such as softmax over a neighborhood (e.g., as used for attention normalization in GATs; prior work [4] on GATs, skips this crucial step).

Novel methods to mitigate sparsity effects, and overcome load imbalances and compute bottlenecks, include:

- **Load balancing during Weighting** based on splitting vertex feature vectors into blocks (Section IV-A). Together with load balancing (Section IV-C), this enhances throughput during Weighting by ensuring high PE utilization and skipping unnecessary computations, by (a) Recomputing on a flexible MAC (FM) architecture to address imbalances due to input feature vector sparsity variations. Computations are dynamically mapped to heterogeneous PEs, each with different numbers of MAC units. (b) *Static load redistribution* to nearby PEs, offloading computations from heavily-loaded to lightly-loaded rows, minimizing inter-PE communication.

- **Load-balanced edge Aggregation** (Section VI) through a mapping scheme that fully utilizes the PEs. For GATs, we further propose a novel linear-complexity computation that implements compute-bound attention vector multiplication similarly as Weighting, and memory-bound attention coefficient computation to maximize reuse of cached data.

**Lightweight graph-specific dynamic caching** (Section VI), fetching vertices in unprocessed degree order; aggregation operates on dynamic subgraphs formed by cached vertices. This new lightweight scheme is effective in avoiding the random DRAM accesses that plague graph computation.

**Speedups:** On five GNN datasets, results based on an RTL implementation and cycle-accurate simulation show that even including all of its preprocessing overheads, GNNIE delivers average speedups of 21233× over CPUs (Intel Xeon Gold 6132 + PyTorch Geometric), 699× over GPUs (V100 Tesla V100S-PCI + PyTorch Geometric) and 35× over prior work.

### II. BACKGROUND

In layer \( l \) of a GNN, each vertex \( i \) in the graph is represented by an \( F^l \)-dimensional row vector, \( h_i^l \), called the vertex feature vector; \( h_0^l \) is the input vertex feature vector. For each vertex \( i \) in a layer, over a set of neighboring vertices \( j \), the GNN aggregates information from vectors \( h_j^{l-1} \) of the previous layer, and processes it to create the output feature vector, \( h_i^l \).

Table I shows the Weighting and Aggregation operations for graph convolution networks (GCNs) [21], GraphSAGE [14], graph attention networks (GATs) [32], and GINConv [37].

### Table I: Summary of operations in layer \( l \) of various GNNs.

| GNN     | \( h_i^l \) = \( \sigma \left( \sum_{j \in \{i \} \cap N(i)} \frac{W_{ij}}{d_{ij}} h_j^{l-1} W^l \right) \) |
|---------|------------------------------------------------------------------|
| GraphSAGE | \( h_i^l = \sigma \left( e_{ij} h_i^{l-1} W^l f_{ij} \right) \) |
| GAT     | \( h_i^l = \sigma \left( \sum_{j \in \{i \} \cap N(i)} \exp(\exp(W_{ij})) \right) \) |
| GINConv | \( h_i^l = \text{MLP}^l \left( (1 + \epsilon) h_i^{l-1} + \sum_{j \in N(i)} h_j^{l-1}, W, b \right) \) |

**Weighting** multiplies the vertex feature vector, \( h_i^{l-1} \) of each vertex by a weight matrix, \( W_i^l \), of dimension \( F^{l-1} \times F^l \). **Aggregation** combines the weighted vertex feature vectors neighboring vertex \( i \). If \( N(i) \) is the immediate one-hop neighborhood of vertex \( i \), then for GCNs, GATs, and GINConv, \( N(i) = \{i\} \cup N(i) \). For GraphSAGE, \( N(i) = \{i\} \cup S_{N(i)} \), where \( S_{N(i)} \) is a random sample of \( N(i) \). At vertex \( i \):

**GCNs:** Each product \( h_i^{l-1} W^l j \) is multiplied by \( \frac{1}{\sqrt{d_i d_j}} \) (\( d_i \) is the vertex degree). The result is summed.

**GraphSAGE:** The products \( h_i^{l-1} W^l j \) are combined over \( j \in N(i) \) using aggregator \( a_o \) (typically, mean or pooling).

**GATs:** For each edge \( \langle i, j \rangle \), an inner product with a learned attention vector \( a \) finds the normalized attention coefficient

\[ \alpha_{ij} = \text{softmax}(\text{LeakyReLU}(\alpha^T \cdot [h_i^{l-1} W^l j \vert h_j^{l-1} W^l j])) \]

followed by \( \sum_{j \in \langle i \rangle} \alpha_{ij} h_i^{l-1} W^l j \), a weighted aggregation.

**GINConv:** The vertex feature vectors of all neighbors of a vertex \( i \) are summed and added to \( \epsilon \) times the vertex feature vector of \( i \), where \( \epsilon \) is a learned parameter, using a multilayer perceptron (MLP) with weights \( W^l \) and \( b^l \):

\[ h_i^l = \text{MLP}^l \left( (1 + \epsilon) h_i^{l-1} + \sum_{j \in N(i)} h_j^{l-1}, W^l, b^l \right) \]
GINConv concatenates the sum of all vertex feature vectors across all layers to obtain a representation for the graph as

$$h_G = \left\{ \sum_{l=1}^{L} h_l^i \right\}$$ (2)

DiffPool [40] can be combined with any of these GNNs to reduce the volume of data. It uses two GNNs, one to extract vertex embeddings for graph classification, and one to extract embeddings for hierarchical pooling. The embedding GNN at layer $l$ is a standard GNN with Weighting and Aggregation,

$$Z^{l-1} = \text{GNN}_{\text{emb}}(A^{l-1}, X^{l-1});$$ (3)

where $A^{l-1}$ is the adjacency matrix of the coarsened graph at level $(l-1)$, and $X^{l-1}$ is the matrix of input cluster features. The pooling GNN generates the assignment matrix:

$$S^{l-1} = \text{softmax} \left( \text{GNN}_{\text{pool}}(A^{l-1}, X^{l-1}) \right)$$ (4)

The number of clusters in layer $l$ is fixed during inference. The coarsened adjacency matrix $A_l = S^{l-1} \cdot A^{l-1} \cdot S^{l-1}$, and the new embedding matrix $X_l = S^{l-1} \cdot Z^{l-1}$.

III. ACCELERATOR ARCHITECTURE

The block diagram of the proposed accelerator is illustrated in Fig. 3 and it consists of the following key components:

1. **HBM DRAM**: The high-bandwidth memory (HBM) DRAM stores information about the graph. The adjacency matrix of the graph represents its connectivity information and is stored in sparse compressed sparse row (CSR) format. Other formats (CISR [11], C$^2$SR [31], CISS [32]) are not viable candidates as they ignore the underlying graph structure: GNNIE uses adjacency matrix connectivity information to schedule computations and is not a matrix multiplication method.

The sparse input vertex feature vectors are encoded using run-length compression (RLC) [28]. We choose RLC because it is lossless and the decoder has low power/area overhead: this is important because it is only used for the input layer and it is lossless and the decoder has low power/area overhead: this reduces the volume of data. It uses two GNNs, one to extract vertex embeddings for graph classification, and one to extract embeddings for hierarchical pooling. The embedding GNN at layer $l$ is a standard GNN with Weighting and Aggregation, and the result after Aggregation. The end result is written to off-chip memory. The weight buffer holds the values of the weight matrix $W^l$ during Weighting, and, for GAT computations, the attention vector during Aggregation.

The memory access scheduler coordinates off-chip memory requests from the input/output/weight buffers.

3. **An array of processing elements (PEs)**: The array consists of an $M \times N$ array of computation PEs (CPEs). Each CPE has two scratch pads (spads) and MACs.

Within the array of CPEs, we merge multiple columns of Special Function Units (SFUs) (e.g., exp, leaky ReLU) [grey blocks], and a row of merge PEs (MPes) [red blocks]. Interleaved placement allows low latency and communication overhead with CPEs. For exponentiation, we use an accurate, low-area lookup-table-based implementation [25].

Merge PEs (MPEs) are used to aggregate partial results of vertex features sent from the CPE array during Weighting and Aggregation. One MPE is dedicated for each CPE column in the array (Fig. 3), collecting partial results from the CPEs in its column. Each MPE has one update spad to hold the partial results sent from the CPEs in its column. The update spad contents are sent to an accumulator bank. A bank of partial sum (psum) spads holds intermediate results from the accumulator bank. When the summation is complete, the psum bank sends results to the output buffer.

4. **The Activation unit** performs an activation operation on the vertex features at the final activation stage of computation.

5. **The controller** coordinates operations, including assigning vertex features to the CPE, workload reordering among the CPEs, sending CPE results to the MPEs, sending MPE data to the output buffer, and writing concatenated MPE data.

For a GCN, the layer-wise computation can be written as:

$$h_i = \sigma(\hat{A} h_i W^l)$$ (5)

Here, $\hat{A} = D^{-1/2}(A + I)D^{-1/2}$ is the normalized adjacency matrix, $I$ is the identity matrix, and $D_{ii} = \sum_j A_{ij}$. This can be computed either as $(\hat{A} \times h_i^{l-1}) \times W^l$ or $\hat{A} \times (h_i^{l-1} \times W^l)$. The latter requires an order of magnitude fewer computations than the former [12], [22], and we use this approach. Moreover, as $\hat{A}$ is highly sparse and shows power-law behavior, we will perform edge-based Aggregation with optimized graph-specific cache replacement policies to limit off-chip accesses.
Each column of $W$. Within each pass, the CPEs are loaded as follows: and the process continues under the weight-stationary scheme. N sets with feature vectors (i.e., processing all vertices in all sets). As pass DRAM to the weight buffer. A is constrained by the size of the input buffer. To process all vertices at a time in the PE array, as shown in Fig. 5, where across vertices: (2) Across the vertex feature vector: We process feature vectors for a set of s vertices at a time in the PE array, as shown in Fig. 5 where s is constrained by the size of the input buffer. To process all vertices in the graph $G(V,E)$, we process $|V|/s$ sets as:

$$h_{i}^{l-1}W^{l} = \left\{ \begin{array}{ll}
\sum_{i=0}^{F^{l-1}} h_{(0:k-1)i}^{l-1}W_{(0:k-1,i)}^{l} & \text{if } i=0 \\
\sum_{i=0}^{F^{l-1}} h_{(k:2k-1)i}^{l-1}W_{(k:2k-1,i)}^{l} & \text{if } i=1 \\
\ldots & \\
\sum_{i=0}^{F^{l-1}} h_{((N-1)k:F^{l-1})i}^{l-1}W_{((N-1)k:F^{l-1},i)}^{l} & \text{if } i=F^{l-1}
\end{array} \right.$$  

(6)

where the term in each sum is processed in a separate CPE. We use a weight-stationary scheme (Fig. 4). Each vertex goes through Weighting set by set, placing $k$-element blocks of the vertex feature vectors for each set into the input buffer. We fetch $N$ columns of the weight matrix, $W^{l}$, from the DRAM to the weight buffer. A pass processes all vertex feature vectors (i.e., processing all vertices in all sets). As shown in Fig. 5, we multiply the vertex feature vectors in all sets with $N$ columns of $W^{l}$ in the pass. At the end of a pass, the next set of $N$ columns of $W^{l}$ is loaded. After all passes are completed, the current set of weights is replaced by a new set, and the process continues under the weight-stationary scheme. Within each pass, the CPEs are loaded as follows:

- Each column of $W^{l}$ is loaded to a CPE column in chunks of $k$ rows, i.e., $W_{(ik:(i+1)k-1,j)}^{l}$ is loaded into CPE (i,j).
- For a given set of $s$ vertices, the $i^{th}$ subvectors, of size $k$, of all $s$ vertex feature vectors are broadcast to the entire CPE row $i$. This is indicated by $h$ in Fig. 4.

To leverage input data sparsity, a zero detection buffer is used to skip CPE computations involving zeros. Completed CPE results are sent to the MPE for accumulation, and the next block of size $k$ is loaded to the CPE.

**Benefit of using vertex feature subvector blocks:** Our use of $k$-element blocks instead of the entire vector allows a CPE to skip zero subvectors during pipelined execution and immediately move on to a block from the next available subvector. The next block will be fetched from the input buffer, and under the weight-stationary scheme, it can start computation with the already-loaded weights in the CPE.

The proposed weight-stationary dataflow maximizes the reuse of the weights cached in the weight buffer, which turn reduces the size requirement of the on-chip weight buffer. Though the feature vectors fetched in the input buffer are get reused, for all datasets evaluated, the computation time for vertices cached in the input buffer is seen to be larger than the memory fetch time under the HBM 2.0 off-chip bandwidth.

**B. MPE Processing and Weight Updates**

The MAC operation within each CPE generates a partial result for an element of the transformed vertex features. This is sent to the MPE in its column for accumulation over the vertex feature subvectors, along with a tag that denotes its vertex. Due to the irregular completion times for the CPEs, the MPE may accumulate partial sums for several vertices at a time. A bank of psum buffers holds the partially accumulated results: when all partial sums are accumulated for a vertex feature vector, the MPE sends the result to the output buffer, along with the vertex ID $i$: this is one element of the result of multiplying the feature vector of vertex $i$ and $W^{l}$. When all $F^{l}$ elements are computed, the result is written back to DRAM.

After a CPE column processes all feature blocks for all vertices, the next pass begins. The weights in that column are replaced with the next column of weights from $W^{l}$. To overlap computations and keep the CPEs busy, we use double-buffering to fetch the next block of weights from the DRAM to the chip while the CPEs perform their computations.

**C. Load Balancing for Weighting**

The Weighting computation skips zeros in the vertex feature vector. Vertex feature vectors in the input layer have different sparsity levels (e.g., in Regions A and B of Fig. 2), and this is also true of the $k$-subvectors. Hence, some $k$-subvectors are processed rapidly (“rabbits”) while others take longer (“turtles”). This causes workload imbalance in the CPE array.

The MPEs that accumulate the results of the CPEs must keep track of psums from a large number of vertices, but they
have only limited psum slots for accumulating information. The rabbit/turtle disparity implies that stalls may have to be introduced to stay within the limits of available psum memory in the MPE. As results are accumulated in the output buffer, a larger number of vertex feature vectors must be stored within the buffer, waiting to be completed and written to the DRAM, to account for the disparity between rabbits and turtles.

**Flexible MAC (FM) Architecture:** We can avoid stalls and speed up computation with more MACs per CPE. Increasing the number of MACs per CPE uniformly throughout the array overcomes the bottleneck of “turtles,” but is overkill for “rabbits.” Our flexible MAC architecture uses a heterogeneous number of MAC units per CPE in different rows of the array. The CPE array is divided into \( g \) row groups, each with an equal number of rows; the number of MAC units per CPE, \( |MAC|_i \), is monotonically nondecreasing from the first row to the last, i.e., \( |MAC|_1 \leq |MAC|_2 \leq \cdots \leq |MAC|_g \).

The input buffer has a scheduler that assigns vertex feature vectors to CPE rows. The scheduler uses information about the total nonzero workload for each \( k \)-element block of the vertex feature vector to assign the workload to CPE rows. The workloads for the \( k \)-element blocks are first binned based on the number of nonzeros, where the number of bins equals the number of CPE groups. Workload binning is carried out as a preprocessing step in linear time. The bin with fewest nonzeros is sent to the first CPE group with fewest MACs, and so on; the bin with the most nonzeros is sent to the last CPE row group with the most MACs.

An example of workload reordering among CPE rows is shown in Fig. 6. The CPE array is divided into three groups, Group 1, 2, and 3, where Group \( i \) is equipped with \( |MAC|_i \) MACs per CPE, where \( |MAC|_1 < |MAC|_2 < |MAC|_3 \). The vertex feature blocks are binned into three bins that will be assigned to each group. Each bin has several vertex feature blocks: the vertex feature blocks in the left-most bin have the most nonzeros (six), and those of the right-most bin have the fewest of nonzeros (four). We see that the least populated bin is assigned to the group with the fewest MACs, the next to the group with the next number of MACs, and so on.

**Load Redistribution (LR):** The FM approach does not completely balance the workload. For greater uniformity, we redistribute loads among nearby CPEs. Based on workload distribution in CPE rows, the controller selects pairs of CPE rows to perform workload redistribution, offloading a portion of workload from heavily loaded to lightly loaded CPE rows.

To perform computation on the offloaded workloads, the weights must be transferred with the data. To minimize communication overhead, we first finish the computation in FM, to the point where the current weights are no longer needed, before applying LR. The spads for weights in these CPE rows are loaded with weights for the offloaded workloads.

**V. Aggregation Computations**

For most GNNs in Section IV, Aggregation is a simple summation over the neighbors of the vertex, but GATs require significantly more computation in determining attention coefficients, which are used for weighted aggregation. The first two subsections focus on GAT-specific computations. We then consider Aggregation operations that affect all GNNs.

**A. Reordering for Linear Computational Complexity**

We present a new method for reordering GAT computations for efficient hardware implementation. We define the weighted vertex attention vector for vertex \( p \) as \( \eta_{wp} = h_p \cdot \text{W}^T \). The first step in finding the attention coefficient \( \alpha_{ij} \) for neighboring vertices \( i \) and \( j \), is to multiply the \( 2F \)-dimensional attention vector, \( a^i \), by a concatenation of two \( F \)-dimensional weighted vertex feature vectors, \( (\eta_{wp}, \eta_{wj}) \). We now show how this operation is carried out in the PE array by the CPEs.

Rewriting \( a^i = [a^i_1 a^i_2] \), where \( a^i_j \) is the subvector that multiplies \( \eta_{wp} \), we can denote this inner product as

\[
e_{ij} = a^i_1 \cdot \eta_{wp} + a^i_2 \cdot \eta_{wj} = e_{i,1} + e_{j,2} \tag{7}
\]

where \( e_{i,1} = a^i_1 \cdot \eta_{wp} \) and \( e_{j,2} = a^i_2 \cdot \eta_{wj} \). This goes through a LeakyReLU and then a softmax over all neighbors of \( i \) to find the normalized attention coefficient,

\[
\alpha_{ij} = \text{softmax} \left( \text{LeakyReLU}(e_{ij}) \right) \tag{8}
\]

A naïve approach would fetch \( \eta_{wp} \) from each neighbor \( j \) of \( i \), compute \( e_{ij} \) using (7), and perform softmax to find \( \alpha_{ij} \). However, since \( e_{j,2} \) is required by every vertex for which \( j \) is a neighbor (not just \( i \)), this would needlessly recompute its value at each neighbor of \( j \). To avoid redundant calculations, we reorder the computation: for each vertex \( i \), we compute

(a) \( e_{i,1} = a^i_1 \cdot \eta_{wp} \), used to compute \( \alpha_{i,j} \) at vertex \( i \).
(b) \( e_{i,2} = a^i_2 \cdot \eta_{wj} \), used by all vertices \( j \) for which \( i \) is a neighbor, to compute \( \alpha_{j,i} \) at vertex \( j \).

Since \( a^i = [a^i_1 a^i_2] \) is identical for each vertex, we calculate \( e_{i,2} \) just once at vertex \( i \), and transmit it to vertices \( j \).

For \( |V| \) vertices and \( |E| \) edges, the naïve computation performs \( O(|E|) \) multiplications and memory accesses to \( \eta_{wp} \) per vertex, for a total cost of \( O(|V||E|) \). Our reordered computation is \( O(|V||E|) \), with \( O(|E|) \) accumulations over all vertices, i.e., latency and power are linear in graph size.

**B. Mapping Attention Vector Multiplication**

As in Weighting, we use a block strategy to distribute computation in the CPE array. The vector \( \eta_{wp} \) is distributed across all \( N \) columns of a row, so that the size of each block allocated to a CPE for vertex \( i \) is \( G = \lceil |F|/N \rceil \). Each CPE column processes \( V_a \) vertices. Here, \( V_a \) depends on the number of columns \( N \) in the CPE array, and also depends on the size of the output buffer \( |OB| \), i.e., the size of the set of vertices that can be cached in the output buffer: \( V_a = |OB|/N \).
This dot product computation is very similar to the weight-
stationary scheme used in the Weighting step, i.e., the attention
vectors remain stationary until a pass through all the vertices.
As the CPEs in a column finish computation for a vertex, the
partial results are sent to the corresponding MPE for
Aggregation. We overlap the computation in a CPE column and
with the Aggregation in the corresponding MPE: as the
MPE aggregates partial results for the current vertex, the
blocks of the next weighted feature vectors are loaded into the
CPE. Thus, all CPEs and MPEs remain busy.

After all \( V_n \) vertices in the row are processed, the spad that
contains \( a_1 \) is loaded with \( a_2 \), and the second inner product
computation for the \( V_n \) vertices is performed, reusing \( \eta_w \).
The computed \( e_{1,1} \) and \( e_{1,2} \) are written back to the output buffer and
are appended to the feature vector of vertex \( i \).

C. Mapping Edge-based Computations

The last step requires edge aggregation from each neighbor of
a vertex. All GNNs, perform edge-based summations followed
by an activation function; for GATs, the weights for this
summation are computed using methods in the above subsections.

Typical graphs are too large for the on-chip buffers. We use a
dynamic scheme (Section VI) to process a subgraph of the
graph at a time, processing edges in parallel in the CPE array.

Load Distribution: The Aggregation computation brings data
into the input buffer. For each vertex in the subgraph corresponding
to the vertices in the buffer, it accumulates edge data by
pairwise assignment to CPE spads. Due to power-law behavior, the vertex degrees in the
subgraph may have a large range. To distribute the load, the
Aggregation summations are divided into unit pairwise
summations and assigned to CPEs. For instance, accumulation
of a sum effectively implements an adder tree in which the
number of CPEs required to process Aggregation for each
vertex depends on its degree in the subgraph.

GATs: The final step in computing the attention coefficient
\( \alpha_{ij} \) involves edge-based computations (Equation (9)): the addition, \( e_{ij} = e_{i,1} + e_{j,2} \)
a LeakyReLU step, \( \text{LeakyReLU}(e_{ij}) \)
a softmax step, \( \exp(e_{ij}) \eta_{w,ij} / \sum_{k \in \{i\} \cup \{N(i)\}} \exp(e_{ik}) \)
Each edge from a neighbor \( j \) to vertex \( i \) contributes an \( e_{ij} \)
to the numerator of the softmax, and one to the
denominator. These computations are parallelized in the CPEs among
incoming edges of a vertex using pull-based aggregation \[23\].

The computation of numerator in the softmax step is shown in Fig. 7.
For a target vertex \( i \) connected to a neighbor \( j \) by edge \((i, j)\), \( \eta_{w,ij} \), \( e_{i,1} \), and \( e_{i,2} \), are loaded into one spad of a
CPE, and the corresponding data for \( j \) into the other spad. For
vertex \( i \), the result \( e_{i,1} + e_{j,2} \) is sent to the SFU to perform
LeakyReLU followed by exponentiation. The output returns
to the CPE and is multiplied with \( \eta_{w,ij} \). A similar operation is performed for vertex \( j \) to compute \( \exp(e_{ij}) \eta_{w,ij} \).

Other GNNs: The Aggregation step for GCN, GraphSAGE, GAT and GINConv involves a sum of weighted vertex feature
vectors over all neighbors \( j \) (or a sample of neighbors for
GraphSAGE) of each vertex \( i \). This computation is similar to
but simpler than that in Fig. 7 just addition is performed.

As before, a subgraph of the larger graph is processed at a
moment. In processing vertex \( i \), the data for all neighbors \( j \)
is processed in an adder tree, placing operands in spad1 and
spad2 of a CPE, and storing the result in spad1. The partial
results for a vertex (partial sum for a general GNN, or the
summed numerator and softmax denominator for a GAT) are
written to the output buffer after each edge computation. For a
GAT, the values of \( \exp(e_{ik}) \) are also added over the
neighborhood to create the denominator for the softmax. Finally, the
accumulation over neighbors is divided by the denominator,
in the SFU to obtain the result. When all components of the
sum for vertex \( i \) are accumulated, the result is sent through the
Activation unit and written to DRAM.

VI. Graph-Specific Caching

Aggregation operations intensively access the graph adjacency
matrix. Computational efficiency requires graph-specific caching techniques to transfer data to/from on-chip input and
output buffers, maximizing data reuse and minimizing off-chip
random memory accesses. A notable feature of our proposed
policy is a guarantee that all random-access patterns are
confined to on-chip buffers and off-chip fetches are sequential.

As stated earlier, the adjacency matrix is stored in the CSR
format. Our input is a graph represented by three arrays: (i) the
coordinate array lists the incoming/outgoing neighbors of each
vertex, (ii) the offset array contains the starting offset of each
vertex in the coordinate array, and (iii) the property array with
the weighted vertex feature, \( \eta_{w,i} \) (see Section V-A), for each
vertex \( i \); for GATs, this is concatenated with \{\( e_{i,1}, e_{i,2} \}\).

Subgraph in the Input Buffer: Edge-mapped computations
involve a graph traversal to aggregate information from neighbors.
At any time, a set of vertices resides in the input buffer: these vertices, and the edges between them, form a subgraph
of the original graph. In each iteration, we process edges in
the subgraph to perform partial Aggregation operations (Section V-C)
for the vertices in the subgraph. Under our proposed caching strategy, ultimately all edges in the graph
will be processed, completing Aggregation for all vertices.

We illustrate the concept through an example in Fig. 8
showing a graph with vertices \( V_1 \) through \( V_{15} \). The highest
degree vertices are first brought into the cache, i.e., the input

![Fig. 7. Data flow corresponding to computation of an edge.](image-url)
The algorithm processes each such set of vertices in the input buffer in an iteration. This continues until all vertices are processed. At the end of iteration 1, i.e., after finishing computation of the subgraph corresponding to the first \( n \) vertices, if \( \alpha_i < \gamma \) for any vertex, where \( \gamma \) is a predefined threshold, it is replaced from the cache. We replace \( r \) vertices in each iteration using dictionary order if fewer (or more) than \( r \) candidates are available. These vertices are replaced in the input buffer by vertices \((n + 1)\) to \((n + 1 + r)\) from DRAM: these have the next highest vertex degrees. For each such vertex \( i \), we write the \( \alpha_i \) value into DRAM. When all vertices are processed once, we have completed a Round.

Similarly, the partial sums for the vertex feature vector in the output buffer are updated as more edges in the subgraphs are processed. Any \( h^t_i \) for which all accumulations are complete is written back to DRAM. Due to limited output buffer capacity, and only a subset of partial vertex feature vector sums can be retained in the buffer, and the rest must be written to off-chip DRAM. To reduce the cost of off-chip access, we use a degree-based criterion for prioritizing writes to the output buffer vs. DRAM. As partial Aggregation results for softmax are written to DRAM, the numerator and denominator components for a vertex are stored nearby, for locality during future fetches.

**How our policy avoids random-access DRAM fetches:** Our policy makes random accesses only to the input buffer; all DRAM fetches are sequential. In the first Round, data is fetched from consecutive DRAM locations. In the CPE array, aggregation of each vertex fetches the vertex feature data of its neighbors in the current subgraph in the cache. Each vertex feature vector may be thus fetched by the CPE array multiple times according to the graph neighborhood structure, but all such random accesses are limited to the cache, which has much better random-access bandwidth than the off-chip memory.

Vertices evicted from the cache, with \( \alpha_i < \gamma \), may be fetched again in a subsequent Round. Even in these Rounds, data blocks are brought into cache in serial order from DRAM: there are no random accesses from DRAM. During DRAM fetches, a cache block is skipped if all of its vertices are fully processed. The total unprocessed edges in a cache block is tracked through inexpensive hardware, similar to tracking \( \alpha_i \).

The effectiveness of the approach is illustrated in Fig. 10 which shows the histogram of \( \alpha_i \) distributions in the input buffer after each Round. The initial distribution corresponds to the power-law degree distribution, and in each successive Round, the histogram grows flatter – with both the peak frequency and maximum \( \alpha \) becoming lower, thus mitigating the problems of power-law distribution. In contrast, HyGCN ignores the power-law problem, and AWB-GCN overcomes it using high inter-PE communication. Moreover, our approach is shown to be effective even for much more intensive GAT computations (prior accelerators do not address GATs).

Fig. 11 shows the impact of \( \gamma \) on DRAM accesses for
three datasets. As $\gamma$ increases, more vertices are evicted and may have to be brought back to the cache, resulting in more DRAM accesses. However, if $\gamma$ is too low, vertices may not be evicted from the cache, resulting in deadlock as new vertices cannot be brought in. In our experiments, we use a static value $\gamma = 5$, but in practice, $\gamma$ may have to be changed dynamically when deadlock arises. Deadlock detection is inexpensive and is based on the number of total unprocessed edges in the partition, which is monitored by a counter, and this dynamic scheme will be expensive in hardware.

VII. RELATED WORK

There has been much work on CNN accelerators [2], [7], [15], [17], [18], [27], [30], but these are not efficient for processing GNNs. Research on graph analytics accelerations includes Graphicionado [13], using modules tuned for irregular memory access, memory bandwidth bottlenecks, and optimized on-chip memory utilization; FPGP [8], a multi-FPGA-based accelerator that partitions the graph based on intervals and shards; GraFBoost [19], employing a sort-reduce accelerator to convert random accesses to flash memory to sequential ones; GraphPIM [24], using Hybrid Memory Cube (HMC) for in-memory processing. However, graph accelerators target lightweight operations per vertex, do not focus on data reuse, and would be challenged by computation-intensive GNNs.

Software frameworks for GNNs include Deep Graph Library [34], AliGraph [39], and TensorFlow [1]. Some hardware accelerators have been proposed, but we know of no prior work that can handle networks that require softmax nonlinearities on graphs such as GATs. Although some GAT computations are addressed in [41], the crucial attention normalization step is left out. To our knowledge, no methods handle extreme input feature vector sparsity using graph-specific methods.

The HyGCN accelerator [38] uses an Aggregation engine for graph processing and a Combination engine for neural operations. This requires separate on-chip buffers for each engine; with workload imbalance at different stages of computation, these are not fully utilized. HyGCN must arbitrate off-chip memory access requests coming from on-chip buffers of two different engines, which involves complicated memory access control. Using a single hardware platform optimized to handle both the irregular graph computation and compute-intensive, albeit regular, DNN computation, GNNIE achieves performance gains over HyGCN. Moreover, HyGCN uses sharding with window sliding/shrinking to reduce random memory access during Aggregation: this has (1) limited efficiency for highly sparse adjacency matrices as the number of overlapping neighbors of vertices is a small fraction of the total number of vertices in a shard, undermining its efficacy; moreover, no specific effort is made to address power-law degree distributions. (2) limited parallelism as the sliding window of the current shard depends on the shrinking of the previous shard; HyGCN does not fully leverage data reuse opportunities of high-degree vertices during Aggregation, performing $\langle \Delta h_{i-1}W \rangle$, instead of cheaper $\hat{A}(h_{i-1}W')$, which is much cheaper [12], [22]. Moreover, input feature vector sparsity is not addressed and can result in stalls, resulting in computational inefficiency. These factors explain GNNIE’s high speedups (35× on average) over HyGCN.

AWB-GCN [12], which is limited only to GCNs and not general GNNs, views the problem as a set of matrix operations. It does not specifically try to reduce random memory accesses to the highly sparse graph adjacency matrix. Its dynamic scheduling scheme in AWB-GCN for workload redistribution among PEs may incur high inter-PE communication, degrading energy efficiency. EnGN [22] uses a ring-edge-reduce (RER) dataflow for Aggregation, where each PE broadcasts its data to other PEs in the same column. To reduce communication, EnGN reorders the edges, but this is an energy-intensive step, undermined by high sparsity in the adjacency matrix, that occurs frequently as the limited number of cached edges are replaced. The scheme has large preprocessing costs. Although EnNGN attempts dimension-aware stage reordering to perform Aggregation or Weighting first, their results confirm that in practice, the Weighting-first scheme used in GNNIE is better.

Prior accelerators have not fully explored load balancing. Methods that offload tasks to idler PEs (ring-edge-reduce [22], multistage networks [12]) involve high communication and control overheads. GNNIE bypasses such approaches and uses the flexible MAC architecture for load balancing, using heterogeneous PEs, and assigning computation according to needs. The idea is simple, effective, and easily implemented. It results in low inter-PE communication, low control overhead, and high speedup gain for the hardware overhead (Fig. 18). Preprocessing is cheap and involves linear-time binning of vertex features blocks into groups.

Frequency-based caching techniques for graph data have been proposed in [41] using a programming interface. However, GNNIE is a purely software-based framework, agnostic to the underlying hardware, for traditional graph analytics and uses a static approach. GNNIE uses a hardware-centric dynamic frequency-based caching scheme that tracks the $\alpha$ value for each vertex with minimal hardware overhead, and ensures serial access to DRAM. Other schemes are also static and more
computational than GNNIE: they use hashing functions \[6\] or perform more computation \[3, 35\] in finding static communities/partitions that do not specifically address cache size. On the other hand, GNNIE's computationally cheap dynamic scheme automatically adapts to the cache size using subgraphs built from vertices in the cache. GRASP \[10\], another cache management scheme for graph analytics, employs a most-recently-used (MRU) approach. However, this scheme is based on past history, while GNNIE's use of the unprocessed vertex count measures future potential for a vertex.

VIII. EVALUATION

A. Experimental Setup

**Accelerator Simulator:** We develop a cycle-accurate simulator to measure the execution time in terms of the number of cycles required. The simulator models each module of GNNIE and integrated with Ramulator \[20\] to model the memory access to the off-chip HBM with 256 GB/s bandwidth.

Each module was implemented and synthesized in Verilog and the synthesized design was verified through RTL simulations. Synopsys Design Compiler was used to synthesize the accelerator at 32nm technology node with standard VT cell library. The chip area, critical path delay, and dynamic/static power, extracted from Design Compiler, are used for evaluations. Synopsys Design Compiler was used to synthesize the accelerator, i.e., GAT, GCN, GraphSAGE, GINConv, and DiffPool, and the synthesized design was verified through RTL simulations. The speedup calculations account for preprocessing due to degree-based vertex reordering (Aggregation) and workload assignment in our FM architecture tackles the feature vector sparsity challenge. (ii) Our degree-aware cache management policy avoids random memory accesses to DRAM; datasets (PB, PPI, RD). The area and power numbers reported later correspond to the larger input buffer size. The output buffer is larger since it must cache many partial results before they are aggregated, particularly for high-degree vertices. For a 1-byte weight, for the dataset with the largest feature vector (~4K for CS), to keep 16 CPE columns occupied, the buffer size is 4K × 16 × 2 (for double-buffering) = 128KB.

The chip area, critical path delay, and dynamic/static power, extracted from Design Compiler, are used for evaluations. As shown in Fig. 12a), the average speedup of GNNIE over the PyG-CPU across the datasets used for GCN, GAT, GraphSAGE, GINConv, and DiffPool are 18556 × 12120 × 12120 × 12120 × 12120, respectively. According to Fig. 12b) the average speedup of GNNIE over the PyG-GPU across the datasets used for GCN, GAT, GraphSAGE, GINConv, and DiffPool are 18556 × 12120 × 12120 × 12120 × 12120, respectively. According to Fig. 12b) the average speedup of GNNIE over the PyG-GPU across the datasets used for GCN, GAT, GraphSAGE, GINConv, and DiffPool are 11 × 416 × 2427 × 412 × 231, respectively.

The speedup calculations account for preprocessing due to degree-based vertex reordering (Aggregation) and workload reordering (Weighting). For both, we use a binning approach that has linear time complexity. For GraphSAGE, the time taken for sampling the vertex neighborhood is included. Performance comparisons with CPU and GPU: To make a fair performance comparison with the general-purpose CPU and GPU, we implement the GNN models with the PyTorch Geometric (PyG) software framework. The PyG-based implementations for CPU and GPU used in our experiment are denoted as PyG-CPU and PyG-GPU, respectively. Neighbor sampling for GraphSAGE is based on cycling through a pregenerated set of random numbers: the cost of random number generation is included in the evaluation. As shown in Fig. 12a), the average speedup of GNNIE over the PyG-CPU across the datasets used for GCN, GAT, GraphSAGE, GINConv, and DiffPool are 18556 × 12120 × 12120 × 12120 × 12120, respectively. According to Fig. 12b) the average speedup of GNNIE over the PyG-GPU across the datasets used for GCN, GAT, GraphSAGE, GINConv, and DiffPool are 11 × 416 × 2427 × 412 × 231, respectively.

### Table II: Dataset Information \[29\]

| Dataset       | Vertices | Edges  | Feature Length | Labels | Sparsity |
|---------------|----------|--------|----------------|--------|----------|
| Cora (CR)     | 2708     | 10556  | 1435           | 7      | 98.73%   |
| Citeseer (CS) | 3327     | 9104   | 3703           | 6      | 99.15%   |
| Pubmed (PB)   | 19717    | 88648  | 500            | 3      | 90%      |
| Protein-protein interaction (PPI) | 56944  | 1.63M  | 50              | 121    | 98.1%    |
| Reddit (RD)   | 232965   | 114.6M | 602            | 41     | 48.4%    |

### Table III: Convolution layer configurations (len[h] = length of \(h\))

| GNN Model     | Weighting | Aggregation | Sample size |
|---------------|-----------|-------------|-------------|
| GAT           | len[h] : 128 | Sum        | --          |
| GCN           | len[h] : 128 | Sum        | --          |
| GraphSAGE     | len[h] : 128 | Max        | 25          |
| GINConv       | len[h] : 128 / 128 | Sum | --          |
| DiffPool (GCNconv) | len[h] : 128 | Sum | --          |
| DiffPool (GCNembedding) | len[h] : 128 | Sum | --          |

**Benchmark GNN Datasets and Models:** For evaluation of the performance of GNNIE, we use the benchmark graph datasets listed in Table II. We used five GNN models for evaluations, i.e., GAT, GCN, GraphSAGE, GINConv, and DiffPool. The convolution layer configurations are shown in Table III. All preprocessing costs are included in the evaluation.

**Configurations for Baseline/Cross-Platform Comparison:** We first compare GNNIE against two baseline architectures, i.e., a general-purpose CPU and a GPU. The CPU platform is equipped with Intel Xeon Gold 6132@2.60GHz and 768 GB DDR4. The GPU platform is equipped with V100 Tesla V100S-PCI @1.25GHz and 32 GB HBM2.

For GNNIE, the sizes of output and weight buffers are 1MB and 128KB, respectively. The input buffer size is 256KB for the smaller datasets (CR, CS) and 512KB for the larger datasets (PB, PPI, RD). The area and power numbers reported later correspond to the larger input buffer size. The output buffer is larger since it must cache many partial results before they are aggregated, particularly for high-degree vertices. For a 1-byte weight, for the dataset with the largest feature vector (~4K for CS), to keep 16 CPE columns occupied, the buffer size is 4K × 16 × 2 (for double-buffering) = 128KB.

The speedup comes from several GNNIE optimizations: (i) The segmentation of vertex feature vectors and their assignment in our FM architecture tackles the feature vector sparsity challenge. (ii) Our degree-aware cache replacement policy avoids random memory accesses to DRAM; datasets with lower speedups (e.g., PPI) have less strong power-law
degree distributions and are unable to fully benefit from our methods. (iii) During Weighting, distributing the computation across multiple batches enables weight reuse, increasing efficiency. Note that PyG-CPU and PyG-GPU do not allow our dynamic caching scheme to be implemented within their purely software based frameworks.

C. Cross-platform Comparisons

We conduct cross-platform performance comparisons with HyGCN and AWB-GCN. Neither computes exponentiation for softmax, required by GATs, and AWB-GCN only implements GCN. Thus, for GCN we perform a comparison with HyGCN and AWB-GCN. For GraphSAGE and GINConv we also show a comparison with HyGCN. Unlike the original implementations, HyGCN uses 128 channels for hidden layers of all the GNN models, and therefore we have also configured the hidden layers similarly (Table III). To compare with HyGCN, AWB-GCN runs the customized GCN model with 128 channels for hidden layers on a E5-2680v3 CPU with PyG and reports relative speedup and inference latency. We leverage inference latency data from AWB-GCN for our comparison.

To compute speedup over HyGCN for GraphSAGE, GINConv, and DiffPool we run the GNN models on Intel Xeon Gold 6132@2.60GHz CPU, which has similar performance as the E5-2680v3@2.50GHz CPU, and determine the relative speedup of GNNIE. We then take a ratio of the computed relative speedup with the relative speedup of HyGCN compared to E5-2680v3 CPU. Fig. 13 shows that for GCN, GNNIE achieves average speedup of 25× and 2.1× over HyGCN and AWB-GCN, respectively. Compared to HyGCN, GNNIE achieves average speedup of 72× and 7× for GraphSAGE and GINConv, respectively. A comparison for DiffPool is not possible: HyGCN does not report results on the widely used datasets that we evaluate. As before, these speedup comparisons include GNNIE preprocessing costs.

D. Throughput and Energy Comparisons

Table IV shows the throughput for various datasets for our configuration of GNNIE. The table shows that the throughput degrades only moderately as the graph size is increased.

![Fig. 13. Performance comparison with HyGCN and AWB-GCN.](image)

Even though the on-chip buffer size of HyGCN (24 MB + 128 KB) is much larger than GNNIE (1.7 MB), GNNIE shows an average speedup of 35×. The improvements are attributable to differences between GNNIE and HyGCN described in Sections I and VII. Although AWB-GCN uses 4096 MACs against 1216 for GNNIE, GNNIE is 2.1× faster.

D. Throughput and Energy Comparisons

Table IV shows the throughput for various datasets for our configuration of GNNIE. The table shows that the throughput degrades only moderately as the graph size is increased.

The power dissipation of GNNIE is 3.9W in 32nm, lower than HyGCN (6.7W in 12nm), similar to recent CNN edge inference engines (Edge TPU, Hailo-8, InferX1). Fig. 14 shows the energy breakdown for GNNIE for GAT and GCN across three datasets, including DRAM energy required to supply the output, input, and weight buffers. The output buffer has the most of transactions with DRAM due to psum storage. On-chip weight buffer energy is negligible and not shown.

Fig. 15 compares GNNIE’s energy efficiency with prior works. The efficiency ranges from ranges from $2.3 \times 10^4$ – 5.2 $\times 10^5$ inferences/kJ for HyGCN and 1.5 $\times 10^4$ – 4.4 $\times 10^5$ inferences/kJ for AWB-GCN. GNNIE clearly outperforms the others, going from 7.4 $\times 10^3$ – 6.7 $\times 10^6$ inferences/kJ.

E. Optimization Analysis

We analyze key optimization techniques applied in GNNIE. To evaluate these techniques we select a baseline design (Design A) which uses four MACs per CPE uniformly. Parameters for the flexible MAC architecture and on-chip buffer sizes for all designs are as described at the end of Section VIII-A. The dimension of the PE array in all cases is 16 × 16.

Optimizing Weighting Time: We first analyze the performance improvement of applying flexible MACs (FM) on the baseline design during Weighting. For the Cora, Citeseer, and Pubmed datasets, the workload distribution among the CPE rows for the baseline (without load-balancing) and FM designs are shown in Figs. 16(a), (b), and (c), respectively. Due to vertex feature sparsity, the CPE rows in the baseline design suffer from workload imbalance. The FM design balances the workload distribution among the CPE rows results in 6% (Cora), 14% (Citeseer), and 31% (Pubmed) reduction in the number of cycles required to compute 16 elements of the output vertex features during Weighting. The imbalance between the maximum and minimum is also reduced by FM.

For all datasets, the last four CPE rows require more cycles than others (heavily loaded CPE rows) and the first four CPE
rows finish computation earlier (lightly loaded rows) in FM. We perform load redistribution (LR) between “LR pairs” of heavily loaded and lightly loaded CPE rows, offloading a portion of the workload from the heavily loaded CPE row to the lightly loaded one. The figure shows that applying LR on FM further smooths the workload distribution, reducing the imbalance between the maximum and minimum significantly, and also further reduces the number of cycles.

**Speedup Gain vs. Hardware Overhead Ratio:** We introduce a metric, the speedup gain vs. added hardware ratio:

$$\beta = \frac{\text{Baseline Design Cycles} - \text{Design}[i] \text{ Cycles}}{\text{Design}[i] \text{ MACs} - \text{Baseline Design MACs}}$$  \hspace{1cm} (9)

where $i$ refers to a specific design that is compared with the baseline. We measure $\beta$ with respect to the baseline with 1024 MACs (4 MACs/CPE). The gain in speedup is measured in terms of reduction of the number of cycles required for Weighting as MACs are increased in CPEs of the baseline design uniformly. The additional hardware overhead is measured in terms of the number MACs added to the baseline design. We compute $\beta$ for four designs with respect to the reference designs. These design choices are as follows:

(i) 5 MACs per CPE (i.e., Design B, 1280 MACs in all),
(ii) 6 MACs per CPE (i.e., Design C, 1536 MACs in all),
(iii) 7 MACs per CPE (i.e., Design D, 1792 MACs in all),
(iv) flexible MAC architecture for GNNIE, described at the end of Section VIII-A (i.e., Design E, 1216 MACs in all).

Fig. [17] plots $\beta$ on the three datasets used in our experiment for the four design choices. As MAC units are added uniformly to the baseline design $\beta$ drops and is lowest for Design D across all datasets, $\beta$ drops for Designs B, C, and D as the high sparsity and sparsity variation among vertex features yield low speedup gains as more MACs are added. By employing MACs among CPE rows as needed, the FM approach tackles input vertex feature sparsity, achieving high $\beta$ across all datasets.

**Optimizing Aggregation Time:** Our baseline design has 4 MACs/row (no FM), no load balancing (i.e., no degree-dependent load distribution in Aggregation), and no graph-specific caching (i.e., vertices are processed in order of ID).

We first evaluate our degree-aware graph reordering and our proposed cache replacement policy (CP). We measure the execution time of the baseline during Aggregation with and without CP. Fig. [18](left) shows that CP reduces Aggregation time by 11% (Cora), 35% (Citeseer), and 80% (Pubmed). This is due to reduced random off-chip memory accesses as more edges in a subgraph are processed under degree-aware caching.

Next, we apply CP over FM to measure their combined effect. From Fig. [18](left), the added MACs in CP + FM yield gains of 17% (Cora), 39% (Citeseer), and 82% (Pubmed).

We add our approach for load-balancing (LB) during Aggregation, using the load distribution approach in Section V-C. The combined effect (CP+FM+LB) is shown in Fig. [18](left) to reduce Aggregation time cumulatively by 47% (Cora), 69% (Citeseer), and 87% (Pubmed).

**Optimizing Inference Time:** We evaluate our techniques on GCN and GAT inference time. We first analyze the effect of CP on inference time. Next, we incrementally add FM and LR optimization to CP and measure their combined effect on inference time. Finally, we add all load-balancing (LB) methods: the LR technique for Weighting as well as load distribution during Aggregation. Figs. [18](middle) and (right) shows the reduction in the GCN and GAT inference time, respectively for CP, CP+FM, and CP+FM+LB. The reduction in inference time is higher for Pubmed (19717 vertices) than Cora (2708 vertices), indicating the scalability of GNNIE.

**IX. CONCLUSION**

We have proposed GNNIE, a versatile GNN acceleration platform for to a wide degree of GNNs, including GATs. GNNIE efficiently works with unstructured data, input vertex feature vector sparsity, and adjacency matrix sparsity, and “power-law” vertex degree distribution. It mitigates load balancing issues, computational bottlenecks, and irregular/random data accesses using multiple methods: splitting the computation into blocks to leverage sparsity; optimized caching strategies; employing a flexible MAC architecture in the CPE array. Substantial improvements over prior work are shown.
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