Abstract: Multilevel converters are well suited for high-power and high-quality power conversion. This paper presents a new seven-level V-clamp multilevel converter (VMC) with reduced clamping devices. All phases of the VMC share common DC-link capacitors and realize bidirectional power conversion without flying capacitors. Each branch of the VMC sustains only a single-level voltage of the DC-link capacitors during its commutation process. Hence, the series switches can be controlled as simple as one switch and the dynamic voltage unbalancing issue is avoided. In this paper, the operation principle and the modulation method of the VMC are analyzed in detail. In addition, compensation control for non-ideal factors is designed to improve the output performance. The output fundamental distortion is compensated and the harmonics are reduced. Finally, a laboratory prototype of the seven-level VMC is set up to verify the feasibility of the presented topology and analysis.

Keywords: power conversion; multilevel converter; V-clamp; dead-time effects; compensation control
voltage jumping of the output voltage may occur during the commutation process. It further results in permanent damage to the series switches and over-pressure on the insulation of the filter/motor [17].

In this paper, a new seven-level converter in which the clamping branches resemble a “V” shape, named as a V-clamp multilevel converter (VMC), is introduced [18]. With reduced clamping devices and no FCs, the VMC has a smaller footprint and simple control. Meanwhile, the issues of dynamic voltage unbalancing in series switches and multilevel voltage jumping of the output voltage are avoided with appropriate switching states’ design.

This paper is organized as follows. In Section 2, the configuration and operation principle of the seven-level VMC are introduced. Its commutation process is described in Section 3. Then the modulation method is discussed in Section 4, and the sinusoidal pulse-width modulation (SPWM) is applied. In Section 5, the effects of non-ideal factors including dead-time, switching delay, and voltage drop of devices are analyzed in detail. In addition, a compensation control for the seven-level VMC is designed to improve its output performance. In Section 6, experimental results are presented to validate the presented theory and analysis. Finally, conclusions are summarized in Section 7.

2. Topology and Operation Principle

2.1. Topology Configuration

Figure 1 illustrates the configuration of the three-phase seven-level VMC. All phases share six common DC-link capacitors in series (C1, C2, C3, C4, C5, C6), whose rated voltage is the single-level voltage \( E = V_{dc}/6 \). Considering “O” as the reference zero-point, the DC-link is evenly divided into seven levels, i.e., \(+3E, +2E, +E, 0, -E, -2E \) and \(-3E\).

![Figure 1. The configuration of the three-phase seven-level V-clamp multilevel converter (VMC).](image)

In each phase leg, there are one power arm and six clamping branches, composed of 18 power switching devices (such as IGBT or MOSFET) and six diodes. All power components have the same rated voltage of \( E \). The power arm is composed of \( S_1, S_2, S_3, S_4, S_5, S_6, S_7, \) and \( S_8 \). Meanwhile, \( S_9, S_{10a} \), and \( D_1 \) form three forward clamping branches, which diode currents flow to the power arm. \( D_2, S_{11}, \) and \( S_{12} \) form three backward clamping branches, which diode currents flow to the DC-link. Corresponding nodes of the DC-link and the power arm are linked by these six clamping branches respectively, then the AC terminal potential can be clamped to any of the seven levels.
In the presented topology, series switches are applied to achieve higher withstand voltage. Then, $S_4$ represents three series switches ($S_{4a}$, $S_{4b}$, and $S_{4c}$) and so does $S_5$. Likewise, $S_{10}$ and $S_{11}$ represent two series switches, $D_1$ and $D_2$ represent three series diodes, as seen in Figure 1.

2.2. Switching States Analysis

To ensure the availability of the seven-level VMC, the switching states analysis hereafter is given under the following operation principles:

1. Series switches operate simultaneously. Then, the states of $S_{4a}$, $S_{4b}$, and $S_{4c}$ are represented by $S_4$. So does $S_5$, $S_{10}$, and $S_{11}$.
2. In order to prevent the short-circuit of capacitors, switches $S_1$ and $S_9$, $S_2$ and $S_{10}$, $S_3$ and $S_5$, $S_4$ and $S_6$, $S_7$ and $S_{11}$, and $S_8$ and $S_{12}$ operate in a complementary way, respectively.
3. To reduce the switching times, only one complementary switching pair should change in each commutation process.

Therefore, the switching states of the seven-level VMC are designed as Table 1. Where “1” represents the switching state is on, and “0” represents the switching state is off. The corresponding current paths of each state are illustrated in Figure 2, where the red line represents a positive phase current ($i_o > 0$) and the blue line represents a negative phase current ($i_o < 0$).

![Table 1. Switching states of the seven-level VMC.](image)

2.3. Topology Comparison

Table 2 presents the number of power components required in the three-phase seven-level VMC and other conventional multilevel converters, including the NPCC, FCC, CHBC and MMC. The rated voltages of capacitors, diodes, and power switches are all set as $E$ here. It can be seen that, only one power source and six capacitors are required in the proposed topology and the NPCC. Moreover, the number of total required power components in the VMC is reduced from 132 to 78 in comparison with the NPCC.

![Table 2. Topology comparison between five different topologies.](image)
3. Commutation Process

One concern in the seven-level VMC is that the inconsistent switching actions of the series switches ($S_4, S_5, S_{10}, \text{and } S_{11}$) may result in dynamic voltage unbalancing. But, since the output voltage of the converter only changes one level in each commutation process, the dynamic over-voltage would not appear in the presented topology.

For better understanding, the commutation process from state of $+2E$ (seen as Figure 2b) to state of $+E$ (seen as Figure 2c) is discussed in the following text. During this commutation process, $S_2$ is
turned off firstly, then the series switches of \( S_{10a} \) and \( S_{10b} \) are turned on, the current paths are shown in Figure 3.

![Current paths during the commutation process from state of +2E to state of +E.](image)

**Figure 3.** Current paths during the commutation process from state of +2E to state of +E.

At a condition of \( i_o < 0 \) (blue line), \( i_o \) freewheels through the anti-paralleled diode of \( S_2 \). The output voltage is +2E, and the total blocking voltage of \( S_{10} \) is E. Thus, when switching actions of \( S_{10a} \) and \( S_{10b} \) are inconsistent, the last turned-on switch will withstand whole blocking voltage stress, which is E.

At a condition of \( i_o > 0 \) (red line), \( i_o \) freewheels through the diodes of \( S_{10a} \) and \( S_{10b} \). The output voltage is +E, and the total blocking voltage of \( S_{10} \) is 0. So the voltage stress of both \( S_{10a} \) and \( S_{10b} \) keeps to 0 during this commutation process.

Other commutation processes can be deduced similarly. To summarize, series switches only sustain E during their commutation process. Thus, the unbalancing voltage of the series switches caused by inconsistent switching actions will not exceed their rated voltage stress.

It is also noted that the multilevel voltage jumping of the output voltage would not appear in the VMC. During the commutation process between any two adjacent levels, the output voltage depends on the current direction of \( i_o \). When \( i_o > 0 \), the output voltage is connected to the lower level; and when \( i_o < 0 \), the output voltage is connected to the higher level. Thus, the output voltage keeps unchanged or only changes a single level in each commutation process.

### 4. Modulation Method

In this paper, phase disposition SPWM (PD-SPWM) is adopted in the VMC due to its low complexity and superior performance [19]. Figure 4 illustrates the PD-SPWM waveforms arrangement and the corresponding switching signals. Six triangular carriers \( (v_{tri1}, v_{tri2}, v_{tri3}, v_{tri4}, v_{tri5}, \text{ and } v_{tri6}) \) are compared with a reference wave \( (v_{ref}) \) to get control signals for switches. The peak-to-peak value of each carrier is 1/3, the peak value of output voltage is \( V_o \), then the modulation index \( m \) can be expressed as:

\[
m = \frac{2V_o}{V_{dc}}
\]

The relationship between comparison results and switching signals are as follows:

1. When \( v_{ref} > v_{tri1} \), \( S_1 \) is turned on and \( S_9 \) is turned off.
2. When \( v_{ref} > v_{tri2} \), \( S_2 \) is turned on and \( S_{10} \) is turned off.
3. When \( v_{ref} > v_{tri3} \), \( S_3 \) is turned on and \( S_{11} \) is turned off.
4. When \( v_{ref} > v_{tri4} \), \( S_4 \) is turned on and \( S_6 \) is turned off.
5. When \( v_{ref} > v_{tri5} \), \( S_5 \) is turned on and \( S_7 \) is turned off.
6. When \( v_{ref} > v_{tri6} \), \( S_{12} \) is turned on and \( S_8 \) is turned off.
According to Figure 2, the expression of conduction voltage drop (2) can be considered that the corresponding operation cell is shifting its higher level to the analysis in Section 3, each phase can be decomposed to six half-bridge converters as the basic operation cells, as shown in Figure 5a. When the output voltage of converter changes between any two adjacent levels, it can be considered that the corresponding operation cell is shifting its higher level and lower level output. Where, \( S_p \) is the equivalent upper/lower switch. The output phase voltage is \( v_o \). \( V_\text{P} \) and \( V_\text{N} \) represent the higher level and lower level in the operation cell respectively, and

\[
V_\text{P} - V_\text{N} = E
\]  

Figure 5b illustrates the actual \( v_o \) of the converter considering non-ideal factors. Where, \( G_{p,\text{ref}} \) and \( G_{N,\text{ref}} \) are the reference signals of \( S_p \) and \( S_N \) respectively, and \( G_{p,\text{actual}} \) and \( G_{N,\text{actual}} \) are the actual signals with dead-time. \( T \) is the switching period, and \( t_r \) represents the duration of the positive reference signal. \( t_d \) is dead-time, \( t_{on} \) and \( t_{off} \) are the switching turn-on and turn-off time, respectively. According to Figure 2, the expression of conduction voltage drop \( (V_{\text{on}}) \) is shown in Table 3, where \( V_{\text{sat}} \) is the collector-emitter saturation voltage of switches, and \( V_D \) is the diode forward voltage.

5. Compensation Control Strategy

During each commutation process of the VMC, the dead-time is generally introduced to prevent the short-circuit of capacitors. Whereas, the dead-time, along with the switching delay and voltage drop of devices, will cause inevitable output distortion and finally deteriorate the system performance [20,21]. To solve this problem, a compensation control for the seven-level VMC is proposed in this section.

5.1. Non-Ideal Factors Analysis

The effects of the above-mentioned non-ideal factors in the VMC are discussed firstly. Referring to the analysis in Section 3, each phase can be decomposed to six half-bridge converters as the basic operation cells, as shown in Figure 5a. When the output voltage of converter changes between any two adjacent levels, it can be considered that the corresponding operation cell is shifting its higher level and lower level output. Where, \( S_p/S_N \) is the equivalent upper/lower switch. The output phase voltage is \( v_o \). \( V_\text{P} \) and \( V_\text{N} \) represent the higher level and lower level in the operation cell respectively, and

\[
V_\text{P} - V_\text{N} = E
\]
4. When $v_{\text{ref}} > v_{\text{tri}4}$, S4 is turned on and S6 is turned off.
5. When $v_{\text{ref}} < v_{\text{tri}1}$, S1 is turned on and S2 is turned off.

Table 3. Conduction voltage drop of the seven-level VMC.

| States   | $V_{\text{on}} (i_o > 0)$ | $V_{\text{on}} (i_o < 0)$ |
|----------|--------------------------|--------------------------|
| $+3E$    | $6V_{\text{sat}}$        | $6V_D$                   |
| $+2E$    | $5V_{\text{sat}} + V_D$  | $V_{\text{sat}} + 5V_D$ |
| $+E$     | $4V_{\text{sat}} + 2V_D$ | $2V_{\text{sat}} + 4V_D$ |
| $0$      | $3V_{\text{sat}} + 3V_D$ | $3V_{\text{sat}} + 3V_D$ |
| $-E$     | $2V_{\text{sat}} + 4V_D$ | $4V_{\text{sat}} + 2V_D$ |
| $-2E$    | $V_{\text{sat}} + 5V_D$  | $5V_{\text{sat}} + V_D$  |
| $-3E$    | $6V_D$                   | $6V_{\text{sat}}$        |

For simplifying the calculation, $V_{\text{sat}}$ and $V_D$ are considered approximately equal here. Then the $V_{\text{on}}$ of each conduction path is the same and can be expressed as (3).

$$V_{\text{on}} = V_{\text{on}0} + r|i_o|$$

(3)

where $V_{\text{on}0}$ represents the equivalent on-state threshold voltage of six switches, and $r$ represents the equivalent on-resistance [5].

The direction of $i_o$ is defined as:

$$\text{dir}(i_o) = \begin{cases} 1, & i_o > 0 \\ -1, & i_o < 0 \end{cases}$$

(4)

From Figure 5b, the equivalent dead-time ($t_{d_{\text{eq}}}$) in one switching period can be expressed as:

$$t_{d_{\text{eq}}} = t_d + t_{\text{on}} - t_{\text{off}}$$

(5)

Based on the pulse area equal principle, the reference phase voltage ($v_{o_{\text{ref}}}$) and actual $v_o$ are shown as (6) and (7), respectively.

$$v_{o_{\text{ref}}} = \frac{t_r}{T} V_P + (1 - \frac{t_r}{T}) V_N$$

(6)

$$v_o = \frac{t_r}{T} V_P + (1 - \frac{t_r}{T}) V_N - \text{dir}(i_o)[V_{\text{on}} + \frac{t_{d_{\text{eq}}}}{T} E]$$

(7)

Then, the distortion of the output voltage ($\Delta v_o$) is obtained:

$$\Delta v_o = -\text{dir}(i_o)[V_{\text{on}} + \frac{t_{d_{\text{eq}}}}{T} E]$$

(8)
To analyze the effects of non-ideal factors, define the instantaneous value of \( i_o \) as:

\[
i_o(t) = I_m \sin(\omega t - \varphi)
\]

where \( I_m \) is the amplitude of the phase current, \( \omega \) is the phase angular frequency, and \( \varphi \) is the initial phase angle.

From (3)–(9), the instantaneous value of \( \Delta v_o \) can be expressed as:

\[
\Delta v_o(t) = \begin{cases} 
-(V_{on0} + \frac{I_{d_{eq}}E}{T}) - rI_m \sin(\omega t - \varphi), & \varphi + 2k\pi \leq \omega t < \varphi + 3k\pi \\
V_{on0} + \frac{I_{d_{eq}}E}{T} + rI_m \sin(\omega t - \varphi), & \varphi + 3k\pi \leq \omega t < \varphi + 4k\pi
\end{cases}
\]

(10)

It is noted that \( \Delta v_o(t) \) is the superposition of a square and a sinusoidal waves with a period of \( 2\pi \), and they are both odd-symmetrical about axial of \( \omega t = \varphi \). Then (10) can be decomposed by Fourier transform:

\[
\Delta v_o(t) = -(K + rI_m) \sin(\omega t - \varphi) - K \sum_{n=1}^{\infty} \frac{1}{2n+1} \sin[(2n+1)(\omega t - \varphi)]
\]

(11)

where

\[
K = \frac{4V_{on0}}{\pi} + \frac{4I_{d_{eq}}E}{\pi T}
\]

(12)

As shown in (11), a fundamental variation and odd harmonics with decreasing amplitude are introduced to \( v_o \). Moreover, the value of \( K \) is independent of \( v_{\alpha,ref} \), which means a serious distortion is introduced at the condition of a low modulation index. For the load voltage and current in the three-phase three-wire system as shown in Figure 1, the harmonics with \( 3n \) times of fundamental frequency are canceled out. Whereas, the fundamental variation and the harmonics with \( (6n \pm 1) \) times of fundamental frequency still remain.

5.2. Compensation Control Strategy

According to the previous analysis, the non-ideal factors compensation control (NFCC) for the seven-level VMC is proposed, as shown in Figure 6. Current sensors are required to acquire the phase current. The compensation value (\( \Delta v_{ref} \)) is obtained in each switching cycle for the reference voltage (\( v_{ref} \)). In this way, the output distortion caused by non-ideal factors can be compensated.

![Figure 6. Control diagram for the seven-level VMC.](image)

6. Experiment Results

To verify the validity of the above-mentioned analysis and control strategy, a 7.2 kVA prototype of the three-phase seven-level VMC was designed and constructed as shown in Figure 7. Six cascaded DC power supplies with \( E = 120 \) V are employed to provide DC-link input. In addition, three-phase
resistors in series with inductor filter are connected in Y-style for the load of the converter. The values of $V_{\text{off}}$, $r$, $t_{\text{on}}$, and $t_{\text{off}}$ can be obtained in the datasheet of switches and diodes. Other main system parameters are shown in Table 4.

![Controller](image1)

**Figure 7.** Experiment platform of the three-phase seven-level VMC.

### Table 4. Experimental parameters.

| Parameters                  | Symbol | Value |
|-----------------------------|--------|-------|
| DC-link voltage             | $V_{dc}$ | 720 V |
| Modulation index            | $m$    | 0.86  |
| Fundamental frequency       | $f$    | 50 Hz |
| Carrier frequency           | $f_s$  | 10 kHz|
| Load resistance             | $R$    | 20 Ω  |
| Filter inductance           | $L_f$  | 2 mH  |
| Dead-time                   | $t_d$  | 2 μs  |

The experimental results are shown in Figures 8–12. Among them, Figures 8–11 illustrate the operation characteristics of the seven-level VMC without the NFCC. Figure 12 shows the comparison results for the NFCC.

![Waveforms](image2)

**Figure 8.** Waveforms of output voltage ($m = 0.86$).
The distortion caused by the THD decreases from 7.36% to 5.50%. The voltage distribution of series switches $S_{10}$ and $S_{11}$ is shown in Figure 11. The voltage of $S_{10a}/S_{10b}/S_{11a}/S_{11b}$ is clear in Figure 12. Among them, Figure 10 shows the voltage and current waveforms of load ($m = 0.86$).

Figure 9. FFT analysis of $v_A (m = 0.86)$.

Figure 10. Output voltage and current of load ($m = 0.86$).

Figure 11. Voltage distribution of $S_{10}$ and $S_{11} (m = 0.86)$.
Figure 12. Comparison results of phase current for the NFCC: (a) phase current waveforms \( m = 0.2 \); (b) phase current waveforms \( m = 0.86 \); (c) FFT analysis \( m = 0.2 \); (d) FFT analysis \( m = 0.86 \); (e) vector trajectory \( m = 0.2 \); (f) vector trajectory \( m = 0.86 \).

Figure 8 shows the output waveforms of \( v_A \) and \( v_{AB} \). As can be seen, \( v_A \) contains seven levels and \( v_{AB} \) contains eleven levels at \( m = 0.86 \), the voltage of each level is 120 V. Each voltage ladder is clear, no multilevel voltage jumping is observed. In the zoom-in picture of \( v_A \), a voltage drop of the conduction path at state 0 can be observed. \( V_{on} \) changes polarity with the direction of \( i_{oa} \), and its value increases with \( |i_{oa}| \) from 4 V to 6.5 V.

FFT analysis of \( v_A \) is illustrated in Figure 9. The total harmonic distortion (THD) is 24.4\%, and most harmonics are distributed around the switching frequency. It is noted that the non-ideal factors cause a fundamental voltage loss of about 22 V (rated value is 310 V), and low order odd harmonics are also observed in the zoom-in picture. This distortion will be compensated after the NFCC is applied.

Figure 10 shows the voltage and current waveforms of the load. The high-frequency harmonics are attenuated by a filter, then good load voltage and current waveforms are achieved. The THD of the phase current is 2.24\%.

The voltage distribution of series switches \( S_{10,1} \) and \( S_{11} \) are shown in Figure 11. Each switch withstands static voltage of 60 V \((E/2)\) and 120 V \( E \) respectively in one fundamental cycle. When
the switches are turned off, the total blocking voltage of $S_{10}$ or $S_{11}$ is 120 V, so the dynamic voltage of the single switch caused by the switching inconsistencies will not exceed its rated value. Detailed waveforms are shown in the zoom-in picture, the voltage spike results from stray inductance are about 15 V.

It can be seen from Figure 8 to Figure 11, the VMC operates well under the presented switching states and the modulation method. The dynamic voltage unbalancing in series switches and multilevel voltage jumping of the output voltage are avoided.

Figure 12 illustrates the comparison results of $i_o$ for the NFCC at both $m = 0.2$ and $m = 0.86$. The experimental results at $m = 0.2$ are provided in Figure 12a,c,e. The current waveforms, FFT analysis, and vector trajectory are illustrated respectively. Noted that, after the NFCC is applied, an obvious improvement of the waveform and vector trajectory can be observed in Figure 12a,e. In Figure 12c, the amplitude of the fundamental current increases from 91.0% to 100.1% of the rated value (3.6 A), the content of 5th and 7th harmonics are reduced, the THD decreases from 7.36% to 5.50%.

The comparison results at $m = 0.86$ are shown in Figure 12b,d,f. As seen in Figure 12d, the amplitude of the fundamental current increases from 95.1% to 99.4% of the rated value (15.5 A), and the THD decreases from 2.24% to 1.88%. The distortion caused by the non-ideal factors is compensated well by the NFCC, which means better waveforms and vector trajectory are achieved, as shown in Figure 12b,e.

7. Conclusions

A new seven-level V-clamp multilevel converter (VMC) is presented and implemented in this paper. From the analysis and experimental results, the following conclusions can be obtained:

1. The seven-level VMC reduces the clamping devices compared with conventional topologies.
2. With the switching states designed in this paper, the VMC is free of the issues on dynamic voltage unbalancing in series switches and multilevel voltage jumping in its output voltage.
3. With the proposed non-ideal factors compensation control, the output fundamental distortion is well compensated and the THD is reduced.

The theoretical and experimental validity of the seven-level VMC is demonstrated. This topology shows good potential for medium-voltage high-power applications.

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