Segmented Successive Cancellation List Polar Decoding with Tailored CRC

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Abstract As the first error correction codes provably achieving the symmetric capacity of binary-input discrete memory-less channels (B-DMCs), polar codes have been recently chosen by 3GPP for eMBB control channel. Among existing algorithms, CRC-aided successive cancellation list (CA-SCL) decoding is favorable due to its good performance, where CRC is placed at the end of the decoding and helps to eliminate the invalid candidates before final selection. However, the good performance is obtained with a complexity increase that is linear in list size \( L \). In this paper, the tailored CRC-aided SCL (TCA-SCL) decoding is proposed to balance performance and complexity. Analysis on how to choose the proper CRC for a given segment is proposed with the help of virtual transform and virtual length. For further performance improvement, hybrid automatic repeat request (HARQ) scheme is incorporated. Numerical results have shown that, with the similar complexity as the state-of-the-art, the proposed TCA-SCL and HARQ-TCA-SCL schemes achieve 0.1 dB and 0.25 dB performance gain at frame error rate FER = 10\(^{-2}\), respectively. Finally, an efficient TCA-SCL decoder is implemented with FPGA demonstrating its advantages over CA-SCL decoder.

Keywords Polar codes · segmented CA-SCL · tailored CRC · HARQ · VLSI

1 Introduction

Polar codes, proposed by Arıkan [1, 2], are considered as a breakthrough of coding theory. It is shown that polar codes can provably achieve the symmetric capacity of binary-input discrete memory-less channels (B-DMCs) [2]. Besides the capacity achieving performance, the asset of polar coding compared to the state-of-the-art (SOA) is its corresponding low-complexity decoding algorithms. Therefore, polar codes have been adopted by 3GPP for eMBB control channels.

Though linear programming (LP) decoder [3], successive cancellation (SC) decoder, and belief propagation (BP) decoder [4, 5] have been proposed for polar codes, their performance is not comparable with maximum likelihood (ML) decoder. Thus, the breadth-first SC decoder named SC list (SCL) decoder, was proposed by [6, 7]. Cyclic redundancy check (CRC), widely adopted for error detection, has been proved as a simple and effective enabler for further performance improvement with respect to SCL decoder. Numerical results have shown that, CRC-aided SCL (CA-SCL) decoder [8] achieves at least no worse performance than the SOA turbo and low-density parity-check (LDPC) decoders [9]. Usually, CRC is placed at the end of decoding to eliminate invalid candidates before final decision. The disadvantages are: 1) Though has better performance than SCL decoder, CA-SCL decoder still suffers from time and space complexity regarding the list size \( L \). 2) For intermediate candidates which have already gone wrong, no early elimination could be taken...
in time until the decoding end is reached, and the computation afterward is in vain.

To address the complexity and redundancy, [10] proposed a segmented CA-SCL (SCA-SCL) decoder. At the same time, [11] independently proposed a partitioned CA-SCL (PSCL) decoder, which is similar as the SCA-SCL decoder but with a different partition method. Both decoders divide code bits into segments and insert CRC bits in between, to rule out invalid candidates per segment rather than to wait until the decoding ends. Thus, they can reduce redundancy while keeping comparable performance as CA-SCL decoders. However, existing decoders usually apply the same CRC length to the same number of information or code bits. Though convenient, those straightforward schemes fail to take the code construction into consideration. It is not clear whether the existing uniform partition schemes are optimal and whether better performance can be achieved with the same number of CRC bits.

To our best knowledge, no existing literature has discussed the CRC distribution for SCA-SCL decoding, and its hardware implementation. Analysing the CRC requirement by unequal-length segments and introducing concepts of virtual transform and virtual length, this paper devotes itself in figuring out a tailored CA-SCL (TCA-SCL) decoding of improved performance and lower complexity than SOA. An HARQ-TCA-SCL decoding is proposed for further performance improvement. Contributions of this paper are: 1) Efficient CRC distribution is proposed for the first time, showing performance advantage over SOA. 2) This paper does not limit itself to specific decoder design, but proposes a formal TCA methodology, which can be readily applied to any existing SCA-SCL decoders. 3) The efficient implementation methodology is also proposed and verified with FPGA implementations.

The remainder of the paper is organized as follows. Section 2 reviews the preliminaries. Section 3 analyzes the SCA-SCL decoders for possible refinement. The TCA-SCL decoding is given in Section 4. The HARQ-TCA-SCL decoding is given in Section 5. Section 6 gives the performance and complexity analysis of the proposed decoding schemes. Section 7 proposes a hardware architecture for TCA-SCL decoding. FPGA implementations are given in the same section. Finally, Section 8 concludes the entire paper.

2 Preliminaries

2.A Polar Codes

Denote the input alphabet, output alphabet, and transition probabilities of a B-DMC by $\mathcal{X}$, $\mathcal{Y}$, and $W(y|x)$. With block length $N = 2^n$, the information vector, encoded vector, and received vector are $u^N_1 = (u_1, ..., u_N)$, $x^N_1 = (x_1, ..., x_N)$, and $y^N_1 = (y_1, ..., y_N)$. The polar encoding is given by

$$x^N_1 = u^N_1 G_N = u^N_1 B_N F^{\otimes n},$$

(1)

where $G_N$ and $B_N$ are the generation matrix and bit-reversal permutation matrix respectively, and $F = [1 \, 0 \, 1 \, 1]$. Transmitting channels between $x^N_1$ and $y^N_1$ are $W^{(i)}_N(y^N_1, u^{i-1}_1 | u_i)$, derived by channel combining

$$W^N(y^N_1 | x^N_1) = W^N(y^N_1 | u^N_1 G_N)$$

(2)

and channel splitting

$$W^{(i)}_N(y^N_1, u^{i-1}_1 | u_i) = \sum_{u_i} \frac{1}{N} W^N(y^N_1 | x^N_1), i = 1, ..., N.$$  (3)

Define $I(W)$ as the symmetric capacity. For B-DMC $W$ and $\delta \in (0, 1)$, $W^{(i)}_N$ polarizes: as $N$ goes to infinity via powers of 2, $I(W^{(i)}_N) \in (1 - \delta, 1)$ approaches $I(W)$ and $I(W^{(i)}_N) \in (0, \delta)$ approaches $(1 - I(W))$. In $(N, K)$ codes, the K most reliable channels with indices in information set $A_1$ are chosen to transmit the K information bits in $u^N_1$, whereas the others, with indices in frozen set $A_0$, transmit the $(N - K)$ frozen bits.

2.B SC and SCL Polar Decoders

The SC polar decoding tree is a full binary tree. Fig. 1 shows a toy example for $N = 8$. For each node at the $n$-th level, two possible choices are 0 and 1. Each set consisting of all the leaf nodes is associated with a unique estimated codeword $\hat{u}_N = (\hat{u}_1, \hat{u}_2, ..., \hat{u}_N)$. If $i \in A_1$, $\hat{u}_i = 0$. Otherwise, the SC decoder computes its log-likelihood ratio (LLR):

$$L^{(i)}_N(y^N_1, \hat{u}^{i-1}_1) = \log \frac{W^{(i)}_N(y^N_1, \hat{u}^{i-1}_1 | u_i = 0)}{W^{(i)}_N(y^N_1, \hat{u}^{i-1}_1 | u_i = 1)},$$

(4)

and generates its decision as

$$\hat{u}_i = \begin{cases} 0, & \text{if } L^{(i)}_N(y^N_1, \hat{u}^{i-1}_1) \geq 0; \\ 1, & \text{otherwise}. \end{cases}$$

(5)

The LLR updating is conducted based on the two equations listed in Eq. (6). $\text{max}^*$ denotes the Jacobi logarithm:

$$\text{max}^*(x_1, x_2) \triangleq \ln(e^{x_1} + e^{x_2}) = \max(x_1, x_2) + \ln(1 + e^{-|x_1 - x_2|}).$$

(7)

This recursive process starts from each (sub-)tree’s root and always traverses the left branch before the right (Fig. 1). When the leaf level is reached, hard decision is made and returned to the parent node.

As a greedy search algorithm, SC decoding keeps only one path based on step-wise decision, with complexity of $O(N \log N)$. However, this single-candidate
\[ L_N^{2^{(i-1)}}(y_1^N, \hat{u}_{2i-2}^N|u_{2i-1}) = \max^* \left( L_{N/2}^{(i)}(y_1^{N/2}, \hat{u}_{2i-2}^{N/2} \oplus \hat{u}_{2i-1}^{N/2}|u_{2i-1}) + L_{N/2}^{(i)}(y_{N/2+1}^{N}, \hat{u}_{2i-2}^{N}|0) \right), \]
\[ L_{N/2}^{(i)}(y_1^{N/2}, \hat{u}_{2i-2}^{N/2} \oplus \hat{u}_{2i-1}^{N/2}|u_{2i-1}) + L_{N/2}^{(i)}(y_{N/2+1}^{N}, \hat{u}_{2i-2}^{N}|1) \right) + L_{N/2}^{(i)}(y_{N/2+1}^{N}, \hat{u}_{2i-2}^{N}|u_{2i}). \]

Fig. 1 Tree illustration of SC decoding process.

method only guarantees the local optimality, and will possibly result in incorrect result. To this end, the SCL decoding, which keeps a list of \(L\) survivals, was proposed by [6, 7] independently. Fig. 2 illustrates the difference between SC and SCL algorithms. The complexity of SCL decoder is \(O(L N \log N)\). At the \(i\)-th step, if \(i \in \mathcal{A}\), the SCL decoder splits each current path into two paths with both \(\hat{u}_i = 0\) and \(\hat{u}_i = 1\). Out of the \(2L\) paths, only the \(L\) best ones are kept. Finally, the decoder chooses the best path at the end of decoding process.

Fig. 2 SC decoding and SCL decoding with \(L = 2\).

Fig. 3 CA-SCL polar decoding.

2.C CA-SCL Polar Decoder

For further improvement, CA-SCL decoder introduces CRC as a detection tool at the end of decoding [8]. Illustrated in Fig. 3 CRC detector helps to decide which candidates are possibly correct before metric comparison. Here, \(m\) denotes the number of CRC bits. The CRC-passed candidate with the largest metric value is chosen as the final result. If no candidate passes the CRC detection, a decoding failure is claimed.

3 Segmented CA-SCL Decoding Schemes

In this section, we first introduce two SCA-SCL decoding schemes, then propose a refined version. Without loss of generality, the \((1024, 512)\) code [2] is employed as a running example, whose polarization is in Fig. 4. Here \(W\) is a BEC with erasure probability \(\epsilon = 0.5\). \(I(W_N^{(i)})\) is computed by:
\[
\begin{align*}
&I(W_N^{(2i-1)}) = I(W_N^{(i/2)})^2, \\
&I(W_N^{(2i)}) = 2I(W_N^{(i/2)}) - I(W_N^{(i)})^2;
\end{align*}
\]
with \(I(W^{(1)}) = 1 - \epsilon\). The blue stars in Fig. 4 denote the information bits, whereas the red points denote the frozen bits.

Fig. 4 Channel polarization for a BEC with \(\epsilon = 0.5\).

3.A Comparison of Different Segmented Schemes

To the authors’ best knowledge, there are two segmented CRC-aided SCL methods. The PSCL scheme proposed
in [11] aims to reduce memory consumption, and applies uniform partitions to code bits for implementation convenience. The hardware reduction comes at the cost of some performance loss compared to the conventional CA-SCL algorithm and always forces the number of candidate paths to 1 after each CRC. The SCA-SCL scheme proposed in [10] aims to reduce both the time and space complexity. Uniform segments are applied to information bits and CRC is employed as a tool to eliminate decoding redundancy without harming the performance.

Let \( P \) denote the number of segments. For PSCL decoder, the index set of Segment-\( i \) is \( T_i \) \((1 \leq i \leq P)\). | \( \cdot \) | denotes the cardinality of one set. We have
\[
\sum_{i=1}^{P} |T_i| = N, \quad \text{and} \quad |T_1| = N/P. \tag{9}
\]
For SCA-SCL decoder, the index set of Segment-\( i \) is \( S_i \) \((1 \leq i \leq P)\). we have
\[
\sum_{i=1}^{P} |S_i| = N, \quad \text{and} \quad |S_i \cap A| = K/P. \tag{10}
\]

One simple example of \( P = 4 \) is illustrated in Fig. 5.

Theoretically, both schemes are similar but differ in the partition methods. PSCL decoding employs uniform code bit partition, which is implementation friendly. However, since only one candidate can survive after each CRC, small performance degradation is expected, especially in low SNR region. SCA-SCL decoding employs uniform information bit partition, which can keep the performance as CA-SCL decoding while successfully reducing the space and time complexity. This advantage comes from the decoding flexibility. However, the flexibility will make the implementation more complicated.

### 3.B PSCL with Early Termination

The first observation is that, both schemes apply the same CRC to the uniformly partitioned segments. Without looking into the symmetric capacity of each binary channel, this straightforward scheme may not be optimal. The second observation is that both schemes have their own merits, it would be smarter to merge them together. In other words, it is estimated that we can propose a new approach which is both implementation friendly and adaptive.

One simple mixture of both schemes is to introduce early termination to PSCL decoding. However, this simple combination may not be reasonable in certain cases. Fig. 5 gives an example with \( P = 4 \). Shown in Fig. 5 for the (1024, 512) code with \( m = 32 \), the information lengths of four segments are 20, 123, 156, and 245, respectively. If uniform CRC bits are employed, the first segment has \( |T_1^i| = |T_1| - |C_1| = 12 \) information bits and the last segment has \( |T_4^i| = |T_4| - |C_4| = 237 \) information bits. It is unreasonable to use the same 8-bit CRC to both the 12-bit and 237-bit segments. To this end, the TCA-SCL decoding is proposed in the following section.

### 4 CA-SCL Decoding with Tailored CRC

In this section, we first discuss how to measure the requirement of CRC bits for different segments. Then the concepts of virtual transform and virtual length are introduced. A visualization method of polarized channel's symmetric capacity is also proposed. The detailed TCA-SCL decoding is finally proposed. It should be noted that though the TCA-SCL decoding is based on uniform partition of code bits, it can be readily applied to other uniform or nonuniform partition schemes.

#### 4.A Requirement of CRC Length for Polar Codes

Assume a total of \( m \) CRC bits are available and are divided into \( P \) segments \( C_1, C_2, \ldots, C_P \). It may not be suitable to set \( |C_1| = |C_2| = \ldots = |C_P| \) for \( P \) segments with different lengths. How to measure the requirement of the CRC length for each segment is critical. To the authors’ best knowledge, no literature has addressed this specific problem. To maintain the same error detection capability in the situation of independent channels, it is concluded that longer sequence requires more CRC bits [12]. However, this conclusion does not suit polar codes because the reliability of different channels are different. A reasonable measurement on requirement of CRC length should take both sequence length and symmetric capacity into account. In the following, concepts of virtual transform and virtual length are proposed to this end.

#### 4.B Virtual Transform and Virtual Length

Including CRC bits, we always pick the \( K + m \) most reliable bits out of \( N \) based on the symmetric capacity

![Fig. 5 Different segmented decoding schemes with P = 4.](image-url)
The virtual value of the channel is 

\[ I(W_i^{(i)}) \] with \( i \in \mathcal{A} \), \( \mathcal{A}' \) is the new information set including CRC bits, and \( |\mathcal{A}'| = K + m \). Calculate \( I \) as follows:

\[
I = \frac{1}{K + m} \sum_{i \in \mathcal{A}'} I(W_i^{(i)}).
\]  \hspace{1cm} (11)

**Definition 1 Virtual Transform** To operate the virtual transform, we first calculate \( I'(i) \):

\[
I'(i) = \frac{I}{I(W_i^{(i)})}.
\]  \hspace{1cm} (12)

The virtual value of the channel is

\[
J(i) = \begin{cases} 
1 + \frac{(I'(i) - 1)}{2(1 - I)}, & \text{if } I'(i) \geq 1; \\
1 - \frac{(1 - I'(i))}{2(1 - I)}, & \text{if } I'(i) < 1.
\end{cases}
\]  \hspace{1cm} (13)

**Definition 2 Virtual Length** The summation of \( J(i) \) in the \( k \)-th segment is its virtual length:

\[
vl_k = \sum_{i \in \{ T_k \cap \mathcal{A}' \}} J(i).
\]  \hspace{1cm} (14)

The CRC allocation is given by

\[
|C_1| : \ldots : |C_P| = \text{adjust} \left( \frac{m \times vl_1}{\sum_{i=1}^{P} vl_i}, \ldots, \frac{m \times vl_P}{\sum_{i=1}^{P} vl_i} \right),
\]  \hspace{1cm} (15)

where \( \text{adjust}() \) is a function which adjusts the allocation results to near integers and takes the following steps: 1) find an unmarked \( k \) which has minimum \( \lfloor \text{ROUND}(\frac{m \times vl_i}{\sum_{i=1}^{P} vl_i}) \rfloor \), then mark \( k \) and set \( |C_k| = \text{ROUND}(\frac{m \times vl_i}{\sum_{i=1}^{P} vl_i}) \); 2) repeat step 1) for \( P - 2 \) times; 3) Assume the left unmarked index is \( k' \). Set \( |C_k'| = m - \sum_{i \neq k'} |C_i| \), where \( 1 \leq i \leq P \).

4.C Visualization of Channel Symmetric Capacity

Before we give more details of the proposed TCA-SCL decoding, one visualization method of symmetric capacity is proposed for easy understanding and illustration. In this visualization, the gradient colors from iridescent are used to demonstrate the symmetric capacity of each channel. According to the legend, the more symmetric capacity approaching 1 (0), the more bathochromic (hypsochromic) it will be. Fig. 8(a) shows the visualization for polar codes with \( N = 64 \).

**Example 1** For \( (1024, 512) \) polar codes with 32 CRC bits, visualization of code bits is given in Fig. 8(b).

The visualization of 512 information bits is given in Fig. 8(c). For TCA-SCL decoding, set \( P = 4 \). According to Definition [2], the ratio of virtual lengths is:

\[
vl_1 : vl_2 : vl_3 : vl_4 = 3.54 : 9.84 : 10.91 : 7.70.
\]  \hspace{1cm} (16)

which is illustrated by Fig. 8(d). Then the CRC allocation is obtained according to Eq. (15):

\[
|C_1| : |C_2| : |C_3| : |C_4| = 3 : 10 : 11 : 8.
\]  \hspace{1cm} (17)

The refined CRC allocation based on virtual length is given in Fig. 8(e).

**Remark 1** Generally speaking, the hypsochromic part in the visualization chart mainly contributes to the virtual length. The more hypsochromic segment requires more CRC bits.

This refined SCA-SCL decoding based on virtual length is named TCA-SCL decoding. Details of TCA-SCL decoding is given as follows. The corresponding performance and implementation are discussed in Section 4 and Section 7.

4.D Tailored CA-SCL Decoding

The detailed tailored CA-SCL decoding is given in this subsection. For TCA-SCL encoding, we set \( P \) segments
and perform the virtual transform to obtain the corresponding virtual lengths. Then we allocate the CRC bits according to the ratio of virtual lengths before polar encoding.

Here, \( \text{addCRC}(\cdot) \) is function which performs Eq. (15). Function \( \text{encoder}(\cdot) \) performs conventional polar encoding. For TCA-SCL decoding, SCL decoding with early termination is performed as follows. Here, the function \( SCL'(\cdot) \) is the SCL decoding for Segment-\( j \). Define \( U_i \) as the the output paths set of SCL(\( \cdot \)) in \( i \)-th segment. Define \( \text{passCRC}(\cdot) \) as the function which checks if at least one path of \( U_i \) can pass the CRC. If one or more than one path can pass the CRC, the path with the largest metric of them is chosen to refresh \( \hat{u}_N^j \).

### 5 TCA-SCL Decoding with HARQ

Besides early termination, the proposed TCA-SCL decoding can also work in a HARQ way when segmented CRC fails. HARQ has been widely used in delay insensitive communication systems for a capacity-approaching throughput [13][15]. Recently, HARQ has been considered for polar decoding. [16] introduced a HARQ scheme based on a class of rate-compatible polar codes constructed by performing punctures and repetitions using punctured polar coding [17]. An incremental redun-

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**Algorithm 1 TCA-SCL Polar Encoding**

**Input:** \( u_N^1, I(W^{(i)}_N), N, K, m, P \).

1. Set \( P \) segments;
2. \( I = \frac{1}{N} \sum_{i \in A^1} I(W^{(i)}_N) \);
3. for \( i = 1; i <= N; i + + \) do
4. \( I'(i) = I/I(W^{(i)}_N) \);
5. if \( I'(i) \geq 1 \) then
6. \( J(i) = 1 + \frac{(I'(i)-1)}{2(I-1)} \);
7. else
8. \( J(i) = 1 - \frac{(1-I'(i))}{2(I-1)} \);
9. end if
10. end for
11. for \( k = 1; k <= P; k + + \) do
12. \( v_{l_k} = \sum_{i \in \{T_k \cap A^1\}} J(i) \);
13. end for
14. \( \text{addCRC}(u_N^1, v_{l1}, v_{l2}, ..., v_{lP}) \);
15. \( x_N^1 = \text{encoder}(u_N^1) \).

**Output:** \( x_N^1 \).
Algorithm 2 TCA-SCL Polar Decoding

Input: $y_i^N$, $N$, $P$, $L$.
1: for $i = 1$; $i <= P$; $i += 1$ do
2: $U_i = \text{SCL'}(y_i^N, i, L);$ 
3: if passCRC($U_i$) = false then 
4: break;
5: end if
6: refresh $\hat{u}_i^N$ by the survival path in $U_i$;
7: end for

Output: $\hat{u}_i^N$.

Algorithm 3 HARQ-TCA-SCL Polar Decoding

Input: $y_i^N$, $T$, $P$, $L$.
1: $i = 1$;
2: for $j = 1$ to $P$ do
3: mark = false;
4: while $i < T$ and mark = false do
5: $U_j = \text{SCL'}(y_i^N, j, L);$ 
6: mark = passCRC($U_j$);
7: if mark = false then 
8: $i = i + 1$;
9: Retransmit and combine Segment-$j$;
10: end if
11: end while
12: if mark = false then
13: break;
14: end if
15: refresh $\hat{u}_i^N$ by the survival path in $U_j$;
16: end for

Output: $\hat{u}_i^N$.

The proposed HARQ-TCA-SCL scheme is illustrated in Fig. 9. Let $i$ denotes the current number of times a transmission attempted, $T$ denotes the maximum retransmission times, and $j$ ($\leq P$) denotes the current position of the segments. The details of HARQ-TCA-SCL scheme are listed as follows:

We initialize $i = 1$ for the HARQ-TCA-SCL decoding, then perform the SCL decoding for Segment-$j$ (function SCL'($\cdot$)) and obtain CRC results on each survival path at the end of segment SCL decoding. If at least one path can pass CRC, we save the path with the highest probability and move to the next segment. Otherwise, we update $i$ to $i + 1$, combine Segment-$j$ with the retransmitted part and the old ones, redo the TCA-SCL decoding. Algorithm terminates with a decoding failure if $i = T$.

6. Performance and Complexity Analysis

6.A Performance Analysis

In this subsection, performance comparison between different algorithms is given with binary-input additive white Gaussian noise channels (BI-AWGNCs). Different code lengths, rates, and partition schemes are considered: for Fig. 10(a), we have $N = 64$, $K = 36$, $m = 8$, and $P = 2$; for Fig. 10(b), we have $N = 1024$, $K = 512$, $m = 32$, and $P = 4$. The information set $A$ is selected according to [2, 19]. We use corresponding hex value to represent CRC polynomial. For example, a CRC-4 detector with polynomial $g(D) = D^4 + D + 1$ is described as CRC-4 (0x9) in this paper (the ‘+1’ is implicit in the hex value). For (64,36) code, we set 2 copies of CRC-4 (0x9) for (HARQ-)PSCL scheme, and CRC-5 (0x12) and CRC-3 (0x5) for (HARQ-)TCA-SCL scheme. For (1024,512) code, we set 4 copies of CRC-8 (0xA6) for (HARQ-)PSCL scheme, and CRC-3 (0x5), CRC-10 (0x327), CRC-11 (0x583), and CRC-8 (0xA6) for (HARQ-)TCA-SCL scheme. All the CRC detectors are with the best CRC generation polynomial suggested by [12].

According to Fig. 10, compared with the PSCL scheme, the proposed TCA-SCL scheme has a 0.1 dB perfor-
1.5 2 2.5 3 3.5 4 4.5 5
10
−4
10
−3
10
−2
10
−1
10
0
Eb/N 0 (dB)
FER
PSCL
TCA−SCL
HARQ−PSCL ( T = 3)
HARQ−TCA−SCL ( T = 3)

(a) (N = 64, K = 36, m = 8, P = 2)

(b) (N = 1024, K = 512, m = 32, P = 4)

Fig. 10 FER comparison of (HARQ-)TCA-SCL and (HARQ-)PSCL schemes.

Fig. 11 Average list sizes of (HARQ-)TCA-SCL and (HARQ-)PSCL schemes.

Suppose the i-th frame is retransmitted $R_i$ times ($0 \leq R_i \leq T$). For the HARQ-TCA-SCL decoder, $L_H$ is calculated as

$$L_H = \frac{L \times \sum_{i=1}^{F} (P_i + R_i)}{P \times F}.$$  (19)

For low SNR, thanks to the early termination $L_T$ is small due to high error rate. On the other hand, a larger number of retransmissions leads to a higher $L_H$ for HARQ-TCA-SCL decoder. As SNR increases, $L_T$ and $L_H$ converge to $L$: 1) TCA-SCL decoder is more likely to finish the decoding process, and 2) the retransmission time of HARQ-TCA-SCL decoder converges to 0. It should be noted that, according to Eq. (18) and (19) $0 \leq L_H - L_T \leq \frac{L}{P} T$.

Shown in Fig. 11 (HARQ-)TCA-SCL scheme has the same complexity as (HARQ-)PSCL scheme. The HARQ-TCA-SCL scheme has 50.3% and 38.5% higher complexity than the PSCL scheme at SNR = 1.5 dB.

6.B Complexity Analysis

Define the product of the actual decoding length and list size as the average list size. Since the average computational complexity is proportional to the average list size, here we analyze the average list sizes of TCA-SCL and HARQ-TCA-SCL decoders denoted by $\bar{L}_T$ and $\bar{L}_H$, respectively. Assume the total frame number is $F$, and the decoder ends at the $P_i$-th segment of the i-th frame. For the TCA-SCL decoder, $\bar{L}_T$ can be calculated as

$$\bar{L}_T = \frac{L \times \sum_{i=1}^{F} P_i}{P \times F}.$$  (18)
for (64, 36) and (1024, 512) codes, respectively. As SNR goes up, the complexity of HARQ-TCA-SCL scheme tends to be as same as the PSCL scheme asymptotically with better performance.

7 Efficient TCA-SCL Decoder Architectures

To facilitate the application of the proposed TCA-SCL decoder, efficient architectures and FPGA implementations are proposed in this section and are also given to demonstrate its merits. Since hardware consumption and decoding latency are two main concerns of SCL family decoder, the proposed architecture aims to achieve a good balance in between. The HARQ-TCA-SCL decoder can also be designed similarly.

7.A Hardware Consumption Analysis

7.A.1 Full Module TCA-SCL Architecture

In this subsection, a full module TCA-SCL architecture is proposed, which is mainly based on the conventional folded SC architecture proposed in [20]. The architecture for full module TCA-SCL decoder is illustrated in Fig. 12. It divides all mixed node modules (MNs) into \( n = \log_2 N \) stages, and each MN implements two types of calculations mentioned in Eq. (6). According to the conclusions in [20], for an \( N \)-bit SC decoder, \((N - 1)\) MNs are required. For an \( N \)-bit CA-SCL decoder, \( L(N - 1)\) MNs are employed.

**Theorem 1** For one \( P \)-segmented TCA-SCL decoder with list \( L \), the total number of MNs is

\[
MN_{\text{total}} = N - L + (L - 1) \frac{N}{P}. \tag{20}
\]

**Proof** For the given decoder, its MNs can be categorized into two parts. The first part includes Stages 1 to \( \log_2 P \). The second part includes Stages \((\log_2 P + 1)\) to \( n \). It should be noted that since \( N \) is power of 2, \( \log_2 P \) is always an integer.

Since each segment outputs only one candidate, the first part obeys SC decoding rule, and list size \( L \) is not necessary. The number of MNs is

\[
MN_1 = \sum_{i=1}^{\log_2 P} \frac{N}{2^{i-1}} = N - \frac{N}{P}. \tag{21}
\]

The second part obeys CA-SCL decoding rule without considering the fine-gain scheduling. The number of MNs is

\[
MN_2 = L \sum_{i=\log_2 P+1}^{n} \frac{N}{2^{i-1}} = L(N - \frac{N}{P} - 1). \tag{22}
\]

Since the memory block corresponds to MNs, the memory complexity is as follows

**Corollary 1** Assume the quantization length for the LLR message is \( q \), the memory bits required are

\[
\text{mem}_{\text{total}} = q \times MN_{\text{total}} = q \left( N - L + (L - 1) \frac{N}{P} \right). \tag{23}
\]

The list core (LC) module in Fig. 12 mainly implements the sorting operation. In order to reduce both the sorting latency and complexity, the efficient distributed sorting (DS) proposed in [21] is employed here.

7.A.2 Folded Module TCA-SCL Architecture

Thanks to the early termination scheme, the proposed full module architecture for TCA-SCL decoding is memory efficient compared to conventional CA-SCL decoding. However, the hardware utilization ratio (HUR) of MNs is very low. Borrowing the fine-folding idea proposed in [21, 22], this paper then proposes the folded module TCA-SCL architecture for higher HUR. We set up a sub-decoder with \( (2^{\lceil n/2 \rceil} - 1)L \) MNs for Stage 1 to \([n/2]\). Stage \((n/2) + 1\) to \( n \) can also be implemented by this sub-decoder in a time-multiplexing manner. Fig. 13 gives an example of a even \( n \), Stage 1 and Stage \( n/2 + 1 \), Stage 2 and Stage \( n/2 + 2 \), ... Stage \( n/2 \) and Stage \( n \) are time-multiplexing. If \( n \) is odd, Stage 1 and Stage \((n + 1)/2 + 1\), Stage 2 and Stage \((n + 1)/2 + 2\), ..., Stage \((n + 1)/2 - 1\) and Stage \( n \) are time-multiplexing, and Stage \((n + 1)/2\) uses the last stage alone. Parameter \( j \) in Fig. 13 denotes the current folding order. However, the characteristics in Section 7.A.1 which helps to reduce the complexity of the first \( \log_2 P \) stages could not be employed here, because folding technique is based on uniform hardware. The complexity is

**Theorem 2** For one folded module TCA-SCL decoder with list \( L \), the total number of MNs is

\[
MN_{\text{total}} = (2^{\lceil n/2 \rceil} - 1)L. \tag{24}
\]

**Proof** When implementing Stage 1 to \([n/2]\), all the input and output multiplexers choose mode ‘0’. \( 2^{\lceil n/2 \rceil} + 1 \) executions are required to output \( 2^{\lceil n/2 \rceil} + 1 \) LLLRs for Stage \([n/2]\). For \( P \)-segmented decoder, if \( \log_2 P \geq \lceil n/2 \rceil \), \((2^{\lceil n/2 \rceil} - 1)(L - 1)\) MNs are idle during this decoding stage. Otherwise, according to Eq. (21), \((2^{\lceil n/2 \rceil} - 2^{\lceil n/2 \rceil}/P)(L - 1)\) MNs are idle. Therefore, \((2^{\lceil n/2 \rceil} - 1)L\) MNs are sufficient.

When implementing Stage \([n/2] + 1\) to \( n \), all the input and output multiplexers choose mode ‘1’. Since \( 2^{\lceil n/2 \rceil} + 1 \) LLLRs become the input of the sub-decoder, no MN is idle during this stage. Therefore, the total number of MNs is \((2^{\lceil n/2 \rceil} - 1)L\).

**Theorem 3** Assume the quantization length for the LLR message is \( q \), the memory bits required by the folded...
module TCA-SCL architecture is
\[ \text{mem}_{\text{total}} = q \left( N - L + (L - 1) \frac{N}{q} \right) \].

**Proof** The folded design only reduces the complexity of MNs. However, the memory complexity stays the same as the full module TCA-SCL architecture.

Table 2 gives FPGA results in accordance with Theorem 3.

### 7.7. Timing Analysis

#### 7.7.1 Single Frame Scheme

As Fig. 12 shown, the decoding process for TCA-SCL has the following steps: 1) In Segment \( j \), MNs complete the main decoding in Eq. (6). The 2L LLRs correspond to \( \hat{u}_i \) for each path. 2) 2L LLRs are input to the LC module. DS method [21] is employed to select the best \( L \) paths. 3) The memory is updated and partial sum vector \( \hat{u}_{\text{sum}} \) is calculated for \( \hat{u}_{i+1} \). 4) We repeat the above steps to get the \( L \) paths for \( \hat{u}_i \). Then, \( \hat{u}_{\overline{x}_j} \) is directly chosen as ‘0’ or ‘1’ for each path without decoding. After that, we input information bits in \( \hat{u}_{\overline{x}_j} \) for 2L paths to CRC\(_j\) to pick up the only path for Segment \( j+1 \). CRC is implemented with linear feedback shift register (LFSR) [23], and determines the coefficient of XOR. Shown in Fig. 12, \( P \) CRC modules are employed. It should be noted that here CRC\(_j\) takes care of 2L paths in serial manner. Admittedly, designers can process 2L with parallel CRCs. Considering the simple
CRC and its short processing time, serial manner is employed here.

The scheduling of this single frame (SF) scheme is shown in Fig. 14(a). The latency of SF TCA-SCL decoder is

\[ T_{SF} = T_{CA} + 2L(T_1 + \ldots + T_{P-1}). \]  

(25)

**Theorem 4** Assume the latency of CA-SCL is \( T_{CA} \) clock cycles. The latency for CRC \( T_{crc} \) is \( T_i \). For one SF \( P \)-segmented TCA-SCL decoder with list \( L \), the decoding latency is

\[ T_{SF} = T_{CA} + 2L(T_1 + \ldots + T_{P-1}). \]  

Proof After checking all 2L paths of Segment \( i \), the decoder selects one path and begins to decode Segment \( (i+1) \). In SF scheme, segmented CRC scheme increases latency for serial checking of Segment \( i \)

\[ T_{crc} = 2LT_i. \]  

(26)

In SF scheme, checking Segment \( P \) of Frame 1 and decoding Segment 1 of Frame 2 can be done at the same time. Since the checking time is shorter than decoding time, the latency increase is

\[ T_{inc} = 2L \sum_{i=1}^{P-1} T_i. \]  

(27)

Now the proof is immediate.

Folded module TCA-SCL decoder can also work in the proposed SF scheme.

**Corollary 2** Assume the folding technique introduces \( F \) extra clock cycles per frame, the latency of SF folded module TCA-SCL decoder is

\[ T_{SF} = T_{CA} + F + 2L(T_1 + \ldots + T_{P-1}). \]  

(28)

7.B.2 Double Frame Scheme

SF decoding introduces \( 2L(T_1 + \ldots + T_{P-1}) \) extra clock cycles per frame. During CRC detection, all MNs are idle and HUR is therefore low. To this end, the double frame (DF) scheme is proposed.

The main idea of DF is shown in Fig. 14(b). Two frames are decoded simultaneously in an interleaved manner: when Frame 1 checks (decodes) its Segment \( i \), Frame 2 decodes (checks) its Segment \( (i-1) \). Since both frames share the same architecture, every time a new segment is decoded, all LLRs in memory belong to the other frame. If we keep the decoding latency of each frame the same as CA-SCL decoder, Stage 1 to \( \left( \log_2 P - 1 \right) \) need an extra memory block of \( q(N - L + (L-1) \frac{N}{P}) \) bits to save LLRs, which is not appreciated by hardware design.

If no extra memory is available, each new segment begins its decoding with Stage 1. In this way, DF scheme still requires a memory block of \( q(N - L + (L-1) \frac{N}{P}) \) bits with slightly increased latency. For DF full module TCA-SCL decoder:

**Theorem 5** For one DF \( P \)-segmented TCA-SCL decoder with list \( L \), the decoding latency is

\[ T_{DF} = T_{CA} + P \log_2 P - 2P + 2. \]  

(29)

Proof For the interleaved manner in Fig. 14(b) the latency of each segment is

\[ T_{seg_i} = \max\{T_{dec_i}, T_{crc_i}\}, \]  

(30)

where \( T_{dec_i} \) denotes the SCL decoding latency for Segment \( i \), which includes SC decoding and DS.

According
to [24], the DS latency for Segment $i$ is approximately $2LT_i$, therefore

$$T_{\text{dec}_i} > 2LT_i.$$  \hfill (31)

Since $T_{\text{crc}_i} = 2LT_i$

$$T_{DF} = \sum_{i=1}^{P} T_{\text{seg}_i} = \sum_{i=1}^{P} T_{\text{dec}_i}.$$  \hfill (32)

It is believed that there are $2^i$ segments, which could calculate from Stage $(i+1)$, now calculates from Stage 1 and introduce latency of $i \cdot 2^i$. Therefore, the decoding increased latency is

$$T_{\text{inc}} = \sum_{i=1}^{\log_2 P - 1} i \cdot 2^i = P \log_2 P - 2P + 2.$$  \hfill (33)

Now the proof is immediate.

Folded module TCA-SCL decoder can also work in the proposed DF scheme with the following latency.

**Corollary 3** Assume the folding technique introduces $F$ extra clock cycles per frame, the latency of DF folded module TCA-SCL decoder is

$$T_{DF} = T_{\text{CA}} + F + P \log_2 P - 2P + 2.$$  \hfill (34)

Table 1 shows comparison between five different schemes: CA-SCL decoder, SF (DF) full module TCA-SCL decoders, and SF (DF) folded module TCA-SCL decoders. According to Section 4.C, CRC allocation is $(|C_1|, |C_2|, |C_3|, |C_4|) = (3, 10, 11, 8)$. Data in red show the example of $N = 1024$, $K = 512$, $P = 4$, and $L = 2$.

### 7.C FPGA Implementation Results

To better demonstrate the advantages of the proposed TCA-SCL decoders, FPGA implementations based on Altera Stratix V are given as well. To be in accordance with Table 2, five decoders have been implemented. The same parameters as the aforementioned example are employed here: $N = 1024$, $K = 512$, $m = 32$, $P = 4$, and $L = 2$. All the five decoders employ the same LLR quantization scheme of 1 sign bit, 6 integer bits, and 1 decimal bit. In Fig. 15, the FER performance comparison of floating SC and quantized-SC with $q = 8$ bits indicates the validity of the quantized scheme.

The implementation results are compared in terms of adaptive logic modules (ALMs), registers, and memory bits. It is shown that, compared to the CA-SCL decoder, TCA-SCL (SF or DF) decoder can achieve 18.8% or 15.0% ALMs reduction. For further ALMs reduction, with the help of folding technique, FTCA-SCL (SF or DF) decoder consumes 40.11% or 42.9% ALMs compared to TCA-SCL (SF or DF) with slightly increased latency, as analyzed in [22]. It is also observed that the ALMs’ reduction is not that much as the reduction of MNs listed in Table 1. This is because Table 1 does not consider the comparison part, which introduces major part of ALMs consumption and stays the same between different architectures.

For implementation convenience, here memory has been employed by both folded decoders. Therefore, we consider the sum of registers and memory bits as the total memory consumption. It is observed TCA-SCL (SF or DF) decoder requires 77.03% or 82.1% memory compared to the CA-SCL decoder. Also, the introduction of folding technique does not affect the memory cost, which has been indicated by Theorem 3. Comparing FTCA-SCL (DF) decoder and FTCA-SCL (SF) decoder, when DF scheme is employed, the latency can be reduced 15.90% at the cost of 11.90% increased ALMs.

For the latency issue, since the critical paths of all designs are determined by the critical path of the same SC decoding kernel, we believe it is safe to compare in term of clock number. It is shown that the segmented CRC decoders will introduce more latency due to more serial CRC operations. Second, the DF scheme is more time efficient. Third, the folded versions come at the cost of higher latency.

In general, the proposed four architecture of DC-SCL decoding can reduce the hardware consumption compared to CA-SCL decoder. Designers can choose the suitable one according to different application requirements.

### 8 Conclusions

In this paper, a segmented SCL polar decoding with tailored CRC is proposed. Method on how to choose the proper CRC for a given segment is proposed with help.
of concepts of virtual transform and virtual length. Numerical results have shown that the proposed TCA-SCL decoder can achieve better performance and lower complexity than conventional CA-SCL decoder. Thanks to the more reasonable CRC partition scheme, the TCA-SCL decoder can also outperform the PSCL decoder. For further performance improvement, HARQ-TCA-SCL scheme is proposed at the cost of increased complexity. Efficient architectures and FPGA implementations are also proposed for a good balance between hardware consumption and decoding latency.

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