Effect of high-k dielectric material on the characteristics of Single Gate and Double Gate Multi-Channel Junctionless Nanowire Transistors

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Abstract. In this work, we have designed and analyzed the performance characteristics of n-type silicon based multi-channel junctionless nanowire transistors (JLNTs) for both single gate and double gate configurations. Numerical simulations using CVT (lambardi) model has been carried out to investigate the effects of different device parameters such as gate insulator dielectric, gate insulator thickness, and separating materials between channels. To illustrate and evaluate the performances, input characteristic curves, transconductance, and $I_{on}/I_{off}$ ratio of the devices have been extracted. It is observed that $I_{on}/I_{off}$ ratio are directly affected by the variation of dielectric and thickness of the gate. Devices having a high-κ dielectric provides steeper characteristics and better $I_{on}/I_{off}$ ratio for both the structures. The value of transconductance is also found to be greater for high-κ dielectric in both configurations with the double gate providing a higher value compared to the single one.

Keywords. High-κ dielectric, Junctionless Transistors, Multi-channel, Double Gate, Transconductance

1. Introduction
MOSFETs with multigate are proposed and designed to overcome the limitations and promising issues of classical planar device structure [1, 2]. In a multigate transistor the channel (the basis for conduction) gets surrounded by the gate from separate directions. Thus providing the device an opportunity to secure a better control of the channel [3], which is not feasible with the traditional design of planar transistors. It (multigate), therefore, has been proven to be an advantageous device that shows reduced short-channel-effects (SCEs) and low leakage currents [4]. Moreover, fabricating junctions in intersection of drain and channel or source and channel is considered to be a complicated process in manufacturing industry, as the junction needs a very sharp doping concentration gradient with decreasing channel length. So, junctionless transistor has become the real effective solution to save a lot of time and efforts of the engineers. Basically no junctions exist between drain/source and channel to give an eminent way out to the junction manufacturing crisis [5].

In terms of fabricating the devices, junctionless transistors contain a channel that has a doping concentration of uniform dimension, for which engineers have a viable option. Taking consideration of this easier process, several research works have been already conducted, where suppressed SCEs (low drain-induced barrier-lowering (DIBL) and leakage currents) are reported...
Though the behavior of junctionless device with double gate having single channel is already studied extensively, double gate with multi-channel is yet to be explored in detail. However, junctionless technology with multi-channels are considered in a recent work, in which little bit of oscillation peaks have been observed in drain current for combined effect of current flowing through multiple channels [10]. Thus, combining double gate with multi-channel is a potential field of study to have better control over the channel.

In this research, multi-channel JLNTs in both single gate (SG) and double gate (DG) configurations are studied using the CVT model to explore their performance parameters. A rigorous comparison of performance attributes - $I_D$ vs $V_{GS}$ characteristic and $I_{on}/I_{off}$ ratio - of the SG and DG devices is also demonstrated in terms of using different gate insulators and different sets of oxide thickness, keeping the channel length unaltered. Moreover, a transconductance study is also carried out on the devices of both configurations for investigating the effects of different gate insulators. 

Figure 1: (a) Cross-sectional (left) and 3D view (right) of the Single Gate multi-channel JLNT and (b) Cross-sectional (left) and 3D view (right) of the Double Gate multi-channel JLNT.

2. Device Structure and Modeling
We have employed the inversion-layer-model of Lombardi (CVT) using SILVACO TCAD software for the simulation purpose. In this model, different mobility components are combined by Matthiessen’s rule to get the total mobility ($\mu_{total}$) [11, 12]. Any other mobility model gets overridden by this type of model, which is used to include phonon-scattering limited mobility, field-dependent mobility, surface-roughness induced mobility, and impurity-scattering limited mobility [13]. Because of having high doping concentration in channel region, in JLNTs, surface roughness induced mobility components dominates to degrade the mobility in the flat-band and partial-depletion-mode [14]. Furthermore, we have chosen Gummel’s method, which performs Gummel iteration for the Newton solution. The parameters used in the JLNTs are estimated using Shockley-Read-Hall (SRH), Newton Gummels numerical methods, and CVT.

Table 1: Design parameters of our simulated device.

| Parameter                  | Value          |
|----------------------------|----------------|
| Doping concentration      | $10^{19} \text{cm}^{-3}$ |
| Channel Thickness         | 4 nm           |
| Gate dielectric material  | $SiO_2, Si_3N_4, HfO_2$ |
| Gate oxide thickness      | 1, 1.25, 1.5   |
| Dielectric constant       | 3.9, 6.2, 22   |

Schematic views of our designed SG and DG multi-channel JLNTs are depicted in Figures 1a and 1b, respectively. Device parameters considered in our study are also presented in
Table 1. While keeping the doping concentration, channel length, and channel thickness fixed at $10^{19} \text{cm}^{-3}$, 4 nm, and 15 nm respectively, oxide thickness and gate dielectric are varied for both structure to evaluate their effects on the performance. Transconductance is also analyzed by varying gate dielectric for both the structures.

3. Results and Discussions

3.1. Effects on Transfer Characteristics

Three gate dielectrics - SiO$_2$ (Silicon Dioxide), Si$_3$N$_4$ (Silicon Nitride) and HfO$_2$ (Hafnium Oxide) - with a doping concentration and oxide thickness of $10^{19} \text{cm}^{-3}$ and 1 nm are considered to study their effects on the $I_D$ vs $V_{GS}$ curves of both SG and DG multi-channel JLNTs. These characteristic curves are illustrated in Figures 2a and 2b, respectively for the SGJLNT and DGJLNT, with a fixed channel length of 15 nm. It is evident from the figures that the transfer characteristics curve tends to be steeper for high-$\kappa$ dielectric in both the devices with that of DGJLNT being steeper than the SGJLNT in every cases. As evident from the figures, HfO$_2$ provides the highest threshold voltage $V_{th}$ for its dielectric constant being the greatest among the materials considered.

![Figure 2a](image1.png)  
![Figure 2b](image2.png)

**Figure 2:** (a) Drain Current $I_D$ as a function of gate to source voltage $V_{GS}$ for different dielectric materials used in gate oxide for single gate and (b) double gate multi-channel JLNTs with channel length $L_g = 15$ nm, $T_{ox} = 1$ nm and $V_{DS} = 0.3$V.

3.2. Effects on $I_{on}/I_{off}$ ratio

$I_{on}/I_{off}$ ratio for three different gate dielectrics in both SGJLNT and DGJLNT are presented graphically in Figure 3a. The better performance of DGJLNT for each dielectric is clearly evident from the figure here. Double gate structures, surrounding the channel from both sides, provides greater control of the channel. Thus, reducing gate leakage in off state and enhancing carrier concentration in on state increases the $I_{on}/I_{off}$ ratio. Again, both the structures seem to have higher $I_{on}/I_{off}$ ratio for high-$\kappa$ dielectric, which is HfO$_2$ in our study. The highest value of $I_{on}/I_{off}$ ratio is found to be around $1.2 \times 10^9$ for SGJLNT and $10^8$ for DGJLNT for HfO$_2$, providing a significant improvement of almost $10^5$ times for the later.

Again, oxide thickness is changed from 1 to 1.50 nm, keeping other parameters constant, to observe its (oxide thickness) effect on $I_{on}/I_{off}$ ratio for both the structures. The graphical illustration of this study is presented in Figure 3b. Comparing the results, we can see that double
Figure 3: (a) $I_{on}/I_{off}$ ratio as a function of dielectric constant of different gate dielectric materials with $T_{ox} = 1\, \text{nm}$ and $V_{DS} = 0.3\, \text{V}$ for SG and DG JLNTs and (b) $I_{on}/I_{off}$ ratio as a function of gate oxide thickness with $L_g = 20\, \text{nm}$ and $V_{DS} = 0.5\, \text{V}$ for both configurations.

Gate structure provides more $I_{on}/I_{off}$ ratio than the single one. As higher oxide thickness degrades gate-voltage’s control over the channel, $I_{on}/I_{off}$ ratio is decreased along with the increment of oxide thickness for both. Capacitive action of the devices increases along with the decrement of $T_{ox}$, which enhances the volume-depletion of the channel in off-state. This gives reduced $I_{off}$, resulting in a higher $I_{on}/I_{off}$ ratio. This consistency of $I_{on}/I_{off}$ ratio of our study is coherent with the result found by M. Haque et al. and Jamwal et al. [15, 16].

3.3. Transconductance Comparison

Figure 4: (a) Transconductance as a function of gate voltage for single gate and double gate multi-channel JLNTs with $T_{ox} = 1\, \text{nm}$ and $L_g = 20\, \text{nm}$ (b) Transconductance comparison for different dielectric gate insulator with $L_g = 15\, \text{nm}$.

For 1 nm $T_{ox}$ and 20 nm $L_g$, transconductance of SG multi-channel JLNT and DG multi-
channel JLNT is shown for different gate voltages in Figure 4a. From the figure, it is obvious that the transconductance of DGJLNT is enhanced as compared to SGJLNT. The Transconductance is defined as, \( g_m = \frac{dI_D}{dV_{GS}} \). It is seen from Figure 4a that the trans-conductance gets increased with an increase in gate voltage, reaches a peak, and then shows a decreasing trend. The transconductance of a JLNT describes the gain. So, Double gate structure converts voltage to current more efficiently, thus improves the performances of transistors by enhancing the effective-gate area surrounding the channel.

A comparative study of transconductance for different gate dielectric insulator materials are also conducted with 15 nm channel length for both SGJLNT and DGJLNT structures. As depicted in Figure 4b, high-\( \kappa \) dielectric (\( HfO_2 \)) provides higher value of transconductance for both - 53 \( \mu \)S for double gate and 34 \( \mu \)S for single gate. For every dielectric the double gate device has sharp peak with higher value compared to the lower broadened peak of single gate device. DGJLNT, therefore, ensures higher intrinsic DC gain for having maximum transconductance.

3.4. Different insulation materials between the channels

![Figure 5](a) \( I_D \) vs \( V_{GS} \) characteristic curve for different insulation between channels for Single gate and (b) Double gate multi-channel JLNTs with \( T_{ox} = 1 \) nm, \( L_g = 15 \) nm and \( V_{DS} = 0.5 \) V.

Three different insulating materials have been used between the channels of the device to explore the effect of interaction among the conducting channels. In Figures 5a and 5b, the transfer characteristic of the transistor has been illustrated for single gate and double gate JLNTs respectively. Since all channels simultaneously conduct, huge amount of current flows from the drain to the source. So, the interaction between the channels is becoming a challenge for multiple channel transistor design. It is more intensified when channel length is smaller. Because the presence of heavy current causes electromagnetic flux interference, and thus, resulting in bumps and dips in the continuous curve. So the desire of achieving maximum current is not fulfilled. To get remedy from these situations, we investigate the effects of using different dielectric insulators between the channels. From Figures 5a and 5b, it can be realized that high-\( \kappa \) dielectric compound (Nitride) provides better performance in both structures compared to the lower ones (air and oxide). The insulator materials considered in the study is such that they can be easily deposited in the bulk with electrical and chemical properties taken into accounts.
4. Conclusion
We have found that high-$\kappa$ dielectric material in gate dielectric results in better performance in terms of input characteristics, transconductance, and $I_{on}/I_{off}$ ratio in both single gate and double gate devices. Lower leakage current in off-state and higher current in on-state, achieved through high-$\kappa$ dielectric, improves $I_{on}/I_{off}$ ratio significantly. For a specific material to be used in insulation between gate and channels, $I_{on}/I_{off}$ ratio performance can be depicted from the results. Moreover, for having greater control over the channel, double gate multichannel JLNT architecture is found to provide noteworthy improvement in all the above-mentioned performance parameters compared to the single one. As reported in our study, overall improvement of junctionless transistors can be achieved with double gate structure by implementing high-$\kappa$ material in gate dielectric and insulation between channels.

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