The design, analysis, and simulation of an optimized all-optical AND gate using a Y-shaped plasmonic waveguide for high-speed computing devices

Surya Pavan Kumar Anguluri · Srinivas Raja Banda · Sabbi Vamshi Krishna · Sandip Swarnakar · Santosh Kumar

Received: 13 March 2021 / Accepted: 20 July 2021 / Published online: 6 August 2021
© The Author(s), under exclusive licence to Springer Science+Business Media, LLC, part of Springer Nature 2021

Abstract
All-optical logic gates have proven their significance in the digital world for the implementation of high-speed computations. We propose herein a novel structure for an all-optical AND gate using the concept of a power combiner based on a Y-shaped metal–insulator–metal waveguide with a 4 µm × 7 µm footprint. This design works based on the principle of linear interference. The insertion loss and extinction ratio of the design are given as 0.165 and 14.11 dB, respectively. The design is analyzed by using the finite-difference time-domain (FDTD) method and verified using MATLAB. The minimized structure can be used to design any complex logic circuit to achieve better performance in the future.

Keywords All-optical logic gates · Metal–insulator–metal waveguide · Y-combiner · Linear interference · Plasmonic · FDTD

1 Introduction
Communication now plays a unique role in everyday human life. As technology advances, the need for faster communication also advances at the same pace. Along with the speed of communication, several other factors must be considered when designing a device, including the cost of the individual circuit, the size of the device, its power handling capacity, heat dissipation issues, and interconnect delays [1]. The first generation of electronics was based on semiconductor technology, making use of vacuum tube-based transistors for logical operations, but suffering from effects such as strong heat dissipation and interconnect delays [2]. These limitations were somewhat mitigated by the next technology, called photonics [3, 4]. In this field, instead of electrons, photons are used to exchange information [5]. However, optical devices suffer from the diffraction limit when their size approaches the operating wavelength [6]. Also, the size of optical components is nearly 1000 times larger than electronic devices, which represents another drawback [7]. The next generation of technology came with a new proposal called surface plasmons, where optical signals interact with metallic structures at the nanoscale, resulting in the new field called plasmonic [8, 9] that combines the effects of a miniaturized version of electronics with the capacity of photonics [10]. When light of a certain wavelength is incident on a metal surface, free electrons are excited by absorbing the energy from the light but are bound at the interface between the metal and dielectric [11]. These surface plasmon polaritons (SPPs) can avoid the diffraction limit found in photonics.

* Sandip Swarnakar
sandipswarnakar.2008@gmail.com
1 Department of Electronics and Communication Engineering, Godavari Institute of Engineering and Technology, Chaitanya Knowledge City, East Godavari, Rajahmundry, Andhra Pradesh 533296, India
2 Department of Electronics and Communication Engineering, Ravindra College of Engineering for Women, Nandikotkur Road, Kurnool, Andhra Pradesh 518452, India
3 Photonics Lab, Department of Electronics and Communication Engineering, G. Pullaiah College of Engineering and Technology, Nandikotkur Road, Kurnool, Andhra Pradesh 518002, India
4 Department of Electrical and Electronics and Communication Engineering, DIT University, Dehradun, Uttarakhand 248009, India
5 Shandong Key Laboratory of Optical Communication Science and Technology, School of Physics Science and Information Technology, Liaocheng University, Liaocheng 252059, Shandong, China

© Springer
SPPs can confine and control light beyond the diffraction limit, while the losses inside SPPs can be overcome by using different waveguides such as metal–insulator–metal (MIM) [15, 16], insulator–metal–insulator (IMI), and dielectric-loaded surface plasmon polariton waveguide (DLSPPW) [14, 17–24]. Among these, the MIM waveguide is best suited because of its capacity to confine light to deep subwavelength [2, 16]. Logic gates are the basic building blocks of all digital circuits. Several optical devices such as the directional coupler (DC), Mach–Zehnder interferometer (MZI), power combiners, and power splitters are used to realize different logic gates such as AND, OR, NOT, XOR, and XNOR, as well as universal gates such as NAND and NOR [25–32, 45–48]. These all-optical logic gates can thus be used to design all combinational circuits such as multiplexers, demultiplexers, code converters, adders and subtractors, and parity generators [33–41]. In this paper, a minimized design for an all-optical AND gate is proposed based on a power combiner using a Y-shaped waveguide [42] and verified using the FDTD method [43]. Section 2 describes the design of the Y-combiner, followed by the design of the AND gate. Simulation results are presented in Sect. 3. Section 4 includes an analysis of the results, where the present work is also compared with previously reported works, while Sect. 5 provides the conclusions on the proposed design.

2 The design of the AND gate using a Y-combiner

The proposed design for the AND gate using a Y-combiner operates on the principle of linear interference [42]. The inputs applied to the arms of the power combiner are controlled by an external phase shifter to obtain the desired output of the logical AND gate. The Y-combiner is designed using the S-bend sine waveguide, whose equation is defined as

$$y(t) = \frac{D - 2 \times W}{4} + \frac{D}{4} \cos \left( \frac{\pi t}{L} \right). \quad (1)$$

where $D$ is the input separation gap between the two arms of the combiner, $W$ is the width of the waveguide, and $L$ is the length of the S-bend-shaped waveguide. The waveguide is structured using Eq. (1), as shown in Fig. 1.

Another waveguide of the S-bend shape is arranged symmetrically along the X-axis to obtain the Y-combiner.

In this paper, an all-optical AND gate is designed using the concept of a power combiner with the help of a Y-shaped waveguide. The design of the Y-combiner is achieved by combining two symmetrical S-bend structures, joined at one end to form a Y-shaped structure as shown in Fig. 2.

The above structure is designed using a plasmonic waveguide by keeping the refractive index as 2.1. The final minimized structure is obtained as a result of altering the parameters of the Y-combiner such as the S-bend length, the input separation gap, and the length of the linear waveguide.

By keeping the input separation gap at 3 µm, various parameters such as the peak output power in the ON state, the peak output power in the OFF state, the Y-angle, and the extinction ratio (ER) can be calculated when varying the S-bend length, as presented in Table 1. revealing that

![Fig. 1 The structure of the S-bend sine waveguide](image1)

![Fig. 2 A schematic of the symmetric Y-combiner](image2)

| S. no. | S bend length (µm) | $P_{ON}$ | $P_{OFF}$ | Extinction ratio (dB) |
|--------|-------------------|----------|-----------|----------------------|
| 1      | 4.3               | 1.9668   | 0.0916    | 13.31                |
| 2      | 4.2               | 1.9516   | 0.0903    | 13.34                |
| 3      | 4.1               | 1.9462   | 0.0889    | 13.40                |
| 4      | 4                 | 1.9156   | 0.0878    | 13.38                |
| 5      | 3.9               | 1.9300   | 0.0869    | 13.47                |
| 6      | 3.8               | 1.9267   | 0.0871    | 13.44                |
| 7      | 3.7               | 1.9250   | 0.0879    | 13.40                |
| 8      | 3.6               | 1.9099   | 0.0879    | 13.37                |
the ER is maximum for an S-bend length of 3.9 µm with a value of 13.47 dB. A plot of the S-bend length versus ER is shown in Fig. 3.

Similarly, the mentioned parameters are calculated by varying the input separation gap while keeping the S-bend length constant at $L = 3.9$ µm, yielding the values presented in Table 2.

From Table 2, at the value of $D = 2.6$ µm, the ER is found to be greater than the previously noted value, reaching 13.62 dB. A plot of the input separation gap versus the ER is shown in Fig. 4.

The S-bend length and the input separation gap are now kept constant at 3.9 and 2.6 µm, respectively, while the length of the linear waveguide is modified to obtain the maximum extinction ratio. The ER for various lengths of the linear waveguide is presented in Table 3.

The ER is found to be larger for a linear waveguide length of 2.9 µm, reaching 14.11 dB, which is significantly greater

**Table 2** The extinction ratio for various input separation gaps at $L = 3.9$ µm

| S. no. | $D$ (µm) | $P_{ON}$ (0.084) | $P_{OFF}$ (0.088) | Extinction ratio (dB) |
|--------|-------------|-----------------|-----------------|---------------------|
| 1 | 3.2 | 1.9109 | 0.0884 | 13.34 |
| 2 | 3.1 | 1.9425 | 0.0888 | 13.39 |
| 3 | 3.0 | 1.9300 | 0.0869 | 13.46 |
| 4 | 2.9 | 1.9401 | 0.0851 | 13.57 |
| 5 | 2.8 | 1.9905 | 0.0873 | 13.58 |
| 6 | 2.7 | 2.0181 | 0.0883 | 13.59 |
| 7 | 2.6 | 2.0307 | 0.0883 | 13.62 |
| 8 | 2.5 | 2.0585 | 0.0895 | 13.61 |

**Table 3** The extinction ratio for various lengths of the linear waveguide

| S. no. | Linear (µm) | $P_{ON}$ (0.0807) | $P_{OFF}$ (0.0815) | Extinction ratio (dB) |
|--------|-------------|-----------------|-----------------|---------------------|
| 1 | 3.1 | 2.0307 | 0.0883 | 13.62 |
| 2 | 3 | 2.0526 | 0.0807 | 14.05 |
| 3 | 2.9 | 2.0775 | 0.0806 | 14.11 |
| 4 | 2.8 | 2.0781 | 0.0813 | 14.07 |
| 5 | 2.7 | 2.0845 | 0.0815 | 14.07 |
| 6 | 2.6 | 2.0865 | 0.0815 | 14.08 |
| 7 | 2.5 | 2.0941 | 0.0928 | 13.53 |
| 8 | 2.4 | 2.0956 | 0.0938 | 13.49 |

**Fig. 3** A plot of the S-bend length versus the extinction ratio at $D = 3$ µm

**Fig. 4** The input separation gap versus the extinction ratio at $L = 3.9$ µm

**Fig. 5** The linear waveguide length versus the extinction ratio at $L = 3.9$ µm and $D = 2.6$ µm
than already obtained values. A plot of the linear waveguide length versus the ER is shown in Fig. 5.

The final dimensions of the Y-combiner at which the maximum ER is obtained are presented in Table 4.

### Table 4 The design parameters for the AND gate using a Y-combiner

| S. no. | Parameter       | Value  |
|--------|-----------------|--------|
| 1      | S-bend length (L) | 3.9 µm |
| 2      | Input separation (D) | 2.6 µm |
| 3      | Linear length    | 2.9 µm |
| 4      | Refractive index of waveguide | 2.1 |
| 5      | Width of the waveguide | 0.25 µm |

### Table 5 The simulation parameters for the AND gate using a Y-combiner

| Parameter                        | Value |
|----------------------------------|-------|
| Type of polarization             | TE    |
| Wavelength                       | 1.55 µm |
| Mesh size X (µm)                 | 0.0114 |
| Mesh size Z (µm)                 | 0.0114 |
| No. of mesh cells X              | 349   |
| No. of mesh cells Z              | 603   |
| Input field transverse           | Gaussian |
| Low-intensity signal power       | 1 × 10⁹ W/m |
| High-intensity signal power      | 3 × 10⁹ W/m |

### Table 6 The truth table for the AND gate along with the phase and transmission efficiency

| Inputs | A | B | Input phase A | Input phase B | Phase difference | Transmission efficiency (%) | (A × B) |
|--------|---|---|---------------|---------------|------------------|-----------------------------|---------|
| 0      | 1 | 180° | 0°          | 180°          |                  | 19.67                       | 0       |
| 1      | 0 | 180° | 0°          | 180°          |                  | 21.64                       | 0       |
| 1      | 1 | 0°   | 0°          | 0°            |                  | 152.6                       | 1       |

3 The simulation results for the AND gate using FDTD

The minimized design of the logical AND gate is verified using MATLAB and FDTD simulations. The analysis of the structure is carried out with the help of the FDTD method.

A continuous wave of 1550 nm is applied at both input terminals of the Y-combiner. The input optical signals with power of 1 × 10⁹ and 3 × 10⁹ W/m are considered as the low and high optical intensity signals. The entire simulation is carried out in the transverse electric (TE) mode of the plasmonic waveguide, excited by a source with a Gaussian wave for both inputs. The simulation parameters of the proposed design are presented in Table 5.

As shown in the truth table for the AND gate in Table 6, the output of the AND gate is high when both of the inputs are high; otherwise, it is low. The timing diagram of the AND gate is shown in Fig. 6, as verified using MATLAB, where the two input signals A and B are represented by first and second row while the last row represents the output of the logical AND gate.

Case 1: A = 0 and B = 0

In this case, the two inputs of the Y-combiner are given a low-intensity signal with power 1 × 10⁹ W/m. According to the truth table of the AND gate, the output power is low.

A phase difference of 180° is created between the two input signals. Since the two input signals have the same amplitude...
and are out of phase, destructive interference will occur and the output of the AND gate is low \(Y = 0\).

**Case 2: \(A = 0\) and \(B = 1\)**

In this case, the upper arm of the combiner is provided with the low-intensity signal \(1 \times 10^9 \text{ W/m}\) while the lower arm of the combiner is given the high-intensity signal \(3 \times 10^9 \text{ W/m}\). A phase shift of 180° is introduced between the two input signals. Similarly, in case of \(A = 0\) and \(B = 0\), destructive interference will occur, which in turn reduces the intensity of the output signal. Hence, the output of the AND gate is low \(Y = 0\). The optical field propagation for logic “0 & 1” is shown in Fig. 7a.

**Case 3: \(A = 1\) and \(B = 0\)**

Unlike the previous case, here the upper arm of the combiner is provided with the high-intensity signal \(3 \times 10^9 \text{ W/m}\) while the lower arm is supplied with the low-intensity signal \(1 \times 10^9 \text{ W/m}\). Thereby, due to the similar amplitudes of the input signals and out of phase \(180^\circ\) relation, again destructive interference will occur, making the output of the AND gate be low \(Y = 0\). The optical field propagation for logic “1 & 0” is shown in Fig. 7b.

**Case 4: \(A = 1\) and \(B = 1\)**

In this case, both input ports of the power combiner are supplied with a high-intensity signal \(3 \times 10^9 \text{ W/m}\). Here, the phase difference between the signals is made to 0°. According to the principle of constructive interference, when two signals have the same amplitude and same phase difference, then the intensity of the output signal will be twice the input signal intensity \(Y = 1\). The optical field propagation for logic “1 & 1” is shown in Fig. 7c.

All the input combinations along with the phase values are presented in Table 6.

### 4 An analysis of the results

The proposed device has a footprint of 7 µm × 4 µm. Performance parameters such as the insertion loss and extinction ratio are calculated from the output results. The insertion loss is given by

\[
\text{Insertion Loss (IL)} = 10 \log_{10} \left( \frac{P_{out}}{P_{in}} \right),
\]

where \(P_{out}\) is the peak output power and \(P_{in}\) is the peak input power.

The extinction ratio is defined as

\[
\text{Extinction ratio (ER)} = 10 \log_{10} \left( \frac{P_{out|ON}}{P_{out|OFF}} \right),
\]

where \(P_{out|ON}\) is the output optical power in the ON state and \(P_{out|OFF}\) is the output optical power in the OFF state.

The IL and ER in this work are found to be 0.165 and 14.11 dB, respectively. For better performance of logic gates, the insertion loss should be low while the extinction ratio should be as high as possible [44]. The current work is
compared with previously published works in terms of the mentioned parameters in Table 7.

### 5 Conclusions

An all-optical AND logic gate is designed with the help of a Y-shaped plasmonic MIM waveguide. The design has an area of $4 \times 7 \ \mu m^2$, which is smaller when compared with previous works. Key parameters such as the insertion loss and extinction ratio are calculated. The IL and ER in this work are found to be 0.165 and 14.11 dB, respectively. Design parameters such as the S-bend length, input separation gap, and linear waveguide are optimized to obtain the maximum extinction ratio and minimize the losses inside the waveguide. Due to its simple structure and controllability, the Y-combiner-based AND gate can provide a new method to implement logic functions in digital electronics. This design has a minimized structure and can also be used in future work to design ultracompact devices for fast optical computing.

### Acknowledgements

This work was supported by the Science and Engineering Research Board, India (grant no. TAR/2018/000051).

### Availability of data and materials

The authors can provide the data on request.

### Code availability

No source code is available for this manuscript.

### Declarations

**Conflict of interest** The authors declare that they have no conflict of interest.

**Consent to participate** For this type of study formal consent is not required.

### References

1. Cotter, D., Manning, R.J., Blow, K.J., Ellis, A.D., Kelly, A.E., Nesset, D., Phillips, I.D., Poustie, A.J., Rogers, D.C.: Nonlinear optics for high-speed digital information processing. Science 286(5444), 1523–1528 (1999)
2. Kumar, S., Singh, L.: Proposed new approach to design all-optical AND gate using plasmonic-based Mach-Zehnder interferometer for high-speed communication. In: Proceedings of SPIE, Nanophoton, VI, vol. 9884, pp. 1–7 (2016)
3. Tang, Y., Zeng, X., Liang, J.: Surface plasmon resonance: an introduction to a surface spectroscopy technique. J. Chem. Educ. 87(7), 742–746 (2010)

5. Wu, Y.D.: Nonlinear all-optical switching device by using the electric-loaded surface plasmon-polariton waveguides. Phys. Rev. B 75(24), 1–12 (2007)
6. Holmgaard, T., Bozhevolnyi, S.I.: Theoretical analysis of dielectric-loaded surface plasmon-polariton universal gates using plasmonics Mach-Zehnder interferometer for WDM applications. Plasmonics 13, 1277–1286 (2018)

7. Ozbay, E.: Plasmonics: merging photonics and electronics at nanoscale dimensions. Science 311(5758), 189–193 (2006)
8. Gibbs, H.M.: Optical bistability: controlling light with light. Academic, New York (1985)

9. Hu, X., Jiang, P., Ding, C., Yang, H., Gong, Q.: Picosecond and low-power all-optical switching based on an organic photonic-bandgap microcavity. Nat. Photon. 2(3), 185–189 (2008)
10. Harashi, S., Okamoto, T.: Plasmonics: visit the past to the future. J. Phys. D: Appl. Phys. 45, 1–24 (2012)
11. Barnes, W.L., Deraux, A., Ebbesen, T.W.: Surface plasmon subwavelength optics. Nature 424, 824–830 (2003)
12. Zhang, Q., Huang, X.G., Lin, X.S., Tao, J., Jin, X.P.A.: Subwavelength coupler-type MIM optical filter. Opt. Exp. 17(9), 7549–7554 (2009)
13. Talebi, N., Mahjoubfard, A., Shahabadi, M.: Plasmonic ring resonator. J. Opt. Soc. Am. B 25(12), 2116–2122 (2008)
14. Gramotnev, D.K., Bozhevolnyi, S.I.: Plasmonics beyond the diffraction limit. Nat. Photon. 4, 83–91 (2010)
15. Khan, S.A., Chang, C.M., Zaidi, Z., Shin, W., Shi, Y., Bowden, A.K.E., Solgaard, O.: Metal-insulator-metal waveguides for particle trapping and separation. Lab Chip 16(12), 2302–2306 (2016)
16. Armacost, M., Augstinz, A., Felsner, P., Feng, Y., Friese, G., Heidenreich, J., Hueckel, G., Prigge, O., Stein, K.: A high reliability metal insulator metal capacitor for 0.18 μm copper technology. In: International Electronic Devices Meeting (IEDM) Technical Digest, IEEE Conference, CA, USA, pp. 157–160 (2000). https://doi.org/10.1109/IEDM.2000.942822
17. Feng, N., Brongersma, M.L., Negro, L.D.: Metal—dielectric slot-waveguide structures for the propagation of surface plasmon polaritons at 1.55 μm. IEEE J. Quant. Electron. 43(6), 479–485 (2007)
18. Singh, A., Pal, A., Singh, Y., Sharma, S.: Design of optimized all-optical NAND gate using metal-insulator-metal waveguide. Optik 182, 524–528 (2019)
19. Zia, R., Schuller, J.A., Chandran, A., Brongersma, M.L.: Plasmonics: the next chip-scale technology. Mater. Today 9(7–8), 20–27 (2006)
20. Dionne, J.A., Sweatlock, L.A., Atwater, H.A., Polman, A.: Plasmon slot waveguides: towards chip-scale propagation with sub-wavelength-scale localization. Phys. Rev. B 73(3), 035407 (2006)
21. Pile, D.F., Ogawa, T., Gramotnev, D.K., Matsuzaki, Y., Vernon, K.C., Yamaguchi, K., Okamoto, T., Haraguchi, M., Fukui, M.: Two-dimensionally localized modes of a nanoscale gap plasmon waveguide. Appl. Phys. Lett. 87(26), 1–3 (2005)
22. Chen, Z., Holmgaard, T., Bozhevolnyi, S.I., Kravtin, A.V., Zayats, A.V., Markey, L., Deraux, A.: Wavelength-selective directional coupling with dielectric-loaded plasmonic waveguides. Opt. Lett. 34(3), 310–312 (2009)
23. Charbonneau, R., Lahoud, N., Mattiussi, G., Berini, P.: Demonstration of integrated optics elements based on long-ranging surface plasmon polaritons. Opt. Exp. 13(3), 977–984 (2005)
24. Jung, J.H.: Optimal design of dielectric-loaded surface plasmon polariton waveguide with genetic algorithm. J. Opt. Soc. Korea 14(3), 277–281 (2010)
25. Rao, D.G.S., Swarnakar, S., Palacharla, V., Raju, K.S.R., Kumar, S.: Design of all-optical AND, OR, and XOR logic gates using photonic crystals for switching applications. Photon. Netw. Commun. 41, 109–118 (2021)
26. Birr, T., Zywietz, U., Chhantyal, P., Chichkov, B.N., Reinhardt, C.: Ultrafast surface plasmon-polariton logic gates and half-adder. Opt. Exp. 23(25), 31755–31765 (2015)
27. Fakhruuldeen, H.F., Mansour, T.S.: All-optical NOT gate based on nanoring silver-air plasmonic waveguide. Int. J. Engg. Tech. 7(4), 2818–2821 (2018)
28. Gogoi, N., Sahu, P.P.: Design of all-optical inverter using nonlinear plasmonic two-mode waveguide. Adv. Res. Elect. Electron. Eng. 2(11), 35–38 (2015)
29. Nozhat, N., Alitokak, H., Khodadadi, M.: All-optical XOR and NAND logic gates based on plasmonic nanoparticles. Opt. Commun. 392, 208–213 (2017)
30. Gogoi, N., Sahu, P.P.: All-optical surface plasmonic universal logic gate devices. Plasmonics 11, 1537–1542 (2016)
31. Moradi, M., Danaie, M., Orouji, A.A.: Design of all-optical XOR and XNOR logic gates based on Fano resonance in plasmonic ring resonators. Opt. Quant. Electron. 51(5), 1–18 (2019)
32. Abdulnabi, S.H., Abbas, M.N.: All-optical logic gates based on nanoring insulator-metal–insulator plasmonic waveguides at optical communications band. J. Nanophoton. 13(1), 016009 (2019)
33. Swarnakar, S., Rathi, S., Kumar, S.: Design of all-optical xor gate based on photonic crystal ring resonator. J. Opt. Commun. 41(1), 1–6 (2017)
34. Swarnakar, S., Kumar, S., Sharma, S.: Performance analysis of all-optical full-adder based on two-dimensional photonic crystals. J. Comput. Electron. 17, 1124–1134 (2018)
35. Kumar, S., Singh, L., Swarnakar, S.: Design of one-bit magnitude comparator using nonlinear plasmonic waveguide. Plasmonics 12, 369–375 (2016)
36. Rao, D.G.S., Swarnakar, S., Kumar, S.: Performance analysis of all-optical NAND, NOR, and XNOR logic gates using photonic crystal waveguide for optical computing applications. Opt. Eng. 59(5), 1–11 (2020)
37. Rao, D.G.S., Palacharla, V., Swarnakar, S., Kumar, S.: Design of all-optical D flip-flop using photonic crystal waveguides for optical computing and networking. Appl. Opt. 59(23), 7139–7143 (2020)
38. Swarnakar, S., Kumar, S., Sharma, S., Singh, L.: Design of XOR / AND gate using 2-D photonic crystal principle. Proc. SPIE 10130, 1–11 (2017)
39. Rath, S., Swarnakar, S., Kumar, S.: Design of one-bit magnitude comparator using photonic crystals. J. Opt. Commun. 40(4), 1–5 (2017)
40. Swarnakar, S., Kumar, S., Sharma, S.: Design of all-optical half-subtractor circuit device using 2-D principle of photonic crystal waveguides. J. Opt. Commun. 40(3), 195–203 (2017)
41. Swarnakar, S., Kumar, S., Sharma, S.: All-optical half-adder circuit based on beam interference principle of photonic crystal. J. Opt. Commun. 39(1), 13–17 (2016)
42. Sharma, P., Kumar, V.D.: All optical logic gates using hybrid metal insulator metal plasmonic waveguide. IEEE Photon. Tech. Lett. 30, 959–962 (2018). https://doi.org/10.1109/LPT.2018.2826051
43. Taflove, A., Hagness, S.C.: Computational electrodynamics: the finite-difference time-domain method. Artech House, Boston, London (2000)
44. Pal, A., Ahmed, M.Z., Swarnakar, S.: An optimized design of all-optical OR, XOR, and NOT gates using plasmonic waveguide. Opt. Quant. Electron. 53(84), 1–13 (2021)
45. Al-Musawi, H.K., Ali, K., Janabi, A., Al-abassi, S.A.W., Abusiba, N.A.H., Al-Fatlawi, N.A.H.Q.: Plasmonic logic gates based on dielectric-metal-dielectric design with two optical communication bands. Optics 223, 1–14 (2020)

46. Kumar, S., Raghuwanshi, S.K.: Design of optical reversible logic gates using electro-optic effect of lithium niobate-based Mach-Zehnder interferometers. Appl. Opt. 55(21), 5693–5701 (2016). https://doi.org/10.1364/ao.55.005693

47. Singh, P., Tripathi, D.K., Jaiswal, S., Dixit, H.K.: Design and analysis of all-optical AND, XOR and OR gates based on SOA–MZI configuration. Opt. Laser Tech. 66, 35–44 (2015). https://doi.org/10.1016/j.optlastec.2014.08.002

48. Sharaiha, A., Topomondzo, J., Morel, P.: All-optical logic AND–NOR gate with three inputs based on cross-gain modulation in a semiconductor optical amplifier. Opt. Commun. 265(1), 322–325 (2006). https://doi.org/10.1016/j.optcom.2006.03.036

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.