Limitations of the intrinsic cut-off frequency to correctly quantify the speed of nanoscale transistors

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Abstract—The definition of the intrinsic cut-off frequency \( f_T \) based on the current gain equals to one (0 dB) is critically analyzed. A condition for the validity of the quasi-static estimation of \( f_T \) is established in terms of the temporal variations of the electric charge and electric flux on the drain, source and gate terminals. Due to the displacement current, an electron traversing the channel length generates a current pulse of finite temporal width. For electronic devices where the intrinsic delay time of the current after a transient perturbation is comparable to such width, the displacement currents cannot be neglected and the quasi-static approximation becomes inaccurate. We provide numerical results for some ballistic transistors where the estimation of \( f_T \) under the quasi-static approximation can be one order of magnitude larger than predictions obtained from a time-dependent numerical simulations of the intrinsic delay time (including particle and displacement currents). In other ballistic transistors, we show that the gate current phasor can be smaller than the drain one at all frequencies, giving no finite value for \( f_T \).

Index Terms—Cut-off frequency, THz, displacement current, nano transistor, time-dependent simulation.

I. INTRODUCTION

The development of faster electron devices for digital and analog applications is a constant demand in the electronics industry [1], [2]. The scientific community tries to quantify how fast the field effect transistors (FETs) work through some figures of merit (FoMs). Unfortunately, there is no such a unique FoM that unequivocally quantifies the speed. Some definitions are linked to a particular circuit or application, others to the intrinsic device itself. Some FoMs are redefined to make them more easily accessible from simulations, or from measurements. Usually, the FoM in digital FET applications are related with times, while in analog ones are commonly described with frequencies.

In digital FET applications, for example, an important FoM is the intrinsic delay time \( \tau_d \). The idea of this FoM is to quantify the time needed for an output signal to respond to an input signal [3]. Many times, a simpler quasi-static definition of the intrinsic delay time, \( \tau_d^{QS} \approx C \cdot V_{gs}/I_{ds} \), is preferred because it is easily accessible from DC (time-independent) simulations [1]. Such expression can be interpreted as the time needed to charge the next gate capacitor \( C \) until the gate voltage \( V_{gs} \) associated to the ON state, with a constant drain-source current \( I_{ds} \). From an experimental point of view, however, a new definition of the intrinsic delay time from a ring oscillator of \( N \) (odd) CMOS inverters is used. By taking the inverse of the frequency at which the ring oscillator runs and dividing it by \( N \), such intrinsic delay time can be easily obtained [4].

In analog applications, the cut-off frequency \( f_T \) and the maximum oscillation frequency \( f_{\text{max}} \) are the main FoMs. The \( f_T \) is defined as the frequency at which the drain and gate currents become equal (that is a current gain of 0 dB) [5], [6]. Equivalently, the \( f_{\text{max}} \) is the frequency at which the power gain is 0 dB [1]. Both frequencies are easily accessible from the measurement of \( S \)-parameters and even their intrinsic values (when all parasitic elements of the circuit are eliminated using de-embedding techniques) are measurable. Needless to say, \( f_{\text{max}} \), based on Mason’s identities [7], becomes a more relevant FoM in high-frequency analog applications [2].

It is accepted that, although the intrinsic \( f_T \) is not the relevant FoM in high frequency analog applications, it is a meritorious FoM providing useful information on the speed of FETs. In order to provide an expression of the cut-off frequency accessible from DC (time-independent) simulations, the so-called quasi-static approximation \( f_{T}^{QS} \approx g_m/(2\pi C) \) is presented in the literature [8]–[12]. It is based on assuming that the drain current is only the DC component related to the (linear) transconductance \( g_m = dI_{ds}/dV_{gs} \approx I_{ds}/V_{gs} \), while the gate current is the displacement component proportional to the capacitor \( C \) and frequency. From the previous quasi-static definition of the intrinsic delay time \( \tau_d^{QS} \approx C \cdot V_{gs}/I_{ds} \) in digital applications, we easily arrive to the approximation \( f_{T}^{QS} \approx 1/(2\pi\tau_d^{QS}) \) [13], [14]. This last expression supposedly justifies why the cut-off frequency is a good FoM to quantify the intrinsic switching speed in digital applications. Alternatively, several non-quasi-static approximations are also proposed for more accurate predictions of \( f_T \) [6], [8], [15], [16].

In this paper, we discuss if \( f_T \) can be an appropriate FoM to quantify the intrinsic speed of these nanoscale FETs with dimensions of few nanometers for digital or analog TeraHertz (THz) applications. In such FETs, the electric field generated by an electron crossing the channel is not properly screened and it induces displacement current on the terminals. We will construct a condition for the validity of the quasi-static estimation of \( f_{T}^{QS} \) and prove that \( f_T \) can be a quite misleading estimator (with or without approximations) for the speed of ballistic FETs.

We summarize here four relevant time intervals that will be used along the paper. The intrinsic delay time \( \tau_d \) quantifies
the temporal difference between the time when a gate voltage perturbation starts and the time when the gate, drain and source currents reach steady-state values. The \( \tau_d^{QS} \) and \( \tau_d^{NQS} \) are the intrinsic delay time mentioned above under the quasi-static approximation and under the zero-order non- quasi-static approximation, respectively. Due to the displacement current, one electron traversing the channel length generates a current pulse \( I(t) \). The temporal width of such pulse is defined as \( \tau_p \). 

The value of \( \tau_p \) is influenced by the device geometry and the dielectric relaxation time needed for the background charge to neutralize (screen) the electric field generated by the single electron. In the text, we also define \( f_d^{d} \), \( f_d^{QS} \) and \( f_d^{NQS} \) as the cut-off frequencies associated to \( \tau_d^{d} \), \( \tau_d^{QS} \) and \( \tau_d^{NQS} \), respectively. Finally, \( f_T \) is the exact definition of the cut-off frequency from the current gain equals to one. We will see in this paper that \( f_T \) can differ from \( f_d^{d} \).

**II. FOURIER ANALYSIS OF \( f_T \)**

In this Section, a Fourier analysis of the definition of \( f_T \) from the current gain equals to one will be discussed, with special attention to the role played by the particle and displacement currents on it. This complete discussion is valid for any type of (ballistic or non-ballistic) FETs. We will also present the conditions of validity of the quasi-static approximation in terms of the temporal variations of the electric charge plus the electric flux on the drain, source and gate terminals.

**A. Preliminary Discussion**

We consider a dual-gate FET depicted in Fig. 1(a) with three terminals. The three relevant total (displacement plus particle) currents, named \( I_1(t) \), \( I_2(t) \) and \( I_3(t) \) are associated to the gate, drain and source terminals, respectively, as

\[
I_m(t) = \int_{S_m} \epsilon(\vec{r}) \frac{d\vec{E}(\vec{r}, t)}{dt} \cdot d\vec{s} + \int_{S_m} J(\vec{r}, t) \cdot d\vec{s},
\]

being \( \epsilon(\vec{r}) \) the electric permittivity, \( \vec{E}(\vec{r}, t) \) the electric field and \( J(\vec{r}, t) \) the particle current density. We consider \( d\vec{s} \) outward. The three surfaces in equation 1 construct a surface \( S = S_1 + S_2 + S_3 \) that totally enclose an arbitrary volume \( \Omega \). Then, by construction, at any time \( t \), the three currents satisfy

\[
I_1(t) + I_2(t) + I_3(t) = 0.  \tag{2}
\]

which is just the conservation of the total current in the active region \( \Omega \) due to the application of Gauss’s law in \( S \).

In the evaluation of \( f_T \), we are interested in a transient simulation. Initially, the three currents have steady-state values \( I_m(0) \). At \( t = 0 \), a (small-signal) voltage perturbation is applied on one of the three FET terminals. Then, during a time interval \( \tau_d \) (we will see later that this time is indeed the intrinsic delay time), the three output currents oscillate. Finally, new steady-state values \( I_m(\tau_d) \) for the three currents

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1In the case of an electron with charge \( q \) and velocity \( v \) moving between two infinite parallel metals separated with a distance \( L \), it is well known from the Ramo-Shockley-Pellegrini theorem \( \alpha \) that the square pulse current has a temporal width of \( \tau_p = L/v \) and a height equals to \( qvL \). The total charge of the current pulse is \( (qv/L) \times (L/v) = q \).

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**Fig. 1. (a) Cross-section of the active region \( \Omega = L \times (H' + H + H'') \times W \) in a dual-gate 2D FET being \( L \) the gate length. (b) A two-port network of the intrinsic device.**

are achieved with \( I_m(t) = I_m(\tau_d) \) for \( t \geq \tau_d \). For each contact \( m \), we define the incremental charge during \( \tau_d \) as

\[
\Delta Q_m \equiv \int_0^{\tau_d} (I_m(t) - I_m(\tau_d))dt.  \tag{3}
\]

Using 2 that ensures \( I_1(t) + I_2(t) + I_3(t) - I_1(\tau_d) - I_2(\tau_d) - I_3(\tau_d) = 0 \) at any time, we easily get

\[
\Delta Q_1 + \Delta Q_2 + \Delta Q_3 = 0.  \tag{4}
\]

This equation just states that the variation of electron charge from 0 till \( \tau_d \) in the volume \( \Omega \) is compensated by the variations of the electric flux during this time interval on the surface \( S \).

**B. The All-order Definition of \( f_T \)**

The usual definition of \( f_T \) comes from a FET in common source configuration as plotted in Fig. 1(b). Following the signs of the currents assigned to the FET of Fig. 1(a), the currents on the gate and drain terminals of the two-port network are positive when leaving the network. In the two-port network model of Fig. 1(b), the relationship between the phasor voltages \( \hat{V}_n(\omega) \equiv \mathcal{F}\{V_n(t) - V_m(0)\} \), the phasor currents \( \hat{I}_m(\omega) \equiv \mathcal{F}\{I_m(t) - I_m(0)\} \) and the \( Y \)-parameter matrix is

\[
\begin{bmatrix}
\hat{I}_1(\omega) \\
\hat{I}_2(\omega) \\
\hat{I}_3(\omega)
\end{bmatrix} = \begin{bmatrix}
Y_{11}(\omega) & Y_{12}(\omega) & Y_{13}(\omega) \\
Y_{21}(\omega) & Y_{22}(\omega) & Y_{23}(\omega) \\
Y_{31}(\omega) & Y_{32}(\omega) & Y_{33}(\omega)
\end{bmatrix} \begin{bmatrix}
\hat{V}_1(\omega) \\
\hat{V}_2(\omega) \\
\hat{V}_3(\omega)
\end{bmatrix},  \tag{5}
\]

where \( \omega \) is the angular frequency and \( \mathcal{F}\{\cdot\} \) is the Fourier transform. The frequency-dependent component \( Y_{mn}(\omega) \) of the admittance matrix, due to a small signal current \( I_m(t) - I_m(0) \) collected on contact \( m \) when a step perturbation \( V_n(t) = V_n(0) + \Delta V_n \cdot u(t) \) (with \( u \) the Heaviside step function) is applied on contact \( n \) and zero volts in the rest of terminals, is given by \[5, 18\]

\[
Y_{mn}(\omega) \equiv \Delta I_m \frac{j\omega}{\Delta V_n} + \frac{j\omega}{\Delta V_n} \int_0^{\tau_d} (I_m(t) - I_m(\tau_d))e^{-j\omega t}dt,  \tag{6}
\]

where \( \Delta I_m = I_m(\tau_d) - I_m(0) \). In expression (6), we have considered \( I_m(t) = I_m(\tau_d) \) for \( t \geq \tau_d \).

The intrinsic cut-off frequency \( f_T \) computed from the \( Y \)-parameter is the linear frequency at which the current gain magnitude drops to unity (0 dB) \[5\]

\[
|h_{21}(\omega = 2\pi f_T)| \equiv \left| \frac{Y_{21}^{All}}{Y_{11}^{All}} \right| = \left| \frac{\mathcal{F}\{I_2(t) - I_2(0)\}}{\mathcal{F}\{I_1(t) - I_1(0)\}} \right| = 1.  \tag{7}
\]

The superindex \( All \) means that all orders of the Taylor expansions of the Fourier transform in (6) are taken into account (without approximations).
C. The Quasi-static Definition of $f_T^{QS}$

The expression of $f_T^{QS}$ within the quasi-static approximation is obtained by computing the term $Y_{21}$ from (6) without any frequency dependence, $e^{-j\omega t} \approx 0$, as

$$Y_{21}^{QS}(\omega) \approx \frac{\Delta I_2}{\Delta V_1} \equiv \frac{dI_2}{dV_1} \equiv g_m.$$  \hspace{1cm} (8)

The term $Y_{11}$ is computed with a zero-order approximation, $e^{-j\omega t} \approx 1$, from (6) as

$$Y_{11}^{QS}(\omega) \approx \frac{j\omega}{\Delta V_1} \int_0^{\tau_2} (I_1(t) - I_1(\tau_d)) dt = j\omega \frac{\Delta Q_1}{\Delta V_1},$$  \hspace{1cm} (9)

where $\Delta Q_1$ is defined in (3). The approximation in (9) is based on the assumption that the current pulse $\tau_p$ is short enough to neglect any displacement component of the drain current. Expression (9) assumes that the gate current is the displacement component. As indicated in the Introduction, from [7], using (3) and (5), we get

$$f_T^{QS} = \frac{g_m}{2\pi \Delta Q_1 / \Delta V_1} = \frac{g_m}{2\pi C_1},$$  \hspace{1cm} (10)

where the term $\Delta Q_1/\Delta V_1 \equiv C_1$ is usually associated to the gate capacitor [19]. If we assume that $\Delta Q_1 \approx \Delta Q_2$, during the transient evolution

$$\Delta Q_1 \approx \Delta Q_2 \equiv \int_0^{\tau_2} (I_2(t) - I_2(\tau_d)) dt \approx \Delta I_2^{QS},$$  \hspace{1cm} (11)

we get the condition $C_1 \Delta V_1 = \Delta Q_1 \approx \Delta Q_2 \approx \Delta I_2^{QS}$, where $\tau_2^{QS} \approx C_1 \Delta V_1 / \Delta I_2$ is the typical quasi-static definition of the intrinsic delay time mentioned in the Introduction when $\Delta V_1 \approx V_{gs}$ giving $\Delta I_2 \approx I_{ds}$. Then, the definition of the (small-signal) transconductance in equation (8), with expression (11), can be redefined as (13)

$$g_m \equiv \frac{dI_2}{dV_1} \approx \frac{\Delta I_2}{\Delta V_1} \equiv \frac{\Delta I_2}{\Delta Q_1} \frac{\Delta Q_1}{\Delta V_1} = \frac{1}{\tau_2^{QS}} C_1.$$  \hspace{1cm} (12)

Putting (12) into (10), one arrives to the final result

$$f_T^{QS} = 1/(2\pi \tau_2^{QS}),$$  \hspace{1cm} (13)

which is one of the main reasons why $f_T^{QS}$ is interpreted as a relevant FoM on how fast a digital FET works. In summary, the quasi-static approximation is valid whenever the condition $\Delta Q_1 \approx \Delta Q_2$ is satisfied. From (11), such condition can be equivalently written as $\Delta Q_3 \approx 0$. From (3), the previous conditions in a transient evolution means that the source current rapidly becomes equivalent to its high value $I_3(t) \approx I_3(\tau_d)$ while the drain current remains low $I_2(t) \approx I_2(0)$ during the intrinsic delay time interval $0 < t < \tau_d$. These conditions are typical in many FETs with a large channel length $L$ where the intrinsic delay time $\tau_d$ is much larger than the temporal width of the current pulse generated by one electron $\tau_p$, i.e. $\tau_d \gg \tau_p$. Then, the total (particle and displacement) current in the drain and source contacts are detected only when electrons cross the surfaces $S_2$ and $S_3$, respectively. However, in FET devices with a short channel length $L$, one can easily get scenarios with $\tau_d \approx \tau_p$ where an electron moving along the channel generates a time-dependent electric field that is detected as displacement current on the source and drain contacts without even crossing the surfaces $S_2$ (drain contact) and $S_3$ (source contact).

D. The Zero-order Non-quasi-static Definition of $f_T^{NQS}$

In order to better include the drain displacement current, it seems more appropriate to use the same zero-order approximation of the exponential term, $e^{-j\omega t} \approx 1$, that we have used for $Y_{11}$ in (9), in the computation of $Y_{21}$ from (6)

$$Y_{21}^{NQS}(\omega) \approx g_m + j\omega \int_0^{\tau_2} (I_2(t) - I_2(\tau_d)) dt \approx g_m - j\omega |\Delta Q_2| / \Delta V_1,$$  \hspace{1cm} (14)

where $\Delta Q_2$ is also defined in (3). Consequently, from (7), a non-quasi-static estimation ($NQS$) of $f_T$ gives (20)

$$f_T^{NQS} = \frac{g_m}{2\pi \sqrt{|\Delta Q_1^2 - \Delta Q_2^2| / \Delta V_1}}.$$  \hspace{1cm} (15)

This is a first step (zero-order Taylor approximation) in the evaluation of $f_T^{NQS}$ beyond the quasi-static approximation. In a typical n-type FET, when $\Delta V_1$ is positive, we can expect a positive transient current $I_2(t)$ satisfying $I_2(0) \leq I_2(t) \leq I_2(\tau_d)$, while the current on the source is negative and decreases $I_3(t) \geq I_3(\tau_d)$ because of the signs selected in Fig 1(b). Since we deal with an increment of electrons (negative charge) in the channel, we expect $I_1(t) \geq 0$ in the metal. From (3) we get positive $\Delta Q_1$ and $\Delta Q_2$, while negative $\Delta Q_2$. Therefore, the expression $\Delta Q_1 + \Delta Q_3 = |\Delta Q_2|$ is achieved, which means $|\Delta Q_1| < |\Delta Q_2|$. This condition will be numerically tested later. Therefore, the definition of $f_T^{NQS}$ in (15) can be ill-defined because it deals with a square root of a negative number, that is, the condition $|h_{21}| = 1$ cannot be reached with this zero-order non-quasi-static approximation.

We arrive now to a relevant question about the adequacy of $f_T$ as a proper FoM for testing FET speed. Is it possible to find FETs where the gate phasor current is always smaller than the drain one, even with the exact definition of the $Y$ parameters in (2)? This would imply that, contrarily to what is assumed in the original definition of $f_T$, the current gain never drops to 0 dB at any frequency.

III. NUMERICAL SIMULATION

The conditions of validity of $f_T^{QS}$ were discussed in Section II-C. In Section II-D we pointed out the possibility that the own definition of $f_T$ is ill-defined because there is no guarantee that the gate phasor current becomes higher than the drain phasor current as frequency grows. Next, we provide numerical confirmation of these drawbacks for ballistic nanoscale FETs.

A. Device Structure and Time-dependent Simulations

We will consider dual-gate FETs schematically drawn in Fig.1(a) with a 2D channel material. These 2D materials are expected to improve electron mobility and to suppress the short channel effect for ultra-scaled devices. In order to simplify the numerical simulations (avoiding extra complications, like Klein tunneling or hole transport, that will obscure the interpretations of our numerical results), we will consider only electron transport in the conduction band of a n-type graphene-like material with a linear energy band $E_k = \pm h v_f |k|$ being $v_f = 5 \times 10^3$ m/s the Fermi velocity and $k$ the wave vector.
which contains the two degrees of freedom \( \{ k_x, k_z \} \). The permittivity is \( \epsilon = 4\epsilon_0 \) in the 2D material and \( \epsilon = 3.9\epsilon_0 \) in dielectrics with \( \epsilon_0 \) is the vacuum permittivity. Electron transport will be assumed ballistic (without phonon or impurity scattering) and only the electron-electron interaction through the Poisson equation will be considered. The simulation box will not include the 3D-2D contact resistances and other parasitic elements (which are the well-known frequency bottleneck \([1]\)). Thus, we only simulate the intrinsic performance of FETs.

We will consider FET devices with a width of the current pulse associated to one electron comparable to the intrinsic delay time along the channel, i.e. \( \tau_p \approx \tau_d \). These conditions just mean that the channel is short enough and the dielectric relaxation time large enough so that the displacement current of an electron crossing the channel has to be considered in each terminal even when the electron is in the middle of the channel. The extension \( L' \) depicted in Fig. 1(a) is present to ensure the proper computation of such displacement current, even when the electrons are outside of the volume \( \Omega \). The time-dependent total currents in eq. \( \text{(1)} \) are computed with the BITLLES simulator \([21]\) from self-consistent Monte Carlo solutions of the Boltzmann and Poisson equations. The temporal step of the simulations is \( \Delta t = 7 \times 10^{-16} \) s. Finally, we notice that all the transient simulations have been repeated many times and the results properly averaged in order to minimize the presence of physical noise \([22]\) (random fluctuations) in the current values. The reasons are to avoid extra non-pertinent complexities in the discussions of the results and to approach experimental \( S \)-parameters setups which provide measurements through several periods of the oscillating signals.

### B. Example 1: Device A

We consider device A with a volume \( \Omega_A = 100 \times (45+1+45) \times 1125 \) nm\(^3 \) in Fig. 1(a) with the 2D material thickness \( H = 1 \) nm and the gate length \( L = 100 \) nm. In the simulation box, we set spatial steps \( \Delta x = 10 \) nm, \( \Delta y = 11.25 \) nm and \( \Delta z = 225 \) nm resulting \( 22 \times 11 \times 7 \) cells. The DC characteristic plotted in Fig. 2 is computed by time-averaging the total drain current in \( \text{(1)} \) and by summing the net number of electrons transmitted through the drain surface. Both DC values coincide because the time-averaged displacement current is zero. Such double computation of the drain DC value certifies the correct simulation of the displacement current.

**Fig. 2.** The output characteristic of device A for different \( V_1 \).

The transient currents in response to two square voltage pulses on the gate contact are indicated in Fig. 3. As illustrated in Fig. 1(b), since we deal with a small-signal formalism, the evaluation of \( Y_{21} \) and \( Y_{11} \) is done with a DC bias, \( V_2 = 0.1 \) V, applied between drain and source contacts, and a DC voltage \( V_1 = -0.05 \) V plus the transient perturbation \( \Delta V_1 = 0.1 \) V on the gate. In Fig. 3 the solid lines are \( |Y_{21}^{\text{All}}| \) and \( |Y_{11}^{\text{All}}| \) computed exactly from \( \text{(6)} \) as a function of frequency. For frequencies higher enough, the absolute value of \( Y_{21}^{\text{All}} \) shows strong frequency dependency and the \( |Y_{11}^{\text{All}}| \) is no longer linearly increasing with the frequency, which is qualitatively identical to the experimental observations \([19]\). The values of \( |Y_{21}^{\text{All}}| \) and \( |Y_{11}^{\text{All}}| \) become equal at \( f_T = 1.31 \) THz.

Using the quasi-static approximation in expression \( \text{(10)} \), we get \( f_T^{\text{QS}} = 1.45 \) THz, which is similar to the previous value \( f_T = 1.31 \) THz. In the non-quasi-static approximation, the formula \( \text{(15)} \) requires the restriction \( |\Delta Q_1| > |\Delta Q_2| \). As illustrated in Fig. 4 (red dashed area), \( \Delta Q_1 = 11.62 \times 10^{-19} \) C,
\[ \Delta Q_2 = -26.53 \times 10^{-19} \text{C and } \Delta Q_3 = 14.91 \times 10^{-19} \text{C.} \] The result \( \Delta Q_1 < |\Delta Q_2| \) is coincident with what we anticipated in Section II-D. Since \( \Delta Q_1 \approx \Delta Q_2 \), there is no solution to the \( f_T \) in non-quasi-static case. This result can also be understood from (14) indicating that \( \Delta Q_2 \) controls the frequency slope of \( Y_{11}^{QS} \) at high enough frequencies. Similarly, from (9), the slope of \( Y_{11}^{QS} \) is controlled by the \( \Delta Q_1 \). Since \( \Delta Q_1 < |\Delta Q_2| \), the terms \( Y_{21}^{NQS} \) and \( Y_{11}^{QS} \) never cross as can be seen in Fig. 4. Surprisingly, the (zero-order) non-quasi-static model is even worse than the simpler quasi-static one.

The errors when neglecting the displacement current in the computation of \( f_T^{QS} \) can be quantified from expression (14). The elimination of the drain displacement current can be justified for those frequencies satisfying that \( g_m \) is larger or equal than the \( \omega/|\Delta Q_2|/|\Delta V_1| \). By imposing the previous condition, \( g_m \approx 2 \pi f_c |\Delta Q_2|/|\Delta V_1| \), we get a definition of the maximum frequency \( f_c \) where the drain displacement current can be reasonably neglected.

\[
f_c = \frac{g_m}{2 \pi |\Delta Q_2|/|\Delta V_1|}.
\]

However, since we have demonstrated in equation (14) that \( |\Delta Q_2| > \Delta Q_1 \), we always get \( f_c < f_T^{QS} \) which can be seen in Fig. 4 where solid lines (All) start to deviate from dashed lines (QS) at \( f_c = 0.82 \text{THz} < f_T^{QS} = 1.45 \text{THz} \). Notice that the condition \( \Delta Q_1 \approx \Delta Q_2 \) in (16) implies that \( f_c \approx f_T^{QS} \) justifying the arguments on the range of validity of \( f_T^{QS} \) mentioned in Section II-C.

C. Example 2: Device B

The quasi-static approximation seems to imply that a desired condition for a fast FET is \( \Delta Q_1 \to 0 \) \((C_1 \to 0)\) if short channel effects are still under control. Such condition would imply that \( f_T^{QS} = g_m/(2 \pi \Delta Q_1/\Delta V_1) = g_m/(2 \pi C_1) \to \infty \) in equation (10) and \( \tau_T^{QS} \approx C_1 \Delta V_1/\Delta I_2 \approx \Delta Q_1/\Delta I_2 \to 0 \). We consider a new design (device B) with the goal of getting \( C_1 \to 0 \). In particular we consider the same FET of Fig. 1(a) with the geometry \( \Omega_R = 20 \times (45 + 1 + 45) \times 700 \text{nm}^3 \) (gate length \( L = 20 \text{nm} \)) under the same type of simulation as in device A. In the simulation box, we set spatial steps \( \Delta x = 2 \text{nm}, \Delta y = 11.25 \text{nm} \) and \( \Delta z = 140 \text{nm} \) resulting 22 \times 11 \times 7 cells. We plot the DC current-voltage characteristic of device B in Fig. 5. In spite of the small capacitance, the short channel effects are reasonably under control. We use \( V_2 = 0.1 \text{V} \), applied between drain and source contacts, and \( V_1 = -0.1 \text{V} \) plus the transient perturbation \( \Delta V_1 = 0.15 \text{V} \) on the gate. The total transient currents on the drain, gate and source contacts of device B due to a step voltage perturbation in the gate are plotted in Fig. 6 where the sum of the total currents also maintains consistency with the continuity equation (2). Moreover, the incremental charge \( \Delta Q_1 = 1.54 \times 10^{-19} \text{C}, \Delta Q_2 = -6.76 \times 10^{-19} \text{C} \) and \( \Delta Q_3 = 5.24 \times 10^{-19} \text{C}. \)

The \( Y \) parameters changing with frequency in all orders (solid lines), NQS and QS models (dashed lines) for device B are plotted in Fig. 7. In the quasi-static estimation, because the \( |\Delta Q_1| \) in device B becomes smaller than that of device A, the \( Y_{11}^{QS} \) is shifted towards the horizontal axis, therefore, the quasi-static value of the cut-off frequency increases giving \( f_T^{QS} = 10.64 \text{THz} \). The behaviors of NQS for device B and device A are similar. In the all-orders model, the condition \( |h_{21}| = 1 \) is satisfied at \( f_T = 4.97 \text{THz} \). The oscillations of \( Y_{11}^{All} \) and \( Y_{21}^{All} \) at higher frequencies are the Fourier transform of time-dependent variations of the total currents in Fig. 6 which can be associated to plasmonic oscillations with shorter
The DC current is plotted in Fig. 8, which indicates the ability of the gate to control the channel. In the transient current periods than the value of \( \tau_d \) plotted there. So the exact value of the \( f_T \) is randomly influenced by such oscillations. We have assumed an ideal metallic contact (dielectric relaxation time equals to zero) in all simulations. One can expect significantly different randomness in the oscillations of the \( Y \) parameters at high frequency for heavily doped contacts [23]. The problem present in device B is that the real frequency where the device switches will be needed, in principle. However, the present simulations are enough to compare the different FET speed estimators. The relation between the input and output signals in Figs. 3, 6 and 9 can be modeled from linear system theory. It is clear that the relevant frequencies are inversely proportional to the time interval \( \tau_d \). A reasonable expression could be \( f_d^T \approx 1/(2\tau_d) \) 24 25.

In device A, from Fig. 3 we get a value of the intrinsic delay time \( \tau_d = 0.352 \) ps, resulting \( f_d^T = 1.42 \) THz, which is similar to the quasi-static cut-off frequencies \( f_T^{QS} = 1.45 \) THz. However, in device B, from Fig. 6 we get a simulated \( \tau_d = 0.185 \) ps giving \( f_d^T = 2.70 \) THz, which is much smaller than the value \( f_T^{QS} = 10.64 \) THz. In device C, the result is even worse where the intrinsic delay time is \( \tau_d = 0.138 \) ps providing \( f_d^T = 3.62 \) THz. The reason why the quasi-static expression \( 10 \) does not capture the real intrinsic delay time in devices B and C is because the approximation \( \Delta Q_2 \approx \Delta Q_1 \) is no longer true. In fact, since we looked for \( \Delta Q_1 \rightarrow 0 \), the result \( \Delta Q_2 \gg \Delta Q_1 \) gives \( f_T^{QS} \) in \( 10 \) much larger than \( f_c \) in \( 16 \). Let us notice that the quasi-static estimation of the intrinsic delay time is again clearly misleading. In device B, we get \( \tau_d^{QS} \approx C_1 \Delta V_1 / \Delta f \approx 0.015 \) ps, which is more than one order of magnitude smaller than our simulated value \( \tau_d = 0.185 \) ps (the ratio \( \tau_d / \tau_d^{QS} \) is different from \( f_d^T / f_T^{QS} \).
because of the factor $\pi$ in $[13]$. In device C, the $\tau_{d}^{QS} \approx 0.012$ ps is also more than one order of magnitude shorter than the simulated value $\tau_{d} = 0.138$ ps. The reason of this discrepancy is also the condition $\Delta Q_{2} \gg \Delta Q_{1}$, which invalidates the quasi-static estimation discussed in Section II-C.

IV. FINAL DISCUSSION AND CONCLUSIONS

In conclusion, we have established the condition for the validity of the quasi-static approximation of $f_{T}^{QS}$ in terms of the electrical current and electrical flux on the gate, drain, and source FET terminals defined in expressions (1) and (3). Such approximation is applicable when $\Delta Q_{1} \approx \Delta Q_{2}$ which means that we are dealing with FETs where the intrinsic delay time is much larger than the temporal width of the current pulse generated by one electron, i.e. $\tau_{d} > \tau_{p}$ (with large channel length $L$ as in device A). On the contrary, in devices where $\tau_{d} \approx \tau_{p}$ (i.e. as in devices B and C with short channel length $L$), the quasi-static approximation is not applicable because the electric field generated by electrons are not screened inside the device active region, and its associated displacement current becomes relevant during all the time while the electron is traversing the channel. We have shown through analytical arguments supported by numerical simulations that the estimations of the intrinsic cut-off frequency based on $|b_{21}| = 1$ (with the quasi-static $f_{T}^{QS}$, zero-order non-quasi-static $f_{T}^{NQS}$ or without approximations $f_{T}$) can provide misleading results for the speed of FETs. This problem is specially severe for nanoscale FETs which are routinely modeled from quantum transport simulators. The explicit quantum simulation of the time-dependent displacement current and $\tau_{d}$ demand such huge amount of computational resources $[17, 23, 26]$ that the intrinsic FoM of the speed of such ballistic FET are routinely taken from quasi-static estimations. As shown in some examples in this work, such type of quasi-static estimations can erroneously predict the FET speed by one order of magnitude. Other examples show no finite value of $f_{T}$ underlying an important limitation of the traditional definition of $f_{T}$ to properly quantify the speed of FETs. However, when parasitic elements are included in the simulation, one can expect a tendency to recover the validity of the quasi-static approximation ($\tau_{d}$ grows and $\tau_{p}$ remains the same) at the price of getting lower FET speed than its intrinsic value.

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