Farview: Disaggregated Memory with Operator Off-loading for Database Engines

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\textbf{ABSTRACT}

Cloud deployments disaggregate storage from compute, providing more flexibility to both the storage and compute layers. In this paper, we explore disaggregation by taking it one step further and applying it to memory (DRAM). Disaggregated memory uses network attached DRAM as a way to decouple memory from CPU. In the context of databases, such a design offers significant advantages in terms of making a larger memory capacity available as a central pool to a collection of smaller processing nodes. To explore these possibilities, we have implemented Farview, a disaggregated memory solution for databases, operating as a remote buffer cache with operator offloading capabilities. Farview is implemented as an FPGA-based smart NIC making DRAM available as a disaggregated, network attached memory module capable of performing data processing at line rate over data streams to/from disaggregated memory. Farview supports query offloading using operators such as selection, projection, aggregation, regular expression matching and encryption.

In this paper we focus on analytical queries and demonstrate the viability of the idea through an extensive experimental evaluation of Farview under different workloads. Farview is competitive with a local buffer cache solution for all the workloads and outperforms it in a number of cases, proving that a smart disaggregated memory can be a viable alternative for databases deployed in cloud environments.

\section{INTRODUCTION}

Historically, databases have invested significant efforts to reduce I/O overheads. Initially, memory was very limited in capacity and disks were slow. Over time the bottleneck shifted as faster storage became available (SSDs, Non-Volatile Memory (NVM)), memories became larger, and multicore emerged. Yet, the I/O overhead remains a major factor in the overall performance. To minimize it, databases have relied on keeping more and more data in memory, a trend that cannot continue for two main reasons: databases induce considerable data movement, which is known to be highly inefficient in modern computing; and the amount of data to be processed keeps growing while DRAM capacity does not.

Optimized query plans typically push down selection and projection operators to filter out the base tables as early as possible. However, filtering base tables to get the data actually needed by the query is an expensive step. Base tables are fetched from storage as blocks that are placed in a buffer cache in memory. From there, a query thread reads the data and filters it to form the input to the rest of the query plan. Often, most of the data is dropped because it does not match the query’s selection predicate. As more data is involved, the overhead becomes larger. Data movement has been identified as one of the biggest inefficiencies in computing [30, 31], making the way databases operate intrinsically problematic from a systems perspective, even if main memory could grow indefinitely.

However, DRAM capacity is also a major limitation, because the size of data processed by analytical databases keeps growing [49]. The current approach to tackle such a limitation is to use NVM, introduced as an alternative that is both cheaper and has higher capacity than DRAM (and persists data), but has larger latency. In databases, it is increasingly used to improve and expand the memory hierarchy [18–20, 58, 70, 71]. Such designs do not address the overhead of moving large data sets to the CPU, only to have most of it filtered or projected out. Specialized hardware between memory and the CPU has even been proposed to filter data as early as possible, minimizing bus congestion and cache pollution [12, 35].

An alternative approach for addressing memory pressure is to exploit the distributed nature of database engines, particularly in the cloud, to take advantage of non-local memory. In such distributed settings, the coupling of storage, compute, and memory capacity is problematic both cost-wise and performance-wise: the inability to independently provision each of those elements leads to inefficiencies due to over-provisioning. For instance, allocating large amounts of memory for tasks that are not compute-heavy leaves CPU unused, as other applications might not be able to run on the remaining memory. Conversely, allocating many virtual CPUs to a task may result in the memory being underutilized for lack of compute capacity for other tasks. Due to these challenges, essentially all cloud architectures follow a clear trend towards disaggregation. Currently, the most visible form of disaggregation is the separation of compute and storage. The next step is the disaggregation of memory and compute, which is being pursued in various forms: disaggregated DRAM [39, 50, 51], disaggregated persistent memory [54, 69], far memory [11, 15] and smart remote memory [47, 68].

In this paper we demonstrate that databases are uniquely positioned to exploit disaggregated memory to address both the issues of inefficient data movement and DRAM capacity. Our approach is based on physically detaching query processing from memory buffer management. The buffer pool is placed on network attached disaggregated memory, with query processing nodes provisioned on demand to run a query by reading the data from the network attached buffer pool. This design presents multiple advantages. Consider, for example, queries with high selectivity (e.g., TPC-H Q6) or an aggregation after a \texttt{GROUP BY} statement. In the first case, the query reads a large amount of data from the buffer pool just to discard most of it. In the second case, a query of the form \texttt{SELECT T.a, COUNT(*) FROM T GROUP BY T.a} will usually return only a handful of tuples, but it still requires reading the entire table. The smart disaggregated memory we propose offers the opportunity to
2 BACKGROUND AND RELATED WORK

In this section, we motivate Farview and discuss related work. Farview is based on extensive experience in data center, computer, and processor design [27, 36]. For reasons of space, we focus here only on two salient aspects: memory disaggregation and near-data processing.

2.1 Coping with memory pressure

Data growth has turned DRAM into a major bottleneck [34, 49]. To cope with this bottleneck, advances in memory technologies and networking are leveraged to increase effective DRAM capacity. Within a local node, studies have explored compressing cold pages into local DRAM [49] or using local NVM directly as memory or with DRAM acting as a transparent caching layer [33, 60, 63]. These designs have also been used in databases in different ways, to expand virtual memory [58], directly as memory [18], or as a cache [70]. While in many cases there are performance advantages, these efforts require significant redesign in the database engine and do not address the underlying problem of inefficient data movement.

In a distributed setting, the notion that memory can be shared across a cluster of machines has been around for decades [16]. More recently, the advent of Fast networks like InfiniBand FDR/EDR has renewed interest in exploiting memory (DRAM or NVM) accessed over the network. Remote memory, a distributed memory infrastructure where a group of comparably equipped compute nodes make their memory available to their peers, has been exposed to applications as a remote paging device [15, 41], as a file system [9], and as distributed shared memory [32, 55, 67]. Although this organization leverages existing resources and can improve resource utilization of otherwise unused memory, it entangles compute and memory for provisioning and expands the failure domain and attack surfaces of each machine [10, 49].

In contrast, disaggregated memory systems use network attached memory that is distinct from the memory in the compute nodes [51, 69]. This approach allows the disaggregated memory to scale independently of the system’s computing or storage capacity [50], and removes the need to over-provision one resource to scale another. From the database perspective, this is a promising architecture. An evaluation of existing database engines (MonetDB and PostgreSQL) using LegOS [66], an operating system for disaggregated memory, indicates that the network overhead is the main bottleneck [74, 75]. The authors conclude that disaggregated memory has potential but significant performance loss occurs due to the use of sub-optimal algorithms and lack of suitable data structures.

In Farview, we demonstrate that disaggregated memory is especially suitable to database engines when used as a buffer pool (also suggested in [74]). This makes the integration of disaggregated memory a more natural way to addresses the memory capacity limitation as neither the interface to memory needs to be changed nor the memory hierarchy expanded. What remains to be addressed is the data movement inefficiencies and network overhead.

1) reduce data movement by pushing down operators to the disaggregated memory, so that the processing nodes receive only the relevant data; and (2) reduce memory requirements for computing nodes by centralizing the buffer cache in disaggregated memory. Figure 1 shows an example where projection and selection of two concurrent queries are offloaded to smart disaggregated memory, while the join and the final projection take place at the compute nodes.

To prove that these ideas can work in practice, we have developed Farview (FV), a novel platform for data processing over disaggregated memory. Farview supports near-data processing to compensate for the added latency of accessing memory through the network by moving data reduction operators (selection, projection, aggregation, etc.) to the disaggregated memory. Farview is based on a smart NIC built on top of an open source FPGA shell [48] that enables the FPGA to support dynamic operator push down on concurrent streams reading from memory. The smart NIC supports RoCE v2 at 100 Gbps using an open source RDMA stack [68], optimizing the interaction between network and memory as well as minimizing the network processing overheads on the computing node CPU, thereby freeing processing capacity. From a database perspective, Farview acts as a disaggregated memory buffer pool that is byte addressable by the threads running queries at the computing nodes.

For reasons of space, in this paper we focus on the design, architecture, and experimental evaluation of Farview when running queries, leaving other aspects such as cache replacement policies and query processing elasticity to future work. Farview currently supports a wide range of query operators: selection, projection, aggregation, distinct, group by, regular expression matching, and encryption. All these operators achieve near line-rate speed, adding insignificant latency to baseline network overheads. Farview also supports concurrent access, with multiple clients all accessing the same shared disaggregated memory. Our experiments show that Farview induces almost no overhead over operating on local memory and provides significant performance gains when data can be reduced in the disaggregated memory.

Figure 1: Farview query execution: Offloading of query operators to the smart disaggregated memory and splitting the query plan between compute and memory nodes.

SELECT T.a, S.b
FROM T, S
WHERE T.id = S.id
AND T.c > 50 AND S.d <= 2012;

SELECT R.d, S.b
FROM R, S
WHERE R.id = S.id
AND R.a = 3.14 AND S.a <> 2012;

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AND R.a = 3.14 AND S.a <> 2012;
2.2 Efficient data movement

Data movement inefficiencies can be addressed by using near-data processing. Expanding on decades-old work that memory and storage can be active components [45, 59, 61, 62], several approaches to memory disaggregation explore increasing the intelligence of network-attached memory. Far memory [11] proposes simple hardware extensions to reduce the number of network traversals to access non-local memory, and support for efficient notifications to facilitate consistency of data cached in the local memory of the nodes. In the context of databases, the advantages of processing data in the disaggregated memory have also been suggested [74, 75], but without proposing a possible implementation. The argument in favor of such designs is simple: push down selection and projection operators (as well as potentially other operators such as grouping, aggregation or even joins where one of the tables is small) to the memory or storage so that the base table is filtered out in-situ and irrelevant data does not need to be moved or sent. Although, to our knowledge not yet used with disaggregated memory, the idea mirrors a growing trend to push SQL operators near the data, until now mostly to storage [43, 72]. Even more ambitious are accelerators embedded in the data path between memory and CPU caches [29, 35], which can filter data as it is read from memory to reduce data movement and cache pollution. Finally, in the cloud, systems like Amazon’s AQUA [21] use SSDs attached to FPGAs to implement a caching layer for RedShift that supports SQL filtering operations and operator push-down to minimize the amount of data movement from storage to the processing nodes. These designs are based on introducing a bump-in-the-wire processor to be able to process data closer to where it initially resides, instead of moving it first and then processing it. In Farview we adopt a similar design, but we require neither changes to the storage layer interface nor specialized processors. Moreover, we focus on disaggregating the buffer pool in DRAM, rather than introducing additional caching layers between storage and compute.

The network overhead can be addressed using advances in networking (in addition to compensating for it by using near-data processing). Most of the work on different forms of disaggregated memory relies on RDMA instead of TCP/IP, often extending one-sided operations on RDMA to offload group-based operations for storage replication (e.g., HyperLoop [47]), concurrency and transactions for data structures (e.g., AsymNVM [54]), and memory access operations for key-value stores (e.g., StRoM [68]). RDMA employs the network protocol (InfiniBand [7], RoCE [8]) and the Network Interface Card (NIC) to move data directly between the memory of different machines. At the speed at which networks operate today, RDMA can be used to efficiently transfer large amounts of data across machines at the rates of DRAM memory channels [38]. It is thus especially suitable for disaggregated memory and databases [13]. It has been shown to speed up distributed operators such as data shuffling [52], joins [22, 23], transactional workloads [24], or indexing [76]. In Farview, we use RDMA to efficiently transfer data through the network so that the query processing thread directly gets the data from the remote buffer pool. As suggested by current architectural trends in the cloud, Farview is implemented on top of an FPGA based smart NIC. It supports SQL operators acting on the RDMA data streams as they move along the data path connecting the disaggregated memory to the network. The design efficiently combines near-data processing with a faster network transfers while removing the need for a conventional CPU to support the disaggregated memory (a design resembling that of AQUA, which also uses FPGAs instead of conventional CPUs and also aligned with the way FPGAs are deployed in Microsoft’s Azure [28, 37, 64]).

3 FARVIEW: SYSTEM OVERVIEW

Farview is a smart disaggregated memory with operator offloading capabilities that behaves as a database buffer pool. Traditionally, query processing threads access base tables by reading them from the buffer pool and copying the data to their private working space. With Farview, nothing changes for the query thread, except that the read operation is on remote disaggregated memory rather than local memory, potentially with a subset of the operators already applied.

3.1 Smart buffer pool with operator offloading

Farview exposes a data API to the buffer pool (Section 4.2) that offloads operators to the disaggregated memory. Farview executes an operator pipeline with one or more operators (e.g., a selection and then an aggregation) to process the data as it is read from disaggregated memory, effectively functioning as a bump-in-the-wire stream processor (Section 5). As done in conventional query processing, operator pipelines are constructed from individual blocks that implement a given operator and provide standard interfaces to combine them into pipelines.

Farview supports a range of operators, including: (1) projection operators to reduce the columns returned (and potentially reduce memory accesses) (2) selection operators that filter data according to a collection of predicates; (3) grouping operators that combine tuples (e.g., distinct, group by and aggregation); and (4) system support operators that process data in-situ before sending the data (e.g., encryption/decryption) and perform system optimization tasks like packing the data to reduce the overall network usage.

3.2 FPGA-based architecture

Prototyping smart disaggregated memory requires several components, including DRAM, memory controllers, a network stack, a mechanism to support concurrent access to the memory, and stream processing capacity for operator push-down. Modern FPGAs are a natural match for such functionality, as high performance and flexibility can all be combined in a single device rather than having to connect separate components such as processor, NIC, and memory, all inducing significant data movement overheads. FPGAs can also support substantial amounts of memory local to the FPGA. This onboard memory is usually organized in multiple channels connected to the FPGA chip (even High Bandwidth Memory (HBM)) [14]. Farview’s design (Section 4) leverages these characteristics to implement disaggregated memory as a lean component.

To deploy operators that can process data on the disaggregated memory, the FPGA is divided into multiple isolated virtual dynamic regions that operate concurrently. These dynamic regions can be obtained by different clients and can process different queries. Each dynamic region serves an access request to the disaggregated memory and implements a separate operator pipeline. These regions are dynamically reconfigurable: the logic deployed in them can be
swapped at runtime without having to reconfigure the whole FPGA. This swap takes on the order of milliseconds, depending on the size of the region [48].

An operator pipeline’s combination of operators is precompiled into a hardware design that is dynamically loaded into the FPGA at runtime, upon a request from a client (i.e., a thread processing a query at a computing node). The operators and their pipelines can be modified or extended, and new ones can easily be added by combining the existing ones or changing their parameters.

### 4 FARVIEW: IMPLEMENTATION

Farview is implemented on top of our open source FPGA shell [48]. The shell provides a layer of abstraction hiding services like RDMA network stack and memory virtualization from concurrent system users behind high level interfaces.

#### 4.1 Architecture

As shown in Figure 2, Farview is organized around three main modules: the memory stack, the network stack, and the operator stack. The memory stack (Section 4.4) implements the buffer pool, and can be used as regular memory, with blocks/pages being loaded from storage as needed. The memory stack houses the memory management unit (MMU), which handles all address translations to dynamically allocated on-board memory attached to the FPGA and provides the necessary arbitration and isolation between concurrent accesses. The network stack (Section 4.3) manages all external connections and RDMA requests, providing fair share mechanisms across all concurrent accesses. The operator stack (Subsection 4.5) contains the dynamic logic necessary to push down operators to the disaggregated memory. It lies between the memory and the network stack and it can be seen as a specialized stream processor acting on the data as it moves from the memory stack to the network stack. It also controls how the data is retrieved from the memory stack. The operator stack is reconfigurable and the logic inside can be changed at runtime.

Clients access the disaggregated memory by opening a connection with Farview, which results in the assignment of a dynamic region. Whenever a client makes a request to Farview, the network stack routes the request to the correct virtual dynamic region in the operator stack belonging to the client that initiated the request. The read request is forwarded to the memory stack, which translates the virtual address to a physical address in the on-board FPGA memory, and issues the request. We assume that the clients have local catalog information that is used to determine the addresses of the tables to be accessed. The returned data is streamed back to the dynamic region, where the loaded operators are applied. Finally, the resulting data is forwarded to the network stack, and further sent directly to the memory of the client.

The interfaces of the data and the requests are all based on a simple **AXI stream** handshaking protocol [1], which provides uncomplicated synchronization, pipelining, and backpressure mechanisms, all allowing Farview nodes to support processing at high throughput. The standard interfaces help with portability across different boards as the dynamic region where the operators are loaded always exposes the same set of the interfaces to the operators, thereby simplifying the task of creating the operators. This protocol also allows deep pipelining of the overall design, which allows processing to occur simultaneously in different areas of the system.

To attain high frequencies and reduce the impact of the physical distance between the stacks, data is buffered in queues as it traverses from one stack to the other. The queues, as well as any temporary state created by Farview operators, are implemented using fast on-chip FPGA memory. The buffering allows clear decoupling of processing stages, which helps with structuring the overall system and allows Farview nodes to achieve the operating frequencies necessary to sustain processing at line speeds. The frequencies of the components in Farview range between 250 MHz (network stack, operator stack) and 300 MHz (memory stack).

Compared to existing FPGA frameworks (which support arbitrary functionality), in Farview the dynamic regions must be connected to the network and memory stacks, which have fixed locations within the FPGA, thus reducing the degrees of freedom in placement and sizing. Farview’s management infrastructure must cope with network speeds of 100 Gbps (and even higher internal speeds), which require wide buses (at least 512 bit) [65, 68], further restricting region placement and sizing. We choose pre-defined dynamic regions to accommodate these placement and sizing restrictions. In practice this implies that the size of each virtual dynamic region is fixed and cannot be changed. However, each region is more than large enough for the purposes of offloading the operators we intend to support.

#### 4.2 Farview programmatic interface

Farview exposes a simple high level data API, which provides both the standard low level one-sided RDMA read/write commands to read or write data from/to memory and an extra Farview command, implemented as a one-sided operation that invokes the loaded operator(s) over the read data stream. We use this command as the basis for more complex SQL expressions.
The remote computing node begins by establishing a connection to Farview. In response, it gets a created object representing the connection (QPair), which holds all the necessary information for the connection and is used as an argument to subsequent Farview methods. The following function is used for this purpose:

```c
bool openConnection(QPair *qp, FView *node);
```

Farview memory is virtualized, and can be shared between different remote computing nodes. Since we are focusing on read-only scenarios, Farview does not currently provide concurrency control. Computing nodes allocate memory for tables using the following allocation functions:

```c
bool allocTableMem(QPair *qp, FTable *ft);
void freeTableMem(QPair *qp, FTable *ft);
```

Regular RDMA requests for simple reading/writing of the remote table can be sent with the following two functions:

```c
void tableRead(QPair *qp, FTable *ft);
void tableWrite(QPair *qp, FTable *ft);
```

Farview’s request corresponds to a specialized RDMA verb that invokes the remote processing capabilities with an arbitrary parameter set specific to each operator pipeline. The following generic function is used as the basis for building additional higher level functions supporting specific operator combinations and queries:

```c
void farView(QPair* qp, FTable *ft, uint64_t *params);
```

As an example of a possible higher level function we present a selection operator with real number predicates:

```c
void select(QPair* qp, FTable *ft, uint64_t *projection_flags, float predicate);
```

This function can be used for the following type of queries:

```sql
SELECT S.a FROM S WHERE S.c > 3.14;
```

In this case, the `projection_flags` variable signal column a while the `selection_flag signal column c`. The `predicate` is passed as a value. More complex variations are possible: for instance, if the hardware operator supports it, the predicate operation could also be a variable.

The interface presented here is intended to be used by the query compiler in Farview, rather than directly by the client. The development of the query compiler is left as future work.

### 4.3 Network stack

Farview’s network stack implements a reliable RDMA connection protocol, building on an existing open source stack [68] that implements regular one-sided RDMA read and write verbs. We extend the original stack with support for out-of-order execution at the granularity of single network packets. The out-of-order execution, along with credit-based flow control and packet based processing, allows the Farview to provide the fair-sharing, an important feature in a system shared by multiple separate clients concurrently. Crucially, it prevents any malevolent behaviour by any of the users that could lead to a complete system stall.

Similar to other remote memory systems based on RDMA (e.g., [54]), we add a Farview one-sided verb based on an RDMA write to control the operators. It includes a number of additional parameters containing the necessary signals to the disaggregated memory on how to access and process the data. The network stack manages connections and keeps the necessary state, while remaining highly customizable so that it can support further extensions.

In RDMA, the information describing a single node-to-node connection or RDMA flow is associated with a queue pair. Farview identifies flows using such queue pairs, information that is used internally as well as to route the flow of requests and data through the system. The queue pairs contain unique identifiers which are used to differentiate the flows and to provide isolation through a series of hardware arbiters. Upon connection establishment, each network connection flow and its corresponding queue pair gets associated with one of the virtual dynamic regions and in turn with one data stream from the Farview memory stack. This data stream is used to read the query data into the dynamic regions, process it and finally send it over the network. The operator pipeline corresponding to the flow is loaded into the dynamic region, and the flow is then ready to be processed. Queue pairs are also used to keep track of the dynamically allocated memory locations used in the RDMA requests between remote nodes. This dynamically allocated memory can also be shared between different queue pairs. It is virtual and client sends the virtual address of the local client buffer where data results will be loaded by one-sided RDMA operations from Farview. The client node needs to be equipped with a commercial NIC which supports same RDMA protocol.

### 4.4 Memory stack

The memory stack implements the buffer pool memory using the on-board DRAM memory attached to the FPGA. It handles dynamic memory allocations, address translations, and concurrent accesses.

The central part of this stack is the MMU, which is responsible for all memory address translations to a shared dynamically allocated memory. It propagates and routes all memory requests and subsequent data. It supports the issuing of multiple outstanding requests and has fully decoupled read and write channels. It provides parallel interfaces, isolation and protection for the requests stemming from different dynamic regions with a set of arbitrators, crossbars, and dedicated credit-based queues. Farview’s MMU supports naturally aligned 2 MB pages, which greatly reduces the coverage problem of smaller pages. The MMU contains a translation lookaside buffer (TLB) implemented on Block RAM (BRAM), the fast on-chip FPGA memory. Farview’s TLB holds all virtual-to-physical address mappings for the dynamic regions.

The on-board DRAM memory is organized into multiple channels. The “softcore” memory controllers for these channels are instantiated in the fabric of the FPGA. Each memory channel can provide a certain amount of memory bandwidth. Our prototype uses the Xilinx Alveo u250 [2], which has up to four separate memory channels. For the tests in this paper we utilized up to two channels, each with its own softcore controller that runs at 300 MHz. The width of the interface to the memory channel controller is 64 bytes. This implies a maximum theoretical bandwidth of 18 GBps per channel.
Figure 3: Single dynamic region in the operator stack

(Figure 2). The bandwidth matches the bandwidth usually found on more conventional systems with general purpose CPUs [25].

The multiple channel organization of on-board FPGA memory offers additional parallelization potential. Farview’s MMU provides an interleaved abstraction for DRAM accesses that aggregates the bandwidth from multiple memory channels. It does this by allocating memory in a striping pattern across all available memory channels [48], thus maximizing the available bandwidth to each dynamic region. The higher bandwidth available to each dynamic region also enables a vectorized processing model (Section 5.3).

4.5 Operator stack

The operator stack is where the operator pipelines attached to connection flows to/from memory are deployed. The stack is implemented as a collection of predefined dynamic regions. The operators deployed in the dynamic regions use the interfaces exposed by Farview’s network and memory stacks.

Operator pipeline logic can be deployed and swapped on-the-fly without affecting the integrity and operation of the system or other operator pipelines belonging to other clients. These regions and their access to memory are isolated from each other (see Section 4.4). Such functionality is typically not available in commercial systems, but very often studied in the literature, e.g., [46, 53, 73].

Figure 3 illustrates how a single dynamic region processes a request. The base RDMA read and write requests forward the virtual address and transfer length parameters directly to the memory stack and to the MMU (the blue path in Figure 3), bypassing the dynamic region. If the request is a simple RDMA read/write request, it contains no additional parameters. If the request is a Farview command, it carries a number of operator-specific parameters (green path), along with information about the virtual memory locations it is accessing. The number of parameters can vary depending on the specific operators that are present in the operator pipeline. The write path allows RDMA updates to the memory. The operators’ bump-on-the-wire data processing occurs along the read data path. The width of the input of this path to the dynamic region scales with the number of available memory channels. This way, each dynamic region gets full bandwidth potential of the disaggregated memory and its multiple memory channels. This is possible via the aforementioned striping technique. The output is forwarded to the network stack using a 64-byte datapath width, the same as the provided network interface. This is enough to fully saturate it.

Responses to these requests containing the resulting data are sent via the response channel (green path). With this architecture, operators can dynamically control and influence the size of the response data transfers. This enables the implementation of filtering, for instance, where the size of the filtered data is unknown prior to processing. The direct data streams between the memory controller, the operator, and the network are scaled so as to saturate the bandwidth in each module and to provide optimal performance.

5 FARVIEW: OPERATORS AND PIPELINES

In this section we discuss operator pipelines and four classes of operators: projection, selection, grouping and system support.

5.1 Operator pipelines

As described above, a query is transformed into an operator pipeline, which is deployed on a dynamic region allocated to the corresponding client. An operator pipeline contains one or more operators that provide partial query processing on datapath operations to disaggregated memory. This processing is effectively a bump-in-the-wire that operates on data without introducing significant overheads.

Figure 4 illustrates a generic operator pipeline that includes a broad set of operator classes, including projection, selection (e.g., predicate selection, regular expression matching), grouping (e.g., distinct, group by, and aggregation), and system support (e.g., encryption/decryption).¹ These example operators are described in more detail in the remainder of this section. Which operators are actually present in the pipeline depends on the requested query. In one scenario, the pipeline can support projection, followed by selection and group by. In another, it can support regular expression matching on encrypted strings, which requires decryption early in the pipeline. The reconfigurable nature of the regions provides flexibility, as it allows arbitrary operator types and combinations to be natively supported by the system.

When a query request arrives, it is first forwarded to the projection operator, which requests the data from the memory stack. At the same time, any necessary parameters for additional processing are forwarded to the remaining operators in the pipeline. Data arriving from the memory is processed in a streaming fashion by these operators. Once the processing is done, the resulting data is sent back to the client over the network. Each pipeline has the potential to be fed with input data every single FPGA clock cycle. In query terms, this translates to each pipeline being fed with up to a single tuple in each cycle. In the same manner, a pipeline has the potential to produce results on the output of every cycle. Using this design, operator processing overhead can be efficiently hidden behind the memory and network operations.

Operators are written by the Farview developer as part of the smart disaggregated memory system design, using common hardware description languages like VHDL or Verilog or in the C++-like syntax supported by high-level synthesis tools such as Vivado HLS. The operator pipeline is pre-compiled, so that it can be deployed to a dynamic region at runtime. Operator implementations use Farview’s

¹We assume that all data is stored in row format, but there is nothing intrinsic preventing the support for column data.
network, memory and operator stack interfaces, rather than the interfaces of the underlying FPGA board, which makes the operators portable across Farview deployments on different FPGA boards.

5.2 Projection operators

Projection: A common operation in databases is projection, which returns a subset of a table’s columns. Consider for example a projection of the form SELECT S.car, S.price FROM S, where S.car, S.price are non-consecutive attribute and have a number of attributes of fixed length between them. The projection operator reads the table from the disaggregated memory, parses the incoming data stream based on query parameters describing the tuples and their size, and projects the requested tuples into the pipeline for further processing. During parsing, the tuples are annotated with parameters from the requested query, and obtained from the parameter queues. These parameters are simple flags that state which of the columns are part of the selection, projection or grouping phases. Their interpretation depends on the actual combination of operators being used and their specific implementations.

Smart addressing: In scenarios where queries request only a small subset of the columns from a very wide table, performance would benefit from reading only the requested columns from memory, rather than reading full rows and applying the projection on the incoming data stream. For this purpose, we implement a smart addressing optimization that issues multiple more specific data requests to memory. Smart addressing is most effective when the total number of columns per tuple is large and the number of projected columns is much smaller than the total; otherwise, it is more efficient to read entire tuples and project using annotations, as described above, since the memory access is sequential. We explore the crossover point between these two modes in Section 6.3.

5.3 Selection operators

Selection operations that filter data directly map to the SQL WHERE clause (e.g., in queries of the form SELECT * FROM T WHERE T.a > 50). These operators have the ability to greatly reduce the amount of data to be processed by later stages and ultimately the overall amount of data sent through the network, thus reducing the overall network bandwidth usage. For example in TPC-H Q6, only 2% of the data is finally selected. Pushing the filtering to the disaggregated memory reduces the I/O overhead by orders of magnitude. Farview’s selection operators include both predicate selection and a regular expression matching operator.

Predicate selection: For selection involving conventional data types, the value of an attribute is compared against a constant provided in the query. In FPGAs, such a comparison can be implemented in different ways. We choose to hardwire the selection predicate as an actual matching circuit instead of creating a truth table as done in [72], as Farview has the ability to dynamically exchange the operators. This approach uses fewer resources and, at the same time, supports a variety of different possible predicates. It also permits complex predicates defined over different tuple columns, which can be split into multiple pipelined cycles. The supplied annotations from the request determine which of the columns in the tuple are evaluated during the predicate matching phase.

Regular expression matching: String matching is becoming an increasingly important operator in SQL (e.g. using either LIKE predicates like in TPC-H Q16 or regular expression matching). This is even more eminent in unstructured data types, such as in the case of JSON fields in PostgreSQL. In Farview we have integrated an open source regular expression library for FPGAs [42] and use it to filter strings. In these operators, data is retrieved from the remote node only when it matches the given regular expression. The operator implements regular expression matching using multiple parallel engines, instantiated in the operator stack. The parallelization allows the module to fully sustain processing at line rate. Unlike software solutions, the performance of the operator is dominated by the length of the string and does not depend on the complexity of the regular expression used [42].

Vectorization: Farview implements a limited form of vectorization as an optimization to improve the performance of stateless operators like selection. To alleviate the inefficiencies of the tuple-at-a-time query processing model [40] and its next() function calls that pass tuples from one operator to the next, the database community has adopted query compilation [57] and column stores. Column stores either process data in full batches like MonetDB [26], or in smaller vectors like VectorWise [77]. The latter allows the use of tight loops and/or SIMD instructions to process column data, allowing DBMSs to take advantage of the latest CPU advances for data processing. In Farview, we use a vectorized model similar to that of VectorWise, but with a smaller vector size that is chosen based on the degree of memory striping (described above), rather than to fit the size of the processor’s L1 cache. With vectorization, data is read in parallel from multiple memory channels, and individual tuples are emitted to a set of selection operators executing in parallel. The number of parallel operators is chosen based on the number of memory channels and the tuple width. This approach achieves both higher read bandwidth from the memory stack (due to memory striping) and higher processing throughput (due to the parallel operators).
As the complete hashing is calculated in the FPGA, the distinct operation can be done on multiple columns without noticeable performance overhead, but using more FPGA resources.

To sustain the line rate without negatively affecting the overall pipeline processing, the distinct operator needs to be fully pipelined, to overcome the latency of the lookups and updates of the hash table. This pipelining creates potential data hazards, in the case where two successive tuples with the same value will be inserted into the hash table and ultimately sent over the network as distinct elements. Because of the latency of the hash table, the second (following) tuple cannot see the update produced by the first one. To approach this problem we apply the strategy explained in [72] by implementing an LRU cache to hide the hash table latency. The main difference is the far higher line rate that we have to sustain in our system (over 40 times greater), yielding additional design constraints.

To guarantee full pipelining and constant lookup times, the hash table that we implement does not handle collisions. Instead, collisions are written into a buffer, which is sent to the client to be deduplicated in software. To greatly reduce the collision likelihood, we implement cuckoo hashing, with several hash tables that can be looked up in parallel. Upon the eviction from one of the tables, the evicted entry is inserted into the next hash table with a different function. This occurs in the background and does not affect the full pipelining of the operator.

To successfully hide the latency of the hash table, we implement a cache to hold the most recent keys. The cache needs to be a true Least Recently Used (LRU) cache in order to guarantee the protection from possible data hazards. The standard implementations of LRU caches come with a lot of overhead, as pointers and extra history-keeping data structures need to be present. For this reason, we implement the cache with a shift register which adds a negligible latency to the data streams (the amount depends on the number of cuckoo hash tables), but is able to efficiently provide a quick lookup. The nature of the shift register provides a true LRU replacement policy and this solution thus fully satisfies the strict requirements imposed by Farview. The design of the distinct operator is shown in Figure 5.

Figure 5: Architecture of the DISTINCT operator

5.4 Grouping operators

**Distinct:** The distinct operator eliminates repeated column entries before they are sent over the network. It directly maps to the SQL DISTINCT clause in queries such as `SELECT DISTINCT T.a, T.b FROM T`. It operates by hashing the values and preserving the entries in the hash tables present in the fast FPGA on-chip memory. As the complete hashing is calculated in the FPGA, the distinct operation can be done on multiple columns without noticeable performance overhead, but using more FPGA resources.

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**Group by:** In many applications, data is often read and grouped to perform some form of aggregation (e.g., TPC-H Q1). Operations like these directly map to the SQL GROUP BY clause (e.g., for queries such as `SELECT T.a, COUNT(*) FROM T GROUP BY T.b`). Farview provides a group by operator, with a structure quite similar to the distinct operator; most of the challenges and design choices exist here, as well. The same cuckoo hash tables are used to preserve the groups. The implemented cache in this case is write-through, as it is no longer sufficient to just discard the data prior to sending it. The operator reads the complete table and all of its tuples without sending anything over the network, to perform the full aggregation. At the same time, it inserts the distinct entries into a separate queue. Once the aggregation has completed, the queue is used to lookup and flush the entries from the hash table along with any of the requested aggregation results to the network.

**Aggregation:** In FPGAs, aggregation operators can easily be supported, either standalone, where simple computations are performed directly on the passing data streams, or on top of the group by operator, where each entry in the hash table contains an additional aggregation result. Farview supports a range of standard aggregation operators like `COUNT`, `MIN`, `MAX`, `SUM` and `AVERAGE`.

5.5 System support operators

**Encryption/Decryption:** A key concern for both remote memory and smart disaggregated memory is the need for data encryption [49]. Farview implements encryption so that the data is treated similarly to Microsoft’s Cypherbase [17], where a database stores only encrypted data, but can still answer queries over such data by using an FPGA as a trusted module. We have implemented encryption as an operator using 128-bit AES in counter mode. Since the AES module is fully parallelized and pipelined, it can operate at full network bandwidth. This means that no throughput penalty is paid when this operator is applied on the stream, incurring only a negligible overhead in latency. This allows the data to be stored securely. Because no real processing penalty is incurred, encryption can be placed at multiple spots in the overall system architecture. Similarly one could provide additional system support operators such as compression, decompression, etc.

**Packing:** At the end of the processing pipeline, the annotated columns are first packed based on their annotation flags in a bid to reduce the overall data sent over the network. Multiple columns across the tuples are packed into 64 byte words prior to their writing into the output queue. This packing uses an overflow buffer to efficiently sustain the line rate. In case of the vectorized processing model, the tuples are first combined from each of the parallel pipelines with a simple round-robin arbiter.

**Sending:** The sender unit is the final step before the results are emitted to the network stack. It monitors the queue present in this module where the packed results are written. Based on the status of this queue this module issues specific RDMA packet commands necessary for the production of correct packet header information in the network stack. The dynamic way of handling the RDMA commands by the sender module allows us to create RDMA commands even when the final data size is not known a priori, as is the case with most of the operators.
Table 1: Resource overhead of Farview

| Configuration               | CLB LUTs | Regs | BRAM tiles | DSPs |
|-----------------------------|----------|------|------------|------|
| Packing/Sending             | <1%      | <1%  | 0%         | 0%   |
| En(de)cryption              | 2.1%     | 1.3% | 8%         | 0%   |
| Distinct/Group by           | 3.6%     | <1%  | 0%         | 0%   |
| Regular expression          | <1%      | <1%  | 0%         | 0%   |

6 EVALUATION

In this section we evaluate Farview’s performance, and compare it with alternatives using a local buffer cache or a remote buffer cache. We first describe our experimental setup, including the hardware implementation details of our platforms. We then measure baseline RDMA performance using microbenchmarks, individual query performance using various operators, and query performance with multiple clients.

6.1 Experimental setup

We compare Farview’s smart disaggregated buffer pool (FV) with two different baselines: a buffer cache implemented in local (client) memory, where the processing is done on the local CPU (LCPU), and a remote buffer cache implemented on the memory of a different machine and reachable through a commercial NIC via two-sided RDMA operations (RCPU). This latter configuration resembles what is being done today for storage, where part of the processing is moved to a CPU located in the storage server. It also matches the definition of remote memory proposed in the literature. For RDMA microbenchmark experiments, we compare remote reads from Farview (FV) to remote reads to a different machine using one-sided RDMA operations over a commercial NIC (RNIC). This configuration resembles Farview does not utilize more than 30% of the total on-chip resources. The majority of the utilized on-chip memory is attributed to the memory management unit and the state keeping structures of the operator and network stack. Additionally, most of the implemented operators are not compute heavy and do not consume many resources making it easier to combine them.

6.2 RDMA throughput and response time

For each experiment, we measure the running time until the final results are written to the memory of the client machine for both Farview and the baselines. This makes the performance numbers comparable, as the initial and end states are the same. We evaluate performance for a range of the operators and supported queries. Unless otherwise mentioned, our base tables consist of 8 attributes, where each attribute is 8 bytes long. The results for each experiment are averaged over multiple runs. As the CPU configurations may experience interference (e.g., due to context switches, interrupts), the LCPU and RCPU results are averaged over 10000 runs. Because the FPGA circuits provide more deterministic behavior, the Farview (FV) experiments are averaged over 1000 runs.

To characterize the system, we measure the network throughput and response time of RDMA reads from Farview (FV). For reference and to establish a baseline we also provide the results for the same reads over the memory of a different machine being accessed with a commercial RDMA NIC (RNIC).

Figure 6(a) shows the median throughput for RDMA read operations. In Farview, a single dynamic region is present. To obtain valid read measurements, we measure the network Round Trip Time (RTT) and average it over 1000 runs. The transfer size represents the total data sent over the network for a single request. We vary this parameter until we saturate the network. We set the packet size to 1 kB. The results show the that when we use RDMA and the with up to ten regions, the empirical limit for our device. Similarly to DRAM channels, we choose six to limit compilation times and routing complexity.

The CPU baselines contain Intel Xeon Gold CPUs: LCPU uses a Xeon 6248 (clocked at 3.0–3.7 GHz), and RCPU uses a Xeon 6154 (clocked at 2.5–3.9 GHz). For the CPU RDMA baseline and RDMA base tests (RCPU and RNIC, respectively), we used a commercial Mellanox 100G card (ConnectX-5 VPI)[4]. For the CPU-based baselines we used all available compiler and code optimizations.

Farview does not require a large amount of resources, even considering that it contains the entire management logic, all the dynamic regions, the network stack, and the memory controller. The resources used for the deployed system on the FPGA are shown in Table 1. Farview does not utilize more than 30% of the total on-chip resources. The majority of the utilized on-chip memory is attributed to the memory management unit and the state keeping structures of the operator and network stack. Additionally, most of the implemented operators are not compute heavy and do not consume many resources making it easier to combine them.
As mentioned, selection in Farview can have more than one predicate, even on multiple columns. The overhead of the selection on the overall processing is negligible and is fully hidden behind memory operations. For the evaluation, we run the following query:

```sql
SELECT * FROM S WHERE S.a < X AND S.b < Y;
```

We compare Farview with the aforementioned baseline systems. Since the tuples are 64 bytes, they are equal to the width of pipeline. That leads to highest pipeline throughput, as at every cycle another tuple is forwarded into it. We vary the selectivity of the query and present our results in Figure 8.

As we observe, in all cases (FV, FV-V) Farview outperforms both LPCU and RCPU. LPCU pays a significant price, because it has to read the data from DRAM and not from cache, and also write it back to DRAM. The RCPU baseline additionally has to transfer the data through the network, and therefore in all the cases it is slower than LPCU. The advantage of the bump-in-the-wire processing present in Farview is clear, especially as the amount of data becomes larger. We now go into specific details for every selectivity level.

On Figure 8(a), the query does not discard any tuples and it fetches the whole table. The query is equivalent to executing:

```sql
SELECT * FROM S;
```

Since no data is excluded from the selection predicate, FV and RCPU send the whole table through the network. Farview has similar performance for the vectorized (FV-V) and non-vectorized (FV) models of processing, because the available network bandwidth is the bottleneck (i.e., parallelization does not provide additional benefit). The memory bandwidth of the remote node is thus underutilized in this specific scenario.

Figure 8(b)’s 50% selectivity query alleviates the pressure on the network and permits more utilization of the DRAM bandwidth, leading to higher overall performance for Farview. In this case, the vectorized model is slightly more performant than the standard execution model, as the parallelization of the processing allows the reads from DRAM to occur at higher speeds. Still, even at this selectivity the DRAM bandwidth is not fully utilized for a single client, and the network is again the bottleneck. The execution times of the baselines improve relative to 100% selectivity, especially as the input size grows, but they are still slower than both of Farview’s execution models.

With 25% selectivity, only a small portion of the data is sent over the network, so the network is no longer the bottleneck. For LPCU, data movement between the DRAM and the CPU is reduced because less selected data is written back; as a result, its performance faster as compared to 50% selectivity, but still slower than Farview. For Farview’s non-vectorized model (FV), the bottleneck shifts to the...
bandwidth of a single query pipeline, and its performance remains similar to the 50% selectivity case. The query pipeline parallelization of the vectorized model (FV-V) can fully utilize the large amount of available memory bandwidth, and thus FV-V is roughly twice as fast as FV.

6.5 Grouping

In this section we evaluate the performance of the grouping operators and more specifically the DISTINCT and GROUP BY operators. We use the same baselines as in the selection experiments. For these operators, our baselines use hashing; the implementation is based on a very fast hash map library\(^2\). Figure 9(a) presents the results for the following query:

\[
\text{SELECT DISTINCT} \ (S.a) \ \text{FROM} \ S;
\]

The number of distinct elements is the same as the number of tuples contained in the base table. For the cuckoo hash table implemented in Farview, we assume that no hash collisions occur. In the case of collisions, they would be written in an overflow buffer and sent to the CPU for post-processing.

Farview outperforms both baselines, and the baseline runtimes increase dramatically as the input size gets larger. We attribute part of the difference to reading from/writing to DRAM, as in the case of selection. Two additional factors that explain the slowdown of the baselines are: 1) the memory resizing of the hash table as more elements are added 2) the ability of FPGAs to hash much faster than CPUs, even when the hash function is complex [44]. Additionally in Farview, the query is fully pipelined and there is not much overhead compared to the base selection. Finally, the number of distinct tuples has an impact on the performance, similar to the one selectivity had in the selection experiments. The lower the number of distinct elements is, the lower the amount of data moved through the network, leading to better performance.

Next, we execute a simple query that has a GROUP BY and an aggregation (SUM):

\[
\text{SELECT} \ S.a, \ \text{SUM}(S.b) \ \text{FROM} \ S \ \text{GROUP BY} \ S.a;
\]

In Figure 9(b) and Figure 9(c), we present the performance of the query for increasing data sizes and number of tuples, respectively. The GROUP BY operator performs a similar operation as the distinct operator. The main difference is that in the case of the GROUP BY, we calculate an aggregated statistic. For this reason we first insert all of the tuples being read into the hash table. After the aggregation is complete, the unique entries along with their aggregations from the hash table are sent over the network. This process adds a small amount of latency to the operator execution. The response time is thus bigger if the number of aggregates is higher. Even with this added latency, Farview outperforms the LCPU and RCPU baselines for both experiments, for the same reasons that were mentioned in the distinct experiment.

6.6 Regular expression matching

We compare the performance of Farview and the baselines for regular expression matching for different string sizes, where the regular expression matches 50% of the generated strings. The baselines use the highly optimized Google RE2 regular expression library [5]. FV outperforms both LCPU and RCPU. FV’s regular expression operator is able to sustain the full line rate regardless of the predicate complexity, due to its use of deep pipelining and parallel regular expression engines, which take advantage of the spatial architecture of the FPGA. This implementation outperforms RE2, as the implementation on the CPU has a far smaller parallelization potential and the overhead of the data movement from/to DRAM is quite high.

6.7 Encryption/decryption

As an example of a system support operator commonly used in systems, we explore encryption/decryption. The encryption algorithm used in Farview is a 128-bit AES in parallelized counter mode. The operator can be placed at the beginning or the end of the operator pipelines (handling decryption and encryption) with only a small extra overhead. This allows Farview to, e.g., decrypt data residing in memory for processing and sending it to the client, to encrypt data after processing to secure the transmission to the client, or

\[
\text{SELECT} \ S.a, \ \text{SUM}(S.b) \ \text{FROM} \ S \ \text{GROUP BY} \ S.a;
\]

\[
\text{Figure 9: Response time comparisons for (a) a distinct query, (b) a group by query with aggregation on an increasing number of distinct elements, and (c) a group query by with aggregation on a stable number of elements}
\]

\[
\text{Figure 10: Regular expression matching}
\]

\[
\text{Figure 10: Regular expression matching}
\]

\[
\text{Figure 10: Regular expression matching}
\]

\[
\text{Figure 10: Regular expression matching}
\]

\[
\text{Figure 10: Regular expression matching}
\]
We finally evaluate the behaviour of the system with multiple clients. The throughput graph in Figure 11(b) compares an RDMA read operation in Farview (FV-RD) and the same operation together with the decryption (FV-RD+Dec) done directly on the read data stream. As the throughput graph shows, there is no noticeable performance penalty, indicating that encryption/decryption can be easily combined with all the previous operators without changing the overall performance.

6.8 Multiple clients

We finally evaluate the behaviour of the system with multiple clients reading from memory at the same time. We use six clients running the distinct query in both Farview and the two CPU baselines (LCPU, RCPU). The number of distinct elements is small to prevent the network from becoming the main bottleneck and to maximize DRAM performance in all of the clients. For the CPU baselines, we use MPI with 6 processes. The measurements shown in Figure 12 represent the time taken until all six client queries have completed. Farview achieves better performance than both CPU baselines due to the spatial parallelization between multiple dynamic regions, each containing a separate client. The decoupling of the DRAM and the fair-sharing (Section 4.4) provide optimal distribution of the DRAM bandwidth between all dynamic regions and their clients. Both CPU baselines compete for access both to the DRAM and the shared caches, causing interference that affects the overall performance.

7 CONCLUSIONS

Farview implements network-attached disaggregated memory with the capability to offload parts of query processing directly to the memory. In the paper, we have discussed the design of Farview and how it helps to address the problems of DRAM capacity, by allowing us to move the buffer pool to a central location, and data movement inefficiencies, by enabling near-data processing to filter the data before it is sent through the network. Through the use of RDMA, Farview provides performance that is comparable to that attainable using local memory, a performance advantage that is augmented by the ability to process data in-situ. The next steps for the Farview project are to develop a query optimizer that takes the new parameters and abilities of the system into consideration, to design suitable cache management strategies to move data back and forth to persistent storage, and to expand the range of operations supported. We also want to explore, as part of a query optimizer, options such as performing joins against small tables in the memory by reading the small table into the FPGA and matching the tuples read from memory against it.

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