GuardNN: Secure DNN Accelerator for Privacy-Preserving Deep Learning

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Abstract—This paper proposes GuardNN, a secure deep neural network (DNN) accelerator, which provides strong hardware-based protection for user data and model parameters even in an untrusted environment. GuardNN shows that the architecture and protection can be customized for a specific application to provide strong confidentiality and integrity protection with negligible overhead. The design of the GuardNN instruction set reduces the TCB to just the accelerator and enables confidentiality protection without the overhead of integrity protection. GuardNN also introduces a new application-specific memory protection scheme to minimize the overhead of memory encryption and integrity verification. The scheme shows that most of the off-chip meta-data in today’s state-of-the-art memory protection can be removed by exploiting the known memory access patterns of a DNN accelerator. GuardNN is implemented as an FPGA prototype, which demonstrates effective protection with less than 2% performance overhead for inference over a variety of modern DNN models.

I. INTRODUCTION

Modern machine learning (ML) models such as deep neural networks (DNNs) are compute and memory intensive, and are often executed on hardware accelerators in the cloud [1], [2], [3]. At the same time, the data-intensive nature of DNNs raises a series of concerns for security and privacy. For example, ML algorithms typically require collecting, storing, and processing a large amount of personal and potentially private data which can be exposed or misused by a remote server if it is either compromised or malicious. This paper proposes a secure DNN accelerator architecture, named GuardNN, which enables privacy-preserving ML under untrusted environments. A promising approach to providing strong confidentiality and integrity guarantees under untrusted environments is to create a hardware-protected trusted execution environment (TEE), also called an enclave as in Intel SGX [4]. So far this approach has primarily been studied in the context of general-purpose processors. This paper extends the approach to DNN accelerators as shown in Figure 1. To protect sensitive data, the secure DNN accelerator keeps all confidential information including inputs, outputs, training data, and network parameters (weights) in an encrypted form outside of the trusted hardware boundary, such as a dedicated ASIC/FPGA accelerator chip or an accelerator IP in an SoC. Each accelerator contains a unique private key that can only be used by the accelerator hardware itself. Users can authenticate the accelerator remotely using the corresponding public key and the certificate, and send private inputs and weights encrypted to the accelerator for processing. In this way, the secure accelerator can ensure that private user data and model parameters cannot be accessed by an adversary even if they control software or physically access the accelerator. The secure accelerator can also protect the integrity of ML computation by incorporating remote attestation and off-chip integrity verification.

While GuardNN adopts the high-level approach of the secure enclaves such as Intel SGX, it addresses the new challenges raised by the ML acceleration to protect a large amount of data in a heterogeneous system and improves both security and performance over the general-purpose enclaves. Unlike processors that are allowed to perform arbitrary operations and memory accesses, custom accelerators only need to support a relatively small set of operations and often have a memory access pattern that is specific to the target application. This application-specific nature of accelerators enables GuardNN to customize both its security architecture and protection mechanisms for DNN computations, and provide strong security with almost no performance overhead.

The following summarizes the key benefits and insights that GuardNN provides compared to directly applying today’s enclave approach to DNN accelerators. 1) GuardNN carefully designs its architecture and instructions to enable confidentiality and integrity protection without trusting a host CPU that controls scheduling and resource allocation. This design reduces the trusted computing base (TCB) to just the accelerator. 2) The GuardNN instruction set enables confidentiality-only protection, which is sufficient for privacy-preserving ML, without the complexity and overhead of integrity protection. 3) GuardNN introduces a new application-specific memory protection (ASMP) scheme, which enables memory encryption and integrity verification with almost zero overhead by customizing protection for the DNN memory access patterns. 4) We make an observation that the memory access pattern and the timing of a DNN accelerator without dynamic pruning is independent of input and weight values, which enables strong...
side-channel protection not available in today’s TEEs.

To validate and evaluate the GuardNN design, we implemented a prototype system based on CHaiDNN [5], an open-source DNN accelerator from Xilinx. This FPGA prototype implements the customized memory encryption scheme for confidentiality protection. The experimental results on a Xilinx Zynq UltraScale+ FPGA board demonstrate functional correctness and show that the overhead of memory encryption is negligible. For more detailed analyses, we performed additional experiments using a combination of RTL simulation for CHaiDNN and cycle-level simulation for a memory system. The simulation results show that GuardNN can provide both memory encryption and integrity verification with almost no overhead. The results suggest that today’s general-purpose memory protection schemes lead to 30% performance overhead as memory bandwidth is often a bottleneck in DNN accelerators. The prototype and the analysis also show that the area overhead of GuardNN mainly comes from AES encryption engines and is small compared to today’s DNN accelerators.

This paper makes the following major contributions:

- We present a secure DNN accelerator architecture and interface, which enables secure DNN computation in untrusted environments with a minimal TCB and decoupled protection for confidentiality and integrity.
- We propose an application-specific memory protection scheme, which minimizes the performance overhead of memory protection by customizing protection for application-specific memory access patterns.
- We demonstrate the low performance overhead of GuardNN through both a functional FPGA prototype and detailed simulation studies. The overhead of GuardNN is less than 2% for DNN inference on the state-of-the-art models.

II. SECURE DNN ACCELERATOR ARCHITECTURE

A. Threat Model

We assume that a DNN accelerator is capable of running both DNN inference and training. A scheduler runs on a host CPU and coordinates computation and data movement by communicating with a remote user and issuing commands to the DNN accelerator. The remote user sends inputs and a DNN model and receives final results.

The goal of a secure DNN accelerator is to protect the confidentiality and optionally the integrity of DNN data and computation in an environment where only the accelerator itself can be trusted. For privacy, the secure DNN accelerator aims to protect inputs, outputs (prediction results), training data, network parameters (weights), and all intermediate results as secrets. On the other hand, we consider the DNN network architecture as public information and do not hide the network structure. For integrity, the secure DNN accelerator aims to detect any unauthorized changes to its state and execution so that a user can verify that the output represents the outcome of the given DNN model/input.

The DNN accelerator itself is trusted and authenticated by the remote user using a unique private key that is only known by the accelerator hardware. The accelerator hardware needs to be designed and fabricated by a trusted manufacturer. The manufacturer also needs to securely embed a private key specific to each accelerator instance, and provide a certificate. We assume that the internal operations and state of the DNN accelerator cannot be directly observed or changed by an adversary whereas anything outside of the accelerator including off-chip memory and a host processor are assumed untrusted.

We aim to prevent information leakage through memory and timing side-channels by ensuring external memory accesses and timing are independent of secret data. Other physical side-channels, such as the power and EM side-channels, are not considered. We also do not consider adversarial examples that exploit weaknesses in a model itself.

B. Key Insights and Features

Today’s secure enclaves for processors aim to provide general-purpose protection and support arbitrary code inside an enclave. On the other hand, the interface and protection mechanisms can be customized for the target application scenario and workload when protecting an application-specific accelerator. GuardNN leverages this high-level insight to reduce its trusted computing base (TCB), reduce complexity and overhead, and provide stronger security. Here, we summarize the key insights and features in GuardNN for application-specific protection for privacy-preserving deep learning.

Insight 1. Small TCB: The accelerator can allow untrusted host to manage scheduling and resource allocation if no instruction can leak secrets.

DNN accelerators typically rely on scheduling and optimization algorithms on a host processor to determine which operations to run. Directly extending today’s secure enclave will lead to a large TCB with complex mechanisms, requiring protection mechanisms for both the host processor and the accelerator, and a secure communication channel between them. Instead, GuardNN ensures confidentiality without trusting a host processor by designing its accelerator instruction set so that sensitive information is always encrypted no matter which instruction is executed. The outputs are encrypted so that they can only be decrypted by the remote user who initiates a session and sends an encrypted model, weights, and inputs. The untrusted host processor chooses which DNN operations to be performed, but cannot make the accelerator produce outputs.
in plaintext. This design significantly reduces the size of the TCB and the cost of adding security protection.

**Insight 2. Confidentiality-Only Protection:** By always encrypting outputs and making the external behavior independent of data, confidentiality can be provided without integrity.

The custom instruction set enables GuardNN to decouple confidentiality and integrity protection, and protect the confidentiality of private data without paying the cost of integrity protection. Regardless of the sequences of instruction, private data are always encrypted outside the accelerator. In addition, the memory access patterns and execution times of DNN accelerators without dynamic pruning [6], [7], [8], [9], [10], [11] are independent of input data values. Hence, the confidentiality guarantees of GuardNN do not depend on the integrity of the instruction sequences and data values. In contrast, the secure enclaves require integrity protection even for confidentiality; since the trusted software inside the enclave is allowed to output confidential information unencrypted, the integrity of the program must be protected even when only confidentiality is needed.

**Insight 3. Application-Specific Memory Protection:** For accelerators, the overhead of memory protection can be greatly reduced by customizing protection for a specific application.

The cryptographic protection of off-chip memory, typically represents the main source of overhead in secure processors [4], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. The traditional memory protection requires additional meta-data such as version numbers and Message Authentication Codes (MACs) stored in memory. Meta-data accesses add delays and also consume memory bandwidth, which is often a scarce resource in DNN accelerators. Modern ML models increasingly require a more massive amount of memory, and memory protection can lead to nontrivial performance overhead for bandwidth-limited ML models. For example, recommendation networks may need tens to hundreds of GBs for embedding tables with poor temporal locality [26].

The overhead of memory protection can be significantly reduced by customizing the protection for DNN computation. The key observation is that application-specific accelerators move data between on-chip and off-chip memory following a relatively simple pattern that is tailored to an application and largely known at the design time. For example, the memory accesses in a DNN accelerator follow a simple and static pattern specific to a given DNN structure. By exploiting the application-specific memory pattern for DNNs, GuardNN calculates version numbers from its state without storing them in off-chip memory; when integrity protection is needed, it maintains MACs at a coarse granularity that matches the accelerator’s access granularity. This application-specific memory protection (ASMP) enables confidentiality and integrity protection with almost no performance overhead. Moreover, for confidentiality-only protection, ASMP requires no off-chip meta-data and can be added to an existing DNN accelerator with no impact on scheduling and data placement.

**Insight 4. Side Channel Resilience:** Accelerators tend to have more regular memory access patterns and provide an opportunity for stronger side-channel resilience at low costs.

For a DNN accelerator without dynamic pruning techniques, the memory access pattern and the timing of a given DNN model are agnostic to inputs and weights. In that sense, DNN accelerators provide strong protection against software-visible side-channels such as timing and memory access patterns, which is expensive in general-purpose processors.

**C. GuardNN Architecture**

Here we introduce the GuardNN architecture and the protection mechanisms. Figure 2 shows the high-level block diagram, and Table I summarizes the protection mechanisms.

The accelerator needs to be able to establish a secure communication channel with a remote user. For this purpose, GuardNN requires a unique private key (SK\textsubscript{Accel}) and a true random number generator (TRNG) in each secure accelerator, and introduces an instruction that allows the accelerator to securely exchange a symmetric key (K\textsubscript{Session}) with the remote user. We assume that the user obtains the corresponding public key using a public key infrastructure (PKI) as in Intel SGX or Trusted Platform Modules (TPMs). DNN model parameters, inputs, and outputs are sent through the secure communication channel. GuardNN provides instructions to import encrypted inputs and parameters, and produce an encrypted output.

During the execution, the GuardNN accelerator receives instructions from its host CPU to perform DNN computations. The instruction set is carefully designed to ensure that confidential information is always encrypted outside the accelerator no matter which instruction runs. For side-channel protection, GuardNN requires that the timing and memory access pattern of the accelerator are independent of secret data such as user data and model parameters. This ensures that confidentiality is protected without trusting the host.
To protect data in external memory (DRAM), GuardNN includes a memory encryption (Enc) engine that encrypts data in DRAM, and an integrity verification (IV) engine that detects unauthorized changes on a read from external memory. To minimize the performance overhead of memory protection, GuardNN introduces a new memory protection scheme as detailed in Section IV. The memory protection scheme is based on the counter-mode encryption, and GuardNN maintains a set of counters which ensure the same version number is never re-used for encryption. Table II summarizes the cryptographic keys and the accelerator state in GuardNN.

For integrity protection, at runtime, GuardNN computes the hashes of inputs and weights when they are imported, and the hash of each running instruction and its input arguments. Then, GuardNN provides an instruction that signs the hash of the output and other hashes using the accelerator’s private key so that the user can check the initial state and the execution. As shown in Figure 2, a microcontroller is used to perform these instructions.

III. GUARDNN INSTRUCTION SET

This section describes the GuardNN instruction set and shows how the instructions can be used for DNN inference.

A. GuardNN Instructions

The GuardNN instruction set is designed to be an extension that can be added to a DNN accelerator without changing the base instructions. Table III shows three instructions for common DNN operations and the GuardNN extension for security functions. A user can choose if integrity protection is needed when initiating a session. If it is enabled, the operations inside the parentheses will be performed.

GetPK: Returns the public key (PK) and the certificate (Cert).
InitSession: Given a public key from a remote user, the accelerator runs a key exchange protocol to agree on a symmetric session key and establish a secure communication channel with the user. In this work, we use the DHE key-exchange protocol and the standard AES counter mode (AES-CM) for encrypted communications for inputs, weights, and outputs. We will not elaborate the details of our particular implementation here, since this is a well-known problem that can be solved by standard protocols. Other protocols such as SSL can also be used for encrypted and authenticated communication.

The accelerator also clears all states (keys, data, and hashes), sets a new memory encryption key (K_{MEnc}), resets all counters to zero, and enables memory protection. If integrity protection is enabled, memory integrity verification (IV) and hashing of instructions and their operands are also enabled.

SetWeight and SetInput: On SetWeight, the accelerator imports encrypted weights; these weights are decrypted with the session key (K_{Session}) and protected by the accelerator’s memory encryption and optionally integrity verification schemes. Then, the weight counter (CTR_W) is incremented (see Section IV). Similarly, on SetInput, the accelerator imports the encrypted input from the user into its protected memory, and increments the input counter (CTR_{IN}). If integrity protection is enabled, the accelerator also computes the hash of the input/weights for remote attestation.

ExportOutput: The accelerator reads the output of DNN computation from its protected memory, and re-encrypts the output with K_{Session} so that the output can be sent to the user.

SignOutput: The accelerator computes a digital signature of the hashes of the input, output, weights, and the sequence of instructions/operands using its private key (SK_{Accel}). By verifying this signature using the corresponding public key, the user can verify that the output was produced by the particular accelerator using the correct initial state and the correct sequence of instructions.

SetReadFID: The application-specific memory protection scheme (detailed in Section IV) uses the feature map ID (i.e., ID_{FR}) to determine the version number when decrypting feature values. This number is pre-determined based on the network structure and scheduling, and does not need to be trusted for confidentiality as it only affects decryption. To reduce hardware overhead, GuardNN lets the host CPU to set the feature ID for an address range (base and bound addresses).

B. DNN Execution using GuardNN Instructions

Figure 3 illustrates how DNN inference is performed using GuardNN instructions. 1. The host uses GetPK to obtain the PK and the certificate of the accelerator, and sends them to the remote user. The user uses a PKI to verify that the PK belongs to a trustworthy accelerator.

2. The user initiates a secure session with the accelerator using InitSession. Our implementation uses the DHE key-exchange protocol; the user sends the public part of a randomly-
SetWeight weights into DRAM, and calls weights. The host CPU parses the model, loads the encrypted
Traditional memory encryption and the DFG of a DNN model.

encryption (AES-CM) to hide AES latency. AES-CM requires techniques [28], [29], [14] typically use the counter-mode
A. Memory Protection Basics
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Fig. 4: Memory encryption and integrity verification.

generated ephemeral key-pair (PKUE), and the accelerator also generates an ephemeral key-pair and sends the public part (PKXE) signed by its private key SKacc. The user verifies that the received ephemeral key belongs to the trusted accelerator and computes a symmetric key, as does the accelerator. The host CPU passes messages between the two.

The user sends a plaintext DNN definition, and encrypted weights. The host CPU parses the model, loads the encrypted weights into DRAM, and calls SetWeight. The accelerator decrypts the weights and protects them with the application-specific memory encryption scheme. Similarly, the user sends an encrypted input that is imported by the accelerator on the SetInput instruction. At this point, the accelerator is ready to execute the DNN inference.

For each layer, the host CPU uses SetReadFID to set IDf, for the input features, and issues Forward to start the computation. The accelerator performs the computation while keeping both input and output features encrypted in memory. For training, the host CPU also uses the base instructions for training (Backward and Aggregate) to update the weights.

After all the layers are finished, the host CPU uses ExportOut to obtain an encrypted output, and sends the encrypted output to the user. If integrity protection is needed, the host also sends the digital signature from the SignOutput instruction. The user receives the output and digital signature, decrypts the output, and verifies the hash values and the digital signature to check the integrity of the output.

IV. APPLICATION-SPECIFIC MEMORY PROTECTION
This section presents the application-specific memory protection (ASMP) scheme in GuardNN, which provides secure yet low-overhead memory protection leveraging regular and mostly static memory access patterns of DNN accelerators.

A. Memory Encryption – As shown in Figure 4a, existing techniques [28], [29], [14] typically use the counter-mode encryption (AES-CM) to hide AES latency. AES-CM requires a non-repeating counter value for each encryption under the same AES key. In a secure processor, the counter value often consists of the physical memory address (PA) of the data block that will be encrypted and a (per-block) version number that is incremented on each memory write. When a data block is written, the encryption engine increments the VN and then encrypts the data. When a data block is read, the encryption engine retrieves the VN used for encryption and then decrypts the block. Let $K_{Enc}$, $V$ be the AES encryption key, plaintext, and ciphertext, respectively. The AES encryption can be formulated as $V = U \oplus AES_{K_{Enc}}(PA||VN)$, where $\|$, and $\oplus$ represent bit-field concatenation and XOR, respectively.

As general-purpose processors can have an arbitrary memory access pattern, the VN for each cache block can be any value at a given time. In order to determine the VN for a later read, a secure processor needs to store the VNs in DRAM. To avoid re-using the same counter value, the AES key needs to change once the VN reaches its maximum, which implies that the size of the VN needs to be large enough to avoid frequent re-encryption. For example, Intel SGX [29] uses a 56-bit VN for each 64-byte data block, which introduces 11% storage and bandwidth overhead. In general, the VNs cannot fit on-chip and are stored in DRAM. As the VNs are stored in the off-chip memory, the integrity and freshness of VNs also need to be protected with MACs to ensure the confidentiality.

Integrity Verification – To prevent off-chip data from being altered by an attacker, integrity verification cryptographically checks if the value from DRAM is the most recent value written by the processor. For this purpose, a MAC of the data value, the memory address, and the VN is computed and stored for each data block on a write, and checked on a read from DRAM. However, only checking the MAC cannot guarantee the freshness of the data; a replay attack can replace the data and the corresponding VN and MAC in memory with stale values without being detected. To defeat the replay attack, a Merkle tree (i.e., hash tree) [30] is used to verify the MACs hierarchically in a way that the root of the tree is stored on-chip. As shown in Figure 4a, a state-of-the-art method [31] uses a Merkle tree to protect the integrity of the VNs in memory, and includes a VN in a MAC to ensure the freshness of data. Previous designs use Carter-Wegman MAC [29] and AES-GCM [32] as the hash function. Let us denote the key, plaintext, and ciphertext as $K_{IV}, U, V$, respectively. The MAC of an encrypted data block can be calculated as $MAC = H_{K_{IV}}(V||PA||VN)$. The overhead of integrity verification is nontrivial as it requires traversing the tree stored in DRAM. To mitigate this overhead, recently verified MACs are stored in a cache.

B. Application-Specific Version Number Generation
The main overhead of memory protection comes from storing and accessing VNs and MACs for VNs in the off-chip memory. Because DNN accelerators are often memory-intensive, these additional meta-data accesses can lead to non-trivial performance overhead. We propose to significantly reduce the memory protection overhead by generating VNs without storing
them in memory and customizing the protection granularity based on the application-specific memory access pattern.

As their memory accesses are customized for a particular application, specialized accelerators tend to have more predictable and regular memory access patterns compared to general-purpose CPUs. In particular, both DNN inference and training can be scheduled statically based on the network structure. For example, most popular ML frameworks such as Caffe [27], TensorFlow [33], and MXNet [34] adopt declarative programming, where the frameworks optimize the static data-flow graph (DFG) before execution. Given a DFG, the operations and the corresponding memory accesses in that DFG are scheduled statically. The scheduler can assign a VN for each memory access without storing the VNs in memory.

Moreover, DNNs have the same access pattern to a large chunk of memory. For example, DNNs without dynamic pruning write the output feature maps of a layer to DRAM the same number of times. As VNs reflect the maximum number of writes to the corresponding memory block, this regular memory access pattern means that we only need one VN for all the output features of a layer. For example, if DNN accelerators only write the output features to DRAM once per layer, we can simply use the layer number as part of the VN.

Based on the observations, we propose to generate VNs from the accelerator state instead of storing them in memory. When the DNN scheduler is trusted, the scheduler can assign VNs for both memory reads and writes based on the DFG before execution. Given a DFG, the scheduler can assign VNs for memory writes using on-chip counters and ensure that the same VN value is never reused for encrypting one memory block even with an untrusted scheduler. For memory reads, GuardNN receives VNs from the scheduler on the host CPU. The scheduler can easily determine the VNs for reads as it owns the DFG and controls the scheduling of DNN. Note that VNs for reads do not affect confidentiality because they are only used for decryption. Once the VN is determined, the encryption (Enc) engine can decrypt/encrypt each 128-bit data block using the same equations in AES-CM. As the VNs no longer need to be stored in DRAM, the integrity protection for VNs (e.g., Merkle tree) also becomes unnecessary.

For integrity protection, MACs still need to be stored in memory. We propose to reduce the overhead of integrity protection by customizing the size of a memory block that each MAC protects to match the data movement granularity of the accelerator. For example, the DNN accelerator that we use for a prototype reads a 512-B chunk from memory at a time.

For reading the input features written by the previous layer, GuardNN uses $\text{ID}_{\text{FE}}$ from the scheduler on the host CPU to form the VN, and thus avoids tracking the status of the VN. We use a constant as the VN for the weights until they are updated. To allow updating weights, GuardNN adds $\text{CTR}_{W}$ in the accelerator state and keeps track of the number of updates to the weights ($\text{SetWeight}$ instruction).

Algorithm 1 shows the VN generation for the key instructions used in DNN inference. Note that $\text{CTR}_{IN}$, $\text{CTR}_{W}$, and $\text{CTR}_{FEW}$ are all kept in on-chip registers, and there is no VN stored in external memory. The on-chip counters can be made large enough to avoid overflows. For the 53-bit $\text{CTR}_{IN}$ in our design, an accelerator with a throughput of 1000 inputs per second can run for 0.28 million years before an overflow.
Algorithm 1: The pseudo-code for GuardNN instructions — 

\[ \text{Input} : \text{input data } \mathbf{in}, \text{input features } \mathbf{x}_i, \text{and weights } \mathbf{w}_i \text{ of layer } l \]
\[ \text{Output} : \text{output features } \mathbf{y}_i, \text{of layer } l, \text{output prediction } \mathbf{out} \]

1) **SetInput** /* Re-encrypt the input using ASMP */
   \( \mathbf{in} = \text{LD}_{\text{Ksource}}(\mathbf{in}, \text{Addr}); \)
   \( \text{CTR}_{\text{IN}}++; \text{CTR}_{\text{RF}} = 0; \)
   \( \text{ASMP.ST}_{\text{in}}(\mathbf{in}, \mathbf{x}_0, \text{Addr}, \{0 \| \text{CTR}_{\text{IN}} \| \text{CTR}_{\text{RF}}\}); \)
2) **Forward** /* Forward propagation of a layer */
   \( \mathbf{w}_l = \text{ASMP.LD}_{\text{Ksource}}(\mathbf{w}_l, \text{Addr}, \{1 \| \text{CTR}_{\text{RF}}\}); \)
   \( \mathbf{x}_l = \text{ASMP.LD}_{\text{Ksource}}(\mathbf{x}_l, \text{Addr}, \{0 \| \text{CTR}_{\text{IN}} \| \text{CTR}_{\text{RF}}\}); \)
   \( \mathbf{x}_{l+1} = \text{ReLU}(\mathbf{x}_l \cdot \mathbf{w}_l); \)
   \( \text{ASMP.ST}_{\text{in}}(\mathbf{x}_{l+1}, \mathbf{x}_{l+1}, \text{Addr}, \{0 \| \text{CTR}_{\text{IN}} \| \text{CTR}_{\text{RF}}\}); \)
   \( \text{CTR}_{\text{RF}}++; \)
3) **ExportOutput** /* Re-encrypt the output */
   \( \mathbf{out} = \text{ASMP.LD}_{\text{Ksource}}(\mathbf{y}_l, \text{Addr}, \{0 \| \text{CTR}_{\text{IN}} \| \text{CTR}_{\text{RF}}\}); \)
   \( \text{St}_{\text{Ksource}}(\mathbf{out}, \text{out, Addr}); \)

**DNN Training** — One iteration of training consists of a forward propagation and a backpropagation. The forward propagation is the same as inference except that all features are saved, and can use the VN generation strategy for inference. Here, we describe the VN generation for the backpropagation. Figure 6b shows the DFG of the backpropagation. Each vertex first computes the gradients flowing to the previous vertex using the gradients flowing to current vertex and the associated weights (e.g., \( \mathbf{g}_1 = \mathbf{g}_2 \cdot \mathbf{w}_h \)). Then, the layer’s weights are updated using the incoming gradients and the saved features (e.g., \( \mathbf{w}_b^+ = -\eta \cdot \mathbf{g}_b \cdot \mathbf{f}_2 \)).

The VNs are constructed the same way as shown in Figure 5. The backpropagation only adds additional reads to the features and does not affect the VN generation for features. The VNs for weights still use CTR\(_W\) as all weights are updated the same number of times. However, CTR\(_{IN}\) and CTR\(_W\) are incremented more frequently; CTR\(_{IN}\) is incremented on each training iteration even if there is no new input. CTR\(_W\) tracks the number of updates to the weights. Each gradient edge in the DFG has a corresponding feature edge. As the gradients and the features are stored in different memory locations, the gradients can use the VN for the corresponding features.

**V. SECURITY ANALYSIS**

As our threat model assumes that the internal operations and state of an accelerator cannot be directly observed or changed, an adversary can only attack external interfaces or components: 1) communication with a user, 2) off-chip memory, 3) host interface, and 4) side channels.

**Communication channel** — GuardNN provides mechanisms to establish a secure communication channel with a remote user that protects confidentiality, integrity, and freshness. More specifically, the current implementation supports the standard DHE key-exchange protocol, and a true random number generator for secure key generation. The user can also use a PKI to ensure that they are interacting with a trustworthy accelerator. As secure network communication is a well-established area with standard solutions such as SSL, secure accelerators can adopt an existing solution for this attack surface.

**Off-chip memory** — GuardNN includes memory encryption and integrity verification to protect confidentiality and integrity of data stored in external memory. The memory protection unit is enabled on the **InitSession** instruction before any sensitive data are placed in memory, and all off-chip memory accesses are protected with no exception. The memory encryption key also is changed (newly generated using the TRNG) for every session. The proposed memory protection scheme uses the standard AES counter-mode encryption and the standard MAC construction used in today’s secure processor designs, with the only difference that that the version numbers (VNs) are not stored in off-chip memory. Therefore, if the VN is unique for each write to a given memory location, the proposed memory protection scheme is equivalent to the standard AES counter-mode encryption and MAC. As discussed in Section IV-B, GuardNN ensures that the VN is different for each write by increasing the counters inside the accelerator after each write to features/weights.

**The accelerator’s host interface** — The host CPU can arbitrarily change the instructions and input operands to the accelerator. However, GuardNN’s instruction set does not include any instruction that outputs confidential information in plaintext. In fact, memory accesses and outputs from the GuardNN accelerators are always encrypted. Although the on-chip counter values (CTR\(_{IN}\), CTR\(_W\), and CTR\(_{RF}\)) for VNs can be affected by some GuardNN instructions, these counters can only be incremented. If one of the counters overflows, the accelerator stalls and a user needs to initiate a new session. Hence, no instruction can be used to make the encryption engine reuse the same counter value.

For integrity, the accelerator computes the hashes of weights, inputs, outputs, and a sequence of instructions and supports remote attestation. While a malicious host can perform a DoS attack and also make the GuardNN accelerator generate incorrect results, such changes in the initial state or the instruction sequence can be detected by the remote user.

**Side channels** — DNN accelerators without dynamic pruning have memory access patterns and timing that are independent of private values such as inputs, outputs, and weights. In that sense, they are secure against memory and timing side channels. GuardNN does not protect against physical side channels.

**VI. EXPERIMENTAL RESULTS**

**A. Methodology**

**DNN Accelerator** — We use CHaiDNN [5], an open-source accelerator from Xilinx for our experimental evaluation. CHaiDNN consists of an array of processing elements to perform multiply–accumulate operations, and is built for 8-bit quantized operands. To hide the memory access latency, CHaiDNN exploits double buffering as shown in Figure 7. At a high level, the accelerator overlaps loading weights for the next block with the computation for the current block.
The memory accesses are simulated using DRAMSim2 [37] by simulating protection mechanisms and DRAM accesses. To calculate the total execution time and the bandwidth usage, we generate a trace of computation and memory events. Then, the accelerator is simulated in a cycle-accurate RTL simulator to calculate the total execution time and the bandwidth usage.

The CHaiDNN simulator has three main components — accelerator, memory protection, and off-chip memory. The CHaiDNN model is used to validate our instruction set design and is functional for memory encryption protection. We also obtained estimates needed to match the memory bandwidth used by CHaiDNN.

### Cycle-level Simulation
We use cycle-level simulations to (1) compare the overhead of multiple memory protection schemes, (2) study the overhead of integrity protection, and (3) evaluate the overhead for DNN training. As shown in Figure 8, the simulator has three main components — accelerator, memory protection, and off-chip memory. The CHaiDNN accelerator is simulated in a cycle-accurate RTL simulator to generate a trace of computation and memory events. Then, a memory protection simulator (in Python) uses the event trace to calculate the total execution time and the bandwidth usage by simulating protection mechanisms and DRAM accesses. The memory accesses are simulated using DRAMSim2 [37].

### FPGA Prototype
We implemented a prototype of the GuardNN accelerator on the Xilinx ZCU102 by adding the VN generator and encryption engine (AES-128) to the CHaiDNN accelerator. The prototype uses a CHaiDNN configuration with 512 DSP blocks and 8-bit weights/activations. The AES engines are fully-pipelined with a 12-cycle latency. The FPGA prototype is verified against Verilog timing models from Micron.

### FPGA Prototype Results
Table IV shows the throughput for various DNNs on our FPGA prototype. The performance overhead is less than 2% on all networks for ImageNet dataset. The relatively higher overhead for ResNet is not due to our scheme, but a result of inefficient scheduling by HLS for memory accesses in the element-wise addition layer. The results show that we can get near-zero memory encryption overhead in real systems.

In our FPGA prototype, we use an open-source AES-128 IP core [38] that uses 9.0K LUTs and 3.0K FFs. The area overhead of one AES core is 8.2% and 2.6% in LUTs and FFs, respectively. Because the FPGA clock (200 MHz) is much slower than the memory bus clock, three AES engines are needed to match the memory bandwidth used by CHaiDNN.
We also implemented the microcontroller (see Figure 2) as a Xilinx MicroBlaze [39], for which the controller program can fit within 256KB local memory. The soft processor’s resource usage (overhead) was 3.7K LUTs (3.4%), 2.4K FFs (2.1%), 64 BRAMs (11.0%) & 6 DSPs (0.9%).

Here, we present the latency of various GuardNN instructions using the compute and memory intensive VGG network as an example. GuardNN needs to perform a key exchange and load weights once per session. On the MicroBlaze, the GetPK and InitSession (specifically, ECDHE–ECDSA and SHA-256 for deriving $K_{Session}$) take 25ms. The key-exchange latency is independent of a network. Importing (decrypting and re-encrypting) weights on SetWeight takes 43ms for the 138M parameters using AES engines. The CHaiDNN latency of inference for a single input is 111ms for VGG. For each input, GuardNN adds overhead to import an input, and export/sign an output. SetInput for a single input image only takes 0.05 ms. For the 1000-class output, the ExportOutput and SignOutput take 7 ms. This recurring per-output latency can be hidden by pipelining it with the inference of the next input. Thus the GuardNN extension instructions incur negligible overhead when processing multiple inputs.

C. Simulation Results

We compare the accelerator performance with three different protection schemes: no protection (NP), today’s baseline memory protection (BP), and the application-specific memory protection (ASMP). For BP and ASMP, we also study the encryption-only protection (Enc), and protection involving both encryption and integrity verification (EncIV); $BP_{Enc}$ and $BP_{EncIV}$ for BP and ASMP for ASMP.

Memory Traffic Increase – As the throughput of a DNN accelerator is often limited by the memory bandwidth, we first compare the memory traffic increase. The memory traffic increase is defined as the ratio between the total number of memory accesses with and without memory protection. ASMP$_{Enc}$ has no impact on the memory traffic because it does not require any meta-data (i.e., VNs) to be stored in off-chip memory. Figure 9 compares the memory traffic increase of inference and training.

![Memory Traffic Increase Comparison](image)

**Fig. 9:** The mem. traffic increase of inference and training.

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time with 1, 2, and 4 DDR channels. The performance of GuardNN with the application-specific memory protection (ASMP_{Enc} and ASMP_{EncIV}) is almost the same as the one with no protection for all configurations. For the baseline protection scheme (BP), the performance overhead is noticeably higher with only one DDR channel as the accelerator becomes more memory-bound. The overhead is reduced with more DDR channels as more DNN layers become compute-bound.

D. ASIC Area Overhead Estimate

The application-specific memory protection scheme does not require an on-chip cache for version numbers and MACs, and only use a small number of registers for keys and counters. In that sense, the area overhead mainly comes from the AES engines, used for both encryption and integrity verification.

The area and power overhead will be low for an ASIC design. TPU-v1 runs at 700 MHz in 28nm and has a peak memory bandwidth of 272 Gbps. The area and power consumption of TPU-v1 is 331 mm² and 75 W, respectively. An ASIC low-power AES engine [40] achieves a 991 Mbps throughput at 875 MHz in 28 nm. The area and power consumption of the AES engine is 0.0031 mm² and 3.85 mW, respectively. Assuming the AES engine runs at 700 MHz with the same power consumption, 344 AES engines are required to match the memory bandwidth of TPU, which leads to 0.3% area and 1.8% power overhead. We can also use a smaller number of high-performance AES engines with similar overall overhead.

VII. DISCUSSION

Static and Dynamic Pruning – Static pruning still results in a static network model that can be executed by GuardNN. At a glance, it may appear that application-specific memory protection does not work with dynamic pruning, which skips memory accesses for some features and weights at run time. However, skipping VNs does not affect the security of memory protection as long as the VNs are not reused. The decryption and integrity verification will also be functional as long as a write and the corresponding reads use the same VN. We implemented multiple dynamic pruning schemes such as Compressed Sparse Row [41], Compressed Sparse Column [42], [43], and Run-Length Compression [6], [44] in PyTorch and emulated the proposed memory protection scheme in software. The study shows that the ASMP is still applicable to DNNs with dynamic pruning; pruning removes both writes and following reads to the pruned features and weights, and the VNs from the proposed scheme can still be used for unpruned features and weights. In that sense, we believe that the GuardNN architecture can be extended to support dynamic pruning. However, dynamic pruning will introduce new side channels through memory accesses and timing, and may require additional protection against side-channel attacks.

Application to Other Accelerators – While this paper focuses on building a secure DNN accelerator, we believe that the key insights from this study are also applicable to other application-specific accelerators. For example, GuardNN shows how the size of the TCB can be reduced and confidentiality-only protection can be provided without the overhead of integrity protection by leveraging the application-specific instruction set of an accelerator. GuardNN also shows that both security and performance can be improved by customizing protection based on the application-specific characteristics, such as memory access patterns, of an accelerator. As case studies, we studied applying the application-specific memory protection scheme to an H.264 video decoder [45], [46], the Darwin genome assembly accelerator [47], and vertex-centric graph accelerators [48], [49], [50], [51] based on open-source RTL implementations. We found that the proposed VN generation approach can be applied to all three types of accelerators to minimize performance overhead of memory protection.

VIII. RELATED WORK

Privacy-Preserving Deep Learning – GuardNN provides hardware-based protection for DNN inference and training in an untrusted environment. Alternatively, fully homomorphic encryption (FHE) can provide stronger protection by performing all computations in an encrypted format. While FHE algorithms provide strong cryptographic guarantees without trusting any remote hardware or software, they come with significant overhead [52], [53]. Recent studies [54], [55] show the overhead for DNN inference by optimizing linear operations. However, cryptographic solutions are still multiple orders of magnitude slower than the baseline with no protection. GuardNN provides a design point that provides hardware-based security with much lower performance overhead.

TEEs [4], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25] provide hardware-protected execution environments where confidentiality and integrity are ensured even under an untrusted OS or physical attacks. Recent proposals use the secure enclave directly [56], [57] or extend the enclave with a secure GPU accelerator [58] to enable remote DNN computations with strong privacy and integrity guarantees. GuardNN extends the high-level TEE approach to DNN accelerators and shows that secure accelerators have a potential to provide both higher performance and higher security compared to the general-purpose platforms by customizing its architecture and protection for a specific application.

Memory Encryption and Integrity Verification – Recent designs for memory encryption [59], [60] use the counter-mode with smaller VNs to optimize memory encryption. For integrity verification, recent efforts [31], [61], [62], [63] propose counter-based integrity-tree design to reduce the performance overhead. Morphable counters [64] further reduce the overhead by compressing the counters. Another line of research attempts to optimize the integrity tree traversal. Prior works propose to store the VNs in the last-level cache to exploit the locality [30], [65] and reduce the latency of integrity verification by predicting VNs or using unverified VNs speculatively [66], [67], [68]. The application-specific memory protection in GuardNN is built on the previous memory protection schemes but customized for DNN accelerators. The application-specific memory
protection leverages the characteristics of DNN accelerators to remove off-chip VNs, and significantly reduces the performance overhead compared to the state-of-the-art.

**Side-channel Attacks and Protection** – A variety of side-channel attacks have been shown to work against DNN accelerators. Memory and timing side-channels have been used to infer the underlying network structure of an accelerator with encrypted weights [69], [70]. GuardNN has a fixed memory access pattern and execution time, and is is secure against memory and timing side-channels. GuardNN needs additional countermeasures when dynamic pruning is used, or when other physical side-channels are considered. ORAM [71], [72], [73] offers a strong security guarantee for memory accesses with high overhead. Physical side-channel attacks on DNNs have been also recently exploited. A power side-channel attack has been used to retrieve the input image from a DNN accelerator [74]. Electromagnetic side-channel emanations have been used to recover the entire network topology including weights, albeit on a microcontroller-based inference engine [75].

**IX. Conclusion**

In this paper, we propose a secure DNN accelerator, named GuardNN, with a particular focus on enabling privacy-preserving ML. We discuss the architecture, interface, and implementation of GuardNN in detail. Our FPGA prototype shows that the GuardNN accelerator only adds less than 2% performance overhead on multiple DNN models.
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