Effective dc- link voltage variation for renewable power application

G. Maheswaran¹, M. Ettappan², T. Kavitha³  R. Senthil Kumar⁴
¹Centre for Energy Research, Chennai Institute of Technology, Chennai, India.
²Centre for Energy Research, Chennai Institute of Technology, Chennai, India.
³Department of Electrical and Electronics Engineering, VelTech Rangarajan Dr.Sagunthala R & D Institute of Science and Technology, Chennai, India.
⁴Department of Electrical and Electronics Engineering, Saveetha Engineering College, Thandalam, Chennai, India.

Email Id: ¹mageshdeepakkumar@gmail.com, ²ettappanm@gmail.com, ³drkavitha@veltech.edu.in, ⁴senthilkumar@saveetha.ac.in

Abstract. The proposed method analysis the effective utilization of dc-link voltage for a Multi-Level Converter by controlling the sequential operation of switching devices as per the load requirement. Here a different switching pattern is followed, where the number of switching devices are switched ON depending on the value of input voltage needed for the inverter, thereby unnecessary switching ON of all devices are avoided. Initial DC needed voltage is generated from renewable voltage source. The proposal also quotes on various application of these switching pattern in the field of renewable energy and voltage back-up systems where voltage generated is utilized with minimal switching losses. This Varied DC link voltage method by Selective Switch Count (SSC) is used in Voltage Source Inverter. Simulation using MATLAB is used to validate the proposed SSC method feasibility.

1. Introduction

Growing usage of conventional sources energy and its resultant environmental effect have a huge necessity to switch over to non-conventional resources in possible applications because of their abundant availability in nature as well as their non-polluting nature. In this proposal, voltage is obtained through set of photo voltaic panels which is viewed as one potential energy source for balancing the varying energy demand. Various other forms of energy sources like wind, hybrid renewable energy system, battery storage system etc. can be used as potential energy sources [1]. In the method considered here, Photo Voltaic (PV) panels already in operation enhanced by MPPT system [2] charges the batteries of SSC-MLC from which various voltages are obtained by proper selection of switches (sw₁ to sw₄).

Switching losses contribute for major share of total inverter losses that too at higher switching frequencies. If needed to reduce the switching losses, optimization of the switching frequency has to be done, which is not a preferable method under variable load conditions. Other parameter which decides the
switching losses are magnitude of DC link voltage \( v_{dc} \) and current value \( I \) [3]. From the below power loss equation (4) it can be understood that, if the magnitude of \( V_{dc} \) is keep as per the load voltage requirement unnecessary switching losses can be reduced.

Instantaneous voltage \( i(t) \) and current \( i(t) \) during turn on time \( t_{on}(on) \) are

\[
v(t) = v_{dc} - (v_{dc} - v_{on}) \left( \frac{t}{t_{on}} \right); \quad 0 < t \leq t_{on}(on)
\]

\[
i(t) = I_{dc} \cdot \frac{t}{t_{on}}; \quad 0 < t \leq t_{on}(on)
\]

For switching frequency \( (Fs) \), average switching loss during the instant of each turn on/off is given by the equation 3 and equation 4

\[
P_{c,on} = \left( \frac{V_{dc \cdot 1dc}}{T_s} \cdot \frac{t_{on}}{T_s} \right) + \left( \frac{V_{on \cdot 1dc}}{T_s} \cdot \frac{t_{on}}{T_s} \right)
\]

\[
P_{c,off} = \left( \frac{V_{dc \cdot 1dc}}{T_s} \cdot \frac{t_{off}}{T_s} \right) - \left( \frac{V_{on \cdot 1dc}}{T_s} \cdot \frac{t_{off}}{T_s} \right)
\]

\[
P_{sw} = \frac{1}{6} \cdot V_{dc} \cdot I_{dc} \cdot \frac{t_{on} + t_{off}}{T_s} + \frac{1}{3} \cdot V_{on} \cdot I_{dc} \cdot \frac{t_{on} + t_{off}}{T_s} \quad \text{----------(5)}
\]

The main purpose and application of this research work is to prove that, reducing the dc-link voltage \( (V_{dc}) \) to a lower value (by varying switch count as per the load voltage requirement) has many advantages like, minimized voltage-stress across inverter switches thereby increases the life of the switching device, switching losses gets reduced and THD of the inverted voltage reduces.

One potential application of the proposed method can be used in real power balancing during night time by delivering the maximum voltage it has stored by solar harvesting. In day time instead of delivering the full voltage charged during day light, reduced voltage is delivered as per the load requirement from this SSC method. The inverter circuit is the used to converts the variable dc voltage in to alternating quantity on requirement.

2. Voltage for Multi Level Converter from Proposed Selective Switch Count Method

In most existing methodologies of VSI, dc-link voltage is adjust ed to be fixed value \( (2V_{pcc}) \) for any loading points[4]. In actual practice, the value of required dc-link voltage is less during the non loaded time, but if a fixed dc-link voltage is utilized it may increase unnecessary device switching and switching losses that too even at decreased load. Alternatively if variable dc-link voltage is used in proportional to the load magnitude, the voltage stress on the Voltage Source Inverter (VSI) switches reduces thereby reducing the switching losses. The operation of this SSC method and the resultant dc-link voltage \( (V_{dc}) \) obtained as per the load requirement is discussed in detail with the aid of Figure 1.

The maximum dc-link voltage \( (V_{dc \cdot max}) \) considered here is twice the value of PCC voltage [3]. The dc-link voltage and the corresponding switches that are made to operate in SSC method is shown in Table. 1.
Figure 1. Selective Switching Device Converter

Table 1. DC-link voltages with respect to selective switching devices for a multi level converter

| Ranges of $V^{*}_{dc}$ in MLC | Operating switches | DC-link voltage ($V_{dc}$) |
|-------------------------------|--------------------|----------------------------|
| $< V_{dc\ min}$              | sw2, w4            | Vb1                        |
| $V1 - V2$                    | sw1(d2), sw4       | Vb1+Vb2*d2                 |
| $V2 - V3$                    | sw1, sw4           | Vb1+Vb2                    |
| $V3 - V4$                    | sw1, sw3(d1)       | Vb3*d1+ Vb1+Vb2            |
| $V4 - V5$                    | sw1, sw3(d2)       | Vb3*d2+ Vb1+Vb2            |
| $V5 - V_{dc\ max}$          | sw1, sw3           | Vb1+Vb2+Vb3                |

The levels of ($V_{dc}$) is divided evenly from $V_{dc\ min}$ to $V_{dc\ max}$. During every subsequent switching, the increment voltage in step ($V_{dc}$) is obtained as shown in Figure 2.
Figure 2. Variation of DC-link voltage with switching sequence variation

Hence, various voltages are obtained in steps such as \( V_{dc\ min} \), \( V_{dc\ min} + V_{dc} \), \( V_{dc\ min} + 2V_{dc} \), ..., \( V_{dc\ max} \) based on load voltage requirement. This SSC method is basically a type of buck-converter, where input voltage is stepped down with respect to its duty cycle. Here, the duty cycle \( d_1 = \frac{1}{3} \) and \( d_2 = \frac{2}{3} \) are selected to maintain equal voltage value between \( V_{dc\ min} \) to \( V_{dc\ max} \) by using the desired increment \( V_{dc} \). Here, \( V_{dc\ min} \) is same as the voltage across battery \( V_{b1} \) and \( V_{dc\ max} \) is the summation of voltage across the batteries \( V_{b1}, V_{b2}, \) and \( V_{b3} \).

For example:

(a) \( V_{dc\ min} = V_{b1} \) is obtained by switching ON \( sw_2 \) and \( sw_4 \) permanently,
(b) \( V_{dc\ min} + V_{dc} = V_{b1} + V_{b2} \) \( * d_1 \) is obtained when \( sw_4 \) ON and operating \( sw_1 \) with duty cycles \( d_1 \) and \( d_2 \).
(c) \( V_{dc\ min} + 2V_{dc} = V_{b1} + V_{b2} \) \( * d_2 \) when \( V_{dc\ max} \), \( sw_1 \) and \( sw_3 \) are permanently ON.

The change in variable dc voltage \( \Delta V_{dc} \) is given in equation (6)

\[
\Delta V_{dc} = \frac{V_{dc\ max} - V_{dc\ min}}{6}
\]

Duty cycles \( d_1, d_2 \) are calculated and gate pulses are generated by saw tooth step PWM technique as shown in Fig. 3(a) and Fig. 3(b). Gate pulse is obtained by comparing carrier signal \( c(t) \) with modulating signal \( m(t) \), and in case of \( c(t) \) being greater than \( m(t) \), gate pulse is taken to be ON (i.e: \( ton \) is present), else gate pulse is considered to be in OFF state.

Figure 3. Saw tooth-step PWM technique
Duration of ton period is varied by varying modulating signal magnitude as given by equation (7). Hence, on varying carrier signal frequency both ton and T changes, thereby duty cycle is maintained at same value. Hence for duty cycle d1= 1/3, ton=1/3, the calculated value from equation (7) is h=4/3.

\[ \frac{h}{T-\tau_{on}} = \frac{2}{T} \]

------- (7)

where, T corresponds to total time period of pulse, h corresponds to modulating signal magnitude, duty cycle d of the operation switches is given by d = ton /T.

Example, for modulating signal magnitudes of h= 4/3 and h = 2/3, d1 is 1/3 and d2 is 2/3. With switches sw1 to sw4 in operation, various output values can be attained with larger flexibility. So, the objective of attaining reduced switching losses at VSI during low voltage requirement condition can be obtained by reduced dc-link voltage. In this methodology, six dc voltage levels obtained because of decreased switching devices is shown in Table 1. Figure 4 shows the complete MATLAB simulation circuit design which includes decreased switching devices count (DC side) and inverter topology.

In this analyzed method, SSC-MLC regulates dc-link voltage leading to minimization of switching losses and unnecessary voltage stress on VSI switches at reduced load as well as at low voltage requirement condition.

![Schematic diagram of Selective Switch Count MLC – Inverter simulation Circuit](image)

Figure 4. Schematic diagram of Selective Switch Count MLC – Inverter simulation Circuit
3. Designing of SSC-MLC parameters

3.1. DC-link inductor (Ldc) design:
The dc link inductor is vital for eliminating current ripples and smooth voltage variations. From the basic buck converter [5], the value of Ldc is designed based on maximum current ∆IL,max, and switching frequency fsw.

\[ \Delta I_{L,max} = \frac{V_{b2} \text{ or } V_{b3}}{4L_{dc}f_{sw}} \] \hspace{1cm} (8)

In this paper, Vb2 = 75 V, fsw = 10 kHz, ∆I_L,max = 0.3 A. On substituting these values, the value of Ldc = 0.062 mH.

3.2. Design of Capacitors
For eliminating SSC output voltage ripples, dc-link capacitor Cdc plays a major role. The maximum voltage ripple ∆Vo;max across dc-link capacitor for the buck converter is given by equation (9),

\[ \Delta V_{o,max} = \frac{V_{dc}}{2L_{dc}C_{dc}f_{sw}^2} \] \hspace{1cm} (9)

For effective performance, allowable ripple voltage considered is 4% of Vc. On substituting the values in equation (10) Cdc of 0.28 µF is obtained. The capacitors C1, C2 and C3 shown in Fig.4 are connected in parallel to the respective voltage sources. Thus by effective selection of Cdc and capacitors C1, C2 and C3, voltage ripples at the SSC output can be eliminated in addition with battery charging when connected in parallel. Design of these capacitors C1, C2 and C3 depend on voltage rating, current and charge q where q=CVc, Vc is rated voltage across capacitor.

So,

\[ I_{c} = \frac{C\Delta V_{c}}{\Delta t} \] \hspace{1cm} (10)

where IC = capacitor current, ∆V_C = voltage across C, ∆t = 1/fsw. and on substituting the terms, the following expression is obtained.

\[ C = \frac{I_{c}}{f_{sw}\Delta V_{c}} \] \hspace{1cm} (11)

Here, the capacitors C1, C2 and C3 are connected across PV panels of rated output voltages (Vc) 100 V, 75 V and 100 V respectively. Here, ∆V_C = 4% of Vc, Ic = 0.5 A and fsw = 10 Kilo Hz are considered. On substituting the above values, capacitor parameters obtained are C1=2.07 µF, C2=6.24 µF and C3=2.07 µF.

4. Simulation Studies and Analysis
The switching sequence as proposed in Table I for the given schematic diagrams shown in Figure 1 and 4 is done in Matlab Simulink software. Detailed analysis and feasibility of the SSC variable DC link voltages obtained are used as the VSI input.
Figure 5(a) and 5(b). DC link voltage $V_{dc}$ and Inverter Voltage at $V_A$ if $V_{dc} = V_b1 + V_b2 + V_b3 \cdot d1$

Figure 6(a) and 6(b). Load current and Inverter Voltage of a VSI for $V_{dc} = V_b1 + V_b3 \cdot d1$
Figure 7. Vdc link voltage at $V_{dc} = V_{b1} + V_{b2} + V_{b3}$ and corresponding VSI phase voltage $V_A$, $V_B$, $V_C$ of VSI

The output so obtained from the VSI are shown in Figure 5(a), 5(b), 6(a), 6(b) and 7 shows the VSI output for its corresponding DC link voltage. Power loss calculated and THD obtained from VSI are tabulated in Table 2. Simulation results confirms that the proposed method of SSC operation on the converter side will reduce the stress and switching losses at the switches of the inverter side. Numerical data’s from Table 2 also confirms that, as the magnitude of DC link voltage increases switching losses also increases.

Table 2. THD and switching losses of a VSI with SSC DC link voltage

| DC link voltage $V_{dc}$ | Phase A | Phase B | Phase C | Total switching losses (mJ) |
|--------------------------|---------|---------|---------|-----------------------------|
| $V_{b1}$                 | 3.31    | 3.63    | 3.28    | 9.72                        |
| $V_{b1} + V_{b2}*d2$     | 7.87    | 8.02    | 8.31    | 11.84                       |
| $V_{b1} + V_{b2}$        | 16.01   | 16.27   | 16.56   | 13.42                       |
| $V_{b1} + V_{b2} + V_{b3}*d1$ | 19.17  | 19.69  | 19.89  | 19.74                       |
| $V_{b1} + V_{b2} + V_{b3}*d2$ | 27.4  | 28.16  | 28.02  | 27.60                       |
| $V_{b1} + V_{b2} + V_{b3}$ | 41.4  | 44.60  | 42.14  | 34.65                       |

Another important implication is that, as the level of voltage and switching losses increases, THD level also increases considerably as shown in Figure 8.
5. Conclusion
A method discussed here regulates the dc-link voltage obtained from renewable energy resource using SSC-MLC. In this SSC method, PV panels are used to generate and store DC voltage in batteries, from which required voltage as per the AC load can be utilized from the converter side. It can be observed that switching losses and THD level reduces in proportion to the level of DC link voltage. In terms of design flexibility, this method using SSC-MLC have many advantages like, simple control techniques, lesser voltage stress and losses at switches. Overall this method will increases the effective usage of renewable energy generated due to this SSC flexible switching pattern.

References

[1] Kalidoss R, Bora A, Natraj V, Jayaraman S V, Sivalingam Y 2021 Self-powered, rapid-response, and highly flexible nanosensors in Micro and NanoTechnologies, Elsevierm, 397-415. doi: 10.1016/B978-0-12-823358-0.00020-4.
[2] Sera D, Mathe L Kerekes, Spataru and Teodorescu R 2013 On the Perturb-and-Observe and Incremental Conductance MPPT Methods for PV Systems IEEE Journal of. Photo volt 3 1070-78.
[3] Mishra M K. and Karthikeyan K 2019 An Investigation on Design and Switching Dynamics of a Voltage Source Inverter to Compensate Unbalanced and Nonlinear Loads IEEE Trans. Ind. Electronics 56 2802-10.
[4] Gupta K K, Ranjan A, Bhatnagar P, Sahu L K and Jain 2016 Multilevel Inverter Topologies With Reduced Device Count: A Review IEEE Trans. Power Electronics 31 135-51.
[5] Wang L, Prokhorov A V 2017 Dynamic Stability Analysis of a Hybrid Wave and Photovoltaic Power Generation System Integrated Into a Distribution Power Grid IEEE Trans. Sustain. Energy 8 404-13.
[6] Varma R K and Salehi R 2017 SSR Mitigation With a New Control of PV Solar Farm as
STATCOM (PV-STATCOM) *IEEE Trans. Sustain. Energy* 8 1473-83.

[7] Maheswaran Gopalswamy, Mohana Sundaram, and Siddappa Naidu 2017 SSR Oscillations Mitigation in TCSC Series Compensated Power System Using ANFIS Controller *Journal of Advanced Research in Dynamical and Control Systems* 6 879-890.

[8] Senthilkumar R and Maheswaran G Modeling of Closed Loop ZVS Double Boost DC-DC Converter 2020 *Test Engineering and Management* 82 3082 – 92.

[9] Danalakshmi, Ettappan M, Prathiba S, Mohan Krishna D 2021 Reparation of Voltage Disturbance Using PR Controller Based DVR In Modern Power Systems Production Engineering Archives 27 16-29.

[10] Ettappan M, Vimala V, Ramesh S Thiruppathy Kesavan V 2020 Optimal reactive power dispatchfor real power loss minimization and voltage stability enhancement using Artificial Bee Colony Algorithm *Microprocessors and Microsystems* 76 085.

[11] Rashid M H 2014 *Power Electronics: Circuits, Devices and Applications*  Pearson USA.