SIGNED: A Challenge-Response Based Interrogation Scheme for Simultaneous Watermarking and Trojan Detection

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ABSTRACT
The emergence of distributed manufacturing ecosystems for electronic hardware involving untrusted parties has given rise to diverse trust issues. In particular, IP piracy, overproduction, and hardware Trojan attacks pose significant threats to digital design manufacturers. Watermarking has been one of the solutions employed by the semiconductor industry to overcome many of the trust issues. However, current watermarking techniques have low coverage, incur hardware overheads, and are vulnerable to removal or tampering attacks. Additionally, these watermarks cannot detect Trojan implantation attacks where an adversary alters a design for malicious purposes. We address these issues in our framework called SIGNED: Secure Lightweight Watermarking Scheme for Digital Designs. SIGNED relies on a challenge-response protocol based interrogation scheme for generating the watermark. SIGNED identifies sensitive regions in the target netlist and samples them to form a compact signature that is representative of the functional and structural characteristics of a design. We show that this signature can be used to simultaneously verify, in a robust manner, the provenance of a design, as well as any malicious alterations to it at any stage during design process. We evaluate SIGNED on the ISCAS85 and ITC benchmark circuits and obtain a detection accuracy of 87.61\% even for modifications as low as 5-gates. We further demonstrate that SIGNED can benefit from integration with a logic locking solution, where it can achieve increased protection against removal/tampering attacks and incurs lower overhead through judicious reuse of the locking logic for watermark creation.

KEYWORDS
Hardware Security, Watermarking, Trojan Attacks, Logic Locking, CAD for Security, Challenge-Response Protocol

1 INTRODUCTION
The increasing complexity of modern Intellectual Property blocks has resulted in a globally distributed manufacturing ecosystem. Although this entails considerable economic benefits, it increases the risk of an untrusted intermediary gaining access to the circuit. This can potentially result in IP piracy, counterfeiting and overproduction. Another security concern is that the untrusted entity may be able to insert a hardware Trojan into the design - either by tampering with the foundry mask or through a third-party IP that is added to the design.

IP Watermarking is a promising solution employed by the EDA industry to overcome the challenges of IP piracy, counterfeiting and overproduction. The watermarking process involves the addition of a unique signature to the original design which would enable the IP vendor to verify the provenance of the device at any stage in the supply-chain. The unique signature is usually added by carefully modifying a specific property of the original design. For example, recent works \cite{1,7} have focused on either modifying the Finite State Machine (FSM) of the design or adding additional constraints during the EDA flow. However, a significant drawback of these techniques is the limited coverage offered by the watermarking scheme. That is, the watermarking techniques are unable to detect whether a part of the IP has been modified. Consequently, an adversary could tamper with the circuit by removing critical functionality or by implanting hardware Trojans. Trojans are malicious circuits introduced by an adversary into the original design. Existing watermarking schemes either fail to detect these Trojans (FSM-based techniques where the Trojan does not interfere with the control logic) or are modified by the Trojans and therefore cannot prove the authenticity of the circuit (Since now there is no way to distinguish between a modified circuit and a completely different circuit).

In order to address this issue, we propose SIGNED a Secure Lightweight Watermarking Scheme for Digital Designs. SIGNED is a hardware watermarking scheme that can detect hardware Trojans and malicious modifications while introducing low overheads. SIGNED can be utilized at any stage in the design transformation process. It takes the RTL netlist as input and identifies the nets in the design that have an high switching activity. SIGNED then uses specially crafted test vectors that toggle these selected nets, also termed as sensitive nets, and records their response. The test vectors and response are stored in a challenge-response database. During the authentication phase, the IP vendor uses the challenge vectors on the design in-order to verify the provenance of the IP, to detect malicious modifications, or to detect the presence of Trojans. Unlike other watermarking schemes, even if the Trojan interferes with the watermark, we are still able to prove that the original circuit has been modified because we use more than one challenge vector in the authentication phase. Figure 1a shows the watermark insertion process and Figure 1b highlights the authentication process. The major contributions of the paper can be summarized as follows:

1. It presents a novel watermarking technique termed as SIGNED for digital IP blocks that uses a challenge-response protocol based interrogation scheme and can be applied to the IP at any stage in the design transformation process for authentication and provenance analysis. The watermarks inserted by SIGNED are design transformation invariant, i.e., they remain intact when a design goes through transformation from register transfer level (RTL) to gate level to transistor and layout.
2. We demonstrate that our proposed watermarking is lightweight, exhibits high structural coverage by showing that it can detect changes made to any portion of the circuit with high probability.

3. We leverage the high coverage exhibited by SIGNED to show that we can also detect malicious alterations in the design or Trojan attacks at an untrusted facility (e.g., foundry). To the best of our knowledge, this is the first watermarking technique that is capable of simultaneously detecting Trojan attacks.

4. We also present possible integration of the proposed approach with any existing logic locking solution. While watermarking provides passive protection against IP piracy and helps with provenance analysis, logic locking provides active protection against piracy, reverse engineering and extraction of design secrets. By combining these two approaches, we achieve the benefits of both solutions towards comprehensive protection of hardware IPs, while also reducing overhead and strengthening each technique.

5. We have developed a prototype CAD tool for the SIGNED framework. We use the CAD tool to evaluate the effectiveness of SIGNED on ITC and ISCAS benchmarks. We show that the quality of the proposed watermarking, the coverage values of the internal nodes for Trojan detection, and hardware overheads obtained for these benchmark designs are highly promising.

The rest of this manuscript is organized as follows: Section 2 describes the SIGNED framework in detail. Section 3 presents our experimental set-up and evaluation results. Section 4 describes previous related work. Finally, we conclude the paper in Section 5.

2 THE SIGNED FRAMEWORK

SIGNED consists of two major steps - watermark insertion and design authentication. Watermark authentication is performed on the RTL netlist and happens in the design house. On the other hand, design authentication is performed in the field in order to verify ownership and authenticity of the design. As shown in Figure 1, the watermark insertion process can be split up into three separate components, namely sensitive net selection, digest logic insertion and challenge vector generation. We will now explain each of these with the help of Algorithm 1 and Figure 2.

Algorithm 1: Sensitive Net Selection

| Line | Description |
|------|-------------|
| 1    | \( R_C \leftarrow \text{set of random test vectors for circuit } C \) |
| 2    | \( S \leftarrow \emptyset \) |
| 3    | Initialize circuit to a default value |
| 4    | foreach \( R^*_C \in R \) do |
| 5    | apply \( R^*_C \) on \( C \) |
| 6    | foreach edge \( e^*_C \in C \) do |
| 7    | store the value of \( e^*_C \) for \( R^*_C \) |
| 8    | end |
| 9    | end |
| 10   | \( T^C \leftarrow \text{transition matrix with } e^*_C \text{ columns and } R^*_C \text{ rows} \) |
| 11   | \( D_{ij} \leftarrow \text{EuclideanDistance}(T^C_{ij}, T^C_{ij}) \) |
| 12   | Group nearby nets into a cluster \( K^*_C \) |
| 13   | \( K_C \leftarrow \text{nets partitioned into } K \text{ clusters based on } D_{ij} \) |
| 14   | foreach partition \( K^*_C \in K_C \) do |
| 15   | \( S \leftarrow \emptyset \) |
| 16   | \( K_{nj} \leftarrow \text{set of nets in } K^*_C \text{ based on parameter } p_{nj} \) |
| 17   | \( e^*_C \leftarrow \text{random}(K^*_C, \text{threshold}) \) |
| 18   | \( S \leftarrow S \cup K^*_C \) |
| 19   | end |
| 20   | return \( S \) |

Sensitive Net Selection: In order to identify the sensitive nets within the circuit, we first simulate the design with a large number of random test vectors (lines 3-9 in Algorithm 1). The transitions of the Boolean values of the nets in the design are stored in the Transition matrix \( T^C \). Next, we apply unsupervised learning techniques (K-means - lines 10 -13) to cluster the nets of the design based on their transitions in the Transition matrix. Nets that transition together i.e. undergo a change in their Boolean values in the same cycle are more likely to be in the same cluster. Once the \( K_C \) clusters of the Transition matrix have been formed, we select one representative net from each cluster based on the weighted combination of the switching activity and fan-in values of the nets (lines 15 - 18). In Figure 2a, the nets in the circuit are split up into two clusters and nets N11 and N19 are selected as the representative nets. The set of all representative nets together are called the sensitive nets.

Digest Creation Logic: After having selected the sensitive nets from the design (N11 and N19 in Figure 2b), we insert a compaction...
An effective watermark must possess the following properties:

1. **Cost**: The overheads introduced by the watermark should be acceptable for the use-case of the design.
2. **Immutability**: The various design transformations in the EDA flow must not affect the watermark.
3. **Undetectability**: The watermark should not be easily removable by an adversary, e.g., an untrusted foundry.
4. **Uniqueness**: An adversary should not be able to clone the watermark and insert it into an arbitrary IP.
5. **Verifiability**: A legitimate user should be able to verify the authenticity of the design.
6. **Coverage**: Even minute modifications (or Trojans) in the design should be captured by the watermark.
7. **Cost**: The overheads introduced by the watermark should be acceptable for the use-case of the design.

The second step of SIGNED i.e., design authentication, takes place in the field. The user verifies the provenance of the design by comparing the digest output with the digest output of the golden (fault-free) design when challenge vectors are applied.

### 3 EVALUATION

An effective watermark must posses the following properties: (1) **Immutability** - The various design transformations in the EDA flow must not affect the watermark; (2) **Undetectability** - The watermark should not be easily removable by an adversary, e.g., an untrusted foundry; (3) **Uniqueness** - An adversary should not be able to clone the watermark and insert it into an arbitrary IP; (4) **Verifiability** - A legitimate user should be able to easily verify the authenticity of the design; (5) **Coverage** - Even minute modifications (or Trojans) in the design should be captured by the watermark; (6) **Cost** - The overheads introduced by the watermark should be acceptable for the use-case of the design. We now present the results of SIGNED on the ISCAS and ITC benchmarks and evaluate our watermarking scheme with reference to the above criteria.

SIGNED is capable of detecting malicious modifications in circuits even when the number of gates modified is less than 0.1% of the total gate count. Figure 3 shows the performance of SIGNED on a subset of the ITC benchmark. We observe that even when the percentage of gates modified is below 0.1% of the total gate count, SIGNED is able to detect the modifications more than 80% of the time. We would also like to highlight that when the percentage of gates modified is increased to 0.5%, SIGNED is able to detect the modification every single time.

The detection accuracy of SIGNED can be tuned using two parameters (knobs) - i) Size of the digest and ii) Number of challenge response pairs. Increasing the size of the digest allows us to capture more information about the circuit and therefore detect a greater number of malicious modifications or Trojans. Similarly, increasing the number of challenge vectors increases the probability of a modification or Trojan causing a mismatch in the Boolean values of the sensitive nets. Therefore, both of these parameters are directly proportional to the detection accuracy. Figure 4 clearly shows the dependence of the detection accuracy on the number of challenge vectors applied.

As discussed in Section 2, SIGNED has two major steps viz, watermark insertion and watermark verification. Watermark verification is performed in-field, and under resource-constrained scenarios. Due to the sensitive and time critical nature of this process, it would be beneficial for the designer if they were provided with information regarding the nature of the malicious modification in the design. Figure 5 shows the relation between the size of the malicious modification and the number of mismatched bits in the digest. We observe that the degree of mismatch in digest bits is a reliable indicator of the number of gates that have been modified. For example, we observe that a modification as low as 5-bits produces a mismatch on one digest output for a 4-bit digest size. Thus, the designer can rely on the degree of change in the digest outputs to estimate the amount of modification.

The results above clearly show that SIGNED satisfies the coverage criteria mentioned at the beginning of the section. It should also be noted that since SIGNED relies upon the stored golden responses to authenticate a circuit, it cannot be inserted into an arbitrary IP by an adversary (uniqueness property). Also, since the watermark does not change the functionality or usage of the design, the verification process is completely transparent to the end-user (easy verifiability).
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Figure 3: Detection Accuracy vs Number of Modified Gates

Figure 4: Detection Accuracy vs Number of Challenge Vectors

Table 1: Table showing overheads for different benchmarks after 4-bit watermark insertion

| Benchmark | Before SIGNED | After SIGNED |
|-----------|---------------|--------------|
| Gate Count | Area | Power | Delay | Gate Count | Area | Power | Delay |
| c5415 | 1176 | 55.16 | 22.3 | 3.23 | 1204 | 57.63 | 22.7 | 5.29 |
| b20 | 1267 | 67.62 | 32.1 | 6.63 | 1339 | 61.54 | 30.0 | 9.66 |
| b11 | 7220 | 394.86 | 6.2 | 8.55 | 7248 | 397.35 | 6.2 | 8.55 |
| b17 | 2487 | 136.0 | 14.0 | 10.24 | 24797 | 1217.28 | 14.0 | 10.24 |
| b19 | 2487 | 136.0 | 14.0 | 10.24 | 24797 | 1217.28 | 14.0 | 10.24 |
| b19 | 9015 | 495.17 | 35.8 | 11.84 | 90185 | 495.10 | 35.9 | 11.84 |
| b20 | 11546 | 618.70 | 10.8 | 8.96 | 11494 | 621.39 | 10.8 | 8.97 |
| b21 | 8882 | 387.44 | 12.2 | 12.29 | 88683 | 387.91 | 12.4 | 12.48 |
| b22 | 16655 | 887.17 | 14.4 | 13.33 | 16683 | 889.66 | 14.4 | 12.56 |

3.1 Overhead analysis

SIGNED modifies the design by injecting additional circuitry in order to enhance the security of the IP. However, a significant overhead in terms of delay or area would render it unsuitable for low-resource domains. Hence, it is important to quantify the overheads of our proposed technique. We evaluate the impact of SIGNED-based watermarking on ISCAS85 and ITC benchmarks. The results for the largest benchmarks (>1000 gates) are presented in 1. We observe that SIGNED has negligible impact on the overall area, power and delay of the circuits, meaning that it also successfully satisfies the cost criteria.

3.2 Security Analysis

Although SIGNED is able to overcome tampering and Trojan insertion, it is still susceptible to removal attacks. In order to overcome this, we can combine our watermark insertion scheme with logic locking and consequently prevent reverse-engineering and removal attacks. SIGNED and logic locking will complement and strengthen each other.

4 RELATED WORK

Existing IP watermarking techniques can be categorized into two distinct types based on the medium in which the watermark is embedded [1, 7]. Constraint-based watermarking methods [1, 3, 4, 6] or FSM-based watermarking techniques [2, 8, 10]. In constraint-based watermarking, the IP owner first creates a message that proves his ownership over the design. This message is then transformed into constraints for one specific phase of the IC design flow [6] and supplied to the EDA tool. The resulting design therefore carries the watermark through these constraints. On the other hand, in FSM based watermarking the watermark is embedded in the unused transitions of the state transition graph. Traversing the embedded sequence allows the designer to prove ownership of the design. However, these methods fail to meet the aforementioned properties of a robust watermarking technique. In particular, they cannot be easily verified by the consumer and can often be easily removed or circumvented by malicious actors. Moreover, they are unable to detect hardware Trojans or malicious modifications in the design. Therefore, there is a need for a robust watermarking scheme that detects tampering and meets the criteria delineated above. As we have shown in the previous sections, SIGNED satisfies all the properties needed for a robust watermark and is also capable of detecting hardware Trojans. We provide a qualitative comparison of SIGNED with other recent watermarking schemes in Table 2.

Table 2: Table comparing the different state-of-the-art watermarking schemes based on the level at which they are implemented, detectability, Transparency (Change in functional behaviour), and Coverage

| Work | Level | Type | Security | Transparency | Coverage | Overheads |
|------|-------|------|----------|--------------|----------|-----------|
| [5]  | Behavioural | Constraint | Medium | High | Medium | Medium |
| [4]  | Physical | Constraint | Medium | High | Medium | High |
| [1]  | Physical | Constraint | Medium | High | Small | High |
| [6]  | Architectural | Constraint | Medium | High | Medium | Medium |
| [8]  | Physical | FSM | Low | High | Small | High |

Data: Architectural, CRP | High | High | High | Low

Figure 5: Percentage change in Digest bits vs Num. of Modifications
5 CONCLUSION

IP Watermarking has emerged as a promising candidate for protection of semiconductor Intellectual Properties against a range of security threats. In this paper, we have introduced a novel challenge-response based IP watermarking scheme that is sensitive to extremely small modifications in the design. We insert the watermark by analyzing the structural properties of the design and achieve a high detection accuracy across multiple benchmarks. We also qualitatively compare SIGNED with other recent watermarking approaches and evaluate it for the area, power and timing overheads. We show that such a scheme not only provides robust IP authentication and provenance analysis capability, but it also entails reliable detection of malicious alterations or Trojan attacks.

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