An Area Efficient and High Speed EBCOT for JPEG2000 Using Cadence EDA Tools

V Srinivasa Rao¹, Rajesh K Panakala², Rajesh Kumar Pullakura³

¹Dept of ECE, SVECW, Bhimavaram, AP, India, ²Dept of ECE, PVPSIT, Vijayawada, AP, India, ³Dept of ECE, AUCE, Visakhapatnam, AP, India

Abstract: JPEG2000 is a very effective system to perform the compression of an image. With JPEG2000, the better quality of an image can be obtained after the reconstruction. Extended Block Coding with an Optimized Truncation (EBCOT) is a key component in the JPEG2000. EBCOT consisting of Context modeling and the Coder. The improved EBCOT architecture has been implemented with Cadence EDA Environment. The results obtained with the improved EBCOT architecture is proved to be better compared with the existing architectures. The improved EBCOT algorithm consumes 20% less area and operates at a faster speed compared with the existing results when implemented on Cadence EDA tools.

Keywords: Image Compression, EBCOT, JPEG2000, CADENCE EDA.

1. INTRODUCTION

Nowadays JPEG2000 codec is an alternative to JPEG in image compression. For the applications like Digital cinema, Medical Imaging and Satellite Images JPEG2000 play an important role for the compression of images and for the storage purposes. In JPEG2000, EBCOT[2][4] is an important subsystem for the coding of the data coming from discrete wavelet transforms (DWT). The DWT converts an image into wavelet coefficients and the coefficients are represented in time and frequency domain. The DWT coefficients are quantized and the quantized coefficients are needed to be encoded by EBCOT block. The EBCOT consisting of Context modeling and the MQ coder. The context modeling generates (CX,D) pairs. CX stands for Context and D stands for the decision. The output of a EBCOT is a bit stream in encoding form. Embedded Block Coding operates on block samples.

In order to meet the real-time requirement, high speed EBCOT architecture [6][9] must be designed carefully. Current hardware implementations of JPEG and JPEG2000 codec mostly target maximizing speed performance so as to achieve real time behavior even when compressing image with very high resolutions. The experimental results shows that CADENCE EDA results proved to be better compared to other backend implementation results. The improved EBCOT architecture consumes relatively smaller area and operates at higher speed.
compared with the existing architectures [4][6]. Section II explains about the improved architecture, section III covering the details about the implementation, section IV gives the details about the results and finally section V concluded the paper.

2. PROPOSED ARCHITECTURE

A. Extended Block Coding with Optimized Truncation (EBCOT)

The block diagram of a improved EBCOT system architecture of JPEG2000 is shown in fig 1. EBCOT [2] is another wavelet-based coding algorithm that has the capability of embedding many advanced features in a single bit stream while exhibiting state-of-the-art compression performance. Due to its excellent features, efficient implementation complexity and excellent compression performance, the EBCOT algorithm has been adopted in the evolving new still image coding standard.

![Fig1.Block Diagram of JPEG2000 System](image)

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B. EBCOT ALGORITHM

The JPEG 2000 system consisting of three main components; the DWT, Quantization, and the EBCOT coder as seen in Figure 2. The DWT transforming the pixels of an image into time and frequency representation. The coefficients produced by DWT are represented in sign and magnitude representation. The EBCOT consisting of code blocks in sign and magnitude representation, context modeler and coder. The MQ coder is a context-based adaptive binary arithmetic unit. CxD pairs generated by BPC are fed to the MQ coder.
The EBCOT algorithm performs the bit plane coding in 3 non overlapping passes and generates the context and data bit pair, which are applied to the BPC coder. A high-speed parallel bit-plane coding (BPC) hardware architecture for the EBCOT module in JPEG 2000 is improved and implemented. EBCOT comprises of two tiers. In Tier-1, image samples are compressed using context modeling and arithmetic coding. Obtained bit-stream is formatted and truncated in Tier-2. In this work, we introduced an efficient and high-speed VLSI hardware architecture design of context formation for EBCOT tier-1.

The embedded block coder is also known as Tier-1 coder. The bit-plane coder is the first block of the EBCOT algorithm. The BPC generates context-symbol pairs on the basis of quantization indices grouped in code-blocks. Input data has been read in the sign magnitude form and analyzed bit-plane wise, starting from the most significant bit plane (MSB) with a non-zero element to the least significant bit-plane (LSB). Each bit-plane is scanned in three coding passes called significance propagation, magnitude refinement, and cleanup. Each pass provides a variable quality contribution to the reconstructed image.

The Improved Block Diagram of EBCOT is shown in fig 3. The bit plane coder generates CX,D pairs. These pairs are stored in FIFO. Meanwhile mean square error (MSE) can be calculated for the output produced by BPC. The BPC output has been applied to MQ (BAC) coder. The CX,D pairs are stored in SRAM. The memory controller selects a magnitude and sign bit plane to be encoded. The state memories are implemented using dual port RAM. The architecture mainly consists of code block status memory, context bit modeling, context FIFO, arithmetic coder and bit-stream memory in a sequential fashion. The input to the coprocessor is a code block status buffer and the outputs are compressed code streams. The context-window comprises of two parts. The first part processes all samples that are coded by pass 1 and pass 2 in column C, and the second part processes the rest samples coded by pass 3 in column C table to shift left one column to be coded in column D table.
Fig 3. Improved Architecture for EBCOT

entropy coding consists of Context Modeling. In context modeling the code-block data has been arranged in order, to first encode the bits which contribute to the largest distortion reduction for the smallest increase in file size. the fractional biplane coding (EBCOT) produces a sequence of symbols, pairs of context and decision (CX, D), in each coding pass. The context-based adaptive binary arithmetic MQ-coder that is used in JPEG2000 standard to encode these symbols. The block diagram representation of MQ coder is shown in fig 4. The MQ coder performs entropy coding and produces embedded bit stream.

Fig 4. MQ Encoder top level block diagram

Algorithm for block coding process

1. Assume we are in block k, and c(i,j) is a coefficient in block k.
2. Perform Division on c(i,j) into its sign s(i,j) and m(i,j) its magnitude.
3. Perform Quantization in the quantization step for block k.
4. Indicate the first non zero bit of v(m,n)
5. Indicate the magnitude refinement coding has been applied to v(m,n)
6. if D = 0 then
7. if MPS(CX) = 0 then
8. return SPP
9. else
10. return MRP
11. end if
12. else
13. if MPS(CX) = 1 then
14. return cleanup
15. else
16. return MRP
17. end if
18. end if
19. for all coefficients in the code block do
20. compute context of the current sample
21. if sample is insignificant and has a non-zero context then
22. send the bit and context to arithmetic encoder
23. if bit is 1 then call ENCODE SIGN to encode sign of the coefficient
24. end if
25. end if
26. end

3. IMPLEMENTATION

A. CADENCE VIRTUOSO
The proposed algorithm implemented using Cadence Virtuoso Schematic and Layout Editor. The improved architecture was implemented in Cadence 6-L. The EBCOT algorithm was also developed using verilog language to validate the architecture by comparison with the hardware behavioral.

Cadence Virtuoso integrates analog layouts with block placements. Cadence Virtuoso produces schematic and layout for the improved architecture. The proposed method increases the speed of the EBCOT algorithm is mainly due to the minimization of the number of memory access by adopting efficient memory architecture to store the state variables and the code block data. The system level architecture has been developed and validated using Verilog language. The implementation of the EBCOT tier-1 encoder successfully passed all functional tests on real image data using the simulation tools. Cadence Affirma Spectre Circuit Simulator tools are used to simulate and synthesize the verilog codes into gate level codes.

These gate level codes are then placed and routed to a 90nm environment using cadence IC station. It is worth noting that synthesized maximum achievable clock frequency is of 112GHz for the current implementation technology and Verilog code. It takes around 0.36 million cycles in simulations to compress a 256*256 grayscale image.

B. CADENCE EDA TOOLS FLOW

Fig 5. indicates the various steps in Cadence design flow. In the initial step the entire design created in schematic window. The second step analyzes and estimates the amount of resistances and capacitances in the design. After analyzing the design successfully then a layout can be created to know about the area details occupied by the design. Finally verification can be done by performing design rule checks and Layout vs schematic check.
C. CADENCE EDA DESCRIPTION

Cadence is a major provider of EDA and semiconductor IP. It also offers design and verification IP for memories, interface protocols, analog/mixed-signal components, and specialized processors. And reaching up to the systems level, It also provides hardware/software co-development platforms. The cadence synthesizer generates placement and minimized version of the design. In cadence environment the design can be done using an HDL. EDA software is a computer-aided design and engineering software specifically geared towards the design automation of electronic systems. The on-chip power consumption of the simulated circuit is obtained from Cadence Analog Artist Mixed Signal simulation tools. The power consumption obtained after synthesis for the EBCOT tier-1 system as 92uw.

4. RESULTS

Simulation and synthesis results of BPC and BAC(MQ Coder) design are discussed under this subsection. This section also discusses important control signal associated with BPC and BAC with waveforms using cadence L version. The simulation waveform for BPC Coder in EBCOT is shown in fig 6.
The simulation waveforms for context modeling (CX) produced by BPC coder using cadence simulator is shown in fig 8.

The generated results using CADENCE EDA are depicted in the table 1.

| Parameter     | Cadence EDA(Proposed) | Existing Architecture [6] |
|---------------|------------------------|----------------------------|
| Power         | 92uw                   | 125mW                      |
| Speed         | 100ns                  | 189ns                      |
| Area(cells)   | 125um²                 | 185um²                     |

The obtained results compared with existing architectures and are shown in Table 2.

| Parameter     | Existing Architecture[4] | Proposed |
|---------------|--------------------------|----------|
| Gates         | 8560                     | 6892     |
Performance (clock frequency) | 82GHz | 112GHz
---|---|---

5. Conclusion

Thus the paper presents the implementation of an area efficient and high speed EBCOT architecture using CADENCE EDA tools on a back end process. The increase in speed and reduction of the size of architecture is useful to achieve rapid data transfer over the internet or through channels. Hence, this high speed and area efficient EBCOT employed in different applications such as medical images, Satellite images and others which require high speed transmission. Thus the improved design can achieve increase in throughput, reduces the memory size and memory access with minimal increase in hardware.

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V.Srinivasa Rao, working as Assoc.Prof at SVECW, Bhimavaram, AP, India. Currently pursuing Ph.D at JNTU Kakinada. He done his M.Tech at JNTU Anantapur and B.Tech at JNTU Kakinada. His areas of interest are VLSI Design and Image Processing. He Published various papers in different journals and conferences.
Rajesh K Panakala working as Prof and HOD at PVPSIT, Vijayawada, AP, India. He was awarded Ph.D from IIT Chennai in the area of VLSI and Robotics. He done his masters from Osmania University, Hyderabad and Bachelors from VR Sidhartha Engg College, Vijayawada. He published various papers in reputed journals like IEEE, Elsevier. His areas of interests are VLSI, Robotics and Image processing.

Rajesh Kumar Pullakura working as Prof and HOD at AU College of Engineering, Visakhapatnam. He was awarded Ph.D from AU College of Engineering. He has done ME from AU and Bachelors degree from CBIT, Hyderabad. He published various papers in international conferences and journals. His areas of interests are radar signal processing.