**TeleHammer: A Stealthy Cross-Boundary Rowhammer Technique**

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**Abstract**—Rowhammer exploits frequently access specific DRAM rows (i.e., hammer rows) to induce bit flips in their adjacent rows (i.e., victim rows), thus allowing an attacker to gain the privilege escalation or steal the private data. A key requirement of all such attacks is that an attacker must have access to at least part of a hammer row adjacent to sensitive victim rows. We refer to these rowhammer attacks as PeriHammer. The state-of-the-art software-only defenses against PeriHammer attacks is to make such hammer rows inaccessible to the attacker.

In this paper, we question the necessity of the above requirement and propose a new class of rowhammer attacks, termed as TeleHammer. It is a paradigm shift in rowhammer attacks since it crosses memory boundary to stealthily rowhammer an inaccessible row by virtue of freeloading inherent features of modern hardware and/or software. We propose a generic model to rigorously formalize the necessary conditions to initiate TeleHammer and PeriHammer, respectively. Compared to PeriHammer, TeleHammer can defeat the advanced software-only defenses, stealthy in hiding itself and hard to mitigate.

To demonstrate the practicality of TeleHammer and its advantages, we have created a TeleHammer’s instance, called PThammer, which leverages the address-translation feature of modern processors. We observe that a memory access can induce a fetch of a Level-1 page-table entry (PTE) from memory and thus cause hammering the PTE once. To achieve a high hammer-frequency, we flush relevant TLB and cache efficiently and effectively. To this end, PThammer can cross user-kernel boundary to rowhammer rows occupied by Level-1 PTEs and induce bit flips in adjacent victim rows that also host Level-1 PTEs. We have exploited PThammer to defeat advanced software-only defenses in bare-metal systems.

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**I. INTRODUCTION**

In 2014, Kim et al. \([18]\) discovered an infamous software-induced hardware fault, the so-called “rowhammer” bug. In particular, frequent accessing the same addresses in two DRAM (Dynamic Random Access Memory) rows (i.e., hammer rows) can cause bit flips in an adjacent row (i.e., a victim row). If sensitive structures, such as page tables, are placed onto the victim row, an adversary can corrupt the structures by exploiting adjacent hammer rows although she has no access to the structures. As such, the bug is able to break MMU-based memory isolation between different security domains without any software vulnerabilities, thus enabling a powerful class of attacks targeting DRAM-based systems. The attacks are so hazardous that they can either gain the privilege escalation \([35], [12], [5], [8], [34], [11], [35], [37]\) or steal the private data \([32], [8], [21]\). To utilize the rowhammer bug, all existing rowhammer attacks require an access to at least a part of an exploitable hammer row (a hammer row is only exploitable when it is adjacent to sensitive victim rows \([33]\) or one part of it is sensitive \([21]\) as shown in Figure 1. As their access to the hammer row is legitimate and within memory boundary, we term such attacks as PeriHammer. To defeat PeriHammer based attacks, numerous hardware and software-based mitigation techniques have been proposed. As hardware-based mitigation require DRAM updates or upgrade and cannot be backported, recent software-only defenses including CATT \([6]\), CTA \([36]\) and RIP-RH \([4]\) are practical for bare-metal systems and target different rowhammer attacks. These defenses in common enforce DRAM-based memory isolation at different granularity to prevent exploitable hammer rows from being accessed by attackers. Take CATT \([6]\) as an example, it isolates DRAM memory of kernel domain with guarding rows such that all exploitable hammer rows that induce bit flips in kernel structures belong to kernel domain. Our contributions: we introduce a paradigm shift in rowhammer attacks through a new class of rowhammer attacks, called
TeleHammer (shown in Figure 1). It freeloads a chain of built-in features (e.g., out-of-order execution) of modern hardware and/or software to hammer inaccessible rows through a benign entity. It thus essentially eliminates the above requirement necessary to PeriHammer and make it possible again to break the above advanced defenses.

To rigorously formalize the necessary requirements to initiate TeleHammer, we propose a generic formal model, which can also formalize PeriHammer. The model indicates that PeriHammer is a special case of TeleHammer, and TeleHammer exhibits the following advantages over PeriHammer.

- TeleHammer can defeat the advanced software-only defenses, since it eschews the critical requirement of PeriHammer.
- TeleHammer is stealthy, since it hammers a hammer row not by itself but using a benign entity, making it hard to trace the real culprit.
- TeleHammer is hard to be mitigated, since abundant instances can be derived by its design. A countermeasure against specific instances cannot defeat TeleHammer.

To demonstrate the practicality of TeleHammer, we create a working instance, called PThammer, that satisfies the formal requirements of TeleHammer. Specifically, we observe that a memory access triggers the address translation in modern OSes on x86-84 microarchitecture. In response to the memory access, the processor first searches Translation-lookaside Buffer (TLB) to check if a corresponding physical address exists. If the search fails (i.e., a TLB miss), then the processor searches paging structure that hosts a partial address mapping of different page-table levels [2]. If another miss occurs, it fetches four-level page-table entries (PTEs) from CPU cache, otherwise DRAM memory. Fetching PTEs from memory causes hammering the PTEs once. Although PTEs reside in the kernel space and are inaccessible to users, PThammer can cross user-kernel boundary to hammer them by freeloading the address-translation feature.

In order to trigger exploitable rowhammer bit flips, PThammer targets Level-1 PTEs and needs to effectively and efficiently flush the address mapping from TLB and Level-1 PTE from cache. However, it is not authorized to perform such flushes by the means of instructions. PThammer instead constructs a minimal eviction set for TLB and cache, respectively. By doing so, PThammer can implicitly flush any target entry from TLB and memory line from cache, resulting in subsequent memory access hammering Level-1 PTEs. On top of that, PThammer forces Level-1 PTE allocation to span over hammer and victim rows so as to induce bit flips in PTEs and gain kernel privilege. By performing stealthy cross-memory-boundary hammer, PThammer not only crosses the user-kernel boundary but also defeats all the aforementioned practical defenses (we will talk about how to compromise the defenses in Section IV).

The main contributions of this paper are as follows:

- All previous rowhammer exploits (i.e., PeriHammer) require access permissions to an exploitable hammer row. In contrast, we propose a new class of rowhammer attacks, called TeleHammer, that eschews this critical requirement.
- We present a generic model to formally define necessary conditions to launch TeleHammer and PeriHammer, respectively. Based on the model, we summarize three advantages of TeleHammer over PeriHammer.
- We propose an instance of TeleHammer, called PThammer, that leverages the address-translation feature of modern processors to hammer page tables and defeat the advanced software-only defenses in bare-metal systems.

The rest of the paper is structured as follows. In Section II we briefly introduce the background information and summarize related works. In Section III we present a formal model of TeleHammer and talk about how to instantiate TeleHammer in detail. Section IV evaluates PThammer thoroughly. In Section V we discuss how to compromise ZebRAN [20], a defense for virtualization systems, shed light on other possible instances of TeleHammer and discuss possible mitigation against TeleHammer and PThammer. We conclude this paper in Section VI.

II. BACKGROUND AND RELATED WORK

A. CPU Cache

In commodity Intel x86 micro-architecture platforms, there are three levels of CPU caches. Among all levels of caches, the first level of cache (i.e., L1 cache) is closest to CPU. L1 cache has two types of caches, i.e., L1D caching data and L1I caching instructions. The second level of cache, L2, is unified caching both data and instructions. Similar to L2, the last-level cache (LLC) or L3, is also unified. Generally speaking, cache of a specific level is set-associative and it consists of S sets. Each set contains L lines and data or code can be cached in any line of the set; this is referred as a L-way set-associative cache set. For each cache line, it stores B bytes. Thus, the overall cache size of that level will be S × L × B. As L1 and L2 are private to a physical core and LLC is shared among all cores, LLC cache is first partitioned into slices and one slice serves one core with a higher priority. For each slice, it is further divided into cache sets as mentioned above.

When an accessed variable is stored in a cache set, Intel micro-architectures use its virtual or physical address to decide its corresponding cache set of a specific cache level. For instance, L1 cache set is indexed using bits 6 to 11 of a virtual address. For L3, its indexing scheme is more complicated. In contrast to L1 and L2 that are private to a physical core, L3 is shared among all cores. So L3 cache is firstly partitioned into slices, and one slice serves one core with a higher priority. For each slice, it is further divided into cache sets as mentioned above. As such, some physical-address bits are XORed to decide a slice, and some bits (bits 6 to 16) are XORed to index a cache set [25].

B. Translation-lookaside Buffer

Translation Lookaside Buffer (TLB) has two levels. The first-level (i.e., L1), consists of two parts: one that caches translations for code pages, called L1 instruction TLB (L1
iTLB), and the other that caches translations for data pages, called L1 data TLB (L1 dTLB). The second level TLB (L2 sTLB) is larger and shared for translations of both code and data. Similar to the CPU cache above, the TLB at each level is also partitioned into sets and ways.

Note that a virtual address (VA) determines a TLB set of each level. Although there is no public information about the mapping between the VA and the TLB set, it has been reverse-engineered on quite a few Intel commodity platforms [10].

C. Address Translation

Memory Management Unit (MMU) enforces memory virtualization primarily by the means of paging mechanism. Paging on the x86-64 platform usually uses four levels of page tables to translate a virtual address to a physical address. As such, virtual-address bits are divided into 4 parts. The bits 39 to 47 are used to index a selected page directory pointer table (the base address of PDPT comes from the PML4 entry and the entry determines a physical page frame number and attributes (e.g., access rights) for access to the physical page). The bits 21~29 are used to index a selected page directory (PD) table (the base address of PD comes from the PDPT entry). The bits 12~20 are used to index a selected page table (the base address of PT comes from the PDPT entry). The bits 0~11 are the offset into that page.

In order to facilitate the process, TLB is introduced to cache the address translations while cache is involved to store the accessed data as well as the page table entries of all levels.

D. Dynamic Random-Access Memory

Main memory of most modern computers uses Dynamic Random-Access Memory (DRAM). Memory modules are usually produced in the form of dual inline memory module, or DIMM, where both sides of the memory module have separate electrical contacts for memory chips. Each memory module is directly connected to the CPU’s memory controller through one of the two channels. Logically, each memory module consists of two ranks, corresponding to its two sides, and each rank consists of multiple banks. A bank is structured as arrays of memory cells with rows and columns.

Every cell of a bank stores one bit of data whose value depends on whether the cell is electrically charged or not. A row is a basic unit for memory access. Each access to a bank “opens” a row by transferring the data in all the cells of the row to the bank’s row buffer. This operation discharges all the cells of the row. To prevent data loss, the row buffer is then copied back into the cells, thus recharging the cells. Consecutive access to the same row will be fulfilled by the row buffer, while accessing another row will flush the row buffer.

E. Rowhammer Overview

Rowhammer bugs: Kim et al. [18] discovered that current DRAMs are vulnerable to disturbance errors induced by charge leakage. In particular, their experiments have shown that frequently opening the same row (i.e., hammering the row) can cause sufficient disturbance to a neighboring row and flip its bits without even accessing the neighboring row. Because the row buffer acts as a cache, another row in the same bank is accessed to flush the row buffer after each hammering so that the next hammering will re-open the hammered row, leading to bit flips of its neighboring row.

Hammering techniques: generally speaking, there are three techniques regarding hammering a vulnerable DRAM.

Double-sided hammer: two adjacent rows of a victim row are hammered simultaneously and the adjacent rows are called hammer rows [18].

Single-sided hammer: Seaborn et al. [33] proposed a single-sided hammering by randomly picking multiple addresses and just hammering them with the hope that such addresses are in different rows within the same bank.

One-location hammer: one-location hammering randomly selects a single address for hammering. It exploits the fact that advanced DRAM controllers employ a more sophisticated policy to optimize performance, preemptively closing accessed rows earlier than necessary.

Key requirements: the following requirements are needed by PeriHammer-based attacks to gain either privilege escalation or private information.

First, CPU cache must be either flushed or bypassed. It can be invalidated by instructions such as clflush on x86. In addition, conflicts in the cache can evict data from the cache since cache is much smaller than the main memory. Therefore, to evict hammer rows from the cache, we can use a crafted access pattern [13] to cause cache conflicts for hammer rows. Also, we can bypass the cache by accessing uncached memory.

Second, the row buffer must be cleared between consecutive hammering DRAM rows. Both double-sided and single-sided hammering explicitly perform alternate access to two or more rows within the same bank to clear the row buffer. One-location hammering relies on the memory controller to clear the row buffer.

Third, existing rowhammer attacks require that a hammer row be accessible to an attacker in order to gain the privilege escalation or steal the private data, such that a victim row can be compromised by hammering the hammer row.

Fourth, either the hammer row or the victim row must contain sensitive data objects (e.g., page tables) we target. If the victim row hosts the data objects, an attacker can either gain the privilege escalation or steal the private data [33], [3]. If the hammer row hosts the data objects, an attacker can steal the private data [21].

1) Rowhammer Attacks: In order to trigger rowhammer bug, frequent and direct memory access is a prerequisite. Thus, we classify rowhammer attacks into three categories based on how they flush or bypass cache.
**Instruction-based cache flush:** the `clflush` instruction is commonly used for explicit cache flush [18], [33], [11], [32] ever since Kim et al. [18] revealed the rowhammer bug. This instruction can flush all levels of cache entries related to a specific virtual address and it can be executed by an unprivileged process on the x86 architecture.

**Eviction-based cache flush:** alternatively, an attacker can evict a target address by accessing congruent memory addresses which are mapped to the same cache set and same cache slice as the target address [1], [13], [5], [25], [27]. A set of congruent memory addresses is called an eviction set. Our PThammer also applies the eviction-based approach to flush Level-1 PTEs from cache.

**Uncached Memory Access:** as direct memory access (DMA) memory is uncached, past works such as Throwhammer [34] and Netherhammer [23] on x86 microarchitecture and Drummer [35] on ARM platform have abused DMA memory for hammering. Note that although Throwhammer and Netherhammer appear to be similar to PThammer on the surface, unlike PThammer they can neither achieve the privilege escalation nor steal the private data. They can achieve the disturbances in the computer system and potentially achieve the denial of services.

### III. TeleHammer Overview

In this section, we first present the threat model and assumptions, and then introduce the formal model of TeleHammer, followed by an instance of TeleHammer to demonstrate its practicality.

**A. Threat Model and Assumptions**

Our threat model is similar to other rowhammer attacks [37], [32], [31], [5], [12], [33]. Specifically,

- The kernel is considered to be secure against software-only attacks. In other words, our attack does not rely on any software vulnerabilities.
- An adversary controls an unprivileged user process that has no privileges such as accessing `pagemap` that has the mapping between a virtual address and a physical address.
- An attacker has no knowledge about the kernel memory locations that are bit-flippable.
- The installed DRAM modules are susceptible to rowhammer-induced bit flips. Pessl et al. [30] report that many mainstream DRAM manufacturers have vulnerable DRAM modules, including DDR3 and DDR4 memory.

**B. Formal Modeling of TeleHammer**

We propose a formal model of TeleHammer to characterize its attack paradigm.

Let $U$ be a set of entities, which can be any component in modern OSes that is able to initiate memory accesses. If $u \in U$, then $u$ could be, for instance, an unprivileged attack process, processor, DMA controller and etc. A set of memory addresses is denoted by $M$. Each memory address has access permissions assigned to each entity. Given a memory address $m \in M$, the permission function $\Pi(m)$ returns a set of entities that can access $m$. That is, if $u \in \Pi(m)$, then $u$ has read/write/execute permissions to $m$.

Only in this model, memory refers to not only the DRAM memory row but also other types of high-speed memory (e.g., cache, register, DRAM row buffer, etc.). Generally, a memory access starts by searching the content in the fastest memory hardware first (e.g., registers). If the search fails, then it goes to other memory hardware such as the slowest DRAM memory row but also other types of high-speed memory (e.g., cache, register).

**Definition 1 (Directed Memory Graph).** A directed memory graph $G$ (e.g., Figure 2) is a pair $(M, E)$, where memory addresses in $M$ constitute the nodes of $G$, and $E$ contains all the directed edges. A directed edge in $E$ is represented by a quintuple such as $(m_a, u_1, m_1)$ in Figure 2 where $m_a$ and $m_1 \in M$, $u_1 \in U$, respectively. An edge $(m_a, u_1, m_1) \in E$ has the following semantics:

- $u_1 \in \Pi(m_1)$ and,
- an access to $m_a$ can potentially trigger $u_1$ to access $m_1$ within time $T_{\text{edge}}(m_a, u_1, m_1)$.

Note that the time $T_{\text{edge}}(m_a, u_1, m_1)$ is decided by $m_a$ triggering $u_1$ and then $u_1$ accessing $m_1$. As such, $T_{\text{edge}}(m_a, u_1, m_1)$ should be greater than $T_{\text{node}}(u_1, m_1)$ given the time taken by the trigger. Since memory addresses in this model have different memory types, there exist other edges starting from $m_a$ such as $(\tilde{m}_a, u_1, \tilde{m}_1)$. Which edge to access at runtime is highly dependent on the time taken by the edge. Intuitively, the edge that has a shorter time would have a higher chance to be selected. Take Level-1 cache as an example, it is shared between all the cores of the processor and partitioned into multiple slices (one for each core). Each core will choose to access its own slice rather than others since the time to access its own slice is faster.

To exploit the rowhammer bug, an attacker must hammer a node (e.g., $\tilde{m}_h$ in Figure 2) that is located in the DRAM row, rather than other nodes (e.g., $\tilde{m}_h$ in cache). As such, the attacker is supposed to select the edge $(m_n, u_h, \tilde{m}_h)$ at runtime and we call such edge a memory access edge.

**Definition 2 (Memory Access Edge).** An edge $(m_n, u_h, \tilde{m}_h)$ with $\nu(\tilde{m}_h) = 1$ is defined as a memory access edge, denoted by $(m_n, u_h, \tilde{m}_h)$ if $\nu(m_n, u_h, \tilde{m}_h) \in E$ ($\tilde{m}_h \neq m_h$) satisfies the following requirements:

- $\nu(\tilde{m}_h) = 0$ or,
- $T_{\text{edge}}(m_n, u_h, \tilde{m}_h) > T_{\text{edge}}(m_n, u_h, m_h)$. 


If $\mathcal{V}(\hat{m}_h) = 0$, such nodes are printed in a dashed circle in Figure 2 and they do not contain valid content. Thus, their edges will not be taken. Or if the edges (e.g., $(m_n, u_h, \hat{m}_h)$) take a longer time, then such edges will not be taken, either.

As such, the entity $u_h$ can specify the memory access to $m_h$ at runtime by setting $\mathcal{V}(\hat{m}_h) = 0$ if $T_{\text{edge}}(m_n, u_h, \hat{m}_h) < T_{\text{edge}}(m_n, u_h, m_h)$.

For instance, let $\hat{m}_h$ and $m_h$ be within the cache and DRAM row, respectively, which has the same valid data. If $u_h$ wants to hammer $m_h$ frequently to trigger rowhammer bug, it must specify access to $m_h$ every time it performs hammering. To this end, $u_h$ can invoke `ciflush` instruction to flush $\hat{m}_h$. Alternatively, $u_h$ can achieve the same goal by leveraging the cache eviction policy (1). (13)

However, if both $\hat{m}_h$ and $m_h$ store the same page-table entry while $u_h$ has no access permissions to them, it becomes quite challenging to set $\mathcal{V}(\hat{m}_h) = 0$. Besides, the time to set must be as low as possible, because hammering $m_h$ requires a high frequency. We use a function $T_{\text{set}}(m_h)$ to denote the time cost of specifying the access to $m_h$.

To overcome the aforementioned challenges, we need to build a minimal eviction set to evict the page-table entry from $\hat{m}_h$ and make $\mathcal{V}(\hat{m}_h) = 0$. When $\hat{m}_h$ is invalid, then an access to $m_a$ in Figure 2 can trigger subsequent accesses and will access $m_h$, thus building up a communication path. Formally, the communication path is defined below.

**Definition 3** (Communication Path). As shown in Figure 2, $m_1$ and $m_n \in M (n > 1)$. A communication path $P(m_1, m_n)$ is a sequence of memory access edges $(e_i, i \in [1, 2, ..., n - 1])$ such that $e_i = (m_i, u_{i+1}, m_{i+1})$ for $i \in [1, 2, ..., n - 1]$.

Given the path $P(m_1, m_n)$, we use $\lambda \text{ast}(P(m_1, m_n))$ to denote the last memory access edge in the path. Let $\hat{e} = \lambda \text{ast}(P(m_1, m_n))$. Then, $P(m_1, m_n)|\hat{e}$ means a subpath of $P(m_1, m_n)$ excluding $\hat{e}$; that is, the concatenation of $P(m_1, m_n)|\hat{e}$ and $e$ is $P(m_1, m_n)$. For path $P(m_1, m_n)$, its time latency is denoted by $T_p(P(m_1, m_n))$.

**Definition 4** (Communication Latency). Let $P(m_a, m_h)$ be a communication path, $\lambda \text{ast}(P(m_a, m_h)) = \hat{e}$, and $e' = (m_n, u_h, \hat{m}_h)$. Then, $T_p(P(m_a, m_h))$ is defined as:

- $T_p(P(m_a, m_h)) = T_{\text{edge}}(m_n, u_h, \hat{m}_h)$, if $P(m_a, m_h) = \hat{e}$,
- otherwise,

$$T_p(P(m_a, m_h)) = T_p(P(m_a, m_h)|\hat{e}) + T_{\text{edge}}(m_n, u_h, \hat{m}_h).$$

Note that when $P(m_a, m_h) = \hat{e}$, then $m_a$ and $m_n$ are the same node, i.e., $m_a = m_n$, such that $P(m_a, m_h)$ has only one memory access edge.

When a hammer row is being hammered, the rowhammer bug can badly affect either a victim row that is either the hammer row itself or a victim row that is multiple-row away (within the same DRAM bank) from the hammer row. (18). (37) As such, $R_{\text{max}}$ is given to indicate the maximum row distance between a hammer row and victim row. The DRAM row-index function $\text{Row}(m_h)$ returns the row index in DRAM if a node $m_h$ is within a DRAM row, or $-1$ otherwise.

As a minimum hammer frequency is needed to successfully hammer a DRAM row, we use $T_{\text{max}}$ to represent a required maximum time latency to hammer once.

Note that both $R_{\text{max}}$ and $T_{\text{max}}$ are decided not only by the DRAM module itself but also the rowhammer techniques (e.g., single-sided rowhammering).

Besides, a sensitivity function $S(m_v)$ returns 1 if $m_v$ contains critical information (e.g., a page table or a cryptographic key), otherwise 0. When $m_v = 1$ and it suffers from the rowhammer bug, it indicates that an attacker is able to gain privilege escalation, steal private data, etc.

To this end, the following defines the necessary conditions for a TeleHammer based exploit.

**Definition 5** (TeleHammer). Let $G$ be the directed memory graph of a computing task being conducted by an attack process $a$, exemplified in Figure 2 where $m_a$, $m_h$ and $m_v$ ($a \notin \Pi(m_v)$) represent an attack address, a hammer address and a victim address, respectively. $a$ can launch a TeleHammer-based exploit, if conditions below are satisfied:

- $\text{Row}(m_h) \neq -1, \text{Row}(m_v) \neq -1, S(m_v) = 1$,
- $|\text{Row}(m_h) - \text{Row}(m_v)| \leq R_{\text{max}}$,
- $\exists P(m_a, m_h)$ in $G$,
- $T_{\text{set}}(m_h) + T_{\text{node}}(a, m_a) + T_p(P(m_a, m_h)) + T_\delta \leq T_{\text{max}}$.

As shown in Figure 2, modern hardware expects to take the fastest path to handle the computing task for the attack process $a$, i.e., $P(m_a, m_h)$. However, the path must be changed to $P(m_a, m_h)$ so as to hammer $m_h$ by using $u_h$. As such, $a$ must set the nodes such as $\hat{m}_h$ to invalid, since $u_h$ accessing such nodes takes a shorter time. The time taken by the setting is $T_{\text{set}}(m_h)$. To successfully do hammering once, $a$ also need to consider the time by accessing $m_a$ (i.e., $T_{\text{node}}(a, m_a)$), the time by walking through the path $P(m_a, u_h, m_h)$ (i.e., $T_p(P(m_a, m_h))$) and the time $a$ has to wait to perform next hammering (i.e., $T_\delta$). Thus, the sum of all the aforementioned time cost should be no greater than $T_{\text{max}}$, as shown in the last condition.

When $m_a$ and $m_h$ refer to the same memory address, i.e., $m_a = m_h$, then TeleHammer has an access to $m_h$ and actually becomes PeriHammer. As such, we can also formally define PeriHammer below based on the above formal model.

**Definition 6** (PeriHammer). PeriHammer would succeed if the following conditions are met:

- $\text{Row}(m_h) \neq -1, \text{Row}(m_v) \neq -1, S(m_v) = 1$,
- $|\text{Row}(m_h) - \text{Row}(m_v)| \leq R_{\text{max}}$,
- $a \in \Pi(m_h)$,
- $T_{\text{set}}(m_h) + T_{\text{node}}(a, m_h) + T_\delta \leq T_{\text{max}}$.

Clearly, the last condition removes the latency caused by the path $P(m_a, m_h)$, making it faster to hammer once. Besides, it is much easier for $a$ to specify the access to $m_h$ other than other nodes and spend much less time compared to $a$ in TeleHammer as discussed in Definition 3-B.
A comparison of TeleHammer and PeriHammer: as shown in Figure 2 TeleHammer is effective against the rowhammer defenses where \( m_h \) is located in a physically isolated DRAM partition, since it requires no access to \( m_h \).

On top of that, TeleHammer is stealthy and hard to be traced by dynamic analysis at runtime, since it has a complicated communication path and can only hammer \( m_h \) by using \( u_h \). In contrast, an attacker via PeriHammer hammers \( m_h \) directly by herself.

Besides, mitigating TeleHammer is challenging due to abundant communication path candidates. TeleHammer can identify as many paths as possible by leveraging built-in features of modern hardware and/or software. Thus eliminating the communication path we have identified in the following sections essentially cannot defend against TeleHammer.

Clearly, TeleHammer is slower than PeriHammer by comparing their time condition in their respective definition, indicating that PeriHammer is faster in inducing bit flips.

To demonstrate the practicality of TeleHammer, we have created an instance of it, called PThammer. Besides, we discuss in detail about other possible instances in Section V.

C. PThammer: page-table based TeleHammer

PThammer is page-table based TeleHammer. It allows an unprivileged attacker to hammer page tables by exploiting a processor, resulting in bit flips in other page tables.

In the following, we discuss how PThammer exploit can satisfy the formal conditions specified in Definition 5.

1) How Satisfy Formal Definition 5 First, page tables are critical in memory isolation and are inaccessible to an unprivileged attacker. If the attacker can compromise a memory address hosting page tables by the rowhammer effect, then it satisfies the first condition; here, the address refers to \( m_v \) and \( S(m_v) = 1 \).

Second, page tables are common and can be widely distributed in modern OS kernels. Thus, both \( m_h \) and \( m_v \) can be kernel addresses hosting page tables, that is, hammering page tables of \( m_h \) will flip bits in page tables of \( m_v \). To this end, we can leverage previous works such as memory spray [7] and memory ambush [33] to force the kernel to create a large number of page-table pages, with the hope that some page tables are placed into hammer addresses like \( m_h \) while some are within victim addresses like \( m_v \). As such, we can create numerous pairs of such hammer addresses and victim addresses so that they become highly likely to induce exploitable bit flips in page tables. Note that the rowhammer defense (i.e., CTA [36]) allocates all page tables from a reserved memory partition and this will greatly increase the number of pairs compared to page-table allocation from the whole system memory.

Third, there exists a communication path (see Definition 5) that allows an attacker to indirectly access page tables. To this end, we observe that a least privileged memory triggers an address translation where the processor can access page tables from memory. When a user allocates a virtual memory page by malloc and then accesses the page for the first time, an address-translation process occurs. Within the process, the processor performs multi-level page-table walk, populates corresponding page-table entries (PTEs) and allocates a physical memory page for the user. To facilitate subsequent memory access as shown in Figure 3 Translation Look-aside Buffer (TLB) stores a complete address mapping from a virtual address to a physical address. Paging structure caches a partial address mapping of different page-table levels [2]. For instance, the paging structure of Level-2 PD translates a virtual address to a physical address of Level-1 PT. With bits 12~20 from the virtual address [15], a corresponding physical address of a Level-1 PTE can be obtained. CPU cache copies the accessed four-level PTEs from memory. By doing so, the processor will search these hardware structures in the order of priority to get a matching physical address. If TLB, paging structure and cache are all effectively flushed, the processor then has to access the four-level PTEs from memory. As such,
an access to an address $m_a$ by $a$ can trigger the processor to access four-level PTEs from memory if the flushing operation is conducted effectively.

**Last,** as $m_a$ can be within cache, the time ($T_{node}(a, m_a)$) to access it is negligible. To meet the time condition in the definition, the time ($T_p(P(m_a, m_h))$) to walk through the above identified path, the time ($T_{set}(m_h)$) to specify the path, and the time ($T_s$) to wait for next hammering must all be as low as possible.

**Optimize $T_p(P(m_a, m_h))$ and $T_s$:** We optimize the identified communication path by making $m_h$ host Level-1 PTE rather than other-level PTE, shown as a solid line with an arrow in Figure 3. The path is optimized for following reasons:

- flushing paging structure is required when $m_h$ hosts other-level PTE. Directly flushing paging structure requires executing a privileged instruction such as `invlpg`, while indirect flushing needs to reverse-engineer the mapping between a virtual address and the paging structure index.
- flushing all-level (or other single-level) PTEs from paging structure and cache is intuitively more time consuming compared to flushing Level-1 PTE, as shown in Figure 3.
- specifying such a path consumes much less memory, making the exploit stealthier. As mentioned above, we need to allocate a lot of page-table pages to flip exploitable bits in page tables. Creating a PT-level page of 512 entries requires exhausting 2MiB memory. For a higher page-table-level page, its creation requires much more memory. For example, the PD-level page creation requires 1GiB memory.
- compared to other-level PTEs, a bit flip in a Level-1 PTE is easier to become exploitable and gain privilege escalation, since the Level-1 PTE determines the physical memory address that a user can access.

As $m_h$ hosting Level-1 PTE is the last accessed memory address when translating a virtual address, it means that $T_s \approx 0$.

**Optimize $T_{set}(m_h)$:** To specify the path to the Level-1 PTE (shown in red solid line in Figure 3), we only need to flush the address mapping from TLB and the Level-1 PTE from cache with the PD-level paging structure still being effective.

Intuitively, we can simply invoke `invlpg` to flush the whole TLB. As for the cache flush, we can perform a page-table walk, get the virtual address of the Level-1 PTE and thus flush its valid content from cache by invoking `clflush`. By doing so, we are able to flush both TLB and cache as quickly as possible. However, kernel privilege is required to complete the flushing. Alternatively, we can perform the flushing indirectly by manipulating cache and TLB replacement states. As the size of TLB and cache is limited, we can simply create many pages as an eviction buffer and access those pages one by one so as to evict target TLB entry and cache line. Although this approach can effectively flush both TLB and cache, it does not reduce $T_{set}(m_h)$ to its minimum.

In a nutshell, the key challenge to minimize the time is to determine two minimum eviction sets so as to flush targeted TLB entry and cache line effectively and efficiently.

![Address Translation](image)

**Fig. 3: Address Translation.** A solid line with an arrow indicates the fastest communication path that PThammer identifies to hammer a Level-1 page-table entry (PTE). When specifying the path, PThammer only flushes TLB and cache while retains all-level paging structure effective. Note that PML4E, PDPT, PDE are other three-level PTE, respectively.

2) **Effective and Efficient TLB Flush:** As Gras et al. have revealed that there exists an explicit mapping between a virtual page number and multi-level TLB sets, we simply create an initial eviction set that contains multiple (physical) pages to flush a cached virtual address from TLB. One subset of the pages is congruent and mapped to a same L1 dTLB set while the other is congruent and mapped to a same L2 sTLB set if TLB applies a non-inclusive policy.

Take one of our test machines, Lenovo Thinkpad T420, as an example, both L1 dTLB and L2 sTLB have a 4-way set-associative for every TLB set and thus intuitively 8 (physical) pages are enough as an minimum eviction set to evict a target virtual address from TLB. Actually, when we create such an eviction set and then profile the access latency of a target virtual address, its latency remains quite unstable.

To collect finer-grained information on TLB misses induced by the target address, we develop a kernel module that applies Intel Performance Counters (PMCs) to monitor a certain performance event related to TLB misses, that is, `dtlb_load_misses` and `missCausesAWalk`. The experimental results show that TLB misses in both levels do not always occur during the aforementioned profiling operation, meaning that the target address has not been effectively evicted by the eviction set, and thereby rendering the TLB flush ineffective. This is probably because that the eviction policy on TLB is not true Least Recently Used (LRU).

**How Decide the Minimal Size for a TLB Eviction Set:** To this end, we propose a working Algorithm 1 that can decide a minimal size without knowing its eviction policy. Note that the minimal size is used to construct a minimal TLB eviction set in PThammer while PThammer itself does not use the algorithm.
Algorithm 1: Decide a minimal eviction-set size for TLB

```
1 Initially: target_addr is a page-aligned virtual address that needs its cached TLB entry flushed. A buffer (buf) is pre-allocated, size of which is decided by available TLB entries. A set (init_set) is initialized to empty. A unique number is assigned to data_marker.

2 Function profile_tlb_set(set)
3      target_addr ← data_marker
4      foreach page ∈ set do
5          page[0] ← data_marker
6      end
7      tlb_miss_num is decided by accessing target_addr.
8      return tlb_miss_num
9      foreach page ∈ buf do
10         if page and target_addr are in the same set then
11            page[0] ← data_marker
12            add page into init_set.
13         end
14      end
15      threshold ← profile_tlb_set(init_set)
16      for page ∈ init_set do
17         take one page out of init_set.
18         temp_tlb_miss ← profile_tlb_set(init_set)
19         if temp_tlb_miss < threshold then
20            put page back into init_set and break.
21         end
22      end
23 return the size of init_set
```

Specifically, line 2 to 8 defines a function profile_tlb_set that reports a TLB-miss number (tlb_miss_num) induced by accessing target_addr. Specifically, the function argument (i.e., set) is write-accessed (line 4-6) to flush the cached target_addr in TLB (line 3) and then tlb_miss_num of write-accessing target_addr is reported in line 7. Based on a pre-allocated buf, we select those all pages that are indexed to the same TLB set as the target_addr by leveraging the reverse engineered mapping in line 9-14. Note that the buf size is large enough to effectively flush any targeted virtual address and it is decided by the number of TLB entries that serve 4KiB-page translation if target_addr is allocated from a 4KiB-page list, otherwise, the number of TLB entries that support 2MiB or 1GiB should be involved. The selected pages are then populated and added into init_set as shown in line 10-13. It is necessary to populate the selected pages in order to trigger the address-translation feature and thus TLB will cache address mappings accordingly. In line 15, we can gain a threshold for effective TLB flushes. We then start to tailor the set to its minimum while retain its effectiveness in line 16-23.

3) Effective and Efficient Cache Flush: now we are going to flush a cached Level-1 PTE (L1PTE) that corresponds to a target virtual address. Considering that last-level cache (LLC) is inclusive, we target flushing the L1PTE from LLC such that the L1PTE will also be flushed out from both L1 and L2 caches (we thus use cache and LLC interchangeably in the following section). In contrast to TLB that is addressed by a virtual page-frame number, LLC is indexed by physical-address bits, the mapping between them has also been reverse engineered. Based on the mapping, we can intuitively create an eviction set consisting of many congruent memory lines (i.e., cache-line-aligned virtual addresses), which are mapped to the same cache slice and cache set as the L1PTE. On top of that, the eviction set can also be minimized in case where the eviction policy of LLC is not publicly documented.

How Decide the Minimal Size for a Cache Eviction Set: we extend the aforementioned kernel module to count the event of last-level cache misses (i.e., longest_lat_cache.miss) and have a similar algorithm to Algorithm 1 to decide the minimal size for a cache eviction set, namely, construct a large enough eviction set congruent as a target virtual address and gain a threshold of cache-miss number induced by accessing the target address, remove memory lines randomly from the set one by one and verify whether currently induced cache-miss number is less than the threshold. If yes, a minimal size can be determined. Note this this algorithm is also performed in an offline phase long before PThammer is launched.

Although the size of eviction-set is determined ahead of time, PThammer in our threat model cannot know the mapping between a virtual and a physical address, making it challenging to construct an eviction set for any target virtual address during its execution. Also, PThammer cannot obtain the L1PTE’s physical address, and thus it is difficult to learn the L1PTE’s exact location (e.g., cache set and cache slice) in LLC. To address the above two problems during the execution, PThammer first constructs a complete pool of eviction sets, which can be used to flush any target data object including the L1PTE. It then selects an eviction set from the pool to evict a target L1PTE without its cache location.

How Construct a Complete Pool of Cache Eviction Sets: the pool has a large enough number of eviction sets and each can be used to flush a memory line from a specific cache set within a cache slice. The size of each eviction set is the pre-determined minimum size. We implement the construction based on previous works.

If a target system enables superpage, a virtual address and its corresponding physical address have the same least significant 21 bits, indicating that if we know a virtual address from a pre-allocated super page, then its physical address bit 0~20 is leaked and thus we know the cache set index that the virtual address maps to (see Section II-A). The only unsolved is the cache slice index. Based on a past algorithm, we allocate a large enough memory buffer (e.g., twice the size of LLC), select memory lines from the buffer that have the same cache-set index and group them into different eviction sets, each for one cache slice.

If superpage is disabled, then only the least significant 12 bits (i.e., 4KiB-page offset) is shared between virtual and physical addresses and consequently we know a partial cache-set index (i.e., bits 6~11). As such, we utilize another previous work to group potentially congruent memory lines into a complete pool of individual eviction sets. Compared to
Algorithm 2: Select a minimal cache eviction set

Initially: a virtual page-aligned address (target_addr) is allocated and needs its L1PTE cache-line flushed. A complete pool of individual eviction sets (eviction_sets).

\( l1pte_offset \) is decided by the page offset of target_addr. max_latency is initialized to 0 and indicates the maximum latency induced by accessing target_addr. max_set represents the eviction set used for the L1PTE cache flush.

Function profile eviction set(set, target)

foreach memory_line \( \in \) set do
| read-access memory_line.
end
flush a target TLB entry.
latency is decided by accessing target.
return latency

foreach set \( \in \) eviction_sets do
| obtain page offsetY from first memory line in set.
if page offsetY == l1pte offsetY then
| latency \( \leftarrow \) profile eviction set(set, target_addr).
if max_latency < latency then
| max_latency = latency.
| max_set = set.
end
end
return max_set

discuss the above grouping operation, this grouping process is much slower, since there are many more memory lines sharing the same partial cache-set bits rather than complete bits.

How Select a Target Cache Eviction Set: After completing the pool construction, we develop an Algorithm 2 to select an eviction set from the pool and evict a L1PTE corresponding to a target address.

In line 9, we enumerate all the eviction sets in the pool and then collect those sets that have the same page offset as the L1PTE in line 11. This collect policy is based on an interesting property of the cache. Oren et al. [29] report that if there are two different physical memory pages that their first memory lines are mapped to the same cache set of LLC, then the rest memory lines of the two pages also share (different) cache sets. This means if we request many (physical) memory lines that have the same page offset as the L1PTE and access each memory line, then we can flush the L1PTE from LLC.

After the selection, line 12-16 will select the target eviction set from the collected ones. In line 12, we profile every selected eviction set through a predefined function from line 2-8. Within this function, we perform read access to each memory line of one eviction set, which will implicitly flush the L1PTE from cache if the eviction set is congruent with the L1PTE, and then flush the target TLB entry related to target_addr to make sure the subsequent address translation will access the L1PTE. At last, we measure the latency induced by accessing target_addr. Based on this function, we can find the targeted eviction set that causes the maximum latency in line 13-16, as fetching the L1PTE from DRAM is time-consuming when accessing target_addr triggers the address translation in line 7. Given that cache is shared between page-}

| System Setting | Evic. Pool Construct | Evic. Set Select |
|----------------|----------------------|------------------|
| superpage enabled | 11millisec 0.3min | 1microsec 285millisec |
| superpage disabled | 11millisec 18min | 1microsec 283millisec |

TABLE I: Time costs for eviction pool construction and eviction set selection. Note that we perform the pool construction only once at the beginning of PThammer and then select TLB and cache eviction sets to perform double-sided rowhammer.

table entries and user data, we must carefully set target_addr to page-aligned, that is, its page offset is 0 and different from the L1PTE. As such, they are placed into different cache sets and the selected eviction set is ensured to flush the target L1PTE rather than target_addr.

IV. Evaluation

In this section, we test PThammer on Lenovo Thinkpad T420 with Intel i5-2540M and Samsung 8GiB DDR3 memory. The operating system running above is Ubuntu 16.04 LTS for x86-64 and has a Linux kernel of 4.8.0-generic. By default, the system disables the superpage feature. No matter whether the feature is enabled, we can observe the first cross-boundary bit flips on the test machine within an hour. As a case, we then leverage PThammer to compromise the state-of-the-art rowhammer defenses with the default system setting.

A. PThammer

We first decide the minimal eviction-set size to effectively and efficiently flush TLB and last-level cache (LLC) at an offline stage. Based on the pre-determined size, we can dynamically construct a minimal TLB or LLC eviction set from a complete pool of TLB or LLC eviction sets, and corresponding time costs are presented in Table I.

1) Decide Respective Minimal Eviction-Set Size: Based on the Algorithm [1] in Section III-C2, we first obtain an initial eviction set where its page number is twice the number of both L1dTLB and L2sTLB wayness and each page is mapped to the same L1dTLB set or L2sTLB set as a target page-aligned virtual address. We then remove one page from the set each time to check a TLB miss rate of the target virtual address, as shown in Figure 4a. As we can see from the Figure, the TLB miss rate initially remains quite stable (nearly 100%) when the eviction-set size drops down by one until 12, and thereafter decreases dramatically. Clearly, 12 ought to be the minimal size.

For LLC, out test machine has 12-wayness of LLC and each initial eviction set is set to have 24 memory lines that map to the same LLC set as a target virtual address. Similar to TLB, memory lines in the eviction set are also removed one by one and the LLC miss rate for each removal is shown in Figure 4c. Clearly, the LLC miss rate on each machine remains quite stable (i.e., almost 100%) until the set size of 16, but decreases gradually below 90% after 12. For the sake
of effectiveness and efficiency, we choose 12 as the minimal size and are able to induce bit flips using PThammer.

2) Prepare Respective Minimal Eviction Set: As mentioned in Section III-C2 and Section III-C3, preparing a minimal eviction set for either TLB or LLC consists of a complete pool construction and target eviction set selection and corresponding time costs are displayed in Table I.

For TLB, we allocate a complete pool of 4KiB pages and its page number is twice the number of both L1dTLB and L2sTLB entries that support a 4KiB-page, since we target a virtual address that requires four-level page-table. As can be see from the table, its construction and selection in both settings are fast.

For LLC, we construct a complete pool of either 2MiB pages (superpage enabled) or 4KiB pages (superpage) and its size in both settings are twice the size of LLC. As the cache-set bits in the 2MiB setting are known, the eviction pool construction is much faster (0.3 minutes) compared to that (18 minutes) in the 4KiB setting. The number of eviction sets in each pool is almost the same as the LLC set-number, making their selection efficiency similar to each other.

3) Double-sided PThammer: As mentioned in Section III-C, the time cost for each hammer must be no greater than the maximum latency allowed to induce bit flips. Given that double-sided hammer is the most efficient way to flip bits, we first determine the maximum latency of the machine by applying a previously published tool

The tool embeds the clflush instructions inside one round of double-sided hammer, which is the most efficient (costs only around 300 cycles) and effective (cache miss rate per one round is 100%) way to flush the CPU caches. In order to increase the time cost for each round of hammer, we add a certain number of NOP instructions that precede the clflush instructions and produce the result in Figure 5. As shown in the Figure, the time until the first bit flip to occur grows gradually until the time per hammer increases to around 1100 cycles and thereafter increases significantly before the hammer cost reaches 1500. We cannot observe any bit flip within 3 hours when the cost increases a bit from 1500 and thus we use 1500 as the maximum cost permitted to flip bits.

We then check whether the time cost for each hammer meets the allowed latency. For each double-sided PThammer, it requires accessing two user virtual addresses as well as their respective TLB eviction set (i.e., 24 virtual addresses) and cache eviction set (i.e., 24 virtual addresses). In both system settings, we conduct double-sided PThammer for a thousand rounds and measure the time that each round takes. The results show that the time taken of every round is in the range of \{650, 860\}, which is much less than the maximum latency and also
To defend against rowhammer attacks, numerous software-only defenses have been proposed. Among the software-based defenses, CATT [6], CTA [36] and RIP-RH [4] are practical to mitigate existing rowhammer attacks in bare-metal systems. Note that RIP-RH [4] enforces DRAM-based process isolation and thus prevents attackers from hammering target user processes. However, it does not protect the kernel and its page tables. Clearly, PThammer can defeat it by inducing rowhammer bit flips in a Level-1 PTE and gain kernel privilege. In this section, we demonstrate proof-of-concept attacks against CATT [6] and CTA [36] respectively in the default system setting.

**Compromise CATT [6]:** CATT [6] partitions each DRAM bank into a kernel part and a user part. These two parts are separated by at least one unused row. When physical memory request is initiated, CATT allocates memory from either the kernel part or the user part according to the intended use of the memory. By doing so, CATT can confine bit-flips induced by the user domain to its own partition and thereby prevent rowhammer attacks from affecting the kernel domain, the so-called physical kernel isolation.

Essentially, CATT can prevent some of PeriHammer based rowhammer attacks from positioning attacker-accessible memory adjacent to vulnerable but critical kernel memory. However, we are still able to indirectly hammer kernel memory from the user domain by leveraging PThammer and thus induce exploitable bit flips in the page table entries. It mainly consists of the following four steps:

1. Rely on past works [7], [35], [21] to allocate consecutive DRAM rows for page-table pages;
2. Perform double-sided PThammer by using a pair of selected user virtual addresses;
3. Verify whether “exploitable” bit flips have occurred by checking if a virtual address points to a page-table page. If not, go to step 2 to restart PThammer;
4. If yes, we have gained the kernel privilege and we can gain the root privilege by changing uid of current process to 0.

**Compromise CTA [36]:** the latest software defense is CTA (i.e., Cell-Type-Aware) [36], which focuses on PTE-based privilege escalation rowhammer attacks. In such attacks, all the attackers induce bit-flips in Level-1 page table entries (PTEs) such that the induced PTEs no longer point to the attackers’ memory pages but instead point to other page-table pages of the same process, thereby gaining illegal access to the page tables. In order to destroy this core property, CTA proposes CTA memory allocation and places Level-1 page tables in DRAM true-cells above a “Low Water Mark” in the physical memory. If a PTE has a bit-flip in its physical frame number, it only points to a physical address lower than the “Low Water Mark” rather than the page-table region.

By leveraging PThammer, we can break CTA and gain the root privilege. The key steps for the exploit are listed below:

1. We spray the physical memory under the “Low Water Mark” with a large enough number of security critical structures, i.e., cred (note that cred stores the critical uid field.). To this end, the attack process creates 32K child processes by invoking the fork system call. For each child process creation, the kernel is forced to allocate a kernel stack and multiple kernel structures including cred.
2. Inside each child process, it firstly registers a signal and then goes to sleep. The registered signal will help the attack process wake up the child process when necessary.
3. After completing the child-process creations, the attack process starts to occupy consecutive DRAM rows above the “Low Water Mark” by forcing page-table page allocations.
4. The attack process performs double-sided PThammer;
5. The attack process verifies whether “exploitable” bit flips have occurred by checking if a virtual address (VA) points to cred structure page. As the cred contains three user

| System Setting | Run # | Hammer Cost Until First Flip | Total Cost |
|----------------|-------|-----------------------------|------------|
| superpage enabled | run 1 | 8min | 9min |
|                 | run 2 | 17min | 18min |
|                 | run 3 | 4min | 5min |
| averaged cost   | all runs | 10min | 11min |
| superpage disabled | run 1 | 10min | 29min |
|                 | run 2 | 15min | 33min |
|                 | run 3 | 6min | 25min |
| averaged cost   | all runs | 10min | 30min |

TABLE II: Time costs of double-sided PThammer for three runs on each system setting. On average, both settings can observe the first bit flip within 10 minutes of hammer and complete PThammer within 30 minutes.
ids (e.g., $uid$ and $suid$) and three group ids (e.g., $gid$ and $sgid$) stored sequentially, the attack process can construct a unique string of the six ids and compare the string to the VA-pointing page. If the pointed page does not contain the string, then go to the step 4 to restart PThammer;

6) If yes, the attack process has located a cred structure, changes $uid$ to 0 and then wakes up every child process by delivering the registered signal. Inside the signal-catching function, each child process can check whether it has become a root process by invoking $getuid$.

V. DISCUSSION

Defeat ZebRAM [20]: ZebRAM is a rowhammer defense but only works for a virtualized system, it thus does not suit our threat model and we can extend PThammer a bit to defeat it in our future work.

Empirically, ZebRAM observes that hammering a $row_i$ can only affect adjacent $row_{i+1}$ and $row_{i-1}$. Based on this observation, ZebRAM leverages the hypervisor to split memory of a VM into safe and unsafe regions using even and odd rows in a zebra pattern. That is, all even rows of the VM are for the safe region that contains data, while all odd rows are for the unsafe region as swap space. As such, a rowhammer attack from the safe region can only incur useless bit flips in the unsafe region. For a rowhammer attack from the unsafe region, it is not possible since the unsafe region is inaccessible to an unprivileged attacker.

However, Kim et al. [18] report that the above empirical observation is not correct, i.e., hammering a row can affect three rows or more in a certain number of DRAM modules. Besides, an attacker can compromise ZebRAM as follows. ZebRAM does not protect the physical memory of the hypervisor and thus extended page tables (EPTs) residing in the hypervisor space are adjacent to each other. As such, an unprivileged attacker can initiate regular memory accesses to conduct PThammer-like attacks, causing bit flips in EPT entries and escaping the VM.

Other Possible Instances of TeleHammer: Besides PThammer, there might also exist other instances of TeleHammer that leverage other built-in features of modern hardware/software. Particularly, features that focus more on functionality and performance may become potential candidates. For the hardware, we discuss about two famous CPU features. Specifically, out-of-order and speculative execution are two optimization features that allow a parallel execution of multiple instructions to make use of instruction cycles efficient. As such, an unprivileged attacker can leverage such features to bypass memory isolation and access kernel memory by using the processor [19, 24].

For the software, we talk about OS kernel features that handle local and network requests. A system call is a programmatic feature in which a user application requests a service from the kernel. By invoking a system call handler, a user can indirectly access kernel memory by using the kernel. A network I/O mechanism is also a programmatic feature that allows the OS to serve requests from the network. Particularly, the network interface card (NIC) will throw out a hardware exception to notify the kernel of each network packet NIC receives. Within the exception handler, the kernel will access kernel memory. Thus, a remote user can invoke this feature to access kernel memory by using the kernel.

As a result, an attacker can potentially build up an exploitable communication path to a target kernel address by abusing the above features.

Mitigation: Intuitively, we might detect both TeleHammer and PeriHammer using performance counters [1]. However, such anomaly-based detection is prone to false positives and/or false negatives by nature [6].

Alternatively, we might take hardware defenses such as PARA [18], TRR [28], [17] and TWiCe [22] to increase DRAM refresh rate for specified rows, which would reduce $T_{max}$ in Definition 5 (see section III-B) as much as possible so as to break the last time condition in the definition. Unfortunately, they require new hardware designs and thus cannot be used to protect legacy systems.

For PThammer, we might cache PTEs in an isolated cache to eliminate a communication path identified by PThammer. Since PTEs are placed in a separated cache, then PThammer cannot use the cache-eviction approach to evict PTEs. However, reserving an isolated cache only for page-table pages is expensive in hardware and requires re-designing hardware. Even if such an isolated cache for PTEs would be released by CPU manufacturers, there might exist other communication paths for PThammer to hammer PTEs, or other instances of TeleHammer that hammers other critical structures in the kernel space. Summarizing, we believe that TeleHammer-based rowhammer attacks are hard to mitigate.

VI. CONCLUSION

In this paper, we first observed a critical condition required by existing rowhammer exploits to gain the privilege escalation or steal the private data. We then proposed a new class of rowhammer attacks, called TeleHammer, that eschews the condition. Besides, we presented a formal model to define key conditions to set up TeleHammer and PeriHammer and summarized three advantages of TeleHammer over PeriHammer. On top of that, we created an instance of TeleHammer, called PThammer and developed a PThammer-based attack that allows an unprivileged attacker to compromise the latest software-only rowhammer defense and gain the root privilege.

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