A Power-adjustable Fully-integrated CMOS Optical Receiver for Multi-rate Applications

Kangyeob Park, Eun-Jung Yoon, and Won-Seok Oh*

SoC Platform Research Center, Korea Electronics Technology Institute (KETI), Seongnam 13509, Korea

(Received August 31, 2016 : revised September 22, 2016 : accepted September 24, 2016)

A power-adjustable fully-integrated CMOS optical receiver with multi-rate clock-and-data recovery circuit is presented in standard 65-nm CMOS technology. With supply voltage scaling, key features of the optical receiver such as bandwidth, power efficiency, and optical sensitivity can be automatically optimized according to the bit rates. The prototype receiver has -23.7 dBm to -15.4 dBm of optical sensitivity for 10^{-9} bit error rate with constant conversion gain around all target bit rates from 1.62 Gbps to 8.1 Gbps. Power efficiency is less than 9.3 pJ/bit over all operating ranges.

Keywords: Optical receiver, Transimpedance amplifier, CMOS, Silicon, Optical interconnect

OCIS codes: (250.3140) Integrated optoelectronic circuits; (130.0250) Optoelectronics; (060.2330) Fiber optics communications; (060.4510) Optical communications

I. INTRODUCTION

Ultra-high definition displays mainly drive high-speed interconnect markets in consumer electronics. Display interfaces such as DisplayPort, high-definition multimedia interface (HDMI), and mobile high-definition link (MHL) are required to have more data rates, more pixels, and longer transmission distances. As demands on long-distance display interconnects have increased, optical interconnect technology makes inroads into existing copper-based interconnects. The optical receiver is one of the most critical components in optical interconnect systems. The optical receiver has an optimum bandwidth for the target bitrates due to the trade-off between inter-symbol interference and noise. However, the strong correlation between bandwidth, noise, conversion gain, and power efficiency of the optical receiver is the hardest part to adjust as a function of the bit rate. In this paper, we report a power-adjustable fully-integrated CMOS optical receiver for DisplayPort 1.3 having multi data rates: 1.62, 2.7, 5.4, and 8.1 Gbps. Backwards compatible with earlier DisplayPort standards, i.e. it has to cover multi data rates: 1.62, 2.7, 5.4 and 8.1 Gbps. DisplayPort also embeds the clock signal inside the data signal, so the receiver should be accompanied with clock-and-data recovery (CDR) circuits [1, 2].

II. OPTICAL RECEIVER AND EXPERIMENTAL SETUP

The optical receiver for DisplayPort 1.3 should be fully...
(ring-VCO) locks the output clock phase of ring-VCO to that of the 135-MHz input reference clock \( f_{\text{REF}} \). According to the bit rates of the input data, a programmable frequency divider (Prog FD) having dividing factors of 6, 10, 20, and 30 can control the output clock frequency to be half of the input bit rates, 0.81, 1.35, 2.7, and 4.05 GHz. Once a lock detector (LD) detects the frequency of \( f_{\text{VCO}/M} \) is equal to \( f_{\text{REF}} \), it disables the frequency tracking loop and enables the phase tracking loop by simply controlling a multiplexer. The phase tracking loop leads to phase locking through the half-rate bang-bang phase detector (BBPD), and the BBPD finally retimes the data with the extracted clock. Two bits of digital inputs, mode\( <1:0> \), indicate what data rate comes into the input ports: 00, 01, 10, and 11 signals present 1.62, 2.7, 5.4, and 8.1 Gbps, respectively.

Ring-type VCO is composed of 3-stage inverters and current mirrors for delay control. The current of the inverter is controlled by both analog tuning voltage through the LF and digital codes, Early/Late, from the BBPD. With these, the VCO has fast locking and wide tuning characteristics. Tuning range of the VCO is 0.5 to 4.4 GHz and the worst phase noise is 95.8 dBc/Hz at 10-MHz offset.

III. BANDWIDTH ADJUSTMENT OF ANALOG FRONT-END

Figure 2 shows the schematic of the AFE. To adjust the bandwidth, \( \text{VDD}_{\text{AFE}} \) is scaled down from 1.2V to 0.9V as a function of the bit rates by controlling mode\( <1:0> \). And common-source topology is used for all amplifiers to make bandwidth of the AFE be able to change according to \( \text{VDD}_{\text{AFE}} \) [9, 10]. In the shunt-feedback pre-amplifiers, lower supply voltage makes the conversion gain be small as well as the bandwidth. By increasing the feedback resistance \( R_f \), the gain can be kept to the desired value [11]. Each resistance
of the parallel resistor bank is optimized to the four bit rates, and mode<1:0> controls each NMOS switches through a one-hot decoder. The $R_F$ is designed to be 2, 3.3, 6.2, and 10 kΩ for 8.1-, 5.4-, 2.7-, and 1.62-Gbps data rates, respectively.

Figure 3 shows measured 3-dB bandwidth, optical sensitivity for $10^{-9}$ bit error rate (BER), conversion gain, and power efficiency as a function of target bit rates with and without adjusting bandwidth. Without any adjustment, 41.5, 24.8, 12.4, and 8.3 pJ/bit of power efficiency is measured at each bit rate. And the experiment results indicate -17.1, -16.8, -15.9, and -15.4 dBm of optical sensitivities without scaling, respectively. Smaller differences than expected between the sensitivities are caused by high frequency noise due to wider bandwidth than the optimal value. When scaling both $VDD_{AFE}$ and $R_c$, the bandwidth can be closer to the optimum value and better sensitivities are hereby obtained than in the case of scaling only $VDD_{AFE}$, as shown in Fig. 3(a) and 3(b). Also almost the same conversion gains can be achieved by controlling $R_c$, as depicted in Fig. 3(c). Through these bandwidth adjustments, the AFE exhibits uniform power efficiency over the all bit rates and better sensitivity with higher conversion gain, as described in Fig. 3(d) [12].

### IV. CHIP IMPLEMENTATION AND EXPERIMENTAL RESULTS

Figure 4 shows the measurement setup and chip microphotograph. The prototype receiver is realized in 65-nm
A bandwidth-adjustable optical receiver with multi-rate CDR is realized in 65-nm standard CMOS technology. With supply voltage and feedback resistance scaling, the receiver front-end has the optimum bandwidth at 1.62-, 2.7-, 5.4-, and 8.1-Gbps data rate without any other performance degradation. As a result, better optical sensitivity and power efficiency at low-speed operation are achieved. The proposed receiver makes an optical module for long-haul display interconnects, such as DisplayPort and HDMI, more easily have backward compatibility to their previous standards.

ACKNOWLEDGMENT

This research was supported by Industrial Technology Innovation Program through the Ministry of Trade, Industry, and Energy, Korea (Project No. 10060166).

REFERENCES

1. “VESA,” [Online]. Available: http://www.vesa.org/uncategorized/vesa-releases-displayport-1-3-standard/ [Accessed: 30-June-2016].
2. J.-C. Seo, Y.-H. Moon, J.-H. Seo, J.-Y. Jang, T.-J. An, and J.-K. Kang, “A 1.62/2.7/5.4 Gbps Clock and Data Recovery Circuit for DisplayPort 1.2 with a single VCO,” J. of Semicon. TECH. SCI. 13, 185 (2013).
3. C. Hermans and M. Steyaert, “A High-Speed 850-nm Optical Receiver Front-End in 0.18-μm CMOS,” IEEE J. Solid-State Circuits 41, 1606-1614 (2006).
4. S. H. Park, Q. Le, and B. Choi, “An Optical Transimpedance Amplifier Using an Inductive Buffer Stage Technique,” IEICE Trans. on Comm. E92-B, 2239-2242 (2009).
5. W.-Z. Chen, Y.-L. Cheng, and D.-S. Lin, “A 1.8V 10-Gb/s Fully Integrated CMOS Optical Receiver Analog Front-End,” IEEE J. of Solid-State Circuits 40, 1388-1396 (2005).
6. W.-Z. Chen and C.-H. Lu, “A 2.5 Gbps CMOS optical receiver analog front-end,” in Proc. IEEE Custom Integrated
Circuits Conf. (Orlando, USA, 2002), pp. 359-362.
7. W.-S. Oh, K. Park, K.-H. Park, C.-J. Kim, and J.-K. Moon, “Design and Implementation of 10-Gb/s Optical Receiver Analog Front-End in 0.13-μm CMOS Technology,” IEICE Trans. on Electron. **E93-C**, 393-398 (2010).
8. J. -S. Youn, M.-J. Lee, K. Park, H. Rucker, and W.-Y. Choi, “A bandwidth adjustable integrated optical receiver with on-chip silicon avalanche photodetector,” IEICE Electron. Express **8**, 404-409 (2011).
9. Y.-H. Chien, K.-L. Fu, and S.-I. Liu, “A 3-25 Gb/s Four-Channel Receiver With Noise-Canceling TIA and Power-Scalable LA,” IEEE Trans. Circuits Syst. II, Exp. Briefs **61**, 845-849 (2014).
10. K. Park, B. C. Kim, B. Jung, and W.-S. Oh, “A 1-13 Gbps tunable optical receiver with supply voltage scaling,” IEICE Electron. Express **11**, 20140733 (2014).
11. J. Sangirov, I. A. Ukaegbu, T.-W. Lee, M. H. Cho, and H.-H. Park, “10 Gbps Transimpedance Amplifier-Receiver for Optical Interconnects,” J. Opt. Soc. Korea **17**, 44-49 (2013).
12. E. Sackinger, “The Transimpedance Limit,” IEEE Trans. Circuits Syst. I, Reg. Papers **57**, 1848-1856 (2010).