Design of CMOS Power Amplifier for LTE MTC System Transmitter

Xiangning Fan¹ a, Jian Tao¹ and Xiangfei Zhu²

¹Institute of RF-&OE-ICs, School of Information Science and Engineering, Southeast University, 210096 Nanjing, China
²Institute of RF-&OE-ICs, School of Integrated Circuit, Southeast University, 210096 Nanjing, China

Abstract. An high linearity power amplifier based on TSMC 65nm LP CMOS process was designed, which can meet the application requirements of LTE MTC communication standards in 1.88~1.92GHz band, and the average efficiency was improved. As the core module of the system, the power amplifier employs a two-stage linear amplifier structure, and implemented with the technique of lossy networks and matching compensation, meets the requirements of indicators in wide-band range. According to the post-simulation results, in the working frequency band of 1.88~1.92GHz ,the proposed PA achieves maximum output power of more than 26dBm, power gain is over 20dB.The OP1dB is more than 24dBm,and the power added efficiency (PAE) at OP1dB is over 25%.The simulated S11 is under -10dB and achieved good input matching feature.

1 Introduction

With the development of wireless communication technologies, the modes and standards of wireless communication are increasing. In the field of mobile communications, China's self-developed third-generation mobile communication standard TD-SCDMA and the WCDMA and CDMA2000 standards developed by countries such as Europe and the United States, have been widely used. At present, the 3GPP-LTE, an evolved version of the 3G standard, has also been commercialized in some regions, providing people with higher quality mobile communication services. China, due to the marginalization of WIMAX and other technologies, and LTE's own perfect industrial chain, scale effect and higher maturity, it has been favored by most operators. TD-LTE-Advanced is a smooth evolution based on LTE, and is backward compatible with the LTE standard.Simultaneously, it is extended, enhanced, and improved on the basis of LTE. TD-LTE-Advanced is a new generation of mobile communication technology with independent intellectual property rights proposed by China after TD-SCDMA, which reflects the latest independent innovation achievements of China's communication industry in the field of broadband wireless mobile communication. Accelerating the industrialization of TD-LTE-Advanced is of great strategic significance for improving China's scientific and technological level and comprehensive national strength. The terminal radio frequency chip is a very important link in the TD-LTE-Advanced industry chain, and it is also a relatively weak link in China. The power amplifier (PA) is the largest and most energy-consuming circuit module in the radio receiving transmitter. It amplifies and transmits the RF signal to the transmitting antenna, which plays a very important role in the entire RF transceiver system. Due to the high yield and low cost of the CMOS process, the circuit is simple to implement and the volume can be made smaller. As the technology progresses, the cutoff frequency of the transistor can be continuously increased, so the RF power amplifiers are increasingly implemented in CMOS technologies[1].

According to the working state of the power amplifier, it can be divided into a linear power amplifier and a switching power amplifier. The linear power amplifier can be divided into Class A, Class B, Class AB and
Class C power amplifiers according to the conduction angle of the transistor. The difference between linear power amplifiers is mainly due to the difference in efficiency, as shown in Table 1. The transistor of the switching power amplifier operates in a switching state, and ideally the efficiency can reach 100%.

Table 1. Leading angle and maximum efficiency of linear power amplifier

| Classification | Leading angle(2θ) | Maximum efficiency(η_{max}) |
|----------------|-------------------|----------------------------|
| A              | 360°              | 50%                        |
| AB             | 180°<2θ<360°      | 50%<η_{max}<78.5%          |
| B              | 180°              | 78.5%                      |
| C              | <180°             | >78.5%                     |

2 Power Amplifier

Linear power amplifiers usually have the same circuit model, as shown in Figure 1. By setting different bias voltages for the transistors and adjusting their quiescent operating points, the power amplifiers can have different operating states in one signal period. Depending on the conduction angle of the transistor, it is divided into different amplifier types. Among them, the conduction angle of the class A power amplifier is 2π, the power amplifier of the class B is π, the conduction angle of the class AB power amplifier is between π and 2π, and the conduction angle of the class C power amplifier is between 0 and π.

The conduction angle of a linear amplifier is mainly determined by its static operating point. For a sinusoidal input signal, the transistor of the Class A amplifier is turned on during the entire period and its quiescent operating point is at the center of the current. The transistor of the Class B amplifier is turned on in half a cycle and the bias voltage is generally set and the threshold voltage V_{th} of the device is determined[2]. The static working point of the class AB power amplifier is between class A and class B. The static working point of the class C power amplifier is in the cutoff region of the transistor and the on time is less than half an input period. The static working point of the four linear power amplifiers is shown in Figure 2.

![Figure 1. Linear power amplifier circuit model](image1)

![Figure 2. MOS tube output characteristic curve and static working point of the amplifier](image2)
According to the analysis of Class A and Class B power amplifiers, Class A power amplifiers have better linearity, while Class B power amplifiers have higher efficiency. In the actual design, class AB power amplifiers become a common type of design by a compromise between linearity and efficiency. It can be seen from the static operating point setting in Figure 2 that the device of the class AB power amplifier is biased at a position between Class A and Class B operating conditions with a conduction angle between $\pi$ and $2\pi$. According to the different requirements of the amplifier operating frequency, efficiency, linearity and other indicators, its operating current is usually 5%-30% of the maximum current. Class AB power amplifiers have higher efficiency than Class A power amplifiers, and also provide better linearity than Class B power amplifiers[3][4].

The bias point of a Class C power amplifier is below the transistor turn-on voltage, so the turn-on time is less than half a signal period. When the conduction angle $\theta$ is close to zero, the efficiency will approach 100%. However, the output power and efficiency of the device are zero at this time, and the power amplifier has lost its practical significance. In the actual design, the most common design method is not to add the bias voltage at the gate even if the zero bias voltage is used for design. At this time, the design process is no longer implemented according to the set conduction angle and the amplifier design is performed according to the state of the transistor under zero bias.

2.1 Architecture of PA
The main content of the project is to design a power amplifier based on TSMC 65nm LP CMOS technology. The standard supported by this power amplifier should include the mainstream 4G LTE (Band39 1880MHz~1920MHz) MTC communication standard and improve efficiency as much as possible while ensuring the necessary output power. High linearity requirements are important indicators of this topic, and linear power amplifiers generally have better linear performance than switching power amplifiers. Therefore, this topic chooses to use class AB power amplifiers to implement the power amplifier body. In the CMOS process, the transconductance of the transistor is low. When the power is output under the premise of ensuring stability, the gain of a single MOS transistor is generally about 10dB. It is difficult to achieve the index requirement by using the one-stage amplification circuit. Therefore, the MTC power amplifier adopts a two-stage amplification structure to meet the requirements of gain and so on. In addition, both the driver and power stages use a cascode structure, which provides higher gain and improves reverse isolation between input and output and achieves high power output. In order to reduce the influence of source key and line inductance, the designed power amplifier adopts a differential structure. Under ideal conditions, the output power is increased by 3dB compared with the single-ended structure, which reduces the output power requirement of a single tube. Power amplifier structure diagram shown in Figure 3.

2.2 Analysis of PA
The TSMC 65nm LP CMOS process provides a variety of transistors with a breakdown voltage of 1.2VDD. To prevent tube breakdown, a 3.3V transistor with a thick gate oxide structure was selected after comparing the process characteristics of several transistors. As a power tube, the MOS transistor has a minimum gate length of 500nm, which satisfies the requirements of high power output. The drive tube power is small, so the lower voltage can be selected, and a 1.2V thin grid tube is used to achieve a larger gain. The characteristic frequencies of the two transistors are much higher than the upper frequency limit of 1.9 GHz required for the design. The power amplifier is designed for a fixed supply voltage of 3.3V. To achieve a 1dB compression point of 24dBm, the maximum output power is at least 26dBm for Class A operation. The required quiescent bias current

$$I_0 = \frac{2P_{\text{out}}}{V_{\text{DD}}} = 241mA$$
Comparing the requirements of efficiency and linearity, the power amplifier can be biased in class AB. The bias current can be reduced based on the class A state, and then divided by the differential circuit. The single-tube bias current can be set to 100mA. In order to facilitate the test and work type adjustment, the gate bias of this design is directly added to 0.9V. The transistor size can be determined by scanning the DC parameters of the tube. Considering the factors such as layout symmetry and line width, the number of transistors and the index of each transistor are reasonably distributed[5]. The driver stage transistor design method is similar to the power stage. It is worth noting that in order to ensure the overall linearity and the linear output range of the entire power amplifier is not guaranteed, the output stage 1dB compression point of the driver stage is greater than the input stage 1dB compression point. A large deterioration occurs due to the lack of linearity of the driver stage. The gain of the power stage transistor is about 10dB, so the driver stage needs to provide about 15dBm of output power. The static bias current required for a single circuit of the differential circuit is estimated to be about 30mA with 1.8V voltage source, which is an estimate of the optimum load impedance at the output. The conjugate matching method is adopted between the output of the driver stage and the input of the power stage. In this case, in order to achieve an output power of 15dBm, the driver stage needs to appropriately increase the static bias current based on the theoretical calculation, and then the driver stage can be determined. The size of cascode tube can be designed to double the size of the cross-conduit. The design specifications of the power amplifier include Power Supply Voltage, Working Frequency, Output 1dB Gain Compression Point (OP1dB), Power Gain, Power Added Efficiency (PAE), Kf, Input-Output Matching Degree, etc. The design specifications are shown in Table 2. The circuit structure used is as shown in Figure 4.

### Table 2. Design indicators of power amplifier

| Process   | TSMC 65nm LP CMOS |
|-----------|-------------------|
| Voltage   | 1.8V, 3.3V        |
| Working Frequency | 1880MHz-1920MHz   |
| OP1dB     | 24dBm             |
| PAE       | ≥15%              |
| Power Gain| ≥20dB             |
| S11       | ≤-10dB            |
| Kf        | ≥1                |

**Figure 4.** Power amplifier circuit structure

2.3 Post-simulation Results

The power amplifier layout design proposed in this project uses TSMC 65nm LP CMOS process library, and the layout is drawn under Cadence Virtuoso software, as shown in Figure 5. The area of the whole circuit is 0.81mm×1.68 mm.
Layout design is a key step in the process of moving a chip from a schematic to a physical object. Difference from the ideal connection in the schematic diagram, the actual interconnection line has many parasitic capacitances, inductances and resistances\cite{6}. There is also mutual coupling between the signals. Therefore, the simulation, extracting the parameters, is closer to the actual situation than the previous simulation and it has better reference value. The layout of the power amplifier also needs to consider metal current density, pad position arrangement, large-size transistor arrangement and separation between power supply and ground\cite{7}.

### 2.3.1 Metal Line Width

Power lines, ground lines and input and output signal lines of the power transistor need to flow a large current. The metal line with insufficient line width is more likely to be blown due to the electric migration effect, resulting in short life or direct burnout of the chip. In the project, the line current density requirement should be observed. Meanwhile, the line width of each line should be strictly calculated and a certain margin should be reserved. There are 9 layers of metal in the TSMC 65nm LP CMOS process. The first to second layers of metal allow a DC current density of $1.48 \text{mA/}/\mu \text{m}$ (110°C), and the second layer of metal has a DC current density of $1.84 \text{mA/}/\mu \text{m}$ (110°C). The corresponding AC current density is usually 3-4 times of the DC current, so the width of each metal signal line can be estimated based on the simulation results. Since the maximum width of the single-layer metal is limited by the process, it is preferable to use multiple layers of metal parallel wiring, and the layers are interconnected by punching so that the area of the entire chip area can be minimized and the parasitic resistance of the metal trace can be reduced\cite{8}. Reducing power loss is also more conducive to wiring.

For large-sized power transistors, due to the width of the interdigital fingers and the limited trace width of the drain and source of a single component, all currents that a single transistor cannot support should be connected in parallel with multiple MOS transistors and the crossover index should be properly set.

### 2.3.2 Delay Consistency

Since the power amplifier has to output a large power, the power tube has a large size. Considering the metal line and the interdigital current density limitation, multiple MOS transistors are required in parallel, which results in a long metal trace distance. When the lengths of the input and output signal lines of the transistors are not equal, a phase difference may occur between the signals, resulting in attenuation of the synthesized power at the output.

In order to avoid this situation, a “one split into two, two combine into one” routing method is adopted in the signal line design and a synthesized structure is performed for each two signals to ensure each signal of 16 parallel MOS transistors. The line distances are equal and the synthesis efficiency of the output power is improved, as shown in figure 5.

Before evaluating circuit performance, we need to ensure the stability of the amplifier. The simulation setting frequency range is from 1.6GHz to 2.2GHz. Figure 6 shows the $K_f$ factor simulation result of the circuit. If $K_f$ is greater than 1, the circuit is unconditionally stable in the frequency band and leaves an appropriate margin.

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**Figure 5.** Layout of the power amplifier
Figure 6. Layout of the power tube

Figure 7. Stability factor $K_f$

The input power ranges from -15dBm to 15dBm when the frequency is set to 1.9GHz. The power amplifier is linearly simulated. The result is shown in Figure 7. The simulation results show that the Output 1dB Gain Compression Point is equal to 24.1dBm, which meets the requirement of 24dBm.

Figure 8. OP_{1dB}

The input frequency is from 1.7 GHz to 2.1 GHz, and the simulated S-parameter results are shown in Figure 8 below. As can be seen from the figure, in the operating band of 1.9 GHz, $S_{11} < -12$ dB, indicating that the input is well matched and the return loss is small. $S_{12} < -50$ dB, indicating that the reverse transmission coefficient is small and the reverse gain is low. $S_{21} > 21$ dB, indicating that the power gain size meets the requirements of the indicator. $S_{22} < -10$ dB, indicating that the output is well matched and the insertion loss is small.
In the 1.9GHz band, the input power range of -1dBm~15dBm is set, and the power added efficiency of the simulation is as shown in Figure 8. The simulation results show that when the Output 1dB Gain Compression Point is greater than 24dBm (IP1dBm=5.8dBm), the power added efficiency is greater than 25%, which has higher efficiency and meets the requirements of the index.

3 Conclusion
The simulation results are now compared with the project indicators, as shown in Table 3.
Table 3. Results and comparison with requirements

| Index             | Requirements   | Results    |
|-------------------|----------------|------------|
| Voltage           | 1.8V, 3.3V     | 1.8V, 3.3V |
| Working Frequency | 1.88GHz-1.92GHz | 1.88GHz-1.92GHz |
| OP_{dBm}          | 24dBm          | 24.1dBm    |
| PAE               | ≥15%           | ≥25%       |
| Power Gain        | ≥20dB          | 21dB       |
| S11               | ≤-10dB         | ≤-12dB     |
| K_f               | ≥1             | ≥15        |

A 3.3V high-linearity power amplifier in 65nm LP TSMC RF CMOS technology is presented. The simulation results show that the power amplifier operates correctly with the 1.88-1.92GHz input. At the maximum input power, a current of 98 mA is drawn from the 3.3V supply and a current of 36 mA is drawn from the 1.8V supply. At the same time, it has good input and output matching, high linearity and efficiency.

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