Accelerating Fully Connected Neural Network on Optical Network-on-Chip (ONoC)

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Abstract—Fully Connected Neural Network (FCNN) is a class of Artificial Neural Networks widely used in computer science and engineering, whereas the training process can take a long time with large datasets in existing many-core systems. Optical Network-on-Chip (ONoC), an emerging chip-scale optical interconnection technology, has great potential to accelerate the training of FCNN with low transmission delay, low power consumption, and high throughput. However, existing methods based on Electrical Network-on-Chip (ENoC) cannot fit in ONoC because of the unique properties of ONoC. In this paper, we propose a fine-grained parallel computing model for accelerating FCNN training on ONoC and derive the optimal number of cores for each execution stage with the objective of minimizing the total amount of time to complete one epoch of FCNN training. To allocate the optimal number of cores for each execution stage, we present three mapping strategies and compare their advantages and disadvantages in terms of hotspot level, memory requirement, and state transitions. Simulation results show that the average prediction error for the optimal number of cores in NN benchmarks is within 2.3%. We further carry out extensive simulations which demonstrate that FCNN training time can be reduced by 22.28% and 4.91% on average using our proposed scheme, compared with traditional parallel computing methods that either allocate a fixed number of cores or allocate as many cores as possible, respectively. Compared with ENoC, simulation results show that under batch sizes of 64 and 128, on average ONoC can achieve 21.02% and 12.95% on reducing training time with 47.85% and 39.27% on saving energy, respectively.

Index Terms—Optical network on chip, fully connected neural network, parallel computation, mapping.

1 INTRODUCTION

Artificial Neural Networks (ANNs), such as Fully Connected Neural Network (FCNN), Convolution Neural Network (CNN) and Recurrent Neural Network (RNN), are very popular nowadays. FCNN known as Multilayer perceptron (MLP) has the architecture that all the neurons in one layer are connected to the neurons in the next layer, which is widely employed in the applications related to prediction, pattern classification and function approximation in practical. Theoretically, FCNN is able to approximate any functions with a degree of loss and had already been proved to be a universal function approximator [1]. It is reported that FCNN dominates the communication workloads in data centers, where FCNN, CNN and RNN represent 61%, 19% and 5% of the total workload respectively [2]. Moreover, the fully connected network structure is commonly used by CNN to implement classification. However, FCNN training process can take a long training time with large data sets mainly due to the data movement latency in the hierarchical memory architecture [3]. Therefore, it is of great significance to break the bottleneck of training FCNN.

To accelerate the training of FCNN, parallel computations are adopted by using parallel programming architectures, such as MPI, OpenCL, OpenMP, CUDA, and etc. With these parallel programming architectures, FCNN training model or training data can be divided and then assigned to different computing units or platforms. Nevertheless, the latency caused by the data movement from the traditional bus-based main memory to cache, is hard to satisfy the demand of high performance computing in many-core processors. Though Electrical Network-on-Chip (ENoC) has been proposed to replace the traditional communication methods, transmission delay and power consumption are still two major concerns [4]. With more and more cores integrated in one single chip, parallel computing for FCNN training can easily reach communication bottleneck due to the limitations of ENoC.

To break the communication bottleneck, ONoC has been proposed as a promising alternative with the recent development of CMOS-compatible optical devices [5]. Instead of using electrical signal, ONoC uses optical signals to transmit data through waveguides with obvious advantages over ENoC, including low transmission delay, low power cost, high bandwidth and high throughput. According to [6], the average transmission latency in ENoC is 10 times more than that in ONoC, and ENoC has much higher power consumption than ONoC. Moreover, ONoC enables multiple optical signals to be transmitted simultaneously in one waveguide using different wavelengths by Wavelength Division Multiplexing (WDM) [7]. With these advantages, ONoC has great capability to perform intensive and high throughput inter-core communications required by the data exchange among cores for accelerating the parallel computing of FCNN training. The latest research progress [8] also indicates that more and more scientists are applying light based technologies for the research area of neural networks.

By leveraging the advantages of ONoC, we aim to develop an acceleration model for FCNN training by addressing the following challenges: (1) Modeling the computations and communications for training FCNN on ONoC and (2) assigning cores of ONoC to different execution stages of FCNN.
with the objective of minimizing the total training time. The specific problems include: What are the optimal numbers of cores for training a FCNN in different execution stages? How to map the neurons to cores on an ONoC for both forward propagation (FP) and back propagation (BP) within the wavelength limitation? What are the memory requirements of cores to store the FCNN parameters? In this paper, we address the above challenges with key contributions summarized as follows:

- We propose a fine-grained parallel computing model for FCNN training on ONoC, which can be used to analyze the trade-off between computation and communication in FP and BP processes. Based on this model, we derive the optimal number of cores required in each execution stage to minimize the total training time.

- We propose three mapping strategies for allocating the optimal numbers of cores to different stages of FCNN training. The advantages and disadvantages for each mapping strategy are discussed and analyzed in terms of hot-spot level, memory requirement, and state transitions.

- We evaluate our proposed acceleration schemes with extensive simulations. Firstly, we conduct simulations to show that the average prediction error on the optimal number of cores using NN benchmarks is within 2.3%, which verifies the effectiveness of our model. Secondly, we compare our proposed methods with traditional parallel computing methods that either allocate a fixed number of cores or allocate as many cores as possible. Results show that FCNN training time by our proposed scheme on ONoC is reduced by 22.28% and 4.91% on average, respectively. Lastly, we evaluate the performance and energy consumption of our methods between ONoC and ENoC, which shows the training time on ONoC is reduced by 21.02% and 12.95% and the energy consumption is reduced by 47.85% and 39.27% compared with ENoC under batch sizes 64 and 128, respectively.

The rest of this paper is organized as follows. Section 2 presents the background with motivation examples. Section 3 describes our proposed model and optimal solution. Section 4 illustrates three mapping strategies. Section 5 evaluates proposed models and methods, and Section 6 presents related work. Finally, Section 7 concludes the paper.

## 2 Background and Motivation

### 2.1 Fully Connected Neural Network

A FCNN has one input layer, one or more hidden layers and one output layer. The neurons of a FCNN are fully connected from one layer to the next layer with weights and bias. All neurons in the same hidden layer have the same activation function (e.g., Sigmoid, Tanh, ReLU and Softmax). Similarly, all neurons in the output layer have the same cost function (e.g., Mean squared error, Cross entropy, log-likelihood). For each neuron, it first reads the input and executes linear computation with weights and biases, then executes the non-linear function as follows:

$$ Y = A(W^T X + b), $$

where $X$ is the input vector, $Y$ is the predicted output vector, $W$ is the weight vector, $b$ is the bias vector, and $A$ is the activation or cost function. The output of the neuron from the activation function is used as the input of the neurons in the next layer. All neurons follow the same computation pattern layer by layer until the output layer. This is called the forward propagation in FCNN training.

After forward propagation, the predicted output and the expected output in the output layer are compared to get the loss of forward propagation. Then, partial derivatives are used to calculate the gradients to minimize the loss of forward propagation. The gradients are back-propagated to the previous layers to update the weights and biases through the chain rule computation. In back propagation, if the gradient vector calculated based on the loss is $\rho_j$, the weights are updated as follows:

$$ \rho = \sum_{j=1}^{T} \rho_j, $$

$$ W = W + \eta \rho, $$

where $\eta$ is the learning rate and $T$ is the number of training samples.

![Fig. 1. Ring-based ONoC with three planes.](image-url)

### 2.2 Optical Network-on-Chip

The ONoC architecture used to accelerate FCNN is shown in Fig. 1, which contains three planes: core plane, optical control plane, and optical data plane. In general, the core plane contains the cores to realize parallel computing, while the manager core is used to calculate routing and wavelength assignment and send requests to routing and wavelength allocator (RWA) in the control plane. The optical control plane contains the RWA and a cyclic optical control channel to configure the state of cores in the core plane and the optical routers in the optical data plane, as can be seen in Fig. 2. The optical data plane utilizes the configurable optical routers connected by a ring topology to provide optical data transmission, which enables cores to send and receive data packets simultaneously using WDM technology. The cores and optical routers are connected to the control channel by Through-Silicon Via (TSV) for router configuration and data transmission. Note that there are two control components: the manager core in the core plane calculates the configurations and the RWA in the optical control plane controls the network configuration. The manager core and the RWA share the same optical interface and they cooperate to transmit control packets to different interfaces by different
wavelengths at the same time and each interface can receive the right packets according to the wavelength. Accordingly, the corresponding modulators in transmitters’ routers and drop filters in receivers’ routers are configured and ready for communications. Fig. 3 illustrates the connections for optical components in the optical router, where the splitter is used to split optical signals on the receiver side (Rx), then the activated drop filters absorb the corresponding optical signals, and finally, optical signals are converted to electrical signals by photo-detector. The coupler on the transmitter side (Tx) is used to inject modulated light into the waveguide. We assume single waveguide is used in our design with off-chip laser source, while extended work can be further investigated for multiple waveguides [11] or on-chip laser source [12]. Besides, we assume that each core in the core plane has an on-chip distributed memory architecture with its L1 private cache and distributed SRAM connected to the main memory via the memory controller. The details of routing and wavelength assignment scheme and system parameters will be described in Section 4.6 and Section 5.

Fig. 2. The connection of optical interfaces in the optical control channel.

Fig. 3. Configurable optical router.

### 2.3 Motivating Examples

We first explain how a FCNN can be trained in an ONoC, and then present the motivations of our solution that leverages ONoC to accelerate FCNN training. The example given in Fig. 4(a) is used to explain the process of FCNN training in an ONoC. To speed up training using parallel computation, the neurons in a FCNN can be mapped to multiple cores to execute in parallel on the ONoC, where multiple neurons can be mapped onto the same core. As illustrated in Fig. 4(a), one epoch of training is divided into multiple periods based on layers, and these periods are executed sequentially. In Period 0, data and FCNN instructions in main memory are loaded to the distributed SRAM of ONoC cores. In the subsequent periods, the cores mapped with neurons in the corresponding layer perform computations concurrently and then pass the outputs to the cores mapped with neurons in the next layer through inter-core communications instead of accessing main memory.

With such a mapping of FCNN training on ONoC, we illustrate our motivations by the following examples:

**Example 1:** This example is to illustrate FCNN training can be accelerated by exploiting optical transmission for data exchange between cores in adjacent periods. When a FCNN is trained in a traditional multi-core system, the outputs of each neuron, weights, biases and gradients in the current execution stage may be written to the main memory for further processing in the subsequent execution stage. When the neurons in two adjacent periods are not mapped to the same core, the data needed for the computation in the next period may be loaded from the main memory to the corresponding cores. If the cores are reading the same parameters in the main memory, more delay will occur due to bank or port conflict in the main memory. These frequent read and write operations in main memory will cause relatively longer delay, thereby slowing down the FCNN training process with high energy cost. For instance, it takes around 180 cycles to access main memory in three level cache intel i7 CPU [13] and takes about 30 cycles and 375 cycles in the shared memory and main memory of NVIDIA Volta GPU architecture [14]. However, the off-chip memory access for neural network training can be alleviated by 94.1% on average using on-chip inter-core communication [15]. The average latency of inter-core communication ranges from 19 to 91 cycles in ENoC [16] and 3 to 7 cycles in ONoC [17], which are much faster than main memory access. Obviously, in comparison with ENoC, ONoC has much more potential...
to reduce the amount of time required for data communication during FCNN training. Moreover, by leveraging the WDM technology, multiple cores can transmit and receive data concurrently through waveguide as long as they use different wavelengths. This can further reduce the amount of time for data communications between neurons in adjacent layers.

Example II: This example is to illustrate there is a trade-off between computation and communication for FCNN training on ONoC, which allows the use of optimization techniques to further reduce the amount of training time. Suppose that the FCNN given in Fig. 4(a) is trained on an ONoC with four cores connected by ring topology, and assume that the number of available wavelengths is 2. We use the execution of Period 1 and Period 2 as an example, and consider the following two mapping schemes between neurons and cores: (1) Scheme 1: assigning 2 cores for Period 1 and 4 cores for Period 2. The four neurons in Period 1 are mapped to Core 1 and 2 with each core having two neurons, and the eight neurons in Period 2 are mapped to Core 1, 2, 3 and 4 with each core having two neurons. Since only 2 wavelengths are available, Core 1 and 2 can send their data to the other cores in parallel using 2 wavelengths (represented by the red and blue curved arrows), as illustrated in Fig. 4(b). (2) Scheme 2: assigning 4 cores for both Period 1 and Period 2. Since only two cores can send in parallel at one time, TDM has to be used costing two time slots. In the first time slot, as illustrated in Fig. 4(c), Core 1 and Core 2 can send their data to other cores in parallel using 2 wavelengths; In the second time slot, Core 3 and Core 4 can send their data to the other cores in parallel reusing the 2 wavelengths, as illustrated in Fig. 4(d). Hence, Scheme 1 uses fewer cores in Period 1 spending more time on computation with less time on communication than Scheme 2. During the backpropagation, cores can be reused according to a data locality constraint (to be defined in Eqs. (11) in Section 3.1.3), so that each neuron is mapped to the same core in the FP and BP to maximize data locality. For example, the cores assigned to Period 1 in FP process (e.g. Core 1 and 2 in Scheme 1) are the same as that assigned to Period 8 in BP process, while the cores assigned to Period 2 in FP process (e.g. Core 1, 2, 3 and 4 in Scheme 1) are the same as that assigned to Period 7 in BP process. Therefore, the senders (Core 1 and 2) in Period 1 become the receivers in Period 8 and the receivers (Core 1, 2, 3 and 4) in Period 2 become the senders in Period 7. It can be seen that using more cores can reduce the computation time, but incur more time on communication, which shows there is a trade-off between computation and communication in the mapping between neurons and cores. The challenging problem is: to train a given FCNN on an ONoC with a limited number of available wavelengths, how to map the neurons to cores for different periods so that the total amount of time for FCNN training is minimized. To tackle this challenge, we propose a FCNN acceleration model for ONoC that explores the trade-off between computation and communication to calculate the optimal number of cores for each period and minimize the FCNN training time.

3 FCNN Acceleration Schemes on ONoC

In this section, we first present our FCNN accelerating model, and then derive the optimal number of cores for each period to minimize the total training time.

3.1 Parallel Accelerating Model on ONoC

We consider the training of a FCNN with $l + 1$ layers labeled from layer 0 to layer $l$, where layer 0 and layer $l$ are the input and output layer, respectively. The number of neurons in layer $i$ is represented by $n_i$ for $i \in \{0, l\}$. As illustrated in Fig. 4(a), one epoch of training is divided into multiple periods based on layers. The FP process is divided into $l$ periods labeled from Period 0 to Period $l$, and the BP process is divided into another $l$ periods labeled from Period $l + 1$ to Period $2l$. We assume the ONoC contains $m$ cores connected by ring topology, and the number of available wavelengths is $\lambda_{max}$. We focus on the acceleration of one epoch during FCNN training because each epoch is repetitive. Note that all FCNN parameters and intermediate values are stored in SRAM of the corresponding cores distributively, with these parameters staying in the corresponding SRAM during one epoch of training. Cores used in different layers exchange data by optical communications in ONoC.

3.1.1 Computation Cost

We use $m_i$ to represent the number of cores assigned to Period $i$ for parallel computation, and assume that the neurons are evenly mapped to the $m_i$ cores in each period. In the FP process, Period 0 is used to map neurons to cores and load the training data to the corresponding cores from the main memory. Hence, computation starts from Period 1. According to the definition of periods, the neurons in layer $i$ where $i \in \{0, l\}$ get involved in Period $i$ in the FP process. The neurons in layer $2l - i + 1$ where $i \in \{1, 2l\}$ get involved in Period $i$ during the BP process. Therefore, the corresponding neuron number $n_i$ in FP process is the same as $n_{2l - i + 1}$ in the BP process. Let $X_i$ be the number of neurons mapped to each core in Period $i$ during the FCNN training. We have

$$X_i = \begin{cases} \left\lceil \frac{n_i}{m_i} \right\rceil, & i \in \{1, l\}; \\ \left\lceil \frac{n_{2l - i + 1}}{m_i} \right\rceil, & i \in \{l + 1, 2l\}. \end{cases}$$

Assume that all cores are homogeneous with the same computation capacity $C$. In the FP process, the computations consist of multiply-accumulate operations in the corresponding functions at each layer. We use $\alpha_i$ to represent the amount of each neuron computation in Period $i$ of the FP process. When the batch size (i.e., the number of samples in one training epoch) is larger than one, $\alpha_i$ is the amount of computation for each neuron in Period $i$ to process all samples in the current training. Then the amount of computation time at each core in Period $i$ of the FP process is $\frac{\alpha_i X_i}{m_i}$. In the BP process, the computation is dominated by the updates on weight and bias that consists of differentiation operations. For each neuron in Period $i$ of the BP process, it needs to update the weights for the connections to all neurons in Period $i - 1$. We use $\beta_i$ to represent the amount of computation to update the weight of one connection based on all training samples according to Eqs. (2) and (3). Since the gradient calculation related to the neurons in the next layer, the amount of computation updating weight at each core in Period $i$ of the BP process is $\beta_i X_i n_{2l - i}$. Unlike weight update, the bias is updated on a per-neuron basis. As updating a weight and updating a bias have the same
complexity, the amount of computation for bias update in Period \( i \) of the BP process is \( \beta_i X_i \). Therefore, the computation time cost for Period \( i \) during the BP process is 
\[
\beta_i X_i (n_{g_{2i-1}+1}/C), i \in [l+1, 2l].
\]

Let \( f(m_i) \) represent the amount of computation time required for each of the \( m_i \) cores in Period \( i \). We have
\[
f(m_i) = \begin{cases} 
\alpha_i X_i, & i \in [1, l]; \\
\beta_i X_i (n_{g_{2i-1}+1}/C), & i \in [l+1, 2l]. 
\end{cases}
\] 
(5)

3.1.2 Communication Cost

In the FP process, the outputs of the neurons in layer \( i \) need to be propagated to neurons in layer \( i+1 \), whereas the gradients computed at each neuron in layer \( i \) need to be back propagated to all neurons in layer \( i-1 \) in the BP process. As illustrated in Fig. 4(b), the propagation of neuron outputs and gradients can be effectively implemented in a ring-based ONoC using the broadcast operation, that is, if one core in the current period sends data along the ring, the cores assigned to the next period can receive the data by filtering a small portion of the transmitted optical signal. By leveraging the WDM technology, the communications in each period can be parallelized by letting multiple cores transmit simultaneously using different wavelengths. For Period \( i \) that demands communications, all the \( m_i \) cores can transmit concurrently if \( m_i \leq \lambda_{\text{max}} \); otherwise TDM needs to be used to complete the transmissions from the \( m_i \) cores. We use \( B_l \) to denote the amount of time for one core in Period \( i \) to complete the communications, which can be calculated based on the amount of data to be transmitted, the read and write operations for cache access, and the O/E and E/O conversions. Let \( g(m_i) \) be the total amount of time required to complete communications in Period \( i \). We have
\[
g(m_i) = \begin{cases} 
0, & i = 1, l \text{ and } 2l; \\
\left\lceil \frac{m_i}{\lambda_{\text{max}}} \right\rceil B_l, & \text{otherwise}. 
\end{cases}
\] 
(6)

\( g(m_1) = g(m_{2l}) = 0 \) because there is no communication in these periods.

3.1.3 Problem Formulation

Our objective is to compute the optimal number of cores allocated to each period, so that the training time required for one epoch can be minimized. The total amount of time to complete one epoch training, denoted by \( T \), includes the time for FP \( (\text{Time}_{\text{fp}}) \) and the time for BP \( (\text{Time}_{\text{bp}}) \). Based on our acceleration model, it can be calculated as follows:
\[
T = \text{Time}_{\text{fp}} + \text{Time}_{\text{bp}} = D_{\text{input}} + \sum_{i=1}^{2l} \left( f(m_i) + g(m_i) + \zeta_i \right),
\] 
(7)

where \( D_{\text{input}} \) represents the time delay caused by loading input data and FCNN instructions from the main memory to the assigned cores in Period \( 0 \), and \( \zeta_i \) represents the additional delay caused by extra main memory access, software overhead, synchronization, and etc. in the \( i \)th period. We formulate our problem as an optimization problem as follows:

Minimize \( T \),
(8)
and the optimization subjects to the following constraints.

- **Constraint on the size of ONoC**: The number of assigned cores \( m_i \) in each period is no larger than \( \phi m \):
\[
m_i \leq \phi m, i \in [1, 2l], \phi \in (0, 1],
\] 
(9)
where \( \phi \) is used to control the utilization of cores according to the system limitations such as signal crosstalk and power loss. As higher utilization of cores requires longer optical transmission path through more optical elements leading to higher crosstalk and power loss, \( \phi \) can be predefined according to the ONoC system as a threshold to satisfy the crosstalk and power loss limitations.

- **Constraint on the size of FCNN**: The number of assigned cores in each period cannot be larger than the number of the neurons in that period:
\[
m_i \leq n_i, i \in [1, l] \text{ and } m_i \leq n_{2l-i+1}, i \in [l+1, 2l].
\] 
(10)

- **Constraint on data locality**: each neuron is mapped to the same core in the FP and BP to maximize data locality. Hence, the number of cores assigned to Period \( 2l-i+1 \) in BP process:
\[
m_{2l-i+1} = m_i, i \in [1, l].
\] 
(11)

3.2 Optimal Solution

In this section, we derive the optimal solution for the optimization problem formulated in Eq. (8).

**Lemma 1.** The optimal number of cores allocated to Period \( i \), denoted by \( m_i^* \) is
\[
m_i^* = \begin{cases} 
\min\{\left\lceil \frac{\theta_i}{B_i C} \right\rceil, \phi m\}, & i = 1; \\
\min\{\left\lceil \frac{\theta_i}{(B_i + B_{i-1}) C} \right\rceil, \phi m\}, & 1 < i < l; \\
\min\{\left\lceil \frac{\theta_i}{B_{i-1} C} \right\rceil, \phi m\}, & i = l;
\end{cases}
\]
where \( \theta_i = n_i \lambda_{\text{max}}[\beta_{2l-i+1}(n_{i-1} + 1) + \alpha_i] \).

**Proof.** According to Eq. (4), \( T \) is a multi-variable function with variables \( m_1, m_2, \cdots, m_i \). Assuming each \( m_i \) where \( i \in [1, l] \) is real number and the ceiling operators in all equations are removed, \( T \) becomes a continuous function. Hence, \( T \) is minimized when
\[
\frac{\partial T}{\partial m_i} = 0, \forall i \in [1, l].
\] 
(12)

**Case I:** When \( i = 1 \), only \( f(m_1) \), \( f(m_{2l}) \), and \( g(m_1) \) are functions of \( m_1 \) and \( f(m_{2l}) = 0 \). According to Eqs. (5), (6) and (7),
\[
\frac{\partial T}{\partial m_1} = \frac{\partial f(m_1)}{\partial m_1} + \frac{\partial f(m_1)}{\partial m_1} + \frac{\partial g(m_1)}{\partial m_1} = -\frac{n_1 [\alpha_1 + \beta_{2l}(n_0 + 1)]}{C m_1^2} + \frac{B_l}{\lambda_{\text{max}}}. 
\]
Let \( \frac{\partial T}{\partial m_1} = 0 \), then \( T \) is minimized when
\[
m_1 = \sqrt{\frac{n_1 \lambda_{\text{max}} [\beta_{2l}(n_0 + 1) + \alpha_1]}{B_l C}}.
\] 
(13)
Case II: When \(2 \leq i \leq l-1\), only \(f(m_i), f(m_{2l-i+1}), g(m_i)\) and \(g(m_{2l-i+1})\) are functions of \(m_i\). Similarly, let \(\frac{\partial T}{\partial m_i} = 0\), then \(T\) is minimized when
\[
m_i = \frac{n_l \lambda_{\text{max}}[\beta_{2l-i+1}(n_{2l-i} + 1) + \alpha_i]}{(B_i + B_{2l-i+1})C}. \tag{14}
\]

Case III: When \(i = l\), only \(f(m_l), f(m_{l+1})\), and \(g(m_l)\) are functions of \(m_l\) and \(g(m_l) = 0\). Similarly, \(T\) is minimized when
\[
m_l = \frac{n_l \lambda_{\text{max}}[\beta_{l+1}(m_{l+1} + 1) + \alpha_l]}{B_{l+1}C}. \tag{15}
\]

From the above three cases, we use \(\theta_i\) to represent the numerator of \(m_i\) so that we have \(\theta_i = n_l \lambda_{\text{max}}[\beta_{2l-i+1}(n_{2l-i} + 1) + \alpha_i]\). Since \(m_i\) for \(i \in [1, l]\) must be an integer and it must be no larger than \(\phi m\) according to the constraint given in Eq. (3), \(m_i^* = \min([m_i], \phi m)\). Hence, this lemma holds.

Theorem 1. Given a FCNN with \(l+1\) layers with layer \(i\) having \(n_i\) neurons, the minimum amount of time to perform one epoch training on an ONoC with \(m\) cores and \(\lambda_{\text{max}}\) wavelengths is \(T^* = D_{\text{input}} + \sum_{i=1}^{2l} \left( f(m_i^*) + g(m_i^*) + \zeta_i \right) \).

Proof. According to the proof for Lemma 1, the amount of time for one epoch training \(T\) is minimized when \(m_i = m_i^*\) for each \(i \in [1, 2l]\). Hence, by replacing \(m_i\) with \(m_i^*\) in Eq. (17), the minimum amount of time for epoch training is \(T^* = D_{\text{input}} + \sum_{i=1}^{2l} \left( f(m_i^*) + g(m_i^*) + \zeta_i \right) \).

\[ \square \]

4 Allocation of Cores on ONoC

After the optimal number of cores required for each period is derived, the next step is to investigate the core allocation for different periods on ONoC. In the following, we first present three mapping strategies and then discuss their advantages and disadvantages with the analysis of hotspot level, memory requirement and state transitions.

4.1 Three Mapping Strategies

Strategy I: Fixed Mapping (FM). The cores for each Period \(i\) are mapped sequentially along the ring in clockwise order, always starting from a fixed core (e.g. core \(1\)). That is, the cores allocated to Period \(i\) is \([\text{core}_1, \text{core}_2, ..., \text{core}_{m_i^*}]\).

For example, for a 5-layer FCNN to be trained on an ONoC with 9 cores, assume \(m_1^* = 3\), \(m_2^* = 4\), \(m_3^* = 5\), and \(m_4^* = 3\) according to our model. As illustrated in Fig. 5 (a), \([\text{core}_1, \text{core}_2, \text{core}_3]\) are assigned to Period 1, \([\text{core}_1, \text{core}_2, \text{core}_3, \text{core}_4]\) are assigned to Period 2, \([\text{core}_1, \text{core}_2, \text{core}_3, \text{core}_4, \text{core}_5]\) are assigned to Period 3, and \([\text{core}_1, \text{core}_2, \text{core}_3]\) are assigned to Period 4. The advantages of this strategy include: (1) fewer messages to receive due to the core reuse, even though the number of transmitted messages remains unchanged. For example, \([\text{core}_1, \text{core}_2, \text{core}_3]\) are reused in Period 1 and Period 2. Each time one of these three cores transmits a message, only three of the cores assigned to Period 2 need to receive the message. If there is no core reuse, all four cores assigned to Period 2 need to receive the message; (2) less energy consumption due to the low frequency to change state of the cores and optical routers. For example, \([\text{core}_1, \text{core}_2, \text{core}_3]\) are used for all periods, and they just need to change state one time in each epoch training; (3) less crosstalk and insertion loss since the maximum path length during the whole FCNN training is \(\max_{l=1}^{l} m_l^* - 1\) (e.g. 5 in the example). However, this method also has several disadvantages: (1) high memory requirement because the reused cores need to store the parameters for all involved periods; (2) hot-spot and unbalanced thermal dissipation because some cores keep working during the training process.

Strategy II: Round-Robin Mapping (RRM). The cores for each Period \(i\) are mapped sequentially along the ring, starting from the core next to the last core allocated to Period \(i-1\). As illustrated in Fig. 5 (b), \([\text{core}_1, \text{core}_2, \text{core}_3]\) are assigned to first period, \([\text{core}_4, \text{core}_5, \text{core}_6, \text{core}_7]\) are assigned to the second period, and so on. Different from FM, there are no reused cores in adjacent periods in RRM. The merits of the RRM are: (1) hot-spot avoidance and balanced thermal dissipation due to the nature of round-robin selection; (2) less memory requirement since the cores are involved in fewer periods, thus only the parameters of the involved periods are stored. However, it also has some drawbacks including: (1) more messages to receive since there is no core reuse between adjacent period; (2) more energy consumption due to the frequent state changes at the cores and optical routers. For example, different from FM, \([\text{core}_1, \text{core}_2, \text{core}_3]\) in RRM are active before Period 1 starts, and then become idle after Period 1 is finished. \([\text{core}_4, \text{core}_5, \text{core}_6, \text{core}_7]\) are active before Period 2 and receives the message from \([\text{core}_1, \text{core}_2, \text{core}_3]\), then become idle in the end of Period 2 and so on.

Strategy III: Overlapped Round-Robin Mapping (ORRM). To overcome the drawbacks of both FM and RRM, we propose a third mapping scheme called Overlapped Round-Robin Mapping, which is similar to RRM strategy but allows core reuse in the adjacent periods. As illustrated in Fig. 5 (c), \([\text{core}_1, \text{core}_2, \text{core}_3]\) are assigned to Period 1 and \([\text{core}_2, \text{core}_3, \text{core}_4, \text{core}_5]\) are assigned to Period 2, where \([\text{core}_2, \text{core}_3]\) are reused in these two periods.

Let \(r_i\) be the number of cores reused in Period \(i\) and Period \(i-1\). To balance core reuse, we define the expected number of reused cores in two adjacent periods, denoted by \(E[r]\), as
\[
E[r] = \begin{cases} 
0, & \text{if } \sum_{i=1}^{l} m_i^* \leq m; \\
\sum_{i=1}^{l} m_i^* - m, & \text{otherwise.} 
\end{cases} \tag{16}
\]

When \(\sum_{i=1}^{l} m_i^* \leq m\), no core will be reused to reduce the memory requirement, which is equivalent to FM strategy. When \(\sum_{i=1}^{l} m_i^* > m\), some cores are reused, which are expected to be evenly distributed in different periods to balance hot-spot and thermal dissipation. Based on only \(E[r]\), it might occur that the expected number of cores to be
is at most 4 in one epoch FCNN training. FP, the maximum periods that a core can run consecutively used in the first period of BP are reused in the last period of than 2 consecutive periods in the FP process. While the cores without exceeding one circular round of the ring.

Lemma 2. In ORRM, the number of consecutive periods that a core can run is at most four in one epoch FCNN training, when \( m_i^* + m_{i+1}^* - r_{i+1} \leq m, \forall i \in [1, l - 1] \).

Proof. In the FP training process, when \( m_i^* + m_{i+1}^* - r_{i+1} \leq m, \forall i \in [1, l - 1] \), any two adjacent periods are allocated to the cores without exceeding one circular round of the ring. It can be easily proven that there is no core running for more than 2 consecutive periods in the FP process. While the cores used in the first period of BP are reused in the last period of FP, the maximum periods that a core can run consecutively is at most 4 in one epoch FCNN training.

The pseudo-code of ORRM is given in Algorithm 1. The input includes the optimal number of cores for each period \( m_i^* \) and the total number of cores in the ONoC \( m \). The output is a mapping matrix where \( M(i,j,k) = 1 \) if the \( j^{th} \) neuron in the \( k^{th} \) layer is mapped to core \( k \). Line (3) and line (8) are executing the mapping of the neurons in each period evenly to the cores assigned to that period.

Algorithm 1: Overlapped Round Robin Mapping

\begin{algorithm}
\begin{algorithmic}
\State \textbf{input} : \( m_i^* \) where \( i \in [1, l] \) and \( m \)
\State \textbf{output} : \( M(i,j,k) \) where \( i \in [1, l], j \in [1, n_i], \ k \in [1, m] \)
\State \text{sum} = \sum_{i=1}^{l} m_i^*; \quad \text{1. Calculate } E[r_i] \text{ according to Eq. (16).}
\State \text{Assign } [\text{core}_{e_1}, \text{core}_{e_2}, \ldots, \text{core}_{e_{m_i^*}}] \text{ to Period 1;}
\State k = \left\lfloor \frac{\text{sum}}{m} \right\rfloor; \quad \text{4. Assign } \text{core}_{e_{id_i + \text{mod } m_i^*}}, \text{core}_{e_{id_i + \text{mod } m_i^* + 1}}, \ldots, \text{core}_{e_{id_i + m_i^* - 1}} \text{ mod } m_i^* \text{ to Period 2;}
\State M[j, k] = 1, \text{ where } j \in [1, n_i]; \quad \text{5. } M[1, k] = 1, \text{ where } j \in [1, n_i];
\State \text{for } i \leftarrow 2 \text{ to } l \text{ do}
\State \text{Calculate } id_i, \text{ according to Eq. (18).}
\State \text{Assign } \text{core}_{e_{id_i + \text{mod } m_i^*}}, \text{core}_{e_{id_i + \text{mod } m_i^* + 1}}, \ldots, \text{core}_{e_{id_i + m_i^* - 1}} \text{ mod } m_i^* \text{ to Period 3;}
\State k = \left\lfloor \frac{\text{sum}}{m} \right\rfloor; \quad \text{8. Assign } \text{core}_{e_{id_i + \text{mod } m_i^*}}, \text{core}_{e_{id_i + \text{mod } m_i^* + 1}}, \ldots, \text{core}_{e_{id_i + m_i^* - 1}} \text{ mod } m_i^* \text{ to Period 4;}
\State M[j, k] = 1, \text{ where } j \in [1, n_i]; \quad \text{9. } M[1, k] = 1, \text{ where } j \in [1, n_i];
\State \text{end}
\end{algorithmic}
\end{algorithm}

4.2 Hotspot Analysis
Hotspots can be caused by non-uniform workload distribution among cores where some cores need to handle relatively higher workload on computation and communication than others. Hence, we analyze hotspots by comparing the maximum number of consecutive periods for cores to run in three mapping strategies.

Theorem 2. The maximum number of consecutive periods for cores to run during one epoch training (FP and BP) is

- 2l in Fixed Mapping;
- 2 in Round-Robin Mapping when \( m_i^* + m_{i+1}^* \leq m, \forall i \in [1, l - 1]; \)
- 4 in ORRM when \( m_i^* + m_{i+1}^* - r_{i+1} \leq m, \forall i \in [1, l - 1]. \)

Proof. Fixed Mapping has relatively severe hot-spot situation because there are \( m_i^* \) cores that keep running from Period 1 to Period 2l, where there are \( m - \max_{i=1}^{l} m_i^* \) cores that keep idle. This can lead to hot-spots with unbalanced thermal dissipation. For Round-Robin Mapping, cores are not reused by two adjacent periods if the number of cores assigned to these two periods does not exceed the total number of cores in the ring (i.e. \( m_i^* + m_{i+1}^* \leq m, \forall i \in [1, l - 1] \)), except for those cores running 2 consecutive periods in last period of FP reused in the first period of BP. This round-robin fashion allows the cores to take turns to be active and idle, which maintains relatively balanced thermal dissipation and prevents the occurrence of hot-spots to some extent. For ORRM, cores are reused only in two adjacent periods in FP and BP processes with cores reused at the end of FP and beginning of BP running for at most four consecutive periods according to Lemma 2. Therefore, the difference of active time among the cores is at most three periods no matter how many periods during the training process, which is not easy to form hot-spots with relatively balanced thermal dissipation.

4.3 State Transition Analysis
When a FCNN is trained on an ONoC, some cores and their associated optical routers need to stay active for some periods and turn to idle in other periods. Frequent transitions between the active state and idle state can degrade the performance and energy efficiency. Therefore, we estimate the number of state transitions in one FCNN training epoch for the three mapping strategies ranking from low (1) to high (3) as in Table 1.

| Name of mapping | Number of state transitions | Rank |
|-----------------|-----------------------------|------|
| FM              | \( 2(m_i^* + \sum_{i=2}^{l} m_i^* - m_{i-1}^*) \) | 1    |
| ORRM            | \( 2(\sum_{i=1}^{2l} r_i) \) | 2    |
| RRM             | \( 2(\sum_{i=1}^{2l} m_i^* - m_i^*) \) | 3    |

4.4 Crosstalk and Insertion Loss
Insertion loss and signal crosstalk are critical issues for ONoC design. For a specific optical routing path, the insertion loss \( IL \) can be calculated as

\[ IL = IL_{4} \times (N_{r} - 1) + IL_{r} \times N_{r} + IL_{eo} + IL_{oe}, \]
where $N_r$ is the total number of optical routers in the path, $IL_i$ and $IL_r$ are the insertion losses of one optical link and one optical router respectively, and $IL_{es}$ and $IL_{eo}$ are the insertion losses of E-O and O-E converters respectively \[18\]. Since $IL_i$, $IL_r$, $IL_{es}$, and $IL_{eo}$ are constant parameters for specific optical devices and router structure, the worst-case insertion loss $IL_{wc}$ is decided by the maximum length of the routing paths. Similarly, in terms of signal crosstalk, longer routing path passing through more optical elements can also lead to more crosstalk during transmission. Table 2 shows the maximum length of routing paths for the three mapping strategies during the FCNN training, indicating that FM has the least insertion loss and crosstalk ranked as (1), and RRM has the most insertion loss and crosstalk ranked as (3):

| Name of mapping | Maximum path length | Rank |
|-----------------|---------------------|------|
| FM              | $\max_{i=1}^{l} (m_i - 1)$ | 1    |
| ORRM            | $\max_{i=2}^{l} (m_i + m_{i-1} - r_i)$ | 2    |
| RRM             | $\max_{i=2}^{l} (m_i + m_{i-1} - 1)$ | 3    |

4.5 Memory Analysis

We use $\psi$ to denote the memory requirement for storing one parameter such as weight, bias, gradient, input and output in distributed SRAM of cores and $\mu$ to represent the batch size number in one epoch ($\mu \geq 1$). As neurons are involved in both FP and BP processes, we calculate the memory requirement for one neuron. For the FP process, according to Eq. (1), the memory requirement to process one neuron in layer $i$ includes $n_{i-1}$ weights, one bias, $n_{i-1}$ inputs, and one output, with a total memory requirement of $2(n_{i-1} + 1)\mu\psi$. For the BP process, since the weight and bias have already been stored in the SRAM of the corresponding core, the additional parameters to be stored include one bias gradient, $n_{i-1}$ weight gradients, one learning rate, with a total extra memory requirement of $(n_{i-1} + 2)\mu\psi$. Hence, when batch size is equal or larger than 2, the total memory requirement of each neuron on layer $i$ in both FP and BP process can be calculated as $s_i = (3n_{i-1} + 4)\mu\psi$, $i \in [1, l]$. The memory requirement for SRAM in each core depends on the number of mapped neurons and the mapping strategy, which can be calculated as $\sum_{i=1}^{l} \sum_{j=1}^{n_i} M[i, j, k] \times s_i$. So, the maximum memory requirement among SRAMs of all the cores (worst case) for the mapping strategy is formulated as:

$$\max_{k=1}^{m} \sum_{i=1}^{l} \sum_{j=1}^{n_i} M[i, j, k] \times s_i.$$  \hspace{1cm} (20)

Therefore, we estimate the maximum memory requirement among cores for three mapping strategies by Eq. (20) ranking from low (1) to high (3), as shown in Table 3.

| Mapping method | Maximum memory requirement of core | Rank |
|----------------|-----------------------------------|------|
| RRM            | $\max_{i=1}^{l} \left[ \frac{(3n_{i-1} + 4)\mu\psi n_i}{m_i} \right]$ | 1    |
| ORRM           | $\max_{i=1}^{l} \left[ \frac{(3n_{i-1} + 4)\mu\psi n_{i-1}}{m_i} + \frac{(3n_{i-1} + 4)\mu\psi n_{i+1}}{m_i} \right]$ | 2    |
| FM             | $\sum_{i=1}^{l} n_i \mu\psi (3n_{i-1} + 4)$ | 3    |

4.6 Routing and Wavelength Assignment

We describe the details of routing and wavelength assignment, and then use an example to illustrate the control process in the ring-based ONoC by using RRM. We assume the communication is bidirectional, where transmission direction in FP is clockwise and transmission direction in BP is anticlockwise.

![Routing and wavelength assignment example](image)

As mentioned in Section 2.2, the ONoC architecture consists of electrical core, optical control and optical data planes. The processes of routing and wavelength control are managed by the optical control plane. Firstly, the manager core calculates the optical number of cores and sends request to Routing and Wavelength Allocator (RWA), and then RWA generates the corresponding wavelength matrix and optical control packets. Secondly, RWA broadcasts the control packets along the cyclic optical control channel to configure the optical routers based on the generated wavelengths matrix. After control packets are received by the optical routers, the modulators and drop filters of the corresponding optical routers are configured with routing paths setup from each core in the previous period to all the cores in the next period. A specific wavelength for each routing path is specified according to the wavelength matrix, and multiple routing paths can transmit in parallel by different wavelengths through the same waveguide by WDM.

As shown in Fig. 5(a), the wavelength matrix, denoted by $WM[i, j]$, determines the routing and wavelength allocation, where $WM[i, j] = \lambda_k$ indicates core $i$ should communicate...
with core $j$ using wavelength $\lambda_k$. Assuming that 3 cores $[\text{core}_1, \text{core}_2, \text{core}_3]$ are assigned for Period 1 and 4 cores $[\text{core}_4, \text{core}_5, \text{core}_6, \text{core}_7]$ are assigned for Period 2 using RRM strategy. According to the W.M., $\lambda_1$ is assigned for the optical path from the source $[\text{core}_1]$ to the destinations $[\text{core}_4, \text{core}_5, \text{core}_6, \text{core}_7]$, with $\lambda_2$ and $\lambda_3$ assigned to optical paths from the sources $[\text{core}_2]$ and $[\text{core}_3]$ respectively. With all sender’s modulators and receivers’ drop filters activated, these three optical paths from source cores $[\text{core}_1, \text{core}_2, \text{core}_3]$ allocated for Period 1 can send their data to cores $[\text{core}_4, \text{core}_5, \text{core}_6, \text{core}_7]$ allocated for Period 2 simultaneously by three different wavelengths $\lambda_1, \lambda_2$ and $\lambda_3$, as illustrated in Fig. 6 (b).

5 Evaluation

In this Section, we conduct extensive simulations to verify the effectiveness of our methods. We first introduce our simulation setup in Section 5.1, and present the comparisons between theoretical results and simulation results in Section 5.2. Then, we carry out simulations to compare our methods with exiting methods in Section 5.3, and compare our methods on ONoCs with ENoCs in Section 5.4.

5.1 Simulation settings

The simulation platform is implemented in a machine with intel i5 3200 CPU and 32 Gb main memory. Gem5 [19] is used to simulate the target ONoC and ENoC systems, and DSENT [20] is used in calculating the energy consumption. To collect computation time and communication traces, we implement the FCNN in C using GNU Scientific Library [21]. Sigmoid is used as the non-linear activation function in hidden layers and softmax is used as the activation function in the output layer. We run the configured workloads with up to 1000 threads to generate the communication traces for up to 1000 cores. The communication traces are fed into Gem5 to obtain the communication time of each core.

To show Lemma 1 can predict the optimal number of cores accurately, first we calculate the Average Prediction Error (APE) and Average Performance Difference (APD) for the optimal number of cores for each layer of each benchmark in simulated environment. We use Batch Sizes (BS) 1, 8, 32, 64 and number of cores, ranging from 1 to 1000, in order to find the optimal number of cores for each layer of each benchmark in simulated environment. We use Batch Sizes (BS) 1, 8, 32, 64 and wavelength numbers 8 and 64 in the simulation.

In this experiment, we simulate the training process of the NN benchmarks for each layer under different numbers of cores, ranging from 1 to 1000, in order to find the optimal number of cores for each layer of each benchmark in simulated environment. We use Batch Sizes (BS) 1, 8, 32, 64 and wavelength numbers 8 and 64 in the simulation.

Table 7. Prediction accuracy for optimal number of cores

| Neural network | APE (%) | APD (%) |
|---------------|---------|---------|
| NN1           | 0.83    | 1.26    |
| NN2           | 1.24    | 2.78    |
| NN3           | 1.82    | 2.53    |
| NN4           | 1.92    | 3.68    |
| NN5           | 0.93    | 1.42    |
| NN6           | 2.22    | 4.29    |

5.2 Optimal number of cores

In this experiment, we simulate the training process of the NN benchmarks for each layer under different numbers of cores, ranging from 1 to 1000, in order to find the optimal number of cores for each layer of each benchmark in simulated environment. We use Batch Sizes (BS) 1, 8, 32, 64 and wavelength numbers 8 and 64 in the simulation.

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with batch size set to 32 and the number of wavelengths set to 64. The x-axis of the figure is the number of wavelengths ranging from 1 to 1000. The three curves in each subgraph of Fig. 7 represent the computation time, communication time and the total time of the layer, where Fig. 7(a) is for layer 3 during FP, Fig. 7(b) is for layer 3 during BP, and Fig. 7(c) is the combined results for layer 3 during both FP and BP. It can be seen from Fig. 7(a) and (b) that the optimal number of cores marked by red dots for FP and BP are 896 and 704 respectively, because computations and communications workload in FP and BP are different. Since the same cores need to be assigned to the same layer to guarantee the data locality, we calculate the optimal number of cores by using the combined results in both FP and BP processes. As shown in Fig. 7(c), the optimal number of cores assigned for layer 3 during both BP and FP is 769.

**TABLE 9. Energy difference of the optimal solution over FNP and FGP.**

| NN   | BS 1 | BS 8 | BS 64 | BS 128 | Average |
|------|------|------|-------|--------|---------|
| FNP  | 10.68% | 9.85% | 9.86% | 9.96% | 10.08% |
| FGP  | 9.95% | 10.7% | 3.00% | 3.00% | 2.51% |
| FNP  | 13.52% | 18.02% | 20.53% | 20.84% | 18.23% |
| FGP  | 19.52% | 3.51% | 0.26% | 0.10% | 5.80% |
| FNP  | 19.28% | 24.96% | 27.61% | 27.94% | 24.95% |
| FGP  | 18.87% | 3.49% | 0.19% | 0.09% | 5.14% |
| FNP  | 21.49% | 29.25% | 31.93% | 32.36% | 28.76% |
| FGP  | 17.75% | 4.56% | 0.17% | 0.06% | 5.63% |
| FNP  | 17.00% | 26.63% | 31.16% | 31.62% | 26.80% |
| FGP  | 12.76% | 4.22% | 0.64% | 0.29% | 4.48% |
| FNP  | 15.66% | 24.68% | 29.84% | 30.21% | 25.05% |
| FGP  | 14.98% | 6.09% | 0.93% | 0.42% | 5.61% |

5.3 Comparisons with Traditional Methods

To show better performance and energy efficiency of our proposed optimal solution, two traditional methods, (1) Finest-Grained Parallel method (FGP) [28] by mapping one neuron to one core; (2) Fixed Number Parallel method (FNP) [29], which is set with a fixed number of cores (200) for each period during the training, are compared with the optimal solution. When comparing the above three methods, we adopt Fixed Mapping strategy in the simulation, and use Batch Sizes (BS) 1, 8, 64, 128 and wavelength numbers 8 and 64 in the simulation.

Table 8 shows the average performance improvement for the optimal solution over FNP and FGP for each NN benchmark using wavelength numbers 8 and 64. As can be seen from Table 8, with the increasing of batch sizes, the performance improvement for the optimal solution compared with FNP is increasing, while performance improvement compared with FGP is decreasing for all NN benchmarks. That is because computation workload is increasing with the increase of batch size, thus the optimal solution tends to use more cores getting close to FGP. Table 9 shows the energy difference for the optimal solution with FNP and FGP for each NN benchmark. It can be seen that the optimal solution is more energy efficient than FGP, and less energy efficient than FNP in most cases.

Fig. 8 and Fig. 9 show the comparisons on performance and energy consumption between the optimal solution and two traditional methods with NN benchmarks under batch sizes 1 and 8 with wavelength numbers 8 and 64. All results are normalized by dividing the first result of NN1. The corresponding optimal number of cores generated by our optimal solution is shown in Table 10. From Fig. 8(a) and (b), we can see that the total training time of the optimal solution is the lowest among three methods under different batch sizes and wavelengths. On average, when the batch size is set to 1 and the number of wavelengths is set to 8 or 64, the training time of the optimal solution compared with FGP and FNP is reduced by 16.27% and 15.27% respectively. When the batch size is 8, the training time of the optimal solution is reduced by 22.23% and 3.85%, respectively. It can be seen from Fig. 9(a) and (b) that the training time of FCNN using 64 wavelengths is less than that using 8 wavelengths. This is because the communication time is largely reduced
TABLE 10. Optimal number of cores

| NN1   | BS = 1, wavelength = 8  | BS = 1, wavelength = 64  | BS = 8, wavelength = 8  | BS = 8, wavelength = 64  |
|-------|-------------------------|--------------------------|-------------------------|--------------------------|
|       | [1000, 257, 10]         | [1000, 257, 10]          | [1000, 257, 10]         | [1000, 257, 10]          |
| NN2   | [1000, 393, 505, 257, 10] | [1000, 449, 513, 321, 10] | [1000, 401, 505, 329, 10] | [1000, 704, 641, 500, 10] |
| NN3   | [1000, 753, 393, 505, 257, 10] | [1000, 769, 449, 513, 257, 10] | [1000, 769, 449, 513, 257, 10] | [1000, 769, 500, 10] |
| NN4   | [1000, 673, 753, 393, 505, 257, 10] | [1000, 707, 769, 449, 517, 353, 257, 10] | [1000, 681, 733, 417, 517, 353, 257, 10] | [1000, 897, 1000, 449, 577, 353, 257, 10] |
| NN5   | [1000, 505, 665, 10]     | [1000, 833, 833, 10]     | [1000, 601, 817, 10]    | [1000, 1000, 833, 10]    |
| NN6   | [1000, 1000, 833, 10]    | [1000, 513, 801, 513, 801, 513, 801, 10] | [1000, 513, 801, 513, 801, 513, 801, 10] | [1000, 1000, 833, 10]    |

Fig. 8. Comparisons on the training time by three methods for NN benchmarks with 8 and 64 wavelengths under (a) batch size 1 and (b) batch size 8. The shaded part quantifies the communication time among the total training time.

Fig. 9. Comparisons on the normalized energy by three methods for NN benchmarks with 8 and 64 wavelengths under (a) batch size 1 and (b) batch size 8. The shaded part represents for dynamic energy consumption while the un-shaded part represents for static energy consumption.

due to concurrent communications achieved by WDM with more wavelengths and less time slots.

Fig. 9 (a) and (b) show that the optimal solution consumes the least energy among three methods under wavelength number 64, and FNP consumes the least energy under wavelength number 8 for both batch sizes 1 and 8. That is because the static energy affected by the training time is dominated in the total energy consumption under wavelength number 64, while dynamic energy affected by the number of cores takes up more proportion in total energy consumption under wavelength number 8. This indicates that our method tends to be more energy-efficient especially when the number of wavelengths is large (e.g. 64 in the example). On average, when the batch size is set to 1 and the number of wavelengths is set to 8 or 64, the energy consumption of the optimal solution compared with FGP is reduced by 23.67% but is increased by 7.64% compared with FNP. When the batch size is 8, the energy consumption of the optimal solution compared with FGP is reduced by 11.26% but is increased by 1.83% compared with FNP.

5.4 Comparisons with ENoC

In order to demonstrate the advantages of using ONoCs, we compare our methods on ONoC with ENoC in terms of both performance and energy consumption. The performance of the three mapping strategies (FM, RRM, and ORRM) in ONoC are almost the same because latency is not affected much by the transmission distance in ONoC due to the very high transmission speed of optical signals. However, different mapping strategies will make a huge difference in training time for ENoC because of the hop by hop routing in ENoC. In order to make a fair comparison, we compare the performance and energy consumption between ONoC with ENoC by Fixed Mapping with a range of fixed number of cores (40, 65, 90, 150, 250, 350), rather than comparing based on the optimal number of cores. We use NN2 with batch sizes 64 and 128 because NN2 has a moderate size, neither too small nor too deep. The parameters for ONoC and ENoC in Gem5 are set as follows. The packet size for both ONoC and ENoC is set to 64 bytes and 16 bytes/flit. The number of wavelengths used for ONoC is 64. The latency of hop by
hop routing in ENoC is set to 2 cycles. Shortest path routing is used for the 4-channel electric routers in ENoC.

Fig. 10(a) and (b) show the comparisons of performance and energy consumption between ONoC and ENoC for NN2 with batch size 64 and 128 respectively. It can be seen from Fig. 10 (a) that FCNN training time on ONoC is smaller than ENoC for both batch sizes. Compared with ENoC, the average time reductions for ONoC under batch size 64 and 128 are 21.02% and 12.95% respectively. That is because ONoC allows concurrent communications using WDM to deal with large volume of core-to-core communications resulting in less communication time. When the number of cores is increasing, the performance difference is becoming more obvious for both batch sizes, because ENoC has larger communication latency among cores due to increasing routing delays.

From Fig. 10(b), we can see that the energy consumption of ONoC is larger than ENoC when the number of cores is small (no more than 90 in the example), and much smaller than ENoC when the number of cores is large (more than 90 in the example). This is because the static power is dominant in ONoC when the number of cores is small, while the dynamic energy in ENoC caused by the communication overhead is increasing rapidly when the number of cores is increased. On average, the energy consumption of ONoC is reduced by 47.85% and 39.27% compared with ENoC under batch size 64 and 128 respectively.

In summary, the performance of our method on ONoC outperforms ENoC under different batch sizes, with more energy-efficiency especially when the number of cores is large.

6 RELATED WORK

There are many studies on parallel computing for neural network training with CPU, GPU, FPGA, ASIC, and etc. [30], which attempts to utilize the computing cores to accelerate neural networks. Due to the space limitation, we only show the related researches in the following aspects:

(1) Data Reuse Methods: The state-of-the-art neural network acceleration approaches are mostly based on data reuse methods. One data reuse method called weight reuse stashes the weight in the cache of cores during the training, which is used in co-processor design [31] and mobile co-processor designed for CNN training [32]. A second data reuse method is called output reuse, with the partial sum collected and maintained in the cache of cores, which is used in Shidiannao [33]. Another data reuse method called row reuse is proposed in Eyeriss [34], where the computation of any given CNN shape is mapped onto the PE array. Our work reuses outputs and weights by storing the neural network parameters in different cores’ SRAM distributively and reusing them in the back propagation.

(2) Neural Network Acceleration Architectures: To reduce average data latency and energy consumption, a mesh NoC is proposed for FCNN training [35]. To increase throughput and power efficiency, a 3D NoC architecture for ANN [36] and a NoC-based accelerator for CNN [34] are proposed. A microswitch NoC is proposed as a spatial neural network accelerator [37] with the consideration of latency, throughput, area and energy. More interestingly, a study on NoC based DNN accelerators [38] shows that the communication in neural networks accounts for the major delay in training and the memory accesses are accountable for most energy cost. All the above studies are based on ENoC, which has much higher latency and energy cost compared with ONoC.

(3) Mapping Methods: In [39], several models for mapping neural networks on ENoC are proposed to get the high performance. In [40], a mapping method is used by considering the wire-length between neurons for a TrueNorth neuromorphic system. In [41], mini-column used as basic functional element is mapped to each core, where each mini-column consists of 100 neurons. All of the above mapping strategies follow a sequential mapping scheme that maps neuron populations to cores one by one, which does not provide good performance for inter-neuron communications between different cores. Moreover, they cannot be applied to ONoC directly because they are not designed with the consideration of the ONoC’s properties, thus cannot take advantage of optical transmissions. Besides, there are some studies for ONoC mapping problem by designing wavelength assignment [42], or reducing crosstalk [43] and thermal sensitivity influence [44]. However, these approaches are all based on heuristic algorithm so they suffer from long training time to get the approximate optimal solution.

It is worth mentioning that there is no research on the optimization of parallel FCNN training through the computation and communication trade-off in the context of ONoC, which we develop to bridge the gap in this paper.
7 CONCLUSIONS

In this paper, we analyze a fine-grained parallel computing model to analyze the trade-off between communication and computation for training FCNN on ONoC with the objective of minimizing the total training time. Based on the model, we derive the optimal number of cores required for each training period in both forward propagation and backpropagation processes. We further present three mapping strategies (FM, RRM and ORRM) and compare their advantages and disadvantages with regard to hotspot level, memory requirement and state transitions. Simulation results show that the average prediction error on the optimal number of cores using NN benchmarks is within 2.3%. Extensive simulations demonstrate that our proposed methods can reduce FCNN training time by 22.28% and 4.91% on average compared with two traditional parallel computing methods, respectively. Compared with ENoC, our methods on ONoC can achieve 21.02% and 12.95% on reducing training time and 47.85% and 39.27% on saving energy under batch sizes 64 and 128, respectively. Future work can be conducted for model extensions to other neural networks or other ONoC topologies.

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