A 40nm CMOS Hysteretic Buck DC-DC Converter With Digital-Controlled Power-Driving-Track-Duration Current Pump

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ABSTRACT A fast-transient voltage-mode hysteretic buck converter with digital-controlled power-driving-tracked-duration (PDTD) auxiliary current pump is proposed. The pump injection current duration is digitally controlled by the driving signal of the power stage. It aims at enhancing the transient response time which is limited by the large inductor used in typical buck converters and reducing the multiple undershoot/overshoot effect encountered in conventional current pump injection technique. The converter has been fabricated using TSMC 40nm CMOS technology with the silicon area of 830 µm × 620 µm. The proposed converter regulates properly in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The measured output ripple is about 30mVpk and the switching frequency is about 1.45MHz. The peak efficiency is 93%. The measured load transient settling time for a 60-to-300mA/300-to-60mA load step change is 369ns/335ns, resulting in 350% faster than that of conventional counterpart without PDTD control scheme. The performance comparison with the representative state-of-art works has shown that the proposed converter shows good balance on performance metrics and the best figure-of-merit (FOM) in transient-response efficiency.

INDEX TERMS DC-DC buck converter, hysteretic control, fast-transient, current pump.

I. INTRODUCTION

In recent years, a rapid growth of portable devices, such as smartphones, tablets, laptops and digital cameras is resulted from the development of system-on-chip (SoC) [1]–[8] which have different energy requirements [6]–[9]. Concurrently, low power consumption is one of the primary design agenda for the battery-powered SoC [10]. Switching converters are widely used due to its high power-conversion efficiency [9]–[11]. Operating under different modes tends to be an effective method of reducing power consumption [12], [13]. As such, the embedded digital systems or microprocessors operating at high speed need to switch between different modes [14], [15]. During the dynamic loading change and the operation mode transfer, a massive load current change can induce a large undershoot/overshoot from the output voltage for a significantly long time owing to the transient regulation latency [12]. The undershoot voltage may cause missing of data and operation distortion under high speed scenario, whereas the overshoot voltage may contribute extra power loss and even damage the ambient devices and the overall chip. The long settling time limits the system mode switching frequency, and thus it may deteriorate the overall system performance and narrow its application scenarios [4]. In this prospective, fast-transient response becomes one of the key requirements for DC-DC converters in high performance applications [11], [16]–[19].

FIGURE 1 shows the block diagram of a DC-DC converter which comprises the power stage and the controller stage. The transient response is mainly constrained by the controller stage delay and the LC limitation of power stage [20]–[23]. Various techniques have been reported to achieve fast-transient response and reliable output voltage.
Some of them focus on speeding up the controller stage at the expense of increased system complexity. Although the adaptive bandwidth compensation techniques [24], [25] and the capacitor multiplier techniques [26] aim to extend the compensated bandwidth, their transient responses are still limited by the OTA bandwidth through the frequency compensation in compromising overall closed-loop stability. In addition, V^2 converters are successful by introducing the feedforward path to bypass the slow error amplifier (EA) [12], [18], [27], but this approach may suffer from the subharmonic oscillation [8], [27]. Regarding the hysteretic converters, they offer faster response time and better-guaranteed stability using these compensation-free controller stage [28]–[33]. Moreover, these converters can operate at Pulse Frequency Modulation (PFM) mode automatically under the light load conditions to reduce the frequency-dependent switching loss, thus improving the light load efficiency [27], [34]. However, the transient speed of existing hysteretic converters is still constrained by the inductor. To overcome this limitation, an auxiliary current pump is applied to bypass the inductor, compensating the load current change for enhanced transient response [35]–[39]. The prior reported analog control topology in [4] is applied to achieve an instant current injection and a smooth turning-off, but it requires careful design of compensation network for stability whilst at expense of circuit complexity. Transient improvement of the auxiliary current is degraded by the compensated bandwidth of the error amplifier control loop. Besides, several voltage-triggering current pump sources inject auxiliary current by detecting the output voltage directly, supporting fast auxiliary current injection [36]–[38]. However, without output tracked turning-off control, multiple undershoot/overshoot may be induced when the current pump sources are turned off instantly, thus deteriorating the expected transient performance and the system stability. Although digital slope control scheme can avoid instantly turning-off control for current pump [20], [39], it requires complicated components and topology. In this work, a fast-transient hysteretic buck converter with a digital-controlled Power-Driving-Tracker-Duration (PDTD) scheme for the auxiliary current pump source is proposed. The auxiliary current is injected and hold for a long enough time to optimize the transient improvement of the auxiliary current. The current duration is well-defined to track the output variation through the effective digital control method. Due to hysteretic based design, it can eliminate the need of compensation network as encountered in analog approach whilst it yields low cost design by using simple digital components. It overcomes the above stated drawbacks whilst providing the optimal performance tradeoff arising from the transient enhancement technique.

This paper is organized as follows. Section II presents the respective time-domain transient analysis for the conventional and proposed voltage-mode hysteretic DC-DC converters. Section III presents the system and circuit design of the proposed fast-transient DC-DC converter. Section IV shows the circuit and system implementation. Section V discusses the measurement results and the performance comparison with the representative reported works. Section VI gives the concluding remarks.

II. LOAD TRANSIENT RESPONSE ANALYSIS
In this Section, the undershoot transient response for the voltage-mode hysteretic converter is analyzed at the output node shown in Fig. 2(a) and Fig. 2(b). The current-voltage relationships in Fig. 2(a) are obtained as follows:

\[ I_R(t) = I_L(t) + I_C(t) \]  
\[ V_{out}(t) = V_C(t) - I_C(t)R_C \] (1) (2)

The transient behavior of the inductor current \( I_L(t) \) and the load current \( I_R(t) \) are assumed as:

\[ I_R(t) = \begin{cases} 
  m_1 t & 0 < t < t_{Edge} \\
  I_R & t_{Edge} < t < t_{Recover}
\end{cases} \]  
\[ I_L(t) = \begin{cases} 
  m_2 t & 0 < t < t_{Max} \\
  -m_3 t + (m_2 + m_3)I_{Max} & t_{Max} < t < t_{Recover}
\end{cases} \] (3) (4)

where \( m_1 \) and \( m_2 \) are the ramp-up slopes of \( I_R(t) \) and \( I_L(t) \), respectively and \( m_1 \gg m_2, m_3 \) is the falling slope of \( I_L(t) \). \( V_{OUT} \) is the designed dc output voltage and \( I_R = V_{OUT}/R \) is the corresponding load current at \( V_{OUT} \).

A. WITHOUT \( I_P \) (T)
The analysis is based on Fig. 2(a). and the case A timing waveforms are shown in Fig. 3. The key response waveforms are shown in Fig. 4.
1) REGION_A1: $0 < t < t_{\text{edge}}$

In this region, assuming $V_C(0) = V_{\text{out}}(0) = V_{\text{OUT}}$, we have

$$I_C(t) = \Delta m \times t$$

$$V_C(t) = -\frac{1}{2C} \Delta m t^2 + V_{\text{OUT}}$$

$$V_{\text{out}}(t) = -\frac{1}{2C} \Delta m t^2 - \Delta m R_C t + V_{\text{OUT}}$$

Where $\Delta m = m_1 - m_2$. Since $I_C(t) > 0$, the output capacitor $C$ is discharged and a negative $V_{\text{ESR}}(t)$ is induced across $R_C$. As a result, both $V_C(t)$ and $V_{\text{out}}(t)$ decrease within $[0, t_{\text{edge}}]$, causing large undershoot variation. If $I_R(t)$ ramps very rapidly where $\frac{dt}{dt} \ll R_C$ can be easily fulfilled, then

$$V_{\text{out}}(t) \approx -\Delta m R_C t + V_{\text{OUT}}$$

The output variation $\Delta V_{\text{out}}(t) = V_{\text{OUT}} - V_{\text{out}}(t)$ mainly consists of the negative $V_{\text{ESR}}(t)$ and hence $V_{\text{out}}(t)$ decreases linearly.

2) REGION_A2: $t_{\text{edge}} < t < t_{\text{Max}}$

$$I_C(t) = -m_2 t + I_R$$

$$V_C(t) = \frac{1}{2C} m_2 t^2 - \frac{I_R}{C} t + \frac{I_R^2}{2m_1 C} + V_{\text{OUT}}$$

$$V_{\text{out}}(t) = \frac{1}{2C} m_2 t^2 + (m_2 R_C - \frac{I_R}{C}) t - I_R R_C + \frac{I_R^2}{2m_1 C} + V_{\text{OUT}}$$

$$I_C(t)$$ is decreasing, and $I_C(t) = 0$ when $I_L(t) = I_R$. Solving $dV_C(t)/dt = 0$ to yield $t_{\text{Equal}} = I_R/m_2$. Hence, at $t = t_{\text{Equal}}$, we have

$$V_C(t) = V_{\text{OUT}} - \frac{\Delta m I_R^2}{2m_1 m_2 C}$$

Similarly, solving $dV_{\text{out}}(t)/dt = 0$ to yield $V_{\text{out}}(t)_{\text{min}}$ at the time $t_{\text{min}} = I_R/m_2 R_C$, we have

$$V_{\text{out}}(t)_{\text{min}} = V_{\text{OUT}} - \frac{\Delta m I_R^2}{2m_1 m_2 C} - \frac{m_2 R_C^2}{2}$$

The undershoot variation $\Delta V_{\text{UN}}$ is obtained as follows:

$$\Delta V_{\text{UN}} = V_{\text{OUT}} - V_{\text{out}}(t)_{\text{min}} = \frac{m_2 R_C^2}{2}$$

Since $V_{\text{out}}(t)$ of the voltage-mode hysteretic converter is regulated by itself, when $t > t_{\text{Equal}}$, $V_{\text{out}}(t)$ rises continuously until $V_{\text{out}}(t)$ reaches the high-side boundary of the window comparator $V_H$. The settling time $t_{\text{Settle}}$ is assumed when $V_{\text{out}}(t) = V_{\text{OUT}}$. As such, the settling time expression is obtained as

$$t_{\text{Settle}} = \sqrt{\frac{2C \Delta V_{\text{UN}}}{m_2} + \frac{I_R}{m_2} - R_C C}$$

When, $V_{\text{out}}(t) = V_H$, we have

$$t_{\text{Max}} = \sqrt{\frac{2C(\Delta V_{\text{WIN}} + \Delta V_{\text{UN}})}{m_2} + \frac{I_R}{m_2} - R_C C}$$

$\Delta V_{\text{WIN}}$ is the hysteretic window, given by $\Delta V_{\text{WIN}} = V_H - V_{\text{OUT}}$.

3) REGION_A3: $t_{\text{Max}} < t < t_{\text{Recover}}$

In this region, the $I_L(t)$ ramps down and we have

$$I_C(t) = m_3 t + [I_R - (m_2 + m_3) t_{\text{Max}}]$$

In this case, $I_C(t) < 0$ and it continuously charges up $C$. When $t = t_{\text{Recover}}$, $I_C(t) = 0$ and $V_{\text{out}}(t_{\text{Recover}}) = V_C(t_{\text{Recover}})$. At this juncture, $I_C(t)$ finishes one complete discharging and charging cycle after the change of load current.

Table 1 summarizes the time domain expressions for key parameters. Both $\Delta V_{\text{UN}}$ and $t_{\text{Settle}}$ are highly dependent on the load current magnitude $I_R$. The transient performance can be improved by reducing $I_R$. Of particular noted, the $I_R$ is the magnitude value over $[I_{\text{Edge}}, I_{\text{Recover}}]$. This gives the proposed improvement by means of adding the current pump $I_P(t)$, as illustrated in Fig. 2(b), to bypass $L$ so as to compensate the change of $I_L(t)$. In order to enhance the transient performance, the $I_P(t)$ in this work is designed to be hold until $I_{\text{End}}$ as indicated in Fig. 3.
TABLE 1. Transient parameters for Case A and Case B.

| Parameters | Case A [Without Ir(t)] | Case B [With Ir(t)] |
|------------|------------------------|---------------------|
| $V_C(t)_{\text{min}}$ | $V_{\text{sat}} - \frac{\Delta m^2 t}{2m_mC}$ | $V_{\text{sat}} - \frac{\Delta m^2 t}{2m_mC}$ |
| $V_{\text{out}}(t)_{\text{min}}$ | $V_{\text{sat}} - \frac{\Delta m^2 t}{2m_mC} - \frac{m_1 C R_C t^2}{2}$ | $V_{\text{sat}} - \left[ \frac{I_R^2}{2m_mC} + \frac{m_1^2 R_C^2}{2} \right] - \frac{m_1 t^2_{\text{Edge}}}{2C}$ |
| $AV_{UN}$ | $\frac{\Delta m^2 t}{2m_mC} - \frac{m_1 C R_C^2}{2}$ | $\frac{\Delta m^2 t}{2m_mC} - \frac{m_1 C R_C^2}{2}$ |
| $t_{\text{Settle}}$ | $\frac{2C V_{\text{sat}}}{m_3} \left( \frac{1}{m_2} - R_C \right)$ | $\frac{2C V_{\text{sat}}}{m_3} \left[ \frac{1}{m_2} - R_C \right] + \frac{t_{\text{Edge}}^2}{m_3} - R_C$ |
| $k$ | N.A. | $k = \frac{m_0 t^2_{\text{Edge}} - m_1 t_{\text{Edge}}^2}{2C} + V_{\text{sat}}$ |

B. WITH PTD T $I_P(t)$

The analysis is based on Fig. 2(b) and the Case B timing waveforms in Fig. 3. The key response waveforms are shown in Fig. 5. In this case, the $I_P(t)$ in $[0, t_{\text{End}}]$ is described as

$$I_P(t) = \begin{cases} 
  m_2 t & 0 < t < t_P \\
  I_P & t_P < t < t_{\text{End}} \end{cases}$$ (18)

1) REGION B1: $0 < t < t_{\text{Edge}}$

$$I_C(t) = \Delta m^2 t$$ (19)
$$V_C(t) = -\frac{1}{2C} \Delta m^2 t^2 + V_{\text{OUT}}$$ (20)
$$V_{\text{out}}(t) = -\frac{1}{2C} \Delta m^2 t^2 - \Delta m^2 R_C t + V_{\text{OUT}}$$ (21)

If $t_{\text{Edge}} < R_C$, we have

$$V_{\text{out}}(t) \approx -\Delta m^2 R_C t + V_{\text{OUT}}$$ (22)

where $\Delta m^2 = m_1 - m_2 - m_4$ and $\Delta m' < \Delta m$. With the injected $I_P(t)$, a smaller $I_C(t)$ is required to compensate the change of $I_L(t)$ while $V_C(t)$ and $V_{\text{out}}(t)$ become larger. This is because $I_P(t)$ helps to compensate the change of $I_L(t)$, reducing the discharge current $I_C(t)$. Consequently, $V_C(t)$ decreases with a smaller rate and $\Delta V_{\text{ESR}}$ becomes smaller, leading to reduced $\Delta V_{\text{UN}}$.

2) REGION B2: $t_{\text{Edge}} < t < t_P$

In this region, $I_P(t) = I_R$ while $I_P(t)$ keeps on increasing. As a result, $I_C(t) = I_R m_4 t$ is reducing and the same goes for $I_C(t)$. The corresponding transient relationship for $I_C(t)$, $V_C(t)$ and $V_{\text{out}}(t)$ can be obtained as follows:

$$I_C(t) = -m_2^2 t + I_R$$ (23)
$$V_C(t) = \frac{1}{2C} m_2^2 t^2 - \frac{I_R}{C} t + \frac{m_1 t_{\text{Edge}}^2}{2C} + V_{\text{OUT}}$$ (24)
$$V_{\text{out}}(t) = \frac{m_2^2 t^2}{2C} + \frac{m_1 R_C C - I_R}{C} t + \frac{m_1 t_{\text{Edge}}^2 - 2 I_R R_C}{2C} t + V_{\text{OUT}}$$ (25)

where $m_2^2 = m_2 + m_4$. Solving $dV_C(t)/dt = 0$ to yield $t = t_{\text{Edge}} + I_R / m_2$, we have

$$V_C(t)_{\text{min}} = -\frac{I_R^2}{2m_2 C} + \frac{m_1 t_{\text{Edge}}^2}{2C} + V_{\text{OUT}}$$ (26)

Solving $dV_{\text{out}}(t)/dt = 0$, it yields $t_{\text{min}} = t_{\text{Edge}} - R_C C$, assuming $t_{\text{min}} > t_{\text{Edge}}$ we have

$$V_{\text{out}}(t)_{\text{min}} = -\left[ \frac{I_R^2}{2m_2 C} + \frac{m_1 R_C^2 C}{2} \right] + \frac{m_1 t_{\text{Edge}}^2}{2C} + V_{\text{OUT}}$$ (27)

Comparing with Case A, $I_C(t)$ decreases with a larger slope in this region. $V_C(t)_{\text{min}}$ becomes larger. Equation (27) indicates $V_{\text{out}}(t)_{\text{min}}$ varies with respect to $m_2$, in which $m_2 = m_2 + m_4$, and it gives $\frac{\delta V_{\text{out}}(t)_{\text{min}}}{\delta m_3}$ over $[0, I_R R_C C - m_2]$. Assumed that $t_{\text{min}} > t_{\text{Edge}} > 0$, we have $m_3 < I_R R_C C - m_2$. Hence, $V_{\text{out}}(t)_{\text{min}}$ increases with respect to $m_4$ over $[0, I_R R_C C - m_3]$ and becomes larger in Case B, and hence the $\Delta V_{\text{UN}}$ is reduced through $I_P(t)$.

3) REGION B3: $t_p < t < t_{\text{Max}}$

In this region, $I_P(t) = I_P$ and the equivalent output current $I_{\text{Eq}}(t) = I_R - I_P$. The corresponding transient relationship for $I_C(t)$, $V_C(t)$ and $V_{\text{out}}(t)$ can be obtained as follows:

$$I_C(t) = -m_2^2 t + I_{\text{Eq}}$$ (29)
$$V_C(t) = \frac{m_2^2 t^2}{2C} - \frac{I_{\text{Eq}} t}{C} + \frac{m_1 t_{\text{Edge}}^2}{2C} + V_{\text{OUT}}$$ (30)
$$V_{\text{out}}(t) = \frac{m_2^2 t^2}{2C} - \frac{I_{\text{Eq}} t}{C} + m_2 R_C t$$
$$- \frac{I_{\text{Eq}} R_C}{C} + \frac{m_1 t_{\text{Edge}}^2}{2C} + V_{\text{OUT}}$$ (31)

In this region, $I_C(t) < 0$, $C$ is charged up. Both $V_C(t)$ and $V_{\text{out}}(t)$ rise with an increasing slope over $[t_P, t_{\text{Max}}]$. As such, the transient settling time will be significantly reduced.
This gives
\[ t_{\text{Settle}} = \sqrt{\frac{2C(V_{\text{OUT}} - k)}{m_2} + \left(\frac{I_{\text{Eq}}}{m_2}\right)^2 + \frac{I_{\text{Eq}}}{m_2} - R_C C} \]  
\[ (32) \]

When \( V_{\text{out}}(t) = V_H \), the time becomes
\[ t'_{\text{Max}} = \sqrt{\frac{2C(V_H - k)}{m_2} + \left(\frac{I_{\text{Eq}}}{m_2}\right)^2 + \frac{I_{\text{Eq}}}{m_2} - R_C C} \]
\[ (33) \]
where \( k \) is a constant and \( k = -\frac{m_2 I_{\text{P}}}{2C} + \frac{m_1 I_{\text{Edc}}}{2C} + V_{\text{OUT}} \). Comparing with Case A, we have \( I_{\text{Eq}} < I_R \), and it can be proved that \( t'_{\text{Settle}} < t_{\text{Settle}} \) with \( I_P < I_R \).

4) REGION B4: \( t_{\text{Max}} < t < t_{\text{End}} \)
In this region, \( I_L(t) \) decreases. \( I_C(t) < 0 \) and it is given as
\[ I_C(t) = m_3 t + [I_{\text{Eq}} - (m_2 + m_3) t'_{\text{Max}}] \]
\[ (34) \]

The \( I_C(t) \) continuously charges up \( C \). When \( t = t'_{\text{Recover}} \), \( I_C(t) = 0 \) and \( V_{\text{out}}(t'_{\text{Recover}}) = V_C(t'_{\text{Recover}}) \). At this juncture, \( I_C(t) \) finishes one complete discharging and charging cycle after the change of load current. The transient parameters in Case A and Case B are summarized in Table 1. It proves that both \( \Delta V_{\text{UN}} \) and \( t_{\text{Settle}} \) can be reduced through holding on the \( I_P(t) \).

III. CIRCUIT AND SYSTEM IMPLEMENTATION
Fig. 6 illustrates the whole system architecture of the voltage-mode hysteretic buck converter with the proposed PDTD control stage. The output capacitor is required to have a large ESR value to provide sufficient output voltage ripple \( \Delta V_{\text{out}}(t) \). As suggested in [31], [40], the required minimum ESR value can be estimated by
\[ R_C > \frac{1}{\sqrt{\frac{L(V_H - V_L)}{C} \left(\frac{1}{V_{\text{IN}} - V_{\text{OUT}}} + \frac{1}{V_{\text{OUT}}}\right)}} \]
\[ (35) \]

where \( V_L \) is the low-side boundary of the window comparator and the other symbols have been defined before. With the large ESR, \( V_{\text{out}}(t) \) is dominated by the \( V_{\text{ESR}}(t) \) and it is fed to the hysteresis comparator, generating the voltage signal \( V_{\text{WIN}} \) as well as the adaptive control signals of undershoot/overshoot detection circuit, \( ON_{\text{UN}} \) and \( ON_{\text{OV}} \). \( V_{\text{WIN}} \) is used to regulate \( I_L(t) \) through controlling the power transistors. The PFM control is added to improve the light load efficiency. Dual current pump sources are employed to compensate the large current difference between \( I_R(t) \) and \( I_L(t) \). They are triggered by the undershoot/overshoot detection signal. The \( I_P(t) \) turning-on duration is modulated by the power-driving-tracked-hold stage whereas the turning-off mechanism is controlled by the hold-period delayed ramping generator. The detailed circuit implementation of the proposed transient enhanced stage will be described in the following sub-sections.

A. UNDERSHOOT/OVERSHOOT DETECTION STAGE
In this work, the undershoot/overshoot is detected through a pair of adaptively-biased comparators [41]. As shown in Fig. 7, the adaptive biasing signals \( ON_{\text{UN}} \) and \( ON_{\text{OV}} \) are generated through the hysteretic comparator. They are added to reduce the standby power consumption of the undershoot and overshoot detection comparators. Once \( V_{\text{FB}} \) is larger than the overshoot detection reference \( V_{\text{OVHI}} \), the \( OV \) goes high. When \( V_{\text{FB}} \) is smaller than the undershoot detection reference \( V_{\text{UL}} \), \( UN \) goes to high.

B. POWER-DRIVING-TRACKED-HOLD STAGE
In this work, the \( I_P(t) \) hold-on duration is designed to track \( V_{\text{out}}(t) \) variation such that a sufficient hold-on duration is guaranteed to enhance the transient response. In the meantime, once \( V_{\text{out}}(t) \) settles down, \( I_P(t) \) will be turned off to save power.
This methodology is realized through the power-driving-tracked-hold stage in Fig. 8. It consists of two sub-stages: (1) wide pulse trigger stage with an exclude stage logic which is formed by the cross-coupled NAND gates and (2) pulse duration control stage.

The wide pulse trigger stage is to extend the undershoot/overshoot detection signal UN/OV such that it provides a long enough turning-on duration for \( I_P(t) \). The endpoint of wide pulse signal \( WP_{UN}/WP_{OV} \) is determined by the pulse duration control stage, which detects \( V_{out} \) by monitoring the power transistor driving voltage \( P \) and \( N \). The exclude stage logic is to guarantee that \( UN \) and \( OV \) are exclusively extended. \( WP_{UN}/WP_{OV} \) is the inverting signal of \( WP_{UN}/WP_{OV} \). \( EN_{UN} \) and \( EN_{OV} \) are the pulse duration detection signals for the narrow and wide pulse trigger stage, respectively. \( EN_{UN} \) and \( EN_{OV} \) are the output signals of the dual pulse hold stage for undershoot/overshoot.

C. WIDE PULSE TRIGGER STAGE

In Fig. 7, the \( UN/OV \) state of output signal changes whenever \( V_{FB} \) crosses \( V_{HH}/V_{LL} \), giving fast detection speed. However, this narrow \( UN/OV \) pulse output causes insufficient turning-on duration for \( I_P(t) \). To guarantee fast detection as well as sufficient turning-on duration, the turning-on and turning-off mechanism of \( I_P(t) \) is separated in this work. This is realized through the pulse duration control stage as illustrated in Fig. 9.

When \( EN_{UN} = 1 \), the equivalent wide pulse trigger stage is shown in Fig. 10(a). When \( V_{FB} < V_{LL} \), the narrow detection pulse \( UN \) goes to high, setting \( WP_{UN} \) to 0 and \( WP_{OV} \) to high. When \( V_{FB} > V_{HH} \), \( UN \) drops to 0. Due to the feedback logic, \( WP_{UN} \) will be latched to 0 by itself and the \( WP_{UN} \) is kept at high. In this case, a wide pulse \( WP_{UN} \) can be triggered by the narrow \( UN \) pulse and the pulse duration of \( WP_{UN} \) is independent of \( UN \). When \( EN_{UN} = 0 \), the equivalent circuit is shown in Fig. 10(b). In this case, \( EN_{UN} \) will cut off the logic path and set the wide pulse \( WP_{UN} \) to 0 regardless of \( UN \) state. The narrow trigger pulse \( UN \) is extended to a wide pulse \( WP_{UN} \) to provide sufficient hold-on duration for current pump \( I_P(t) \). The rising edge of \( WP_{UN} \) is only triggered by \( UN \) when \( EN_{UN} = 1 \). On the other hand, the falling edge of \( WP_{UN} \) is only controlled by the falling edge of \( EN_{UN} \). In this way, the turning-on and turning-off mechanism of \( I_P(t) \) is then separated. The falling edge of \( EN_{UN} \) is realized through the pulse duration control stage.

D. PULSE DURATION CONTROL STAGE

To improve the transient response of the voltage-mode hysteretic DC-DC converter, \( I_P(t) \) is required to be hold for a long enough time. After \( V_{out} \) (recover) back, \( I_P(t) \) is required to be turned off to save power. In this work, the endpoint of \( I_P(t) \) duration is designed to be at \( t_{end} \) in Fig. 3. In the voltage-mode hysteretic buck converter, a large ESR value is required to keep \( V_{out} \) in phase with \( I_L(t) \) and \( I_L(t) \) is directly controlled by the power PMOS/NMOS transistor. Hence, the endpoint \( t_{end} \) can be determined by monitoring the power PMOS/NMOS transistor driving voltage \( P/N \). This is realized through the circuit as depicted in Fig. 11.
Once a large undershoot is detected, the $\overline{\text{HOLD}}$ will be triggered to logic 0, discharging the capacitor $C_{\text{RAMP}}$ rapidly through the large size $M_N$. As a result, $\overline{\text{V}}_{\text{RAMP}}$ is pulled down instantly whereas $I_p(t)$ is triggered on instantly to enhance the transient response. After $V_{\text{out}}(t)$ recovers back, $\overline{\text{HOLD}}$ is reset to high at $t_{\text{End}}$ instantly to cut off $I_p(t)$. Different from the $\overline{\text{HOLD}}$, a ramping period is generated in $\overline{\text{V}}_{\text{RAMP}}$ by a relatively small constant current $I_{\text{Charge}}$ to slow down the $I_p(t)$ changing rate. If $I_p(t)$ can compensate the change of $I_p(t)$, the multiple undershoots/overshoots will be significantly reduced or even eliminated. The ramp-up rate of $\overline{\text{V}}_{\text{RAMP}}$ is given as follows:

$$\frac{d\overline{\text{V}}_{\text{RAMP}}(t)}{dt} = \frac{I_{\text{Charge}}}{C_{\text{RAMP}}}$$

(36)

F. DUAL CURRENT PUMP SOURCE

As shown in Fig. 13, either the current pump $I_{p,\text{UN}}$ or $I_{p,\text{OV}}$ is injected to the output node directly. Both $I_{p,\text{UN}}$ and $I_{p,\text{OV}}$ are designed to be supply independent through the constant biasing current $I_1$ to $I_3$. $S_1$ to $S_3$ are controlled by the ramping voltage for undershoot or overshoot. Hence, $I_{p,\text{UN}}/I_{p,\text{OV}}$ can be instantaneously turned on to enhance the transient response and slowly turned off to reduce the multiple undershoot/overshoot. During the steady state, $S_1$ to $S_3$ are turned on, pulling $V_{P_1}$, $V_{P_2}$ and $V_{P_3}$ up to $V_{DD}$ while pulling $V_{N_1}$ and $V_{N_2}$ down to ground. In this way, $I_{p,\text{UN}}$ and $I_{p,\text{OV}}$ can be totally off to save power. $I_1$ and $I_3$ are always on to speed up the current pump startup process. $I_2$ and $I_4$ are adaptively controlled by $S_6$ and $S_7$ to reduce the quiescent current.

G. DCM OPERATION

The DCM control algorithm is added to eliminate the reverse current, thus improving the light load efficiency [5]. The reverse current detection is realized by the common gate comparator [42]. A large size free-wheel switch (FWS) transistor is added to reduce the ring effect when both NMOS and PMOS are turned off [43].

IV. RESULTS AND DISCUSSIONS

The proposed converter has been fabricated using TSMC 40nm CMOS process which is suitable for low-voltage SoC applications, the micrograph is shown in Fig. 14. The occupied silicon area is $830\mu\text{m} \times 620\mu\text{m}$. Other support blocks...
TABLE 2. Performance comparison with the reported works.

|     | [11] JSSC 2015 | [27] TCAD 2015 | [33] ISSCC 2015 | [6] JSSC 2015 | [44] TVLSI 2016 | [20] TVLSI 2017 | [21] TVLSI 2018 | [22] TPE 2018 | [33] TCAS 2019 | This Work |
|-----|----------------|----------------|-----------------|--------------|----------------|----------------|----------------|---------------|-------------|-----------|
| P (nm) | 350 | 350 | 350 | 40 | 350 | 130 | 350 | 28 | 65 | 40 |
| V in (V) | 2.7-4.2 | 2.7-4.2 | 2.7-4.5 | 2.7-3.6 | 2.4-3.6 | 3.3 | 2.6-4.0 | 3.3 | 3.3 | 1.2-2.5 |
| V out (V) | 0.8-2.4 | 1.2 | 2 | 0.8-2.1 | 0.2-3.3 | 1.2-1.8 | 1.2 | 1.05 | 1-2.5 | 0.6-2.1 |
| I p (mA) | <2000 | 18-700 | N.A | <900 | 600 | 1250 | 600 | 0.3-1.7 | 900 | 450 |
| ΔV acc (mV) | 10‖ | 15 | 150 | 30‖ | 15 | 12‖ | 45 | 6 | 40‖ | 30 |
| L (μH) | 1 | 2.2 | 4.7 | 4.7 | 4.7 | 0.9 | 4.7 | 1 | 4.7 | 4.7 |
| C (μF) | 4.7 | 10 | 10 | 4.7 | 10 | 0.9 | 4.7 | 1 | 4.7 | 4.7 |
| Freq (MHz) | 1.25 | 300 | 400 | 100 | 450 | 1250 | 300 | 1400 | 450 | 240 |
| M (mA) | 0.9 | 5 | 3 | 4.8 | 15 | 2.1 | 0.22 | 2.5 | 4 | 0.369 |
| V out (mV) | 25 | 48 | 35 | 30 | >120 | 72 | 167 | 75 | 65 | 73 |
| V in (mV) | 0.9 | 5 | 3 | 4.8 | 15 | 3.5 | 0.15 | 2.8 | 5 | 3 | 0.335 |
| V out (V) | 35 | 30 | 38 | 30 | >160 | 33 | 180 | 90 | 70 | 72 |
| η peak (%) | 90 | 95.7 | 95.5 | 89 | 91 | 83.6 | 90 | 94 | 92 | 93 |
| η peak (%) | 0.254 | 0.264 | 0.757 | 4.5 | 1.853 | 0.08 | 3.261 | 1.246 | 0.375 | 0.106 |

FOM = \frac{Δt(μs) \times ΔV acc (mV) \times C(μF)}{L(μH) \times ΔI p (mA)}

where \( Δt = \frac{ΔI L \cdot H + ΔI L \cdot H}{2} \) and \( ΔV acc = \frac{ΔV out + ΔV in}{2} \)

FIGURE 14. Micrograph of the proposed fast-Transient converter.

such as dead time control, over-current protection and soft start circuits are also realized in the DC-DC converter in order to protect the overall system and maintain the power efficiency. The fabricated fast-transient DC-DC buck converter has been tested with the input voltage of 2.5V and the nominal output voltage of 1.2V. The output capacitor is 4.7μF and the inductor is 4.7μH.

A. STEADY-STATE MEASUREMENT
The steady-state measurement results for CCM and DCM are illustrated in Fig. 15(a) and Fig. 15(b), respectively. Fig. 15(a) shows the steady-state waveforms of the output voltage \( V out(t) \) and the inductor current \( I L(t) \) at the load current of 60mA. It has validated that the proposed converter can regulate properly in CCM. The output ripple is about 30mV pk whereas the switching frequency is about 1.45MHz. It also shows that the \( V out(t) \) is in phase with the \( I L(t) \) because of the large ESR in the voltage-mode hysteretic converter as discussed in Section III. Fig. 15(b) shows the waveforms of the output voltage \( V out(t) \), the inductor current \( I L(t) \) and the switching node voltage \( V X(t) \) at the load current of 20mA. It has confirmed the design methodology of the DCM operation. During the light load condition, the reverse current can be detected and eliminated. The ringing at the output node can be significantly reduced by applying the FSW control. As a result, the light load efficiency is improved. The efficiency at different load currents is plotted in Fig. 16. The peak efficiency \( η peak \) is 93% at 60mA at \( V out = 1.2V \). Finally, due to the PFM control of hysteretic converters under DCM, the light load efficiency at 20mA is close to 90%.

B. TRANSIENT RESPONSE MEASUREMENT
For the conventional hysteretic buck converter without the \( I P(t) \), the undershoot and overshoot transient response

FIGURE 15. Steady state waveforms in (a)CCM; (b)DCM.
FIGURE 16. Power Efficiency at Different Load Currents at $V_{\text{out}} = 1.2\text{V}$.

FIGURE 17. Output Transient Responses for (a) Step-Up Load Change, (b) Step-Down Load Change without $I_P(t)$.

for the 60-to-300mA and 300-to-60mA load current change under the load current control signal $V_{\text{step}}(t)$ is illustrated in Fig. 17(a) and Fig. 17(b), respectively. The edge time of the current load step is about 5ns. The undershoot/overshoot variation $\Delta V_{\text{UN}}/\Delta V_{\text{OV}}$ is 128mV/127mV whereas the undershoot/overshoot transient settling time $t_{L-H}/t_{H-L}$ is 1.31µs/1.185µs.

For the hysteretic buck converter with PDTD $I_P(t)$, the undershoot/overshoot transient response for the 60-to-300mA/300-to-60mA load current change is depicted in Fig. 18(a) and Fig. 18(b), respectively. In comparison to the conventional counterpart, the undershoot/overshoot variation $\Delta V_{\text{UN}}/\Delta V_{\text{OV}}$ is reduced to 73mV/72mV whereas the transient settling time $t_{\text{Settle}}$ is improved to 369ns/335ns. This suggests that the proposed work offers 350% faster than that of the conventional counterpart, validating the effectiveness of the PDTD control scheme.

C. PERFORMANCE COMPARISON

Table 2 shows the performance comparison of the converter with the reported state-of-art works. In order to compare the transient-response effectiveness under different settings and load transient steps, a normalization based FOM is established. It includes the LC components value, the average setting time $\Delta t$, the average voltage $\Delta V_{\text{spike}}$ and the load transient step $\Delta I_L$. This FOM takes both transient settling time and transient spike voltage into consideration. It also normalizes the LC component effect under different load steps. The smaller FOM gives better transient response performance. The proposed method has achieved an excellent FOM value and peak efficiency simultaneously. It has demonstrated the converter provides fast transient response together with balanced performance metrics.

V. CONCLUSION

The analysis, design and circuit implementation of the voltage-mode hysteretic DC-DC buck converter using the digital-based PDTD control scheme for generating well-defined digital-controlled auxiliary current pump are presented. The measurement results have shown that the converter regulates properly in both CCM and DCM. With freewheel switch control, the ringing at the output node can be significantly reduced. Through the PDTD control scheme, the transient response time of the voltage-mode hysteretic DC-DC buck converter can be significantly reduced with respect to most of representative prior-art topologies. Not only does it provide sufficient turning-on duration of the current pump to speed up the transient response, it also reduces the multiple undershoot/overshoot significantly whilst maintaining reasonable ripple voltage and efficiency at low output voltage to yield the balance performance metrics. Compared with conventional converter without PDTD control scheme, it improves the transient response time by 350%.
Hence, the proposed digital-based PTDT current pump technique is very useful for realizing fast-transient response in DC-DC buck converters.

ACKNOWLEDGMENT

The authors would like to thank MediaTek, Singapore for the scholarship and the sponsorship of chip fabrication.

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