High-throughput GPU layered decoder of multi-edge type low density parity check codes in continuous-variable quantum key distribution systems

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ABSTRACT

The decoding throughput in the postprocessing is one of the bottlenecks for a continuous-variable quantum key distribution (CV-QKD) system. In this paper, we propose a layered decoder to decode quasi-cyclic multi-edge type LDPC (QC-MET-LDPC) codes based on graphic processing unit (GPU) in continuous-variable quantum key distribution (CV-QKD) systems. We optimize the storage method of the parity check matrix, merge the sub-matrices which are unrelated, and decode multiple codewords in parallel on GPU. Simulation results demonstrate that the average decoding speed of LDPC codes with three typical code rates, i.e., 0.1, 0.05 and 0.02, is up to 64.11 Mbits/s, 48.65 Mbits/s and 39.51 Mbits/s, respectively, when decoding 128 codewords of length $10^6$ simultaneously without early termination.

Introduction

In the current data-driven era, the demand of secret communications has been increasingly desired. A straightforward approach to secret communications is achieved by encryption techniques. However, encryption with the key, which is established with algorithms based on the assumptions of computation complexity, may no longer guarantee data security, as the large-scale universal quantum computer being reachable.

Quantum key distribution (QKD), which establishes a secret key between two remote participants based on quantum mechanics principles, can provide the guaranteed security between two participants by using a one-time-pad encryption algorithm to encrypt and decrypt data. So far, QKD has been quickly developed in both theory and experiment since the groundbreaking work of Bennett and Brassard in 1984, and become one of the most mature branches of quantum information technologies.

There exist two categories of QKD. One is the discrete variable QKD (DV-QKD) where the key information is encoded on discrete Hilbert space, such as the polarization or phase of single photon pulse, the other is the continuous variable QKD (CV-QKD) where the key information is encoded on continuous Hilbert space, such as the quadratures of coherent states. Compared with the DV-QKD which is based on single-photon preparation and detection, CV-QKD can directly utilize the standard telecommunication technologies (such as coherent detection), and hence has more potential advantages in practice.

Generally, the two participants in a CV-QKD system desire to establish a secret key for a long distance with a very low signal-to-noise ratio. Then it naturally raises a problem on designing codes with good error-correction performance, under such a stringent channel condition. In this case, only low-rate codes with very long block lengths can be exploited to achieve high efficiency key reconciliation.

Low density parity check (LDPC) codes have been shown to possess Shannon-limit approaching error-correction performance, and they have also been broadly applied in various communication systems, such as the DVB-S2 standard and the Enhanced Mobile Broadband (eMBB) data channels for 5G New Radio. Chung et al. designed an irregular LDPC code of length $10^7$ which achieves within 0.04 dB of the Shannon limit. Consequently, LDPC codes with long block lengths have become one of the most promising candidates for a CV-QKD system. Herein, multi-edge-type (MET) LDPC codes have attracted much attention due to their excellent performance.
The authors of Ref.\textsuperscript{7} reported a random MET-LDPC code with rate 0.1, where the decoding speed was up to 7.1Mbits/s using a graphic processing unit (GPU) implementation at signal-to-noise ratio (SNR) = 0.161, in a CV-QKD system. In Ref.\textsuperscript{8}, the authors employed a quasi-cyclic (QC) MET-LDPC code of expansion factor 512 and rate 0.1, where the simulation results demonstrated that the decoding speed was up to 9.17Mbits/s under the early termination condition at SNR = 0.161. Note that if the messages of the degree-1 variable nodes are updated only once at the end of the iterative decoding procedure, the decoding speed of the rate-0.1 MET-LDPC code can be up to 30.39Mbits/s when SNR = 0.161 and 64 codewords are decoded simultaneously\textsuperscript{9}.

One of main bottlenecks that restrict the secret key rate of an LDPC-coded CV-QKD system is the throughput of the belief-propagation (BP) decoder in the postprocessing of CV-QKD. This is because successful decoding at very low SNR requires a large number of iterations. Towards this end, the layered BP algorithm\textsuperscript{10} can be utilized to speed up the decoding convergence. In addition, a large expansion factor is employed when constructing QC-MET-LDPC codes in order to making full use of the parallel computing ability of GPU.

When implementing the GPU-based layered BP decoder, we optimize the storage of the matrix message by merging bits into one number, and combine two processes into one kernel to complete a whole iteration. As a consequence, it reduces the computation amounts. We also merge the unrelated sub-matrices because they do not affect each other and can thus be computed simultaneously by threads. The speed of our layer decoder is up to 64.11Mbits/s for a code of length $10^6$ and rate 0.1 under the condition of SNR = 0.161, 50 iterations without early termination.

Results

Based on the fact that the LLR messages update at variable/check nodes can be performed in parallel, the layered BP decoding algorithm is deployed on GPU. This section optimizes the GPU implementation of layered BP decoding algorithm.

The decoder implementation is optimized in such a way that the LLR is stored in global memory for coalesced access. For memory access in a warp, coalesced access means that the data address of a thread always keeps the same as the thread index, instead of the unordered access. Since the GPU kernel is executed by a warp consisting of 32 threads, the decoding latency can be hidden well for a code with length being a multiple of 32. The layered BP decoder has a coalesced global memory access, and stores the parity-check matrix in one file for indexing the corresponding LLR messages. Such a file denoted by $H_{\text{compact}}$, will be applied in calculating the LLR messages related to the check nodes. Each element in file $H_{\text{compact}}$ contains three pieces of information: the amount of the shift, the position of the element after row rearrangement in the base matrix, and the position of the column where the non-negative element located in the base matrix. For example, Fig. 1 displays a 4-by-8 base matrix with an expansion factor of 100. Each non-negative element of the base matrix $H$ in Fig. 1-(a) indicates the amount of shift and ‘-1’ represents an all-zero matrix. The second information indicating the position of the element after row rearrangement is demonstrated in Fig. 1-(b). Then, one sub-matrices shown in Fig. 1-(c) are used for indexing the needed messages. Accordingly, the one-dimensional matrix on the right side in Fig. 1-(c) represent the degrees of the base matrix (i.e., each element of the the one-dimensional matrix represents the number of elements non negative 1 in the corresponding column of the base matrix).

The GPU-based layered BP decoder updates the LLR messages of variable nodes and check nodes simultaneously, and it also enables us to decode multiple codewords in parallel. For each individual codeword, the required number of GPU threads is the same as the number of check nodes in a sub-matrix. Each thread computes the LLR messages received from the neighboring variable nodes, and also calculates the LLR messages for each adjacent variable node. This procedure is illustrated in Fig. 2 by taking an LDPC code with 4 check nodes and 6 variable nodes as an example. It is worth noting that at each iteration, one thread corresponds to a check node. If the expansion factor $Z$ is equal to 100, 1 × 100 threads corresponding to check nodes of a sub-matrix send LLRs to neighboring variable nodes, and also calculate the messages from variable nodes. Next the 1 × 100 reusing threads update LLRs at the second group of check nodes and their neighboring variable nodes. The number of reuse of this group of threads is equal to that of rows of the base matrix. Nonetheless, the layered BP decoder consumes less thread resources, and the number of threads for each sub-matrix is only 1 × 64 × $Z$ (recall that $Z$ is the expansion factor) when decoding 64 codewords simultaneously. The greater the values of $Z$ and the number of codewords are, the higher the utilization rate of the thread is.

The layered BP decoder only involves one file $H_{\text{compact}}$ for indexing. This leads to one GPU kernel implementation of the layered BP decoder for each decoding iteration and each sub-matrix, whose structure is demonstrated in Fig. 3. In the unique kernel, the amount of computation in one thread to calculate the message from a variable node to a check node or from a check node to a variable node, defined by the number of edges on which LLRs are computed, is equal to the degree of the corresponding check node. The LLR $L_{r_{tn}}^{(t,l)}$ is updated through $L_{r_{tn}}^{(t-1,l)}$ and $L_{q_{l}}^{(t,l-1)}$, which represents the message from the $n$-th variable node to the $m$-th check node in the $t$-th iteration and the $l$-th layer $l$. Then each thread calculates the intermediate values $L_{r_{tn}}^{(t,l)}$. In the remaining part of the kernel, each thread computes the message from the $m$-th check node to the $n$-th
The original layered decoder decomposes the $H$ matrix into many sub-matrices on the basis of layers which is equivalent to treating each layer as a sub-code. Each sub-matrix utilizes $1 \times Z$ threads and the serial calculation is conducted among sub-matrices. In order to increase the layered decoder’s thread utilization, we merge the unrelated sub-matrices into a new sub-matrix. For example, a 3-by-3 base matrix shown in Eq. (1) with the expansion factor $Z$ can be divided into three sub-matrices and the degree of any variable node in each sub-matrix is equal to one or zero. Herein, a non-negative integer $a$ in Eq. (1) such as ‘1’, ‘0’, and ‘2’ corresponds to a matrix obtained by cyclically shifting the $Z \times Z$ identity matrix to the right by $a$ bits, and ‘-1’ indicates the all-zero matrix of $Z \times Z$.

$$H = \begin{bmatrix} 1 & 0 & -1 \\ 2 & 1 & 1 \\ 0 & 2 & 0 \end{bmatrix}. \quad (1)$$

If a base matrix is of the form given in Eq. (2), we can combine its first two rows into one layer; that is, the first two rows form a sub-matrix in which the degree of any variable node is equal to one or zero, and the third row separately forms a sub-matrix. Two sub-matrices work in a serial manner by using $2 \times Z$ and $1 \times Z$ threads, respectively.

$$H = \begin{bmatrix} 1 & -1 & -1 \\ -1 & 2 & 1 \\ 2 & 0 & 0 \end{bmatrix}. \quad (2)$$
Figure 3. The GPU implementation of the layered decoder showing one multithreaded computation kernel and data flow from top to bottom for one decoding iteration

Given a base matrix of the form shown in Eq.(3), the first and the third rows of this matrix can be combined into one sub-matrix, and the second row forms a sub-matrix.

$$H = \begin{bmatrix} 1 & -1 & -1 \\ 2 & 0 & 0 \\ -1 & 2 & 1 \end{bmatrix}. \quad (3)$$

If all the sub-matrices consist of $K_1$ layers and the number of codewords that are decoded at the same time is $K_2$, the thread utilization rate is computed by $K_1 \times K_2 \times Z \div 67108864$.

Note that too many calls of external functions in a kernel function spends much time when using CUDA programming. Moreover, the warp divergence increases the waiting time when warp threads encounter control flow statements and enter different branches, which means that the remaining branches except the branch being executed are blocked at this moment. In this work, the kernel function needs to distinguish the sign of the input data, which can be done by calling the application programming interface (API) provided by CUDA, thereby avoiding warp divergence and reducing the calls of external functions. An infinite value or invalid value may appear because of the iterative running of the kernel function. To avoid this, an API function for clipping is needed. Another optimization is to cut down the branches since the branch structure has great drawbacks when different threads utilize different branches with a high probability. For instance, each thread has different calculation amounts and computation time, and thus the finished threads need to wait for other unfinished ones. Towards
this end, we can transform the branch structure to an arithmetic operation when parity checks are used, and hence reduce the decoding time.

The performance of GPU-based layered BP decoders are investigated for QC-MET-LDPC codes with rates 0.1, 0.05 and 0.02 on an NVIDIA TITAN Xp GPU, where the expansion factor is 2500. Fig. 4 demonstrates the error correction speed when different number of codewords are decoded simultaneously. The speed grows steadily from 1 to 128 codewords, and it does not converge even if the number of codewords reaches 128. Due to the shortage of storage space, the decoding speed is not considered when the number of codewords decoded simultaneously exceeds 128. Thus, the proposed layered BP decoder in this paper decodes 128 codewords simultaneously, and its thread utilization rate is \( \frac{1 \times 128}{2500 \times 67108864} = 0.00477 \) where each sub-matrix consists of one layer of the base matrix.

![Figure 4.](image)

Table 1 compares the performance of the layered BP decoder with two types of sub-matrices. The one consists of a single layer and the other consists of multiple layers. When decoding 128 codewords of lengths \( 10^6 \) simultaneously, the layered BP decoder with sub-matrices formed by multiple layers performs better than its counterpart in terms of decoding throughput. The improvement is 3.2Mbits/s, 1.9Mbits/s and 1.6Mbits/s, respectively, when three rates 0.1, 0.05 and 0.02 are considered. The method of combining uncorrelated sub-matrices needs to be further improved, and hence speeds up the decoding and promotes the thread utilization.

| Code rate | 0.1 | 0.1 | 0.05 | 0.05 | 0.02 | 0.02 |
|-----------|-----|-----|------|------|------|------|
| SNR       | 0.161 | 0.161 | 0.076 | 0.076 | 0.03 | 0.03 |
| Number of iterations | 50 | 50 | 75 | 75 | 100 | 100 |
| Form of sub-matrix | single | multiple | single | multiple | single | multiple |
| Latency per iteration(s) | 0.0164 | 0.0156 | 0.0214 | 0.0206 | 0.0263 | 0.0253 |
| Error correction speed(Mbits/s) | 60.91 | 64.11 | 46.72 | 48.65 | 37.96 | 39.51 |

Table 1. Performance comparison of the layered BP decoder when decoding different forms of sub-matrices.

**Discussion**

As described in Ref.8, the early termination scheme can be used as an efficient way to reduce the complexity of LDPC decoder and avoids unnecessary iterations at high SNR. However, this scheme may not be efficient at low SNR since the decoding
| Code rate | 0.1  | 0.05 | 0.02 |
|-----------|------|------|------|
| SNR       | 0.161| 0.076| 0.03 |
| $\beta$   | 92.86%| 94.63%| 93.80%|
| Number of iterations | 50  | 75  | 100  |
| Total number of edges |3767500| 3480000| 3337500|
| FER       | 0.179688 | 0.25 | 0.328125 |
| Number of codewords | 128 | 128 | 128 |
| Latency per iteration(s) | 0.0156 | 0.0206 | 0.0253 |
| Error correction speed (Mbits/s) | 64.11 | 48.65 | 39.51 |

**Table 2.** Performance of the layered BP decoder with GPU implementation.

often fails after multiple iterations in this case. Table 2 illustrates the performance of layered BP decoders without early termination when three rates 0.1, 0.05, and 0.02 are considered, respectively. In the decoding process, the layered BP decoder uses the sub-matrices which consist of unrelated layers of the base matrix. In Table 2, the first row represents code rates, and the second one is SNR under the BIAWGNC. The third row $\beta$ indicates the reconciliation efficiency related to the code rate and the number of discarded parity bits, which has an influence on the reconciliation distance and the secret key rate. The fifth row represents the number of edges of Tanner graph involved in the decoding, and the eighth row displays the decoding time consumption within a iteration. Accordingly, the decoding speed for three tested codes is 64.11Mbits/s, 48.65Mbits/s and 39.51Mbits/s, respectively.

Table 3 demonstrates the performance comparison of the layered BP decoders with or without early termination at different SNRs where the code length and the code rate are $10^6$ and 0.1, respectively. When SNR = 0.161 and 0.171, the layered BP decoder without early termination performs a little faster than that with early termination since less calculations are required to determine whether a valid codeword is obtained in the former. Nevertheless, When SNR = 0.181, the layered BP decoder with early termination is better and the corresponding decoding speed is up to 93.49Mbits/s. This improvement is attributed to the fact that the introduction of the early termination condition reduces the number of iterations significantly at high SNR.

| SNR          | 0.161 | 0.161 | 0.171 | 0.171 | 0.181 | 0.181 |
|--------------|-------|-------|-------|-------|-------|-------|
| Early termination | No    | Yes   | No    | Yes   | No    | Yes   |
| FER          | 0.1797| 0.1797| 0.0273| 0.0273| 0.0273| 0.0273|
| Max iterations | 50  | 50    | 50    | 50    | 50    | 50    |
| Average iterations | 50  | 50    | 50    | 50    | 50    | 30    |
| Latency per iteration(s) | 0.0156 | 0.0162 | 0.0156 | 0.0162 | 0.0156 | 0.0107 |
| Error correction speed(Mbits/s) | 64.11 | 61.74 | 64.11 | 61.89 | 64.11 | 93.49 |

**Table 3.** Performance comparison of the layered BP decoder when decoding 128 codewords with/without early termination.

We also compare the performance of the layered BP decoder with other decoders given in previous works, when the code rate is 0.1 and SNR = 0.161. As can be seen from Table 4, the decoding speed of the decoder given in Ref.7 was

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7.1Mbits/s with MET-LDPC codes. In Ref.\textsuperscript{8}, the decoder achieved 9.17Mbits/s throughput with QC-LDPC codes under the early termination condition, and the speed reduced to 8.21Mbits/s when executing the whole iteration process. In Ref.\textsuperscript{9}, the decoding speed of 30.39Mbits/s was obtained by using MET-LDPC codes and decreasing the computations of variable nodes with degree-1. In contrast, the decoding speed of the proposed layered BP decoder reaches 64.11Mbits/s with no performance degradation by decoding 128 codewords in parallel.

| Refs. | Code type   | Block length | Average number of iterations | FER  | Latency per iteration(s) | Decoding speed (Mbits/s) |
|-------|-------------|--------------|-----------------------------|------|--------------------------|--------------------------|
| [7]   | MET-LDPC    | $2^{20}$     | 100                         | 0.04 | 1.48                     | 7.1                      |
| [8]   | QC-MET-LDPC | $2^{20}$     | 78                          | 0.0243 | 1.47                      | 9.17                     |
| [9]   | MET-LDPC    | $10^6$       | 100                         | 0.1094 | 0.0329                    | 30.39                    |
| This work | QC-MET-LDPC | $10^6$       | 50                          | 0.1797 | 0.0156                    | 64.11                    |

Table 4. Performance comparison with prior works using different types of codes, for rate-0.1 and SNR=0.161 in BIAWGNC.

Despite the high throughput of the GPU-based layered BP decoder, it also has some shortcomings. On one hand, most of threads are not used and thus there exists much space to increase the number of codewords that are decoded simultaneously; but on the other hand, memory shortage limits the number of parallel decoding. Our future work will focus on cutting down on the memory consumption when decoding one codeword and hence increase the thread utilization by decoding more codewords simultaneously.

Methods

In this paper, the layered BP decoding algorithm is employed, which uses less number of decoding iterations to achieve almost the same performance as the flooding BP algorithm. The procedure of the layered BP decoding algorithm is described as follows.

Let $m$ and $n$ denote the $m$-th check node and $n$-th variable node, respectively. Moreover, we denote by $L_{q_{in}}$ the LLR passed from the $n$-th variable node to $m$-th check node, and by $L_{r_{im}}$ the LLR update for the opposite direction. The superscript $(t)$ indicates the current iteration number, and the maximum number of decoding iterations is $T$. Let $l$ indicate the current check node index, which is also the current layer index of $H$. Note that the total number of layers in $H$ is $L$. The layered BP decoding algorithm views each check node as a sub-matrix, while the flooding BP decoding algorithm views all check nodes as a whole matrix.

**step 1:** Initialize the LLR value of the variable nodes by using the received codeword $R$ and channel information where $\sigma^2$ denotes the variance of noise in BIAWGNC. Let $L_{q_{in}}^{(t,0)}$ denote the LLR of the $n$-th variable node at the $t$-th iteration and the $l$-th sub-matrix.

$$L_{q_{in}}^{(0,0)} = \frac{2R_s}{\sigma^2} \quad (4)$$

**step 2:** Update the LLR transmitted from check nodes to variable nodes. Note that $\text{sgn}(x)$ is a sign function and $\Phi(x) = \Phi^{-1}(x) = -\ln(\tanh(x/2))$. Let $N(m)$ represent a set of variable nodes connected to the $m$-th check node and $N(m) \setminus n$ excludes the $n$-th variable node from $N(m)$. Similarly, we use $M(n)$ to denote a set of check nodes connected to the $n$-th variable node and $M(n) \setminus m$ excludes the $m$-th check node from $M(n)$. Next, $s$ represents the syndrome of the received vector where $s_m = 0$ and $s_m = 1$ indicate the syndrome of the $m$-th check node is even and odd parity, respectively.

$$\text{sgn}(L_{r_{lm}}^{(t,1)}) = \prod_{n' \in N(m) \setminus n} \text{sgn}(L_{q_{in'}}^{(t,1),l}) \quad (5)$$

$$|L_{r_{lm}}^{(t,1)}| = \Phi^{-1}\left(\sum_{n' \in N(m) \setminus n} \Phi(|L_{q_{in'}}^{(t,1),l}|)\right) \quad (6)$$

$$L_{r_{lm}}^{(t,1)} = \text{sgn}(L_{r_{lm}}^{(t,1)}) \times |L_{r_{lm}}^{(t,1)}| \quad (7)$$

$$L_{r_{lm}}^{(t,1)} = \begin{cases} L_{r_{lm}}^{(t,1)}, & s_m = 0 \\ -L_{r_{lm}}^{(t,1)}, & s_m = 1 \end{cases} \quad (8)$$
step3: Update the LLR transmitted from variable nodes to check nodes.

\[
L_{q_{(t,j)}}^{(t,l)} = L_{q_{(t,l-1)}}^{(t-1,l)} - L_{r_{(t,l-1)}}^{(t-1,l)}
\]

(9)

\[
L_{d_{(t,l)}} = L_{q_{(t,l)}} + L_{r_{(t,l)}}
\]

(10)

step4: Decide the codeword \( c \) by the LLR value of the variable node.

\[
c_n = \begin{cases} 
0, & L_{q_{(t,l)}}^{(t,l)} \geq 0 \\
1, & \text{otherwise} 
\end{cases}
\]

(11)

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Author contributions statement

Yang Li, Yong Li and B. Xu proposed and guided the work. X. Zhang, L. Ma, J. Yang and W. Huang designed and performed the experiment. All authors analyzed the results and wrote the manuscript.

Additional information

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