An energy-efficient SAR ADC using a single-phase clocked dynamic comparator with energy and speed enhanced technique

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Abstract: This paper presents an energy-efficient 500 kS/s 8-bit SAR ADC with a novel dynamic comparator. The proposed dynamic comparator employs a cross-coupling cascode based preamp and an inverter-based pseudo-latch. This approach achieves a 40% higher speed, a 24% lower power consumption, and a similar input-referred noise level, compared with a conventional double-tail dynamic comparator. Moreover, only one single phase clock is required for the proposed comparator. The prototype ADC was fabricated in a 0.5 \textmu m CMOS process with an active area of 0.18 mm\textsuperscript{2}. Operating under a 1.8 V supply with Nyquist frequency input signal, the ADC consumes 18.2 \textmu W at 500 kS/s and achieves SNDR and SFDR of 47.5 dB and 63.2 dB, respectively. Walden FoM of 188 fJ/conv.-step is achieved.

Keywords: SAR ADCs, asynchronous, dynamic comparator, latch-type comparator, cross coupling, single phase clock

Classification: Integrated circuits

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1 Introduction

A low-power comparator is attractive in energy-efficient successive approximation register (SAR) analog-to-digital converters (ADCs), especially for biomedical applications. Compared with conventional static comparators [1], dynamic comparators [2, 3, 4, 5, 6, 7] are free of static power consumption, which is important to a full dynamic operating SAR ADC. Dynamic comparators also show faster conversion speed than time-domain comparators [8]. However, conventional latch-type sense dynamic comparators [2, 3] confront with voltage headroom issue under a low supply voltage (smaller than two times of threshold voltage). Double-tail latch-type dynamic comparators [4, 5] have less stacking and can therefore operate at lower supply voltages. However, they need two phase triggered clocks, which results in extra power consumption and layout complexity. A single-phase clocked dynamic comparator was presented in [6] to relax clock management. However, the additional loading capacitances at the output of the preamp lead to more power consumption and slower conversion speed.

In this work, we explore a novel single-phase clocked two-stage dynamic comparator with the proposed energy and speed enhanced technique. A cross-
coupling cascode based preamp and an inverter-based pseudo-latch are used in the proposed dynamic comparator to achieve high-speed and low-energy level detection with single phase triggered clock. Furthermore, a split capacitor digital-to-analog converter (CDAC) array with a unit bridge capacitor [9] is adopted for benefits of area and matching. An energy-efficient 500 kS/s 8-bit SAR ADC with the proposed dynamic comparator was fabricated in a 0.5 µm CMOS process, achieving 188 fJ/conv.-step Walden FoM with a 1.8 V power supply.

2 Proposed energy and speed enhanced dynamic comparator

Fig. 1(a) presents a well-known latch-type sense dynamic comparator [2] which is a single-stage implementation, hence, the noise and power consumption are hard to be optimized independently. The latch-type sense dynamic comparator also suffers from strong kick-back noise and stacked transistors issue [2]. A double-tail dynamic comparator [5] which is shown in Fig. 1(b) solves the above drawbacks of the latch-type sense structure. However, the small voltage gain of the first stage and the on-resistances of $M_7$ and $M_8$ decrease the regeneration speed of the latch. Moreover, two phase clocks (CLK and NCLK) are essential, which adds additional power consumption and layout complexity. Fig. 1(c) shows a single-phase clocked double-tail dynamic comparator [6]. Both the small voltage gain and the heavy output loading ($M_9$ to $M_{14}$) of the first stage preamp lead to slower conversion speed and more power consumption.

A novel two-stage dynamic comparator is proposed in Fig. 1(d) to achieve high-speed and low-power level detection. The preamp of the dynamic comparator adopts a cross-coupling cascode structure [7] to increase the voltage gain, which reduces the input-referred noise due to the regeneration latch, thus allowing a
reduction of the latch size to save power. Because of the high voltage gain of the preamp, an inverter-based (M9 to M12) pseudo-latch (M13 and M14) instead of a conventional regeneration latch [5, 6] is used in the second stage for additional power saving purposes. Both the high gain preamp and the inverter-based pseudo-latch speed up the voltage comparison process. Furthermore, only single phase clock (CLK) is required. Fig. 2 shows the transient waveforms of the proposed dynamic comparator with 20 MHz comparison clock (CLK) and 10 µV differential input voltage under 1.8 V power supply.

![Fig. 2. Voltage waveforms of the proposed comparator.](image)

The operation flow of the proposed dynamic comparator in Fig. 1(d) can be divided into four phases. The first phase is the reset phase of the comparator with a low level CLK. The inverter-based pseudo-latch is reset by the output of the preamp, which makes the single clock phase operation possible. In the second phase, CLK becomes high. The differential nodes VXP and VXN discharge in proportion to the input differential voltage through the input pair (M1 and M2). In the third phase, when VXP (or VXN) drops one VTH (M3 and M4) below VN (or VP), the corresponding cascode transistor M3 (or M4) turns on and triggers the pseudo-latch (M3 and M4) action. The latch action makes the voltage difference between the nodes VP and VN eventually reach the threshold voltage of M3 (or M4), which is shown in Fig. 2. In the fourth phase, CLK keeps high. When the output of the preamp VP (or VN) drops below one VTH (M9 and M10), the pre-latch transistor M13 (or M14) pulls VON (or VOP) to the supply voltage and keeps VOP (or VON) at ground voltage through the feedforward connection.

For comparison purposes, the four comparators in Fig. 1 are carefully designed in a 0.5 µm CMOS process with the same dimension transistors and 50 fF load capacitances. The delays of the four comparators are simulated at 20 MHz frequency with VDD = 1.8 V and VCM = 0.9 V. The simulated delays versus the differential input voltage are illustrated in Fig. 3. With the assistance of the
cross-coupling cascode structure and the inverter-based pseudo-latch, the proposed comparator presents the fastest comparison speed. More than 40\% of conversion speed improvement is achieved when compared with the conventional double-tail dynamic comparator [5] with a differential input voltage smaller than 0.1 mV. The delay sensitivity to input voltage (delay/log(ΔV\text{m})), the input-referred noise, the power consumption and the required clock phase of each comparator are compared in Table I with 20 MHz comparison clock, 1.8 V power supply and 0.9 V input common mode voltage. The proposed energy and speed enhanced dynamic comparator achieves the fastest comparison speed and smallest power consumption with the similar input-referred noise and only one single phase clock.

![Fig. 3. Simulated comparison delay versus the differential input voltage.](image)

**Table I.** Simulated performance comparison

|                  | [2] | [5] | [6]  | Proposed |
|------------------|-----|-----|------|----------|
| Delay sensitivity [ns/dec] | 3.22 | 3.87 | 3.23 | 2.30     |
| Input-referred noise [µV]    | 138 | 167 | 218  | 201      |
| Power consumption [fJ/conv.]  | 580 | 657 | 626  | 497      |
| Number of clock phases       | 1   | 2   | 1    | 1        |

### 3 SAR ADC architecture

A 8-bit asynchronous SAR ADC with the proposed energy and speed enhanced dynamic comparator is present in Fig. 4. To save switching energy and area of capacitor array, a 5b+3b split CDAC is adopted. Asynchronous control logic [10] is also used in the SAR ADC to speed up the binary search comparison process. The prototype SAR ADC only needs one 500 kHz sampling clock with 25\% duty cycle, the comparison clock of the comparator (CLKC) is internally generated.
4 Implementation of key building blocks

The fundamental building blocks of the proposed SAR ADC are a CDAC array, a dynamic comparator, and a SAR control logic. The implementation of the novel dynamic comparator has been illuminated in section 2. The following subsections describe the design consideration of the CDAC array and the SAR control logic.

4.1 CDAC array

Split CDAC is one of the solutions to reduce both input capacitance and area of a SAR ADC. However, a fractional value bridge capacitor causes poor matching with the other capacitors. In this work, a unit bridge capacitor [9] is implemented by removing the dummy capacitor of the L-side capacitor array in Fig. 4. Only the H-side capacitors sample the input signal through adding a sample dummy capacitor at the H-side of the CDAC array. A $V_{CM}$-based switching procedure [11] is adopted to achieve half capacitance realization when compared with the conventional switching method [9].

4.2 Asynchronous SAR control logic

To avoid using a high-frequency clock generator, the proposed SAR ADC uses an asynchronous control logic [12]. Fig. 5 shows the schematic and timing diagram of
the SAR control logic. CLKS is the control signal of the sampling switches with 500 kS/s frequency and 75% duty cycle. It turns on the sampling switches at low potential and turns off the switches at high potential. CLKC is the internally generated clock of the proposed dynamic comparator. When the CLKC is low, the outputs of the dynamic comparator are reset to ground. When CLKC goes high, one of the outputs of the dynamic comparator (\(V_{ON}\) or \(V_{OP}\)) goes high, which generates the falling edge of CLKC after a delay of \(T_{d2}\) (the delay of INV and AND gates are ignored). The delay of \(T_{d2}\) relaxes the reconstruction time of the CDAC. Furthermore, the delay cell \(T_{d2}\) comes after the RDY signal, which allows more reconstruction time for the CDAC. \(T_{d1}\) is inserted after the sampling phase to relax the setting time of the reversal phase because of the bottom plate sampling.

5 Measurement results

The prototype 8-bit SAR ADC was fabricated in a 0.5 µm CMOS process. The microphotograph of the chip is shown in Fig. 6. The active area of the SAR ADC is 380 µm x 470 µm. The designed SAR ADC was tested with a 1.8 V supply voltage and a 500 kS/s conversion clock with 25% duty cycle. The input differential signal is rail-to-rail at 3.6 Vp-p.

![Fig. 6. Die microphotograph of the 8-bit SAC ADC.](image)

The static linearity performance of the SAR ADC was tested using the code density method. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC at a full conversion rate of 500 kS/s are shown in Fig. 7. The maximum DNL and INL measured are +0.20/-0.57 LSB and +0.61/-0.35 LSB, respectively.

The ADC’s dynamic performance is measured using single tone testing. Fig. 8 shows the Fast Fourier Transform (FFT) spectra of the ADC output. The ADC achieves 47.5 dB SNDR and 63.2 dB SFDR with a Nyquist frequency input at a conversion rate of 500 kS/s. The ADC has an effective number of bits (ENOB) of 7.6 bit. In Fig. 9, the measured SNDR and SFDR are plotted over a series of input signals with different frequencies, all sampled at 500 kS/s. The ADC has a quite flat SNDR/SFDR response for all the input frequencies.
At a power supply voltage of 1.8 V and a conversion rate of 500 kS/s, the SAR ADC consumes a total power of 18.2 µW. As illustrated in Fig. 10, a detailed breakdown shows that 19% of the total energy is consumed by the split-CDAC, 13% by the CDAC driver, 15% by the proposed dynamic comparator, and 53% by the digital asynchronous SAR logic.

To compare the performance between the proposed ADC and the other works, a commonly cited figure-of-merit (FoM) is used here for comparison:

![DNL and INL errors](image1)

Fig. 7. Measured DNL and INL errors.

![fft spectra](image2)

Fig. 8. Measured 8192-point FFT spectra of ADC output.

![SFDR and SNDR](image3)

Fig. 9. Measured SFDR and SNDR versus input frequency.
The FoM of the proposed SAR ADC is 188 fJ/conversion-step at 500 kS/s and 1.8 V supply with a Nyquist frequency input. Table II summarizes the performance of the proposed ADC, along with state-of-the-art implementations from literature for comparison. Although the proposed ADC was fabricated using an older technology, it still shows competitive FOM with similar conversion rates and resolutions.

### Table II. ADC performance summary and comparisons

|                  | [13] | [14] | [15] | This Work |
|------------------|------|------|------|-----------|
| Technology       | 0.25 µm | 0.18 µm | 0.35 µm | 0.5 µm |
| Active area [mm²] | 0.053 | 0.08 | 0.16 | 0.18 |
| Power supply [V] | 1.4 | 1.0 | 1.4 | 1.8 |
| Sampling rate [S/s] | 100 k | 500 k | 2 k | 500 k |
| ENOB [bits]      | 7.45 | 7.5 | 7.8 | 7.6 |
| Power [µW]       | 4.6 | 7.75 | 0.101 | 18.2 |
| FOM [fJ/conv.step] | 263 | 86 | 227 | 188 |

### 6 Conclusion

This paper presents a single-phase clocked dynamic comparator with energy and speed enhanced technique. The proposed dynamic comparator employs a cross-coupling cascode based preamp and an inverter-based pseudo-latch, achieving high-speed and energy-efficient voltage level decision with only one single phase clock. A 8-bit SAR ADC with split-CDAC employing the proposed dynamic comparator was fabricated in a 0.5 µm CMOS process, achieving 7.6 bit ENOB and 188 fJ/conversion-step FoM with a 500 kS/s conversion rate.