An FPGA Based General Purpose DAQ Module for the KLOE-2 Experiment

A.Aloisio, P. Branchini, A. Budano, A. Balla, M. Beretta, P. Ciambrone, E. De Lucia

1Università di Napoli Federico II.
2INFN Sezione di Roma Tre, Roma Italy.
3INFN Laboratori Nazionali di Frascati, Frascati, Italy.
Paolo.Branchini@roma3.infn.it

Abstract. A general purpose FPGA based DAQ module has been developed based on a Virtex-4 FPGA. It is able to acquire up to 1024 different channels distributed over 10 slave cards. The module has an optical interface a RS-232 a USB and a Gigabit Interface. The KLOE-2 experiment is going to use it to collect data from the Inner tracker and the QCALT. An embedded processor (power pc 604) is present on the FPGA and a telnet server has been developed and installed. A new general purpose data taking system has been based on this module to acquire the Inner Tracker. The system is at the moment working at LNF (Laboratori Nazionali di Frascati).

1. Introduction

This document describes a prototype of Data Acquisition System (DAQ) for the Inner Tracker (IT) [1] of the KLOE-2 experiment.

After the completion of the KLOE data taking [2], a proposal has been presented for a physics program to be carried out with an upgraded KLOE detector, KLOE-2 [3], at an upgraded DAΦNE machine, which has been assumed to deliver an integrated luminosity of about $O(20) \text{ fb}^{-1}$.

The KLOE-2 physics program will be focused on physics coming from the Interaction Point, where the $\Phi$-meson is produced. Its decays into $K^+\pi^-$, $K^-\pi^+$, $\eta$ and $\eta'$ decays as well as $K^+K^-$ interference and search for physics beyond the Standard Model will be studied in this environment.

The improvement in the reconstruction performance for tracks near the interaction region is then of fundamental importance for the accomplishment of this physics program.

The Inner Tracker (IT) will be inserted in the available space inside the Drift Chamber. The proposed solution consists of four independent tracking layers, each providing a 3-D reconstruction of space points along the track with a 2-D readout. The innermost layer is placed at 12.7 cm from the beam line, corresponding to $20\tau_s$ avoiding to spoil the $K_s^0K_L^0$ interference. We have chosen to realize each layer as a cylindrical-GEM detector (CGEM) [4].
A constraint concerns the KLOE DAQ timing: since the Level 1 trigger is delayed of about 200 ns with respect to the Bunch Crossing, the IT discriminated signals must be properly stretched to be acquired. To fulfill the mentioned requirements a novel 64-channels front-end ASIC prototype, named GASTONE (GEM Amplifier Shaper Tracking ON Events) [5], has been developed; this version is a mixed analog-digital circuit, consisting of 64 analog channels followed by a digital section implementing the slow control and readout interface. The amplified and shaped signals are digitized and serially readout using both edges of a 50 MHz clock, achieving a 100 Mb/s transfer rate.

2. The IT DAQ test stand

In this paper we present the first test stand we have realized in order to test the final IT DAQ System. In particular we have used five layers of planar triple-GEMs detectors with 650 μm pitch (more details are in [3] and [4]). The five detectors are equally spaced between each other, with the XV chamber placed at the center (see first left figure in Fig. 1). The entire setup is 1 meter long. The acquisition system is composed essentially by three electronic systems: the front-end boards (GASTONE card), the GIB (Off GASTONE Electronics) board, and the Farm on-line System. The information delivered by the detector is digitized by the GASTONE cards. Each GASTONE Card can process signals coming from 128 channels of the detector and is connected to the GIB, using a 3 meters long twisted pair cable (13 couples).

![Diagram of DAQ System](image)

Fig. 1. The Architecture of the DAQ System: the detector is made by 5 GEM layers. The detector data are collected by the GASTONE which are readout by the boards in the GIB crate. Through the Ethernet connection the data in the GIB Boards are delivered to the Farm on-line system.

The GIB boards have been designed to set up the front-end chip parameters, deliver the power supply and download data from up to eight GASTONE cards (1024 channels) the GIB board performing also a first level event building. The event building process has been implemented in VHDL and it is trigger driven. These are stand alone boards that are based on a Xilinx Virtex 4FX FPGA (Field Programmable Gate Array). An embedded IBM Power PC (PPC405) running at 300 MHz is present on the board. Using an address logic it's possible to set the parameters of GIB board and of the GASTONE chips. All the
peripherals are connected to the processor through the PLB46 (Processor Local Bus) bus running at 100MHz.
The processor is interfaced with the external world through four different peripherals: the 2 Gb/s Optical Port and Gigabit Ethernet to deliver data to the on line farm; full speed USB2 and RS232 are implemented only for debugging and testing purposes.
Moreover, this core performs zero suppression algorithm (if this features is enabled), saves data in a FIFO and delivers them via 2 Gb/s optical link or using 1 Gb/s Ethernet link, as stated before.
Due to the complexity of the operation to be performed, the code dimension of the Power PC acquisition software is greater than the FPGA embedded memory connected to the Power PC (8 Kbyte). To solve this problem we have implemented a system based on a small boot loader that downloads the software from a flash memory and execute it in an external DDR2 memory. This is used even as cache memory for the processor.
The layout of the full system is shown in Fig. 1. The GIB board is in this case connected to the DAQ system by a gigabit Ethernet interface.
A PC based DAQ system equipped with a Gigabit Ethernet interface is used as Farm system and multiple GIB board are also used in the DAQ for testing the even building algorithm.

![Image](image_url)

**Fig. 2.** A snapshot of the Run Control Application. This application is used for managing the full DAQ System and for configuring the parameters of the GASTONE Cards and the GIB Boards.
3. DAQ Processes

In order to acquire data events from a single GIB board in the FPGA chip we have installed a telnet server that listens to the Ethernet port using the TCP/IP protocol (L2GET process). This server allows to manage the board and all GASTONE cards connected to it. In particular it’s possible to set and read all the registers pointing to specific components by sending a specific command to the server. The output of the command returns the value of this register. All the values are in hexadecimal format.

The registers are memory mapped into the PPC405 processor addressing space. This allows us to set the GASTONE chip parameters such as thresholds, mask channels and pulse amplitude, and to read the acquisition parameters such as trigger count.

Moreover the L2GET process acquires data through a TCP socket stream from the Farm system and delivers a command to check the status of data FIFO. The DAQ system we have built has multiple GIB sources. In this case several L2GET processes will be launched by the on-line farm and will write on different shared memory at the farm level their event-fragment. A process named farmbuild had to be written to merge these different event-fragments. This process accesses the data from the shared memory filled by all the L2GETs processes and builds up the event by merging all the fragments delivered by the different sources.

4. Run Control

In order to manage the DAQ system and configure the Front End Electronics (FEE), a simple Graphical User Interface (GUI) was built. This GUI named “Run Control” was written in Java language and allows to program the GIB board and the 16 GASTONE chips hosted in each board. The Application Window is logically divided into three parts: a buttons region which manages the DAQ system process, a second part which checks the DAQ parameters and finally the dialog region, in white, in the lower part of the window. This part allows to read messages coming from the DAQ system. There is also a system to configure the FEE such as GASTONE Cards and some other options on the GIB Board. A snapshot of the windows application is shown in Fig. 2.

A Java class was implemented to start the appropriate DAQ command with ssh remote login. In this way the computer where the control run works can be independent from the DAQ system computers. The application gives the possibility to choose different type of runs: Production run, Pulse run and Calibration run. The Production run allows to set the correct parameters on the Front-end and starts the DAQ process to acquire the physics event. The Pulse run sets the corresponding parameters on the GASTONE cards and on the GIB boards in order to pulse the odd (or even) channels, this features has been used to debug the Front-end electronic. Finally the Calibration run allows to find the thresholds for the single channel in the GASTONE chips. The procedure used sets a specific value for the delivered pulse and by varies the thresholds for the single channels until only half of the events overcome the imposed thresholds.

5. DAQ Performance

The DAQ systems is made of 16 GASTONE Cards and 2 GIB Boards, needed to acquire the full detector. We have measured a value of up to 300 kB/s of data throughput from each GIB board. The throughput is limited because the GIB board can store only one event into the data FIFO. The TCP transfer then takes place for one event at the time a new event cannot be stored into the FIFO memory before the memory is emptied. In order to test the data acquisition and the detector we have collected cosmic ray runs. A trigger has been asserted only when the OR64 signals delivered from the first and last chamber was present within a 100 nsec window. Pulse runs were routinely done to debug the setup before starting long cosmic runs. Finally we have analyzed the data in order to track the trajectory of an event on our detector. In Fig. 3, we show the angular distribution of the tracks.
tracks are built using the second and third layers. The average value of the angle of about 90 degree and its root mean square of about 1.5 degree come from the consideration that the distance between the farthest layers is 50 cm and the single GASTONE channel reads a strip a 4.16 cm wide (each side).

6. Future development

In order to increase DAQ performances we intend to increase the current FIFO memory on the GIB board. The final solution anyhow foresees to use the GIB Optical link already present on the board to transfer data. A new board, named Concentrator Board (CB), is under test. This board has 16 optical ports to acquire 16 GIB boards and a FPGA to perform event building features [8]. The VME interface in the CB can be finally used for managing/acquiring this board.

![Fig. 3. Angular distribution of the track, the track are built using the 2.3 layers.](image)

7. Conclusions

The GASTONE card and GIB Boards have been integrated successfully in a single test stand. The full DAQ System has been running smoothly since then. An offline analysis program has been written to analyze and monitor collected data. Our DAQ system is actually general purpose and can be used to acquire data from other detectors. In KLOE-2 we’ll use it to collect data from the QCAL as well.
References

[1] F. Archilli et al., KLOE-2 Collaboration, “Technical Design Report of the Inner Tracker for the KLOE-2 experiment”, arXiv:1002.2572v1 and LNF-10/3(P) INFN-LNF, Frascati, 2010.

[2] F. Bossi, E. De Lucia, J. Lee-Franzini, S. Miscetti, M. Palutan and KLOE Collaboration, “Precision Kaon and Handron Physics with KLOE”, Rivista Nuovo Cimento, vol. 31, no. 10, 2008.

[3] R. Beck et al. KLOE-2 Collaboration, “Expression of interest for continuation of the KLOE physics program at DAΦNE upgraded in luminosity and in energy”, available at http://www.lnf.infn.it/Infadmin/direzione/roadmap/LoIKLOE.pdf.

[4] A. Balla et al., “Status of the Cylindrical-GEM project for the KLOE-2 Inner Tracker”, arXiv:1003.3770v1, 2010.

[5] A. Balla et al., “GASTONE: A new ASIC for the cylindrical GEM inner tracker of KLOE experiment at DAΦNE”, Nucl. Inst. & Meth. A, vol. 604, no. 23, 2009.

[6] A. Aloisio, F. Cevenini, R. Giordano and V. Izzo, “Characterizing Jitter Performance of Multi Gigabit FPGA-Embedded Serial Transceivers”, IEEE Trans. Nucl. Sci, vol. 57, pp. 451-455, 2010.

[7] A. Aloisio, F. Cevenini, R. Giordano and V. Izzo, “High-Speed, Fixed-Latency Serial Links With FPGAs for Synchronous Transfer”, IEEE Trans. Nucl. Sci, vol. 56 , pp. 2864-2873, 2009.

[8] P. Marciniowski et al., “A Trigger and DAQ System Based on Fast Sampling ADCs”, these proceedings.