A 3.3 Gbps SPAD-Based Quantum Random Number Generator

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Abstract—Quantum random number generators are a burgeoning technology used for a variety of applications, including modern security and encryption systems. Typical methods exploit an entropy source combined with an extraction or bit generation circuit in order to produce a random string. In integrated designs there is often little modelling or analytical description of the entropy source, circuit extraction and post-processing provided. In this work, we first discuss theory on the quantum random flip-flop (QRFF), which elucidates the role of circuit imperfections that manifest themselves in bias and correlation. Then, a Verilog-AMS model is developed in order to validate the analytical model in simulation. A novel transistor implementation of the QRFF circuit is presented, which enables compensation of the degradation in entropy inherent to the finite non-symmetric transitions of the random flip-flop. Finally, a full system containing two independent arrays of the QRFF circuit is manufactured and tested in a 55 nm Bipolar-CMOS-DMOS (BCD) technology node, demonstrating bit generation statistics that are commensurate to the developed model. The full chip is able to generate 3.3 Gbps of data when operated with an external LED, whereas an individual QRFF can generate 25 Mbps each of random data while maintaining a Shannon entropy bound > 0.997, which is one of the highest per pixel bit generation rates to date. NIST STS is used to benchmark the generated bit strings, thereby validating the QRFF circuit as an excellent candidate for fully-integrated QRNGs.

Index Terms—Quantum random number generation (QRNG), Single-photon avalanche diodes (SPADs), Hardware security

I. INTRODUCTION

RANDOM number generators (RNGs) are well-established security primitives used in a variety of schemes ranging from key generation/distribution to, encryption, and privacy activation [1]. With the proliferation of the Internet of Things (IoT) and connected devices, security has become a critical aspect of all system-level design. Consequently, true random number generators (TRNGs) [2], [3], which exploit some classical physical entropy source, are a mature technology available commercially as both discrete silicon devices and IP blocks inside more complex computing circuitry [4] and are able to achieve energy per bit ratios lower than pJ/bit [5]. However, due to the inherent limitations of classical entropy sources in providing sufficient randomness, i.e. limitation of bit bias and correlation, these TRNG ASICs often require complex post-processing in order to establish an acceptable output entropy in the generated bit stream, which in turn significantly reduces the bit rate output [1]. Finally with the emergence of quantum computing, the required security parameter for a generated key increases, doubling the required key length for symmetric encryption algorithms [6], [7].

Quantum random number generators, which exploit inherently random phenomena in nature, are promising technologies which aim to address the challenge/tradeoff between system complexity and randomness performance. QRNG standardisation is underway while debate remains regarding requirements for and specifics of post-processing methods [8], [9], along with the validity of randomness testing [10], [11]. Nevertheless, the exploitation of quantum phenomena provides advantages for the development of future random number generators, particularly for Entropy-as-a-Service (EaaS) and quantum key distribution (QKD) applications, which necessitate very high bit generation rates.

Systems and methods for QRNG designs come in many flavors, including those which exploit photon timing statistics, polarization, quantum tunneling, laser phase noise, to name a few. Furthermore, as an additional measure for combating environmental changes or attacks on the device itself, complex generators that are proven to be device [12] and measurement independent [13] have been demonstrated in literature, although they remain very impractical owing to the very low bit rate (bits-kbps) and bulky setups. A compromise between so-called trusted systems that suggest the quantum nature of the entropy source can create a sufficient generator, and those that contrive more secure bounds, using post-processing or source/device independence, are so-called self-testing quantum random number generators that test for generator defectiveness [14], [15]. This is performed by creating tests tailored specifically to verify the generator output string against its randomness model. Regardless of the generator design, those which provide the most pragmatic solution can be readily modelled, integrated in silicon, and scalable in order to produce designs with high data throughput. For these reasons, single-photon avalanche diode (SPAD) based systems are attractive for QRNG technology development as they are highly scalable (> 1 Mpixel [16], [17]) and reproducible in

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The composition of this paper is as follows. In Section II, we review some previously developed theory on the quantum random flip-flop (QRFF) circuit [18], [19] and thereby introduce the considerations for an integrated circuit that employs this method. From there, a Verilog-AMS model (Section III) is developed in order to thoroughly investigate, in simulation, how circuit imperfections manifest themselves in bias and correlations, thereby validating the analytical model of the bit generation method. In Section VI, a novel full-custom implementation of the QRFF flip-flop is proposed, which uses dynamic logic to overcome effects of finite and non-symmetric transitions present in logic circuits, on the quality of generated bit strings. This QRFF is then implemented in a 55 nm BCD process with measurements comparing the results to the analytical and simulated predictions provided. Finally, we scale the QRFF circuit to a full Gbps QRNG design on chip. Two independent arrays, capable of running concurrently, are implemented with separate readout schemes and achieve a combined 3.3 Gbps output data-rate showing the suitability of the approach in practice. A discussion is provided in Section VII, followed by a conclusion in Section VIII.

II. THE QUANTUM RANDOM FLIP-FLOP

A. Fundamental Operation

The QRFF describes a simple circuit concept that, upon the arrival of a clock strobe, generates a random bit. A symbol representation is shown in Fig. 1a. A specific circuit realization of the QRFF concept is shown in Fig. 1b. Here, an exponentially distributed (in time) discrete event clocks a toggle flip-flop that has its toggle input continuously held to logic 1, thereby realizing the well-known random telegraph signal/process (RTS) with random transitions in time. In principle, as the arrival events occur randomly, the TFF output over a sufficient integration, is uniformly distributed $X \sim U\{0,1\}$. Therefore, once the sampling DFF is clocked by the strobe signal $CLK_{BG}$, a random bit is generated. The architectural simplicity allows for accurate modeling of the bias and autocorrelation of generated bit strings, while the ability to vary internal parameters such as the arrival rate of Poisson events, and external parameters, such as the generation rate, enables flexibility from a system point-of-view, which we will demonstrate in further sections.

B. Model for bias and correlation

Evidently, no imperfectionless source or circuit can exist which then perfectly matches the theory of the Fig. 1a concept. The output of the TFF indeed has finite, and non-symmetric rise/fall times. Furthermore, the sampling threshold of the signal, which distinguishes between low and high has some deviation from center, resulting in a RTS that resembles the waveform depicted in Fig. 1c. The time between transition edges, $\tau_D$, is determined by the detection rate $\lambda_D = 1 / \tau_D$ and splits the signal into two equal half-periods. The rise and fall times are denoted by $t_r$ and $t_f$, respectively, and represent the transition time between the ‘1’ and ‘0’ states until the level of the normalized sampling threshold, $\eta$.

It can be shown that the statistical bias i.e. deviation from $P(X = 1) = 0.5$ for the high state is described by (1) [19].

$$b = \frac{t_f - \eta(t_r + t_f)}{2} \cdot \lambda_D. \quad (1)$$

Some key guidelines for circuit design can be extracted from this model. First, it is clear that the bias should scale linearly in magnitude with increasing detections and that it is desirable to have a fast TFF. Furthermore, it should be possible to essentially eliminate bias resulting from any non-symmetry of the rise/fall times by dynamically adjusting the sampling threshold.

Sources of correlation in any RNG must also be modelled and understood. The autocorrelation function for a binary RTS with normalized amplitudes is defined by (2).

$$R_{XX}(\tau) = e^{-2 \lambda |\tau|}. \quad (2)$$

The time lag interval, $\tau$, for calculation of the autocorrelation coefficient, is controlled by the clock frequency of the sampling DFF in Fig. 1b. Therefore, correlation coefficients, $a_i$, corresponding to specific bit lags, $i$, can be calculated with (3).

$$a_i = e^{-2 \lambda_D / (i \cdot f_{BG})}, \quad (3)$$

The 1-bit lag correlation coefficient, $a_1$, therefore has the highest magnitude, and can be minimized by increasing the ratio $\lambda_D / f_{BG}$. Consequently, there exists an inherent tradeoff between designing for acceptable bias, which increases linearly, and for correlation, which decreases exponentially, with increasing detection rate.
This model is limited by the assumptions that a true Poisson counting process is used as the entropy source. Therefore, care must be taken to ensure that detector imperfections, such as afterpulsing, are negligible or reduced to a minimum, and that the circuit/illumination conditions allow for consistent detection dead times.

C. Benchmarks for Performance

As noted earlier, while the security requirements of any given system and cryptographic scheme can vary, we aim to design a generator which is capable of complying with entropy requirements of the AIS-31 standard, therefore, the Shannon entropy, $H_1(X) = -\sum_{i=1}^{n} p_i \log p_i$, must remain $\geq 0.997$ for a sufficiently long bit string [20]. The corresponding acceptable bias and correlation values must therefore remain below a level of $10^{-3}$. The NIST Statistical Test Suite is used to validate the performance of overall bit strings generated by the final array.

III. VEROILOG-AMS SIMULATION OF QRFF ANALYTICAL MODEL

A. Model details

In order to validate these analytical equations, a simple SPICE-compatible Verilog-AMS model of the QRFF circuit was developed. An exponential source was used by taking advantage of the $\text{Sdist}_{\text{exponential}}$ function provided by the Verilog-AMS language standard. The parameters in Table I were investigated as variables in simulation of bias, $b$, and correlation coefficients, $a_i$.

| Param.  | Description                                              |
|---------|----------------------------------------------------------|
| $\eta$  | DFF sampling threshold normalized to 1 V                 |
| $t_r$   | TFF rise time                                            |
| $t_f$   | TFF fall time                                            |
| $\lambda_D$ | Detection rate from exponential source                  |
| $f_{BG}$ | Sampling frequency of bit gen. clock ($f_{BG}$)         |

TABLE I

VERILOG-A MODEL PARAMETERS OF QRFF

B. Simulation results

Simulation results of bias are displayed in Fig. 2. The generation of bits is a Binomial process with $N$ trials, therefore the variance of bias from simulation can be calculated with $\sigma^2 = 1/(4N)$. In our results, we plot $\pm \sigma$ for reference. Fig. 2a displays the simulated bias compared to the analytical calculation for varying $t_r$, $t_f$, given a fixed detection rate $\lambda_D$ = 80 Mcps and a sampling threshold, $\eta = 0.499$, placed close to the center of the waveform. As the discrepancy between the rise and fall time increases, so does bias, matching very closely to the analytical calculation. In Fig. 2b, a similar analysis was performed but with a varying $\eta$. Here, we can see that a mismatch between $t_r$ and $t_f$ can be compensated for by adjusting the threshold, thereby allowing for the minimization of bias. This is a critical finding from the perspective of integrated circuit implementation, as the foundry process will always create some small, albeit present, variation, across an array regardless of how carefully the circuit is designed. In order to confirm that the bias magnitude scales linearly with increased count rate, at a fixed sampling rate and threshold, a final simulation is performed with the results displayed in Fig. 2c.

Autocorrelation simulations with comparison to the calculation of an RTS, equation (3), are presented in Fig. 3. At a fixed sampling rate, the 1-bit lag correlation coefficient should decrease exponentially, which is indeed observed in the results of Fig. 3a. Conversely, at a fixed detection rate, the correlation should increase exponentially for increased sample...
the above analysis. Given a detection rate of 80 Mcps, which is readily achievable in an integrated SPAD circuit, and a DFF which contains a tunable sampling threshold, a generator which is capable of producing 25 Mbps per pixel is achievable while maintaining a Shannon entropy bound of 0.997. This per pixel generation rate is considerably higher than those demonstrated by other SPAD-based QRNG techniques [21], [21], [22]. Finally, the model could be further improved by formulating the effects of detector imperfections, in particular those containing correlated effects, such as afterpulsing and crosstalk. Clearly, this analysis is only effective for a single QRFF, therefore exploration of system consideration such as PVT of the TFF, count-rate/breakdown non-uniformity, and others, must be performed in order to have a clear view of the scalability of this circuit concept.

IV. DESIGN OF A FULL-CUSTOM CMOS QRFF

A. Technology Consideration

Recently, it has been shown that low afterpulsing detectors (< 1%) are achievable in multiple deep sub-micron processes [23], [24]. Moreover, high-brightness MicroLEDs [25] and SPADs have both been demonstrated in the 55 nm BCD process. These recent advances bring new promise for research into the commercially-viable SPAD-based QRNG sensors, especially for architectures which employ the QRFF method. In this work, we take a step towards that vision by integrating all the detection, bit generation and readout circuitry while leaving the illumination external.

B. Pixel Design

In order to test the model presented, and take advantage of the findings from the simulation analysis, which demonstrates the ability to overcome circuit imperfections, a pixel design containing a full-custom version of the QRFF is proposed and shown in Fig. 4. Although very-high performing SPADs were recently demonstrated in the GF 55 nm BCD process [24], it is not considered a mature CMOS image sensing process, as a standard flow was used for the fabrication of this chip. Therefore, several tunable pixel functions were implemented in order to limit detector variability.

For the TFF, a true-single-phase clock (TSPC) logic-based circuit was implemented for enabling fast transitions, with the output buffer sized appropriately for symmetric rise/fall times. However, as previously stated, process variation will always result in some mismatch across the array. For this reason, a comparator based sampling flip-flop is an evident choice in order to achieve a mean bias centered at zero, overcoming any inevitable non-symmetry. A strongARM comparator-based DFF was designed for fast latching, further enabling high-speed solution which require serialization of many QRFF’s onto a readout bus. The sampling threshold of the DFF is controlled by a global signal $V_T$.

The pixel employs a passive-quench active-recharge (PQAR) circuit in order to limit afterpulsing based off of the design from [26]. The passive-quench transistor, $M_Q$, is designed for a high-impedance, limiting charge flow, which reduces the population of trapped carriers upon an avalanche.
[27], and quickly quenches the SPAD. Reduction of the SPAD bias, $V_{OP}$, also reduces afterpulsing. However, since the variability of breakdown voltages in this process, until this point in time, remained unexplored, it was critical to allow for large range of excess bias values so that all pixels in the array can be utilized. For this reason, a thick-oxide cascode transistor, $M_C$, was chosen so that higher excess bias values can be used without damaging the electronics. A voltage-controlled tunable delay element in the monostable feedback loop was implemented to further investigate the optimal dead-time i.e. a high count rate/afterpulsing tradeoff. The hold and recharge times of the SPAD pulse are determined by the discharging and recharging time of the feedback capacitor, $C_T$, which can be adjusted using the global control pins, $V_H$ and $V_R$. As $V_H$ is increased, the discharging time of $C_T$ decreases, thereby decreasing the length of time until $M_R$ is turned on following an avalanche, consequently decreasing the hold time. Conversely, increasing of $V_R$ adjusts the length of time for which $M_R$ is on, allowing for a controllable recharge time.

This complete pixel, represents a realization of a QRFF, and its general functionality is described by the timing diagram in Fig. 4. Upon an avalanche detection, the SPAD becomes inactive until recharged, which is determined by the external voltage control, and the TFF is consequently toggled. With the arrival of the global bit generation clock signal, $CLK_{BG}$, a random bit is generated at the output, $QRFF_Q$.

V. QRNG ARCHITECTURE AND CHARACTERIZATION SETUP

A sensor with 2800 total QRFF circuits, which was given the moniker FortunaSPAD, was fabricated in the GF 55 nm BCD process with the aim of achieving multi-gigabit operation without the need of post-processing. The block diagram is shown in Fig. 5. FortunaSPAD contains two independent sub-arrays of QRFFs that can be operated simultaneously, along with readout and control circuitry. The chip micrograph and system testing infrastructure is illustrated by Fig. 6. A requirement of the system was to service two different interfaces, which is the reasoning for the two separate arrays.

The first sub-array, denoted as A1, contains 70x32 QRFFs, which are individually read-out through an output multiplexer.
Furthermore, in this sub array each individual pixel is combined with a multiplexer controlled by COUNT (Fig.4), which can bypass the TFF/DFF circuit, allowing for monitoring of the count rate. This enables a comparison between expected results, based on the model, and measurements, along with a more quantitative method for which to decide the illumination intensity.

The second sub-array, A2, contains a more complex readout scheme. An on-chip digital PLL is used to operate a serializer block which serializes 70 SPADs onto a single readout channel. In order to ensure that data transmitting from the chip to the FPGA is valid, the FortunaSPAD contains a control flag that, when enabled, outputs a known pattern to the FPGA. The FPGA is then able to tune the IO delays of each channel appropriately until the known pattern is received.

The two sub-arrays are read out to two separate FPGAs for firmware simplicity, although there is nothing precluding the system from using a single FPGA. A motherboard containing all the required voltage generation and illumination control for the ASIC is designed so that the entire QRNG can be operated using a USB interface. An optical tube houses the LED and a diffuser in order to provide a uniform illumination across the array while also shielding external light. The LED wavelength is 470 nm, which was chosen based on measurements of the photon detection probability (PDP), described in the following section. The FortunaSPAD die area is 1.72 x 2.1 mm with horizontal and vertical pixel pitches of 24 µm and 35 µm, respectively.

VI. Measurement Results

A. SPAD performance characterization

1) Specifications: The design of the SPAD is similar to that published in [24] with the cross-section shown in Fig. 7. The junction is buried deep inside the silicon using a deep p-well, buried n-well (DPW/BNW) implants. The advantage of using a deep junction is that they typically have lower afterpulsing, compared to shallower junctions, as traps from the silicon oxide interface have a greater distance to diffuse in order to enter the multiplication region and cause a spurious avalanche. Furthermore, the PDP is enhanced, enabling a larger spectrum from which to choose the illumination wavelength. The SPAD active radius is 4.4 µm, a virtual guard ring spanning 1 µm on each side and a total radius of 6.5 µm.

![Fig. 7. Cross-section of 55 nm BCD SPAD used in the FortunaSPAD. The junction is formed by the DPW/BNW interface.](image)

2) Afterpulsing: As discussed, perhaps the most critical parameter of the SPAD is afterpulsing, as it induces correlated noise into the random bit generation circuitry. Using the inter-arrival time histogramming technique we estimate the afterpulsing by connecting the test pixel output to a fast 40 GS/s oscilloscope (Teledyne LeCroy WaveMaster 813 Zi-B) with an active probe and bin width of 10 ns. The pixel dead time was tuned to ≈ 8 ns, in order to attain accurate measurements for high-count rate applications. A low-level of light was added to the measurement, in order to attain a count rate ≈ 1 kcps. The results of the experiment are shown in Fig. 8. The extracted afterpulsing is ≈ 0.005 %. From the histogram, it can be seen that the lifetime of traps decays completely after approximately 100 ns. Both the lifetime and afterpulsing percentage are excellent results for a silicon SPAD in a deep sub-micron process.

![Fig. 8. Afterpulsing measurement performed at room temperature using the inter-arrival histogramming method.](image)

3) PDP: The same test pixel was used for measurement of the PDP, with results shown in Fig. 9. The data was taken using the continuous light method at 10 nm intervals up to 3 volts excess bias (V_{EX}) using a setup that has been detailed in [28]. Due to the process, which was not optimized for image sensing, a clear standing wave pattern is seen across the spectrum. An LED (Cree C503B-BAN-CZ0A0452) in the blue spectrum (λ = 470 nm) is selected for the QRNG in order to avoid the efficiency troughs caused by this standing wave pattern, while maintaining a high relative detection efficiency to avoid using higher LED current.

![Fig. 9. PDP measured using integrated PQAR circuit at room temperature across excess bias.](image)

4) DCR: The dark count rate was measured across all pixels in A1, by bypassing the random flip-flop circuitry. The results are shown in Fig. 10. The DCR across all pixels remains relatively low with 95 % of pixels remaining <10 cps/µm² with only three ‘hot’ pixels that are >100 cps/µm².
Therefore, all QRFF’s in A1 should be operable in the desired entropy bounds if circuit and illumination parameters are chosen carefully.

In order to test the limits on performance of the QRFF, the dead-time is reduced to a minimum by adjusting $V_H$ to VDD and keeping the value of $V_R$ to a low value of 0.1 V in order to avoid any effects from pile up. A summary of results for correlation and bias are shown in Table II. The results for both bias and correlation remain above the acceptable entropy bound even until 25 MHz. These results were calculated by generating 327 Mb of data for each sample rate, therefore the calculated $\sigma$ for bias and correlation are $2.76E^{-5}$, and $1.3E^{-5}$, respectively.

C. Array performance characterization

1) SPAD operating voltage: In order to determine proper operation of the chip, the non-uniformity of breakdown voltages across the array must be understood. The $V_{OP}$ should then be set to the minimum value of excess bias where all QRFFs are operating correctly, in order to reduce effects of afterpulsing. A method that can be used to determine this voltage is to observe the per QRFF bit bias at a constant illumination while increasing excess voltages. A visualization of the results from this test is shown in Fig. 13, where a spatial heat map of the per QRFF bias is shown. It can be observed that as the excess voltage is increased, the bit bias reaches a uniform (low) value, at a $V_{OP} =$ 33.3 V, which is the operating value used for all subsequent measurements.

2) Bias and correlation analysis as function of model parameters: The root mean square (RMS) and mean values of per QRFF bias, $b$, and serial correlation, $a_1$, are shown as a function of illumination intensity in Fig. 14 with $f_{BG} =$ 5 MHz. From the perspective of bit bias, the RMS value across the array increases with an increase in LED current, as expected, since the higher count rates scale bias proportionally. Meanwhile, it is observed that the mean bias from 2-3.5 mA remains constant, as a constant sampling threshold ($\eta$) is maintained for all tests. A deviation from this constant magnitude of the mean bias between 1-1.5 mA is observed. This is caused by a low number of pixels, which remain at lower count rates, therefore shifting the mean of the bias slightly.

The sampling threshold is also swept and in doing so, the mean bias of the entire array is very close to 0. The results are shown in Fig. 15. Three points along the curve are also placed in a histogram to visualize the shifting of the entire array in bias, while remaining unchanged for autocorrection. At higher values for the sampling threshold, a small amount of pixels becomes stuck, as their inherent comparator offset prevents the toggling of the output.
**Analytical Model** vs **Measured**

(a) 1, 2, and 3-bit lag correlation coefficients with swept sampling frequency, $f_{BG}$, and $I_{LED} = 5$ mA.

(b) $P = 1$ bias at $f_{BG} = 5$ MHz as a function of normalized sampling threshold and LED current.

Fig. 12. Measured bias and autocorrelation results of a test pixel for comparison to expected results based on derived analytical model. Measurements performed with $V_H = 0.7$ V.

**Spatial bias map across excess bias with constant illumination, $I_{LED} = 2$ mA and a sampling rate $f_{BG} = 5$ MHz.**

Fig. 13. (a) $V_{OP} = 32.8$ V. (b) $V_{OP} = 33.1$ V. (c) $V_{OP} = 33.3$ V.

**Bias and correlation analysis across all QRFFs in A1 ($n = 2240$) as a function of LED current at a $f_{BG} = 5$ MHz.**

Fig. 14. (a) RMS bias. (b) Mean bias. (c) RMS 1-bit lag autocorrelation coefficient. (d) Mean 1-bit lag autocorrelation coefficient.

**D. A2 Performance**

In order to characterize the serialized array, a strobe signal is also implemented inside the FortunaSPAD, which is synchronized to the first QRFF output in the array. This allows for a per pixel spatial analysis in order to make sure there are no malfunctioning circuits/detectors and no particular ‘hot’ spots in the array. The calculated bias and correlation coefficient of all QRFFs in A2 are shown in Fig.16. All QRFF’s in the serialized array achieve a bias and serial correlation coefficient within the required entropy bounds. The max calculated bias and correlation are, $4.09 \times 10^{-4}$ and $4.41 \times 10^{-4}$, respectively, with RMS values across the array of $1.69 \times 10^{-4}$ and $1.32 \times 10^{-4}$, respectively.

Overall for both arrays, under the same operating conditions, only 4 pixels fall slightly outside these benchmarks.
Although the 2796 QRFFs within the entropy bounds are capable of generating 14 Gbps of data, the limitations of the readout circuitry and IOs results in a combined data rate of 3.3 Gbps. In order to ensure that no spatial cross-correlations affect the results of the generated bit strings, a full frame of data is readout in a single CLKBG cycle for statistical testing.

E. NIST-STS

The ability to achieve erroneous results from the NIST Statistical Test Suite when incorrect parameters are chosen is well documented [10], [11]. Therefore, we choose strict parameters for NIST testing with 1 Gb of data split into 1000 bit strings using a significance level ($\alpha$) of 0.001. The results for the NIST test are outlined in Table III with all tests passing.

VII. DISCUSSION AND COMPARISON

A summary of relevant integrated SPAD-based QRNGs, which include the bit generation/extraction method on-chip is shown in Table IV. It can be seen that for an SPAD array-based solution with bit generation on chip, we demonstrate the highest per-pixel generation rate reported. Furthermore, the ability of a single pixel to generate 25 Mbps is the highest reported for an integrated solution. Most prior art either rely on the quantum nature of the entropy source or an arbitrarily chosen post-processing method for justification of the bit generation quality. However, in our work, we systematically model the degradation of entropy and validate it through simulation. As a result, we were able to propose a circuit innovation which was capable of overcoming this, without the expense of a reduced generator speed, an outcome that would inevitably be the case if post-processing was employed.

VIII. CONCLUSION

We have demonstrated a full multi-Gbps integrated SPAD-based QRNG system when using external illumination based on the QRFF method. The QRFF is an architecturally simple but feature-rich, scalable, model-testable bit generation method. By analyzing the degradation of entropy caused by circuit limitations, we were able to propose and validate a simple circuit innovation, namely the addition of a tunable...
sampling threshold, in order to essentially eliminate bias from a single QRFF. This opens the door for more complex QRNG systems based on our circuit technique, that can continually monitor and correct for changes in operation caused by, for example, changes in environmental settings. Furthermore, the ability to precisely control the generator bias and correlation is interesting for certain applications, such as stochastic computing [33].

To the authors’ knowledge, the total throughput of 3.3 Gbps is the highest reported for a single-die SPAD-based system that also integrates its bit generation circuitry. Moreover, the generation capability of a single QRFF of 25 Mbps while maintaining a Shannon entropy > 0.997 is the highest single pixel throughput reported. We have taped-out an improved version of the FortunaSPAD, which contains an improved readout method for higher throughput along with integrated illumination.

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