Dark current analysis of p-i-n NiO/BiTiO3/ZnO thin film heterojunction diode

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Abstract. Dark current analysis of fabricated NiO/BiTiO3/ZnO heterojunction thin film p-i-n diode is demonstrated in this paper. The diodes layers; p-type NiO, i-type BiTiO3 and n-type ZnO were fabricated by using a sol-gel method on glass substrates. This method is the most practical techniques used for manufacturing the nanostructured thin films of metal oxide and perovskite semiconductors. The electrical characteristics of the vertical p-i-n diode were investigated using current-voltage characterization at room ambient condition. The parameters, for example, threshold voltage, rectifying ratio, ideality factor, junction resistance and leakage current, were extracted from the measured data. The turn on voltage, ideality factor, saturation current, junction series resistance, and junction shunt resistance were estimated to be 0.6 V, 6.1, 8 × 10^{-7} A, 40 Ω and 760 Ω, respectively. The effect of post-fabrication heat treatments on electrical properties has been studied. The optimum temperature at 100°C that improves the device performance. The performance enhancement attributed to the interface improvement of the between the aluminum contact and p-i-n thin films. With respect as-deposited p-i-n devices, the heat-treated diodes performance parameters such as threshold voltage, ideality factor and leakage current of devices are found to improve by 5%, 47.3%, and 63.3%, respectively. The rectification performance of the device was 13.6 at 100°C and degrades after the temperature reached 125°C attributed to new material phases appears at interfaces.

1. Introduction

For specific electronics applications, p-i-n diode is an appropriate alternative to other diodes types such as pn, Schottky diode and metal–semiconductor–metal (MSM) diodes [1]. By inserting an intrinsic layer in pn junction between heavy doped p-type and n-type layers p-i-n diode can be achieved. Inserting undoped region make the depletion layer does not change with applied voltages. This can increase the breakdown voltage and improve the optical, radio and microwave frequencies response [2,3]. These features make it appropriate for fast switches, attenuators, modulator, phase shifter, high voltage power electronics and photodetectors [2,3]. However, the drawback of this layer makes the device a poorer rectifier and switching speed [4].

Many researchers have been reported on thin film transition-metal oxide semiconductors based pin diode [5–7]. The transition-metal oxides semiconductors exhibit unique properties. Such as inherently n-type or p-type semiconducting behavior, energy gap can be tailored by doping, high work function, have good transparency, and their ability to produce different size and shape of nanostructures [8,9]. Transition metals oxides can be formed as monoxide (ZnO, NiO), dioxide (RuO2, TiO2), Trioxides (MoO3, WO3), Ternary oxides (LiTiO2, Sr2V2O5), perovskite (BiTiO3, LaNiO3), etc [10]. A novel thin film transition-metal oxide semiconductor pn diodes have been realized by many research groups, ZnO/NiO as an example [11–13]. Fewer works reported on pin structures for thin film transition-metal oxide semiconductors materials [5–7,14].
ZnO is a very attractive wide band transition-metal oxide inherently n-type semiconductor. In terms of electrical and optoelectrical properties, low cost, environmental friend, nanostructure self-assembly higher electron mobility compared to other wide band-gap oxides and chemical stability. However, stable reproducible p-type ZnO is difficult to be achieved [15]. On the other hand NiO is a wide band, intrinsic p-type direct band semiconductor. Due to the compatibility between ZnO and NiO wide band, direct band semiconductor materials, many attempts is reported to propose ZnO/NiO pn junction wide band diode [11–13].

The fixed depletion-layer by the relatively large thickness of intrinsic region in p-i-n reduce the junction capacitance and the internal electric field is established across the total intrinsic layer [13]. As a result, the charge carriers drift transport speeds up by the aid of this internal electric field, make the diode faster and suitable to work at high frequency [16]. We use a perovskite transition-metal oxide semiconductors BiTiO3 thin film as an intrinsic layer. The bandgap of intrinsic BiTiO3 layer is 2.6 eV smaller than both NiO (3.5 eV) and ZnO (3.37 eV) [17][18]. Due to the band alignment, the p-type NiO film can provide holes to diffuse to BiTiO3 film, while the n-type ZnO film offers electrons to diffuse to BiTiO3 film in heterojunction. BiTiO3 is used as an advanced material for solar cell, sensors, capacitors, diodes, and memory devices applications [19].

Here in this paper, vertical p-i-n heterostructure diode from transition-metal oxide thin film is fabricated and characterized in dark condition. All materials can synthesis by low cost sol-gel method. ZnO thin film was used as n-type layer, BiTiO3 film as an intrinsic layer and NiO thin film as p-type layer to form p-i-n. The dark current parameters have been extracted and analyzed.

2. Experiment

The synthesis of undoped transition-metal oxide ZnO, BiTiO3, NiO thin films were prepared by using sol-gel method in ambient conditions. The ITO coated glass (ITO/glass) substrates are used for deposition of thin film layers. Before deposition, the ITO/glass substrates were cleaned by immersed in acetone for 2 min and then quenching in isopropanol for 2 min, then washed with deionized water.

ZnO sol-gel was prepared as reported in our previous work [20]. The achieved sol-gel was subsequently, deployed for coating by spinning the ITO/glass substrate at a speed of 2000 r/min for 40 s, subsequently the coating was preheated on a hotplate at 90°C for 1 min, the deposition and preheating process was repeated for three times.

BiTiO3 solution was performed by mixing 0.174899 g of BiTiO3 powder (99.9%) without any further purification with 20 ml from isopropanol and stirred for one hour at a temperature of 50°C. Then the resultant solution was deposited on ZnO/ITO/glass substrates by spin coater. The substrate spun at 2000 rpm for 40 s, then dried on the hot plate for 1 min, the process was repeated six times to get wanted thickness.

NiO sol-gel was made by 1.7678 g of Nickel acetate (C4H6NiO4·4H2O) in 20 ml of isopropanol and 1 g of DEA. After 1 h of stirring, a green-blue clear solution was obtained. The achieved sol-gel was then used for coating by spin coating technique on the BiTiO3/ZnO/ITO/glass substrates by spin coater substrate for 40 s at a speed of 2000 r/min then the coating is preheated at 90°C for 1 min on a hotplate, this sequence was repeated for four times. The molarity of solutions was kept at 0.5 M.

Next, the heterostucture films NiO/BiTiO3/ZnO/ITO/glass were calcined in the furnace for 1h at 350°C to get the good crystallinity of thin films. Finally, the comb-like Al electrode with a thickness of 200 nm was deposited onto the NiO/BiTiO3/ZnO/ITO/glass layers using a shadow mask through the thermal evaporation technique. The vertical structure of the studied pin diode shown in Figure 1.

The I-V characteristics were carried out using Keithley - Semiconductor Characteristic System (SCS-4200) at room ambient and dark condition for bias voltage between -1.5 V to 1.5 V. The effect of post-fabrication heat treatments on electrical properties has been studied. For each temperature step the values of the turn-on voltage, ideality factor, leakage current, and rectification ratio were estimated from the I-V curve. Curves plotted and analyzed by using Origin software (Origin-06 Professional).
3. Results and discussion

Figure 2 shows the plotted I-V curve of the Al/NiO/BiTiO3/ZnO/ITO heterojunction p-i-n diode measured under the dark condition at room ambient. The post-heat treatment of the studied diode is 100°C. The temperature is selected based on the investigation of effect of the performance of fabricated p-i-n diodes. This investigation presented later in this work.

![Figure 1](image1.png)

Figure 1 The schematic diagram of the vertical structure of p-i-n formed from transition metal oxide thin films.

![Figure 2](image2.png)

Figure 2. I-V characteristics for Al/NiO/BiTiO3/ZnO/ITO diode under dark condition. The inset is semi-log of I-V curve.

From the figure, we can observe that the I-V characteristic demonstrates post-heat treatment a rectification behavior. The threshold voltage is around 0.6 V and the rectification ratio is found to be 13.6 at ± 1.5 V which are comparable with ZnO based diodes those reported by others [20–22]. According to the Shockley equation, the pn junction current-voltage relation is [21][23]:

\[
-J_s = J_0 (e^{\frac{qV}{nkT}} - 1)
\]
\[ I = I_s \exp \left( \frac{eV}{n_0 kT} - 1 \right) \]  \hspace{1cm} (1)

Where \( V \) is the bias voltage, \( I_s \) is the leakage current, \( e \) is the electric charge, \( k \) is Boltzmann constant, \( T \) is the temperature, and \( n \) is the ideality factor. The \( n \) measures the conventionality of the junction to pure thermionic emission, that can be written as \[ 23]\:

\[ n = \frac{e}{kT} \frac{dV}{d(\ln I)} \]  \hspace{1cm} (2)

The leakage current is estimated from the straight-line intercept of log \( I \) at \( V = 0 \), the inset of Figure 2 shows a semilogarithmic graph of forwarding bias I-V characteristics to extract \( I_s \) and \( n \). The ideality factor is extracted from the slope of the linear part of between (0.2 to 0.5 V). The \( n \) for ideal diode should be between 1 > \( n \) > 2 \[ 23]\.

The quality factor of the Al/NiO/BiTiO3/ZnO/ITO heterojunction was estimated to be 6.1 which is in agreement with those reported by \[ 20\][22]. The obtained saturation current was found to be \( 8 \times 10^{-7} \) A, the saturation current found in present work is lower than reported by \[ 20,22\]. The large ideality factor (>2), indicates that the transport of charge carriers cannot be described by thermionic emission theory only. The device shows a non-ideal performance due to the presence of surface states, which is in agreement with the previously reported. Table 1 summarizes the studied device parameters measured under the dark and post-heat treatment at 100°C.

The parasitic resistances affect the current-voltage characteristics of the diode. These parasitic resistances are the series resistance (Rs) and shunt resistance (Rsh). Rs is due to the interfaces between the semiconductors, while the Rsh related to semiconductor interface with metal (electrode) \[ 22\].

Table 1: Device parameters at post heat treatment 100°C and dark condition.

| Parameter               | Value     |
|-------------------------|-----------|
| Turn on voltage         | 0.6       |
| Ideality factor         | 6.1       |
| Saturation current      | \( 8 \times 10^{-7} \) A |
| Rectification ratio     | 13.6      |

The resistance of the junction \( R_j \) is written as \[ 22\]:

\[ R_j = \frac{dV}{dI} \]  \hspace{1cm} (3)
Figure 3. The $R_j$ at (a) Forward bias, (b) Reverse bias.

The $R_s$ and $R_{sh}$ is found from the $I$ versus $V$ curve. $R_s$ can be found from higher forward bias when reach to a constant value. While $R_{sh}$ can be determined from higher reverse voltages [22].
Figure 3 shows the junction resistance $R_J$ versus $V$ have plotted for forward and reverse voltages. Figure 3 (a) illustrates the forward regime to estimate $R_s$. The figure shows four regions in $R_J$. In the first section ($V < 0.2V$) the $R_J$ value increases sharply with voltage, whereas, in the second region ($0.2V < V< 0.5V$), $R_J$ decreases with less slope, then third region ($0.5V < V< 0.7V$) $R_J$ reductions gradually, and in forth region ($V > 1 V$) approaches a saturation that shows that the $Rs$ that equal to 40 Ω, it’s in a good agreement with series resistance reported by others [21,24,25], and the relatively low series resistance cause low turn-on voltage (0.6 V). In the reverse bias regime, the $R_J$ characterizes the $R_{sh}$ of the diode. As shown in Figure 3. (b), the junction resistance reductions with the applied voltage and it saturates to 760 Ω. The $R_{sh}$ initiates from the surface, and grain boundaries carrier recombination.

To investigate the effect of post-fabrication heat treatments on the heterojunction, the electrical properties of the devices have been studied at different temperatures. The heat treatment temperatures, ranging from (25–125°C) in the step of 25°C under dark current. The work was done by using a computer program which applies a voltage sweep up to maximum desired voltage from Keithly (SCS-4200) instruments. For each temperature step the values of the turn-on voltage, ideality factor, leakage current, and rectification ratio were estimated from the I-V curve. The optimum temperature found at 100°C that improve the device performance, the performance enhancement attributed to the interface improvement of the between the aluminum contact and p-i-n thin films.

The ideality factor was plotted versus temperature as shown in Figure 4. The figure demonstrates that the ideality factor was about to be constant around 12 for range 25 to 75°C then decreases to the minimum value at 100°C before rises again at 125°C and become 9. These results demonstrate that the improvement in the device performance because of the deletion of unwanted surface states and the mobility improvement at an optimum post-heating temperature. It is further noticed that the device performance degrades after the heat treatment temperature increase beyond 125°C [20].

Figure 5 shows the saturation current against post-heat treatment temperature. The figure shows that the saturation decreases gradually from $3.26 \times 10^{-6}$ A at 25°C into $3 \times 10^{-6}$ A at 75°C, then reaches it is the minimum value at 100°C which was the optimum $2.26 \times 10^{-6}$ before rises again $3 \times 10^{-5}$at 125 °C. The increases in the saturation current and the degradation in the device performance might be attributed to the new phase of materials performs at interfaces. Figure 6 seen that the rectification ratio was very low for as-deposited device about 1.67, at this stage the device behave as semi-ohmic with leaky I-V characteristics. The rectification ratio gradually increases into 1.73 before rises dramatically into 13.6 at the optimal temperature of 100°C, then degrade again to be 2.8 at 125°C.

This change in the device performance shows that the heat treatment makes changes of interface structure, and the carrier transport mechanism should not be explained by thermionic emission theory only and that other charge transport emission must be incorporate. The degradation in the I-V performance of the device, when the heat treatment reached 125°C also propose that the tunneling charge transport emission cannot be ignored. Also, the rectification ratio reduces, and it found to be 2.8 at 125°C. The degradation in the rectification ratio at higher treatment temperature indicates the increase in carrier concentration that tends the device to perform more like an ohmic contact [20,26].
Figure 4. The ideality factor versus heated treated temperature.

Figure 5. The saturation current versus heated treated temperature.
4. Conclusion
In this paper dark current analysis of fabricated NiO/BiTiO3/ZnO heterojunction thin film p-i-n diode is demonstrated. Effect of post-fabrication heat treatments on the device performance have been studied at the range of 25‒125°C under dark current. The optimum temperature post-heat treatments have found at 100°C. The dark current device performance improvement of the parameters; turn-on voltage, ideality factor, leakage current and rectification ratio are found to be 5%, 47.3% and 63.3%, 714.4%, respectively with respect as-deposited p-i-n devices. The turn-on voltage, ideality factor, saturation current, and rectification ratio at 100°C were estimated to be 0.6 V, 6.1, $8 \times 10^{-7}$ A, 13.6, respectively. The performance enhancement attributed to the improvement of the interface between the layers of p-i-n devices. The device performance degrades quickly after the temperature reached 125°C attributed to new material phases appears at interfaces.

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