Multiple-Symbol Interleaved RS Codes and Two-Pass Decoding Algorithm

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Abstract: For communication systems with heavy burst noise, an optimal Forward Error Correction (FEC) scheme is expected to have a large burst error correction capability while simultaneously owning moderate random error correction capability. This letter presents a new FEC scheme based on multiple-symbol interleaved Reed-Solomon codes and an associated two-pass decoding algorithm. It is shown that the proposed multi-symbol interleaved Reed-Solomon scheme can achieve nearly twice as much as the burst error correction capability of conventional single-symbol interleaved Reed-Solomon codes with the same code length and code rate.

Keywords: burst error; erasure decoding; FEC; interleaved Reed-Solomon codes

I. INTRODUCTION

TWO important error types present in most digital communication systems are random and burst errors. Random errors are typically the result of independent error events and are scattered. Burst errors are the result of correlated noise events and appear in clusters. In some applications, such as automotive networks with high level interference from adjacent systems, burst noise is much more prominent than random noise. In such situations, an optimal FEC scheme is expected to have a large Burst Error Correction Capability (BECC) while owning moderate Random Error Correction Capability (RECC) at the same time. Most of the existing FEC schemes are designed for random errors that are inefficient in dealing with burst errors [1], [2]. For example, Low-Density Parity Check (LDPC) code is vulnerable to burst errors due to its soft-decision probability-based decoding [3]. Interleaved Reed-Solomon (IRS) codes were proposed when both large RECC and BECC are emphasized [4], [5]. The IRS codes integrate a high RECC of RS codes with interleaving techniques to improve BECC. An IRS code usually consists of several independent RS codes with the same code length and code rate. Depending on the codeword dimension, homogeneous and heterogeneous IRS codes were developed with their associated decoding algorithms, such as shift-register synthesis-based joint decoding method [6] and interpolation-based probabilistic decoding algorithm [7].

Existing IRS schemes interleave the independent RS codes at single-symbol level and adopt a single-pass decoding method. In this letter, we present a novel IRS code that interleaves codewords at multiple-symbol level. We call it Multiple Symbol IRS (MS-IRS) scheme (or burst-interleaved RS coding). A two-pass decoding algorithm is presented to increase the BECC of MS-IRS schemes. Specifically, in the first pass, as long as there exists one RS code that is decodable, the burst
This letter is organized as follows. Section II introduces the MS-IRS encoding scheme. Section III presents the proposed two-pass decoding algorithm. Theoretical BECC and decoding latency are studied as well. Monte-Carlo simulations on an example channel are presented in Section IV.

II. MS-IRS Codes

Assume the considered IRS codes have an interleaving depth equal to $L$. Each independent RS code is denoted by $RS(N, K, m)$, where $N$ is the number of symbols in a codeword, $K$ is the number of information symbols in a codeword, and $m$ is the number of bits in each symbol. The burst-length (denoted as $BL$) refers to the number of symbols in each dispatch of data to one component code.

Fig.1 (a) shows an example of a conventional SS-IRS code with three independent RS component codes. The interleaving depth is $L=3$. In this case, the information symbols are dispatched to different RS codes symbol by symbol. After RS encoding, the coded symbols from all component codes are multiplexed together in the same way.

Fig.1 (b) shows an example of an MS-IRS code also with interleaving depth $L=3$ and the length of burst interleaving is 3 RS symbols (i.e., $BL=3$). In this case, the information symbols are dispatched to each component code at 3 symbols per time. The encoded symbols from all component codes are multiplexed together in the same way.

III. Two-Pass Decoding Algorithm

In this section, we present a two-pass decoding algorithm to enable the increased BECC for MS-IRS codes. Fig. 2 illustrates the flow diagram of the two-pass decoding algorithm. In the first pass, the algorithm checks if any code can be decoded. With multiple-symbol interleaving, we can predict the erasure starting segment when at least one RS code is decodable. In this case, an erasure decoding (or combined error and erasure decoding [8] error locations can be deduced from locations of those corrected errors. Then in the second pass of decoding, a combined error and erasure coding [8] is performed to improve the BECC. Without knowing burst error locations, the proposed MS-IRS scheme can achieve nearly twice as much the BECC as conventional Single Symbol IRS (SS-IRS) codes with the same code length and code rate. Also, the BECC and processing latency of the proposed MS-IRS codes can be optimized by adjusting the length of each independent RS codes.

![Flow chart of the two-pass decoding algorithm for MS-IRS codes](image-url)
when burst length $BL$ is smaller than the error correction length $t$) will be performed in the second pass of error decoding.

In the following discussion, we assume two or more (moderately long) bursts of errors will not appear in one FEC block. This is very reasonable since the probability of having two or more (moderately long) bursts of errors in a FEC block is much lower than that having a long burst of errors for a communication system receiver with error propagation (e.g., when using decision feedback equalizer). From coding theory [1], we know a RS code with designed error correction capability $t$, can correct $2t$ erasure errors, or $u$ random errors plus $2v$ erasure errors when $u + 2v < 2t$, $u > 0$, $v > 0$. For example, assume each RS code in Fig. 1 (a) has an error correction capability of four symbols, i.e., $t = 4$. In addition, assume there is one random error that is outside of the burst noise for at least one component code. Now, we investigate the maximum length of the burst errors that can be corrected without knowledge of the burst error locations. Fig. 1 (a) shows an example of the maximum burst error length in the best and the worst cases, respectively, when all RS codes can be decoded correctly. For example, the burst noise in the best case can start from the first bit of the first code-1 symbol and end at the last bit of the third code-3 symbol. The burst noise in the worst case can start from the last bit of the first code-1 symbol and end at the last bit of the third code-3 symbol. Hence, the maximum length of burst noise can be corrected in the best case is $3\times 3 = 9$ RS symbols.

Similarly, the maximum lengths of burst noise that can be corrected by the MS-IRS codes in the best and the worst cases are both shown in Fig. 1 (b), wherein one random symbol error outside of the burst noise was assumed for some of the component codes. In either case (best case or worst case), code-3 is decodable since the burst noise only corrupts 3 symbol for this $t=4$ component code. Based on detected consecutive error locations from decoding, it is proper to assume the burst noise starts at the first symbol of code-1 shown in Fig. 1 (b). We can employ a decoding of combined 1 random error with 6 erasure errors (note: $1\times 2 + 6 = 2\times 4$) for both code-1 and code-2. Therefore, we can correct a long burst of $3\times 5 = 15$ symbol errors in the best case, comparing to 9-symbol errors in the SS-IRS case with the same code length and code rate.

In general, assume each RS component code has an error correction capability of $t$ symbols over GF$(2^m)$. Without knowing the burst noise locations, the SS-IRS and MS-IRS codes have a BECC of $L^*t^*m$ bits and $(2^*L–1)^*t^*m$ bits in the best case, respectively. It means that MS-IRS codes can achieve nearly twice the BECC as conventional SS-IRS codes when $L$ is moderately large. In fact, when the burst noise is no longer than $L^*t^*+(L–1)^*t$ symbols, at least one component RS code is decodable in the above defined best case. Thus erasure information (i.e., error locations) can be obtained and erasure decoding can correct all errors caused by the burst noise.

For MS-IRS codes, the above BECC equation assumes the number of symbols in each colored segment is equal to $t$, i.e., $BL = t$. If the number of symbols in each colored segment is less than $t$, a combination of random and burst errors can be corrected. Then, the BECC is equal to $(2^*L–1)^*BL^*m$ bits in the best case. In general, we only reserve a small portion of $t$ for correcting random errors outside of the long burst. This reservation depends on how low the Gaussian noise level is in the considered application.

We next calculate the encoding and decoding latencies of the MS-IRS codes. At the transmitter, a data buffer is needed to accommodate for increased data rate after FEC encoding. The buffering latency is calculated based on the total FEC block size and the parity data size. At the receiver, latency includes receiving time for the interleaved component codes and the decoding latency. For example, given a RS code (144, 129, $t=7$) over GF$(2^9)$ and 3-way interleaving with $BL = t–1 = 6$, and
assuming 1Gbps of information rate, the buffering latency is \(3(N-K)9/(N/K*1.0\text{Gbps})=3\times(144-129)/9/(144/129)\times1.0\text{ns}=363\text{ns}\). The receiving latency is \(3\times129\times9\times1.0\text{ns}=3483\text{ns}\). Decoding can be easily completed within 120ns [8]. Therefore, the total latency associated with FEC process is no more than \(3483+363+120=3968\text{ns}\), which is less than \(4\mu\text{s}\).

IV. SIMULATIONS

In this section, the advantage of the proposed MS-IRS code is verified by simulating an example communication system with PAM3 modulation scheme. This system is quite similar to an automotive networking system being standardized. The block diagram of the system model is shown in Fig. 3. The short RS code blocks are burst interleaved in the interleaver block, whereas for the long RS code, the interleaver is not applied. The output of the RS encoder and the interleaver is applied to a mapper that maps the symbols (3 bits each) to physical layer values \{-1, 0, +1\}. The method of mapping is given in Table I. The physical layer symbols \{-1, 0, +1\} are then transmitted. The channel is assumed to be real valued and the imaginary and the real parts of symbols at the mapper output are transmitted as the even and odd samples. The channel response is depicted in Fig. 4. It is seen that the channel is dispersed over several physical layer symbols, which results in severe Inter Symbol Interference (ISI). To remove the ISI, a Decision Feedback Equalizer (DFE) is used at the receiver. The block diagram of the channel, noises, and the DFE are shown in Fig. 5. Note that it is assumed that the channel response is known to the receiver. The slicing is performed in one dimensional form as soon as one symbol is received; it is compared against a threshold (±0.5) and accordingly is selected from the set \{-1, 0, +1\}. Once a pair of even and odd are collected, the symbol bits are obtained by demapper (see Table I).

Normally the RS decoder is able to correct the errors during the burst duration. In practice, however, the number of errors can be more than the number of symbols corrupted by the burst noise. This is due to the error propagation problem associated with the DFE when the slicer makes a few decisions, the errors propagate through the feedback filter and arrive at the slicer input causing more errors to occur. These errors are bursty in nature and could easily extend to a number beyond the error correction capability of RS codes. In the following simulation cases, it will be shown that short RS codes, when followed by a multi-symbol interleaver, significantly improve the performance when compared with long RS codes.

| Symbol Bits | 000 | 001 | 010 | 011 |
|-------------|-----|-----|-----|-----|
| Mapper Output (even, odd) | {-1,-1} | {-1,0} | {-1,+1} | {0,-1} |
| Symbol Bits | 100 | 101 | 110 | 111 |
| Mapper Output (even, odd) | {0,+1} | {+1,-1} | {+1,0} | {+1,+1} |

**Table I** Mapping table

**Fig.3** Simulation model block diagram

**Fig.4** Channel response
4.1 Case 1

In this case, we compare a long code RS\((N=432, K=387, t=22, m=9)\) \(L=1\), with three short codes RS\((N=144, K=129, t=7, m=9)\) that has been multi-symbol interleaved with parameters \(L=3\) and \(BL=6\). The channel noise includes AWGN with Signal-to-Noise Ratio (SNR) of 30dB and burst noise. The burst duration and period are set equal to 38 symbols and 5400 symbols, respectively. The rate of symbol transmission is 750MHz in the recent automotive standard (1000Base-T1). 38 symbols burst is around 50ns in time. The Bit Error Rate (BER) and Block Error Rate vs. the Signal to Burst Noise Ratio (SBNR) are shown in Fig. 6 and Fig. 7, respectively. It is seen that the short RS code with multi-symbol interleaver with single pass exhibits a very similar performance to the long RS code. But, it is clear that RS\((144,129)\) with a multi-symbol interleaver \((L=3, BL=6)\) performs significantly better than RS\((432,387)\) when combined with a two-pass decoder. Moreover, the MS-IRS scheme has much lower computation complexity than the long RS code due to significantly reduced \(t\) of each component code, which generally leads to lower decoding latency and lower power consumption. On the other hand, the second pass of decoding requires extra hardware and computation time compared to conventional single-pass decoding of SS-IRS codes. Due to the limited space, the details will not be provided in this letter.

4.2 Case 2

In this case, RS\((N=147, K=132, t=7, m=9)\), \(L=3, BL=7\), is compared against RS\((N=144, K=129, t=7, m=9)\), \(L=3, BL=6\), under the same channel conditions as given in Case 1, except that the burst duration is increased to 114 symbols. The BER and Block Error Rate vs. the SBNR are shown in Fig. 8 and Fig. 9, respectively. It is seen that RS\((147,132)\) \(L=3, BL=7\) performs better than RS\((144,129)\) \(L=3, BL=6\). In other words, depending on the burst noise duration and severity, the \(BL\) value can be select-
with a two-pass decoding algorithm. The analyses were provided and the detailed simulation results have been presented to verify the benefits of the proposed coding and decoding methods. It is worth mentioning that the component codes to be interleaved can also be selected as BCH, LDPC, or other FEC codes.

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Biographies

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