A 2.5 V, 2.56 ppm/°C Curvature-Compensated Bandgap Reference for High-Precision Monitoring Applications

Guangqian Zhu, Zhaoshu Fu, Tingting Liu, Qidong Zhang * and Yintang Yang

School of Microelectronics, Xidian University, Xi’an 710071, China; zhugq@stu.xidian.edu.cn (G.Z.); combfu@163.com (Z.F.); ttingtingliu1997@163.com (T.L.); yyang@xidian.edu.cn (Y.Y.)
* Correspondence: qdzhang@xidian.edu.cn; Tel.: +86-153-1993-8896

Abstract: This work presents a high-precision high-order curvature-compensated bandgap voltage reference (BGR) for battery monitoring applications. The collector currents of bipolar junction transistor (BJT) pairs with different ratios and temperature characteristics can cause greater nonlinearities in ∆V_{EB}. The proposed circuit additionally introduces high-order curvature compensation in the generation of ∆V_{EB}, such that it presents high-order temperature effects complementary to V_{EB}. Fabricated using a 0.18 µm BCD process, the proposed BGR generates a 2.5 V reference voltage with a minimum temperature coefficient of 2.65 ppm/°C in the range of −40 to 125 °C. The minimum line sensitivity is 0.023%/V when supply voltage varies from 4.5 to 5.5 V. The BGR circuit area is 382 × 270 µm², and the BMIC area is 2.8 × 2.8 mm².

Keywords: bandgap reference; curvature compensation; low temperature coefficient; BCD process; battery monitoring

1. Introduction

The battery management system (BMS) guarantee the working performance and service life of the battery, and provides new energy management for various applications such as electric vehicles (EVs), energy storage system, and aerospace satellites. Battery monitoring (including voltage, current, temperature, State of Charge (SOC), State of Health (SOH)) is the most basic and core application of the BMS. In typical BMS, it is necessary to constantly evaluate various parameters pertaining to Li-ion battery packs. Monitoring precision is the fundamental guarantee for the reliability and performance of EVs. Figure 1 presents the structure of the proposed BMS.

“One master, many slaves” architecture is used for our BMS. The master unit (MU) mainly measures the total voltage, total current, pressure and collision information of the battery pack, calculates the SOC and SOH values, and controls multiple slave units (SUs). The SUs mainly sense the voltage of each battery cell and the temperature of several points in the BMS box. Communication between MU and SUs is through a controller area

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network (CAN) interface. The battery monitoring integrated circuit (BMIC) is the most significant device used in the BMS slave unit. It connects directly to the battery pack and is designed to monitor multiple cell voltages and temperatures [1, 2]. Figure 2 presents the structure of the proposed BMIC.

![Figure 2. The structure of the proposed BMIC.](image)

In order to achieve a high-integration and low-power BMS design as much as possible, a multiplexer structure is used in the BMIC to expand the number of measurable battery cells, and then a high-precision reference circuit and ADC are used to ensure the measurement accuracy. In this structure, the monitoring error mainly comes from the error on the multi-channel sensing channel, the ADC error and the reference error. The accuracy of the voltage reference is the most important criterion that determines the precision of battery monitoring, and it is also an indispensable part in other precision sensors or applications [3–5].

Bandgap voltage reference (BGR) is the mainstream temperature- and voltage-insensitive reference used in the field. In high-precision BGR applications, the use of only first-order linear compensation [6–12] is insufficient for achieving the required temperature coefficient (TC). Effective and simple high-order temperature compensation methods have thus become the norm for optimized circuit design. The curvature-compensation methods reported in the literature [13–22] further offset the temperature nonlinearity of the emitter-base voltage ($V_{EB}$). The topologies in [13] combine opposing curvature characteristics produced by the two BGR cores to achieve the reference voltage. However, even with high-order temperature compensation, the output voltage inevitably drifts owing to factors such as process spread, device aging, and stress. Therefore, the on-chip calibration or trimming structure after production is important to ensure accuracy. The BGR circuits in [14, 16] were designed specifically for battery management applications; specifically, the switched-capacitor bandgap reference in [14] and its high-order compensation are achieved by replacing the analog circuitry with a more sophisticated digital correction algorithm [15]. The internal temperature sensor and a lookup table will incur additional cost. The topologies in [16] have piecewise exponential curvature compensation such that good temperature characteristics can be obtained over a wide temperature range, however, the compensation structure is slightly complicated. A zero TC biased MOSFET compensation method is used in [17], but the untrimmed reference voltage is greatly affected by process spread. The circuit in [18] is an ultra-low-power BGR structure, but the TC of the reference voltage is extremely large.
This paper presents a $V_{EB}$-based high-order curvature-compensated BGR with a low TC over a temperature range of $-40$ to $125 \, ^\circ\text{C}$. The designs in [19] exploit different collector currents to enable logarithmic curvature compensation of $\Delta V_{EB}$. Based on the idea, a new $\Delta V_{EB}$ generation structure is also proposed. The remainder of this paper is organized as follows. Section 2 illustrates the principle of the proposed BGR, and Section 3 presents the experimental results; the conclusions are presented in Section 4.

2. Principles of the Proposed BGR

2.1. Basic BGR Topologies

The $V_{EB}$ of a bipolar junction transistor (BJTs) (or $V_{BE}$ for an NPN transistor) is a complementary-to-absolute-temperature (CTAT) parameter with a TC of about $-1.6 \, \text{mV/}^\circ\text{C}$, and the temperature dependence of $V_{EB}$ [23] can be expressed as

$$V_{EB}(T) = V_{G0}(T_r) - \frac{[V_{G0}(T_r) - V_{EB0}(T_r)]T/T_r - V_T(\eta - \theta) \ln(T/T_r)}{\text{linear}} - \frac{V_T(\eta - \theta) \ln(T/T_r)}{\text{nonlinear}},$$

where $V_{G0}(T_r)$ is the extrapolated bandgap voltage at a reference temperature $T_r$, $\eta$ is a temperature-insensitive parameter [24], and $\theta$ is the temperature dependence order of the collector current. Figure 3 shows two widely used BGR structures based on the first-order temperature compensation.

Figure 3. Schematic of the widely used BGR structures: (a) voltage-mode; (b) current-mode.

The bandgap voltage $V_{bgr}$ of the voltage-mode BGR [6] in Figure 3a is given by

$$V_{bgr} = V_{EB} + \frac{R_2}{R_1} \Delta V_{EB} = V_{EB} + \frac{R_2}{R_1} \cdot \frac{kT}{q} \ln(N),$$

and the $V_{bgr}$ of the current-mode BGR [7] in Figure 3b is given as

$$V_{bgr} = R_3 \left( \frac{V_{EB}}{R_2} + \frac{\Delta V_{EB}}{R_1} \right) = R_3 \frac{V_{EB}}{R_2} + R_3 \frac{kT}{q} \ln(N),$$

where $V_T = kT/q$ is the thermal voltage with a TC of about $85 \, \mu\text{V/}^\circ\text{C}$, $k$ is the Boltzmann constant, $q$ is the electron charge, and $N$ is the emitter-area ratio of $Q_2$ to $Q_1$.

First-order compensation can only decrease the TC of $V_{ref}$ to about $13 \, \text{ppm/}^\circ\text{C}$ in the presence of nonlinearity [6–12]. In high-precision battery monitoring, it is necessary to detect voltage changes below 3 mV, and the TC of the reference voltage must be less than or equal to $6 \, \text{ppm/}^\circ\text{C}$ [16]. Therefore, further reduction of the TC requires compensation of the higher-order terms related to $T\ln(T)$ in $V_{EB}$.
2.2. Insertion of Nonlinear Compensation in $\Delta V_{EB}$

The current-mode or voltage-mode BGRs primarily use the proportional-to-absolute-temperature (PTAT) characteristic of $\Delta V_{EB}$, where $\Delta V_{EB}$ is expressed as

$$\Delta V_{EB} = V_{EB1} - V_{EB2} = \frac{kT}{q} \ln \left( \frac{I_{c1}}{I_{c2}} \right). \quad (4)$$

If the collector currents $I_{c1}$ and $I_{c2}$ of the PNP BJT pair (Q1 and Q2) have the same temperature characteristics, and $\Delta V_{EB}$ is a more easily controllable linear compensation term. However, if the TC of collector currents are different, then a nonlinear term is introduced into $\Delta V_{EB}$ through the logarithm function.

Therefore, based on the conventional BGR structures in Figure 3, the principle of the curvature-compensated BGR in this work is shown in Figure 4. Based on the original bias current $I_x$ of Q1 and Q2, the current $I_y$ is introduced and drawn to form the difference in the collector currents of the BJT pair. $I_x$ and $I_y$ have different temperature characteristics, which lead to an increase in the nonlinearity of $\Delta V_{EB}$. Hence, $\Delta V_{EB}$ is rewritten as

$$\Delta V_{EB} = V_T \cdot \ln(N) + V_T \cdot \ln \left( \frac{1 + I_y/I_x}{1 - I_y/I_x} \right). \quad (5)$$

Assuming that $I_y/I_x$ is a temperature-dependent function, i.e., $x(T) = I_y/I_x$. The natural logarithm has the Maclaurin series

$$\ln(1 + x) = (-1)^{n+1} \sum_{n=1}^{\infty} \frac{x^n}{n} = x - \frac{x^2}{2} + \frac{x^3}{3} \cdots + (-1)^{n+1} \cdot \frac{x^n}{n}, \quad (6)$$

which converges for $|x| < 1$. The logarithmic term in $\Delta V_{EB}$ can thus be calculated as

$$\ln \left( \frac{1 + x}{1 - x} \right) = 2 \left( x + \frac{x^3}{3} + \frac{x^5}{5} + \frac{x^7}{7} + \cdots + \frac{x^{2n-1}}{2n-1} \right). \quad (7)$$

From the Taylor expansion results, it is evident that the logarithmic function can compensate for the third-order term at least. It is worth noting that $|x| < 1$ is a necessary condition, so it must be guaranteed during circuit design. To simulate the compensation ef-
effects of (7) on the nonlinear term $T\ln(T)$ in $V_{EB}$, construct the temperature-related functions $F_1(T)$ and $F_2(T)$ for the ideal calculations. $F_1(T)$ and $F_2(T)$ are expressed as

\[
\begin{align*}
F_1(T) &= -r_0 \cdot T \cdot \ln\left(\frac{T}{T_0}\right), \\
F_2(T) &= r_0 \cdot T \cdot \ln\left(\frac{1+h T}{1-h T}\right),
\end{align*}
\]

where $r_0$ is a constant, and $h$ is a coefficient that ensures $hT < 1$. $F_1(T)$ and $F_2(T)$ were combined in different proportions to obtain the predicted compensation results shown in Figure 5.

**Figure 5.** Ideal results calculated for the proposed curvature compensation.

It is observed that the deviation between the maximum and minimum values of $F_1(T)$ after compensating for $F_2(T)$ is only 4% of that before compensation, which better suppresses the nonlinear term in $V_{EB}$ and realizes curvature compensation.

In Figure 4, after obtaining the $\Delta V_{EB}$ with high-order compensation effect, the $\Delta V_{EB}$ with the coefficient $R_2/R_1$ is obtained through $R_1$, $R_2$, $M_1$ and $M_3$, and it is added to the $V_{EB}$ of $Q_3$ to obtain the compensated bandgap voltage $V_{bgr}$. In order to further obtain the required reference voltage, the final reference voltage $V_{ref}$ is obtained through the negative feedback structure composed of $R_3$, $R_4$, $R_{t1}$ and the amplifier. $V_{ref}$ can be expressed as

\[
V_{ref} = \frac{R_3}{R_3 + R_4 + R_{t1}} \cdot V_{bgr} = \frac{R_3}{R_3 + R_4 + R_{t1}} \cdot \left(V_{EB} + a \cdot \frac{R_2}{R_1} \Delta V_{EB}\right),
\]

where the parameters $a$ is the size ratio of $M_1$ and $M_3$.

### 2.3. Implementation of the Proposed Circuit

According to the ideal results obtained above, the main design goal is to introduce a nonlinear $\Delta V_{EB}$ in the BGR core circuit. Figure 6 presents the implementation of the proposed circuit, including a start-up circuit, a nonlinear $\Delta V_{EB}$-based curvature-compensated BGR core circuit, a temperature-independent current generating structure, and a final reference voltage output.
Figure 6. Schematic of the proposed curvature-compensated BGR circuit.

The $R_3$ and NMOS $M_{12}$, $M_{13}$, $M_{14}$ constitute a start-up circuit to drive the reference circuit out of the degenerate bias point when the supply voltage $V_{DD}$ is turned on. When $V_{DD}$ rises, $M_{12}$ and $M_{13}$ are turned on, and the gate voltage of the PMOS current mirrors is pulled down. After the whole circuit is started, $M_{14}$ is turned on, and $M_{12}$ and $M_{13}$ are turned off.

The traditional scheme of $\Delta V_{EB}$ generation uses currents with the same temperature characteristics to drive a pair of BJTs. The main difference in the proposed nonlinear $\Delta V_{EB}$ generation unit is that two sets of currents with different temperature characteristics are used to drive two sets of BJTs ($Q_1$ and $Q_3$, $Q_2$ and $Q_4$). The $\Delta V_{EB}$ of the proposed BGR is then given as

$$\Delta V_{EB} = V_{EB1} + V_{EB2} - V_{EB3} - V_{EB4} = 2V_T \cdot \ln(N) + V_T \cdot \ln \left( \frac{I_{c3}}{I_{c1}} \right) + V_T \cdot \ln \left( \frac{I_{c4}}{I_{c2}} \right),$$

(10)

where the emitter area ratios of $Q_3$ to $Q_1$ and $Q_4$ to $Q_2$ are both $N = 24$. Analyzing the collector current of each BJT, $Q_1$ and $Q_3$ are biased from the classic PTAT current ($I_{R1} = \Delta V_{EB}/R_1$). However, the collector currents of $Q_2$ and $Q_4$ are mainly the temperature-insensitive current $I_0$ mirrored by $M_6$, which are changed by the compensation currents $I_{co1}$ and $I_{co2}$. Thus, the high-order temperature characteristics of $\Delta V_{EB}$ are changed.

The voltage $V_{fb}$ is equal to $V_{ref}$ because of the effects of the amplifier and NMOS source follower $M_9$. The temperature-insensitive current $I_0$ can be expressed as

$$I_0(T) = \frac{V_{ref}}{R_{fb}(T)} = \frac{V_{ref}}{R_{fb}(T_r) \cdot [1 + \alpha(T - T_r)]},$$

(11)

where the temperature also affects the resistance, the current obtained is not strictly temperature-independent.
The drain currents of $M_3$, $M_8$, $M_{10}$ and $M_{11}$ are obtained by mirroring $M_1$, those of $M_2$ and $M_4$ are mirrored from $M_6$, and the parameters $b$, $x_1$, $x_2$, $y_1$ and $y_2$ are the scale coefficients. By substituting (13) into (10), we obtain

$$
\Delta V_{EB} = V_T[2 \ln(N) + \ln(b)] + V_T \ln\left(\frac{x_2 \cdot I_0 + y_2 \cdot I_{R1}}{x_1 \cdot I_0 - y_1 \cdot I_{R1}}\right).
$$

Assuming that $x_2 = cx_1$ and $y_2 = cy_1$, where $c$ is a constant. (14) can be rewritten as

$$
\Delta V_{EB} = V_T[2 \ln(N) + \ln(b) + \ln(c)] + V_T \ln\left(\frac{1 + c y_1/x_1 \cdot I_{R1}/I_0}{1 - c y_1/x_1 \cdot I_{R1}/I_0}\right).
$$

In Equation (15), it can be seen that the curvature compensation term shown as $F_2(T)$ in Equation (8) is introduced into $\Delta V_{EB}$ to compensate for the nonlinearity of $V_{EB}$. Once the desired $\Delta V_{EB}$ is obtained, $I_{R1}$ is mirrored by $M_3$, and the resulting $V_{bgr}$ is expressed as

$$
V_{bgr} = V_{EB} + a \cdot \frac{R_2}{R_1} \Delta V_{EB} = V_{EB} + a \cdot \frac{R_2(T)}{R_1(T)} \left[V_T \ln\left(bcN^2\right) + V_T \ln\left(\frac{1 + c y_1/x_1 \cdot I_{R1}/I_0}{1 - c y_1/x_1 \cdot I_{R1}/I_0}\right)\right].
$$

Substitute (16) into (9) to obtain the final reference voltage $V_{ref}$.

### 2.4. Process Variations and Trimming

The BJTs, resistances, and current mirrors in the proposed BGR circuit are the main sources of error owing to process variations and mismatches. BGR error sources are classified into two types: PTAT and non-PTAT errors. The errors caused by the spread of BJT saturation current and resistances $R_1$ and $R_2$ are mainly of the PTAT type. The BJT current gain spread, BJT base resistance, opamp offset, and BJT collector current mismatches mainly constitute the non-PTAT errors.

PTAT errors are easily eliminated; thus, non-PTAT errors often determine the achievable precision of the BGR and require additional structures to ensure circuit accuracy. The proposed circuit contains many current mirror structures to provide bias and compensation currents for different BJTs. To minimize mismatches in the current mirrors, cascode-type current mirrors are used in the circuit to improve precision. In addition, the non-PTAT
errors caused by process changes affect the proposed high-order curvature compensation method. The proposed trimming structure is shown in Figure 7.

![Figure 7. Schematic of the proposed trimming structure in BGR circuit: (a) resistance R_{t2} Trimming; (b) compensation current trimming.](image)

Figure 7a is a 4-bit trimming resistance network [16] for I_0 scaling, which is mainly used to ensure that the I_0 change caused by the resistance spread does not affect the curvature compensation precision. At the same time, the change of I_0 will also change the parameters c in (16). Figure 7b also depicts a 4-bit trimming structure for scaling the compensation currents I_{co1} and I_{co2} in the proposed circuit. This trimming structure is connected to the two nodes A and B shown in Figure 6 to change the parameters y_1/x_1 in (16) and achieve curvature compensation trimming. The two trimming blocks ensure appropriate curvature compensations in the presence of process variations or different application requirements. There are also trimming resistance R_{t1} connected to the output to adjust the reference voltage V_{ref}. All trimming signals are generated by a fuse module controlled by the digital unit in our BMIC chip.

3. Experimental Results

Firstly, the temperature characteristics of some key points are analyzed based on the simulation results. Figure 8a presents the simulation results of V_{EB} and \Delta V_{EB} with temperature changes. The nonlinear \Delta V_{EB} and V_{EB} present complementary slope trends in the range of −40 to 125 °C.

![Figure 8. Simulated results of (a) V_{EB} and \Delta V_{EB} versus temperature; (b) the first-order and proposed compensation of V_{bgr} versus temperature.](image)
The bandgap voltage $V_{bgr}$ before and after curvature compensation is shown in Figure 8b. $V_{bgr-1order}$ is a first-order compensation result achieved after removing nonlinear compensation. The simulated results reveal that the maximum and minimum differences in $V_{bgr}$ are reduced from 2 mV (without curvature compensation) to 0.2 mV (with curvature compensation) in the range of $-40$ to $125$ °C. The best-found TC of $V_{bgr}$ is 0.7 ppm/°C in the simulation result shown in Figure 8b.

Figure 9 presents the 500 runs Monte Carlo (MC) simulation results of the proposed BGR with a 5 V supply voltage. The variation ($\sigma/\mu$) of the reference voltage from MC results is 0.271% in Figure 9a. In Figure 9b, the statistical distribution of the TCs indicates that the average TC is 2.63 ppm/°C and the standard deviation is 1.48 ppm/°C. The MC simulation results show that the circuit is insensitive to mismatch.

![Figure 9](image_url)

Figure 9. Statistics of untrimmed Vbgr from a 500-run Monte-Carlo simulation. (a) $V_{bgr}$ @ 27 °C; (b) TC in ppm/°C of $V_{bgr}$.

Figure 10a presents the chip microphotographs of proposed high-precision BGR circuit in the designed BMIC, which was implemented in a 0.18 µm BCD process. The whole BMIC area is $2.8 \times 2.8 \text{ mm}^2$, and the BGR circuit occupies a chip area of $0.38 \times 0.27 \text{ mm}^2$. We designed a BMIC test circuit to test the temperature and other related characteristics of the reference voltage of the chip. In the test circuit, place the BMIC in a white circle whose size corresponds to the cover of the temperature controller, isolated from other power supply and control modules, as shown in Figure 10b. This is to independently test the BMIC while simulating rapid temperature changes, ensuring accurate testing. At the same time, on the PCB, the relevant signals are connected to the outside of the white circle to ensure that the reference voltage changes can be monitored without affecting the temperature test.

![Figure 10](image_url)

Figure 10. (a) Chip microphotograph of the proposed BGR circuits; (b) Photo of the BMIC test platform.
Figure 11 presents the measured temperature dependence of the bandgap voltage $V_{\text{bgr}}$ and the reference voltage $V_{\text{ref}}$ from $-40$ to $125 \, ^\circ\text{C}$ for six chips. The untrimmed $V_{\text{bgr}}$ results are shown in Figure 11a. Process deviations cause the BGR output voltage to exhibit a positive temperature sensitivity, with an average TC of $26.04 \, \text{ppm/}^\circ\text{C}$. Figure 11b presents the measured $V_{\text{ref}}$ results after TC trimming and voltage magnitude trimming. The tested optimal and worst TCs were $2.56$ and $4.75 \, \text{ppm/}^\circ\text{C}$, respectively, and the $\sigma/\mu$ of the reference voltage is $0.11\%$ at room temperature. The untrimmed inaccuracy is about $\pm0.43\%$ (the maximum and minimum difference of $V_{\text{bgr}}$ is $10.3 \, \text{mV}$) over a temperature range of $165 \, ^\circ\text{C}$, which decreases to approximately $\pm0.05\%$ (the maximum and minimum difference of $V_{\text{ref}}$ is $2.4 \, \text{mV}$) after trimming at ambient temperature.

![Graph](image1.png)

**Figure 11.** Measured TCs of six samples: (a) untrimmed $V_{\text{bgr}}$ as a function of temperature; (b) trimmed $V_{\text{ref}}$ as a function of temperature.

In Figure 12a, it can be seen that the $V_{\text{ref}}$ remains stable by continuously reducing the input voltage from $5.5 \, \text{V}$ to $4.5 \, \text{V}$. Figure 12b presents the variation of six reference voltages versus supply at room temperature. When the supply voltage is increased from $4.5$ to $5.5 \, \text{V}$, the average variation in $V_{\text{ref}}$ is $0.58 \, \text{mV}$. Therefore, the average line sensitivity is $0.023\%/\text{V}$.

![Graph](image2.png)

**Figure 12.** Measured reference voltage versus supply voltage: (a) oscilloscope monitoring results; (b) six chip measurement results.

Table 1 summarizes the performances of the proposed BGR and compares it with some state-of-the-art designs. Compared to other BGR circuits, the proposed design achieves excellent temperature insensitivity, with a TC of $2.56 \, \text{ppm/}^\circ\text{C}$ in the range of $-40$ to $125 \, ^\circ\text{C}$. The current consumption of BGR is $53 \, \mu\text{A}$ with a $5 \, \text{V}$ supply voltage, and the area of the fabricated BGR circuit is $0.103 \, \text{mm}^2$. 
Table 1. Performance summary and comparison with other works.

| Tech (µm) | Year | Supply Voltage (V) | Reference Voltage (V) | Temperature Range (°C) | TC Range (ppm/°C) | LS (%/V) | Power (µA) | PSRR (dB) | Area (mm²) |
|----------|------|-------------------|-----------------------|------------------------|-------------------|--------|----------|----------|-----------|
| 0.18     | 2021 | 1.2–2.4           | 0.628                 | −40–120                | 2.5–5             | 0.03   | 64.2     | −91.4 *  | 0.024     |
| 0.18     | 2019 | 3.5–5             | 3.11                  | −40–130                | 4.6–7.6           | 0.031  | 108      | −92 *    | 0.223     |
| 0.18     | 2017 | 5.2               | 3.65                  | −40–110                | ±3σ               | N/A    | 750      | −127     | 0.063     |
| 0.13     | 2015 | 1.2               | 0.735                 | −40–120                | 9.3               | N/A    | 120      | −80      | 0.036     |
| 0.18     | 2014 | 1.2               | 0.767                 | −40–120                | 4.9               | 0.54   | 36       | −74      | 0.12      |
| 0.16     | 2011 | 1.8               | 1.088                 | −40–125                | 5–12              | 0.48   | 55       | −84 *    | 0.103     |
| 0.18     | 2022 | 5                  | 2.5                   | −40–125                | 2.5–4.75          | 0.023  | 53       |          |           |

* Simulation results.

4. Conclusions

A 2.5 V, 2.56 ppm/°C high-order curvature-corrected BGR over a temperature range of −40 to 125 °C is presented herein and implemented using 0.18 µm BCD technology. The circuit is based on the classic BGR structure using currents of different ratios and TCs to bias two sets of BJT pairs, thereby introducing nonlinear terms with compensation effects in ∆VEB to achieve temperature-independent voltage. The proposed structure is suitable for high-precision battery monitoring applications, such as EVs, energy storage, etc. Furthermore, this circuit has been used in the designed BMIC.

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