Analysis and Design of the Soft-Switched Clamped-Resonant Interleaved Boost Converter

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Abstract—This paper presents the detailed analysis and design of a soft-switching DC-DC converter called clamped-resonant interleaved boost converter (CRIB). This topology, thanks to a resonant L-C tank connected between the drain terminals of the switches of two interleaved boost cells, achieves zero-voltage and zero current commutations of all devices, independently of the load current, with a reduced dv/dt across the switches, making the converter suitable for high-frequency operation. Moreover, a proper no-load operation is proved, whenever the minimum voltage gain is higher than a given threshold. Differently from previous works on current-fed resonant converters, the presented theoretical analysis includes the effect of the input filter inductors, allowing to derive a simple design procedure to meet the given specifications. According to the outlined design steps, an experimental prototype was built, rated at 42–54 V to 400 V–300 W. Measurements confirm the theoretical predictions, showing an efficiency above 96% at the nominal power in the whole input voltage range. Finally, the possibility to reduce the overall magnetic volume by coupling the two input inductors is demonstrated.

Index Terms—Interleaved boost converters, resonant DC-DC converters, soft-switching.

I. INTRODUCTION

THE interface between photovoltaic panels as well as fuel-cells and the grid in distributed energy generation systems, but also battery powered loads, like headlamps in the automobile environment, are examples of applications that can benefit from converter topologies capable of providing high voltage conversion ratios, together with a smooth input current absorption. Moreover, when the load power increases, interleaving operation becomes an attractive feature, thanks to the reduced device current rating and total input current ripple. From this standpoint, the interleaved boost converter is the simplest topology that can be used, but its hard-switching characteristics limits the increase of the switching frequency, and can represent a source of electromagnetic noise, which is not acceptable in sensitive environments, like in cars or airplanes.

Many examples of soft-switching interleaved boost converters employing passive auxiliary snubbers can be found in literature. Some of them employ coupled inductors to boost the voltage gain while providing ZCS turn on for the switches, like in [1] and [2]. A simple turn-off inductor is proposed in [3] that employs just two auxiliary diodes and one capacitor, but hard turn on with reverse recovery diode problems still exists. A more complex passive structure was proposed for a high power factor rectifier in [4], allowing ZCS turn-on and ZVS turn-off of the switches at the price of using more six diodes, three auxiliary capacitors and three auxiliary inductors, plus coupled windings on the main boost inductors. The snubber used in [5] was inherited by solutions already proposed for the single boost converter and allows for ZCS turn-on and ZVS turn-off of the switches. Unfortunately, the switches suffer from a severe increase of their voltage stress caused by the added auxiliary circuit.

As already known, the major drawbacks of passive snubbers are the duty-cycle limitation due to the time needed to reset their condition at each commutation, and the increased switch current stress. These aspects can be mitigated by using active soft-switching cells, like in [6]–[14]. In some of these examples, like in [7], [10], [11] and [14], the auxiliary switch drain-source voltage is not clamped, thus exposing it to high frequency ringing and possible overvoltage.

A different approach was proposed in [15], for a current-fed push-pull topology, by exploring the resonance between the switches’ output capacitance and the transformer magnetizing inductance, which is connected between their drain terminals. The converter exploits the added degree of freedom, offered by the use of a synchronous rectification, to allow for a duty-cycle control at constant switching frequency, but its ZVS condition is load-dependent. Moreover, the resonant transitions, as well as the effect of the input inductors in the resonance mechanism, are ignored. The same approach was applied to an interleaved boost converter in [16], to the interleaved boost/flyback converter in [17] and to the interleaved boost converter with an asymmetrical voltage doubler rectifier in [18], [19]. Paper [16] proposes a variable frequency control, while papers [17]–[19] claim the possibility of using the duty-cycle to control the output voltage at constant switching frequency, which is not possible, as it will be proved in the converter analysis reported in the following sections. This fact was also demonstrated, not only in [16], but also in [20]. The latter presents an interleaved boost converter with a symmetrical voltage doubler rectifier, that employs a variable inductor, as resonant element, to control the converter gain at constant switching frequency, although with a rather limited regulation capability. In any case, the
The involved sub-topologies are described in [21], while Fig. 1(b) shows the same circuit with a voltage doubler rectifier. This paper, based on the work presented in [21], is aimed to fill the gaps left by the previous works, and specifically:

- It demonstrates the possibility to reduce the overall magnetic volume by coupling the two input inductors
- It shows a detailed design procedure, starting from given converter specifications
- It derives the equations for controlling the output voltage/power by varying the switching frequency
- It demonstrates, for the first time, the possibility of no-load operation, with an exact analysis that highlights the role of the different converter parameters
- It provides a thorough analysis of the converter operation
- It derives the equations for controlling the output voltage/power by varying the switching frequency (Section III)
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The presented theoretical analysis and design were validated by experimental results, reported in section V, taken on a 42–54 V to 400 V–300 W converter prototype based on the topology of Fig. 1(b).

II. CONVERTER OPERATION

The two topologies shown in Fig. 1 are equivalent and can be studied in an unified manner by analyzing the basic scheme and considering an equivalent output voltage $V_o' = \alpha V_o' (I_o' = \alpha I_o')$, with $\alpha = 1$, or $\alpha = 0.5$, for the basic and the voltage doubler configuration, respectively. The circuit is assumed symmetrical, i.e., $L_a = L_b = L$. The switching period is divided into eight sub-intervals. However, being the converter operation symmetrical in each half-switching period, we limit the analysis to interval $0 \leq t \leq T/2$. The involved sub-topologies are described in Fig. 2. Differently from the previous works [15]–[20], the input current is not assumed constant, thus allowing to select the input inductors value based on the desired total input current ripple, that will be reduced as a result of the interleaved operation. In the following, current $i_2(t)$ stands for $i_2(t)$ and the same equations apply to $i_2(t)$ in the second switching half period. The analysis here reported is done in normalized form, using the notation $u = v/V_o$ and $i = i/I_o$ for normalized voltages and currents, respectively. Moreover, lowercase letters indicate instantaneous variables, while uppercase letters are used for constant values, like DC quantities or voltage and current values at particular time instants (as also indicated in Fig. 3).

The following base quantities and parameters are used:

$$V_N = V_o', I_N = \frac{V_o}{Z_N}, Z_N = Z_r \cdot \frac{1 + \lambda}{\lambda}, \quad \lambda = \frac{L_m}{L}, \quad \theta = \omega_s t, \quad (1)$$

where

$$Z_r = \sqrt{\frac{L_m}{C_r}}, \quad \omega_s = \frac{1}{\sqrt{L_m C_r}}, \quad L_m = \frac{1}{L} + \frac{1}{L_m}. \quad (2)$$
where $J_{10}$ and $J_{m0}$ are the normalized current values in the corresponding inductor at the end of the previous sub-interval. At instant $t_4$, the diode current $i_{D_1}(t) = i_m(t) - i_{m0}(t)$ goes to zero, causing the turn off of $D_1$. The interval duration is calculated as follows:

$$\theta_{12} = \theta_3 - \theta_1 = \frac{\lambda}{1 + \lambda \left(1 - \frac{1}{M_i}\right)}.$$  

**Interval** $t < t_{t_3}$ (see Fig. 2(a)). This is the same topology of the first sub-interval, with different initial conditions, $i_m(t_2) = i_{m0}(t_2)$, $v_r(t_2) = V_o$. Accordingly, we have:

$$j_m(\theta) = J_{m0} + \frac{J_{co}}{1 + \lambda} \left[1 - \cos(\theta)\right] + \frac{1}{M_i(1 + \lambda)} \left[\theta - \sin(\theta)\right],$$  

$$j_L(\theta) = J_{co} \cos(\theta) + \frac{1}{M_i} \sin(\theta) + j_m(\theta),$$  

$$u_r(\theta) = \frac{\lambda}{1 + \lambda} \left[J_{co} \sin(\theta) + \frac{1}{M_i} \left[1 - \cos(\theta)\right]\right],$$

where $J_{co} = J_{co1} - J_{co0}$ is the normalized initial resonant capacitor current. The intrinsic voltage gain that appears in the above equations is defined as:

$$M_i = \frac{V_o}{V_r}.$$  

The interval duration is determined by the instant the resonant capacitor voltage tends to reverse polarity, thus forward polarizing the other switch body-diode ($D_b$). From (13), we can derive:

$$\theta_{31} = \theta_3 - \theta_2 = \arccos\left[1 - M_i \left(\frac{1 + \lambda}{1 + \lambda M_i}\right)\right].$$

**Interval** $t_3 < t < t_6$ (see Fig. 2(b)). During the clamping phase, current $i_m$ starts to rise while current $i_{m0}$ decreases, both in a linear fashion, i.e.,

$$j_m(\theta) = J_{m1} + \frac{1}{M_i} \left[\theta - \theta_1\right],$$

$$j_L(\theta) = J_{co} \cos(\theta) + \frac{1}{M_i} \sin(\theta) + j_m(\theta),$$  

$$u_r(\theta) = \frac{\lambda}{1 + \lambda} \left[J_{co} \sin(\theta) + \frac{1}{M_i} \left[1 - \cos(\theta)\right]\right],$$

where $J_{co1}$ and $J_{co0}$ are the normalized current values in the corresponding inductor at the end of the previous sub-interval. At instant $t_6$, the diode current $i_{D_1}(t) = i_m(t) - i_{m0}(t)$ goes to zero, causing the turn off of $D_1$. The interval duration is calculated as follows:

$$\theta_{12} = \theta_3 - \theta_1 = \frac{\lambda}{1 + \lambda \left(1 - \frac{1}{M_i}\right)}.$$  

From the above analysis and the main waveforms shown in Fig. 3, it appears that, during intervals $[t_5, t_6/2]$ and $[t_6, t_7]$, one switch and the other switch’s body-diode are conducting, thus short circuiting the resonant tank. Changing the turn-on interval of the two switches does not modify the duration of these two intervals, labeled $D_a$ and $D_b$ in Fig. 3, thus impeding the use of the duty-cycle (at constant switching frequency) as the control variable (the same conclusion can be found in [16] and [20]).
III. Design Considerations

The analysis reported in the previous section is used here to calculate the amount of power transferred to the load as well as the conditions to achieve a proper no-load operation. The final goal is to devise suitable design criteria to meet a set of given specifications.

A. No-Load Condition

The converter can operate at no load whenever the resonant voltage $v_r(t)$ peak value does not exceed the equivalent output voltage. In this condition, the first sub-interval ends when the resonant voltage, after a half cycle, returns to zero, thus forward polarizing the body-diode of the non-conducting switch. The main waveforms, at the boundary condition, are reported in Fig. 4. All currents have a zero average value, as a consequence of a zero output power. The resonant voltage waveform is described by (5), and the sub-interval duration is given by:

$$J_{C0a} = J_{0a} - J_{m0}.$$  

Using (3) and (16) together with the condition $j_m(\theta/2) = 0$, the initial condition $J_{m0}$ results:

$$J_{m0} = -\frac{1}{1 + \lambda} \left( J_{0a} + \theta/2M_i \right).$$  

Then, the input inductor current initial value is derived from:

$$J_{L0a} = 2J_{m0} \left( \alpha \theta/2 - 2\theta_m \right).$$  

The specification on the maximum switching frequency can then be used to find a constraint on the resonant frequency through (23). Clearly, in order to reduce the conduction losses under no-load condition, the switching frequency can be further increased, until the overlapping angle is shrunk to zero.

The plot of the overlapping angle $\theta_m$ given by (25), as a function of the intrinsic voltage gain $M_i$ and the parameter $\lambda$, is shown in Fig. 5. This figure highlights a very weak dependency of $\theta_m$ from $\lambda$, and also reveals a minimum value for the intrinsic voltage gain $M_i$ that guarantees a correct no-load operation, i.e., a positive $\theta_m$ value. By imposing the condition $\theta_m = 0$ from (25), it is possible to find numerically such a critical voltage gain for different $\lambda$ values, as can be seen in Fig. 6. As a final remark, this converter is able to operate at no load only if the voltage gain is higher than the minimum value reported in Fig. 6.
The condition for the resonant voltage to reach zero during interval \([t_2, t_3] \) is that the amplitude of the co-sinusoidal term in (13) is higher than its DC term, i.e.,

\[ (26) \]

If \( M_i \geq 2 \), the above condition is satisfied for any \( \lambda \) value, being the latter a positive non-zero quantity. Being the minimum intrinsic voltage gain for a correct no-load operation higher than 3 (see Fig. 6), guaranteeing this condition automatically ensures the ZVS condition. This analysis reveals a positive aspect of this topology, for which the ZVS condition is load independent.

### C. Average Output Current

From Fig. 3, exploiting the output capacitors charge-balance condition that holds in steady-state, we get:

\[ (27) \]

Expressing (27) in normalized form and using (10), we obtain:

\[ (28) \]

where \( \theta_{sw} = \omega_r T_s \) is the normalized switching period. Clearly, for topologies employing the voltage doubler rectifier, the actual normalized output current is \( J_o = \alpha J'_{o} \) with \( \alpha = 0.5 \). (28) shows the dependency of the output current on \( J_{C1} = J_{i1} - J_{m1} \), thus revealing the importance of including the input inductors as part of the overall resonant inductor \( L_r \) anytime the input current ripple is not negligible.

### D. Output Power Transfer

In order to calculate the power transferred to the output at a given switching frequency, let’s exploit the steady-state condition for the input inductor currents. The only approximation involved in this derivation is related to sub-interval \( \theta_{01} \), that is considered small enough to assume \( \sin(\theta_{01}) \approx \theta_{01} \) and \( \cos(\theta_{01}) \approx 1 - \theta_{201}^2/2 \). In this way, expressions (3) and (4) can be simplified into the following linear equations:

\[ (29) \]

\[ (30) \]

Combining (29) and (30), the normalized capacitor current \( J_{C1} = J_{L1} - J_{m1} \) at the beginning of the energy transfer sub-interval is

\[ (31) \]

Now, using (9), (12), (15), the normalized inductor current values at the end of each sub-interval are:

\[ (32) \]

\[ (33) \]

\[ (34) \]

Combining (30), (32), (33) and (34), being angles \( \theta_{01} \) and \( \theta_{12} \) functions of \( J_{C0} \) and \( J_{C1} \) respectively (see (7) and (10)), a first equation with the two unknowns \( J_{C0} \) and \( J_{C1} \) is found that, together with (31) allows to determine the normalized capacitor
The average input current, assuming unity efficiency, is power we can write:

\[ \text{currents are increasing. Neglecting interval approximately, during interval that the total instantaneous input current value on each input inductor. Looking at Fig. 3, we can observe } \]

\[ F. \text{ Input Current Ripple} \]

The interleaved arrangement of this topology allows a reduction of the overall input current ripple, compared to the value on each input inductor. Looking at Fig. 3, we can observe that the total instantaneous input current \( i_\text{in} = i_{\text{in}1} + i_{\text{in}2} \) increases, approximately, during interval \( T_{\text{on}} \), where both input inductor currents are increasing. Neglecting interval \( T_{\text{on}} \) at nominal power we can write:

\[ \Delta I_{\text{in}} = 2V \frac{\theta_{a}}{L} \approx 2V \frac{\theta_{a}}{L\omega_{r}} \left( \frac{\theta_{a}}{2} - \theta_{12} + \theta_{13} - \theta_{3} \right). \]  

(36)

The average input current, assuming unity efficiency, is expressed as \( I_{\text{in}} = MJ_{r}^2 \). Accordingly, the relative input current ripple is (the normalized output current is used):

\[ r_{\text{in}} = \frac{2}{M J_{r}^2} \left( \frac{\theta_{a}}{2} - \theta_{12} - \theta_{3} \right). \]  

(37)

\[ \text{ IV. Design Steps} \]

In this section, the detailed design procedure is outlined based on the specifications listed in Table I. Note that the considered topology is the one with the voltage doubler rectifier of Fig. 1(b), so that \( V_{\text{o}} = \alpha V_{\text{n}} = 200 \text{ V}. \)

\[ A. \text{ Resonance Frequency} \]

The converter resonance frequency is calculated so as to guarantee a no-load operation at the maximum input voltage \( (M_{\text{max}}) \) and at the desired maximum switching frequency \( (f_{\text{max}}) \). From the analysis carried out in the previous section, we learned that, in no-load condition, the converter behavior is hardly affected by parameter \( \lambda \). Thus, the analysis can be simplified setting \( \lambda = 1 \) in all equations from (19) to (25), and, from (23), the resonance frequency is calculated as follows:

\[ f_r = \frac{f_{\text{max}}}{\pi} \left[ \sqrt{M_{\text{max}}^2 - M_{\text{min}}^2} + \frac{1}{2} \arccos \left( \frac{1}{2M_{\text{max}}} \right) \right]. \]  

(38)

With the given specifications, the above equation yields \( f_r = 513 \text{ kHz}. \)

\[ B. \text{ Input Inductors} \]

Both input and resonant inductors contribute to determine the output current (see the dependency of \( J_{\text{r}} \) in (28) on \( J_{\text{in}} = J_{\text{in}1} - J_{\text{in}2} \), which is a value close to the sum of input and resonant current peak values). The two inductors are derived based on the two constraints given by the need to transfer the nominal power (at minimum input voltage and switching frequency), and to obtain the desired input current ripple. Their value is calculated iteratively, starting by setting the value for the input inductors, which is \( L = 33 \mu\text{H} \). This value can be modified based on the outcome of the following subsections IV-C and IV-D. Specifically, if the input current ripple turns out too high \( L \) should be increased, and viceversa.
the needed resonant capacitor turned out to be $C_r = 5.8 \text{ nF}$. In order to account for converter losses, the selected value was $\lambda = 1$, slightly lower than the calculated one. Based on this value, and using the resonance frequency definition (2), the needed resonant capacitor turned out to be $C_r = 5.8 \text{ nF}$.

Fig. 8 shows other two curves calculated at a different minimum switching frequency: reducing the frequency range, i.e., increasing $f_{s,min}$, will call for a lower $\lambda$ value to obtain the desired output power, with a consequent increase in the resonant current amplitude (lower $L_m$ values are needed), while reducing $f_{s,min}$ leads to higher $L_m$ values and to a higher input current ripple. The selected value of $f_{s,min}$ in Table I is simply a trade off between these different aspects.

As far as the input voltage range is concerned, there are no theoretical limitations. If, for instance, the minimum voltage is reduced (with the same maximum value), the curve in Fig. 8 simply shifts downward, calling for a reduction of the minimum switching frequency and/or of the resonant inductance value (higher current stress), in order to transfer the nominal power. However, for photovoltaic applications, the nominal power is extracted in a narrow input voltage range, while, at different irradiance conditions, the panel voltage may change in a fairly broad range, but the power that needs to be transferred is much lower than the nominal value.

### D. Input Current Ripple

Using (37) at the operating point corresponding to the minimum input voltage and switching frequency and to the nominal power, the input current ripple is estimated. The outcome of this calculation is $r_i = 0.57$, value considered acceptable for prototype testing.

It is interesting to check the switching frequency variation at different input voltage values at the same output power (nominal value) for the designed converter. This behavior is shown in Fig. 9 together with the relative input current ripple. The same figure shows the comparison with the PLECS™ simulation for three input voltage values: the matching with the switching frequency curve reveals the accuracy of the steady-state analysis, while the error in the input current ripple prediction comes from the approximation used (the input current is not perfectly triangular and contains resonant sub-intervals). Nonetheless, the matching is still good, and certainly acceptable for design purposes.

### V. Experimental Results

In order to verify the theoretical analysis, a converter prototype based on the CRIB topology with voltage doubler rectifier (see Fig. 1(b)) was built. The values of the used components are listed in Table II. Each input inductor has been realized in two types based on the CRIB topology with voltage doubler rectifier (see Fig. 1(b)). The values of the used components are listed in Table II. Each input inductor has been realized in two types based on the CRIB topology with voltage doubler rectifier (see Fig. 1(b)).

![Fig. 8. Normalized output current as a function of parameter $\lambda$ (operating points $V_{in}$ and $f_{s,min}$, $f_s = 100$ kHz, $f_s = 200$ kHz).](image)

![Fig. 9. Switching frequency and relative input current ripple as a function of the converter voltage gain (nominal output power). Symbols represent simulation points at three input voltage values: switching frequency marked with $\ast$, relative input current ripple marked with $\diamond$.](image)

| Parameter                        | Symbol | Value       |
|----------------------------------|--------|-------------|
| Input filter inductors           | $L_k = L_b$ | $\approx 32 \mu\text{H}$ |
| Resonant inductor                | $L_m$  | $34.5 \mu\text{H}$ |
| Resonant capacitor               | $C_r$  | $5.8 \text{ nF}$ |
| Voltage doubler capacitor        | $C_1 = C_2$ | $1 \mu\text{F}$ |
| Output capacitor                 | $C_o$  | $1 \mu\text{F}$ |
| Input capacitor                  | $C_{in}$ | $2 \times 0.68 \mu\text{F}$ |
of Litz wire (bundle of 270 strands, having each a diameter of 71 μm). The obtained inductance value was slightly lower than the calculated one ($L_m = 31.5 \, \mu H, L_n = 32.3 \, \mu H$, measured with the Agilent 4294A precision impedance analyzer at 200 kHz). The resonant inductor was built on an EFD25 core (material N87) with 25 turns of Litz wire (bundle of 200 strands, having each a diameter of 50 μm), so as to yield a maximum peak-to-peak flux density variation lower than 100 mT. The measured inductance value is $L_m = 34.5 \, \mu H$, for an equivalent inductance ratio of $\lambda = 34.5/32 = 1.08$. The used resonant capacitor value is 4.4 nF, to account for the non negligible MOSFET’s output capacitance (IPB64N25S3-20 by Infineon) that, from datasheet, ranges from 2.9 nF at $V_{DS} = 25$ V down to roughly 250 pF at $V_{DS} = 200$ V. The diodes $D_2$ and $D_4$ are STTH1003S-Y, while $D_1 + D_3$ are included in the same package as STTH2003, all from STMicroelectronics. The converter was connected to an active load (Chroma ATE 63202) set at constant voltage. The prototype was tested open loop using a simple circuitry, shown in Fig. 10, to generate the logic signals for the gate drivers. An external pulse generator (not shown) provides the variable-frequency, 50% duty-cycle, input signal $v_{in}$ that enters the first comparator $C_1$, used just to have sharp signal transitions. The passive network $R_3 - C_3$ and the second comparator $C_2$ generate a delayed signal $v_{o1}$ that, together with the first comparator output $C_1$ and two logic gates, yields the two interleaved signals $DR_{Sa}$ and $DR_{Sb}$ with a minimum overlap time $t_{ov}$ (adjusted to $\approx 100$ ns).

The main converter waveforms, recorded at nominal input voltage ($V_{in} = 48$ V) and output power ($P_o = 300$ W), are shown in Fig. 11. The switching frequency is $f_s = 193 \, kHz$, very close to the theoretical value of 190 kHz. On the same figure are reported the time instants corresponding to the theoretical analysis, for an immediate comparison with the expected waveforms of Fig. 2: very good agreement is observed except for the small high-frequency ringing on $v_{DS}(t)$ waveforms when diodes $D_2$ and $D_4$ start conducting, caused by parasitic inductances (diode and capacitor internal inductance and PCB traces).

The no-load operation can be observed in Fig. 12, taken at the maximum input voltage ($V_{in} = 54$ V) and zero output power: the boundary condition is shown, where the switch drain-source voltages have a peak value of roughly 200 V. The switching frequency here is $f_s = 435 \, kHz$, slightly higher than the predicted value. On the other hand, a small uncertainty must be expected, being the resonant capacitance heavily affected by the non linear switches output capacitance (see the reduced $dv/dt$ when the drain-source voltages approach zero).

The minimum switching frequency is measured at minimum input voltage and nominal power, and turns out to be $f_{s,min} = 161 \, kHz$, higher than the specified value of 150 kHz, mainly because of the lower $\lambda$ value used in the experimental prototype.

The relation between the output power and the switching period is shown, in normalized form, in Fig. 13, where the outcome of the theoretical analysis is compared with PLECS simulations as well as experimental measurements. As already pointed out in section III, the approximation used to derive the steady-state current values causes the deviation of the theoretical curve with respect to the simulated points at low output power, where sub-interval $\delta t_0$ becomes less negligible. On the other hand, experimental points slightly differ from the
analysis, mainly for the losses in the experimental prototype as well as for the non-linear equivalent resonant capacitance due to the non negligible MOSFET’s output capacitance. The interesting aspect of this investigation is the practically linear relationship between the converter output power and the switching period, that makes it easier to design a suitable controller for closed-loop operation (the curve slope represents a constant system small-signal gain). The photo of the converter prototype is shown in Fig. 14 (resonant capacitor and voltage doubler cell components are mounted on the PCB back side).

The conversion efficiency (power stage only) was calculated measuring input and output powers using digital multimeters (Keysight 34461A), for input/output voltages and output current, while the input current was read directly on the DC power supply Chroma 62050P-100-100. The overall relative error on the efficiency calculation is lower than 0.5%, the main contribution coming from the input current measurement (0.1% of reading plus 0.1% of range). The results are shown in Fig. 15, where curve (a) is taken varying the input voltage at nominal output power, while curve (b) shows the efficiency variation with the output power at nominal input voltage. As we can see, at nominal power, the efficiency is well above 96%, and remains higher than 90% down to roughly 40 W. These encouraging results suggest the possibility to significantly increase the switching frequency so as to reduce the overall volume of the magnetic components, since the topology guarantees zero-voltage and zero-current commutations of all devices.

It could be interesting to analyze how the proposed topology compares with a standard hard-switched interleaved boost (HSIB) converter, operating at constant switching frequency ($f_s = 193$ kHz, corresponding to the nominal operating point). In this case, the theoretical duty-cycle is $D_b = (M - 1)/M = 0.88$, and, assuming the same input current relative ripple (at the nominal operating point), the input inductors turn out $L_b = 53 \mu H$. Selecting two 600 V CoolMOS™ devices (IPB60R120P7 from Infineon) as switches, and two SiC diodes STPSC406 from STMicroelectronics so as to avoid any reverse recovery problem, the estimated main losses, at the nominal operating point, are shown in Fig. 16. As we can see, the device conduction losses are worse in the standard topology mainly because of the higher voltage rating of switches and diodes.

![Fig. 13](image13.png)

**Fig. 13.** Relation between the output power and the switching period in normalized form ($V_g = 48 V$). Comparison between theoretical analysis (continuous line), PLECS™ simulations (discrete points marked with +), and experimental measurements (discrete points marked with *).

![Fig. 14](image14.png)

**Fig. 14.** Photo of the converter prototype.

![Fig. 15](image15.png)

**Fig. 15.** Measured converter efficiency. (a) As a function of input voltage at nominal load (axes on the bottom and to the right). (b) As a function of output power at nominal input voltage (axes on the top and to the left).

![Fig. 16](image16.png)

**Fig. 16.** Estimated converter losses comparison between the proposed CRIB converter and a hard-switched interleaved boost (HSIB) topology.
Fig. 18. Simplification of the input port during each half switching period, when one switch is constantly on.

Fig. 17. Clamped-resonant interleaved boost topology with coupled input inductors.

original topology, where the intrinsic voltage gain definition modifies as \( M = \frac{V_o}{V_i} \). In particular, all the equations reported in section II, remain valid. However, since the calculation of \( J_a \) and \( J_{on} \) in subsection III-D exploits the continuity property of the state variables \( i_{b(t)} \), such calculation is affected by the different current waveform. In particular, (34) is no longer valid, and must be re-written considering the behavior of \( i_{b(t)} \) during the second half switching period (which is identical to \( i_{b(t)} \) in the first half switching period).

For the same reason, the analysis at no-load needs to be modified as well. However, the interested reader can apply the same procedure, here described for the original topology, to derive the modified expressions for the coefficients \( B_{on} \) in the Appendix. In any case, the topology maintains the same positive characteristics in terms of no-load operation and soft-switching capability. To demonstrate it, the implemented prototype was modified substituting the two input inductors with a single ETD34 magnetic core (material N87), with two windings (21 turns of Litz wire each) realized on the core lateral legs. The values obtained were \( L_a = 28.5 \, \mu H, L_c = 11 \, \mu H \), measured at 200 kHz with the Agilent 4294A precision impedance analyzer. With these values, the equivalent inductance results \( L \approx 36 \, \mu H \), very close to the value used with the original topology with separated input inductors. Fig. 19 shows the converter main waveforms, taken at nominal input voltage and output power: note the trapezoidal input current waveform, instead of the almost triangular behavior of the original topology. The measured efficiency was \( \eta = 96.8\% \), slightly higher than the original topology, thanks to the reduced core losses (less core volume and partial flux cancellation in the central leg). Moreover, compared to the two separated RM10 cores, the single ETD34 core achieves a volume reduction of roughly 11%.

VI. COUPLED INPUT INDUCTORS

A magnetic volume reduction can be obtained by coupling the two input inductors using a single magnetic core, as illustrated in Fig. 17. Compared with the original topology, an additional input inductor \( L_o \) appears at the converter input port, thus affecting the current \( i_{b(t)} \) and \( i_{b(t)} \) waveforms. However, considering that each switch remains in the on state during at least one half of the switching period, the input port can be modified as shown in Fig. 18, where a new parameter \( \gamma = \frac{L_a}{L_a + L_c} \) is introduced, and \( L = L_a + L_c \). \( L_c \) is the equivalent input inductance. According to this simplified scheme, the steady-state analysis follows the same steps outlined with the and also because the latter, being SiC diodes, have a higher voltage drop, compared to silicon counterparts. But, the main contribution comes from the device’s switching losses, that deserve a careful investigation. First, we need to consider the losses associated to the discharge of the MOSFET’s output capacitance, which are estimated as \( P_{loss} = 2E_{loss}f_s = 1.5 \, W \) (\( E_{loss} = 4 \, \mu J \) at 400 V from datasheet). The turn-on and turn-off losses are harder to predict because of the lack of accurate data from datasheet, that gives only the rise voltage subinterval at turn off \( t_v = 6 \, ns \), and the fall voltage subinterval at turn on \( t_g = 14 \, ns \), assuming a current rise time at turn on \( t_i = 15 \, ns \) (this value must be lower than the given \( t_{on} = 21 \, ns \)), and a current fall time at turn off \( t_f = 15 \, ns \) (this is a guessed value), the switching losses are \( P_{sw} = 10.8 \, W \) (with no reverse recovery contribution). Thus, the estimated converter efficiency for the standard HSIB converter turns out to be \( \eta_H = 0.937 \), while for the proposed CRIB topology we obtain \( \eta_{CRIB} = 0.977 \), which is roughly 1% higher than the value measured on the prototype.

Fig. 19. Main waveforms in few switching periods for the CRIB topology with coupled input inductors, taken at nominal input voltage and output power \( f_s = 191 \, kHz \). Voltage scale: 40 V/div; current scale: 2 A/div.

VII. CONCLUSIONS

This paper reports the detailed analysis of the CRIB converter, a topology that, thanks to its soft-switching characteristic
independent of load current, is suitable for high frequency operation. Differently from previous works on resonant current-fed topologies, the input inductors are not treated as current generators, because they are involved in the resonance phases and impact on the overall converter performance. The topology proves to be capable of no-load operation, provided that the minimum voltage gain is higher than a given minimum value. The presented analysis allows to derive a simple design procedure, capable of meeting the given specifications.

The possibility to substitute the two input inductors with a single magnetic core with coupled windings is also proved.

To validate the theoretical expectations, a 42–54 V to 400 V –300 W prototype is built and tested: not only the theoretical analysis is confirmed, but the measured power stage efficiency, above 96% at the nominal power in the whole input voltage range, together with the complete soft-switching operation, suggests the possibility to push the switching frequency to higher values, without incurring into an unacceptable efficiency drop. In any case, considering that the soft-switching feature of this topology allowed to avoid any heatsink for the two D2PAK switches mounted on a standard 2-layers PCB (see Fig. 14), we can conclude that, even in the chosen frequency range, its power density is likely to be higher than its hard-switched counterpart.

APPENDIX

Steady-state analysis. As said in section III, combining (30), (32), (33) and (34), and using (7) and (10), following equation, with the two unknowns $J_{CO}$ and $J_{CI}$, is found

$$\frac{B_i}{J_{CO}} + B_2 J_{CI} + B_4 = 0,$$  

(40)

being

$$B_i = \frac{1 + \lambda}{2\lambda},$$  

(41)

$$B_2 = \frac{\lambda}{1 + \lambda \left[ \frac{1}{M_i} - \frac{1}{M_f} \right]},$$  

(42)

$$B_4 = \frac{\theta_{2s}}{M_f} \frac{\lambda}{1 + \lambda} \left( 1 - \frac{\lambda}{1 + \lambda} \frac{1}{M_f} \sin(\theta_{2s}) - \frac{\theta_{2s}}{M_f} \right),$$  

(43)

where $\theta_{2s}$ is given by (14). A second equation with the same variables is (31), here reported

$$J_{CI} - J_{CO} - \frac{B_4}{J_{CO}} = 0,$$  

(44)

with

$$B_4 = \frac{1 + \lambda}{\lambda} \left[ \frac{1}{M_i} - \frac{1}{2} - \frac{1}{2\lambda} \right].$$  

(45)

Combining (40) and (44), a simple second order equation is solved, giving

$$J_{CO} = -\frac{B_1}{2B_2} + \sqrt{\left( \frac{B_1}{2B_2} \right)^2 - \frac{B_4}{B_2}},$$  

(46)

$$J_{CI} = J_{CO} + \frac{B_4}{J_{CO}}.$$  

(47)

These expressions allow to determine all current values and the output power for any given operating point.

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