Electronic Bottleneck Suppression in Next-generation Networks with Integrated Photonic Digital-to-analog Converters

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Digital-to-analog converters (DAC) are indispensable functional units in signal processing instrumentation and wide-band telecommunication links for both civil and military applications. In photonic systems capable of high data throughput and short delay, a commonly found system limitation stems from the electronic DAC due to the delay in sub-micron CMOS architectures and E-O conversions. A photonic DAC, in contrast, directly converts electrical digital signal to optical analog one with high speed and low energy consumption. Here, we introduce a novel parallel photonic DAC along with an experimentally demonstration of a 4-bit passive iteration of DAC. The design guarantees a linear intensity weighting functionality with a 50Gs/s and much smaller footprint compares to any other proposed photonics DACs. This design could be potentially implemented into novel photonic integrated neuromorphic computing engines for next generation label processing and edge computing platforms.

Keywords: Digital-to-analog converter, Photonic, Parallel Processing, networks

Introduction
The total annual global IP traffic is estimated to reach 4.8 ZB per year by 2022¹. The continuous increase of both low-delay access and efficient processing of data demands novel platforms that can perform computational tasks closer to the edge of the network, thus enabling to analyze important data efficiently and in near real-time. In this context, most of the data travel in optical fibers which supports both high channel rates and throughput. Yet, the network’s bottlenecks in terms of power consumption and throughput are found in limitations arising from connections and interfaces at its edge; that is, peripheral input/output (I/O) devices such as digital systems or sensors require a digital-to-analog conversion (DAC), and vice versa (ADC)²³. Therefore, it becomes a pressing challenge, especially for large-scale data centers, to optimize or even re-invent their networks for meeting the needs of large data processing and low delay without trading power consumption.

Photonic integrated circuits (PIC) have shown the potential to satisfy the demand of high data-processing capabilities while a) acting on optical data, while b) interfacing with digital systems, and doing so at featuring compact size, short delay, and low power consumption². However, the performance gains of photonic platforms when interfacing with digital architectures are reduced by their interfaces to/from electronics, which often due to the achievable bandwidth and the resolution of the DACs and ADCs in addition to cumbersome domain-crossings between electronics (E) and
optics (O). The ultimate performance and power consumption of this DSP-based technological pathway will be constrained by CMOS technology that is approaching its fundamental physical limit. A DAC, for software-defined transmitters or as interface to computing systems, should be able to operate conversions at high speed, for a broadband spectrum, and in an accurate manner, without being affected by jitter and noise. Due to the maturity of the electronic components, electronic digital-to-analog conversion devices can provide high-accuracy, and high linear conversion trend accompanied by remarkable stability; nevertheless, they are intrinsically limited by their bandwidth and high timing jitter, which precludes the further development of purely electronics-based DAC for next-generation information systems. High speed electronic D/A can be based on multi-ladder voltage/current weighting circuits, switch and latch architectures or a combination of segmented architectures in addition of binary weighting. Currently, for achieving greater sampling rate, and improve the high-speed performance, the converter design comprises multiple data converters with analog circuitry, such as Time or Analog Bandwidth Interleaving and Multiplexed DACs. However, the delay in sub-micron CMOS architectures, due to the high resistance of the interconnection wires and the increased parasitic capacitance, can seriously compromise the very high frequency performances.

In the past decade, paying the cost of a larger footprint, several high-speed optical DACs (ODACs) compatible with fiber communication have been proposed, based on different schemes, such as optical intensity weighting of multiwavelength signal modulated using micro-ring resonators, nonlinear optical loop mirrors, or interferometry and polarization multiplexing or phase shifters. Therefore, to overcome the bandwidth limitations and timing jitter of current electronic-only DACs, requiring a cumbersome opto-electric-opto (OEO) conversions, i.e. improving delay and energy consumption while not trading off footprint, developing a photonic-based binary-weighted DAC (BW-DAC) becomes a main prerogative.

Considering that the bandwidth of state-of-the-art DACs is lower than that of state-of-the-art electro-optical modulators, and being inherently immune to electromagnetic interference, this DAC can simultaneously enable high-speed sampling rates and high conversion efficiency, while not being affected by jitter and electromagnetic noise, and most importantly, allow to by-pass O-E-O conversion, thus facilitating network simplicity and possibly cascadability to other photonic networks. In addition, the BW-DAC is intrinsically compatible with optical fiber communication systems; therefore, they could be used for low-latency label processor, routing data in miniaturized switching networks, or interface to data processor and classifiers at the edge of the network.

Specifically, in our vision, BW-DACs will be an essential device towards the realization of the next generation networks, which comprises photonic circuits, replacing inefficient D/A conversions and bulky devices. High speed photonic DAC can be used at the interface of network-edge photonic dedicated devices, in the fog, such as digitally controlled transmitters and receivers or photonic computing architectures, which can significantly lower the cost of running a network by providing edge-cloud capabilities. At higher level in the network, the DAC can be used as digitally controlled photonic micro datacenters and routers for intelligent re-direction of the traffic and label processing (Fig.1).
Figure 1: Schematic representation of the impact and potential uses of a photonic digital-to-analog converter (PDAC) in a 5G network. The DAC would be used at the interface between the electronics and photonic platforms both in the fog and cloud layer, such as photonic computing, intelligent routing, and label processing at the edge of the network and within servers in the cloud.

More recently, few photonic DAC implementations have been proposed, which can be categorized as serial or parallel according to their operating scheme. The serial type (Fig. 2b) is usually based on the summation of weighted multiwavelength pulses opportunely spaced in time by properly setting the wavelength spacing and the length of dispersive medium, which recreates an analog waveform after being detected by a photoreceiver, enabling fast digital to analog conversion. Serial DAC can be straightforwardly cascaded for long-distance optical communication systems, which primarily operates in serial mode. The operating speed is hindered by multiple factors, such as pulse source and stability, dispersion component, optical modulator, and dispersion compensator. In this scheme, bit resolution trades off with sampling frequency. Experimental studies show 4bit serial DAC with an operating speed of 12.5Gs/s.

On the other hand, parallel type (Fig. 2a), are generically characterized by a simpler architecture and usually employs electro-optic modulators (EOMs) to weight the intensities of multiple optical carriers according to an electrical digital signal input and subsequent summation at the end of optical link. Parallel schemes can potentially leverage on a lower power consumption, while taking full advantage of the combined fast sampling rate and rather high-bit resolution, provided by the multiple parallel channels. One main limitation comes from the summation of the modulated optical carriers, since for achieving a full dynamic range and linear operation the optical signals need to be added coherently (in phase). The technical issue related to the incoherent summation is primarily addressed by the photodetectors which integrates the optical power and additional electronics, which, however, limiting the operating bandwidth, hence conversion latency of typical parallel photonic DACs.
Although, the conversion in the electrical domain by means of a photodetector is not necessarily desirable, especially for those applications which would still benefit from keeping the analog signal in the optical domain, such as optical machine learning\textsuperscript{16-21} or optical telecommunication\textsuperscript{12,23}. (Fig. 2)

\textbf{Figure 2} Schematic representation of three different implementations of photonic DACs (Parallel, serial and Coherent-parallel). \textbf{a}) The parallel implementation is based on weighted integration of multiple wavelengths which encode a bit sequence. \textbf{b}) The serial scheme is based on summation of weighted multiwavelength pulses opportunely spaced in time by properly setting the wavelength spacing and the length of dispersive medium. \textbf{c}) Coherent parallel photonic DAC [this work] uses a pre-set unbalanced directional coupler that split light unevenly in different channels, which are then individually modulated at high speed, the pre-determined phase shift (in case of a 0 or 1) is actively compensated with phase shifters towards a coherent summation.

In this work, we propose an original and synergistic-to-implement parallel type photonic BW-DAC scheme which exploits a combination of unbalanced couplers\textsuperscript{24} and electro-absorption modulators (EAMs), or alternatively also electro-optic 2x2 switches, for overcoming the issues related to the uncoherent summation without requiring any conversion to the electrical domain. (Fig. 2c) In this
configuration, in fact, a series of unbalanced couplers divides the optical power in multiple branches in a seemingly exponential manner; thence EAMs are employed for absorbing the optical power in each branch according to a digital electric signal. In this way, the EAMs will modulate the intensity of the optical signal travelling in each branch only if triggered by a digital input ‘0’; this would lead also to an alteration of the optical path length in a systematic, hence controllable manner. The systematic phase variations, in fact, can be easily compensated through PIC-integrated heaters or high-speed phase modulators, added at each branch, enabling a coherent summation. As such, the novel approach introduced here entirely avoids additional electronics or large-area photodetectors. In this work, we demonstrate a passive iteration of the 4-bit parallel BW-DAC, and show the potential of conversion speeds of 50 GS/s along with energy consumptions as low as few pJ/S. We also analyze the performance degradation due to limited extinction ratios of the applied electro-optic modulators, the integral and differential nonlinearities, highlighting a seamlessly linear digital-to-analog conversion. This simple and relatively compact scheme can be employed in network-edge processors enabling low latency computing or high-speed routing such as for miniaturized data centers.

Figure 3 Schematic diagram of a 4-bit Photonic DAC based on unbalanced directional couplers and electro absorption modulators. 

a) Schematic of the working principle. b) Sketch of a photonic DAC in parallel configuration. A carrier (CW Laser) is split in multiple branches thanks to unbalanced directional coupler (i.e. SEM image of the directional couplers and its operation) according to the formula: \((1-r)^n\) where \(r\) is the splitting ratio \((r=0.75)\) and \(n\) is the number of bits. The intensity of the signal is modulated in each branch by an electro absorption modulator (Extinction Ratio=4.6dB) according to a digital input electrical signal. In presence of a ‘0’, a systematic phase shift is added to the branch allowing to compensate for the optical pathlength variation afterwards modulation. The optical signals are phase-coherently summed by means of a combiner (ii. SEM image of the combiner and device principle). c) Microscope taken image of passive 4-bit DAC circuit with the integration of thermal phase tuner for the digital input ‘1’’1’’1’. d) Optical measurements of a passive 4-bit DAC. The output for each digital input configuration is collected by an Infrared camera. The layout of the photonic DAC (red) is superimposed to the infrared image for easy understanding. This passive iteration shows the optical power for the digital input ‘1’’1’’1’.
We demonstrate a N-bit electro-optical D/A conversion utilizing asymmetrical directional coupler, for binary weighting according to the DAC resolution, and Y-combiner (Fig. 3). Following this concept, the BW-DAC converts the parallel digital signals comprising of N-bits into an analog output signal in the optical domain utilizing a silicon PIC. For the operation, in brief; a single continuous wave laser is coupled into the PIC passed through a sequence of asymmetrical directional couplers with a splitting ratio of 3:1$^{24,26}$, which results to the best linearity of output optical power vs digital bit inputs. By design, each consecutive channel $i$, here named bit-waveguide, receives a fraction of the optical power ($r = 0.75$) incoming from the previous unbalanced coupling stage, the analog signal power can be written as:

$$E_i = r(1-r)^{N-i}E_{\text{input}}$$

In this way, we obtain N separated continuous and weighted waves travelling in N channels (i.e. each waveguide presenting a bit), which represent the intensity weighting factors corresponding to each bit of the digital input signals. Thus, the resolution of the BW-DAC given by the number of waveguides $N$. Thanks to the pre-determined and successive splitting obtained by the series of unbalanced couplers and the systematic correction of phase alteration, the signal, modulated according to the N-bit sequence, is in-phase combined by a sequence of Y-junctions. $I = \frac{cE_{\text{in}}}{\sqrt{2}} |E|^2$

The final optical power output with the combination of each channel is given by:

$$P_{\text{Analog}} = \left( \frac{1}{2} \sum_{i=2}^{N} \left[ r(1-r)^{N-i}E_{\text{input}} \exp \left( -2\pi \frac{r}{\lambda} \kappa_{(0,1)}^{L} \right) + r(1-r)^{N-i+1}E_{\text{input}} \exp \left( -2\pi \frac{r}{\lambda} \kappa_{(0,1)}^{L} \right) \right] \right)^2$$  Eq. 1

with $i$ being even numbers between 2 and $N$, e.g. \{2, 4, ..., N\}. (see methods). The final analog optical signal (Eq. 1) can be either collected and converted by photodetectors for obtaining an electrical analog signal or kept in the optical domain, for interfacing other photonic platforms, such as neuromorphic photonic computing or micro-router. In fact, it is the latter that enables simplicity and low signal delay cascadability of optical network and is the main value proposition of this BW-DAC introduced here.

To assess its correct working principle of the PDAC scheme and understand its performance, several passive implementations of a 4-bit BW-DAC ($N = 4$) representing different bit-combination ($2^N = 16$) are prototyped. For example, when the $i^{th}$ bit represents a ‘1’, then the $i^{th}$ bit-waveguide is use as is, thus preserving the optical power passing through the combiners. Contrarily, to emulate in a passive fashion the $i^{th}$ bit being equal to a ‘0’, we simply disconnect the $i^{th}$ bit-waveguide from the PDAC output port and thus simulating zero optical power. Notice, that in this way there is a vanishing amount of optical leakage power contributing to the optical analog output signal, thus overestimating the DACs performance. To assess the correct functionality of the passive iteration of the PDAC, we perform full wave FDTD 3-dimensionsal simulation for a 2-bit DAC, which indeed shows near perfect agreement with the experimental results (supplementary online material, Fig. S1). In our experimental demonstration of a 4-bit PDAC, a CW laser source is coupled to the circuit by means of grating couplers and successively split to each arm with sequential weights (Fig. 3a, SOM). The 16 states of the 4-bit BW-DAC prototype demonstration is experimentally validated as individual circuits, where each circuit represents one-bit combination (SOM). Note, for the operation, a predetermined bias voltage was applied to metal heaters to tune the phase of waveguide (Fig. 3d).
To demonstrate the correct functioning of the coherent photonic DAC, a total of 16 passive (with systematic active tuning of the phase) 4-bit PDAC circuits were measured using optical probe station. (the infrared image of measured ‘1111’ PDAC circuit is shown in Fig. 3C). We perform numerical simulations (see methods section) to verify the design functionality and gain insights into the experimentally tested PDAC performance including an analysis of i) delay (throughput), ii) frequency and phase stability, and iii) DAC benchmarks such as differential nonlinearity. In brief, we use foundry-approved device models for improved yield and repeatability, and timely time-to-market; the EAMs have an extinction ratio of 4.6 dB and are driven by NRZ pulse generator to inject the binary digital bit sequence at 50 Gbit/s (supplementary online information).

![Figure 4 Digital to analog conversion. (a) Generated optical power of the analog signal for different 4-bit combinations. Comparison between the Experimental results obtained for all the possible \(2^n=16\) passive versions (blue solid line), the photonic circuit simulated version (gold solid line) and the theoretical prediction according to the formula (red solid line). (b) Eye diagram of a 4bit DAC assuming thermal noise of the PD, static (1ps) and random jitter (1ps) of the pseudo-random code used as digital input of the electro-absorption modulators. (c) Integral and (d) Differential nonlinearity for a given electrical digital signal inputs for measured analog outputs correspond to 1LSB respect to the best fit regression. The DNL is between -0.94 and 0.71LSB while the INL is smaller than 1.99LSB.]

The measured and simulated output optical powers of the PDAC are in good agreement with each other as highlighted by the (expected) quadric trend, which reflects the relationship between the linear superposition of the electric field waves at the Y-junctions and the resulting intensity (Eq.1, Fig. 4b). The discrepancies between the model and the experimental case are associated with the reflections at the waveguide dislocation representing the different bit-combinations and scattering at the Y-junctions.
In the passive implementation, the circuit that represents the digital input combination ‘0000’, obviously provides zero optical power output due to the pruned bit-waveguides. In the numerical simulation instead, which accounted the presence of modulators in each arm, a small amount of 2.6 µW (10% of pass through optical power) output power was recorded, due to the limited extinction ratio of the modulators, which leads to an offset error between numerical and experimental outputs. Furthermore, the optoelectronic components, i.e. the modulator and detector (if used back-end), are associated to physical noise; for instance, the electrical signal driving the modulators is affected by phase jitter and intensity noise, whilst for detecting the output signal a and SINAD correspond to the measurement results are 65 and 10, respectively. The two values correspond to the result of dynamic simulation are 67 and 11 which are significant higher that other PDAC structures. It indicates the high accuracy of this PDAC.

|                | Speed (GS/s) | Power (mJ/bit) | FOM (GS/s-mJ/bit) | Footprint (mm²) | Resolution (#bit) |
|----------------|--------------|----------------|-------------------|-----------------|-------------------|
| Electronic off-chip | 55-65        | 375            | ~0.2              | 2.0             | 8                 |
| Electronic off-chip | 0.1          | 17             | <0.01             | 20.2            | 8                 |
| Electronic on-chip | 100          | 312            | 0.3               | 1.6             | 8                 |
| Huang et al     |              |                |                   |                 |                   |
| This work       | 50           | 20             | 2.5               | ~4.0            | 8                 |

*Table 1.* Summary of the state-of-the-art photonic integrated DAC and commercially available electronic DAC. Where this work’s performance is calculated based on the speed of SiGe EAM provided by IMEC, power consumption of eight EAMs and six thermal phase shifters.

|                | Speed (GS/s) | DNL (unitless) | INL (unitless) | ENOB (unitless) | Resolution (#bit) |
|----------------|--------------|----------------|----------------|-----------------|-------------------|
| Parallel PDAC  | 2.5          | 0.5            | 0.5            | 4.1             | 4                 |
| Serial PDAC    | 12.5         | 0.1            | 0.5            | 3.0             | 4                 |
| This work      | 50           | 0.9            | 2.0            | 10.4            | 8                 |

*Table 2.* Summary of the state-of-the-art photonic integrated DAC and proposed off chip parallel and serial photonic DAC.

Finally, we are interested in comparing the performance of this PIC-based PDAC with electronic approaches selecting a medium-high 8-bit resolution (*Table 1*). We use our experimental-numerical cross-validation approach from the 4-bit prototype for the 8-bit resolution performance analysis. Focusing on the core-functionality of DACs, namely the ratio of the conversion speed divided by the dynamic power we find that the PDAC has an 10x higher sampling-speed-efficiency than a speed-comparable electronic on-chip implementations and an about two orders of magnitude
higher than a non-chip integrated system. Additionally, the PIC offers a competitive footprint being 5-times smaller than the off-chip commercially available DACs but having double the size of the electronic on-chip counterpart. This may come as a surprise to electronic circuit designers, since the critical dimension in PICs is often regarded being 10-100x larger compared to electronics. The reason for only a 2x areal increase lies in the small footprint of GeSi EAM and elegant weighting mechanism by introducing sequence of asymmetrical directional couplers which do not require large on-chip space.

Moreover, the operating speed and power consumption of the BW-DAC is mainly limited by the performance of the modulators. Thus, sample speed will linearly increase with component (modulator) speed improvement in future generations, which is unlike electronic circuits where circuit delay is dominated by interconnect delay which does not improve with device performance improvement such as scaling. Regarding the maximum resolution, the PDAC is limited by the signal discrimination (i.e. extinction ratio) of the modulators; here the optical power of the LSB needs to exceed the leakage power of the MSB when the input digital signal for the MSB is ‘0’. Numerical results predict a possible resolution up to 14-bit considering absorption modulator with a 4.6-dB extinction ratio (see methods and SOM). Meanwhile, we compare this work with other off-chip parallel and serial photonic approach (Table 2). For most of the proposed PDAC, they chose to use off-chip set up to verify the functionality of devices, there is no power consumption or footprint discussion. So, we chose to compare other FOM of PDAC such as DNL, INL and ENOB. The higher value DNL and INL are mainly caused by the nonlinear power summation of serial of Y-combiner circuit.

In conclusion we designed and engineered a novel, easy-to-fabricate, Electro-Optical-DAC (EO-DAC) scheme, in which the intensity of optical carriers is split by unbalanced directional couplers, weighted according to multiple input digital signals which drive foundry-ready electro-absorption modulators, and ultimately summed using combiners at the end of the photonic link. The design guarantees a super-linear intensity weighting functionality with a prospective operating bandwidth of 50 GS/s, consuming as low as 3 pJ/S. We experimentally demonstrate a 4-bit passive iteration of the proposed EO-DAC which is in perfect agreement with both full-wave and integrated circuits simulations. Additionally, the proposed scheme does not require the signal to be converted in the electrical domain as other parallel photonic DAC, and therefore could support the I/O interface to novel photonic integrated neuromorphic computing engines and edge-computing platforms for routing.

**Methods**

*Mathematica description of the PDAC operations:*

The optical carrier of each bit-waveguide is fed into an EAM, which tunes the intensity of the electric field travelling in the waveguide $a^{(1,0)} = \exp\left(-\frac{2\pi}{\lambda} \kappa^{(0,1)}_{\text{eff}} L\right)$ being $\kappa^{(0,1)}_{\text{eff}}$ the imaginary part of the effective refractive index of the propagating mode for the on (‘1’) and off state (‘0’) and $L$ the length of the electro-absorption modulator. The power of the optical signal travelling in the $i^{th}$ bit-waveguide is tuned according to $i^{th}$ input bit with a dynamic extinction ratio of 4.6 dB (up to 5.2dB) and an operating frequency up to 50 GHz. The optical power at the $i^{th}$ bit-waveguide can be written as

$$P_{i^{th}\text{-bit-wg}} = \left[r(1-r)^{N-i}E_{\text{input}}\exp\left(-\frac{2\pi}{\lambda} \kappa^{(0,1)}_{\text{eff}} L\right)\right]^2$$
Where \( r \) is the splitting ratio of directional coupler. The most (least) significant bit, MSB (LSB) digital signal controls the modulator with the highest (smallest) amount of optical power i.e. \( i = \mathrm{N} \) \( (i = 1) \). The driving voltage thresholds associated to the bit sequence is attenuated using the EAMs or unaltered (insertion losses of the modulator). According to the presence of a ‘1’ or a ‘0’, a systematic phase variation is introduced in each arm, which was designed to be compensated using thermal phase tuner. The electric field from two consecutive bit-waveguides is linearity additive.

\[
E = E_1 + E_2
\]

For a monomodal waveguide, the local intensity is related to the amplitude of electric field \( I = \frac{c \epsilon_0 n |E|^2}{\sqrt{2}} \). Based on the proportional relationship between power density and E-field, the power density can be generalized by

\[
P_{l,i-1} = \frac{E_i^2 + E_{i-1}^2 + 2E_iE_{i-1} \cos \Delta \varphi}{2}
\]

where \( \Delta \varphi = \varphi_i - \varphi_{i-1} \). Considering that phase tuners were used for compensating the variations of the phase induced by the EAMs \( (\Delta \varphi = 0) \), the optical power at each combiner output is given by:

\[
P_{\text{Analog}} = \sum_{i=2}^{N} \left\{ r(1-r)^{N-i}E_{\text{input}} \exp \left\{-\frac{2\pi}{\lambda} \frac{k_i(0,1)}{r_i \text{eff} L} \right\} \right\}^2
\]

with \( i \) being even numbers between 2 and \( N \), e.g. \{2, 4, ..., N\}.

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