Sparse Matrix-Matrix Multiplication on Multilevel Memory Architectures: Algorithms and Experiments

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Abstract

Architectures with multiple classes of memory media are becoming a common part of mainstream supercomputer deployments. So-called multi-level memories offer differing characteristics for each memory component including variation in bandwidth, latency and capacity. This paper investigates the performance of sparse matrix multiplication kernels on two leading high-performance computing architectures—Intel’s Knights Landing processor and NVIDIA’s Pascal GPU. We describe a data placement method and a chunking-based algorithm for our kernels that exploits the existence of the multiple memory spaces in each hardware platform. We evaluate the performance of these methods w.r.t. standard algorithms using the auto-caching mechanisms. Our results show that standard algorithms that exploit cache reuse performed as well as multi-memory-aware algorithms for architectures such as KNLs where the memory subsystems have similar latencies. However, for architectures such as GPUs where memory subsystems differ significantly in both bandwidth and latency, multi-memory-aware methods are crucial for good performance. In addition, our new approaches permit the user to run problems that require larger capacities than the fastest memory of each compute node without depending on the software-managed cache mechanisms.

1 Introduction

Complex memory subsystems with multiple levels of memory are part of both recently deployed supercomputers [1][2][3] and proposed future deployments [4]. The use of different types of memory is driven by multiple factors including cost, performance and energy. This results in significant variation in memory bandwidth and latency. Additionally, with growing diversity of solutions due to the inclusion of byte-addressable non-volatile memories, this discrepancy in memory bandwidth and latency is expected to increase. Such systems will experience much greater variability in memory access times due to the asymmetry of read/write access times. These complexities lead to the question “do algorithms have to be redesigned to account for these multi-memory subspaces?”.

Bender et al. considered two-level memory and corroborated the need for multilevel algorithms using simulation [5]. That particular study focused on sorting algorithms and was limited to simulation due to the unavailability of hardware. It used Sandia National Laboratories’ Structural
Simulation Toolkit (SST) simulator for projecting the behavior of multi-level memory aware algorithms. This study was extended later to a k-means clustering in [7]. In this paper, we consider this theoretical work in the context of a new linear algebra kernel, and evaluate it on two different hardware with complex memory subsystems and varying levels of concurrency.

Our primary focus is on the development and optimization of sparse matrix-matrix multiplication (SpGEMM) kernels for complex memory subsystems. This kernel is of interest in a variety scientific computing applications as SpGEMM is the most expensive kernel in many algorithms including the setup phase of multigrid methods. Sparse matrix-matrix multiplication also has applicability in data analysis problems as it is a foundational kernel for the GraphBLAS effort [8]. Many graph analysis problems can be expressed in terms of SpGEMM [9, 10]. Hence optimizing SpGEMM on multilevel memory architectures has the potential to impact a wide variety of applications. The baseline SpGEMM algorithm used in this study has been shown to outperform equivalent vendor implementations [11, 12] (On average 12% and 2.56× faster than best MKL method and cuSPARSE [12]). This algorithm has become the default in Trilinos [13]. Hence, improving the performance of this SpGEMM algorithm will directly impact a number of exascale computing applications that rely on Trilinos. This baseline algorithm was also used as a kernel within the linear-algebra based triangle counting method [10] where Wolf et al. demonstrated that linear-algebra based methods can be as fast as graph traversal based methods when using the SpGEMM algorithm.

Since the Bender et al. paper, Intel has provided the option to treat the high bandwidth memory (HBM) as a “cache” on KNLS. This is despite the latency costs of HBM being higher than one would typically expect from a “cache”. Software managed mode is still an option for applications that will not fit into HBM, but where cache mode does not perform well. On the GPU, memory accesses to host pinned DDR memory is allowed and Unified Memory (UVM) accesses work similar to the “cache” mode. All these options allow a number of variations of the standard algorithms that can be run in real hardware. This raises the question “When and where are two-level algorithms needed for an optimized kernel like SpGEMM?” We develop a two-level scratchpad memory-aware “chunked algorithm”, and compare it to a highly optimized traditional, one-level aware algorithm with all the vendor provided options for ease-of-use of multilevel memories.

The contributions of this paper are summarized below.

• We provide a thorough performance analysis of the baseline state-of-art SpGEMM method using different memory subsystems on GPUs and KNLS. This analysis studies the effects of access patterns, selective data placement methods and cache-modes provided by the architectures on the performance of SpGEMM.

• We identify which data structures are critical in the performance of SpGEMM on these architectures. Using this, we propose a data placement method and chunking-based algorithm that better exploits multi-memory subsystems.

• We evaluate the performance of these methods w.r.t. standard algorithms on GPU and KNLS. Using the different characteristics of the memory subsystems in these architectures, we demonstrate where and when the proposed chunked algorithm and data placement strategies are useful for the SpGEMM kernel.

2 Background

Some of the earliest work on the porting of algorithms to multiple pools of memory with differing performance occured during the very earliest days of computing. In previous machines, application
working sets would have been written to physical media and then loaded back into the limited volatile memory stores for processing in blocks.

Recently the emergence of GPU-based accelerators \[14\] has reinvigorated interest in the algorithms field due to the limited memory capacities available on GPU-based compute engines. Our anecdotal experience has been that many application developers porting to GPU-based systems have opted to house their data sets entirely resident in the GPU memory because the cost of transfer has been too high to sufficiently amortize during execution. The recent addition of NVIDIA’s NVLINK bus \[15\], which provides much higher data transfer bandwidth, has the potential to change this balance in favor of buffered algorithms.

The arrival of Intel’s Knights Landing processor \[16, 17\], which was one of the first modern HPC processors to provide multiple classes of memory on a single die, provided new opportunities for algorithmic optimization because data structures no longer needed to be entirely resident in any specific class of memory. Instead, developers have been given additional choices, where data structure placement can significantly affect performance \[18, 19, 20, 21\]. Intel’s forthcoming Optane class memory \[22, 23\], will add additional algorithm challenges and opportunities. In these systems, byte-addressable non-volatile memory technology will be available, enabling much larger memory capacities than ever before. However, this increased capacity will sacrifice performance and present significant asymmetry in read and write operation times. The use of multi-memory aware methods and a development focus on data reuse has the potential to alleviate some of these concerns but will require new families of algorithms to be developed.

Bender et al. \[7\] proposed a theoretical model that describes four necessary properties for algorithms to benefit from a chunked variant: (1) memory boundedness; (2) computation that can be broken down in scratch pad size chunks; (3) computation where cache chunking is insufficient, and, (4) computation that can reuse data loaded into a scratchpad. This follows from their earlier work on sorting \[5\] which showed that chunking based algorithms can benefit sorting. Although this work provides a thorough study, the proposed model does not consider the latency-based differences between the memory subsystems. Our work experimentally validates these properties on knls, and extends these studies for the memory subsystems with differing latency characteristics, e.g. GPUS.

There are multilevel algorithms in other contexts such as between SSD and DDR. Zheng et al. \[24\] have shown that two level memory algorithms are useful for sparse matrix times a dense vector/matrix operation. This work is similar to our data placement strategy where they hold the dense vector/matrix in memory. A recent work \[25\] can be considered similar to our chunking algorithm for two level SSD and DDR memory algorithm for a sequential implementation. The similarity in sequential chunking for a different level of memory subsystem \[25\] and our performance-portable approach validates the usefulness of the chunking strategy.

2.1 Baseline SpGEMM Method: KKMEM

In a recent work, we introduced a spgemm method, KKMEM \[11, 12\], designed to provide portability and cross-platform performance, which performs well on various architectures such as CPUs, knls and GPUs. KKMEM is a hierarchical, multithreaded 1D/2D row-wise algorithm. It assigns the multiplication of each row to threads. Different multiplications within the row are assigned to different vector lanes. KKMEM is a two-phase algorithm: the number of non-zeros in each row of the result matrix is calculated in the first (symbolic) phase, then the actual values are computed in the second (numeric) phase. We focus on the numeric phase in this paper.

KKMEM uses a compression technique to encode multiple columns of the right hand side matrix with fewer integers. This reduces the number of operations and the memory requirements in the symbolic phase (See \[11, \ref{10}\] for effects of compression on different matrices). This also permits the
use of bitwise operations from union/intersection of different rows. Our implementation uses sparse hashmap-based accumulators together with a uniform memory pool for better memory scalability.

Figure 1 gives an example of a simple multiplication. Assume that a single thread performs the whole multiplication. The rows of \( A \) will be processed sequentially with each row being multiplied with the nonzeros of the corresponding rows of \( B \), to compute a single row of \( C \). The arrows in the figure show the data access order for the multiplication of the first row. The entry in column, \( a_{11} \), of \( A \) is read, and multiplied with the entries in corresponding row of \( B \) (first row). Every non-zero in the first row of \( B \) is read and multiplied and the results are inserted into an accumulator. Then next column of \( A \) \( (a_{16}) \) is read, and algorithm reads through the 6th row of \( B \). The results of the multiplication are inserted into hashmap accumulator. When all multiplications are completed the accumulator writes the values back to the corresponding row of \( C \).

This \texttt{spgemm} algorithm is a more challenging kernel than sorting for multilevel chunked algorithms as it has been heavily optimized for efficient memory accesses and cache reuse both on GPUs and KNL systems [11]. Bender et al. observed that if cache chunking is sufficient one might not benefit from scratchpad based algorithms. While the \texttt{spgemm} implementation does not perform cache chunking explicitly, it does optimize for spatial locality. There are number of other variants \texttt{spgemm} based on implementation on different architectures, data structures used and partitioning employed. Deveci et al. [11, 12] provide a summary of the most recent work that differ based on these parameters. Theoretical approaches for avoiding communication in parallel \texttt{spgemm} have been extensively studied [26, 27]. However, all these approaches are limited to one level memory. Deveci et al. is also one of the fastest implementations that we are aware of on KNLs and GPUs. Related benchmarks can be found in [11, 12], and [https://github.com/kokkos/kokkos-kernels/wiki/SpGEMM_Benchmarks]. We adapt this highly scalable, performance-portable \texttt{spgemm} algorithm to two-level memories on two different architectures.

This \texttt{spgemm} algorithm has also been used as part of a fast triangle counting approach on matrices from social networks [10], which has been shown to be faster than highly optimized graph-based implementations. Using this, we also demonstrate the effect of memory systems on triangle counting problem.

3 Performance Analysis of KKMEM

We analyze the memory accesses of KKMEM [11] analytically and experimentally on multilevel memories on KNLs and GPUs. These analyses establish the need for strategies for handling multilevel memories differently on different architectures.
3.1 KKMEM Access Patterns

Based on the access patterns given in Figure 1 and explained in previous section, some key observations on these access patterns follow:

- **A** is read in a stream-like fashion. Each entry is read once and used in many multiplications. The accesses to **A** are regular regardless of its structure. **C** is written in the same order as **A**. Each entry in **C** is written only once in a streamed fashion, and oblivious to its structure. Single row \( j \) of **B** is accessed as many times as the non-zeros in the column \( j \) of **A**. If each column of **A** has uniform degree \( (\delta) \) we will read **B** \( \delta \) times. These accesses to **B** can be irregular based on the structure of **A**.

- The number of insertions to the accumulators are as many as the number of multiplications. Depending on the type of accumulator, **B**’s structure might affect the memory accesses. For example, the first row of **B** would insert first and last positions of the dense accumulators, resulting in non-localized memory accesses breaking **spatial locality**. Having narrow **B** rows (low bandwidth) improves the spatial locality for dense accumulators. On the other hand, accesses to sparse accumulators have high locality regardless of **B**’s column indices, since they use much smaller memory. This improves the locality in the hashmap accumulators. However, the structure of **B** might affect the number of hash comparisons based on the collusions when sparse hashmap accumulators are used as in KKMEM.

- **Temporal locality** is exploited by accessing a recently accessed row of **B**. For example, the multiplication of first row requires the first and last rows of **B**. They are not accessed again until the multiplication of the last two rows of **A**. On the other hand, multiplication of the third row of **A** accesses the second and third rows of **B**. These rows are immediately used in the multiplication of the fourth row of **A**, and they are likely to be in the cache. As a result, having overlapping columns in consecutive rows of **A** improves temporal locality.

- **Cache Prefetching** reduces the latency cost by prefetching the data based on a heuristic which is typically spatial locality. When rows of **B** are very sparse, prefetching might bring data from the next row, which may never be used. For example, in Figure 1 multiplication of the first row of **A** might prefetch data from the second row of **B** after accessing first row of **B**. This row is not used in the multiplication of first row, and may not be used in the following multiplications based on the structure of **A**. When the rows of **B** gets larger, these dense rows are likely to be prefetched and useful flops can be achieved with a lower latency cost.

In summary, we expect most memory cost of KKMEM to be based on **B** accesses depending on the structure of **A**. Denser rows in **B** help the performance with prefetching. Better performance is expected when consecutive rows of **A** have similar columns (increasing temporal locality). The temporal locality can be further improved using hypergraph/graph partitioning methods [24]. However, we avoid such preprocessing as they require large number of multiplications to amortize their cost. Based on this analysis, it is not clear whether the insufficient cache chunking property required by the analysis of Bender et al. applies immediately to spGEMM. In addition, how the performance of the algorithm reacts to the bandwidth and latency differences in the memory subsystems requires further analysis. These result are dependent on problem structure and architecture, which are studied below.
3.2 Analysis on KNL

We evaluate 48 different multiplications from four multigrid problem domains that are representative of different (but typical) applications in the scientific computing domain at varying scales. Triple products in the form of $A_c = R \times A_f \times P$ are a key kernel in the setup of multigrid methods to generate a coarser matrix $A_c$ from a fine matrix $A_f$. Figure 2 gives the nonzero patterns for the $R$ and $A$ matrices for one of the problems – Laplace3D. $P$ is transpose of $R$ in our examples. In these scientific computing problems, $A$ matrices usually exhibit a regular structure. The number of nonzeros per row of $A$ are 7, 13, 27, and 81 on Laplace3D, BigStar2D, Brick3D, and Elasticity, respectively. We expect a high temporal locality whenever $A$ is on the left hand side. On the other hand, $R$ is a short and wide rectangular matrix as shown in the figure. The rows have strided columns, and consecutive rows do not have similar structure. Therefore, we expect very low temporal and spatial locality when $R$ is on the left hand side.

Using these four instances, we evaluate the performance of our kkmem implementation using the various memory modes supported on our production Intel Xeon Phi 7250 (knl) systems. These nodes comprise a single socket 7250 Xeon Phi running at 1.4GHz, which have 34 dual-core ‘tiles’ (for 68 cores in total), 16GB of on-package MC-DRAM and 96GB of capacity DDR4 system memory. Each core provides 4-way multi-threading (SMT). We utilize the Intel 17.2 compiler, configured with GCC 4.9.3 for header file and basic system libraries. The results are presented in Figures 3 and 4 are for $A \times P$ and $R \times A$ problems.

We run these experiments using 64 threads (one thread/core), and 256 threads (with four hyperthreads/core). For each problem domain, we scale the size of the $A$ matrix from 1GB to 32GB given on the X-axis (the Laplace problem with 32GB $A$ matrix does not fit into 96 GB DDR and is excluded). The sizes of $R$ and $P$ are usually much lower and differ based on the problem (an example for the sizes of $R$ and $P$ can be found in Table 3, the rationale holds for all sizes). We run both $A \times P$ and $A \times R$ to study the effects of the structure of the matrices on the left and right hand sides of the multiplication, excluding $RA \times P$ and $R \times AP$ as the size of the intermediate results differ for different problems. As a result it is difficult to run weak scaling tests on these configurations. Moreover, they usually show the same trends as $R \times A$. Each run is repeated 20 times with the bars representing the median performance. As the matrix sizes are increased, the overall required size

| $A \times P$ L2-Miss% | Laplace3D | BigStar | Brick3D | Elasticity |
|-----------------------|-----------|---------|---------|------------|
| 21.52                 | 20.51     | 8.51    | 8.23    |
| $R \times A$ L2-Miss% | 55.07     | 30.22   | 13.73   | 3.20       |

**Figure 2**: Examples of the Laplace matrices used in the paper

**Table 1**: L2 Cache Miss Percentages for the $R \times A$ and $A \times P$ Problems
Figure 3: $A \times P$ GFLOPs on KNL. Top and bottom figures present the GFLOPs achieved on 64 and 256 threads, respectively. X axis refers to sizes of $A$ matrices (in GB) used in the experiments.

Figure 4: $R \times A$ GFLOPs on KNL. Top and bottom figures present the GFLOPs achieved on 64 and 256 threads, respectively. X axis refers to sizes of $A$ matrices (in GB) used in the experiments.
for three matrices increases to as much as 90% of the overall memory capacity. At such scales, the runtimes can fluctuate significantly. We added error bars to represent the best performance achieved in 20 repetitions, which we expect to observe in the presence of larger memory capacities.

HBM is run using the KNL flat memory mode — all data is placed into MC-DRAM (HBM). As the overall HBM capacity is 16 GB, this option is only run when the overall problem size requires less than 16GB. DDR is also on the same flat memory mode as HBM but in this configuration all data is placed in DDR memory. Cache16 (Cache8) is run on the KNL nodes with the entire (half) HBM memory used by the hardware to provide caching of accesses to the DDR and the rest available as a flat memory space for data allocation. Even in Cache8 runs we allocate all data structures in the DDR but use the runtimes to show the effect of a smaller (8GB) hardware cache. This simulates what would happen when these kernels are run with real applications.

Figure 3 shows the results for the $A \times P$ multiplication runs. We observe that KKMEM scales beyond the cores with the hyperthreads for almost all multiplication instances (except the Laplace $R \times A$ problem in DDR). Its performance is constant across memory spaces, and it does not take a significant performance change with HBM. These results suggest that KKMEM is not bandwidth bounded on DDR when using 64 threads. We observe benefits of HBM when hyperthreads are enabled based on the matrix properties. Yet, the performance gain on $A \times P$ multiplications are rather smaller compared to $R \times A$. Regular structures of $A$ matrices result in more regular accesses to $P$, and improve the temporal cache locality. This reduces the global memory accesses and decreases the algorithms’ ability to become bandwidth bound. As a result, the effect of the use of HBM on $A \times P$ multiplication is still minimal. On the other hand, for $R \times A$, $R$ has more strided accesses and less reuse of the rows of $A$. This lowers temporal locality, and increases the memory accesses, making the algorithm more prone to be affected by the bandwidth-related overheads. Even with $R \times A$, we observe that the performance differences reduce as we go from Laplace to Elasticity with the increasing $\delta$. As density of $A$ increases, it benefits from spatial locality as well as prefetching opportunities. In general, having high temporal or spatial locality reduce the observed performance difference between HBM and DDR.

To support this theory, first, we run the Kokkos-profiling [28] cache measurement tools to measure the L2 cache misses. These cache-miss ratios are listed in Table 1. In general, we observe that $A \times P$ multiplications have lower L2 cache-miss ratios than $R \times A$ due to $R \times A$’s poor temporal localities. Larger L2 cache miss ratios cause more frequent memory accesses. This exhausts more memory bandwidth and results in larger performance differences between HBM and DDR. One exception to this is in Elasticity, where the performance of $R \times A$ is at least as good as $A \times P$ because of the high density of $A$.

Second, in order to further experiment the effect of the density of right handside matrix, we take the $R$ and $A$ matrices belonging to Elasticity problem, and generate right hand-side matrices for both $R$ and $A$ with increasing $\delta$. For each problem, we measure the achieved GFLOP/s on the DDR and HBM memories modes, as well as the L1 and L2 miss ratios using the Kokkos tools cache profiler. The results are listed in Table 2. Similar to what we have observed, the performance difference between DDR and HBM for $R \times A$ multiplication decreases with the increasing $\delta$. As $\delta$ increases, the algorithm makes use of spatial locality more, which is reflected in the decreasing L1 cache misses. This suggests that, even when the temporal locality is low, additional spatial locality reduces global memory accesses, helping the algorithm to be more resistant to bandwidth changes. We observe smaller performance differences for $A \times P$. For low $\delta$, there are slight performance differences, as we observe for our $A \times P$ multiplications ($\delta$ of $P$ is usually between 3 and 4.5). Note that increasing $\delta$ is likely to reduce temporal locality as we have seen in $R \times A$ multiplication, as bigger rows are

\[\text{Spatial locality is likely to increase L1 hits, while more temporal locality is likely to improve L2 hits.}\]
Table 2: GFLOP/s achieved on DDR and HBM of KNLs for the multiplications of Elasticity’s $R$ and $A$ matrices with randomly generated right hand side (RHS) matrices. L1 and L2 Cache miss ratios are listed on the last two column.

| $\delta$ of RHS | DDR GFLOP/s | HBM GFLOP/s | L1 M% | L2 M% |
|-----------------|-------------|-------------|-------|-------|
| $R \times RHS$  |             |             |       |       |
| 1               | 0.34        | 0.92        | 1.1   | 17.14 |
| 4               | 1.09        | 2.26        | 0.69  | 16.45 |
| 16              | 2.66        | 3.59        | 0.36  | 11.71 |
| 64              | 4.42        | 4.78        | 0.27  | 8.06  |
| 256             | 4.79        | 4.99        | 0.29  | 6.31  |
| $A \times RHS$  |             |             |       |       |
| 1               | 1.17        | 1.69        | 1.09  | 3.96  |
| 4               | 3.00        | 3.27        | 0.89  | 3.14  |
| 16              | 4.19        | 4.32        | 0.46  | 3.98  |
| 64              | 5.00        | 5.02        | 0.3   | 5.1   |
| 256             | 5.07        | 5.14        | 0.29  | 6.1   |

more likely to increase the probability of cache eviction.

Another observation from Figure 3 and 4 is that the KNL caching-modes achieve as good performance as with HBM. While on first thought this is trivial to achieve when the whole problem fits into HBM, it reflects the efficient design of the hardware even when additional caching logic is active. In this experiment, we also study the performance of the cache-mode by increasing the problem sizes, and reducing the effective cache sizes on the KNL processor. We observe that all cache-modes are mostly successful at maintaining the performance achieved by HBM on larger scales. We observe a slight performance difference on Laplace $R \times A$ multiplication, the problem with the worst spatial and temporal locality, between lower cache sizes. However, we conclude that even a small cache-size as low as 8GB is sufficient to achieve HBM performance on large scale problems.

On memory systems differing mainly for bandwidths such as MC-DRAM and DDR, we do not observe high performance differences for kkmem. The performance difference of DDR and HBM decreases with better temporal and spatial locality. Moreover, the vendor-provided cache mode achieves the performance of HBM even for the cases where the problem size is much larger than the cache size. This suggests a reduced need of a multi-level SpGEMM algorithm for memory subsystems where the main differences are in terms of bandwidth.

3.2.1 Selective Data Placement

As shown in the previous section cache-mode maintains the performance of HBM on large scale problems. However, cache-mode is a boot-time (BIOS) option for the compute node. Large-scale KNL systems are known to experience significant node reconfiguration times. Additionally, applications which utilize sparse-matrix multiplication will often use large portions of the system memory for other application data or problem state. In such cases, the application may run in flat mode with a problem size that does not fit into HBM. Anecdotal experience from our production environment at Sandia has shown this mode of execution to be common enough for developers to request support in the Trilinos framework. In these cases, KKMEM performance in DDR can be as low as half of the performance of HBM (Laplace $R \times A$). We can perform a selective data placement (deciding where to allocate specific data structures), where only one or two matrices are stored in HBM. As explained in previous sections, for $C = A \times B$, the accesses to $A$ and $C$ are regular and occur in a streaming fashion in KKMEM. Moreover, since we utilize sparse accumulators, the accesses to these hashmap accumulators are mostly localized in caches. $A$, $C$, and the accumulators are not likely to need higher bandwidth. On the other hand, the accesses to $B$ can be irregular depending on the structure of $A$. As a result, for the cases where HBM cannot store the entire problem, we propose storing only $B$ in HBM to recover HBM performance. We show the effect of this method in the experiments section. This method, DP (data placement), only works when $B$ fits into HBM.
### 3.2.2 Chunking Method For KNLs

Problems where $B$ is larger than HBM requires partitioning of $B$. Column-wise partitions have been explored in one level memory before [29]. However, since our data is stored row-wise, finding column-wise partitions that will fit into HBM is usually prohibitively expensive. Instead, we use a row-wise partition of $B$ as shown in the Figure 5. Assume $B$ is partitioned into three chunks, with each chunk fitting into HBM. Note that, a row-wise partition of $B$ induces a column-wise partition of $A$ as in the figure, as rows of $B_1$ are only accessed by the columns in $A_1$. We avoid explicit column-wise partition of $A$ because of the introduced partitioning overhead in practice. Instead, the multiplication kernel is provided with the row ranges of the $B$ partition, allowing it to skip any columns of $A$ outside of this range (we do not assume that columns are sorted). A slightly modified kkmem kernel is used as a subprocedure to perform a matrix multiplication with row ranges. This kernel first performs $A_1 \times B_1$ to find the partial result $C^1$. Then $C^2$ is found by performing a multiplication and a matrix addition as $C^2 = A_2 \times B_2 + C^1$. This subprocedure is a fused multiply and add kernel. Once a multiplication for row is completed, it inserts the existing values of $C^1$ into its hashmap accumulators to find $C^2$. Algorithm 1 shows the simple chunking strategy for KNLs. First, the number of partitions are found so parts of $B$ fits in memory. With a binary search, we find $P_B$ which stores the begin and end row indices of each partition. Then one by one, each row partition of $B$ (ranges are defined in $B_{rp}$) is copied into fast memory and a fused multiple/add kkmem is used to compute $C$. As observed, there is little room for improvement between DDR and HBM on KNLs in most cases. Hence, we expect the amortization of data movement cost of chunking in only a few cases.

![Figure 5: Example of a simple chunking for KNL](image)

**Algorithm 1** Chunking method for KNL. FastSize refers to HBM size.

| Line | Description                                                                 |
|------|-----------------------------------------------------------------------------|
| 1.   | procedure kkmemKNLchunk(A, B, C, FastSize)                                  |
| 2.   | $np = ceil\left(\frac{\text{size}(B)}{\text{FastSize}}\right)$            |
| 3.   | $pSize = \frac{\text{size}(B)}{np}$                                        |
| 4.   | $P_B = \text{BinarySearch}(B, pSize)$                                      |
| 5.   | for all $B_{rp} \in P_B$ do                                                 |
| 6.   | $FastB = \text{copy2Fast}(B, B_{rp})$                                       |
| 7.   | $C = kkmem(A, FastB, C, B_{rp})$                                            |

### 3.3 Analysis on GPUs

We perform the experiments on the same matrices using NVIDIA’s P100 (“Pascal”) GPUs. Each GPU has a dedicated high bandwidth global memory, which we refer as HBM. In our system, each P100 is connected to the host IBM OpenPOWER8 host-processor architecture with NVLINK (Version 1) [15]. The GPU can access the host CPU pinned memory space directly. Accessing pinned memory has high latency overheads, as well as much lower bandwidth. This is different from KNLs where HBM and DDR have approximately similar latency overheads. Moreover, NVLINK additionally provides unified memory spaces (uvm) that handle data movements automatically between host and...
GPU memories. A data structure that is allocated through UVM can be located in HBM or pinned memory based on the request from host and GPU sides. As a result, UVM works in a similar way to cache-mode in KNLS.

Using these three configurations, we perform the same multiplications as earlier. Results in Figure 6 and 7 show achieved GFLOP/s are usually much higher on the GPU systems than KNLS. We observe much higher performances for $A \times P$ w.r.t. $R \times A$. Both spatial and temporal locality on KNLS translate to coalesced memory accesses on GPUs. Based on the structure of the matrices, a half, quarter, etc., warp may be assigned for the computation of a single row. When a warp is partitioned across the consecutive rows, the structure of $A$ improves coalesced memory accesses since consecutive rows of $A$ are likely to have closer or even the same memory accesses to $P$. Moreover, our algorithm allocates its first level hashmap accumulators in the GPU shared memory. When the values do not fit into first level hashmap, the second level is allocated in the GPU’s global memory. $A \times P$ matrix multiplications tend to have fewer nonzeroes in the result. As a result, most of the hashmap insertions happen in the faster GPU shared memories.

We observe a huge performance drop when host pin memory is used. This suggests that, although kkmem is tolerant to bandwidth drops, it is much more affected by significant memory latency overheads. We expect to see similar differences for wide latency disparity in systems such as non-volatile memory with DDR or HBM.

For problems that fit into the GPU global memory, UVM should not have any overheads, as the data moved to GPUs are never brought back to host memory. Therefore, UVM should not have data movement cost in and out of GPUs during execution. We observe that UVM achieves as low as 30% of the HBM performance for such cases. We observe bigger performances drops with UVM w.r.t. HBM when the problem size gets larger. Whenever the problem requires more memory than HBM, UVM is observed to achieve only the performance of pinned memory. The missing data points in the chart
Figure 7: \( R \times A \) GFLOPs achieved by HBM, Pinned Memory, and UVM on P100 GPUs. X axis refers to sizes of A matrices (in GB) used in the experiments.
The huge performance difference between pinned memory and HBM is used for of the systems, a different chunking strategy is required. For the design decisions, we perform an experiment given in Table 3. In this experiment, we first test the effect of placing different matrices in either HBM or host pin memory. HBM refers to the performance of KKMEM when all data is in HBM, and HostPin refers to its performance when all data is in host-pinned memory. For the other columns, we place one of $A$, $B$ and $C$ ($A \times B = C$) into host-pinned memory while the others are kept in HBM. The sizes (in GBs) of these matrices are given on the right side of the table. When $B$ is placed into host-pinned memory, the performance drop ranges from $7 \times$ to $29 \times$. In these examples, either the sizes of $B$ are large, or they are accessed frequently. As a result, leaving $B$ in host-pinned memory is not a performant option. On the other hand, the effects of placing $A$ and $C$ differs based on the different problems. The effect of placing these matrices into host-pinned memory is minimal whenever the sizes as well as the accesses to these matrices are much lower compared to $B$. For example in Elasticity problem with $R \times A = RA$, the sizes of $R$ and $RA$ are 5% and 11% of the total problem size. Moreover, each row of $A$ is accessed roughly 4.5 times. In this case the accesses to $R$ and $RA$ are around 1% and 3% of the overall memory accesses. On the other hand, when performing Laplace $R \times A$, these ratios and their effects on performance are much higher. The effect of the placement is also high for $A \times P$ multiplication, as $A$ is the largest matrix, and accesses to $A$, $B$ and $C$ are more uniform.

Based on these results, in our chunking algorithm, we chunk all of the $A$, $B$ and $C$ matrices. Note that, there are cases in which keeping $A$ or $C$ in pinned memory does not harm the performance. These are the cases when the sizes of $A$ and $C$ are found to be very small. As a result the cost of the data movements are also expected to be very low. Figure 8 shows a simple chunking method for GPUs. In addition to row-wise partitions of $B$ ($P_B$), now we also have row-wise partitions of $A$ and $C$ ($P_{AC}$). Note that, as in KNLS, we do not physically partition the A column-wise; instead multiplication kernel skips columns of $A$ based on the row range of $B$. For such 2D partitioning algorithm, two different streaming orders of chunks can be followed. For example KKMEMGPUCHUNK1, in Algorithm 2 brings a row-wise partition of $A$ and $C$ into fast memory. This partition of $A$ and $C$ is kept in

| Table 3: Achieved GFLOPs with the different data placements on GPUs. |
|-----------------|-------------------|-----------------|-----------------|
|                 | HBM               | A_Pin           | B_Pin           | C_Pin           | HostPin         | A   | B   | C   |
| Laplace         | RxA               | 3.68            | 2.98            | 0.17            | 1.91            | 0.15 | 2.3 | 4   | 5   |
|                 | AxP               | 16.67           | 3.68            | 1.56            | 0.26            | 0.21 | 4   | 2.3 | 5   |
| BigStar         | RxA               | 10.65           | 9.38            | 0.36            | 3.09            | 0.30 | 1.5 | 6.6 | 3   |
|                 | AxP               | 23.20           | 2.26            | 2.95            | 0.65            | 0.54 | 6.6 | 1.5 | 3.3 |
| Brick           | RxA               | 11.11           | 10.95           | 0.94            | 11.34           | 0.18 | 0.5 | 4   | 1.8 |
|                 | AxP               | 17.10           | 4.15            | 1.45            | 2.24            | 0.37 | 4   | 0.5 | 1.8 |
| Elasticity      | RxA               | 12.94           | 12.75           | 1.08            | 12.89           | 0.44 | 0.25| 3.9 | 0.5 |
|                 | AxP               | 19.34           | 3.71            | 2.19            | 4.87            | 0.50 | 3.9 | 0.25| 0.5 |
This variation copies $B$ changes. Once it finds size becomes $A$ are copied as many as the number of row partitions of $A, AC$ and $C$. Given the high-bandwidth memory size, we make sure that we provide at least 25% of the memory for the matrix that will be copied in the inner loop. First, we try to place the whole matrix into fast memory. If $B$ or $A$ and $C$ fits into the fast memory we achieve optimal data movement cost. However, when we follow these approaches in practice, within a single multiplication, the computation units will not be fully utilized. For this reason, we follow the heuristic in Algorithm 4 for determining the partitions. Given the high-bandwidth memory size, we make sure that we provide at least 25% of the memory for the matrix that will be copied in the inner loop. First, we try to place the whole matrix into fast memory. If $B$ or $A$ and $C$ fits into the fast memory we achieve optimal data movement cost. In this case, we leave the rest of the memory to be used for the other matrices. With a binary search method, we determine the ranges of the rows that fit into fast memory, and call the chunk algorithm with the minimum cost. If neither $A$ and $C$, or $B$ fits into the fast memory, we check the data movement costs of $A$ and $C$ with respect to $B$. We aim to minimize the data movement cost of the larger one by choosing the algorithm that copies it in the outer loop. We further aim to minimize the cost of the inner loop by giving the larger cost matrix the big portion of the fast memory so

**Algorithm 2** Chunking Method: AC in place

1: **procedure** kkmemGPUchunk1($A, B, C, P_{AC}, P_B$)  
2:    **for all** $AC_{rp} \in P_{AC}$ **do**  
3:        $FC = copy2Fast(C, AC_{rp})$  
4:        $FA = copy2Fast(A, AC_{rp})$  
5:    **for all** $B_{rp} \in P_B$ **do**  
6:        $FB = copy2Fast(B, B_{rp})$  
7:        $FC = kkmem(FA, FB, FC, AC_{rp}, B_{rp})$  
8:        $copy2Slow(FC, C, AC_{rp})$

fast memory and partitions of $B$ are streamed to fast memory and multiplied. The algorithm first performs the partial multiplication $C_1^1 = A_1 \times B_1$ ($C_1^1$ denotes partial result for $C_1$), and then brings the next chunk of $B, B_2$. It then performs $C_2^1 = A_2 \times B_2 + C_1^1$. The outer loop in the algorithm copies a row partition of $A$ and $C$ into fast memory. Note that $C$ is initially empty; only its row pointers need to be copied from the slow memory. The inner loop brings different row partitions of $B$ into fast memory. Each iteration of the inner loop calculates a partial result for corresponding rows of $C$. As a result, when the inner loop terminates, a final product is found for the partition of $C$ and this is copied back to slow memory. Then outer loop brings the next $A$ and $C$ into fast memory. The algorithm copies $A$ and $C$ once, while $B$ chunks are copied as many as the number of row partitions of $A$ and $C$. The copy cost of this algorithm becomes $\text{size}(A) + \text{size}(C) + \text{size}(B) \times \|P_{AC}\|$.

A variation of Algorithm 2, kkmemGPUchunk2 given in Algorithm 3, brings the row partition of $B$ into fast memory and streams through $A$ and $C$ chunks by switching the two for loops with small changes. Once it finds $C_1^1 = A_1 \times B_1$, it moves to next chunks $A_4$ and $C_2$ to perform $C_2^1 = A_4 \times B_1$. This variation copies $B$ ones, while $A$ and $C$ are copied as many times as the number of partitions of $B$ ($C$ is partially copied in the first part). The copy cost becomes $(\text{size}(B) + \text{size}(A) \times \|P_B\| + \text{size}(C) \times (\|P_B\| - 1))$.

Given the parts $P_{AC}$ and $P_B$, we calculate the data movement cost of both methods, and we choose the method with the smaller cost. Note that, the data movement of kkmemGPUchunk1 is minimized by reducing the number of partitions of $A$ and $C$. This provides the maximum space for $A$ and $C$ and we use the rest for $C$. Similarly, the copy cost of the variation (kkmemGPUchunk2) is minimized by reducing the number of partitions of $B$, by providing $B$ the maximum space. However, when we follow these approaches in practice, within a single multiplication, the computation units will not be fully utilized. For this reason, we follow the heuristic in Algorithm 4 for determining the partitions. Given the high-bandwidth memory size, we make sure that we provide at least 25% of the memory for the matrix that will be copied in the inner loop. First, we try to place the whole matrix into fast memory. If $B$ or $A$ and $C$ fits into the fast memory we achieve optimal data movement cost. In this case, we leave the rest of the memory to be used for the other matrices. With a binary search method, we determine the ranges of the rows that fit into fast memory, and call the chunk algorithm with the minimum cost. If neither $A$ and $C$, or $B$ fits into the fast memory, we check the data movement costs of $A$ and $C$ with respect to $B$. We aim to minimize the data movement cost of the larger one by choosing the algorithm that copies it in the outer loop. We further aim to minimize the cost of the inner loop by giving the larger cost matrix the big portion of the fast memory so
Algorithm 3 Chunking Method: B in Place
1: procedure kkmemGPUchunk2(A, B, C, P_{AC}, P_B)
2:   for all B_{rp} \in P_B do
3:     FB = copy2Fast(B, B_{rp})
4:   for all AC_{rp} \in P_{AC} do
5:     FC = copy2Fast(C, AC_{rp})
6:     FA = copy2Fast(A, AC_{rp})
7:     FC = kkmem(FA, FB, FC, AC_{rp}, B_{rp})
8:     copy2Slow(FC, C, AC_{rp})

Algorithm 4 Chunking Decision Heuristic
1: procedure Partition(A, B, C, FastSize)
2:   BigPortion = 0.75 \times \text{FastSize}
3:   SmallPortion = 0.25 \times \text{FastSize}
4:   if size(B) < BigPortion then
5:     P_B = [(0, n)] //n = num rows of B
6:     Add left over from big to small portion
7:     Find the balanced partition size pSize_{AC} for A and C
8:     P_{AC} = \text{BinarySearch}(A, C, pSize_{AC})
9:     kkmemGPUchunk2(A, B, C, P_{AC}, P_B)
10:   else if size(A) + size(C) < BigPortion then
11:     Same as above but A and C gets bigger portion
12:     kkmemGPUchunk1(A, B, C, P_{AC}, P_B)
13:   else if size(A) + 2 \times \text{size}(C) > size(B) then
14:     Find pSize_{AC} for A and C using big portion
15:     P_{AC} = \text{BinarySearch}(A, C, pSize_{AC})
16:     Add left over from big to small portion
17:     Find the balanced partition size pSize_B for B
18:     P_B = \text{BinarySearch}(B, pSize_B)
19:     choose the heuristic with lower copy cost
20:   else
21:     Same as above where B gets the larger portion
22:     choose the heuristic with lower copy cost

that its number of partitions are minimized. Once the number of partitions are calculated we call the algorithm with lower copy cost.

4 Evaluation of Data Placement and Chunking Methods

4.1 KNL Experiments

This section evaluates the performance of the selective data placement technique (DP) and the chunking method for KNLS. Comparison of the baseline method KKMEM against state-of-art SPGEMM literature can be found in [11, 12], and is out of the scope of this paper, which focuses on the evaluation of algorithm performance on multilevel-memory systems.

4.1.1 Multigrid Computations

Figure 9 and 10 present the GFLOP/s achieved on A \times P = AP and R \times A = RA multiplications. We only show Cache16 and DDR from Figure 3 and 4 for the simplicity of figures. For all A \times P multiplications, P is smaller than the HBM size, thus, allowing us to run DP for all instances. The performance of KKMEM across different memory systems is similar in these problems. This is also the case for DP method as well. We do not observe a significant benefit of HBM with DP; because of the regular structure of A, the accesses to P are not expensive. Moreover, the sizes of A and AP
are much larger than $P$. As a result, the accesses to $P$ are not the dominant memory operations in these multiplication operations.

For $R \times A$ multiplications, $A$ has both the largest size, and irregular access patterns because of the structure of $R$. As a result, the accesses to $A$ are the most dominant memory operations. DP significantly benefits from placing $A$ into HBM. In most cases, placing $A$ on HBM alone recovers the performance drop of using DDR as the main area for allocation, and makes it very close to the performance of HBM (or Cache16). However, DP only works when $A$ fits into HBM.

We run the chunking algorithm for KNLs only for $R \times A$ multiplication for 256 threads. We expect a performance improvement only for this case. For other cases, the performances of HBM and DDR are similar, and the data movement cost introduced by chunking further reduces the performance. We run the chunked algorithm where fast memory size is limited to 8GB (as allocations exceeding 11GB led to exhaustion of the memory capacity due to memory fragmentation). For the inputs where $A$ is 8GB, the algorithm copies all of $A$ into HBM and performs the multiplication. The performance of the core multiplication kernel is same as DP; however, the cost of the data movement drops the overall GFLOP/s achieved by 10%. However, for bandwidth bound $R \times A$ multiplications, this copy can still improve the performance w.r.t. DDR (except Elasticity). For larger inputs, the copy overhead only amortizes for those that greatly benefit from HBM. However, when the multiplication performance is similar on HBM and DDR, as in Elasticity, the use of chunking introduces a copy overhead and drops the performance.

In conclusion, DP and chunking benefit SpGEMM on KNLs, where memory systems differ in terms of bandwidth, only when:

1. Accesses to $B$ are irregular (lower temporal locality).
2. A row of $B$ is accessed many times without temporal locality.
3. The density of the rows in $B$ is small (lower spatial locality).

Point (1) holds for $R \times A$ multiplications. However, each column appears around 3 to 4.5 times in these problems, breaking the second condition. Such lower reuse tends to not amortize the copy cost. (3) varies over the matrices, and it is lowest for $R \times A$ of Laplace problem. We get the most benefit in this problem. $A \times P$ has many accesses to $P$ but these accesses show temporal locality.

4.1.2 Triangle Counting

So far, we have exclusively used matrices from multigrid solvers. This was mainly because it allows us to perform weak scaling studies and evaluate two extreme access patterns: regular $A \times P$, highly irregular $R \times A$. In this section, we demonstrate characteristics on the application of SpGEMM when used to perform triangle-counting – a graph analytics problem of interest.

Triangle counting problem is used in many network analysis applications, including social network analysis, spam detection, link recommendation, and dense neighborhood discovery. For these experiments we use three graphs from these applications areas to replicate realistic use cases. These graphs include: (1) twitter-2010, a social network graph; (2) uk-2005, web crawl graph, and, finally, (3) g500s25f16, which is a graph500 scale25 graph. In these experiments, we use an extension of kkmem proposed by Wolf et al. [10] for triangle counting. In this method, the rows are sorted in terms of their degree and a lower triangular matrix is multiplied and masked with itself. The sum of the overall values correspond to the number of triangles in the graph. Wolf et al. uses kkmem with a fused masking operation for this triangle counting. We use the same technique with data placement using kkmem as all matrices fit into HBM.
Figure 9: $A \times P$ Multiplications on KNL.
Figure 10: \( R \times A \) Multiplications on KNL.
Figure 11: Triangle counting times in seconds.
Table 4: Cache miss rates for triangle counting on KNL for 64 threads.

|          | L1-M% | L2-M% |
|----------|-------|-------|
| g500s25f16 | 0.78  | 4.63  |
| twitter   | 0.24  | 16.95 |
| uk-2005   | 0.09  | 18.19 |

In the triangle counting problem we work only on the symbolic structure of matrix - there is no output matrix. Since kkmem performs a symbolic compression of the right hand side matrix, our matrix multiplication kernel simply computes $L \times \text{compressed}(L)$. In DP, we only place compressed $L$ into HBM. In Figure 11, we give the overall runtime of the triangle counting for three matrices in DDR. These times include preprocessing times such as sorting, creation of lower triangular matrices, as well as compression time. However matrix multiplication time dominates (using up to 95% of execution time except uk_2005 which is 30%). In this experiment, all memory modes obtain similar performances on the same number of threads. The triangle counting kernel is also oblivious to the bandwidth characteristics of the underlying memory system. Among these matrices, the kernel scales well using all hyperthreads on twitter and g500s25f16. Table 4 shows the profiled L1 and L2 cache-miss ratios provided by Kokkos [28] Profiling tools. As shown, uk_2005 has the highest percentage of cache misses on L2. The more frequent access to the memory system will drive the problem to become bandwidth bound more quickly which is also the reasoning for the scaling issues seen with 256 threads. In these problems, the right hand side has denser rows, while left hand side has irregular access patterns. As a result, these problems are similar to $R \times A$ multiplication of the Elasticity problem. The performance trends also show similarities where memory system or data placement has minimal effect on the performance. As a result, a chunking method with extra copy cost is not critical and it is likely to reduce the performance in these problems.

4.2 GPU Experiments

In this section we evaluate the performance of the proposed chunking method on GPUs. Figures 12 and 13 follow the same structure as in Figure 6 and 7 and includes the results for two chunking options. Chunk8 and Chunk16 run chunking operations where the fast memory sizes are limited to 8 and 16GBs, respectively.

For problems where $A$ is smaller than 4GB, both Chunk8 and Chunk16 fit whole problems into fast memory. In this case, there is no chunking that is performed. Instead, the whole problem is copied into the fast memory. Multiplication is performed in the fast memory and the result is copied back to the host. In these cases, the multiplication kernel achieves the performance of HBM; however the data movement costs reduce the achieved FLOP/s. We observe at most $5.7 \times$ performance drop w.r.t. HBM performance, yet we achieve as high as $14.7 \times$ speedup w.r.t. host pinned memory runs. UVM obtains better performance than chunking when the problem fits into HBM. Note that in these cases the data is already in GPU, and there is no copy out to host. As a result, UVM should have no data movement costs. UVM performance drops significantly once the problem no longer fits into GPU memory. In this case it is outperformed by the chunking methods.

In $A \times P$ multiplication, $P$ fits into HBM. The Chunk16 method copies the whole $P$ matrix into HBM and streams through the partitions of $A$ and $AP$. It obtains optimal data movement cost. As a result, its GFLOP/s remain constant for each $A \times P$ multiplication as the data size gets larger. Note that there is a performance drop for Chunk8 for 32GB BigStar and Brick matrices as the $P$ no longer fits into HBM space for this portion.

In $R \times A$ multiplication, $A$ is the largest size. Our algorithm tries to fit $R$ and $RA$ into HBM first. Chunk16 achieves optimal copy cost for all instances of Elasticity. The optimal data movement is not satisfied for Laplace, BigStar and Brick matrices for the $A$ with sizes of 16, 16 and 32 GBs, as none
Figure 12: Algorithmic GFLOP/s achieved by HBM, Pinned Memory, and UVM and Chunked Algorithms on $A \times P$ multiplications.

of the matrices fits into bigger portion of the HBM. Still, Chunk16 method achieves $3.10\times$, $5.36\times$ and $13.27\times$ speedups w.r.t. host pinned memory, in the Brick, BigStar and Elasticity, problems respectively.

GPU architectures can support double and triple buffering, i.e., overlapping data movement and computation. When these techniques are used, the available memory is required to be partitioned into multiple discrete segments. While some data is copied to one of the segments, the computation is performed on a separate segment. The Kokkos runtime is currently adding support for this feature. We do not have implementation using these strategies but plan to provide an additional analysis using these capabilities in the near future. However, the performance of Chunk8 on $A \times P$, on most of $R \times A$ multiplication signals high potential performance gains.

In conclusion, memory systems in GPU architectures differ significantly from knls on latency-based overhead. There is big room for improvement, and this is explored by the proposed chunking method. We achieve higher performances when we can fit $B$ or $A$ and $C$ into GPU memory, as the data movement cost is minimized. The performance drops when all matrices have to be partitioned. Yet, we obtain significant speedups w.r.t. UVM and host pinned memory alternatives.

5 Conclusion

Multi-level memory systems have the potential to offer a balance between bandwidth, latency, capacity, cost and power consumption. Already present in a number of supercomputers, multiple-levels of memory are proving to be a complex target for algorithms which require performance but must operate over data structure sizes that exceed the capacity of the highest performing pool of memory in each compute node.
Figure 13: Algorithmic GFLOP/s achieved by HBM, Pinned Memory, and UVM and Chunked Algorithms on $R \times A$ multiplications.
In this paper we have evaluated methods for performing sparse matrix multiplication on two complex multi-level memory-enabled architectures – Intel's Knights Landing processor and NVIDIA's Pascal GPU. We evaluated the performance when placing individual matrices in different memory pools, the use of hardware-based caching modes, and the chunking of matrices into blocks that can be copied to/from the most performant memory in a node for computation. For KNL, the use of hardware cache very often provides performance which is consistent with an HBM-only execution demonstrating the relatively low overhead the hardware provides in this mode. GPUs show a different trend, with chunking methods being essential once data structures exceed the capacity of the HBM memory resource. As we look to the future, the arrival of yet more complex memory subsystems, particularly the potential use of non-volatile memory, will make the computing architecture landscape even more challenging for performant algorithms. Our results suggest that the design of the multi-level-memory algorithms are crucial for memory systems that significantly differ in both latency and bandwidth related metrics. On the other hand, a carefully designed cache-friendly standard algorithm can reduce the need of such methods for the architectures that have memory sub-sytems with similar latencies. In the future, we would like to extend this study to simulate on SST toolkit to simulate on memory subsystems with variable latency and bandwidth overheads.

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