Multimaterial Nanoporous Membranes Shaped through High Aspect-Ratio Sacrificial Silicon Nanostructures

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ABSTRACT: We present an innovative fabrication method for solid-state nanoporous membranes based on the casting of sacrificial silicon nanostructures. The process allows the individual definition of geometry and placement of each nanopore through e-beam lithography and is compatible with a wide range of materials without the need to adapt the process to the materials used. We demonstrate the fabrication of membranes integrating high aspect-ratio nanopores with critical dimensions as small as 30 nm, 1.2 μm in length, with round or elongated shapes, and made of silicon dioxide or amorphous carbon. The capability to engineer nanoporous membranes made of a variety of materials and with tailored designs will lead to new applications in the field of electrochemical sensing, flow modulation, or the chemical functionalization of nanopores.

1. INTRODUCTION

Technological advances in the field of micro- and nanofabrication have recently enabled unique applications based on the peculiar properties of nanofluidics. The ability to modulate relevant nanochannel parameters such as critical dimensions or the span of the electrical double layer has extended the use of nanoporous membranes from passive to active applications such as water-desalination, nanofluidic diodes,1,2 or transistors.3,4 Nanofluidic devices actively controlling the behavior of liquids at the molecular level could lead to breakthroughs in nanomedicine, filtration, energy production, or biochemical analysis.5−7

Although nanofluidics is relevant to many fields of research, its development has been hindered by the lack of reliable and flexible manufacturing techniques enabling engineering of key parameters such as nanopore geometry, surface charge, and materials.8−11

Different methods have been developed to fabricate solid-state nanoporous membranes. The most widespread and commercially successful is the track-etching of membranes, whereby the pores are defined through heavy atom bombardment of polymeric films.12 A new approach to synthesize polymeric membranes through self-assembly of block-copolymers has recently emerged.13 This approach allows the synthesis of large surface membranes with control over the porosity and pore dimension, however it falls short when nonpolymeric materials or more strict pore positioning are desired.14 To extend the choice of materials beyond polymers, the intrinsic properties of aluminum anodization were exploited to define a self-assembled hard mask for the material of interest.14 Although these methods allow the quick fabrication of membranes with controlled porosity and pore size, they rely on stochastic methods and are thus inappropriate when a more rigorous control over single-pore geometry and positioning is required. Methods that independently define the pore shape and placement were developed using focused ion beam (FIB) or electron beam lithography (EBL). FIB-based methods, which independently sculpt every single nanopore of the membrane,15 are widely used for the fine control they offer over nanopore geometry but, due to their serial nature, are time consuming and inappropriate for large scales. EBL followed by deep reactive ion etching (DRIE) is faster and more time efficient than FIB, but the geometries one can obtain are limited by the performance of the DRIE on the membrane material.16 To increase the range of materials and properties at the nanopore−liquid interface, an effort was made to coat nanopores with different materials using techniques ranging from atomic layer deposition17,18 to organic coatings.2 This effectively changes the surface charge of the nanopores or electrically insulates the underlying electrodes. Other techniques rely on the control of intrinsic properties of materials such as NaFon,19 or on the controlled creation of defects to define nanopores.20 Finally, techniques based on sacrificial structures to define the shape of the nanopores were developed using track-etched membranes,21 silicon structures,22 or SiO2 layers23,24 as a template. These approaches can be more laborious than the ones previously cited but are more general and often offer greater flexibility in terms of the design and choice of material. However, even when using sacrificial templates to define the placement and positioning of nanopores, the fabrication method still strongly influences the capability to engineer the membrane. The use of hydrofluoric...
acid to remove SiO₂ templates²³,²⁴ limits the use of metals in the process. Additionally, the use of evaporation to obtain multilayers²² results in pores with conical sections. A manufacturing method allowing the simultaneous definition of a material, and the position and shape of the nanopores is still missing.

We propose here an innovative wafer-scale method based on sacrificial silicon templates to fabricate solid-state nanoporous membranes in a wide range of materials. The presented method defines the geometry of each nanopore by means of a silicon template (Figure 1(1)), which is thereafter used as a sacrificial cast for the desired material for the membrane (Figure 1(2)). The advantage of this rationale is that the placement and geometry of each nanopore is independent of the materials used to cast the membrane and thus relies only on the micromachining of the silicon templates by EBL followed by DRIE, which are reliable processes, well controlled, and uniform at the wafer scale.²⁵ Once the material comprising the membrane is conformally molded on the templates, the whole surface is planarized until the silicon template forms the desired surface from the surrounding material using a process that combines chemical mechanical polishing (CMP) and ion beam etching (IBE) (Figure 1(3)). The selective removal of the silicon template with a combination of consecutive KOH and XeF₂ etches (Figure 1(4)) at the end of the process reveals the nanopore, whose shape is the exact negative of the silicon template (Figure 1(5)).

The advantages of the presented strategy compared to other fabrication methods are numerous. The use of a combination of EBL and DRIE to define the shape of the silicon structures allows control of the placement and geometry of every single pore by design, independent from other nanopores and from the material used for the membrane. Free-shaped, nonround, conic or high aspect-ratio nanopores can thus be easily manufactured in a reliable manner.

The use of conformal deposition methods to deposit the material comprising the membrane has several implications. First, it allows the deposition of a wide range of materials and with different technologies, from sputtering to different variants of chemical vapor deposition (CVD), as long as the material is deposited adherent to the template. Second, the possibility to stack different layers on top of each other to constitute the membrane enables fine engineering of the membrane mechanical and interfacial properties. This concept is illustrated in Figure 1, where a stack of two materials (blue and yellow) is used to form the membrane. The underlying material (blue) is deposited first and then covered with a second material (yellow). At the end of the process, the blue layer dictates the solid–liquid interface behavior of the nanopore whereas the yellow material does not contribute to the nanofluidic properties of the device but provides the desired mechanical properties for the structure. This enables the use of materials for the nanopore–electrolyte interface that are usually not suitable for monolithic membranes due to cost, mechanical properties, or quality of deposition. The proposed method relies on a cleanroom process, which is widespread, reliable, well controlled, quick, and uniform at the wafer scale (unlike, e.g., FIB). The process is easily integrable within a more complex process flow (e.g., for microfluidic channel fabrication) and enables the integration of multiple membranes with different properties and geometries within the same device. As a proof-of-concept, we present here a passive nanoporous membrane made of a thin layer of hydrogenated amorphous carbon–nitrogen (a-C:N:H)²⁶ as the interface material and SiO₂ as the structural material, embedding nanopores with critical dimensions from 30 to 70 nm, 1.2 μm long, with round and elongated geometries. a-C:N:H can be easily deposited through CVD and has a wide polarizable window;²⁷ it is therefore an ideal candidate for a nanopore–liquid interface.

Figure 1. Graphical representation of the process flow. First, the sacrificial templates are obtained in bulk silicon (1). Second, the interfacial (blue) and the passive material (yellow) are deposited frontside (2). After planarization combining CMP and IBE methods (3), the membrane is released (4) through timed KOH etching followed by XeF₂ etching. The final result (5) is a suspended membrane whose nanopores at the electrolyte-nanopore interface are made of the “interface material” (blue) and whose shape and positioning are defined through e-beam lithography.
material in gating applications. SiO$_2$, on the other hand, is inert, electrically insulating, and mechanically robust which justifies its choice as the structural material.

2. RESULTS

2.1. Template Definition. Arrays of silicon nanostructures were defined through EBL using hydrogen silsesquioxane (HSQ) as the resist and carved in the bulk of a silicon wafer using a continuous DRIE process based on SF$_6$ and C$_4$F$_8$. The nanostructures were fabricated with two different geometries (round and wavy), three different etching times (4, 6, and 8 min), and with a pitch of 1 or 3 μm (Figure 2a,b). For an etch process of 4 min, round silicon structures (nanopillars) with diameters down to 40 and 1220 nm tall were fabricated with HSQ masks of 50 nm in diameter. Structures 1690 nm tall (6 min etch) showed an increase in the minimal diameter that could be successfully fabricated to 49 nm, and structures 2260 nm tall (8 min etch) were obtained with minimal diameters of 70 nm. The maximal aspect-ratio for the columnar structures was 30−34 regardless of height (Figure 2c). Etching times higher than 8 min were not investigated as all of the 130 nm of HSQ used as a mask was consumed at this point, resulting in a selectivity of the etch process of about 17, silicon to HSQ.

As previously described, the shape of the template can influence the stability of the silicon structure, and thus the minimal critical dimension attained. Wavy linear structures (nanofins) were fabricated and critical dimensions of 30 nm were consistently obtained, independently from the height of the structure and etching times.

2.2. Influence of Etching. The DRIE process used to carve the silicon nanostructures can be tuned to control the shape of the nanopores. The quantity of passivator (C$_4$F$_8$) and etchant (SF$_6$) gasses used during the etching step determines the verticality of the walls of the template. An excess of SF$_6$ results in structures with a tip wider than the base (underetch), whereas a greater quantity of passivator results in structures where the base is wider than the tip because of the accumulation of C$_4$F$_8$ on the wafer. Furthermore, the density of the patterns influences the optimal ratio of SF$_6$/C$_4$F$_8$ similar to a “load effect”: the denser the pattern, the higher the area to passivate, the higher the flow of C$_4$F$_8$ needed for optimal results. Two guidelines can be given based on such considerations: first, the mentioned “load effect” creates a trade-off between uniformity of the structures and local variation of template density. Second, by tailoring the SF$_6$/C$_4$F$_8$ ratio, conical sacrificial structures (and therefore conical pores) can be easily obtained. In our case, the etching process was optimized for columnar structures of 50 nm. The same etching recipe is suboptimal for structures with a slightly greater surface, such as nanofins, which were therefore produced with a base slightly wider than the tip.

2.3. Impact of Conformal Deposition Process. The aforementioned silicon nanostructures were then coated with 250 nm of a-C: N: H and 2 μm of SiO$_2$, corresponding to the blue and yellow regions, respectively, in Figures 1 and 3. The process used to deposit SiO$_2$ is not perfectly conformal, and therefore voids were created between nanostructures whose pitch was not greater than the height of the structures. This is a well known and characterized process, which has even been exploited to fabricate nanochannels. In our case, given the high aspect-ratio of the structures, the relationship between the desired thickness of a membrane and the minimal distance between pores (pitch) needs to be considered when designing the membrane. Membranes with templates too closely packed together will result in small bumps around the pores and a thinned membrane, whereas a membrane with templates sufficiently spaced from each other will not suffer from these limitations. In Figure 3, an array is shown with 1 μm tall structures either spaced 1 μm (left) or 3 μm (right) apart. The FIB cross-sections at the top show how the void is a direct consequence of the deposition method and pitch between nanostructures. The SEM micrographs at the bottom show the effect of the presence of voids on the structure of the membrane after planarization. Such voids are not present when the pitch is greater than twice the height of the nanostructures, thus the membrane is flat as shown in Figure 3b,d.
2.4. Planarization Characterization. The process of uncovering the buried silicon nanostructures through planarization and thinning of the membrane material is of utmost importance, as the thickness and surface quality of the membrane depends on it. CMP is the reference process for planarization and thinning of thin films but suffers from some important drawbacks: it is difficult to obtain a uniform etch rate at the wafer scale and the whole process is strongly material-dependent which means that the results on heterogeneous structures would have to be optimized for every material combination. IBE does not suffer from those problems because it is not a material-dependent process and has a uniform etch rate at the entire wafer scale. However, IBE is not suitable for planarization as its nature tends to preserve the surface topography of the wafer rather than planarize it. The strategy we adopted efficiently combines CMP and IBE to take advantage of both techniques. First, a uniform flat surface is obtained with a short CMP step (∼1 min) that levels the wafer without significantly affecting the native uniformity of the film. Then, IBE is used to uniformly etch the entire frontside of the wafer until the buried silicon nanostructure surface is obtained from the surrounding material (Figure 4a). To prevent prematurely reaching the underlying a-C:N:H layer or the silicon structures early during the CMP step, about 1 μm of SiO2 in excess was deposed. This way, the CMP process will only “see” the SiO2 layer on top, independent of the material underneath.

To investigate in more detail, a suboptimal CMP processing of SiO2 was characterized on three different wafers for three different etch times (1, 2, and 3 min). The thickness and uniformity of the SiO2 film was measured before and after CMP at 25 points with an interferometer to evaluate the rate and uniformity of the process. Although the etch rate can be considered constant (350 nm min⁻¹, not shown), the uniformity of the film decreases with CMP time. It is clear from Figure 4b-left how, after 1 min of CMP, the nonuniformity of the SiO2 film, represented by the standard deviation of the thickness of the SiO2 layer over the entire wafer surface, increases with etch time. The same wafers were then processed with IBE for three different times (4, 6, and 8 min) to characterize the etch rate and uniformity of the process. Figure 4b-right shows how the measured standard deviation remains unchanged before and after IBE etching, and this is independent from the etch time. Furthermore, the measured IBE etch rates are extremely reproducible and were measured to be (80 ± 3) nm min⁻¹.

The precision and control provided by this technique were consistently used to level and thin SiO2 films with a precision of ±10 nm, independent of the combination of materials used and without having to adapt the CMP or IBE parameters.

2.5. Membrane Release and Final Results. By combining the controlled nanostructure fabrication and the planarization method previously mentioned, arrays of silicon
templates embedded in a-C:N:H and SiO₂ were fabricated. The fabricated array had 441 template nanostructures deposited in a hexagonal lattice and spaced 1 and 3 μm apart. The structures did not show defects and had uniform thickness and template geometry along the entire array (Figure 5a). Figure 5b,c shows further magnification of the nanopillar and wavy nanofin silicon templates embedded in a-C:N:H and SiO₂. As shown in Figure 5b, the 40 nm silicon template is clearly distinguishable as a brighter spot in the middle of the image. The amorphous carbon layer surrounding the template is slightly set back in the SiO₂ film because of its minimally different etch rate during the IBE process. Wavy template nanofins with critical dimensions of 30 nm, shown in Figure 5c, were successfully processed without any modifications of the fabrication process used for the template nanopillars. No differences in terms of uniformity or stability of the process were observed compared to that for the columnar templates or depending on the different material combinations tested.

Following a partial backside KOH etch, the silicon template nanostructures were removed through XeF₂ etching, revealing nanopores whose shape corresponds to the negative of the silicon nanostructures (Figure 5d,e).

The XeF₂ etch has a key role in the fabrication process. XeF₂ gas etching is known to selectively affect only silicon, silicon nitride, tungsten, and titanium, the etch rate for other materials being null.30,31 This high selectivity allows a wide spectrum of materials to be used in the process without having to adapt the release of the nanopores to the material used and without compromising the final geometry of the nanopore. Furthermore, XeF₂ etching of silicon, being purely chemical (without the physical ion bombardment characteristic of plasma etching), guarantees not to damage either the nanopore walls or the membrane surface.

2.6. Functional Test. To verify the functionality and integrity of the membrane, its transmembrane electrical resistance was measured and compared to that from theoretical predictions. The chip was placed between two reservoirs filled with 1 M KCl (Figure 6a), and the current flowing across the membrane was measured as a function of the transmembrane voltage with a potentiostat (Figure 6b). To calculate the resistance of the membrane, we neglected any nanofluidic effects as the high electrolyte concentration resulted in no overlap of the electrical double layer, therefore the theoretical resistance of the system was dictated purely by geometrical parameters Table 1. The total resistance of the system is the sum of the geometrical resistance of the membrane $R_{\text{mem}}$, the access resistance for each pore on both sides of the membrane $R_{\text{acc}}$, and the KOH pyramid resistance $R_{\text{KOH}}$. The bulk resistance $R_{\text{bulk}}$ and the electrode–electrolyte interface resistance were neglected. The geometrical resistance for a membrane with $n$ pores of diameter $2r$ and length $h$ is defined as

$$R_{\text{mem}} = \rho_{\text{KCl}} \frac{h}{n A_{\text{pore}}} = \rho_{\text{KCl}} \frac{h}{nr^2}$$

(1)

where $\rho_{\text{KCl}}$ is the resistivity of 1 M KCl. The access resistances were estimated using the formula32

$$R_{\text{acc}} = \rho_{\text{KCl}} \frac{1}{n 4r}$$

(2)

and the KOH pyramid resistance was calculated as...
The total electrical resistance of the membrane is therefore achievable with the presented fabrication strategy. 

demonstrates the high control over the geometrical parameters integrity of the membrane and an absence of any leakages. This good agreement with theoretical data, we can assume the currents greater than expected and, as the measurements are in side of the KOH pyramid, and

\[ R_{\text{mem}} = \int_0^t \frac{dx}{(d + \frac{x(D-d)}{2t})} \]

where \( d \) and \( D \) are, respectively, the size of the small and large side of the KOH pyramid, and \( t \) is the thickness of the wafer. The total electrical resistance of the membrane is therefore

\[ R_{\text{tot}} = R_{\text{KOH}} + R_{\text{mem}} + 2R_{\text{acc}} \]  

A fracture, leakage, or defect in the membrane would result in currents greater than expected and, as the measurements are in good agreement with theoretical data, we can assume the integrity of the membrane and an absence of any leakages. This demonstrates the high control over the geometrical parameters achievable with the presented fabrication strategy.

3. DISCUSSION

3.1. Considerations of Pore Geometry. The ability to control the pore geometry is important for many applications involving nanoporous membranes.

In applications such as nanofluidic transistors or diodes, the critical dimension of the nanochannel has to be smaller than twice the Debye length for the electric double layer (EDL) overlap to occur.\(^{33-35}\)

By controlling the geometry of the nanopore, it will be possible to fabricate membranes capable of discriminating between specific molecules or particles. Experiments have shown that by engineering longitudinal irregularities inside nanopores, the shape and volume of translocating objects can be deduced.\(^{36}\) Such nanopores can be fabricated by slightly modifying the fabrication process previously presented using an alternating Bosch-process to fabricate corrugated templates. This would result in nanopores with corrugations where the roughness of the structure is defined by the scalloping effect.\(^{37}\)

The same nanopores with controlled corrugation but made of hydrophobic materials could be used to produce membranes with extremely low hydrodynamic resistance, which may be particularly efficient in the study of streaming currents.

Finally, the presented method allows the controlled fabrication of high aspect-ratio nanopores regardless of the materials used, which is impossible to imitate with other manufacturing techniques. This opens up interesting perspectives for electro-osmotic control of flows where effects of back-pressure flows will be mitigated by the higher hydrodynamic resistance of high aspect-ratio nanochannels.

3.2. Discussion on Materials. Membranes made of a-C:N:H–SiO\(_2\) and purely SiO\(_2\) were successfully fabricated with the very same process and showed the same quality in terms of pore geometry and yield. The possibility to change and stack materials as desired without the need to adapt the fabrication process, and the variety of materials that can be used by this process have many implications.

The compromise between interface properties and mechanical stability of a membrane often necessary for monolithic membranes can be easily avoided. The function of mechanically supporting the membrane is entrusted to the passive material (in our case SiO\(_2\)) whereas the interface properties of the nanopore can be optimally chosen for the desired application (a-C:N:H in our case) as long as it can withstand XeF\(_2\). This results in a wide choice of materials as most materials, including oxides, metals, and organic compounds are not at all or weakly attacked by XeF\(_2\). Therefore, nanopores made of exotic or expensive materials can be fabricated with thicknesses that would not be possible with other techniques for the sake of mechanical stability, material-stress, or cost. Additionally to a-C:N:H–SiO\(_2\) and monolithic SiO\(_2\), we explored the use of other materials. A membrane with 200 nm of platinum (Pt) at the nanopore–electrolyte interface and SiO\(_2\) as the structural material was fabricated using the same process as that for the a-C:N:H–SiO\(_2\) and SiO\(_2\) membranes.

Furthermore, the number of combined materials is not limited to two. Additional layers can be integrated in the stack that, once planarized, could behave as functional electrodes directly integrated in the membrane.

This flexibility in the choice of materials opens up new opportunities for easy functionalization of nanopores as the most appropriate membrane-material/surface-chemistry couple can be chosen.\(^ {11}\) Simulations have shown that grafting charged

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Table 1. Numerical Values of Parameters Used in Equations 1 to 4

| variable | value | variable | value |
|----------|-------|----------|-------|
| \( n \) | 441 | \( r \) | \( 20 \times 10^{-6} \) m |
| \( h \) | \( 630 \times 10^{-6} \) m | \( \rho_{\text{KCl}} \) | 11.88 S m\(^{-1}\) |
| \( d \) | \( 60 \times 10^{-6} \) m | \( D \) | \( 600 \times 10^{-6} \) m |
| \( t \) | \( 380 \times 10^{-6} \) m | \( R_{\text{mem}} \) | 95.69 \( \times 10^3 \) Ω |
| \( R_{\text{KOH}} \) | 1.61 \( \times 10^3 \) Ω | \( R_{\text{acc}} \) | 2.38 \( \times 10^3 \) Ω |
| \( R_{\text{tot}} \) | 102.08 \( \times 10^3 \) Ω |
polymers inside nanopores dramatically impacts the potential distribution inside nanochannels,38 and that nanopores functionalized with poly(ethylene glycol) (PEG) may prevent fouling in an efficient way.39 For example, high aspect-ratio gold nanopores, easily functionalizable with thiol-terminated molecules, can be fabricated in a reliable and cost efficient way with the presented method by stacking a thin layer of gold and chrome (for adhesion) and a thick layer of SiO2 as the structural support.

One other promising class of materials to investigate are polarizable materials such as boron-doped diamond, diamond-like carbon or a-C:N:H.27,40−42 Nanopores made of polarizable materials at the nanopore-electrolyte interface are suitable for gating applications as they enable a potential to be applied at an interface without leakage currents. In this way, it is possible to directly modulate the magnitude and polarity of the surface field damping.3,43,44

4. CONCLUSIONS

We demonstrated a new strategy for the manufacturing of solid-state nanoporous membranes with pore geometry, positioning, and thickness independently defined from each other. The method relies on the use of sacrificial silicon nanostructures as templates to cast the nanopores, thus being compatible with a wide range of materials. Critical aspects and limitations of the process include an attainable maximal aspect-ratio of 35, the relation with the template shape and its stability, and the necessary trade-off between porosity and membrane thickness. Arrays of nanopores were obtained with the same procedure and without observable defects with critical dimensions as little as 30 nm and 1.2 μm long, made of monolithic SiO2 and a combination of a-C:N:H and SiO2. The functionality and integrity of the fabricated membranes as well as the high control provided over the geometrical parameters were proven through SEM inspection and transmembrane resistivity measurements. Manufacturable alternatives of nanopore geometries and potential new materials possible due to the presented method leading to innovative applications of nanofluidic membranes were discussed. The presented fabrication strategy provides a new tool to fabricate nanoporous membranes at the wafer scale with simultaneous control over nanopore shape, material, and placement. The freedom in tailoring the membrane characteristics to the desired application will open new perspectives in the field of functional materials and active control of molecules inside nanopores.11

5. EXPERIMENTAL SECTION

5.1. Sacrificial Silicon Template Fabrication. The nanopore geometries were defined with frontside e-beam lithography on a double side polished silicon wafer (Figure 1(1)), covered by a thin film of 120 nm of Si3N4 on the backside only to be used as a hard mask for a KOH etching step later in the process. On the frontside, 140 nm of 6% HSQ was used as a negative tone e-beam resist (Dow Corning, XR-1541-006). The patterns were then transferred in the bulk silicon through DRIE specifically optimized28 to obtain the sacrificial structures used as the template. The resulting structures had critical dimensions down to 30 nm for heights up to 2.7 μm. The details of this fabrication step are presented in a previous publication.22

5.2. Membrane Deposition. The material comprising the membrane-electrolyte interface, the membrane material, and the material physically supporting the membrane, the support material, were then conformally deposited on top of the templates (in blue and yellow, respectively, in Figure 1(2)). The membrane material was 250 nm of a-C:N:H deposited through CVD (Oxford PlasmaLab 100, 50 W of RF generator power, 800 mTorr deposition chamber pressure at a temperature of 45 °C for 40 min).26 As the support material, 2 μm of SiO2 was deposited through CVD (Oxford PlasmaLab 100, 20 W of RF generator power, 1500 mTorr deposition chamber pressure at a temperature of 300 °C for 40 min).

5.3. Planarization. The deposited materials were then planarized using a combination of CMP and IBE (Figure 1(3)). A short CMP step (ωhead = 65 rpm, ωplate = 75 rpm, head pressure = 0.76 bar, polishing time = 1 min, backside pressure = 0.76 bar, slurry 30N50 from KLEBOSOL, on a pad IC 1000 from DOW with a specific gravity of 0.794) was used to level the wafer and remove the excess material over the templates. Once the surface was leveled, IBE (Veeco NEXUS IBE350, 600 W, at an incidence angle of 60 °C) was used to uniformly erode the support material until the buried silicon template surfaced.

5.4. Membrane Release. To release the membranes, a combination of KOH and XeF2 etching was used (Figure 1(4)). First, the Si3N4 backside layer was structured as the hard mask using a standard photolithography processes (2 μm of AZ9260 as photoresist) followed by He/CHF3-based DRIE to expose the silicon underneath. The wafer was then etched in KOH (40% at 60 °C for about 19 h) using a waterproof teflon chuck to protect the frontside until only a few microns of silicon were left. At this point, the wafer was diced and stored in this state until needed. Just before use, to completely release the membranes from the last microns of silicon and remove the sacrificial nanostructures, the chips were etched with pulsed XeF2 gas (50 × 30 s at 2700 mbar).

5.5. Resistivity Measurements. The membrane test chip had 441 circular nanopores of 40 nm in diameter and 630 nm in length. The chip was placed between two separate reservoirs each containing 850 mL of 1 M KCl (Figure 6a). A voltage was then applied across the membrane with two Ag/AgCl electrodes fabricated by anodization of a silver wire in 0.1 M HCl and equilibrated overnight in a solution of 1 M KCl.

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