A Linearity Improvement Front End with Subharmonic Current Commutating Passive Mixer for 2.4 GHz Direct Conversion Receiver in 0.13 µm CMOS Technology

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Abstract: Direct conversion receiver (DCR) architecture is a promising candidate in the radio frequency (RF) front end because of its low power consumption, low cost and ease of integration. However, flicker noise and direct current (DC) offset are large issues. Owing to the local oscillator (LO) frequency, which is half of the RF frequency, and the absence of a DC bias current that introduces no flicker noise, the subharmonic passive mixer (SHPM) core topology front end overcomes the shortcoming effectively. When more and more receivers (RX) and transmitters (TX) are integrated into one chip, the linearity of the receiver front end becomes a very important performer that handles the TX and RX feedthrough. Another reason for the requirement of good linearity is the massive electromagnetic interference that exists in the atmosphere. This paper presents a linearity-improved RF front end with a feedforward body bias (FBB) subharmonic mixer core topology that satisfies modern RF front end demands. A novel complementary derivative superposition (DS) method is presented in low noise amplifier (LNA) design to cancel both the third- and second-order nonlinearities. To the best knowledge of the authors, this is the first time FBB technology is used in the SHPM core to improve linearity. A Volterra series is introduced to provide an analytical formula for the FBB of the SHPM core. The design was fabricated in a 0.13 µm complementary metal oxide semiconductor (CMOS) process with a chip area of 750 µm × 1270 µm. At a 2.4 GHz working frequency, the measurement result shows a conversion gain of 36 dB, double side band (DSB) noise figure (NF) of 6.8 dB, third-order intermodulation intercept point (IIP3) of 2 dBm, LO–RF isolation of 90 dB and 0.8 mW DC offset with 14.4 mW power consumption at 1.2 V supply voltage. These results exhibit better LO–RF feedthrough and DC offset, good gain and NF, moderate IIP3 and the highest figure of merit compared to the state-of-the-art publications.

Keywords: complementary DS; SHPM; FBB; quadrature LO generation

1. Introduction

Today, portable electronic devices with less power consumption are urgently required. Therefore, integrated circuit (IC) designers have drawn much attention to direct-conversion transceiver architectures because of their low cost, low power and ease of integration. To implement a direct-conversion receiver successfully, frequency-conversion circuits should be carefully designed.
because the DC offset and flicker noise generated by a down mixer could significantly corrupt the output signal-to-noise ratio (SNR) in the receiver path and the large leakage of the local oscillator (LO) to radio RF port could severely degrade the linearity of the system [1,2]. The subharmonic RF front end, in which the LO frequency is half the RF frequency, overcomes the DC offset effectively because the RF signal mixes with the LO signal, which feeds through into the RF port that is out of band [3–8]. The absence of a DC current in the current commutating passive mixer has no 1/f noise [9,10]. Hence, the subharmonic passive current-driven mixer topology is suitable for the direct conversion receiver. The crowded RF band and monolithic integration of the transceiver have required designers to increasingly focus on linearity [11,12]; however, the linearity of subharmonic mixer topology has not been discussed much. In Reference [13], a 25% duty cycle LO switching is implemented to improve the second-order intermodulation intercept point (IIP2) of the subharmonic mixer (SHM). References [14,15] used the second-order intermodulation (IM2) current injection method to improve the active SHM linearity, but the flicker noise was higher than the passive SHM. The authors of [5] used a common gate (CG)–common source (CS) LNA with a positive- or negative-feedback technique to improve LNA linearity, but they did not include a mixer core. A resistively degenerated method is introduced for the passive current driving mixer architecture to improve NF and linearity [16].

To implement a high linearity RF front end with current driving passive SHM, some linearity improvement methods have been introduced. For LNA, the complementary derivative superposition (DS) method is used to improve IIP3. With more mixer core cascades than a conventional current driving passive mixer, the on-resistance of SHM is more sensitive to the front end. The feedforward body bias (FBB) is applied to reduce the on-resistance and can improve linearity. The quadrature square-like LO is needed for one channel of SHM. The polyphase filter and LO buffer are carefully designed and deeply discussed in this paper. The 2.4-GHz subharmonic RF front end is implemented in a 0.13-μm CMOS process.

2. Circuit Design

2.1. Proposed LNA Design

The circuit’s block diagram is shown in Figure 1, where TIA is a transimpedance amplifier and PPF is a polyphase filter. The differential RF and LO inputs are obtained by an off-chip balun. The first stage of the circuit is a cascoded inductively degenerated common source (IDCS) LNA with an improvement in linearity. The cascode structure provides better reverse isolation than a common-source structure, avoiding the large LO leakage back into the RF input.

Figure 1. Block diagram of the proposed circuit.
For the cascoded IDSC LNA, the degeneration inductor is transformed at the input to create a resistive portion to the input impedance. With proper selection of $g_m, C_{gs}$ and $I_{ds}$, the input of the amplifier can be matched to $R_i$ for maximum power transfer. With degeneration, the second-order tones generated from the second-order nonlinearities are fed back to mix with the fundamental tones at the input, creating third-order tones. Hence, the third-order intermodulation (IM3) with feedback consists of two contributions: one from the third-order nonlinearity of the transistor and the other from the second-order nonlinearity. The authors of [17] used an IM3 sinker to improve the linearity of LNA, but they did not consider the feedback of second-order tones. The authors of [18] introduced a modified superposition method for linearizing LNA. In the LNA proposed this paper, as illustrated in Figure 2a, positive metal oxide semiconductor (PMOS) ($M_5$ and $M_6$) and negative metal oxide semiconductor (NMOSaux ) ($M_3$ and $M_4$) were introduced to eliminate the second- and third-order distortions. $M_1$ and $M_2$ were biased to the strong inversion state for high conversion gain. The inputs of PMOS $M_5$ and $M_6$ were cross-connected with the inputs of $M_1$ and $M_2$ and were also biased to the strong inversion state, while $M_3$ and $M_4$ were biased to the weak inversion state.

![Figure 2](image_url)

**Figure 2.** Schematic diagram of the proposed: (a) LNA (low noise amplifier); and (b) current flow of the left half-circuit.

According to Kirchhoff’s current law, as depicted in Figure 2b:

$$i_{s7} = i_{d3} + i_{d1} - i_{d5} \quad (1)$$

In general, the drain current $i_{ds}$ of an MOS transistor can be expressed as:

$$i_{ds} = I_{DS} + g_m v_{gs} + \frac{1}{2!} g_{m2} v_{gs}^2 + \frac{1}{3!} g_{m3} v_{gs}^3 + \ldots \quad (2)$$

By substituting Equation (1) into Equation (2), we can get:

$$i_{s7} = (g_{1m1} + g_{5m1} + g_{3m1}) v_{in} + \frac{1}{2!} (g_{1m2} - g_{5m2} + g_{3m2}) v_{in}^2 + \frac{1}{3!} (g_{1m3} + g_{5m3} + g_{3m3}) v_{in}^3 \quad (3)$$

By carefully designing the sizes of $M_1$, $M_3$ and $M_5$, as well as the bias voltage, we get:

$$g_{1m2} + g_{3m2} = g_{5m2}, g_{1m3} + g_{5m3} + g_{3m3} = - g_{3m3} \quad (4)$$

The second- and third-order nonlinearities of the main NMOS are eliminated simultaneously, as shown in Figure 3; thus, the linearity is notably improved.
Referring to the notation in [18], the third-order intermodulation distortion (IMD3) of the drain current of a traditional IDCS LNA is proportional to:

\[ IIP3 = \frac{4g_2^2\omega^2LC_{gs}}{3|\varepsilon|} \]  

(5)

\[ \varepsilon = g_3 - \frac{2g_2^2/3}{g_1 + \frac{1}{j\omega L_e} + j2\omega C_{gs} + Z_1(2\omega)C_{gs} L_e} \]  

(6)

In this paper, \( g_3 = g_{1m3} + g_{5m3} + g_{3m3} \) and \( g_2 = g_{1m2} - g_{5m2} + g_{3m2} \). Figure 4a,b shows the improvement in linearity of the LNA with PMOS and NMOSaux.

Figure 5a,b displays the simulation results of the cascoded IDCS LNA and the proposed IDCS LNA, respectively. The IIP3 of the proposed IDCS LNA was improved by 13 dB, compared to that of the former’s 4-dB gain drop, with a 4-mW increase in power consumption and a deterioration in NF of 0.4 dB. Finally, the proposed IDCS LNA achieved an NF of 1.9 dB, a gain of 16.8 dB, an IIP3 of 9.3 dBm and a power consumption of 10 mW.
Thus, this circuit can be regarded as a passive mixer with square-wave switching at twice the LO frequency. Therefore, a high Q LC parallel circuit is not good for LNA gain but is necessary for the performance of the mixer core, thus the analysis of the mixer core cannot be done separately. Because of the influence of the current, the output impedance of the LNA and the mixer core should be as high as possible, while the input impedance of the mixer core and the TIA should be as low as possible.

2.2. Current Commutating Subharmonic Passive Mixer Design

The second stage of the circuit is a current commutating subharmonic passive mixer (Figure 6a), in which the bias circuit is not given. Transistors $M_1$–$M_4$ form the first stage, which is a regular double-balanced passive mixer, while transistors $M_5$–$M_8$ form the second stage to achieve subharmonic mixing. In every quarter-cycle, two of the first- and second-stage transistors are turned on, modulating the current to the intermediate frequency (IF) port. It can be observed that, in one complete cycle of the LO, the current from LNA is commutated four times, and, hence, at twice the LO frequency. Thus, this circuit can be regarded as a passive mixer with square-wave switching at twice the LO frequency, as illustrated in Figure 6b [19].

Because the passive mixers exhibit intrinsic bidirectionality, the TIA amplifier and LNA co-influence the performance of the mixer core, thus the analysis of the mixer core cannot be done separately. Because of the influence of the current, the output impedance of the LNA and the mixer core should be as high as possible, while the input impedance of the mixer core and the TIA should be as low as possible. Therefore, a high Q LC parallel circuit is not good for LNA gain but is necessary for
enhancing the performance of the mixer core. Figure 7a is the equivalent circuit of the front end. For simplicity, we only consider half of Figure 7a, and this circuit is simplified as Figure 7b, where \( R_{sw} \) is the on-resistance of MOS switch. For the ideal switch consideration, we express it on the Fourier series, where \( a_n \) is the \( n \)th Fourier coefficient. The derivation formula of the input impedance is given in [9]; in this paper, the input impedance was changed to (9), twice the on-resistance of the double-balanced mixer (DBM).

\[
\begin{align*}
S_1(t) &= \sum_{n=-\infty}^{\infty} a_n \exp(jn2\omega_{LO}t) \quad (7) \\
S_2(t) &= \sum_{n=-\infty}^{\infty} (-1)^n a_n \exp(jn2\omega_{LO}t) \\
Z_{in} &\approx 8r_{sw} + 8a_1^2[Z_{BB}(\omega - 2\omega_{LO}) + Z_{BB}(\omega + 2\omega_{LO})] \quad (9) \\
R_{mix_{out}} &= \frac{1}{4C_{par} \times 2f_{LO}} \quad (10)
\end{align*}
\]

The value of the output impedance of the mixer core decreases because of a more cascaded MOS switch than the conventional DBM, as shown in (10), where \( C_{par} \) is the parasitic capacitance of the mixer core. A small \( R_{mix_{out}} \) has negative effects on the noise of the TIA. Of course, the big size of the mixer core introduces large capacitance, which leads to a finite rise and fall time of the LO. Furthermore, NF and linearity also worsen [10,20,21]. Hence, the size of the mixer core should be set carefully under both noise and gain considerations. The bias voltage \( V_{G} \) of the mixer core is another important parameter for the performance of the mixer core. \( V_{G} \) should be set a bit higher to ensure that the mixer core works in the on-overlap state [10].

**Figure 7.** Equivalent circuit of: (a) the front end; and (b) the simplified equivalent circuit. LO, local oscillator.

### 2.3. FBB for Enhancing the Performance of the Mixer Core

As mentioned above, the on-resistance of the mixer core should be as small as possible, which means that a large-sized MOS is needed, leading to an increase in the parasitic capacitance. In SHM, its on-resistance is double that of the DBM, thus the size of the mixer core should be more sensitive than that of the DBM in terms of front end performance. The on-resistance of NMOS is equal to:

\[
R_{SW} = \frac{1}{\mu_c C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \quad (11)
\]
where \( V_{TH} = V_{TH0} + \gamma \left( \sqrt{2|\phi_F + V_{SB}|} - \sqrt{2|\phi_F|} \right) \); if \( V_{SB} < 0 \), \( V_{TH} \) decreases and then \( R_{SW} \) decreases.

In this paper, the FBB voltage is used in the mixer core to reduce the on-resistance. As shown in Figure 8a, the on-resistance of MOS reduces when using the FBB voltage. For example, the blue line shows a 58% decrease in \( R_{SW} \) from 31 \( \Omega \) to 20 \( \Omega \), with \( W = 50 \mu m \) and \( V_{DS} = 0.15 \) V at \( V_B = 0.6 \) V and 0 V. Figure 8b shows the output impedance of the SHM core; the small size of the MOS means that large output impedance is expected in the front end. Therefore, a small-sized mixer core with FBB is chosen in this paper, and a deep N-well process is needed. The authors of [22] stated that the deep N-well implantation MOS does not impact the DC, AC, RF and noise performance of the multi-fingered transistor, hence allowing model consistency with the standard-well multi-fingered transistor.

The process of simplification of the circuits is shown in [20], assuming that the load is a pure resistance \( R_L \). The circuit is illustrated in Figure 9a, b for the calculation of a Volterra core, where \( g_{SW} \) is the conductance of the mixer core and \( i_{NL2} \) and \( i_{NL3} \) are the second and third nonlinear sources, respectively.

\[
g_{SW} = \left\{ \begin{array}{ll}
\mu_n C_{ox} W (V_{LO} + V_{GS} - V_{TH}) |_{\text{switch = on}} \\
0 |_{\text{switch = off}}
\end{array} \right.
\]  

Figure 8. (a) The on-resistance of MOS; and (b) the output impedance of the subharmonic mixer (SHM) core.

Figure 9. (a) Equivalent circuit of the proposed mixer; and (b) the nonlinearity source.

For nonlinearity analysis, the source and drain voltages can be expressed as a converging Volterra series of input current, as shown in Figure 9a, b. Thus,

\[
v_S = H_{1s} i_m + H_{2s} i_m i_m + H_{3s} i_m i_m i_m + \ldots
\]  

where \( \gamma \) is the conductance of the mixer core and \( i_{NL2} \) and \( i_{NL3} \) are the second and third nonlinear sources, respectively.
where \( H_{ns} \) and \( H_{nd} \) are the \( nth \)-order Volterra kernels for the source and drain ports, respectively [20].

The nonlinear current source is a function of the first-order Volterra kernels [23], which is given by (17), ignoring the cross derivative.

\[
i_{NL2} = \frac{1}{(g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L})^2} \left[ K_{2g_{ns}}(g_{sw} + g_{L})^2 + K_{2g_{nd}}g_{sw}^2 \right]
\]

(17)

The second-order Volterra kernels are [20]:

\[
H_{2s} = \frac{g_{L}}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}} i_{NL2} = \frac{g_{L} \left[ K_{2g_{ns}}(g_{sw} + g_{L})^2 + K_{2g_{nd}}g_{sw}^2 \right]}{(g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L})^3}
\]

(18)

\[
H_{2d} = -\frac{2}{\pi} \frac{g_{S}}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}} i_{NL2} = -\frac{2}{\pi} \frac{g_{S} \left[ K_{2g_{ns}}(g_{sw} + g_{L})^2 + K_{2g_{nd}}g_{sw}^2 \right]}{(g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L})^3}
\]

(19)

\[
i_{NL3} = \frac{1}{K_{2g_{ns}}} \left[ \frac{1}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}} \right] \left[ K_{3g_{ns}}(g_{sw} + g_{L})^3 + K_{3g_{nd}}g_{sw}^3 \right] + \frac{g_{L} \left( g_{sw} + g_{S} \right) K_{2g_{ns}}(g_{sw} + g_{L})^2 + K_{2g_{nd}}g_{sw}^2}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}}
\]

(20)

\[
H_{3s} = \frac{g_{L}}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}} i_{NL3} = \frac{g_{L} \left[ K_{3g_{ns}}(g_{sw} + g_{L})^3 + K_{3g_{nd}}g_{sw}^3 \right] + \frac{g_{L} \left( g_{sw} + g_{S} \right) K_{2g_{ns}}(g_{sw} + g_{L})^2 + K_{2g_{nd}}g_{sw}^2}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}}}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}}
\]

(21)

\[
H_{3d} = -\frac{2}{\pi} \frac{g_{S}}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}} i_{NL3} = -\frac{2}{\pi} \frac{g_{S} \left[ K_{3g_{ns}}(g_{sw} + g_{L})^3 + K_{3g_{nd}}g_{sw}^3 \right] + \frac{g_{S} \left( g_{sw} + g_{S} \right) K_{2g_{ns}}(g_{sw} + g_{L})^2 + K_{2g_{nd}}g_{sw}^2}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}}}{g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L}}
\]

(22)

Typically, \( g_{S} \) is much smaller than both \( g_{SW} \) and \( g_{L} \); hence, \( H_{3s} \) is the main nonlinearity contribution and \( H_{3d} \) may be ignored. Additionally, we can assume that:

\[
g_{sw}g_{S} + g_{sw}g_{L} + g_{S}g_{L} \approx g_{sw}g_{L}
\]

(23)

The simplified expression for Equation (22) is given by:

\[
H_{3s} \approx g_{L} \left[ K_{3g_{ns}} \left( \frac{g_{sw} + g_{L}}{g_{sw}} \right)^3 + K_{3g_{nd}} \frac{1}{g_{sw}} + \frac{K_{2g_{ns}}}{g_{sw}} \left( \frac{g_{sw} + g_{L}}{g_{sw}} \right) \frac{1}{g_{sw}} \left( \frac{g_{sw} + g_{L}}{g_{sw}} \right)^2 + \frac{1}{g_{sw}} \left( \frac{g_{sw} + g_{L}}{g_{sw}} \right)^3 \right] + K_{2g_{ns}}K_{2g_{nd}} \frac{1}{g_{sw}} \left( \frac{g_{sw} + g_{L}}{g_{sw}} \right)^2
\]

(24)

For the triode region, the drain current is equal to:

\[
i_{D} = \mu_{COX}W \left( v_{GS} - V_{TH} \right) \left( v_{DS} - \frac{v_{DS}^2}{2} \right)
\]

(25)
Taking into account the variation of the depletion layer along the channel, (25) can be rewritten in terms of the voltages $v_{GB}$, $v_{DB}$ and $v_{SB}$ (Equation (26)) [23]:

$$
\frac{\mu_{OX} W}{L} \left[ (v_{GB} - V_{FB} - \phi)(v_{DB} - v_{SB}) - \frac{v_{DS}^2}{2}(v_{DB}^2 - v_{SB}^2) - \frac{2}{3}(\phi + v_{DB})^{3/2} - (\phi + v_{SB})^{3/2} \right] \right)
$$

(26)

$$
K_{2g_{nd}} = \frac{1}{2} \frac{\partial^2 i_D}{\partial v_{DB}^2} = -\frac{\mu_{OX} W}{2L} \left[ 1 + \frac{\gamma}{2 \sqrt{\Phi_F + V_{DB}}} \right]
$$

(27)

$$
K_{3g_{nd}} = \frac{1}{6} \frac{\partial^3 i_D}{\partial v_{DB}^3} = \frac{\mu_{OX} W}{24L} \frac{\gamma}{(\Phi_F + V_{DB})^{3/2}}
$$

(28)

$$
K_{2g_{sw}} = \frac{1}{2} \frac{\partial^2 i_D}{\partial v_{SB}^2} = -\frac{\mu_{OX} W}{2L} \left[ 1 + \frac{\gamma}{2 \sqrt{\Phi_F + V_{SB}}} \right]
$$

(29)

$$
K_{3g_{sw}} = \frac{1}{6} \frac{\partial^3 i_D}{\partial v_{SB}^3} = \frac{\mu_{OX} W}{24L} \frac{\gamma}{(\Phi_F + V_{SB})^{3/2}}
$$

(30)

Figure 10 displays the simulation results of $K_{3g_{nd}} / g_{sw}$ and $K_{2g_{nd}} / g_{sw}$. Increasing the $V_B$ leads to a decrease in both $K_{2g_{nd}} / g_{sw}$ and $K_{3g_{nd}} / g_{sw}$ as well as an increase in $g_{sw}$. Finally, from (30), a decrease in $H_{3_s}$ as the $V_B$ increases can be obtained.

![Figure 10. Simulation results of $K_{3g_{nd}} / g_{sw}$ and $K_{2g_{nd}} / g_{sw}$.](image)

Figure 11 provides the simulation results of $K_{3g_{sw}} / g_{sw}$ and $K_{2g_{sw}} / g_{sw}$, according to which we can observe that a small value of $V_S$ is beneficial for linearity.

$$
V_{RF} = \left[ R_{sw} + \frac{1}{\pi^2} Z_{BB}(+j\omega_m) \right] V_{RF} e^{j\phi_{RF}}
$$

(31)

$R_{sw}$ decreases when $V_B$ increases, which means that $V_{RF}$ also decreases, while it is equal to $V_S$. Hence, FBB can improve the linearity of the proposed mixer core. According to the simulation, the MOS of the mixer core with a width of 30 μm has an optimized IIP3 value, as well as good voltage gain and NF performance, as shown in Figure 12a,b. When $V_B = 0.4$ V, compared to $V_B = 0$ V, the voltage gain increased by approximately 1 dB, from 36.3 dB to 37.4 dB; the integrated DSB NF decreased by 0.4 dB, from 3.8 dB to 3.4 dB; and the IIP3 value increased significantly from $-13.6$ dB to $-3.1$ dB.
with a parallel resistor and capacitance for feedback. The TIA gain is, assuming which provides a very high IIP3. The TIA is always composed of an operational amplifier (op-amp) whole circuit. As mentioned in [24], the input impedance of the TIA is “low enough” (\(Z_{\text{in, TIA}} < R_{\text{sw}}\)), which leads to a decrease in both \(H_{\text{dc}}\) and \(I_{\text{IP3}}\) values.

The careful design of the TIA is very important to the noise performance and the linearity of the whole circuit. As mentioned in [24], the input impedance of the TIA is “low enough” (\(Z_{\text{in, TIA}} < R_{\text{sw}}\)), which provides a very high IIP3. The TIA is always composed of an operational amplifier (op-amp) with a parallel resistor and capacitance for feedback. The TIA gain is, assuming \(|A_v(j\omega)| >> 1:\)

\[
\frac{V_{\text{out}}(s)}{I_{\text{in}}(s)} = -Z_f \left| \frac{A_v(s)}{1 + A_v(s)} \right| \approx -Z_f
\]  

(32)

The simulation results of the input impedance of the TIA are shown in Figure 13b. The TIA achieved a DC trans-impedance gain of 1 kΩ \((R_f = 1 \, \text{kΩ})\) and a bandwidth of 20 MHz. The TIA op-amp had a low-frequency gain, an \(A_{\text{vo}}\) of 1000 v/v, and a gain-bandwidth product (GBW) of 1 GHz. When increasing the GBW, the input impedance of TIA remained quite low at a high frequency, which is good for linearity but results in more power consumption. From (32) and Figure 13b, we can observe that gain and linearity are conflicting targets.
Because of the finite output impedance of the mixer, the total output noise would be given by:

\[ v_{\text{nout,amp}}(f) = A(f) \left(1 + \frac{2R_f}{R_{\text{out}}}\right)v_{n,\text{amp}}(f) \]  

(33)

By substituting Equation (10) into Equation (32), we can get:

\[ v_{\text{nout,amp}}(f) = A(f)\left(1 + 16R_f f_{\text{LO}} C_{\text{par}}\right) \]  

(34)

The feedback resistors in the TIA and mixer core should be as small as possible for noise considerations. In this paper, the core of the TIA is a fully differential operational transconductance amplifier (OTA), as shown in Figure 14. The OTA comprises a PMOS input stage and an NMOS load. A common-mode feedback (CMFB) circuit is also adopted to maintain a common-mode voltage of 0.3 V. A PMOS input stage is chosen for a lower noise contribution than that of an NMOS one. The value of the common-mode sensing resistor is chosen to be 1 MΩ. The CMFB op-amp is a single-stage op-amp, consisting of a PMOS input stage and an NMOS current mirror active load. All devices work in saturation mode.

The quadrature LO is generated by a poly-phase filter, as illustrated in Figure 15a.
Because of the finite output impedance of the mixer, the total output noise would be given by:

\[
V_{\text{out}} = V_{\text{amp}} + V_{\text{noise}}\]

(33)

By substituting Equation (10) into Equation (32), we can get:

\[
V_{\text{out}} = V_{\text{LO}} + V_{\text{par}} + V_{\text{vf}} \cdot A_f \cdot R_f \cdot C_f
\]

(34)

The feedback resistors in the TIA and mixer core should be as small as possible for noise considerations. In this paper, the core of the TIA is a fully differential operational transconductance amplifier (OTA), as shown in Figure 14. The OTA comprises a PMOS input stage and an NMOS load. A common-mode feedback (CMFB) circuit is also adopted to maintain a common-mode voltage of 0.3 V. A PMOS input stage is chosen for a lower noise contribution than that of an NMOS one. The common-mode feedback circuit comprises a common-mode sensing stage, along with an operational amplifier to generate the common-mode bias. The value of the common-mode sensing resistor is chosen to be 1 MΩ. The CMFB op-amp is a single-stage op-amp, consisting of a PMOS input stage and an NMOS current mirror active load. All devices work in saturation mode.

![Figure 14. Schematic of the OTA (operational transconductance amplifier) and CMFB (common-mode feedback) circuit.](image)

Figure 14. Schematic of the OTA (operational transconductance amplifier) and CMFB (common-mode feedback) circuit.

The quadrature LO is generated by a poly-phase filter, as illustrated in Figure 15a.

![Figure 15. (a) PPF (polyphase filter) with load and (b,c) two input connection methods.](image)

Figure 15. (a) PPF (polyphase filter) with load and (b,c) two input connection methods.

One branch of the output signal can be derived with the superposition principle:

\[
V_{Q+j} = V_{I+j} \cdot \frac{(sC)^{-1}/Z}{R + (sC)^{-1}/Z} + V_{I-Q} \cdot \frac{R/Z}{(sC)^{-1} + R/Z}
\]

(35)

The output signals of the other three branches are obtained using the same method, thus they can be depicted in a matrix notation:

\[
\begin{bmatrix}
V_{I,\text{out}} \\
V_{Q,\text{out}}
\end{bmatrix} = \frac{Z}{R + Z + sCRZ} \begin{bmatrix}
1 & -sCR \\
sCR & 1
\end{bmatrix} \begin{bmatrix}
V_{I,\text{in}} \\
V_{Q,\text{in}}
\end{bmatrix}
\]

(36)

There are two kinds of input connections in PPF. For the first one (Figure 15b), according to (35), the output voltage ratio of I and Q is:

\[
\frac{V_{Q,\text{out}}}{V_{I,\text{out}}} = \frac{1}{sCR}
\]

(37)

Then, the output signals have the same magnitude at \(\omega = 1/RC\), and the phase difference between I and Q outputs is 90° at all frequencies and with all R and C values in (37). For the second one (Figure 15c), the output voltage ratio of I and Q is:

\[
\frac{V_{Q,\text{out}}}{V_{I,\text{out}}} = \frac{1 - sCR}{1 + sCR}
\]

(38)

The output signals have the same magnitude at all frequencies and with all R and C values in (38). The ratio of the load-to-signal impedances of PPF should be large, which is an effective way to decrease the voltage loss [25]. Meanwhile, the same values of C in the first and second stages and the value of R in the second stage triple that in the first stage are chosen to decrease voltage loss. A square LO signal is good to ensure the performance of the mixing core, thus an LO buffer and driver, comprising an inverter with feedback (linear amplifier) and a series of inverters, is designed. In consideration of power consumption, the driver is biased on subthreshold voltage. The inverter design is based on the standard F04 inverter sizing, meaning that the sizing of each inverter stage progressively increases by a ratio of 3. Figure 16b shows the simulated results of the quadrature LO signal.
which introduced more phase noise than in the simulation.

was fixed at 1 MHz for the measurements. Figure 17 shows that the measured S11 parameter was

was closer to the optimum value of the chip than the circuits simulation, and the large capacitance of

obviously changed with the LO sweep. At 0 dBm LO, the NF was 6.8 dB, i.e., 3 dB higher than the

to 8 dBm at an IF frequency of 1 MHz. The voltage gain remained almost the same, but the NF

can be depicted in a matrix notation:

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One branch of the output signal can be derived with the superposition principle:

One branch of the output signal can be derived with the superposition principle:

\[
I_{\text{out}} = I_{\text{in}} + Q_{\text{out}} - Q_{\text{in}}
\]

Thus, the output signals have the same magnitude at

The measured NF (noise figure) and gain.

The chip was designed and fabricated in a 0.13-μm CMOS process. The chip’s microphotograph

is shown in Figure 17, with an area of 650 μm × 1070 μm. Two off-chip baluns, of the 1720BL15A0100

(Johanson Technology Inc., Camarillo, CA, USA) types and with a 1.5-dB insertion loss from 625 MHz
to 2800 MHz, were used to obtain differential LO and RF inputs. The power supply V_{DD} and the LO

input frequency were set to 1.2 V and 1.2 GHz, respectively, while the down-converted IF frequency

was fixed at 1 MHz for the measurements. Figure 17 shows that the measured S11 parameter was

−15 dB, which means that the RF port was well matched to 50 Ω.

Figure 18 shows the measured conversion gain and the NF of the chip, sweeping LO from −8 dBm
to 8 dBm at an IF frequency of 1 MHz. The voltage gain remained almost the same, but the NF

obviously changed with the LO sweep. At 0 dBm LO, the NF was 6.8 dB, i.e., 3 dB higher than the

simulation result. This is because of the process variation of the R and C values of a poly-phase filter,

which introduced more phase noise than in the simulation.
Figure 19. The measured IIP3.

The port isolation is illustrated in Figure 20. The proposed circuit exhibited notable LO–RF port isolation, and the LO–IF port isolation was even better. The 2LO–RF and IF port isolations were also good.

Figure 18. The measured NF (noise figure) and gain.

Figure 19 shows the measured IIP3 of −2 dBm; the two-tone signal was swept from −50 dBm to −20 dBm with a ±100 kHz spacing at a center frequency of 2.4 GHz and an unchanged LO. The measured results were slightly higher than those of the simulation. The FBB voltage achieved an optimum value that improved the linearity of the circuit. One reason might be that the FBB voltage was closer to the optimum value of the chip than the circuits simulation, and the large capacitance of the printed circuit board (PCB) test board-filtered high-frequency signal might be another reason.

Figure 19. The measured IIP3.

The port isolation is illustrated in Figure 20. The proposed circuit exhibited notable LO–RF port isolation, and the LO–IF port isolation was even better. The 2LO–RF and IF port isolations were also good.

Figure 20. The measured port-to-port isolation.
The time-varying DC offset measurement followed the same process as that mentioned in [26], quantified using the formula:

\[ V_{eq} = V_{\text{leak}} R_{\text{amp}} \frac{G_{LO-BB}}{G_{RF-BB}} \]  

(39)

where \( R_{\text{amp}} \) is a reflection factor at the LNA output port, and both \( G_{RF-BB} \) and \( G_{LO-BB} \) are the conversion gains of the RF and LO signal frequency to the baseband, respectively. The measured DC offset was 0.8 mV with a 1.2 GHz LO at 0 dBm. Table 1 provides a summary of the performance of the chipset in comparison to other subharmonic mixers in the CMOS technology. In this table, we can observe that the proposed front end exhibits notable voltage gain, good IIP3 and acceptable NF performance. To evaluate the dynamic performance of the proposed mixer, a figure of merit \( (FOM) \) was adopted. The performance of the mixer was compared in terms of conversion gain, linearity, noise figure and power dissipation. However, in the prospect of low-cost subharmonic mixing implementation, the consumption of the chip area was taken into account in the \( FOM \) calculation. The LO–RF isolation was also incorporated for a fair comparison of the \( FOM \) with other reported works. The modified \( FOM \) of the subharmonic mixer can be expressed as [13]:

\[ FOM = 10 \log \left\{ \frac{10^{CG/20} + (IIP3-10) + P_{iso}/10}{10^{NF/10} \times P_{dc} \times Area/(mm^2)} \right\} \]

(40)

where \( CG \) is the conversion gain in decibels, \( IIP3 \) is the input-referred third-order intercept point in decibel milliwatts, \( P_{iso} \) is the LO–RF isolation in decibels, \( NF \) is the noise figure in decibels, \( P_{dc} \) is the power consumption of the subharmonic mixer core in megawatts and \( Area \) is the consumption of the chip area for the subharmonic mixer core circuitry in square millimeters. Table 1 shows that the proposed subharmonic front end exhibited an \( FOM \) value of 78.1, which is the highest value compared to other reported works. However, the proposed work had a higher power consumption and a bigger chip area compared to the other works listed in Table 1, because the LNA became the most power-hungry component when the complementary DS method was introduced and occupied most of the chip area. The authors of [8] used a single-to-differential transformer connected to the transconductance stage of the following mixer core, which saved the chip area and power consumption. However, the complimentary DS method could not be used in a single-input LNA. When comparing the proposed circuits to those in [27], the voltage gain, NF and \( FOM \) were better than those of the latter, and the two works achieved nearly the same power dissipation when removing TIAs. When the bias body voltage was set to zero, the figure of merit of the proposed circuit decreased to 67.3, meaning that the FBB technology is suitable for enhancing the performance of the entire circuit.

### Table 1. Performance comparison with published front end.

| Performance Parameters | This Work | [6] | [8] | [13] | [28] | [27] |
|------------------------|-----------|-----|-----|------|------|------|
| Process (µm)           | 0.13      | 0.18| 0.18| 0.18 | 0.18 | 0.13 |
| Topology               | LNA + SHPM + TIA + LO buffer | LNA + SHAM | SHAM | SHAM + SH balun + IF buffer | SHAM + SH LO | LNA + SHPM + LO buffer |
| AM: active mixer; SH: subharmonic | SHAM | SHAM | SHAM | SHAM | SHAM | SHAM |
| RF (GHz)               | 2.401     | 2.4 | 2.4 | 2.401 | 8    | 2.2  |
| LO (GHz)               | 1.2       | -  | -  | 1.2  | 3.95 | -    |
| Supply voltage         | 1.2       | 0.8 | 1.8 | 1.2  | 0.8  | 1.2  |
| DC power (mW)          | 14.4      | 0.65| 9   | 5.82 | 9.8  | 12.7 |
| CG (dB)                | 36.8      | 14.5| 31  | 13.6 | 9.4  | 4.5  |
| IIP3 (dBm)             | -2        | 23  | 3   | 20   | 20.9 | 11   |
| LO-RF isolation        | 90        | 41  | 80  | 65   | 60   | 95   |
| Core size (mm²)        | 0.95      | 0.52| 1.21| 0.12 | 1.57 | 0.4  |
| \( FOM \)              | 78.1      | 25.4| 72.1| 74.7 | 55.0 | 69   |
4. Conclusions

In this paper, a 2.4 GHz front end with subharmonic mixer topology is proposed. The transconductance stage comprises an LNA with a novel complementary DS method for improving linearity. The mixer core is a passive SHM architecture, chosen because the offset of DC and the immunity of flicker noise are suitable for zero-IF. FBB technology is introduced to enhance the performance of the mixer core. To the best of the authors’ knowledge, this is the first time that FBB technology has been adopted in SHPM for performance enhancement and the first time that a Volterra series has been introduced to provide an analytical formula for the FBB of a SHPM core. The measured results show that this process achieves good voltage gain and IIP3, with moderate NF and the highest figure of merit compared to state-of-the-art publications.

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