Submicron Wire Fabrication on Silicon Substrate Based on Atomic Force Microscopy Technique

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Abstract. This article presents on a simple sub-micron wire fabrication by means of local anodic oxidation atomic force microscopy technique. The silicon-based structure consists of two adjacent terminals serve as probing pads and connected with a wire width less than 200 nm. The pad dimension and wire length are 49 µm\textsuperscript{2} and 11 µm each, respectively. The fabrication process is conducted at room temperature 24 – 27 °C with 50 – 60 % relative humidity and operated by commercial atomic force microscopy without any modification done. Furthermore, the local oxidation is performed using gold coated AFM probe tip and assisted by the used of special language supported by the equipment software. In addition, 9.0 V applied voltage with 2 µm / sec writing speed is used to realize the oxidation process. I-V characteristic of bare device shows there is a current flow through the device when a range of voltage is applied. By using this local anodic oxidation technique, the silicon wire-based structure is fabricated and used as gas sensor sensing part. The silicon device demonstrates an increase in resistance as introduced to gas environment. The silicon wire device shows relative sensitivity of 35 % to the oxygen gas.

1. Introduction
Atomic Force Microscopy (AFM) nanolithography is a proven technique to pattern materials at nanometer scale precisely which divided to bias-assisted nanolithography and force-assisted nanolithography [1]. Local oxidation or local anodic oxidation (LAO) which is in bias-assisted class has been used to define structures, modify and develop nano-electronic devices fabrication process with low cost and simple approaches [2]-[3]. In this technique, the bias is applied to the AFM probe tip to generate localized electric field with a distance of nanometer gap between tip and sample [1]. This local oxidation can be used to create oxide patterns on semiconductors and metals such as single electron transistors (SETs), nanomechanical structures, quantum electronic devices and molecular template [2]-[3]. This process is an electrochemical process which sample surface serves as an anode, AFM probe tip acts as a cathode and water molecules serve as electrolytes to the oxidation process [4], [5]-[6]. Under a controlled humidity, water molecules absorbed on substrate surface and AFM probe tip and water layer thickness depends on the relative humidity introduced to the air in the sealed environment [7]. This article will discuss on the device fabrication process by means of atomic
force microscopy local anodic oxidation, physical and electrical characterization of fabricated device and device testing in the target sample environment.

2. Experimental
The p-type SOI (silicon-on-insulator) wafer was used as substrate for structure patterning. Prior to the experiment, the sample was cleaned using standard cleaning process. In this study, a device with two adjacent probing pads that connected with a wire will be fabricated by the aforementioned technique. The fabrication process was performed by commercial atomic force microscopy and operated at temperature and relative humidity of 24 – 27 °C and 50 – 60 %, respectively. Furthermore, the lithography process was assisted with the used of special language supported by the AFM software for process recipe, applied voltage (9 V), writing speed (2 µm / sec) and gold-coated AFM probe tip. The created oxide layer during lithography process will serve as a masking layer for etching process. Therefore, unwanted and underlying silicon layer will be removed using tetramethylammonium hydroxide solution. The masking layer was removed by using diluted hydrofluoric acid to obtain final device. Figure 1 exhibits the schematic diagram of the device fabrication process, starting from oxidation process by using AFM, followed by etching process and masking layer removal.

![Figure 1. Schematic diagram of device fabrication process; (a) oxidation process by means of AFM, (b) etching process, (c) masking layer removal process.](image)

3. Result and discussion
After fabrication process, the device was physically and electrically characterized. Atomic force microscopy and scanning electron microscopy (SEM) were used for physical characterization. For the electrical testing, semiconductor parameter analyzer, (SPA) was used to characterize the fabricated device. Figure 2 shows the SEM image of the final fabricated device. The inset image shows the measured wire diameter using SEM. From the measurement, the wire diameter of fabricated device was approximately 187 nm. In addition, the pad size and wire length were approximately 7 µm x 7 µm and 11 µm each, respectively.
Figure 2. SEM image of fabricated device. The inset image shows the measured wire diameter which around 187 nm.

The fabricated device was electrically characterized by using semiconductor parameter analyzer to measure the current-voltage (I-V) properties. Figure 3 shows the current characteristic of fabricated device (Device_A) as a function of applied voltage which was scanned from -2 V to 2 V. The observed result depicts a current flow through the device from one contact point to another point. However, small current was observed at reverse applied voltage than forward applied voltage. Another set of device with different wire width but has similarity in device structure, namely as Device_B, was fabricated to verify the current-voltage properties. The Device_B wire width has an approximately 40 nm larger than the Device_A. From the graph shown in Figure 4, Device_A conducts more current compared to Device_B, where, Device_A has smaller wire width than Device_B. From the obtained result, therefore, smaller wire width has better conductivity than larger wire width.

Figure 3. Current-Voltage characteristic of fabricated bare device for Device_A.
In order to prolong the functionality of fabricated device, the device (Device_A) was tested under gas environment. The testing was conducted at room temperature and oxygen (O\textsubscript{2}) gas was selected as target gas. The device was exposed to the gas environment in a closed chamber and current values were recorded. Figure 5 depicts the difference in current distribution for bare device and exposed device to the gas environment. The plotted boxplot shows small current distribution for the device that was exposed to the environment containing target gas. The obtained result shows that the resistance of the device leads to increase after target gas exposure. Therefore, different electrical characteristic was observed between bare and gas tested device. In addition, the fabricated device shows relative sensitivity of 35 % to the oxygen gas at room temperature. The percentage of absolute relative sensitivity, S, is defined as (1), where, I\textsubscript{o} and I correspond to current obtained before and after gas exposure, respectively [8]-[9].

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S (%) = \left(\frac{|\Delta I|}{I_o}\right) \times 100 = \left[\frac{(I-I_o)}{I_o}\right] \times 100
\] (1)

At room temperature, a new type of physiochemical phenomenon such as incomplete covalent bonds and dangling bonds will affect the gas sensing behaviour at room temperature [10]. In p-type semiconductor, the majority carriers are holes. As the electrons from the target gas are injected to the valence band and recombine with the holes, this phenomenon leads to increase the resistance by reducing the number of charge carriers. The Fermi level energy will shift from the valence band if more surface donor states ionized and lead to slow down the process. At last, the Fermi level will stop at new energy value due to the dynamic equilibrium is set up between gas molecules diffused out from the surface to rejoin the gas flow and other gas molecules diffuse into the surface. Therefore, this phenomenon leads to increase the resistance of the tested device [11].
4. Conclusion
As conclusion, a device with two probing pads connected with a wire width less than 200 nm was successfully fabricated and tested. Furthermore, the current-voltage characteristic of the fabricated device was verified with different set of wire width device. As the wire width increases, the device conducts less current. In addition, as the device was introduced to the target gas, the current distribution was decreased and higher resistance was observed. Future research will focus on fabrication of various types of device structure and usage of different target gases for device sensing.

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Figure 5. Current distribution of bare device and gas tested device.
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