Optimizing Hardware-Based Network Computation DAGs for Multiple Tenants with SuperNIC

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Abstract—With CPU scaling slowing down in today’s data centers, more functionalities are being offloaded from the CPU to auxiliary devices. One such device is the SmartNIC, which is being increasingly adopted in data centers. In today’s cloud environment, VMs on the same server can each have their own network computation (or network tasks) or workflows of network tasks to offload to a SmartNIC. These network tasks can be dynamically added/removed as VMs come and go and can be shared across VMs. Such dynamism demands that a SmartNIC not only schedules and processes packets but also manages and executes offloaded network tasks for different users. Although software solutions like an OS exist for managing software-based network tasks, such software-based SmartNICs cannot keep up with the quickly increasing data-center network speed.

This paper proposes a new SmartNIC platform called SuperNIC that allows multiple tenants to efficiently and safely offload FPGA-based network computation DAGs. For efficiency and scalability, our core idea is to group network tasks into chains that are connected and scheduled as one unit. We further propose techniques to automatically scale network task chains with different types of parallelism. Moreover, we propose a fair share mechanism that considers both fair space sharing and fair time sharing of different types of hardware resources. Our FPGA prototype of SuperNIC achieves high bandwidth, low latency performance whilst efficiently utilizing and fairly sharing resources.

I. INTRODUCTION

Data-center networking is seeing three trends recently. First, with the slowdown of Moore’s Law and Denard’s Scaling, more network functionalities are offloaded from the CPU to network devices like RDMA NICs. In a cloud or virtualized data-center environment, that means many tenants will be sharing the same network device. Second, more network devices such as SmartNICs [13, 18, 46] and programmable switches [10, 27, 49, 72] are offering programmability that allows users to offload customized network functions. Third, network speed in the data center is increasing fast. Today, 40 Gbps and 100 Gbps are the norm, with 200 Gbps [50] available and 400 Gbps [51] on the horizon.

As a result, we anticipate the need for a SmartNIC that offers (1) multi-tenancy support, (2) programmability, and (3) hardware acceleration. Both (1) and (2) are essential to providing the flexibility, resource-efficiency, and safety of user network computation offloading, while (3) is essential to providing the network-line-rate performance of such offloading. Unfortunately, no existing SmartNIC solutions offer these three features together.

In this paper, we propose SuperNIC (or sNIC for short), a hardware-based, programmable, and multi-tenant SmartNIC. sNIC consists of an ASIC for fixed systems logic that receives, schedules, and sends packets, an FPGA for executing user-offloaded network computation, and software cores for executing the control plane. We support three types of network computation offloading, and we collectively call them network tasks, or NTs. The first type is traditional network stack capabilities running at server CPU, such as a transport layer. The second is network functions commonly seen in today’s data-center network management, such as firewalls and IPSec. The third is application-specific packet processing such as key-value store operations [32, 42], real-time analytics [32], and serverless/microservice functions [13, 48]. In a sense, each NT can be thought of as a network-oriented accelerator that is offloaded to sNIC, and different tenants can dynamically choose what NTs to offload for their workloads.

In addition to deploying single NTs to sNIC, users can deploy a DAG of NTs (i.e., a directed task flow). We expect DAGs of NTs to be more common as they allow users to develop their network computation in a microservice manner or to easily put together a set of existing, third-party NTs [35]. sNIC enables more users to deploy more types of NTs, in a dynamic and more complex way. This presents an interesting and challenging new research question: How to schedule and deploy NTs? Traditional network devices focus on scheduling packets or flows, while operating systems schedule software execution units. It’s unclear how to best schedule and manage hardware-based network tasks.

To answer this question, we first solve a connectivity problem: how to connect NTs to the packet scheduler that receives packets from receiving ports and schedules packets’ execution on sNIC. Prior works [44] connect all NTs to a crossbar, which is then connected to a packet scheduler. As the number of NTs increase, this solution would require a complex crossbar that consumes a huge FPGA area and/or increase switching latency. To solve this scalability problem, our idea is to group NTs that are likely to be executed in a sequence into a chain and only use one port on the crossbar to connect to an entire chain. We increase the flexibility of this chaining design by supporting the skipping of NTs in a chain for packets that do not access the entire chain.

Next, we answer the question of how to improve the latency and throughput of NT DAG execution by introducing two types of parallelism in addition to packet pipelining. The first type explores the parallelism within an NT DAG by executing multiple NT chains in parallel so as to shorten the total execution time of an NT DAG. The second type increases the overall packet execution throughput by creating multiple parallel instances of an NT DAG or a subset of it. We
automatically determine the type and amount of parallelism for an NT DAG based on request load, sNIC resource availability, and proper share of the resource a user gets.

The third key new problem we solve is how to fairly and efficiently share FPGA and other NIC resources across multiple tenants. We support multiple types of resource sharing, including the space sharing of FPGA chip, bandwidth sharing of an NT chain or a part of it, and time sharing an FPGA area by context switching between multiple NT chains. sNIC needs to ensure fairness across tenants when performing all these types of sharing. Traditional fairness solutions only consider space- or time-sharing. We propose an algorithm that jointly considers fair space and time sharing in an adaptive and fine-grained manner. We also propose techniques to avoid or hide the overhead of time sharing FPGA resources across tenants.

We prototype sNIC with FPGA using a 100 Gbps HiTech Global HTG-9200 boards [1]. We build six NTs in three types to run on sNIC: a reliable transport, traditional network functions like firewall and encryption, and application-specific tasks such as key-value data replication and caching. We evaluate sNIC with micro- and macro-benchmarks and compare sNIC with PANIC [44], a recent multi-tenant SmartNIC that supports ASIC-based and CPU-based offloads. Our results show that sNIC is able to deliver 100 Gbps throughput while adding only 196 ns scheduling overhead. Our real NT-DAG experiments reveal that our NT-chain-based scheduling system can largely reduce the crossbar size while reducing NT-DAG latency by up to 40% compared to PANIC. Furthermore, our NT-sharing mechanism improves performance per FPGA area by up to 2.81x, and our fairness algorithm achieves better aggregated utilization while guaranteeing fairness.

II. MOTIVATION AND RELATED WORKS

A. Network Function Offloading in Data Centers

While CPU’s frequency scaling is slowing down, network speed is increasing much faster. Today, most data centers are running at 40 Gbps or 100 Gbps [23, 43]. Soon, 200 Gbps [50] and 400 Gbps [51] networks will arrive. As a result, the CPU consumption of software network stacks becomes increasingly prohibitive. Network stacks tend to consume 30-40% of CPU cycles [8]. As such, more network functionalities are being offloaded from the CPU to various networking devices. For example, RDMA NICs execute a transport layer in hardware and allow the full bypass of the CPU. Another example is Aquila, a recent network system developed by Google that aims for ultra-low-latency communication [23]. Aquila consists of a set of customized network devices called TiNs, each of which provides NIC-like functionality [63] and switching functionality.

Apart from the above processor trend, application needs for accelerated packet processing in a cloud environment are another driver for more powerful SmartNICs that can support different function offloads for many tenants. The first type of needs is traditional network problems like packet scheduling [64], congestion control [60, 61], and load balancing [52]. The second broad type is applications-specific computation such as accelerating consensus [41], storage [28, 29], databases [37, 40, 71], and machine learning [57]. In a cloud environment, a physical machine can host hundreds or even thousands of (lightweight) VMs or containers, each of which could have its own network offloading need. As the cloud keeps adopting more lightweight virtualization environments, we expect this need to grow even more in the future, justifying the need for a device like sNIC.

B. Existing SmartNIC Solutions

SmartNICs are NICs with programmability. Depending on the hardware providing the programmability, SmartNICs can be categorized into three types.

The first type is SoC-based SmartNICs that run a Linux-like operating system to host user software programs, usually on an ARM processor [4, 39]. Software is flexible but cannot sustain the high processing speed needs with today’s 100 Gbps or higher line rate [16].

The second type is ASIC-based SmartNICs, which include specialized network-function accelerators such as AES, compression, regular expression matching, and flow steering/filtering. Although ASICs often offer excellent performance, they only offer fixed sets of functionalities and cannot meet the needs of users who desire to offload customized functionalities. Moreover, ASIC makes it hard and expensive to iterate over versions and updates of deployed network functionalities. Because of the ASIC limitation, many recent SmartNICs combine general-purpose processors with ASIC accelerators [2, 4, 53]. For example, NVidia BlueField SmartNICs [4] use general-purpose cores and several fixed-logic network function accelerators together with an RDMA NIC to support network processing offloading. Although only using the fixed-logic accelerators, BlueField can achieve high throughput, when software offloading is added, the performance drops dramatically [45].

The third type is FPGA-based SmartNICs. Unlike software-based or ASIC-based SmartNICs, FPGA-based ones support full programmability at the hardware speed. Because of this benefit and with FPGA development tool chains becoming mature, FPGA and FPGA-based SmartNICs have been deployed at scale inside Microsoft [18] and Alibaba [19] and offered as a cloud service in public clouds like AWS [58], Alibaba Cloud [7], Tencent Cloud [59]. For the same reason and following cloud trends, we also adopt FPGA as the media for executing NTs in sNIC.

As more data-center workloads and cloud users use FPGA-based SmartNICs, there will be the need to share FPGA-based SmartNICs across multiple tenants. Unfortunately, no existing works provide multi-tenancy support for FPGA-based SmartNICs. This paper fills this hole by proposing the first multi-tenant FPGA-based SmartNIC, sNIC.

Among all prior SmartNIC solutions, PANIC [44] is the most relevant to sNIC. PANIC is a SmartNIC platform that schedules and executes chains of network functionalities for multiple tenants. There are four main differences between PANIC and sNIC. First, PANIC focuses on packet scheduling,
while sNIC focuses on NT scheduling in addition to packet scheduling. Second, PANIC’s design is for fixed-logic network function accelerators and CPU-based compute units. In contrast, sNIC is designed for FPGA-based SmartNICs and solves unique challenges related to FPGA space sharing and reconfiguration. Although PANIC uses FPGA for prototyping, they do not address such FPGA issues. Third, PANIC connects all network function units directly to a crossbar, thereby incurring space and/or performance overhead and scalability limitations. sNIC uses the novel NT-chain mechanism to reduce both the burden on the crossbar and the overhead of the scheduler (§IV-A). Finally, unlike sNIC, PANIC only has primitive fairness support (e.g., Weighted Fair Queuing), not handling fair spatial and temporal allocation of different hardware resources.

C. Multi-Tenancy Support for Generic FPGA Sharing

There are several solutions that provide virtualized, isolated generic FPGA environments that can be used by multiple tenants for computing acceleration as explained below, but none target network acceleration (FPGA-based SmartNICs).

The first sharing mechanism is time multiplexing, where an entire FPGA chip is dedicated to one tenant for a time period before it is reconfigured to serve the next tenant. Today’s cloud FPGA services like AWS F1 [58] take this approach. The main issue with this mechanism is that an FPGA chip can be largely idle when a tenant only uses a small part of it.

The second type is space sharing, where different tenants’ applications run on different parts of an FPGA chip. Initial efforts [11, 12, 17, 34, 68] for FPGA space sharing partition the physical FPGA into fixed sized slots each of which is assigned exclusively to an application. For example, Coyote [36] virtualizes FPGA by dividing it into a number of fixed-size slots and scheduling user tasks onto these slots. Another approach is exemplified by AmorphOS [33], which packs FPGA applications that are then scheduled onto dynamically sized slots. The most recent work, ViTAL [69], compiles and decomposes an FPGA application into a set of fixed-size chunks, each of which can freely run on any fixed-size slots in an FPGA.

Although these prior works proposed various solutions to time- and space-share an FPGA, they are not targeting network usages and are largely orthogonal to sNIC. sNIC is a multi-tenant SmartNIC that customizes the FPGA for executing network task DAGs, by allowing an NT DAG to be broken into subsets that run in different FPGA regions and by allowing different users to share a subset of NTs. In addition to space-sharing and time-sharing with context switching, sNIC also allows multiple tenants to safely share the same NT’s bandwidth. We further propose different types of NT parallelism and autoscaling techniques.

D. Fair Sharing of Network Devices

As more customized network functions are offloaded to network devices, the requirements on multi-tenancy mechanisms also become higher [25, 67]. To provide performant multi-tenancy, a key challenge that needs to be solved is performance isolation.

Performance isolation for network devices is typically provided by a packet scheduling policy that ensures each tenant gets their fair share. A host of solutions have been proposed to fairly share the link bandwidth of network devices [15, 24, 54, 62]. They treat a network device as a single type of resource that is time-shared by different flows. However, today’s SmartNICs have many different types of resources, such as accelerators, general-purpose cores, and on-board memory that can be shared by multiple tenants.

DRF [22] is a seminal multi-resource space-sharing solution that guarantees that the “dominant” resources of different users get their fair share. As the input to DRF, each user specifies a vector whose element represents her demand for a particular type of resource. DRF finds the dominant type of resource and the dominant share for each user. For example, consider a user $x$ who requires 1 CPU core and 4 GB of memory for a unit task. When scheduled on a server with 9 CPU cores and 18 GB of memory, the user’s dominant resource is memory (2/9 of the total memory as opposed to 1/9 of CPU cores). DRF provides an allocation that equalizes the dominant shares of different users while maximizing resource utilization. Suppose another user $y$ demands 3 cores and 1 GB of memory per unit task. DRF would solve the equations of $x + 3y \leq 9$, $4x + y \leq 18$, and $2x/9 = y/3$ (result being $x = 3$, $y = 2$). DRF targets a server setting and does not consider time-sharing by statically assigning each user the exclusive ownership of a part of a resource over the entire duration. It prevents a user from using any statically assigned resource to another user, even if the latter is not using all of it.

DRFQ [21] is a multi-resource fairness algorithm for time-shared resources that allows each user to get the fair time shares of her dominant resource. DRFQ adapts DRF with the additional notion of packet processing time, representing the processing time of a particular packet at a resource. It aims to allocate a fair dominant share of packet processing time across users. This fair time-sharing mitigates the above problem of DRF. However, DRFQ is insufficient for processing hardware like FPGA that can be configured into different units that execute at the same time. DRFQ would treat FPGA as one unit and time share it.

Different from these prior works, sNIC considers both fair space and fair time sharing of its hardware resources (§IV-E), which is what is needed for network processing hardware like FPGA. Another difference is that sNIC needs to consider each NT DAG as a distinct type of resource, because sNIC supports the time sharing of an NT DAG. Moreover, we propose a new approach to measuring user load requirements.

E. Summary

In short, this work is motivated by the need in data centers for multiple tenants to offload an increasing amount of network functionalities to a SmartNIC and for the offloads to be fully programmable, hardware-based, and properly
isolated. As no such solution exists prior to this work, we fill up an important gap in the design space of SmartNICs by building sNIC, a multi-tenant FPGA-based SmartNIC that achieves high and fairly-isolated performance for network task offloading.

III. USAGE MODEL AND DESIGN OVERVIEW

Before delving into the detailed design of sNIC, this section first gives an overview of sNIC, how to use it, its high-level architecture, and path taken by a packet through sNIC.

A. Using SuperNIC

To use sNIC, users first write and deploy NTs as FPGA netlists; they can also use provider-supplied or third-party FPGA netlists. Optionally, users can specify what NT(s) they are willing to share with other users, with sNIC’s guaranteed performance and memory isolation. These NTs are usually supplied by the cloud provider or a trusted third party. We expect users who share NTs to not trust each other but trust the supplier of the shared NTs. We expect most sharing cases to follow this trust model, as user-supplied NTs are application specific and cannot be shared.

After deploying NTs, a user can specify one or more user-written or compiler-generated [38, 65] DAGs of the deployed NTs. Different from traditional NT execution flows that execute NTs in sequence, we also allow multiple NTs to execute in parallel. The sNIC stores user-specified DAGs in its memory and assigns a unique identifier (UID) to each DAG. At run time, each packet carries a UID, which sNIC uses to fetch the DAG.

Finally, in addition to NT DAGs, user also supply their desired ingress bandwidth for each NT DAG. In a cloud setting, this desired ingress bandwidth could be viewed in the same way as how clouds today ask users to specify the size of a VM. Our fairness algorithm will guarantee that all users get at least their desired ingress bandwidth (§ IV-E).

B. Board Architecture and Packet Flow

Figure 1 illustrates the high-level architecture of the sNIC board. sNIC’s data plane handles all packet processing. It consists of reconfigurable hardware (FPGA) for running NTs (blue parts in Figure 1) and a small amount of non-reconfigurable hardware (ASIC) for non-NT systems stacks. sNIC’s control plane is responsible for setting up policies and scheduling NTs. It runs as software on a small set of general-purpose cores (SoftCores for short) (e.g., a small ARM-based SoC). Although by design, sNIC consists of an FPGA, an ASIC, and SoftCores, in our prototype, we built everything on FPGA for ease of deployment.

When a packet arrives at an RX port, it goes through a standard physical and reliable link layer. Then our parser parses the packet’s header and uses a Match-and-Action Table (MAT) to decide where to route the packet next. The parser creates a packet descriptor for each packet and attaches it to its header. The descriptor contains fields for storing metadata, such as an NT DAG UID. Data-plane packet payloads are sent to the packet store. Their headers go to a central scheduler. The scheduler determines when and which NT(s) will serve a packet and sends the packet accordingly. After an NT chain finishes, if there are more NTs to be executed, the packet is sent back to the scheduler to begin another round of scheduling. When all NTs are done, the packet is sent to the TX port.

IV. SUPERNIC DESIGN

A key and unique challenge in designing sNICs is space- and performance-efficient execution of hardware-based NTs in a multi-tenant environment. Moreover, we target a dynamic environment where not only the load of an application but also the applications themselves could change from time to time. Thus, unlike traditional SmartNICs that focus on packet processing and packet scheduling, sNIC also needs to schedule NTs efficiently. We design sNIC to simultaneously achieve several critical goals:

- (G1) a system stack (non-NT parts) that can process packets at line rate.
- (G2) high-throughput, low-latency NT DAG execution.
- (G3) quick adaptation to workload changes.
- (G4) efficient usage of on-board hardware resources.
- (G5) safe and fair sharing of all on-board resources.

This section first discusses how sNIC organizes, deploys, launches, auto-scales, and parallelizes NTs. We then discuss how we schedule packets and how we ensure fairness, and finally, how we build our virtual memory system.

A. NT Region and NT Chain

NT chains and NT regions. As more tenants occupy a server and more types of workloads start to benefit from network task offloading, we anticipate sNIC to handle not only more NTs but also more complex DAGs of NT than a normal SmartNIC. The first challenge that arises from this is the on-board connectivity between the NTs and the scheduler. Previous solutions like PANIC [44] connect all NTs and the scheduler to a central crossbar. The area and performance overheads of a crossbar grow dramatically as its connectivity increases. To tackle this problem, we propose to chain NTs and put one chain (i.e., a sequential list of NTs) in one NT region, as shown in Figure 1. Our observation is that applications usually have the same processing chain for all or most flows, and the chain can thus be accessed as one unit. We then use a much smaller crossbar to connect the central scheduler to the NT regions, thereby reducing hardware complexity and area cost (G4). One NT DAG can have multiple parallel chains in multiple regions, but we do not put parallel chains in one region, as parallel execution of chains need scheduler involvement (§IV-B).

An implication of the above NT chain design is that each unique chain requires its own region, even when some NTs in the chain are the same as NTs in other chains. To more efficiently utilize FPGA space (G4), we propose a mechanism for re-using a part of a chain among multiple NT DAGs. Our idea is to allow the skipping of arbitrary NT(s) in a chain...
NTs to the sNIC platform. The sNIC scheduler sends the same packet to each of the parallel regions by duplicating the packet header. For example, to reduce the execution time of DAGA, we can run NT1→NT2 and NT3 in parallel, as in S2, which reduces DAGA's execution time from four units to three units. Note that after executing NT3, the packet needs to go back to the scheduler, which waits for the completion of NT1→NT2 before executing NT4 (§IV-D). Finally, we create multiple instances of the same NT chain to further increase packet-processing throughput (we call it instance parallelism). The scheduler sends different packets in a round-robin way to the parallel instances of an NT DAG (§IV-D). For example, we create two instances of NT1→NT2 and two instances of NT4 in S3 to improve S2's overall throughput.

We decide the amount of DAG and instance parallelism dynamically. Based on request load to an NT DAG and the fair share we assign to the user, sNIC automatically scales the number of instances of an NT DAG or a subset of it. The number here is not necessarily an integer and can be less than one, as an NT can be shared by multiple users (e.g., NT3 and NT4 in Figure 3). For DAG-level parallelism, we infer the NTs that can run in parallel within a DAG from the DAG architecture and execute them in different regions if the user's fair share of FPGA regions allow and if doing so could reduce the DAG's execution time. We defer the discussion of policy for determining the amount of these parallelism to §IV-E.

C. NT Deployment and Launching

NT deployment. Users deploy NTs to the sNIC platform ahead of time as FPGA netlists and specify DAG of these NTs. We generate a set of FPGA bitstreams, each for a subset of the DAG whose size does not exceed a region (Figure 4). We currently enumerate all possible subsets at deployment time so that sNIC can quickly choose any subset to launch, share, or duplicate at run time without waiting for slow bitstream-generation phases. Future compiler works could optimize this step by better selecting the subsets to generate. When generating bitstreams, we attach a small sNIC wrapper to each NT (Figure 2). This wrapper is essential: it enables skipping an NT in a chain, monitors the runtime load of the NT (§IV-E), ensures signal integrity during PR, and

(1) Users deploy NTs to the sNIC platform in deployed chains of DAGs by skipping NT1 and NT3 in these chains.

NT region. An NT region is the unit to launch an NT chain. Each region can be independently re-programmed via FPGA partial reconfiguration (PR) [47]. Since the FPGA areas for PR need to be pre-determined before launching the FPGA, the region size also needs to be pre-configured. A larger region could fit more NTs in a chain but would waste FPGA space when NTs cannot fill the whole region. Our advised heuristic is to choose a relatively small region size because smaller regions enable more efficient usage of FPGA space. A tradeoff of smaller regions is that NT chains that occupy more space will need to be broken up into sub-chains in multiple regions, and between sub-chains a packet needs to go back to the scheduler. However, a smaller region could still host long chains of small NTs. We observe that it is more beneficial to chain smaller NTs together, as smaller NTs are likely to run shorter. The alternative of not chaining them and going through the scheduler after each small NT would have a bigger relative performance impact on it. Thus, a smaller region size achieves both efficient space utilization and good application performance. It is also possible to divide an FPGA into regions of different sizes, as shown by previous work [33, 69]. In sNIC's context, regions of different sizes could complicate the offline DAG compilation process and the fairness algorithm. We leave this exploration to future work.

B. NT Pipelining and Parallelism

When executing an NT DAG, we exploit various pipelining and parallelism, as illustrated in Figure 3. First, we pipeline a chain of NTs by dividing it into individual NT stages and sending a new packet to each stage in these every new time cycle, as in S1 of Figure 3. Here, the two DAGs share the single chain, and to execute DAGb, NT1 and NT3 are skipped. Second, we execute different chains of a DAG in parallel to reduce the total time needed to process a packet (we call it DAG parallelism). The sNIC scheduler sends the same packet to each of the parallel regions by duplicating the packet header. For example, to reduce the execution time of DAGA, we can run NT1→NT2 and NT3 in parallel, as in S2, which reduces DAGA’s execution time from four units to three units. Note that after executing NT3, the packet needs to go back to the scheduler, which waits for the completion of NT1→NT2 before executing NT4 (§IV-D). Finally, we create multiple instances of the same NT chain to further increase packet-processing throughput (we call it instance parallelism). The scheduler sends different packets in a round-robin way to the parallel instances of an NT DAG (§IV-D). For example, we create two instances of NT1→NT2 and two instances of NT4 in S3 to improve S2’s overall throughput.

We decide the amount of DAG and instance parallelism dynamically. Based on request load to an NT DAG and the fair share we assign to the user, sNIC automatically scales the number of instances of an NT DAG or a subset of it. The number here is not necessarily an integer and can be less than one, as an NT can be shared by multiple users (e.g., NT3 and NT4 in Figure 3). For DAG-level parallelism, we infer the NTs that can run in parallel within a DAG from the DAG architecture and execute them in different regions if the user’s fair share of FPGA regions allow and if doing so could reduce the DAG’s execution time. We defer the discussion of policy for determining the amount of these parallelism to §IV-E.
We now discuss how we launch DAG\textsubscript{b}:
\[\text{S1: Single chain shared by two DAGs}\]
\[\text{NT chain launching.}\]

Our first idea is to pre-launch NTs to avoid application-perceived PR time. Specifically, when the user deploys an NT DAG (prior to when it is accessed), we check if any of its NTs is missing on an sNIC. If so, and if there are free regions on the sNIC, we launch them at these regions.

Afterwards, when a deployed NT DAG is first accessed, we check if any of its NTs are the same as existing NTs on the sNIC. If so, and if the existing NTs still have available bandwidth, we time share the existing NTs with the new application. In this case, new traffic can be served immediately. Otherwise, we check if there is a free region. If so, we enable space sharing by launching the NT at this region, and new traffic can be served after FPGA PR finishes.

If all of the above fail, we invoke a context switch, which is the slowest on-board operation in sNIC and thus our last resort. To perform a context switch, the SoftCore picks the region that is least loaded and goes through a stop-and-launch process. The SoftCore sends a signal to the current NTs to let them “stop”. These NTs then store their states in on-board memory to prepare for the stop. At the same time, the SoftCore informs the scheduler to stop accepting new packets. The scheduler will buffer packets received after this point. After the above steps finish, the SoftCore reads the new bitstream from the on-board memory and starts the FPGA PR process (launch). Afterwards, the newly launched chain can start serving packets, and it will first serve previously buffered packets, if any.

To further reduce PR costs, we use a technique similar to the traditional victim cache [30]. We cache a de-scheduled NT chain in a region around for a while unless the region is needed to launch a new chain. If the de-scheduled NT chain is accessed again during this time, we can directly use it in that region, reducing the need to do PR at that time.

D. Packet Scheduling Mechanism

We now discuss the design of sNIC’s packet scheduling mechanism. Figure 2 illustrates the overall flow of sNIC’s packet scheduling and execution.

Based on the NT-chain architecture, we propose a scheduling mechanism that reduces scheduling overhead and increases the scalability of the scheduler (G1, G2). Our idea is to try reserving credits for an entire NT chain in a region as much as possible and then execute the chain as a whole without involving the scheduler in the middle. Executing chains in their entirety improves both the packet’s processing latency and the central scheduler’s scalability (G5). However, to reserve credits for a whole chain, the schedule needs to wait until each NT in the chain has available credits, which could delay the processing of packets. To mitigate this issue, we only reserve credits for whole chains opportunistically. If all NTs in a chain have available credits when a packet is about to be scheduled, the scheduler reserves a credit from each of these NTs. Otherwise, when not all NTs have available credits, we fall back to PANIC [44]’s scheduling policy by sending the packet to each subsequent NT when it has credits or to the scheduler when it does not.

To utilize multiple instances of an NT chain (§IV-B), our scheduler pipelines different packets to the instances in a round-robin fashion. To explore DAG parallelism, the scheduler makes copies of the packet header and sends them to these regions concurrently. To obey the order of NTs that users specify, we maintain a synchronization buffer to store packet headers after they return from an NT chain’s execution and before they can go to the next stage of NTs (Figure 2).

E. Fairness Policy

As we target a multi-tenant environment, sNIC needs to fairly allocate its resources to different users (G5). These resources include ingress and egress ports, packet-store buffer space, on-board memory space, and FPGA chip area. As explained in §II-D, traditional fairness solutions that target server environments fairly allocate different portions (i.e., space shares) of each type of resource among multiple jobs, and prior fairness solutions that target network devices time share each type of resource.
Different from these traditional environments, we integrate both space and time sharing on an sNIC for more efficient consolidation. This is especially hard for FPGA\(^1\), because we aim to partition an FPGA chip into regions that can be space shared across users and to time share a region across different NT chains via context switching. In addition, we also aim to support the time sharing of the same NT chain across packets from different users. Finally, unlike server computing jobs, network load can vary quickly and by considerable amounts.

To confront the above challenge, our proposal is to tackle space and time sharing one at a time, while “freezing” the other, and to dynamically adjust fair allocation based on observed load, as explained below and illustrated in the example in Figure 4. Overall, our fairness algorithm guarantees a sharing incentive and strategy-proofness with all sNIC’s hardware resources. As defined in the DRF work \cite{22}, a sharing incentive means that each user should be better off sharing the resources than exclusively using her own partition of resources, and strategy-proofness means that users should not be able to benefit by lying about their resource demands.

**Resource requirement and load monitoring.** For a fairness algorithm to work, it needs to know the user demand for each type of resource. Different from previous works \cite{21,22} that ask users to specify this demand for all resources, we use a combination of methods to more automatically and precisely capture resource demands. As introduced in §III-A, users only need to supply their desired ingress bandwidth going to each NT DAG. This is the service level that sNIC will deliver (if sNIC finds that the requirement cannot be met, it will reject the NT DAG). sNIC automatically interprets other demands. When the sNIC platform generates bitstreams of NT DAGs (§IV-C), it captures the FPGA area consumption of the DAG. It also estimates the memory consumption and the egress bandwidth based on the desired ingress bandwidth \cite{21}.

After the user workload starts, sNIC keeps monitoring the load that is needed by each user at every type of resource. If the actual load is lower than the user-input demand, sNIC will only allocate for the actual load, harvesting the remaining for other users. Here, we capture the intended load requirement, not the load that is actually handled by a board unit. For example, for each user, the central scheduler measures the rate of packets that should be sent to an NT before assigning credits; i.e., even if there is no credit for the NT, we still capture the intended load it should handle. We capture the intention so that sNIC can properly and promptly react to potentially satisfy it (under the user’s fair share).

**Step 1: Fair space sharing.** Different from traditional networking devices, sNIC divides its FPGA area and on-board memory spatially across user NTs. Our first step in achieving fair share is to find a fair spatial allocation and determine how many instances of an NT chain (i.e., number of regions) to launch and how much on-board memory to assign to each user. Different from traditional server settings where each resource has a maximum space and users specify the space they need within each resource \cite{22}, our users instead specify their required bandwidth. Thus, we represent the demanded FPGA size to be the FPGA area multiplied by the ratio of user-required bandwidth to the NT’s maximum bandwidth. For example, if a user requires 10 Gbps and uses an NT DAG that occupies 4 units of FPGA area and supports a maximum of 40 Gbps, we will calculate the user’s demand for FPGA as 1 unit (4 * 10/40).

With this representation, we then calculate the FPGA area and memory space to allocate to each user by solving a set of linear equations as in DRF (§II-D). The decision may result in the launch of multiple instances of a DAG (assignment greater than one region) or multiple users sharing NTs (assignment less than one region or the non-integer part of an assignment). Afterwards, we adjust the FPGA area and on-board memory allocation accordingly. We trigger this spatial-allocation step when a new NT DAG is launched or an existing NT DAG is de-scheduled. Thus, even though spatial allocation adjustment involves the slow PR process, it only happens infrequently.

**Step 2: Fair time sharing.** Between two space-sharing steps, the space allocation does not change. Thus, we can treat each NT DAG as a fixed-size resource type, reducing the time-sharing problem to a traditional one. For the time-share allocation, we use the monitored load, since, unlike the space-sharing phase, we can now perform a more fine-grained allocation of time without the need to perform PR. We run the DRFQ \cite{21} algorithm to assign a virtual start time and virtual finish time to each packet, allowing users to time share each NT region, the ingress bandwidth, the egress bandwidth, and the packet store buffer, based on the monitored load at each

\(^{1}\)We time-share other resources like ingress/egress ports and packet buffer and space-share on-board memory.
resource type for each user. Note that we do not time-share on-board memory, since it is usually used to store longer-term data that lives beyond a packet.

Although the calculations in Step 1 and Step 2 are each similar to DRF and DRFQ, we apply them in a novel way: we first treat an FPGA as a single resource with capacity calculated in consideration of area and bandwidth; we then treat each NT region as a separate type of resource and fairly time share them. Another major difference is how we provide strong upper-bound guarantees on the utilization of each resource type for each user. Instead of throttling a user’s packets at each NT and every type of resource to match the desired allocation, we only control the user’s ingress bandwidth allocation. Our observation is that since each NT’s throughput for an application, its packet buffer space consumption, and egress bandwidth are all proportional to its ingress bandwidth, we could effectively control these allocations through the ingress bandwidth allocation. Doing so avoids the complexity of throttling management at every type of resource. Moreover, throttling traffic early on at the ingress ports helps reduce the load going to the central scheduler and the amount of payload going to the packet store.

An example. We now illustrate how our fairness algorithm works with a simple example in Figure 4. There are two users running two DAGs on an sNIC with 6 units of FPGA resource (e.g., LUTs and BRAM). The FPGA is divided into three regions, each of 2 units and each sustaining 10 Gbps. Each NT occupies 1 unit of FPGA resource and sustains the peak bandwidth of 10 Gbps. We assume that U1’s requested ingress bandwidth is 8 Gbps, and U2’s requested ingress bandwidth is 14 Gbps. We further assume that U1’s memory consumption is 1 GB, U2’s memory consumption is 2 GB, and the total memory size is 10 GB. Thus, U1’s FPGA demand is $8 \times 4 = 32$ (i.e., $8/15$ of the total FPGA area-bandwidth product), and U2’s FPGA demand is $14 \times 2 = 28$ (i.e., $7/15$ of the total). U1’s memory demand is 1/10, and U2’s memory demand is 1/5. Thus, for both U1 and U2, their dominant resource type is FPGA. We then run DRF with these demands, which yields the FPGA allocation of U1 to be 32 units and U2 to be 28 units. These allocations represent the bandwidth-area product of U1 and U2 to be 7.27 and 2.73.

V. Evaluation Results

We implemented sNIC on the HiTech Global HTG-9200 board [1], which has nine 100 Gbps ports, 10 GB on-board memory, and a Xilinx U9P chip with 2,586K LUTs and 43 MB BRAM. We implemented most of sNIC’s data path in SpinalHDL [5] and sNIC’s control path in C (running in a MicroBlaze SoftCore [3] on the FPGA). Most data path modules run at 250 MHz. In total, sNIC consists of 23.8k SLOC. Figure 6 shows the FPGA resource consumption of different modules in sNIC and our implemented NTs. The core sNIC modules consume less than 5% resources of the Xilinx U9P chip, leaving most of it for NTs.

Environment. We perform both cycle-accurate simulation (with Verilator [6]) and real end-to-end deployment. For the end-to-end deployment, we use a cluster with a 100 Gbps Ethernet switch, an HTG-9200 board, two Dell PowerEdge R740 servers each equipped with a Xeon Gold 5128 CPU and an NVIDIA 100 Gbps ConnectX-4 NIC, and a Xilinx 10 Gbps ZCU106 board running as the Clio [26] disaggregated memory device. We also project sNIC’s latency in a potential ASIC implementation in a similar way as previous work [70]. We collect the latency breakdown of time spent in third-party IPs and cycles spent in sNIC components. We then scale the frequency of sNIC component to 2 GHz while maintaining the amount of time spent in third-party IPs. This estimate is conservative as most of the latency is introduced in the third-party MAC and PHY modules. Real ASIC implementations of these IPs would lower overall latency further.

For most experiments, we use PANIC as a baseline. As PANIC’s open-source code is specific to their FPGA setup, we re-implemented PANIC’s core scheduling mechanism on our FPGA platform. It uses the same other on-board components like MAC and PHY as sNIC. Our baseline is our own implementation of PANIC’s scheduling mechanism on our platform, where everything else is the same as sNIC.

A. NT and NT DAG Implementation

We implemented three types of NTs and constructed several realistic NT DAGs, which we will present now.
To demonstrate sNIC’s ability of supporting transport offloading, we implemented a simple reliable transport using the go-back-N protocol on top of a lossless network. When the receiver receives an out-of-order packet, it simply discards it and sends a NACK to the sender. When the sender sees a NACK, it will retransmit all packets that were sent after the last acknowledged packet.

We then implement a set of NTs that represent what cloud users use in a Virtual Private Cloud (VPC) setting. VPC allows users to have an isolated network environment where their traffic is not affected by others and where they can deploy their own network functions such as firewall and encryption. We implemented four NTs on sNIC for VPC: network address translation (NAT), firewall, AES encryption, and load balancer.

Application-specific NTs. To demonstrate how users can offload application-specific tasks to sNIC, we build an NT for key-value stores. The NT performs key-value pair caching, where the NT maintains recently written/reads key-value pairs in a small buffer. If there is a cache hit, the NT directly returns the value to the client. Our current implementation that uses simple FIFO replacement already yields good results. Future improvements like LRU could perform even better.

NT DAGs and NT sharing. We deploy several NT DAGs as illustrated in Figure 5. DAG-D is adapted from a prior network-function-chaining work [35]. We further deploy several NT sharing and skipping cases. Here, we assume a scenario where DAG-D already runs on an sNIC, and one of the NTs is then triggered. Because DAG-A/B/C’s NTs all exist in the DAG-D, we can leverage sharing to execute them without launching new DAGs. For example, to execute DAG-A, sNIC skips NAT in DAG-D, execute FW, skips the next three NTs, and finally executes AES.

As the above real NT DAGs were developed in a traditional data-center networking setting that does not have the support like sNIC, they are simple chains of NTs. To explore more complex DAGs, we also evaluated two DAGs with dummy NTs, following the example in Figure 3.

B. Overall Performance

We first test the throughput an sNIC board can achieve with a dummy NT. These packets go through every functional module of the sNIC, including the central scheduler and the packet store. We change the number of initial credits and packet size to evaluate their effect on throughput, as shown in Figure 7. These results demonstrate that our FPGA prototype of sNIC could reach more than 100 Gbps throughput per port, and with more credits in the system, sNIC can reach full bandwidth with smaller packet sizes. With higher frequency, future ASIC implementation could reach even higher throughput.

Next, we evaluate the latency overhead an sNIC FPGA board adds. It takes 1.3 µs for a packet to traverse the entire sNIC data path. Most of the latency is introduced by the third-party PHY and MAC modules, which could potentially be improved with ASIC implementation and/or a PCIe link. The sNIC core only takes 196 ns (or 25 ns with ASIC projection). Our scheduler achieves a small, fixed delay of 16 cycles, or 64 ns with the FPGA frequency (8 ns with ASIC projection). To put things into perspective, commodity switch’s latency is ~0.8 to 1 µs.

C. Deep Dive into sNIC Designs

We now perform a set of experiments to understand the implications of sNIC’s various designs. For these experiments, we generate traffic load using the Facebook distribution [55], which captures various traffic in the Facebook datacenter.

NT chaining. To evaluate the effect of sNIC’s NT-chaining technique and compare it with PANIC, we use an artificial sequence of dummy NTs with length from 2 to 7 (as prior work found real NT chains are usually less than 7 NTs [65]). We also evaluate a case where sNIC splits the chain into two sub-chains. Figure 8 shows the total latency of running the NT sequence with these schemes. sNIC outperforms PANIC because it only goes through the scheduler once (for Single-Chain) or twice (for Half-Chain) for the entire chain, whilst Panic could go through the scheduler after every single NT in the chain.

DAG parallelism and instance parallelism. We evaluate the different parallelism mechanisms introduced in §IV-B by measuring the throughput and latency of the three schemes (S1, S2, S3) in Figure 3 for the two DAGs: DAGa and DAGb. Here, we treat all NTs as dummy ones that simply spins for 10 or 50 cycles for each packet; we set each NT’s max processing bandwidth to 64 Gbps. Figure 10 plots the throughput of packets going to the two DAGs under the three schemes. As can be seen, S3 improves the throughput of DAGas as we launch two instances of NT1, NT2, and NT4. The throughput is less than doubles of S1/S2’s because the two instances of NT2 and NT4 are shared by DAGb.

Figure 11 plots the average execution time of the two DAGs under the three schemes and two different NT processing latency. Adding DAG parallelism (S2) largely reduces the total execution time for DAGa when each NT runs for 50 cycles. However, when each NT runs for 10 cycles, S2 has no execution-time improvement. This is because S2 requires a packet to go back to the scheduler after processing NT3, which adds 16 cycles and is relatively large for short-running NTs. This indicates that when NTs are short running, it is more beneficial to chain them in a single region (§IV-A).

We also evaluate DAG parallelism by increasing the number of dummy NTs. We compare two settings of sNIC and our emulated PANIC. The first setting runs all NTs in parallel;
the second setting splits NTs into two groups and run these groups as two parallel NT-chains (half-parallel). Figure 9 shows the total latency of these schemes. As expected, running all NTs in parallel achieves the best performance. Half-parallel only uses two regions and still outperforms PANIC.

**Real NT DAGs.** We now present real NT DAG evaluation results (DAGs in Figure 5). Figures 12 and 13 plot the latency and throughput of running these DAGs on sNIC and on our emulated PANIC. Similar to the artificial workload, real NT DAGs also benefit from sNIC, both in latency and in end-to-end burst throughput, especially when the DAG is long. We also evaluate the impact of instance parallelism with a real NT DAG (DAG-D). In this DAG, AES is the bottleneck NT, which achieves the lowest bandwidth. Thus, launching two parallel AES NTs in DAG-D-paral, we see a clear throughput increase in Figure 13.

**NT sharing.** We evaluate the effect of sharing NTs by running DAG-D in Figure 5 as a background workload, with bandwidth consumption of 15 Gbps. We then add one of the DAG-A/C as the foreground workload and vary the foreground workload’s traffic load. We compare the foreground workload’s throughput and FPGA area consumption when enabling and disabling NT sharing. We calculate FPGA area consumption by measuring FPGA LUTs and BRAM each NT consumes, normalized to DAG-D-paral’s usage. Figure 17 plots the throughput of DAG-A and DAG-C divided by their area consumed. Overall, sharing improves throughput per area for both DAGs, since without sharing, we would need to launch each DAG in its own region. DAG-A’s throughput keeps increasing as its load increases until 15 Gbps. Afterwards, its throughput saturates at 15 Gbps. This is because the AES NT can only achieve 30 Gbps maximum throughput, and the background DAG-D consumes 15 Gbps. Yet, we still see a small gain in throughput per area. DAG-C does not utilize AES and can fully utilize the unused bandwidth of the remaining NTs in DAG-D. Thus, it can scale to 60 Gbps, providing a large benefit in throughput per area with sharing.

**Effect of victim cache.** To evaluate the effect of our victim-cache design (§IV-C), we set the baseline to be disabling victim cache (blue dot at the middle of Figure 18). We then change how often a de-scheduled NT can be kept around as a victim instead of being completely deleted (shown as percentage on the green line). This models how often an sNIC’s area is free to host victim NTs. As expected, the more de-scheduled NTs we keep around, the better performance we achieve, with no victim cache (baseline) having the worst performance. The OpEx implication is less intuitive. Here, we only count the time and amount of NT regions that are actually accessed, as only those will cause the dynamic power (when idle, FPGA has a static power consumption regardless of how it is programmed). With fewer de-scheduled NTs kept around, more NTs need to be re-launched (through FPGA PR) when the workload demands them. These re-launching overhead causes the OpEx to also go up.

**Effect of area over-commitment.** We change the degree of area over-commitment by limiting how much hardware resources (i.e., NT regions) the workload can use compared to the ideal amount of resources needed to fully execute it. Figure 18 shows that increasing the area over-commitment rate causes worse performance but less resources used.

**Fair resource sharing.** To evaluate the effectiveness of our fairness policy, we ran a synthetic workloads that includes two users and in a multi-resource environment. User 1 runs 4 dummy NTs in a chain, and user 2 runs 2 dummy NTs in a chain. User 2’s chain is a subset of user 1’s. Their user-supplied load requirement is the same. Thus, a good fairness policy should ensure that they each gets half of their dominant resource. We run the two workloads for 100 seconds. At 50 seconds, user 1’s load increases. We evaluate this workload on three different schemes. Static is the baseline, where each user gets assigned an equal number of NT regions. The DRF scheme uses DRF to space share, but does not allow the time-sharing of NT DAGs amongst different users. Finally, sNIC is our complete sNIC fairness policy.
Figure 14 shows the resulting dominant share timeline for the two users, and Figure 15 shows the utilization of each type of resource aggregated across the two users. sNIC consistently delivers fair share for both users even when one user's load changes. In contrast, the DRF scheme cannot adjust to the load change, because it statically decides resource allocation.

Figure 16 shows the aggregated throughput of the two users. By allowing the time sharing of common NT DAGs, sNIC allows for underutilized DAGs to process other users' flows. Thus, sNIC achieves higher aggregated throughput than DRF. Compared to Static, DRF can fully use all the regions, resulting in a slightly higher aggregated throughput Static.

D. End-to-End Application Performance

We now present our end-to-end application performance. For this experiment, we deployed sNIC with Clio [70], a recent disaggregated memory system. Clio includes a client-side server that issues remote-memory access requests such as key-value get and put. It also includes a network-attached hardware-based memory device that hosts the user data and performs the accesses. When deploying sNIC, we connect the sNIC board to the Clio memory board via Ethernet. We then connect the client-side server and the sNIC board to a 100 Gbps Ethernet switch. After the connection, we offload Clio's transport (go-back-N) to sNIC. We further deploy a key-value cache NT in the sNIC.

We run YCSB’s workloads A (50% set, 50% get), B (5% set, 95% get), and C (100% get) [14] for this experiment. We use 100K key-value entries and run 100K operations per test, with YCSB’s default key-value size of 1 KB and Zipf accesses ($\theta = 0.99$). We compare sNIC to several baselines: the original Clio, a one-sided RDMA-based key-value store, Clover [66], a RPC-like RDMA-based key-value store, HERD [31]. We run Clover and HERD with NVidia 100 Gbps ConnectX-4 RDMA NIC. We also run HERD on the NVidia 100 Gbps BlueField-Gen1 SmartNIC.

We evaluate the sNIC performance when we only run the Go-back-N transport NT at it and when we run both the transport NT and the key-value caching NT. Figures 19 and 20 show the latency and throughput of sNIC and other baseline systems. sNIC's performance is on par with Clio, Clover, and HERD, as it only adds a small overhead to the baseline Clio. With caching NT, sNIC achieves the best performance among all systems, esp. on throughput. This is because all links in our testbed are 100 Gbps except for Clio board’s 10 Gbps link, which connects to the sNIC board. When there is a cache hit at the sNIC, we avoid going to the 10 Gbps Clio boards. HERD-BF performs the worst because of the slow link between its NIC and the ARM processor. Newer generations of BlueField are more powerful than BlueField-1. Unfortunately, we do not have access to the newer generations.

VI. CONCLUSION

We presented a multi-tenant, programmable, hardware-based SmartNIC, sNIC, that focuses on optimizing NT DAG execution. Our proposal include the design of NT chain, DAG and instance parallelism, various NT launching optimization techniques, and a full set of fair sharing mechanisms. Our FPGA prototype demonstrates the performance, fairness, and cost benefits of sNIC.
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APPENDIX

A. FPGA Resource Utilization

The following table shows the FPGA resources used by sNIC shell. Most of the resources are left for running NTs.

| Module      | Logic (LUT) | Memory (BRAM) |
|-------------|-------------|---------------|
| sNIC Core   | 4.36%       | 4.74%         |
| Packet Store| 0.91%       | 9.17%         |
| PHY-MAC     | 0.72%       | 0.35%         |
| DDR4Controller| 1.57%    | 0.29%         |
| MicroBlaze  | 0.25%       | 1.81%         |
| Misc        | 1.52%       | 0.75%         |
| **Total**   | **9.33%**   | **17.11%**    |

B. Cost Calculation

We explain the different deployment models and the cost calculation formulas behind our CapEx comparisons. We limit our scope to rack-scale as the higher-level network hierarchies are orthogonal to the resource pool deployment models. We calculate that, to deploy a certain number of endpoints, what's the network cost (i.e., the network interface card, cable, and switch port costs).

We compare the following models: 1) Non-disaggregation model, or the traditional model, termed traditional. 2) Disaggregation model, in which we insert the network pool between endpoints and the ToR switch (Figure ?? (a)), termed ring. 3) Disaggregation model, in which we connect the pool of network devices directly to the ToR switch (Figure ?? (b)), termed direct. For both disaggregation models, we further compare two type of devices: sNIC which has auto-scaling capability and multi-host NIC which can only provision for max resource usage. With runtime dynamic scaling and load balancing features, sNICs can provision for less than the max required resource, the specific ratio is calculated by comparing a particular workload’s the sum-of-peak versus the peak-of-sum.

In all, we have the following models under comparison: traditional, sNIC-direct, sNIC-ring, mhnic-direct, mhnic-ring.

We now detail the cost calculations. In the traditional non-disaggregation model, each endpoint has a full-fledged NIC and a normal high-speed cable for connection to the ToR switch. In both disaggregation models, since most network tasks are offloaded to the network resource pool, each endpoint can use a down-scaled NIC. Furthermore, the last hop link layer between endpoints and the network resource pool is reliable, we can leverage down-scaled, cheaper and less reliable physical cable [73]. We use the following parameters in our calculation:

- Deploy N devices.
- Each switch port has a cost of costSwitchPort
- A full-fledged NIC’s cost is costNIC. A down-scaled NIC cost is costDSNIC.
- A normal high-speed cable cost is costCable. A down-scaled less reliable physical cable cost is costDSCable.
- A consolidation ratio consolidRatio determines how many endpoints are sharing one network resource pool device. We can calculate the number of network pool devices by M = N / consolidRatio.
- For a network device, only a certain portion is dedicated to running network task, other parts are used as shell. We define the cost ratio used by network task to be NTCostRatio.
- The peak-of-sum versus the sum-of-peak yields the auto-scaling potentials. A multi-host NIC (mhnic) provisions for the sum-of-peak while an sNIC provisions for the peak-of-sum. We call this ratio capExConsolidRatio.
- The multi-host NIC’s cost can be calculated as costMHNIC = costNIC * N.
- The sNIC’s cost can be calculated as costSNIC = costMHNIC * capExRatio, in which capExRatio = (1 - NTCostRatio) + NTCostRatio * capExConsolidRatio.

We now define each model’s cost.

The traditional deployment model’s cost is straightforward, it includes NIC, cable and switch ports:

\[ N \times (\text{costNIC} + \text{costCable} + \text{costSwitchPort}) \]  

The disaggregation models’ cost has more moving parts than the traditional. It includes the down-scaled NICs and cables, network pool devices, the cables to the ToR switch, and switch ports.

The first disaggregation model (Figure ?? (a)) can be calculated as follows (for both sNIC-ring, mhnic-ring).

\[ N \times (\text{costDSNIC} + \text{costDSCable}) \]  

The second disaggregation model (Figure ?? (b)) can be calculated as follows (for both sNIC-direct, mhnic-direct).

\[ M \times (\text{costSNIC} + \text{costCable} + \text{costSwitchPort}) \]

This tables shows the real-world numbers we use.

| Parameters       | Value       | Note                                      |
|------------------|-------------|-------------------------------------------|
| costSwitchPort   | $250        | FS 100Gbps switch [29]                    |
| costNIC          | $500        | Mellanox Connect-X3                       |
| costCable        | $100        | FS DAC 100Gbps cable                      |
| costDSNIC        | costNIC * 0.2 | Numbers from our prototype [73]        |
| costDSCable      | costCable * 0.6 | Current model                            |
| consolidRatio    | 4           | Numbers from our prototype                |
| NTCostRatio      | 0.9         | Facebook Hadoop trace [56]                |
| capExConsolidRatio| 0.23       |                                           |

C. End-to-End Application Performance and Cost with Consolidation

To evaluate the benefit and tradeoff of consolidation, we deploy a testbed with four sender and four receiving servers with four setups: each endhost connects to a ToR switch with 100 Gbps or 40 Gbps link (baseline, no consolidation), and four endhosts connect to an sNIC, each with 100 Gbps or 40 Gbps link, and the sNIC connects to the ToR switch with a 100 Gbps or 40 Gbps link (sNIC consolidation). For both
settings, we execute two NTs, firewall and NAT, in FPGA. For the baseline, each endhost has its own set of NTs, while sNIC autoscales NTs as described in §IV-E. On each server, we generate traffic to follow inter-arrival and size distribution reported in the Facebook 2012 key-value store trace [9].

Figure 21 reports the throughput comparison of sNIC and the baseline. sNIC only adds 1.3% performance overhead to the baseline under 100 Gbps network and 18% overhead under 40 Gbps network. We further analyze the workload and found its median and 95-percentile loads to be 24 Gbps and 32 Gbps. With four senders/receivers, the aggregated load is mostly under 100 Gbps but often exceeds 40 Gbps. Note that a multi-host NIC would not be able to achieve sNIC’s performance, as it subdivides the 100 Gbps or 40 Gbps into four 25 Gbps or 10 Gbps sub-links, which would result in each endhost exceeding its sub-link capacity.

We then calculate the amount of FPGA used for running the NTs multiplied by the duration they are used for, to capture the run-time resource consumption with sNIC’s autoscaling mechanism. The baseline has one set of NTs per endhost for the whole duration. Figure 22 shows this comparison when consolidating two and four endhosts to an sNIC and using NTs of different performance metrics. For a slower NT (e.g., one that can only sustain 20 Gbps max load), the sNIC autoscales more instances of it, resulting in less cost saving. Our implementation of firewall NT reaches 100 Gbps, while the AES NT is 30 Gbps, resulting in a 64% cost saving when deploying both of them.