Optimization of DSP Applications Using Parameterized Error Models for Low Power Approximate Adders

Celia Dharmaraj, Student Member, IEEE, Vinita Vasudevan, Member, IEEE, and Nitin Chandrachoodan, Member, IEEE

Abstract—Approximate circuit design has gained significance in recent years targeting error tolerant applications. In this paper, we first demonstrate that the commonly used assumption that the inputs to the adder are uniformly distributed results in an inaccurate prediction of error statistics for multi-level circuits. To overcome this problem, we derive parameterized error models that can be used within any optimization framework in order to optimize the number of approximate bits. We also show that in order to accurately compute the MSE, the optimization framework needs to take into account not just the functionality of the adder, but also its position in the circuit, functionality of its parents and the number of approximate bits in the parent blocks. We demonstrate a significant improvement of accuracy in the prediction of the noise power of DSP systems containing approximate adders.

Index Terms—Approximate computing, error model, static probability, optimization, noise power.

I. INTRODUCTION

Approximate computing is widely used in signal and image processing applications to obtain improvements in power and/or speed while maintaining the required accuracy. Adders are the basic building blocks in these applications and a typical implementation has a large number of adders. A variety of approximate adders have been proposed in the literature, with different levels of trade-offs between accuracy and performance. These adders can be classified as low-latency [1] (and references therein) and low-power approximate adders (LPAA) [2]–[7]. Low power implementations of DSP systems using LPAA optimize the power consumption by maximizing the number of approximate bits in each adder for a given accuracy.

In the literature, multiple approaches have been proposed to find optimal approximation levels for adders used in low power implementations. An approximate Finite Impulse Response (FIR) filter is designed by fixing the level of approximation of the adders using Monte-Carlo (MC) simulations in [8]. Approximate mirror adder-5 (AMA-5) [4] modeled assuming uniformly distributed inputs are used in a 2D Discrete Cosine Transform (DCT) module constructed using 1D DCT blocks in [9] and the optimization problem is solved using a mixed integer non-linear problem solver. Cartesian Genetic Programming (CGP) is used to design various approximate implementations of four point 1D DCT in [10]. An expression for variance of error of AMA 1-5 adders [4] and Lower-part-OR adder (LOA) [5] is obtained in [11] empirically by regression assuming uniform inputs, and heuristics are used to solve the approximation-level optimization problem. In [12], AMA 1-5 adders and Transmission Gate based Approximate adders TGA I-II [13] are considered. An expression for mean square error (MSE) is obtained assuming that the distribution of inputs and error are uniform. This is then used in a Lagrange multiplier based optimization approach.

All of the above previous works on optimization use error metrics based on uniformly distributed inputs. Moreover, the same error model is used for all adders in the circuit. To verify the validity of these assumptions, we found the MSE in an approximate 8 × 8 DCT module [14], that has 288 adders in a 6-level adder tree. We evaluated the noise power in dB (10×log₁₀MSE), assuming an error model for LOA based on uniformly distributed inputs [5] and compared it with values obtained using MC simulations, with 10⁶ uniformly distributed random inputs (NP₁ and NP₁₅ respectively in Table I). The numbers after levels (L₁ − L₆) indicate the number of approximate bits. As seen from Table I the analytical noise power differs from the simulated value by as much as 11 dB, though the model worked well for an individual adder.

While the assumption of uniformly distributed lower order bits may be justified for the primary inputs, neither the output of LPAA nor the error is uniformly distributed. A more accurate method of obtaining the probability mass function (PMF) of error is proposed in [15]. However, including this method within an optimization routine would require extensive computations. Moreover, in most applications, an accurate estimate of the mean error and MSE is sufficient and we do not need the PMF of the error.

In this paper, we show that mean and MSE can be computed accurately without computing the PMF of the error if the number of approximate bits and the static probabilities of the inputs is taken into account. To this end, we derive parame-

| NP₁ | NP₁₅ | e | No. of approximate bits |
|-----|------|---|-------------------------|
| -53.45 | -51.20 | 2.25 | L₁ − L₅: 5; L₆ − L₉: 6 |
| -51.76 | -54.67 | 7.09 | L₁ − L₂: 5; L₃ − L₆: 6 |
| -51.32 | -53.00 | 8.32 | L₁ − L₂: 5; L₃ − L₅: 6; L₆: 7 |
| -50.55 | -41.21 | 9.34 | L₁ − L₂: 5; L₃ − L₄: 6; L₅ − L₆: 7 |
| -47.59 | -36.50 | 11.09 | L₁: 5; L₂ − L₃: 6; L₄ − L₅: 7; L₆: 8 |

TABLE I: Noise power (in dB) of an 8 × 8 DCT module that uses Lower part OR adders. NP₁: Noise power assuming uniform distribution, NP₁₅: Noise power using simulations, e = |NP₁₅ − NP₁|.
erated error models that can be used within any optimization framework in order to optimize the number of approximate bits. We also show that in order to accurately compute the MSE, the optimization framework needs to take into account not just the functionality of the adder, but also its position in the circuit, functionality of its parents and the number of approximate bits in the parent blocks. We demonstrate a significant improvement of accuracy in the prediction of MSE in applications such as FIR filter, IIR filter and DCT using a variety of LPAs.

Each approximate adder requires the static probabilities of its input bits, which eventually traces back to the primary inputs. Even though the PMF of the input signal is usually very non-uniform, the PMF of the lower order bits is often close to uniform, so that simple expressions for the error can be used. Some justification for this assumption is included in [2], but it is heuristic and there is no condition that can be checked to test for uniformity. In this paper, we show that the discrete Fourier transform (DFT) of the input signal has to satisfy certain constraints if the PMF is uniform. This can be used to easily find the maximum number of bits that can be considered to be uniformly distributed.

II. PARAMETERIZED ERROR MODELS FOR LOW POWER APPROXIMATE ADDERS

As mentioned, the simple error models fail to give accurate estimates of the mean error and MSE since they typically assume that the inputs or the error is uniformly distributed. The more complex models that compute the PMF of the error are more accurate, but unsuitable for use in an optimizer. We propose parameterized error models with the input static probability as parameters, that can take into account the input distribution without evaluating the full PMF. The models are more complex than the expressions in [12], but they are analytical expressions, suitable for use in an optimizer.

Assume that an \((N,k)\)-bit LPAA with inputs \(a\) and \(b\) has \(k\) approximate bits and \(N-k\) accurate bits, with \(\hat{s}_i = f(a_i, b_i, \hat{c}_i-1)\) and \(\hat{c}_i = g(a_i, b_i, \hat{c}_i-1)\) denoting the \(i\)th bit of the approximate sum and carry. Let \(P_{s_i}\) denote the static probability of a signal \(x_i\). As with all models in the literature, we continue to assume that \(a\) and \(b\) are independent. This assumption is an approximation when the circuit has non-convergent fanouts. However, it is a reasonable approximation in many cases as correlations are diluted as the logic depth increases, as argued in [15].

The error in the output is due to the approximate lower part sum and the approximate carry to accurate adder. This can be written as

\[
e = \sum_{i=0}^{k-1} (a_i + b_i)2^i - \sum_{i=0}^{k-1} \hat{s}_i2^i - \hat{c}_k-12^k.
\]

The mean error of the approximate adder is given by

\[
E[e] = \sum_{i=0}^{k-1} (P_{s_i} + P_{\hat{s}_i})2^i - \sum_{i=0}^{k-1} P_{s_i}2^i - P_{\hat{c}_k-1}2^k.
\]

To derive \(P_{s_i}\), we need \(P_{\hat{c}_k-1}\). One way to do this is to start with the LSB, for which \(P_{\hat{c}_k-1} = 0\) and find the static probability of all the other carry bits based on the truth table. Alternatively, we can assume that the static probability of the carry is independent of the position i.e., \(P_{c_i} = P_{\hat{c}_i-1}\). This is a reasonable assumption as the input static probability is not expected to vary with location. For example, for AMA-1 if we assume \(P_{c_i} = P_{\hat{c}_i-1}\), we get 0.67 as the static probability, whereas if we use the first method, we get [0.5,0.625,0.656,0.67,0.67] for the five LSBs as in [4]. Using 0.67 as the static probability of the carry, \(P_{c_i} = 0.33\) which matches well with actual values for \(k > 3\). Note that we have not assumed anything about the PMF of the inputs. If it happens to be uniform, we can use \(P_{a_i} = 0.5\). However, if the inputs come from another approximate adder, we just need to use the right value of the static probability.

The MSE \(\langle e^2 \rangle\) can be derived in a similar fashion. The expression for MSE computation requires evaluation of correlated terms such as \(E\{\hat{s}_i \hat{s}_j\}, E\{a_i \hat{s}_j\}, E\{b_i \hat{s}_j\}, E\{a_i \hat{c}_{k-1}\}, E\{b_i \hat{c}_{k-1}\}\) and \(E\{\hat{s}_i \hat{c}_{k-1}\}\) in terms of the static probabilities. Each of these can be derived using truth table of the approximate adder. The correlation between bits \(E\{\hat{s}_i \hat{s}_j\}\) can be neglected in most adders i.e., the individual bits of the sum are independent. However, it is significant in a few adders such as AMA2 \((\hat{s}_i = \hat{c}_i)\), where there is a close relationship between the sum and carry. An exception to this method for deriving error models is ETA-I [6], where the lower part sum cannot be written as a truth table. Its error metrics are derived in our earlier work [10].

III. MULTI-LEVEL SYSTEMS

In DSP systems, the inputs to the adder are either the primary inputs or they are output of another approximate adder, subtractor or (in our case, accurate) multiplier. In each case, the static probabilities of the input needs to be evaluated correctly. We consider each case in the following subsections.

A. Static Probabilities: Primary inputs

Typical PMF of any primary input such as an image is not uniform. However, since error expression of a LPAA involves the static probability of the lower \(k\) bits, we would only need to check if the PMF of these \(k\) bits is uniform. A brute-force technique to check would be to compute the PMF of the lower order bits for each value of \(k\) and check for uniformity of the PMF. In this section, we show that it is possible to check if the distribution is uniform by computing the DFT of the input. A single DFT is sufficient to find the values of \(k\) for which this assumption is reasonable.

Let \(F_A\) be the \(2^N\)-point DFT of the PMF of \(N\)-bit signal \(A\) and \(F_{AL}\) be the \(2^k\)-point DFT of the PMF of \(A_L\) (\(k\) LSBs of \(A\)). We have,

\[
F_{AL}[m] = \sum_{n=0}^{2^k-1} P(A_L = n) e^{-jmn2\pi/2^k} = \sum_{n=0}^{2^k-1} P(A = n) e^{-jmn2\pi/2^k} = \sum_{n=0}^{2^k-1} P(A = n') e^{-jmn'2\pi/2^k} e^{jnt2^k2\pi/2^k},
\]

where

\[
\begin{align*}
L[m] & = \sum_{n=0}^{2^k-1} P(A = n) e^{-jmn2\pi/2^k} \\
& = \sum_{n=0}^{2^k-1} P(A = n) e^{-jmn2\pi/2^k} \\
& = \sum_{n=0}^{2^k-1} P(A = n') e^{-jmn'2\pi/2^k} e^{jnt2^k2\pi/2^k}.
\end{align*}
\]
\[ P(A = n') = \frac{1}{2^{k}} \cdot 0 \leq n < 2^k. \] (4)

If \( A_L \) is uniform, \( P(A_L = n) = \frac{1}{2^{k}} \cdot 0 \leq n < 2^k \). Hence from (5), if \( A_L \) is uniform, we have

\[ F_A[m \cdot 2^{N-k}]_{0 \leq m < 2^k}. \]

Since DFT is unique, the converse is also true. Therefore using (4), we have the following condition to be satisfied for \( A_L \) to be uniformly distributed.

\[ F_A[m \cdot 2^{N-k}] = \begin{cases} 1, & \text{if } m = 0 \\ 0, & \text{if } 0 < m < 2^k. \end{cases} \] (6)

In [17], they have similar condition for continuous signals that are quantized, although the derivation is a little more involved.

To illustrate this condition (6), let us consider the Cameraman image with \( N = 8 \). For the image pixel distribution, \( F_A[m \cdot 2^{N-k}] \) for different values of \( k, m \) varying from 0 to \( 2^k - 1 \), is plotted in Fig. 1. It is seen that for lower values of \( k \), the value of the transform is very close to zero for \( 0 < m < 2^k \). As \( k \) increases, the value of transform also increases and for \( k = 5 \), the values are high. This is confirmed from the actual PMF of the lower order bits of the image shown in Fig. 2. From the figure, it is seen that distribution can be considered uniform even if half the bits are approximated. This turns out to be true for all the standard images we have looked at (for example, for the Lena image, \( k = 6 \), for Rice, \( k = 5 \)). Hence, we assume that the PMF of the lower order bits of primary inputs to the approximate adder is uniform i.e., the static probability is 0.5.

B. Static Probabilities: Adders in the higher levels

If the inputs to the adder are the output of another adder as in Fig. 3a, the mean and MSE are derived using \( P_{s_i} \) and \( P_{c_{i-1}} \) as discussed previously.

The other possibility is that input is the output of a multiplier. In this work, we are only optimizing adders and all multipliers are accurate, with the output truncated to the standard precision used in the circuit. Also, we only consider linear systems, so that one of the inputs to the multiplier is a constant coefficient. In Fig. 3b consider Adder3 which has an input from the output of the multiplier. Depending on the value of the constant coefficient \( c \), the probability of the LSBs at the output of the multiplier \( (P_{b_i}) \) will vary. Let \( P_i \) denote the probability that the \( i^{th} \) bit of the \( k_2 \) LSBs of the multiplicand (output of Adder2) is 1. Consider the following cases.

1) When \( c = 2^l \) and \( l \geq 0 \), the product is the logical left shift of the multiplicand. So \( P_{b_i} = 0 \) for the first \( l \) LSBs and \( P_{b_i} = P_{i-l} \) for the next \( k_2 - l \) LSBs.

2) When \( c = -2^l \) and \( l \geq 0 \), \( P_{b_i} = 0 \) for the first \( l \) LSBs and \( P_{b_i} = 1 - P_{i-l} \) for the next \( k_2 - l \) LSBs is a good approximation, accounting for flipping involved in the two’s complement representation for negative numbers.

3) When \( c = 2^l \) and \( l < 0 \), the product is the right shift of the multiplicand. So \( P_{b_i} = P_{i+l} \) for \( k_2 - l \) LSBs.

4) When \( c = -2^l \) and \( l < 0 \), \( P_{b_i} = 1 - P_{i+l} \) for \( k_2 - l \) LSBs.

5) If \( c \) is an arbitrary constant that is not a power of 2, MC simulations indicate that the average static probability of the output bits is 0.5 ± 0.03. This is also intuitively correct, since the product is the sum of several partial products and the LSBs are truncated to the precision maintained in the system. Hence, the overall PMF is likely to be symmetric (moving towards Gaussian), which means that the static probability is 0.5. So we assume that \( P_{b_i} = 0.5 \) for \( k_2 \) LSBs.

C. Truncation and Median adder (MA) in higher levels

Both Truncation and MA [7] have their lower part sum bits fixed to constant all 0’s and 1’s respectively. In these adders, since the lower part sum is known, the lower part sum of the adders in higher levels can be fixed more accurately so that the accuracy of the approximate circuit is improved. In case of Truncation adder, the approximate sum is obviously zero. In Fig. 3a with MA, Adder1 and Adder2 will have their lower part sum as \( 2^k_1 - 1 \) and \( 2^k_2 - 1 \), respectively. For Adder3, we...
lower the MSE of the circuit by setting the sum to $2^{k_3 + 1} - 1$ instead of $2^{k_3} - 1$ for the following cases:

1) When $k_3 \leq k_1, k_2$, the lower part sum is known exactly and is equal to $2^{k_3 - 1}$.

2) When $k_1 \geq k_3 > k_2$, the mean of the sum is $(3 \times 2^{k_3} + 2^{k_2} - 4)/2$, which is closer to $2^{k_3+1} - 1$ than $2^{k_3} - 1$.

Using this setting, we obtain up to 6 dB improvement in MSE for the adder tree in Fig. 3a. Beyond the first level, the input static probability for Median adders is set to 1.

**IV. Optimization framework**

Classical wordlength optimization uses a simple model for the quantization error and the same model is used for all nodes in the circuit. In the literature, a similar framework with a single expression for error for all the adders has been used to find the optimal number of approximate bits. However, the discussion in the previous section shows that this is inadequate to get accurate numbers. Hence, we made several modifications to the framework, which are detailed below.

The input to the optimizer is the circuit implemented using adders, multipliers and registers and the corresponding signal flow graph. The primary inputs to the system are normalized to $1 \times N$ fixed point numbers. For each functional unit in the system, we use the required number of integer bits while maintaining the number of fractional bits as $N$. The goal of the optimizer is to maximize the number of approximate fractional bits of the adders in the circuit for a given MSE at the output. We use the three step procedure discussed in [18] and adapt it for approximate computing. It uses Minimum Width algorithm, Mildest Greedy Ascent algorithm and Tabu search algorithm. The main steps in our optimization framework are as follows:

- We have a pre-processing step in which adder gets the static probability of the inputs based on its parent nodes. If the parent is a register, it gets the static probability of the inputs to the register. Also, the transfer function from each adder node to the output is computed.

- Next, we run a minimum width algorithm (MWA) that gives the maximum number of approximate fractional bits at the output of each adder when all the other adders are accurate and the required MSE constraint is satisfied.

- Starting with the number of approximate bits from the MWA, a greedy descent procedure is used to decrease the number of approximate bits in the adder that causes the maximum improvement in MSE. An important difference from the quantization noise optimization in [18] is that the approximation noise can worsen even if the number of approximate bits is decreased. For circuits with multiple outputs, we find the fan-in cone of each output in sequence. The adders in the fan-in cone are optimized while keeping the adders in the fan-in cone that increase the MSE of previously targeted outputs untouched.

- Finally we run a tabu search algorithm targeting signals with minimum number of approximate bits (instead of the most sensitive signal) and keep increasing the number of approximate bits as long as MSE constraint is met. We found that this heuristic provides better optimization of approximate bits.

In each of these algorithms, the overall MSE at the output is computed using the transfer functions from the adder nodes and the parameterized error model for the adder.

**V. Experimental results**

In this section, we first validate our error model. Each assumption is tested against simulation and verified for correctness. We then obtain the optimum number of approximate bits for a given MSE using our optimization framework. This is done for FIR and IIR filters and an $8 \times 8$ DCT module. These results are used to show that the optimizer requires the parameterized error models with the correct values of the static probability for accurate prediction of the MSE.

In order to validate our error model, we used the simple adder tree depicted in Fig. 3a. Some of the LPAs like AMA-1 and AMA-2 adders involve carry propagation in the approximate lower part sum. Therefore, in addition to the correct value of the static probability, evaluation of the MSE also requires correlations between bits to be taken into account. Fig. 4 shows a comparison of the error in noise power computation of Adder3 in Fig. 3a (1) assuming $P_{a,i} = P_{b,i} = 0.5$ (2) assuming that the individual bits of each input are independent (i.e. $P_{a,i} = a_i P_a$) (3) assuming that $P_{c,i} = P_{c,i-1}$ (4) using the parameterized error model including all the correlations. It can be seen that $P_{c,i} = P_{c,i-1}$ is a good approximation for $k > 3$. The correlations between the bits in each input can be ignored in AMA-1, AMA-2 requires all correlations to be taken into account. From the discussion in Section III both these results are as expected.

We validated our optimization framework using an 18-tap FIR filter (direct form I realization), IIR filter (direct form II realization of a 4th order low pass Butterworth filter) and DCT [14] consisting of 17, 8 and 288 adders respectively. These are typically the benchmarks that have been used in the literature. For each of these systems, we obtained the optimum number of approximate bits for each adder in the system, given an overall MSE specification. This was done for the Truncation, MA, AMA-5, LOA and ETA-I adders. These adders have minimal hardware for evaluation of the approximate sum and are energy-efficient. Using the optimal configuration of approximate bits for each adder obtained from the optimizer, the circuits are implemented and simulated with $10^5$ uniform random inputs to obtain the actual MSE of the
incorporated these error models in an optimization framework. We have shown that the parameterized error models provide better noise power prediction than the typical error models that assume uniform input distribution. The results of FIR and IIR filters and DCT module show that the use of parameterized error model in the optimization framework improves the accurate prediction of the overall MSE.

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