Limitations on counting in Boolean circuits and self-assembly

Tristan Stérin
Hamilton Institute and Department of Computer Science, Maynooth University
https://dna.hamilton.ie/tsterin/
tristan.sterin@mu.ie

Damien Woods
Hamilton Institute and Department of Computer Science, Maynooth University
https://dna.hamilton.ie
damien.woods@mu.ie

Abstract
In self-assembly, a \( k \)-counter is a tile set that grows a horizontal ruler from left to right, containing \( k \) columns each of which encodes a distinct binary string. Counters have been fundamental objects of study in a wide range of theoretical models of tile assembly, molecular robotics and thermodynamics-based self-assembly due to their construction capabilities using few tile types, time-efficiency of growth and combinatorial structure. Here, we define a Boolean circuit model, called \( n \)-wire local railway circuits, where \( n \) parallel wires are straddled by Boolean gates, each with matching fanin/fanout strictly less than \( n \), and we show that such a model can not count to \( 2^n \) nor implement any so-called odd bijective nor quasi-bijective function. We then define a class of self-assembly systems that includes theoretically interesting and experimentally-implemented systems that compute \( n \)-bit functions and count layer-by-layer. We apply our Boolean circuit result to show that those self-assembly systems can not count to \( 2^n \). This explains why the experimentally implemented iterated Boolean circuit model of tile assembly can not count to \( 2^n \), yet some previously studied tile system do. Our work points the way to understanding the kinds of features required from self-assembly and Boolean circuits to implement maximal counters.

2012 ACM Subject Classification Theory of computation → Models of computation

Keywords and phrases Algorithmic self-assembly, Boolean circuits, computational complexity.

Funding Tristan Stérin: Research supported by European Research Council (ERC) under the European Union’s Horizon 2020 research and innovation programme (grant agreement No 772766, Active-DNA project), and Science Foundation Ireland (SFI) under Grant number 18/ERCS/5746.
Damien Woods: Research supported by European Research Council (ERC) under the European Union’s Horizon 2020 research and innovation programme (grant agreement No 772766, Active-DNA project), and Science Foundation Ireland (SFI) under Grant number 18/ERCS/5746.

Acknowledgements We thank Jarkko Kari for pointing us to key results on Boolean circuits and functions. We thank Christopher-Lloyd Simon for introducing us to the theory of ramification degrees and their application to quasi-bijections. We thank Constantine Evans for helpful discussions on self-assembled counters, and Dave Doty and Erik Winfree for discussions on IBCs over the years.

1 Introduction

Both from the theoretical and the experimental points of view, counting is considered a fundamental building block for algorithmic self-assembly. On the theoretical side, it was established early in the field of algorithmic self-assembly that counters are a tile-efficient method to build a fixed-length ruler. Once one can make a ruler, it can be used to (efficiently) build many larger geometric shapes. For example, using an input structure containing \( O(\log n) \) square tile types, an additional (mere) constant number of tile types can then be used to first make a ruler and then an \( n \times n \) square. Or by using a single-tile seed, a size \( \Theta(\log n / \log \log n) \)
Limitations on counting in Boolean circuits and self-assembly

![Figure 1](image)

**Figure 1** A tile-based 63-counter in the 6-bit Iterated Boolean Circuit (IBC) model. In Section 5 we prove there is no 6-bit IBC 64-counter. (a) Atomic force microscopy image of a self-assembled DNA tile 63-counter. Starting from a seed structure on the left-hand side (not shown), DNA tiles attach to grow the assembled structure from left to right. 1-bits are labelled with yellow ‘circles’ (streptavidin protein), 0s are unlabeled (brown). Scale bar 100 nm. Data taken from [29]. (b) Schematic showing intended assembled tile structure. (c) Zoom-in detail of (b), showing the first (seed) layer with the input bit sequence (from top to bottom) 111101, where yellow tile-glues denote 1 and brown denote 0. (d) Abstract schematic of the 63-counter: the 6-bit input 111101 appears on the left, followed by 62 distinct sequences, followed by 111101 again on the right. (e) Zoom-in of attaching tiles on right-hand side of a partially assembled structure, the attachment of a tile computes a function from two bits to two bits, and the entire tile set encodes the 63-counter algorithm.

tile set can go on to build \(n \times n\) square in optimal expected time \(\Theta(n)\) [23, 8, 1]. These ideas easily generalise beyond squares to a wide class of more complicated geometric shapes [25]. On some models, the combinatorial structure of tile/monomer-type efficient counters can be “loose enough” to allow highly-parallel construction [8, 28], yet in others can be “tight enough” to enable large thermodynamically-stable structures [13]. Counters were also used to build complex circuit patterns [9], universal constructions in self-assembly [12, 10], and as a benchmark for new self-assembly models [13, 21, 17, 22]. Hence, counters, and binary counters in particular, are fundamental to the theory of algorithmic self-assembly [1].

Experimentally, there has been a reasonable amount of effort dedicated to implementing counters [2, 8, 13, 29]. An experimental piece of work [29] (Figure 1), defined a Boolean circuit model of self-assembly, called *iterated Boolean circuits* (IBCs), see Figure 2(a). The model was expressive enough to permit programming of a wide range of 6-bit computations, and physical enough to permit their molecular implementation using DNA self-assembly. When generalised beyond 6-bit inputs to arbitrary inputs of any length \(n \in \mathbb{N}\) the model is Turing universal [29]. However, despite its computational capabilities, the authors of [29] did not manage to find, by hand nor by computer search, any circuit that is a \(2^n\) counter, or *maximal counter* meaning in the 6-bit case an iterated circuit that iterates through \(2^6 = 64\) distinct bit strings before looping forever. Since programming requires some ingenuity, and since the search space for these circuits is huge, it remained unclear whether such maximal

---

1. In contrast though, it should be noted that there are efficient geometry-inspired, and cellular-automata inspired, constructions for building of shapes and or patterns that do not use counters [3]. Although they are not as tile-type efficient as counters, they bring a more geometric, rather than counter-like information-based, flavour to shape construction.

2. There are \(2^{44}\) possible 6-bit IBCs, and that number goes down to around \(10^{10}\) when symmetries are taken into account.
binary counters were permitted by the model or not. In this paper we prove they are not, and more generally give similar results on a class of Boolean circuits called railway circuits and certain classes of self-assembly systems.

Considering Boolean circuits, it is known since [26], in the context of reversible computing, that adding pass-through input bits (i.e. input bits that only copy their value to the output) to reversible Boolean gates prevent them from implementing odd bijections. It is essentially that result that will prevent railway circuits from implementing maximal bijective counters. However, other tools are needed to deal with quasi-bijective maximal counters which, we show, is the only other family (besides bijections) of maximal counters.

1.1 Results

In Section 2, we define a Boolean circuit model called \textit{n-wire local railway circuits}. An \textit{n}-wire railway circuit consists of \textit{n} wires that run in straight parallel lines, with gates that straddle multiple adjacent wires (see Figure 2(b)) such that each gate has its fanin equal to its fanout. Gates are \textit{local} in the sense that no gate may straddle all \textit{n} wires. There is no restriction on the depth of these circuits. Railway circuits are a generalisation of IBCs and allow more possibilities for gate placement and wiring between those gates, yet they are restrictive enough to model a wide variety of self-assembly systems. Building on previous work on reversible circuits [26, 30, 6] and the notion of ramification degree of a function [16, 5, 18], we show that \textit{n}-wire local railway circuits cannot implement \textit{2^n} counters:

\textbf{Theorem 1.} For all \(n > 0\), there is no local \textit{n}-wire railway circuit that implements a \textit{2^n} counter.

More generally we show that no \textit{n}-wire railway circuit implements Boolean functions \(f : \{0,1\}^n \rightarrow \{0,1\}^n\) that are odd bijections or odd quasi-bijections (these terms are defined in Section 2).

We then apply these results to self-assembly in Section 5. We define a class of directed self-assembly systems that compute iterated/composed Boolean \textit{n}-bit functions, layer-by-layer, and show that that class of self-assembly systems are simulated by railway circuits. Hence such systems cannot assemble maximal binary counters. This class includes \textit{n}-bit IBC tile sets, hence we get:

\textbf{Theorem 2.} For all \(n \geq 3\), there is no \textit{n}-bit IBC tile set that self-assembles a \textit{2^n} counter.

While the layer-by-layer class of tile sets is wide enough to include an experimentally implemented IBC tile set [29], and certain zigzag systems (see Section 5), we also find that, from a self-assembly point of view, it is quite a restrictive class. Indeed building maximal counters is achievable through small, and quite reasonable, modifications to that class, which, in turn, highlight improvements that can be made to railway circuits to enable them to maximally count. Hence, this paper outlines some design principles that one should not follow when concerned with designing maximal binary counters. One take home message is that in order to have an \textit{n}-bit tile set that computes a maximal \textit{2^n} counter, layer-by-layer, then one should exploit some property that violates our notion of simulation by railway circuits: for example by having some tiles with fanout not equal to fanin.

1.2 Future work

We defined \textit{n}-wire local railway circuits to specifically model certain kinds of self-assembly systems. We leave as future work to characterise the exact family of Boolean circuits for
Limitations on counting in Boolean circuits and self-assembly

\[ f \in \mathcal{C} \]

\[ g_0, \ldots, g_6 \]

\[ x_0, \ldots, x_5, y_0, \ldots, y_5 \]

(a) Iterated Boolean circuit (IBC) layer with inputs \((x_0, \ldots, x_5)\), Boolean gates \((g_0, \ldots, g_6)\) and outputs \((y_0, \ldots, y_5)\). The circuit computes on a 6-bit circuit input by iterating (repeating) this layer over and over. (b) A railway circuit that simulates a 6-bit IBC. The railway circuit uses 6 wires, is of (horizontal) width 7 and the decomposition of \( f \) into 7 atomic components is shown with each component denoted \( f_{g_0}, f_{g_1}, \ldots \). Black dots delimit sections. The railway circuit is local because none of its gates span all 6 wires.

which Theorem 1 holds. That family is certainly larger than local railway circuits (for example, it would presumably include railway circuits that have gates that straddle up to \( n - 1 \) non-adjacent wires) and goes beyond the scope of the type of circuits discussed in [26] [33] [3], but also provably does not contain the kinds of railway-like circuits that simulate the maximal \( 2^n \) counters from the self-assembly literature discussed in Sections 5.4.2 and 5.4.3.

Another direction is to find the most general class of self-assembly system for which something like Theorem 2 or Theorem 3 holds. Classes of self-assembly systems that are not handled by our techniques include both undirected systems (that exploit nondeterminism in non-trivial ways to produce multiple final assemblies) and systems that do not grow in an obvious layer-by-layer fashion. This would include systems that vary their growth pattern depending on the state of a partially grown counter structure. One approach is to attempt to find a more general class of circuits than railway circuits that models such general self-assembly systems. However, it seems that a different approach might be more profitable as it is not obvious how to map such systems to a clean Boolean circuit architecture.

We leave as open work to explore how our results on self-assembly generalise to higher, even or odd, alphabet sizes beyond the binary alphabet explored here. Existing literature on reversible circuits offers pointers as they characterize the ability of local Boolean gates to implement odd/even bijections when alphabet sizes are larger than two [7].

2 Counting with \( n \)-wire local railway circuits

Let \( n, k \in \mathbb{N}^+ \).

For \( X = \{0, 1, \ldots, m - 1\} \) and \( f : X \to X \) let \( \text{Im}(f) = \{ f(x) | x \in X \} \), denote the image of \( f \), and let, for a finite set \( Y \), \( \text{card}(Y) \) denote the cardinality of \( Y \).

An \( n \)-wire, width-\( k \), railway circuit \( C \) is composed of \( n \) parallel wires divided into \( k \) sections each of width 1. Wires carry bits. A gate \( g \) is specified by the tuple \((s, i, j, f_g)\) where \( s \in \{0, 1, \ldots, k - 1\} \) is called the gate’s section, where \( 0 \leq i, j < n \), and where
\[ f_g : \{0, 1\}^{j-i+1} \to \{0, 1\}^{j-i+1} \] is an arbitrary total function called the gate function of \( g \). The gate \( g = (s, i, j, f_g) \) is of width 1, is located in section \( s \), and there is exactly one gate per section. The gate \( g \) applies its function \( f_g \) to the section’s input wires between \( i \) and \( j \) (included). We use the notation \( f_g \) to refer to the extension of \( f_g \) from \( \{0, 1\}^{j-i+1} \) to the domain \( \{0, 1\}^n \). The extended \( f_g \) simply passes through the bits on which it does not act (i.e. bits outside of the \([i, j]\) discrete interval as shown in Figure 2(b)). A railway circuit computes the circuit function \( f_C : \{0, 1\}^n \to \{0, 1\}^n \) by propagating its \( n \) input bits from section to section and applying at each step the section’s gate function to the appropriate subset of bits. In other words, we have \( f_C = (f_{g_{s-1}}) \circ (f_{g_{s-2}}) \circ \cdots \circ (f_{g_1}) \circ (f_{g_0}) \) with \( g_s \) being the gate in section \( s \). Figure 2(b) gives an example of a class of 6-wire railway circuits of width 7. This example is implementing the 6-bit iterated Boolean circuit model \([29]\) shown in Figure 2(a). A gate \( g = (s, i, j, f_g) \) of an \( n \)-wire railway circuit \( C \) is local if \( j - i + 1 < n \), i.e. the gate does not span all \( n \) wires. The railway circuit \( C \) is local if all of its gates are local. For instance, the railway circuit in Figure 2(b) is local.

The following lemma defines the notion of atomic components. Intuitively, it states that we can decompose the circuit function of a local railway circuit into a composition of functions that have properties crucial to our work.

**Lemma 3 (Atomic components).** Let \( f_C : \{0, 1\}^n \to \{0, 1\}^n \) be the circuit function of a local railway circuit \( C \) of width \( k \). Then there are functions \( f_0, f_1, \ldots, f_{k-1} \) mapping \( \{0, 1\}^n \to \{0, 1\}^n \), called atomic components, with the following three properties:

\[
f_C = f_{k-1} \circ f_{k-2} \circ \cdots \circ f_0 \tag{1}
\]

For all \( 0 \leq i < k \), there exists \( 0 \leq j < n \), such that, \( \forall (x_0, \ldots, x_{n-1}) \in \{0, 1\}^n \):

\[
π_j(f_i(x_0, \ldots, x_{n-1})) = x_j \tag{2}
\]

\[
\forall l \neq j, π_l(f_i(x_0, \ldots, x_{n-1}) = π_l(f_{i-1}(x_0, \ldots, x_{n-1})) \tag{3}
\]

where \( π_j \) is the projection operator on the \( j \)th component.

**Proof.** Let \( f_i = f_{g_i} \) where \( g_i \) is the gate in section \( i \leq n - 1 \). Then, by the definition of \( f_{g_i} \), we have \( f_C = (f_{g_{s-1}}) \circ \cdots \circ (f_{g_1}) \circ (f_{g_0}) = f_{k-1} \circ f_{k-2} \circ \cdots \circ f_0 \) which gives Equation (1).

Intuitively, Equations (2) and (3) state that each function \( f_i \) ignores at least one of its parameters \( x_j \). Since \( C \) is local, for each section \( i \) the gate \( g_i \) is local, meaning there is a \( j \) such that wire \( j \) is pass-through on section \( i \) of the circuit, yielding Equations (2) and (3).

In this paper, we are interested in iterating local railway circuits in order to count. The \( i \)th iteration of a \( n \)-wire railway circuit \( C \) is written \( f_C^i(x) = \underbrace{f_C(\ldots f_C}_{\text{\( i \) times}}f_C(x)) \), with the convention \( f_C^0(x) = x \). Since our input space is of size \( 2^n \), we know that the sequence of iterations of \( C \) on input \( x \) is periodic of period at most \( 2^n \). We define the trace of \( x \) (relative to \( C \)) to be the sequence \( x, f_C^1(x), f_C^2(x), \ldots, f_C^{2^n-1}(x) \), i.e. the first \( 2^n \) iterations of \( C \) on \( x \). We now define what counters are:

---

Note that locality does not prevent long distance influences in the circuit. If one concatenates three instances of the railway circuit in Figure 2(b), they obtain a new railway circuit where every input bit has an influence on every output bit: for instance, \( x_0 \) will influence \( y_5 \).
Limitations on counting in Boolean circuits and self-assembly

Figure 3 Each node represents a distinct n-bit string, each arrow represents application of a circuit function. The figure captures the intuition that there are only two kinds of $2^n$-counter: (a) a cycle that repeats all bit strings forever, and (b) an almost-cycle, that (if we begin at $y$) hits all strings once, and then cycles on a smaller loop. Note that $y$ has no antecedent. (a) is a bijection, (b) is a quasi-bijection.

Definition 4 ($k$-counter). An $n$-wire railway circuit is called a $k$-counter if it meets the following two conditions:
1. For all inputs $x \in \{0,1\}^n$, the number of distinct elements in the trace of $x$ is less or equal to $k$.
2. There exists at least one $x \in \{0,1\}^n$ such that the number of distinct elements in the trace of input $x$ is exactly $k$.

Since this paper is mostly concerned with proving negative results we use a relatively relaxed notion of counter that does not ab initio preclude any 2-bit string-enumerator, including counters that use the 'standard' ordering on binary strings, Gray code counters, etc. Nevertheless, we show a negative result about local railway circuits:

Theorem 1. For all $n > 0$, there is no local $n$-wire railway circuit that implements a $2^n$-counter.

The proof of Theorem 1 is given in Section 4. In order to prove Theorem 1 we are going to describe requirements on the structure of the circuit function of a $2^n$-counter (Lemma 8). Then, we are going to prove limitations on the ability of atomic components $f_0, \ldots, f_{k-1}$ to meet those requirements (Lemma 28). Those limitations will be stable by composition, they will transfer to the entire circuit function $f_C = f_{k-1} \circ f_{k-2} \circ \cdots \circ f_0$ which will end the proof.

Remark 5. In the following, when we talk about a function, in general we will set its domain to be $\{0,1,\ldots,m-1\}$ for some arbitrary $m \neq 0$. When we consider a circuit’s function, the domain of the function is the set of strings $\{0,1\}^n$ which we will sometimes (for convenience) identify with the set of numbers $\{0,1,\ldots,2^n-1\}$, i.e. $m = 2^n$.

Definition 6 (Quasi-bijection). A quasi-bijection $f : \{0,1,\ldots,m-1\} \to \{0,1,\ldots,m-1\}$ is such that there exists exactly one $y \in \{0,1,2,\ldots,m-1\}$ reached by no antecedent: $\forall x \in \{0,1,2,\ldots,m-1\}, f(x) \neq y$.

Remark 7. By the pigeonhole argument, because there is exactly one $y$ with no antecedent in a quasi-bijection $f$, there is also exactly one $z$ which is reached by exactly two antecedents.

Lemma 8. The circuit function of a $2^n$-counter on $\{0,1\}^n$ is either a bijection or a quasi-bijection.

Proof. Figure 3 illustrates the only two behaviors that match the definition of a $2^n$-counter (Definition 4). The case of Figure 3(a) corresponds to the circuit function being a bijection: every $x \in \{0,1\}^n$ has exactly one antecedent. The case of Figure 3(b) corresponds to the circuit function being a quasi-bijection: there is only one $y \in \{0,1\}^n$ that has no antecedent. □
3 Ramification degrees and theory of bijective functions

In order to prove limitations on the expressiveness of atomic components (Lemma 28) we will make use of the general theory of functions and bijective functions.

3.1 Ramification degree of a function

We make use of, in a self-contained manner, the notion of ramification degree of a function which has been developed much further in the field of Analytic Combinatorics [16, 5, 18].

Definition 9 (Ramification degree). Take any function \( f : \{0, \ldots, m - 1\} \rightarrow \{0, \ldots, m - 1\} \). For \( i \in \{0, \ldots, m - 1\} \), define \( a_i(f) \) to be the number of antecedents of \( i \) under \( f \): 
\[
a_i(f) = \text{card}\{j \mid f(j) = i\}.
\]
Define \( r_i(f) \), the ramification degree of input \( i \) under \( f \), to be:
\[
r_i(f) = \max\{0, a_i(f) - 1\}
\]
Finally, define \( r(f) = \sum_{i \in \{0, \ldots, m - 1\}} r_i(f) \) to be the ramification degree of the function \( f \).

\[
f : X \rightarrow X
\]

\[
\text{card}(\text{Im}(f)) = 4
\]

\[
\text{r}(f) = 3
\]

\[
X
\]

\[
X
\]

Figure 4 Illustration of the ramification degree for \( f : X \rightarrow X, X = \{0, 1, \ldots, 6\} \) and \( m = 7 \). Also illustrates Lemma 10: \( r(f) + \text{card}(\text{Im}(f)) = \text{card}(X) = m = 7 \).

We have an elegant way to describe what \( r(f) \) is counting:

Lemma 10. Let \( X = \{0, \ldots, m - 1\} \) and \( f : X \rightarrow X \) then
\[
r(f) = \text{card}(X) - \text{card}(\text{Im}(f)) = m - \text{card}(\text{Im}(f))
\]

Proof. We are going to show that \( r(f) + \text{card}(\text{Im}(f)) = m \). Figure 4 gives a general example of the situation. For \( i \in X \), consider the set \( f^{-1}(i) \) of the antecedents of \( i \) by \( f \). By definition of \( f^{-1}(i) \) we have \( \sum_{i \in X} \text{card}(f^{-1}(i)) = \text{card}(X) \). Now, define \( J \), the set of \( i \) such that \( f^{-1}(i) \neq \emptyset \). By definition of \( r_i(f) \), we have \( r_i(f) + 1 = \text{card}(f^{-1}(i)) \) when \( i \in J \) and \( r_i(f) = 0 \) otherwise. By definition of \( \text{Im}(f) \), we have \( \text{card}(\text{Im}(f)) = \text{card}(J) \). Now we have
\[
r(f) + \text{card}(\text{Im}(f)) = \sum_{i \in X} r_i(f) + \text{card}(J) = \sum_{i \in J} r_i(f) + \sum_{i \notin J} 0 + \text{card}(J)
\]
\[
= \sum_{i \in J} (\text{card}(f^{-1}(i)) - 1) + \text{card}(J) = \sum_{i \in J} \text{card}(f^{-1}(i)) - \text{card}(J) + \text{card}(J)
\]
\[
= \sum_{i \in J} \text{card}(f^{-1}(i)) = \sum_{i \in X} \text{card}(f^{-1}(i)) = \text{card}(X) = m
\]

We can easily describe functions with ramification degree 0 and 1:
Lemma 11. Let \( f : \{0, \ldots, m-1\} \to \{0, \ldots, m-1\} \) then we have the two following equivalences:
1. \( r(f) = 0 \Leftrightarrow f \) is a bijection.
2. \( r(f) = 1 \Leftrightarrow f \) is a quasi-bijection.

Proof. Let \( X = \{0, \ldots, m-1\} \).
1. If \( r(f) = 0 \), by Lemma 10 we have \( \text{card}(\text{Im}(f)) = \text{card}(X) \). It means that \( f \) is surjective, but \( f \) has the same domain and range so \( f \) is bijective.
2. If \( r(f) = 1 \), by Lemma 10 we have \( \text{card}(\text{Im}(f)) = \text{card}(X)-1 \). It means that there is exactly one \( x \in X \) which is not reached by \( f \) so \( f \) is a quasi-bijection (see Definition 6).

An important property of ramification degree is that it does not decrease under composition:

Lemma 12. Let \( f, g \in \{0, \ldots, m-1\} \to \{0, \ldots, m-1\} \). Then we have:
\[
r(f \circ g) \geq \max(r(f), r(g))
\]

Proof. Let \( X = \{0, \ldots, m-1\} \). By Lemma 10, we wish to show that \( \text{card}(\text{Im}(f \circ g)) \leq \text{card}(\text{Im}(f)) \) and \( \text{card}(\text{Im}(f \circ g)) \leq \text{card}(\text{Im}(g)) \). Firstly, we have: \( \text{Im}(f \circ g) \subseteq \text{Im}(f) \). Hence, \( \text{card}(\text{Im}(f \circ g)) \leq \text{card}(\text{Im}(f)) \). Secondly, we have \( \text{Im}(f \circ g) = \{f(x) \mid x \in \text{Im}(g)\} \). It follows that \( \text{card}(\text{Im}(f \circ g)) \leq \text{card}(\text{Im}(g)) \).

From Lemma 12 we immediately get the following:

Corollary 13. Let \( f : \{0, \ldots, m-1\} \to \{0, \ldots, m-1\} \) such that there exists \( f_0, f_1, \ldots, f_{k-1} \) with \( f = f_{k-1} \circ f_{k-2} \circ \cdots \circ f_0 \). Then:
1. \( r(f) = 0 \Rightarrow \forall i, r(f_i) = 0 \)
2. \( r(f) = 1 \Rightarrow \forall i, r(f_i) = 0 \) or \( r(f_i) = 1 \)

Remark 14. Said otherwise, you can only construct a bijection by composing bijections and you can only construct a quasi-bijection by composing bijections and quasi-bijections.

3.2 Bijective functions

The following results about bijections are well-known group theoretic results which the reader can find, for instance, in [24]. Here, we define a few notions that are required to state and prove our main results (Lemma 28 and Theorem 1), with some details left to Appendix A.

Definition 15 (The symmetric group \( \mathfrak{S}_m \)). The set of all bijections with domain and image \( \{0,1,\ldots,m-1\} \), is called \( \mathfrak{S}_m \), the symmetric group of order \( m \). It is a group for function composition \( \circ \) and its neutral element is the identity.

Remark 16. Note that the set of bijections on \( \{0,1\}^n \to \{0,1\}^n \) corresponds to \( \mathfrak{S}_{2^n} \).

Definition 17 (A swap). A swap (or transposition) is a bijection \( \tau \in \mathfrak{S}_m \) which leaves all its inputs invariant except for two that it swaps: i.e. there exists \( i_0 \neq i_1 \in \{0,1,\ldots,m-1\} \) such that \( \tau(i_0) = i_1 \), \( \tau(i_1) = i_0 \) and \( \tau(i) = i \) for all \( i \notin \{i_0, i_1\} \).

Remark 18. A swap is its own inverse: \( \tau \circ \tau = \text{Id} \).

Lemma 19 (Decomposition into swaps). Take any \( f \in \mathfrak{S}_m \). There exists \( p \) swaps \( \tau_0, \tau_1, \ldots, \tau_{p-1} \) such that: \( f = \tau_{p-1} \circ \cdots \circ \tau_0 \). We call \( (\tau_0, \tau_1, \ldots, \tau_{p-1}) \) a swap-decomposition of \( f \).
Proof. Another way to read $f = \tau_{p-1} \circ \cdots \circ \tau_0$ is $\tau_0^{-1} \circ \cdots \circ \tau_{p-1}^{-1} \circ f = \text{Id}$ which means that the composition of transpositions $\tau_0^{-1} \circ \cdots \circ \tau_{p-1}^{-1} = \tau_0 \circ \cdots \circ \tau_{p-1}$ is sorting the permutation $f$ back to the identity. The existence and correctness of the bubble sort algorithm, which operates uniquely by performing swaps, proves that such a sequence of swaps exists: we can take the swaps done by bubble sorting the sequence $[f(0), f(1), \ldots, f(m-1)]$.

▶ Theorem 20 (Parity of a bijection). Let $f \in \mathfrak{S}_m$. The parity of the number of swaps used in any swap-decomposition of $f$ does not depend on the decomposition. If $f = \tau_{p-1} \circ \cdots \circ \tau_0$ and $f = \tau_{p'}_{p'-1} \circ \cdots \circ \tau_0'$ then $p \equiv p'$ [2]. Hence we say that the function $f$ is even if $p$ is even and odd otherwise.

The proof is in Appendix A.

▶ Remark 21. From the points made in the proof of Lemma 19 and in Theorem 20, we can also interpret the parity of a bijection to be the parity of the number of swaps needed to sort it back to the identity.

▶ Example 22. By $f = (1,0,3,2) \in \mathfrak{S}_4$, we mean $f(0) = 1$, $f(1) = 0$, $f(2) = 3$, $f(3) = 2$. The bijection $f = (1,0,3,2)$ is even as we can sort it in 2 swaps by swapping 1 and 0 then 3 and 2. The bijection $f = (0,2,1) \in \mathfrak{S}_3$ is odd as we can sort it in 1 swap by swapping 2 and 1.

▶ Corollary 23 (Multiplication table). When looking at the parity of bijections, the following multiplication table holds: odd $\circ$ odd = even, odd $\circ$ even = odd, even $\circ$ odd = odd, even $\circ$ even = even.

Proof. We give the proof for even $\circ$ even = even, other cases are similar. Take $f, g \in \mathfrak{S}_m$ to be two even bijections. Decompose $f$ and $g$ into swaps: $f = \tau_{p-1} \circ \cdots \circ \tau_0$, $g = \tau'_{q-1} \circ \cdots \circ \tau'_0$. Because $f, g$ are even, we know that $p$ and $q$ are even. Note that $f \circ g = \tau_{p-1} \circ \cdots \circ \tau_0 \circ \tau'_{q-1} \circ \cdots \circ \tau'_0$. Hence there exists a swap-decomposition of $f \circ g$ using an even number, $p + q$, of swaps. By Theorem 20, we conclude that $f \circ g$ is even.

In this paper, we are only concerned by a very specific kind of bijections: $k$-cycles. Indeed, Lemma 20 will show that the circuit function of a bijective $2^n$-counter is a $2^n$-cycle. The parity of a $k$-cycle is easy to compute: it is equal to the parity of $k - 1$ (Theorem 25).

▶ Definition 24 ($k$-cycle). For $k \geq 1$, a $k$-cycle $\rho \in \mathfrak{S}_m$ is a bijection such that there exists distinct $x_0, x_1, \ldots, x_{k-1} \in \{0, \ldots, m-1\}$ such that $\rho(x_0) = x_1, \rho(x_1) = x_2, \ldots, \rho(x_{k-1}) = x_0$ and $\forall x \notin \{x_0, \ldots, x_{k-1}\}$, $\rho(x) = x$.

▶ Theorem 25 (Parity of $k$-cycle). A $k$-cycle $\rho$ has the parity of the number $k - 1$. It means that $\rho$ is odd iff $k - 1$ is odd and $\rho$ is even iff $k - 1$ is even.

The proof is in Appendix A.

▶ Lemma 26. The circuit function of a bijective $2^n$-counter is a $2^n$-cycle.

Proof. The mapping produced by the circuit function of a bijective $2^n$-counter is illustrated in Figure 3(a), it matches the definition of a $2^n$-cycle and generalises to any $n \in \mathbb{N}^+$.

---

4 Also known as the “Futurama theorem” [https://www.youtube.com/watch?v=J650tFfL94c]
Corollary 27 (Bijective $2^n$-counters have odd circuit functions). The circuit function of a $2^n$-counter is an odd bijection.

Proof. We know that the circuit function of a $2^n$-counter is a bijection (Lemma 8). We know that it is a $2^n$-cycle (Lemma 26). Hence, a $2^n$-counter has the parity of $2^n - 1$ which is odd (Theorem 25).

4 Local railway circuits do not count to $2^n$

Here we use the results of Section 3 to show our main result, Theorem 1, by giving two results on atomic components. The first is that atomic components are not quasi-bijections. This result is known in the context of reversible circuits [26, 30, 6], we give a proof that fits our framework of railway circuits. The second is that atomic components are not quasi-bijections.

Lemma 28 (Locality restricts atomic components). Let $f_C = f_{k-1} \circ f_{k-2} \circ \cdots \circ f_0$ be the decomposition into atomic components of the circuit function of a local $n$-wire railway circuit. Then we have the following:

1. No $f_i$ can be an odd bijection
2. No $f_i$ can be a quasi-bijection, i.e., $r(f_i) \neq 1$

Proof. In the following, when we refer to the truth-table of $f_i$, we mean the Boolean $(n, 2^n)$ matrix where the $p^{th}$ column corresponds to the bits of the $p^{th}$ element in the $2^n$-long sequence $[f_i(0, 0, \ldots, 0), f_i(0, 0, \ldots, 1), \ldots, f_i(1, 1, \ldots, 1)]$.

1. Because $f_i$ is local either its first bit or its last bit has to have the properties outlined in Lemma 3, Equations 2 and 3. Two cases:

   - Let suppose that the first bit of $f_i$ has the properties: it is pass-through ($y_0 = x_0$) and it does not affect any other output bits than $y_0$. Then, $M$, the truth-table of $f_i$ has a very remarkable structure, the first line is composed of $2^{n-1}$ zeros followed by $2^{n-1}$ ones. Furthermore, the following $(n - 1, 2^{n-1})$ sub-matrices of $M$, $M_1$ and $M_2$ are equal. The sub-matrix $M_1$ is defined by excluding the first row of $M$ and taking the first $2^{n-1}$ columns while $M_2$ also excludes the first line of $M$ but takes column between $2^{n-1}$ and $2^n$. Indeed, since $x_0$ has no influence on $y_1, \ldots, y_{n-1}$ we have $M_1 = M_2$. That means that we can sort $M$ in an even number of steps by using twice the sequence of swaps needed to sort $M_1 = M_2$: we first sort the first half of $M$ then transpose the swaps we used to the second half. Hence, since we can use an even number of swaps to sort $f_i$, by Theorem 20, $f_i$ is even.

   - Let suppose that the last bit of $f_i$ has the properties: it is pass-through ($y_{n-1} = x_{n-1}$) and it does not affect any other output bits than $y_{n-1}$. Again, $M$, the truth-table of $f_i$ has a very remarkable structure: an even column $p$ is such that column $p + 1$ share the same first $n - 1$ bits and the last bit of column $p$ is 0 while the last bit of column $p + 1$ is 1. Column $p$ and column $p + 1$ are next to each other in lexicographic order. It means that we sort the columns of $M$ by swapping blocks of two columns at each step. Since swapping two blocks of two columns can be implemented by using 2 swaps, with this technique, we will use a multiple of 2 swaps to sort the table. By Theorem 20, it implies that $f_i$ is even.

2. The truth-table of a quasi-bijection has the following properties: only two columns appear twice with $n$-bit vector $x_0 \in \{0, 1\}^n$ and exactly one $n$-bit vector $x_1 \in \{0, 1\}^n$ appears nowhere in the table. The Hamilton distance of $x_0$ and $x_1$ is at least one. Let suppose that $x_0$ and $x_1$ disagree in their $j^{th}$ bit, $\pi_j(x_0) \neq \pi_j(x_1)$. W.l.o.g we can take $\pi_j(x_0) = 1$. Now, because the vector $x_0$ is the only vector to appear twice in the truth table, it means
that on the $j^{\text{th}}$ line of $M$ we see $2^{n-1} + 1$ ones versus $2^{n-1} - 1$ zeros, so we see an odd number of ones and an odd number of zeros. That contradict the fact that, because $f_i$ is local, $y_j$ does not depend on at least one input and hence, the number of zeros and ones on the $j^{\text{th}}$ line of $M$ is at least a multiple of 2. ▶

We now have all the elements to prove our main result:

**Theorem 1.** For all $n > 0$, there is no local $n$-wire railway circuit that implements a 2$^n$-counter.

**Proof.** Consider the circuit function of a local $n$-wire railway circuit $C$ which implements a 2$^n$-counter and its decomposition into atomic components, $f_C = f_{k-1} \circ f_{k-2} \circ \cdots \circ f_0$. We know that $f$ must be either a bijection or a quasi bijection (Lemma 8), giving two cases:

1. If $f$ is a bijection, by Corollary 13 each atomic component must be a bijection too. Furthermore, by Corollary 27 $f$ must be an odd bijection. But, with Lemma 28 we know that each atomic component can only be an even bijection, and by Corollary 28 composing even bijections only leads to even bijections. Hence, $f$ cannot be odd and there are no bijective 2$^n$-counter.

2. If $f$ is a quasi-bijection, by Corollary 13 each atomic component must be either a bijection or a quasi-bijection. Furthermore we need at least one atomic component to be a quasi-bijection since composing bijections only leads to bijections. However, Lemma 28 shows that no atomic component can be a quasi-bijection. Hence, $f$ cannot be a quasi-bijection and there are no quasi-bijective 2$^n$-counter. ▶

## 5 Self-assembled counters

Here we apply the Boolean circuit framework already established in previous sections to show limitations of self-assembled counters that work in base 2. We give a short description of the abstract Tile Assembly Model (aTAM) [27, 23]. more details can be found elsewhere [20, 11].

### 5.1 Self-assembly definitions

Let $\mathbb{N} = \{0, 1, \ldots\}$, $\mathbb{N}^+ = \{1, 2, \ldots\}$, and $\mathbb{Z}, \mathbb{R}$ be the integers and reals.

In the aTAM, one considers a set of square tile types $T$ where each square side has an associated **glue type**, a pair $(s,u)$ where $g$ is a (typically binary) string and $u \in \mathbb{N}$ is a glue strength. A tile $(t, z) \in T \times \mathbb{Z}^2$ is a positioning of a tile type on the integer lattice. A glue is a pair $(g, z) \in G \times \mathbb{H}$ where $\mathbb{H}$ is the set of half-integer points $\mathbb{H} = \{z + h \mid z \in \mathbb{Z}^2, h \in \{(0, 0.5), (0.5, 0)\}\}$ and $G$ is the set of all glue types of $T$. An assembly is a partial function $\alpha : \mathbb{Z}^2 \to T$, whose domain is a connected set. For $X \subset \mathbb{Z}^2$ we let $\alpha|_X$ denote the restriction of $\alpha$ to domain $X$, i.e. $\alpha|_X : X \to T$ and for all $z \in X$, $\alpha(z) = \alpha|_X(z)$.

Let $T = (T, \sigma, \tau)$ be an aTAM system where $T$ is a set of tile types, $\tau \in \mathbb{N}^+$ is the temperature and $\sigma$ is an assembly called the seed assembly. The process of self-assembly proceeds as follows. A tile $(t, z)$ **sticks** to an assembly $\alpha$ if $z \in \mathbb{Z}^2$ is adjacent in $\mathbb{Z}^2$ to, but not on, a tile position of $\alpha$ and the glues of $t$ that touch $\mathbb{H}$ glues of $\alpha$ of the same glue type have the sum of their strengths being at least $\tau$. A tile **placement** is a tuple $(t, z, \ln) \in T \times \mathbb{Z}^2 \times \{N, E, S, W\} \times \mathbb{Z}^4$, where $\ln$ denotes the $k \in \{1, 2, 3, 4\}$ tile sides which stick with matching glues and are called **input sides**; the remaining $4 - k$ sides are called

---

\(^5\) A pair of glues touch if they share the same half-integer position in $\mathbb{H}$. 

---
output sides. For example, a tile of type \( t \) that binds at position \( z \) using its north and west side would be denoted \((t, z, (N, W))\). After the tile placement \((t, z, \text{In})\) to assembly \( \alpha \), the resulting new assembly \( \alpha' = \alpha \cup \{z \rightarrow t\} \) is said to contain the tile \((t, z)\), and we write \( \alpha \to_T \alpha' \). An assembly sequence is a sequence of assemblies \( \vec{\alpha} = \alpha_0, \alpha_1, \ldots, \alpha_k \) where for all \( i \), \( \alpha_i \to_T \alpha_{i+1} \), in other words: each assembly is equal to the previous assembly plus one newly-stuck tile. A terminal assembly of \( T \) is an assembly to which no tiles stick. \( T \) is said to be directed if it has exactly one terminal assembly and undirected otherwise.

### 5.2 Computing Boolean functions by self-assembly

The following definitions are for representing Boolean functions as assembly systems.

**Definition 29** (bit-encoding glues). A bit-encoding glue type is a pair \( g = (s, b) \in \Sigma^* \times \{0, 1, \epsilon\} \), where \( s \) is a string over the finite alphabet \( \Sigma \). If \( b \neq \epsilon \), \( g \) is said to encode bit \( b \), otherwise if \( b = \epsilon \), we say \( g \) does not encode a bit. A bit encoding glue is a pair \((g, z)\) where \( g \) is a bit-encoding glue type, and \( z \in \mathbb{H} \) is a position.

In a tile placement, if a bit encoding glue is on an input side of the tile placement we call that an input bit to the tile placement, if it is on an output side it is called an output bit.

**Definition 30** (Cleanly mapping tile placements to a railway circuit gate). Let \( A \) be a set of assembly sequences that use tiles with bit-encoding glues, let \( z \in \mathbb{Z}^2 \) be a position, and \( P_z \) be union of the tile placements from position \( z \) over all \( \vec{\alpha} \in A \). \( P_z \) is said to cleanly map to a railway circuit gate if

- (a) each \( \vec{\alpha} \) has a tile placement at position \( z \); and
- (b) there is a \( k \in \{0, 1, 2\} \) such that all placements in \( P_z \) map \( k \) input bits to \( k \) output bits; and
- (c) if an \( \epsilon \)-glue \( g \) (non-\( 0/1 \) encoding glue) appears at direction \( d \in \{N, W, S, E\} \) for some \( \vec{\alpha} \in P_z \) then all \( \vec{\alpha}' \in P_z \) have glue \( g \) at direction \( d \).

**Remark 31.** The previous definition is crafted to allow glues to encode bits in a way that can be mapped to railway circuit gates, but also to prevent tiles from exploiting non-bit-encoding glues to “cheat” by working in a base higher than 2.

**Definition 32** (glue curve). A glue curve \( c : (0, 1) \to \mathbb{R}^2 \) is an infinite-length simple curve\(^6\) that starts as of a vertical ray from the south, then has a finite number of unit-length straight-line segments that each trace along a tile side (and thus each touch a single point in \( \mathbb{H} \)), and ends with a vertical ray to the north.

By a generalisation of the Jordan curve theorem to infinite-length simple polygonal curves, a glue curve \( c \) cuts the \( \mathbb{R}^2 \) plane in two \( \text{H} \) (Theorem B.3). We let \( \text{LHS}(c) \subseteq \mathbb{Z}^2 \) denote the points of \( \mathbb{Z}^2 \) that are on the left-hand side\(^7\) of \( c \), and \( \text{RHS}(c) \subseteq \mathbb{Z}^2 \) denote the points of \( \mathbb{Z}^2 \) that are on the right-hand side of \( c \). For a vector \( \vec{v} \) in \( \mathbb{R}^2 \) we define \( c + \vec{v} \) to be the curve with the same domain as \( c \) (the interval \((0, 1))\) but with image \( \cup_{x \in (0, 1)} c(x) + \vec{v} \) i.e. the translation of the image of \( c \) by \( \vec{v} \).

For an assembly \( \alpha \) and glue curve \( c \) let \( \alpha \cap c = g_0, g_1, \ldots \) denote the sequence of all glues of tiles of \( \alpha \) that are positioned on \( c \), written in \( c \)-order. Let \( \mathcal{B} : \{g \mid g \text{ is a sequence of bit-encoding glues}\} \times \mathcal{F} \to \mathcal{O} \) the set of all glue curves.
Proof. then sticks to Definition 35.

|Definition 33 (Layer-computing an n-bit function). Let \( n \in \mathbb{N} \). The tile set \( T \) is said to layer-compute the n-bit function \( f : \{0, 1\}^n \rightarrow \{0, 1\}^n \) if there exists a temperature \( \tau \in \mathbb{N} \), a glue curve \( c \), and a vector \( \vec{v} \in \mathbb{R}^2 \) with positive x-component such that, for all \( i \in \{1, 2, \ldots, n\} \), \( \text{Im}(c) \cap \text{Im}(c + i \cdot \vec{v}) = \emptyset \), and for all \( x \in \{0, 1\}^n \) there is an assembly \( \sigma_x \) positioned on the left-hand side of \( c \), such that the tile assembly system \( T_x = (T, \sigma_x, \tau) \) is directed and:

| (a) \( B(\sigma_x[c]) = x \) and \( B(\alpha_x + (c + \vec{v})) = f(x) \) where \( \alpha_x \) is the terminal assembly of \( T_x \); and
| (b) \( T_x \) has at least one assembly sequence \( \alpha_x \) that assembles all of \( \alpha_{|\text{LHS}(c+i\vec{v})} \) without placing any tile of \( \alpha_{|\text{RHS}(c+i\vec{v})} \); and
| (c) for all positions \( z \in (\text{RHS}(c) \cap \text{LHS}(c + \vec{v})) \subseteq \mathbb{Z}^2 \), and for all \( x \) the set \( P_z \) of tile placements at position \( z \) in \( \alpha_x \) (from \( \vec{v} \) map cleanly to a gate (Definition 34).

Remark 34. Definition 33 and Lemma 36 below are not needed to prove our main result, but are included to show that any system satisfying Definition 33 can be “iterated” to compute layer-by-layer, similar to the sense in which tile-based counters in the literature compute layer-by-layer.

|Definition 35 (Computing an iterated n-bit function). The tile set \( T \) is said to layer-compute \( f^k \), i.e., \( k \) iterations of the Boolean function \( f : \{0, 1\}^n \rightarrow \{0, 1\}^n \), if:

| (a) \( T \) layer-computes \( f \) via Definition 33 and
| (b) \( T_x \)'s terminal assembly \( \alpha_x \), for each \( i \in \{0, 1, \ldots, k-1\} \), has \( B(\alpha_x[c+i\vec{v}]) = f^i(x) \).

|Lemma 36. Let \( T \) be a tile set that layer-computes the n-bit function \( f \) according to Definition 33. Then for any \( k \in \mathbb{N} \), \( T \) also computes \( f^k \) according to Definition 35.

|Proof. We give a simple proof by induction on iteration \( f^i \) for \( i \in \{0, 1, \ldots, k-1\} \). The intuition is to let \( y' = f^i(x) \in \{0, 1\}^n \), then use Definition 33 to compute \( f^i(y') \), and then translate the resulting assembly to a later layer to compute \( f^{i+1}(y') = f(f^i(y')) \).

For the base case, let \( i = 0 \). By Definition 33 the seed \( \sigma_x \) encodes \( x \in \{0, 1\}^n \) along \( c \) as \( B(\sigma_x[c]) = x \) and \( \sigma_x \) places no tiles in \( \text{RHS}(c) \subseteq \mathbb{Z}^2 \). Hence \( T \) computes \( f^0(x) = x \) according to Definition 35.

For the inductive case, let \( i > 0 \). Let \( \vec{a} = \alpha_0, \alpha_1, \ldots, \alpha_m \) be an assembly sequence of \( T_x \) such that, inductively, we assume that on the last assembly \( \alpha_m \) of \( \vec{a} \) the cut \( c + i \cdot \vec{v} \) encodes the bit sequence \( f^i(x) = B(\alpha_x[c + i \cdot \vec{v}]) \in \{0, 1\}^n \), and \( \alpha_m \) has no tiles in \( \text{RHS}(c + i \cdot \vec{v}) \), and no more tiles can stick in \( \text{LHS}(c + i \cdot \vec{v}) \). Next, consider the seed assembly \( \sigma_{y'} \) that encodes \( y' = f^i(x) \), and let \( \vec{a} = \sigma_{y'}, \alpha_1, \alpha_2, \ldots \) be an assembly sequence that satisfies Definition 33 and (c). For each \( k \in \{0, 1, \ldots, |\vec{a}| - 1\} \) let \( (t, z)_k \) be the tile that sticks (is attached) to assembly \( \alpha_k \) to give the next assembly \( \alpha_{k+1} \) in \( \vec{a} \). We make a new assembly sequence \( \vec{a}' \) that starts with the assembly \( \alpha_m \) (defined above), then stick the ‘translated tile’ \( (t, z + i \cdot \vec{v})_0 \), and then sticks \( (t, z + i \cdot \vec{v})_{1} \), and so on. In other words define \( \vec{a}' = \sigma_{m, 0} \rightarrow_{T} \alpha_{m, 1} \rightarrow_{T} \cdots \) by beginning with \( \alpha_m = \alpha_{m, 0} \) and in turn attaching the tiles \( (t, z + i \cdot \vec{v})_0, (t, z + i \cdot \vec{v})_{1}, \ldots \) in order. The assembly sequence \( \vec{a}' \) eventually contains an assembly that encodes \( f(y') = f^{i+1}(x) \) along the curve \( c + (i + 1) \cdot \vec{v} \) as \( f^{i+1}(x) = B(\alpha_x + (c + (i + 1) \cdot \vec{v})) \). This completes the induction. \( \square \)
5.3 Tile sets computing layer-by-layer are simulated by railway circuits

Lemma 37 (Railway circuits simulate layer-computing tile sets). Let $T$ be a tile set that layer-computes, via Definition 33, the Boolean function $f : \{0, 1\}^n \rightarrow \{0, 1\}^n$ for $n \geq 3$. Then there is a local railway circuit that computes $f$.

Proof. By Definition 33, let $\tau$ be the temperature, $c$ the glue curve, $\vec{v}$ the vector, and for each input $x \in \{0, 1\}^n$ let $\sigma_x$ be the seed assembly encoding $x$ and let $T_x = (T, \sigma_x, \tau)$. We will construct a $n$-wire local railway circuit from $T$.

For each $x$, let $\vec{\alpha}_x$ be the assembly sequence that satisfies Definition 33(a) and (b). By directedness, the choice of $\vec{\alpha}_x$ over other assembly sequences is inconsequential since all assembly sequences for $x$ compute the same output $f(x)$ for the layer. For any $z \in (\text{RHS}(c) \cap \text{LHS}(c + \vec{v})) \subseteq \mathbb{Z}$ and for all $x \in \{0, 1\}^n$, let $P_z$ denote the set of tile placements that appear at position $z$ in the set of assembly sequences $\bigcup_x(\vec{\alpha}_x)$. By Definition 33(c), $P_z$ maps cleanly to a gate, and we let $g_z$ denote that gate. Via Definition 30, there are $k_z \in \{0, 1, 2\}$ inputs and $k_z$ outputs to $g_z$ (i.e. fanin and fanout are equal to $k_z \leq 2$ for $g_z$). In the railway circuit for each gate $g_z$ we define a section $s_z$; there are $n$ inputs and $n$ outputs to the section, $k_z$ of those $n$ are fed through gate $g_z$ and the remaining $n - k_z$ are pass-through. In other words, the $n$-bit function computed by the section is defined by the extension $f_{g_z, 1}$ to $n$ bits of the function $f_{g_z}$ computed by gate $g_z$ on $k_z$ bits (see Section 2). The section is local since $k_z < n$.

It remains to wire the sections together (order them) so that they compute $f$. Choose any $x \in \{0, 1\}^n$, and let $z_0, z_1, \ldots, z_m$ be the sequence of positions in the order defined by the canonical assembly sequence $\vec{\alpha}_x$ as defined earlier in the proof. Let $x' \in \{0, 1\}^n$ where $x' \neq x$ and let $\vec{\alpha}'_x$ be the canonical assembly sequence for $x'$. By Definition 30 all assembly sequences share the same set of tile positions from $\mathbb{Z}^2$. We will define a new assembly sequence $\vec{\beta}'_x$, that has $\vec{\alpha}'_x$ as its first assembly, fills positions in the order $z_0, z_1, \ldots, z_m$ (we used for $\vec{\alpha}_x$) and produces the same terminal assembly as $\vec{\alpha}'_x$. For $z$ in $z_0, z_1, \ldots, z_m$, in the order given, let $p$ be tile placement at position $z$ in $\vec{\alpha}'_x$, choose any $\vec{\alpha}_x$ to the current assembly $\beta$ to get a new assembly $\beta'$. Since, the assembly $\alpha$ from $\vec{\alpha}_x$ that receives the placement at position $z$ to make $\alpha'$ (i.e. $\alpha \rightarrow \tau \alpha'$), has neighbouring positions providing sufficient tile sides (glues) for the placement at $z$, and since we are iterating through placement positions in the same order, the same is true of $\beta$. Hence $p$ can be placed on $\beta$ to give $\beta'$. Since $\vec{\alpha}_x, \vec{\alpha}'_x$ and $\vec{\beta}'_x$ all share the same set of positions, and since $\vec{\alpha}_x$ and $\vec{\beta}_x$ share the same tile placement at each shared position, the terminal assembly of $\vec{\alpha}_x$ and $\vec{\beta}_x$ are identical. Each position $z_0, z_1, \ldots, z_m$ defines a section $s_{z_0}, s_{z_1}, \ldots, s_{z_m}$, and we wire the sections in the order given. Since each section is a local railway circuit from $n$ bits to $n$ bits, their composition/concatenation is too. By Definition of $T$, $B(\alpha'_x \upharpoonright (c + \vec{v})) = f(x) \in \{0, 1\}^n$, and by construction the output of section $s_{z_m}$ is the same value $f(x)$.

Theorem 38. Let $n \in \{5, 6, \ldots\}$. There is no tile set $T$ that layer-computes, via Definition 33, an odd bijective $n$-bit function, or a quasi-bijective $n$-bit function, or a $2^n$ counter on $n$-bits.

Proof. By Lemma 37, there is a railway circuit $\mathcal{C}$ that layer-computes the same function, $f$, as $T$. By Theorem 28, $\mathcal{C}$ does not compute an odd bijection nor quasi-bijection, and hence (or by Theorem 1) $\mathcal{C}$ does not compute a $2^n$ counter.

5.4 Examples: application of our main self-assembly result

We illustrate our definitions by applying them to previously studied self-assembly systems.
Figure 5 Impossibility of a $2^n$ counter in IBCs. The lattice is rotated by 45°, relative to the standard $Z^2$ lattice. Theorem 2 shows that although there are 64 possible bit-strings that appear across the all cuts for all 6-bit systems, no 64-counter is possible in any one system. (a) First few layers of a 6-bit 63-counter for the 6-bit IBC tile model that appeared in [29]. The glue curve c, and its translations by multiples of vector $\vec{v}$ are shown in dashed green. (b) Layer for the same system showing tile positions $z_0, z_1, \ldots, z_8 \in Z^2$. Glues that encode 0/1 bits are shaded black, c-glues (that do not encode a bit) are shaded grey, for use in Definition 33. (c) Local railway circuit that computes a Boolean function according to Definition 33.

5.4.1 Example: IBC tile sets

Example 39 (IBC tile sets). For $n, \ell \in N$, with $n$ even, the directed $n$-bit $\ell$-layer IBC model is defined in Section SI-A-S1 of [29], and the 6-bit 1-layer IBC tile assembly model is defined graphically in Figure 1b of the same paper. Here it is illustrated in Figure 5. The IBC model is a restriction of the aTAM, hence we use the terminology from Section 5.1. A directed 6-bit IBC tile set $T$ is a set of 31 tile types with 4 tiles for each of positions $z_2, z_3, \ldots, z_6$ (mapping two input bits to two output bits), two tiles for each of positions $z_1$ and $z_7$ (mapping one input bit to one output bit), and one seam tile for each of positions $z_0$ and $z_8$ (mapping no input bits to no output bits – using $\epsilon$ glues in Definition 29). The set of tile types associated to a position is unique to that position, hence in an assembly all cuts for all 6-bit systems, no 64-counter is possible in any one system. (a) First few placements for position $z_1$, where $i \in \{0, 1, 2, \ldots, 8\}$, Figure 5(a) illustrates the 4 tile placements for position $z_2$.

More generally, for any even $n$, and $\ell \geq 1$, the $n$-bit, $\ell$-layer IBC model is defined in [29]. For the $\ell$-layer case, there are $2\ell$ tiles that map 1 input bit to 1 output bit, $(n - 1)\ell$ tiles that map 2 input bits to 2 output bits, and $2\ell$ tiles (or merely $\ell$ tiles if using a tube topology as in [29]) that map 0 input bits to 0 output bits.

Lemma 40. For any even $n \in \{2\ell' \mid n \in N\}$, $\ell \in N^+$, an $n$-bit IBC tile set $T$ layer-computes a Boolean function according to Definition 33.

Proof. IBCs (described in Example 39 illustrated in in Figure 5) satisfy Definition 33. In that definition let $\tau = 2$, let $c$ run along the seed $\sigma_x$ as shown in Figure 5, and let $\vec{v} = (0, \ell \sqrt{2})$ (assuming the x-axis is horizontal). Next, note that Definition 33 is satisfied by $c$, $\vec{v}$, $\sigma_x$ for each $x \in \{0, 1\}^n$, and the fact that the tile set outputs a bit sequence (that we define to
Figure 6 Impossibility and possibility of a $2^n$ zig-zig counter in the aTAM. (a) An aTAM tile set. Glues that encode 0/1 bits are shaded black, $\epsilon$-glues (that do not encode a bit) are shaded grey. Red denotes a glue type $w$ that can be either be a 0/1 encoding glue (assembles a $2^{n-1}$ counter – non-maximal), or an $\epsilon$-glue (assembles a $2^n$ counter – maximal). Each row has a unique set of tile types, indicated by tile colour. (b) Example growth starting from a seed assembly $\sigma_x$ that encodes the input $x = x_0x_1x_2 = 000$. (c1) A layer defined by the curve $c$ and its translation $c + \vec{v}$, both in green, and (c2) its simulation by a circuit. The circuit is not a railway circuit since gates $z_1$ and $z_2$ have fanout unequal to fanin; this can be seen by counting the number of wires that intersect each section border (3 wires on the green borders, 4 on the blue). The layer in (c1) and the circuit in (c2) define a maximal $2^n$-counter for $n = 3$, and the construction generalises to give a maximal $2^n$-counter for any $n \in \mathbb{N}$. Likewise, (d1) and (d2) define a $2^n$ counter by exploiting unequal fanin and fanout on some gates: in particular, in (d1) we’ve chosen the $w$ glue to be a 0/1-encoding glue and the resulting circuit in (d2) is not a railway circuit (the green section borders intersect 3 wires, the blue intersect 4 wires). Finally, in (e1) we define $c$ and $\vec{v}$ in a way that gives a $2^{n-1}$ counter (since setting $x_0 = 1$ enables counting on 3 bits, and setting $x_0 = 0$ does not help – forces the other bits to merely be copied). In this case the resulting circuit in (e2) is not a valid railway circuit (neither maximality nor application of our main result).

Thus, via Lemma 37, $n$-bit IBC tile sets are simulated by $n$-wire local railway circuits (Figure 5(c) shows an example). Hence by Theorem 38 we immediately get:

**Theorem 2.** For all $n \geq 3$, there is no $n$-bit IBC tile set that self-assembles a $2^n$ counter.

### 5.4.2 Example: zig-zig tile sets

Figure 6 illustrates a simple “zig-zig” counter system, where each column of tiles increments an $n$-bit binary input, for $n = 3$. By repeating the rows of green tiles (either by using the same tile types or hardcoding rows) the system generalises to arbitrary $n \in \mathbb{N}$.

Our main self-assembly result does not apply to zig-zig systems. Figure 6(c1), (d1) and (e1) show a number of choices for 0/1-encoding glues, versus $\epsilon$-glues, as well as two choices
for the curve $c$, and in the three cases our attempt to construct a railway circuit fails. The circuit (and tile types) exploit unequal gate fanin and gate fanout, hence some positions do not map cleanly to a gate hence Definition 33 does not apply. Furthermore, it can be seen that for any $n \in \mathbb{N}^+$ a maximal $2^n$ counter is achieved (shown for $n = 3$ in Figure 6).

### 5.4.3 Example: zig-zag tile sets

Figure 7 Zig-zag tile assembly system, similar to Evans [15]. (a) Schematic of a zig-zag system showing the seed $\sigma_x$ and arrows indicating tile attachment order. The first column of tiles (“zig”) implements a binary increment, using tile types similar to those in Figure 6(a), the second column of tiles (“zag”) copies a columns of input bits to the right. The choices for the curve $c$ (in green) and vector $\vec{v} = (2, 0)$ for Definition 33 are shown. (b) A layer consists of a single zig (tiles at positions $z_0, \ldots, z_5$) followed by a zag (tiles at position $z_6, \ldots, z_{11}$). Intuitively, because some glues output constant bits (e.g. $x_0 = y_0 = 1$) we are free to choose whether those glues should be 0/1-encoding glues (black), and $\epsilon$-glues (grey), in (b) we have all glues be 0/1-encoding which leads to a valid railway circuit in (c) that simulates the tile layer in (b). Specifically, in (c) all gates having fanin and fanout that is equal; in other words the functions from one green/blue cut to the next green/blue cut are all from $n$ bits to $n$ bits. Moreover, no gate spans all 6 wires hence the railway circuit is local. Hence our main theorem applies that this system does not implement a $2^n$ counter on $n = 6$ bits (it does however, implement a $2^{n-1}$-counter on $n = 6$ bits). (d) If we instead assume that $x_0, y_0$ are $\epsilon$-glues, we get a maximal $2^n$ counter (but on only $n = 5$ bits). In (e) the resulting circuit is not a railway circuit since some gates $z_0, z_4, z_6, z_{10}$ have unequal fanin and fanout. Unequal fanin and fanout means that the function from blue/green cut to blue/green cut are not all on a fixed number $n$ bits, hence our techniques do not apply.

Figure 7(a) illustrates an aTAM schematic of a “zig-zag” counter system that was implemented experimentally in [15]. The system has alternating increment (“zig”) and copy (“zag”) columns. The increment columns use similar tiles to those shown in Figure 6(a).

If we fix $n$ (e.g. for Figure 6, let $n = 6$), and vary our interpretation of the glues as either
0/1-encoding or $\epsilon$-glues, the counter can be seen to implement a non-maximal $2^{n-1}$ counter on $n$ bits, or a maximal $2^n$ counter on $n-1$ bits.

Specifically, within each zig-zag layer, Figure 7(b) interprets glue positions shown in black (e.g. $x_0$ and $y_0$) as encoding a bit, and in this case the system meets Definition 33 and via the proof of Lemma 37 we get the railway circuit shown in Figure 7(c). Hence, with that glue interpretation a $2^n$ counter is impossible (Theorem 38). Further intuition be obtained due from the tile set design: in Figure 6(a) the bit $x_0 = y_0$ and is always 1, and an analysis of the tile set shows that we get a $2^{n-1}$-counter.

If we instead, use the interpretation in Figure 7(d) interprets several of the glue positions (e.g. $x_0$ and $y_0$) as not encoding a bit, and instead being $\epsilon$-glues. In this case our attempt to apply Definition 33 fails as some tile positions map to Boolean gates with fanin unequal to fanout; see for example gates $z_0, z_4, z_6, z_{10}$ in Figure 7(e). Hence our techniques do not apply. An analysis of the tile set shows that we get a maximal counter (but on one fewer bit that the sub-maximal counter above). This example shows that a system that sticks to our formalism, except for the fanin/fanout criteria, may exhibit sufficient expressive capabilities to achieve a maximal counter.

References

1 Leonard Adleman, Qi Cheng, Ashish Goel, and Ming-Deh Huang. Running time and program size for self-assembled squares. In STOC: Proceedings of the 33rd Annual ACM Symposium on Theory of Computing, pages 740–748, Hersonissos, Greece, 2001. doi:http://doi.acm.org/10.1145/380752.380881.

2 Robert D Barish, Paul W K Rothemund, and Erik Winfree. Two computational primitives for algorithmic self-assembly: Copying and counting. Nano letters, 5(12):2586–2592, 2005.

3 Robert D Barish, Rebecca Schulman, Paul W K Rothemund, and Erik Winfree. An information-bearing seed for nucleating algorithmic self-assembly. Proceedings of the National Academy of Sciences, 106(15):6054–6059, 2009.

4 F. Becker, Ivan Rapaport, and E. Rémila. Self-assembling classes of shapes with a minimum number of tiles, and in optimal time. LNCS, 4337:45–56, 01 2006.

5 François Bergeron, Gilbert Labelle, and Pierre Leroux. Combinatorial Species and Tree-like Structures. Encyclopedia of Mathematics and its Applications. Cambridge University Press, 1997. doi:10.1017/CBO9781107325913.

6 Tim Boykett, Jarkko Kari, and Ville Salo. Strongly universal reversible gate sets. In Reversible Computation - 8th International Conference, RC 2016, Bologna, Italy, July 7-8, 2016, Proceedings, pages 239–254, 2016. URL: https://doi.org/10.1007/978-3-319-40578-0_18

7 Tim Boykett, Jarkko Kari, and Ville Salo. Strongly universal reversible gate sets. In International Conference on Reversible Computation, pages 239–254. Springer, 2016.

8 Qi Cheng, Ashish Goel, and Pablo Moisset de Espanés. Optimal self-assembly of counters at temperature two. In Proceedings of the First Conference on Foundations of Nanoscience: Self-assembled Architectures and Devices, 2004.

9 Matthew Cook, Paul W. K. Rothemund, and Erik Winfree. Self-assembled circuit patterns. In Jungheui Chen and John H. Reif, editors, DNA Computing, 9th International Workshop on DNA Based Computers, DNA9, Madison, WI, USA, June 1-3, 2003, revised Papers, volume 2943 of Lecture Notes in Computer Science, pages 91–107. Springer, 2003. URL: https://doi.org/10.1007/3-540-24628-2_11

10 Erik D. Demaine, Matthew J. Patitz, Trent A. Rogers, Robert T. Schweller, Scott M. Summers, and Damien Woods. The two-handed tile assembly model is not intrinsically universal. In ICALP: Proceedings of the 40th International Colloquium on Automata, Languages, and
11 David Doty. Theory of algorithmic self-assembly. *Communications of the ACM*, 55(12):78–88, 2012.

12 David Doty, Jack H. Lutz, Matthew J. Patitz, Scott M. Summers, and Damien Woods. Intrinsic universality in self-assembly. In *STACS: Proceedings of the 27th International Symposium on Theoretical Aspects of Computer Science*, pages 275–286, 2009. Arxiv preprint: [arXiv:1001.0208](http://arxiv.org/abs/1001.0208).

13 David Doty, Matthew J. Patitz, Dustin Reishus, Robert T. Schweller, and Scott M. Summers. Strong fault-tolerance for self-assembly with fuzzy temperature. In *FOCS 2010: Proceedings of the 51st Annual IEEE Symposium on Foundations of Computer Science*, pages 417–426. IEEE, 2010.

14 David Doty, Trent A. Rogers, David Soloveichik, Chris Thachuk, and Damien Woods. Thermodynamic binding networks. In *DNA 2017: Proceedings of the 23rd International Meeting on DNA Computing and Molecular Programming*, volume 10467 of *LNCS*, pages 249–266, 2017. Arxiv preprint: [arXiv:1709.07922](http://arxiv.org/abs/1709.07922).

15 Constantine Evans. *Crystals that count! Physical principles and experimental investigations of DNA tile self-assembly*. PhD thesis, Caltech, 2014.

16 Philippe Flajolet and Robert Sedgewick. *Analytic Combinatorics*. Cambridge University Press, USA, 1 edition, 2009.

17 Bin Fu, Matthew J Patitz, Robert T Schweller, and Robert Sheline. Self-assembly with geometric tiles. In *ICALP: International Colloquium on Automata, Languages, and Programming*, pages 714–725. Springer, 2012.

18 André Joyal. Une théorie combinatoire des séries formelles. 1981.

19 Pierre-Étienne Meunier, Damien Regnault, and Damien Woods. The program-size complexity of self-assembled paths. In *STOC: Proceedings of the 52nd Annual ACM SIGACT Symposium on Theory of Computing*. ACM, 2020. Accepted. Arxiv preprint: [arXiv:2002.04012](http://arxiv.org/abs/2002.04012).

20 Matthew J. Patitz. An introduction to tile-based self-assembly and a survey of recent results. *Natural Computing*, 13(2):195–224, 2014.

21 Matthew J Patitz, Robert Schweller, Trent A Rogers, Scott M Summers, and Andrew Winslow. Resiliency to multiple nucleation in temperature-1 self-assembly. *Natural Computing*, 17(1):31–46, 2018.

22 Matthew J Patitz, Robert T Schweller, and Scott M Summers. Exact shapes and Turing universality at temperature 1 with a single negative glue. In *International Conference on DNA-Computing and Molecular Programming*, pages 175–189. Springer, 2011.

23 Paul W K Rothemund and Erik Winfree. The program-size complexity of self-assembled squares. In *STOC: Proceedings of the thirty-second annual ACM symposium on Theory of computing*, pages 459–468. ACM, 2000.

24 Joseph J Rotman. *An introduction to the theory of groups*, volume 148. Springer Science & Business Media, 2012.

25 David Soloveichik and Erik Winfree. Complexity of self-assembled shapes. *SIAM Journal on Computing*, 36(6):1544–1569, 2007.

26 Tommaso Toffoli. Reversible computing. In *Automata, Languages and Programming, 7th Colloquium, Noordwijkerhout, The Netherlands, July 14-18, 1980, Proceedings*, pages 632–644, 1980. URL: [https://doi.org/10.1007/3-540-10003-2_104](https://doi.org/10.1007/3-540-10003-2_104), doi:10.1007/3-540-10003-2_104.

27 Erik Winfree. *Algorithmic Self-Assembly of DNA*. PhD thesis, California Institute of Technology, June 1998.

28 Damien Woods, Ho-Lin Chen, Scott Goodfriend, Nadine Dabby, Erik Winfree, and Peng Yin. Active self-assembly of algorithmic shapes and patterns in polylogarithmic time. In *ITCS: Proceedings of the 4th conference on Innovations in Theoretical Computer Science*, pages 353–354. ACM, 2013. Arxiv preprint: [arXiv:1301.2626](http://arxiv.org/abs/1301.2626) [cs.DS], doi:10.1145/2422436.2422476.
Limitations on counting in Boolean circuits and self-assembly

29 Damien Woods, David Doty, Cameron Myhrvold, Joy Hui, Felix Zhou, Peng Yin, and Erik Winfree. Diverse and robust molecular algorithms using reprogrammable DNA self-assembly. *Nature*, 567(7748):366–372, 2019.

30 Siyao Xu. Reversible logic synthesis with minimal usage of ancilla bits. *CoRR*, abs/1506.03777, 2015. URL: http://arxiv.org/abs/1506.03777, arXiv:1506.03777.
A Parity of a bijection

For the sake of completeness we prove Theorems 20 and 25 from Section 3.

\textbf{Theorem 20 (Parity of a bijection).} Let $f \in \mathfrak{S}_m$. The parity of the number of swaps used in any swap-decomposition of $f$ does not depend on the decomposition. If $f = \tau_{p-1} \circ \cdots \circ \tau_0$ and $f = \tau'_{p-1} \circ \cdots \circ \tau'_0$ then $p \equiv p'$ [2]. Hence we say that the function $f$ is even if $p$ is even and odd otherwise.

\textbf{Theorem 25 (Parity of $k$-cycle).} A $k$-cycle $\rho$ has the parity of the number $k - 1$. It means that $\rho$ is odd iff $k - 1$ is odd and $\rho$ is even iff $k - 1$ is even.

These are known group theoretical results and the literature offers a lot of different proofs for them [21]. The following lemma is crucial:

\textbf{Lemma 41 (Sign of a bijection).} Let $f \in \mathfrak{S}_m$. Define $\epsilon : \mathfrak{S}_m \to \{-1,1\}$, the sign of $f$, to be:

$$
\epsilon(f) = \prod_{0 \leq j < i < m} (j - i) \prod_{0 \leq j < i < m} (f(j) - f(i))
$$

We have:
1. $\epsilon(f) = 1$ or $\epsilon(f) = -1$
2. Let $g \in \mathfrak{S}_m$, then $\epsilon(f \circ g) = \epsilon(f)\epsilon(g)$
3. Let $\tau$ be a swap then $\epsilon(\tau) = -1$

\textbf{Proof.} 1. Because $f$ is a bijection, the sets $\{\{j, i\} \mid 0 < j < i < m\}$ and $\{\{f(j), f(i)\} \mid 0 < j < i < m\}$ are the same. However, the sets of ordered pairs $\{(j, i) \mid 0 < j < i < m\}$, $\{(f(j), f(i)) \mid 0 < j < i < m\}$ might differ when $f(j) > f(i)$, i.e when $f$ reverses the order of $(j, i)$. Hence $\epsilon(f) = 1$ if $f$ reverses the order an even number of times and $\epsilon(f) = -1$ if $f$ reverses the order an odd number of times.

2. We have

$$
\epsilon(f \circ g) = \frac{\prod_{0 \leq j < i < m} (j - i)}{\prod_{0 \leq j < i < m} (f \circ g(j) - f \circ g(i))} = \frac{\prod_{0 \leq j < i < m} (j - i)}{\prod_{0 \leq j < i < m} (g(j) - g(i))} \prod_{0 \leq j < i < m} (f \circ g(j) - f \circ g(i))
$$

But because $g$ is a bijection, we have

$$
\prod_{0 \leq j < i < m} (g(j) - g(i)) = \prod_{0 \leq j < i < m} (f(j) - g(i))
$$

So we have:

$$
\frac{\prod_{0 \leq j < i < m} (j - i)}{\prod_{0 \leq j < i < m} (f \circ g(j) - f \circ g(i))} = \prod_{0 \leq j < i < m} (f(j) - f(i))
$$

In other words: $\epsilon(f \circ g) = \epsilon(f) \circ \epsilon(g)$.

3. Let’s consider a swap $\tau$ which swaps $i_0$ and $i_1$ with $i_0 < i_1$. We have $\frac{i_1 - i_0}{i_1 - i_0} = -1$. We just need to focus on un-ordered pairs that features $i_0$ or $i_1$ since $\tau$ leaves all other elements unchanged. Now, three cases:

a. Let’s consider $i_2$ such that $i_2 < i_0 < i_1$. We have $\frac{i_2 - i_0}{i_2 - i_0} = 1$. We also have $\frac{i_2 - i_1}{i_2 - i_1} = 1$.

---

9 See this thread:
https://math.stackexchange.com/questions/46403/alternative-proof-that-the-parity-of-permutation-is-well-defined
b. Let’s consider \( i_2 \) such that \( i_0 < i_2 < i_1 \). We have \( \frac{i_2 - i_0}{i_1 - i_2} = -1 \) which compensates.

c. Let’s consider \( i_2 \) such that \( i_0 < i_1 < i_2 \). We have \( \frac{i_2 - i_0}{i_1 - i_2} = 1 \). We also have \( \frac{i_2 - i_0}{i_0 - i_2} = 1 \).

In all those cases, the sign is not affected: either it is compensated either it is positive.

The only part of \( \epsilon(f) \) with a negative sign which is not compensated is \( \frac{i_0 - i_1}{i_1 - i_2} = -1 \). Hence \( \epsilon(\tau) = -1 \). We gave the proof for \( i_0 < i_1 \), the argument is symmetric and can be adapted to the case \( i_1 < i_0 \).

Remark 42. Without saying it we proved that \( \epsilon : \mathbb{S}_m \rightarrow \{-1, 1\} \) is a group morphism between groups \((\mathbb{S}_m, \circ)\) and \((\{-1, 1\}, \times)\). In fact, it is the only non-trivial one (i.e. not the identity), see [24].

Theorem 20 becomes a piece of cake:

**Theorem 20 (Parity of a bijection).** Let \( f \in \mathbb{S}_m \). The parity of the number of swaps used in any swap-decomposition of \( f \) does not depend on the decomposition. If \( f = \tau_{p-1} \circ \cdots \circ \tau_0 \) and \( f = \tau_{p'-1}' \circ \cdots \circ \tau_0' \) then \( p \equiv p' \) [2]. Hence we say that the function \( f \) is even if \( p \) is even and odd otherwise.

**Proof.** Let \( f \in \mathbb{S}_m \) and \( f = \tau_{p-1} \circ \cdots \circ \tau_0 \) and \( f = \tau_{p'-1}' \circ \cdots \circ \tau_0' \). By Lemma 41 we have:

\[
\epsilon(f) = \epsilon(\tau_{p-1} \circ \cdots \circ \tau_0) = \epsilon(\tau_{p-1}) \times \cdots \times \epsilon(\tau_0) = (-1)^p
\]

\[
\epsilon(f) = \epsilon(\tau_{p'-1}' \circ \cdots \circ \tau_0') = \epsilon(\tau_{p'-1}') \times \cdots \times \epsilon(\tau_0') = (-1)^{p'}
\]

Hence we must have \( p \equiv p' \) [2].

Remark 43. The bijection \( f \) is even if \( \epsilon(f) = 1 \) and odd if \( \epsilon(f) = -1 \).

Now we compute the parity of a \( k \)-cycle:

**Definition 24 (k-cycle).** For \( k \geq 1 \), a \( k \)-cycle \( \rho \in \mathbb{S}_m \) is a bijection such that there exists distinct \( x_0, x_1, \ldots, x_{k-1} \in \{0, \ldots, m-1\} \) such that \( \rho(x_0) = x_1, \rho(x_1) = x_2, \ldots, \rho(x_{k-1}) = x_0 \) and \( \forall x \not\in \{x_0, \ldots, x_{k-1}\}, \rho(x) = x \).

**Theorem 25 (Parity of k-cycle).** A \( k \)-cycle \( \rho \) has the parity of the number \( k - 1 \). It means that \( \rho \) is odd if \( k - 1 \) is odd and \( \rho \) is even if \( k - 1 \) is even.

**Proof.** Let \( \rho \) be a \( k \)-cycle acting on \( x_0, x_1, \ldots, x_{k-1} \). One can decompose \( \rho \) is \( k - 1 \) transposition: \( \rho = \tau_{x_0, x_1} \circ \tau_{x_1, x_2} \circ \cdots \circ \tau_{x_{k-2}, x_{k-1}} \). Where \( \tau_{x_i, x_j} \) swaps \( i \) and \( j \). Hence \( \epsilon(\rho) = (-1)^{k-1} \) and \( \rho \) is even if \( k - 1 \) is even.