The Simplified Toffoli Gate Implementation by Margolus is Optimal

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Abstract

Unitary operations are expressed in the quantum circuit model as a finite sequence of elementary gates, such as controlled-not gates and single qubit gates. We prove that the simplified Toffoli gate by Margolus, which coincides with the Toffoli gate up to a single change of sign, cannot be realized with less than three controlled-not gates. If the circuit is implemented with three controlled-not gates, then at least four additional single qubit gates are necessary. This proves that the implementation suggested by Margolus is optimal.

1 Introduction

The simplified Toffoli gate realizes the unitary map $M : \mathbb{C}^8 \rightarrow \mathbb{C}^8$ given by

- $|00\rangle \otimes |\phi\rangle \mapsto |00\rangle \otimes |\phi\rangle,$
- $|01\rangle \otimes |\phi\rangle \mapsto |01\rangle \otimes |\phi\rangle,$
- $|10\rangle \otimes |\phi\rangle \mapsto |10\rangle \otimes Z|\phi\rangle,$
- $|11\rangle \otimes |\phi\rangle \mapsto |11\rangle \otimes X|\phi\rangle,$

where $|\phi\rangle$ is an arbitrary state in $\mathbb{C}^2$, $X$ denotes the not gate, and $Z$ a phase gate,

$$X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \quad Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}. \quad (1)$$

The unitary map $M$ coincides with the Toffoli gate $[1]$ on all vectors of the standard basis, except that it maps the state $|101\rangle$ to $-|101\rangle$ instead of $|101\rangle$; this strong resemblance explains the name.

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The simplified Toffoli gate has an elegant implementation [1], which is due to Margolus [4,2], see also [1,3]. It merely requires three controlled-not gates and four single qubit gates:

\[
\begin{align*}
\begin{array}{c}
\bullet \\
\bullet
\end{array} 
& \cong 
\begin{array}{c}
Y \\
Z
\end{array} 
= 
\begin{array}{c}
G \\
G \\
G^\dagger \\
G^\dagger
\end{array} \\
\begin{array}{c}
\bullet \\
\bullet
\end{array}
\end{align*}
\]

where

\[
Y = ZX = \begin{pmatrix} 0 & 1 \\ -1 & 0 \end{pmatrix}, \quad G = \begin{pmatrix} \cos(\frac{1}{8}\pi) & -\sin(\frac{1}{8}\pi) \\ \sin(\frac{1}{8}\pi) & \cos(\frac{1}{8}\pi) \end{pmatrix}.
\]

(2)

The congruence sign indicates equivalence up to a multiplication with a diagonal matrix of phase factors. There are some alternatives to \( M \) that differ in some other basis state by a sign, but that is not an essential change.

The simplified Toffoli gate cannot substitute for the Toffoli gate in general, because phase factors are important in true quantum algorithms. However, if the Toffoli gates appear in pairs, then it is possible to adapt the circuit structure to take advantage of the simplified Toffoli gate [1]. The saving are quite substantial in this case, because the best implementations of the Toffoli gate known to date need fourteen controlled-not and single qubit gates.

Our main result expresses our appreciation of the beautiful structure of the quantum circuit (2). We prove that the circuit is optimal in the following sense:

**Theorem M** Suppose that the simplified Toffoli gate \( M \) is realized by a sequence of controlled-not and single qubit gates. Any such sequence contains at least three controlled-not gates. If it contains three controlled-not gates, then at least four single qubit gates are needed.

Our proof reveals that the elegant structure of the circuit (2) is not an arbitrary artifact. Indeed, any optimal quantum circuit realizing \( M \) is essentially of this form, except that the single qubit gates are possibly different.

We followed the seminal paper [1] in our choice of the universal set of gates, because this has been adopted in several textbooks as well. Choosing controlled-not gates and single qubit gates is somewhat arbitrary, but similar arguments can be carried out for other universal sets of quantum gates. The main reason for our choice is that the number of controlled-not and single
qubit gates constitute the prevailing measure of complexity currently used in Computer Science. This paper is part of a larger program, where we try to gain a better understanding of basic quantum circuit structures.

Notations. In addition to the gates introduced in (1) and (3), we use
\[
H = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix}
\]
to denote the Hadamard gate. The state \(|0_x\rangle = H|0\rangle\) denotes the eigenstate of \(X\) with eigenvalue +1. The most significant qubit is represented by the topmost wire in the quantum circuit notation, and the least significant qubit by the lowest wire. We denote by \(\mathbb{C}\) the field of complex numbers, and by \(\mathbb{R}\) the field of real numbers.

2 Review of Previous Work

We review in this section some useful lemmas, all of which are proved in [5]. We will use these results in the proof of Theorem M. Recall that it is possible to switch the control and the target qubit of a controlled-not gate by conjugation with Hadamard matrices \(H\):

Due to this important fact, it suffices to consider controlled-not gates where the control is on a higher significant qubit that the target qubit when we write down the general form of a circuit.

**Lemma 1** Let \(|\psi\rangle, |\phi\rangle\) be nonzero elements of \(\mathbb{C}^2\). The input \(|\psi\rangle \otimes |\phi\rangle\) to a controlled-\(U\) gate will produce an entangled output state if and only if \(|\phi\rangle\) is not an eigenvector of \(U\) and \(|\psi\rangle = a|0\rangle + b|1\rangle\) with \(a, b \neq 0\).

**Lemma 2** Assume that \(|\phi\rangle\) is an eigenvector of a unitary \(2 \times 2\) matrix \(U\) with eigenvalue \(\lambda_{\phi}\). Let \(|\psi\rangle\) denote a state in \(\mathbb{C}^2\). If we input \(|\psi\rangle \otimes |\phi\rangle\) to the controlled-\(U\) gate, then the output is of the form \(\text{diag}(1, \lambda_{\phi})|\psi\rangle \otimes |\phi\rangle\). In particular, the output is not entangled.
A controlled-$U$ gate can be realized with two controlled-not gates and several single qubit gates, as follows:

\[ U = A_1 A_2 A_3 \]

The following two lemmas describe some constraints on the gates $A_1, A_2,$ and $A_3$. We call a single qubit gate sparse if it is realized by a diagonal or antidiagonal $2 \times 2$ matrix.

**Lemma 3** If the matrix $A_1$ is sparse, then $A_2, A_3$ are sparse as well.

**Lemma 4** Suppose that $U$ is not a multiple of the identity matrix. If $A_1$ in the circuit (5) is not sparse, then $A_2, A_3$ are not sparse either.

## 3 Proof of Theorem M

We proceed to show that three controlled-not gates are necessary and sufficient in any realization of unitary map $M$ by a sequence of controlled-not and single qubit gates. We first prove that at least two controlled-not operations act on the last qubit:

**Lemma 5** Suppose there are some interactions between the top two qubits, but only one controlled-not interaction between the two control qubits and the target bit. The circuit cannot realize the Margolus map $M$.

**Proof.** Any such circuit can be represented in the form

\[ B_1 \quad C_1 \quad B_2 \quad C_2 \]

Let $|0_x\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$, and denote by $|\varphi\rangle$ an arbitrary state in $\mathbb{C}^4$. If we input $|\varphi\rangle \otimes C_1^0|0_x\rangle$ to the above quantum circuit, then the least significant qubit of the output state is not entangled with the remaining two qubits, regardless of the nature of input state $|\varphi\rangle$.

However, if we choose the input $|00\rangle \otimes |\phi\rangle + |10\rangle \otimes |\phi\rangle + |11\rangle \otimes |\phi\rangle$, then the output of $M$ is $|00\rangle \otimes |\phi\rangle + |10\rangle \otimes Z|\phi\rangle + |11\rangle \otimes X|\phi\rangle$. Note that the
target qubit is entangled with the other two qubits, since $|\phi\rangle$ cannot be an eigenvector of $X$ and $Z$ at the same time. Contradiction. □

**Corollary 6** The target qubit is affected by at least two controlled-not operations.

**Two Controlled-Not Gates.** Assume there are only two controlled-not gates in the circuit. Taking Corollary 6 and the identity (4) into account, we may assume that both controlled-not gates operate on the target bit. The control qubits of the two gates have to be different, for otherwise it would not be possible to entangle all input qubits with the output qubit.

Since $M = M^\dagger$, we do not need to concern ourselves with the order the two controlled-not gate in such a circuit. Therefore, we may assume that the circuit is of the form

\[
\begin{array}{c}
B_1 \quad B_2 \\
C_1 \quad C_2 \\
\end{array}
\begin{array}{c}
A_1 \\
A_2 \\
\end{array}
\]  \quad (7)

**Lemma 7** The circuit (7) cannot implement the simplified Toffoli gate.

*Proof.* When the top qubit is $|0\rangle$, then the circuit (7) can still entangle the least significant two qubits, contradicting the behavior of $M$. □.

**Corollary 8** At least three controlled-not gates are necessary in an implementation of the simplified Toffoli gate $M$ by a sequence of controlled-not and single qubit gates.

**Three Controlled-Not Gates.** The remaining argument proceeds by considering all possible configurations of the three controlled-not gates. Initially, we allow an arbitrary number of single qubit operations. Thus, we may assume that the target qubit has lesser significance than the control qubit by applying (4), so that we have to consider $\binom{3}{2}^3 = 27$ configurations of controlled-not gates. We use the pictogram

```plaintext
+---+---+---
|   |   |   |
+---+---+---
|   |   |   |
+---+---+---
|   |   |   |
+---+---+---
```
as a shorthand for a general quantum circuit of the form \( \mathcal{R} \) that contains in addition to the specified controlled-not configuration all potential single qubit gates. We distinguish three different cases that we record here for the orientation of the reader:

- Case 1
- Case 2
- Case 3

The remaining configurations

are excluded because they are ruled out by Corollary \( \mathcal{R} \) or lack the capability to entangle all three qubits, hence cannot implement \( M \).

It turns out that only a single configuration allows to realize the simplified Toffoli gate \( M \). In most cases, we are able to exclude circuit structures because they exhibit entanglement properties that are inconsistent with the behavior of the simplified Toffoli gate \( M \). We record the following trivial observation:

**Lemma 9** Suppose that two systems \( A \) and \( B \) of qubits are entangled. If the remaining gate operations affect the systems \( A \) and \( B \) separately, then \( A \) and \( B \) remain entangled.

**Proof.** Seeking a contradiction, we assume that the resulting output state is not entangled, i.e., is of the form \( |\phi_A\rangle \otimes |\phi_B\rangle \). The gate operations leading to this output state can be written in the form \( U_A \otimes U_B \), since the operations affect the systems separately. This would imply that the input state \( U_A^\dagger |\phi_A\rangle \otimes U_B^\dagger |\phi_B\rangle \) was separable as well, in contradiction to the assumption. \( \square \)

**Case 1.** The circuits configuration are in this case characterized by the fact that exactly two controlled-not gates act on the target qubit of \( M \), and they are controlled from different qubits. The third controlled-not gate is between the two most significant qubits. It turns out that none of these circuits can implement \( M \), even if we allow single qubit gates on all possible positions.

**Lemma 10** A circuit with one of the configurations

would implement \( M \). In most cases, we are able to exclude circuit structures because they exhibit entanglement properties that are inconsistent with the behavior of the simplified Toffoli gate \( M \). We record the following trivial observation:

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cannot implement the simplified Toffoli gate $M$.

Proof. The most general circuit corresponding to the first pictogram is given by

$$\begin{array}{cccccccc}
B_1 & & A_1 & & A_2 & & A_3 \\
& & B_2 & & B_3 & & \\
C_1 & & & & C_2 & & C_3
\end{array}$$

(8)

Seeking a contradiction, we assume that $A_1$ is not sparse. If we provide an input $|0\rangle \otimes |\phi\rangle \otimes C_1^\dagger |0\rangle$, then the top two quantum bits could possibly get entangled by Lemma 1 and if so, these two qubits would remain entangled by Lemma 9 contradicting the behavior of $M$. Hence, $A_1$ must be sparse.

By the same token, $A_2$ has to be sparse, because otherwise we can find an input state of the form $|0\rangle \otimes |\phi\rangle$, such that the most and least significant qubit get entangled, contradicting the behavior of $M$. As a consequence, $A_3$ is sparse as well.

Therefore, the behavior of the circuit (8) on input of $|0\rangle \otimes |\phi\rangle$, $|\phi\rangle \in C^4$, can be simulated by a circuit of the form

$$\begin{array}{cccccccc}
A_3 & A_2 & A_1 \\
B_1 & & B_2 & & B_3 \\
& & C_1 & & C_2 & & C_3
\end{array}$$

(9)

where the values of $k, \ell \in \{0, 1\}$ depend on whether $A_1$ and $A_2$ are diagonal or antidiagonal. It is obvious from this circuit that we can choose a separable state $|\phi\rangle$ such that the two least significant qubits get entangled, even though the topmost qubit is in the state $|0\rangle$. This contradicts the behavior of $M$, thus a circuit of the form (9) cannot realize $M$.

In the same way, it is straightforward to see that neither the second nor the third pictogram can realize $M$.

Finally, the last three pictograms represent the inverse circuits of the first three, so none of them can realize $M$ since $M$ is self-inverse. □

Case 2. The circuit configurations of the second case are characterized by the fact that exactly two controlled-not gates act on the target qubit, and both are controlled from the same qubit. We distinguish in our discussion whether they are controlled by the middle qubit (Case 2.1), or by the most significant qubit (Case 2.2).
Case 2.1. This case treats the configurations of controlled-not gates that have the pictorial representation

\[ \text{Diagram} \]

Lemma 11 A circuit with one of the controlled-not configurations

\[ \text{Diagram} \]

cannot implement the simplified Toffoli gate $M$.

Proof. The most general circuit corresponding to the first pictogram is given by

\[ (10) \]

The second pictogram is covered by taking the inverse of the above circuit, hence does not need to be treated separately. If we input $|0\rangle \otimes B_1 \otimes |0\rangle \otimes |0\rangle$, then the circuit will produce an entangled output state by Lemmas 1 and 9 if $A_1$ is not sparse. Hence, $A_1$ has to be sparse, and consequently $A_2$ as well.

If we take the input state $|0\rangle \otimes |\varphi\rangle$, with $|\varphi\rangle \in \mathbb{C}^4$, then the circuit (10) has to act identically on $|\varphi\rangle$. Consequently, we obtain the circuit identity

\[ (11) \]

On the other hand, we can derive from the input $|1\rangle \otimes |\varphi\rangle$ the circuit identity

\[ (12) \]

Combining the previous two circuit identities, we obtain

\[ \text{Diagram} \]
which is absurd. Therefore, a circuit of the form (11) cannot implement $M$. 

**Lemma 12** A circuit with controlled-not configuration

\[ \begin{array}{c}
\text{1} \\
\text{2} \\
\text{3} \\
\text{4}
\end{array} \]

cannot implement the simplified Toffoli gate $M$.

**Proof.** The most general circuit corresponding to the configuration depicted in the last pictogram is given by

\[
\begin{array}{cccccccc}
B_1 & A_1 & B_2 & A_2 & B_3 & B_4 \\
C_1 & & B_2 & & B_3 & & B_4 \\
& C_2 & & & C_3 & & \\
& & & X & & & \\
\end{array}
\]  

(13)

Once again, we want to show that this circuit structure cannot implement $M$. We note that $A_1$ and $A_2$ have to be sparse (for otherwise it would be possible to find a state $|\varphi\rangle \in \mathbb{C}^4$ such that $|0\rangle \otimes |\varphi\rangle$ leads to an entangled output state, arguing as in the previous case). The circuit (13) has to act as the identity on an input state $|0\rangle \otimes |\varphi\rangle$. Thus, we obtain the circuit identity

\[
\begin{array}{cccccccc}
B_1 & A_1 & B_2 & A_2 & B_3 & B_4 \\
C_1 & & B_2 & & B_3 & & B_4 \\
& C_2 & & & C_3 & & \\
& & & X & & & \\
\end{array} = I
\]  

(14)

Similarly, the input $|1\rangle \otimes |\phi\rangle \otimes |\psi\rangle$ leads to the circuit identity

\[
\begin{array}{cccccccc}
B_1 & & B_3 X^l B_2 & & B_4 \\
C_1 & & B_2 & & B_3 & & B_4 \\
& C_2 & & & C_3 & & \\
& & & Y & & & \\
\end{array} = YZ
\]  

(15)

From circuits (14) and (15), we have,

\[
\begin{array}{cccccccc}
B_1 & & B_3 X B_3^l & & B_4^l \\
C_1 & & B_3 & & B_3 & & B_4^l \\
& C_2 & & & C_3 & & \\
& & & Y & & & \\
\end{array} = YZ
\]  

(16)
Moving $Z$ to the left-hand side of the equation, we have

\[
\begin{array}{c}
\begin{array}{c}
B_1 \\
C_1 \\
\end{array}
\end{array}
\begin{array}{c}
B_3XB_3^\\dagger \\
\end{array}
\begin{array}{c}
B_4^\\dagger \\
\end{array}
\begin{array}{c}
ZC_1^\\dagger \\
\end{array}
= Y
\end{array}
\tag{17}
\]

Now for any input state $|\phi\rangle \otimes (C_1)^{\dagger}|0_x\rangle$, such that $|\phi\rangle = a|0\rangle + b|1\rangle$ is in superposition, $a, b \neq 0$, the circuit on the left hand side does not entangle the two qubits. Therefore, by Lemma 1 we know that $(C_1)^{\dagger}|0_x\rangle$ has to be an eigenvector of $Y$. Furthermore, by Lemma 2 we have

\[
B_4^\\dagger B_3^\\dagger XB_3B_1 = \text{diag}(1, y_0),
\tag{18}
\]

where $y_0$ is one the eigenvalues of $Y$, i.e., $y_0 = (-i)$ or $i$. Taking the trace on both sides, we get a contradiction. \square

Case 2.2. We now treat the configurations that have the pictorial representation

\[
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\end{array}
\]

Changing the role of the two most significant qubits, we arrive at simplified Toffoli gate $M'$ that is implemented by

\[
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\end{array}
Y 
Z
\]

Thus, it is equivalent to use the circuits (10) and (13) of the previous case to implement $M'$.

**Lemma 13** Circuits with configuration

\[
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\end{array}
\]

cannot realize the Toffoli gate $M$.

**Proof.** We use the above trick and show that circuit (10) cannot implement $M'$. We derive from the input state $|0\rangle \otimes |\phi\rangle \otimes |\psi\rangle$ the circuit identity

\[
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
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\end{array}
\end{array}
\begin{array}{c}
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\begin{array}{c}
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\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\end{array}
B_2X^lB_1 \\
C_1
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
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\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\end{array}
B_3 \\
C_2
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
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\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\end{array}
B_4 \\
C_3
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
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\begin{array}{c}
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\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
\end{array}
\end{array}
\end{array}
Z
= Y
\tag{19}
\]
Similarly, the input state $|1\rangle \otimes |\phi\rangle \otimes |\psi\rangle$ yields
\[
\begin{align*}
\begin{array}{c}
|1\rangle \otimes |\phi\rangle \otimes |\psi\rangle \\
\end{array}
\end{align*}
\] (20)

We can deduce from circuits (19) and (20) the relation
\[
\begin{align*}
\begin{array}{c}
B_1^\dagger X B_1 \\
\end{array}
\end{align*}
\] (21)

which clearly leads to a contradiction. □

Lemma 14 Circuits with configuration
\[
\begin{align*}
\end{align*}
\]

cannot realize the Toffoli gate $M$.

Proof. It suffices to show that circuit (13) cannot implement $M'$. Considering the input state $|0\rangle \otimes |\phi\rangle \otimes |\psi\rangle$, we obtain the circuit identity
\[
\begin{align*}
\begin{array}{c}
|0\rangle \otimes |\phi\rangle \otimes |\psi\rangle \\
\end{array}
\end{align*}
\] (22)

And with input $|1\rangle \otimes |\phi\rangle \otimes |\psi\rangle$, we get
\[
\begin{align*}
\begin{array}{c}
|1\rangle \otimes |\phi\rangle \otimes |\psi\rangle \\
\end{array}
\end{align*}
\] (23)

Combining circuits (22) and (23), we have,
\[
\begin{align*}
\begin{array}{c}
\end{array}
\end{align*}
\] (24)

Similar to the proof for circuit (17), we again arrive at a contradiction after considering the trace. □

Case 3. We now examine five of the remaining six configurations.
Lemma 15  Circuit configurations of the form

\[
\begin{array}{cccc}
A_1 & A_2 & & \\
B_1 & B_2 & B_3 & \\
C_1 & C_2 & C_3 & C_4
\end{array}
\]

cannot implement the simplified Toffoli gate \( M \).

Proof. The most general circuit corresponding to the first configuration in the statement of the lemma is of the form

\[
\begin{array}{cccc}
A_1 & A_2 & & \\
B_1 & B_2 & B_3 & \\
C_1 & C_2 & C_3 & C_4
\end{array}
\]

(25)

Following the same steps as in the proofs of Lemmas 11 and 13, it is straightforward to see that such a circuit cannot realize \( M \) nor \( M' \). Therefore, the first and the third configuration can be ruled out. The other two configurations can be ruled out by realizing that \( M \) is self-inverse. □

Lemma 16  The circuit configuration

\[
\begin{array}{cccc}
A_1 & A_2 & & \\
B_1 & B_2 & & B_3 \\
C_1 & C_2 & C_3 & C_4
\end{array}
\]

(26)

cannot implement the simplified Toffoli gate \( M \).

Proof. It suffices to prove that the circuit

\[
\begin{array}{cccc}
B_1 & A_1 & A_2 & B_3 \\
B_2 & B_3 & & \\
C_1 & C_2 & C_3 & C_4
\end{array}
\]

(26)

cannot realize \( M' \). As in Lemma 11 we note that both \( A_1 \) and \( A_2 \) have to be sparse. Considering input states of the form \( |0\rangle \otimes |\phi\rangle \otimes |\psi\rangle \), it follows from circuit (26) that the circuit identity

\[
\begin{array}{cccc}
B_1 & B_2 & B_3 & \\
C_1 & C_2 & C_3 & C_4
\end{array} = Z
\]

(27)
must hold. We derive from the action on the input \( |1\rangle \otimes |\phi\rangle \otimes |\psi\rangle \) the circuit identity

\[
\begin{array}{c}
B_1 \quad C_1 \\
B_2 \quad C_2 \quad X^{1-l} C_2 \\
B_3 \quad C_4 \\
\end{array} = X
\] (28)

Combining circuits (27) and (28), we have,

\[
\begin{array}{c}
B_1 \quad C_1 \\
C_1 \quad C_2 X C_2 \\
B_1^T \quad C_1^T \\
\end{array} = Y
\] (29)

The right hand side of (29) cannot produce entangled output states when provided with the input states \( B_1^T |0\rangle \otimes |\phi\rangle \) and \( B_1^T |1\rangle \otimes |\phi\rangle \). It follows that either

\[
C_1^T C_2 X C_2 C_1 = I
\] (30)

or

\[
C_1^T X C_2^T X C_2 X C_1 = I
\] (31)

holds. Taking the trace on both sides, we arrive at a contradiction in either case.

Final Step. We have now excluded 26 of the 27 possible control-not configurations. We know that the only viable configuration

actually allows to realize the simplified Toffoli gate \( M \). The general circuit associated with the circuit configuration is of the form (26).

**Lemma 17** At least four single qubit gates are necessary in any realization of the simplified Toffoli gate \( M \) with three controlled-not gates.

**Proof.** The only viable general circuit structure with three controlled-not gate is given by the circuit (26). We will show that at least four single qubit gates in this circuit differ from multiples of the identity, and that the gate count cannot be reduced by flipping the gates using (4).

A circuit (26) realizing \( M \) is supposed to leave an input state of the form \( |0\rangle \otimes |\varphi\rangle \) invariant. This implies the circuit identity

\[
\begin{array}{c}
B_1 \quad C_1 \\
B_2 \quad C_2 \quad X C_2 \\
B_3 \quad C_4 \\
\end{array} = I
\] (32)
And we obtain from the action on $|1\rangle \otimes |\varphi\rangle$ the identity

$$B_1 C_1 \cdots C_3 X^{1-l} C_2 = YZ \quad (33)$$

Combining circuits (32) and (33), we obtain the equality

$$B_1 C_1 \cdots C_2 X = YZ \quad (34)$$

It follows from Lemma 4 that $B_1$ has to be sparse. By Lemma 3, this implies that the gates $B_2$ and $B_3$ in circuit (33) have to be sparse as well. Since we know that $A_1$ and $A_2$ are sparse, flipping any number of controlled-not gates in circuit (26) using equality (4) cannot decrease the count of the single-qubit gates. It remains to show that none of the four gates $C_1, \ldots, C_4$ in circuit (26) can be a multiple of the identity.

Since $B_1$ is sparse, let $B_1 = \text{diag}(e^{i\theta_0}, e^{i\theta_1})X^k$. Considering the input state $|0\rangle \otimes |\phi\rangle$ and $|1\rangle \otimes |\phi\rangle$, we can deduce from circuit (34) the equalities

$$C_1^\dagger X^k C_2^\dagger X C_2 X^k C_1 = Z, \quad (35)$$

$$C_1^\dagger X^{1-k} C_2^\dagger X C_2 X^{1-k} C_1 = X. \quad (36)$$

If follows from equations (35) and (36) that neither $C_1$ nor $C_2$ can be a multiple of the identity. Since $M = M^\dagger$, we can apply the same argument to the inverse of the circuit (26), hence neither $C_3$ nor $C_4$ is a multiple of the identity either. Therefore, at least four single qubit gates are non-trivial, as claimed. □

4 Conclusions

We have demonstrated that the simplified Toffoli gate by Margolus cannot be realized with fewer than three controlled-not gates. Four additional single qubit gates are required when $M$ is realized with minimal number of controlled-not gates. Our proof of this lower bound revealed the interesting fact that the solution by Margolus is essentially uniquely determined by these constraints. The tedium of cases in lower bound proofs can be daunting, but one usually gains valuable structural insights, particularly if
the bounds are tight. It would be interesting to know tight lower bounds for other fundamental constructions of quantum circuits, such as the Toffoli gate. It is conjectured that the Toffoli gate cannot be implemented with less than six controlled-not and eight single qubit gates.

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