Neutron-induced strike: Study of multiple node charge collection in 14nm FinFETs

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Abstract—FinFETs have replaced the conventional bulk CMOS transistors in the sub-20nm technology. One of the key issues to consider is, the vulnerability of FinFET based circuits to multiple node charge collection due to neutron-induced strikes. In this paper, we perform a device simulation based characterization study on representative layouts of 14nm bulk FinFETs in order to study the extent to which multiple transistors are affected. We find that multiple transistors do get affected and the impact can last up to five transistors away (~200nm). We show that the potential of source/drain regions in the neighborhood of the strike is a significant contributing factor. In the case of multi-fin FinFETs, the charge collected per fin is seen to reduce as the number of fins increase. Thus, smaller FinFETs are susceptible to high amounts of charge collection.

Index Terms—multiple transients, layout approach, critical area, soft error

I. INTRODUCTION

When high energy particles such as alpha particles or neutrons strike a semiconductor device, they generate charge at the region of strike. This charge can either recombine or get collected in the source/drain regions through diffusion or other mechanisms [1], [2], [3], resulting in a transient current known as single event transient (SET). A particle strike on a device layout can generate SETs in multiple transistors across different standard cells, affecting multiple logic gates. These SETs can propagate to flip-flops and flip the stored value resulting in multiple bit-flip errors, known as soft errors. The rate at which these errors occur is known as soft error rate (SER).

Typically, the reliability estimates at the architectural level are calculated based on a single-bit-flip fault model for soft errors in which a single random bit is expected to flip at any time [4], [5], [6]. Similarly, at the circuit level, an SET is modeled as a current injection into the drain of a single transistor [7], [8]. If multiple transients and multiple flips were to occur, these models will not accurately represent the reality and will result in optimistic reliability estimates. Therefore, it is important to quantify the extent to which a circuit/layout is susceptible to multiple transients especially in the current technology.

Device layouts with FinFETs, which have replaced the planar MOSFETs for sub-22nm technologies, are also susceptible to SETs. Most existing studies on soft errors in FinFETs focus on memories and show that the radiation sensitivity of FinFET based SRAMs is better than that of planar SRAMs [9], [10]. This is mainly attributed to the fact that the volume of the source/drain region (the fin) that connects to the substrate is small as compared to planar devices, resulting in reduced charge collection. With technology scaling, a radiation-induced strike can have a large region of influence and can affect multiple transistors and logic gates. The phenomenon of a radiation-induced strike affecting multiple transistors has been studied to some extent in [11], [12], [13] for planar MOSFETs but has not been understood to the same extent in FinFETs. Some studies with respect to FinFETs are performed in [14], [15] and they report that multiple cell upsets do occur in FinFET based SRAMs. Further, bulk FinFET based designs are reported to have higher soft error rate than that of SOI based designs [16]. Studies in [10], [17], [18] insist that better understanding of layout effects is necessary to predict multiple event transients. In this paper, we confirm the already known fact that multiple transients do occur, and we add value by quantifying the fraction of a layout that is affected due to a single particle strike.

We find that a strike can have an impact up to five transistors away (nearly 200nm) from the strike location. A source/drain region which is at a higher potential, collects higher amounts of charge. However, the nearest two transistors are the ones that are most affected. In the case of multi-fin FinFETs, charge collected per fin reduces as the number of fins increase. Thus, FinFETs with smaller widths are susceptible to high amounts of charge collection. Since the region of influence is large, the problem cannot be entirely tackled using simple layout techniques. A careful circuit-aware placement of small vulnerable gates may be necessary.

The rest of this paper is organized as follows. In Section II, we describe the device construction. We explain the role of potentials on charge collection in Section III. We present the quantification of multiple node charge collection in a layout of single-fin and multi-fin FinFETs in Section IV. We summarize and conclude the paper in Section V.

II. DEVICE CHARACTERIZATION

In the 2D and 3D analysis of planar transistors, we saw that the range of impact of a particle strike is large and hence multiple transistors are affected. Simple layout techniques did not help reduce the charge collection in multiple transistors. To study the extent to which multiple transistors are affected in an emerging technology, we perform particle strike simulations of 14nm bulk FinFET devices in 3D. We study the range of impact of a particle strike and the role of potentials on charge collection.
In Figure 1, we show a bulk n-FinFET built based on the information available in [19], [20]. The geometry of the device and doping concentrations are shown in Table I. The gate stack is constructed with TiN/HfO2 [21]. Parameters such as the fin height, STI depth, source/drain doping, channel doping and fin doping are calibrated to meet the on/off current ($I_{on}$ and $I_{off}$) and sub-threshold slope requirements of the 14nm bulk FinFET data [22]. The upper fin has a gaussian doping profile towards the channel as shown in the figure. The stress in the channel region is modeled as a gaussian profile as per the data available in [23], [24]. The device had a total of 78k elements after meshing.

![Figure 1](image)

Figure 1. (a) Structure of the 14nm bulk n-FinFET. (b) The fin is shown explicitly. (c) The FinFET device is shown along with the mesh

![Figure 2](image)

Figure 2. (a) Drain current (A/um) versus Gate source voltage (Vgs) is plotted for a drain source voltage (Vds) of 0.7V and 0.05V. The plot from our device is denoted by ‘Sim’ and the one in the specification [22] is denoted by ‘Spec’. (b) log of Drain current (A/um) is plotted versus Gate source voltage (Vgs).

![Figure 3](image)

Figure 3. Drain current(A/um) versus Drain source voltage (Vds) is plotted for gate source voltages (Vgs) of 0.5V, 0.6V and 0.7V. The plot from our device is denoted by ‘Sim’ and the one in the specification [22] is denoted by ‘Spec’.

| Device parameter         | Value   |
|--------------------------|---------|
| Gate length              | 20nm    |
| Effective oxide thickness| 1.2nm   |
| Fin height               | 45nm    |
| Fin width                | 10nm    |
| Fin pitch                | 42nm    |
| Gate pitch               | 70nm    |
| STI depth                | 60nm    |
| Total depth of the substrate | 400nm |
| Lower fin doping (Boron) | $1e19$ cm$^{-3}$ |
| Channel doping (Boron)   | $3e18$ cm$^{-3}$ [25] |
| Source/drain doping (Arsenic) | $1e20$ cm$^{-3}$ |

Table I

GEOMETRY AND DOPING CONCENTRATIONS OF THE 14NM BULK N-FINFET

In Figure 2, we show a plot of the drain current versus gate to source voltage ($V_{ds}$) of our device (denoted by ‘Sim’) for gate-source voltage ($V_{gs}$) of 0.5V, 0.6V and 0.7V, as compared with that in the specification (‘Spec’) [22].

We model the particle strike as a cylindrical column of charge with a gaussian radial track and is simulated using the HeavyIon module in Sentaurus Device. The physics models used in the simulation are as follows. Mobility degradation effects due to impurity scattering, carrier-carrier scattering, high electric fields and mobility degradation at the silicon-insulator interface are specified using the models: PhuMob, CarrierCarrierScattering, HighFieldsaturation, inversion and accumulation layer model (IALMob) and Enormal (Lombardi) respectively. Generation and recombination processes of electron-hole pairs are modeled using Auger, Band2Band and SRH recombination models. Quantum effects at the semiconductor–insulator interface are modeled using the eMultiValley modified local-density approximation (MLDA) model. These physics models are consistent with the models used in [26].

III. THE ROLE OF POTENTIALS ON MULTIPLE NODE CHARGE COLLECTION

To study the role of potentials of source/drain regions on charge collection in the case of FinFETs, we setup the following experiment. We construct a layout of two bulk n-FinFETs with a 11MeV particle strike in between the two
devices, as shown in Figure 4 (a). We vary the voltages of all the source/drain regions and perform particle strike simulations for each voltage combination. The charge collected in each source/drain region (A1, B1, A2 or B2) is plotted against the voltages in Figure 4 (b) and (c).

We notice that the charge collected in a source/drain (A1, B1, A2 or B2) is high, when the terminal is biased high, and it reduces by nearly 50% when the terminal is biased low. For example, from Figure 4 (b), we see that when B1 is biased low, the charge collected in that node reduces by over 50%. When all nodes are biased low (Figure 4 (c)), the charge collected in all the source/drain regions is minimum. This observation is similar to that observed with the planar transistors.

IV. MULTIPLE NODE CHARGE COLLECTION IN A LAYOUT OF 14NM BULK FINFETS

A. Charge collection in a layout of n and p FinFETs

We construct a layout of six bulk n-FinFETs as shown in Figure 5(a), to study the extent to which a particle strike can affect multiple transistors. Layouts with three device separations are simulated: 4λ, 7λ and 14λ (where 2λ = 14nm). We assume a particle to be incident in between the first two devices as shown in the figure and measure the charge collected in the drain regions (biased high to measure the maximum charge) of all the devices. Figure 5 and Figure 6, we plot the collected charge against the number of devices which collect at least so much amount of charge, for a particle energy of 11MeV and 5MeV respectively. For a 11MeV strike, we see that up to five devices (collect at least 2fC) can be affected due to a single particle strike. The overall part of the layout that collects 2fC is marked in the figure and the range of impact is nearly 200nm. However, the nearest two devices collect maximum amount of charge (8-10fC). In the case of 5MeV strike, two devices get affected on an average.

We performed a similar experiment on an array of six bulk p-FinFETs shown in Figure 7. The number of devices affected in the case of p-FinFETs is lesser than the number of devices affected in a layout n-FinFETs.

![Figure 4](image_url)

Figure 4. (a) Layout of two bulk n-FinFETs showing the particle strike location 'P'. The source/drain regions are marked as A1, A2, B1 and B2. (b) Charge collected in B1 and A2 is high when the respective nodes are biased high. (c) Charge collected in B1 and B2 is high when the respective nodes are high. The least charge collection is also shown.

![Figure 5](image_url)

Figure 5. (a) Layout of 6 bulk n-FinFETs showing the strike location and charge collection map for a 11MeV particle strike. (b) Graph showing the number of devices collecting more than a certain charge Q (x-axis).

![Figure 6](image_url)

Figure 6. (a) Layout of 6 bulk n-FinFETs showing the strike location and charge collection map for a 5MeV particle strike. (b) Graph showing the number of devices collecting more than a certain charge Q (x-axis).

B. Charge collection in a layout of multi-fin FinFETs

Typically FinFETs have multiple fins. In this section, we study the charge collection in a layout of such multi-fin FinFETs as the number of fins is varied. So, we construct five different layouts of two adjacent multi-fin FinFETs as shown in Figure 8. The number of fins in these five layouts

![Figure 8](image_url)
Figure 7. (a) Layout of 6 bulk p-FinFETs showing the strike location and charge collection map for a 11MeV particle strike. (b) Graph showing a comparison between the number of devices collecting more than a certain charge Q (x-axis) in n-FinFETs and p-FinFETs for 11MeV and 5MeV particle strikes.

varies from one to five respectively as shown in the figure. We assume a 11MeV particle to be incident in between the two devices and measure the charge collected in all the source/drain regions in each case. In Figure 9, we plot the minimum of the collected charge in these source/drain regions as the number of fins is increased. We see that a 2 fin FinFET does not collect twice as much charge as a single fin FinFET; it collects less. Similarly, a 5 fin FinFET does not collect five times as much charge as a single fin FinFET. This can also be observed from the transient current plots in Figure 10. If we were to calculate the charge collected per fin, it is highest in the case of two adjacent single fin FinFETs as compared to multi-fin FinFETs. So, single fin FinFETs are thus more susceptible to particle strikes.

Figure 8. Layout of two adjacent multi-fin bulk n-FinFETs. The number of fins varies from one to five.

V. Conclusion

We performed the analysis on 14nm bulk FinFETs to understand the extent to which multiple transistors are affected in the current technology. Our observations in the case of FinFETs are similar to those in the case of planar transistors. Multiple transistors are affected due to a single particle strike and the impact can last up to five transistors away (up to 200nm). However, the nearest two transistors are the ones that are most affected. Potentials of the source/drain regions have a significant impact on charge collection: higher the potential, higher is the charge collected. Further, we find that FinFETs with lesser number of fins are more vulnerable to a particle strike.

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References

[1] P. Dodd and L. Massengill, “Basic mechanisms and modeling of single-event upset in digital microelectronics,” Nuclear Science, IEEE Transactions on, vol. 50, no. 3, pp. 583–602, 2003.
[2] R. Ramanarayanan, V. Degalahal, R. Krishnan, J. Kim, V. Narayanan, Y. Xie, M. Irwin, and K. Unlu, “Modeling soft errors at the device and logic levels for combinational circuits,” Dependable and Secure Computing, IEEE Transactions on, vol. 6, no. 3, pp. 202–216, 2009.
