Study on the Output Low-Level Property of the SN74LS00N Chip

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Abstract. Generally, the load capacity of the integrated gate circuit depends on its output low-level property. This paper gives a theoretical and experimental study on the output low-level volt-ampere property of the current popular TTL NAND-gate SN74LS00N, and the true output property model and reasonable parameters that are considered to be inconsistent with those in relevant classical textbooks. In addition, with the actual measurement of the change of the power supply current of each gate under different logic states, the method and specific values of the key circuit parameters of the internal part of the integrated circuit—the input stage resistor \( R_1 \) and the inverting stage pull-up resistor \( R_2 \)—are given. This will play an active role in understanding the TTL 74LS series of electronic device circuits and their experimental teaching, related electronic engineering design, as well as the writing, publishing and teaching of the textbooks.

Introduction

The explanation of the TTL gate circuit is the popular and necessary content of the teaching of "Digital Electronic Technology" in Chinese universities [1-2], but most of the textbooks only explain the so-called "standard 74 TTL series" gate circuit that has long been outdated, although some also mention that the 74LS series of gates have been in use for more than 50 years but are still widely used. Therefore, it is rare to focus on the 74LS series of gates in the textbooks, and naturally it is inevitable that there is no detail description on 74LS gates [3-12]. This paper measures the output low-level volt-ampere property curve \( V_{OL}-I_{OL} \) of the TTL "four NAND gate" SN74LS00N gate circuit (manufactured by HLF, Huilyf, China) with high level inputs when the output is unloaded, which is supplemented by the measured power supply current \( I_{CC} \) of each gate under different logic states. This report gives the theoretical explanation of the volt-ampere property curve \( V_{OL}-I_{OL} \), and strives to enrich all the contents of the "Digital Electronic Technology" textbooks explaining the 74LS00 gate circuit.

The Principle Circuit of the 74LS00 NAND Gate

The principle circuit of 74LS00 NAND gate is shown in Figure 1 [6]. The figure shows the theoretical design values of the involved various resistors \( R_{1,2,4,5,6} \) and \( R_{B,C} \). This article does not cover its full voltage transfer property \( V_O-V_L \), input volt-ampere property \( V_I-I_I \) (this property at the input low-level state with no negative voltage is equivalent to the input load property), output high-level property \( V_{OH}-I_{OH} \), fan-out performance, noise tolerance, etc. Here, only the circuit parameters (the resistor \( R_1 \) at the input stage and the pull-up resistor \( R_2 \) at the inverting stage) and the overall low-level-output property of the internal part of the integrated circuit are discussed, so the values of \( R_{1,2} \) are the most important in this paper, and assuming that the turn-on voltage \( V_D \) of the Schottky diode \( D_{1,2} \) is constant at 0.3 V, the emitter junction of the anti-saturation Schottky transistor \( T_{2,5} \) is sufficiently conductive with a bias voltage of \( V_{BE} = 0.7 \) V.
Measurement and Analysis of the Power Supply Current $I_{CC}$ of the SN74LS00N

Usually, the power supply currents ($I_{CCH}$ / $I_{CCL}$ of one gate at the output high / low level states) of the gate in different logic states are known to evaluate the power consumption of the circuit. But our purpose we measured $I_{CCH}$ / $I_{CCL}$ is to derive out the internal related parameters $R_{1,2}$ of the integrated circuit that cannot be directly measured, and further confirm the working state of the gate. Since four NAND gates of the SN74LS00N use one power supply $V_{CC}$, the currents $I_{CC}$ we measured are the total current $I_{CC}$ of the four NAND gates.

In general, when all of the 8 inputs of the SN74LS00N are grounded, we can get the 4 $I_{CCH}$. If all 8 inputs are connected to $V_{CC}$ or left impending, the 4 $I_{CCL}$ can be obtained. However, here we also measured the $I_{CC}$ in the other three states: the number $l/h$ of gates whose logic states of output are low / high level is 1/3, 2/2 and 3/1, respectively, as shown in Figure 2, where $h + l = 4$.

![Figure 2. The measured power supply current ICC of SN74LS00N related to the state of each gate.](image)

From the first and last data points in Fig. 2, we can measure the $I_{CCH}$ and $I_{CCL}$ as 0.265 mA and 0.820 mA, respectively. Combined with the other three data points, it is found that the linearity of their connection line is very good, and all three data points are also perfectly satisfied:

$$I_{CC} = 0.265h + 0.820l$$  \hspace{1cm} (1)

This shows that the parameters of the $I_{CCH}$ and $I_{CCL}$ related components are very consistent inside the four gates when the output is unloaded. However, both of these parameters are larger than the
theoretical values calculated according to the principle circuit Fig.1. According to the conventional method of estimating the averaged gate power consumption $P$ at the normal operating state, the average power consumption of each gate is

$$ P = \frac{V_{CC} (I_{CCH} + I_{CCL})}{2} = 2.70 \text{ (mW)} $$

(2)

This parameter is 35% larger than the 2 mW given in all relevant manuals! All the inputs of the four NAND gates of this integrated circuit are suspended, that is, all the gates are on the turn-on state and $V_0 = V_{OL}$, and the maximum total power consumption is up to $5V \times 3.28mA = 16.4$ mW, which should be deeply sensed by teachers, students and device users.

In addition, the consistent between the measured input short-circuit current $I_{IS}$ value 0.264 mA of a single gate and the average $I_{CCH} = 0.265$ mA per gate indicates that the $I_{CCH}$ basically flows through the input stage resistor $R_1$, so that the actual $R_1$ can be derived:

$$ R_1 = \frac{V_{CC} - V_D}{I_{IS}} = \frac{5 - 0.3}{0.264} = 17.8 \text{ (kΩ)} $$

(3)

This is 89% of the published design value 20 kΩ, but it is reasonable after all, because the precision of the large resistance inside the integrated circuit is intrinsically limited.

Further, when the input $A/B$ is the high level $V_{IH}$, the base current $I_{B2}$ flowing through $T_2$ can be relatively accurately calculated to determine whether $T_2$ is in the saturated state. At this time, first one can assume that $T_2$ is not turned on, but $T_5$ is turned on, then the voltage drop across $R_6$ (only calculated by design value 12 kΩ) is $(5 - 0.7) \times 12 / (17.8 + 12) = 2.1$ V, which can guarantees the required bias voltage $V_{BE2} = 0.7$ V for $T_2$’s turning-on.

Then the base current of $T_2$ is divided:

$$ I_{B2} = \frac{V_{CC} - 2V_{BE}}{R_1} = \frac{5 - 0.7 \times 2}{17.8} = 0.14 \text{ (mA)} $$

(4)

Because the current flowing through $R_2$ is:

$$ I_{C2} = I_{CCL} = \frac{V_{CC} - 2V_{BE}}{R_2} = \frac{0.82 - 5 \times 0.7}{17.8} = 0.62 \text{ (mA)} $$

(5)

it is obvious that $T_2$ must be saturated, but $T_2$ is an anti-saturation transistor and its collector potential $V_{C2}$ is clamped at $1.4 \text{ V} - 0.3 \text{ V} = 1.1 \text{ V}$, then the value of $R_2$ can be calculated as:

$$ R_2 = \frac{V_{CC} - V_{C2}}{I_{C2}} = \frac{5 - 1.1}{0.62} = 6.29 \text{ (kΩ)} $$

(6)

This is 78.6% of the published design value of 8 kΩ, which is the main source of $T_2$ in the saturation conduction state and average power consumption over 2 mW.

Since the discharge circuit composed of $T_6$ and $R_{B,C}$ is in a lightly conducting state at this time, the $T_5$’s base current $I_{B5} \approx I_{B2} + I_{C2} = 0.76$ mA, the current amplification factor is assumed to be $β \approx 20$ for $T_5$, and the load sink current $I_{OL} < 8$ mA is limited, $T_5$ must be in deep saturation.

Measurement and Analysis of the $V_{OL}$-$I_{OL}$ Property of the SN74LS00N

The schematic diagram of the experimental test of the $V_{OL}$-$I_{OL}$ property carried out in this paper is shown in Figure 3, where the current sinking loads of the low level output are adjustable resistors $R_{1,1,2}$ with 100 kΩ and 10 kΩ value, respectively.
The test experiment used an EL-ELL-VI digital circuit teaching experiment instrument produced by Beijing Techshine Ltd. The \( V_{CC} \) used the 5 V voltage source on the instrument. At the test time, \( V_{CC} = 5.00 \) V \( \sim \) 5.04 V, and it was connected to the two inputs of the tested NAND gate, and all inputs of the other non-tested gate were grounded in order to reduce the power consumption of the entire SN74LS00N.

In this paper, we have thoroughly tested the four NAND gates of SN74LS00N and found that the consistency is very good, so we give a \( V_{OL}-I_{OL} \) property curve of one of the NAND gates, as shown in Fig. 4.

First, we found that the direct measurement of the output voltage \( V_{OL} \) without a load is 0.040 V, and because the actual leakage current \( I_{CEO} \) of \( T_4 \) makes the collector current \( I_{CS} \) of \( T_5 \) nonzero, this \( V_{OL} \) which is very close to 0 V is very stable. This is intrinsically different from the collector clamp voltage of 0.2 to 0.3 V of the anti-saturation transistor indicated in the textbook, and also meets the expectation that the lower the output voltage is, the better it is. From this we can try to speculate that \( T_5 \) and \( T_4 \) are not or don’t need to be anti-saturated Schottky transistors at all, but are ordinary low power transistors, which need to be verified from the manufacturer for further research.

Then, we connected the 100 kΩ adjustable resistor \( R_{L1} \) with a resistance of about 50 kΩ. Carefully adjust \( R_{L1} \) to make \( I_{OL} = 0.1 \) mA and find that the \( V_{OL} \) rises slightly to 0.048 V. At the next steps, five \( V_{OL} \) values are measured to \( I_{OL} = 0.6 \) mA at an \( I_{OL} \) increment of 0.1 mA at every step. In order to ensure the measurement accuracy, \( R_{L1} \) is changed to the 10 kΩ adjustable resistor \( R_{L2} \), the measurement continues to \( I_{OL} = 1.0 \) mA at an \( I_{OL} \) increment of 0.1 mA at a step. Next, it is measured at an \( I_{OL} \) increment of 0.5 mA to \( I_{OL} = 10 \) mA at every step, and finally measured at \( I_{OL} \) increments of 1 mA to \( I_{OL} = 13.15 \) mA. All 32 data points are plotted in Fig. 4, where the data points \( I_{OL} > 10 \) mA are
only quickly adjusted near the integer mA in order to protect the integrated circuit, but absolutely do not affect the linearity of the entire property curve.

From the linearity of the property curve, regardless of the neglect of the open/unloading voltage \( V_{OL(min)} = 0.040 \) V, the gate output can be equivalent to a linear resistance \( R_{OL} \) with a value of approximately 47 Ω.

Thus, it can be seen that when \( I_{OL} = 8 \) mA, \( V_{OL} = 0.412 \) V, which is consistent with \( I_{OL(max)} = 16 \) mA of the standard TTL series 7400 specification, so this is the root for \( I_{OL(max)} \) of the LS TTL gate dropping to 8 mA as the typical sink current value. Of course, because the TTL 7400 integrated circuit is not available at the moment, comparative studies are not possible.

Therefore, it is debatable to continue the teaching of "low-level output resistance \( R_{OL} \) as low as 10 Ω for the LS TTL gate” in the textbook. In particular, the starting point of this line of the \( V_{OL}-I_{OL} \) property map cannot be drawn above 0.1 V, but it can be approximated as the starting point through the origin. It is also wrong to carry out the depiction in the text according to the starting point of 0.3 V, but the starting point of the line of the \( V_{OL}-I_{OL} \) property map is drawn at the origin, which is not self-consistent between the depiction and map [1].

In addition, it can be seen that when the \( V_{OL} \) reaches the specification value \( V_{OL(max)} = 0.5 \) V, the corresponding \( I_{OL} \) is already about 10 mA, so some textbooks (including many materials explaining the standard TTL 74XX series) will be \( V_{OL(max)} \). It is not appropriate to do a complete correspondence with \( I_{OL(max)} \) and \( V_{OL(max)} \) (including text explanation and graphic explanation).

**Summary**

Through theoretical and experimental research on the power supply current change \( I_{CC} \) and low-level output volt-ampere \( V_{OL}-I_{OL} \) property of the LS TTL NAND gate SN74LS00N, it is inferred that the key circuit parameters the resistor \( R_1 \) at the input stage and the pull-up resistor \( R_2 \) at the inverting stage of the internal part of the integrated circuit are respectively 17.8 kΩ and 6.29 kΩ, and the low-output output gate output is equivalent to a 47 Ω linear resistor (ignoring the small low voltage when the sink current load is idling), which can play a constructive help for the deep understanding on the LS TTL gate circuits and its experimental teaching, related electronic engineering design, as well as the preparation and teaching of the textbooks.

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