Design and Analysis of Multilevel Inverter based on Cascaded Half-Bridge and Three-Phase Unfolder Circuit

Farhana N. Rosli, M. F. M. Elias, N. A. Rahim

Higher Institution Centre of Excellence (HICoE), UM Power Energy Dedicated Advanced Centre (UMPEDAC), Level 4, Wisma R & D, University of Malaya, Jalan Pantai Baharu, 59990 Kuala Lumpur, Malaysia

E-mail: nurfarhanarosli@gmail.com

Abstract. In this paper, a multilevel inverter based on cascaded half-bridge and three-phase unfolder is proposed. The proposed inverter design is simulated by using MATLAB Simulink. The converter is designed with four series-connected half-bridge cells and a three-level neutral-point-clamped inverter. The proposed converter is able to produce an output voltage of 230V and a frequency of 50 Hz. There are two modulation techniques implemented for the proposed inverter topology namely; phase-shifted modulation and phase opposition disposition modulation. The basic principle of operations using both modulation techniques including the performance analysis are presented.

1. Introduction
Multilevel inverters are currently a promising power converter especially for medium and high-power applications [1]. The most commonly used MLI configurations are cascaded H-Bridge (CHB), neutral-point-clamped (NPC) and flying capacitor (FC). Generally, MLI has better quality of harmonic profile, reduced dv/dt stress on load voltage and enables the use of power switches with lower voltage rating. MLI also can be implemented in low voltage applications such as integration of renewable energy into power grids due to the advantages of decreased output harmonics and switching losses [2, 3].

MLI can be arranged in symmetric, asymmetric, unipolar and bipolar configurations as listed in [4-12]. Recently, the MLI topologies categorized as reduced device count topologies have been introduced [13]. The features and analysis of several MLI topologies were summarized and discussed in [13, 14]. The utilization of multiple dc sources and switches is a known concept to generate multilevel output voltage in MLI especially using CHB inverters. Owing to many advantages it has, MLI is particularly suited for renewable energy systems. However, if a CHB is extended to three-phase application, it will have a significant increase in the number of devices count such as power switches, dc sources or capacitors. In [9], half-bridge (HB) modules are connected to each dc source and a full-bridge inverter is used to unfold the rectified dc-link into AC output voltage. This configuration is called bipolar as the circuit composed of level and polarity circuits.

To generate a 3-phase 5-level output line voltage for the topology in [9], it requires 3 dc sources and 18 power switches. For 3-phase CHB configuration, 12 power switches and 3 dc sources are required to generate 5-level output line voltage. A combination of FC and CHB topology was
implemented in [15]. However, the topology has shortcomings in terms of the utilization of large electrolytic capacitor and it requires additional control strategy to balance the capacitors in FC.

Recently, a series resonant converter based on a dual-active bridge with a three-phase NPC unfolder circuit has been introduced in [16] in which the converter is able to reduce dc-link capacitance requirement and switching losses of the inverter by using an unfold circuit. Thus, with the advantages of NPC unfold and half-bridge circuits, a new three-phase multilevel inverter topology based on half-bridge cell and NPC unfold circuit is proposed in this paper. Since the half-bridge inverter is a multilevel configuration circuit, the harmonic distortion of the output voltage can be further reduced. Moreover, the converter size and control parameters are further reduced as the usage of capacitor is eliminated from the proposed topology. The advantage of the proposed topology based on half-bridge cell and NPC unfold circuit is that the maximum level of output voltage that can be generated is seven at the maximum modulation index. Thus, the total dc-link voltage of the inverter is higher than the total input voltage. Another advantage of the proposed topology based on HB and NPC is the utilization of power switches are reduced from 36 to 32 as compared to 3-phase configuration producing 13-level output line voltage in CHB.

In Section 2, the circuit configuration and operation of half-bridge and NPC inverter are presented. In Section 3, phase-shifted modulation and phase opposition disposition modulation are explained and compared. In Section 4, the simulation results of both modulation techniques are shown and compared in terms of output voltage levels, harmonic distortion, modulation index, and filter requirement.

2. Design and Operation Principles
Circuit configuration of the proposed three-phase unfolder topology based on multilevel inverter is illustrated in Fig. 1.

![Figure 1. Circuit Configuration of Half Bridge Modules with Three Phase NPC Unfolder](image)

The proposed topology consists of three modules. Module 1 and Module 2 form an arrangement of series connection of half-bridge for top and bottom dc-link of the inverter. The combination of the two modules acts as level generation part of the unfold circuit. Module 3 consists of three-phase neutral-point-clamped inverter (NPC) and act as a polarity circuit. The half-bridge inverter is chosen since it is modular in nature and it can generate multilevel dc-link easily by connecting them in series [5, 9]. Whereas, the NPC inverter is selected since it can provide additional voltage level at higher modulation index compared to the two-level conventional inverter, thus producing higher output quality.

Level generation modules consist of 4 half-bridge cells in series with each cell has one direct current (dc) source and two switches operate in a toggle mode. Therefore, 8 switches and 4 dc sources are used to design the level generation modules as depicted in Fig.1. The first four switches (S1 to S4) are combined to form top module of dc-link while the later four switches (S5 to S8) are joined to form
bottom module of the dc-link. There are 4 possible switching states of the half-bridge cell as listed in Table 1.

| Table 1. Switching States of Half-Bridge Inverter |
|-----------------------------------------------|
| State | Voltage level $(V_{\text{top}}/V_{\text{bot}})$ | S1/S5 | S2/S6 | S3/S7 | S4/S8 |
|-------|-----------------------------------------------|
| 1     | 0Vdc                                         | 0     | 1     | 0     | 1     |
| 2     | Vdc                                          | 1     | 0     | 0     | 1     |
| 3     | Vdc                                          | 0     | 1     | 1     | 0     |
| 4     | 2Vdc                                         | 1     | 0     | 1     | 0     |

Note: S1-S2, S3-S4, S5-S6, S7-S8 are a complement to each other, 1 and 0 indicate the ON and OFF states of the switches respectively.

When S2 and S4 are turned ON, $V_{\text{top}}$ or voltage across between the switches in the top module is equal to 0. When only S1 or S3 is turned ON, the output voltage of the top module dc-link is equal to Vdc. When both S1 and S3 are turned ON, $V_{\text{top}}$ is equal to 2Vdc. A similar concept of switching state can also be applied in generating $V_{\text{bot}}$ or voltage across between the switches in bottom module. It can be observed that, to obtain a given level at total dc link, two switches are required to conduct simultaneously in top and bottom modules of the dc-link. It also can be observed that since voltage level is synthesized by combining all the input sources, equal load sharing is possible. These redundancies can provide flexibility if the capacitor is used for voltage balancing method. Based on the switching states shown in Table 1, the output voltage of dc-link can be presented as given in (1) for top dc-link, (2) for bottom dc-link and (3) for total dc-link voltage.

$$V_{\text{top}} = V_{\text{dc1}} (S1) + V_{\text{dc2}} (S3)$$  \hspace{1cm} (1)

$$V_{\text{bot}} = V_{\text{dc3}} (S5) + V_{\text{dc4}} (S7)$$  \hspace{1cm} (2)

$$V_{\text{tot}} = V_{\text{top}} + V_{\text{bot}}$$ \hspace{1cm} (3)

The inverter shown in Fig. 1 is a three-phase or a three-leg of NPC inverter. The leg has a dc link voltage of $V_{\text{tot}}$ which is generally halved into $V_{\text{top}}$ and $V_{\text{bot}}$. The leg consists of four bidirectional power switches with the additional two clamping diodes to produce common point ‘g’\[17\]. The three possible states of one leg NPC inverter are listed in Table 2. For analysis, the point ‘g’ is used as the reference node with a potential of 0V. The potential difference between the point ‘a’ which represents a leg for phase A and the common point which represents as ‘g’ is inverter output voltage at common point, Vag. It means that Vag can be in form of -1, 0 and 1.

| Table 2. Switching States of One Leg NPC Inverter |
|-----------------------------------------------|
| State | Vag | T1 | T2 | T3 | T4 |
|-------|-----|----|----|----|----|
| 1     | 1   | 1  | 1  | 0  | 0  |
| 2     | 0   | 0  | 1  | 1  | 0  |
| 3     | -1  | 0  | 0  | 1  | 1  |

The modulation technique for the proposed topology will be discussed later in the next section. Before that, the reference signals of the pulse-width modulation (PWM) technique and switching states of three-phase unfolding are derived based on a three-phase line-to-line voltage equation in the balanced system as listed in (4). Since the NPC has a common point and the dc-link voltage of NPC is halved into two, there are two reference signals at level generation part in which each of
the reference signal is represented for top (Vref1) and bottom module (Vref2). The two reference signals are generated after implementing equation (5) and its corresponding switching states are presented in Table 3.

Table 4 lists the switching state of the reference signals at inverter output voltage between each phase to a common point (Vxg) where x represents phase a, b, and c. Equation (6) and (7) show the relationship between inverter output voltage (Vxg), load voltage (Vxn) and line voltage (Vxx). Fig. 2 shows the illustrations of step-by-step procedures in generating two reference signals for half-bridge modules. The switching states of three-phase unfolder can be derived from the Vxg and its corresponding switching states as depicted in Fig 3.

\[
\begin{align*}
V_{ab}(\theta) &= V_m \times \sin(\theta) \\
V_{bc}(\theta) &= V_m \times \sin(\theta - 240^\circ) \\
V_{ca}(\theta) &= V_m \times \sin(\theta - 120^\circ)
\end{align*}
\]

where \( \theta = 2\pi f t \), \( f \) = frequency, \( V_m \) = Peak Amplitude of reference signal

\[
\begin{align*}
V_{ab}(\theta) &= | V_m \times \sin(\theta) | \\
V_{bc}(\theta) &= | V_m \times \sin(\theta - 240^\circ) | \\
V_{ca}(\theta) &= | V_m \times \sin(\theta - 120^\circ) |
\end{align*}
\]

\[
\begin{align*}
V_{an} &= \frac{2}{3} V_{ag} - \frac{1}{3} V_{bg} - \frac{1}{3} V_{cg} \\
V_{bn} &= -\frac{1}{3} V_{ag} + \frac{2}{3} V_{bg} - \frac{1}{3} V_{cg} \\
V_{cn} &= -\frac{1}{3} V_{ag} - \frac{1}{3} V_{bg} + \frac{2}{3} V_{cg} \\
V_{ab} &= V_{an} - V_{bn} \\
V_{bc} &= V_{bn} - V_{cn} \\
V_{ca} &= V_{cn} - V_{an}
\end{align*}
\]

Table 3. Switching States of Two Reference Signals

| Sector | Angle (°) | Vref1 | Vref2 |
|--------|-----------|-------|-------|
| 1      | 0 < \theta \leq 60 | Vca   | Vab   |
| 2      | 60 < \theta \leq 120 | -Vca  | -Vbc  |
| 3      | 120 < \theta \leq 180 | Vab   | Vbc   |
| 4      | 180 < \theta \leq 240 | -Vab  | -Vca  |
| 5      | 240 < \theta \leq 300 | Vbc   | Vca   |
| 6      | 300 < \theta \leq 360 | -Vbc  | -Vab  |

Table 4. Switching States for Inverter Output Voltage

| Sector | 1 | 2 | 3 | 4 | 5 | 6 |
|--------|---|---|---|---|---|---|
| Vag    | 0 | 1 | 1 | 0 | -1| -1|
| Vbg    | -1| -1| 0 | 1 | 1 | 0 |
| Vcg    | 1 | 0 | -1| -1| 0 | 1 |
3. Phase-Shifted (PS) and Phase-Opposition Disposition (POD) Modulation Techniques

The structure of converters can directly relate to its modulation techniques. Depending on the converter structure, each topology has its own best modulation technique. One carrier signal modulation method is typically adopted in two-level inverters whereas multilevel signal method is normally implemented in multilevel inverters to accommodate more switches as compared to the conventional inverters [18, 19]. PWM signals can be produced by using scalar and vector modulation techniques. For scalar PWM modulation technique or sinusoidal PWM (SPWM), the switching signals are generated by comparing a sinusoidal reference signal with a triangular carrier signal.

SPWM method typically uses phase-shifted (PS) and level-shifted (LS) modulation techniques [20, 21].

The LS modulation technique can be further categorized into phase disposition (PD), phase opposition disposition (POD) and alternate phase opposition disposition (APOD). POD and PS techniques have been identified as a suitable modulation technique for NPC and cascaded inverters. Therefore, PODPWM and PSPWM are adopted to modulate top and bottom modules of dc-link in the proposed multilevel inverter. A simple comparison between both modulation
techniques is made for a circuit configuration utilizing, two half-bridge cells for top and bottom modules of the proposed topology.

For PS modulation, N number of the cells of half-bridge inverter require $360^\circ/N$ number of phase-shifted carrier signals. Each module has two half-bridge cells, thus 2 carrier signals with 0 and 180 phase shift are needed for PS modulation as demonstrated in Fig 4. Each module is modulated independently using the corresponding reference signals as listed in Table 3 and depicted in Fig 2.

The POD modulation technique is arranged in a vertical shift instead of a phase shift as used in PS. A similar concept of PS modulation can be applied by calculating the number of carrier signals required. The amount of carrier signal is directly proportional to the number of cells. Therefore, 2 carrier signals are required, and each carrier is set between two voltage levels since there are 2 cells of half-bridge. The difference between POD and other LS modulation is that the carrier signal for the top module is in phase with each other whereas the carrier signals for the bottom module which represent a negative carrier is in opposite phase of the carrier signal for the top module. Fig.5 shows the arrangement of LS modulation technique with the corresponding reference signals. A stepped multilevel waveform of PS and POD are demonstrated in Fig.6 whereby Equation (8) - (9) show the relationship between the carrier signal ($V_{c1}, V_{c2}$) reference signals ($V_m = V_{ref1}, V_{ref2}$) and inverter output line voltage ($V_{out}$)

$$M = V_{out}/V_{in} = V_m / V_c$$

(8)

$$V_{ref1} OR V_{ref2} >= V_{c1} OR V_{c2} = S1 or S3 or S5 or S7$$

(9)

where $V_{c1} = $ Carrier Signal 1, $V_{c2} = $ Carrier Signal 2

![Figure 4. Configuration of Carrier and Reference Signals for PSPWM](image1)

![Figure 5. Configuration of Carrier and Reference Signals for PODPWM](image2)
4. Results and Discussion

The performance of the proposed multilevel converter based on half-bridge cells and NPC inverter is simulated by using MATLAB Simulink. The converter is designed to provide an output of 260V line voltage. This means that the minimum total dc-link voltage required for top and bottom modules is 320V. This will be the dc input voltage for NPC inverter to produce the desired AC output voltage. In this case, an off-grid system with a resistive load is considered. A low pass LC filter is used to smooth the inverter output [22]. Equation (10) shows the relationship of the peak amplitude of reference signal (Vref1, Vref2) with modulation index (M) whereby the simulation parameters of the proposed topology are given in Table 5.

\[
V_{\text{ref (peak)}} = M \times \sin(60^\circ)
\]

(10)

| Parameters                  | Value            |
|-----------------------------|------------------|
| DC input voltage, Vdc       | 160 V x 4        |
| Filter inductor, Lf         | 3-20 mH          |
| Filter capacitor, C\text{f} | 75-450 nF        |
| Load resistor, R            | 150Ω             |
| Carrier frequency, fc       | 10-60 kHz        |
| AC Voltage, Vrms            | 260 V Power      |
| Frequency, Hz               | 50 Hz            |

Fig. 7 shows the output voltage of the top and bottom modules as well as the total dc-link voltage for both PS and POD modulations. The output voltage produced at each module is 320V and this will serve as dc input for the inverter. For a fair comparison, both modulation methods are evaluated at the same operating conditions whereby in this case, the carrier frequency for PS is set to half of the carrier frequency under POD modulation. It means that as fc = 30kHz at POD modulation, the fc for PS modulation is 30kHz/2 = 15kHz. The carrier frequency of PS is divided by half due to the presence of 2 half-bridge cells in one module. Thus, the effective switching frequency for PS will be the same as the POD.

The configuration effect of the carrier frequency (fc) of PS and POD can be seen in the output voltage of top module as shown in the first row of Fig. 8 and Fig.9. Notice that at a certain instant of time, when fc is 30kHz (POD) and 15kHz (PS), there are 3 triggered pulses for output voltage at top module (Vtop). Switches S1 and S3 are turned ON at 1.5 pulses for PS modulation and for POD modulation, S3 continuously switched ON while S1 is switched ON at 3 pulses. This shows...
that PS modulation has an advantage over POD as it can generate 3 pulses at Vtop with reduced carrier frequency and it has even power distribution among switches as the switches is turned ON at toggle mode continuously. The switching patterns of switches T5 to T8 of the three-phase NPC unfolder are illustrated in Fig. 10. The switches of NPC unfolder are operated at the fundamental frequency of 50 Hz and both modulation methods use the same switching pulses for NPC unfolder. The inverter output line voltage (V_o) produce 3-level, 5-level and 7-level at 0.4, 0.96 and 1.15 modulation index.

Fig.11 shows the three-phase five-level of unfiltered and filtered line voltage with its current waveforms at M = 0.96. Output voltage at M = 0.4 and 1.15 are shown in Fig.12 and Fig.13 respectively. Fig.13 shows that the produced line voltage is 368V and it can generate one extra level at unfiltered output line voltage as compared to when M = 0.96. This is due to the fact that when M is equal to 1.15, the peak amplitude of the reference signals is 1. Thus, the total dc-link voltage can utilize additional 0.15% from the total dc input voltage.

The Fast Fourier Transform (FFT) of the Vab and Iab at M = 0.96 with carrier frequency at 30kHz (POD) and 15kHz (PS) are shown in Fig. 14 and Fig.15 respectively where the total harmonic distortion (THD) for voltage and current are below 5 percent which is still within the acceptable range of THD recommended by IEEE Std. 519, which are around 0.90% to 0.96%. From both figures, the magnitudes of the low order harmonics are very low as compared to the fundamental component.
Figure 9. Phase Shifted Vtop and Switches S1 and S3

Figure 10. Switching Pulses of Unfolder Switches

Figure 11. Output Waveform of Three-Phase (Unfiltered and Filtered Voltage, Line current)
THD can be further reduced at $M = 1.15$ where the range of THD for voltage and current is around 0.80% to 0.82%. At $M = 0.4$ and 1.15, the difference between PS and POD can be seen clearly in terms of waveform pattern and peak amplitude of line voltage as illustrated in Fig. 12 and Fig. 13.

The value of line voltage at $M = 0.4$ is 128V in which falls under range that can be supplied using a single dc source = 160V. Therefore, only 1 dc power supply and 1 half-bridge cell are utilized to operate at $M = 0.4$ as shown in POD modulation. However, this is opposite for PS modulation in which both half-bridge cells are utilized and produce 320V line voltage at $M = 0.4$. Notice that during PS modulation, there is a small spike on the output voltage at $M = 1.15$ compared to no spike at POD modulation.
By considering Fig. 14 and Fig.15, the load voltage of PS modulation has better THD as compared to POD modulation by 0.03% whereas the THD of load current at POD modulation is slightly lesser by 0.02% over PS modulation. Figure 16 shows THD range of unfiltered and filtered line voltage in terms of carrier frequency.

The results are obtained when the carrier frequency is set at 30 kHz and $M = 0.96$ as the THD of unfiltered line voltage is lesser than other carrier frequencies. It is also noticed that as the carrier frequency increased, the THD is also increased. However, as the carrier frequency increased, the filter requirement on inductor and capacitor values is reduced as shown in Fig. 17. Fig.18 shows the relationship between output voltage and THD for both modulation methods. It shows that as the modulation index increases which contributes to the greater output voltage, the THD is reduced. Comparing both techniques, it shows that POD modulation has better THD and utilize dc-link efficiently over PS modulation as $M$ is increased.

![Figure 14. FFT Analysis of Load Voltage (PS and POD)](image)

![Figure 15. FFT Analysis of Load Current (PS and POD)](image)

Figure 16. THD Unfiltered and Filtered Line Voltage against Carrier Frequency
Figure 17. Inductor and Capacitor values against Carrier Frequency

Figure 18. THD and Amplitude of Filtered Line Voltage against M

5. Conclusion
In this paper, the design and analysis of a three-phase multilevel inverter based on cascaded half-bridge cells and three-phase NPC inverter have been presented. It consists of two modules of cascaded half-bridge to produce the dc-link for the NPC inverter. The half-bridge cell can generate 3-level PWM output voltage whereas, the NPC inverter is switched at the fundamental frequency of 50 Hz. From the results, it showed that half-bridge modules modulated using PS has higher switching loss but even power distribution among switches as compared to POD that has lower switching loss but possess uneven power distribution among switches. The simulation results obtained verified the functionality of the proposed inverter employing both modulation technique, POD and PS. Closed-loop control is recommended as further works to maintain the inverter output voltage with input voltage derived from renewable energy sources such as solar energy. In addition, a prototype of the proposed multilevel inverter topology can be built to verify its performance experimentally.

Acknowledgement
The authors thank the technical and financial assistance of UM Power Energy Dedicated Advanced Centre (UMPEDAC) and the Higher Institution Centre of Excellence (HICoE) Program Research Grant, UMPEDAC - 2018 (MOHE HICOE-UMPEDAC), Ministry of Education Malaysia, RU007-2018 and RU012-2019, University of Malaya.
References

[1] Akagi H. Multilevel converters: Fundamental circuits and systems. Proc IEEE. 2017;105(11):2048-65.

[2] Yuan X. Derivation of voltage source multilevel converter topologies. IEEE Trans Indust Electr. 2016;64(2):966-76.

[3] Cecati C, Ciancetta F, Siano P. A multilevel inverter for photovoltaic systems with fuzzy logic control. IEEE Trans Indust Electr. 2010;57(12):4115-25.

[4] Babaei E, Kangarlu MF, Hosseinzadeh MA. Asymmetrical multilevel converter topology with reduced number of components. IET Power Electronics. 2013;6(6):1188-96.

[5] Babaei E. A cascade multilevel converter topology with reduced number of switches. IEEE Trans Pow Electr. 2008;23(6):2657-64.

[6] Najafi E, Yatim AHM. Design and implementation of a new multilevel inverter topology. IEEE Trans Indust Electr. 2011;59(11):4148-54.

[7] Babaei E, Kangarlu MF, Sabahi M. Extended multilevel converters: an attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters. IET Power Electronics. 2014;7(1):157-66.

[8] Xiao B, Hang L, Mei J, Riley C, Tolbert LM, Ozpineci B. Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications. IEEE Trans Ind Appl. 2014;51(2):1722-31.

[9] Su G-J. Multilevel DC-link inverter. IEEE Trans Ind Appl. 2005;41(3):848-54.

[10] Saeidabadi S, Gandomi AA, Hosseini SH, Sabahi M, Gandomi YA. New improved three-phase hybrid multilevel inverter with reduced number of components. IET Power Electronics. 2017;10(12):1403-12.

[11] Rahim NA, Chaniago K, Selvaraj J. Single-phase seven-level grid-connected inverter for photovoltaic system. IEEE Trans Indust Electr. 2010;58(6):2435-43.

[12] Hasan MM, Abu-Siada A, Dahidah MS. A three-phase symmetrical DC-link multilevel inverter with reduced number of DC sources. IEEE Trans Pow Electr. 2017;33(10):8331-40.

[13] Gupta KK, Ranjan A, Bhatnagar P, Sahu LK, Jain S. Multilevel inverter topologies with reduced device count: A review. IEEE Trans Pow Electr. 2015;31(1):135-51.

[14] Vijeh M, Rezanejad M, Samadaei E, Bertilsson K. A general review of multilevel inverters based on main submodules: Structural point of view. IEEE Trans Pow Electr. 2019;34(10):9479-502.

[15] Lezana P, Aceitón R. Hybrid multicell converter: Topology and modulation. IEEE Trans Indust Electr. 2010;58(9):3938-45.

[16] Chen WW, Zane R, Corradini L. Isolated bidirectional grid-tied three-phase ac–dc power conversion using series-resonant converter modules and a three-phase unfolder. IEEE Trans Pow Electr. 2017;32(12):9001-12.

[17] Gupta KK, Bhatnagar P. Multilevel inverters: conventional and emerging topologies and their control: Academic Press; 2017.

[18] Arslan AO, Kurtoglu M, Eroglu F, Vural AM, editors. Comparison of phase and level shifted switching methods for a three-phase modular multilevel converter. 2018 5th International Conference on Electrical and Electronic Engineering (ICEEE); 2018: IEEE.

[19] McGrath BP, Holmes DG. Multicarrier PWM strategies for multilevel inverters. IEEE Trans Indust Electr. 2002;49(4):858-67.

[20] Al Hadi A, Fu X, Waithaka W, Challoo R, Li S, editors. Comparison and Simulation of the Level-Shifted and Phase-Shifted Modulation for a Five-Level Converter for Integration of Renewable Sources. 2018 Clemson University Power Systems Conference (PSC); 2018: IEEE.

[21] Arazm S, Vahedi H, Al-Haddad K, editors. Phase-shift modulation technique for 5-level packed U-cell (PUC5) inverter. 2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018); 2018: IEEE.

[22] Texas Instruments. LC Filter Design. 2016.