We have carried out a coordinated experimental and theoretical study of single-electron traps based on submicron metallic (aluminum) islands and Al/AlO_x/Al tunnel junctions. The results of geometrical modeling using a modified version of MIT’s FastCap were used as input data for the general-purpose single-electron circuit simulator moses. The analysis indicates reasonable quantitative agreement between theory and experiment for those trap characteristics which are not affected by random offset charges. The observed differences (ranging from a few to fifty percent) can be readily explained by the uncertainty in the exact geometry of the experimental nanostructures.

I. INTRODUCTION

Recent advances in the physics of single-electron charging of macroscopic conductors (for general reviews see, e.g., Refs. 1,2) have led to proposals for several new analog and digital electronic devices. Such devices are considered, in particular, to be the most likely candidates to replace silicon transistors in future ultra-dense electronic circuits – see, e.g., Refs. 3,4.

Single-electronics is presently one of the most active areas of solid state physics and electronics, with hundreds of experimental and theoretical works being published annually. We are not aware, however, of any previous attempts to quantitatively compare experimental data for a particular device with results of theoretical analysis including geometrical modeling 5. Such a comparison was the main objective of this work. To that end, we selected one of the simplest devices, the single-electron trap 6.

Figure 1 shows the schematic layout of the circuit we discuss in this paper, which consists of a trap coupled to a single-electron electrometer. We will distinguish two types of conductors (“nodes”) in the circuit: externals, wires which extend to the edges of the chip and connect to the external measuring devices; and islands, small metallic segments that are connected each other and to the externals by tunnel junctions.

![FIG. 1. Schematic view of the 8-junction single-electron trap/electrometer circuit. Islands 12 and 13 are strongly coupled and together provide the energy well for an extra electron. Islands 6-11 form the array separating the well from the drive external 1.](image-url)
trap island, a voltage $V = V_-$ is applied, causing a hole
to tunnel from the drive external to the trap island, an-
ihilating the trapped electron.

If conditions (1) and (2) are satisfied, and the number
$N$ of junctions in the array is large enough, the rates
of thermal activation and cotunneling may be very low.
Thus, the lifetime $\tau_L = (\Gamma_T + \Gamma_Q)^{-1}$ of both the zero-
electron and the one-electron states of the trap may be
quite long, and the device may be considered bistable.

When the voltage $V$ is driven beyond the threshold
$V_+$ or $V_-$, the electron or hole tunnels through the ar-
ray in time $\tau \sim C_j / G_j$, which may be many orders of
magnitude shorter than $\tau_L$. Thus, in principle, the trap
can serve as a memory cell. Its contents can be read out
non-destructively by capacitive coupling of the trap to
the single-electron electrometer (see Section V).

Electrons can also overcome the energy barrier by ther-
amal activation and by macroscopic quantum tunneling of
charge (“cotunneling”). At sufficiently low temperatures,
the rate of thermally activated hopping over the bar-
rier is roughly

$$\Gamma_T \sim \frac{G_j}{C_j} \exp \left( \frac{-\Delta W}{k_B T} \right),$$

while the rate of spontaneous cotunneling through the
barrier scales as

$$\Gamma_Q \sim \frac{G_j^4}{C_j^2} \left( \frac{G_j h}{4\pi^2 e^2} \right)^{N-2}.$$
same file is also used to start the computational modeling process (see Section III). Wide lines in Fig. 3 represent the parts of the externals that extend from the trap and electrometer to contact pads at the edge of the chip. The narrow lines extending inward from the wide lines (Fig. 4) represent the inner parts of the externals. The short, narrow line segments (Fig. 4a) represent islands.

FIG. 3. Mask for complete chip containing several circuits. Pattern for circuits discussed in this paper is circled.

FIG. 4. Closeup of layout of circuits discussed in this paper, showing 20 µm cutoff radius used in simulations, and external node numbers. Externals have wide \( W = 1 \mu \text{m} \) and narrow \( w \simeq 50 \text{ nm} \) sections.

FIG. 5. (a) Central part of mask. (b) AFM image of central part of fabricated circuit. (c) 3-D outline of central part of geometrical model used for capacitance calculation.

The pattern of lines is written on the mask using the electron beam. Upon chemical development, each line in the PMMA becomes a window opening into a larger cavity in the copolymer, which is more susceptible to the electrons. This procedure results in a mask, shown schematically in Fig. 6, with several suspended bridges.
B. Deposition

The aluminum islands are deposited in two layers. The first layer is resistively evaporated in high vacuum directly onto the room-temperature substrate (Fig. 6a). This layer is then oxidized at \( \sim 10 \) mTorr \( \text{O}_2 \) for \( \sim 10 \) min (Fig. 6b), covering the Al islands with a \( \sim 1 \) nm layer of \( \text{AlO}_x \). Before depositing the second layer, the chamber is re-evacuated and the substrate is tilted relative to the Al source. The tilt creates a shift \( s \) between these two groups of islands, so that they partially overlap (Fig. 6c). The \( \text{AlO}_x \) creates tunnel barriers between the first and second layer islands. In our circuits, the shift \( s \) was about 120 nm along the vertical direction in Fig. 5a,b. The second aluminum layer is made thicker than the first, to allow reliable step coverage.

An AFM image of the resulting circuit is shown in Fig. 5b. This image exaggerates the island widths because of the finite angle of the AFM tip. Other observations (including SEM imaging) show that the islands oriented perpendicular to the direction of the shift were in fact spatially separated, in the successful samples.

Figure 5c shows a simplified model of the central part of the circuit, with externals and islands numbered. There are two islands for each corresponding window in the mask. For example, islands 6 and 7 are the first- and second-layer products of the same window (see also Fig. 7c.). Since the two layers of each external overlap each other extensively and are connected to the same voltage/current source, they effectively serve as one conductor. Thus, there is only one external for each corresponding window in the mask.

III. GEOMETRICAL MODELING

The essential electrostatics of a group of conductors can be described by their mutual capacitance matrix, \( C \). A program known as FastCap \[14\] can calculate \( C \) for an arbitrary collection of conductors, given the geometry of the conductors as input. The conductor surfaces are presented to FastCap as a set of discrete elements, or “panels”. We wrote a program called Conpan (for conductor panels) to generate a 3D paneling of a simplified model of the experimental system, starting from a 2D mask file. We will first explain the Conpan algorithm, then how its input parameters were derived from experiments.

A. Conpan Algorithm

Conpan represents circuit nodes by means of data structures called “sections”. Each section is a collection of data about a node or part of a node. The data include parameters such as node number, layer number, and limits in the \( xy \) plane. Sections may be recursively divided into subsections to represent overlaps and to facilitate paneling.

Consider two line segments from the larger mask file (Fig. 7a). These two segments eventually produce four islands separated by three tunnel junctions. Conpan expands each segment into a first-layer section (Fig. 7b) using the line-width \( w \). The second-layer sections (Fig. 7c) are initially identical to the first-layer sections except for a uniform translation \( s \) that results in overlaps.
FIG. 7. Geometrical model construction in Conpan: (a) Two segments of the array. (b) First-layer sections generated by Conpan for the two segments. (c) Second-layer island sections (shaded), partially overlapping first-layer sections. (d) Shape of first-layer islands. (e) Shape of second-layer islands overlapping first-layer. (f) First- and second-layer islands paneled for capacitance calculation.

1. Overlap Detection

Since a single second-layer section can overlap more than one first-layer section, Conpan detects the overlaps using a recursive detection algorithm. To begin, each second layer section is compared against each first layer section to detect overlaps. When an overlap is found, the second layer section spawns two daughter sections, one overlapping and one not. The axis and coordinate of the split are stored in the mother section, along with pointers to the daughter sections. The mother section becomes a placeholder, used only to keep track of the relationship among its daughter sections.

The non-overlapping daughter is then is compared against the remaining first-layer sections to find other overlaps. If there are more overlaps, the daughter spawns a pair of sub-daughters, and so on. The recursive process stops when no new overlaps are found. The daughter sections that remain undivided are called “final daughters”. Figure 8 gives a schematic view of the recursive overlap detection process for a single island.

FIG. 8. Recursive overlap detection in Conpan for a circuit fragment where a second-layer island S overlaps two first-layer islands F1 and F2. (a) Top view, with overlap areas shaded. (b) Comparing S to all first-layer islands, overlap of F1 is detected. S is split into two daughter sections, Sa and Sb, at y = y". (c) Comparing Sb to all first-layer islands, overlap of F2 is detected. Sb is split into Sba and Sbb at y = y"b. (d) Daughter sections Sa, Sba, and Sbb, having no further overlaps, are used to build the 3D structure shown in (e).

In addition to dividing up the second-layer sections to account for overlaps, Conpan also splits first-layer sections along the line where they are overlapped (see Fig. 7f). This allows the edges of panels facing each other across a junction to line up, facilitating convergence in capacitance calculations.

2. 3D Representation

Once all the overlaps have been found, Conpan can begin to create the 3-D model of the circuit. Each final daughter section becomes the base of a “block”, a rectilinear solid representing part of a conductor. The heights of the two layers are specified by the parameters h1 and h2. First-layer blocks and non-overlapping second-layer blocks have their base at z = 0. Overlapping second-layer blocks have their base at z = h1 + t, where t is the thickness of the gap between overlapping islands that represents the tunnel junction.
Finally, each block surface is divided into panels. The goal is to divide the surfaces in such a way that an acceptably accurate capacitance calculation can be performed, within the limits of available computer memory and calculation time. The division process is guided by an input parameter \( a \), the goal panel length. The surface of a block with length \( L_i \) along axis \( i \) is divided into the number \( n_i \) of divisions that brings \( L_i/n_i \) closest to \( a \). Once the block surface has been divided along both its axes, the resulting grid of panels is written to a panel file for input to FastCap. Each panel is stored simply as a quartet of \( x, y, z \) coordinates, one for each of the four corners, together with the number of the node it belongs to.

### B. Conpan Input Parameters

#### 1. Junction Thickness

In the physical circuit, the tunnel barriers separating the islands consist of \( \text{AlO}_x \), with unknown \( x \) and thickness \( t_j \). From literature data on similar junctions \([13]\), we expect a dielectric constant \( \epsilon_j \sim 4 \) and \( t_j \sim 1 \) nm. FastCap can handle dielectric surfaces much as it handles conductors – by dividing them into panels. However, each additional dielectric panel demands more computer memory and calculation time. Since \( t_j \) is much smaller than the transversal dimensions in all junctions, the electric field configuration outside the junctions does not depend strongly on their internal geometry. Therefore, we avoided modeling the junction dielectrics explicitly by replacing them with uniform free-space gaps (\( \epsilon = 1 \)) with the effective thickness \( t = t_j/\epsilon_j \). This effective thickness was adjusted to make the junction specific capacitance match the standard experimental value \( 4.5 \mu F/cm^2 \) typical for the \( \text{Al/AlO}_x/\text{Al} \) junctions with tunnel conductivity in our range (\( \sim 10^3 \) S/cm) \([15,16]\).

#### 2. Line Widths

The effective line width \( w \) of islands (and of the narrow parts of externals) is difficult to measure directly, because of its small magnitude (see Fig. 3). We determined \( w \) by requiring that the simulated inverse self-capacitance of the electrometer island \( (C_{14,14}^{-1}) \) match its experimentally measured value. We derive \( C_{14,14}^{-1} \) from the maximum value of the electrometer Coulomb blockade threshold voltage \( U_t \), as seen in electrometer I-V plots (Fig. 3):

\[
(U_t)_{\text{max}} = eC_{14,14}^{-1} \approx e/C_{14,14}.
\]

#### 3. Layer Heights

The heights of the two layers (\( h_1 \) and \( h_2 \)) are determined with a quartz monitor in the deposition unit during fabrication. In our case, these heights were measured to be 30 and 50 nm (\( \pm 10\% \)), respectively.

### C. Substrate

To calculate the effects of the substrate on circuit capacitances, FastCap requires a paneling of the comple-
membrane image of the “footprint” of the nodes, because panels representing the dielectric/metal interface (parts of the substrate covered by nodes) must be treated differently than panels representing the dielectric/air interface (the exposed substrate). In a manner analogous to that used for conductor panels (see Section IV), one could investigate various methods of paneling the complementary substrate image in order to minimize the number of panels, while yet retaining an acceptable level of accuracy. Such a paneling algorithm itself is not simple to create.

We avoided this problem through an old calculational trick in electrostatics – the image method. A modified version of FastCap was created, called ImageCap, which can simulate the effects of a single- or double-layer substrate by creating a set (or multiple sets, in the double-layer case) of image panels.

![Image panels in ImageCap](image)

FIG. 10. Image panels in ImageCap: (a) single substrate, (b) double substrate.

In the single substrate case, each image panel is formed by reflecting the original panel about the plane of the surface of the substrate (Fig. 10a). For the purposes of calculating the electrostatic potential above the substrate, the charge on the image panel is

$$q_1 = -\frac{\epsilon - 1}{\epsilon + 1} q,$$

(6)

where $q$ is the charge on the original panel, and $\epsilon$ is the relative dielectric constant of the substrate.

For a substrate covered by an oxide of thickness $H$, an infinite series of image charges is required for an exact representation of the electrostatic effect of the substrate (Fig. 10b). However, the distance from the original charge to each successive image charge increases linearly,

$$z_{2,i} = -2Ti - d, \quad i = 1, 2...$$

(7)

while the value of each successive image charge decreases exponentially,

$$q_2,i = 4\beta \frac{\epsilon_1 \epsilon_2}{(\epsilon_1 + \epsilon_2)^2} (\alpha \beta)^{(i-1)} q, \quad i = 1, 2...$$

(8)

Here $\epsilon_1$ and $\epsilon_2$ are the dielectric constants of the surface oxide layer and the bulk substrate, respectively. For our circuits, we have accepted the table values $\epsilon = 12.1$ for the bare Si substrate and $\epsilon_1 = 4.5$, $\epsilon_2 = 12.1$ for the SiO$_2$/Si substrate ($\alpha = 0.64$, $\beta = -0.46$). The resulting expression for the double-layer image charges,

$$q_{2,i} = -0.36 \times (0.29)^{(i-1)} q, \quad i = 1, 2...$$

(10)

shows that $q_{2,4}$ is already down by three orders of magnitude from the original charge. In our calculations, adding image levels beyond $q_{2,4}$ made no difference to the result, within a relative error (of the largest self-capacitances) below $\sim 10^{-4}$.

IV. CAPACITANCE MATRICES

A. Matrix Structure

Using the circuit panels generated by Conpan, ImageCap generates the capacitance matrix for the circuit. ImageCap adds the effect of image panels when calculating potentials, and uses no multipole acceleration; otherwise, its algorithms are the same as in FastCap [14]. First, the inverse capacitance matrix for panels is calculated and inverted. Each element $\hat{C}_{ij}$ in the capacitance matrix for nodes is then formed by summing all the panel capacitance matrix elements linking nodes $i$ and $j$. The charges and potentials on the nodes are related by

$$\bar{q} = \hat{C}\bar{\phi},$$

(11)
so that $\hat{C}_{ij}$ is numerically equal to the amount of charge induced on node $j$ when node $i$ is held at unit potential and all other nodes have zero potential.

$\hat{C}$ is an $N \times N$ matrix, where $N = N_e + N_i$, and $N_e$ and $N_i$ are the numbers of external nodes and island nodes in the circuit, respectively. Ordering all the external nodes before the island nodes, we can write $\hat{C}$ in terms of submatrices:

$$\hat{C} = \left( \begin{array}{c|c} \bigotimes & -\hat{C} \\ \hline -\hat{C}^t & C \end{array} \right).$$

(12)

Here $C$ is the symmetric $N_e \times N_e$ matrix of island-island capacitances and $\hat{C}$ is the $N_e \times N_i$ matrix of external-island capacitances (with elements defined positive, by convention). External-external capacitances (represented above by the $\bigotimes$) are not needed for our simulations.

The matrices calculated for our circuits are shown in Tables I and II. Note the up/down alternation of mutual capacitances along the array for the circuit on Si—e.g., $\hat{C}_{1,4}$, the capacitances linking external node 1 to the islands. For example, although island 7 is closer to external 1 than is island 8, $\hat{C}_{1,7} \approx 0.030 \times 10^{-16}\text{F}$ is smaller than $\hat{C}_{1,8} \approx 0.045 \times 10^{-16}\text{F}$ (similarly for islands 9 and 10). In $C$, we see that $\|C_{6,9}\|$ is smaller than $\|C_{6,10}\|$, etc. This phenomenon reflects the influence of the silicon substrate, which, due to its high dielectric constant ($\epsilon \approx 12$), links externals to the first-layer islands (which lie flat on the substrate) more strongly than to the second-layer islands (which lie partly on top of the first-layer islands). The capacitances for the circuit on SiO$_2$/Si do not show these oscillations as strongly, as we would expect from the smaller permittivity ($\approx 4.5$) of SiO$_2$.

**B. Model Accuracy**

Our model contains three main simplifications related to computational constraints, each of which introduces error into our capacitance matrix calculations.

1. **Free-space Junctions**

As noted above, we calculate $\hat{C}$ using free-space junctions of thickness $t$ instead of dielectric junctions of thickness $t_j$. (Although initially this approximation was intended for convenience, it later became a necessity as ImageCap does not handle explicit dielectric panels.) The error involved in this approximation was estimated by using FastCap to model a chain of islands in two ways: with explicit dielectric junctions and with free-space junctions. Results for an 8-island chain, with effective dielectric thickness chosen to make the island self-capacitances in both models the same, indicate that the error involved in this approximation is below 1% for junction-linked islands, and between 1% and 4% for non-junction-linked islands.

2. **Paneling**

In calculating capacitances, FastCap/ImageCap assigns a uniform charge distribution to each panel. Hence, its accuracy depends on how well the paneling follows changes in charge distribution on the node surfaces. Clearly, the denser the paneling, the better the representation of changes in charge distribution. However, panel density is effectively limited by available computer memory. For example, a FastCap simulation with 5000 panels typically requires more than 128 MB. ImageCap uses even more memory, since it calculates all panel interactions directly. We investigated the dependence of calculated capacitance on paneling density for a simple two cube system (Fig. 11a).

![FIG. 11. Two cube system with $L/t = 10$: (a) Panelings with 1, 3, and 9 panels/side. (b) Capacitances as a function of panel density ($\bar{q} = C\bar{\phi}$).](image)

The results (Fig. 11b) suggest that a non-uniform 3 × 3 grid (with a 1/10 ratio of edge panel length to central panel length, reflecting the peak in surface charge near the edges) for the smaller, roughly square-shaped node faces (Fig. 7f) is sufficient to calculate capacitances with an error below 10%. This is essentially how we paneled roughly square-shaped island surfaces. For longer faces (Fig. 12a) we used a larger number of divisions along their length. In an islands-only test circuit, increasing the total number of panels from $\sim 2000$ (corresponding
to the $3 \times 3$ grid for roughly square-shaped surfaces) to 6000 resulted in less than 1% changes in island-island capacitances. Thus we believe that the total error in island-island capacitances due to finite panel density is perhaps only $\sim 1\%$.

3. Lengths of Externals

The calculated capacitance values depend on the lengths of the external wires used in the model. In general, island-external capacitances increase with external length, at the expense of island stray capacitance (capacitance to a ground at infinity); the self-capacitance of islands does not change appreciably. To measure the error introduced by cutting off the externals at a given length, we have calculated capacitance matrices for test circuits with varying external lengths (Fig. 14). These circuits consisted of only one island and only the wide parts of the five externals. As a result, the error induced by cutting off externals in these test circuits should be proportionately larger than the error in the complete circuits. Still, the test circuits indicate that the error involved in cutting of the circuit at a radius of $20 \mu m$ (as in our final versions of the complete circuits) was less than 2%.

![Paneling](image)

**FIG. 12.** Paneling used in our calculations: (a) Trap islands (nodes 12 and 13). (b) Thin parts of externals. (c) Wide parts of externals.

To reduce the number of panels in the model, the two layers of an external are fused into one where they overlap. The error involved in this simplification is negligible. In addition, the narrow parts of the externals were divided along their length without edge panels (Fig. 12b). This simplification was found to cause an error in island-external capacitance of $\sim 5\%$ when the island and the external are connected by a junction (Fig. 13), and $\sim 1\%$ otherwise. Finally, wide parts of the external leads were represented by only their top and bottom surfaces (Fig. 12c), again to save panels. Since the width to height ratio $W/h \simeq 12$, the error introduced by this simplification is negligible. The top and bottom surfaces are divided according to the $3 \times 3$ type scheme described above for islands. Despite the large size of the resulting panels, the error involved in this simple paneling appears to be $\sim 1\%$.
Circuit radius $r$ (μm)

![Graph](image.png)

**FIG. 14.** Effect of lead length cutoff on the calculated island-external capacitance. The test circuit had only island 12 and wide parts of externals.

4. Total Error

Considering the error caused by the above simplifications in the calculation of $\hat{C}$ itself, it seems safe to say that the combined error for any given calculated capacitance matrix element was less than 10%. Note that we are not yet considering how well the geometrical model corresponds to the physical circuit (see Section VI).

V. SIMULATED AND EXPERIMENTAL RESULTS

We have calculated most properties of our circuits using MOSES, the single-electron circuit simulation program [17]. This program uses a Monte Carlo algorithm to simulate arbitrary SET circuits within the framework of the orthodox theory of single-electron tunneling [18]. MOSES needs to know the capacitance sub-matrices $C$ and $\hat{C}$ and the conductances of all tunnel junctions. The resistance of two electrometer junctions connected in series can be extracted from the slope of the experimental $I - V$ curve of the electrometer at high voltage ($V \gg e/C_\Sigma$). From this measurement, we calculated tunnel conductance per unit area. Conductances of all other junctions in the circuit were then calculated by assuming that their conductance is proportional to their nominal area. This assumption may only be accurate to an order of magnitude; however, most of the results discussed below pertain to stationary properties of the system, and are thus unaffected by deviations in conductance.

A. General Electrostatic Relations

Solving the matrix equation (11) for the island potentials $\phi_i$, with our definition (12) of the capacitance matrix we get

$$\phi_i = \sum_{j \in isl} C^{-1}_{ij} (q_j + \tilde{q}_j), \quad \tilde{q}_j = \sum_{k \in ext} \tilde{C}_{kj} V_k,$$

or, in a different form,

$$\phi_i = \sum_{j \in isl} C^{-1}_{ij} q_j + \sum_{k \in ext} \alpha_{ik} V_k, \quad \alpha_{ik} \equiv \sum_{j \in isl} C^{-1}_{ij} \tilde{C}_{kj},$$

(14)

where $V_k$ are the external potentials. These relations allow us to establish useful relations between changes in the external potentials $\{V_k\}$ and the charge state of the islands $\{q_j\}$, and the dynamics of the system as determined by the island potentials $\{\phi_i\}$.

B. Electrometer

Let us apply these relations, in particular, to the island of the single-electron transistor (number 14 in our notation, see Fig. 1) serving as the electrometer. Experimentally, we measure the dc voltage $U_{3,4}$ between the “source” and “drain” of the transistor (externals 3 and 4) under a small ($\sim 100$ pA) dc current bias. If the temperature is small enough ($k_B T < e^2 C^{-1}_{14,14}$), the voltage $U_{3,4}$ in such an experiment closely follows the threshold $U_t$ of the Coulomb blockade of the transistor — see Fig. 4.

It is well known (see, e.g., Refs. [13]) that the threshold is determined by the effective background charge $Q_o$ of the transistor island, which may be defined as

$$\phi_{14} |_{U_{3,4}=U_o} = C^{-1}_{14,14} (q_{14} + Q_o).$$

Comparing (15) and (14) above, we obtain in our notation

$$Q_o = \frac{1}{C^{-1}_{14,14}} \left[ \sum_{j \neq 14} C^{-1}_{14,j} q_j + \sum_{k \in ext} \alpha_{14k} V_k \right].$$

(16)

Eq. (16) allows us to find the theoretically expected variation of $Q_o$ due to any changes in the system. On the other hand, the threshold voltage is an $e$-periodic function of $Q_o$, and its maximum amplitude is expressed by Eq. (3) (for the case when the two transistor junction capacitances are the same). Thus, after we measure the experimental value of $(U_t)_{max}$, we can express the change in the effective charge $Q_o$ via the observed variation in $U_t$:

$$\Delta Q_o = \frac{e \Delta U_t}{2(U_t)_{max}}.$$

(17)

We have applied this approach to compare experiment and theory for two samples (#LJS011494A with SiO$_2$/Si substrate and #LJS011494B with Si substrate).
C. High-\( T \) electrometer response

We can readily measure \( \Delta V_i \) (\( i = 1, 2, 5 \)), the change in external voltage corresponding to one period of the oscillating threshold voltage (Fig. 15). At \( kBT \geq 0.1e^2/C_\Sigma \) (experimentally, \( T \geq 0.5K \)), thermal activation of electrons smears the Coulomb blockade effects and makes the junctions essentially transparent to tunneling, while the periodic response of the electrometer is still visible up to \( kBT \approx 0.3e^2/C_\Sigma \) (\( T \approx 1.5K \)). Thus, the measured values of \( \Delta V_i \) depend only on the circuit geometry and are essentially independent of the properties of the junctions.

Fig. 15. A typical experimental dependence of electrometer dc voltage \( U_{3-4} \) on gate voltage \( V_5 \) for a circuit comprising only an electrometer.

Moses is not a useful tool for directly modeling high-\( T \) behavior, as the number of jumps involved would be extremely high. However, we can simulate high-\( T \) behavior in Moses by specifying very high external voltages \( V_i \) while keeping temperature low (say, \( T = 0 \)). Under these high voltage conditions, the islands are flooded with extra electrons, and the tunnel junctions become effectively transparent to tunneling, just as in the high temperature case. Thus we simply apply an external voltage \( V_i \gg e/C_\Sigma \), measure how many electrons enter the electrometer island, and find the ratio of voltage \( V_i \) to electrometer charge \( q_14 \).

Table III shows values of the ratio \( \Delta V_i \) for simulated circuits and for experimental circuits averaged over several nominally identical samples. For the experimental values, the uncertainties given reflect the spread of among the samples. For the simulated values, the uncertainties given reflect the \( \sim 10\% \) error in calculated values, as described in Section 11. The simulated values are all lower than the experimental ones (with the exception of \( \Delta V_5 \) on SiO\(_2\)/Si), differing by as much as 50\%. The agreement is somewhat better for the circuits on SiO\(_2\)/Si.

D. Trap phase diagram

The simplest measurable characteristic involving single-electron charging of the trap is its phase diagram (Fig. 16), which reflects changes in the charge states of the array and trap as a function of the drive voltage \( V_1 \).

In Moses, we can directly view the charge state of each island in the array and trap as we vary \( V_1 \), as well the resulting change in \( Q_o \). In the physical circuit, however, we can only measure the response \( U_{3-4} \) of the electrometer and reduce it to the changes in \( Q_o \) using Eq. 17.

Figure 16 shows experimental and simulated electrometer response to ramping the trap drive voltage \( V_1 \) up and down over a period of several minutes. In both cases, the effects of the crosstalk between external 1 and the electrometer have been removed. In the experiment, superconductivity in aluminum is suppressed by a 2T magnetic field.

Figure 16. Electrometer phase diagram: \( Q_o \) as a function of trap drive voltage. \( V_2 = 8.2mV \), sample on SiO\(_2\)/Si. Crosstalk from drive voltage to electrometer has been subtracted, leaving only influence of trap charge state. In experiment, superconductivity in aluminum is suppressed by a 2T magnetic field.
tal. In simulations, MOSES accomplishes the same effect by subtracting $\Delta \varphi_{14} = \alpha_{114} V_1$ from the electrometer island potential.

Horizontal plateaus in Fig. 16 correspond to particular charge states of the system (trap + array), while vertical jumps correspond to changes of charge state. Thus, the hysteretic loops are regions of bi/multi-stability. The blow-up of the theoretical curve (Fig. 17) indicates the states for several plateaus. In particular, notice that the largest plateau correspond to states that are most stable because the array is either charged uniformly (one electron on each island, for example) or in a regular alternating pattern such as 1-0-1-0 (Fig. 13). The smaller plateaus correspond to more complex charge states which are less stable.

The experimental phase diagram bears a qualitative resemblance to the theoretical one, with somewhat shorter plateaus, though the order of magnitude is the same ($\sim 2$ mV for major plateaus). Simulated phase diagrams with randomly selected $\varphi_0$ show shorter plateaus than the $\varphi_0 = 0$ phase diagram (see Sec. VII below).

In Fig. 18, the large jumps in $Q_o$ correspond to a single electron entering the trap: $\delta Q_o \equiv (\Delta Q_o)_{e \rightarrow \text{tr}}$. Using Eq. (16), we can also express the simulated value of $\delta Q_o$ as

$$\delta Q_{\text{sim}} = \frac{C^{-1}_{\text{tr},14}}{C^{-1}_{14,14}} e,$$

where $\text{tr} = 12$ or 13, depending on which trap island the electron stops in. For comparison with experimental results, we take the average of the two possible values. The results are shown in Table IV. The difference between simulated and experimental values for Si is within the estimated geometric calculation error (10%), while the value for SiO$_2$/Si is not.

**E. Plateau dependence on $V_2$**

For a given plateau, the switching voltages $V_1 = V_\pm$ depend on the “ground” voltage $V_2$ (see Fig. 1). In the simplest model, with no stray capacitances, (see, e.g., Ref. [2] the charge state of the system depends only on the voltage $V = V_1 - V_2$. In that model, the dependences $V_{\pm}(V_2)$, corresponding to changes in the charge state, would form parallel 45° lines in the $[V_1, V_2]$ plane. In reality, however, stray capacitances of the islands to “infinity” (i.e. to a distant common ground) make the average potential $(V_1 + V_2)/2$ of the system relevant as well. As a result, the region corresponding to each charge state acquires a shape similar to a stretched diamond (Fig. 19).
FIG. 19. Experimental and simulated threshold voltages \( V_{\pm} \) as functions of \( V_2 \): Si substrate, superconductivity suppressed.

Simulations using MOSES show that the diamond shape results from the alternation of two types of electron transport that switch the charge state. At the low-\( V_2 \) end of the diamond, the charge state switches with the transfer of an electron in/out of the trap (see the energy diagram in Fig. 2a). However, at the high-\( V_2 \) side, the barrier for holes to enter or exit is lower than for electrons (cf. Fig. 2b). Near the sharp ends of the diamond, the critical transport may be even more complex (e.g., creation of an electron-hole pair inside the array, with the sequential motion of its components apart, one into the trap, and another into the external electrode). In these regions, however, the plateau corresponding to the charge state of the trap is already small and virtually disappears among numerous plateaus corresponding to various internal charge states of the array (Fig. 17). Figure 19 shows that while the diamond shape of the charge state in \([V_1, V_2]\) is well reproduced in experiment, the simulated width \( |V_+ - V_-| \) of the bistability region in \( V_1 \) is roughly twice the experimental value.

For each \( V_2 \), there is one value of \( V_1 \), called \( V_{eq} \), at which the energy barrier is the same for an electron to tunnel into or out of the trap \([18]\). A good measure of the relative influence of the two external voltages on the trap is the derivative

\[
dV_{eq}/dV_2 = \frac{\alpha_{2,tr}}{1 - \alpha_{1,tr}},
\]

where \( tr = 12 \) or 13, depending on which trap island actually traps the electron for a given \( (V_1, V_2) \). The two values are typically within 5% of each other, and we take their average when comparing simulated and experimental results. In the experimental data, we define the average \( V_{eq} \) by bisecting the diamond shape in the graph (Fig. 19). \( dV_{eq}/dV_2 \) is essentially a geometric property of the circuit and should not depend on thermal activation or cotunneling. As Fig. 19 shows, the simulated and experimental values are very close.

**F. Energy barrier**

At \( V_1 = V_{eq}(V_2) \), we can measure the energy barrier \( \Delta W \) experimentally by measuring trapping lifetime as a function of temperature (for experimental details, see Ref. \([10]\)). The Arrhenius law for lifetimes gives

\[
\tau_L \propto \exp(\Delta W/kT),
\]

so that plotting \( \log(\tau_L) \) vs. \( 1/T \) gives us \( \Delta W \). Dynamical simulations \([18]\) have shown that (20) is virtually unaffected by cotunneling for relatively high temperatures (\( \sim 100 \) mK and above). In simulation, MOSES allows us to measure \( \Delta W \) directly. Figure 20 shows the dependence of the trap energy barrier \( \Delta W \) on the bias voltage \( V_2 \), for the circuit on the SiO\(_2\)/Si substrate. The simulated energy barrier profile peaks at roughly the same value of \( V_2 \) as in the experiment, and the peak barrier value is within \( \sim 10\% \) of the experimental value. However, the simulated peak is sharper.
VI. DISCUSSION

Let us first discuss the results independent of the single-electron charging effects: the transistor response $\delta Q_o$ to a single electron entering the trap, the oscillation periods $\Delta V_i$, and the slope $dV_{eq}/dV_2$. The differences between simulated and experimental values for $\delta Q_o$ are 6% and 23% for the Si and SiO$_2$/Si substrates, respectively. Values for $\Delta V_i$ do not agree as well: differences between simulated and experimental values range from 15 to 38% for the trap on SiO$_2$/Si, and from 29 to 50% for the trap on Si. We had experimental data for $dV_{eq}/dV_2$ only on Si. Here the difference between experimental and simulated results was $\sim$ 12%. These numbers suggest how well our geometrical model corresponds to the physical circuit (the accuracy of the orthodox theory and of the MÖSÈS simulator is presumably much higher).

The most obvious idealization involved in our geometric modeling is that the islands created by Conpan are rectilinear and uniform. Even at the limited resolution of an AFM image (Fig. 5b), the contours of the fabricated circuits appear rounded and irregular on a scale of $\sim$ 10 nm. This is to be expected, due to the relatively large grain size of evaporated Al ($\sim$ 50 nm, comparable to the line width $w$) and the stochastic nature of the grain growth process. Most capacitance matrix elements should not depend strongly on small details of the island shape. However, irregularities in the shape of overlapping islands may change the area, and thus the capacitance, of the junctions linking them.

All other results involve single-electron charging effects. Here the difference between the theory and experiment is larger - typically by a factor of 2, and sometimes larger. We believe that the most important origin of this difference is the set of background charges $\vec{q}_0$. The Si substrate is capable of trapping charged impurities near the circuit islands. The result of these impurities is that the charge on island $i$ effectively changes from $\tilde{q}_i$ to $\tilde{q}_i + q_0$. These charges may furthermore be capable of thermal migration over time.

Simulated plots of the electrometer response to trap charging with three randomly selected $\vec{q}_0$ are shown in Fig. 21. It appears that the wide ($\sim$ 4 mV) steps near $V_1 = 0$ in the $\vec{q}_0 = 0$ plot are not stable to variations in $\vec{q}_0$: in most plots with random $\vec{q}_0$, as in the experimental plot, all step widths are less than 3 mV.

VII. ACKNOWLEDGMENTS

We greatly appreciate numerous fruitful discussions with D. Averin, R. Chen, L. Fonseca, A. Korotkov, W. Zheng, and K. Nabors. This work was supported in part...
by AFOSR grants #F49620-1-0044 and #F49620-96-1-0320.

[1] D. V. Averin and K. K. Likharev, in *Mesoscopic Phenomena in Solids*, edited by B. Altshuler, P. A. Lee, and R. A. Webb (Elsevier, Amsterdam, 1991), p. 173.

[2] *Single Charge Tunneling*, edited by H. Grabert and M. H. Devoret (Plenum, New York, 1992).

[3] D. V. Averin and K. K. Likharev, “Possible Applications of Single Charge Tunneling”, Ch. 9 in Ref. 2.

[4] A. N. Korotkov, “Coulomb Blockade and Digital Single-Electron Devices”, preprint (1996).

[5] After this work was completed, we received a preprint by M. Knoll, H. F. Uhlmann, M. Götz, and W. Krech (Report #ESE-3 at Applied Superconductivity Conference, Pittsburgh, PA, August 25-30, 1996) which compares geometrical modeling with experimental results for much simpler circuits comprising a single SET transistor.

[6] T. A. Fulton, P. L. Gammel, and L. N. Dunkleberger, Phys. Rev. Lett. 67 3148 (1991).

[7] D. V. Averin and Y. V. Nazarov, “Macroscopic Quantum Tunneling of Charge and Co-Tunneling”, Ch. 6 in Ref. 2.

[8] P. Lafarge et al., C. R. Acad. Sci. Paris 314, 883 (1992).

[9] K. Nakazato, R. J. Blaikie, J. R. A. Cleaver, and H. Ahmed, Electron. Lett. 29, 384 (1993); J. Appl. Phys. 75, 5123 (1994).

[10] P. D. Dresselhaus, L. Ji, S. Han, J. E. Lukens, and K. K. Likharev, Phys. Rev. Lett. 72, 3226 (1994).

[11] L. Ji, P.D. Dresselhaus, S. Han, K. Lin, W. Zheng, and J. Lukens, J. Vac. Sci. Technol. B 12, 3619 (1994).

[12] G. J. Dolan and J. H. Dunsmuir, Physica B 152, 7 (1988).

[13] T. A. Fulton and G. J. Dolan, Phys. Rev. Lett. 59, 109 (1987).

[14] K. Nabors, S. Kim, and J. White, IEEE Trans. on Microwave Theory and Techniques, 40, 1496 (1992).

[15] M. Maezawa, M. Aoyagi, H. Nakagawa, I. Kurosawa, and S. Takada, Appl. Phys. Lett. 66, 2134 (1995).

[16] J. K. Magerlein, IEEE Trans. on Magn. 17, 286 (1981).

[17] *MOSES*, Monte Carlo Single-Electronics Simulator (1995), available from Ruby Chen (rchen@felix.physics.sunysb.edu).

[18] L. R. C. Fonseca, A. N. Korotkov, K. K. Likharev, A. A. Odintsov, J. Appl. Phys. 78, 3238 (1995).
|   | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|----|----|
| 1 | 1.8268 | 0.0304 | 0.0452 | 0.0176 | 0.0343 | 0.0139 | 0.0749 | 0.0569 | 0.0342 | 0.0417 |
| 2 | 0.0122 | 0.0060 | 0.0146 | 0.0073 | 0.0181 | 0.0092 | 0.0883 | 0.1418 | 0.0393 | 0.0630 |
| 3 | 0.0388 | 0.0168 | 0.0352 | 0.0150 | 0.0305 | 0.0125 | 0.0838 | 0.0564 | 2.0413 | 0.1169 |
| 4 | 0.0167 | 0.0074 | 0.0163 | 0.0072 | 0.0153 | 0.0065 | 0.0461 | 0.0360 | 2.0835 | 0.1529 |
| 5 | 0.0113 | 0.0053 | 0.0125 | 0.0059 | 0.0137 | 0.0064 | 0.0551 | 0.0599 | 0.0864 | 0.1889 |

**TABLE I.** Capacitance matrix generated by ImageCap for circuit on Si substrate. Rows 1-5 belong to \( \tilde{C} \), rows 6-15 belong to \( C \). By convention, all \( \tilde{C}_{ij} > 0 \). All values in \( 10^{-16} \)F.

|   | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|----|----|
| 1 | 2.5498 | 0.0179 | 0.0147 | 0.0092 | 0.0110 | 0.0072 | 0.0267 | 0.0245 | 0.0147 | 0.0196 |
| 2 | -0.0223 | -1.7587 | 3.6101 | 0.0044 | 0.0034 | 0.0051 | 0.0039 | 0.0060 | 0.0049 | 0.0310 | 0.0580 | 0.0151 | 0.0254 |
| 3 | 0.0135 | 0.0095 | 0.0125 | 0.0086 | 0.0111 | 0.0074 | 0.0338 | 0.0270 | 1.2194 | 0.0540 |
| 4 | 0.0060 | 0.0043 | 0.0059 | 0.0041 | 0.0056 | 0.0038 | 0.0181 | 0.0166 | 1.2317 | 0.0638 |
| 5 | 0.0045 | 0.0033 | 0.0048 | 0.0035 | 0.0051 | 0.0037 | 0.0207 | 0.0248 | 0.0307 | 0.0739 |

**TABLE II.** Capacitance matrix generated by ImageCap for circuit on SiO\(_2\)/Si substrate. Rows 1-5 belong to \( \tilde{C} \), rows 6-15 belong to \( C \). All values in \( 10^{-16} \)F.
| Node $i$ | $\Delta V_i^{exp}$  | $\Delta V_i^{sim}$ | Difference | $\Delta V_i^{exp}$ | $\Delta V_i^{sim}$ | Difference |
|---------|-----------------|-----------------|-------------|-----------------|-----------------|-------------|
| 1       | 16(2)           | 8(1)            | 50%         | 32(5)           | 20(2)           | 38%         |
| 2       | 24(1)           | 17(2)           | 29%         | 54(2)           | 45(5)           | 15%         |
| 5       | 14(2)           | 7(1)            | 50%         | 38(6)           | 51(5)           | 34%         |

**TABLE III.** Values for $\Delta V_i$ in mV.

| Substrate          | $\delta Q_o^{exp}$ | $\delta Q_o^{sim}$ | Difference |
|--------------------|---------------------|---------------------|------------|
| Si                 | 0.064e              | 0.060e              | 6%         |
| SiO$_2$/Si         | 0.059e              | 0.045e              | 23%        |

**TABLE IV.** Response of electrometer to single electron entering the trap.