Double-sided transistor device processability of carrierless ultrathin silicon wafers

Ruby A. Lai¹ | Thomas M. Hymel² | Bofei Liu² | Yi Cui³

¹Department of Physics, Stanford University, Stanford, California
²Department of Materials Science and Engineering, Stanford University, Stanford, California
³SLAC National Accelerator Laboratory, Stanford Institute for Materials and Energy Sciences, Menlo Park, California

Correspondence
Yi Cui, Stanford Institute for Materials and Energy Sciences, SLAC National Accelerator Laboratory, 2575 Sand Hill Road, Menlo Park, CA 94025.
Email: yicui@stanford.edu

Abstract
Double-sided metal-oxide-semiconductor field-effect-transistor processing is demonstrated for the first time on an ultrathin crystalline silicon substrate of 6-20 μm in a 100 mm diameter wafer format without a carrier wafer, the thinnest free-standing silicon wafers ever fabricated. The compatibility of the flexible material with conventional semiconductor processing tools is enabled by supporting an interior ultrathin silicon with a surrounding thicker ring of silicon. Current-voltage characteristics of transistors on ultrathin silicon show performance as expected from bulk silicon, with electron mobility ~1500 cm² V⁻¹ second⁻¹. Mechanical measurements quantify the handleability.

KEYWORDS
carrierless wafers, flexible electronics, integrated circuits, ultrathin silicon

1 | INTRODUCTION

Crystalline silicon is the most widely used and superior semiconductor material. It is mechanically strong, chemically versatile yet easily passivated, thermally stable, dopable in electron or hole carriers, made from cheap and plentiful precursors, and has chemical precursor forms that can be distilled to extremely high purity. Ultrathin silicon adds mechanical flexibility to this list of silicon's attributes: a 3 μm thick Si sheet can be folded to a 1 mm bending radius.¹ The flexibility afforded by the form factor along with the high carrier mobility of crystalline silicon, orders of magnitude superior to organic semiconductors, is crucial for high-performance flexible electronics.²⁻⁴ with previous work on 290 nm ultrathin silicon ribbons demonstrating transistor device mobilities a few factors below that of bulk Si.⁵ Previously, mechanical flexibility with crystalline silicon had been achieved on the millimeter scale using flexible interconnects connecting silicon dies.⁶ In this work, we demonstrate that ultrathin silicon can achieve the same carrier mobility as bulk Si.

Ultrathin silicon has applications in 3D integrated circuits, where the ultrathin substrate enables fabrication of short through vias for improved chip performance and reduced power dissipation.⁷,⁸ The optical transparency also enables through-wafer alignment for a more facile backside lithography and stacked alignment process. Increasingly thinner silicon wafers are being pursued in crystalline silicon photovoltaics for enhanced photocurrent.⁹,¹⁰ Thin silicon electron detectors have recently driven advances in cryogenic electron microscopy.¹¹,¹² Ultrathin silicon may also prove useful for radiation-insensitive devices for its transparency to high energy neutrons, similarly to silicon-on-insulator radiation-hard devices.¹³
A key roadblock to incorporating thinner silicon into electronics is its processability. High tech manufacturing apparatuses and handling mechanisms assume levels of rigidity and strength which silicon no longer meets as the material is thinned below 150 μm. Thus, previous work on ultrathin silicon fabrication methods have focused on fabricating the device first, then employing methods to release a thin layer of silicon from the top, or to remove the bulk of the silicon from the backside.25

In other approaches, an ultrathin silicon substrate is supported by a wafer support system, typically by temporarily bonding it to a carrier wafer of silicon or glass.20-24 There are yield challenges to this approach, because of the difficulty of attaining both sufficiently high-bond strength needed for high-temperature processing, and sufficiently weak-bond strength for de-bonding without breakage.25 The presence of a carrier wafer also presents integration challenges for existing fabrication tools, as all automated handling and alignment robotics will need to be modified for the presence of a carrier wafer.25

In this paper, we use a carrierless approach by first thinning the interior area of a 100 mm wafer substrate, leaving a recess surrounded by a thick handling ring around the edge for mechanical strength. This silicon handling ring shape is similar to the TAIKO substrate developed by DISCO, which uses mechanical polishing to remove the interior area.26 Due to the mechanical stress of the polishing, the TAIKO substrates are limited to thicknesses of minimally 20 μm and more typically 150 μm.27 Promising results on fabrication handleability on 60-150 μm substrates have been pioneered with short single-sided process flows.28,29

We focus here on even thinner substrates in the range of 6-20 μm, which we can achieve controllably with alkaline wet etching, and on dual-sided processing, which have not been previously demonstrated. We directly fabricate transistors using conventional semiconductor tools, demonstrating a complex dual-sided process-flow on ultrathin wafer-scale silicon for the first time, incorporating an entire transistor fabrication process flow involving high-temperature, wet-processing, spin-coating, and vacuum. We believe this novel capability is of broad interest to the scientific community, where it may inspire new directions of study for materials physics,30 batteries,31 photovoltaics,32 bio-compatible materials,33,34 and advanced physics particle detectors.35

2 | RESULTS

In order to provide the mechanical strength and rigidity necessary for processing in standard semiconductor equipment, we begin by fabricating an ultrathin silicon wafer supported by a thicker ring of silicon (Figure 1A). We used 100 mm diameter double-side-polished (100) wafers of 350 μm thickness. Silicon nitride was deposited on both sides by chemical vapor deposition in a 25 mm annulus at the outside edge of the wafer, with the interior 75 mm diameter area physically masked by a glass disk. The wafers were then etched in tetramethyl ammonium hydroxide (TMAH) until the interior region reached the desired thickness. With our etching conditions, the specularly smooth surface of the double-side-polished wafer was retained in the interior, and the outer ring remained 350 μm in thickness.

The thick support ring of silicon allows full materials compatibility in all equipment, unlike other handling wafer mechanisms which require the use of adhesive materials that have reduced thermal budget or chemical incompatibilities. The use of thermosonic bonding, which uses no adhesive between a handle and a thin silicon substrate, does not work well with ultrathin wafers because of the fragility of the thin silicon. We then followed a 76-step fabrication process flow, to fabricate n-type metal-oxide-semiconductor transistors on two sides of the thin silicon (Figure 1B). The thin interior section, which is 6-20 μm and optically transparent to red light (Figure 1C), is then laser-cut to die (Figure 1D). The flexibility and the double-sided characteristic of our process is showcased by wrapping the thin processed die around a 1-in. diameter glass tube.

A benefit of the use of the silicon handling ring in lieu of other carrier wafer systems is that it does not require the consideration of chemical compatibility of the carrier or adhesive. Usual chemical dipping methods were used, including dips in cassette or manual dipping in beakers (Figure 2A). Additionally, the rigidity of the handling ring prevented adhesion of the flexible membrane to the wet-processing cassettes. We found this to a major problem when working with free-standing silicon membranes: a thin water layer would adhere the films to the Teflon cassettes or to each other, preventing their removal (Figure 2B).

Similarly, the handling ring’s mechanical rigidity enabled easy integration for the high temperature processing (Figure 2C). A flexible free-standing membrane could not be held vertically in shallow furnace tube quartz boat without toppling over. Due to the high temperature gradients present in these processes, there are strong air currents during the loading and unloading processes. These air currents caused breaking in free-standing wafers, but do not break the thin wafers supported by the handling ring.

To spin-coat resist on our wafers, we used spin coater with a vacuum chuck of diameter less than 3 in. and contacted only to the interior thin silicon membrane. Visible
thickness variation was visible in the pattern of the vacuum lines of the vacuum chuck due to the flexibility of the thin Si, but these nonuniformities did not prevent successful patterning at our minimum feature size of 4 μm. We also used a larger chuck which contacted the outer thick handling ring. The inner area bowed downwards (Figure 2D), causing large variation in resist thickness, so we did not use this method for processing.

We modified the use of the Karlsruhe manual mask aligner so that only the interior Si membrane was contacted by the mask and chuck. A 2.5 in. Cr glass disk photomask was adhered by tape to a 5-in. blank mask. A second chuck glass of 2.5 in. diameter was positioned underneath the sample. This enables the mask to be pressed firmly onto the silicon surface. To adhere the thin silicon membrane to its chuck, we used a droplet of water as the adhesion layer. As shown in Figure 2E, this adhesion is quite strong, yet the wafer and its carrier can be very quickly and easily separated by lifting up on the handling ring with tweezers, avoiding direct mechanical handling of the membrane. This is the same adhesion that was problematic for the wet-processing of free-standing silicon sheets.

Etching, ion implantation, and deposition steps were followed with standard equipment. In these processes, a variety of wafer handling mechanisms were used, all of which interacted only with the handling ring. For metal liftoff, gentle sonication was demonstrated to be possible although not required for our feature sizes (Figure 2F).

After the 76-step fabrication process flow, the ultrathin silicon dies were released from the handling ring by an infrared laser cutter. The transistors were measured by probe station I-V measurement (Figure 3). The transistors qualitatively behave as designed. The Id-Vg of the same transistor on a 6 μm thick wafer measured on a flat surface and measured on a surface with radius of curvature 70 mm were not significantly different (Figure 3C). This is consistent with the small applied tensile strain of approximately 6 μm/(2 × 70 mm) = 4e−5, two orders of magnitude less than typical device strains of ~0.1% applied via Si-SiGe lattice mismatch. We do not observe a dependence on the substrate thickness, which has been observed for ultrathin Si of 50 nm thick. From these data for the device on the 6 μm wafer, we extract a threshold voltage of V_T = −0.70 V and electron mobility ~1500 cm² V⁻¹ second⁻¹, identical to what we expect from devices on standard bulk Si wafers.

We observed significant variation in the threshold voltage and the sub-threshold current, which we attribute to gate-pattern misalignment to the source and drain contacts. During our process, we observed typical misalignment of less than 0.25 μm, but up to 1 μm misalignment. We also subjected the 6 μm thick Si die to 1000 cycles of bending to a 70 mm radius of curvature,
which decreased the channel current in the triode region but not the saturation region. We attribute this observation to increased contact resistance, which causes a smaller voltage to drop across the device at the same nominally applied $V_{ds}$.

Clearly, our substrates’ ability to withstand the numerous processing steps demonstrates the increased handleability with the handling ring. To more quantitatively characterize this increase in handleability, we compared the force required to break a 20 μm thick Si wafer with and without the supporting ring with a ring-on-ring compression test (Figure 4C). The samples are placed on a ring of 55 mm and compressed from above with a ring of 20 mm diameter. The free-standing ultrathin silicon is made using the same etching method described but is freed from its support by laser cutting. The breaking force for the supported thin silicon is about 150 times greater than the free-standing silicon.

Our free-standing ultrathin silicon dies of 6 μm thick withstood bending of 12.7 to 70 mm radius of curvature. We observed higher and variable minimum bending radii for nominally identical thickness ultrathin silicon pieces in comparison to Reference 1. Because we used very similar etching method to achieve ultrathin Si pieces, we attribute this difference to the sensitivity of ultrathin silicon to the scissor-cut vs laser-cut edges.40 Other authors have achieved minimum bending radii of 17 mm for 60 μm thick wafer-scale nanotextured Si and 1.4 mm for 15 μm thick Si chips.41,42

Our reported wafer thicknesses were established via SEM cross-section imaging of a wafer section from the wafer center. Nondestructive thickness mapping across a wafer was also performed on a thinned wafer via spectral reflectance measurement (Filmetrics F50), showing a total thickness variation (TTV) of 12 μm after etching (Figure 4D). The original unetched wafer was specified to be TTV < 10 μm, indicating that the described etching process has some etch-rate non-uniformity. Furthermore, the gradient in the transmitted color of the thinned wafer from Figure 1C indicates a thickness for that wafer.
ranging from approximately 2-10 μm, in excess of the <1 μm TTV specified by the manufacturer. However, we also had etched wafers with a uniform transmitted color.

3 CONCLUSION

In this paper, we demonstrate dual-sided fabrication of transistors on 6 μm ultrathin crystalline silicon substrates for the first time. To our knowledge, we have shown the thinnest free-standing silicon wafer ever fabricated. Aside from the first step to etch the silicon wafer, we used all conventional CMOS lithography and handling steps to fabricate the devices, demonstrating the robustness of the substrate to processing and its ease of integration into existing process flows. We achieved this dual-sided transistor device on such a thin and fragile substrate by using a thicker support ring of silicon for its rigidity and handleability during processing.

4 EXPERIMENTAL SECTION

4.1 Preparation of substrates

100 mm diameter, boron-doped p-type, 1-10 Ω-cm resistivity, (100) double-side-polished prime Si wafers with total thickness variation <1 μm were used. 280 nm of silicon nitride was deposited on the outer annulus of width 25 mm using plasma-enhanced chemical vapor deposition, Plasma-Therm Shuttlelock SLR-730-PECVD, 350°C, 100 W RF power, 1 Torr, 6 sccm flow NH3, 1000 sccm He, 200 sccm SiH4, and 400 sccm N2. The interior area was masked by a 75 mm diameter glass disk. This was repeated on the backside. Just prior to etching, the wafers are cleaned with 10 m of RCA1 (5:1:1 H2O: 30% H2O2: 30% NH4OH) at 50°C, 10 m of RCA2 (5:1:1 H2O: 30% H2O2: 30% HCl) at 50°C, and 30 seconds of room temperature 2% HF in H2O, with each cleaning step followed by six times dump rinse in H2O. The wafers are placed in

FIGURE 3 A, Scanning electron micrograph of devices fabricated on ultrathin silicon. B, Microscope image of probe tips deforming ultrathin silicon during measurement. C, Id-Vg measurements with Vds = 1 V of transistor on 6 μm thick wafer, flat and bent around 70 mm radius of curvature. D, Id-Vg measurements of double-sided transistors with channel width 60 μm and length 24 μm on silicon wafers of various thicknesses. E, Id-Vd measurement of transistor with channel width 60 μm and length 24 μm fabricated on 6 μm thick wafer, before and after 1000 cycles of bending over a 70 mm radius of curvature.
Teflon wafer cassette and submerged in a 91°C etch bath of 25% by weight tetramethyl ammonium hydroxide in H2O. To ensure steady etching temperature, the etch bath is fitted with a reflux condenser and placed in a controlled temperature water bath covered in foil to reduce evaporation. To refill the controlled temperature water bath during the etch, water is pre-heated to 91°C to reduce temperature fluctuations. The double-sided etch rate is 1.090 μm min⁻¹ for lightly doped n-type and 1.038 μm min⁻¹ for lightly doped p-type. To accurately target a desired thickness without overetching, we use a “canary wafer” which is 10-20 μm thicker than the other wafers. When the canary wafer disappears or becomes very thin, it visibly signals the thickness of the remaining wafers at that time. We approximate the thickness by shining a flashlight behind the wafer; the brightness and color of the transmitted light reveals the approximate thickness < 40 μm.¹ The etched thickness is later determined accurately by cross-section scanning electron microscopy. When the desired thickness is reached, the wafers are rinsed in water, singly dried by nitrogen gun or altogether by heating the cassette in a 110°C oven. These substrates are stored in a standard vertically slotted cassette box. To prevent crushing, we remove the slots in the lid.

4.2 Double-sided transistor fabrication

We closely referred to Reference 36, modifying it for double-sided transistors. We fabricated photomasks on 2.5 in. diameter, 1/16 in. thick fused glass disks (Accuglass). The glass disks were cleaned in RCA1, RCA2, and electron beam evaporated with 100 nm of Cr (Kurt J. Lesker LAB 18, 0.5 A s⁻¹). The following photolithography module for Shipley 3612 resist was used here and in all of following photolithography steps: eight 1 second pulses of hexamethyldisilazane vapor prime at 150°C (Yield Enhancement System), photoresist spun at 4.5 krpm for 30 seconds on a Headway manual spinner, hot-plate baked at 90°C for 1 m, exposed with 15 mJ cm⁻² I-line Karlssuss MJ6 mask aligner, hot-plate baked for 2 m at 110°C, developed for 25 seconds in MF-26A, hot-plate baked 110°C for 1 m, descummed in oxygen plasma for 40 seconds in a 250 W, 150 mTorr, 100 sccm O₂ flow DryTek2 plasma cleaner. Then, the disk was dipped in Transene Chrome Etchant 1020 AC for 1 m, and cleaned in acetone, methanol, and isopropanol. For each step, to ensure process compatibility, the lithography module, process step, and photoresist strip (Gasonics Aura Asher and/or 20 m of piranha etch (120°C 9:1 H₂SO₄: 30% H₂O₂) are done in sequence for the front side, then flipped and the lithography module, process step, and photoresist strip repeated on the back side. The process steps are as follows:

1. Etching alignment marks (500 nm deep, AMT-8100 Plasma Etcher 1600 W, −530 V DC bias, 40 mTorr, 30 sccm O₂, 50 sccm CHF₃)
2. Dry oxide growth (30 nm thick, no patterning, clean in 20 m piranha, 30 seconds 2% HF, 10 m RCA1, 10 m RCA2, and 30 seconds 2% HF with H₂O rinse after each, 900°C dry oxidation 2 hours 40 minutes)
3. Channel doping (30 m bake in 110°C oven, ion implantation with boron $1 \times 10^{13}$ cm$^{-2}$, 60 keV, 7° tilt, Luxience, Inc.)
4. Isolation well doping (30 m bake in 110°C oven, ion implantation with arsenic $2 \times 10^{15}$ cm$^{-2}$, 60 keV, 7° tilt, Luxience, Inc.)
5. Source/Drain contact doping (30 m bake in 110°C oven, ion implantation with boron $1 \times 10^{15}$ cm$^{-2}$, 60 keV, 7° tilt, Luxience, Inc.)
6. Dopant drive-in (no patterning, 15 seconds at 1050°C, 10 sccm Ar, and 1 sccm O$_2$ flow, Allwin Rapid Thermal Annealer)
7. Source/Drain contact etch through oxide (AMT-8100 Plasma Etcher 1600 W RF, –530 V bias, 40 mTorr, 6 sccm O$_2$, 85 sccm CHF$_3$)
8. Gate, source, drain metal deposition (30 seconds dip in 2% HF, H$_2$O rinse, electron beam evaporation of 2 nm Ti and 50 nm Pt at 0.2 nm s$^{-1}$ at 8 e$^{-7}$ Torr pressure)
9. Anneal (no patterning step, forming gas flow 10 sccm for 10 m at 350°C, Allwin Rapid Thermal Annealer)

### 4.3 Laser-cutting ultrathin silicon

We used an Epilog Fusion M2 50 W 1062 nm laser cutter. Substrates on dummy Si wafers were cut repeatedly with lower-power cuts, which prevented edge warping and breakage in comparison with single cuts with slower beam speed. We used 50% power, speed, and frequency corresponding to 25 W over 8-25 μm spot size at 44 m s$^{-1}$.

### 4.4 Ring-on-ring mechanical tests

ABS plastic test rings were fabricated using a Flashforge Creator Pro 3D Printer. Samples were centered on a 55 mm diameter bottom ring. An Instron 5565 compressed a 20 mm diameter ring downwards, measuring the force and displacement.

**CONFLICT OF INTEREST**
The authors declare no conflict of interest.

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**ORCID**
Ruby A. Lai https://orcid.org/0000-0002-4922-5943

**REFERENCES**
1. Wang S, Weil BD, Li Y, et al. Large-area free-standing ultrathin single-crystal silicon as processable materials. Nano Lett. 2013; 13(9):4393-4398.
2. Wong WS, Salleo A. Flexible Electronics, Materials and Applications. New York, NY: Springer Science and Business Media; 2009.
3. Bao Z, Chen X. Flexible and stretchable devices. Adv Mater. 2016;28(22):4177-4179.
4. Shih CW, Chin A. Remarkably high mobility thin-film transistor on flexible substrate by novel passivation material. Sci Rep. 2017;7(1):1147.
5. Ahn JH, Kim HS, Lee KJ, et al. High-speed mechanically flexible single-crystal silicon thin-film transistors on plastic substrates. IEEE Electron Device Lett. 2006;27(6):460-462.
6. Kim DH, Ahn JH, Choi WM, et al. Stretchable and foldable silicon integrated circuits. Science. 2008;320(5875):507-511.
7. Manna AL, Buisson T, Detalle M, et al. Challenges and improvements for 3D-IC integration using ultra thin (25 μm) devices. Paper presented at: 2012 IEEE 62nd Electronic Components and Technology Conference. 2012; 532–6.
8. Knickerbocker J, Andry P, Dang B, et al. 3D silicon integration. Paper presented at: 2008 58th Electronic Components and Technology Conference. 2008.
9. Ferry VE, Verschuuren MA, Li HB, et al. Light trapping in ultrathin plasmonic solar cells. Opt Express. 2010;18(102):A237-A245.
10. Wang KX, Yu Z, Liu V, Cui Y, Fan S. Absorption enhancement in ultrathin crystalline silicon solar cells with antireflection and light-trapping nanocone gratings. Nano Lett. 2012;12(3):1616-1619.
11. Mcmullan G, Faruqui AR, Henderson R, et al. Experimental observation of the improvement in MTF from backthinning a CMOS direct electron detector. Ultramicroscopy. 2009;109(9): 1144-1147.
12. Moldovan G, Li X, Wilshaw P, Kirkland A. Thin silicon strip devices for direct electron detection in transmission electron microscopy. Nucl Instrum Meth A. 2008;591(1):134-137.
13. Schwank J, Ferlet-Cavrois V, Shaneleyt M, Paillet P, Dodd P. Radiation effects in SOI technologies. IEEE Trans Nucl Sci. 2003;50(3):522-538.
14. Bedell SW, Shahjerdi D, Hekmatshoar B, et al. Kerf-less removal of Si, Ge, and III-V layers by controlled spalling to enable low-cost PV technologies. IEEE J Photovolt. 2012;2(2): 141-147.
15. Martini R, Gonzalez M, Dross F, et al. Epoxy-induced spalling of silicon. Energy Procedia. 2012;27:567-572.
16. Nakamura T, inventor; Rohm Co Ltd, assignee. Method for forming SOI structure. US patent 5417180. May 23, 1995.
17. Sevilla GA, Rojas JP, Fahad HM, et al. Flexible and transparent silicon-on-polymer based sub-20 nm non-planar 3D FinFET for brain-architecture inspired computation. Adv Mater. 2014;26 (18):2794-2799.
18. Delachat F, Constacias C, Fournel F, et al. Fabrication of buckling free ultrathin silicon membranes by direct bonding with thermal difference. ACS Nano. 2015;9(4):3654-3663.
19. Gaucher A, Cattoni A, Dupuis C, et al. Ultrathin epitaxial silicon solar cells with inverted Nanopyramid arrays for efficient light trapping. Nano Lett. 2016;16(9):5358-5364.
20. Zoschke K, Wegner M, Wilke M, et al. Evaluation of thin wafer processing using a temporary wafer handling system as key technology for 3D system integration. Paper presented at: 2010 Proceedings 60th Electronic Components and Technology Conference (ECTC) 2010;1385–92.
21. Pargfrieder S, Kettner P, Privett M, Ting J. Temporary bonding and debonding enabling TSV formation and 3D integration for ultra-thin wafers. Paper presented at: 2008 10th Electronics Packaging Technology Conference. 2008;1301–5.
22. Jouve A, Fowler S, Privett M, et al. Facilitating ultrathin wafer handling for TSV processing. Paper presented at: 2008 10th Electronics Packaging Technology Conference. 2008;45–50.
23. Charbonnier J, Cheramy S, Henry D, et al. Integration of a temporary carrier in a TSV process flow. Paper presented at: 2009 59th Electronic Components and Technology Conference. 2009;865–71.
24. Shuangwu MH, Pang DL, Nathapong S, Marimuthu P. Temporary bonding of wafer to carrier for 3D-wafer level packaging. Paper presented at: 2008 10th Electronics Packaging Technology Conference. 2008;405–11.
25. Justin WHST, Chai TC, Rao VS, David SWH, Fernandez DM, Siow LY, Lee WS, Serene MLT, Lee J. Evaluation of support wafer system for thin wafer handling. Paper presented at: 2010 12th Electronics Packaging Technology Conference. 2010;580–4.
26. Yoshida S, Nagai O., inventors; Disco Corp, assignee. US patent 7462094. Dec 9, 2008.
27. Biëck F, Spiller S, Molina F, et al. Carrierless design for handling of ultra-thin wafers. Paper presented at: 2010 Proceedings 60th Electronic Components and Technology Conference (ECTC). 2010;316–22.
28. Spiller S, Molina F, Wolf JM, et al. Processing of ultrathin 300 mm wafers with carrierless technology. Paper presented at: 2011 IEEE 61st Electronic Components and Technology Conference (ECTC) 2011;984–8.
29. Biëck F, Spiller S, Molina F, et al. Integration of carrierless ultrathin wafers into a TSV process flow. Paper presented at: 2010 12th Electronics Packaging Technology Conference. 2010;571–5.
30. Cuffe J, Ristow O, Chávez E, et al. Lifetimes of confined acoustic phonons in ultrathin silicon membranes. Phys Rev Lett. 2013;110(9):095503.
31. Lu Z, Zhu J, Sim D, et al. Synthesis of ultrathin silicon nanosheets by using graphene oxide as template. Chem Mater. 2011;23(24):5293-5295.
32. Kempa TJ, Cahoon JF, Kim SK, et al. Coaxial multishell nanowires with high-quality electronic interfaces and tunable optical cavities for ultrathin photovoltaics. Proc Natl Acad Sci. 2012;109(5):1407-1412.
33. Agrawal AA, Nehilla BJ, Reisig KV, et al. Porous nanocrystalline silicon membranes as highly permeable and molecularly thin substrates for cell culture. Biomaterials. 2010;31(20):5408-5417.
34. Phan HP, Zhong Y, Nguyen TK, et al. Long-lived, transferred crystalline silicon carbide Nanomembranes for implantable flexible electronics. ACS Nano. 2019;13(10):11572-11581.
35. Hartmann R, Strüder L, Kemmer J, et al. Ultrathin entrance windows for silicon drift detectors. Nucl Instrum Meth A. 1997;387(1–2):250-254.
36. Shulaker M, Park R, EE412 Project: NMOS-Depletion Mode Process for EE410. https://snf.stanford.edu/SNF/processes/ee412-projects. Accessed May 1, 2017.
37. Thompson SE, Armstrong M, Auth C, et al. A logic nanotechnology featuring strained-silicon. IEEE Electron Device Lett. 2004;25(4):191-193.
38. Song E, Guo Z, Li G, et al. Thickness-dependent electronic transport in ultrathin, single crystalline silicon nanomembranes. Adv Electron. 2019;5:1900232.
39. Chan TY, Chen J, Ko PK, Hu C. The impact of gate-induced drain leakage current on MOSFET scaling. International Electron Devices Meeting. 1987;1987:718-721.
40. Domke M, Egle B, Stroj S, Bodea M, Schwarz E, Fasching G. Ultrafast-laser dicing of thin silicon wafers: strategies to improve front-and backside breaking strength. Appl Phys A. 2017;123(12):746.
41. Kashyap K, Zheng LC, Lai DY, Hou MT, Yeh JA. Rollable silicon IC wafers achieved by backside nanotexturing. IEEE Electron Device Lett. 2015;36(8):829-831.
42. Navaraj WT, Gupta S, Lorenzelli L, Dahiya R. Wafer scale transfer of ultrathin silicon chips on flexible substrates for high performance bendable systems. Adv Electron. 2018;4(4):1700277.

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