GGArray: A Dynamically Growable GPU Array

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Abstract—This work presents a dynamically growable GPU array (GGArray) fully implemented in GPU that facilitates the programming of GPU applications with dynamic memory. The GGArray is based on an array of LFVectors, taking advantage of the GPU architecture and its synchronization at block level. The GGArray is compared to other state of the art approaches such as a pre-allocated static array and a semi-static array that needs to be resized through communication with the host. Experimental evaluation shows that the GGArray achieves an efficient memory usage close to the optimal and not greater than $2\times$ the needed memory, as well as a competitive insertion/resize performance, but it is slower for regular parallel memory accesses. Given these results, the GGArray is a potentially useful structure for applications with high uncertainty on the memory usage as it does not require pre-allocating GPU VRAM for the worst case scenario. It can also be useful in applications that exhibit phases in terms of memory behavior, such as an insertion phase followed by a regular r/w GPU phase. In these cases, the GGArray can be used for the first phase and then data can be flattened for the second phase in order to allow the regular and faster GPU memory accesses to take place. These results constitute a step towards achieving a parallel efficient C++ like vector for modern GPU architectures.

Index Terms—GPGPU, Dynamic Array, Dynamic Memory, Parallel Algorithms

I. INTRODUCTION

GPUs have become a great contribution in HPC, scientific simulations and other applications because of their high parallel performance and energy efficiency [14]. Furthermore, recent GPU improvements such as tensor cores and ray tracing cores have cemented their use in certain areas that receive an even greater benefit from these technologies. GPUs are especially useful when dealing with grid-like structured data such as arrays or matrices, offering up to an order of magnitude of speedup over a CPU based approach. It is also known that when dealing with graphs, sparse matrices and other irregular structures that do not follow a static grid-like layout, the GPU speedup is not as high because of several memory access performance penalties [4].

This problem also extends to the use of dynamic memory. Given the impossibility to maintain data contiguously in memory when dynamically allocating it without any kind of global synchronization, it is natural that the use of dynamic memory does not provide the same speedups as the ones obtained with static structured data. Although there are several studies on graph algorithms and sparse matrices [1], [3], [12], [17] for GPUs, some of which also explore the use of dynamic memory, there has not been an attempt to implement a more general dynamic array that works on GPU. Dynamic arrays, such as for example C++ vectors, are one of the most commonly used structures in programming languages and some of them do not even include static arrays in their standard library (e.g., python). Dynamic arrays provide an easier way of programming and allow simpler code designs due to its capacity to grow or shrink as required during execution.

This simplicity is a valuable feature for a large community who’s work is more focused on developing an application than a tool, i.e., their effort should not be focused on writing the needed data structures. A significant part of the scientific community has these requirements as they focus on the study of certain phenomena that requires the use of intensive computer simulations accelerated by GPU libraries. Currently, it is highly difficult to take advantage of the benefits of dynamic arrays on GPU, and when it is absolutely necessary, it requires a significant amount of low-level programming effort. Also, in many cases this programming effort results in a handmade structure for an specific application, to some degree, making it unusable for other applications. Having a general purpose dynamic array for GPUs would improve the programming model substantially, however, accomplishing an efficient one for GPUs is considered a difficult challenge [15].

One of the first aspects to consider in dynamic arrays is that they are by design slower than static ones due to the work required to maintain data integrity after each operation, especially on GPUs where it is necessary to deal with thousands of parallel operations. In exchange, it offers a more efficient use of VRAM memory, due to its capacity to adjust its size to the amount of data contained at each moment of the execution. This efficient memory usage allows to run more applications simultaneously in a GPU, via concurrent kernel execution, as long as the peak memory consumption doesn’t occur at the same time. Much of the knowledge in parallel dynamic arrays has come from the LFVector [6] structure proposed in 2006, which is one of the first works that describes an implementation of a parallel dynamic array for CPUs.

This work proposes a dynamically growable array for the GPU, named GGArray, which is based on the LFVector...
idea adapted to the massive parallelism programming model. The structure is divided into blocks, exploiting the asynchronous advantage of GPU thread blocks and diminishing global synchronization issues, however at the cost of having a slower access to its elements. An experimental evaluation is performed in terms of performance and memory usage, showing competitive insertion performance and a more efficient memory usage when compared to other approaches such as static and semi-static arrays. The GGAArray is a first step into the construction of a data structure with an interface similar to the C++ vector that works on a massively parallel architecture.

The remaining sections cover related work (Section II), current approaches for array data structures and insertion schemes (Section III), the presentation of the proposed GGAArray (Section IV), a theoretical analysis of memory usage (Section V), an experimental evaluation (Section VI) and conclusions (Section VII).

II. RELATED WORK

While there is no openly available general dynamic array fully implemented in GPU, there are implementations of resizable GPU arrays from the host and a significant amount of research on parallel arrays for multi-core CPUs. Also, there are works that implement hand-tailored GPU-based dynamic memory management for specific scientific applications.

A. GPU Resizable Arrays

The closest data structures to a dynamic array on a GPU device are offered by the libraries Thrust [2] and stdgpu [18], but none of these manage the dynamic operations fully in GPU. Thrust is a well known CUDA library that implements useful data structures to simplify CUDA programming. Among these structures are host_vector and device_vector, dynamic arrays that reside on the host and device memory respectively. But device_vector works like a doubling array and its resizing methods can only be called from the host. On the other hand, there is stdgpu, that implements data structures from the C++ STL in CUDA. In this case the vector implementation allows operations to be called from the device, push_back being one of them, but they are implemented with locks, penalizing the potential benefits from parallelization.

B. General Parallel Dynamic Array

Lock-Free Vector (LFVector) [6] was the first proposed parallel dynamic array and the catalyst for further research on them. It proposes an idea similar to doubling arrays by duplicating the size each time more memory is needed. Differently from doubling arrays it abandons the idea of storing an array contiguously, and divides it into buckets. This difference is important as it avoids the necessity of moving the elements to the new array when resizing, and doesn’t require as much synchronization between the distinct threads.

Further research on the topic include improvements to the LFVectors, such as the Wait-Free Vector [7] and new approaches like RCUArray [11] which uses the Read-Copy-Update mechanism. From the point of view of massive GPU parallelism, one drawback of the mentioned arrays is that some of their stages rely on synchronization mechanisms thought for CPU architectures, not for GPU ones.

C. GPU Synchronization

Global synchronization is usually avoided in the GPU, because of the overhead that it introduces. Unfortunately, in some cases it is highly difficult to avoid it. The simplest way to synchronize all threads is by dividing a parallel application into several kernels and using the host as a synchronization barrier. This design makes any data update operation to travel between the host and device in both directions, which can become a performance bottleneck. Because of this, efficient GPU implementations should try to find designs that make synchronization occur inside the device, even if it requires doing it at block-level and not globally.

Research on synchronization includes Fast Barrier Synchronization [21] and methods proposed for memory allocation [8] among others. The first work proposes two algorithms for inter-block synchronization. A lock-based method with the use of atomic operations and a lock-free one, which dedicates one block of threads and global memory to indicate whether threads from other blocks are allowed to pass the barrier. The second work focuses on memory allocation, which they separate into two stages. In the first stage, accounting the available resources, global synchronization is needed, for which they implement semaphores that allow concurrency in the critical section diminishing the principal bottleneck of semaphores. The work also highlights the importance of global synchronization when dealing with dynamic memory or memory allocators.

D. GPU Memory Allocators

Winter et al. (2021) [20] compared and evaluated various memory allocators for NVIDIA GPUs including the allocator provided by the CUDA-Toolkit and non-proprietary allocators starting from XMalloc [10] and ScatterAlloc [15] up to Ouroboros [19], one of the latest. Although this work does not focus on proposing a new memory allocator, they are relevant as potential tools that can complement and improve the ideas of this work.

E. Specific GPU Dynamic Applications

When a GPU application requires a dynamic array or similar solution, many times it implements an specific and hand-tailored structure that suits the application needs. A common example is when working with triangular meshes [9], [13]. In the first work authors introduces a general idea, using parallel prefix-sum to obtain the indexes at which each threads inserts an element. On the other hand, the second work instead of dealing with dynamic memory, introduces handles to each of the graphs elements in a way that modifying the handles offers a similar result to managing dynamic memory.

Given these works, it is clear that a generic vector-like structure is still missing in GPU programming. Specially one with the capacity of being resized dynamically, competitive
in performance, and able to take advantage of asynchronous parallelism as well as adapt to the GPU architecture. In this work, we focus on studying the growing aspect of such desired structure.

III. CURRENT KNOWN GPU APPROACHES

The design idea for a parallel growable array can be divided into two parts. The first part consists of the data structure, as well as how it is resized when needed and the second part consists of how elements are inserted in the array.

A. Known GPU Data Structure Approaches

Two approaches are known for growable GPU arrays:

1) Static: The static data structure consists of a flat C like array allocated with `cudaMalloc` at the start of the program and insertions can occur in a GPU kernel by each thread using a parallel insertion algorithm. This approach does not support any kind of resize operation and it is necessary to know the maximum possible size beforehand for it to not result in a segmentation fault. For many GPU applications, this is the default way of managing a dynamic growth of memory.

2) Semi-static: Similar to the static approach, a C array is utilized as the base structure, but with mechanisms to grow its size via memory reallocation and synchronization from the Host, which allows to use resizing schemes such as the one from doubling arrays. Another possibility is to use a low-level API for virtual memory management provided by CUDA [16], which allows skipping the data copy between doubling arrays. The low-level CUDA API offers functions to modify the mappings between virtual and physical memory. This allows to allocate only the desired extra memory and remap the virtual memory in such a way that indexing is contiguous even if the elements are not physically contiguous. It is worth mentioning however that this benefit comes at the cost of some fragmentation in GPU memory.

B. Known GPU Parallel Insertion Approaches

The main objective of the parallel insertions algorithms is to allow multiple threads to insert data and consistently update the global size of the array. This involves giving each inserting thread a unique index greater than the previous size and less than the subsequent size, such that each thread inserts its element in a different position as if it was a contiguous array. Three approaches have been identified for GPU architectures.

1) Atomic: The simplest way of obtaining a unique position for each new element is to use the CUDA instruction `atomIc Add`, which takes as parameters a memory address and an addend. It returns the value stored in the address and updates its value by adding the addend. For the insertion algorithm each inserting thread adds 1 to the size of the array, obtaining an index where to insert the element and updating the size of the array.

2) Parallel Prefix-sum: A more parallel approach for inserting elements consist of considering numbers of insertion per thread as an array with 0s or 1s depending if the threads need to insert an element and calculating the prefix-sum of this array. In CUDA this can be implemented locally per block with the warp `__shfl_up_sync` instruction and globally with atomic operations.

3) Tensor-cores Parallel Prefix-sum: As demonstrated by Dakkak et al. (2019) [5] it is possible to further accelerate the prefix-sum computation with CUDA tensor cores by representing the work as matrix multiplications. Although this approach works better on dense problems with a many-to-one mapping between data and threads, respectively, it is still a motivation to consider it in this work and know how efficient is this new use case for tensor cores outside machine learning.

All these known approaches are taken into account when proposing a new data structure for a growing array fully on GPU. In terms of data structure, the goal is to have a fully dynamic one that can update during kernel execution (static and semi-static cannot, therefore their role is for comparison purposes), and for the insertion approach all three are evaluated in order to choose the fastest one to be used in the new GGArray structure.

IV. PROPOSING GGArray

In this section we introduce GGArray, a fully dynamic GPU structure with an interface similar to an array based on the LFVector dynamic data structure which was originally proposed for CPU architectures. The LFVector is based on the idea of doubling arrays, where the size of the array is doubled whenever more space than its current capacity is needed. This doubling is usually done by creating a new array with double the size and moving all elements of the previous array before deleting it. However, when multiple threads are accessing the elements of the array at the same time, having two copies introduces a synchronization problem as it is necessary for all threads to know when the array changes. The LFVector eliminates this problem by dividing the array into non-contiguous blocks, each double the size of the previous one, and allocating them when needed.

The original idea of the LFVector lies on the use of Compare-And-Swap (CAS) with every thread trying to allocate memory and deleting all except from the first allocated memory. This mechanism is not suitable for GPUs, given that there is not enough memory for thousands of threads to try allocating a doubled buffer before knowing which one succeeded. Another way would have been to use the busy waiting logic for the threads to synchronize when allocating memory, but this approach only works inside a block, where there is a high synchronization between threads, and not among blocks. For multiple thread blocks deadlocks can occur as the swapping between busy and idle blocks can make the allocating block become swapped out by the busy ones, locking the execution for an unknown amount of time. There are two ways to solve this problem, the first is globally synchronizing all the blocks and the other is avoiding the
synchronization by dividing the data structure. We opted to further divide the array and take advantage of the block independent execution by creating a macro structure made of multiple LFVectors, one for each block of threads as illustrated in Figure 1.

Although this design limits the parallelization of the problem as there is a fixed number of threads that can work on each block, it does not add additional limits to the number of blocks neither the amount of data to be processed in each block (i.e., thread coarsening can be applied so that more work is assigned to each thread). Also the amount of GPU cores is increasing in recent GPU architectures (Ampere, Lovelace), reaching the tens of thousands, therefore the larger the array of LFVectors, the less noticeable this parallel limit will be perceived. This design also allows to synchronize LFVectors with builtin CUDA instructions. The formal diagram for the structures is shown in Figure 2.

The functionalities are shown in Algorithms 1 and 2.

**Algorithm 1** LFVector push_back

Requires: e

idx = get_insertion_index()
b = get_bucket(idx)
if bucket[b] = nil then
    new_bucket(b)
end if

synchronize()
vecto(idx) = e

**Algorithm 2** new_bucket for an LFVector

Requires: b

if not CAS(is_bucket(b), False, True) then
    bsize = 2^log(first_block_size)+b
    bucket[b] = malloc(bsize * type_size)
end if

Given that each LFVector is constrained to its own block, the dynamic array requires a new structure to keep track of its size and the ranges encompassed by each LFVector. This structure is a prefix-sum of the sizes of all LFVectors, it contains the index of the first element contained by them. We are using a C-style array, which offer great amount of parallelism for updating its values, but it is needed to search over this array to locate the LFVector that contains a certain index. Using a prefix-sum allows us to partially reduce the time needed for this search using binary search.

The insertion method for the GGArray consists of delegating the process to each of the LFVectors. At a global level, it only needs to update the global size and prefix-sum indices, as the actual push_back insertions are taken care locally by the LFVectors during kernel execution. The source code is available on Github.

V. THEORETICAL MEMORY USAGE

A major advantage of the GGArray is its ability to dynamically grow during kernel execution according to the needs of the application. This allows programmers to run applications without concern about the amount of memory to pre-allocate nor if the program will fail due to an invalid memory address. This is not a big issue for static methods when it is known beforehand the insertion behaviour of each thread, however, when there is not enough information or there is only a rough idea of the growing behaviour of the array, the worst case for the static or semi-static methods start to grow excessively. Figure 3 shows the memory needed for an example where the amount of insertions are given by the size of the array times a factor given by a log-normal distribution with parameters $\mu = 0$ and $\sigma \in [0, 2]$.

It shows how with a larger standard deviation and uncertainty about the amount of insertions realized, more memory it is needed for the static method to fail only 1% of the times it is executed. On the other hand, GGArray remains closer to the optimal amount of memory needed, reaching in the worst case approximately $2\times$ more. Note that in the case of only one kernel call the behaviour of a semi-static structure (e.g. memMap) the behaviour is the same as a static structure. The main difference between these two is that while a static structure needs to account for the worst case of the whole program, a semi-static structure only needs to cover the worst case of a single kernel call, adjusting its size before the call. On the other hand, GGArray can grow as needed in the device as long as there is enough memory.

VI. EXPERIMENTAL EVALUATION

All performance tests were ran on the TITAN RTX and A100 GPUs. Their specifications are listed in Table I.

| TABLE I |
| GPUS SPECIFICATIONS |
| TITAN RTX | A100 |
| CUDA Cores | 4608 | 6912 |
| Tensor cores | 576 | 432 |
| Memory | 24 GB | 40 GB |
| FP16 performance | 32.62 TFLOPS | 77.97 TFLOPS |
| FP32 performance | 16.31 TFLOPS | 19.49 TFLOPS |
| Boost Clock Speed | 1770 MHz | 1410 MHz |

A. CHOOSING THE FASTEST INSERTION ALGORITHM

The static array was used as the structure to test the different insertion approaches. The reason for not testing with the other structures is that insertion algorithms are independent of the underlying structure and the static array is the simplest, allowing to only measure the time of the insertion algorithm without being affected by the time needed to access the structure elements. The test consists of an array with 1e6 elements and a sufficient capacity for duplicating its size 10 times, finishing with an array of 1.024e9 elements. Time is measured for each iteration of duplication. Figure 4 (first
Data block #1
Data block #2
Data block #3

LFVector 1
LFVector 2

Fig. 1. In GGArray, one LFVector per data block is used. This allows to correlate each data block with a thread block independently.

Fig. 2. GGArray structure, each LFVector maps to a GPU block and it is independent from other LFVectors.

Fig. 3. Theoretic memory usage of GGArray and the static/semi-static arrays.

column) shows the results for the algorithms using atomic operations, warp-shuffle prefix-sum and tensor-core prefix-sum. Insertions with atomic operations were the slowest, while the shuffle scan is the fastest closely followed by the tensor core one.

Regarding the scan operation being slower when implemented with tensor cores than with the usual algorithms, as opposite from other studies in the state of the art, it is due to not meeting the necessary workload for this specific case. For this particular test, the size of the problem for the insertion algorithm is the amount of threads participating in the insertion. Thus, when using tensor cores that multiplies 16x16 matrices per warp, there are not enough elements to fill all matrices from all warps. In the tensor scan algorithm only one eighth of the warps are computing the algorithm while the rest are idle, not taking advantage of the full potential of tensor cores. Other applications with a higher ratio of data elements to threads could exhibit an scenario where the tensor core approach runs faster. It is also important to note that the difference between the two scan versions is lower in the A100 GPU, due to the improvement in tensor cores from the previous generations being larger than the improvement in CUDA cores.

B. Choosing An Optimal Number of LFVectors

The variables that affect time execution of the GGArray are its size, the amount of blocks in which it is divided and the amount of memory allocations previously realized. The size impacts read/write and insertion operations since the more elements the array contains, more operations are needed to operate over the whole array. Similarly, more concurrent blocks allows a larger amount of parallelization in these operations, except for atomic ones. In the case of memory allocation more parallelization means more allocations which do not occur in parallel due to the limitations of current technology. We ran tests to determine the optimal amount of blocks, with the results shown in Figure 4 (second and third columns). The Figure shows the amount of time it takes to duplicate the amount of elements in the array utilizing different numbers of blocks. The duplication process includes the memory allocation and insertion of elements. The plots of the third column show the time spent to realize read/write operations in two ways. The first one (rw_g) utilizes the structure as if it were an array with one thread per element. On the other hand, rw_b follows the block structure and uses one GPU block per array block avoiding the process of determining which block contains an element which is slow. In general, a low number of blocks implies the growth of the structure is slower due to the lack of parallelization in insertion, reaching optimal configurations at 32 and 512 blocks. With over 32 blocks, read/write operations by block are faster and their time is inversely related to the number of blocks.

C. Growable Array Operations

The experiment to test the performance of array operations consists of starting with an array of size 1e6 and duplicating (with scan algorithm) its size 10 times. Inserting less elements than the size of the array doesn’t reduce the time taken, because even threads that do not insert elements play a role in the insertion algorithm and are also needed for synchronization. The duplication of the array is divided in the grow operation and the insertion operation. Also, for each size the time to operate on each of its elements is measured. The results are displayed in Figure 5. Moreover, Table II shows the exact time
taken by each operation on the last iteration. In accordance to the previous results, 32 and 512 blocks are utilized for read/write operations per block. In the legend, GGArray32 and GGArray512 correspond to the variants of the proposed structure with the numbers of blocks in which it is divided, and memMap is the semi-static array using the NVIDIA low-level memory management API. The first two figures show the time to duplicate the capacity of the arrays. The two in the middle depict the time needed for the insertion of elements filling the capacity of the array. The last column of plots displays the time required to realize operations in all elements of the array. The operation used is a kernel that adds +1, 30 times to each element.

TABLE II
TIME (MS) TO DUPLICATE AN ARRAY OF SIZE 5.12e8 IN THE LAST ITERATION USING NVIDIA A100

|        | grow | insert | read/write |
|--------|------|--------|------------|
| static | —    | 7.07   | 6.27       |
| memMap | 5.21 | 7.87   | 6.28       |
| GGArray512 | 8.76 | 11.79  | 69.73      |
| GGArray32 | 0.52 | 27.90  | 198.32     |

It draws attention that the third resize barely takes time. The explanation is that the growth in capacity of the GGArray is not a constant factor, but it tends to grow with the capacity from the previous iteration. The major drawback of the proposed structure are the slow read/write operations. While allocating memory for a large amount of LFVectors and inserting elements are slower than the other structures, the difference is not large enough to cause a bottleneck, especially when realizing more complex operations in-between resizing. However, in order to realize application work with the contents of the structure it is necessary to read and write its elements, and these operations are slow, currently more than 10 times slower, even when working by block without the need to search which LFVector contains each element. This is produced by the more complex indexing operation, a worse cache locality and the need to pass over multiple pointers to reach an element. Something that may only be resolved by a truly contiguous array.

Still, there are some applications that may benefit from the GGArray structure. For applications that need a dynamic array and that do not have a way to confidently know beforehand the maximum size, or the uncertainty of the maximum size is big enough, our structure offers a way to dynamically grow the array from inside the kernel and using no more than double the necessary memory. Also, applications that can be defined in phases where one phase only inserts elements and the other phases realize work on a static structure could be benefited by moving the elements between our structure and a static array. This reduces the read/write operations to only a few per each growth phase and can still take advantage of the characteristics of static arrays in work phases. Applications that meet these conditions may be encountered in computer geometry and triangular mesh refinement.

D. Case study: Two Phase Application

Figure 6 shows the speedup of GGArray over memMap for a two phase application. The work phase simply consists of a kernel that adds 1 to every element of the array called multiple times (between 1 and 1000) corresponding to the X axis of the plot. The results illustrate how the overhead added by the dynamic structure can be disregarded when the amount of
In this work we proposed GGArray, a fully dynamic array for the GPU that offers the interface of a growable array and works inside the GPU without the need of synchronizing through the host. This allows to allocate memory when required from kernel code without the need to pre-allocate all necessary memory. The GGArray has one important drawback; its slow access to the elements, which makes it still unsuitable as a general purpose array. Nonetheless, there are certain applications where it can still prove to be useful, such as where dynamic allocation is crucial, or applications that can be divided into phases where most work is static and the insertion can be done in a separate stage. Also, it is important to note that this structure affects the programming of CUDA kernels to some degree, due to the per-block design which requires threads to stay in execution for warp synchronization and insertion algorithms.

Further improvements are needed for accessing elements faster, one idea that should improve performance significantly is to make GGArray use the L1 cache (programmable shared memory) for segments of the array. In addition, it would be interesting to depart from the relation in the data structure with CUDA thread blocks by using cooperative groups. Also, NVIDIA has made progress in favor of dynamic applications in the last years, for example RT cores, and currently they are being researched as a computation tool outside ray tracing. This may be an interesting approach to implement a dynamic data structure. On the other hand the issue of accessing elements does not exist if a contiguous array is utilized, although it brings a lot of synchronization issues, that could be solved with cooperative groups in combination with the recent thread block clusters introduced with the Hopper GPU architecture. NVIDIA has also recently unlocked the GPU System Processor, a chip similar to a CPU, but inside the GPU. This processor could bring a lot of benefits if it is used for synchronization instead of the CPU. Finally, separating the data structure and allocation from the insertion algorithm leaves open the possibilities for the use of any scan algorithm already studied or even other algorithms that outputs an unique index per thread.

VII. CONCLUSIONS AND FUTURE WORK

In this work we proposed GGArray, a fully dynamic array for the GPU that offers the interface of a growable array and works inside the GPU without the need of synchronizing through the host. This allows to allocate memory when required from kernel code without the need to pre-allocate all necessary memory. The GGArray has one important drawback; its slow access to the elements, which makes it still unsuitable as a general purpose array. Nonetheless, there are certain applications where it can still prove to be useful, such as where dynamic allocation is crucial, or applications that can be divided into phases where most work is static and the insertion can be done in a separate stage. Also, it is important to note that this structure affects the programming of CUDA kernels to some degree, due to the per-block design which requires threads to stay in execution for warp synchronization and insertion algorithms.

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