Characterization of an architecture for front-end pixel binning in an integrating pixel array detector

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ABSTRACT: Optimization of an area detector involves compromises between various parameters like frame rate, read noise, dynamic range and pixel size. We have implemented and tested a novel front-end binning design in a photon-integrating hybrid pixel array detector using the MM-PAD-2.0 pixel architecture. In this architecture, the pixels can be optionally binned in a $2 \times 2$ pixel configuration using a network of switches to selectively direct the output of 4 sensor pixels to a single amplifier input. Doing this allows a trade-off between frame rate and spatial resolution. Tests show that the binned pixels perform well, but with some degradation on performance as compared to an un-binned pixel. The increased parasitic input capacitance does reduce the signal collected per x-ray as well as increases the noise of the pixel. The increase in noise is, however, less than the factor of 2 increase one would observe for binning in post-processing. Spatial scans across the binned pixels show that no measured signal intensity is lost at the inner binning unit boundaries. In the high flux regime, at a $2 \times 2$ pixel wide beam spot (FWHM) size, binned mode responds linearly up to a photon flux of $10^7$ x-rays/s, and performs comparably with un-binned mode up to a photon flux of $10^8$ x-rays/s. While this study demonstrates a proof of concept for front-end binning in integrating detectors, we also identify changes to this early-stage prototype which can further improve the performance of binning pixel structures.

KEYWORDS: Electronic detector readout concepts (solid-state); Front-end electronics for detector readout; Hybrid detectors; X-ray detectors

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1 Introduction

One of the major advantages presented by hybrid pixel array detectors (PADs) is that the separate sensor and readout layers can be optimized independently of each other. Important specifications of an area detector include frame rate, read noise, dynamic range, and pixel size. The design of an area detector inevitably involves some degree of compromise and trade-off between parameters as not all can be optimized in a single device. For example, frame rate tends to trade off with number of pixels and noise, both because more pixels require more time to read out through a given number of data channels and because electronic noise tends to increase with bandwidth. One way to cover a wider range of use cases is to make some of these trade-offs selectable, for example by allowing the user to choose to read out fewer bits in exchange for a higher frame rate at the expense of dynamic range [1, 2], or by allowing the user to choose to bin sets of pixels together, i.e., trading spatial resolution for increased frame rate.

In the test structures evaluated in this paper, we have implemented the latter approach in the readout ASIC (Application Specific Integrating Circuit) for a photon-integrating hybrid pixel array detector. We describe the design and characterization of an architecture for front-end binning in an integrating framework, wherein the pixel array can be optionally operated with pixels binned in a $2 \times 2$ configuration for a potential factor of 4 improvement in frame rate. Because the binning architecture chosen involves additional circuitry on the pixel front end, it has potential impact on important parameters such as read noise, effective gain and integrator slew rate.

Previous studies have investigated pixel binning in various kinds of x-ray detectors [3]–[13]. Pixel binning implemented before the charge-to-voltage conversion node has been common in
CCDs [4, 5]. Additionally, binning during post-processing of data using various algorithms has been well established [6]–[8]. Medipix3 is an example of a PAD which can be operated in “charge summing” mode, where signal from neighboring pixels are added together before readout [9]–[13] in order to deal with charge sharing between pixels. The impact of binning on read noise depends on the way binning is implemented. In typical CCD binning, where the integrated charge is summed before being converted to voltage by the readout amplifier, the read noise associated with a binned pixel unit is equal to that of an un-binned pixel. On the other hand, if binning is performed during post-processing, the read noise of each pixel within the binning unit adds in quadrature, which for a $2 \times 2$ binning unit translates to an increase in noise by a factor of 2. Through our measurements, we show a significant improvement over this factor of 2 in noise enabled by our novel front-end binning architecture. In the following sections we describe this design, as well as measurements using a low-flux lab x-ray source to characterize its gain, noise and spatial response, and using a high-intensity synchrotron radiation source to characterize the high-flux performance.

2 Front-end binning architecture

2.1 Pixel design

Pixel binning has been implemented in a portion of a $16 \times 16$ pixel test chip using a version of the MM-PAD-2.0 pixel design described in [14]. This pixel is a successor of the original Mixed Mode Pixel Array Detector (MM-PAD) developed at Cornell [15, 16]. While [14] described an MM-PAD-2.0 variant with adaptive front-end gain, the pixel variant used here implemented a fixed front-end gain for the sake of simplicity. A single-pixel schematic is shown in figure 1.

![Figure 1. Single-pixel MM-PAD-2.0 schematic, showing the fixed-gain variant used here. The sensor is represented by a diode on the pixel input node. The binning structures are omitted in this schematic. The front-end feedback capacitance $C_F$ is implemented as a metal-insulator-metal (MiM) capacitor. The input capacitance $C_{in}$ is shown for reference, and is comprised of the sensor capacitance, bond capacitance, and parasitic contributions from various CMOS components in the pixel. The load capacitance $C_L = 300$ fF is dominated by the MiM capacitors in the dual track-and-hold circuit.](image)

The MM-PAD family of pixels all use a photon-integrating pixel front-end coupled with a charge removal mechanism to achieve an extended dynamic range. A relatively small integration
capacitor (in the MM-PAD-2.0 pixel, 40 fF) is used to maintain reasonable single-photon resolution in the low-signal regime. When the output of the front-end integrator reaches an externally-set threshold $V_{th}$, a charge removal circuit is triggered and removes a fixed amount of charge from the integration capacitor, without interrupting integration of additional incoming photocurrent. In the MM-PAD-2.0 pixel, charge equivalent to about 400 keV total deposited energy is removed per charge removal operation. An in-pixel counter keeps track of the number of charge removals in a given exposure. At the end of an exposure, the counter value as well as the residual analog voltage at the integrator output are both read out. In a fully-calibrated system, the digital and analog portions are scaled together to reconstruct the total signal detected during the exposure. Dual track-and-hold circuits and dual in-pixel counters are used to achieve readout with approximately 98% duty cycle [17].

![Figure 2](image)

**Figure 2.** Schematic of a four-pixel binning network. The four amplifiers shown are the input amplifiers of figure 1 for 4 adjacent pixels. For simplicity, only the front-end integrator of each pixel is shown, with the pixel reset switch (shown in figure 1) omitted. When binned, all four pixels act as a “super-pixel” that is read out through a “master pixel” amplifier (lower right).

Figure 2 shows the four-pixel binning scheme. In general, the input capacitance of the pixel, $C_{in}$, depicted in figure 1, has contributions from CMOS parasitics on the ASIC, the capacitance of the pixel bond pad to the ASIC substrate, the capacitance of the sensor, and contributions from the bond itself. Compared to a pixel with no binning structures, the binning switches themselves add a small additional parasitic capacitance which is present whether binning is on or off. Also, when binning is enabled the master pixel sees additional capacitance from each of the other three pixels in the $2 \times 2$ binning unit, consisting of the sensor and bond capacitances plus any CMOS parasitics that are upstream of the binning switches.

Increasing $C_{in}$ has the effect of decreasing the apparent gain of the pixel front-end by reducing the charge collection efficiency of the amplifier. Incoming photogenerated charge from the sensor
is not purely integrated onto the feedback capacitor $C_F$ but instead split between $C_F$ and $C_{in}$. The charge collection efficiency is given by

$$\text{CCE} = \frac{(1 + A)C_F}{C_{in} + (1 + A)C_F}$$  \hspace{1cm} (2.1)$$

where $A$ is the open-loop voltage gain of the amplifier. This can be viewed as an equivalent decrease in gain assuming the ideal case of zero $C_{in}$ and an effective feedback capacitance of $C_{F,\text{eff}}$ given by

$$C_{F,\text{eff}} = \frac{C_F C_{in} + (1 + A)C_F}{(1 + A)C_F}.$$  \hspace{1cm} (2.2)$$

In the pixel under consideration here, $A$ is approximately 40 and $C_F$ is 40 fF. $C_{in}$ is empirically determined to be 484 fF for un-binned mode and 767 fF for binned mode, as shown in section 3.2.

An increase in $C_{in}$ when binning is switched on is also expected to increase the noise seen at the pixel output node. This noise has contributions from the amplifier itself (i.e., transistor thermal and flicker noise) and from switching noise associated with the opening of the pixel reset switch (shown in figure 1) at the start of an exposure. A quantitative estimation of these relative noise contributions is beyond the scope of this paper; detailed considerations of the impact of $C_{in}$ on amplifier noise and switching noise can be found in [18] and [19, 20], respectively. A brief qualitative discussion of the expected dependence on $C_{in}$ follows.

We will refer to the combination of these noise sources, and any others in the analog readout chain, as the pixel read noise. In the context of an x-ray detector, it is useful to consider the read noise in units of equivalent noise charge, since this allows for quick comparison with the signal produced by an individual x-ray stopped in the sensor, which is given in units of charge by the ratio of the x-ray energy to the energy required to produce an electron-hole pair in the sensor (3.65 eV in the case of silicon).

The integration of charge $Q$ onto $C_{F,\text{eff}}$ produces a change in voltage $V = Q/C_{F,\text{eff}}$ at the pixel output. As such, the output-referred amplifier voltage noise $V_{n,\text{amp}}$ can be interpreted as an equivalent noise charge $Q_{n,\text{amp}} = C_{F,\text{eff}}V_{n,\text{amp}}$. $V_{n,\text{amp}}$ is given by

$$V_{n,\text{amp}}^2 = S \frac{G_m(C_F + C_{in})^2}{(C_F + C_{in})C_F C_L + C_F^2 C_{in}}$$  \hspace{1cm} (2.3)$$

where $S$ is the power spectral density of the amplifier noise as seen as a voltage source at the non-inverting input and $G_m$ is the amplifier transconductance. $S$ and $G_m$ are properties of the amplifier itself, and are unchanged by the state of the binning switches. Since $C_F$ and $C_L$ are also fixed, an increase in $C_{in}$ will lead to an increase in $V_{n,\text{amp}}$. Furthermore, from equation (2.2), the effective feedback capacitance $C_{F,\text{eff}}$ also increases with $C_{in}$. These factors together lead to an increase in $Q_{n,\text{amp}}$, the amplifier’s contribution to the total pixel read noise.

The switching noise associated with the opening of the pixel reset switch at the beginning of an exposure, also referred to as the pixel’s $kTC$ noise, can be understood as arising from sampling, at the moment the reset switch opens, the thermal fluctuation of charge on the capacitors connected to the pixel input node. This gives a contribution from $C_{in}$ to the pixel read noise, in units of equivalent noise charge, that scales as $\sqrt{kTC_{in}}$ [19–21]. Because the binning switches (shown in figure 2) are configured to be either open or closed while the pixel is in reset before the start of an exposure, and
do not switch states during an exposure, they do not contribute switching noise to the total pixel read noise.

A third contribution to the read noise arises from the injection of charge from the reset switch onto the pixel input node when the switch is opened at the start of an exposure [22]. This results in a noise charge contribution that depends on the switch size and is expected to be independent of $C_{in}$. However, because the reset switches in the pixel examined here are large, this contribution to the read noise is significant and may be on par with the amplifier noise charge $Q_{n,amp}$. Circuit simulations suggest that these two noise sources dominate over the $kT\!C$ noise in the pixel examined here.

2.2 Small-scale detector system

A small-scale detector module was assembled consisting of a $16 \times 16$ pixel readout ASIC stud bonded (Polymer Assembly Technology, Michigan, U.S.A.) to a 500 $\mu$m thick Si sensor (SINTEF, Oslo, Norway) with a pixel pitch of 150 $\mu$m $\times$ 150 $\mu$m. The detector module was wire-bonded into a ceramic pin grid array package, which can be plugged into a zero-insertion force socket on a host PCB that supplies power, current and voltage biases. A Virtex 6 FPGA resident on a Xilinx ML605 development board handles detector control waveform generation and data capture. Captured data is assembled into frames and transmitted to a host computer over Ethernet for storage and analysis.

During operation, the detector module temperature is held at $-20^\circ$C via a thermoelectric cooler. To prevent water condensation, vacuum is maintained around the detector via a “clamshell” housing with an x-ray transparent window fitted around the detector module. Figure 3 shows the wire-bonded detector inserted in the socket (left), and the vacuum housing with the host PCB and ML605 board (right).

Within the ASIC, the pixels are organized into four banks of $4 \times 16$ pixels each. Each bank is a variant of the MM-PAD-2.0 pixel and each has its own analog and digital readout channel. Binning is implemented only on one bank (“bank 1” in this report). A neighboring bank (“bank 2”) has an identical pixel design with no binning structures. Both of these banks have a 40 $\text{fF}$ feedback capacitor with no adaptive gain.

![Figure 3](image-url). (Left) Wire bonded chip with attached sensor in a pin grid array package. (Right) “Clamshell” vacuum housing mounted around the detector socket, to provide a condensation free environment for testing the system at low temperatures. A bottom portion of the clamshell (below the printed circuit board and not seen in the figure) houses a thermoelectric module used to cool the detector.
3 Low-flux characterization

The gain and noise of the detector in binned mode and un-binned mode were measured and compared. The spatial response of the 2 × 2 binning unit was also tested by raster scanning x-rays across the detector using a tungsten pinhole mask.

3.1 Signal measurement and analysis method

The signal from a MM-PAD-2.0 pixel consists of a digital number corresponding to the number of charge removal steps, plus the analog value remaining on the output of the charge integrator at the end of the frame. The analog values are digitized to 14 bits and are scaled to and combined with the digital counts to produce a wide-dynamic-range intensity value, here reported in Analog-to-Digital units (ADU) of the analog measurements. The output is offset corrected by subtracting the average of multiple dark frames taken with no x-ray signal [23].

3.2 Pixel gain measurements

An x-ray spectral histogram can be used to determine the gain of each pixel in binned and un-binned mode. Here, a 150 μm thick tungsten pinhole mask with 25 μm holes is used to isolate the illuminated region to the central portion of a pixel. Integration time was chosen such that the signal would correspond to only a few x-rays/pixel/frame. The mask was translated to provide datasets for each pixel. X-rays were produced via a 50 W silver anode tube operated at 45 kV and 0.4 mA. A graphite monochromator was used to isolate the 22.16 keV Ag K-alpha line.

For each pixel, 10,000 frames for binned mode and 50,000 frames for un-binned mode were captured, each with integration time of 12.5 ms. To determine the gain of a pixel, the signal recorded by that pixel is histogrammed across all frames; the result is a series of peaks corresponding to integer numbers of photons (i.e. 0, 1, 2, …) detected by that pixel during the integration window, as shown in figure 4. The distance between consecutive peaks gives the gain (in ADU/ph) of the pixel for a single photon.

A sum of Gaussians was fit to the data to extract the gain. The height of each Gaussian is constrained to follow a Poisson distribution, and the width of each Gaussian is constrained to be equal. The following equation shows the fit function for a histogram containing \( n \) photon peaks, where \( G, \sigma \) and \( h \) are free parameters to be fit:

\[
f(x) = \sum_{k=0}^{n} \frac{h}{k!} \left( \frac{x_{av}}{G} \right)^k \exp\left(-\frac{x_{av}}{G}\right) \exp\left(-\left(\frac{x-kG}{\sigma}\right)^2\right)
\]

where \( x \) denotes the signal in the pixel, \( G \) denotes the gain of the pixel, \( \sigma \) denotes the width of each Gaussian photon peak, and \( x_{av} \) is the average signal falling on the pixel across all frames. Figure 4 (left) shows the x-ray spectrum for pixel on row 4 and column 7 in un-binned mode. Figure 4 (right) shows the x-ray spectrum for the same pixel for binned mode. It is important to note here that for binned mode, the measured gain in any pixel refers to when the photons are incident on that pixel but are still read out through master pixel of the corresponding master pixel of the 2 × 2 unit. The average gain measured for the detector in un-binned mode is 433±9 ADU/22.16 keV and binned mode is 382±24 ADU/22.16 keV. Hence, the gain decreases by 12±6% when binning is switched on.
Figure 4. Pinhole spectra for pixel on row 4, column 7 when (left) binning is switched off, and (right) binning is switched on. The average gain for the pixels is measured to be 433 ADU/22.16 keV in un-binned mode and 382 ADU/22.16 keV for binned mode. The gain is reduced by 12% in the binned mode as compared to the un-binned mode.

From the measured gain we obtain the effective feedback capacitance, $C_{\text{F,eff}}$, for un-binned and binned mode, which is calculated to be 52 fF and 59 fF for the two modes respectively. Using equation (2.2), we calculate the total input capacitance, $C_{\text{in}}$, of the pixel to be 484 fF for un-binned mode and 767 fF for binned mode. From this we estimate a capacitance of 94 fF per pixel upstream of the binning switches, with 390 fF per pixel downstream. The downstream capacitance is due, in large part, to various test structures included in this chip that are unrelated to pixel binning. A significant reduction in $C_{\text{in}}$ can be expected for future ASICs.

3.3 Pixel noise measurements

System noise was measured with and without binning enabled by comparing 6700 frames with a short integration time (20 ms) with no added signal. The dark charge accumulated during this short period added negligible noise to the overall measurement.

In un-binned mode, the average read noise of the binning-capable pixels was $107\pm19$ ADU rms (5.48±0.89 keV). No difference is seen between the master binning pixels and the secondary pixels. This was the same noise seen for pixels in bank 2 which have no binning structures. When binning was turned on in bank 1, the master pixels had an average noise of $175\pm28$ ADU (10.15±1.74 keV). Hence, the noise goes up by 63±8% when binning is switched on. An increase in noise is expected due to the increased input capacitance in the binned case. We note that the noise in the now unconnected secondary pixels drops to $92\pm16$ ADU. This is due to the reduction in input capacitance in this case.

3.4 Spatial response measurements

To confirm that no signal is lost in binning mode, especially at pixel boundaries within a 2×2 binning unit, a raster scan was conducted across bank 1. A 25 μm pinhole was shifted across each binning unit in steps of 50 μm in both the vertical and horizontal directions to get 25 different measurements of signal intensity, as shown in figure 5 (left). A 50 W silver anode tube was operated at 45 kV and 0.4 mA, with a graphite monochromator to isolate x-rays of 22.16 keV.
Figure 5. (Left) Cartoon depiction of the positions at which signal intensity was measured for a binning unit in binned mode, depicted by ‘x’ marks. The spatial response of the detector in binned mode is obtained in terms of the deviation of measured signal intensity, in horizontal and vertical direction, and averaged together. (Right) Percent deviation of the signal averaged together for all the raster scans, versus the distance of pinhole from the inner pixel boundaries. The response of the super-pixel unit is constant and varies less than 1%, with no loss at the inner pixel boundaries.

For each pinhole position, a total of 10,000 frames were captured with an integration time of 20 ms. The deviation of the measured signal as a function of distance from the inner binning unit boundary was averaged across different binning units. The variation in the signal is measured to be less than 1% across the unit, as shown in figure 5 (right). The uncertainty in the signal deviation is attributed to the variation in the photon flux from the x-ray source. No loss of signal is observed at the boundaries within a binning unit. The gain was also measured across the same grid points using the method described above. Measurements of gain at the interior pixel boundaries of the binning unit using the spectral method agreed with measurements in the pixel interior within 1.6%. Additionally, no difference was seen between any of the four sub-pixels in the binning unit.

4 High-flux characterization

High-flux measurements were conducted at beamline 4B of the Cornell High Energy Synchrotron Source (CHESS), which recently underwent an upgrade where a double-bend achromat lattice is used to achieve high flux density [24]. The beamline is fed by a 1.5 m long CHESS Compact Undulator (CCU) [25]–[26]. A diamond (111) monochromator was used to set the x-ray energy to 11.2 keV. Slits were used to set the beam size to 100 μm × 100 μm approximately 1 m upstream of the detector. Due to beam divergence, the spot size on the detector was about 2 × 2 pixels (FWHM) wide. An ionization chamber immediately downstream of the slits provided an independent measure of the incident flux. Throughout the measurement, the direct beam intensity as measured by the ionization chamber was stable to within 5%. A set of seven 10 μm thick copper foils was placed
directly in front of the detector and removed one at a time in order to vary the flux incident on the detector from $10^6$ x-rays/s to $10^{10}$ x-rays/s.

At each attenuation step, the ionization chamber reading was averaged over 20 s, and a series of 500 exposures, each of 200 μs, was acquired. The flux incident on the detector at each step was computed from the average ionization chamber reading and the known attenuation of the Cu foils. A correction factor for the 800 mm of air after the ionization chamber was applied. The detector measurement integrated the entire beam spot over the size of $2 \times 2$ pixels (FWHM).

Figure 6 shows the flux measured by the detector versus the incident flux measured by the ionization chamber. Included are curves for bank 1 in binned and un-binned mode, as well as bank 2. The largest uncertainty is a systematic uncertainty in the gain factor of the ionization chamber readings. All three cases have a linear response up to a flux of at least $4 \times 10^7$ x-rays/s. For context, most photon counting PADs see a count rate limit of $10^6-10^7$ s$^{-1}$ [27]. Behavior of the binned pixel matches that of the un-binned pixel up to at least $7 \times 10^8$ x-rays/s. At higher rates, the binned pixel performance begins to roll off from that of the un-binned pixel. This is expected behavior due to the fact that the flux incident over 4 pixels is processed by only one front-end amplifier when binning is enabled. The additional input capacitance when binning is enabled does not appear to have an additional adverse affect on the high-flux performance. As noted in section 2.2, adaptive front-end gain was not implemented in either banks 1 or 2. Combining adaptive gain with binning would further improve the high-flux performance of the pixel in terms of maximum sustained flux capability.

5 Conclusions

We have implemented a novel front-end binning architecture in a photon-integrating PAD. The gain of the pixel decreased and the noise increased, as anticipated, due to the increased input capacitance seen when 4 pixels are binned together. The increase in noise is nevertheless less than the increase in noise one would obtain via $2 \times 2$ pixel binning in post-processing. Measurements of the spatial response showed no loss of signal at pixel boundaries within a binning unit.

This ASIC was an early-stage prototype intended, in part, to provide a proof of concept of the front-end binning architecture. No attempt was made to implement a readout architecture for the 16 × 16 pixel array (i.e., pixel addressing and multiplexing during readout) that could realize the increased frame rate that is possible via $2 \times 2$ pixel binning. Any future binning implementation would be accompanied by a streamlined readout architecture capable of realizing the approximately 4× improvement in frame rate.

Improvements in overall performance, particularly in terms of noise and input capacitance, are possible. We note that a number of structures were included in this test chip, such as input protection diodes which will have an impact on the total input capacitance. One contribution to $C_{in}$ that deserves particular attention is any overlap between the bump bond and any underlying metallization on the ASIC, e.g., power planes, which often cover most of the pixel area. The ASIC passivation is often thin with a relatively high dielectric constant, and therefore has the potential to contribute significantly to $C_{in}$. This can be mitigated by adding an additional, thicker passivation layer during ASIC post-processing. We also note that the pixel reset switches, as implemented in this pixel, were quite large to evaluate behavior at extremely high fluxes. These switches contribute
Figure 6. The measured vs. Incident flux (x-rays/s) in the first and the second bank. In the first bank, the response of binned and un-binned mode were measured. A linear fit for the initial region of the curves is displayed. The blue band depicts the uncertainty on the incident flux, dominated by the systematic uncertainty in the ionization chamber gain factor, shown here only for the blue curve. The other curves have the same uncertainty associated with the incident flux. Binned mode performs comparably with the other two curves in the linear region. The binned curve deviates from the un-binned curve in the high flux region, since the flux incident on 4 pixels is now handled by only one front-end amplifier.

significantly to the overall input capacitance. Through careful design, we expect that a significant reduction in input capacitance can be made in future devices, leading to both improved CCE and a reduction in noise. High-flux performance can also be expected to improve if an adaptive gain architecture is added to the front end.

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