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Non-volatile spin switch for Boolean and non-Boolean logic

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We show that the established physics of spin valves together with the recently discovered giant spin-Hall effect could be used to construct Read and Write units that can be integrated into a single spin switch with input-output isolation, gain and fan-out similar to complementary metal oxide semiconductor inverters, but with the information stored in nanomagnets making it non-volatile. Such spin switches could be interconnected, with no external amplification, just with passive circuit elements, to perform logic operations. Moreover, since the digitization and storage occur naturally in the magnets, the voltages can be used to implement analog “weighting” for non-Boolean logic.

The advances of the last two decades have effectively integrated two distinct fields of research, spintronics and nanomagnetics, into one. Spin valves (SVs) and magnetic tunnel junctions (MTJs) are now used both to read from and to write to nanomagnets. This has transformed the field of memory devices and it is natural to ask whether logic devices too can be designed to take advantage of these seminal advances.1

Performing logic operations is conceptually straightforward if external amplifiers or clocking circuitry are used to interface the output from a Read unit to the input of a Write unit. This paper, however, is about autonomous or self-contained logic (SCL) units that can be interconnected to perform logic operations just with passive circuit elements and a power supply, without external amplifiers or clocks. This requires an SCL unit to exhibit internal gain and directivity, attributes that are well-known for transistors, but not for magnets. Of course, one may still want to use clocks to regulate the flow of data as one does with transistor circuits, but it is not a necessary component for fundamental logic operations.

In earlier work on all-spin logic (ASL), we discussed the possibility of implementing such SCL units using bistable nanomagnets as digital spin capacitors that act as threshold elements interacting via spin currents $I_s$.

$$\hat{m} \rightarrow \hat{I}_s \text{ Transmit } \hat{I}_s \rightarrow \hat{m}'$$

in a non-reciprocal manner2 based on the phenomenon of non-local spin transfer torque (NLSTT)3,4 (Fig. 1(a)). The purpose of this paper is to draw attention to the possibility of a scheme (Fig. 1(b)) which also exploits the digital nature of magnets like ASL, but the communication occurs through charge currents $I$ instead of spin currents (Fig. 1(b))

$$\hat{m} \rightarrow \hat{I} \text{ Transmit } \hat{I} \rightarrow \hat{m}'$$

Although charge currents carry less information than spin currents, they should be adequate for many applications while making the communication more robust and long range.

In our proposed scheme, the Read unit (see Fig. 1(b)) is based on MTJs or SVs while the Write unit is based on the giant spin Hall effect (GSHE). In principle, the Write unit could be implemented using an ordinary spin transfer torque (STT) device, but the charge current $I$ would then be larger.
than the spin current $I_s$ needed to switch the magnet. By contrast, recent experiments\cite{5} have clearly shown that the GSHE allows the use of a current $I$ considerably less than $I_s$. This makes it relatively straightforward to design our spin switch with the internal gain and directivity characteristic of SCL units that can be used to build circuits without external amplifiers or clocks. We leave it to future work to determine whether other writing mechanisms can be used to achieve similar gain and directivity.

We will show that like ASL, the spin switch meets the five basic tenets required of a digital logic device:\cite{6} It is inherently non-linear due to the bistable nature of magnets and the output is electrically isolated from the input with negligible feedback. It is concatenable, that is, the output of one unit can drive the input of the next, can be designed to provide gain based on present-day technology and can be used to construct a complete set of Boolean logic gates.

One disadvantage of the structure in Fig. 1(b) is that it draws current continuously which could be reduced a little if the writing mechanism were voltage-driven. Even with the current-driven mechanism we are discussing, it may be preferable to put the resistor “$r$” in series with a capacitor which reduces the standby current. Appendix B in supplementary material\cite{16} describes a simulated operation of a majority gate and fan-out including capacitors in series with the “$r$.”

We estimate the energy-delay product of our proposed spin switch to be inferior to complementary metal oxide semiconductor (CMOS) inverters, but this could change with further advancements in spintronic switching of magnets and requires a careful discussion beyond the scope of this paper. On the other hand, unlike CMOS devices the information is stored in nanomagnets and not in the voltage, making it non-volatile. It also naturally allows for non-Boolean operation as we will illustrate with a simple example of a reconfigurable comparator (Fig. 5), an ability not ordinarily available in a CMOS implementation.

Let us start with the basic physics underlying the Read and Write units that comprise the spin switch and then show how these units can be integrated to provide a concatenable device that we call a spin switch.

**Read unit:** The read device consists of two nanopillars on top of the input magnet $m$ (Fig. 1(b)), each representing an SV or an MTJ whose conductance is determined by the orientation of the input magnet relative to the fixed magnets $M$ and $-M$.

This structure can be modeled with the equivalent circuit shown in Fig. 2, where $G$ and $\Delta G$ represent the sum and difference, respectively, of the parallel ($G_P$) and anti-parallel ($G_{AP}$) conductances of the SV or MTJ. This circuit leads straightforwardly to the following expression for the open circuit voltage and the current:

\[
V_{out} = \frac{\Delta G}{G} \cdot \hat{m} \cdot \hat{M},
\]

\[
I = \frac{V_{out}}{r + 1/G}.
\]

$V_{out}$ is thus proportional to the component of the input magnetization $\hat{m}$ along a fixed direction $\hat{M}$ determined by the fixed magnets. Note that $\Delta G = G_P - G_{AP}$ and $G = G_P + G_{AP}$. Assuming a TMR of 135% and resistance-area product of $A/G_P = 4.3 \, \Omega \, \mu m^2$,\cite{7} we estimate a polarization and a conductance of

\[
P \equiv \Delta G/G = TMR/(TMR + 2) = 0.4
\]

\[
G \sim (1.1 \, K \, \Omega)^{-1}
\]

for a junction area of $\sim 80 \, nm \times 30 \, nm$.

**Write unit:** The Write unit is essentially the same as that described in Ref. 5 and is based on the GSHE recently observed in high spin-orbit materials like platinum, tantalum, and tungsten\cite{8,9,10} or alloys like CuBi.\cite{11} A charge current $I$ gives rise to a spin current $I_s$ that carries $\hat{z}$ spins in the $\hat{y}$ direction

\[
\vec{I}_s = \beta \vec{I} \hat{z},
\]

with

\[
\beta = \text{Spin-Hall Angle} \times (A_s/A),
\]

where $A_s$ and $A$ being the cross-sectional areas for the spin current and charge currents, respectively. For a magnet with $L = 80 \, nm$, this ratio could be $\sim 40$ if the thickness $t_0$ of the high spin-orbit metal layer is $2 \, nm$. Based on the demonstrated spin-Hall angle of 0.3 in tungsten,\cite{9} this would give a charge to spin amplification factor of $\beta = 12$. Note, however, that the high resistivity of thin tungsten layers\cite{9} could make the resistance “$r$” fairly large. Other materials like CuBi with comparable spin-Hall angles but lower resistivity\cite{11} may be preferable.

We will now describe a possible scheme for combining a Read unit with a Write unit to form a spin switch that is concatenable, whereby the output of one switch can drive the next switch.

**Concatenable spin switch:** Our proposed spin switch (Fig. 3(a)) consists of a Write unit and a Read unit that are electrically isolated, but magnetically coupled through a dipolar interaction that is strong enough to ensure that the angle $\theta$ between them always has a fixed value. The interaction could be ferromagnetic making $\theta = 0$, or antiferromagnetic making $\theta = \pi$ or even something in-between. Although the Write and Read units are shown side by side as is common in nanomagnetic logic,\cite{12} in practice, it may be better to lay the Read unit on top of the Write unit to enhance the magnetic interaction. For our simulations, we have assumed identical magnets each of which creates a dipolar field equal to the coercive field $H_K$ at the other magnet in a direction that keeps the two magnets anti-parallel.
entering the write unit is large enough to generate a spin current $\beta V_{in}/(R_{in} + r)$ through the SHE that exceeds a certain critical value, it will switch the magnet $\vec{m}'$ to the $+\hat{Z}$ direction, putting the other magnet $\vec{m}$ of the pair in the $-\hat{Z}$ direction, so that the output voltage $V_{out} = -V\Delta G/G$ (see Eq. (3)). If we now reverse the input voltage beyond the critical value, the magnets are switched in the opposite direction with a reversal of the output voltage, resulting in a hysteretic inverter-like characteristic as shown in Fig. 3(d). Note that the sign of $V_{out}/V_{in}$ in Fig. 3(d) could be changed by reversing either the sign of the $\beta$ or the $V$ associated with the Write and Read units, respectively.

In Fig. 3(d), we have normalized the input spin current $\beta V_{in}/(R_{in} + r)$ by $4I_{s,c}, I_{s,c}$ being the critical current for one of the magnets ($\vec{m}'$ or $\vec{m}$ which are assumed identical)\(^5\)

$$I_{s,c} = (2q/\hbar) x \mu_0 M_s \Omega (H_K + M_s/2), \quad (4)$$

where $M_s$ is the saturation magnetization, $H_K$ is the coercive field, $\alpha$ is the damping parameter, and $\Omega$ is the volume of the magnet. As we might expect, a spin current $\sim 2 I_{s,c}$ is needed to switch since two magnets are coupled together. We consider only in-plane magnets, leaving perpendicular magnetization for future work.

Note that with negligible voltage applied to the Read unit, the switching current is the same for $-Z$ to $+Z$ and for $+Z$ to $-Z$. But, a voltage $V$ applied to the Read unit shifts the loop along the $x$-axis because it injects a spin current along $-Z$ which aids the Write unit when the Read unit is switching to $-Z$. The value of $V$ used for the solid curve in Fig. 3(d) is chosen to exceed what is needed to ensure that a Read unit generates an input voltage of $V_{in} = V\Delta G/G$ for the next Write unit that is large enough to switch it assuming $r \ll R_{in} = 1/G$. According to Fig. 3(d), this requires

$$V \geq \frac{4I_{s,c}}{\beta V\Delta G} (1 + Gr). \quad (5)$$

With $\Omega = 80 \text{ nm} \times 100 \text{ nm} \times 1.6 \text{ nm}$, and $\mu_0 M_s \sim 1 \text{ T}$, $\mu_0 H_K \sim 0.02 \text{ T}$, $\alpha \sim 0.01$, we have $I_{s,c} \sim 160 \mu A$. Using $\beta = 12$, $G \ll 1$, $\Delta G/G \sim 0.4$, $G^{-1} \sim 1.1 \text{ K} \Omega$ from our earlier estimates, we have $V \sim 150 \text{ mV}$. We use these parameters for all simulations, though they have not been optimized and other choices may be preferred depending on the application. Details of the simulation model are described in Appendices A and B.\(^16\)

**Ring Oscillator:** Fig. 4 shows an example of how spin switches of the type shown in Fig. 3(a) (represented by the symbol in Fig. 3(b)), are interconnected to implement a circuit function, in this case, a ring oscillator. If the voltages $V$ on the Read units exceed the threshold value given by Eq. (5), then each unit will try to switch the corresponding magnet of the next unit anti-parallel to itself. But, with an odd number of magnets (three in this case) in the loop, there is no way to make all neighboring magnets anti-parallel and so no satisfactory steady state can be achieved. Instead, each magnet switches the magnet downstream which in turn switches the next magnet, resulting in continuous oscillations as shown in Fig. 4 from our simulations.
suggesting that the proposed spin switch could be involving majority gates with multiple fan-out (see Appendix B). Such oscillations are well-known in the context of CMOS inverters and Fig. 4 shows that our proposed spin switch has these transistor-like characteristics allowing it to generate an oscillatory output from a dc power supply without any external amplifier or clock. This requires properties like directivity and input-output isolation needed for SCL units. We have also simulated more sophisticated circuits involving majority gates with multiple fan-out (see Appendix B), suggesting that the proposed spin switch could be used to construct large scale circuits.

Reconfigurable comparator: Figure 5 shows a different device that could be implemented by interconnecting our proposed spin switches (Fig. 3(a)). It should provide an output that correlates the incoming signal \( \{X_n\} \) with a reconfigurable reference signal \( \{Y_n\} \) stored in the \( m_i \) of the switches. Such oscillations are well-known in the context of CMOS inverters and Fig. 4 shows that our proposed spin switch has these transistor-like characteristics allowing it to generate an oscillatory output from a dc power supply without any external amplifier or clock. This requires properties like directivity and input-output isolation needed for SCL units. We have also simulated more sophisticated circuits involving majority gates with multiple fan-out (see Appendix B), suggesting that the proposed spin switch could be used to construct large scale circuits.

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Since the output current (see Eq. (1)) of each Read unit is a product of \( V \) \((\sim X_n)\) and \( m_i \) \((\sim Y_n)\), it is determined by \( X_n Y_n \) which are all added up to drive the output magnet. If the sequence \( \{X\} \) is an exact match to \( \{Y\} \), then the output voltage will be \( N \), since every \( X_n Y_n \) will equal +1, being either \((+1)Y_n + 1\) or \((-1)Y_n - 1\). If \( \{X\} \) matches \( \{Y\} \) in \( (N-n) \) instances with \( n \) mismatches, the output will be \( N - (2^n) \) since every mismatch lowers output by 2. If we set the threshold for the output magnet to \( N - (2^n) \), then the output will respond for all \( \{X\} \) that matches the reference \( \{Y\} \) within a tolerance of \( N_e \) errors. The inset in Fig. 5 shows an example with \( N_e = 0 \).

Weighted interconnections: An important distinction of the spin switch with a CMOS device is the representation and storage of information in nanomagnets rather than in voltages. This makes the switch non-volatile, and also allows us to use the voltages to change the weight of the connection between a Read and a Write unit in an analog manner, with magnets naturally providing the digitization. We could extend Eq. (5) to define the weight \( a_{ij} \) as the ratio of the current from the Read magnet of unit “i” normalized to the critical current needed to switch the Write magnet of unit “i”:

\[
a_{ij} = \frac{(V \Delta G)_{ij}}{4I_{c,i}/|\beta|} \frac{1}{1 + G_{tot} r_i},
\]

where \( G_{tot} \) is the sum of the \( G_i \) for all Read units connected to the same Write unit.

This feature could make it possible to interconnect our proposed spin switches to implement hardware neural networks \(13\) where both the sign and the magnitude of the weights \( a_{ij} \) (Eq. (6)) associated with each Read-Write connection can be conveniently adjusted through the voltages \( V \) applied to the Read unit and the gain \( \beta \) of the Write unit. Using present day technology, it should be possible to implement weights that exceed switching thresholds either individually (Fig. 3(d)) or collectively (Fig. 5), but even subthreshold networks could find use in probabilistic logic as discussed for ASL in Ref. 14. Note also the additional factor \((1 + G_{iso} r_i)\) that enters the expression for the weights \( a_{ij} \). Ordinarily, the resistances \( r_i \) arise from that of the high spin-orbit material in the Write units. But, it may be possible to add a phase change resistance in series that could provide an automatic adjustment of weights, perhaps making it possible for networks to “learn.”

Summary: We have shown that the established physics of SVs/MTJs could be used to construct a Read unit that converts the information stored in a nanomagnet into a current which can be used to operate a Write unit based on the physics of the GSHE. We then show how the Write and Read units could be integrated into a single spin switch showing inverter like characteristics having input-output isolation, directivity and fan-out similar to CMOS inverters, but with the information stored in nanomagnets making it non-volatile.

The gain \( \beta \) made possible by the GSHE allows us to engineer a Write-Read asymmetry whereby the switch follows the Write signal and not the Read signal. This is a key requirement for SCL units analogous to the well-known
property of field effect transistors (FETs) that makes them switch in response to a *gate voltage* (which “writes” the input onto the state of the transistor) but not in response to a comparable *drain voltage* (which “reads” the state of the transistor).

We have analyzed only the simplest design with identical Read and Write magnets leaving it to future work to determine if the Write-Read asymmetry can be enhanced through other means such as making one magnet softer or smaller than the other. Indeed, even the basic Read and Write mechanisms could possibly be improved for lower switching energy, delay and standby power.

However, the key point is that the proposed spin switches can be interconnected just with passive circuit elements, to perform logic operations, without any external circuitry for signal conversion or amplification. Moreover, since the digitization and storage occur in the magnets, the switches are non-volatile and reconfigurable and the voltages can be used to implement analog “weighting” for non-Boolean logic.

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1See for example D. Nikonov, G. I. Bourianoff, and T. Ghani, in *IEEE International Conference in Nanotechnology* (2011); X. Yao, J. Harms, A. Lyle, F. Ebrahimi, Y. Zhang, and J. P. Wang, *IEEE Trans. Nanotechnol.* **11**, 120 (2012), and references therein.

14 See supplementary material at http://dx.doi.org/10.1063/1.4769989 for appendix A (modeling a spin switch) and appendix B (modeling spin switch networks).