

**eSampling**: Rethinking Sampling with Energy Harvesting

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**Abstract**—In general, real world signals are analog in nature. To capture these signals for further processing, or transmission, signals are converted into digital bits using analog-to-digital converter (ADC). In this conversion, a good amount of signal energy is wasted because signal that is captured within the sampling duration is utilized, while rest of the signal waveform is discarded. In this context, this paper revisits the sampling process and proposes to utilize this discarded signal for energy harvesting, naming the method as *eSampling*, i.e., sampling with energy harvesting. The proposed idea of *eSampling* is demonstrated via modifying the circuitry of the hold phase of ADC. The system is designed using standard Complementary Metal Oxide Semiconductor (CMOS) 65 nm technology and simulations are performed on Cadence Virtuoso platform with input signal at different frequencies (100 Hz and 40 MHz). These results show that 10% of the sampling period is sufficient to sample the input analog signal, while the remaining 90% can be used for harvesting the energy from the input analog signal. In order to validate *eSampling* for practical scenarios, results with hardware setup have also been added.

**Index Terms**—Energy harvesting, Sampling, Sampling period and Analog-to-digital converter

**I. INTRODUCTION**

Energy harvesting (EH) via ambient sources has become an important area of research due to the advent of low power [1], [2] and small form-factor devices [3], [4]. Small form factor has not only led to reduction in size of electronic devices, but also enhanced it’s functionality. This has also led to plethora of wearable devices that has replaced most of the functionalities of portable devices. For instance, smart watches have replaced some of the functionalities of smart phones. Further, the advancement in low power microelectronics technology has reduced the power consumption of devices by a considerable amount and hence, devices can be operated by harvesting the energy from ambient sources. Energy harvesting can either increase the lifetime of the device or can ensure a battery-free system [5]. Similarly, in case of wireless sensor networks (WSNs), battery-free sensors can eliminate the difficulties of replacing or recharging the batteries at remotely located sensors [6]–[8]. EH also finds applications in toxic environments, medical body area networks (MBANs), and body area networks (BANs) [9]–[11], where replacing or recharging batteries is an arduous task.

Energy can be harvested either from human activities such as walking, jogging, and cycling [12], [13] or from environmental sources such as solar [14], [15], wind [16], thermal [17] and mechanical pressure etc. [18]. Recently, harvesting the energy from radio frequency (RF) signals has gained a lot of popularity over other energy sources [19]. The foremost reason for the same is that RF signals, being harvested, are abundant in the humanized environment, whereas solar/wind resources are not perennially available. Furthermore, RF signals contain both information as well as energy and hence, an energy constrained receiver can decode the information as well as harvest the energy. This method is known as simultaneous information and power transfer (SWIPT). The two realistic protocols for SWIPT, namely, time switching (TS) and power splitting (PS) [20], [21] affect the system performance in order to harvest the energy. However, the phrase ‘energy harvesting’ refers to the process of converting discarded/wasted/unused energy into useful electrical energy for fulfilling the energy requirements, for instance, solar EH. Thus, energy should be harvested from the discarded signals without degrading system performance.

In this paper, we propose a novel method for energy harvesting termed as *eSampling*, where *e* signifies the process of energy harvesting. *eSampling* has been proposed for harvesting the unused/discarded signal energy during the sampling process of an analog-to-digital converter (ADC). Since most of the real signals are analog in nature, to capture and store the data, these are converted into equivalent digital bits by using an ADC. An ADC consists of two processes, namely sampling and quantization. Sampling converts the input analog signal into discrete samples, while quantization converts the discrete samples into digital bits. Typically, a sample and hold (S/H) circuit is used to sample the input analog signal in an ADC. The S/H circuit consists of two phases, *acquisition phase* and *hold phase*. In acquisition phase, the S/H circuit tracks the input analog signal. The sampled value captured in the acquisition phase is converted into digital bits during hold phase. Therefore, during sampling process of an ADC, the input signal is processed only for a small fraction of time (acquisition phase) and neglected/discarded for the remaining time interval (hold phase). Hence, a method *eSampling* is proposed which modifies the hold phase of the sampling...
process to harvest the energy from the input signal. To the best of our knowledge, no such work has been reported till date which harvests the input signal energy during the sampling process without degrading the performance of an ADC or any other block in the system.

A. Related work

In literature, methods have been proposed for harvesting energy from discarded signals [22], [23]. For example, a method has been proposed for harvesting energy during modulation and filtration in [22]. Since a part of signal energy is often discarded or lost during modulation, this can be harvested to generate electrical power. Likewise, filtering also discards some part of the signal in the process of accomplishing desirable task. Signal portion discarded during filtering can be utilized to harvest energy. Similarly, signal energy has been harvested from the redundant portion (i.e. the cyclic prefix) in Orthogonal Frequency Division Multiple Access (OFDMA) system in [23].

The method eSampling has worldwide applications, since real signals are analog in nature and most of the existing systems are energy constrained. For example, the proposed method can be directly utilized in WSNs because the sensor nodes are energy constrained nodes and are typically powered by batteries with a limited lifetime [24]. Therefore, energy harvesting systems can be employed to supplement the lifetime of the battery. Most of the recent work focuses on developing an effective energy management solution [25]–[28] because even though additional energy can be harvested from the external environment, it remains a limited resource, and hence should be consumed wisely. Effective energy management relies on re-designing of circuit to harvest maximum available energy [25], [26] and also on re-designing of network which includes various opportunistic transmission strategies and routing algorithms to reduce the energy consumption [27], [28]. On the other hand, the current work proposes an entirely different approach and provides an alternative form of energy harvesting that is carried out during the sampling of its own sensed analog signal. Generally, sensor nodes generate analog signals corresponding to the sensed parameters that are digitized using ADC and are transmitted to the Fusion center [8], [24]. The generated analog signals at sensor nodes have a good amount of energy that was wasted earlier. This energy can be harvested by using the proposed eSampling method. Therefore, self-sustainable wireless sensor nodes can be fabricated that can charge themselves from their own sensed parameter without using any dedicated energy harvesting source. Similar to above, eSampling method will find tremendous utility in wireless body area network (WBAN) because sensor devices are generally autonomous and implanted inside the body, where batteries are irreplaceable [29].

Further, the proposed eSampling method can be applied to numerous industrial application scenarios including but not limited to radar, wireless communication [30]–[32], vehicular networks [33] and Internet of things [25]–[28]. In future, energy constrained devices or circuits involving sampling process at some stage may like to replace the conventional sampling with eSampling with re-design of the associated circuitry.

Rest of the paper is organized as follows: Section II describes the proposed eSampling method, Section III reports the simulation model designed for eSampling, Section IV discusses simulation results for the validation of the proposed method and Section V provides the real time validation of eSampling using hardware setup. Finally, conclusions are drawn in section VI.

II. PROPOSED eSampling METHOD

A. Overview

Consider Fig. 1a) and b) that describe the acquisition and hold phase of the sampling process, respectively controlled by a common sampling clock (Clk). The acquisition phase is the duration for which S/H switch is connected to capacitor $C_h$ to track the input analog signal. Once the acquisition phase is over, the hold phase starts. In this phase, the S/H switch is open or disconnected from $C_h$ as shown in Fig. 1b) such that $C_h$ can hold the sampled value acquired in the acquisition phase. This signal value is converted into digital bits using the quantization process. This is to be noted that the discarded input signal during the hold phase contains a considerable amount of energy that can be harvested. In this work, we propose an alternative phase, henceforth called as EH phase, during which the switch will be connected to another capacitor $C_{EH}$ to store the energy as shown in Fig. 1c). This phase can be seen as the modified version of the hold phase of the conventional ADC. It should be noted that the modified hold phase with the EH phase does not impact the functionality of the conventional ADC circuit.

Consider an input analog signal with maximum signal frequency $f_m$ sampled at Nyquist sampling rate. Hence, the sampling period is given as $T_s = \frac{1}{f_s} \leq \frac{1}{2f_m}$, where $f_s$ is the sampling frequency. The sampling period is given by

$$T_s = T_{aq} + T_h,$$

where $T_{aq}$ is the acquisition time or the time allocated to the acquisition phase as shown in Fig. 1a). It is defined as the minimum time required for $C_h$ to charge itself to the full input signal voltage. $T_h$ is the hold time during which the input analog signal is disconnected from the ADC and the sampled value obtained across $C_h$ is converted by ADC into corresponding digital bits as shown in Fig. 1b). Since the input analog signal is not processed during $T_h$, it can be harvested to recharge the batteries or to drive other on-chip circuits.

B. eSampling System Model

Fig. 2(a) presents the block diagram of eSampling system with input signal ($V_{in}(t)$). It comprises of two branches: ADC branch and EH branch. A differential Successive-Approximation Register (SAR) ADC has been employed in the ADC branch of the system that comprises of a sampling switch ($S_1$), a voltage comparator, a digital-to-analog converter (DAC), and a SAR logic. On the other hand, EH branch consists of a switch $S_2$, a rectifier, and a energy storage capacitor ($C_{EH}$). The voltage across the capacitor
is denoted as $V_{EH}$. Switches $S_1$ and $S_2$ of the model are controlled by $Clk$ as shown in Fig. 2(b). The operation of the $esampling$ system is divided in two phases:

**Acquisition Phase** ($S_1$ is ON and $S_2$ is OFF): The time period of this phase is equal to $T_{aq}$. The equivalent block diagram is shown in Fig. 2(c). The functioning of both ADC and EH branch in acquisition phase is described below.

- ADC branch: Input analog signal from the surrounding or preceding blocks is sampled onto the DAC capacitors of SAR ADC [34].
- EH branch: It is isolated from the signal source ($V_{in}(t)$).

**Energy harvesting (EH) Phase** ($S_1$ is OFF and $S_2$ is ON): The time period of this phase is equal to $T_h$. The equivalent block diagram is shown in Fig. 2(d). The functioning of ADC and EH branch in EH phase is explained below.

- ADC branch: SAR ADC converts the sampled signal into equivalent digital bits using a quantizer.
- EH branch: The input analog signal is rectified to store the maximum amplitude of the signal on capacitor $C_{EH}$. However, due to non-idealities associated with the rectifier and switches, certain voltage drop is experienced. Hence, the maximum voltage on $C_{EH}$ is given by

$$V_{EH} = \eta_e V_M,$$

where $V_M$ is the maximum amplitude of the input signal $V_{in}(t)$ and $0 < \eta_e \leq 1$ is the efficiency of the EH branch. Further, the maximum time that can be assigned for harvesting the input signal energy is given by using (1) as below:

$$T_{EH} = T_s - T_{aq}.$$  \hfill (3)

The amount of energy harvested/stored from the input analog signal can be calculated as

$$E_h = \frac{1}{2} C_{EH} V_{EH}^2,$$  \hfill (4)

The conversion efficiency, i.e., the percentage of energy harvested from the input signal until $C_{EH}$ attains the steady state is given by

$$\eta_e = \frac{E_h}{E_{in}} = \frac{C_{EH} V_{EH}^2}{2 P_{in} T_{CEH}},$$  \hfill (5)

where $P_{in}$ is the root mean square (rms) power of the input signal $V_{in}(t)$ and $T_{CEH}$ denotes the time taken by energy harvesting capacitor ($C_{EH}$) to charge up to steady state voltage, i.e., $V_{EH}$.

**III. Simulation Model**

In order to demonstrate the proposed idea, a system model is designed using standard 65 nm Complementary Metal Oxide Semiconductor (CMOS) technology. Design details of all sub-blocks in the system model are described below.
1) Switches: Switches $S_1$ and $S_2$ follow differential implementation and are realized using two different switch topology. $S_1$ is implemented using n-channel MOS (NMOS) bootstrapped switch [35], while $S_2$ is implemented using p-channel MOS (PMOS) pass transistors. Both switches are controlled by $Clk$.

Switch $S_2$ is implemented using two PMOS transistors as shown in Fig. 3(a). The PMOS transistor turns ON and passes the input signal ($V_{in}(t)$) when $Clk$ is at logic '0'. However, it turns OFF and isolates the input signal from the next block when $Clk$ is at logic '1'. PMOS transistors are used instead of NMOS because PMOS transistors pass the logic '1' (high voltage) without experiencing the voltage drop.

The on-resistance, $R_{ON}$ of a pass transistor $M_p$ is given by [36]

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L} (|V_{GS}| - |V_{TH}|)}$$

where $\mu$ is the mobility, $C_{ox}$ is the oxide capacitance, $\frac{W}{L}$ is the aspect ratio, $V_{GS}$ is the gate-to-source voltage, and $V_{TH}$ is the threshold voltage of the transistor. $V_{GS}$ of the pass transistor varies with time according to the input signal $V_{in}(t)$ and hence, $R_{ON}$ will also vary as given in (6). The variation in the $R_{ON}$ introduces non-linear distortion at the output of ADC and hence, bootstrapped switch is generally used for ADC. The bootstrap switch can typically ensure constant $R_{ON}$ [35].

Switch $S_1$ is implemented using two NMOS single-ended bootstrapped switches as shown in Fig. 3(b). In order to ensure a nearly constant $R_{ON}$, the gate of transistor $M_1$ is bootstrapped using two PMOS transistors $M_2$ and $M_3$, three NMOS transistors $M_4$, $M_5$ and $M_6$, and one capacitor $C_B$ [35]. Two CMOS inverters $I_1$ and $I_2$ are also employed in the structure to generate required clock signals for proper operation of the switch.
2) ADC: The architecture of SAR ADC is implemented using a sampling switch \( S_1 \), voltage comparator, SAR logic, and DAC. Switch \( S_1 \) is a bootstrap switch as explained above. A two stage voltage comparator is implemented, where the first stage is a dynamic pre-amplifier and second stage is a latch [37]. Furthermore, SAR logic is implemented using two arrays of shift registers that operate in serial-in-serial-out and parallel-in-parallel-out modes [38]. The ADC operates asynchronously, hence the clock pulses for comparator and SAR logic are generated internally from \( Clk \) using clock generation logic [38]. In addition, binary-weighted capacitive DAC is used in the ADC. The capacitive DAC is implemented using merge capacitor switching (MCS) scheme [34] because it eliminates the most significant bit (MSB) capacitor compared to conventional design [39] and hence, reduces the total capacitance of the DAC \( (C_{DAC}) \) by half. It should be noted that \( C_{DAC} \) of SAR ADC mimics \( C_h \) (Fig. 1). By reducing \( C_{DAC} \) and \( T_{aq} \) of the ADC can be reduced, because \( T_{aq} \) is defined as [36]

\[
T_{aq} = R_{ON}^{S1} C_{DAC},
\]

where \( R_{ON}^{S1} \) is the on-resistance of \( S1 \) switch. Further, \( C_{DAC} \) for \( n \)-bit SAR ADC is defined as

\[
C_{DAC} = \left(1 + \sum_{i=0}^{n-2} 2^i\right) C_u,
\]

where \( C_u \) is the unit capacitor of the DAC array. \textit{eSampling} demands low value of \( T_{aq} \) so that more time could be allocated for harvesting the input signal energy [3]. It should be noted that to further reduce \( T_{aq} \), \( C_{DAC} \) and \( R_{ON} \) should be reduced as evident from (7). Reducing \( R_{ON} \) demands wider transistors, which in turn increases the device capacitance and thus, reduces the operating speed of the ADC. In addition, wider devices leads to charge injection problem, which degrades the SNR of the ADC and hence, the performance of the ADC is compromised. On the other hand, employing small values for \( C_{DAC} \) results in mismatch issues and sampling noise, which degrade the ADC conversion accuracy. These issues demand the \( T_{aq} \) to be large enough such that the ADC performance is not compromised. A large \( T_{aq} \) will reduce time available for the energy harvesting, \( T_{EH} \). As a consequence, there is trade-off between \( T_{EH} \) and \( T_{aq} \).

3) Rectifier: A full wave rectifier has been employed in the simulation model as shown in Fig. 4. Due to inherent threshold voltage drop in NMOS transistor, the rectifier is implemented using PMOS (p-type MOS) transistors. The two PMOS transistors have been connected in a cross-coupled fashion as shown in Fig. 4. It should be noted that in this circuit, a negative to positive transition at point A results in positive to negative transition at point B, and hence, \( M1 \) is ON and \( M2 \) is OFF. While in vice-versa condition, \( M1 \) is OFF and \( M2 \) is ON. Therefore, a full wave rectification can be observed at the output.

![Diagram of Rectifier](image)

IV. Simulation Results and Discussions

A complete schematic of the \textit{eSampling} model has been created in Cadence Virtuoso platform. Schematic simulation uses mathematical models, which help us to authenticate the behavior of \textit{eSampling}. However, schematic simulations exclude the effect of parasitic capacitance and resistance associated with the connecting wires and devices employed in the system model. Therefore, post-layout simulations have been also performed to ensure similar performance of the model when fabricated to work in real world environment. Since the focus of the paper is to harvest maximum energy from the input signal without effecting the performance of ADC, post-layout simulations were carried out for switch \( S1 \) and EH branch. Layouts of these blocks are presented in Fig. 5. It should be noted that for obtaining the desirable performance of \( n \)-bit ADC, the output signal-to-noise and distortion ratio (SNDR) of \( S1 \) should be greater than \( 6.02n + 1.76 \text{ dB} \) [36].

![Layout of the eSampling model](image)

To demonstrate the efficiency of the proposed idea of energy harvesting along with sampling, an 8-bit SAR ADC has been used in the ADC branch of the \textit{eSampling} system. In addition, to cover a wide range of applications, \textit{eSampling} system has been simulated for both low (KHz) as well as high (MHz) input signal frequencies. During simulation, the acquisition time is chosen to be 10% of the total sampling period, i.e., \( T_{aq} = 0.1 T_s \) such that 90% of the sampling time can be allocated for energy harvesting, i.e., \( T_{EH} \approx 0.9 T_s \).

A. Low-frequency Simulation of \textit{eSampling} System

Low frequency simulations are performed at a sampling frequency \( \left( \frac{1}{T_s} \right) \) of 10 KHz. The frequency of the input signal is calculated using coherent sampling principle and following the Nyquist rule. A sinusoidal signal with amplitude varying from -0.4 V to 0.4 V is selected as an input with an input rms power of 27.7 \( \mu \text{W} \) for a source impedance of 50 ohm.

A SAR ADC has been designed to operate at \( T_{aq} = 0.1 T_s = 10 \mu\text{s} \) with \( C_{u} = 12 \text{nF} \). From schematic
Simulations, the output SNDR of $S1$ is around 65 dB. The FFT plot of the reconstructed signal is presented in Fig. 6, which shows SNDR of 49 dB and ENOB (equivalent number of bits) equals to 7.85 bits for an 8 bit ADC that implies no loss of bits. In addition, from post-layout simulations, the obtained output SNDR of $S1$ is around 62 dB, which is greater than $6.02n + 1.76$ dB. Therefore, as mentioned above, it can drive an 8-bit SAR ADC.

Simulation results of EH branch is presented in Fig. 4. It is observed that when $Clk$ is ‘logic 0’ (during $T_{EH}$ time period), the two PMOS transistors defining the $S2$ switch track the input analog signal $V_{in}(t)$ that will be the input of the rectifier $V_{rec}^{in}$. Rectifier rectifies $V_{rec}^{in}$ to provide a DC output voltage $V_{EH}$. Consider Fig. 8 for both schematic and post-layout simulation results for $V_{EH}$.

For schematic simulation a DC voltage close to 307.16 mV is obtained at $C_{EH} = 100 \ \mu F$. This implies $\eta_v = 76.79\%$. The time taken by the capacitor to charge up to 307.16 mV is $T_{CEH} = 224.91$ ms. Therefore, 75.7% of the input signal energy has been harvested by using the eSampling system. In addition, $V_{EH}$, $T_{CEH}$, $\eta_v$, and $\eta_e$ have been calculated from post-layout simulations as 304.7 mV, 250.12 ms, 76.175% and around 67%, respectively. The degradation in performance is due to the parasitic capacitance and resistance involved in the post-layout simulations.

![Fig. 6. FFT plot of 8-bit SAR ADC for 10 KHz sampling frequency.](image)

**B. High-frequency Simulation of eSampling System**

In this section, the proposed model is simulated at a sampling frequency of 40 MHz. Following the above specification, the SAR ADC is designed to operate at $T_{aq} = 0.1 \ T_s = 2.5$ ns with $C_u = 15 \ fF$. A sinusoidal signal with $V_M = 0.4$ V is considered with the source impedance of 50 Ohm. The obtained input signal rms power ($P_{in}$) is 27.255 $\mu W$.

From schematic simulations, the output SNDR of $S1$ is around 61 dB. The FFT plot of the reconstructed signal is presented in Fig. 7. From the plot, it is observed that the achievable SNDR and ENOB are 48.52 dB and 7.77 bits, respectively. Furthermore, from post-layout simulations, the obtained output SNDR of $S1$ is around 58 dB, which is greater than $6.02n + 1.76$ dB. Therefore, as mentioned above, it can drive an 8-bit SAR ADC.

Simulation results of EH branch is presented in Fig. 10. Compared to the low frequency operation (Fig. 7), less time is available for energy harvesting during the high frequency operation. The obtained $V_{rec}^{in}$ is rectified and stored in $C_{EH}$ as shown in Fig. 11. From schematic simulations, a DC voltage of 304 mV is obtained across $C_{EH} = 25 \ nF$ without degrading the performance of ADC. This implies $\eta_v = 76\%$. The time taken by $C_{EH}$ to charge up to $V_{EH} = 304 \ mV$ is $T_{CEH} = 58.32$ $\mu s$. Therefore, 72.64% of the input energy could be harvested using the proposed system model at high frequency. In addition, $V_{EH}$, $T_{CEH}$, $\eta_v$, and $\eta_e$ have been calculated from post-layout simulations as 300 mV, 65 $\mu s$, 75% and around 65.53%, respectively. The degradation in performance is due to the parasitic capacitance and resistance involved in the post-layout simulations.
## Table 1: Performance Metric

| Operation | $T_s$ ($\mu$s) | $T_{aq}$ ($\mu$s) | $T_{EH}$ ($\mu$s) | $C_{EH}$ (µF) | $V_{EH}$ (mV) | $T_{C_{EH}}$ (ms) | $\eta_c$ (%) | $\eta_e$ (%) |
|-----------|----------------|-------------------|-------------------|---------------|---------------|-----------------|-------------|-------------|
| Sampling@10 KHz Schematic | 100 | 10 | 90 | 100 | 307.16 | 224.391 | 76.79 | 75.7 |
| Sampling@10 KHz Post-layout | 304 | 0.05832 | 67 | 76.79 | 220.12 | 76.79 | 75.7 |
| Sampling@40 MHz Schematic | 0.025 | 0.0225 | 0.025 | V EH=304 mV | V EH=300 mV | T C
EH
=62.93 s | T C
EH
=58.32 s |
| Sampling@40 MHz Post-layout | 300 | 0.063 | 304 | 0.05832 | 76 | 75 | 65.53 |

![Schematic Simulation](image1)

![Post-layout Simulation](image2)

![Sampling clock, input signal and input to the rectifier in the EH branch at 40 MHz.](image3)

![Voltage obtained across $C_{EH}$ at 45 MHz KHz sampling frequency.](image4)

![Fig. 9. FFT plot of 8-bit SAR ADC for 40 MHz sampling frequency.](image5)

![Fig. 10. Sampling clock, input signal and input to the rectifier in the EH branch at 40 MHz.](image6)

C. Discussion

For both low and high frequency simulations, it is observed that the input signal energy can be harvested while maintaining the optimal performance of 8 bit SAR ADC (ENOB ≥ 7.75 bits at the Nyquist rate). The obtained results for high and low frequency simulations are summarized in Table I.

The size of the energy harvesting capacitor, i.e., $C_{EH}$ plays an important role and generally based upon the load to be driven. It can be expressed as

$$C_{EH} = \frac{I_{load} T_P}{\Delta V},$$  

(9)

where $I_{load}$ is the load current, $T_P$ is the duration between two consecutive peaks of ripples, and $\Delta V$ is the amount of ripple that can be tolerated by the load. From equation (9), it is seen that the small value of $\Delta V$ implies large $C_{EH}$. However, a larger value of $C_{EH}$ implies that more time will be taken by the capacitor to charge up to the peak value. Therefore, the capacitor might not be charged to the maximum input signal amplitude, which implies $\eta_c < 1$. Hence, depending upon the load conditions, a suitable value of $C_{EH}$ should be selected.

Generally, electronic systems have lower ripple tolerance capability, and hence $\Delta V \approx 1$mV has been considered in this paper. In order to have a fair comparison between low and high frequency setup, $C_{EH}$ for both setup have been calculated under similar load condition, i.e., $\Delta V \approx 1$mV. The value of $C_{EH}$ obtained for low and high frequency setup is 100 µF and 25 nF, respectively. It is observed that $C_{EH}$ for both setup is around $0.4 \times 10^{-3}$ F/s. However, the value of $V_{EH}$ is 307.16 mV and 304 mV for low and high frequency, respectively. Therefore, slightly lower conversion efficiency is obtained for high frequency setup under similar load condition. It may be noted that the high frequency setup can also attain $V_{EH} = 307.16$mV (same as of low frequency) if $C_{EH} = 7$ nF. However, such small value of $C_{EH}$ will provide high amount of ripples ($\Delta V > 7$ mV).

Furthermore, if harvested voltage has to drive an application or load which require supply voltage ($V_L$) much greater than $V_{EH}$, then dc-dc converter [40]–[42] can be deployed to boost.
Fig. 12. Harvested Voltage boosted to the required level ($V_L$) $V_{EH}$ up to $V_L$ in the EH branch as shown in Fig. 12.

V. REAL TIME VALIDATION OF eSampling

A. Hardware setup

To demonstrate the proposed eSampling framework in real world environment, a hardware set up similar to Fig. 2 a) has been built. The hardware prototype has been shown in Fig. 13. The input analog signal, $V_{in}(t)$ is obtained via the sensing of the external temperature using a sensing element i.e., thermal electric generator (TEG). TEG can produce an output voltage from 10 mV to 50 mV per °C change in temperature [43]. The switches $S_1$ and $S_2$ have been implemented using single pole double throw (SPDT) ADG791 monolithic CMOS switch. A $C_{lk}$ signal similar to the low-frequency simulation set up has been generated externally and applied to ADG719. The switch will connect the $V_{in}(t)$ to one output terminal for duration of 10% of the total sampling period ($T_s$) and to another output terminal with duration of 90% of the total sampling period, respectively. The output terminals obtaining 10% and 90% time of the total sampling period has been connected to $C_h$ for acquiring data samples and $C_{EH}$ for storing energy, respectively. The maximum voltage received at energy storage capacitor i.e., $V_{EH}$ is boosted up to 5V using a dc-dc converter i.e., LTC3108.

Fig. 13. Hardware Prototype

B. Experimental Results

Fig. 14 compares $V_{in}(t)$ with the sampled output voltage obtained at $C_h$ using eSampling. From the figure, it can be observed that the input signal is similar to the sampled output signal, and hence harvesting the energy along with sampling using eSampling is not degrading the performance of conventional sampling process of an ADC. The experiment has been computed for $f_s = 10$ KHz, $T_{aq} = 0.1 \ T_s$, and hence $T_{EH} = 0.9 \ T_s$. Furthermore, the harvested voltage has been boosted to $V_L = 5V$ by using LTC3108 as shown in Fig. 15. The remaining parameters used are as follows: $C_h = 1 \ \mu F$, $C_{EH} = 100 \ \mu F$ and $C_L = 10 \ \mu F$. The time required by $C_L$ to reach 5V is 16.58 seconds as shown in Fig. 15 with conversion efficiency of 64.98%.

VI. CONCLUSION

In this paper, modifications in conventional sampling circuitry of an ADC has been proposed for harvesting energy from the discarded portion of the input analog signal. The method is named as eSampling. For validating the presented method, CMOS 65 nm technology based system has been designed. In the experiment, only 10% of the sampling period has been used to sample the signal (with perfect recovery of the original analog signal subsequently), while rest 90% has been used for energy harvesting. The experiment has been performed at both low (10 KHz) as well as high frequency (40 MHz). It is observed that more than 65% conversion...
efficiency has been obtained with post-layout simulations for both experiments. The experiment has also been replicated on a hardware setup by obtaining the analog signal from TEG at 10 kHz sampling frequency. The obtained conversion efficiency is 64.98%.

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