Distributed Pinning Spot Model for High-k Insulator - III-V Semiconductor Interfaces

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III-V metal-insulator-semiconductor (MIS) structures are recently attracting attentions as possible candidates of high-k gate stack for next generation CMOS transistors on the silicon platform. However, their basic electrical properties are not well understood. In order to further confirm the validity of the recently proposed distributed pinning-spot (DPS) model for anomalous admittance behavior of III-V MIS structures, we have carried out in this paper a detailed experimental and computer simulation study of a HfO$_2$/GaAs high-k MIS structure controlled by a silicon interface control layer (Si ICL). It is clearly shown that the measured frequency dependences of C-V curves and admittance are far away from the predictions by the standard Si MOS theory. On the other hand, they can be well reproduced by the DPS model which assumes random spatial distribution of pinning spots with high densities of interface states in addition to pinning-free regions with low interface state densities. The model indicates that use of low-dimensional structures such as nanowires and nanodots may be beneficial for removal of pinning spots.

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I. INTRODUCTION

With the approach of the ultimate scaling limit of Si complimentary metal-oxide-semiconductor (CMOS) field effect transistors (FETs), strong interests have come back to III-V materials as candidates for alternative channel materials on the Si platform. Here, atomic scale control of the III-V semiconductor metal-insulator-semiconductor (MIS) interface is the key for success. As such control technologies, use of the Si interface control layer (Si ICL) structure [1, 2], use of the GaGuO/GaAs$_2$ structure [3], and use of atomic layer deposition (ALD) of high-k insulator [4] have achieved low values of interface state densities and realized III-V MISFETs which significantly outperform Si MOSFETs [2–4] due to higher values of the channel mobility. However, basic characterization and understanding of the electrical properties of the interface are still missing. In fact, we recently fabricated HfO$_2$/GaAs high-k MIS structures controlled by a Si ICL, and realized MIS interfaces free from Fermi level pinning [5]. However, we also observed various anomalies in the admittance behavior and proposed a distributed pinning-spot (DPS) model [6] as a possible model to explain them.

In order to further confirm the applicability of the DPS model, the purpose of this paper is to carry out a detailed experimental and computer simulation study of a HfO$_2$/Si ICL/GaAs high-k MIS structure. Marked anomalies were seen in the measured capacitance-voltage (C-V) and conductance curves, and serious difficulties were encountered in their interpretation by the standard Si MOS theory. Particularly, measured relaxation frequencies of capacitance and conductance were far away by many orders of magnitude from those predicted by the Si MOS theory. On the other hand, these anomalies could be well explained quantitatively by the DPS model which assumes random spatial distribution of pinning spots with high densities of interface states in addition to pinning-free regions with low interface state densities.

II. EXPERIMENTAL

The structure of the sample is shown in Fig. 1. The details of the fabrication process and its characterization by the in-situ X-ray photoemission spectroscopy was described elsewhere [5]. Briefly, it was fabricated as follows. The (001) surface of a molecular beam epitaxy (MBE)-grown GaAs layer was annealed with As-flux off to prepare a Ga-stabilized (4×6) surface. Then, the Si ICL was grown by MBE by carefully adjusting the temperature of the Si K-cell and growth time. Subsequently, the Si ICL was subjected to partial nitridation at room temperature by irradiation of a nitrogen radical beam in order to form Si$_3$N$_x$ layer which protects the interface structure from air exposure. Then, the sample was taken out from the ultra-high vacuum (UHV) system into the air and was transferred to a separate chamber for deposition of a HfO$_2$ film either by electron-beam evaporation.

FIG. 1: Sample structure.
SiO$_2$ additional layer was deposited by plasma CVD to enhance the insulator resistivity and breakdown strength to perform a reliable $C$-$V$ analysis without changing the interface structure. In this study, an initial Si ICL thickness of 3 monolayers (MLs) was used, although our previous study [7] has shown that an initial Si ICL thickness of 5-6 ML was optimum to obtain low interface state densities. This is because the frequency dispersion is more pronounced in the 3 ML sample, so that anomalies are more pronounced in $C$-$V$ and conductance curves. The sample was annealed at 400°C for 3 min in nitrogen.

III. RESULTS AND DISCUSSION

A. Experimental Results

The measured $C$-$V$ curves of the sample with Si ICL of 3 ML are shown in Fig. 2(a). Marked frequency dispersion is seen in $C$-$V$ curves. Presence of such frequency dispersion is very common in III-V MIS systems. It may also seem to be similar to the behavior of unoptimized Si MOS systems. The traditional approach to characterize III-V MIS interfaces has been to evaluate the distribution of the interface state density ($D_{it}$) from the 1MHz $C$-$V$ curve, using the Terman’s method or the high frequency capacitance method [8]. Here it is assumed that the capture and emission processes of all the interface states cannot follow the 1 MHz measurement signal. The result of such a $D_{it}$ analysis is shown in Fig. 2(b). For comparison, the $D_{it}$ distribution of a 5 ML-Si ICL sample is also shown. The results show U-shaped continuous distributions which are very commonly seen in the literature on III-V MIS systems. Closed squares in Fig. 2(b) show $D_{it}$ values obtained by conductance method which will be explained later.

We also measured the frequency dependences of MIS admittance, since the conductance method is believed to be the most accurate evaluation method of $D_{it}$ in the Si community [8]. Measured $G/\omega$ vs $f$ curves are shown in Fig. 3 for various values of the sample bias voltage, where $\omega$ is the angular frequency and $f$ is the frequency ($\omega = 2\pi f$). Appearance of peaks and their systematic shifts with the bias voltage are seen in $G/\omega$ vs $f$ curves of Fig. 3, which are expected from the Si MOS theory. One anomaly noted here is that the value of $G/\omega$ does not seem to become zero away from the peak, leaving a almost bias-independent conductance off-set value.

B. Interpretation by Standard Si MOS Theory

Apart from the conductance offset mentioned above, the frequency dependences of $C$-$V$ curves and those of conductance curves seem to agree qualitatively with those seen in the Si MOS systems. In order to investigate whether the measured results can be explained quantitatively by the Si MOS theory, $C$-$V$ and conductance curves were calculated by using the standard Si MOS theory.

For this, we started from the measured $D_{it}$ distribution of the 3 ML sample shown in Fig. 2(b), and calculated the capacitance and conductance of the MIS structure as functions of bias voltage and frequency, using the standard equivalent circuit shown in Fig. 4(a) where $C_I$ is the insulator capacitance, $C_D$ is the semiconductor depletion-layer capacitance, and $C_P$ and $G_P$ are the frequency dependent interface-state capacitance and conductance, respectively. In the calculation, $C_D$ was computed using the standard F-function in the text book [8]. For the cal-

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![Fig. 2: (a) Measured $C$-$V$ curves for a high-$k$ GaAs MIS structures with 3 ML Si ICL and (b) $D_{it}$ distribution evaluated from $C$-$V$ curves in Fig. 2(a) (solid lines). $D_{it}$ distribution of a 5 ML sample is also shown for comparison. Closed squares show $D_{it}$ values by conductance method explained later.](image-url)
where \( \sigma_B \) and \( \sigma_S \) denote the standard deviations of the surface potential due to fluctuation of the bulk doping and that of the interface fixed charge, respectively. A similar equation exists for \( C_p \), which is not shown here.

In both cases, the time constant of the interface state was obtained by using the following standard equation:

\[
\tau(E) = \frac{1}{\sigma_{0n} N_C v_{th}} \exp \left( \frac{E_C - E}{kT} \right)
\]

(4)

where \( \sigma_{0n} \) is the electron capture cross section of the interface state, \( N_C \) is effective density of states of the conduction band, and \( v_{th} \) is the thermal velocity of electrons.

The calculated \( C-V \) curves using the continuum model are shown by solid curves in Fig. 4(b) together with the measured curves shown by dashed lines. Here we used \( N_C = 4.7 \times 10^{17} \text{ cm}^{-3} \), \( v_{th} = 7 \times 10^6 \text{ cm/s} \), and \( \sigma_{0n} = 1 \times 10^{-15} \text{ cm}^2 \). Since the flat band voltage shifts are not discussed in this paper, the theoretical curves were shifted toward right so that both of theoretical and experimental 1 MHz curves overlap. It should be noted that only majority carrier response of interface states was considered in this calculation. Thus, the capacitance dip on the lowest-frequency theoretical curve, which is reminiscent of the minority carrier response, is actually due to the U-shaped \( D_N \) distribution. If the minority carrier responses are taken into account, \( C-V \) curves in the weak inversion regime may change rather drastically. However, such details are beyond the scope of the present paper.

The calculation reproduces the experimental 1 MHz curve very well up to the bias voltage of about 7 V beyond which it deviates. This deviation takes place at the surface potential position around 0.2 eV below \( E_C \). Thus, it is either due to the fact that the response of the interface states becomes faster than 1 MHz in spite of the assumption of \( C_p \) and \( G_p \), two models including the effect of the so-called time constant dispersion were used. One is the continuum model taking account of thermal spread of Fermi distribution. For this case, \( G_p \) is given by:

\[
\frac{G_p(\omega)}{\omega} = \frac{C_S}{2} \frac{1}{\sqrt{2\pi(\sigma_S^2 + \sigma_B^2)}} \int_{-\infty}^{\infty} \exp \left\{ \frac{(E - E_0)^2}{2(\sigma_S^2 + \sigma_B^2)} \right\} \frac{1}{\omega \tau(E)} \ln \left\{ 1 + (\omega \tau(E))^2 \right\} dE,
\]

(3)

where \( C_S \) is the interface state capacitance at the low-frequency limit given by:

\[
C_S = q^2 D_{it},
\]

(2)

and \( \tau \) is the time constant of the interface state lying at energy, \( E \), below the conduction band edge, \( E_C \). A similar equation exits for \( C_p \) which is not shown here.

The other model was the statistical model taking into account of surface potential fluctuation caused by fluctuation of doping and interface fixed charge. For this case, \( G_p \) is given by:

\[
\frac{G_p(\omega)}{\omega} = \frac{C_S}{2} \frac{1}{\omega \tau(E_0)} \ln \left\{ 1 + (\omega \tau(E_0))^2 \right\}.
\]

(1)

where \( C_S \) is either due to the fact that the response of the interface states becomes faster than 1 MHz in spite of the assumed behavior of the 1 MHz curve being the high-frequency limit, or due to the fact that the capture cross-section of the interface state is larger than the assumed value. This discrepancy is a minor one, and can be resolved by a further detailed study. In contrast to this, a much more serious discrepancy lies on the lower frequency side. Namely, we see that large discrepancies exist in the values of the relaxation frequency of \( C-V \) curves. For example, near a bias voltage of 3 V which roughly corresponds to the surface potential at the midgap, the theoretical curve for \( 10^{-2} \text{ Hz} \) shows a rapid relaxation whereas the closest experimental \( C-V \) curve for this relaxation is that for \( 100 \text{ kHz} \), implying a large difference of 13 orders of magnitude in frequency scale. Such a discrepancy reduces as the frequency is raised, and almost disappears at around \( 1 \text{ MHz} \).

One may be surprised at the appearance of such slow relaxation frequencies in theory. However, this is simply because the energy gap of GaAs is much larger than that of Si. Thus, for example, the time constant of GaAs midgap states is about 300 sec, whereas that for Si midgap states is about \( 10^{-2} \text{ sec} \). Thus, relaxation frequencies much slower than those in Si MOS are naturally expected.

It is obvious that the observed discrepancy is too large to be resolved by adjustments of parameters such as the capture cross-section. Use of the statistical model was also tried. But, the simulated \( C-V \) curves remained almost the same with those by the continuum model, as expected.

Additionally, the calculated conductance curves are shown in Fig. 5. Here, since the continuum model gives conductance peaks with narrow peak widths, the statis-
cal model with an arbitrary value of $(\sigma_B^2 + \sigma_S^2) = 0.001$ was used, so that the full widths at half maximum (FWHM) of the conductance peaks become comparable to those of the experimental curves. Again, it is clear that the calculated values of the frequency which gives the conductance peak are very far away from those of the experimental conductance peaks seen in Fig. 3.

Thus, attempts to interpret the measured $C$-$V$ and conductance curves quantitatively by the standard Si MOS theory have totally failed. Since our $C$-$V$ and conductance data are similar to those reported on III-V MIS structures, we believe that this is a general conclusion concerning the electrical properties of III-V MIS interfaces.

C. Interpretation by Distributed Pinning Spot Model

In an attempt to explain the frequency dispersion behavior of GaAs MIS $C$-$V$ curves, we have recently
A distributed pinning spot (DPS) model [6]. The concept of this model is schematically illustrated in Fig. 6(a). Traditionally, in assessments of any MIS systems including the Si MOS system, it has been tacitly assumed that the interface states are distributed uniformly over the interface. The statistical model deals with spatial non-uniformity, but it takes account of the lateral fluctuation of the surface potential, but not that of the interface state density. In contrast to this, the DPS model assumes that the \( D_{\text{L}} \) distribution is not uniform laterally over the interface, as shown in Fig. 6(a). More specifically, pinning spots having high density of interface states are distributed randomly in the sea of nearly ideal pinning-free region with low interface state densities. The pinning spots have a strong tendency to pin the Fermi level locally on the spot.

The lateral cross-section of the MIS structure and its equivalent circuit for the DPS model are shown in the DPS model in Fig. 6(b). Here, the pinning-free region has a bias dependent surface potential, \( \Psi_S \), whereas the pinning spot has an almost bias-independent surface potential, \( \Psi_{S_{\text{ps}}} \).

Since the interface state capacitance at the pinning spot, \( C_{S_{\text{ps}}} \), is expected to be much larger than the insulation capacitance, \( C_I \), the contribution of the pinning spots to the total MIS capacitance is approximately given by \( \alpha C_I \), being independent of bias and frequency. As for the conductance contribution of the pinning spots, one has to take account of the fact that spot-to-spot variation of \( \Psi_{S_{\text{ps}}} \) is expected to be large, making the overall shape of the conductance peak a very flat one. From such considerations, the following approximate relations for the MIS capacitance, \( C \), and conductance, \( G \), have been derived [6]:

\[
\frac{C}{C_I} = (1 - \alpha) \frac{(C_D + C_P(\omega))(C_I + C_D + C_P(\omega)) + (G_P/\omega)^2}{(C_I + C_D + C_P(\omega))^2 + (G_P/\omega)^2} + \alpha, \tag{5}
\]

\[
\frac{G/\omega}{C_I} = (1 - \alpha) \frac{C_I(G_P/\omega)}{(C_I + C_D + C_P(\omega))^2 + (G_P/\omega)^2} + \alpha \frac{C_I}{C_{S_{\text{ps}}}}, \tag{6}
\]

where \( \alpha \) is the fraction of the total area occupied by pinning spots out of the whole interface area. The second term in Eq. (6) provides an explanation for the conductance offset seen in Fig. 3.

It may seem at first sight that pinning spots and the pinning-free regions are independent without any interaction. However, this is impossible due to long range nature of Coulomb force. A more realistic situation is that the potential profile of the pinning-free region is modified by that of the high potential mountains of the pinning spots. Such an interaction has been indeed reported in heterogeneous Schottky barriers as discussed by Tung [9]. The situation is schematically shown in Fig. 7 where the potential profile of the pinning free region is modified so as to produce a saddle point. Then, such a profile can have two surface potentials. One is the actual surface potential, \( \Psi_{S_{\text{SS}}} \), at the interface, and the other is the effective surface potential, \( \Psi_S \), determined by the extension of the inner part of the potential profile. The proposed potential profile is related to the admittance measurement in the following way. Since \( \alpha \ll 1 \), the predominant part of the MIS admittance comes from the pinning-free region in Fig. 6(b) where the potential profile is now assumed to possess a saddle point. When the frequency is so high that the interface states in the pinning free region cannot respond to the small a.c. signal, only free electrons deep beyond the saddle point can respond to the a.c. signal. Thus, the high frequency capacitance measurement detects \( \Psi_S \). However, as the frequency is lowered, the interface states of the pinning-free region start to respond where the relaxation frequency of states is determined by \( \Psi_{S_{\text{SS}}} \). Thus, the conductance measurement should determine the value of \( \Psi_{S_{\text{SS}}} \). This model can provide an explanation for the observed extremely high relaxation...
Fig. 8: (a) $G_p/\omega - f$ plot and their fitting to the statistical model (dashed lines) and to the tunneling model (solid lines). (b) Calculated C-V data points in comparison with measured C-V curves.

frequencies of admittance observed at a low bias corresponding to a large value of $\Psi_{SS}$, or a large band-bending. If the present model is correct, the conductance method measures the real $D_{\text{eff}}$ values of the pinning-free region while the high frequency $C$-V measurement gives a gross effective $D_{\text{eff}}$ distribution of the whole interface, including contributions from the pinning spots.

In order to see whether the DPS model can reproduce the observed C-V and conductance curves, we tried to convert the observed MIS conductance to interface state conductance $G_p$ at selected bias points. Here, the usual conversion procedure is to use the following equation:

$$G_p = \frac{C_f^2 (G/\omega)}{(G/\omega)^2 + (C_f - C)^2}.$$  \hspace{1cm} (7)

However, this procedure did not work properly, because it led to $G_p/\omega - f$ curves showing monotonically decreasing behavior vs. frequency without any peaks. On the other hand, use of the approximate equations, Eqs. (5) and (6), produced conductance peaks as shown in Fig. 8(a), where the peak positions shifted systematically with bias as we expected. Here, the value of the offset conductance of 1.3 pF in Fig. 3, while a value of $\alpha$ was assumed to be $\alpha = 0.01$.

Then, attempts were made to fit the resultant peak profiles to existing conductance models, including the continuum model [8] given in Eq.(1), the statistical model [8] given in Eq.(3) and the tunneling model [10]. In the last tunneling model, interface states are assumed to be traps distributed in space and energy in the insulator near the interface. Then, the time constant dispersion is caused by tunneling of electrons into these trapping states with various tunneling distances. According to this model, the conductance is given by the following equation [10];

$$G_p(\omega) = \frac{C_S}{2} \frac{(\omega \tau_0)^{1/\gamma}}{\gamma} \int_0^{1/(\omega \tau_0)} z^{1/\gamma} \ln \left( 1 + \left( \frac{1}{z} \right)^2 \right) dz,$$  \hspace{1cm} (8)

where $\tau_0$ is dominant time constant. $\gamma$ is the quantity given by;

$$\gamma = 2 \sqrt{\frac{2m^*_e \Delta E_C}{\hbar}} x_{SS}.$$  \hspace{1cm} (9)

Here, $m^*_e$ is the effective mass of electron, $\Delta E_C$ is an energy barrier for electron, $\hbar$ is the Planck constant and $x_{SS}$ is the decay distance of interface state distribution into the insulator where we have assumed an exponentially decaying spatial distribution.

As a result of fitting trials, the conductance continuum model did not work due to too small peak widths. Results of fitting attempts to the statistical model are shown in Fig. 8(a) by dashed curves. Fitting could be made only partially due to the asymmetrical shapes of the measured conductance peaks. On the other hand, excellent fittings could be made with the tunneling model as shown by the solid curves in Fig. 8(a). This is similar to the anodic oxide/GaAs case which our group studied long time ago [11].

Using the conductance method based on the tunneling model, $D_{\text{eff}}$ values were evaluated as shown by closed squares in Fig. 2(b) where energy position was determined by Eq. (4). Here, a value of the capture cross-section of $1 \times 10^{-15}$ cm$^2$ was used as a typical value for MIS interface states. The values of $\Psi_S$ and $\Psi_{SS}$ determined, respectively, by the high frequency C-V method

| V [V] | E - $E_C$ [eV] |
|-------|----------------|
| 2     | -0.94          |
| 5     | -0.54          |
| 9     | -0.22          |

| $\Psi_S$ by C-V method | $\Psi_{SS}$ by conductance method |
|------------------------|----------------------------------|
| -0.30                  | -0.20                            |

TABLE I: Values of two surface potentials defined in Fig. 7.
and by the conductance method are compared in Table I. Except the case of 9 V bias where the saddle point disappears, two values are very different. According to the DPS model, the extremely large discrepancies in relaxation frequencies which were observed in attempting to interpret the measured $C-V$ and conductance curves by the Si MOS theory, are caused by the these differences between two surface potentials. It is now apparent that the measured conductance curves can be completely reproduced theoretically by using the tunnelling model and two surface potentials listed in Table I.

$C-V$ points calculated using Eqs. (5) and (6) are also plotted in Fig. 8(b) by circles and squares on the measured $C-V$ curves. It is seen that the calculation based on the DPS model can reproduce the measured $C-V$ curves reasonably well in spite of approximate nature of Eqs. (5) and (6) and presence of various fitting errors.

Thus, the basic validity of the DPS model has been confirmed quantitatively in this study. However, formation of potential saddle points with two characteristic surface potential values remained to be an assumption throughout this study. For this, a future three-dimensional potential simulation study is necessary to confirm formation of such a potential profile as well as to clarify its relation to separation of pinning spots, their pinning strength, bias conditions and overall $D_{it}$ distributions. A previous study on inhomogeneous Schottky barriers [9] as well as our potential simulation on nanometer-size Schottky dots seems to indicate that the separation of pinning spots is several ten to hundred nanometers for production of saddle points. The origin of pinning spots is also an unsolved issue. One possible mechanism is the random stress produced by bond-mismatches at the interface which may produce misfit dislocations or other types of bond disorder. If this is the case, low-dimensional structures such as nanowires and nanodots [12] whose sizes are smaller than the distance of pinning spots may be effective to avoid formation of pinning spots.

IV. CONCLUSIONS

A detailed experimental and computer simulation study of a HfO$_2$/GaAs high-$k$ MIS structure controlled by a silicon interface control layer (Si ICL) was carried out in order to check the validity of the recently proposed distributed pinning-spot (DPS) model. By carrying out computer simulations of $C-V$ and curves, it has been clearly shown that the measured frequency dependences of $C-V$ curves and admittance are far away from the predictions by the standard Si MOS theory. Then, a detailed analysis of the measured conductance has been made from the viewpoint of the DPS model. It has been shown that the measured data can be well reproduced by the DPS model which assumes formation of potential profiles with saddle points as a result of electrostatic interaction between the pinning spots with high densities of interface states and the pinning-free regions with low interface state densities. The model indicates that use of low-dimensional structures such as nanowires and nanodots may be beneficial for future removal of pinning spots.

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