Energy-efficiency evaluation of Intel KNL for HPC workloads

Enrico CALORE\textsuperscript{a1}, Alessandro GABBANA\textsuperscript{a}, Sebastiano Fabio SCHIFANO\textsuperscript{a} and Raffaele TRIPICCIONE\textsuperscript{a}

\textsuperscript{a}University of Ferrara and INFN, Italy

Abstract. Energy consumption is increasingly becoming a limiting factor to the design of faster large-scale parallel systems, and development of energy-efficient and energy-aware applications is today a relevant issue for HPC code-developer communities. In this work we focus on energy performance of the Knights Landing (KNL) Xeon Phi, the latest many-core architecture processor introduced by Intel for the HPC market. We take into account the 64-core Xeon Phi 7230, and analyze its energy efficiency using both the on-chip MCDRAM and the regular DDR4 system memory as main storage for the application data domain. As a benchmark application we use a Lattice Boltzmann code heavily optimized for this architecture, and implemented using different memory data layouts to store the data-domain. We then assess the energy consumption using different data-layouts, memory configurations (DDR4 or MCDRAM), and number of threads per core.

Keywords. Energy, KNL, MCDRAM, Memory, Lattice Boltzmann, HPC

1. Introduction

Energy consumption is quickly becoming one of the critical issues in modern HPC systems, and HPC facilities are constantly trying to increase their energy-efficiency, in order to hold down the total cost of ownership, increasingly given by the electricity bill. Processors and accelerators are the main sources of power drain in computing systems \cite{1} and thus assessing their energy-efficiency is of paramount importance for the design of efficient parallel systems. Hardware manufacturers are clearly trying to improve the energy-efficiency increasing the peak FLOP/watt ratio of their architectures \cite{2}. Beside of this, it is also relevant to analyze and profile the hardware energy-performance running real-applications, since high energy-efficient processors may behave highly inefficiently when running codes unable to exploit a large fraction of their peak performance. For this reason in this work we study the energy-efficiency of the Intel Knights Landing (KNL) architecture, using as a benchmarking code a real HPC application, heavily optimized for several architectures and used for production runs of fluid-dynamics simulations based on Lattice Boltzmann methods. This application is a good representative of a wider class of lattice based stencil-codes, including also HPC Grand Challenge applications such as Lattice Quantum Chromodynamics (LQCD) \cite{3,4,5,6}.

\textsuperscript{1}Corresponding Author: Enrico Calore, University of Ferrara and INFN, Via Saragat 1, I-44122 Ferrara Italy; E-mail: enrico.calore@unife.it.
The Intel KNL features a 16GB on-package HBM (High Bandwidth Memory) namely MCDRAM (Multi-Channel DRAM) which resides on the CPU chip, close to the processing cores. This memory can be configured as a wide cache, interposed between the cores and the DDR4 system memory, or as a separate addressable space.

In this work we evaluate the impact on the energy consumption required by the KNL to complete different kernels of our application, using different number of threads per core, different memory configurations (i.e. MCDRAM and DDR4), and different memory data layouts. We then compare the results with recent NVIDIA GPUs. To benchmark different processors we adopt different code implementations of the same LBM application, each specifically optimized for a different target system.

2. Lattice Boltzmann Application

Behaviour of flows are widely described using the Lattice Boltzmann method (LB) \cite{7} based on the synthetic dynamics of populations sitting at the sites of a discrete lattice. These methods, discrete in position and momentum spaces, propagate populations from lattice-sites to lattice-sites, and then collide them changing their values accordingly. In this work we consider a state-of-the-art $D_2Q_{37}$ LB model with 37 populations per lattice-site, that correctly reproduces the thermo-hydrodynamical evolution of a fluid in two dimensions, and enforces the equation of state of a perfect gas ($p = \rho T$) \cite{8,9}. This model has been extensively used for large scale simulations of convective turbulence \cite{10} on HPC systems \cite{11}.

A Lattice Boltzmann simulation starts with an initial assignment of the populations values, and then for each lattice-point applies in sequence two kernel functions as many time-steps as needed. The first kernel, called propagate, moves populations across lattice sites collecting at each site all populations that will interact at the next step (collide) according to an appropriate stencil depending on the LB model used. This kernel performs only a large number of sparse memory accesses, and for this reason is strongly memory-bound. The latter, called collide, uses as input the populations gathered by the previous propagate kernel, and performs all the mathematical steps associated to the computation of the new population values. This function is strongly compute-bound making heavy use of the floating-point units of the processor. These two kernels take a large fraction of the simulation execution time.

In the last years several implementations of this model have been developed, and used both for convective turbulence studies \cite{12}, and as benchmarks to profile performance of recent developed HPC hardware architectures based on commodity CPUs and GPUs \cite{13,14,15,16,17}. In this work we use an implementation initially developed for Intel CPUs \cite{18}, and later ported and optimized for the Intel Knights Corner (KNC) processor \cite{19,20}.

3. The Knights Landing Architecture

The Knights Landing (KNL) is the first generation of self-bootable processor based on the Many Integrated Cores (MIC) architecture developed by Intel. The processor integrates an array of 64, 68 or 72 cores together with four high speed Multi-Channel DRAM
(MCDRAM) memory banks, providing an aggregate raw peak bandwidth of more than 450 GB/s [21]. It also integrates 6 DDR4 channels supporting up to 384 GB of memory with a peak raw bandwidth of 115.2 GB/s. Two cores are bonded together into a tile sharing an L2-cache of 1 MB. Tiles are connected by a 2D-mesh of rings and can be clustered in several NUMA configurations. In this work we only run using the Quadrant cluster configuration where the array of tiles is partitioned in four quadrants, each connected to one MCDRAM controller. This configurations is the one recommended by Intel to run applications using the KNL as a symmetric multi-processor, as it reduces the latency of L2-cache misses, and the 4 blocks of MCDRAM appear as contiguous block of memory addresses [22].

MCDRAM on a KNL can be configured at boot time as Flat, Cache or Hybrid mode. The Flat mode configures the MCDRAM as a separate addressable memory, Cache mode configures the MCDRAM as a last-level cache. The Hybrid mode, allows to use the MCDRAM partly as addressable memory and partly as last-level cache [23]. In this work we only consider Flat and Cache configurations.

KNL allows to exploit two levels of parallelism: the first is the task parallelism built onto the array of cores, and the latter is the data parallelism using the AVX 512-bit vector (SIMD) instructions. Each core has two out-of-order vector processing units (VPUs) and supports the execution of up to 4 threads. The KNL has a peak theoretical performance of 6 TFlops in single precision and 3 TFlops in double precision, and the typical thermal design power (TDP) is 215 W, including MCDRAM memories. For more details on KNL architecture see [24].

4. Measuring Energy Consumption on the KNL

As other Intel processors – starting from Sandy Bridge architecture onward – the KNL integrates power meters and a set of Machine Specific Registers (MSR) that can be read through the Running Average Power Limit (RAPL) interface. In this work we use the PACKAGE_ENERGY and DRAM_ENERGY counters to monitor respectively the energy consumption of the processor Package (accounting for: Cores, Caches and MCDRAM) and the DRAM memory system.

A popular way to access these counters is through a library named PAPI [25] providing a common API for energy/power readings for different processors, partially hiding architectural details. The use of this technique to read energy consumption figures from Intel processors is a consolidate practice [26], validated by several third parties studies [27,28].

On top of the PAPI library we have developed a custom library to manage power/energy data acquisition from hardware registers. It allows benchmarking codes to directly start and stop measurements, using architecture specific interfaces, such as RAPL for Intel CPUs and the NVIDIA Management Library (NVML) for NVIDIA GPUs [29]. Our library also lets benchmarking codes to place markers in the data stream in order to have an accurate time correlation between the running kernels and the acquired power/energy values. Our code, exploiting the PAPI library, is available for download as Free Software [30].

We use the energy-to-solution (E_s) as metric to measure the energy-efficiency of processors running our application. This is defined as product of time-to-solution (T_s) and
average power ($P_{avg}$) drained while computing the workload: $E_s = T_s \times P_{avg}$. To measure $P_{avg}$ we read the RAPL hardware counters thanks to our wrapper library, and then convert readout values to Watt. The Package and DRAM power drains can then be summed to obtain the overall value or analyzed separately.

In the following, we measure this metric for the two most time consuming kernels of our application, *propagate* which is strongly memory-bound, and *collide* which is strongly compute-bound.

5. Experimental Results

The LB application described in Sec. 2 has been originally implemented using the AoS (Array of Structure) data layout, showing a satisfactory performance on CPU processors. While porting the application to GPU devices, a data layout re-factoring has been implemented to fully exploit the parallelism of GPUs, leading to an implementation based on the SoA (Structure of Array) data layout.

More recently, two slightly more complex data layouts have been introduced \cite{31} in the quest of a single data structure to be used for a portable implementation, allowing good performances on most architectures. These data structures, named: CSoA (Clustered Structure of Array) and the CAoSoA (Clustered Array of Structure of Array), allow to exploit vectorization on both CPUs and GPUs, still guaranteeing efficient data memory accesses and vector processing, for both of our application’s critical kernels.

In this work we test all of the above data layouts on the KNL architecture, measuring the energy consumption of both the Package and DRAM. Moreover we run with various number of threads and with different memory configurations: i) allocating the lattice only in the DRAM using the Flat/Quadrant configuration; ii) allocating the lattice only in the MCDRAM using the Flat/Quadrant configuration; or iii) allocating the lattice only in the DRAM, but using the MCDRAM as a last level cache, using the Cache/Quadrant configuration. In the latter case we use a bigger lattice, which could not fit in the cache, and for this reason we report all the results normalized per lattice site. Our aim is to analyze and highlight possible differences in performance, average power, and energy-efficiency.

In Fig. 1a and Fig. 1b we show the results of our tests, where Power and Energy values account for the sum of Package and DRAM contributions and Energy is normalized per lattice site.

Concerning the *propagate* function, as shown in Fig. 1a using Flat-mode and allocating the lattice in the MCDRAM memory, the maximum bandwidth using the AoS data layout is 138 GB/s, while using SoA it can be increased to 314 GB/s (i.e., 2.3×), and then can be further increased using CSoA layout, reaching a peak bandwidth of 433 GB/s (3.1× w.r.t AoS). When using just the regular DRAM, bandwidth drops for all the data layouts: 51 GB/s for AoS, 56 GB/s for SoA, and 81 GB/s for CSoA. When using the Cache-mode with a bigger lattice size, which do not fits in the MCDRAM, we measure a quite constant bandwidth of 59, 60 and 62 GB/s respectively for AoS, SoA and CSoA. The CAoSoA data layout on the other side, do not provides any benefit over the CSoA for the *propagate* function, but as we see in Fig. 1b it is beneficial for the performance of the *collide*.

We record the best $E_s$ using Flat-MCDRAM configuration and the CSoA data layout with a result of $\approx 2.5\times$ energy saving wrt using the AoS data layout.
(a) *propagate* function: we report $T_s$ in nano-seconds per site (Top), $P_{avg}$ in Watt (Middle) and $E_s$ in micro-joules per site (Bottom).

(b) *collide* function: we report $T_s$ in nano-seconds per site (Top), $P_{avg}$ in Watt (Middle) and $E_s$ in micro-joules per site (Bottom).

Figure 1. All the performed tests for the three memory configuration (DDR4 Flat, MCDRAM Flat and Cache) and for different thread numbers (64, 128, 192 and 256). We report three metrics: the time-to-solution ($T_s$), the average Power drain ($P_{avg}$) and the energy-to-solution ($E_s$). In Fig 1a for the *propagate* function and in Fig 1b for the *collide*. 
From the point of view of all the evaluated metrics, using just 64 threads is the best choice, since it gives the best performance plus the lowest Power drain and Energy consumption. This is justified by the fact that the propagate function is completely memory-bound and 64 threads are enough to keep fully busy the memory controllers.

Concerning the collide function, similar plots are reported in Fig. [15] where again the average Power drain and \( E_S \) are given as the sum of Package and DRAM contributions and \( E_S \) is normalized per lattice size. For Flat-MCDRAM configuration, performance increases when changing the data layout from AoS to CSoA and in this case it can be further increased changing to CAoSoA. On the other side, the worst performance is shown using SoA, since vectorization can not be exploited successfully in this case, and moreover memory-alignment can not be granted. When using CAoSoA we measure a sustained performance of \( \approx 1 \text{Tflops} \), corresponding to \( \approx 37\% \) of the raw peak performance of the KNL. From our measures, the CAoSoA layout gives the best \( E_S \), \( \approx 2 \times \) lower wrt to the AoS, both for performance and \( E_S \).

In contrast to the behaviour of the propagate, for the collide function \( E_S \) decreases using more threads per CPU since this kernel is compute-bound.

For both functions we see that the \( E_S \) differences, between the various tests performed, are mainly driven by \( T_S \). Despite the fact that average Power drain shows differences up to \( \approx 30\% \), it seems always convenient to choose the best performing configuration from the \( T_S \) point of view, to obtain also the best energy-efficiency.

In Fig. 3 we highlight the \( E_S \) metrics for all the different data layouts, using the Flat configuration and thus using either the off-chip (DDR4) or the on-chip (MCDRAM) memory, to allocate the whole lattice. Here we display separately the Package and DRAM contributions, where for each bar in the plot, Package energy is in the bottom and DRAM energy on top. When using the MCDRAM, its energy consumption is accounted with the rest of the Package and thus what is displayed as DRAM energy is just due to the idle Power drain.

The main advantage in using the MCDRAM is clearly for the propagate function where we can save \( \approx 2/3 \) of the energy wrt the best performing test run using the DDR4 system memory (be aware of the different scales in the y-axes of Fig. [22]). Anyhow, also for the collide function, shown in Fig. [20] we can halve the energy consumption. In both the cases the energy saving is mainly given by the reduced execution time, since the DDR4 average Power drain accounts at most for \( \approx 10\% \).

6. Comparison with other architectures

In this section we comment on the energy-efficiency of the KNL, comparing it to other processors and accelerators. We have run different implementations of the same code presented in Sec. 2, each optimized for a specific processor or accelerator, and we have measured the corresponding energy-to-solutions. To read power and energy hardware counters we have used our custom wrapper code based on the PAPI library presented in Sec. 4.

In Fig. 3 we compare the energy-efficiency of a KNL with that of a GK210 GPU hosted into an NVIDIA K80 board. We have configured the KNL in Flat mode, and used a lattice size that fits in the 16GB of the KNL’s MCDRAM as well as in the on-board GPU memory. For both the architectures we report the results using a naive AoS implementation and using the respective best performing memory layout.
(a) *propagate* function. Flat configuration, using the DDR4 system memory (Top) and the MCDRAM (bottom). We highlight to the reader the different scales on the y-axes.

(b) *collide* function. Flat configuration, using the DDR4 system memory (Top) and the MCDRAM (bottom).

**Figure 2.** Energy consumption in nano-joules per lattice site, using different memory data layouts and different number of threads. Each bar represents the Package Energy (bottom), plus the DRAM energy (top), which is just the DRAM idle energy consumption, when using the MCDRAM.
To use the AoS data layout is sub-optimal for both the architectures, and the KNL exhibits a lower $E_S$ than the GPU by a factor $\approx 3x$ for both propagate and collide kernels. Using the most energy-efficient data layout for both architectures – i.e., CAoSoA for the KNL and SoA for the GK210 – the propagate and the collide kernels are respectively $\approx 31\%$ and $\approx 55\%$ more energy-efficient on the KNL compared to the GPU. Using the Cache configuration for the KNL (not shown Fig. 3), if the lattice fits into the cache, computing performance and energy-efficiency are the same measured for Flat mode. For lattices which do not fit into the cache, both computing performance and energy-efficiency of the KNL drops to the level of standard multi-core Intel Xeon CPUs.

Considering the fact that the KNL architecture is more recent than the GK210 used in this comparison, we can conclude that the energy-efficiency of Intel Xeon Phi and of NVIDIA GPUs is comparable if data can fit in the KNL’s MCDRAM.

7. Conclusion and future works

In this work we have investigated the energy-efficiency of the Intel KNL for Lattice Boltzmann applications, assessing the energy to solutions for the most compute relevant kernels, i.e., propagate and collide. Based on our experience in using the KNL, related to our application, and the experimental measures we have observed, some concluding remarks are in order:

i) applications previously developed for ordinary X86 multi-core CPUs can be easily ported and run on KNL processors;

ii) performance is strongly affected by the level of vectorization and core parallelism that applications are able to exploit, otherwise a drop to the level of ordinary multi-core CPUs or even worst can be easily observed;

iii) for LB applications – and for many others – appropriate data layouts plays a relevant role to allow for vectorization and an efficient use of the memory sub-system, improving computing and energy efficiency;

iv) if application data fits within the MCDRAM, performance of KNL are very competitive with that of recent GPU accelerators in terms of both computing and energy-
efficiency; unfortunately, if this is not the case, performance drops to levels of ordinary multi-core CPUs or even worst;

In the future, we plan to further investigate energy-efficiency of the KNL providing a more comprehensive comparison, taking into account more recent GPUs architectures (such as Pascal and Volta), and also exploring the possibility to use DVFS to tune the KNL clock frequency.

Acknowledgements

This work was done in the framework of the COKA, COSA projects of INFN, and the PRIN2015 project of MIUR. We would like to thank CINECA (Italy) for access to their HPC systems. AG has been supported by the EU Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No 642069.

References

[1] Ge, R., Feng, X., Song, S., Chang, H.C., Li, D., Cameron, K.W.: Powerpack: Energy profiling and analysis of high-performance systems and applications. IEEE Transactions on Parallel and Distributed Systems 21(5), 658–671 (2010), doi:10.1109/TPDS.2009.76
[2] Attig, N., Gibbon, F., Lippert, T.: Trends in supercomputing: The european path to exascale. Computer Physics Communications 182(9), 2041 – 2046 (2011), doi:10.1016/j.cpc.2010.11.011
[3] Bernard, C., Christ, N., Gottlieb, S., Jansen, K., Kenway, R., Lippert, T., Mackenzie, P., Niedermayer, F., Sharpe, S., Tripiccione, R., Ukawa, A., Wittig, H.: Panel discussion on the cost of dynamical quark simulations. Nuclear Physics B - Proceedings Supplements 106(Supplement C), 199 – 205 (2002), doi:10.1016/S0920-5632(01)01664-A
[4] Bilardi, G., Pietracaprina, A., Pucci, G., Schifano, F., Tripiccione, R.: The potential of on-chip multiprocessing for QCD machines. Lecture Notes in Computer Science 3769, 386–397 (2005), doi:10.1007/11602569_41
[5] Bonati, C., Calore, E., Coscetti, S., D’Elia, M., Mesiti, M., Negro, F., Schifano, S.F., Tripiccione, R.: Development of scientific software for HPC architectures using OpenACC: the case of LQCD. In: The 2015 International Workshop on Software Engineering for High Performance Computing in Science (SE4HPCS). pp. 9–15. ICSE Companion Proceedings (2015), doi:10.1109/SE4HPCS.2015.9
[6] Bonati, C., Coscetti, S., D’Elia, M., Mesiti, M., Negro, F., Calore, E., Schifano, S.F., Silvi, G., Tripiccione, R.: Design and optimization of a portable LQCD Monte Carlo code using OpenACC. International Journal of Modern Physics C 28(5) (2017), doi:10.1142/S0129183117500632
[7] Succi, S.: The Lattice-Boltzmann Equation. Oxford university press, Oxford (2001)
[8] Sbragaglia, M., Benzi, R., Biferale, L., Chen, H., Shan, X., Succi, S.: Lattice Boltzmann method with self-consistent thermo-hydrodynamic equilibria. Journal of Fluid Mechanics 628, 299–309 (2009), doi:10.1017/S002211200900665X
[9] Scagliarini, A., Biferale, L., Sbragaglia, M., Sugiyama, K., Toschi, F.: Lattice Boltzmann methods for thermal flows: Continuum limit and applications to compressible Rayleigh–Taylor systems. Physics of Fluids (1994-present) 22(5), 055101 (2010), doi:10.1063/1.3392774
[10] Biferale, L., Mantovani, F., Sbragaglia, M., Scagliarini, A., Toschi, F., Tripiccione, R.: Second-order closure in stratified turbulence: Simulations and modeling of bulk and entrainment regions. Physical Review E 84(1), 016305 (2011), doi:10.1103/PhysRevE.84.016305
[11] Biferale, L., Mantovani, F., Pivanti, M., Sbragaglia, M., Scagliarini, A., Schifano, S.F., Toschi, F., Tripiccione, R.: Lattice Boltzmann fluid-dynamics on the QPACE supercomputer. Procedia Computer Science 1(1), 1075–1082 (2010), doi:10.1016/j.procs.2010.04.119 ICSS 2010
[12] Biferale, L., Mantovani, F., Sbragaglia, M., Scagliarini, A., Toschi, F., Tripiccione, R.: Reactive Rayleigh-Taylor systems: Front propagation and non-stationarity. EPL 94(5), 54004 (2011), doi:10.1209/0295-5075/94/54004
[13] Biferale, L., Mantovani, F., Pivanti, M., Pozzati, F., Sbragaglia, M., Scagliarini, A., Schifano, S.F., Toschi, F., Tripiccione, R.: A Multi-GPU Implementation of a D2Q37 Lattice Boltzmann Code. In:
[14] Calore, E., Schifano, S.F., Tripiccione, R.: On Portability, Performance and Scalability of an MPI OpenCL Lattice Boltzmann Code. In: Euro-Par 2014: Parallel Processing Workshops: Euro-Par 2014 International Workshops, Porto, Portugal, August 25-26, 2014, Revised Selected Papers, Part II, pp. 438–449. Lecture Notes in Computer Science, Springer International Publishing, Cham (2014), doi:10.1007/978-3-319-14313-2_37

[15] Calore, E., Schifano, S.F., Tripiccione, R.: Energy-performance tradeoffs for HPC applications on low power processors. Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics) 9523, 737–748 (2015), doi:10.1007/978-3-319-27308-2_59

[16] Calore, E., Gabbana, A., Kraus, J., Schifano, S.F., Tripiccione, R.: Performance and portability of accelerated lattice Boltzmann applications with OpenACC. Concurrency and Computation: Practice and Experience 28(12), 3485–3502 (2016), doi:10.1002/cpe.3862

[17] Calore, E., Gabbana, A., Kraus, J., Pellegrini, E., Schifano, S.F., Tripiccione, R.: Massively parallel lattice-Boltzmann codes on large GPU clusters. Parallel Computing 58, 1 – 24 (2016), doi:10.1016/j.parco.2016.08.005

[18] Mantovani, F., Pivanti, M., Schifano, S.F., Tripiccione, R.: Performance issues on many-core processors: A D2Q37 Lattice Boltzmann scheme as a test-case. Computers & Fluids 88, 743 – 752 (2013), doi:10.1016/j.compfluid.2013.05.014

[19] Crimi, G., Mantovani, F., Pivanti, M., Schifano, S.F., Tripiccione, R.: Early Experience on Porting and Running a Lattice Boltzmann Code on the Xeon-phi Co-Processor. Procedia Computer Science 18, 551–560 (2013), doi:10.1016/j.procs.2013.05.219

[20] Calore, E., Demo, N., Schifano, S.F., Tripiccione, R.: Experience on Vectorizing Lattice Boltzmann Kernels for Multi- and Many-Core Architectures. In: Parallel Processing and Applied Mathematics: 11th International Conference, PPAM 2015, Krakow, Poland, September 6-9, 2015. Revised Selected Papers, Part I, pp. 53–62. Lecture Notes in Computer Science, Springer International Publishing, Cham (2016), doi:10.1007/978-3-319-32149-3_6

[21] McCalpin, J.D.: Memory bandwidth and machine balance in current high performance computers. IEEE Computer Society Technical Committee on Computer Architecture (TCCA) Newsletter pp. 19–25 (Dec 1995)

[22] Colfax: Clustering modes in Knights Landing processors (2016), https://colfaxresearch.com/knl-numa/

[23] Colfax: MCDRAM as high-bandwidth memory (HBM) in Knights Landing processors: Developers guide (2016), https://colfaxresearch.com/knl-mcdram/

[24] Sodani, A., Gramunt, R., Corbal, J., Kim, H.S., Vinod, K., Chinthamani, S., Hutsell, S., Agarwal, R., Liu, Y.C.: Knights landing: Second-generation intel xeon phi product. IEEE Micro 36(2), 34–46 (Mar 2016), doi:10.1109/MM.2016.25

[25] Dongarra, J., London, K., Moore, S., Mucci, P., Terpstra, D.: Using PAPI for hardware performance monitoring on linux systems. In: Conference on Linux Clusters: The HPC Revolution. vol. 5. Linux Clusters Institute (2001)

[26] Weaver, V., Johnson, M., Kasichayanula, K., Ralph, J., Luszczek, P., Terpstra, D., Moore, S.: Measuring energy and power with PAPI. In: Parallel Processing Workshops (ICPPW), 2012 41st International Conference on. pp. 262–268 (2012), doi:10.1109/ICPPW.2012.39

[27] Hackenberg, D., Schone, R., Ische, T., Molka, D., Schuchart, J., Geyer, R.: An Energy Efficiency Feature Survey of the Intel Haswell Processor. In: Parallel and Distributed Processing Symposium Workshop (IPDPSW), 2015 IEEE International. pp. 896–904 (May 2015), doi:10.1109/IPDPSW.2015.70

[28] Desrochers, S., Paradis, C., Weaver, V.M.: A validation of dram rapl power measurements. In: Proceedings of the Second International Symposium on Memory Systems. pp. 455–470. MEMSYS ’16 (2016), doi:10.1145/2989081.2989088

[29] Calore, E., Gabbana, A., Schifano, S.F., Tripiccione, R.: Evaluation of DVFS techniques on modern HPC processors and accelerators for energy-aware applications. Concurrency Computation: Practice and Experience (2017), doi:10.1002/cpe.4143

[30] https://baltig.infn.it/COKA/PAPI-power-reader
[31] Calore, E., Gabbana, A., Schifano, S.F., Tripiccione, R.: Optimization of lattice Boltzmann simulations on heterogeneous computers. The International Journal of High Performance Computing Applications pp. 1–16 (2017), doi: 10.1177/1094342017703771