Classical Simulation of Intermediate-Size Quantum Circuits

Jianxin Chen,1,* Fang Zhang,2,3,† Cupjin Huang,2,3 Michael Newman,2,4 and Yaoyun Shi2

1Aliyun Quantum Laboratory, Alibaba Group, Hangzhou, Zhejiang 311121, China
2Aliyun Quantum Laboratory, Alibaba Group, Bellevue, WA 98004, USA
3Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109, USA
4Department of Mathematics, University of Michigan, Ann Arbor, MI 48109, USA

(Dated: May 8, 2018)

We introduce a distributed classical simulation algorithm for general quantum circuits, and present numerical results for calculating the output probabilities of universal random circuits. We find that we can simulate more qubits to greater depth than previously reported using the cluster supported by the Data Infrastructure and Search Technology Division of the Alibaba Group. For example, computing a single amplitude of an $8 \times 8$ qubit circuit with depth 40 was previously beyond the reach of supercomputers. Our algorithm can compute this within 2 minutes using a small portion ($\approx 14\%$ of the nodes) of the cluster.

Furthermore, by successfully simulating quantum supremacy circuits of size $9 \times 9 \times 40$, $10 \times 10 \times 35$, $11 \times 11 \times 31$, and $12 \times 12 \times 27$, we give evidence that noisy random circuits with realistic physical parameters may be simulated classically. This suggests that either harder circuits or error-correction may be vital for achieving quantum supremacy from random circuit sampling.

PACS numbers: 03.65.Ud

I. INTRODUCTION

Classically simulating quantum systems is a relatively old problem [1]. However, only recently have nascent quantum computers become competitive in simulating general quantum circuits. Recent announcements of larger systems with reasonable target fidelities [2, 3] are pushing the boundary of what classical simulations can handle. With this push, a variety of techniques have been invented in order to keep up with newer quantum processors [4–11]. Unfortunately, this race is one that us classical beings cannot win in the long-term, but there are many good reasons to try.

Practically speaking, as we broach the boundary of the unsimulable, it is important to verify that our quantum computers are behaving as predicted. Classical simulations in the regime of NISQ [12] computers may prove invaluable as an experimental testbed for characterizations of noise, for the development of quantum error correction, and for the verification of quantum systems. Furthermore, classifying the boundary beyond which our quantum computers are doing something genuinely unattainable classically is of fundamental interest. This landmark, termed quantum supremacy [13], represents the point beyond which we must trust the theory of quantum mechanics rather than our limited simulation of it. It is then important to both our capacity for testing our quantum processors, as well as our pride as classical beings, to push this boundary as far as possible. Only then will quantum supremacy be meaningful.

Towards this goal, increasing attention has been devoted to general quantum simulation. Already, there are more than 100 classical simulators for various types of quantum systems available [24]. Several different types of simulators [4–10] have produced a wide range of results in different contexts. More specifically, for a quantum circuit with $N$ qubits and depth $d$, there are two major amplitude-wise simulation approaches. The first approach stores the entire state vector in memory, while the second calculates the amplitude $\alpha_x$ for any $N$-bit string $x \in \{0, 1\}^N$.

It is not surprising that for the first approach, memory is a major issue. In this context, the largest quantum system that could be classically simulated one decade ago was a 42-qubit one on the Jülich supercomputer by the Massively Parallel Quantum Computer Simulator [4]. In [6], Intel’s qHiPSTER was used more specifically to simulate quantum supremacy circuits of up to 42 qubits [13]. In 2017, quantum supremacy circuits of 45 qubits were simulated on the Cori II supercomputing system using 0.5 petabytes of memory and 8,192 nodes [5]. Finally, in 2018, quantum

*Electronic address: liangjian.cjx@alibaba-inc.com
†Electronic address: fang.z@alibaba-inc.com
supremacy circuits operating on $7 \times 7$ grids of depth 39 were simulated on the Sunway TaihuLight supercomputer [10].

In this work, we focus on computing a single amplitude, which may be far less restrictive on our memory requirements. Towards this end, we consider an algorithm introduced by Markov and Shi [14] for tensor network contraction as a template for simulating quantum circuits. This technique is among the very few that are capable of simulating circuits operating on more than 50 qubits to a reasonable depth. By combining this technique with the Feynman path integral, [8] introduced the undirected graphical model to evaluate circuits with diagonal operators more efficiently. Their work succeeded in simulating $5 \times 9$ qubits to depth 40 and $7 \times 8$ circuits to depth 30 on a single workstation.

Ultimately, this is a numbers game, and so we coarsely summarize existing simulation parameters in Table I. A more detailed presentation of our simulation parameters is shown in Figure 1.

### II. OUR CONTRIBUTIONS

In this work, we introduce new techniques for quantum simulation that help us to push this barrier even further. We implement a single-amplitude simulator that computes $\langle x | C | 0 \cdots 0 \rangle$ for an arbitrary quantum circuit $C$ and we test our simulator for $C$ drawn randomly from a restricted circuit class yielding a plausibly intractable sampling problem [13].

Our simulation technique is based off of Google’s model for variable elimination in the line graph. This approach is fundamentally tensor network contraction with built-in methods for preprocessing the tensors to minimize cost. Their work was performed on a single workstation, which is useful for performing individual simulations at low-cost.

In this work, we develop heuristics within this framework that lend themselves naturally to parallelization on a cluster. We find that, with only a fraction of the power of a cluster, we can perform simulations that break new barriers in the classical simulation of quantum circuits.

Our first contribution is adapting the variable elimination algorithm to the requirements of a typical cluster. Storing the full amplitude of 50 qubits requires 16 petabytes of memory if one uses double-precision values. Furthermore, a major restriction is the required inter-node communication. Several attempts have been made to reduce this communication cost, such as global gate optimization [5] and qubit reordering [5, 10]. In particular, the Alibaba cluster has 10,000 computers, but inter-node communication is very expensive. Thus, the first approach is not suitable for our cluster.

The algorithm we developed is based on tensor network contraction [8, 14], in which treewidth will be the dominant factor in determining the time- and space-complexity. Both of these grow exponentially with the treewidth. The Alibaba cluster has $96 \times 10,000$ CPUs in total, which is just 10% of the CPUs available in the top supercomputer Sunway Taihulight [15]. However, the 256 Sunway processors share 256 gigabytes of memory, which limits each processor to a smaller amount of memory. While there are algorithms that limit memory requirements and could take advantage of the powerful Sunway CPUs, our algorithm fits the Alibaba cluster by providing a reasonable number of processors and a reasonable amount of memory for each processor.

Our second contribution is, naturally, to develop techniques that take full advantage of this parallelization. We can drastically simplify the graph to be evaluated by parallelizing over the values of key nodes. This approach balances sequential and parallel techniques to optimize the evaluation of a quantum circuit. The particular ideas that help to achieve our results are the following.
FIG. 1: The depth vs. runtime plot for our simulator acting on an $n \times n$ square of qubits. The different lines represent different $n$, and the $y$-axis is plotted on a log-scale. For reference, two hours of run-time is approximately $10^{3.86}$ seconds. Although we request 131072 nodes for some instances, when collecting the data, we run one subtask to calculate the running time. This is because the subtasks in the same circuit have the same runtime, and are performed in parallel. Each point represents the 80\% percentile runtime among 1000 randomly generated circuits. We emphasize that the largest depth for $10 \times 10$ to $12 \times 12$ grids are not the limit of our algorithm. We use QuickBB, which implements an anytime tensor network contraction algorithm, to generate the elimination ordering. We pre-specify a running time of 60 seconds, which may not be sufficient for larger depth circuits. This can be overcome by allowing QuickBB more time to perform its estimation.

1. Construct a simplified undirected graph.

2. Divide the whole task into many subtasks while keeping the running time of each subtask as short as possible. We know the running time of each subtask will be exponential in its treewidth. However, calculating treewidth is in NP-hard. The central idea is to use QuickBB’s algorithm to roughly estimate the treewidth, and then use the treewidth to estimate the running time.

   Our central observation is that we can remove the most costly nodes by parallelizing over their values. In spite of its simplicity, we observe tremendous gains using this technique for simulation on a cluster.

3. Use this estimation again to determine an efficient order of elimination for the remaining nodes in each subtask.

   We present a more detailed accounting of these techniques in Section III, and the performance of our simulator is summarized in Figure 1.

The final contribution of this work is to apply this powerful simulator in the context of quantum supremacy. In Section V, we give evidence that quantum supremacy is unachievable in the low-depth random circuit model defined in [13]. We find that this holds true even under idealized (but plausible) target gate fidelities. This re-emphasizes the integral role error-correction may play in existing quantum computation technologies.

Our paper is outlined as follows. In Section III we detail our algorithm through a simple example, and then describe it in full. Then, in Section IV, we present our testing parameters as well as the hardware and software used by the algorithm. In Section V we address limitations on showing quantum supremacy through random circuit sampling. Finally, in Section VI, we discuss some of the subtleties of our implementation, and potential future considerations.
any quantum circuit will be the dominant factor in determining the time- and space-complexity.

We briefly review the undirected graphical model in Subsection III A. We then describe the full tensor network contraction approach proposed by Markov and Shi [14], but which also takes advantage of diagonal gates. We will be the dominant factor in determining the time- and space-complexity.

Our simulator is based on the complex undirected graphical model introduced in [8]. This is essentially a variant of the tensor network contraction approach proposed by Markov and Shi [14], but which also takes advantage of diagonal gates. We evaluate using the graphical model.

III. THE ALGORITHM

In this subsection, we will review the undirected graphical model [8] which is also used in our base algorithm. For any quantum circuit $C$, the amplitude of a particular bit-string $x$, $\langle x|C|0\ldots0\rangle$, is given by

$$\langle x|C|0\ldots0\rangle = \sum_{i_1,i_2,...,i_{d-1}\in\{0,1\}^N} \langle x|C_{i_d}\ldots C_2 C_1|0\ldots0\rangle$$

where $C_1, C_2, \ldots, C_d$ are unitary matrices corresponding to clock cycles $1, 2, \ldots, d$, respectively. One may further expand the formula as

$$\langle x|C|0\ldots0\rangle = \langle x|C_d\ldots C_2 C_1|0\ldots0\rangle = \sum_{i_1,i_2,...,i_{d-1}\in\{0,1\}^N} \langle x|C_d|i_{d-1}\rangle \ldots \langle i_2|C_2|i_1\rangle \langle i_1|C_1|0\ldots0\rangle.$$ \hspace{1cm} (1)

For example, let's consider a circuit with qubit number $N = 4$ and depth $d = 8$ as described in Figure 2. Consider $C = C_8 \ldots C_2 C_1$ defined by

$$
C_1 = H_1 \otimes H_2 \otimes H_3 \otimes H_4; \quad C_5 = CZ_{2,4} \otimes I_3 \otimes \sqrt{X}_1;
C_2 = CZ_{1,2} \otimes \sqrt{X}_3 \otimes \sqrt{Y}_4; \quad C_6 = CZ_{2,3} \otimes \sqrt{Y}_1 \otimes \sqrt{Y}_4;
C_3 = T_1 \otimes T_2 \otimes CZ_{3,4}; \quad C_7 = CZ_{1,4} \otimes I_{2,3};
C_4 = CZ_{1,3} \otimes I_2 \otimes \sqrt{X}_4; \quad C_8 = H_1 \otimes H_2 \otimes H_3 \otimes H_4.
$$

Then we may expand Equation 1 as,

$$\sum_{i_1,i_2,i_3,i_4,i_5,i_6,i_7\in\{0,1\}^4} \langle x|H_2 \otimes H_3 \otimes H_4|i_7\rangle \langle i_7|CZ_{1,4} \otimes I_{2,3}|i_6\rangle
\cdot \langle i_6|CZ_{2,3} \otimes \sqrt{X}_1 \otimes \sqrt{Y}_4|i_5\rangle \langle i_5|CZ_{2,4} \otimes I_3 \otimes \sqrt{X}_1|i_4\rangle
\cdot \langle i_4|CZ_{1,3} \otimes I_2 \otimes \sqrt{X}_4|i_3\rangle \langle i_3|T_1 \otimes T_2 \otimes CZ_{3,4}|i_2\rangle
\cdot \langle i_2|CZ_{1,2} \otimes \sqrt{X}_3 \otimes \sqrt{Y}_4|i_1\rangle \langle i_1|H_1 \otimes H_2 \otimes H_3 \otimes H_4|0000\rangle.$$ \hspace{1cm} (2)

The summation in Equation 2 is carried out over the seven 4-bit strings $i_1, i_2, \ldots, i_7$. Because T and CZ are diagonal matrices, the terms in summation will appear only if $i_1 = (1,2), i_2 = i_3, i_3^{(123)} = i_4, i_4^{(234)} = i_5^{(2,3)} = i_6^{(2,3)}$.

FIG. 2: The example circuit $C$ that we evaluate using the graphical model.
and \(i_6 = i_7\). By considering the diagonal gates in this way, we have drastically reduced the total number of terms from \(2^{28}\) to \(2^{10}\).

We now formulate the above procedure in the language of undirected graphical models. Given the index sequences \((i_0 = 0 \ldots 0, i_1, i_2, \ldots, i_{d-1}, i_d = x)\) in Equation 1, we construct a graph \(G\), where each distinct variable \(i_k^{(j)}\) corresponds to a vertex, and two vertices are connected by an edge if there is an operator acting on both of them. Each term in the Feynman path integral then corresponds to a complex number associated to labelling all vertices in the graph by \(\{0, 1\}\).

Such a graph can be simplified if some tensor operators happen to be diagonal. For example, if node \(u\) and \(v\) are connected by a single-qubit diagonal gate, then one term in the Feynman path integral can only survive if the corresponding labelling we choose satisfies \(u = v\). Therefore, the two nodes \(u\) and \(v\) can be merged together.

Similarly, the tensors on the lefthand side of Figure 3 correspond to the graph gadgets on the right. Back to our example in Figure 2, let \(i_1 = abcd, i_2 = i_3 = abef, i_4 = abeg, i_5 = hbeg, i_6 = i_7 = ibej\). Then the corresponding undirected graph can be drawn as in Figure 4.

B. Our Algorithm

1. Variable elimination

Our base algorithm for evaluating the sum in Equation 1 is similar to the algorithm in [8], and proceeds by eliminating one variable at a time. This process will usually produce tensors of rank greater than 2. To eliminate the binary variable \(v = i_k^{(j)}\) from Equation 1:

1. Find the set of tensors \(T_v = \{\tau \mid v \text{ appears in } \tau\}\), and the set of variables \(V_v = \bigcup_{\tau \in T_v} \{v' \mid v' \text{ appears in } \tau\}\).
2. Multiply together all tensors $\tau \in T_v$ to obtain a new tensor $\sigma$ of rank $|V_v|$ and indexed by variables in $|V_v|$.

3. Sum $\sigma$ over the index corresponding to $v$ to obtain $\sigma'$.

4. Remove the variable $v$ and all the tensors in $T_v$ from the summation, and then add the new tensor $\sigma'$. Update the undirected graph by connecting any two neighbors of vertex $v$, and then removing $v$.

To evaluate the entire sum, repeat the above steps to eliminate all of the variables in any convenient order. When all variables are eliminated, we get a tensor of rank 0 (i.e. a complex number) which is exactly the value of the amplitude.

Steps 2 and 3 constitute the bulk of the computation. Fortunately, they can be computed on Python using the numpy package with a single call to the function numpy.einsum. This is optimized by first combining the small input tensors, and then only evaluating large tensors in the final step [25].

If eliminating a variable $v$ incurs a noticeable time cost, then usually the dominant term in that cost comes from the appearance of a high rank tensor $\sigma'$. Therefore, we estimate that the time cost of each step by the size of $\sigma'$. Given the undirected graph at that step, the size of $\sigma'$ is $2^{\deg(v)}$. The cost function of a particular contraction ordering is then the sum of the costs over all steps. We will use this estimation as a guide when simplifying the graph by fixing the values of certain variables, as we describe next.

2. Parallelization by fixing the values of variables

There is an even more straightforward method to evaluate Equation 1, which is just to split the sum into pieces. We can simply choose any variable $v$ and evaluate the summation twice, once with the value of $v$ fixed to 0 and once with the value of $v$ fixed to 1, and then combine the outcomes.

Similar to eliminating a variable, fixing the value of a variable also removes it from the summation. However, whereas eliminating a variable usually amalgamates several tensors into a higher rank tensor, fixing the value of a variable does not introduce any new tensor. This can potentially simplify the summation, as illustrated in Figure 5. In the undirected graph model, fixing the value of a variable translates to removing the corresponding vertex along with all of its edges.

![FIG. 5: Illustration of parallelizing by fixing the value of a node. The initial undirected graphical model is shown in the leftmost figure. Fixing the value of node $c$ does not help simplify the graph much, and is displayed in the middle figure. Instead fixing the value of node $e$ simplifies the graph significantly, and is shown in the rightmost figure.](image-url)

On the other hand, evaluating an undirected graph using only this strategy would be highly inefficient compared to our base algorithm. This is because each time we remove a vertex in this manner, we need to recursively evaluate the resulting graph twice. The number of evaluations blows up exponentially in the number of vertices we remove this way.

The advantage of this strategy is that all of these evaluations can be done in parallel. Our overall strategy is to remove $t$ vertices this way, essentially dividing the graph evaluation task into $2^t$ subtasks, and then perform each subtask
using the base algorithm. Of course, this is only effective if the cost of evaluating the resulting graph is substantially lower than the cost of evaluating the original graph.

Removing different vertices may have wildly different effects on the cost of the base algorithm. Intuitively, removing high-degree vertices should simplify the graph further, but even a low-degree vertex can be a “key vertex” that holds large parts of the graph together. In order to choose which vertices to remove, we use a greedy strategy based on the estimated time cost of the base algorithm.

Finally, since our goal is only to compute the value of \( \langle x | C | 0 \ldots 0 \rangle \), the final values of all qubits are fixed to \( x \), and so all corresponding vertices can be removed for free \([26]\). Fortunately, for the circuits we consider, we find that this optimization simplifies the initial graph considerably.

3. The variable elimination ordering

Similar to \([8]\), the variable elimination ordering can heavily affect the time-complexity of our base algorithm (See Fig. 6 for an example). Additionally, it can also affect the choice of vertices we remove before applying our base algorithm, as this choice is based on the estimated time cost to evaluate the graph.

In \([8]\), all of the TensorFlow experiments use the “vertical ordering”, eliminating variables corresponding to each qubit in temporal order before moving on to the next qubit. In the same paper, the heuristic algorithm QuickBB \([16]\) is also used to find a better elimination ordering (and a better upper bound for the treewidth). We observe that QuickBB usually finds an ordering that improves both the maximum tensor rank \( R \) and the estimated time cost. Furthermore, initially using QuickBB makes the greedy vertex removal more efficient in reducing the time cost.

However, QuickBB itself is slow enough that we cannot afford to run it whenever we would like to estimate the time cost. To compromise, we run QuickBB once initially for each circuit to obtain an elimination ordering, and then use that ordering throughout to remove vertices. We then run QuickBB a second time after vertex removal to obtain a new elimination ordering that will evaluate the graph efficiently.

In our experiments, we use an off-the-shelf QuickBB implementation by \([16]\). We specified the command line options \(--\text{min-fill-ordering} \--\text{time 60} \) to run QuickBB for 60 seconds both before and after the greedy vertex removal.

![Variable Elimination Diagrams](image)

FIG. 6: Illustration of variable elimination. The initial undirected graphical model is displayed in the leftmost figure. Eliminating node \( c \) in the reduces the number of tensors, as displayed in the middle figure. However, eliminating node \( e \) introduces a tensor of rank 4, as shown in the rightmost figure.

IV. NUMERICAL RESULTS

Although our algorithm can be applied to any quantum circuit, we will use the circuit family proposed for quantum supremacy in \([13]\) as test cases. These circuits were chosen through numerical optimizations to minimize the convergence time to the Porter-Thomas distribution. For the sake of completeness, we next recall the rules used to construct these quantum supremacy circuits.
(Rule 1) Begin with a cycle of all Hadamard gates.

(Rule 2) Place CZ gates alternating between the 8 configurations shown in Figure 7.

(Rule 3) Place single-qubit gates chosen at random from the set \(\{\sqrt{X}, \sqrt{Y}, T\}\) at the remaining positions, conditioned on the following restrictions.

(3.A) Place a gate at a qubit only if that qubit is occupied by a CZ gate in the previous cycle.

(3.B) Place a T-gate at a qubit if there are no single-qubit gates in the previous cycles at that location, except for the initial cycle of Hadamard gates.

\[
\begin{array}{cccccccc}
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\end{array}
\]

(a) Configuration 1 (b) Configuration 2 (c) Configuration 3 (d) Configuration 4

\[
\begin{array}{cccccccc}
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\end{array}
\]

(e) Configuration 5 (f) Configuration 6 (g) Configuration 7 (h) Configuration 8

FIG. 7: Layouts of CZ gates in the 8 configurations producing supremacy circuits operating on an \(8 \times 7\) lattice of 56 qubits [13].

We ran our tests on a small portion of the cluster provided by the Data Infrastructure and Search Technology Division of the Alibaba Group. It consists of 10,000 machines, each with 96 Intel Skylake Xeon Platinum 8163 vCPUs @ 2.5 GHz and with 512 GB of memory. We requested 131072 nodes via Docker containers and 8 GB of memory for each node. We divided the circuit simulation task into \(131072 = 2^{17}\) subtasks as described in Subsection III B. If the circuit is not that large, or more specifically, if the undirected graph has treewidth less than 28, then each node has sufficient memory for the subtask. For larger circuits, if these subtasks require more than 8 GB of memory, we further divide each subtask into sub-subtasks until the memory requirement can be met by each node. In this case, we run multiple sub-subtasks sequentially on each node and count the total running time of these sequential sub-subtasks on each node.

We generate 1000 random circuits operating on \(n \times n\) lattices of depth \(d\) according to the rules described above. We test each circuit on the 131072-node cluster and calculate the running time if it succeeds. If it succeeds for 80% of these circuits, we count the 80% percentile running time for these instances, and claim that a typical circuit of size \(n \times n \times d\) can be classically simulated within that time on our cluster [17]. We use double precision since Python’s built-in float and complex types have double precision.
FIG. 8: The runtime versus success probability plot for our simulator acting on a 10 × 10 grid of depths 34 and 35. Lines with different colors represent different numbers of subtasks that we divide our simulation task into. Regular lines and dashed lines represent depths 34 and 35, respectively. More subtasks always help to increase the success probability, until we reach the limit of our processors. After that, in order to improve the success probability, we have to tolerate a longer running time.

V. APPLICATION TO RANDOM CIRCUIT SAMPLING

We next apply our simulator in the context of quantum supremacy from random circuit sampling. We argue that, even for idealized gate fidelities on superconducting circuits, any circuit with a reasonable output fidelity may be simulated classically.

We study circuit fidelity by using the digital error model where each quantum gate is followed by an error channel [18]. The circuit fidelity for this model can be coarsely estimated as

$$
\alpha \approx \exp\left(-\epsilon_1 \times g_1 - \epsilon_2 \times g_2 - \epsilon_{\text{init}} \times N - \epsilon_{\text{mes}} \times N\right)
$$

where $\epsilon_1, \epsilon_2 \ll 1$ are the Pauli error rates for single- and two-qubit gates, $\epsilon_{\text{init}}, \epsilon_{\text{mes}} \ll 1$ are the initialization and measurement error rates, $g_1, g_2$ are number of single- and two-qubit gates in the circuit, and $N$ is the number of qubits. In [13], the same technique was adopted to estimate the largest depth of circuits with 7 × 7 qubits that can be demonstrated in state-of-art superconducting quantum computers.

For simplicity, we make the physically-motivated assumption that $\epsilon_2 = \epsilon_{\text{init}} = \epsilon_{\text{mes}} = \epsilon$ and $\epsilon_1 = \frac{\epsilon}{10}$. For an $m \times n \times d$ circuit, the number of two-qubit gates in the configurations specified by Figure 7 can be estimated as

$$
g_2 \approx \frac{d}{8} \left((m - 1)n + m(n - 1)\right),
$$

and this is precise whenever $d | 8$. Furthermore, we can approximate

$$
g_1 \approx \frac{d}{8} \left(3mn - (m + n + 1)\right) - \frac{1}{4}mn
$$

when our circuit is drawn from that same family defined in [13]. Then, assuming $m \approx n$ and taking into account the initial application of Hadamard gates along with the first layer, we can approximate

$$
\alpha \approx \exp\left(-\left[\frac{d}{4} \left(N - \sqrt{N}\right) + 2N + \frac{d}{80} \left(3N - 2\sqrt{N} - 1\right) + \frac{3}{40}N\right] \epsilon\right).
$$

State-of-the-art superconducting technology is expected to achieve two-qubit gate fidelities of at most 99.5% [2, 19],
corresponding to $\epsilon = 0.005$. We plot our simulator bounds, given less than two hours of runtime, superimposed on the two-qubit gate fidelity graph required for a 5% circuit fidelity. We observe that we are well above the supremacy threshold for a 99.5% two-qubit gate fidelity, drawn as a red dashed line. These results are summarized in Figure 9.

We re-emphasize that we are reporting runtimes for single-amplitude simulation. In order to generate a full distribution, significant overhead may be required in generating many amplitudes and sufficient trials. However, these runtimes give evidence that, subject to tolerating this overhead, quantum supremacy will be difficult to achieve within this particular framework. Generating a large slice of amplitudes, similar to [7], would be an interesting future direction that could provide more robustness to this simulation model.

VI. DISCUSSION

In summary, we have described a cluster-based algorithm for quantum circuit simulation. By appropriately choosing vertices to eliminate in the undirected graphical model, we can reduce the treewidth significantly compared to selecting vertices at random. By running our algorithm on the cluster provided by the Data Infrastructure and Search Technology Division of the Alibaba Group, we simulated quantum supremacy circuits of size $6 \times 6 \times 68, 7 \times 7 \times 53, 8 \times 8 \times 44, 9 \times 9 \times 40, 10 \times 10 \times 35, 11 \times 11 \times 31, \text{ and } 12 \times 12 \times 27$. We did this using 131072 processors and 1 petabyte
of memory. Finally, we gave evidence that noisy random circuits for realistic physical parameters and circuit fidelities may be simulated classically. This suggests that new approaches or even error-correction may be necessary in demonstrating quantum supremacy [13, 20]. Fortunately, towards this end, there are already alternative proposals [21–23].

In terms of the further improving the algorithm, we plan to explore an alternative to the greedy algorithm used to optimize the vertex elimination ordering. We observe that the vertices chosen for elimination via the greedy algorithm are always connected by at least two edges corresponding to CZ gates. Although this partially explains why it is more efficient than simply eliminating a random vertex (since by this choice, two rank-2 tensors will be replaced by a single rank-2 tensor as \( CZ_{12} \times CZ_{13} = |0\rangle\langle 0| \otimes I_{23} + |1\rangle\langle 1| \otimes Z_2 Z_3 \)), it is worth further exploring this choice. More generally, one could also consider an algorithm that is optimized for a particular restricted circuit class.

We should also mention that there are several limitations to our current implementation, which may be improved in future work.

1. The numpy package cannot handle too many subscripts within the einsum function, which is due to NPY_MAXDIMS, the maximum number of dimensions allowed in arrays. This is defined as 32 in numpy.

2. If we need to divide the circuit simulation task into many more subtasks than the number of processes we have access to, our naive algorithm will run many of these subtasks sequentially on each processor. This reduces the gains obtained through parallelization.

3. For larger circuits, it is very slow to use QuickBB to generate a good elimination ordering. This is not surprising; choosing an optimal ordering is an NP-hard problem. However, it is worth exploring other avenues towards generating good orderings according to our cost function. Currently, we only use QuickBB twice. When running QuickBB in between the removal of each vertex, we can simulate much larger circuits (e.g. of size \( 7 \times 7 \times 60 \)), but with an appreciably longer running time. Potentially, if we could find a faster algorithm, then we could run that algorithm between the removal of vertices. This may further simplify the subtasks at low cost.

One final consideration is our measure for characterizing the quality of our quantum devices. Both here and in [13], we consider the circuit fidelity as a good measure of this quality. However, there may be circuits with poor fidelity, but which still display quantum power with respect to a different metric.

We hope that the increasing power of classical simulators pushes quantum processors to realize their near-term physical limits. In the race to simulate quantum systems, we expect that our classical simulators will ultimately lose; this loss will be a demonstration of the intrinsic potential of quantum processing.

Acknowledgements

J. C. and F. Z. contributed equally to this project. J. C. would like to thank Mingcheng Chen for discussing an alternative approach to circuit simulation and the boundary of state-of-the-art superconducting hardware. He also thanks Mario Szegedy and Hua Xu for helpful conversations. We thank our colleagues at Alibaba: Xiaowei Jiang, Xiaojun Jin, Guodong Yang, Min Zhang, Chi Zhang and Liang Ye for support with the computing facilities. Finally, the authors thank Sergio Boixo, Igor Markov, and Mingsheng Ying for their valuable comments on an earlier draft of the paper.

---

[1] R. P. Feynman, International Journal of Theoretical Physics 21, 467 (1982).
[2] J. Kelly, R. Barends, A. Fowler, A. Megrant, E. Jeffrey, T. White, D. Sank, J. Mutus, B. Campbell, Y. Chen, et al., Nature 519, 66 (2015).
[3] C. Song, K. Xu, W. Liu, C.-P. Yang, S.-B. Zheng, H. Deng, Q. Xie, K. Huang, Q. Guo, L. Zhang, et al., Physical Review Letters 119, 180511 (2017).
[4] K. De Raedt, K. Michielsen, H. De Raedt, B. Trieu, G. Arnold, M. Richter, T. Lippert, H. Watanabe, and N. Ito, Computer Physics Communications 176, 121 (2007), quant-ph/0608239.
[5] T. Häner and D. S. Steiger, in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis (ACM, 2017) p. 33.
[6] M. Smelyanskiy, N. P. D. Sawaya, and A. Aspuru-Guzik, ArXiv e-prints (2016), arXiv:1601.07195 [quant-ph].
[7] E. Pednault, J. A. Gunnels, G. Nannicini, L. Horesh, T. Magerlein, E. Solomonik, and R. Wisnieff, ArXiv e-prints (2017), arXiv:1710.05867 [quant-ph].
[8] S. Boixo, S. V. Isakov, V. N. Smelyanskiy, and H. Neven, ArXiv e-prints (2017), arXiv:1712.05384 [quant-ph].
