Next generation low temperature polycrystalline materials for above IC electronics. High mobility n- and p-type III–V metalorganic vapour phase epitaxy thin films on amorphous substrates

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Abstract

We report on the growth and electronic properties of polycrystalline III–V semiconductors, which to date have not been discussed in depth in the literature. III–V polycrystalline semiconductor thin films were grown by metalorganic vapour phase epitaxy in the temperature range 410 °C–475 °C, which is compatible for integration into the Back-End-Of-Line (BEOL) silicon based integrated circuits. The thickness of the films in this study is in the range of tens to a few hundreds of nanometers, and deposited on amorphous substrates (either smart-phone-grade glass or Si/SiO2) and, also, on oxidised GaAs epi-ready wafers. Extensive AFM, SEM and TEM analyses show interlinked-to-continuous polycrystalline III–V films based on In(Al)As or GaSb. Hall-van der Pauw measurements return results of high mobility and controllable charge density for n- and p-type field effect transistors. In the GaAs/In(Al)As system, electron density ranging from $1 \times 10^{16}$ to $1 \times 10^{19}$ cm$^{-3}$ $(n)$ was achieved, with room temperature mobility values in the range of 100–150 cm$^2$ V$^{-1}$ s$^{-1}$ and hole mobility values in the range of 1–10 cm$^2$ V$^{-1}$ s$^{-1}$ have been measured in Zn doped samples. Polycrystalline GaSb films demonstrated p-type behaviour ($1 \times 10^{12}$ cm$^{-3}$) with remarkably high room temperature hole mobility values up to 66 cm$^2$ V$^{-1}$ s$^{-1}$ for the films grown on Si/SiO2 substrate (and 300 cm$^2$ V$^{-1}$ s$^{-1}$ for the GaAs substrate where an epitaxial process is actually in place). Materials could be stacked into heterostructures, providing a promising platform for complex devices enabling compatible n- and p-type hetero-layers for 3D integration formed at temperatures ≤80 °C.

1. Introduction

As conventional silicon based field effect transistors approach the limit of dimensional scaling, the hardware underpinning information and communication technologies is exploring new integration strategies, which depart from conventional dimensional scaling. Future high performance Integrated Circuits (ICs) would benefit greatly from a practical realization of heterogeneous 3D processing, where memory, logic and photonic functions are incorporated into the traditionally passive back end of line metallization [1]. This approach has the potential to deliver improvements in energy efficiency, functionalities, and performance. To realize this potential, it is required to develop processes to form semiconductor thin films at temperatures low enough for ‘above IC’ applications, which generally limits processing (on time scales from minutes to hours) to temperatures <500 °C. As dopant activation is usually at the highest temperature in a transistor process, this suggests exploring semiconductor material systems where dopant activation is generally not required.

In addition to high performance silicon integrated circuits, there is a wider variety of applications, largely referred to under the category of ‘internet of everything’, which will require the development of highly integrated systems on low temperature and flexible substrates, where a thermal budget constrain is also present. This
indicates a convergence of requirements in the field of large area/flexible electronics and integration of functionality for ‘above IC’ applications, which both need the development of semiconducting thin films for electronic and photonic devices with a constraint on the thermal budget of the deposition and any subsequent post deposition annealing conditions.

Today a number of candidates (e.g. organic polymers, semiconducting oxides, amorphous or polycrystalline silicon, III-nitrides)\([2–5]\) are actively investigated, but currently none of the options is meeting all the necessary requirements, such as: the ability to form high mobility \(n\) and \(p\)-type channels, low temperature processing, low voltage operations and substrate adaptability.

In this contribution we present a selection from a wide variety of thin polycrystalline III–V material films, which simultaneously demonstrate high mobility, both \(n\)- and \(p\)-type tunable charge density and ability to form complex heterostructures due to their overall compatibility, all delivered via low temperature, reproducible and customizable industry-friendly metalorganic vapour phase epitaxy (MOVPE) processes.

It will indeed be shown that it is possible to obtain III–V polycrystalline thin films grown by MOVPE on amorphous substrates at relatively low temperature (410–475 \(^\circ\)C), demonstrating remarkable electrical properties; i.e. showing both \(n\)- and \(p\)-type mobilities in the range 100–150 \(\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}\) and 1–10 \(\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}\), respectively, in the same material, and even higher \(p\) values (up to \(66 \text{ cm}^2\ \text{V}^{-1}\ \text{s}^{-1}\)) for other.

It will be clear from the discussion that our result add significant new insights in the field, expanding the current literature \([6–8]\) by adding extensive data on MOVPE growth of polycrystalline III–V semiconductors.

2. Experimental

The samples used in this study were grown by MOVPE at low pressure (80 millibars) in a commercial horizontal reactor with purified \(\text{N}_2\) [9], or a mixture of \(\text{N}_2\) and \(\text{H}_2\) [10], used as carrier gases. The precursors were trimethylindium (TMIn), trimethylaluminium (TMAI), trimethylgallium (TMGa), triethylgallium (TEGa), trimethylantimony (TMSb), diethylzinc (DEZn), arsine (\(\text{AsH}_3\)), phosphine (\(\text{PH}_3\)) and disilane (\(\text{Si}_2\text{H}_6\)).

Due to the multiple variables involved, some of the growth conditions were locked, to allow for identification of the influence of individual effects of specific parameters. Namely, for the majority of the samples from the arsenide family, growth temperature used was 475 \(^\circ\)C (thermocouple), \(V/III\) ratio (ratio between molecules of column V and column III elements sent to the reactor) of \(V/III\) \(=\) 370 and growth rate \(GR = 0.05 \text{ or } 0.1 \mu \text{h}^{-1}\) for GaAs; \(V/III\) \(=\) 150 and \(GR = 0.375 \mu \text{h}^{-1}\) for In(Al)As. For GaSb samples the typical growth conditions were: growth temperature 475 \(^\circ\)C (thermocouple), \(V/III\) \(=\) 2 and \(GR = 0.3 \mu \text{h}^{-1}\), \(\text{N}_2/\text{H}_2\) carrier gas mixture was with 30/70. Relevant variations from these are mentioned alongside particular samples’ descriptions later in the text.

Several substrates, as described specifically in each section of the manuscript (e.g. ‘smartphone grade’ glass, silicon oxide on silicon, GaAs ‘epi-ready’ wafers as references), were investigated, along substrate preparation methods (like HF acid etching, oxygen-plasma exposure), aiming to create the best possible starting surface on Si substrates (from now on indicated as \(\text{Si}/\text{SiO}_2\)). Different batches of \(\text{Si}/\text{SiO}_2\) were also used. In general, no significant variations in the samples’ morphologies were found when differently processed substrates of a particular kind were utilized, therefore, for simplicity, we used them ‘as received’ without additional processing steps pre-growth. However, we consistently observed a dramatic morphology difference between the depositions on GaAs, \(\text{Si}/\text{SiO}_2\) and glass substrates, confirming a specific ‘catalytic’ role of the substrate.

Morphological studies were performed with a Veeco Multimode V atomic force microscope (AFM) in tapping/non-contact mode at room temperature and in air.

Secondary-ion mass spectrometry (SIMS) measurements were performed employing a CAMECA SC Ultra instrument under ultra-high vacuum (UHV), usually of \(4 \times 10^{-10}\) mbar. Positive ions detection mode and 3D imaging were used in these experiments with moderate impact energy of 3 kV for a \(\text{Cs}^+\) primary beam scanned over 250 \(\times\) 250 \(\mu\text{m}^2\) while the analysis area was limited to 200 \(\times\) 200 \(\mu\text{m}^2\).

Cross-sectional transmission electron microscopy (XTEM) was performed to gain greater understanding of film structure. Samples were prepared on a dual beam focused ion beam (FIB, Helios Nanolab 460 and 660i) using standard high kV milling and a final low kV polish; this rendered the lamella electron transparent indicating an appropriate thickness for TEM. A platinum capping layer was used. Transmission electron microscopy (TEM, FEI Osiris and JEOL JEM-2100) was performed using bright-field and scanning TEM (STEM) imaging. During STEM, detector lengths were 220, 550, and 770 mm. The accelerating voltage was 200 kV. The energy dispersive x-ray (EDX) beam current was 1 nA, at an acquisition time of 30 min.

Scanning electron microscopy (SEM) provided useful information on morphology of the film surface. Images were obtained using an FEI Quanta 650 FEG SEM. Composition of the films was studied through EDX analysis, using Oxford Instruments X-Max EDX. This was performed while the sample was in the SEM vacuum chamber, allowing for elemental chemical analysis of the film.
Hall effect measurements were conducted using LakeShore Model 8404 AC/DC Hall effect measurement system. Samples used for measurements were \( \sim 1 \text{ cm}^2 \) and cut from the centre of the growth substrate to ensure all edges were clean, thus avoiding unwanted parasitic conduction pathways. Contacts were applied in a van der Pauw configuration. Unless otherwise stated, results presented here were obtained at room temperature.

3. Results and discussion

3.1. Growth protocol

MOVPE is a non-trivial, multistep process where substrates have a catalytic role enabling the precursors’ decomposition and subsequent material growth [11]. We emphasize this aspect here, as it is both relevant for the interpretation of what we report, and is rarely underlined in mainstream discussions of MOVPE processes. The substrate surfaces of interest in this study were expected to be amorphous (the reactor was never heated above the growth temperature of 475 \(^\circ\)C, therefore even the reference GaAs substrates were expected to preserve the original oxidised surface) and created additional challenges in obtaining uniform, interlinked polycrystalline film, especially if a quasi-universal method was required to achieve deposition on various substrates simultaneously in a single run.

In the early stages of this project we tried different recipes of direct deposition (i.e. without any special preparation pre-growth process). These essentially failed, as the nucleation was largely not uniform preventing the formation of a continuous film, or the deposition itself was inhibited.

For this reason, we moved to a more complex approach. The method of choice was a multistep deposition process, following a droplet epitaxy-inspired protocol [12, 13], where the group III precursor (normally TMGa, TEGa or TMIn) was injected into the reactor individually, and the resulting surface was then exposed to group V precursor (either AsH\(_3\) or TMSb) for a period of time (minutes) to form crystalline ‘seeds’ for further, standard epitaxial overgrowth (with group III and V precursor injected simultaneously, see figure 1).

In multi-layered heterostructures, the seeding step was sometimes repeated on top of the grown bulk poly-GaAs layer, with a relevant precursor being deposited sequentially (e.g. for InAs layers, we injected TMIIn and then subsequently exposed to AsH\(_3\)).

Some surprises immediately emerged. For example, the precursor choice for Ga containing layers turned out to be critical for the material being grown. On the substrates used in this study, and with the range of growth parameters investigated, we identified TEGa + TMSb and TMGa + AsH\(_3\) as optimum combinations to obtain GaSb and GaAs seed deposition, respectively, with very little, to none, deposition observed in other cases (see figures 2(a)–(d)). For GaSb growth, seeding was a necessary protocol not only to obtain a uniform polycrystalline layer with small grain size (as was the case for GaAs), but also a requirement for bulk deposition in itself (figures 2(e)–(f)). In figure 2 we give some examples of the variety of morphologies obtained. It should be noted, before continuing our discussion, that the surprising failure for example of TEGa + AsH\(_3\) combination for droplets deposition (on Si/SiO\(_2\)) is a strong indication that standard considerations about low temperature decomposition processes for MOVPE precursors (TEGa is universally considered to decompose at lower T than TMGa [14]) cannot be simply applied here, and more detailed insights in the complexity of catalytic process should be investigated.

Of all investigated alloys, GaAs had the most uniform coverage of the amorphous substrates, therefore in many grown heterostructures, GaAs often served not only as a nucleation layer, but also as uniformity-inducing buffer. When materials like InAs or GaSb were grown on the GaAs buffer (of 25–50 nm in thickness), the observed roughness was in general significantly lower, and the uniformity of the growth was higher compared to growth on seeding crystallites only (not shown). Deposition was however also possible without the GaAs buffer, and multiple samples grown directly were investigated and are discussed below.

During the development of the project we have made several hundreds of growths, sampling the space of growth parameters and heterostructures’ designs, with the objective of finding the conditions in which we’d be able to grow uniform thin films with high mobility and controllable charge density. The volume of that research is too extensive to be presented here in full, therefore we report only highlights and outstanding values, saving the full development pathway story for subsequent reports.
3.2. Results

3.2.1. III-As thin films

Despite the above mentioned relative ease of depositing polycrystalline GaAs layers on the amorphous substrates, Hall analysis of the films demonstrated poor electric properties, with low electron mobility ($<0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and charge density values in range of $1.3-3.9 \times 10^{16} \text{ cm}^{-3}$, even with intentional doping provided by disilane (with gas fluxes expected to deliver a charge density of $>10^{18} \text{ cm}^{-3}$ in planar epitaxy).

One of the most striking examples of the capability of the investigated materials were InAs thin films. Simple single layer deposition (nominally 25 nm of undoped InAs deposited on TMIn + AsH$_3$ droplets on glass and Si/SiO$_2$) resulted in significantly higher electron mobility (over $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and a flat temperature dependence of the mobility, typical for a 2D electron gas or a surface carrier mobility limited by surface roughness (figure 3). It should be noted that epitaxial InAs is known for creating a 2D free electron gas on planar surfaces with high charge density ($10^{12}-10^{13} \text{ cm}^{-2}$), even in the absence of any intentional n-doping or thermal annealing for activation [15]. The van der Pauw results alone cannot be fully conclusive to prove the exact nature of the electron gas, and more characterization work is needed. Here we concentrate on the deposition challenges and their outputs, while further electrical analyses will be presented elsewhere.
As anticipated, samples grown without the nucleation droplets demonstrated partially unlinked, discontinued films. Samples grown on GaAs polycrystalline buffers, deposited as described previously, showed lower roughness, an important parameter for device fabrication. The results of van der Pauw measurements were comparable in both cases and not affected by the morphological change.

TEM imaging revealed that the GaAs growth rate on amorphous substrates was close to the nominal one (see figure 4), while InAs appeared to be thinner than designed. The layer was continuous, with a clear polycrystalline structure.

The high charge density in the InAs layers was not a result of intentional doping and was showing a high intrinsic electron density \(10^{12} - 10^{13}\) cm\(^{-2}\) present in InAs surfaces, as expected. However, the charge density could be controlled by sending extra dopants during deposition or by surfactant use. PH\(_3\) assistance during growth reduced the charge density by an order of magnitude, and counter-doping with zinc successfully reduced...
the measured $n$-type charge density by up to 3 orders of magnitude (from levels around $1 \times 10^{18}$ to values in the $1 \times 10^{15}$ cm$^{-3}$ range), while preserving electron mobility in the range of 10–65 cm$^2$ V$^{-1}$ s$^{-1}$ in both cases (figure 5).

Further increase of the counter-dopant flux produced $p$-type layers, as above a $2 \times 10^{-5}$ DEZn flux (mol min$^{-1}$) in our reactor (corresponding to a Zn/III ratio of approximately 1), the carrier concentration underwent an abrupt increase in density and a switch to a $p$-type InAs(P) layer. A nominally 25 nm InAs(P):Zn sample deposited on 25 nm GaAs polycrystalline buffer shown $p$-type mobility of 6.3 cm$^2$ V$^{-1}$ s$^{-1}$ and 5.4 $\times$ 10$^{19}$ cm$^{-3}$ charge density on glass, and respective values of 10 cm$^2$ V$^{-1}$ s$^{-1}$ and 4.8 $\times$ 10$^{19}$ cm$^{-3}$ on Si/SiO$_2$. More moderate amounts of zinc precursor flux resulted in expected, and still high, but noticeably lower charge densities, however the obtained mobilities were also diminished (to 2–3 cm$^2$ V$^{-1}$ s$^{-1}$).

The Hall/van der Pauw measurements values showed some dependence on the deposited layer thickness, with thicker layers demonstrating higher mobilities, while the charge density was nearly constant above a threshold thickness allowing for uniform coverage and achieving fully continuous layers (figure 6).

Addition of gallium (effectively growing low Ga concentration polycrystalline InGaAs layers) immediately reduced the measured mobility by a factor of $\sim$20 (a reference InAs sample showing 30 cm$^2$ V$^{-1}$ s$^{-1}$ would drop to 1.3 cm$^2$ V$^{-1}$ s$^{-1}$ if small amount of gallium was incorporated).

The flexibility of those simple structures is noteworthy, as there are not many materials that can be doping-controlled in such range of charge densities, especially providing both $n$- and $p$-type charges’ types, while preserving high mobilities across the full range.

With possible applications in mind, the intrinsic mobility of the semiconductor used is not the only factor contributing to the device performance, as the microstructural quality of the layer and the device design itself have significant impact on the measured carrier mobility. Multilayer heterostructures and high mobility channels are to be considered; therefore we explored more complex architectures to further improve the materials’ performance and controllability.

![Figure 5. Hall/van der Pauw measurements of charge density and mobility values in Zn-doped InAs(P) layers as a function of increasing Zn precursor flux. Dash lines are guides for the eyes.](image-url)
The high mobility and possible 2D electron gas behaviour made InAs thin layers promising candidates for quantum well (QW) structures. We used higher bandgap material (AlInGa(P)) as a barrier, trying to exploit alleged similar electronic properties to InAs.

The design reported here comprised a polycrystalline GaAs buffer overgrown with an InAs QW sandwiched between two AlInAs(P) barriers with graded Al composition (i.e. the external ends of gradings had higher Al content) (figure 7(a)). A 3D SIMS analysis is presented on figure 7(b) as cross-sectional view—the data was reconstructed with an assumption that a substrate is almost flat and thus topography of the surface was preserved. The result confirmed the graded nature of the AllnAs layer, with variable Al and In content. The measured thickness values were in good correspondence with the nominal ones, for all layers involved (GaAs buffer, graded AlInAs and InAs QW). The estimated Al content in barriers was about 50% lower than nominal (reaching 30%, instead of 70%). (Figure 7(b))—please note the SIMS-analysed sample was grown without PH3 as a surfactant and the QW thickness was 10 nm.

An unexpected result came from the detailed analysis of the substrate/layer interface, where a gallium oxide layer (~8 nm thick) was observed. It is important information from the point of view of electrical characterization and performances of future devices, as the layer will have significant impact on their performances and measured values, especially for back gated field effect transistors. The gallium oxide layer was observed both on Si/SiO2 substrate and on glass, with comparable thickness.

PH3 was used mostly in its surfactant capability in those growths (i.e. PH3 flux was extremely low and we could not detect any phosphorous incorporation, coherently with the known preference for alloy order formation in MOVPE [16] and surface competition between arsenic and phosphorus when co-present during growth [17]; also AsH3 pyrolysis is faster than PH3 one, an effect highlighted at lower temperatures [18], however at extremely low growth temperatures the process might be more complicated [19]) as we discovered that the large scale uniformity of the samples was improved, when small amount of phosphine was used during growth.

Figure 6. Hall/van der Pauw measurements of charge density and mobility values in Zn-doped InAs(P) layers as a function of layer thickness (Zn/III ratio 0.057).
Those macroscopically uniform samples were obtained when undoped, or \( n \)-type samples were grown. However, there seemed to be an opposite effect for \( p \)-type samples—when PH\(_3\) was used alongside DEZn, morphology worsened, showing even different colour patches on the samples, indicating thickness differences and non-uniformities. Remarkably, van der Pauw results were not significantly affected by the PH\(_3\) use.

Van der Pauw measurements performed on a series of samples following the above mentioned design resulted in electron mobility values around 115 cm\(^2\) V\(^{-1}\) s\(^{-1}\) and charge density of 1.3 \( \times \) 10\(^{16}\) cm\(^{-3}\) for samples with 10 nm InAs QWs grown on glass. We could also reach up to 130 cm\(^2\) V\(^{-1}\) s\(^{-1}\) and 2 \( \times \) 10\(^{16}\) cm\(^{-3}\) mobility and charge density, respectively, on Si/SiO\(_2\) substrate in case of sample with 15 nm thick InAs QW and Zn-doped AlInAs barrier (with nominal 70% Al). (Figure 8).

Growth temperature had a significant impact on the material performance and morphology. The temperature reduction to 450 °C allowed lowering the charge density by one order of magnitude, while keeping the mobility high (figure 9). We could successfully drop the growth temperature down to 410 °C and still obtain quality material, an important aspect for low temperature processing. In \( p \)-type samples the temperature drop correlated with reduction of the RMS value by a factor of 4 from the usual \( \sim \) 10 nm for 10 \( \times \) 10 \( \mu \)m\(^2\) flattened AFM scan, to \( \sim \) 2.5 nm (figure 10).

### 3.2.2. III-Sb thin films

GaSb layers were significantly less uniform in morphology than their arsenide counterparts, and basically could only be grown effectively on Si/SiO\(_2\). While some deposition as a function of growth conditions resulted in the early stages of our work in polycrystalline growth on glass, these always resulted in high resistive layers, and we concentrated subsequently exclusively on the Si/SiO\(_2\).
The typical surface of a single layer growth on Si/SiO2 (deposited directly on a GaAs seeding layer without buffer bulk growth) was showing large individual, elongated crystallites, forming interlinked, but not fully continuous layers at nominal thickness below 100 nm. The thicker layers appeared continuous; however the large crystallites were still present on the surface (figure 11).

The large crystallites resembled nanowires and even had dome-shaped tops, indicating a ‘pulled-up’ growth mode. However, the EDX analysis did not show any segregation along the features’ shapes. Traces of As were found at the substrate interface, consistently with the GaAs seeding method used (figure 12).

All the samples analysed indicated that the non-intentionally doped GaSb thin films on Si/SiO2 were p-type, with carrier concentrations from around $2 \times 10^{16} \text{cm}^{-3}$ to $2 \times 10^{17} \text{cm}^{-3}$. The hole mobility did not show a significant increase as nominal thickness increased from 50 to 100 nm on Si/SiO2 substrate. However, when the nominal thickness increased to 250 nm, a large increase in mobility was observed. These results suggest that in the thinner films there is some degree of discontinuity, which is not present in the 250 nm film. The measured values of van der Pauw measurements are listed in table 1.

The significant roughness and apparent discontinuity of the thinner films make the measured mobilities even more surprising. Even for very thin (50 nm nominally) films, the measured mobility exceeded 20 cm$^2$ V$^{-1}$ s$^{-1}$, a very competitive value for a p-type polycrystalline semiconductor, and at 250 nm exceeds the values reported for oxides semiconductors [20, 21] and 2D materials formed at $T < 500 \, ^\circ\text{C}$ [22, 28]. It is noted that the Hall measurements were carefully analysed to ensure the p silicon under the tens of nm of SiO2 was not contributing to the measured data. In this case, the maximum voltages applied during the Hall measurement and the sheet carrier concentrations obtained confirms the measured data is from the overlying polycrystalline GaSb film.

The lowest growth temperature resulting in reasonable morphology for GaSb films was estimated to be around 450 °C, with, however, noticeably lower uniformity of the deposition.

GaAs-buffered growths were smoother, as in the previously described case of arsenide heterostructures. A possible second cascaded GaSb seeding layer was investigated, without significant impact on the surface appearance (both GaAs and GaSb seeds were tested, as well as direct deposition, resulting in similar samples’
morphologies). However, we observed a detrimental effect of exposing the already grown GaAs buffer layer to TMSb overgrowth, especially evident on reference epi-ready GaAs substrates, where the buffer GaAs layer was etched away by the Sb-precursor, leaving no deposition after the process completion. On other substrates the effect was less evident, highlighting again a critical role of the substrate choice.

Despite the improved surface appearance, the mobility for planarised samples was lowered by a factor of $\sim 2$. A 50 nm thick GaSb layer deposited on 50 nm GaAs buffer on Si/SiO$_2$ substrate shown 9.09 cm$^2$ V$^{-1}$ s$^{-1}$ ([table 2 column 2]).

Surface planarization was attempted also with the use of surfactants. DEZn is a well-known precursor for p-doping in III–V alloys, but importantly it is known to affect surface morphology of the materials grown with it, for example by reducing InP step-bunching [23]. However, as TMSb plays similar role in arsenides [24], a ‘competing’ behaviour led to suppressed deposition when high DEZn fluxes were used in unbuffered samples. Moderate amount of Zn did have a modest effect on the surface morphology. In buffered growths, the surfactant slightly roughened the surface of the heavily doped layers ([figure 13]).

Carrier concentration increased by $\sim 2$ orders of magnitude when Zn was introduced. This was expected as Zn is also a p-type dopant for GaSb. With increased carrier concentration, the GaSb hole mobility decreased. These results somehow demonstrate the ability to control the hole concentration and influence the level of surface roughness using the Zn dopant source ([table 2]).

We previously used phosphine to assist the polycrystalline growth in arsenides—and the incorporation was not expected or observed in those growths. However, in the case of GaSb, as soon as we utilized PH$_3$ in very small fluxes, the samples morphologies changed dramatically. When GaSb:P was grown, the surface appearance was strikingly different to the naked eye (yellowish, metallic layers were observed), and the more detailed morphology revealed significantly altered growth mode—the nanowire-like features were no longer present, substituted by evenly distributed polycrystalline structures ([figure 14(a)]) indicating a compositional change in the layer. When we attempted a bilayer growth, with thin GaSb:P layer deposited first, and then overgrown with

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**Figure 9.** Hall/van der Pauw measurements of charge density and mobility values of GaAs/InAs:Zn heterostructures as a function of growth temperature.
Figure 10. SEM (left column) and AFM (right column) height images of 25 nm InAs:Zn layer (Zn/III ratio = 1) deposited on 25 nm GaAs buffer, grown at (a) and (b) 410 °C, (c) and (d) 425 °C, and (e) and (f) 475 °C, showing RMS of 2.6, 3.4 and 10.1 nm, respectively. RMS calculated from $5 \times 5 \mu m^2$ flattened images.

Figure 11. SEM (a and b) and TEM (c) images of nominally 250 nm GaSb deposition of GaAs on Si/SiO$_2$.

Figure 12. EDX in STEM measurement of 150 nm thick GaSb layer deposited on GaAs seeds on Si/SiO$_2$. 
Table 1. Hall/van der Pauw measurement results for samples of various GaSb thickness deposited on GaAs seeds on Si/SiO₂ substrate.

| GaSb layer thickness | 50 nm | 150 nm | 250 nm |
|----------------------|-------|--------|--------|
| Mobility (cm² V⁻¹ s⁻¹) | 22.1  | 22.88  | 66.49  |
| Carrier type         | p     | p      | p      |
| Carrier concentration (cm⁻³) | 1.92 × 10¹⁶ | 2.17 × 10¹⁷ | 1.84 × 10¹⁷ |
| Sheet carrier concentration (cm⁻²) | 9.61 × 10¹⁰ | 3.26 × 10¹² | 4.6 × 10¹² |

Table 2. Hall/van der Pauw measurement results for samples of 50 nm thick GaSb deposited on 50 nm GaAs buffer on Si/SiO₂ substrate in respect to Zn-precursor flux.

| Zn/Ga ratio | 2.5 | 0.25 | 0.025 |
|-------------|-----|------|-------|
| Mobility (cm² V⁻¹ s⁻¹) | 9.09 | 0.7  | 4.04  | 3.88 |
| Carrier type         | p   | p    | p     |
| Carrier concentration (cm⁻³) | 1.37 × 10¹⁷ | 1.77 × 10¹⁹ | 1.89 × 10¹⁶ | 4.19 × 10¹⁷ |
| Sheet carrier concentration (cm⁻²) | 1.65 × 10¹³ | 8.87 × 10¹⁵ | 9.46 × 10¹₂ | 2.09 × 10¹² |

* Sample with Zn/Ga ratio of 2.5 was the most difficult to measure as it had significant measurement error—the result is included to indicate the observed trend.

Figure 13. SEM images of 50 nm GaSb growth on GaAs crystallites on Si/SiO₂: (a) no Zn; (b), (c) and (d) Zn assisted, with Zn/Ga ratio 2.5, 0.25 and 0.025 respectively.

Figure 14. SEM images of (a) 50 nm P-assisted GaSb growth on GaAs crystallites on Si/SiO₂; (b) 5 nm GaSb:P + 45 nm GaSb.
GaSb, two separate morphologies were evident—underlying small crystallites, related to phosphine use, and a nanowire-like growth of GaSb on top (figure 14(b)).

With future device low temperature processing in mind, we tested the possibility of dropping the growth temperature. Successful growth was obtained at 450 °C, but the sample morphology was not as uniform as with higher temperatures. Nevertheless the deposition was possible, opening future optimization routes for low temperature growth, if needed.

Samples deposited on glass showed somewhat similar morphologies in the examples measured, however the results were harder to obtain—SEM imaging was difficult, due to suspected charging, and electrical contacting was less successful in the case of van der Pauw measurements. Therefore we avoid discussing this aspect here, while the most consistent picture was obtained for the Si/SiO2 substrates.

3.2.3. Epi-ready GaAs substrate for InAs and GaSb thin films

For a number of growths a piece of an epi-ready semi-insulating substrate (GaAs) was included as a comparative growth reference. This resulted in an unexpected growth process: with layers growing largely epitaxially on GaAs substrates. This is surprising, as the typical deoxidation temperature for GaAs substrates in around 575 °C (significantly higher than the one utilized).

Indeed, despite the low temperature deposition (and the omission of the conventional high temperature deoxidation step), the TEM images show defected, but clearly epitaxial layers grown (figure 15). Despite our initial surprise, we notice that this is not unheard of in case of low temperature epitaxial growth (in molecular beam epitaxy) when the surface is exposed to metallic droplets/layers [25], so it is reasonable to infer that we observed a similar deoxidation process to the one reported in [25]. Obviously the structural and electrical results obtained on those substrates are not representative of polycrystalline thin film materials. Nevertheless, for completeness, the morphology and electrical properties are reported here.

The morphology of the GaAs-based samples was reproducibly much smoother than in the case of glass and Si/SiO2 in all investigated materials, showing mostly continuous layers, spanning from perfectly smooth in some architectures and growth conditions, to presenting 3D features and visible defects in other, nevertheless they did not look polycrystalline.

Undoped InAs grown directly on TMIn + AsH3 seeds on GaAs showed for 25 nm layers mobility of about 700 cm2 V−1 s−1 with charge density of 2 × 1018 cm−3 and 1400 cm2 V−1 s−1 with 5.5 × 1018 cm−3 when thin (5 nm) layers were deposited on a GaAs buffer. Here charge densities are inferred assuming that the current path is going through the InAs layer only, due to the band offset.

For the GaSb layers, we could obtain a p-type room temperature mobility of 299.4 cm2 V−1 s−1 and 1.27 × 1017 cm−3 charge density for an undoped 250 nm thick growth on GaAs seeds. Measurements of the
temperature dependence of the carrier concentration and mobility were also different than in the case of Si/SiO$_2$ based samples (figure 16) resembling a behaviour typical for phonon limited mobility [26].

4. Conclusions

In conclusion, this work has demonstrated the ability to grow polycrystalline films of InAs and GaSb on SiO$_2$/Si substrates by metalorganic vapour phase epitaxy (MOVPE) in the temperature ranging from 410 °C to 475 °C. While the InAs thin films, of nominal thickness from 10 to 100 nm, are polycrystalline with a surface roughness in the range 10–30 nm, the electron mobility values are in the range 40–130 cm$^2$ V$^{-1}$ s$^{-1}$. Moreover, through the use of Zn doping during the growth process the electron concentration in the InAs film can be controlled over the range $1 \times 10^{16}$ cm$^{-3}$ to $1 \times 10^{19}$ cm$^{-3}$. Further increases in the flux of Zn dopant converts the InAs film to a $p$-type semiconductor, with hole mobility values in the range (0.7–10 cm$^2$ V$^{-1}$ s$^{-1}$). A reduction in growth temperature to 410 °C achieved electron mobility values of $\sim$100 cm$^2$ V$^{-1}$ s$^{-1}$ with a reduced surface roughness of 2.5 nm.

In the case of GaSb films grown on SiO$_2$/Si substrates at 475 °C, with a nominal thickness ranging from 50 to 250 nm, the films are $p$-type with hole mobility values ranging from 22 cm$^2$ V$^{-1}$ s$^{-1}$ (50 nm GaSb) to 66 cm$^2$ V$^{-1}$ s$^{-1}$ (250 nm GaSb) and hole concentrations in the range $2 \times 10^{16}$–$2 \times 10^{17}$ cm$^{-3}$. These values of hole mobility exceed those reported for oxides semiconductors and 2D materials formed at $T < 500$ °C on insulating substrates. The surface of the GaSb film appears smoother when deposited on a GaAs buffer, with a reduction of the hole mobility to 10 cm$^2$ V$^{-1}$ s$^{-1}$. The next step in the development of the poly III–V materials for technology applications is the reduction in surface roughness and the fabrication of full MOSFET structures to examine important factors such as: the $I_{on}/I_{off}$ ratio, the field effect mobility and the inverse sub-threshold slope.

This work is of technological relevance to the development of semiconductor processes on substrates with a restricted thermal budget which, in principle, is relevant to both electronic and photonic devices. This could include display technology, the development of electronics (even possibly on flexible substrates, for the growth in the lower temperature range) and the incorporation of logic, memory and photonic elements in the traditionally passive back end of line of integrated circuits. There have been promising results reported in recent years using semiconducting oxides such as SnO$_2$, InGaZnO and ITO [20, 21, 27]. While these results are promising in terms of $n$-type semiconductors, there are limited results to date for high hole mobility channels.
with semiconducting oxides. A complimentary $p$-type semiconductor is required for CMOS logic. This work has demonstrated a route to high ($>50 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) electron and hole mobility using polycrystalline InAs and GaSb films deposited on amorphous SiO$_2$ at temperatures below 480 °C, which is within the thermal budget limit for the back-end-of-line of silicon integrated circuits and also opens up possibilities in displays technology.

While this work has focused on the transport properties of polycrystalline III–V materials, it is noted that the research also has relevance to optical devices through the formation of driving circuitry for the monolithic integration of photonic devices above silicon integrated circuits. More work is ongoing to trial their optical responses, and while a significant effort is necessary to optimise the III–V material properties to achieve reasonable optical emission efficiencies, there is potential for technological impact for both electronic and photonic integration above CMOS circuits.

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