Multi-relational Instruction Association Graph
for Cross-architecture Binary Similarity Comparison

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**Abstract.** Cross-architecture binary similarity comparison is essential in many security applications. Recently, researchers have proposed learning-based approaches to improve comparison performance. They adopted a paradigm of instruction pre-training, individual binary encoding, and distance-based similarity comparison. However, instruction embeddings pre-trained on external code corpus are not universal in diverse real-world applications. And separately encoding cross-architecture binaries will accumulate the semantic gap of instruction sets, limiting the comparison accuracy. This paper proposes a novel cross-architecture binary similarity comparison approach with multi-relational instruction association graph. We associate mono-architecture instruction tokens with context relevance and cross-architecture tokens with potential semantic correlations from different perspectives. Then we exploit the relational graph convolutional network (R-GCN) to perform type-specific graph information propagation. Our approach can bridge the gap in the cross-architecture instruction representation spaces while avoiding the external pre-training workload. We conduct extensive experiments on basic block-level and function-level datasets to prove the superiority of our approach. Furthermore, evaluations on a large-scale real-world IoT malware reuse function collection show that our approach is valuable for identifying malware propagated on IoT devices of various architectures.

**Keywords:** Cross-architecture binary similarity comparison · IoT malware defense · Instruction association graph · Relational graph convolutional network.

1 Introduction

Cross-architecture binary similarity comparison task aims at measuring the functional semantic similarity of binary snippets compiled from different CPU architectures. It is of great significance in many systems security applications, such
as vulnerability detection, patch analysis, and malware detection. In this paper, we explore its application in malware defense of the Internet of Things (IoT) environments. IoT devices have been widely used in various real-life scenarios in recent years. However, the security protection of many IoT devices is not yet perfect, leaving hidden dangers such as weak authentication services and security vulnerabilities, which have attracted the attention of malware developers. Many attackers use malware as a weapon to invade vulnerable devices to build large-scale IoT botnets and operate them to launch Distributed Denial of Service (DDoS) attacks, causing severe damage [1,5,16].

Due to the diversity of underlying hardware architectures of IoT devices, malware developers often reuse source code to generate malware binaries of multiple architectures, thereby infecting more devices and expanding the scale of attacks. Cozzì et al. [6] conducted empirical analysis on over 93k IoT malware emerged between 2015 and 2018, and results have shown that the samples involve more than a dozen kinds of architectures, with ARM and MIPS in the majority. They also found the prevalence of code reuse across malware samples of different families and architectures. Wang et al. [44] deployed IoT honeypots in real-world network environments and captured a large number of wild IoT malware samples. After code-level analysis, they confirmed that many samples with the same code origin are reused and propagated on IoT devices of different architectures. Therefore, an effective cross-architecture binary code similarity comparison approach can help discover reused IoT malware fragments under different architectures, providing solutions for defending against IoT attacks.

Traditional binary similarity comparison approaches are categorized into two main technical routes, static analysis-based approaches and dynamic analysis-based approaches. The former compares the syntactic or statistical features of disassembly instruction sequences [17,21,34], or design hash algorithms to calculate the similarity of binary fragments [11,37,47]. However, since different architectures have separate instruction sets, the mnemonics, registers, and memory access strategies are different, making it difficult to achieve decent performance. Dynamic-based approaches compare the runtime state information [20] or the input-output pairs of binary code fragments to measure their semantic similarity [7,32]. But it is challenging to perform scalable analysis on large-scale binary collections. Meanwhile, supporting diverse architectures and compilation settings will lead to extra workload for dynamic analysis environment configuration.

Considering the above disadvantages, researchers have recently shifted their focus to learning-based approaches. They generally adopted the following working paradigm: (i) Generate the initial representations of disassembly instructions by manually-designed features or external pre-training mechanism. (ii) Exploit deep neural encoders to individually extract vectorized representations of each binary snippet. (iii) Calculate the similarity score based on the distance metrics. Specifically, Gemini [46] extracted statistical vectors of basic blocks within the control-flow-graph of binary function pairs, then encoded the overall graph with the structure2vec network and measured their cosine similarity. INNEREYE [50] used word2vec to learn the assembly instructions embeddings (numerical
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vectors) on external code corpus, then deployed RNN encoders to separately generate sequential features of instruction sequences, and evaluated the similarity of cross-architecture binary snippets based on the \textit{Manhattan} distance. \cite{SAFE} set up similar instruction representation and sequence encoding modules, with additional self-attention layers to automatically assign high weights to important instructions, improving the semantic similarity matching performance. Although showing promising results, these approaches have two main dilemmas:

- First, these approaches individually encode binaries of different architectures and then perform similarity comparisons on their vectorized representations. However, the semantic representation spaces of the cross-architecture instruction sets have a clear gap. The separate binary characteristics encoding mechanism will accumulate this gap, resulting in inaccurate comparison results. This phenomenon will be more pronounced for larger binary snippets.
- Second, although state-of-the-arts have proved that pre-trained instruction representations perform better than statistical features \cite{50,40,48}, it relies on high-quality, large-scale external code corpora. Considering real-world binaries are generated under diverse architectures and compilation settings, especially for IoT environments, collecting a comprehensive corpus for instruction pre-training generally takes considerable time and effort.

In this paper, we design a novel cross-architecture binary similarity comparison approach with \textit{multi-relational instruction association graph}, which can effectively alleviate these two deficiencies. For a pair of binary snippets, we first associate mono-architecture opcode and operand token pairs with the operational relationship or co-occurrence-based relevance. Then we associate the cross-architecture token pairs with multi-perspective potential semantic correlations, including prefix-match, value-match, type-match and heuristic position alignment dependencies. The mono-architecture associations can effectively enhance the functional semantic representation of instructions without external instruction pre-training. The cross-architecture associations can effectively bridge the gap in the semantic feature spaces of instructions under different architectures, and significantly improve the cross-architecture binary similarity matching performance. We apply the relational graph convolutional network (R-GCN) to propagate information on the constructed multi-relational instruction association graph. R-GCN groups different types of relations and uses a separate neighbor message-passing mechanism, which can effectively aggregate multi-type associations and iteratively refine the semantic representations of instruction tokens.

Our major contributions can be summarized as follows:

- We creatively design a novel cross-architecture similarity binary comparison approach with multi-relational instruction association graph. It can associate the semantic dependencies of instructions from different perspectives, bridge the gap in the representation spaces of cross-architecture instructions, and significantly improve binary comparison performance.
- We implement our solution as an end-to-end cross-architecture binary similarity comparison system and conduct extensive evaluations at two granulari-
ties, basic block-level and function-level. Results show that our approach significantly outperforms the existing learning-based approaches (AUC=0.9924 for basic block-level and Precision@1 = 0.9216 for function-level).

- We further evaluate our approach on a large-scale cross-architecture reuse function dataset (460,386 pairs) constructed from IoT malware in real-world environments. Promising results prove that our method is valuable for defending against malware spread on IoT devices of different architectures.

2 Overview

2.1 Problem Statement

In this section, we give a formal definition of the cross-architecture binary code similarity comparison problem. The input is a pair of binary code snippets compiled on two different CPU architectures, and the output is a semantic similarity score. We set the output value in the range of 0 to 1, where 1 represents that the input binary snippets are compiled from the exact same source code, and 0 means that their source code implements completely different functions.

2.2 System Workflow

Our approach is implemented as an end-to-end cross-architecture binary code similarity comparison system. Figure 1 shows the overall system workflow, including four major modules:

- Instruction representation module (Module 1): We disassemble and preprocess the input binary snippets, obtaining the initial instruction token representations with token-level and character-level (char-level) features.
- Instruction sequence encoding module (Module 2): We use Bi-LSTM as the backbone encoder to extract the sequential representations of disassembly instruction token sequences.
- Graph-based instruction association module (Module 3): We construct the corresponding instruction association graph of the input pair of binary snippets, then generate the refined token representations by relational graph convolutional network.
- Binary similarity comparison module (Module 4): We fuse the final representation vectors of the binary snippets and generate the similarity comparison score by Multilayer Perceptron (MLP) network.

3 Instruction Vectorization Module

The input pair of binary snippets $S_a$ and $S_b$ are originally discrete byte streams, and we first extract their corresponding disassembly instruction sequences. Each instruction contains an opcode and a set of operands. The opcode specifies the
operation performed by the instruction, and the operands represents the operation object, like registers and immediate literals. We tokenize raw disassembly instruction sequences and treat each independent opcode or operand as a token unit for vectorization. The input pair can be represented as token sequence \(T_a = (t_{a1}, t_{a2}, ..., t_{al_a})\) and \(T_b = (t_{b1}, t_{b2}, ..., t_{bl_b})\). \(l_a\) and \(l_b\) are the length of the sequences. To improve generality, we preprocess the original token sequence, replacing the numerical constants with 0 while preserving the negative signs.
Figure 2 shows the working process of our instruction token vectorization module. We create a token lookup dictionary for the processed opcode and operand units. The initial representation of each token is a sparse one-hot vector based on its index within the dictionary, and then we set a trainable token embedding layer to learn the discrete dense vector $e_{a_i}^{(token)}$ of token $t_{a_i}$.

We further extract the char-level features to enrich the instruction token representations with lexical information. We extract the corresponding character (char) sequences of the tokens and generate a char lookup dictionary. Then each token can be represented as a sequence of one-hot vectors of the chars. Similar to the token embedding process, we set up an embedding layer to obtain the dense vector of each char. After that, we deploy a one-dimensional-Convolutional (1D-Conv) layer to extract the local-spatial features of the char sequences. It will slide fixed-size 1D-Conv filters over the char vector sequence of the instruction token and generate corresponding feature maps. Then we process the feature maps by a max-pooling layer to generate the final char-level representations. In specific, for token $t_{a_i}$ with char one-hot sequence $(c_{a_1}, c_{a_2}, ..., c_{a_M})$ of length $M$, its char-level vectorized representation is generated as follows:

$$e_{a_i}^{(char)} = \text{max-pooling} \left( 1\text{D-Conv} \left( c_{a_1}, c_{a_2}, ..., c_{a_M} \right) \right)$$

The final vectorization result $e_{a_i}$ of the instruction token $t_{a_i}$ is the concatenation of token embedding features and character-level features. Note that our initial instruction vectorization process is implemented entirely through learnable parameters without relying on any external pre-trained instruction embeddings.

$$e_{a_i} = \text{Concat} \left( e_{a_i}^{(token)}; e_{a_i}^{(char)} \right)$$

4 Instruction Sequence Encoding Module

From the instruction vectorization module, we obtain the instruction token vector sequences $E_a = (e_{a_1}, e_{a_2}, ..., e_{a_l})$ and $E_b = (e_{b_1}, e_{b_2}, ..., e_{b_l})$ of binary snippets $S_a$ and $S_b$. Our next goal is to encode the functional semantics of the overall binary sequences and generate their meaningful representations. The recurrent neural network (RNN) has a strong sequential context modeling ability and has been widely used in text sequence characterization. We apply it into our binary instruction sequence encoding process. To prevent the gradient vanishing and exploding problems that are prone to occur when encoding long sequences, we apply the LSTM variant instead of the vanilla RNN. We deploy the bidirectional LSTM (Bi-LSTM), with two LSTMs separately encoding forward and backward information. The hidden state $h_{a_i}$ of token $t_{a_i}$ is generated as follows:

$$\overrightarrow{h_{a_i}} = \overrightarrow{\text{LSTM}} (t_{a_1}, t_{a_2}, ..., t_{a_i})$$
$$\overleftarrow{h_{a_i}} = \overleftarrow{\text{LSTM}} (t_{a_i}, t_{a_{i-1}}, ..., t_{a_1})$$

$$h_{a_i} = \text{Concat} \left( \overrightarrow{h_{a_i}}; \overleftarrow{h_{a_i}} \right)$$
After the encoding layers, the binary snippets are represented as the sequences of token hidden vectors, $H_a = (h_{a1}, h_{a2}, ..., h_{al})$, $H_b = (h_{b1}, h_{b2}, ..., h_{bl})$. We keep all tokens’ hidden states without any aggregation or pooling operation. They will be used for subsequent instruction association and instruction representation refinement process.

5 Graph-based Instruction Association Module

5.1 Multi-relational Instruction Association Graph

In this section, we give a specific description of our designed instruction association graph schema. Our goal is to model dependencies of instructions from multiple perspectives and refine the quality of instruction token representations. For the instruction token sequence $T_a$ and $T_b$ processed from the input binary snippets, we regard each token as a node and establish the corresponding instruction association graph $G = (T, E, R)$. $T$ is the node set, $E$ denotes the edge set, and $R$ is the type set of the edges. Note that we construct an independent instruction association graph for each binary pair to be compared, so the graph structure will change dynamically for different input pairs.

We design the following six types of edges to represent the semantic relationships between instruction token nodes, including edges of mono-architecture token pairs and edges of cross-architecture token pairs.

Mono-architecture Association Edges

- **Mono-architecture opcode-operate-operand edge ($e_0$)**: We associate the opcode with each operand within the same disassembly instruction, indicating the operational relationship.
- **Mono-architecture operands co-occurrence edge ($e_1$)**: We associate each operand pair within a disassembly instruction, displaying their co-occurrence-based relevance.

In specific, for the instruction "MOV $\sim R0, R4" , we associate token "MOV" with tokens "R0" and "R4" by edges of type $e_0$, indicating that opcode "MOV" operates on registers "R0" and "R4". Meanwhile, tokens "R0" and "R4" are associated with the $e_1$ edge, denoting that they co-occurred within the same disassembly instruction. These two types of edges will establish context-based dependencies of the mono-architecture token sequence, improving the semantic representations of opcodes and operands without resorting to external instruction pre-training.

Cross-architecture Association Edges

- **Cross-architecture opcodes prefix-match edge ($e_2$)**: We connect two cross-architecture opcodes with the same $n$ prefix characters. Although different architectures have separate instruction sets, some opcodes that perform similar operations have similar char-level lexical characteristics. Such
as “SUB”, “SUBSD”, “SUBPD”, “SUBSS” of the x86 architectures, and “SUB”, “SUBS” of the ARM architecture will perform similar operations, and they all contain the “SUB” prefix. This type of edge is meaningful for identifying instruction sequences implementing similar functions.

- **Cross-architecture operands value-match edge**\( (e_3) \): We associate two cross-architecture operands with the same value after preprocessed. It will establish dependencies between numeric constants, identical symbols, and identical string literals of different architectures, assisting the semantic comparison process of disassembled code fragments.

- **Cross-architecture operands type-match edge**\( (e_4) \): For a similar purpose to \( e_3 \), we associate cross-architecture operands with the same fine-grained category. We consider three fine-grained operand types: registers, immediate literals, and memory address pointers.

- **Cross-architecture heuristic position alignment edge**\( (e_5) \): We define heuristic rules to establish positional associations between the token pairs of cross-architecture instruction sequences. Specifically, tokens \( t_{a_i} \) and \( t_{b_j} \) of sequences \( T_a \) and \( T_b \) will be associated if they meet the following conditions:

\[
\left| \frac{a_i \times l_a}{l_b} - b_j \right| < \xi
\]

\( a_i \) and \( b_j \) are the position indices of the tokens in the respective sequences. \( l_a \) and \( l_b \) are the lengths of the sequences. \( \xi \) is a pre-defined threshold.

The \( e_5 \) edge is inspired by Redmon et al. [40]. We set the edge weights of the instruction association graph as their statistical frequencies, \( e_0 \) is unidirectional, and \( e_1 \) to \( e_5 \) are undirected edges. The same endpoint token nodes may be associated with multiple different types of edges, and our strategy of utilizing multi-type of dependencies will be illustrated in the next subsection.

### 5.2 Relational Graph Convolutional Network

After building the instruction association graph, we expect to refine the semantic representation of instruction tokens with the multi-relational graph schema. Graph neural network (GNN) [42] has strong graph structures representation abilities, and it has achieved promising performance in diverse tasks such as node classification and link prediction. The classic GNN is a message-passing framework with two core operations, neighbor node information aggregation and node representation update. It iteratively aggregates neighbor node information and updates the vectorized representations of nodes with local subgraph features.

Specifically, for a token node \( t_v \) of set \( \mathcal{F} \) with the corresponding neighbor set \( \mathcal{N}(t_v) \), the neighbor node information aggregation and node representation update process of a GNN layer are performed as:

\[
h_{t_v} = \mathcal{F}(x_{t_v}, \text{AGG} (\{h_u : t_u \in \mathcal{N}(t_v)\}))
\]

\( x_{t_v} \) is the initial representation of \( t_v \), and \( h_{t_v} \) denotes the updated representation calculated by the aggregated neighbor node features and the fusion function \( \mathcal{F} \).
Our instruction association graph connects instruction token pairs with semantically distinct edges. To better exploit the multi-type dependencies, we choose the relational graph convolutional network (R-GCN) [43], a GNN variant that can efficiently handle multi-relational graph data. R-GCN extends the classic GNN framework with type-specific parameters to model the relations of different types separately. For token node \( t_v \), the \( l \)th R-GCN layer maps its neighbor node-set \( \mathcal{N}_{e_r}^{er}(t_v) \) associated with edge type \( e_r \) to a unified vector space through relation-specific transformation matrix \( W_{l e_r} \), and aggregates the transformed vectors in the normalized summation way. The node’s characteristics of the previous layer \( h_{l t_v} \) is preserved by a separate feature transformation matrix \( W_{l 0} \). The overall \( l \)th layer node representation refinement process is as follows:

\[
    h_{l+1}^{t_v} = \sigma \left( \sum_{e_r \in R} \sum_{t_u \in \mathcal{N}_{e_r}^{er}(t_v)} \frac{1}{|\mathcal{N}_{e_r}^{er}(t_v)|} W_{l e_r}^{t_v} h_{l t_u}^{e_r} + W_{l 0}^{t_v} h_{l t_v}^{l 0} \right)
\]  

(7)

A Single R-GCN layer can only aggregate first-order neighbor information. We stack multiple R-GCN layers to propagate multi-hop neighbor messages, learning the substructure of different scales within the instruction association graph. For token \( t_a \), its corresponding input node attributes of the first R-GCN layer are the hidden states \( h_a \) generated by the previous token vectorization layers and the Bi-LSTM encoder, which contains the tokens’ lexical semantics and the sequential information of the mono-architecture binary sequence. The final R-GCN layer will output its refined representation \( r_a \), and \( B_a \) and \( B_b \) will be represented as \( R_a = (r_{a_1}, r_{a_2}, ..., r_{a_n}) \) and \( R_b = (r_{b_1}, r_{b_2}, ..., r_{b_k}) \).

Figure 3 is the technical explanation of the overall graph-based instruction association module. The left side is an instruction association graph schema cor-
responding to an input pair of disassembly instruction sequences. We reserve one example edge for each type. On the right is the node representation refinement process performed by R-GCN layers.

6 Binary Similarity Comparison Module

The graph-based instruction association module will generate refined instruction token representation sequences \( R_a \) and \( R_b \). We send the sequences to another Bi-LSTM layer to strengthen the sequential context information, and then employ a max-pooling layer to generate the final binary snippet representations \( F_a, F_b \).

The process can be simplified as follows:

\[
F_a = \text{max-pooling} \left( \text{Bi-LSTM} \left( r_{a_1}, r_{a_2}, \ldots, r_{a_l} \right) \right) \quad (8)
\]

We set up a fusion function to aggregate the final vector \( F_a \) and \( F_b \), and then feed the result into a one-layer MLP classifier with the softmax function to predict the similarity score of \( S_a \) and \( S_b \). The fusion function is based on [4], including the concatenation, element-wise difference, and element-wise product of \( F_a \) and \( F_b \), as follows:

\[
F_{(a,b)} = \text{Concat} \left( F_a; F_b; F_a - F_b; F_a \odot F_b \right) \quad (9)
\]

This fusion way ensures that the MLP classifier can identify the boundary of the two representation vectors, and calculate the similarity between \( F_a \) and \( F_b \) more accurately. The overall neural model is optimized by minimizing the cross-entropy loss between the predicted scores and the ground truth pair labels.

7 Evaluation

7.1 Preliminary

Dataset. We evaluate our approach on three datasets with two granularities:

(i) Dataset1 is a collection of basic block pairs provided by INNEREYE [49] with annotated ground truth, compiled from coreutils-8.29, findutils-4.6.0, diffutils-3.6, binutils-2.30, and OpenSSL-1.1.1-pre1 packages by the clang-6.0.0 compiler and O2 optimization, into x86 and ARM architectures.

(ii) We build the function-level Dataset2 from the same packages of Dataset1 by two compilers, clang-6.0.0 and GCC-5.4.0, also with O2 optimization.

(iii) We construct Dataset3 with seven families of IoT malware samples captured by honeypots deployed in real-world network environments. We select samples spread on ARM and MIPS architectures, which are widely used in IoT devices, and build a large-scale cross-architecture malware reuse function matching dataset.

We annotate the ground truth of Dataset2 and Dataset3 with binary name and function name as the unique ID to identify functions compiled from the same source code. When building Dataset3, we filtered out functions of stripped
### Table 1. Statistical information of evaluation datasets

| Dataset | Architectures   | Granularity | # Pairs | Average # Edges | Average # Instructions |
|---------|-----------------|-------------|---------|----------------|------------------------|
| Dataset1 | x86-ARM         | Basic-Block | 11,2019 | 239.50         | 7.09                   |
| Dataset2 | x86-ARM         | Function    | 74,841  | 1142.31        | 28.38                  |
| Dataset3 | ARM-MIPS        | Function    | 460,386 | 737.21         | 33.49                  |

binaries whose names could not be correctly identified by the disassembler. Table 1 shows the information of our datasets. The last two columns represent the average number of edges of the instruction-association graphs, and the average number of disassembly instructions contained in each binary snippet.

**Evaluation metrics.** We consider two groups of metrics in evaluation:

(i) For basic block-level evaluation, we follow the prior art [50,40] and use AUC-ROC (Area under ROC curve) as the evaluation metric.

(ii) For function-level evaluation, we set up the function search task as the prior art [28,31,48]. It will compare a query binary function with multiple candidate functions and rank the corresponding similarity scores. In our experiments, we set one positive candidate similar to the query function, together with $N_{neg}$ dissimilar candidates. We adopt two commonly used evaluation metrics, precision@1 and MRR (Mean Reciprocal Rank). For each query function, the precision@1 value indicates whether the score of the positive candidate function is ranked first, and the MRR value is calculated as the reciprocal of the positive candidate’s ranking position.

**Implementation details.** We implement the proposed method with the PyTorch framework, PyTorch Geometric library [14], and radare2 disassembler [38]. The parameters are optimized by Adam with a learning rate of 1e-3. The dimension of the instruction token embedding layer is set to 128, and the char embedding dimension is 32. The size of char 1-D convolutional filters is 2, and the number is 64. We set up one Bi-LSTM layer and two R-GCN layers with the hidden dimension of 256. The $n$ value of the Cross-architecture opcode prefix-match edge ($e_2$) is set to 3, and the $z$ threshold of the Cross-architecture heuristic position alignment edge ($e_5$) in the equation 5 is set to 2. Under this setting, our system can achieve the best results on the development sets. For Dataset2 and Dataset3, the number of negative candidates $N_{neg}$ for each query function is 20.

### 7.2 Basic block-level Experiments

**Comparisons with the prior art.** In this section, we evaluate our approach at the basic block-level dataset and compare it with two manually designed baselines and three state-of-the-art cross-architecture binary similarity comparison approaches. The implementations of the comparison methods are as follows:
- String edit distance: We use python-Levenshtein [25] to compute edit-distance-based similarity scores of the cross-architecture basic block pairs.
- Char n-gram: We extract the char n-gram sets of the assembly instruction sequences and calculate their Jaccard similarity score. 4-gram performs best in our evaluation.
- Gemini [46] features + SVM: Xu et al. extracted the statistical features to represent a basic block, such as the number of instructions, calls, and numeric constant. Following Zuo et al. [50], we concatenate the features of two blocks and use SVM with RBF kernel to predict their similarity.
- INNEREYE [50]: Zuo et al. used word2vec to pre-train assembly instruction embeddings on external code corpus. Then encode the cross-architecture instruction sequences by two individual LSTM networks and generate the similarity score based on the distance metric.
- Redmon et al. [40] proposed an instruction pre-training method based on joint objectives. They establish position-based alignments of cross-architecture instruction pairs, and set the mono-architecture and cross-architecture objectives to training instruction embeddings.

Table 2. Basic block-level cross-architecture binary similarity comparison results on Dataset1.

| Approaches                     | ROC-AUC |
|--------------------------------|---------|
| String edit distance           | 0.8087  |
| Char n-gram                    | 0.7746  |
| Gemini features + SVM [46]     | 0.8647  |
| INNEREYE [50]                 | 0.9764  |
| Redmond et al. [40]            | 0.9069  |
| (- Mono-arch edges)            | 0.9917  |
| (- Cross-archs edges)          | 0.9885  |
| (- Type-specific aggregation)  | 0.9825  |
| **Our approach**               | **0.9924** |

We use the instruction embedding files of INNEREYE [49] and Redmond et al. [39] to make fair comparison. The AUC-ROC on Dataset1 are shown in the upper part of Table 2. From the results, we can mainly draw the following conclusions:

- The performance of edit distance, char n-gram, and Gemini + SVM is not ideal, which shows the syntax or statistical-features based comparison can not handle the significant differences of cross-architecture instruction sets.
- INNEREYE and our approach outperform other methods by large margins, which proves that exploiting deep neural networks to automatically extract the features of disassembly instruction sequences is a very effective solution.
Our approach can achieve the best performance. The improvement is mainly because our graph-based instruction association module can effectively bridge the gap in the representation spaces of cross-architecture instructions. Furthermore, we do not rely on external pre-training to generate initial instruction embeddings, avoiding the additional workload and time consumption.

Ablation studies. We design three ablation variants of our approach to evaluate the core components of our graph-based instruction association module: (i) Remove the mono-architecture association edges ($e_0$ and $e_1$). (ii) Remove the cross-architecture association edges ($e_2 \sim e_5$). (iii) Remove the type-specific neighbor message aggregation mechanism of R-GCN layers and use the classic graph convolutional network [22]. The lower part of Table 2 presents the results of the ablation experiments. It proves that the mono-architecture and cross-architecture associations all contribute to performance improvement. And separately aggregating neighbor messages from different types of dependencies can more effectively refine the instruction representation and improve the cross-architecture similarity comparison performance.

7.3 Function-level Experiments

In this section, we evaluate our approach at the function-level Dataset2 and compare it with two existing approaches. We set up the binary function search task on Dataset2. The first work we make comparison with is INNEREYE, which performs best in the basic block-level experiments. The second is another function-level binary similarity comparison approach, SAFE [31]. It also used word2vec to implement instruction pre-training, and deployed the Bi-GRU network to encode disassembly instruction sequences. Then it added the self-attention mechanism to generate instruction representation weights. Instructions that are more important for binary semantic comparison results will be assigned higher weights.

Since the pre-trained instruction vocabulary provided by INNEREYE are pretrained on the code corpus compiled by clang, while Dataset2 also involves the GCC compiler, 42.12% of the instructions are out-of-vocabulary (OOV). Meanwhile, the instruction embeddings provided by SAFE are also generated by the external corpus inconsistent with the compilation environment of Dataset2. Therefore, we use the trainable instruction embedding and concatenate the char-level features similar to our approach for their instruction vectorization. This phenomenon also illustrates the limitations of the external instruction pre-training approach. Since it is difficult to accurately predict the binary compilation settings in practical applications, serious instruction OOV issue is prone to occur.

Table 3 shows the comparison results on Dataset2. From the table, we can see that our approach has significant performance advantages, with at least 21.19 points improvement of the precision@1 value and 17.22 points improvement of the MRR value than the variants of INNEREYE and SAFE. Compared with the results of basic block-level experiments, our function-level improvement is more prominent. On the one hand, the reason is that the instruction sequences of
Table 3. Function-level cross-architecture binary similarity comparison results on Dataset2.

| Approach                  | Precision@1 | MRR  |
|---------------------------|-------------|------|
| INNEREYE (42.12% OOV)    | 0.5014      | 0.6619 |
| INNEREYE + Char-features | 0.6386      | 0.7665 |
| SAFE + Char-features      | 0.7097      | 0.7828 |
| **Our approach**          | **0.9216**  | **0.9550** |

Function-level binary snippets are longer and implement more complex semantic functional modules, which increases the difficulty of cross-architecture binary semantic comparison. As shown in Table 1, our instruction association graph will establish more multi-type edges on Dataset2, and the effect of bridging the semantic representation space of binary snippets of different architectures is more significant. On the other hand, the function search task needs to compare the query function with multiple candidates and rank the similarity scores, which is more challenging than the pairwise comparison conducted at basic block-level.

7.4 Real-world IoT Malware Reuse Function Matching Experiments

In this section, we use Dataset3 to evaluate the scalability and practicability of our method in real-world applications. Dataset3 is constructed from malware captured in the public network by IoT honeypots. We use radare2 to process unstripped malware samples of ARM and MIPS architectures and construct a large-scale dataset containing over 460k cross-architecture function pairs, characterizing malicious behaviors from a more refined perspective. We also make comparisons with INNEREYE and SAFE. Since their pre-trained instruction embeddings did not support MIPS architecture, we still compare with their variants using trainable embeddings and char-level features for instruction vectorization.

Table 4. Cross-architecture binary similarity comparison results on Dataset3.

| Approach                  | Precision@1 | MRR  | Offline training-time (seconds/epoch) | Online prediction-time (milliseconds/pair) |
|---------------------------|-------------|------|--------------------------------------|------------------------------------------|
| INNEREYE + Char-features | 0.7780      | 0.8366 | 101                                  | 1.58                                      |
| SAFE + Char-features      | 0.7840      | 0.8386 | 318                                  | 1.84                                      |
| **Our approach**          | **0.9375**  | **0.9597** | 823                                  | **3.72**                                  |

Table 4 shows the performance of the three approaches on Dataset3, along with their offline training time (seconds per epoch) and online prediction time (milliseconds per function pair). The results show that our method significantly
outperforms the variants of INNEREYE and SAFE, with precision@1 and MRR values improving at least 16.97 and 12.11 points, respectively. Due to the instruction association graph construction and the R-GCN-based multi-type dependencies aggregation on the graph, the training time and prediction time of our method are increased. However, the online prediction speed is still acceptable as inferencing the similarity score of a binary function pair can be completed in 3.72 milliseconds. Meanwhile, we do not need additional time collecting external code corpus consistent with the specific application’s compilation settings and pre-training disassembly instruction embeddings. In conclusion, our method can be effectively applied to large-scale real-world cross-architecture binary similarity comparison collection and provides a valuable solution for defending against malware reused and propagated on IoT devices of different architectures.

8 Related Work

8.1 Traditional Binary Similarity Comparison Approaches

Traditional binary similarity comparison approaches are mainly divided into two categories, static analysis techniques comparing syntax or structural features [24,21,29,36,41,37,19] and dynamic analysis techniques comparing behavioral semantics [27,33,32,20,45]. For static analysis-based methods, Rendezvous [21] extracted the instruction n-perms, control flow sub-graphs, and constants of binary code to construct a code search engine. Qiao et al. [37] used the simhash algorithm to generate basic block signatures, then exploited inverted index to achieve fast reuse function detection. CoP [29] first checked block-level semantic equivalence with theorem prover, and then performed the breadth-first search on the inter-procedural control-flow-graph (I-CFG) to compute path-level binary semantic similarity. These approaches are designed for mono-architecture binary comparison without handling the differences in instruction sets of different architectures. For dynamic analysis-based methods, Ulf et al. [20] recorded the execution traces and output values of a binary pair when given same input, and used matching features to identify programs with similar semantics but different syntax characteristics. BinSim [32] performed enhanced dynamic slicing and extracted the symbolic formulas of the code fragments to check the semantic equivalence. Dynamic analysis will meet challenges when analyzing large binary collections, and it requires additional efforts to configure execution environments supporting diverse architectures and compilation settings.

To support cross-architecture comparison, some existing work converted the instructions of different architectures into the intermediate representation (IR) [35,18,3,12]. Specifically, Multi-MH [35] first converted binary code into platform-independent VEX-IR, then used the input-output pairs of basic blocks to construct their semantic signatures. XMATCH [12] conducted static analysis on IR and extracted conditional formulas as semantic features, improving the binary vulnerability search accuracy. These methods may be limited by the adaptability and precision of IR extraction tools. Esh [7] decomposed binary procedures into small fragments, named strands, then checked the semantically equivalence
of strand pairs and used statistical reasoning for procedure-level similarity comparison, but it also suffers the unscalable issue on the large-scale collections.

8.2 Learning-based Binary Similarity Comparison Approaches

Recently, deep learning technology has achieved promising improvements in intelligent program analysis. To improve the effectiveness and efficiency of the binary similarity comparison task, researchers pay attention to learning-based approaches [10,13,23,46,50,28,15,31,8,30,48,26,9]. α-diff exploited the siamese-CNN network to achieve cross-version binary code similarity detection. They adopted in-batch random negative sampling and contrastive loss to optimize the model. Asm2Vec [8] used the PV-DM model to implement binary function vectorization, achieving accurate binary clone detection against changes introduced by code obfuscation and optimization techniques.

For cross-architecture binary similarity comparison, Gemini [46] extracted the attribute control flow graph (ACFG) of the binary functions. Then it used the structure2vec network and cosine similarity to implement bug search for IoT firmware images. VulSeeker [15] extends ACFG into labelled semantic flow graph (LSFG) by adding additional data flow edges. INNEREYE [50] leveraged wordvec to pre-train instruction embeddings on external code corpus, then implemented binary comparison by LSTM encoders and Manhattan distance. SAFE [31] added the self-attention mechanism to calculate the importance weights of the instructions within the disassembled code sequence, improving the cross-architecture binary similarity matching accuracy. The common dilemma of existing learning-based approaches is that the cross-architecture binary snippets are encoded separately by neural layers and then compared based on the similarity metrics. The significant difference between cross-architecture instruction sets will lead to a considerable gap in their semantical representation spaces, which limits the comparison performance. Our method utilizes the multi-relational instruction association graph and R-GCN layers to close the gap in the semantic spaces of cross-architecture instructions, effectively alleviating the deficiency.

9 Conclusion

In this paper, we propose a novel cross-architecture binary similarity comparison approach. We design an instruction association graph schema to bridge the gap in the semantic spaces of instruction sets from different architectures. It consists of six types of dependencies, which respectively define the context relevance of mono-architecture instruction tokens and multi-perspective semantic associations of cross-architecture tokens. We leverage the R-GCN network to propagate the multi-type dependencies within the graph and improve the cross-architecture binary matching performance. We conduct extensive experiments on datasets of different granularities. Results show that it outperforms existing learning-based approaches on basic block-level and function-level comparisons.
Furthermore, our approach can achieve effective cross-architecture reuse function detection on a large-scale IoT malware dataset collected from the real-world network environment, which is meaningful for identifying malware spread on IoT devices of various architectures and defending against IoT attacks.

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