Analysis and Experiment of Nanosecond Pulse Circuit Based on Commercial Si-p-i-n Rectifier Diode

Zhaoyang Wu, Yan Wang, Jingwen Zhang, Fanbao Meng, Hengqing Zhang, and Xun Hou

Abstract—In this article, a nanosecond pulse generation circuit is designed and fabricated based on a commercial Si-p-i-n rectifier diode using the DSRD principle. The circuit is composed of four parallel stacks with a 3-kV pulse output and a rise time of less than 2 ns. Each stack contains four diodes in a series. The working principle and main parameters of the circuit are analyzed by Pspice, and the simulation results are consistent with the experimental results. Switching cutoff speed, reverse voltage, offset voltage, and the topological circuit structure of connecting the rectifier diodes affect the amplitude and rise time of the output pulse.

Index Terms—Circuit simulation, DSRD, nanosecond, p-i-n diode, pulse.

I. INTRODUCTION

HIGH-VOLTAGE fast switch has a wide range of application values in ultrawideband technology [1], laser drive technology [2], particle accelerator systems [3], [4], automobile engine ignition systems [5], plasma discharge [6], sewage treatment [7], medical treatment [8], and other fields. The gas engine ignition systems [5], plasma discharge [6], sewage technology [2], particle accelerator systems [3], [4], automobile engine ignition systems [5], plasma discharge [6], sewage treatment [7], medical treatment [8], and other fields. The gas engine ignition systems [5], plasma discharge [6], sewage technology [2], particle accelerator systems [3], [4], automobile engine ignition systems [5], plasma discharge [6], sewage treatment [7], medical treatment [8], and other fields. The gas engine ignition systems [5], plasma discharge [6], sewage technology [2], particle accelerator systems [3], [4], automobile engine ignition systems [5], plasma discharge [6], sewage treatment [7], medical treatment [8], and other fields. The gas engine ignition systems [5], plasma discharge [6], sewage technology [2], particle accelerator systems [3], [4], automobile engine ignition systems [5], pulse.

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is limited. The third type is the single switch circuit [12], [20] that only needs one primary switch. The forward injection and reverse extraction of DSRD are realized through switch’s opening and closing states. This circuit has a simple structure and low loss. By selecting high-speed MOSFET as the primary switch, MHz repetitive operation frequency can be realized.

Unfortunately, much of the literature directly gives the circuit’s final parameters for the third kind of circuit, and the parameters in similar circuits are differing. When using a rectifier diode to design a pulse circuit in the DSRD operating mode, circuit parameters’ choice is confusing. In addition, the literature often focuses on the pulse’s output power and repetition frequency, while the factors affecting pulse output performance are less discussed.

This article designs a high-voltage nanosecond pulse generation circuit based on commercial Si-p-i-n rectifier diodes with only one primary switch. The circuit configuration and main parameters are analyzed in detail, and the factors affecting pulse output are also discussed by the Pspice simulation and experiment. Using the combination of four stacks in parallel, each stack containing four diodes in series, a 3-kV nanosecond pulse is generated with a rise time of about 2 ns. This article’s analysis and experiment methods are beneficial for developing a fast high-voltage nanosecond pulses circuit with commercial devices similar to DSRD. This article is arranged as follows. Section II presents the nanosecond pulse generation circuit principle and estimates the circuit parameters. At the same time, the effects of diode cutoff time and load parasitic parameters on output performance are analyzed by simulation. Experimental results are given in Section III, and the factors affecting pulse output are discussed. The conclusion is highlighted in Section IV.

II. THEORY OF PULSE GENERATING CIRCUIT

A. Principles of Circuits

The circuit configuration of high-voltage pulse generation is shown in Fig. 1. At the initial time, switch $S$ is opened, and capacitor $C_2$ is charged through the loop of $V_1 - L_1 - C_2 - L_2 - R_1 - V_2$, where $V_1 > V_2$ [see Fig. 1(a)]. Then, switch $S$ is closed to pump the current of the diode $D$ in the forward direction through the $C_2 - S - D - L_2$ loop, and $V_1$ charges $L_1$ concurrently [see Fig. 1(b)]. Tens of nanoseconds later, switch $S$ is opened again. The current through $L_1$ changes direction to $C_2 - L_2 - D$, resulting in diode $D$ pulsing in the reverse direction. Diode $D$ is quickly interrupted when the carrier stored in the p-n junction is extracted completely. The current through diode $D$ is switched to $R_L$ through capacitor $C_4$, generating a high-voltage pulse on $R_L$ [see Fig. 1(c)]. Diode $D$ cutoff speed determines pulse rise time. Setting the value of $V_1 - V_2$ can be used to adjust the forward pumping current. $V_1$ can also be used to adjust the reverse current. The time of switch $S$ turning on determines the forward pumping time. $C_1$ is the power supply regulated capacitance. $C_3$ can limit the overshoot voltage of switch $S$ when diode $D$ is interrupted. $C_4$ blocks the direct current. $R_1$ limits the charging current of $V_2$ and blocks voltage pulses when diode $D$ is interrupted.

B. Circuit Parameters’ Estimation

As shown in Fig. 1, when switch $S$ is closed [see Fig. 1(b)], $C_1$, $L_1$, $S$, and the resistance $R_d$ (including switch-on resistance and loop distribution resistance) form an oscillation loop. To obtain a large current, the inductor $L_1$ value should be less than hundreds of nanohenries, while the regulated capacitance $C_1$ is usually greater than or equal to 1 $\mu$F. Thus, the resistance $R_d$ is approximately equal to $2(L_1C_1)^{1/2}$, and the $L_1$ current is

$$I_{L_1} = \frac{V_1}{L_1} \Delta t e^{-\frac{R_d}{2L_1} \Delta t}$$

(1)

where $\Delta t$ is the turn-on time of switch $S$.

When switch $S$ opens again [see Fig. 1(c)], $L_1$ current will transfer to $L_2$, and its energy will transfer to $L_2$ through $C_2$; consequently, $L_1 = L_2$ and $I_{L_1} = I_{L_2}$, where $I_{L_2}$ is the current flowing through $L_2$. The reverse current of diode $D$ can be approximately equal to $I_{L_2}$, that is, $I_D = I_{L_2} = I_{L_1}$.

As diode $D$ turns off, its resistance increases with time, and time dependence resistance is set as $R_d(t)$. To obtain a large voltage on $R_L$, $C_4$ capacitance should meet

$$Z_{C4} = \frac{1}{\omega C_4} \ll R_L$$

(2)
where \( \omega \) is the angular frequency. The total impedance of the subsystem composed of diode \( D \), capacitor \( C_1 \), and load \( R_L \) is

\[
R_{\text{tot}} = \frac{(R_L + 1/\omega C_4) \cdot R_D(t)}{(R_L + 1/\omega C_4) + R_D(t)} \approx \frac{R_L \cdot R_D(t)}{R_L + R_D(t)}.
\]  (3)

During the diode \( D \) cutoff, the current \( I_D \) will decay exponentially with a decay constant of \( L_2/R_{\text{tot}} \). When diode \( D \) is completely cut, the maximum load current on is

\[
I_{RL,\text{max}} = I_D e^{-\frac{t}{\tau}}.
\]  (4)

\( t \) is the time of diode \( D \) completely interrupted. According to (1) and (4), \( L_1 = L_2 \), \( I_D = I_{L1} \), and the maximum load current is

\[
I_{RL,\text{max}} = \frac{V_1}{L_1} \Delta t e^{-\frac{\Delta t}{\tau}} e^{-\frac{\Delta t}{\tau}}.
\]  (5)

According to (5), the maximum current on load is related to \( L_1 \). Taking \( t \) as a constant, derivate \( L_1 \) for (5) and set (6) to zero

\[
\frac{dI_{RL,\text{max}}}{dL_1} = 0.
\]  (6)

When \( I_{RL,\text{max}} \) is maximized, \( L_1 \) is equal to

\[
L_1 = \frac{R_l R_D(t)}{[R_L + R_D(t)]} t + \frac{R_D}{2} \Delta t.
\]  (7)

When diode \( D \) is turned off, \( R_L \ll R_D \), so \( L_1 \approx R_L t + (R_D/2) \Delta t \). In general, the Si-p-i-n rectifier diode with reverse withstand voltage \( \geq 1 \) kV has an \( i \) layer width \( \geq 120 \) \( \mu \)m. Since Si’s electron saturated drift velocity is around \( 1 \times 10^7 \) cm/s, the time needed for electron transit through \( i \) layer is \( > 1.2 \) ns. Thus, when sets \( t = 2 \) ns, \( \Delta t = 80 \) ns, \( R_D = 1 \) \( \Omega \), and \( R_L = 50 \) \( \Omega \), \( L_1 \) is about 140 nH.

In addition, when switch \( S \) is closed [see Fig. 1(b)], \( C_2 \), \( S \), \( D \), \( L_2 \), and distribution resistance also form an oscillation loop that pumps diode \( D \) in the forward direction. The pumping time (\( \Delta t \)) should be less than half of the period of oscillation. Here, we take \( \Delta t < \pi (L_2 C_2)^{-1/2} \) for simplicity, so when \( \Delta t = 80 \) ns and \( L_2 = 140 \) nH, \( C_2 \) should exceed 4.6 nF.

**C. Circuit Simulation**

The circuit shown in Fig. 1 is simulated by Pspice software. Switch \( S \) is an ideal model with a turn-on time of 80 ns, and the front and rear edges of the switching time are less than 10 ns. The other circuit parameters are set as: \( C_1 = 1 \) \( \mu \)F, \( C_2 = 100 \) nF, \( C_3 = 1 \) nF, \( C_4 = 1 \) nF, \( R_1 = 1 \) k\( \Omega \), and \( R_L = 50 \) \( \Omega \). Diode \( D \) adopts the Pspice diode model of 1N4007 [12]. When \( V_1 \) is 105 V and \( V_2 \) is 55 V, the load output voltage is approximately 1.2 kV, and the rise time is about 2 ns.

The simulated waveform of load voltage and diode current is shown in Fig. 2. The black curve represents the ON state of switch \( S \).

As shown in Fig. 2, the interrupted diode current is about 42 A, which is close to the calculated current, according to (1) (about 45 A), while the current on load is about 24 A. It takes time for the diode to cut off, so the load current is less than the cutoff current. According to (4), the shorter the cutoff time, the larger the load current obtained. In other words, the faster the pulse rise time, the greater the load current. The simulation’s influence of pulse rise time on load current is shown in Fig. 3, where a Pspeice open switch model \( S_2 \) replaces the diode’s cutoff process.

Initially, switch \( S_1 \) is open and \( S_2 \) is closed. Next, \( S_1 \) is closed at time \( t_1 \) and \( V_s \) charges the inductive \( L_c \). After a few tens of nanoseconds, \( S_2 \) is open at time \( t_2 \). The current flowing through \( L_c \) changes its direction to load \( R_2 \).

The load currents with different rise times are obtained by setting different switch \( S_2 \) cutoff times, as shown in Fig. 4. The current amplitude decreases with the increase of rise time. When the rise time is about 2 ns, the load current slightly exceeds half of the maximum current.

In generating nanosecond pulses, the load distribution parameters impact output characteristics. The distributed parameters mainly come from the series parasitic inductance and parallel parasitic capacitance the load connection introduces. The capacitive reactance and inductive reactance are \( Z_{cr} = 1/2\pi fC \) and \( Z_{Lcr} = 2\pi fL \), respectively. For pulse voltage with rise time \( t_r \), \( f = 0.35/t_r \). When \( t_r = 2 \) ns, calculated, \( Z_{cr} = 0.9 \times 10^{-3}/C \) and \( Z_{Lcr} = 1.1 \times 10^6 L \). The schematic of parasitic inductance (\( L_1 \)) and parasitic capacitance (\( C_i \)) introduced by the load is shown in Fig. 5.

The load current is reduced when the series parasitic inductance is introduced. Assuming a requirement to reduce the
load current by less than 10%, the parasitic inductive reactance should meet \( R_L/(R_L + Z_{Ls}) > 0.9 \), where \( R_L = 50 \) Ω. Thus, \( Z_{Ls} < 5.5 \) Ω and \( L_s < 5 \) nH. The simulation results of load current variation under different series parasitic inductance are shown in [see Fig. 6(a)]; when \( L_s < 5 \) nH, the load current waveform hardly changes, \( L_s = 10 \) or 15 nH, the load current decreases, and the rise time increases.

When parallel parasitic capacitance is introduced, the capacitance will shunt the load current. Assuming that the parasitic capacitance current required is less than 10% of the load current, the capacitive reactance of the parasitic capacitance needs to be met, \( Z_{cs} > 10R_L \). Thus, \( C_s < 1.8 \) pF. The simulation results of load current variation under different parallel parasitic capacitance are shown in [see Fig. 6(b)]. When \( C_s = 1 \) pF, the load current is hardly unchanged. When \( C_s = 10 \) pF, 100 pF, and 1 nF, the load current decreases and the rise time increases.

III. EXPERIMENTAL RESULTS AND DISCUSSION

According to simulation circuit parameters, a pulse generator was made by a cell rectifier diode (ARS50M by Taiwan Semiconductor with 1000-V reverse voltage and 50-A forward current), as shown in Fig. 7. Switch \( S \) is replaced by a high-speed MOSFET (DE475-102N21A by IXYS), and inductors \( L_1 \) and \( L_2 \) are wound by a hollow helix. A noninductive
resistor of 0.1 Ω is installed between diode D and the reference ground for current measurement, which is tested by a voltage probe with a bandwidth of 500 MHz. The output pulse was measured with a 50-Ω high-voltage, high-frequency attenuator (60 dB) and an oscilloscope with a bandwidth of 1 GHz (LeCroy wave runner 140Xi-A).

Set driving time of MOSFET to 80 ns. When \( V_1 = 105 \) V and \( V_2 = 55 \) V, the output voltage is about 1.17 kV and the rise time is about 2 ns, as shown in Fig. 8.

**A. Influence of \( V_1 \) and \( V_2 \) on Output**

Keeping \( \Delta V \) \((V_1 - V_2)\) and \( \Delta t \) unchanged and changing the voltage amplitudes of \( V_1 \) and \( V_2 \), the test waveforms are shown in Fig. 9. When \( V_1 = 105 \) V and \( V_2 = 55 \) V, the maximum cutoff current (about 38 A) and output voltage (about 1.17 kV) are obtained. However, when \( V_1 \) and \( V_2 \) are above or below 105 and 55 V, respectively, the cutoff current and output voltage decrease, and multiple pulses occur simultaneously. In addition, although \( \Delta V \) and \( \Delta t \) were unchanged, the forward injection current is not maintained but decreases with increasing \( V_1 \) and \( V_2 \).

According to the DSRD operational principle, the forward injected charge should be equal to the extracted charge [17]. If \( V_1 \) is too small, the reverse current cannot extract all the forward injected charge when the reverse current reaches the maximum. Only after the reverse current has passed, the maximum can the forward injected charge be extracted completely. At this point, the cutoff current exceeds the maximum value, resulting in a smaller output voltage of the load, as shown in Fig. 9(a) and (b).

If \( V_1 \) increases, \( V_2 \) will also increase to keep \( \Delta V \) constant. From the circuit shown in Fig. 1, \( V_2 \) adjusts the voltage of capacitor \( C_2 \) and is the reverse voltage of diode \( D \). Under the reverse voltage \( V_2 \), the p-n junction depletion layer width is

\[
W_d = \sqrt{2\varepsilon V_2/qN}
\]

where \( \varepsilon \) is the relative permittivity of Si, \( q \) is the electron charge, and \( N \) is the doping concentration in the \( i \) layer. Therefore, the capacitance of the p-n junction is

\[
C_{PN} = \varepsilon A/W_d = A\sqrt{\frac{\varepsilon qN}{2V_2}}
\]

where \( A \) is the chip area of diode \( D \). When the forward current is injected into diode \( D \), the charge consumed by the depletion layer is

\[
Q_d = V_2C_{PN} = A\sqrt{\frac{\varepsilon V_2 qN}{2}}.
\]

Equation (10) indicates that the higher the bias voltage \( V_2 \), the more charge is consumed. Under the same conditions of \( \Delta V \) and \( \Delta t \), the forward injection charge is reduced with \( V_2 \) increase, resulting in a decreased forward injection current. When \( V_1 \) and \( V_2 \) increase to 155 and 105 V, respectively, the forward injection charge is dramatically reduced and quickly extracted completely, as shown in [see Fig. 9(d)], and the cutoff current and load voltage are greatly reduced.

When switch \( S \) is reopened [see Fig. 1(c)], \( L_2, C_2, C_3 \), and diode \( D \) form an oscillation circuit. If \( V_1 \) and \( V_2 \) are too large or too small, diode \( D \) will be interrupted before or
after the maximum reverse current is reached. In both cases, energy stored in \( L_2 \) cannot be fully transferred to the load. The remaining energy in \( L_2 \) will repeatedly inject and extract diode \( D \) through the oscillation loop and generate multiple pulse voltages on the load. Only when diode \( D \) is interrupted at maximum reverse current, can the energy in inductor \( L_2 \) be fully transferred to the load, as shown in [see Fig. 9(c)]. Thus, the best working condition of the pulse generating circuit is that diode \( D \) is cut off when the reverse current reaches the maximum.

### B. Effect of Diode Parallel or Series Connection on Pulse Output

Keep the circuit parameters unchanged and only change the number of diodes \( D \) in parallel. Fig. 10 shows the output pulses with a different number of diodes in parallel. With increase in the number of parallel diodes, the “pedestal” voltage (pedestal voltage refers to the part where the output voltage rises slowly) decreases and the rise time increases.

The “pedestal” voltage mainly is from the voltage on the \( i \) layer before the diode \( D \) is quickly interrupted. It is determined by the reverse current density \( J_{re} \), the width of the \( i \) layer \( W \), and the doping concentration \( N \) of the \( i \) layer

\[
U_{ped} = \frac{J_{re} W}{q \mu_e N} = \frac{I_D W}{q \mu_e N A} \quad (11)
\]

where \( U_{ped} \) is the “pedestal” voltage and \( \mu_e \) is the electron mobility. The drift velocity of electrons in the \( i \) layer is

\[
V_e = \frac{J_{re}}{qN} = \frac{I_D}{qNA}. \quad (12)
\]

According to (11), the “pedestal” voltage is directly proportional to the width of the \( i \) layer. With the increase of series diodes, the total \( i \) layer width increases, increasing “pedestal” voltage.

In addition, when the series diode increases, diode resistance \( R_D \) increases. It can be seen from (4) that the load’s maximum current decreases with an increase of resistance \( R_D \), so the load voltage amplitude also decreases.

Multiple diodes need to be connected in series to prevent breakdown when using diodes to generate higher pulse voltage. When the diodes are connected in series, due to the increase of \( R_D \) and the increase of \( i \) layer width, “pedestal” voltage increases and the load voltage decreases, which is not the desired result. A solution is to use parallel diodes to increase diode area \( A \) and reduce \( R_D \) simultaneously to offset the impact of series diodes.

Although the increase of diode area \( A \) will lead to longer rise time, the higher output voltage also means higher reverse current \( I_D \). From (12), if \( I_D \) and \( A \) increase simultaneously, the electron drift speed can remain unchanged, so the rise time of load pulse voltage can remain unchanged.

Four stacks of diodes are connected in parallel to generate high-voltage pulses, each stack containing four diodes.
in series. The MOSFET driving time is set to 80 ns. The diode reverse current is interrupted at the maximum when in series. The MOSFET driving time is set to 80 ns. The output pulse reaches 3 kV and the rise time is less than 2 ns. The load pulse waveform is shown in Fig. 12.

IV. CONCLUSION

This article makes a pulse generator circuit with commercial p-i-n rectifier diodes. The output pulse is 3 kV, and the rise time is less than 2 ns. The factors affecting the output voltage, such as diode cutoff speed, reverse extraction voltage, bias voltage, diode series, or parallel connection, are studied. It is found that the faster the diode cutoff speed, the greater the current obtained on the load. If the reverse and bias voltages are too large or too small, the diode will have multiple interactions and extraction, resulting in multiple pulses. To obtain the best output voltage, it is necessary to ensure that the reverse extraction current is interrupted when it reaches the maximum. Series connection of multiple diodes accelerates the cutoff speed and increases the “pedestal” voltage. Parallel connection of multiple diodes is beneficial to reducing the “pedestal” voltage but causes rise time increase. In some applications that need to generate nanosecond pulses, p-i-n rectifier diodes are easy to obtain and can replace DSRDs to reduce the cost of pulse generation circuits. However, it should be noted that the commercial p-i-n diode is not specially designed for subnanosecond pulse generation, and it is difficult to generate pulses with a rise time less than 1 ns by using the p-i-n rectifier diode. This article’s analytical and experimental methods have reference significance for developing higher nanosecond pulse voltage using a p-i-n diode with the fast cutoff characteristic similar to DSRD.

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