Modular sub-wavelength diffractive light modulator for high-definition holographic displays

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Abstract. Holography is undoubtedly the ultimate 3D visualization technology, offering true 3D experience with all the natural depth cues, without the undesirable side-effects of current stereoscopic systems (uncomfortable glasses, strained eyes, fatiguing experience). Realization of a high-definition holographic display however requires a number of breakthroughs from existing prototypes. One of the main challenges lies in technology scaling, as holography is based on light diffraction and interference – to achieve wide viewing angles, the light-modulating pixels need to be spaced close to or below the wavelength of the used visible light. Furthermore, achieving high 3D image quality, hundreds of millions of such individually programmable pixels are needed. As a solution, we develop a modular sub-wavelength light modulator, consisting of three main sub-systems: the optical sub-system, comprising a 2D array of sub-wavelength pixels; the driver sub-system for individual pixel control, and the holographic computational engine. Based on conclusions from our state-of-the art studies, numerous experiments and holographic demonstrators, we have focused on reflective phase-modulating MEMS-based system and its scaling beyond 500nm pitch. We have devised a unique binary-programmable phase-modulating pixel architecture realizing vertical pixel displacement of up to 150nm at 500nm pixel pitch, while sustaining low operating voltages compatible with CMOS driver circuitry. IMEC SiGe MEMS technology enables integration of the CMOS pixel-line drivers, scan-line drivers and I/O circuits underneath the 2D MEMS array, resulting in a compact and modular single-chip system design. Refresh rates of few hundred frames per second are achieved using our patented segmented driver-array architecture. Integrated circuits implementing parallel holographic computational engines can be added to the module using advanced 3D stacking technology. Herein we further report on our progress in realizing our first prototype system, featuring 2000x2000 pixels with 1.2µm pixel pitch, to demonstrate the first holographic video module with approximately 30 degree diffraction angle.

1. Introduction

Holography is the only visualization technique that can provide completely natural 3D perceptions. Digital holography combines this unique characteristic of classical holography with the flexibility of computer graphics, making it the ultimate display technology (of the future) [1].

Holographic visualization is in its essence based on two elementary properties of light propagation: light diffraction and interference of the diffracted light waves. Light diffraction is the more effective the smaller the diffractive optical elements, e.g. diffractive gratings or spatial light modulators, splitting the energy of the incident light into multiple diffraction orders (Figure 1). This means that the
ultimate holographic display is simply a spatial light modulator (SLM) with plenty of programmable micro-scale (or even nano-scale) pixels. Reprogramming of these pixels can so-to-speak focus the energy of diffracted light into specific points in 3D space and so create a complex 3D scene [2]. It is however mainly the physical size and pitch of the pixels that determines the overall display efficiency, i.e. the distribution of the incident light energy into ideally only one wide-angle diffraction order, the 3D projection. Such high efficiency 3D projection however requires development of SLM array with sub-wavelength pixel devices (in the range of 400 - 600nm, or smaller), as we demonstrate with our static holographic display chip (Figure 2).

![Figure 1: Diffraction angle of the first five diffraction orders as a function of relative pixel pitch (of a regular diffractive grating), wavelength $\lambda = 635$nm (red). Scaling pixels to sub-wavelength dimensions is critical for high efficiency and wide viewing angle holography. A - IMEC static demo holograms with diffraction angle of 38° (shown in Figure 2). B – IMEC prototype display with pixel pitch of 1.2µm and diffraction angle of 15° (described in Section 5). C – academic state of the art research scaling LCD-based displays to 3µm pixel pitch. D – commercially available LCD and DMD based display devices with pixel pitch down to 6 µm.](image1)

In our feasibility study we have identified the display technology scaling, and so the scaling of the light modulating pixels, as the main challenge limiting the development of high-definition digital holographic displays. As shown in Figure 1, the existing DMD [4] and LCD [5] technologies have rather limited diffractive performance, small projection angles and angular resolution. Furthermore they diffract light into multiple diffraction orders considerably reducing the overall display efficiency.

![Figure 2: Photograph of IMEC static demo hologram with pixel pitch of 500nm, 38° diffraction angle, 104mm × 32mm total surface, 19° off-axis illumination, 158nm vertical pixel displacement and 3D scene of approx. 600k voxels.](image2)
In our previous work we have successfully developed and manufactured large size MEMS-based SLM for deployment in mask-less lithography [6]. Our poly-SiGe MEMS process technology provides means to achieve very high density of MEMS integration as it enables their post-processing on top of standard CMOS circuitry (Figure 3). This prior experience encourages us to further develop our MEMS platform and scale its critical dimensions down to only a few tens of nanometers, making it suitable for manufacturing of holographic display devices.

Figure 3: IMEC µ-mirror device with 8μm pixel pitch, processed using low-temperature polycrystalline SiGe MEMS technology on top of standard CMOS. A 2D chip with 11 million devices has been manufactured at IMEC.

Herein we present the results of our feasibility study, consisting of the display system architecture (Section 2), sub-micron MEMS device design (Section 3), IC circuitry engineering (Section 4), as well as the latest prototype experiments (Section 5).

2. Display module overview
Our display system design is inspired by the PhD work of Mark Lucente [3], more specifically by his idea of holographic elements, the hogels: Imaging a large size holographic display composed of individual hardware modules, a sort of hardware hogels, of a size well below angular resolution of the human eye. Assuming, for example, minimal viewing distance of 2 meters, we devise a holo module of 500×500 μm². Such holo module is made by stacking together a display sub-module (of 1000×1000 500nm MEMS pixels with integrated CMOS drivers) and a digital-hologram generator (DHG) (Figure 4). The 500nm pixel pitch corresponds to about 30° projection angle (for green light wavelength), and the large pixel density guarantees high angular resolution. Incident light is modulated by 1-bit programmable vertical displacement of individual pixels over a distance of approximately 1/4 of the wavelength, resulting in phase modulation. The pixels are designed to have high fill-factor (of at least 80%) for good optical performance.

Operating at 50Hz in full colour mode (using red, green and blue coherent illumination) each holo module requires 150Mb/s data throughput that is easily achievable using existing CMOS technologies. Assuming each holo module encodes/projects approximately 10000 voxels (point sources of light in 3D space), it requires 1.5T holo operations per second. Each such operation is a fully pipelined custom hardware that is implementing the bipolar intensity algorithm [2]. To illustrate these computational requirements, a Radeon HD 5970 can for example reach 5TFLOPS performance, though executing relatively simple standard floating point operations. An ASIC implementation of the 1.5Tops DHG requires 750 bipolar-intensity pipelines running at 2GHz operating frequency. The DHG pipelines, implemented in 12nm CMOS technology, occupy an area of approximately 3mm², which is 12-times the area of the corresponding MEMS module. It is however very likely that further algorithmic
optimizations reduce the DHG computational requirements by more than the factor 12 and the DHG hardware would be implemented on silicon area the size of the corresponding display sub-module. This would enable a relatively straightforward 3D stacking of the two chips, as shown in Figure 4.

The main challenge of the system integration is the seamless tiling of the holo modules, although the ultimate challenge definitely remains the design and development of the MEMS pixel device itself.

Figure 4: Modular holographic display design: Left – detail of a HW holo module with 3D stacked I/O back plate, DHG chip (containing approximately 60 full DHG pipelines) and display chip (including 1 million MEMS pixel devices of 500nm pitch, with integrated CMOS driver logic underneath). Right – example of 16×9 holo modules creating a 144M pixel holographic display with 30° projection angle and a total area of 8×4.5 mm².

3. Sub-wavelength MEMS design
We have explored a large number of rather unorthodox mechanical designs that could eventually deliver the 1/4 wavelength lift (of approximately 150nm in case of red illumination) within the area of just 500×500nm². Most of these designs are however very “MEMS processing unfriendly” as they require very small critical feature sizes. The most suitable and realistic design, which was eventually selected for later prototyping, is the staggered cantilever with three-electrode electrostatic actuation shown in Figure 5. As can be noticed, the actuator part of the pixel device is basically a considerably down-scaled version of the already proven micro-mirror design [6].

Figure 5: Conceptual design of 2D MEMS array with pixel pitch of 500nm and critical processing dimension of 50nm. The staggered MEMS actuators use 3-electrode electrostatic actuation to offset the extended cantilever. This provides an amplified vertical lift to the regularly aligned metallic mirrors atop. The metallic mirrors are designed to reach fill factor of 81% using advanced lithographic processes.
We have evaluated and refined our design using multi-physics simulation tools, taking into account mechanical and electrical properties, as well as constraints imposed by the integrated CMOS driver logic. The most limiting constraint, imposed by the standard high-voltage CMOS technology, is the 32V maximum operating voltage. This restriction considerably influences the mechanical properties of the final design (shown in scale in Figure 5): The actuator “pull-in” voltage is approximately 20V, which is well within the 32V limit, yet the critical dimension for SiGe processing is only 50nm. Resonance frequency of the whole MEMS pixel is in the range above 10MHz, which gives us more than enough time for device reprogramming and mechanical pull down, considering that each of the pixels needs to be reset only once in a few milliseconds.

Device itself exhibits an electrostatic memory effect as it operates in a so-called pull-in actuation regime. This means that we only need to apply the high voltage to pull the actuator into the programmed position, but we can hold the device in that state with much lower voltage. This allows us to simplify the programming scheme for the 2D pixel array, as described in the next section.

The main attention points of the mechanical pixel design are the stiffness of the main torsional element, together with overall robustness and stability of the extended cantilever. These issues are (to considerable extend) taken care of in the prototype design and optimization phase (Section 5).

4. Integrated driver circuitry

The main challenge of the driver logic design has been, simply said, the ever-present question of how to literally squeeze a high-voltage driver underneath every MEMS pixel to reach full array programmability. Inspired by the passive LCD display driver matrix, we have managed to combine the unique “CMOS under MEMS” feature of our MEMS technology with the electro-static memory effect of the MEMS into a so-called segmented passive driver array (Figure 6). The driver logic of the array consists of local low-voltage Pixel-Line Drivers (PLDs) and few global Scan-Line Drivers (SLDs). The 2D MEMS array is split into segments of PLDs implemented right underneath the MEMS devices they control. The PLDs in the segments run all in parallel resulting in refresh rates of few hundred Hertz for arrays as large as 100M pixels.

Reprogramming of the MEMS devices in each array segment is executed as follows (Figure 6-d): Each PLD sets the programming voltage to either “ON” (-2V) or to “OFF” (0V) state as required. A row of pixels is then selected using high-voltage SLD by pre-charging the scan line to 10V (considering for example 11V pull-in voltage). All other scan lines are kept at hold voltage (of 5V) that is well above the “pull out” voltage of the pixel devices (3V in this example). The hold voltage is applied to the scan lines for the whole duration of the image frame. This way a single row (scan line) of pixels is reprogrammed in each segment in parallel. Considering a single PLD takes approximately 9-times the area of a MEMS pixel, an example design of 100M-pixel array consist of 1111 segments driven by the 9 global SLDs. Each segment consists of 3333×3 PLDs programming a total of 3333×3×9 pixels (in 9 cycles). Reprogramming of the total of 9999 × 9999 pixels can reach maximum refresh rate of 750Hz. Arrays of 1M pixel (such as used in the holo modules) can be in principle reprogrammed at refresh rates of few kHz.

We have further optimized the layout of the segmented array by eliminating any optically inactive chip area (SLD and I/O circuits) - we simply reduce the number of the PLD circuits and place also all the SLD and I/O circuitry neatly underneath the MEMS array. This on one hand enables seamless packaging of the module, yet on the other reduces the maximum reprogramming rate of the array.

I/O connection from the DHG to the display sub-module, implemented using standard CMOS through-silicon via technology, can reach up to 10Gb/s with only 6-pin configuration, which guarantees more than necessary data throughput between the two integrated circuits. Simulation results also show that approximately half of the total power is used by the I/O logic, while all the PLDs used only about 5%. The example 100M pixel array running at 750Hz, implemented in standard high-voltage CMOS, dissipates only approximately 0.5W of power.
5. Prototype development

The original MEMS device architecture, described in Section 3, has been further optimized, taking into account practical limits of our current SiGe MEMS technology platform as well as our latest results from a project with similar processing constraints - MEMS nano-switch development for ultra low power applications [7]. The main goal of the optimizations has been improved design scalability towards the sub-wavelength dimensions.

The first prototype module is going to use a scaled down 1.5µm (instead of previously mentioned 1.2µm) pixels with greatly simplified mechanical structure (Figure 7): We have managed to double the critical processing dimension from previously required 150nm to more relaxed 300nm. Our latest experiments show that we can also reduce the vertical pixel displacement to about 50nm with only moderate influence on optical performance. We have considerably increases the mechanical stiffness of the cantilever, while keeping the pull-in voltage at approximately 26V. We further simplify the design using a two-electrode actuation instead of the previous 3-electrode proposal.

The fabricated modules will consist of 4M (2000×2000) MEMS devices with a total active area of 3×3mm². For demonstration purposes, we are also designing integrated driver logic providing 50Hz display refresh rate and 200Mb/s of input data rate. An early version of the prototype chip is foreseen with no driver circuitry underneath, focusing purely on proving the viability of the MEMS processing and experimental verification of their performance and reliability.
6. Conclusions

We believe that the main challenge of digital holography remains the development of suitable display technologies with wide projection/diffraction angles and high angular resolution. Due to the physical principles of holography this is only really achievable with very large numbers of sub-micron diffractive light modulators. We show that MEMS technologies have reach a state where dense integration of sub-micron electro-mechanical pixels with their driver circuitry has become feasible. Moreover, we propose a holographic display module that combines the advanced MEMS spatial light modulator with digital hologram generator in a self-contained, compact and modular package. Such modules can be tiled together in large numbers to create TV sized holographic display system. The display system can reach realistic power requirements as most of the computationally intensive operations and data transfers are distributed over the many holo modules and executed locally within the DHG and MEMS sub-modules. We are working on a prototype of our holographic module to demonstrate its feasibility. Further scaling of the system will however be required to reach the true high-definition visual quality.

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