Exploiting Beam Search Confidence for Energy-Efficient Speech Recognition

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Abstract—With computers getting more and more powerful and integrated in our daily lives, the focus is increasingly shifting towards more human-friendly interfaces, making Automatic Speech Recognition (ASR) a central player as the ideal means of interaction with machines. Consequently, interest in speech technology has grown in the last few years, with more systems being proposed and higher accuracy levels being achieved, even surpassing Human Accuracy. While ASR systems become increasingly powerful, the computational complexity also increases, and the hardware support have to keep pace. In this paper, we propose a technique to improve the energy-efficiency and performance of ASR systems, focusing on low-power hardware for edge devices. We focus on optimizing the DNN-based Acoustic Model evaluation, as we have observed it to be the main bottleneck in state-of-the-art ASR systems, by leveraging runtime information from the Beam Search. By doing so, we reduce energy and execution time of the acoustic model evaluation by 25.6% and 25.9%, respectively, with negligible accuracy loss.

I. INTRODUCTION

Nowadays, computers are immensely more powerful than 50 years ago and have become nearly ubiquitous, with more and more people having access to them. However, computer interfaces remain complicated, and most of the time, they require the user to completely focus on the computer in order to use it. Some current trends try to blur the idea of *using a computer*, by proposing systems that interact with humans in a more natural way, with interfaces that are familiar, or directly invisible, to us. In such a world of fluid human-computer interactions, the so-called *Cognitive Computing* is going to be a key component on all kind of systems.

From all the technologies wrapped under the umbrella term *Cognitive Computing*, Automatic Speech Recognition (ASR) will play a key role, becoming the next big leap in human-machine interactions. ASR is a marathon that started around fifty years ago with very high expectations, but soon faced important technology limitations, causing the progress in the field to slow down. However, with more powerful and ubiquitous computers, interest in this technology is again gaining popularity, and the industry and academia are working towards meeting the growing demand. Not long ago an important milestone was reached, when some systems were claimed to perform better than humans in specific conditions for Large Vocabulary Continuous Speech Recognition [34].

State-of-the-art ASR systems can be classified as either *Hybrid DNN-HMM* or *End-to-End (E2E)* systems. The Hybrid approach consists of a DNN-based *Acoustic Model*, followed by a *Viterbi Beam Search* to generate a word lattice with the most likely transcriptions, that is later re-scored by an RNN-based *Language Model*. To reduce the complexity of the ASR pipeline, the End-to-End solutions aim at generating a transcription from audio features by using a stand-alone DNN. However, E2E systems include a Beam Search with a Language Model (LM) to significantly improve their accuracy, as detailed in section II and therefore, despite being called End-to-End, they usually combine multiple DNNs and a Beam Search to achieve the best recognition accuracy.

In this work, we aim at improving the energy-efficiency of low-power hardware-accelerated ASR systems. To this end, we first analyze the behavior of a state-of-the-art ASR system when running on an accelerator-rich System-on-Chip (SoC). From the software perspective, the system is representative of recent proposals as it includes a DNN-based Acoustic Scoring stage [24] and a Beam Search [28]. From the hardware point of view, our baseline SoC consists of a multicore ARM CPU, a DNN accelerator [2] and a Beam Search accelerator [36]. Our results show that the DNN evaluation used for acoustic scoring is the main performance and energy bottleneck, consuming 82% of the execution time and 68.3% of the energy.

Our key ambition in this work is to improve the energy efficiency of the DNN evaluation, as it is the main performance and energy bottleneck. To this end, we take a novel approach based on the observation that not all the frames require...
the same level of precision. Figure 1 shows the number of hypotheses, a.k.a. tokens, expanded by the Beam Search at each frame of speech. As it can be seen, in some frames the decoder is very confident about the best hypothesis and, hence, the number of tokens expanded is very small, whereas in other parts of the speech the decoder is much less confident, which leads to a large number of hypotheses to be considered. Regions of speech where the Beam Search is not confident require highly accurate DNN scores to avoid discarding the correct hypothesis. However, we show in this work that regions of the speech where the search is highly confident, i.e. the number of tokens is small, do not require a high level of accuracy to make the correct choice and, hence, precision in DNN evaluation can be relaxed with negligible impact in WER.

In this paper, we present a novel technique to reduce the time and energy consumed during ASR, focusing on local real-time evaluation in low-power devices. In this technique, we leverage feedback information from the Beam Search accelerator to select the appropriate accuracy in the DNN accelerator. More specifically, for regions of the speech where the search is highly confident, the DNN is evaluated at low precision (e.g. 4 bits), whereas regions of the speech with low confidence are evaluated at high precision (e.g. 8 bits). By counting the number of tokens at each frame in the Beam Search accelerator, and comparing it with a threshold, we can decide if the level of confidence is high enough to evaluate the Acoustic Model in low precision. The threshold is computed at run-time so it automatically adapts to the particular situation. By using the number of tokens as metric of confidence and the run-time threshold, we can save 16.9 % of the energy and reduce the overall execution time by 19.6% of the complete system.

This paper focuses on energy-efficient hardware-accelerated ASR. We claim the following contributions:

- We characterize the performance and energy consumption of state-of-the-art ASR systems on an accelerator-rich SoC. We identify the evaluation of the DNN-based Acoustic Model as the main bottleneck, as it requires 82% and 68.3% of the total execution time and energy, respectively.
- We analyze the impact of reducing the precision of the DNN-based Acoustic Model in different regions of the speech. We conclude that frames with a high confidence in the search, i.e. with a small number of tokens expanded, can be evaluated at low precision with negligible impact in WER.
- We present a novel technique that dynamically selects the precision of the DNN accelerator based on the feedback information provided by the Beam Search accelerator. Our system evaluates the DNN at low precision for 50% of the frames, resulting in 19.6% reduction in execution time and 16.9% energy savings for the entire Librispeech test set.

The rest of the paper is organized as follows. Section II contains some background about the software and hardware solutions employed on ASR. In Section III we present our analysis of the ASR system with a discussion of its bottlenecks and a description of the proposed solutions to alleviate them. Section IV is a detailed description of the changes required in the hardware platform to support our technique. In Section V we describe our experimental methodology, providing some details regarding the configuration of the system and the models employed for its evaluation and Section VI contains our experimental results. Finally, Sections VII and VIII contain a brief review of the related work and the main conclusions of this work, respectively.

II. STATE-OF-THE-ART ASR

This section summarizes the state-of-the-art software and hardware solutions for ASR. First, we review the software pipeline of a modern ASR system, that is largely influenced by recent advances in deep learning. Modern ASR systems combine several DNNs used for different sub-tasks, such as Acoustic Scoring or Language Model re-scoring, with other algorithms for speaker adaptation, Beam Search, etc. Second, we describe a mobile hardware platform for real-time large vocabulary ASR, including a quad-core ARM CPU integrated with recently proposed accelerators for the most computationally demanding tasks in ASR systems.

A. ASR Pipeline

The top part of Figure 2 shows the software pipeline of a modern ASR system. The first stage is the Feature Extraction. This component first splits the raw audio signal in overlapping frames of 25 ms of speech. Next, it computes a vector of features to encode each frame, typically Mel Frequency Cepstral Coefficients (MFCC). Furthermore, it also computes an iVector (i1) for speaker adaptation. Therefore, each frame is encoded as a vector that is the concatenation of the audio features and the iVector. The objective of this representation is to expose the information that is relevant for the system in a compact manner.

The next pipeline stage is the evaluation of the Acoustic Model. This model is executed for every frame of speech. It
takes as input the acoustic features, i.e. MFCC+iVector, of one frame of speech and its neighbor frames and it computes the probability of that frame representing each of the possible sound units (referred to as sub-phonemes, or senones1) included in the model.

The state-of-the-art solution to implement the Acoustic Model consists of a DNN trained to compute senones’ probabilities, a.k.a. acoustic scores, for each input frame. Although different deep learning solutions, such as Multi-Layer Perceptrons (MLP) or Recurrent Neural Networks (RNN), have been successfully applied for acoustic scoring, a more effective approach is to use a Time Delay Neural Network (TDNN) [24]. Although the use of TDNNs for speech recognition was proposed long ago [33], they have been proven recently to improve the accuracy of state-of-the-art systems more efficiently than other approaches, such as using RNNs or introducing long contexts to an MLP.

In an E2E system, a greedy algorithm could be used to obtain a transcription from the acoustic scores computed by the Acoustic Model: it just selects the sub-phoneme with maximum score for each frame of speech and performs a simple post-processing to provide a transcription. However, this greedy decoding leads to sub-optimal WER, and accuracy is substantially improved by incorporating a lexicon and a language model by means of a beam search. For example, Google’s E2E system LAS (Listen Attend and Spell) reduces its Word Error Rate (WER) from 6.8% to 5.8% in the Librispeech dataset [22] when using a Beam Search with an LM [23]. NVIDIA’s Jasper improves its WER from 11.9% to 8.7% for the same dataset when using a Beam Search and a TransformerXL LM to re-score the likelihoods of the E2E DNN [12]. Baidu’s DeepSpeech obtains a relative improvement of 41.6% in WER when using the output likelihoods of the E2E RNN to drive a Beam Search with a 3-gram LM [1]. Finally, recent work from Facebook in E2E systems [31] also reports large improvements in WER when using a Beam Search and LM re-scoring. Therefore, the state-of-the-art solution is to use the DNN-computed acoustic scores to perform a Beam Search.

The objective of the Beam Search is to find the best path in a graph that contains all the possible sequences for the transcription, weighted by probabilities. This graph is known as the Decoding Graph and is usually generated by combining a language model with a Hidden Markov Model and a lexicon. All these models are efficiently represented through a Weighted Finite State Transducer (WFST) [19], a mathematical framework to build graphs specifically for sequence-to-sequence translation. The WFST is a type of weighted graph over which there are defined operations that allow to efficiently combine information from several models into the same graph. The use of a WFST makes it possible to merge together a lexicon and a language model into the same graph.

In order to efficiently traverse the decoding graph, an algorithm known as Viterbi Beam Search [28] is used. This algorithm obtains the less costly path, i.e., the most likely transcription, given the acoustic scores and the WFST-based decoding graph. This Beam Search algorithm works by expanding, for each frame, all the active states in the graph, named tokens. At start time, the only token in the Active Set represents a special state from the graph, denoted as Start State. For each frame of speech, each token in the Active Set is replaced by a set of new tokens corresponding to all reachable states from it, each with a weight equal to the addition of the source token weight, the traversed arc’s weight and the score obtained by the Acoustic Model for the destination state.

In order to keep the search space manageable, a Beam Width is used to discard very unlikely tokens. Hence, after expanding the tokens for a given frame, a pruning step is performed: for each token, the distance between its weight and the best token’s weight is computed and if it is larger than the Beam Width the token is discarded. Note that due to this pruning the number of alternative tokens considered for each frame may largely vary as shown in Figure 1. More specifically, for regions of speech where the decoder is highly confident only a few tokens are expanded, whereas the Beam Search expands a large number of tokens when it is less confident about the correct transcription. In this work, we exploit the degree of confidence in the Beam Search to perform a more efficient acoustic Model evaluation: we argue that precision of acoustic scores is critical when the Beam Search shows low confidence, but it can be relaxed when the decoder is highly confident.

The output of the Beam Search is a word lattice containing the most likely transcriptions for the input audio signal. At this point, the best path in the lattice could be recovered by following back-pointers with an inexpensive backtracking step. However, to further improve the WER, the word lattice is normally re-scored by using a more sophisticated language model encoded with an RNN or a Transformer Network [31].

Note that although our baseline system is a TDNN-based hybrid scheme, the ideas presented in this paper can be applied to any ASR system as long as it contains a DNN-based acoustic model capable of streaming evaluation and a beam search, which includes the vast majority of systems present in the literature.

B. Low-Power Hardware for ASR

Figure 2 illustrates the mobile SoC assumed in this work. It consists of a quad-core ARM CPU, a DNN accelerator and a Beam Search accelerator, all of them sharing the same system memory (8GB of LPDDR4). The CPU, an ARM Cortex A57, orchestrates the execution of the ASR pipeline: it prepares the datasets in main memory and issues commands to the accelerators to offload the most computationally intensive parts. Furthermore, it also runs part of the Feature Extraction.

The DNN accelerator is inspired in DianNao [2]. It consists of a command processor, local scratchpad memories and 16 Neural Function Units (NFU). The NFU contains all the units required to perform the DNN computations, including an array
of adders and multipliers, in addition to specialized units for the activation functions. The NFU is pipelined in three stages: NFU-1, to multiply the inputs by the weights; NFU-2, to add-reduce the results from NFU-1; and NFU-3, to perform the activation function. The internal memory is composed of three SRAM buffers to store weights (16KB), inputs (1KB) and outputs (1KB).

We employ the Beam Search accelerator presented in [36]. It contains specialized units to fetch from memory the required data to traverse the decoding graph: state issuer, arc issuer and acoustic likelihood issuer. The likelihood evaluation unit computes the weights of the new tokens by combining source token weight, the arc’s weight and the DNN-computed acoustic score. Finally, the token issuer maintains the list of tokens and generates the word lattice.

Regarding the on-chip memories, it includes several caches to speedup the accesses to different data (state cache of 128KB, arc cache of 256KB and token cache of 128KB) and two hash tables to track the tokens for the current frame and next frame of speech (768KB).

Each ASR component is executed on the best suited hardware. Figure 3 shows a diagram of the execution of the different components of the ASR pipeline. The extraction of the features from the audio frames is essentially composed of matrix-vector and matrix-matrix operations, so it can be executed almost exclusively in the DNN accelerator. The extraction of the iVector contains matrix-matrix operations, which can be efficiently handled by the DNN accelerator, and other operations not well-suited for DNN hardware that are executed in the CPU. The Acoustic Model DNN inference and Beam Search are computed in the DNN and Beam Search accelerators, respectively.

Although some steps in the ASR pipeline run on different hardware, they cannot be executed in parallel because each step depends on the previous one. Apart from that, we are assuming a Stream Evaluation of the input utterance, in which the frames are evaluated one by one, while the utterance is being captured by the ASR front-end; this is commonly referred to as online real-time speech recognition. Because of using an online ASR system on a hardware that runs faster than real-time, we cannot parallelize among different frames, either.

Another limitation for parallel execution of the Beam Search and the DNN accelerators is that the DNN evaluation requires a large amount of data from Main Memory. In fact, performance is mainly limited by the amount of bandwidth that it requires.

### III. Analysis of Bottlenecks

In this section we analyze the main performance and energy bottlenecks of a state-of-the-art hardware-accelerated ASR system for mobile devices. We implement the ASR pipeline described in Section II-A using Kaldi [25], a widely used framework for building speech recognition systems. Table I shows the relevant parameters of the system.

The Acoustic Model is a TDNN network, trained to receive as input a 40-dimension MFCC array concatenated with a 100-dimension iVector, complemented with a context of 21 past frames and 21 future frames. The network weights and inputs are linearly quantized to 8 bits. The output of the Acoustic Model represents the probabilities for the 6056 sub-phoneme elements or senones present in the model. The Decoding Graph is a WFST that combines a lexicon of 200k words and a 4-gram language model.

On the other hand, we execute the ASR system in the hardware platform described in Section II-B. Table II shows the parameters for the mobile SoC. We chose a low-power ARM CPU with 8GB of LPDDR4 DRAM, complemented with two accelerators: one to perform the Beam Search [36] and the other for the DNN inference [2]. All these subsystems share the same address space, are connected to the main system bus and are served by the same memory controller. The methodology to obtain execution time and energy consumption of this platform is described in Section V.
Table II: Mobile SoC parameters. Technology node is 28nm.

| ARM Cortex A57 | DNN Accelerator | Beam Search Accelerator | LPDDR4 Main Memory |
|----------------|-----------------|-------------------------|--------------------|
| Frequency 1.7 GHz | Frequency 55 MHz | Frequency 600 MHz | Capacity 8GB |
| Number of cores 4 | SRAM Buffers 1KB (Input), 1KB (Output), 16KB (Weights) | Caches 128KB (State), 256KB (Arc), 128KB (Token) | Bandwidth 16 GB/s |
| DNN Caches 32KB (L1I), 48KB (L1D), 2MB (L2) | NFUs 16 (16 MULs and 16 ADDs per NFU) | Hash Tables 768KB, 32K entries | Test clean: base q8 q4 |
|                  |                  | Likelihood Evaluation 4 FP adders and 2 FP comparators | WER test other |

Fig. 4. Breakdown for energy consumption during ASR evaluation on the mobile SoC presented in Section II-B. Chart (a) shows the energy breakdown by ASR component, where the clear bottleneck is the Acoustic Model TDNN evaluation, whereas chart (b) shows the energy breakdown among hardware components during the AM evaluation. Here, it can be seen how reads and writes from the DRAM are responsible for most of the consumed energy.

A. Bottlenecks

According to our experiments, the distribution of energy consumption among the ASR system components is as shown on Figure 4 where we can see how most of it is consumed by the DRAM memory during the DNN inference. Chart 4a shows the breakdown of the energy consumed during the evaluation of the Librispeech test set, that consists of more than five hours of speech of a large number of speakers, split by the components of the ASR pipeline. The most expensive parts are the iVector and the Acoustic Model evaluation, consuming 28.9% and 68.3%, respectively. The iVector computation is expensive in terms of energy consumption because it has to be partially executed on the CPU, running at an average power of 2.7W. Since the Acoustic Model evaluation is the main bottleneck, our target is to identify how much of that energy is consumed by each hardware component. Chart 4b shows the breakdown of the energy consumed during the Acoustic Model evaluation by the different hardware components. The DRAM memory is the clear bottleneck, consuming 85% of the energy. The rest of the energy is consumed by the CPU, which is idle during the TDNN evaluation, and the accelerators, of which the Beam Search accelerator is also idle. It is not shut off because it is beneficial to reuse its internal caches and scratchpads across consecutive frames.

Regarding the execution time, TDNN evaluation for acoustic scoring is also the main bottleneck as it takes 82% of the execution time. The Feature Extraction and the Beam Search require 14.8% and 3.2% of the execution time respectively. The mobile SoC platform meets the real-time constraints for all the utterances in Librispeech test set (more than 2k utterances and more than 5 hours of speech), achieving real-time factors of 0.05xRT on average and 0.09xRT in the worst case.

In conclusion, it is clear from these results that the TDNN is the main performance and energy bottleneck. Furthermore, we have identified that most of the energy (58.1%) is consumed because of main memory accesses during TDNN evaluation. We have measured that 99% of the memory accesses during TDNN evaluation are accesses for fetching weights. The network is too large to be kept in on-chip memory, and since we are evaluating the input frames one-by-one, we can not take advantage of temporal locality of weights for different input frames.

A well-known optimization to alleviate this bottleneck consist on pruning the network by an iterative process of removing some weights and retraining. This approach results in a sparse network, which can be significantly smaller than the dense network. However, the pruning algorithm is expensive, and the inference with a sparse network requires important changes in the DNN accelerator.

Another well-known technique to alleviate this bottleneck is aggressive DNN quantization. However, quantizing to less than 8 bits results in an important degradation in recognition accuracy, making it a bad solution. Figure 5 shows the
WER for test_clean and test_other evaluated with the TDNN acoustic model at different levels of quantization. While 8 bits results in minor accuracy loss compared to full precision, going to 4 bits increases the WER by 49% in test_clean and 61% in test_other, and if the weights are quantized to 2 bits, the system does not work, generating invalid transcriptions.

In the following sections, we show how Beam Search confidence can be leveraged to reduce energy consumption and increase performance by dynamically selecting the appropriate precision for the Acoustic Model inference.

IV. DYNAMIC DNN PRECISION

This section describes our technique to dynamically set the precision of the DNN used for acoustic scoring based on the confidence of the Beam Search. In Section III, we showed that fetching the DNN weights from main memory takes a large percentage of the total energy consumption. Furthermore, we showed that reducing DNN precision for all the frames results in a significant accuracy loss. Therefore, we take a different approach and propose to reduce the precision for parts of the speech where the confidence of the decoder is high and, hence, it does not require highly accurate acoustic scores to avoid discarding the correct hypothesis.

Determining in advance which frames require more or less precision is a challenging problem. To solve that, we propose to look at the number of tokens expanded during the Beam Search, based on the observation that a high number of tokens means that the Beam Search is not very confident about the correct transcription, whereas a low number of tokens is related with a high confidence. Figure 6 compares the WER obtained for test_clean and test_other with different percentages of frames computed at 4 bits. When the precision is reduced for frames with a low number of tokens, we can evaluate in low precision many more frames while maintaining a low WER loss, than if the frames are chosen randomly. Therefore, frames with high confidence, i.e. low number of expanded tokens, are good candidates to be evaluated in low precision in the DNN-based acoustic model. Note that when the DNN has to be evaluated, the number of tokens is already known by the Beam Search accelerator, and thus, this information can be exposed to the DNN accelerator to set the precision at run-time.

A. Threshold Computation

Our technique decides which frames of speech show high/low confidence in the decoding, based on the number of tokens expanded during the previous Beam Search step. If the evaluation of one frame results on few current hypotheses, the DNN inference for the next frame is performed in low precision. The threshold for the number of tokens is set dynamically with the goal of trying to achieve a given target percentage of frames evaluated at low precision. There are two options to set this ratio, a per-utterance ratio, meaning that each utterance will be forced to keep it; or a global ratio, meaning that the ratio will not be forced for each utterance but it will be achieved after computing a number of utterances. We have observed that a global ratio gives better results because different utterances have different precision requirements. If the threshold is set individually for each utterance, we are undermining that, and so the global WER increases.

The easiest solution for a global threshold would be to measure the number of tokens for each frame in the test set, and fix the threshold according to the desired ratio. However, we have observed that the threshold obtained with this method does not match the desired ratio of low precision frames in the test sets (Figure 7). In this figure, the train set was evaluated with high precision, then we sorted the frames according to the number of tokens expanded by Beam Search, and selected the frames at percentiles 30, 50 and 70. The number of tokens at those frames was used as threshold to evaluate test_clean and test_other and measure the ratio of frames classified for low precision. This approach to set the threshold results in a percentage of low precision frames significantly lower than in the train set. The reason is that when low precision is used, the number of tokens expanded during the Beam Search changes with respect to the case when high precision is always used, modifying the token distribution and moving the percentiles.

Figure 8 shows the cumulative frequency of frames from test_clean and test_other according to the number of tokens expanded, when the DNN is evaluated completely at 8 bits and 4 bits. In this case, the percentile 50 for the test set evaluated at 8 bits is at 883 tokens, whereas when the test set is evaluated at 4 bits, it is at 1961 tokens. It is clear from the figure that when the acoustic model is evaluated at lower precision, the number of tokens per frame increases. In other words, the overall confidence decreases when low precision is used.

We propose instead an alternative heuristic that tries to compute 50% of the frames at low precision by doing runtime adjustments to the threshold. For that, we keep a variable, \( h \), that contains the difference between the number of frames evaluated in low precision and those computed at high precision, and try to keep it at 0, by increasing or decreasing the threshold for the number of tokens.
To avoid the threshold from oscillating wildly, we define an additional variable, \( h_t \), which also contains the difference between high precision and low precision frames, but constrained to a window of latest frames. This way, we know if we need more frames at low or high precision, and also the current tendency. If we have more low-precision than high precision frames in the local window (\( h_t > 0 \)), we assume that the number of frames at low precision is increasing. If the opposite is true, i.e. \( h_t < 0 \), we assume that the number of frames evaluated at low precision is decreasing. With these values, we update the threshold (\( T_h \)) using the following formula:

\[
T_h = \begin{cases} 
T_h - \Delta & h > 0 \land h_t > 0 \\
T_h + \Delta & h < 0 \land h_t < 0 
\end{cases}
\]

(1)

When the system has evaluated more low-precision than high-precision frames and the tendency goes towards increasing low-precision frames, the heuristic decreases the threshold by \( \Delta \), so it is more difficult for frames to be classified for low precision. On the other hand, if it has evaluated less frames in low precision, both globally and in the local window, the threshold is increased, so more frames are classified as low-precision. Both \( \Delta \) and the starting value of \( T_h \) are parameters of the system. To avoid using floating point arithmetic, \( \Delta \) is an integer value, and we introduce another parameter to regulate the number of frames between consequent threshold updates.

This heuristic means that the threshold is going to fluctuate. To put the amplitude of the threshold oscillations into perspective, we can compare it with the number of tokens per frame (Figure 2). Since the oscillations in both signals are orders of magnitude apart, we can conclude that the proposed heuristic leads to a well stable threshold.

**B. DNN Accelerator**

In order to implement the described technique, we quantize the weights from the full-precision Acoustic Model into two levels (8-bit and 4-bit), which we keep stored in memory. On each frame, depending on the number of tokens expanded by Beam Search, we command the DNN accelerator to evaluate the input frame using one model or the other.

The low-precision model is half the size of the high-precision model, which results in half the time required to read the model from main memory while using the same bandwidth between the accelerator and the DRAM memory. In order to take advantage of that in the most efficient way, we modified the accelerator so it can perform computations in base precision or half precision, with the same hardware, so we can double the number of operations per cycle when operating in 4-bit mode, with very low area and power overheads over the baseline design.

The DNN accelerator now has to support two different modes of operation: base-precision and half-precision, which in this case means operating at 8 bits or 4 bits.

One of the main parameters of the accelerator is \( T_n \), which configures the number of NFUs and the NFU vector size. In the baseline design, each NFU carries out the computation of a different neuron, whereas the NFU vector size enables to compute in parallel several inputs for that neuron.

Without loss of generality, we assume a configuration of the DNN accelerator with \( T_n = 16 \), using 8-bit weights for base-precision mode and 4-bit weights for half-precision mode. Hence, during full-precision mode, the DNN accelerator computes 16 neurons in parallel, and for each of those, 16 parallel inputs. In order to do so, it receives 16 × 16 weights and 16 inputs each cycle.

For half-precision mode, however, the accelerator receives 32 × 16 weights and 16 inputs per cycle (i.e., 32 neurons are computed in parallel), that is, the size of the input buffer is the same as in the baseline design. We decided not to quantize the inputs to half-precision because we found it has an important impact on WER for a small benefit on performance. During half-precision mode, we partition each compute unit so it computes 16 inputs for 2 × 16 neurons. In this case, each compute unit would receive 2 × 16 half-precision weights and 16 base-precision inputs. In this solution, we still have to modify the multiplication units to support both base-precision (one 8-bit×8-bit multiplication) or half-precision (two 8 × 4
multiplications). However, since in half-precision mode we are computing two neurons at the same time at each compute unit, every two multiplications share the same 8-bit input operand. We design our multiplication units to either multiply two base-precision operands, or multiply two half-precision operands by the same base-precision operand. Figure 11 shows a diagram of our multiplication unit.

Since in half-precision mode each compute unit accumulates two different neurons, the add-tree must be able to perform one base-precision accumulation of 16 values, or two half-precision accumulations of 16 values each. For that purpose, we modify the adders in the tree so the transmission of the carry from one half to the other is conditioned on the mode of operation. By doing this simple modification, when the add-tree operates in half-precision mode, each adder operates as two independent adders, and thus the complete tree is unfolded in two separated trees, as shown in Figure 10.

Additionally, since we are merging different levels of precision, the bit-width of the adder units has to be carefully set in order to avoid arithmetic overflow.

C. DNN Activation unit and output buffer

The activation unit performs the neuron activation function after all the neuron inputs have been accumulated. Since this unit is only used at the end of the neuron evaluation, and the accelerator is alternating the computation of several neurons (to leverage temporal locality of inputs), there is a lot of time from one activation to the next, and thus the activation unit only requires support to serialize the output from the compute unit when operating in half-precision mode. A similar argument applies for the output buffer.

D. Beam Search Accelerator

In order to compute the threshold updates following the proposed heuristic, we introduce some modifications in the Beam Search accelerator. First, it has to count the generated tokens on each search step, and keep track of the threshold, Th, and the variables h and hl used by the heuristic. To this end, we modify the Token Issuer to include a few adders, a very small buffer for the hl window, and a register for each variable, resulting in a negligibly area overhead. With these modifications, the Token Issuer keeps track of the threshold and the number of tokens expanded during each Beam Search step. After each step, the number of expanded tokens is compared with the threshold, and the required precision is exposed to the DNN accelerator. When a new frame is captured and transformed into a Feature Vector, the DNN accelerator computes the inference for that frame in the required precision.

V. METHODOLOGY

To measure performance and energy consumption of the accelerators, we relied on cycle-accurate simulators to count cycles and usage of logic units. We model the mobile SoC platform described in Section II-B, illustrated in Figure 2. The hardware parameters for the experiments are shown in
To obtain the power values for all the logic units, we modeled them in Verilog, employing IPs from the Synopsys DesignWare Building Block IP when available, and writing the Verilog ourselves when required. To report accurate power, we employed the Synopsys Power Compiler tool, which requires a switching activity file. These activity files were obtained by simulating the Verilog designs with specific test-benches.

The SRAM memories were modeled through the modified version of CACTI [20] included in McPAT [13], whereas the DRAM memory was modeled with Micron DRAM Power model [17]. The latter requires the memory usage conditions, which we set by estimating the average read and write bandwidth required by the accelerators when operating at different frequencies.

The clock frequency for each logic unit was derived from the critical path as estimated by the Synopsis Synthesis tool from our Verilog code and the limit established by the bandwidth requirement between the accelerators and the main memory. The clock frequency for the Beam Search accelerator is constrained by the logic units, and was set to 600 Mhz whereas the frequency for the DNN accelerator is limited by the main memory bandwidth and was set to 55 Mhz. Of course, a DRAM with higher bandwidth could be used to improve the performance, but that would increase the overall system’s power and energy consumption, rendering it less attractive for low-power solutions.

To measure the CPU performance, we used a Jetson Tx1 Board from Nvidia, which contains, among other components, the ARM CPU that we are assuming for our baseline. Those tasks previously identified to run on CPU were executed on this board, while reading the internal performance counters for time and CPU energy. To ensure that the measurements were accurate, we launched the utterance evaluations one by one, making sure that the GPU was not being used, and that this process was the only one running (apart from OS tasks).

Regarding the speech corpus, we employed Librispeech [22], which is composed of 1000 hours of speech, divided in 5 sets: train, test_clean, test_other, dev_clean and dev_other. The train set, augmented with different techniques included in Kaldi, was used to train the models (see Table I), whereas test_clean and test_other, containing more than 5 hours of speech each, were used for the evaluations. The difference between both test sets is that test_other contains more challenging utterances than test_clean.

VI. EXPERIMENTAL RESULTS

In this section we evaluate the speedups and energy savings achieved by our dynamic DNN precision scheme based on Beam Search confidence. The baseline system is the mobile SoC platform described in Section II-B. It includes a multicore ARM CPU, a DNN accelerator and a Beam Search accelerator. We have implemented our scheme on top of this SoC as described in Section IV.

In order to implement our technique, the baseline accelerators require some modifications. More specifically, the DNN accelerator must support two operation modes: base-precision and half-precision, whereas the Beam Search accelerator has to compute the heuristic and maintain the threshold. These modifications, made as described in Section IV, result on an area overhead of 3.1% over the baseline accelerators, resulting on a negligible overhead over the complete platform, since the accelerators are very small when compared to the 8GB LPDDR4 or the 4-core ARM CPU. The DNN accelerator occupies an area of 0.42mm², split between buffers (25.5%), MULT arrays (62.6%) and AddTrees (11.9%), whereas the Beam Search accelerator occupies 3.34mm².

Since we keep on memory an additional DNN model (AM quantized to 4 bits), our solution incurs on memory footprint overheads. However, since the additional model is fairly small, the overall overhead is just 3.8% increase in memory footprint.

The average power of the complete system, including CPU, accelerators and external DRAM, is 1.17W (3.3% increase over the baseline), and the frames are evaluated 20x faster than real time, consuming 0.7 mJ/frame.

A. Performance Gains of Dynamic Precision AM

Since our heuristic modifies the threshold slowly, during a single utterance evaluation it does not change by a large extent, and thus, although for a long run the number of frames evaluated in low precision converges at 50%, that is not the case for individual utterances. Figure 12 shows the distribution of utterances according to the percentage of frames evaluated at low precision. Most of them fall between 40 – 60%, but a few of them evaluated at low precision more than 80% of their frames.

Figure 13 shows the savings obtained from the proposed technique compared to the evaluation on the baseline platform. Both for energy and time, three cases are plotted: the Worst Utterance, the Best Utterance and the Test Set Average. The Worst and Best utterances are chosen regarding the percentage of frames evaluated at half-precision. We can see how even for the worst case, significant savings are achieved.
By applying our technique, we can save up to 47.2% of energy and reduce the execution time up to 47.4% for the Acoustic Model evaluation on utterances where the Beam Search confidence is high for most of its frames. On average, our scheme reduces energy consumption by 25.6% and execution time by 25.8% when evaluating the complete test set.

Since the low-precision (4-bit weights) Acoustic Model network is half the size than the full-precision (8-bit weights) network, whenever a frame is evaluated at low-precision, we save half the reads from main memory. Operating at half-precision results in significant speedups for two reasons. First, the Neural Function Units (NFUs) are modified so they can operate at double throughput in half-precision mode with negligible hardware overheads. Second, the DNN accelerator is memory bound since data reuse is largely limited in TDNN networks and, hence, reducing one half of the reads from main memory results in large performance improvements. Therefore, the execution time for Acoustic Model evaluation is reduced by approximately one half during low-precision frames.

On the other hand, the reduction in energy consumption is also mostly explained by the reduction in reads from off-chip memory. As detailed in Section III, off-chip reads of the acoustic model weights are the main bottleneck of the system, contributing to 85% of the energy consumed during Acoustic Model evaluation. Another source of energy savings comes from the reduction in static energy consumed by the rest of the components during the time that the Acoustic Model is being evaluated. Since around 50% of the total number of frames are evaluated at low precision, the observed savings of around 25% in time and energy during Acoustic Model evaluation are consistent.

When we take into account the complete ASR system, the savings obtained in the acoustic model evaluation translate to an average reduction on energy consumption of 16.9% and a reduction of execution time of 19.5% (Figure 13). As discussed in Section III when the low precision acoustic model is employed, the average confidence of the Beam Search is decreased, which translates to a decrease in the performance of the Beam Search when our technique is used. Consequently, the energy and time consumed by the Beam Search is generally increased with respect to the baseline. However, even for the worst cases observed in the test sets, the benefits outperform the overheads, resulting in a net improvement in performance for all the utterances.

**B. Effect on Accuracy**

As discussed in Section III, reducing the accuracy for the Acoustic Model evaluation results in a minor degradation in the recognition accuracy when the frames for low precision evaluation are carefully chosen. Our experiments show that by using the proposed heuristic based on the number of tokens, we can compute at low precision 50% of the test sets frames incurring in less than 1% absolute WER loss for test_clean, and 2.69% for test_other.

![Energy Breakdown](a)

![Time Breakdown](b)

In order to select a target for the percentage of frames computed at low precision, we performed a sensitivity analysis, modifying the target percentage from 0% (every frame in high precision) to 100% (every frame in low precision). Figure 14 shows the relation between WER and savings. Note that the time and energy savings are proportional to the percentage of frames evaluated at low precision. If some percentage of frames, x%, is evaluated in low precision, we save around x/2% of time and energy during the DNN evaluation. The figure shows a curve with an elbow around x = 50% for both cases: test_clean, and test_other. Choosing this target grants a significant gain with negligible WER loss.

**VII. Related Work**

The field of Machine Learning has experienced an enormous growth in the last few decades, and that has been reflected in the computer architecture research, with a high number of proposals to increase the performance of Machine Learning algorithms. Since heterogeneous systems have also been gaining popularity, many of the new proposals regarding machine learning are related to accelerators for specific algorithms, being DNN acceleration a popular alternative. However, many
of the proposed accelerators focus on exploiting characteristics of specific types of networks, such as CNNs [3], [4], [6] or RNNs [7], [30], which are not a good fit for our baseline ASR system, which relies on a TDNN acoustic model [24], [26], mostly composed of fully-connected layers. Other recent works focus on high performance computing. Chen et al. [16] propose DaDianNao, a modular accelerator for DNN and CNN composed of 67.72\textit{mm}² nodes, consuming 15.97\textit{W} each. Song et al. [8] designed ESE, a DNN accelerator optimized for LSTM layers, consuming 41\textit{W} on an FPGA. This work is different because we focus on low-power on-edge computation, with tight constraints in area and power dissipation.

Regarding specific proposals for speech recognition, prior work was focused on older ASR systems, and assumed smaller vocabularies and/or acoustic models than state-of-the-art solutions as the one considered in this paper. Price et al. [27] designed a chip encompassing from Voice Activity Detection (VAC) and audio capture, to Beam Search decoding. The area of the chip is 13.18\textit{mm}², and consumes 11.27\textit{mW} (not including power from off-chip components, such as main memory, which is the main bottleneck according to our models) while running a 145k word vocabulary benchmark. On the other hand, our work focus on bigger models, including a 200k vocabulary decoding graph, and a 16.17\textit{MB} acoustic model (opposed to their 3.71\textit{MB} model) to achieve state-of-the-art accuracy.

Other proposals try to optimize a specific part using only information local to that component, for example, Yazdani et al. [36], [37] propose a Beam Search accelerator, consuming 462\textit{mW} plus the power dissipated by the GPU (between 2\textit{W} and 6\textit{W}), which is used for the Acoustic Model evaluation. Additionally, they optimize the Beam Search accelerator by performing on-the-fly composition of the WFST-based decoding graph [35]. Our work is different since our aim is not to improve the Beam Search energy-efficiency, but to leverage information known in the Beam Search accelerator to improve energy and performance of the DNN accelerator.

Another common optimization consists in exploiting computation reuse in the DNN accelerator [9], [10], [21], [29], or compressing the DNN model, e.g. via weight pruning [7], [8]. In this work, we follow a different approach. Instead of optimizing a component by exploiting local properties, we look at the system from a high-level perspective, exploiting the inter-dependencies among ASR stages. Note, however, that our proposal can still be applied on top of any of these optimizations, providing additional gains.

Earlier proposals for hardware accelerated ASR [5], [14], [18] focused on GMM based recognizers, with CMU’s Sphinx as an usual software baseline, and vocabularies with less than 100k words (e.g. 5k/20k-word Wall Street Journal, 64K-word Broadcast News,...). More recently, Tabani et. al. [32] proposed an accelerator for the PocketSphinx system, configured to decode a 130k-word librispeech-based benchmark. PocketSphinx is based on CMU Sphinx, aimed at portability. By using that accelerator (a 0.94\textit{mm}², 110\textit{mW} chip), the decoding time and energy is reduced by 5.89\textit{x} and 241\textit{x}, respectively, over a mobile GPU implementation. However, this type of systems have become less popular nowadays due to their lower accuracy. For instance, Tabani et. al. [32] report a WER of 24.14, which is much higher than current state-of-the-art systems.

VIII. CONCLUSIONS

In this work, we show how the number of tokens expanded during the Beam Search can be used to improve the performance of the Acoustic Model evaluation, the main bottleneck of ASR systems.

Following the observation that a low number of expanded tokens is related with high confidence in the partial decoding, we set a threshold on the number of tokens and evaluate in low precision the Acoustic Model for those frames falling below it. This threshold is computed in run-time by using a heuristic that guarantees that 50% of the frames will be computed at low precision.

To support this computation scheme, we modified a baseline low-power DNN accelerator, changing the array multiplication and add-tree units by specifically designed duplex units, so the accelerator can operate either in base or half precision, doubling the throughput for the low precision frames, with minimal impact on area and power. By using our proposal, the performance of the DNN-based Acoustic Model evaluation is improved by 25.9%, whereas the energy consumption is reduced by 25.6% on average for the entire Librispeech test set.

ACKNOWLEDGEMENTS

This work has been supported by the CoCoUnit ERC Advanced Grant of the EU’s Horizon 2020 program (grant No 833057), the Spanish State Research Agency under grant TIN2016-75344-R (AEI/FEDER, EU), the ICREA Academia program and the Spanish MICINN Ministry under grant BES-2017-080605.
