A hardware Markov chain algorithm realized in a single device for machine learning

He Tian\textsuperscript{1,2}, Xue-Feng Wang\textsuperscript{1,2}, Mohammad Ali Mohammad\textsuperscript{3}, Guang-Yang Gou\textsuperscript{1,2}, Fan Wu\textsuperscript{1,2}, Yi Yang\textsuperscript{1,2} & Tian-Ling Ren\textsuperscript{1,2}

There is a growing need for developing machine learning applications. However, implementation of the machine learning algorithm consumes a huge number of transistors or memory devices on-chip. Developing a machine learning capability in a single device has so far remained elusive. Here, we build a Markov chain algorithm in a single device based on the native oxide of two dimensional multilayer tin selenide. After probing the electrical transport in vertical tin oxide/tin selenide/tin oxide heterostructures, two sudden current jumps are observed during the set and reset processes. Furthermore, five filament states are observed. After classifying five filament states into three states of the Markov chain, the probabilities between each states show convergence values after multiple testing cycles. Based on this device, we demo a fixed-probability random number generator within 5\% error rate. This work sheds light on a single device as one hardware core with Markov chain algorithm.

\textsuperscript{1}Institute of Microelectronics, Tsinghua University, Beijing 100084, China. \textsuperscript{2}Beijing National Research Center for Information Science and Technology (BNRist), Tsinghua University, Beijing 100084, China. \textsuperscript{3}School of Chemical and Materials Engineering (SCME), National University of Sciences and Technology (NUST), Sector H-12, Islamabad 44000, Pakistan. These authors contributed equally: He Tian, Xue-Feng Wang. Correspondence and requests for materials should be addressed to H.T. (email: tianhe88@tsinghua.edu.cn) or to T.-L.R. (email: RenTL@tsinghua.edu.cn)
In the past decade, we have witnessed a fast growing trend in developing two-dimensional (2D) material-based devices using graphene\(^1\), MoS\(_2\)\(^2\), etc. Although the 2D material family is very large; however, limited options\(^3\) (such as graphene, hBN, MoS\(_2\), and WSe\(_2\)) exist with moderate stability in ambient conditions. The remaining 2D materials (silicene\(^4\), metallic dichalcogenides\(^5\), etc.) show rapid degradation in ambient conditions, which is a major obstacle for practical applications. A critical question is how to develop novel devices based on other 2D materials in ambient conditions. The oxidation of 2D materials is regarded as a drawback, which can introduce scattering sources and trapping centers in the forbidden band resulting in hysteresis\(^6\), fast degradation\(^7\), or even decomposition leading to loss of film altogether\(^8\). Another group of 2D crystals are numerous oxides which cover a rich variety of materials such as micas, layered Cu oxides, TiO\(_2\), layered perovskites, etc.\(^9\)-\(^10\). As 2D oxides, these crystals are less sensitive to air but they tend to lose oxygen and may react with water\(^3\). In order to obtain robust 2D oxides, direct oxidation of 2D materials for fabricating resistive memories have also been used\(^11\)\(^12\). But the electrical behaviors of these materials are similar to that of traditional resistive memories. The native oxide of 2D materials may be potentially useful as a resistive switching layer with different behaviors to traditional resistive memories—application area which has rarely been investigated.

Resistive random access memory (RRAM) shows great potential for machine learning applications due to its working mechanism involving ionic transport and hence good analogy to bio synapses\(^13\)\(^14\). However, hardware approaches in machine learning applications are mainly based on an array of RRAM devices with external electronics\(^15\)\(^16\), which require software or hardware assistance. At present, using a RRAM array\(^15\)\(^17\) can only implement or built partial algorithms (matrix multiplication and weight update). Besides, although different kinds of machine learning algorithms can be realized by software approaches, it consumes even more transistors on-chip\(^18\). The machine learning algorithm realized at a single device level remains elusive. If the learning algorithm can be realized in a single device without external electronics, the machine learning system can be extremely compact and efficient. Markov chain is one of the most important and fundamental algorithms in the field of machine learning. This algorithm has wide applications for modeling queueing systems, the internet, remanufacturing systems, inventory systems, DNA sequences, genetic networks, and many other practical systems\(^19\). For example, in DNA sequences, Markov chain is used to predict the existence of DNA bases (A, C, T, G) at certain sites\(^20\).

Here, we propose a Markov machine learning algorithm in a single device based on native tin oxide (SnO\(_x\)) of multilayer tin selenide (SnSe). The SnO\(_x\)/SnSe/SnO\(_x\) stack is a self-formed heterostructure by creating native oxide on both sides of the SnSe at room temperature (300 K), in air (21% oxygen) for 24 h. The thickness of native oxide SnO\(_x\) via transmission electron microscope (TEM) for both thin (~40 nm) and thick SnSe (~200 nm) are around 10 nm, which is a further indication of the self-limited mechanism of native oxide in SnSe. The native oxide SnO\(_x\) thickness is self-limited, which can guarantee repeatable resistance states despite different total SnSe thickness. Anomalous double set and reset processes are observed during unipolar switching. The theoretical model is also established and double set and reset phenomenon can be well understood, which can be connected to Markov chain algorithm. We also demo a single SnO\(_x\)/SnSe/SnO\(_x\) device as one core of Markov chain and the probabilities between each states show convergence values after multiple testing cycles.

### Results

**Characterization of SnSe-RRAM.** Recently, black phosphorus with orthorhombic crystal structure (Cmca space group) attracted a lot of attention due to its high mobility, anisotropy, large dispersion of bandgap by tuning layer numbers, etc.\(^21\). Meanwhile, there is another orthorhombic crystal SnSe at room temperature in Pnma space group. Its bulk form shows high-ZT factor\(^22\)\(^23\), which makes it a suitable candidate for being used in a wide variety of thermo-electrical devices. However, the 2D form of the multilayer SnSe is relatively unexplored. Here, we investigate SnSe thin films by mechanical exfoliation in ambient conditions. Figure 1a shows the orthorhombic crystal structure of SnSe. Similar to black phosphorus, SnSe has strong anisotropy due to the effective mass difference in armchair and zigzag directions. The in-plane Sn–Se covalent bonds exhibit puckered structure and the SnSe layers are bonded by weak van der Waals forces. As a result, SnSe flakes can be obtained by mechanical exfoliation. Pristine SnSe flake observed by TEM shows an interlayer distance of 1.325 nm and the diffraction image indicates a high-quality crystal structure (see Supplementary Fig. 1). The oxidized SnSe is also observed by the TEM cross-section with sandwich structure of native oxide (10 nm)/SnSe/native oxide (10 nm) (see Supplementary Fig. 2). As shown in Fig. 1b, two types of resistive memory devices are proposed based on the thickness of SnSe. For thin SnSe films (<20 nm), due to the complete SnSe oxidation in air, a conventional metal–oxide–metal device can be obtained. While for thick SnSe films, only top and bottom surfaces are oxidized and thus we can create a novel metal-oxide-SnSe-oxide–metal structure (Fig. 1b). This novel structure may have anomalous resistive behaviors and is worth exploring. The binding energy of native oxide and SnSe were analyzed by X-ray photoelectron spectroscopy (XPS). The large-area exfoliated SnSe flakes exposed in air (24 h) shows a very strong O1s peak, while the pristine SnSe sample after Ar sputtering (5 min) shows almost no O1s peak (Fig. 1c). This indicates that the native oxide is only present at the surface. Moreover, the SnSe with native oxide on the surface exhibits a noticeable double peak in Sn3d\(_{5/2}\) and Sn3d\(_{3/2}\), which corresponds to the mixture of SnO\(_2\) and SnO (Fig. 1d). The intrinsic SnSe after Ar sputtering shows a main peak of SnSe with a small reduction in the peak height of Sn. In this way, we can conclude that the native oxide is SnO\(_x\) (x = 1 or 2).

Since the thicker SnSe can form native oxide on both sides of SnSe, the SnO\(_x\)/SnSe/SnO\(_x\) heterostructure can be used as a resistive memory. A cross-bar (500 nm × 500 nm) based on bottom and top Au electrodes sandwich the SnO\(_x\)/SnSe/SnO\(_x\) heterostructure. This minimizes the effective device area and improves the device uniformity (see Methods for detail fabrication process). A typical 100 nm SnSe sample is shown in Fig. 1e. The initial SnSe is quite resistive (~100 M\(\Omega\)) due to 10 nm oxidation on both sides. After the forming at 6.7 V (see Supplementary Fig. 3) the SnO\(_x\)/SnSe/SnO\(_x\) heterostructures become conductive (~100 k\(\Omega\)). Meanwhile, the intrinsic SnSe with 40 nm thickness shows a resistance of ~500 \(\Omega\) in the vertical direction (Supplementary Fig. 4). A typical switching behavior for SnO\(_x\)/SnSe/SnO\(_x\) heterostructures is shown in Fig. 1f. There are obvious two-step upward jumps in current at 3.6 V (first-set) and 4.1 V (second-set) and two-step downward jumps at 5.0 V (first-reset) and 6.5 V (second-reset). The reproducibility has been demonstrated among more than 20 samples with the yield around 80%. Such behavior is quite different from conventional resistive memory with single set and reset process. Also our device behavior is different from complimentary resistive switches (CRS)\(^24\), which contains two antiserial RRAM devices with bipolar switching. In our device, two in-serial resistive memory devices are formed with unique two-step set and two-step reset.
Since the multi-layer SnSe material is in the middle, our device tends to operate with unipolar switching. This unique behavior (two-step set and two-step reset) cannot be realized by CRS due to the antiserial connection and bipolar switching of that device. Another fully oxidized SnSe sample with ~20 nm thickness is also fabricated (Fig. 1g). It shows a regular single set and reset at 3.5 and 4.8 V (Fig. 1h), respectively. The set and reset voltage are quite close to the value of first-set and first-reset in Fig. 1e. This indicates that the upper and lower oxide layer in the SnOx/SnSe/SnOx heterostructure sets and resets separately due to the SnSe in the middle. This is in contrast to the fully oxidized SnOx, which can form a filament as a result of only one set step as no blocking...
layer (of SnSe) is in the middle. The reverse voltage sweeps immediately after the forward sweeps can induce the unwanted set and influence the cycle to cycle reproducibility (Supplementary Fig. 5). In order to keep stable cycling performance, only single sweep from 0 to 10 V was applied to the devices.

Double set and reset behaviors of SnO$_x$/SnSe/SnO$_x$ heterostructure. The surface of SnO$_x$/SnSe/SnO$_x$ heterostructures is investigated by an atomic force microscope (AFM). The sample surface still shows atomic steps with roughness less than 1.3 nm (Fig. 2a). Such a phenomenon is drastically different from conventional native oxide (such as AlO$_x$) which exhibits an obvious
The SnO$_x$ can be regarded as an insulator where the injected electrons can easily exceed the equilibrium concentration and fill the trap states in the forbidden band. As a result, the conduction mechanism of SnO$_x$/SnSe/SnO$_x$ heterostructure can be explained by space-charge-limited current (SCLC)$^{56}$, which describes the conduction in the insulator with traps. The SCLC theory, linear dependence with voltage at low voltage ($0\,{-}\,1\, V$), as shown in Fig. 2c, is related to the Ohmic law region: $I \propto V$. When the voltage is in the range of $3.6\,{-}\,4.2\, V$, current follows a squared dependence with voltage $I \propto V^2$, which is related to Child’s law region. In this region, the free electrons exceed the equilibrium concentration in the SnO$_x$ and fill the trapped states, resulting in a large contribution to the current. When the voltage continues increasing past $4.2\, V$, the high-electrical field described by the Frenkel effect can lower the trap depth inside the SnO$_x$, and make the electrons jump out to be conducted easier, which can contribute to increasing the index factor larger than two (Fig. 2d). The other conduction mechanisms can be excluded, e.g., Poole–Frenkel (PF) emission requires a linear relationship $\ln(I/V) \propto \sqrt{V}$, and Schottky emission requires another type of linear relation $\ln(I) \propto \sqrt{V}$. The PF or Schottky emission is related to the electrode/oxide interface limited mechanism, while the SCLC indicates that the SnO$_x$/SnSe/SnO$_x$ heterostructure dominates the conduction instead of the electrode/oxide interface. Three more curves have been fitted (Supplementary Fig. 6). All of the results show similar trend of Ohmic law at low voltage bias and Child’s law at high-voltage bias, which belong to the SCLC theory. The initial resistance under low voltage is in the high-resistance state (HRS). After the first-set, the device is in the middle-resistance state (MRS). After the second-set, the device is in the low-resistance state (LRS). The HRS, MRS, and LRS distribution are shown with good uniformity (Fig. 2e). Especially, the MRS shows quite stable resistance level around $200\, k\Omega$. This proves that the MRS is a physically stable state in the SnO$_x$/SnSe/SnO$_x$ heterostructure without controlling the compliance current. The distribution of first- and second-set and reset voltage are shown in Fig. 2f. The first- and second-set are always centered at $3.0\, V$ and $4.2\, V$, respectively with Gaussian distribution. The resistive switching performance is also verified with different SnSe total thickness ranging from $75\, to\, 250\, nm$. Different thickness devices show similar first- and second-set voltage (Fig. 2g) at $3.3\,{-}\,3.6\, V$ and $4.2\,{-}\,4.3\, V$, respectively. This indicates that the oxide layer on both sides of the SnSe is dominated by the electrical conduction and the native oxide thickness is self-limited with similar thickness. Comparing to the set voltage vs. thickness in Fig. 2g, reset voltage vs. thickness (Supplementary Fig. 7) has larger voltage distributions. This is due to the dynamic and competing effects between filament growth and filament rupture during the reset process$^{37}$. Not only is the set voltage similar, the HRS, MRS and LRS are also uniform among three devices with $\pm 100\, nm$ thickness. The error bars for HRS, MRS, and LRS are calculated from 100 cycles for each device. The two-step set/reset switching behavior of SnO$_x$/SnSe/SnO$_x$ resistive memory under (f) $300\, K$ and (j) $77\, K$, respectively.

The mechanisms and simulation of SnO$_x$/SnSe/SnO$_x$ heterostructure. The set and reset mechanisms are different in unipolar devices. For the set process, the electrical field can promote the growth of the filament. There is a positive feedback process during set whereby the electrical field promotes the growth of the filament, which results in a more conductive RRAM with larger Joule heating. This in turn improves the growth of the filament and hence completes the feedback loop. For the reset process, the Joule heating can break the filament. There is a competition between the filament rupture and filament growth during the reset process. At a higher voltage, more Joule heating can break the filament, while the filament growth rate also increases. These
mechanisms were verified by reports of previous unipolar RRAM\textsuperscript{27,29}. A theoretical model is established by combing SCLC theory, tunneling effect and Joule heating effect (Fig. 3a). (More details can be found in the Methods section and Supplementary Discussion). This model is used to fit the experimental double set/reset curve to further interpret the inner mechanism of the proposed device. Following this exercise, the whole double set and reset process can be understood deeply based on this model (see Methods for details). As shown in Fig. 3b, our simulation results fit well with the experimental results, which indicates that the model is suitable for SnO\textsubscript{x}/SnSe/SnO\textsubscript{x} heterostructure. In this way, the double set and reset process can be understood by analyzing the filament growth and rupture process. For double set process, since the filament growing speed for upper and lower SnO\textsubscript{x} could not always be the same, the upper and lower layer of SnO\textsubscript{x} can be set separately. As a result, double set can happen. Figure 3c shows the simulation of filament growth process with double set, which exhibits the different growing speed of the filament during the set process. In the reset process, as the filament for the upper and lower layer cannot be always the same, the Joule heating in upper and lower layer can be different. As a result, either upper or lower layer with more Joule heating can break first. Figure 3c shows the filament length during the voltage sweep. It shows that the filament in the bottom layer grows to 10 nm first at 3.5 V, followed by the upper layer filament reaching the top electrode at 4 V. In the reset process, the filament in the upper layer breaks first followed by the lower layer. Such sequence can be further explained by the potential distribution on the filament. As shown in Fig. 3d, before the first set, the lower layer has a high potential as compared to the upper layer. As a result, the lower layers sets first. Immediately after the lower layer sets, the potential in the lower layer drops and the potential in the upper layer increases sharply. This can lead to the set process happening in the upper layer. During the reset process, the filament in the gap of the upper layer breaks first as a result of the higher applied potential $V_{l1}$. The whole double set and reset processes can be understood by analyzing the filament growth and rupture process. For double set process, since the filament growing speed for upper and lower SnO\textsubscript{x} could not always be the same, the upper and lower layer of SnO\textsubscript{x} can be set separately. As a result, double set can happen. Figure 3c shows the simulation of filament growth process with double set, which exhibits the different growing speed of the filament during the set process. In the reset process, as the filament for the upper and lower layer cannot be always the same, the Joule heating in upper and lower layer can be different. As a result, either upper or lower layer with more Joule heating can break first. Figure 3c shows the filament length during the voltage sweep. It shows that the filament in the bottom layer grows to 10 nm first at 3.5 V, followed by the upper layer filament reaching the top electrode at 4 V. In the reset process, the filament in the upper layer breaks first followed by the lower layer. Such sequence can be further explained by the potential distribution on the filament. As shown in Fig. 3d, before the first set, the lower layer has a high potential as compared to the upper layer. As a result, the lower layers sets first. Immediately after the lower layer sets, the potential in the lower layer drops and the potential in the upper layer increases sharply. This can lead to the set process happening in the upper layer. During the reset process, the filament in the gap of the upper layer breaks first as a result of the higher applied potential $V_{l1}$. The whole double set and reset

![Fig. 3](image-url) Theoretical model and simulations for SnSe RRAM. a A theoretical model for the SnO\textsubscript{x}/SnSe/SnO\textsubscript{x} heterostructure. b The simulated switching behavior showing good fit with experimental results for the two-step set and reset behavior. c The filament length vs. the voltage in the SnO\textsubscript{x}/SnSe/SnO\textsubscript{x} heterostructure. d The filament potential vs. the voltage in the SnO\textsubscript{x}/SnSe/SnO\textsubscript{x} heterostructure. e Proposed filament growth and rupture mechanism to explain the double set and reset processes.
processes are shown in Fig. 3e, and these processes are matched with the switching behavior in Fig. 3b. Our model can also simulate the double set and reset behaviors at 77 K (Supplementary Fig. 11), which is a good proof of the correctness of our model.

Markov chain properties of SnO$_x$/SnSe/SnO$_x$ heterostructure. The I–V curves indicates five major kinds of filament states (Fig. 4a) of the devices: (i) 010, (ii) 121, (iii) 020, (iv) 120, and (v) 021. The number represent the conducting filament numbers in upper or lower layers. The first, second, and third numbers
The schematic showing the definition of three Markov states and these behaviors are quite related to the initial resistance state. There are five possible filament states inside the SnSe-RRAM: (i) 010, (ii) 121, (iii) 020, (iv) 120, and (v) 021 (numbers represent the conducting filament numbers in upper or lower layers. The first, second, and third numbers represents initial, after set and after reset states, respectively). In order to reduce the complexity of peripheral designs, the five filament states have been classified into three states of Markov chain. b The typical resistive switching behavior for state I: one set and one reset (010), state II: one set and one reset (121), state I: two sets and two resets (020), state III: one set and two resets (120), and state III: two sets and one reset (021). c The relation between initial resistance and the states in 100 cycles. d The probability for each state in 270 testing steps. e The error rate between each state showing continuous decrease after more testing steps. f The Markov chain after validation. The circular with certain stage in it represents the current or next stage. The arrow line between two state represents the state transfer direction and the number near it is the state transition probability between these two states (pm). f After the filament rupture, it can result in less Joule heating as a consequence of the rupture of the first filament with larger resistance. Moreover, a higher voltage can improve the competition between the filament rupture and the filament growth. So the filament breakage of the second layer of metal–oxide film is much harder than the first layer. Figure 3c shows the simulation results of filament growth and rupture process. The two sets can happen directly due to the positive feedback of the filament formation. However, for the reset process, after the first reset, the broken filament regrows twice, which causes the overall reset process to be slower and is also a proof that there is significant competition between the filament rupture and filament growth during the reset. This is the reason why in some cases, only one reset happens, which can result in the occurrence of state-I or state-I, and state III are shown in Fig. 4b. During the classification, only resistance change larger than two times can be regarded as an effective set/reset. During the experiment, we found that the transfer between states shows Markov chain property, which means that the probability of the next state happening only depends on the current state and is irrelevant to all of the past states. As shown in Supplementary Fig. 13a, for conventional RRAM, the gap distance is only influenced by the previous reset. However, the residual filament is influenced by all the switching history. As shown in Supplementary Fig. 13b, the switching state (one set or two sets) belonging to state-I, state-II, or state-III is only influenced by the previous reset conditions. As shown in Fig. 4c, the high-initial resistance (before each cycle) in the range of 10^7–10^10 ohm can result in state-II happening with a higher probability, while state-I or state-III mainly distributes with lower initial resistance (before each cycle) below 10^7 ohm. We also noticed that partial state-I or state-III distributes with high-initial resistance, which is in agreement with the two filament structures in state-I and state-III proposed in Fig. 4a. Figure 4c indicates that the three states are quite related to the initial resistance. The states can be also justified by reading the initial states of the RRAM. The Markov property can be described as follows:

\[ P(X_{n+1} = j|X_n = i, X_{n-1} = i_1, X_{n-2} = i_2, \ldots, X_0 = i_0) = P(X_{n+1} = j|X_n = i). \]  

In order to verify Eq. (1), we investigate the frequency distribution of nine state-transfer conditions. However, this type random number generator such that a certain state appears well with our proposed single device. 

For developing / testing a practical application involving the Markov property of the device, we demo a fixed probability random number generator such that a certain state appears randomly in a large cycle number scale. Fixed-probability random numbers have vital applications in big data processing and optimization such as simulated annealing algorithm, genetic algorithm, and Monte-Carlo simulations. However, this type of random number generated by software is usually a pseudo-random number achieved by shift registers and XOR gate, which shows large periodicity and is not a true random number. As to our random number generator, it depends on the Markov property, therefore periodicity does not appear in this device. Previous reported operation mechanism of 0/1 RNG application are mainly based on random telegraph noise or set voltage
variability. For our device, RNG application is realized based on Markov chain algorithm with three values per bit. Moreover, if the bits are increasing, three numbers per bit in our devices array configuration can enable an even larger amount of random numbers compared to the two numbers “0/1” per bit in conventional RRAM devices. The states-I, -II, and -III represent random numbers 1, 2, and 3. As shown in Fig. 4g, the generated number shows random distribution.

According to the state transition diagram of our implemented Markov chain, we can obtain the transition probability matrix \( A \), which can be written as

\[
A = \begin{bmatrix}
0.433 & 0.250 & 0.317 \\
0.243 & 0.390 & 0.367 \\
0.268 & 0.446 & 0.286
\end{bmatrix}.
\]

If we define the probability of state I, II, and III as \( \pi_1, \pi_2, \pi_3 \), and the initial state is state I which is extracted from experimental results, according to the Markov probability theory, the equation group (7) must be satisfied:

\[
\begin{align*}
\pi_1 + \pi_2 + \pi_3 &= 1; \\
[\pi_1 \pi_2 \pi_3]A &= [\pi_1 \pi_2 \pi_3].
\end{align*}
\]

By solving this equation group, we can obtain three theoretical probabilities separately. In our case, the result is 0.3102, 0.3648, and 0.3250 (More details are described in Supplementary Discussion). Meanwhile, after 270 testing cycles, the frequency distribution of the three states is 0.3186, 0.3481, 0.3333, respectively. The error rate of the three states are all below 5% (Fig. 4h), which indicates that our hardware fixed-probability random number generator is highly consistent with theoretical design and can be put into practical applications. Moreover, five devices are analyzed with similar probability distribution (Supplementary Table 1). All the devices show the relation of P (state II) > P (state-III) > P (state-I), and the total discrepancy to the theoretical values are all below 4%, which prove the good uniformity of the sequence by different devices.

In order to measure the device in a faster manner, the test method based on sawtooth waves has been developed (Fig. 4i), which is similar to the concept of “pulsed operation.” When compared with pulse operation, sawtooth waves are similar to the DC sweep. In such an operation manner, SnSe RRAM has good durability up to \( 1.1 \times 10^6 \) cycles. By analyzing the total times of set and reset, the state-I, -II, and -III can be determined and random numbers can be obtained (Fig. 4j). Moreover, the error rate between each state shows continuous decrease after more testing cycles (Fig. 4k), which validates the Markov chain algorithm inside the SnSe-RRAM. For DC sweep, it will take 3 s for one sweep and the average power consumption for 270 DC sweeps is \( 3.75 \times 10^{-4} \) W. For the sawtooth waves operation, the average power consumption is \( 0.9 \times 10^{-7} \) W during \( 1.1 \times 10^6 \) cycles. The random numbers generated by our SnSe RRAM were also checked by NIST test (see details in Supplementary Discussion). The final NIST report reveals that the random numbers generated by our devices have overall good randomness and the potential to be applied in industry in the future.

In order to highlight the advance of using a single device as a fixed-probability random number generator, we also compare the hardware resources required for implementing a software approach with the same function—and the requirement is around 13,700 transistors! (see Supplementary Fig. 14). Therefore, a Markov chain (core) realized via a single device can simplify the system enormously, and open new application areas in data optimization and machine learning. For large scale integration and for making multiple Markov cores, wafer-scale SnSe films can be grown by the chemical vapor deposition method.

**Discussion**

In summary, a Markov chain algorithm is successfully built in a single RRAM device where the resistive switching layer is based on a multilayer SnSe material whose both sides develop native oxide with atomic flatness. A unique two-step set and reset behavior is observed. Numerical simulation can reproduce such unique behavior and provide a deeper understanding of the switching sequence. The three states of a Markov chain are defined based on the step number of the set and reset. Moreover, we demonstrate that the three states are only related to the current states instead of the overall history of the system, which validates the Markov chain. A fixed-probability random number generator is also demonstrated for practical applications.

**Methods**

**Device fabrication.** Bottom electrode line with 500 nm width was first patterned by e-beam lithography, followed by thermal evaporation of Cr/Au with 3/35 nm thickness. Then SnSe crystal was exfoliated on the bottom metal line by the well-known mechanical exfoliation method. After the SnSe flakes were identified by optical microscopy, another e-beam lithography followed by thermal evaporation of Cr/Au with 3/35 nm thickness and lift off was performed to fabricate the top electrodes (also 500 nm wide). In this way, a cross-bar structure (with bottom electrode) was formed. For SnSe-RRAM, the oxidation condition can be described as the oxidation at room temperature (300 K), in air (21% oxygen) for 24 h.

**XPS characterization.** The XPS spectra was collected using monochromatic 1486.7 eV Al Ka X-ray source on PHI VersaProbe II X-ray Photoelectron Spectrometer with a 0.47 eV system resolution. The energy scale had been calibrated using Cu 2p3/2 (932.67 eV) and Au 4f7/2 (84.00 eV) peaks on a clean copper plate and a clean gold foil.

**AFM characterization.** The AFM images were captured using a Bruker Dimension-Icon FastScan system.

**SEM and EDX characterization.** The micrographs were taken using the Hitachi SU8230 CFE SEM with EDX function.

**Electrical measurement.** The electrical measurement was conducted by two-point probing the top and bottom electrodes of the device in a Lakeshore cryogenic probe station with the pressure well below \( 10^{-4} \) T. Such measurement condition can exclude the influence from water and moisture, which can reveal the intrinsic behaviors of the SnSe-RRAM. Temperature dependent measurements down to 77 K were performed in the Lakeshore probe station with substrate cooling via liquid nitrogen. DC single sweep from 0 to 10 V was measured by B1500A, and up to 270 such cycles were applied. The sawtooth waves were generated by B1500A with 1542A pulse IV package.

**Numerical modeling the resistive switching in SnO2/SnSe/SnO2 heterostructures.** The theoretical model is shown in Fig. 3a where the interlayer SnSe can be regarded as series resistance without change during the switching. The initial filament length after forming are \( l_I \) and \( l_B \), respectively. There is a gap region between the filament and top electrode both for the top and bottom SnO2 layers. The gap is assumed to be physically located at the top of each filament. The set and reset process can be described by bridging or breaking the gap respectively. \( V_{gb} \) and \( V_{g} \) represent the potential on the top of the filament for upper and lower SnO2 layers, respectively. \( V_f \) and \( V_B \) represent the top and bottom potential of SnSe. Since the current flow should pass through the boundaries of the upper gap region of SnO2, upper filament region of SnO2, interlayer SnSe, lower gap region of SnO2, and the lower filament region of SnSe, therefore the equation set can be written as:

\[
\begin{align*}
I &= \frac{V - V_{gb}}{r_{SnSe}} + f \left( V - V_f, T, \alpha \left( V - V_f \right), b \right); \\
I &= \frac{V - V_{g}}{r_{SnO2}}; \\
I &= \frac{V_f - V_{gb}}{r_{SnO2}} + f \left( V_f - V_B, T, \alpha \left( V_f - V_B \right), b \right); \\
I &= \frac{V_f - V_B}{r_{SnSe}}.
\end{align*}
\]

where \( V \) is the electric potential between tunneling distance, \( T \) is the temperature, \( I \) is the electrical current, and \( r \) is the resistance. The set and reset voltages are defined as the potential difference of the adjacent two states which are in a sequence order of SnO2/SnSe/SnO2.
is the length of CF; \( R_0 \) is the resistance of SnSe. For simplification, the function \( f(V, T) \) represents the tunneling current, which can be expressed as:

\[
I = A q \frac{8 \pi m}{h_0} k T \left( \frac{\sin(\pi c_i k T)}{c_i} \right)^2 V \phi_h. 
\]  

(9a)

\[
I = 2 A q \frac{8 \pi m}{h_0^2} \phi_h \left( \frac{V}{h} \right)^2 e^{-\frac{\phi_h}{\sqrt{2m} V}}. V < \phi_h. 
\]  

(9b)

where \( A \) is the area of filament, \( m \) is effective electron mass, \( h_0 \) is Planck’s constant, and \( \phi_h \) is the barrier height with zero applied bias. The parameter \( c_i \) satisfies Eq. (10)

\[
e_i = \left( \frac{a h_0}{\sqrt{qV}} \left( \phi_h - \phi_0 - \phi_h \right)^{1/2} \right) \phi_h \phi_0, 
\]  

(10)

and the parameter \( a \) satisfies Eq. (11)

\[
a = 2 \sqrt{2m} h. 
\]  

(11)

Ion drift causes the device to experience localized heating and has an effect on the \( I-V \) property. We simplify the Joule heating as a linear process, which can be written as Eq. (12)

\[
T = T_0 + a I V. 
\]  

(12)

Using Eq. (13) to estimate the CF length at a certain time,

\[
l_1(t_0 + \Delta t) = l_1(t_0) + \frac{d}{d t} \Delta t; 
l_2(t_0 + \Delta t) = l_1(t_0) + \frac{d}{d t} \Delta t. 
\]  

(13)

the growth rate of CF is written as:

\[
\frac{dl}{dt} = 2 d V \exp \left( -\frac{q U}{k T} \right) \sinh \left( \frac{q V}{k T} \right) U_o, U_o = \frac{q V}{2(h - l)} > 0. 
\]  

(14a)

\[
\frac{dl}{dt} = s \exp \left( -\frac{q U}{k T} \right) \sinh \left( \frac{V}{k T} \right) U_o, U_o = \frac{q V}{2(h - l)} < 0. 
\]  

(14b)

Data availability

The data that support the results of this study are available from the corresponding author on reasonable request. See author contributions for specific data sets.

Received: 3 December 2017 Accepted: 18 September 2018 Published online: 17 October 2018

References

1. Novoselov, K. S. et al. Two-dimensional gas of massless Dirac fermions in graphene. Nature 438, 197–200 (2005).
2. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, J. V. & Kis, A. Single-layer MoS\(_2\) transistors. Nat. Nanotechnol. 6, 147–150 (2011).
3. Geim, A. K. & Grigorieva, I. V. Van der Waals heterostructures. Nature 499, 419–425 (2013).
4. Tao, L. et al. Silicene field-effect transistors operating at room temperature. Nat. Nanotechnol. 10, 227–231 (2015).
5. Avsar, A. et al. Air-stable transport in graphene-contacted, fully encapsulated ultrathin black phosphorus-based field-effect transistors. ACS Nano 9, 4138–4145 (2015).
6. Cao, Y. et al. Quality heterostructures from two-dimensional crystals unstable in air by their assembly in inert atmosphere. Nano Lett. 15, 4914–4923 (2015).
7. Favaron, A. et al. Photonics and quantum confinement effects in exfoliated black phosphorus. Nat. Mater. 14, 826–832 (2015).
8. Mas-Ballesta, R., Gomez-Navarro, C., Gomez-Herrero, J. & Zamora, F. 2D materials: to graphene and beyond. Nanoscale 3, 20–30 (2011).
9. Osada, M. & Sasaki, T. Two-dimensional dielectric nanosheets: novel nanoelectronics from nanocrystal building blocks. Adv. Mater. 24, 210–228 (2012).
10. Xu, M., Liang, T., Shi, M. & Chen, H. Graphene-like two-dimensional materials. Chem. Rev. 113, 3766–3798 (2013).
11. Bessonov, A. A. et al. Layered memristive and memcapacitive switches for printable electronics. Nat. Mater. 14, 199–204 (2015).
with the experiments. T.-L. Ren and H. Tian supervised the project. H. Tian, X.-F. Wang, and T.-L. Ren co-wrote the manuscript. M.A.M. revised the manuscript.

**Additional information**

*Supplementary Information* accompanies this paper at [https://doi.org/10.1038/s41467-018-06644-w](https://doi.org/10.1038/s41467-018-06644-w).

**Competing interests:** The authors declare no competing interests.

**Reprints and permission** information is available online at [http://npg.nature.com/reprintsandpermissions/](http://npg.nature.com/reprintsandpermissions/)

**Publisher’s note:** Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.