Non-Isolated High Gain Quadratic Boost Converter Based on Inductor’s Asymmetric Input Voltage

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ABSTRACT This paper introduces the concept of inductors asymmetric input voltage to derive a new high voltage gain converter. The proposed converter has continuous input, positive output, and high-power density features suitable for renewable energy applications. The operating principle, steady-state performance, practical voltage gain, small-signal analysis, and efficiency of the converter are presented in this work. A comprehensive comparison is made with the high voltage gain converters available in literature in terms of component count, voltage gain, effectiveness index, voltage and current stress on the power devices, per unit switching device rating, and other features like output polarity and availability of common ground. The proposed topology possesses a higher effectiveness index and lower switching device power rating (SDP), resulting in a good form factor. To validate the performance of the proposed converter, the experiments are conducted on the 150 W laboratory prototype, and corresponding results are presented in this work.

INDEX TERMS DC–DC converter, high voltage gain, quadratic converter, steady-state analysis, voltage stress.

NOMENCLATURE

\[ M = \text{Voltage gain.} \]
\[ \text{CCM} = \text{Continuous conduction mode.} \]
\[ \text{DCM} = \text{Discontinuous conduction mode.} \]
\[ \text{BCM} = \text{Boundary conduction mode.} \]
\[ M_{\text{CCM}} = \text{Voltage gain in CCM.} \]
\[ M_{\text{DCM}} = \text{Voltage gain in DCM.} \]
\[ D = \text{Duty ratio.} \]
\[ f_s = \text{Switching frequency.} \]
\[ T_s = \text{Switching time period.} \]
\[ S_1, S_2 = \text{Switches.} \]
\[ D_1, D_2, D_0 = \text{Diodes.} \]
\[ L_1, L_2 = \text{Inductors.} \]
\[ C_1, C_2, C_0 = \text{Capacitors.} \]
\[ V_{G1}, V_{G2} = \text{PWM pulses to switches.} \]
\[ V_{\text{in}} = \text{Input voltage.} \]
\[ I_{\text{in}} = \text{Input current.} \]
\[ V_O = \text{Output voltage.} \]
\[ I_O = \text{Output current.} \]
\[ P_O = \text{Output power.} \]
\[ \Delta i_L = \text{Peak inductor current ripple.} \]
\[ R = \text{Load resistance.} \]
\[ \text{ESR} = \text{Equivalent series resistance.} \]
\[ R_L = \text{ESR of inductor resistance.} \]
\[ R_C = \text{ESR of capacitor resistance.} \]
\[ R_S = \text{Switch on-state resistance.} \]
\[ R_D = \text{Diode forward resistance.} \]
\[ V_D = \text{Diode forward resistance.} \]
\[ \tau_L = \text{Inductor time constant.} \]
\[ \text{CIC} = \text{Continuous input current.} \]
\[ \text{PO} = \text{Positive output.} \]
\[ \text{CG} = \text{Common ground.} \]
\[ \text{SSO} = \text{Small signal analysis.} \]
\[ \text{EI} = \text{Effectiveness index.} \]
\[ \text{TVS} = \text{Total voltage stress.} \]
\[ \text{TCS} = \text{Total current stress.} \]
\[ \text{SDP} = \text{Switching device power rating.} \]
\[ 
\text{FPGA} = \text{Field programmable gate array.} 
\]
I. INTRODUCTION

The drastic climatic changes, pollution, and depletion of fossil fuels motivated the world to work towards renewable power generation and electric vehicles. The recent developments in power electronic technology have enabled opportunities for renewable energy sources to penetrate into the modern grid and load systems, as shown in Figure 1. Power electronic technology makes the cost-effective power generation for future needs as well. Due to low voltage at renewable power sources, a high gain dc-dc converter with the continuous input is required to meet the requirement of the dc bus voltage and loads [1].

Among the primary dc-dc converters, boost and buck-boost converters have the capability to increase the voltage level. However, these converters do not give high output voltage in real-time due to the presence of parasitic elements and also have high electric stress on power semiconducting devices. To increase the voltage gain, transformer-based converters are used by adjusting the turn ratio and are widely reported in the literature [2]. But these converters have setbacks due to the cost and size of the transformer. Moreover, many applications do not need electrical isolation. The widely used method to enhance the voltage gain is voltage multiplier cell (VMC) based converters [3]–[8]. These converters make use of switched-capacitor (SC) and/or switched inductors (SL) cells; these VMC cells are applied to the conventional converters to increase the voltage gain. Despite their simple structure, a relatively low power density of the converter due to usage of more components, and instantaneous overcurrent phenomenon in SC-based converters are its setbacks. However, the over-current phenomenon in switched capacitor converters can be resolved at the cost of an additional small LC resonant circuit for energy transference. Similarly, the design and size of the SL-based converters have been significant limitations. Recently, the coupled-inductor-based converters for high voltage gain have been highly reported in the literature [9], [10], yet, they suffer from leakage inductance which causes voltage spikes at the power devices. Few attempts have been made to resolve the issue of voltage spikes by using the non-dissipative clamping circuits. However, power density has been the issue due to the additional circuits for coupled-inductor-based converters.

To meet the high voltage gain requirement, quadratic converters have taken significant attention due to their practical feasibility. The quadratic converters can produce high voltage gain with a lower value of duty ratio. The family of quadratic converters is devised using the concept of component selection approach [11], reduced redundant power processing [12], flux-balance principle [13], X-Y type converters [14]. However, the voltage gain of these converters is limited, and few converters have the disadvantage of discontinuous input current, as continuous input is desired for renewable applications. In [15], a new quadratic buck-boost converter is proposed for a wide conversion ratio, but it has negative output polarity. Another quadratic buck-boost converter is proposed [16] for zero output ripple; however, this converter uses higher voltage rated capacitors and produces inverted output. A family of continuous input and continuous output enhanced gain buck-boost converters is proposed [17], but the converter has limited upper voltage gain; besides, the converters use more passive components. In [18], the high gain quadratic boost converter uses a higher component count. For increased voltage gain, a switched capacitor network is connected to the modified cascaded converter [19]. Although this converter provides the high voltage gain with continuous input, there is no common ground between input and output terminals and uses more components. A switched capacitor-inductor network-based dc-dc converter for high gain [20] uses a higher number of semiconducting power devices, and the controller design is complex as the converter order is very high. A new quadratic buck-boost converter is proposed to achieve the continuous input and high voltage gain [21]. Despite the wide conversion ratio, it has a drawback of inverted output. Recently, another quadratic buck-boost converter [22] produced a very high voltage gain with continuous input but exhibited poor power density due to more passive components (4 inductors and five capacitors).

Thus, the controller design is complex as the small-signal order of the converter is high. A new quadratic converter is introduced [23] for high gain by connecting switched capacitor cell to the single switch conventional quadratic boost converter. However, it produces high gain higher-order passive components (3 inductors and four capacitors) and lacks common ground between input and output ports.

Various attempts have been made to derive the new quadratic converters for high voltage gain. In [24], a single-switch converter is proposed by cascading the modified quadratic boost, switched capacitor, and non-inverting cell. Although the converter has high voltage gain, the poor power density due to the higher number of circuit elements and lack of common ground has been its drawbacks. A new single-switch converter with switched-inductor-network is proposed [25] for high step-up gain. However, the converter has the drawback of limited upper gain, discontinuous input current, lack of common ground, and requirement of a higher-order control circuit. A modified Luo converter for the extendable gain converter is proposed [26]; despite the high voltage gain, the converter lacks common ground between...
input and output terminals. In addition, the controller design becomes complex with the presence of three inductors and five capacitors, respectively. Recently, an active switched-inductor network-based high gain quadratic boost converter is proposed [27] with a high voltage conversion ratio, continuous input, positive output. However, it requires three active switches, and there is no common ground between input and output terminals.

In addressing the above shortcomings, in this work, the concept of asymmetric input voltage to the inductor is introduced and applied for the first time to improve the converter’s gain. In general, to get quadratic boost gain, two conventional boost converters will be connected in cascaded nature, where one converter output is fed to another converter, as shown in Figure 2(a). Here, the load side cascaded converter’s inductor experiences 2V during ON and OFF states to improve the voltage gain using the capacitor-diode cell, as shown in Figure 2(b). The converter derived has the gain of (1 + D)2 with minimum components, which is better than the existing topologies. Further, the converter has a low switching device power rating (SDP), continuous input current, positive output voltage, and higher power density. These features are much suitable for applications like renewable power generation, electric vehicles, and avionics.

II. ANALYSIS ON CONVERTERS GAIN FOR INDUCTORS ASYMMETRIC INPUT VOLTAGE

Considering the conventional quadratic boost converter, the output of the primary converter is fed to the secondary converter, as shown in Figure 2(a). The output of the primary boost converter is V_C1, which is equal to 1/(1-D) times of input voltage, V_in. The voltage across the inductor L_2 of the secondary boost converter during its ON-state and OFF-state is V_C1 and V_C1-V_O, respectively. The output of the secondary boost converter is equal to 1/(1-D) times of V_C1, and hence, the total gain of the converter is 1/(1-D)^2 times of input voltage, V_in. In this work, an attempt is made to study the impact of diverse input voltage in the ON and OFF states of secondary converter on voltage gain.

The diverse input voltage in the ON and OFF state of the secondary converter can be achieved using an additional capacitor, C_2, and diode, D_2, as shown in Figure 2(b). Here, the configuration enables the capacitor C_2 to maintain the voltage same as capacitor C_1, i.e., V_C2 = V_C1. Further, if the converter configuration supports the capacitor in aiding the input voltage to V_C1 + V_C2 (=2V_C1) across the secondary inductor L_2 of the converter during the ON state. The volt-second balance equation and the secondary converter voltage gain is given below:

\[
\begin{align*}
V_{L2} &= 0 = 2V_{C1} \cdot D + (V_{C1} - V_O) \cdot (1-D) \\
V_O &= 1 + D \\
V_{C1} &= \frac{1}{1-D}
\end{align*}
\]

Similarly, if the configuration is modified such that the capacitor C_2 aids the input voltage to V_C1 + V_C2 (=2V_C1), the total voltage across the secondary inductor L_2 of the converter during the OFF state becomes 2V_C1-V_O. The volt-second balance equation and the secondary converter voltage gain are as follows:

\[
\begin{align*}
V_{L2} &= 0 = V_{C1} \cdot D + (2V_{C1} - V_O) \cdot (1-D) \\
V_O &= 2 - D \\
V_{C1} &= \frac{1}{1-D}
\end{align*}
\]

The secondary converter gain of the conventional and gains derived in (1) and (2) at different duty ratios are shown in Figure 3. From the figure, the gain derived using capacitor-diode cell in aiding the input voltage during ON-state yields wide voltage gain as compared to the other cases. In this work, the above concept is adopted to derive a new high gain quadratic boost converter.
III. PROPOSED CONVERTER

The proposed converter shown in Figure 4 is derived utilizing diverse input voltage in the ON and OFF states of the secondary converter by integrating the diode-capacitor cell to the conventional quadratic converter. The proposed converter consists of two synchronously operated active power semiconducting switches (S1 and S2), three diodes (D1, D2, and D0), two inductors (L1 and L2), three capacitors (C1, C2, and C0), and finally, the load resistance (R). This topology supports capacitor C2 in aiding the input voltage to 2V<sub>C1</sub> across the secondary inductor L2 of the converter during the ON state.

A. OPERATION OF PROPOSED CONVERTER IN CCM

The assumptions for circuit operation are, all the components used in the circuit are ideal, the capacitors are large enough to maintain output voltage constant, and the converter is operating in continuous conduction mode (CCM). The proposed converter has two modes of operation. The power flow in Mode-I and Mode-II of the proposed converter is represented with red lines, as shown in Figure 5.

In mode-I (0 < t < DT), the two active switches will be turned on simultaneously, and the three diodes will be reversed biased. In mode-I (0 < t < DT), the two active switches will be turned on simultaneously, and the three diodes will be reversed biased. In this mode, inductor L<sub>1</sub> will be energized with the help of the input voltage source; and the inductor L<sub>2</sub> will get energized with the total voltage supplied by the capacitor C<sub>1</sub> and additional capacitor C<sub>2</sub>. The output capacitor is large enough to support the load current during this mode, and the corresponding power flow is shown in Figure 5(a). The dynamic equations of the proposed converter during mode-I are given below.

\[
\begin{align*}
\frac{v_{L1}}{v_{in}} + i_{L1} &= v_{C1} + v_{C2} + v_{in} \\
i_{C1} &= i_{C2} = -i_{L2} \\
i_{C0} &= -i_{O} = \frac{v_{O}}{R}
\end{align*}
\]

Here, the voltage across the switches, diodes, inductor, and capacitors are defined as v<sub>S1</sub>, v<sub>S2</sub>, v<sub>D1</sub>, v<sub>D2</sub>, v<sub>D0</sub>, v<sub>L1</sub>, v<sub>L2</sub>, v<sub>C1</sub>, v<sub>C2</sub>, and v<sub>C0</sub>, respectively. Similarly, the current flowing through S1, S2, D1, D2, D0, L1, L2, C1, C2, and C0 are defined as i<sub>S1</sub>, i<sub>S2</sub>, i<sub>D1</sub>, i<sub>D2</sub>, i<sub>D0</sub>, i<sub>L1</sub>, i<sub>L2</sub>, i<sub>C1</sub>, i<sub>C2</sub>, and i<sub>C0</sub>, respectively.

In mode-II (0 < t < DT), the two active switches will be turned off, and the three diodes will be in conduction as they are forward-biased. The inductors will be demagnetized, and capacitors will get charged in this mode, and the corresponding power flow is shown in Figure 5(b). The dynamic equations of the proposed. The dynamic equations of mode-II operation are given below.

\[
\begin{align*}
\frac{v_{L1}}{v_{in}} - v_{C1} &= v_{in} - v_{C2} \\
i_{C1} &= i_{C2} = \frac{i_{L1} - i_{L2}}{2} \\
i_{C0} &= i_{L2} - i_{O} = \frac{i_{L2} - v_{O}}{R}
\end{align*}
\]

The time-domain steady-state waveforms of the proposed high gain quadratic boost converter when it is operating CCM are shown in Figure 6.

IV. STEADY-STATE ANALYSIS IN CCM

This section gives the steady-state analysis of the proposed converter operating in CCM. In general, steady-state analysis refers to the derivation of the voltage gain of the converter, computation of electric stress experienced by the power devices, designing of passive components, computation of practical voltage gain, and efficiency calculations. A detailed explanation of each of the above-mentioned analysis is presented below.
A. VOLTAGE CONVERSION RATIO

From Figure 5, the voltage gain of a dc-dc converter can be derived using the volt-second balance equations of the inductors \( L_1 \) and \( L_2 \), and are given below:

\[
\begin{align*}
V_{L1} &= 0 = V_{in} - V_{C1}(1-D) \\
V_{L2} &= 0 = V_{C1} + V_{C2}D - V_{O}(1-D)
\end{align*}
\]

By solving the above equations, the steady-state voltage expression of capacitors is given below.

\[
V_{C1} = V_{C2} = \frac{V_{in}}{1-D}
\]

The equations (5), (6) help to derive the voltage conversion ratio of a proposed high voltage gain boost converter and is given below.

\[
M_{CCM} = \frac{V_O}{V_{in}} = \frac{1+D}{(1-D)^2}
\]

Similarly, the current gain of a converter can be derived by using the ampere-second balance principle of a capacitor. From (3) and (4), the expressions for average inductor current and current gain are given below.

\[
\begin{align*}
I_{C1} &= I_{C1} = 0 = -I_{L2} - \frac{I_{L1} - I_{L2}}{2}(1-D) \\
I_{C0} &= 0 = I_{L2}(1-D) - I_O \implies I_{L2} = \frac{I_O}{1-D} \\
I_{L1} &= I_{in} = \frac{1+D}{(1-D)^2} \\
M_{CCM} &= \frac{I_{in}}{I_O} = \frac{1+D}{(1-D)^2}
\end{align*}
\]

The above derived steady-state expressions will be further helpful to analyze the electric stress on power devices, design of circuit parameters, and efficiency calculations.

B. ELECTRIC STRESSES ON POWER DEVICES

The electric stress of a converter can be defined as the voltage and current stress experienced by a power semiconducting device over a switching time. It is one of the performance indices of a dc-dc converter, which is used to analyze the efficiency and reliability of a converter.

The voltage stress experienced by semiconducting power devices can be defined as the blocking voltage capability of the power device when it is in OFF state. The expressions of voltage stress of each power device can be derived from the steady-state waveforms and aforementioned steady-state equations (6)-(8), and are given below.

\[
\begin{align*}
V_{S1} &= V_{C1} = \frac{V_{in}}{1-D} \\
V_{S2} &= V_{O} = \frac{V_{in}}{(1-D)^2} \\
V_{D1} &= V_{C1} = \frac{V_{in}}{1-D} \\
V_{D2} &= V_{C2} = \frac{V_{in}}{1-D} \\
V_{D0} &= V_{C2} + V_{O} = \frac{2}{(1-D)^2}V_{in}
\end{align*}
\]

Similarly, the current capability of the power device during its conduction state is called as current stress, and can be derived as follows.

\[
\begin{align*}
I_{S1} &= (I_{L1} + I_{L2})D = \frac{2D}{(1-D)^2}I_O \\
I_{S2} &= I_{L2}D = \frac{D}{1-D}I_O \\
I_{D1} &= \frac{I_{L1} + I_{L2}}{2}(1-D) = \frac{1}{1-D}I_O \\
I_{D2} &= \frac{I_{L1} - I_{L2}}{2}(1-D) = \frac{1}{1-D}I_O \\
I_{D0} &= I_{L2}(1-D) = I_O
\end{align*}
\]

The expressions for RMS current flowing through the circuit components given in equation (11) are necessary to determine the power losses of a particular component.

\[
\begin{align*}
I_{S1,\text{rms}} &= \frac{2D}{(1-D)^2}I_O \sqrt{D} \\
I_{S2,\text{rms}} &= \frac{D}{1-D}I_O \sqrt{D} \\
I_{D1,\text{rms}} &= \frac{1}{1-D}I_O \sqrt{1-D} \\
I_{D2,\text{rms}} &= \frac{1}{1-D}I_O \sqrt{1-D} \\
I_{D0} &= I_O \sqrt{1-D}
\end{align*}
\]

C. DESIGN OF PASSIVE COMPONENTS

A dc-dc converter’s design process starts with defining the expression of a duty cycle in terms of voltage gain. By using equation (7), the duty cycle of two active power switches, \( S_1 \) and \( S_2 \), is defined as

\[
D = \frac{1 + 2M_{CCM} - \sqrt{1 + 8M_{CCM}}}{2M_{CCM}}
\]
To validate the performance of the proposed converter in continuous conduction mode, proper designing of the passive components is desired. In general, the inductors (L1, L2) and capacitors (C1, C2, and C0) values can be expressed using dynamic equations (3) and (4) and are shown below.

\[
\begin{align*}
L_1 \frac{di_{L1}}{dt} &= V_{in} \
L_2 \frac{di_{L2}}{dt} &= (V_{C1} + V_{C2}) \
C_1 \frac{dv_{C1}}{dt} &= \frac{I_1}{C_1} \
C_2 \frac{dv_{C2}}{dt} &= \frac{I_2 - I_1}{C_2} \
C_0 \frac{dv_{C0}}{dt} &= \frac{I_0}{C_0}
\end{align*}
\]  

By using the above equation (13), the value of inductors and capacitors is selected based on the given ripple specifications and the power rating of the converter.

**D. EFFECT OF NON-IDEALITIES ON VOLTAGE GAIN**

Practically, all the power electronic devices and passive components consist of some non-idealities. These non-idealities influence the performance of a converter, especially in the case of voltage gain and efficiency of the converter. The equivalent circuit of the proposed converter, including all the non-idealities shown in Figure 7, is used to analyze the practical gain and efficiency. In this figure, R_{S1}, R_{S2} are switch ON-state resistances, R_{D1}, R_{D2}, R_{D0} are the forward diode resistances, V_{D1}, V_{D2}, and V_{D0} are the forward diode voltages. R_{L1}, R_{L2} is the equivalent series resistance of inductors, and R_{C1}, R_{C2}, and R_{C0} are the equivalent series resistance of capacitors.

The effect of non-idealities on the voltage gain can be derived by applying the volt-second balance principle to the converter shown in Figure 7. The dynamic model equations during the two active switches are at ON state.

\[
\begin{align*}
V_{L1} &= V_{in} - i_{L1}R_{L1} - (i_{L1} + i_{L2})R_{S1} \\
V_{L2} &= 2V_{C1} - i_{L2}R_{L2} - (i_{L1} + i_{L2})R_{S2} - (R_{C1} + R_{C2})i_{L2} \\
&- (i_{L1} + i_{L2})R_{S1}
\end{align*}
\]

The dynamic model equations of the converter are given below when the switches are OFF and diodes are at ON state.

\[
\begin{align*}
V_{L1} &= V_{in} - V_{C2} - i_{L1}R_{L1} \\
&- \left[ \frac{i_{L1} - i_{L2}}{2} \right] (R_{C2} + R_{D2}) - V_{D2} \\
V_{L2} &= V_{C1} - V_{O} - i_{L1}R_{L1} \\
&- \left[ \frac{i_{L1} + (i_{L1} - i_{L2})}{2} \right] R_{D1} - i_{L2}R_{L2} \\
&- V_{D1} - V_{D0} - i_{L2}R_{D0} - i_{L2}(R_{D0})R_{C0}
\end{align*}
\]

By applying the volt-second balance principle to the inductors, the practical voltage gain of the proposed converter can be derived and is given below:

\[
\frac{V_D}{V_{in}} = \frac{1}{\left[ 1 - \left( \frac{V_{D1} + V_{D0}}{1} \right) (1 - D)^2 + \frac{V_{D2}}{1} (1 - D) \right]} + 1
\]

Among all the non-idealities, the equivalent series resistance of the inductor will significantly affect the ideal voltage gain, shown in Figure 8. From the figure, it is clear that the per-unit ESR of the inductor has to be less to achieve the higher voltage gain.

**E. POWER LOSSES CALCULATION AND EFFICIENCY**

The non-idealities of circuit components cause the power losses in the converter. The computation of the power losses is necessary to verify the performance of the converter in real-time applications. To simplify the analysis, the inductor current ripple and capacitor voltage ripple are neglected. The power losses of the dc-dc converter comprise the losses due to switches, diodes, inductors, and capacitors.

The power losses in the switches are due to conduction and switching losses. The on-state resistance of a switch is responsible for conduction losses, and the turn-on and turn-off times are responsible for switching losses in a power
switch. The total power switch losses are obtained as
\[ P_S = R_S * I_{S(\text{rms})}^2 + \frac{1}{2T_S} \left[ I_S(\text{peak}) * V_S * (t_{d(on)} + t_{d(off)}) \right] \]  
(17)

The power losses of two switches S1 and S2 expressed in terms of output power as
\[ P_{S1} = \frac{4D^3P_O}{(1 - D)^4} \frac{R_{S1}}{R} + \frac{DP_O}{(1 - D)(1 + D)} \left[ \frac{t_{d(on)} + t_{d(off)}}{T_S} \right] \]
\[ P_{S2} = \frac{D^3P_O}{(1 - D)^3} \frac{R_{S2}}{R} + \frac{DP_O}{(1 - D)} \left[ \frac{t_{d(on)} + t_{d(off)}}{T_S} \right] \]  
(18)

In the diode, the forward resistance and forward voltage drop are the reasons for the power losses and can be obtained as
\[ P_D = R_D * I^2_{D(\text{rms})} + V_D * I_{D(\text{avg})} \]  
(19)

The power losses of three diodes D1, D2, and D0 can be written in terms of output power as follows
\[ P_{D1} = \frac{P_O}{(1 - D)^3} \frac{R_{D1}}{R} + \frac{P_O}{1 + D} \]
\[ P_{D2} = \frac{D^2P_O}{(1 - D)^3} \frac{R_{D2}}{R} + \frac{DP_O}{1 + D} \]
\[ P_{D0} = \frac{P_O}{1 - D} \left( \frac{2P_O}{R} + \frac{2P_O}{1 + D} \right) \]  
(20)

The equivalent series resistance of passive components (inductors and capacitors) is responsible for power losses, as given in equation (21).
\[ \begin{align*}
P_L &= R_L * I^2_{L(\text{rms})} \\
P_C &= R_C * I^2_{C(\text{rms})}
\end{align*} \]  
(21)

The power losses in the inductors and capacitors are expressed in terms of output power as follows
\[ \begin{align*}
P_{L1} &= \frac{(1 + D)^2P_O}{(1 - D)^4} \frac{R_{L1}}{R} \\
P_{L2} &= \frac{P_O}{(1 - D)^2} \frac{R_{L2}}{R} \\
P_{C1} &= \frac{D(1 + 3D)P_O}{(1 - D)^4} \frac{R_{C1}}{R} \\
P_{C2} &= \frac{DP_O}{(1 - D)^4} \frac{R_{C2}}{R} \\
P_{CO} &= \frac{DP_O}{1 - D} \frac{R_{C0}}{R}
\end{align*} \]  
(22)

The total power losses of the proposed converter can be summarized as
\[ P_{\text{total}} = P_{S1} + P_{S2} + P_{D1} + P_{D2} + P_{D0} + P_{L1} + P_{L2} + P_{C1} + P_{C2} + P_{CO} \]  
(23)

The efficiency of the proposed converter can be derived with the help of output power and total power losses, as given below
\[ \text{Efficiency} = \frac{P_O}{P_O + P_{\text{total}}} \times 100\% \]  
(24)

\[ \text{FIGURE 9. Theoretical efficiency at different operating conditions.} \]

The output power is calculated using the practical voltage gain, and then the total losses are computed using equation (23). The theoretical efficiency of the proposed converter when it is operated at different duty ratios and load resistance is shown in Figure 9. The parameters considered for the efficiency analysis are \( V_{\text{in}} = 12 \text{ V}, L_1 = 0.5 \text{ mH}, L_2 = 1 \text{ mH}, C_1 = C_2 = 25 \mu\text{F}, \) and \( C_0 = 20\mu\text{F}. \) It is clear from the figure that the proposed converter has promised good efficiency over the range of wide duty ratio and load resistance.

V. DISCONTINUOUS CONDUCTION MODE

The discontinuous mode operation of the proposed converter is considered when one of the inductor currents is reached to zero value. In this section, boundary condition mode and boundary condition between CCM and DCM are also explained.

A. OPERATION OF PROPOSED CONVERTER IN DCM

The DCM of the proposed converter has three modes of operation, and corresponding time-domain waveforms are shown in Figure 10.

In mode-I \( (0 < t < DT_s) \), the two active switches are turned ON. The DCM operation is the same as CCM in this mode, and the equivalent circuit is shown in Figure 5(a). The inductor \( L_1 \) is magnetized with the input voltage source, whereas inductor \( L_2 \) is magnetized with the total voltage of capacitor \( C_1 \) and additional capacitor \( C_2 \). The currents of both inductors rise from minimum (zero) to maximum \( (I_{Lp}) \) value.

The peak values of inductor currents are expressed as
\[ I_{L1p} = \frac{V_{\text{in}}}{L_1} DT_s \quad \text{and} \quad I_{L2p} = \frac{2V_{\text{in}}}{(1 - D)L_2} DT_s \]  
(25)

In mode-II \( (DT_s < t < DT_s) \), the two active switches are turned OFF, and three diodes are forward biased as similar mode-II in CCM. In this mode, the inductor current reaches its zero value in the \( D_1T_s \) interval, as shown in Figure 10. The peak current of the inductor can be expressed in terms of \( D_1 \) as
\[ I_{L2p} = \frac{[V_{\text{in}} - V_O(1 - D)]}{(1 - D)L_2} D_1 T \]  
(26)

In mode-III \( (DT_s < t < T_s) \), the inductor currents will be zero, and all the power devices will be at an OFF state.
where \( \tau \) can be derived by further simplification of equation (29), as expressed as

\[
\tau_{L1,2} = \frac{L_1.2f_s}{R} \quad (31)
\]

From equation (8), the boundary conditions of the two inductors \( L_1 \) and \( L_2 \) of the proposed converter can be expressed as

\[
\begin{align*}
\tau_{L1B} &= \frac{D(1-D)^2}{2(1+D)}
\tau_{L2B} &= \frac{D(1-D)^2}{2(1+D)}
\end{align*}
\]

(32)

Using the above equation, the relationship between the inductor time constant and the duty ratio is plotted in Figure 12.

VI. SMALL-SIGNAL ANALYSIS

This section analyzes the low-frequency behavior and small-signal dynamics of the proposed quadratic boost converter with the help of a state-space averaging-based small-signal model. The inductor currents and capacitor voltages are considered as the state variables of the system. From the previous steady-state analysis, the capacitor \( C_2 \) is analogous to \( C_1 \) as they experience the same operating voltage and current at any time. Therefore, the system is reduced into the fourth order from the fifth order [21]. Applying the state-space averaging to the dynamic equations (2) and (3) is given below.

\[
\begin{align*}
d(\langle i_{L1} \rangle) &= \frac{V_{in}}{L_1} - \frac{\langle v_{C1} \rangle}{L_1} (1-d) \\
\frac{d}{dt} \langle i_{L2} \rangle &= \frac{\langle v_{C1} \rangle}{L_2} \left( \frac{1+d}{2} \right) - \frac{\langle v_{C0} \rangle}{L_2} \left( \frac{1-d}{2} \right) \\
\frac{d}{dt} \langle v_{C1} \rangle &= \frac{\langle i_{L1} \rangle}{C_1} \left( \frac{1-d}{2} \right) - \frac{\langle i_{L2} \rangle}{C_1} \left( \frac{1+d}{2} \right) \\
\frac{d}{dt} \langle v_{C0} \rangle &= \frac{\langle i_{L2} \rangle}{C_0} (1-d) - \frac{\langle v_{in} \rangle}{K C_0}
\end{align*}
\]

(33)

where, \( \langle i_{L1} \rangle \), \( \langle i_{L2} \rangle \), \( \langle v_{C1} \rangle \), \( \langle v_{C2} \rangle \), \( \langle v_{C0} \rangle \) and \( \langle v_{in} \rangle \) designate the averaged values of the \( i_{L1}, i_{L2}, v_{C1}, v_{C2}, v_{C0} \), and \( v_{in} \), respectively, and \( d \) indicates the duty cycle. Here, the uppercase letters of these voltages and current reference to the steady-state value of the parameter. To linearize the system, the slight deviation (denoted with cap) in these parameters is considered. However, the deviation is negligible as compared to its average value, as mentioned below.

\[
\begin{align*}
i_{L1} &= \hat{i}_{L1} + i_{L1} \\
i_{L2} &= \hat{i}_{L2} + i_{L2} \\
v_{C1} &= \hat{v}_{C1} + \hat{v}_{C1} \\
v_{C0} &= \hat{v}_{C0} + \hat{v}_{C0} \\
v_{in} &= \hat{v}_{in} + \hat{v}_{in} \\
d &= D + \hat{d}
\end{align*}
\]

(34)

B. BOUNDARY CONDITION BETWEEN CCM AND DCM

Defining the boundary conditions is necessary to understand the operating mode of a converter. Generally, the boundary condition of a converter is defined as where the peak inductor current ripple (\( \Delta i_L \)) equals twice the inductor average current (\( i_L \)). The normalized inductor time constants can be defined as

\[
\tau_{L1,2} = \frac{L_1.2f_s}{R} \quad (31)
\]

FIGURE 10. The time-domain waveforms of the converter in DCM.

FIGURE 11. Mode-III operation in DCM.

The output capacitor feeds the load current; the equivalent circuit of the proposed converter in this mode is shown in Figure 11. By using the equations (25) and (26), the \( D_1 \) can be represented as

\[
D_1 = \frac{2V_{in}D}{V_{in} - V_O(1-D)} \quad (27)
\]

The average output capacitor current, \( I_{C0} \), value can be expressed as

\[
I_{C0} = \frac{1}{2} D_1 I_{L2p} - I_O \quad (28)
\]

Substituting the equations (26) and (27) in (28), then, \( I_{C0} \) can be expressed as

\[
I_{C0} = \frac{2 V_{in}^2 D^2 T_S}{[V_{in} - V_O(1-D)](1-D) L_2} - I_O \quad (29)
\]

The voltage gain of the proposed converter in DCM, \( M_{DCM} \), can be derived by further simplification of equation (29), given below.

\[
M_{DCM} = \frac{1}{2(1-D)} \left[ 1 \pm \sqrt{1 + \frac{4D}{\tau_{L2}}} \right] \quad (30)
\]

where \( \tau_{L2} \) is the inductor \( L_2 \) time constant, it is equal to \( \frac{L_2 f_s}{2R} \).
where,

\[
\begin{align*}
G_{vo}(s) &= \frac{\dot{V}_o}{\dot{V}_{in}} \\
&= \frac{A_1}{B_1s^4 + B_2s^3 + B_3s^2 + B_4s + B_5} \\
G_{vd}(s) &= \frac{\dot{V}_o}{\dot{d}} \\
&= \frac{A_2s^3 + A_3s^2 + A_4s + A_5}{B_1s^4 + B_2s^3 + B_3s^2 + B_4s + B_5}
\end{align*}
\]  

(35)

where,

\[
\begin{align*}
A_1 &= R(1 + D)(1 - D)^2 \\
A_2 &= -2RL_1L_2C_1I_L \\
A_3 &= 2RL_1C_1(1 - D)(V_{C1} + V_{C2}) \\
A_4 &= -RL_1(1 + D)(1 - D)(I_L + I_{L2}) \\& \quad -RL_2(1 - D)^2I_{L2} \\
A_5 &= RL(1 - D)^3(V_{C1} + V_{C2}) \\& \quad +V_{C1}(1 + D)(1 - D)^2 \\
B_1 &= 2RL_1L_2C_1C_2 \\
B_2 &= 2L_1L_2C_1 \\
B_3 &= 2RL_1C_1(1 - D)^2 + RL_2C_2(1 - D)^2 \\& \quad +RL_1C_2(1 + D)^2 \\
B_4 &= L_1(1 + D)^2 + L_2(1 - D)^2 \\
B_5 &= R(1 - D)^4
\end{align*}
\]  

(36)

By using the above equations, the small-signal dynamic behavior of the proposed converter can be analyzed. It is clear from equation (35) that the proposed converter has three right-hand side zeros, making the proposed converter a non-minimum phase system. However, the system poles are located at the left side of the s-plane, which means the proposed converter is stable. The frequency response of the proposed converter is analyzed with the help of a bode plot of derived transfer functions, as shown in Figure 14.

VII. COMPARATIVE ANALYSIS

This section compares the proposed quadratic boost converter with other high voltage gain converters available in the literature. The comparison is in terms of the voltage gain, steady-state electric stresses on circuit components, switching device power rating, and other features.

Figure 15 shows the comparison of proposed converter voltage gain with a quadratic buck-boost converter [16], the enhanced gain buck-boost converter [17], a new quadratic following boost converter [18], a negative output buck-boost converter [15], a continuous input quadratic buck-boost converter [21], and a switched capacitor-inductor network-based boost converter [20], a high gain quadratic buck-boost converter [22], a switched capacitor cell extended modified cascaded converter [19], and single-switch high gain quadratic
boost converter [23]. Figure 15 shows that the proposed converter has a higher voltage gain than other converters except for the converter in [22]. Although the converter in [22] has better voltage gain, it uses a higher number (fourteen) circuit components. The effectiveness index (EI) is another performance index that is measured by taking the ratio of voltage gain and the total number of components used in the converter and is used to evaluate the power density of the power electronic converter [22]. From Table 1, the EI is calculated at different duty ratios for all the high gain converters and is depicted in Figure 16. From the figure, the proposed converter has the highest effectiveness index compared to the remaining converters due to the capability to produce the highest voltage gain with the lower number of circuit components.

The detailed steady-state performance comparison is given in Table 1. To improve the efficiency and reliability of the converter, the electric stresses on the power devices have to be a minimum. Understandably, the voltage stress across the output switch S2 and diode D0 of the proposed converter is high due to its high voltage output with a lower number
TABLE 1. Comparison of various high gain quadratic converters.

| Topology | [16] | [17] | [18] | [15] | [21] | [20] | [22] | [19] | [23] | Proposed Converter |
|----------|------|------|------|------|------|------|------|------|------|-------------------|
| Switches | 2    | 2    | 2    | 2    | 2    | 5    | 2    | 2    | 2    | 2                |
| Diodes   | 2    | 2    | 3    | 2    | 3    | 4    | 3    | 4    | 3    | 3                |
| Inductors| 2    | 3    | 2    | 2    | 2    | 2    | 4    | 3    | 3    | 2                |
| Capacitors| 2   | 3    | 3    | 2    | 3    | 4    | 5    | 4    | 4    | 3                |
| Total    | 8    | 10   | 10   | 8    | 10   | 11   | 14   | 12   | 12   | 10               |

Voltage gain (V_{o}/V_{a})

\[
\frac{D}{(1-D)^2} \frac{D^2}{(1-D)^2} \frac{1-D+D^2}{(1-D)^2} \frac{(D-2-D)}{(1-D)^2} \frac{2-D}{(1-D)^2} \frac{2D(2-D)}{(1-D)^2} \frac{(D+1)}{(1-D)^2} \frac{1+D}{(1-D)^2} \frac{1+D}{(1-D)^2}
\]

Voltage stress on switch (V_{o}/V_{a})

\[
\frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2}
\]

Voltage stress on diode (V_{o}/V_{a})

\[
\frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2}
\]

Current stress on switch (I_{o}/I_{a})

\[
\frac{D^2}{(1-D)^2} \frac{D^2}{(1-D)^2} \frac{D}{(1-D)^2} \frac{D}{(1-D)^2} \frac{1}{(1-D)^2} \frac{2}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2}
\]

Current stress on diode (I_{o}/I_{a})

\[
\frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2} \frac{1}{(1-D)^2}
\]

CIC: √ √ √ √ √ √ √ √ √ √
PO: × √ √ × × √ √ √ √ ×
CG: √ √ √ √ √ √ √ √ √ ×
SSO: 4 6 5 4 4 5 9 6 6 4

\[p.u.SDP = \frac{1}{P_O} \sum_{i=1}^{n} V_{si}I_{si} \] (37)

V_{si} and I_{si} are the voltage and current stress of the power device, respectively, and ‘n’ is the total number of power devices present in the converter. The SDP of the proposed converter and other high gain converters can be calculated with the help of Table 1.

The per-unit SDP comparison of the proposed converter and other converters is plotted and shown in Figure 18. The figure shows that the per-unit SDP is lower than a few other converters despite its high voltage gain capability. In addition, the proposed converter gives the positive polarity output along with continuous input current and is very much essential for renewable energy and electric vehicle applications.

VIII. EXPERIMENTAL VERIFICATION

To validate the performance of the proposed high gain quadratic boost converter, experiments are conducted on...
TABLE 2. Experimental specifications.

| Parameter         | Specifications               |
|-------------------|------------------------------|
| Input Voltage     | 12 V                         |
| Inductors         | L₁ = 0.5 mH and L₂ = 1 mH    |
| Capacitors        | C₁ = C₂ = 24 μF and C₃ = 20 μF|
| Load Resistance   | 100 Ω                        |
| Output Power      | 150 W                        |
| MOSFET            | IRF 540                      |
| Diode             | MUR 860                      |
| Optocoupler       | HCPL 3120                    |
| Switching Frequency| 50 kHz                     |

The 150 W laboratory prototype, which is shown in Figure 19. The schematic of the hardware implementation of the control circuit of the proposed converter is given in Figure 20. The PWM pulses for two synchronously operated active switches are generated with the SPARTAN 6 FPGA controller. The HCPL 3120 optocoupler-based driver circuit is used to drive the switches and to isolate the control circuit from the power circuit. The corresponding experimental specifications are given in Table 2.

Figure 21 shows the experimental waveforms of the proposed high gain quadratic boost converter considering the load resistance of 100 Ω. Figure 21(a) shows the input voltage, capacitor C₁, output, and input inductor L₁ current. The input voltage of 12 V is applied to the converter and is operated at the 0.5 duty ratio. As per equations (5) and (6), the capacitor C₁ voltage, the output voltages are 24 and 72 V, respectively. From Figure 21(a), the experimental values are 23 and 69 V, respectively. The deviation between the theoretical and experimental values could be due to the non-consideration of contact and soldering resistance. Figure 21(b) shows the capacitor C₂ voltage, and the diode D₂ voltages. The voltage across capacitors C₁ and C₂ are equal. The measured S₁, D₁ voltages, and S₂, D₂ voltages are shown in Figure 21(c) and Figure 21(d), respectively. From the figure, the measured values are in agreement with the theoretical findings. The inductors currents are depicted in Figure 21(a) and Figure 21(d); it is clear that measured inductors (L₁ and L₂) current and its ripple are in the specified design limits.

Further, the dynamic response of the proposed converter for the change in input voltage, duty ratio, and load is shown in Figure 22. In this figure, initially, the converter is operated at 10 V of input voltage, 0.4 duty ratio, the load resistance of 100 Ω, and corresponding output voltage and current are 60 V and 0.6 A, respectively. Then, the input is changed from 10 V to 12 V at 1.5 seconds. At this point, the output voltage is changed from 60 V to 70 V, and the load current is changed from 0.6 A to 0.7 A. Then, the duty ratio is changed to 0.5 from 0.4 at 3 seconds, and the input voltage is kept constant at 12 V; then, the output voltage is changed to 46 V from 70 V, and the load current has changed to 0.46 A from 0.7 A. Further, the load resistance has changed from 100 Ω to 75 Ω at 4.5 seconds; the output voltage remains constant and equal to 46 V.

The experiments were performed to obtain the practical voltage gain at different duty ratios and are compared with...
ideal and non-ideal theoretical voltage gain calculated using equations (6) and (16), respectively. The voltage gain comparison is given in Figure 23; the practical voltage gain is very close to the non-ideal theoretical voltage gain and validates the superiority of increased input voltage contribution across the inductor even asymmetrically.

The experimental efficiency of the proposed high gain quadratic boost converter is measured. The converter operates at different power ratings by varying the duty ratio for fixed load resistance shown in Figure 24. The figure shows that the proposed converter efficiency is poor at lower duty cycles and is maximum at 0.5 duty ratio. Beyond the 0.5 duty ratio, an increase in duty cycle leads to a decrease in efficiency due to the higher value of load currents. The breakdown of power losses in the circuit components of the proposed converter is shown in Figure 25. The efficiency and power losses are measured when the proposed converter is operated at 12 V input voltage, 0.5 duty ratio, and load the resistance of 100 Ω. The figure shows that the diodes contribute significantly to losses compared to other components and proposed converter promising efficiency.

IX. CONCLUSION
This paper illustrates the advantage of utilizing inductors’ asymmetric input voltage for the first time, and the concept is adopted for developing a new high gain quadratic boost converter. The steady-state and small-signal analysis of proposed converter exhibits the features of reduced electric stress and good dynamic response, respectively. A comprehensive comparison of the proposed converter has shown promising superiority in terms of voltage gain, effectiveness index, the total voltage stress on power devices, per-unit SDP. In addition, the proposed converter has continuous input, provides the positive output and common ground; therefore, the converter is well suited for renewable energy generation, electric vehicles, avionics, and dc microgrid applications. Moreover, the proposed methodology can be further investigated to derive new high gain dc-dc converters.

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