Novel silicon drift detector design enabling low dark noise and simple manufacturing

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ABSTRACT: The Silicon Drift Detectors (SDDs) have replaced simple diodes in demanding X-ray fluorescence applications like in element analysers capable of detecting light elements. The reason for this is that with similar collection area the SDDs have a much smaller output capacitance than diodes due to a much smaller anode size. Thus the SDDs provide much better Signal to Noise Ratio (SNR) at smaller signal levels than diodes. The small capacitance in SDDs is achieved by placing concentric rings around a miniature sized anode. These rings are biased such that inside the SDD’s fully depleted bulk a radial electric field component is established guiding signal charges towards the anode.

Problems complicating the design of SDDs are positive oxide charge and interface dark noise. The latter is caused when leakage current generated at depleted interfaces mixes with the signal charge. It has been shown previously that by utilizing a chain of resistors connected to SDD’s p+ drift rings and intermediate n+ rings both of these problems can be solved but the resistor chain arrangement requires an additional process step, which may not be standardly available. The interface generated dark noise and the requirement for a resistor chain can be removed by implementing suitable gaps in the p+ rings or with a resistive spiral as well as by implementing an additional anode for the collection of interface leakage current. Such SDDs are, however, vulnerable to accumulation of positive oxide charge complicating the manufacturing and likely reducing the effective lifetime of the detector.

We present an SDD design comprising a novel ring arrangement preventing the formation of interface dark noise, being resistant to positive oxide charge, and removing the need for a resistor...
chain. In this work the design and operation principle of the proposed SDD is presented. The operation of the proposed SDD has been evaluated on TCAD with cylindrically symmetric 3D process and device simulations.

**KEYWORDS:** Solid state detectors; X-ray detectors; Radiation-hard detectors; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc)
1 Introduction

The Silicon Drift Detector (SDD) was introduced first in 1984 by E. Gatti and P. Rehak [1]. The first satisfactory working devices were built in a collaborative effort by J. Kemmer at the Technical University of Munich, the Max Planck Institute in Munich, and the inventors (Rehak et al.) in 1985. They made the observation that the capacitance of the device is independent of the detector area, so that “very large area radiation detectors or photodiodes using this principle may have much improved noise performance when compared to traditional diode detectors”. The first circular SDD, optimized for energy rather than position measurement, was described in 1985 by Rehak and Gatti et al. [2].

The early drift detectors used drift rings on both sides of the detector to produce the radial field. In 1987, Kemmer [3] introduced a design using a planar doping on one side and drift rings on the opposite side only. Such an SDD was easier to manufacture and provided a thin, unstructured homogeneous dead layer on the entrance side (backside radiation entry window). The manufacturability was further improved by introducing punch through biasing of the backside layer [4] removing the need to place a contact on the backside of the detector.

There are two basic problems related to the drift detectors which are the interface generated dark noise and positive oxide charge. Both of these problems can be removed with the SDD of figure 1 wherein a resistor chain arrangement is utilized for biasing the p+ drift rings and intermediate n+ rings. This biasing configuration ensures that the n+ rings are always reverse biased when compared to the neighbouring p+ rings. The n+ rings collect the interface generated electrons. The proper biasing of the n+ rings prevents electron injection from the n+ rings into the substrate as well as hole current flow from one p+ ring to another. The latter feature ensures proper operation of the resistor chain and the former one prevents the formation of interface generated dark noise. Important design aspects are the separation of the p+ rings, the size of the n+ ring, the voltage drop across individual resistors, the resistivity of the substrate, and to some extent also the amount of positive oxide charge. Particularly, a relatively large reverse bias must be applied between the n+ and the neighbouring p+ rings in order to prevent electron flow from the n+ ring to the substrate as well as hole flow from one p+ ring to another.
In addition in the SDD of figure 1 it is important to utilize a large enough reverse bias between the innermost p+ ring and the n+ anode for three different reasons. Firstly, it is important to prevent punch-through hole current flow from the innermost p+ rings to a backside p+ layer. Secondly, it is important to avoid radiation-induced electrons being absorbed by the innermost n+ rings. Thirdly, the relatively high reverse bias between the n+ and p+ rings results in an undulating potential profile reaching relatively deep inside the substrate causing problems close to anode where radiation-induced electrons are transported relatively close to the front surface. With the aid of a large enough reverse bias between the anode and the innermost p+ ring the radiation induced electrons can be pushed next to the anode deeper into the substrate wherein the undulating potential profile has no effect.

Another procedure to mitigate problems related to undulating potential profile next to anode is to utilize a larger drift field (i.e. higher potential difference between adjacent p+ rings) close to the anode than in areas located further away from the anode. Directly beneath the anode the high reverse bias between the innermost p+ ring and the anode complicates the vertical transport of the radiation-induced electrons towards the anode, which can be overcome by providing a large enough anode.

The relatively high reverse bias between the p+ and n+ rings means that the dead volume, i.e. the region from which the n+ rings collect radiation induced electrons, reaches relatively deep into the high resistivity substrate (roughly to the width of the n+ ring) resulting in the formation of a relatively large low drift field region at the border of the dead volume underneath the n+ rings. This fact increases the amount of split events enlarging somewhat the Full Width at Half Maximum (FWHM) of the X-ray peaks except for low energy X-rays. In a split-event an X-ray is absorbed in the low drift field region and part of the X-ray induced electrons are collected by an n+ ring and another part by the anode. Before the introduction of the large area radiation entry window on the backside [3] the relatively large low drift field region at the front side corresponding to gaps in the p+ doping used to increase somewhat also the FWHM of higher energy X-rays beside severely impairing the FWHM of low energy X-rays.

By reducing the separation between the p+ rings problems related to the undulating potential profile and the dead volume could be mitigated. This means, however, that inside the substrate there is a higher risk for punch-through current flow from one p+ ring to another unless reasonably high reverse bias is applied between the n+ ring and the neighbouring p+ rings. On the other hand, in case the separation between the p+ rings is reduced the width of the n+ rings should be also diminished but this is challenging from manufacturing point of view in case contact aligner is utilized in the manufacturing process.

A fact is that the X-rays and high-energy particles increase the amount of positive oxide charge. The bigger the amount of positive oxide charge is and the larger the reverse biases between the n+ and p+ rings as well as between the anode and the innermost p+ ring are, the larger is the maximum electric field value at the interface. If the maximum electric field at the interface exceeds a certain manufacturing process dependent limit then avalanche breakdown is resulted in limiting the lifetime of the detector. Thus the SDD structure of figure 1 needs to be designed and manufactured carefully in order to guarantee long lifetime in X-ray and/or particle detection applications. One way to reduce the effect of the build-up of positive oxide charge is to utilize a large area p spray implant on the front side of the SDD.
In the SDD of figure 1 an extra process step is required for the realization of the resistor chain that may not be standardly available in the manufacturing facility. The resistor chain (as well as the n+ rings) can be avoided in the SDD of [5] wherein the p+ drift rings comprise gaps as depicted in figure 9 in [5]. The positive oxide charge in these gaps enables the formation of electron “rivers” next to the interface, i.e., due to the positive oxide charge there is a potential minimum for electrons at the oxide interface in the gaps of the p+ drift rings as well as in between adjacent p+ drift rings. The gap in the p+ drift ring allows interface generated electrons to move in these electron “rivers” towards an additional anode situated in between the two innermost p+ drift rings (the innermost p+ drift ring does not comprise a gap). The additional anode collects all the interface-generated electrons except the ones generated in between the anode and the innermost p+ drift ring reducing thus very much the interface generated dark noise.

The interface and part of bulk generated holes are collected by the p+ rings and are transported from one p+ ring to another towards the outermost p+ ring in electron potential barriers located underneath the space in between adjacent p+ rings, i.e., the punch-through effect between the p+ drift rings can be exploited since there is resistor chain. The formation of afore said electron potential barriers depends on the amount of positive oxide charge, on the separation between the p+ drift rings, and on substrate doping concentration. As already previously explained the barriers prevent also interface-generated electrons from flowing into the substrate if they can be removed e.g. with afore said “electron river” approach.

The benefits of the SDD design of [5] are that no resistor chain is required, that the dead volume is smaller, and that the undulating potential profile underneath the rings is less severe than in the case of the structure presented in figure 1. The design of [5] is, however, highly dependent on the amount of positive oxide charge in the gaps piercing the p+ drift rings and in between the p+ drift rings. This is likely to complicate the manufacturing, to lower the yield, and to reduce the effective lifetime of the detector.

Instead of using gaps in the p+ rings one could alternatively use a p doped spiral wherein the p spiral itself acts as a resistor providing thus a potential gradient inside the p ring and consequently also outside the p spiral. In this design the interface generated electrons are flowing at the interface next to the p spiral towards an additional anode collecting interface-generated electrons. The benefit of the design is that the resistor chain is avoided but on the other hand the design is very much dependent on the amount of positive oxide charge at the interface next to the p spiral. Consequently further away from the anode the radiation-induced electrons would flow radially towards the anode but close to the anode, depending on the amount of positive oxide charge, the radiation-induced electrons would be prone to follow a spiral path. Since the build-up of positive charge during manufacturing and in use cannot be well controlled and since this spiral device is highly dependent on positive oxide charge the design is likely to have manufacturing issues, low yield, and reduced lifetime.

The novel SDD structure presented in section 2 prevents the formation of interface generated dark noise, is not sensitive to the amount of positive oxide charge, avoids the use of a resistor chain, enables simple manufacturing with standard process steps, does not suffer from an undulating potential profile inside the substrate, and is insensitive to the width of the rings.
Figure 1. A typical SDD ring arrangement utilizing a resistor chain for the biasing of the p+ and n+ rings. The p+ rings act as drift rings and collect interface generated and radiation-induced holes. The purpose of the n+ rings is to collect interface generated electrons.

2 Modified silicon drift detector structure

The cross-section of the SDD ring structure and anode of the proposed modified SDD structure is presented in figure 2 excluding the edge area. The front side of the modified SDD is presented in figure 3 comprising also a possible edge configuration. In figure 3 the n+ area in the upper left corner is used for contacting a neutral area next to the detector edge and the p+ area in the lower left corner is used for contacting the backside p+ area via punch-through effect. The cross-section of the other half of the modified SDD equipped with a standard edge configuration is presented in figure 4. The leftmost n+ node (at V6) contacting the neutral area next to the detector edge is biased at a slightly more positive potential than the potential would be in case the neutral area would be floating. In this manner the edge generated electrons are collected by the leftmost n+ node and not by the n+ anode (at V5), i.e., there is no edge generated dark noise, while at the same time the depleted edge area and thus the edge generated leakage current will be kept at a relatively small level.

In figure 5 an alternative edgeless detector configuration [6] optimised for pixelated detectors is presented avoiding the formation of edge-generated electrons. The edge is covered with insulator and conductor layers and by biasing the conductor layer at a sufficiently low potential an inversion layer of holes is realised beneath the insulator layer preventing the formation of interface generated dark noise and enabling the biasing of the backside p+ layer.

Figure 2. Schematic cross-section of the novel modified SDD.
Figure 3. Schematic layout of the SDD structure including also the edge area. The cross-section of the area comprising the SDD rings is presented at figure 2. In the upper left corner of the detector chip there is an n+ node contacting a neutral area next to the detector edge (see also figure 4 and corresponding explanation). In the lower left corner of the detector chip there is a p+ node for punch-through biasing of the backside p+ layer.

Figure 4. A modified SDD structure comprising a standard edge design. SDD operation is established by biasing properly the nodes at $V_1$, $V_2$, $V_3$, and $V_5$. The potential at the second outermost p+ ring (at $V_4$) is monitored in order to avoid electric break down. The n+ node (at $V_6$) contacting the neutral area next to the detector edge is biased at a slightly more positive potential than the potential would be in case the neutral area would be floating.

As usual on the backside of the modified SSD in figure 2 there is a thin large-area p+ type doping functioning as a homogeneous radiation entry window which is preferably biased from the front side with the punch through biasing scheme [4]. On the front side of the device there is a large area deep low dose n type implanted layer and a large area shallower and higher dose p type implanted layer. These n and p type large area layers are preferably implanted with the same mask.
Figure 5. An edgeless modified SDD structure comprising an insulator conductor stack at the detector edge. A sufficiently negative potential on the conductor layer (at \(V_6\)) results in an inversion (or accumulation layer) of holes at the interface beneath the insulator preventing the formation of interface generated dark noise and enabling the biasing of the backside p+ layer.

Besides on the front side there are alternative p+ and n+ type rings surrounding the anode. The n+ rings act as gates of very large concentric JFETs (Junction Field Effect Transistor). The p+ rings act as sources and drains of the very large concentric JFETs — the wording very large concentric JFET is utilised to highlight that standard JFETs are much smaller in size. The parts of the p layer situated underneath the n+ rings form the channels of the very large concentric JFETs. The role of the deep n layer is to vertically confine the p layer particularly at the location of the channel. Close to the anode the deep n layer prevents also unwanted punch-through hole current flow from the front side p layer to the backside p+ radiation entry window. In addition close to the anode the p layer functions also as a potential barrier preventing radiation-induced electrons from being absorbed by the innermost n+ rings.

Excluding the two outermost p+ rings the p+ rings are connected to an n+ ring of larger radius in such a manner that in between these interconnected p+ and n+ rings there is always one intermediate p+ ring and one intermediate n+ ring as depicted in figure 2. This means that the electric potential of the intermediate p+ ring is always one JFET channel threshold voltage \(V_{\text{th}}\) (or slightly less) smaller than the electric potential of the interconnected p+ and n+ rings inclosing the intermediate p+ ring. Consequently, the electric potential of the interconnected rings reduces at steps of \(V_{\text{th}}\) towards the outer rim of the detector resulting in a horizontal drift field inside the substrate. The two outermost p+ rings do not have an n+ ring to be interconnected with. It is beneficial to have an electric contact on the second outermost ring that can be monitored externally. The anode is marked with green colour in figure 2 because it could be replaced e.g. with a Modified Internal Gate (MIG) readout transistor [7].

The SDD ring structure of figure 2 is operated by first biasing all the nodes \((V_1, V_2, V_3, \text{ and } V_4)\) of the SDD ring structure at the same potential. Next a suitable reverse bias is applied in between the anode (at potential \(V_5\)) and all the nodes of the SDD ring structure. Then the potential of the innermost n+ ring \((V_2)\) is biased such that the channel underneath is slightly conductive, i.e., the source to gate biasing of the innermost JFET is set close to threshold bias. Next a decreasing
negative potential is applied to the node $V_1$ while the potential at $V_4$ is monitored. The negative potential at $V_1$ is decreased as long as the potential at $V_4$ is at around the same potential than $V_1$. At the onset when the potential at $V_4$ starts to be less negatively biased than $V_1$ one should stop decreasing the potential $V_1$ or to adjust $V_1$ at a value around $V_{th}$ smaller than the potential at $V_4$. In case the potential at $V_1$ is further reduced there will be a too big voltage difference between the outermost n+ ring and the outermost p+ ring and the device will break, i.e., at some point the drain to gate bias of the outermost JFET would exceed the breakdown voltage.

Ideally the biasing of the backside p+ layer is punch-through biased from the front side by a separate large area p+ contact located outside the SDD ring structure e.g. in one corner of the modified SDD chip. In addition, punch-through hole current should be prevented from flowing either from the innermost p+ rings to the p+ backside layer or from the p+ backside layer to the p+ rings. This can be achieved by choosing properly the doping of the large area deep n layer, by adjusting properly the size of the anode, the distance in between the anode and innermost p+ ring, the reverse bias between the anode and innermost p+ ring, as well as by adjusting the substrate doping, the wafer thickness, the amount of concentric JFETs with respect to $V_{th}$, and the bias of the backside p+ layer.

In order for the arrangement to work it is crucial that the innermost n+ ring is biased such that a hole current will run from the innermost p+ ring through the channel beneath the innermost n+ ring to the second innermost p+ ring and onwards towards the outermost p+ ring biased at $V_1$. This current will ensure proper biasing of the SDD ring structure — without it the proposed SDD ring structure would likely break due to the build-up of a too high reverse bias between some of the SDD rings. Afore said current is somewhat analogous to air blown into an inflatable boat for the sake of providing necessary rigidity.

The purpose of the biasing of the SDD’s electrodes (and the backside p+ layer) is first of all to fully deplete the semiconductor body underneath the SDD rings and secondly to create a necessary radial drift field transporting radiation-induced electrons towards the anode as depicted in figure 2. The p+ rings and the backside p+ layer collect the radiation-induced and interface generated holes. The n+ rings collect the interface-generated electrons and thus the generation of dark noise at depleted interfaces is prevented except in the area next to the anode.

In the substrate beneath the deep n layer there is no undulating potential profile in the modified SDD. Instead a constant radial drift field is established in the substrate at relatively small distance from the deep n layer. This stems from the facts that in a p type JFET the electric potential of a conductive p channel is always around the same or smaller than the potential of the p+ source, that the drain is more negative than the source, and that the drain acts as the source of the next JFET situated further away from the anode. On the other hand, the pn junction between the conducting p channel and the deep n layer forms a potential barrier for radiation-generated electrons drifting in the substrate preventing them from being absorbed by the innermost n+ rings. The very same barrier prevents also punch-through hole current flow from the innermost p+ rings towards the p+ backside layer. These aspects enable the radiation-induced electrons to drift next to anode relatively close to the innermost p+ ring meaning that a relatively small reverse bias can be applied between the anode and the innermost p+ ring enabling also a relatively small anode size.

In the modified SDD the maximum reverse bias between the n+ and p+ rings is $2 \times V_{th}$, which is relatively small. Besides, the reverse biased pn junction between the conducting p channel and the n+ rings collecting the interface generated electrons acts as potential barrier for electrons lo-
icated in the n+ rings preventing them from flowing into the substrate. Furthermore, in the modified SDD the biasing of the n+ and p+ rings is not dependent on the amount of positive oxide charge since the potential distribution of the SDD rings is defined by the JFET threshold voltage $V_{th}$ which is not affected by the positive oxide charge but by the p type channel doping beneath the n+ ring as well as by the deep n layer and n type substrate doping. The reason is that the n+ ring situated in between the channel and the interface shields the channel from the influence of the positive oxide charges located at the interface above the n+ ring.

The facts that relatively small reverse biases between the anode and the innermost p+ ring as well as between the n+ and p+ rings may be utilised, that the operation is not affected by positive oxide charge, and that the formation of interface generated dark noise is prevented mean that the modified SDD should be relatively radiation hard. Yet another feature is that the width of the n+ or p+ rings does not play any crucial role in the modified SDD and can be thus chosen freely in different parts of the SDD (e.g. smaller width can be utilized close to anode).

In the proposed novel modified SDD altogether 4 electrodes ($V_1$, $V_2$, $V_3$, and $V_4$) are required for the biasing of the ring configuration whereas only 2 are required in the conventional SDD of figure 1. In the modified SDD no resistor chain is, however, needed and it can be manufactured with standard process steps — beside the n+ and p+ regions only one additional implant mask is required for the large area p and n implanted layers.

3 TCAD simulation study

The simulated modified SDD structure is presented in figure 6. Only half of the structure is needed for 3D simulations since the device is cylindrically symmetric — the rotation axis is depicted in the figure. The width of the p+ drift ring is 5 $\mu$m, the width of the n+ ring acting as the gate is 2 $\mu$m, and the gap between the p+ and n+ rings is 2 $\mu$m. The radius of the n+ anode doping (n6) is 10 $\mu$m and the gap between the innermost p+ drift ring (p6) and the anode is 5 $\mu$m. The simulated device comprises an n- type 300 $\mu$m thick silicon substrate having a resistivity of 2 $k\Omega$cm. The effect of the fixed charge at the Si/SiO$_2$ interface is taken into account by defining an oxide charge concentration as $1e11$ cm$^{-3}$.

The electrostatic potential distribution in the modified SDD is presented in figure 6a and a magnification of the upper part of the device is presented in figure 6b. Electrostatic potential curves along vertical cutlines 1–11 of figure 6b are presented in figure 7 and electrostatic potential curves along the horizontal cutlines A and B of figure 6b are presented in figure 8. The horizontal cutline A intersects the n+ and p+ rings whereas the horizontal cutline B intersects the channel.

Based on figures 7 and 8 one can see(5,6),(993,992) that a constant radial drift field is established inside the substrate guiding signal charges towards the anode, i.e. an undulating potential profile is avoided. The electron current distribution on the cross-section of the modified SDD is presented in figure 9 based on which one can see that no interface-generated electrons are collected by the anode, i.e., there is no interface-generated dark noise in the simulated SDD structure.
Figure 6. Schematic cross-section of the simulated cylindrically symmetric SDD. The rotation axis is depicted in the figure. Contacts p2, n1_p3, n2_p4, n3_p5 are not biased.

Figure 7. (a) The electrostatic potential distribution on a cross-section of the simulated fully depleted SDD structure. (b) A magnification of the upper part of the figure 7a. Vertical cut-lines numbered from 1 to 11 are depicted in the figure 8. The horizontal cut-lines A and B are marked with one line only since the distance between the lines is very small. The horizontal cut-line A intersects the n+ and p+ rings whereas the horizontal cut-line B intersects the large area p type implanted layer along the conducting channels. The potential profiles on the cut-lines A and B are depicted in figure 9.
Figure 8. Electrostatic potential distribution on vertical cut-lines 1–11 depicted in figure 7b. A horizontal drift field is established inside the substrate due to the gradually diminishing potential of the p+ rings.

Figure 9. The horizontal cut-line A of figure 7b intersects both n+ and p+ rings and one can see from the corresponding potential profile that $V_{th}$ of a concentric JFETs is around 2 V and that the potential of the n+ rings as well as of the p+ rings diminishes gradually towards the outer rim of the SDD. The horizontal cut-line B of figure 7b intersects the large area p type implanted layer along the channels and one can deduce from the corresponding potential profile that the channel and the source are approximately at the same potential, i.e., no undulating potential profile is established in the substrate underneath.
Figure 10. (a) Electron current distribution on the cross-section of the simulated modified SDD structure. (b) Magnification of the upper part of figure 10a indicating that no interface-generated electrons are collected by the anode.

4 Conclusions

The simulated proposed modified SDD structure comprises only a small amount of rings surrounding the anode but it is sufficient to prove that the concept functions as intended. The proposed SDD has the advantages that no resistive chain is required, that the formation of interface dark noise is prevented, that the operation is not sensitive to positive oxide charge, and that it should be relatively radiation hard. It should be also possible to utilise the proposed ring structure in detectors that are made from other semiconductor materials than Silicon like e.g. Germanium.

One should note that by incorporating similar large area p and n layers one should be able to provide largely the same benefits than with the proposed modified SDD albeit with the cost of an extra manufacturing step required for the formation of the resistive chain.

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