H/V linear regulator with enhanced power supply rejection

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Abstract: This letter describes a H/V linear regulator for enhancing power supply rejection (PSR) for generating the program/erase voltage. In order to reduce the ripple voltage of the H/V linear regulator, using an additional feedback technique is proposed. The proposed H/V linear regulator has dual loop feedback that improves loop gain and PSR. In the simulated PSR performance, 43.1 dB is observed with the proposed H/V linear regulator at 2.12 MHz. This result is 13 dB better than results obtained with the conventional H/V Linear regulator.

Keywords: Solid State Drive (SSD), NAND flash memory, charge pump, linear regulator

Classification: Integrated circuits

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1 Introduction

There is growing demand for a high performance, high reliability, and low power solid state drive (SSD). The typical SSD consists of several NAND flash memories, DRAMs, and a NAND controller [1, 2].

NAND Flash memory requires some critical improvements to high-voltage analog circuits because of the excessive voltage ripple at the output of a conventional high-voltage generator. The output ripple degrades the...
reliability of NAND Flash memory requiring an improved regulator [3].

In this paper, ripple voltage critical issues will be addressed with analytical methods and HSPICE simulation results. The circuit level improvements make NAND Flash memory an appropriate solution for the solid state drive (SSD).

2 High voltage linear regulator

2.1 High voltage generator

Fig. 1 shows the conventional high-voltage wordline generator circuit. It consists of a charge pump, an oscillator, switching, and linear regulators. The output of the high-voltage generator drives a selected wordline through a switch circuit during the program operation in NAND flash memory. The charge pump with a number of pump stages elevates the supplied voltage to a higher voltage, where the unit stage is composed of transfer elements, a pumping capacitor and switching elements. The oscillator generates a periodic clock and drives the pumping capacitors in the charge pump. The regulator limits the pump output voltage to the required voltage. The regulator consists of a switching regulator and a linear regulator. The output from the switching regulator becomes the input of the linear regulator [3].

A switching regulator is composed of a resistive divider and a comparator, where the comparator detects whether the divided voltage is higher or not than a reference level and acts as an on/off switch. Since the switching regulator switches the driving clock of the charge pump, the output ripple voltage is hard to avoid, and has the effect of widening the programmed cell distribution [4].

An H/V linear regulator consists of a resistive divider, an error amplifier, and a pass element as a NMOS or PMOS transistor. A PMOS transistor can easily achieve low drop output voltage, but NMOS has a better slew rate and transient load response characteristics. The circuit shown in Fig. 2 can be improved in terms of the maximum output voltage by using triple well transistors in order to eliminate the body effect on the follower and low-VTH transistors in order to reduce the voltage drop between the gate and source due to the threshold voltage of the follower [1].

The ripple voltage during the program operations increases the chance of an over programmed cell with a higher threshold voltage than the nominal programmed value. This will reduce the boosted channel program inhibit voltage, increasing the program stress and lowering endurance [4].

In order to have good PSR at high frequency, the DC gain and the bandwidth of the error amplifier (EA) of an H/V linear regulator have to be
large, which is very challenging [4].

2.2 Simple model for PSR of H/V linear regulator

The noise on the charge pump output (PMP_OUT) can be coupled to the output of the H/V linear regulator (VPGM,OUT) through the drain of the pass transistor (path 1), the gate of the pass transistor (path 2), the internal supply voltage (VCCI), (path 3), and the reference voltage (path 4), as shown in Fig. 2.

The switching noise of a charge pump can be seriously coupled to the output of an H/V linear regulator (VPGM,OUT) through path 1 and path 2. The ripple of the charge pump through path 2 is coupled to the gate of the pass transistor, and directly affects the output of the H/V linear regulator. The ripple of the charge pump through path 1 becomes less problematic due to the drain terminal path of the pass transistor, as it is clear that the charge pump noise coupling through path 2 is dominated.

An intuitive and insightful model for analyzing the PSR of a typical H/V linear regulator is presented in Fig. 3. This model consists of an impedance ladder comprising of the channel resistance of the pass tr. ($r_{\text{on,pass tr.}}$), the modeled transconductance resistance ($1/g_{m\text{, pass tr.}}$), a parallel combination of the open-loop output resistance to ground ($z_o$), and the shunting effect of the feedback loop ($z_{\text{reg}}$). Hence, referring to Fig. 2 and Fig. 3, we can see that

$$Z_o = (R_1 + R_2)||R_L||Z_{\text{OUT}},$$

and,

Fig. 3. Intuitive model for PSR in action at various frequencies
\[ Z_{o\_reg} = \frac{(R_1 + R_2)|R_L||Z_{OUT}}{A_{ol} \times \beta} \]

where \( A_{ol} \) is the loop gain of the H/V linear regulator feedback, \( \beta \) is the ratio of \( R_1 \) and \( R_2 \) [5, 6].

2.3 Model in action over a wide frequency range

Fig. 4 depicts a sketch of a typical PSR curve and how the intuitive model allows us to determine the PSR performance of an H/V linear regulator over a large range of frequencies, simply by accounting for the frequency dependence of \( z_o \) and \( z_{o\_reg} \) [5, 6].

At low frequencies, the high loop gain \((A_{ol\_dc} \cdot \beta)\) allows \( z_{o\_reg} \) to shunt \( z_o \). The following simplification can be derived:

\[
PSR|_{Path2_{DC}} \approx \frac{R_1 + R_2}{1 + \frac{R_1 + R_2}{g_{m1} A_{ol} \times \beta}} \approx \frac{R_1 + R_2}{1 + \frac{(R_1 + R_2) \times g_{m1}}{A_{ol} \times \beta}} \approx \frac{1}{A_{ol} \times \beta} \quad (3)
\]

Consequently, the PSR of the H/V linear regulator is intimately related to the open-loop gain of the system.

At moderate frequencies, the shunting effect of the feedback loop deteriorates at frequencies beyond the bandwidth of the amplifier, \( BW_A \) (or dominant \( P1 \)), thereby causing an increase in the regulated output impedance, \( z_{o\_reg} \). This leads to a rise in the output ripple and, consequently, the dominant PSR breakpoint in the form of a PSR zero \((Z_1)\). The resultant degradation in the PSR can be obtained by replacing the open loop gain \((A_{ol})\). Between the dc and the unity-gain frequency (UGF) of the system, the following simplification can be derived:

Fig. 4. Intuitive model for PSR in action at various frequencies
The presence of a PSR pole (P1) at the unity-gain frequency, as predicted by (5), can be easily understood when we note that the deterioration of the PSR due to the increasing closed-loop output resistance ceases at the UGF. At this stage, the shunting effect of the feedback loop no longer exists and the PSR is determined simply by the frequency-independent resistive divider between the transconductance resistance of the pass device (1/gmn) and the feedback resistors (R1+R2). The PSR is given by

$$\text{PSR}|_{\text{Path2}, f \leq \text{UGF}} \approx \frac{1}{A_{ol}} \times \frac{1}{1 + \frac{s}{P1}}.$$

(4)

At these frequencies, the PSR of the system is the weakest because the closed loop output resistance is not decreased by the feedback loop and the output capacitor cannot shunt the output ripple to ground.

At high frequencies, when the output capacitor starts shunting (R1+R2) to ground, a smaller ripple appears at the output, thereby causing an improvement in the PSR (Zo = decreases with increasing frequency) and the PSR pole (P2). Thus,

$$\text{PSR}|_{\text{Path2}, f = \text{UGF}} \approx \frac{R_1 + R_2}{R_1 + R_2 + \frac{1}{g_m}}.$$

(5)

The simple model depicted in Fig. 4 provides an intuitive understanding of the relationship between PSR and the open-loop gain of the H/V linear regulator.

### 3 Proposed high voltage linear regulator

The supply noise rejection (PSR) capability of the regulator is dominated by the transfer function of the H/V linear regulator at low frequency. When the frequency becomes high, the PSR is dominated by the feed-through of the output resistance of the pass transistor. The PSR will become the ratio between the voltage divider ron and (R1+R2)//Rl//ZCOUT. This effect will become more severe when the output capacitor is small. The extension of the bandwidth will have a positive effect on the PSR as shown in Fig. 5 (a). Therefore, to get an H/V linear regulator with high supply noise rejection at high frequency, a wide-gain-bandwidth H/V linear regulator topology should be used.

The proposed high voltage linear regulator is shown in Fig. 5 (b). The dual op amp regulator is constituted by a main feedback path and by an auxiliary feedback path. In order to extend the PSR bandwidth, an extra amplifier (Amp.2) is added. It will drive the gate of a pass transistor together with the conventional error amplifier (Amp.1). The output of Amp.1 is compensated by miller capacitor but the output of Amp.2 is not compensated, so the pole1A, and pole1B is located in different frequency
(a) Concept of the improved PSR strategy

(b) Proposed high voltage linear regulator

(c) Small-signal model of the proposed high voltage generator

(d) Concept of the improved open loop gain

(e) Adopted topology of Amp.1 and Amp.2 (Ref. [7])

Fig. 5. Proposed high voltage linear regulator
range.

As shown in Fig. 5 (e), the Amp.1 and Amp.2 is designed to achieve a higher gain compare with conventional regulator, it improve the dc loop gain [7]. The Amp.1 and Amp.2 is designed to achieve a higher bandwidth compare with conventional regulator to improve the PSR performance at high frequency.

We proposed the hybrid topology of Amp.1 and Amp.2 instead of doubling DC current of Amp. The designed output impedance of Amp.1 (Z_{out1}) and output impedance of Amp.2 (Z_{out2}) have different frequency range.

The main feedback path, (Amp. 1) covers the low frequency, and the auxiliary feedback path (Amp. 2) covers the high frequency ranges. The main feedback path is compensated by the miller capacitor (C_C), and the output of Amp.1 create a dominant pole (Pole 1A). However, the auxiliary feedback path (Amp.2) is not compensated for improving the high frequency response. The small-signal model of the regulator is shown in Fig. 5 (c).

As shown in Fig. 5 (d), the overall open loop transfer function is given by when the low frequency

\[
\text{Loop Gain (Low Freq.)} = \frac{V_{FB}}{V_{IN}} = \left\{ g_{m,\text{amp.1}} \times \left( \frac{1}{s \cdot \left( C_C \times g_{m1} \times R_D \right)} \right) \right\}
\]

\[
+ g_{m,\text{amp.2}} \times R_{out,\text{amp2}} \right\} \times \left\{ \left( g_{m1} + g_{m2} \right) \cdot R_D \right\}
\]

\[
\times 1 \times \left\{ \frac{R_2}{R_1 + R_2} \right\}
\]

and when the high frequency

\[
\text{Loop Gain (High Freq.)} = \frac{V_{FB}}{V_{IN}} = \left( g_{m,\text{amp.2}} \times R_{out,\text{amp2}} \right) \times \left( g_{m2} \cdot R_D \right) \times 1
\]

\[
\times \left\{ \frac{R_2}{R_1 + R_2} \right\}
\]

where \( g_m \) and \( r_o \) represent the transconductance and output resistance of the transistor, respectively, and \( C_{out} \) is the output capacitor.

Under the same total quiescent current of the H/V linear regulator, the proposed H/V linear regulator results in a higher DC gain and bandwidth than the conventional H/V linear regulator.

### 4 Simulation results

For AC analysis of the H/V linear regulator, we can break the feedback loop, as shown in Fig. 5 (b).

The simulated H/V linear regulator condition of the internal on-chip output capacitor is 15 pF, and the maximum output current of 1 mA. And the quiescent current of the H/V linear regulator is 150 \( \mu \)A. The H/V linear regulator stability and its specifications are ensured for all of the process corners and over a temperature range of \(-20^\circ\text{C}\) to \(100^\circ\text{C}\). The simulated
open loop gain of the proposed H/V linear regulator is 51.6 dB, the unit gain frequency is 14.1 MHz, and the phase margin is 83.4° for a load current variation from 0 mA to 1 mA, as shown in Fig. 6 (a). These results are 17.7 dB and 11.65 MHz better than the results obtained without the proposed auxiliary amplifier.

The achieved PSR performance of the proposed H/V linear regulator topology is presented in Fig. 5 (b). As can be seen by inspection of Fig. 6 (b), the proposed strategy allows a large improvement of the PSR.
when compared to the conventional topology. As discussed previously, the PSR performance is highly correlated with the bandwidth and open loop gain. As can be seen in Fig. 6 (b) the system has $-51.7 \text{ dB}$ at DC and $-43.1 \text{ dB}$ at 2.12 MHz. These results are 17.7 dB and 13 dB better than the results obtained without the proposed auxiliary amplifier. As shown in Fig. 6 (b), The PSR is worse around 40 MHz, so the linear regulator is used at less than 40 MHz.

The transient simulation results of the H/V linear regulator are shown in Fig. 6 (c) to confirm the stable operation and ripple voltage. The HSPICE simulation result shows the high-voltage ripples at a 20.0 V target voltage. We used the cross coupled charge pump, H/V switching regulator, and H/V linear regulator for the simulation. The ripple voltage of the H/V linear regulator is reduced from 30.4 mV to 20.5 mV by using the proposed H/V linear regulator. The important parameters of the H/V linear regulator are summarized in Table I.

| Table I. HSPICE Simulation Results |
|-------------------------------------|
| Loop Gain ($V_{IN}/V_{OUT}$) & PSR ($V_{PGM,OUT}/V_{PREV,OUT}$) & Trans. ($\Delta V_{PGM,OUT}$) |
| Unit Gain Freq. (P.M.) & @ DC [dB] & @ 2.12 MHz |
| Conven. 2.45[MHz] / (79°) & -34 [dB] & -50.1 [dB] & 30.4 [mV] |
| Proposed 14.1[MHz] / (83.4°) & -51.7 [dB] & -43.1 [dB] & 20.5 [mV] |

5 Conclusion

We describe a high-voltage analog system particularly suited for application to a NAND Flash memory. In order to reduce the ripple voltage of the program/erase voltage, a technique using additional feedback is proposed. The proposed H/V linear regulator has dual loop feedback. In the simulated PSR performance of proposed circuits, $-43.1 \text{ dB}$ was observed at 2.12 MHz. This result is 13 dB better than the results obtained conventional H/V Linear regulator.

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