Single event burnout hardening of trench shielded power UMOSFET using High-$\kappa$ dielectrics

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Keywords: single event burnout (SEB), high-$\kappa$ dielectric, P+ shielding region, SEB hardening, U-shaped trench-gate MOSFET (UMOSFET), silvaco TCAD simulation

Abstract
This study proposes the High-$\kappa$ dielectric Trench Shielded power UMOSFET (HK TS-UMOSFET) to be assessed using the two-dimensional numerical simulations. The simulations are employed to evaluate HK TS-UMOSFETs susceptibility to single-event burnout (SEB) mechanism. Based on the findings, the influence of alternative high permittivity gate dielectrics to silicon dioxide ($\text{SiO}_2$) in TS-UMOSFET was discussed. Furthermore, in order to improve the performance of the device, its electrical behaviour was simulated with several high-$\kappa$ dielectrics including $\text{Al}_2\text{O}_3$, $\text{Si}_3\text{N}_4$ and Aluminium Nitride (AlN). When heavy ions strike the sensitive areas of the device, the electric field distribution and SEB threshold values were extracted. Based on the values yielded, (AlN) was identified as a promising high-$\kappa$ material to achieve SEB-hardened TS-UMOSFET compared to the other high-$\kappa$ dielectrics. In conclusion, with (AlN), the HK TS-UMOSFET offers a high SEB tolerance and improved electrical characteristics.

1. Introduction

High-frequency power switching systems usually prefer power MOSFETs, especially trench MOSFETs in space applications. However, its reliability is affected by the radiation effects induced by the energetic heavy ions in the radiation environment [1–3]. Among the destructive radiation effects is the Single-Event Effects (SEE), which is capable of permanently damaging the device. SEEs are classified into Single-Event Burnout (SEB) and Single-Event Gate Rupture (SEGR). SEB mainly depends on the inherent parasitic bipolar junction transistor (BJT) in the MOSFET structure. So, heavy-ions that pass through the power MOSFET during OFF state condition deposit charge along its ion track. The deposited charge then turns ON the parasitic BJT resulting in the high level of current due to the short between source and drain, which finally causes the device to burnout. The activation of the parasitic BJT is due to the interaction of the ionized space charge generated by the high energy ions along its trajectory through the device and the strong electric field in the depletion region of the reverse biased n/drift/substrate junction.

Furthermore, the Linear Energy Transfer (LET) is used to describe the amount of ionisation depending on the ion species and energy. Meanwhile, the geometry of the MOSFET elementary cells determines the shape of the electric field and the active volume of the parasitic transistor. When the ionisation column interacts with the high applied electric fields, a substantial amount of current passes along the space charge column. A drop in the voltage occurs when a fragment of the current runs laterally into the bulk. Voltage drop is determined by the bulk resistivity, where it may surpass the threshold value required to directly polarise (forward bias) the base-emitter junction (i.e. source-bulk) of the parasitic transistor. In the case of SEGR, the sensitive strike location is at the neck region i.e., centre of the device or area between p-body diffusions. It will then accumulate excessive holes at the Si–$\text{SiO}_2$ interface causing a gate-oxide breakdown [4–6]. Therefore, this study focuses on the primary design concerns namely the suppression of the electric field density and the prevention of gate oxide damage in the enhancement of the trench MOSFET structure.
occurs in a silicon UMOSFET. The addition of a high-

2. High-κ dielectrics on trench shielded MOSFET

Figure 1 illustrates the schematic diagram of a standard power UMOSFET and High-κ Trench shielded UMOSFET with a breakdown voltage of 70 V. The width of the device’s unit cell was 3.0 μm, while the channel length was 0.4 μm. On the other hand, the electric field increases at the bottom of the trench corner when SEB occurs in a silicon UMOSFET. The addition of P⁺ shielding region below the trench bottom significantly reduces the high electric field. But, this P⁺ shielding region increases the ON-resistance due to the formation of JFET region. In order to reduce the resistance, n-region was added to cover the P⁺ shielding region at the bottom of the trench. Besides that, different high-κ dielectric materials were used instead of SiO₂ to prevent the gate oxide damage at the bottom of the trench. Hence, two-dimensional SEB simulations for the High-κ TS-UMOSFET and a structure with standard gate dielectric were performed using the Silvaco ATLAS simulator to compare the characteristics of the parameters. Finally, the SEB performance was investigated by analysing the inner physical behaviour, a critical value of LET and the safe operating voltage of the device during heavy-ion radiation. The simulation results indicated that high-κ dielectrics are promising techniques to achieve SEB hardened power TS-UMOSFET.

Previous literature has extensively investigated many potential hardening techniques to improve the SEE survivability of trench MOSFET which is also known as power U-shape Metal Oxide Semiconductor Field Effect Transistor (UMOSFET) [7–12]. Previous solutions are mainly focused on the Radiation Hardened by Design (RHBD) techniques to mitigate the radiation effects in UMOSFET. However, some researchers have assessed the Radiation Hardness by Process (RHBP) method for SEE hardening of Vertical Double Diffused Metal Oxide Semiconductor Field Effect Transistor (VDMOSFET). Wan et al proposed that Si₃N₄ is a promising gate dielectric to achieve SEB-hardened VDMOS [13]. In addition, [14] high-κ dielectric material for an inner dielectric layer (ILD) and passivation layer designs have been identified to significantly improved the Total Ionizing Dose (TID) and SEB performance of VDMOS. However, the effects of SEB on UMOSFETs using high-κ dielectric as a gate oxide has not been fully investigated and discussed.

Consistent with previous practice in VDMOS, this study also incorporated high-κ dielectric as a gate oxide on TS-UMOSFET to mitigate the SEB effects. In order to reduce the high electric field and ON-resistance, the n-type region was added to cover the P⁺ shielding region at the bottom of the trench. However, the standard SiO₂ gate oxide was unable to withstand a high electric field, resulting in the breakdown of the gate oxide. In order to prevent the gate oxide damages, a high-κ dielectric material is used instead of SiO₂.

In contrast to standard UMOSFET, the HK TS-UMOSFET contains P⁺ shielding region surrounded by n-region with the thickness are set to 0.1 and 0.2 μm, respectively. The doping concentration of the layers were set at 1.0 × 10¹⁹ cm⁻³ and 6.0 × 10¹⁶ cm⁻³. In addition, the n-buffer layer was included to enhance the SEB performance [18]. The thickness of the drift region was reduced from 2.5 to 2.4 μm in order to insert the buffer layer. The thickness of the buffer layer and doping concentration was set at 0.7 μm and 5.6 × 10¹⁶ cm⁻³, respectively. Table 1 summarises the device parameters used for the design simulation. Table 2 lists the various high-κ materials used in this study along with their physical properties. Since the dielectric constants for Al₂O₃,
Table 1. Device Parameters for Simulation

| Device Parameter | Standard UMOS | Hardened UMOS |
|------------------|---------------|---------------|
| Trench width \((W_g)\) | 0.5 μm | 0.5 μm |
| Mesa width \((W_p)\) | 1 μm | 1 μm |
| Trench depth | 1 μm | 1 μm |
| Gate oxide thickness | 0.05 μm | 0.05 μm |
| \(P^+\) shielded thickness \((L_{ps})\) | ... | 0.1 μm |
| \(n\) region thickness \((L_{an})\) | ... | 0.1 μm |
| \(n\) region width \((W_{an})\) | ... | 0.25 μm |
| \(P^+\) source depth | 0.2 μm | 0.2 μm |
| \(n^+\) source depth \((L_{as})\) | 0.2 μm | 0.2 μm |
| P-base region depth \((L_p)\) | 0.6 μm | 0.5 μm |
| Drift region thickness \((L_d)\) | 2.5 μm | 2.4 μm |
| Buffer Layer thickness \((L_b)\) | ... | 0.7 μm |
| \(P^+\) source doping | \(2.0 \times 10^{19}\) cm\(^{-3}\) | \(2.0 \times 10^{19}\) cm\(^{-3}\) |
| \(n^+\) source doping | \(1.0 \times 10^{19}\) cm\(^{-3}\) | \(1.0 \times 10^{19}\) cm\(^{-3}\) |
| \(n\) region doping | ... | \(6.0 \times 10^{16}\) cm\(^{-3}\) |
| \(P^+\) shielded doping | ... | \(1.0 \times 10^{18}\) cm\(^{-3}\) |
| P-base region doping | \(1.7 \times 10^{17}\) cm\(^{-3}\) | \(1.7 \times 10^{17}\) cm\(^{-3}\) |
| Buffer Layer doping | ... | \(5.6 \times 10^{16}\) cm\(^{-3}\) |
| Drain region doping | \(5.6 \times 10^{14}\) cm\(^{-3}\) | \(5.6 \times 10^{14}\) cm\(^{-3}\) |
| Substrate doping | \(1.0 \times 10^{19}\) cm\(^{-3}\) | \(1.0 \times 10^{19}\) cm\(^{-3}\) |

Table 2. Dielectric Material Properties

| Material | Dielectric constant \((\kappa)\) | Bandgap \(E_{g}\) (eV) | \(\Delta E_c\) (eV) for Si |
|----------|-------------------------------|------------------------|--------------------------|
| SiO\(_2\) | 3.9                           | 8.9                    | 3.2                      |
| Si\(_3\)N\(_4\) | 7.0                | 5.1                    | 2.0                      |
| Al\(_2\)O\(_3\) | 9.0              | 8.7                    | 2.8                      |
| AlN  | 9.14                          | 6.23                   | 2.2                      |

Figure 2. Transfer characteristics of TS-UMOSFET with various high-\(\kappa\) material as gate oxide.
Si₃N₄ and AlN are higher than that of SiO₂, the thickness of high-κ dielectric used for the simulation was calculated using equation (1).

$$T_{\text{high-κ}} = EOT \times \frac{\epsilon_{\text{high-κ}}}{\epsilon_{\text{SiO₂}}}$$  \hspace{1cm} (1)

where $\epsilon_{\text{high-κ}}$ and $T_{\text{high-κ}}$ are the dielectric constant and thickness of high-κ materials. While $\epsilon_{\text{SiO₂}}$ is the dielectric constant of SiO₂. Hence, equivalent oxide thickness (EOT) for the rest of the high-κ materials was fixed as the same value as SiO₂ to maintain the oxide capacitance [19].

2.1. Simulation setup

The Silvaco ATLAS device simulator was utilised to perform the two-dimensional numerical simulations. The physical models employed in the simulations are classified into recombination, mobility, carrier statistics and impact ionisation model. The recombination model of ShockleyReadHall (SRH) measures the rate of recombination of electrons and holes, in which the concentration-dependent carrier lifetimes (CONSRH) is recommended for silicon (Si) material and Auger recombination is used for high current densities. Next, the mobility models namely FLDMOD and Caughey-Thomas ANALYTIC consider the electric field dependencies in order to calculate the carrier concentration and temperature. The Fermi–Dirac and Band-gap narrowing (BGN) statistics models were used since this study to assess the heavily doped regions in the structure.
addition, the impact ionisation model was utilised to calculate the ionisation rates, while the Selberherr model was used for the blocking characteristics simulation. On the other hand, a simplified heavy-ion model was additionally included using the SINGLEEVENTUPSET statement to investigate the SEB performance. Moreover, in order to simulate an ionising impact within a structure, a function that generates the electron-hole pairs at the vertical direction in a specific area was defined and computed using equation (2).

\[ G(r, l, t) = G_{\text{LET}}(l) \ast S(r, l) \ast T(t) \]  

where \( S(r, l) \) and \( T(t) \) are functions describing the spatial and temporal variations of the generation rate. \( r \) is the radial distance from the centre of the track to the point and \( l \) represents the variation of carrier generation along the path of the track. \( G_{\text{LET}}(l) \) is the LET generation density relating to the LET (pC/\( \mu \)m) of the ions [20]. In addition, \( G, S \) and \( T \) are user-specifiable parameter in the units of cm\(^{-3}\), \( \mu \)m and s, respectively. For this research simulation, the track radius of the spatial Gaussian function was set to 0.05 \( \mu \)m, the initial time \( T_0 \) of the charge generation was fixed to \( 4 \times 10^{-12} \) s and the temporal Gaussian function width \( T_C \) was set to \( 2 \times 10^{-12} \) s. The ion track information is specified by an entry point and exit point locations, \((x_0, y_0, z_0)\) and \((x_1, y_1, z_1)\), respectively. As for the 2-dimensional simulation, \( z_0 \) and \( z_1 \) were assumed to be negligible. The incident position of ions \( x_0 \) and \( x_1 \) are positioned at different locations (0, 0.7, 1.25) to identify the sensitive positions. Heavy ions are assumed to penetrate in a perpendicular direction, for that \( y_0, y_1 \) coordinates are set to 0 and 4.3 respectively.

![Figure 5](image-url) **Figure 5.** Negative I-V characteristics of standard and hardened power UMOSFET.

![Figure 6](image-url) **Figure 6.** The input (Ciss), reference (Crss) and output (Coss) capacitances for standard and hardened power UMOSFET.
While performing radiation experiments, the LET described the total energy loss per path length by a charged particle, which is given in the units of MeV/mg/cm². During the simulations, however, the LET is usually described as the deposited charge per unit length of the track and is expressed in pC/μm. Hence, equation (3) represents the conversion from MeV/mg/cm² to pC/μm:

\[
\frac{Q}{W_{dp}} \times \text{LET (MeV/mg/cm}^2\text{)} \times \rho = \text{LET (pC/μm)}
\]  

(3)
where $W_{e-h}$, which is the average energy required to produce an electron-hole pair in Si was 3.6 eV, while the $\rho$ which represents the density of the Si material was 2.33 g cm$^{-3}$ and $Q$ denotes the charge of an electron ($1.6 \times 10^{-19}$ C). Hence, the simplified result for the Si material is 1 pC/\mu m = 97 MeV/(mg/cm$^2$). The desirable LET value used in the simulation that was set at 0.6 pC/\mu m, corresponds to 60.0 MeV/mg/cm$^2$ heavy ion beam Iodine (I) ($Z = 53$), depending on the conversion factor of 0.0097. The overall simulation was carried out at an atmospheric temperature of 300K [21].

### 2.2. Parameter characteristics

This section describes the simulated electrical behaviour of power TS-UMOSFET with different high-$\kappa$ dielectrics as a gate oxide. A threshold voltage value of ($V_{th}$) was observed in the transfer characteristics as depicted in figure 2. Based on the figure, the high-$\kappa$ material was confirmed to influence the $V_{th}$. However, the threshold voltage decreases with an increase in dielectric constant. In this study, the high-$\kappa$ material was chosen based on the optimised threshold and breakdown voltage almost similar to the standard SiO$_2$. The threshold voltage for TS-UMOSFET was confirmed at 1.4 V using high-$\kappa$ dielectric material, AlN. Next, figure 3 summarises the breakdown characteristics. The figure indicated that AlN as gate oxide yielded a similar breakdown voltage with the standard (i.e. 70V). The IV characteristics for positive drain currents at $V_{GS} = 4, 5, 6$ and 7 V are illustrated in figure 4. Based on the figure, the drain current was estimated at a slightly higher value for the hardened TS-UMOSFET due to the specific lower resistance $R_s$.

On the other hand, the negative drain current characteristics were characterised at a bias voltage of $V_{GS} = -4$ V as demonstrated in figure 5. The value of the negative drain current for the hardened device increased slightly compared to the standard device. Figure 6 illustrates the dynamic characteristics of standard and hardened power MOSFETs. The hardened structure was identified to possess similar trends of input (Ciss), reference (Crss) and output (Coss) capacitances with the standard. Therefore, the SEB hardened mechanism of trench shielding and AlN high-$\kappa$ material as a gate oxide is not affected by the current handling capability.

Table 4. SEB Simulation Results with Different LET Values for power UMOSFET

| LET (pC/\mu m) | 30 | 40 | 45 | 50 | 55 | 60 | 65 | 68 |
|---------------|----|----|----|----|----|----|----|----|
| 0.1           | N  | N  | N  | N  | N  | N  | Y  | Y  |
| 0.3           | N  | N  | N  | N  | N  | Y  | Y  | Y  |
| 0.4           | N  | N  | N  | N  | Y  | Y  | Y  | Y  |
| 0.6           | N  | Y  | Y  | Y  | Y  | Y  | Y  | Y  |
| 0.9           | N  | Y  | Y  | Y  | Y  | Y  | Y  | Y  |

Note. $^a$ Y = SEB is present, N = SEB is absent.
2.3. Fabrication procedure

This study utilised the numerical simulation tools to verify the characteristics of the device. A feasible fabrication procedure was employed to demonstrate the possibility of this optimised structure. The process initiates with the formation of a buffer layer on the top of an arsenic-doped Si substrate. Followed by the epitaxially grown first drift layer on the buffer layer and the formation of a mask layer on the drift region. Referring to figure 7(a), ion implantation progressed to form the added n-type region. Next, the second drift layer (the area above the dashed line) as depicted in figure 7(c), was formed on the first layer upon the removal of the mask layer. Both the drift layers provide a whole drift region of the device with a doping concentration and thickness of 2.5 μm and 5.6 × 10¹⁴ cm⁻³, respectively. Then, the third epitaxial layer p-base region with a thickness of 0.5 μm is grown. Subsequently, ion implantation was performed using Al and P ions over the P-body to form P⁺ and n⁺ regions, respectively (figure 7(d)). The thickness of the n⁺ region is limited to 0.2 μm. Consequently, the Reactive-Ion Etching (RIE) technique was used to form the trench structure (figure 7(e)). At the bottom of the trench, the P⁺ shielding region was obtained through ion implantation (figure 7(f)). Next, the high-κ dielectric gate oxide film was deposited through the Atomic Layer Deposition (ALD) technique where the gate electrode was fabricated by depositing polysilicon (figure 7(g)). The metallization of source and drain regions are formed through the deposition and patterning of the Al metal layer. Figure 7(h) represents the complete device structure.

3. SEB simulation results and discussion

The SEB simulation results are analysed and discussed in this section. Based on the findings, HK TS-MOSFET was identified to be harder and less sensitive to SEB compared to UMOSFET. The improved performance of HK TS-MOSFET was due to the presence of high-κ dielectric material as the gate oxide, with added n-region covering the P⁺ shielding region along with an optimised buffer layer. The high-κ dielectric maintains a moderate electric field at the gate oxide, while the P⁺ shielding region provides additional leak path for hole currents and the buffer layer reduces the impact ionization at the junction of the drift layer and substrate [18, 22].
The SEB’s performance of power UMOSFET was extensively investigated using a heavy-ion strike model with variable voltage from drain to source while keeping the gate voltage constant at zero. The position of ion collision is defined by the entrance and exit in the x and y directions, respectively. Therefore, when the power UMOSFET is biased off, the energy ions that strike the structure trigger the parasitic bipolar transistor causing SEB. In order to investigate the SEB trigger mechanism, the most vulnerable heavy ion strike position needs to be ascertained as the device is highly affected by it compared to the other strike positions. The 3 different positions chosen for the assessment are positions (a) $x_0 = 0 \mu m$, (b) $x_0 = 0.7 \mu m$ and (c) $x_0 = 1.25 \mu m$ (table 3) (figure 8). Based on the observations, position $x_0 = 0 \mu m$ was identified as the most sensitive position of SEB for both the conventional and proposed device. Subsequently, the effects of various LETs were simulated under different drain bias voltages as listed in table 4. Since an increase in LET after 0.6 pC/μm did not affect the occurrence of SEB, LET = 0.6 pC/μm heavy ions were generated at different incidents and transient drain performances were investigated for several drain bias voltages. As a result, the LET value of 0.6 pC/μm and ions track position (a) were chosen to investigate the SEB performance in the proposed device.

Figure 10. Hole concentrations of (a,b) UMOSFET, (c,d) TS-UMOSFET and (e,f) hardened High-κ TS-UMOSFET at $t = 150$ ps (left) and $t = 1$ ns (right) after an ion’s strike at LET = 0.6 pC/μm.
In addition, the time variation of the hole-concentration distribution when the SEB of the HK TS-UMOSFET is triggered is depicted in Figure 9. The evolution of the hole concentrations inside the structure following an ion’s strike time at 5ps, 50ps, 150ps and 1ns was extracted for from a drain voltage of 40 V at a LET = 0.6pC/μm. These variations are helpful in understanding the mechanism of the SEB effect. At 5ps, the holes were distributed in the P⁺ region, channel and part of the drift region. When the hole concentration of p-body increased to 50ps, parasite BJT was activated. At 150ps, the distribution of the holes in the drift layer was wider and filled up with a device. During this time, many holes are injected into the channel which turns ON the parasite BJT. Even after t = 1 ns, the concentration of the holes kept increasing and the transient current remained high. Hence, when the SEB effect was triggered, the proposed device was exhausted.

Figure 10 compares the hole distribution in UMOSFET, TS-UMOSFET and the HK TS-UMOSFET following the ion strike at V_{DS} = 40 V. Based on the observation, the hole concentration at t = 150ps and t = 1 ns for the conventional structure reached a high concentration rate which subsequently caused SEB. To the contrary, the hole concentration decreased to a very low level for the HK TS-UMOSFET due to the high-κ gate oxide material, the shielding region at the bottom of the trench and the presence of buffer layer.

Changes in an electric field can also reflect on the impact of single event effects on a devices performance. Figure 11(a) represents a preliminary investigation conducted to assess the influences of high-κ dielectric
material on the electric field under $V_{DS} = 50$ V following an ion strike at $t = 150$ ps. The higher electric field was found to exist at the trench corner and junction of $N^+ drift / N^0$ substrate. The high-$\kappa$ dielectric material reduces the electric field compared to standard gate oxide. The peak electric field of TS-UMOSFET using $SiO_2$ yielded $3.22 \times 10^5$ V/cm, while using high-$\kappa$ dielectric namely $Al_2O_3$, $Si_3N_4$ and $AlN$ yielded $1.16 \times 10^5$ V/cm, $1.12 \times 10^5$ V/cm and $0.8 \times 10^5$ V/cm, respectively. In addition, the distribution of the electric field was also noticed during an ion strike at $t = 1$ ns (figure 11(b)). A similar trend was also observed, where the peak electric field at the junction was estimated at $1.37 \times 10^5$ V/cm for $AlN$ compared to $5.78 \times 10^5$ V/cm for $SiO_2$. Hence, $AlN$ material was identified as a promising gate oxide to reduce the electric field in the TS-UMOSFET.

A comparison of the electric field distribution inside the structure for the standard UMOSFET, TS-UMOSFET and hardened HK TS-UMOSFET is presented in figure 12(a). The peak electric field of the standard UMOSFET was measured at $4.69 \times 10^5$ V/cm, while for TS-UMOSFET it was $3.22 \times 10^5$ V/cm at $t = 150$ ps. However, the electric field in the drift layer of the hardened TS-UMOSFET was lowered to $0.8 \times 10^5$ V/cm, due to the spread-out distribution of the electric fields. The electric field distribution of the standard UMOSFET and hardened TS-UMOSFET at $t = 1$ ns after an ion strike was depicted in figure 12(b). Based on the observation, high electric field recorded a peak value of $5.78 \times 10^5$ V/cm compared to $2.67 \times 10^5$ V/cm for standard oxide and $1.37 \times 10^5$ V/cm with high-$\kappa$ oxide.
In standard MOSFET, the electric field observed in the simulated structures consistently peaks at the P+ body/N-drift junction towards the end of the simulation. This observation was possible through the highly localized current which passes along the right side of each structure. For instance, a bulk of the current passes between the inherent parasitic npn transistor (n+ cathode/p-body/n-drift). Similarly, when a simulation reaches the end, the electric field also peaks at the homo-junction (n-drift/n+ substrate) for UMOSFET, TS-UMOSFET and HK TS-UMOSFET. A strong avalanche rate is formed at a maximum electric field as the ionisation coefficients are exponentially related to the electric field. Thus, the generated currents lead to thermal runaway and burnout. Furthermore, the peak electric field is directly proportional to the impact ionisation coefficient, which is related to the SEB sensitivity \[23, 24\]. Hence, the reduction of the peak electric field will improve the SEB performance \[25\]. The ionisation coefficients of the hardened structure are relatively low. The lower electric field results in a less sensitive device towards SEB. Thus, the proposed structure achieved a 76.3% lower electric field compared to the conventional structure.

The changing of drain current as a function of time after a single heavy ion strikes the device for the standard and various high-κ dielectrics used in TS-UMOS is demonstrated in figure 13. The response indicated that the transient current increases rapidly to reach a maximum value of less than 100 ps. Next, the hole current that was generated at the termination of the simulation was not able to be sustained without parasitic BJT, hence, the current dropped to zero immediately. In addition, standard devices generate higher currents at higher drain voltages, while the hardened structure yield lower currents at the same \(V_{DS}\). Therefore, in short, the drain voltage can significantly affect the triggering of the SEB because higher \(V_{DS}\) represents a wider space of charge region resulting in a larger transient current.

The drain SEB threshold voltage is considered as one of the main indexes to characterise a devices SEB performance. Table 5 summarises the SEB threshold voltage simulation results of the devices for different biased

![Figure 13. Drain current versus time for the silicon dioxide and high-κ dielectrics as gate oxide in TS-UMOSFET after an ion strike.](image)

**Table 5.** SEB Threshold Voltage values for Power UMOSFETs at \((LET = 0.6 \, \text{pC/μm})\)

| Type                     | \(V_{a,supply}(V)\) |
|--------------------------|----------------------|
|                          | 40                   |
| Standard UMOSFET         | Y                    |
| TS-UMOSFET using SiO\(_2\) | N                  |
| Hardened TS-UMOSFET      | \(Al_2O_3\)          |
|                          | \(Si_3N_4\)          |
|                          | AlN                  |

| Type                     | \(V_{a,supply}(V)\) |
|--------------------------|----------------------|
|                          | 50                   |
| Standard UMOSFET         | Y                    |
| TS-UMOSFET using SiO\(_2\) | N                  |
| Hardened TS-UMOSFET      | \(Al_2O_3\)          |
|                          | \(Si_3N_4\)          |
|                          | AlN                  |

| Type                     | \(V_{a,supply}(V)\) |
|--------------------------|----------------------|
|                          | 55                   |
| Standard UMOSFET         | Y                    |
| TS-UMOSFET using SiO\(_2\) | N                  |
| Hardened TS-UMOSFET      | \(Al_2O_3\)          |
|                          | \(Si_3N_4\)          |
|                          | AlN                  |

| Type                     | \(V_{a,supply}(V)\) |
|--------------------------|----------------------|
|                          | 60                   |
| Standard UMOSFET         | Y                    |
| TS-UMOSFET using SiO\(_2\) | N                  |
| Hardened TS-UMOSFET      | \(Al_2O_3\)          |
|                          | \(Si_3N_4\)          |
|                          | AlN                  |

| Type                     | \(V_{a,supply}(V)\) |
|--------------------------|----------------------|
|                          | 65                   |
| Standard UMOSFET         | Y                    |
| TS-UMOSFET using SiO\(_2\) | N                  |
| Hardened TS-UMOSFET      | \(Al_2O_3\)          |
|                          | \(Si_3N_4\)          |
|                          | AlN                  |

| Type                     | \(V_{a,supply}(V)\) |
|--------------------------|----------------------|
|                          | 68                   |
| Standard UMOSFET         | Y                    |
| TS-UMOSFET using SiO\(_2\) | N                  |
| Hardened TS-UMOSFET      | \(Al_2O_3\)          |
|                          | \(Si_3N_4\)          |
|                          | AlN                  |

**Note.**

*Y = SEB is present, N = SEB is absent.*
voltages. In addition, figures 14(a) and (b) represent the drain currents of TS-UMOSFET and HK TS-MOSFET at different biased conditions after an ion strike with a LET of 0.6 pC/μm. The SEB occurred at a drain voltage of 53 V for TS-MOSFET, while no SEB was observed at 50 V. As for the proposed structure, the SEB threshold voltage was 67 V, but at 64 V no SEB was recorded. However, at a critical LET value, the proposed structure generated a greater SEB threshold voltage with an improved percentage of 26.41%. Although the proposed structure increased the SEB threshold voltage, the power performance needs to be considered to use as a practical device in the applications.

4. Conclusion

The SEB performance of TS-UMOSFET was assessed for various possible high-κ dielectric gate oxide materials. The 2-D numerical simulation employed in this study predicted a shift in the threshold and breakdown voltage for high-κ dielectrics with fixed layer thickness. Based on the findings, high-κ dielectrics significantly reduced the amount of electric field and drain current during the heavy ion strike compared to conventional SiO$_2$ gate dielectric. The simulation results also indicated that (AlN) is a promising material for SEB hardened TS-UMOSFETs to maintain the improved SEB performance and electric characterisation. Since the SEB threshold voltage for HK TS-UMOSFET was recorded at 67 V compared to 53 V for TS-UMOSFET that were obtained at

Figure 14. Analysis of drain current versus time under different drain voltages at ion strike (LET = 0.6 pC/μm) (a) Conventional TS-UMOSFET (b) Proposed HK TS-UMOSFET.

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the same LET value of 0.6pC/\mu m, the proposed device demonstrated high resistance towards SEB compared to the standard power UMOSFET.

Acknowledgments

This research was funded by Yayasan UTP Fundamental Research (YUTP) under grant number 015LC0-069. The authors would like to thank Universiti Teknologi PETRONAS (UTP), Malaysia for supporting this work.

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