Analysis and Design of a Transformerless Boost Inverter for Stand-Alone Photovoltaic Generation Systems

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Abstract—A novel transformerless boost inverter for stand-alone photovoltaic generation systems is proposed in this paper. The proposed inverter combines the boost converter with the traditional bridge inverter. The switch S₁ not only realizes the boost function but also participates in inverting process. The inverter has a higher voltage gain and good characteristics when the inductor L is operated in discontinuous mode (DCM) and the nonpolarized capacitor can be chosen as bus capacitor, which makes the volume smaller and the service life of the inverter is increased. The inverter consists of five switches in which only two switches are operated at high frequency state and a monopole sinusoidal pulse width modulation (SPWM) strategy is used. Therefore, the modulation strategy of switches is very simple and the switching loss is reduced. The principle of inverter is described in detail and mathematical models are built by small-signal analysis. Finally, the correctness of the theoretical analysis is verified by simulation and experiment.

Index Terms—Boost inverter, discontinuous mode (DCM), monopole sinusoidal pulse width modulation (SPWM), nonpolarized capacitor, photovoltaic generation systems, transformerless.

I. INTRODUCTION

In the last ten years, the photovoltaic (PV) power systems have become very popular among the renewable energy sources[1]–[28]. Normally, the inverter is the key interface between the solar cells and the AC load. However, the output voltage of the PV systems is generally low. Consequently, inverters need to have the ability to boost the output voltage of PV in order to maintain a stable AC voltage for the load [1]–[2].

The traditional voltage source inverter is a step-down inverter. When the input voltage is low, the traditional voltage source inverter is usually added a DC-DC boost circuit at its front stage. So the step-up inverter can be realized by cascading the DC-DC converter and the traditional full bridge inverter [3]. However, due to the large number of switching devices, complex control strategy and higher cost in this two stages inverter. The flyback micro-inverter can step up the input voltage, and isolate the output and the input. However, the volume and cost of the inverter are relatively high due to the existence of transformers. Some single stage boost inverters are studied in [1]–[20], for example: Z source inverter [4]–[5], double Boost inverter [8]–[9], double Cuk integrated inverter [10]–[11], Buck-Boost integrated inverter [12]–[13] and so on. The typical Z source inverter can achieve the function of the boost by using the controlled direct connection of the upper and lower bridge arm power switches. However, it has many disadvantages, such as complex topology, starting shock and oscillation, voltage gain restricted by duty cycle and modulation ratio. The inverter is a combination of two improved Cuk DC converters by input series and output parallel in [10]. By setting the appropriate regulator, the inverter can obtain good dynamic and static performance. However, the inverter requires two independent input power supplies and two independent boost inductors, which leads to low utilization rate of power source and the large volume of the circuit. Moreover, the voltage gain of the inverter circuit is low. The inverter proposed in [11] is composed of an inverting and a non inverting Cuk converter. Due to the inherent up-down voltage capacity of the Cuk converter, the output voltage can be higher or lower than the input voltage. But the inverter has six switches and four switches are operated at high frequency, so it is a challenge to improve the efficiency of the inverter.

A new boost transformerless photovoltaic inverter is proposed in this paper, which integrates boost converter with the traditional full bridge inverter. The inverter has characteristics of high gain, high integration, few power devices and easy to control. Moreover, the proposed inverter adopts monopole sinusoidal pulse width modulation (SPWM) strategy to realize the voltage pumping and the control of output voltage.

II. A NOVEL TRANSFORMERLESS STEP-UP INVERTER

A. The Topology of Proposed Inverter

This paper presents a boost transformerless inverter topology,
The filter inductor \( R \) is an integral component. The capacitors are also essential, and the control signal of the switch \( S \) involves a modulation wave with the triangle wave as the carrier wave. SPWM and the modulation strategy is shown in Fig. 2.

**B. Analysis of Operational Principle**

The power switches of the inverter are based on monopole SPWM and the modulation strategy is shown in Fig. 2. The SPWM signal used by the switch \( S_1 \) is generated by the comparison of the absolute value of the sine wave as modulation wave with the triangle wave as the carrier wave. The control signal of the switch \( S_1 \) is the same as that of the \( S_i \), when it works in the positive half cycle of sine wave. While it is turned off in the negative half cycle of the sine wave.

The proposed inverter operates in discontinuous current mode of boost inductor. Table I shows the switching sequence of the proposed inverter in one switching cycle. There are six operating modes in one switching cycle. The six operating modes of the circuit are shown in Fig. 3. The mode I, II and III operate in the positive half period of the output voltage. While the mode IV, V and VI operate in the negative half cycle. The respective analysis is as follows and the key waveforms of the proposed inverter in discontinuous mode (DCM) are shown in Fig. 4.

The power switches \( S_1 \) and \( S_2 \) operate at high frequency in the positive half cycle. So they are in the alternating state of turn-on and turn-off. The power switches \( S_3 \) and \( S_4 \) are in turn-off state and the power switch \( S_5 \) is conducted. The circuit has six modes of operation.

**Mode I \([t_0-t_1]\)** The equivalent circuit is shown in Fig. 3(a). At \( t = t_0 \), the switches \( S_1 \), \( S_2 \), \( S_3 \) and \( D_1 \) are turned on. While the switch \( S_4 \) and \( S_5 \) are turned off. At this moment, the input DC power \( U_{in} \) charges the inductor \( L_1 \) through the \( D_1 \) and the power switch \( S_1 \). The inductance current \( i_{L1} \) increases linearly. The capacitor \( C_1 \) charges the inductor \( L_2 \) and supplies power to the \( R_0 \) through switches \( S_2 \) and \( S_4 \).

\[
i_{L1}(t) = \frac{U_{in}}{L_1}(t - t_0) + \frac{U_{in}}{L_1}i_{L1}(t_0)
\]

**Mode II \([t_1-t_2]\)** The equivalent circuit is shown in Fig. 3(b). At \( t = t_1 \), the switch \( S_1 \) and diode \( D_3 \) are turned on. Switches \( S_2 \), \( S_3 \), \( S_4 \) and \( S_5 \) are turned off. At this moment, the \( U_{in} \) and \( L_1 \) charge \( C_1 \) through the \( D_1 \) and \( D_3 \). The \( i_{L2} \) can not change suddenly at the load terminal. So \( L_2 \) continues to charge \( R_0 \) through \( D_3 \). At the moment of \( t_2 \), \( i_{L2} \) is linearly reduced zero.

\[
i_{L1}(t) = \frac{U_{in} - U_{C1}}{L_1}(t - t_1) + \frac{U_{in} - U_{C1}}{L_1}i_{L1}(t_1)
\]

**Mode III \([t_2-t_3]\)** The equivalent circuit is shown in Fig. 3(c). At \( t = t_2 \), the switch \( S_1 \) is still turned on. Switches \( S_2 \), \( S_3 \), \( S_5 \) and \( S_4 \) are turned off. At this moment, there is no charging loop because the inductance current \( i_{L3} \) is zero. The inductor \( L_2 \) continues to charge the load \( R_0 \) through the body diode \( D_3 \) until \( t_3 \) and the mode III ends.

\[
i_{L1}(t) = 0
\]
**Mode IV** \[t_4-t_5\] The equivalent circuit is shown in Fig. 3(d). At \(t = t_4\), switches \(S_1, S_2\) and \(S_4\) are turned on. While \(S_1, S_2\) and \(S_6\) are turned off. At this moment, \(U_{in}\) charges \(L_1\) through the diode \(D_1\) and the switch \(S_5\). The \(i_{L1}\) increases linearly. The capacitor \(C_1\) charges the inductor \(L_2\) and supplies power to the \(R_3\) through switches \(S_1, S_2\) and \(S_3\). At \(t = t_5\), the mode IV ends.

\[
i_{L1}(t) = \frac{U_{in}}{L_1}(t - t_4) + i_{L1}(t_4) \tag{4}
\]

**Mode V** \[t_5-t_6\] The equivalent circuit is shown in Fig. 3(e). At \(t = t_5\), switches \(S_1, S_2\) and \(S_3\) are turned on while switches \(S_1, S_2\) and \(S_6\) are turned off. At this moment, the input power \(U_{in}\) and \(L_1\) charge \(C_1\) through \(D_1\) and \(D_3\). The \(i_{L2}\) can not change suddenly at the load terminal, so the inductance \(L_2\) continues to charge \(R_3\) through \(S_1, S_2, S_3\). At the moment of \(t_6\), the \(i_{L2}\) is linearly reduced zero and the mode V ends.

\[
i_{L2}(t) = \frac{U_{in} - U_{out}}{L_2}(t - t_5) + i_{L2}(t_5) \tag{5}
\]
The equivalent circuit is shown in Fig. 3(f). At $t = t_6$, switches $S_1$ and $S_3$ are still turned on. Switches $S_1$, $S_2$, and $S_4$ are turned off. At this moment, there is no charging loop because the inductance current $i_L$ is zero. $L_2$ continues to charge $R_o$ through $S_3$ and $D_{S4}$ until $t_7$ and the mode VI ends.

$$i_L(t) = 0$$  \hfill (6)

### III. Voltage Gain and Parameters of the Proposed Inverter

#### A. Analysis of Voltage Gain

From the above analysis, one can see that the duty cycle $d_i$ of the signal $S_1$ in each carrier period varies. Assuming that the duty ratio of $S_1$ is $d_i$ in $i$ carrier cycle. The $m$ is the modulation ratio. According to the regular symmetry sampling rule in [21], the duty cycle can be expressed as (7).

$$d_i = msin\omega t_i$$  \hfill (7)

Since the inductance $L_1$ of the inverter operates in DCM, the $i_L$ reaches the maximum value $I_{L,P}$ at the moment of $t_i$ and drops to zero when the time is $t_c$. The current $i_L$ remains zero between the time of $t_2$ and $t_3$. As you can see from Fig. 5, the formula can be obtained as follows: $d_i'' = (t_2 - t_i)/T_s, d_i + d_i'' < 1$.

According to the voltage second balance of inductor $L_1$, the following equation can be expressed as:

$$U_{i}d_iT_s = (U_{C1} - U_{i})d_i'T_s.$$  \hfill (8)

If the loss of all components in this circuit is neglected, the input power is equal to the output power and thus the formula can be obtained as:

$$U_{i}I_{i} = (U_{C1}/\sqrt{2})^2 R_o.$$  \hfill (9)

where $U_{i}$ is amplitude of the output voltage of the inverter.

It can be expressed as: $U_{i} = mU_{C1}$. Since the input average current is equal to the inductance average current, the following equations can be written as:

$$I_i = I_{i1},$$  \hfill (10)

and the average value of $i_L$ can be obtained as:

$$I_{i1} = (d_i + d_i'')I_{L,P}/2.$$  \hfill (11)

According to (8)–(11), the equations of the input voltage and the DC bus voltage can be derived as:

$$\frac{U_{i}}{U_{in}} = \frac{1}{2} \left(1 + \sqrt{1 + \frac{4d_i'^2 T_s R_o}{L_1 m}}\right).$$  \hfill (12)

The $d_i$ is taken as the valid value and the voltage gain can be expressed as:

$$G = \frac{U_{i}}{U_{in}} = \frac{m}{2} \left(1 + \sqrt{1 + \frac{2T_s R_o}{L_1}}\right).$$  \hfill (13)

Fig. 6 shows the three-dimensional relationships of voltage gain $G$ versus inductance $L_1$ and modulation ratio $m$ when $f_S = 20 \text{ kHz}, R_o = 100 \Omega$ are given. As can be seen from Fig. 6, the $G$ increases when the $m$ increases or the $L_1$ decreases.

#### B. Range of Modulation Ratio $m$

The range of modulation ratio $m$ is discussed based on the open-loop condition. According to (8), the $d_i''$ can be obtained as:

$$d_i'' = \frac{U_{i}}{U_{C1} - U_{i}}.$$  \hfill (14)

Because $d_i + d_i'' < 1$, the duty cycle $d_i$ can be expressed as:

$$d_i < \frac{1}{\frac{U_{i}}{U_{C1} - U_{i}} + 1}.$$  \hfill (15)
According to (7), \( \sin \omega t_i \in (0, 1) \), the range of modulation ratio \( m \) can be derived as:

\[
m < \frac{1}{U_{in}/(U_{C1} - U_{in}) + 1}.
\]

When the intermediate variable \( U_{C1} \) is represented by an independent variable \( m \). According to (16), the range of modulation ratio \( m \) can be derived as:

\[
m < \frac{U_{in}}{U_{in} + U_{out}}.
\]

### C. The Value of Boost Inductor

In order to ensure the inverter is operated in DCM, the critical inductance of the boost inverter is derived firstly.

When the boost inductor works in DCM, the inductance current is exactly zero at the start and at the end of each switching cycle. The average current of inductance is equal to half of the variation of inductance current. It is assumed that the threshold inductance is \( L_C \). According to (10) and (11), the following equation can be expressed as:

\[
I_{in} = I_{br}/2.
\]

The formula between current and voltage is as follows:

\[
I_{br} = U_{in} d_1 T_s / L_C.
\]

According to (9), (18) and (19), the following equation can be derived as:

\[
U_{in} d_1 T_s / (2L_C) = m^2 U_{C1} / (2R_C U_{in}),
\]

The critical inductance \( L_C \) can be obtained as:

\[
L_C = \frac{U_{in} d_1 T_s R_C}{I_{br}^2}.
\]

As we can see from (21), \( L_C \) is related to input voltage, load and modulation ratio. In order to ensure the inductor current is always discontinuous throughout the entire range of \( U_{in} \). The value of the inductor should be less than \( L_C \). The three-dimensional image of the inductance \( L_C \) is shown in Fig. 7, in which \( d_1 = 0.7, f_s = 20 \text{kHz}, U_{in} = 155 \text{V} \).

### D. Design of the Bus Capacitor

During the operation of the boost inverter, the design of the capacitor mainly considers the voltage stress and the maximum acceptable voltage ripple across it. The capacitor is charged and discharged continuously with the change of the power switch state. The relation between the charge quantity and the capacitance value is satisfied as follow:

\[
\Delta Q = C \Delta U_{C1} = I_C \Delta T.
\]

In a switching cycle, \( \Delta Q \) is the quantity of charge during charging or discharging process of capacitors. \( \Delta U_{C1} \) is the value of the capacitor voltage ripple. \( I_C \) is the average current of capacitor during charging or discharging process. \( \Delta T \) is the charging time or discharging time. Therefore, the value of the capacitor can be selected according to (23), in which \( P_o \) represents the output power.

\[
C_1 \geq \frac{P_o d_1}{(U_{C1} - U_{in}) \Delta U_{C1} f_s}.
\]

In order to ensure the performance of the inverter, the value of capacitor voltage ripple is limited to 1% of \( U_{C1} \). Thus, the value of \( C_1 \) should be greater than 15 \( \mu \text{F} \). The capacitor value of the inverter is selected for 47 \( \mu \text{F} \).

### E. Design of Filter Inductor and Capacitor

The design method of filter inductance and capacitor is \( K \) low-pass filter in proposed inverter refer to the design in reference [22]. This design method can be expressed as: \( K = R^2 = L/C, R = (0.5 - 0.8) R_o \).

The cut-off frequency \( f_c \) is increased by 10 times, which is the carrier frequency \( f_s \). And then:

\[
L = \frac{R}{2 \pi f_c},
\]

\[
C = \frac{1}{2 \pi f_c R}.
\]

It is calculated that the value of \( L_2 \) is 3.7 m\( \text{H} \) and the value of \( C_2 \) is 1.3 \( \mu \text{F} \). Therefore, the value of filter inductance and filter capacitor is respectively 3 m\( \text{H} \) and 10 \( \mu \text{F} \) in proposed inverter.

### IV. INVERTER MODELING AND CONTROLLER DESIGN

#### A. Inverter Modeling

This paper builds a state space averaged model to obtain a linearized model of the proposed inverter. In addition, designing a suitable controller to achieve good steady-state performance and dynamic characteristics by small-signal analysis. To simplify the analysis, following assumptions are made. Components including capacitors and inductors are ideal.
devices, regardless of the effects of parasitic parameters and the initial conditions of elements are zero. Inductor currents ($i_L1$, $i_L2$) and capacitor voltages ($U_{C1}$, $U_{C2}$) are considered as state variables $x$.

$$x = \begin{bmatrix} i_{L1} & i_{L2} & U_{C1} & U_{C2} \end{bmatrix}^T$$  \hspace{1cm} (26)

The input voltage ($U_{in}$) is selected as the input variable $u$, and the output voltage ($U_O$) is the output variable $y$, and the state space equation can be written:

$$\begin{align*}
\dot{x} &= Ax + Bu, \\
y &= Cx.
\end{align*}$$  \hspace{1cm} (27)

The expressions for the state variables during three operating modes are given in Table II.

For easier analysis, the duty ratio weighting factor of the converter mode I is $D_1$, the duty ratio weighting factor of the mode II is $D_2$, and the duty ratio weighting factor of the mode III is $D_3$. By using the average state space method, the coefficient matrices $A$, $B$ and $C$ can be calculated by the following formulas:

$$A = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & \frac{D_1}{L_2} & -\frac{1}{L_2} \\
\frac{D_2}{C_1} & \frac{D_2}{C_1} & 0 & 0 \\
0 & \frac{1}{C_2} & 0 & -\frac{1}{R_{C_2}}
\end{bmatrix}$$  \hspace{1cm} (28)

$$B = \begin{bmatrix} D_1 & D_2 & 0 & 0 & 0 \end{bmatrix}^T$$  \hspace{1cm} (29)

$$C = [0 \ 0 \ 0 \ 1].$$  \hspace{1cm} (30)

Perturbations in the steady-state values of state variables and the duty cycle are as follows:

$$\begin{align*}
x &= X + \hat{x} \\
d_1 &= D_1 + \hat{d}_1 \\
d_2 &= D_2 + \hat{d}_2 \\
u &= U + \hat{u} \\
y &= Y + \hat{y}
\end{align*}$$  \hspace{1cm} (31)

where $\hat{x}$, $\hat{d}_1$, $\hat{d}_2$, $\hat{u}$, $\hat{y}$ are the state variable $x$, the duty cycle $d_1$, the duty cycle $d_2$, the input voltage $u$, and the disturbance component near the $y$ static operating point. Substituting (31) into (8), the relationship between $\hat{d}_1$ and $\hat{d}_2$ can be obtained as follows:

$$\hat{d}_1 = \frac{U_{C1} - U_{in}}{U_{C1} - U_{in}}.$$

### Table II

| Mode I       | Mode II ($i_{L1} > 0$) | Mode III ($i_{L1} = 0$) |
|--------------|------------------------|-------------------------|
| $U_{in}$     | $U_{C1}$               | $U_{C1}$                |
| $i_{L1}$     | $i_{L1}$               | $i_{L1}$                |
| $i_{L2}$     | $i_{L2}$               | $i_{L2}$                |

Substituting (31), (32) into (27) and writing $\hat{d}_i$ in terms of $\hat{d}_1$ and neglecting higher order terms, small-signal AC model represented in matrix form is obtained as:

$$\begin{align*}
\dot{x} &= A\hat{x} + B\hat{u} + Ed, \\
y &= C\hat{x},
\end{align*}$$  \hspace{1cm} (33)

where the coefficient matrices $A$, $B$, $E$ and $C$ can be calculated by the following formulas:

$$A = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & \frac{D_1}{L_2} & -\frac{1}{L_2} \\
\frac{D_2}{C_1} & \frac{D_2}{C_1} & 0 & 0 \\
0 & \frac{1}{C_2} & 0 & -\frac{1}{R_{C_2}}
\end{bmatrix}$$  \hspace{1cm} (34)

$$B = [0 \ 0 \ 0 \ 0]^T$$  \hspace{1cm} (35)

$$E = \begin{bmatrix} 0 & U_{in} & \frac{i_{L2}}{C_1} + \frac{U_{in}i_{L1}}{C_1(U_{C1} - U_{in})} & 0 \end{bmatrix}$$  \hspace{1cm} (36)

$$C = [0 \ 0 \ 0 \ 1].$$  \hspace{1cm} (37)

Based on the small signal model given by (33) and the control ($d$) to output voltage ($U_O$) transfer function $G_p(s)$ is obtained as follow:

$$G_p(s) = \left. \frac{Y(s)}{D(s)} \right|_{d(s) = 0} = \left. \frac{U_O(s)}{D(s)} \right|_{d(s) = 0} = C(SI - A)^{-1}E$$  \hspace{1cm} (38)

Using the parameters given in Table III, the transfer function $G_p(s)$ can be obtained as (39).

$$G_p(s) = \frac{U_O(s)}{D(s)} = \frac{4.68 \times 10^9 S + 1.673 \times 10^{12}}{S^3 + 7 \times 10^3 S^2 + 5.88 \times 10^5 S + 2.36 \times 10^7}$$  \hspace{1cm} (39)

### B. Controller Design

In addition, it is necessary to design a suitable controller.
to achieve a good steady-state performance and dynamic characteristics. PR controller is advantageous in tracking sinusoidal signals as it provides a high gain at grid frequency, thereby eliminating the steady state error [23]. Fig. 8 shows the block diagram representation of the voltage control loop including the PR controller \( G_p(s) \). As shown in Fig. 8, these delays are added and incorporated into the control loop as \( e^{-T_d s} \), where \( T_d = 0.75 T_c \). To minimize the steady state error at grid frequency, PR controller is tuned to grid frequency of 50 Hz. This ensures high loop gain at the grid frequency. The transfer function is as follow:

\[
T_c(s) = \frac{S^2 + \xi_o \omega S + \omega^2}{S^2 + \xi_o \omega S + \omega^2},
\]

where \( \omega \) is the required frequency, \( \xi_o \) and \( \xi_p \) are the damping coefficients [24].

The controller gain depends on the ratio of the damping coefficients. For a steady state error of 0.1%, values of \( \xi_o \) and \( \xi_p \) are obtained as 1 and 0.5 respectively.

The Bode plot of \( G_p(s) \) and the open loop gain \( G(s) = G_L(s) \times e^{-T_d s} \times G_p(s) \) are shown in Fig. 9. It can be seen that the gain is high at resonant frequency, which is the grid frequency and hence, the steady state error is negligible at grid frequency.

V. SIMULATION AND EXPERIMENTAL VERIFICATIONS

In order to verify the correctness of the feasibility and theoretical analysis of the proposed boost inverter in this paper, the simulation is carried out firstly. Then, an experimental prototype taking DSP320F2812 as core controller is built to verify the performance of inverter. The specific parameters are shown in Table III. Fig. 10 shows the external view of the prototype.

VI. CONCLUSIONS

A transformerless boost inverter topology for stand-alone photovoltaic generation systems is proposed in this paper, which can work in a wide input voltage range. The integrated boost inverter can be derived from a boost converter and a full bridge inverter by multiplexing the switch of basic boost converter. In the proposed inverter, only one power device is operated at high frequency in a line frequency cycle, the other one is operated at high frequency in half cycle, and the rest switches are all operated in low frequency of 50 Hz. In addition, values of the boost inductor \( L_1 \) and the bus capacitor \( C_b \) can be designed to be very small so that the volume and the cost of the circuit are significantly reduced. The operating principle and steady-state characteristics of the inverter are analyzed in detail when the input inductor current is designed in DCM. The correction of the theoretical analysis is proved by
Fig. 11. Experimental waveforms. (a) $u_{g,S1} - u_{g,S5}$. (b) $u_{ab}$, $i_L / i_{in}$. (c) $u_{C1}$, $u_O$. (d) $i_O$, $i_{L2}$.

Fig. 12. Experimental waveforms of the power switches.
Fig. 13. The efficiency curves for different conditions.

| TABLE IV | COMPARISON OF SINGLE-STAGE INVERTER TOPOLOGIES |
|----------|-----------------------------------------------|
| Topology | Components & Devices | THD (%) | Max.eff (%) |
| [25]     | 4 3 3 2 | 4 | 91.3 |
| [26]     | 6 0 2 2 | 4 | 92.6 |
| Proposed | 5 1 2 2 | 1.8 | 96.2 |

the experimental waveforms.

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