Improving the functionality of the semiconductor matrix receiver of optical radiation

A A Shnyakin, E Ph Pevtsov, T A Demenkova

Associate professor, MIREA - Russian Technological University, Moscow, Russia
E-mail: pevtsov@mirea.ru

Abstract. The work is devoted to improving the functionality of the semiconductor integrated matrix receiver of visible range radiation with a capacitor multichannel analog-to-digital Converter on a chip. Reading is carried out by a column capacitor of sequential approximation with a digital-analog converter based on switched capacitors DAC with charge summation. In the matrix receiver, the occupied area and the dissipated power of the semiconductor chip are significantly reduced with the simple implementation of capacitor structures by the technology of semiconductor micro-devices manufacturing.

1. Introduction

Analysis of papers on metal-oxide-semiconductor (CMOS) image sensors reveals current developmental trends aimed to combine functions of converting radiation into electrical signals, digitizing them and digital processing in a single chip or package [1‒3].

There are three main approaches as regards placing an ADC in a readout integrated circuit chip, that is, a chip-level ADC, a column-level ADC and pixel-level ADC. Column-level ADCs may have complex architecture and combine various ways of analog-to-digital conversion since its layout implementation is only one-dimension limited and is not limited in other one. The speed of such ADCs is comparable to the rows’ readout rate of a readout IC which positively affects power consumption. Thus, using a column-level ADC implies balancing such factors as speed, conversion accuracy, power consumption and chip area [4, 5].

The main goal of this work was to prototype ADC IP-core intended for reuse in different families of CMOS image sensors. The circuitry and layout of resulting design solutions are determined by the following main factors: optimization of production costs and detectors’ characteristics; minimization of the area occupied by ADC units; minimization of power consumption upon reaching at least twelve bits of conversion for at least 1.0 MHz clock frequency and 77000 op/sec working speed.

2. Condenser multi-channel ADC

Widely used optimal solution for the ADC in the composition of the semiconductor structures for complementary CMOS receivers is a diagram of a successive approximation ADC based on a digital-to-analog converter Binary-Weighted capacitor DAC, capacitance which is a multiple of a power of two. This is due to the relative ease of implementation of capacitor structures in the framework of standard technological processes of modern VLSI. The main disadvantage of this solution is the area of capacitor structures, increasing with the growth of the conversion bit width. Accordingly, the currents required for charging and discharging them and the dissipated power increase significantly.
The peculiarity in the proposed version of the ADC in which an attempt is made to correct this drawback is that where the DAC circuit is made with three subunits of weighing capacitors, each subunit is supplied with different reference voltages, the values of which correspond to a certain range of the conversion bit width [6].

The composition of the ADC includes: voltage comparator, parallel DAC on switchable capacitors with charge summation and digital control circuit (successive approximation register). The main elements of the DAC are: a matrix of weighting capacitors with switchable keys and an operational amplifier with a capacitor and a key in the negative feedback circuit.

The basis for the design of the topology of the complex functional ADC module was the PDK (process design kit), the base gate width of the transistor cell of which was 0.54 $\mu$m. Multiple ratios between the capacitance values of the capacitors are provided by multiplying the cell of the dual capacitor, and the subsequent parallel Association of the multiplicated fragments of the topology in accordance with the required capacitance value.

Simulation of the ADC electrical circuit Assembly was carried out using models of devices included in the customer-provided library of parameterized cells, CMOS-oriented technology with design standards of 0.35 $\mu$m.

The simulation with the extracted parasitic parameters of the topology is obtained, that the conversion efficiency is up to 10 bits without correction. When adjusting the DAC by varying the reference voltage and the mixing voltage, the ADC efficiency can be increased to 11-12 bits.

The design solutions and GDS-files of the topology of successive approximation column ADCs intended for placement on a chip with CMOS photomatrix are obtained.

3. Analyzing Test Chip Characteristics

In order to analyze test chips for the ADC IP-core and CMOS image sensors, a hardware and software was developed that allows recording automatically dynamic and static characteristics of the tested devices and their components. Structure of the test equipment is shown in Figure 1.

![Figure 1. Schematic structure of the test stand.](image)

The main stand element is the process controller, made as Spartan 3E family FPGA chip firmware. The main functions of the controller are the following: 1) to control the DAC; 2) to collect data from the tested ADC; 3) to form a clock cycle and output signals to synchronize the external ADC which is used to measure parameters of the device under test. To describe the controller behavior, the VHDL language and the standard XILINX libraries were used. Software set for testing the ADC provides adjustment of reference voltages, creating a description of the clock diagram and its loading into the
generator’s memory, programming the FPGA, data collection and display. Software includes: a program for setting modes and measuring parameters, a clock pattern editor, tools for controlling operation of the InSys ADM216x100M external ADC and displaying the obtained data. Device resolution can be programmed for 20 bits with output voltage accuracy up to 0.003 % reached within 15 ms.

Analyzing test chips of the ADC IP-core was carried out as follows. First of all, operability of each sample was confirmed by sequentially switching each of the three DAC units as a Most Significant Bit Block, meanwhile the remaining units were disabled. When supplying alternately each unit under test with 1.5 V as the reference voltage and 2.5 V as the common reference voltage, the ADC input voltage from the test stand DAC varying within the 2.5316 V to 3.43785 V range in 0.0156 V increments, the results for each tested unit at the DAC reference output point of the tested ADC were the same within the measurement error. Data from the ADC digital outputs were also identical. Operation of the ADC as a whole was tested with normal switching of all three capacitor units and the calculated from expressions reference voltages for the input signal varying all over the range of input voltages.

Studying linearity characteristics of the DAC circuit showed significant deviation from the required and calculated values (Figure 2) due to stray capacitances between digital control lines and the common bus of capacitor structures in each of the twelve digital units of switch control, storage and output which was ignored during the initial design.

![Figure 2. Fragment of the DAC transfer characteristic.](image)

A layout chart fragment of a digital unit with marked places where stray capacitive couplings were formed is shown in Figure 3.

![Figure 3. Layout chart fragment of a digital unit of switch control, storage and output.](image)

The DAC circuit linearity characteristics are negatively affected by capacitive parasitic cross-talks of switch control digital buses and the common bus of capacitor structures which was confirmed by the results of measurements upon specifying certain conditions. If reference voltages are applied to the ADC inputs, the DAC output voltage must remain unchanged for any combination of control signals.
As a result, it was decided to eliminate capacitive parasitic cross-talks by grounded shielding metallization layer between digital control buses and the common bus of capacitor structures. However, experiments of the test chips’ sample quantity of the layout adjusted ADC IP-core revealed complete failure for all the investigated samples containing a single column of the ADC IP-core. By comparing layout by means of the DRC and LVS CAD (Figure 4a), and the test chip layout by means of optical and electron microscopy (Figure 4b), the cause of the failures was found to be defects which caused short-circuiting of the external control enable bus and the supply voltage bus.

![Figure 4. Localization and elimination of circuit closure.](image)

To eliminate the identified defects, a method to correct test chip layout by means of ion-beam etching and ion-stimulated deposition based on focused ion beam (Figure 4b) was developed and applied in practice.

Optimization of ion beam formation allowed getting images of underlying metallization layers to adjust on a chip and localize short-circuiting of conduct buses without complete removal of a passivation layer. By means of ion-beam etching, all layers of inter- and intra-layer dielectrics were opened, and the short circuited section of the bus was separated. Then, by means of ion-stimulated deposition in a special installation with sharply focused ion beam (NanoLab complex with FIB), previously damaged integrity and conductivity of the control bus has been restored by a platinum layer. In this way, the technique aimed to restore working capacity of ADC chips was tested.

Analyzing chips of the second revision showed that the proposed change in the layout chart where influence of stray capacitive coupling was eliminated by introducing a grounded screen metallization layer, allowed to significantly reduce the DAC output voltage deviations (Figure 5) which as a result led to adjustment of data in the DAC transfer characteristic (Figure 6).
4. Conclusion
The main characteristics of a capacitor multichannel analog-to-digital Converter in a semiconductor integrated circuit of a matrix radiation receiver are investigated. Circuit and layout solutions for a 12-bit column-level ADC were developed which allowed performing conversion in 12 cycles. When using the 0.5 μm CMOS technology level, the frame rate for the 1024×1024 pixel array is 75 Hz, while using the 0.18 μm technology level it will reach 1 kHz. The main design problems are related to strictly limited power consumption, limited ADC layout sizes (30 μm width for 15×15 μm² cells and dual-sided arrangement of ADCs) and the need to minimize stray capacitances that strongly affect conversion accuracy. To reduce the area of a capacitor divider, the ADC uses a novel three-stage circuit with three weighted reference voltage sources.

Acknowledgments
This work was supported by the Ministry of Education and Science of Russian Federation (project 8.5098.2017/8.9 basic part of the State task)

References
[1] Baker R J et al 1997 CMOS Circuit Design, Layout, and Simulation, Wiley-IEEE Press.
[2] Normanov D, Osipov D 2013 Proceedings of the 12th WSEAS International Conference on Circuits, Systems, Electronics, Control & Signal Processing (CSECS ’13) Budapest. 90-94
[3] Pevtsov E Ph et al 2017 IOP Conf. Ser.: Mater. Sci. Eng. 168 012095. doi: 10.1088/1757-899X/168/1/012095
[4] Ilan E et al 2013 Proc. SPIE 8659 A-1-0A-6. doi: 10.1117/12.2002845
[5] Gao L et al 2012 Proc. SPIE 8562 10-1-10-6. doi: 10.1117/12.981856
[6] Borodin D V, Osipov Yu V 2017 Television Technique series 2 25–30 (in Russian)