PC$_{70}$BM n-type thin film transistors: Influence of HMDS deposition temperature on the devices properties

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Abstract

This study investigates the influence of the deposition temperature of hexamethyldisilazane (HMDS) on the performances of organic thin film transistors (OTFTs) using the [6,6]-phenyl-C$_{71}$-butyric acid methyl ester (PC$_{70}$BM) as semiconductor. N-type OTFTs have been fabricated using this fullerene derivative, deposited from solution by drop casting technique on HMDS self-assembled monolayer (SAM) deposited at three different temperatures, 7°C, 25°C and 60°C, in order to evaluate the influence of these deposition conditions on the morphology of PC$_{70}$BM films and on the electrical responses of fullerene derivative-based OTFTs.

The effect of the treatments of the surfaces was observed through contact angle measurements. AFM imaging of the deposited material has been used to analyse its structure and morphology. The transistors performances have been evaluated through I vs. V static characterization and parameters extraction.

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Contact angle vs. HMDS deposition temperature shows the minimum value at 60°C, instead field effect mobility presents a maximum. It has been observed that the lower hydrophobicity of the surface of the SAM induces the formation of more homogeneous surface of the PC\textsubscript{70}BM film, resulting in an increase of the OTFTs performances.

*Keywords*: OTFTs, PC\textsubscript{70}BM, HMDS, SAM, Organic electronics.

### 1. Introduction

A critical issue of the Organic Electronics technology is the fabrication of CMOS-like circuits, because of the difficulties to obtain good performances and stability from the n-type organic thin film transistors (OTFTs) compared to the p-type ones.

It is well known that performances of transistors based on organic molecules strongly depend on different parameters, such as the molecular order, the morphology, the grain boundaries within the active semiconductor layer, etc. These factors can be well controlled by different ways, for example by varying the wafer cleaning procedures [1-4], the deposition rate of the organic layer [5], the substrate temperature during the depositions [5-7] and applying surfaces modification using the so-called self-assembled monolayers (SAM) [8,9]. Moreover, the quality of the semiconductor channel can be strongly influenced by the surface conditions, which, for a bottom-gate bottom-contacts (BGBC) OTFT, is the gate insulator.

For these reasons, in this work, n-type OTFTs have been studied, using the fullerene derivative [6,6]-phenyl-C71-butyric acid methyl ester (PC\textsubscript{70}BM) as the semiconductor. This molecule is soluble in various organic solvents, allowing an easy deposition from solution [10], and so being potentially much advantageous in the area of the large-area organic electronics [11-13]. Here, the hexamethyldisilazane (HMDS) has been used as a SAM, and the effects of its deposition temperature on the performances of the OTFTs have been characterized using a bottom-gate bottom-contacts (BGBC) devices configuration [14].

A two-steps surface treatment has been used, to modify the quality of the gate insulator (Silicon dioxide, SiO\textsubscript{2}) and improve the performances of the OTFTs, applying an ultraviolet/ozone (UV/O\textsubscript{3}) cleaning followed by the SAM coating on the SiO\textsubscript{2} gate insulator. In particular, UV/O\textsubscript{3} cleaning procedure is a cheap and simple method that allows to remove organic contaminations on the dielectric surface, thanks to the formation of hydroxyl groups (-OH) generated by the UV/O\textsubscript{3} ambient [15]. This results in a more hydrophilic insulator surface. However, the presence of these groups on the surface can increase interface trap density [16,17], that can catch charge carriers, resulting in a decline of the OTFT performances. The use of a SAM, in particular the HMDS, can reduce the traps [18] induced by Si-OH groups on the gate insulators: the alkane chains of this self-assembled monolayer are able to modify the surface energy making it more hydrophobic. This results in an increase of the OTFT performances [18].

We have observed that different deposition temperatures of the SAM allow to obtain surfaces with different hydrophobic characters, resulting in OTFTs with different electric performances.

### 2. Experimental details

PC\textsubscript{70}BM-based OTFTs, with bottom-gate and bottom-contacts configuration, were fabricated on commercial substrates made of heavily doped n-type silicon, acting as the gate contact, with 200 nm thick SiO\textsubscript{2} as the gate dielectric and gold (50 nm) interdigitated contacts (W/L = 550). The substrates were exposed to UV/ozone for 20 min in a dedicated cleaner (MBRAUN UV-O\textsubscript{3} OP73), and then were treated with HMDS as a self-assembled monolayer (SAM). The HMDS was purchased from Sigma-Aldrich and used as-is. It was deposited at three different temperatures (7°C, 25°C, 60°C), keeping the samples and a reservoir of the HMDS inside a sealed container. For the deposition at 7°C, the container was maintained in a refrigerator for 4 days; the samples at 25°C were processed for 1 day; and the process at 60°C was performed for 1 day using a hot plate. Before the semiconductor deposition, all the substrates were baked on a hot plate for 1 h at 100°C in inert atmosphere (glove box, H\textsubscript{2}O < 1 ppm, O\textsubscript{2} < 1 ppm). The evaluation of the effect of the surface treatments was performed by static contact angle (CA) measurements of H\textsubscript{2}O, using a contact angle system Dataphysics OCA20 in sessile drop mode with a drop volume of 0.5 μL.
PC$_{70}$BM powder was purchased from Solenne BV. The thin films were deposited by drop casting technique from chlorobenzene solution (2 wt%) at room temperature in inert atmosphere, and their morphology was examined by atomic force microscopy (AFM Veeco NSIV model) in tapping mode. The electrical characteristics of the OTFTs were measured using a probe station CASCADE Summit 11000B-M at room temperature, keeping each sample under nitrogen flow during all the measurements. The data acquisition was done by a Keithley 4200-SCS Semiconductor Characterization System.

3. Results and discussion

The variation of the OTFTs performances, due to the treatments of the dielectric/semiconductor interface, was firstly observed by studying the surface properties of the dielectric material. The surface treatments and the contact angle measurements performed on the SiO$_2$ gate insulator are shown in table 1. The contact angle is the angle between the tangent to a drop’s profile and the tangent to the surface at the intersection of the vapor, the liquid, and the solid. The contact angle is an index of the wettability of a solid surface. A low contact angle between a solid surface and a water-drop indicates that the surface is hydrophilic and has a high surface energy. On the contrary, a high contact angle means that the surface is hydrophobic and has a low surface energy.

Table 1. Summary of the surface treatment conditions and SiO$_2$ contact angle values.

| Substrate | UV/Ozone | HMDS deposition temperature | SiO$_2$ contact angle |
|-----------|----------|----------------------------|-----------------------|
| Si/SiO$_2$/Au | Untreated | Untreated                  | 30°                   |
| Si/SiO$_2$/Au | 20 min   | Untreated                  | 3°                    |
| Si/SiO$_2$/Au | 20 min   | 7°C                        | 106.1°                |
| Si/SiO$_2$/Au | 20 min   | 25°C                       | 109.1°                |
| Si/SiO$_2$/Au | 20 min   | 60°C                       | 104.1°                |

As shown in table 1, UV/O$_3$-only treated samples showed lower contact angle values than untreated samples. When SiO$_2$ gate insulator is cleaned with UV/O$_3$ process, unstable dangling bonds with terminals hydroxyl groups can form on the insulator surface [19]. A great number of hydroxyl groups can make the SiO$_2$ surface more hydrophilic; this means to have highly polar surfaces. This hydrophilic character was well confirmed by CA values, as reported in table 1. Residual organics on the gate dielectrics are suspected to be the major source of contamination [20]. The contact angle is expected to decrease as the quantity of organic residues is reduced.

In order to decrease the surface energy of the SiO$_2$ gate insulator, and thus convert the hydrophilic surface into a hydrophobic one, we have used the HMDS. As said, HMDS can form self-assembled monolayers on SiO$_2$ surface during evaporation process of the solution, and the alkane chains in the materials changes the property of the SiO$_2$ dielectric layer from hydrophilic to hydrophobic character. In general, most inorganic oxide surfaces show hydrophilic state, while most organic semiconductors show hydrophobic state. This mismatch can influence negatively the deposition of the semiconductor layer on an oxide substrate. HMDS treatment can improve the quality of the growth of an organic semiconductor, in terms of the material crystallinity and so for the charge carrier mobility [21].

The samples treated with HMDS showed a large increase of the contact angle value, confirming that a more hydrophobic character of the surface was obtained. The images of the contact angles reported in figure 1 show the variation of the CA values after each treatment. However, as it is possible to observe from table 1 and figure 1, the different deposition temperatures of the SAM (7°C, 25°C, 60°C) allowed to obtain surfaces characterized by
different hydrophobicity. This is probably due to a different condensation behaviour of the HMDS, that varies with
the temperature deposition.

To observe the effect of the surface conditioning on the semiconductor, the atomic force microscopy (AFM)
analysis was used (figure 2). The images are related to the semiconductor films deposited on the transistors channel
area. The different hydrophobicity of the SiO₂ surface leads to obtain PC₇₀BM thin films characterized by very
different roughness, as reported in table 2. The PC₇₀BM films obtained on HMDS deposited at 7°C and 60°C, show
the most homogeneous surface, whereas the HMDS obtained at 25°C induces the formation of a very
inhomogeneous surface with high roughness. The evaporation/condensation mechanism of the HMDS SAM varies
with preparation condition, in particular with the deposition temperature, probably because the chemical action of its
terminal silane groups is more efficient during the process at 7°C and 60°C. Indeed, the reduced surface energy (i.e.,
high contact angle) for the samples obtained at 25°C, leads to increase of the number of nucleation sites, which
results in a decrease of the grain sizes and an increase of the surface roughness [22].

![Contact angle images for SiO₂ substrate treated at different condition of HMDS deposition temperatures.](image1)

![AFM images of PC₇₀BM thin films deposited on SiO₂ dielectric treated with HMDS: (a) at 7°C; (b) at 25°C; (c) at 60°C.](image2)
The homogeneous surfaces for the samples prepared at 7°C and 60°C would lead to an improved mobility of the manufactured devices. This aspect was confirmed by I vs. V static characterizations and parameters extraction.

Transfer curves of the PC_{70}BM OTFT samples obtained using the combined scheme UV/ozone and HMDS treatments are shown in figure 3. The extracted electrical parameters, such as mobility ($\mu_{\text{SAT}}$), threshold voltage ($V_t$) and on/off current ratio ($I_{\text{ON}}/I_{\text{OFF}}$), are listed in table 2. The devices fabricated without the SiO$_2$ surface treatments (one or both) are not presented, because no meaningful data were obtained during measurements.

Fig. 3. Transfer curves of PC$_{70}$BM based OTFTs obtained under various temperatures for HMDS deposition: (a) 7°C; (b) 25°C; (c) 60°C. (d) Comparison of the transfer curves at $V_{ds} = 80$ V for the three different deposition temperatures.

| Devices               | Roughness $\text{rms (nm)}$ | $\mu_{\text{SAT}}$ (cm$^2$V$^{-1}$s$^{-1}$) | $V_t$ (V) | $I_{\text{ON}}/I_{\text{OFF}}$ |
|-----------------------|-----------------------------|---------------------------------------------|--------|---------------------|
| UV/ozone 20 min + HMDS 7°C | 0.17                        | $3.47 \times 10^{-3}$                       | 22.2   | $10^6$             |
| UV/ozone 20 min + HMDS 25°C | 0.30                        | $2.5 \times 10^{-3}$                       | 10.0   | $10^3$             |
The trends of the mobility and of the threshold voltage of the OTFTs vs. the contact angle measurements and vs. the HMDS deposition temperatures are shown in figure 4.

![Fig. 4. Mobility and threshold voltage compared (a) vs. the HMDS surface contact angle, and (b) vs. the HMDS deposition temperature.](image)

The results demonstrate that the greater hydrophobicity do not imply the best mobility. Contact angle shows the highest values at 25°C temperature for the HMDS deposition, while here mobility presents a minimum. This higher hydrophobicity of the SAM induces the formation of very inhomogeneous dimensions of the PC70BM crystalline grains, as confirmed by the AFM analysis, so giving the smaller value of the mobility, because of the scattering of the charges along the devices channel.

The samples at 60°C temperature for HMDS deposition show the best OTFTs performances: this temperature allows the surface energy of the gate dielectric to be matched to the semiconductor material, so in the channel it results in a more homogeneous film and a higher charge carrier mobility.

It can be concluded that to obtain a good growth of an organic semiconductor and a tailored interface it is necessary to develop and apply specific treatments of the underlying surface, that induce a specific level of hydrophobicity, instead to simply search for the highest values of it.

4. Conclusion

In this work, n-type PC70BM bottom-gate bottom-contacts OTFTs have been prepared on silicon wafers, using silicon dioxide as insulator, and applying different conditioning to the SiO2 surface prior the semiconductor deposition. We have demonstrated that a two-steps combined scheme of UV/ozone cleaning and HMDS treatment is beneficial for the performances of the OTFTs.

The temperature of the HMDS deposition not obviously influences the growth of the following PC70BM films: the treatment at 60°C gives the best OTFTs performances, as a result of the surface hydrophobicity, resulting in the formation of homogeneous semiconductor films.

These results show the importance to fine tailor the fabrication processes to obtain the best performances of n-type PC70BM OTFTs.
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References

[1] B. J. Song, K. Hong, W. K. Kim, K. Kim, S. Kim, J. L. Lee, J. Phys. Chem. B 114 (2010) 14854-14859.
[2] J. W. H. Smith, I. G. Hill, J. Appl. Phys. 101 (2007) 044503.
[3] W. K. Kim, K. Hong, J. L. Lee, Appl. Phys. Lett. 89 (2006) 142117.
[4] Q. Qi, A. Yu, P. Jiang, C. Jiang, Appl. Surf. Sci. 255 (2009) 5096-5099.
[5] M. Shitein, J. Mapel, J. B. Benziger, R. Forrest, Appl. Phys. Lett. 81 (2002) 268-270.
[6] S. Steudel, D. Janssen, S. Verlaak, J. Genoe, P. Heremans, Appl. Phys. Lett. 85 (2004) 5550-5552.
[7] H. S. Lee, D. H. Kim, J. H. Cho, M. Hwang, Y. Jang, K. Cho, J. Am. Chem. Soc. 130 (2008) 10556-10564.
[8] T. W. Kelly, L.D. Boardman, T. D. Dunbar, D. V. Muyres, M. J. Pellerite, T. P. Smith, J. Phys. Chem. B 107 (2003) 5877-5881.
[9] C. Bock, D.V. Pham, U. Kunze, D. Käfer, G. Witte, Ch. Wöll, J Appl. Phys. 100 (2006) 114517.
[10] C. Waldau, P. Schilinsky, M. Parisutti, J. Hauch, C. J. Brabec, Adv.Mater. 15 (2003) 2084-2088.
[11] P. H. Wobkenberg, T. D. Anthopoulos, Synthetic Metals 158 (2008) 468-472.
[12] T. D. Anthopoulos, C. Tanase, S. Setayesh, E. J. Meijer, J. C. Hummelen, P. W. M. Blom, D. M. de Leeuw, Adv.Mater. 16 (2004) 2174-2179.
[13] T. D. Anthopoulos, D. M. de Leeuw, E. Cantatore, P. van 't Hof, J. Alma, J. C. Hummelen, J. Appl. Phys. 98 (2005) 054503.
[14] C. L. Fan, Y.Z. Lin, C. H. Huang, Semicond. Sci. Technol. 26 (2011) 045006.
[15] H. C. Tiao, Y.J. Lee, Y.S. Liu, S.H. Lee, C.H. Li, M.Y. Kuo, Organic Electronics 13 (2012) 1004-1011.
[16] J. B. Koo, S. Y. Kang, I. K. You, S. K. Suh, Solid-State Electron. 53 (2009) 621.
[17] A. Wang, I. Kymissis, V. Bulović, A. Akinwande, Appl. Phys. Lett. 89 (2006) 112109.
[18] H. Ohnuki, W. Changhui, M. Izumi, Y. Tatewaki, K. Ikegami, This Solid Films 516 (2008) 2747.
[19] S. K. Park, Y. H. Kim, J. I. Han, D. G. Moon, W. K. Kim, IEEE Trans. Electron Devices 49 (2002) 2008-2015.
[20] D. Lu, Y. Wu, J. Guo, G. Lu, Y. Wang, J. Shen, Mater. Sci. Eng. B97 (2003) 141-144.
[21] A. Ulman, Academic press, New York (1991).
[22] J. W. Chang, H. Kim, J. K. Kim, B. K. Ju, J. Korean Phys. Soc. 42 (2003) S268.