High Level Synthesis Implementation of a Three-dimensional Systolic Array Architecture for Matrix Multiplications on Intel Stratix 10 FPGAs

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Abstract—In this paper, we consider the HLS implementation of a three-dimensional systolic array architecture for matrix multiplication that targets specific characteristics of Intel Stratix 10 FPGAs in order to produce designs that achieve a high floating-point throughput using most of the DSPs at high frequencies in a way that avoids the congestion of the routing fabric. The investigated three-dimensional systolic array architecture is able to produce hardware designs that use 99% of the available DSPs with maximum frequencies that let us achieve performance above 3 TFLOPS.

Index Terms—high-level synthesis, matrix multiplication, systolic arrays

I. INTRODUCTION

In the last years, the utilization of FPGA accelerator cards became more common thanks to the availability of integrated tool flows based upon high level synthesis (HLS), which allow to generate hardware starting from a code listing easing the development and testing of designs. Even if multiple particular programming patterns [1] [2] [3] are available in order to write codes that turn into efficient HLS designs, none of them can prevent a problem that shows up when many FPGA logic resources are used: a low maximum frequency. This limits the attainable performance, since the maximum frequency effects directly the throughput of memory and floating-point operations. A low maximum frequency is mostly dictated by critical paths, i.e., interconnections between logic resources that have large delays in signal propagation. These delays are due to the congestion of the routing fabric, that can be a consequence of a poor route and place of FPGA logic resources. In order to fix this issue, it is fundamental to investigate algorithms that do not create routing congestion once implemented with HLS. The past provides us interesting examples of architecture-aware algorithms such as the ones for systolic array architectures, that allow solve a broad range of problems based on matrix computations [4] [5] [5].

Several papers implement bi-dimensional systolic array architectures for matrix multiplication on FPGAs [6] [7] [8]. In this paper, we want to investigate a new connection scheme between the processing elements in order to go beyond their bi-dimensional floorplanning, lowering the granularity of processing elements while increasing the total resource utilization. In this regard, it is fundamental to investigate algorithms that properly implemented in HLS can produce efficient interconnections (i.e., that do not create critical paths) between the more important logic resources: the DSPs for floating-point arithmetic, the on-chip memories, and the global memory controllers for data provisioning. This brought us to the formulation of a three-dimensional systolic array architecture for matrix multiplication.

The concept of three-dimensional systolic array architectures was already developed to target three-dimensional fabrication processes [9] [10]. Recently, Kung et al. [11] proposed a three-dimensional mapping of systolic arrays into the 2.5-dimensional Xilinx FPGA architecture. In our investigation, the third dimension is more conceptual than physical. It is a parameter for controlling the data throughput between processing elements.

II. TOOL FLOW AND HARDWARE DESCRIPTION

In this paper, we consider the Intel FPGA SDK for OpenCL tool flow, that lets us integrate OpenCL kernels within the FPGA. This process is made of distinct automated phases: the synthesis, that translates the kernel code into logic resources, the fitter, that places and routes these logic resources into specific FPGA blocks honoring the timing constraints, and the timing analysis, that validates the timing performances, establishing the maximum frequency ($f_{max}$) of the design and determining de facto its performance. The only way users can achieve high performance is by writing kernel codes that translate into good designs in these phases.

The Intel HLS tool aims to create pipelined logic circuits (a.k.a. pipelines) starting from loops within the code. The instructions within the loop body are turned into a logic circuit, that performs the original operations in a time, measured in clock cycles, that we define as loop-body latency ($l_{body}$). The iterations of the loop are executed in pipeline, i.e, in each clock cycle, different loop iterations are executed concurrently by different stages of the logic circuit. The main design goal is creating pipelines that can start the execution of a new iteration in each clock cycle, i.e., having an initiation interval (II) equal
to one. This is very important since the total latency taken by a loop executed in pipeline is

\[ l_{tot} = l_{body} + II \#it \text{ [cycles]} \]

whereas \#it is the number of loop iterations. In this regards, the HLS tool provides pragmas and reports that lets the user adjust the code for the sake of achieving \( II = 1 \). In case of an ideal pipeline, in which \( II = 1 \) and \( \#it >> l_{body} \), the throughput of op-operations (e.g., floating-point operations) measured in op-per-second is

\[ T_{op} = T_{op} f_{max} \left[ \frac{op}{s} \right] \]

whereas \( T_{op} \) is the op throughput measured in [op/cycle], i.e., the number of op-operations started in each clock cycle. The last equation shows that the throughput of a given operation is linearly dependent on \( T_{op} \) and \( f_{max} \). In case of an ideal pipeline, \( T_{op} \) is equal to the number of op-operations present in the loop body, which reflects directly in FPGA resource utilization, not only in terms of blocks but also in required routing fabric, e.g., a floating-point multiplication uses a DSP block and all the wires needed to carry operands, the result, and other required control signals. Unfortunately, \( T_{op} \) and \( f_{max} \) conflict since increasing \( T_{op} \) increases wire usage, this can cause routing congestions, that create critical paths, that lower the \( f_{max} \). This is the reason why it is important to investigate algorithms and HLS implementation methods that can connect most FPGA logic resources without creating routing fabric congestions. Nevertheless, the knowledge of the FPGA accelerator card, in particular its memory systems, plays a fundamental role in the investigation of efficient implementations.

A. Global Memory

The term global memory refers to the main memory within the accelerator card, outside the FPGA. The host system manages the global memory by means of OpenCL API function calls, that allow the user to allocate, transfer, delete buffers within it. In this paper, we consider a Bittware 520N accelerator card, which has four 8 GByte DDR4@2400MT/s memory modules, each of them can provide a peak theoretical throughput of

\[ B_{ddr} = 19200 \text{ MB/s} \]

for a total of 76800 MB/s. Each memory module is connected to the FPGA via a dedicated memory controller. The HLS tool turns the global memory pointers accessed within the kernel code into load-or-store units (LSU) that can read or write a fixed number of bytes per clock cycle depending on the pointed data, e.g., reading or writing a location of a single-precision floating-point array produces a 4-byte LSU. It must be noted, that the HLS tool is only able to create LSUs having a size of power-of-two bytes, e.g. reading or writing three sequential values of a single-precision floating-point array produces a 16-byte LSU.

Global memory accesses can create stalls. A stall is introduced within the pipeline if the memory controller is not able to cope with the transmission rate requested by LSUs, i.e.

\[ B_r f_{max} > e B_{ddr} \]

whereas \( B_r \) is the throughput of data requests in [bytes/cycle] and \( e \) is the memory controller efficiency, which is close to 1 in case of sequential aligned read-or-write-only accesses [12]. These kind of accesses produce aligned burst-coalesced LSUs, which are the most suited for Stratix 10 FPGAs [2]. If a stall is present (i.e., [2] holds true), the stall rate is evaluated as

\[ stall = 1 - \frac{e B_{ddr}}{B_r f_{max}} \]

which corresponds to the fraction of requests that cannot be fulfilled by a memory controller. A stall does not allow the pipeline to run with \( II = 1 \) even if the HLS tool is able to generate it. In case of stalls, the throughput of op-operations within the loop body (1) is reformulated as

\[ T_{op} = (1 - \text{stall}) T_{op} f_{max} \left[ \frac{op}{s} \right] \]

This shows the importance of avoiding stalls, since they decrease linearly the throughput of the operations present in the loop body. In summary, considering that LSUs have a power-of-two byte size and that the memory controller efficiency \( (e) \) for aligned burst-coalesced accesses is close to 1, depending on \( f_{max} \), a global memory LSU can at most request

\[ B_{ddr} = \begin{cases} \left( \frac{64 \text{ bytes}}{\text{cycle}} \right) = 16 & 150 \text{ MHz} < f_{max} \leq 300 \text{ MHz} \\ \left( \frac{32 \text{ bytes}}{\text{cycle}} \right) = 8 & 300 \text{ MHz} < f_{max} \leq 600 \text{ MHz} \end{cases} \]

(4)

to a memory controller without creating stalls. For convenience, in the following sections, the data throughput (\( B \)) is expressed in terms of single-precision floating-point values transferred per clock cycle, i.e., [sp-floats/cycle].

B. Floating-Point Operations

The Stratix 10 architecture features Variable Precision DSP blocks [13] that can be configured in order to perform operations on different data types. Most notably, these DSPs can execute single-precision floating-point operations natively. A DSP block can do different kind of operations, such as multiplications, additions or fused multiply–adds. In the last configuration, a DSP block is able to perform two floating-point operations per clock cycle. So, the maximum floating-point throughput of a design using \#DSP blocks in fused multiply–add configuration is

\[ T_{peak} = 2 \#DSP f_{max} \text{ [FLOPS]} \]

(5)

Variable Precision DSP blocks can also accumulate values produced in successive iterations within an internal register. Unfortunately, it is not possible to exploit this capability in pipelines with \( II = 1 \). Multiple DSP blocks can be chained together in order to do floating-point operations involving more operands, such as a dot product. The HLS tool is able
to recognize a dot product computation and translate it into a dot product unit, which performs the sum of the product of two vectors \{v_i, w_i \mid 0 \leq i < d_p\} with a scalar z, i.e.,
\[ r = z + \sum_{i=0}^{d_p-1} v_i w_i \]  
(6)

Each dot product unit embeds \(d_p\) DSP blocks. The peak floating-point throughput of a dot product unit in pipeline is
\[ T_{flot} = 2 \cdot d_p \text{ [FL op/ cycle]} \]  
(7)

which needs to be sustained by the input-data throughput for reading \(z\) and \(d_p\) values of \(v\) and \(w\)
\[ B_{in} = 2 \cdot d_p + 1 \text{ [sp-floats/cycle]} \]  
(8)

This data throughput needs to be constantly satisfied in order to avoid stalls that can decrease the floating-point throughput, as seen in (3). Considering (4), the floating-point throughput sustainable using only the global memory is extremely low, it is around ten GFLOPS, since the available data throughput can feed just few DSPs without stalls. The on-chip memory is necessary for exploiting a large number of DSPs.

C. Local Memory

The term local memory refers to the memory stored on chip within M20Ks or MLABs and is usually generated by arrays declared within the kernel code.

These on-chip memories can implement two kind of memory systems: FIFO, that allows to enqueue and dequeue data, and mapped, that lets access data randomly by its address. Mapped memory systems features LSUs similar to the global memory partitioning, i.e., the user can constrain array portions to be allocated in specific parts of the memory system, having their own independent LSU, that can work concurrently in order to provide the data throughput required without stalls. The possibility of having many small partitions (i.e., made just of few M20K/MLAB blocks) is a key aspect, since it allows the fine-grain distribution of the data throughput throughout the FPGA, close to the blocks that need it, in our case the DSPs.

III. SYSTOLIC ARRAY ARCHITECTURE FOR MATRIX MULTIPLICATION

Systolic array architectures are made of a grid of processing elements (PE). Each PE exchanges data with its neighbouring PEs without a global control logic. A systolic array architecture does computations in virtue of the operations that each PE applies on data passing through them. One simple application of a systolic array architecture is matrix multiplication.

A. Classical Systolic Array

A classical example of systolic array architecture for matrix multiplication has been proposed by Okuda-Song [14], it is organized as a bi-dimensional grid of \(d_i \times d_j\) PEs. During the computation, PE\(_{ij}\) receives and sends all the elements of the \(i\)-row of \(A\) and the \(j\)-column of \(B\), multiply-accumulating them in order to compute \(c_{ij} \in C\). This kind of systolic array architecture can be defined as follows.

**Definition 1** (Classical Systolic Array Matrix Multiplication). Given \(A \in (d_i^0 \times K)\) and \(B \in (K \times d_j^0)\), \(AB = C \in (d_i^0 \times d_j^0)\) can be computed in pipeline by a bi-dimensional Cartesian grid of \(d_i^0 \times d_j^0\) multiply-accumulate units in a total latency of
\[ l_{tot} = d_i^0 + d_j^0 + K - 1 + l_{MAC} \text{ [cycles]} \]

The input matrices enter the grid by two of its edges, the \(A\) values enter in \{PE\(_{i0}\) \mid 0 \leq i < d_i^0\}, whereas the \(B\) values enter in \{PE\(_{0j}\) \mid 0 \leq j < d_j^0\}. The floating-point throughput of this systolic array architecture is
\[ T_{flot} = 2 \cdot d_i^0 \cdot d_j^0 \text{ [FL op/ cycle]} \]
whereas the data throughput of \(A\) and \(B\) values entering the grid is
\[ E_A = d_i^0 \cdot B \quad E_B = d_j^0 \text{ [sp-floats/cycle]} \]

B. Proposed Systolic Array

The systolic array architecture investigated in this paper differs from the one defined in the previous section for two aspects. First, these PEs are made of a dot product unit (such as in [8], [15], [16]) performing more floating-point operations than a single multiply-accumulation. Second, the grid structure is three-dimensional. The time dimension of the classical systolic array is partially projected into the third dimension. In this regard, the investigated architecture can be considered as a stack of bi-dimensional layers, as shown in Figure I. The value computed by the dot product unit is no more stationary within a PE but it is sent through the third dimension.

**Definition 2** (Investigated Systolic Array Matrix Multiplication). Given \(A \in (d_i^0 \times K)\) and \(B \in (K \times d_j^0)\), \(AB = C \in (d_i^0 \times d_j^0)\) can be computed in pipeline by a three-dimensional Cartesian grid of \(d_i^0 \times d_j^0 \times d_p^0\) dot-product units of size \(d_p\) with a total latency of
\[ l_{tot} = d_i^0 + d_j^0 + K - 1 + \frac{d_i^0}{d_p^0} \cdot l_{dotd_p} \text{ [cycles]} \]
The matrices enter the grid by two of its faces, the \(A\) values enter in \{PE\(_{i0L}\) \mid 0 \leq i < d_i^0, 0 \leq L < \frac{d_i^0}{d_p^0}\}, the \(B\) values in \{PE\(_{0jL}\) \mid 0 \leq j < d_j^0, 0 \leq L < \frac{d_i^0}{d_p^0}\}. The floating-point throughput is
\[ T_{flot} = 2 \cdot d_i^0 \cdot d_j^0 \cdot d_p^0 \text{ [FL op/ cycle]} \]  
(9)

whereas the data throughput of \(A\) and \(B\) values entering the grid is
\[ E_A = d_i^0 \cdot d_p^0 \quad E_B = d_j^0 \cdot d_p^0 \text{ [sp-floats/cycle]} \]  
(10)

For the rest of the paper, superscript 0 denotes systolic array architecture sizes.

It is important to note that \(d_p^0\) effects linearly the throughput of floating-pointing operations and data. This third dimension can be considered a parameter useful in design space exploration.
C. HLS implementation

Listings 1 and 2 show a possible HLS implementation of the three-dimensional systolic array architecture in Definition 2 whereas, dim0_i = d_0^i, dim0_j = d_0^j, dim0_k = d_0^k, DP_SIZE = d_p, and K = K. The arrays A and B defined in Listing 1 contain A \in (d_0^i \times K) and B \in (K \times d_0^j) distributed in \frac{K}{d_p} blocks of size (d_0^i \times d_0^j) and (d_0^j \times d_0^p), i.e.,

\[
\begin{align*}
A[T][k][k] &= A_{ik} \quad \forall 0 \leq i < d_0^i \\
B[T][k][j] &= B_{kj} \quad \forall 0 \leq j < d_0^j
\end{align*}
\]

such that \( k = \frac{K}{d_p} T + k \quad \forall 0 \leq T < \frac{K}{d_p}, \quad 0 \leq k < d_0^k \).

Each iteration of the loop at line 7 in Listing 1 passes a block of A and a block of B to the function systolic_mmm defined in Listing 2. This function multiply-accumulates \( A[T] \in (d_0^i \times d_0^j) \) and \( B[T] \in (d_0^j \times d_0^p) \) in \( C \in (d_0^i \times d_0^p) \) for all \( 0 \leq T < K/d_p \). After the execution of the loop in Listing 1, C contains the solution computed as the inner product between A and B.

Listing 1. Implementation of Definition 2

```c
float A[K[dim0_k][dim0_i][dim0_k] __attribute__((numbanks(dim0_i*dim0_k)))
float B[K[dim0_k][dim0_k][dim0_j] __attribute__((numbanks(dim0_k*dim0_j)))
float C[dim0_k][dim0_j]
// filling of A and B ...
for(int T=0; T<K[dim0_k]; ++T)
systolic_mmm( A[T], B[T] );
```

The fact that loops at Line 7, 9 and 11 in Listing 2 are completely unrolled allows Line 16 to allocate

\[ \#DSP = d_0^i d_0^j d_0^p \] (11)

DSP blocks. Each of them performs 2 FLOP per clock cycle providing the floating-point throughput in (9). These DSP blocks are distributed in

\[ \#PE = d_0^i d_0^j d_0^p \] (12)

PEs within a \((d_0^i \times d_0^j \times d_0^p)\) Cartesian grid. Each PE is made of a dot product unit with a size of \( d_p \). This size can be set defining DP_SIZE, otherwise \( d_p \) is equal to \( d_0^k \) forming a single layer systolic array architecture. In case of multiple layers (i.e., \( d_0^k/d_p > 1 \)), Line 21 in Listing 2 transmits the partial solution to the upper layer in the L direction.

The unrolling of Line 14 in Listing 2 at \( j=0 \) produces \( d_0^i d_0^j d_0^k \) load units that read the values of A. Each load unit is connected to a partition of A declared at Line 1 in Listing 2. Same applies for B, where the unrolling of Line 15 in Listing 2 at \( i=0 \) produces \( d_0^j d_0^k \) load units for B, each load unit is connected to a partition of B declared at Line 2 in Listing 2. These load units read one floating-point value for each clock cycle producing the input data throughputs in (10). Moreover, Line 14 and 15 in Listing 2 propagate the A and B values through the PEs in the i and j directions by mean of the _fpga_reg() function, which provides at least one register between a PE and its neighbor, adding a clock cycle delay in data propagation. In particular, Line 14 produces the creation of \( d_0^i d_0^k \) chains, that are \( d_0^i \)-register-long. Each chain is fed by one load unit generated by A partitions. Same applies for Line 15, whereas \( d_0^j d_0^k \) chains, that are \( d_0^j \)-register-long, are fed by load units generated by B partitions. These register chains are very important for two reasons: first, they can break critical paths between PEs; second, they reduce the fan-out of data passing from load units to DSP blocks. Setting the sizes of the systolic array architecture changes the number and the length of the register chains, this allows to balance the input-data throughput requirements of the dot product units (8) between different sources. For example, keeping \#DSP constant while decreasing \( d_0^i \) lowers \( B_A \) and \( B_B \) coming from block memories and increase the data throughput provided by the registers, having fewer register chains but longer.

Ideally, the loop in Listing 1 could produce a pipeline with
II = 1 and a loop-body latency of
\[ l_{\text{body}} = d_i^0 + d_j^0 - 1 + \frac{d_0}{d_p} t_{\text{data},p} \]  \hspace{1cm} \text{(13)}
executing \( \frac{K}{d_p} \) iterations. Unfortunately, this is not the case since it is not possible to obtain \( II = 1 \) with the accumulation in successive iterations. Moreover, the aforementioned loop-body latency does not consider global memory accesses, its real value is higher for pipelines reading and writing the global memory. Anyway, \( (13) \) influences the loop-body latency of the pipeline where it is included allowing the user to interact with the HLS tool by changing the systolic array architecture sizes in order to explore the design space.

In the following sections, we describe how to integrate the function in Listing 2 in a design in order to compute off-chip matrix multiplications.

IV. MEMORY THROUGHPUT ANALYSIS FOR OFF-CHIP MATRIX MULTIPLICATION

In order to test the three-dimensional systolic array architecture described in the previous section, we use it for performing a matrix multiplication in which the operands and the result cannot fit into the FPGA on-chip memory.

Problem 1 (Off-chip Matrix Multiplication). Given \( A \in (d_i^2 \times d_k^2) \) and \( B \in (d_k^2 \times d_j^2) \), compute \( AB = C \in (d_i^2 \times d_j^2) \). Where none of the matrices can fit entirely into the on-chip memory. For the rest of the paper, superscript 2 denotes off-chip matrix sizes.

So, our investigation must consider that data need to transit from/to the global memory to/from the systolic array architecture. The systolic array architecture in Definition 2 is able to ingest \( B_A \) and \( B_B \) floating-point numbers for each clock cycle. As seen in Section III-A, a global memory LSU is able to request \( B_{\text{ddr}} \) floating-point numbers for each clock cycle without stalls. A systolic array architecture with a large \( T_{\text{flip}} \) implies \( B_A > B_{\text{ddr}} \) and \( B_B > B_{\text{ddr}} \).

We can formulate the problem as follows. How to connect the systolic array architecture to the global memory system since a global memory LSU is not able to provide enough data throughput in order not to stall the pipeline? The answer to this question involves the utilization of a cache system living into on-chip memories. This cache contains some values of \( A \) and \( B \) that need to be reused for a certain number of times in order to let the global memory feed the systolic array architecture without stalls. We define the reuse ratio \( r \) as the minimal number of times that a datum in the on-chip memory needs to be reused in order to let a global memory LSU cope with \( B_A \) and \( B_B \) needed by the systolic array architecture. The reuse ratios for the element of matrices \( A \) and \( B \) can be computed as
\[ r_A = \frac{B_A}{\bar{B}_A}, \quad r_B = \frac{B_B}{\bar{B}_B} \]  \hspace{1cm} \text{(14)}
where \( \bar{B}_A \) and \( \bar{B}_B \) are the number of \( A \) and \( B \) elements read in each clock cycle.

At this point, it is useful to define a notation for expressing the partition of a matrix into blocks.

Definition 3 (Block matrix representation). Given \( M \in (d_i^2 \times d_j^2) \), it is possible to represent its partition into \( \frac{d_i^2 d_j^2}{d_k^2} \) blocks of size \( (d_i^1 \times d_j^1) \), as \( \bar{M} : (d_i^2 / d_i^1 \times d_j^2 / d_j^1) \rightarrow (d_i^1 \times d_j^1) \), whereas \( \bar{M}^{I_j} = M_{ij} \) s.t.
\[ \begin{cases} i = d_i^1 I + i \quad \forall 0 \leq I < d_i^1 / d_i^1, \quad 0 \leq i < d_i^1 \\ j = d_j^1 J + j \quad \forall 0 \leq J < d_j^2 / d_j^1, \quad 0 \leq j < d_j^1 
\]  \hspace{1cm} \text{(15)}
where \( d_i^1 \) is a multiple of \( d_i^2 \) and \( d_j^1 \) of \( d_j^2 \). Practically, \( \bar{M}^{I_j} \) identifies the block in the \( I \)—row and \( J \)—column of the partition. This definition can be applied recursively adding another order of indexes.

A. Implemented Algorithm

The algorithm, that solves Problem 1 by means of the systolic array architecture discussed in Section III-C, needs to address two aspects. First, it needs to set as parameters the data reuse for \( A \) and \( B \) in order not to stall computation. Second, it needs to avoid the floating-point accumulation between successive iterations since the Variable Precision DSP blocks cannot achieve it in pipeline with \( II = 1 \). For the sake of this, we implement the following algorithm.

Definition 4 (Two-level blocked Matrix Multiplication). Problem 1 can be solved with a two-level blocked algorithm. The first level acts on the following partition
\[ \bar{A} : (d_i^2 / d_i^1 \times 1) \rightarrow (d_i^1 \times d_k^2) \]
\[ \bar{B} : (1 \times d_k^2 / d_j^1) \rightarrow (d_k^1 \times d_j^1) \]
\[ \bar{C} : (d_i^2 / d_i^1 \times d_j^2 / d_j^1) \rightarrow (d_i^1 \times d_j^1) \]
aiming to solve Problem 1 by computing \( \bar{C} \) single blocks as
\[ \bar{C}_{I_j} = \bar{A}_{I_j}^i \bar{B}_{I_j}^j \quad \forall 0 \leq I < d_i^2 / d_i^1, \quad 0 \leq J < d_j^2 / d_j^1 \]  \hspace{1cm} \text{(16)}
Each block \( \bar{C}_{I_j} \) is computed by means of a second level partition
\[ \bar{A} : (d_i^1 / d_i^0 \times d_k^2 / d_k^0) \rightarrow (d_i^0 \times d_k^0) \]
\[ \bar{B} : (d_k^0 / d_k^1 \times d_j^2 / d_j^1) \rightarrow (d_k^1 \times d_j^1) \]
\[ \bar{C} : (d_i^1 / d_i^0 \times d_j^2 / d_j^0) \rightarrow (d_i^0 \times d_j^0) \]
that allows the systolic array architecture implemented in Listing 2 with a size of \( d_i^0 \times d_j^0 \times \frac{d_0}{d_p} \) to solve
\[ \bar{C}_{I_j}^{I_k} = \sum_k \bar{A}_{I_k}^{I_k} \bar{B}_{I_k}^{I_k} \quad \forall 0 \leq i < d_i^1 / d_i^0, \quad 0 \leq j < d_j^1 / d_j^0 \]  \hspace{1cm} \text{(17)}
as a cyclcal accumulation of outer products between the columns of \( \bar{A} \) and the rows of \( \bar{B} \) (i.e., \( k \) is the slowest index) in order to avoid the accumulation in successive iterations of the values in \( \bar{C} \). The reuse ratio in \( (13) \) are applied by setting \( d_i^1 \) and \( d_j^1 \) as
\[ d_i^1 = r_B d_i^0, \quad d_j^1 = r_A d_j^0 \]  \hspace{1cm} \text{(18)}
which implies that each element of \( \bar{A} \) is reused \( r_A \) times and each element of \( \bar{B} \) is reused \( r_B \) times in the computation of the outer product in \( (17) \).
These memory systems are made of columns of the design. During Compute mapped memory systems, and a FIFO system. Basically, the goal is to write in the local memory some portions of the memory mapped systems.

Where \( d^0_d \), \( d^1_d \) floating-point values per clock cycle, which could be greater than \( B_{ddr} \), causing stalls not effecting computation since Write happens alone in Phase 4. \( C \) is saved in row-major format allowing the store unit to be burst-coalesced.

The implementation is made of a single-kernel containing a single for-loop, in a way that allows the HLS tool to produce a single efficient pipeline, as suggested in [2] for Stratix 10 FPGAs. In order to obtain a single loop, we manually fused all the phases. The fraction of iterations in which the dot-product units are computing is

\[
c_{\%} = \frac{\#it_{comp}}{\#it_{tot}} \approx \frac{d^2_d}{d^2_d + d^2_d + B_{ddr}}
\]

whereas \( \#it_{tot} \) are the iterations taken by all the phases and \( \#it_{comp} \) are only the Compute ones.

### V. Implementation

The algorithm in Definition 4 can be implemented as the sequential computation of \( C \) blocks done in three phases:

1. **Read** \( A^0_i \) and \( B^0_j \) from the global memory, store them into on-chip memory.\( A^0_i \) and \( B^0_j \) from the global memory, while at the same time, the systolic array architecture is reading from the local memory some other portions of \( A^0_i \) and \( B^0_j \).

So basically, given \( I \) and \( J \), \( C^j_j \) can be computed as in (16) by four sequential phases:

1. **Read** from global memory \( \{A^0_i \mid 0 \leq i < d^1_i/d^0_i\} \) and \( \{B^0_j \mid 0 \leq j < d^1_j/d^0_j\} \) and store them into on-chip memory and Initialize \( C^j_j \) to zero.

2. For all \( k \mid 0 \leq k < (d^2_d/d^0_k - 1) \}
   a) **Read** from global memory \( \{A^1_i \mid 0 \leq i < d^2_i/d^0_i\} \) and \( \{B^0_j \mid 0 \leq j < d^2_j/d^0_j\} \)
   b) **Compute** \( C^j_j \) as \( A^1_i \times B^0_j \) for all \( 0 \leq i < d^2_i/d^0_j, 0 \leq j < d^2_j/d^0_j \)

3. **Compute** \( C^j_j \) as \( \hat{A}^1_i \times \hat{B}^0_j \) for all \( 0 \leq i < d^2_i/d^0_j, 0 \leq j < d^2_j/d^0_j \)

4. **Write** \( C^j_j \) to the global memory.

Whereas **Read** spans from 1 to 2, **Compute** from 2 to 3 being completely overlapped in 2, and **Write** is executed alone in 4, as shown in Figure 3.

![Graphical representation of the connections between the parts of the design. Where \( d^0_d = 4, d^1_d = 3, d^0_k = 3 \), \( B_{A} = 2 \) and \( B_{B} = 1 \). MMAPs stands for the partitions of the memory mapped systems.](image)

![Fig. 3. The four phases described in Section V for the computation of a block of \( C \).](image)

The implemented design is made of three main parts: a three-dimensional systolic array, two mapped memory systems, and a FIFO system.

The three dimensional systolic array is the central core of the design. During **Compute**, it constantly multiplies two blocks of \( A \) and \( B \) loading their values from the two mapped memory systems and accumulating the results in the FIFO system.

Overlapping **Read** and **Compute** implies that just two columns of \( A \) and two rows of \( B \) need to fit entirely into the mapped memory systems. These memory systems are made respectively of \( d^0_d d^1_d \) and \( d^0_k d^1_k \) partitions, their load units are connected to the systolic array architecture by the register chains as described in Section III-C. In order to fill these partitions with the values coming from global memory, their store units are connected to two global memory load units. Each of them read \( B_{A} \leq B_{ddr} \) and \( B_{B} \leq B_{ddr} \) floating-point values per clock cycle, in order to avoid stalls. All accesses are performed by burst-coalesced LSUs for achieving an high memory controller efficiency, i.e., \( c \) in (2) approaches to 1.

For this reason \( A \) is saved in a column-major format since it is accessed by columns and \( B \) is saved in a row-major format since it is accessed by rows.

Since a \( C \) block is accessed entirely during **Compute**, it needs to fit completely into the on-chip memory. The outer product computation allows to store it in a collection of \( d^0_j d^0_j \) FIFOs. During **Write**, a global memory store unit writes \( d^0_j \) floating-point values per clock cycle, which could be greater than \( B_{ddr} \), causing stalls not effecting computation since **Write** happens alone in Phase 4. \( C \) is saved in row-major format allowing the store unit to be burst-coalesced.

The implementation is made of a single-kernel containing a single for-loop, in a way that allows the HLS tool to produce a single efficient pipeline, as suggested in [2] for Stratix 10 FPGAs. In order to obtain a single loop, we manually fused all the phases. The fraction of iterations in which the dot-product units are computing is

\[
c_{\%} = \frac{\#it_{comp}}{\#it_{tot}} \approx \frac{d^2_d}{d^2_d + d^2_d + B_{ddr}}
\]

whereas \( \#it_{tot} \) are the iterations taken by all the phases and \( \#it_{comp} \) are only the **Compute** ones.

### VI. Evaluation

In our experiments, we used the BittWare 520N Stratix 10 GX2800 accelerator card with has a board support package (BSP) based upon Quartus 19.4.0 Build 64 Pro, on top of that there is the Intel FPGA SDK for OpenCL version 20.4.0 Build 72. The BSP occupies part of the FPGA resources, 4713 of 5760 Variable Precision DSPs are available for the kernel logic. Our designs are able to use up to 4704 of them, the 99.8% of the available. All designs get the Hyperflex optimization on allowing them to reach higher \( f_{max} \).

Table 1 contains the best \( f_{max} \) of the designs varying systolic array architecture sizes. In particular, \( d^0_d, d^1_d, d^0_k \) and \( d^1_k \) are the parameters in Definition 2. \#PEs is defined in (12). The DSPs column shows the number of DSP block
forming the systolic array architecture, they are equal to \#DSP as defined in (11), these values are confirmed by the report.html generated by the Intel HLS tool. The $f_{\text{max}}$ values are taken from the Kernel $f_{\text{max}}$ field in the acl_quartus_report.txt file within the design directory. The peak floating-point throughput ($T_{\text{peak}}$) is computed as (5). The designs A, B, and D fail the synthesis since the fitter is not able to place dot product units with a size larger than 1 for the considered architecture sizes.

Table III-V show the floating-point throughput and the DSP efficiency for the considered designs varying the sizes of the matrices involved in the matrix multiplication. For reference, we present also the floating-point throughput for an Intel Xeon Gold 6148 CPU and a Nvidia GeForce RTX 2080 Ti GPU doing the same operation using optimized BLAS libraries: MKL version 20.2 for the CPU, CUBLAS version 11.2 for the GPU. In all cases, we report the performance obtained by measuring the actual execution time of the multiplication of matrices within the global memory of the devices. The sizes of the matrices are different between the designs since they depend on (18) and (14). The measured floating-point throughput is computed by the total number of single-precision floating-point operations executed for the matrix multiplication

$$\#FLOP = d_i^2 d_j^2 (2d_k^2 - 1)$$

divided by the actual kernel execution times measured with OpenCL profiling events, i.e.,

$$T_{\text{flops}} = \frac{\#FLOP}{\text{kernel execution time}} \text{ [FLOPS]}$$

The measured DSP efficiency is computed as the ratio between the obtained and the peak floating-point throughput, i.e.,

$$e_D = T_{\text{flops}} / T_{\text{peak}}$$

As expected, the measured DSP efficiencies are close to their evaluations shown in (19).

In order to compare our results, we selected works that use the Intel Stratix 10 GX2800. The FBLAS library includes a systolic SGEMM function that is able to use 3270 DSPs at 216 MHz [8]. It has a performance similar to the Cannon matrix multiplication algorithm implemented in (17) that uses 3323 DSPs at 294 MHz. Unfortunately, these designs do not achieve Hyperflex optimization and reach a floating-point throughput just below the 1.5 TFLOPS.

Another reference is established by the matrix multiplication example code optimized for Stratix 10 that is shipped within the Intel FPGA SDK for OpenCL. This is far from being a simple example code, it is a complex design involving multiple kernels connected by channels that multiples off-chip matrices using a configurable bi-dimensional systolic array architecture. Unfortunately, its source code does not allow to isolate functions that can be reused, e.g., on-chip matrix multiplication function. The user can specify the grid size by setting the number of PEs in rows (PE_ROWS) and columns (PE_COLS). Each PE contains a dot product unit having a size of 4, 8, or 16, other sizes are not possible. An optional flag (FORCE_dot_4) allows to split these dot product units in multiple ones having a size of 4. In order to guarantee the fairest comparison, we synthesized the Intel SDK example with different grid sizes and seeds, Table VII reports the best $f_{\text{max}}$ obtained. The configuration reported as optimal in the Intel SDK example README is made of a 32 × 14 grid, in which each PE is made of a dot product unit of size 8. The resulting design has 3584 DSPs working at 412 MHz with a peak floating-point performance of 2953 GFLOPS. We went further and tried different grid sizes in order to use more DSPs. Many attempts, using 4096 DSPs or more, failed during the fitter phase. A 32 × 16 grid, in which each PE contains two dot product unit of size 4, achieves the best result that we are able to obtain, producing a design made of 4096 DSPs working at 407 MHz and providing a peak floating-point performance of 3342 GFLOPS.

We evaluate the floating-point throughput of these designs in the same way of ours, results are shown in Table VII and VIII. Also the Intel SDK example has constraints on matrix sizes. In the case of the 32 × 14 grid, $d_j$ needs to be multiple of 1024 and $d_j^2$ of 448, whereas for the 32 × 16 grid, $d_i^2$ needs to be multiple of 1024 and $d_i^2$ of 512. The floating-point throughput shows that the DSP efficiency is above 0.9 for $d_k^2 \geq 2048$, our designs reach this efficiency just for $d_k^2 = 4096$. Unfortunately, the DSP efficiency of our designs is lower due to the fact that Write (i.e., Phase 4) is performed without any kind of overlapping computation. The higher efficiency of the Intel SDK example comes at the cost that all the matrices need to be reordered by the host in order to be multiplied by the accelerator card. In fact, considering off-chip matrices in row-major format, A needs to be reordered block wise, B need to be transposed and then reordered block-wise. C needs to sustain a two level reverse block-wise reordering in order to be in the row-major format. This implies that the result matrix has a different format respect to both operands, implying that it needs to be transferred back to the host in order to be reordered in case we want use it as an operand for the next matrix multiplication on the accelerator card. In our design, the only transformation that needs to be applied to off-chip matrices in row-major format is the transposition of A in order to save it in column-major format. On the other side, C has the same row-major format of B. So, we can use the multiplication result as an operand for another multiplication without any transfer to the host for the reordering.
TABLE II

| ID  | $d_1^2 = 672$ | $d_2^2 = 1344$ | $d_3^2 = 2688$ | $d_4^2 = 5376$ | $d_5^2 = 10752$ | $d_6^2 = 21504$ |
|-----|--------------|--------------|--------------|--------------|--------------|--------------|
| C   | 1799 0.51    | 2331 0.67    | 2715 0.74    | 2907 0.84    | 3010 0.87    | 3085 0.89    |
| GPU | 1230 2.07    | 2016 0.96    | 2077 0.89    | 2232 0.84    | 2445 0.88    | 2802 0.97    |

TABLE III

| ID  | $d_1^2 = 576$ | $d_2^2 = 1152$ | $d_3^2 = 2804$ | $d_4^2 = 6068$ | $d_5^2 = 12616$ | $d_6^2 = 14432$ |
|-----|--------------|--------------|--------------|--------------|--------------|--------------|
| E   | 1462 0.47    | 2469 0.71    | 2783 0.82    | 3083 0.90    | 3211 0.94    | 3301 0.97    |
| GPU | 1258 1.86    | 2106 0.97    | 2193 0.89    | 2357 0.94    | 2513 0.97    | 2577 0.98    |

TABLE IV

| ID  | $d_1^2 = 560$ | $d_2^2 = 1280$ | $d_3^2 = 2240$ | $d_4^2 = 4480$ | $d_5^2 = 8960$ | $d_6^2 = 17920$ |
|-----|--------------|--------------|--------------|--------------|--------------|--------------|
| F   | 1704 0.46    | 2511 0.48    | 2807 0.51    | 3209 0.59    | 3549 0.58    | 3576 0.66    |
| CPU | 1889 2.07    | 2718 0.96    | 2821 0.94    | 3040 0.90    | 3129 0.93    | 3139 0.93    |
| GPU | 1873 0.42    | 2652 0.86    | 2743 0.84    | 2901 0.89    | 2951 0.94    | 2957 0.91    |

TABLE V

| ID  | $d_1^2 = 512$ | $d_2^2 = 1024$ | $d_3^2 = 2048$ | $d_4^2 = 4096$ | $d_5^2 = 8192$ | $d_6^2 = 16384$ |
|-----|--------------|--------------|--------------|--------------|--------------|--------------|
| D   | 1488 0.48    | 2205 0.65    | 2527 0.80    | 2927 0.94    | 3519 0.97    | 3607 0.98    |
| B   | 1388 0.48    | 2106 0.66    | 2341 0.80    | 2670 0.88    | 3121 0.94    | 3211 0.97    |
| C   | 1509 0.48    | 2216 0.66    | 2522 0.80    | 2890 0.89    | 3505 0.94    | 3572 0.97    |
| M   | 1469 0.49    | 2103 0.67    | 2427 0.81    | 2649 0.89    | 2815 0.94    | 2810 0.97    |
| S   | 1432 0.49    | 2074 0.66    | 2353 0.81    | 2680 0.89    | 2951 0.94    | 3059 0.97    |
| CPU | 1561 0.47    | 2341 0.80    | 2659 0.89    | 2953 0.94    | 3579 0.97    | 3679 0.98    |
| GPU | 1261 0.42    | 2652 0.86    | 2743 0.84    | 2901 0.89    | 2951 0.94    | 2957 0.91    |

TABLE VI

| PRROWS | PRCOLS | DOT_PROD_VECTOR_SIZE | # | % avail | TIME_MAX [MHz] | TIME_FLEX [GHz] |
|--------|--------|-----------------------|---|---------|----------------|----------------|
| 32     | 18     | 4 (for 2 dot prod units) | 608 97.7% | first failed | first failed |
| 32     | 16     | 4 (for 2 dot prod units) | 609 96.9% | 400 3143 | first failed |
| 32     | 32     | 4 (for 2 dot prod units) | 609 96.9% | first failed | first failed |
| 12     | 14     | 8                      | 594 78.9% | 412 2533 | first failed |

TABLE VII

| $d_1^2 = 1024$ | $d_2^2 = 1024$ | $d_3^2 = 2048$ | $d_4^2 = 4096$ | $d_5^2 = 8192$ |
|-------|-------|-------|-------|-------|
| $T_{flops} \times D$ | $T_{flops} \times D$ | $T_{flops} \times D$ | $T_{flops} \times D$ | $T_{flops} \times D$ |
| 1982 0.86 | 2109 0.84 | 2246 0.82 | 2499 0.97 | 2843 0.96 |

VII. Conclusion

We presented a HLS design for off-chip matrix multiplication, its main component is a three-dimensional systolic array architecture for on-chip matrix multiplication expressed by a simple function that can be adapted and reused. Our systolic array architecture allows the user to fine tune its sizes in order to increase logic resource utilization and explore the design space. Our investigation does not provide the ultimate answer to matrix multiplications in HPC because GPUs deliver easily higher performance. The performance of our implementation is in the same ranges as highly optimized CPU codes. However, we think that this investigation is useful for suggesting new HLS design methods within the wide theoretical background of systolic array architectures. The possibility to describe these architectures in an analytical way and the fact that they can be implemented efficiently could be fundamental for establishing FPGA accelerators in HPC. In the future, we plan to use the function in Listing 2 into designs implementing complete numerical solvers entirely into the FPGA logic for the sake of achieving a performance improvement over GPUs. Source code available at https://github.com/pc2/3d-systo-fpga.
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