HOLL: Program Synthesis for Higher Order Logic Locking

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Abstract. Logic locking “hides” the functionality of a digital circuit to protect it from counterfeiting, piracy, and malicious design modifications. The original design is transformed into a “locked” design such that the circuit reveals its correct functionality only when it is “unlocked” with a secret sequence of bits—the key bit-string. However, strong attacks, especially the SAT attack that uses a SAT solver to recover the key bit-string, have been profoundly effective at breaking the locked circuit and recovering the circuit functionality.

We lift logic locking to Higher Order Logic Locking (HOLL) by hiding a higher-order relation, instead of a key of independent values, challenging the attacker to discover this key relation to recreate the circuit functionality. Our technique uses program synthesis to construct the locked design and synthesize a corresponding key relation. HOLL has low overhead and existing attacks for logic locking do not apply as the entity to be recovered is no more a value. To evaluate our proposal, we propose a new attack (SynthAttack) that uses an inductive synthesis algorithm guided by an operational circuit as an input-output oracle to recover the hidden functionality. SynthAttack is inspired by the SAT attack, and similar to the SAT attack, it is verifiably correct, i.e., if the correct functionality is revealed, a verification check guarantees the same. Our empirical analysis shows that SynthAttack can break HOLL for small circuits and small key relations, but it is ineffective for real-life designs.

1 Introduction

High manufacturing costs in advanced technology nodes are pushing many semiconductor design houses to outsource the fabrication of integrated circuits (IC) to third-party foundries [27, 44]. A fab-less design house can increase the investments in the chip’s intellectual property, while a single foundry can serve multiple companies. However, this globalization process introduces security threats in the supply chain [26]. A malicious employee of the foundry can access and reverse engineer the circuit design to make illegal copies. We can classify the protection methods in passive and active. Passive methods, like watermarking, allow designers to identify but not prevent illegal copies [3]. Active methods, like logic locking, alter the chip’s functionality to make it unusable by the foundry [16].
This alteration depends on a locking key that is re-inserted into the chip in a trusted facility, after fabrication. The locking key is thus the “secret”, known to the design house but unknown to the foundry. Logic locking assumes that the attackers have no access to the key but they may have access to a functioning chip (obtained, for example, from the legal/illegal market). However, logic locking has witnessed several attacks that analyze the circuit and attempt key recovery [32, 45, 50, 61].

In this paper, we combine the intuitions from logic locking, program synthesis, and programmable devices to design a new locking mechanism. Our technique, called higher order logic locking (HOLL), locks a design with a key relation instead of a sequence of independent key bits. HOLL uses program synthesis [4, 52] to translate the original design into a locked one. Our experiments demonstrate that HOLL is fast, scalable, and robust against attacks. Prior attacks on logic locking, like the SAT attack [53], are not practical for HOLL. Since the functionality of the key-relation is completely missing, attackers cannot simply make propositional logic queries to recover the key (like [45, 53, 19]). There are variants of logic locking, like TTLock [63] and SFLL [62], that attempt to combat SAT attacks [53]. However, these techniques use additional logic blocks (comparison and restoration circuits) which makes them prone to attacks via structural and functional analysis on this additional circuitry [49]. HOLL is resilient to such techniques as it exposes only a programmable logic that does not leak any information related to the actual functionality to be implemented.

In contrast to logic locking, attacking HOLL requires solving a second-order problem (see §10 for a detailed discussion on this). To assess the security of our method, we design a new attack, SynthAttack, by combining ideas from SAT attack [53] and inductive program synthesis [52]. SynthAttack employs a counterexample guided inductive synthesis (CEGIS) procedure guided via a functioning instance of the circuit as an input-output oracle. This attack constructs a synthesis query to discover key relations that invoke semantically distinct functional behaviors of the locked design—witnesses to such relations, referred to as distinguishing inputs, act as counterexamples to drive inductive learning. When the locked design is verified to have unique functionality, the attack is declared successful, with the corresponding provably-correct key relation.

Our experimental results (§8) show that the time required by an attacker to recover the key relation for a given set of distinguishing inputs (attack time) increases exponentially with the size of key relation. While the attacker may be able to recover key relations for small HOLL-locked circuits with small key relations, larger circuits are robust to SynthAttack. For example, for the des benchmark with 4,174 gates, the asymmetry between HOLL defense and SynthAttack is large; while HOLL can lock this design in less than 100 seconds, the attack cannot recover the design even within four days for a key relation that increases the area overhead of the IC by only 1.2%. Further, the attack time required to unlock the designs increase exponentially with the complexity of the key relation and the number of distinguishing inputs.

The key relation can be implemented with reconfigurable or programmable
devices, like programmable array logic (PAL) or embedded finite-programmable gate array (eFPGA). For example, eFPGA, essentially an IP core embedded into an ASIC or SoC, is becoming common in modern SoCs [2] and has been shown to have high resilience against bit-stream recovery [8].

Our contributions are:

- We propose a novel IP protection strategy, called higher order logic locking (HOLL), that uses program synthesis, challenging attackers to synthesize a key relation (as opposed to a key bit-string, as in logic locking);
- To evaluate the security offered by HOLL, we propose a strong adversarial attack algorithm, SynthAttack;
- We build tools to apply HOLL and SynthAttack to combinational logic;
- We evaluate HOLL on cost, scalability, and robustness.

2 HOLL Overview

2.1 Threat Model: the Untrusted Foundry

We focus on the threat model where the attacker is in the foundry [46, 47] to which a fab-less design house has outsourced its IC fabrication. Such an attacker has access to the IC design and the (locked) GDSII netlist which can be reverse-engineered. Also, if the attacker can access a working IC (e.g., by procuring an IC from the open market or a discarded IC from the gray market), they can leverage the functional IC’s I/O behavior as a black-box oracle. However, we assume the attacker cannot extract the bitstream, i.e. the correct sequence of configuration bits, from the device. This can be achieved with encryption techniques when the bitstream is not loaded into the device. Also, anti-readback solutions can prevent the attacker from reading the bitstream from the device. The parameters used to synthesize the key relation and the locked circuit (like the domain-specific language (DSL), budget etc.) are not known to the attacker (see §10).

2.2 Defending with HOLL

Consider a hardware circuit \( Y \leftrightarrow \varphi(X) \), where \( X \) and \( Y \) are the inputs and outputs, respectively. HOLL uses a higher-order lock—a secret relation \( \psi \) among a certain number of additional relation bits \( R \). We refer to \( \psi \) as the key relation.

Figure 1a shows an example of a 2-bit adder with input \( X = \{x_1, x_0, x_3, x_2\} \) and output \( Y = \{y_2, y_1, y_0\} \). The circuit is locked by transforming the original expressions (marked in blue) in Figure 1a to the locked expressions (marked in red) in Figure 1b. The locked expressions use the additional relation bits \( r_2, r_3, \) and \( r_4 \), enabling that this locked design \( \hat{\varphi}(X, R) \) functions correctly when the secret relation \( \psi \) (Figure 1c) is installed. The relation \( \psi \) establishes the correct relation between the relation bits \( R \). The key relation can be excited by circuit inputs (like in \( r_0 \) and \( r_1 \)), constants, or random bits (e.g., from system noise, etc.); for example, the value \( \text{rand} \) in Figure 1c represents the random generation of a bit
\( t_0 = x_0 \land x_2 \)
\( t_1 = x_3 \land t_0 \)
\( t_2 = (x_1 \land t_0) \)
\( y_0 = x_0 \oplus x_2 \)
\( y_2 = (x_1 \land x_3) \lor t_2 \lor t_1 \)
\( y_1 = t_0 \oplus x_1 \oplus x_3 \)

(a) Original circuit

\( t_0 = x_0 \land x_2 \)
\( t_1 = (x_0 \land (r_4 \oplus r_2) \land x_3) \)
\( t_2 = (x_0 \land r_3) \)
\( y_0 = x_0 \oplus x_2 \)
\( y_2 = (x_1 \land x_3) \lor t_2 \lor t_1 \)
\( y_1 = t_0 \oplus x_1 \oplus x_3 \)

(b) Locked circuit

\{ (r_0 \leftrightarrow x_1), (r_1 \leftrightarrow x_2), (r_2 \leftrightarrow \text{rand}), (r_3 \leftrightarrow r_0 \land r_1), (r_4 \leftrightarrow r_1 \oplus r_2) \}

(c) Key relation

(0 or 1) assigned to \( r_2 \). The “output” from the key relation are bits \( r_3 \) and \( r_4 \) that must satisfy the relational constraints enforced by the key relation.

For the sake of simplicity, in the rest of the paper, we assume the relation bits are drawn only from the inputs \( X \) of the design. We will attempt to infer key relations of the form \( \psi(X, R) \). The reader may assume the value \( \text{rand} \) of in Figure 1c to be a constant value (say 0) to ease the exposition.

As \( \hat{\varphi} \) also consumes the relation bits \( R \), HOLL transforms the original circuit \( Y \leftrightarrow \varphi(X) \) into a locked circuit \( Y \leftrightarrow \hat{\varphi}(X, R) \) such that the locked circuit functions correctly if the relational constraint \( \psi(X, R) \) is satisfied. In other words, HOLL is required to preserve the semantic equivalence between the original and locked designs \((\varphi = \hat{\varphi} \land \psi)\). Note that it only imposes constraints on the input-output functionality of the circuits and the values generated off the internal gates may diverge. For example, in Figure 1b, the value of \( t_1 \) may be different from the one in the original design (Figure 1a), but the final output \( y_2 \) remains equivalent to the original adder.

This approach has analogies with the well-known logic locking solution \([11, 38, 55]\). Traditional logic locking produces a locked circuit by mutating certain expressions based on input key bits. HOLL differs from logic locking on the type of entities employed as hidden keys. While logic locking uses a key value (i.e., a sequence of key-bits), our technique uses a key relation (i.e., a functional relation among the key bits). We refer to our scheme as higher-order logic locking (HOLL). As synthesizing a relation (a second-order problem) is more challenging to recover than a bit-sequence (a first-order problem), HOLL is, at least in theory, is more secure than logic locking. Our experimental results (§8) show that this security also translates to practice.

**Hardware constraints.** Since the key relation must be implemented in the final circuit, we need to consider practical hardware constraints; details of the hardware implementation is provided in §7. For example, the size of the key relation affects the size of the programmable logic to be used for its implementation. This, in turn, introduces area and delay overheads in the final circuit. The practical realizability of this technique as a hardware device adds certain constraints:

- The key relation must be small for it to have a small area overhead;
The key relation must only be executed once to avoid a significant performance overhead;
- The key relation must encode non-trivial relations between the challenge and response bits to strong security;
- The locked expressions are evenly distributed across the design to protect all parts of the circuit, disallowing focused attacks by an attacker on a small part of the circuit that contains all locks.

Inferring the key relation. HOLL operates by

1. carefully selecting a set of expressions, \( E \subseteq \varphi \), in the original design \( \varphi \);
2. mutating each expression \( e_i \in E \) using the relation bits \( R \) to create the corresponding \emph{locked expression}, \( \hat{e}_i \).

For example, in Figure 1a, we select two expressions, \( E = \{e_1, e_2\} \) where \( e_1 = x_1 \land t_0 \) and \( e_2 = x_2 \land t_0 \). \( e_1 \) computes \( t_2 \) and is a function of \( t_0 \) and \( x_1 \), while \( \hat{e}_1 \) uses \( x_0 \) and \( r_3 \), which is in turn a relation of \( r_0 \) and \( r_1 \). We formalize our lock program synthesis problem as follows.

\[ \text{Lock Inference.} \quad \text{Given a circuit } Y \leftrightarrow \varphi(X), \text{ construct a locked circuit } Y \leftrightarrow \hat{\varphi}(X,R) \text{ and a key relation } \psi(X,R) \text{ such that } \hat{\varphi} \text{ is semantically equivalent to } \varphi \text{ with the correct relation } \psi. \]

Specifically, it requires us to construct: (1) a key relation \( \psi \) and (2) a set of locked expressions \( \hat{E} \) relating to the set of selected expressions \( E \) extracted from \( \varphi \) such that the following conditions are met:

- **Correctness:** The circuit is guaranteed to work correctly for all inputs when the key relation is installed:
  \[
  \forall X. (\forall R. \psi(X,R) \implies (\hat{\varphi}(X,R) = \varphi(X))) \tag{1}
  \]

  where \( \hat{\varphi} = \varphi[\hat{e}_1/e_1, \ldots, \hat{e}_n/e_n] \), for \( e_i \in E \subseteq \varphi \). The notation \( \varphi[e_a/e_b] \) implies that \( e_b \) is replaced by \( e_a \) in the formula \( \varphi \).

- **Security:** There must exist some relation \( \psi' \) (where \( \psi' \neq \psi \)) where the circuit exhibits incorrect behavior; in other words, it enforces the key relation to be non-trivial:
  \[
  \exists \psi \exists X \exists R. (\psi'(X,R) \implies \hat{\varphi}(X,R) \neq \varphi(X)) \tag{2}
  \]

We pose the above as a program synthesis problem. In particular, we search for “mutations” \( \hat{e}_1, \ldots, \hat{e}_2 \) and a suitable key relation \( \psi \) such that the above constraints are satisfied.

2.3 Attacking with SynthAttack

As we attempt to hide a relation instead of a key-value, prior attacks on logic locking (like SAT attacks), which attempt to infer key bit-strings, do not apply.
Table 1: In-out samples.

| X     | Y     | Ŷ     |
|-------|-------|-------|
| 1111  | 1110  | 110   |
| 1001  | 011   | 011   |
| 0000  | 000   | 000   |
| 1100  | 011   | 011   |
| 0101  | 010   | 110   |

\{(r_0 \leftrightarrow x_2),
 (r_1 \leftrightarrow x_0),
 (r_2 \leftrightarrow 0),
 (r_3 \leftrightarrow r_0 \land r_1),
 (r_4 \leftrightarrow 0)\}

Fig. 2: Generated key relation

However, the attackers can also use program synthesis techniques to recover the key relation using an activated instance of the circuit as an input-output oracle.

We design an attack algorithm, called SynthAttack, combining ideas from SAT attack (for logic locking) and counterexample guided inductive program synthesis. Our attack algorithm generates inputs \(X_1, X_2, \ldots, X_n\) and computes the corresponding outputs \(Y_1, Y_2, \ldots, Y_n\) using the oracle, to construct a set of examples \(\Lambda = \{(X_1, Y_1), \ldots, (X_n, Y_n)\}\). Then, the attacker can generate a key relation \(\psi\) that satisfies the above examples, \(\lambda\), using a program synthesis query:

\[
\prod_{X_i, Y_i \in \Lambda} \exists R_i \cdot \hat{\phi}(X_i, R_i) \land \psi(X_i, R_i) = Y_i
\]

The above query requires copies of \(\hat{\phi}(X, R)\) for every example—hence, the formula will quickly explode with an increasing number of samples. Our scheme is robust since the sample complexity of the key relationships increases exponentially with the number of relation bits employed. Additionally, the attacker does not know which input bits excite the key relation and how the relation bits are related to each other.

For the locked adder (Figure 1b) with the input samples shown in Table 1 (first four rows), the above attack can synthesize the key relation shown in Figure 2. Columns \(Y\) and \(\hat{Y}\) in Table 1 represent the outputs of the original circuit and the circuit obtained by the attacker, respectively. Even on a 4-bit input space, when 25% of all possible samples are provided, the attack fails to recover the key relation as shown by the last input row of Table 1. The red box highlights the output in the attacker circuit does not match the original design.

Definition (Distinguishing Input). Given a locked circuit \(\hat{\phi}\), we refer to input \(X\) as a distinguishing input if there exist candidate relations \(\psi_1\) and \(\psi_2\) that evoke semantically distinct behaviors on the input \(X\). Formally, \(X\) is a distinguishing input provided the following formula is satisfiable on some relations \(\psi_1\) and \(\psi_2\):

\[
\hat{\phi}(X, R_1) \neq \hat{\phi}(X, R_2) \land \psi_1(X, R_1) \land \psi_2(X, R_2)
\]

It searches for a distinguishing input, \(X_d\), that produces conflicting outputs on the locked design. Any such distinguishing input is added to the set of examples, \(\Lambda\), and the query repeated. If the query is unsatisfiable, it implies that no other

\footnote{All free variables are existentially quantified}
relation can produce a different behavior on the locked design and so the relation that satisfies the current set of examples must be a correct key relation.

Though SynthAttack significantly reduces the sample complexity of the attack, our experiments demonstrate that SynthAttack is still unsuccessful at breaking HOLL for larger designs.

3 Program Synthesis to Infer Key Relations

We represent the key relation $\psi$ as a propositional formula, represented as a set (conjunction) of propositional terms. The terms in $\psi$ belong are categorised as:

- **Stimulus terms**: As mentioned in §2, a subset of the relation bits are related to input bits or constants; the stimulus terms appear as $(r_i \leftarrow x_j)$ where $r_i \in R, x_j \in X \cup \{0, 1\}$.

- **Latent terms**: These clauses establish a relation among the relation bits; the variables $v$ in these terms are drawn from the relation bits $R$, i.e., $v \in R$.

For example, in Figure 1c the terms $(r_0 \leftarrow x_1)$, $(r_1 \leftarrow x_2)$, and $(r_2 \leftarrow \text{rand})$ are stimulus terms, while $(r_3 \leftarrow (r_0 \land r_1))$ and $(r_4 \leftarrow (r_1 \oplus r_2))$ are latent terms.

**Budget.** As the key relation may need to be implemented within a limited hardware budget, our synthesis imposes a hard threshold on its size. The threshold could directly capture the hardware constraints for implementing the key relation (e.g., the estimated number of gates or ports) or indirectly indicate the complexity of the key relation (e.g., number of relation bits, propositional terms, or latent terms).

3.1 Lock and Key Inference

Algorithm 1 outlines our algorithm for inferring the key relation and the locked circuit. The algorithm accepts an unlocked design $Y \leftrightarrow \varphi(X)$ and a budget $T$.

**Main Algorithm.** The algorithm iterates, increasing the complexity of the key relation, till the budget $T$ is reached (Lines 4-21). In every iteration, the algorithm selects a set of suitable expressions $E$ for locking, uses our synthesis procedure to extract a set of additional latent terms $H$ for the key relation, and produces the mutated expressions $\hat{e}_i$ for each expression $e_i \in E$ (Line 6).

If the additional synthesized relations keep the key relation within the budget $T$ (Line 5), the mutated expressions are replaced for $e_i \in E$ (Line 11). HOLL verifies that the solution meets the two objectives of correctness and security (§2). We handle correctness in the Synthesize procedure of Algorithm 1 and security in Lines 13-14 of the same algorithm. The CheckSec() procedure verifies if the synthesized (locked) circuit and key relations satisfy the security condition (Eqn 2). If CheckSec() returns True, the key relation $\psi$ and the locked circuit $\hat{\varphi}$ are returned; otherwise, synthesis is reattempted.
Algorithm 1: HOLL($\varphi, T, Q$)

1. $\psi \leftarrow \emptyset$
2. $\hat{\varphi} \leftarrow \varphi$
3. done $\leftarrow$ False
4. while not done do
5.   $E \leftarrow \text{SelectExpr}(\hat{\varphi})$
6.   $H, \hat{E} \leftarrow \text{Synthesize}(\psi, \hat{\varphi}, E)$
7.   $\psi' \leftarrow \psi \cup H$
8.   if Budget($\psi'$) $\leq T$ then
9.     $\psi \leftarrow \psi'$
10.    $\hat{\varphi} \leftarrow \hat{\varphi}[\{\hat{e}_i/e_i \mid e_i \in E, \hat{e}_i \in \hat{E}\}]$
11. else
12.    $q \leftarrow \text{CheckSec}(\psi, \hat{\varphi})$
13.    if $q$ then
14.      done $\leftarrow$ True
15.    else
16.      $\psi \leftarrow \emptyset$
17.      $\hat{\varphi} \leftarrow \varphi$
18.    end
19. end
20. return $\hat{\varphi}, \psi$

Correctness. HOLL attempts to synthesize (via the Synthesize procedure) a key relation $\psi$ and a set of locked expressions $\hat{e}_i$ such that the circuit is guaranteed to work correctly for all inputs given to $\psi$; this requires us to satisfy:

$$\exists \psi, \hat{e}_1, \ldots, \hat{e}_n. \forall X. \forall R. (\psi(X, R) \implies \hat{\varphi}(X, R) = \varphi(X))$$

(5)

where $\hat{\varphi} \equiv \varphi[\hat{e}_1/e_1, \ldots, \hat{e}_n/e_n]$, for $e_i \in (E \subseteq \varphi)$. In other words, we attempt to synthesize a set of modified expressions $\hat{E}$ that, once replaced the selected expressions in $E$, produces a semantically equivalent circuit as the original circuit if the relation $\psi$ holds. We solve this synthesis problem via counterexample-guided inductive synthesis (CEGIS) [4]. We provide a domain-specific language (DSL) in which $\psi$ and $\hat{e}_i$ are synthesized. CEGIS generates candidate solutions for the synthesis problem and uses violations to the specification (i.e. the above constraint) to guide the search for suitable programs $\psi$ and $\hat{e}_i$.

A problem with the above formulation is illustrated in Figure 4: the key relation in Figure 3a uses 5 gates without reusing expressions, “wasting” hardware resources. Figure 3b shows an optimized key relation that reuses the response bit $r_5$, allowing an implementation with only 3 gates. To encourage subexpression
(r₀ ← x₁),
(r₁ ← x₂), (r₂ ← x₀),
(r₅ ← (r₀ ∧ r₁)),
(r₄ ← ((r₀ ∧ r₁) ∧ r₂)),
(r₃ ← ((r₀ ∧ r₁) ∨ r₂))

(a) Without optimization

(r₀ ← x₁),
(r₁ ← x₂),
(r₂ ← x₀),
(r₅ ← (r₀ ∧ r₁)),
(r₃ ← (r₅ ∧ r₂)),
(r₄ ← (r₅ ∧ r₂))

(b) With optimization

Fig. 4: Key relations generated without and with optimization. In the optimized version, (r₀ ∧ r₁) in r₃ and r₄ is replaced by reusing the term r₅ similar to multi-level logic optimizations.

reuse, we solve this optimization problem:

\[ \arg\min_{\psi} \exists \psi', \hat{e}_1, \ldots, \hat{e}_n, \forall X. (\forall R. \psi(X, R) \implies \hat{\phi}(X, R) = \phi(X)) \]  

where \( \hat{\phi} \equiv \phi[e_1/e_1, \ldots, e_n/e_n] \), for \( e_i \in E \subseteq \varphi \).

**Security.** The security objective requires that the locking (i.e., the key relation \( \psi \) and the locked expressions) is non-trivial; that is, there exists some relation \( \psi' \neq \psi \) for which the circuit is not semantically equivalent to the original design:

\[ \exists \psi', \psi' \neq \psi, \text{ s.t. } \exists X. (\exists R. \psi'(X, R) \land \hat{\phi}(X, R) \neq \phi(X)) \]  

The above constraint is difficult to establish while synthesizing \( \psi \); it requires a search for a different relation \( \psi' \) that makes \( \hat{\phi} \) semantically distinct from \( \phi \) while \( \psi \) maintains semantic equivalence. Instead, we use a two-pronged strategy:

- We carefully design the DSL used to synthesize \( \psi \) and \( \hat{e}_i \) to reduce the possibility they generate trivial relations;
- After obtaining \( \psi \) and \( \hat{\phi} \), we attempt to synthesize an alternative relation \( \psi' \) (using \[8\]) such that \( \hat{\phi} \) is not semantically equivalent to \( \phi \), ensuring that \( \psi \) and \( \hat{\phi} \) do not constitute a trivial locked circuit.

\[ \exists \psi'. \exists X, R'. \phi(X) \neq \hat{\phi}(X, R') \land \psi'(X, R') \]  

The procedure \textit{CheckSec}(\( \psi, \hat{\phi} \)) (Algorithm 1, Line 13) implements the above check (Eqn. 8).

**Theorem 1.** If Algorithm 1 terminates, it returns a correct (Eqn. 1) and secure (Eqn. 2) locked design.

**Proof.** The proof follows trivially from the design of the \textit{Synthesize} (in particular, Eqn. 5) and \textit{CheckSec} (in particular, Eqn. 8) procedures (respectively).
3.2 Expression Selection

HOLL constructs the dependency graph \((V, D)\) for expression selection, where nodes \(V\) are circuit variables. A node \(v \in V\) represents an expression \(e\) such that \(v\) is assigned the result of expression \(e\), i.e. \((v \leftarrow e)\). The edges \(D\) are dependencies: the edge \(v_1 \rightarrow v_2\) connects the two nodes \(v_1\) to \(v_2\) if variable \(v_1\) depends on variable \(v_2\). The tree is rooted at the output variables and the input variables appear as leaves.

For example, Figure 5 shows the dependency graph for the circuit in Figure 1a. Triangles represent input ports \((x_0, x_1, x_2, x_3)\) while inverted triangles represent output ports \((y_0, y_1, y_2)\).

Our variable selection algorithm has the following goals:

1. **Ensure expression complexity**: The algorithm selects an expression \(e_z\) as a candidate for locking only if the depth of the corresponding variable \(z\) in the dependency graph lies in a user-defined range \([L, U]\) to create a candidate set \(Z\). The lower threshold \(L\) assures the expression captures a reasonably complex relation over the inputs, while the upper threshold \(U\) ensures the relation is not too complex to exceed the hardware budget. The algorithm starts by randomly selecting a variable \(z_0 \in Z\) from this set.

2. **Encourage sub-expression reuse in key relation**: We attempt to select multiple “close” expressions; for the purpose, the algorithm randomly selects variables \(w_i \in Z\) on which \(z_0\) (transitively) depend on.

3. **Encourage coverage**: We select expressions for locking in a manner so as to cover the circuit. To this end, interpreting \((V, D)\) as an undirected graph, we randomly select expressions \(u_i \in Z\) that are farthest from \(z_0\), i.e. the shortest distance between \(u_i\) and \(z_0\) is maximized.
Our algorithm first executes step (1), and then, indeterminately alternates between (2) and (3), till the required number of variables are selected. Let us use the dependency graph in Figure 5 to show how the above algorithm operates:

- Given the user-defined range $[1,3]$, we compose the initial candidate set $Z = \{y_0, t_0, t_1, t_2, y_1, y_2\}$.
- Let us assume we randomly pick the expression for $y_2$. Now, $y_2$ depends on expressions $t_0$, $t_1$ and $t_2$ ($\{t_0, t_1, y_2\} \subseteq Z$) [Rule 1].
- We randomly choose new expressions to lock/transform from $\{t_0, t_1, y_2\}$. For example, we select $t_2$ and $t_0$—[Rule 2].
- We find $y_0$, which is the furthest expression from $t_0, t_2, y_2$ in $Z$. We select to lock the set of expressions $\{y_1, y_2, t_0, t_2\}$—[Rule 3].

4 HOLL: Implementation and Optimization

Implementation. We implemented HOLL in Python, using SKETCH \[51\] synthesis engine to solve the program synthesis queries. We used BERKELEY-ABC \[9\] to convert the benchmarks into Verilog and PYVERILOG \[54\], a Python-based library, to parse the Verilog code and generate input for SKETCH. We use the support for optimizing over a synthesis queries provided by SKETCH to solve Eqn. 6. Algorithm 1 may not terminate; our implementation uses a timeout to ensure termination.

Domain Specific Language. We specify our domain-specific language for synthesizing our key relations and locked expressions. The grammar is specified as generators in the SKETCH \[51\] language. The grammar for the key relations and locked expressions is as follows:

\[
\langle G \rangle ::= r \leftarrow x \mid r \leftarrow \langle Bop \rangle r \mid r \leftarrow \langle Uop \rangle r \mid r \leftarrow r
\]

\[
\langle Bop \rangle ::= or \mid and \mid xor
\]

\[
\langle Uop \rangle ::= not
\]

The rule $\langle G \rangle ::= r \leftarrow x$ is only present in the key relation grammar since the locked expressions have no input bits.

Backslicing. To improve scalability, we use backslicing \[57\] to extract the portion of the design related to the expressions selected for locking. For a variable $v_i$, the set of all transitive dependencies that can affect the value of $v_i$ is referred to as its backslice. For example, in Figure 5 $\text{backslice}(t2) = \{t_0, x_0, x_1, x_2\}$.

Given the set of expressions $E$, we compute the union of the backslices of the variables in $E$, i.e. all expressions $B$ in the subgraph induced by $e \in E$ in the dependency graph; we use $B \subseteq E$ for lock synthesis.

Backslicing tilts the asymmetrical advantage further towards the HOLL defense. The attacker cannot apply backslicing on the locked design since the dependencies are obscured, preventing the extraction of the dependency graph.
Algorithm 2: SynthAttack($\tilde{\psi}$, $\parallel\tilde{\psi}(\psi)\parallel$)

1. $i \leftarrow 0$
2. $Q_0 \leftarrow \top$
3. while True do
   4. $X' \leftarrow \text{Solve}_X(Q_i \wedge$
      5. $(\tilde{\phi}(X, R_1) \neq \tilde{\phi}(X, R_2)) \wedge$
      6. $\psi_1(X, R_1) \wedge \psi_2(X, R_2))$
   7. if $X' = \bot$ then
      8. break;
   end
   9. $Y' \leftarrow \parallel\tilde{\phi}(\psi)(X')\parallel$
10. $Q_{i+1} \leftarrow Q_i \wedge (\tilde{\phi}(X', R_1') \leftrightarrow$
11. $Y') \wedge (\tilde{\phi}(X', R_2') \leftrightarrow Y')$
12. $\wedge \psi_1(X', R_1')$
13. $\wedge \psi_2(X', R_2')$
14. $i \leftarrow i + 1$
   end
17. $\psi_1, \psi_2 \leftarrow \text{Solve}_{\psi_1, \psi_2}(Q_i)$
18. return $\psi_1$

Incremental Synthesis. Given a set of expressions $E$, the procedure Synthesis in Algorithm 1 creates a list of relations $H$ and a new set of locked expressions $\hat{E}$. If the list of expressions is large, we select the expressions in the increasing order of their depth in the dependency graph. The lower the depth of the expression is, the closer it is to the inputs, and the simpler is the expression. Selecting an expression with the lowest depth first (say $e_1$) ensures that other expressions ($e_j$) depending on this expression can use the relations $H$ generated during synthesis of $\hat{e_1}$. This also makes synthesizing the other expressions easier as the current relation has some sub-expressions on which the new relations can be built.

5 SynthAttack: Attacking HOLL with Program Synthesis

As HOLL requires inference of relations and not values, existing attacks designed for logic locking do not apply. We design a new attack, SynthAttack, that is inspired by the SAT attack [53] for logic locking and counterexample-guided inductive program synthesis (CEGIS) [52].

5.1 The SynthAttack Algorithm

SynthAttack runs a counterexample-guided inductive synthesis loop: it accumulates a set of examples, $\Lambda$, by discovering some “interesting” inputs, and uses an activated circuit as an input-output oracle to compute its corresponding response. These examples, $\Lambda$, are used to constrain the space of the candidate
key-relations. SynthAttack then, uses a verification check to confirm if the collected examples are sufficient to synthesize a valid key-relation, i.e. one that provably activates the correct functionality on the locked circuit. Otherwise, the counterexample from the failed verification check is identified as an "interesting input" to be added to $\Lambda$, and the algorithm repeats. The verification check is based on the existence of a distinguishing input $\varphi$.

If there does not exist any distinguishing input for the locked circuit $\hat{\varphi}$, then $\hat{\varphi}$ has a unique semantic behavior—and that must be the correct functionality. Any key-relation that satisfies the counterexamples (distinguishing inputs) generated so far will be a valid candidate for the key relation. An inductive synthesis strategy based on distinguishing inputs allows us to quickly converge on a valid realization of the key-relation as each distinguishing input disqualifies many potential candidates for the key relation. Note that (as we illustrate the following example) there may be multiple, possibly semantically dissimilar, realizations of a key-relation that enables the same (correct) functionality on the locked circuit.

SynthAttack is outlined in Algorithm 2; the algorithm accepts the design of the locked circuit $\hat{\varphi}$ and an activated circuit $\hat{\varphi}(\psi)$ (the locked circuit $\hat{\varphi}$ activated with a valid key-relation $\psi$). The notation $\hat{\varphi}(\psi)$ indicates that this activated circuit can only be used as an input-output oracle, but cannot be inspected.

SynthAttack runs a counterexample-guided synthesis loop (Line 3). It checks for the existence of a distinguishing input in Line 4: if no such distinguishing input exists, it implies that the current set of examples is sufficient to synthesize a valid key-relation. So, in this case, the algorithm breaks out of the loop (Line 7-8) and synthesizes a key-relation (Line 17), that is returned as the synthesized, provably-correct instance for the key relation.

If there exists a distinguishing input $X'$ (in Line 4), the algorithm uses the activated circuit to compute the expected output $Y'$ corresponding to $X$ (Line 10). This new counterexample $(X', Y')$ is used to block all candidate key-relations that lead to an incorrect behavior, thereby reducing the potential choices for $\psi_1$ and $\psi_2$. The loop continues, again checking for the existence of distinguishing inputs on the updated constraint for $Q_i$. The theoretical analysis of SynthAttack is provided in §6.

The algorithm only terminates when it is able to synthesize a provably valid key-relation, that allows us to state the following result.

**Theorem 2.** Algorithm 2 will always terminate, returning a key-relation $\psi_1$ such that $\hat{\varphi}(\psi_1)$ is semantically equivalent to $\hat{\varphi}(\psi)$, where $\psi$ is the “correct” relation hidden by HOLL.

**Proof.** The number of loop iterations in the above procedure is upper-bounded by the number of distinguishing inputs and the number of distinguishing inputs is upper-bounded by the number of possible inputs (that is upper-bounded by $2^n$ where $n$ is the number of input of $\hat{\varphi}$). Hence, termination of the procedure is guaranteed. That the algorithm only returns a valid key-relation is ensured by the check for the existence of distinguishing inputs at Line 7 in Algorithm 2.
\{(r_0 \leftrightarrow x_1), \\\n(r_1 \leftrightarrow x_2), \\\n(r_2 \leftrightarrow r_0), \\\n(r_3 \leftrightarrow r_2 \land r_1), \\\n(r_4 \leftrightarrow \neg r_2 \land r_1)\}\}

Table 2: Distinguishing inputs.

| X   | Y   |
|-----|-----|
| 1101| 100 |
| 0001| 001 |
| 0101| 010 |
| 0111| 100 |
| 1001| 011 |
| 0011| 011 |

Fig. 6: Key relation generated by SynthAttack.

Example. Executing SynthAttack on Figure 1b iteratively generates six distinguishing inputs as shown in Table 2. Figure 6 shows the key relation synthesized by SynthAttack. This key-relation (Figure 6) is not semantically equivalent to the hidden key-relation that was computed and hidden by HOLL (Figure 1c). This shows that there may exist multiple valid candidates for the key-relation that all evoke the same functionality on the locked design. For example, \(X = 0100\) generates \(r_4 = 1\) for the key relation in Figure 1c but \(r_4 = 0\) for Figure 6; however, the output of the locked circuit remains the same in both cases (\(Y = 001\)).

6 Analysis of SynthAttack

The attack resilience of HOLL against SynthAttack can be captured by the total execution time (\(T\)) taken to generate a valid key-relation:

\[ T \geq \sum_{i=1}^{n} t_i \quad (9) \]

where \(n\) is the total number of distinguishing inputs (counterexamples) generated by the algorithm and \(t_i\) is the verification time (Algorithm 2, Line 4) in the \(i^{th}\) iteration of the loop (i.e. the time taken to generate the \(i^{th}\) distinguishing input or prove unsatisfiability). We say that a locked circuit, \(\hat{\varphi}\), is attack resilient against SynthAttack if \(T\) is sufficiently large. One can increase \(T\) by either increasing \(n\) or \(t_i\) (or both).

Verification Time (\(t_i\)). Line 11 in the Algorithm shows that the formula \(Q_i\) grows in each iteration (i.e. with \(i\)) by more than two times the size of the locked circuit \(\hat{\varphi}\). As the worst-case time for program synthesis increases exponentially with the size of the formula, successive iterations tend to get quite hard. This is also confirmed by our experimental results (§8.1).

Number of iterations (\(n\)). The number of iterations (\(n\)) depends on the number of distinguishing inputs accumulated till the verification check returns UnsAT. The number of distinguishing inputs is upper-bounded by the minimum of the number of possible inputs (that is exponential in the number of input ports)
and the number of possible functional relations that can be candidates for the key-relation (which is exponential in the number of relation bits). We attempt to increase $n$ by controlling the hardware budget for the key-relation and the expression selection heuristics (§3.2). Unfortunately, it is difficult to establish a non-trivial lower-bound; it depends on the design of the locked circuit and that of the key relation.

7 Hardware Implementation

We discuss how to hide the key relation from the untrusted foundry in a provably secure way. We need a solution to store the key relation as a program (not simply key bits), which must be hidden during chip fabrication. For this, we borrow concepts from programmable logic circuits that can implement any relation provided by a customer. The use of programmable devices is common in the hardware industry [2].

Depending on the key relation, we can use different solutions, based on the size and complexity of the key relation:

We can implement a simple relation with an embedded Programmable Array Logic (PAL). A PAL device includes a set of elements that can be programmed by the users with specialized machines. The transistors are arranged in a “fixed-OR, programmable-AND” plane to implement the well-known sum-of-products (SOP). In Boolean algebra, any relation $R$ can be expressed with an SOP form, also known as disjunctive normal form. The SOP form is then a canonical representation of the relation $R$. Most common logic synthesis tools can easily extract the SOP form associated with each relation bit $r_i$ to program the PAL. For example, given the relation $r_3 ← r_0 \land r_1 \lor r_2$ of Figure 3a, the corresponding SOP minterms are shown in Figure 7a, while Figure 7b shows its implementation with a single-output PAL.

PAL devices are fast and simple to program, but can only support small circuits. For example, the simple expression above has three literals but requires five minterms (so taking five gates in the AND plane). If the designer requires more complex relations that require more logic resources and even also storing capabilities, she can use an embedded Field-Programmable Gate Array (eFPGA). An eFPGA is a device composed of several configurable logic blocks, flip-flop registers, and heterogeneous resources interconnected with a reprogrammable fabric. In this case, the designer must use specific toolchains from the eFPGA provider to generate the proper configuration bitstream, i.e. the sequence of bits needed to specify the desired functionality [50].

In both cases, implementing a relation with programmable devices requires translating the specification into a configuration for all cells and/or switches. The more configurable cells, the more complex key relations we can implement. Without the correct configuration of all elements, the device cannot reproduce the correct relation. The attacker cannot know how many and which gates are used in the programmable device to implement the key relation. So, these devices can be a valid solution to securely store the key relation.
a = r_0 \cdot r_1 \cdot r_2 \\
b = r_0 \cdot r_1 \cdot r_2 \\
c = r_0 \cdot r_1 \cdot r_2 \\
d = r_0 \cdot r_1 \cdot r_2 \\
e = r_0 \cdot r_1 \cdot r_2 \\
r_3 = a + b + c + d + e

(a) Minterms and SOP form of the relation \( r_3 \).

We end this section with an important remark: the eFPGA configuration can be represented as a sequence of configuration bits. However, such a configuration bit-sequence represents a function, as compared to the key bits in traditional logic locking that simply represent a value. While any function can be encoded as a bit-sequence [16, 30], inferring a function bit-sequence is a computationally much harder problem (a second-order problem) as compared to inferring a value bit-sequence (a first-order problem). In the case of functions, only a complete configuration bit recovery allows the attacker to unlock the function. The complexity of inference lies in the complete interpretation of the entire bit-sequence, not in its simple or partial representation.

The circuit configurations from HOLL are one to two orders larger than the typical sizes of key bits in logic locking even when the key relation has a limited size [49]. Further, as the attacker does not know how the gates are used in the programmable device to implement the key relation, an attacker will have to consider all possible gate allocations, resulting in an impractical search over a huge design space.

8 Experimental Evaluation

We selected 100 combinational benchmarks from ISCAS’85 [1] and MCNC [60] and report the time for program synthesis and the overhead after applying our locking method. For long running experiments, we select a subset of 10 randomly selected benchmarks where, number of input ports range between 16 and 256, output ports range range between 7 and 245, AND gates range between 135 and 4174. Table 3 summarizes the ten selected benchmarks. We use BERKELEY-
Table 3: Our selected benchmark set.

| Ports | Bench | #IN | #OUT | #Total | #Gates |
|-------|-------|-----|------|--------|--------|
|       | al2   | 16  | 47   | 63     | 135    |
|       | cht   | 47  | 36   | 83     | 185    |
|       | C432  | 36  | 7    | 42     | 212    |
|       | C880  | 60  | 26   | 86     | 330    |
|       | i9    | 88  | 63   | 151    | 682    |
|       | i7    | 199 | 67   | 266    | 763    |
|       | x3    | 135 | 99   | 234    | 816    |
|       | frg2  | 143 | 139  | 282    | 1,233  |
|       | i8    | 133 | 81   | 214    | 2,175  |
|       | des   | 256 | 245  | 501    | 4,174  |

ABC to get the number of AND gates after we flatten the circuit using strash command.

For our experiments, we use the number of relation terms in the key relation as a proxy for its complexity. We define our budget in terms of it and use a budget threshold for the key relation in the range [12-14] latent terms and depth of expression selection in range [2-4]. We use a timeout of 20 minutes for locking and 4 days for attacks. We conduct our experiments on a machine with 32-Core Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz with 32GB RAM.

For both HOLL and SynthAttack, we use the Sketch synthesis tool. Since synthesis solvers are difficult to compare across different problem instances, we were wary of the case where the defender gets an edge over the attacker due to use of different tools. We create the attack-team-defence-team asymmetry by controlling the computation time: while the defender gets 20 minutes (1200s) to generate locked circuit, the attacker runs the attack for up to 4 days.

Our experiments aim to answer five research questions:

**RQ1.** What is the attack resilience of HOLL? ($8.1$)

**RQ2.** How do impact expression selection heuristics affect attack resilience? ($8.2$)

**RQ3.** What is the hardware cost for HOLL? ($8.3$)

**RQ4.** What is the time taken to synthesize the locked design and key-relation for HOLL? ($8.4$)

**RQ5.** What are the impact of the optimizations for scalability (backslicing and incremental synthesis)? ($8.5$)

Here is a summary of our findings:
Security. The key relations can be recovered completely by the attacker via SynthAttack but only for small circuits with a small hardware budget. For medium and large designs, key relations are fast to obtain (<1200s) but cannot be recovered by our attack even within 4 days. This shows our defense is efficient while our attack is strong but not scalable.

Hardware Cost. Our key relations with a budget of 12–14 latent terms have a minimal impact on the designs and the overhead reduces as the size of the circuit grows. On the largest benchmark, the area overhead is 1.2%. The corresponding configurations for programmable devices are small and provide high security.

HOLL Performance. The HOLL execution time ranges between 8s and 1001s, with an average of 33s for small, 17s for medium, and 60s for large designs for the budget of 8–10 latent terms. Our optimizations are crucial for the scalability of our HOLL defense (locking) algorithm: we fail to lock enough expressions in large circuits without these optimizations.

8.1 Attack Resilience

We define attack resilience of locked circuit, $\hat{\phi}$, in terms of time taken to obtain a key relation, $\psi'$, such that $\hat{\phi} \land \psi'$ is equivalent to original circuits, $\varphi$.

Attack time. Figure 8 shows the cumulative time spent till the $i^{th}$ iteration (y-axis) of the loop versus the loop counter $i$, that is also the number of distinguishing inputs (samples) generated so far (x-axis). We show exponential trend curves (as a solid pink line) to capture the trend in the plotted points while the data-points are plotted as blue dots. The plots show that the plotted points follow the exponential trend lines, illustrating that SynthAttack does not scale well, thereby asserting the resilience of HOLL.

SynthAttack failed to construct a valid key-relation for any of these ten designs within a timeout of 4 days. However, for small designs with lesser number of latent terms, SynthAttack was indeed able to construct a valid key-relation. For example, SynthAttack is able to construct a valid key-relation for the benchmarks a12 and i9 within 10 hours for 7 latent terms, respectively (see Figure 9).

Attack resilience vs. number of latent terms. The complexity of the key relation increases with the number of relation bits. As shown in Figure 9 (for benchmarks a12 and i9), the time required to break the locked circuit increases exponentially as the number of relation bits increases. We gave a timeout of 10 hours for this experiment and a12 timed out at 9 latent terms, and i9 timed out at 8 latent terms. Both results are for locked circuits with variables selected with the depth of locked expression, $\hat{c}_i$, equal to 1.
Fig. 8: figure
Cumulative time for successive iterations of SynthAttack (best viewed in color)
8.2 Impact of Expression Selection on Attack Resilience

Attack resilience vs. Depth of locked expression. The attack resiliency of $\hat{\varphi}$ increases significantly as we increase the depth of the locked expression selected for HOLL for $\varphi$. We observe that for a number of latent terms in key relation equal to 2, for benchmark a2l, increases from 213s to 3788s for depth 1 and 2, respectively. For benchmark i9, attack time increases from 351s to 1141s for depth 1 and 2, respectively.

Attack time vs. Coverage. To show the effect of coverage we select expressions (in $e_i \in E$) such that the distance (3.2) among the expressions is largest (termed as diverse) and smallest (termed as converged). When the coverage of locked expressions is larger, i.e. locked expressions are spread out in the circuit, the attack requires more time than breaking locked expressions limited in one locality. For example, for benchmarks C432 and i9, attack time increases from 115s to 142s and 229s to 316s, respectively, when expression selection heuristic is changed from converged to diverse. The results are with three latent terms.

8.3 Hardware cost

The key relations can be implemented either as embedded Field Programmable Gate Array (eFPGA) or Programmable Array Logic.

We synthesize the original and locked designs with SYNOPSYS DESIGN COMPILER R-2020.09-SP1 targeting the Nangate 15nm ASIC technology at standard operating conditions (25°C).

Table 4 provides the estimated cost for implementing the key relations with programmable devices. To do so, we compute the number of equivalent NAND2 gates used to estimate the number of 6-input LUTs. Given the number of LUTs, we provide an estimation of the equivalent number of configuration bits—including those for switch elements. Results show that the size of the key relations is independent of the size of the original design. Table 4 reports the fraction of the area locked with HOLL (key relation) to the area of the original circuit. The results show that the impact of HOLL is low, especially for large designs.
Table 4: Hardware Impact of HOLL.

| Bench | Orig. Area (µm²) | Key Relation Area (µm²) | #Eq. LUT | #Eq. conf. bits | Overhead Area (%) |
|-------|-----------------|--------------------------|-----------|----------------|------------------|
| a12   | 17.89           | 4.473                    | 138       | 8,832          | 25.0             |
| cht   | 20.74           | 4.178                    | 132       | 8,448          | 20.1             |
| C432  | 20.05           | 4.866                    | 150       | 9,600          | 24.3             |
| C880  | 50.04           | 4.325                    | 132       | 8,448          | 8.6              |
| i9    | 77.07           | 4.129                    | 126       | 8,064          | 5.4              |
| i7    | 80.41           | 4.129                    | 126       | 8,064          | 4.3              |
| x3    | 95.21           | 5.014                    | 156       | 9,984          | 5.3              |
| frg2  | 100.81          | 4.669                    | 144       | 9,216          | 4.6              |
| i8    | 120.37          | 4.325                    | 132       | 8,448          | 3.6              |
| des   | 445.37          | 5.554                    | 174       | 11,136         | 1.2              |

(a) Time for 100 benchmarks
(b) Time vs # relation bits for a12

Fig. 10: Execution time for program synthesis.

8.4 HOLL Lock Inference Time

Figure 10a shows the size of the circuit has minimal impact on the time for inferring the key relations, thanks to backslicing (§4). The number of gates in the benchmarks increases as we move along the x-axis, which is on a logarithmic scale. The data is for 100 benchmarks with the number of latent terms in the range [8, 10]. Figure 10b shows the number of relation bits has a linear impact on the time for key relation inference. We select expression selection depth in range [2-4], HOLL timeouts (20 minutes) for inferring the key relation when lower limit of depth is increased to 3 or upper limit to 5 for benchmark a12. We try to keep the depth as high as possible so that the attack resilience for SynthAttack is more (§8.2).

8.5 Impact of HOLL Optimizations

Incremental vs. Monolithic Synthesis This experiment shows the advantage of incremental synthesis versus monolithic synthesis (§4). As can be seen
Table 5: Impact on HOLL time.

(a) Incremental for x3

| Time (sec.) | # of expressions |
|-------------|------------------|
| Monolithic  | 1 31 timeout 4 hrs |
| Incremental | 1 2 8 9 12 13 14 |

(b) Impact of backslicing (bkslice) for a12

| Time (sec.) | # of expressions |
|-------------|------------------|
| with bkslice | 4 timeout 4 hrs |
| w/o bkslice  | 1 2 25 512 513 514 548 642 |

in Table 5a for benchmark x3, monolithic synthesis does not scale beyond two expressions (even with a 1 day timeout for synthesis) while incremental synthesis synthesizes key relations for 7 locked expressions within 15s. We provided exactly the same set of expressions in both cases. While the results of incremental synthesis may be sub-optimal, we found them close to the optima in most cases. Figure 11 shows the key relations synthesized by the two settings when the threshold for the number of expressions is 2: both the algorithms generate compact relations with 8 terms (five stimulus and three latent terms) and using 8 relation bits.

(a) Monolithic synthesis

\{(r_0 \leftrightarrow i0), (r_1 \leftrightarrow j0),
(r_2 \leftrightarrow d2), (r_3 \leftrightarrow m0),
(r_4 \leftrightarrow l0), (r_5 \leftrightarrow (r_1 \lor r_0)),
(r_6 \leftrightarrow (\neg r_3)),
(r_7 \leftrightarrow (r_2 \land r_4))\}

(b) Incremental synthesis

\{(r_1 \leftrightarrow i0), (r_2 \leftrightarrow j0),
(r_3 \leftrightarrow d2), (r_0 \leftrightarrow m0),
(r_4 \leftrightarrow l0), (r_6 \leftrightarrow (r_2 \lor r_1)),
(r_5 \leftrightarrow (\neg r_0)),
(r_7 \leftrightarrow (r_3 \land r_4))\}

Fig. 11: Key relations generated for two expressions of x3.

Backslicing Backslacing (§4) is a critical optimization as shown in Table 5b. For example, if backslicing is disabled for the benchmark a12, HOLL is not able to generate a key relation beyond 2 expressions with a timeout of 4 hours. Instead, when backslicing is active, the HOLL performance is linearly dependent on the number of locked expressions to infer. These results are with depth of variable selection in range [2, 4].
9 Related Work

Logic Locking: Attacks and Defenses. Existing logic locking methods aptly operate on the gate-level netlists [55]. Gate-level locking cannot obfuscate all the semantic information because logic synthesis and optimizations absorb many of them into the netlist before the locking step. For example, constant propagation absorbs the constants into the netlist. Recently, alternative high-level locking methods obfuscate the semantic information before logic optimizations embed them into the netlist [38, 18]. For example, TAO applies obfuscations during HLS [38] but requires access to the HLS source code to integrate the obfuscations and cannot obfuscate existing IPs. Protecting a design at the register-transfer level (RTL) is an interesting compromise [30, 11]. Most of the semantic information (e.g., constants, operations, and control flows) is still present in the RTL and obfuscations can be applied to existing RTL IPs. In [30], the authors propose structural and functional obfuscation for DSP circuits. In [11], the authors propose a method to insert a special finite state machine to control the transition between obfuscated mode (incorrect function) and normal mode (correct function). Such transitions can only happen with a specific input sequence. Differently from [14], we extract the relation directly from the analysis of a single RTL design, making the approach independent of the design flow. None of these methods consider the possibility of hiding a relation among the key bits.

Program Synthesis. Program synthesis has been successful in many domains: synthesis of heap manipulations [40, 21, 59], bit-manipulating programs [28], bug synthesis [42], parser synthesis [31, 38], regression-free repairs [7, 6], synchronization in concurrent programs [58], boolean functions [23, 25, 24] and even differentially private mechanisms [39]. There has also been an interest in using program synthesis in hardware designs [17]. VeriSketch [5] exploits the power of program synthesis in hardware design. Our work is orthogonal to the objectives and techniques of VeriSketch: while VeriSketch secures hardware against timing attacks, we propose a hardware locking mechanism. Zhang et al. [64] use SyGUS based program synthesis to infer environmental invariants for verifying hardware circuits. We believe that this work shows the potential of applying programming languages techniques in hardware design. We believe that there is also a potential of applying program analysis techniques, both symbolic [10, 22, 13, 37, 35], dynamic [43, 15] and statistical [29, 33, 12, 34], for hardware analysis; this is a direction we intend to pursue in the future.

10 Discussion

We end the paper with an important clarification: the eFPGA configuration in HOLL can also be represented as a bit sequence (i.e., a sequence of configuration bits). So, why can an attacker not launch attacks similar to SAT attacks on logic locking to recover the HOLL configuration bitstream?
The foremost reason is that while the key-bits in traditional logic locking simply represent a value that the attacker attempts to recover, the bit-sequence in HOLL is an encoding of a program \cite{16,36}. This raw bit-sequence used to program an eFPGA is too “low-level” to be synthesized directly—the size of such bit-streams is about 60-85 times of the keys used in traditional logic locking (128 key bit-sequence). So, the HOLL algorithm designer uses a higher-level domain-specific language (DSL) to synthesize the key relation (see \S4), that is later “compiled” to the configuration sequence. The attacker will also have to use a similar strategy of using a high-level DSL to break HOLL.

However, while the designer of the key relation can use a well-designed small domain-specific language (DSL) that includes the exact set of components required (and a controlled budget) to synthesize the key relation, the attacker, not aware of the key relation or the DSL, will have to launch the attack with a “guess” of a large overapproximation. In other words, the domain-specific language used for synthesis is also a secret, thereby making HOLL much harder to crack than traditional logic locking.

We evaluate HOLL (\S8.1) under the assumption that the DSL (and budget) are known to the attacker. In real deployments (when the DSL is not known to the attacker), HOLL will be still more difficult to crack.

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