The suppression of DC-link voltage fluctuations through a source active current feedforward in the active power filter

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Abstract

An active power filter (APF), which operates under the power-balance-based scheme (PB scheme), suffers heavier DC-link voltage fluctuation when the loads change suddenly, so that it is apt to be interfered and degraded or even out of stable operation. By analyzing the cause of DC-link voltage fluctuation, this study proposes an improved PB scheme which feeds forward the increment of the fundamental-frequency positive sequence component of the source current. The feed-forward channel is designed by use of the cascaded delayed signal cancellation algorithm and integrated into the conventional PB scheme APF without adding any extra hardware circuit. The current increment fed forward is added into the output of the voltage controller to timely amend the reference current of the current control loop, and thus the active power flow, which caused by loads change, between the APF and its external circuitry can be suppressed. As a result, the DC-link voltage fluctuation is mitigated to allow the APF to better accommodate the abrupt load changes. The configuration of the improved control system is introduced and the stability is analysed. The experiment results demonstrate the effectiveness of the proposed control scheme.

1 INTRODUCTION

Following the widespread use of various non-linear loads and harmonic-susceptive loads, along with increasing renewable energy generators being put into operation via PWM converters, the power quality issues became significant and urgent [1–5]. The active power filter (APF) is widely used to eliminate harmonics and reactive currents for better power quality of distribution systems [6–9]. Whether the target harmonic components are needed to be detected from load or source currents leads to two APF control schemes: the harmonic-extraction-based scheme (HE scheme) and the power-balance-based scheme (PB scheme).

In the HE scheme [10–14], the harmonic components must be detected and extracted from load or source currents first, so as to produce the corresponding same amplitude and antiphase harmonic currents and inject them into the point of common coupling (PCC) to maintain the source current as a sinusoid in phase with the grid voltage. Therefore, the HE scheme is always considered as an open-loop system, some factors such as the harmonic sensing and acquiring circuits, the harmonic extraction algorithm and the current control methods will easily affect the performance of the HE-based APF in the practical field. Comparatively, the PB scheme calculates the reference value of the source side current through the DC voltage regulation link and directly controls the source side current, which is regarded as a controlled variable to form a close-loop system from the point of the entire power distribution system and has the advantages of high accuracy and robustness with low requirements of the parameters matching [15–18].

The PB scheme exhibits a more promising filtering performance. However, the serious oscillation of the DC-link voltage will occur at some sudden load change conditions when an APF employs the existing PB scheme [19]. It decreases the DC voltage utilisation and deteriorates the compensating performance of the APF, and even induces the instability and even damages the APF, limiting the application of APFs in occasions of frequent load changes such as traction motor,

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beam-pumping unit and so forth. Therefore, how to keep the oscillation of the DC-link voltage within a reasonable range is vital for implementation of the PB scheme in an APF.

There have been some reports regarding to improve the APF performance via regulating its DC-link voltage [19–28]. Literature [20] suggests suppressing the DC-link voltage oscillation in transient states by controlling the energy flowing into the DC capacitor to be zero in one source cycle. Afterwards, a more accurate 7-step compensator had been presented in [21] to maintain the mean active-power flowing into or out of the DC capacitor at zero every 1/(k – 1) source cycle. Based on this, Tomoyuki et al. modified the voltage feedback reference utilising the calculated value of the theoretical stored energy ripple [22]. Considering the impact induced by the third-order harmonic current compensation, an additional fundamental current compensating scheme was used in [23] to suppress DC-link voltage impulse. In order to enhance the dynamic performance of the APF under load variation condition, a controller based on online trained recurrent probabilistic fuzzy neural network with an asymmetric membership function (RPFN-AMF) had been developed to substitute for the conventional proportional-integral (PI) controller in [24]. Additionally, some non-linear and adaptive control strategies were studied [25–27]. However, these approaches are only suitable for the HE scheme APF and not for the PB scheme APF.

In the studies of the PB scheme APF, a modified one cycle control scheme was proposed in [15] to distinguish harmonic components from reactive components of load currents and an advanced control strategy with the conventional PI and vector PI controller was proposed in [30] to enhance the compensation performance. However, the DC-link voltage regulation performance of the APF was still poor. To overcome the DC-link voltage fluctuation of the PB scheme APF, a feed-forward method has been used, in which the fundamental component is filtered out from the load current and fed forward to improve the dynamic speed of responding to load change [18]. Undoubtedly, it is an effective restraint method against the DC-link voltage impulse. In order to enhance the dynamic performance of the APF under load variation condition, a controller based on online trained recurrent probabilistic fuzzy neural network with an asymmetric membership function (RPFN-AMF) had been developed to substitute for the conventional proportional-integral (PI) controller in [24]. Additionally, some non-linear and adaptive control strategies were studied [25–27]. However, these approaches are only suitable for the HE scheme APF and not for the PB scheme APF.

The features of the existing relevant schemes are summarised in Table 1 for easier comparison. It can be seen from Table 1 that the proposed method requires less sensors and can eliminate the DC-link voltage fluctuation of the PB scheme to achieve satisfactory harmonics compensation performance by simpler computation.

On the basis of analysing the relationships of the source current, the APF current and the DC-link voltage fluctuation, this study introduces a source current feed-forward channel into the conventional PB scheme to mitigate the DC-link voltage fluctuation. By feeding the increment of the source active current forward and adding it to the output of the voltage control loop (VCL) to amend the reference current of the current control loop (CCL), the proposed improved PB scheme finally managed to prevent the active-power from flowing into or out of the APF. In this study, the cascaded delayed signal cancellation (CDSC) operator has been used to design the feed-forward channel to extract control signals from the source current effectively. The proposed method can be developed without adding any extra hardware circuit and can share the same algorithm (i.e. CDSC) with PLL, thus it is easier to be integrated into the existing PB scheme based APF.

The rest of this study is organised as follows. The proposed method of the source active current feed-forward is derived based on the analysis of the cause of DC-link voltage fluctuation in Section 2. The implementation of the proposed method is introduced in Section 3, including the configuration of DC-link voltage and current regulators, the design of newly added feed-forward link and the stability analysis of the improved PB scheme. Experiments have been conducted to compare the performances of the conventional and improved PB schemes in Section 4. Section 5 gives a conclusion and Section 6 gives the acknowledgements.

| Scheme          | Harmonics filtering | $u_{dc}$ Regulation | Sensors number | Computation |
|-----------------|---------------------|---------------------|----------------|-------------|
| CS scheme       | Poorer              | Good                | 10             | Complex     |
| PB scheme       | Good                | Poorer              | 7              | Simple      |
| Improved CS scheme [14] | Good                | Good                | 10             | Moderate    |
| Improved PB scheme [18] | Good                | Good                | 10             | Complex     |
| Improved PB scheme [19] | Good                | Moderate            | 7              | Complex     |
| Proposed scheme | Good                | Good                | 7              | Simple      |

CS scheme: Current-source-based scheme.
2 | THE CAUSE OF DC-LINK VOLTAGE FLUCTUATIONS AND THE SUPPRESSING SOLUTION

2.1 | The APF configuration and the cause of DC-link voltage fluctuation

Figure 1 presents the one-line diagram of a three-phase shunt APF with the schematic of the PB scheme. It takes voltage source converter (VSC) as the power circuit and accesses PCC through a LCL low pass filter (LPF) to filter switching frequency noises. The symbols involved are defined as follows, where bold letters denote three-phase variables:

\[
\begin{align*}
\text{Grid voltage } \epsilon &= \begin{bmatrix} \epsilon_{a} \epsilon_{b} \epsilon_{c} \end{bmatrix}^T; \\
\text{Phase signal of grid voltage } \epsilon_{ph} &= \begin{bmatrix} \epsilon_{pha} \epsilon_{phb} \epsilon_{phc} \end{bmatrix}^T; \\
\text{Source current } \bar{i} &= \begin{bmatrix} \bar{i}_{a} \bar{i}_{b} \bar{i}_{c} \end{bmatrix}^T; \\
\text{Reference source current } \bar{i}_{sref} &= \begin{bmatrix} i_{srefa} i_{srefb} i_{srefc} \end{bmatrix}^T; \\
\text{Amplitude of the reference source current } I_{sref} &= \begin{bmatrix} i_{srefa} i_{srefb} i_{srefc} \end{bmatrix}^T; \\
\text{Source current error } \Delta \bar{i} &= \begin{bmatrix} \Delta i_{srefa} \Delta i_{srefb} \Delta i_{srefc} \end{bmatrix}^T; \\
\text{Load current } \bar{I} &= \begin{bmatrix} \bar{I}_{a} \bar{I}_{b} \bar{I}_{c} \end{bmatrix}^T; \\
\text{Compensation current } \bar{I} &= \begin{bmatrix} i_{ca} i_{cb} i_{cc} \end{bmatrix}^T; \\
\text{DC-link voltage } u_{dc}; \\
\text{DC-link voltage error } \Delta u_{dc}; \\
\text{DC-link capacitor } C_{dc}; \\
\end{align*}
\]

As observed from Figure 1 that the APF utilises the double close loop structure:

- The inner CCL for the supply current regulation.
- The outer VCL for the DC-link voltage regulation.

Only three kinds of electric variables (\(e, i, u_{dc}\)) need to be detected for the PB scheme control implementation. \(e\) is sent to the phase-locked loop (PLL) to provide the \(s_{ph}\), which tracks the real-time phase of the grid voltage. \(u_{dc}\) is fed to the outer loop to compare with \(U_{dc}\) first, and then the compared result \(\Delta u_{dc}\) turns into the voltage regulator (VR) to generate the desired \(I_{sref}\), which multiplies \(s_{ph}\) to get \(i_{sref}\). Finally, \(i_{s}\) is directly fed back to track its reference \(i_{sref}\) and the error signal \(\Delta i_{s}\) is fed to current regulator (CR) to produce compensating signal. It is thus obvious that an APF with the PB scheme not only saves sensors but also avoids designing the complicated harmonics extraction link, and this also makes the CR computation more efficient relatively. However, a defect of heavy DC-link voltage fluctuation would begin to surface when this control scheme faces abrupt load changes.

Why does the PB scheme induce a poor performance under the severe load variations? How to speed up the dynamic response of the source current to the load change and reserve excellent steady state filtering performance of the APF at the same time? To solve these problems, this study turns to the control block diagram of the conventional PB scheme shown in Figure 2 to find the factors in slowing down the speed of response to abrupt load changes.

As shown in Figure 2, the sudden change of \(i_{s}\) will certainly lead to a corresponding change of \(i_{s}\) first, but this incipient change of \(i_{s}\) will be suppressed swiftly by the CCL because its reference, \(i_{sref}\), still remains unchanged. However, due to the system need of maintaining a power balance, the power difference between the source and the load has to be supplemented instantly by the APF current \(i_{s}\) that comes from charging or discharging the DC-capacitor, and this will make for a DC-link voltage fluctuation, which is also the only variable to reflect the active-power change of the system according to the PB scheme. Subsequently, after the time-consuming filtering and regulating process of the VCL, the VR generates the updated \(I_{sref}\) with the changed \(u_{dc}\), and then new value of \(i_{sref}\) is obtained by modulating \(I_{sref}\) with \(s_{ph}\), and thus the updated \(i_{s}\) can finally be obtained, via the CCL, to fit the changed load and recover the value of DC-link voltage.

From the above adjustment process after the load changes, it can be discerned that the \(u_{dc}\) fluctuation cannot be eliminated completely because the power imbalance originated from the load change has not been sensed by the control system until it gave rise to variation of \(u_{dc}\). Furthermore, the VCL has only a narrow frequency band in general to prevent the DC-link voltage ripple from entering the CCL, which also further prolongs
the update duration of $i_{\text{ref,ag}}$ and aggravate the fluctuation of $u_{\text{dc}}$

2.2 The solution to suppress the DC-link voltage fluctuation

According to the aforementioned analysis, in the transient process, a part of active-power which should have been supplied directly to the load from the source, now with interventions from the APF controller, has to be buffered by the APF before being provided to the load. This is exactly the operating principle of the PB scheme as well as the intrinsic reason of $u_{\text{dc}}$ fluctuation. Therefore, trying to speed up the update speed of $i_{\text{ref,ag}}$ to keep up with the changed $i_t$ could be the fundamental approach to lessen the exchange capacity of instantaneous active power between the APF and its external circuitry to suppress the excessive $u_{\text{dc}}$ fluctuation. Improving the dynamic performance of the VCL would broaden its frequency band and leak some voltage ripples into CCL, which would degrade the harmonics compensation performance and even lead to an instability of the whole control system. Taking the active component of $i_t$ as a feed-forward signal and adding it to the initial value of $i_{\text{ref,ag}}$ could help acquiring new reference current more quickly [18], however, additional sensors for load currents measurement would not only increase cost but also make the system more complicated.

Considering the relationship between $i_t$ and $i_t$ in the PB scheme based APF, the fundamental-frequency active component (FFAC) increment of source current, $\Delta i_{\text{sp}}$, is an appropriate variable as a feed-forward signal to modify the current reference of the CCL.

From Figure 1, there is

$$i_t = i_t - i_c$$  \hfill (1)

When the system goes into steady state, currents $i_s, i_c, i_l$ meet following expressions:

$$\begin{cases} 
  i_s = i_{sp} \\
  i_c = i_{lh} - i_p \\
  i_l = i_{lh} + i_p 
\end{cases}$$  \hfill (2)

where $i_{sp}$ is the FFAC of source current, and $i_{sp}, i_{lh}$ are the FFAC and other components of the load current respectively, $i_p$ is the dissipating current of APF itself. From Equations (1) and (2), Equation (3) can be obtained as

$$i_s = i_{sp} = i_{lp} + i_p$$  \hfill (3)

After the load changed to $i'_t$ as

$$i'_t = i_t + \Delta i_t = i_t + \Delta i_{lp} + \Delta i_{lh}$$  \hfill (4)

and in view of the change possibility of $i_p$ throughout the control process, the source current would change with the load and produce corresponding increment $\Delta i_t$ as

$$\Delta i_t = \Delta i_l + \Delta i_p = \Delta i_{lp} + \Delta i_{lh} + \Delta i_p$$  \hfill (5)

where $\Delta i_{lp}, \Delta i_{lh}$ and $\Delta i_p$ are the increments of $i_{lp}, i_{lh}$ and $i_p$ respectively. The corresponding active power current variation is the increment of $i_{sp}$, that is

$$\Delta i_{sp} = \Delta i_{lp} + \Delta i_p.$$  \hfill (6)

From Equation (6), $\Delta i_{sp}$ represents the total active power current demand of the whole APF system caused by the load change. Therefore, it is more reasonable to use $\Delta i_{sp}$ instead of $\Delta i_{lp}$ as a feed-forward signal to help updating the reference input of CCL more quickly.

Moreover, according to the PB scheme, $i_t$ is constantly controlled to track $i_{lp}$ by the close loop control system, so its fundamental frequency positive sequence (FFPS) component is automatically equal to $i_{lp}$ when the system reaches a dynamic balance. They both have the same phase with the grid voltage, that is, the output phase of the PLL. Thus, only the amplitude increment of FFPS component is needed to be directly added up to the output of the VR as shown in Figure 3.

Figure 3 shows the modified control system structure of the proposed strategy for the PB scheme APF. A feed-forward channel made up of the CDSC filter and the amplitude increment operator (AIO) is added to the conventional PB scheme. The CDSC filter is employed to extract the FFPS component, $i_{sp,ag}$, from $i_t$. Then, the amplitude of $i_{sp,ag}$ and its increment for every interval $\Delta i_t$, denoted by $\Delta i_{sp}$, are figured out by the AIO and sent to merge with $I_{\text{ref}}$ to form the modified amplitude of the current reference, $I'_{\text{ref}}$, which can be expressed as

$$I'_{\text{ref}} = I_{\text{ref}} + \Delta I_{sp}$$  \hfill (7)

The updated reference input of CCL is eventually gained as

$$I'_{\text{ref,ff}} = I'_{\text{ref}} \Delta \phi_{ph,ff}$$  \hfill (8)
3 IMPLEMENTATION OF THE PROPOSED SCHEME

From Figure 3, it is demonstrated that only a feed-forward branch is to be added and nothing else of the conventional control system of the PB scheme APF needs to be changed in the proposed strategy. So, classical control methods such as PI control and proportional-resonant (PR) control are still suitable for the VR and CR. The configuration of relevant controllers will be presented below. The crucial performance of the feed-forward channel is its rapidity. In order to shorten the signal processing time, the CDSC algorithm was designed to extract the FFPS current from \( i_s \) in the study.

3.1 Configuration of DC-link voltage regulator and current regulator

In this study, the control model has been established on the basis of instantaneous energy balance principle [37]. A PI controller has been employed as the VR, whose transfer function \( G_{VR}(s) \) is

\[
G_{VR}(s) = k_{VP} + \frac{k_{V1}}{s}
\]  

where \( k_{VP} \) affects response speed and stability of VR, and \( k_{V1} \) is related to static errors and dynamic performance of VR.

According to the internal model principle, a PR controller in a stationary reference frame is able to compensate the target harmonics without steady-state tracking errors [38]. In order to avoid the instability derived from an infinite gain and to improve the adaptability to frequency jitters, a quasi-PR controller has been applied here, combining with an integral unit, to form the CR which transfer function \( G_{CR}(s) \) is expressed as

\[
G_{CR}(s) = k_{CP} + \frac{k_{CI}}{s} + \sum_{n=3,5,9} \frac{\omega_n}{s^2 + \omega_n s + (\omega_n)^2}
\]  

In Equation (10), \( k_{CP} \) and \( k_{CI} \) have the similar effects on CR as \( k_{VP} \) and \( k_{V1} \) have on VR. The value of resonant coefficient \( k_{CR,n} \) affects system immunity and actual effect of compensation for the target harmonics \((\omega_n)\), and the cutoff angle frequency \( \omega_C \) can change the bandwidth around \( \omega_C \). In this study, \( k_{CP} \) and \( k_{CI} \) were adjusted to meet requirements of stability, dynamic and steady-state performance, and \( \omega_C \) was selected to put up with frequency jitter from 49.5 to 50.5 Hz. The specific parameters of the VR and CR are shown in Table 2.

3.2 Design of the CDSC-filter for the FFPS component

The CDSC filter is made up of several delayed signal cancellation (DSC) operators. For ease of presentation of the DSC operator, the three-phase source current \( i_s = [i_{a,s}, i_{b,s}, i_{c,s}]^T \) is first transformed into a \( \alpha\beta \)-frame variable \( i_{\alpha\beta}(t) \) as follows:

\[
i_{\alpha\beta}(t) = \begin{bmatrix} i_{\alpha}(t) \\ i_{\beta}(t) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} \\ 0 & \frac{1}{2} \sqrt{3} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix}
\]  

where \( T_{\alpha\beta} \) is Clarke transformation matrix. When \( i_s \) is asymmetric and distorted, \( i_{\alpha\beta}(t) \) can be decomposed as a series harmonics \( \sum k_{\alpha\beta} b(t) \) where \( b \) is the harmonic order. The DSC operator distinguishes the targeted harmonic component from multitudinous harmonic components in the distorted current signal by the law that different harmonics rotate over different angles in the same duration [31–36]. According to references [32–33], the structure diagram of the generalised DSC operator can be given as in Figure 4 and the corresponding equation can be expressed as:

\[
DSC_{\alpha\beta}^m \left[ i_{\alpha\beta}(t) \right] = \frac{1}{2} \begin{bmatrix} i_{\alpha\beta}(t) + R(\theta_c) \cdot i_{\alpha\beta} \left( t - \frac{T}{m} \right) \\ 0 \end{bmatrix}
\]  

FIGURE 4 Structure diagram of the general delayed signal cancellation (DSC) operator

| Regulators | Parameters | Value |
|------------|------------|-------|
| VR         | \( k_{VP} \) | 0.1   |
|            | \( k_{V1} \) | 0.2   |
| CR         | \( k_{CP} \) | 0.03  |
|            | \( k_{CI} \) | 0.1   |
|            | \( \omega_c \) | 3.14 rad/s |
|            | \( k_{CR2} \) | 20    |
|            | \( k_{CR3} \) | 20    |
|            | \( k_{CR7} \) | 20    |
|            | \( k_{CR11} \) | 20   |
|            | \( k_{CR13} \) | 20   |
|            | \( k_{CR17} \) | 20   |
|            | \( k_{CR19} \) | 20   |
where $R(\theta)$, $T$, and $m$ are the rotation matrix, the fundamental period of source current and the delay factor, respectively, and $R(\theta)$ is

$$R(\theta) = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix}$$

(13)

where $\theta = \frac{2\pi b^*}{m}$ is the controllable rotation angle determined by $m$ and the targeted harmonic order $b^*$. By choosing parameters $m$ and $b^*$ suitably, a generalised DSC operator can be configured to retain the desired frequency component and eliminate or attenuate other frequency components as well. Furthermore, a specified harmonic can be eliminated by multiple DSC operators with different $m$ and $b^*$, and in turn, a given DSC operator under a pair of $m$ and $b^*$ can eliminate a series of harmonics. Therefore, it is possible to construct a CDSC filter with the minimum number of optimal DSC operators to extract FFPS component, $i_{sp,\alpha\beta}$, from distorted source current.

In this study, aiming at an APF working in the typical three-phase three-wire supply system with the rated frequency of 50 Hz and the asymmetrical harmonic source load, DSC1, DSC4, DSC8, DSC16 and DSC32 are selected and the overall CDSC filter can be constituted as shown in Figure 5. The amplitude-frequency characteristics of each DSC operator and overall CDSC filter are given in Figure 6, which shows obviously that the FFPS current can be extracted exactly whereas almost all other frequency components had been removed.

### 3.3 | Stability analysis of the improved PB scheme

According to Figure 3, the closed-loop transfer function of the source current controller can be expressed as

$$G_{CCT}(s) = \frac{G_{CR}(s) \cdot G_d(s) \cdot G_{PWM}(s) \cdot G_L(s)}{1 + G_{CR}(s) \cdot G_d(s) \cdot G_{PWM}(s) \cdot G_L(s)}$$

(14)

where $G_d(s) = \frac{1}{1 + 1.5 \cdot T_s \cdot s}$ is used to characterise the delay of sampling and filtering, and $T_s$ is the sampling period; $G_L(s) = \frac{1}{\frac{L_1 + L_2}{R} + s}$, in which $L_1 = L_2 + L_2$ and $R$ are the equivalent inductance and internal resistance of the output filter respectively.

Bode diagram of the $G_{CCT}(s)$ is plotted in Figure 7.

From Figure 3, the closed-loop transfer function of VCL can be expressed as

$$G_{VCL}(s) = \frac{G_d(s) \cdot G_{VR}(s) \cdot G_{CCT}(s) \cdot G_{dc}(s)}{1 + G_d(s) \cdot G_{VR}(s) \cdot G_{CCT}(s) \cdot G_{dc}(s)}$$

(15)

where $G_{dc}(s) = \frac{k_p}{s \cdot \tau_{C_{dc}}}$, in which $k_p$ is the equivalent gain between the APF current and the DC-link capacitor current.

Figure 8 shows the bode diagram of the $G_{VCL}(s)$ with the proposed control scheme. From Figure 8, it can be seen that $G_{VCL}(s)$ maintain unity gain at low frequency range up to 10 Hz and the designed current regulators do not cause the magnitude of $G_{VCL}(s)$ going higher than 0 dB.

Figure 9 shows the pole-zero map of the $G_{VCL}(s)$ with the proposed control scheme. From Figure 9, it can be seen that all poles of the voltage closed-loop transfer function $G_{VCL}(s)$
remain to the left of the imaginary axis, which means that the proposed control system is stable.

Besides, considering the influence of the feed-forward link on the system, the transfer function of DC-link voltage and load disturbance is obtained as

\[
G_N(s) = \frac{G_{dc}(s) \cdot (1 - G_{FF}(s) \cdot G_{CCT}(s))}{1 + G_{d}(s) \cdot G_{VR}(s) \cdot G_{CCT}(s) \cdot G_{dc}(s)}
\]  

(16)

where \( G_{FF}(s) = 1 + \frac{e^{-T_2 s^2}}{1 + \frac{e^{-T_4 s^2}}{1 + \frac{e^{-T_8 s^2}}{1 + \frac{e^{-T_{32} s^2}}}}}} \) is the equivalent transfer function of designed feed-forward link and the delay brought by the CDSC filter is about \( T \approx 0.97T \).

It can be seen intuitively from Figures 13 and 14 that the waveforms of \( i_{sa} \) had been close to a sinusoid after having been compensated by the APF with either the conventional or the improved PB scheme. The THD values of \( i_{sa} \) were reduced to [39–41]. The loads are composed of a resistive load, an inductive load and a three-phase diode rectifier with resistors \( R_1 \) (called case 1) or \( R_1 \) in parallel with \( R_2 \) (called case 2) in DC side. The supply voltage is generated by a 12 kVA programmable AC source supply (Chroma 61511). The simplified main circuit diagram and experimental platform appear in Figures 10 and 11. The detailed parameters are given in Table 3.

### 4 EXPERIMENTAL VERIFICATION

A series of simulations and experiments were carried out based on the three-phase APF depicted in Figure 1 and had similar results, so only experimental results are given here. The VSC consisted of three Infineon IGBT modules (FF150R12RT4) driven by the Concept 2SC0108Ts which received control signals from digital signal processor chip TMS320F28377, by which the algorithms of the two different schemes were implemented. The LCL output filter was designed according to [39–41]. The loads are composed of a resistive load, an inductive load and a three-phase diode rectifier with resistors \( R_1 \) (called case 1) or \( R_1 \) in parallel with \( R_2 \) (called case 2) in DC side. The supply voltage is generated by a 12 kVA programmable AC source supply (Chroma 61511). The simplified main circuit diagram and experimental platform appear in Figures 10 and 11. The detailed parameters are given in Table 3.

#### 4.1 The steady state performance

Figure 12 shows the steady state waveforms and harmonic spectra of phase A source current, \( i_{sa} \), before the APF put into operation. Obviously, the time domain waveforms of \( i_{sa} \) distorted seriously and THD values of \( i_{sa} \) were 23.89% (in case 1) and 16.03% (in case 2).

It can be seen intuitively from Figures 13 and 14 that the waveforms of \( i_{sa} \) had been close to a sinusoid after having been compensated by the APF with either the conventional or the improved PB scheme. The THD values of \( i_{sa} \) were reduced to
### TABLE 3 System parameter settings in the experiments

| Parameters                  | Value         |
|-----------------------------|---------------|
| Power supply Voltage $e_s$  | 50 V/50 Hz    |
| Line impedance             |               |
| Line inductance $L_s$       | 330 $\mu$H    |
| Line resistance $R_s$       | 0.5 ohms      |
| LCL LPF                    |               |
| Grid-side inductor $L_1$   | 0.13 $m$H     |
| VSC-side inductor $L_2$    | 0.82 $m$H     |
| Capacitor $C_{ac}$         | 12 $\mu$F     |
| APF                        |               |
| DC-link voltage $u_{dc}$    | 200 V         |
| Switching frequency $f_s$  | 12.8 kHz      |
| DC-link capacitor $C_{dc}$ | 2350 $\mu$F   |
| Rectifier loads            |               |
| DC-side resistor $R_1$     | 44 $\Omega$   |
| DC-side resistor $R_2$     | 44/10/5 $\Omega$ |
| AC-side inductor $L_3$     | 6 $m$H        |
| Linear loads               |               |
| Resistive loads $R_L$      | 150 $\Omega$  |
| Inductive loads $L_L$      | 0.115 H       |

#### FIGURE 12 Experimental waveforms and frequency spectrums of phase A source current without an APF

3.42% (in case 1) and 2.22% (in case 2) with the conventional PB scheme, and to 3.38% (in case 1) and 2.21% (in case 2) with the improved PB scheme, respectively. Thus, the steady state compensation performances of the two different schemes were almost identical and satisfying.

4.2 The DC-link voltage regulating performance

Figure 15 presents the experiment waveforms of DC-link voltage, phase A load current, $i_{dc}$ under the two different schemes. In Figure 15(a), with the conventional PB scheme, $u_{dc}$ dropped down to 180.5 V and went upward to 219.4 V, respectively, with the rectifier load shifting from case 1 to case 2 and back to case 1 again, and took about 2.2 s to restore to the set value of 200 V. The control effect of the improved PB scheme is shown in Figure 15(b). When the load changed from case 1 to case 2, $u_{dc}$ went down to 194.5 V at first and rebounded to 203.7 V, and then reverted to the set value. The whole transient process lasted about 0.42 s. Similarly, when the load got back to case 1 from case 2, $u_{dc}$ ranged from 200 V through 205 to 196.5 V, then recovered to 200 V again. The entire process lasted about 0.44 s. It is obvious that the improved PB scheme has obtained
MENG ET AL.

4.3 The compensation performance and the adaptability to the load fluctuation

Figure 16 displays the waveforms of $u_{dc}$, $i_s_a$, $i_{la_a}$, phase A filter current $i_{c_a}$ and frequency spectrum of $i_{s_a}$ under two different schemes. Figures 16(a) and (c) give the entire waveforms of the conventional PB scheme during the load shifting between case 1 and case 2, and the zoom-in waveforms from 1 s to 1.2 s after the load had switched, respectively, while Figures 16(b) and (d) give the corresponding waveforms of the improved PB scheme. It can be observed from the waveforms of $i_{c_a}$ and its frequency spectrums in Figures 16(c) and (d) that there were a large number of harmonic components superimposing on $i_{s_a}$ with the conventional PB scheme, but a good sine wave had been obtained by the improved PB scheme due to its shorter transient process.

Further, to compare the immunities to the load sudden change between the two schemes, the experiments had been redone with replacing value of $R_2$ with 5 ohms. As in Figure 17(a), the APF with the conventional PB scheme was not able to limit the DC-link voltage to a manageable range and quit running owing to overvoltage protection. But with the improved PB scheme, the APF controlled the DC-link voltage back to the set value effectively and maintained normal operations under the same conditions, as shown in Figure 17(b).

5 CONCLUSION

Existing PB scheme based APFs have the drawback of DC-link voltage fluctuation caused by sudden load change, which degrades their compensation performances, threatens their operation safety and limits their application scenarios. The reason for the DC-link voltage fluctuation is that the DC-capacitor buffered some of the active power while the load changed. This study proposed an improved PB scheme, in which a feedforward link had been added to prevent the active power from being buffered. The CDSC filter that had been selected and designed to draw out the FFPS active components from the source current, combined with the amplitude increment operator to form the feed-forward link. Simulations and experiments
are conducted to validate the proposed scheme and relevant designs. Confirmed by Figures 12–17, the proposed scheme has significantly weakened the DC-link voltage fluctuation and improved the adaptability to sudden load changes along with a certain extent improvement in the compensation performance. The scheme is not only easy to implement but also cost saving because it only needs to add the feed-forward correlation algorithm to the original algorithm without adding any hardware.

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