CALICE: status of a data acquisition system for the ILC calorimeters

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Abstract. A data acquisition system is described which will be used for the next generation of prototype calorimeters using particle flow algorithms for the International Linear Collider. The system could also be the basis for the final detector. The design is sufficiently generic such that it should have applications elsewhere, be they either ILC detectors or within high energy physics in general. The data acquisition system will be implemented using FPGAs and built using off-the-shelf components and networking hardware. The EUDET ECAL technical prototype will be used to demonstrate the feasibility of this approach. The design philosophy, the current status of the project and its aims are presented giving an overview of the effort.

1. Constraints on the Data Acquisition System

The concept of particle flow algorithms and the beam structure of the planned ILC accelerator put constraints on the data acquisition (DAQ) system which are described in the following.

Particle flow algorithms are a widely accepted approach to improve the energy resolution at the International Linear Collider (ILC). Particle flow uses the high segmentation of about 1 cm $\times$ 1 cm in the detection layer of a sampling calorimeter to track particles through the calorimeter. The segmentation results in about 24 million readout pads in the electromagnetic calorimeter (ECAL) of a planned ILC detector [1]. It is estimated that about 250 GB of raw data per bunch train need to be handled depending on the very front end electronics (VFE) and the detector type chosen for the final calorimeter. Because of the high number of readout channels it is necessary to minimise the cost of the electronics. This is achieved by using standard networking chipsets and protocols. Already at an early stage of the calorimeter prototypes the DAQ system has been designed for scalability. In the current detector plans the space for the electronics and cooling inside the calorimeters is very small. In the EUDET prototype the DAQ components are not yet minituarised to allow some flexibility for the test beams.

The ILC accelerator will generate bunch trains with a length of about 1 ms and a repetition rate of 200 ms resulting in an inter-train gap between bunch trains of about 199 ms which can be used for the readout of the calorimeters. It is vital that no data is lost through buffer overflows during the bunch train phase and that the data get time stamps for the event building which is done at a later stage.
2. Overview over the proposed Data Acquisition System

2.1. Detector Interface Board

Fig. 1 shows a schematic of a calorimeter module and its DAQ system. The detector signals are buffered and digitised by the Very Front End (VFE) ASICs situated on the detector slabs. The VFE ASICs depend on the detector used in the prototypes. The interface between the VFE and the DAQ system is provided by the detector interface (DIF) board which is located at the end of the calorimeter slabs. The DIF board consists of a customised part which translates the signals of the ASICS into more generic signals and a generic part of the DIF which passes the data on and sends configuration on to the VFE electronics. Thus providing a common interface to the DAQ components further away from the detector. The connections between the DIFs have been designed in order to give an additional level of redundancy as can be seen in Fig. 2. The DIF is connected via HDMI cabling to the rest of the DAQ system. HDMI [2] is a home entertainment system standard with small cabling and connectors which are commercially available, at low cost. They are rated at more than 300 Mb/sec for data.

2.2. Link Data Aggregator

In order to accumulate the data sent from the DIF a link data aggregator (LDA) collects the data from several DIFs and sends it further to the off detector receiver (ODR). The number of DIFs aggregated in the LDA depends on the detector type chosen in the detection layer. The optimal number of DIFs/LDA must take into account the number of available pins on the FPGA, the bandwidth per DIF and the cost effective maximum bandwidth of the optical link. The current LDA prototype can host up to eight links to the DIFs, but plans for a new

**Figure 1.** Integration of the DAQ components in the EUDET module
prototype with a higher number of DIF connections are already made. Physically the LDA has banks of HDMI connectors for connections to the DIFs and a small form-factor pluggable (SFP) connector for the optical link off-detector. The prototype version of the LDA is built on a commercial development board with a Xilinx Spartan3-200 FPGA and two purpose specific add-on boards: one providing the SFP and serialiser chipset for the optical link, and the second hosting eight working HDMI connectors with clock fan-out hardware.

2.3. Off Detector Receiver
The LDA is situated at the edge of the detector, the ODR however is located in the counting room connected to the on-detector DAQ system by an optical fibre. It sends control and configuration data to the LDA for distribution to the DIFs and finally sends the data off the detector to the event building. The ODR is realised as a PCI-Express card and can serve up to four LDAs per card, one PC can host up to two ODRs. For the proposed DAQ system currently a Xilinx Virtex 4 FPGA is used, thereby using a commercial FPGA board. At present, the data stream which will come from the detector in the EUDET test beam is simulated by an internal data generator in the firmware, or data received via an on-board ethernet interface.

The user interface to the ODR card contains two parts: a custom driver - mainly tasked with mapping card memory to the user space and providing direct memory access (DMA) support and a client program. The client retrieves data from the ODR card memory and stores it on the local disk. The client is a fully programmable multi-threaded application with separate threads for data transfer from the ODR to the host memory and IO threads for storing to the local disk. The performance of the prototype ODR has been investigated using the Ethernet interface to provide an input data stream which is coped to host memory and is currently higher than 500 MByte/sec without any disk writes as can be seen in Fig. 3. The number of DMAs has been optimised for this figure.

3. Clock and Control Handling
3.1. Clock and Control Board
For the event building a good clock is essential. It is understood that a machine clock will be used which will be fed into the ODRs and fanned out to the LDAs and DIFs. The requirements on the clock are a low jitter and a fixed latency between the machine clock and the clock in the DIFs. Commercial networking hardware is not suited for this task as it is most efficient when it can buffer data and provides no guarantees on delivery times. Similarly networking hardware built into modern FPGAs suffers from varying latency. Therefore a clock and control board has
been custom designed with links to eight ODRs. The clock and control module must interface with the machine and provide stand-alone signal and clock generation. It will also receive a busy signal from the very front end electronics. The HDMI cables configuration used for the DIF to LDA link will be reused here. Control data will be sent over the same HDMI type cabling.

3.2. Resets due to Single Event Upsets

Single event upsets (SEUs) can occur in the electronics if a particle (typically a neutron, proton or pion above a certain threshold energy which is about 20 MeV) traverses it. The traversing particle transfers energy to a nucleus in the sensitive volume which creates a large ionization along its short path. If the deposited energy in the sensitive volume is higher than the threshold energy the electronics changes its state, in other words an upset has been triggered which needs to be reset by the control data. A study has been made to estimate the frequency of resets needed and therefore to estimate the impact of SEUs on the control stream.

For this study which is described in more detail in [3] simulations using PYTHIA and MOKKA have been performed for physics events and beamstrahlung remnant events which occur frequently according to the TESLA TDR. WW, QCD, t\bar{t}, Bhabha, beamstrahlung pair production and $\gamma\gamma \rightarrow$ hadrons events were simulated. A spectrum of particles traversing the ECAL front-end electronics is shown in Fig. 4. The $\gamma\gamma \rightarrow$ hadrons machine background and QCD events dominate the spectrum. By comparing the particle spectrum with SEU cross sections of several FPGAs as found in the literature the SEU rate has been estimate to lie between 14 minutes to 12 hours for all of the FPGAs in the TESLA ECAL. This requires the FPGAs in the ECAL to be reset at a higher rate to mitigate these effects.

Figure 3. Data transfer rates of the off detector receiver depending on the data size.
4. DAQ Software
As framework of the DAQ and control software DOOCS [4] has been chosen. DOOCS provides a three layered modular framework. The lowest layer being hardware interfaces also called device servers, the middle layer provides an interface to a finite state machine, a naming service, a DAQ server and web service e.g. for alarm handling, the upper layer provides user interfaces to programs like ROOT, MATLAB or LabVIEW and DOOCS specific user interfaces. Several network protocols can be used like remote procedure calls, TINE and channel access.

The device server handles all properties of a particular device, e.g. an ODR, LDA, DIF or ASIC. These servers then create as many device instances also called locations as needed of its type. A client server is an independent program which receives that data and sends control messages to the servers. The system is distributed, because the device definition is done on the server side only and is transparent to the clients. Whenever a server is started, new device instances are created or new properties are added, these changes are immediately available on the network; there is no central database to hold the items. The names of the device server (IP-Addresses) for the clients are resolved by an Equipment Name Server (ENS). For the EUDET prototype an ENS naming convention has been chosen. The device servers however have not yet been implemented.

5. Conclusion and Outlook
The DAQ system for the EUDET detector will be a hierarchical DAQ system which minimises the area needed on the detector and uses commercial components to minimise the cost of the DAQ system. In order to make the development for the test system independent of the detector type tested a DIF board will make the readout generic. An LDA card will concentrate the data from the DIF and send it off to the ODR which is located off the detector in a control room. The task of the ODR is to store the data. At the time of writing each hardware component of the DAQ system exists and tests are ongoing. For the LDA the needed firmware still needs to be implemented. The component tests will be finished this autumn with the integration tests starting this winter. It is envisaged that the hardware interfaces of the DAQ software to each hardware components will be finished this autumn. This means that the hardware and software developments are synchronised. The goal is to have the whole DAQ system ready for the EUDET test beam in 2009.
6. References
[1] TESLA Technical Design Report, Part IV, A Detector for TESLA, T. Behnke et al., 2001.
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[3] V. Bartsch, et al., Nucl. Instr. and Meth. A (2008)
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