FPGA-Based Real-Time Simulation for Multiple Energy Storage Systems

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Abstract. Combining the renewable energy system, the Energy Storage (ES) station can maintain stable power transfer between renewable energy systems and power grid. This paper works on real-time simulation for multiple energy storage systems under different operating modes. Then taking a large number of ES converters and power grid into account, a modified electromagnetic transient program (EMTP) algorithm is proposed which is fit for the field-programmable gate array (FPGA)-based real-time simulation. By compressing the steps of the traditional EMTP algorithm, the simulation can be completed only by updating the history current source in each simulation cycle. In the meantime, the system is decoupled and multiple subsystems are simulated independently. Furthermore, to fully utilize the high parallelism of FPGA, we design and build a CPU-FPGA-based real-time simulation platform to implement the ES station. Using the simulation platform, we build a model of ES station and connect to the grid through an inverter. The whole system is tested in a single FPGA under different scenarios.

1. Introduction
As photovoltaic [1][2], wind power [3] and electric vehicles [4][5] are connected to the grid on a large scale, uncertainty and randomness can cause great security problems if they are not effectively suppressed and controlled [6]. Energy storage (ES) station plays a vital role in renewable energy access. First, ES station suppresses voltage fluctuations caused by the renewable energy system and improves the disturbance immunity of power grid [7][8]. Secondly, by adjusting the charging/discharging power of the ES station, it balances the electricity consumptions and renewable energy generation [9]. It is necessary to simulate and verify the electrical system and control system of the ES station before being applied in practice [10]. Thus, real-time simulation is of great significance to improve the efficiency of the ES station test [11]. It is valuable to select a suitable real-time simulation platform and develop a real-time simulation algorithm for ES station.

In recent years, the field programmable gate array (FPGA) has been widely utilized for electromagnetic transient real-time simulation studies [12][13]. However, the control system contains a lot of serial computation, which may slow down the real-time simulation if the whole system simulated in a single FPGA. Therefore, the electrical system is simulated in the FPGA and the control system is simulated in the CPU [14]. In this work, a CPU-FPGA architecture real-time simulation
platform is established for the ES station. The nodal analysis method is one of the most widely used methods in EMTP [15]. However, a large number of serial calculation steps limit its application in FPGA. To take full advantage of FPGA’s parallel computing resources and simulate the electrical system in sub-microsecond time-step, a modified EMTP algorithm is proposed for the ES station. By redesigning the EMTP algorithm, the simulation process is converted into three parallel subtasks which is suitable for FPGA implementation.

In this paper, the real-time simulation platform which is suitable for ES station is proposed, with the implementation method of the system. Besides, a modified EMTP algorithm is proposed to convert the EMTP algorithm to multiple parallel processes. Also, the modified EMTP algorithm enables parallel simulation of multiple ES converters. By using a two-layer parallelization approach, the computational advantages of FPGAs are fully utilized. The sections of the paper are arranged as follows. Section II gives the structure of the ES station and the real-time simulation platform. The modified EMTP algorithm which is suitable for ES station is proposed in Section III. Section IV and V are the simulation analysis and the conclusion.

2. The architecture of simulation system

2.1. Energy storage station

The ES station integrating five ES converters and one grid-connected inverter was selected as the case study and studied on the real-time simulation platform. The ES converter uses a double active bridge (DAB) topology, while the inverter uses a two-stage converter. In this paper, the grid-connected maintains the DC bus voltage, and the ES converter controls the battery charging and discharging power, as shown in Figure 1.

![Figure 1. Energy storage station](image)

Considering the operation of the charging station, the main parameters are shown in Table 1.

| Table 1. Energy storage station parameters |
|------------------------------------------|
| Parameter                        | Value | Unit |
|-----------------------------------|-------|------|
| AC power grid                    | 220   | V    |
| Filter inductor of rectifier     | 1     | mH   |
| Filter capacitor of rectifier    | 100   | μF   |
| Capacitor on DC bus              | 800   | μF   |
| Leakage inductance of transformer| 160   | μH   |
| Transformer ratio                | 2:1   |      |
| Output filter capacitor          | 800   | μF   |
| DC bus rated voltage             | 800   | V    |
### 2.2. Real-time simulation platform

The main architecture of the CPU-FPGA simulation platform is shown in Figure 2. PXIe-8135 as the master control board. It contains a quad-core Intel i7-3610QE processor, dual-channel DDR3, 1600MHz memory controller, all standard I/O, and integrated hard disk, connecting with Kintex-7 XC7K410T FPGA board and host PC. The control strategy is carried out in the CPU. The CPU receives the instantaneous circuit parameters from the FPGA and sends a modulation wave signal to the FPGA through the PXIe bus. The core operating frequency of the CPU is 2.3 GHz. The FPGA board is a slave board, which performs real-time simulation of the ES station electrical system and the generation of PWM switching signals under the instructions of the master board. The clock frequency of the FPGA board is set to 160MHz. 254200 look-up tables (LUT) and 508400 flip-flops (FF) constitute a configurable logic block (CLB), which can realize combinational logic and sequential logic. The FPGA contains 1540 digital signal processing (DSP) chips and 28620 block RAMs. It provides 25×18 multipliers and memory resources. It is mainly used for historical current update and circuit parameter calculation in matrix operations. Besides, the FPGA I/O interface can be connected to an oscilloscope to observe the simulation results.

![Figure 2. The structure of real-time simulation platform](image)

PXI Express plays a vital role in the communication between the CPU controller and the FPGA, increasing the available bandwidth to 8GB/s. It guarantees low-latency data exchange of control signal and electrical signal and ensures the real-time and accuracy of real-time simulation. When the time step achieves sub-microseconds, the real-time communication is more important. Otherwise, too much delay may cause system instability. The host-PC provides a human-machine interface (HMI) to sample CPU data, display control and simulation waveforms.

### 3. Real-time simulation algorithm

#### 3.1. The modified EMTP algorithm

The traditional EMTP algorithm involves complex serial calculations. In order to take full advantage of the parallelism of FPGA, the modified EMTP algorithm obtains parallel computing steps by redesigning simulation process that using the EMTP algorithm. Through this algorithm, the serial calculation is transferred to two parallel subtasks, which only contain simple matrix calculations and avoid the calculation of intermediate variables. The first subtask is to observe the node voltage and branch current in the simulation. The second subtask is to update the history current. The modified
EMTP algorithm greatly compresses the computation amount and steps. The full simulation process using the modified EMTP algorithm is shown in Figure 3.

**Figure 3.** The structure of the modified EMTP algorithm

First, all branches in the network are converted into Norton’s equivalent circuits through discretization. For voltage source or current source branches are equivalent to equivalent admittance and parallel injection current sources.

\[ I^n_h = I^n_s \]  \hspace{1cm} (1)

where \( I_h \) is the history current and \( I_s \) is the injection current.

Similarly, for inductance and capacitance, branches are equivalent to equivalent admittance and parallel history current source. We apply backward Euler method for numerical integration. For the inductance branch \( L \), we have

\[ I^n_{h+1} = I^n_h, \quad Y_b = dt/L \]  \hspace{1cm} (2)

For the capacitance branch \( C \), we have

\[ I^n_{h+1} = -Y_b V^n_h, \quad Y_b = C/dt \]  \hspace{1cm} (3)

where \( Y_b \) is the equivalent admittance of the branch.

**Figure 4.** The switch model

For the switch branch, we use the L/C model. The switch is equivalent to a small inductance \( L_s \) when it’s on, and equivalent to a small capacitance \( C_s \) when it’s OFF as shown in Figure 4. According to (1) and (2), we have

\[
\begin{align*}
I^n_{h+1} &= I^n_h, \quad Y_{sw} = dt/L, \quad \text{ON state} \\
I^n_{h+1} &= -Y_{sw} V^n_h, \quad Y_{sw} = C/dt, \quad \text{OFF state}
\end{align*}
\]  \hspace{1cm} (4)

To ensure that the node admittance matrix keeps constant during the simulation, we generally make the turn-on admittance and turn-off admittance equal.
After determining the parameters of each branch, we can calculate the node voltage $V_n$ according to the node injection current and the node admittance matrix

$$V_n^i = Y_n^i A^T I_h^b$$

(6)

where $I_h$ is the $N_b \times 1$ vector composed of injection current and history current, where $N_b$ is the number of branches in the circuit. $Y_n$ is the $N_n \times N_n$ nodal admittance matrix and $N_n$ is the number of nodes. $A$ is the correlation matrix. Then, the branch voltage vector $V_b$ can be expressed as

$$V_b^n = A V_n^n$$

(7)

By analyzing the relationship between branch voltage $V_b$ and current $I_b$, the following equation can be written:

$$I_b^n = Y_b V_b^n + I_b^n$$

(8)

From (2) - (4) we can conclude

$$I_b^{n+1} = a Y_b V_b^n + b I_b^n$$

(9)

Where $a$ and $b$ are the coefficients of the history current when using different numerical integration methods. Substituting $Y_b$, $V_b$, and $I_b$ into equation (9) to update the history current.

According to (1) and (6) - (9), we can summarize the entire algorithm process into three parallel subtasks.

Subtask 1: Node voltage calculation

$$V_n^n = Y_n^i A^T I_h^b = G_i I_h^b$$

(10)

Subtask 2: Branch current calculation

$$I_b^n = Y_b V_b^n + I_b^n = Y_b A Y_n^i A^T I_h^b + I_b^n = G_i I_h^b$$

(11)

Subtask 3: History current update

$$I_b^{n+1} = a Y_b V_b^n + b I_b^n = (a + b) G_i - a I_h^b = G_i I_h^b$$

(12)

Equation (10) - (12) reveals that the simulation only needs three parallel steps to complete. Compared with the traditional EMTP algorithm, the modified EMTP algorithm converts all serial steps into parallel steps. This algorithm is very friendly to FPGA hardware implementation, which improves simulation efficiency through parallel computing.

3.2. Implementation

CPU is more suitable for calculating complex control system operations and FPGA is more suitable for large scale matrices calculation. Based on the CPU-FPGA-based real-time simulation platform, the control strategy and circuit topology are simulated at different time steps. The interaction between the electrical system and control system as shown in Figure 5.

**Figure 5.** The interaction between the electrical system and control system
For the ES station, all the calculations of the circuit and control subsystems begin simultaneously. The control signal calculation on CPU usually takes more time than the circuit update on FPGA. The dynamics of the control system is slower than the electrical system. As a result, the control system calculated in the CPU with a 100us time-step, and the electrical system is calculated on FPGA with a 250ns time-step. The CPU transfer control signals to the FPGA every 100us. During this 100us, the FPGA calculates simultaneously with the control signals of the last step.

In the calculation of the electrical system on FPGA, matrix multiplications occupy the most resources and time. The most important thing we need to address is the problem of matrix multiplications. We use two methods to optimize matrix operations: The first is to divide the whole ES station into multiple subsystems to reduce the matrix dimensionality and the second is to use logical units to calculate the matrix containing only 1 and 0 to save multiplier resources. The use of the pipeline method on FPGA also improves resource utilization.

4. Simulation and analysis

4.1. Power control scenarios

Figure 6. The AC bus voltage and DC bus voltage

Figure 7. The input AC current
While the battery is being charged and discharged, the voltage can be kept constant or the power can be kept constant. The operating mode of the power plant can be determined according to the capacity of the battery and the actual needs. We have selected a battery charging scenario for simulation testing, and we can see that each charging system can independently provide the battery with different Charging Power. The AC bus voltage and DC bus voltage fluctuate slightly when the charging power varies, but the inverter makes the system stable. The AC bus voltage and DC bus voltage is shown in Figure 6. Similarly, the input AC current is shown in Figure 7. Figure 8 shows the charging power performance of each ES converter.

4.2. Fault ride-through scenarios
To test the ES station's fault ride-through capability, a single-phase earth fault of the AC bus occurs at 10.0s. At this point, the system changes from a steady state to a fault state. After a single-phase earth fault lasts 0.2s, the fault clears and the system still returns to steady state. During the transient process, both the AC and DC sides fluctuate considerably but still recover to steady-state values, indicating that the ES has fault ride-through capability. The transient waveforms of AC bus voltage and current, DC bus voltage and output voltage are presented in Figure 9 - Figure 11.

![Figure 8. The charging power of converters](image)

![Figure 9. The AC bus voltage and DC bus voltage during fault](image)
5. Conclusion
In this paper, a modified EMTP algorithm has been proposed to achieve the real-time simulation of an ES station in a CPU-FPGA-based platform. Through the redesign of the simulation process and matrix operation optimization, FPGA computing resources and parallel computing capabilities are fully utilized. According to the different characteristics of CPU and FPGA, a reasonable interaction mode is designed for the control system and the electrical system. The simulation results of the modified EMTP algorithm for ES station with multiple ES converters indicates that the ES station can operate under different modes. The implementation of ES station real-time simulation provides a great basis for the system design. In future work, the multi-FPGA simulation system will be developed for a larger power system.

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