EFFICIENT ARCHITECTURE-AWARE ACCELERATION OF BWA-MEM FOR MULTICORE SYSTEMS

A PREPRINT

Vasimuddin Md, Sanchit Misra,
Parallel Computing Lab,
Intel Corporation, Bangalore, India.
Email: {vasimuddin.md,sanchit.misra}@intel.com

Heng Li,
Department of Biostatistics and Computational Biology,
Dana-Farber Cancer Institute, Boston, USA.
Department of Biomedical Informatics,
Harvard Medical School, Boston, USA.
Email: hli@jimmy.harvard.edu

Srinivas Aluru,
School of Computational Science and Engineering,
Georgia Institute of Technology, Atlanta, USA.
Email: aluru@cc.gatech.edu

ABSTRACT

Innovations in Next-Generation Sequencing are enabling generation of DNA sequence data at ever faster rates and at very low cost. For example, the Illumina NovaSeq 6000 sequencer can generate 6 Terabases of data in less than two days, sequencing nearly 20 Billion short DNA fragments called reads at the low cost of $1000 per human genome. Large sequencing centers typically employ hundreds of such systems. Such high-throughput and low-cost generation of data underscores the need for commensurate acceleration in downstream computational analysis of the sequencing data. A fundamental step in downstream analysis is mapping of the reads to a long reference DNA sequence, such as a reference human genome. Sequence mapping is a compute-intensive step that accounts for more than 30% of the overall time of the GATK (Genome Analysis ToolKit) best practices workflow. BWA-MEM is one of the most widely used tools for sequence mapping and has tens of thousands of users.

In this work, we focus on accelerating BWA-MEM through an efficient architecture aware implementation, while maintaining identical output. The volume of data requires distributed computing and is usually processed on clusters or cloud deployments with multicore processors usually being the platform of choice. Since the application can be easily parallelized across multiple sockets (even across distributed memory systems) by simply distributing the reads equally, we focus on performance improvements on a single socket multicore processor. BWA-MEM run time is dominated by three kernels, collectively responsible for more than 85% of the overall compute time. We improved the performance of the three kernels by 1) using techniques to improve cache reuse, 2) simplifying the algorithms, 3) replacing many small memory allocations with a few large contiguous ones to improve hardware prefetching of data, 4) software prefetching of data, and 5) utilization of SIMD wherever applicable – and massive reorganization of the source code to enable these improvements. As a result, we achieved nearly 2×, 183×, and 8× speedups on the three kernels, respectively, resulting in up to 3.5× and 2.4× speedups on end-to-end compute time over the original BWA-MEM on single thread and single socket of Intel Xeon Skylake processor. To the best of our knowledge, this is the highest reported speedup over BWA-MEM (running on a single CPU) while using a single CPU or a single CPU-single GPGPU/FPGA combination.

Source-code: https://github.com/bwa-mem2/bwa-mem2

©2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes,
creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

1 Introduction

Innovations in Next-Generation Sequencing (NGS) have enabled generation of DNA sequence data at an enormous rate and very low cost. This is best exemplified by Illumina sequencers; a single Illumina NovaSeq 6000 can generate nearly 6 Terabases of data in a 44-hour run, sequencing nearly 20 billion short DNA fragments, called reads, of length 150 base-pairs each at the cost of only $1000 per human genome [1]. This has established short read sequencing using Illumina sequencers as the standard for modern genomics studies with large sequencing centers employing hundreds of such sequencers.

The widespread use of NGS has enabled several applications – sequencing of individual genomes, sequencing genomes of new species, sequencing RNA samples to gather digital gene expression data, sequencing metagenomic samples of communities of microbial organisms, and single cell sequencing. Each of these usually requires mapping reads to one or more reference sequences or genomes. Sequence mapping is a compute intensive step; for example, it accounts for more than 30% of the overall time of the GATK (Genome Analysis ToolKit) best practices workflow [2–4], one of the most prominent workflows for analyzing sequencing reads.

As the sequencers continue getting faster and cheaper at an exponential rate much faster than the Moore’s law, we need commensurate speedups in sequence mapping. BWA-MEM [5] is one of the most popular tools used for mapping short reads to reference sequences as it is able to achieve both speed and accuracy. The software already has tens of thousands of users. The volume of data necessitates the use of distributed memory systems and most of it is processed on clusters and cloud deployments with multicore processors usually being the platform of choice.

In this work, we focus on accelerating BWA-MEM on multicore systems using efficient architecture-aware implementation. Since performance on multiple sockets can be achieved by just distributing the reads equally and load imbalance is usually not an issue, our efforts are focused on single socket performance.

An important requirement is to maintain identical output. Many genomics studies can take years to complete. For these studies, it is critical that the output of the sequence mapping tool does not change over a long period of time. Thus, we maintain identical output while accelerating BWA-MEM to allow like-for-like replacement. This makes optimizing the tool extremely challenging. The compute time of BWA-MEM is dominated by three key kernels that collectively account for over 85% of the total compute time - (i) search for super maximal exact matches (SMEM) between reads and the reference sequence, (ii) suffix array lookup (SAL), and (iii) banded Smith Waterman (BSW) algorithm. There are several heuristics applied within the kernels and while connecting the kernels. The tool suffers from irregular memory accesses and irregular computation with too many branches and data dependencies making the use of SIMD extremely difficult. Attempts to make the computation or memory access more regular by modifying the algorithm usually result in change in output.

Given the complexity of the BWA-MEM algorithm, only a few attempts have been made to accelerate it [6–9]. Most of these approaches use FPGAs or GPGPUs to accelerate one of the key kernels of BWA-MEM and report less than $2 \times$ speedup over the end-to-end compute time. One of them [9] demonstrates a $2.6 \times$ performance gain on end-to-end compute time by accelerating two out of the three kernels using four FPGAs.

In this paper, we present end-to-end optimization of BWA-MEM targeting multicore systems. We demonstrate the benefits of our improvements using an Intel® Xeon® Skylake processor and an Intel® Xeon® E5 v3 processor, but our optimizations are generic and can provide performance gains on any of the modern multicore processors.

Our key contributions are as follows.

- We performed rigorous architecture-aware optimizations on the three kernels by 1) designing techniques to improve cache reuse, 2) simplifying the algorithms, 3) replacing many small fragmented memory allocations with a few large contiguous ones to improve hardware prefetching of data, 4) exploiting software prefetching of data, 5) utilizing SIMD wherever applicable, and 6) applying shared memory parallelism using OpenMP. We undertook a massive reorganization of the source code to enable these improvements.
- We achieved $2 \times$, $183 \times$ and $8 \times$ speedup, respectively, on SMEM, SAL and BSW kernels.
- Our optimizations achieve up to $3.5 \times$ and $2.4 \times$ speedups on end-to-end compute time over the original BWA-MEM on single thread and single socket, respectively, of Intel Xeon Skylake processor.

\footnote{Intel, Xeon and Intel Xeon Phi are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Other names and brands may be claimed as the property of others. ©Intel Corporation}
Since our output is identical to the original BWA-MEM, it can seamlessly replace the original.

We present detailed performance analysis of our implementation, and use the resulting insights to conduct architecture bottleneck analysis when using the Skylake processor for BWA-MEM.

To the best of our knowledge, this is the highest reported speedup over BWA-MEM while using a single CPU or a single CPU-single GPGPU/FPGA combination.

2 A Brief Overview of BWA-MEM

In what follows, we use capital letters $X$, $Y$, etc. to denote DNA sequences, modeled as strings over the alphabet $\Sigma = \{A,C,G,T\}$ representing the four possible nucleotides (also called bases). The bases within a sequence are denoted using small letters like $a$, $b$, $c$, etc. We use $|X|$ to represent the length of sequence $X$. Let $X[i]$ denote the base at position $i$, and $X[i,j]$ ($i \leq j$) denote the substring $X[i]X[i+1]X[i+2] \cdots X[j]$. The bases ‘A’ and ‘T’ are considered complements of each other and ‘C’ and ‘G’ are complements of each other. We denote the complement of a base $c$ as $\bar{c}$.

2.1 Short Read Sequence Mapping Problem

Let $Q$ be a short read and $R$ be a long reference sequence. The sequence mapping problem is to find the best matches of $Q$ in $R$. For short reads, typical lengths of $Q$ range from 50 to 250. $|R|$ can range anywhere from a few hundred thousand (for bacterial genome) to several billions (for plant genomes). An important special case is the human genome, at 3 billion base-pairs long.

Most popular sequence mapping tools, including BWA-MEM, use the seed and extend method. In the seeding phase, matches for short substrings of the reads (called seeds) are found in the reference sequence while allowing for zero or very small number of differences in the match. This gives the potential locations where the entire read can match. In the extension phase, the seed matches are extended on both sides to cover the entire query, typically using a dynamic programming based algorithm, and the best matches are reported. BWA-MEM uses an FM-index of the reference sequence to perform seeding.

2.2 FM-index

The FM-index of a reference sequence is based on its Burrows-Wheeler Transform (BWT) and suffix array. Figure 1 shows how to construct the BWT, suffix array and FM-index of an example sequence $R$. First, $R$ is appended with the character $\$ \in \Sigma$ which is lexicographically smaller than all characters in $\Sigma$. Subsequently, all the rotations of $R$ are obtained (Rotations(R)). Lexicographically sorting the rotations gives the BW matrix. The BWT ($B$) is the last column of this matrix. The suffix array ($S$) stores the original positions in $R$ of the first bases of these rotations, equivalent to the sorted order of the suffixes of $R$. All the exact matches of a query are prefixes of the rotations in the BW-matrix. These matches are located in contiguous rows of the BW-matrix since the rotations are lexicographically sorted. Therefore, all the matches of a query can be represented as a range of rows of the BW-matrix. This range is called the SA interval of the query. For example, in Figure 1 matches of sequence “AC” correspond to the SA interval $[1, 2]$.

To facilitate fast search of BWT, FM-index is used [11]. It consists of $D$ and $O$ data structures. $D[x]$ is the number of bases in $R[0, |R| - 1]$ (excluding $\$) that are lexicographically smaller than $x \in \Sigma$, and $O[x, i]$ is the number of occurrences of $x$ in $B[0, i]$.

2.3 BWA-MEM algorithm

The BWA-MEM algorithm consists of the following steps.

SMEM: Perform seeding by searching for super maximal exact matches (SMEM) between the read and the reference sequence. Formally, maximal exact matches (MEMs) are exact matches between substrings of two sequences that cannot be further extended in either direction. An SMEM is a MEM that is not contained in any other MEMs on the query sequence [12]. BWA-MEM uses FM-index to search for SMEMs and outputs SA intervals of the SMEMs.

SAL: Suffix array lookup is performed to get the coordinates in the reference sequence from the SA intervals.

CHAIN: BWA-MEM chains the seeds that are collinear and close to each other. The chains thus formed are used to filter seeds for alignment.
**BSW:** The seeds are extended using dynamic programming (DP) based banded Smith-Waterman (BSW) alignment algorithm that computes only a diagonal band of the DP matrix. The diagonal band may shrink as the computation moves from the top row to the bottom row.

**SAM-FORM:** The algorithm concludes by formatting the alignment output in the SAM format.

### 2.4 Break up of computation time spent

To identify compute hotspots for acceleration, we performed rigorous run-time profiling of BWA-MEM (version 0.7.25) by hand instrumenting the source code with trackers. Table 1 reports percentage of the run-time spent in various steps of BWA-MEM. Clearly, SMEM, SAL and BSW are the most time consuming steps accounting for 86.5% and 85.7% of the total run-time of BWA-MEM, on D1 and D4 datasets, respectively. Therefore, we select them as targets for acceleration.

![Figure 1: FM-index (S, B, D, O) and BW-matrix for reference sequence R ← ATACGAC$. $](image)

The lexicographical ordering $[^{10}]$.

Table 1: Single thread run-time profiling of BWA-MEM workflow on D1 and D4 datasets (Table 3). We performed the profiling using default parameters and single-end reads.

| Stage         | Compute Blocks/Datasets | D1       | D4       |
|---------------|-------------------------|----------|----------|
| 1             | SMEM                    | 21.5%    | 44.4%    |
|               | SAL                     | 18%      | 15.5%    |
|               | CHAIN                   | 6%       | 5.9%     |
| 2             | BSW Pre-processing      | 4.7%     | 4.9%     |
|               | BSW                     | 47.2%    | 26.4%    |
| 3             | SAM-FORM                | 2.5%     | 2.9%     |
|               | Total run-time          | 292.73   | 182.79   |

[^10]: lexicographical ordering
2.5 Potential for improvement of the key kernels

In this section, we analyze the performance characteristics of the three kernels of BWA-MEM to identify target areas for performance improvement. To do so, we extracted the source code corresponding to each kernel from BWA-MEM and created a benchmark for each kernel. To prepare input datasets for the benchmarks, we executed BWA-MEM using read datasets and intercepted inputs to each of the kernels. The benchmarks produce the exact same output as the corresponding kernels in the original BWA-MEM.

2.5.1 SMEM

As shown in Section 6.2.1, Table 4, the SMEM kernel executes nearly 17 Billion instructions for 60,000 reads; that is; nearly 285 thousand instructions per read. The main reason for this is that BWA-MEM uses a compressed version of FM-index. Due to excessive compression, it requires a large number of instructions to compute the SA interval. Moreover, the kernel suffers from high LLC miss rate resulting in a significantly high average memory latency (24).

2.5.2 SAL

SAL kernel just retrieves the coordinate of reference sequence from the SA interval. What should have been a simple array lookup requires nearly 5000 instructions per lookup due to the use of compressed suffix array.

2.5.3 BSW

Due to the irregular nature of the BSW algorithm with significant branching and short loops, it uses a scalar implementation. As we explain in Section 5.1, BSW is a compute bound kernel. So, while memory access is not an issue, BSW implementation of BWA-MEM is instruction bound, due to the scalar implementation, resulting in lower performance.

3 Modifications Applied to Entire Code

3.1 Reorganization of the Workflow

Original BWA-MEM processes a chunk of reads at a time. Figure 2 shows how we transform the workflow of processing one chunk. For each read in a chunk, the original implementation processes it through all the steps until BSW before moving on to the next read. It maintains the BSW output for the reads until the entire chunk is processed. The BSW output of each read is then converted to SAM format. Multithreading is done using pthreads by dynamically
is discussed in the next Section. Algorithm 4 returns all the SMEMs passing through position \( i \). The software prefetching, introduced by us, Algorithms 2, 3 and 4 provide the details of SMEM search algorithm as given in [12]. The dots signify details of the algorithm that are omitted as they are not relevant to this discussion. The implementation of FM-index in BW A-MEM differs from the description in Section 2.2 in two ways. First, since same buffer is used repeatedly across batches, it also improves cache reuse. Contiguous memory allocation provides benefits of hardware prefetching, reducing the memory latency. Moreover, does not provide hardware prefetcher with a long predictable pattern of memory access, and does not allow cache reuse. Instead, we allocate all the required memory once in large contiguous blocks and reuse it across the batches. The BW A-MEM implementation allocates and de-allocates small blocks of memory frequently, which is expensive, since we use 2-bit representation using \( \{0, 1, 2, 3\} \) for \{A,C,G,T\}. The count of base \( c \) in the first \( y \) positions of \( bwt \) (line 4) is obtained by using bitwise operations. 

3.2 Improving Inefficient Memory Allocation

The BWA-MEM implementation allocates and de-allocates small blocks of memory frequently, which is expensive, does not provide hardware prefetcher with a long predictable pattern of memory access, and does not allow cache reuse. Instead, we allocate all the required memory once in large contiguous blocks and reuse it across the batches. Contiguous memory allocation provides benefits of hardware prefetching, reducing the memory latency. Moreover, since same buffer is used repeatedly across batches, it also improves cache reuse.

4 Optimizations Applied to SMEM and SAL

4.1 FM-Index Structure

The implementation of FM-index in BW A-MEM differs from the description in Section 2.2 in two ways. First, SMEM algorithm requires the FM-index of the sequence formed by concatenating the reference sequence with its reverse complement. Second, in order to reduce the memory footprint, the FM-index is compressed by dividing \( O \) into buckets of size \( \eta \). The compressed data structure \( O_c \) has only \( |R|/\eta \) entries. In each entry \( i \), two items are stored – 1) count: the count values of the bases up to bucket \( i \); thus, for each base \( c \), \( O_c[i]\).count\( (c) \) holds the counts \( O[c, i \times \eta] \), and 2) \( bwt \): the substring of BWT, \( B[i \times \eta, (i + 1) \times \eta - 1] \). The \( O \) values of any position can be computed using the \( O_c\), \( count \) and \( bwt \) (Algorithm 4). A power-of-2 number is picked for the value of \( \eta \) to replace the expensive division and modulo operations (lines 1 and 2) with right-shift and bitwise AND operations. Base \( c \) and \( bwt \) use 2-bit representation using \( \{0, 1, 2, 3\} \) for \{A,C,G,T\}. The count of base \( c \) in the first \( y \) positions of \( bwt \) (line 4) is obtained by using bitwise operations.

4.2 SMEM Search Algorithm

Algorithms 2, 3 and 4 provide the details of SMEM search algorithm as given in [12]. The dots signify details of the algorithm that are omitted as they are not relevant to this discussion. The software prefetching, introduced by us, is discussed in the next Section. Algorithm 4 returns all the SMEMs passing through position \( i_0 \) in \( X \). It starts at position \( i_0 \) and finds all the extensions in the forward direction that have matches. For all matches, it maintains the bi-interval, \((k, l, s)\), where - (i) \( k \) is the starting position of the SA interval of the matching substring of \( X \), (ii) \( l \) is
Algorithm 3 Forward_Ext((k, l, s), b)
Input: Bi-interval (k, l, s) of DNA string X and a base b
Output: Bi-interval of string Xb
1: \((l', k', s') \leftarrow \text{Backward_Ext}\((l, k, s), \bar{b}\)\)
return \((k', l', s')\)

Algorithm 4 SMEM(X, i₀)
Input: String X and start position \(i₀\)
Output: Set of bi-intervals of SMEMs overlapping position \(i₀\) in X
1: Initialize \(\text{Curr}, \text{Prev}\) and \(\text{Match}\) as empty arrays
2: \((k, l, s) \leftarrow (D([X[i₀]], D[X[i₀]], D(X[i₀] + 1) - D[X[i₀]])\)
3: for \(i \leftarrow i₀ + 1\) to \(|X|\) do
4: \(
\end{verbatim}

While the compression of FM-index reduces memory footprint, there is also an additional benefit. More accesses fall into the same \(O_c\) entry, improving data locality. In particular, as the matching string gets longer, the corresponding SA interval gets shorter and the likelihood of both \(k\) and \(k + s\) entries falling in the same cache line increases. With compressed FM-index, this should happen more frequently. The trade off is the increase in runtime for processing a base from \(O(1)\) to \(O(h)\).
4.3 Applying Software Prefetching to SMEM Kernel

Given the irregular memory access to \( O_c \), hardware prefetching will be ineffective. However, note that each access to \( O_c \) results in new values of \((k,l,s)\) that, if a match, decides the memory locations of a later access to \( O_c \). We can prefetch this location using software prefetching. Therefore, whenever new values of \((k,l,s)\) are computed that are likely to be used in the future to access \( O_c \), we software prefetch the corresponding locations of \( O_c \). During forward extension, if a new match \(((k,l,s))\) is found, it is either used in the next forward extension or appended to \( \text{Curr} \) which is used for a future backward extension. Therefore, we prefetch the corresponding locations of \( O_c \). Similarly, during backward extension, any new match \(((k,l,s))\) that is added to \( \text{Curr} \) is used for a future backward extension and, thus, we prefetch the corresponding locations of \( O_c \). However, software prefetching will only be useful if we can hide the latency of prefetching by computation. When a match found during forward extension is used for the next forward extension, or when the number of matches in \( \text{Prev} \) are small during backward extension, there may not be sufficient compute to hide memory latency. Since backward extension stage dominates the run time and \( \text{Prev} \) is sufficiently large frequently enough, software prefetching is quite useful. But it can not alleviate memory latency completely.

In order to get sufficiently large compute to hide the memory latency for every \( O_c \) access, we also tried processing multiple queries simultaneously in a round robin fashion performing one call to backward extension (or forward extension) per query every time and software prefetching according to the new match produced. However, given the intricacy of the algorithm and number of different branches possible, this approach resulted in a much larger number of instructions. The additional advantage of alleviating memory latency completely could not overcome the disadvantage of extra instructions.

4.4 Choosing Compression Factor

For our implementation, we choose the value of \( \eta \) to be 32 due to the following reasons. It is better to ensure that the size of one entry of \( O_c \) is less than that of one cache line. Otherwise, we will need to prefetch multiple cache lines per \( O_c \) access that can cause more data to be read from memory resulting in higher memory bandwidth requirement.

Each count needs 4 bytes (unsigned integer). Thus, in a \( O_c \) entry, 16 bytes are consumed to store the count values. That leaves a maximum of 48 bytes for the BWT substring. We use power-of-2 value for \( \eta \) to prevent expensive division and modulo operations. Thus, we can only use 32 bytes for the BWT substring. BWA-MEM uses the value of \( \eta \) as 128 and uses 2-bits to represent each base in the BWT string, thus consuming 32 bytes for the BWT string. However, extracting the count of a particular base from a BWT string of length 128 requires a large number of instructions. Moreover, 2-bit representation requires significant bit manipulation making it expensive. Therefore, we opt for a one byte representation of bases to enable partial vectorization of the computation of occurrences, thus choosing the value of \( \eta \) as 32. We perform a byte level compare using AVX2 to get a 32-bit mask containing 1 for match and 0 for mismatch. Consequently, we use a 32-bit popcnt instruction on the mask to get the count. We store each entry of \( O_c \) in a cache aligned location for effective prefetching by adding padding of 16 bytes to use a full cache line per entry.

4.5 Improvements to Suffix Array Lookup

Given a position \( i \) in the suffix array, \( S \), SAL returns the corresponding coordinate in reference sequence, \( j \), as shown in Equation 1.

\[
j = S[i]
\]

Similar to FM-index, BWA-MEM stores a compressed version of \( S \) with compression factor of 128. It obtains the value of \( S[i] \) through an intricate algorithm requiring access to multiple locations in the compressed \( S \) and FM-index. As a result, it requires nearly 5000 instructions on an average for each \( S[i] \) and a large number of memory accesses.

There is sufficient memory available to store the suffix array for most reference sequence sizes. For example, for entire human genome, we need about 48 GB of memory. Therefore, we use the uncompressed SA and use the expression in Equation 1 to get the coordinate of reference sequence.

5 Optimizations Applied to BSW

5.1 Banded Smith Waterman Algorithm Used in BWA-MEM

The BSW algorithm used in BWA-MEM is derived from the Smith Waterman (SW) algorithm, which is a dynamic programming (DP) based sequence alignment algorithm. Given a pair of DNA sequences \( X \) and \( Y \), both SW and
BSW compute the cells of a DP matrix $H$ of size $|X| \times |Y|$ in a row-wise manner. Here, the value $H[i, j]$ at each cell represents the alignment score between sub-sequences $X[0, i−1]$ and $Y[0, j−1]$. The key difference in the computation pattern is that, while SW computes all the cells of the DP matrix, (a) BSW restricts the cell computations to within a certain band size ($\lambda$) around the main diagonal, (b) BSW aborts the matrix computations, if all the scores in a row are zero or the best score of the current row drops by a certain threshold from best score so far, and (c) after computing a row, BSW adjusts the value of $\lambda$ based on number of cells with zero value from both ends. The top matrix of Figure[3] illustrates the full matrix and a diagonal band.

In BSW, computation of a cell $(i, j)$ of $H$ uses the following recursion.

$$
H[i, j] = \max\{H[i−1, j−1] + S(X[i], Y[j]), E[i, j], F[i, j]\}
$$

$$
E[i + 1, j] = \max\{H[i, j] - g_o, E[i, j] - g_e, 0\}
$$

$$
F[i, j + 1] = \max\{H[i, j] - g_o, F[i, j] - g_e, 0\}
$$

(2)

Where, $g_o$ and $g_e$ are gap open and extension penalties. $S(a, b) = m$ (match score), if $a = b$, else $S(a, b) = m'$ (mismatch score). For $1 \leq i \leq |X|$, $1 \leq j \leq |Y|$, the matrices are initialized as,

$$
H[i, 0] = \max\{0, H[0, 0] - (g_o + g_e, i)\},
$$

$$
H[0, j] = \max\{0, H[0, 0] - (g_o + g_e, j)\},
$$

$$
E[i, 1] = F[1, j] = 0
$$

(3)

Since BSW extends a seed, the initial matrix score $H[0, 0]$ is the match score of the seed. Given the computation of a cell is only dependent on the three neighbors, BSW in BWA-MEM only maintains one row each of $E$, $F$, and $H$. Smaller sequence sizes ensure that these arrays are present in caches and only the sequence pairs need to be fetched from memory, making BSW a compute bound problem.

### 5.2 Vectorization approaches and challenges

Given that BSW is compute bound, we chose to vectorize it using SIMD parallelism. Vectorization of standard SW has been studied extensively. There are two popular approaches: intra-task and inter-task. We see the following challenges in application of these approaches to BSW.

#### 5.2.1 Intra-task

Intra-task approach vectorizes the computation of SW of one pair. It either leverages the independence between anti-diagonal cells of the matrix to vectorize across them or uses striped SIMD approach. However, this kind of approach is unwieldy for BSW. Short sequences, computation only within the band, and potential reduction in the band size due to band adjustment, restrict the available parallelism for vectorization.

#### 5.2.2 Inter-task

In inter-task approach, each vector lane computes the matrix for different sequence pairs. The irregularity of matrix sizes, number of cells computed, and the positions within matrices of cells computed across matrices, makes extracting performance using inter-task approach difficult.

Moreover, in BWA-MEM, whether a seed is extended using BSW or not depends on the previously extended seeds of a read. Such dependency restricts the parallelism across seeds of a read.

Due to availability of better parallelism, we utilize inter-task vectorization for accelerating BSW (Figure[3]).

### 5.3 Inter-Task Vectorization

Our approach for inter-task vectorization is illustrated in Figure[3] and is based on our previous work [10]. Let $W$ be the SIMD width. We process $W$ sequence pairs at a time. For each cell $(i, j)$ that is computed, each vector lane computes the corresponding cell $(i, j)$ for all matrices. Therefore, even if one of the sequence pairs requires a particular matrix cell to be computed, the corresponding matrix cell is computed for all the sequence pairs leading to wasteful cell computations.
Figure 3: Inter-task vectorization of BSW over a batch of sequence pairs. Dark cells represent the banding, grey cells represent the computed cells in the matrix, and green cell represents the cell $H_{ij}$ being computed.

5.3.1 Sorting

While any aborted sequence pair can be replaced with a new one to avoid idle vector lanes, the overhead of the operation supersedes its benefits. Wasteful cell computations due to variations in sequence lengths can be better curbed by ensuring uniformity in sequence lengths. We use radix sort to sort the tasks by their respective sequence lengths, and then group together tasks with the same or close sequence lengths to ensure uniformity of tasks filling vector lanes.

5.3.2 Increasing parallelism

Given the dependency between seeds, the parallelism is only available across reads. However, the count of seeds per read can vary a lot leading to imbalance of computation across reads. A dynamic allocation of reads to vector lanes can potentially balance computation across vector lanes. However, given the imbalance in number of computed seeds across reads, it requires a large number of reads in a batch to succeed. Large batches are not possible due to memory constraints as we have to maintain the metadata corresponding to each read between steps of the BWA-MEM algorithm. Therefore, we manage the dependency between the seeds by first extending all the seeds of a read, and then post process them to filter out the ones that should not have been extended.

5.3.3 AoS to SoA conversion of sequence pairs

We convert the input sequences from AoS to SoA format to allow reading of corresponding bases from sequence pairs using vector load operation instead of a gather operation.

5.4 Overview of operations

For a given row, we do the following computations. (a) To perform cell computations within a given band, we utilize instructions such as cmp, blend, max, mov, add, and sub. Similar instructions are used to identify the best score and its position. (b) To find the global score, at each cell in a row, we check whether the end of query is reached for all the pairs using cmp instruction and update the global score and its position using cmp and blend instructions. (c) After the row computations, the cell range (for next row) is adjusted again based on the number of empty cells from both ends of the row. From both ends of the row, with one cell at a time, we use cmp and blend vector instructions to check for empty cells and update the range. (d) Moreover, we use mask and cmp instructions for maintaining the correct values for aborted sequence pairs.

5.4.1 Precision

Smaller integer-widths provide more vector lanes. Since matrix scores are proportional to sequence lengths, it is possible to use different integer-widths for matrix computation depending on sequence lengths. In BSW optimization, we use 8-bit or 16-bit implementations depending on the sequence length.
Table 2: System configuration

|                           | Intel® Xeon® Platinum 8180 Processor (SKX) | Intel® Xeon® E5-2699 v3 Processor (HSW) |
|---------------------------|-------------------------------------------|------------------------------------------|
| Sockets × Cores × Threads | 2 × 28 × 2                                 | 2 × 18 × 2                                |
| AVX register width (bits) | 512, 256, 128                              | 256, 128                                  |
| Vector Processing Units (VPU) | 2/Core                                    | 2/Core                                    |
| Base Clock Frequency (GHz) | 2.5                                        | 2.3                                       |
| L1D/L2 Cache (KB)         | 32/1024                                    | 32/256                                    |
| L3 Cache (MB) / Socket    | 38.5                                       | 45                                        |
| DRAM (GB) / Socket        | 96                                         | 64                                        |
| Bandwidth (GB/s) / Socket | 114                                        | 68                                        |
| Compiler Version          | ICC v. 17.0.2                              | ICC v. 17.0.2                             |

6 Results

6.1 Experimental Setup

6.1.1 System Configuration

While our implementation achieves best performance by running on latest processors with AVX512 support from heavy use of AVX512 instructions, we also support alternate AVX2-only and scalar-only executions for older generation multicore processors. To confirm the wide applicability of our improvements, we evaluated our implementations on two generations of processors – the latest Intel Xeon Scalable family of processors (Skylake) and Intel E5 v3 family (Haswell). Our specific Skylake and Haswell processors are detailed in Table 2 and referred to as SKX and HSW, respectively, from here on. Each AVX512 VPU can process multiple 8-bit and 16-bit integers thus capable of SIMD widths of 64 and 32, respectively; similarly, each AVX2 VPU can process multiple 8-bit and 16-bit integers thus capable of SIMD widths of 32 and 16, respectively. We used Intel® VTune® Amplifier 2018 for performance analysis by measuring hardware performance counters.

We perform all our experiments on a single sockets of SKX (28 cores) and HSW (18 cores) and use numactl utility to force all memory allocations to one socket. For multi-threaded runs, we run 2 threads per core to get the benefit of hyper threads. Since optimizing file IO is beyond the scope of this paper, we do not include file IO time in any of our results.

6.1.2 Datasets

To demonstrate the performance of our improvements, we make use of the following real datasets. We use the first half of the human genome (version Hg38), containing nearly 1.5 billion nucleotides, as the reference sequence for all our experiments. We use five different read datasets covering all prominent short read lengths (Table 3) to demonstrate the versatility of our implementation. We received the read datasets D1 and D2 directly from the Broad Institute to evaluate the performance of our implementation.

6.1.3 Correctness

For each experiment, we verified that our output is exactly identical to that of original BWA-MEM.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to www.intel.com/benchmarks.

Benchmark results were obtained prior to implementation of recent software patches and firmware updates intended to address exploits referred to as “Spectre” and “Meltdown”. Implementation of these updates may make these results inapplicable to your device or system.
Table 3: Real read datasets for application performance evaluation.

| Dataset | #Reads   | Read Length | Dataset Source      |
|---------|----------|-------------|---------------------|
| D1      | $5 \times 10^5$ | 151         | Broad Institute     |
| D2      | $5 \times 10^5$ | 151         | Broad Institute     |
| D3      | $1.25 \times 10^6$ | 76          | NCBI SRA: SRX020470 |
| D4      | $1.25 \times 10^6$ | 101         | NCBI SRA: SRX207170 |
| D5      | $1.25 \times 10^6$ | 101         | NCBI SRA: SRX206890 |

Table 4: Evaluation of SMEM kernel on a single thread of SKX using performance counters. Read dataset: 60,000 reads from D2.

| Performance Counters       | Original          | Optimized minus S/W prefetching | Optimized |
|----------------------------|-------------------|---------------------------------|-----------|
| # Instructions ($\times 10^6$) | 17,117            | 7,880                           | 8,160     |
| # Loads ($\times 10^6$)     | 4,429             | 2,200                           | 2,115     |
| # Stores ($\times 10^6$)    | 1,696             | 1,415                           | 1,393     |
| # LLC Misses ($\times 10^6$) | 23.9              | 29.7                            | 9.5       |
| Average latency (cycles)   | 24                | 33                              | 18        |
| # Cycles consumed ($\times 10^6$) | 10,496          | 6,986                           | 5,238     |
| Time                       | 4.20s             | 2.79s                           | 2.10s     |

6.2 Performance Evaluation of Key Kernels On a Single Thread

In this section, we evaluate the benefits of our improvements on the individual key kernels using real datasets on SKX. We extracted the kernels from both the implementations so that we are comparing only the kernels and nothing else.

6.2.1 SMEM search using FM-index

Table 3 evaluates our improvements to the SMEM kernel. Our modifications in the design to use the value of bucket size $\eta$ as 32 and vectorization to reduce the number of instructions has resulted in a greater than $2 \times$ reduction in the total number of instructions and the number of load instructions. However, lower value of $\eta$ results in less values of $k$ and $k+s$ falling into the same bucket, thus resulting in lower cache reuse. This is shown in the increase in the number of LLC misses and average latency of memory accesses between “Original” and “Optimized minus S/W prefetching” implementations. The use of software prefetching dramatically reduces the number of LLC misses (by nearly $3 \times$) and average latency of memory accesses at the cost of slightly higher instruction count. The change in performance counters is clearly reflected in the time consumed. Overall, our improvements achieved $2 \times$ performance gain over the original.

6.2.2 Suffix Array Lookup (SAL)

Table 3 shows the benefit of simplifying the SAL kernel. There is a dramatic reduction in the number of instructions per SA offset (nearly $200 \times$). Therefore, despite the increase in number of LLC misses per load, and thereby average memory latency, we see a speedup of nearly $183 \times$. There is further scope of performance improvement by using software pre-fetching. However, for our optimized implementation the time consumed in this kernel is negligible compared to the full application run time. Therefore, there isn’t much benefit in pursuing it.

6.2.3 Banded Smith-Waterman

Table 5 shows the performance benefit of our vectorized implementations at 8-bit and 16-bit precisions with or without sorting. For this experiment, we only used the sequence pairs for which 8-bit precision was sufficient. The results show clear benefit of sorting which provides $1.5 \times$ to $1.7 \times$ performance boost by increasing the chances of pairs that are processed simultaneously using SIMD parallelism having similar lengths. Overall, our 8-bit and 16-bit implementations achieve nearly $11.6 \times$ and $6.7 \times$ speedup, respectively, over the original implementation.

Table 6 uses hardware performance counters to explain the speedup. BSW is a compute-intensive task. Consequently, any reduction in number of instructions executed would result in reduction in execution time. Vectorization led to reduction in the number of instructions executed by $13.85 \times$ (for 8-bit implementation) over the original implementation.
Table 5: Evaluation of SAL kernel on a single thread of SKX using performance counters. We prepared the input data for this by running the full application using real data and extracting the input to this stage. Read dataset: 600,000 reads from D2.

| Performance Counters         | Original | Optimized |
|------------------------------|----------|-----------|
| # SA offsets ($\times 10^6$) | 41.05    |           |
| # Instructions ($\times 10^6$) | 213,065  | 1,058     |
| # Loads ($\times 10^6$)      | 23,617   | 241       |
| # Stores ($\times 10^6$)     | 5,459    | 156       |
| # Inst. per SA offset        | 5,190.7  | 25.8      |
| # LLC Misses ($\times 10^6$) | 452.3    | 5.0       |
| Average latency (cycles)     | 26       | 69        |
| # Cycles consumed ($\times 10^6$) | 161,170  | 880      |
| Time                         | 64.47s   | 0.35s     |

Table 6: Run-time of optimized (with AVX512) and original BSW benchmarks on a single thread of SKX for 48 million sequence pairs obtained by running the full application using real data and intercepting the input to BSW stage. Read dataset used: D3.

| BSW Benchmarks | Original | 16-bit w/o sort | 16-bit w/ sort | 8-bit w/o sort | 8-bit w/ sort |
|----------------|----------|-----------------|----------------|----------------|---------------|
| Time (sec)     | 283      | 65.36           | 44.46          | 42.09          | 24.46         |

Table 7: Evaluation of optimized 8-bit (with AVX512) and original implementations of BSW benchmark on a single thread of SKX using hardware performance counters.

| Performance Counters | Original | Optimized 8-bit |
|----------------------|----------|-----------------|
| # Instructions       | $1,385 \times 10^9$ | $100 \times 10^9$ |
| # Clock cycles       | $440 \times 10^9$   | $46 \times 10^9$   |
| IPC                  | 3.14      | 2.17            |

Table 8: Breakup to run time of optimized 8-bit BSW (with AVX512) on a single thread of SKX.

| Components           | Time (%) |
|----------------------|----------|
| Pre-processing       | 33       |
| Band adjustment I    | 9        |
| Cell computations    | 43       |
| Band adjustment II   | 15       |

of the BSW kernel that was a scalar implementation. The reduction in IPC is explained by the fact that a large majority of the instructions in our optimized code are SIMD instructions. Therefore, with two ports for SIMD instructions, an IPC of 2.17 is expected while accounting for a few scalar instructions. In contrast, there are 4 ports for scalar ALU instructions explaining an IPC of 3.17 for the original implementation.

Note that 16-bit and 8-bit integer precision values provide SIMD widths of 32 and 64, respectively, with AVX512 facilitating potential speedups of $32 \times$ and $64 \times$, respectively. In order to understand the gap between these ideal speedups and achieved speedups, Table 8 presents the breakdown of time spent in different components of the optimized 8-bit BSW. Run-time profiling shows that only 43% of the total time is spent in calculating the DP matrix; while remaining time is spent in pre-processing of the input sequences (which converts the input sequences from AoS to SoA order), and cell range adjustment. AoS to SoA conversion is performed specifically for the vectorized implementation and is not needed for the original scalar implementation.

Owing to multiple factors such as variations in sequence lengths and aborting of matrix computations (discussed in section 5), our inter-task vectorization ends up computing wasteful cells. Empirical analysis shows that the useful cells are roughly half of the total cells computed. Therefore, only 21.5% of the run time is spent in computation of useful cells of the DP matrices.
Figure 4: Comparison of scaling of three kernels and application between our implementation (Opt.) and original BWA-MEM (Orig.), from 1 core to 28 cores of SKX. Dotted line represents the perfect scaling. Datasets used: D1 and D5. Turbo boost was switched OFF for reliability of scaling performance.

6.3 End-to-end Performance Evaluation on Single Socket

In this section, we present the comparison of the end-to-end compute time of the original and our optimized implementation of BWA-MEM, with all the optimized kernels integrated.

6.3.1 Scaling with respect to the number of cores

We evaluate the multicore scaling of our implementation and three integrated kernels in (Figure 4). All the kernels demonstrate good scaling from 1 core to 28 cores on single socket closely matching the scaling of the original BWA-MEM with our optimized implementation achieving better scaling for the memory intensive SMEM and SAL kernels for the D5 dataset. We see a dip in scaling performance of the overall application for our implementation (D1: 22×, D5: 20×). The decline in scaling stems from the part of the application other than the three kernels. That is the part of the implementation that has not been optimized yet. Though all three key kernels achieve greater than 25× scaling, some of the components in Misc are memory bandwidth bound and do not scale beyond 15×.

6.3.2 Time to solution

We compared the time to solution of our optimized implementation with the original implementation using five different real datasets (Table 3). The run-time of our two implementations and original BW A-MEM, and speedup of our implementations over original BW A-MEM, are depicted in Figures 5a & 5c (single thread) and Figures 5b & 5d (single socket). All the three kernels sustain their benchmark speedup in the application. In fact, SAL kernel’s run-time barely contributes to the overall run time due to the 183× speedup. However, application performance benefit for the BSW kernel is lowered owing to the processing of extra seeds (Section 5.3). On an average, we see 14% extra sequence pairs aligned by our method. For dataset D2 on SKX, we observed that there were 13.5% extra seed pairs, but resulted in nearly 1.43× more BSW time, incurring a loss of speedup over BSW of BW A-MEM by 1.47×. On overall application: on SKX, we see speedup range of 2.6 × 3.5× on single thread, and of 1.7 × 2.4× on single socket; while, we see speedup range of 2.3 × 3.0× on single thread, and of 1.9 × 2.7× on single socket, on HSW.

7 Related Work

Owing to the complexity of BWA-MEM, a majority of the attempts to speed it up are confined to accelerating one of the three kernels, either on GPGPU or on FPGA [6,7,9]. Additionally, these methods pipeline the non-optimized kernels on the host CPU for execution. Out of the three kernels, given that standard SW has been extensively targeted for acceleration and BSW of BWA-MEM is a variant of standard SW, a lot of studies [6,9] have targeted only BSW for acceleration. Due to dependencies between the seeds within a read, all of the mentioned acceleration approaches for BSW kernel employ intra-task parallelism. Excluding [9], the other approaches manage to achieve 1.6× to 3× speedup on BSW and 1.45× to 2× overall. Chang et al. [7] exclusively target SMEM optimizations on FPGAs and demonstrate 4× and 1.26× performance improvement on SMEM and overall application, respectively. Due to pipelining of computations between host CPU and accelerator, the benefits of BSW speedup are contingent on speed of non-optimized kernels. Ahmed et al. [9] target all the three kernels for optimizations. They use 4 FPGAs to speedup
SAL and BSW kernels by $2.8 \times$ and $5.7 \times$ respectively. Also, they apply algorithmic enhancements to optimize SMEM kernel on host CPU, speeding it up by $1.7 \times$ and overall performance by $2.6 \times$. However, their output may differ from BWA-MEM output, due to bypassing of some of the heuristics used in BWA-MEM BSW. To the best of our knowledge, no published work contains a holistic architecture-aware optimization of BWA-MEM software on multicore systems.

FM-index methods and SW based alignment are widely used techniques in NGS data analysis and have been classified as computational building blocks [2]. Due to the intricacy of FM-index based algorithms, few works considered optimization of these problems [13–15] and most of them have targeted the simpler, exact search algorithm (find exact matches of full query sequences). Chacon et al. [15] developed a clever technique for exact search, which reduces the number of memory accesses. Application of their technique to SMEM search is non-trivial. Additionally, they tried software prefetching for exact search [15] with minimal benefit due to an inefficient design. Misra et al. [10] demonstrated significant performance gains on exact search with software prefetching by batching multiple queries together to hide memory latency.

Intra- and inter-task vectorization are both popular approaches for SW acceleration [10,19,22]. However, BSW of BWA-MEM has some key variations from standard SW as discussed in section 5. Therefore, there have been only a few attempts to accelerate exact BSW kernel from BWA-MEM.
8 Conclusion and Future Work

In this paper, we presented an efficient implementation of BW A-MEM for multicore systems while maintaining identical output so that the current users of BW A-MEM can seamlessly switch to the new implementation. We presented our improvements through architecture aware optimization to speedup the three key kernels - SMEM, SAL and BSW - by $2 \times$, $183 \times$, and $8 \times$, respectively. This results in an overall performance gain of $3.5 \times$ and $2.4 \times$ over the compute time of BW A-MEM on a single thread and single socket, respectively, of an Intel Skylake processor. Our implementation has been open sourced so that the users of BW A-MEM can benefit from increased performance.

We were successful in making the SAL kernel virtually insignificant contributor to the overall run time. The other two kernels are instruction bound and SMEM is also partly memory latency bound. Given the irregular structure of the algorithms, SMEM can not benefit from vectorization, while gains for BSW due to vectorization are limited. Therefore, processors that rely heavily on SIMD performance can only achieve limited performance on BW A-MEM. While better support for gather operations will help, an architecture that does not rely on SIMD for performance will be better.

As future work, we plan to make the following improvements - (i) attempt to improve the parts of BW A-MEM apart from the three kernels that we focused on in this paper in order to improve multicore scaling and performance of the overall application further, and (iii) explore if there is additional scope of reducing average memory latency of SMEM kernel and the instruction counts of SMEM and BSW kernels.

References

[1] Illumina Inc., “Hiseq™ series of sequencing systems,” url=https://www.illumina.com/content/dam/illumina-marketing/documents/products/datasheets/novaseq-6000-system-specification-sheet-770-2016-025.pdf, accessed: October 2018.
[2] M. Vasimuddin, S. Misra, and S. Aluru, “Identification of significant computational building blocks through comprehensive investigation of NGS secondary analysis methods,” [Preprint] bioRXiv, April 2018.
[3] M. A. DePristo, E. Banks, R. E. Poplin, and et al., “A framework for variation discovery and genotyping using next-generation DNA sequencing data,” Nat Genet, vol. 43, no. 5, pp. 491–498, 2011.
[4] Broad Institute: GATK best practices. [Online]. Available: https://software.broadinstitute.org/gatk/best-practices
[5] H. Li, “Aligning sequence reads, clone sequences and assembly contigs with bwa-mem,” arXiv preprint arXiv:1303.3997, 2013.
[6] E. J. Houtgast, V.-M. Sima, K. Bertels, and Z. Al-Ars, “Hardware acceleration of bwa-mem genomic short read mapping for longer read lengths,” Computational Biology and Chemistry, vol. 75, pp. 54 – 64, 2018. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1476927118301555
[7] M. F. Chang, Y. Chen, J. Cong, P. Huang, C. Kuo, and C. H. Yu, “The smem seeding acceleration for dna sequence alignment,” in 2016 IEEE 24th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), vol. 00, May 2016, pp. 32–39. [Online]. Available: doi.ieeecomputersociety.org/10.1109/FCCM.2016.21
[8] M. Alser, H. Hassan, H. Xin, O. Ergin, O. Mutlu, and C. Alkan, “Gatekeeper: A new hardware architecture for accelerating pre-alignment in dna short read mapping,” arXiv:1604.01789 [q-bio.GN], 2016.
[9] N. Ahmed, V. Sima, E. Houtgast, K. Bertels, and Z. Al-Ars, “Heterogeneous hardware/software acceleration of the bwa-mem dna alignment algorithm,” in 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov 2015, pp. 240–246.
[10] S. Misra, T. C. Pan, K. Mahadik, G. Powley, P. N. Vaidya, M. Vasimuddin, and S. Aluru, “Performance extraction and suitability analysis of multi- and many-core architectures for next generation sequencing secondary analysis,” in Proceedings of the 27th International Conference on Parallel Architectures and Compilation Techniques, ser. PACT ’18, 2018, pp. 3:1–3:14.
[11] P. Ferragina and G. Manzini, “An experimental study of an opportunistic index,” in Proceedings of the twelfth annual ACM-SIAM symposium on Discrete algorithms. Society for Industrial and Applied Mathematics, 2001, pp. 269–278.
[12] H. Li, “Exploring single-sample snp and indel calling with whole-genome de novo assembly,” Bioinformatics, vol. 28, no. 14, pp. 1838–1844, 2012. [Online]. Available: http://dx.doi.org/10.1093/bioinformatics/bts280
[13] J. Zhang, H. Lin, P. Balaji, and W.-c. Feng, “Optimizing burrows-wheeler transform-based sequence alignment on multicore architectures,” in Cluster, Cloud and Grid Computing (CCGrid), 2013 13th IEEE/ACM International Symposium on. IEEE, 2013, pp. 377–384.

[14] A. Chacón, S. Marco-Sola, A. Espinosa, P. Ribeca, and J. C. Moure, “Boosting the FM-Index on the GPU: Effective techniques to mitigate random memory access,” IEEE/ACM Trans. Comput. Biol. Bioinformatics, vol. 12, no. 5, pp. 1048–1059, Sep. 2015. [Online]. Available: http://dx.doi.org/10.1109/TCBB.2014.2377716

[15] A. Chacón, J. C. Moure, A. Espinosa, and P. Hernández, “n-step fm-index for faster pattern matching,” Procedia Computer Science, vol. 18, pp. 70 – 79, 2013, 2013 International Conference on Computational Science. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S187705091300313X

[16] J. Pantaleoni and N. Subtil. NVBIO: A library of reusable components designed by NVIDIA corporation to accelerate bioinformatics applications using CUDA. [Online]. Available: http://nvlabs.github.io/nvbio/

[17] P. Rastogi and R. Guddeti, “Gpu accelerated inexact matching for multiple patterns in dna sequences,” in 2014 International Conference on Advances in Computing, Communications and Informatics (ICACCI), Sept 2014, pp. 163–167.

[18] L. S. N. Nunes, J. L. Bordim, K. Nakano, and Y. Ito, “A fast approximate string matching algorithm on gpu,” in 2015 Third International Symposium on Computing and Networking (CANDAR), Dec 2015, pp. 188–192.

[19] J. Daily, “Parasail: Smd c library for global, semi-global, and local pairwise sequence alignments,” BMC Bioinformatics, vol. 17, no. 1, p. 81, Feb 2016. [Online]. Available: https://doi.org/10.1186/s12859-016-0930-z

[20] T. Rognes, “Faster smith-waterman database searches with inter-sequence simd parallelisation,” BMC bioinformatics, vol. 12, no. 1, p. 221, 2011.

[21] I. T. Li, W. Shum, and K. Truong, “160-fold acceleration of the smith-waterman algorithm using a field programmable gate array (fpga),” BMC Bioinformatics, vol. 8, no. 1, p. 185, Jun 2007.

[22] Y. Liu, B. Schmidt, and D. L. Maskell, “Cudasw++ 2.0: enhanced smith-waterman protein database search on cuda-enabled gpus based on simt and virtualized simd abstractions,” BMC research notes, vol. 3, no. 1, p. 93, 2010.