Engineering Schottky Barrier in Black Phosphorus field effect devices for spintronic applications

M. Venkata Kamalakar*, B. N. Madhushankar, André Dankert, Saroj P. Dash#
Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296, Göteborg, Sweden
e-mail: *venkata.mutta@chalmers.se; #saroj.dash@chalmers.se

ABSTRACT

Black phosphorous (BP) is recently unveiled as a promising two-dimensional direct bandgap semiconducting material. Here, we report the ambipolar field effect transistor behavior of multilayers of BP with ferromagnetic tunnel contacts. We observe a reduced Schottky barrier < 50 meV by using TiO$_2$/Co contacts, which could be further tuned by gate voltages. Eminently a good transistor performance is achieved in our devices, with drain current modulation of four to six orders of magnitude. The charge carrier mobility is found to be $\sim$155 and 0.18 cm$^2$ V$^{-1}$ s$^{-1}$ for holes and electrons respectively at room temperature. Furthermore, magnetoresistance calculations reveal that the resistances of the BP device with applied gate voltages are in the appropriate range for injection and detection of spin polarized holes. Our results demonstrate the prospect of engineering BP nanolayered devices for efficient nanoelectronic and spintronic applications.

Key words: Black Phosphorous, Phosphorene, Field Effect Transistor, Spintronics, Ferromagnet, Tunnel contact, magnetoresistance.
INTRODUCTION

The interest in two-dimensional (2D) van der Waals crystals and their heterostructures for next-generation electronics is rapidly growing since the past few years\cite{1,2}. Over the last decade, graphene has attracted enormous attention for its extremely high carrier mobility\cite{1,2} and long distance spin transport capabilities\cite{3–5}. These qualities have large prospects for applications such as ultra-high frequency transistors\cite{6} and spin communication\cite{7}. However, pristine graphene lacks a band gap and spin-orbit coupling, which are crucial requirements for switching action of transistors\cite{6} and spin based devices\cite{7}. In this context, semiconducting 2D crystals of transition metal dichalcogenides (TMD) with larger bandgaps and spin-orbit coupling have been investigated intensively for future electronics devices\cite{7–12}. However, TMD transistors show n-type behavior because of the atomic vacancies and the location of the charge neutral level in the vicinity of the conduction band. This considerably limits their role for CMOS applications, where both n and p-type transistor are required as complementary devices in logic circuits\cite{7–9,11–13}. Additionally, spin transport in TMDs is largely eclipsed due to the intrinsically high spin-orbit coupling in them. Therefore, a 2D crystal possessing both charge and spin transport/control capability is necessary for integration of spin-based memory and logic operations in a single device.

The recently reported semiconducting 2D crystal “black phosphorous (BP)” possesses a direct bandgap of 0.3-2 eV depending on its thickness\cite{14}, and may lead to potential applications in nanoelectronics and optoelectronics. The field effect transistors (FET) and photo response have been demonstrated in BP nanolayers showing ambipolar property (both n and p-type)\cite{14–18}. In addition to electronic transport, spin related properties of BP are also interesting, because of the low spin-orbit coupling and +1/2 nuclear spin of phosphorous (P) atoms\cite{19}. This makes BP a unique platform for investigating the creation of spin polarized charge carriers\cite{20}, nuclear hyperfine interaction\cite{21} and dynamical nuclear spin polarization\cite{22} effects.

For these experiments, the realization of high performance BP transistors with ferromagnetic tunnel contacts constitute the primary requirements\cite{20,23,24}. Such contacts can act as efficient spin injectors/detectors, and circumvent the conductivity mismatch issues\cite{23,24}. However, it has been recently reported that there exists a Schottky barrier of 200 meV for holes at the Ti/BP
interfaces\textsuperscript{[15]}. With such energy barriers at the interface, only carriers that are thermally emitted over the Schottky barrier can flow across the contact, resulting in a reduced spin polarization and a low drive current\textsuperscript{[125–28]}. Therefore, engineering of a reduced Schottky barrier via suitable contact materials is necessary to enhance the performance of BP transistor, which has not been explored so far\textsuperscript{[10,14]}. In view of the interesting electronic and spintronics properties of BP, further investigations of this material are desirable to understand the electronic processes involved and unveil its prospect.

In this article, we present field effect transistor characteristics of multilayers of black phosphorous with ultra-thin TiO\textsubscript{2} and cobalt (Co) contacts. Using such ferromagnetic tunnel contacts, we demonstrate a reduction in Schottky barrier, which could further be tuned by gate voltages. The BP devices show ambipolar transistor behavior with efficient hole conduction, high on/off drain current and mobilities. Magnetoresistance calculations based on spin diffusion model\textsuperscript{[23,24]} show that the transistor properties are in the appropriate range for exploration of spin related phenomena in BP.

**RESULTS AND DISCUSSIONS**

The device scheme and an optical microscope image of a fabricated BP field effect transistor are presented in figure 1 (a) and (b) respectively. The BP flakes were prepared on a clean SiO\textsubscript{2} (285 nm), highly doped Si substrate. We used BP exfoliated from a bulk crystal (purchased from Smart Elements) using the conventional scotch tape method\textsuperscript{[2]}. The flakes were identified by a combination of optical and atomic-force microscopy as shown in Supplementary Information Fig. S1. We used multilayer BP with a thickness of ~ 5 nm and widths of around ~ 3 \( \mu \)m. The SiO\textsubscript{2}/n-Si is used as a back gate to control the carrier concentration in the BP. Contacts of TiO\textsubscript{2} (1nm)/Co (65 nm)/Al (2 nm) were fabricated on BP samples by electron-beam lithography, electron beam evaporation and lift-off techniques. Electrodes with widths 0.5–1 \( \mu \)m and a channel length of 1-3 \( \mu \)m were used. The BP flakes were covered by PMMA e-beam resist soon after exfoliation to avoid possible degradation upon longer exposure to air\textsuperscript{[16]}. All the transport measurements were carried out under high vacuum conditions.
Figure 1. Nanolayer black phosphorous (BP) field effect device (a) Schematic of a BP FET with source, drain and back gate electrodes. (b) Optical image of a fabricated 5 nm BP FET with TiO$_2$ (1nm)/Co contacts and SiO$_2$/n-Si back gate.

To extract the Schottky barrier height at the Co/TiO$_2$/BP contacts, we performed detailed temperature dependent drain–source current ($I_{ds}$) voltage ($V_{ds}$) characteristics of device at different gate voltages. The BP devices showed ambipolar behavior with gate voltage ($V_g$), hole conduction for $V_g < 0$ and electron conduction for $V_g > 0$. In Fig.2a, we show representative temperature dependence of $I_{ds}$–$V_{ds}$ characteristics at gate voltage of $V_g = 20$V. Such dependence of $I_{ds}$ indicates the presence of a Schottky barrier at the interface. We analyze the data using the thermionic emission equation describing the electrical transport through a Schottky barrier into the BP channel $^{[25–27]}$

$$I_{ds} = AA^* T^2 \exp \left[ -\frac{e}{k_B T} \left( \Phi_b - \frac{V_{ds}}{n} \right) \right]$$

where $A$ is the contact area, $A^*$ is the Richardson constant, $e$ is the electron charge, $k_B$ the Boltzmann constant, $\Phi_b$ is the Schottky barrier height, and $n$ is the ideality factor. Figure 2b shows the Arrhenius plot (ln ($I_{ds}T^{-2}$) versus $T^{-1}$) for different bias voltages $V_{ds}$. The slopes $S$ ($V_{ds}$) extracted from the Arrhenius plot follow a linear dependence with $V_{ds}$ ($S(V_{ds}) = -(e/k_B)(\Phi_b - (V_{ds}/n))$), as displayed in Figure 2c. The Schottky barrier is evaluated from the extrapolated value of the slope at zero $V_{ds}$ ($S_0 = -(e\Phi_b/k_B)$).
Figure 2. Schottky barrier for BP/TiO\textsubscript{2}/Co contact. (a) Temperature dependence of $I_{ds}$–$V_{ds}$ at $V_g=20$V. (b) Arrhenius plot with $I_{ds}T^2$ dependence on $T^{-1}$ with linear fits provides slope $S$ at $V_g=20$V and different $V_{ds}$. (c) Bias voltage dependence of the extracted slope $S$ provides the zero bias slope $S_0$, which is used to calculate the Schottky barrier height. (d) Schottky barrier height $\Phi_b$ extracted at different gate voltages. (e) Band diagram depicts the BP/TiO\textsubscript{2}/Co interfaces for both p and n-type behavior of BP with gate voltage. $V_g$ and $V_{FB}$ represent gate voltage and flat band voltages respectively.

The evaluated Schottky barrier for different gate voltages is presented in Fig. 2d. For hole conduction ($V_g < 0$), we observe a very small Schottky barrier of $< 50$ meV. Notably, the barrier heights obtained with our TiO\textsubscript{2}/Co contacts are much lower than recent reports of $200$ meV with Ti/Au contacts\textsuperscript{[14,15]}. Higher work function of Co in comparison to Ti and/or de-pinning of Fermi level by ultra-thin TiO\textsubscript{2} may be responsible for such reduction of the Schottky barrier of BP in
the hole conduction regime\textsuperscript{[10,25]}. In the electron conduction conditions with $V_g > 0$, a higher Schottky barrier height $\Phi_b$ of 200 meV at $V_g=20$ V has been extracted. We note that the Schottky barrier can be tailored by applying a gate voltage. As shown in Fig.2d, the Schottky barrier height can be reduced to 25 meV for holes and 50 meV for electrons at high magnitudes of gate voltage. The lowering of the Schottky barrier at higher gate voltages for both electrons and holes are also evident from $I_{ds}$–$V_{ds}$ characteristics shown in Supplementary Information Fig. S2. Such lowering of Schottky barrier can be attributed to the tuning of band alignment of Co and BP and also doping of BP with gate voltage as depicted in Fig. 2e. The low Schottky barrier also gives rise to a lower contact resistance of Co/TiO$_2$/BP devices. By applying a gate voltage, a drastic reduction of the contact $R_{\text{cont}} = 1.4 \times 10^{-9}$ Ωm$^2$ and a channel resistivity of $\rho_{\text{ch}} = 2.4 \times 10^{-4}$ Ωm could be achieved in the hole conduction regime. Similarly, for electrons the $R_{\text{cont}} = 1.75 \times 10^{-9}$ Ωm$^2$ and $\rho_{\text{ch}} = 7.2 \times 10^{-2}$ Ωm could be obtained. Such engineering of interface resistances using Co/TiO$_2$ contacts and gate voltages are of great significance for BP transistors with electrical spin injection capabilities.

Next we examine the field effect transistor (FET) characteristics of BP with TiO$_2$/Co source and drain contacts and SiO$_2$/n-Si back gate. The output characteristics were obtained by measuring the drain–source current ($I_{ds}$) while sweeping the drain–source voltage ($V_{ds}$), at several gate voltages ($V_g$). Figure 3a presents the measured output characteristics showing a non-linear behavior at higher $V_{ds}$ and linear dependence only in a small bias voltage range. The presence of a finite Schottky barrier and the carrier depletion at the interfaces gives rise to such bias voltage dependence\textsuperscript{[10,14]}. The measurements of $I_{ds}$–$V_{ds}$ at different gate voltages $V_g$ shows an efficient modulation of the drain current $I_{ds}$ and a transistor behavior at room temperature. Notably, significant source-drain conduction has been observed for both hole ($V_g < 0$) and electron ($V_g > 0$) conduction regime, proving ambipolar behavior of BP FET.

In Fig. 3b we show the room temperature transfer characteristics of BP transistor obtained by measuring the $I_{ds}$ with back gate voltage $V_g$ sweep with constant $V_{ds}$. The measured data shows a typical ambipolar BP FET with asymmetry in $I_{ds}$, which is determined by the position of the Co Fermi level close to the valence or conduction bands of the BP. The negative and positive gate voltages correspond to hole and electron doping in BP respectively. The high current densities reaching up to 150 $\mu$Aμm$^{-2}$ for holes and 1 $\mu$Aμm$^{-2}$ for electrons with carrier densities of $9 \times$
$10^{12}$ cm$^{-2}$, make the device characteristics even more viable for applications. The ambipolar behavior in BP devices is dominant in p-type character, in contrast to the mostly observed n-type behavior of MoS$_2$ and WS$_2$ devices. Our BP devices with ferromagnetic tunnel contacts show a reasonable transistor $I_{on}/I_{off}$ ratio with $>10^4$ for hole and $>10^2$ for electron conduction regimes at room temperature. We would like to emphasize here that it is possible to achieve even higher drain current modulation as the present on state current of our devices is below the saturation. Attaining such high values is limited by the achieved doping level by backgate voltage and breakdown electric field of the SiO$_2$ dielectric. By using high-k gate dielectrics, it should be possible to achieve higher carrier densities and hence a higher saturation of the drain current. We observe a subthreshold swing (SS) of $\sim 11$ V per decade (V/dec), which lies in the same order of magnitude as reported in other 2D semiconductor devices with 285 nm thick SiO$_2$ dielectric$^{[10]}$. Compared to commercial Si devices with SS of 70 mV/dec, the larger SS obtained in our devices can be attributed to the thicker SiO$_2$ backgate dielectric and possible presence of interface states$^{[27]}$. It is therefore expected that the SS can be significantly improved by using ultra-thin high-k dielectrics with minimum interface states. The effective field-effect mobility in BP for both electrons and holes has been estimated from the measured transfer characteristics. We extract the slope in the linear region of the data by using the standard expression$^{[8,10,14]}$

$$
\mu = [(dI_{ds}) / (dV_g)] \times [L / (WC_iV_{ds})]
$$

where $L = 690$ nm is the length and $W = 3.1$ $\mu$m is the width of the channel, $V_{ds} = 0.5$ V and $C_i$ is the capacitance between the channel and the back-gate per unit area ($C_i = \varepsilon_0\varepsilon_r/d$; $\varepsilon_r = 3.9$ for SiO$_2$; $d = 285$ nm for back gate oxide thickness)$^{[8]}$. Figure 3b shows the transfer curve, where $dI_{ds}/dV_g$ is the slope of the linear fit for mobility extraction. Since BP devices show an ambipolar behavior, we extract effective channel mobility for both electron and hole transport regimes. The extracted hole mobility is found to be 155 cm$^2$V$^{-1}$s$^{-1}$ for a 5 nm thick BP flake on SiO$_2$ substrates, which is comparable to reported values$^{[15,17,18]}$. The mobility is also dependent on thickness of the BP, the highest value being reported for 10 nm flakes$^{[15,17,18]}$. The electron mobility is extracted to be 0.18 cm$^2$V$^{-1}$s$^{-1}$, which is considerably lower than the hole mobility. The higher
Schottky barrier and lower mobility in electron conduction regime gives rise to three orders of magnitude lower current density than for holes. We have also observed similar mobility values for BP measured in four terminal configurations, which rules out the possible influence of the contacts (see Supplementary Information Fig. S3). The calculated mobilities may be the underestimated values as we have not considered the effects of anisotropic electronic properties in BP, defect states with back gate SiO$_2$ and possible surface degradation of BP even with short exposure to atmosphere$^{[15,17,18]}$. We further examined the temperature dependence of the transistor characteristics of our BP FETs. The transfer curves measured at 2 and 300 K are shown in Fig. 3d. The transistor $I_{on}/I_{off}$ performance is increased by two orders of magnitude at 2 K. These results clearly indicate that BP field effect transistors with ferromagnetic tunnel contacts, show a high mobility and significantly large values of on state current for hole conduction regime. Such p-type BP transistors can be used in complementary circuits together with n-type MoS$_2$ transistors for 2D transparent electronics.

Figure 3. Characterization of BP FETs. (a) Output characteristics $I_{ds}$–$V_{ds}$ measured in high bias range for different gate voltages ($V_g$). (b) Transfer characteristic in linear scale for $V_{ds} = 1$V. The effective field-effect mobility for electrons and holes are 155 and 0.18 cm$^2$ V$^{-1}$ s$^{-1}$ respectively, as calculated from the subthreshold slope of the transfer curve. (c) Transfer
characteristic in logarithmical scale for \( V_{ds} = 1\text{V} \) with an \( I_{on}/I_{off} > 10^4 \) and sub-threshold swing \( SS \sim 11 \text{ V/dec} \). (d) Temperature dependence of BP transfer characteristic \( I_{ds}=V_g \) for \( V_{ds}= 1\text{V} \) measured at 2 and 300 K.

In addition to the electronic properties of p-type BP devices, spin transport studies of holes are also interesting because of the low spin-orbit coupling in BP and the presence of nuclear spin of \( \frac{1}{2} \) on each of it’s P atom\(^{[19]} \). A versatile way of creating spin polarization in semiconductors is the electrical spin injection from ferromagnetic tunnel contacts\(^{[20]} \). However, the resistances of the contacts and semiconductors channels have to be in the optimum range to observe magnetoresistance effects. In order to grasp the capability of BP for spin polarized transport, we evaluate the contact and channel resistances on the basis of spin diffusion theory\(^{[23]} \). We consider a FM/I/BP/I/FM structure, where I is the interface contact and FM is the ferromagnet. The optimal contact and channel resistances required are estimated by considering experimentally measured mobility and resistance values. To observe a high MR, the interface resistance should lie within the range

\[
\rho_N L < R_{cont} A < \rho_N \frac{l_s^2}{L} 
\]

(3)

where \( \rho_N \) is the resistivity of the BP channel of length \( L \), \( R_{cont} \) is the contact resistance with a contact area \( A \), \( l_s \) is the spin diffusion length. The calculated MR as a function of contact RA is shown in Fig. 4a, where we have considered \( L = 50 \text{ nm} \) and different expected spin lifetimes (0.01- 1 ns) for holes in BP. Experimentally, lateral \( L \) of < 50 nm can be achieved by electron beam lithography, shadow evaporation\(^{[29]} \) or using vertical device structures of BP. The spin lifetime for holes in the valence band are expected to be in the above mentioned range and not exactly known at this stage.. In BP,Spin relaxation mechanism due to nuclear hyperfine interaction may exist\(^{[21,22]} \). However, experiments performed on nuclear spin of C-13 atomic graphene do not show significant influence on spin lifetime. Thus, the adopted spin lifetime values are reasonable considering the low spin orbit coupling expected in BP. The MR calculations show the possibility of observation of a significant magnetoresistance in BP in a narrow contact resistance range. The low MR for small contact resistances is due to the conductivity mismatch, preventing a spin injection from the Co into BP. For larger contact resistances, the reduction in MR is caused by the relaxation of the spins in the BP channel due to longer dwell time\(^{[23]} \).
The contact resistance is $R_{\text{cont}}A = 1.4 \times 10^{-9} \ \Omega \text{m}^2$ for on state of BP FET in the hole conduction regime with $V_g = -80 \ \text{V}$, and lies in the optimum range for the observation of a large MR. In fig. 4b, we also show that the calculated MR as a function of gate voltage $V_g$ and contact resistance $R_{\text{cont}}A$ for hole conduction. The observed change in MR with gate voltage is because of the tuning of the hole carrier density in the BP channel by the gate voltage. The contact resistance of our device is shown by the dashed lines in Figure 4a and 4b. Our results demonstrate the tunability of the channel and contact resistances, and expected MR by applying a gate voltage. The TiO$_2$/Co spin tunnel contacts are in the optimum range for spin injection and detection in BP in higher hole doping ranges. Although our present devices with TiO$_2$/Co contacts show more favorable conditions for spin polarized hole injection, similar results for electrons spin could be achieved by using lower work function materials at the interfaces$^{[30-32]}$. Such design will align the Fermi level near the conduction band edge and lower contact resistances to more optimal values$^{[32]}$. Further enhancements in the MR can be achieved by improving the mobility of the BP channel by high k-dielectrics encapsulation$^{[8]}$. These heterostructures of BP with ferromagnetic contacts will allow exploring electrical methods$^{[20,33,34]}$ to create spin polarization in BP, and also alternative approaches such as thermal$^{[35]}$ and dynamical$^{[36]}$ spin injection.

**Figure 4. Magnetoresistance (MR) calculation** – Calculated MR of FM/I/BP/I/FM spin FET structure as a function of the contact resistance area product ($R_{\text{cont}}A$) for a channel length $L=50 \ \text{nm}$ at room temperature. The values are normalized to the peak value at a spin lifetime $\tau_{\text{sf}} = 1 \ \text{ns}$. (a) MR calculation for different spin lifetimes $\tau_{\text{sf}}$ at a gate voltage $V_g = -80 \ \text{V}$ (on-state). The dashed lines represent the $R_{\text{cont}}A$ value for the TiO$_2$/Co tunnel contact on BP in our experiments. (b) MR as a function of gate voltage and contact resistance for $\tau_{\text{sf}}=0.5 \ \text{ns}$ and $L=50\text{nm}$. The dashed lines represent the variation of contact $R_{\text{cont}}A$ of our devices with gate voltage.
CONCLUSION

In conclusion, we have investigated the field effect transistor characteristics of nanolayers of black phosphorous with ferromagnetic tunnel contacts. Lower contact resistances and ambipolar behavior with both hole and electron conduction could be achieved by using TiO$_2$/Co contacts and gate voltage. The Schottky barrier heights could be reduced to values less than 50 mV for both holes and electrons. We demonstrate ambipolar transistor with $I_{on}/I_{off} > 10^4$ and on-state current reaching 150 µA/µm in the hole conduction regime. At low temperatures the transistor characteristics show an increase in $I_{on}/I_{off}$ by two orders of magnitude $> 10^6$, which are comparable to other 2D semiconducting crystal based devices. Due to a smaller bandgap of multi-layer BP devices, both electron and hole conduction could be achieved by application of gate voltages. The effective field effect channel mobility for holes and electrons are found to be $\sim$155 and 0.18 cm$^2$ V$^{-1}$ s$^{-1}$ respectively at room temperature. Our calculations for the observation of magnetoresistance in BP indicate that the resistances of BP/TiO$_2$/Co FET can be tuned to the optimum range by the application of gate voltage. The integration of such ferromagnetic tunnel contacts on BP circumvents the conductivity mismatch problem with promising transistor performance. This opens up the prospect for spin based nanoelectronic devices using 2D semiconducting crystals.

Acknowledgements

The authors acknowledge the support from colleagues of Quantum Device Physics Laboratory and Nanofabrication Laboratory at Chalmers University of Technology. This research is financially supported by Nano Area of Advance program at Chalmers University of technology, EU FP7 Marie Curie Career Integration grant, and Swedish Research Council Young Researcher Grant.

References

[1] A. K. Geim, I. V Grigorieva, Nature 2013, 499, 419–25.
[2] K. S. Novoselov, V. I. Fal’ko, L. Colombo, P. R. Gellert, M. G. Schwab, K. Kim, Nature 2012, 490, 192–200.
[3] N. Tombros, C. Jozsa, M. Popinciuc, H. T. Jonkman, B. J. van Wees, Nature 2007, 448, 571–574.
[4] B. Dlubak, M.-B. Martin, C. Deranlot, B. Servet, S. Xavier, R. Mattana, M. Sprinkle, C. Berger, W. a. De Heer, F. Petroff, A. Anane, P. Seneor, A. Fert, *Nat. Phys.* 2012, 8, 557–561.

[5] A. Dankert, M. V. Kamalakar, J. Bergsten, S. P. Dash, *Appl. Phys. Lett.* 2014, 104, 192403.

[6] F. Schwierz, *Nat. Nanotechnol.* 2010, 5, 487–96.

[7] H. Dery, H. Wu, B. Ciftcioglu, M. Huang, Y. Song, R. Kawakami, J. Shi, I. Krivorotov, I. Žuti, L. J. Sham, I. Zutic, *IEEE Trans. Electron Devices* 2012, 59, 259–262.

[8] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* 2011, 6, 147–50.

[9] D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, M. C. Hersam, 2014, 1102–1120.

[10] A. Dankert, L. Langouche, M. V. Kamalakar, S. P. Dash, *ACS Nano* 2014, 8, 476–82.

[11] S. Das, H.-Y. Chen, A. V. Penumatcha, J. Appenzeller, *Nano Lett.* 2013, 13, 100–5.

[12] K. F. Mak, C. Lee, J. Hone, J. Shan, T. F. Heinz, *Phys. Rev. Lett.* 2010, 105, 136805.

[13] A. Dankert, L. Langouche, M. V. Kamalakar, S. P. Dash, *ACS Nano* 2014, 8, 476–82.

[14] L. Li, Y. Yu, G. J. Ye, Q. Ge, X. Ou, H. Wu, n.d.

[15] H. Liu, A. T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, P. D. Ye, *ACS Nano* 2014, 8, 4033–41.

[16] F. Xia, H. Wang, Y. Jia, n.d.

[17] S. P. Koenig, R. a. Doganov, H. Schmidt, a. H. Castro Neto, B. Özyilmaz, *Appl. Phys. Lett.* 2014, 104, 103106.

[18] M. Buscema, D. J. Groenendijk, S. I. Blanter, G. a Steele, H. S. J. van der Zant, A. Castellanos-Gomez, *Nano Lett.* 2014, 14, 3347–52.

[19] J. J. Pla, K. Y. Tan, J. P. Dehollain, W. H. Lim, J. J. L. Morton, F. a Zwanenburg, D. N. Jamieson, A. S. Dzurak, A. Morello, *Nature* 2013, 496, 334–8.

[20] S. P. Dash, S. Sharma, R. S. Patel, M. P. de Jong, R. Jansen, *Nature* 2009, 462, 491–494.

[21] R. J. Warburton, *Nat. Mater.* 2013, 12, 483–93.

[22] H. Search, C. Journals, A. Contact, M. Iopscience, I. P. Address, n.d., 395.
[23] A. Fert, H. Jaffrès, *Phys. Rev. B* **2001**, *64*, 184420.

[24] G. Schmidt, D. Ferrand, L. Molenkamp, a. Filip, B. van Wees, *Phys. Rev. B* **2000**, *62*, R4790–R4793.

[25] R. T. Tung, *Phys. Rev. Lett.* **2000**, *84*, 6078–81.

[26] J. Bardeen, *Phys. Rev.* **1942**, *71*, 717.

[27] S. M. Sze, K. K. Ng, *Physics of Semiconductor Devices*, John Wiley & Sons, Inc., Hoboken, NJ, USA, **2006**.

[28] B. C. Min, K. Motohashi, C. Lodder, R. Jansen, *Nat. Mater.* **2006**, *5*, 817–22.

[29] J.-F. Dayen, V. Faramarzi, M. Pauly, N. T. Kemp, M. Barbero, B. P. Pichon, H. Majjad, S. Begin-Colin, B. Doudin, *Nanotechnology* **2010**, *21*, 335303.

[30] R. S. Patel, S. P. Dash, M. P. de Jong, R. Jansen, *J. Appl. Phys.* **2009**, *106*, 016107.

[31] R. Jansen, B. C. Min, S. P. Dash, *Nat. Mater.* **2010**, *9*, 133–8.

[32] R. Jansen, B. C. Min, S. P. Dash, S. Sharma, G. Kioseoglou, a. T. Hanbicki, O. M. J. van ’t Erve, P. E. Thompson, B. T. Jonker, *Phys. Rev. B* **2010**, *82*, 241305.

[33] A. Dankert, R. S. Dulal, S. P. Dash, *Sci. Rep.* **2013**, *3*, 3196.

[34] S. Sharma, a. Spiesser, S. P. Dash, S. Iba, S. Watanabe, B. J. van Wees, H. Saito, S. Yuasa, R. Jansen, *Phys. Rev. B* **2014**, *89*, 075301.

[35] A. Dankert, S. P. Dash, *Appl. Phys. Lett.* **2013**, *103*, 242405.

[36] E. Shikoh, K. Ando, K. Kubo, E. Saitoh, T. Shinjo, M. Shiraishi, *Phys. Rev. Lett.* **2013**, *110*, 127201.
Supplementary Information

Engineering Schottky Barrier in Black Phosphorus field effect devices for spintronic applications

M. Venkata Kamalakar*, B. N. Madhushankar, André Dankert, Saroj P. Dash#
Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296, Göteborg, Sweden
e-mail: *venkata.mutta@chalmers.se; #saroj.dash@chalmers.se

Nanolayers of Black Phosphorous: Flakes of black phosphorous are exfoliated onto Si/SiO$_2$ substrate by the scotch tape technique. Flakes having thicknesses ~ 5 nm are selected by a combination of optical and atomic force microscopy (Fig. S1).

Figure S1: (a) Optical microscope image of a group of Black phosphorus flakes with various thicknesses. (b) Atomic force microscope image of a 5 nm thin flake.
Schottky Barrier for the electron and hole regimes: Reduction in Schottky barrier in the electron and hole regimes is evident from the weak temperature dependence of the $I_{ds}$–$V_{ds}$ characteristics obtained on the device at the two extremes of applied gate voltage as presented in Fig. S2

![Image of I$_{ds}$–V$_{ds}$ characteristics](image)

Figure S2: $I_{ds}$–$V_{ds}$ characteristics at different temperatures for the (a) Hole regime at $V_g = -80$ V (b) Electron regime at $V_g = 80$ V.

Mobility extraction from four probe measurements: In order to rule out the possible influence of contacts on the evaluation of field effect mobility, we performed the gate dependent four probe measurements of the channel. The hole and electron mobilities using the four probe measurements were found to be close to the values obtained in FET measurements.

![Image of mobility extraction](image)

Figure S3: Gate dependent four probe measurements of the BP channel with extraction of hole and electron mobilities at room temperature.