AppGNN: Approximation-Aware Functional Reverse Engineering using Graph Neural Networks

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ABSTRACT
The globalization of the Integrated Circuit (IC) market is attracting an ever-growing number of partners, while remarkably lengthening the supply chain. Thereby, security concerns, such as those imposed by functional Reverse Engineering (RE), have become quintessential. RE leads to disclosure of confidential information to competitors, potentially enabling the theft of intellectual property. Traditional functional RE methods analyze a given gate-level netlist through employing pattern matching towards reconstructing the underlying basic blocks, and hence, reverse engineer the circuit’s function.

In this work, we are the first to demonstrate that applying Approximate Computing (AxC) principles to circuits significantly improves the resiliency against RE. This is attributed to the increased complexity in the underlying pattern-matching process. The resiliency remains effective even for Graph Neural Networks (GNNs) that are presently one of the most powerful state-of-the-art techniques in functional RE. Using AxC, we demonstrate a substantial reduction in GNN average classification accuracy—from 98% to a mere 53%. To surmount the challenges introduced by AxC in RE, we propose the highly promising AppGNN platform, which enables GNNs (still being trained on exact circuits) to: (i) perform accurate classifications, and (ii) reverse engineer the circuit functionality, notwithstanding the applied approximation technique. AppGNN accomplishes this by implementing a novel graph-based node sampling approach that mimics generic approximation methodologies, requiring zero knowledge of the targeted approximation type.

We perform an extensive evaluation targeting wide-ranging adder and multiplier circuits that are approximated using various AxC techniques, including state-of-the-art evolutionary-based approaches. We show that, using our method, we can improve the classification accuracy from 53% to 81% when classifying approximate adder circuits that have been generated using evolutionary algorithms, which our method is oblivious of. Our AppGNN framework is publicly available under https://github.com/ML-CAD/AppGNN.

KEYWORDS
Graph neural networks, GNN, Security, Approximate computing, Reverse engineering, Machine learning

1 INTRODUCTION
Functional Reverse Engineering (RE) aims to analyze gate-level netlists that have been synthesized from a Register-Transfer Level (RTL) description of an Integrated Circuit (IC) design. A gate-level netlist contains information about the individual gates of a design and how they are interconnected to implement certain functionality. A description of which functionality is actually implemented however, is no longer present. It is the goal of functional RE to retrieve this information and reconstruct a high-level description of the functionality within the netlist [21]. While the retrieval of a high-level description itself is challenging, it becomes even more of a task when analyzing approximate circuits.

Approximate Computing (AxC) achieves significant advantages over traditional computing concerning circuit area and power efficiency in scenarios where some loss of quality in the computed result can be tolerated [12]. For instance, in deep learning [7, 28] or media processing [20] such as audio, video, or image compression, where an exact computation is often not necessary due to the limited perception capability in humans [24].

Despite the widespread employment of AxC, the research community did not investigate its security aspects so far. To the best of our knowledge, we are the first to evaluate the resilience of AxC to functional RE. In this work, we show that existing functional RE methods fail to reverse engineer approximate circuits.

In the following we discuss the limitations of existing methods, which are also summarized in Table 1.

1.1 Motivation and Research Challenges
Golden Design Requirement: Traditional functional RE methods that are based on template matching [5, 10, 15, 16] have shown great potential in unveiling the functionality of gate-level netlists. However, these methods work by identifying sub-circuits and matching them to a “golden” library of components known in prior. This makes them prone to erroneous classification caused by variations in the implementation of a module (i.e., structural or functional variations). With the rise of AxC, these methods finally fall short.

Table 1. Comparison of functional RE methods and their ability to identify exactly matching sub-circuits, sub-circuits with slight variations, and their applicability on AxC

| Method                  | Exact matching | Variations | AxC |
|-------------------------|----------------|------------|-----|
| Template matching       | ✓              | ×          | ✓   |
| [10, 15, 16, 21]        |               |            |     |
| Traditional ML [6, 8]   | ✓              | ✓          | ×   |
| GNN-RE [2]              | ✓              | ✓          | ×   |
| Proposed AppGNN         | ✓              | ✓          | ✓   |
Approximation aggressiveness increases along the X-axis following key research challenges.

Figure 1. Number of identified sub-circuits by bsim [21] in an exact 16-bit adder and an approximate 16-bit adder circuit.

Figure 2. Node-level classification accuracy of GNN-RE [2] on the approximate adders from the EvoApprox [19] dataset. Approximation aggressiveness increases along the X-axis (drop in normalized area). GNN-RE classification accuracy drops with the increase in approximation aggressiveness.

due to the vast design space that is opened up by the different possible methods of approximation. To investigate this, we employed the bsim tool [21], one of the state-of-the-art algorithmic RE methods, on selected exact and approximate adder circuits. In our experiments, we have observed a mismatch between the types of recovered sub-circuits between the exact and the approximate implementations, i.e., they are not mapped to the same functionality, as Figure 1 illustrates. This further highlights the fact that template matching-based approaches are not suitable for functional RE of AxCs.

Low Classification Performance: Machine Learning (ML)-based approaches that employ Convolutional Neural Networks (CNNs) [6, 8] as well as Graph Neural Networks (GNNs) [2] have been introduced for the task of functional RE [4]. They promise to be more resilient against variations due to their generalization capabilities. However, their performance in the the presence of AxC has not yet been evaluated. Therefore, we evaluated the state-of-the-art GNN-RE [2] for the task of classification of approximate adder circuits. While classification accuracy for exact adder circuits is on average 98%, once it was used for classification of approximate adder circuits, it reports an accuracy as low as 0%. Figure 2 further demonstrates this loss of performance and shows the relation between the aggressiveness of the approximation and the corresponding classification accuracy. The higher the aggressiveness in the approximation, the smaller individual circuits become and the more area is saved in the final integrated circuit [19]. At the same time, the loss in GNN classification accuracy becomes larger with increasing approximation aggressiveness.

Research Challenges: The discussion and experimental analysis above demonstrate that performing functional RE on approximate circuits is still an open research problem that imposes the following key research challenges.

1.2 Our Novel Concept and Contributions

To address the above challenges, we propose the AppGNN platform that extends GNN-based functional RE to allow for the accurate classification of approximated circuits, all while training on exact circuits. Based on the fact that GNN-based RE relies on the structural properties of a circuit, we implement a novel graph-based sampling approach in AppGNN that can mimic a generic approximation of any design, in terms of structure, requiring zero knowledge of the targeted approximation type and its aggressiveness. Our platform operates on flattened (i.e., without hierarchy) gate-level netlists and automatically identifies the boundaries between sub-circuits and classifies the sub-circuits based on their functionalities, whether the designs are approximate or not (see Figure 3).

![Figure 3. AppGNN approximation-aware node-level classification. Individual nodes in a given gate-level netlist are classified according to their role in a sub-circuit.](image)

The novel contributions of this work are as follows:

1. A comprehensive security analysis (Section 3.2) is provided. To the best of our knowledge, we are the first to investigate the resilience of AxC to functional RE.
2. An GNN-based functional RE platform (Section 3.3) is developed. Our AppGNN approach does not rely on the exact matching of sub-circuits to a preexisting library, making it much more flexible in classifying AxCs.
3. A novel graph-based sampling method (Section 3.4) is proposed. Our AppGNN methodology mimics common adder approximation methods, on the graph-level, in order to improve the classification accuracy.
4. Our AppGNN framework is publicly available to the scientific community under: https://github.com/ML-CAD/AppGNN

Key results: We perform an extensive experimental evaluation of AppGNN and GNN-RE [2] on various types of approximate circuits. We show that GNN-RE fails to reliably classify approximate circuits and that this failure is proportional to the aggressiveness of the approximation. To this end, we evaluate state-of-the-art
GNN-RE and our AppGNN on the EvoApprox approximate adders and multiplier circuits [19], as well as various bit-width variations of Almost Correct Adder (ACA) [25], Error-Tolerant Adder I (ETA-I) [30], Lower-part OR Adder (LOA) [17], Lower-part Copy Adder (LCA) [11], Lower-part Truncation Adder (LTA), Leading one Bit based Approximate (LoBA) multiplier [9] and Rounding-based Approximate (RoBA) multiplier [26], all of which are described in detail in Section 2.1. Over all these extensive datasets, our approach achieves an improvement in classification of approximate adders and multipliers of up to 28 percent points compared to GNN-RE, reaching a classification accuracy of up to 100% for some circuits.

2 BACKGROUND AND RELATED WORK

In this section, we present a brief introduction to AxC along with the datasets used in this work. We will also explain the underlying principles of GNNs and functional RE.

2.1 Approximate Computing (AxC)

AxC is established as a new paradigm to boost design efficiency by trading the intrinsic error resiliency of several applications such as signal, image, video processing [20] and ML [7, 28]. Driven by the high potential for energy savings, designing approximate functional units has attracted significant research interest [29]. In the following, we review approximate adder and multiplier functional units that we employ in this work as a case study. It is noteworthy that our work is not limited to certain type of approximate circuits.

2.1.1 Approximate Adders (AxAs). AxAs can generally be classified as (i) Lower-Part Adders (LPA) with low-magnitude frequent errors, (ii) Block-based Speculative Adders (BSA), which result in high-magnitude infrequent errors, and (iii) Evolutionary Approximate (EvoApprox) circuits generated using evolutionary algorithms.

Lower-Part Adders (LPAs). LPAs split their operation into an exact part with \( w - k \) Most Significant Bits (MSBs) and an approximate part with \( k \) Least Significant Bits (LSBs), where \( w \) is the bitwidth and \( k \) is the approximation level. The higher \( k \), the higher the errors in the LPA class. In this work, we consider the following LPAs:

- LTA which truncates \( k \) LSBs of the output with logic 0.
- LCA [11] copies the \( k \) LSBs of an operand to the \( k \) output LSBs.
- LOA [17] attributes a bitwise OR logic of the \( k \) LSBs operands to the \( k \) output LSBs.
- ETA-I [30] performs a carry-less sum with a bitwise XOR of the operands (i.e., a propagate operation). To compensate for the missing carry, if a carry-generate (i.e., a bitwise AND of the operands) is true in a bit of the approximate part, the previous output LSBs are set to 1. An OR-logic chain propagates the set-to-one command from the generate position up to the LSB.

Block-based Speculative Adders (BSA). BSAs split their operation into blocks of \( m \) width, where \( m \) is related to the approximation level. The higher \( m \), the lower are the errors and the benefits of the BSAs class. In this paper, we consider the following BSA.

ACA [25] implements \( m \)-bit overlapping blocks to speculate the carry operation. ACA generates exact output values for the first \( m \) LSBs. Each output bit at the position \( m \) up to the MSB is independently generated by overlapping adder blocks that speculate \( m \) bits of the operands.

2.1.2 Approximate Multipliers (AxMs). AxMs are commonly designed by (i) mathematically refactoring the multiplication for eliminating parts of its equation and (ii) detecting the Leading One Bit (LOB) position of the operands for discarding the hardware that computes unnecessary leading zeros and (iii) truncating part of the LSBs. We employ the following multipliers that comprehend these strategies as case studies in this work.

- RoBA multiplier [26] simplifies the multiplication process by using numbers equal two to a power \( n (2^n) \). The multiplication is factored as \( A \times B = (A_r - A)(B_r - B) + A_rB + AB_r - A_rB_r \). Then, the \( A_rB, A_rB_r \) and \( AB_r \) sub-expressions are approximated by simple shift operations. Thus, the multiplication is simplified for \( A \times B \approx A_rB + AB_r - A_rB_r \). A sweep process in the operands bits finds the nearest value of \( A_r \) and \( B_r \). The \( A_r[i] \) is logic 1 in two cases. In the first case, \( A[i] \) is set to logic 1, and all the bits on its left side are logic 0 while \( A[i - 1] \) is logic 0. In the second case, when \( A[i] \) and all its left-side bits are logic 0, \( A[i - 1] \) and \( A[i - 2] \) are both logic 1. The circuit employs \( B_r \) by the same process of \( A_r \).
- LoBA multiplier [9] splits the multiplication in smaller fixed-width multiplier blocks. LoBA multiplier identifies the LOB position and defines two \( k \)-bit new operands \( A_{\text{LoA}} \) and \( B_{\text{LoA}} \), which are multiplied and shifted left based on the LOB position. It multiplies the higher \( k \)-bit part of the operands starting from the LOB position suppressing leading zeros and truncating the lower part operators. Therefore, LoBA reduces the length of the multiplication to just \( k \) bits. We refer as LoBA the LoBA0 configuration in [9].

2.1.3 Evolutionary-based Approximate (EvoApprox). EvoApprox adder and multiplier circuits are automatically generated by a genetic algorithm, a method inspired by natural selection that mimics biological evolution [19]. EvoApprox circuits are created by an extensive design exploration which evolves strong candidates and discards weak generations of circuits with a given error metric. We employ the EvoApprox library made available online by [19].

2.2 Graph Neural Networks (GNNs)

GNNs perform graph-representation learning on graph-structured data and generate a vector representation (i.e., embedding) for each node in a given graph to be used for a desired task such as node classification. The embeddings are generated based on the input features of the nodes and the underlying graph structure so that similar nodes in the graph are close in the embedding space.

Let \( G(V, E) \) denote a graph, where \( V \) represents its set of nodes, and \( E \) represents its set of edges. Each node in the graph \( v \in V \) is initialized with a feature vector \( x_v \) that captures its properties. In GNNs, typically an Aggregation function collects the node information from the direct neighborhood of node \( v \), denoted as \( N(v) \). An Update function updates the current embedding of node \( v \) by combining its previous state with the aggregated information. GNNs run such a neighborhood aggregation procedure for \( L \) rounds (increasing the depth of the aggregated information) [13].

GNNs mainly differ based on the Aggregation and Update functions used. The fundamental Graph Attention Network (GAT) [23] measures the importance (weight) of the edges during the aggregation phase. It employs a multi-head attention mechanism of \( K \), in...
Figure 4. AppGNN work flow. Exact gate-level netlists are transformed into a graph representation. Node sampling is performed on the graph-level before the sampled graph is added to the training dataset and for the GNN to perform training.

which the layer \( l - 1 \)'s information propagates to layer \( l \) as follows;

\[
h^{l}_{0} = \sigma \left( \sum_{u \in N(v)} a^{k}_{u,v} W^{k} h^{l-1}_{u} \right)
\]

(1)

\[
a^{k}_{u,v} = \text{LeakyReLU} \left( (a^{k}) \gamma [W^{k} h^{u} \| W^{k} h^{v}] \right)
\]

(2)

Where \( h^{l}_{0} \) denotes the generated embedding of node \( v \) at the \( l^{th} \) round, \( h^{0}_{0} = x_{v} \), and \( \sigma(\cdot) \) is a non-linear activation function (e.g., ReLU). \( a^{k}_{u,v} \) specifies the weighting factor (i.e., importance) of node \( u \)'s features for node \( v \), which is computed as a byproduct of an attention mechanism \( a \). The multi-head attention mechanism replicates the aggregation layers \( K \) times, each replica having different trainable parameters \( W^{k} \), and the outputs are feature-wise aggregated using a concatenation operation as described in Equation (1). The final embedding vector of node \( v \), after \( L \) layers, is as follows:

\[
z_{v} = h^{L}_{0}
\]

(3)

2.3 Functional Reverse Engineering (RE)

Without access to the RTL design of a circuit, functional RE is one option to gain further detailed insight on the functions that are implemented inside a circuit. However, gate-level netlists are inherently difficult to analyze, since structural information about the function and boundaries of sub-circuits is usually omitted during the synthesis process. This leaves only the high-level circuit description and list of gates and their interconnections to be analyzed. Therefore, automated algorithmic analysis tools, such as [21], have been introduced. Their functionality is based on partitioning the gate-level netlist by identifying replicated bit slices and, in turn, aggregating them into individual candidate modules. Afterwards, using formal verification methods, these candidate modules are matched against a "golden" component library containing reference circuits in order to infer their high-level functionality, e.g. adder, multiplier, subtractor, etc [10, 15, 16, 21].

A shortcoming of pattern matching approaches like these is that they are extremely dependant on the quality and size of the "golden" component library that is used. Due to this, components that differ from the ‘standard’ implementation, for instance of an adder circuit, will not be classified correctly and may remain undetected [2]. Additionally, formal verification methods can be very resource demanding in terms of compute power, limiting their applicability. Therefore, other methods have been proposed in literature.

Recently, ML-based methods have shown great potential [2], achieving high classification accuracy at only a one-time training effort. In GNN-RE, the gate-level netlist of a circuit is first transformed into a graph representation. The graph representation preserves the structure of the netlist, captures the features of each gate (for instance gate type, number of inputs/outputs, etc.) and also encodes the neighborhood of each gate. This way, the graph representation encodes both the structural and functional attributes of each node and it’s surrounding circuitry. Then, GNN-RE employs a GNN to learn on the graph representation of the circuit to predict the sub-circuit each gate belongs to (i.e., node classification task).

In any GNN implementation, the quality of the model depends on the quality of the training data set that is used as a ground truth. Including a wide range of different implementations and bit-widths for each high-level component (e.g. adder, multiplier, etc.), the ML model can learn to generalize and become robust to variations.

Functional RE can be very helpful to various entities such as IC designers to verify to correctness of a chip. For instance, using functional RE, Hardware Trojans (HTs) or Intellectual Property (IP) infringements in competitor products can be detected [3, 6, 8]. On the flipside, functional RE can potentially also be abused to gain insights into patented designs and steal IP [18].

3 OUR PROPOSED GNN-BASED REVERSE ENGINEERING: APPGNN

In the following, we describe our concept of AppGNN. We first cover the assumptions that we make. Then, we explain the graph representation for our GNN model, the datasets that we use for training and finally demonstrate our node sampling techniques.

The overall work flow of AppGNN is illustrated in Figure 4. We start in step ① with a gate-level netlist, which is transformed into a graph (Section 3.3) and abstracted in steps ② and ③. In step ④, we perform node sampling using either random node sampling (Section 3.4.1) or leaf node sampling (Section 3.4.2). In final step ⑤, the sampled graph is added to the training dataset (Section 3.6).
3.1 Threat Model and Assumptions

We perform functional RE on AxCs under the following assumptions, which are consistent with prior work [2, 3, 6, 8, 10, 15, 16, 21]. We assume that the gate-level netlist of the design that is being analyzed has been correctly retrieved, either by deriving it from the physical chip [22] or by other means (e.g., access to layout information). In particular, access to the RTL source code of the design is not available. We make no assumptions about the given netlists that are analyzed. In particular, we do not assume any knowledge about the used approximation technique or the aggressiveness of the approximation. In fact, we do not assume it to be an approximate circuit at all. This allows us to develop a generic approach and to operate on exact circuits as well as approximate ones.

3.2 Why do Approximate Circuits Appear to be Reverse-Engineering Resilient?

Approximate circuits can differ substantially from their exact counterparts in terms of their general graph structure, gate count and gate type. As an example, Figure 5 illustrates the graph representation of two 12-bit adder circuits. In the figure, (a) displays the connectivity of the individual gates of an exact adder circuit, (b) displays this for an AxC adder that has been generated using LCA [11]. Six of the twelve primary outputs are approximated (copied directly from the input to the output). As the figure illustrates, the graph structure of both circuits and their node count is dissimilar.

In addition to the graph structure and gate count being different, the type of used gates in both circuits varies as well, as Figure 6 shows. It can be seen from the figure that some gate types appear exclusively in one of either circuits, such as CLKBUF, OAI21 (Or-And-Invert) and XOR2 which only appear in the exact implementation.

Table 2. The datasets used in the training of AppGNN

| Datasets          | #Nodes | #Circuits | Source                             |
|-------------------|--------|-----------|-----------------------------------|
| Add-Mul-Mux       | 15,582 | 7         | GNN-RE [2]                        |
| Add-Mul-Mux       | 21,602 | 6         |                                   |
| Add-Mul-Combine   | 14,288 | 6         |                                   |
| Add-Mul-All       | 51,472 | 19        |                                   |
| Add-Mul-Comp      | 15,898 | 6         |                                   |
| Add-Mul-Sub       | 18,206 | 6         |                                   |
| Add-Mul-Comp-Sub  | 19,151 | 6         |                                   |
| Adder 9bit        | 469    | 8         | This work (AppGNN)                |
| Adder 12bit       | 792    | 9         |                                   |
| Adder 16bit       | 981    | 9         |                                   |
| LTA               | 2028   | 28        |                                   |
| ACA [25] adder    | 2618   | 28        |                                   |
| LOTA [30] adder   | 2282   | 28        |                                   |
| LCA [11] adder    | 2210   | 28        |                                   |
| LTA               | 2028   | 28        |                                   |
| EvoApprox-Add [19]| 9981   | 214       |                                   |
| EvoApprox-Mul [19]| 78155  | 159       |                                   |
| Exact circuit     | 467    | 5         |                                   |
| Exact circuit     | 13701  | 6         |                                   |

Table 3. Adders and multipliers in our evaluation dataset

| Evaluation dataset | Circuit type | #Nodes | #Circuits |
|--------------------|--------------|--------|-----------|
| ACA [25] adder     | 2618         | 28     |           |
| LOTA [30] adder    | 2282         | 28     |           |
| LCA [11] adder     | 2210         | 28     |           |
| LTA                | 2028         | 28     |           |
| EvoApprox-Add [19] | 9981         | 214    |           |
| LoBa [9] multiplier| 43694        | 31     |           |
| RoBa [26] multiplier| 31077       | 5      |           |
| EvoApprox-Mul [19] | 78155        | 159    |           |
| Exact circuit      | 467          | 5      |           |
| Exact circuit      | 13701        | 6      |           |

Figure 6. Histogram of the occurrence of individual gate types in a 12-bit exact adder implementation and a LCA-based 12-bit AxC adder circuit.

Figure 7. Node-level classification accuracy on the EvoApprox [19] adders dataset of GNN-RE and when the LTA dataset of approximate adders is included in the training.
whether gates are Primary Inputs (PI) or Primary Outputs (PO) or
(wires) between individual gates/nodes. This transformation from
a netlist to a graph will retain all structural information present
in the netlist, e.g. the connectivity between individual gates will
be represented using an adjacency matrix. In order to retain infor-
mation about the individual gates, such as the gate type (e.g. XOR),
whether gates are Primary Inputs (PI) or Primary Outputs (PO) or
the input and output degree, each node will keep a reference to a
feature vector \( x \) with length \( k \) describing these details. The length
of \( k \) is largely determined by the number of available gate types in
the used technology library\(^1\), in our case \( k = 24 \).

Figure 8 shows an example of a netlist that contains various
gate types. In this example, node \( g \) is a primary output (since it is
a leaf node) which is captured in the first two fields of the feature
vector \( x_g \) (Ports section in Figure 8). The feature vector also contains
information about the gate type of \( g \) (XOR) as well as the gate
types and number of occurrences of other gates present in the two-
hop neighborhood\(^2\) of \( g \). In this example, the 2-hop neighborhood
contains two NAND, two XOR, one NOR and one INV gate. This
neighborhood information is stored in the following fields of \( x_g \)
(Neighborhood section in Figure 8). The last two fields (Structure
section in Figure 8) capture the input (2) and output (1) degree of \( g \).

A feature matrix \( X \in \mathbb{R}^{n \times k} \), with \( n \) describing the total number
of nodes, will aggregate the feature vectors of all nodes. The feature
matrix \( X \) is then standardized by removing the mean and scaled
to unit variance. Such a representation of node features has been
found efficient in other works \([1, 2]\).

Next, we describe two node sampling methods that aim to mimic
a generic approximation technique.

### 3.4 Node Sampling

As described in Section 3.2, the structure of approximate circuits
can differ substantially from an exact implementation. However,
there are typically fewer nodes and connections in an approximate
circuit. Our approach aims to exploit this observation by mimicking
a generic approximation constructed from an exact circuit.

In the following, we describe two node sampling methods which
remove individual nodes and all transient inputs to this node (the
datapath of the node). The number of initially selected nodes (for
removal) relates to the level of the approximation. Selecting a large
number of initial nodes for removal thus corresponds to a high
level approximation, while selecting only a few initial nodes relates
to a lower level of approximation. In the following examples, we
demonstrate two approaches: (i) random node sampling and (ii) leaf
cnode sampling. We illustrate these methods on a simple 3-bit adder
circuit. Note that 3-bit adder circuits are not included in the actual
AppGNN dataset and this is for demonstrative purposes only.

\(^1\)In our experiments, a 14nm FinFET library containing 24 individual gates was used.

\(^2\)The two-hop neighborhood of a node \( g \) includes all nodes directly adjacent to \( g \) and
all nodes that in turn are adjacent to these nodes.

#### 3.4.1 Random Node Sampling

We select a number of nodes for removal based on the desired level of approximation. In this example, we are randomly selecting a single node. We then identify the datapath of this node and remove all found nodes (including the initially selected node) from the graph. We now describe this process in detail, which is also displayed in Figure 9.

We start with a directed graph that is constructed from a gate-
level netlist according to Section 3.3 (Step 1). Then, we randomly
select a node in the graph for removal. U17 (in red) is selected
in this example (Step 2). In order to mimic approximation, we
identify the datapath of the selected node using Algorithm 1. The
identified nodes, including the initially selected one, will be marked
for removal (Step 3). Finally, all found nodes are removed from the
data path (Step 4) using Algorithm 2. Depending on the chosen node,
the remaining subgraphs can differ substantially. In the example
shown in Figure 9, node U17 is selected and four additional nodes
are identified as the datapath of U17. If node U20 had been chosen
instead of U17, only this node would be removed since the datapath
is empty as it is a root node.

#### 3.4.2 Leaf Node Sampling

In contrast to the random node sampling technique previously described, we will now explain our leaf node sampling technique. This method is closer to actual approximation since it takes the role of primary outputs (leaf nodes in the graph representation) into account. Depending on the desired level of approximation, this method will select a number of leaf nodes for removal. Leaf nodes in a graph are identified using Algorithm 3. The entire sampling process is displayed in Figure 10 and is described in the following.

Similar to the random node sampling technique, we start with a
directed graph that is constructed from a gate-level netlist in a way
according to Section 3.3 (Step 1). Next, all leaf nodes that are
present in the graph are identified using Algorithm 3 (Step 2).
Depending on the desired level of approximation, a number
of identified leaf nodes are selected for removal (Step 3). In this example, only one node (U19, in red) is selected. Thereafter, the datapath(s) of the previously selected leaf node(s) are identified using Algorithm 1 and all found nodes are marked for removal. Finally, all previously marked nodes are removed from the graph (Step 4) using Algorithm 2. Since leaf nodes (which correspond to primary outputs) have been removed, their datapath is replaced with a single new node. This is to ensure that the resulting graph has the same number of leafs as before and to retain more of the original graph structure. The feature vector $x$ associated with this node will capture that this node is a primary input and a primary output (it redirects all input directly to the output), that the input and output degree are both be one and that the gate type is $BUF$.

Algorithm 1 Find all nodes in the datapath of a node

**Input:** Graph $G(V, E)$; current node $c \in V$; empty list $N_{DP}$

**Output:** a set of nodes $N_{DP} \subseteq V$

1: procedure FINDDATA_PATH
2: $N_{pre} \leftarrow$ predecessors($G, c$)
3: if $c \in N_{pre}$ then
4: $N_{pre}.remove(c)$  // Avoid loops
5: for $v \in N_{pre}$ do
6: if $v \notin N_{DP}$ then
7: FINDDATA_PATH($G, v, N_{DP}$)  // Recursively find nodes
8: if outputDegree($c$) = 1 then
9: $N_{DP}.append(c)$  // $c$ is exclusive to this path
10: return $N_{DP}$

Algorithm 2 Graph sampling

**Input:** Graph $G(V, E)$; nodes to remove $N_r \subseteq V$

**Output:** Sampled graph $G'(V', E')$

1: procedure SAMPLE_GRAPH
2: nodesToDrop $\leftarrow$ \{\}
3: for $i \in N_r$ do
4: $dataPath \leftarrow$ FindDataPath($G, i, \{\})$
5: nodesToDrop.append(dataPath)
6: $G' \leftarrow G.removeNodes(nodesToDrop)$
7: return $G'$

Algorithm 3 Identify leaf nodes

**Input:** Graph $G(V, E)$

**Output:** A set of nodes $L \subseteq V$

1: procedure IDENTIFY_LEAF_NODES
2: $L \leftarrow$ \{
3: for $v \in V$ do
4: if outputDegree($o$) = 0 then
5: $L.append(o)$
6: return $L$

3.5 GNN Model

We employ the fundamental GAT architecture described in Section 2.2 to perform node classification. We further utilize the node sampling approach, GraphSAINT [27], to maintain scalability, as suggested in [2]. The GraphSAINT approach samples sub-graphs from the original input graph, and a full GNN is constructed for each extracted sub-graph. We employ two GAT aggregation layers with a hidden dimension of 256 each and ReLU activation function. For the attention mechanism, $K = 8$. The final layer is a fully-connected layer of size 5 with a Softmax activation function for classification. The GNN is trained using the Adam optimization algorithm, with an initial learning rate of 0.01 and a dropout rate of 0.1.

3.6 Dataset Generation

In order to improve the classification accuracy of the GNN on approximate circuits, we extend the training dataset. We do so by adding 35 exact adder circuits of varying bit-widths (see Table 2). After these circuits are converted into their graph representation, as described in Section 3.3, they are passed through the node sampling stage, as described in Section 3.4. During this stage, either random sampling or leaf node sampling is performed. For each bit-width of the exact adders (8, 9, 12 and 16), 9 sampled graphs (8 for the 8bit adder) with increasing approximation aggressiveness are retrieved. This means that 1 to 9 nodes of a original graph are selected for removal (including their datapath).

An overview over the training dataset used in AppGNN can be found in Table 2. For the training process, this dataset is split as follows: 65% for training, 25% for validation and 15% for testing. In the following, we show the evaluation of our AppGNN approach.

4 EXPERIMENTAL OVERVIEW

We evaluate AppGNN on the AxC dataset shown in Table 3. We compare the node-level classification accuracy of AppGNN to that of GNN-RE [2], which serves as a baseline. All datasets consist flat gate-level netlists that are synthesized from their RTL description using Synopsys Design Compiler [14] using the compile_ultra directive while performing area optimization. The designs are synthesized using a 14nm FinFET technology library. The conversion from netlist to the graph representation is implemented in Perl and Python3. Our node sampling methods are also implemented in Python3. Training is carried out on a single computer with 16 cores (Intel Core i7-10700 CPU @ 2.90GHz) and 32GB of DDR4 RAM.

We employ the random walk sampler of GraphSAINT with a walk depth of 2 and 3000 root nodes. We run training for 100 epochs. The GNN model is evaluated on the graphs in the validation set after each epoch. The best-performing model on the validation set is restored at the end of training and subsequently used to evaluate the GNN on the testing set.

4.1 Results

Our results are presented in the following. Figure 11 shows the classification accuracy of AppGNN and GNN-RE [2], which serves as a baseline, for all classes of AxC adders in Table 3. In each figure, the X-axis displays the normalized circuit area and thus is related to the level of approximation (which increases from left-to-right on the X-axis). Figure 12 summarizes these results and displays the average classification accuracy of GNN-RE and AppGNN.

Comparison to GNN-RE. As Figure 11 demonstrates, AppGNN outperforms GNN-RE in all benchmarks, regardless of the used sampling method or type of approximation. Except for very high levels of approximation in LOA-based circuits (Figure 11 (c)) when using random node sampling. Here, AppGNN performs circa 8 percentage points worse than GNN-RE. However, AppGNN with leaf node
sampling still performs better than GNN-RE in this benchmark. It is noteworthy that, in the case of ACA (Figure 11(a)) and EvoApprox adders (Figure 11(f)) benchmarks, AppGNN with leaf node sampling performs better with an increase of approximation aggressiveness.

On average, AppGNN outperforms GNN-RE on all types of approximate adder circuits as Figure 12 shows. The smallest gains in classification accuracy are achieved on the ACA based circuits with 8.8 percentage points compared to GNN-RE, which already performs well on this type of circuit. The largest gains can be seen in the EvoApprox adder dataset. Here, AppGNN outperforms GNN-RE by 28 percentage points.

**Effect of the AxA Type.** With up to 91% classification accuracy, AppGNN performs best on LTA based circuits. This is not a surprising finding; LTA and LCA based circuits are implemented by either truncating m input bits of the operands (LTA) and feeding the output with logical zeroes, or by copying (LCA) m bits of an input operand to the output. In our graph representation, this architecture leads to many isolated nodes (nodes that are both PIs and POs and no adjacent nodes). Our node sampling methods produce graphs that are structurally similar to these, thus allowing AppGNN to classify them more accurately. Simultaneously, the classification accuracy of AppGNN on exact adder circuits is comparable to that of GNN-RE, as Figure 12 shows. Only a negligible difference of up to 1.3 percentage points is observed.

**Effect of the AxM Type.** Figure 13 illustrates the classification accuracy of GNN-RE and AppGNN on multiplier circuits. In general, GNN-RE does not suffer the same accuracy loss when classifying approximate multipliers as seen in approximate adders. Although AppGNN was not specifically designed to improve the classification accuracy in approximate multipliers, it still manages to outperform GNN-RE by 3.7 percentage points on ROBA based multipliers as Figure 13 shows. On the LOBA dataset, GNN-RE and AppGNN are on a par with each other, only a negligible difference in classification accuracy can be observed. However, in the case of EvoApprox multipliers, AppGNN suffers significantly. Here, the approximation-unaware GNN-RE actually outperforms AppGNN by 14.2 percentage points. Lastly, the evaluation shows that AppGNN performs similar to GNN-RE when classifying accurate multiplier circuits. A difference of up to 1.4 percentage points can be observed.

**Effect of the Aggressiveness of the Approximation.** As Figure 11 demonstrates, the classification accuracy of GNN-RE significantly drops with an increase of approximation aggressiveness with the exception of ACA and LOA based circuits. Although a similar trend is observable in the results of AppGNN, it is typically much weaker or even reversed, i.e. in EvoApprox adders (Figure 11(f)).

Figure 11. Classification accuracy of GNN-RE [2] and AppGNN with random node sampling and with leaf node sampling. The X-axis is the normalized circuit area. A small circuit area correlates with a high approximation aggressiveness, thus the level of approximation increases from left-to-right in each plot.

Figure 12. Average classification accuracy of GNN-RE [2] and AppGNN with random node sampling and with leaf node sampling for all evaluated classes of adder circuits.

Figure 13. Average classification accuracy of GNN-RE [2] and AppGNN with random node sampling and with leaf node sampling for all evaluated classes of multiplier circuits.

5 CONCLUSION

In this work, we investigated the impact of Approximate Computing (AxC) on functional Reverse Engineering (RE). To the best of our knowledge, this is the first time such an investigation is performed. We demonstrated that traditional means of functional RE are insufficient in the context of AxC. Although Machine Learning (ML)-based methods can handle some variation in the circuit and still provide reasonable results, with an increase of approximation aggressiveness their classification accuracy declines rapidly. We proposed a method for approximation-aware functional RE using Graph Neural Networks (GNNs). Our presented graph sampling based methods aim to mimic the structure of a generic approximation method in order to make a GNN aware of approximation. We evaluated our approach on a wide range of different datasets to show the improved classification accuracy of AppGNN against state-of-the-art GNN-RE. Our extensive evaluation demonstrated how AppGNN outperforms the GNN-RE method in almost all cases.

ACKNOWLEDGEMENTS

This work was supported in part by the German Research Foundation (DFG) through the Project “Approximate Computing aCROSS the System Stack (ACCROSS)” AM 534/3-1, under Grant 428566201.
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