A differential memristive synapse circuit for on-line learning in neuromorphic computing systems

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Abstract. Spike-based learning with memristive devices in neuromorphic computing architectures typically uses learning circuits that require overlapping pulses from pre- and post-synaptic nodes. This imposes severe constraints on the length of the pulses transmitted in the network, and on the network’s throughput. Furthermore, most of these circuits do not decouple the currents flowing through memristive devices from the one stimulating the target neuron. This can be a problem when using devices with high conductance values, because of the resulting large currents. In this paper we propose a novel circuit that decouples the current produced by the memristive device from the one used to stimulate the post-synaptic neuron, by using a novel differential scheme based on the Gilbert normalizer circuit. We show how this circuit is useful for reducing the effect of variability in the memristive devices, and how it is ideally suited for spike-based learning mechanisms that do not require overlapping pre- and post-synaptic pulses. We demonstrate the features of the proposed synapse circuit with SPICE simulations, and validate its learning properties with high-level behavioral network simulations which use a stochastic gradient descent learning rule in two classification tasks.

1. Introduction

Neuromorphic computing systems typically comprise neuron and synapse circuits arranged in a massively parallel manner to support the emulation of large-scale spiking neural networks [3, 10, 21, 23, 28, 31, 36, 42]. In these systems, the bulk of the silicon real-estate is taken up by synaptic circuits, where the memory and computational sites are co-localized [23]. Consequently, to save area and maximize density, many neuromorphic computing approaches avoid implementing complex synaptic circuits with on-chip learning mechanisms [28, 32, 41], and resort to training the network on external computers. However, these approaches lose the ability to execute on-line “life-long” learning and require that the network parameters (such as the synaptic weights) be programmed at deployment time. In addition, if these parameters are stored in Static Random Access Memory (SRAM) cells or in Dynamic Random Access Memory (DRAM) banks, they need to be re-programmed every time the system is
reset. For large networks [15, 28, 44], the time required to initialize the system with these parameters can become prohibitive.

Memristive devices can potentially address these problems by virtue of their compactness and non-volatility [22]. Given their advantages, several neuromorphic arrays that use memristive devices have been proposed [25, 30, 39, 40, 48]. Typically, these approaches propose to use memristive devices in dense synaptic arrays for implementing large-scale neural networks. For instance, [37, 40] describe use of 1R arrays to implement perceptrons trained by supervised learning protocols such as [45]. Similarly, in [50], the authors train a 1T-1R array to implement perceptrons classifying face images from the Yale face database [17]. In [14], the authors use the Recursive Least-Squares (RLS) algorithm for training synaptic weights to perform complex tasks such as human motor control. In works such as [14, 40], the authors propose the use of two devices per synaptic element to implement positive and negative weight terms. Other approaches describe synaptic arrays with a 1T-1R synapse elements that learn using classical [11, 16, 39, 43, 48] or stochastic [4, 30, 46] Spike-Timing Dependent Plasticity (STDP) learning rules. In these arrays the currents used to program the memristive devices can be very large, especially for devices in high-conductance states. This imposes severe restrictions on the power budget, capacitor sizes, and other aspects for the design of ultra-low power memristive-neuromorphic circuits. Moreover, the learning protocols employed in most of these architectures couple the length of the pulses used to transmit signals across the layers of the network with the duration of the pulses required to program the devices [16, 39]. This requirement imposes severe constraints on the maximum data throughput of the network, because each row or column in the cross-bar array has to wait for the pre- and post-synaptic pulses to finish, before a new one can be sent. In this paper we propose a novel synaptic circuit that addresses at the same time both the large current and overlapping pulses problems. To overcome the problem of integrating large currents in the post-synaptic neuron, we propose a novel differential-mode sub-threshold memristive synapse circuit that decouples, normalizes, and re-scales the memristive device current from the one supplied to the post-synaptic neuron. To overcome the problem of overlapping pulses in cross-bar architectures, we propose an event-based scheme that decouples the duration of the input spikes from the read and update phases of the target synapse, coupled with the use of a novel spike-based synaptic update mechanism.

In recent years, several algorithms employing spike-triggered learning based on post-synaptic neuronal activity, instead of vanilla STDP mechanisms, have been proposed in computational neuroscience literature [6, 20, 49]. Several neuromorphic implementations of these mechanisms have also been realized [19, 21, 31, 33, 42]. In this paper, we demonstrate how the proposed differential memristive synapse circuit can be incorporated in a neuromorphic system that employs a learning circuit based on such ideas. This circuit is inspired by the biologically plausible learning rule presented in [49] and gradient-descent based methods applied to memristive devices [35, 47]. We use these learning circuits to implement a randomized unregulated step descent algorithm,
Figure 1: Multi-neuron chip architecture: input AER events are converted into read and write pulses sent to multiple memristive synapses; the currents produced by the synaptic circuits are integrated by the neuron assigned for the row; output spikes are converted into AER events and transmitted off-chip.

Figure 2: Pulse-shaping circuit for creating a sequence of Read and Write pulses, with each AER input event.

which has been shown to be effective for synaptic elements with limited precision [34].

In the following Section, we present the network architecture that is compatible with the proposed differential memristive synapse circuit. In Section 3 we describe the techniques used for sensing and changing the memristive device conductances, and present circuit simulation results that quantify its performance figures. In Section 4, we assess the features of neuromorphic architectures that make use of the proposed circuits and validate them with behavioral simulations in a binary classification task. Finally, in the Supplementary material we present extensions and variants to the proposed differential synapse memory cell, including their use in dense 1T-1R cross-bar arrays.

2. Neuromorphic architectures for memristive synapses

The architecture we propose is composed of an array of synapses and neurons that receive input spikes into columns of synaptic cells, and produce output spikes from the silicon neurons arranged in rows (see Fig. 1). This type of architecture can be integrated within a full-custom neuromorphic Very Large Scale Integration (VLSI) chip, or be used as a single-core in multi-core neuromorphic systems [28, 32]. Both the input and output spikes are represented by fast digital pulses that are encoded using the AER [5, 9, 12, 29].
Figure 3: Memristive synapse circuits for on-line learning in a neuromorphic architecture.

On the input side, asynchronous AER circuits ensure that events are transmitted as they arrive. Upon the arrival of a pre-synaptic address-event a pulse-shaping circuit decouples the duration of the input spikes from the read and update phases of the target synapse. This frees the communication bus to transmit spikes from sender nodes to the cross-bar array, increasing the throughput of the network by use of shared or time-multiplexed communication resources. The block diagram describing the operation of the pulse-shaping circuits is shown in Fig. 2. The pulse-shaping circuit consists of two pulse-extender circuits [42] and is configured to produce two pulses in quick succession on the arrival of an AER event. These pulses sequentially enable the read-mode operation, where the state of the addressed synapse is sensed, followed by the write-mode operation, where the state of the memristive devices are increased or decreased, in the targetted synapse. The write-mode operation is directed by the UP and DN control signals produced by the learning circuits in the post-synaptic neuron.

On the output side a 1-D arbiter circuit enqueues output events in case of collisions and transmits them on the shared output bus [5]. A programmable bias-generator circuit [13] provides a set of globally-shared temperature-compensated current signals for biasing the analog parameters of the neuromorphic circuits, such as time-constants, refractory periods, or learning rates.

Address-events target destination columns of the memristive array. By construction, all rows of the stimulated column will process the input event in parallel. Furthermore, the extended read and write pulses typically last longer than the input AER event duration. Therefore, a sequential AER stimulation of multiple columns will produce multiple read/write operations across the full array that will overlap in time and operate in parallel. A block diagram of the circuits present in a single row of the cross-bar architecture illustrated in Fig. 1 is shown in Fig. 3. It comprises multiple synaptic circuits that receive the voltage pulses from the pulse-shaping circuits, two current-mode Differential Pair Integrator (DPI) circuits that emulate excitatory and inhibitory synapse dynamics with biologically realistic time constants [1, 2], a current-mode learning block that implements a spike-driven learning mechanism [31, 42], and an ultra-low-power adaptive Integrate-and-Fire (I&F) neuron circuit that faithfully reproduces biologically realistic neural dynamics [24, 27]. In the read-phase, the synaptic circuit senses the state of the two memristive devices in it, and produces rescaled and normalized differential currents that are driven into the positive and negative DPI inputs. The DPI circuits
integrate these weighted currents and generate a rescaled output current that is driven into a neuron and its learning block. The learning block uses a copy of this “dendritic” current to compare it to the net input current, which includes contributions from the neuron and an external source. The external source could represent a teacher signal in supervised learning protocols, or contributions from other neurons in unsupervised learning protocols. Based on this comparison, the learning block evaluates an error signal and produces the UP and DN weight update control signals that are used during the write-mode phase to increase or decrease the weights of the stimulated target synapse. We demonstrate the operation of this architecture with a concrete example in Section 4.

3. The differential memristive synapse circuit

The differential memristive synapse circuit is based on the classic Gilbert-normalizer element [18, 26], whose output currents, originally designed for bipolar transistors, but functional also for Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) operated in the sub-threshold domain [26]. The synapse circuit stores its weight as the difference between the conductances of two memristive devices, one representing a positive term and the other representing a negative term. Programming the devices is done in a push-pull manner: to increase the synaptic weight, the conductance of the positive term is increased, and that of the negative term is decreased. The complementary operation is achieved by simultaneously decreasing and increasing the conductances of the positive and negative terms, respectively. The output current produced by this circuit, in read-mode, can be scaled to very low values (e.g., in the range of pico Amperes). This reduces the total current driven into the post-synaptic neuron, which can then be implemented with very small capacitors and ultra-low power sub-threshold circuits. The differential operation coupled with the normalizing ability of the circuit has two additional advantages. It reduces the effect of memristive device variability and implements both positive (excitatory) and negative (inhibitory) synapse contributions, effectively doubling the “high-low” dynamic range of the synaptic weight. In write-mode, the circuit enables programming the memristive devices with programmable current limits, pulse widths, and heights. These can be chosen by the user to optimize the write-mode power consumption depending on the memristive device integrated in the circuit.

The operating principles of the circuit is independent of the memristive device technology used. It can be used in combination with a wide range of different resistive memory technologies, with arbitrary number of resistive stable states. In this work we assume our Complementary Metal-Oxide-Semiconductor (CMOS) circuits can be directly interfaced to $HfO_2$ based devices through post-processing methods, as described in [8].

The schematic diagram of the differential memristive synapse circuit is shown in Fig. 4. The circuit is used in a “read-mode” phase to measure the conductance of the two memristive devices produce scaled output currents that are conveyed to the
downstream current-mode neural processing circuits. It is then operated in a “write-mode” for updating the state of the memristive devices via the downstream learning circuit control signals. All $S_i$ MOSFETs represent switches, with gates controlled by digital signals. Signals with an overline, such as $\overline{X}$, represent the inverted version of the signal $X$. The signal $V_{\text{Read}}$ represents the digital voltage used during the read-mode, while the signals $V_{\text{Set}}$ and $V_{\text{Reset}}$ represent the digital set and reset pulses used in the write-mode to increase/decrease the synaptic weight. The signal $V_b$ is a sub-threshold bias voltage that sets the (sub-threshold) scale of the output currents. The MOSFETs $Sx$ have dimensions $W/L = 5\mu m/0.5\mu m$; MOSFETs $M1$ & $M4$ have $W/L = 1\mu m/2\mu m$, $M2$ & $M3$ have $W/L = 0.5\mu m/1\mu m$, and $M5$ $W/L = 2\mu m/1\mu m$.

3.1. Read-mode operation

To operate the circuit of Fig. 4 in read-mode, the switches $S1$, $S2$, $S7$, and $S8$ are turned on and all other switches are turned off; the digital control signals $V_{\text{set}}$ and $V_{\text{reset}}$ are set to logical zero. The current-mode normalizer circuit is implemented by MOSFETs $M1$-$M6$. In this mode of operation the memristive devices $D_{\text{pos}}$ and $D_{\text{neg}}$ are connected to corresponding $V_{\text{top}}$ and $V_{\text{bot}}$ nodes. When the $V_{\text{read}}$ pulse is active the currents flowing through the memristive devices are measured and the output currents, $I_{\text{pos}}$ and $I_{\text{neg}}$, are sent to the excitatory and inhibitory DPI circuits, respectively.

Therefore, in this mode of operation, during a $V_{\text{read}}$ pulse:

\[ I_{D_{\text{pos}}} = I_{M1} \quad \text{and} \quad I_{D_{\text{neg}}} = I_{M4} \]  \hfill (1)
where $I_{Dx}$ is the current through the device $D_x$, and $I_{Mi}$ is the current through the MOSFET $Mi$.

For low-power operation, it is desirable to make $I_{Dx}$ very small. Under this condition, we can assume that the transistors operate in sub-threshold domain. This allows us to analytically derive the relationship between the circuit parameters, and the current flowing through the circuit’s output branches. By writing the sub-threshold equations for a MOSFET and equating it to the currents through the resistive devices, we get:

\[
(V_{RD} - V_i) = R_x I_x
\]

\[I_{Mi} = I_0 e^{\frac{-V_i - V_s}{U_T}}
\]

\[I_x = I_{Mi}
\]

where $R_x$ represents the resistance of the memristive device $D_x$, $V_{RD}$ the supply voltage provided in “read-mode”, $V_s$ the source voltage of the input MOSFETs $M1$ and $M4$, $V_i$ the gate voltage of the MOSFET $Mi$, $\kappa$ the sub-threshold slope factor [26], and $U_T$ the thermal voltage. By solving for $V_i$:

\[I_x = I_0 e^{\frac{-\kappa R_x I_x}{U_T}} e^{\frac{V_{RD} - V_s}{U_T}}
\]

(3)

If $R_x I_x$ is sufficiently small, then

\[I_0 e^{\frac{-\kappa R_x I_x}{U_T}} \approx I_0 (1 - \frac{\kappa}{U_T} R_x I_x)
\]

(4)

so

\[I_x = I_{Mi} = I_0 e^{\frac{V_{RD} - V_s}{U_T}} + \frac{\kappa}{U_T} R_x I_0
\]

(5)

Equation 5 describes how the input current changes with the conductance of the memristive device, and with $V_{RD}$ and $V_s$ voltages. In particular, for large $V_{RD} - V_s$ values, the current is approximately linear with respect to the memristive device conductance, but assumes relatively large values (large values make the circuit less power-efficient). For very small $V_{RD} - V_s$ voltage differences, the circuit produces very small currents that change linearly, but with a very small dependence on the device memristance $R_x$.

The effect of this trade-off is highlighted in Fig. 5a, which plots eq. 5 for different values of $V_s$, with $V_{RD}$ set to 1.8 V. Figure 5b shows circuit simulations results, carried out using a standard 130nm CMOS process, which support the theoretical analysis. $V_{RD}$ was set to 1.8 V, while $V_s$ was swept to obtain the three different $V_{RD} - V_s$ values shown in the figure legend. In this mode of operation the voltage applied across the memristive device is set low enough to prevent conductance changes. This allows us to model the device as a fixed resistor, and to characterize the circuit as a function of all resistance values between the memristive device’s low and high resistance states.

The output currents of the differential memristive circuit are directly proportional to the input currents sensed from the corresponding input branch and scaled by the bias current $I_b$. Specifically, if all transistors operate in sub-threshold saturation domain:
Figure 5: (a) Theoretical solution of the input current as a function of memristive device resistance, for different values of \( V_{RD} - V_s \) settings, with \( V_{RD} \) set to 1.8 V. (b) SPICE circuit simulations of the same current for a 130nm CMOS process.

\[ I_{M1} = I_0 e^{\frac{\kappa}{kT} V_1 e^{-\frac{V_s}{kT}}} \]

\[ I_{M4} = I_0 e^{\frac{\kappa}{kT} V_4 e^{-\frac{V_s}{kT}}} \]

By solving for \( e^{-\frac{V_s}{kT}} \) using the extra condition that \( I_b = I_{pos} + I_{neg} \), and replacing terms in eq. 6, we obtain:

\[ I_{pos} = I_b \frac{I_{M1}}{I_{M1} + I_{M4}} \quad I_{neg} = I_b \frac{I_{M4}}{I_{M1} + I_{M4}} \] (6)

This allows us to produce output currents that are scaled versions of the currents flowing through the memristive devices, and potentially much smaller, thus enabling the design of ultra low-power current-mode memristive sensing architectures. In order to ensure proper operation of the differential memristive output normalizing behavior, while minimizing the power dissipated in the input current sensing stage, it is important to have large \( V_s \) values, with small \( V_{RD} - V_s \) values.

Figure 6 shows the theoretical normalized output current \( I_{pos} \), for a bias current \( I_b = 20nA \), for resistance values of \( D_{pos} \) increasing from 1KΩ to 20KΩ, and of \( D_{neg} \) decreasing proportionally from 20KΩ to 1KΩ. A differential current-mode readout circuit that computes \( I_{pos} - I_{neg} \) can double the resolution of the conductance/memory state sensing operation. More realistic circuit simulation results for a 130nm CMOS process are shown in Fig. 7. To generate this plot, the memristive devices were modelled as resistors and the resistance of \( D_{pos} \) was swept from 100Ω to 20KΩ. The bias voltage \( V_b \) was set to generate a bias current, \( I_b \), of 20nA. The simulation results show the output of the circuit for different settings of \( V_s \) and as a function of different conductance values assumed for the memristive devices. The blue, red, and green traces are the current outputs when the resistance of \( D_{neg} \) was set as 1KΩ, 10KΩ, and 19KΩ respectively.
Figure 6: Theoretical normalized output current of the analytic differential memristive circuit as a function of 20 different memristive conductance values, for three different \((V_{RD} - V_s)\) settings, with \(I_b = 20nA\), and \(V_{rd} = 1.8V\).

Figure 7: Circuit simulation results for the transfer characteristics of the normalizer circuit. Different colors represent different the circuit response for different values of the \(D_{neg}\) resistor. Solid traces represent the current \(I_{pos}\) while dashed ones represent \(I_{neg}\). Different markers denote different \(V_{rd} - V_s\) settings.

The solid and dashed lines plot \(I_{pos}\) and \(I_{neg}\) respectively. It can be seen from the plots that the cross over point shifts as the resistance values of \(D_{neg}\) change. Note how the linearity of the circuit is improved when \(V_{rd} - V_s\) is reduced, at the cost of slightly reduced difference between \(I_{pos}\) and \(I_{neg}\).
Figure 8: Effect of memristive device variability on synapse circuits outputs. (a) Distribution of device resistance values (Mean, Std Dev) for $\Omega_{D_{\text{neg}}} = (2.87 \, k\Omega, 490 \, \Omega)$ and $\Omega_{D_{\text{pos}}} = (6.12 \, k\Omega, 1.3 \, k\Omega)$. The dashed lines represent the sampling distributions. (b) Distribution of output currents for the resistance samples derived from (a). (c) Difference of output current samples versus difference of high-low resistance samples derived from (a). (d) Coefficient of variation of output current difference and of resistance difference as a function of different high-low ratios, and for three different values of resistance CV (0.2, 0.3, and 0.4 for the circles, crosses and stars respectively).

3.2. Variability reduction

The strategy to use two memristive devices programmed in a complementary fashion and connected to the current-mode normalizer circuit has the additional benefit of significantly reducing the impact of memristive device variability in the output currents. To demonstrate this effect, we show in Fig. 8 the results of Monte Carlo simulations in which we compare the variability of the output currents versus the one of the memristive devices. In these simulations we set $I_b = 20 \, nA$ and $V_S = 0.9 \, V$. On the basis of $HfO_2$ data available from the literature [7], we used conservative figures for the distributions of the memristive device high/low states and their variance. In particular, we sampled resistance values from a Gaussian distribution with (mean, standard deviation) of $(6 \, k\Omega, 1200 \, k\Omega)$ and $(3 \, k\Omega, 600 \, \Omega)$ in the high and low resistance states, respectively (see...
samples in Fig. 8a), and measured the circuit response using such values (see Fig. 8b). We observed that the histogram of the output currents $I_{\text{pos}}$ and $I_{\text{neg}}$ are symmetric, illustrating the effect of normalization, with a standard deviation of approximately 2.12 nA for both branches. The normalization circuit effectively compresses the error in output current for large difference between resistances and expands it for small differences as shown in Fig. 8c. Even for these conservative values of resistance figures, with a very small high-low ratio, the reduction in the Coefficient of Variation (CV) went from 0.429 for the $\Omega_{\text{pos}} - \Omega_{\text{neg}}$ to 0.284 for $I_{\text{pos}} - I_{\text{neg}}$. For more typical cases, for example with high-low resistance values equivalent to 100 K$\Omega$ and 10 K$\Omega$, the same analysis shows a drastic reduction of CV from 0.219 to 0.003. In Fig. 8 we show a systematic comparison of the CVs between the basic resistance differences and the output current differences, for increasing ratios of high-low states. The comparison was performed running Monte Carlo simulations in which the device high and low resistance states were sampled from a normal distribution with three different coefficients of variation (0.2, 0.3, and 0.4), and the output currents were calculated using the circuit’s transfer function derived analytically in Section 3.

3.3. Write-mode operation

The write-mode operation takes place immediately after the read-mode phase, as determined by the sequence of $V_{\text{read}}$ and $V_{\text{write}}$ pulses generated by the pulse-shaper circuit of Fig. 2. In this phase, $V_{\text{read}}$ is zero, the $V_{\text{write}}$ is high. Furthermore, the switches of two memristive devices (S4-S10) are turned on in a complementary way, such that the resultant voltage across the memristive devices induce opposite changes in their conductance values. For example, to increase the net output current ($I_{\text{pos}} - I_{\text{neg}}$), the conductance of $D_{\text{pos}}$ is increased and that of $D_{\text{neg}}$ is decreased. This is done by enabling the switches S5, S6, S9, and S10 by programming the $V_{\text{set}}$ signal to logical one, and $V_{\text{reset}}$ to logical zero. This connects $V_{\text{topp}}$ to $V_{\text{ST}}$, $V_{\text{botp}}$ to ground, $V_{\text{botn}}$ to $V_{\text{RST}}$, and $V_{\text{topn}}$ to ground. Similarly, to decrease ($I_{\text{pos}} - I_{\text{neg}}$), the $V_{\text{reset}}$ signal is to set logical one, and $V_{\text{set}}$ is set to logical zero. The MOSFETs M7 and M8 are current-limiting transistors that protect the devices from damage during programming. The signal $V_{\text{lim}}$ is a bias voltage chosen that ensure that the memristive devices are not damaged during the forming operation. To minimize power consumption all switching transistors are turned on only during a read or write pulse.

The pulse shaping circuit of Fig 2 can be tuned to increase or decrease the write pulse duration. So by programming the length of these pulses and by choosing appropriate values for $V_{\text{ST}}$ and $V_{\text{RST}}$ voltages, it is possible to use this circuit to produce reliable binary, gradual, or stochastic changes in the memristive devices [7, 22]. The mode of operation of the memristive devices and the nature of the changes that should be induced in the memristive device conductance depend on the specific learning algorithm implemented in the learning block of Fig. 3.
4. Learning simulations

In this section we demonstrate examples of spike-based learning simulations using a learning rule that is ideally suited for implementation in neuromorphic architectures that comprise the memristive synapse proposed. In the first subsection we learn a single low-dimensional pattern with varying contrast, in the second subsection we learn many overlapping high-dimensional patterns.

4.1. Single pattern binary classification

Here we show simulation results of two neurons trained to classify an input spike-train by adjusting their synaptic weights. We study the performance of such a learning system connected by multiple binary synapses and compare it to that of a hypothetical 32-bit floating-point precision synapse in the same setting. This illustrates what the performance limitation is with an ‘ideal’ synaptic element for classifying a finite-rate Poisson train with a leaky integrator neuron.

In this task, the neurons $a$ and $b$ are connected via randomly initialized synapses to two neural populations $p_1$ and $p_2$, which fire with two different average firing rates, with Poissonian statistics. The goal is for neuron $a$ to learn to fire more than neuron $b$, whenever input units from population $p_1$ fire at a higher rate than input units in $p_2$. To achieve this, we use a supervised training protocol: given the input, we provide a teacher signal to the neuron that should fire more. The teacher signal is represented by a Poissonian spike train sent to the target neurons via an additional, separate, channel. The spike-based learning algorithm is a discretized version of the one presented in [49]. It performs a gradient descent procedure on the difference of the observed and desired neuron firing rates, and it can be readily implemented in mixed signal CMOS neuromorphic hardware [34, 42]. A detailed description of this learning rule and the parameter values used are provided in the Supplementary Material.

In Fig. 9 we compare the classifications results produced by the best system using a 32-bit floating-point precision synapse with the results obtained simulating the proposed binary synapse in the same setting. Each of the two variables is proportional to the firing rate of the respective subpopulation. When they are equal the pattern has no ‘constrast’, when they are very different it is strongly contrasted. The colors indicate which of the two learning neurons fired more strongly; the ideal solution is a separation of red and blue at a $45^\circ$ angle. The proposed learning rule finds a good solution to the classification problem, in that the misclassified points only elicit a slightly higher response in the wrong output neuron.

4.2. Classifying multiple patterns

Here we show how it is possible to train a population of output neurons to classify multiple overlapping patterns in a supervised setting. For this demonstration we use the common benchmark of classifying handwritten digits from the MNIST data-set.
Figure 9: Comparison of the classification output of the two neuron system with 40 binary weight elements (left) and 40 floating-point resolution synapses (right). The size of the circles indicates the difference in output rates of the two neurons.

Namely we test the system using MNIST digits from 0 to 4 scaled to 24 × 24 pixels, as in [4]. In the network, there is an input layer consisting of 24 · 24 · n_c Poisson neurons, whose spike rates are scaled according to the intensity of the MNIST digit image pixel, and the output layer consisting of 5 neurons that should learn to respond to the corresponding digit, and an additional layer of teacher neurons indicating which of 5 output neurons should fire in response to a given input. The index of the output neuron that fires the most in response to a test stimulus is considered the label that the network assigns to this input. During training 1000 digits, randomly drawn from the training set, are presented for 100 ms each while the learning circuits are enabled. The learning circuits are then disabled and the performance of the network is evaluated on 500 further digits (randomly drawn from the test set). Further implementation details are given in the supplementary material.

The learning algorithm is the same one used in Section 4.1. To compensate for the discretization errors, the update is made probabilistic as in [34]. Although we restrict ourselves to probabilistic signals that are independent per neuron, rather than per synapse, we achieve a performance comparable to that of [4].

In Fig. 10a we report the performance of the network as a function of the number n_c of synapses used per pixel, in terms of classification accuracy. In Fig. 10b we show two examples of the learned weight matrices.
(a) Error on the (reduced) MNIST classification task (test set) as a function of the number of binary synapses per input pixel for high and low CV. The CV settings correspond to Fig. 8. Errorbars indicate std. dev. on 5 repetitions.

(b) Learned weight matrices with one and eight synaptic weights.

5. Discussion

The memristive synapse circuit proposed in this paper comprises two memristive devices, 20 MOSFETs, and a pulse controller module. Clearly, the resulting synaptic circuit is much larger in area than synapse elements employed in dense 1R or 1T-1R crossbar arrays [16, 38, 40]. However, the large area overhead used allows the system to operate multiple synapses in parallel, both along the rows and along the columns of the synaptic array (e.g., by sending multiple AER pulses in quick succession across multiple columns). In addition, as the currents passing through the memristive devices are contained in each individual synapse element and do not diffuse to neighboring devices, there are no sneak-path issues and no problems for quickly charging/discharging high capacitive loads. The strategy of using two memristive devices per synapse allows the use of a normalizer circuit, which has the desirable property of minimizing the effect of variability across the memristive devices. In addition, the strategy adopted to use the two devices in a differential way, increasing one while decreasing the other, eliminates the need for a precise reference for the normalizer operations, and provides automatically the possibility to implement both positive and negative synaptic weights in the network.

6. Conclusion

We proposed a differential current-mode memristive synapse circuit that decouples the current used to sense or change memristive device state from the current used to stimulate ultra low-power post-synaptic neuron circuits. We showed that the circuit proposed significantly reduces the effect of device variability, and that it is ideally suited for implementing advanced spike-based learning mechanisms that do not use overlapping pulses at the terminals of the target synapse. We argued that the strategy of using pulse extenders and Gilbert-normalizers in each synapse element maximizes throughput
and minimizes power consumption in large-scale event-based neuromorphic computing platforms. For applications that do not require online adaption or simultaneous read-write functionality, we describe how the synaptic circuit can be integrated with dense memristive crossbar arrays (Supplementary material). Given that memory-related constraints, such as size and throughput, represent one of the major bottlenecks in conventional computing architectures [23], and given the potential of neuromorphic computing platforms to perform robust computation using variable and slow computing elements, the proposed circuit offers an attractive solution for building alternative non von Neumann computing platforms with advanced and emerging memory technologies.

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Supplementary material:
A differential memristive synapse circuit for on-line learning in neuromorphic computing systems

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1. Learning Simulation Setup

The following differential equations define our neuron model. They were derived in [1] to describe the behavior of a neuron circuit that approximates an exponential adaptive integrate-and-fire neuron. Compared to [1] we added an additional term $I_{\text{comp}}$ that reflects the compensation current injected by the learning circuit, which was not present in the original equations. This current enforces that the neuron fires in accordance with its input teacher signal.

$$ \frac{dI_m(t)}{dt} = \frac{I_{\text{pos}}(t) - I_m(t) (1 + I_{\text{adapt}}(t)/I_\tau)}{\tau_m(1 + \frac{I_{\text{th}}}{I_m(t) + I_0})} $$  \hspace{1cm} (1)

$$ \frac{dI_{\text{adapt}}(t)}{dt} = \frac{I_p - I_{\text{adapt}}(t)}{\tau_{\text{adapt}}} $$ \hspace{1cm} (2)

$$ I_m(t) \leftarrow I_{\text{reset}} \quad \text{if} \quad I_m(t) > I_{\text{spkthr}} $$ \hspace{1cm} (3)

With synaptic differential equation

$$ \frac{I_{\text{syn}}(t)}{dt} = -I_{\text{syn}}(t) + I_a w_{\text{syn}} \sum_i \delta(t_{\text{spike}}^i - t). $$ \hspace{1cm} (4)

For compactness we introduced

$$ I_{\text{pos}}(t) = I_{\text{fb}}(t) + \frac{I_{\text{th}}}{I_\tau} (I_m(t) + I_{\text{comp}}(t) + I_{\text{syn}}(t) - I_{\text{adapt}}(t) - I_\tau) $$ \hspace{1cm} (5)

$$ I_{\text{fb}}(t) = \frac{I_a(t)}{I_\tau} (I_m(t) + I_{\text{th}}) $$ \hspace{1cm} (6)

$$ I_a(t) = \frac{I_g}{1 + \exp \left(-\frac{(I_m(t) - I_{\text{ath}})}{I_{\text{anorm}}} \right) $$ \hspace{1cm} (7)

The table 1 clarifies the meanings and where appropriate the values of the above variables and parameters.
### Table 1: Neuron and Synapse Variables and parameters.

| Name          | Description                                      | Value                      |
|---------------|--------------------------------------------------|----------------------------|
| $I_m(t)$      | Membrane Current                                | Variable                   |
| $I_{pos}(t)$  | Positive input to the neuron                    | Variable                   |
| $I_{adapt}(t)$| Adaptation feedback                             | Variable                   |
| $I_\tau$      | Neuron time constant bias                        | 2 pA                       |
| $\tau_m$      | Neuron time constant                             | 8.9 ms                     |
| $I_{th}$      | Global synaptic input scaling factor             | 1 pA                       |
| $I_0$         | Leak Current (process parameter)                 | 0.5 pA                     |
| $I_p$         | Feedback rate                                    | 0.5 pA                     |
| $\tau_{adapt}$| Adaptation time constant                         | 17.7 ms                    |
| $I_{reset}$   | Membrane reset level                             | 1 pA                       |
| $I_{spkthr}$  | Spike threshold                                  | 60 pA                      |
| $I_{syn}$     | Synaptic input current                           | Variable                   |
| $n_{in}$      | no. synapses per input channel                   | given in plots             |
| $I_w$         | Synaptic bias current                            | 16 pA (MNIST)              |
| $w_{syn}$     | Synaptic bias current                            | 1 nA /$n_{in}$ (single pattern) |
| $t_{spike}$   | Times of presynaptic spikes                      | Variable                   |
| $I_{fb}(t)$   | Feedback current                                 | Variable                   |
| $I_{a}(t)$    | Fitting variable for feedback                    | Variable                   |
| $I_g$         | Feedback gain                                    | 1 nA                       |
| $I_{ath}$     | Fitting variable                                 | 20 nA                      |
| $I_{anorm}$   | Fitting variable                                 | 1 nA                       |

#### 1.1. Learning Equations

The learning block acts according to:

\[
\frac{dT(t)}{dt} = -\frac{T(t)}{\tau_{\text{learn}}} \tag{8}
\]
\[
\frac{dS(t)}{dt} = -\frac{S(t)}{\tau_{\text{learn}}} \tag{9}
\]
\[
I_{\text{comp}}(t) = g_{\text{comp}}(T(t) - S(t))(t < t_{\text{stop}}) \tag{10}
\]
\[
q(t) = (S(t) + S_0 - I_{\text{syn}}(t)) \tag{11}
\]
\[
L(t) = \text{sign}(q(t))(|q(t)| > \alpha) b_p(t) \tag{12}
\]

When a presynaptic spike arrives, $w_{\text{syn}}$ is updated according to the value of $L(t)$. The update is to redraw $w_{\text{syn}}$ from one of the two distributions given in the main paper for high and low coefficient of variation, rescaled so that both have the same mean. For the single pattern simulations the distributions were normal distributions with the same
mean and variance as the aforementioned. Overall this results in a probabilistic binary update.

In the case of the high resolution synapse the last equation becomes an analog update proportional to \( q(t) \) (with scaling factor 0.0001).

On a postsynaptic spike / a teacher spike \( w_S \) / \( w_T \) are instantaneously added to \( S(t) / T(t) \).

This implements an update that is similar to [6]; the key differences are the use of a sign function to limit the output of the circuit to \( \{-1, 0, 1\} \) (decrease, keep, increase synaptic value) and the addition of \( b_p(t) \) that probabilistically enables / disables the learning block to implement a form of RUSD [3].

The functional effect of these equations is to perform a gradient descent procedure of brining the output spike rate of the neuron close to the teacher signal (as shown in [6]), but in contrast to [6] updates are discretized and probabilistic as in RUSD [3].

The table 2 clarifies the meanings and where appropriate the values of the above variables and parameters.

1.2. Population Level Parameters

The table Tab. 3 gives an overview of the values population level parameters were set to.

2. Advantages of the normalizer circuit over a current mirror

Isolating the current flowing through the device from that sent into the post-synaptic neuron can also be achieved by use of a simple current mirror circuit as shown in Fig. 1.
Table 3: Population level parameters.

| Description                      | Value                                                                 |
|----------------------------------|----------------------------------------------------------------------|
| Firing rate positive single pattern | \((x \cdot 50 \text{ kHz} + 5 \text{ kHz})/n_{in} ; x \sim U(0.5, 1)\) |
| Firing rate negative single pattern | \((x \cdot 50 \text{ kHz} + 5 \text{ kHz})/n_{in} ; x \sim U(0, 0.5)\) |
| Teacher rate positive single pattern | 50 kHz                                                               |
| Teacher rate negative single pattern | 0 kHz                                                                |
| Firing rate MNIST              | \(z \cdot 100 \text{ Hz} ; z \) is the pixel value                  |
| Teacher rate positive MNIST class | 100 Hz                                                               |
| Teacher rate negative MNIST class | 0 Hz                                                                |
| No. teacher neurons            | 40                                                                   |

This circuit is put in read mode when \(Read\) and \(\overline{Read}\) are set to logical 1 and 0 values, respectively. However, with this circuit the \(\frac{\text{Width}}{\text{Length}}\) ratio between the transistors M1 and M2 will have to be made very large to reduce the output current \(I_x\). For example, to reduce the read current from 1\(\mu A\) to 1\(nA\), which is a typical value for input currents to sub-threshold silicon neurons [2], would require a ratio of 1000. Secondly, without use of power-hungry active feedback circuit, the drain voltages of M1 and M2 will be different, which will result in poor current mirroring accuracy. The normalizer circuit we propose addresses both of these issues. The proposed circuit is also more compact. This is because while the normalizer uses two extra transistors (M5 and S13 in Fig. 3), these are the sized comparably to M1-M4. The absence of large scaling factors makes the total area of the circuit smaller. Note that while the differential synapse circuit comprises two copies of the basic current mirror, it also provides twice the dynamic range. Finally, the proposed design can be extended in various ways as described in the following sections.
3. Improving linearity

Equation ?? is obtained by making an approximation to the transcendental Eq. ???. The approximation error can be eliminated by use of active elements as shown in Fig. 2. By use of feedback circuits, the voltage at the bottom nodes of the memristive devices are set to $V_{REF}$. Therefore, the current flowing through M1 and M4 is made a linear function of the device conductance. The normalizer outputs are consequently a linear function of the device conductance.

$$I_{M1} = G_{pos} \cdot (V_{RD} - V_{REF})$$
$$I_{M4} = G_{neg} \cdot (V_{RD} - V_{REF})$$
$$I_{pos} = I_b \cdot \frac{I_{M1}}{I_{M1} + I_{M4}} = I_b \cdot \frac{G_{pos}}{G_{pos} + G_{neg}}$$
$$I_{neg} = I_b \cdot \frac{I_{M4}}{I_{M1} + I_{M4}} = I_b \cdot \frac{G_{neg}}{G_{pos} + G_{neg}}$$

While the active circuits will consume additional power and area, it improves linearity. Additionally, by making the difference $V_{RD} - V_{REF}$ small, the currents $I_{M1}$ and $I_{M4}$ can be made much smaller, partly compensating for the increased power consumption resulting from the use of Op-Amps.

4. Multi-device memory block

The proposed normalizer circuit can be extended to multiple memristive devices. This can be used to create multi-state memory cells using devices that have only two
stable states. Figure 3 illustrates this for $n$ devices where each branch comprises the arrangement highlighted with green circles. The currents generated by each branch are approximately equal to:

$$ I_k \approx I_b \cdot \frac{G_k}{\sum_{x=1}^{n} G_x} $$  \hspace{1cm} (17)

where, $G_k$ is the conductance of device $D_k$.

Figure 3: Extension to multiple memory devices

These output currents can be combined to create positive and negative output
currents in different ways, depending on the application. For example,

\[ I_{\text{pos}} = \sum_{x=1}^{m-1} I_x \]  \hspace{1cm} (18)

\[ I_{\text{neg}} = \sum_{x=m}^{n} I_x \]  \hspace{1cm} (19)

Another possibility to expand the dynamic range of the output currents is to weigh the currents output from each branch as follows:

\[ I_{\text{pos}} = \sum_{x=1}^{m-1} 2^x \cdot I_x \]  \hspace{1cm} (20)

\[ I_{\text{neg}} = \sum_{x=m}^{n} 2^{x-m} \cdot I_x \]  \hspace{1cm} (21)

**Read operation** : The read operation of multi-memory cell is enabled when the \( V_{\text{sel}}, \) \( \text{Read}, \) and \( \overline{\text{Read}} \) signals are set to logical 1, 1 and 0, respectively. In this mode, transistors S1 and S2 in each branch shown in Fig. 3 are on, and transistors S3-S6 are off. In this configuration, each branch in the circuit shown in Fig. 3 generates a current given by Eq 17.

**Write operation** : As in the case of the two device differential cell, programming the state of the devices is achieved by suitably setting the corresponding \( \text{Set}x \) and \( \text{Reset}x \) signals of the branch. Increasing or decreasing the synaptic weight is achieved by modifying the conductances of a subset of devices contributing to \( I_{\text{pos}} \) and \( I_{\text{neg}} \). The specific control circuitry for determining \( \text{Set}x \) and \( \text{Reset}x \) signals depends on the specific equations used to generate the output currents, \( I_{\text{pos}} \) and \( I_{\text{neg}} \).

### 5. Integration into a crossbar array

There are several applications where area is an important concern, and dense 2D synaptic arrays are desired.

The circuits presented can be integrated in a dense crossbar array by taking apart the circuit shown in Fig 3 and rearranging them as illustrated in Fig 4. The crossbar circuit shown in Fig 3 has 6 synapses implemented in a \( 6 \times 3 \) crossbar array connected to two neurons, where each synapse comprises a three device memory cell. The circuit elements implementing the proposed normalizer circuits are highlighted in green and labeled to match to the corresponding circuit elements in Fig. 3. In this design, circuits elements are shared by multiple synapses. That is, all the memristive devices in a column, \( \text{Cx} \), share the transistors \( S1_{-\text{Cx}}, S3_{-\text{Cx}}, \) and \( S5_{-\text{Cx}} \). All the memristive devices in a row, \( \text{Rx} \), share the transistors \( S2_{-\text{Rx}}, S4_{-\text{Rx}}, \) and \( S6_{-\text{Rx}} \). The normalizer bias circuits comprising, \( M5_{-\text{Nx}} \) and \( S13_{-\text{Nx}} \), are shared by all synapses associated
with neuron Nx. When a synapse, Synx_Ny is read, the three devices in it are put in a configuration equivalent to the one shown in Fig. 3 with \( n = 3 \). In Fig 4, each memristive device, Dxy, has a series access transistor, Sxy, that prevents flow of current through inactive synapses. This transistor can be eliminated to increase crossbar density without affecting the functionality of the circuit at the cost of increased power consumption.

**Read operation**: When a spike train addressed to neuron \( Ni \) arrives, the corresponding \( Sel_{Ni} \) signal turns on the the switches Sxy of the synapses afferent to the neuron. Transistors S1_Cx and S2_Ry corresponding to the neuron \( Ni \) are also turned on. This connects all the synapses belong to neuron \( Ni \) to its normalizer bias circuit. By the principle of linear super-position. Even though all synapses share the same normalizer bias block, the current read out of the normalizer is the same as that generated if each synapse had its own normalizer block.

**Write operation**: At the end of the read operation, all the synapses are updated as per the directions of the learning block or the downstream neuron. However, unlike the differential memristive synapse circuit, described in Sec ??, a subset of the synapses cannot be programmed while part of it is being read. The write operation in this arrangement requires a controller that issues a sequence of signals that gates all read activity while the state of the crossbar array is being updated. The entire array can be updated in two phases. In the first phase, all those device whose conductances need to be increased are updated by enabling to corresponding \( SetColx \) and \( SetRowy \) signals. In the next phase, the devices whose conductances are to be decreased are programmed by programming the \( ResetColx \) and \( ResetRowy \) signals. Similar update schemes have also been proposed in earlier works such as [4, 5].

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Figure 4: The differential memory circuit in a crossbar array. The switches $S_{xy}$ can be eliminated to increase crossbar density without affecting the functionality of the circuit at the cost of increased power consumption.