Line current ripple reduction of two paralleled three-phase two-level converter using optimized common-mode voltage injections

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Abstract
This paper proposes a common-mode voltage injection-based pulse width modulation strategy to optimize the AC current ripple of parallel interleaved converters. In general, modulation methods entail a trade-off between switching times and voltage error. Given the redundancy in the available vector sequences, we sequentially minimize the switching times and the voltage error. Specifically, we propose eight candidate vector sequences with minimized switching times for each 60° sector. Then, we quantitate the current ripple introduced by the eight vector sequences, and according to the calculations, we split each 60° sector into eight subsectors, each employs the respectively optimal vector sequence with the minimized current ripple. For implementation, the candidate vector sequences are further unified by a common-mode voltage injection scheme. The injection depends on the momentary subsector in which the reference lies. Despite the complex geometry of the subsectors, we propose a simple decision procedure that can be easily implemented in mainstream microcontrollers. Compared to the conventional methods, the proposed common-mode voltage injection-based pulse width modulation has a smaller AC current ripple at the same switching loss. The experimental results verify the theoretical analysis and the effectiveness of the proposed common-mode voltage injection-based pulse width modulation strategy.

1 | INTRODUCTION

Paralleled interleaved three-phase converter consisting of two two-level voltage-source converters (VSCs) can double the current working rating and the load-carrying capacity [1–3]. The two converters are connected to a common DC-link, which reduces the system volume but leads to the zero-sequence-circulating current (ZSCC) [4, 5], and common-mode (CM) inductors are inserted before the joint AC connectors (Figure 1) to suppress the circulating current across the converters. Various control methods are proposed to eliminate the low-frequency ZSCC [6–10].

In past years, many different modulation strategies have been proposed to improve the performance of the parallel converter in various aspects. References [11, 12] propose strategies to eliminate line current low-frequency distortion introduced by the imbalance in system parameters and the grid voltages. References [13–15] develop optimized pulse width modulation (PWM) strategies to suppress the high-frequency ZSCC, which is the main part of ZSCC for the reduction of the size of the CM inductors. References [16–20] focus on the optimization of the AC current ripple using the optimized PWM schemes.

The AC current ripple is the time integral of the real-time error between the output AC voltage and the ideal sinusoidal reference voltage. For grid-connected converters, the AC current ripple and thus the total harmonics distortion (THD) have to meet certain grid codes; for motor drives, the AC current ripple produces high-frequency torque ripple, introducing undesirable acoustic noise and torsional vibrations. Therefore, in these applications, AC current ripple reduction has a high priority, as is reflected by the intensive research in the past years.

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In the parallel topology, the line current quality depends on the PWM schemes as well as the interleaving angles. References [16, 17] demonstrate that the interleaved angle should be adjusted according to the modulation index, in order to minimize the AC current ripple. Considering the complexity of the method, Reference [17] further introduces a quasi-optimal strategy with a fixed interleaving angle of 180°. The experimental results validate that the shift angle of 180° yields an AC current ripple close to that of the optimal interleaved angle adjustment.

In addition to optimizing the interleaved angles, many approaches in the literature optimize the PWM schemes for AC current ripple reduction. Reference [18] modulates the parallel converter with the conventional space vector modulation (CSVM) based on two sets of interleaved carriers, which doubles the equivalent output switching frequency and reduces the current ripple. Reference [19] replace the conventional SVM with the active zero-state PWM (AZSPWM), which causes better ZSCC but the same current ripple compared with the CSVM. Reference [14] proposes the modified discontinuous PWM (MDPWM) to suppress the ZSCC, but additional computation efforts are required. Reference [15] develops the interleaved carrier phase-shift PWM (ICPSPWM) for ZSCC suppression, which can be easily introduced into an interleaved parallel converter with an arbitrary number of sub-converter. Although the modulation strategies in [13–15] reduce the ZSCC, their current ripples are relatively high.

Reference [19] treats the two paralleled interleaved converter as a three-level converter, and the consequent method (3LSVM) divides the vector plane into 24 subsectors, where three optimized vectors are used, which reduces the ZSCC and current ripple simultaneously. Reference [20] introduces a hybrid PWM (HBPWM) to minimize the current ripple in parallel interleaved converters. This method uses the nearest three vectors to synthesize the reference voltage, which achieves smaller voltage errors than the above modulation strategies. However, the vector sequences in the HBPWM need 33% more switching times per carrier period compared to the other modulation strategies. The consequent limited effective switching frequency deteriorates the output current, limits the system dynamics, and increases the ZSCC peak. Ideally, the reduction of voltage errors should not cost more switching times. The methods in [13–15,18,19] maintain fewer switching times but suffer a larger voltage error. The HBPWM causes a smaller voltage error but switches more often. This paper aims to find a better and more general trade-off between the switching times and the voltage tracking error.

The paralleled converter constitutes 19 basic voltage vectors and hence some redundancy among them. We prioritize the switching loss and develop eight vector sequences for each of the 60° sector. Then, we further quantitate the current ripples of the eight vector sequences. According to the calculations, each 60° sector can be further divided into eight subsectors, where different vector sequences should be used to reduce the voltage errors. The decision boundary between the candidate vector sequences are complex in shape but allows programming along with a simple flow chart for mainstream microcontrollers. On the other hand, we show that the candidate vector sequences can be unified by the carrier-based implementation, with the only distinction in common-mode voltage injections. Such a finding further simplifies the implementation. We, therefore, name the proposed method the common-mode voltage injection PWM (CMJPWM) strategy. Compared to the modulation strategies except for HBPWM, the CMJPWM has better AC current ripple performance. Compared to the HBPWM, the CMJPWM attains a smaller current ripple except for the region of 0.6 < M < 0.85, where both behaves practically the same; furthermore, the ZSCC of the CMJPWM is much smaller than that of the HBPWM. The experimental results verify the theoretical analysis and the effectiveness of the proposed CMJPWM strategy.

2 | OPERATION PRINCIPLE OF THE TWO PARALLELED THREE-PHASE INTERLEAVED CONVERTER

Figure 1 demonstrates the topology of the two paralleled converters with the common DC side, and the paralleled AC sides through two CM inductors. The output voltages of the two individual two-level converters are

\[
\begin{align*}
\bar{u}_{n1a} &= (2s_{i1} - s_{i2} - s_{i3})V_{dc}/3 \\
\bar{u}_{n1b} &= (2s_{i2} - s_{i3} - s_{i4})V_{dc}/3 \\
\bar{u}_{n1c} &= (2s_{i3} - s_{i4} - s_{i5})V_{dc}/3
\end{align*}
\]  

where \(i = 1,2\) means the two individual two-level converters, \(n\) denotes the neutral point, \(s_{i\alpha}(\alpha = a,b,c)\) is the switch-state function of the \(i\)th leg with \(s_{i\alpha} = 1\) when the upper IGBT is on and \(s_{i\alpha} = 0\) when the upper IGBT is off.

An individual three-phase two-level converter has eight available vectors consisting of six active vectors \((V_{1} - V_{6})\) and two

\[
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\bar{u}_{n1a} &= (2s_{i1} - s_{i2} - s_{i3})V_{dc}/3 \\
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\bar{u}_{n1c} &= (2s_{i3} - s_{i4} - s_{i5})V_{dc}/3
\end{align*}
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\end{align*}
\]
OVERVIEW OF EXISTING METHODS

We briefly review these methods in the first 60° sector of the conventional methods, including CSVM, AZSPWM, and MDPWM consistently use

FIGURE 2 Space-vector plane (a) individual converter, (b) paralleled converter

TABLE 1 Available voltage vectors and switch-state combinations

| Switch states of VSC2 | 000 | 100 | 010 | 011 | 001 | 101 | 111 |
|-----------------------|-----|-----|-----|-----|-----|-----|-----|
| Switch states of VSC1 | 000 | V_0 | V_1 | V_2 | V_3 | V_4 | V_5 |
|                       | 100 | V_1 | V_2 | W_1 | W_2 | W_3 | W_4 |
|                       | 110 | W_2 | W_3 | W_2 | V_3 | V_4 | V_5 |
|                       | 010 | V_3 | V_4 | V_3 | V_4 | V_5 | V_6 |
|                       | 001 | V_4 | W_4 | V_4 | W_4 | W_5 | W_6 |
|                       | 101 | W_5 | W_6 | W_5 | W_6 | V_7 | V_8 |
|                       | 111 | V_6 | V_7 | V_6 | V_7 | V_8 | V_9 |

zero vectors (V_0 and V_2), which are shown in Figure 2(a). When the two converters are paralleled, the equivalent output phase voltages are

\[
\begin{align*}
\nu_{\alpha} &= \left(\nu_{\alpha1} + \nu_{\alpha2}\right)/2 \\
\nu_{\beta} &= \left(\nu_{\beta1} + \nu_{\beta2}\right)/2 \\
\nu_{\delta} &= \left(\nu_{\delta1} + \nu_{\delta2}\right)/2
\end{align*}
\]

(2)

The available vectors of the paralleled converter can be developed by submitting all the switching states (\(\nu_{\alpha} \)) into Equations (1) and (2), which are shown in Figure 2(b). The switch-state combinations of the two individual converters and the resulted 64 available vectors of the paralleled converter are given in Table 1, with VSC1 denoting the first converter (Figure 1) and VSC2 denoting the second converter (Figure 1).

3 | OVERVIEW OF EXISTING METHODS

Many modulation strategies have been proposed to improve the line current quality, including CSVM, AZSPWM, MDPWM, ICPSPWM, 3LSVM, and HBPWM. We briefly review these methods in the first 60° sector of Figure 3(a).

The instantaneous voltage error between the actual instantaneous output phase voltage and ideal sinusoidal reference voltage leads to the AC current ripple. The total AC current ripple \(i_{\text{rip}}\) is a crucial indicator for the evaluation of the three-phase output current quality. If the parasitic resistance of the inductor is neglected, the total AC current ripple \(i_{\text{rip}}\) can be expressed as

\[
i_{\text{rip}} = \sqrt{\nu_{\text{rip}_a}^2 + \nu_{\text{rip}_b}^2 + \nu_{\text{rip}_c}^2} = \sqrt{\frac{3}{2} \left(\nu_{\text{rip}_a}^2 + \nu_{\text{rip}_b}^2\right)}
\]

(3)

where \(\nu_{\text{rip}_a}, \nu_{\text{rip}_b}\) and \(\nu_{\text{rip}_c}\) denote the components under three-phase and two-phase stationary coordinate systems of the current ripple; \(\nu_{\text{rip}_a}\) and \(\nu_{\text{rip}_b}\) are the instantaneous voltage error components under the two-phase stationary coordinate system; \(L\) is equivalent inductance \(L = L_a + L_{cm}/2\); \(\Delta t\) is the time interval.

Equation (3) shows that it is vital to reduce voltage errors \(\nu_{\text{rip}_a}\) and \(\nu_{\text{rip}_b}\) in order to optimize the current ripple.

In Sectors \(\rho_1\), \(q_1\), and \(r\) [see Figure 3(a)], the CSVM, AZSPWM, and MDPWM consistently use \(V_{\alpha 1}, V_{\beta 1}\), and \(V_0\) to synthesize the reference voltage, resulting in voltage vector errors \(V_{\text{err}_{\alpha 1}}, V_{\text{err}_{\beta 1}}\), and \(V_{\text{err}_0}\) (see Figure 3(b)). For high modulation regions, vector \(V_0\) introduces a larger error; for low modulation regions, \(V_{\rho 1}\) introduces a larger voltage error. Therefore, those PWM strategies always suffer a large voltage error.

In Sectors \(\rho_1\) and \(q_1\), 3LSVM uses \(V_{\alpha 1}, V_{\beta 1}\), and \(V_0\) to synthesize the reference. The corresponding voltage vector errors \(V_{\text{err}_{\alpha 1}}, V_{\text{err}_{\beta 1}}\), and \(V_{\text{err}_0}\) are smaller than those of the above three methods. In Sector \(r\), the 3LSVM uses the nearest three vectors \(V_{\rho 1}, V_{\beta 1}\), and \(V_{\alpha 1}\), which possess the smallest voltage errors. With the smaller voltage vector errors in all sectors, the 3LSVM gets a better line current quality than those of the three methods. However, the 3LSVM does not achieve minimal voltage vector errors in Sectors \(\rho 1\) and \(q 1\).

The space-vector plane and available vectors of the paralleled converter shown in Figure 2(b) are similar to that of the 3L-NPC converter. Mimicking the nearest three vectors
method of a 3L-NPC converter, the HBPWM divides the first 60° sector into four small regular triangle areas, in which the nearest three vectors are used to synthesize reference. Thus, the voltage errors of the HBPWM are smaller than those of the other methods. However, to select the nearest three vectors, four IGBTs need two more switching times per carrier period. For instance, if the reference is in Sectors \( \rho 1, \rho 2 \) (Figure 3), the HBPWM uses three vectors \( V_{s1}, V_{s2}, \) and \( V_{s0} \), and one of the arranged sequences is

\[
V_{s1}(100/111) \rightarrow V_{s0}(000/111) \rightarrow V_{s2}(000/110) \rightarrow V_{s1}(000/100) \rightarrow V_{s2}(110/000) \rightarrow V_{s0}(111/000) \rightarrow V_{s1}(111/100)
\]

As a result, the switches \( s_{11}, s_{14}, s_{21}, \) and \( s_{24} \) in Figure 1 need to switch four times per carrier period. The total switching times of the HBPWM per carrier period is 32, whereas the other methods switch 24×. In addition, due to the twice switching in a carrier period, the HBPWM requires extra hardware to control the gate signals of the IGBTs, which is not required by the other methods.

ICPSPWM adopts phase-shifted carriers among three phases and between two individual converters, which makes the analysis of the voltage vector errors infeasible. The numerical analysis of the ICPSPWM is presented in Section 6.

In summary, the CSVM, AZSPWM, MDPWM, and 3LSVM maintain fewer switching times while having a larger voltage error; the HBPWM has a smaller voltage error at the expense of more switching times.

The switching loss is roughly proportional to the switching times in one carrier period. Therefore, when compared to those of the other methods, the HBPWM needs to reduce its achievable effective switching frequency by \( \approx 25\% \) to keep the same switching loss. The achievable switching frequency is the leading factor of AC current ripple reduction, and the lower effective switching frequency introduces a higher current ripple.

### 4 I OPTIMAL VECTOR SEQUENCES FOR VOLTAGE ERRORS REDUCTION WITH MINIMAL SWITCHING TIMES

Table 1 lists the basic vectors as well as their redundancies; the redundancies further allow targeted performance optimization by the special vector sequences. Intending to reduce the voltage error with minimized switching times, we investigate the available vector sequences in the six subsectors in Figure 3(a) one by one according to the rules:

1. The vector sequence uses the minimized switching times per carrier period.
2. The vector sequence introduces minimal voltage errors.
3. The optimal voltage error is subjected to the minimized switching times.

In addition, vector sequence with the minimized switching times has the following features:

1. The switching times per carrier period is minimal.
2. In each switching period, each IGBT is not allowed to switch more than once.
3. At any instance, only one commutation is allowed.

In Sectors \( \rho 1, \rho 2 \) (Figure 3), the vectors \( V_{s0}, V_{s1}, \) and \( V_{s2} \) are the nearest three vectors, which result in the minimal voltage errors. For minimal switching times, we propose two vector sequences Seq1 and Seq2, as shown in Table 2. The Seq1 and Seq2 achieve the same voltage errors as that of the HBPWM, but with fewer switching times. In Sector \( \tau \), vectors \( V_{s1}, V_{s2}, V_{s1}, \) and \( V_{s1} \) are the nearest three vectors. Conforming the above rules, we develop Seq7, which also needs fewer switching times than that of the HBPWM. Also, a similar conclusion can be made for Sector \( \iota \), where Seq8 achieves the same voltage errors but less switching loss than HBPWM.

In Sectors \( \rho 1, \rho 2, \tau, \) and \( \iota, \) the switching times and the vector error can be concurrently optimized. However, in Sectors \( q1 \) and \( q2, \) the selection of the nearest three vectors \( (V_{s1}, V_{s2}, \) and \( V_{s2}) \) contradicts the minimized switching times. Alternatively, we investigate the vectors combinations that introduce the suboptimal errors in Sectors \( q1 \) and \( q2, \) which are \( V_{s1}/V_{s2}/V_{s2}, V_{s2}/V_{s3}/V_{s1}, V_{s1}/V_{s2}/V_{s2}, \) and \( V_{s2}/V_{s1}/V_{s1}. \) To minimize the switching times, we propose vector sequences (Seq3–Seq6) of these suboptimal vectors, as listed in Table 2. Note that Table 2 only shows the vectors sequence in the first half switching period due to the symmetry.

According to the space-vector synthesis and volt-second balance principle, for three basic vectors used in a vector sequence, only the reference vectors located inside the triangle formed by the terminals of the three vectors can be synthesized, which means that the vector sequences have different linear modulation zones. The available zones of the eight candidate sequences are marked in Figure 4. Triangle \( \Delta OCD \) pertains to vector sequences Seq1 and Seq2; \( \Delta CDB, \Delta DCA, \Delta CEB, \Delta DEA, \Delta CEA, \) and \( \Delta DEB \) respectively corresponds to Seq3, Seq4, Seq5, Seq6, Seq7, and Seq8. Figure 4 reveals some overlaps of different modulation zones, which is further detailed in Table 3. We exploit the redundancy in the overlapped regions to optimize the switching sequence.

![Figure 4](image-url)
TABLE 2  Available vector timing sequences with minimal switching times

| Seq1 | \( V_{1a} \) 110 → \( V_{2a} \) 111 → \( V_{1a} \) 111 → \( V_{2a} \) 111 → \( V_{1a} \) 111 |
| Seq2 | \( V_{1a} \) 000 → \( V_{1a} \) 110 → \( V_{1a} \) 110 → \( V_{1a} \) 110 → \( V_{1a} \) 110 |
| Seq3 | \( V_{1a} \) 111 → \( V_{1a} \) 111 → \( V_{1a} \) 111 → \( V_{1a} \) 111 → \( V_{1a} \) 111 |
| Seq4 | \( V_{1a} \) 000 → \( V_{1a} \) 110 → \( V_{1a} \) 110 → \( V_{1a} \) 110 → \( V_{1a} \) 110 |
| Seq5 | \( V_{1a} \) 111 → \( V_{1a} \) 111 → \( V_{1a} \) 111 → \( V_{1a} \) 111 → \( V_{1a} \) 111 |
| Seq6 | \( V_{1a} \) 000 → \( V_{1a} \) 110 → \( V_{1a} \) 110 → \( V_{1a} \) 110 → \( V_{1a} \) 110 |
| Seq7 | \( V_{1a} \) 111 → \( V_{1a} \) 111 → \( V_{1a} \) 111 → \( V_{1a} \) 111 → \( V_{1a} \) 111 |
| Seq8 | \( V_{1a} \) 000 → \( V_{1a} \) 110 → \( V_{1a} \) 110 → \( V_{1a} \) 110 → \( V_{1a} \) 110 |

TABLE 3  The overlaps and the corresponding vector sequences

| Sector | Sequences | Sector | Sequences | Sector | Sequences |
|--------|-----------|--------|-----------|--------|-----------|
| i      | Seq1, Seq2 | iv     | Seq4, Seq7 | vii    | Seq5, Seq8 |
| ii     | Seq3, Seq4 | v      | Seq6, Seq7 | viii   | Seq3, Seq8 |
| iii    | Seq4, Seq5 | vi     | Seq5, Seq6 | ix     | Seq3, Seq6 |

Despite the overlap, the optimality of Seq7 in DEB holds because the nearest three vectors construct DEB. A similar conclusion applies to ΔCEA, where the Seq8 uses the nearest three vectors. However, except for ΔDEB and ΔCEA, the optimization of the vector sequence demands further analyses. Sector i (Figure 4) is taken as an example, which is covered by both Seq1 and Seq2. According to the voltage-second balance principle, the duty ratios of the vectors satisfy

\[
\begin{aligned}
V_{1a}d_1 + V_{2a}d_2 + V_{0a}d_0 &= n_{\alpha} \\
V_{1b}d_1 + V_{2b}d_2 + V_{0b}d_0 &= n_{\beta} \\
d_1 + d_2 + d_0 &= 1
\end{aligned}
\]

where \( n_{\alpha} \) is the voltage reference vector; Variables \( d_0, d_1, \) and \( d_2 \) are the duty ratios of vectors \( V_0, V_{1a}, \) and \( V_{2a}, \) respectively; Subscript \( \alpha/\beta \) mean the \( \alpha/\beta \)-axis components of the corresponding vectors.

The solutions to Equation (4) are

\[
\begin{aligned}
d_1 &= \frac{3n_{\alpha} - \sqrt{3n_{\beta}}}{V_{dc}} \\
d_2 &= 2\sqrt{3n_{\beta}}/V_{dc} \\
d_0 &= 1 - \left(3n_{\alpha} + \sqrt{3n_{\beta}}\right)/V_{dc}
\end{aligned}
\]

Figure 5 shows the current ripple of different vector timing sequences with a given reference. The mean value of the current ripple over the carrier period is zero. Since vector sequences are symmetric, the AC current ripple also shows symmetry within the first half carrier period. Thus, it is enough to do the analysis in the \( T_s/4 \) instead of \( T_s/2 \).

Based on Figure 5, the current ripple \( i_{\text{rip}} \) within a quarter of carrier period are

\[
i_{\text{rip}} = \begin{cases} 
\frac{\mu_{\text{err}_1}t}{L_s} & [0, t_1] \\
\frac{\mu_{\text{err}_2}t}{L_s} & [t_1, t_2] \\
\frac{\mu_{\text{err}_3}t}{L_s} & [t_2, T_s/4] 
\end{cases}
\]

where \( \mu_{\text{err}_1}, \mu_{\text{err}_2}, \) and \( \mu_{\text{err}_3} \) are the \( \alpha \)-axis components of the voltage vector errors during the intervals.
The current ripple $i_{\text{ripp}}$ within quarter of carrier period are

$$i_{\text{ripp}} = \begin{cases} 
\nu_{\text{err}1\beta}/L, & [0, t_1] \\
\nu_{\text{err}2\beta} (t - t_1)/L + \nu_{\text{err}1\beta} t_1/L, & [t_1, t_2] \\
\nu_{\text{err}3\beta} (t - T_s/4)/L, & [t_2, T_s/4]
\end{cases}$$

(7)

where $\nu_{\text{err}1\beta}$, $\nu_{\text{err}2\beta}$ and $\nu_{\text{err}3\beta}$ are the $\beta$-axis components of the voltage vector errors during the intervals.

For the Seq1, the vector errors $\nu_{\text{err}1\alpha}$, $\nu_{\text{err}2\alpha}$, and $\nu_{\text{err}3\alpha}$ are:

$$\begin{align*}
\nu_{\text{err}1\alpha} &= V_{\text{r1}\alpha} - u_{\alpha} = V_{dc}/3 - u_{\alpha} \\
\nu_{\text{err}2\alpha} &= V_{\text{r2}\alpha} - u_{\alpha} = V_{dc}/6 - u_{\alpha} \\
\nu_{\text{err}3\alpha} &= V_{\text{r3}\alpha} - u_{\alpha} = -u_{\alpha}
\end{align*}$$

(8)

and the vector errors $\nu_{\text{err}1\beta}$, $\nu_{\text{err}2\beta}$, and $\nu_{\text{err}3\beta}$ are:

$$\begin{align*}
\nu_{\text{err}1\beta} &= V_{\text{r1}\beta} - u_{\beta} = -u_{\beta} \\
\nu_{\text{err}2\beta} &= V_{\text{r2}\beta} - u_{\beta} = \sqrt{3}V_{dc}/6 - u_{\beta} \\
\nu_{\text{err}3\beta} &= V_{\text{r3}\beta} - u_{\beta} = -u_{\beta}
\end{align*}$$

(9)

For the Seq1, $t_1$, and $t_2$ in Figure 5(a) are:

$$\begin{align*}
t_1 &= d_1T_s/4 \\
t_2 &= d_1T_s/4 + d_2T_s/4
\end{align*}$$

(10)

For the Seq2, the vector errors $\nu_{\text{err}1\alpha}$, $\nu_{\text{err}2\alpha}$, and $\nu_{\text{err}3\alpha}$ are:

$$\begin{align*}
\nu_{\text{err}1\alpha} &= V_{\text{r1}\alpha} - u_{\alpha} = V_{dc}/6 - u_{\alpha} \\
\nu_{\text{err}2\alpha} &= V_{\text{r2}\alpha} - u_{\alpha} = V_{dc}/3 - u_{\alpha} \\
\nu_{\text{err}3\alpha} &= V_{\text{r3}\alpha} - u_{\alpha} = -u_{\alpha}
\end{align*}$$

(11)

and the vector errors $\nu_{\text{err}1\beta}$, $\nu_{\text{err}2\beta}$, and $\nu_{\text{err}3\beta}$ are:

$$\begin{align*}
\nu_{\text{err}1\beta} &= V_{\text{r1}\beta} - u_{\beta} = \sqrt{3}V_{dc}/6 - u_{\beta} \\
\nu_{\text{err}2\beta} &= V_{\text{r2}\beta} - u_{\beta} = -u_{\beta} \\
\nu_{\text{err}3\beta} &= V_{\text{r3}\beta} - u_{\beta} = -u_{\beta}
\end{align*}$$

(12)

To investigate the current ripple performance of Seq1 and Seq2, Equations (6)–(13) are submitted into Equation (3). Two current ripple examples are shown in Figure 6, where we select two reference voltages at $M = 0.4$ but with different angles ($15^\circ$ and $45^\circ$). Figure 6 is the current ripple locus under the $\alpha$-$\beta$ coordinate system, where the triangle $\Delta OP_1 P_2$ is the locus of Seq1 in the first $T_s/4$, and $\Delta OQ_1 Q_2$ is the locus of Seq2.

For Seq1, the line segments $| OP_1 |$, $| P_1 P_2 |$ and $| P_2 O |$ denote the current deviations caused by the voltage vector errors $V_{\text{err}-11}$, $V_{\text{err}-12}$, and $V_{\text{err}-0}$, respectively; For Seq2, the line segments $| OQ_1 |$, $| Q_1 Q_2 |$ and $| Q_2 O |$ denote the current deviations caused by the voltage vector errors $V_{\text{err}+12}$, $V_{\text{err}+11}$, and $V_{\text{err}+0}$. For synthesizing the reference voltage, Seq1 and Seq2 are identical. However, their current ripples vary on the vector angle; particularly, Seq2 results in a smaller current ripple at $15^\circ$; and the situation reverses at $45^\circ$ (see Figure 6).

The root mean square (RMS) value is an important index to evaluate AC current ripple. To generalize the results in Figure 6, we derive the carrier-period-based RMS value of the AC current ripple:

$$I_{\text{ripp RMS}} = \sqrt{\frac{4}{T_s} \int_0^{\frac{T_s}{4}} \frac{I_{\text{ripp}}^2}{I_{\text{ripp}}} \, dt} = \sqrt{\frac{4}{T_s} \int_0^{\frac{T_s}{4}} \frac{\frac{3}{2} \left( i_{\text{ripp}}^2 + i_{\text{ripp}}^2 \right)}{2} \, dt}$$

(14)
5 | PROPOSED LINE CURRENT RIPPLE REDUCTION USING OPTIMIZED COMMON-MODE VOLTAGE INJECTIONS

Section 4 develops the vector sequences with minimized switching times for the total current ripple reduction, which occupy different regions in the space-vector plane. It is significant to investigate how to implement the optimal sequences in the mainstream microcontrollers, which uses the carrier-based modulation approach to generate the gate signals. Due to the complementary operation of the lower and upper IGBTs, the development of the carrier-based modulation signal is usually focused on the upper IGBT. Figure 8 shows the carrier-based implementation of the parallel converter using two interleaved carriers, where the $d_a$, $d_b$, and $d_c$ denote the conduction duty ratios of $S_{11}/S_{21}$, $S_{13}/S_{23}$, and $S_{15}/S_{25}$, respectively. According to Figure 8(a), if the Seq2 is used (Subsector I in Figure 7), the following expression can be obtained:

$$\begin{align}
    d_a &= 1/2 - d_b / 2 = (u_{ra} - u_{rb}) / V_{dc} \\
    d_b &= 1/2 + d_c / 2 = (u_{rb} - u_{ra}) / V_{dc} \\
    d_c &= 0 = (u_{rc} - u_{ra}) / V_{dc}
\end{align}$$

(18)

where $d_a$, $d_b$, and $d_c$ are the same as that of (5); $u_{ra}$, $u_{rb}$, and $u_{rc}$ are the three-phase reference voltages.

According to Figure 8(b), if Seq3 is used (Subsector III), the three-phase carrier-based modulation signals are:

$$\begin{align}
    d_a &= 1 = 1 + (u_{ra} - u_{rc}) / V_{dc} \\
    d_b &= 1 - d_1 / 2 = 1 + (u_{rb} - u_{ra}) / V_{dc} \\
    d_c &= 1/2 - d_2 / 2 = 1 + (u_{rc} - u_{ra}) / V_{dc}
\end{align}$$

(19)

When Seq5 is used (Subsector V), the three-phase carrier-based modulation signals are:

$$\begin{align}
    d_a &= 1 = 1 + (u_{ra} - u_{rc}) / V_{dc} \\
    d_b &= 1/2 + d_1 / 2 = 1 + (u_{rb} - u_{ra}) / V_{dc} \\
    d_c &= 1/2 - d_2 / 2 = 1 + (u_{rc} - u_{ra}) / V_{dc}
\end{align}$$

(20)

If the reference is in the Subsector VII, the Seq7 is used, and the three-phase carrier-based modulation signals are:

$$\begin{align}
    d_a &= 1 = 1 + (u_{ra} - u_{rc}) / V_{dc} \\
    d_b &= 1/2 - d_1 / 2 = 1 + (u_{rb} - u_{ra}) / V_{dc} \\
    d_c &= d_1 / 2 = 1 + (u_{rc} - u_{ra}) / V_{dc}
\end{align}$$

(21)

With similar approaches, we calculate the current ripple RMS of the Seq3–Seq8 in the first 60° sector and obtain the optimal vector sequences for the minimized current ripple. The decision boundaries are shown in Figure 7(b), yielding eight subsectors, each pertains to a particular vector sequence.
Equations (18)–(21) reveal that the carrier-based modulation signals in the first 30° sector consist of two parts: (1) the three-phase reference voltages ($u_{ra}, u_{rb},$ and $u_{rc}$), which are identical across the regions, and (2) the common-mode voltage injections, which are different. In Subsector I, the common-mode injection is $-u_{rc}$; in Subsectors III, V and VII, the common-mode injection is $V_{dc} - u_{ra}$.

In the first 30° sector, $u_{rc}$ is the minimal one of the three-phase references, and $u_{ra}$ is the largest one. Equation (18) can be further unified as

$$d_c = (u_{rc} - u_{r, \text{min}}) / V_{dc}$$  \tag{22}

where $u_{r, \text{min}}$ is the minimal one of three-phase references.

Similarly, Equations (19), (20) and (21) are unified as:

$$d_c = (u_{rc} + V_{dc} - u_{r, \text{max}}) / V_{dc}$$  \tag{23}

where $u_{r, \text{max}}$ is the maximum one of three-phase references.

Similarly, the carrier-based three phase modulation signals in the Subsector II are developed

$$d_c = (u_{rc} + V_{dc} - u_{r, \text{max}}) / V_{dc}$$  \tag{24}

The carrier-based three phase modulation signals in the Subsector IV, VI and VIII are

$$d_c = (u_{rc} - u_{r, \text{min}}) / V_{dc}$$  \tag{25}

Note that the proposed CM voltage injections in Subsectors I, IV, VI and VIII are equivalent to that of the DPWMMAX method, i.e., injecting $V_{dc} - u_{r, \text{max}}$; whereas the injections in Subsectors II, III, V and VII amounts to the DPWMMIN strategy, where the injections are consistently set to $-u_{r, \text{min}}$. Equations (22)–(25) further reveal that different subsector should use the optimized common mode injections; the common mode injections in the first 30° sector are different from that in the second 30° sector. The common-mode voltage injection of DPWMMAX or DPWMMIN is not optimal for the voltage vector error reduction. However, with the optimized common-mode injections, the proposed method achieves the smallest possible current ripples without increasing the switching loss. In summary, the carrier-based modulation signals are:

$$d_c = u_{rc}^* + u_{cm}^*$$  \tag{26}

where $u_{cm}^*$ is the CM voltage injection; $u_{rc}^* = u_{rc} / V_{dc}$; $u_{cm}^* = u_{cm} / V_{dc}$.

The optimal common-mode voltages depend on the subsectors. It is, therefore, essential to develop a sector identification method. Taking the first 60° sector as an example, the boundary between Subsectors I and III is

$$u_{ra}^* - u_{rc}^* = 1/2$$  \tag{27}

If $u_{ra}^* - u_{rc}^* > 1/2$, we inject $V_{dc} - u_{ra}^*$; else inject $-u_{ra}^*$.

Similarly, the boundary of Subsectors II and IV is

$$u_{ra}^* - u_{rc}^* = 1/2$$  \tag{28}

If $u_{ra}^* - u_{rc}^* > 1/2$, we inject $-u_{rc}^*$; else inject $V_{dc} - u_{ra}^*$.

Note that the boundary of 0–30° sector and 30–60° sector is $u_{rb} = 0$. If $u_{rb}^* < 0$, reference is in the 0–30° sector; else the reference is in 30–60° sector.

In addition, we investigate the boundary conditions of the subsectors in the remaining vector plane (60–360°) and develop a simple flow chart to select the optimal common-mode injections, which is shown in Figure 9, where $u_{rmid}$ is the middle one of three-phase references.
PERFORMANCE COMPARISONS BETWEEN CONVENTIONAL STRATEGIES AND PROPOSED CMJPWM STRATEGY

We compare CMJPWM to the conventional methods to complete the review in Section 3.

As discussed in Section 3, when evaluating the current ripples, it is essential to adjust the switching frequency to ensure the identical switching loss. Therefore, the resultant frequencies of conventional methods should be normalized to the switching frequency of the CMJPWM ($f_\text{s} = 1/T_s$): the resultant switching frequency of HBPWM should be $f_\text{s}/2$; the CSVM, AZSPWM, MDPWM, and ICPSPWM have a resultant switching frequency of $2f_\text{s}/3$. The resultant switching frequency of the 3LPWM depends on the modulation index. If the modulation index is $<2/3$, the frequency is set to that of the CSVM. If the modulation index is $>2/3$, the equivalent frequency is set by

$$f_{\text{eq-M}} = \frac{4}{3}f - \frac{2}{\pi} f \arcsin\left(\frac{\sqrt{3}}{3M}\right). \quad (29)$$

Equation (29) tells that in the high modulation region where the track of the reference in the first $60^\circ$ is exclusively located in the Subsectors VII and VIII, the 3LSVM is equivalent to the proposed CMJPWM strategy.

With the normalized frequency, we investigate the AC current ripples under the conventional methods and calculate the carrier-period-based RMS values defined by Equation (14) using a similar approach introduced in Section 4. Figure 10 shows the results under different modulation indexes ($M = 0.3, 0.6, \text{and } 0.9$), which demonstrate that the proposed CMJPWM is superior to the methods except HBPWM in terms of the carrier-period-based RMS defined by Equation (14). In addition, Figure 10 reveals the CMJPWM has a better performance than that of HBPWM when $M = 0.3$; there are some intersections between the HBPWM and the CMJPWM in high modulation region. The indicator defined by Equation (14) has its limit when evaluating the performance of the HBPWM and the CMJPWM.

It is essential to investigate the current ripple in the whole fundamental period, evaluating the current quality of a modulation strategy. Thus, the fundamental-period-based RMS of the current ripple is a key parameter, which is defined as Equation (30) and is a function of $M$ only:

$$i_{\text{ripRMS}}(M) = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i_{\text{ripRMS}}^2(T_s-M, \theta) \, d\theta} \quad (30)$$

We calculate the RMS values defined by Equation (30) of the proposed method and the conventional methods and obtain that of the ICPSPWM through a simulation in Matlab. It can be seen from Figure 11 that the proposed CMJPWM has much lower RMS values than the methods except HBPWM in the whole modulation region; the proposed CMJPWM has a lower RMS value than the HBPWM except the region where $M$ ranges from 0.6 to 0.85; when $M$ ranges from 0.6 to 0.85, the RMS values of the CMJPWM is close to that of the HBPWM. Therefore, in most of the modulation region, the proposed CMJPWM has a lower AC current ripple than the HBPWM.

In addition, the ZSCC is another critical indicator of the paralleled converter, which determines the size of the CM inductor. We also compare the ZSCC of the proposed CMJPWM to that of the conventional methods. Figure 12 demonstrates that the CSVM and HBPWM have the largest ZSCC peak, which is $2.25 \times$ larger than that of the proposed CMJPWM; the other four methods have the minimal ZSCC peak, which is three-fourth of that of the proposed CMJPWM.

EXPERIMENT VALIDATION

The proposed CMJPWM strategy is implemented on an experimental prototype (see Figure 13), which is constructed by a TMS320F2808 DSP, IGBTs (SKM200GB12T4, SEMIKRON), IGBT gate drivers (SKYPER 32 PRO R, SEMIKRON), and DC-link capacitors (SHP-1100-400-FS, EACO). To focus on the modulation strategy validation, we configure the prototype shown in Figure 13 as a parallel interleaved inverter with a common DC-link and a three-phase resistive AC load. The DC-link voltage is built through a three-phase diode rectifier. Two common-mode inductors are used to be the three-phase filters and suppress the ZSCC. The main parameters of the prototype are shown in Table 4.

| Vdc | Icm | C   | R_load | f   |
|-----|-----|-----|--------|-----|
| 400V | 4mA | 1500μF | 25Ω    | 6 kHz |

The conventional PWM strategies CVSVM, AZSPWM, 3LSVM, MDPWM, ICPSPWM, HBPWM, and the proposed CMJPWM techniques are tested on the experimental prototype. In order to get the performance of the proposed CMJPWM in a wide modulation index range, we select two typical modulation
The carrier-period-based RMS of the current ripple under the proposed CMJPWM and the conventional methods (a) $M = 0.3$, (b) $M = 0.6$, (c) $M = 0.9$

The experimental prototype

The fundamental-period-based RMS values of the current ripple indices ($M = 0.3$ and $0.7$). Figures 14–27 show the experimental results containing the line current, the current ripple, and the ZSCC of the PWM methods under evaluation. The experimental results when $M$ is 0.3 are presented in Figures 14–20. It can be seen from the current ripple results in Figures 14–20 that the proposed CMJPWM can effectively reduce the AC current ripple of the existing PWM methods. The ZSCC results verify the analysis in Section 6 that the proposed CMJPWM has a small ZSCC peak in the lower modulation region than the conventional PWM methods. The experimental results when $M$ is 0.7 are presented in Figures 21–27. It is clear that the AC current ripple of the CMJPWM strategy is the same as that of HBPWM, and both are smaller than CSVM, AZSPWM, ICPSPWM, and 3LSVM. Besides, when compared to the HBPWM, the ZSCC of the proposed CMJPWM is significantly smaller. The results shown in Figures 21–27 are in good agreement with the analysis in Section 6.

To further validate the theoretical analysis in Section 6, more tests are conducted with modulation indices, and the results are shown in Figures 28 and 29. Figure 28 shows that among the conventional methods, HBPWM has a smaller line current ripple than CSVM, AZSPWM, ICPSPWM, 3LSVM, and MDPWM, and Figure 29 shows that AZSPWM, ICPSPWM, 3LSVM, and MDPWM have a smaller ZSCC peak than that of HBPWM. According Figures 28 and 29, the proposed CMJPWM achieves as good line current ripple as HBPWM, both of which are smaller than CSVM, AZSPWM, ICPSPWM, 3LSVM, and MDPWM. Besides, the proposed CMJPWM significantly reduces the overly large ZSCC peak of the HBPWM. When compared to the AZSPWM, ICPSPWM, 3LSVM, and MDPWM, the proposed CMJPWM has a much smaller line current ripple, and its ZSCC peak is close to those of AZSPWM,
ICPSPWM, 3LSVM, and MDPWM. Therefore, Figures 28 and 29 confirm that the proposed CMJPWM achieve a better compromise between line current ripple and ZSCC peak than conventional methods.

8 | CONCLUSION

This paper proposes a common-mode voltage injection-based pulse width modulation (CMJPWM) method to optimize the
AC current ripple of the paralleled interleaved converter. We investigate the available vector sequences of the paralleled converter and propose eight candidate vector sequences with minimized switching times. To implement the optimal vector sequences, we split the first $60^\circ$ sector into eight subsectors, each of which should use the optimal vector sequence with the minimized current ripple. The carrier-based modulation signals reveal that the optimal common-mode injection into the
FIGURE 22 Experimental result of AZSPWM when $M$ is 0.7 (a) three-phase line current, (b) total current ripple, (c) ZSCC

FIGURE 23 Experimental result of MDPWM when $M$ is 0.7 (a) three-phase line current, (b) total current ripple, (c) ZSCC

reference enables optimal vector sequences. With such adaptive CM injection, we name the proposed method CM voltage injection PWM (CMJPWM) strategy. The comparisons between the proposed CMJPWM and the conventional methods reveal that under the same switching loss, the proposed CMJPWM has better AC current ripple performance than the methods except for HBPWM. When compared to the HBPWM, the proposed CMJPWM achieves the smaller current ripple in the

FIGURE 24 Experimental result of ICPSPWM when $M$ is 0.7 (a) three-phase line current, (b) total current ripple, (c) ZSCC

FIGURE 25 Experimental result of 3LSVM when $M$ is 0.7 (a) three-phase line current, (b) total current ripple, (c) ZSCC
major region. If the modulation ranges from 0.6 to 0.85, the current ripple of the HBPWM is close to that of the CMJPWM. Meanwhile, the ZSCC of the CMJPWM is much smaller than that of the HBPWM over the entire modulation region. Therefore, the overall performance of the CMJPWM is better than that of the HBPWM. The experimental results verify the theoretical analysis and the effectiveness of the proposed CMJPWM strategy.

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