Ternary Logic with Stateful Neural Networks Using a Bilayered TaO$_x$-Based Memristor Exhibiting Ternary States

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A memristive stateful neural network allowing complete Boolean in-memory computing attracts high interest in future electronics. Various Boolean logic gates and functions demonstrated so far confirm their practical potential as an emerging computing device. However, spatio-temporal efficiency of the stateful logic is still too limited to replace conventional computing technologies. This study proposes a ternary-state memristor device (simply a ternary memristor) for application to ternary stateful logic. The ternary-state implementable memristor device is developed with bilayered tantalum oxide by precisely controlling the oxygen content in each oxide layer. The device can operate 157 ternary logic gates in one operational clock, which allows an experimental demonstration of a functionally complete three-valued Łukasiewicz logic system. An optimized logic cascading strategy with possible ternary gates is ≈20% more efficient than conventional binary stateful logic, suggesting it can be beneficial for higher performance in-memory computing.

1. Introduction

Conventional computing systems suffer from the von Neumann bottleneck problem, which has resulted from the drastic increase in data transfer rates between memory and logic units. To address this, in-memory computing (or near-memory computing) techniques that do not require a data bus have received significant interest in efforts to develop next-generation computing.\cite{1-4} Among the various solutions that have been proposed,\cite{5-7} memristive stateful logic is considered quite promising.\cite{8-16} It utilizes the resistance values stored in the memristor cells as logical variables and performs logic operations inside the memristor array by applying appropriate operating voltages to selected cells. As a result, the logical output can be stored in a defined location in the array. In this way, no data transfer is needed for logic operations, which allows complete in-memory computing most straightforwardly compared to all other technologies.

Multivalued computing is another interesting approach in next-generation computing. It utilizes more than two logical states for computing, compared with conventional Boolean logic (BL), which utilizes binary states, True (1) and False (0).\cite{17} Multivalued computing can increase computational efficiency by reducing the size of data. Jan Łukasiewicz proposed the first modern form of multivalued (or many-valued) logic in 1920.\cite{18} He added a third state between the two BL states (i.e., True and False) and theoretically suggested some ternary gates. Following his theory, we also use a ternary numeral system to express the ternary states: 0 (False in BL), 1, and 2 (True in BL).

The initial three-valued Łukasiewicz logic (Ł3) consisted of inversion (INV) and implication (IMP) gates. However, the logic was not functionally complete yet; their cascading could not reproduce all ternary gates. Later, it was found that introducing a so-called “T-function” (T()), which always produces the state 1 output regardless of the inputs, to Ł3 can realize the functionally complete algebra, which can be given as < E, IMP, INV, T(), 0, 2>, where E = \{0, 1, 2\}.\cite{19-21} This confirmed that ternary logic could be used in computing.

Since then, studies have proposed various devices to implement ternary logic systems.\cite{22-26} Among these studies, some have dealt with the ternary logic using a memristive crossbar array.\cite{27-31} This previous memristive ternary logic was achieved in a nonstateful manner; the form of inputs were voltages, not the resistances of the cells. In more detail, the multivalued states were provided by the voltage amplitudes, which can be produced at the periphery circuits. Therefore, these methods can be considered to belong to the near-memory computing regime.\cite{34}

Ternary memristive in-memory computing is possible only if the memristive cell supports ternary states, which has not been demonstrated yet. Even though some studies have proposed multilevel states in some memristive systems, a more detailed strategy is needed to realize memristive ternary logic.
In this study, we propose a reliable ternary-state memristor system which is capable of achieving ternary logic in a stateful logic manner. The device is composed of a bilayer of tantalum oxides, and it exhibits three distinct and stable resistance states, which permit the ternary states to be realized with resistance. In our investigation based on a stateful neural network theory, 157 ternary gates are theoretically executable in one voltage clock with the device. Afterward, we experimentally demonstrated functionally complete three-valued Łukasiewicz logic gates and the ternary full adder operations. We examined that the ternary full adder was about 20% more efficient than a state-of-the-art binary full adder.

2. Ternary State Memristor Device

Ternary stateful logic requires a memristor with three discrete states (namely, a high resistance state (HRS), an intermediate resistance state (IRS), and a low resistance state (LRS)). Also, the transition between the states should be sharp to ensure a clear distinction between the states. To meet the requirements, we theoretically devised a serial configuration of two distinct memristive components (M1 and M2). We designated the low and high resistance states of M1 as ON1 and OFF1, respectively, to distinguish them from the total resistance states (HRS, IRS, and LRS) and similarly designated ON2 and OFF2 for M2.

For the direct transition between states, the specification of the two memristors should satisfy the following conditions. One (i.e., M1) should have a higher OFF1 resistance and a lower set voltage than the other (i.e., M2). Then, in the M1-M2 serial configuration, when the applied voltage (V_app) is increased from the HRS (i.e., the OFF1-OFF2 states for M1-M2), most of the V_app is applied to the M1 as R_OFF1 >> R_OFF2, and thus, M1 can be set-switched first. Once the M1 becomes ON1, the V_app will be redistributed by a voltage divider. If the redistributed voltage across M2 is still lower than the set voltage of M2, the overall device state will be stable at ON1-OFF2, which corresponds to the IRS. Then, increasing the V_app will eventually set-switch the M2, resulting in ON1-ON2, the LRS.

To realize the desired serial memristor configuration in a single device, we employed a conventional bipolar-type Ta/TaOx/Pt memristor system and formed the TaOx layer as two layers with different oxygen contents and layer thickness. We tried various combinations of oxygen contents and thickness of the two layers to optimize the system and found the optimum device stack (see Note S1 and Figure S1 in the Supporting Information).

Figure 1a shows a schematic of the optimized Ta/TaOx_/TaOx+/Pt stack (top panel) and its transmission electron microscopy (TEM) image (bottom panel). The upper TaOx_- and lower TaOx_+ layers were deposited with O2/Ar gas flow ratios of 0.15 and 0.3, and thicknesses of 9 and 3 nm, respectively. Due to the different O2 partial pressure during deposition, the two layers contained different amounts of oxygen in the film. The X-ray photoelectron spectroscopy (XPS) analysis of the Ta 4f spectra determined that X= ~1.6 and X+ = ~1.9 as shown in Figure 1b, meaning both layers were oxygen-deficient and TaOx_- was more oxygen-deficient than TaOx_. The energy levels of the four peaks related to Ta4f7/2 were 26.8 ± 0.1 eV for Ta5+, 25.3 ± 0.2 eV for Ta6+/5+, 23.6 ± 0.2 eV for Ta4+, and 22.3 ± 0.2 eV for Ta3+. Each Ta 4f5/2 peak is 1.9 eV higher than each Ta 4f7/2 peak. The area ratio of the doublet was 1 (for 4f5/2) : 1.3 (for 4f7/2). The FWHM (full width at half maximum) of all peaks was applied equally with 1.73 eV. The bottom table panel shows the atomic percentage of each peak. The O 1s spectra of both layers are shown in Figure 1c, of which results are consistent with the Ta 4f spectra. The blue peak located at 530 eV (O1) and the green peak at 531 eV (O2) are related to Ta-O bonding in a stoichiometric Ta2O5 and oxygen-deficient one, respectively. The area ratio of O1 (blue)/O2 (green) is 3.57 in the TaOx_-, and 5.0 in the TaOx_+, confirming TaOx_+ is more oxygen-deficient.

We integrated the cell at the crossbar device to demonstrate the stateful logic. Figure 1d shows an optical microscopy image of the 16 x 16 crossbar array device. The line width at the cross-point is 5 µm, so the device area is 5 x 5 µm². Figure 1e shows the resistance switching I-V curves of the optimized ternary state memristor after electroforming with a 700 µA of compliance current (I_CC). It shows a drastic set switching from HRS to IRS at 0.64 V, and from IRS to LRS at 0.78 V, allowing a clear distinction between states. For the convenience of calculation, we defined the higher set voltage leading to LRS as V_SET and the lower set voltage as α V_SET (0 < α < 1), where α = 0.82 in the device. The two set voltages distributions were not overlapped during cycling, suggesting a reliable stateful logic operation is possible (The variations of the set voltages are shown in Figure S2, Supporting Information). Also, it shows a two-step set process. One of the set curves is highlighted, which shows a two-step reset from LRS to ~0.8 V and from to HRS at ~1.24 V. As the reset switching is gradual, the two-step reset switching is less distinguishable than the two-step set switching. In the stateful logic operation, only the first reset voltage is important, and the second one is unnecessary. Because once the reset switching is initiated, the device goes to the HRS spontaneously due to the node voltage increase by the voltage divider. For calculation, the reset voltage from LRS to HRS (V_RESET/I(H)) was normalized to ~1.02 V_SET. When the initial state was IRS, the reset voltage from IRS to HRS (V_RESET/I(H)) was decreased to ~0.66 V as shown in Figure 1e, which was normalized to ~0.84 V_SET for calculation. The reset voltage from the IRS is smaller than from the LRS because the filament in the IRS is weaker than the LRS. Also, the conductance of each state could be normalized to the conductance of the LRS; G IRS is 0.1 G LRS, and G IRS is 0.5 G IRS.

The double switching mechanism from the oxygen concentration-modulated TaOx_/TaOx_+ can be understood in Figure 1f. Figure 1f-i shows the pristine state of the device, where oxygen vacancies are drawn as blue dots. It shows a higher concentration of oxygen vacancies in the upper TaOx_- layer than in the lower TaOx_+ layer. After electroforming with a positive bias, a conical shape conducting filament was formed with a wider width at the upper side, as shown in Figure 1f-ii. With this filament configuration, the first reset switching destroys the filament in the bottom TaOx_+ layer where the filament is the weakest (Figure 1f-iii). Then, additional reset switching ruptures the filament in the TaOx_- layer from the bottom, resulting in the complete HRS (Figure 1f-iv). In the HRS, the 1st set switching at a V SET can partially rejuvenate the filament only in the upper TaOx_- layer because it contains more oxygen vacancies so forms the filament easily. This leads to the IRS (ON1 of M1 and OFF2 of M2) as shown in Figure 1f-v. At the IRS, additional voltage to V_SET completely set-switches M2, producing the LRS (Figure 1f...
Figure 1. A ternary-state bilayer tantalum oxide memristor device and its mechanism. a) The structure of the device and a cross-section TEM. (Scale bar: 50 nm) b) Ta 4f peak fittings of the XPS spectrum of the TaO$_{X^-}$ and TaO$_{X^+}$ layers, and the atomic percentage of each component derived as a result. c) O 1s peak fittings of the XPS spectrum of the oxide layers. d) Optical microscopic image of the 16 × 16 array (Scale bar: 200 μm). e) The $I$–$V$ characteristics of two switching cycles, one from HRS to LRS (blue) and the other from HRS to IRS (red). f) Schematic illustrations to show the oxygen vacancy distributions at each state. g) Retention characteristics of the LRS, IRS, and HRS at room temperature. h) Cycling endurance results. The inset shows the pulse timing sequence to read the ternary states.

-vi) again, which is the 2nd set switching. Or, the IRS can be reset switched to the HRS (Figure 1f -iv) by applying $V_{\text{RESET(I-H)}}$. The suggested model can also consistently explain other devices in Figure S1 (Supporting Information) made of various combinations of oxygen contents and thickness (see Note SI for more detailed discussion, Supporting Information). The conduction mechanism analysis results are included in Figure S3 (Supporting Information). All states showed ohmic or hopping conduction except for the Schottky conduction of HRS at high voltages, validating the proposed oxygen vacancy-mediated switching model in Figure 1e.$^{[90]}

To confirm the stability of the device required for the ternary stateful logic operation, retention and endurance characteristics of the device were investigated. Figure 1g shows the retention of all states up to $10^4$ s in room temperature, suggesting the device is viable for the ternary stateful logic demonstration. Figure 1h shows the cycling endurance of the device. The inset shows a pulse cycle to read the ternary states. All states were constant up to 6900 cycles and degraded to the HRS gradually. Although both retention and endurance performance should be improved for practical use, they were sufficient to validate the ternary stateful logic for this study.

3. Ternary Stateful Logic Gate Investigation via Stateful Neural Network

We investigated viable ternary stateful logic gates using the developed ternary memristor. Figure 2a shows a set of cells for executing the ternary stateful logic in the memristive crossbar array. The configuration and operating process are identical to conventional binary stateful logic, but have the ternary state cell characteristics. Figure 2b shows a representative $I$–$V$ curve of the ternary state memristor. Here, the HRS, IRS, and LRS are defined as states 0, 1, and 2, respectively. A stable IRS can be obtained at the applied voltage between $\alpha V_{\text{SET}}$ and $V_{\text{SET}}$. In this study, the output cell is initialized to HRS, and the logical output is obtained by a conditional (partial or full) set switching of it. Thus, the ternary gate operation would result in nonswitching (from 0 to 0) or partial switching (from 0 to 1) or full switching (from 1 to 2) of the output cell.

Sun et al. established a stateful neural network theory, expanded from the conventional binary stateful logic, a systematic method for finding possible stateful logic gates by drawing a decision boundary from the input state plot.$^{[9,51,52]}$ We adopted this methodology to find the possible ternary stateful logic gates. The
stateful neural network theory can be summarized as follows. For the three cell configuration in Figure 2a, the set switching condition for the output memristor (MO) is $V_O - V_{\text{NODE}} \geq V_{th}$, where $V_{\text{NODE}} = \frac{\sum_i G_i V_i}{\sum_i G_i}$ according to Kirchhoff’s current law, $\sum_i (V_i - V_{\text{NODE}}) G_i = 0$. By multiplying both sides by $\sum G_i$, which is always positive, the set switching condition can be organized to $\sum G_i w_i \geq 0$, where $w_i = V_O - V_i - V_{th}$. $\sum G_i w_i$ is the form of the weighted sum in the neural network, making the stateful logic a stateful neural network.

In the ternary state memristor, partial switching and full switching are sequential. Thus, the ternary gate operation, which utilizes both the partial and full switching, can be understood as two layers of the stateful neural network, as shown in Figure 2c. Here, $G_A$ and $G_B$ are two logical inputs in conductance, $G_{O,0}$, $G_{O,1}$, and $G_{O,0''}$ are the initial, interim, and final conductance of the output cell and $G_R$ is the conductance of the load resistor. Also, $w_{i1}$ (where $i = A, B, O', R$) is the weight connecting $G_i$ of the input neurons and $G_{O,0'}$ of the output neuron in the first layer. Here, $w_{i1}$ can be defined as $V_O - V_i - V_{th,1}$, where $V_{th,1}$ is $aV_{\text{SET}}$. Similarly, in the second layer, $w_{ij}$ (where $i = A, B, O', R$) is the weight connecting $G_{O,i}$ of the input neurons and $G_{O,i''}$ of the output neuron, and $V_{th,2}$ is $V_{\text{SET}}$.

Finding all of the operating voltage solutions for all ternary gates is a strenuous process. Before performing that, one can easily estimate if there are possible switching voltage solutions or not from the input state diagram, with decision boundary as shown in Figure 2d. In the diagram, two input conductances ($G_A$ and $G_B$) are assigned to the x and y-axis, and the desired logical output values are plotted corresponding to the gate. $G_{A,0}$, $G_{A,1}$, and $G_{A,2}$ (or $G_{B,0}$, $G_{B,1}$, and $G_{B,2}$) are the three conductance states of the input cell $M_A$ (or $M_B$) corresponding to state 0, 1, and 2, respectively. The open, gray, and black symbols represent the final state 0, 1, and 2 of the output cells, respectively. The diagram in Figure 2d shows a strong disjunction gate ($\oplus$) of Ł3 as an example, whose truth value can be expressed by $\oplus(G_{A,0}, G_A) = \min\{2, G_A + G_B\}$. By definition, the output of $(G_{A,0}, G_{B,0})$ should be 0, and
the output of \((G_{A,1}, G_{B,0})\) and \((G_{A,0}, G_{B,1})\) should be 1. Otherwise, the output should be 2. Here, the switching condition equation \((\sum G_{w} \geq 0)\) can be re-arranged into a linear equation \((G_{B} \geq a G_{A} + b G_{LRS})\), where \(a\) and \(b\) are arbitrary values, which corresponds to the boundary line dividing the diagram into two sections with respect to the output states. Then, two decision boundaries can be drawn; the first one distinguishes the output state 0 or 1 (red line), and the other one does state 1 or 2 (yellow line).

As such, one can easily determine if any gate is viable or not just by drawing two boundary lines in the input state diagram as in Figure 2d. A detailed methodology is discussed in Note SII and Figures S3–S7 (Supporting Information).

After surveying all cases satisfying the conditions, we concluded that 551 ternary gates out of 19 683 were potentially possible in one operational clock. We called them potential ternary gates (PTG). The 551 PTG were obtained by just considering the final state of the output cell in the input state diagram and neglecting the change of inputs. Thus, the input boundary conditions should be additionally considered to confirm whether the gate operation would not destroy the inputs. That is, the applied voltages across the input memristor cells \((v_{M})\) of 0 state should be lower than \(a V_{SET} (v_{M} < a V_{SET})\), an input of 1 should be higher than \(V_{RESET(L-H)}\) and lower than \(V_{SET} (V_{RESET(L-H)} < V_{SET})\), and an input of 2 should be higher than \(V_{RESET(L-H)}\) (\(V_{RESET(L-H)} < v_{M}\)).

After considering the input boundary conditions, we could determine that 157 gates satisfied both the input and output boundary conditions so were implementable in the given device. We called them “ternary unit gates (TUG)”. The number of TUG was sufficient to perform ternary computing (see Note SIII and Figures S8–S10 for more details, Supporting Information).

Figure 2e shows an experimental demonstration of one of the TUG, the strong disjunction gate. The black and red lines indicate the applied voltage pulses and the conductance of the cells, respectively. For better presentation, all voltages are normalized by \(V_{SET}\). After solving the inequality equations of the boundary conditions as shown in Figure S8 (Supporting Information), the operating pulse heights were selected to be \(-1.3 V_{SET}\) to \(V_{A}\) and \(V_{B}\), and 0.31 \(V_{SET}\) to \(V_{O}\) with 0.15 \(G_{LRS}\) to \(G_{R}\). The pulse widths at the maximum amplitude were 150 \(\mu s\), and rise time, and fall time were equally 50 \(\mu s\). At each panel, before and after applying the operating voltages, the initial states of \(G_{A}\), \(G_{B}\), and \(G_{O}\) and the final state of \(G_{O}''\) were sequentially read by 0.1 \(V_{SET}\) of read pulse. This confirmed that the strong disjunction gate operation was successful.

4. Execution of Stateful Three-Valued Łukasiewicz Logic and Full Adder

We experimentally demonstrated all of the required Łukasiewicz (Ł3) logic gates (i.e., \(0, 1,\) INV, IMP) as well as the \(T()\) using the integrated device in Figure 1C.[15] (Note that \(0\) (Bold zero) and \(1\) (Bold one) refer to the names of the gates that result in outputs 0 and 2, respectively.) The truth tables of the Ł3 gates and \(T()\) are shown in Figure 3a. The 0, 1, and \(T()\) gates are initialization...
Figure 4. Demonstration of an Ł3 implication (IMP) gate. a) Input state diagrams of each of the three clocks for the IMP gate. Each step is included in the ternary unit gates. b) Two-input-one-output configuration, and required voltages and resistors connected for each clock for the IMP gate operation. c) Experimental demonstration of the IMP gate for nine input cases of two ternary inputs. The read currents and operating voltages are shown in red and black, respectively.

gates that program the output cell to state 0, 2, and 1, respectively, regardless of the inputs. Thus, they can be achieved by applying 0.1 \( V_{\text{SET}} \) for 0, \( V_{\text{SET}} \) for 1, and 0.82 \( V_{\text{SET}} \) for T, as shown in Figure S11 (Supporting Information).

Figure 3b shows the input state diagram of the INV gate. The INV gate is a one-input-one-output gate so that it needs only one dimension in the diagram. The INV gate belongs to the PTG but is not in the TUG, meaning the gate operation is possible for multiple clocks. Therefore, we executed it with two sequential clocks. Figure 3c,d shows the cell configuration and the experimental demonstration results, respectively. For the first clock, \( V_A \) and \( V_O \) were set to 1.09 \( V_{\text{SET}} \) and 1.5 \( V_{\text{SET}} \), respectively, which would result in a partial set switching of the output cell from 0 to 1, only if the input was 0 or 1. For the second clock, \( V_A \) and \( V_O \) were changed to 1.98 and 2.17 \( V_{\text{SET}} \), respectively, and it would switch the output cell from 1 to 2, only if the input was 0.

Next, the IMP gate of Ł3 was investigated. The IMP gate is also included in PTG but not in TUG, and thus it is executable by three sequential clocks. Figure 4a shows the input state diagram for the three clocks. Figure 4b shows the cell configuration for executing the IMP gate and the applied voltage conditions for each clock. Figure 4c shows the experimental data for all input
conditions, proving the IMP gate operation was successful. In this way, 19,683 of all two-input ternary gates can be realized through the cascading of Ł3 logic gates.

Next, we demonstrated a ternary full adder operation with the device. One of the advantages of stateful logic with a neural network is that it is easy to execute multi-input (more than two) gates such as carry-out and sum operations by selecting multiple word lines. In the binary stateful logic, both the carry-out and sum operations were possible with one clock per each using three and four inputs.\[^9\] Similarly, we investigated the most compact carry-out and sum operation sequences for executing the ternary full adder.

In our methodology, the first step in the gate investigation was to draw an input state diagram. However, multi-input gates require multiple dimensional spaces to express all input cases, which is complicated. Therefore, we reduced the dimensions of the input states with the following treatment. We defined a new parameter \( G_T \) to be the sum of all inputs \( (G_T = G_A + G_B + G_{Cin}) \), considering that the carry-out value is associated with the sum of the inputs. In this way, the 27 input cases could be reduced to 7, assuming the conductance ratios were \( G_{state1} \approx 0, G_{state3} = 0.5, \) and \( G_{state2} = 1.0 \) (see Figure S12 for the reduced truth table of the full adder, Supporting Information). Then, a 1D input state diagram can be drawn for the carry-out operation, as in Figure 5a.

In this diagram, if \( G_T \) is greater than or equal to \( 3G_{LRS} \), the output is 1, and if \( G_T \) is greater than or equal to \( 6G_{LRS} \), the output is 2. The two boundary conditions satisfied the switching rules so that they were executable with one voltage clock.

Next, the sum operation required at least three clocks and seven cells (i.e., four inputs, two caches, and one output). The cache cells were initialized to 0 before the operation for temporarily storing intermediary values for the first and second clocks. Those cache values can be deleted after the computation process finishes. For the first and second clocks, a 2D input state diagram can be drawn using \( G_{Co} \) and \( G_T \) as the two inputs, where \( G_{Co} \) is the output of the carry-out gate. Then, the decision boundaries for each clock can be drawn as in Figure 5b,c. With the first clock, the first cache was programmed to 1 only if a remainder of \( G_T/3 \) was 2. With the second clock, the second cache was programmed to 1 if a remainder of \( G_T/3 \) was 1 or 2. Then, with the third clock, the
strong disjunction gate operation with two buffers as inputs can complete the sum operation. The entire demonstration of the full adder can be found in Figure S13 (Supporting Information). In summary, the ternary full adder required 7 cells (i.e., three inputs, one output for carry-out, two caches for sum, and one output for sum) and 4 clocks (i.e., one for carry-out and three for sum). Alternatively, if the caches are reset initialized for subsequent use, the total number of required cells and clocks can be 5 and 5, respectively.

The efficiency of the developed ternary full adder was compared to that of a binary full adder. For the measure of efficiency, we adopted a spatiotemporal cost (STC) which is the value multiplying the number of required core cells and the number of clocks.\[^{[4,5,31]}\] For a fair comparison, it was considered an N-digit decimal number calculation task. Also, it was assumed that all bits were located along the same row. In binary stateful logic, Sun et al. proposed that the binary stateful full adder can be executable with 5 cells and 2 clocks, which was the most efficient full adder sequence.\[^{[9]}\] In this case, the STC value of the two-bit binary full adder is 10.

In an n-bit full adder, the carry-in value from the second bit comes from the carry-out of the previous bit. So only the first bit needs 5 cells and the second and next bits need additional 4 cells. Thus, the total number of cells is 4n+1, while the number of clocks is 2n. This results in 8n²+2n of the STC value of the n-bit full adder. Similarly, the proposed ternary stateful logic requires 4n+1 cells and 4n+1 clocks including the reset initialization clock at the end (see Figure S14 for resetting the cache cells to be reused through one extra clock, Supporting Information). Considering that the N-digit decimal number can be converted into an \(8.818N^2+6.64N\) for binary logic and \(70.56N^2+16.80N\) for ternary logic. When N is high enough, the linear term will be negligible and the ternary logic will be more efficient, by about 20%. Table 1 summarizes the comparison.

### Table 1. Comparison of the full adder execution in binary and ternary stateful neural networks.

|                      | Binary full adder (Sun et al.\[^{[9]}\]) | Ternary full adder (This work) |
|----------------------|------------------------------------------|-------------------------------|
| Clocks / Cells / STC for n digit adder | 2n / 4n + 1 / 2n \((4n + 1)\) | 4n + 1 / 4n + 1 / \((4n + 1)^2\) |
| Clocks / Cells / STC for addition of N-digits decimal number | 6.64N / 13.28N + 1 / \| 8.40N + 1 / 8.40N + 1 / \|

We fabricated a bilayered tantalum oxide memristor device that possessed discrete ternary states, and the switching between states was abrupt. This allowed us to implement ternary logic on the device via a ternary stateful neural network. Before the experimental demonstration, we investigated all possible ternary gates theoretically, utilizing an input state diagram and neural network-based classification methodology. Consequently, we concluded that 157 gates were possible in this device. Their optimized combinations and multi-input operation strategy ensured a functionally complete three-valued Łukasiewicz logic and enabled a ternary full adder operation about 20% efficiently than the binary stateful logic. The computational efficiency can be further improved by device parameter optimization. For example, if the amplitudes of the two reset voltages and \(V_{\text{SET}}\) are high enough, the sum operation can be possible with two clocks using \(G_{\text{T}}, G_{\text{C}},\) and \(G_{\text{C}}\) as inputs.

Although this study showed the feasibility of the ternary stateful logic, there are still challenges to resolve before it can be practically used. One of the most crucial issues is switching reliability, which is also associated with device-to-device and cell-to-cell variations. To solve those issues, it may be better to develop and apply error-correction methodologies for the ternary logic, similar to those employed with binary stateful logic.\[^{[53]}\]

### 5. Conclusion

We fabricated a bilayered tantalum oxide memristor device that possessed discrete ternary states, and the switching between states was abrupt. This allowed us to implement ternary logic on the device via a ternary stateful neural network. Before the experimental demonstration, we investigated all possible ternary gates theoretically, utilizing an input state diagram and neural network-based classification methodology. Consequently, we concluded that 157 gates were possible in this device. Their optimized combinations and multi-input operation strategy ensured a functionally complete three-valued Łukasiewicz logic and enabled a ternary full adder operation about 20% efficiently than the binary stateful logic. The computational efficiency can be further improved by device parameter optimization. For example, if the amplitudes of the two reset voltages and \(V_{\text{SET}}\) are high enough, the sum operation can be possible with two clocks using \(G_{\text{T}}, G_{\text{C}},\) and \(G_{\text{C}}\) as inputs.

### 6. Experimental Section

**Device Fabrication:** The Ta/TaO\(_x\)/TaO\(_x\)/Pt structure was fabricated using the following process. The bottom electrode (50 nm thick Pt) was deposited on a Ti(adhesion layer) /Si substrate by e-beam evaporation after photoresist pattern formation, and it was patterned by lift-off process. Afterward, two layers of tantalum oxide were deposited by reactive sputtering with various combinations of oxygen flow rates and thicknesses. The deposition conditions of the device used in this study were an Ar/O\(_2\) flow ratio of 0.15 and a thickness of about 9 nm for the TaO\(_x\)\(_{\text{---}}\) layer, and an Ar/O\(_2\) flow ratio of 0.3 and a thickness of about 3 nm for the TaO\(_x\)\(_{\text{+++}}\) layer. Then, the top electrode (120 nm thick Ta and 50 nm thick Pt for passivation) was formed by e-beam evaporation followed by lift-off patterning.

**Electrical Measurements:** All electrical testing was performed using a semiconductor analyzer (Keithley 4200A-SCS) and a probe station. The I–V characteristics were obtained in a DC sweep using two SMUs (Source Measurement Unit). The bottom electrode was ground while the top electrode was biased, and the current was read at the top electrode with a sweep rate of 0.8 V s\(^{-1}\). For the gate operation demonstration, voltage pulses were applied using a Keithley 4225-PMU (Pulse Measurement Unit) and 4225-RPM (Remote Amplifier/Switch). The pulse width was 150 µs, and the rise time, fall time, delay time, and hold time were all 50 µs.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Data Availability Statement**

The data that support the findings of this study are available from the corresponding author upon reasonable request.
