Analysis and Investigation of Hybrid DC–DC Non-Isolated and Non-Inverting Nx Interleaved Multilevel Boost Converter (Nx-IMBC) for High Voltage Step-Up Applications: Hardware Implementation

Mahajan Sagar Bhaskar  
*Prince Sultan University, Saudi Arabia*

Dhafer J. Almakhles  
*Prince Sultan University, Saudi Arabia*

Sanjeevikumar Padmanaban  
*Aalborg University, Denmark*

Frede Blaabjerg  
*Aalborg University, Denmark*

Umashankar Subramaniam  
*Prince Sultan University, Saudi Arabia*

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Authors
Mahajan Sagar Bhaskar, Dhafer J. Almakhles, Sanjeevikumar Padmanaban, Frede Blaabjerg, Umashankar Subramaniam, and Dan M. Ionel

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Analysis and Investigation of Hybrid DC–DC Non-Isolated and Non-Inverting Nx Interleaved Multilevel Boost Converter (Nx-IMBC) for High Voltage Step-Up Applications: Hardware Implementation

MAHAJAN SAGAR BHASKAR1, (Member, IEEE), DHAFER J. ALMAKHLES1, (Member, IEEE), SANJEEVIKUMAR PADMANABAN2, (Senior Member, IEEE), FREDE BLAABJERG2, (Fellow, IEEE), UMASHANKAR SUBRAMANIAM1, (Senior Member, IEEE), AND DAN M. IONEL3, (Fellow, IEEE)

1Renewable Energy Lab (REL), Department of Communication and Networks, College of Engineering, Prince Sultan University (PSU), Riyadh 11586, Saudi Arabia
2Center of Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark
3Power and Energy Institute Kentucky, Department of Electrical and Computer Engineering, University of Kentucky, Lexington, KY 40506, USA

Corresponding author: Mahajan Sagar Bhaskar (sagar25.mahajan@gmail.com)

This work was supported by the Renewable Energy Lab (REL), College of Engineering, Prince Sultan University, Riyadh 11586, Saudi Arabia.

ABSTRACT In significant cases, the generated voltage needs to be step-up with high conversion ratio by using the DC-DC converter as per the requirement of the load. The drawbacks of traditional boost converter are it required high rating semiconductor devices and have high input current ripple, low efficiency, and reverse recovery voltage of the diodes. Recently, the family of Multilevel Boost Converter suggested and suitable configuration to overcome the above drawbacks. In this article, hybrid DC-DC non-isolated and non-inverting Nx Interleaved Multilevel Boost Converter (Nx-IMBC) is analyzed in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) with boundary condition and investigated in detail. The Nx-IMBC circuit combined the features of traditional Interleaved Boost Converter (IBC) and Nx Multilevel Boost Converter (Nx-MBC). The modes of operation, design of Nx-IMBC and the effect of the internal resistance of components are presented. The comparison study with various recent DC-DC converters is presented. The experimental and simulation results are presented with or without perturbation in input voltage, output power and output reference voltage which validates the design, feasibility, and working of the converter.

INDEX TERMS DC-DC, high step-up, hybrid converter, interleaved, low voltage stress, low current ripples, multilevel, non-isolated, non-inverting, voltage multiplier.

I. INTRODUCTION

When the current world energy scenario is analyzed, all the nations of the world is riveted towards ingestion of exhaustible sources to beget the energy and to feed the energy requisites. The idea of energy generation is entirely unaffordable, which would eventually create paucity of fossil fuels soon. As a result, the entire focus has increasingly shifted towards inexhaustible energy sources [1]–[5]. There are so many ways to generate power using these sources like solar, wind, fuel-cell, tidal etc. Among these sources, solar energy is one of the conventional renewable sources due to abundance,
eco-friendly, free of cost and continuously developing with the advancement in photovoltaic cells which is leading to the high efficiency of the solar system. Photovoltaic technology is tenaciously growing with betterment in photovoltaic cells which ultimately leads to the priceless powered nation and the world too [6]. More and more renewable energy sources such as solar arrays, wind turbines, and fuel cell stacks are widely employed for front-end DC/DC applications [7], [8]. These inexhaustible energy sources need a DC-DC converter with a high conversion ratio to augment the voltage magnitude to feed the power grid or power DC-AC converter (Inverter) [9], [10]. The solar arrays give out low output voltage which certainly cannot suffice the voltage requisite. Therefore, the low voltage fed to boost converter to inflate the voltage level to suffice the application requirements [11]–[13]. A traditional Boost converter (Fig. 1(a)) is not preferred practically to fulfill the high voltage demand due to its design constraints, low efficiency and diode reverse recovery problem etc. [14], [15].

For attain a high voltage conversion ratio, many DC-DC converters with the different boosting technique are reviewed in [16]. Isolated topologies introduce transformer, results in bulky and costly circuitry [17], [18]. Unfortunately, a significant voltage spike across the switch observed due to leakage...
inductance of the transformer. Thus, energy regeneration and clamping techniques are employed to recycle the energy and to limit the voltage stress [19], [20]. However, these techniques make the circuit complex and increase the cost of the converter. Coupled Inductor employed in the converter, e.g., coupled inductor-based boost converter [21], three winding coupled inductor [22], [23] to attain high voltage conversion ratio. However, additional input filter and active clamped techniques are required to minimize the input current ripple when turns ratio increased to meet desired voltage level, and complex structure is the main drawbacks of these converters [24], [25]. Interleaved converters based on coupled inductor are proposed to attain higher voltage conversion ratio with minimum input current ripple and higher efficiency [26], [27]. Nevertheless, complicated design, control, winding arrangement, and high frequency coupled inductor are the main challenges for these converters.

Numerous non-isolated converters are proposed to achieve high voltage conversion ratio without using a transformer and coupled inductor [28], [29]. Several existing DC-DC converter topologies are analyzed, and the power circuits of DC-DC converter topologies are depicted in Fig. 1 and their voltage conversion ratio is given in the Table-1. Cascaded Boost Converter (CBC) and Quadratic Boost Converter (QBC) are employed in [29], [30], whereas the method of cascading the necessary converters causes very high voltage stresses across the switches. Moreover, the efficiency is likely to get lessened with rising stages because of the several synchronous control switches and semiconductor device losses. In QBC (Fig. 1(b)), when the control switch turned OFF, the voltage across control switch is equal to the output voltage. Thus, high voltage rating control switch is required to design QBC, which increases the cost and decreases the efficiency of the converter due to higher conduction and switching losses [31]–[33].

Switched Capacitor (SC) and Switched Inductor (SI) are other possible solutions to increase the voltage conversion ratio of the converter. In [34], SI is employed in boost converter to step up the voltage. However, the voltage conversion ratio is not improved by several times and the voltage stress across the switch is equal to the output voltage. To overcome this drawback, several DC-DC converters, e.g. Three-level boost converter, Quadratic Three-level converter, converter using a bootstrap capacitor and inductor, switched capacitor boost converter are proposed [28], [35], [36]. However, the converter voltage conversion ratio is not enhanced by a higher factor even though multiple switches and boosting stages are employed. A high voltage converter is proposed in [37] using several reactive stages. However, it required a large number of inductors, capacitor and diodes.

For overcome the abovementioned drawback, the ground-breaking solution is voltage multipliers to raise the output voltage, which is the most affordable and frugal way to increase the gain of the converter [38]. Non-inverting, as well as inverting boost converter topologies with a combination of the traditional converter with voltage multiplier, are discussed [39]. Later, in [40] Nx inverting configuration of the boost converter is also recommended for photovoltaic DC Link applications. These multiplier boost converter topologies provide a practical solution to intensify the voltage conversion ratio. The multilevel DC-DC converters circuit avail Cockcroft Walton (CW) voltage multiplier which can be a crucial solution for the voltage conversion ratio intensification. Fig. 1(k) and 1(l) show the power circuit of Nx Multilevel Boost Converter (Nx MBC) and Nx Multilevel Buck-Boost Converter (Nx MBBC), respectively [38]–[40]. Reactive elements incorporated in the power converter topology, and operating frequency holds a pivotal role in the designing of the reactive element. Lower magnitudes of reactive components along with high switching frequency serves an acceptable magnitude of the output voltage. However, it also produces a noticeable amount of ripple at the input side.

For clarify the issue of current ripple across the inductor, the value of inductance designed according to application requirement, which may increase the cost, size of the converter and its transient response time. In the original, the configuration of the interleaved structure of positive output multilevel converter for two levels (parallel connected at both input side and load side) is discussed to minimize

| Converter Topology | Voltage Conversion Ratio, D= Duty Cycle |
|-------------------|---------------------------------------|
| Traditional DC-DC Boost Converter | 1/(1-D) |
| Switched Inductor (SI) DC-DC Boost Converter | (1-D)/(1-D) |
| Single switch DC-DC Quadratic Boost Converter (QBC) | 1/(1-D)² |
| Traditional Three-Level DC-DC Boost Converter | 2/(1-D) |
| Quadratic Three-Level DC-DC Boost Converter | 1/(1-D)² |
| Converter using bootstrap capacitors and boost Inductors | 3/(1-D) |
| Switched Capacitor Based DC-DC Boost Converter | (1-D)/(1-D) |
| 2-phase quadrupled interleaved Boost Converter (IBC) | 4/(1 − D) |
| High-voltage gain 2-phase Interleaved Boost Converter (IBC) using one VMC (Voltage Multiplier Cell) | (VMC + 1)/(1 − D) |
| Extra-High Voltage (HV) DC-DC Converter | 4/(1-D) |
| Nx Multilevel Boost Converter (Nx MBC) | N/(1-D) |
| N-level Multilevel Buck Boost Converter (MBBC) | (N-D)/(N-D) |

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the input current ripple and the size of the passive components [39], [41]. However, the only circuitry suggested, and the work extended to another CW multiplier based high gain interleaved DC-DC converter with centralized source using negative and positive multiplier for input ripple cancellation (parallel connected at the input side and series-connected at output side) [39], [41], [42] to attain high voltage conversion ratio with minimum input ripple. Two input boost stage interleaved converters [43] is proposed to attain high voltage conversion ratio with minimum input ripple. However, in [43], two sources and load capacitor with a high voltage rating increases the cost of the converter. Modified Dickson charge pump is used to achieve high step-up voltage by reducing the number of semiconductor devices [44]. However, the converter is limited in the number of stages, and further addition of more number of levels is not possible to achieve high voltage as per requirement. Also, the high rating output capacitor is required to attain a constant output voltage. In [45], the structure of 2x interleaved multilevel converter [39] is extended for higher levels (N), and four different modes of operation are suggested with simulation results for renewable energy applications to boost the voltage with high conversion ratio. In [45], the interleaved multilevel structure is obtained from two same Nx multilevel DC-DC converters [38] connected in parallel at the input side and combined at output side and operated at a higher duty cycle. It reduces the current rating of the components as well as reduces the input current distortion compared to Nx-MBC suggested in [38].

In light of the advantages of interleaved structure and voltage multiplier, this article contributes to the following: Detail analysis and investigation of a non-isolated Nx Interleaved Multilevel Boost Converter (Nx-IMBC) with hardware implementation for different operation modes to achieve high output voltage and minimum input ripples. Possible modes of operation are discussed with analysis of CCM and DCM boundary condition. The effect of internal inductor resistance and semiconductor devices is analyzed in detail. The design of reactive components and the selection of semiconductor devices are discussed. The comparison of the suggested converter and recently addressed converter is provided in detail to show the benefits. The performance of Nx-IMBC converter is tested through numerical simulation and hardware implementation of 100W three-level prototypes with or without perturbation in input voltage, output reference voltage and power.

This article is structured as follows: Introduction and several existing derived DC-DC converters, the motivation of converter, and the main contribution are discussed in section-I. The circuit description, modes of operation (CCM and DCM) of hybrid non-isolated and non-inverting Nx-IMBC are discussed in section-II. The effect of inductor internal resistance and semiconductor devices on a voltage conversion ratio of Nx-IMBC, steady-state analysis for CCM and DCM, efficiency and power losses are provided in section III. Various range of operation and waveforms discussed in section IV. The design, current and voltage stress, and selection of semiconductor devices for Nx-IMBC are explained in section-V. Also, comparison of Nx-IMBC with recently addressed converters is provided in section V. Experimental and numerical simulation results of Nx-IMBC are discussed with applications in section-VI. Finally, based on the detailed investigation of obtained experimental and simulation results, the conclusion is provided in section-VII.

II. HYBRID DC-DC NON-ISOLATED AND NON-INVERTING Nx INTERLEAVED MULTILEVEL BOOST CONVERTER (Nx-IMBC)

A. CIRCUIT DESCRIPTION OF Nx-IMBC

Hybrid DC-DC non-isolated and non-inverting Nx-IMBC power circuit is depicted in Fig. 2. Nx-IMBC circuitry combines the features of traditional Interleaved Boost Converter (IBC) and Cockcroft Walton (CW) voltage multiplier. 3N2 capacitors, 4N=2 diodes, two equal rated inductors along with 2 power switches are required to design circuitry of Nx IMBC, where N is the number of levels at the output side. Nx-IMBC provides N times conversion ratio \((N/(1−D))\) compared to traditional boost converter and same ratio as compared to Nx MBC. Fig. 3(a)-(d) show the graph of the required number of capacitors, diodes, inductor and switches versus the number of levels, respectively.

![Figure 2. The power circuit of Nx IMBC.](image-url)
3) N-times high voltage conversion ratio compared to traditional Boost converter (N is the number of levels),
4) Low input current and output voltage ripple,
5) Suitable to feed MLI due to capacitor stack, and
6) Voltage stress across semiconductor devices is low.

Additionally, Nx-IMBC circuitry is simple, and the number of output levels can be easily increased by adding diode-capacitor circuitry to increase the voltage conversion ratio. The output voltage is calculated by adding the voltage across output side capacitors $C_1$, $C_2$, ..., and $C_N$ as follows,

$$V_O = V_{C1} + V_{C2} + \ldots + V_{CN} = \sum_{r=1}^{N} V_{Cr}$$  \hspace{1cm} (1)

**B. THE POSSIBLE STATES IN CONTINUOUS CONDUCTION MODE**

To explain the states of operation, 3x Interleaved Multilevel Boost Converter (Nx-IMBC with $N = 3$) is assumed with ideal components, capacitors are large enough to provide constant voltage, and the circuit operated in Continuous Conduction Mode (CCM). The proposed converter can exercise in four states of operations.

1) **STATE-1: WHEN SWITCHES $S_1$ AND $S_2$ ARE ON**

When the switches ($S_1$ and $S_2$) are ON, inductors $L_1$ and $L_2$ magnetized from the input source ($V_{in}$), and the capacitors $C_1$, $C_2$ and $C_3$ are discharged through the load ($R_o$).

The voltage across the capacitors make diodes $D_{21}$, $D_{22}$, $D_{41}$ and $D_{42}$ forward biased and the load side capacitors $C_1$, $C_2$ discharged through the path of diodes to charge capacitors $C_{21}$, $C_{22}$ and $C_{31}$ and $C_{32}$, respectively. Fig. 4(a) shows the equivalent power circuit when both the switches $S_1$ and $S_2$ are ON. In this mode, diodes $D_{11}$, $D_{12}$, $D_{31}$, $D_{32}$, $D_{51}$ and $D_{52}$ are reversed biased. The voltage across inductors and capacitors are calculated as follows,

$$V_{L1} = V_{L2} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = V_{in}$$

$$V_{C21} = V_{C22} = V_{C31}$$

$$V_{O} = V_{C1} + V_{C2} + V_{C3}$$

2) **STATE-2: WHEN SWITCH $S_1$ IS ON, AND SWITCH $S_2$ IS OFF**

The equivalent power circuit when switch $S_1$ is ON and switch $S_2$ is OFF is depicted in Fig. 4(b). The inductor $L_1$ is magnetized from input voltage ($V_{in}$) and at the same time, the capacitors $C_1$, $C_2$ and $C_3$ charged by inductor $L_2$ and capacitors $C_{22}$ and $C_{32}$. The inductor $L_2$ and capacitors $C_{22}$ and $C_{32}$ also charge capacitors $C_{21}$, $C_{31}$ of the multiplier cell and provides energy to load ($R_o$). In this mode, diodes $D_{11}$, $D_{31}$, $D_{51}$, $D_{22}$, $D_{42}$ are reversed biased, and diodes $D_{21}$, $D_{41}$, $D_{12}$, $D_{32}$ and $D_{52}$ are forward biased. The voltage across...
inductors and capacitors are calculated as follows,

\[
\begin{align*}
V_{L1} &= L_1 \frac{di_{L1}}{dt} = V_{in} \\
V_{C_{21}} &= V_{C_1}, \quad V_{C_{21}} + V_{C_{31}} = V_{C_1} + V_{C_2} \\
V_{C_1} &= V_{in} - L_2 \frac{di_{L2}}{dt} \\
V_{C_2} + V_{C_1} &= V_{in} - L_2 \frac{di_{L2}}{dt} + V_{C_{22}} \\
V_o &= V_{C_3} + V_{C_2} + V_{C_1} = V_{in} - L_2 \frac{di_{L2}}{dt} + V_{C_{22}} + V_{C_{32}}
\end{align*}
\]

\begin{equation}
(3)
\end{equation}

3) STATE-3: WHEN SWITCH S_1 AND SWITCH S_2 ARE OFF

The equivalent power circuit when switches S_1 and S_2 are OFF is depicted in Fig. 4(c). In this mode, inductors L_1 and L_2 are demagnetized to charge output side capacitors. Capacitors C_1, C_2 and C_3 are charged by series combination \( V_{in}, L_1, C_{21}, C_{31} \) and series combination of \( V_{in}, L_2, C_{22} \) and \( C_{32} \). Diodes \( D_{11}, D_{31}, D_{51}, D_{12}, D_{32}, D_{52} \) are forward biased, and diodes \( D_{21}, D_{41}, D_{22}, D_{42} \) are reversed biased. The voltage across

inductors and capacitors are calculated as follows,

\[
\begin{align*}
V_{C_1} &= V_{in} - L_1 \frac{di_{L1}}{dt} = V_{in} - L_2 \frac{di_{L2}}{dt} \\
V_{C_2} + V_{C_1} &= V_{in} - L_1 \frac{di_{L1}}{dt} + V_{C_{21}} = V_{in} - L_2 \frac{di_{L2}}{dt} + V_{C_{22}} \\
V_{C_3} + V_{C_2} + V_{C_1} &= V_{in} - L_1 \frac{di_{L1}}{dt} + V_{C_{21}} + V_{C_{31}} \\
V_o &= V_{C_3} + V_{C_2} + V_{C_1} = V_{in} - L_2 \frac{di_{L2}}{dt} + V_{C_{22}} + V_{C_{32}}
\end{align*}
\]

\begin{equation}
(4)
\end{equation}

4) STATE-4: WHEN SWITCH S_1 IS OFF, AND SWITCH S_2 IS ON

The equivalent circuit of the proposed converter when switch S_1 is OFF and switch S_2 is ON is depicted in Fig. 4(d). The inductor L_2 is magnetized from input voltage (\( V_{in} \)) and at the same time, the capacitors C_1, C_2 and C_3 charged by inductor L_1 and capacitors C_{21} and C_{31}. The inductor L_1 and capacitors C_{21} and C_{31} also charge capacitors C_{22}, C_{32} of the multiplier cell and provides energy to load (\( R_o \)). In this mode, diodes \( D_{11}, D_{31}, D_{51}, D_{22}, D_{42} \) are forward biased, and diodes \( D_{21}, D_{41}, D_{22}, D_{42} \) are reversed biased.
$D_{41}, D_{12}, D_{32}, D_{32}$ are reversed biased.

\[
\begin{align*}
V_{L2} &= L_2 \frac{di_{L2}}{dt} = V_{in} \\
V_{C22} &= V_{C1}, V_{C22} + V_{C32} = V_{C1} + V_{C2} \\
V_{C1} &= \frac{V_{in} - L_1 \frac{di_{L1}}{dt}}{} + V_{C21} \\
V_{C1} + V_{C1} &= \frac{V_{in} - L_1 \frac{di_{L1}}{dt} + V_{C21} + V_{C31}}{}
\end{align*}
\]

The CCM inductor current and voltage waveforms for all the states are shown in Fig. 5.

\[
\begin{align*}
\Delta i_{L1} &= i_{L1}(0) - i_{L1}(t) \\
\Delta i_{L2} &= i_{L2}(0) - i_{L2}(t)
\end{align*}
\]

\textbf{FIGURE 5. CCM inductor current and voltage waveform for all the states.}

C. THE POSSIBLE STATES IN DISCONTINUOUS CONDUCTION MODE

When Nx-IMBC circuit operates in DCM, there are three possible states which depend on the switching of the switches $S_1$ and $S_2$.

1) STATE-1: WHEN SWITCH $S_1$ IS ON, SWITCH $S_2$ IS OFF, AND $L_2$ CURRENT IS ZERO

The equivalent power circuit for this state is depicted in Fig. 6(a). The inductor $L_1$ is magnetized from input voltage ($V_{in}$) and the capacitors $C_{21}$ are charged by the capacitor $C_1$ through diode $D_{21}$ and switch $S_1$. Capacitor $C_{31}$ is charged by the capacitor $C_2$ through diode $D_{41}$ and switch $S_1$. At the same time, capacitors $C_1, C_2, C_3$ also discharged through the load ($R_o$). In this mode, diodes $D_{11}, D_{12}, D_{22}, D_{31}, D_{32}, D_{42}, D_{51},$ and $D_{52}$ are reversed biased and diodes $D_{21}, D_{41}$ are forward biased. The slope of inductor current and capacitors voltage is calculated as follows,

\[
\begin{align*}
\frac{di_{L1}}{dt} &= \frac{V_{in}}{L_1}, \frac{di_{L2}}{dt} = 0 \\
V_{C1} &= V_{C1} + V_{C21} + V_{C31} = V_{C1} + V_{C2} \\
V_{o} &= V_{C1} + V_{C2} + V_{C1}
\end{align*}
\]

2) STATE-2: WHEN SWITCH $S_1$ IS OFF, SWITCH $S_2$ IS ON, AND $L_1$ CURRENT IS ZERO

The equivalent power circuit for this state is depicted in Fig. 6(b). The inductor $L_2$ is magnetized from input voltage ($V_{in}$) and the capacitor $C_{22}$ is charged by the capacitor $C_1$ through diode $D_{22}$ and switch $S_2$. Capacitor $C_{32}$ is charged by the capacitor $C_2$ through diode $D_{12}$ and switch $S_2$. At the same time, capacitors $C_1, C_2, C_3$ discharged through the load ($R_o$).

In this mode, diodes $D_{11}, D_{12}, D_{21}, D_{31}, D_{32}, D_{41}, D_{51},$ and $D_{52}$ are reversed biased, and diodes $D_{22}, D_{32}$ are forward biased. The slope of inductor current and capacitors voltage is calculated as follows,

\[
\begin{align*}
\frac{di_{L2}}{dt} = \frac{V_{in}}{L_2}, \frac{di_{L1}}{dt} = 0 \\
V_{C22} &= V_{C1}, V_{C22} + V_{C32} = V_{C1} + V_{C2} \\
V_{o} &= V_{C1} + V_{C2} + V_{C1}
\end{align*}
\]

3) STATE-3: WHEN SWITCHES $S_1, S_2$ ARE OFF, $L_1$ AND $L_2$ CURRENT IS ZERO

The equivalent power circuit for this state depicted in Fig. 6(c). In this mode, all the diodes are reversed biased and capacitors $C_1, C_2, C_3$ discharged through the load ($R_o$). The slope of inductor current and the output voltage is calculated as follows,

\[
\begin{align*}
\frac{di_{L2}}{dt} = \frac{di_{L1}}{dt} = 0 \\
V_{o} &= V_{C1} + V_{C2} + V_{C1}
\end{align*}
\]

Inductor current and voltage waveforms for all the state of DCM are shown in Fig. 7.

D. BOUNDARY OF CCM AND DCM

In general, DCM is occurring when the inductor current reaches zero. The condition for CCM and DCM for Nx-IMBC is,

\[
\begin{align*}
\text{DCM} &\Rightarrow I_{L1} < \Delta i_{L1}(t); I_{L2} < \Delta i_{L2}(t) \\
\text{CCM} &\Rightarrow I_{L1} > \Delta i_{L1}(t); I_{L2} > \Delta i_{L2}(t)
\end{align*}
\]

For simple calculation, assume all the components and semiconductor devices are ideal. Consider $D$ is the duty ratio of gate pulses provided to switches $S_1$ and $S_2$ (Note: Both switches have an equal duty cycle $(D)$ and switching frequency). The pulse given to switch $S_2$ is delayed by 50% compared to switch $S_1$. Therefore, according to circuit topology, the voltage across all the capacitors is the same, and the voltage across the load is calculated as follows,

\[
V_{o} = V_{N_{x-IMBC}} = N \times V_{C1} = \frac{N \times V_{in}}{1 - D}
\]

It is noteworthy that, the current flowing through both the inductors is same ($I_{L1} = I_{L2} = I_L$). The condition for DCM is obtained as,

\[
\begin{align*}
I_L &= \frac{N^2 \times V_{in}}{2R_o(1-D)2} < \frac{V_{in}D}{L_1 \times f_s}; \frac{V_{in}D}{L_2 \times f_s} \\
\frac{fsL_1}{R_o} or \frac{fsL_2}{R_o} < \frac{2D \times (1-D)2}{N^2}; B < B_{\text{critical}}(D)
\end{align*}
\]

Boundary Surface $= B_{\text{critical}}(D) = \frac{2D \times (1-D)2}{N^2}$

The boundary for DCM and CCM is shown in Fig. 8. Investigated that $B_{\text{critical}}(D)$ decreases as the number of levels increased, and $8/27N^2$ is the maximum value of $B_{\text{critical}}(D)$ for N level at $D = 1/3$. 
III. STEADY-STATE ANALYSIS AND EFFECT OF INTERNAL RESISTANCE OF INDUCTOR AND SEMICONDUCTOR DEVICES FOR Nx-IMBC

A. ANALYSIS IN CCM

In real-time applications, the voltage conversion ratio of any DC-DC converter is restricted by parasitic resistance of passive components or devices; specially inductor of the converter. Parasitic $R_{L1}$ and $R_{L2}$ (Equivalent Series Resistance) is considered in series with inductor $L_1$ and $L_2$ respectively. The voltage across inductors $L_1$ and $L_2$ is calculated when switches $S_1$ and $S_2$ are ON and OFF as follow,

$$S_{1\,ON} \Rightarrow V_{in} - I_{L1}R_{L1} = L_1 \frac{di_{L1}}{dt}$$
$$S_{2\,ON} \Rightarrow V_{in} - I_{L2}R_{L2} = L_2 \frac{di_{L2}}{dt}$$
$$S_{1\,OFF} \Rightarrow V_{in} - I_{L1}R_{L1} - V_{C1} = L_1 \frac{di_{L1}}{dt}$$
$$S_{2\,OFF} \Rightarrow V_{in} - I_{L2}R_{L2} - V_{C1} = L_2 \frac{di_{L2}}{dt}$$

(12)

Note: for simplicity, consider ideal diode ($V_d = 0$) and ideal switch ($V_S = 0$) in Nx-IMBC with load $R_o$.

$$V_{in} \times I_{in} = I_o \times V_o = \frac{N^2 V_{in} V_{C1}}{(1 - D)R_o}$$

(13)

Inductor volt balanced second method is applied and equations obtained as follow,

$$V_{L1} = D(V_{in} - I_{L1}R_{L1}) + \overline{D}(V_{in} - I_{L1}R_{L1} - V_{C1}) = 0$$
$$V_{L2} = D(V_{in} - I_{L2}R_{L2}) + \overline{D}(V_{in} - I_{L2}R_{L2} - V_{C1}) = 0$$

(14)

$$V_{in} = \frac{I_{L1}R_{L1} + I_{L2}R_{L2}}{2} + (1 - D) V_{C1}$$

(15)
FIGURE 9. Voltage Conversion ratio plot versus the duty cycle for different cases of $\frac{R_L}{R_o}$ (a) $N = 1$, (b) $N = 2$, (c) $N = 3$, (d) voltage conversion ratio plot versus duty cycle for $N = 1$ to 5 when $R_L = 0$.

Noted that identical rating inductor are used. So, their internal resistance is the same ($R_{L1} = R_{L2} = R_L$). Thus,

$$V_{in} = \frac{(I_{L1} + I_{L2})R_L}{2} + (1 - D)V_{C1}$$

$$V_{in} = \frac{I_{LR}}{2} + (1 - D)V_{C1}$$

(16)

By the above equation, the voltage conversion ratio obtained as,

$$\frac{V_o}{V_{in}} = \frac{1}{\frac{N \times R_L}{2 (1 - D) R_o} + \frac{D}{N}} = \frac{N}{(1 - D) + \frac{N^2 \times R_L}{2 (1 - D) R_o}}$$

(17)

In Fig. 9(a) - 9(c), the voltage conversion ratio is a plot against duty cycle for various cases of $\frac{R_L}{R_o}$ when $N = 1$ to 3. In Fig. 9(d), the voltage conversion ratio is a plot against duty cycle for $N = 1$ to 5 and $R_L = 0$ (ideal case). Examined that the voltage conversion ratio is linear increases up to duty cycle 80%, and this linear region called a Quasi Linear Region.

To calculate the efficiency of the converter, let us consider voltage $V_C$ and $V_S$ is the drop of each diode and each switch, respectively.

It is examined that capacitor $C_1$ transfers its energy to charge capacitor $C_{21}$ through diode $D_{21}$ and switch $S_1$ in state I and II. Also, capacitor $C_1$ transfers its energy to charge capacitor $C_{22}$ through diode $D_{22}$ and switch $S_2$ in state I and IV. The voltage across capacitor $C_{21}$ and $C_{22}$ are obtained as follows,

$$V_{C21} = V_{C1} - V_d - V_S$$

$$V_{C22} = V_{C1} - V_d - V_S$$

(18)

The capacitor $C_{21}$ and $C_{22}$ transfer its energy to charged capacitor $C_2$. The voltage across $C_2$ is obtained as follows,

$$V_{C2} = V_{C21} - 2V_d = V_{C1} - 3V_d - V_S$$

(19)

The capacitor $C_2$ transfers its energy to charge capacitor $C_{31}$ through diode $D_{31}$ and switch $S_1$ in state I and II. Also, capacitor $C_2$ transfers its energy to charge capacitor $C_{32}$ through diode $D_{32}$ and switch $S_2$ in state I and IV. The voltage across capacitor $C_{31}$ and $C_{32}$ is obtained as follows,

$$V_{C31} + V_{C21} = 2V_{C1} - 5V_d - V_S$$

$$V_{C32} + V_{C22} = 2V_{C1} - 5V_d - V_S$$

$$\therefore V_{C31} = V_{C32} = V_{C1} - 4V_d$$

(20)

Further, observed that the voltage across capacitors $C_{31}$, $C_{32}$, $C_{41}$, $C_{42} ...$, $C_{N1}$, and $C_{N2}$ is same and equal to $V_{C1} - 4V_d$. The total output voltage is calculated as follows (21), shown at the bottom of the next page.
The efficiency ($\eta$) of the Nx-IMBC obtained as follows,

$$\eta = \frac{1}{1 + \frac{NL}{2(1-D)R_o} + N}$$

if semiconductor devices are ideal, then

$$\eta = \frac{1}{1 - \frac{NL}{2(1-D)R_o} + N}$$

The power loss due to semiconductor devices ($P_{LS}$) and internal resistance of inductor ($P_{Li}$) of the Nx-IMBC obtained as follows,

$$P_{LS} = P_{in} \left( 1 - \left( 1 - \frac{(1-D)N}{2(1-D)R_o} + (1-D)/N \right) \right)$$

$$P_{Li} = P_{in} \left( 1 - \frac{(1-D)/N}{2(1-D)R_o} + (1-D)/N \right)$$

(B. ANALYSIS OF DCM)

Let’s consider, switch $S_1$ is ON and inductor $L_1$ is magnetized for the time $D_1T_S$; switch $S_1$ is OFF and inductor $L_1$ is demagnetized for the time $D_2T_S$; and switch $S_1$ is OFF and inductor $L_1$ current is zero for the time $D_3T_S$. Similarly, at 180° phase shift, switch $S_2$ is ON and inductor $L_2$ is magnetized for the time $D_1T_S$; switch $S_2$ is OFF and inductor $L_2$ is demagnetized for the time $D_2T_S$; and switch $S_2$ is OFF and inductor $L_2$ current is zero for the time $D_3T_S$. The time relations obtained as follows,

$$One cycle Time = T_S = \frac{1}{f_s} = DT_S + D_1T_S + D_2T_S \Rightarrow (D + D_1 + D_2) = 1$$

The voltage across inductor $L_1$ and $L_2$ for each time-period obtained as follows,

$$V_{in} - I_{L1}R_{L1} = V_{L1} \quad for \quad D_1T_S$$

$$V_{in} - I_{L2}R_{L2} = V_{L2} \quad for \quad D_2T_S$$

If both inductors are identical and ideal then, $L_1 = L_2 = L$ and $R_{L1} = R_{L2} = 0$;

$$V_o^2 - \frac{NV_o^2}{2B} = \frac{V_o}{V_{in}} = 0$$

The solution of (31) yields two roots. However, we know that the output of the proposed converter is positive. Therefore positive root is selected, and the voltage conversion ratio obtained as follows,

$$V_o/V_{in} = 0.5 \left( 1 + \frac{1 + 2ND_1^2}{B} \right)$$

Examined that the voltage conversion ratio is load-dependent and consequent increasing converter output impedance.

$$V_o = \frac{1}{\frac{1}{N \times R_L} \left( 1 - (4N - 3)D \right) + N} \times \frac{V_{in} - (4N - 3)V_d - V_S}{2(1-D)R_o}$$

where,

$$\left\{ \begin{array}{l}
1 \frac{N \times R_L}{2(1-D)R_o} \rightarrow Effect \ of \ Internal \ Resistance \ of \ Inductor \\
(4N - 3)D \rightarrow Effect \ of \ diode \\
V_S \rightarrow Effect \ of \ switch 
\end{array} \right.$$
The converter is possible to control in three different range of duty cycle i) duty cycle higher than 50% ii) duty cycle lesser than 50% and iii) duty cycle is equal to 50%. The slope of the inductor currents is used to calculate critical inductance such that considered current ripples obtained. The critical inductance and current stress calculated for three different ranges of duty cycle, as shown in Fig. 10(a)-(c). First, analyzed that the proposed converter operates in states 1, 2 and 4 when the duty cycle is higher than 50%. Second, analyzed that the proposed converter operates in states 2, 3 and 4 when the duty cycle is lesser than 50%. Third, analyzed that the proposed converter operates only in state 2 and 4 when the duty cycle equal to 50%.

V. DESIGN AND COMPARISON OF Nx-IMBC

The voltage across all the capacitors is precisely the same if all the diodes are considered ideal. Therefore, due to the balanced voltage structure of voltage multiplier, it is feasible to select all the capacitors with an equal rating. The critical capacitance and current calculated and examined that each switch voltage is equal to each capacitor voltage. The current flowing through switch is equal to the addition of inductor current and capacitor clamping current. Voltage and current rating of the switch are decided as,

\[ V_D > \frac{V_o}{N} = \frac{V_{in}}{1-D}, \quad I_D > I_L > \frac{I_{in}}{2} \]  

(35)

The drain to source voltage of both switches \( S_1 \) and \( S_2 \) calculated and examined that each switch voltage is equal to each capacitor voltage. The current flowing through switch is equal to the addition of inductor current and capacitor clamping current. Voltage and current rating of the switch are decided as,

\[ \begin{align*} 
(V_{S1} = V_{S2}) > \frac{V_o}{N} = \frac{V_{in}}{1-D}, \\
(i_{S1}(t) = i_{S2}(t)) > i_{in}(t) + C_{apacitor \ clamping \ current} \\
(i_{S1}(t) = i_{S2}(t)) > i_{in}(t), 
\end{align*} \]

(36)

In Table-2, Nx-IMBC configuration compared with existing DC-DC converter in terms of voltage conversion ratio, voltage stress, number of the inductor, number of the capacitor, number of diodes, number of switches, input current behavior. It is noteworthy that the Nx-IMBC provides high voltage conversion ratio with the low voltage across switch, input current ripple cancellation, and without using a more significant number of inductors and switches. In Fig. 11, the Nx-IMBC and existing converters are compared in terms of voltage conversion ratio. Notably, Nx-IMBC provides a practical solution to obtain high voltage with reduce input ripple, and low rating components are suitable to design converter.

VI. NUMERICAL SIMULATION AND EXPERIMENTAL RESULTS

Nx-IMBC configuration is simulated with ideal components for three-level (i.e 3x IMBC) with the designed parameter to verify its functionality. The designed parameters given in Table 3. Fig. 12(a) shows the output and input voltage of three levels 3x IMBC, and investigated that the voltage conversion ratio converter is 12 at 75% duty cycle. Thus, the required output voltage 120V obtained from a 10V input voltage at a 75% duty cycle. Fig. 12(b) shows the voltage

\[ V_{o} = \frac{V_{in} \times 3}{1-D} \]

The converter is possible to control in three different range of duty cycle i) duty cycle higher than 50% ii) duty cycle lesser than 50% and iii) duty cycle is equal to 50%. The slope of the inductor currents is used to calculate critical inductance such that considered current ripples obtained. The critical inductance and current stress calculated for three different ranges of duty cycle, as shown in Fig. 10(a)-(c). First, analyzed that the proposed converter operates in states 1, 2 and 4 when the duty cycle is higher than 50%. Second, analyzed that the proposed converter operates in states 2, 3 and 4 when the duty cycle is lesser than 50%. Third, analyzed that the proposed converter operates only in state 2 and 4 when the duty cycle equal to 50%.
TABLE 2. Comparison of Nx IMBC and existing DC-DC converter.

| Converter  | Inductors | Capacitors | Diodes | Switches | Output voltage at D=0.6 | Ripples Cancellation | Output capacitor stack | Voltage across switch |
|------------|-----------|------------|--------|----------|--------------------------|----------------------|------------------------|----------------------|
| Fig. 1(a)  | 1         | 1          | 1      | 1        | 2.50Vt             | NO                   | NO                     | V_o                  |
| Fig. 1(c)  | 2         | 1          | 4      | 1        | 4Vt                 | NO                   | NO                     | V_o                  |
| Fig. 1(b)  | 2         | 2          | 3      | 1        | 6.25Vt             | NO                   | NO                     | V_o                  |
| Flg. 1(d)  | 1         | 2          | 2      | 2        | 5Vt                 | NO                   | NO                     | V_o/2                |
| Fig. 1(e)  | 2         | 2          | 2      | 2        | 6.25Vt             | NO                   | NO                     | 0.4V_o               |
| Fig. 1(f)  | 2         | 3          | 4      | 3        | 9Vt                 | NO                   | NO                     | V_o                  |
| Flg. 1(g)  | 2         | 3          | 2      | 1        | 4Vt                 | NO                   | NO                     | V_o/0.4              |
| Flg. 1(h)  | 2         | 4          | 4      | 2        | 10Vt               | YES                  | NO                     | V_o/4                |
| Flg. 1(i)  | 5         | 6          | 9      | 1        | 10Vt               | NO                   | NO                     | V_o/4                |
| Flg. 1(j)  | 2         | 3          | 4      | 2        | 5Vt                 | YES                  | NO                     | V_o/2                |
| Nx MBC     | 1         | 2N-1       | 2N-1   | 1        | NV_o/0.4            | NO                   | YES                    | V_o/0.4              |
| Nx MBC     | 1         | 2N-1       | 2N-1   | 1        | ((N-1)+0.6)V_o/(0.4) | NO                   | YES                    | V_o/0.4              |
| Nx IMBC    | 2         | 3N-2       | 2(2N-3)| 2        | NV_o/0.4            | YES                  | YES                    | V_o/4                |

TABLE 3. Parameter of numerical simulation test.

| Parameter | Value |
|-----------|-------|
| Input Voltage, Output Voltage | 10V, 120V |
| Power, Load | 100W, 144Ω |
| Number of Output Levels | Three |
| Inductance, Capacitance | 150uH, 220uF |
| Duty Cycle, Switching Frequency | 75%, 50kHz |

FIGURE 11. Voltage conversion ratio versus duty cycle (A: Fig. 1(h), 1(i), Nx MBC, Nx IMBC; B: Fig. 1(f); C: Fig. 1(b), 1(e); D: Fig. 1(d), 1(j); E: Fig. 1(c), 1(g); F = Fig. 1(a)).

at a different output level. Observed that each level contributes to equal voltage (V_o/3, i.e. 40V). Thus, the voltage at the first level is 40V, the voltage at the second level is 80V, and the voltage at the third level is 120V. Fig. 12(c) shows the voltage distribution across output side capacitors (C_1, C_2 and C_3). Investigated that voltage across output side capacitors is equal to V_o/3 (i.e. 40V). The voltage distribution across all the output side capacitors (C_1, C_2 and C_3) shows that the converter performs satisfactorily. Fig. 12(d) shows the voltage distribution across multiplier capacitors. Investigated that voltage across capacitors of the multiplier is equal to V_o/3 (i.e. 40V). The voltage distribution across all the capacitors C_21, C_22, C_31 and C_32 shows that the converter performs satisfactorily.

Fig. 13(a) shows the inductor current waveform with the gate pulse of switches. Investigated that 5.2A current is flowing through the inductor (L1 and L2) which is nearly half of the input current (I_in/2). Fig. 13(b) shows the drain to source voltage of switches (V_DS1 and V_DS2) with gate to source voltage of switches (V_GS1 and V_GS2). Observed that the drain to source voltage of switches is equal to V_o/3 i.e 40V. This drain to source voltage of switch remains same even also of the voltage levels at the output. Output and input current ripples shown in Fig. 13(c). Observed that the input current and output current ripple is 600mA and 2mA, respectively. Thus, 3Nx IMBC provides a low input and output current ripple, and highly desired in photovoltaic application.

The 3x IMBC investigated experimentally, and the result shows a good match with the simulation results. The detail of the hardware components used for the experimental purpose shown in Table 4. The hardware prototype of Nx IMBC is designed for three-level (3x IMBC) and tested at power 100W, and gate pulses are generated through FPGA with a classical PI controller to control the output voltage.

Fig. 14(a) shows the obtained output voltage, input voltage, output current and input current waveform. Examined that output voltage (V_o) 120.17V achieved by feeding input voltage (V_in) 10V. The observed input current (I_in) and output current (I_o) are 10.63A and 808.5mA, respectively. Fig. 14(b) shows the obtained voltage waveform at various levels of the designed converter. Examined that the voltage at level one, two, and three are 40.13V, 80.19V, and 120.21V, respectively. Separately, the voltage across each output side capacitor also measured and shown in Fig. 14(c). The obtained voltage
FIGURE 12. Simulation results of 3x IMBC (a) output voltage and input voltage, (b) output voltage at different levels, (c) voltage distribution across capacitors $C_1$, $C_2$ and $C_3$, (d) voltage distribution across capacitors $C_{21}$, $C_{31}$, $C_{22}$ and $C_{32}$.

TABLE 4. Hardware implementation detail.

| Components                  | Value or type | No. of components |
|-----------------------------|---------------|-------------------|
| Input voltage/output voltage| 12V/120V      | -                 |
| Switch ($S_1$ and $S_2$)    | IRF540 (0.077 ON state resistance) (2 pcs) | 02 |
| Power Diodes                | BYQ28E (10 pcs) | 02 |
| Power Inductor              | 150uH (10A current rating) | 02 |
| Capacitors                  | 220uF, 100V (7 pcs) | 07 |
| Load                        | 144 Ω, 100W   | 01 |
| Switching Frequency         | 50kHz         | -                 |

FIGURE 13. Simulation results of 3x IMBC (a) Inductor current waveforms ($I_{L1}$ and $I_{L2}$) with gate pulse of switches ($V_{GS1}$ and $V_{GS2}$) (b) Voltage stress across switches ($V_{DS1}$ and $V_{DS2}$), (c) Input and output current ripples.

across capacitor $C_1$, $C_2$, and $C_3$ are 40.13V, 40.09V, and 40.05V, respectively. The voltage across multiplier capacitors $C_{21}$, $C_{31}$, and $C_{22}$, $C_{32}$ is shown in Fig. 14(d) and Fig. 14(e), respectively. The obtained voltage across capacitor $C_{21}$, $C_{31}$, $C_{22}$, and $C_{32}$ is 40.07V, 40.05V, 40.09V, and 40.08V, respectively. Based on the obtained results, it is clear that voltage
distributions in all the capacitors are equal, and the magnitude is equal to the voltage at the first level of the converter. Fig. 14(f) shows the waveform of inductor current ($i_{L1}$, $i_{L2}$) and input current ($i_{in}$). Noted that both the inductor current are same, but shifted by 180°. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current ($i_{in}$). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero.

The performance of the designed converter also tested under the perturbation from the input side, load side and output voltage reference. Note: State-space modelling skipped from the article; however, the results discussed. Fig. 15(a) shows the waveform of input voltage ($v_{in}$), inductor $L_1$ current ($i_{L1}$), output voltage ($v_o$) and output current ($i_o$) when power is abruptly changed from 100W to 120W and 120W to 100W. Fig. 15(b) shows the waveform of the drain to source voltage across switch $S_1$ ($v_{DS1}$), inductor $L_1$ current ($i_{L1}$), output voltage ($v_o$) and output current ($i_o$) when power is abruptly changed from 100W to 120W and 120W to 100W.
For convenient, the obtained waveforms sectioned in three sections A, B and C. Section A and C are the obtained waveform when the converter operated at 100W, and section B are the obtained waveform when the converter operated at 120W. Highlighted part AB shows the transients when the power of the converter abruptly changed from 100W to 120W. Highlighted part BC shows the transients of the converter when the power of the converter abruptly changed from 120W to 100W. Notably, the output voltage is maintained; even power abruptly changed with constant input voltage ($v_{in}$). Due to the constant input voltage ($v_{in}$) and output voltage ($v_{o}$), inductor current ($i_{L1}$) and output current ($i_{o}$) are changed to fulfill the demand for power. There is no change in the drain to source switch voltage ($v_{DS1}$) even power changed 100W to 120W and 120W to 100W because of constant output voltage ($v_{o}$).

Fig. 15(c) shows the waveform of input voltage ($v_{in}$), inductor $L_1$ current ($i_{L1}$), output voltage ($v_{o}$) and output current ($i_{o}$) when output reference voltage ($v_{oref}$) is abruptly changed from 100V to 110V and 110V to 120V at constant load. For convenient, the obtained waveforms sectioned in three sections A, B and C. Section A, B, and C shows the obtained waveform when converter output reference ($v_{oref}$) is set to 100V, 110V, and 120V respectively. Highlighted part AB and BC shows the transients when the power of the converter output reference ($v_{oref}$) is changed from 100V to 110V and 110V to 120V, respectively. Noticed that expected output voltage achieved even there is no change in input voltage ($v_{in}$). It is interesting to know that to maintain the equal power at the input and output side, inductor current ($i_{L1}$) and outputs current a changed according to output voltage reference ($v_{oref}$).

Fig. 15(d) shows the waveform of input voltage ($v_{in}$), inductor $L_1$ current ($i_{L1}$), output voltage ($v_{o}$) and output current ($i_{o}$) when the input voltage ($v_{in}$) abruptly changed from 8V to 10V and 10V to 12V. Section A, B, and C shows the obtained waveform when the converter input voltage ($v_{in}$) set at 8V, 10V, and 12V, respectively. Highlighted part AB and BC shows the transients when input voltage ($v_{in}$) converter abruptly changed from 8V to 10V and 10V to 12V, respectively. Notably, constant output voltage ($v_{oref}$) 120V achieved even changed in input voltage ($v_{in}$). For maintain the equal power at the input and output side, the inductor current is increased or decreased according to input side voltage ($v_{1}$).
Fig. 15(e) shows the waveform of the drain to source switch $S_1$ voltage ($v_{DS1}$), inductor $L_1$ current ($i_{L1}$), output voltage ($v_o$) and output current ($i_o$), when the input voltage ($v_{in}$) abruptly changed from 8V to 10V, 10V to 12V, and 12 V to 14V. Section A, B, C and D show the obtained waveform when the converter input voltage ($v_{in}$) set at 8V, 10V, 12V and 14V, respectively. Highlighted part AB, BC and CD shows the transients when input voltage ($v_{in}$) converter abruptly changed from 8V to 10V, 10V to 12V, and 12V to 14V respectively. Drain to source voltage of switch $S_1$ ($v_{DS1}$) and output voltage ($v_o$) is constant even input voltage changed. For maintain equal power at the input and output side, the inductor current is increased or decreased according to the input voltage ($v_1$). Various tests conducted, and observed efficiency at 100W shown in Fig. 16(a). It observed that on an average 91.37% efficiency of the 3x IMBC. It noted that the 3x IMBC is slightly improved when compared to the multilevel boost converter ($\sim 89\%$) at 100W proposed in [38], Interleaved Converter ($\sim 94\%$) at 150W proposed in [43], and Interleaved converter ($\sim 93.5\%$) proposed in 150W [44].

The converter is operated at various power levels from 60W to 120W. The observed efficiency at various power levels shown in Fig. 16(b). During power variation, the efficiency of the 3x MBC is in range of 87 to 92%. Majorly, the PV to the grid system, MLI circuitry needs several voltage sources along with several DC-DC converters at the input side. The Nx-IMBC configuration is suitable to feed MLI due to capacitor stack structure at the output side, as shown in Fig. 17. The Nx IMBC provides a solution to feed MLI with single DC-DC converter. Additionally, the Nx-IMBC configuration finds the applications like automotive, renewable appliances, electric vehicles and microgrid were low to high conversion ratio is necessary. Further, it is also possible to increase the phases of the interleaved converter based on the applications.
VII. CONCLUSION

The detail investigation and boundary of CCM and DCM with steady-state analysis of hybrid Nx-IMBC are presented. Nx-IMBC converter topology extended the feature of 2x interleaved boost converter and combines the features of the interleaved converter and recently proposed Multilevel Boost Converter (MBC). Nx-IMBC provides higher voltage conversion ratio compared to recently addressed converters with reduced input ripples. The main advantages of Nx IMBC are that in case if one phase of the converter is failing, then also Nx-IMBC provides the same voltage conversion ratio. Additionally, it is also possible to feed Nx-IMBC with two different sources.

Additional merits of the novel converter include:
1. The non-inverting output voltage, and performed as similar as a recently proposed multilevel boost converter.
2. Non-isolated configuration, and avoided bulky transformers.
3. Low input/output current and output voltage ripple.
4. Voltage stress across the switch is low.
5. The number of output side levels raised by adding a diode-capacitor circuit, thereby the voltage conversion ratio increased.

Moreover, the Nx-IMBC converter compared with a new non-isolated DC-DC converter and multilevel converters in terms of switch voltages and number of components. Based on the experimental and simulation result, it is possible to conclude that Nx-IMBC is a promising topology for feeding MLI, photovoltaic applications, automotive appliances, PV drives, and electric vehicles. The experimental shows a good match with simulation results and verifies the validity of the design, feasibility, working of the converter.

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He worked as a Research Student with the Power Quality Research Group, Department of Electrical Power Engineering, Universiti Tenaga Nasional (UNITEN), Kuala Lumpur, Malaysia, from August to September 2017. He is currently with the Renewable Energy Lab, Department of Communications and Networks Engineering, College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia. He has authored 100 plus scientific articles with a particular reference to dc/dc and dc/ac converter, and high-gain converters, received the Best Paper Research Paper Award from the IEEE ICCPCT 2014, IET CEAT 2016, ETAEERE 2016, and the IEEE CENCON 2019, and sponsored Lecture Notes in Electrical Engineering, a springer book series. He is a member of the IEEE Industrial Electronics Society, the IEEE Power Electronics Society, the IEEE Industrial Application Society, the IEEE Power and Energy Society, the IEEE Robotics and Automation Society, and the IEEE Vehicular Technology Society, the IEEE Young Professionals, various IEEE councils, and technical communities. He received the Reviewer of Month Award of IEEE Access, in January 2019, for his valuable and thorough feedback on manuscripts, and quick turnaround on reviews. He is a Reviewer Member of various international journals and conferences, including the IEEE and IET.

DHAFER J. ALMAKHLES (Member, IEEE) received the B.E. degree in electrical engineering from the King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, in 2006, and the master’s degree (Hons.) and Ph.D. degree from The University of Auckland, New Zealand, in 2011 and 2016, respectively. Since 2016, he has been with Prince Sultan University, Saudi Arabia, where he is currently the Chairman of the Department of Communications and Networks Engineering and the Director of the Science and Technology Unit and the Intellectual Property Office. He is the Leader of the Renewable Energy Research Team and Laboratory. His research interests include power electronics, control theory, unmanned aerial vehicles, renewable energy systems, and FPGA applications. He is a member of the IEEE Power Electronics Society and the IEEE Control Society. He is a Reviewer Member of various international journals and conferences, including the IEEE and IET.

SANJEEVIKUMAR PADMANABAN (Senior Member, IEEE) received the bachelor’s degree in electrical engineering from the University of Madras, Chennai, India, in 2002, the master’s degree (Hons.) in electrical engineering from Pondicherry University, Puducherry, India, in 2006, and the Ph.D. degree in electrical engineering from the University of Bologna, Bologna, Italy, in 2012.

He was an Associate Professor with the Vellore Institute of Technology (VIT), from 2012 to 2013. In 2013, he joined the National Institute of Technology, India, as a Faculty Member. In 2014, he was invited as a Visiting Researcher at the Department of Electrical Engineering, Qatar University, Doha, Qatar, funded by the Qatar National Research Foundation (Government of Qatar). He continued his research activities with the Dublin Institute of Technology, Dublin, Ireland, in 2014. He was an Associate Professor with the Department of Electrical and Electronics Engineering, University of Johannesburg, Johannesburg, South Africa, from 2016 to 2018. Since 2018, he has been a Faculty Member of the Department of Energy Technology, Aalborg University, Esbjerg, Denmark. He has authored more than 300 scientific articles. He was a recipient of the Best Paper cum Most Excellence Research Paper Award from IET SEISCON 2013, IET CEAT 2016, the IEEE EECI 2016, and the IEEE CENCON 2019, and five best paper awards from ETAEERE 2016, and sponsored Lecture Notes in Electrical Engineering, a Springer book. He is a Fellow of the Institution of Engineers, India, the Institution of Electronics and Telecommunication Engineers, India, and the Institution of Engineering and Technology, U.K. He is an Editor/Associate Editor/Editorial Board Member of refereed journals, in particular the IEEE SYSTEMS JOURNAL, the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, IEEE ACCESS, IET POWER ELECTRONICS, and the International Transactions on Electrical Energy Systems (Wiley), and the Subject Editor of the IET Renewable Power Generation, IET Generation, Transmission, and Distribution, and FACTS journal (Canada).

FREDE BLAABJERG (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Aalborg University, in 1995, and the Honoris Causa degree from University Politehnica Timisoara (UPT), Romania, in 2017, and Tallinn Technical University (TTU), Estonia. He was with ABB Scandia, Randers, Denmark, from 1987 to 1998. He became an assistant professor in 1992, an associate professor, in 1996, and a full professor of power electronics and drives, in 1998. In 2017, he became a Villum Investigator. He has published more than 600 journal articles in the fields of power electronics and its applications. He is the coauthor of four monographs and an editor of ten books in power electronics and its applications. His current research interests include power electronics and its applications such as wind turbines, PV systems, reliability, harmonics, and adjustable speed drives.

Dr. Blaabjerg was a Distinguished Lecturer of the IEEE Power Electronics Society, from 2005 to 2007, and the IEEE Industry Applications Society, from 2010 to 2011 and from 2017 to 2018. He currently serves as the President of the IEEE Power Electronics Society. He is the Vice-President of the Danish Academy of Technical Sciences. He has received 32 IEEE prize paper awards, the IEEE PELS Distinguished Service Award, in 2009, the EPE PEMC Council Award, in 2010, the IEEE William E. Newell Power Electronics Award, in 2014, the Villum Kann Rasmussen Research Award, in 2014, the Global Energy Prize, in 2019, and the IEEE Edison Medal. He was nominated by Thomson Reuters to be between the most 250 cited researchers in engineering in the world, from 2014 to 2019. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS, from 2006 to 2012.
UMASHANKAR SUBRAMANIAM (Senior Member, IEEE) is with the Renewable energy Lab, College of Engineering, Prince Sultan University, Saudi Arabia, and has 15+ years of teaching, research, and industrial research and development experience. Previously, he worked as an Associate Professor, the Head, and a Senior Research and Development and Senior Application Engineer in the fields of power electronics, renewable energy, and electrical drives, with the Vellore Institute of Technology (VIT), Vellore. Under his guidance, 24 master’s degree students and more than 25 bachelor’s degree students completed the senior design project work. Also, six Ph.D. degree scholars completed their doctoral thesis as research associates. He is also involved in collaborative research projects with various international and national level organizations and research institutions. He has published more than 250+ research articles in national and international journals and conferences. He has also authored/coauthored/contributed 12 books/chapters and 12 technical articles on power electronics applications in renewable energy and allied areas. He is a member of the IACSIT, IDES, and ISTE. He has taken charge as the Vice-Chair of the IEEE Madras Section and the Chair of the IEEE Student Activities, from 2018 to 2019. He was an Executive Member, from 2014 to 2016, and the Vice-Chair of the IEEE MAS Young Professional, IEEE Madras Section, from 2017 to 2019. He received the Danfoss Innovator Award-Mentor, from 2014 to 2015 and from 2017 to 2018, and the Research Award from VIT, from 2013 to 2018. Also, he received the INAE Summer Research Fellowship, in 2014. He is an Editor of Hellyon journal (Elsevier).

DAN M. IONEL (Fellow, IEEE) received the M.Eng. and Ph.D. degrees in electrical engineering from the Polytechnic University of Bucharest, Bucharest, Romania. His doctoral program included a Leverhulme Visiting Fellowship with the University of Bath, Bath, U.K. He was a Postdoctoral Researcher with the SPEED Laboratory, University of Glasgow, Glasgow, U.K. He is currently a Professor of electrical engineering and the L. Stanley Pigman Chair in power with the University of Kentucky, Lexington, KY, USA, where he is also the Director of the Power and Energy Institute of Kentucky and the SPARK Laboratory. He previously worked in the industry, most recently as a Chief Engineer of Regal Beloit Corp., Grafton, WI, USA, and before that as the Chief Scientist of Vestas Wind Turbines. Concurrently, he was also a Visiting and Research Professor with the University of Wisconsin and Marquette University, Milwaukee, WI, USA. He has authored or coauthored two books and more than 200 technical articles, including five that received IEEE awards. He held more than 30 patents. He has contributed to technology developments with long-lasting industrial impact. He was the Inaugural Chair of the IEEE Industry Applications Society’s Renewable and Sustainable Energy Conversion Systems Committee and an Editor of the IEEE TRANSACTIONS ON SUSTAINABLE ENERGY. He is the Editor-in-Chief of the Electric Power Components and Systems journal and the Past Chair of the IEEE Power and Energy Society’s Electric Motor Subcommittee and the IEEE WG 1812, and was the General Chair of the IEEE 2017 Anniversary Edition of the International Conference on Electrical Machines and Drives.