Non-isolated Modified Quadratic Boost Converter with Midpoint Output for Solar Photovoltaic Applications

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Abstract. This paper presents a boost DC-DC converter topology with non-isolated high gain and output midpoint, to boost the voltage obtained from solar photovoltaic panels. The three-level boost converter is coupled to the output port of the single-switch quadratic boost converter to derive the proposed converter topology. The voltage gain of the proposed converter is greater than that of the classical boost converter. The voltage stress on the switches of the proposed converter is equal to half of the converter output voltage. Static analysis, operating modes, experimental waveforms in continuous current conduction and discontinuous current conduction modes are shown. A 520 W prototype converter was implemented in the laboratory and its results are presented.

1 Introduction

In photovoltaic systems with multiple modules connected in series, partial shadowing can lead to a reduction of voltage and power available from the panels together. In addition, the tracking of maximum power point is complex because the system has multiple peaks, resulting from the local maximum power points. In [1, 2] a comparative investigation of various photovoltaic arrangements with partial shading is presented. Still, the power of a photovoltaic panel is between 100 W and 350 W, and the voltage at maximum power point is 12 V to 42 V. The above values are not sufficient when compared to the voltage required in the dc bus of inverters, which reduces the efficiency of the whole system [3, 4].

To extend the conversion range, the cascaded boost converters was used [5, 6]. However, the resulting structure is large and control is complex. With simplified structure, the quadratic boost converter with a single switch was proposed and analysed in [7-9], and in [9, 10] the drive cell has been associated to aid self-resonant switching, allowing the zero-voltage switching in the converter switch. The voltage gain can be increased by using magnetic coupling, coupled inductors based high gain converters are introduced in [11, 12]. With this technique, the ripples in the inductor current and the reverse recovery problems in the diodes are reduced. However, the voltage stress of the output diode is still high, the leakage inductance and parasitic capacitor of the diode will form a resonant circuit. Additionally, the ripples in the input current is highly discontinuous. By switched - capacitor technique, the topologies proposed in [13, 14] provide increased gain, but this can be achieved by using large number of capacitors.

The conduction and switching losses of quadratic converters are significant, making these converters more suitable for low power applications. Using three-state cells, high-gain converters with reduced input current ripple was proposed in [15, 16]. The solution presents a high gain, where the gain is increased by increasing the turns-ratio of the coupled inductor. A converter topology utilizing three-state cell and voltage multiplier cell was proposed in [17]. This solution may be limited to high power applications as a function of the current flowing through the capacitors. The voltage stresses in the semiconductor devices can be reduced as in [18], where the maximum voltage applied to the switches are equal to the fraction of its converter output voltage. The topology proposed in [19] presents asymmetry in the voltages across the switches when the gain is greater than 4, being characterized as a disadvantage despite the converter can operate with gains higher than four. Other quadratic converter topologies were presented in [20, 21], for driving the Light Emitting Diode, but the step-down voltage version. Besides these applications, a quadratic converter was used as a battery charger in [22]. In this case the system was developed to contemplate a high power-factor. With high voltage gain and low input current ripple, a converter topology based on interleaving technique was proposed in [23]. This article proposes a new topology for high gain DC-DC converter based on quadratic feature, which use low voltage switch and access to the midpoint of the output voltage.

The proposed converter topology is devised by connecting the three-level boost cell [24] shown in Fig. 1 (a) to the output port of the quadratic boost converters [5-7] which is shown in Fig. 1 (b). The resultant proposed converter is shown in Fig. 2.

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2 Principle of operation

To understand the proposed converter operation, the analysis is made for Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) operations and the converter is investigated in the two regions defined by the duty cycle ratios.

2.1 Operation in CCM

The operating modes in CCM for duty ratio less than 0.5 are described below. The four operating modes of proposed converter for $D < 0.5$ is shown in Fig. 3. The theoretical waveforms related to these modes are shown in Fig. 5.

First step of operation $(t_0 - t_1)$ - (Fig. 4 (a)): Switches, $S_1$ and $S_2$ are in off state and the inductor current decreases linearly. While the $C_{int}$ capacitor and the inductor $L_1$ are being charged from the input power source, the inductor $L_2$ and the capacitors $C_{out}$ and $C_{o2}$ supply power to the load.

Second step of operation $(t_1 - t_2)$ - (Fig. 4 (b)): In this step of operation, $S_1$ remains in off state and $S_2$ is switched on. The energies from the input source and inductors are transferred to both the capacitor $C_{out}$ and the load.

Third step of operation $(t_2 - t_3)$ - (Fig. 3 (a)): This step of operation begins when $S_2$ is turned off. The topological structure and the operation of this step are similar to the first step of operation.

Fourth step of operation $(t_3 - t_4)$ - (Fig. 3 (c)): During this step of operation, switch $S_1$ is turned on and the switch $S_2$ remains in off state. The energy is transferred to the capacitor $C_{o2}$ and load from the input source. From the theoretical waveforms which was shown in Fig. 4, for $D < 0.5$, the equations for time intervals in terms of duty cycle, $D$ and time period, $T$ are given in (1) and (2).

The voltage gain of the proposed converter in Continuous Conduction Mode for duty cycle less than 0.5 can be obtained by determining the average voltage in inductors $L_1$ and $L_2$ during one full cycle of operation. Since this converter is composed of two conversion stages, static gain analysis can be done individually.

$$\Delta t = \Delta t_e = \frac{T(1-2D)}{2}$$  

$$\Delta t_e = \Delta t_f = DT$$  

At steady state, the average inductor voltage across $L_1$ is equal to zero, as given by (3), where $V_{in}$ is the input voltage; $V_{int}$ is the intermediate voltage and $V_o$ is the output voltage. The partial voltage gain of the first step of operation is calculated and given in (4).

$$\frac{V_{in}}{V_o} = \frac{1 - D}{2D^2 - 2D + 1}$$  

Multiplying the partial voltage gains (4) and (6), which gives equation (7), the total voltage-gain of the proposed converter in continuous conduction mode for $D < 0.5$.

$$\frac{V_{in}}{V_o} = \frac{1}{2D^2 - 2D + 1}$$  

The converter operating in CCM for duty cycle greater than 0.5 is described below. Fig. 4 illustrates the different operation steps and Fig. 6 shows the key waveforms of the proposed converter.

First step of operation $(t_0 - t_1)$ - (Fig. 4 (a)): Switches, $S_1$ and $S_2$ are in conduction state and the inductor current increases linearly. At this stage of operation, there is no energy transfer between the source and the load. The load is being powered by capacitors $C_{int}$ and $C_{o2}$.

Second step of operation $(t_1 - t_2)$ - (Fig. 4 (b)): The second operating step starts when the switch, $S_2$ is switched off and diodes $D_1$ and $D_2$ are in conducting state. The capacitor $C_{int}$ is being charged from the supply voltage $V_{in}$ and the energy from inductor, $L_1$. The inductor $L_2$ transfers its energy to the capacitor $C_{o2}$. 

![Fig. 1. Boost converter (a) Three level boost converter (b) Quadratic boost converter](image1)

![Fig. 2. Proposed boost converter](image2)
Third step of operation ($t_2 - t_3$) - (Fig. 4 (a)): This step begins when $S_2$ is turned on again. The topological condition and operation of this step are the same as the first step of operation.

Fourth step of operation ($t_3 - t_4$) - (Fig. 4 (c)): When the switch, $S_1$ is turned off, the fourth step of converter operation starts. However, switch, $S_2$ continues its conduction process. During this operation, the power from input source, energy from $L_1$, charge across $C_{\text{int}}$ and energy of the inductor $L_2$ deliver energy to the capacitor $C_{\text{o1}}$. The waveforms shown in Fig. 6 is used to determine the equations of the time intervals of the four operating steps in terms of time period and duty cycle and they are given in equations (8) and (9).

\[ \Delta t_1 = \Delta t_4 = \frac{T(2D-1)}{2} \quad (8) \]

\[ \Delta t_2 = \Delta t_3 = T(1-D) \quad (9) \]

For $D > 0.5$, the voltage gain of the proposed converter in continuous conduction mode can be determined by analysing each operating step of converter. At steady state, the average voltage developed in the inductor, $L_1$ is...
zero. Thus, the expression can be written as in (10). The partial voltage gain of the proposed converter in first operating step is given by the relationship between \( V_{in} \) and \( V_{out} \). It is determined by (11). In steady state, the average voltage across inductor, \( L_2 \) equals zero, as shown in (12). Equation (12) gives equation (13), which is the partial voltage gain of the proposed converter in its second operating step.

The partial voltage gains which are given in equations (11) and (13) are multiplied to determine the total voltage gain of the proposed converter in continuous conduction mode for duty cycle more than 0.5 and it is given in (14).

\[
2 \left[ V_{in} \Delta t_1 + \Delta t_2 (V_{in} - V_{out}) \right] = 0 \tag{10}
\]

\[
\frac{V_{in}}{V_{out}} = \frac{1}{2(1-D)} \tag{11}
\]

\[
2 \Delta t_1 V_{in} + \Delta t_2 (2V_{in} - V_{out}) = 0 \tag{12}
\]

\[
\frac{V_{in}}{V_{out}} = \frac{1}{1 - D} \tag{13}
\]

\[
G_{CM(D>0.5)} = \frac{V_{out}}{V_{in}} = \frac{1}{2(1-D)^2} \tag{14}
\]

Fig. 7 demonstrates the voltage gain of classic boost converter, basic quadratic boost converter and the proposed converter, all operating in the continuous conduction mode. It is observed from the figure that the voltage gain of the proposed converter is always greater than (or equal at D = 0.5) the gain of the classic boost converter. In this way, one can obtain higher voltages from a lower voltage, without using larger duty cycles, which results in reduction of power losses in the semiconductor devices.

For a given current ripple specifications, it is possible to obtain the value of inductances \( L_1 \) and \( L_2 \), for both the duty cycle less than 0.5 and greater than 0.5, and it is given in equations (15) to (18).

\[
L_{1(D>0.5)} = \frac{V_{out} \left[ 4D^2 - 4D^2 + D \right]}{2 \Delta t_1 f} \tag{15}
\]

\[
L_{2(D>0.5)} = \frac{V_{out} \left[ D(1 - 2D) \right]}{2 \Delta t_2 f} \tag{16}
\]

\[
L_{1(D<0.5)} = \frac{V_{out} \left[ (1-D)^2(2D-1) \right]}{\Delta t_1 f} \tag{17}
\]

\[
L_{2(D<0.5)} = \frac{V_{out} \left[ (1-D)(2D-1) \right]}{2 \Delta t_2 f} \tag{18}
\]

The equations of the current ripple in the inductor \( L_1 \) can be normalized by dividing (15) and (17) by the input current of the converter. The input current is related to output current, which results in (19) and (20). Thus, we have (21) and (23), where \( R_o \) represents load resistance. The current ripple of inductor \( L_2 \) has been normalized by dividing (16) and (18) by the output current of converter, which results in equations (22) and (24).

\[
I_{\text{norm}(D>0.5)} = \frac{I_o}{2D^2 - 2D + 1} \tag{19}
\]

\[
I_{\text{norm}(D<0.5)} = \frac{I_o}{2(1-D)^2} \tag{20}
\]

\[
\Delta I_{L1(D>0.5)} = \frac{L_{f} f}{R_o} \left( 4D^2 - 4D^2 + D \right)(2D^2 - 2D + 1) \tag{21}
\]

\[
\Delta I_{L1(D<0.5)} = \frac{D(1-2D)}{2} \tag{22}
\]

\[
\Delta I_{L2(D>0.5)} = \frac{L_{f} f}{R_o} \left( (1-D)(2D-1) \right) \tag{23}
\]

\[
\Delta I_{L2(D<0.5)} = \frac{(1-D)(2D-1)}{2} \tag{24}
\]

The normalized relative ripple current of the inductors for the two operating regions are shown in Fig. 8. The voltage ripples in the intermediate capacitor \( V_{Co1} \) and output filter capacitors \( V_{Co1} \) and \( V_{Co2} \) are determined from the expressions (25) and (26), respectively. \( V_{Co1} \) and \( V_{Co2} \) are the voltages in the output filter capacitors, \( I_o \) is the output current of the converter and \( f \) is the switching frequency of the converter.

\[
\Delta V_{Co1} = \frac{2I_o \left( V_{out} - V_{in} \right)}{C_{o1} f} \tag{25}
\]

\[
\Delta V_{Co2} = \frac{I_o \left( 2V_{Co1} - V_{out} \right)}{2C_{o2} f} \tag{26}
\]

**Fig. 7.** Voltage gain of classic boost converter, basic quadratic boost converter and proposed converter

**Fig. 8.** Normalized relative ripple current of the inductors

### 2.2 Operation in DCM

In the discontinuous conduction mode, three possible discontinuities occur in the proposed converter operation. The first two possibilities are identified by the discontinuity of current in the inductor \( L_1 \) or current in the inductor \( L_2 \). While the third possibility is indicated by the discontinuity of currents flowing in both \( L_1 \) and \( L_2 \). The first two possibilities will be called as first Partial
Discontinuous Conduction Mode (PDCM) and the third possibility will be called as Total Discontinuous Conduction Mode (TDCM). However, considering that the mean current of L1 is greater than the mean current of L2 and if the current ripple in both inductors are equal, then the current flowing in inductor L2 always cancels the current flowing in the inductor L1. Thus, in this work, the PDCM operation refers to the current discontinuity only in the inductor L2.

The analysis for the PDCM is presented for the two operating conditions defined by the duty cycle (for D < 0.5 and for D > 0.5). The six operating steps of the proposed converter in the PDCM for the duty cycle less than 0.5 are explained below. The circuit diagrams of the converter for different operation steps and the theoretical waveforms of the proposed converter are shown in Fig. 9 and Fig. 10.

**Fig. 9.** Proposed boost converter operating modes in Partial Discontinuous Conduction Mode (D < 0.5)

First operation step (t0 - t1) - (Fig. 3 (a)): The switches, S1 and S2 remain in off state and the inductor current decreases linearly. While the source V_in and L1 send energy to C_off, the inductor L2 and the capacitors C_o1 and C_o2 feed energy to the load.

Second operation step (t1 - t2) - (Fig. 9): This operation step starts when the current of L2 reaches zero, blocking D3 and D4. In this step, the C_off capacitor continues to be charged with the energy of V_in and L1, however the load is fed by the capacitors C_o1 and C_o2.

Third operation step (t2 - t3) - (Fig. 3 (b)): When the switch S2 is turned on and switch S1 remains in off state, this third step of operation starts. The current flowing through the inductors L1 and L2 increases linearly, and energy is transferred to C_o1 and the load.

Fourth operation step (t3 - t4) - (Fig. 3 (a)): During this operation step, switches S1 and S2 are in off state. The topological condition and operation of this step are the same as first mode.

**Fig. 10.** Theoretical waveforms of the proposed converter in partial discontinuous conduction mode (D < 0.5)

Fifth operation step (t2 - t3) - (Fig. 9): This mode of operation starts, when the L2 current reaches zero. The topological condition and operation of this step are the same as the second step of operation.

Sixth operation step (t3 - t4) - (Fig. 3 (c)): In this operation step, the switch S1 is turned on, and switch S2 remains in off state. During this operating mode, current flowing through the inductors L1 and L2 increase again. The capacitor C_o2 and the load receives the energy from the inductors.

The six converter operating steps in PDCM for duty cycle greater than 0.5 are described below. The converter operating modes and the theoretical waveforms are shown in Fig. 11 and Fig. 12.

First step of operation (t0 - t1) - (Fig. 5 (a)): In this mode of operation, the switched S1 and S2 are in conducting state and the current flowing through the inductors increases linearly. D1, D3 and D4 are in off state. The load is being powered by the capacitors C_o1 and C_o2.

Second operation stage (t1 - t2) - (Fig. 5 (b)): In this operating step S1 remains conducting and S2 is turned off. The currents in the inductors decrease linearly. The source V_in and inductor L1 transfers the energy to C_off however L2 transfers the energy to C_o2 and load.

Third operation step (t2 - t3) - (Fig. 11 (a)): This stage begins when the L2 current reaches zero, reverse biasing D3 and D4. The supply voltage V_in and the inductor L1 charges C_off continues to charge with the energy obtained from V_in and L1, and the load is fed by the capacitors C_o1 and C_o2.

Fourth operation phase (t3 - t4) - (Fig. 5 (a)): this operation mode starts when S2 is turned on again. In this step, the inductors store energy and capacitors C_o1 and C_o2 feed the load.
Fifth stage operation (t₄ - t₅) - (Fig. 5 (c)): When the switch \( S_1 \) is turned off, the converter shifts to this operating mode. In this mode, the source \( V_{in} \) and \( L_1 \) charge the capacitor \( C_{out} \), while the inductor \( L_2 \) delivers the energy to \( C_{out} \) and the load.

Sixth stage operation (t₅ - t₆) - (Fig. 11 (b)): This mode occurs when the current in \( L_2 \) reaches zero, and the diode \( D_3 \) is reverse biased. The topological state and operation of this step are similar to the third step.

Based on the converter operating mode waveforms shown in Fig. 10 and Fig. 12, the mean values of the voltages in the inductors \( L_1 \) and \( L_2 \) are calculated, we obtain (27) and (28), which gives the equations for the total voltage gain of the proposed converter in partial discontinuous conduction mode. The parameter \( \gamma_2 \) is a current parameter which represents the external factors that influence the static behaviour of the converter.

\[
G_{recr(n-a)} = \left[ 1 + \frac{D^2}{\gamma_2 (1 - 2D)} \right] \frac{1 - D}{2D^2 - 2D + 1} \tag{27}
\]

\[
G_{recr(n-b)} = \left[ 2 + \frac{(2D - 1)^2}{\gamma_2} \right] \frac{1}{2(1 - D)} \tag{28}
\]

3. Experimental results

A laboratory prototype of the proposed converter with a power rating of 520 W was built in order to demonstrate its operation and performance. The parameters used to design the proposed converter is given in Table 1. The power rating and rated voltage values are equal to an array of four solar photovoltaic panels, each having 130W and 17 V at maximum power. The switching frequency was chosen with the purpose of comparing the constructive aspects of this converter with the work carried out in [19].

The design parameters of the inductors and the capacitors presented in the proposed converter were calculated by considering the duty cycle, \( D = 0.79 \). The maximum current ripples of the inductors were limited to 20% of the mean value of the current in each inductor. The voltage ripples on the capacitors were limited to 1% of the mean voltage on the respective capacitor.

Fig. 13 shows the experimental waveforms of the proposed converter. The input voltage is 34 V and the mean current flowing through the inductor is 15.38 A with ripple of 9 %, which is allowable as shown in Fig. 13 (a). The intermediate voltage across the capacitor is almost 80 V and the mean current flowing through the inductor \( L_2 \) is 6.47 A, with ripple of 12 % as shown in Fig. 13 (b). The voltage stress across the switches \( S_1 \) and \( S_2 \) and maximum reverse blocking voltage across the diodes \( D_1 \) and \( D_4 \) are 190 V, which is equal to half of the total output voltage of the converter as shown in Fig. 13 (c) and 13 (d). The proposed converter has midpoint in the output port, so that the inverter can be directly connected to it without using any extra components. The voltage across each output capacitor is equal to 190 V as shown in Fig. 13 (e). The output voltage and current of the proposed converter for given specification is shown in Fig. 13 (f), and they are 380 V and 1.37 A, respectively. Fig. 14 shows the efficiency curve of the converter as a function of output power. The efficiency reaches its maximum value at the output power of 350W. Although the efficiency value is low when compared to other single-stage and high-voltage converters, similar results were found in other high gain and low input voltage converters.
Fig. 13. Experimental waveforms of the proposed converter

Fig. 14. Efficiency – output power characteristics of the proposed boost converter

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