**Low-Power, Low-Voltage Complex Gm-C Filter Structure With Self-Common-Mode Control**

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Low-Power, Low-Voltage Complex $G_m$–$C$ Filter Structure With Self-Common-Mode Control

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Abstract—This work develops a low-power and low-voltage differential $G_m$–$C$ filter structure that effectively achieves self-common-mode control (SCC), including DC stabilization and common-mode (CM) rejection, without employing extra control circuitry. The structure relies on an incorporation of voltage inverting amplifiers to make it inherently contain no CM positive feedback loops for DC stabilization, and to enable splitting of the core transconductors into pairs for CM signal rejection. A DC CM stability analysis reveals that stabilization of the SCC structure can be reached without any dedicated CM control circuitry. An analytical comparison on power consumption of a high-order lowpass $G_m$–$C$ filter implemented using an inverter-based transconductor for the SCC structure and the same transconductor with a CM control network (the Nauta’s technique) for the conventional structure indicates theoretical overhead power saving by over 50%. Furthermore, an even higher overhead power saving at over 70% can be achieved in the complex SCC $G_m$–$C$ filter because no additional inverting amplifiers are required to eliminate CM positive feedback loops in the crossing transconductors for complexification. The impact of the inverting amplifiers on the noise and frequency characteristics as well as the compensation technique are outlined to enable design optimization. The SCC filter was verified via extensive simulations of a 5th-order 1.1-MHz elliptic complex filter in a 0.18-$\mu$m CMOS process. As compared to the conventional filter counterpart with similar SNR (–63dB) and in-band/out-of-band SFDRs (~52dB/56dB), the proposed structure yields an overhead power saving by 70% with an improved figure-of-merit over 40% under a 1-V supply.

Index Terms—$G_m$–$C$ filter, transconductor, Nauta, complex filter, CMOS, common-mode, stability, positive feedback

I. INTRODUCTION

A complex filter is one of the essential building blocks in modern wireless Low-IF receivers [11]–[13]. Its main function is to remove any image signal interference coming from adjacent radio channels after an RF-to-IF down conversion. The transconductor-capacitor ($G_m$–$C$) complex filter has been an attractive filtering solution due to its suitability for high-frequency and low-voltage operation stemming from the transconductor’s simplicity and compactness [14]–[16]. Under a very low-voltage supply $V_{DD}$, it becomes increasingly challenging to implement a MOS transconductor with the capability to reject common-mode (CM) signals and prevents

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Fig. 1. Conventional differential $G_m$–$C$ filter (convention: output current flow into the transconductor with a positive voltage swing)
The recent current-recycling technique [24-25] offers a compact and low power $G_m$-C complex filter with a very competitive figure-of-merit. This technique, however, might not be applicable to a general $G_m$-C filter such as that realized from a LC-ladder prototype. Alternatively, the Nauta’s inverter-based transconductor has been widely employed in $G_m$-C filters intended for high-frequency, highly linear and large-dynamic range applications under a low-voltage supply [7]. [26–37]. However, the CM control network inside the Nauta’s transconductor, which equivalently sets $g_m = G_c$ (Fig. 1(b)), is responsible for nearly half of the filter’s total power consumption and transconductor area.

To alleviate the aforementioned problems, a power-efficient low-voltage LC-ladder-based differential $G_m$-C complex filter structure is proposed. The structure is stabilized systematically by removing all the CM positive feedback loops typically found in the conventional structure. Without employing any CMFB or CMFF technique to maximize $g_m$ or minimize $G_c$, the filter can be inherently CM stabilized, thereby achieving significant power reduction.

Section II.A introduces the low-voltage $G_m$-C filter with basic self-CM-control (SCC) that can be directly realized from a LC-ladder lowpass filter structure. The complete SCC filter structure with CM rejection ability is developed in Section II.B as a more general filter structure. An analysis on the loop gains and nodal conductances is carried out in Section II.C, D for the filter’s DC CM stability and CM gain inspection. The filter’s power efficiency is assessed in Section II.E with an overhead-power ratio between the proposed and the conventional based on the Nauta’s transconductor. Section III.A illustrates a low-power 5th-order SCC complex elliptic filter. An overhead-power comparison of the complex filter is estimated in Section III.B. Noise performance and frequency response influenced by non-idealities of the proposed structure are also studied with a frequency compensation method presented. The practical feasibility of the SCC filter is verified in Section IV with extensive simulations of the 5th-order 1.1-MHz complex elliptic filter in a standard 0.18-μm CMOS process.

II. $G_m$-C FILTER STRUCTURE WITH SELF COMMON-MODE CONTROL (SCC)

A. Basic SCC Structure with DC Stabilization

Without loss of generality, the basic self-CM-control (SCC) structure will be developed from the LC-ladder-based 5th-order $G_m$-C filter of Fig. 1(a). This is illustrated with the differential $G_m$-C filter in Fig. 2(a). Without disturbing the transfer function of the conventional filter, inverting voltage amplifiers are inserted only at the even $n$ nodes (even type) or only at the odd $n$ nodes (odd type). The inverting voltage amplifier can be simply constructed from two transconductors (the bottom of Fig. 2(a)). Since there are sign alterations of $-V_1$, $-V_4$ and $V_2$, $-V_3$ in Fig. 2(a) as compared to the node voltages in the conventional filter, this basic SCC filter thus necessitates cross-over connections of $C_{13}$ and $C_{35}$.

The key purpose for the inclusion of the inverting amplifiers is to eliminate CM positive feedback loops normally existing in the conventional differential filter structure. This can be explained by considering the CM equivalent circuits of the SCC $G_m$-C filter structures. As shown in Fig. 2(b), the associated CM feedback loops (dash circles in the figures) are all in a negative feedback manner. Thus, the proposed structure requires no additional circuitry to stabilize the CM voltages inside each of the transconductors. This significantly helps save power consumption and silicon area compared to the conventional structure. The extra power and area consumptions added to the core transconductors, $G$, are mainly from the inverting voltage amplifiers.

With the inclusion of the inverting amplifiers, this SCC structure might look similar to the biquadratic-based $G_m$-C filter in [38]. However in this case, there is no requirement to load the output of each transconductor with a small adjustable
he degree of multiple loops such as the CM
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non the loops still remain in a negative feedback manner.
By inspecting the circuits in Fig. 2, it is clear that the DC
Common-mode rejection ratio (CMRR) of unity. In order
to maintain the DC-stabilizing feature and simultaneously allow
circuits in Fig. 2(a) are modified into the complete SCC structure in Fig. 3(a) without disturbing
the original DM response with the modified transconductors
\( G_{\text{cm}} = (1 \pm \delta)G/2 \) and \( G_{\text{in}} = (1 \pm \delta)G/2 \). Note that \( \varepsilon \) and \( \delta \) are of
the same polarity and \( 0 < (\varepsilon, \delta) \leq 1 \) or \( -1 < (\varepsilon, \delta) < 0 \). This
complete SCC structure, still preserves the original low-power property where the total transconductance value of the core
transconductors and the inverting amplifiers remains unchanged.

When \( (\varepsilon, \delta) \neq 0 \), it can be seen from the corresponding CM
equivalent circuit in Fig. 3(b) that the associated CM feedback
loops still remain in a negative feedback manner. Moreover,
there is a certain degree of CM current cancellation between
the shaded transconductor pairs, \( G_{\text{sh}} \) and \( G_{\text{sh}} \) as well as the
non-shaded pairs, between \( G_{\text{sh}} \) and \( G_{\text{sh}} \) due to the presence of
the inverting amplifiers. By inspecting the DM and CM signal
excursions inside the \( G_{\text{sh}} \) pairs and the \( G_{\text{sh}} \) pairs, it suggests
that these transconductor pairs basically resembles CM/DM-
FF operation (with shared inverting amplifiers) at the
structural level as compared to the circuit-level implementation found in [21-23]. Such similarity renders the
forward CM transconductance from \( j \)-th node to \((j+1)\)-th node, \( G_{\text{cm}} = G_{\text{cm}} \), and the backward CM transconductance from \( j \)-th
to \((j-1)\)-th node, \( G_{\text{cm}} = \varepsilon G_{\text{cm}} \).

If \( \varepsilon = \delta = 0 \), one may hope to enjoy a perfect CM rejection. However, since all the filter’s internal nodes (except the first
and last nodes) becomes a DC CM open circuit (zero conductance) and the filter stays right at the borderline
between DC stable and unstable regions. This issue will become clearer with the CM analysis presented in the following
subsection. Specifically for \( \varepsilon = \delta = +1 \), the
transconductors \( G_{\text{cm}}, G_{\text{cm}} \) would vanish and the
inverting amplifiers associated with them become redundant.
Thus the structure is simply reduced to the original even-type (odd-type) basic SCC filter of Fig. 2(a). Therefore the complete
SCC filter is a more general structure that covers both odd- and even-type basic SCC filters.

C. DC and Common-Mode Stability Inspection

Fig. 4(a) shows the DC CM equivalent circuit of the proposed SCC filter structure for DC stability verification via an
analysis of the DC loop gains. To enable the use of the
analysis for DC stability discussion on the conventional filters
with other CM control techniques, the CM output conductance
\( g_{\text{oc}} \) of each \( G_{c} \) (except the input \( G_{i} \) for ease of analysis) is also
included. The factor \( \gamma \) represents the inverting amplifier’s
voltage gain which may be different from \(-1\). The parameters
\( G_{\text{cm}}, G_{\text{cm}} \) are the DC CM conductance looking from the \( j \)-th
node to the right side and the left side, respectively. According
to these conductance definitions, it follows that
\( G_{1} = G_{N} = 2g_{\text{oc}} + G_{c}, \) and \( G_{j} \) for \( j = N-1, N-2 ..., 1 \) can be calculated recursively as
\[ G_{j} = G_{\text{oc}} - \frac{G_{j}}{4G_{j-1}} \left[ (1 + \gamma) \varepsilon (1 - \gamma) \right] \left( (1 + \gamma) \mp \varepsilon (1 - \gamma) \right]. \] (1)
Similarly, \( G_{j} \) for \( j = 2, 3 ..., N \) can be expressed as
\[ G_{j} = G_{\text{oc}} - \frac{G_{j}}{4G_{j+1-1}} \left[ (1 + \gamma) \varepsilon (1 - \gamma) \right] \left( (1 + \gamma) \mp \varepsilon (1 - \gamma) \right]. \] (2)

Similar to the analysis in [39], the effective DC loop gain \( LG_{j} \) at the \( j \)-th node, for \( j = 1, 2, ..., N \) in Fig. 4(a), can be derived in terms of the \( j \)-th conductances from the two possible feedback formations in Fig. 4(b), and their corresponding current
feedback system in Fig. 4(c) as
\[ LG_{j} = 2 \left( G_{j} + \hat{G}_{j} \right) / 2G_{\text{oc}}. \] (4)

It is known that a negative feedback loop gain indicates stability regardless of its magnitude. On the other hand, a
positive loop gain can indicate stability only if its magnitude is
less than unity. For the case of multiple loops such as the CM
DC equivalent circuit of Fig. 4(a), all the loop gains \( LG_{j} \) must be
less than unity to indicate overall DC stability, i.e., \( LG_{j} < +1 \) for all \( j = 1 \) to \( N \).
It is also worth exploring the total grounded DC CM conductance, \(G_{ij}\), at the \(j^{th}\) node as an alternative to \(LG_i\) for stability inspection. From the feedback system of Fig. 4(c), the loop gain, \(L_{ij}\), can be directly linked with \(G_{ij}\) by
\[
G_{ij} = i/V_{cj} = 2g_{oc} \left(1 - LG_i\right)
\]
(5)
for \(j = 1, 2, ..., N\). This total conductance \(G_{ij}\) of Fig. 4(a)–(b) can also be seen from the circuit perspective, as the sum of two conductances \(G_i\) and \(\hat{G}_j\) subtracted by the excess (common) output conductance \(2g_{oc}\), i.e.
\[
G_{ij} = G_i + \hat{G}_j - 2g_{oc}
\]
(6)
for \(j = 1, 2, ..., N\). With the \(LG_j\) expression in (4), the conductance \(G_{ij}\) relations in (5) and (6) are directly related.

The filter is DC stable if this total conductance is positive, i.e., \(G_{ij} > 0\), which is the same condition as the stable feedback loop condition of \(LG_i < 1\) and this can also be seen from (5). Thus, the condition “\(LG_i < 1\)” or “\(G_{ij} > 0\)” are equivalent for stability inspection. In the following discussion, only \(G_{ij}\) will be used for stability assessment. The nodal conductance \(G_i\) and \(\hat{G}_j\) from (1) and (2) can be summarized in Table I with \(\gamma = +1\) for the conventional \(G_{mC}\) filter structure of Fig. 1 and with \(\gamma = +1\) for the SCC \(G_{mC}\) filter structure of Fig. 3. Note also that if \(\varepsilon = \delta = \pm 1\) for \(\gamma = -1\), the SCC structure simply converges to the basic SCC \(G_{mC}\) filter structures in Fig. 2.

Since the pseudo-differential inverter-based transconductor (\(M_1−M_4\) in Fig. 5) will be the transconductor choice for the implementation and verification of the SCC filters in Sections II and III, it is instructive to use the CM analysis to examine DC stability in the conventional \(G_{mC}\) filters of Fig. 1 based on such a transconductor. This complementary inverter-based transconductor is a core part of the complete Nauta’s transconductor [26]–[28] in Fig. 5 where a CM control network is also included. By using Table I, under the condition \(\gamma = +1\) (“\(\gamma^\prime\)” amplifiers associated with \(G_c^\prime\) and \(G_{\hat{c}}^\prime\) in Fig. 4 become redundant), \(\varepsilon = \delta = +1\) and \(g_{oc} \approx 0\) as no CM control network is added and the transconductor ideally possesses a zero output conductance, with \(N = 0\) odd this renders \(\hat{G}_j = G_j \approx -G_i\) and \(G_{\hat{c}}\) for even \(\gamma^\prime\)th and odd \(\gamma^\prime\)th nodes respectively. This consequently produces \(G_{ij} = -2G_i\) for even \((\gamma^\prime)\) nodes and \(+2G_i\) (odd \((\gamma^\prime)\) nodes) indicating an unstable filter. It is also important to note that for \(\gamma = +1\) and \(g_{oc} \approx 0\), even a perfect CM-rejection transconductor (i.e., \(G_i = 0\)) could only give \(G_{ij} = 0\) with DC stability cannot be guaranteed. The conventional filter can become stable by adopting the CM control network of the Nauta’s transconductor (Fig. 5), which makes \(g_{oc} = G_i\). Note that the Nauta transconductor’s core possesses the same value of DM and CM transconductances, i.e., \(G = G_c\) while its CM control network provides a zero DM transconductance with a CM transconductance of \(G_i\). To simplify the analysis description, we firstly choose to omit the CM control network at the first and last nodes, i.e., by setting \(g_{oc} = 0\) for \(j = 1\) and \(N\), while still keeping \(g_{oc} = G_i\) for \(j = 2, 3, ..., N−1\). Since \(\hat{G}_1 = G_1 \approx +G_i\), the first row of Table I gives \(\hat{G}_j = G_j \approx +G_i\) for \(j = 2, 3, ..., N−1\), and \(G_j = \hat{G}_{N−1} = -G_i\) and \(G_{N−1} = 0\) for all \(j = 1, 2, ..., N\). This indicates that the above \(g_{oc}\) setting yields a borderline condition between DC stable and unstable.
filter. By also setting \( g_{oc} = G_c \) for \( j = 1 \) and \( N \) as employed in the original Nauta’s \( G_m - C \) filter [7], [26-29], the DC stability can thus be guaranteed. Although this DC stabilization technique has been demonstrated to be very effective, especially under a very low-voltage supply, it is at the expense of high power and large silicon area.

In case of the SCC filter with no extra CM control circuitry in Fig. 3(a) with \( \gamma = -1 \), applying the second row of Table I to (6) renders \( G_{ij} = 2g_{oc} + \varepsilon\delta G_c \) \((G_{j+1} + G_{j+1})\) for \( j = 2, \ldots, N-1 \) where \( G_{11} = G_1 + G_c \) and \( G_{TN} = G_N + G_c \). Under a typical scenario where \( g_{oc} \approx 0 \), this simplifies \( \tilde{G}_1 \) and \( \tilde{G}_j \) in Table I to

\[
G_j \approx + \varepsilon\delta G_c G_{j+1} \quad \text{for} \quad j = 1, 2, \ldots, N-1 \quad \text{and} \quad \tilde{G}_j \approx + \varepsilon\delta G_c G_{j+1} \quad \text{for} \quad j = 2, 3, \ldots, N.
\]

Since \( \tilde{G}_1 = G_N \approx +G_c \), this further yields \( G_j \) and \( \tilde{G}_j \) with \( N = \text{odd} \), to \( G_j = \tilde{G}_j \approx + \varepsilon\delta G_c \) with \( G_j \approx + \varepsilon\delta G_c \) for \( j = \text{even} \) and \( G_j = \tilde{G}_j \approx + \varepsilon\delta G_c \) with \( G_j \approx + \varepsilon\delta G_c \) for \( j = \text{odd} \). Moreover, with the condition \( g_{oc} \approx 0 \), these basic SCC filters possess \( G_1 = \tilde{G}_N \approx +G_c \), \( G_1 = \tilde{G}_N = G_c \) for \( j = 2, \ldots, N \), and \( \tilde{G}_1 = +G_c \) for \( j = 1, \ldots, N-1 \) resulting in \( G_{j+1} \approx +G_c \) for all \( j \) which is higher than those from the SCC filters at \( j = \text{even} \) implying a more stable condition offered by the basic SCC filters. Conclusively, the inclusion of the inverting amplifiers in the SCC filters fundamentally makes all of the total node conductances positive. As a result, these SCC filter structures are inherently DC stable.

When \( \varepsilon, \delta \) are close to zero with \( N = \text{odd} \), then \( G_{ij} \) also approaches zero for \( j = \text{even} \). This simply pushes the filter very close to the unstable region. Although a CM control network can be included (i.e. to set \( g_{oc} >> 0 \)) to guarantee stability, this may inevitably incur significant cost to power consumption. A more practical approach is to keep the condition \( 0 < (\varepsilon, \delta) < 1 \) or \(-1 < (\varepsilon, \delta) < 0 \) and find a suitable trade-off between the stability and CM rejection for a particular filter implementation. This will be discussed in the next subsection.

**D. DC CM Gain Analysis and Design Trade-off**

The DC CM voltage at each stage, \( V_{Cj} \) of the SCC Filter in Fig. 4(a) for \( j = 2, 3, \ldots, N \) can be expressed for \( N = \text{odd} \) (even) as

\[
V_{Cj} = V_{Cj+1} \frac{G_c}{2} (1+1), \quad j = \text{even} \quad (7a)
\]

\[
V_{Cj} = V_{Cj+1} \frac{G_c}{2} (1+1), \quad j = \text{odd} \quad (7b)
\]

If a perfect inverting amplifier is assumed, i.e., \( \gamma = -1 \), the magnitude of these DC CM voltages become

\[
|V_{Cj}| = |V_{Cj+1}| G_c G_{j+1} \quad (7c)
\]

for \( j = 2, 3, \ldots, N \) and \( V_{C1} = |V_{C2}| G_c G_{2+1} \). Following the \( G_i \) and \( \tilde{G}_j \) values of the SCC filter with \( g_{oc} \approx 0 \) in Section II.C, we have \( G_{11} = 2G_c \) for \( N = \text{odd} \) (only an odd-order filter is considered due to its popularity over its even-order counterpart). If \( G_{ij} = G_c \), the DC CM voltage at first node \( V_{Cj} \) from the CM input voltage \( V_{ic} \) then becomes \( V_{Cj} = V_{ic}/2 \) for \( N = \text{odd} \). Therefore the \( N^{th} \)-order filter’s CM DC gain, \( A_{cm} \), can be found by using (7c) recursively as

\[
A_{cm} = \frac{V_{Cj}}{V_{ic}} \frac{1}{2} \left( \frac{\varepsilon}{\delta} \right)^{N-1} \quad (8)
\]

The above equation (8) indicates that a small \( \varepsilon/\delta \) ratio is required for a good CM rejection. As already shown in Section II.C, with \( N = \text{odd} \), the product of \( \varepsilon/\delta \) should be sufficiently large to obtain a positively large \( G_{ij} (= +2\varepsilon\delta G_c) \) at \( j = \text{even} \), for a high degree of DC stability. As a consequence, there is a design trade-off for the odd-order SCC filter between the stability (i.e., \( G_{ij} \) values) and the DC CM gain (\( A_{cm} \)), by balancing \( \varepsilon \) and \( \delta \) to provide a stable filter with CM rejection that meets the required specifications.

**E. Overhead Power Comparison: Inverter-based Pseudo-Differential Transconductor Case**

In order to quantify the power saving offered by the SCC structures, a comparison between the overhead power consumption required for CM stabilization in an \( N^{th} \)-order lowpass \( G_m - C \) filter using the proposed and conventional structures is given. Due to its class-AB operation and versatility for a very low supply voltage, the complementary inverter-based pseudo-differential pair is chosen as the core transconductor \( G \) of the filters. In the conventional structure, each of these individual transconductors is equipped with the CM control network which resembles a complete Nauta’s transconductor [7], [26]-[30]. In the SCC structures of Fig. 2(a) and Fig. 3(a), the same core transconductor is also employed to implement the inverting amplifiers.

Since the relation between the quiescent supply current and transconductance is approximately linear in the inverter-based transconductor, the overhead power comparison can be directly related to the added transconductance for CM stabilization and control. In the conventional \( N^{th} \)-order lowpass \( G_m - C \) filter using the Nauta’s type CM network, it is straightforward to show that the added transconductance is \( G_{Cob} = (2N+1)G \). In the SCC \( N^{th} \)-order filter counterparts, the added transconductance is from the inverting amplifier, which requires \( 2 \alpha \) basic units (\( G / 2 \)) of the pseudo-differential transconductors for each implementation, e.g. \( \alpha = 1 \) as in Fig. 2(a) and Fig. 3(a). For the basic even-type SCC filter structure similar to the left one in Fig. 2(a), its \( G_{Cob} \) is equal to \( \alpha N G \) and \( \alpha(N-1)G \) for \( N = \text{even} \) number and odd number, respectively. While for the basic odd-type SCC structure (the right one in Fig. 2(a)), the \( G_{Cob} \) becomes \( \alpha N^2 G \).
respectively for \( N = \text{even} \) and \( \text{odd} \). Whereas for the SCC structure as in Fig. 3(a), the \( G_{\text{cm}} \) is \( \alpha N G \) for even and odd \( N \). Therefore, the overhead power ratio, \( OPR \), between the conventional and the basic SCC or the SCC filters is given by

\[
OPR = \left( 2N + 1 \right) \left( N + c \right),
\]

where \( c = 0 \) for the SCC structure with \( N = \text{even} \) and for both the basic \( \text{even} \)- and \( \text{odd} \)-type SCC filters. But for the basic SCC structures with \( N = \text{odd} \), \( c \) becomes \(-1 \) and \(+1 \) for the \( \text{even} \)- and \( \text{odd} \)-type configurations, respectively. Specifically for a 5th-order lowpass filter and \( \alpha = 1 \), equation (9) gives \( OPR = 11/4 \) (11/6) = 2.75 (1.83) for the \( \text{even} \)- (odd-) type basic SCC filter in Fig. 2(a) and \( OPR = 11/5 \) = 2.2 for the SCC filter in Fig. 3(a). The equation also suggests that for a very high order filter, \( N \gg 1 \), the \( OPR \) converges to 2 which is equivalent to 50% overhead-power saving. This implies that, by using the inverter-based pseudo-differential circuit as the core transconductor, the conventional filter structure essentially requires twice as much overhead power as that required in the SCC structures for CM stabilization. Plot of the \( OPR \)’s versus \( N \) using (9) is displayed in Fig. 6.

### III. LOW-POWER DIFFERENTIAL COMPLEX GM-C FILTER USING SELF-CM-CONTROL STRUCTURE

#### A. Self-CM-Controlled (SCC) Differential Complex GM-C Filter with Common-Mode Rejection

In the conventional complexification technique for differential GM-C filters, appropriate pairs of crossing transconductors are introduced between \( I \) and \( Q \) lowpass filter (LPF) sections. These include one crossing transconductor pair, \( G_{ij} (= a_i C_i) \), for each grounded capacitor \( C_i \) (as also shown in Fig. 7(a)), and four crossing transconductor pairs, \( G_{ij} (= a_i C_i) \), for each floating capacitor \( C_i \), where \( a_i \) is the center radian frequency of the complex filter [5], [7], [29-30], [40]. Since these \( G_{ij} \)s and \( G_{ij} \)s are connected in a head-to-tail fashion similar to those core transconductors, \( G_0 \)s, inside the \( I \) and \( Q \) LPFs, the complexification structure inevitably introduces more CM positive feedback loops. In order to suppress the resulting CM positive feedback effect and hence stabilize the complex filter, each of these \( G_{ij} \)s and \( G_{ij} \)s must require a CM control network in addition to those already needed in the \( I \) and \( Q \) LPF sections. This, as a result, significantly increases power and silicon area.

**Fig. 7.** Implementation for complexification with \( G_{ij} \) (a) conventional (b) employing the SCC feedback structure from Fig. 3(a) with \( G_{ij} \) = \((1 \pm \varepsilon)G_{ij}/2, G_{ij} = (1 \pm \delta)G_{ij}/2\).}

Fig. 7(b) shows a differential implementation example for the crossing \( G_{ij} \) at any node \( j \) with grounded \( C_j \) where the \( I \) and \( Q \) sections utilize the proposed SCC filter structure from Fig. 3(a) and each \( G_{ij} \) in Fig. 7(a) has been split into a pair of \( G_{ij} \)s and \( G_{ij} \)s as similar to the SCC structure in Fig. 3(a) with \( G_{ij} = (1 \pm \varepsilon)G_{ij}/2, G_{ij} = (1 \pm \delta)G_{ij}/2\). Co-operation with two half-sized inverting amplifiers already existed in the \( I \) and \( Q \) sections gives two necessary differential negative feedback loops for complexification. Since each of these loops essentially involves one inverting amplifier, this thus prevents CM positive feedback loops inevitably introduced in the conventional differential complex filter (Fig. 7(a)). Regard to a CM signal, the second row of Table I can also be applied to Fig. 7(b) for calculating the CM conductance \( G_{j i}(Q) \) looking into the complexification \( G_{j i}(Q) \) \((G_{j i}(Q) = \text{network from the } I \text{ (} Q \text{) section at } j^\text{th} \text{ node as influenced by the } G_{j i}(Q) \text{ from the opposite } I \text{ (} Q \text{) section, i.e., } G_{j i}(Q) \approx +\varepsilon G_{j i}(Q) \approx G_{j i}(Q)^{-1} \text{. The offsets } \varepsilon \text{ and } \delta \text{ can thus be assigned to modify the resultant total CM nodal conductance, } G_{j i}(Q) \text{ on both } I \text{ and } Q \text{ sections namely } G_{j i}(I) \text{ and } G_{j i}(Q) \text{. This complexification technique for } G_{ij} \text{s can be directly applied for } G_{ij} \text{‘s (split into } G_{ij} \text{ and } G_{ij} \text{ with } G_{ij} = (1 \pm \varepsilon)G_{ij}/2, G_{ij} = (1 \pm \delta)G_{ij}/2 \text{) and this eventually renders a fully-functional low-power } 5^\text{th}-\text{order} \text{ SCC complex filter as shown in Fig. 8 (illustrated with } \varepsilon, \delta = 0). \text{ }

The ideal inverting amplifiers with perfect matching among \( G_{ij} \)’s and \( G_{ij} \)’s (\( \varepsilon, \delta = 0 \)) would result in a complete CM signal cancellation from the \( I \) section to \( Q \) section and vice versa, i.e. \( G_{ij} \)’s and \( G_{ij} \)’s become open circuit for CM signal. This would basically isolate \( I \) and \( Q \) sections from each other yielding the complex filter’s CM response and stability characteristic that closely converges to those of the two separate stable SCC LPFs. Thus, it follows that the complex filter of Fig. 8 requires neither extra CM control network nor additional inverting amplifiers, apart from the existing ones in the \( I \) and \( Q \) LPF sections. As a consequence, the proposed SCC filter structure of Fig. 3(a) is even more efficient in terms of power and area consumptions when utilized for complex filter implementations.

**An impact by the inverting amplifier’s finite bandwidth on the imbalances of the \( I \) and \( Q \) signals from the required quadrature phase shift may be investigated by considering only the \( even \) nodes for simplicity. A differential–mode voltage at the node \( j \) (for \( j = 2, 4 \ldots \)) of the combined \( I-Q \) sections can be given by**
The above equations suggest that the perfect quadrature phase relations between the I and Q voltages can be realized by setting $G_{v_{ec}(j)} = G_{v_{ec}(k)}$ with $e_i = -\delta_i$ (including $e_i, \delta_i = 0$ as in Fig. 8) because the factors $\gamma$ associated with the inverting amplifier’s response are perfectly balanced within the $I$ and $Q$ sections. Since the same conclusion applies for the $odd$ nodes, it can be deduced that the complex filter’s balanced characteristic between $I$ and $Q$ sections can be maintained regardless of the inclusion of the inverting amplifiers in the differential SCC complex filter. The crossing $G_{v_{ec}}$, $G_{v_{ec}}$, network renders a negative CM conductance $G_{v_{ec}(k)}$ for $e_i = -\delta_i$ (non-zero values). A similar recursive calculation on the second row of Table I suggests that if this negative $G_{v_{ec}(k)}$ is applied to the $odd$ nodes only, it would effectively modify the original $G_{v_{ec}}$’s of the simple SCC complex filter (with $e_i = \delta_i = 0$) such that the $G_{v_{ec}}$’s at $j = odd (even)$ is decreased (increased) from $+2G_e (+2\alpha G_e)$. This in turn helps reduce the difference of the resultant $G_{v_{ec}}$ within the SCC complex filter and bring the quiescent CM DC voltage levels (including the bias voltages) among all the nodes closer to each other. However, to ensure the SCC complex filter’s stability with this $e_i = -\delta_i$ condition, the magnitude of $e_i, \delta_i$ has to be sufficiently small so that all the modified $G_{v_{ec}}$’s remained positive.

B. Overhead Power Consumption: An Inverter-Based Pseudo-Differential Transconductor Study Case

By using the overhead power ratio OPR, the complex $G_{v_{ec}}$ filters based on the conventional and SCC structures are compared in terms of the added power consumption necessary to achieve the CM DC stabilization. Since the complex filter with the elliptic characteristic is the main focus in this work, only the ratio analysis for an odd-order filter is given. In the conventional structure, it requires that the CM stabilization network of the Nauta’s type be employed for all the core and the crossing transconductors $G$’s, $G_{v_{ec}}$’s [7, 29-30]. By contrast, no additional circuit is required in the SCC filter, since the embedded inverting amplifiers readily provide CM negative feedbacks for both internal and cross-coupling loops.

Fig. 8. Proposed low-power SCC $G_{v_{ec}}$ complex filter structure with CM rejection where $G_{v_{ec}} = (1\pm\alpha)G/2$, $G_{v_{ec}} = (1\pm\alpha)G/2$, $\alpha = 1$ and $e_i, \delta_i = 0$. 
Fig. 9. Overhead power ratio by the SCC N-th order elliptic complex filter from (28) (N = order of the I, Q lowpass sections) with \( \alpha = 1.0, 1.5 \).

Similar to the analysis in Section II.E, the overhead power comparison is determined by the added transconductance for CM stabilization. For complexification, since each of the N grounded capacitors requires two crossing transconductors \( G_{ij} \) and each of the \((N-1)/2\) floating capacitors needs eight crossing transconductors \( G_{aij} \), the OPR can be written as

\[
OPR = \left( \frac{2(2N+1) + \sum_{i=1}^{N} 2G_{aij}}{G} \right) \left/ \left( \frac{N-1}{2} \frac{8G_{0j}}{G} \right) \right. \right/ \left( \frac{\alpha}{2N} \right) \quad (11)
\]

with \( G_{aij} = \alpha \omega C_i \) (\( i = 1, \ldots, N \)), \( G_{ai2j} = \alpha \omega C_k \) (\( j = 1, \ldots, (N-1)/2 \)). By putting the average values of \( G_{aij} \) and \( G_{ai2j} \), as \( \overline{G}_{aij} \) and \( \overline{G}_{ai2j} \), respectively, (11) is simplified to

\[
OPR = \left( \frac{2(2N+1) + \sum_{i=1}^{N} \overline{G}_{aij}}{\overline{G}} \right) \left/ \left( \frac{N-1}{2} \frac{8\overline{G}_{0j}}{\overline{G}} \right) \right. \right/ \left( \frac{\alpha}{2N} \right) \quad (12)
\]

To investigate how the OPR is dependent on the complex filter’s bandwidth (2\( \omega_h \)) and center frequency (\( \omega_h \)) of the I/Q LPF section, the bandwidth \( \omega_h \) can be approximately related to the core transconductance, \( G \), and the average grounded capacitance, \( \overline{C} \) (\( \overline{C} = G/\omega_h \)) by \( \omega_h \cong \overline{G} \overline{C} \). Together with the average value of the floating capacitance \( \overline{C}_{ij} (\overline{G}_{aij}/\omega_h) \), the OPR in (11) can alternatively be expressed as

\[
OPR = \left( \frac{2(2N+1) + (\overline{G}_{aij}/\omega_h)}{\overline{G}_{ij}} \right) \left/ \left( \frac{N-1}{2} \frac{8(\overline{G}_{0j}/\overline{C})}{\overline{G}_{ij}} \right) \right. \right/ \left( \frac{\alpha}{2N} \right) \quad (13)
\]

For a special case of the elliptic complex filter with \( \omega_h \overline{G}_{ij} = 1/2 \) and \( \overline{C}_{ij}/\overline{C} = 1/4 \) as in the design in Section IV, both (12) and (13) yield \( OPR = 5/\alpha \), e.g., the OPRs are 5.0 and 3.3 for \( \alpha = 1.0 \) and 1.5, respectively. Note that, the factor \( \alpha \) plays a vital role in the filter’s noise performances as will be analyzed in Section III.D. This specifically indicates that based on the inverter-based pseudo-differential transconductors, the conventional complex filter requires at least three times as much overhead power as that required in the SCC complex filter for CM stabilization. The significant power saving in the proposed complex filter simply stems from the fact that there is no overhead power required for those crossing transconductors \( G_{aij} \).

Plots of the OPRs using (13) are illustrated in Fig. 9 showing how OPR is related to the filter’s order \( N = \) (odd) and the bandwidth/center frequency ratio \( \omega_h/\omega_0 \) for \( \alpha = 1.0 \) and 1.5. As evident from the plots, the OPR is almost constant against the filter’s order (Fig. 9(a)). Also for a high-order filter (\( N \geq 5 \)), the OPR is inversely proportional to \( \omega_h/\omega_0 \) (Fig. 9(b)). This is mainly because of the relation \( \omega_h \propto G \) where a larger \( \omega_h \) results in a larger \( G \), making the effect of no added power in \( G_{aij} \) in the SCC filter less significant.

C. Effect of Inverting Amplifier on Noise Performance

The impact of the inverting amplifiers on the noise characteristic of the SCC filter is analyzed using a second-order circuit, which serves as the core structure of both higher-order and complex filters, as shown in Fig. 10 where \( G_{vfa} = (1+\varepsilon)G_f/2 \), \( G_{vfb} = (1+\delta)G_f/2 \) with \( G_f = G \) for the lowpass sections’ transconductors, and \( G_f = G_{aij} \) and \( G_{aiij} \) of the crossing transconductors. The inverting amplifier comprises a pair of pseudo-differential transconductors, with \( G_{vim} = \alpha \epsilon G_f \). The conductor–capacitor networks, \( (g_s + sC) \) and \( (g_s + sC_i) \) have been included to model adjacent second-order stage loading. Also shown in Fig. 10 are noise sources, which model the thermal noise associated with the transconductors \( G_{vfa} \), \( G_{vfb} \), and \( G_{vim} \), where \( \overline{i}_{vfa} = (1+\varepsilon)\overline{i}_{vm} \) and \( \overline{i}_{vfb} = (1+\delta)\overline{i}_{vm} \) with \( \overline{i}_{vm} = \gamma_c k T G_f \) and \( \overline{i}_{vm} = \gamma_c k T G_{fin} / 2 = \alpha \epsilon \overline{i}_{vm} / 2 \). The conductors’ noise may also be included but this is omitted for simplicity. The mean-square noise voltages \( \overline{v}_{aij}^2 \) and \( \overline{v}_{aiij}^2 \), generated from these uncorrelated current noise sources were analyzed as summarized in Table II.

For the mean-square noise voltages due to \( \overline{i}_{aij}^2 \) and \( \overline{i}_{aiij}^2 \) in Table II, they are the same as the noise transfers in the second-order filter without the inverting amplifier. This thus indicates no difference between the noise characteristics of the SCC and conventional filters due to these sources. On the other hand, the mean-square noise voltages due to \( \overline{i}_{aiij,A,B}^2 = \alpha \epsilon \overline{i}_{vm} / 2 \) indicate that the noise contribution from the inverting amplifier’s transconductors is dependent on the factor \( \alpha \epsilon \).
In case of a lowpass filter design using the SCC structure with small $\varepsilon$, $\delta$ and $\alpha_\varepsilon = 1$, i.e., $G_{inv} = G_F = G$, the mean-square noise transfers due to $\gamma_{inv}(A,B)$ is similar to those due to $\gamma_{inv}(A,B)$’s. However, because the total conductance is smaller, the SCC filter structure therefore exhibits less total noise as compared to the conventional filter with CM control networks. Specifically at low frequencies, the SCC lowpass filter can provide total thermal noise reduction by a significant amount, thereby demonstrating a degree of power saving factor as discussed in Section II.E.

In case of a complex filter design, the crossing transconductors $G_{a}$’s and $G_{a'}$’s can be treated as $G_F$ in the second-order circuit of Fig. 10. The values of $G_{a}$’s are typically larger than $G$ in the lowpass $I$, $Q$ sections depending on the $\alpha$/$\alpha_k$ ratio. As a consequence, with $G_{inv} = G_F$, the factor $\alpha_\varepsilon$ ($=G_{inv}/G_{a}=G/G_{a}$) could be much less than unity. As indicated in Table II, the noise contribution from $\gamma_{inv}(A,B)$ is essentially increased by the factor $1/\alpha_\varepsilon^2$. This adverse effect must be taken into account when designing a SCC complex filter. As adopted in the prototype filter in Section IV, a general design guideline is to select the transconductance $G_{inv}>G$ so that the factor $\alpha_\varepsilon$ is increased and the SCC complex filter exhibits an overall noise performance comparable to that of its conventional counterpart, while still enjoying a significant amount of power saving.

D. Effect of Inverting Amplifier’s Parasitic Capacitance on Frequency Response

The non-ideal effect due to the inverting amplifier’s parasitic capacitor $C_{inv}$ on the filter’s frequency response can be investigated from the single-ended 2nd-order SCC circuit as shown in Fig. 11. The impedance looking into node $X$, $Z_X$ can be expressed as

$$Z_X = \frac{sC_{inv}(G_{inv}/2)^2}{[1+\delta] + \frac{(1-\varepsilon)}{[1+\delta](\alpha_\varepsilon^2/sC_{inv})]}(1-\varepsilon) + \frac{(1-\varepsilon)}{[1+\delta](\alpha_\varepsilon^2/sC_{inv})]}.$$  

To provide insight and, at the same time, simplify the analysis, this SCC structure can be reduced to a simple even- or odd-type basic SCC structure with $\varepsilon = \delta = +1$ or $-1$, respectively where the second-order circuit is transformed into an equivalent parallel RLC circuit as also provided in Fig. 11. The equivalent series inductor $L_S$ and resistor $R_S$ are given by

$$L_S = \frac{C_{inv}}{G_{inv}}, R_S = \frac{-\alpha_\varepsilon(1/C_{inv} + G_{inv})}{C_{inv}/G_{inv}}.$$  

As indicated by (14b), the capacitance $C_{inv}$ has no impact on the inductance $L_S$. On the contrary, it goes rise to $R_S$, which is proportional to $C_{inv}$ and is of a frequency-dependent negative resistance (FDNR) type. This thus results in a higher quality factor of the parallel RLC circuit than the desired value, and the effect is more pronounced at higher frequencies. Another non-ideal effect is on the resonant frequency $\omega_\varepsilon$, defined as the frequency that yields zero imaginary part in the admittance of the RLC circuit. It is given by

$$\omega_\varepsilon = \frac{G_{inv}}{2 \sqrt{CL_S}},$$

when $C_{inv}$ approaches zero, by using the approximation $(1+x)^2 \approx 1 + (x/2)$, we have the ideal resonant frequency $\omega_\varepsilon = G_{inv}/\sqrt{CL_S}$. By rearranging (15) as follows:

$$\omega_\varepsilon^2 = \frac{1}{\omega_\varepsilon^2} + \frac{1}{(\omega_\varepsilon^2)^2},$$

and since all the variables are positive, it can be deduced that $\omega_\varepsilon > \omega_\varepsilon$. Thus, the effect of $C_{inv}$ results in a lower resonant frequency than the designed value. Both the increase in the quality factor and the decrease in the resonant frequency due to $C_{inv}$ invariably change the frequency response of the biquad circuit, and hence distort the overall frequency response of the filter. Therefore the parasitic $C_{inv}$ must be kept sufficiently small to maintain the desired response, unless a suitable compensation technique is introduced as described next.

E. Series-Resistor Technique for Parasitic Pole Cancellation in SCC Filter

As widely employed in integrated continuous-time filters, and extensively explored in [41], the technique employing a passive resistor $R_Z$ in series with the capacitor $C_1$ can be used to compensate for the effect of $C_{inv}$ from the inverting amplifier associated with $C_1$ in the 2nd-order SCC filter of Fig. 11. The resistor $R_Z$ effectively introduces a zero at $-1/R_Z C_1$ at the inverting amplifier’s input voltage. This helps cancel out the parasitic pole at $-G_{inv}/C_{inv}$ at its output voltage, thereby enabling the associated $G_{inv}/2 = (1+\varepsilon)G_{inv}/2$ to produce the output current with no magnitude or phase distortion as compared to the ideal case when $C_{inv} = 0$.

This simple series-resistor technique can be extended to compensate for the effect of $C_{inv}$ from any inverting amplifier in a general SCC filter structure. Similar to the case of Fig. 11,
the underlying compensation principle is to make sure that all
the transconductors and the floating capacitors in Fig. 3(a) and
Fig. 8 supply the current signals into the grounded integrating
 capacitors C with no frequency-response distortion. Fig. 12
shows the general schematic at the jth node of the SCC
compound filter’s I section (with \( \varepsilon \), \( \delta \) = 0). Also included in the
schematic are the compensation resistors \( R_s \)’s in series with
the grounded capacitors \( C_i \) and the floating capacitors \( C_{i+2} \),
\( C_{i-2} \). Following this, the voltage \( \tilde{v}_j \) at the inverting
amplifier’s output can be related to the voltage \( \tilde{v}_j \) at its input,
and the associated current signals injected into \( C_i \), as given by

\[
\tilde{v}_j = \frac{v_{j-1} + R_C \left( 1/I_{C_j} \right) \sum_{k} \left( c_{j+k} + t_{j-2+k} \right)}{1 + s \left( C_j / G_m \right)}
\]

(17)

where \( \sum_{k} \) represents the sum of the currents from \( G_{ci} \), \( G_{di} \),
\( \pm G_{bip} \), \( \pm G_{di+2} \), \( \pm G_{di-2} \), and \( \pm G_{i+2j} \), \( \pm G_{i-2j} \). Since \( C_{i+2} \) and \( C_{i-2} \) are
connected from the adjacent nodes, (\( j-2 \))th and (\( j+2 \))th to
the jth node, (17) can be rewritten as

\[
\tilde{v}_j = \frac{R_C \left( 1/I_{C_j} \right) \sum_{k} \left( v_{j+2-k} + t_{j-2+k} \right)}{1 + s \left( C_j / G_m \right)}
\]

(18a)

\[
\tilde{v}_j = \frac{R_C \left( 1/I_{C_j} \right) \sum_{k} \left( v_{j+2-k} + t_{j-2+k} \right)}{1 + s \left( C_j / G_m \right)}
\]

(18b)

Based on the above equations, it requires that the following
conditions be satisfied to achieve perfect compensation:

\[
R_C C_j = R_{i+j+2} C_{j-2} = R_{i+j-2} C_{j+2} = C_m / G_{m0}.
\]

(19)

The ideal relation between the input voltages and output
currents of the transconductors at jth node is restored by
applying the condition in (19) to (18) where the voltage \( \tilde{v}_j \) of
the associated inverting amplifiers can now be expressed as

\[
\tilde{v}_j = \frac{1}{s C_j} \left( \sum_{k} \left( c_{j+2-k} t_{j-2+k} \right) + s C_{j+2-k} \left( t_{j+2-k} \right) \right).
\]

(20)

It is important to note that only the correctly compensated
voltage \( v_j \) or its inverted version \( \tilde{v}_j \) (not its over-compensated
counterpart, \( \tilde{v}_j \)) are used by various transconductors, e.g. \( v_{j+2} \)
and \( \tilde{v}_{j+2} \) are used by \( G_{j+2} \) and \( G_{j+2} \), respectively in Fig. 12. Thus,
the compensation resistors \( R_s \)’s are required only for the
grounded capacitors \( C_j \) and the floating capacitors \( C_{j+2} \),
\( C_{j-2} \) at the input of the inverting amplifiers.

**IV. CIRCUIT VERIFICATIONS**

The proposed SCC complex filter structure in Fig. 8 has
been verified via simulation in a standard 0.18-\( \mu \)m CMOS
process employing an inverter-based pseudo-differential
transconductor from Fig. 5 as the core transconductor cell with
minor modification as depicted in Fig. 13(a). In this design, \( \alpha \)
is selected to be 1.5 to achieve the output noise and the
dynamic range (DR) close to that of the conventional design.
Since the common-mode \( G_{cm} \) value is identical to the
differential-mode \( G \), the value of the DC CM nodal
conductance \( G_{j}\) is well-defined where \( G_{j} \approx +2 \delta \delta_{G} \),
for \( j=even \) and \( G_{j} \approx +2 \delta_{G} \) for \( j=odd \) with \( \delta_{G} = 0 \) as discussed
in Section II.A. Therefore, similar to the technique in [7], [26-
29], at a fixed body voltage of PMOS, \( V_{bb} \), NMOS and PMOS
of the transconductor cell can be appropriately sized to set
their gate and drain DC bias voltages to \( V_{DD}/2 \) for the entire
filter without extra circuitry. However, to counter process,
temperature and supply voltage variations, a master-slave
scheme (e.g. in [23]) is utilized to automatically adjust \( V_{bb} \)
and accurately set up the required DC bias voltage. This \( V_{bb} \)
is generated from the master bias set-up circuit of Fig. 13(b)
comprising the diode-connected transconductor’s DC half
circuit in a negative-feedback servo loop. This
transconductor’s half-circuit replicates the desired DC voltage
level of the transconductors working within the filter.

The filter operates at \( V_{DD} = 1 \)V with 1.1-MHz center
frequency and 0.8-MHz bandwidth. A stabilization of the SCC
filter with \( \varepsilon = 1.0, \delta = 0.25 \) is verified in Fig. 14(a) depicting
Monte-Carlo (MC) simulations of transient response of
the output voltage converge to a stable value of \( V_{DD}/2 = 0.5 \)V after
the supply voltage being subjected to a step change from 0 to
1V (without input signal). Moreover, the histogram plots in
Fig. 14(b) and (c) compare the filter’s nodal bias voltages for
\( \varepsilon = 0 \), \( \delta = 0 \), and \( \varepsilon = -\delta = 0.075 \) (applied to \( G_{j+2}, G_{j+2} \) at \( j = 1, 3, 5 \)) with the respective means (\( \mu \)) and standard deviations
(\( \sigma \)). As predicted in Section III.A, having \( \varepsilon = -\delta \) renders the
bias voltage levels closer to \( V_{DD}/2 \) (especially those at nodes
4). Fig. 15(a) shows the filter’s frequency responses with \( \varepsilon = 0.75, 1.0 \) and \( \delta = 0.25 \). The CM frequency response is also
included in Fig. 15(a). The in-band CMRR is level is at ~43dB
and it is clear that the DC CM gain decreases with the \( \delta \varepsilon \) ratio
where its value is as closely predicted by (8). Fig. 15(b)
depicts the MC frequency response indicating that component mismatch plays role in the image-band distorted response.

An two-tone test was carried out with two input frequencies at 1.05 and 1.15MHz. Fig. 16 shows an in-band intermodulation (IM) level plot where the IIP3 values are at +3dBVrms for the SCC filter and +1dBVrms for the conventional filter. The output noise power spectral density is shown in Fig. 17 with the output noise levels (integrated from 10kHz to 10MHz) of 6.4x10^-3V2 and 6.1x10^-3V2 for the SCC and conventional filters, respectively. With the filter's passband gain of 0.5, these output noise could be respectively translated to an input-referred noise of -75.92dBVrms and -76.13dBVrms. The IM test also indicates a linear gain up to an input level of -13.0dBVrms for both filters – with the corresponding signal-to-noise ratios (SNR) of 62.9dB and 63.1dB. Following the calculation in [2], [7], where the spurious-free dynamic range, SFDR_{in} = (2/3)(IIP3_{dBVrms} – InputNoise_{dBVrms}), the in-band SFDRs have been calculated at 52.6dB (the SCC) and 51.4dB (the conventional). The out-of-band IM was also simulated with two blocker frequencies at 3 kHz and 4MHz where the corresponding SFDRs have been found at 56.3dB (the SCC) and 56.8dB (the conventional).

The conventional and proposed complex filters consume static power of 851μW and 549μW, respectively. The SCC filter prototype thus renders OPR ≈ 3.4 or 70.5% saving on the overhead power consumption with no significant deterioration on the DR. This OPR value is closely agreed with the calculated from (13) using \( \alpha = (0.88/2)/1.1 = 2.5 \), \( \frac{C_f}{C} \approx 0.23 \), and \( \alpha = 1.5 \) for this particular design. As summarized in Table III, the filters have been compared using a figure-of-merit, FoM = (Power Consumption)/(N-f{DR}) where f_c is the centre operating frequency. The calculation suggests that the SCC filter renders a significant improvement by 40% and 30% on the FoM respectively with the in-band and out-of-band SFDR.

V. CONCLUSION

A low-power \( G_m-C \) filter structure with self CM stabilization and CM rejection has been proposed. Through the use of inverting amplifiers, the proposed structure removes all the CM positive feedback loops and achieves stabilization without employing a dedicated, power-hungry CM control network usually utilized in the conventional design. The filter’s CM conductance, CM gain, frequency and noise responses have been analyzed to assist the design. With no performance degradation in terms of in-band and out-of-band SFDR or SNR, the self-CM-controlled 5th-order elliptic complex filter offers over 70% saving on the overhead power compared to the conventional design. Although the proposed \( G_m-C \) filter has been demonstrated with the inverter-based pseudo-differential transistor, the concept can be applied to a vast range of low-voltage transconductors – especially those without intrinsic capability to reject CM signals.

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| Filter type, $V_{dd}$ | Complex 5th-order elliptic, 1V |
|-----------------|-------------------------------|
| Total integrating capacitance | 151.74 pF |
| Total transconductance | 4198.29μS |
| Power consumption, $OPR$ | 851μW, 3,4 |
| Input-referred noise | -76.13dB |
| Signal-to-noise ratio (SNR) | 63.1dB |
| In-band DR: SFDR | 51.4dB |
| Out-of-band DR: SFDR | 56.8dB |
| FoM based on: In-band SFDR | 0.21 pJ |
| Out-of-band SFDR | 0.11 pJ |

Table III: Performance Comparison in 0.18-μm CMOS

Fig. 16. In-band two-tone intermodulation test

Fig. 17. Output noise power spectral density

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