Improved Model Predictive Control Strategy for Modular Multilevel Converter

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Abstract. For reducing switching frequency and decrease computation of the traditional model predictive control (MPC) for modular multilevel converter, an improved MPC strategy is proposed. The control of AC current, circulating current and capacitor voltages are realized synchronously by building multi-objective functions. Combining with capacitor voltage sorting method, MPC calculation is decreased. The switch frequency was lowered by introducing weighting factors. Capacitor voltage difference among the sub-modules is lessened through the allowable value of capacitor voltage deviation between sub-modules. The simulation results verify its correctness.

1. Introduction
Modular multilevel converter (MMC) is widely applied to high-voltage direct current, power quality control, AC drive and other high-voltage and high-power applications due to its prominent features such as modularity and cascade. But in the application of MMC, it is still urgent for MMC to solve the stability of sub-module capacitor voltages and the suppression of circulating current due to the interaction between the sub-module capacitor voltages and the circulating current. So a lot of literature has done a number of studies on it.

In [1-3], the balance strategy of the capacitor voltages for sub-modules is proposed, but the influence of the circulating current on the capacitor voltages of sub-modules is ignored. In [4], the arm inductance is used to suppress the circulating current. The method not only increases the equipment cost of the system, but also has limited effect on the suppression of the circulating current. In order to suppress double frequency circulating current in MMC, a circulating current suppressor is proposed in [5] based on double frequency negative sequence coordinate transformation. But it is more complex because of double frequency negative sequence coordinate transformation and interphase current decoupling. Model predictive control (MPC) is used to control MMC in [6, 7]. However, it is necessary to predict all possible switch state combinations of the upper and lower arms for the next cycle in each control cycle to achieve multi-objective optimization control. For a 5-level MMC, the number of sub-modules per arm is 4, and the number of switch states to be considered for each control cycle is $C_4^2 = 70$. With the increase of the number of MMC level and the number of sub-modules, the computational complexity of the switch state combinations is obviously increased, which puts forward higher requirements for the controller.

For realizing AC / DC power conversion and safe and stable operation, a MPC strategy based on $n+1$ level MMC is proposed with the control targets of AC current, interphase circulating current and capacitor voltage of sub-modules. In this strategy, the weight accumulation factors are used to fuse the multiple control objectives and to construct the multi-objective optimization functions. The strategy can reduce the calculation of MPC by combining the capacitor voltage sorting method and lower
switching frequency by introducing weight factors and shrink the difference among the capacitor voltages by giving allowable value of capacitor voltage deviation among sub-modules. The effectiveness of the strategy is verified by MATLAB simulation.

2. Mathematical model

The topology of three-phase MMC is shown in figure 1. There are three phase units in the converter, each of which consists of an upper arm and a lower arm. While each arm is connected by \( n \) identical sub-modules (SM) and a reactor in series. The reactor is equivalent to a series of inductance \( L \) and resistance \( R \), and the entire voltage of a arm is the sum of the voltage of all the sub-modules of the arm. Each sub-module has a IGBT half-bridge and a capacitor. For maintaining the relative stability of DC voltage, the total number of input sub-modules of each phase unit is fixed to \( n \) at any time.

![Figure 1. Basic structure of MMC](image)

The AC current on the grid side is \( i_k \), the AC voltage is \( u_{sk} \) \((k=a, b, c)\). The current and voltage of the upper arm of each phase are respectively \( i_{kp}, u_{kp} \), the current and voltage of the lower arm of each phase are respectively \( i_{kn}, u_{kn} \). The common DC bus voltage is \( u_{dc} \), and the circulating current is \( i_{zk} \).

According to the circuit shown in figure 1, the Kirchhoff’s law of current equation is established:

\[
\begin{align*}
\frac{1}{2} i_k + i_{zk} = i_{kp} + i_{kn} \\
\frac{1}{2} i_k + i_{zk} = i_{kp} + i_{kn}
\end{align*}
\]

The circulating current is superimposed on the upper and lower arm currents of each phase, which not only increases the rated current capacity of the power switch devices, but also increases the loss of the power switch devices. In addition, it can cause the capacitor voltage ripple easily. Therefore, it is necessary to effectively suppress circulating current.

According to the reference direction shown in figure 1, the circuits of the upper and lower arm and the DC side of each phase in MMC are as follows:

\[
\begin{align*}
\frac{u_{dc}}{2} - u_{kp} - Ri_{kp} - L \frac{di_{kp}}{dt} = u_{sk} \\
\frac{u_{dc}}{2} + u_{kn} + Ri_{kn} + L \frac{di_{kn}}{dt} = u_{sk}
\end{align*}
\]

The sub-module capacitor is \( C \), DC capacitor voltage is \( u_c \), the output voltage of the sub-module is \( u_{SM} \), the switching function of the \( k \) phase \( i \) sub-module is \( S_{imi}(m=P,N,i=1,2,\ldots,n) \), the capacitor voltage of the sub-module can be written as
\[ u_c(t + T_s) = u_c(t) + \frac{T_s i_{km}(t)}{C} S_{km} \]  

(3)

Where \( S_{km} = 1 \) if sub-module \( i \) is input, and \( S_{km} = 0 \) otherwise. According to (1) and (2),

\[ \frac{di_k}{dt} = \frac{u_{kn} - u_{kp}}{L} \frac{2}{L} u_{sk} - \frac{R}{L} i_k \]  

(4)

\[ \frac{di_{zk}}{dt} = \frac{1}{2L} u_{dc} - \frac{u_{kn} + u_{kp}}{2L} - \frac{R}{L} i_{zk} \]  

(5)

The discrete descriptions of (4) and (5) lead to the following equation:

\[ i_k(t + T_s) = \frac{T_s}{L + RT_s} \left( u_{kn}(t + T_s) - u_{kp}(t + T_s) - 2u_{sk}(t + T_s) + \frac{L}{L + RT_s} i_k(t) \right) \]  

(6)

\[ i_{zk}(t + T_s) = \frac{T_s}{2(RT_s + L)} \left( u_{dc} - u_{kp}(t + T_s) - u_{kn}(t + T_s) \right) + \frac{L}{RT_s + L} i_{zk}(t) \]  

(7)

Where \( T_s \) is sampling period, \( t \) and \( (t + T_s) \) respectively represent the current measurement value and the predictive value of the variable for the next sampling period.

3 Model predictive control

3.1 MPC Objective Functions

A MPC strategy is proposed in order to track AC current of the system in real time, to suppress circulating current and to maintain the capacitance voltage balance of the sub-modules. It can find the optimal switching sequence for the next cycle to control the AC current, circulating current and capacitor voltage simultaneously.

If sampling period is small enough, the current measurement value of \( u(t) \) can be used instead of its predictive value \( u(t + T_s) \). Let us define \( \{ \}^\star (t + T_s) \) to be the ideal value of the corresponding variable for the next sampling period, \( u_{dc} \) is assumed to be stable, that is, \( u_{dc} \) is a constant. In order to realize the accurate tracking of AC current and the goal of zero circulation, \( \star \) can be applied to (6) and (7) separately.

\[ i_k^\star(t + T_s) = \frac{T_s}{L + RT_s} \left( u_{kn}(t + T_s) - u_{kp}(t + T_s) - 2u_{sk}(t + T_s) + \frac{L}{L + RT_s} i_k(t) \right) \]  

(8)

\[ i_{zk}^\star(t + T_s) = \frac{T_s}{2(RT_s + L)} \left( u_{dc} - u_{kp}(t + T_s) - u_{kn}(t + T_s) \right) + \frac{L}{RT_s + L} i_{zk}(t) = 0 \]  

(9)

Let us use \( E \) to be the error between the predictive value and ideal value of a variable, subtracting (8) from (6) leads to

\[ E_{ik} = \frac{T_s}{L + RT_s} \left( E_{ukn}(t + T_s) - E_{ukp}(t + T_j) \right) \]  

(10)

Subtracting (7) from (9) leads to

\[ E_{zk} = \frac{-T_s}{2(RT_s + L)} \left( E_{ukn}(t + T_s) + E_{ukp}(t + T_j) \right) \]  

(11)

In order to control the AC current and the circulating current simultaneously, the objective function is obtained with the weighting accumulation to (10) and (11).
\[ f(u) = \min \left( \alpha (E_a)^2 + \beta (E_{ak})^2 \right) \] (12)

Eq. (10) and (11) can be applied to (12). The weighting factors \( \alpha \) and \( \beta \) are defined as follows:

\[ \alpha = \left( \frac{L + RT_s}{T_s} \right)^2, \beta = \left( \frac{2(RT_s + L)}{-T_s} \right)^2 \] (13)

Then Eq. (12) can be written as

\[ f(u) = \min \left( (E_{akN}(t + T_s) - E_{akP}(t + T_s))^2 + (E_{akN}(t + T_s) + E_{akP}(t + T_s))^2 \right) \] (14)

To maintain the capacitance voltage balance of the sub-modules, the objective function should be satisfied

\[ g(u) = \min \left( \sum_{i=1}^{n} \left( u_{i,N}(t + T_s) - \frac{u_{dc}}{n} \right)^2 + \sum_{i=1}^{n} \left( u_{i,N}(t + T_s) - \frac{u_{dc}}{n} \right)^2 \right) \] (15)

Eq. (13) and (14) must be satisfied \( \sum_{i=1}^{n} S_{i,1} + \sum_{i=1}^{n} S_{i,-1} = n \). For \( n+1 \) level MMC, it is necessary for the traditional MPC strategy to need calculate combination switch states in each control cycle to find the optimal switch sequence. When the number of sub-modules is large, the calculation of the switch combinations is greatly increased, and the controller is difficult to meet the real-time requirement. To reduce the calculation, this paper realizes multi-objective control by combining the sub-module capacitor voltage sorting method. The approach proposed includes three steps.

**Step 1.** This step need predict the value of of the control variables for the next sampling period.

**Step 2.** The approach sorts the sub-modules of upper and lower arms. When the arm current >0, the input sub-modules get charged, the algorithm prefers to select the sub-modules with lower capacitance voltages. Thus they are sorted in ascending order. Likewise, the sub-modules are sorted in descending order if the arm current <0.

**Step 3.** To ensure that the number of sub-modules of input in each phase unit is \( n \), there are \( n+1 \) kinds of sub-module input combinations, that is, \( n+1 \) switch sequences, as shown in figure 2. Thus the algorithm need find the optimal switching sequence only in \( n+1 \) switch sequences. The computation of each control period is reduced from \( \sum_{i=1}^{n} C_{2n}^1 \) to \( n+1 \). Then, the algorithm compares the value of the objective function corresponding to \( n+1 \) switch sequences. The sequence which can make the objective function \( f(u) \) reach the minimum value is the optimal sequence. If more than one switch sequence can make the function \( f(u) \) reach the minimum value, the switch sequence that makes the function \( g(u) \) reach the minimum value is the final solution.

![Figure 2. Module input Combination diagram](image)

**3.2. Improved MPC strategy for reducing switching frequency**

The above conventional capacitive voltage sorting method can maintain the capacitor voltage balance of the sub-modules well. However, the change of the small capacitor voltage will bring great changes to the sorting, resulting in the higher switching frequency of the sub-modules and lower MMC operating efficiency. For this, the MPC strategy using the traditional capacitor voltage sorting method is improved in this paper. The specific processing method is as follows:

1. If the arm current is >0, the prediction of the next sampling period for the capacitor voltage of the sub-module is revised to
Where $\lambda_1$ is the weight factor whose value is greater than 1.

(2) If the arm current is $<0$, the prediction of the next sampling period for the capacitor voltage of the sub-module is revised to

$$u_{c_i}(t + T_s) = u_{c_i}(t) + \lambda_2 \frac{T_i}{L} i_{km}(t) S_{kmi} \quad (17)$$

Where $\lambda_2$ is the weight factor whose value is less than 1.

Although the above method can effectively reduce the switching frequency of the devices, there is too much difference in sub-module capacitor voltages. When the deviation between the maximum and minimum capacitor voltages of the sub-modules exceeds a certain range, the distortion rate of output voltage will increase and the fluctuation of the capacitor voltages will be aggravated.

To ensure that the difference in capacitor voltages is not too large, the algorithm first define

$$\Delta c_{max_{max}, min_{max}}, max_{min}, min_{min} = \frac{\Delta c_{max}}{max_{max}} - \frac{\Delta c_{min}}{min_{min}} \quad (18)$$

Then the algorithm gives a allowable deviation $\Delta u_{cM}$ among capacitor voltages of sub-modules. To ensure $u_{c_{max}}$ sub-module is cut off and $u_{c_{min}}$ sub-module is input, the processing is as follows:

(1) When $i_{km} > 0$, the sorting number of $u_{c_{max}}$ sub-module is set to $n$, and the sorting number of $u_{c_{min}}$ sub-module is set to 1. Then, the capacitor voltages of the remaining n-2 sub-modules of the arm is processed according to Eq. (16).

(2) When $i_{km} < 0$, the sorting number of $u_{c_{min}}$ sub-module is set to $n$, and the sorting number of $u_{c_{max}}$ sub-module is set to 1. Then, the capacitor voltages of the remaining n-2 sub-modules of the arm is processed according to Eq. (17).

The next step is to sort the capacitor voltages of the n-2 sub-modules after processing. Then n-2 sub-modules along with the $u_{c_{max}}$ sub-module and $u_{c_{min}}$ sub-module are carried out according to the steps (3) of the 3.1 section described above. In this way, the sub-modules can increase the ability to maintain the current state. Not only the switching frequency of the devices is reduced, but also the capacitor voltage equalizing performance of the sub-modules is not decreased.

4. Simulation verification

To verify the correctness of the proposed MPC strategy, the simulation model is built with MATLAB software. The system simulation parameters are as follows. The system voltage is 6kV, the rated DC voltage is 8kV, the number of sub-modules of the arm is 4, the rated capacitor voltage of the sub-module is 2kV, the capacitor of sub-module is $9000 \mu F$, the inductance of arm is 68mH, and the allowable value of capacitor voltage deviation among sub-modules is $\Delta u_{cM}=0.04$ kV.

Figure 3 shows the output three-phase AC current for MMC. It can be seen that the proposed strategy can realize the tracking of the current well. The current waveforms not only contain lower harmonic components, but also achieve good amplitude and phase.
Figure 4 shows the current waveform and circulating current waveform of upper arm for the proposed MPC strategy. We can make out that the current waveform of the arm tends to be sinusoidal, and the 2nd, 4th harmonic components in the circulating current are well suppressed.

Figure 4. Waveform comparison of upper arm current and circulating current

Figure 5 and 6 present the comparison of sub-module capacitor voltages and sub-module trigger pulses for conventional MPC strategy and improved MPC strategy. For the improved MPC strategy, weight factors are chosen to be $\lambda_1=8$ and $\lambda_2=0.1$.

Figure 5. Capacitance voltage waveform

We can see that that capacitor voltages of sub-modules can be well balanced and have a common trend for the traditional MPC strategy. However, the working state of sub-modules change frequently and the switching frequency is also higher. For the improved MPC strategy, the difference among the capacitance voltages of the sub-modules is increased; the fluctuations of capacitor voltages deviation from rated value of sub-modules also increase. But the switching frequency of IGBT is obviously decreased, the fluctuation range is still within the allowable range and the maximum difference in capacitor voltages among sub-modules is also within the allowable value of 0.04 kV.

5. Conclusion
An improved MPC strategy is proposed to realize the control of MMC AC current, the stability of capacitor voltage and the suppression of circulating current. The strategy reduces the computation by combining capacitive voltage sorting method to find the optimal switching sequence of the next cycle. It lowers the switching frequency of the devices by introducing the weighting factors and lessens the
deviation among the capacitor voltages of the sub-modules by giving the allowable voltage deviation of the capacitor voltage. Simulation results verify the feasibility of the proposed strategy.

6. References
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