PLL-based nanoresonator driving IC with automatic parasitic capacitance cancellation and automatic gain control

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Abstract
This paper presents a phase-locked loop (PLL) based resonator driving integrated circuit (IC) with automatic parasitic capacitance cancellation and automatic gain control. The PLL consisting of a phase frequency detector (PFD), a loop filter, and a voltage-controlled oscillator (VCO) makes the driving frequency to be locked at the resonant frequency. The resonator is modeled by Butterworth–Van Dyke equivalent circuit model with motional resistance of 72.8 kΩ, capacitance of 6.19 fF, inductance of 79.4 mH, and parasitic parallel capacitance of 2.59 pF. To mitigate the magnitude and phase distortion in the resonator frequency response, it is necessary to compensate for the parasitic capacitance. The proposed automatic parasitic capacitance cancellation loop is operated in the open-loop mode. In the automatic parasitic capacitance cancellation phase, the outputs of the transimpedance amplifier (TIA) at the lower and higher frequency than the resonant frequency (VH and VL), are compared, and the programmable compensation capacitor array matches the VH and VL using binary-searched algorithm to cancel the parallel parasitic capacitance. The automatic gain control (AGC) loop keeps the oscillation at the suitable amplitude, and the AGC output can be used as a measurement of the motional resistance. The AGC loop is also digitally controlled. The proposed resonator driving IC is designed in a 0.18-μm bipolar complementary metal oxide semiconductor double-diffused metal oxide semiconductor (BCDMOS) process with an active area of 3.2 mm². The simulated phase noise is −61.1 dBc/Hz at 1 kHz and the quality factor (Q-factor) is 59,590.

Keywords
Phase-locked loop, automatic parasitic capacitance cancellation, automatic gain control, Butterworth-Van Dyke equivalent circuit model, motional series resonant frequency

Introduction
As the development of internet of things (IoT) technologies, various sensor markets are continuously growing. Recently, nanotechnology-based nanoresonator sensor is of interests to expected to have various sensor applications with the growth of the nano/microelectromechanical system (NEMS/MEMS) sensor market. By the motional resistance or motional inductance detection method of a nanoresonator, it can be used for measuring physical properties of liquid, such as density or viscosity,¹ ² ³ and it can be applied as bio sensors or chemical sensors that measure the blood glucose, and so on.

There are two main categories for the resonator driving system: open-loop system and closed-loop system. In open-loop system, resonant frequency and quality factor (Q-factor) can be obtained with the full frequency curve of a nanoresonator,⁷ but the additional input driving source with frequency sweeps near resonant frequency is required. In the case of high Q-factor of resonator, the sweep size of the input frequency should be fine. With unknown resonant frequency, it can be difficult to find the resonant frequency
depending on the frequency sweep range and size. Also, there are limitations in obtaining the continuous changes in Q-factor or resonant frequency. In closed-loop system, self-sustained oscillator\textsuperscript{4,11} circuit and phase-locked loop (PLL) architecture\textsuperscript{4,12} are mainly used. Compared to the oscillator circuit, PLL architecture has better adaptability to resonators and better performance with large damped resonators.\textsuperscript{1}

This paper presents PLL-based nanoresonator driving integrated circuit (IC) with automatic parasitic capacitance cancellation and automatic gain control. The nanoresonator was modeled by Butterworth-Van Dyke equivalent circuit model\textsuperscript{13–17} with motional series branch (resistance, inductance, and capacitance) and parallel parasitic capacitance. The purpose of the proposed nanoresonator driving IC is detection of the motional resistance, which is damping parameter of the mechanical lumped-parameter model. The nanoresonator model used in the proposed circuit has the motional series resonant frequency of 7.16 MHz, and the parallel capacitance of 2.59 pF. As the parasitic capacitance cause magnitude and phase distortions of frequency response and affect the resonant characteristic, the influence of the parasitic capacitance should be minimized. In this paper, a new method for the parasitic compensation is presented for the parasitic capacitance compensation. The automatic parasitic capacitance cancellation loop of the proposed nanoresonator driving IC automatically matches the programmable compensation capacitor array to the parasitic capacitance by using binary-searched algorithm, and compensate the parasitic capacitance properly.

PLL consists of phase frequency detector (PFD), loop filter, and voltage-controlled oscillator (VCO). PLL tracks the resonant frequency of the nanoresonator and keeps the oscillation frequency at the resonant frequency. The path through the AGC amplifier $A_3$, resistor $R_{REF}$ and $A_4$, which is the replica path with the path through the AGC amplifier $A_1$, nanoresonator and TIA compensate the phase delay because of the AGC amplifier, nanoresonator, and TIA.

The automatic gain control loop (AGC)$^{11,18}$ keeps the oscillation amplitude properly, by automatically tracking the set reference voltage $V_{AGC}$. As the motional resistance can be obtained digitally by the AGC loop operation, the proposed circuit does not require an additional analog-to-digital converter (ADC).

The remainder of this paper is organized as follows. Section “Circuit implementation” describes the overall structure and compositions of the proposed scheme. Section “Circuit operation” describes the detailed operation principle of each mode (automatic parasitic capacitance cancellation loop, PLL, and AGC loop) of the proposed scheme. Section “Experimental results” shows the operation verification of the implemented circuit. The end of the paper concludes the proposed PLL-based nanoresonator driving IC.

### Circuit implementation

Figure 1 shows the top architecture of the proposed PLL-based nanoresonator driving IC with automatic parasitic capacitance cancellation and AGC. The automatic parasitic capacitance cancellation loop mode and the AGC loop mode can be selected by switching operation. Before the operation of PLL and the AGC loop, the automatic parasitic capacitance cancellation loop is activated first to compensate the parasitic parallel capacitance of a nanoresonator.

The automatic parasitic capacitance cancellation loop consists of 10-bit programmable compensation capacitors array $C_{comp}$, buffer $A_{P1}$, unity gain inverting amplifier $A_{P2}$, TIA, peak detector, sampling capacitors $C_H$ and $C_L$, comparator $COMP_{APC}$, and successive approximation register (SAR) logic. In the parasitic capacitance cancellation loop phase, a higher frequency and a lower frequency compared with the resonant frequency is implied to the input terminal $F_{inH}$ and $F_{inL}$, respectively. By the sequential operation of two switches $F_{inH}$ and $F_{inL}$, the circuit is driven in higher frequency and lower frequency sequentially. In the parasitic capacitance cancellation phase, $R_{AGC}$ and the gain of the AGC amplifiers ($A_1$, $A_2$, and $A_3$) has a static value.

PLL consists of PFD, VCO, and loop filter. The phase of TIA output and VCO output are compared by two comparators $COMP_{PLL1}$ and $COMP_{PLL2}$, and PFD output that proportional to the phase difference controls VCO. The PFD output voltage is applied to the VCO and keeps the VCO output frequency at the resonant frequency. The AGC loop consists of 9-bit programmable resistor array $R_{AGC}$, AGC amplifier, TIA, peak detector, comparator $COMP_{AGC}$, and SAR logic register. The DC voltage input terminal $V_{AGC}$ at the comparator $COMP_{AGC}$ is the reference voltage that is compared with the peak voltage of the TIA output. The reference voltage $V_{AGC}$ can be arbitrarily set to a desired oscillation amplitude.

The nanoresonator model used in the proposed IC is shown in Figure 2. The nanoresonator was modeled by Butterworth-Van Dyke equivalent circuit model with the motional series resonant frequency of 7.16 MHz (the motional resistance of 72.8 k$\Omega$, the motional inductance of 79.4 mH, the motional capacitance of 6.19 fF, and the parasitic parallel capacitance $C_p$ of 2.59 pF).

Figure 3 shows the charge pump PFD (CPPFD)$^{19}$ implemented in the proposed IC. The CPPFD is implemented with two D flip-flops, source current $I_{SRC}$, and sink current $I_{SNK}$. $I_{SRC}$ and $I_{SNK}$ which has the current value of 12 $\mu$A in the proposed circuit force the current into or out the loop filter. The loop filter is implemented with second-order passive loop filter with $R_{LF}$ of 600 $\Omega$, $C_{LF}$ of 80 pF, and $C_F$ of 8 pF. The CPPFD compares the phase of VCO output and of TIA output, and locks the oscillation frequency at the resonant frequency of the nanoresonator. To avoid a dead zone
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region of the CPPFD, reset input is delayed using two inverter cells.

Figure 4 shows the schematic of operational amplifier (op-amp) used in TIA, AGC amplifier, and peak detector. The op-amp is implemented with rail-to-rail folded cascode architecture and Monticelli’s class-AB output stage. For the wide input range, M1–M4 forms rail-to-rail input stage. M9–M12, M17, and M18 constitute Monticelli’s class-AB output stage to achieve power efficiency. $C_{m1}$ and $C_{m2}$ is used to nested-Miller
compensation capacitor to secure frequency response stability.

**Circuit operation**

**Automatic parasitic capacitance cancellation loop**

In the Butterworth-Van Dyke equivalent circuit model, the MSRF $\omega_{rs}$ of the nanoresonator that parasitic capacitance $C_p$ is ignored is expressed as:

$$\omega_{rs} = \frac{1}{\sqrt{L_m C_m}}$$  \hspace{1cm} (1)

In the case of $C_p >> C_m$, the parallel resonant frequency $\omega_{rp}$ that $C_p$ is considered can be expressed as:

$$\omega_{rp} = \omega_{rs} \sqrt{1 + \frac{C_m}{C_p}}$$  \hspace{1cm} (2)

The equations (1) and (2) indicate that parasitic capacitance affect the frequency response of the resonator, and it should be compensated properly.

As shown in Figure 5, if the parasitic capacitance $C_p$ is not compensated, the resonator no more has a band-pass filter characteristic having an accurate resonant frequency, and the gain continuously increases or decreases with the variation of frequency. By taking advantage of this these characteristics, the automatic parasitic capacitance cancellation loop operates by the method of comparing the output voltage by sequentially applying a low-frequency signal input and a high-frequency signal input compared to the resonant frequency of $F$. After the parasitic capacitance is compensated by $C_{comp}$ to the parasitic capacitance $C_p$, before compensation, the initial frequency characteristic of the nanoresonator is shown as in Figure 5. As the automatic parasitic capacitance cancellation loop operates, the output at the frequency of $F_{inh}$ and $F_{inl}$ is compared and $C_{comp}$ is adjusted using SAR control. In this process, over compensation and under compensation of $C_p$ is repeated, tracking the point where the gain at the frequency of $F_{inh}$ and $F_{inl}$ are same, that is, the point where $C_{comp}$ is matched to $C_p$.

**PLL and Automatic gain control loop**

After the parasitic capacitance is compensated by the operation of the automatic capacitance cancellation loop, PLL, and AGC loop mode are activated. Figure 9 shows the connection status of PLL and AGC loop mode. The current output of the nanoresonator driven by VCO output is converted to voltage and amplified by TIA and the peak voltage of TIA output is compared to set reference voltage $V_{AGC}$. The comparator COMP$_{AGC}$ compares the peak voltage of TIA output and $V_{AGC}$, and 9-bit programmable resistor array $R_{AGC}$ is controlled by the method of binary-searched algorithm using 9-bit SAR logic register. As $R_{AGC}$ is controlled, the gain of the circuit is controlled and the peak voltage of the TIA output automatically tracks the reference voltage $V_{AGC}$.

The motional capacitance $C_m$ and the motional inductance $L_m$ of the nanoresonator driven in resonant frequency are canceled each other out and if the parasitic capacitance $C_p$ is compensated properly, the TIA output can be expressed as:
The motional resistance $R_m$ can be expressed as:

$$R_m = R_{AGC} \cdot \frac{R_{TIA}}{R_2} \cdot \frac{V_{IN}}{V_{O,TIA}}$$

Assuming the nanoresonator as a narrow-band mechanical bandpass filter, the fundamental frequency of $V_{in}$ is the natural frequency of the nanoresonator. The $C_F$ is about ten times smaller than $C_{LF}$, the open-loop gain of the PLL can be approximated as:

$$G(s) \approx \frac{1}{2\pi} \cdot I_{CP} \cdot K_{VCO} \cdot \frac{sRC + 1}{s^2C_1}$$

Where $I_{CP}$ is the charge pump current and $K_{VCO}$ is the voltage-to-frequency conversion coefficient of the
Figure 8. Conceptual frequency response of the nanoresonator during the automatic parasitic capacitance cancellation loop operation.

Figure 9. Circuit connection status of automatic gain control loop operation.
VCO. Thus, the simplified closed-loop transfer function can be expressed as:

\[
H(s) = \frac{I_{CP}}{s^2 + \frac{I_{CP}}{2\pi C_p} K_{VCO} \cdot R_L + \frac{I_{CP}}{2\pi C_L} \cdot K_{VCO}} (6)
\]

**Experimental results**

Figure 10 shows the layout of the proposed PLL-based nanoresonator driving IC with automatic parasitic cancellation and automatic gain control. The proposed IC is designed with a 0.18-μm bipolar complementary metal oxide semiconductor double-diffused metal oxide semiconductor (BCDMOS) process with an active area of 3.2 mm\(^2\).

The op-amp shown in Figure 4 is implemented with unit gain bandwidth (UGBW) of hundreds of megahertz to drive the nanoresonator model with the resonant frequency of 7.16 MHz. Figure 11 shows the loop gain simulation results of the op-amp. The op-amp has DC gain of 82.2 dB, and UGBW of 260 MHz, which is sufficient to drive the nanoresonator with 7.16 MHz of resonant frequency. The op-amp has the phase margin of 50° and secures the frequency stability.

Figure 12 shows the simulation result of the automatic parasitic capacitance cancellation loop. The 10-bit programmable compensation capacitor array \(C_{\text{comp}}\) implemented with the unit capacitance of 33.4 fF matches the 2.59 pF of the parasitic capacitance \(C_p\) of the nanoresonator at digital register input of 76 or 77 in decimal. The SAR logic digital output controls the compensation capacitor array \(C_{\text{comp}}\), comparing the output at the frequency of \(F_{\text{inH}}\) and \(F_{\text{inL}}\), as shown in Figure 8. The simulated SAR logic register digital output is 76 and the parasitic capacitance is compensated properly.

Figure 13(a) shows the time domain simulation result of AGC loop when the motional resistance \(R_m\) is 10 kΩ, and the reference voltage \(V_{\text{AGC}}\) is 1.2 V. The oscillation frequency is locked at 7.16 MHz, which is close to the resonant frequency of the nanoresonator. The peak detector output of the black line automatically tracks the reference voltage \(V_{\text{AGC}}\). Figure 13(b) shows the digital output of the AGC loop under the same condition and the simulated digital output is 13 in decimal.

Figure 14 shows the motional resistance \(R_m\) detection simulation. Digital output of the AGC loop is simulated under the variation of the motional resistance \(R_m\) from 10 to 100 kΩ with intervals of 10 kΩ. The
A nanoresonator is shown in Table 1. As the parallel parasitic capacitance compensation loop automatically tracks and automatically compensating for the parasitic capacitance is proposed.

**Table 1.** Performance summary of the proposed PLL-based nanoresonator driving IC and comparison with other studies.

| Method              | Technology (µm) | Frequency (MHz) | Q-factor | Phase noise at 1 kHz (dBc/Hz) | Parasitic cancellation |
|---------------------|-----------------|-----------------|----------|-------------------------------|------------------------|
| This work           | 0.13            | 7.16            | 59,590   | −61.1                         | Yes                    |
| Seth et al.⁹        | 0.18            | 20              | 160,000  | −131                          | No                     |
| Nabki and El-Gamal¹⁰| 0.18            | 8.29            | 1,040    | −89                           | No                     |
| Wojciechowski et al.²²| 0.35            | 101.7           | 3,100    | −90.6                         | No                     |
| Johnston et al.²¹   | 0.18            | 864             | 1257     | −68                           | No                     |

Figure 14. Motional resistance $R_m$ detection simulation result.

Figure 15. FFT simulation result of the proposed PLL-based nanoresonator driving IC.

**Conclusion**

As nanotechnology-based sensor is expected to have various sensor application, nanoresonator can be applied as a bio/chemical sensor by the method of detecting the motional inductance or the motional resistance. This paper presents PLL-based nanoresonator driving IC with automatic parasitic capacitance cancellation and automatic gain control. The purpose of the proposed IC is to detect the motional resistance of a nanoresonator. To compensate the phase or the magnitude distortion of the frequency response, the parallel parasitic capacitance of the nanoresonator should be compensated. The automatic parasitic...
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