Single-Stage Injection-locked Frequency Sixtupler in CMOS Process

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ABSTRACT High multiplication-factor even-modulus frequency multipliers are often configured as multi series frequency multipliers. This paper designs a single-stage LC-tank injection locked frequency sixtupler (ILFS) fabricated in 0.18 μm CMOS process and the ILFS merges many sub-circuits in one by sharing a common supply and passive inductive elements. The circuit design, operation principle and measurement results of the ILFS are addressed. The differential input and single-phase output ILFS circuit is made of two frequency doublers, a first-harmonic injection-locked oscillator and an active frequency tripler using one frequency doubler. The free-running frequency of the ILO is around 5.716 GHz. At the dc power consumption of 20.9 mW and at the incident power of 0 dBm, the ×6 input locking range is from the incident frequency 0.94 GHz to 1.02 GHz to provide an output signal source from the frequency 5.64 GHz to 6.12 GHz. The whole chip occupies a die area of 1.141×1.2 mm². Other high multiplier factors are also measured on the designed chip.

INDEX TERMS frequency doubler, frequency tripler, injection-locked frequency sixtupler, locking range, phase noise.

I. INTRODUCTION

Frequency multipliers (FMs) are often used in wireless transceivers or radar systems, converting a low frequency signal into a high frequency signal. LC-type frequency multipliers have been formed in active frequency multipliers with filters, multiple-push harmonic voltage-controlled oscillators or injection-locked frequency multipliers (ILFMs). High-even multiplier factor frequency multipliers may consist of two frequency multipliers as well as amplifiers. Times six multipliers are probably made up of a frequency tripler (FT), a buffer amplifier, and a frequency doubler. The active frequency sixtupler [1]-[5] comprises of a first frequency tripler, a buffer amplifier, a second frequency doubler and an output power amplifier. A frequency tripler may use the concept of nonlinear amplifier or mixing first and second harmonics to generate third harmonic [6]. An integrated frequency sixtupler [7] can be composed of a non-linear differential amplifier used as a frequency tripler followed by a Gilbert mixer used as a frequency doubler. The 2nd sixtupler design approach [8] uses a two-stage approach. The first stage is an even-order harmonics generator and the second stage mixes the 2nd and the 4th harmonics, to generate the desired 6th harmonic. A CMOS frequency sixtupler chain [9] uses a frequency tripler in front of a frequency doubler in the transmitter.

A CMOS two-stage injection-locked frequency sixtupler (ILFS) [10], [11] as shown in Fig. 1(a) uses a single-FET frequency tripler in front of an injection-locked oscillator (ILO) as a push-push frequency doubler, the FT FET biased at the pinch-off voltage uses filters as the load, this filter approach is a narrow-band approach, otherwise harmonics are injected to the ILO. The property of this sixtupler such as phase noise is not characterized. The 6th harmonic signal is obtained from the ILO common inductor node based on the push-push technique, it suffers from low output voltage amplitude [11]. Fig. 1(a) and Fig. 1(b) show two block diagrams of conventional two-stage ×6 ILFS. A ×6 ILFS as shown in Fig. 1(a) can be configured as an active frequency tripler and an injection-locked frequency doubler. Combining an independent frequency doubler and an ILO forms an injection-locked frequency doubler with large output signal. The ×6 ILFS in Fig. 1(b) is formed using an injection-locked frequency tripler (ILFT) and a frequency...
doubler [12], [13]. Combining an active frequency tripler and an ILO forms an injection-locked frequency tripler. On the other hand, the order of two sub-circuits in Fig. 1(a) and Fig. 1(b) can be rearranged. Fig. 1(c) shows a sixtupler [14] by interchanging the order of two sub-circuits in Fig. 1(b). Active frequency multipliers in Fig. 1(a) ~ Fig. 1(c) can be replaced by \( \times n \) ILO to form frequency sixtupler circuits. Rigorously speaking, the previous circuits fall in the categories of active frequency multipliers and \( \times 2, \times 3 \) ILFs. A PLL with a \( \times 6 \) FM [15] is used to boost the frequency of output signal and Fig. 1(d) shows a PLL with a \( \times 6 \) ILFM to increase the frequency of output signal. A \( \times 6 \) ILFM can be formed with an active \( \times 6 \) FM, followed by a balun and an ILO to boost the output signal strength. The output locking range is limited by the output signal strength of the \( \times 6 \) FM.

This paper proposes a new single-stage injection-locked frequency sixtupler, which combines an injection-locked frequency doubler and an injection-locked frequency tripler in one, both sub-circuits share the same injection-locked oscillator (ILO). As compared to the frequency multiplier chains, the single-stage ILFS approach simplifies circuit design because of reduced circuit component numbers and no frequency misalignment between \( \times 3 \) FM and \( \times 2 \) FM stages. Secondly, it has large conversion gain at low injection power. By using a new balanced frequency doubler, large \( \times 6 \) output amplitude is obtained enabling driving a next stage.

II. CIRCUIT DESIGN

The ILFS can be arranged in two ways. The first one uses a balun before frequency doubler, a balun after the doubler and an IFT, and the second one uses a balun before a frequency tripler, an IFT and a frequency doubler. Since the latter can merge the IFT and the doubler in one circuit, it is the simpler ILFS structure used in this study. Fig. 2(a) shows the proposed single-stage sixtupler consisting of an \( LC \) resonator, a negative resistance circuit \( R_{OSC}=2/g_m, g_m : \) transconductance of \( M_1 \), a frequency tripler and a frequency doubler. \( M_1, M_2, C_1, C_2, R_3, \) and \( R_4 \) act as a negative resistance generator, which forms an oscillator with the resonator composed of \( L_1, L_2, L_3 \) and a parasitic capacitor \( C_T \).

**FIGURE 1.** Block-diagrams of the injection-locked frequency sixtupler and a PLL.

**FIGURE 2.** (a) Block-diagram of an injection-locked frequency sixtupler. \( L_{BS}, L_{DS} \): bonding wires. \( C_T \) is the parasitic capacitor. (b) & (c) Block-diagram of two reference injection-locked frequency sixtuplers.
The size and bias of $M_1$ affect the value of $R_{\text{OSC}}$. A frequency tripler (FT) can be constructed by an isolated frequency doubler followed by a mixer [16]. Here, $L_6$, $M_3$, and $M_4$ construct a mixer-based frequency tripler [17], they act concurrently as a frequency doubler and a frequency tripler. A differential injection signal is applied to the gates of $M_3$ and $M_4$, even-order ($2^{\text{nd}}$ & $4^{\text{th}}$) harmonics existing in the FET currents are added in phase at the common FET source and the odd-order harmonics are suppressed due to $180^\circ$ phase difference. Thus the common node $V_{L6}$ of $L_6$, $M_3$, and $M_4$ generates a $2^{\text{nd}}/4^{\text{th}}$ harmonic of injection signal and the drains of $M_3$ and $M_4$ as mixers contain a $3^{\text{rd}}$ harmonic of injection signal by mixing the even-harmonic source signal and the gate input signal.

The multiplier-by-3 (FT) input/output frequency relation of the injection mixer [11] is given by $\omega_{\text{FT}} = 2\omega_{\text{inj}} = \omega_{\text{inj}}$, where $\omega_{\text{inj}}$ is the frequency of injection source/FT output. Alternatively, an additional FT input/output frequency relation of the injection mixer is given by $4\omega_{\text{RF}} = \omega_{\text{inj}}$, where $\omega_{\text{RF}}$ is self-generated at the common node of $L_6$, $M_3$, and $M_4$. The oscillator and the FT form an injection-locked frequency sixtupler [11] uses the architecture shown in Fig. 1(a) with an FT, buffers and injection locked frequency doubler, this circuit doesn’t use the injection self-induced harmonic to enhance the locking range because the buffers block the feedback signal to the pregenerator. In the two-stage ILFS [11], the FT output frequency must falls in the input locking range of ILO, the load filter of the FT and the load tank of the push-push doubler are concurrently designed to ensure wide locking range. The designed single-stage ILFS uses one ILO and one active frequency doubler, no frequency alignment problem is encountered, because the doubler always tracks the output frequency of the ILFT. $M_5$ and $M_6$ form a new balanced frequency doubler by taking the inputs from the ILO outputs via dc blocking capacitors $C_3$ and $C_4$, and the common source of $M_5$ and $M_6$ outputs a $6^{\text{th}}$ harmonic of injection signal. $R_3$, and $R_6$ are biasing resistors and $V_{B1}$ is the gate bias. $M_5$, $R_7$ and $C_3$ form an output buffer for the sixth harmonic extraction. In Fig. 2(a) $C_P$ is the parasitic capacitor due to the source-body diodes of $M_5$ and $M_6$. The new frequency doubler consumes no dc power and doesn’t increase the voltage headroom.

![FIGURE 3](image-url) (a) Simulated voltage waveforms of ILFS. Black dotted: input. Blue dotted: common drain of $M_1$ and $M_2$. Green dashed-dotted: drain of $M_2$. Red solid: drain of $M_1$. (b) Simulated current and voltage waveforms of ILFS. Black dashed: drain current of $M_1$. Blue dashed: drain current of $M_2$. Red solid: common voltage source of $M_1$ and $M_2$. Green dashed-dotted: gate voltage of $M_5$. Orange dashed-dotted: source voltage of $M_5$. $V_{DD} = 1.1$ V, $V_{DD} = 0.85$ V, $V_{DD} = 0.0$ V, $V_{DD} = 1.6$ V, $V_{DD} = 1.7$ V, $V_{DD} = 0.85$ V, $f_{INJ} = 1.2$ GHz, $V_{INJ} = 0.85$ V, $V_{INJ} = 0.0$ V, $V_{INJ} = 0.0$ V, $V_{INJ} = 1.6$ V, $V_{INJ} = 1.7$ V, $V_{INJ} = 0.85$ V. Green circle (right vertical axis): free-run output frequency. Red & black symbols (left axis): output locking range.

![FIGURE 4](image-url) (a) Simplified circuit of the LC ILO. Dashed box representing the RLC resonator. Ignoring $L_5$, $L_6$ for simplicity. (b) Pre-layout simulated ×6 output locking range versus channel width of $M_5$ ($M_6$). $V_{DD} = 0.9$ V, $V_{DD} = 0.85$ V, $V_{DD} = 0.0$ V, $V_{DD} = 1.6$ V, $V_{DD} = 1.7$ V, $V_{DD} = 0.85$ V. Green circle (right vertical axis): free-run output frequency. Red & black symbols (left axis): output locking range.
show two reference ×6 ILFMs adapted from Fig. 2(a) by reconfiguring the frequency doubler. Both circuits tap the voltage \( V_s \) as the output signal. The 1st one in Fig. 2(b) normally has smaller voltage swing and it relies on the resonator connected to the \( V_s \) node, and \( M_1 \) and \( M_2 \) supplies the 6th harmonic current to generate the desired sixtupler output signal. The 2nd one in Fig. 2(c) increases the voltage headroom caused by the current reused frequency doubler FETs \( M_5 \) and \( M_6 \) with biased gates. This frequency doubler accepts ILO output voltage to generate the 6th harmonic current by biasing \( M_5 \) and \( M_6 \) in the class C mode. Fig. 2(a)-Fig. 2(c) use different push-push techniques to build the frequency doubler.

Fig. 3(a) shows simulated voltage waveforms of injection-locked frequency sixtupler and it explains that the circuit contains the fundamental, second harmonic, third and sixth harmonics. The input signal is at \( \omega_o \), the self-induced signal of \( M_5 \) source is at 2\( \omega_o \), the self-induced signal of \( M_5 \) drain is at 3\( \omega_o \), and the self-induced output signal of \( M_6 \) drain is at 6\( \omega_o \). The ILO push-push node \( V_o(L) \) also contains a 6th harmonic which is much smaller in amplitude than the sixth harmonic at the common node of \( M_5 \) and \( M_6 \). Fig. 3(b) shows simulated current and voltage waveforms to explain the operation function of the balanced frequency doubler. The gate terminal of one transistor is connected with current reused frequency doubler FETs \( M_5 \) and \( M_6 \) with biased gates. This frequency doubler accepts ILO output voltage to generate the 6th harmonic current by biasing dynamically \( M_5 \) and \( M_6 \) in the class AB mode. According to Fig. 3 at \( V_{DD}=1.1 \) V, and \( V_{BI}=1.7 \) V, \( M_5 \) and \( M_6 \) is dc-biased in the linear mode. The drain current of each transistor from the common node \( M_5 \) and \( M_6 \) to the supply node shows one peak for each period while the ILO output voltage shows one voltage peak and the frequency doubler pair \( M_5 \) and \( M_6 \) provides an output voltage with two peaks. In Fig. 2(a), the gate voltage of \( M_5 \) can be described by \( V_{BI}+A\cos(3\omega_o t) \), where \( A \) is the voltage amplitude and the source voltage of \( M_5 \) is given by \( V_{DD} - A\cos(3\omega_o t) \). When the dynamic gate-source voltage \( V_{GS} \) is above the threshold voltage \( V_{TH} \), and when the drain voltage of \( M_5 \) is low, \( M_5 \) is on and \( C_P \) dumps the charges on \( C_P \) and \( V_{DD} \) goes down. When the drain voltage of \( M_5 \) is higher than \( V_{DD} \), \( C_P \) sinks the charges from...
the supply and \( V_{S6} \) goes up. Gate-source voltage of \( M_5 \) and \( M_6 \) is enough to turn on the FETs so the FETs operates in the class AB mode and dynamic drain-source voltage of \( M_5 \) and \( M_6 \) plus the gate-source voltage generates the 6th drain harmonic voltage. Increasing \( C_P \) reduces the voltage swing of \( V_{S6} \). The 3\( \omega_o \) source currents of \( M_5 \) and \( M_6 \) flow alternatively to the common node parasitic capacitor \( C_P \) of \( M_5 \) and \( M_6 \) create a 6\( \omega_o \) harmonic voltage. The common source of \( M_5 \) and \( M_6 \) is a virtual ground for the 3\( \omega_o \) harmonics. According to the simulation, the 6th harmonic voltage \( V_{S6} \) is significantly larger than \( V_{S6} \) and \( V_{D6} \), this is a merit of the proposed circuit to be used as a frequency sixtupler. According to the simulation under the bias condition as Fig. 3(b) when the load at \( V_{O3} \) varies from 50 \( \Omega \) to 250 \( \Omega \), the free-running oscillation frequency \( f_{oscS6} \) in the ILFS output is almost unchanged, because the node \( V_{S6} \) is a virtual ground. When the operating temperature varies from -20°C to 50°C, the free-running \( f_{oscS6} \) in the ILFS output varies from 6.94GHz to 6.96 GHz. The free-running ILFS is robust to ambient variation.

The locking range of a parallel RLC-tank ILO as shown in Fig. 4(a) around a resonant frequency is derived as \[18\]:

\[
\Delta \omega_{RFIL} = (3 \omega_{RF} - 3 \omega_o) = \frac{3 \omega_o I_{inj}}{2Q_{es}}.
\]

The fundamental current \( I_{inj} \) to the \( LC \) tank is from injection mixer, and the fundamental oscillation current \( I_{osc} \) comes from the switching FET to the tank. The locking range is given by \( 2 \Delta \omega_{RFIL} \). In Fig. 4(a) \( R/C \) represents the equivalent resistance/capacitance due to the frequency doubler and injection FETs. The output phase noise of ILFT can be modified as \[19\]:

\[
S_{\omega,o} = \frac{(3^2) S_{\omega,RFil}}{1 + (\omega_m / \omega_o)^2} + \frac{(\omega_m / \omega_o)^2}{1 + (\omega_m / \omega_o)^2} S_{\omega,ILFT}
\]

(2)

where \( \omega_m \) is the offset frequency and \( \omega_o \) is a parameter of injection source and the ILFT circuit. \( S_{\omega,RFil} \) and \( S_{\omega,ILFT} \) are respectively the phase noise of the injection source and the equivalent output noise due to the free-running ILFT. The output phase noise of an ILFS due to two independent noise sources is as follows:

\[
S_{FSO} = (2^2) \cdot S_{\omega,o}
\]

(3)

Suppose the ac drain-body and gate-body voltages of injection FET are respectively given by

\[
v_d = v_{dc} \cos(3\omega_o t + 3\phi) + v_{df} = v_{RF} \cos(\omega_{RF} t + \theta)
\]

(4)

where \( v_{dc}/V_{RF} \) is the amplitude of the drain/gate voltage component, \( 3\phi \) and \( \theta \) are phases. The drain current is given by

\[
i_d = g_m v_d v_{gs} + v_{ds} \cos(3\omega_o t + 3\phi) \cos(\omega_{RF} t + \theta)
\]

(5)

\( V_L \) is the multiplication of the drain current (5) and the impedance associated with \( L_c \). \( g_m \) is the drain current expansion coefficient. Under the injection-locked condition, \( \omega_{RF} = \omega_o \), \( V_L \) contains the signals at \( 4\omega_o \) and \( 2\omega_o \), which mix...
with the injection voltage to generate the 3rd harmonic injection current. The turn-on of cross-coupled FETs $M_1, M_2$ increase the drain voltage swing of $M_1, M_2$, so that the voltage swing of even-harmonic $V_{IL}$ increase, and the self-induced harmonic increases the locking range. The size of $M_3$ and $M_6$ and gate bias $V_{BI}$ are used to optimize the circuit performance. At $V_{DD} = 0.9$ V and $V_{BI} = 1.7$ V, the free-run ILO oscillation frequency is 3.47 GHz. The simulated output locking range at 0 dBm input power is from 6.6 GHz to 7.62 GHz as shown in Fig. 4(b). $M_3$ and $M_6$ can be modeled as a channel resistor in shunt with parasitic capacitor. Decreasing the channel width of $M_5$ and $M_6$ increases the channel resistance and reduces the parasitic capacitance, this increases the free-run ILO oscillation frequency as shown in Fig. 4(b) and increases the output ILO strength and the locking range decreases because of increasing resonator Q-factor. As $V_{BI}$ decreases from 1.7 V, the ILO voltage swing increases but the ×6 output power strength decreases and the locking range decreases too. If the channel width of $M_5$ and $M_6$ and gate bias $V_{BI}$ are too large, the ILO can’t oscillate, because the ILO outputs are shorted. Simulation shows the gate bias $V_{IN}$ of $M_3$ and $M_4$ increases from 0.4 V to 0.85 V, the locking range increases and the power consumption increases too.

### III. MEASUREMENT RESULTS

The ×6 ILFM has been designed and fabricated in the TSMC 0.18 μm 1P6M CMOS technology. The die micrograph occupying an area of 1.141×1.2 mm$^2$ is shown in Fig. 5. The three left-hand side inductive passives are for the frequency tripler, while the right-hand side inductive passives are for the ILO. Die measurement was carried on PCB using Agilent signal generator NS183A, KRYTAR’s 3 dB 180 Degree Hybrid and Agilent spectrum analyzer E4407B. Fig. 6(a) shows measured free-run spectrum of ILO buffer output. The carrier is at 2.88 GHz. Fig. 6(b) shows measured locked spectrum of ILO buffer output, the output contains the 1st, 2nd, 3rd and 4th harmonics. The former is the leakage caused by the layout in the PCB and IC asymmetry. The 2nd and 4th harmonics are the mixing by-products. Fig. 7(a) shows measured ×3 input sensitivity measured from ILO buffer output $V_{0+}$. At $V_{DD} = 1$ V and 0 dBm input power, the output locking range is from 2.72 GHz to 3.56 GHz. Fig. 7(b) shows measured phase noises of the locked ×3 circuit and the

| Ref | Tech. (μm) | Architecture | $P_{in}$ (dBm) | $V_{DD}$ (V) | $P_{m}$ (mW) | Die area (mm$^2$) | Lock Range (GHz)(% Or bandwidth) |
|-----|-----------|--------------|---------------|-------------|--------------|----------------|----------------------------------|
| [11] | 0.065 CMOS | ×6 ILFM | 0 | 1.0 | 6.3 | 0.51 × 0.68 | 9.6(%) |
| [8] | 0.025 InP | Mixer-FM | 7 | 1 | 20 | 0.5 | 1.5(%) BW~5dB |
| [5] | 0.025 InP | FM chain | 1.8 | 100 | 0.58 | 48(%) BW~3dB |
| This(×6) | 0.18 CMOS | ×6 ILFM | 0 | 1 | 20.8 | 1.14×1.2 | 5.62~6.23(10.29%) |
| This(×3) | 0.18 CMOS | ×3 ILFM | 0 | 1 | 22.9 | 1.14×1.2 | 2.72~3.56(26.47%) |
| This(×5) | 0.18 CMOS | ×5 ILFM | 0 | 0.9 | 17.1 | 1.14×1.2 | 2.8~3.26 (15.18%) |
| This(×10) | 0.18 CMOS | ×10 ILFM | 0 | 0.9 | 16.2 | 1.14×1.2 | 5.59~5.92 (5.73%) |
injection signal at $f_{\text{inj}} = 0.976$ GHz. The locked phase noise at 1 MHz is greater than the injection signal by 8.92 dBc/Hz at 1 MHz offset frequency. Fig. 8(a) shows measured free-run spectrum of ILFS output buffer, the carrier is at 5.75 GHz and its output power is -11.15 dBm. Other harmonics are smaller than the carrier by more than 21.46 dBm. Fig. 8(b) shows measured locked spectrum of ILFS buffer output, it contains more harmonics than those shown in Fig. 8(a) and the harmonics are caused by the leakage of injection signal and mixing products. The sixth harmonic is larger than the 1st harmonic by 17.55 dBm. Caused by the unbalanced layout, the phase difference of the ILFT inputs may not be exactly 180°, the injected fundamental is leaked to the ILFT outputs and it induces a doubler frequency signal at the ILFS output. The fundamental leakage is suppressed by the ILFT load filter, and the doubler leakage in the ILFS output is also suppressed. Fig. 9(a) shows measured ×6 input sensitivity measured from $V_{\text{INj}}$. At 0 dBm input power and $V_{\text{THI}}=1$ V, the locking range is from 5.628 GHz to 6.234 GHz. The performance improves as the supply decreases, because the locking range increases and the power reduces. Fig. 9(b) shows measured phase noise of the locked ILFS and the injection signal at $f_{\text{inj}} = 0.976$ GHz. The locked phase noise at 1 MHz is greater than the injection signal by 15.4 dBc/Hz at 1 MHz offset frequency. The ideal phase noise difference is 17.37 dBc/Hz. Fig. 10 shows measured ×6 locking range, power consumption and free-run doubler frequency versus $V_{\text{INj}}$. As $V_{\text{INj}}$ decreases, the conductance of $M_3$ and $M_4$ decreases, the power consumption decreases and the measured locking range increases.

Fig. 11(a) shows measured ×6 harmonic output power levels after calibration of the cable loss over different chip input power at the input frequency $f_{\text{inj}}$ of 1.01 GHz, the harmonic injection suppression improves as injection power increases and the ILFS operates normally irrespective of input power level. Fig. 11(b) shows the harmonics over frequency range of interest with the input power of 0 dBm. From 5.916 GHz to 6.084 GHz, the undesired harmonics are lower than the 6th harmonics by more than 10 dBm. Around 6.06 GHz, the harmonic suppression is more than 15 dBm.

The designed circuit in Fig. 2(a) can perform other frequency conversions. It can be used as a differential ×5 injection locked frequency multiplier performed by the previous ILFT except the change of the input frequency range and a single-phase ×10 injection locked frequency multiplier played by the previous ILFS. Table 1 is the measured performance summary. Measured data shows that the proposed ×6 ILFM with the new balanced frequency doubler provides undesired harmonic suppression, large output power and good phase noise performance at all measured offset frequency range.

IV. CONCLUSION

This paper presents a single-stage, compact fully integrated n-core CMOS LC-tank injection-locked frequency sixtupler that combines an injection-locked frequency tripler and a new balanced frequency doubler. The proposed ×6 circuit shows good injection-locked phase noise performance with enough locking range, good harmonic suppression from low to high input power, and large output amplitude to drive next stage, and it uses a 1st harmonic pre-generator combining a mixer and a frequency doubler/quadrupler, and a new balanced frequency doubler, the circuit can be used as an injection-locked frequency tripler too by taking the output from the ILO buffers. The circuit is also used as an injection locked ×10/×5 frequency multiplier, and further improvement can be achieved by using output filtering. The other high multiplication-factor injection-locked frequency multipliers also show good phase noise and the frequency sixtupler is extendable to a ×12 and ×18 frequency multiplier by combining with a frequency doubler and tripler respectively.

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