Zero-power calibration of photonic circuits at cryogenic temperatures

Ben M. Burridge\textsuperscript{1,2}, Gerardo E. Villarreal-Garcia\textsuperscript{1}, Antonio A. Gentile\textsuperscript{1,3}, Pisu Jiang\textsuperscript{1}, Jorge Barreto\textsuperscript{1*}

\textsuperscript{1}Quantum Engineering Technology Laboratories, University of Bristol, Bristol, United Kingdom.
\textsuperscript{2}Quantum Engineering Centre for Doctoral Training, Centre for Nanoscience & Quantum Information, University of Bristol, Bristol, United Kingdom.
\textsuperscript{3}Qu & Co BV, Amsterdam, the Netherlands.
\*Corresponding Author: g.barreto@bristol.ac.uk

Abstract

The continual success of superconducting photon-detection technologies in quantum photonics asserts cryogenic-compatible systems as a cornerstone of full quantum photonic integration. Here, we present a way to reversibly fine-tune the optical properties of individual waveguide structures through local changes to their geometry using solidified xenon. Essentially, we remove the need for additional on-chip calibration elements, effectively zeroing the power consumption tied to reconfigurable elements, with virtually no detriment to photonic device performance. We enable passive circuit tuning in pressure-controlled environments, locally manipulating the cladding thickness over portions of optical waveguides. We realize this in a cryogenic environment, through controlled deposition of xenon gas and precise tuning of its thickness using sublimation, triggered by on-chip resistive heaters. \(\pi\) phase shifts occur over a calculated length of just \(L_\pi = 12.3 \pm 0.3 \ \mu\text{m}\). This work paves the way towards the integration of compact, reconfigurable photonic circuits alongside superconducting detectors, devices, or otherwise.

1 Introduction

Photonic integrated circuits (PICs) offer a promising glimpse at the prospect of universal quantum information processing using quantum states of light \cite{1–6}. As we progress towards a fully integrated, reconfigurable quantum photonic platform, single-photon detectors must be implemented alongside existing devices to remove bottlenecks in scaling to larger circuits, minimize feed-forward associated delays, and mitigate optical coupling losses. Current best-in-class detectors, superconducting nanowire single-photon detectors (SNSPDs) \cite{7,8}, combine outstanding performance metrics in dark count rates, efficiencies, and jitter time. Furthermore, the realization of SNSPDs on integrated photonic circuits facilitates a further boost to their performance \cite{9–15}, enabling a scalable approach at the cost of low-temperature (typically below 4 kelvin) operation.

Modern reconfigurable PICs are reliant on methods of static compensation to maximize overall performance and ensure the proper functionality of PICs \cite{16}. Phase modulators, such as thermo-optic \cite{17, 18}, electro-optic \cite{19} and plasma-dispersion based devices \cite{20} are often used at ambient temperature. Historically, the basic levels of integration achieved have allowed the constraints of these particular devices to be somewhat compensated for or overlooked. Reconfigurable PICs were thus successfully used to explore and demonstrate small scale quantum experiments with high fidelity \cite{21, 23}. Although thermo-optic phase shifters (TOPS) have been successfully tested in cryogenic environments \cite{24}, power requirement concerns render them infeasible for large-scale photonic circuits within cryogenic systems. On the other hand, the use of exotic non-linear materials such as barium titanate allows for efficient high-speed electro-optic modulation at cryogenic temperatures as reported recently \cite{25}.

Here we demonstrate a method of tuning the optical properties of an individual waveguide element that breaks with convention. We facilitate the deposition of a xenon (Xe) cladding on the surface of an exposed waveguide core by controlling environmental pressure and temperature. We demonstrate this method’s functionality using a Silicon-On-Insulator (SOI) photonic circuit - containing a Mach-Zehnder Interferometer (MZI) with one of its arms exposed to our controlled environment. We take full advantage of the cryogenic conditions required for the operation of SNSPDs to dynamically and reversibly adjust the geometry of exposed sections of waveguide. We also re-purpose TOPS as on-chip temperature controllers. They function as localized and precise heat sources capable of sublimating the deposited cladding material, thus controlling the effective refractive index.

Our work expands on the ideas presented previously by \cite{26} and \cite{27}, aimed at the control of resonances in optical nano-cavities. We use localized on-chip heat delivery to address specific circuit elements and control the structural properties of individual components. Once the devices are operating as required, the waveguide components retain these characteristics as long as the environmental conditions are kept stable. As a result, cladding layer manipulation (CLM) requires no static power, releasing the entire on-chip power budget to more crucial components.
2 Theoretical Background

The power budget of a PIC is an often-overlooked parameter of current-generation photonic devices. However, modern cryostats have limited cooling powers (typically on the order of a fraction of a watt at temperatures close to 1 kelvin), which can be quickly saturated by power-hungry devices. PICs must therefore aim to function optimally in these conditions. We can separate the power consumption of integrated devices into two distinct categories based on their role within a PIC, namely controllable and configurable components. Controllable components serve to rapidly re-arrange the optical paths of a circuit into specific configurations that are, for example, capable of processing information. An example of this is re-routing a photon, based on a feed-forward signal [28]. Conversely, configurable components program and stabilize the optical path for consistent operation; with the added benefit of reconfigurability as required. Components of this kind can therefore compensate for inaccuracies in the PICs stemming from the fabrication process [29]. For example, waveguide structures such as directional couplers (DCs), and to a lesser extent multi-mode interferometers (MMIs) [30] are sensitive to fabrication tolerances [31]. These imperfections may ultimately translate to infidelities when preparing quantum states using the PIC. MZIs combine either DCs or MMIs, alongside a method of phase control, and are regarded as a tool for post-manufacture reconfiguration [14,16]. However, this comes at the cost of an increase in circuit complexity and static power consumption.

Waveguides on the SOI platform confine and guide light using the contrast between silicon’s (Si) high refractive index (3.476 at 1550 nm) that forms the waveguide core; and the lower index material of silica (SiO$_2$, 1.44 at 1550 nm) that creates the waveguide cladding. In standard waveguide geometries (500 nm x 220 nm), the optical mode is mostly present in the waveguide core, with a small fraction of evanescent mode propagating in the cladding. The cladding layer acts as a protective barrier to the waveguide core, diminishing the interaction between the externally propagating evanescent field and the environment. Consequently, the composition of these layers and their refractive index strongly affect the supported optical modes.

The effective refractive index determines how much phase an optical mode accumulates as it propagates, influenced by both the waveguide core and the cladding layer. The resultant optical path stems from the interference of all the possible optical paths. Therefore, we can alter the refractive indices of either material to control the final path of the mode. Prevalent techniques target the optical properties of the waveguide core as it carries most of the propagating mode [17,20].

The cladding material plays a comparatively minor role via the evanescent field. However, it is possible to precisely modify the effective refractive index the optical modes see by shaping the cladding layer. Under specific environmental conditions, substances can accumulate and form a film on the device surface via condensation or deposition. We can harness these phenomena by controlling the temperature, pressure, or chemical composition of the environment. For example, in a pressure-controlled chamber, a gaseous substance will condense (deposit) on a surface provided that the substance’s vapor pressure at the surface temperature is below the chamber pressure. Temperatures and pressures where this can occur are determined using the gas’ vapor pressure curve [32] (as reproduced in Fig. 1). Conversely, a solid substance at a given temperature will sublime (desorb) if its vapor pressure is higher than the pressure exerted by its environment. A chamber pressure in equilibrium with substance vapor pressure results in a balancing of condensation and sublimation rates, leading to an inherent lack of control over the deposited film.

Accurate on-chip sensing of waveguide, and specifically cladding changes induced by the presence of thin solid films is possible using an MZI [33]. Relative differences in accumulated phase; for instance due to different waveguide geometries, between the two arms of the MZI results in a significant interference pattern at the output, providing an easy map between phase and intensity. Long waveguide sections may be used as a sensor, by taking advantage of their large interaction region with the environment (Fig. 1b-c).

The free spectral range (FSR) is the wavelength separation between successive peaks (or troughs) in the transmission of an unbalanced interferometer setup. The FSR of an MZI can therefore be used to extract the difference in effective group index ($\Delta n_g$) between two equal length arms of the interferometer, using equation 1:

$$FSR = \frac{\lambda^2}{\Delta n_g L}$$

Here $\lambda$ is the central wavelength used to measure the FSR of the MZI, $L$ is the length of the exposed spiral, and $\Delta n_g$ is the change in effective group index between the exposed and fully clad waveguide arms of the MZI.

We follow the experiment by Mosor [26] and use Xe as our substance of choice. Xe is non-reactive, has a reasonably high vapor pressure at low temperatures, and a solid phase refractive index of 1.47 [34] close to that of an SiO$_2$ cladding. Temperatures lower than the deposition temperature of oxygen (O$_2$) and nitrogen (N$_2$) require higher vacuums or temperature cycling of the device to minimize contamination stemming from the unwanted deposition of any other gases in the environment.
Figure 1: Simulation results and experimental design.

a) Vapor pressures of relevant gases [32]. The dashed line highlights the chamber’s base pressure. b) Artist’s impression of the photonic circuit. Light is injected and collected using an array of optical fibers coupled to input/output grating couplers. MMIs are used to split the light 50:50, forming the interferometer. The electrical contacts are used to apply a voltage to the heater elements, placed above the cladding close to the long spiral delay arms. c) Scanning Electron Microscopy image of the exposed 1056±2 μm section of waveguide, with 10 μm scale; d - f) Simulated mode profiles for unclad, glass and ideal Xe clad waveguide cross-sections. g) Image capture of the experiment after a full-film deposition with Xe build up on the chip. h) An overhead view of the experimental setup, mirrors were used to align the setup while under vacuum.

3 Materials and Methods

Fabrication

We designed an integrated Mach-Zehnder Interferometer (MZI) on a commercially-available SOI platform (Fig. 1b) to characterize the modulation capability of Xe. We used standard strip waveguides of 500 nm width x 220 nm height for operation within the telecom C-band and to support the fundamental TE mode. The SOI platform uses a 2 μm layer of SiO$_2$ buried oxide (BOX) and another 3 μm of SiO$_2$ cladding. Thin metallic layers (2 μm - aluminium and 120 nm - titanium nitride respectively) are deposited and patterned on top of the cladding to form electrical wires, pads and resistive heaters to be used for localized thermo-optic phase shifting over specific waveguide sections. The SiO$_2$ cladding was removed from one of the arms of the MZI using a Buffered Oxide Etch (BOE 7:1), exposing the spiral section entirely.

Simulation

Simulations (Lumerical MODE) calculated the modes supported by the cross-section of a straight waveguide (Fig. 1d-f). We approximately modelled how Xe would deposit on top of the waveguide and assumed structural symmetry because of its spiral nature (Fig. 1c). The waveguide’s geometry will ultimately affect how Xe distributes across it. Surfaces without line-of-sight to Xe flow (shadowed) would see reduced deposition; conversely, direct line-of-sight implies enhanced growth. Simulated Xe shadows are at an angle of 60° to the horizontal, approximated from the experimental setup shown in Fig. 1g-h). We also make an assumption based on the Knudsen number, (the ratio between the mean free path of Xe [35] and the vessel diameter) that Xe flows in the molecular regime at the low pressures of our cryogenic vessel. To emulate an over-etch, we removed SiO$_2$ from under the waveguide until the group indices of experiment and simulation coincided. Within the experimental error, this occurred for undercuts of 200 nm. The thermo-optic effect plays a large role when dropping from room temperature to cryogenic temperatures. Therefore, we extracted the group indexes of Si [36] and SiO$_2$ [37].
from refractive index data around cryogenic temperatures. Similarly, the group index of Xe was extracted using its extrapolated refractive index [34].

Circuit design

We used grating-couplers as optical inputs and outputs to interface with the chip. These are standard components optimized for the quasi-TE mode and an angle of incidence of 11° to avoid back reflections from second-order diffraction effects [38]. The input light is split using a multi-mode interference structure (MMI), acting as balanced beam-splitters designed for a 50:50 splitting ratio. We used MMIs for their relative resilience to fabrication imperfections [30] and to reduce the number of variables we had to control during the experiment. Waveguide sections of 1 mm in length were arranged in a spiral configuration and placed on each side of the MZI; both arms were then path-matched. The MZI structure is completed with a second 50:50 MMI and coupled out of the chip into optical fibers through two additional grating couplers.

Heater elements (each 180 µm in length) are located symmetrically along each arm of the MZI to provide a local heat source. These follow standard design rules used for TOPS. Both heater elements are connected electrically in parallel (centered symmetrically within 170 µm of the exposed region) to minimize any phase-shift in the optical path induced by heat. The dimensions of the cladding openings (windows) limit heater proximity to the exposed waveguides. This makes it difficult to estimate accurately the amount of heat dissipated by the resistor that reaches the waveguide sections. We give the total power consumption ($P_{total}$) for every example, but only half of that ($P_{local}$) is dissipated in immediate proximity to the spirals; the other half is at a distance of 400 µm.

Experimental setup

We placed the device under test (DUT) inside a continuous-flow cryogenic probe station (Lakeshore CPX). We ensured thermal contact with the probe station sample-stage using a high thermal conductivity varnish (CMR-Direct GE-7031). The probe station was evacuated to $1 \times 10^{-4}$ mBar using an Agilent TPS-compact pumping system, and then cooled using liquid helium. Intrinsic system cryopumping brought the internal pressure down to $1 \times 10^{-6}$ mBar. The sample stage temperature was stabilized by adjusting the helium flow rate and local heating using PID temperature controllers (Lakeshore Model 336 Temperature Controller). We operate between the equilibrium vapor pressure of Xe and O$_2$ at our chosen range of temperatures, reducing the likelihood of any external contamination while maintaining negligible sublimation rates of Xe.

We controlled the Xe flow rate using a Bronkhorst F-201CV mass flow controller (MFC) connected to a Xe line pressurized to $>$1 atm to prevent external contamination. The Xe used is 99.999% pure, and the lines between the gas bottle and the main chamber were evacuated to $1 \times 10^{-4}$ mBar before the first pressurization. We directed Xe flow using a bi-axial translation stage connected to a wobble stick, with the Xe entering the main chamber through a nozzle of diameter 2 mm (Fig. 1h).

Measurement procedures

We used custom software to control the experimental hardware and synchronize data acquisition, in addition to real-time monitoring of the Xe’s effect on the DUT.

The DUT was probed optically using a C-band tunable CW laser source (Yenista T100S-HP centred at 1550 nm), paired with a Yenista CT440 to accurately set the wavelength of the laser and collect full optical spectra (1510 nm - 1590 nm) from both outputs of the DUT. We set the input light polarization using a strain-based polarization controller, maximizing light coupled into the PIC.

Once the vacuum chamber reached its base temperature, we lowered the sample stage temperature to ranges determined from the data in Fig. 1. We coupled light into and out of the chip through the use of the on-chip grating couplers and used the balance of optical power between the different outputs of the on-chip MMI as a means to observe the deposition and sublimation processes.

The sample temperature was kept at 50-43 K while lowering the external radiation shields to 4.8 K, 10 K, and 19 K. The sample stage temperature target was determined using Fig. 1h. This data was refit using the Antoine equation [39]; optimized to be accurate over temperatures where vapor pressure lines intersect experimental vessel pressures. Here, we chose 50-43 K, settling on 45-43 K for the longest measurements due to subtle sublimation observed at 50 K. Xe was injected into the chamber in discrete steps, with a flow range between 3 ml/min and 15 ml/min. Flow rates and injection times were changed dynamically throughout the experiment as the Xe films saturated. Once Xe had deposited on the waveguide surface, we used on-chip TOPS to accurately control the local temperature and sublimate the Xe at a controlled rate. Xe sublimation was tested using two pre-programmed depositions, followed by controlled sublimation until no further change was observable. Multiple films were deposited for consistency, and we observed no noticeable changes in film deposition behavior.
4 Results

Simulations

We simulate the optical modes supported by the device without any cladding (Fig. 1d), with a conventional glass cladding (Fig. 1e), and for different Xe cladding layer thicknesses (Fig. 1f). We then extract the simulated values of $n_g$ to estimate the change in Xe layer thickness (Fig. 2) of our MZI test device (Fig. 1b).

Our model accounts for a potential under-etch during the fabrication process by including a 200 nm undercut in the buried oxide (BOX) layer. Additionally, we consider variations in waveguide height and width according to deviations shown in [40]. Initial simulations estimate the group index to be 4.35, rather than the experimentally observed 4.43 (Fig. 2). This value can be simulated more accurately if a certain undercut is assumed. Finally, we also account for the apparent directionality of Xe flow (Fig. 1g-h)). Our simulations suggest that a solid Xe film of thickness 200 nm will produce a considerable phase shift in the MZI, by reducing $n_g$ from 4.43 to 4.27.

Analysis of the modal overlaps between the clad and unclad sections of the undercut waveguide predicts total device insertion losses of $\leq 0.0226 \text{ dB}$. Specifically, the mode mismatch between SiO$_2$ and vacuum (or air) interfaces result in scattering losses of 0.0113 dB. On the other hand, the interface between a waveguide clad in solid Xe (1 $\mu$m thickness), and SiO$_2$ lowers the modal mismatch and associated loss to 0.0064 dB. Our simulations suggest that ideal (non-undercut, as in Fig. 1f) Xe geometries would have mismatch losses of as low as 0.0002 dB for saturated layers (additional Xe induces no further change). Device insertion losses such as these can be effectively neglected when we make comparisons to record low waveguide propagation losses of 2.7 dB/m [41].

Deposition

We monitor the power balance of the on-chip MZI to observe real-time shifts in the relative phase of the two arms during Xe deposition. Further, we extract the FSR of the structure by spectrally scanning our laser source to measure the wavelength of successive peaks in transmission. In the general case, we map the FSR values to our simulated data via $n_g$ (Fig. 2) using equation 1, ultimately providing us with an experimental estimate of Xe layer thickness.

We designed both arms of the MZI to be the same length, with the unclad waveguide length estimated to be 1056 $\pm$ 2 $\mu$m; the MZI is therefore unbalanced with an FSR of $8.3 \pm 0.1$ nm.

The change in $n_g$ with Xe thickness is less significant as the film grows, and it becomes negligible (saturated) beyond 700 nm-thick films. Xe’s effect gradually diminishes due to the increase in distance from the waveguide core, effectively reducing the interaction with the evanescent component of the mode propagated along the waveguide.

We used higher deposition rates to reach deposited film thickness values above 400 nm. An FSR of 36.2 $\pm$ 1.2 nm was measured for saturated Xe films, equivalent to a SiO$_2$-clad path mismatch of 15.8 $\mu$m, or 15 nm per micron of the exposed waveguide.

Figure 2: Dependence of the group index on Xe film thickness.

The experimentally extracted values of group index ($n_g$) with the volume of Xe introduced into the chamber. The black line represents the simulated results of our model, calculating the corresponding $n_g$ with Xe layer thickness. This is our map between experimental $n_g$ and the simulated thickness of a Xe film.
Sublimation

Once Xe has been deposited, we use on-chip heaters (see Fig. 1b) to increase the temperature in the vicinity of the exposed waveguide section. We control the temperature via the power dissipated resistively, and the total energy delivered depends on the duration of the electrical pulse. We monitor the power output of the MZI and use interference data obtained during deposition to characterize the sublimation of the Xe films (Fig. 2). Plotting the oscillation in optical power out of the chip allows us to observe this accumulation of phase, which we wrap to the phase difference ($\Delta \phi$) between the two arms of the MZI.

Figure 3(a-b) shows the thickness extrapolated from FSR measurements for different sequences of heater steps of specific power and time. For context, we observed no sublimation of thin Xe films (23.9±7.7 nm thickness) when addressing them with power cycles dissipating a total power ($P_{\text{total}}$) of <18.8 mW. As a result, this suggests induced waveguide temperatures of <60 K. We also deposited thick films (120.8±21.4 nm thickness, Fig. 3b) to scrutinize any potential changes in behavior compared to thinner films. Rates of sublimation can be approximated with a linear response for heater powers above $P_{\text{total}} = 37$ mW, for both thick and thin films. As can be seen in Fig. 3, a 2-fold increase in power typically results in an order of magnitude reduction in the time required to completely sublimate a thin film.

![Figure 3: Controlled local Xe sublimation using resistive heaters. Extrapolated values for Xe film thickness following sequential heater cycles. The translucent regions indicate the uncertainty. The heaters were activated at set power levels, and for set time periods (steps) to illustrate the sublimation process obtained starting from either, a) Thin (23.9±7.7 nm) or b) Thick (120.8±21.4 nm) Xe films. Plots (c, d) below each graph depict the electrical power delivered and the oscillation in relative phase ($\Delta \phi$) between the two arms of the MZI as the Xe sublimates with time. $\Delta \phi$ is approximately mapped from the optical power at one of the outputs of the chip.](image)

Figures 3c & d show both the measured phase and the power delivered with each consecutive step. The phase oscillates with gradually decreasing period as the Xe films become thinner. The cumulative total phase change ($\Delta \phi$) for thin films is 24.8±0.04 $\pi$; thick films demonstrated a total $\Delta \phi$ of 71.5±0.5 $\pi$, and saturated depositions (>600 nm) exhibited a total $\Delta \phi$ of 86.0±2.0 $\pi$ with a predicted $\Delta \phi$ of 85.0 $\pi$. For context, if we had used TOPS; like those re-purposed to sublimate Xe (Fig. 1b), to achieve 86 $\pi$, the device would have a length of over 8 mm. This is calculated using the approximate waveguide temperature at the highest powers used here (73 mW, Fig. 3a-b).

Figure 4a shows the optical power output with time, alongside the heater power applied to obtain a $\Delta \phi$ of $\sim 2\pi$, taken from thin-film testing. We see how desorption occurs over the entire duration of the heater on-state, with the optical power balance remaining reasonably stable while no heater power is applied. Figure 4b shows, comparatively, the response of the MZI’s optical output to the flow of Xe over the circuit, resulting in a $\Delta \phi$ of $\sim 4\pi$. Figure 4c shows the same behavior at SNSPD-friendly temperatures of 4 K. In both cases, the film grows steadily as long as the Xe flow rate remains stable, with no significant changes in the absence of Xe flow.
Figure 4: Change in the output of an integrated MZI with Xe deposition and sublimation. Measured optical power output at each arm of the MZI, showing: a) $\sim 4\pi$ phase shift as 0.3 ml of Xe is introduced into the chamber at a rate of 3 ml/min. The total cumulative Xe volume in the vessel before this measurement was 1.5 ml at a temperature of 45 K. b) $\sim 9\pi$ phase shift as 1.45 ml of Xe is introduced into the chamber at a rate of 3 ml/min. Xe thickness before this deposition is estimated to be 30 nm at a temperature of 4 K. c) $\sim 2\pi$ phase shift as 37 mW of power is applied for 10 s to the on-chip heaters. This data corresponds to step 8 in testing the sublimation of thin Xe films at a temperature of 43 K (Fig. 3d).

5 Discussion

Our results demonstrate the feasibility of re-configuring and locally tuning individual components in PICs by means of cladding layers of frozen gas. We chose Xe due to its stability in a convenient temperature and pressure range [32], which lends itself to more reproducible results ([26], Fig. 2). Similar approaches can be implemented for different environmental conditions and different substances, suggesting the potential for room-temperature operation.

More immediate benefits of Xe come from the minimal refractive index difference between SiO$_2$ ($\eta = 1.44$) and solid Xe ($\eta = 1.47$ as found in [34]). In particular, this benefits the high-index contrast attainable with Si waveguides and helps reduce insertion loss for a device of this kind. Photonic platforms based on core materials with lower refractive index, such as aluminium nitride (AlN) or silicon nitride (Si$_3$N$_4$), are likely to perform similarly, or even better due to their larger effective mode area.

The CLM device we present here exhibits under-etching of the areas where the cladding was removed, as evidenced by discrepancies between the simulated and experimentally observed group indices as highlighted in the simulation results. Our model is accurate enough to infer from collected data the under-etch depth to be 200 nm. Ideal devices would have zero under-etch to minimize mode-mismatch losses. Invariably, this would be supplemented by a slightly larger device footprint to compensate for cladding that would otherwise be missing underneath the waveguide. Under-etch implemented intentionally could instead reduce device footprint, exploiting the trade-off between mode-mismatch losses and propagation losses. CLM-ready devices introduce an element of fragility to the circuit due to an inherent coupling of the circuit to the local environment.
sequently, cleanliness and environmental isolation become fundamental factors in their storage and operation. Cryogenic environments are in a vacuum as a standard, which leaves storage alone as a criticality when compared to fully clad circuits.

The precision to which we can set a certain phase shift comes from our ability to dial-in a certain effective index. We target a specific film thickness either on the deposition of Xe or on its sublimation. A linear sublimation response translates into a nearly-exponential phase response of the MZI, as seen in Fig. 2. We observe three distinct trends in this relationship, which we define as thin (< 60 nm), thick and saturated films (> 600 nm). Figure 3(a-b) infers specific sublimation rates. For deposition, we fit early data for thin films and estimate deposition rates of between 1.6 and 1.06 mm/s. Note how such rates are partially limited in our setup by the v-groove array (VGA), covering the unclad spiral (see Figs. 2k & c respectively). For example, depositing Xe until the film saturates on a 70 µm-long device will typically yield a total phase change of 0.009 π/s, as estimated from lowest deposition rates. The accumulated phase drops to 0.006 π/s, if a thin film was already present at the start of the deposition. The precision of CLM varies over a deposition cycle, becoming exponentially more precise as the layer grows, in correspondence with a reduced effect of the thickness on the phase change.

Sublimation rates of Xe decrease rapidly away from the sublimation temperature as described by Fig. 1, suggesting that for localized heat delivery, neighboring Xe will experience little to no change in thickness. This is evidenced by the lack of observed sublimation at P suggesting that for localized heat delivery, neighboring Xe will experience little to no change in thickness. This is strongly dependent on the geometry of the device (as well as the cooling power of the cryostat) and is expected to be much lower for smaller, more compact structures.

In a similar fashion to the V_π metric used for optical modulators [42], we define the L_π as the minimum exposed length of waveguide in an MZI arm necessary to obtain a π phase shift. Consequently, for the extreme case of saturated films, L_π is 12.3±0.3 µm, while a more conservative thin film case (23.9±7.7 nm thickness), the obtained L_π is 42.5±0.1 µm. Coupled with the TOPS comparison in the sublimation results, the range of lengths observed here suggests that the exposed waveguide sections in a CLM device can be significantly shorter than typical thermo-optic [42] or electro-optic phase-shifting devices [25].

The most phase-stable operating conditions for a phase-shifting device lie between thin films and saturated films (for environmental conditions similar to this experiment), suggesting a minimum exposed waveguide length of 70 µm for at least 4 π phase-stability. Estimates for the device size will vary for different photonic platforms, in line with the index contrast between core and cladding materials. Our results show that we can deposit Xe at 45 K, tune the layer thickness, and then work at ideal SNSPD temperatures (4 K). We have also demonstrated the viability of Xe deposition directly at the base 4 K temperature, suggesting that CLM can be performed entirely at base-temperature, whilst minimizing non-Xe contamination.

CLM relies on the physical deposition of Xe and its subsequent sublimation, an intrinsically slow process. Its speed is not comparable to conventional switching mechanisms in integrated photonics. Despite this, CLM can still be used effectively for a systematic and sequential pre-calibration of the PIC’s configurable components, without a meaningful impact on the power budget. Therefore it is possible to deploy critically larger reconfigurable circuits (including photon-sources, filters, etc.) without any additional power overhead. Within these circuits it is also worth noting that such large tunability suggests the encouraging use-case of CLM as a fabrication tolerant, on-chip tunable optical delay line.

Our results provide a substantial contribution to the quest towards a fully integrated quantum photonic platform, taking advantage of the extreme temperature conditions required for the operation of superconducting devices. Specifically, our approach facilitates the use of on-chip SNSPDs with phononic integrated circuits embedding reconfigurable components that draw no power once configured, freeing up the entire power budget for the controllable components that are required to process quantum information. We envisage how the scheme we have developed offers opportunities for further exploration: for example, direct-laser-writing (DLW, [43][44]) could be used directly to tune the Xe film with zero cross-talk and no need for on-chip electrical connections.

Moreover, CLM is not restricted to switches and is intrinsically compatible with any device that uses effective/group indices to determine performance characteristics, with devices more sensitive to fabrication tolerances benefitting the most. MMI are known for their fabrication tolerance, but directional couplers, sub-wavelength gratings, and grating couplers are all examples that could be optimized in-situ using our approach.

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Author Contributions J.B conceived the idea, A.A.G designed the experiment, P.J post-processed the photonic circuit. B.M.B and G.E.V-G assembled the experimental apparatus and ran simulations. B.M.B designed the control software, performed the experiment, and analyzed the data. J.B supervised the project. B.M.B. wrote the manuscript with the support from all the authors.

Data Availability. All data needed to evaluate the conclusions in the paper are present in the paper and/or the Supplementary Materials. The primary data that supports the plots and other findings reported in this study can be requested from the corresponding author.

Supplemental Document. See the supplementary materials for supporting content.

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Low–power reconfigurability for cryogenic photonics

The practicality of the quantum devices employed in delivering successful protocols has been mostly based upon designing and testing noise–resilient approaches in the data processing. In this way, it was possible to avoid complex quantum circuits with width and depth too high to be handled within current photonic technological limits, or the demand for a cryogenic environment when using solid–state quantum sensors.

However, software developments alone are likely not enough to push the application boundaries of quantum technologies in many cases of interest. Here, we picked a specific technological challenge: the reconfigurability of photonic devices in a cryogenic environment. The ability to reconfigure a photonic circuit is key in deploying a scalable photonic architecture for LOQC, as well as implementing digital quantum simulations.

Thermo-optic phase shifters (TOPS) are limited to operate in the range of $\text{MHz}$. This can be a severe limitation in several applications. In LOQC, the feed-forward scheme requires high–speed reconfiguration, to avoid incurring unacceptable losses when employing on–purpose delay lines. High–speed reconfigurability is also a necessary requirement for classical photonic processors, recently pursued as a promising route towards achieving lower power and higher speed data processing, when compared to their electronic counterparts (e.g. $\text{GHz}$).

A perhaps even stronger limitation appears when considering cryogenic operation scenarios, required either by efficient superconducting classical processors, or by the monolithic integration of SNSPDs in the quantum photonics realm.

It is known that the TO coefficient rapidly drops below $10^{-5}\text{K}^{-1}$ at temperatures below $50\text{K}$. This might be (at least partially) compensated by the corresponding decrease in the specific heat coefficient, however, even if allowing for room–temperature power consumption, TO heaters are no scalable approach in a cryogenic environment.

Additional challenges arise when considering SOI quantum photonics, as for a satisfactory modulation several performances should be targeted simultaneously:

1. CMOS–compatibility, or compatibility with industrial–scale fabrication technologies for integrated photonic devices;
2. device footprint;
3. losses and noise introduced by the modulator;
4. power consumption;
5. speed / bandwidth;
6. low temperature ($1-4\text{K}$) operability.

Standard modulators in silicon photonics leverage upon the plasma dispersion effect: altering the concentration of free charges in Si it is possible to modulate the material refractive index $n$. Unfortunately, already at room temperature these modulators are known to introduce unwanted additional noise and losses in the device. This drawback is made worse when moving to lower operating temperatures, because the carrier freeze–out leads to higher concentrations of dopants in the Si WG, which in turns lead to higher losses and lower bandwidth. All–optical modulation, if a promising candidate for classical photonic devices, is impractical in the realm of quantum photonics, where filtering out on–demand signals from an additional bright pump is possible in principle, but technologically difficult.

The failure of $\chi^{(3)}$–based approaches to deliver a suitable modulation of $n$ in Si has pushed for solutions that introduce a $\chi^{(2)}$ effect in SOI platforms, which can be achieved in several different ways. As $\chi^{(2)} = 0$ is due to the centro–symmetric structure of Si crystals, a possibility is to break such symmetry, by either strain or strong electrical fields. If the CMOS compatibility of the first approach is yet to be proven, such an implementation

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1 Either via carrier accumulation, injection or depletion.
has already been demonstrated with satisfactory bandwidth, limited to few GHz [33]; however, the latter still requires improvements, as it introduces additional losses as high as $\sim 0.2 \text{ dB}$ per modulator.

Finally, a more radical and direct approach is to hybridize the SOI platform by introducing materials that natively exhibit strong non–linearities (e.g. they have $\chi^{(2)} \neq 0$) [6]. To achieve this, it is not necessary to completely replace the material of the WG. The confinement of the guided optical mode within the WG is high, but not perfect. Therefore, by depositing other materials in the proximity of the Silicon WG, where the evanescent field is not yet negligible, modulation of the effective refractive index is still possible. This is the approach pursued in this work. A natural choice for such a hybrid material was offered by LiNbO$_3$. However, even if already widely adopted in the field of classical communication, its widespread adoption has been hindered by the lack of a credible CMOS–compatible process to integrate it in SOI.

Non–volatile, cryo–compatible light manipulation via Xe condensation

Here we outline an approach to low–power reconfigurable on–chip switches, that is based on the principle of interacting with the evanescent field in the proximity of a WG, that we dub as non–volatile. Such naming is due to its fundamental distinction, when compared with all other technological solutions listed until now: non–volatile modulators dissipate power only when their configuration is changed, but not when it is maintained. Indeed, this is not the case for thermo-optic nor plasma-dispersion modulators: the only configurations that they can maintain without dissipating energy are the ones in absence of any external (electrical) power supply. However, any reconfiguration implies operating with an applied bias voltage $V \neq 0$. As soon as the external power supply is removed, such reconfiguration ceases: in our wording, it is volatile.

Such strategy is inspired by observing how for some experiments, most phases implemented in the circuit are held constant throughout several measurements, and sometimes even for the whole experiment. This leads to a passive level of power consumption, in line with the heat output of the thermo-optic phase shifters. In such cases, the target is to achieve low (virtually none) power consumption, rather than fast reconfigurability.

Here, we propose and perform a preliminary investigation of an unconventional solution: the controlled condensation of gases in the proximity of the WGs. This idea leverages upon the very challenge to power dissipation in integrated chips: their installation in a cryogenic setup, whereby the gas condensation can be obtained for free. The evanescent field at the surface of the cladding layer is too weak to envisage any substantial effect of replacing the SiO$_2$-vacuum interface(in a cryogenic scenario) with a SiO$_2$-X interface, with any substance X; gaseous at room temperature, but solid at the cryostat base temperature. Therefore, as schematically described in Fig. 1a, cladding has to be removed in order to expose a section of the WGs (a window).

Condensing gases on top of exposed light-confinement nanostructures is a technique already known in the literature, but its application was limited so far to the tuning of peaks in the spectral response of photonic crystal cavities [26]. More broadly, the idea to expose sections of a waveguide to the environment, transducing changes occurring in its composition into a change in $n_{\text{eff}}$, was employed for sensing purposes [33].

Experimental considerations and stability analysis

This experiment aimed to demonstrate the principle of using gas deposition as a means to fine-tune the phase of a guided optical mode, in an approach we are calling cladding layer manipulation (CLM). Beyond this it becomes important to investigate the finer details of our methodology. Here we address;

1. Geometric considerations of Xe flow for the prediction of deposition behaviour (Simulation, Fig. S1).
2. Feasibility of dropping to $4K$ after deposition at $40K$ (Fig. S2).
3. Trend in MZI stability as temperature decreases (Fig. S3).
4. Stability of Xe film thickness over time in a vacuum of $1 \times 10^{-6} \text{ mBar}$ (Fig. S4).
5. Geometric considerations of a thermo-optic solution for the tuning of film thickness (Fig. S5).
We interpreted discrepancies between simulations of Xe film growth and experimental data in terms of Xe film uniformity. Any initial differences in $n_g$ were attributed to the waveguide geometry (Fig. S1a-b). We simulated shadows (and associated regions of enhanced growth) to more accurately represent the device’s geometry and better approximate film growth behavior (Fig. S1c). The shadow angle of $60^\circ$ was estimated from the experiment and re-adjusted through repeated simulations; finally resulting in the Xe deposition behavior presented in Fig. 2.

We investigated our second point with a film of approximately 70 nm. After depositing the initial layers of Xe at 40 K and measuring the output spectrum of the MZI, we dropped the sample to a temperature of 4 K and again measured the output spectrum of the MZI (Fig. S2). We observed a phase shift per $\mu$m of $6\pm1\times10^{-4}\pi$, which correlates to a phase shift of $4.2\pm0.7\times10^{-2}\pi$ for a 70 $\mu$m device.
Another way to reduce the phase shift when dropping to 4 K would be to use thicker films if a higher quality vacuum is not available. This is evidenced in Fig. S4 where we perform stability tests of over an hour in length. Figure S4a shows us the high stability expected from a thicker (110 nm) film, especially when compared to the original 70 nm films (Fig. S4b) which were also used in our first point. Figure S4c shows the expected behavior of a vacuum system with a leak (data taken during late stage Xe depositions). This allows us to make the claim that even for non ultra-high vacuums, CLM can be used to create high-stability Xe films.

Finally, we can discuss some geometric considerations when it comes to a thermo-optic method of sublimating Xe films. Our heaters were located away from the unclad section of waveguide, to allow us to post-process the circuit. This resulted in some interesting behavior for higher heater powers, due to the lag time for heat to reach the majority of the Xe film. Figure S5(a-b) shows this as an addendum to Fig. 3(c-d), we can see that there is some asymmetry in the sublimation of the film, where the rate of sublimation rapidly increases after a sub-second period. This behavior can be further observed in Fig. 4c where some obvious asymmetry can be seen as the heaters are switched on.

Figure 8: Plots showing stability of the Xe film in different scenarios. a) 110 nm films, b) 70 nm films, c) During Xe deposition (representative of a leaky system).
Problems related to geometry can be alleviated in future implementations due to the small feature size required from a CLM device, minimizing lag times, and reducing the overall footprint. Alternatively, the heaters should be located in much closer proximity to the spiral, or another method of energy delivery is needed (such as LDW mentioned in the discussion). Existing devices (MZIs or otherwise) can also have their total device footprints reduced using Xe, by substituting or combining path mismatch with a change in $n_g$. Here power consumption is tied only to the changing of phase inside the device, steady-state configurations require no additional power to maintain.

Figure 9: Plots (a, b) depict the electrical power delivered and the oscillation in relative phase ($\Delta \phi$) between the two arms of the MZI as the Xe sublimates with time as in Fig. 3. (a) is from Fig. 3a. at $37\,mW$ for $10\,s$. (b) is from Fig. 3b. at $55\,mW$ for $10\,s$. Here we notice some lag time in the phase shift of the interferometer which can be narrowed down to the geometry of the experiment.