An Effective Pulse Width Modulation Technique Analysis for CHB Multilevel Inverters

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Abstract - This paper narrates the pulse width modulation techniques used in the multilevel inverters (MLIs). In recent industrial revolution era, MLIs found in medium voltage high power applications especially in drives domain. The control technique employed in the MLIs decides the effective conversion of power in the circuit. The harmonic content present in the output signal will lead to the performance changes in the load side. This is indicated as measure of total harmonic distortion (THD). The output signal from MLIs is fewer harmonic when the number of levels is high without any filtering process. In addition, the control method of MLIs decides the effectiveness of the system and calculating the THD. There are different types of control methods employed in the MLIs in the various literatures. Each method differs from its benefits and suitable for driving the inverter switches for a particular application. The working of each models was discussed in detail. The models are created in MATLAB/Simulink platform and analyzed its effectiveness.

Keywords - Multilevel inverters, direct current source, pulse width modulation, total harmonic distortion, cascaded H bridge inverters

1. Introduction

Inverter is a power electronic circuit that converts direct current signal into alternating current signal. Conventional inverter suffers from various problems such as high THD, higher switching stress, higher dv/dt and increased switching losses. These shortcomings are not accepted for the effective operation of an inverter in the real-world applications. In order to overcome the above said concerns, additional circuits are necessary which increases cost and complexity of the overall system. Also due to the limitations, it is difficult to interface the inverter circuit with the motor drive and utility grid. Addressing these issues in the conventional inverters, the concept of multilevel inverters became popular in the early 1980s. MLIs are having many power semiconductors switches able to produce the output with staircase type of structure. The most attractive features of MLIs include low distortion, operate with low switching frequency, low dv/dt and smaller common mode voltage. MLIs are categorized into three types: diode clamped MLI, flying capacitor MLI and cascaded H bridge (CHB) MLI. Common DC sources are utilized by diode clamped and flying capacitor MLIs. Whereas in CHB MLIs need separate DC sources as an input. Out of three configurations, MLIs with CHB structure is mostly preferred because of its potential flexibility [1]. The shortcomings of CHB MLIs are it requires a greater number of switches and DC sources.

Extensive researches are going on to reduce the number of semiconductor switches and corresponding DC sources. The significant part in the inverter circuit is its control technique [2]. This paper proposes an effective pulse width modulation technique used for MLIs. There are varieties of PWM strategies available in the literature, these are suitably selected based on the application.

Fig. 1: MLI classification

The multilevel inverter family classification is shown in Figure 1. These MLIs have certain arrangement of power semiconductor devices and capacitor voltage sources in order to synthesize the output voltage with better harmonic spectrum.

Fig. 2: Staircase output of MLI.

With respect to Figure 2, it is observed that the number of levels decides the output quality in terms of harmonics. More the number of levels, the shape of the output is closer
to sine wave [3]. This decreases the filtering process and associated accessories at the load side.

2. Cascaded H Bridge MLI

The CHB MLI is found in many applications due to its advantages. In cascaded structure, numbers of cells or modules or H bridges are connected in series to obtain the required output voltage. Each cell has a full bridge inverter arrangement with isolated DC link [4]. If the cell voltage is \( V_{dc} \), then each cell produces three voltages at the output \(+V_{dc}, 0\) and \(-V_{dc}\). The output voltage level is calculated using the Equation (1),

\[
V_{out} = (2n + 1)
\]

\( n = \) Number of cells

\[\text{Fig. 3: Five level MLI}\]

Consider the number of cells is two in the MLI structure shown if Figure 3, there are five levels in the output voltage possible. Voltage across the load will be the addition of individual H bridge voltages at any time. The input source may be equal or unequal for each cell that describes the structure with the name of symmetrical and asymmetrical [5]. In asymmetrical configuration, devices of different structures with the name of symmetrical and asymmetrical may be equal or unequal for each cell that describes the individual H bridge voltages at any time. The input source is possible. Voltage across the load will be the addition of multiplicities in MLIs. It is the inherent property of MLI that involves (m-1) carriers to obtain ‘m’ levels in its output.

The CHB MLI is found in many applications due to its advantages. It is used to redistribute the losses or charging and discharging the capacitors. Number of multiplicities in each stage is shown in the following Table 2.

| \( V_{out} \) | \( V_{H1} \) | \( V_{H2} \) | Multiplicity |
|---|---|---|---|
| \( V_{dc} \) | \( V_{dc} \) | \( V_{dc} \) | 1 |
| \( 0 \) | \( V_{dc} \) | \(-V_{dc}\) | 2 |
| \( -V_{dc} \) | \( V_{dc} \) | \(-V_{dc}\) | 1 |
| \( -2V_{dc} \) | \( V_{dc} \) | \(-V_{dc}\) | 2 |

3. Modulation techniques

Modulation technique employed in MLI is based on the switching frequency used to control the power devices. Multiple commutations in a cycle occur if the switching frequency is more [7]. Multilevel inverter generates sinusoidal voltages from discrete voltage level, the PWM strategies accomplish this task. Different application of the system would require type of PWM to be employed in the system [8]. Various modulation schemes employed in multilevel inverter is shown in Figure 4. Each scheme will implies a unique nature with respect to the harmonic spectrum.

| MLI Modulation Methods |
|---|
| Based on Space vectors |
| Based on Voltage levels |
| Space Vector PWM | Space Vector control | Multicarrier PWM | Selective Harmonic Elimination |
| Phase Shifted PWM | Level Shifted PWM |
| In-phase disposition (IPD) | Opposite Phase Disposition (OPD) | Alternate Phase Disposition (APD) |

Fig. 4: MLI modulation types

From the table, it is clearly comprehended that, to obtain the required output voltage level 0, \(+V_{dc}\) and \(-V_{dc}\) there are number of connection schemes available. This flexibility in the switching scheme is referred as multiplicity in MLIs. The following Table 1 shows different switching states with the respective output levels.

| Table 1: Switching States |
|---|---|---|---|---|
| Cell H1 | Cell H2 | Output |
| \( S_{11} \) | \( S_{12} \) | \( S_{13} \) | \( S_{14} \) | \( S_{21} \) | \( S_{22} \) | \( S_{23} \) | \( S_{24} \) | 2\( V_{dc} \) |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | \( V_{dc} \) |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | \( V_{dc} \) |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | \( V_{dc} \) |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | \( V_{dc} \) |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | \( V_{dc} \) |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | \( V_{dc} \) |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | \( V_{dc} \) |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | \( V_{dc} \) |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | \( V_{dc} \) |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | \( -2V_{dc} \) |

Table 2: Multiplicity Levels
disposition, opposite phase disposition and alternate phase disposition are the types of level shifted PWM method [10].

**Phase shifted PWM**

The carriers have the same magnitude and frequency shifted in phase levels in phase shifted PWM. Phase shifting among the carriers is found by Equation (2),

\[ \theta = \frac{360}{m - 1} \]

Where, \( \theta \) = Phase shift angle
\( m \) = Number of levels in phase voltage

From \((m-1)\) carriers, \(2(m-1)\) switching pulses are obtained and given to \(2(m-1)\) switches. PSPWM arrangement is shown in Figure 5.

**Level shifted PWM**

Level shifted PWM exposes the carriers have the same magnitude and frequency, but shifted in DC level. Based on the carrier arrangement, LSPWM is categorized into three types namely in phase disposition (IPD), opposite phase disposition (OPD) and alternate phase disposition (APD) [6]. The carrier structure of IPD, OPD and APD is shown in Figure 6(a) and 6(b) and 6(c).

**Hybrid PWM**

Hybrid pulse width modulation technique combines the features of space vector modulation and selective harmonic elimination techniques. If the multilevel inverter operates under steady state condition, then selective harmonic elimination will be much useful in controlling the inverter switches. On the other hand, if it exposes the dynamic behavior, space vector modulation is widely used [8]. It’s a mixed frequency PWM, where a high voltage module is operated at low frequency and lower voltage module is operated at high frequency. The combined effect is realized using hybrid technique in multilevel inverter is shown in Figure 8.
One of the challenging tasks in multilevel inverters is managing the switches with respect to the conduction periods. Because in MLIs, the number of semiconductor switches increases with the output voltage level. With the higher number of switches, the associated complexity in designing the control circuit will increase. Also, the conduction losses will have a significant effect on system efficiency [9]. In order to address these limitations, reduced switch count multilevel inverters came into picture in recent times. Many literature effectively analyze this topology with reduced carrier PWM signal [10]. It requires \((m-1)/2\) level shifted unipolar carriers to drive \(m\)-level inverter. The polarity of the output voltage is defined by the polarity of the modulating signal. Figure 9 shows the carrier arrangement for a five-level inverter.

**Fig. 8: Hybrid PWM**

**Reduced carrier PWM**

4. **Simulation results**

Simulation study of the model is performed using the MATLAB/Simulink platform in order to validate the results. Conventional five-level CHB and its control scheme using PSPWM is shown in Figure 10.

**Fig. 10: Simulation model**

The output voltage and current for the five-level MLI is obtained for the RL load (\(R=10 \Omega, L=5 \text{ mH}\)) is shown in Figure 11. The corresponding harmonic spectrum is illustrated in Figure 12.

**Fig. 11: Output voltage and current**

(a)
Fig. 12: Harmonic spectrum

Results obtained from the simulation shows that each modulation technique will expose different harmonic spectrum.

5. Conclusion

Different pulse width modulation techniques are discussed and analyzed in this paper. Effective conversion of input DC voltage to an output AC voltage depends on the modulation technique will be used in the system. It is used to control the operation of multilevel inverter. Also, the multiplicity details for each stage will give the flexibility in the operation, which is the inherent property of MLIs. The simulation results give better understanding of using LSPWM with reduced harmonic content. For asymmetric configuration, hybrid PWM will be most suitable in MLI structure.

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