Advances and Frontiers in Single-Walled Carbon Nanotube Electronics

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Single-walled carbon nanotubes (SWCNTs) have been considered as one of the most promising electronic materials for the next-generation electronics in the more Moore era. Sub-10 nm SWCNT-field effect transistors (FETs) have been realized with several performances exceeding those of Si-based FETs at the same feature size. Several industrial initiatives have attempted to implement SWCNT electronics in integrated circuit (IC) chips. Here, the recent advances in SWCNT electronics are reviewed from in-depth understanding of the fundamental electronic structures, the carrier transport mechanisms, and the metal/SWCNT contact properties. In particular, the subthreshold switching properties are highlighted for low-power, energy-efficient device operations. State-of-the-art low-power SWCNT-based electronics and the key strategies to realize low-voltage and low-power operations are outlined. Finally, the essential challenges and prospects from the material preparation, device fabrication, and large-scale ICs integration for future SWCNT-based electronics are foregrounded.

1. Introduction

As the dimension of electronic devices shrinks continuously along Moore’s law,[1] the physical limits to silicon (Si)-based complementary metal–oxide–semiconductor (CMOS) transistors scaling have been reached, resulting in severe performance degradations due to the short-channel effects,[2] gate oxide tunneling, and unmanageable power consumption.[3,4] To further downscale the transistors without degrading their performance along the more Moore trend, great efforts have been devoted to exploring revolutionary new materials and device structures such as strained Si, nanotubes and nanowires, III–V materials, high-k (dielectric constant) gate dielectric, as well as trigate device configuration.[5–10]

Among these emerging electronic materials, single-walled carbon nanotube (SWCNT) is the most promising electronic material, owing to its quasi-1D sp² structure, extremely high carrier mobility, thermal conductivity, and superior flexibility and stability.[11–16] Due to the excellent electrostatic gate control on the SWCNT channel,[17–19] SWCNT-field effect transistors (FETs) are expected to play an important role in the next-generation digital integrated circuits (ICs) as the fundamental building blocks. Since report of the first SWCNT-FET in 1998,[20] a remarkable progress in SWCNT-based electronics has been made, especially in the past decade. To study the transport properties and explore the excellent device performance with unique functionalities, many innovative device structures and process approaches have been adopted.[19,21–38] The electrical performances of these devices have even outperformed Si-based counterparts in comparable sizes. High-performance individual SWCNT CMOS-FETs with the gate length less than 10 nm have been demonstrated.[30] These ultrasmall-scaled SWCNT devices exhibited higher intrinsic carrier mobility and on-state performance than Si CMOS-FETs with a similar gate length but at a lower supply voltage. Furthermore, graphene-contacted SWCNT-FETs with a gate length of 5 nm have also been reported, where the conventional metal source (S) and drain (D) electrodes (e.g., Pd or Sc) were replaced with graphene.[30] Because of broadening of the depletion region at the graphene/SWCNT contacts, the direct tunneling between the S and D is prohibited, leading to an essentially improved off-state performance with a much smaller subthreshold swing (SS) of 73 mV dec⁻¹. Based on low-resistance end-bonded contacts formed through a solid-state reaction between a semiconducting SWCNT (s-SWCNT) and deposited Co–Mo alloy S/D electrodes,[39] a p-channel SWCNT transistor with all components restricted within 40 nm has been constructed.[31] The end-bonded contact scheme allows the scaling of the contact length down to 10 nm without increasing the contact resistance. As a result, the sub-10 nm gate length SWCNT-FET can deliver a significantly higher current density above 0.9 mA μm⁻¹ at a low supply voltage of 0.5 V with an SS of 85 mV dec⁻¹. This remarkable performance has well exceeded that of mainstream Si devices.

Despite these notable achievements, the inability to precisely control specific chirality, diameter, position, and orientation of SWCNTs significantly increase the device-to-device variations...
and restrict realistic technology applications based on individual SWCNTs. In contrast, a SWCNT thin film that is composed of a huge number of individual SWCNTs, in the form of either random networks or aligned arrays, is immune to the challenges of individual SWCNTs because the thin film structure offers attractive homogenous electrical properties even with heterogeneous SWCNTs. This could also offer a large active area to achieve a high current driving capability.[40–43] A variety of electronic devices and circuits based on SWCNT thin-film transistors (TFTs), such as the driver circuits for flat-panel displays,[44,45] biosensors,[46,47] fundamental logic gates,[48–51] medium- and large-scale ICs,[41,54–55] and even a 16-bit microprocessor (RV16X-NANO) composed of more than 14,000 CMOS SWCNT-TFTs,[56] have been demonstrated with excellent electrical performances and industrialization feasibility. However, several key issues are to be addressed in order for practical applications of SWCNT thin films as an active channel material in FETs, including high packing density, high semiconducting purity, and high alignment of SWCNTs.[57,58] As-produced SWCNTs are a mixture of semiconducting (s-) and metallic (m-) SWCNTs,[59,60] and the existence of m-SWCNTs in a transistor channel could short the S and D electrically, leading to device failure. Great efforts have been devoted to selective synthesis of high-purity s-SWCNTs. One way is to synthesize s-SWCNTs by particular catalyst design[61,62] or introduce a process of in situ selectively etching m-SWCNTs during CNT growth based on the differences in reactivity and conductivity of s-SWCNTs and m-SWCNTs.[63–66] The other way is to sort SWCNTs by noncovalent functionalized post-treatment, in which m- or s-SWCNTs are selectively wrapped with specific surfactants/polymers. The commonly used noncovalent methods include density gradient ultracentrifugation,[67,68] chromatography,[69] DNA[70] and conjugated polymer wrapping.[60,71] The s-SWCNTs sorted by these methods usually possess extremely high purity up to 99.99%.[59,72–74] In addition to high semiconducting purity, a highly aligned array with high packing density is also required to implement large-scale SWCNT-based ICs. Compared with chemical vapor deposition (CVD)-grown aligned SWCNTs, solution-processed aligned SWCNTs exhibit higher packing densities and higher yields.[58,75–78] All these advancements and achievements on the growth, sorting, and processing enable potential applications of SWCNT-TFTs on ultralarge-scale ICs. Recently, methylation-induced reversible metallic-semiconducting transition of CVD-grown SWCNT arrays has been reported.[70] It was found that selective reaction of methyl radicals to the surface of m-SWCNTs could reversibly destroy π-conjugated electronic structure and open up the bandgap of the methylation-treated m-SWCNTs, yielding a high purity of s-SWCNTs (>97.5%). In addition, solution-processed well-aligned s-SWCNT arrays with a purity of 99.9999% have been prepared on a 4 in. Si wafer.[58] These aligned s-SWCNT arrays have high packing density (between 100 and 200 tubes μm−1) with full surface coverage. Top-gated transistors fabricated on these aligned s-SWCNT arrays exhibited a high on-state current exceeding 1.3 mA μm−1 and a peak transconductance of 0.9 mS μm−1 under a power supply of 1 V, which is better than that of commercial Si MOS-FETs. Through modifications and optimizations of standard solution-based processing methods, fabrication of SWCNT-TFTs on industry-standard 200 mm wafers using commercial Si manufacturing facilities has also been reported.[80] The wafer-scale uniformity and reproducibility of the device performances enable the SWCNT-TFT technologies from research laboratories to commercial Si CMOS compatible manufacturing facilities.

Further development of SWCNT-based transistors for next-generation high-performance and low-power consumption ICs is still facing many daunting challenges from the material preparation, device fabrication, and circuit design and device–circuit system optimization. In this review, recent advances and breakthroughs in SWCNT-based FETs/TFTs and their electronic applications will be the focus. We begin with the fundamental electronic structures and properties of SWCNTs in Section 2. Then, several device structures of SWCNT-FETs will be introduced and discussed with the contact properties and the sub-threshold switching properties of SWCNT-FETs in Section 3. Section 4 explores the ballistic transport in SWCNTs and outlines the progress of SWCNT-FETs/TFTs in high-performance electronic applications. In Section 5, we concentrate on the state of the art low-power SWCNT-FETs/TFTs and the representative strategies to realize low-voltage and low-power operations. Finally, the key challenges and outlooks for SWCNT-based high-performance and low-power electronics are summarized.

2. Structure and Electronic Properties of SWCNTs

An individual SWCNT can be structurally described as a seamless, hollow cylinder rolled up from a piece of graphene sheet along a chiral vector C (Figure 1a).[81,82] Most of SWCNTs have a diameter less than 2 nm, making them 1D nanostructure due to the high aspect ratio (i.e., the length over diameter). The chiral vector C indicates the rolling-up direction and defines the circumference of the SWCNT. Based on the basis vectors (a1 and a2) of the graphene sheet, the vector C can be defined as

\[
C = n a_1 + m a_2
\]

where n and m are integers, and \( n \geq m \), \( |a_1| = |a_2| = a = \sqrt{3} a_{C-C} \), \( a_{C-C} = 0.142 \text{ nm} \) is the nearest-neighbor C–C bond length. Thus, each SWCNT can be described by a pair of chiral indices (n, m) with a diameter \( d_{\text{CNT}} = |C|/\pi = (a/\pi) \sqrt{n^2 + m^2 + nm} \) and a chiral angle \( \theta \) (the angle between \( C_0 \) and \( a_1 \)).[81–85] As shown in Figure 1b, in terms of the chiral indices and the chiral angle, SWCNTs can be categorized as zigzag tubes (m = 0, \( \theta = 0^\circ \)), whose chiral vectors are purely along \( a_1 \), or armchair tubes (n = m, \( \theta = 30^\circ \)), whose chiral vectors are all along the direction exactly between \( a_1 \) and \( a_2 \), and chiral tubes (n ≠ m, 0° < \( \theta < 30^\circ \)).[82,86]

Carbon atoms in SWCNTs are in the covalent sp2 hybridization, the same as those carbon atoms in graphene.[87,88] Thus, the electronic properties and the band structures of an SWCNT can be simply derived from that of graphene. Figure 1c shows the calculated energy dispersion contours of graphene using a tight-binding model consisting only of \( \pi \) orbital electrons,[89] where the upper \( \pi^* \) antibonding band (conduction band) and the lower \( \pi \) bonding band (valence band) touch at six points (Dirac points) at the corners of the Brillouin zone.[89,90] The Fermi level passes through the six points, suggesting graphene is a zero-bandgap semiconductor or semimetal.[19,87,89] As electron motion is along not only the axis of an SWCNT, but also its circumference, the

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Atomic structure and electronic properties of SWCNTs. a) An individual SWCNT rolled up from a graphene sheet along a chiral vector \( C_h \). b) Classification of SWCNTs: zigzag, armchair, and chiral CNTs, respectively. (a,b) Reproduced with permission.\(^{[82]}\) Copyright 2020, Elsevier. c) The calculated energy dispersion contours of graphene. d) The band-structures of SWCNTs with different electronic properties depending on the relation of the quantized lines to the Brillouin zone of graphene. (c,d) Reproduced with permission.\(^{[89]}\) Copyright 2006, IOP Publishing. e) The density of states (DOS) for (11, 7) and (9, 9) SWCNTs, respectively. Reproduced (Adapted) with permission.\(^{[98]}\) Copyright 2020, American Chemical Society.

The band structure of an SWCNT can be achieved by imposing a periodic boundary condition around the circumference of the nanotube.\(^{[91,92]}\) Electron motion along the nanotube axis is free and the corresponding component of the momentum \( k_\parallel \) is continuous. In contrast, the perpendicular component of the momentum \( k_\perp \) is along the direction of the chiral vector \( C_h \) and quantized due to the periodic boundary condition

\[
k_\perp \cdot C_h = 2\pi p
\]

where \( p \) is a nonzero integer. Therefore, the allowed electronic states for an SWCNT are defined only by a set of parallel lines in the \( k \)-space with quantized \( k_\perp \) states superimposing on the 2D Brillouin zone of graphene (Figure 1d).\(^{[83,89]}\) The 1D sub-band structures of an SWCNT can be obtained via cross-sectional cutting of the energy dispersion of graphene with these parallel quantized lines.\(^{[84,89,90]}\) The band structure in the vicinity of the Fermi level is determined by those \( k_\perp \) states that are near the Dirac points and they govern the electrical transport properties in SWCNTs. If the quantized lines cut across the Dirac points of graphene (see the upper-right panel in Figure 1d), the SWCNT is a metallic tube with a zero-energy gap (see the lower-right panel in Figure 1d). Otherwise, the SWCNT is a semiconducting tube with a finite energy gap between the valence and conduction bands (see the upper-left and lower-left panel in Figure 1d). In summary, an \((n, m)\) SWCNT is semiconducting if \( n - m \) is not dividable by 3.\(^{[90–94]}\) The bandgap is inversely proportional to its diameter, i.e., \( E_g \approx 0.7 \text{ eV}/d_{\text{CNT}} (\text{nm}) \).\(^{[95]}\) Otherwise, the SWCNT is metallic with a relation of \( n - m = 3q \), where \( q \) is an integer. All armchair \((n = m)\) SWCNTs are metallic. However, owing to the curvature effect induced by small diameters, the rest of metallic \((n \neq m)\) SWCNTs exhibit quasi-metallic behavior with a small bandgap \( E_g \approx k_B T \) at room temperature.\(^{[90,96,97]}\)

Figure 1e shows the density of states (DOS) for (11, 7) and (9, 9) SWCNTs, respectively.\(^{[98]}\) For the (11, 7) SWCNT, the DOS vanish, and an energy gap of \( \approx 0.57 \text{ eV} \) occurs at the Fermi level \((E = 0)\), showing it is a semiconductor. In contrast, the DOS are finite in the vicinity of the Fermi level in the (9, 9) SWCNT, indicating a metallic tube. Due to the 1D characteristics, the 1D DOS of SWCNTs shows Van Hove singularities at higher energies.\(^{[99]}\)

In addition to the unique electronic properties, SWCNTs also possess excellent mechanical properties resulting from the covalent sp\(^2\) bonding between carbon atoms. Their superior mechanical properties, e.g., high Young’s modulus (270–950 GPa) and tensile strength (11–63 GPa),\(^{[100]}\) have made SWCNT a promising material for flexible and stretchable electronics.\(^{[101]}\)
3. SWCNT-FET Fundamentals

3.1. Device Structures of SWCNT-FETs

Since the first FET based on an individual SWCNT was demonstrated in 1998, several kinds of device structures of SWCNT-FETs have been proposed and implemented. The two most common structures are back-gated structure (Figure 2a) and top-gated structure (Figure 2b). In the back-gated device, a heavily doped Si is normally used as the substrate and the back-gate. The active channel consists of either an individual SWCNT or an SWCNTs thin film, separated from the gate using a thin dielectric layer. Although the back-gated devices are easily fabricated and have been successfully employed for the purpose of proof-of-concept, they are not easily integrated with other components because of their global back-gates. In contrast, the top-gated structures are more suitable for device integration and have been extensively employed in SWCNT-based ICs. The top-gated devices are conventionally built on an insulating substrate, like a quartz wafer, a flexible plastic film, or a Si wafer with thermally grown SiO$_2$. To obtain high gate capacitance and gate control efficiency, high-$k$ HfO$_2$, ZrO$_2$, and Y$_2$O$_3$ thin films have been adopted as the gate dielectric layers.\cite{9,102,103}

In Si CMOS technology, a self-aligned device structure is usually adopted to accurately position the edges of the S/D and the gate (G) electrodes so that there is no significant overlap or gap between these electrodes.\cite{104} This symmetric-gate FET (SG-FET) structure (Figure 3a) has been employed for making high-performance SWCNT-FETs because of the minimized parasitic capacitances and leakage current between the G and S/D electrodes.\cite{24,27,54} In addition to the SG-FET structure, asymmetric-gate FET (AG-FET) structures have been also proposed and realized for SWCNT-FETs.\cite{105-111} In the AG-FETs, the main-gate covers most of the SWCNTs channel with a gap between the G and the D electrodes (Figure 3b). In addition, a partial-gate connected to the D electrode (Figure 3c), or a
specially biased assistant-gate near the D electrode (Figure 3d) can be introduced. In the SG-FETs (upper panel of Figure 3e), the barrier near the drain contact is very thin at the off-state due to the strong gate control on the ultrathin body of the SWCNTs channel, giving rise to obvious electron tunneling current and ambipolar behavior. Contrarily, in the AG-FETs, because of the gap between the G and D electrodes, the partial-gate or a specially biased assistant-gate near the D electrode, the main-gate control on the energy band of the channel near the drain contact is significantly reduced, leading to a relative thick barrier near the drain contact (lower panel of Figure 3e), which could significantly suppress electron tunneling current and ambipolar behavior even at a high source–drain bias, $V_{DS}$. Table 1 lists several kinds of device structures of SWCNT-FETs and their advantages.

### 3.2. Contacts Properties of SWCNTs and Metal Electrodes

In a conventional Si MOSFET, the S and D electrodes are usually heavily doped Si, making the S (or D)/Si-channel contacts ohmic. However, owing to the lack of simple and efficient doping approaches for SWCNTs, the S and D electrodes in a SWCNT-FET are metals and the S (or D)/SWCNTs contact exhibits typical Schottky contact properties.\cite{15,112–114} The Schottky barriers (SBs) at the metal electrodes/\textit{s}-SWCNT interface plays a significant role in the operation of SWCNT-FETs.

When a metal is in contact with a bulk semiconductor such as silicon, metal-induced gap states (MIGSs) form on the semiconductor surface. The MIGS decay exponentially away from the metal/semiconductor interface. Thus, a dipole sheet is created at the interface due to the charges in the semiconductor side and the image charges induced in the metal side. It results in bending of the energy band near the semiconductor surface. Thus, the position of the Fermi level (i.e., the charge neutrality level) at the semiconductor surface is pinned due to the MIGS.\cite{115} The Fermi level pinning effect dominates the formation of the Schottky barriers at the metal/bulk semiconductor interface, leading to nearly constant barrier height, which is only weakly dependent of the metal work-function. However, the MIGS induced Fermi level pinning plays a minor effect in the metal/SWCNT contact due to the 1D ultrathin SWCNT.\cite{112,116,117} Self-consistent calculations show that the MIGS in SWCNT decay more rapidly than in bulk semiconductors. As a result, the barrier width at the metal/SWCNT interface is only a few nanometers so that electrons or holes can effectively transport across the contacts, with a negligible effect of the Fermi level pinning. As a consequence, a metal/SWCNT contact is strongly affected by the work-function difference between the metal and SWCNT.\cite{89} For example, a high work-function metal, such as Pd (5.1 eV), easily forms a nearly transparent barrier (or a negative barrier) with an SWCNT since the Fermi level of the metal tends to line up with the valence band of the SWCNT, in favor of holes transport, but not for electrons transport. Contrarily, a low work-function metal, such as Sc (3.3 eV), in contact with a SWCNT produces an almost transparent barrier for electrons, promoting electrons transport. If the electron barrier is much higher than the hole barrier, a SWCNT-FET works as a p-type FET. Otherwise, it operates as an n-type FET. For the SWCNT with a small bandgap, its electron barrier is comparable with its hole barrier, the SWCNT-FET is likely ambipolar.\cite{113,114,118}

As the band bending near the contacts of a SWCNT-FET can be modulated by the applied gate voltage to achieve the control of the channel current, the device operates more like a SB transistor (Figure 4).\cite{15} When the FET is at the off-state, the SB at the source contact is thick and the tunneling current is very small. The off-state current is mainly determined by the thermionic emission over the SB. With increasing of the gate voltage above the threshold voltage, $V_{TH}$, the energy band of the SWCNT in the middle of the channel is raised gradually, leading to a very thin SB at the source contact and an increased tunneling current. The FET operates at the on-state. Consequently, the carrier transport in a Schottky-contact SWCNT-FET is determined by the competition between the thermionic emission and thermally

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Table 1. Several kinds of device structures of SWCNT-FETs and their advantages. (SG: symmetric gate; AG: asymmetric gate; BG: back-gated; TG: top-gated; SA-TG: self-aligned top-gated).

| Device structure | Advantages of the device structures |
|------------------|-----------------------------------|
| SG-FET BG device (Figure 2a) | 1) Simple and easy fabrication processes. 2) Suitable for purpose of proof-of-concept. |
| TG device (Figure 2b) | 1) High-performance arising from highly efficient gate control capability through ultrathin high-\textit{k} gate dielectric. 2) Suitable for large-scale device integration. |
| SA-TG device (Figure 3a) | High-performance resulting from the reduced parasitic capacitances and leakage current between the G and S/D electrodes. |
| AG-FET AG with a gap between the G and D electrodes (Figure 3b) | High-performance achieved from: 1) Suppression of off-state leakage current. 2) Suppression of ambipolar behavior at high source–drain bias. |
| A partial-gate connected to the D electrode (Figure 3c) |  |
| A specially biased assistant G near the D electrode (Figure 3d) |  |

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Figure 4. Energy band diagram of a Schottky-contact SWCNT-FET showing the carrier injection mechanism at the off-state and on-state, respectively. Reproduced with permission.\cite{15} Copyright 2002, American Physical Society.
assisted tunneling, which is controlled by the gate voltage modulation of the SB at the source contact.\textsuperscript{[119]} This carrier transport mechanism is entirely different from that in conventional bulk-switching transistors where the current is controlled by the thermionic emission over the bulk barrier inside the channel.\textsuperscript{[15]}

The SB at a metal/SWCNT contact is easily affected by adsorbed oxygen.\textsuperscript{[114,120,121]} Typical SWCNT-FETs built from as-grown nanotubes are usually unipolar p-type devices. It was observed experimentally that the adsorption of oxygen may change the work-function of the metal and thus affect the SB and the device performance as well.\textsuperscript{[114]} After oxygen exposure, the conduction behavior of the device could change from n-type to p-type, suggesting that oxygen adsorption enhances hole conduction, but inhibits electron conduction.

### 3.3. Switching Properties in SWCNT-FETs

Continuously scaling down of the feature size of CMOS FETs has enabled remarkable improvements in the integrated device density, circuit switching speed, functionality, and manufacturing cost of digital ICs. However, high power consumption becomes a bottleneck for further scaling down of ICs owing to the increasing leakage currents and difficulty in scaling down of the supply voltage, $V_{DD}$,\textsuperscript{[122,123]} and heat dissipation. In modern CMOS technology, the $V_{DD}$ has been reduced to below 0.7 V.\textsuperscript{[124]} The difficulty of further scaling down of $V_{DD}$ mainly arises from the limit ($\approx 60 \text{ mV} \text{ dec}^{-1}$) of SS at room temperature.\textsuperscript{[122,125,126]}

In terms of the operation modes of MOSFETs, when the gate bias ($V_{GS}$) is greater than the threshold voltage ($V_{TH}$), the device operates in the above-threshold region, in which the on-state current increases almost linearly with the bias voltage $V_{GS}$. The variation of the drain current ($I_{DS}$) with $V_{GS}$ can be characterized by transconductance, $g_{m}$, which is defined as

$$ g_{m} = \frac{dI_{DS}}{dV_{GS}} $$

A higher $g_{m}$ could offer higher current driving capability and signal amplifying capability of the device in the above-threshold region. When $V_{GS} < V_{TH}$, the device works in the subthreshold region. The subthreshold switching behavior is generally characterized by SS, which is defined as the inverse of the subthreshold slope

$$ SS = \frac{d\log_{10} (I_{DS})}{dV_{GS}} $$

The SS reflects the required gate voltage that causes the variation of the subthreshold current by one order of magnitude. Therefore, a small SS implies a steep switching behavior of the device, enabling a low off-state leakage current and thus a minimized passive power.\textsuperscript{[127]} The SS of SWCNT-FETs can be empirically obtained from the transfer characteristic of the device. It can be derived from electronic transport analysis based on carrier thermionic emission theory.\textsuperscript{[128]}

$$ SS \approx \frac{k_{B}T}{e} \left( 1 + \frac{C_{ox}}{C_{intrinsic}} \right) \ln 10 $$

where $k_{B}T$ is the thermal energy; $e$ is electron charge; $C_{intrinsic}$ is the capacitance induced by interface trap states and $C_{ox}$ is the gate dielectric capacitance. The $C_{ox}$ in SWCNT-FETs can be analytically expressed as\textsuperscript{[129]}

$$ C_{ox} = \left\{ \frac{1}{2\pi\epsilon_{r}\epsilon} \ln \left( \frac{\Lambda_{0}}{\pi \tau_{1}} \right) \sinh \left( \frac{2\pi t_{d}}{\Lambda_{0}} \right) \right\}^{-1} \Lambda_{0}^{-1} $$

where $\epsilon$ is the dielectric constant of the gate dielectric; $\Lambda_{0}$ is the average distance between the tubes; $\tau_{1}$ is the tube radius; $t_{d}$ is the thickness of the gate dielectric and $C_{intrinsic} \approx 10^{-10} \text{ F m}^{-1}$\textsuperscript{[130]} is the intrinsic quantum capacitance of SWCNTs.

According to the above expressions of SS and $C_{ox}$, lowering the trapped charge density (i.e., reducing $C_{intrinsic}$) at the SWCNTs-channel/gate dielectric interface, and increasing $C_{ox}$ via reducing the gate dielectric thickness $t_{d}$, or using high-$k$ dielectric materials are the most straightforward and effective approaches to reduce the SS or, in other word, increase the gate control capability. For an ideal case, $C_{intrinsic} \ll C_{ox}$, the SS could reach its limit ($(k_{B}T/e)\ln10\approx60 \text{ mV} \text{ dec}^{-1}$) at room temperature. This fundamental limit of the SS is mainly determined by the temperature-dependent thermionic emission of carriers over an energy barrier.\textsuperscript{[115,131]}

The power consumption of digital ICs is usually calculated by the formula

$$ P = V_{DD} \times I_{DD}. $$

Therefore, reducing the supply voltage $V_{DD}$ together with a low off-state leakage current is very important to achieve a low power dissipation. Downscaling of $V_{DD}$ requires a simultaneously lowered $V_{TH}$ so that the on-state performance ($I_{ON}$) can be maintained via keeping the overdrive factor ($V_{DD} - V_{TH}$) constant. As a result, the off-state current ($I_{OFF}$) inevitably increases exponentially (see the intersections between the current–voltage ($I_{DS} \approx V_{GS}$) curves and the vertical axis in Figure 5) because of an unscalable SS with a limit of 60 mV dec$^{-1}$ at room temperature.\textsuperscript{[123]} Therefore, further downsizing
of $V_{DD} < 0.5$ V, while maintaining a reasonable on/off current ratio, $I_{ON}/I_{OFF} \geq 10^4$ and a lower power consumption, requires a different carrier injection approach (e.g., band-to-band (BTB) tunneling$^{[132]}$ or Dirac source (DS) injection$^{[113,114]}$), in which the Boltzmann thermal distribution dominated limit of SS is no more a governing factor and newly established SS could be less than 60 mV dec$^{-1}$ at room temperature. The devices with higher $g_m$ and lower SS have sharp switching behavior from their off-states to on-states and vice versa and, therefore, could provide a large downsampling space of $V_{DD}$ without sacrificing the off-state performance.

4. High-Performance SWCNT-FET/TFT Electronics

4.1. Ballistic Transport in SWCNTs

Ballistic transport is highly demanded in high-performance electronic devices as it yields high current driving capability and high operating speed. Like bulk semiconducting materials, the electrical transport in SWCNTs is also affected by scattering events induced by defects or lattice vibrations, giving rise to electrical resistance. However, due to its unique 1D nanostructure, SWCNT contacted with 3D metal electrodes exhibits a quantized resistance.$^{[135,136]}$ As discussed in Section 2, the motion of the electrons along the circumference of an SWCNT is confined because of the periodic boundary condition, leading to a series of discrete quantized states. When the SWCNT contacts with metal electrodes, these discrete quantized states in the SWCNT could superimpose on the continuous states of the electrodes, producing a quantized contact resistance $R_q$. Theoretical studies indicate that each metallic SWCNT has two conducting channels with the energies near the Fermi levels of the electrodes, and each of the channels contribute a conductance quantum $G_0 (G_0 = 2e^2/h$, where $h$ is Planck’s constant) to the total conductance.$^{[137–139]}$ Therefore, a metallic SWCNT has a quantized contact resistance $R_q = 1/(2G_0) = h/4e^2 = 6.45$ kΩ.$^{[19]}$

For an SWCNT with a high structural integrity, the electron transport scattering rate in the SWCNT is low so that electrons could even have a very long mean-free-path $\lambda_{MFP}$ of the order of a micrometer.$^{[19]}$ In other words, when the SWCNT channel length is scaled down to the sub-micrometer range, for example, ≤ 100 nm, the ballistic transport can take place and the SWCNT can act as a good ballistic conductor. Si-MOSFETs with ultrashort channel length usually suffer from poor device performance due to the short-channel effects.$^{[12]}$ However, in SWCNT-FETs with very short channel length, the gate electrostatic control is significantly enhanced owing to the 1D ultrathin structures, making the SWCNT-FETs effectively immune to the short-channel effects.$^{[140]}$ As the channel length decreases, the contact resistances between the SWCNTs channel and the S(D) electrodes, rather than the channel resistance, are dominant, and their adverse impact on the ballistic transport becomes more significant. Schottky-contact SWCNT-FETs usually exhibit high contact resistances and the on-state current ($I_{ON}$) is thus exponentially decreased with increasing the SB height.$^{[15,113,118,141]}$ Therefore, mitigating the SBs and realizing ohmic contact to SWCNTs with low contact resistances are crucial to achieve ballistic transport in high-performance SWCNT-FETs.$^{[142]}$

4.2. Progress in High-Performance SWCNT-FETs

As discussed in Section 4.1, reducing the channel length and the contact resistance are two important routes to implement ballistic transport in SWCNTs. Considerable efforts on these two routes have been devoted to developing ballistic SWCNT-FETs.

In 2003, Javey et al. successfully fabricated ohmic-contact p-type SWCNT-FETs using the high work-function metal Pd as the S/D electrodes$^{[13]}$ realizing zero or slightly negative SBs at the Pd/SWCNT contacts and room-temperature ballistic transport in a short channel ($L_{ch} = 300$ nm) device (Figure 6a) with on-state conductance $G_{on} \approx 0.8G_0$. For n-type ballistic devices, Zhang et al. studied the Sc-contacted SWCNT-FETs (Figure 6b) and found almost ballistic electron transport and metallic-like behavior of the on-state conductance ($\approx 0.98G_0$ at 250 K),$^{[28]}$ suggesting barrier-free ohmic Sc/SWCNT contacts. By further optimizing the device with a self-aligned top-gated structure and adopting high-k HfO$_2$ as the dielectric layer,$^{[64]}$ the Sc-contacted n-type SWCNT-FET ($L_{ch} = 120$ nm) (Figure 6c) exhibited excellent on- and off-state performance with $G_{on} \approx 0.64G_0$, $g_m \approx 25$ μS, and SS $\approx$ 100 mV dec$^{-1}$. In addition to Sc, the low work-function metal Y (3.1 eV) can also form an ohmic contact with the conduction band of the SWCNT channel (Figure 6d).$^{[143]}$ The Y-contacted SWCNT-FET ($L_{ch} = 400$ nm) exhibited near-ballistic electron transport with a room temperature on-state conductance of $\approx 1.1G_0$.

In a ballistic device, the channel resistance is negligible, and the contact resistance mainly determines the device performance. The most commonly used contact geometry in SWCNT-FETs is side-contact or planar-contact. The contact resistance of such contact schemes increases rapidly with decreasing of the contact area and it is proportional to the contact length. Previous experiments have shown that the contact resistance increased from $\approx 5$ kΩ with contact length more than 200 nm to $\approx 65$ kΩ with contact length of 9 nm.$^{[140]}$ The increase in the contact resistance has become a major performance roadblock to ultrascaled devices. In 2015, Cao et al. proposed an end-bonded contact geometry (Figure 6e), in which the ends of the SWCNT channel were attached to the deposited Mo electrodes through carbide bonds formed in a solid-state carbide-formation reaction.$^{[19]}$ Owing to the formation of the carbide bonds, the end-bonded contact showed a zero SB and a size-independent contact resistance, resulting in an excellent downsampling behavior of the contact without increasing resistance. The Mo end-bonded SWCNT-FET ($L_{ch} = 60$ nm), with contact length scaled down to 9 nm, exhibited ballistic hole transport with a device resistance below 36 kΩ and an on-state current of 15 μA. In 2017, they further reduced the channel length to 11 nm and constructed an end-bonded device with ultrascaled contact length (≈10 nm) (Figure 6f)$^{[11]}$ The entire device has been scaled down to a tiny footprint of 40 nm, and delivered a higher current density above 0.9 mA μm$^{-1}$ at a low supply voltage of 0.5 V with an SS of 85 mV dec$^{-1}$.

When the channel length is scaled down to the deep sub-micrometer range, SWCNT-FETs can still maintain their performance and are immune to the short-channel effects. In 2010, Franklin and Chen investigated the scaling behavior of the Pd-contacted SWCNT-FETs with the channel length from 3 μm to 15 nm (Figure 6g)$^{[140]}$. The 15 nm device exhibited room-temperature conductance of 0.7G$_0$ and peak transconductance of 40 μS. The nearly ballistic transport resulted in the
Figure 6. Development of high-performance SWCNT-FETs. a–d) Ohmic-contacted SWCNT-FETs with typical metal electrodes such as Pd, Sc, and Y. (a) Reproduced with permission. [13] Copyright 2003, Springer Nature. (b) Reproduced with permission. [24] Copyright 2008, American Chemical Society. (c) Reproduced with permission. [26] Copyright 2007, American Chemical Society. (d) Reproduced with permission. [143] Copyright 2009, American Chemical Society. e,f) SWCNT-FETs with end-bonded contact formed in a solid-state carbide-formation reaction. [31,39] (e) Reproduced with permission. [31] Copyright 2017, The American Association for the Advancement of Science. (f) Reproduced with permission. [39] Copyright 2015, The American Association for the Advancement of Science. g–i) Downscaling of the SWCNT channel length \( L_{\text{ch}} \) in SWCNT-FETs. (g) Reproduced with permission. [29] Copyright 2012, American Chemical Society. (h) Reproduced with permission. [30] Copyright 2017, The American Association for the Advancement of Science. (i) Reproduced with permission. [140] Copyright 2010, Springer Nature.

Device resistance of about 11 kΩ, which approaches the quantum limit resistance \( R_Q = 6.45 \) kΩ. When the channel length was further reduced to 9 nm (Figure 6h), the device exhibited a diameter-normalized current density of 2.41 mA μm\(^{-1}\), which was four times more than that of the Si nanowire devices with similar channel length. The contact resistance was extracted to be 6.6 kΩ, suggesting excellent contact properties at the Pd/SWCNT interface. In 2017, Qiu et al. developed a top-gated Pd-contacted SWCNT-FETs with a 5 nm gate length, which delivered a large on-state current of 20 μA and an ultrasmall device resistance of 10 kΩ at a low bias of 0.4 V. [30] By introducing graphene as the S/D electrodes, the 5 nm graphene-contacted device (Figure 6i) maintained the excellent on-state performance with a much smaller SS of 73 mV dec\(^{-1}\), which was attributed to the improved gate efficiency induced by the ultrathin graphene S/D. Although there have been a few pioneering theoretical studies on sub-5 nm gate-length SWCNT-FETs, accurate simulation and comparison with the existing experimental data were highly desirable. Recently, Xu et al. used the first-principles quantum transport approach ( benchmarked with the performance of 5 nm gate length SWCNT-FETs) to investigate the performance limit of sub-5 nm gate-length SWCNT-FETs with a gate-all-around (GAA) device geometry. [144] It was found that the device could be potentially scaled down to 2 nm gate-length and fulfill high-performance with an on-state current of more than 1000 μA μm\(^{-1}\), an intrinsic delay time of 0.02 ps, and an SS of 150 mV dec\(^{-1}\). However, considering the tradeoff between the performance and power consumption, 5 nm gate-length seemed to be the optimum scaled limit.

4.3. State-of-the-Art of SWCNT-TFTs and ICs

While a variety of individual SWCNT-based FETs have been demonstrated with performance preceding Si-based counterparts (with similar gate length) and even toward the theoretical
limits,[30,31] the high-performance and large-scale IC applications require a high current drive capability and a high uniformity of device performance, which are unfeasible to be realized using an arbitrary individual SWCNT as the channel. To develop SWCNT-based high-performance IC electronics, a feasible channel can be constructed with a large number of SWCNTs in order to smooth out the arbitrary chirality, diameter, length, and orientation. SWCNT thin-films in the form of either random network or aligned array have been extensively studied and utilized to build TFTs and ICs. As-grown SWCNTs contain both semiconducting and metallic tubes and how to get rid of metallic ones is a challenge as the processes removing these metallic tubes unavoidably give rise to creation of defects in semiconducting tubes. To reduce the short-circuit caused by metallic tubes across the S and D electrodes, the network-channel length must be designed to be much larger than the average length of the SWCNTs. As a result, the tube–tube junctions and the defects in the network-channel could severely affect the device performance, leading to a low carrier mobility and poor on-state performance. The resulting ICs typically had an operating speed less than 1 MHz,[41,48] much less than that (approximately GHz) of conventional Si-based ICs. Recently, the semiconducting purity of solution-processed SWCNTs has been remarkably increased up to 99.99% through several dispersion and purification technologies.[59,68,72,73] Availability of a highly pure solution-processed SWCNTs network makes high-performance scalable SWCNT ICs feasible.[147,148] Thanks to the development of alignment techniques, such as dose-controlled floating evaporative self-assembly (DFES),[75] dimension-limited self-assembly (DLSA),[58] DNA-assisted assembly,[149] and Langmuir–Blodgett (LB)[76,77] or Langmuir–Schaefer (LS)[78] method, a channel packed with a well-aligned SWCNT array with a density of more than ≈100 tubes μm−1, a semiconducting purity of larger than 99.99%, and a relatively narrow distribution of the tube diameters could be utilized for high-performance SWCNT-based ICs.[57]

As an important application, TFT has become the building block for back-panel drive circuit of flat-panel display technology. SWCNT-TFTs drive circuits for active-matrix (AM) organic light-emitting diode (OLED) have been successfully demonstrated. In 2011, Zhang et al. reported a sorted s-SWCNT-TFTs drive circuit for an AMOLED display with 500 pixels (Figure 7a).[44] 348 out of 500 pixels can be turned on with a yield of ≈70%. In 2013, Zou et al. demonstrated, for the first time, static and dynamic AMOLED display driven by CVD-grown SWCNT-TFTs drive circuit (Figure 7b).[45] The highly uniform TFTs performance ensured an excellent control capability of the drive circuit.

In addition to the drive circuits for flat-panel displays, SWCNT-TFTs have also been extensively used to construct digital ICs. Due to the lack of effective and stable approaches to fabricate n-type SWCNT-TFTs, the early demonstrated SWCNT-based ICs were constructed only with p-type SWCNTs network-channel.[143,48,130] In 2013, Gao et al. successfully fabricated p- and n-type TFTs (Figure 7c) based on CVD-grown SWCNTs network film using coating Al2O3 and Si3N4 thin layer on the channels, respectively.[49] Both the p- and n-type TFTs had comparable on- and off-state performances, and the constructed CMOS ICs demonstrated logic functionalities. In 2017, Yang et al. demonstrated solution-processed high purity (>99.9%) s-SWCNTs complementary TFTs (Figure 7d)[44] using a doping-free technology[26] in which Pd and Sc were used as the S/D electrodes to selectively inject holes and electrons into the channels to achieve p- and n-type TFTs, respectively. The fabricated complementary TFTs (with a gate length of 1 μm) exhibited highly symmetrical electrical characteristics with significant improvement in the on-state performance. A medium-scale IC, 4-bit full adders containing 132 complementary TFTs, were realized and functioned well with 100% yield.

Although SWCNT-TFT technologies have developed for more than a decade, only very basic logic circuits have been demonstrated. In 2013, the first CNT computer (Figure 7e) was successfully demonstrated using 178 SWCNT-TFTs.[151] More than 99.99% of the metallic tubes in the CVD-grown aligned SWCNTs array were removed by electrical burn-off process. The CNT computer can execute multiple programs synchronously. As a major advance for very-large-scale SWCNT-based integrated system, a 16-bit microprocessor (RV16X-NANO) (Figure 7f) consisting of more than 14 000 CMOS SWCNT-TFTs was developed by MIT in 2019.[146] Solution-sorted s-SWCNTs (99.99% purity) network was used in the microprocessor, and optimized processing and circuit design techniques were employed to overcome the inherent SWCNT problems, such as metallic tubes and tube-bundles. This 16-bit microprocessor could execute standard 32-bit instructions on 16-bit data and addresses.

As discussed above, SWCNT-TFTs with ultrashort channels are contact dominated with the quasi-ballistic transport mechanism and different from that of junction-dominated long-channel SWCNT-TFTs. The operation speed of SWCNT-based ICs has been significantly promoted with downscaling of the channel length into the sub-micrometer range.[147,152–154] In 2017, Han et al. reported a five-stage CMOS ring oscillator (RO) constructed by solution-processed, self-assembled s-SWCNTs (purity >99.9%) array TFTs with channel length of 100 nm (Figure 7g).[147] The RO circuit had an oscillation frequency of 282 MHz and a corresponding sub-nanosecond stage delay of 35 ps at VDD of 1.9 V. A remarkable leap in the operation speed (up to GHz regime) of SWCNT-based ICs was achieved by Zhong et al. in 2018.[152] They fabricated top-gated p-type devices using solution-processed s-SWCNTs (purity >99.99%) network film. Their devices were optimized with a 120 nm thick gate metal to suppress the gate series resistance and 70 nm air gaps between the G and S/D contacts to reduce the parasitic capacitances (Figure 7h). The constructed five-stage RO with a gate length of 115 nm yielded an oscillation frequency up to 5.54 GHz with an average gate delay of 18 ps, which was comparable to that of Si CMOS ICs with a gate length of 130 nm.[155]

Although ballistic transport has been realized in the FETs containing an individual SWCNT in the channel, it is difficult to achieve ballistic transport in a SWCNTs-network-film channel even when the channel length is scaled down to the sub-micrometer scale as the intertube junctions and random tube orientations in the network greatly deteriorate carrier mobility and on-state conductance. In comparison, a well-aligned s-SWCNT array can be an ideal ballistic-transport channel material if excellent SWCNT alignment, high packing density, and high semiconducting purity can be obtained. In 2016, Brady et al. reported quasi-ballistic transport in a solution-processed aligned s-SWCNTs (purity >99.98%) array (Figure 7j).[148] A “rinsed and annealed” post-treatment process and an optimized tube density (47 tubes μm−1) were adopted to improve the contact properties and...
reduce the electrostatic screening effect arising from intertube interactions, leading to an excellent on-state performance with the conductance as high as 0.46\textit{G}_\text{0} per tube, nearly seven times higher than that of previously reported SWCNTs-array-based devices. The saturated on-state current density (392 \mu A \mu m^{-1}) of the device (\textit{L}_\text{ch} = 140 \text{ nm}) was 1.9-fold higher than that of a 90 nm node Si MOSFET. Recently, a significant breakthrough in producing aligned s-SWCNTs array has been achieved by Liu et al.\cite{58} They developed a multiple-dispersion sorting process and DLSA method to successfully assemble aligned s-SWCNTs
array with extremely high purity (≈99.9999%), adjustable tube-pitch (5–10 nm), narrow diameter distribution (≈1.5 nm), and full wafer coverage (4 in.). A top-gated SWCNT-array TFT with an optimal tube density of 120 tubes µm−1 in the channel (Figure 7j) exhibited an on-state current density of 1.3 mA µm−1 and a peak transconductance of 0.9 mS µm−1 at VDS = 1 V. Both values were higher than that of Si-based MOSFETs with a similar gate length (≈100 nm). In addition, a five-stage RO circuit constructed by the SWCNT-array TFTs was able to work at an oscillation frequency of 8.06 GHz under VDD = 2.6 V. However, due to the large interface trapped charge density (≈1012 cm−2),[161] the SS of the device is only 190 mV dec−1, much below the requirement (<100 mV dec−1) for digital ICs.

In addition, the excellent electronic and mechanical properties have made SWCNT thin-films especially suitable for flexible and stretchable electronics. There have already been lots of demonstrations on SWCNT thin-film-based flexible/stretchable electronic devices.[41,48,157–164] Using high-purity s-SWCNTs solution, Wang et al. fabricated SWCNT-TFTs and fundamental logic gates on an ultrathin polyimide substrate (Figure 7k).[157] The flexible SWCNT-TFTs with channel length of 4 µm exhibited highly uniform device performance with on-state current and transconductance up to 15 µA µm−1 and 4 µS µm−1, respectively. Additionally, such highly flexible devices and logic gates exhibited excellent stability even after 1000 bending cycles. High-performance flexible TFTs and ICs have also been demonstrated using CVD-grown SWCNT networks. Cao et al. adopted stripe-patterning to reduce the percolating metallic pathways in the SWCNT networks.[41] The fabricated transistors showed ION/IOFF as high as 105 and carrier mobility of 80 cm2 V−1 s−1. A 4-bit row decoder circuit (Figure 7l) consisting of 88 transistors was further demonstrated on a plastic substrate. By controlling the percolation threshold density of the SWCNT networks, Sun et al. fabricated TFTs and ICs on flexible and transparent substrates (Figure 7m) with high ION/IOFF of 106 and field-effect mobility of 35 cm2 V−1 s−1, respectively.[48] Because of the large length/diameter ratio, SWCNTs are naturally highly curved and entangled in their thin-film form, making them promising materials for stretchable electronics.[165,166] Chae et al. reported a highly stretchable TFT (Figure 7n) with graphene electrodes, SWCNT network channel, and a geometrically wrinkled Al2O3 dielectric layer.[165] The randomly distributed wrinkles imparted the Al2O3 layer a certain degree of stretchability. The resulting devices retained performance after stretching and releasing for over 1000 cycles under a tensile strain up to 20%. Using intrinsically stretchable dielectric materials such as ion gel, Xu et al. fabricated stretchable SWCNT-TFTs (Figure 7o) that could be stretched up to 50%.[162] There was no appreciable degradation in the device performance after repeated mechanical cycling. Table 2 summarizes the device structures and performances of the state-of-the-art SWCNT-FETs/TFTs.

### Table 2. Device structures and performances of state-of-the-art SWCNT-FETs/TFTs. (BG: back-gated; TG: top-gated; G0: conductance quantum (2e2/h)).

| Refs. | Device structure | Channel | S/D | Gate dielectric | Channel length [nm] | ION [mA µm−1] | ION/IOFF | G0 (μS) | SS [mV dec−1] | gmn |
|-------|------------------|---------|-----|-----------------|---------------------|---------------|-----------|--------|----------------|------|
| [13]  | BG Single tube   | Pd      | 500 nm SiO2 | 300         | 7       | 106       | 0.8G0     | 170    |                  |      |
| [26]  | BG Single tube   | Sc      | 100 nm SiO2 | 300         | 10      | 106       | 0.98G0    | 250    |                  |      |
| [24]  | TG Single tube   | Sc      | 15 nm HFO2  | 120         | 5       | 104       | 0.64G0    | 100    | 25 μS per tube  |      |
| [143] | BG Single tube   | Y       | 500 nm SiO2 | 400         | 12      | 105       | 1.1G0     | 400    |                  |      |
| [39]  | BG Single tube   | Mo      | 20 nm SiN4  | 60          | 9       | 107       | 100       |        |                  |      |
| [1]   | TG Single tube   | Co–Mo   | 5 nm Al2O3  | 11          | 0.9     | 104       | 85        |        |                  |      |
| [140] | BG Single tube   | Pd      | 10 nm HFO2  | 15          | 105     | 0.7G0     | 85        | 40 μS per tube  |      |
| [29]  | BG Single tube   | Pd      | 3 nm HFO2   | 9           | 2.41    | 104       | 94        | 55 μS per tube  |      |
| [30]  | TG Single tube   | Pd      | 3.5 nm HFO2 | 5           | 15      | 106       | 0.64G0    | 105–130|                  |      |
| [54]  | TG Network       | Pd/Sc   | 18 nm HFO2  | 1000        | 0.015   | 106       | 73–82     | 20 μS µm−1 |                  |      |
| [157] | BG Network       | Pd      | 20 nm Al2O3 | 4000        | 0.015   | 106       | 400       | 4 μS µm−1  |                  |      |
| [147] | BG Network       | Pd/Sc   | 4 nm Al2O3  | 100         | 105     |           |           |        |                  |      |
| [152] | TG Network       | Pd      | 7.5 nm HFO2 | 120         | 0.35    | 105       | 160       | 460 μS µm−1 |                  |      |
| [154] | TG Array         | Pd      | 5 nm HFO2   | 95          | 1.92    |           | 1400 μS µm−1 |        |                  |      |
| [148] | BG Array         | Pd      | 15 nm SiO2  | 140         | 0.392   | 104       | 0.46G0 per tube | 100 μS µm−1 |                  |      |
| [58]  | TG Array         | Pd      | 7.3 nm HFO2 | 120         | 1.3     | 105       | 190       | 900 μS µm−1 |                  |      |
restrict the low-power electronic applications of SWCNT-FETs/TFTs. Therefore, two main strategies for suppression of the power consumption (Figure 8) have been attempted. One is to reduce the SS. As discussed in Section 3.3, a small SS implies a large downscaling range of the supply voltage $V_{DD}$, resulting in reduction in the device power consumption. To achieve this goal, many efforts have been devoted to enhancing gate control efficiency and exploring new carrier injection mechanisms (e.g., BTB tunneling[132,169] and Dirac source injection[133,134]). The other strategy is to suppress off-state leakage current. Several device structures that can inhibit ambipolar behavior and off-state leakage current have been proposed and implemented.[105–111] In addition, the devices and ICs working in deep-subthreshold region with small current have also been reported.[170] In this section, these two strategies will be discussed in detail.

### 5.1. Effective Reduction of SS

From discussion on expression of SS in Section 3.3, lowering the interface trapped charge density (i.e., reducing $C_{it}$) and enhancing the gate efficiency (i.e., increasing $C_{ox}$) are the most straightforward measures to reduce SS toward its room temperature limit, $\approx 60$ mV dec$^{-1}$ governed by the Boltzmann thermal equilibrium distribution. The density of trapped charges and adsorbates on the gate dielectric layer could be reduced through a dehydration reaction occurred in a hexamethyldisilazane (HMDS) vapor prime process, leading to a small SS of 62 mV dec$^{-1}$ and an average lowest static power consumption of $\approx 10$ pW in a SWCNT-TFT-based inverter.[163] However, in solution-processed SWCNTs, the surfactant/polymer residues around the SWCNTs usually induce high interface trapped charge density up to $10^{12}$ cm$^{-2}$.[156] which are hardly removed using simple rinsing and annealing processes.[38]

Since the thickness of gate dielectric is of great importance in determining gate capacitance and gate control efficiency (see Section 3.3), the exploration of the downscaling behavior and the scaling limit of the gate dielectric thickness could provide a benchmark for selection of dielectric materials and their thickness. Reducing gate dielectric thickness and engaging high-$k$ dielectric materials have been evidenced to be efficient for reduction of the SS.[171] Their devices exhibited a clear trend of the SS decreasing with downscaling of $t_{ox}$ (Figure 9a). When $t_{ox}$ was decreased to 7.3 nm, the average SS approached 62 mV dec$^{-1}$. Unfortunately, the gate leakage current was found to increase apparently when $t_{ox}$ was less than 6.8 nm. As a result, optimization of $t_{ox}$ should be based on a trade-off between a large leakage current and a small SS, between 7 and 10 nm for a HfO$_2$ gate dielectric layer. In addition, the SS was found to be increased with downscaling of the channel length (Figure 9b). When the channel length is scaled down to deep-sub-micrometer, the most of SWCNTs in the channel could bridge the S and D directly. The fluctuations in SWCNTs orientations and diameters inevitably cause variation in $V_{TH}$ of these tubes.[171,172] As a result, all these individual tubes could not concurrently switch off, incurring a poor SS.

To achieve an SS less than the room temperature limit, $\approx 60$ mV dec$^{-1}$, and also maintain a large on/off current ratio ($I_{ON}/I_{OFF} \geq 10^4$) require a completely different carrier injection mechanism, in which the Boltzmann thermal distribution dominated injection is no more a dominant carrier injection mechanism. BTB tunneling[173,174] dominated injection has been found to be capable of an SS of $\approx 40$ mV dec$^{-1}$ at room temperature in an individual SWCNT-FET (Figure 10a).[132] A Si back-gate was employed to adjust the electrostatic potential of the nanotube channel close to the Fermi level of the S and D, while an Al gate could control the potential of the middle part of the nanotube channel creating a p–n–p band structure. The device exhibited two conduction branches (Figure 10b). The “A” branch corresponds to thermionic emission dominated hole injection (see the energy band diagram for the “A” branch in Figure 10b) with an SS ($\approx 65$ mV dec$^{-1}$) close to the limit at room temperature. Interestingly, the “B” branch presents an SS of $\approx 40$ mV dec$^{-1}$, which can be attributed to the bandpass-filter-like BTB tunneling. The tunneling occurs in the gate voltage window determined by the difference between the valence band near the source and the conduction band in the middle part of the channel (see the energy band diagram for the “B” branch in Figure 10b). The high-energy

**Figure 8.** Two main strategies for suppression of the power consumption of SWCNT-FETs/TFTs: decrease of the SS and reduction of the off-state leakage current.
Figure 9. Downscaling behavior of self-aligned top-gated SWCNTs-network-TFTs. a) Schematic device structure and downscaling behavior (statistical SS distribution as a function of $t_{ox}$) of the devices with a channel length of 5 $\mu$m at $V_{DS} = -0.1$ V. b) Lateral downscaling behavior (statistical SS distribution as a function of channel length) of the devices with $t_{ox} = 7.3$ nm at $V_{DS} = -0.1$ V. Reproduced with permission. [171] Copyright 2018, AIP Publishing.

Figure 10. BTB tunneling in an individual SWCNT-FET. a) SEM image and schematic cross-sectional structure of a BTB tunneling SWCNT-FET. b) Transfer characteristics of the device at $V_{DS} = -0.5$ V and $V_{gs-Si} = -3$ V, and the corresponding energy band diagrams (in the lower panel) of the device for the “A” and “B” branches of the transfer characteristics, respectively. Reproduced with permission. [132] Copyright 2004, American Physical Society.

tail of the holes injected from the source is cut off, resulting in a “cold” electronic system.\textsuperscript{[123,175]} The device is analogous to a conventional MOSFET operating at a temperature below 300 K, but enabling an SS of less than 60 mV dec$^{-1}$. Occurrence of the BTB tunneling in SWCNT-FETs benefits from the ultrathin tunneling barrier that originates from the 1D nature of the nanotube channel and the excellent gate coupling.\textsuperscript{[119,132]}

In addition to the BTB tunneling devices, a novel steep-slope device, called DS-FET (Figure 11a), was proposed by Qiu et al. in 2018.\textsuperscript{[133]} An individual s-SWCNT channel was contacted to the n-doped graphene source and Pd-drain electrode. An ultrathin Y$_2$O$_3$ gate dielectric layer (equivalent oxide thickness (EOT) of 1.5 nm) provided strong gate coupling to the SWCNT channel. The DS-SWCNT-FET could function as an energy-efficient electronic switch with an SS of 35 mV dec$^{-1}$ at room temperature, a large $I_{ON}/I_{OFF} \geq 10^6$, and a high $I_{ON}$ of 6.5 $\mu$A at $V_{DS} = -0.5$ V. It is well known that in an ordinary Si-based MOSFET, the DOS in the conduction band increases with energy, and the electron density $n(E)$ subexponentially decays toward higher energy due to the Fermi distribution function (Figure 11b). In sharp contrast,
graphene is of a linear energy dispersion near the Dirac points, which causes superexponentially decaying of electron density toward the Dirac points (Figure 11c), leading to a more localized electron density distribution around the Fermi energy $E_F$ (blue curve in Figure 11d). The SS in a DS-FET can be expressed as

$$ SS = \frac{1}{\xi} \left(1 - \frac{k_B T}{E_{\text{Dirac}} - \Phi_B}\right) \frac{k_B T}{e} \ln 10 \quad (7) $$

where $\Phi_B$ is the SB height at the off-state; $E_{\text{Dirac}}$ is the energy of the Dirac point; $\xi = -d\Phi_B/d(eV_{GS}) \leq 1$ is the gate efficiency that describes the sensitivity of the SB lowering to $V_{GS}$. In a DS-FET with the condition of $E_{\text{Dirac}} - \Phi_B > nk_B T$, the SS could be smaller than $(k_B T/e) \ln 10 \approx 60$ mV dec$^{-1}$ at room temperature. The source acts as a “cold source” for the electronic system without a high energy tail of electron density distribution. Therefore, at the off-state of the DS-FET, the thermally activated electron density with energy over the SB decreases superexponentially with decreasing $V_{CS}$, resulting in a steeper SS compared with that in a conventional MOSFET (Figure 11e).

5.2. Suppression of Off-State Leakage Current

SWCNT-FETs typically suffer from a large off-state leakage current, $I_{\text{OFF}}$, because of the small bandgaps (0.3–0.6 eV) of SWCNTs.$^{[15,24,113]}$ In this case, a high $I_{\text{OFF}}$ is caused by carrier tunneling through the thin potential barrier formed by the small bandgap at the drain contact, in particular under a high gate control efficiency. The poor off-state properties would inevitably lead to a significant increase in the static power consumption of SWCNT-based ICs. In conventional Si MOSFETs, introducing a lightly doped region between the heavily doped drain region and the channel has been proven to be able to effectively suppress $I_{\text{OFF}}^{[176,177]}$. However, due to the lack of simple and efficient doping methods for SWCNTs, the $I_{\text{OFF}}$ of SWCNT-FETs is not easily suppressed.
Recently, several kinds of asymmetric device configurations (e.g., partial-gate and dual-gate structures) have been reported to effectively suppress ambipolarity and \( I_{OFF} \) in SWCNT-FETs/TFTs.\(^{105-110}\) In the common asymmetric single-gate structure (Figure 12a\(^{110}\) and Figure 12b,\(^{105}\) a similar design also shown in Figure 3b), a trench or a gap between the gate and the drain electrode is introduced. In consequence, the gate has a less impact on the energy band near the drain contact so that a thick barrier forms near the drain contact at the off-state (see Figure 3e) to efficiently suppress the electron tunneling current (\( I_{OFF} \)) even at a high \( V_{DS} \).

In addition to asymmetric single-gate structures, specially designed dual-gate structures have also been adopted to reduce \( I_{OFF} \). Qiu et al. fabricated a dual-gate FET (Figure 12c) based on a single SWCNT channel,\(^{106}\) where the main-gate (Gate1, overlapped with the source) covers most of the channel and controls the electrostatic potential, and the extra-gate (Gate2, overlapped with the drain) directly connects to the drain electrode and makes the drain contact region extend into the channel (similar to the structure shown in Figure 3c). In this design, Gate2 does not function as an ordinary gate. Instead, it actually extends the drain potential, shielding the electrical potential from Gate1 away from the SWCNT/drain contact. A result, a thick potential barrier near the drain can be obtained for remarkable suppression of \( I_{OFF} \). In 2019, Liu et al. adopted the dual-gate structure in a SWCNT-TFTs with a channel length of 375 nm (Figure 12d).\(^{110}\) Compared to a self-aligned symmetric single-gate device, the dual-gate device exhibited a significantly suppressed \( I_{OFF} \) by 2 orders of magnitude. Recently, Zhao et al. reported CMOS SWCNT-TFTs with a dual-gate structure (Figure 12e),\(^{109}\) but different configuration from that in Figure 12d. In addition to the main-gate overlapped with the source, an assistant gate was introduced and overlapped with the drain contact. The assistant gates in p- and n-type TFTs were biased to the ground and \( V_{DD} \), respectively, to maintain a thick barrier at the drain contact and suppress the carrier tunneling at the off-state. The SWCNT CMOS logic gates constructed using the dual-gate devices demonstrated suppressed static power dissipation by 3 orders of magnitude compared to the SWCNT CMOS circuits built on symmetric single-gate devices.

Exploring the capability of FETs/TFTs in the deep-subthreshold regime (i.e., near the off-state) is an effective approach to realization of ultralow-power electronics because of low subthreshold current and steep SS. Oxide semiconductor FETs\(^{179}\) as well as organic semiconductor FETs\(^{179-181}\) have been shown excellent deep-subthreshold characteristics with a power less than 1 nW. Very recently, Portilla et al. have reported deep-subthreshold SWCNT-TFTs and ICs\(^{179}\) whose static power consumption was only 1 pW at a supply voltage of 0.2 V. A self-assembled monolayer (SAM) was incorporated together with an ultrathin (\( \approx 3 \) nm) AlO\(_x\) layer to form a high quality hybrid AlO\(_x\)/SAM gate dielectric. The resultant flat-band voltage was in favor of a well-balanced ambipolar conductance in the deep-subthreshold regime, leading to ultralow-power consumption of their SWCNT-based ICs. In addition, Zou et al. recently fabricated SB-contacted SWCNT-TFTs that were operated in the subthreshold region.\(^{182}\) A thin high-\( k \) gate dielectric and asymmetric gate configuration enabled highly efficient gate modulation of the SB at the source contact, resulting in excellent subthreshold switching characteristics with small SS (\( \approx 67 \) mV dec\(^{-1}\)), large current on/off ratio (\( \approx 10^6\)), and low off-state current (\( \approx 0.5 \) pA). The p-channel metal–oxide–semiconductor (PMOS) inverter built with the subthreshold SB-SWCNT-TFTs presented
almost rail-to-rail outputs with ultralow power consumption less than 1 pW under a small supply voltage of 0.2 V.

6. Outlook

Over the past two decades, remarkable achievements have been made in both fundamental research and applications of SWCNT-based electronics. SWCNT thin-films have become highly promising for unique electronic applications, including flexible electronics, large-scale ICs, and sensors. It has been theoretically predicted that computers based on SWCNT-FETs/TFTs can provide a power-performance improvement of ten times over computers based on Si-CMOS technology.[16] Compared to the TFTs based on other semiconductors, like amorphous silicon, polysilicon, and organic semiconductors, SWCNT-TFTs offer significantly better performance. SWCNT-FETs/TFTs and ICs have been demonstrated with comparable or even supercharacteristics in comparison of conventional Si-based counterparts with similar gate lengths.[10,54,58,152] All these advancements have revealed a great potential of SWCNTs for future electronic applications in the more Moore era. To that destination, several key challenges must be overcome before commercialization of SWCNT-based electronics comes into reality.

From the perspective of large-scale ICs fabrication, SWCNTs should be well aligned with a density of 100–200 tubes μm\(^{-1}\) in the wafer scale. High semiconducting purity (>99.99%) and a narrow chirality distribution are required to guarantee a high uniformity of SWCNT-based devices and ICs. Recent advances in SWCNTs dispersion, sorting, and self-assembly alignment have made SWCNTs toward the requirements. Recently, 200 mm wafer-scale uniformity and reproducibility of SWCNT-TFTs fabricated using commercial Si manufacturing facilities have been achieved.[80] Along the development, efforts are still required to mitigate the effects of defects, interface trapped charges, and polymer residues around the SWCNTs.

In addition, the SWCNT-based device design and fabrication processes are still far from mature compared to that of modern Si-based electronics. New device structures and fabrication techniques are to be explored to reduce the parasitic capacitance between the G and the S/D and the contact resistance between the SWCNTs channel and the S/D in order to raise the operating speed and reduce the power consumption of the SWCNT-based devices and ICs.

SWCNTs, with a dangling-bond-free quasi-1D carbon sp\(^2\) atomic architecture, are of a unique distribution of electronic states, which is distinct from other semiconductors. Novel device designs as well as the electrode materials are required to reduce the contact resistance between SWCNTs and S/D pads, mitigate the impact of the small bandgap on the electron transport in the deep-subthreshold regime, and enhance the gate control efficiency. Compared to the common planar packaging technology adopted in SWCNT-FETs/TFTs and ICs at present, 3D integrated SWCNT-based ICs using multilayer interconnects could further boost the device operation speed and cut down the device operation power.[183]

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

carbon nanotubes, electronic devices, field-effect transistors, integrated circuits, low-power, subthreshold swing

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