Research and Design of DDS Low Frequency Signal Generator Based on FPGA

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ABSTRACT

Signal generator is the most widely used basic instrument in the field of electronic technology. The research and development of DDS low frequency signal generator based on FPGA has certain practical significance. With the core of EP2C8Q208C8N and the necessary peripheral analog circuit, a low frequency signal generator based on direct digital frequency synthesis technology is designed and its output performance is tested under the control of Verilog program.

KEYWORDS

Signal generator, FPGA, DDS, Verilog.

INTRODUCTION

In 1971, American scholar J. Tierney et al. “A Digital Frequency Synthesizer” academic paper first proposed a new principle of frequency synthesis based on all-digital technology to directly synthesize required waveforms from the concept of phase[1]. Due to the limitation of technology and device level at that time, its performance bidding cannot be compared with the existing technology, so it has not received enough attention. In recent years, with the rapid development of electronic technology, direct digital frequency synthesizer (DDS or DDFS) has been developed rapidly. It has become the best one in modern frequency synthesis technology because of its superior performance and characteristics different from other frequency synthesis methods.

The main advantages of DDS[2]are: (1) the frequency resolution of the output signal can be very high. Moreover, the number of frequency points of the output signal can be very large, which can be approximately regarded as the frequency of the output signal is continuously adjustable. (2) Fast frequency conversion. (3) Continuous phase. (4) Signal coherence. (5) Low phase noise. (6) Complex signal modulation is easy to implement. DDS system can realize linear frequency modulation, FSK/PSK/GMSK modulation conveniently. (7) Microprocessor interface, easy to control, stable and reliable. (8) Large-scale integration, small size, low power consumption, light weight.

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At the same time, it is more flexible to design DDS circuits with FPGA than with special DDS chips. Because any waveform can be generated by changing the data in ROM, it has considerable flexibility. FPGA chips also support on-line upgrade, embedding DDS design into the system composed of FPGA chips, and using pipeline technology, the system cost will not increase much, and the price of purchasing dedicated chips is many times that of the former. Therefore, using FPGA to design DDS system has a high performance-price ratio.

At the beginning of the advent of DDS, the speed limitation of components and the noise caused by digitization hindered the development and practical application of DDS. In recent years, with the development of ultra-high speed digital circuits and in-depth study of DDS, the highest operating frequency and noise performance of DDS have approached and reached the level of phase-locked frequency synthesizer. With the development of this frequency synthesis technology, it has been widely used in communication, navigation, radar, remote control and telemetry, electronic countermeasures and modern instrument industry.

![Figure 1. Structural diagram of commonly used programmable DDS.](image)

The structure of the commonly used programmable DDS is shown in Figure 1.

The core of the DDS system is the phase accumulator, which consists of two adders $\Sigma$ and a N-bit phase register. N is generally 24-32 bits. For each clock $f_c$, the phase register increases with step M. The output of the phase register is added to the phase control word and then input to the address of the sinusoidal query table. The sinusoidal query table contains the digital amplitude information of a periodic sinusoidal wave, and each address corresponds to a phase point in the range of 0-2\(\pi\). The sinusoidal query table maps the input address phase information into sinusoidal wave amplitude signal, drives DAC and outputs analog signals. M* N / 2 $f_c$ clocks return to the original starting state, and the corresponding sinusoidal query table also returns to the original starting position through a cycle. The whole DDS circuit system can output a sine wave.

DDS is an all-digital circuit system, one of its drawbacks is that it has too much stray, which is one of the main reasons why DDS technology has not been applied in practice for a long time. After analysis, the bigger the value of the bit N of the phase register, the smaller the output waveform error sequence of DDS, and the smaller the spurious signal caused by the waveform error sequence. If the value of N is large enough, the spurious signal caused by the waveform error sequence can be effectively suppressed. In addition, the spurious power of DDS...
results from the combination of phase truncation error and amplitude quantization error. If the output signal of phase accumulator contains more digits \( A \) and \( D \) for waveform memory addressing and DAC, the total spurious power (caused by phase truncation error and amplitude quantization error) will be smaller. The value of \( A \) is usually equal to \( D+2 \), or slightly larger than \( D+2 \), which is a basis for the design of DDS. The control frequency word \( K \) should be mutually prime with \( 2^N \), which can improve spurious 3.9 db. That is to say, \( K \) equals odd numbers. In addition, DAC with good performance should be selected to reduce the influence of DAC nonlinearity.

At present, there are three ways to implement DDS with FPGA[3]: the implementation method based on IIR filter, the implementation method based on LUT and the implementation method based on CORDIC algorithm. Among them, the LUT method is more general, and it is the mainstream way in the design of the FPGA. This is because there are plenty of LUT resources in the chip of the FPGA. A frequency/phase/amplitude programmable DDS structure is shown in Figure 2.

The reference signal is a highly stable crystal oscillator, whose output provides synchronous signals for all parts of DDS: the phase accumulator is the core of DDS, which consists of a binary adder of N-bit word length and a N-bit register sampled by clock \( f_c \). The function of the reference signal is to accumulate the frequency control word \( K \) linearly; the waveform memory stores a function waveform query table, which does not correspond to it. A series of discrete amplitude codes are obtained by addressing the waveform memory with the same phase sequence. After D/A conversion, the corresponding step wave can be obtained. Finally, the required analog waveform can be obtained by smoothing the low-pass filter.

The phase parameters of the output signal can be controlled by changing the phase control word \( P \). When the word length of the phase adder is \( M \), the input of the waveform memory is the sum of the output of the phase accumulator and the output of the phase control word \( P \) when the phase control word is changed from 0 to \( P \). Therefore, the amplitude-coded phase of the output will be increased and the final output analog signal will be phase-shifted. The minimum step \( P_{\text{min}} \) of phase shift mainly depends on the word length of the phase adder, and the minimum phase shift resolution \( \Delta P_{\text{min}} \) depends on the word length \( N \) of the phase accumulator. The amplitude of DDS output signal can be achieved by inserting a digital multiplier after the waveform memory. The amplitude control word \( A \) weights the output amplitude coding of the waveform memory. From the above analysis, we can know that when the word length of DDS phase accumulator and
phase adder is fixed, the frequency, phase and amplitude of DDS output analog signal can be effectively controlled by changing K, P and A. DDS is an open-loop system with full digital structure and no feedback link, so it is very fast, generally in ns order.

DEVICE SELECTION AND SYSTEM BLOCK DIAGRAM

The frequency range of this design is 1Hz-5MHz, and the frequency accuracy is Hz. The voltage range (peak value) of the signal source is 0.2V-5V, and the voltage precision is 0.1V. The signal types are sinusoidal wave, square wave and triangular wave.

FPGA CORE

The EP2C8Q208C8N of Cyclone II device of Altera company is used in the FPGA. It contains 8256 logic units and 18 18*18 multipliers[4], which are enough for design. With the peripheral circuit of the FPGA, the hardware devices such as digital frequency synthesizer (DDS), memory and I/O interface are centralized on one piece of the FPGA by top-down method, which is conducive to the direct digital frequency synthesizer technology to generate the required waveforms. The realization of different frequencies and amplitudes is solved by state machine control. The data from ROM of the sinusoidal table in the chip is transmitted through the digital multiplier THS5651. The digital-to-analog conversion is completed. The signal amplitude is controlled by controlling the multiplication coefficient of the multiplier. Then the output is connected to the input of the oscilloscope to observe the designed waveform. The main clock frequency $f = 50$ MHz provided by the development board. Because each module needs different clock signals, the clock requirement of keys and control circuits is not high, 10 kHz is enough, while the accumulator, query table ROM module and DA driver need up to 100 MHz clock. So the PLL unit of Quartus II software is called here to generate 100 MHz and 20 MHz frequencies, and a distributor is used to make 20 MHz time. The clock frequency is divided into 10 kHz, so that the clock frequency required by each module of the system has been generated. The system block diagram is shown in Figure 3.
CHOICE OF DAC

The quality of DAC directly affects the spurious components in the output signal of DDS system, so we should pay enough attention to it. Considering ease of use, adequacy and cost, 10 bit DACTTHS 5651 is selected. THS5651 is a high-speed and low-power COMS digital-analog converter with fast speed, the fastest update rate up to 100 MSPS, and excellent performance. THS5651 operates under 4.5 V to 5.5 V power supply. The low power consumption of its internal 175mW ensures that the device is well suited for portable and low power applications[5]. THS5651 latches DATA at the rising edge of CLK, and the converted analog signal is output at the next clock.

DESIGN OF THE CORE OF FPGA

DESIGN OF SYSTEM CONTROL MODULE

The main components of the system control module are phase accumulator, amplitude control circuit, frequency control circuit and waveform selection circuit. The clock frequency of phase accumulator is 100 MHz, and the clock frequency of amplitude control circuit, frequency control circuit and waveform selection circuit is 10 KHz.

The waveform selection circuit is the basis of choosing the three waveforms of sine wave, square wave and triangle wave required by the system, and generating a single pulse every time the key is pressed by the above circuit. So it only needs one button to select one waveform one by one. It can be easily realized by the state machine[6]. The state diagram is shown in Figure 4.
The frequency control circuit mainly adjusts the frequency control word K. If the bit N of the phase accumulator and the clock frequency of the system remain unchanged, the frequency control word M can change the frequency of the output signal. The frequency accuracy of the design target is 1Hz, while the digit N of the phase accumulator is 32 bits, the clock frequency of the system is 100MHz, and the frequency resolution of the output signal is 0.023283064 Hz. It can be concluded that the frequency accuracy of the design target is 1Hz, and the size of the frequency control word should be 43 times. Because the keys are limited and the size of the output signal frequency range is large, there are four sets of output signal frequency gears, namely, 1MHz, 10kMz, 100Hz and 1Hz. One key is used to select the gears and the other two keys are used to adjust the increase or decrease of the frequency. The state diagram is shown in Figure 5.

The function of the amplitude control unit is to adjust the amplitude of the output voltage by changing the control word A and output voltage \( VO = 0-5V \). Two step gears are selected, which are 0.1V and 1V respectively. One key is used to adjust the gears, and the other two keys are used to adjust the increase and decrease of output voltage. The state diagram is shown in Figure 6.

Phase accumulator is the key of DDS system. It consists of a N-bit phase register and a N-bit word-length binary adder. The N value of the phase register is usually 24 to 32 bits. For each clock \( fc \), a step M is added to the phase register. The output of the phase register is added with the phase control word sent by the microcontroller to form the address code of the sinusoidal query table. The sinusoidal query table consists of an amplitude value of a periodic sinusoidal wave, and each address corresponds to a phase point in the range of 0-2\( \pi \) in the sinusoidal wave. The sinusoidal inquiry table outputs the corresponding sinusoidal wave amplitude signal according to the inputted address code inquiry table, and outputs the analog value through DAC conversion. The phase register returns to the original starting state after passing through M*N/2 \( fc \) clocks, and
the corresponding sinusoidal query table returns to the original starting position after a cycle. The whole DDS circuit system can output a sine wave. The frequency of the output signal is \( f_o = \frac{f_c \times K}{2N} \). The frequency of the output signal is determined by the frequency control word. According to Nyquist sampling theorem, \( f_{\text{max}} \leq 0.5 f_c \).

After the frequency control word \( K \) enters the output of the phase accumulator, only the 12-bit address signal enters the LUT. On the premise of frequency accuracy, ROM resources can be saved.

The phase accumulator module is shown in Figure 7 (a).

![Figure 7. Phase accumulator module, frequency operation processing module, digital tube driver module.](image)

**KEYBOARD JITTER ELIMINATION MODULE**

If the jitter is not processed, it will cause logical confusion. The key of jitter elimination is to extract the stable level (which can be low level or high level) of the key signal, and then filter the jitter impulse before and after the stable level. First, in a clock pulse signal time, the key state is scanned and judged. If it is low level, the delay circuit is started. After a set period of time, after the delay is over, the key state is judged three times continuously. If the three judgements are low level, then the key is judged to be in a stable state and a key confirmation signal is output. If in three consecutive judgements, not all of them are low level, it is judged that the button is still in the state of jitter. The key confirmation signal is not output at this time. The state diagram of the key-press jitter elimination circuit is shown in Figure 8.

![Figure 8. State diagram of key-press elimination circuit.](image)

**FREQUENCY DISPLAY MODULE**

Because there is less information to display, the display of voltage and frequency uses a four-bit seven-segment LED digital tube[7].

Frequency display module is mainly composed of frequency control word processing module and four-bit seven-segment digital tube driving module. Because the numerical value of the frequency control word is a multiple of 43, it
is necessary to process the frequency control word and get four segments of the numerical value to send back to the digital tube driver module. Based on the consideration of occupancy, resource saving and comprehensiveness, the arithmetic module is implemented by using the divider IP core of Quartus II and an arithmetic control module. The frequency control word operation processing circuit is shown in Figure 9, and its module is shown in Figure 7 (b). Digital tube driver is to convert the value of each segment to 8 bit, and display it by dynamic scanning mode. As long as the refresh rate is greater than 48Hz, according to the visual retention effect of the human eye, people feel that the data on the digital tube is always bright. The driver module of the digital tube is shown in Figure 7 (c).

![Figure 9. Frequency operational processing circuit.](image)

**VOLTAGE AMPLITUDE DISPLAY MODULE**

Because the precision of voltage display is 0.1V and the maximum amplitude is 5V, only two segments of LED digital tube display are needed. By adjusting the output current of DA, the magnitude of the control word can be exactly 10 times of the voltage magnitude, so only one divider can divide the magnitude control word by 10 to get the value of the high and low segments of the digital tube, and then the magnitude of the voltage can be displayed with decimal points after the high position. The module circuit is shown in Figure 10.

![Figure 10. Voltage amplitude display circuit.](image)

**ROM LOOKUP TABLE[8] MODULE**

Altera company provides LPM ROM core on Quartus II. The realization of ROM function is in the integrated optimization stage of FPGA design, compiling LPM ROM core file with Quartus II synthesis. The waveform file is a waveform. MIF file preset by Quartus II. According to the previous analysis, it can be
concluded that for every + 1 address number of waveform memory, spurious will be reduced by 6 db. Take ROM address = 12 bit, output = 10 bit, DAC is 10 bit, corresponding to it. LPM ROM core includes address signal with input port: address [ ]~ROM and output port: output data of q [ ]~ROM.

In order to ensure the smoothness of the output waveform, the normalized amplitude of the output waveform in one period is divided into 1024 points. There are many ways to generate the waveform file. The waveform file designed here is obtained by waveform generation software. The software is simple, convenient and fast, and the corresponding waveform can be obtained only by selecting various parameters in the selection.

**DIGITAL MULTIPLIER MODULE**

Digital multiplier is used to adjust the amplitude of output waveform[9]. Because the waveform amplitude output by LUT corresponds to the maximum value of output signal voltage, the digital multiplier module wants to design a fractional multiplier by multiplying the amplitude of normalized waveform with the amplitude control word and then moving left. The accuracy and error of output amplitude are directly affected by the left shift number. After simulation and experiment, the left shift number is 6, which can achieve the target very well. The circuit diagram of the digital multiplier is shown in Figure 11.

![Figure 11. Digital multiplier circuit.](image)

**DDS SYSTEM SIMULATION**

The simulation results of DDS system are shown in Figure 12.
PERIPHERAL INTERFACE CIRCUIT

The peripheral interface circuit consists of digital-to-analog conversion circuit, display circuit, key circuit and LED indicator circuit. The chip used in the core board of the FPGA is EP2C8Q208C8 + EPCS4. It also has 5V and 3.3V power supply, which can supply power for the key LED indicator board and display board. The key LED indicator circuit is composed of eight keys and 16 LED lights. The display circuit consists of a digital tube and a 74HC245 chip, in which 74HC245 can play the role of converting level and increasing driving capacity. The DAC circuit consists of power supply, THS5651 and THS4001. THS 4001 is a high-speed operational amplifier used to construct LPF. THS 4001 needs dual power supply, so the DAC board has independent power supply. The DAC circuit is shown in Figure 13.

DEBUGGING

The debugging process includes various simulations to verify whether the design objectives have been achieved. Through simulation, problems can be found and corrected in time, so that the design progress can be accelerated, which is conducive to the improvement of reliability.

After that, comprehensive optimization is carried out to see if the required functions can be implemented on the FPGA. Finally, online debugging is carried out, and the generated configuration files are written to the chip for various tests.

The debugging process of this design is mainly based on FPGA + DAC. The waveform, amplitude and frequency of the output signal of the whole system are observed whether the waveform is consistent with the key control and whether...
the waveform is distorted. If there are problems, Quartus II software provides the debugging and observation tool Signal Tap II. Through JTAG port, the internal signals of the FPGA can be observed and located in real time. On-line logical analysis [], the logic errors in the FPGA can be repaired. The key control and display part simulates the waveform simulation files of each part separately, observes whether there are logic errors, if there are, where the errors occur and corrects them. Finally, the core board of the FPGA is connected with the peripheral interface hardware circuit to observe whether the key operation control is normal, the waveform and display are normal in real time, and adjust the output current of the DAC and the circuit parameters of the external op amp until the output waveform meets the requirements.

**PERFORMANCE AND OUTPUT WAVEFORM TESTING**

The output waveforms of the system are sinusoidal wave, square wave and triangular wave, and their frequencies and amplitudes can be adjusted. The test environment is as follows: the output waveform is displayed and observed with PH DS1052E (dual channel 50 MHz 1GSa/s) and GW GOS-1152A (150 MHz 1GSa/s) oscilloscope.

The test results show that the maximum frequency error and amplitude error of the three waveforms are less than 0.12% and 1.2%, respectively. The measured waveforms are shown in Figure 14.

![Output of measured waveform.](image)

**CONCLUSIONS**

Based on the core board of EP2C8Q208C8N, a high cost-effective Cyclone II series of FPGA chips from Altera Company, the logic design of the digital part of DDS has been completed, and the preset targets have been achieved with the help of the related peripheral circuits.

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