Substrate-morphology driven tunable nanoscale artificial synapse

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ABSTRACT

Two-terminal memristive devices are considering as a potential candidate to mimic human brain functionality to enable artificial intelligence. Particularly, two-terminal nanoscale devices are regarded as a promising solution for implementing bio-synapses due to their small dimensions, extremely compact, and low power to operate neuromorphic functions. Here, we demonstrate that the nanoscale charge transport and resistive switching behavior of VO\(_x\) thin film can be tuned by modulating the substrate morphology. Particularly, the device prepared with flat-Si shows totally distinguished behavior in comprising of reactive ion-etched-Si substrates. Interestingly, conductive atomic force microscopy current maps revealed the electric field inhomogeneity due to a change in substrate morphology. A reliable bipolar resistive switching behavior of the corresponding etched devices have been demonstrated. Due to an increase in the etching time of substrate, an increase in active area and decrease in work function was observed. Further, nanoscale synaptic functions were generated from the corresponding devices, showing a strong conduction path at preferential bright spots of the particular devices. Moreover, finite element simulations confirm the modulation in generation of localized current conduction in particular etched devices by applying tip voltages. These findings represent a new way to generate nanoscale artificial synaptic functions.

1. Introduction

Nowadays, the convoluted and unformulated complex problems are driven by traditional “von Neumann” digital computer architecture, which has been demonstrated as advances in deep learning neural networks [1,2]. In von Neumann architecture, instruction and program data are stored as separate memory units, which are not appropriate way to solve complex problems. On the other hand, the human brain, consisting approximately ~ 10\(^{11}\) neurons and ~ 10\(^{15}\) synapses, can parallelly perform
these complex learning, forgetting, thinking, audio/visual recognition, and movement control [3]. In addition, the power consumption of the human brain (~20 W) is about one millionth of the operating speed of supercomputer based on von Neumann architecture (10^7 W) [4,5]. Thus, developing the artificial neural networks to mimic the synaptic functions of the human brain is essential. Therefore, researchers are encouraged to offer alternative ideas to develop smartest electronic and photonic devices for the implementation of brain-inspired synaptic functions [2,6–8].

To date, tremendous efforts have been made to develop emerging synaptic devices including two-terminal (memristors) [9] and three-terminal devices (transistors and memtransistors) [10,11]. Therefore, two-terminal devices are considered as a potential candidate for neuromorphic functions, due to their simple geometry, fast operability, scalability, and higher density [12], which make them ideal for artificial neural networks. However, the current level across a two-terminal resistive switching device can be tuned for utilization in development of next-generation nonvolatile memory devices [13] and brain-inspired nanosized artificial synapse processing [14]. Generally, current–voltage characteristics of the two-terminal device shows a hysteresis loop, which is called as resistive switching, where the current of the active channel switched electrically from low-resistance state to high resistance state. It has been shown that the resistive switching of the devices can be changed by surface treatment of substrates [15]. The reported surface treatment included methods like nitrogen plasma treatment [16], nanoimprint lithography [17], reactive-ion etching [18–21], pulsed plasma polarization [22], and hydrothermal treatments [23,24] have been used for surface treatment and in turn change the resistive switching. However, the role of changing the surface morphology and in turn tuning the artificial synaptic property, particularly at nanoscale, has yet to be reported.

To investigate a nanoscale charge transport, conductive atomic force microscopy (c-AFM) has been used, which is used to obtain an evidence about the topographic changes and simultaneously local electrical conduction at nanoscale [25–27]. Conductive tip used in c-AFM as a top electrode offer the possibility to the precise location of the device even at 10-nm level, which is useful in scaled-down semiconductor devices [28]. Meanwhile, this kind of nanoscale engineering gives a way toward the critical applications of modernized concepts of artificial neuromorphic computing. Recently, such nanoscale synaptic devices have been implemented in advanced neuromorphic applications [15,29]. Normally, surface-treated substrate at different level causes difference in work function of the device [30]. Furthermore, Kelvin probe force microscopy (KPFM) is a non-contact mode that offers the measurement of potential difference between its conduction tip and device surface at high spatial resolution as well as calculate the carrier concentration [31].

Herein, the interesting phenomena that encouraged this study is to show the modulation of resistive switching and nanoscale synaptic behavior caused by surface modulation, generated by reactive-ion etching (RIE) at different levels. The VO_x layer is deposited from V_2O_5 target by radio frequency (RF) sputtering as an oxide channel on the surface treated Si substrate to make a two-terminal device. The X-ray diffraction (XRD) was used to confirm the crystallization and existence of multiphasic VO_x film. Moreover, surface-treated topographies show different nanostructures of the devices at different etching time in AFM images. The nanoscale charge transport by c-AFM indicates the charge transportation is mainly governed by well-defined and localized channels. While surface potential variations of the devices caused by etching are confirmed by KPFM. Additionally, synaptic behavior of the surface-treated devices at nanoscale level also shows modulation of current conduction. Such characteristics of the proposed study open new varieties of design to produce advanced and on-demand nanoscale artificial neuromorphic devices.

2. Experimental section

2.1. Device fabrication

Nanoscale artificial synaptic device was fabricated in a configuration of Au/VO_x/Si, in which Si (001) wafer (thickness = 500 μm) was used as substrate. The substrates were cleansed ultrasonically in acetone, isopropanol, and deionized water separately for 5 min each. Then, it was washed with ethanol and dried with nitrogen gas. After chemically decontaminating, the substrate was annealed at 100°C for 30 min. Moreover, the cleaned wafer was dry-etched by reactive-ion etching (RIE) in SF_6-based plasma environment.

The RIE is a plasma process for etching materials by radio frequency (RF) gas discharges (ions, radicals) in a low-pressure chamber. It is a collaborative process between energetic ion bombardment and chemically active species. On the other hand, several conditions were applied in an attempt to engineer nanostructures of the surface of substrate at required nanoscale level. After all, the working pressure was kept at 150 mTorr with 50 W of power. SF_6 gas pressure was kept fixed at 20 sccm for 30 and 60 s, separately.

Furthermore, VO_x thin films were fabricated by radio-frequency sputtering V_2O_5 (99.99%) target at 600°C on surface-treated Si substrate for 30 min. The base pressure for the deposition was kept to 2 × 10^-6 Torr. Ultrapure (99.999%) Ar gas flow was
introduced inside the chamber with a flow rate of 30 sccm. During the deposition time, 3 mTorr working pressure was maintained while RF power was fixed at 80 W with substrate rotation of 5 rpm to achieve uniformity. The top electrode of Au/Ti was deposited by e-beam evaporation. Herein, the substrate surface-treated devices at without etching, 30 s etching, and 60 s etching time along with multiphasic VOx sputter-deposition are termed as Vpristine, V30, and V60, respectively.

2.2. Device characterization/measurements

The structural characterizations of nanoscale artificial synaptic device were determined by a MiniFlex (Japan) desktop X-Ray diffraction (XRD) technique with Cu Kα radiation in the Bragg-Brentano geometry over diffraction angle of 5–85°. Surface topographic images of the surface treated devices were observed by ex-situ atomic force microscopy (AFM). The cross-sectional surface morphology and energy dispersive X-ray spectroscopy (EDS) were taken by field emission scanning electron microscopy (FESEM) (JEOL JSM-6700-F). For the devices measurement, the Kelvin probe force microscopy (KPFM) surface potential image and conductive atomic force microscopy (c-AFM) were carried out by ex-situ AFM (NT-MDT) with conductive Pt/Ir-coated Si probes (ACS 240-TM), having a diameter of ~20 nm, stiffness of 0.2 N m⁻¹ and a resonance frequency of ~75 kHz. The KPFM measurement was obtained at a user-defined lift height of 40 nm under room temperature.

2.3. Finite element simulation

The finite element method (FEM) by employing Agros2D simulation software with fine triangular meshing was used to confirm the electric field distribution and estimating the strength of localized conduction at different nanoscale surface morphologies.

3. Results and discussion

3.1. Device fabrication scheme

Figure 1(a) shows the schematic structures of Si surface before (as pristine) and after 30 s (middle) and 60 s (bottom one) etching time. In fact, these sequential schematic diagrams visually demonstrate the difference of etched surfaces with respect to the time of etching. The controlled formation of nano-level structures on Si substrate was created with particular conditions, which are provided in experimental section. In the next step, the multiphasic VOx oxide channel was deposited on pristine and treated Si substrates using the RF sputtering technique, as shown in Figure 1(b) schematically. In short, an ultrapure V2O5 target (99.99%) at high temperature of 600°C was used to accelerate the deoxygenation and crystallization of oxide layer [32]. Supporting Figure S1(a) shows the X-ray diffraction (XRD) graph, confirming the crystallization and existence of multiphasic VOx film. The multiphasic VOx film consists of three main components, such as V2O5, V2O3 (x < 1), and VO2. Figure 1(c) schematic shows the structure of device, consisting sputter-deposited VOx (~60 nm) on top of the etched

![Figure 1](attachment://image.png)
Si surface. The aluminum (Al) film was used as a bottom electrode. In addition, the schematic diagram also shows the topographical trace of the device produced by the AFM tip scanning with high and low probability of current conduction. The spacing between the two high conductive surfaces is considered as “d”.

### 3.2. Device surface characterization

To check the surface morphologies of the VOₓ/Si/Al devices, AFM topographic images were obtained over a scanning area of 3 × 3 µm². The nanostructures were observed from the surface morphologies of Vpristine, V30 and V60 samples exhibited in Figure 2(a-c), respectively. The topography of Figure 2a shows the granular nature of the pristine film. On the other hand, Figure 2(b, c), corresponding to the RIE etching time of Si substrate for 30 and 60 s, respectively, reveals that average surface roughness obtained by AFM as a function of the etching time is increased from 6.96 nm to 10.81 nm and the nanostructures are developed gradually with increasing RIE etching time (Figure R1-1 or S1(b), Supporting Information). To measure the height of nanostructures, the surface line profiles were obtained from its above given topographic images. The topographic images show an increase in nanostructures size due to the increase in substrate surface morphology produced by RIE. To measure the surface nanostructures, the surface line profiles images were obtained from its above given topographic images. The underneath graphs of Figure 2(a-c) shows the height profile (peak to trough) of 1.99 nm, 6.96 nm, and 10.89 nm corresponding to Vpristine, V30, and V60, respectively. Indeed, such a small nanostructure of Vpristine device indicates a smooth surface, while V30 and V60 devices signifies a nanostructures enhancement. It is worth mentioning here that the Si substrate etching shows an impact on the nanostructures of VOₓ sputter-deposition film. In addition, for further granular distribution analysis and to find out the effect of substrate etching, FESEM images were produced. Figure 2(d-f) shows cross-sectional SEM images corresponding to Vpristine, V30, and V60, respectively. These cross-sectional images not only confirm the ~60 nm thickness of VOₓ film but also reveal nanoscale etched areas on Si substrate, which are also affecting on the VOₓ film, as clearly appeared in Figure 2(e), and (f). Notably, the formation of nanostructures increases with the increase of etching time. Moreover, the correspondent underneath energy-dispersive X-ray spectroscopy (EDS) graphs depict the elemental distribution of silicon (Si), oxygen (O), and vanadium (V), respectively. In particular,

![Figure 2](image-url) Figure 2. Device surface characterization. (a-c) AFM topographic images highlighting the difference from granular nature between (a) Vpristine, (b) V30, and (c) V60 devices; underneath graphs correspondingly represent their surface morphology profiles. (d-f) Cross-sectional FESEM images showing (top) VOₓ film thickness and (bottom) EDS elemental mapping result of (d) Vpristine, (e) V30, and (f) V60 devices. Here, EDS images (underneath FESEM images) present the distribution of silicon (Si), oxygen (O), and vanadium (V). The scale bars in AFM and FESEM images are 0.6 µm and 100 nm, respectively.
the elemental distributions of V and O are completely overlapped on top surface of the corresponding images showing the multiphasic VO₂ thin film.

### 3.3. c-AFM and KPFM measurements

To understand the current conduction phenomenon and its modulation with increasing of etching substrate time, the current map along with the topographic image was obtained by performing c-AFM technique. In addition, the devices indicate an increase in current conduction with the increasing of voltage scanning window. A Pt/Ir c-AFM probe was used to perform these measurements. The c-AFM tip voltages of 1 V were applied through Vpristine, V30, and V60 devices separately over a scanning area of $3 \times 3 \, \mu\text{m}^2$, as shown in Figure 3(a-c), respectively. The smooth surface of Vpristine device produce less significant localized current map (bright current spots, grains) during device operation as revealed in Figure 3(a). Supporting Figure S2(a) reveals the 3D structure of c-AFM current map confirming nominal surface variation in the Vpristine device. A negligible current (in the range of pA) was appeared in the device, which reveals the transportation of minor amount of charge carriers during the device operation, as shown in Supporting Figure S2(b). In the meantime, higher current of 13.09 nA was recorded corresponding to V30 device, containing the $\sim 75\%$ area of bright current spots as shown in Figure 3(b). Herein, the c-AFM current map shows relatively strong current conduction across the preferential bright spots with a diameter of $\sim 21 \, \text{nm}$ (encircled by yellow color in Figure 3(b)), confirms the transport of charge carriers. It describes the etching of substrate produces vertical nanostructure and forms a bigger channel conduction area. The 3D configuration of c-AFM current map validates the said morphological analysis of V30 device, shown in Supporting Figure S2(c). Moreover, the bigger conduction channel was created by 30 s of RIE, forming an easy conduction path due to the generation of higher electric field as described in Supporting Figure S2(d). Although, V60 device was synthesized (60 s etching time) to obtain more strong conduction path and it also shows $\sim 90\%$ area of bright current spots across

![Figure 3](image-url)

**Figure 3.** C-AFM and KPFM measurements. (a-c) Nanoscale current maps of (a) Vpristine, (b) V30, and (c) V60 devices obtained using c-AFM; here, the scale bar is 100 nm. The change in surface topography of the samples is evidence for the etching effect of RIE, and bright spots on these maps can be viewed as current conduction channels. The bright spots encircled by yellow color show the grain diameter of ca. 21 and 58 nm for V30 and V60, respectively. (d-f) The local current-voltage ($I-V$) curves, obtained along with those c-AFM current maps, of (d) Vpristine, (e) V30, and (f) V60 devices under consecutive dual voltage sweeping of $\pm 10 \, \text{V} \, (\sim 10 \sim +10 \, \text{V})$. The $I-V$ results reveal the capacitive behavior of Vpristine and the bipolar resistive switching behavior of V30 and V60. (g) Contact potential difference, obtained using KPFM, showing the localized work function related to the variation of electric field of the corresponding devices. Here, the scale bar is 0.6 μm. (h,i) Decreases in work function and increases in total active area of Si samples as a function of etching time, respectively. Here, the active area was estimated during c-AFM mapping.
typical scanning area of 3 × 3 μm², as shown in Figure 3(c). However, the current conduction (6.46 nA) appears as smaller than V30 device despite an increased preferential bright spot diameter of ~58 nm (encircled by yellow color in Figure 3(c)), nevertheless better than Vpristine device. The Si substrate appears to be chopped from top and deep dug (spikier surface) at some places by RIE etching of V60 device, and channel conduction area becomes smaller as shown in Supporting Figure S2(e). Since it is known that the RIE can generate the surface defects, which leads to a decrease in the current with increasing the RIE etching time. Therefore, competition between surface morphology change and surface defect generation during RIE is likely to decide the overall performance. In short, the current map area generating a smaller conduction channel is instigated by the spikier surface of the device. In this case, schematic diagram of Supporting Figure S2(f) illustrates the current conduction mechanism of V60 device current map. As the tip voltage was applied to the bright spot, a smaller but strong electric field formed, and nA level current develops. Our devices appear to work at 1 V bias, challenging the low operating voltage devices. In addition, Supporting Figure S3(a-c) depicts the measurement of higher currents when tip voltages were enhanced to 2 V for Vpristine, V30, and V60 devices, respectively. The current conduction of Vpristine, V30, and V60 devices at 1 V measured on 5.15 pA, 17.9 nA, and 6.46 nA was enhanced by applying 2 V to 17.6 pA, 19.8 nA, and 7.5 nA, respectively.

To perform the resistive switching measurements, typical current-voltage (I–V) characteristics from negative to positive biasing of ±10 V (stated as “−10 + 10 V”) was applied on random bright spots of c-AFM current maps. The c-AFM conductive tip was used for applying bias with grounded Si/Al electrode at room temperature to generate resistive switching behavior (hysteresis loop) as shown in Figure 3(d-f). The structural design of conductive tip (~40 nm diameter) offers the measurement of the device configuration at even nanoscale level. Besides, in Vpristine device, the I–V hysteresis shows the disappearance of loop opening while applying the tip voltage on the preferential bright spot appears in the c-AFM current map area as shown in Supporting Figure S4(a). The resistive switching graph of Figure 3(d) shows the capacitive behavior of the device, caused by charge trapping [33]. A very small amount of maximum current of 0.71 nA was recorded, while the capacitive loop moves as marked in black arrows. A slighter shift in I–V curve was noticed in the course of three complete cycles, measured from the single bright spot to see the stability, as shown in Supporting Figure S4(b). Meanwhile, I–V from a random bright spot of V30 device current map (see, Supporting Figure S4(c)) indicates a clockwise hysteresis loop open, which shows a perfect resistive switching behavior, as shown in Figure 3(e). The loop opening depicts that the gradual and nonlinear current followed a stable path by applying the tip voltage sweep, called as analog resistive switching. The analog-resistive switching phenomenon is an essential and important feature to mimic the bio-synaptic functions. Note that the resistive switching displays an outstanding behavior during the negative voltage biasing (−10 ~ 0 V) by set of the device at the same way as for reset resistive switching loop (0 ~ +10 V). The V30 device loop opening indicates the existence of bipolar resistive switching behavior. In fact, resistive switching may vary at different bright spots of current map due to the inhomogeneous current distribution. Additionally, the I–V curve was repeated at the same bright spot for three consecutive cycles, indicating variation (slight shift) of nanoscale current conduction as shown in Supporting Figure S4(d). On the other hand, to further modulate the resistive switching behavior by etching of Si substrate, the I–V curves of V60 device was measured by applying tip voltage (−10 ~ +10 V) on the preferential bright spot of current map shown in Supporting Figure S4(e). Figure 3(f) reveals the analog resistive switching behavior while the loop opening was not as outstanding as for V30 device. For the reason that the negative biasing (−10 ~ 0 V) was not set fully, after it shows loop opening in reset measurement (0 ~ +10 V). V60 device-resistive switching maximum current state was lower than V30 device, happening due to the Si substrate etching discussed in c-AFM current maps. The current conduction appears to be lower in V60 device than V30 device (discussed in Figure 3(c)). Furthermore, Supporting Figure S4(f) shows repeated I–V curves at the same bright spot for three consecutive cycles, indicating variation (slight shift) of nanoscale current conduction. Resistive switching behavior may appear different at different bright spots, due to inhomogeneous current distribution of the device caused by the presence of grains and grain boundaries in the VOₓ films. Further, local I–V curves of the devices were measured at fixed nanoscale level bright spots by applying negative to positive bias. In fact, the gradual change and instability in the I–V curves can be more likely due to the gradual change in nanoscale filament size. Here, nanoscale current conduction mechanism is different than bulk measurement process [34]. This might be the reason for the instability and poor I–V behavior of the devices. The increase in current conduction with respect to cycle numbers shows the increase in electric field effect in the etching area. In addition, the calculated loop opening ratio of high current (I_high) and low current (I_low) for Vpristine, V30, and V60 device was 2.7, 8.16, and 7.47, respectively. The I_high/I_low ratio for V30
device is higher than Vpristine, and V60 device, indicating another essential feature for the bio-synaptic functions [35].

To ensure the change in nanoscale geometry the work function of the devices was required, which explains the change in electron tunneling sites [36]. Thus, to disclose the nanoscale nature of the devices, Kelvin probe force microscopy (KPFM) surface potential measurements were performed as shown in Figure 3(g). KPFM measurement is an innocuous scanning probe technique measured by the electrostatic interaction of sample surface and AFM tip. The KPFM measurements depict the nanoscale variation of current conduction in Vpristine, V30, and V60 devices over a scanning area of 3 x 1 µm². The localized work function indicates the variations of current conduction related to the variation of electric field of corresponding nanoscale devices. In general, the surface nanostructures of the device induced a shift of Fermi level position, which caused a change in the work function of the device. Figure 3(h) graph shows the work function of thin films versus Si substrate etching time. Interestingly, the work function for Vpristine, V30, and V60 thin films decreasing with the increasing of etching time. The Vpristine device shows the highest work function (5.39 eV). The change in work function happened due to change in electron tunneling sites caused by RIE etching, as shown in Figure 3h. Further, KPFM measurements show the nanoscale variation in the contact potential difference, which offers different conductive paths for the current conduction. Indeed, a distinct variation in the KPFM maps of the devices is observed as a function of etching time. Moreover, the possibility to generate the surface defects cannot be avoid during the RIE. However, as revealed by the simulation, the dominating part in the noticed charge transport is driven by the surface morphology. As the abrupt topographic height changes, the effective area changes and thus, altering the decrease of work function at 5.32 and 5.27 eV. The change in the work function could be due to abrupt change in topographic height or perhaps the etching is changing the stoichiometry of the surface. In Figure 3(i), the active area of the c-AFM current maps versus etching time was obtained. By comparison, the most etched Si substrate surface generates the maximum active area for current conduction.

3.4. Nanoscale synaptic behavior

Herein, we have demonstrated the tunable current levels of the proposed nanoscale-based devices by varying the etching time of Si substrate. Therefore, the proposed devices are befitting for use in nanoscale electronic synaptic functions. The human brain consists of connecting channel between pre- and postsynaptic neuron, which transmits information in the form of electrical or chemical synapses [37,38], as illustrated in schematic of Figure 4(a). Besides, to check the performance of nanoscale synaptic behavior of the devices, current was measured between the AFM tip and Al/Si electrode. Therefore, continuous electric pulses were applied on multiple points on a single bright spot to realize the synaptic behavior. However, synaptic behavior may vary at different nanoscale bright spots of current map due to the inhomogeneous current distribution. Further, the synaptic current was measured across bright spot of Vpristine device after applying the continuous electric pulses (+10 V, Δt = 20 ms), as shown in Figure 4(b). The

Figure 4. Nanoscale synaptic behavior. (a) Illustration of a synapse within a human brain. (b-d) Nanoscale synaptic response of (b) Vpristine, (c) V30, and (d) V60 devices under positive electric pulses of +10 V and duration of 20 ms, obtained using c-AFM. (e) Change in PPF (%) of Vpristine, V30 and V60 devices as a function of pulse interval (Δt); here, their PPF indexes gradually decrease as the pulse interval increases. (f-h) Finite element simulation obtained using Agros2D for demonstrating the electric field distribution from the c-AFM tip to VO, layers of (f) Vpristine, (g) V30, and (h) V60 devices. Meanwhile, red areas possess the highest current conduction while blue areas possess the lowest conduction.
synaptic current gradually increases with the applied electric pulses, indicating the nanoscale synaptic behavior. The maximum synaptic current was recorded at 0.06 nA for Vpristine device. On the other hand, same number of electric pulses was applied on c-AFM map of V30 device as illustrated in Figure 4(c). It is interesting that the preferential nanoscale bright spot exhibits an abrupt increase against continuous electric pulses (+10 V, Δt = 20 ms), as maximum current of 17.9 nA was recorded. Note that the instant increase in synaptic current caused by the strong current conduction due to etching of Si substrate as discussed above in Supporting Figure S3(d) schematic. Likewise, Figure 4(d) depicts nanoscale synaptic current behavior by applying the exact number of electric pulses at a specific bright spot on V60 device current map area. The V60 device also present the instant increase in synaptic current due to the electric field current conduction in nanoscale bright spot. However, the maximum current was lower at 4.77 nA than V30 device, indicating the behavior discussed previously in Supporting Figure S3(e) schematic. The gradual increase in current is caused by the strong current conduction due to etching of Si substrate, which is the primary signature to realize the synaptic behavior. Meanwhile, these results confirm the PPF-like nature of the devices. In fact, the gradual increase in the current indicates the strengthening of filament formation as we increase the number of bias pulses, as marked by the black arrow in Figure 4(b-d). Further, this phenomenon provides the information to understand the synaptic behavior at nanoscale with applied electric pulses. In addition, the nanoscale synaptic behavior of the devices indicates the ideal paired-pulse facilitation (PPF) nature of growth in synaptic current. PPF is an essential parameter that is defined by the ratio of post-synaptic current among two continuous pulses [1]. PPF (%) was calculated as (P2 – P1)/P1, where P1 and P2 are the first and second post-synaptic current, respectively [2,39]. As comparatively described in Figure 4(f), the facilitation ratio of Vpristine, V30 and V60 devices gradually decreases as the pulse interval increases. It can be observed that the V30 device produces the PPF ratio close to 500%, which is much higher than Vpristine and V60 devices. The nanoscale synaptic response of V30 device nanostructure indicate an essential feature to mimic the bio-synaptic function.

Furthermore, the measured higher performance of devices at low applied potential may be caused by the excessive mobile charges on the surface nanostructures. The feasible justification behind the modulation of current conduction could be due to the probe-assisted localized electric field inhomogeneity of the surface. Following this, the finite element method (FEM) by employing Agros2D simulation software was performed to confirm the possibility of probe-assisted filament formation and estimating the strength of localized electric field at different nanoscale surface morphological devices [40,41]. As in c-AFM measurements, the potential of 10 V was applied through AFM Pt tip on preferential position of devices with grounded Si/Al electrode, the FEM simulations were also performed in the same manner for Vpristine, V30 and V60 devices as shown in Figure 4(f-h), respectively. As for Vpristine device simulation (see, Figure 4(f)), there was no tip-induced filament formation occurred as already illustrated in experiment details. The field distribution of the Vpristine device confirmed an insignificant electric field production due to the smooth surface of the VOx thin film. On the other hand, a well confined and localized electric field distribution developed for V30 device as presented in Figure 4(g) and magnified view in the subsequent top inset. The top edge of the surface nanostructures contacted with tip potential causes a strong filament formation. Meanwhile, edges of the bump with ground also show tip-induced filament formation due to the strong electric field distribution in the device. It is worth mentioning here that the edges with the top contact are the most preferable bright positions for the strong electric field distribution. Moreover, the distribution of filament formation could be different at any random edge position on the bump. In addition, the observation for the V60 device reveals the relatively lower distribution of nanostructures than V30 device due to morphological electric field effect, as shown in Figure 4(h). It is noted that the edges on the top contact of bright spots are the only preferable positions where strong electric field distribution appears with a well-confined and localized filament formation.

4. Conclusion

In conclusion, RIE-etched Si substrate along with VOx multilayered sputter-deposition was fabricated. Conductive atomic force microscopy current maps with adjacent topographic images were obtained, disclosing the change of conductive area occurred due to etched substrates at different level. The reproduceable and consistent bipolar loop opening behavior of the corresponding devices have been demonstrated along with their change in work function. Nanoscale synaptic functions along with finite element simulations simultaneously explain the changes in localized filament formation for corresponding devices. Altogether, these findings support to provide an insight to produce advanced nanoscale synaptic applications as changing surface morphology to modulate E-field.
localization and pulse-switching behavior.

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Disclosure of potential conflicts of interest

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