Research on Fault Diagnosis Method of Gearbox Based on FPGA and LabVIEW

Zhuo Chen, Xiufang Yang*, Xiaolong Cheng
School of mechanical and precision instrument engineering, Xi’an University of Technology, Xian, China

*Corresponding author e-mail: yxf5078@xaut.edu.cn

Abstract. Gearbox is an important part of mechanical equipment. Its running state directly affects the working performance of the whole machine. Therefore, it is of great practical value in the research on gearbox fault diagnosis method. A gearbox fault diagnosis system based on FPGA and LabVIEW is designed in this paper, which consists of upper computer and lower computer. The lower computer uses FPGA as the core device to sample, convert, store and transmit signals, while the upper computer takes LabVIEW as the development environment to complete the signal processing and interface design of the fault diagnosis system. The experimental results show that the system is convenient for operating and user interface friendly. It can realize the real-time acquisition and transmission of the vibration signal of the gearbox, and the display and analysis of the vibration signal of the gearbox.

1. Introduction
With the rapid development of science and technology in recent years, the method of fault diagnosis of gearboxes should also advance with the times. It is an inevitable trend to apply the results of modern science and technology to the diagnosis of gearbox faults. For example, the literature [1] proposed an ARM-based gearbox vibration monitoring system. It can realize the state prediction of wind turbine gearbox system. In literature [2], a fault information acquisition and processing system is designed. STM32F103 microcontroller is used to control the peripheral chip to achieve data acquisition, communication and other functions. In literature [3], a vibration acceleration signal acquisition and processing system is designed with ATmega128 as the main control chip. It can meet the actual needs of modern industrial production. Literature [4] combined with time domain statistical feature analysis and multi-sensor information fusion technology, proposed a new method based on gray wolf optimized kernel extreme learning machine (GWO-KELM) for wind turbine gearbox condition monitoring. Based on the fusion data set, a fault classification recognition model based on GWO-KELM is established. Literature [5] proposed a fault diagnosis method that combined local wave decomposition and wavelet denoising. The FPGA has a high clock frequency, small internal delay, and high integration and flexibility, which is suitable for large data transmission. In this paper, a gearbox fault diagnosis system based on FPGA and LabVIEW is designed. Real-time data acquisition and transmission is realized by FPGA as the core device, and timely analysis and processing are performed to the upper computer to realize gearbox state diagnosis.
2. Over scheme design

Figure 1 shows the overall block diagram of the fault diagnosis system. The system consists of the upper computer and the lower computer. The lower computer uses FPGA as the core device, and the state machine (FSM) module is designed. The state control machine controls the ADC control module separately. The FIFO module and the UART control module implement the signal according to the specific workflow. Sampling, conversion, storage, transmission, in the ADC control module, the module drives the ADC128S022 device to sample and convert the output signal of the vibration sensor; the FIFO module works to buffer the converted digital signal in the FIFO; the UART control module is the FIFO. The digital signal is uploaded to the host computer through the UART serial port to complete the data transmission. The upper computer completes the processing and display of the signal to realize the analysis of the state of the gear box.

![Figure 1. General system diagram.](image)

3. FPGA data acquisition module design

The FPGA data acquisition module is based on the FPGA, which realizes sampling, conversion, buffering and transmission of data. The module includes an FSM module, an ADC control module, a data buffer module, and a data transfer UART module [6]. The ADC control module drives the AD module to perform analog-to-digital conversion of the sensor output signal. Considering that the reading rate of AD to the sensor is much higher than the transmission rate of the serial port, the data buffer memory FIFO is designed. The digital signal of A/D conversion is first written into the FIFO, and then the data is sent out at the data transmission rate of the UART serial port.

3.1. AD module design

The AD conversion module uses the low-power chip ADC128S022, which has 8-channel and 12-bit resolution. The conversion speed is between 50kps and 200kps. Typically, the power consumption is 1.2mw when powered by 3V and 7.5mw when powered by 5V. The chip ADC128S022 port functions are shown in table 1.

| port | Functions |
|------|-----------|
| CS   | Chip select, low level gating |
| VA   | Analog power input, input range: 2.7V-5.25V |
| AGND | Analog ground |
| IN0…IN7 | Analog input channel, input range 0-VREF |
| DGN   | Digitally |
| VD    | Digital power input, input range is 2.7V-VA |
| DIN   | Serial data input, sample input on the rising edge of SCLK |
| DOUT  | Conversion result output, output on the falling edge of SCLK |
| SCLK  | Clock input |

It can be seen from the SPI timing diagram of ADC128S022 in Figure 2. It takes 16 SCLK clocks to sample and convert one data. CS is the chip select terminal, low-level is valid, DIN is the chip serial data input, on the rising edge of SCLK Time sampling input, input three- bit address control channel selection port, DOUT is the serial data output of AD conversion, output on the falling edge of SCLK.
During the first three SCLK cycles, the ADC is in the sample mode. In the next thirteen cycles, the hold mode is held, the conversion is completed and the data output is completed [7].

The AD control module is designed according to the timing diagram of the AD chip. Figure 4 is the port diagram of the AD control module. In Figure 3, the left port is the input port and the right side is the output port. Channel is the sampling channel selection port, controlled by the state machine; Clk is the AD control module system clock port; Rst_n is the AD control module reset port, connected to the system total reset port; DIV_PARAM is the AD module clock divider setting port, setting ADC_SCLK Frequency, controlled by the state machine; En_Conv is the sample conversion enable port, controlled by the state machine; ADC_DOUT is the ADC conversion result port, connected to the DOUT port of the AD chip; ADC_SCLK provides the clock for the ADC operation, and the clock input SCLK port of the AD chip Connected; ADC_CS_N is the ADC enable signal, active low, connected to the chip select terminal CS port of the AD chip; ADC_State is the ADC working state signal port, low level during AD conversion, high level when idle, this signal Connected to the state machine; ADC_DIN is connected to the input port DIN of the AD chip to select the input signal channel of the AD chip; Data is the output port, and the AD control module converts the 12-bit serial data (from the ADC_DOUT input) converted by the AD chip to 12 Bit parallel data, output by the Data port, storing parallel data in the FIFO; Conv_Done is the output port when a data conversion is detected Upon completion, the Conv_Done port outputs a high level for one clock cycle.

3.2. FIFO data cache module design

The FIFO is a special data buffer that is input from one end of the FIFO in a specific direction and outputted at the other end, following the first-in first-out data transfer rules. In the FPGA software development environment Quartus, the FPGA is used to implement the FIFO design. Figure 4 is a port diagram of the designed FIFO buffer, where clock is the clock port, data is the data input port, rdsreq is the read enable port, wrreq is the write enable port; empty is the empty flag signal, full is the full flag signal, q is the data output port, usedw indicates the number of data in the FIFO, and the storage state in the FIFO can be observed.

3.3. Data transmission module design

The data transmission module uses a Universal Asynchronous Receiver Transmitter (UART) to transmit data. The UART transmission module is mainly composed of two parts, the baud rate generation module and the data transmission module [8]; the commonly used baud rates are 9600, 19200, 38400, 57600 and 115200; the baud rate indicates the number of data bits transmitted per second. The timing diagram of the UART transmitting one byte is shown in Figure 5.
It can be seen from the timing diagram of Figure 5 that when there is no signal transmission, the output terminal Rs232_Tx of the data transmitting module maintains a high level. When the signal is transmitted, it is controlled by the baud rate clock, and the low level of one bit is first transmitted as the START start bit. Then, the data is transmitted from the lowest bit Bit0. After the 8-bit data is sent, that is, after Bit0 to Bit7 are transmitted, a high level is sent as the STOP stop bit. The signal line Rs232_Tx remains high after the transmission is completed.

Figure 5. UART sends a byte timing diagram

Figure 6 is UART module implemented by an FPGA. Where band_set is the baud rate setting port, clk is the system clock port, rst_n is the system reset port, data_byte is the 8bit number to be transmitted, send_en is the transmit enable signal, rs232_tx is the rs232 signal output, and tx_done is the one byte send completion signal. One byte is sent and completed, generating a high level for one clock cycle. Uart_state is the transmit status port and is high when in the transmit state.

3.4. Finite State Machine (FSM) Design

In order to realize the control of the ADC control module, FIFO module and UART control module, according to the specific workflow, the finite state machine (FSM) module is designed. Figure 7 is a port diagram of a state machine module designed with an FPGA. In Figure 8, the left port is the input port and the right port is the output port. Connect the channel value Channel and the clock division DIV_PARAM set in the program to the Channel port and DIV_PARAM port of the ADC control module; connect the baud rate setting baud_set to the band_set of the UART serial port transmission module; wait for the button press after resetting the module When the button is pressed, the Key_Flag is high, and when the Key_State is low, the AD sampling state is entered and the En_Conv signal is generated according to the set sampling frequency to enable the AD control module; when a data sampling is finished, a Conv_Done signal is received. At this time, set wrreq to 1 to set rdreq to 0, enable FIFO write port, add 1 to the sampling counter until the set number of sampling points, and write data to FIFO at the same time; set wrreq to 0 to set rdreq to 1 to enable FIFO reading. The port enters the data transmission state, so that send_en effectively enables the UART serial port transmitting module to send data. When a data transmission is completed, a Tx_Done signal is received and the data transmission counter counts up to the set number of data, and the data is sampled and transmitted.

Figure 8 is a connection diagram of each module port. In the experiment, the button module is used to start the AD into the sampling state, and the button module is designed.
4. Fault diagnosis system interface design

In the host computer, LabVIEW is used as the development environment to realize the signal processing and interface design of the fault diagnosis system.

4.1. Serial communication function VISA

LabVIEW provides a powerful VISA library. VISA is a general term for standard I/O function libraries and related specifications for instrument programming. The VISA library resides in a computer system and completes the connection between the computer and the instrument for program control of the instrument. The essence is the standard API for the virtual instrument system. VISA serial port configuration this node is mainly used to initialize the serial port specified by the VISA resource name according to specific settings. In the process of communication transmission, the properties of the upper computer and the lower computer port are specified according to the same communication rule, that is, the communication ports of the two are initialized.

The VISA serial port configuration functions used in this system mainly include:

1. VISA Configuration Serial Port. Used for serial port initialization, select serial port, set baud rate, data bit, stop bit and check digit. The serial port baud rate is 9600bps, 8 data bits, 1 stop bit, and no parity.

2. VISA Read function (VISA Read). The data in the specified serial receive buffer is read into the computer memory by the specified number of bytes, which is an important node of the program.

3. VISA serial port number function (VISA Bytes at Serial Port). Returns the number of data bytes in the specified serial receive buffer.

4. VISA is closed (VISA Close). End the session with the specified serial port resource and close the serial port resource.

4.2. Design of upper computer for gearbox fault diagnosis system

In the LabVIEW development environment, the design interface is shown in Figure 9. The gearbox fault diagnosis system interface consists of time domain waveform display window, frequency domain waveform display window, serial port part VISA control port, sampling frequency and sampling point setting column, stop button and data display window; time domain waveform display window real-time display acquisition The data, the frequency domain waveform display window can intuitively reflect the frequency domain information of the collected signal; the VISA control port can select the matching serial port on the current interface, and the serial port configuration performs baud rate, data
bit, parity bit and Stop bit setting. The sampling frequency and sampling point setting column can
design the sampling frequency and the number of sampling points; the data display box can observe
the displayed real-time data, which is mainly a hexadecimal string type, and the stop button exits the
currently running system. It can be seen from the figure that the right side is the VISA function to
realize the configuration of the serial port. The data read by the serial port is subjected to a series of
analysis processing and data type conversion, thereby storing the received data in the data receiving
column. The collected data can be observed in the time domain to observe its time domain map, and
the collected data is subjected to fast Fourier transform to perform frequency domain display. Observe
the spectrum characteristics of the normal operation of the gearbox and reflect its working status in
real time to realize the function of fault diagnosis.

Figure 9. The system interface.

Figure 10. Sampling frequency is 2000 Hz.

4.3. Analysis and verification of gearbox fault diagnosis system

In the experiment, an AC signal containing a DC component was tested. The frequency of the AC
signal was 100 Hz, and the sampling frequency was set to 1000 Hz, 2000 Hz, 5000 Hz, and the
sampling time was 0.1s. Figure 10 shows the results of measurements at a sampling frequency of 2000
Hz. Comparing the measurement results at different sampling frequencies, from the time domain
diagram, the original signal is well restored, and the frequency domain analysis is also correct. The
peak frequency is at 100 Hz, accompanied by a large DC component. This system can be used for the
acquisition, transmission and analysis of gearbox vibration signals.

5. Conclusion

Based on FPGA and LabVIEW, this paper studies the gearbox fault diagnosis system, and uses
FPGA and LabVIEW to collect and analyze the gearbox running state. In the hardware FPGA
environment, the gearbox running status signal is collected in real time, and the gearbox fault signal is
timed. The frequency domain analysis can obtain the frequency component of the signal, and judge the
fault signal according to the fault characteristic frequency; the obvious result can be obtained. This
result is of great significance for the real-time detection of the gear fault.

References

[1] WANG Xiao, LIU Xiaoguang. Design of Vibration Monitoring System for Wind Power Gearbox
Based on ARM [J]. Generation & Air Conditioning, 2013, 34(02): 16-19.

[2] Wang Enbo, Sun Wei, Li Cui. Design and Implementation of Distributed Fault Information
Acquisition and Processing System [J]. Microprocessor, 2019, 40(02): 61-64.

[3] Ding Chuanyong, Liu Wei, Weng Tie, and Zhang Yan. Vibration Signal Acquisition and
Processing System in Mechanical Equipment Failure Warning [J]. Computer Products and
Circulation, 2019(06): 269.

[4] Long Xiafei, Yang Ping, Guo Hongxia, Zhao Zhuoli, Zhao Zhi. Fault Diagnosis of Wind Power
Gearbox Based on KELM and Multi-sensor Information Fusion [J]. Automation of Electric
Power Systems, 2019(17): 132-139.
[5] Li Sha. Research on gearbox fault diagnosis based on local wave decomposition [J/OL]. Mechanical Engineering and Automation, 2019(03): 154-156+159[2019-09-17].http://Kns.cnki.net/kcms/detail/14.1319.TH.20190603.0855.126.html.

[6] A high-precision data acquisition system for special equipment industry based on STM32 and FPGA [J].Journal of The Hebei Academy of Sciences, 2019, 36(02):7-14.

[7] Xu Mengjie, Liu Wenchen, Liu Yun. AD sampling design based on FPGA [J].Ship Electronic Engineering, 2015, 35(01): 114-118.

[8] DANG Junbo, LI Zhe, LI Yajun. Design and Implementation of Serial Communication Circuit Based on FPGA [J].Electronic Science and Technology, 2016, 29(07):106-109.