Test Time Reduction of 3-D Stacked ICs Using Ternary Coded Simultaneous Bidirectional Signaling in Parallel Test Ports

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Abstract—In order to meet the increasing demand for more performance with reduced power consumption and chip function-factor, semiconductor manufacturing is moving toward 3-D stacked integrated circuits (SICs). One of the challenges in bringing this technology into realization is the complicated test accessibility requirements of 3-D chips, which apart from having adequate defect coverage, should also have minimal test time. A major limiting factor in test time improvement of ICs is the number of chip terminals, such as pins or through silicon vias (TSVs) available for bulk vector transport in testing. In the conventional design, a chip terminal is only used to either send or receive data at any given time. In this article, a test accessibility architecture based on ternary encoded simultaneous bidirectional signaling (SBS), intended for use in parallel test access mechanism (TAM) in system on chip (SoC)-based designs, is proposed. This method enables the use of chip terminals to simultaneously send and receive test vectors, effectively doubling the per-pin efficiency during testing. Experiments show that this technique reduces the overall test time (OTT) by up to 53.6% as compared to conventional TAM design methods.

Index Terms—3-D stacked integrated circuits (SICs), design for testability (DFT), simultaneous bidirectional, system on chip (SoC), test access mechanism (TAM).

I. INTRODUCTION

WITH advancement in manufacturing technology, electronic devices are miniaturizing at an exponential pace. The transistor density has continued to increase with smaller technology nodes; however, further scaling, as per Moore’s law, seems to be difficult owing to performance and power concerns [1]. One of the promising ways forward is by forming 3-D stacked integrated circuits (SICs), in which the individual dies are stacked vertically and interconnected using through silicon vias (TSVs), micro-bumps or wire bonds, before being packaged as a single chip, as illustrated in Fig. 1. This allows more functionality to be embedded with a reduced footprint and also addresses another critical problem being observed in 2-D designs, that of increasingly long interconnects and latency issues. This concept is already beginning to gain attention in processor design [2], multicore processors with stacked memory [3], FPGAs [4], and chips have been manufactured by leveraging the third dimension, such as DDR 3 memory ICs [5].

The test time of ICs increases with design complexity and node density and has been a subject of significant research over the years. A significant contributor to test time is the test vector transport phase, in which a large volume of data is required to be serially shifted into the internal scan-chains [6]. 3-D stacking brings about several additional and more complex challenges for test access [7]–[10]. First, higher transistor density increases the probability of manufacturing defects, such as metal bridging, metal opens, via opens, and transistor defects. It, therefore, requires higher test vector volume for adequate coverage but without any significant increase in the chip terminals which further tightens the test access bottleneck. Second, the manufacturing process of 3-D SICs introduce additional defects and necessitates multiple test instances. Apart from wafer level and chip-level testing (known as prebond and post-bond testing, respectively), the 3-D SIC has to be tested at every point during the stacking process, known as mid-bond testing. Finally, the limited number of interdie vertical connections (such as TSVs, micro-bumps, or wire-bonds) add a further test access restriction in addition to chip terminals when transporting test vectors to dies higher up in the stack. As a result of the stated challenges, the overall test time (OTT) in 3-D SICs increase significantly compared to conventional 2-D chips, necessitating new test-access designs to bring down the test time and hence the test cost of the chips. Testing 3-D SICs is therefore considered a major constraint and listed as one of the difficult challenges for the industry by the international technology roadmap for semiconductors (ITRSs) [11].

In this article, a novel test access mechanism (TAM) design is proposed for 3-D SICs that doubles the data transfer efficiency of the Pins and TSVs, resulting in a substantial
This article further discusses the TAM design considerations for the incorporation of SBS in 3-D SICs such that it does not interfere with the functional mode performance and standard design for testability (DFT) logic, such as JTAG compliant boundary scan registers (BSRs). An example implementation suitable for low-frequency test vector transportation is presented, and its electrical characteristics are discussed. The performance gains of SBS compared to the traditional TAM design methods have been investigated on previously reported 3-D SIC designs based on ITC’02 benchmarks. In this way, the logic level, the circuit level, and the application level implications of this approach are evaluated. The proposed design supports scan tests for all test instances (pre-, mid-, and post-bond) in a 3-D IC test flow.

The remainder of this article is organized as follows. In Sections II and III, the background and prior work are described. In Section IV, the SBS-based TAM design approach and design considerations are presented. In Section V, the circuit design for SBS and spectre simulations are presented. Test time reduction of SBS compared to UDS in 3-D SICs is discussed in Section VI. This article concludes in Section VII.

II. BACKGROUND AND MOTIVATION

In VLSI devices, testing is a vital requirement for any IC design to ensure its reliable operation. Testing of a core-based chip design involves three main components: 1) the cores and the wrappers; 2) a tester which generates required test vectors, controls the test operation, and evaluates test response; and 3) a TAM which transports the test patterns/responses between the cores and tester. Scan-based testing is the most common way of DFT in core-based designs. The functional front end of the chip is designed as usual, and later the Flip Flops are made scan-test accessible by forming them into shift registers or scan chains using CAD tools. Testing is performed by sending in a set of precalculated test vectors to these scan chains and observing the response.

The scan vectors could be transported to the scan chains in several ways. The simplest being a serial TAM (STAM) such as IEEE 1149.1 (also known as JTAG) [12]. However, JTAG only has a single serial channel, which means that the data has to be shifted one bit at a time, which severely limits it is used for high data volume transfer for which a parallel TAM (PTAM) is used. In a PTAM, such as that allowed by IEEE 1500 Standard [13], a chip’s functional I/Os are temporarily used to enable data transfer on multiple test channels in parallel instead of one. It may be noted that the data is still shifted serially through the PTAM but using a higher number of test channels. Here, a “channel” is defined as a single bit path capable of transporting a test vector to and from the automatic test equipment (ATE) and the core under test. A similar architecture based on a combination of STAM and PTAM is expected for 3-D SICs, a standard for which is under development as P1838 Standard [14].

The OTT of a System on Chip (SoC) depends primarily on the test data volume (V), scan frequency (sf), and the available number of test channels (Tch) in a PTAM. A simplified estimate of the OTT can be given by $\text{OTT} = V / (sf \cdot T_{ch})$. Clearly, the OTT decreases with decreasing $V$ and increasing $sf$ and $T_{ch}$. The test data volume reduction can be achieved using test compression techniques [6]; however, beyond a certain point, it is likely to come at the cost of reduced fault coverage. The scan frequency is limited by thermal and design constraints; the scan chain insertion is not optimized for performance, and therefore the scan frequency is usually limited to a few tens of MHz. Most of the conventional TAM design methods, therefore, rely on either increasing the number of test channels, which is limited by the chip pins or increasing the pin efficiency by techniques, such as time division multiplexing (TDM) or Serializer/ Deserializer (SerDes) [15]–[18].

In the conventional TAM design, a test channel is formed using a separate terminal for input and output; therefore, the number of test channels in a PTAM is half the available chip terminals, as shown in Fig. 2(a). This is because conventional chip terminals are designed to communicate in simplex (unidirectional) or half-duplex (bidirectional) configuration. In either case, only a single transmit-receive pair is active at a given time, and the data could only travel in one direction. This simplifies the hardware implementation and has been sufficient in keeping the OTT of medium complexity chip designs down to an acceptable level; however, it does not scale well for more complex designs such as 3-D SICs which demand a higher number of test channels.

On the other hand, if a full-duplex configuration, such as SBS is used in the TAM, the data could be shifted in and out at the same pin simultaneously, as shown in Fig. 2(b), resulting in channel width equal to the number of chip terminals. The parallelism introduced by SBS increases the number of test channels, significantly reducing the OTT. Consider the example of an SoC with two cores and two chip terminals.
Each core has a single scan chain of 50 bits and requires two test patterns (say P1 and P2) for the scan-test. In a conventional TAM design using simplex/half-duplex chip terminals, the two pins would form a one bit wide TAM. Consequently, both the scan chains could be concatenated to form a single channel of $50 + 50 = 100$ bits as shown in Fig. 3(a). If however, an SBS-based TAM is used, the resulting TAM would be two channels of 50 bits each as shown in Fig. 3(c). The resulting schedule for both arrangements is shown in Fig. 3(b) and (d). $C_x - C_y$ denotes that the cores $x$ and $y$ will be connected in series, and $C_x || C_y$ indicates the cores will be connected in parallel to form a test session. It is evident that the OTT in the case of unidirectional TAM with schedule $C_1 - C_2$ is 300 clock cycles because of a single TAM channel, whereas for SBS TAM with schedule $C_1 || C_2$, the OTT is only 150 cycles. It could, therefore, be concluded that SBS ports increase the available TAM width, allowing more parallelism, which in the case of this example resulted in a reduction of 150 cycles in the OTT.

The added advantage of using SBS is that it can work in conjunction with the conventional TAM, as shown in Fig. 2(c). This means that instead of modifying all chip terminals to support SBS, only the most essential subset causing the bottleneck may be fitted with SBS while the remaining chip terminals operate as usual. This also implies that this method can be used to integrate hard-dies, in which the chip terminals are not modifiable.

III. PRIOR WORK

Most of the previous research has been focused on design, optimization, and scheduling of a TAM aimed at minimizing the OTT while using minimal chip resources. The TAM could connect the cores in series, such that the scan chains are tested sequentially, or the cores could be connected in parallel such that they could be tested simultaneously. In an ideal situation, all the cores in a die and all the dies in a 3-D SIC would be tested simultaneously, in parallel, which would result in the minimum OTT. However, several constraints limit this approach, such as: 1) it may not be possible to access all cores at a time due to limitations posed by IC terminals and TSVs; 2) there may be limitations of power and thermal dissipation which need to adhere; and 3) chip area that could be dedicated for the test architecture may be limited. In SoC, every core has specific test requirements that are specified by the core designer and it is the job of SoC vendor to put in place an appropriate TAM that fulfills these requirements. Clearly, there is a tradeoff between resources and the test time, and the task of the designer is to find the best possible solution for a TAM.

TAM optimization is shown to be an NP-Hard problem, and one way of reducing OTT is to find an improved optimization algorithm that points out the best possible TAM in the entire solution space with the objective of minimizing OTT while adhering to the chip constraints. Most of the noticeable work has been focused on 2-D SoC designs and various approaches to solving the problem have been adopted, such as integer linear programming [19], rectangle bin packing [20], and heuristics [21], [22]. While most of the work on 2-D TAMS has been focused on the constraints imposed by available TAM width, some researchers [23], [24] have also focused on thermal and power consideration, which is also an important factor since significantly higher switching activity is observed during tests.

As mentioned previously, 3-D SICs are considerably different and make the optimization process more challenging [7]–[9]. Wu et al. [25] presented a method to optimize the 3-D TAM designed using wrapper design suggested in [19] using a heuristic combination of integer linear programming (ILP), randomized rounding, and LP relaxation. Wu et al. [26] addressed the problem of scan chain ordering and partitioning using the genetic algorithm and ILP combined with heuristics to reduce wire length and OTT. Deutsch et al. [27] proposed heuristics to design optimized TAM under a set of uncertainties. It may be pointed out that the TAM optimization solution space is bounded by the physical layer of the TAM design. Most of the above works have relied upon conventional Unidirectional TAM design techniques and have not proposed any significant improvements in the physical design of the access infrastructure itself, more specifically, the improvement in pin efficiency.

The works that involve improvement of pin-efficiency include using TDM [15], [16]. The work in [15] has been concerned with reducing access time for serial reconfigurable scan networks (RSNs). Georgiou et al. [16] proposed a TDM-based method to reduce the OTT of 3-D SICs. The data is loaded through parallel buses at the scan frequency and is then serialized. The serial data can then be transferred from one die to another through TSVs operating at higher frequencies. Time de-multiplexers at the receiving end perform the serial to parallel conversion, and the data is shifted into scan chains at the scan frequency. Another approach to allow optimal utilization of tester resources was presented in [17] and [18]. Sehgal et al. [17] introduced the concept of virtual TAMS to efficiently utilize tester resources. Instead of operating the tester channels at a lower frequency to match scan frequency, SerDes were used to enable high-frequency data transfer between ATE and SoC I/O and low-frequency operation at the scan chains, thus maximizing ATE resource utilization. The approach adopted in this article focuses on SBS at the chip terminal, which internally presents two virtual unidirectional
I/Os to the SoC, just like UDS. The test time reduction techniques-based on TDM and SerDes could be designed on top of these virtual I/Os providing further test time reduction, with an added advantage that SBS would require one pin, whereas UDS would need two.

The idea of SBS was initially reported in [28], following which improved designs capable of delivering up to 900 Mb/s and 8 Gb/s (450 Mb/s and 4 Gb/s in either direction, respectively) were proposed and tested on fabricated devices in [29] and [30]. While these works rely on voltage-mode signaling, further enhanced design using current-mode differential transceivers were proposed in [31]–[33] for improved power efficiency in off-chip (chip to chip) [31], [32] as well as on-chip (core to core) [33] signaling. In 3-D SICs, SBS through TSVs has different design requirements, primarily because of negligible path resistance when compared to off-chip communication. Park et al. [34] presented an SBS transceiver (SBS TR) design for vertical communication in 3-D SICs through TSVs and achieved a data rate of 9.1 Gb/s. The performance of a single SBS channel has been shown to be better than two UDS channels, both in terms of power as well as on-chip area [29], [34]. The decrease in power consumption is attributed to lower switching activity as well as reduced voltage swing in SBS.

The research in SBS has mostly been focused on functional communication at higher data rates. High-speed SBS is usually complicated by noise concerns, such as common-mode noise rejection, echo cancelation, EMI considerations, and tight control of threshold voltage and comparator tolerances. However, as mentioned earlier, scan frequencies are typically a few tens of MHz, for which the design considerations become much relaxed, making testing a very viable application of SBS. The difference, however, is that unlike single-ended chip to chip channels where communication takes place between two transceivers, in this case, the chip terminal needs to be capable of functional communication in normal mode (assuming it is UDS) and SBS in test mode. To the best of our knowledge, TAM design methodology in 3-D SICs using SBS has not been studied in the past.

IV. PROPOSED APPROACH

SBS could be made possible by using ternary level encoding at the chip terminals (Pins and TSVs). The output from the sender and receiver is encoded into the ternary level at the chip terminal, and a decoding circuitry is used to convert back to binary levels. Here, it may be noted that the chip-terminal could either be the chip pin (only in case of the die which connects to the PCB, mostly the lowermost die) or a TSV. It is assumed that the functional communication at the chip terminal is UDS, and the proposed design aims to add SBS capability specifically for use in the test mode.

A. Ternary Level Coding

The overall idea is illustrated in Fig. 4, using an example chip with a single scan chain comprising of two FFs. The output of the scan chain is denoted as scan out (SO) and is fed to the chip terminal using an inverter as a transmitter (Tx), which becomes active during SBS mode. The external end of the chip terminal is to be driven using a similar setup (not shown in the figure) in another die (in case of TSVs) or the tester (in case of the first die) and is denoted as scan in (SI).

Two series resistors of equal value R1 (located on-chip) and R2 (on tester/another die) form a voltage divider circuit and essentially encode the binary input signal into the ternary level Vx at the node X. It may be noted that the resistors R1 and R2 are explicitly shown for clarity; in actual implementations, the SI and SO line driver output impedances and the I/O cell resistance may be sufficient to form the voltage divider circuit. The encoded signal is denoted as Vx, and it could take three values 0 (Vx|l), Vdd (Vx|h), or 1/2 Vdd (Vxm) depending on if SI and SO are both low, high, or in opposite states, respectively.

The ternary decoder (TD), shown in the hatched block, receives a copy of the SO signal, which is tapped just before the Tx where it remains in the binary state. The other input to the TD is the ternary encoded signal Vx, which is fed to one of the inputs to the two voltage comparators C1 and C2. The second input of the comparators is connected to high voltage reference Vref, which in this case are taken to be 2/3 and 1/3 Vdd, respectively. If Vx is 0 or Vdd, both comparators produce the same output (0 or 1); and if Vx is equal to 0.5 Vdd, C2 produces a 1 (since 1/2 Vdd > 1/3 Vdd), and C1 produces a 0 (since 1/2 Vdd < 2/3 Vdd). The outputs of C1 and C2 could be fed to an XOR gate, which in turn controls a 2 to 1 Multiplexer M1. One input of the Multiplexer M1 receives the SO signal while the other input received an inverted copy of the SO. The output of the Mux is the output of the ternary encoder and is denoted by decoded SI (DSI) signal, which is the input to the scan chain. The DSI always takes on the same value as SI, simply by deciding whether it is the same as SO or the opposite, depending on the Mux Sel signal from the XOR gate. In this way, the transmission and reception of the signal could be achieved simultaneously.

B. Test and Functional Mode Isolation

The use of SBS signaling in testing is complicated by the requirement of usability of the chip terminals in the functional operation of the chip as well. The design of the SBS must take into consideration that the functional path, which could be required to operate in the GHz range, may not be affected by the presence of SBS mode connections. Therefore, a transmission gate (TG)/analog switch is inserted just before the TD on the
ternary encoded signal $V_x$, and the drivers or the receiver at the functional side is designed as a tristate buffer (TB). These switches are controlled by the test enable (TE) signal of the chip, which could either be provided externally through a dedicated chip terminal or could be sourced from the die-level JTAG IR decoder by loading an appropriate user-defined instruction via the TAP controller. The overall arrangement is illustrated in Fig. 5. In this case, TE is de-asserted, and TG isolates the test side (dashed line) while TB is active, allowing the normal operation of the functional side (solid line). On the contrary, when TE is asserted, the functional side will be isolated.

### C. Integration With Boundary Scan

JTAG is a widely used DFT feature that allows essential test accessibility features at all levels of system hierarchy, such as die, chip, circuit board, and system level. BSRs is an essential component of JTAG, which allows the observability and controllability at the chip pins for test and debug purposes. Therefore, it would often be necessary to ensure that the incorporation of SBS does not affect the boundary scan capability of the chip. An illustration of an observable and controllable boundary scan cell (BSC) (using an example implementation given in [12]) is shown in Fig. 6(a). The proposed incorporation of SBS for a functional pin (in this case, an input) could be achieved, as shown in Fig. 6(b). As with the nonboundary scan chip terminal (Fig. 5), the tri-state buffer is used as a receiver along with TG for isolation. A multiplexer M1 is inserted between test data in (TDI) of the JTAG and R1 flip-flop of the BSR, such that depending on the state of control signal TE, either conventional boundary scan is selected (TE is low) or SBS is selected (TE is high) as shown in Table I. The state of the multiplexers M2 and M3 will depend on the current instruction in the JTAG IR. This configuration supports all the functionality of a conventional BSR, such as normal function, EXTEST, INTEST, SAMPLE, and PRELOAD, with an added option of SBS to support Parallel INTEST (for example when using WPPs of the IEEE 1500 standard compliant core wrappers).

It may be noted that the implementation, shown in Fig. 6(b), does not add any logic in the functional path and does not incur any additional penalty on functional mode performance. However, this comes at the cost of increasing the scan chain length by 1 bit, as the BSR Cell must be a part of the scan chain. An alternate arrangement is shown in Fig. 6(c), which allows the scan chain to be fed either from the BSR or from the chip terminal (using M4), while retaining all the functionality of Fig. 6(b). However, it necessitates the inclusion of the multiplexer M1 in the functional path which may affect the functional mode performance. If the performance degradation is acceptable, the arrangement in Fig. 6(c) is preferable because SBS can now be used for both functional and test mode communication along with UDS. Moreover, both these implementations also ensure that in case of a defect in the SBS circuitry, the testing could still be performed using conventional UDS-based DFT resources, thus providing redundancy.

### D. Vertical Access Considerations in Mid- and Post-Bond Testing

SBS implementation through TSVs is different in terms of transceiver design characteristics due to the low resistance and high capacitance of the TSV path. Therefore, further considerations are required for overall TAM design when accessing...
bypass flip-flops. The test time of the core 2-D SoCs given in [35] can be extended to stacked dies with dies using SBS, the equation for core test time calculation of the position of the die in the stack.

In order to calculate the test time of the cores in 3-D stacked dies using SBS, the equation for core test time calculation of 2-D SoCs given in [35] can be extended to stacked dies with bypass flip-flops. The test time of the core $T_c$ is then given by

$$T_c = (s + \max\{s_i, s_o\}) \cdot p + \min\{s_i, s_o\} + s - 1 \quad (1)$$

where $s$ is the position of the die in the stack, $s_i$ and $s_o$ represent the longest SI and SO chain lengths of the core wrapper, respectively, and $p$ is the total number of test patterns required by the core. This effects the test time of every core in the SIC except the first die in which case $s = 1$, and the equation reduces to $T_c = (1 + \max\{s_i, s_o\}) \cdot p + \min\{s_i, s_o\}$ which is the same as given in [35] for 2-D SoCs.

$E$. Prebond Testing

The case of TSV accessible dies is complicated due to difficulty in probing the TSVs at the prebond stage. Current processes are capable of producing TSVs with pitch and diameter of less than 5 $\mu$m [36]–[38], which is too small to be accessed through tester probes. Although a die may contain hundreds of TSVs, due to the stated probing issues, only a small subset of TSVs may be made accessible at the prebond stage using sacrificial probe pads. Therefore, the problem of prebond testing of TSV accessible dies can be considered similar to the pin accessible dies. The TAM design problem for the prebond testing may only be required to ensure the maximal utilization of SBS resources in all test instances (pre- mid- and post-bond).

$F$. Reference Sharing

The comparators C1 and C2 of the TD shown in Fig. 4 require a high and low reference voltage ($V_{ref_l}$ and $V_{ref_h}$). For low-frequency applications, the dies can have separate references generated locally on the die or sourced through the tester. However, for high-frequency applications, in order to couple the common mode noise to the receivers as well as to cancel out the effect of power supply variations, it may be necessary to have a shared reference between the dies, as shown in Fig. 8.

The requirement of two wires for reference generation between the first die and the tester, and between the dies also reduces the number of test Pins and TSVs available for the transportation of the test vectors. If the number of available test pins is denoted by $P_{max}$ and the total number of TSVs in the entire stack is given by $TSV_{max}$, then the pins available for testing ($W_{bi}$) and TSVs available for testing ($TSV_{bi}$) using SBS is given by

$$W_{bi} = P_{max} - 2 \quad (2)$$

$$TSV_{bi} = TSV_{max} - 2(M - 1) \quad (3)$$

where $M$ is the number of dies in the stack. Despite the reduction in test Pins and TSVs in the SBS scheme, the number of test channels increases significantly compared to the conventional unidirectional approach since a single wire forms a channel in the former approach, whereas two wires form one channel in the latter approach.

$V$. SBS Transceiver Circuit Design

In this section, an example SBS TR design is presented for use in low-frequency test mode for 3-D TSV communication.
There are several ways in which SBS can be implemented. For high-frequency applications, differential mode communication is used [39], [40]. Although differential mode transceivers are power efficient and highly noise resistant, allowing very high bandwidth, the requirement of two pins to form a channel limits its use in parallel test ports, for which single-ended transceiver designs [34], [41], [42] is preferable.

The above works are designed for normal mode communication for high-speed data transfer. The implementation discussed below is intended to be used as an additional circuit for used in test-mode such that: 1) the effect on functional performance is minimal and 2) given the low-frequency requirements, the implementation is simplified and power efficient.

The main components of an SBS implementation shown in Fig. 9(a), where SBS communication takes between the second die and the first die through a TSV. The Transmitter and the TD in both dies are similar; therefore, the detailed schematic is shown only for the second die. In the following paragraphs, the circuit design is described in light of the different design options.

A. Transmitter

The transmitter can simply be designed as an inverter of appropriate size to allow the required bandwidth. However, this design may not be power efficient when the driving transmitters at either end of the channel are in opposite states, consuming static power, as reported by Park et al. [34]. To limit the static current, the proposed transmitter is built as an inverter with diode-connected MOSFETs, as shown in Fig. 9(a) [31]. The MOSFETs $M_{PS}$ and $M_{PS}$ perform the inverter switching and the diode-connected MOSFETs $M_{NR}$ and $M_{PR}$ serve as active series resistors, minimizing the static current and hence the static power consumption. Similar to a normal inverter, there is no static power consumption when the transmitters at both ends are either high or low.

The resistance of the diode-connected MOSFETs at a given instance is a function of $V_x$, and consequently the state of both the transmitters $(11,10,01,00)$. Fig. 9(b) shows the equivalent circuit for the middle voltage level $(V_{xm})$ when one of the transmitters is high, and the other is low $(10,01)$. Ignoring the TSV resistance and assuming the switching transistors as ideal, the middle voltage level $V_{xm} = V_{dd} (R_P/(R_P+R_N))$ where $R_P$ and $R_N$ are the resistance of $M_{PR}$ and $M_{NR}$ at $V_x = V_{xm}$. The resistance $R_{on}$ of a diode-connected MOSFET can be approximated by

$$R_{on} = \frac{V_{DS}}{I_d}$$

where $I_d = \mu C_{ox} \frac{W}{L} (V_{GS} - V_t) V_{DS}$

therefore

$$R_P = \frac{L_p}{\mu_n C_{ox} W_p (V_{xm} - V_{dd} - V_{tp})}$$

$$R_N = \frac{L_n}{\mu_n C_{ox} W_n (V_{xm} - V_{tn})}$$

where $L$ and $W$ are the length and width of the diode-connected MOSFETs, $\mu$ is the mobility of the channel, $C_{ox}$ is the oxide thickness, and $V_t$ is the threshold voltage. It is clear that the $W$ and $L$ ratios of the diode-connected nMOS and pMOS can be adjusted to obtain the desired $V_{xm}$ level. When both the transmitter inputs are low $(00)$, as shown in Fig. 9(c), $V_x$ is pulled high through the $M_{PS}$ and $M_{PR}$, however as $V_x$ approaches $V_{dd}$, $M_{PR}$ enters into the subthreshold region and the resistance $R_{P1}$ approaches the off resistance $R_{off}$, restricting the upper voltage swing to $V_{xh} = V_{dd} - V_{tn}$. Nevertheless, since there is a small conduction current in the cut-off region as well, $V_x$ will gradually approach $V_{dd}$ and hence $V_{dd} \geq V_{sh} \geq V_{dd} - V_{tp}$. Similarly, when both the transmitters are sending high $(11)$, $V_x$ is pulled low to $V_{dl} \leq V_{tn}$ as shown in Fig. 9(d). The upper and lower voltage swing can be further improved by using body effect to reduce $V_t$.

In Fig. 9(a) the transmission gate switch TG added after the transceiver ensures that the transceiver does not affect the normal mode operation (TG is open when $TE = 0$). However, the diffusion parasitic capacitances of TG do appear in the functional path, but it is minimal compared to the TSV capacitance, and the effect on normal mode performance is expected to be negligible.

B. Ternary Decoder

The main component of the TD is the voltage comparator which could be designed either as a differential amplifier [41] or a voltage-sense amplifier [34]. The proposed receiver has

![Fig. 9. (a) Proposed SBS TR circuit, (b) equivalent circuit for $V_{xm}$, (c) equivalent circuit for $V_{sh}$, and (d) equivalent circuit for $V_{dl}$.](image-url)
been based on the later, because of its simple design, robustness, and low power consumption. The circuit diagram of the sense-amplifier-based TD is shown in Fig. 9(a). Note that the TD in Fig. 4 contained two comparators, an XOR gate and a multiplexer, however for area and power efficiency the proposed implementation is optimized such that the XOR gate and the multiplexer is not required and only one comparator is used and the reference is switched between the high value (Vref_h) and low (Vref_l). When the SO signal is high (SO = 1), the transmitter output is low and the signal Vx can only take the low and middle value and vice-versa. Therefore, the lower reference Vref_l is selected when SO = 1 and Vref_h when SO = 0. The reference switching is achieved using the transmission gate multiplexer with SO as the control signal.

The sense amplifier receives the ternary encoded input Vx and the reference voltage Vref at the gates of nMOS transistors Msbs and Mref, respectively. The transistor pairs M1, M2, and M3, M4 form two cross-coupled inverters, forming a regenerative latch. The sensing takes place during the positive half cycle. The transistors Msbs and Mref, depending on the voltages at the respective gates, will have different resistance and hence the voltage drop. In the negative half cycle, one of the nodes of the regenerative latch with the higher voltage is pulled high, and the lower voltage is pulled low, hence the comparator action. Since the input to TD was inverted by the transmitter, the inverting output of the sense-amplifier is taken as the output DSI, which can be fed directly to the scan chain. The transistors M5 to M7 are controlled by the clock and allow the latch action.

The proposed TD behaves like a neg-edge triggered flip-flop and introduces a delay of one clock cycle; however, it removes the requirement of a separate flip-flop required for die-to-die communication, as shown in Fig. 7. As noted earlier in Section IV-D, the inclusion of the flip-flops is necessary from the DFT standpoint and is expected to be a part of the upcoming 3-D IC DFT standard P1838 [14].

### C. Simulation Results

The SBS TR was simulated with Cadence Spectre using 180-nm technology. The design was limited to 50 MHz frequency, which was easily achieved by using minimum size for all transistors in the transceiver. Assuming a TSV with 5 μm diameter, 20 μm length, substrate doping concentration Na of 2 × 10^{15}/cm^3, and oxide thickness of 200 nm, the TSV was modeled based on [43] as a lumped RC circuit with a resistance Rs\textsubscript{tsv} ≈ 100 mΩ and capacitance Cs\textsubscript{tsv} ≈ 30 fF as shown in Fig. 9. The series inductance of the TSV was ignored as it is negligible at low frequencies. Minimum sized transistors provided a Vx swing with Vxh ≥ 0.7 Vdd, Vxm ≤ 0.2 Vdd. Vref_l and Vref_h were chosen to be 0.28 and 0.47 Vdd, respectively. The voltage levels at various points for the four possible combinations of SI and SO are shown in Fig. 10. The output, DSI, of the TD, correctly reproduces the SI signal and appears at the output of the first scan-flop (DSIf) with a delay of one clock cycle.

The power consumption of the proposed SBS TR was compared with the unidirectional transceiver designed as 4×-buffers.

The average power consumption for a pair of transceivers (one channel), when transmitting and receiving the same pseudo-random binary sequence (PRBS), is given in Table II. The SBS TR consumes approximately 27% more power compared to UDS. However, it may be noted that the TD samples the Vx at the negative edge of the clock cycle; therefore, one of the TG (hence the transmitter) can be turned off during the remaining (negative) half cycle of the clock, further reducing static power. This can be achieved with a NOR gate with Clk and TE as the inputs, whose output (and a complement, generated using an inverter) controls the TG. In this case, the SBS TR consumes approximately 6% lesser power compared to UDS (inclusive of the power consumed by the added circuit), at the expense of six additional transistors per channel.

TSVs are usually designed in clusters, and so, cross-coupling with the neighboring TSVs is an essential concern in TSV communication. The performance of the SBS TR in the presence of noise coupling was studied, assuming a 3×3 TSV cluster with the center TSV as the victim, as shown in Fig. 11(a). Considering 10-μm pitch between TSVs and silicon resistivity of 6.89 Ω.cm (for Na = 2 × 10^{15}/cm^3), the values of the coupling capacitances C_{si,j} and resistances R_{si,j} of the silicon substrate between the victim TSV i and aggressor j were calculated using the coupling model described in [44], as shown in Fig. 11(b). Assuming all the aggressors are being driven by similar SBS TRs with different PRBS
In all cases, $V_x$ remains stable at approximately $V_{cm} \approx 0.39$ Vdd, $V_xh \geq 0.7$ Vdd, and $V_{xl} \lesssim 0.2$ Vdd. Also, as the drain current is not ideally zero in the subthreshold region, $V_xh$ and $V_{xl}$ will slowly tend to approach $V_{dd}$ and $Gnd$, respectively. This explains the signal spread above $V_xh$ and below $V_{xl}$, caused when the input of both transmitters does not change over consecutive cycles and augmented by the cross-coupling. Sufficient voltage margins exist between $V_{ref}$ and $V_x$ to account for the process variation (TD requires as little as 40 mV difference between $V_x$ and $V_{ref}$). The transceiver operation was also verified across all process corners in the presence of noise coupling.

Overall, at the expense of only 19 minimum sized transistors per TSV, up to 53.6% reduction in test time could be achieved as detailed in the next section. Moreover, separate die-bypass flip-flops may not be required as the TD acts like a flip-flop.

VI. OVERALL TEST TIME COMPARISON

SBS doubles the bandwidth of the channel for a given clock frequency compared to UDS. This statement may be sufficient to report the improvement expected in normal mode communication in which the exact usage of the link over a longer period may not be known. However, testing is a complete process in which the link utilization over the entire period of the test is known, and it is possible to calculate the exact improvements in test times. The overall reduction in test time would depend on the number of available test Pins and TSVs, the construction of the SIC and the dies, their test requirements, and also the TAM, which may be different for both. In this section, the test time improvements of SBS versus UDS are quantified for various 3-D SIC designs reported in the literature for a varying number of pins, TSVs, and the number of dies.

A. TAM Design Methodology

In order to compare the test time of the conventional UDS TAM with SBS (assuming all Pins and TSVs support SBS), experiments were conducted using $3 \times$ handcrafted 3-D SICs from the ITC'02 [45] Benchmarks reported in [46] and a fourth SIC in which the number of dies was gradually incremented from 2 to 9. The composition of each SIC is shown in Table III. The optimal TAM design and test schedule for both were obtained using ILP, based in part on the model presented in [19] for Test-Bus architecture-based die level TAM design [47], and on [46] for 3-D SIC TAM design. The optimization problem using ILP is known to be NP-Hard [48], and the complexity increases exponentially with an increasing number of variables and constraints. Therefore, for better runtime efficiency, first, the optimal solutions for all possible values of the die test time for different TAM widths were precalculated using the enumerative method $P_{NDAW}_{enumerate}$ described in [19]. This was followed by 3-D TAM design using the ILP model described in [46]. As both of these methods are based on ILP, the solution is always optimal.

The overall problem could be stated as: given an SIC with $M$ number of dies, each die has $N$ cores such that $N_b$ denotes the total number of cores in die $b$. Each core has certain I/Os, scan chains of specific lengths, and the number of test patterns to be applied. Let $P_{max}$ denote the maximum number of pins available at the lowermost die and $TSV_{max}$ denote the global TSV limit. Find the best possible TAM design that minimizes the OTT by:

1) finding the 3-D schedule (how dies should be tested) by optimal allocation of Test Channels [calculated using (2) and (3), for SBS] to each die such that the upper limit $P_{max}$ and $TSV_{max}$ is not exceeded;
2) finding the optimal 2-D schedule (how cores within the die should be tested) such that the allocated number of channels dictated by the SIC level schedule (in part a) is not exceeded.

The optimization solution returns the TAM for the SIC, which includes a 3-D schedule, 2-D schedule, and the resultant minimum possible test time (OTT). The 2-D and 3-D scheduling policy and the test time calculation method used in this article is further elaborated with the help of an example in the following paragraph.

Consider the third row of Table IV which gives the optimal solution for SIC 1 with 40 Pins and 200 TSVs. The optimal 3-D schedule for SBS is $1[2−3]\{4\}[5]$ with TAM widths of 24, 14, 20, 16, and 2 channels, respectively, for Dies 1–5. This implies that the 3-D schedule has two sessions (separated by “−”); in session 1, Dies 1 and 2 will be tested in parallel using TAM widths of 24 and 14 channels, respectively, followed by session 2 in which the TAM will be reconfigured to access Dies 3, 4, and 5 with 20, 16, and 2 channels, respectively.

The TAM width allocated to a die in a 3-D schedule is further

![Fig. 11. TSV cross-coupling: (a) victim TSV (center) and 8 aggressor TSVs in a 3×3 cluster; (b) TSV-TSV coupling model [44]; (c) histogram of $V_x$ voltage levels at the receiver sampling time, under cross-coupling.](image-url)
divided into sub-TAMs to form a 2-D schedule. For instance, the 2-D schedules for all dies in SIC 1 of the above example (row 3 of Table IV) are shown in Table V. A TAM width of 16 channels was allocated to Die 4, for which the optimal 2-D schedule is “[1]∥[2−3−4]” with sub-TAMs of {8, 8}. This implies that the 16 channels allocated to the die are further divided into two sub-TAMs of eight channels each. Sub-TAM1 connects exclusively to core 1, and sub-TAM2 connects cores 2, 3, and 4 in series. The cores within a sub-TAM are tested sequentially, and the test time of the sub-TAM is the sum of all core test time, i.e., \( T_{sub-TAM} = \sum (T_{core}) \), where \( T_{core} \) is calculated using (1) for SBS. As all the sub-TAMs run tests simultaneously, the test time of the die \( T_{die} = \max(T_{sub-TAM}) \). Subsequently, as one or more dies may be tested simultaneously within a 3-D session, \( T_{session} = \max(T_{die}) \); and finally, as the 3-D test sessions are run sequentially, the OTT of the SIC \( OTT = \sum(T_{session}) \). In this way, for the given 2-D schedule, the test time for Die 4 was 374 009 cycles. \( T_{die} \) for the remaining dies is calculated similarly (Table V), which gives the OTT of 1541512 cycles for the given 3-D test schedule.

For simplicity, only post-bond test scenarios of soft-dies and soft-cores have been considered. Moreover, only the test time involved in the shift cycle of the internal scan-test has been calculated as the rest can be ignored, being negligible. The effect of bypass flip-flops has only been accounted for SBS and ignored for UDS.

**Table IV**

| Pins \((F_{max})\) | TSVs \((T_{max})\) | OTT (cycles) | Schedule | Channel Allocation | OTT (cycles) | Schedule | Channel Allocation | % OTT improvement (uni- vs bi-directional TAMs) |
|-----------------|-----------------|-------------|----------|------------------|-------------|----------|------------------|-------------------------------------|
| 20              | 200             | 5632583     | [1-2-3-4] | 10;7;5;9;1       | 3211831     | [1-2-3] | 18;18;10;8;18    | 42.98                               |
| 30              | 200             | 3781790     | [1-2-3-4] | 12;11;3;4;15     | 2077911     | [1-2-3] | 23;19;8;5;1      | 45.05                               |
| 40              | 200             | 2854606     | [1-2-3-4] | 20;14;6;18;2     | 1541512     | [1-2-3] | 24;14;20;16;2    | 46.00                               |
| 50              | 200             | 2271852     | [1-2-3-4] | 25;14;6;5;25     | 1232343     | [1-2-3] | 23;14;6;5;48     | 45.76                               |
| 60              | 200             | 1929521     | [1-2-3-4] | 25;20;9;5;1      | 1022692     | [1-2-3] | 28;17;7;6;48     | 47.00                               |
| 70              | 200             | 1643683     | [1-2-3-4] | 34;20;8;7;1      | 863264      | [1-2-3] | 33;19;8;7;1      | 47.48                               |
| 80              | 200             | 1455507     | [1-2-3-4] | 20;11;5;4;25     | 774276      | [1-2-3] | 37;23;10;8;48    | 46.80                               |
| 90              | 200             | 1314575     | [1-2-3-4] | 22;12;6;5;25     | 698956      | [1-2-3] | 41;26;10;9;2     | 46.98                               |
| 100             | 200             | 1167503     | [1-2-3-4] | 24;14;6;5;1      | 629794      | [1-2-3] | 45;30;11;10;2    | 46.06                               |
| 110             | 200             | 1079197     | [1-2-3-4] | 26;15;7;6;1      | 579846      | [1-2-3] | 49;32;13;12;2    | 46.27                               |
| 120             | 200             | 993597      | [1-2-3-4] | 29;17;7;7;22     | 545324      | [1-2-3] | 52;35;14;13;4    | 45.12                               |
| 130             | 200             | 901726      | [1-2-3-4] | 31;18;8;7;1      | 545324      | [1-2-3] | 57;35;14;18;4    | 39.52                               |
| 140             | 200             | 836701      | [1-2-3-4] | 34;20;8;7;1      | 545324      | [1-2-3] | 65;35;22;14;2    | 34.82                               |
| 150             | 200             | 790304      | [1-2-3-4] | 36;21;9;8;1      | 545324      | [1-2-3] | 54;35;13;21;16   | 31.00                               |
| 160             | 200             | 735361      | [1-2-3-4] | 38;23;10;8;1     | 545324      | [1-2-3] | 52;35;13;18;4    | 25.84                               |

**Table V**

| Die Level Schedule | Channels | \( T_{die} \) |
|--------------------|----------|--------------|
| Die1               | [5-7-10-12-16-18-24-25-26-17-29-32] || [2-3-6-8-13-14-28-30] || [1-4-9-11-15-17-19-20-21-22-23-31] | 7,8,9       | 1167503         |
| Die2               | [1-4-5-8-11-15-16] || [2-6-7-12-14-17-19] || [3-9-10-13-18] | 2,5,7       | 1144129         |
| Die3               | [2-3-8-10-13-14-16-17-19-20-22-23-24-27] || [7-9-11-12-18-21-25-28] || [1-4-5-6-15-26] | 4,5,11     | 368546          |
| Die4               | [1] || [2-3-4] | 8,8          | 374009         |
| Die 5              | [2-3-4-5-7-9] || [1-6-8-10] | 1,1           | 323743         |

**Fig. 12.** % improvement in OTT of SIC 1 with varying Pins and TSV limits.

**Fig. 13.** Variation of the core test time with increasing number of test channels.

**B. Results and Discussion**

Table IV shows the exact solutions for the OTT and the relevant schedule and channel allocation of SIC 1 using conventional, and SBS-based TAM when the number of pins of the bottom die is varied from 20 to 160 in steps of 10, and the global TSV limit is 200. It is evident that SBS offers significant OTT reduction; however, it may be noted that as the number of test-pins is increased, while the OTT in the case...
of both conventional and SBS TAMs decreases (as expected), the advantage offered by SBS decreases. The effect of variation of both $P_{\text{max}}$ and $TSV_{\text{max}}$ on the %OTT improvement for SIC 1 is shown in Fig. 12. A maximum improvement of 53.6% could be observed when $P_{\text{max}} = TSV_{\text{max}} = 60$ for this particular SIC. Below this number, the advantage of using SBS decrease to 19.6% (at $P_{\text{max}} = 20$, $TSV_{\text{max}} = 20$). This is due to the fact that when the pin and TSV count is too low, the reference generation overheads become significant (in this case, two Pins and eight TSVs).

Fig. 12 also shows a decrease in the percent improvement using SBS (10.8%) as the pin and TSV limit approach 200. This could be explained using Fig. 13 in which the test times of 3 SoCs (f2126, p22810, and p34392 of the ITC’02 benchmarks) are shown against the number of channels available for testing. It can be seen that as the number of test channels is increased, the test time of the die decreases until a certain point is reached, after which there is no further decrease. In the literature, this is commonly referred to as the Pareto-optimal point, at which the $T_{\text{die}}$ does not decrease with the increase in the number of test channels and is constrained by the length of the longest scan chain in the die cores. When using SBS, the number of test channels increase quickly with increasing Pins/TSVs and reaches Pareto-optimal point much earlier. However, as Pins/TSVs are increased further, the conventional TAM scheme also reaches the Pareto-optimal point, at which both schemes will have the same testing time. It may also be mentioned that at this point, the OTT of SBS may even be slightly higher due to the inclusion of die-level bypass flip-flops.

Figs. 14 and 15 show the OTT improvement using SBS for SIC 2 and 3. In both cases, a maximum improvement of around 48% percent could be observed. Unlike SIC 1, both SIC 2 and 3 do not exhibit the Pareto-optimality effect at $TSV_{\text{max}} = P_{\text{max}} = 200$ (Pareto-optimal point does exist well beyond $TSV_{\text{max}} = P_{\text{max}} = 200$ but not shown for clarity). This is because SIC 1 has the most complex die (p93791) placed at the bottom and benefitted directly from the increase in pin count as well as the TSV count. However, SIC 2 and 3 have the most complex die placed on top and the middle, and require a relatively large increase in TSVs to allocate more channels to reduce OTT(die). For example, to increase one test-channel for Die 5, which is the most complex die in SIC 2, at least four TSVs are required to be added for SBS TAM (and 8 for UDS TAM). On the contrary, if the OTT limiting complex die is the third die as in SIC 3, an increase in only two TSVs (4 for UDS TAM) would deliver the same result. Therefore, if complex dies are higher up in the stack, a higher number of TSVs would be required to bring down the test time to the Pareto-optimal point.

The average improvement in OTT over the range of Pins and TSVs considered is 40.53% for SIC 1, 42.4% for SIC 3, and 43.07% for SIC 2.

In order to study the offered improvement in OTT using SBS with the increasing number of dies (and hence the complexity) of the SIC, the number of dies in SIC 4 was incremented from 2 to 9 in a single die step. The global TSV limit was fixed to 100, and the percent improvement in OTT ($\Delta \text{OTT} \%$) when the number pins are 50, 100, 150, and 200 are shown in Fig. 16(a)–(d), respectively. It is evident that as the number of dies increase, $\Delta \text{OTT} \%$ either remains constant or increases with the SBS approach. The relatively lesser improvement observed for Dies 2 and 3 when the number of pins equals 150 in Fig. 16(c) and 200 in Fig. 16(d) is because both TAM design schemes are operating in the Pareto-optimal region. Moreover, the addition of the sixth die which is q12710 of the ITC’02 benchmark circuits, causes the relative improvement to dip down to 34% in all cases. This is due to the fact that q12710 SoC has only 13 scan chains of lengths ranging from 413 to 1689 bits. Therefore, the test time of the SoC is now constrained by the length of the longest scan- chain of 1689 bits and remains the same as the TAM width is increased beyond 12 channels. Moreover, q12710 is placed high up in the stack and becomes the source of TSV constraint very quickly and dominates the test time for the entire stack. In all other instances, SBS offers a significant improvement of up to 46%, and hence it is clear that this scheme scales well with the increasing SIC complexity. Also, the average $\Delta \text{OTT} \%$ for the four cases of Fig. 16(a)–(d) are 43.37%, 42.41%, 35.45%, and 32.98%, respectively, i.e., the improvement offered by SBS is more pronounced when there is a lesser number of pins, and diminished as the pins are increased. In practical scenarios, the test-channels (Pins and TSVs) are mostly very limited and that the advantage of SBS is likely to be more pronounced.
VII. CONCLUSION

A novel PTAM design method leveraging the ternary encoded simultaneous bidirection signaling method was proposed for test time reduction of 3-D SICs. At the logic level, design considerations for the incorporation of SBS into PTAM while allowing functional mode utilization of chip terminal and co-existence with conventional UDS-based DFT resources was presented. At the circuit level, an example SBS TR design along with simulations was presented. At the overall test application level, experiments with four handcrafted 3-D SICs showed a maximum improvement of 53.6% is possible. The advantage of SBS is more significant when the chip terminals are limited and scales well with SIC complexity.

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Fig. 16. Comparison of OTT and the percent OTT difference ΔOTT (%) using Conventional and SBS-based TAMs with increasing number of dies in SIC 4. Global TSV limit has been fixed to 100 and Pins equal to (a) 50, (b) 100, (c) 150, and (d) 200.
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