Impact of Synaptic Device Variations on Classification Accuracy in a Binarized Neural Network

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Brain-inspired neuromorphic systems (hardware neural networks) are expected to be an energy-efficient computing architecture for solving cognitive tasks, which critically depend on the development of reliable synaptic weight storage (i.e., synaptic device). Although various nanoelectronic devices have successfully reproduced the learning rules of biological synapses through their internal analog conductance states, the sustainability of such devices is still in doubt due to the variability common to all nanoelectronic devices. Alternatively, a neuromorphic system based on a relatively more reliable digital-type switching device has been recently demonstrated, i.e., a binarized neural network (BNN). The synaptic device is a more mature digital-type switching device, and the training/recognition algorithm developed for the BNN enables the task of facial image classification with a supervised training scheme. Here, we quantitatively investigate the effects of device parameter variations on the classification accuracy; the parameters include the number of weight states ($N_{state}$), the weight update margin ($\Delta G$), and the weight update variation ($G_{var}$). This analysis demonstrates the feasibility of the BNN and introduces a practical neuromorphic system based on mature, conventional digital device technologies.

Conventional computing architectures (von Neumann architectures) consume large amounts of energy when solving cognitive tasks due to the unavoidable inefficiency of data transfer between the processor and the off-chip memory. This inefficiency is referred to as the von Neumann bottleneck. Alternatively, by mimicking both the functional and structural advantages of the biological neural system, power-efficient computing systems (i.e., neuromorphic systems1) have recently been developed and are expected to offer promising breakthroughs. The practical implementation of the neuromorphic system depends on the development of ideal synaptic weight storage (i.e., the synaptic device). Highly integrated synaptic devices with sufficient reliability are essential for the on-chip implementation of a neuromorphic system that can process big data in real time, similar to the human brain.

Currently, various nanoelectronic synaptic devices based on two-terminal resistive switches (i.e., memristors) have demonstrated promising results by emulating the functionalities of biological synapses using their intrinsic analog conductance states2–8. Furthermore, using an integrated memristor network, functional neuromorphic systems have been experimentally applied to practical calculation tasks involving pattern recognition9, sparse coding10, matrix equations11, and differential equations12. Nevertheless, the sustainability of such devices is still in doubt due to the variability that is common to all nanoelectronic devices13–15. Because the physical mechanism of the conductance modulation in most prospective synaptic devices is a random process, that is, an atomic-level change based on electro/thermodynamics16, both cycle-to-cycle and device-to-device variations of conductance modulation are unavoidable17.

This concern may result from a misunderstanding of the neuromorphic system. The neuromorphic system simulates and exploits the characteristics and advantages of the brain, but this simulation and exploitation do not mean that the system must exactly imitate all of the structural and functional features of the brain. Unfortunately, with the goal of realizing a neuromorphic system that resembles the brain, most previous synaptic device studies blindly worked to demonstrate devices that were as similar as possible to biological synapses. As a result, most of

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the previous studies have focused only on the development/improvement of the analog conductance modulation dynamics, attempting to make them more similar to the dynamics of biological synapses while ignoring the variability issues2–8.

Alternatively, the sustainability and reliability of digital-type switching devices have been consistently ensured over the past 20 years18. Using current NAND flash technology, stable multiple memory states (4-bit = 16 states) with three-dimensional stackability have already been applied to a product. Therefore, if well-qualified conventional digital devices can contribute to a synaptic device, the aforementioned variability issues from memristors can be addressed. We have demonstrated a binarized neural network (BNN) in our previous study19, in which the synaptic device was a mature digital-type switchable device—a gate-all-around (GAA) silicon nanosheet transistor. By applying a supervised online training scheme, a set of multiple digital-type synaptic devices (buckets) were able to represent the analog synaptic weight. The BNN had an image classification capability that was verified by simulation and experiment19. However, our previous simulation was limited because the effect of synaptic device variations was ignored; the simulation was performed under the assumption that all synaptic devices in the system had equivalent characteristics without any variations. Therefore, in this study, the BNN is applied to facial image classification, and the effect of the synaptic device variations such as the number of weight states ($N_{\text{state}}$), the weight update margin ($\Delta G$), and $G_{\text{var}}$ is included. The effect of device variations on the classification accuracy is analyzed quantitatively using the simulation. These results demonstrate the feasibility of BNNs, which provide higher immunity to synaptic device variability than conventional neuromorphic systems based on analog synaptic devices do.

**Results and Discussion**

In our previous work, we demonstrated a BNN and its supervised training scheme for an image classification application19. Briefly, Fig. 1a depicts the architecture of a BNN with $M$ inputs and $N$ outputs. The input image information corresponds to $u_1(i)$ and $w_1(i)$. The vector $s_1(i)$ enables supervised training by selecting a specific row, and $z_1(i)$ is the output of the network. (b) The schematic of a synaptic transistor array, where $s_1(i)$ involves $V_G$, and either $u_1(i)$ or $w_1(i)$ involves $V_D$. The integration of $I_s$ along a row corresponds to $z_1(i)$. (c) Schematics of the applied pulse trains used to characterize the channel conductance modulation property of the GAA silicon nanosheet transistor. Each pulse train consists of potentiation and depression pulses applied to the gate ($V_{\text{pot}}$ and $V_{\text{dep}}$ for 100 μs). Control of the $V_{\text{pot}}$ level contributes to the different conductance-switching behaviors of $N_{\text{state}}$, $\Delta G$, and $G_{\text{var}}$.
stochastically determined by the learning probability $p$, defined as $p = \gamma u_i(i)$ ($\gamma$ is the learning rate). Note that the most distinctive feature of the BNN is that the synaptic weights in the network $G(i,j)$ are given within a binary value: $G(i,j) = \{G_{\text{high}} \text{ or } G_{\text{low}}\}$, where $G_{\text{high}}$ and $G_{\text{low}}$ represent the high- and low-conductance states of the synaptic device, respectively. To represent actual analog weights using only $G_{\text{high}}$ and $G_{\text{low}}$ the network $G$ is partitioned into sub-buckets (the size of each bucket is $B_j$). Each bucket is trained with a single specific input image according to the label. In addition, the selection vector $s_i(i)$, defined as $s_i(i) = [1 - 1 0]$, directs the training on the input image according to the label, where $1, -1, 0$ represent “potentiation,” “depression,” and “no update” of the synaptic weight, respectively. Consequently, a set of binary values stored in the bucket can represent analog synaptic weights, which are related to the input image according to the label. Additional explanations for the operational principles of the BNN are presented in Supplementary Information Note 1.

In this study, the performance of the BNN is evaluated through the task of classifying images of faces from the Yale Face Database, which contains a total of 165 grayscale images (32 × 32 pixels) of 15 individuals. In the database, there are 11 images per subject, and each image represents a different facial expression or configuration (center light, with glasses, happy; left light, without glasses, normal; right light, sad, sleepy, surprised, and winking). Here, we select 8 of the 11 images for the training set, and the remaining 3 images are used as the test set. Only the images in the training set are inputted to the network during the training phase. To evaluate the classification accuracy during the recognizing phase, only the images in the test set are inputted into the network.

For the storage of binarized synaptic weights in the BNN, a GAA silicon nanosheet transistor is used as the synaptic device (Fig. S2, Supplementary Information Note 2). The embedded charge-trap layer (silicon nitride, SiN) in the gate dielectric enables adjustable channel conductance (i.e., a synaptic weight update). The synaptic device array is configured such that $s_i(i)$ corresponds to the gate voltage ($V_G$) of the synaptic transistors in a particular row, and either $u_i(i)$ or $v_i(i)$ corresponds to the drain voltage ($V_D$). The integrated $I_D$ of each row ($\sum I_D = \sum G \cdot V_D$) is the summation vector $s_i(i)$. Figure 1c shows the evolution of channel conductance in synaptic transistors as a pulse train is applied. Negative $V_G$ ($V_D = V_{\text{dep}}$) leads to the detrapping of electrons in the SiN layer, which results in an increase in channel conductance up to $G_{\text{high}}$ (i.e., potentiation). In contrast, positive $V_G$ ($V_D = V_{\text{dep}}$) results in the decrease in channel conductance down to $G_{\text{low}}$ (i.e., depression). The number of trapped electrons in the SiN layer depends on the level of $V_D$. This dependence allows $G_{\text{high}}$ or $G_{\text{low}}$ to be adjusted, which enables control of the weight update margin ($\Delta G = G_{\text{high}}/G_{\text{low}}$) and the multiple weight state ($N_{\text{state}}$). The cycle-to-cycle weight variation ($G_{\text{var}} = |\max(G) - \min(G)/\text{mean}(G)|$) is relatively smaller even after thousands of switchings, and $\Delta G$ is larger than the previous two-terminal memristors whose $\Delta G$ is below 10 with severe fluctuations. The remainder of the paper discusses how the improved reliability of the digital-type weight update will contribute to the sustainability of the entire neuromorphic system.

First, we investigate the impact of the number of weight states ($N_{\text{state}}$) on the classification accuracy of the BNN. Conventional memristors can theoretically have infinite internal conductance states ($N_{\text{state}} = \infty$), but considering only the states that can guarantee reliability (e.g., data retention time or endurance), $N_{\text{state}} = 8$–16 is the current technological limit. Considering this reliability limitation, $N_{\text{state}}$ that can be obtained with current digital-type switching devices (e.g., a quad-level cell NAND flash is 16) is not inferior to memristors. To identify the effect of $N_{\text{state}}$ on the classification accuracy in the BNN, two different cases are compared: one with $N_{\text{state}} = 2$ (Fig. 2a) and the other with $N_{\text{state}} = 16$ (Fig. 2b). The comparison assumes that there is no device-to-device variation. The simulated accuracy of facial image classification is shown in Fig. 2c,d as a function of the training epoch, where the number of networks alters the training curve (red curve). With the source current of each synaptic transistor ($I_{\text{source}}$) and the number of networks, the accuracy reaches approximately 50% with $B_i = 200$. By deploying an additional network (red curve), the accuracy improves to approximately 70% with $B_i = 200$ and $B_i = 100$. The accuracy continues to improve with more networks, up to 80% (blue curve). However, as shown in Fig. 2d, a larger $N_{\text{state}}$ is less effective in improving the accuracy; rather, a greater number of training epochs are required. In the case of typical neuromorphic systems, the synaptic weight should be adjustable exactly as we designed to achieve the higher accuracy, a larger $N_{\text{state}}$ is advantageous for more precise $G$ control. However, in the case of our BNN, as binarized/quantized weight is gathered to represent a specific analog weight, the effect of the controllability in each synaptic weight on the accuracy is relatively reduced. Additionally, the pattern classification in the BNN is performed based on the bucket grouping multiple synaptic weights, and the effect of each weight value is also inevitably reduced. This unique feature of the BNN allows a feasible implementation of the neuromorphic systems; engineering of the synaptic device to have a larger $N_{\text{state}}$ is not required any more like a conventional memristor-based neuromorphic systems. Consequently, although only binarized/quantized weight is used, a reasonable accuracy can be obtained from a BNN with a higher training speed. This result indicates that a neuromorphic system without analog-type synaptic weights can perform a cognitive task by exploiting both BNN architecture and its supervised training scheme.

Next, a similar analysis was performed to study the effect of the weight update margin ($\Delta G$) on the classification accuracy. In a conventional memristor-based neuromorphic system, increasing $\Delta G$ can improve the classification accuracy. The $\Delta G$ of common memristors is about $10^{-1}$–$10^{-2}$, thus, much research has been devoted to further increasing $\Delta G$. In contrast, our digital-type synaptic device (i.e., a GAA silicon nanosheet transistor) can obtain larger $\Delta G$ of up to $10^4$ (Fig. 1c) by modulating the amplitude of $V_{\text{dep}}$ or $V_{\text{tra}}$. In this BNN simulation, as shown in Fig. 3a, $\Delta G$ is adjusted from 2 to $10^4$, assuming no device-to-device variation. Figure 3b shows the classification accuracy as a function of $\Delta G$. The modulation of $\Delta G$ (as well as the increased $N_{\text{state}}$) has little effect on the accuracy, which is contrary to the behavior of conventional memristor-based neuromorphic systems. The reason for this conflicting result is as follows: The memristor-based neuromorphic system uses multiple analog states defined within $G_{\text{high}}$ and $G_{\text{low}}$ for image training and recognizing, and the distinguishability and stability of each analog state critically affect the performance of the system. A larger $\Delta G$ leads to better distinction of each
analog state, resulting in better distinction between the patterns to be distinguished and the background (noise)\(^3\). However, since BNN uses only binarized synaptic weight values (\(G_{\text{high}}\) and \(G_{\text{low}}\)), the amount of difference between \(G_{\text{high}}\) and \(G_{\text{low}}\) is not critical. Therefore, the classification accuracy in BNN is independent of \(\Delta G\). This feature of the BNN can be a great advantage in realizing practical on-chip neuromorphic systems, because current nanoelectronic device technology is already sufficient to produce a \(\Delta G\) of more than 10 without any further engineering of synaptic device.

Finally, the effect of the weight variation (\(G_{\text{var}}\)) on the classification accuracy was analyzed. The intrinsic instability and lack of control of analog conductance switching behavior in memristors critically degrade the performance of neuromorphic systems\(^24,28\), although these systems are capable of tolerating device-to-device variation.

Figure 2. The distribution of synaptic device conductance (G) in the BNN when (a) \(N_{\text{state}}\) is 2 and (b) \(N_{\text{state}}\) is 16. It is assumed that there is no device-to-device variation, that is, all synaptic devices in the simulation have equivalent \(G_{\text{high}}\) and \(G_{\text{low}}\) values. The evolution of the classification accuracy as a function of the training epoch is shown for when (c) \(N_{\text{state}}\) is 2 and (d) \(N_{\text{state}}\) is 16. The simulated accuracy is obtained by repeating the simulation 10 times.

Figure 3. (a) The distribution of synaptic device conductance (G) in the BNN with different \(\Delta G\). It is assumed that there is no device-to-device variation, that is, all synaptic devices in the simulation have equivalent \(G_{\text{high}}\) and \(G_{\text{low}}\) values. (b) The simulated accuracy as a function of \(\Delta G\), which is obtained by repeating the simulation 10 times.
The distribution of synaptic device conductance ($G$) in the BNN considering $G_{var}$. The device conductance of all synaptic devices is determined stochastically within a given $G_{var}$ range during the weight update process. Here, $\Delta G = \text{mean}(G_{\text{high}})/\text{mean}(G_{\text{low}})$ is fixed to 10. (b) The simulated accuracy as a function of $G_{var}$, which is obtained by repeating the simulation 10 times.

or noise to a certain degree. In our digital-type synaptic device, shown in Fig. 1c, $G_{\text{high}}$ and $G_{\text{low}}$ fluctuate during repeated switching. $G_{var}$ can be defined as $[\text{max}(G) - \text{min}(G)]/\text{mean}(G)$, where $G$ is either $G_{\text{high}}$ or $G_{\text{low}}$. In this BNN simulation, shown in Fig. 4a, $G_{var}$ is adjusted from 0.2 to 1.0 with fixed $\Delta G = 10$. As the weight of all synaptic devices is determined stochastically within a given $G_{var}$ range during the weight update process, this simulation considers not only cycle-to-cycle variation but also device-to-device variation. Figure 4b shows the classification accuracy as a function of $G_{var}$. An increase of $G_{var}$ leads to the degradation of the accuracy. When $\Delta G = 2$ (blue curve), the accuracy is severely degraded, to below 40%. However, when $\Delta G$ is above 5 (green and red curves), the effect of an increase of $G_{var}$ is not critical. As a BNN uses only binarized synaptic weight values, the immunity of cycle-to-cycle or device-to-device variations is considerably higher than for memristor-based neuromorphic systems. The high immunity to device variability is not the result of a well-demonstrated digital-type synaptic device. Instead, the BNN architecture and its supervised training scheme contribute to the high sustainability of the system. Therefore, further research efforts to implement a practical neuromorphic system should be devoted to developing the architecture and training scheme, rather than focusing on the improvement of analog properties in the synaptic device.

In summary, we have analyzed the impact of synaptic device variations on image classification accuracy in a BNN. The BNN has the following unique characteristics: 1) By using only binarized weight, the BNN can classify the input images with reasonable accuracy through the supervised training scheme. 2) The classification accuracy is independent of the weight update margin ($\Delta G$) of the synaptic device. 3) The BNN is highly immune to variability (such as $G_{var}$). Due to characteristics 2 and 3, current device technology is sufficient to create a synaptic device without any further research effort. Actually, prior to our study, memristor-based BNNs has been proposed to reduce the memory access by binarizing the weight. But it is still an open question how to build and train a neural network with binarized weight. So far, each previous study has proposed different BNN operation schemes, and each study has a different point of view. The main goal of previous memristor-based BNNs is to focus on more energy-efficient processing of deep neural network algorithms. However, our research rather focuses on providing an architecture and operation scheme that is less sensitive to synaptic device variations. Consequently, our BNN can provide a device-level breakthrough for neuromorphic systems, which are currently based on conventional memristors, and provide a novel direction and inspiration for future neuromorphic engineering.

**Methods**

**Test images form the yale face database.** We are compliant with Yale’s policy of reuse/use of these images (http://vision.ucsd.edu/content/yale-face-database).

Received: 14 August 2019; Accepted: 8 October 2019;
Published online: 23 October 2019

**References**

1. Mead, C. Neuromorphic Electronic Systems. *Proc. IEEE* **78**, 1629–1636 (1990).
2. Zamarreño-Ramos, C. et al. On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex. *Front. Neurosci.* **5**, 26 (2011).
3. Serrano-Goñi, T., Masquelier, T., Prodromakis, T., Indiveri, G. & Linares-Barranco, B. STDP and STDP variations with memristors for spiking neuromorphic learning systems. *Front. Neurosci.* **7**, 2 (2013).
4. Jo, S. H. et al. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* **10**, 1297–1301 (2010).
5. Yu, S., Wu, Y., Jeysasingh, R., Kuzum, D. & Wong, H. S. P. An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation. *IEEE Trans. Electron Devices* **58**, 2729–2737 (2011).
6. Kim, S. et al. Experimental demonstration of a second-order memristor and its ability to biorealistcally implement synaptic plasticity. *Nano Lett.* **15**, 2203–2211 (2015).
29. Kim, S.
28. Burr, G. W.
27. Stathopoulos, S.
26. Kim, W.
24. Yu, S.
23. Chen, P. Y.
22. Huang, P.
33. Yu, S.
31. Bocquet, M.
32. Huang, P.
11. Sun, Z.
12. Zidan, M. A.
13. Narayanan, P.
14. Zhao, W., Querlioz, D., Klein, J.-O., Chabi, D. & Chappert, C.
17. Kuzum, D., Yu, S. & Philip Wong, H.-S. Synaptic electronics: materials, devices and applications.
10. Sheridan, P. M.
9. Prezioso, M.
8. Zhu, L. Q., Wan, C. J., Guo, L. Q., Shi, Y. & Wan, Q. Artificial synapse network on inorganic proton conductor for neuromorphic systems. Nat. Commun. 5, 333–342 (2014).
9. Prezioso, M. et al. Training and operation of an integrated neuromorphic network based on metal-oxide memristors. Nature 521, 61–64 (2015).
10. Sheridan, P. M. et al. Sparse coding with memristor networks. Nat. Nanotechnol. 12, 784–789 (2017).
11. Sun, Z. et al. Solving matrix equations in one step with cross-point resistive arrays. Proc. Natl. Acad. Sci. USA 116, 4123–4128 (2019).
12. Zidan, M. A. et al. A general memristor-based partial differential equation solver. Nat. Electron. 1, 411–420 (2018).
13. Narayanan, P. et al. Parameter Variability in Nanoscale Fabrics: Bottom-Up Integrated Exploration. In 2010 IEEE 25th International Symposium on Defect and Fault Tolerance in VLSI Systems 24–31, https://doi.org/10.1109/DTF.2010.10 (IEEE, 2010).
14. Zhao, W., Querlioz, D., Klein, J.-O., Chabi, D. & Chappert, C. Nanodevice-based novel computing paradigms and the neuromorphic approach. In 2012 IEEE International Symposium on Circuits and Systems 2509–2512, https://doi.org/10.1109/ISCAS.2012.6271812 (IEEE, 2012).
15. Pouyan, P., Amat, E. & Rubio, A. Reliability challenges in design of memristive memory. In 2014 5th European Workshop on CMOS Variability (VAR1) 1–6, https://doi.org/10.1109/VAR1.2014.6957074 (IEEE, 2014).
16. Ielmini, D. Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth. IEEE Trans. Electron Devices 58, 4309–4317 (2011).
17. Kuzum, D., Yu, S. & Philip Wong, H.-S. Synaptic electronics: materials, devices and applications. Nanotechnology 24, 382001 (2013).
18. Monzio Compagnoni, C. et al. Reviewing the Evolution of the NAND Flash Technology. Proc. IEEE 105, 1609–1633 (2017).
19. Kim, S. et al. Binarized neural network with Silicon nanosheet Synaptic transistors for Supervised pattern Classification. Sci. Rep. 9, 11705 (2019).
20. Belhumeur, P. N., Hespahna, J. – P. & Kriegman, D. J. Eigenfaces vs. Fisherefaces: Recognition Using Class Specific Linear Projection. Ieee Transactions on Pattern Analysis And Machine Intelligence 19 (1997).
21. Park, S. et al. Neuromorphic speech systems using advanced ReRAM-based synapse. In Technical Digest - International Electron Devices Meeting, IEDM 25.6.1–25.6.4, https://doi.org/10.1109/IEDM.2013.6724692 (IEEE, 2013).
22. Burr, G. W. et al. Experimental demonstration and tolerancing of a large-scale neural network (165,000 synapses), using phase-change memory as the synaptic weight element. In 2014 IEEE International Electron Devices Meeting 29.5.1–29.5.4, 10.1109/IEDM.2014.7047135 (IEEE, 2014).
23. Chen, P. Y. et al. Mitigating effects of non-ideal synaptic device characteristics for on-chip learning. In 2015 IEEE/ACM International Conference on Computer-Aided Design, ICCAD 2015 194–199, https://doi.org/10.1109/ICCAD.2015.7372570 (IEEE, 2016).
24. Yu, S. et al. Scaling-up resistive synaptic arrays for neuro-inspired architecture: Challenges and prospect. In Technical Digest - International Electron Devices Meeting, IEDM 17.3.1–17.3.4, https://doi.org/10.1109/IEDM.2015.7409718 (IEEE, 2015).
25. Prakash, A. et al. Demonstration of Low Power 3-bit Multilevel Cell Characteristics in a TaOx-Based RRAM by Stack Engineering. IEEE Electron Device Lett. 36, 32–34 (2015).
26. Kim, W. et al. Multistate Memristive Tantalum Oxide Devices for Ternary Arithmetic. Sci. Rep. 6, 36652 (2016).
27. Stathopoulos, S. et al. Multihit memory operation of metal-oxide bi-layer memristors. Sci. Rep. 7, 17532 (2017).
28. Burr, G. W. et al. Experimental Demonstration and Tolerancing of a Large-Scale Neural Network (165 000 Synapses) Using Phase-Change Memory as the Synaptic Weight Element. IEEE Trans. Electron Devices 62, 3498–3507 (2015).
29. Kim, S. et al. Pattern Recognition Using Carbon Nanotube Synaptic Transistors with an Adjustable Weight Update Protocol. ACS Nano 11, 2814–2822 (2017).
30. Kim, S., Lim, M., Kim, Y., Kim, H.-D. & Choi, S.-I. Impact of Synthetic Device Variations on Pattern Recognition Accuracy in a Hardware Neural Network. Sci. Rep. 8, 36738 (2018).
31. Bocquet, M. et al. In-Memory and Error-Immune Differential RRAM Implementation of Binarized Deep Neural Networks. In 2018 IEEE International Electron Devices Meeting (IEDM) 20.6.1–20.6.4, https://doi.org/10.1109/IEDM.2018.8614639 (IEEE, 2018).
32. Huang, P. et al. Hardware implementation of RRAM based binarized neural networks. APL. Mater. 7, 081105 (2019).
33. Yu, S. et al. Binary neural network with 16 Mb RRAM macro chip for classification and online training. In 2016 IEEE International Electron Devices Meeting (IEDM) 16.2.1–16.2.4, https://doi.org/10.1109/IEDM.2016.7838429 (IEEE, 2016).

Acknowledgements
This research was supported by the Nano-Material Technology Development Program (2016M3A7B4910430) funded by the Ministry of Science, ICT and Future Planning, research programs supported by the National Research Foundation of Korea (NRF) grant (2019R1A2C1002491, 2019R1A2B5B01069988, and 2016R1A5A1012966), and the Future Semiconductor Device Technology Development Program (Grant 10067739) funded by MOTIE (Ministry of Trade, Industry & Energy) and KSRC (Korea Semiconductor Research Consortium).

Author contributions
The manuscript was prepared by S.K. and S.-J.C. Device fabrication, measurement, and simulation were performed by H.-D.K. and S.K.

Competing interests
The authors declare no competing interests.

Additional information
Supplementary information is available for this paper at https://doi.org/10.1038/s41598-019-51814-5.
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