Design and implementation of HF signal receiving and processing module based on FPGA

Q Y Gong¹, L Zhang¹, L Y Yu¹ and R L Yan¹
¹PLA Strategy Support Information Engineering University, Zhengzhou, Henan, China

Email: 423430350@qq.com

Abstract. This article designs and implements a receiving processing module based on the Xilinx ZCU102 evaluation board for the signal waveform defined in Appendix C of MIL-STD-188-110C. The focus is on the digital down-conversion, synchronization capture, and adaptive equalization algorithm for this signal processing module. Compare and design two adaptive algorithms, LMS (Least Mean Square) and DLMS (Delayed Least Mean Square). LMS algorithm has better convergence effect than DLMS algorithm, and the calculation efficiency is lower than the DLMS algorithm based on the structure of the systolic array. The signal waveform is tested under CCIR (International Radio Consultative Committee) HF (High Frequency) channel. The experimental results show that the receiving processing module has good feasibility for signals under medium HF channels.

1. Introduction

HF communication is an effective long-distance transmission wireless communication method without relay. It is widely used in military communication because of its anti-destroy, strong anti-interference ability, flexible configuration, and low cost. The US Department of Defence proposed MIL-STD-188-110C (hereinafter referred to as the 110C protocol) HF standard specification, in which the maximum signal bandwidth is 24kHz. The signal will be affected by multipath, channel fading and Doppler frequency shift during the propagation process, resulting in inter-symbol interference and signal distortion, which makes it impossible to demodulate and judge the signal correctly.

GPU (Graphic Processing Unit), CPU (Central Processing Unit), DSP (Digital Signal Processor), FPGA (Field-Programmable Gate Array) are commonly used as signal receiving and processing platforms. The parallel processing capabilities of CPU and GPU are insufficient and need to rely on a higher computer configuration to ensure real-time signal processing. Although DSP is easier to implement in software, it processes data through serial operations and is less efficient. FPGA adopts parallel architecture to develop signal processing platform, but the development cycle is longer and the development efficiency is lower. In response to the above problems, the ARM (Advanced Reduced Instruction Set Computing Machine) + FPGA method is used to build a signal processing platform to complete the complex algorithm of the system and achieve rapid execution of instructions[1][2]. At the same time, with the rapid development of IC technology, short-wave signal processing platforms have also evolved to SoC (System on Chip) platforms that integrate ARM processors with software and hardware coordinated design, which increases the flexibility of the HF receiving and processing platform.
This paper designs and implements a Xilinx ZCU102 evaluation board-based receiving processing module for 110C protocol Appendix C signals with high transmission reliability, strong business adaptability and wide application range.

2. Principle of waveform and signal reception processing module

2.1. MIL-STD-188-110C Appendix C Waveform Definition

The 110C protocol defines a waveform with a channel bandwidth of 3kHz and a baud rate of 2400 symbols/s in Appendix C [3]. The linear modulation techniques mainly include PSK (Phase Shift Keying) and QAM (Quadrature Amplitude Modulation). Among them, the transmission rate with coding can reach 9600bps, and the transmission rate without coding can reach 12800bps. Figure 1 lists the HF signal frame structure.

![Figure 1. MIL-STD-110C Appendix C HF signal frame structure.](image)

The initial synchronization preamble shall consist of 287 symbols and a modulation method of 8PSK [4]. The first 184 symbols are pseudo-random sequences used for synchronization acquisition and frequency offset estimation. The last 103 symbols are the same as the re-insertion of the synchronization header for timing synchronization, and carry data transmission rate and interleaving information. The mini-probe sequence is a repeating Frank-Heimiller sequence that is 31 symbols in length and located after the data block and at the end of the initial synchronization preamble. It is often used for carrier frequency offset tracking.

2.2. HF signal receiving and processing module

The HF signal receiving and processing flow includes DDC (digital down-conversion), signal synchronization, signal equalization and demodulation decision. This article designs and implements digital down-conversion module, synchronization acquisition module and signal equalization module based on LMS adaptive equalization algorithm. The digital down-conversion module is one of the important modules in HF communication. By reducing the speed of HF signals, the adaptability of HF communication to different hardware processing platforms is improved. The digital down-conversion module mainly includes a digital mixer, a digitally controlled oscillator, and a decimation unit.

HF communication is easily affected by the ionosphere, and the received signal has delay spread and frequency offset. In order to obtain reliable and stable communication quality, synchronization technology is essential. Use the pseudo-random code sequence in the HF communication protocol for correlation detection, compare the correlation peak with the set threshold, determine whether the capture is successful, and get the delay information [5].

In order to overcome the crosstalk between codes, an equalization filter is used in the signal receiving process. Due to the limited duration of the burst signal and the short signal synchronization sequence, the LMS adaptive equalization algorithm with fast convergence speed, simple structure and wide application is adopted here[6]. The LMS adaptive equalization algorithm must serially update the iterative filter coefficients in a specified order in the implementation process. In order to increase the throughput of the adaptive filter, a DLMS algorithm is proposed, that is, a delay unit is introduced into the input signal and error signal, the structure of the LMS algorithm is changed, and the algorithm efficiency is improved[7]. Equation (1) is the update formula of DLMS algorithm filter coefficient.

\[
W(n+1) = W(n) - \mu e(n-m)X(n-m)
\]
$W(n)$ is the filter coefficient, $e(n)$ is the error signal, $X(n)$ is the input signal, $\mu$ is the convergence step, $m$ is the number of delay units.

3. Receiving and processing module design scheme

This paper aims at the data rate of 3200bps, carrier frequency of 1800Hz, modulation method of 8PSK, and interleaving length of 1.08s in MIL-STD-188-110C appendix C. The design and implementation of the receiving processing module based on Xilinx ZCU102 platform are completed. The number of input signal bits of this module is designed to be 16bit, the local clock is 48Mhz, and the baseband sampling rate is 12kHz.

3.1. Platform introduction

This article uses the Xilinx ZCU102 evaluation board based on the XCZU9EG chip [8]. Zynq UltraScale includes a PL (programmable logic) part and a PS (processor system) part. The PL part mainly includes CLB (Configurable Logic Blocks), RAM (Random Access Memory) and Ultra RAM, DSP (Digital Signal Processing) Blocks, and 100 Gb/s network cards. The PS part mainly includes the APU (Application Processing Unit), a quad-core ARM Cortex-A53 processor based on the ARMv8-A architecture that supports 64-bit operations. PL and PS use AXI (Advanced eXtensible Interface) protocol interface for data transmission and communication.

3.2. Architecture

The overall system design is shown in figure 2. The PL part of the XCZU9EG chip realizes signal receiving and processing, including digital down-conversion, synchronous capture and LMS adaptive equalization algorithms. The processed data is transmitted to the PS part through the AXI bus, and the data is output through the G-bit network port of the PS part in preparation for subsequent analysis of the signal. In addition, the APU of the PS part is called to control the synchronization capture module and the LMS adaptive equalization module in the PL, effectively using logic resources and improving calculation efficiency.

![Figure 2. Overall system block diagram](image)

3.3. Components

3.3.1. Digital down converter. After AD (Analog to Digital) sampling, the signal sampling rate is 48MHz, which needs to be reduced by 4000 times through a decimation filter. This article uses four IP (Intellectual Property) cores DDS (Direct Digital Synthesis) compiler, CIC (Cascaded Integrated Comb) filter, FIR (Finite Impulse Response) filter and multiplier to complete the above functions. The DDS compiler generates 18kHz sine and cosine signals, which are multiplied by a multiplier to achieve mixing. The CIC filter is used to achieve decimation and speed reduction, and the FIR filter is to reshape the decimated signal.

3.3.2. Synchronization capture. The previous 184 pseudo-random sequences of 110C Appendix C signal frame were used as local reference sequences for correlation operations. After the signal is
digitally down-converted, it enters the synchronization capture module to determine the starting position of the signal. Since the sampling multiple is 5, the baseband signal is buffered to a register with a depth of 184x5 and a width of 16bit. Take the fifth sample of the baseband signal and multiply it with the local reference sequence stored in ROM (Read-Only Memory), and use the parallel structure to complete the multiplication in one clock cycle. Finally, the result of the multiplier can be accumulated. The realization structure of the synchronization capture module is shown in Figure 3.

![Figure 3. Synchronization capture block diagram](image1)

**Figure 3.** Synchronization capture block diagram

**Figure 4.** LMS adaptive equalization block diagram

### 3.3.3 LMS adaptive equalization

According to the structure of LMS adaptive equalization algorithm, it can be divided into error calculation module, weight update module, and storage module for implementation. The components of the signal and the weight are correspondingly multiplied and accumulated, and subtracted from the reference sequence to obtain the error. Subsequently, the error is input to the weight update module to obtain the latest weight. Repeat the above calculation process until convergence. The structure of the LMS adaptive equalization algorithm is shown in Figure 4. The processing capability of the system is greatly limited by the data access capability, so when implementing the DLMS algorithm, a systolic array structure based on pipeline technology is adopted, so that both the signal output and the filter coefficient update part can be calculated at the same time, which improves the data utilization rate. The block diagram of the DLMS algorithm based on the systolic array structure is shown in Figure 5. Combining the LMS algorithm and formula (1), the DLMS algorithm output and coefficient update are deformed, and formula (2) (3) is the principle of the calculation unit [9].

\[
y_j(t - j) = \left( \sum_{k=0}^{j-1} x(t - 1 - [j - 1] - k)w_k(t - 1 - [j - 1] - k) \right) + x(t - 2 j)w_j(t - j - 1)
\]

\[
y_j(t - j) = y_j(t - j) + x(t - 2 j)w_j(t - j - 1)
\]

\[
w_j(t - j) = w_j(t - j - 1) - 2\mu e(t - N - j)x(t - N - 2 j)
\]

The delayed input signal and error signal are transmitted in a systolic manner, and the calculation result is retained in the calculation unit. The internal structure of the computing unit is shown in Figure 6.
The step size factor $\mu$ is introduced in the algorithm. Within the range of values that ensure the convergence of the mean square error, the larger the value of $\mu$, the faster the adaptation speed.

4. Experiment and result
The experimental signal adopts the signal specifications described in Part 3, and the channel model adopts the medium HF channel in the CCIR standard, in which the Doppler extension is 0.5 Hz and the multipath extension is 1.0 ms, and the signal-to-noise ratio is 20dB. During the experiment, the signal processed by each module was output to the computer through the network port for time-domain and frequency-domain analysis. In this paper, the step factor $\mu$ of adaptive equalization algorithm is 0.5, and the order of the adaptive equalization filter is 16.

4.1. Digital down converter
The result of the signal passing through the digital down conversion module is shown in the figure below. Figure 7(a) shows the comparison of the spectrum results before and after signal mixing.

The decimation multiples of the CIC filter and fir filter are 1000 and 4, respectively, the output enable frequency of the CIC filter and the data output frequency of the FIR filter in Fig. 7(b).

4.2. Synchronization capture
Using the correlation detection method to capture the digital down-conversion signal. The relevant detection results are shown in Figures 8(a) and 8(b). The correlation peak is obvious, and the delay time can be obtained directly.
4.3. LMS and DLMS adaptive equalization

The influence of the LMS equalization algorithm parameter step on the equalization. After outputting the error vector, find its corresponding squared difference. It can be seen from Figure 9(a) that the larger the step size $\mu$, the faster the convergence speed. It can be seen from Figure 9(b) that under the same conditions, the more delay units of the DLMS algorithm, the worse the convergence characteristics. LMS can be regarded as a special DLMS algorithm.

Figure 8(a). Synchronization capture

Figure 8(b). Correlation detection timing diagram

Figure 9(a). Convergence comparison of LMS equalization algorithm at different steps

Figure 9(b). The difference between LMS algorithm and DLMS algorithm

Figure 9(c). Comparison before and after equalization under CCIR medium HF channel signal
As shown in Figure 9(c). The signal pass LMS equalization algorithm can effectively compensate the influence of the CCIR standard channel on the signal.

4.4. XCZU9EG resource utilization

Table 1 shows the XCZU9EG PL resource utilization generated by Xilinx Vivado synthesis tool.

| Resource | Utilization | Available | Utilization% |
|----------|-------------|-----------|--------------|
| LUT      | 18358       | 274080    | 6.70%        |
| LUTRAM   | 6008        | 144000    | 4.17%        |
| FF       | 22569       | 548160    | 4.12%        |
| DSP      | 8           | 2520      | 0.32%        |
| IO       | 81          | 328       | 24.69%       |

5. Conclusion

This paper designs the receiving and processing module for the signal with a data rate of 3200bps and an interleaving length of 1.08s in the appendix C of 110C, and realizes the digital down-conversion module, synchronization capture module and adaptive equalization algorithm module based on Xilinx ZCU102 evaluation board. At the same time, the influence of the step size factor on the LMS adaptive equalization algorithm is analyzed. The larger the step size, the faster the algorithm convergence speed. The LMS equalization algorithm has an obvious effect on the signal equalization of the CCIR medium HF channel. The DLMS algorithm is based on the LMS algorithm by adding delay units, adjusting the algorithm structure, and sacrificing algorithm convergence to improve filter throughput. The design of the DLMS algorithm based on the systolic array structure ensures good spatial and temporal locality, and improves the pipelining capability. This paper uses an open-loop structure based on data-assisted synchronization capture algorithm to quickly capture burst signals to obtain delay information. In summary, the receiving and processing scheme has good feasibility and accuracy for 110C HF signals, and has a certain reference effect on HF design and implementation of receiving and processing based on the SoC architecture.

6. References

[1] Xinyao Q 2016 Design and implementation of software radio platform based on ZYNQ M.S. thesis p 11
[2] Yangang L 2016 FPGA-based design and implementation of software defined radio M.S. thesis p 11
[3] MIL-STD-188-110C Interoperability and performance standards for data modems 2011. p 120
[4] Tianlin W 2014 Research on key technology of MIL-STD-188-110C high-order QAM Signal demodulation M.S. thesis p 10
[5] Yingbo G 2015 Research on channel estimation and synchronization in short wave communication M.S. thesis p 37
[6] Simon H 2010 Principle of adaptive filter p 70-366
[7] Ming L 2017 Reserch on key technologies of VLSI implementation of adaptive filtering algorithm M.S. thesis p 26
[8] Xilinx Inc. 2019 ZCU102 Evaluation Board User Guide p 13 https://www.xilinx.com/support/documentation/boards_and_kits/zcu102/ug1182-zcu102-eval-bd.pdf
[9] Yangang L 2011 Research on FPGA high speed implementation of digital signal processing algorithm M.S. thesis p 61