Design of a 60-GHz receiver front-end with broadband matching techniques in 65-nm CMOS

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Abstract: A 60-GHz CMOS receiver front-end with wide IF bandwidth is presented. The receiver front-end consists of an LNA, a down-conversion mixer and an IF buffer. In order to support both channel-bonding and single-channel operations, two types of broadband inter-stage matching networks are analyzed from a new perspective and adopted in the design. Fabricated in a 65-nm CMOS process, the receiver front-end achieves wide IF bandwidth, a 39-dB gain, and a 5-dB noise figure in the high-gain mode. In Channel-2 measurement, the receiver front-end achieves a maximum 3-dB IF bandwidth of 6.83 GHz, which covers three channels and meets the channel-bonding bandwidth requirement.

Keywords: CMOS, receiver, broadband, LNA, down-conversion mixer, 60 GHz

Classification: Integrated circuits

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1 Introduction

Thanks to the wideband spectrum nature, millimeter-wave (mmWave) wireless technology has become a key enabler for the next-generation wireless communication (5G) and radar systems. With 9-GHz (i.e., 57–66 GHz) unlicensed spectrum, the 60-GHz frequency band is very suitable for short-range multi-Gb/s wireless link [1, 2]. Accordingly, a broadband receiver front-end (RFE) is needed. In particular, to further increase the data rate, a channel-bonding scheme [3] has been used in the 60-GHz band, making the broadband design more challenging. However, due to the bandwidth limit of the down-conversion mixer, 60-GHz RFEs [1, 4, 5] typically only support single-channel (i.e., 2.16 GHz) applications. In addition, to improve the output signal-to-noise ratio (SNR), the RFE should achieve a high-gain and low-noise figure (NF) performance.

To address above issues, a 60-GHz RFE suitable for the dual down-conversion architecture is presented in this paper. To meet the wide bandwidth requirement for the channel-bonding operation, two different types of inter-stage broadband matching networks are analyzed and designed in a new method, and adopted in the co-design of the LNA, mixer, and IF buffer. The presented RFE achieves maximum 3-dB IF bandwidth of 6.83 GHz, which covers the first three 60-GHz band channels.
(i.e., 57.24–63.72 GHz). In addition, it achieves a 39-dB conversion gain, and a 5-dB NF.

2 Receiver front-end architecture

Fig. 1 shows a 60-GHz dual down-conversion sliding-IF receiver architecture. The first and second LO frequencies are located at 4/5 and 1/5 of the RF center frequency respectively, making it possible to achieve low I/Q mismatch and high image rejection ratio [6]. As an essential part of the receiver, the presented RFE consists of a 3-stage LNA, a Gilbert down-conversion mixer, a 12-GHz IF buffer and a 48-GHz LO balun.

3 Circuit design

3.1 60-GHz LNA and new broadband matching method

Fig. 2 shows the schematic of the 60-GHz LNA. A 3-stage cascaded structure is employed to provide enough gain for noise suppression. The common-source (CS) topology is used because of its good noise and linearity performance [7]. To solve the amplifier stability problem and enhance its gain, the capacitive neutralization technique [8] is used in each LNA stage.

The input matching network of the LNA includes an RF input pad, a transformer and a pair of series inductors, and is optimized for two purposes: (1) a good performance trade-off for the first LNA stage in terms of available gain ($G_A$), NF and input impedance matching, as shown in Fig. 3(a); (2) minimizing its own insertion loss (IL) to reduce noise degradation. Transformer is used because of its compact layout and good common-mode rejection. Simulation results show that the
input matching network (including the pad) has an IL about 1 dB, and the first LNA stage achieves a maximum $G_A$ of 12 dB and a minimum $NF$ of 3.5 dB, as shown in Fig. 3(b). Note that the gain bandwidth is traded for high gain and low $NF$. The wide bandwidth of the RFE is achieved by the following broadband matching design.

![Fig. 3.](image)

(a) Matching strategy of the input matching network.
(b) Performance of the first LNA stage.

Basically, the amplifier gain-bandwidth product is limited by its input/output parasitic capacitance [9]. Therefore, broadband matching techniques have to be used. As shown in Fig. 4(a), $I_{out}$, $R_{out}$ and $C_{out}$ form the output equivalent circuit of the previous transistor amplifier stage, while $R_{in}$ and $C_{in}$ represent the input

![Fig. 4.](image)

(a) Inter-stage matching schematic.
(b) Output reflection coefficient trajectory of the MN with an inductor in parallel.
(c) Narrowband $S_{21}$ of this MN.
equivalent circuit of the next stage. In order to achieve conjugate matching, using an inductor in parallel is necessary to convert the capacitive $Y_{\text{out}}$ to an inductive admittance, as shown in Fig. 4(b). Furthermore, to realize ideal broadband matching, the matching network (MN) is required to create a $\Gamma_{\text{MN}}$ trajectory approximating $\Gamma_{\text{in}}^*$ at each frequency point in the target frequency band. However, placing an inductor in parallel cannot fulfill this requirement: as shown in Fig. 4(b), the $\Gamma_{\text{MN}}$ trajectory rotates clockwise with frequency (shown from 48 to 75 GHz), presenting an opposite direction to $\Gamma_{\text{in}}^*$. In this situation, the minimum mismatch loss is only obtained at one frequency (approximating 61 GHz), resulting in a narrowband $S_{21}$ performance, as shown in Fig. 4(c).

To solve the above issues, a new design method for broadband matching networks is proposed in this work. Based on the above analysis, a $\Gamma_{\text{MN}}$ trajectory following the $\Gamma_{\text{in}}^*$ direction in the inductive region is needed as shown in Fig. 5(a), which means

$$\text{Im}[Y_{\text{MN}}(\omega_2)] < \text{Im}[Y_{\text{MN}}(\omega_1)].$$

(1)
Where $Y_{MN}$ is the admittance corresponding to $\Gamma_{MN}$; $\omega_2$ and $\omega_1$ are higher and lower angular frequencies, respectively. To achieve such $Y_{MN}$ from $Y_1$ by adding an inductor $L$ in parallel, which is a necessary step to have an inductive admittance, the following condition must be satisfied for $Y_1$ considering Eq. (1).

$$\text{Im} \left[ Y_1(\omega_2) - j \frac{1}{\omega_2 L} \right] < \text{Im} \left[ Y_1(\omega_1) - j \frac{1}{\omega_1 L} \right]$$

$$\Rightarrow \text{Im} [Y_1(\omega_2)] - \frac{1}{\omega_2 L} < \text{Im} [Y_1(\omega_1)] - \frac{1}{\omega_1 L}.$$  \hspace{1cm} (2)

$$\Rightarrow \text{Im} [Y_1(\omega_2)] - \text{Im} [Y_1(\omega_1)] < \frac{1}{\omega_2 L} - \frac{1}{\omega_1 L}.$$

Where $Y_1$ is the admittance before adding $L$ in parallel. As $\omega_2 > \omega_1$,

$$\text{Im} [Y_1(\omega_2)] < \text{Im} [Y_1(\omega_1)].$$  \hspace{1cm} (3)

Fig. 5(b) shows the required trajectory of $\Gamma_{out}$ (corresponding to $Y_1$), in which the higher-frequency point locates in the anticlockwise direction along a constant conductance circle. To realize such a direction, two matching structures are adopted. Fig. 5(c) and Fig. 5(d) show two $\Gamma_{out}$ trajectories provided by a series inductor and an L-C network cascaded to $Y_{out}$ respectively, and both fulfill Eq. (3). Then, to convert $\Gamma_{out}$ to $\Gamma_{MN}$ for the impedance matching, an inductive L-matching network is used after the series inductor, creating a T-shaped matching network, as shown in Fig. 5(c); a single inductor in parallel is placed after the L-C network, forming a $\pi$-shaped matching network, as shown in Fig. 5(d). Each of the two final $\Gamma_{MN}$ trajectories follows the direction of $\Gamma_{in}$ in part and intersects itself, resulting in at least two $S_{21}$ peaks.

$\Gamma_{MN}$ trajectories can be adjusted by tuning the component values in T- and $\pi$-shaped matching networks, and therefore the $S_{21}$ flatness and center frequency can be controlled, as shown in Fig. 6. In addition, it can be seen that $\Gamma_{TMN}$ in Fig. 6(a) has a shorter in-band trajectory than $\Gamma_{PLMN}$ in Fig. 6(b). As a result, the

![Fig. 6](image-url)
$S_{21}$ curve with the T-shaped matching network has a smaller ripple and a wider frequency spacing between its two peaks, as shown in Fig. 6. The two types of matching networks are suitable for different scenarios in this design: the π-shaped matching network is better to compensate the transistor gain roll-off and the passive loss due to its larger in-band ripple, while the T-shaped one is suitable to maintain good $S_{21}$ flatness for cascaded stages.

As shown in Fig. 2, the π-shaped matching network is used in LNA last two stages to compensate the first LNA stage gain roll-off on both sides of the center frequency as shown in Fig. 3(b). It also enables easy layout routing for dc biases. Fig. 7 shows the simulated results of the broadband LNA. Its $G_A$ is higher than 22.6 dB with a 3-dB bandwidth larger than 13.5 GHz (55–68.5 GHz), and the in-band NF is about 4.5 dB.

![Fig. 7. Simulated LNA $G_A$, $S_{11}$ and NF.](image)

### 3.2 Down-conversion mixer and IF buffer

Fig. 8 shows the schematic of the down-conversion mixer and the IF buffer. In a conventional Gilbert mixer, the $g_m$ transistor drain parasitic capacitor $C_1$ and the switch transistor source parasitic $C_2$ degrade the gain and bandwidth performance. To solve this problem, a differential peaking inductor $L_{\text{ins}}$ is inserted between the $g_m$

![Fig. 8. Schematic of the down-conversion mixer, the LNA-mixer inter-stage matching network, and the IF buffer.](image)
stage and the switching quad to eliminate the parasitic effect [10]. Moreover, a broadband LO balun is used to provide LO signals $v_{LO}$ of roughly identical amplitudes in four channels.

As good gain flatness is achieved by the LNA (shown in Fig. 7), a T-shaped matching network is chosen and designed for the mixer to obtain a broadband input power, as shown in Fig. 8. To enable easy layout routing for separate dc biases of the LNA last stage and the mixer, a transformer is used to function as an inductive T-shaped network [11, 12]. Fig. 8 shows the layout of the matching network consisting of two series inductors and a transformer.

As shown in Fig. 8, a 12-GHz IF buffer is designed to drive the 50-Ω load for the measurement purpose and improve the SNR. The differential CS amplifier with the capacitive neutralization technique is used in the IF buffer to enhance the gain and ease the output matching.

To ensure a wide IF bandwidth after the frequency conversion, a $\pi$-shaped matching network is used between the mixer and the IF buffer. According to the previous analysis, the $\pi$-shaped matching network is tuned to compensate the high-frequency gain drop due to the frequency conversion and the passive intrinsic loss. Fig. 9 shows the simulated mixer-IF buffer voltage gain and the total RFE gain with a fixed LO frequency of 48 GHz. The mixer-IF buffer peak-gain frequency is tuned to 16 GHz for the gain compensation. Therefore, the RFE gain achieves good flatness below 16 GHz and starts to drop beyond it.

![Simulated gains of the mixer-IF buffer circuit and the total RFE.](image)

### 4 Measurement results

Fig. 10 presents the microphotograph of the proposed 60-GHz RFE. Fabricated in a 65-nm CMOS process, the circuit occupies a silicon area of about 1.19 mm², including all pads. The measurements are performed on a high-frequency probe station with dc pads wire bonded to a PCB.

Fig. 11 shows the S-parameter measurement results with four LO frequencies. For all four 2.16-GHz channels, the RFE conversion gains are about 39 dB. Within the first three channels, the single-channel gain ripples are less than 1.4 dB, and the 3-dB IF bandwidths are 6.81, 6.83 and 5.82 GHz respectively, covering at least two channels. Particularly, measured in Channel 2, the 3-dB IF bandwidth covers the first three channels (i.e., IF bandwidth of 8.856–15.336 GHz and RF bandwidth of 57.24–63.72 GHz), and meets the bandwidth requirement of the 3-channel bond-
The RFE gain drops in Channel 4, which agrees well with the simulated results shown in Fig. 9.

In the case of a large input signal, the RFE gain is lowered by tuning down the LNA bias voltages. Fig. 12 shows the 12-dB gain range from about 26 to 39 dB. The RFE shows wide IF bandwidth in both the high- and low-gain modes.

Fig. 13 plots the measured single-sideband (SSB) NF and input $P_{1\text{dB}}$ of the RFE. In the high-gain mode, the NF is about 5 dB and the input $P_{1\text{dB}}$ is $-33$ dBm. In the low-gain mode, the NF and the input $P_{1\text{dB}}$ increase to about 7 dB and $-19$ dBm, respectively.

Table I compares this work with state-of-the-art receivers with similar architectures. Clearly, the proposed RFE achieves the highest gain and the widest 3-dB IF bandwidth.
5 Conclusion

A broadband 60-GHz RFE is implemented in a 65-nm CMOS process, achieving a 39-dB gain and a 5-dB NF in the high-gain mode. With the proposed broadband matching method and two types of matching networks, 3-dB IF bandwidth covering three channels (i.e., IF bandwidth of 8.856–15.336 GHz and RF bandwidth of 57.24–63.72 GHz) is realized, making it possible to support both channel-bonding and single-channel applications for the high-data rate wireless link.

Table 1. Comparison of state-of-the-art receivers

|                | [13] | [14] | [15] | [16] | This work |
|----------------|------|------|------|------|-----------|
| Process        | 65 nm| 65 nm| 65 nm| 65 nm| 65 nm     |
| IF frequency (GHz) | 12   | 12   | 20   | 20   | 12        |
| Gain (dB)      | >5.6(1) | 20(2) | 35.5(2) | 16.5 | 12        |
| In-band ripple (dB) | <1.3(1) | 3    | 7*   | <1.4 | <1.4      |
| 3-dB IF BW (GHz) | <4(1)* | 2.16 | -    | <1*  | 6.83      |
| NF (dB)        | <11(1) | <8.4 | 5.6–6.5 | 5.3  | 5         |

(1)value without LNA (2)including a demodulator *graphically estimated
Acknowledgments

This work was supported in part by the National High-Tech Project of China (Grant No. 2011AA010201 and 2011AA010202) and in part by the National Nature Science Foundation of China (Grant No. 61306030 and 61674037).