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To cite this article: Qing Hua et al 2019 J. Phys.: Conf. Ser. 1168 022104

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Parasitic parameter extraction and analysis of high voltage SiC intelligent power module for three-phase motor control applications

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Abstract. Parasitic parameter extraction of intelligent power module is crucial to analyze transient noise, ground bounce, voltage and current overshoot. This paper investigates the relationship between the physical layout of a high voltage SiC intelligent power module and its equivalent circuit parasitic parameters. An accurate three-dimensional electronic structure of the high voltage SiC intelligent power module is provided and the parasitic elements are extracted from the three-dimensional physical layout model for crucial graphic patterns. Parameter extraction results are compared and studied with different parameter values of heatsink plate and copper layer in this research. The effects of different values of these two parameters on AC parasitic resistance and inductance are evaluated.

1. Introduction
Intelligent power module, with its outstanding advantages is well suited for a wide range of applications such as motor control, renewable energy, industrial control and power supplies [1]. In recent years, a variety of intelligent power modules in different configurations, packages, voltage and current classes have been designed and manufactured. Thereinto, silicon carbide (SiC) intelligent power modules belong to a newly developed series, which offers several attractive characteristics for high voltage and high power applications when compared to commonly used silicon ones [2-4].

As the power integration density getting higher and the device switching speed getting faster, it has become increasingly important to extracting the parasitic parameters of the intelligent power module in an efficient and accurate way [5-10]. This is because the performance of the intelligent power module will be affected even more seriously by these parasitic elements such as the circuit trace and bond wire resistance and inductance in the module layout. Thus, in order to optimize the system performance, it should be estimated as accurately as possible of the parasitic elements that are unavoidably suffered in the interconnection structure.

By accurate extraction of these electrical parameters, the effects of the parasitic parameters such as crosstalk, ground bounce, interconnect delays and ringing can be quantified, as well as to identify and solve EMC/EMI problems [11]. This is beneficial as the user can minimize path inductance and optimize circuit structure early before the prototype is built. As a result, an efficient and robust system for different industrial applications can be quickly designed and optimized.
In this paper, the Q3D Extractor is used to extract the parasitic parameters (AC resistance, inductance and capacitance). The parasitic parameters obtained by this research will facilitate the further circuit and system simulation studies on the transient noise, ground bounce, voltage and current overshoot under different cases. As an instance, the parasitic parameters of a high voltage SiC intelligent power module are characterized and analyzed. The high voltage SiC intelligent power module principle and parameter extraction process are illustrated and discussed in Section 2. Section 3 is devoted to demonstrating the parameter extract and sweeping results of the proposed high voltage SiC intelligent power module. Finally, the conclusions are stated in section 4.

2. Extracting and analysis of parasitic parameter for high voltage SiC intelligent power module

The research object of this paper is a 600V/30A three-phase SiC intelligent power module which we have developed for motor control applications. For convenience of analysis and research, the structure of SiC intelligent power module is presented below.

Fig. 1 shows the overall layout of 600V/30A SiC intelligent power module. The whole SiC intelligent power module has six high voltage SiC MOSFET chips and six high voltage SiC SBD chips for the inverter circuit, 32 low power devices for the logical control circuit and 18 I/O pins. It can be seen that the intelligent power module is divided into two parts: power inverter circuit unit and logical control and driving circuit unit. The power inverter circuit is constituted by six high voltage SiC MOSFET chips and six high voltage SiC SBD chips, which are soldered on six heatsink plates. It is beneficial to eliminating heat dissipated from power semiconductor chips. The module is built using a single-layer copper with the thickness of 35.56 μm and all the components are placed on the same side. Different heatsink plates are connected to the copper trace by the solder. The electrical I/O terminal pins including power pins and logical control pins are vertically soldered on the required copper layer pad. The source of the SiC MOSFET and the anode of the SiC SBD are connected to the copper trace by two interconnection bond wires with the diameter of 400 μm. The gate of the SiC MOSFET is connected to copper trace by one interconnection bond wire with the diameter of 200 μm. The logical control and driving circuit unit consists of bootstrap resistances and diodes, control and driver devices. For parasitic parameters extraction, it is necessary to extract the parasitic parameters of the critical circuits. Thus, this article only focuses on the parasitic parameter extraction of the power inverter circuit.

![Three-dimensional model of the high voltage SiC intelligent power module.](image-url)
Figure 2. Power inverter circuit schematic of the high voltage SiC intelligent power module.

The power inverter circuit schematic of the high voltage SiC intelligent power module is shown in Figure 2. The power inverter circuit consists of three phases that are in parallel connection, and each phase includes a SiC MOSFET and a SiC SBD. The three-phase full-bridge power inverter circuit converts the DC voltage to AC voltage, of which amplitude and frequency can be modulated to drive the AC motor in high efficiency. In order to sensor the output currents, six shunt resistances connected in parallel have been placed in the negative bus of the power inverter circuit.

The extraction of the parasitic parameters is implemented by Q3D Extractor. The extraction of current path parasitic parameters in the power inverter circuit can be performed step by step. When the power switch device SiC MOSFET performs the on and off operations, the current conduction path is changing accordingly. Therefore, to perform the parasitic parameters extraction, various current conducting nets must be assigned in accordance with the switching sequence of the circuit. In the power inverter circuit parasitic parameter extract, each collection of touching conductor objects separated by non-conducting materials or by the background material is treated as a net. For this case study, there are mainly three conducting paths that are of interest, the phase U, phase V and phase W loops.

Figure 3. The current paths for the copper traces of the power inverter circuit.
The current paths for the copper traces of the power inverter circuit is shown in Figure 3 (a), (c), (e), and the corresponding parts in the schematic is illustrated in Figure 3 (b), (d), (f). In order to take into thorough account of every current branch, each single-phase current conductive path is again divided into subdivisions in the calculation. After the desired conducting current nets have been assigned, source and sink are performed to extract the frequency-dependent parasitic parameters. After extracting the parasitic parameters of the crucial paths in the intelligent power module, an equivalent circuit that represented by the connection of parasitic elements is obtained, which is shown in Figure 4.

![Figure 4. Equivalent circuit model of the power inverter circuit.](image)

### 3. Results and Discussion

Through the above three-dimensional physical layout modelling and analysis, the parasitic parameters have been extracted and summarized in Table 1 below.

| Current path | Resistance (mΩ) | Inductance (nH) | Capacitance (pF) |
|--------------|-----------------|-----------------|------------------|
| P-PW         | 0.87            | 16.2            | 0.48             |
| PW-PV        | 0.44            | 6.3             | 0.34             |
| PV-PU        | 0.14            | 3.5             | 0.3              |
| PW-D1        | $1.332 \times 10^{-3}$ | 0.037          | 0.34             |
| PV-D2        | $1.332 \times 10^{-3}$ | 0.037          | 0.34             |
| PU-D3        | $1.332 \times 10^{-3}$ | 0.037          | 0.34             |
| S3-W’        | 0.12            | 3.97            | 0.22             |
| S2-V’        | 0.09            | 2.95            | 0.22             |
| S1-U’        | 0.14            | 4.04            | 0.37             |
| W’-W         | 0.14            | 1.98            | 0.32             |
| V’-V         | 0.28            | 4.23            | 0.18             |
| U’-U         | 0.65            | 12.6            | 0.3              |
| W’-D6        | $1.332 \times 10^{-3}$ | 0.037          | 0.34             |
| V’-D5        | $1.332 \times 10^{-3}$ | 0.037          | 0.34             |
| U’-D4        | $1.332 \times 10^{-3}$ | 0.037          | 0.34             |
| S6-NW        | 0.08            | 2.4             | 0.24             |
| S5-NV        | 0.1             | 3.4             | 0.27             |
From the parasitic parameter extraction results shown in Table 1, it can be seen that the parasitic resistances and inductances of the copper traces that utilized for the devices interconnection is dominant, which have about 0.08-2.6 mΩ resistance and 1.98-16.2 nH inductance. As the intelligent power module is connected to the circuit board, the resistance and inductance introduced by the I/O pins are approximately 0.19 mΩ and 7.3 nH, respectively. The parasitic parameters which come from heatsink plate and bond wire are within a range of a few μΩ and pH. The parasitic capacitances are normally less than 0.5 pF. Therefore, the parasitic capacitance is not a concern in this study.

In the actual implementation process, there are only few parameters are available for optimization. In order to analyze the influence of these key parameters on the parasitic resistance and inductance, parametric sweep has been carried out by varying the heatsink plate thickness, and copper layer thickness. The parametric sweep graphs of the heatsink plate thickness at different values are shown in Figure 5 and 6, respectively. Table 2 shows the effect of increase the thickness of copper layer to 70 μm on the performance of the parasitic parameters.

|        | Resistance (mΩ) | Inductance (nH) | Capacitance (pF) |
|--------|----------------|----------------|------------------|
| S4-NU  | 0.14           | 3.97           | 0.36             |
| NU-NV  | 0.14           | 2.5            | 0.18             |
| NV-NW  | 0.22           | 4.4            | 0.2              |
| NW-RS  | 2.6            | 13.7           | 0.4              |
| RS-N   | 0.14           | 2.3            | 0.32             |
| I/O Pin| 0.19           | 7.3            | 0.2              |

![Figure 5](image.png)

**Figure 5.** AC parasitic resistance of the heatsink plate under different thickness.

![Figure 6](image.png)

**Figure 6.** AC parasitic inductance of the heatsink plate under different thickness.

The Figures 5 and 6 show that the parasitic resistance and inductance are only slightly affected by the thickness of the heatsink plate. The change in resistance and inductance are from 0.66 μΩ to 2.67 μΩ and 10.7 pH to 131 pH respectively. There is about 4 times and 12.1 times variation in resistance and inductance when heatsink plate thickness changes by a factor of 4 times, but the values are still very low. Compare with the initial values shown in Table 1, it is apparent that the thicker the copper
layer, the smaller the ACR and ACL. The ACR decrease about 7%-80% and the ACL decrease about 0.7%-28%, when the copper layer increasing from 35.56 μm to 70 μm.

Table 2. Summary of the parasitic parameters of the copper traces with the thickness of 70 μm.

| Current path | Resistance (mΩ) | Inductance (nH) | Capacitance (pF) |
|--------------|-----------------|-----------------|------------------|
| P-PW         | 0.65            | 16              | 0.48             |
| PW-PV        | 0.32            | 6.18            | 0.35             |
| PV-PU        | 0.13            | 3.45            | 0.31             |
| W'-W         | 0.1             | 1.95            | 0.15             |
| V'-V         | 0.2             | 4.2             | 0.18             |
| U'-U         | 0.46            | 12.4            | 0.31             |
| NU-NV        | 0.12            | 2.2             | 0.19             |
| NV-NW        | 0.17            | 4.3             | 0.2              |
| NW-RS        | 0.53            | 9.99            | 0.4              |
| RS-N         | 0.09            | 2.23            | 0.32             |

4. Conclusions
This paper presented a general method of characterizing and analyzing the effects of parasitic parameters for high voltage SiC intelligent power module, which has made the foundation for transient noise analysis, physical layout design and electromagnetic compatibility prediction for circuit and system design. The Q3D Extractor is utilized to extract the parasitic parameters (AC resistance, inductance and capacitance). By analysing the extracted results for different cases, the element that has the most significant effect on parasitic parameters is found. Parameter extraction results are compared with different parameter values of heatsink plate and copper layer. Analysis of the parasitic parameter extraction results shows that the parasitic parameter mainly comes from the copper traces, which is related to the physical layout interconnection. The parasitic parameter values of the heatsink plates and bond wires are not a significant number compared to the copper traces.

Acknowledgments
This work was supported by the National Natural Science Foundation of China under grant number 51741706.

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