Enhanced tunneling across nanometer-scale metal-semiconductor interfaces

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We have measured electrical transport across epitaxial, nanometer-sized metal-semiconductor interfaces by contacting CoSi$_2$-islands grown on Si(111) with the tip of a scanning tunneling microscope. The conductance per unit area was found to increase with decreasing diode area. Indeed, the zero-bias conductance was found to be $\sim 10^4$ times larger than expected from downscaling a conventional diode. These observations are explained by a model, which predicts a narrower barrier for small diodes and therefore a greatly increased contribution of tunneling to the electrical transport.

Electrical transport through metal-semiconductor interfaces has received tremendous interest in the past decades, both experimentally and theoretically. Nevertheless, an important shortcoming of existing models is the restriction to infinitely extending interfaces, so that all parameters vary only in the direction perpendicular to the surface. When the interface-size enters the nanoscale regime, many of these models cease to apply. Only a few experiments addressing this topic have been reported. In none of them epitaxial interfaces were used. Scanning tunneling spectroscopy (STS) of metallic clusters on a semiconductor surface has been used to study small metal-semiconductor contacts. In addition, experiments have been carried out in which the tip of a scanning tunneling microscope (STM) was used to contact a semiconductor surface or a metallic cluster on a semiconductor surface to form a small Schottky contact. Various deviations from the large-diode models were revealed, e.g. enhanced conductance, which was interpreted as a lower effective barrier. Besides the work that addresses a single small diode directly, measurements have been carried out on many small diodes in parallel.

In this paper, we present measurements of electrical transport through an epitaxial, nanometer sized metal-semiconductor interface. We argue that the observations can be explained by a simple model for the Schottky barrier thickness in metal-semiconductor interfaces smaller than the free-carrier screening length (Debye length, $L_D$). Our model predicts an interface-size dependent barrier thickness, leading to greatly enhanced tunneling in small Schottky diodes. The CoSi$_2$/Si(111)-interface used in our experiments is among the few metal-semiconductor interfaces of which reliable Schottky barrier height (SBH) values exist, mainly because it can be grown as a virtually perfect, abrupt, epitaxial interface. The SBH in this system is 0.67 eV (for n-type Si) and has been measured with various techniques. It is therefore a nearly ideal system to study electrical properties of metal-semiconductor interfaces and has been intensely used for that purpose.

Both in our model and in the analysis of the measurements, the SBH will be considered as a given quantity, because of the well-determined character of the CoSi$_2$/Si(111) interface. We do not expect that ultra-small-size effects as reported in Ref. play a role here, due to the semi-infinite extension of the semiconductor in our experiment. The focus will be on the size and shape of the space charge region in the semiconductor. The resulting band bending gives in general rise to a potential barrier in the semiconductor, the shape of which is very important as it determines the conductance due to the various transport mechanisms (e.g. thermionic emission, tunneling) across the interface.

In a large diode (an infinite metal-semiconductor interface) the extent of the space charge layer in the semiconductor that compensates the surface charge in the metal is set by the concentration of free carriers and doping atoms. The width of this space charge layer (and thus the thickness of the barrier) is therefore generally proportional to $L_D = \sqrt{\frac{\epsilon kT}{e^2 N}}$, where $N$ is the net carrier concentration and $p$ and $n$ are the free electron and hole concentrations, respectively.

For diodes of finite size, the barrier can be much narrower. This is because any charged object (here the metallic side of the interface) with effective size $a$ at potential $V_0$ with respect to infinity gives rise to a potential that drops as $V \approx V_0 \cdot (a/r)$ when the distance $r \geq a$. Therefore the barrier thickness will be at most a few times $a$, even in the absence of free charge carriers. If there are free carriers they can only make this barrier narrower—in the same way as with the large diode—by depletion or accumulation close to the interface. If, however, the interface size is much smaller than $L_D$, this additional screening can be completely neglected. In the remainder of this paper, we use the terms “large” and “small” for diodes of which the interface size is larger or smaller than $L_D$, respectively. The crossover to this new regime of small diodes is visualized in Fig. with parameters similar to those in the experiments. This figure is based on numerical solutions of the Poisson-equation in silicon for various interface diameters. The main consequence for electrical transport is, that the narrow barrier in small diodes can make tunneling the dominant transport mechanism (instead of thermionic emission) even at very low doping levels.

Note that our description of small diodes has some similarity to that of SBH-inhomogeneities in large diodes as analyzed by Tung. There, the effect of small patches with lower SBH on the space charge region is found to
extend for only a few times the size of these patches.

All experiments were performed in an UHV system with a base pressure of $5 \cdot 10^{-11}$ mbar. About 0.3 monolayers of Co atoms were evaporated onto a clean, 7 × 7-reconstructed Si(111) surface which was held at room temperature. Then the sample was subsequently annealed at 500°C and 800°C, both for about 5 min, so that hexagon-shaped epitaxial CoSi$_2$-islands were formed (Fig. 2(a), inset) $^{[19]}$. The height of the islands ranged from 2–4 nm (with respect to the silicon surface), while the diameters were in the range 15–30 nm. The inter-island distances were much larger than the island diameters. Next, the Si-surface reconstruction was destroyed by exposing the surface to atomic hydrogen for 10 min, while the surface was held at 400°C. The samples used were n-type doped with resistivities of 10 Ωcm and 0.01 Ωcm, respectively. After preparation, the surface was inspected with an STM. The $I$–$V$-measurements were done (at room temperature) by positioning the STM-tip over an island and lowering it by a distance $\Delta z$, sufficient to make contact to the island (with feedback loop switched off). Then the current was measured while ramping the voltage. The value of $\Delta z$ was determined by lowering the tip at a fixed bias and measuring the current. After the expected, initial exponential increase, the current reached a constant, maximum value when it was lowered by $\sim 9$ Å. To ensure good contact, in all $I$–$V$-measurements $\Delta z = 15$ Å was used.

The $I$–$V$-measurements did hardly deteriorate the imaging quality of the STM-tip (Fig. 2(a), inset) and showed excellent reproducibility when repeated on the same island. The advantage of this type of measurement (as compared to the usual STS) is that the measurements are not dominated by the properties of the vacuum-gap, but instead it is possible to directly probe the properties of the buried metal-semiconductor interface. The electro-

![Diagram](image)

FIG. 1: The dashed lines indicate the edge of the depletion region for various disc-shaped contacts (radii ranging from 100 nm (a) to infinite (e)), taken from a numerical solution of the Poisson equation at 300 K. It clearly shows the size dependence of the depletion width for contact radii smaller than a few times $L_D$ (which is 150 nm here). The left-hand vertical axis is an axis of rotational symmetry. The SBH is 0.67 eV.
The measurements in Fig. 2(b) show that in small diodes the edges, which are not included in our simple model, linear, which is presumably due to the contribution of conductance (see Fig. 2(a)). The observed scaling is not a larger diode area leads straightforwardly to a larger resistance of the bulk semiconductor. In small diodes, the exponential increase, the current is limited by the serial resistance of the bulk semiconductor. In small diodes, the current at forward (negative) bias is smaller than at reverse bias) [20]. We found that the observed behavior can be explained qualitatively by considering the small diode as a ballistic point contact and furthermore by taking into account Fowler-Nordheim tunneling from the diode’s edges at positive sample bias.

In conclusion, we have measured electrical transport through epitaxial nanometer scale metal-semiconductor interfaces. Both the observed high zero-bias conduction and the dependence of the zero-bias conduction on the diode area support our model for the extent of the space charge region for interface sizes smaller than the free carrier screening length. This phenomenon provides a way to tune the Schottky barrier thickness lithographically for a fixed doping concentration, which can be useful in making tunnel contacts.

We wish to thank J. Caro for detailed discussions concerning this work and W.J. Eijsenga and W. Crans for granting us access to their “Avant! Medici” device simulation software. One of us, S. R., wishes to acknowledge fellowship support from the Royal Netherlands Academy of Arts and Sciences.

as expected: the barrier thickness is fixed by $L_D$, so that a larger diode area leads straightforwardly to a larger conductance (see Fig. 2(a)). The observed scaling is not linear, which is presumably due to the contribution of the edges, which are not included in our simple model. The measurements in Fig. 2(b) show that in small diodes the conductance per unit area decreases with increasing diode area. This is fully consistent with our model, which predicts a thicker barrier for larger interfaces.

Finally, we want to mention the behavior of small diodes at large bias. In conventional diodes, the current saturates at reverse bias. At forward bias, after the initial exponential increase, the current is limited by the serial resistance of the bulk semiconductor. In small diodes, the situation is completely different, so that it might even reverse the expected diode operation (see Fig. 2(b), inset, where the current at forward (negative) bias is smaller than at reverse bias) [20]. We found that the observed behavior can be explained qualitatively by considering the small diode as a ballistic point contact and furthermore by taking into account Fowler-Nordheim tunneling from the diode’s edges at positive sample bias.

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[19] It must be mentioned that the CoSi$_2$-islands grow into the substrate. However, the three occurring CoSi$_2$/Si(100)-facets do have the same SBH as the CoSi$_2$/Si(111) interfaces.
[20] It has been reported that a significant amount of acceptor-like impurities can be incorporated in the top layer of the substrate during sample flashing at 1200°C in UHV, effectively reversing the doping to p-type in
(initially) n-type low-doped samples. Nevertheless, the concentration of these possible p-type dopants is expected to be so low that it does not affect our main arguments.