Low Power Techniques for Digital System Design

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Abstract
The proliferation of reconfigurable hardware like (FPGAs) put a challenge in front of designers to implement fast and low powered digital designs. Main drawbacks of FPGAs are the complex circuitry which makes them less efficient as compared to ASIC (Application Specific Integrated Circuits). Although appropriate to scaling in CMOS technology reduce the power required for performing the known job, it increase clout indulgence for each part of region. At similar instant request of low power application is swelling due to increase of smart devices and increasing energy costs. Since power consumption is an extremely significant issue in digital classification of designs, so the authors have presented and analyzed some power reduction techniques that can be targeted at different levels of design hierarchy for different target platform. The authors would also discuss concept of ACPI module designed for newer operating systems, which provides basic power management facilities to save system power.

Keywords: ACPI, Clock Tree, Flattening and Factorization, Low Uncertainty Clock Tree (LUCT)

1. Introduction
Despite the continued reduction in power supply voltage, power dissipation will continue to increase as the operating frequencies. If the power dissipation of a circuit is high, the cost increases. The chip may require special packaging. The PCB cost also increases since the chip may require heat sinks or a fan etc. The space required on the board also increases. If it is mobile equipment then the battery life reduces. So it is better to have lower power dissipation. So apart from logic and timing optimization, now day’s power optimization is also employed in design flow of digital systems. The power reduction can be employed at any stage of design cycle. At architectural level, there are more sophisticated techniques are available, which provides more scope for reduction in power. Definitely, this reduction in power achieved at the expense of timing, area, or testability of the design. Voltage, frequency and power dissipation are related parameters.

\[ P = C.V^2.F \]  

(1)

It is clear from the above equation that most of the power is dissipated in the digital circuits whenever there is a transition. In synchronous circuits every clock edge will cause power dissipation. So, higher the frequency higher is the power dissipation. The majority is palpable to decrease power consumption i.e. to reduce the clock frequency and try to do more things in a single clock edge. This is opposite of pipelining¹.

2. Literature Review
Mishra S. and Verma G. presented two design techniques i.e. pipelining and parallelism, so as to minimize the power consumption at architectural level using BCD adder as a test circuit¹. Zhao P., et al., surveyed a variety of devise technique for low down power clock scheme². K. N. Vijeyakumar et al focuses on the power efficiency of the BCD adder³. O. D. Al-Khaleel focuses on making an efficient binary coded decimal digit adder. Two designs are proposed for the adder, the first design involves minimizing delay of the adder and is discussed with the help of CAD flow and the second design includes area efficiency which is discussed using LUTs. These LUTs describe the area required by the FPGA's design⁴. Pawel P., et al., analyzes following issues for reducing power-Clock Frequency, Size of Design, Multi-Domain

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Implementation, Chip area constraints. The strategies involved for this purpose are firstly, consider changes at the organization level akin to generalization of algorithms worn. Secondly, proviso the structural design is preset strive altering the logic partition, map, post and course-ploting. Finally, try enhancing the operating conditions like capacitance, frequency and supply voltage. Anderson J. H., et al., proposes a novel routing switch operates in three different manners: quick, low power or else slumber. The design is centered on three different opinions. Lamoureux J., et al., focuses on the basic techniques to decrease the authority expenditure in an FPGA. The example of the basic technique for reducing dynamic power dissipation is to use technique named clock gating in which clock is enabled off for particular part not using it and in similar way as temperature changes we can use dynamic voltage scaling technique in which supply voltage is adapted to FPGA. M. F. M. Sabri focuses on providing an efficient and simple method for varying the speed of DC motor using pulse width modulation technique. Bishwajeet Pandey et al, used latch free clock gating, clock enable and blocking input technique to reduce the power consumed by ALU on FPGA at different operating frequencies.

3. Proposed Techniques

3.1 Clock Design Considerations

The four major concerns related to design a clocking network for the digital systems are skew, power, noise and delay. Out of these four, skew and power are the most important concerns. It has been observed that for increased clock frequencies, skew may contribute over 10% of the system cycle time. Power is a directly proportional to frequency (Equation 1); it switches at every clock cycle. Clock is often a strong aggressor, so there may be a need of shielding to reduce the noise factor. In the subsequent, some solutions are provided to overcome above major concerns for designing clock network.

3.1.1 Synchronous Clock Tree

The Figure 1 presented a design a 16 bit register, in which synchronous clock is provide to all the flip-flops. Let us say, a clock generator is available to provide this clock to different flip-flops. Now if clock will be provided to every flip-flop randomly, then due to different path delay, first flip-flop will be triggered soon then the last one. Thus, creating a clock skew and violating the synchronous structure. Also due to different path delay the fan-out will be more than the specified, creating more power consumption. Hence, a new method is there to solve the above problems i.e. clock tree. This structure generates equal path delay and fulfilling the specified fan-out requirements, leads to low power consumption.

3.1.2 Low Uncertainty Clock Tree

This approach provides the insight of small insecurity clock hierarchy for clock proliferation in composite digital whittle designing process. There is a great challenge in dealing through such an incredibly lofty regularity, low down distort, plus low down inclusion setback, into arrange in the direction of close up of numerous millions of time path in a rigorous method plus to build the devise succession time small and humdrum.

3.1.2.1 LUCT Level 1

This is balanced tree architecture of towering quality from high level origin watch grid (as PLL o/p) to a transitional deposit of clock net. Its main aim should be towards distributing signals of clock for maximum area of chip from central part of PLL. Addition to that in a tie upped system clock signal is given to the input of clock pin of slab.

3.1.2.2 LUCT Level 2

LUCT is connected to remaining part of the design and for a slab this is achieve by means of custom tools provided by CTS CAE.

Figure 2 reveals that inspite of providing the information of clock distribution at sub chip level, the clock distribution at top level is enough. The technique of clock distribution provides flexibility to the designer in multi user environment or third party macro reusability. This
The same is true for second last and last sequence. So, the second topology is better from the power consumption point of view as area required is same.

3.3 Flattening and Factorization

The Figure 4 presented the concept of flattening and factorization technique. The difference in the results can be easily interpreted form the Figure 4. This is just an example in which factorization after flattening gave better results. The result may vary from case to case.

3.3.1 Flattening

Flattening\textsuperscript{12,13} is defined as renovation of various Boolean equations into sum of product of forms. Thus, flattening removes all logic structures from a design. The result of flattening is a two level, sum of product form.

\textbf{Before flattening:}
\begin{align*}
Y &= x_1 \cdot x_2 \\
x_1 &= a + b (c + f) \\
x_2 &= d + e'
\end{align*}

\textbf{After flattening:}
\begin{align*}
Y &= ad + bdc + bdf + ae' + bce' + be'f
\end{align*}

Figure 3. Two different topologies for 4-input and Gate.
Not all designs can be flattened successfully by the tools. There are following considerations for the same:

- Small designs of 10 inputs or less can always be flattened.
- Large designs having 20 or more inputs are often impossible to flatten.
- Designs whose outputs are consistently true or consistently false for most of the possible input patterns are generally easier to flatten.
- Design with many XOR and multiplexer gates, such as adders and ALUs, are generally difficult to flatten.
- For example, An N-bit XOR function produces $2^{n-1}$ terms.

### 3.3.2 Factorization

In Boolean equation, factorization can be defined as phenomenon of providing intermediate terms. This contribution results into obscure logic structure reducing the dimension of implied circuit and huge fan outs. Factorization is a process which is dependent on constraints and may vary in design such that various structure gives different levels of logic and finally our circuit becomes smaller and slower but circuit also becomes power efficient.

### 3.4 Operand Isolation

Operand isolation is one more technique to reduce power dissipation. Suppose for a given circuit the input is varying quickly, however we are concerned in production following each twenty clock periods as shown in Figure 5.

We can hold the inputs to some combinatorial circuit steady while the productivity is not in exercise, the whole utilization of power can be able to condense. The circuit in Figure 6 shows one way to do this.

A difficulty of the above method is that some of the clock setup has been lost to enable the circuit. The negative effect of operand isolation is increment in the gate count value and it also put adverse effect on the circuit timing. We can use the enable input to improve the circuit timing so that output should be available ahead of clock cycle actually latching of data.

### 3.5 Pre-Computation

The logic beneath pre-computation is to obtain a job that is executed on a huge bus of information (e.g. Comparator) plus rupture it and hooked on two parts. A diminutive pre-computed chunk and respite of the job. This ensures us for the consumption of control in the respite of the job, but the original pre-computation is suitable. Consider the case of comparator as shown in Figure 7.

In a comparator we need to compare the lower order bits only if the higher order bits are matching. So there is a scope for saving power. The circuit shown in Figure 8 provides the solution.
Here the most significant bits are compared first and the registers for lower order bits are enabled only if MSBs match. The same technique can be used in other situations also to save power.

### 3.6 ACPI Module

ACPI stands for Advanced Configuration and Power Interface which is a release trade set for power administration services. Initially targeted at personal computer. The operating system utilizes ACPI to send the required controls to the ACPI compliant hardware and observe the hardware's state as input to the power manager. It supports five global power states: working state, sleeping state, soft state and mechanical OFF state.

### 4. Design Flow

The techniques and designed mentioned above are tested on some benchmark circuits using XPower Analyzer Tool available in Xilinx 14.5 ISE targeted to Virtex-4 FPGA. The Table 1 demonstrates the comparison analysis among various techniques in terms of average power consumption. The observed power standards comprise together dynamic as well as static power. The sources of dynamic power on FPGA embrace power contribute via logic elements and memories other than those cores of DSP and input/output pins whereas static power is permanent for particular tool at a particular node. It is 59.5 mw for the device mentioned above. Therefore we had worn a predetermined static power in favor of our computation. We can clearly observe the power reduction after application of above mentioned techniques.

### 5. Results and Discussions

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### 6. Conclusion

The authors have analysed some techniques for the low power design of digital systems using benchmark circuits. Although there is some other approaches are also available but defining all the approaches in the stipulated space would have been a tedious task. So, the authors have discussed some of the prominent techniques at each level. As seen the power minimization can be targeted at different levels of design hierarchy. At system level, the newer devices being manufactured are expected to support different power modes. The newer operating systems also include an ACPI module, so that the status of the device can be monitored and appropriate power management commands can be issued to save system power.

| Benchmarks (DSP, DCT and Image) | Average Power (in mw) |
|-------------------------------|----------------------|
| Techniques Applied            | Without technique    | With technique     |
| Dir_dct                       | 447.7                | 441.5              |
| Lee_dct                       | 2015.5               | 1728.7             |
| Mcm_dct                       | 563.9                | 521.6              |
| Motion_vector_image           | 270.5                | 242.5              |
| Pr_dct                        | 1682.8               | 1433.8             |
| Sym_conv_dsp                  | 376.5                | 298.6              |

![Figure 9. Advanced configuration and power interface.](image1)

![Figure 10. Detailed design flow from RTL to GLS.](image2)
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