Leakage currents in Al₂O₃/HfO₂ multilayer high-\(k\) stacks and their modification by post-deposition annealing steps

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Abstract. Leakage currents of Al₂O₃/HfO₂ multilayer stacks deposited by atomic layer deposition in the low voltage region (0 \(\pm\) 4V) are investigated in dependence on Al₂O₃ sublayers thickness and the post-deposition annealing in two ambients (O₂, N₂). The stacks with 5cy of Al₂O₃ show highest current, compared to structures with lower (2cy) and higher (10cy) Al₂O₃ content. Oxygen treatment does not affect significantly the leakage current at low voltages, while annealing in nitrogen definitely increases it. The current follows power law dependence, \(V^n\), with \(n\) varying in the interval of about 0.6 to ~1. The application of \(\pm 12\) V pulses shift the leakage curves towards higher or lower current values depending on the polarity of the pulse. Leakage curves after the pulse stress are described either with \(V^n\) or \((V-V_t)^n\) relations depending on both pulse and measurement bias polarity. The results are found consistent with a model similar to the collective transport in array of small metal dots model in which the current is limited by the available sites for charge carriers to move on.

1. Introduction
The importance of non-volatile semiconductor memory devices for the portable electronics and computer systems has been increased dramatically in the recent years. The demands for larger amount of information storage, higher transfer rates as well as price per bit reduction fuels the further scaling down of these devices. The majority of the existing non-volatile semiconductor memories (flash memories) are based on the floating gate cell technology being in production since the early 1980s [1]. The future scaling of this technology, however, becomes problematic as it faces several significant challenges [2]. Among the various potential replacements of floating gate technology, the charge trapping memory (CTM) is clearly gaining momentum recently promising to become main-stream in the near future. CTM storage cell shares the same operational principle as floating-gate one, except for the fact that in floating gate cell the charge is stored in a special poly-Si floating gate whereas in CTM charges are kept directly in the gate dielectric, in discrete traps distributed in the dielectric band-gap. CTM was introduced in 1967 and used Si₃N₄ as a CT layer [3] but the real progress of CTM is associated with the implementation of high-\(k\) dielectrics. The high-\(k\) materials have focused researchers’ attention in the field of microelectronics since mid-1990s. The numerous studies demonstrated the trap-rich nature of these dielectrics, inferring that they are particularly suitable for the CTM applications in the nano-size memories. In fact, future generations of CTM could be realized only by implementation of high-\(k\) dielectrics in them. HfO₂ is one of the most intensively studied high-\(k\) materials, and it has been already
implemented in some advanced devices. Therefore, the possibility for its employment in other kind of microelectronics devices seems very attractive. It has been reported that HfO$_2$ possesses the necessary potential for CTM applications. It has been also suggested [4] that incorporation of Al into HfO$_2$ matrix can further improve its parameters from CTM point of view. Recently we have investigated the charge trapping in atomic layer deposited multilayered HfO$_2$/Al$_2$O$_3$ stacks, demonstrating the feasibility for employment of the stacks as CT medium, and the possibility of tailoring the CT characteristics by variation of Al$_2$O$_3$ content and thermal treatments. [5,6]. In this work we focus on leakage currents through these stacks and their dependence on the voltage pulses charging the capacitors.

2. Experimental procedure
Multilayered HfO$_2$/Al$_2$O$_3$ charge trapping stacks were deposited on p-type (100) Si wafers with resistivity 6–8 Ωcm. The substrates received standard RCA chemical cleaning prior to the deposition. The dielectric stacks were prepared by atomic layer deposition (ALD) in Savannah-100 ALD system at a temperature of 135°C. The precursors were tetrakis(dimethylamido)hafnium (TDMAH) for HfO$_2$ sublayers and trimethylaluminum (TMA) for Al$_2$O$_3$ ones. The multilayered stacks were composed of equivalent bilayer blocks of HfO$_2$ and Al$_2$O$_3$ sublayers with constant thickness; the total stack was obtained by 5 repetitions of the bilayer block. The thickness of HfO$_2$ sublayers was the same for all stacks – 20 ALD cycles, while the Al$_2$O$_3$ sublayer thickness was varied. The leakage currents of three types of stacks with Al$_2$O$_3$ sublayers thickness of 2, 5 and 10 cy (achieving this way variable Al$_2$O$_3$ content in the stack) were investigated. The samples are designated as 5x(20:10), 5x(20:5) and 5x(20:2) reflecting the number of bilayer blocks (5) and the number of HfO$_2$ and Al$_2$O$_3$ sublayer deposition cycles, respectively. The stack thicknesses, d were determined ellipsometrically and were as follows 19 nm for 5x(20:10), 16.5 nm for 5x(20:5) and 15 nm for 5x(20:2) stack. After the deposition part of the samples received rapid thermal annealing (RTA) in O$_2$ or N$_2$ at 800 °C for 1 min. The measurements were carried out on MOS capacitor structures with evaporated Al top (square, 2.25×10$^4$ cm$^2$, patterned by photolithography) and bottom electrodes. The currents were measured at room temperature with Keithley 236 SMU; in all cases the bias was applied to the Al top (gate) electrode while the Si substrate was at zero potential.

3. Results and discussion
The study of the effect of Al$_2$O$_3$ content and the post deposition annealing (PDA) on the I-V characteristics is predominantly concentrated to the low voltage region (up to ± 4V applied bias, V). (The maximum V corresponds to electric field in stack of ~ 2.1 to 2.4 MV/cm in dependence on d.) The reason behind is that at higher applied voltages the inevitable charge trapping in the stacks is influencing the I-V characteristics making it difficult to assess the impact of the Al$_2$O$_3$ content and PDA. Additionally, although the stacks sustain applying of quite high biases for times of ~ 1s [5], in the course of I-V measurements the total time under elevated V is largely increased leading to wear-out and breakdown.

Figure 1 shows the obtained current densities J of the as-deposited samples. The I-V characteristics are almost symmetrical in respect to zero bias up to ~ 3 V. At higher positive V, the slope of the curves for stacks with lower alumina amount increases implying a change of the conduction mechanism. As seen stacks with the highest Al$_2$O$_3$ content exhibit the lowest J. The decrease of alumina concentration from 10 cy to 5 cy in the bilayer block increases J about 3 times; further reduction of Al$_2$O$_3$ (to 2 cy), however, results in a drop of J to levels close to the values of samples with 10 cy Al$_2$O$_3$. The observed behavior suggests that introducing a small Al amount into HfO$_2$ matrix suppresses some of the defects present there, causing a current reduction. With the increase of Al, new defect sites tend to appear in the stack and J increases. When Al$_2$O$_3$ reach a certain critical value, the introduced Al$_2$O$_3$ starts to behave rather as a separate layer than a dopant. As the band gap of Al$_2$O$_3$ is larger than HfO$_2$ one, J through the stack is diminished. The conjecture that the impact of 10 cy Al$_2$O$_3$ is akin to the effect of well-defined Al$_2$O$_3$ layer can be deduced from the lack of a transition point in J-V curves at V>0. The electrons injected from Si substrate in this case experience not only an interfacial SiO$_2$ layer which thickness
and quality is the same for all structures but also the first Al₂O₃ sublayer.

In figure 2 the effect of PDA in N₂ or O₂ on the $J-V$ characteristics of the three kinds of stacks is shown. It is seen that O₂ annealing decreases the leakage currents at both bias polarities. The reduction is generally small at low voltages. It is more significant at positive biases higher than about 2.5 V for the samples with smaller Al₂O₃ content (2 and 5 cy). PDA in N₂ increases leakage currents in all stacks. While this increase is small for 5 cy Al₂O₃ stack, for the stack with 2 and 10 cy Al₂O₃ the leakage current is one order of magnitude or even more (depending on $V$) higher compared to their as-deposited counterparts. Consequently, the leakage currents in N₂ treated samples is lower in the 5x(20:5) stack, unlike the as-deposited ones. It should be also noted that both PDA change the shape of $I-V$ curves as well. For 5x(20:5) and 5x(20:2) stacks steeper part of $J-V$ curves at $V>2$V is not present after PDA in O₂; it is shifted to higher positive biases. The shape of leakage curves of 5x(20:10) stacks is not amended by O₂ treatment. The effect of N₂ on $I-V$ curves shape is just the opposite. For 5x(20:10) samples at $|V|>2$V slope of the curves substantially increases. Similar transformation of $I-V$ curves are detected for the other stacks as well, but only at negative biases. Investigation on the memory effect of the stacks by capacitance-voltage ($C-V$) measurements [5] suggested that RTA in O₂ significantly increases hole and electron trapping compared to the as-grown stacks while nitrogen annealing suppresses both trapings especially for the stacks with smaller Al₂O₃ content. It was also found that O₂ annealing increases the initial positive oxide charge in the structures while RTA in N₂ introduces negative initial charge. The leakage data obtained here also supports the assumption of the distinctly different effect of the annealing ambient on stacks properties. Moreover they suggest that worsening of the memory windows in N₂

![Figure 1. Leakage current characteristics of as-deposited stacks.](image1)

![Figure 2. Effect of PDA on the leakage currents of stacks with different Al₂O₃ content: a) stack with 10 cy Al₂O₃; b) 5 cy Al₂O₃ and c) 2 cy Al₂O₃. Symbols represent experimental data and solid lines fit to $J-V^n$.](image2)
treated stacks could be due to higher leakage in them. The current reduction after O2 annealing in high-
$k$ films is usually ascribed to a partial removal of oxygen vacancies [7,8], on the other hand N2 treatment
was found detrimental for $J$ [8,9]. In case of Al2O3 RTA in N2 was shown to increase also the density of
the interface states through creation of oxygen deficient defects [8] or even AlSi formation [9]. In the
present study, the nature of the traps involved in the CT memory effect [5] are not known, but there are
some indications that they are related rather to introduction of Al [4,5] than to O vacancies in HfO2 or
Al2O3. So the leakage data may be explained either by an annealing/introduction of oxygen deficient
centers and even generation of new defects upon O2/N2 annealing, respectively or by some modification
of Al-related ones. In the former case the defects involved in the low voltage conduction differ from
those associated with the CT memory effect, and in the latter, one could assume that the modification
of the Al-related defect makes it shallower energetically. Based on the $C-V$ measurements of air annealed
stacks [5] showing intermediate results, we speculate that chemical reaction involving N is highly
probable. More detailed investigations, however, are needed to clarify this issue.

The almost symmetrical $J-V$ curves (apart from the case of 5x(20:5) and 5x(20:2) under $+V$ where
change of the slope is found) suggest that conduction in the investigated voltage range is rather bulk
limited one. The $J-V$ curves are fitted well with $J-V^n$ dependence where $n$ is in the range of about 0.6–1
except for the case of 5x(20:2) stacks after RTA in N2 (figure 2). The data could be interpreted as a
manifestation of Ohmic conduction (thermally activated hopping conduction [10] where the sublinearity
arises from the fact that the voltage drop across the dielectric is affected by existing charges there and
differs from the applied bias. Alternatively, the conduction might be described with collective charge
transport in arrays of metal quantum dots [11,12]. According to this mechanism injected electrons are
transported along tunneling paths made from the traps in the stacks, and $J$ is expressed as $J \sim \left(\frac{V}{V_c}\right)^n$ (with
$n=1$ or 5/3 for 1D and 2D conduction paths; $V_c$ is a threshold voltage, characteristic of Coulomb blockage
of transport). The obtained $V_c=0$ implies negligible charge trapping during the measurements [12].
Similarly the electric field distortion in the dielectric could lead to $n$ slightly lower than 1. As pointed
earlier, the change of the slope of the $J-V$ curves for as-grown 5x(20:5) and 5x(20:2) at $V \geq 2$V and for
all N2 treated samples is indicative for a change in the dominant conduction mechanism. The estimation
of these voltage regions shows linear behavior of both $\ln(J)$ and $\ln(J/V)$ vs. $\sqrt{V}$ suggesting Schottky or
Poole-Frenkel conduction, respectively. Taking into account the relative symmetry of the curves in
respect to 0V, the conduction is most probably via Poole-Frenkel mechanism.

Next we will consider the response of the leakage characteristics to voltage pulses ($V_p$) with
amplitude of ±12V and a duration of 1s. The results are illustrated in figure 3 for one of the stacks
(5x(20:10)) and the overall trends can be described as follows. After a positive pulse the current at
positive applied $V$ diminishes and at $-V$ increases. The negative voltage pulse has an opposite effect - $J$
for $-V$ range decreases and for $+V$ region the current increases. More generally, $J$ corresponding to the
negative or positive branch of $J-V$ curve decreases after stress if $V_p$ has the same polarity. And vice
versa, $J$ of the

![Figure 3](image-url)

**Figure 3.** The response of the $J-V$ characteristics to the applied voltage pulse with amplitude ±12 V for
1s.
corresponding branch of \( J-V \) curve increases if the polarity of \( V_p \) is opposite. (Under \( +V_p \) and positive applied bias for \( J-V \) measurements electrons are injected from the Si substrate, and under \( -V_p \) and negative \( V \) at \( J-V \) recording electrons are injected from Al-gate electrode). The variation of \( J \) after the pulse stress is more pronounced at lower biases. Figure 4 summarizes the obtained relative changes of \( J \) at \( \pm 1 \) and \( \pm 2 \) V after the stress for all the samples. The current reduction for 5x(20:2) and 5x(20:10) stacks is almost the same and without clear dependence on PDA (the maximum obtained decrease of \( J \) is \( \approx 1.5 \) times for both \( V \) polarities, and it diminishes with the increase of \( V \)). As is seen the relative reduction of \( J \) of 5x(20:5) stacks for both \( V_p \) polarities is smaller as compared to other stacks, and for applied bias of 2V \( J \) becomes even higher than the initial one. Only after RTA in \( N_2 \) this stack behaves similarly to the other stacks. The increase of \( J \) in the positive bias \( J-V \) branch after applying a negative pulse (figure 4a) is larger than the \( J \) increase for the negative biases after \( +V_p \) stress (figure 4b). In the former case increase of \( J \) up to an order of magnitude is found for as-grown 5x(20:2) stacks, and in the latter the maximum increase is \( \approx 2x \) again for the 5x(20:2) stack. A clear dependence of the increase of \( J \) on the PDA as well as the \( Al_2O_3 \) content of the stacks is difficult to be traced. Nevertheless, the stacks with lower \( Al_2O_3 \) content tend to show a higher increase of \( J \) especially for the as-grown samples. For these structures PDA diminishes the current increase after pulse stress. We also note that the response of \( J-V \) curves at \( |V| \geq 2V \) to the voltage pulses of the thickest stack (5x(20:10)) treated in \( N_2 \), figure 3c diverge from the case of as-grown and \( O_2 \) annealed samples. We will also mention that changes in \( J \) upon pulsing are reversible and sustainable switching between the states with higher and lower conduction can be obtained by cycling the pulse polarity.

Figure 4. The relative change of the leakage current values after applying \( \pm 12 \) V pulses at applied biases of: a) 1 (solid line) and 2 V (dash); b) -1 (solid line) and -2V (dash).

In an effort to clarify the effect of voltage pulsing on the leakage characteristics of the stacks and evaluate the possible conduction mechanisms, the \( J-V \) curves after stress were plotted in log-log scale. Figure 5 depicts the results for 5x(20:2) stack. The \( J-V \) curves at positive biases after -12V pulse along with those at negative \( V \) after +12V pulse are well described by straight lines with slopes \( n \) in range of 0.5±0.9, implying that \( J \sim |V|^n \). The current at positive \( V \) after +12V and \( J \) at –\( V \) after -12V stress, however, are fitted with \( J \sim (|V|-V_p)^n \), where \( n \) are in the interval of 0.65±1.6, and \( |V| \) varies between 0.2 and 0.8V. A clear dependence of the values of \( n \) on the pulse stress is not observed, but for the as-grown and annealed in \( O_2 \) stacks the stress tends to reduce slightly \( n \). For the structures treated in \( N_2 \), an increase of \( n \) for the \( J \) curves at positive \( V \) after +12V pulse and at negative \( V \) after -12V pulse is found (\( n \geq 1 \) and for the 5x(20:10) stack are \( \approx 1.6 \)). The samples processed in \( N_2 \) demonstrate also lower \( V \). The obtained transition of \( J \sim |V|^n \) for the pre-stressed \( J-V \) curves towards \( J \sim (|V|-V_p)^n \) suggests that the conduction through the stacks is governed by a mechanism similar to the collective charge transport in arrays of metal quantum dots in which the role of quantum dots is taken by electron traps [11,12]. When +12V pulse is applied the injected form the substrate electrons are trapped in the stack reducing the available sites
in the conductive paths thus reducing $J$ at positive biases and shifting the $J-V$ curves by $V_t$. The electron trapping, however, is likely to be confined in the area near the injecting electrode, as evidenced by almost the same current values under positive applied biases after $+V_p$ and at negative voltage after $-V_p$ (figure 5). The observed increase of $J$ at negative biases after $+V_p$, however, suggests that during the stress electron detrapping near the opposite gate electrode occurs and the current measured at $-V$ increases and $V_t$ becomes 0. Similarly, at -12V stress the electrons are injected from the gate and are trapped near gate electrode and electrons at sites near the Si are detrapped, hence $J$ under $+V$ is increases and $J$ at $-V$ decreases and the $J-V$ curve is shifted to more negative $V$. The higher increase of $J$ at positive biases after -12V compared to the current increase at negative biases after +12V stress means that during the -12V pulse a hole substrate injection also takes place thus enhancing the detrapping process. The values of $n$ imply 1D path, but in case of PDA in N$_2$ conduction through 2D paths ($n=5/3$) after pulse stress could be assumed reflecting the higher density of the defects through which conduction takes place. The smaller values of $V_t$ for these stacks (compared to as-grown and O$_2$ annealed ones) is in an agreement with the reduced electron trapping detected from C-V investigations [5].

4. Conclusion
Leakage currents in multilayered Al$_2$O$_3$/HfO$_2$ stacks in the low voltage region are influenced by the stack composition as well as by the post deposition treatments. The results imply that depending on the amount of Al$_2$O$_3$ in the stack a reduction or increase of the leakage current levels can be obtained, i.e there is an optimum Al$_2$O$_3$ content (thickness of Al$_2$O$_3$ sublayers) providing minimum leakage currents. Additional improvement of the leakage currents can be achieved by PDA in oxidizing environment. The treatment in nitrogen, however, deteriorates the leakage currents. The origin of the effect of Al content and PDA can be sought in an elimination of existing and an introduction of new types of electronic traps predominantly in HfO$_2$. A switching between a state with higher and lower conductivity for a given bias polarity can be obtained by applying a voltage pulses with a corresponding polarity and amplitude. The observed currents are governed by a bulk limited conduction mechanism. A good agreement with the model of collective transport in an array of metal quantum dots is found, suggesting that conduction through the structures could be controlled by charging pulses.

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