EKV Model for Bulk-Driven Circuit Design Using $g_{mb}/I_D$ Method

Lukas Nagy†, Daniel Arbet, Martin Kovac, Miroslav Potocny, Robert Ondica and Viera Stopjakova
Institute of Electronics and Photonics
Faculty of Electrical Engineering and Information Technology
Slovak University of Technology
Bratislava, Slovakia
†lukas.nagy@stuba.sk

Abstract—The paper addresses a development and application of EKV MOS transistor compact model with focus on the ultra low-voltage / ultra low-power analog integrated circuit (IC) design employing bulk-driven (BD) technique. The presented contribution can be viewed as an extension of standard EKV model application and as a contribution to ultra low-voltage IC design techniques. The paper compares the measured and extracted small-signal parameters of standalone transistor samples fabricated in 130 nm CMOS technology and the simulation results obtained using the proposed bulk-driven EKV v2.63 model and foundry-provided BSIM model v3.3. The transistor samples were analyzed with power supply of $V_{DD} = 0.4$ V. The paper also discusses the implementation of 3D graphs as a result of introducing another degree of freedom into the essential MOS transistor characteristics, while maintaining the ease of using the design hand-calculation with the original $g_{mb}/I_D$ approach.

Index Terms—Bulk-Driven, Ultra Low-Voltage, Low-Power, EKV Model, Analog IC Design

I. INTRODUCTION

The current scaling of MOS transistors is governed by very well-known Moore’s law [1]. The emerging FinFET and GAAFET technologies are exceptional in terms of power efficiency per area, the scale of integration and the maximum operating frequency [2]. However, they also introduce several issues for the designers, as well as, process engineers. From the circuit designer’s point of view, the transistors produced by the cutting-edge technologies are optimized for switching purposes and are therefore, predestined mainly for high-performance (and expensive) digital systems. Analog / Mixed-Signal ICs have been designed in rather mature CMOS processes using planar transistors, such as 65 nm and (much) higher. This is caused by significantly lower cost, lower fabrication process dispersion and the transistor properties, in general. Moreover, the mature process nodes contain high-quality circuit components vital for analog design, such as resistors, capacitors, varactors, inductors, etc. The current trend of employing very low power supply voltages and lowering the overall power consumption is also supported by the recent boom of battery-powered electronic devices on the market. Furthermore, the requirements for minimized power consumption are more pronounced by the onset of on-demand IoT technology [3]. Any electronic circuit working with lowered power supply voltage or working in low-current regime, cannot be designed without accurate component models needed for circuit simulations. There have been developed numerous compact MOS transistor models describing the properties and behavior using different description approaches. For our project, we have chosen to work with $V_{DD} = 0.4$ V and EKV transistor model, which belongs to so-called inversion sheet charge model family [4], [5]. The industry standard BSIM model belongs to a group using so-called quadratic model [6]. The model created for purposes of circuit simulations has been calibrated for weak and moderate inversion levels with precise modeling of $V_{TH}$ shift due to body-effect, as well as, forward-biasing of source-bulk diode within a safe voltage range, to avoid triggering the latch-up [7], [8]. The bulk-driven (BD) design approach is employing the MOS transistor’s bulk voltage to control its parameters and there has been published several papers discussing silicon-proven bulk-driven analog IC designs [9]–[11]. The results presented in this paper are directly linked to [12], which describes the development of EKV model for bulk-driven applications and a novel extraction sequence focused on bulk-driven transistors. The article contains the comparison of measured and simulated small-signal properties of analyzed MOS transistors, as well as bulk-driven transfer characteristics with its derivatives. Furthermore, the paper also introduces bulk-driven $g_{mb}/I_D$ graph as an extension of this already established design technique.

II. EKV TRANSISTOR MODEL FOR BD CIRCUITS

The article [12] discusses the experimental background of the EKV model development. After analyzing 25 prototype chip samples fabricated in 130 nm CMOS technology, each containing standalone MOS transistors of both types and various geometries, we proceeded to processing and analyzing the data, which yielded characteristics for nominal, fast and slow transistors. Models for fast and slow transistors avail us to perform Corner Analysis during the circuit design. We also divided the modeling of MOS transistors into two separate groups (so-called binning), each accurate within a given channel length range. Transistors with the minimal (and close to minimal) channel length will be used for simulation of digital, pulse and switching circuits. The transistors with channel
lengths \( L > 1.5\mu m \) will be used in ultra low-voltage analog circuit design, in order to maximize their inversion level. Both model groups cover the threshold voltage roll-off effect [13]. This section discusses the results of extraction process performed during the bulk-driven EKV model development [14]. As a result, it compares the measured and simulated small-signal properties and the calculated discrepancies for both transistor models.

A. Sub-Threshold Current Slope - SETUP3

The first bulk-driven extraction characteristics, shown in Fig. 1, depict the drain current derivatives of MOS transistor biased into a linear regime (SETUP3 in [12]). This way, we can fine-tune the EKV model’s internal parameters responsible for modeling of the threshold voltage, body-effect factor, Fermi’s potential, transconductance factor and mobility reduction due to high vertical field (VFMR). The picture compares the measurement results obtained at room temperature with simulations using foundry-provided BSIM model and developed EKV model.

As one can observe, EKV model visually exhibits better agreement with measurement data, especially in case of source-bulk PN junction forward-bias \( V_{BD} > 0 \) \( V \) and in sub-threshold conditions. The superior accuracy of EKV model has been confirmed by median discrepancy calculated at -0.5 %, compared to 3.38 % in case of BSIM model. A simulation model precisely fitting the experimental data in this extraction setup ensures a correct modeling of drain current and transconductance in weak and moderate inversion, as well as the threshold voltage value in BD conditions.

B. Output Characteristics - SETUP4

The classic output characteristics for ultra-low voltage IC design were measured at room temperature for gate voltage stepped by 50 mV from zero to \( V_G = 0.4 \) \( V \) [12]. The derivatives of the measured drain current, or in other words, the small-signal output conductance of a MOS transistor is depicted in Fig. 2. The Y-axis is displayed in logarithmic scale. At lower \( V_G \) voltages, the measurement data become rather dispersed. That is caused by the resolution limit of our automated measurement unit. After all, the values of \( g_{ds} \) in this case are below 100 pS. The median discrepancy of simulation results with EKV model versus the measurement is 1.12 %, for BSIM model the value is -31.79 %. The achieved improvement in model accuracy is expected to provide better results in small-signal (AC) simulations. Furthermore, the described setup is also used in extraction of channel modulation coefficient and the longitudinal critical voltage, which governs the saturation voltage calculation during circuit simulations.

C. Transfer Characteristics - SETUP5

Classic transfer characteristics measured with stepped drain voltage provide data of the MOS transistor’s drain current. The derivatives of such curves display the transconductance dependency on the gate voltage. Measured and simulated transconductance characteristics are depicted in Fig. 3. Both models deliver satisfactory results. However, the proposed EKV model just provides better accuracy across the whole gate voltage range. The median discrepancy for this extraction setup was calculated at -0.36 % for EKV model and 8.64 % for BSIM model. The accuracy of EKV model can be credited to its continuous description of the drain current across the whole inversion range, as well as its derivatives. This has been confirmed by the benchmark plot of EKV model \( n = g_{ms}/I_D \) as a function of inversion coefficient (IC) and the substrate factor \( n \) as a function of gate voltage [7]. With the voltage range only up to 0.4 \( V \), we can bias the MOS devices to the verge of strong inversion, depending on its designed channel length and bias conditions. However, most of the times, the transistors employed in the circuits would work in weak inversion or moderate inversion, at best. The according gate voltage range is inherently covered more precisely by inversion sheet charge model group.

We would like to point out the improved accuracy in the linear part of the curve, which in fact describes well-known quadratic dependency of \( I_D \) in MOS transistors. More importantly, the onset of mentioned linear region also serves as a verification of the threshold voltage modeling.
III. THE BULK-DRIVEN CHARACTERISTICS

In this section of the paper, let us analyze and discuss the bulk-driven nature of the essential MOS transistor characteristics. Namely, the transfer characteristics, its derivatives and \( g_m/I_D \) ratio also known as transconductance efficiency factor (TEF). Since by sweeping/stepping of \( V_B \), we are introducing an additional degree of freedom into the characteristics, the dependencies will be displayed in 3D graphs. Fig. 4 depicts the dependency of drain current on the gate voltage and bulk voltage at constant \( V_D \). Hence, the name bulk-driven transfer characteristics. The Y-axis is set to logarithmic scale, in order to display the drain current in its whole range.

One can observe the threshold voltage shift due to changes in \( V_B \), which in fact modifies the drain current across the whole \( I_D \) plane. More positive the \( V_B \) becomes, the lower \( V_{TH} \) and higher \( I_D \) are measured, and vice versa. The strongest \( I_D \) dependency on \( V_B \) is apparently in sub-threshold (weak inversion) region as its value is modulated almost across two orders of magnitude.

The derivative of drain current, the small-signal transconductance is depicted in Fig. 5, which again, combines the dependency on both input voltages. The resulting plane, therefore, contains both transconductance components defined as \( \frac{\partial I_D}{\partial V_G} \) and \( \frac{\partial I_D}{\partial V_B} \), respectively. The threshold voltage shift is also observed, as in the previous measurement results.

The already mentioned benchmark graph of EKV transistor model is arguably the display of \( g_{ma}/I_D \) (TEF) as a function of inversion coefficient. The graph essentially combines the MOS device’s drain current, transconductance and W/L ratio. Naturally, the plot represents a powerful tool for hand-calculations and transistor sizing during the circuit design iterations. Furthermore, it can be also easily implemented in form of automated spreadsheet or application. The bulk-driven version of such a graph is depicted in Fig. 6. The \( g_{ma}/I_D \) measurement has been repeated with stepped bulk voltage. After that, the data have been post-processed and normalized for conditions when \( V_B = 0 \ V \). The presented plane expands the EKV design tool into the bulk-driven realm displaying the TEF of a MOS transistor dependent on inversion coefficient and bulk voltage. Hence, its name would be \( g_{nb}/I_D \), honoring the EKV model naming convention.

As one can observe, the sweeping of \( V_B \) causes the \( g_{nb}/I_D \) plane to deform substantially in low-voltage conditions. In weak inversion, the body-effect can actually increase the transconductance efficiency factor, while in the forward-bias conditions, it can bring TEF almost to the limit of moderate inversion. In moderate inversion (IC between 0.1 and 10), the given \( V_B \) range can modulate the resulting TEF value more than 40 %, as it can modulate IC from the onset of the moderate inversion right to its upper half.
The mentioned discoveries also serve as a justification of the bulk-driven circuit design approach as a whole, but also to the proposed research in the area of ultra low-voltage bulk-driven transistor modeling. The presented plane can be easily modeled a parameterized, which maintains the original possibility of automated or simple hand-calculations.

IV. CONCLUSION

We presented the results of experimental measurements performed on 25 silicon samples fabricated in 130 nm CMOS technology, which have been employed in ultra low-voltage bulk-driven EKV transistor model development. The final model has been used in System-on-Chip design with power supply voltage of $V_{DD} = 0.4 \text{ V}$. The bulk voltage of each transistor sample has been swept from the point of maximum body-effect to the point of maximum forward-bias. The small-signal transistor parameters have been used in the parameter extraction sequence for fine-tuning purposes. The simulation results of the proposed EKV model calibrated for bulk-driving and weak-to-moderate inversion levels, the foundry-provided BSIM model and the experimental data were also compared. In all scenarios, the proposed EKV model performed with superior accuracy, with the worst median discrepancy of 1.12%. The improvement is expected to increase the correlation between the circuit simulations and the actual measurement results obtained on silicon wafer.

The benchmark graph of EKV model has been expanded into easily parameterized 3D graph displaying the $g_{nib}/I_D$ curve as a function of inversion coefficient and $V_B$. Automated or hand-calculations for analog circuit design are therefore fully maintained. The presented work, once again, proves the robustness, versatility and accuracy of EKV transistor model. The post-processing of experimental data also proves validity of ultra low-voltage bulk-driven circuits design as bulk voltage modulation can reasonably control the operating point of a MOS transistor biased into the moderate and weak inversion. This also serves as a motivation for our future research, which includes modeling of bulk-driven MOS transistors in non-ambient temperatures, automation of EKV parameters extraction and employing the proposed model in more complex mixed-signal IC design under ultra low-voltage conditions.

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REFERENCES

[1] R. R. Tummala, “Moore’s Law for Packaging to Replace Moore’s Law for ICS,” in 2019 Pan Pacific Microelectronics Symposium (Pan Pacific), Feb 2019, pp. 1–6.
[2] Y. Huang, M. Chiang, S. Wang, and J. G. Fossum, “GAAFET Versus Pragmatic FinFET at the 5nm Si-Based CMOS Technology Node,” IEEE Journal of the Electron Devices Society, vol. 5, no. 3, pp. 164–169, May 2017.
[3] L. Wang, C. Zhan, L. He, J. Tang, G. Wang, Y. Liu, and G. Li, “A Low-Power High-PSRR CMOS Voltage Reference with Active-Feedback Frequency Compensation for IoT Applications,” in 2018 IEEE International Symposium on Circuits and Systems (ISCAS), May 2018, pp. 1–4.
[4] Binkley, D., Tradeoffs and Optimization in Analog CMOS Design. John Wiley & Sons, Limited, 2008.
[5] C. C. Enz, F. Krummenacher, and E. A. Vittoz, “An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications,” Analog Integrated Circuits and Signal Processing, vol. 8, no. 1, pp. 83–114, 1995.
[6] Y. S. Chauhan, S. Venugopalan, M. A. Karim, S. Khandelwal, N. Paydavosi, P. Thakur, A. M. Niknejad, and C. C. Hu, “BSIM — Industry standard compact MOSFET models,” in 2012 Proceedings of the ESSCIRC (ESSCIRC), Sep. 2012, pp. 30–33.
[7] L. Nagy, D. Arbet, M. Kovac, M. Potocny, M. Sovcik, and V. Stopjakova, “Ekv transistor model for ultra low-voltage bulk-driven circuits,” in 2019 17th International Conference on Emerging eLearning Technologies and Applications (ICETA), 2019, pp. 546–551.
[8] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, “Designing 1-V op amps using standard digital CMOS technology,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 7, pp. 769–780, July 1998.
[9] L. Nagy, V. Stopjakova, D. Arbet, M. Potocny, and M. Kovac, “An ultra low-voltage rail-to-rail comparator for on-chip energy harvesters,” AEU - International Journal of Electronics and Communications, vol. 108, pp. 10 – 18, 2019.
[10] V. Stopjakova, M. Rakus, M. Kovac, D. Arbet, L. Nagy, M. Sovcik, and M. Potocny, “Ultra-low voltage analog ic design: Challenges, methods and examples,” Radioengineering, vol. 27, pp. 171–185, 2018.
[11] D. Arbet, M. Kovac, L. Nagy, V. Stopjakova, and M. Sovcik, “Variable-gain amplifier for ultra-low voltage applications in 130nm cmos technology,” in 2016 39th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO), 2016, pp. 51–56.
[12] L. Nagy, D. Arbet, M. Kovac, M. Potocny, M. Sovcik, and V. Stopjakova, “Evp mos transistor model for ultra low-voltage bulk-driven ic design,” in 2021 24th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS), 2021, pp. 6–10.
[13] V. K. Singh Yadav and R. K. Baruah, “An analytic potential and threshold voltage model for short-channel symmetric double-gate mosfet,” in 18th International Symposium on VLSI Design and Test, 2014, pp. 1–2.
[14] M. Bucher, C. Lallement, and C. C. Enz, “An efficient parameter extraction methodology for the EKV MOST model,” in Proceedings of International Conference on Microelectronic Test Structures, March 1996, pp. 145–150.