Lightweight Strategy for XOR PUFs as Security Primitives for Resource-constrained IoT device

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Abstract—Physical Unclonable Functions (PUFs) are promising security primitives for resource-constrained IoT devices. And the XOR Arbiter PUF (XOR-PUF) is one of the most studied PUFs, out of an effort to improve the resistance against machine learning attacks of probably the most lightweight delay-based PUFs – the Arbiter PUFs. However, recent attack studies reveal that even XOR-PUFs with large XOR sizes are still not safe against machine learning attacks. Increasing PUF stages or components and using different challenges for different components are two ways to improve the security of APUF-based PUFs, but more stages or components lead to more hardware cost and higher operation power, and different challenges for different components require the transmission of more bits during operations, which also leads to higher power consumption. In this paper, we present a strategy that combines the choice of XOR Arbiter PUF (XOR-PUF) architecture parameters with the way XOR-PUFs are used to achieve lightweights in hardware cost and energy consumption as well as security against machine learning attacks. Experimental evaluations show that with the proposed strategy, highly lightweight component-differentially challenged XOR-PUFs can withstand the most powerful machine learning attacks developed so far and maintain excellent intra-device and inter-device performance, rendering this strategy a potential blueprint for the fabrication and use of XOR-PUFs for resource-constrained IoT applications.

Index Terms—IoT security; XOR-PUF; CDC-XPUF; machine learning modeling attack

I. INTRODUCTION

A. Overview and Motivation

The Internet of Things (IoTs) has a wide and deep participation in business and everyday life, forming a variety of networks. Many of them place a premium on security to ensure the integrity of their communications. However, many network nodes, such as sensors and IoT devices, are resource constrained and cannot support traditional cryptographic protocols, which are not lightweight. Physically Unclonable Functions (PUFs) have the potential to provide a lightweight cryptography solution to the omnipresent resource-constrained IoT. Unlike traditional methods, PUFs rely on inherent variations within integrated circuits to provide unique responses. Due to this lightweight feature, PUFs are appealing for resource-constrained IoT device identification and authentication.

PUFs can be divided into two types: weak PUFs and strong PUFs [5]. Weak PUF has a limited challenge-response pairs (CRP) space, so it is suitable for cryptographic key generation. Strong PUF, on the other hand, has an exponentially huge CRP space, which is suitable for challenge-response authentication protocols. Arbitrator PUF (APUF) and its variant, XOR Arbiter PUF (XOR-PUF), are the most common implementations of strong PUFs.

However, strong PUFs are not necessarily "strong" in terms of modeling attack resistance. Though physically unclonable, some PUFs are "mathematically clonable" in the sense that the responses of a PUF can be predicted by machine learning (ML) modeling attacks. Previous studies have demonstrated that APUF is extremely vulnerable to ML modeling attacks. And its most widely studied variant, XOR-PUF, which is proposed to improve ML modeling attack resistance, is still incapable of surviving most recent ML modeling attacks [9–16].

Increasing PUF stages or components and using different challenges for different components are two ways to improve the security of APUF-based PUFs. To begin, as the number of components or stages increases, the cost of hardware and operational power increases proportionately, rendering them unsuitable for resource-constrained IoT devices. Second, previous research [8], [17]–[19] established that XOR-PUF with different challenges for different components (CDC-XPUF) can provide significant resistance to machine learning modeling attacks within the same XOR-PUF architecture. However, the number of transmission bits required by CDC-XPUFs is high, increasing overall hardware overhead and operating power. As a result, the current CDC-XPUF design is still unsuitable for IoT devices with limited resources. Therefore, there is a rising concern that XOR-PUF designs may suffer as a result of PUF designers’ being forced to provide security at the expense of dramatically increased overhead.

To begin, as the number of components or stages increases, the cost of hardware and operational power increases proportionately, rendering them unsuitable for resource-constrained IoT devices. Second, previous research [8], [17]–[19] established that XOR-PUF with different challenges for different components (CDC-XPUF) can provide significant resistance to machine learning modeling attacks within the same XOR-PUF architecture.

In this paper, we describe a new lightweight CDC-XPUF
strategy that achieves low hardware cost and energy consumption while also providing security against ML modeling attacks. Inspired by the different effects on modeling attack resistance between components and stages, we take a different approach by combining a lightweight XOR-PUF architecture parameter strategy that reduces the number of stages while increasing the number of components with the option of using XOR-PUFs with component-differentially sub-challenges. Our experimental results show that,

- by reducing the number of stages while increasing the number of components in conventional CDC-XPUF architecture, our lightweight CDC-XPUFs can maintain high modeling attack resistance while significantly reduce up to 90% hardware cost.
- the required transmission bits of lightweight CDC-XPUFs can be reduced to the same level as traditional XOR-PUFs and still maintain exponentially many challenge-response pairs (CRPs).
- intra-device and inter-device performance evaluation on FPGA hardware implementations confirm the lightweight CDC-XPUFs could attain solid uniqueness, randomness and improved reliability performance.

B. Background Information on PUFs

In order to clarify technical discussions in later sections, we will briefly describe the mechanism of thearbiter PUF, XOR-PUF, and CDC-XPUF in this subsection.

1) The arbiter PUFs: Fig.1 shows a simple case of an arbiter PUF. A n-bit arbiter PUF is made up of n stages, each with two multiplexers (MUXs). When giving a rising signal, the signal enters the arbiter PUF from stage one and splits into two signals. The two signals are routed through gates at each stage, and the propagation paths are determined by the challenge bit to the multiplexers at each stage. Finally, two signals reach the D flip-flop, which acts as an arbiter to determine whether the signal on the top path or the signal on the lower path arrives first. If the top path signal arrives first, the D flip-flop returns 1; otherwise, it returns 0.

2) The XOR-PUFs and CDC-XPUFs: Due to arbiter PUFs' weak resistance to ML modeling attacks, a new PUF was proposed in [20] which increased a non-linear XOR gate to multiple arbiter PUFs to produce the final response. This type of PUF is known as the XOR arbiter PUF. Fig.2 illustrates a simple case of n-bit 3-XOR-PUF. An n-XOR-PUF is made up of n component arbiter PUFs (also known as streams or sub-challenge) in which the responses of all n component arbiter PUFs are XORed at XOR gate to produce one single bit response. It is worth noting that all component arbiter PUFs in an XOR-PUF are fed the same challenge bits.

Studies in [9], [10] show that XOR-PUFs could attain higher modeling attack resistance than arbiter PUFs. When equipped with lockdown scheme mutual authentication [8] to eliminate open-access interface, for XOR-PUFs with 64 stages and more than 9 component arbiter PUFs, all modeling attacks developed so far were not able to crack the XOR-PUF within the limited number of available CRPs (100 million). However, extending the number of streams and challenge stages will raise the cost and power consumption of a PUF, which is an important issue for resource-constrained IoT devices. Also, the expanding number of streams will lower the reliability of PUFs and increase the risk of reliability side-channel attacks [21].

Despite the fact that there are many alternative APUF variants and many new PUF designs proposed, such as Lightweight Secure PUFs [22], FF-PUFs [3], [23], [24], and Interpose PUF [25], to the best of our knowledge, they are still vulnerable to ML modeling attacks [26]–[30]. In this paper, we will only focus on the most widely studied APUF variant – XOR-PUFs.

For CDC-XPUFs, they share the same architecture as XOR-PUFs, which includes different multiple arbiter PUF components and XOR gates. The only difference between CDC-XPUF and XOR-PUF is that CDC-XPUF’s each different component arbiter PUF receives different challenge inputs, while the XOR-PUF receives the same challenges for all its component arbiter PUFs.

Studies [8], [17]–[19]show that applying different challenges to different components of an XOR-PUF can decrease the vulnerability of the PUF against ML modeling attacks. Existing ML attack methods for 64-bit CDC-XPUFs with four components can attain a success rate lower than 90% even if using more than one million CRPs. All the previous experimental results show that the 64-bit CDC-XPUF with four or more components is unbreakable or too expensive to
requirement of transmission bits. In this section, we will investigate a more lightweight CDC-XPUF to achieve low higher power consumption. As a result, we are motivated to mission of more bits during operations, which also leads to for different components in CDC-XPUFs require the trans-

lightweight. However, the drawback that different challenges ML modeling attack resistance and maintain the architecture presented. Finally, concluding remarks are given in section V.

CDC-XPUFs on simulator and FPGA implementations will be presented in section III. In section IV, the experimental result of security evaluation based lightweight CDC-XPUFs will be presented in section II. And the evaluation metric and tools for lightweight CDC-XPUFs design and its implementation are
described in section V.

II. LIGHTWEIGHT CDC-XPUFS DESIGN

As previously stated, CDC-XPUF is proposed to improve ML modeling attack resistance and maintain the architecture lightweight. However, the drawback that different challenges for different components in CDC-XPUFs require the transmission of more bits during operations, which also leads to higher power consumption. As a result, we are motivated to investigate a more lightweight CDC-XPUF to achieve low requirement of transmission bits. In this section, we will describe a new lightweight CDC-XPUF design strategy to reduce overall hardware cost while maintaining high ML attack resistance.

A. Factors impacting ML modeling attack resistance of APUF-based PUF

In general, there are two main factors influencing the ML modeling attack resistance of APUF-based PUF: the number of stages inside each arbiter PUF component and the number of component (the size of XOR-gate). To ensure security against ML attacks, both increasing the number of stages and increasing the number of components can improve the modeling attack resistance. However, the impact on the ML attack resistance of these two factors is not equivalent.

For the first factor, inside the arbiter PUF component, the response \( r \) of the additive delay model \([24]\), which stipulates that the time it takes for each of the two signals to arrive at the arbiter are the summation of the delays incurred at all stages of the PUF. Based on the additive delay model, can be represented as

\[
r = Sgn(v(n)) + \sum_{i=1}^{n} w(i)\phi(i),
\]

where \( \phi' \)'s are transformed challenge \([24]\) given by

\[
\phi(i) = (2c_i - 1)(2c_{i+1} - 1) \cdots (2c_m - 1),
\]

with \( c_i \) being the challenge bit at stage \( i \), \( v \) and \( w \)'s being parameters quantifying gate delays at different stages, and \( Sgn(\cdot) \) the sign function. In \([1]\), the term inside the \( Sgn(\cdot) \) function is linear with respect to the transformed challenge \( \phi' \)'s. The model represented by \([1]\) is hence a linear classification problem with the separating hyperplane represented by equation

\[
w(1)\phi(1) + w(2)\phi(2) + \cdots + w(n)\phi(n) + v(n) = 0,
\]

which results from setting to 0 the term inside the \( Sgn(\cdot) \) function in \([1]\).

For the second factor, inter the outputs from all arbiter PUF components, the response of the \( k \)-XOR arbiter PUF can be expressed as:

\[
r = \bigoplus_{j=1,k} r_j,
\]

where \( r_j \) is the internal output of the \( j^{th} \) component arbiter PUF. The XOR operation increases non-linearity of the relationship between the response \( r \) and the transformed challenges \( \phi' \)'s. Every additional arbiter PUF increases non-linearity as well as the dimension of the parameter space to be machine-learned by attackers \([10]\), leading to higher resistance against machine learning attacks \([31]\).

As a rule, an non-linear classification problem is more difficult problem than the linear classification problem. As well, based on our experience and earlier reports about PUF modeling attack resistance, the ML modeling attack resistance of XOR-PUFs grows much greater as the number of components increases compared to the number of stages. Therefore,
the number of components is a more important factor in ML modeling attack resistance of PUFs than the number of stages, while the number of stages affects attack resistance less effectively than the number of components.

B. Lightweight CDC-XPUF design

Guided by these two factors, for the purpose of maintaining high attack resistance and low hardware overhead, we could increase the number of components while decreasing the number of stages inside each component. And by this way, we are able to obtain a lightweight XOR-PUF design with high attack resistance in this manner. But as previously stated, XOR-PUFs are strong PUFs that should hold exponentially huge CRP spaces for identification and authentication applications. An $n$-stage $k$-XOR-PUF, which take the same challenge input for each component, can hold a $2^n$ available CRP space regardless of $k$. Thus, the number of challenge stages must be large for XOR-PUFs to maintain an exponentially huge CRP space. And this is the reason why the most common stage settings of traditional APUFs or XOR-PUFs are 64 or 128 bits.

However, because of the different challenges that are input into the different components of CDC-XPUFs, the available CRP space of CDC-XPUFs is much larger than that of XOR-PUFs. An $n$-stage CDC-$k$-XPUF can hold a $2^nK$ available CRP space. To make a more detailed comparison, a 64-stage CDC-XPUF with 4 sub-challenges has a $2^{644}$ available CRP space, whereas a 64-stage XOR-PUF with 4 sub-challenges has a $2^{64}$ available CRP space. And both of these two CRP spaces are large enough to fulfill the authentication protocols. If the number of stages is reduced to 16, the available CRP space for a 16-stage CDC-XPUF with 4 sub-challenges is $2^{164}$ ($2^{64}$), which is still exponentially huge, whereas a 16-stage XOR-PUF with 4 sub-challenges only has a $2^{16}$ small available CRP space. Thus, considering the practical authentication and identification applications, XOR-PUFs are not suitable for this strategy to reduce hardware overhead due to the limited available CRP space caused by the stage-decreasing. This light-weighting method could only benefit CDC-XPUFs with enough CRP space.

To conclude this section, the number of components is a more important security factor than the number of stages in terms of PUF attack resistance. This observation motivates us to implement a new setting that increases the number of components while decreasing the number of stages to achieve high attack resistance while maintaining a low hardware cost. However, this method reduces the available CRP space of XOR-PUFs for future authentication protocol applications, and it is only applicable to CDC-XPUFs with a large CRP space. To address this issue, we are inspired to design the CDC-XPUF with shorter stages and more arbiter PUF components in order to keep the hardware overhead lightweight and resistant to modeling attacks.

III. EVALUATION OF LIGHTWEIGHT CDC-XPUFS

A. Evaluation Tools for Modeling Attack Resistance

As is well known, the evaluation tool must exhibit strong attacking capabilities in order to make claims about the security of tested PUFs. We evaluate the resistance to machine learning attacks using the most powerful NN method [15], [32] and the LR-based method [9]. These methods have been widely used for PUF modeling attacking tasks and have been demonstrated to be one of the best.

To demonstrate the practical effectiveness of our evaluation tools, we start with the evaluation of these evaluation tools by applying ML modeling attack on conventional CDC-XPUFs and XOR-PUFs with the NN method and the LR-based method. Tested PUFs contain 64-bit or 128-bit usual stage length.

Ten different simulated 64-bit or 128-bit CDC-XPUF and XOR-PUF instances for each number of components setting are generated using the Pypuf simulator library and CRP generator [33]. The generated PUF instances are all from the normal distribution, with a mean of 0 and a standard deviation of 1, and no noise value was added. The experiments employ a 90-10 training-testing split, with 1% CRP from the training set used for validation. All the code is implemented in Python using the Tensorflow and Keras ML libraries [34], [35]. The codes we developed for the experimental study, including codes implementing the CDC-XPUFs based on the Pypuf library, will be made available for reproducible study by peer researchers when the paper is published.

For the convenience of reading, the parameters of the NN attack method are listed in Table I and the parameters for the LR-based method are listed in Table II. An overview figure of the LR-based method is given in Fig.4 and the overview of the NN method is given in Fig.5.

![Fig. 4. An overview of LR-based method for attacking CDC-XPUFs with component-differential-challenges](image)

The evaluation results of the NN method and LR-based method on normal-stage-length XOR-PUFs and CDC-XPUFs are listed in Table III and IV. The results show that the NN attacking method is effective for breaking XOR-PUFs. Within given CRPs, all 64-bit XOR-PUFs with less than 9 sub-challenges can be cracked. It is even possible to crack 128-bit XOR-PUFs with fewer than 8 sub-challenges. In contrast,
the LR-based method attain better performance than the NN method when attacking CDC-XPUFs. LR-based method can easily break CDC-XPUFs with 4 or 5 components and even could break 64-bit CDC-XPUFs with 6 components.

Based on the result, the evaluation tools we used are powerful enough for examining the security vulnerability of our lightweight CDC-XPUFs against ML modeling attacks.

### Table I

| Parameter              | Description                                      |
|------------------------|--------------------------------------------------|
| Optimizing Method      | ADAM                                             |
| Output Activation Function | Sigmoid                                         |
| Learning Rate          | Adaptive                                         |
| No. Neurons in Each Layer | Layer 1 = Components × Stages                     |
|                        | Layer 2 = Components × Stages/2                   |
|                        | Layer 3 = Components × Stages                    |
|                        | Layer 4 = Components × Stages                    |
| Loss Function          | Binary cross entropy                             |
| Batch Size             | $10^{k-1}$                                       |
| Kernel Initializer     | Random Normal                                    |
| Early Stopping         | True, when validation accuracy is 98%            |

### Table II

| Parameter              | Description                                      |
|------------------------|--------------------------------------------------|
| Optimizing Method      | ADAM                                             |
| Output Activation Function | Sigmoid                                         |
| Base Learning Rate     | 0.01                                             |
| Loss Function          | Binary cross entropy                             |
| Batch Size             | $10^{k-1}$                                       |
| Patience               | 5                                                |

### B. Performance Evaluation Metric for Lightweight CDC-XPUFs

When compared to conventional XOR-PUFs and CDC-XPUFs, the lightweight CDC-XPUF architecture significantly reduces the number of stages, raising the question of whether the new architecture could still achieve acceptable inter- and intra-device performance on the hardware implementation. This subsection will detail the PUF quantitative performance indicators on the hardware implementation, along with their definitions.

1) Uniqueness of Responses of Different Chips when Inputting the Same Challenges: When the PUF was first introduced in 2002, one of its most notable features was its ability to produce different responses from different devices when presented with the same challenge. This property was later referred to as the chip fingerprint or uniqueness. In order to evaluate the CDC-XPUF uniqueness, we generated CRPs from different FPGAs for the same set of challenges. We used the uniqueness proposed by Hori et al. in [36].

Hori’s uniqueness (HU), introduced in [36], calculates the uniqueness of responses of the same PUF design and challenges but from different devices. Hori’s uniqueness is defined as follows:

$$ HU_k = \frac{4}{N_c \times \log_2 N_a} \sum_{i=1}^{N} \sum_{j,m=1,j \neq m}^{N_c} (b_{j,i} \oplus b_{m,i}) $$

where $N$ is the number of chips, $N_c$ is the response length, and $b_{j,i}$ and $b_{k,i}$ are the $i$-th response bit from the $j$-th and $m$-th PUF instances respectively.

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2) Measuring PUFs Reliability: PUF outputs are expected to be persistence. However, many conditions and circumstances may affect the design reliability, such as aging, heating, and the voltage level of the input signals. To measure how correct are PUF’s outputs, we used the Steadiness metric introduce by Hori et al in [36].

An ideal PUF is expected to output the same response when is given the same single challenge on the same chip. Thus, the studying of the a PUF reliability in term of the design output is needed. The steadiness ($S$), as defined in [5], measures if the a response bit ($b$) has changed or last the same among $N_a$ times of the same challenges. The steadiness is defined as follows:

$$ S = 1 + \frac{1}{N_c} \sum_{k=1}^{N_c} \log_2 \left( \frac{\sum_{j=1}^{N_a} b_{k,j}}{N_a} - 1 - \frac{\sum_{j=1}^{N_a} b_{k,j}}{N_a} \right) $$

where $N_c$ is denotes the total number of challenges and $k$ is a single challenge.

3) Difference of Responses from the same PUF instances to Different Challenges: In terms of reaching the unpredictability of PUF’s outputs, each design is expected to produce different responses when given different challenges. If PUF’s outputs were biased to 0 or 1, it would be easy for an attacker to
guess the responses with a higher prediction rate. Thus, evaluating PUF responses in terms of randomness and steadiness, introduced in [36], is essential for guaranteeing the needed authentication and key complexity levels when using PUFs in security applications.

Randomness is the study of PUF responses balanced in terms of 0’s and 1’s. The ideal PUF is expected to produce responses that have a balance of 0’s and 1’s by 50% for each when inputting different challenges to the same chip. We can calculate the frequency of 1’s in responses of a chip for different challenges as follows:

$$p = \frac{1}{N_r} \sum_{i=1}^{N_r} b_i$$

(6)

where $N_r$ is the total number of responses and $b_i$ is the response bit. Then, Randomness ($H$) can be calculated as follows:

$$H = -\log_2 \max(p, 1-p)$$

(7)

IV. EXPERIMENTAL SETUP

A. Experiment Settings for Modeling attacks

To begin with, we evaluate the modeling attack resistance of the lightweight CDC-XPUF design with both the NN model and the LR-based model by inputting a newly generated training set of simulated CRP and then predicting responses to new challenges. To generate new datasets, we reduce the number of stages within the component from the most common 64-bit or 128-bit setting to new 8, 16, and 24 bits settings for each component, while increasing the number of arbiter PUF components to implement our lightweight CDC-XPUF design. Using the Pypuf simulator and CRP generator, we generate 20 different simulated CDC-XPUF instances for each number of components setting with the same experiment settings in section III.A.

In each attack, the number of CRPs used in the attack starts small and gradually increases until having reached a size (the size listed in the column “Training Size” in Table), which results in a 90% attack success rate for all 20 PUF instances or a failure with 100 million CRPs. And only attacks with a testing accuracy of greater than 90% are considered successful. Given that the final outputs of XOR gates may become less reliable as their size increases, we evaluate the attack resistance performance at 0%, 2%, and 5% noisiness levels to identify the performance of our lightweight CDC-XPUF design in real-world applications.

B. FPGA implementation

In our performance evaluation experiments, we programmed the different CDC-XPUFs on Xilinx Artix®-7 FPGA, which includes a configurable MicroBlaze CPU. The experiments were repeated three times on three chips to be able to capture and evaluate the responses’ uniqueness and the reliability experiments were repeated 256 times to generate 10M CRP on each instance to evaluate the steadiness performance. VHSIC Hardware Description Language (VHDL) was used to construct the CDC-XPUFs on Xilinx Vivado 15.4 HL design edition. The CDC-XPUFs placement in the hardware was done horizontally using Tool Command Language (TCL). Also, the Xilinx SDK was used to pass random challenges to the CDC-XPUFs and receive the corresponding response of each challenge.

For generating the CRPs, AXI General Purpose Input/Output (GPIO) interfaces were used as follows: 1 GPIO for submitting the initial traveling signals, 1 for receiving the output response, and the leftovers for feeding the CDC-XPUF
TABLE IV
MODELING ATTACKING PERFORMANCE EVALUATION OF THE LR-BASED METHOD

| Number of Stages | PUF Type   | Training Size | Average Accuracy | Training Time | Success Rate |
|------------------|------------|---------------|------------------|---------------|--------------|
| 64 bits          | 3 XOR-PUF  | 4k            | 95%              | 2 sec         | 100%         |
|                  | 4 XOR-PUF  | 25k           | 97%              | 10 sec        | 100%         |
|                  | 5 XOR-PUF  | 400k          | 97%              | 20 sec        | 100%         |
|                  | 6 XOR-PUF  | 2.5m          | 98%              | 2 min         | 90%          |
|                  | 7 XOR-PUF  | 10m           | 98%              | 30 min        | 90%          |
|                  | 8 XOR-PUF  | 40m           | 96%              | 1 hr          | 90%          |
|                  | 9 XOR-PUF  | 90m           | No Convergence   | 48 hrs        | 0%           |
|                  | CDC-3XPUF  | 6k            | 96%              | 10 sec        | 100%         |
|                  | CDC-4XPUF  | 80k           | 97%              | 1 min         | 100%         |
|                  | CDC-5XPUF  | 4.5m          | 96%              | 30 min        | 90%          |
|                  | CDC-6XPUF  | 100m          | 95%              | 20 hrs        | 10%          |
| 128 bits         | 3 XOR-PUF  | 10k           | 96%              | 15 sec        | 100%         |
|                  | 4 XOR-PUF  | 150k          | 96%              | 1 min         | 100%         |
|                  | 5 XOR-PUF  | 2m            | 95%              | 3 min         | 100%         |
|                  | 6 XOR-PUF  | 35m           | 97%              | 40 min        | 90%          |
|                  | 7 XOR-PUF  | 40m           | No Convergence   | 24 hrs        | 0%           |
|                  | CDC-3XPUF  | 50k           | 96%              | 10 sec        | 100%         |
|                  | CDC-4XPUF  | 450k          | 97%              | 2 min         | 100%         |
|                  | CDC-5XPUF  | 40m           | 97%              | 2 hrs         | 50%          |

with the generated challenges. Our challenges were generated using the Pseudo-Random Number Generator (PRNG) as follows:

\[ C_{n+1} = (a \times C_n + g) \mod m, \]  

where \( C \) is the sequence of the generated random number, \( a \) is a multiplier, \( g \) is a given constant, and \( m \) is \( 2^K \) where \( K \) is the number of stages. To speed up the data transfer between PUFs and the computer, AXI Universal Asynchronous Receiver Transmitter (UART) was used with baud rate equal to 230, 400 bits/second. Finally, the Tera Term, which is a terminal emulator program, used for printing and saving the device output.

Furthermore, the voltage are set to 2.0 W, and the junction temperature reported by the Xilinx Artix®-7 FPGA is 26.0°C and the Thermal maigin is 59.0°C(12.3W).

V. EXPERIMENTAL RESULTS AND DISCUSSION OF LIGHTWEIGHT CDC-XPUF

A. Results of Modeling Attack Resistance Evaluation

Firstly, the ML modeling attack experimental results for lightweight CDC-XPUF s with shorter stages are listed in Table V and Table VI. It is important to note that only attacks with greater than 90% testing accuracy can be considered successful, and the term “Accuracy” refers to the average accuracy of successful attacks. For the PUF instance with a 0% success rate, the term “Accuracy” refers to the average accuracy of all attacks.

From Table V and Table VI, the results show that lightweight CDC-XPUF s with shorter stages and more components could still achieve high resistance to modeling attack. The required CRPs to crack the previously mentioned 64-bit CDC-4-XPUFs are 80K, which is even worse than the performance of 8-bit CDC-6-XPUFs. Furthermore, the attack resistance of 64-bit CDC-5-XPUFs is lower than that of 8-bit CDC-9-XPUFs or 16-bit CDC-8-XPUFs, which require 4.5M CRPs to break. Overall, these results indicate that we can maintain high modeling attack resistance of CDC-XPUFs by acquiring shorter stages and more components architecture.

On the other hand, lightweight CDC-XPUFs with shorter stages and more components continue to dominate the exponentially large CRP space. The available CRP spaces for the lightweight CDC-XPUF design are listed in Table VII.

B. Results of Performance Evaluation

Figures 6, 7, and 9 show the performance evaluation results of some Lightweight CDC-XPUFs with exceptional high ML attack resistance based on the security results. Those PUFs are 8-CDC-XPUF 16-bit, 8-CDC-XPUF 24-bit, 9-CDC-XPUF 16-bit, 9-CDC-XPUF 24-bit, 10-CDC-XPUF 8-bit, and 10-XPUF 64-bit as a comparison. All of the chosen PUFs attain high ML attack resistance and most of them were unbreakable against our attacking model and using 100M CRPs.

1) Randomness Results: Figure [c] shows the results of calculating the difference of the PUFs responses of different challenges and devices, equations [7]. The bar-graph shows the results of the randomness. Some CDC-XPUF shows strong randomness ranged from 95% to 99%, but some PUF shows a randomness around 90%. This would be because the delays of the two selector chains are not ideally close, nevertheless equalizing the two delays is almost impracticable since the architecture of the FPGA is fixed. Nevertheless, in the face of an exponentially large available CRP space, the randomness
**TABLE V**
RESULTS OF ATTACKS ON LIGHTWEIGHT CDC-XPUF DESIGN WITH LR-BASED AND NN METHODS(PART 1)

| Components | Stages | Noise Level | Security Evaluator | Training Size | Accuracy | Success Rate |
|------------|--------|-------------|---------------------|---------------|----------|--------------|
| 6          | 8      | 0%          | NN                  | 1.8m          | 98%      | 100%         |
|            |        | 2%          | LR                  | 190k          | 99%      | 90%          |
|            |        | 5%          | LR                  | 200k          | 96%      | 100%         |
|            | 16     | 0%          | NN                  | 36m           | 98%      | 50%          |
|            |        | 2%          | LR                  | 1.5m          | 97%      | 100%         |
|            |        | 5%          | LR                  | 1.5m          | 95%      | 100%         |
|            | 24     | 0%          | NN                  | 80m           | No Convergence | 0%          |
|            |        | 2%          | LR                  | 1.8m          | 96%      | 90%          |
|            |        | 5%          | LR                  | 2.3m          | 95%      | 100%         |
|            |        | 2%          | LR                  | 2.7m          | 90%      | 90%          |
| 7          | 8      | 0%          | NN                  | 18m           | 98%      | 90%          |
|            |        | 2%          | LR                  | 1.8m          | 99%      | 100%         |
|            |        | 5%          | LR                  | 2.3m          | 94%      | 100%         |
|            | 16     | 0%          | NN                  | 100m          | No Convergence | 0%          |
|            |        | 2%          | LR                  | 2.7m          | 97%      | 90%          |
|            |        | 5%          | LR                  | 3.1m          | 94%      | 90%          |
|            | 24     | 0%          | NN                  | 100m          | No Convergence | 0%          |
|            |        | 2%          | LR                  | 35m           | 96%      | 90%          |
|            |        | 5%          | LR                  | 55m           | 95%      | 100%         |
| 9          | 8      | 0%          | NN                  | 100m          | No Convergence | 0%          |
|            |        | 2%          | LR                  | 18m           | 98%      | 90%          |
|            |        | 5%          | LR                  | 23m           | 94%      | 100%         |
|            | 16     | 0%          | NN                  | 100m          | No Convergence | 0%          |
| 10         | 8      | 0%          | LR                  | 100m          | 99%      | 10%          |
|            |        | 2%          | LR                  | 100m          | No Convergence | 0%          |

**TABLE VI**
RESULTS OF ATTACKS ON LIGHTWEIGHT CDC-XPUF DESIGN WITH LR-BASED AND NN METHODS(PART 2)

| Components | Stages | Noise Level | Security Evaluator | Training Size | Accuracy | Success Rate |
|------------|--------|-------------|---------------------|---------------|----------|--------------|
| 8          | 0%     | NN          | 100m                | 96%           | 30%      |              |
|            | 2%     | LR          | 2.3m                | 99%           | 90%      |              |
|            | 5%     | LR          | 2.7m                | 94%           | 100%     |              |
|            | 16     | 0%          | NN                  | 100m          | No Convergence | 0%          |
|            | 2%     | LR          | 60m                 | 98%           | 90%      |              |
|            | 5%     | LR          | 100m                | 95%           | 40%      |              |
|            | 24     | 0%          | NN                  | 100m          | No Convergence | 0%          |
|            | 0%     | LR          | 100m                | 88%           | 0%       |              |
| 9          | 0%     | NN          | 100m                | No Convergence | 0%          |
|            | 2%     | LR          | 18m                 | 98%           | 90%      |              |
|            | 5%     | LR          | 23m                 | 94%           | 100%     |              |
|            | 16     | 0%          | NN                  | 100m          | No Convergence | 0%          |
| 10         | 0%     | LR          | 100m                | 99%           | 10%      |              |
|            | 2%     | LR          | 100m                | No Convergence | 0%          |
Fig. 6. Calculating the difference of responses of the different challenges within the same chip. The ideal value of the Randomness is 100%.

Fig. 7. Calculating the reliability of CDC-XPUF. The ideal value of the Steadiness is 100%.

Fig. 8. The reliability performance of PUFs with shorter stage. The ideal value is 100%. The reliability decreases as the number of stages increases.

Fig. 9. Calculating the uniqueness of the CDC-XPUF using Hori’s equation. The ideal value of Hori’s equation is 100%.

The reliability of the tested PUF decrease as the number of stages increases. Therefore, the lightweight CDC-XPUF architecture with a shorter stage could help to improve the PUF reliability, which is a major expectation for an ideal PUF to output the same response when given the same single challenge on the same chip.

3) Uniqueness Results: Figure 9 demonstrates the uniqueness results which were calculated using Hori’s equation. The ideal value of the Hori’s calculation is 100%. Both CDC-XPUFs and XOR-PUFs show a uniqueness performance around 50%. Nevertheless, when considering a huge range of possible challenges such as $2^{8 \times 10}$ in the CDC-10-XPUF 8-bit, 50% of possible unique CRPs are relatively large and enough to consider the CDC-PUF in security applications.

C. Hardware cost of lightweight CDC-XPUF design

Also, as previously stated, one of the drawbacks of CDC-XPUFs is that they require more overhead to transmit more bits. But the number of required bits during transmission is dramatically reduced by shortening the number of stages and increasing the number of arbiter components in CDC-XPUFs. Table VII compares the required number of multiplexers (MUXs) and Arbiters hardware components, as well as the required transmission bits. We also include two interpose PUF instances in the comparison to evaluate the hardware cost. The results, as shown in the table, indicate that the required number of transmission bits can be reduced to an acceptable level while maintaining high modeling attack resistance. In addition, the number of MUXs and Arbiters hardware components required for the lightweight CDC-XPUF design is reduced at the same time. On the other hand, the required hardware cost for the interpose PUF is much higher, and the modeling attack resistance is not as good as that of CDC-XPUFs.

These findings provide important evidence that the shortcomings of CDC-XPUFs, which cause more overhead to transmit more bits, can be overcome. As a result, not only can we maintain high modeling attack resistance by acquiring shorter stages and more component architecture, but we can also keep hardware costs and power consumption relatively low. To take it a step further, the lightweight CDC-XPUF design is a potentially good candidate for IoT device authentication.
because it combines high modeling attack resistance with low hardware cost.

VI. CONCLUSION

In this paper, we proposed a lightweight CDC-XPUF strategy for achieving high attack resistance while keeping operation and hardware costs, which further explores the potential of the current XOR-PUF architecture. This lightweight CDC-XPUF design can withstand modeling attacks while keeping the hardware overhead to a minimum. Unlike previous studies that focused on PUFs with 64 or 128 stages in each component, our research on CDC-XPUFs with short stages discovered that reducing the number of stages while increasing the number of arbiter PUF components could achieve good modeling attack resistance while keeping CDC-XPUFs lightweight in resource requirements. As a result, while CDC-XPUFs improve attack resistance at the expense of higher transmission overhead than XOR-PUFs, the transmission cost of this lightweight CDC-XPUF design can be kept to an acceptable level. Thus, reducing the number of stages while increasing the number of sub-challenges allows CDC-XPUFs to achieve high attack resistance while maintaining a low hardware cost. Furthermore, our study on performance evaluation also reveals that our lightweight CDC-XPUF design could attain solid uniqueness, randomness and improved reliability performance. This research will provide new insights into CDC-XPUFs uniqueness, randomness and improved reliability performance.

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