Investigation of the influence of graded-gap layer formed by annealing on the electrical properties of the near-surface of LPE HgCdTe using MIS structure

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Abstract

The influence of the near-surface graded-gap layer formed by annealing of HgCdTe grown by liquid phase epitaxy on the capacitance–voltage characteristics of its MIS structure was studied. We found that HgCdTe grown by LPE can form a near-surface graded-gap layer by annealing under specific conditions after CdTe passivation. After the near-surface graded-layer is generated, the performance of the HgCdTe surface layer has been changed significantly, showing as an increase of slow states, a decrease of fixed charge and the generation of single-level trap in the band gap. Furthermore, a Fermi level pinning phenomenon have been observed on the HgCdTe with graded-gap layer, highlighting the huge density of interface traps at the edge of the band. This effect may be attributed to the electric field generated by the graded-gap layer in HgCdTe driving minority carriers away from the interface. As a result, the surface recombination velocity of minority carriers is reduced. At the same time, it inhibits the oxidation reaction on the surface and consequently reduces the accumulation of fixed charges. During the annealing process to form the graded-layer, the defect system on the surface is reorganized, and the defect aggregation produces single-level defects and higher electron traps.

1. Introduction

The pseudo-binary alloy semiconductor Hg 1-x Cd x Te (HgCdTe) remains the main material for manufacturing high-sensitivity infrared detectors because of its high-efficiency performance and mature industrial preparation process [1–4]. Unfortunately, the stability and reliability of the device are greatly affected by the surface leakage current, but the surface passivation operation of the device can effectively reduce the impact of the leakage current on the device performance [5–8]. Therefore, an important modern task is to optimize the passivation layer to reduce dark current and improve the manufacturability of high-performance HgCdTe infrared detectors [1, 4]. Liquid Phase Epitaxy (LPE) is currently a widely used growth method for HgCdTe materials. Compared with other growth technologies, the liquid phase epitaxy technology of HgCdTe material has irreplaceable advantages in light response performance, preparation cost, growth of doped materials, etc [9]. There are many process technologies developed around the liquid phase epitaxy for HgCdTe. Considering the mother liquor, it is divided into two technologies: tellurium-rich and mercury-rich; considering the process method, it is divided into horizontal sliding method, vertical dipping method and tipping method. Three liquid phase epitaxy technologies have all been successful: Sofradir in France uses the tellurium-rich horizontal sliding technology as the mainstream technology for the second-generation detector materials [10, 11]. The DRS company in the United States uses the tellurium-rich vertical dipping technology to grow thicker mercury cadmium telluride materials for the development of ring-hole structure (HDVIP) infrared focal plane detectors, and has achieved good results [12]. Teledyne uses the tellurium-rich tipping technology as the mainstream method for growing mercury cadmium telluride materials [13].
Because CdTe’s chemical composition, lattice constant, crystal structure, etc are very similar with HgCdTe, CdTe is considered the most ideal HgCdTe surface passivation material. It has stable characteristics and good adhesion to HgCdTe. In addition, the double-layer CdTe/ZnS passivation materials have good insulation properties due to their excellent physical properties, that is wide band gap. Therefore, the double-layer CdTe/ZnS passivation process is regarded as an important surface passivation technology to obtain higher performance HgCdTe infrared detectors whether in laboratory preparation or commercial applications [14, 15]. Actually, even with double-layer ZnS/CdTe passivation, dangling bonds and crystal defects which are well known to play crucial roles in atomic structures will still be created during the HgCdTe surface treatment and passivation process, thereby forming a huge amount of fixed charges and interface states. Both the fixed charge and the interface state increase the dark current inside the device and reduce the high-sensitivity and reliability of the detector. According to the previous research, when HgCdTe has a near-surface graded-gap layer, the electric field generated on its surface will reduce the recombination of carriers at the interface. Therefore, the performance of the detector is significantly improved [16–18].

In the characterization method of the properties of the passivation layers and the near-surface layers of the semiconductor, it is a convenient and universal method to prepare a metal insulator-semiconductor (MIS) structure and perform a capacitance-voltage (C-V) test on it. It has been widely used to study different semiconductors, such as silicon [19], III-V compound [20] and HgCdTe [21]. So far, there are not many experimental studies on the MIS structure of HgCdTe with a near-surface graded-gap layer, and only a small number of the research reports on the HgCdTe with a near-surface graded-gap layer grown by MBE (Molecular Beam Epitaxy). It is reported that when HgCdTe forms a near-surface graded band gap layer, the hysteresis in the C-V characteristics will increase significantly [22, 23]. With the generation of the graded-gap, the capacitance at any voltage will also decrease [24]. Reference [24] also reported that additional annealing of the MIS structure based on HgCdTe reduces the excessive charge in the passivation layer, and some samples have observed Fermi level pinning.

This paper studies the changes in the electrical properties of the interface of the LPE HgCdTe passivation layer after HgCdTe undergoes additional annealing for inter-diffusion of components to form a near-surface graded-gap layer. Through the C-V testing and analysis of MIS structure devices, the experimental results are obtained.

2. Experimental procedures

A p-type long-wave Hg_{1-x}Cd_{x}Te grown by liquid phase epitaxy with a thickness of 10 μm was used in this study. The doping density of the epitaxial layer is 1 × 10^{16} cm^{-3}, and the average cadmium composition is x = 0.225. After bromine etching, a CdTe dielectric layer with a thickness of 300 nm is coated on HgCdTe by electron beam evaporation. In order to compare the effect of the composition gradient formed by annealing on the MIS structure, the wafer is divided into two portions of Sample A and Sample B after the above process. For sample A, the thermal evaporation method was used to coat 100 nm ZnS on the crystal directly. For sample B, annealed at a certain temperature and time value in the Mercury atmosphere, and then coated with 100 nm ZnS by thermal evaporation. Figure 1 shows the schematic diagram of the electrical interface of the HgCdTe MIS structure (with and without annealing).

![Figure 1. The schematic diagram of electrical interface of the HgCdTe MIS structure (with annealing and without annealing).](image)

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which corresponds to a reverse voltage sweep; the bias voltage gradually increases from the initial negative voltage values to positive voltage values, which corresponds to a forward voltage sweep.

3. Results and discussion

The results of secondary ion mass spectrometry (SIMS) are illustrated in figure 2. It is evident from the figure that when the additional annealing process is completed, the interdiffusion area of the CdTe/HgCdTe surface will increase significantly. Due to the influence of interdiffusion, the distribution of Cd content at the interface becomes a gradient distribution instead of a step distribution. In order to investigate the changes in the electrical characteristics of this HgCdTe device which has a graded-layer formed by annealing, the capacitance–voltage test results on the MIS structure of HgCdTe which with a graded-gap layer will be studied below.

Figure 3 shows the C-V curve of the MIS structure prepared by LPE HgCdTe when the forward and reverse voltage sweeps are performed at a temperature of 77 K. The test frequency here is 1 MHz. As shown in figure 3 that the capacitance dependence exhibits obvious hysteresis, and the hysteresis loop is counterclockwise. The hysteresis is significantly enhanced after the sample is annealed. Usually, the slow state in the passivation layer
(also called the passivation layer trap) is the main reason for this situation. When a relatively large positive bias voltage is applied to the electrode, electrons in the semiconductor are injected into the trap of the passivation layer to form a positive flat band voltage; when the gate voltage is applied with a relatively large negative bias voltage, the electrons trapped in the passivation layer are released back to the semiconductor, thereby forming a negative flat band voltage. However, the reason and model for the significant increase in the hysteresis of the MIS structure with a graded-layer still need further study. It is worthwhile mentioning that when HgCdTe has a near-surface graded-gap layer, the concentration of defects near the surface will also increase significantly [23]. As a result, more hysteresis effects will be produced.

Using the existing theoretical model to calculate [25], the flat-band capacitance \( V_{FB} \) of the sample without annealing is \( 6.4 \times 10^{-12} \) F, and the corresponding flat-band voltage is \(-6.5\) V. The expression for the fixed charge density is \( N_F = \frac{-C_F(V_{ms} + V_{m1})}{qS} \), where \( C_F \) layer capacitance, \( V_{ms} \) is the work function difference between the gate metal and the semiconductor; \( q \) is the electron charge, and \( S \) is the area of the MIS structure. The only variable in our experimental samples is the flat band voltage. Figure 3 has a notable feature that the sample without annealing can only form a carrier change under a large negative bias, and the hysteresis loop shows that its flat band voltage within the range of \(-7.5\) V \( \sim \) \(6\) V, which is consistent with our theoretically calculated value of

![Figure 4](image-url)

**Figure 4.** The C-V characteristics of the MIS structure made of LPE HgCdTe at different frequencies. The MIS structure is installed in a cryogenic dewar with zero field of view (FOV) for testing. The test temperature is 77 K and the scanning voltage has forward scanning and reverse scanning. (a) HgCdTe without a graded-gap layer (b) HgCdTe with a graded-gap formed by annealing.
−6.5 V. For the annealing sample, when the initial voltage is changed to −4 V ∼ 4 V, there is still a hysteresis loop similar to that shown in figure 3, and it can be determined that the flat band voltage can be reduced within the range of −4 V ∼ 4 V. Combined with the expression of fixed charge density, it can be obtained that annealing can greatly reduce the fixed charge on the surface of the device. We believe that the process of annealing to form a graded layer effectively inhibits the oxidation reaction, thereby reducing the fixed charge formed by the oxide. Furthermore, the HgCdTe interface with a graded-gap layer will cause a change in the energy band due to the change of the Cd content, and an electric field will be generated at the interface. Then, the accumulation of charges at the interface will be driven out.

The C-V characteristics of the MIS structure made of HgCdTe at different frequencies is shown in figure 4. The MIS structure in figure 4(a) does not have a graded-gap layer, and the MIS structure in figure 4(b) has a graded-gap layer formed by annealing. It is seen that as the frequency increases from 30 kHz to 1 MHz, the capacitance of the samples is reduced. When in the depleted state, the majority of carriers in the space charge region are also depleted. In other words, there are very few carriers in the space charge region. In this case, the capacitance of the space charge region is mainly determined by the charge generated by ionization in the depletion layer. When in the inversion state, the minority carrier concentration on the surface exceeds the majority carrier concentration. Therefore, the minority carrier generation rate becomes a key factor here [25]. It can determine whether the C-V curve exhibits high-frequency behavior or low-frequency behavior. This means that both samples have fast interface states with different time constants. The fast interface state will increase the dark current of the device in terms of current-voltage characteristics. On the one hand, the fast interface state increases the surface recombination rate, leading to a decrease in the effective lifetime of minority carriers; on the other hand, the fast interface state contributes to the surface generation-recombination current. In terms of capacitance-voltage characteristics, under the excitation of an AC (alternating-current) signal, the fast interface state energy level moves up and down with the surface energy band relative to the Fermi level EF, emitting or trapping electrons into the semiconductor. When the frequency is low, the charge captured by the fast interface state can keep up with the change of the small AC signal, which contributes to the capacitance; but when the frequency is high, its contribution can be ignored, due to the time constant or relaxation time of the fast interface state cannot keep up with the small AC signal. It is also noticeable in figure 4 that a decrease of capacitance in the accumulation mode in with increasing frequency. The influence of the resistance of the epitaxial film bulk on the measured capacitance is mainly responsible for this [26].

For the graded-gap HgCdTe, only the high-frequency behavior of C-V curves is observed; while the HgCdTe without annealing is observed to a transition from low-frequency to high-frequency. Considering that many defects are formed while annealing to form a graded-gap layer, we suspect that a very high concentration of electron traps are formed during annealing process. The low frequency response in the positive gate voltage region disappears, because the carriers generated in the gate voltage response are all absorbed by the trap, which
leads to the Fermi level pinning in the forbidden band. Therefore, the Fermi level cannot be close to the conduction band and cannot form the accumulation of anti-type electrons.

Figure 4 shows that in the reverse voltage sweep, the C-V curve at different frequencies will have a special response around 8 V. We changed the starting voltage to measure the C-V characteristics of the graded layer device with the frequency of 1 MHz, and the results are shown in Figure 5. It can be seen that even though the starting voltage of the measurement is different under the same frequency, a special response still be formed near the same capacitance value. This is interpreted as a single-level trap with a large trapping cross-section.

\[ \text{defect system near the interface is rearranged} \]
\[ \text{trap to quickly capture or release carriers, resulting in a change in charge, which responds to the gate voltage and} \]
\[ \text{gap layer. When the Fermi level coincides with the trap level, the tiny movement of the Fermi level enables the} \]
\[ \text{long carrier lifetime} \]

4. Conclusion

Annealing HgCdTe passivated by CdTe under specific conditions can form a graded-gap, where HgCdTe is grown by liquid phase epitaxy. Capacitance–voltage measurements characterize the influence of the graded-gap layer on the electrical properties of the MIS structure of the LPE HgCdTe film. The experimental results show that annealing to form a graded layer can reduce the surface fixed charge and the capacitance at any voltage. The HgCdTe interface will be closer to the flat band state, due to the electric field generated by the graded-gap layer can expel the carriers at the interface. Single-level traps in the band gap layer and a significant capacitance pinning will also occur after LPE HgCdTe annealing to form a graded-gap layer. A possible reason for this change is the suppression of the oxidation reaction and the defect system near the interface has been rearranged during annealing. During the annealing to form the graded-gap layer, traps may gather at the interface. As a result, more trapped charges are generated and then more slow interface states are generated. In this paper, the MIS structure characteristics of LPE HgCdTe, which is annealed to form a graded-gap layer, are qualitatively studied, but the modeling and quantitative analysis need further research.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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