A Current Amplifier Circuit and Control Strategy Based on FPGA

Wei Gu1, Lihui Zhang2,*, Junkai Xie1, Guangnan Shi1, Haibo Zhang3, Quanqing Yu3 and Honglin Zhu3

1State Grid Zhejiang Electric Power Co., Ltd. Shaoxing Shangyu district power supply company, China
2Shaoxing University, China
3Beijing Smartchip Microelectronics Technology Company Limited, Beijing, China

*Corresponding author email: 369364865@qq.com

Abstract. With the extensive application of electric vehicles, energy storage systems and other power electronic equipment, the research on large capacity controllable current source will be an important direction in the future. This paper proposes controllable current source controlled by a full digitally hysteresis current based on field programmable gate array (FPGA), in which the single phase full bridge topology is adopted as the main circuit of current source. The two levels and three levels hysteresis current control strategies are analyzed and compared with the platform of PSCAD/EMTDC. The user defined component was adopted to realize the two difference control strategies with fortran language program. The simulation results verified that the two levels hysteresis current control strategy is much more fit for the controllable current source. Finally, a prototype is designed and fulfilled and it is controlled by the digitally controller with FPGA. The hysteresis current control is realized by FPGA controller with VHDL programming. The experimental results show that the researched hysteresis current control technology is effective for the current amplifier.

Keywords: Power quality; Current amplifier; Current source; Hysteresis current control; FPGA.

1. Introduction

Most of the voltage and current disturbance sources available in the society are based on linear amplifier circuit, mainly using high power transistor (BJT) and field effect transistor (MOS) and other amplifiers made of semiconductor device to finish certain introductions which need current and voltage output. Its advantages are as following [1-5]:

1) excellent linear control, accuracy control is very well;
2) the ability to realize arbitrary voltage and current output;

At the same time, it also has the following disadvantages [6-8]:

1) Switching devices work at linear magnification in the main circuit, resulting in big power dissipation, serious heating, and steady state operating point is easily affected by temperature drift;
2) This disturbance cannot output high power and only apply to low power machines because of capacity of the device voltage and current;

The above-mentioned low-power linear voltage and current disturbance sources are increasingly unable to adapt to the requirements of high voltage, large current and large capacity in the power system [9]. The researches is only limited to voltage source type, having little to do with current amplifier [10]. Therefore, this paper proposes a current disturbance generating device using high-power semiconductor devices working in the saturated region (i.e. switching state), which can solve the problem of excessive
power consumption caused by the semiconductor switch working in the linear amplification region, and can realize the output of large-capacity disturbance current. Supported by the National Ministry of Science and Technology support project, Power Quality Composite Control Technology and Device-Power Electronics Key Components and Major Equipment Development, combined with the high precision digital control technology, in this paper, we carry out the analysis of the selection of circuit parameters of controllable current source controlled by a full digitally hysteresis current on the basis of simulation and theory, and a single-phase current disturbance generator is designed and manufactured for experimental analysis and verification.

2. Main Circuit Topology of Current Amplifier

In order to reduce cost and improve the reliability of the device, this paper has chosen the most commonly used Single-phase full bridge structure as the main circuit structure of controllable current source, as is shown in figure 1, and selected Insulated Gate Bipolar Transistor switch as a power switch, which is characterized by excellent overload capacity and fast switching speed.

![Figure 1. Main circuit diagram of the current amplifier.](image)

3. Analysis of Traditional Analog Hysteresis Control

3.1. Two Levels Hysteresis Control Analysis

The working principle of hysteresis current two levels control is as follows: the current error signal is obtained by subtracting the inductive current and the current reference (voltage error signal), passes through hysteresis comparator to get Pulse Width Modulation (PWM) signal, the isolated and amplified drive IGBT controls the inductive current within the set positive and negative loop width (+h, -h). As is shown in figure 2, hysteresis comparator will output low power voltage when error signal is higher than (+h), converter output -1 level, inductive current decrease. Hysteresis comparator will output high power voltage when error signal is lower than (-h), converter output +1 level, inductive current increase and keep within certain range.

![Figure 2. The working principle of hysteresis current control.](image)
3.2. Three Levels Hysteresis Control Analysis
The working principle of hysteresis current three levels control is as follows: the current error signal is obtained by subtracting the inductive current and the current reference (voltage error signal), passes through hysteresis comparator to get Pulse Width Modulation (PWM) signal, the isolated and amplified drive power tube controls the inductive current within the set positive and negative loop width (+h), as is shown in figure 2(b). Hysteresis comparator do not have voltage output when the output current is in the positive half circumference and is higher than (+h), IGBT S1 and S3 or S2 and S4 on, uAB =0, inverter bridge output 0 level, inductive current decrease; hysteresis comparator output positive level when is lower than (-h), IGBT S1 and S4 on, uAB = Udc, inverter bridge output +1 level, inductive current increase, and reduce error to keep within certain range. when Current output is located in negative of circumference, the same situation occurs.

3.3. Analysis of Hysteresis Control Circuit
(a) Two levels hysteresis circuit control circuit has two states:
When IGBT S1 and S4 on, and then IGBT S3 and S4 off, the output is +1 level, and the circuit equation is as follows at that time

\[ u_{dc} = L \frac{di}{dt} + Ri_L \]  

(1)

When IGBT S1 and S4 off, and then IGBT S3 and S4 on, the output is -1 level, and the circuit equation is as follows at that time

\[ -u_{dc} = L \frac{di}{dt} + Ri_L \]  

(2)

(b). Three levels hysteresis circuit control circuit has three states:
The circuit equation is as follows when circuit work at +1 level:

\[ u_{dc} = L \frac{di}{dt} + Ri_L \]  

(3)

The circuit equation is as follows when circuit work at 0 level:

\[ 0 = L \frac{di}{dt} + Ri_L \]  

(4)

The circuit equation is as follows when circuit work at -1 level:

\[ -u_{dc} = L \frac{di}{dt} + Ri_L \]  

(5)

In the above formula (1~5), L is the total series equivalent inductance of the current source loop, and R is the total series equivalent resistance of the loop.

According to the above two control methods, the two levels hysteresis current control can be obtained, and the rate of change of the current rise and fall is basically the same; while the three levels hysteresis current control is completely different, and the circuit can work in both the +1 state and the -1 state. It is good to achieve current tracking, but when the circuit work in the 0 state, the current rate of change is greatly affected by the load, especially it cannot achieve good tracking during the current drop phase when the load is purely inductive. So it can be concluded: The control strategy of the controllable current source selects the two levels hysteresis current control pattern to better realize the current tracking function, and is less affected by the load characteristics.

3.4. Determination of Key Parameters
The sin current output from controllable current source is analyzed as an example:

\[ i = \sqrt{2} I_n \sin(\omega t) \]  

(6)
Current change rate of current source output is:

$$k_i = \frac{di}{dt} = \sqrt{2} \omega I_N \cos(\omega t)$$  \hspace{1cm} (7)

According to (7), the maximum current rate of change is:

$$k_{\text{max}} = \sqrt{2} \omega I_N$$  \hspace{1cm} (8)

According to (1), the rate of current in actual circuit is:

$$k = \frac{di_k}{dt} = \frac{u_{dc} - R i_k}{L}$$  \hspace{1cm} (9)

In order to ensure excellent current tracking introduction, the actual current change rate must be greater than the required output current change rate, so:

$$\frac{u_{dc} - R i_k}{L} > \sqrt{2} \omega I_N$$  \hspace{1cm} (10)

Usually when the output current is close to the peak, the current change rate is small. As long as the requirement can be met at the peak, the requirement can be met in the entire cycle, and the inductance parameter can be obtained:

$$L < \frac{u_{dc} - R i_k}{\sqrt{2} \omega I_N}$$  \hspace{1cm} (11)

The limitation of hysteresis current control switch, so:

$$\Delta t = \frac{L \times \Delta i}{u_{dc} - R i_k} \geq \frac{T_{\text{max}}}{2}$$  \hspace{1cm} (12)

and then another limitation factor can be obtained:

$$L \geq \frac{T_{\text{min}} (u_{dc} - R i_k)}{2 \Delta i}$$  \hspace{1cm} (13)

According to (11) and (13), based on main parameters of controllable current source, $f=50$Hz, $=100$, $R=3\Omega$, $I_N=14.1$A, the minimum switching period $=100\mu$S can determine the reactor parameter range of the current source $0.758mH \leq L < 9.1$mH, and the inductance parameter $L=1.22$mH is determined by comprehensive consideration.

4. Simulation Analysis of Hysteresis Current Control

4.1. Implementation of Custom Hysteresis Control Module Based on Fortran Language

Based on a custom function module in Power Systems Computer Aided Design (PSCAD) simulation software, and using Fortran language programming the hysteresis current control function is realized, the following table 1 gives the hysteresis current control logic and Fortran language.
Table 1. The logic control of hysteresis current control.

| Achieve hysteresis current control based on Fortan language | Two levels program | Three levels program |
|-----------------------------------------------------------|---------------------|----------------------|
|                                                           | \( f((|ref\,\,ili|)\geq h) \) then | \( f((|ref\,\,ili|)\geq 0) \) then |
|                                                           | \( pwma=0 \)       | \( pwma=0 \)         |
|                                                           | \( pwnmb=1 \)      | \( pwnmb=0 \)        |
| elseif \( ((il-|ref|)\geq h) \) then                     | \( pwma=1 \)     | else if \( ((|il|-|ref|)\geq h) \) then |
|                                                           | \( pwnmb=0 \)      | \( pwma=1 \)         |
| end if                                                     |                     | \( pwnmb=1 \)        |

IGBT states

| S1=pwma;                                         | S1=pwma;                                         |
| S2=\text{not}(pwma);                            | S2=\text{not}(pwma);                            |
| S3=pwnmb;                                       | S3=pwnmb;                                       |
| S4=\text{not}(pwnmb);                           | S4=\text{not}(pwnmb);                           |

4.2. Simulation Analysis and Comparison under Two Control Modes

Based on the above analysis and calculations, a simulation model of a controllable current source controlled by hysteresis current is established using PSCAD/EMTDC simulation software[11]. The key simulation parameters in the simulation model are shown in Table 2 below.

Table 2. Key Simulation parameter.

| reactor     | \( L=1.22\text{mH} \) |
|-------------|------------------------|
| DC bus voltage | \( u_{dc}=100\text{V} \) |
| Rated current   | \( I_{N}=14.1\text{A} \) |
| The hysteresis current width | \( h=1\text{A} \) |

| load  | \( R_{\text{c}}\leq 3\Omega \), \( L_{\text{c}}\leq 3\text{mH} \) |

The following is a simulation analysis of three different working conditions. The detailed simulation waves and data are as follows:

(a) The current source output is shorted (\( R=0\Omega \)) and output current RMS is 14.1A

The simulation waveform is shown in Figure 3, controllable current source has the smallest output capacity at that time, which is similar to the idle experiment. shown in Figure 3(a) is the output current waveform under the two levels hysteresis current control mode, which means that the current tracking effect is good throughout the whole cycle, the actual output current effective value is 14.1A(=14.1A), \( \text{THI}_{1}=3.2\% \). Besides, figure 3(b) is current output waveform under the three levels hysteresis current control, distortion of wave occurs in the positive half-cycle inductive current falling stage and the negative half-cycle inductive current rising stage, mainly because the positive half-cycle only has two working modes: +1 level and 0 level. There are no energy-consuming components in the loop when working in 0 level, so inductive current don’t drop rapidly and crack commanded current, it is similar in the negative half-cycle. At this time, the effective value of the actual output current is 15.8A, and current distortion \( \text{TH}=5.5\% \)

![Figure 3. The simulation waveform of \( R_{0}=0\Omega \), \( L_{0}=0\text{mH} \).](image-url)
(b) Current source output is connected to pure resistive load \((R_0 = 3\Omega, L_0 = 0\text{mH})\) and output current RMS is 14.1A. The simulation waveform is shown in Figure 4, which is similar to the resistive full load experiment in the voltage source. Figure (a) is the output current waveform in the two-state hysteresis current control mode, indicating that the current tracking effect is good throughout the cycle, and the actual output current \(I_{\text{rms}} = 14.1\text{A}, \text{THD}_I = 1.4\%\). Figure (b) shows the current output waveform in the three-state hysteresis current control mode. At this time, there are energy-consuming components in the loop, so the inductive current can quickly track the given current, but there is also a certain waveform at the current zero crossing. Distortion, but the waveform is greatly improved compared with no-load, \(I_{\text{rms}} = 14.1\text{A}, \text{THD}_I = 2.5\%\).

\[ \text{Figure 4. The simulation waveform of } R_0 = 3\Omega, L_0 = 0\text{mH}. \]

(c) Current source output is connected to resistance and inductance is connected load \((R_0 = 3\Omega, L_0 = 3\text{mH})\) and output current RMS is 14.1A. The simulation waveform is shown in Figure 5. At this time, the output capacity of the current source is the largest, and the resistive inductance in the voltage source is full load experiment. Figure (a) is the output current waveform in the two-state hysteresis current control mode. At this time, due to the loop inductance increase, the operating switching frequency of the current source is further reduced, but a good current waveform tracking can also be achieved. The actual output current \(I_{\text{rms}} = 14.1\text{A}, \text{THD}_I = 3.8\%\). Figure (b) shows the current output waveform in the three-state hysteresis current control mode. Compared with the previous working condition, the energy storage element in the loop is further enlarged, so that the waveform distortion at the current zero crossing is aggravated. The actual output current \(I_{\text{rms}} = 14.3\text{A}, \text{THD}_I = 5.5\%\).

\[ \text{Figure 5. The simulation waveform of } R_0 = 3\Omega, L_0 = 3\text{mH}. \]

From the simulation analysis of the above three working conditions, it can be concluded that only the two-state hysteresis current control can achieve a good waveform output, which can ensure the stable value of the output fundamental current, and the output current harmonic content is very small.

5. Experimental Analysis

5.1. Hysteresis Current Controller Based on FPGA

The biggest advantage of FPGA[12], compared with DSP(Digital Signal Processor) controller, which adopts a pipeline form, and the program runs strictly in accordance with the instruction cycle, so the longer the program code, the longer the execution time, lies in that FPGA is a parallel execution form, and the internal hardware circuit completes the program function which is characterized by high
reliability and fast execution speed. The block diagram of the controller circuit used in this device is shown in Figure 6.

The Fortan language in section 4.1 is turned into a hardware description language (Very-High-Speed Integrated Circuit Hardware Description Language), and then is burned into the FPGA chip to form a hardware hysteresis current controller. The hysteresis current control is all realized digitally, such as the FPGA program software in the dashed box in the controller block diagram. This paper adopts two-levels hysteresis current control strategy, as Figure 2(a) and Figure 3(a) show.

5.2. The Influence of Delay Time on the Accuracy of Hysteresis Current Control
Hysteresis current control technology is a fast, non-linear current tracking control technology. The biggest problem is that there are certain requirements for speed. But there also are delay in actual circuit, which includes the following parts, as is shown in Table 3.

| Component                        | Delay Time          |
|----------------------------------|---------------------|
| Transmission delay of current transformer | (1~10)μs           |
| Sampling and conditioning circuit delay | (1~1000)μs         |
| AD sampling delay                | 1 sampling period   |
| FPGA software execution time     | 1 clock cycle       |
| Light transmission time          | <1μs                |
| Opt isolation drive circuit delay (M57962AL) | (2.5~4.3)μs       |
| IGBT(BSM200GB120DN2) turn-on and turn-off delay | (0.82~1.3)μs     |

Table 3 provides delay parameters of device and software in this device. Except that the delay time of the sampling and conditioning circuit is greatly affected by the actual circuit and low-pass filter parameters, the remaining delay time is basically fixed within a certain range, and mainly depends on the selected device signal. In order to filter out noise and high-frequency glitch signals, we usually add low-pass filter circuit, and the cut-off frequency has obvious difference because of different circuit.

Figure 6 provides sampling and conditioning circuit and delay time is around 400μs, DC bus voltage is 25V, and at this time, the hysteresis current control ripple is very large, and the number of switching times per cycle is about 23 times, that is, the average switching frequency is about 1.2kHz.

Figure 7. The experimental waveform of two levels hysteresis current control.
It can be concluded from the experimental waveform analysis that the average switching period is about twice the delay time. Certain current is 4.94A in figure 7(a), but actual current is 5.62A, and steady level error 13.6%; Figure 7(b) provides certain current that is 6.59A, actual current 6.82A, steady level error 3.4%; the result shows that the steady-state accuracy is greatly improved as the output current increases, but the switching ripple is still about 5A. Therefore, the delay time of the low-pass filter should be as small as possible in the hysteresis current control. Only in this way can the current tracking effect be guaranteed. Otherwise, the hysteresis control effect will not be reflected.

5.3. Experimental Analysis after Improving the Control Circuit Parameters

Experimental analysis is carried out based on improving the above circuit parameters and greatly reducing the parameters of the low-pass filter to below 50μs while other parameters remaining unchanged. The experimental waveforms are shown below. Figure 8(a) and (b) are the experimental waveforms when the given current is 2.77A. The actual output current is 2.72A, and the current distortion $THD_r=34.9\%$. shown in Figure 8(c) and (d) are the experimental waveforms when the given current is 11.2A, the actual output current is 11.3A, and the current distortion $THD_r=7.8\%$. Based on frequency spectrum analysis on the time-domain current waveform, the fundamental wave and main sub-harmonic data is obtained, which is shown in Table 4. From the main sub-harmonic data in the table, it can be concluded that the switching ripple in the output current is concentrated around 4.8kHz.

**Table 4.** The spectrum analysis data of current.

| frequency (th) | 1 | 93 | 94 | 95 | 96 | 97 | 98 | 99 |
|---------------|---|----|----|----|----|----|----|----|
| amplitude     | 2.72 | 0.14 | 0.12 | 0.10 | 0.33 | 0.62 | 0.33 | 0.20 |

| frequency (th) | 1 | 90 | 91 | 92 | 93 | 94 | 95 | 96 |
|---------------|---|----|----|----|----|----|----|----|
| amplitude     | 11.3 | 0.20 | 0.34 | 0.26 | 0.12 | 0.25 | 0.25 | 0.35 |

**Figure 8.** The improved experimental waveforms.
6. Conclusion
From the above simulation and experimental research, it can be obviously concluded that though Hysteresis current control technology has good current tracking performance, operating frequency is not easy to control, which lead to the fact that the switching frequency is too high and so the technology cannot be put into practice. This paper proposes that, changing the delay time in the circuit can improve the hysteresis current control technology, using a high-performance FPGA as the controller. Its fast parallel execution capability provides a new direction for the application of hysteresis current control technology. Finally, by showing that the all-digital hysteresis current control technology proposed in this paper can realize the control of the controllable current source, a good control effect is achieved.

Acknowledgments
The research work of this paper has been supported by the science and technology project of State Grid Zhejiang Electric Power Co., Ltd. (B311SX210002).

References
[1] Sun Le, Wu Zhenxing, Ma Weiming. 2014 Analysis of the DC-link capacitor current of power cells in cascaded H-bridge inverters for high-voltage drives. IEEE Transactions on Power Electronics, P 6281-6292
[2] Abolhassani M. 2012 Modular multipulse rectifier transformers in symmetrical cascaded H-bridge medium voltage drives. IEEE Transactions on Power Electronics, P 698-705.
[3] Jeevanathan S, Dananjayan P. 2005 Static Model Verification of IRF Power MOSFETs Using Fluke Temperature Probe (80T-150U) and Performance Comparison of TEHPWM Methods. International Conference on Power Electronics and Drives Systems (Kuala Lumpur.: Malaysia)
[4] Held M, Jacob P, Nicoletti G. 1997 Fast power cycling test of IGBT modules in traction application. Proceedings of Second International Conference on Power Electronics and Drive Systems(Singapore)
[5] Rael S, Davat B. 2008 A Physics-Based Modeling of Interelectrode MOS Capacitances of Power MOSFET and IGBT. IEEE Trans. on Power Electronics, P2585-2594.
[6] Meyer C, De Doncker R W, Yun Wei Li. 2008 Optimized Control Strategy for a Medium-Voltage DVR—Theoretical Investigations and Experimental Results. IEEE Trans on Power Electronics, P2746-2754
[7] Isidori A, Rosso F M, Blaabjerg F. 2014 Thermal loading and reliability of 10-MW multilevel wind power converter at different wind roughness classes. IEEE Transactions on Industry Applications, P 484-494
[8] Al-Hadidi H K, Gole A M, Jacobson D A. 2008 Minimum Power Operation of Cascade Inverter-Based Dynamic Voltage Restorer. IEEE Trans on Power Delivery, P 889-898
[9] Ying Jianping, Shen Hong, Zhang Dehua. 2004 Two-hysterisis control of three-phase two-amplitude actively clamped resonant DC-link inverter. Proceedings of the CSEE, P8-12.
[10] Jun Liu, Yangguang Yan. 2003 A novel hysteresis current controlled dual buck half bridge inverter.Conf.Rec. IEEE PESC’03(Acapulco.: Mexico)
[11] Anaya-Lara O, Acha E. 2002 Modeling and analysis of custom power systems by PSCAD/EMTDC.IEEE Trans on Power Delivery, P266-272
[12] Chu, Pong P. 2017 FPGA Prototyping by VHDL Examples: Xilinx Microblaze MCS Soc