Tunable Current Transport in PdSe₂ via Layer-by-Layer Thickness Modulation by Mild Plasma

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The thickness-modulated phase transition from semi-metallic (bulk) to semiconductor (a few layers) is the most unique property of pentagonal palladium diselenide (PdSe₂). Thus, precise thickness tailoring is essential to fully utilize its unique thickness-dependent property for exotic device applications. Here, tunable current transport in PdSe₂ based field-effect transistors (FETs) enabled by layer-by-layer thinning of PdSe₂ using mild SF₆:N₂ plasma is presented. With this top-down plasma-etching method, the PdSe₂ layer thickness can be precisely modulated without structural degradation, which paves the way to realize the complete potential of PdSe₂-based devices. By modifying the plasma power and exposure time, an atomic layer precision etching rate of 0.4 nm min⁻¹ can be achieved. Atomic-force microscopy, Raman spectroscopy, and secondary ion mass spectrometry confirm the uniform and complete removal of top layers of PdSe₂ flake over a large area without affecting remaining bottom layers. Electrical characterization of current transport in plasma-thinned PdSe₂ FETs reveals excellent layer-dependent conductivity similar to pristine PdSe₂ FETs. This simple but highly scalable and controllable plasma-etching technique provides a promising way to fabricate PdSe₂ devices based on lateral heterostructures composed of different thicknesses PdSe₂ flakes to exploit strongly thickness-dependent electronic structures.

1. Introduction

2D material palladium diselenide (PdSe₂), a puckered pentagonal group-10 transition metal dichalcogenides (TMDs) with low symmetry lattice structure, has emerged as a promising candidate for the future device applications due to its large tunable band gap, strong interlayer coupling, and outstanding environmental stability.[1-5] Especially, the large band gap modulation[6] ranging from 0 eV (semi-metallic) in bulk to 1.3 eV (semiconducting) in monolayer makes PdSe₂ more unique since the electrical conductivity of PdSe₂ flake can be abruptly tuned by modulating its thickness. The presence of excess number of valence electrons in Pd strongly hybridizes Pd and Se atoms, causing strong interlayer coupling which results in this significant dependency of band gap on the layer number of PdSe₂. Oyedele et al.[5] observed distinct layer-dependent transport properties where they found that electron on/off ratio decreases from ~10⁶ to <10 for bilayer to bulk PdSe₂. Recently, Zeng et al.[6] has grown layered PdSe₂ with a tunable thickness from 1.2 to 20 nm by selenizing pre-deposited Pd layer. However, precise thickness-controlled growth of PdSe₂ by the bottom-up growth technique is still challenging, especially for a low layer number. On the other hand, mechanical exfoliation of PdSe₂ usually produces non-uniform domains of flakes containing different numbers of layers in tiny size without any controllability and re-productivity.[5,7] Instead of controlling the PdSe₂ layer number by growth, it can also be modified by removing the layers after synthesis. Therefore, a redefined top-down approach using an etching technique would be the most effective in tuning the thickness of PdSe₂, which can be exploited for selectively (or completely) thinning down PdSe₂ to the desired thickness.

Meanwhile, several post-synthesis etching techniques by different approaches including thermal annealing[8-9] laser[10] and focused ion beam (FIB).[11,12] and plasma etching[13-15] have been extensively studied to achieve ultra-thin TMDs materials. Among these, plasma etching is most commonly used in industry because of its compatibility with conventional complementary metal–oxide–semiconductor processing. However, during the etching process, unwanted damage by direct bombardment of high energy ions is inevitable. Additionally, strain generation due to the thermal heating can cause physical damage to the remaining layers as a consequence electrical performance of thinned layer becomes greatly degraded, which need to be overcome. Furthermore, presently reported recipes on the plasma thinning have been mainly focused on MoS₂[16] and WSe₂.[17] Any complete studies with highly selective and controllable etching method for PdSe₂ which exhibits a wider range of band gap modulation by the thickness are still unavailable. Previous reported studies involving PdSe₂ and its application to thickness dependent conduction behavior have focused on the synthesis by bottom-up technique (e.g., chemical vapor deposition) and the evaluation of its performance.

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However, controlling thickness by top-down technique or a selective etching method have not been reported yet, although it is essential for device fabrication process.

Here, we propose a selective, uniform, and large-area etching of PdSe$_2$ and its direct demonstration on tunable current transport in PdSe$_2$ based field-effect transistors (FETs) by controlling the layer thickness of PdSe$_2$ with atomic layer precision using mild SF$_6$+N$_2$ plasma. A monolayer etching rate of 0.4 nm min$^{-1}$ for PdSe$_2$ was achieved with a mild plasma power density of 1.5 mW cm$^{-3}$ at room temperature. Optical microscopy and atomic force microscopy (AFM) measurements were performed to check the thickness change and surface morphology before and after etching. The effect of plasma etching on the surface modification was examined by Raman spectroscopy and secondary ion mass spectrometry (SIMS) imaging. Furthermore, to investigate the transport property of plasma-thinned PdSe$_2$ flakes, an extensive study was carried out in comparison with pristine PdSe$_2$ flake through the electrical characterization of pristine and plasma-thinned PdSe$_2$ FETs. This highly selective and reproducible plasma etching technique can be applied to demonstrate PdSe$_2$ heterostructures with different thicknesses and sizes; thereby fully utilizing the great potential of PdSe$_2$ for future device applications.

### 2. Results and Discussion

To determine the selective, controlled, and atomic-scale etching method of PdSe$_2$, first we mechanically exfoliated 2D PdSe$_2$ flakes from bulk crystals by modified scotch tape method$^{[18,19]}$ and transferred onto thermally grown 300 nm SiO$_2$ on highly p-doped Si substrates. Since the optical contrast of 2D material varies with the change of its thickness,$^{[20]}$ visual characterization based on the optical contrast on the substrate is an efficient way to roughly identify the thickness of PdSe$_2$ flake. Optical microscopy image was obtained after exfoliation for primary identification of the different layer number of exfoliated flakes. Afterward, a dry chemical etching was carried out to thin down the PdSe$_2$ flakes using SF$_6$ (2 sccm)/N$_2$ (6 sccm) as a gaseous reactor under low power radio frequency (RF) plasma at room temperature. Process pressure was maintained at 20 mTorr throughout unless specified otherwise. By utilizing oxidation-reduction reaction produced by SF$_6$+N$_2$ precursor under a low density plasma RF power, strong oxidant reacts with Pd and Se simultaneously leading to the effective reduction of PdSe$_2$ thickness. Through this reaction, fluorine radicals form gaseous by-products which are removed from the chamber after etching without leaving any residues. Mild plasma etching strongly depends on SF$_6$+N$_2$ gaseous precursor associated with the low power plasma source. Therefore, by varying input plasma power density, etching rate can be precisely regulated. Plasma chemistry for PdSe$_2$ etching applied in this work is similar to the reported soft etching technique for MoS$_2$$^{[20]}$ and MoSe$_2$. Selective etching of PdSe$_2$ could be achieved without having a negligible etching effect on SiO$_2$ by controlling the plasma power density for different plasma irradiation time. Initially a wide spectrum of plasma etching condition was thoroughly investigated by changing the plasma power density. Then the critical value was determined to minimize the etching of SiO$_2$ so that plasma etching could be selective for PdSe$_2$ only. An optimized plasma etching condition is highly desirable for achieving uniform and controlled etching over a large area of sample without any structural degradation in the etched material. Figure 1a,b compares the optical image of multilayer PdSe$_2$ flake before and after plasma etching for 2 min under 1.5 mW cm$^{-3}$ plasma power density. From the optical contrast, a significant amount of change in different domains of flake was observed, indicating the decrease in the thickness of PdSe$_2$ flake. To precisely estimate the thickness change of PdSe$_2$ flake, the thicknesses of before and after the plasma treatment were measured through AFM as shown in Figure 1c,d. AFM line profiles in the bottom panel shows estimated heights of $\approx$ 3.5 and $\approx$ 2.7 nm before and after plasma etching, respectively, measured at dashed lines in Figure 1c,d. By comparing the AFM profile, we found that after 2 min of plasma treatment, about 0.8 nm of PdSe$_2$ thickness was reduced. Therefore, an atomic-scale etching rate of $\approx$0.4 nm min$^{-1}$ which is equivalent to monolayer PdSe$_2$ was achieved at an input plasma power density of 1.5 mW cm$^{-3}$. Additionally, a SiO$_2$ substrate was also etched using PR mask under the same etching condition to identify the etching effect on SiO$_2$ substrate. A remarkably minimal etching depth of $\approx$1.5 nm after 30 min of plasma etching using 1.5 mW cm$^{-3}$ plasma power density was found (Figure S1, Supporting Information). To precisely calculate the etching rate or etched layer number of PdSe$_2$, SiO$_2$ etched depth was deducted from the AFM results. Furthermore, another faster etching condition was obtained by increasing the input plasma density. By doubling the plasma power density to 3 mW cm$^{-3}$, $\approx$25 layers ($\approx$10 nm) of PdSe$_2$ was removed in 10 min of plasma irradiation. Figure 1e summarizes the etching depth as a function of etching time for different plasma power densities. As shown by vertical dotted line, initial etching rate was slow due to the absence of sufficient amount of oxidant. Afterward, a stable and linearly increasing etching rate was maintained with increasing plasma irradiation time. A linear dependence of etching rate was observed for different plasma powers with different slopes of the curves. Etching rates of $\approx$0.4 and $\approx$1 nm min$^{-1}$, defined as slow and fast etching modes, were extracted for the power densities of 1.5 and 3 mW cm$^{-3}$, respectively. Figure If shows the variation of the root-mean-square (RMS) roughness of the surface after etching process with respect to time. RMS roughness values were estimated from AFM image after each etching step. Surface roughness significantly increased within the initial 10 min of etching and became somewhat stable afterward. The roughness values were able to be kept below 0.35 nm during etching up to 30 min. This result validates that the surface roughness of plasma-thinned PdSe$_2$ flakes was comparable to an average roughness value of pristine PdSe$_2$ flakes. Since etching rate and surface roughness rise with increasing plasma density, further increase in plasma power could result in a higher surface roughness by generating more defect sites. It is obvious that producing larger amount of oxidant by increasing pressure or supplying higher amount of precursor can fasten the etching rate, but in consequence it may significantly increase the roughness and damage the crystal surface. Achieving an atomic level etching rate maintaining a smooth and damage-free crystal structure is the principal objective of this study. The mild etching mode below the critical value ($\approx$3 mW cm$^{-3}$) of the
input power density was found to be optimal for thinning down any pre-determined number of PdSe$_2$ layer. Therefore, this condition was maintained throughout this work.

To demonstrate uniform layer-by-layer thinning of PdSe$_2$ over a large area irrespective of the initial thickness, plasma etching was performed on a large (≈80 µm long) and over 60 layers (≈23.8 nm) pristine PdSe$_2$ flake (Figure S2a, Supporting Information). Figure S2a–c, Supporting Information, shows systematic thinning down of thick 60 layers PdSe$_2$ into ≈4 layers. As discussed earlier, PdSe$_2$ etching condition can be efficiently controlled by varying plasma power for different purpose; for example, faster etching using increased plasma power is efficient to thin down thick PdSe$_2$ flakes rapidly, whereas slow etching is useful for fine tuning to obtain ultra-thin thickness. At first, we adopted faster etching rate using increased plasma power which significantly accelerate the etching rate due to the increased ion density and electron temperature of the plasma. As a result, 37 layers (≈14.8 nm) were uniformly thinned down from all over the PdSe$_2$ flakes after 15 min of etching (Figure S2b, Supporting Information). After that, the PdSe$_2$ flake was further thinned down by combining fast and slow etching modes for 5 min, to achieve ≈1.7 nm thick PdSe$_2$ flake (Figure S2c, Supporting Information). The AFM profiles extracted from the corresponding AFM images for different etching times at 0, 15, and 25 min, respectively, are shown in bottom panel of Figure S2d–f, Supporting Information. It is also noticeable that original domain size and shape of the pristine PdSe$_2$ flakes remain unaffected after the long plasma process which is common for the conventional thermal or laser-based etching process.

Raman spectroscopy is a sensitive technique and widely used to study layer numbers, defects, strain, and substrate effects of 2D materials.[22,23] A systematic Raman characterization was carried out to study the effect of plasma on the crystal property of PdSe$_2$ and to estimate the decrease of the PdSe$_2$ layer number along with the various exposure times to plasma treatment. Raman measurement was performed using a confocal Raman microscopy with the laser excitation line of 532 nm. The incident laser power was maintained at 0.5 mW to avoid any additional damage on the etched surface. All the Raman single spectra were calibrated with the Si substrate peak at 520 cm$^{-1}$. Optical images of PdSe$_2$ flakes after different etching times within the range of 0–25 min during Raman study is presented in Figure S3a, Supporting Information. Figure 2a shows the Raman spectra of pristine and plasma-thinned PdSe$_2$ flakes with varying plasma irradiation time. In Figure 2a, there are four apparent peaks located at ≈144.5,
peaks of PdSe2 are appeared due to the movement of Se atoms, frequency shift for the Ag1-B1g1 and Ag3 Raman modes after different S3b, Supporting Information. Figure 2b shows Raman frequency after each fixed interval of plasma treatment at the same location of the etched PdSe2 flake. All five Raman peaks described above monotonously shifted toward higher frequency after each plasma treatment due to the thickness reduction of pristine bulk by etching. This trend of frequency shift with the increasing plasma irradiation time is consistent with the thickness-dependent Raman spectra in the pristine PdSe2 flake.4,5 Although peak intensity and position continuously changes with gradual increase of plasma irradiation time, a clear and strong Raman signal was observed in every etching step which indicates that crystal property of PdSe2 was maintained even after a long plasma etching of 25 min. In addition, as the thickness of PdSe2 changes with increasing plasma irradiation, some new Raman peak at lower wavenumber around 120–130 cm−1 was observed in a few layer PdSe2 which are believed to be due to the orthorhombic space group change from Pba to the Pca21 for few layer PdSe2 (details in Figure S3d, Supporting Information). Figure 2b shows Raman frequency shift for the Ag1-B1g1 and Ag3 Raman modes after different plasma etching time. A significant Raman shift of around 4–5 cm−1 was observed for pristine to 25 min plasma-etched PdSe2. The magnified line spectra from 240 to 280 cm−1 is plotted in Figure S3c, Supporting Information. This degree of peak shift is well agreed with previously reported value5,25 and implies that the thickness of PdSe2 can be precisely tuned with varying the plasma etching time. Raman intensity ratio of Ag3 to Si increased as thickness decreased as a function of etching time as plotted in Figure 2c. Although peak position changes with the continues reduction in thickness after plasma treatment, Raman intensity of Ag3 Raman mode decreased as the Raman signal from the substrate Si peak at ≈520.5 cm−1 becomes dominant with longer etching time, indicating the thinning of PdSe2 flakes (the detail in Figure S3d, Supporting Information).

The surface elemental properties of crystals can be influenced by plasma treatment; therefore, further investigation is necessary to elucidate the surface chemistry and surface chemical composition after plasma treatment. Due to the inefficiency to focus on a small particular region by the X-ray beam in X-ray photoelectron spectroscopy (XPS), it is difficult to observe the significant chemical composition when the flake size relatively small. Therefore, XPS has not been used in this study. Recently, time-of-flight SIMS (ToF-SIMS) has emerged as a powerful technique to characterize atomically thin 2D materials, due to its ultra-high chemical selectivity.24–26 ToF-SIMS spectroscopy provides a direct qualitative analysis of the elemental composition with a unique advantage of obtaining high resolution image of the entire surface.27,28 In order to investigate the elemental surface composition of PdSe2, before and after plasma treatment, ToF-SIMS chemical mapping measurement was carried out with a sub-micron lateral resolution and SEM-level visualization capability. Figure 3a,b presents a 50 × 50 μm area lateral resolution ToF-SIMS image specifying i) Pd, ii) Se, and iii) Si secondary ions by positive and negative probe scan as representative of PdSe2 and SiO2 surfaces. These images were acquired at the same position before and after 10 min plasma treatment corresponding to the optical image of PdSe2 crystal in Figure S4, Supporting Information. ToF-SIMS surface map of Pd and Se− secondary ions represents isolated PdSe2 domain distribution on SiO2 substrate before and after plasma treatment. Elemental chemical maps reveal that the homogeneous incorporation of Pd and Se atoms were well-preserved in the thinned PdSe2 layer even after 10 min plasma treatment. The uniform chemical distribution with a clear sharp boundary between the PdSe2 crystal and SiO2 substrate rules out any non-homogeneous composition conversion after plasma treatment which is consistent with our Raman measurements in Figure 2.

To investigate the transport properties in the plasma-thinned PdSe2 flake, back-gated FETs were fabricated and characterized.
The details in device fabrication steps can be found in the Experimental Section. For complete understanding the effect of plasma treatment on PdSe₂, we fabricated two FETs from pristine PdSe₂ and plasma-thinned PdSe₂ flakes with a similar thickness and compared their transport characteristics. Since previous studies have reported that ≈20 layers (≈8–9 nm) PdSe₂ FETs exhibits the highest mobility[5,7] similar to the other back-gated 2D materials FETs, [29–31] a thickness of ≈9 nm was selected for the preliminary device fabrication. Figure 4a,b shows the schematic and photograph of PdSe₂ FETs along with the optical microscope and AFM images of pristine and plasma-thinned flakes. To obtain plasma-etched PdSe₂ flake, an ≈13.2 nm as-exfoliated flake was etched for 10 min under 1.5 mW cm⁻³ plasma power density. The remaining thickness of ≈9 nm was achieved as shown in Figure 4b. The transfer (Iₑ−Vₑ−Vₛ) characteristics of ≈9 nm thick pristine and plasma-thinned PdSe₂ FETs at a fixed low drain bias (Vₛ) of 0.1 V are compared in Figure 4c. From the transfer characteristics, we observed almost symmetric, but electron dominant, ambipolar behaviors with the on/off ratio greater than 10² for both pristine and plasma-thinned PdSe₂ FETs. Slightly higher current was found for pristine PdSe₂ FETs than plasma-thinned PdSe₂ FETs. We extracted the threshold voltage (Vₖ) for both devices by extrapolating the straight line from the linear transfer characteristics as shown in Figure S5a, Supporting Information. The estimated Vₖ were −8 and +6 V for pristine and plasma-thinned PdSe₂ FETs, respectively. A positive shift in the Vₖ suggests that the native n-type doping in PdSe₂ was removed by SF₆+N₂ plasma treatment while managing the drive current within the same order. Figure 4d displays the output (Iₑ−Vₑ−Vₛ) characteristics (Vₑ−Vₛ sweep range from 0 to 60 V in 10 V step) of both devices. We observed a linearly increasing current at a low drain bias (also see Figure S5b, Supporting Information), indicating the low Schottky barrier at source/drain contacts. [12] Almost similar transport behavior in plasma-thinned PdSe₂ with similar thickness pristine PdSe₂ reveals that crystal structure of PdSe₂ was not altered by the plasma treatment, which was also confirmed in our structural and optical studies. It has been demonstrated that PdSe₂ has strong thickness-dependent electrical conductivity due to its largely tunable bandgap depending on the layer number. [5] To further explore the thickness dependency on current transport of the plasma-thinned PdSe₂ flakes with various thicknesses ranging from ≈3 to ≈25 nm were obtained by etching using our previously described plasma treatment recipe. In particular, a uniform etching time of 10 min was employed under a plasma power density of 1.5 mW cm⁻³ for obtaining various plasma-etched PdSe₂ flakes. Since an etching rate of ≈0.4 nm min⁻¹ was extracted for the power density of 1.5 mW cm⁻³, applied plasma exposure time of 10 min would have resulted ≈10 layers of PdSe₂ etching irrespective of its initial thickness. Therefore, it validates that all the etched flakes were obtained by etching the same thickness under the same etching condition with a consistent surface morphology. Additionally, a different set of pristine PdSe₂ flakes with similar thicknesses to the plasma-thinned PdSe₂ flakes were also prepared by mechanical
exfoliation for comparison. We fabricated a multiple number of devices for each thickness of both pristine and plasma-thinned PdSe$_2$. Some of the representative transfer characteristics of PdSe$_2$ FETs for different thicknesses ($\approx$ 3–$\approx$ 25 nm) were presented in Figure S6a,b Supporting Information, for pristine devices and plasma-etched devices, respectively. Figure 4e summarizes on-current ($I_{\text{on}}$) and off-current ($I_{\text{off}}$) as a function of thickness for both pristine and plasma-etched PdSe$_2$. As the flake becomes thicker, $I_{\text{off}}$ monotonically increases due to the reduction of band gap as confirmed by other studies. [5] On the other hand, $I_{\text{on}}$ also increases for thicker PdSe$_2$ flake and trends to saturate after a certain level due to the large interlayer resistance in thicker PdSe$_2$. [33] The thickness-dependent on/off ratios for the electron and hole current were summarized and displayed in Figure S7, Supporting Information. For both pristine and plasma-thinned PdSe$_2$ FETs, an increase in the on/off ratio from $\approx$10 to $\approx$10$^4$ was observed as the thickness is reduced from $\approx$25 to $\approx$3 nm. Meanwhile, a smaller on/off ratios can be found for the hole current. A trend of increasing the on/off ratio for the thinner PdSe$_2$ flakes is associated with the semimetallic to semiconducting transition in PdSe$_2$ as reported in the previous studies. [5,7] A slight deviation in $I_{\text{on}}$ and $I_{\text{off}}$ in the plasma-etched PdSe$_2$ compared to the pristine PdSe$_2$ is observed. However, all plasma-thinned PdSe$_2$ devices followed the similar trend as in pristine PdSe$_2$ devices with comparable current at a similar thickness range, suggesting that plasma thinning is an effective method for tuning the PdSe$_2$ thickness without altering the thickness-dependent transport properties.
significantly. The field effect mobility was extracted from the linear region of the transfer curves using the equation, $$\mu = \frac{g_m}{W_L} \times \frac{L}{W_L} \times \frac{1}{d_{th}}$$ at low $$V_{th} = 0.1 \text{ V}$$, where $$L$$, $$W$$, and $$d_{th}$$ represent the channel length, width, and effective oxide capacitance per area, respectively. $$C_{ox}$$ was estimated to be $$1.15 \times 10^{-8} \text{ F} \cdot \text{cm}^{-2}$$, considering $$C_{ox} = \varepsilon_0 \varepsilon_r / d_{ox}$$, where $$\varepsilon_0 = 8.85 \times 10^{-14} \text{ F} \cdot \text{cm}^{-1}$$, $$\varepsilon_r = 3.9$$ are the relative permittivity of air and SiO$_2$, respectively, and $$d_{ox} = 300 \text{ nm}$$ is the SiO$_2$ thickness for our device. To examine the mobility variation with the PdSe$_2$ thickness, electron and hole mobilities were plotted as a function of thickness for pristine and plasma-thinned PdSe$_2$ FETs as in Figure 4f. The calculated electron mobility appeared strongly dependent on the flake thickness in a nonmonotonic fashion, as the layer number increases, mobility is generally enhanced due to the reduced Coulomb scattering from charge impurity. Simultaneously, additional interlayer resistance also starts to increase as the layer number increases in the thicker PdSe$_2$ channel of a backgated FET configuration.\textsuperscript{35,36} Therefore, as the flake thickness further increased over $$=9$$ nm, the mobility degradation by interlayer resistance becomes dominant over the mobility gain from the charge screening, thus reversing the trend.\textsuperscript{37,38} This nonmonotonic trend suggests that a layer number in the range of $$=5$$ and $$=20$$ layers would be ideal for maximizing the device performance. Therefore, the precise thickness control achieved by our plasma treatment strategy may pave the realistic way for harvesting the maximum potential of PdSe$_2$. These results show that all plasma-thinned PdSe$_2$ devices followed the same trend as in pristine PdSe$_2$ devices. Although, the dependency of on/off current ratio and mobility on the thickness of pristine and plasma-thinned PdSe$_2$ flakes look alike, there is a minimal degradation in the etched PdSe$_2$ flakes. This minimal but observed degradation in the plasma-etched PdSe$_2$ suggests the impact of surface damages induced by SF$_6$ plasma. The plasma process introduces an increased amount of surface roughness compared with pristine PdSe$_2$. As a result, plasma-etched devices are more susceptible to the carrier scattering which lowers the current. Additionally, interfacial impurities such as surface chemical residue of etched surface also can be responsible for the mobility degradation in plasma-etched PdSe$_2$. Moreover, the dependency of mobility on the thickness of pristine and plasma-thinned PdSe$_2$ flakes look alike with a minimal degradation in the etched PdSe$_2$ flakes, confirming the effectiveness of our plasma etching approach.

To further investigate the plasma etching effect on the device property, a pristine PdSe$_2$ FETs with relatively thicker flake ($=20$ nm) was fabricated and systematically etched as illustrated in Figure 5a. Evolution of transfer and output characteristics of PdSe$_2$ FETs along with the sequential plasma treatment with 1.5 mW cm$^{-2}$ plasma power is shown in Figure 5b,c. The transfer curves in Figure 5b confirms a progressive transition from semi-metallic to semiconducting nature of PdSe$_2$ with an increased etching time and etched depth. As the etching depth increases (in other word, remaining channel thickness decreases) after every etching step, $$I_{on}$$ is lowered monotonically due to the channel thickness reduction and the resulting band gap increase. Therefore, the on/off ratio increases. It is also noted that $$I_{on}$$ decreases after each etching step which is due to the increased channel resistance of the PdSe$_2$ channel as it becomes thinner and hence the band gap increases. This sequential evolution of semimetallic to semiconducting carrier transport in the PdSe$_2$ FET is consistent with the thickness-dependent phase transition from semi-metal to semiconductor in the electronic property of PdSe$_2$. However, it is observed that there is a slight change in $$V_{th}$$ for the current minima, which may be due to the unintentional change in the surface morphology during the etching process. As shown in Figure 5d, total etching time of $29$ min is collectively employed to achieve the final remaining thickness of $=8$ nm. During prolonged etching time, plasma-thinned PdSe$_2$ is likely to experience more ionized impurities. The chemical impurities or residues also may remain on the surface of PdSe$_2$ channel which causes the irregular shift of the current minima in etched device. Figure 5d represents the relationship between the remaining channel thickness and the on/off ratio with respect to the sequentially applied etching steps. As the remaining channel thickness decreased after each etching step, the on/off ratio for electrons increases gradually from $<10$ for pristine $\approx 20$ nm thick PdSe$_2$ to $>10^3$ for $=8$ nm thick PdSe$_2$ after total $29$ min of etching. A positive $$V_{th}$$ shifts with the increasing etching time was observed as shown in the Figure 5e. The $$V_{th}$$ of pristine device moved in the positive direction from $-30$ to $+18$ V upon etching for $29$ min. This positive $$V_{th}$$ shift is an undesirable side effect which can be associated with p-doping induced by fluorine adatoms during the SF$_6$ plasma.\textsuperscript{39,40} Electron mobility in Figure 5f follows monotonically rising and falling trend as a function of etching time as similar as in Figure 4f. As the etching time increased, the remaining channel thickness was further reduced, and a gradual mobility improvement was observed until etching time up to $15$ min. As discussed with Figure 4f, when the channel thickness was thinned down below $=9$ nm, mobility was expected to follow the downfall. A direct comparison of electron mobility trend between plasma etching PdSe$_2$ and plasma-etched FETs device is also presented in Figure S8. Supporting Information. Unlike plasma-etched PdSe$_2$ sample, the mobility of the pristine PdSe$_2$ device started to decrease earlier after $\approx 20$ min of etching at an estimated remaining layer thickness over $=12$ nm, which may be due to the increased surface roughness induced by the longer etching time or the influence of SF$_6$ plasma on the exposed channel layer. In case of plasma-etched PdSe$_2$ the maximum point of mobility was achieved at thickness of $=9$ nm. The mobility degradation suggests that the reduced PdSe$_2$ channel at this point of etching are susceptible for the insufficient charge screening from Coulomb scattering. Our demonstration of thinning down only the channel region in PdSe$_2$ FETs may be useful to fabricate the recessed channel PdSe$_2$ FETs to take advantage of the unique thickness-dependent semi-metallic to semiconducting transition property of PdSe$_2$ to lower the contact resistance, which will be in the scope of future studies.
3. Conclusion

In summary, we have demonstrated a highly controllable, selective, and uniform atomic layer etching of PdSe$_2$ using SF$_6$+N$_2$ plasma irradiation. By controlling the plasma power density, similar number of PdSe$_2$ layers can be etched uniformly over a large area. The surface roughness of plasma-thinned PdSe$_2$ remained homogeneous with RMS roughness less than 0.35 nm at an elongated etching time over 30 min, without any shrinkage in the pristine domain shape or sizes. This highly selective etching of PdSe$_2$ strongly depends on plasma power density and exposure time. Thus, by tuning the slow and fast etching modes, any pre-determined number of PdSe$_2$ layer can be achieved irrespective of their original thickness. AFM, Raman, and ToF-SIMS imaging reveal that only top several layers of PdSe$_2$ were removed while bottom PdSe$_2$ remained unaffected. The fabricated FETs based on plasma-thinned PdSe$_2$ shows similar thickness-dependent transport characteristics with pristine PdSe$_2$ FETs. Therefore, our plasma-assisted layer control of PdSe$_2$ could be useful for the fabrication of PdSe$_2$-based devices utilizing its unique thickness-dependent transport property. Lastly, by controlling the etching depth of PdSe$_2$ channel, ideal optimal thickness range for transistor-based operation can be achieved, where a compromise between a high on/off ratio and mobility is required. These results suggest that our simple but highly efficient way of thickness control of PdSe$_2$ enhances the possibility to realize novel device ideas based on the distinct thickness-dependent semi-metallic to semiconducting transition in PdSe$_2$.

4. Experimental Section

PdSe$_2$ Preparation and Plasma Thinning: PdSe$_2$ flakes were obtained by mechanical exfoliation from bulk crystals (supplied by 2D semiconductors) onto a degenerately doped Si substrate with thermally grown 300 nm of SiO$_2$ with prepared alignment markers. A modified mechanical exfoliation technique was followed using a viscoelastic stamp (Gelfilm from Gelpak) as an intermediate substrate for exfoliation...
to avoid additional polymer residue. Furthermore, the samples were cleaned in acetone and rinsed with isopropyl alcohol and deionized water to remove tape residues. SF6 plasma was excited (commercial 13.56 MHz RF source) with the N2 carrier gas at a pressure of 20 mTorr with flow rates of 2 and 6 sccm, respectively, at room temperature. Soft plasma was maintained to reduce the destructive ion bombardment onto the samples by controlling the input plasma power density. Plasma etching rate was optimized with the different power density values of 1.5 and 3 mW cm⁻² to determine different etching conditions.

Microscopic, Optical, and Electrical Characterizations: Optical microscopy, Raman, and AFM were used to identify the thicknesses of selected flakes. Suitable flakes were identified and imaged using a Nikon LV100ND optical microscope. The thicknesses of selected flakes were confirmed by tapping mode AFM topography imaging (Veco DI-3100 LV100ND optical microscope). The thicknesses of selected flakes were carried out with a ToF-SIMS (ION-TOF 5, Germany) instrument, equipped with a bismuth liquid-metal ion source. Surface chemical mapping was performed over a specified area by a 50 keV Bi⁺ cluster beam with a pixel resolution of 512 × 512.

Device Fabrication: To fabricate bottom gated PdSe2 FETs, source-drain metal electrodes (5 nm Ti/50 nm Au) were patterned using an electron-beam lithography process followed by electron-beam evaporation. Finally, the samples were immersed in acetone to lift-off followed by cleansing with isopropyl alcohol and deionized water.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest
The authors declare no conflict of interest.

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layer-dependent transport, palladium diselenide, plasma etching, thickness modulation

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[29] H. Schmidt, S. Wang, L. Chu, M. Toh, R. Kumar, W. Zhao, A. H. Castro Neto, J. Martin, S. Adam, B. Özyilmaz, G. Eda, Nano Lett. 2014, 14, 1909.
[30] D. Ovchinnikov, A. Allain, Y.-S. Huang, D. Dumcenco, A. Kis, ACS Nano 2014, 8, 8174.
[31] R. A. Doganov, S. P. Koenig, Y. Yeo, K. Watanabe, T. Taniguchi, B. Özyilmaz, Appl. Phys. Lett. 2015, 106, 083505.
[32] D. Schulman, A. J. Arnold, S. Das, Chem. Soc. Rev. 2018, 47, 3037.
[33] Y. Zhang, H. Li, H. Wang, H. Xie, R. Liu, S.-L. Zhang, Z.-J. Qiu, Sci. Rep. 2016, 6, 29615.
[34] N. Ma, D. Jena, Phys. Rev. X. 2014, 4, 011043.
[35] J. Na, M. Shin, M.-K. Joo, J. Huh, Y. Jeong Kim, H. Jong Choi, J. Hyung Shim, G.-T. Kim, Appl. Phys. Lett. 2014, 104, 233502.
[36] S.-L. Li, K. Komatsu, S. Nakaharai, Y.-F. Lin, M. Yamamoto, X. Duan, K. Tsukagoshi, ACS Nano 2014, 8, 12836.
[37] S. Das, H. Y. Chen, A. V. Penumatcha, J. Appenzeller, Nano Lett. 2013, 13, 100.
[38] S.-L. Li, K. Wakabayashi, Y. Xu, S. Nakaharai, K. Komatsu, W.-W. Li, Y.-F. Lin, A. Aparecido-Ferreira, K. Tsukagoshi, Nano Lett. 2013, 13, 3546.
[39] M. Chen, S. Wi, H. Nam, G. Priessnitz, X. Liang, J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater. Process. Meas. Phenom. 2014, 32, 06FF02.
[40] M. Chen, H. Nam, S. Wi, L. Ji, X. Ren, L. Bian, S. Lu, X. Liang, Appl. Phys. Lett. 2013, 103, 142110.