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Four-phase bi-current spinning current on shallow vertical Hall sensor

L. Osberger*, V. Frick, L. Hébrard

ICube laboratory, 23 rue du Loess – BP 20, 67037 Strasbourg, France

Abstract

Vertical Hall-effect devices (VHDs) are CMOS integrated sensors dedicated to the measurement of magnetic field in the plane of the chip. At low frequency, performances are severely reduced by the \(1/f\) noise. We have recently assessed by FEM simulation the capability of the four-phase spinning current technique (SCT) to lower the \(1/f\) noise on shallow VHD designed in low-voltage CMOS technologies (LV-VHD). It was shown than the highest biasing current could be used on each phase of the SCT, i.e. \(I_{13\text{max}}\) for phases 1 and 3, and \(I_{24\text{max}}\) for phases 2 and 4, if the signal on phases 2 and 4 is amplified by a ratio \(I_{13\text{max}}/I_{24\text{max}}\). Here, we propose a practical way to implement this technique, and for the first time we show experimentally its efficiency to lower the \(1/f\) noise, leading to 51 \(\mu\)T resolution over a 1.6 kHz bandwidth with an average biasing current of only 825 \(\mu\)A.

1. Introduction

Semi-conductor Hall sensors are widely used in many industrial and consumer applications requiring magnetic field detection or measurement [1]. The most common and performing Hall sensor topology is the Horizontal Hall Device (HHD), which is sensitive to the component of the magnetic field that is orthogonal to the surface of the chip. Today

* Corresponding author.

E-mail address: osberger@unistra.fr
Offset and low frequency dependent noise (/f noise) are quite difficult to handle and to get rid of on VHDs [6]. The well-known spinning current (SC) technique that has proven dramatically efficient on the HHD [7] does not seem, at first glance, easy to apply on LV-VHD because of the dissymmetry inherent to its structure. Recently we have experimentally shown that SC can be applied on LV-VHD using a four-phase SC technique [8]. However, the biasing current, which has to be constant in the conventional SC, is limited to the maximum current that can be applied in phases 2 and 4. This paper proposes an optimized SC technique where the maximum achievable current is applied in each phase, leading to a bi-current four-phase SC. The next section describes this new SC technique and section 3 provides the experimental results before conclusion.

2. Spinning-current for LV-Vertical Hall Device

In a LV-VHD (Fig. 1), contacts C2 and C4 are linked with a metal line to form an equivalent single contact C24. The conventional way of biasing the sensor is to inject the biasing current into the central contact C3 and sink it from contact C24. The Hall voltage is then picked up between the external contacts C1 and C5 [6]. The first prototype designed in the AMS 0.35 μm CMOS process was a 3 μm wide, 25 μm long VHD. It achieved a resolution of 80 μT over a [5 Hz – 1.6 kHz] bandwidth [5]. This limited resolution is due to the /f noise. In order to improve it, the spinning-current technique (SCT) may be applied [9]. It consists in periodically exchanging the biasing and the sensing contacts. However, as shown in [10], unlike the Horizontal Hall Device where a simple two-phase SC is very efficient to drastically lower the offset and the /f noise, a four-phase SCT is required to be able to remove the systematic offset which appears in phases 2 and 4 (see Fig. 2 for the definition of the SC phases) [8]. This systematic offset comes from the unsymmetrical depleted zone at the N-well/P-substrate junction in phases 2 and 4. When the biasing and the sensing contacts are exchanged, the biasing current has to be kept constant [9]. However, in the LV-VHD, the input resistance in phases 1 and 3, \( R_{13}/2 \), is much smaller than in phases 2 and 4 where it reads 2·R24 (see Fig. 1 for resistances labeling). The biasing voltage being limited by the supply voltage, i.e. 3.3 V for AMS 0.35 μm, the biasing current in the conventional SCT is limited by the maximum current of phases 2 and 4 [8].

![Fig. 1: Cross view of the Low-Voltage Vertical Hall Device](image)

However, we have already shown in [10], by FEM simulation, that we may use the maximum biasing current in each phase, provided the signal in phases 2 and 4 is amplified by the ratio \( G = I_{13\max}/I_{24\max} \) where \( I_{13\max} = V_{\max}/(R_{13}/2) \) is the biasing current in phases 1 and 3, and \( I_{24\max} = V_{\max}/(2·R_{24}) \) is the biasing current in phases 2 and 4. Here, \( V_{\max} \) is the maximum biasing voltage close to the supply voltage. Note that the ratio \( I_{13\max}/I_{24\max} \) is equal to the ratio of the input resistances 2·R24/(R13/2). We report now for the first time experimental results showing the efficiency of the proposed four-phase bi-current Spinning-current technique.
3. Experimental results

For this experiment (Fig. 3), we use the same 3 μm wide, 25 μm long sensor as in [5] from the AMS 0.35 μm CMOS technology. The chip features two current sources providing $I_{13\text{max}} = 1100 \mu A$ and $I_{24\text{max}} = 550 \mu A$, and switches to implement the four-phase bi-current SCT. The output signal is amplified outside the chip with a programmable gain instrumentation amplifier (AD8250). The gain is set to 100 on phases 1-3, and to 200 on phases 2-4, i.e. the signal in phases 2 and 4 is amplified by a factor $G = 2$ relative to the signal in phases 1 and 3. Note that the effective sensitivity of the sensor on phases 1-3 with the bi-current SC is $G$ times higher than its sensitivity with a conventional SC and a current of $I_{24\text{max}}$. However after amplification the conventional and bi-current SC output sensitivity is equal. In phases 2 and 4, the thermal noise is also amplified by $G$ leading to an average thermal noise of $\sqrt{(G^2 + 1)/2}$. As a consequence, the resolution is improved by a factor of $G/\sqrt{(G^2 + 1)/2}$ when the bi-current SC is used compared to the conventional SC.

### Tab. 1: Summary of the main experimental results

| Mode                  | $I_{\text{min}}$ (μA) | Sensitivity (V/T) | Output Noise (V<sub>\text{rms}</sub>) | Resolution (μT) |
|-----------------------|------------------------|-------------------|---------------------------------------|-----------------|
| Phase φ1              | 550 (G=200) or 1100 (G=100) | 1.72 / 1.66 | 2.21·10^{-4} / 1.54·10^{-4} | 128 / 90 |
| Phase φ2              | 550 (G=200)           | 1.65             | 2.13·10^{-4}                       | 129             |
| Phase φ3              | 550 (G=200) or 1100 (G=100) | 1.67 / 1.65 | 2.33·10^{-4} / 1.74·10^{-4} | 139 / 105 |
| Phase φ4              | 550 (G=200)           | 1.70             | 2.06·10^{-4}                       | 121             |
| Conventional SCT      | 550 (G=200)           | 1.68             | 1.07·10^{-4}                       | 64              |
| Bi-current SCT        | 550 (G=200) with φ2/4 and 1100 (G=100) with φ1/3 | 1.67             | 8.52·10^{-5}                       | 51              |
The measured output power spectral density (Fig. 4) shows that this new SCT efficiently reduces the $1/f$ noise. From the measured sensitivity (Fig. 5) and the output power spectral density, the sensor resolution was determined over a [5 Hz – 1.6 kHz] bandwidth. Table 1 gathers the main results and shows that the sensor resolution is improved by 20% (51 μT against 64 μT) in comparison to the conventional SCT where the current is kept constant, equal to $I_{24\text{max}} = 550$ μA. Note that the resolution improvement factor, 64/51 = 1.25 correspond to the theoretical prediction. Furthermore, $2 \cdot R_{24}/(R_{13}/2)$ is slightly higher than 2. In other words, we should apply a slightly higher current than 1100 μA in phases 1 and 3 to get the best possible resolution. However, for experimental convenience, it was easier to keep the amplification ratio between phases 2-4 and 1-3 equal to two.

4. Conclusion

In this paper we have experimentally shown that the bi-current four-phase spinning current technique proposed in [10] is readily efficient to lower $1/f$ noise of Low-Voltage Vertical Hall devices. Thanks to this optimized technique, we were able to get a 51 μT resolution over a 1.6 kHz bandwidth with a very small 3 μm wide, 25 μm long VHD integrated in the shallow N-well (2 μm deep) of the AMS 0.35 μm CMOS technology, the effective biasing current being only 825 μA.

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