ALICE ITS upgrade for LHC Run 3: commissioning in the laboratory

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Abstract. ALICE is the CERN LHC experiment optimised for the study of the strongly interacting matter produced in heavy-ion collisions and devoted to the characterisation of the quark-gluon plasma. To achieve the physics program for LHC Run 3, a major upgrade of the experimental apparatus is ongoing. A key element of the upgrade is the substitution of the Inner Tracking System (ITS) with a completely new silicon-based detector whose features will allow the reconstruction of rare physics channels, not accessible with the previous layout. The enabling technology for such a performance boost is the adoption of custom-designed CMOS MAPS as detecting elements. The installation of the detector in the ALICE cavern is completed and few months of commissioning will allow the final integration into the central systems. In this talk, an overview of the adopted technologies as well as the status of the detector commissioning will be given.

1. ALICE experiment upgrade and Inner Tracking System during Run 3

ALICE (A Large Ion Collider Experiment) \[1\] is a general-purpose, heavy-ion experiment at the CERN LHC. Its main goal is to study the physics properties of the quark-gluon plasma. In LHC Run 3 and Run 4 ALICE will focus on rare processes such as production of heavy-flavour particles, quarkonium states, real and virtual photons and heavy nuclear states \[2\]. The earlier methods of triggering will be limited for many of these measurements, particularly at low-\(p_T\). Therefore, the ALICE collaboration planned to upgrade the Run 1/Run 2 detector by enhancing its low-momentum vertexing and tracking capability, allowing data taking at substantially higher rates and preserving the already remarkable particle identification capabilities. The upgraded experimental apparatus is designed to readout all Pb–Pb interactions, accumulating events corresponding to an integrated luminosity of more than 10 \(nb^{-1}\). This minimum-bias data sample will provide an increase in statistics by about a factor 100 with respect to data collected during Run 1/Run 2 data taking.

The main goals of the ITS upgrade (ITS 2) are an improved reconstruction of the primary vertex as well as decay vertices originating from heavy-flavour hadrons, and an enhanced performance for the detection of low-\(p_T\) particles. The design objectives are to improve the impact-parameter resolution by a factor of 3 and 5 in the \(r\phi\)- and \(z\)-coordinate, respectively, at a \(p_T\) of 500 MeV/c \[3\]. The tracking efficiency and the \(p_T\) resolution at low \(p_T\) will also improve. Additionally, the readout rate will be increased to 50 kHz in Pb–Pb and 400 kHz in pp collisions. In order to achieve this performances, the following measures were taken:
• Granularity increased by an additional seventh layer and by equipping all layers with pixel sensors having cell size of 29.24 $\mu m \times 26.88 \mu m$.
• Innermost detector layer moved closer to the interaction point, from 39 mm to 22.4 mm.
• Material budget reduced to 0.3% $X_0$ per layer for the innermost layers and to 1.0 % $X_0$ for the outer layers.

The ITS 2 will be the first large-area silicon tracker based on the CMOS Monolithic Active Pixel Sensor (MAPS) technology operating at a collider. The basic element of a layer is the stave, which consists of a carbon space frame, supporting the chips, to which the cold plate and the cooling ducts are attached. Based on geometrical position and a few mechanical characteristics, the detector can be pictured as assembled in two parts: the innermost three layers form the Inner Barrel (IB); the middle two and the outermost two layers form the Outer Barrel (OB). Layer radial positions were optimised to achieve the best combined performance in terms of pointing resolution, $p_T$ resolution and tracking efficiency in the expected high track-density environment of a Pb–Pb collision. The detector extends over a total surface of 10.3 m$^2$ and contains about $12.5 \times 10^9$ pixels with binary readout. The ALPIDE, the pixel chip developed for the ITS 2, has been designed to fulfill the requirements of both the IB and OB. It is manufactured using the TowerJazz 180 nm CMOS Imaging Sensor Process, has dimensions $15 \times 30$ mm$^2$ and hosts $512 \times 1024$ pixels. Each pixel cell contains a sensing diode, a front-end amplifier and shaping stage, a discriminator, as well as a multi-hit buffer. The pixels are arranged in double columns and read out by a priority encoder which sends the addresses of the pixels that recorded a hit to the chip peripheral readout circuitry. The digital periphery produces the digitized and zero-suppressed hit data and sends them to the Readout Units (RUs) through high-speed serial data links running at either 1.2 Gbps for the IB sensors or 400 Mbps for the OB sensors. Chip periphery interfaces also with a clock input, and a bi-directional control bus for configuration, control, and monitoring. The RUs, FPGA-based boards, are located outside the detector acceptance in a moderate radiation environment. They receive the triggers from the Central Trigger Processor (CTP) via optical link and ship the data to the Common Readout Units housed in the First Level Processor computers, located in control rooms, where the event reconstruction starts. The same data path is used to control the detector. Power to the stave is provided through a Power Board (PB), generating two 1.8 V supply voltages (for the analog and digital circuits of the pixel chip) and a negative voltage output for the reverse bias. The RUs and PUs are powered by a CAEN distribution system based on EASY3000 crates.

2. Commissioning in the laboratory
Detector was assembled in half-barrels (two, top and bottom, of the IB and two, top and bottom, of the OB) in a large clean room at CERN equipped with the same backend system that will be used in the experiment, including powering system, cooling system, full readout and trigger chains. The first completely assembled and connected half-barrel has been the IB top by July 2019; last one has been the OB bottom by January 2020. Continuous operation of the detector started in May 2019, supported by shift crews alternating along the day every 8 hours. Most of the activities of the standard shift crews have been performed on the IB. Standard data taking schedule foresees hourly execution of a threshold scan, a fake-hit rate run and a readout test. OB took longer for the final assembly and required more time for the complete integration in the system, due to larger number of elements. Most of the verifications performed on the OB staves have been done by detector experts.

2.1. Inner Barrel
During fake-hit rate runs, random triggers are sent to the chips and all the hits created in coincidence are collected. These hits come from the noise and also from cosmic rays crossing
the detector in coincidence with the trigger. In the left plot of Fig. 1 the measured fake-hit rate is plotted as a function of the threshold value for different numbers of masked noisier pixels. It can be seen that, for the target threshold value of 100 e\(^{-}\), masking a total of 10000 pixels, less than the 0.009\% of the considered acceptance, a fake-hit rate value of the order of \(10^{-10}\) hits/pixel/event can be achieved. This can even be improved applying a back-bias voltage of -3 V to the chips, reaching a fraction of masked pixels of the order of 0.0001\%. This is an important result, considering the really low fraction of masked acceptance and the fact that the target value for the fake-hit rate was \(10^{-6}\) hits/pixel/event [3].

Due to the very low recorded chip noise, hits coming from cosmic particles passing through the detector can be clustered together and used to reconstruct the associated tracks. Starting from tracks one can perform an alignment study to determine the displacement of staves in layers obtaining residuals of the order of 100 \(\mu m\). The overlap of the staves at the edges facilitates the reconstruction of a track from 6 aligned clusters in three layers (right plot of Fig. 1).

The quality selection criterion to consider a stave good for installation in the IB was to have a total amount of not working pixels below 50 among the 9 chips. After installation, the total number of pixels found to be dead were less than 1000 out of a total \(226 \times 10^6\) pixels of the full IB. This number is actually reduced with respect to the measurements done on the staves before installation in the barrel, thanks to improved stuck pixel identification and masking mechanism.

Readout tests are used to verify the quality of the data transmission from the chips to the associated RU performing a measurement of the Bit Error Rate (BER) through counting of 8b10b decoding errors. During the test, a fixed number of pixels are stimulated and the chip matrix is read out at a given rate. Multiple injected patterns (256, 512, 1008, 2048 and 4096 pixels) and readout rates (44.9 kHz, 67.3 kHz, 101 kHz, 123 kHz, 202 kHz and 247 kHz) were explored. From [3], a total of \(~250\) activated pixels are expected in case of 100 kHz Pb–Pb minimum-bias collisions with the unavoidable QED background, adding pixel noise of the order of \(10^{-5}\) hits/pixel/event, for an integration time of 30 \(\mu s\). Simulating an occupancy similar to the one described, a BER sensitivity of about \(10^{-12}\) was measured for all the readout rates mentioned above. The BER sensitivity was measured to be of the order of \(10^{-15}\) in a large statistics sample for the readout rate of 44.9 kHz. Under extreme conditions going significantly beyond the possible scenarios during data taking with beams, errors have been recorded on a limited amount of staves and with a rate of error of the order of \(~1/20\) hours.
Figure 2. First result of the OB stave fake-hit rate distribution without (top panel) and with (bottom panel) offline masking of noisier pixels.

2.2. Outer Barrel
Handling of very long and fragile objects, as the staves during the assembly of the layers and half-barrel, required the definition of a rigorous and yet delicate procedure. In spite of the complexity of the stave installation procedure, there was no increase in the number of dead chips, as ascertained from electrical and functional checks. The total number of dead chips over the full OB is 32, corresponding to the 0.14% of the acceptance; no overlap in the radial direction is present between the dead chips in the different layers.

A calibration campaign allowed to characterise the OB staves, and showed that a tuning to $100 \text{ e}^{-}$ threshold target with a $2 \text{ e}^{-}$ precision is possible, having a chip-to-chip spread within the stave of $20 \text{ e}^{-}$.

Due to the very large amount of chips installed in the OB staves ($\sim 24 \times 10^3$ chips), the selection criteria were released with respect to the chip used in the IB. As a consequence we do expect reduced performance in terms of noise. Nonetheless a fake-hit rate value of the order of $10^{-11}$ hits/pixel/event is reachable masking a mean value of 0.00036% of the acceptance (Figure 2). This value is again well below the requirement of fake-hit rate to be less than $10^{-6}$ hits/pixel/event [3].

A long term continuous powering campaign, to bring out events of early infant dead of staves and any service components (e.g. power supply modules), was carried out and no suspicious cases have been found.

3. Conclusions
The ongoing replacement of the ITS will extend the physics reach of ALICE to lower transverse momentum, allowing the characterisation of the QGP via measurements of unprecedented precision. The new ITS is now placed within the ALICE detector in its final position. Few months of standalone and global commissioning will prepare the detector to be ready to take the very first data with collisions in the foreseen LHC pilot run during October 2021.

[1] The ALICE Collaboration et al., JINST 3 S08002 (2008).
[2] The ALICE Collaboration et al., J. Phys. G 41 087001 (2014).
[3] The ALICE Collaboration et al., J. Phys. G 41 087002 (2014).
[4] M. Šulić (on behalf of the ALICE collaboration), in proceedings of the International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Pixel 2016), JINST 11 C11025 (2016).