A new enhanced-boost switched-capacitor quasi Z-source network

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Abstract

This paper proposes a new enhanced-boost non-transformer-based impedance source network. The strong boosting ability of the proposed topology is realized by making use of the switched capacitor concept in the formerly introduced enhanced-boost quasi Z-source network (EB-qZSN) without any additional active switch. Meanwhile, the advantages of the EB-qZSN such as input current continuity and shared ground between the input and the output are maintained. In addition to the lower shoot-through requirement to obtain high voltage gains, the proposed impedance network takes advantage of a smaller size of passive components along with a lower input current ripple to achieve higher power density and higher efficiency. Moreover, the lower total rating of the switching elements, defined by switching device power, directly translates to lower cost for the proposed method. The operation principles and the design guideline of components are explained in detail and a thorough comparison with other ZSN is presented. A 240W DC–DC prototype converter was built to validate the performance principles and properties of the proposed impedance network.

1 | INTRODUCTION

Nowadays the vast consumption of fossil fuel reserves and their corresponding environmental challenges cause a general inclination toward renewable energy resources. In addition to the fact that the renewable energy resources such as photovoltaic panels, deliver a low DC output voltage, the conventional voltage source inverters (VSIs) that are mainly used in the renewable energy systems, can only perform a buck functionality, which makes the use of a DC–DC boost converter unavoidable between them to comply with the AC bus standards. Consequently, this two-stage power conversion imposes higher cost, size and volume to the system and reduces the efficiency [1]. In addition, the EMI noises or gating pulse mismatches possibility of the VSIs may cause the input voltage source to short-circuit. Providing dead time in a VSI, switching pattern can address this problem, but it leads to output waveform distortions. To overcome these shortcomings, the concept of Z-source network (ZSN) was introduced in [2], which equips the VSIs with the ability of utilizing the shoot-through (ST) interval that is the simultaneous conduction of at least one leg of the inverter in zero state operation. The advantageous use of the ST state brings boosting ability and higher reliability against the input voltage source short-circuit for the system. Moreover, better output waveform quality is obtained because there is no need for dead time. Due to these interesting features, many research works are intended for applying the ZSNs to DC–AC power conversion applications with novel control algorithms and modulation schemes [3–5]. They are also adopted to DC–DC [6–8], AC–DC [9] and AC–AC [10] power converters. The flexibility of ZSNs for employing in many types of power converters is investigated in [11]. Despite the advantages, the conventional ZSN suffers from serious drawbacks which restrict its practical applications. Besides a low voltage gain, discontinuous input current and lack of a joint ground between the input and the H-bridge inverter can be mentioned as the main limitations of the conventional ZSN. It can be greatly improved by modifying the component arrangements, which is introduced as quasi ZSN (qZSN) [12]. However, it has the same small gain as the conventional ZSN, which is a major problem particularly in renewable energy systems requiring a wide range of voltage gains. The need for high ST intervals in a ZSN, which has a low input-to-output gain ratio yields high voltage stress on semiconductors of the H-bridge inverter, a low modulation index followed by a low output voltage quality and a reduced efficiency.

Various ZSN topologies have been put forward in literature with high voltage boost factors. The switched inductor (SL) is a well-known technique to augment the voltage gain of the
conventional qZSN and the qZSN. By replacing the inductors in these structures with SL cells, the SL-(q)ZSNs are realized [13], [14]. To further enlarge the boost capability, a novel SL-qZSN is proposed in [15], which utilizes the voltage-lifting unit in its structure. The extended-boost ZSNs proposed in [16], extend the output voltage gain range of the qZSN with extra passive components and diodes, which are arranged in two general manners called the capacitor/diode assisted ZSNs. The (quasi) switched boost networks (q)SBNs proposed in [17] and [18], offer the same voltage gain as that of the conventional ZSN in such a way that one LC pair is saved, although one additional active switch and one extra diode are used in these circuits. By integration of SLs in the SBN-based structures, higher boost factors can be obtained [19], [20]. Besides the high ripple of input current, circuit elements are faced with high voltage stresses in these structures. Further advancements in the SBN structures to achieve higher voltage gains are provided in [21] and [22], but there is no common ground between the input and the output. Another high-boost SBN-based structure is introduced in [23], which uses a low number of passive elements and diodes. However, the inconvenience of no common ground between the input and the output remains unsolved. In [24–26], the concept of the switched capacitor (SC) is used to realize a high voltage gain, but with the aid of an extra active switch. Another approach to realize a high-boost ZSN is to make use of coupled inductors [27–31]. In these types of ZSNs, high voltage gains can be achieved by adjusting the coupled inductors turn ratio. Nevertheless, they are prone to leakage inductances adverse effects, which can cause voltage spikes on switching devices and reduce the efficiency [32].

The enhanced-boost ZSN (EB-ZSN) demonstrated in Figure 1(a) offers a high gain with two switched impedance networks [33]. In comparison with the DA-ZSN and SL-ZSN, the EB-ZSN requires a lower ST duration to obtain the same voltage gain, which results in lower conduction losses and better output waveform quality. However, it suffers from a discontinuous input current and different ground points for the input and the output. These shortcomings have been tackled in the EB-qZSN [34] obtained by properly cascading the qZSN, as shown in Figure 1(b), while maintaining the same boost ability as that of the EB-ZSN with the same number of circuit elements. The active switch used in the EB-ASqZSN [35] is embedded in such a way that the same voltage gain as those of the EB-(q)ZSNs is achievable with two less LC pairs. The voltage gain of the active SL boost-qZSN (ASLB-qZSN) proposed in [36] is similar to those of the EB-(q)ZSNs. The advantages of the EB-qZSN are retained with one less LC pair and one additional active switch. However, the two latter structures are subjected to high voltage stresses on semiconductors. Besides, both require an extra isolated gate driver that can increase the system costs.

In this paper, a new EB-qZSN is proposed in which the realization of the SC concept helps to obtain a high voltage gain. Compared to the competitors, the proposed topology offers a stronger boost ability without any extra active switch. Meanwhile, it retains the advantages of the qZSN such as continuous input current and common ground for the input and the output. Furthermore, it has the advantage of higher power density over the competitors due to its lower size of passive components. Besides, lower rating semiconductors can be applied to this structure. Its low input current ripple allows us to use a low input inductor size. The steady-state performance principles and parameter designs are presented in Section 2 which are followed by the comparative analysis with other high-boost ZSNs discussed in Section 3. Experimental test results on a prototype DC–DC converter are given in Section 4 to verify the theoretical analysis. It should be noted that the proposed ZSN is examined through a DC–DC boost converter just for the sake of simplicity and it can be readily applied to other types of power conversion, the same as traditional ZSNs.

2 | THE PROPOSED TOPOLOGY

2.1 | Circuit derivation

Considering the EB-qZSN, illustrated in Figure 1(b), this topology is a cascaded structure of the qZSN [34]. Despite offering a high gain along with the mentioned advantages, the use of four inductors in this structure results in a bulky circuit, which increases the cost and weight of the converter. In order to obtain the same high-boost performance with higher power density, the SC concept is utilized in this topology, as shown in Figure 2, leading to the proposed structure with a stronger boost ability and an improved power density. Regarding the circuit configuration of the proposed topology, it is obvious that this structure is comprised of three inductors (L₁, L₂, L₃), four capacitors (C₁, C₂, C₃, C₄) and four diodes (D₁, D₂, D₃, D₄). It is worth mentioning that the switched-capacitor concept is
engendered by the effective placement of the capacitors \( (C_1, C_2) \) and the diodes \( (D_1, D_2) \) in harmony with the rest of the circuit components.

### 2.2 Performance analysis

The performance analysis of the proposed topology is carried out by considering two states of operations, ST and Non-ST states, which is a general assumption among all ZSNs. The behaviour of the proposed impedance network will be discussed in both ST and Non-ST states, as shown in Figure 3. In addition, the typical waveforms of elements are presented in Figure 4.

a. **ST state**: According to Figure 3(a), the ST state occurs when the active switch \( SW_o \) is turned ON. \( D_4 \) is blocking the reverse voltage of \( C_3 \) and \( C_3 \). Conduction of \( SW_o \) lets \( C_3 \) to discharge its stored energy to \( L_3 \). \( D_3 \) is forward-biased to provide the path for charging \( C_1 \) and \( L_1 \). As \( D_2 \) conducts, \( C_1 \) and \( L_2 \) receive energy in parallel from \( C_2 \) and \( C_4 \) discharging in series. \( D_1 \) is blocked due to the reverse voltage of \( C_1 \) and \( C_2 \). \( C_4 \) also forms a series-connected path with the input voltage source to charge \( L_1 \). Therefore, during this state, the currents of the inductors and the voltage of \( C_1 \) are linearly increased while the voltages of the \( C_2 \) to \( C_4 \) decrease, as shown in Figure 4. The following voltage equations can be obtained

\[
\begin{align*}
V_{L_1} &= V_{in} + V_{C_4} \\
V_{L_2} &= V_{C_1} \\
V_{L_3} &= V_{C_3} \\
V_{C_1} &= V_{C_2} + V_{C_4}
\end{align*}
\]  

(b) **Non-ST state**: In this operating state, the active switch \( SW_o \) is turned OFF, as shown in Figure 3(b). \( D_1 \) is forward-biased to provide the path for charging \( C_2 \). Therefore, \( D_2 \) is reverse-biased because it is in reverse parallel connection with \( C_1 \). As \( D_3 \) conducts, the series-connected path composed of the inductors \( L_1, L_2 \) and \( L_3 \) and the capacitor \( C_1 \) along with the input source discharge the stored energy for supplying the load. Meanwhile, \( C_3 \) and \( C_4 \) receive energy. \( D_3 \) is blocking the reverse voltage of \( C_3 \). Collectively, the voltages of \( C_2 \)
to \( C_4 \) change with a positive slope while the currents of the inductors and the voltage of \( C_1 \) decrease to their minimum values. The voltage equations can be written as

\[
\begin{align*}
V_{L_1} &= V_{i1} - V_{C_2} \\
V_{L_2} &= V_{C_1} + V_{C_2} - V_{C_3} \\
V_{L_3} &= -V_{C_4}
\end{align*}
\] (2)

The average voltage of an inductor over a switching period under steady-state condition is equal to zero. Thus, by applying volt-second balance to the inductors of the proposed topology, the voltage gain \((G)\) can be obtained as

\[
G = \frac{V_o}{V_i} = \frac{2 - D}{1 - 4D + 2D^2}
\] (3)

where \( D \) is the ST duty cycle. As can be seen, the term \((2-D)\) appears as the numerator in the voltage gain equation of the proposed topology. Unlike the SC-qZSN introduced in [25], the realization of the SC concept in the proposed method is such that no additional active switch is needed for the proposed impedance network.

### 2.3 Component parameters design

In order to design the inductors of the proposed topology, the maximum permitted ripple of the inductor currents must be taken into account as a design constraint. By supposing \( K_v^\% \) as the peak-to-peak ripple of inductor currents, the required inductances can be calculated based on (4)

\[
L = \frac{V_o D T}{K_v^\% I_L}
\] (4)

where \( V_o \) is the voltage across the inductors during the ST state and \( T \) is the switching period.

By substituting the corresponding values into (4), the following expressions can be used to design the inductors:

\[
\begin{align*}
L_1 &= \frac{D(1 - D)^2}{2 - D} G L_B \\
L_2 &= D G L_B \\
L_3 &= D(1 - D) G L_B
\end{align*}
\] (5)

The term \( L_B \) in the above equations is defined by (6), in which \( P \) is the nominal power of the converter

\[
L_B = \frac{V_i^2 T}{K_v^\% P}
\] (6)

The required capacitances for the proposed topology can be calculated based on the capacitor’s maximum tolerable voltage ripple which is supposed to be \( K_v^\% \). Then, this constraint can be expressed as (7), in which \( I_c \) is the current flowing through the capacitors during the ST mode

\[
C = \frac{I_c D T}{K_v^\% V_C}
\] (7)

Therefore, the required capacitances can be obtained by the following equations:

\[
\begin{align*}
C_1 &= (1 - D) \frac{C_B}{G} \\
C_2 &= \frac{1 - D}{1 - 3D + D^2} \frac{C_B}{G} \\
C_3 &= \frac{D}{1 - D} \frac{C_B}{G} \\
C_4 &= \frac{1 + D - D^2}{D(2 - D)} \frac{C_B}{G}
\end{align*}
\] (8)

where \( C_B \) is

\[
C_B = \frac{PT}{K_i^\% V_i^2}
\] (9)

Besides, the size of inductors and capacitors depends on their maximum stored energy [37], which are formulated as

\[
\begin{align*}
W_L &= \frac{1}{2} L f_i^2 \\
W_C &= \frac{1}{2} C V_c^2
\end{align*}
\] (10)

Based on (10), the total maximum stored energy of inductors and capacitors can be calculated for the proposed topology as

\[
\begin{align*}
W_{L_i}^{\text{tot}} &= \sum_{i=1}^{4} W_{L_i} = \frac{D(1 - D)(7 - 8D + 2D^2)}{(2 - D)(1 - 4D + 2D^2)} W_B \\
W_{C_i}^{\text{tot}} &= \sum_{i=1}^{3} W_{C_i} = \frac{1}{1 - 4D + 2D^2} W_B
\end{align*}
\] (11)

The term \( W_B \) in (11) is characterized by (12) as

\[
W_B = \frac{PT}{(K_v^\% \text{ or } K_i^\%)}
\] (12)

Voltage and current stresses of components of the proposed topology are summarized in Table 1, which can be used for semiconductors parameters selection.

### 3 Characteristics Comparison

A comprehensive comparison among the proposed impedance network and the non-transformer-based ZSNs previously introduced such as the DA-qZSN [16], the SL-ZSN [13], the
EB-ZSN [33], the EB-qZSN [34], the EB-ASqZSN [35], the HG-SZSN [22], the ASLB-qZSN [36], the HGAS-qZSN [26] and the HVG-qSBN [23] and is carried out, which is represented in Table 2. Obviously, the same input voltage, output power and voltage gain are supposed for all topologies. Among the mentioned ZSNs, the EB-(q)ZSNs, the EB-ASqZSN and the ASLB-qZSN, which have close similarities with the proposed impedance network, are selected in order to conduct a detailed comparative analysis. For the sake of a fair comparison, the boosting ability, components count, passive components size, semiconductors ratings and input current ripple of these ZSNs are investigated.

### 3.1 Boost ability

In Figure 5(a), the voltage gain profile as a function of the ST duty cycle for the proposed topology and the competitors is plotted. It can be observed from this figure that the proposed topology can produce an output voltage, which is almost twice higher than those of the EB-(q)ZSNs and the EB-ASqZSN under the same input voltage and ST duty cycle. Compared to the ASLB-qZSN, the proposed topology takes advantage of the higher boost ability to use lower ST duty cycles. This ability makes the proposed network an appropriate choice for DC–AC applications since it allows us to use higher modulation indices.

### 3.2 Components count

The number of passive/active components of the proposed structure and the competitors are compared, which are listed in Table 2. It should be noted that the components used only in the impedance networks are considered for this study. Compared to the EB-(q)ZSNs, one inductor and one diode are saved by the proposed topology and the same number of capacitors is used. In addition, the proposed topology uses one more capacitor but two fewer diodes and one less power switch in comparison with the ASLB-qZSN. It can be found that the total number of components including active and passive elements used in the EB-(q)ZSNs and the ASLB-qZSN is 13. However, it is 11 for the proposed topology. Considering the EB-ASqZSN, the proposed topology has two additional capacitors and one more inductor. Unlike the EB-ASqZSN, no active switch is used in its structure.

### 3.3 Passive components

In order to conduct a comparative study in terms of the volume of the passive components between the proposed topology and the competitors, the total maximum stored energy of the inductors and capacitors for each impedance network are computed based on (10) and then normalized according to (12). The results are plotted versus the voltage gain, as shown in Figure 5(b) and (c). It is evident from Figure 5(b) that the total maximum energy of inductors of the proposed topology is considerably lower than the competitors. Moreover, Figure 5(c) shows that the total maximum energy of the capacitors in these impedance networks is comparable. The lower overall size of magnetic elements of the proposed topology implies its higher power density compared to competitors.
| Z-source networks | L | C | D | S | Input current Continuity | Common ground | Voltage gain (G) | Capacitor voltages (Vc/Vm) | Diode voltages (Vd/Vm) | switch voltage (Vss/Vm) | Total blocking voltages (Vbb/Vm) | Inductor currents (Il) | ST current (Ist) |
|------------------|---|---|---|---|---------------------------|---------------|-------------------|---------------------------|-----------------------|------------------|-----------------------------|----------------|----------|
| DA-qZSN [16]     | 3 | 3 | 3 | 0 | Yes                        | Yes           | 1                | 1 - 3D + 2D²             | DG (1 - 2D)G       | —                | —                           | 3G             | (3 - 2D)P/V_m |
| SL-ZSN [13]      | 4 | 2 | 7 | 0 | No                         | No            | 1 + D             | 1 - 3D                   | DG 1 + D G         | —                | 4G             | 1 + D P/V_m                          | 4              | P/V_m    |
| EB-ZSN [33]      | 4 | 4 | 5 | 0 | No                         | No            | 1 - 4D + 2D²      | (1 - D)³ G              | DG (1 - D)G         | —                | 4G             | P/V_m                              | (4 - 2D)P/V_m | P/V_m   |
| EB-qZSN [34]     | 4 | 4 | 5 | 0 | Yes                        | Yes           | 1 - 4D + 2D²      | (1 - D)³ G              | DG (1 - D)G         | —                | 4G             | P/V_m                              | (4 - 2D)P/V_m | P/V_m   |
| EB-ASqZSN [35]   | 2 | 2 | 4 | 1 | Yes                        | Yes           | 1 - 4D + 2D²      | G                        | DG 2(1 - D)G        | —                | 6G             | P/V_m                              | (2 - D)P/V_m | P/V_m   |
| HG-SZSN [22]     | 2 | 2 | 2 | 1 | Yes                        | No            | 1 - 3D + D³       | (1 - D)G                 | DG                    | (1 - D)G         | (4 - 2D)G       | P/V_m                              | (2 - D)P/V_m | P/V_m   |
| ASLB-qZSN [36]   | 3 | 3 | 6 | 1 | Yes                        | Yes           | 1 - 4D + 2D²      | (1 - D)G                 | DG                    | (1 - D)G         | (7 - 3D)G       | P/V_m                              | (3 - D)P/V_m | P/V_m   |
| HGAS-qZSN [26]   | 2 | 3 | 5 | 1 | Yes                        | Yes           | 2 - D             | 1 - 4D + 2D²            | DG                    | G                | 4G             | P/V_m                              | (2 - D)P/V_m | P/V_m   |
| HVG-qSBN [23]    | 2 | 2 | 2 | 1 | Yes                        | No            | 1 - 4D + 2D²      | (1 - D)G                 | DG                    | (1 - D)G         | (4 - 2D)G       | P/V_m                              | (2 - D)P/V_m | P/V_m   |
| Proposed topology | 3 | 4 | 4 | 0 | Yes                        | Yes           | 2 - D             | 1 - 3D + D²             | DG                    | —                | 7 - 4D G          | P/V_m                              | 1 + 3D - 2D² / V_m | P/V_m |

Abbreviations: ASLB, active SL boost; DA, diode assisted; EB, enhanced boost; qZSN, quasi Z-source network; SL, switched inductor
3.4 Voltage and current stresses

In order to better investigate the requirements of semiconductors of the proposed topology, the total switching device power (SDP) is computed. The production of the voltage and current stresses of a switching device is defined as its SDP, which can be regarded as a criterion for measuring the requirements of the semiconductors and consequently, a cost indicator of the system. The corresponding expressions are [38]

\[
\begin{align*}
\text{total peak SDP: } SDP_{\text{peak}} &= \sum_{i=1}^{N} V_i I_i^{\text{peak}} \\
\text{total average SDP: } SDP_{\text{avg}} &= \sum_{i=1}^{N} V_i I_i^{\text{avg}}
\end{align*}
\]  

where \(i\) is the number of semiconductors used in the system, \(I_i^{\text{peak}}\) and \(I_i^{\text{avg}}\) are the peak and average currents flowing through the \(i\)th semiconductor and \(V_i\) is its peak voltage stress.

Accordingly, the total peak and average SDP of the proposed topology are calculated and normalized based on the output power. The results are compared with the competitors as shown in Figure 6(a) and (b). It can be seen from Figure 6(a) that the total peak SDP of the proposed topology is lower than that of the ASLB-qZSN for high values of the voltage gain. In addition, the total peak SDP obtained for the EB-(q)ZSNs and the EB-ASqZSN are the same which is lower than those for the proposed topology and the ASLB-qZSN. Figure 6(b) shows that for the whole range of voltage gain, the total average SDP of the proposed topology is the lowest among others.

3.5 Input current ripple

To compare the proposed topology with the competitors from the input current ripple profile point of view, Figure 6(c) is plotted assuming the same input inductance for all networks. Obviously, the EB-ZSN is not considered in this analysis due to its input current discontinuity. As can be seen from this figure, the proposed topology offers the minimum input current ripple in comparison with the other three competitors which have a continuous input current. Thus, this feature makes the proposed network a suitable solution for renewable energy applications.

Generally concluding, the proposed impedance network with high step-up capability offers improved features compared to its well-known competitors.

4 PRACTICAL EVALUATION

For verification of the functionality and properties of the proposed impedance network, it is implemented as a simple boost DC–DC converter depicted in Figure 7(a). In this realization,
the performance of impedance networks in ST and Non-ST states are mimicked by the ON and OFF modes of the switch (SW<sub>o</sub>) at the output side of the ZSN in parallel with the load, respectively [6], [7], [31]. The laboratory prototype converter is shown in Figure 7(b). The experimental parameters and test conditions are summarized in Table 3. The ST duty cycle is set to 0.144 which results in a voltage gain of 4 with respect to (3). Therefore, the theoretical output voltage can be calculated as 200 V, when the input voltage is set to 50 V. The measured experimental results are shown in Figure 8. The waveforms, shown in Figure 8(a), are the input and output voltages and currents. As can be seen from this figure, the output voltage is raised to 185 V from the 50 V input voltage which is slightly lower than the expected theoretical value already calculated as 200 V. This little difference comes from the equivalent series resistance of the inductors and the capacitors, the ON-state resistance of the MOSFET and the voltage drop of the diodes, ignored in theoretical boost factor calculation. The continuous input current feature of the proposed topology can be confirmed through the corresponding waveform shown in Figure 8(d). Another experimental test is carried out for the proposed network with \( V_{in} = 70 \) V and \( D = 0.086 \). The output voltage and load power are kept constant. The measured results are given in Figure 9. From Figure 9(a), the output voltage can be measured as 189.5 V. It can be found that the difference between the theoretical and measured values of the output voltage is lowered at \( 50 \) V when compared to the operation with 50 V input voltage. This is due to the fact that the ST duty cycle requirement and current stresses are lower for the 70 V input voltage operation than those for \( V_{in} = 50 \) V, leading to lower conduction losses. Based on Figure 9(b), the voltage across the capacitors \( C_1, C_2, C_3 \), and \( C_4 \) can be read as 89 V, 77 V, 175 V and 15.3 V, respectively. However, their theoretically calculated values are 95.5 V, 78 V, 182 V and 17.2 V. The experimental waveform of the inductor currents and diode blocking voltages represented in Figure 9(c) and (d) again support the performance principles.

To better demonstrate the difference between the theoretical and experimental voltage gain values of the proposed network, Figure 10(a) is plotted for \( V_{in} = 50 \) V and \( P_o = 240 \) W. As expected, the gap between the calculated and measured values tends to get increased when higher values of voltage gain are required which correspond to higher ST duty cycles and consequently, higher power losses. The efficiency comparison among the proposed network and the competitors is conducted under \( V_{in} = 50 \) V and \( G = 4 \) for different output power levels and the measured results are illustrated in Figure 10(b). According to this figure, for all ZSNs, the efficiency is decreased when the output power is increased since the conduction losses increase with the rise of output power. In addition, one can observe that the proposed topology offers higher efficiency than those of

### Table 3

| Parameter | Values |
|-----------|--------|
| Rated power, \( P_o/\text{[W]} \) | 240 |
| Input voltage, \( V_{in}/\text{[V]} \) | 50-70 |
| Output voltage, \( V_o/\text{[V]} \) | 200 |
| Switching frequency, \( f_{sw}/\text{[KHz]} \) | 20 |
| Inductances: \( L_1, L_2, L_3/\text{[mH]} \) | 0.5, 1.2, 1 |
| Capacitances: \( C_1, C_2, C_3, C_4)/\text{[µF]} \) | 68, 150, 68, 560, 470 |
| Power MOSFET: SW<sub>o</sub> | SPW47N60CFD |
| Diodes: \( D_1, D_2, D_3, D_4, D_5 \) | APT30D60S |

![Figure 8](image_url)

**Figure 8** Experimental waveforms of the proposed topology when \( V_{in} = 50 \) V and \( D = 0.144 \). (a) Input and output voltages and currents, (b) capacitor voltages, (c) inductor currents and voltage across switch SW<sub>o</sub>, (d) blocking voltage of diodes
FIGURE 9 Experimental waveforms of the proposed topology when $V_{in}=70$ V and $D=0.086$. (a) Input and output voltages and currents, (b) capacitor voltages, (c) inductor currents and voltage across switch $SW_o$, (d) blocking voltage of diodes

FIGURE 10 Efficiency comparative study (a) comparison of the theoretical and experimental voltage gain values under $V_{in}=50$ V and $P_o=240$ W, (b) efficiency comparison among the proposed topology and the competitors under $V_{in}=50$ V and $G=4$ with different output powers, (c) efficiency study of the proposed topology versus output power for 50 V and 70 V input voltage operations with the output voltage of 200 V

the EB-(q)ZSNs and ASLB-qZSN. However, the EB-ASqZSN offers the maximum efficiency compared to the others. In another study, the efficiency of the proposed impedance network as a function of output power is measured for the input voltages of 50 V and 70 V as shown in Figure 10(c). To obtain the output voltage of 200 V, when $V_{in}=70$ V, a lower ST duty cycle is needed when compared to that required for the test condition of $V_{in}=50$ V which results in lower power losses and improved efficiency. The loss distribution among the components of the under-study ZSNs is obtained using the analytical method in [27], for $V_{in}=50$ V, $G=4$ and $P_o=240$ W, and the results are summarized in Figure 11. Evidently, major losses come from the diodes and inductors and the power losses of diodes are dominant for all understudy ZSNs. The lower number of passive components used in the EB-ASqZSN and its lower ST current stress can be mentioned as the main factors in the improved efficiency of this structure which is the highest among others. The higher efficiency of the proposed structure compared to those of the EB-(q)ZSNs and ASLB-qZSN is mainly due to its lower ST requirement along with the smaller size of magnetic elements and the lower number of semiconductors employed in the proposed topology.

5 | CONCLUSION

A new high-boost ZSN is proposed in this paper. The proposed impedance network offers a higher voltage boost factor when compared to the traditional non-transformer-type ZSNs,
which implies its lower ST requirement. The lower voltage stress across the semiconductors allows us to use lower rating semiconductors. The lower size of passive components guarantees the higher power density of the proposed impedance network. Thus, improved efficiency is ensured for the proposed method. The continuous input current with a very low ripple and common ground between the input and the output are other advantages of the proposed topology. The operation principle, steady-state analysis, components design guideline and comparison with the conventional high-boost ZSNs were presented. The extensive experiments on a 240-W laboratory prototype confirm the steady-state operational concepts and theoretical results.

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