A Low Power 2.4 GHz CMOS Mixer Using Forward Body Bias Technique for Wireless Sensor Network

C.J. Yin¹, S.A.Z Murad¹, A. Harun¹, M.M. Ramli¹, T.Z.A Zulkifli² and J. Karim³

¹School of Microelectronic Engineering, Campus Pauh Putra, Universiti Malaysia Perlis, 02600 Arau, Perlis, Malaysia
²Electrical and Electronic Engineering Department, Universiti Technologi PETRONAS, 32610 Bandar Seri Iskandar, Perak, Malaysia
³Fakulti Kejuruteraan Elektrik, Universiti Teknologi MARA (UiTM), 40450 Shah Alam, Selangor, Malaysia

E-mail: sohiful@unimap.edu.my

Abstract. Wireless sensor network (WSN) is a highly-demanded application since the evolution of wireless generation which is often used in recent communication technology. A radio frequency (RF) transceiver in WSN should have a low power consumption to support long operating times of mobile devices. A down-conversion mixer is responsible for frequency translation in a receiver. By operating a down-conversion mixer at a low supply voltage, the power consumed by WSN receiver can be greatly reduced. This paper presents a development of low power CMOS mixer using forward body bias technique for wireless sensor network. The proposed mixer is implemented using CMOS 0.13 μm Silterra technology. The forward body bias technique is adopted to obtain low power consumption. The simulation results indicate that a low power consumption of 0.91 mW is achieved at 1.6 V supply voltage. Moreover, the conversion gain (CG) of 21.83 dB, the noise figure (NF) of 16.51 dB and the input-referred third-order intercept point (IIP3) of 8.0 dB at 2.4 GHz are obtained. The proposed mixer is suitable for wireless sensor network.

1. Introduction

Wireless sensor network (WSN) have grown enormously in the technology markets due to the rapid evolution of portable light weight devices. It can be made to real time monitoring to gather all of the required information of an object at a certain area. WSN are motivated based on its reliability, accuracy, flexibility, expense and power consumption. Battery usage does play a major concern in the WSN devices [1]. Therefore, power consumption reduction is needed to be made to enhance battery endurance ability as it is important in WSN technology for allowing long operating lifetime [2]. A proper architecture for the main building block is needed in order to achieve low power consumption for the overall WSN.

A mixer is one of the circuit blocks in RF transceiver. The mixer is employs to convert high frequency to low frequency spectrum or low frequency to high frequency spectrum that generated by the multiplication of two signals [2]. Nowadays, a low power mixer design is needed to accomplish the desired of the future market for WSN technology. However, when the circuit design is moving towards power consumption, the other parameters will generally impact the overall performance of the
system. Therefore, other important parameters such as conversion gain, linearity, port-to-port isolation and noise figure need to be considered in order to design high performance mixers [3].

2. Design procedure
Figure 1 shows the steps of designing a CMOS 2.4 GHz downconversion mixer using forward body bias technique for wireless sensor network in 0.13 μm Silterra technology. The schematic design and simulation will be done using Cadence software. The first stage in the design process is to estimate the values for each components element which are the design specification and component parameters of the mixer. Basically, the design procedure of the mixer comprise of optimizing several simulations until a desired mixer performance is achieved. The elements that are reflecting the mixer performance are conversion gain, linearity, power consumption and noise figure [4]. The circuit will be redesigned and/or properly readjusted the parameters if it does not meet the specification. By adjusting the circuit design as to optimize a particular performance parameter may serve to unintentionally degrade the other performance parameters. It is therefore important to monitor all of the performance parameters throughout the design process [5]. It is then followed by layout design implementation.

Figure 1. Design and simulation flow chart.
3. **Forward body bias technique**

The transistor can operate under lower voltage using a forward body bias technique. This is an effective ways to consume less power. The voltage across the gate and the source of a MOS transistor would drop by having a low supply voltage. Therefore, low threshold are needed to operate MOSFETs at low supply voltage. A low threshold voltage transistors utilizing current CMOS technologies can be obtained by circuit design techniques. A reverse or forward bias between the body (substrate) and source of a MOSFET can be applied when it is used as a four-terminal device [6].

Under the forward body bias technique, the MOSFET threshold voltage is reduced. Hence, the body-source junction of the NMOS transistor in the mixer will have a negligible leakage current. Body bias is the voltage source that is connected to the body terminal of transistors rather than to power or ground [7]. Figure 2 shows the forward body bias connection for NMOS and PMOS transistor. For this technique, the body is connected to a positive voltage source which allows for the reduction of the threshold voltage of the NMOS transistors. In this design, the biasing voltage will be set to a value that allows the transistors to operate in saturation region. The transistors with forward body bias would enter strong inversion region, while those with zero body bias is in weak inversion region. It is therefore resulting in low supply voltage and subsequently low power consumption [8].

![Figure 2](image)

**Figure 2.** A forward body biased (a) NMOS transistor, (b) PMOS transistor.

4. **Circuit implementation**

Figure 3 shows the proposed schematic of 2.4 GHz CMOS down-conversion mixer. The proposed circuit consists of three stages which are transconductance stage, switching stage and output stage. Transistor M1 and M2 represent the transconductance (RF) stage. The transconductance stage obtains an RF signal and the output current is matching to a voltage of the RF signal. Transistors M3 to M6 represent the switching (LO) stage. The purpose of having switching stage as a frequency translation of RF signal into an intermediate frequency (IF) signal by converting the current which produce from transconductance stage of the circuit in response to local oscillator (LO) signal. The switching NMOS transistors’ body is connected to a bias voltage (VBULK) in the circuit for forward body bias technique. The purposed technique is used to decrease the threshold voltage of the transistors and thus reduce the supply voltage and subsequently power consumption.

Inductors (L1, L2, L3 and L4) and capacitors (C1, C2, C3 and C4) act as input matching of 50 Ω in order to match the impedance between input port and transconductance stage to force the load impedance to be the complex conjugate of the source impedance. Therefore, the maximum power can be transferred to the load. Furthermore, low power consumption and high conversion gain can be optimized at the load stage through resistor R1 and R2.
Cascade LC network, which is also known as resonant circuit, consists of inductors (L5-L8) and capacitor (C5-C12) are connected at the IF output stage to function as low pass filter (LPF). The undesired high frequency at the output can be removed through LPF at the output stage to allow signal to pass through with low frequency to produce low level power consumption. Voltage headroom problems occur through higher current at the switching transistor. The large current reduces load size and thus reduces the voltage conversion gain of the mixer [7]. Therefore, current-bleeding PMOS transistors (M7 and M8) are introduced in LO stage to reduce the bias current of the LO switches. The current-bleeding also can increase the current flow in RF transconductance stage to improve the conversion gain [8]. PMOS transistors are used instead of NMOS due to the fact that PMOS is less prone to noise. Inductor L13 and L14 are placed at the source of RF input transistor to function as source degeneration inductor. The inductive source degeneration technique is utilized to improve linearity performance and provide the input impedance matching [9]. Transistor M0 is used as a current source in a double-balanced differential topology to control mixer tail current so as to adjust conversion gain of transconductance stage.

![Figure 3. Schematic of the proposed 2.4 GHz CMOS mixer using forward body bias technique.](image)

Table 1 shows the list of biasing voltage, transistors’ size and all components values of the proposed mixer. The supply voltage 1.6 V is chosen to obtain good conversion gain. The biasing is selected below 1 V to ensure low power consumption. The forward body bias technique for M3, M4, M5 and M6 is connected with V_BULK 0.6 V. The value of R1 and R2 is optimized at 2 kΩ for good conversion gain. The value of C1, C2, C3 and C4 are good enough as an input matching and DC block.
Table 1. List of biasing, transistors size and component.

| Components       | Parameters     |
|------------------|----------------|
| VDD              | 1.6 V          |
| VBULK            | 0.6 V          |
| VB_RF, VB_LO     | 0.8 V          |
| VP, VB_CS        | 0.8 V          |
| R1, R2           | 2 kΩ           |
| C1, C2, C3, C4   | 10 pF          |
| L1, L2           | 20 nH          |
| L3, L4           | 1 nH           |
| M0               | 2.5 µm / 0.13 µm |
| M1, M2           | 6.0 µm / 0.13 µm |
| M3, M4, M5, M6   | 3.5 µm / 0.13 µm |
| M7, M8           | 2.5 µm / 0.13 µm |

The transistors size of transconductance stage is chosen larger than switching stage transistors size as a tradeoff between conversion gain and linearity. The size of transistors M7 and M8 are optimized for providing enough bias current to switching stage.

5. Simulation result

A 2.4 GHz RF input signal mixer is down-converted to a lower frequency IF output signal through a LO signal of 2.3 GHz using CMOS 0.13 µm process. All the parasitic effects from resistors, capacitors and inductors are taken into consideration during simulation. The conversion gain (CG) corresponding to the LO input power is obtained by using a small signal analysis in Cadence SpectreRF. Figure 4 shows the CG of the proposed mixer. It is observed that the mixer provides the conversion gain when the LO input power is varied between −20 dBm to 10 dBm. The higher conversion gain of 21.83 dB is obtained at LO input power of 1 dBm. The linearity of the switching transistor pairs can become worse for large LO power. Therefore, a LO input power of 0 dBm is chosen.
Figure 4. Conversion gain of the proposed mixer

Figure 5 shows the simulated noise figure of the proposed mixer from 100 Hz to 100 MHz. It can be seen that the noise figure of 16.51 dB is obtained at 10 MHz frequency.

Figure 5. Noise figure of the proposed mixer.

The performances of linearity are measured by P1dB compression point and the third-order intercept point (IIP3). P1dB and IIP3 are simulated by using small signal analysis with the RF input power is swept from −70 dB to 10 dB. Figure 6 depicts the extrapolated P1 dB compression point of −10 dBm is achieved. The two tone test of IIP3 performance is employed. The second tone that is a small tone close to the RF frequency is applied. A 2.40 GHz and 2.41 GHz input frequency is choose at 10 MHz
separation with -20 dBm RF input power and 0 dBm LO power is applied, respectively. Figure 7 represents the simulated result of IIP3. The IIP3 of 8 dBm is achieved.

![Figure 6](image1.png)

**Figure 6.** 1-dB compression point.

![Figure 7](image2.png)

**Figure 7.** Third-order intercept point (IIP3).

Figure 8 depicts the proposed mixer layout which performed in Cadence Virtuoso Layout. The complete layout is designed symmetrically for differential operation to avoid mismatches in the differential circuit. The parasitic capacitance from the input and output interconnects can be
minimized using top 6 metal. A low parasitic effect can be obtained for longer distance from a substrate. The proposed mixer layout occupied a total die area of 1.96 mm x 1.71 mm including the pads. The fabrication process could take place in the near future.

In the case of RF circuits, the performance of the implemented design is to a great extent dependent on the way the circuit is laid out. This is mainly due to the fact that the parasitic coupling between interconnects and devices and/or the substrate is relatively high. In addition, RF circuits are more sensitive to parasitic resistance, inductance and capacitances associated with the interconnects. These undesired couplings and parasitics would affect the performance of the circuit [12].

![Figure 8. Layout of the proposed mixer.](image)

Table 2 shows the proposed mixer performances are compared with the previously published works. As can be seen, the forward body bias technique could achieve low power consumption with good CG and linearity as compare with the previous work. However, the proposed mixer’s noise figure is slightly higher. Therefore, the proposed mixer can obtain low power, high CG and good linearity with other performances are comparable.

| Reference | [13] | [14] | [15] | [16] | [17] | This work |
|-----------|------|------|------|------|------|-----------|
| Technology (μm) | 0.13 | 0.18 | 0.13 | 0.13 | 0.18 | 0.13 |
| Supply voltage (V) | 1.2 | 1.8 | 1.3 | 1.8 | 1.0 | 1.6 |
| RF (GHz) | 2.4 | 2.4 | 2.4 | 2.4 | 2.4 | 2.4 |
| LO power (dBm) | 0 | 5 | 4 | N/A | -13 | 5 |
| Conversion gain (dB) | 15.2 | 25 | 12.9 | 8.8 | 13.8 | 21.8 |
| IIP3 (dBm) | -6.7 | -24.7 | 0 | 0 | -7.2 | 8 |
| Noise figure (dB) | 16.3 | 19.1 | 7.40 | 5.2 | 13.3 | 16.5 |
| Power consumption (mW) | 6.0 | 8.7 | 2.8 | 1.6 | 0.5 | 0.9 |
| Chip area (mm²) | 0.12 | 0.05 | N/A | 1.13 | N/A | 3.35 |
6. Conclusion
A 2.4 GHz low power CMOS mixer using forward body bias technique for wireless sensor network is presented. The proposed mixer is implemented using CMOS 0.13 μm Silterra technology. A low power consumption is obtained using forward body bias technique. The simulation results show that a low power consumption of 0.91 mW is achieved at 1.6 V supply voltage with the conversion gain (CG) of 21.83 dB, the noise figure (NF) of 16.51 dB and the input-referred third-order intercept point (IIP3) of 8.0 dB at 2.4 GHz are obtained. The proposed mixer is suitable for wireless sensor network.

Acknowledgments
This work is supported and contributed from FRGS grant (9003-00387) that enabled the production of this article.

References
[1] T. H. Lin, W. J. Kaiser and G. J. Pottie 2004 Integrated Low-Power Communication System Design for Wireless Sensor Networks IEEE Comm. Magazine 142-150
[2] Murad, S. A. Z., et al. 2013 High gain 2.4 GHz CMOS low noise amplifier for wireless sensor network applications. Conf. IEEE Inter. RF and Microwave (RFM)
[3] Murad, S.A.Z, Shahimin, M.M., Pokharel, R.K., Kanaya, H. and Yoshida, K. 2012 Linearity improvement of 5.2 GHz CMOS up-conversion mixer for wireless applications. Micro. and Opt. Tech. Lett. 54 923-925
[4] Jouri. M, Golmakani Abbas, Yahyabadi. M and Khosrowjerdi. H. 2010 Design and simulation of a down-conversion CMOS mixer for UWB Applications Proc. Electrical Engineering/Electronics Computer Telecommunications and Information Technology (ECTI-CON)
[5] Y. H. Dai and Christina F. Jou 2013 A 5.15-5.825 GHz high-gain and low-noise cmos down-conversion mixer with low-power for WLAN 802.11a Proc. IEEE MTT-S International Microwave Workshop Series on RF and Wireless Technologies for Biomedical and Healthcare Applications (IMWS-BIO)
[6] Anishaziela Azizan and Sohiful Anuar Zainol Murad 2016 A 0.3 mW 2.4 GHz Low Power Low Noise Amplifier using Forward Body Bias Technique for Wireless Sensor Network J. Teknologi (Sciences & Engineering) 31-37
[7] Murad, S. A. Z., et al. 2017 Ultra-Low Power CMOS RF Mixer for Wireless Sensor Networks Application: A Review MATEC Web of Conf. 97, EDP Sciences
[8] Azizan, A., et al. 2015 Design of a 2.4 GHz CMOS LNA using two-stage forward body bias technique for WSN application Conf. IEEE Research and Development (SCORED)
[9] F. Jiang 2013 Broadband Low-Noise CMOS Mixers for Wireless Communications (Ontario, Canada)
[10] Ramiah, Harikrishnan, Jeevan Kanesan, and Tun Zainal Azni Zulkifli 2013 A CMOS up-conversion mixer in 0.18 μm technology for IEEE 802.11 a WLAN application. IETE J. of Res. 59, 454-460
[11] T.-Y. Y. Myoung-Gyun Kim 2014 Analysis and Design of Feedforward Linearity-Improved Mixer Using Inductive Source Degeneration IEEE Trans. On Micro The. and Tech. 62, 323-331
[12] Y. H. Chang, C. Y. Huang and Y. C. Chiang 2012 A 24 GHz down-conversion mixer with low noise and high gain. Conf. Microwave Integrated Circuits (EuMIC)
[13] Chong, W. K., et al. 2014 Design of inductorless, low power, high conversion gain CMOS subharmonic mixer for 2.4 GHz application. Conf. IEEE Inter. Microwave and RF
[14] Patil, Santosh B., and Rajendra D. Kanphade 2015 A 2.4 GHz double balanced differential input single output low power transmitting mixer in TSMC 180nm CMOS RF process. Int. Conf. on IEEE Electronics and Communication Systems
[15] Mahmoud, Fatma M., and M. A. Abdelghany 2016 Low flicker-noise RF CMOS gilbert-cell mixer for 2.4 GHz wireless communication systems. *Int. Conf. on IEEE Electrical, Electronics, and Optimization Techniques*

[16] Murad, S. A. Z., et al. 2016 Low noise figure 2.4 GHz down conversion CMOS mixer for wireless sensor network application. *IEEE Student Conf. on Research and Development (SCOReD)*

[17] Harisankar, P. S., Mayank Chakraverty, and Vaibhav Ruparelia 2016 Analysis of process and temperature variations on a 2.4 GHz RF CMOS down conversion subthreshold mixer *Int. Conf. on IEEE Energy Efficient Technologies for Sustainability (ICEETS)*