Coupled Inductance Three-Level Cuk Converter

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Abstract. A three-level Cuk converter with coupled inductance is proposed in this paper. Based on the research and design of existing three-level Cuk converter and Cuk converter with coupling inductance, this paper combines three-level technology with coupling inductance, which is called the “three-level coupled inductance Cuk converter” in this paper[1-3]. Compared with the existing converter, it has the advantages of boost capability and energy conversion efficiency. This kind of converter integrates the low voltage stress of the switch with three-level DC-DC converter and the boost function of the DC-DC converter with coupling inductance[4-6]. The three-level structure reduces the voltage stress when the switch is turned off, while the coupling inductance structure greatly improves the boost capability of the circuit. The working principle and periodic mode of three-level coupled inductor Cuk circuit are analysed, and the mathematical formula of voltage gain is deduced.

1. Introduction
At present, DC-DC converter is widely used in industrial production. For example, photovoltaic power generation, multi motor HVDC distribution system, UPS system. Apart from high voltage gain, it also requires high efficiency, low electromagnetic interference noise, high switching frequency, fewer components and so on.

The basic topology of Cuk converter can satisfy the requirement of fewer components, but the duty must be infinitely close to one hundred when we need high voltage gain, which makes the efficiency of the circuit dramatically reduced and the safety factor reduced, correspondingly. In the titled as “Research on high gain three-level zeta converter”[1] is proposed to increase voltage gain by introducing coupling winding. This can avoid the emergence of extreme duty ratio, while circuit output high-gain voltage. However, the voltage stress on the switch will rise sharply due to the release of leakage inductance energy, which will affect the the components’s service life and topological efficiency. The three level Buck-Boost converter proposed in paper titled as “Research on a new quasi-Z source three-level Boost DC converter”[2], reduced the stress of the switch and capacitor by half by adding a switch and cap capacitor correspondingly, but it can not meet the requirement of high voltage gain.

On the basis of summarizing all the characteristics of the above topology, a three-level Cuk DC converter with coupling inductor is proposed for meeting the industrialization requirements of this kind of topology. For the converter in this paper, the high voltage gain is achieved by adding coupling windings, and a switch and capacitor is introduced symmetrically on the basis of the original circuit, which can reduce the stress of the switch and capacitor. Under the same conditions, the limit duty ratio can be avoided in this way, the switching frequency of the circuit can be increased, and the security of the topology can be guaranteed. By adding a diode, the leakage inductance energy of the topology is
transmitted to the output capacitor through the diode, thus further improving the efficiency of the circuit. On the basis of this new topology, a series of theoretical analyses are carried out through the detailed description of its work process, the analysis and derivation of voltage gain formula, the establishment simulation of the main circuit model. Finally, the new topology proposed in this paper is verified by the test prototype.

2. Working principle and steady state analysis

Figure 1 shows the circuit diagram of the leakage inductance and the parasitic capacitance of the switch. Compared with the basic circuit, the topology first adds a switching and capacitor by three-level transformation to the basic circuit and keeps symmetry, so that the voltage stress of the switch and capacitor can be reduced by half accordingly; then by introducing coupling windings, the limiting duty ratio can be avoided when the requirements of increasing voltage is needed. Finally, a diode is connected in parallel at the end of the coupling winding to reduce the voltage stress on the switch and the energy loss during charging when the leakage inductance discharge occurs, so as to improve the efficiency of the circuit.

![Figure 1. Circuit principle](image1)

When considering the leakage inductance and parasitic capacitance of the switch, the work cycle can be divided into the following eight stages, in which stage 3 is divided into two small stages: A and B. Figure 2 is the voltage and current waveform of the key components when considering the leakage inductance of the circuit.

![Figure 2. Key device voltage current waveform](image2)

![Figure 3. Work status of Phase 1 and Phase2](image3)

![Figure 4. Phase 3 working state](image4)

Stage 1[t0-t1]: as shown in Figure 3. Switch conducts. The excitation inductor L1 is charged through the loop Vg - L1 - L1k - S1 - S2, while inductor L2 is discharged and inductor L0 is charged. Capacitor C1, C2 is discharged slowly, parasitic capacitance Cst is charged. The discharge of leakage inductance L2k increases the reverse voltage of diode D3 at this stage, which leads to the increase of leakage current.

Stage 2[t1-t2]: as shown in Figure 3. Switch S1 and S2 continue to turn on. The leakage inductance ends the discharge, and the excitation inductance L1 continues to charge through the original current...
loop, and the inductance $L_0$ continues to charge. This stage is the main energy storage stage of the whole cycle. $C_1$ and $C_2$ end the process of slow discharge in the Stage1. The discharge speed increases. The released energy is used for the inductor $L_0$ to store energy, which is prepared for the discharge of voltage rise later.

Stage 3[$t_2$~$t_3$]: as shown in Figure 4. Switch tube and all conduction. In phase 3, inductors $L_0$ and $L_1$ discharge, inductance $L_3$ charges. The $C_{S2}$ which is the parasitic capacitance of switch $S_2$ is discharged. As a result of the discharge of leakage inductance $L_{1k}$, the peak voltage of the switch $S_2$ is generated, which reduces the peak voltage of $S_2$ greatly. Thus diode $D_4$ is turned on. In stage 3, the capacitor $C_3$ is charged, and the current direction is reversed once. The states of the other devices remain unchanged. The state before the reverse of the $i_{C2}$ is called state a, and after the reverse is called state B.

![Figure 5. Working state of phase 4, phase 5, phase 6](image)

Stage 4[$t_3$~$t_4$]: as shown in Figure 5. The switch $S_1$ is turned on and the $S_2$ is turned off. The inductor $L_1$ is charged by input voltage $V_g$ and inductor $L_3$, inductor $L_0$, $L_2$, capacitor $C_1$ are discharged. The load side will be charged by the original energy storage of the previous stage.

Stage 5[$t_4$~$t_5$]: as shown in Figure 5. Switch conducts. The excitation inductor $L_1$ is charged through the current loop $V_g$ - $L_1$ - $L_{1k}$ - $S_1$ - $S_2$, inductor $L_3$ is discharged, inductor $L_0$ is charged. Capacitor $C_1$, $C_2$ is discharged slowly, parasitic capacitance $C_{S1}$ is charged. As the result of the leakage inductance $L_{1k}$ discharge, the reverse voltage of diode $D_4$ increases at this stage, which leads to the increase of leakage current.

Stage 6[$t_5$~$t_6$]: as shown in Figure 5. Switch tube $S_1$ and $S_2$ continue to turn on. The leakage inductance ends the discharge, and the excitation inductance $L_1$ continues to be charged through the original current loop, and the inductance $L_0$ continues to be charged. This stage is the main energy storage stage of the whole circuit. Capacitors $C_1$ and $C_2$ end the process of slow discharge in the last stage. The discharge speed is increased. The released energy is used for the energy storage of inductor $L_0$, which is ready for the discharge of voltage rise later.

Stage 7[$t_6$~$t_7$]: as shown in Figure 6. Switch conducts. In stage 7, inductors $L_0$ and $L_1$ are discharged, inductance $L_2$ is charged. The $C_{S1}$ which is the parasitic capacitance of switch $S_1$ is discharged. The leakage $L_{1k}$ discharge causes the peak voltage of the switch $S_1$. The peak voltage generated by the discharge of leakage inductance $L_{1k}$ is added to the diode $D_3$ to turn it on, which enables the capacitor $C_2$ to be charged faster and reduces the peak voltage borne by the switch $S_1$. In stage 7, the capacitor $C_1$ is charged and the current direction is reversed once. The states of the other devices remain unchanged. The state before the reverse of the $i_{C1}$ is called state a, and after the reverse is called state B.
Stage 8\([t_7\sim t_8]\): as shown in Figure 7. The switch S_2 is turned on and the S_1 is turned off. The inductor L_1 are charged by input voltage V_g and inductor L_2 are charged. Inductor L_0, L_2, capacitor C_1 are all discharged. At the previous stage, the original energy storage will discharge to the load side.

Without considering leakage inductance and some parasitic parameters, the static operating point of the system can be expressed as:

\[
\begin{bmatrix}
\frac{di_{1a}}{dt} \\
\frac{di_{2a}}{dt} \\
\frac{dv_{c1}}{dt} \\
\frac{dv_{c2}}{dt} \\
\frac{dv_{c3}}{dt}
\end{bmatrix}
= A
\begin{bmatrix}
i_{1a} \\
i_{1b} \\
v_{c1} \\
v_{c2} \\
v_{c3}
\end{bmatrix}
+ B
\begin{bmatrix}
v_0 \\
v_3 \\
v_4 \\
v_e
\end{bmatrix}
\tag{1}
\]

In this paper, steady state analysis of four states is carried out: the two switches of S_1 and S_2 are conducted at the same time\([t_8\sim t_9]\), the switch S_1 is turned on, S_2 is turned off\([t_9\sim t_{10}]\), the two switches of S_1 and S_2 are conducted at the same time\([t_{10}\sim t_{11}]\), the switch S_1 turns off and the S_2 turns on\([t_{11}\sim t_{12}]\). A_1, B_1, A_2, B_2, A_3, B_3, A_4 and B_4 can be obtained.

according to:

\[
A = A \left(D - \frac{1}{2}\right)^* 2 + A_2 (1-D) + A_3 (1-D)
\]

\[
B = B_2 \left(D - \frac{1}{2}\right)^* 2 + B_3 (1-D) + B_4 (1-D)
\]

we can get A, B:

\[
A = \begin{bmatrix}
A_{11} & A_{12} & A_{13} & A_{14} & A_{15} \\
A_{21} & A_{22} & A_{23} & A_{24} & 0 \\
A_{31} & A_{32} & 0 & 0 & 0 \\
A_{41} & A_{42} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0
\end{bmatrix}
\tag{2}
\]

\[
B = \begin{bmatrix}
1-D & 1-D & 2(n-1-D) & 2(n-1-D) & 2(n-1-D)
L_{n+1} & L_{n+1} & L_{n+1} & L_{n+1} & L_{n+1}
1-D & 1-D & 2(n-D-n+1) & 2(n-D-n+1) & 2(n-D-n+1)
L_{n+1} & L_{n+1} & L_{n+1} & L_{n+1} & L_{n+1}
0 & 0 & 0 & 0 & 0
0 & 0 & 0 & 0 & 0
0 & 0 & 0 & 0 & 0
\end{bmatrix}
\tag{3}
\]

After substitution, without considering leakage inductance, the voltage gain and circuit efficiency of the topologies obtained by several simultaneous formulas are as follows:

\[
B = V_i / V_g - n(1-2D) - D + (1-D)((V_{g_{in}} + V_{g_{out}}) / V_g)
\]

\[
\eta = V_i / V_{g_{in}} - n(1-2D) - D + (1-D)((V_{g_{in}} + V_{g_{out}}) / V_{g_{in}})
\tag{4}
\]

\[
\frac{1-D}{D[1+n(2D-1)+2(1-D)]}
\]

Figure 6. Phase 7 working state

Figure 7. Phase 8 working state
By formula (4), the relationship between duty and voltage gain, duty and topological efficiency in different turn-to-turn ratios can be plotted, when taking parasitic parameters such as on-resistance of switch, parasitic resistance of coupling inductance and voltage drop of diode into account. Figure 8 shows the relationship between duty and voltage gain under different turns ratio. As can be seen from the figure, with the increase of duty, the voltage gain basically shows an upward trend, and the rising rate is faster and faster, but when exceeding a certain limit value, the voltage gain begins to decline rapidly; and under the same duty, the larger the turn ratio of the coupling winding is, the greater the voltage gain can be achieved. This shows that the addition of coupling windings can improve the voltage gain of the topology and ensure the avoidance of the occurrence of limit duty.

\[
\begin{align*}
    a &= \frac{1-D}{R} \\
    b &= \frac{D(2D-1)(D+n(n+1)+2D^2(1-D))}{(1-D)R} \\
    c &= \frac{2D-1}{R} \\
    d &= \frac{(2D-1)(D(n+1)^2-n(1-D))}{(1-D)R}
\end{align*}
\]

(5)

Figure 8. Duty cycle curve

Figure 9. Efficiency graph

Figure 9 shows the relationship between duty and topology efficiency under different turns ratio. It can be seen from the graph that the efficiency of the topology increases with the increase of duty when the turn-to-turn ratio is fixed, but it decreases rapidly when the duty exceeds its limit value. When the duty is fixed, the efficiency of the topology increases with the increase of the turn-to-turn ratio, and the greater the turn-to-turn ratio, the topology efficiency reaches its maximum value. The duty will decrease correspondingly according to Saber simulation.

Figure 10 is a picture of Saber simulation.
3. Conclusion
It can be seen that under the same conditions, the efficiency and voltage gain increase with the increase of the topological turn ratio. Moreover, regardless of the turn ratio of the coupling winding, the corresponding voltage gain curve and efficiency curve will decrease sharply after a certain maximum value appears. This shows that the optimal duty should be selected according to the curve of voltage gain and topological efficiency to ensure that the circuit can work in the optimal state without limiting duty.

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