Design of Function Signal Generator Based on DDFS

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Abstract. The system is designed to construct a Function Signal Generator based on Direct Digital Frequency Synthesis Technology (DDFS), in which MCU and FPGA are the key components and necessary peripheral circuits are provided. Its main modules are responsible for the formation of oscillogram, the frequency synthesis, the digital-to-analog transformation, the control of range, and back-stage treatment, the user interface and other necessary modules. MCU controls FPGA to generate the oscillogram and other control words, and the FPGA controls output waveform and frequency synthesis. Amplitude control is realized by 2 DA. Low-pass filter and Transistor push-pull power amplification circuit are used to increase the quality of the output waveform and its loading capacity, and display the signal on the LCD. The system constitutes of 2 DAC and the FPGA, so that realizes the expanded requirements of 1 Hz-1MHz of the four waveform output.

1. Introduction

The frequency synthesis module is an important component of the function signal generator. Generally, direct frequency synthesis technology, phase-locked loop frequency synthesizer, and direct digital frequency synthesis technology (DDFS) can be used\textsuperscript{[1]}. Among them, DDFS (Direct Digital Frequency Synthesis) is a frequency synthesis technology that has developed rapidly in recent years. It has the advantages of high frequency resolution, fast frequency switching speed, low phase noise, and high frequency stability\textsuperscript{[2]}. This system adopts digital frequency synthesis technology to realize the design of the function signal generator, and completes 4 kinds of waveform output from 1Hz-1MHz.

2. Theoretical analysis and calculation

Direct Digital Frequency Synthesis (DDFS) consists of an N-bit word binary adder and an N-bit phase register controlled by a fixed clock. The output of the phase register is connected to one input of the accumulator, and the frequency control word K sent by the MCU is synchronously registered and connected to the other input of the accumulator\textsuperscript{[3]}. In this way, when each clock pulse arrives, the phase register samples the sum of the value in the previous clock cycle and the frequency control word K, and takes the upper part as the output sequence of this clock cycle\textsuperscript{[4]}. The frequency control word K determines the corresponding phase increment, and the phase accumulator continuously linearly accumulates the phase increment. When the phase accumulator is full, an overflow occurs, thereby completing a frequency cycle of the DDFS synthesis signal\textsuperscript{[5]}. The DDFS schematic is shown in Figure 1.
Figure 1. Principle block diagram of direct digital frequency synthesis.

The output frequency \( f_{out} \) and step \( \sigma_f \) of DDFS can be expressed as:

\[
f_{out} = \frac{K}{2^N} \times f_{clk}
\]

\[
\sigma_f = f_{clk} \times \frac{K}{2^N}
\]

Among them, \( N \) is the word length of the phase accumulator; \( f_{clk} \) is the frequency of the reference clock signal; \( K \) is the frequency control word. The system requires the waveform frequency range from 1Hz to 1MHz, and the minimum step is 1Hz. In order to extend the frequency to 1MHz and the step to 1Hz, according to the formulae (1) and formulae (2), a waveform table with a width of 10 bits and a depth of 256 bits is selected (that is, each cycle has 256 points). The phase accumulator word length \( N \) is 30 bits \( (2^{30} = 1073741825) \), and the reference clock is directly output by a 50MHz crystal, so that \( 2^N = 21 \times f_{clk} \), so the output frequency \( f_{out} \) is approximately equal to the frequency control word \( K/21 \), and the step is \( \sigma_f = 40MHz \times \frac{K}{2^{30}} = 25MHz \). Change the value of \( K \) to achieve adjustable frequency segmentation.

The frequency controller word \( K \) is 29 bits. According to the Nyquist sampling rule, there must be at least 2 sampling points in a cycle, so the maximum output frequency is

\[
f_{out} = \frac{2^{29}}{2^{30}} \times 50MHz = 25MHz.
\]

Even at the highest frequency of 1M output, the waveform can be guaranteed to have 48 points per cycle. At this point, the output is 1Hz ~ 1MHz, and the frequency segment can be adjusted in the expansion requirements.

3. System design

3.1. Scheme design

Designed with microcontroller AT89S52 as the core, combined with peripheral modules to complete the reading of keyboard operations, control LCD display, and provide control words for FPGA. As the core of frequency synthesis and amplitude control, FPGA communicates with the MCU through the bus to obtain control words and control the high-speed DA converter to ensure the 1MHz waveform output in the system requirements. The waveform data is sent from FPGA to DA converter THS5651, and then another DA converter controls the amplitude. Then it is filtered by a low-pass filter, and finally the load carrying capacity is enhanced by a transistor push-pull power amplifier circuit. The
high-speed AD converter reads the output signal and sends it to the FPGA. The built-in dual-port RAM in the FPGA stores the waveform signal read by the AD to complete the measurement display function of the output waveform. Thus, a function signal generator with adjustable frequency and amplitude modulation and strong loading capacity is produced. The system block diagram is shown in Figure 2.

![Figure 2 System block diagram](image)

The main functions of this system are all designed and implemented by FPGA, using a single-chip computer as the input and output of human-computer interaction, and use a custom virtual bus system to connect the MCU to the FPGA. The MCU interface circuit is shown in Figure 3.

![Figure 3 MCU interface circuit](image)

Functionally, microcontrollers and large-scale programmable logic devices are highly complementary. The former has high cost performance, flexible functions, and easy human-computer interaction; the latter has the characteristics of high speed, high reliability, convenient development, and specifications. The combined circuit structure of these two types of devices can greatly improve system performance and design flexibility, and better meet design requirements.

In the design, the FPGA device EP16T144C8 of Altera Company was selected to match with the MCU to complete the system functions together. Moreover, a bus interface with the MCU is built in the FPGA as a “channel” for data exchange.
3.2. Peripheral module design
The main function of the digital-to-analog conversion and amplitude adjustment module is to complete the digital-to-analog conversion and amplitude program control adjustment. Utilizing dual DA circuits to achieve amplitude adjustment. The specific circuit is shown in Figure 4.

Digital-to-analog conversion uses a 10-bit high-speed analog-to-digital converter THS5651 with a conversion speed of 1ns and a maximum frequency of 100MHz. The device has a fast settling time that fully meets design needs. The amplitude control adopts a dual DA adjustment method. The first DA converter outputs a waveform signal, and another DA converter is controlled to output the reference voltage of the first DA converter according to the amplitude control word. By adjusting the amplitude control word, 0.1V precise adjustment of the output waveform signal is achieved.

![Figure 4 DA conversion and amplitude adjustment circuit diagram](image)

4. Software design and implementation
The frequency synthesis method based on DDFS uses the MCU to generate the required frequency control word, and then the MCU sends the control word to the FPGA, and the DDFS is realized by the FPGA which can perform high-speed calculation. In order to achieve user-friendly operation, the MCU will continuously scan the PS2 keyboard and calculate the code from the keyboard's return key to generate the required control word information, send the required control words to the FPGA, and send information to the LCD at the same time, so that the LCD displays the information returned by the FPGA in real time, and scans the keyboard to control the content required by the LCD display.

The keyboard input method uses the MCU's function for identifying specific key values. When the frequency input key is pressed, it enters the frequency acquisition state, and then the user uses the keyboard to enter the required frequency value. The MCU calculates the corresponding frequency control word, and then uses this control Word to cover the original frequency control word and send it
to the FPGA to implement the frequency conversion function. The frequency control program flowchart is shown in Figure 5.

Figure 5 Flow chart of frequency control program

5. System test and error analysis

5.1. Signal output test

According to the system requirements, the following test data is obtained:

Table 1. Frequency test

| Preset frequency | Sine wave | Square wave | Sawtooth wave | Triangle wave |
|------------------|-----------|-------------|---------------|--------------|
|                  | Measured frequency | Measured frequency | Measured frequency | Measured frequency |
| 1Hz              | 1.01 Hz    | 1.01Hz      | 1.02 Hz       | 1.02Hz       |
| 2Hz              | 2.05 Hz    | 2.05Hz      | 2.05 Hz       | 2.04Hz       |
| 1KHz             | 1.04KHz    | 1.05KHz     | 1.03KHz       | 1.02KHz      |
| 2KHz             | 2.02KHz    | 2.04KHz     | 2.02KHz       | 2.06KHz      |
| 2.1 KHz          | 2.11KHz    | 2.16KHz     | 2.15KHz       | 2.17KHz      |
| 1MHz             | 1.03MHz    | 1.04MHz     | 1.03MHz       | 1.03MHz      |

Table 2. Output voltage amplitude test (1KHz, 50Ω load resistance, peak-to-peak)

| Preset voltage (peak-to-peak) | Actual voltage (peak-to-peak) | Error |
|-------------------------------|-------------------------------|-------|
| 0                             | 0.02V                         |       |
| 2V                            | 2.03V                         | 1.5%  |
| 2.1V                          | 2.13V                         | 1.42% |
| 4V                            | 4.06V                         | 1.5%  |
| 4.1 V                         | 4.16V                         | 1.46% |
| 5V                            | 5.08V                         | 1.6%  |
### Table 3. Frequency vs. Voltage test (1KΩ load resistance, sine wave)

| Frequency (Hz) | Voltage (peak-to-peak) |
|---------------|------------------------|
| 1Hz           | 5.02V                  |
| 1KHz          | 5.03V                  |
| 100KHz        | 5.13V                  |
| 1MHz          | 5.06V                  |

#### 5.2. Error Analysis

The system circuit is mature in principle and stable in performance. The error mainly comes from three parts, the first is the waveform generation circuit, the second is the post-processing module, and the last is the power circuit.

##### 5.2.1. Waveform generation circuit

The DA chip used is a 10-bit high-precision digital-to-analog converter, and the error is very small, so it can be ignored. However, when outputting a small amplitude signal or 0V, errors such as the offset voltage, offset current, and bias current of the integrated op amp may affect the waveform output, resulting in a slight ripple at the 0V output. But the noise amplitude is small (less than 5mV) and can be ignored.

##### 5.2.2. Post-processing module

The smoothing filter designed to reduce the influence of digital signals, when the output signal amplitude is small, is easily affected by the offset voltage, offset current and bias current of the integrated op amp. In addition, this problem also exists in a dual op amp current-spreading circuit. However, the error caused by this part is small and can be ignored.

##### 5.2.3. Power circuit

The random noise of the power supply will also affect the working state of the chip and bring unnecessary noise to the output. In order to reduce the adverse effects of the power supply circuit on the system, the following measures can be taken: improve the power supply characteristics as much as possible, reduce the ripple, and add decoupling capacitors for the power supply and each chip to reduce the impact.

#### 6. Conclusion

The system uses MCU and FPGA as the core components, and uses DDFS technology to realize the design of the function signal generator, which can generate sine wave, triangle wave, sawtooth wave and square wave signals, and finally complete the predetermined parameters. During the system design process, the hardware circuit functions were simple and reliable, and the convenience and flexibility of software programming were fully utilized to meet the system design requirements.

#### References

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