Proposal of a FET-LET Hybrid 6T SRAM

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Abstract—There is an extremely high demand for a high speed, low power, low leakage, and low noise Static Random-Access Memory (SRAM) for high performance cache memories. The energy efficiency of SRAM is of paramount importance in both high performance and ultralow-power portable, battery operated electronic systems. In this article the factors affecting the overall speed and total energy consumption of a conventional 6T SRAM cell/array with 6 FETs, particularly roles of access transistors are analyzed to highlight the needs and directions for improvement. A hybrid 6T SRAM with two access FETs being replaced by light-effect transistors (LETs) and the electrical word lines replaced by optical waveguides (OWGs) is proposed. This hybrid SRAM is analyzed to reveal its potential in improvement of the switching speed and thus total energy consumption over the conventional 6T SRAM. Numerical analyses of a prototype hybrid SRAM array of 64 KB show a factor of 7 and 34 reduction in read delay and read energy consumption, respectively; and 4 and 6 in write delay and write energy consumption, respectively, when the access FETs are replaced by LETs. The potential impacts on the peripheral and assist circuits due to this hybrid structure and application of the LETs there are also briefly discussed.

Index Terms—SRAM, 6T cell, LET, access devices, switching speed, energy consumption.

I. INTRODUCTION

INTEGRATING electronic and photonic systems on the same chip can potentially transform computing architectures and enable more powerful computers. It is now possible to integrate a large number of electronic devices and photonic components on a single chip to perform logic, memory, and interconnect functions [1]. However, typically, the photonic components play only the roles of providing high-speed communications between different electronic subsystems [2], [3] rather than any active roles in processing or modifying information like logic gates. Although photo-conductive devices can potentially offer advantages in switching speed [4] and switching energy [5], one major drawback of using such devices, like a light effect transistors (LETs) [5], [6] is the inconvenience of using the output of one LET based logic gate to directly drive the next similar logic gate without going through relatively inefficient electrical to optical energy conversion. To explore the advantages of LETs but avoid the cascading issue in computing applications [7], we seek to replace some field effect transistors (FETs) that only serve the roles of switching a circuit on and off, such as, the access transistors in a SRAM cell.

One of the most crucial concerns in many ultralow-power applications is energy efficiency. SRAM being one of the most critical building blocks in almost all digital systems, its packing density, speed, power consumption are all crucial performance metrics[8], [9]. SRAMs are generally used in high speed cache memories providing a direct interface with a CPU at high speeds which are not possible to attain by other memory circuits. However, on chip caches typically consume 25%–45% of the total energy of a chip [10], [11]. Moreover, in modern high-performance large density memory circuits, more than 40% of the total energy is consumed due to leakage currents [12]. Hence, high-speed and energy-efficient embedded memories are desirable for a modern electronic system.

A conventional 6T SRAM cell is shown schematically in Fig. 1, consisting of 6 FETs labeled as M1-M6. (M1&M2) and (M3&M4) form the cross-coupled inverter pairs (latches), and M5 and M6 are the access devices that allow the data stored in the cell to be accessed and modified by charging and discharging the output nodes Q and Q and bit lines BL and BL during the read and write operations. The two access transistors play an extremely crucial role in determining the overall speed, power dissipation and stability of the cell [13-15]. Additionally, the three p-FETs, encircled in red in Fig. 1, are the bit line conditioning devices whose roles are to pre-charge and equalize the bit line voltages before each read and write operation. Their switching speed and energy consumption are also critical
to the performance of the SRAM [15], [16]. Many approaches in both device and circuit level have been explored to improve the SRAM performance in various aspects, particularly in speed and energy consumption [17-19].

Our proposal of a FET-LET hybrid 6T SRAM technology represents a drastically different approach that can offer major improvement on the read and write speeds and the corresponding energy consumptions by replacing the two access FETs with two LETs and accordingly the word line electrical wires with optical waveguides (OWGs). This idea offers a more intimate integration of the electronics and photonics, namely on the CPU chip level. Additionally, this application avoids the well-known energy-data rate (EDR) challenge (EDR ≤ 10fJ/bit for on-chip communication) [2], [20], because it does not require using light to address photonic devices individually [7], but in a group simultaneously through an optical waveguide. The focus of this work is on the potential improvement of the 6T SRAM array itself, but the anticipated benefits of applying LETs in the peripheral circuits will also be discussed briefly.

II. Analysis of Delay and Energy Consumptions in A 6T SRAM Array

The primary factors limiting the read and write speeds and the corresponding energy consumptions of a 6T SRAM array are the capacitances of the bit lines and word lines, and the characteristics of the access transistors (rather than the transistors of the inverters).

A. Capacitance Calculations

The critical capacitances of a 6T SRAM cell/array are calculated as follows [15], [21]:

\[ C_{BL} = n_R (C_{\text{drain,access}} + C_{ht}) \]  

\[ C_{WL} = n_C (2C_{\text{gate,access}} + C_{\text{width}}) \]  

\[ C_{out} = C_Q = C_{\text{drain,M1}} + C_{\text{drain,M2}} + C_{\text{gate,M3}} + \] 
\[ C_{\text{gate,M4}} + C_{\text{drain,M5}} \]  

where \( C_{BL} \) is the bit line capacitance, \( C_{WL} \) is the word line capacitance, \( C_{out} \) (or \( C_Q \) for the node \( Q \) in Fig. 1) is the capacitance of the output node, \( C_{\text{drain,access}} \) and \( C_{\text{gate,access}} \) are the drain and gate capacitances respectively of the access devices, \( n_R \) and \( n_C \) are the number of rows and columns respectively for the 6T array and \( n_R = n_C = 1 \) for a 1-bit 6T cell. The bit line wire capacitance (\( C_{\text{bl}} \)) and the word line wire capacitance (\( C_{\text{width}} \)) are calculated using relations from [15].

All the drain and gate capacitances of the access FETs (M5,M6) and the core FETs (M1-M4) are calculated using relations from [13], [22], [23] and considering FET model parameters from [24].

B. Read and Write Delay Calculations

Note that in all subsequent calculations, only a 6T array has been considered with certain assumptions for the cell read, cell write, word line, word line driver and write assist circuitry current, which will be discussed later in Section III-C. The effects of all peripheral and assist circuits are not considered.

The read and write delays are calculated as follows [15]:

\[ T_{\text{read}} = \frac{C_{WL}V_{DD}}{I_{\text{word,drive}}} + \frac{C_{BL}V_{read}}{I_{\text{read}}} \]  

\[ T_{\text{write}} = \max \left( \frac{C_{WL}V_{WL}}{I_{\text{write,ckt}}} + \frac{C_{BL}V_{DD}}{I_{\text{write}}} + \frac{C_{out}V_{out}}{I_{\text{write}}} \right) \]  

where \( I_{\text{read}} \) and \( I_{\text{write}} \) are the 6T cell read and write currents respectively; \( I_{\text{word,drive}}, I_{\text{WL}}, \) and \( I_{\text{write,ckt}} \) are the word line driver, word line, and write circuitry currents respectively [15]; \( AV_{\text{read}}, \) \( AV_{\text{write}}, \) \( AV_{\text{out}} \) are respectively the change in the bit line voltage after read operation and the change of output voltage after write, and \( V_{DD} \) is the supply voltage.

C. Read and Write Energy Calculations

Read and write energies are calculated as follows [15]:

\[ E_{\text{read}} = C_{WL}V_{DD}^2 + C_{BL}V_{DD}AV_{\text{read}} \]  

\[ E_{\text{write}} = C_{WL}V_{WL}V_{DD} + C_{BL}V_{DD}^2 + C_{out}V_{DD}AV_{out} \]  

where \( V_{WL} = V_{DD} \) is the word line voltage. Note that for the above delay and energy equations, the delay and switching energy due to the transit of carriers through the FET channel has not been considered, since they are negligible compared to the gate related RC delays and energies.

As evident from the above formulas, the access transistors and the ways to address them play critical roles in determining the overall SRAM cell performance, and hence if the access devices can be replaced with some high-speed switching devices with very low gate, source and drain junction capacitances, and also can be addressed more efficiently, appreciable improvement in speed and power consumption can be achieved. Therefore, it will be advantageous to replace the FET access devices with a different device structure such as LETs, as described in the next section that does not have a physical gate, and hence has appreciably lesser capacitances as compared to the conventional gated FETs.

D. Energy Consumption Associated with Leakage Currents

There are various types of leakage currents in a modern FET that contribute to the energy loss. For instance, for a standard n-FET fabricated on a p-type substrate, these include multiple gate related leakages: gate-induced drain and source leakage current, gate tunneling leakage current through the bulk, source, and drain; sub-threshold leakage current; punch-through leakage current; and p-n junction leakage currents at the drain-substrate and source-substrate junctions [25], [26]. The leakage in a 6T cell depends on the logic state of the cell, the logic level of the word line, and the type of operation performed [27]. The total leakage current of an individual FET in the 6T cell may be modeled as [25], [27]:

\[ I_{\text{leakage, total}} = I_{\text{sub}} + I_{\text{gate}} + I_{\text{junction}} \]
where, $I_{sub}$ is the subthreshold leakage current, $I_{gate}$ is the total gate leakage current and $I_{junction}$ is the total junction leakage current. Although in the static state, the leakage currents of the two inverters dominate the static energy consumption, during the write and read processes, the leakage of access transistors M5 and M6 also contributes to the total energy consumption. From [27] it can be roughly estimated that about 40% of the total leakage is in the access paths of the 6T cell. If these leakages are severe, it may lead to a false read or write operation and affect the reliability of the 6T cell [25].

### III. Light Effect Transistor (LET)

#### A. Device Overview and Advantages over FETs

A LET as shown in Fig. 2 is a semiconductor nanowire (SNW) placed on an insulating substrate with two metal contacts at the ends [5]. Working mechanism of a LET is different from that of a traditional FET in that the source-drain conductivity of a LET is modulated by light or EM radiation of a suitable wavelength as in photoconductive mechanism [5], [28]. The advantage of an LET over a FET stems from various factors like removal of physical gate, thus minimizing the complex gate fabrication process and random dopant fluctuations in FETs [29]. Hence, the LET can be scaled down to quantum regime without the problem of short-channel effects (SCEs) that are common in nanoscale FETs [30]. Also, because the LET structure does not have a physical gate, the device speed is expected to be only limited by the carrier transit time or lifetime, whichever is smaller, rather than the capacitive delay as in the FET. Although the demonstrated prototype LET was based on a CdSe NW [5], there is no limit to the material system per the device mechanism. At room temperature, many semiconductors (e.g., Si, SiC, InAs, InP, GaAs, CdSe) have saturation electron velocities in the range of $(1-10) \times 10^7$ cm/s when the electrical field is on the order of 100 kV/cm [31], [32], which implies a carrier transit time of the order of $(1-0.1)$ ps for a 100 nm long NW. 100 nm is also the typical length scale of ballistic transport where the saturation velocity can be achieved. For longer NWs in the non-ballistic transport regime, the electron transit time depends on the electrical field. For Si at $E = 10$ kV/cm, the electron velocity is around $7 \times 10^6$ cm/s [31], [32], and the carrier transit time ($t_{LET}$) can be estimated to be 4.3 ps and 7.1 ps, respectively, for a 300 nm and 500 nm long Si NW. If the NW in the LET can be scaled down to operate in the ballistic regime (typically ≤ 100 nm), then ultra-fast switching (of the order of 1 ps or faster) can be obtained. The ultra-fast switching of the LET translates to ultra-small switching energy. For instance, assuming a switching time (carrier transit time) $t_{LET} = 1$ ps for a ballistic device, an on-current of $I_{on} = 1 \mu A$ under $V_{dd} = 1$ V, the electrical switching energy $E_{el} (= I_{on} \times V_{dd} \times t_{LET})$ will be of the order of 1 aJ/switch. However, in the LET, optical gating power also contributes to the switching energy. The net gating power required can be estimated by $P_g = E_{ph}I_{on}/(eG)$, where $E_{ph}$ is the photon energy and $G$ is the photoconductive gain. Assuming $E_{ph} = 2.5$ eV, $G = 10^3$, to have $I_{on} = 1 \mu A$, we get $P_g = 2.5$ nW. Then, assuming $t_{LET} = 1$ ps, the optical switching energy $E_{op}$ will be $2.5 \times 10^{-3}$ aJ/switch $<< E_{el}$, which leaves sufficient room allowing for below 100% light power delivery efficiency. In an even more idealistic case, assuming a ballistic device with a quantum impedance of 12.9 kΩ [33], transit time of 0.1 ps, S-D current of 1 µA, and no voltage loss at the contacts, the electrical switching energy can be as low as $1.3 \times 10^{-21}$ J/switch at a very low $V_{dd}$ of only 13 mV [5]. For a prototype device, a 5 µm long and 80 nm in diameter CdSe NW LET structure studied previously [5], under 532 nm illumination of 110 nW (only about 6% was actually absorbed), yielded $I_{ds} = 0.35$ µA at $V_{ds} = 1.43$ V; in dark, $I_{ds} \sim 1$ pA, which corresponds to 1.5 pW static or off power. Estimating the switching energy for such a large device using the typical room temperature carrier lifetime in a II-VI semiconductor in the order of 100 ps, the total switching energy $E_{tot,sw} = E_{el} + E_{op} \approx 0.06$ fJ/switch would still be better than typical FETs having switching energy of 0.1-1 fJ/switch [34]. In FETs, the gate related RC delays predominate over the transit-time delay; but in the LET, the carrier transit time through the NW channel is expected to be the predominant factor for determining the switching speed and energy of a discrete LET. Moreover, the $I_{on}/I_{off}$ ratio for a LET could be as high as $10^6$ [5], which is almost an order of magnitude better than that of advanced FETs. This reduces the leakage in the access paths and offers more flexibility in the 6T cell design with LET access devices.

#### B. Hybrid 6T SRAM with Access FETs Replaced by LETs

To take advantage of the high switching speed and low energy consumption of LETs, the two access transistors (M5 and M6) in the 6T cell of Fig. 1 are replaced by two LETs (L1 and L2) as shown in the prototype hybrid 6T cell of Fig. 3, where the word line is replaced by an optical waveguide (OWG) that transmits light to the LETs.

To quantify the potential improvement, we consider a design with a moderate size LET based on a generic semiconductor NW: $L = 300$ nm (length) and $D = 50$ nm (diameter) and supported on an insulating substrate (e.g., SiO$_2$/Si) as shown in Fig. 2. Also, a ballistic device with smaller dimensions ($L = 100$ nm and $D = 30$ nm) is considered which yields a much reduced 6T cell and array area and high cell density.
For the LET structure, there will be no MS-junction capacitance that is equivalent to the drain or source capacitance (gate-drain or gate-source overlap capacitance along with the drain-substrate or source-substrate junction capacitance) of FETs, since there is neither a gate nor any electrical paths to ground between the MS structure and the substrate that has no electrical connection as opposed to the doped substrates of FETs. The photocurrents of the NW photodetector are typically in the range of 1-10 µA [35-37]. For the LET access device, the photocurrent is assumed to be 5 µA. The switching delay, as estimated by the transit time earlier, is assumed to be 4 ps and 0.1 ps for the non-ballistic and ballistic cases, respectively.

C. Critical Capacitance, Read, Write Delay and Energy Consumption of the 6T SRAM with LET Access Devices

The critical capacitances of the hybrid 6T SRAM with LET access devices are modified from the $C_{BL}$ and $C_{out}$ calculated in (1) and (3) as follows:

$$C'_{BL} = n_E(C_{BL}) \quad (1')$$

$$C_{out} = C_Q = C_{\text{drain},M1} + C_{\text{drain},M2} + C_{\text{gate},M3} + C_{\text{gate},M4} \quad (3')$$

In (1’), the modified bit line capacitance is predominantly the wire capacitance only, since the LET access devices do not have any MS junction capacitance. In (3’), there is only the drain and gate capacitances of the core FETs. The drain equivalent capacitance of the access FET ($C_{\text{drain},M5}$ in (3)) is not present in case of LET access devices due to the same reason. In the LET accessed SRAM, the word-line capacitance ($C_{WL}$) in (2) should be practically zero, since the access LETs neither have any gate capacitance, nor require a wired electrical signal to control the gates as in the case of access FETs. Accordingly, the read and write delay and the corresponding energies in (4)–(7), are modified as below, with $I_{\text{read}}$ and $I_{\text{write}}$ being replaced by $I'_{\text{read}}$ and $I'_{\text{write}}$ appropriate for the LET access devices, and all the $C_{BL}$ and $C_{out}$ are replaced by $C'_{BL}$ and $C'_{out}$, keeping other parameters almost unchanged.

$$T_{\text{read,LET access}} = t_{WG} + max \left( \frac{C_{BL}V_{\text{read}}}{I'_{\text{read}}}, t_{LET} \right) \quad (4')$$

where the RC-word-line delay during read operation in (4) is replaced by the time taken by the EM signal to propagate through the optical wave-guide ($t_{WG}$), and the second term is the larger term of the modified RC-bit line delay during read and the LET carrier transit delay.

$$T_{\text{write,LET access}} = \max \left( \frac{C_{BL}V_{\text{read}}}{I'_{\text{write}}}, t'_{\text{LET}} \right) \quad (5')$$

where the first term in (5’) is the larger term of $t_{WG}$ and the modified bit line delay during write, and the second term is the larger term of the modified 6T cell flipping delay during write and the LET carrier transit delay.

$$E_{\text{read,LET access}} = (2n_E E_{\text{op}}) + max(C_{BL}V_{DD}ΔV_{\text{read}}, E_{\text{el}}) \quad (6')$$

$$E_{\text{write,LET access}} = (2n_E E_{\text{op}}) + C_{BL}V_{DD}^2 + max(C_{out}V_{DD}ΔV_{\text{out}}, E_{\text{el}}) \quad (7')$$

where the word line energies in (6’) & (7’) (the first terms) will not be present in case of LET accessed cells or arrays, assuming the light propagation loss through OWG is practically negligible. The first terms in both (6’) and (7’) are the optical gating switching energy ($E_{\text{op}}$), and for a whole row it is multiplied by $2n_E$ where $n_E$ is number of 6T cell in a row and each 6T cell has 2 LET access devices. The second term in (6’) is the larger of the modified bit line RC-read energy, and the LET carrier transit electrical switching energy ($E_{\text{el}}$) as described in Section III-A, while the last term in (7’) is the larger term of the modified cell flipping RC-energy during write, and the LET carrier transit electrical switching energy.

Therefore, it can be inferred that a SRAM array with LETs in the access paths will reduce all the critical capacitances (except for the bit line wires) as compared to the array with FET access devices. Also, the carrier transit delay and switching energy (depending on the transit delay) of a LET are much lesser as compared to the RC delay and switching energy of a FET. Using relations (4)-(7) and (4’)-(7’), a set of delays and energy consumptions are calculated for various 6T- SRAM arrays (32 bytes - 64 KB) with respectively, FET, LET and ballistic LET access devices for direct comparison. The values of the currents in the 6T FET SRAM are assumed to be 25 µA [15, 38], considering the effective drive currents of 22 nm FETs [39] and $ΔV_{\text{read}} ≈ 120$ mV and $ΔV_{\text{out}} ≈ V_{DD}/2$ [15]. The results for differ-
ent SRAM array sizes are shown in Figs. 4(a)-(d), and the numerical results are given in Table I for 4-KB and 16-KB arrays. The calculated read and write delays and energies for FET accessed 6T SRAMs agree with previously reported results (of the same orders in magnitude) [38]. It is clear from the results, as summarized in Table I, that using LET access devices may result in marked improvement in the overall delay and energy consumption of the SRAM array. From the delay and energy plots of Fig. 4, it is found that the results for LET and ballistic LET are coinciding despite the ballistic device having much lesser carrier transit delay and switching energy as compared to non-ballistic LETs. This is because for an array, the overall RC delay and energy will dominate (as in (4’)-(7’)) over the carrier transit delay and switching energy of the individual LETs. On read delay, Fig. 4(a) reveals approximately a factor of 6 average reduction with LET access devices over FET access devices. Accordingly, on read energy, Fig. 4(b) reflects approximately a factor of 28 average reduction. On write delay, the average reductions shown in Fig. 4(c) is approximately a factor of 3, and on write energy, Fig. 4(d) shows approximately a factor of 5 average reduction. The results for both the read and write energy can indeed satisfy the requirement of EDR ≤10 fJ/bit for on-chip photonic integration [2], [3], as shown in Table I. The general operating principle, mechanism, and conclusion are in-principle applicable for LETs appropriately fabricated with any semiconductor.

| TABLE I | COMPARISON OF THE PERFORMANCE OF 4-KB AND 16-KB SRAM ARRAYS WITH FET, LET, AND BALLISTIC LET ACCESS DEVICES |
|----------|---------------------------------------------------------------------------------------------------|
| 4-KB SRAM Array | 16-KB SRAM Array |
| FET Access Devices | LET Access Devices | Ballistic LET Access Devices | FET Access Devices | LET Access Devices | Ballistic LET Access Devices |
| Read Delay (ps) | 634.8 | 90.1 | 90 | 1270 | 180.3 | 180 |
| Write Delay (ps) | 598.5 | 149.1 | 149.1 | 1190 | 291.3 | 291.3 |
| Read Energy (fJ) | 15.1 | 0.44 | 0.43 | 30.1 | 0.88 | 0.85 |
| Write Energy (fJ) | 21.8 | 3.43 | 3.41 | 43.5 | 6.81 | 6.79 |

D. Discussion on the Delay and Energy Consumption of the 6T Array with FET and LET Access Devices

6T Array without Peripherals
The improvement in the read delay of the hybrid 6T SRAM array is primarily due to the removal of the word line delay in (4) by the optical-waveguide delay ($t_{WG}$) in (4’) which is almost negligible as compared to the RC word line delay with FET access devices. The improvement in the write delay is due to the removal of the $C_{WL}$ related term and reduced overall bit line capacitance from $C_{BL}$ to $C_{BL}$. Relatively, the improvement in the write delay is lesser than the read delay, because the first term in the write delay in (5) takes the larger one of the two contributions, and hence the advantage of replacing the word line delay in (5’) by $t_{WG}$ does not affect the overall write delay as much
as it affects the read delay. Also, the highest reduction achieved in the read energy is mainly due to the replacement of the RC word line energy consumption in (6) (the first term) with FET access devices by a much smaller optical gating term in (6') (the first term) with LET access devices. Similarly, the improvement in the write energy in (7') is lesser than read energy in (6'), due to the presence of the second and third terms in (7') where $V_{DD} > AV_{out} > AV_{read}$, and thus $C_{BL}V_{DD}^2$, the second term in (7') $> max(C_{BL}V_{DD}AV_{read}, E_{el})$ the second term in (6'), which to some extent lessens the amount of improvement in the write energy as compared to read energy.

Note that in above analyses, the hybrid 6T SRAM array offers improved performance even with a smaller on-current (by a factor of 5) than the conventional 6T SRAM array. Since much lesser current is needed in the 6T cell with LET access devices, the core FETs (the FETs in the inverter pairs) can be scaled down to lesser device widths (FET drive current is proportional to the device width), which may offer saving in area for the 6T cell and hence for the whole array. However, we would like to point out that if the on-current of the hybrid 6T SRAM is increased to the same level as the conventional 6T SRAM, the read delay can be further reduced by approximately a factor of 5, but the improvement on write delay may be less significant, because for a large array it primarily depends on $I_{wriite, ckt}$. The figure of merit (FOM) of the SRAM array can be found from the energy-delay product (EDP) [15]. Considering 50% probability of the array being accessed in a cycle, and 50% probability for each of the read and write operations [15], it can be roughly estimated that the hybrid SRAM array (average EDP of the order of $10^{-25}$ Js) on an average exhibit almost two and three orders of magnitude lesser word line delay and energy consumption respectively over the all FET array with word line drivers [15]. A prototype 6T array with LET access devices and OWG, keeping the core FETs and other peripherals almost unchanged is shown in Fig. 5 below.

The electrical row decoder circuit in a conventional SRAM array has to be replaced by an opto-electronic counterpart to illuminate the OWGs by appropriate optical sources, for example, nanoscale lasers [20]. Secondly, besides using LETs as the access devices, there may be a scope to replace some FET based switches in other peripherals and assisting circuitry of the 6T array by LETs, which will further reduce the relevant delay and energy consumption, and hence further improve the performance of the SRAM array. For instance, there may be a possibility to replace the three p-FETs of the bit line conditioning circuitry of Fig. 3 by LETs, which will further reduce the bit line capacitances and hence bit line related delays and energy consumptions, especially for large 6T arrays.

### E. Improvement on Leakage Using LET Access Devices

For the LET structure, all the leakage mechanisms (currents) for the FET mentioned in Section II-D are eliminated except for the subthreshold current that is equivalent to the dark current of the LET. Since generally doping is not required for the LET, it can have very low dark current (e.g., of order of few pA) [5].

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**Fig. 5. Prototype of a LET accessed hybrid 6T SRAM Array**
LETs have a different turn on mechanism and no SCEs as discussed previously [5] and hence hybrid SRAMS will have minimal subthreshold leakage in the access paths. Since LETs do not have a physical gate, there will be neither any gate related nor any SCE induced leakage [25-27 in the access paths, and thus the leakage power consumption in the hybrid SRAM will be much reduced. Also, LETs do not have any p-n junctions or leakage paths to ground, and hence the hybrid SRAM will also have no junction leakage [25] in the access paths and hence the overall leakage will be much reduced. It can be estimated from [27], that there will be an overall reduction of roughly 35% in the total leakage current in a single hybrid 6T cell, which will be more advantageous in the case of a hybrid 6T array having a large number of such 6T cells.

IV. CONCLUSION

LETs offer high speed and low energy opto-electronic switching, where the switching delay is limited by carrier transit time, which can be made extremely small by using the nanowire based device, particularly in the ballistic transport mode. In contrast, in the FETs, it is generally RC switching, and hence it is much less energy efficient due to high gate-related capacitances in FETs. The biggest advantage of replacing the FET access devices by LETs is that the gate, source and drain related capacitance and electrical word line are no longer present, which removes the word line delay as well as energy consumption. From the above delay and energy calculations of the hybrid 6T SRAM using LET access transistors, it can be concluded that this new hybrid 6T cell and array is much more energy efficient with lesser read and write delays as compared to the all FET 6T cells and arrays. In addition, LETs are expected to have much lower leakage currents than conventional FETs, and thus the hybrid 6T cell and array will have much lesser leakage power dissipation compared to those with FET access devices. The use of the optical waveguide-based word line architecture in the hybrid SRAM array abolishes the need of electrical word lines and also the word line drivers, which drastically reduces the total word line capacitance, RC-delay and energy consumption to almost negligible compared to that in the conventional SRAM array. Furthermore, LETs may find useful applications in other peripheral and assist circuits of the SRAM array like the bit line conditioning circuit for improvement in speed and energy consumption. The proposed hybrid SRAM architecture offers an example of hybrid electronic-photonic integrated circuit with both electronic and photonic devices playing active roles synergistically.

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