Harmonic-summing Module of SKA on FPGA – Optimising the Irregular Memory Accesses

Haomiao Wang, Prabu Thiagaraj, and Oliver Sinnen

Abstract—The Square Kilometre Array (SKA), which will be the world’s largest radio telescope, will enhance and boost a large number of science projects, including the search for pulsars. The frequency domain acceleration search is an efficient approach to search for binary pulsars. A significant part of it is the harmonic-summing module, which is the research subject of this paper. Most of the operations in the harmonic-summing module are relatively cheap operations for FPGAs. The main challenge is the large number of point accesses to off-chip memory which are not consecutive but irregular. Although harmonic-summing alone might not be targeted for FPGA acceleration, it is a part of the pulsar search pipeline that contains many other compute-intensive modules, which are efficiently executed on FPGA. Hence having the harmonic-summing also on the FPGA will avoid off-board communication, which could destroy other acceleration benefits. Two types of harmonic-summing approaches are investigated in this paper: 1) storing intermediate data in off-chip memory and 2) processing the input signals directly without storing. For the second type, two approaches of caching data are proposed and evaluated: 1) preloading points that are frequently touched 2) preloading all necessary points that are used to generate a chunk of output points. OpenCL is adopted to implement the proposed approaches. In an extensive experimental evaluation, the same OpenCL kernel codes are evaluated on FPGA boards and GPU cards. Regarding the proposed preloading methods, preloading all necessary points method while reordering the input signals is faster than all the other methods. While in raw performance a single FPGA board cannot compete with a GPU, in terms of energy dissipation, GPU costs up to 2.6x more energy than that of FPGAs in executing the same NDRange kernels.

Index Terms—Irregular memory access optimisation, harmonic-summing, field-programmable gate arrays (FPGA), OpenCL.

I. INTRODUCTION

The Square Kilometre Array (SKA) is built to extend our understanding of the Universe and ourselves and it will be the world’s largest radio telescope array when finished [6]. A number of key science goals are targeted by the SKA project and one of them is strong-field tests of gravity using pulsars, which are highly magnetized rotating neutron stars. Since most pulsar signals are weaker than white noise and their details are unknown, a number of techniques are employed to search for different types of pulsars over a wide range of searching scales (e.g. sky coverage, frequency, bandwidth, and integration time) [21]. The enormous signal rate of the SKA makes an efficient solution only using general processors to complete the searching tasks in the given time period extremely difficult.

Taking the high-performance computing ability, power consumption, and flexibility into consideration, the field-programmable gate array (FPGA) seems to be an ideal device to accelerate the Central Signal Processor (CSP) of the SKA project. The SKA stage 1 (SKA1) project plans to adopt high-end FPGAs to accelerate part of the function modules in the CSP regarding pulsar search such as frequency domain acceleration search. However, the general hardware description language (HDL, e.g. Verilog HDL and VHDL) based development process makes it hard to achieve fast prototyping design and design space exploration. Additionally, developers of an internationally distributed team, including non-hardware experts, would need to understand the hardware structure of FPGA devices.

To address these problems, we employed a high-level approach by using a high-level language compared to HDL. In this paper, we take a pulsar search module called harmonic-summing as a case study. The harmonic-summing module is a part of the Fourier domain acceleration search (FDAS) module that contains a compute-intensive module. The compute-intensive module performs very well on FPGAs [20], so in order to avoid unnecessary data transfer, it is important to have the harmonic-summing module on the FPGA. The main feature of the harmonic-summing module is that the access to the input signals is irregular and this affects the hardware accelerator in achieving high-performance computing. We investigate a number of methods and architectures to optimise the irregular memory accesses of the harmonic-summing module and using Open Computing Language (OpenCL) for the prototype design. The main contributions are as follows:

1) Reducing Intermediate Data Accesses: The straightforward and proposed approaches for the harmonic-summing module are investigated and designed. The proposed approach reduces the total number of off-chip memory accesses by changing the processing order and storing the intermediate data in on-chip memory.

2) Preloading Data: Based on the proposed approach, two preloading data methods are investigated by: 1) loading points with high touch frequency and 2) loading necessary points that are needed to calculate a block of points. Both these methods preload data to on-chip memory before processing and further reduce the total amount of off-chip memory accesses.

3) Reordering Input: Based on the preloading necessary points method, we investigate reordering the input points to improve the memory access speed. After reordering the input, the data needed for each work group are from consecutive addresses and they can be streamed to the FPGA from off-chip memory.

4) Across Device Evaluation: The proposed methods are
implemented on FPGA using OpenCL. We adjust and port the implementations to different devices and evaluate on different series of FPGAs, general-purpose graphics processing units (GPGPUs) and CPUs for comparison.

The rest of the paper is organized as follows. Section II gives related work on optimising irregular memory accesses and high-level tools for developing for FPGAs. Section III provides the details of the harmonic-summing module and the design goals. In Section IV two approaches of OpenCL-based designs of the harmonic-summing module are proposed and compared. Section V presents the evaluation and results are discussed. Finally, the conclusions are given in Section VI.

II. RELATED WORK

A. Irregular Memory Access Optimisation

In hardware-based high-performance computing, the efficiency of data transfer between the accelerator and the memory system is an important factor. A large amount of research has been done to improve the memory access efficiency for accelerators such as GPGPUs [13] and FPGAs.

For some applications, the accesses to memory are irregular that limits the performance of the accelerator, and this problem has been well-studied [11]. For most applications with irregular memory access, there are mainly two types of optimisation techniques: 1) reducing the number of accesses and 2) scheduling as many accesses in parallel [28]. These two methods can be applied to various platforms such as FPGAs [29]. For some graph computation problems in [27], an on-chip distributed off-chip shard memory architecture with high-performance shuffle network was investigated and the intermediate buffers were reduced to save off-chip memory bandwidth. In [30], prefetching is researched to reduce the number of memory accesses. In [14], an irregular stream buffer (ISB) that targets the irregular sequences of temporally correlated memory references is proposed. Data and computation reordering is employed in [17] to improve memory hierarchy performance. Besides these approaches, many compilers focus on irregular memory access such as ROCCC [10] for FPGAs and Sparse matrix-vector multiplication (SMVM) [8].

Regarding the optimisation of two-dimensional harmonic summing calculations done in this research, we are not aware of any prior work which investigating it on a large-scale, especially in the context of acceleration devices such as GPUs and FPGAs.

B. FPGA as an Accelerator

High-end FPGAs have been widely adopted as accelerators in many commercial applications and research areas such as high-frequency trading [15] and cloud computing [7]. Because of the outstanding energy-efficient performance over GPGPU devices, Microsoft applied high-end FPGAs in their data centers [20], and FPGA-based accelerators appear in other cloud data centers as well [24]. Several science projects of different areas such as SKA [25], CERN [23], and DNA sequence analysis [12] exist that employ a large number of FPGA devices for acceleration, connected through the PCI Express (PCIe) bus or Ethernet cable.

Besides these, FPGAs are widely employed in radio astronomy projects as accelerators. In [5], hundreds of Xilinx Virtex-4 FPGAs are used to implement the correlator of the SKAMP project. In [22], FPGA platforms are employed to accelerate digital channelised receivers. The Berkeley CASPER group, MeerKAT, and NRAO released an FPGA-based acceleration device for implementing the FX correlator for radio telescope array [18].

C. High-level Synthesis

One barrier of employing FPGAs as accelerators are the usual use of the HDL-based development process that makes the time-to-market longer than GPGPUs and multi-core processors. To address this, many high-level synthesis tools have been released. Two primary FPGA vendors, Intel and Xilinx, provide developers with their high-level tools. Intel released several high-level development tools such as high-level synthesis (HLS) compiler, which supports C++ based development, and FPGA SDK for FPGA, which supports OpenCL [3], [4] based development. Xilinx provides two main tools: 1) high-level synthesis of C/C++ and SystemC and 2) SDAccel that supports OpenCL. Besides these official tools, there are several open source high-level synthesis tools such as LegUp [11].

OpenCL for Intel FPGA: OpenCL is an open parallel programming language. The main advantage of OpenCL is that it is compatible with different types of acceleration devices such as GPGPUs, CPUs, and FPGAs. Intel released a dedicated FPGA development tool using OpenCL, which is called Intel FPGA SDK for OpenCL (AOCL). An FPGA-based OpenCL application is divided into two parts: the host programs and the kernels for devices. The host program is written in C/C++. Before launching an OpenCL kernel in the host program, the arguments of it are set, and all necessary data are sent to the off-chip memory of FPGA devices through PCIe bus. OpenCL classifies memory into two types local memory and global memory, with the understanding that access to local memory is faster than global, but sharing is limited. For OpenCL on an FPGA local memory corresponds to on-chip memory such as BRAM and global memory corresponds to off-chip memory such as DDR3 on the FPGA board. In this research, the Intel FPGAs are adopted to implement the harmonic-summing module, so the optimisation syntax and techniques that are mentioned in this paper are targeting Intel FPGAs and AOCL.

Single Work-item and NDRange Kernels: NDRange is an important attribute of an OpenCL kernel that represents its index space. Based on OpenCL 1.0 [9], it contains three integer values, where each value specifies the extent of the index space in a dimension. The FPGA-based OpenCL kernels can be classified into two types based on their NDRange sizes: single work-item kernel and NDRange kernel. For the single work-item kernel, its NDRange size is (1,1,1), which means the index space for all three dimensions are one, resulting in a single work-group with one work-item. The kernel code of a single work-item kernel looks more like C/C++ code than that of NDRange kernels. However, some OpenCL-based
optimisation attributes are included within the kernel code. Generally, there is at least one loop in a single work-item kernel and the number of iterations equals to the global work size of the NDRange kernel. The ideal case of the single work-item kernel is to launch one iteration of the outermost loop per clock cycle, which is called loop pipelining. Regarding NDRange kernels, its NDRange size is larger than (1,1,1) and the overall work size has to be divided into small groups. In each small work group, a small group of data is processed. The size of an NDRange kernel is normally related to the details of a task. For example, if a two-dimension NDRange kernel is designed to process an image with 256 points (16×16), its global work size can be set as (16,16,1). In our research, both two kernel types are studied and the combination of single work-item and NDRange kernels are investigated.

III. HARMONIC-SUMMING MODULE

The harmonic-summing module is a part of the frequency domain acceleration search (FDAS) module [21] of the pulsar search engine (PSS), whose details are depicted in Figure 1. In the FT-based convolution module, the overlap-save algorithm [19] is employed to process the input signals in the frequency domain and the outputs are divided into chunks, several thousands values long. The final output from the FT-based convolution module, which is also the input of the harmonic-summing module, is called filter-output-plane (FOP). The size of the FOP equals to \( N_{temp} \times N_{chan} \), with \( N_{temp} \) being the number of templates in the FT-based convolution and \( N_{chan} \) being the number of channels \( N_{chan} \). In essence, each template is an FIR filter, and the FIR filter lengths of different templates are different. The total \( N_{temp} \) templates can be divided into three groups, group one (index 1 to \((N_{temp} - 1)/2\)), group two (index -1 to \(-(N_{temp} - 1)/2\)) and the (unfiltered) input signals (index 0, one-tap FIR filter). The number of channels is the same as the length of input array of the FT convolution module. In our previous work [26], the FT convolution module has been implemented in an FPGA using OpenCL. Based on current requirements, an FOP contains \( 85 \times 2^{21} \) single precision floating-point (SPF) points, that is \( N_{temp} = 85 \) and \( N_{chan} = 2^{21} \).

The harmonic-summing module (In Figure 1 (right)) consists of two parts: 1) harmonic plane calculation and 2) candidate detection. The task of the harmonic plane calculation part is to generate \( N_{hp} \) harmonic planes using the FOP. First, the FOP is stretched by an integer \( k \) to obtain the \( k \)th stretch plane \( SP_k \), which is computed separately for template group one and template group two by generating \( N_{hp} \) stretch planes with Equation 1

\[
SP_k(i, j) = SP_1(\left\lfloor \frac{i}{k} \right\rfloor, \left\lfloor \frac{j}{k} \right\rfloor), \quad k = 2, 3, ..., N_{hp}
\]  

(1)

where \( SP_1 \) is the FOP and the ranges of \( i \) and \( j \) are \([-1 \times N_{temp} - 1)/2, (N_{temp} - 1)/2\] and \([0, N_{chan} - 1]\), respectively. After all \( N_{hp} - 1 \) stretch planes are generated, the FOP and these \( N_{hp} - 1 \) stretch planes are progressively added to form \( N_{hp} - 1 \) harmonic planes (HPs):

\[
HP_k(i, j) = HP_{k-1}(i, j) + SP_k(i, j), \quad k = 2, 3, ..., N_{hp}.
\]

(2)

It can be seen that the size of each \( HP_k \) is the same as that of the FOP.

For the candidate detection, a threshold-detection logic is applied and the potential candidates are recorded. For each harmonic plane, a threshold array \( (TA) \) that contains \( N_{temp} \) thresholds is employed and one threshold corresponds to one row \( (N_{chan} \) points) of the harmonic plane. For example, \( TA(k_i) \) is the threshold for the \( i \)th row of \( HP_k \). In each harmonic plane, most \( N_{cand} \) candidates are stored and the maximum size of the candidate list for each de-dispersion measure (DM) trail is \( N_{hp} \times N_{cand} \). The output from the candidate detection part is the candidate list and it will be sent to the Fourier Domain Candidates optimisation (FDAO) module for further processing (which is part of the post-processing in Figure 1).

Each candidate in the candidate list contains four elements: periodicity, orbits, pulse-width, and signal power of each detection. We use \( \{F_i, H_i, B_i, A_i\} \) to represent the \( i \)th candidate in the candidate list, where \( F_i, H_i, B_i \), and \( A_i \) are the index of filter, harmonic plane, and bin and the amplitude of the \( i \)th element, respectively. To minimize the data transfer bandwidth and save off-chip memory, we use two 32-bit numbers, \( CL_{i1} \) and \( CL_{i2} \), to store the \( i \)th candidate. For \( F_i, H_i \), and \( B_i \), the minimum number of bits required is \([\log_2(*)]\), so the data sizes for them are 7-bit (85), 3-bit (8) and 21-bit (221), respectively. These three factors can be combined together to form one 32-bit integral \( CL_{i1} \) by using the formula as follows:

\[
CL_{i1} = F_i \times 2^{24} + H_i \times 2^{21} + B_i.
\]

In terms of the amplitude (spectral power), since the default data type from the FT-based convolution module is SPF (Single Precision Floating point, 32-bit), the same data type is maintained after the harmonic-summing calculation, which means \( CL_{i2} = A_i \).

The details of the harmonic summing algorithm are given in Algorithm [21] where the order of the three for loops can be interchanged. The basic parameters of the harmonic-summing module are shown in Table I.

| Parameter | Description | Value |
|-----------|-------------|-------|
| \( N_{temp} \) | Number of templates of the FOP (row) | 85 |
| \( N_{chan} \) | Number of channels of the FOP (column) | \( 2^{21} \) |
| \( N_{hp} \) | Total number of harmonic planes | 8 |
| \( N_{cand} \) | Number of candidates per harmonic plane | 200 |
| \( t_{limit} \) | Computation time limit of each DM trail | 88 ms |

IV. PROPOSED METHODS

The main problem for the harmonic summing module is the irregular memory accesses of the harmonic plane calculation part and it limits the data transfer efficiency. We consider two types of memory access optimisation methods while designing the harmonic plane calculation part: 1) increasing the off-chip memory bandwidth and 2) reducing the number of off-chip memory accesses. Based on the number of processed harmonic planes at a time, two approaches are investigated:
Algorithm 1 General Harmonic-summing Algorithm (SINGLEHP)

\[ SP_1 \leftarrow (\text{filter-output-plane}) \]
\[ CL \leftarrow 0 \{ \text{initialize the detection output} \} \]
\[ \text{for } k = 1 \text{ to } N_{hp}, \text{ do} \]
\[ \quad \text{for } i = -(N_{hp} - 1)/2 \text{ to } (N_{hp} - 1)/2, \text{ do} \]
\[ \quad \quad \text{for } j = 0 \text{ to } N_{chan} - 1, \text{ do} \]
\[ \quad \quad \quad SP_k(i, j) \leftarrow \text{stretch}(SP_1, k, i, j) \{ \text{generate the value in stretched plane} \} \]
\[ \quad \quad HP_k(i, j) \leftarrow HP_{k-1}(i, j) + SP_k(i, j) \{ \text{based on the stretched plane, generate the value in harmonic plane} \} \]
\[ \quad CL \leftarrow \text{append detection}[HP_k(i, j), T_A(k, i)] \{ \text{threshold-detection logic to identify valid peak signals} \} \]
\[ \text{end for} \]
\[ \text{end for} \]
\[ \text{Candidate List } \leftarrow CL \]

the SINGLEHP method (processing a single harmonic plane at a time) and the MULTIPLEHP method (processing multiple harmonic planes at a time).

A. Design Goals

In designing the harmonic-summing module, we mainly consider the latency and energy dissipation of calculating the harmonic planes and detecting the candidates using high-end FPGAs. There are two major factors that affect the execution latency and energy dissipation: 1) parallelisation capacity of an FPGA and 2) data transfer rate between the FPGA and off-chip memory. Most operations in the harmonic-summing module are floating-point operations, however, they are inexpensive functions such as floating-point additions and comparisons with a constant. For high-end FPGAs, there are hundreds of DSP blocks (to implement Floating point operations) and hundred thousand of logic elements that can handle these operations effectively.

In the harmonic plane calculation, the accesses to off-chip memory is not consecutive but irregular due to the index calculations in Equation (1). Ideally, the data transfer bandwidth of any design equals to the device’s theoretical maximum bandwidth, however, this cannot be achieved easily in the harmonic-summing module. Taking a small size FOP (64 \times 2^{12}) as an example, the touching frequencies of the FOP elements in calculating 7 harmonic planes are depicted in Figure 2. For example, 8 points from different positions are needed to calculate point (1000, 60) of \( HP_8 \). In this figure, the size of the deep red area is only 1.7% of the whole FOP, however, each value is touched 204 times. The size of the high touching frequency area (zoomed-in area) is \( 16 \times 2^{10} \) and the sum of the touching times of this area is 73.4% of the overall touching times. It can be seen that the distribution of touching frequency and memory access while calculating do exhibit a very complex pattern. In this paper, we investigate a general design of the harmonic-summing module with low latency, by optimising memory accesses.

The input to the harmonic-summing module, which is the FOP, is up to 710MB in size. Even though it exceeds the on-chip memory size of high-end FPGAs and other types of processors. Though the FOP can be transferred to FPGAs through PCIe bus or Ethernet cable in practice, it is assumed in this research that the FOP is stored in off-chip memory before processing the harmonic-summing module (for example as the output of the FT-convolution also executed on the FPGA device [26]).

In terms of the candidate detection of the harmonic summing module, when there are more than \( N_{cand} \) candidates detected in one harmonic plane, the strategy of sorting candidates has not yet been settled in the PSS sub-project. There are a number of plausible strategies to select candidates, such as storing the largest \( N_{cand} \) candidates or first/last \( N_{cand} \) candidates.
Due to the lack of a settle requirement, and with the assumption that there are usually less than \( N_{\text{cand}} \) candidates (which can be tuned by increasing thresholds), we investigate the methods of storing the last \( N_{\text{cand}} \) candidates. The FPGA device needs to go through all the candidates from each harmonic plane. When there are less than or equal to \( N_{\text{cand}} \) candidates in one harmonic plane, all the candidates will be recorded. Note that based on the method and process order of harmonic plane calculation, the recorded last \( N_{\text{cand}} \) candidates might vary between different approaches.

### B. SingleHP

For the algorithm in Algorithm 1, the processor needs to calculate all harmonic planes individually. The SingleHP method is a straightforward implementation of the harmonic-summing module.

To calculate the points of the \( k \)th harmonic plane \( HP_k \) \((k \geq 2)\), points of the FOP and the \( k-1 \)th harmonic plane \( HP_{k-1} \) are required. During processing, each generated point of \( HP_k \) is compared with a threshold. Since the FOP size, \( N_{\text{temp}}N_{\text{chan}} \), exceeds the on-chip memory of FPGA devices, the FOP and other generated harmonic planes have to be stored in the off-chip memory of FPGA device.

The accesses of loading points from \( HP_{k-1} \) and storing points to \( HP_k \) are both in-order and of consecutive addresses. However, the accesses of loading points from the FOP cannot be calculated as a simple offset. So the data cannot be steamed between off-chip memory and device while processing. To optimise the memory accesses of the SingleHP method, the overall pipeline can be parallelised to increase the off-chip memory bandwidth, and we use that in our implementation.

### C. MultipleHP

In the harmonic summing module, only the candidates are recorded for further processing, it is unnecessary to store the data of all harmonic planes in off-chip memory. To reduce the number of off-chip memory accesses, we investigate the method to get rid of storing harmonic planes except for the FOP. If the points of the same index in multiple or all \( N_{\text{hp}} \) harmonic planes can be generated in parallel, these points can be discarded directly after candidate detection. Without storing the generated points back to off-chip memory, the number of overall off-chip memory accesses can be halved.

By reordering the three for loops in Algorithm 1, we obtain Algorithm 2 where the innermost for loop can be parallelised and the points are discarded after detection.

To optimise the MultipleHP method by reducing the off-chip memory accesses, part of the FOP can be loaded before calculating a chunk of points of all harmonic planes. Two alternatives are proposed and based on the loaded data, they can be distinguished as 1) high touching frequency (by loading as many points as possible in the high touching frequency area of the FOP) and 2) necessary points (by loading points that are needed to calculate a chunk of points in all harmonic planes such as one or several columns of all harmonic planes). For the second method, an FOP reordering method is proposed below to increase data transfer efficiency. Each of these three MultipleHP-based methods adopted at least one type of memory accesses optimisation method and the details of them are as follows.

**Preloading Points with High Touching Frequency:** To create and threshold test \( 8 \) consecutive harmonic planes, each point with the highest touching frequency needs to be loaded over 200 times. If most points with high touching frequency can be preloaded, a large number of load operations can be saved. To further reduce the amount of off-chip memory accesses, part or all of the high touching frequency points can be preloaded in on-chip memory. We use MultipleHP-H to represent the preloading points with high touching frequency method.

The main factor of the MultipleHP-H method is the number of preloaded high touching points \( N_{\text{MHP-H-pred}} \). If the points in the FOP are sorted by touching times, the relationship between the percentage of the FOP size and the percentage of overall touching times is depicted in Figure 3. It can be seen that 2.2% points in the FOP have about 50% of overall touching times and 25% points have 90% percent of overall touching times.

**Loading Necessary Points:** For the Naïve MultipleHP method, calculating one point with the same index of \( N_{\text{hp}} \) harmonic planes, at most \( N_{\text{hp}} \) points need to be loaded from the FOP. However, calculating a chunk of points in all \( N_{\text{hp}} \) harmonic planes need less than \( N_{\text{hp}} \) times the number of points. Take one column with \( N_{\text{temp}} \) points as an example,
it needs $N_{\text{temp}}$ points for $HP_1$, however, $2\left\lceil \frac{(N_{\text{temp}} - 1)}{2} \right\rceil + 1$ points for $HP_2$, $2\left\lceil \frac{(N_{\text{temp}} - 1)}{3} \right\rceil + 1$ points for $HP_3$ and so on. To save loading operations, the harmonic plane calculation task can be decomposed into a number of work-groups. The task of each work group is to generate a number of columns $N_{\text{MultipleHP-N-col}}$ of all $N_{hp}$ harmonic planes, where each column has $N_{\text{temp}}$ points. In a pipeline, the loading part of a work-group can overlap with the computing part of the previous work-group. We use MULTIPLEHP-N to represent the loading necessary points method.

For the MULTIPLEHP-N method, $N_{\text{MultipleHP-N-col}}$ is an important factor that affects the reduced off-chip memory accesses. Assuming the task for each work-group is to generate one column ($N_{\text{MultipleHP-N-col}} = 1$) of $N_{hp}$ harmonic planes ($N_{hp}N_{\text{temp}}$ points in total) and the maximum needed data is

$$2 \sum_{i=1}^{N_{hp}} \left\lceil \frac{N_{\text{temp}} - 1}{2^i} \right\rceil + N_{hp}$$

instead of $N_{hp}N_{\text{temp}}$ points. When $N_{\text{MultipleHP-N-col}}$ is larger than one, more off-chip memory accesses can be reduced. However, the amount of data needed for the same harmonic plane varies based on the column index. For example, if the work-group generates eight columns ($N_{\text{MultipleHP-N-col}} = 8$) of all harmonic planes, the data needed to generate the 3rd harmonic plane are 3 to 4 columns of the FOP. To guarantee that the amount of data loaded for each work-group is a constant (which is needed for efficient pipelining), the maximum number of points for each harmonic plane is chosen.

In this case, when the $N_{\text{MultipleHP-N-col}}$ is specified, the needed number of columns for each harmonic plane can be listed and then the number of needed points for $N_{\text{MultipleHP-N-col}}$ columns can be calculated. Based on the number of overall needed points, the average needed points per column for a work-group is plotted in Figure 4. It can be seen that the average amount drops fast when the value of $N_{\text{MultipleHP-N-col}}$ is smaller than 16 (green dot line) and it decreases slightly toward 64 (red dot line) as the $N_{\text{MultipleHP-N-col}}$ increases. Besides these, the larger the $N_{\text{MultipleHP-N-col}}$, the larger space it needs in the onboard memory. If the $N_{\text{MultipleHP-N-col}}$ is too large, the onboard memory size might limit the $N_{\text{MultipleHP-N-col}}$. As a consequence, it is unnecessary to assign tens or hundreds of columns to a work group.

Reordering the FOP: Comparing with the Naïve MULTIPLEHP method, the MULTIPLE HP-N method can further reduce the total amount of off-chip memory accesses. However, the points needed for each work-group are from at least $N_{hp}$ blocks in FOP and they are from non-consecutive addresses. Thus, the points for each work-group cannot be streamed between off-chip memory and FPGA device.

To optimise the off-chip memory bandwidth of the MULTIPLEHP-N method, we propose the MULTIPLEHP-R method which reorders the FOP to form the reordered FOP (rFOP). After reordering, the needed points to calculate $N_{\text{MultipleHP-R-col}}$ columns of all harmonic planes are from consecutive addresses that can be streamed to the FPGA while processing. However, the size of the reordered FOP is larger than the standard FOP size. Theoretically, the number of rows in the reordered FOP is increased from $N_{\text{temp}}$ to the average needed points per column in Figure 4. Take the $N_{\text{MultipleHP-R-col}} = 16$ as an example, the smallest average needed points per column is 141.5 that makes the size of rFOP at least 1.66x times larger than the original FOP size. It can be seen that the larger the $N_{\text{MultipleHP-R-col}}$, the smaller the relative size of rFOP. The details of rFOP generation and optimisation are discussed in Section V. The latency of extra data transfer and FOP reordering have to be considered in the evaluation of the MULTIPLEHP-R method.

V. ARCHITECTURE AND OPTIMISATION

In this section, we investigate the architecture of the proposed methods and employ OpenCL as the high-level language, whose kernels can be executed on both FPGAs and GPUs. Having that said, since the goal is to evaluate FPGA performance, the optimisation techniques and syntax are dedicated to FPGAs.

A. SINGLEHP kernel

The basic structure of the SINGLEHP kernel while processing the $k$th harmonic plane $HP_k$ is depicted in Figure 5 where $N_{\text{paral}}$ is the parallelisation factor that is restricted by global memory (off-chip memory in this research) bandwidth (GMB) and the logic resources of the FPGA. One optimisation goal for the SINGLEHP kernel is to find the maximum parallelisation factor $N_{\text{paral-max}}$ that leads to a required GMB which equals the physical off-chip memory bandwidth of a specific device.

The FOP, $HP_{k-1}$, $HP_k$, candidate list and $TA$ are all stored in global memory before launching the kernel. When the kernel is launched, $N_{\text{paral}}$ points from $HP_{k-1}$ and $\left\lceil \frac{N_{hp}}{k} \right\rceil$ points from FOP are loaded per clock cycle. These points are summed, according to Equation (1) and Equation (2), to calculate $N_{\text{paral}}$ points of $HP_k$. The generated $N_{\text{paral}}$ points are compared with the corresponding thresholds and detected candidates are saved in a shift register or local memory (on-chip memory in this research) of length $N_{\text{cand}}$, until all FOP points have been processed. Then these $N_{\text{paral}}$ points overwrite the values at the same address of $HP_{k-1}$.

In OpenCL, both single work-item and NDRange kernel types can be adopted to implement the SINGLEHP kernel.
To parallelise $N_{paral}$ points in a single work-item kernel, we partially unroll the outermost loop by a factor of $N_{paral}$ (#pragma unroll $N_{paral}$). Before partially unrolling the outermost loop, the innermost loops are completely unrolled to achieve loop pipelining.

For the NDRange kernel, kernel vectorisation (num_simd_work_items ($N_{paral}$)) and compute unit replication (num_compute_units ($N_{paral}$)) techniques can be employed to parallelise the kernel. Note that detected $N_{cand}$ candidates might be different for the vectorized and replicated kernels, under the condition that the threshold has been triggered more than $N_{cand}$ times. As only the last $N_{cand}$ candidates are stored, different parallelisation result in different execution orders and hence candidates.

The SINGLEHP kernel can be implemented as a generic kernel that needs to be launched $N_{hp}$ times (multiple launches) or a specific kernel that only needs to be launched once (single launch) to generate the candidate list of $H_{hp}$ harmonic planes. The overhead of launching a kernel such as setting kernel arguments will affect the overall latency, especially when the kernel execution latency is short. So the kernel launch time is an important factor for the SINGLEHP kernel. Multiple launches provide more flexibility than the single launch SINGLEHP kernel, as it can be used for any harmonic plane configuration. Both single and multiple launches kernels are evaluated in Section VI.

B. MULTIPLEHP Methods based Kernels

Although parallelising the SINGLEHP kernel can shorten kernel execution latency by increasing GMB, the total amount of global memory accesses (GMA) is not reduced. The main advantage of the MULTIPLEHP method is the reduction of the required GMA by processing multiple harmonic planes at the same time. A number of optimisation techniques are investigated for the MULTIPLEHP-based methods in the following.

Naïve MULTIPLEHP: The Naïve MULTIPLEHP kernel calculates $N_{paral}$ points of all $N_{hp}$ harmonic planes with the same index, where $N_{paral}$ is the parallelisation factor. The architecture of the Naïve MULTIPLEHP kernel is shown in Figure 6, where the operations in the red dot rectangle have to be parallelised $N_{paral}$ times to process $N_{paral}$ points of all harmonic planes. In OpenCL, this is implemented as a single work-item type, and the #unroll pragma $N_{paral}$ is added before the main for loop in the kernel code.

The FOP is stored in global memory and $N_{hp}$ points ($(i, j)$, $([i/2], [j/2])$, ..., $([i/N_{hp}], [j/N_{hp}])$) are loaded in parallel to generate point $(i, j)$ of all $N_{hp}$ harmonic planes. Then these $N_{hp}$ points are compared with the corresponding thresholds, stored as constant memory. $N_{hp}$ independent arrays of size $N_{cand}$, one corresponding to each harmonic plane, are employed to store the candidates. Both local memory and shift register can be adopted to implement $N_{hp}$ arrays and the performance difference is evaluated in Section VI. After all $N_{hp}$ harmonic planes have been processed, the $N_{hp}$ candidate arrays are sent back to global memory. Because the loading accesses to the global memory are irregular, a high memory stall percentage will impede the kernel from achieving a high performance.

MULTIPLEHP-H: The MULTIPLEHP-H kernel builds on the Naïve MULTIPLEHP kernel, which is a single work-item kernel. MULTIPLEHP-H is however split into two parts, preloading and computing. The $N_{MultipleHP-H-preld}$ preloaded points that can be seen as constant cache memory are loaded into a FIFO at runtime. In processing one FOP, there is no overlap between the prefetching and computing parts. The available local memory of the FPGA and the number of high touching frequency points affects the performance of the MULTIPLEHP-H kernel. If the FOP size is comparable to the available local memory, most of the points with high touching frequency can be loaded and then most of the global memory accesses can be reduced. However, if the number of high touching frequency points is significantly larger than the local memory size, it is impossible for the device to hold most of these important points. Besides these, the large proportion of the used on-chip memory might lead to the decrease of kernel frequency. In this case, it is necessary to search for the suitable $N_{MultipleHP-H-preld}$ for the target FPGA by testing a range of preloading data sizes. The relationship between the $N_{MultipleHP-H-preld}$ and the kernel performance is investigated in Section VI.

MULTIPLEHP-N: The MULTIPLEHP-N method is a memory accesses saving method, as discussed in Section IV-C. It decomposes the overall task into a number of work-groups, and the task for each work-group is to process $N_{MultipleHP-N-col}$ columns of all harmonic planes. The NDRange kernel type is employed and the preloading part of a work-group overlaps with the computing part of the
previous work-group. For the NDRange kernel, different workgroups do not share local memory and it is inefficient to save candidates in global memory during processing. The hybrid kernel type that contains both single work-item type and NDRange type is employed to implement the preloading necessary points kernel (MULTIPLEHP-N).

The relationship between the work group size of the NDRange kernel and the execution latency is studied next. The task of each work-group is to generate $N_{\text{MultipleHP-N-col}}$ columns of all harmonic planes, which contains $N_{\text{MultipleHP-N-col}}N_{\text{chan}}$ points. For each work-group, $N_{h}\times N_{\text{MultipleHP-N-col}}N_{\text{chan}}$ points are stored in local memory using the OpenCL barrier technique (barrier (CLK_LOCAL_MEM_FENCE)). A number of points in these $N_{h}\times N_{\text{MultipleHP-N-col}}N_{\text{chan}}$ points are from the same index in the FOP and they only need to be loaded once.

The NDRange harmonic plane calculation kernel is connected with the single work-item candidate detection kernel through OpenCL channels, which is a FIFO buffer in essence. The OpenCL channel is an effective approach to transfer data between different kernels without touching global memory. The candidate detection part is the same as that of Naïve MULTIPLEHP kernel and MULTIPLEHP-H kernel.

MULTIPLEHP-R: The MULTIPLEHP-R kernel is based on the MULTIPLEHP-N kernel and the main difference is the order of the data for each work-group. After reordering, the points needed for a work-group are from consecutive addresses.

The total amount of needed data for a work-group ($N_{\text{total/wg}}$) is the product of average needed data per column times the number of columns per work-group ($N_{\text{MultipleHP-R-col}}$) (see also Figure 7). To achieve stream mode in global memory access, the number of loaded points per clock cycle ($N_{\text{points/cc}}$) has to be an integer constant, which makes the product of $N_{\text{points/cc}}$ and work-group size ($S_{\text{workgroup}}$) usually larger than $N_{\text{total/wg}}$ and never less, 

$$N_{\text{total/wg}} \leq N_{\text{points/cc}}S_{\text{workgroup}}.$$ 

In case of difference, the input array for each work-group has to be padded with dummy values at the end. The relationship between $N_{\text{points/cc}}$ and $N_{\text{MultipleHP-R-col}}$ is shown in Table II, where $N_{\text{points/wi}}$ is the executed points of all harmonic planes per work-item. The value in the bracket ($\times$) represents the ratio of total loaded points over the FOP size:

$$\frac{N_{\text{points/cc}}S_{\text{workgroup}}N_{\text{workgroup}}}{N_{\text{chan}}N_{\text{temp}}} = \frac{N_{\text{workgroup}}}{N_{\text{workgroup}}},$$

where $N_{\text{workgroup}}$ is the total number of work-groups. We use MULTIPLEHP-R($N_{\text{MultipleHP-R-col}}, N_{\text{points/wi}}$) to represent kernel MULTIPLEHP-R with the specified settings. The larger $N_{\text{MultipleHP-R-col}}$ and $N_{\text{points/wi}}$, the less data needs to be loaded from global memory. Because of physical limitation, if the needed bandwidth of loading $N_{\text{points/cc}}$ points exceeds the total device off-chip memory bandwidth, the performance will not increase and the kernel was not implemented.

It is clear that $N_{\text{points/cc}}, N_{\text{MultipleHP-R-col}},$ and $N_{\text{points/wi}}$ are the three main parameters for kernel MULTIPLEHP-R and they have to be balanced to achieve good performance. Using the AOCL compiler, it becomes apparent that using the number that is powers of 2 for $N_{\text{points/cc}}$ results in more efficient implementations than other numbers. Hence, to make the value of $N_{\text{points/cc}}$ equal a power of 2, more data might need to be loaded for each work group. Take the kernel MULTIPLEHP-R-(8, 8) for example, the value of $N_{\text{points/cc}}$ is 13, it has to be increased to the nearest power of 2, which is 16. Since the number of loaded data per work-group is $N_{\text{points/cc}}S_{\text{workgroup}}$, the increase of $N_{\text{points/cc}}$ leads to the increase of loading operations (as can be seen in the example in Figure 7). The optimised $N_{\text{points/cc}}$, where $N_{\text{points/cc}}$ is the lowest power of 2 greater or equal to the corresponding $N_{\text{points/cc}}$ of values without optimisation in Table II. When $N_{\text{MultipleHP-R-col}} \geq 4$, the total loaded data is twice the FOP size (value in the bracket).

Take the $N_{\text{MultipleHP-R-col}} = 16$ and half FOP as an example, the input array needed for one work-group is depicted in Figure 7 where SPI represents the needed points to form the ith stretch plane and “PADDED” are the dummy points to be padded at the end of each array. It can be seen that when $N_{\text{points/wi}}$ is optimised to a power of 2, more points need to be loaded during processing.

For the hybrid kernels (combining NDRange and single work-item kernels) MULTIPLEHP-H, MULTIPLEHP-N, and MULTIPLEHP-R, adding attributes num_simd_work_items($N_{\text{paral}}$) or num_compute_units($N_{\text{paral}}$) can only parallelise the NDRange part but not the single work-item part. To vectorize the hybrid kernel and make it execute in a single instruction multiple data (SIMD) fashion, it has to be parallelised...
manually in the kernel code.

C. Comparison

The main challenge for FPGA devices in efficiently implementing the harmonic-summing module is the global memory bandwidth and the number of global memory accesses. In this section, we analyze the GMA of the kernel discussed above and the GMB is evaluated in Section VI.

For the SingleHP method, to process \( N_{hp} \) harmonic planes, the minimum number of FOP point accesses is:

\[
GMA_{SingleHP-min} = \sum_{i=1}^{N_{hp}} \left[ \frac{N_{chan}}{i} \right] \left[ \frac{N_{temp} - 1}{i} \right] + 2(N_{hp} - 1)N_{temp}N_{chan}.
\]

Except for calculating HP1, the loaded points from the FOP have to be summed with the points of the HPk harmonic plane and then the generated points of the next harmonic planes HPk+1 are stored. The numbers of load and store operations of this part are both \( (N_{hp} - 1)N_{temp}N_{chan} \). Hence, the minimum amount of global memory accesses for SingleHP method \( GMA_{SingleHP-min} \) is the sum of these accesses:

\[
GMA_{SingleHP-min} = \sum_{i=1}^{N_{hp}} \left[ \frac{N_{chan}}{i} \right] \left[ \frac{N_{temp} - 1}{i} \right] + 2(N_{hp} - 1)N_{temp}N_{chan}.
\]

In the MultipleHP methods, only the FOP and candidates need to be stored in global memory and the number of store operations to global memory for all MultipleHP kernels is 0. For the Naïve MultipleHP kernel, at most \( N_{hp} \) points from FOP need to be loaded to calculate one point of the same index in all \( N_{hp} \) harmonic planes. In this case, the maximum number of memory accesses is \( GMA_{Naïve-MultipleHP-max} = N_{hp}N_{temp}N_{chan} \).

For the preloading high touching frequency method MultipleHP-H, the GMA depends on \( N_{MultipleHP-H-preld} \). The maximum amount of memory accesses is \( GMA_{MultipleHP-H-max} = N_{hp}N_{temp}N_{chan} - N_{MultipleHP-H-preld} \) and the minimum amount is to store the whole FOP in the local memory, which means \( GMA_{MultipleHP-H-min} = N_{temp}N_{chan} \). For the preloading necessary points method MultipleHP-N and the reorder FOP method MultipleHP-R, the \( GMA_{MultipleHP-N} \) and \( GMA_{MultipleHP-R} \) are both multiple of the FOP size \( N_{temp}N_{chan} \). Table III summarizes the GMA of the different kernels. \( C_0 \), \( C_1 \) and \( C_2 \) are all constants and no less than 1. The range of \( C_0 \) is \( [1, \frac{N_{hp}N_{temp}N_{chan}}{N_{MultipleHP-H-preld}}] \). For \( C_1 \) and \( C_2 \), \( C_1 \leq C_2 \) and, in Table III, \( C_2 = 2 \) when \( N_{MultipleHP-R-col} \geq 4 \).

The load accesses of the SingleHP kernel \( GMA_{SingleHP-min} \) is larger than the overall point accesses (store+load) of each MultipleHP method based kernel. This is the major advantage of the MultipleHP method over the SingleHP method.

VI. EXPERIMENTAL EVALUATION

To experimentally evaluate the harmonic-summing module, the straightforward SingleHP method and the proposed MultipleHP-based methods are evaluated in this section. The FPGA-based harmonic-summing kernels are assessed according to their resource usage, execution latency, and energy dissipation. Additionally, we compare those results to latency and energy dissipation of the kernels implemented on GPU and multicore CPUs.

A. Experimental Setup

Four different devices are employed to evaluate the performance of the proposed designs on CPU, GPU, and FPGAs. Two types of Intel FPGAs (Stratix V, referred to as S5, and Arria 10, referred to as A10) are compared with one mid-range AMD R7 GPU, referred to as R7, and a general Intel i7 CPU, referred to as i7. The specifications of these platforms are given in Table IV. The FPGA and GPU cards are connected to the host processor through the PCIe bus.

All FPGA-targeting OpenCL kernels are compiled using AOCL version 16.0.0.222 and GPU-targeting kernels are compiled using AMD APP SDK version 3.0. For the CPU platform, the C code, which is based on the same kernel code, is compiled using GCC, using OpenMP for parallelisation.

Since the top half (from row 1 to \( \frac{N_{temp}}{2} \)) and the bottom half (from row \( \frac{N_{temp}}{2} + 1 \) to -1) are independent for the harmonic-summing module, we investigate the performance, in terms of the execution latency and energy dissipation, of half of the FOP as specified in Table IV, which size is \( 42 \times 2^{21} \). Remember from Section III that the upper and lower half of the FOP can be processed independently and the required processing is identical. The size of candidate list is 200.

B. Resource Usage

Because the harmonic-summing module is not a compute-intensive application, the DSP block utilization of all implementations is less than 5%. We discuss the logic utilization, RAM blocks utilization, and kernel frequency in this section.

SingleHP: A series of SingleHP kernels with different parallelisation factors \( N_{paral} \) are evaluated. These kernels are employed to generate eight harmonic planes of half FOP. All these kernels are NDRange kernels and the work group sizes are set to 256. The usage of logic cells and RAM blocks of these kernels are given in Figure 8 where ‘S’ and ‘M’
represent single launch and multiple launches, and 'V' and 'R' represent kernel vectorization and replication. The candidate detection part is included, and the local memory is employed to store the candidate during processing. When $N_{\text{paral}} = 1$, it means the kernel is not parallelised and that vectorization and replication are not employed.

It can be seen that the usage of both resources increases as $N_{\text{paral}}$ increases. These trends are similar to those observed for execution on S5. The kernel frequency drops as the resource usage increases across all kernels. Take the kernel SINGLEHP-$(M,V)$ on A10 as an example, its frequency decreases from 266.9 MHz at $N_{\text{paral}} = 1$ to 236.8 MHz at $N_{\text{paral}} = 16$.

**MULTIPLEHP**: In terms of the MULTIPLEHP designs, Naïve MULTIPLEHP, MULTIPLEHP-H, MULTIPLEHP-H, and MULTIPLEHP-R (Section [V]) are evaluated.

**Naïve MULTIPLEHP and MULTIPLEHP-H**: The MULTIPLEHP-H is based on the Naïve MULTIPLEHP-H, and the main difference is that it preloads a block of data before calculating. The resource usage of these kernels is plotted over the preloaded data size in Figure 8. The value points for $N_{\text{MULTIPLEHP-H}} = 0$ correspond to Naïve MULTIPLEHP. The logic utilization is not affected by the increase of $N_{\text{MULTIPLEHP-H}}$, however, the RAM blocks utilization increases. The kernel frequency is around 210 MHz for S5 based implementations and 220 MHz for A10 based implementations.

**MULTIPLEHP-N and MULTIPLEHP-R**: In contrast to MULTIPLEHP-H, kernel MULTIPLEHP-N and MULTIPLEHP-R do not depend heavily on local memory size. MULTIPLEHP-R is based on MULTIPLEHP-N, however, it does not need to load points from different locations.

For MULTIPLEHP-N, different column numbers ($N_{\text{MULTIPLEHP-N}}$) are evaluated, and the results are listed in Table V. As can be seen with increasing $N_{\text{MULTIPLEHP-N}}$, both logic cell and RAM block utilization increase. For most of the kernels, the kernel frequency is decreased as $N_{\text{MULTIPLEHP-N}}$ increases.

Regarding MULTIPLEHP-R, to arrange the data for each work group into a consecutive address area, the half FOP is reordered into a half RFO (Section [V-C]), in the host program using `memcpy()`. The reordering latency on the employed host is 87.8 ms and the performance of two variants of MULTIPLEHP-R kernels (generating 16 and 64 columns of all eight harmonic planes per work group) are evaluated, which is shown in Table VI. Four different points per work-item values $N_{\text{points}}/w_\text{cc}$ (1, 2, 4, and 8) are tested in this research. Since the values of $N_{\text{points}}/w_\text{cc}$ for $N_{\text{points}}/w_\text{cc} = 1$ and $N_{\text{points}}/w_\text{cc} = 2$ are already powers of 2, so we focus on the other two conditions ($N_{\text{points}}/w_\text{cc} = 4$ and $N_{\text{points}}/w_\text{cc} = 8$) and the resource usage of the general and the optimised implementations with these values are given in Table VI. For the optimised implementations, the values of $N_{\text{points}}/w_\text{cc}$ are powers of 2 and this costs fewer logic cells than the general implementations. Since more points are loaded per clock cycle,
the optimised implementations consume more RAM blocks. Besides these, the kernel frequency of the optimised implementations is higher than that of general implementations.

Since $N_{\text{MultipleHP-R-col}}$, $N_{\text{p/wi}}$, and $N_{\text{points/ce}}$ are three main parameters that affect the performance of MULTIPLEHP-R, we investigate the trend of changing these parameters, but here without candidate detection, hence the values in Table VI are only for the NDRRange part. We do this because after combining with the candidate detection, some of the MULTIPLEHP-R kernels such as MULTIPLEHP-R-(64, 8) cannot be compiled because of the limited resources, and we wanted to explore the influence of the parameters in a good range. We employ the MULTIPLEHP-R-(16, 4) kernel with candidate detection, which can be compiled on both S5 and A10, to compare with other methods. In the future, as FPGA technology upgrades, the amount of on-chip logic cells and RAM blocks increase. The values of $N_{\text{MultipleHP-R-col}}$ and $N_{\text{p/wi}}$ can be raised, and the execution latency is likely to be faster than that achieved in Table VI.

C. Latency Evaluation

Harmonic Plane Calculation on FPGA: To find the suitable design for a specific device, we evaluate the overall execution latency of the harmonic-summing module, including the harmonic plane calculation and the candidate detection. The points of the 8th harmonic plane are compared with the result of a Matlab implementation to verify the correctness of the harmonic plane calculation in the different designs.

SINGLEHP: The used GMBS and execution latencies of the SINGLEHP kernel with various $N_{\text{paral}}$ in Section VI-B are shown in Figure 10. As $N_{\text{paral}}$ increases the GMBS of all SINGLEHP kernels increase, however, not all execution latencies are decreased.

For the two multiple launches (‘M’) kernels SINGLEHP-(M, V) and SINGLEHP-(M, R), the launching overhead is hundreds of times smaller than the kernel execution latency and hence negligible. For the two single launch kernels SINGLEHP-(S, V) and SINGLEHP-(S, R), the performance stops increasing when $N_{\text{paral}}$ is larger than 8. When $N_{\text{paral}} = 8$, kernel SINGLEHP-(S, R) performs better than other kernels and the SINGLEHP-(M, R) kernel performs best when $N_{\text{paral}} = 16$, which is about 7.5 times faster than SINGLEHP-(M, ) with $N_{\text{paral}} = 1$.

Naive MULTIPLEHP: The execution latency of kernel Naive MULTIPLEHP on S5 is over one second (1,210 ms), however, the same kernel achieves a better performance, which is less than 400 ms on A10. The main reason is the kernel frequency achieved on A10 is over two times higher than that on S5. This might be caused by the board support packages (BSPs) provided by different vendors.

MULTIPLEHP-H: The relationship between the number of preloaded data points $N_{\text{MultipleHP-H-preld}}$ and the execution latency of MULTIPLEHP-H is investigated on both S5 and A10. The half FOP is transposed and then processed row by row (each row has $\frac{N_{\text{temp}}}{2}$ points). The execution latencies of these kernels are depicted in Figure 11. It is clear that the execution latency does not have a linear relationship with the $N_{\text{MultipleHP-H-preld}}$ and the execution latency might increase as $N_{\text{MultipleHP-H-preld}}$ gets larger. Unfortunately, even the largest $N_{\text{MultipleHP-H-preld}}$ ($5 \times 2^{15}$) used in the experiments, and limited by the available FPGA resources, contains only 4.7% of the total number of all memory accesses. The best performance achieved on S5 and A10 are both by executing kernel MULTIPLEHP-H-(S, $2^{15}$). Some improvements could be made by overlapping the loading of the high touching frequency points with the computing part, but not substantially. Overall, MULTIPLEHP-H is not gaining performance if the local memory size is not large enough to hold most of the points with high touching frequency.

MULTIPLEHP-N: For kernel MULTIPLEHP-N, the necessary data for each work group are from nonconsecutive addresses and this affects the loading section in achieving streaming mode, which is crucial to fully use the available theoretical bandwidth. Although executing more columns per work group can reduce GMA, the value of $N_{\text{MultipleHP-N-col}}$ does not affect performance. The execution latency of MULTIPLEHP-N is affected by the kernel frequency, which is given in Table V. We employ the kernel with the fastest execution latency to compare with other methods, which is MULTIPLEHP-N(1).

MULTIPLEHP-R: The kernel execution latency and global memory occupancy during execution on A10 are given in Table VI as well. When the value of $N_{\text{points/ce}}$ is a power of 2, the execution latency decreases as $N_{\text{points/ce}}$ increases. Although the occupancy of loading operations drops, the values for the optimised kernels decreases slower than that of the general kernels. The fastest variant of MULTIPLEHP-R in
Figure 12. Execution latency of proposed harmonic summing methods with candidate detection on A10, where SHP represents SINGLEHP and MHP represents MULTIPLEHP.

Table VI
RESOURCE USAGE AND EXECUTION LATENCY OF MULTIPLEHP-R (NDRange part only) with $(N_{i,p/cc}^c)$ IS POWER OF 2 AND WITHOUT OPTIMISING GMB ON A10 (without candidate detection)

| $N_{i,p/cc}^c$ | $N_{p/w}$ | Logic utilization | RAM blocks | Freq. (MHz) | Latency (ms) | Occup. | Logic utilization | RAM blocks | Freq. (MHz) | Latency (ms) | Occup. |
|---------------|----------|-------------------|------------|-------------|--------------|--------|-------------------|------------|-------------|--------------|--------|
| 54            | 8        | 5%                | 64         | 286.5       | 107.7        | 95.7%  | 5%                | 64         | 286.5       | 107.7        | 95.7%  |
| 8             | 4        | 15%               | 16         | 263.0       | 163.9        | 96.6%  | 15%               | 16         | 263.0       | 163.9        | 96.6%  |
| 16            | 8        | 19%               | 16         | 263.0       | 163.9        | 96.6%  | 19%               | 16         | 263.0       | 163.9        | 96.6%  |

Comparing CPU and GPU: We are now comparing the performance of the proposed kernels on CPU (using adjusted OpenCL code) and GPU (using equivalent OpenMP implementations). SINGLEHP-R$(M,D)$ is evaluated on A10 GPU, and the host argument settings are the same as for the FPGA-based implementation. The straightforward C code with OpenMP directives, using three levels of for loops, which is the same as Algorithm I, is evaluated on the $I7$ CPU using all four cores. The execution latency of SINGLEHP using one core of $I7$ CPU ($I7-1C$) can be compared to the baseline and the speedups over it on other devices are given in Table VII, where $I7-4C$ represents using four cores of the $I7$ CPU. It can be seen that $R7$ performs best among these devices and it is about 3.6x times faster than the A10 FPGA. The $R7$ has two major advantages over $S5$ and A10: 1) operating frequency and 2) off-chip memory bandwidth. Though the maximum frequency of $A10$ is higher than $R7$, the maximum frequencies of the implemented kernels are less than 300 MHz in this work.

Regarding the MULTIPLEHP kernels on GPU, a similar OpenCL code as used for the FPGA kernels of $S$ and $R$ are tested. The execution latencies of these kernels are both over 30 seconds, which are about a hundred times slower than that of a single A10 FPGA. Because these two variants are single work-item kernels, the GPU cannot parallelise operations on multiple stream processors. For the fastest MULTIPLEHP kernel on A10, which is MULTIPLEHP-R$(N,D)$ (NDRange kernel part), the execution latency of it (without candidates detection) on $R7$ is 19.7 ms, and it is 3.7 times faster than achieved on $A10$. After combining with the candidate detection, which is a single work-item kernel, the performance drops as $N_{can}$ increases. When $N_{can}=1$, the execution latency is 46.8 ms. However, when $N_{can}$ is increased to 200, the latency increases to 10 seconds. Since single work-item kernels on GPU cannot explore their performance potential, we only compare the performance of NDRange kernels on FPGA and GPU devices.

Based on the above, an $R7$ is over 3.7 times faster than
an A10 in executing the same NDRange kernels. Regarding the single work-item kernels, GPU implementations cannot compete with FPGAs, being tens to hundreds of times slower than FPGAs.

D. Energy Dissipation and Power Consumption

The execution latency is a significant performance criterion for the harmonic-summing module. However, in the context of the pulsar search engine in SKA1-MID, there will be over 2,000 beams that need to be computed in parallel, which is constantly done for many years. As a result, the power consumption is another essential criterion which we investigate in this subsection.

To do so, we calculate the difference between the system power consumption \( P_{idle} \), including the acceleration device, in idle status and the power consumption \( P_{running} \) when the system is executing the kernel. To make sure the value of \( P_{running} \) is stable, each kernel is launched hundreds of times using a loop, which takes several minutes.

The power consumption is measured using a plug-in power meter (Ego smart socket ESS-AU). For the FPGA measurements, the calculated power consumption is the value of using three A10 cards in one host. The power consumption and energy dissipation of executing different kernels are given in Table VIII. The energy cost is the dissipation of processing the input half FOP, and the energy saving ratio is compared with the \( I7 – 1C \). Since the execution latencies of MULTIPLEHP kernels with the single work-item kernel (in Section VII-C) on GPU are over ten times larger than those on FPGA, the MULTIPLEHP kernels with single work-item part are not compared with GPU.

Although the execution latency on \( R7 \) is faster than that of A10, the energy dissipation of \( R7 \) is over 1.8 times higher than that of three A10s. An interesting observation from Table VIII is that the power consumption of kernel SINGLEHP-(\( M, R \)) and MULTIPLEHP-R on A10 are significantly higher than other MULTIPLEHP kernels on A10. The main reason is that the used GMB of SINGLEHP-(\( M, R \)) and MULTIPLEHP-R are optimised and much higher than other kernels. Streaming data between off-chip memory and FPGA makes the power consumption of a kernel up to 3 times higher than that of other MULTIPLEHP kernels.

In summary, it can be found that a single \( R7 \) needs over 2x times more power than three A10 cards. Regarding the energy dissipation, the cost of \( R7 \) is up to 2.6x times higher than three A10 cards in executing the same kernels while providing similar performance.

VII. CONCLUSIONS

In this paper, we investigated FPGA designs of one module of the SKA pulsar search engine called harmonic-summing. OpenCL was chosen to implement the proposed designs, and two types of FPGA cards (Inte Stratix V and Arria 10 FPGAs) and a GPU card were employed for evaluation. Two approaches of harmonic-summing were studied: 1) store intermediate data in off-chip memory and 2) process the input signals directly without storing intermediate data. For the second approach, since a naive implementation does not provide good performance, two approaches of preloading data were proposed and evaluated: 1) preloading points that are touched most 2) preloading all necessary points that are used to generate a chunk of output points. For the necessary points approaches, the reorder of input signals is investigated as well.

The extensive experimental evaluation demonstrated that kernels with intermediate data storage perform worse than kernels without storing intermediate data in both execution latency and power consumption. A single FPGA can achieve 9.5x speedup over single-core CPU using the general SINGLEHP method. By using three A10 FPGAs, the NDRange MULTIPLEHP kernels perform significantly better than a single \( R7 \) GPU in power consumption, while only being slightly slower regarding execution latency. To process the same amount of data using the same OpenCL kernel, \( R7 \) GPU costs up to 2.6x times more energy than three A10 FPGAs. This work shows that FPGA devices can be a good solution for the SKA project for the processing parts of the pulsar search pipeline.

ACKNOWLEDGMENT

The authors acknowledge discussions with the TDT, a collaboration between Manchester and Oxford Universities, and MPIfR Bonn and the work benefitted from their collaboration. We would like to thank Petr Dobias and Emmanuel Casseau from IRISA, University of Rennes 1. We gratefully acknowledge that this research was financially supported by the SKA funding of the New Zealand government through the Ministry of Business, Innovation and Employment (MBIE).

REFERENCES

[1] Andrew Canis, Jongsook Choi, Mark Aldham, Victor Zhang, Ahmed Kammoona, Jason H Anderson, Stephen Brown, and Tomasz Czajkowski. Legup: high-level synthesis for fpga-based processor/accelerator systems. in Proceedings of the 19th ACM/SIGDA international symposium on Field programmable gate arrays, pages 33-36. ACM, 2011.
[2] Christopher Carilli and Steve Rawlings. Science with the Square Kilometer Array: motivation, key science projects, standards and assumptions, arXiv preprint astro-ph/0409274, 2004.
[3] Doris Chen and Deshanand Singh. Invited paper: Using OpenCL to evaluate the efficiency of CPUS, GPUs and FPGAS for information filtering, in 22nd International Conference on Field Programmable Logic and Applications (FPL), 5–12. IEEE, 2012.
[4] Tomasz S Czajkowski, Uttu Aydonat, Dmitry Denisenko, John Freeman, Michael Kinsner, David Neto, Jason Wong, Peter Vannaccouras, and Deshanand P Singh. From OpenCL to high-performance hardware on FPGAs. In 22nd International Conference on Field Programmable Logic and Applications (FPL), 531–534. IEEE, 2012.
