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Reusing Verification Assertions as Security Checkers for Hardware Trojan Detection

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Abstract—Globalization in the semiconductor industry enables fabless design houses to reduce their costs, save time, and make use of newer technologies. However, the offshoring of Integrated Circuit (IC) fabrication has negative sides, including threats such as Hardware Trojans (HTs) – a type of malicious logic that is not trivial to detect. One aspect of IC design that is not affected by globalization is the need for thorough verification. Verification engineers devise complex assets to make sure designs are bug-free, including assertions. This knowledge is typically not reused once verification is over. The premise of this paper is that verification assets that already exist can be turned into effective security checkers for HT detection. For this purpose, we show how assertions can be used as online monitors. To this end, we propose a security metric and an assertion selection flow that leverages Cadence JasperGold Security Path Verification (SPV). The experimental results show that our approach scales for industry-size circuits by analyzing more than 100 assertions for different Intellectual Properties (IPs) of the OpenTitan System-on-Chip (SoC). Moreover, our detection solution is pragmatic since it does not rely on the HT activation mechanism.

Index Terms—Hardware Trojans, Hardware Security, Security Coverage, Verification

I. INTRODUCTION AND BACKGROUND

Over the last decades, the Integrated Circuit (IC) industry has experienced significant changes in the fabrication process due to globalization. This globalization has made the companies define new strategies to reduce their costs in the IC supply chain. Hence, today, it is very unlikely for a design house to fabricate a circuit. Instead, the fabrication process is outsourced to third-party vendors. This opens an opportunity for an attacker to replace some parts of the original circuit with altered ones, or even to remove some logic in the design process [1]. This threat is generally referred to as Hardware Trojans (HTs). Hardware Trojans are known as one of the greatest threats against the trustworthiness of ICs, and they have raised serious concerns about the reliability and security of digital designs [2]. If an IC is utilized in a product/system while Trojan(s) remain there, it may lead to functionality change, reliability degradation/denial of service, and information or data leakage [3].

Unfortunately, typical test and verification tasks are not sufficient to detect HTs that are inserted during the fabrication stage [1] (i.e., fabrication-time attacks). Many accepted approaches exist to enable HT detection [2], [4]–[8]. In these approaches, it is tried to detect the HTs either by disruptive methods or non-disruptive ones. In disruptive methods, the IC is being de-masked and if necessary, de-layered. Then it goes through the investigation using electron microscopes and special measurement equipment to check if it is the same as designed [4]. Non-disruptive methods focus on catching the unwanted behavior of the circuit using analytical or formal methods. Mostly used techniques in non-disruptive methods include side-channel analysis and online monitoring. Side-channel analysis techniques are based on the concept of checking the different parametric characteristics of the circuit such as power and timing and looking for a deviation from the expected signatures to detect Trojans [5], [6]. The major drawback of the side-channel analysis technique is that the obtained results from the analysis can be confused with the process variation. Some approaches try to enhance the detection probability of this technique by applying Automatic Test Pattern Generation (ATPG) or dummy flip-flop insertion [2], [7].

On the other hand, online monitoring techniques rely on embedding checker circuits in different locations of the design to catch the unwanted behavior of the system [8]–[10]. One of the popular approaches for building these checker circuits is to use assertions [11]. Assertions precisely describe the expected behavior of the circuit and help to check if there is a deviation between the intent and the actual behavior of the design using simulation or formal methods [11]. Assertion-Based Verification (ABV) techniques are mostly implemented by writing assertion checkers in Property Specification Language (PSL) [12] or SystemVerilog [13].

Although online monitoring techniques offer a high detection coverage, they impose significant overheads on the circuit. In recent years, it is tried to decrease the overheads while keeping the detection coverage at the maximum level, but still, the trade-off between the detection coverage and the imposed overheads is unfavorable [10].

Since most of the time and efforts spent on the design and verification processes do not contribute to achieving HT detection, a considerable amount of design knowledge (i.e., test benches, coverage, metrics, assertions) is generated and then not re-utilized. In this paper, we propose a methodology for selecting the assertions that have already been written by verification engineers (for functional verification) and explain how to reuse them for security purposes (i.e., HT detection).
Reusing the available data seems to be a wiser choice rather than spending similar (or more) time and resources on complex detection schemes. For this purpose, we present a new metric called security coverage to evaluate the efficiency of online checkers in detecting Trojans considering the amount of overhead imposing on the circuit. This metric helps to remove assertions that are not helpful for HT detection from the circuit in an automated fashion while there is no need for detailed knowledge of the circuit.

The remainder of the paper is organized as follows: In Section II we explain the prerequisites for converting assertions to security checkers and introduce a new security coverage metric. The effectiveness of the selected checkers is studied in Section III. Section IV explains a methodology to optimize the security checker list, and experimental results are presented in Section V. Finally, Section VI concludes the paper.

II. ASSERTIONS AS TROJAN DETECTORS

In this section, we answer the question can assertions be devised for detecting Trojans? For this purpose, we study the B19-T500 benchmark from Trust-Hub [14] which is a Trojan-inserted version of the B19 circuit from the ITC’99 benchmark suite [15]. Trust-Hub benchmarks provide an opportunity for developers to verify the effectiveness of their HT detection schemes since the Trojans can be considered as a representative for real ones due to their small sizes and rare triggering conditions [16]. This implies the HTs remain hidden during standard verification checks [17].

More precisely, the B19 benchmark consists of four copies of the Viper processor, and the Trojan circuit is located inside each Viper processor. The Trojan is triggered by a counter which counts a specific vector and resets with another specific vector. If the counter gets a value between 3’b100 and 3’b110, the Trojan is triggered. The Trojan payload modifies the bits of the Instruction Register (IR) of the embedded Viper processor and changes the functionality of the circuit [14].

A. Prerequisite of good Security Checker

The ideal conditions for assertions to be considered as good security checkers are: 1) they should not impose significant overheads on the circuit once they are synthesized (many of them may be needed in complex designs to reach the high detection coverage), and 2) they should not be limited in scope. Assertions that only check some local signals (i.e., checking if one of the specific bits of a register is 0 or 1) are rarely interesting. Instead, assertions that capture a high-level behavior are preferred. From now on, we call these assertions “top-level assertions”.

To clarify this concept, we have defined a set of manually written assertions that satisfy the aforementioned conditions. While the easiest way for detecting the B19-T500 Trojan is to write some assertions for checking the IR bits directly, this style is not practical for two reasons: First, in a realistic scenario, we do not have any information about the locations of HTs. Even taking this fact into account, thousands (or more) of this type of assertion would be needed for covering all the necessary checks of individual signals, even for small circuits. Furthermore, this style of assertion writing violates the second condition of being a good security checker: it does not describe any notion of a system-level behavior.

Table I contains the top-level assertions considered for detecting Trojans in the B19-T500 circuit. They have been written in PSL. As shown in the table, the assertions check the correctness of transactions between the memory and processor. The first two assertions check the violation (invalid access) of the write operation in the memory while the next ones do the same check for the read operation. For more details about the mechanism of the memory access in the Viper processor, the reader is referred to its documentation [18]. Our simulation results show that our assertions can effectively detect the Trojan inserted in the B19-T500 benchmark. The effectiveness of these assertions is discussed later in Section V.

B. Binding the assertions to the main design

While simulation provides useful information about the incorrect behavior of the circuit and different internal values, it is not sufficient for determining the performance characteristics of the design such as power, timing, and area. Hence, it is impossible to qualify the assertions via simulations only. Instead, the design should be synthesized, and exact performance reports being taken into consideration. As mentioned earlier, PSL and SystemVerilog are the most commonly used languages for describing assertions, but these assertions are not directly synthesizable. Therefore, we have to transform these assertions to a synthesizable format such that the performance results can be obtained after synthesis. For this purpose, we use the MBAC tool [19] to convert PSL and SystemVerilog assertions to a synthesizable Verilog format.

After generating a synthesizable code from the assertions, they can be bound to the main circuit so that we can evaluate the effectiveness of the assertions based on the overheads imposed on the circuit. For this purpose, we first synthesize the main circuit without the assertions and obtain the maximum clock frequency, power, and area reports. Later, the original circuit and the bound assertions is once again synthesized. At this point, the assertion goes from a verification asset to an embedded online checker. Finally, these results of the two syntheses are compared to evaluate the performance of the assertions.

C. Security Coverage

Despite having information about the performance results for each assertion, we cannot still reach a complete decision

| Name | Assertion definition |
|------|----------------------|
| ASR_1 | assert always {(!IR == OP_STORE) -> (!wr)}; |
| ASR_2 | assert always {IR == OP_STORE -> (wr)}; |
| ASR_3 | assert always {(!IR == OP_READ) -> (!rd)}; |
| ASR_4 | assert always {IR == OP_READ -> (rd)}; |

Table I: Considered assertions for detecting Trojans on B19-T500 benchmark.
regarding the effectiveness of a given assertion. In other words, although we know exactly the cost of these assertions, we are not aware of what we achieve. So, a new evaluation scheme is needed to build a trade-off between the costs and the achievements. In this sense, we propose a new metric for the assessment of the assertions considering the security properties. The general idea is to synthesize the original design along with the assertion circuit and check if there are any functional paths from the individual nodes in the main design to the output of the assertion circuit. Cadence JasperGold Security Path Verification (SPV), our tool of choice, performs proofs to find the existence of functional paths between the design nodes and the assertion outputs, and existence of such paths means that the origin nodes are covered by the assertion. Therefore, if the origin node in the design is the location of the payload of a Trojan, an assertion that can be reached by that node can detect the malicious logic. A higher number of nodes reachable from the original circuit to the assertion output represents better coverage in Trojan detection for that assertion. Based on these explanations, we define our security coverage metric as follows:

\[
\text{Security Coverage} = \frac{\text{Number of reachable nodes}}{\text{Number of total nodes}}
\] (1)

To obtain the security coverage for each assertion, first, the circuit is synthesized while the assertion is bound to it. Then, all the nodes in the synthesized netlist have to be extracted for further analysis. For this purpose, a tool is developed which receives a netlist as an input and generates a list containing all nodes inside it. This list is then submitted to SPV. This tool is mainly used to check if a part of a design is securely isolated from the other parts, usually referred to as taint analysis (e.g., test if features of a processor should not be accessible except in the test mode), but with some changes in its initial configuration, it can be utilized to calculate the security coverage we need. For this aim, we create a list of pairs of nodes in the format origin, destination, where all nodes in the circuit are possible origin nodes and a destination node is the output of an assertion. Then, the list of pairs of nodes is fed into the SPV tool to check if there is a functional path between them. In this stage, the inner engines of the SPV tool create properties for each pair and try to prove that there is no functional path for the property or to provide some counterexamples for the opposite condition. After finishing the analysis, the security coverage can be calculated using equation (1). A Tool Command Language (TCL) script is used to automate the process.

Now, the needed information for evaluating the effectiveness of the assertions can be taken into account for qualifying them regarding the security aspects. The security coverage can be utilized to drive a trade-off analysis and help the user to decide which assertions are suitable for his/her purposes. It should be noted that not all the circuits need 100% of security coverage; for example, if some sensitive parts of the circuit are already identified and are the only parts needed to be secured, covering those parts is sufficient to satisfy the user demands.

III. OpenTitan - A Case Study

In the previous section, we studied our own defined assertions to prove that they can detect Trojans and be seen as security checkers. But, this practice is hard to generalize: writing such top-level assertions is significantly time-consuming and hard to achieve. Moreover, the main contribution of this work is precisely to reuse the assertions that already exist for verification purposes, instead of generating new ones. Hence, in this section we study the evaluation of different assertions written for verifying the OpenTitan System-on-Chip (SoC) [20], to check if they can be used as security checkers.

OpenTitan is an open-source project consisting of a RISC-V-based processor and IPs from different vendors [20]. It also includes functional assertions for different Intellectual Properties (IPs) which makes it a remarkable candidate for our study.

For this purpose, the Register Top modules of each IP are chosen. This module controls the transactions between the IP and the bus, and is responsible for granting access to read/write requests for IP registers. Moreover, it has a unique error generation mechanism for writes and reads that target addresses that are not represented within the register list [20]. Since the Register Top modules of different IPs include the same assertions, it provides a good comparison among the experiments. A set of selected assertions is shown in Table I.

In total, 108 different assertions are studied on 35 individual IPs in OpenTitan SoC to demonstrate that the obtained results are comparable to a realistic example and our approach is scalable to industry-size circuits.

To obtain the security coverage of each assertion, the same flow as explained in the previous section is used: MBAC translation, assertion binding, and then synthesis. Finally, the nodes from the synthesized netlist are fed into the SPV tool to calculate the security coverage.

IV. Optimizing the Assertion List

Manually checking the assertions to see if they are top-level or not is a very time-consuming process and it questions the efficiency of the proposed approach. Hence, a decision flow is needed to wisely choose the assertions suitable for the security aims. For this purpose, we present a methodology to help the user only pick efficient security checkers from the available assertions based on his/her needs. This is a necessary step since all the functional assertions are not suitable for security purposes. The overall flow of this methodology is shown in Fig. I. The first step is to create a list of candidates containing the assertions which can be recognized to be synthesized along with the original circuit, and pick one. Then it has to be converted to a synthesizable format (step 2) to be bound to the main design (step 3). After the synthesis process, different

\[1\] A functional path is one that can be exercised with a combination of valid inputs. This is in contrast with structural paths or timed paths (STA) that might not be reachable.

\[2\] Some assertions have simulation-based nature and cannot be synthesized (i.e., assertions checking whether a signal is X or not).
performance reports are generated to help the user decide if the overheads are acceptable or not (step 4). The margin threshold for the overheads can be defined by the user based on his/her needs, and if the overheads for the selected assertion go beyond the defined boundaries, that assertion is put away and another one is picked from the candidate list. Otherwise, the circuit nodes are extracted and fed into the SPV tool to obtain security coverage (step 5). Finally, the user can decide to add this assertion to the security checker list based on the trade-off between the overheads and the security coverage or to select another one from the candidate list.

A. Optimization flow for selecting the assertions

In this part, we choose Alert Handler IP from the OpenTitan SoC [20], which contains several assertions and we show how to form a list of security checkers among these assertions. At the first step, a candidate list including 13 different assertions is created. These assertions are predefined by the OpenTitan developers and their main objective is to make sure that the functionality of the circuit will remain the same as its intent. Since the final security checker list is defined based on the user needs, we defined two different strategies for selecting the appropriate candidates: fixed-threshold and dynamic-threshold strategies. It should be noted that defining the strategies is completely flexible and depends on the amount of security needed in the cost of performance reduction. In the following, we explain the proposed optimization flow for our defined strategies.

Fixed-threshold strategy: If the maximum performance overhead for each assertion is X (percent), the security coverage should be at least 10X (percent).

This strategy defines fixed thresholds for the overheads and/or security coverage of each assertion, and removes the assertions that violate these thresholds from the candidate list. To follow the strategy rules, different overheads of each assertion should be obtained first, and after calculating the security coverage, the maximum overhead (area, power, or timing) goes under comparison. Based on this strategy, only 2 out of 13 assertions of the Alert Handler IP are removed from the candidate list.

Dynamic-threshold strategy: The maximum performance overhead for each assertion should not exceed twice the average performance overheads. For the security coverage, we only pick those assertions that have a positive impact on the overall coverage of the circuit compared to other assertions.

In contrast to the previous strategy, where assertions are assessed individually, the dynamic strategy performs comparisons between competing assertions. We follow the same procedure to obtain the performance overheads for the first condition of this strategy, but by looking at the security coverage results for individual assertions, no information can be obtained regarding the positive impact of the assertions. Instead, this strategy selects only assertions that fare better than average.

The first strategy, while simple and easy to implement, requires the user to define a constant (10) for the threshold. The second strategy requires no such constant, but a sufficient number of assertions is needed for defining what average overhead and coverage look like. More details are provided in the next section, where we show how the dynamic strategy can be more effective than its fixed threshold counterpart. Nevertheless, more convoluted strategies can be defined and this remains as future work.

V. EXPERIMENTAL RESULTS

In this section, we present experimental results including performance overheads and security coverage obtained for different circuits as explained in previous sections. For all experiments reported here, we have used Cadence Genus and our target cell library is a commercial 65nm library.

A. B19-T500 benchmark from Trust-Hub

Fig. 2 shows the normalized numbers of timing, power, and area overheads for the assertions considered for the B19-T500 benchmark. As shown in this figure, while the area overhead

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### TABLE II

| Assertion name | Assertion definition |
|----------------|----------------------|
| **wePulse**    | assert property (@(posedge clk_i) disable iff (!rst_ni) !== 1'b0) $rose(reg_we) |=> !(reg_we)); |
| **rePulse**    | assert property (@(posedge clk_i) disable iff (!rst_ni) !== 1'b0) $rose(reg_re) |=> !(reg_re)); |
| **reAfterRv**  | assert property (@(posedge clk_i) disable iff (!rst_ni) !== 1'b0) $rose(reg_re || reg_we) |=> tl_o); |
| **en2addrHit** | assert property (@(posedge clk_i) disable iff (!rst_ni) !== 1'b0) ((reg_we || reg_re) |-> $onehot0(addr_hit))); |
for three of the assertions (ASR_1, ASR_2, and ASR_4) is zero, the maximum overheads belong to ASR_2 and ASR_1 respectively, which consume approximately 9% more power than the original circuit. Also, the timing overhead is less than 6% for all of the assertions. It should be noted that the normalized numbers lower than 1 are within the noise margin of the circuit and do not have any effect on the performance.

Table III shows the security coverage calculated for the same assertions in the B19-T500 benchmark. As shown in this table, our assertions cover on average 6.8% of the total nodes in the circuit, which means that they can catch the Trojans in their covered areas, regardless of how rare the Trojans are triggered and what impacts they would cause to the circuit. This is one of the main advantages of our method such that the user has no more to be concerned about activating the rare Trojans.

B. OpenTitan SoC

Fig. 3 depicts the security coverage obtained for different IP Register Top modules of OpenTitan SoC. As shown in this figure, the highest number for security coverage is 4.77% for the nmi_gen_reg_top module, and the security coverage percentage for the majority of IPs is less than 1, which does not represent a good candidate for being a security checker. This is mainly because these types of assertions are only performing small interface checks, and do not satisfy the condition of describing the top-level behavior of the circuit. Instead, they only cover some local nodes which leads to a low security coverage for the whole circuit nodes. This justifies the need for the optimization step in our proposed methodology to avoid selecting unnecessary assertions that do not have a considerable impact on Trojan detection.

C. Selecting the Assertions

In this part, we present a practical experiment using the optimization flow as shown in Fig. 1. We defined two strategies for selecting the proper assertions in Section IV, and in the following, we provide more details about the procedure of assertion selection.

| Assertion name | Total nodes | Covered nodes | Security Coverage (%) |
|----------------|-------------|---------------|-----------------------|
| ASR_1          | 5014        | 315           | 6.28 (%)              |
| ASR_2          | 5062        | 304           | 6.01 (%)              |
| ASR_3          | 4916        | 367           | 7.47 (%)              |
| ASR_4          | 4944        | 369           | 7.46 (%)              |
| Average        | 4984        | 339           | 6.80 (%)              |

Fixed-threshold strategy: The performance results for the assertion candidate list are shown in Fig. 4. As shown in this figure, the maximum number for the overheads belongs to timing degradation of ah_asr_8 assertion (2.99%), while the minimum overhead belongs to ah_asr_3 and ah_asr_4 assertions with the number of 0.75%. At the next step, they should be checked for the security coverage which makes it to be at least 10 times higher than the maximum overhead for each assertion. Fig. 5 shows the security coverage results obtained from each assertion using the SPV tool. For better understanding, we simply associated numbers with the assertion names. Based on these results, we can ignore the ah_asr_12, and ah_asr_13 since they do not satisfy the required security coverage condition and consider the other candidates as the final security checkers. Although 15% of the assertions were removed based on this strategy, defining smarter strategies can enhance the effectiveness of the final list. Hence, second strategy is defined on the same candidate list for achieving more efficiency.

Dynamic-threshold strategy: For the first condition of this strategy, we should calculate the average overhead for all the assertions which is 1.79%. Hence, all the candidates are passed since they have less than twice the average overhead in all the cases (Fig. 4). But for the second condition, it is not sufficient to refer to the security coverage results since they do not have any notion of comparison to each other. Hence, an extra step is required to select the security checkers. For this purpose, we organize the assertions from the highest security coverage (ah_asr_11) to the lowest one (ah_asr_12). Starting from the ah_asr_11, we add the assertion with the next highest number (ah_asr_10 in the first round) and calculate the security coverage for the new set of assertions we made. Then, the next highest number is added to the existing set, and this process is repeated until the lowest number is added to the list.

Fig. 6 represents the security coverage numbers for each set of assertions. We include the assertion numbers in naming the set of assertions to identify the effect of added assertion in each step. For example, ah_asr_11_10 represents a set of assertions that starts from ah_asr_11 (the highest coverage) and ends with ah_asr_10 (the last assertion added to the list), and ah_asr_11_9 includes the assertions ah_asr_11, ah_asr_10, and ah_asr_9. Furthermore, a moving average trend-line is
added to this figure to help for choosing the best assertions. Since the period of the moving average trend-line is 2, it can make a good comparison between the security coverage of the newly added assertion in each stage, and the number for the two previous assertions. Therefore, if the security coverage obtained after adding an assertion crosses the moving average trend, it can be realized that a noticeable difference has happened. Returning to the second condition of Strategy 2 and from Fig. 6, we can see that security coverage numbers of only three assertions have crossed the moving average trendline ($ah_{asr\_5}, ah_{asr\_7},$ and $ah_{asr\_13}$). Hence, they can be added to the final list. Moreover, the $ah_{asr\_11}$ assertion is added to the final list since it has the highest security coverage.

In contrast with the results of the Register Top modules of different IPs (Fig. 7), the security coverage numbers of different assertions in Alert Handler IP are relatively higher (Fig. 5). This is mainly because the assertions written for this specific IP are describing a top-level behavior of the design, rather than checking only local signals and interfaces.

As shown in these two examples, different strategies can be defined based on user needs which makes the presented approach flexible. Moreover, one of the advantages of our work comparing with the current approaches is the simplicity of using it without complex procedures. For example, the presented work in [10] supports Trojan detection with flexible overheads, but it requires a lot of effort and complicated steps. In contrast, we use commercial tools that are available to the community, thus increasing the portability and scalability of the presented work.

VI. CONCLUSION

In this paper, we presented a new methodology for using verification assertions as security checkers. The security coverage, our proposed metric for assessing the effectiveness of assertions in Trojan detection, abstracts the notion of a Trojan trigger and focuses on the effect of the payload.

We examined our methodology on case studies from the Trust-Hub benchmarks and the OpenTitan SoC with more than 100 assertions to show the scalability of our work for the industry-size circuits. Moreover, we showed how defining a smart strategy can enhance the assertion selection process. In the future, we will focus on automating these strategies to enhance the current methodology.

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