Depth Optimized Ansatz Circuit in QAOA for Max-Cut

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Abstract

While a Quantum Approximate Optimization Algorithm (QAOA) is intended to provide a quantum advantage in finding approximate solutions to combinatorial optimization problems, noise in the system is a hurdle in exploiting its full potential. Several error mitigation techniques have been studied to lessen the effect of noise on this algorithm. Recently, Majumdar et al. proposed a Depth First Search (DFS) based method to reduce \(n - 1\) CNOT gates in the ansatz design of QAOA for finding Max-Cut in a graph \(G = (V, E), |V| = n\). However, this method tends to increase the depth of the circuit, making it more prone to relaxation error. The depth of the circuit is proportional to the height of the DFS tree, which can be \(n - 1\) in the worst case. In this paper, we propose an \(O(\Delta \cdot n^2)\) greedy heuristic algorithm, where \(\Delta\) is the maximum degree of the graph, that finds a spanning tree of lower height, thus reducing the overall depth of the circuit while still retaining the \(n - 1\) reduction in the number of CNOT gates needed in the ansatz. We numerically show that this algorithm achieves \(\simeq 10\) times increase in the probability of success for each iteration of QAOA for Max-Cut. We further show that although the average depth of the circuit produced by this heuristic algorithm still grows linearly with \(n\), our algorithm reduces the slope of the linear increase from \(\simeq 1\) to \(\simeq 0.11\).

Keywords: QAOA, Max-Cut, depth of circuit, CNOT

1 Introduction

Quantum Approximate Optimization Algorithm (QAOA) \(^1\) is a hybrid quantum-classical algorithm \(^2\), studied primarily for finding an approximate solution to combinatorial optimization problems. A QAOA is characterized by a Problem Hamiltonian \(H_P\) that encodes the combinatorial optimization problem, and a Mixer Hamiltonian \(H_M\) that anti-commutes with \(H_P\) and whose ground state is easy to prepare. Two parameterized unitaries \(U(H_P, \gamma) = \exp(-i\gamma H_P)\) and \(U(H_M, \beta) = \exp(-i\beta H_M)\) are applied sequentially for \(p \geq 1\) times on the initial state \(|\psi_0\rangle\). Here \(\gamma = \{\gamma_1, \gamma_2, \ldots, \gamma_p\}\) and \(\beta = \{\beta_1, \beta_2, \ldots, \beta_p\}\), \(\gamma_i, \beta_i \in \mathbb{R}\) \(\forall i\), are the parameters. A single epoch of a level-\(p\) QAOA is represented as in Eq. \(^1\).

\[
|\psi(\gamma, \beta)\rangle = (\Pi_{l=1}^p e^{-i\beta_l H_M}) e^{-i\gamma_l H_P} |\psi_0\rangle
\]  \(\text{(1)}\)

The parameters are initialized randomly, and after an epoch of iterations, that provides the expectation value \(\langle \psi(\gamma, \beta) | H_P | \psi(\gamma, \beta) \rangle\), the parameters are updated by a classical optimizer. The next epoch uses this new set of parameters and is expected to provide an expectation value that is closer to the optimum solution to the problem.

Farhi et al. first proposed QAOA \(^1\), and studied it in the context of finding a maximum cut in a graph, known as the Max-Cut problem. For 3-regular graphs, they showed that a \(p = 1\) QAOA achieves an approximation ratio better than random guessing, but lower than the best known classical algorithm \(^3\). They also argued that the expectation value of the cut produced by the algorithm is a non-decreasing function of \(p\). Therefore, QAOA is expected to be a potential candidate for quantum advantage using near-term devices. Many researchers, since then, have studied QAOA in the context of the Max-Cut problem \(^4\)\(^9\).

A recent experiment from Google \(^10\) showed that noise overwhelmed QAOA for Max-Cut in current quantum devices, and the expectation value produced by the algorithm decreases beyond \(p = 3\). Error
mitigation processes have been studied in the literature that lowers the effect of noise on QAOA, or in general on hybrid quantum-classical algorithms \[ 11,13 \]. Apart from error mitigation techniques, variation in the Mixer Hamiltonian \[ 7 \], or the Cost Function \[ 6,14 \] have been proposed that either lowers the noise in the circuit, or achieves faster convergence, thus reducing the depth, and hence the effect of decoherence, of the circuit.

In \[ 7 \], Majumdar et al. proposed a Depth First Search (DFS) based method that can eliminate \( n - 1 \) CNOT gates in the circuit of QAOA Max-Cut for any graph \( G = (V, E) \), where \( |V| = n \). Since CNOT gates are one of the primary sources of error in modern quantum devices \[ 15 \], this procedure significantly reduces the noise in the circuit. As this method imposes an ordering of the edges (discussed in detail in Sec. 2), there is an increase in the depth of the circuit. The authors, however, proved that this increase in depth is overshadowed by the reduction in CNOT gates, and the overall circuit has a lower probability of error. Nevertheless, a graph has multiple DFS trees, and the depth of the circuit varies with the height of a DFS tree for the given graph. A circuit with lower depth is naturally preferable with effect of decoherence being lower.

1.1 Contributions of this article

It is not a trivial task to find a DFS tree for a given graph that is guaranteed to provide a low depth ansatz circuit. Further, a circuit tree with lower height does not necessarily result in a lower depth circuit (see Sec. 3). In this paper, we propose a greedy heuristic algorithm to lower the depth of the circuit while still eliminating \( n - 1 \) CNOT gates. The run-time of our proposed algorithm is \( \mathcal{O}(\Delta \cdot n^2) \), where \( \Delta \) is the maximum degree of the graph, and it reduces the depth of the circuit by \( \simeq 84.8\% \) for graphs with number of vertices \( n = 100 \). We show our results on Erdos-Renyi Graphs with the probability of edge varying from 0.4 - 0.8, and complete graphs. For graphs with \( 4 \leq n \leq 12 \), we simulate our proposed heuristic with the ibmq_manhattan noise model, and show more than 10 times increase in the success probability of each iteration of QAOA for Max-Cut. The maximum height of the DFS tree (and hence the depth of the circuit) can be \( n - 1 \), i.e., it increases linearly with the number of vertices with a slope of \( \simeq 1 \). We show that the increase in depth of the circuit with the number of vertices from our method is still linear, the slope is reduced to \( \simeq 0.11 \).

In the rest of the paper, Sec. 2 gives a brief review of QAOA for Max-Cut and the DFS based optimization proposed in \[ 9 \]. In Sec. 3 and Sec. 4 we respectively provide the conditions that lead to a low depth circuit, and a corresponding greedy heuristic algorithm to achieve a low depth. Sec. 5 presents the simulation results of this proposed algorithm, and the concluding remarks appear in Sec. 6.

2 QAOA for Max-Cut and DFS based ansatz optimization

2.1 QAOA for Max-Cut

The traditional QAOA ansatz (the parameterized circuit) is composed of the two parameterized unitaries \( U(H_P, \gamma) \) and \( U(H_M, \beta) \). Given a graph \( G = (V, E) \), with \( |V| = n \), the circuit is initialized in the equal superposition of \( n \) qubits. This initialization step has a depth of 1 (simultaneous operations of Hadamard gate on all qubits). Similarly, the circuit realization of \( U(H_M, \beta) \) is a simultaneous operation of \( R_X(\beta) \) on all the qubits.

The operator \( U(H_P, \gamma) \) depends on the Problem Hamiltonian. For the Max-Cut problem, \( H_P = \sum_{(j,k)\in E} \frac{1}{2}(I - Z_jZ_k) \). The operator \( U(H_P, \gamma) \) can, therefore, be represented as in Eq. (2).

\[
U(H_P, \gamma) = \Pi_{(j,k)\in E} U(H_P^{(j,k)}) = \Pi_{(j,k)\in E} \exp(-i\gamma(\frac{I - Z_jZ_k}{2}))
\]

The circuit realization of the operator \( U(H_P^{(j,k)}) \) corresponding to an edge \((j,k)\) is shown in Fig. 1. In accordance to the nomenclature used in \[ 3 \], we call this circuit a step. More precisely, multiple simultaneous such operators can be executed in each step corresponding to disjoint edges. For example, in Fig. 2 the operators \( U(H_P^{(0,1)}) \) and \( U(H_P^{(2,3)}) \) are operated on simultaneously in the same step.
For the rest of the paper, the term QAOA will refer to the QAOA for the Max-Cut problem where the graph $G = (V, E)$ is connected, undirected, and unweighted, and $|V| = n$ and $|E| = m$. Every analysis, heuristic and algorithm in this paper will be applicable directly or with minimal changes to weighted graphs or graphs with multiple components. Furthermore, the term an edge is operated on, or its equivalent terms, would imply the operation of the circuit of Fig. 1 for that corresponding edge.

For the sake of completeness, in Fig. 2 we show the circuit for a $p = 1$ QAOA corresponding to a 2-regular graph with four vertices.

![Figure 2: QAOA circuit for $p = 1$ corresponding to a 2-regular graph with four vertices](image)

### 2.2 DFS based optimization of the ansatz circuit

We now briefly discuss the DFS based optimization method that was proposed in [9]. Given a graph $G = (V, E)$, this method finds a DFS tree $T$ starting from a randomly chosen root vertex $r$. The DFS tree is an acyclic subgraph of $G$ containing all the $n$ vertices and $n - 1$ edges. The QAOA circuit corresponding to $U(H_P, \gamma)$ can then be partitioned into two portions - the one with edges in $T$, and the other edges. The operators corresponding to the other edges, which are not included in the DFS tree, can be executed in any order once all the operators corresponding to the edges in $T$ are operated on.

For each edge $(u, v) \in T$, the operator $U(H_{e_{u,v}})$ is operated on maintaining the following conditions:

i) Starting from the root vertex $r$, if an edge $e_1$ appears earlier than another edge $e_2$ in the DFS tree $T$, then the operator $U(H_{e_1})$ must precede $U(H_{e_2})$ in the corresponding circuit.

ii) If an edge $e = (u, v)$ is included in $T$ and the vertex $u$ is incident on an edge already in $T$, then $u$ and $v$ must act as the control and target of the CNOT gate respectively in the operator $U(H_{e})$.

Majumdar et al. [9] proved that if these two conditions are satisfied, then the first CNOT gate for the operator in Fig. 1, associated with each edge in $T$ are operated on maintaining the following conditions:

Majumdar et al. [9] proved that if these two conditions are satisfied, then the first CNOT gate for the operator in Fig. 1, associated with each edge in $T$, can be removed while still retaining functional equivalence for $p = 1$ of the QAOA circuit. This optimization method does not hold for $p > 1$. Nevertheless, for any level $p$ QAOA, the first level can be thus optimized. Therefore, the DFS based method can reduce the CNOT count of the overall QAOA circuit by $n - 1$.

This method mandates a sequential ordering of the tree edges, i.e., an edge in $T$ can be operated only after operators for all of its ancestors have been applied. The maximum height of a DFS tree with $n$ vertices can be $n - 1$, thus leading to a significant increase in the depth of the circuit. Fig. 3 shows a 2-regular cycle with 6 vertices. In the traditional QAOA ansatz, the operator $U(H_P, \gamma)$ can be executed in 2 steps only. As indicated with the two colors in the graph of Fig. 3 (a), the edges assigned the same color can be operated on in the same step. The DFS based method on the other hand (the graph of Fig. 3 (b)) requires 6 steps. It is easy to verify that for a 2-regular cycle, the traditional QAOA ansatz always requires 2 (for even $n$) or 3 (for odd $n$) steps only, whereas the DFS based optimized circuit requires $O(n)$ steps. For large graphs, it is possible that the depth of the DFS based optimized circuit leads to an execution time greater than the coherence time of the hardware. Even when such a scenario does not occur, increase in depth makes the circuit more susceptible to decoherence. Therefore, although the authors in [9] showed that reduction in the number of CNOT gates in the ansatz overshadows the

![Figure 3: 2-regular cycle with 6 vertices](image)
increase in depth with respect to probability of error, a pertinent question is whether a DFS tree that reduces the depth of the circuit as well can be found efficiently.

(a) In the traditional QAOA ansatz edges corresponding to the same color can be operated on in the same step; the number of steps needed for this example is 2.

(b) In DFS tree based ansatz optimization — the number of CNOT gates can be reduced by 5, but the number of steps required is 6.

Figure 3: Steps of operation for $U(H_P, \gamma)$ for traditional QAOA ansatz and DFS based optimized one.

Note that this approach to optimizing the number of CNOT gates holds for any rooted spanning tree where the two conditions mentioned above, on the ordering of the tree edges, are met. DFS is merely a method to generate a rooted spanning tree of a graph. Henceforth, instead of specifically finding the DFS tree, we focus on finding a rooted spanning tree for a graph $G$ which serves the above purpose.

3 Formulation of the Ansatz Optimization Problem

Here we focus only on optimizing for the operator $U(H_P)$ associated with each edge because each of the circuits for initialization and the Mixer Hamiltonian having a depth of one, is the same as for the traditional QAOA circuit [1], or for the optimized circuit in [9]. Henceforth, when we mention a circuit, or its depth, we refer to the circuit corresponding to the operator $U(H_P)$ only.

The maximum height of a DFS tree with $n$ vertices is $n - 1$, and so is the depth of the corresponding circuit. It may be claimed that a spanning tree with lower height can lead to a circuit with lower depth. In such a case, a Breadth First Search (BFS) tree may provide a spanning tree with minimum height. However, the two trees shown in Fig.4(a) and (b) have different heights leading to the same depth of the circuit. In both the figures, the values associated with the edges depict the level at which the operator corresponding to that particular edge can be operated on so that the optimization (i.e. reducing the number of CNOT gates) holds. The circuit corresponding to both of the trees, shown in Fig. 5, is the same. These two trees and their corresponding circuit readily show that simply reducing the height of the tree is not sufficient to obtain a circuit of lower depth. Therefore, finding a BFS tree instead of a DFS tree does not guarantee a circuit with lower depth.

Figure 4: Two trees with different heights – the integer label on an edge is the step at which the operator $U(H_P)$ for that edge can be operated on. The maximum value of these labels is the depth of the circuit. The heights of the trees in subfigures (a) and (b) are 3 and 2 respectively. However, both of them lead to the same circuit shown in Fig. 5.
The reason why the tree on the right hand side with height 2 in Fig. 4 cannot lower the depth of the circuit is because the CNOT gates corresponding to two adjacent edges cannot operate at the same step. Therefore, simply reducing the height of the spanning tree is not sufficient to reduce the depth of the circuit. Furthermore, in Fig. 6 we show two trees with the same height, but having circuits of different depth, as evident from the level number attached with the edges.

We now define a few terms to easily clarify the requirements for a rooted spanning tree that will lead to a circuit with lower depth.

1. **Branching Factor**: The branching factor of a vertex $v$ is defined as the number of vertices that have been discovered in the rooted spanning tree from $v$.

   In other words, the branching factor of a vertex $v$ is one less than the degree of that vertex in the spanning tree except for the root vertex, whose branching factor is equal to its degree. For example, in the tree of Fig. 4 (b), starting from the root labelled 1, the branching factor of the root is 1, that of vertex 2 is 2, and that of the leaf vertices are 0.

2. **Level**: If a vertex $v$ is discovered in the rooted spanning tree from a vertex $u$, then the level of vertex $v = \text{level of vertex } u + 1$. The level of the root vertex is 0.

   The definition of level is essentially the same as that for BFS.

3. **Delayed Start**: Delayed start is defined as the phenomenon where the vertices $v_1, \ldots, v_k$ are discovered in the spanning tree from the same vertex $v$, and belong to the same level, but the edges $(v, v_1), \ldots, (v, v_k)$ have to be operated on sequentially. This is because the adjacent edges share a common vertex, and simultaneous CNOT operations are not possible with a common control or target qubit. Therefore, the operation corresponding to the edge $(v, v_i)$ is delayed as long as all the operations corresponding to the edges $(v, v_j), 1 \leq j < i$ are not completed. The operator $U(H_{P(v,v_i)})$ can be operated earliest at the level level$(v) + i$.

   We see an example of delayed start in the tree of Fig. 4 (b). Although both the leaf vertices in that tree are in the same level, they cannot be operated on simultaneously. Therefore, they must be operated on two disjoint levels. Indeed delayed start is the reason that the depth of the circuit does not reduce directly with the height of the tree. It is obvious that a tree with a higher branching factor can
experience more delayed start than a tree with a lower branching factor. On the other hand, the height of the tree increases with decreasing branching factor. Therefore, we need a spanning tree starting from a root vertex \( r \) that has as few delayed starts as possible. This rooted spanning tree is neither a DFS tree that has low branching factor, nor a BFS tree that has low height. It is, rather, a tree that has a trade-off between the branching factor (and hence delayed start) and the height.

### 3.1 Conjecture: The problem is NP-Complete

We have seen that simply finding a rooted spanning tree with minimum height is not sufficient to reduce the depth of the corresponding circuit. What we need instead is to have edges that can be executed in parallel. This is similar to the Edge Coloring problem \[16\]. Edges having the same color are disjoint and can be executed in parallel. This method was exploited in \[9\] as well. However, the problem here is more constrained than the Edge Coloring problem. In a tree, the same color can be used for edges in alternate levels, i.e., it is possible to have edges of same color in level 1, level 3 etc., and in level 2, level 4 etc. For example, in Fig. 3(a), normal Edge Coloring assigns the same color to the edges in levels 1 and 3 since they are disjoint. However, we have already discussed that operators corresponding to these two edges cannot execute in parallel. Therefore, we have an added constraint that an edge cannot be given the color of any of its ancestors. We formally define the problem as follows:

**Problem 1.** Given a graph \( G = (V, E) \), starting from a root vertex \( r \) find a spanning tree \( T \) of \( G \) whose edges can be colored with the minimum number of colors satisfying the conditions that

i) No two edges incident on a common vertex have same color.

ii) No edge has same color as that of any of its ancestors.

Optimal Edge Coloring problem is itself an NP-Complete problem, and Problem 1 has additional constraints. In other words, we want that the degrees of the vertices in the spanning tree are not very large in order to avoid delayed start. Edges which are suffering from delayed start due to the rooted spanning tree ordering cannot have the same colors, and will thus increase the required number of colors. In \[17\], the authors showed that finding a degree constrained spanning tree, i.e., a spanning tree where the degree of any vertex is upper bounded by a predefined value, in NP-Complete.

Hence, we conjecture that Problem 1 is NP-Complete, and propose a greedy polynomial time algorithm to find a better solution instead of the vanilla flavour depth-first search based method.

### 4 Proposed Cost Function and Algorithm

We propose a cost function that respects the following observations:

i) If the branching factors of the vertices are very high, then the corresponding circuit will suffer from delayed start, leading to an increase in the depth. On the other hand, if the branching factor of the vertices are very low, then the height of the tree, and hence of the depth of the circuit, will increase.

ii) Between two vertices \( u \) and \( v \), it is better to branch the one at a lower level of the tree so that the edges in that branch may still have some opportunity to be executed in parallel with other edges at a higher level even after delayed start. An example of this is shown in Fig. 4 where both the trees have the same height, but the tree of Fig. 4 (b) will lead to a circuit with lower depth since the branching is closer to the root.

iii) For graphs with fewer vertices, the branching factor should be low in order to avoid increase in depth due to delayed start. However, as the number of vertices increases, a higher branching factor must be allowed to lower the height of the tree.

Respecting all the three criteria stated above, we propose a cost function \( C_v \) to be associated with every vertex \( v \). Let \( n \) be the number of vertices in the graph, \( l_v \) and \( v_{bf} \) be the level and the current branching factor of the vertex \( v \) respectively, and \( B \) be the maximum branching factor decided for any vertex in the spanning tree, then

\[
C_v = (n - l_v) \cdot (B - v_{bf})
\]  

(3)

When growing the spanning tree from a root vertex, the edge \((v, w)\) for which the cost function \( C_v \) is maximum, is added to the tree. Note here that for a new edge \((v, w)\), the cost function does not depend
on the vertex \( w \), but rather on the vertex \( v \) from which this edge is discovered (the algorithm is provided later on).

The term \((n - l_v)\) is always positive. On the other hand,

\[
B - v_{bf} \begin{cases} 
> 0 & \text{if } v_{bf} < B \\
= 0 & \text{if } v_{bf} = B \\
< 0 & \text{if } v_{bf} > B.
\end{cases}
\]

Our proposed algorithm avoids branching at a vertex for which \( v_{bf} \geq B \). In fact, when \( v_{bf} = B \),

the cost function has a contribution of 0. Therefore, in our result section, we take

\( B = f + 1 \) if we want a maximum branching factor of \( f \) in the spanning tree. Furthermore, the term \((n - l_v)\) is higher for the vertices with lower \( l_v \). Thus, if for two vertices \( u \neq v \), \( v_{bf} = u_{bf} < B \), the algorithm chooses

to branch that vertex which has a lower level. This ensures that delayed start is closer to the root, so that those branches still have some opportunity for parallel execution with some higher level branches. Furthermore, if \( v_{bf} > B \), the product with \((n - l_v)\) leads to significantly low values for low \( l_v \). This discourages branching more than \( B \) in lower levels of the tree strongly to prevent excessive delayed start (like in a BFS tree). In other words, the spanning tree generated by this heuristic cost function is neither a BFS nor a DFS one, but rather an intermediate one. Algorithm 1 presents how to generate a spanning tree that has a trade-off between the height of the tree and the branching factor.

**Algorithm 1** Cost Function Based Rooted Spanning Tree Generation

**Input:** A Graph \( G = (V, E) \), \(|V| = n, |E| = m\); maximum branching factor \( B \).

**Output:** A Rooted Spanning Tree \( T \) of the Graph \( G \).

1. \( T = \{\} \).
2. \( u_{bf} \leftarrow 0 \) for all vertex \( u \).
3. \( r \leftarrow \) randomly selected start vertex.
4. \( \text{Visited} = \{r\} \).
5. \( r_{bf} = r_{bf} + 1 \).
6. \( \text{edges\_to\_add} = \text{neigh}(r) \).
7. \( \text{while} \ |\text{Visited}| < n \ \text{do} \)
8. \( e = \text{edges\_to\_add}[0] \).
9. \( c = 0 \).
10. \( \text{for all} \ edge = (u, v) \in \text{edges\_to\_add} \text{ do} \)
11. \( \text{cost} = (n - l_u) \cdot (B - u_{bf}) \).
12. \( \text{if} \ cost > c \ \text{then} \)
13. \( c = \text{cost} \).
14. \( e = \text{edge} \).
15. \( \text{end if} \)
16. \( \text{end for} \)
17. \( T = T \cup \{e\} \).
18. \( \text{Visited} = \text{Visited} \cup \{y\}, \text{ where } e = (x, y) \).
19. \( x_{bf} = x_{bf} + 1 \).
20. \( \text{Remove all edges of the form } (\ast, q) \text{ from } \text{edges\_to\_add} \).
21. \( \text{for all} \ edge = (p, q) \in \text{neigh}(y) \ \text{do} \)
22. \( \text{if} \ q \notin \text{Visited} \ \text{then} \)
23. \( \text{edges\_to\_add} = \text{edges\_to\_add} \cup \{edge\} \).
24. \( \text{end if} \)
25. \( \text{end for} \)
26. \( \text{end while} \)

**Lemma 2.** Algorithm 1 finds a rooted spanning tree in \( O(\Delta \cdot n^2) \) time for a graph with \( n \) vertices and maximum degree \( \Delta \) which satisfies the conditions in Problem 1.

**Proof.** Let \( r \) be the randomly chosen root vertex of the spanning tree. Therefore, the choice of root does not require any computational time. Since \( \Delta \) is the maximum degree of the graph, \( r \) can have at most \( \Delta \) neighbours. Finding the maximum cost function among these neighbours require \( O(\Delta) \) time. Subsequent vertices in the spanning tree can have at most \( \Delta - 1 \) neighbours since one of its neighbour
must be its parent in the spanning tree. Therefore, the total time requirement in all the steps is

\[ W \leq \Delta \] (to create the spanning tree upto two vertices)
\[ \leq \Delta + (\Delta - 1) \] (to create the spanning tree upto three vertices)
\[ \leq 3\Delta - 2 \] (to create the spanning tree upto four vertices)
\[ \vdots \]

Therefore,

\[ W \leq \sum_{i=1}^{n-1} (i \cdot \Delta - (i - 1)) \]
\[ = \Delta \cdot \sum_{i=1}^{n-1} i - \sum_{i=1}^{n-1} (i - 1) \]
\[ = O(\Delta \cdot n^2) \]

For sparse graphs, \( \Delta = O(1) \) and for dense graphs \( \Delta = O(n) \). Therefore, the time complexity of the proposed Algorithm 1 varies between \( O(n^2) \) to \( O(n^3) \) depending on the sparsity of the given graph.

### 4.1 An Illustration of Algorithm 1

We illustrate the DFS method 9 and our proposed method in action on an example graph given in Fig. 7. First, in Fig. 8 we show the traditional \( p = 1 \) QAOA circuit for this graph. Then, in Fig. 9 we give two spanning trees of the graph. The spanning tree in Fig. 9 (a) is generated using the DFS method 9, whereas the one in Fig. 9 (b) is generated using Algorithm 1 with \( B = 3 \). In Fig. 10 (a) and (b) we show the optimized circuits for the \( p = 1 \) QAOA of the graph in Fig. 7 where the optimized circuits are generated using the DFS method 9 and Algorithm 1 respectively. The values of \( \gamma \) and \( \beta \) are randomly selected.

![Figure 7: An example graph with 6 vertices](image)

![Figure 8: Traditional \( p = 1 \) QAOA circuit corresponding to \( U(H_P, \gamma) \) for the graph in Fig. 7](image)

The depth of the circuits in Fig. 8, Fig. 10 (a) and Fig. 10 (b) are 11, 14 and 12 respectively as obtained using the \texttt{depth()} function of Qiskit 18. The number of CNOT gates in both the optimized
Figure 9: Two spanning trees of the graph in Fig. 7. The left graph is generated using the DFS method, and the right one is generated using Algorithm 1 with $B = 3$.

Figure 10: Optimized $p = 1$ QAOA circuit corresponding to $U(H_P, \gamma)$ for the two spanning trees in Fig. 7 respectively.

circuits in Fig. 10 are 5 less than that in Fig. 8. We note that the depth of both the optimized circuits are greater than that of the traditional QAOA. However, the optimized circuit in Fig. 10 (b) can be considered to be superior since it requires 5 CNOT gates fewer than that in Fig. 8 as well as increases the depth by 1 only. In Sec. 5 we show that our proposed Algorithm 1 can significantly arrest the increase in depth, and in some cases can lead to a lower depth than its traditional circuit.

5 Results of simulation

5.1 Reduction in the depth of the circuit

The entire circuit of $U(H_P, \gamma)$ can be divided into two disjoint parts - one corresponding to the edges in the spanning tree, followed by the other edges in the input graph. Our algorithm can reduce the depth of the circuit corresponding to the spanning tree only. The circuit for the unoptimized edges remains the same as in [9]. Furthermore, the initialization, and the Mixer Hamiltonian is the same for the traditional QAOA circuit [1] or the circuit proposed in [9], and our proposed optimized circuit. Therefore, here we compare the depth of the circuit corresponding to the spanning tree only.

When executing a circuit in a hardware, the graph has to be mapped to the underlying hardware connectivity graph. This process is called transpilation. All the results in this section are generated after transpiling the original circuit in the `ibmq_manhattan` connectivity graph using the transpilation procedure of qiskit [18] with optimization_level = 3.

In the worst case, the height of the DFS tree, and hence the depth of the corresponding circuit, can be as large as $n - 1$. In Fig. 11 (a)-(d) we show the reduction in depth of of the circuit of the spanning tree by our proposed algorithm compared to the worst case depth of the circuit corresponding to the maximum height of the DFS tree. Fig. 11 (a)-(d) show the reduction in depth for Erdos-Renyi graphs with $p_{edge}$, the probability of an edge, varying from 0.4 to 0.8, and complete graphs. For each type of graph, we vary $n$, the number of vertices from 20 to 100, and the value of the depth corresponding to each $n$ is an average over 80 graph instances. The graph instances are same for all the values of $B$. The graphs in Fig. 11 and later in Fig. 12 are averaged over all the possible $n$ spanning trees generated by selecting each of the $n$ vertices once as the root.
For all the types of graphs considered, we observe higher reduction in the depth for a higher value of \( B \) as the number of vertices increases. This is at par with our reasoning earlier, that for larger graphs, it is better to allow higher values of \( B \). We have shown results for \( B = 3, 6 \) and 10 only. For \( B = 10 \) and \( n = 100 \), the reduction in the depth is \( \simeq 84.8\% \). It is evident from the graphs that the depth decreases with increasing \( B \) as the number of vertices increases. So for larger graphs, one should opt for even higher values of \( B \).

![Graphs showing depth of circuit for different values of \( B \).](image)

We observe from the graphs in Fig. 11 that the increase in the depth with \( n \) for various values of \( B \) is still linear. In the worst case, where the depth is \( n - 1 \) for a graph with \( n \) vertices, the slope is \( \simeq 1 \). In Table 1 we show the slopes of the curves for \( B = 3, 6 \) and 10 for each of the graph family considered. From the values it is evident that the slope corresponding to the increase in depth is lowered by \( \simeq \frac{1}{10} \) as the value of \( B \) increases.

| Graph Family     | \( B = 3 \) | \( B = 6 \) | \( B = 10 \) |
|------------------|-------------|-------------|--------------|
| Erdos Renyi (\( p_{\text{edge}} = 0.4 \)) | 0.35        | 0.1875      | 0.1125       |
| Erdos Renyi (\( p_{\text{edge}} = 0.6 \)) | 0.35        | 0.1875      | 0.1125       |
| Erdos Renyi (\( p_{\text{edge}} = 0.8 \)) | 0.3375      | 0.1875      | 0.125        |
| Complete graph   | 0.3375      | 0.1875      | 0.125        |

5.2 Increase in the Probability of Success

QAOA consists of executing the same circuit with the same parameters multiple times to obtain an expectation value of the cut. The performance of the algorithm is determined by this expectation value of the obtained cut. However, since our QAOA circuit, and the QAOA circuit in [9] are functionally equivalent to the traditional QAOA circuit, the performance remains unchanged. In this paper, we define success in a different way. For each iteration of the algorithm, let \( |\psi\rangle \) denote the ideal state vector obtained via noiseless simulation. As real-world quantum devices are noisy, let \( |\psi_e\rangle \) denote the noisy
outcome obtained via noisy simulation. We define the probability of success $P_{\text{success}} = |\langle \psi | \psi_e \rangle|^2$. For a graph with $n$ vertices, the optimization proposed in [9] reduced the number of CNOT gates by at most $n - 1$. Since a CNOT gate is one of the most acute sources of error, the method improved $P_{\text{success}}$. However, this improvement has the overhead of increase in the depth, which exposes the circuit to more decoherence. In this paper, we have retained the $n - 1$ reduction in the number of CNOT gates needed for the operator $U(H_P)$ in the ansatz and have also arrested the increase in depth to a bare minimum (refer Fig. 11 (a)-(d)). This leads to a further improvement in $P_{\text{success}}$.

![Graph plots](image1.png)

Figure 12: $1 - P_{\text{success}}$ for Erdos Renyi Graphs ($p_{\text{edge}} = 0.4, 0.6, 0.8$) and complete graphs

The plots corresponding to $P_{\text{success}}$ is somewhat indecipherable because the decrease in $P_{\text{success}}$ with increasing $n$ is significantly less in our method than the traditional QAOA or the optimization of [9]. Thus the changes are not easily observable in a plot for $P_{\text{success}}$. Therefore, in Fig. 12 (a)-(d) we plot $(1 - P_{\text{success}}) = 1 - |\langle \psi | \psi_e \rangle|^2$ for the four graph families using the `ibmq_manhattan` noise model for the noisy simulation. We show that our proposed method decreases $(1 - P_{\text{success}})$ by more than 10 times as compared to the traditional QAOA or the optimization in [9] for Erdos-Renyi graphs with $0.4 \leq p_{\text{edge}} \leq 0.8$ and complete graph.

We observe that in Fig. 12 (a)-(d), it is not evident that any betterment is achieved by increasing the value of $B$. However, this is simply because for graphs with low values of $n$, the maximum degrees are low as well. This is supported by similar results observed for low values of $n$ in Fig. 11 (a)-(d) as well. However, we see in those plots that as $n$ increases, increasing the value of $B$ leads to a better result. So we expect to see better results for $P_{\text{success}}$ as well with increasing value of $B$ as the number of vertices is increased further.

6 Conclusion

In [9] the authors showed that $n - 1$ CNOT gates can be omitted from the ansatz circuit of QAOA for Max-Cut for an $n$ vertex graph if a DFS based ordering is followed while constructing the circuit. However, this led to an increase in the depth of the resulting circuit. In this paper, we have proposed a polynomial time heuristic algorithm that can find a rooted spanning tree such that the reduction in the number of CNOT gates is retained while significantly arresting the increase in depth. Our method is able to reduce the increase in depth by $\simeq \frac{1}{10}$ as compared to the circuit in [9]. This, in its turn, leads...
to a significant increase in the success probability of the algorithm, since (i) the reduction in CNOT gates is retained, and (ii) the increase in depth is lowered thus making the circuit less susceptible to relaxation error. Our proposed heuristic for circuit synthesis is thus expected to provide a novel scheme for mitigating the effect of error in QAOA for Max-Cut, and can be used together with other error mitigation scheme.

Our results show that higher branching factor is better to arrest the increase in depth as the number of vertices increases. A future prospect can be to study an approximate value of the branching factor for a particular $n$ such that the increase in depth is minimum.

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