A clock synchronization method in power dispatching based on BeiDou navigation system

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Abstract — This paper introduces the problems of poor signal condition of a single time source in time synchronization or error in time source switching in the power system. It adopts the two-clock mode timing scheme of BeiDou 2 synchronous satellite and GPS synchronous satellite to ensure the stable output of the main clock within a certain accuracy. The system takes full advantage of the field programmable gate array (FPGA) hardware method, aligns the internal clock lock signal with the input second pulse phase, and proposes an improved method for the problem of large clock synchronization deviation based on the network, which proves the effectiveness and superiority of the system to accurately output the pulse and provide reliable time synchronization for the power dispatching system.

1. Introduction

The BeiDou Satellite Navigation System (BDS) refers to a global satellite navigation system that is being independently developed and operated by China. Together with the American Russian GPS and Galileo of the EU system, they are known as the four major satellite navigation systems in the world. The BeiDou Navigation provides continuous navigation, positioning and timing services since December 27, 2011. The BeiDou satellite navigation system consists of three parts: space end, ground end and user end. The space end includes 5 geostationary orbit satellites and 30 non-geostationary orbit satellites, and the ground end includes major control stations, injection stations, and monitoring stations. The user terminal consists of the BeiDou user terminal [1-3]. The BeiDou satellite system has the following advantages in timing over the US GPS system: it can provide better timing accuracy than the GPS system. The BeiDou navigation system has two one-way and two-way timing functions. Sync with BeiDou navigation according to different accuracy requirements.

2. Timing Principle and Method of BeiDou Navigation System

2.1. Operating principle of the BeiDou Satellite Navigation System

The timing of the BeiDou satellite system is realized by sending standard satellite time information and satellite location information from the ground central station. The specific process is: First, The ground center station first sends time marking information and DUT1 information to the user at the start frame time of each superframe, The time benchmark per frame of these time information maintains an accurate time synchronization relationship with the atoms; Secondly, When the user needs the rights, For different time information codes are demodulated by different users, In the response to the query signal simultaneously, Enables the user terminal to measure the false clock difference between the user clock and the center station clock through the time counter, The central
station may have the path delay of the standard clock reference signal sent to the user through the response signal information from different users, Digital digital sent to the user to correct false clock difference, Get the actual clock difference. After a series of actions, users can get accurate coordination of world time, adopt 220um BeiDou satellite/GPS dual-mode reception module to receive standby signals of BeiDou satellite and GPS satellite to ensure the stability of satellite signal and continuous and stable output of timing information. The synchronization time signal is obtained by receiving the GPRMC and BDRMC serial time information and 1pps-second pulse information sent by the satellite [4].

2.2. Timing method of BeiDou satellite navigation system

The BeiDou navigation system adopts the synchronous time matching mode in most cases:

(1) Serial port pair timing. It can also be called software timing, which refers to the serial message of the autonomous clock cycle, accepts the clock and decoding work, and analyzes the year, month, day, hour, minutes, seconds and other information.

(2) Pulse-pair timing. It can also be called a difficult data processing module for high-precision positioning and common time, respectively. The covisual data processing module calculates the covisual format data using the time difference measurement data and the original observation data, and it is sent to the data processing center through the communication module [5]. The data processing center combines the co-visual reference source data to calculate the local time deviation and return the time difference result to the reference station receiver. Controlling the internal frequency source and output from this difference produces synchronous, stable, accurate, and continuous standard time signals.

2.3. System function

The main functions of the power system timing equipment include the output of various time information, a stable second pulse output, a timing function, and a delay compensation function. This design mainly performs the following functions:

(1) Sufficient to receive the time information of the BeiDou 2 and GPS satellite systems;
(2) The system can output an accurate second pulse signal;
(3) The system can complete the coding and output of the unified target time code IRIG-B code;
(4) The system can output various forms of time codes, such as a serial port time message;
(5) On punctual effect of time signal when satellite fails;
(6) With the transmission delay compensation function;
(7) The timing accuracy can reach the nanosecond level, about 100ns

3. Hardware Design

The transmission delay system device is organically connected together by each module via the Avalon bus technology. The BeiDou receiving module receives the BeiDou/GPS information first. The output information includes time information and a second pulse signal, read and encoded via the UART serial port via the FPGA, and a second pulse alignment via the PLL phase-locked loop inside the FPGA [6]. The information output of the time information reading module is encoded to the IRIG-B encoding module, encoded by the modulus 100 counter and 10 counter generated by the FPGA itself, constantly generating an IRIG-B code composed of 10010ms elements. After each function completes its responsibilities, various time information is converted into the format required for the power system via the TTL level and RS232, RS485, fiber. This design adopts ALTERA company FPGA development board, EP2C8Q208C type, hardware system contains 420,000 equivalent doors, 64-bit SDRAM, 25MHz provides the system main clock, support download design program.

4. Decoding Process Design

Due to the superior actual performance of one frame, the completion time information conversion to B code becomes the preferred standard code for timing system devices (see Fig.1). The B code contains
three codes, the P high level pulse width 8ms, 1 high level pulse width 5ms, 0 high level pulse width 2ms. 0, 9, 19, 99 are index marker bits (P elements), the rising edge of the second element of two continuous index markers is the starting point of each frame, the second information occupies 1 to 8 bits, the segmentation information occupies 20 to 23, 25 to 27 bits when the segmentation information occupies 10 to 17 bits, the time information is expressed in the form of BCD code, front and back. The decoding of the B code is to read out the BCD code information in each frame into the time.

Fig.1 IRIG-B diagram

Fig.2 Decodes the flowchart
Firstly, the B code signal is filtered through 3 D triggers. To remove the possible spike signals, the pulse width within 10ms is then counted. 1 (01), 0 (00) and P(10) according to pulse width meter value. Then two P judgments, Create a high-level signal, Start the code element counter. Start the counting, The B code signal transmitted during this time is the time signal that we need to decode the output. When the counter counts to 99, The B code signal transmission time is exactly 1s(frame), Jump jump high level to low level, And reset the counter zero. For a second-plus-1 operation, And output the solved time information (can be seen Fig.2 for the specific process).

5. Improved Clock Synchronization Method

5.1. Specific methods:IEEE
The 1588 protocol only provides compensation for the clock deviation of master and slave clock. Establish the equation of state and measurement equation of clock deviation and frequency deviation, and adopt kalman filtering method to correct the clock deviation, thus reduce the deviation statistics and improve the synchronization accuracy. The kalman filtering algorithm is suitable when the process noise and measurement noise are white noise, so the noise characteristic is tested using Allan variance according to the experimental data.

Let the equation of state and the measurement equation be

\[
\begin{align*}
\dot{x}_k &= \Phi(k,k-1)x_{k-1} + G(k-1)w_{k-1} \\
y_k &= H(k)x_k + v_k
\end{align*}
\]

The formula is the system state vector; the measurement vector; the acquisition noise and measurement noise are independent Gaussian white noise and the state matrix; G is the input matrix and H is the measurement matrix. The estimated variance is:

\[
\hat{x}_{k|k} = \Phi(k,k-1)\hat{x}_{k-1|k-1}
\]

The Kalman filter gain is:

\[
K_k = P_{k-1}H^\top (k) \left[ H(k)P_{k-1}H^\top (k) + R_k \right]^{-1}
\]

The status update equation is

\[
\hat{x}_{k|k} = \hat{x}_{k-1|k} + K_k \left[ y_k - H(k)\hat{x}_{k-1|k} \right]
\]

The updated covariance moment is

\[
P_{k|k} = \left[ I - K_kH(k) \right] P_{k-1}
\]

The Kalman filtering algorithm is suitable for the case of process noise and measuring noise Gaussian white noise. In practice, in order to verify the applicability of the model algorithm, the Allan variance is used to test the noise characteristics, and the Allan variance model is defined as:

\[
ADEV(\tau) = \sqrt{\frac{1}{2\tau^2} \left( [x(t + 2\tau) - 2x(t + \tau) + x(t)]^2 \right)}
\]

Combining the kalman state estimation model and the Allan variance inspection model, the obtained deviation value is measured in the realization of synchronization. \(T_0=2s\), one cycle per 10 sampling data, \(n = 10\), with the timestamp obtained as each observation, calculates the information to the model and the acute compensation correction of the clock deviation.

5.2. Improved synchronization deviation accuracy test after the algorithm.
The waveform data of the back-to-back test of the improved algorithm is shown in Fig.3, and the clock deviation of any one time is about 79 ns, the deviation curve is shown in Fig.4, and the deviation distribution histogram is shown in Fig.4. From the deviation distribution histogram, the main deviation distribution is within the range of (-20ns~20ns).
6. **Operation Effect**

The BeiDou Power Grid time synchronous management system can provide high-precision time synchronous timing equipment and the whole network time synchronization system in large areas, realizing the remote centralized state management of the clock equipment. The system is a high precision, high stability, and high reliable time synchronization management system that provides an overall solution of set management, monitoring and unified time timing. After commissioning, discovery and traditional time.

The Synchronization system has the following advantages:
(1) The BeiDou satellite adopts bidirectional timing to solve the inherent time and accumulated errors, such as the traditional one-way timing (one-way timing and GPS timing and one-way BeiDou), to ensure the unified time of the whole network and provide a reliable, safe and accurate time source for the development of the smart grid.

(2) By monitoring the state of the timing device and the entrusted equipment, compare the accuracy of the timing device and the timing equipment in real time, save and analyze the difference between the abnormal alarm, and send it to the central station monitoring system of the entrusted equipment through the BeiDou satellite to ensure the connection of the entrusted equipment. Then, the correct time was received.

(3) Taking the standard configuration of the BeiDou satellite navigation system as the main clock of satellite synchronization and a single GPS as the main time benchmark, it solves the huge security risks brought by the current time synchronization system and realizes the autonomy of the satellite timing of the power grid.

(4) Relying on the communication function of the BeiDou system, the equipment information such as its operation status and accuracy will be sent to the monitoring system of the central main station, monitoring and remote control the operation status and installation time of each station, so as to realize the centralized monitoring and management of the operation status of each clock equipment.

(5) The whole network time synchronization management system of BeiDou Power can integrate SDH, PTP and other local chain network methods, independently set the main preparation mode, intelligent switch, build a comprehensive time management platform, and realize the real "mutual preparation between heaven and earth".

7. Conclusion
This design is based on the BeiDou/GPS FPGA field programmable gate array dual-mode synchronous timing system. The stability of the system is improved through the BeiDou and GPS. At the same time, the fast speed of the hardware codec ensures real-time, and the PLL phase-locked loop achieves the continuous temperature synchronous output of the second pulse. The system outputs time information such as serial information, IRIG-B coding, 1PPS second pulse and other formats, to meet the requirements of time information format and accuracy. At the same time, the BeiDou 2 satellite timing reduces the over-dependence on the GPS system.

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