Empowering GNNs with Fine-grained Communication-Computation Pipelining on Multi-GPU Platforms

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Abstract

The increasing size of input graphs for graph neural networks (GNNs) highlights the demand for using multi-GPU platforms. However, existing multi-GPU GNN solutions suffer from inferior performance due to imbalanced computation and inefficient communication. To this end, we propose MGG, a novel system design to accelerate GNNs on multi-GPU platforms via a GPU-centric software pipeline. MGG explores the potential of hiding remote memory access latency in GNN workloads through fine-grained computation-communication pipelining. Specifically, MGG introduces a pipeline-aware workload management strategy and a hybrid data layout design to facilitate the communication-computation overlapping. MGG implements an optimized pipeline-centric kernel. It includes workload interleaving and warp-based mapping for efficient GPU kernel operation pipelining and specialized memory designs and optimizations for better data access performance. Besides, MGG incorporates lightweight analytical modeling and optimization heuristics to dynamically improve the GNN execution performance for different settings at runtime. Comprehensive experiments demonstrate that MGG outperforms state-of-the-art multi-GPU systems across various GNN settings: on average 3.65× faster than multi-GPU systems with a unified virtual memory design and on average 7.38× faster than DGCL framework.

1. Introduction

Over the recent years, graph-based deep learning has attracted lots of attention from the research and industry field. Among various graph-learning methods, graph neural network (GNN) [28, 54, 48] gets highlighted most due to its success in many graph-based deep learning tasks (e.g., node feature vector (embedding) generation for node classification [26, 19, 12] and link prediction [7, 29, 46]). GNNs consist of several layers, where layer $k+1$ computes the embedding for a node $v$ based on the embeddings at the previous layer $k$ ($k \geq 0$) by applying $a_v^{(k+1)} = \text{Aggregate}^{(k+1)}(\{h_u^{(k)} | u \in N(v) \cup h_v^{(k)}\}$ and $h_v^{(k+1)} = \text{Update}^{(k+1)}(a_v^{(k+1)})$, where $h_v^{(k)}$ is the embedding of node $v$ at layer $k$. The Aggregate function will accumulate neighbors’ ($N(v)$) embeddings of node $v$. The Update function usually consists of a fully-connected NN layer. In comparison with the conventional methods for graph analytics, such as random walk [20, 44, 24] and graph Laplacians [33, 32, 10], GNN features higher accuracy [28, 54, 48, 14, 13] and better generality [23, 59, 9] on various applications.

GNN computation on large input graphs with millions/billions of nodes and edges is a huge challenge because of the high memory and computation demands. Many research efforts have thus been devoted to improving GNN execution performance on powerful multi-GPU platforms (e.g., NVIDIA DGX [39]), which feature high aggregated computation power and memory capacity and become the major building blocks for more than 60% modern HPC systems [45] for large-scale scientific computing and deep learning. The first type of effort [8, 11, 57, 15] eliminates the need for communication by leveraging neighbor sampling and mini-batch processing in a data-parallel fashion. However, existing research [25, 8] shows that such an algorithmic modification would compromise the accuracy of GNN models compared to the original GNNs. It would also destabilize the algorithmic performance (e.g., slower training convergence rate) under different graph inputs and sampling configurations. Another type of effort (e.g., DGCL [4] and NeuGraph [34]) keeps the algorithm intact and leverages the dedicated communication libraries optimized for GNN computation on multi-GPU platforms. However, this type of effort would incur excessive fine-grained irregular remote access for fetching neighbor embeddings.

In this paper, we highlight a more promising, new type of solution for accelerating GNNs on multi-GPU systems. We propose to exploit the fine-grained pipeline of the communication and computations to largely hide the remote data access overhead. Our key observation is that there are many opportunities for overlapping operations at different granularities in GNNs. For instance, for the neighbor aggregation on a single graph node, the remote neighbor access can be overlapped with the local neighbor computation. Among different nodes, the remote data access for certain nodes would potentially be overlapped with the local computation of other nodes.

However, exploring the benefits of such fine-grained pipelining requires non-trivial system-level insights and design efforts. The original neighbor aggregation in multi-GPU GNNs [25, 34, 4] just requires invoking the high-level holistic memory and computation APIs for the non-overlapped communication and computation phases, respectively. In contrast, fusing the communication and computation as a single kernel would significantly increase the design complexity. Since it will break down memory and computation phases into a...
set of low-level detailed operations followed by fine-grained operation interleaving. It requires users to explicitly identify the local and remote computation, properly layout GNN input data to improve data access efficiency, and effectively schedule operations to benefit pipelining. Moreover, the most effective design of operation pipelining would largely vary depending on the GNN inputs (e.g., the graph structures and the node embedding dimensionality) and hardware platforms (e.g., different types/numbers of GPUs). This will impose more burdens on users to handle many low-level design details and complicated configuration tradeoffs.

To this end, we introduce **MGG**, a holistic system design and implementation for GNN acceleration on multi-GPU platforms. The key design insight of MGG is to mitigate the effects of irregular remote neighbor access in GNNs via a fine-grained GPU-based software pipeline with overlapped communication and computation. (Figure 1).

*From the workload and data perspective*, we reshape the irregular GNN workloads to expose sufficient opportunities for pipelining. We explicitly categorize and split GNN computation workloads based on their local and remote memory access patterns at different levels (e.g., inter-GPU and inter-graph-node) of granularity. We also carefully orchestrate the data layout of the graph structure (edge lists) and node embeddings by identifying their key access patterns (e.g., dominated by remote/local access) and leveraging different types of GPU memory (e.g., shared and private device global memory) to minimize their access costs.

*From the GPU-kernel perspective*, we tailor the GPU computation kernel for multi-GPU GNN workloads to maximize the computation capability of GPUs. We decompose the neighbor embedding fetching and embedding aggregation phases into a set of memory access and computation operations. Then we interleave the remote access (for fetching remote neighbor embeddings) with the aggregation computation (for accumulating neighbor embeddings). Such a fine-grained operation overlapping and pipelining will effectively pair appropriate-size communication and computation workloads to amortize the communication overhead. We map memory and computation operations to GPU warps to maximize computation parallelization and improve the scheduling efficiency of GPU Streaming Multiprocessors (SMs).

*From the design configurability perspective*, we parameterize MGG with a set of tunable knobs (e.g., workload partition size and interleaving distance) to maintain pipelining effectiveness. Such a highly configurable design can confidently accommodate diverse GNN inputs (e.g., graphs with a different number of edges and node embedding dimensionalities) and hardware platforms (e.g., different numbers of GPUs and the computation/memory capacity of different GPUs).

We build our design on NVIDIA GPUs with NVSHMEM [41] (a typical type of SHMEM [6, 2, 41]), which is the state-of-the-art programmatic communication library for fine-grained inter-GPU communication. To the best of our knowledge, we are the first to explore the potential of NVSHMEM for GPU kernel operation pipelining in the irregular multi-GPU GNN computation. Despite being tailored for GNN computation on multi-GPU platforms, our design can be generalized with minor changes towards other applications or platforms sharing the similar demands or supports of fine-grained irregular communication (As detailed in §6).

Overall, we make the following contributions in this paper:

- We give an in-depth analysis of existing multi-GPU solutions and identify their performance bottlenecks and key takeaways that inspire our design (§2).
- We propose a pipeline-aware workload management strategy and a hybrid data layout design tailored for multi-GPU GNNs, to facilitate the communication-computation pipelining (§3.1-§3.2).
- We implement an optimized pipeline-centric kernel, encompassing workload interleaving and warp-based mapping for fine-grained computation-communication overlapping and specialized memory designs and optimizations for better data access performance (§3.3-§3.4).
- We introduce lightweight analytical modeling and optimization heuristics to dynamically improve the performance of GNN training at runtime (§4).
- Comprehensive experiments demonstrate that MGG outperforms state-of-the-art multi-GPU systems across various GNN settings: on average 3.65× faster than multi-GPU systems with a unified virtual memory design and on average 7.38× faster than DGCL framework.

### 2. Related Work and Motivation

In this section, we will first give an in-depth analysis of the existing solutions (*Collective Communication* and *Unified Virtual Memory*) in addressing the communication challenges of multi-GPU GNNs. Then we will motivate our SHMEM-based design for communication-computation pipelining.

#### 2.1. Collective Communication Design

The rising popularity of deep neural networks (DNNs) on multi-GPU platforms facilitates an array of Collective Communication designs [38, 1, 35] on optimizing the inter-GPU data movement. Among these designs, NCCL [38] delivers state-of-the-art communication performance on NVIDIA GPUs. NCCL shows its strength in collective operations (e.g., reduce)
for DNN training, which follows a low-communication data-parallel scheme. However, in the communication-intensive GNNs, NCCL could hardly demonstrate its advantages due to two major reasons. **First**, NCCL is designed for regular communication patterns, while the communication in sparse GNN computation is highly irregular. For instance, the well-known NCCL’s collective operation, *all-reduce*, follows the ring-based reduction across GPUs [5, 49]. While in GNNs, the remote access among different GPUs largely relies on irregular point-to-point data transferring in a fine-grained manner. **Second**, NCCL’s APIs can only be used in the CPU program outside the GPU kernel. It has to interrupt (or wait until the exit of) the current GPU kernel execution for communication, leading to non-trivial transitioning costs between communication and computation.

To show the performance of NCCL in multi-GPU GNN computation, we build a basic NCCL-based GNN layer, where each GPU maintains a subset of node embeddings in its device memory, and it will forward its current node embedding subset to the next GPU (a ring-based node embedding forwarding) once it finishes its aggregation. The whole program will end after each GPU has “traversed” all node embeddings. And we select two graph datasets: Reddit with 232 thousand nodes and 114 million edges, and enwiki-2013 with 4 million nodes and 202 million edges. Figure 2 shows that data transferring via NCCL could take more than 5× latency compared to the latency of aggregation computation. This is mainly because of NCCL’s inefficiency in transferring vector-based node embeddings and the huge bandwidth gap between the high-speed global memory (around 1TB/s) and inter-GPU connections, like NVLink (around 100GB/s). There are several potential optimizations that could be applied to improve the performance of NCCL-based GNNs, such as 1) increasing the node embedding chunk size/granularity to avoid redundant communication and 2) mixing the collective communication with point-to-point communication based on the node embedding access pattern at runtime. However, these optimizations may 1) increase the frequency of initializing/invoking the NCCL communication function and context switching between the GPU device kernels and the CPU hosts and 2) introduce additional runtime cost and latency overhead for dynamically determining the communication pattern. This motivates us to incorporate multi-GPU SHMEM [41, 2] to exploit the fine-grained communication-computation pipelining.

2.2. Unified Virtual Memory Design

Unified Virtual Memory (UVM) [43] maintains a global “virtual” view of a single address space spanning across the memory of different devices (CPUs and GPUs). By employing UVM, multi-GPU programming can be simplified as single-GPU programming without worrying about the data’s physical location on different devices [43, 56, 27]. UVM has also been demonstrated in accelerating the irregular graph analytical workload (such as graph traversal [18] and PageRank analysis [27]). In UVM, a global unified virtual memory space is allocated by invoking cudaMallocAsync API on CPUs and the whole memory space is organized as memory pages that reside on different device memory. When a GPU kernel wants to access the data which is not presented on GPU memory, a GPU-side memory page fault would happen and a CPU-to-GPU page migration would be triggered to fetch the corresponding data from the host memory to GPU memory.

Even though UVM offers the easiest way for programming and handling out-of-GPU-memory GNN inputs, the performance of such a design is usually unsatisfactory. There are several major challenges. **First**, GNN computation relies on highly irregular memory access. Therefore, using UVM would trigger lots of GPU-side page-fault for frequently fetching remote data. In addition, the memory page size is fixed and large (around 4KB) while the embedding size of an individual neighbor node is small (less than 0.4KB). Thus, most of the 4KB memory pages migrated through costly page-faulting are largely wasted. **Second**, using UVM has to count on the relatively low-speed CPU processor for host data management and low-bandwidth PCIe connection for CPU-to-GPU data transferring, which largely stall the GPU execution. Besides, the irregular GNN computation can easily cause UVM page thrashing [17, 16] (*i.e.*, the same memory page is bouncing among different device memory), which further exacerbates such a situation, leading to severe GPU under-utilization. To better understand the bottleneck of UVM, we use the NVIDIA NSight System profiler [40] to extract the page-fault-related information of UVM-based GNN design across different settings of GPUs (from 2 to 8 GPUs) on the latest NVIDIA DGX-A100 platform. Figure 3 shows that the increase in the number of GPUs would lead to more page-fault events and page-fault handling cycles, which would largely hinder performance scaling. Note that we start with the 2-GPU setting since our problem setting is about multi-GPU GNN for
scaling datasets that cannot fit into a single GPU. The potential optimization of UVM is to increase the data movement granularity through batching more data on the same memory page [27]. However, in the highly irregular GNN computation, such a strategy would incur non-trivial time costs for careful batch-size selection and data batching, which are essential to maximizing the memory-page utilization and communication efficiency. To conclude, we remark that a design that can offer more flexibility in data movement granularity and leverage high-bandwidth GPU interconnects (e.g., NVLink) would benefit the overall multi-GPU GNN execution performance.

2.3. SHMEM Design

SHMEM [6, 41, 2] is a typical parallel programming model that follows the Partitioned Global Address Space (PGAS) design principle. It consists of a global memory address space that logically concatenates the device memory subspace of each worker (e.g., CPU/GPU). Among existing SHMEM implementations, the recently released NVHSMEM [41] facilitates inter-GPU communication across NVIDIA GPUs. Listing 1 illustrates the basic NVHSMEM APIs in CUDA C. Note that in NVHSMEM, each CPU thread/process manages one GPU device, and the same NVHSMEM-based kernel will be executed on different GPUs concurrently. In the following of this paper, we will mainly discuss our design with NVHSMEM and the same design principles can be applied to other platforms with minor efforts, such as AMD GPUs with ROC_SHMEM [2, 22]. We compare qualitatively SHMEM with Collective Communication and UVM in Table 2.

Despite such potential of NVHSMEM, using NVHSMEM to improve GNN’s runtime performance on multi-GPU platforms is still non-trivial. The existing explorations of NVSHMEM are limited to traditional deep-learning (e.g., Livermore Big Artificial Neural Network [47]) and scientific computing (e.g., quantum chromodynamics [53]), which are regular in remote data access with a relatively lower communication-to-computation ratio. For illustration, we build a baseline design (Direct NVHSMEM) by directly applying NVHSMEM for remote neighbor access to compare with the UVM-based design on GNN aggregation across several representative datasets (detailed in §5). Table 1 shows that NVHSMEM is in fact not a free lunch. Directly applying NVHSMEM would barely show performance advantages (in fact 23% lower on average) over the UVM-based design. Directly applying NVHSMEM on-demand to fetch individual remote neighbors embeddings would initiate many separated NVHSMEM requests and incur non-trivial overheads (e.g., communication warm-up costs). Besides, highly irregular execution of each warp (frequently switching between local computation and remote access) would lead to inefficient warp-level scheduling on GPU SMs, thus, lowering the utilization of GPUs and NVLinks. UVM-based design can potentially merge multiple separated remote access into a single memory page movement based on the locality of remote data, thus, amortizing the communication cost.

2.4. Other Related Work

Existing GNN computing systems are optimized to maximize the computing parallelism while minimizing the impact of the intensive and irregular data communication/access. ROC [25] proposes a distributed GNN computing system with learning-based graph partitioning and dynamic-programming optimized memory management strategy to maximize the efficiency of multi-GPU parallelism of GNNs. P3 [15] introduces pipelined push-pull parallelism and graph-structure-based inter-GPU communication for multi-GPU GNN computation. design differs from these existing GNN systems in several aspects. Pipelining optimization in [15, 34] aims at coarse-grained overlapping of computation of different mini-batched graphs or overlapping of streaming vertex chunks to GPUs with the GNN computation on GPUs. While our design explores...
a new type of pipelining optimization through fine-grained computation-communication overlapping when processing every single graph on individual GPUs. In addition, prior work has yet to leverage the recent software/hardware advancement in communication, such as NVSHMEM-based on NVLink. They tailor their design/optimization for the low-bandwidth PCIe [34, 25, 15] with naturally high communication cost.

2.5. Motivation

Our key research motivation in this paper is to investigate the potential of communication-computation pipelining in addressing the communication and computation in GNN still encounters several key challenges: 1) How to manage the irregular GNN input data systematically so that we could balance data locality, communication & computation workload, and graph partition overhead? 2) How to decompose the communication workload effectively so that we could overlap the communication and computation? 3) how to make the design and optimization flexible enough so that we could accommodate the diverse hardware platforms, GNN models, and inputs?

Since this is the first system work to demonstrating the communication-computation pipelining in multi-GPU GNN computation, we first investigate the communication patterns. For the following sections, §3.1-§3.2 address the first question with pipeline-aware workload management and hybrid GNN data placement. §3.3-§3.4 address the second question with warp-based mapping & pipelining and specialized memory design & optimization. §4 tackles the third question with modeling and design optimization. §5 extensively evaluates MGG in various aspects and compares with existing solutions.

3. MGG Design

In this section, we detail two major components of MGG that collaborate with each other: GNN Workload & Data Management (§3.1-§3.2) and Pipeline-centric Kernel (§3.3-§3.4).

3.1. Pipeline-aware Workload Management

To facilitate efficient GPU kernel operation pipelining, the key enabler is to properly distribute the computation workloads to exploit the opportunity of computation-communication overlapping. In GNNs, the irregularity of graph-based data (e.g., graph structure) makes it hard to distribute GNN workloads among different GPUs for effective pipelining. We propose a novel pipeline-aware workload management technique based on three key metrics, the number of devices, the types of workload, and the number of neighbors. Unlike prior designs [34, 4, 25] which tend to minimize inter-GPU communication, our MGG design aims to maximize the workload balancing while facilitating the overlap of computation and remote memory access. GNNAdvisor [51] introduces a 2D workload management with adjustable workload granularity for GNN computing. However, GNNAdvisor is designed and optimized for single-GPU GNN computation, where all node embedding access is local on the same GPU. Therefore, GNNAdvisor only needs to balance homogeneous GNN aggregation workloads with local memory access demands. In contrast, MGG can support multi-GPU GNN computation and effectively handle heterogeneous GNN aggregation workloads with local and remote memory access demands. Specifically, there are three key strategies of our MGG design:

**Edge-balanced Node Split**: This solution is to partition the GNN input graph by nodes while considering the number of edges within each partition. On the one hand, our strategy would demonstrate the advantage of node split, where each node will only be handled by one GPU. This can avoid additional overhead to synchronizing partial aggregation results on different GPUs. On the other hand, our strategy can enjoy the benefit of the balanced edge split, where different partitions will maintain an approximately equal number of edges for computation across GPUs. We cut the whole graph by selecting $n-1$ node-split points, where $n$ is the number of GPUs. To determine these points, we will first get the total number of edges of the whole graph and divide this number by the number of GPUs to get the approximate number of edges processed for each GPU. Then we develop a range-constrained binary search (Algorithm 1) to determine the node-split points such that each GPU would process an approximately equal number of edges.

**Locality-aware Edge Split**: This step is to split the workload on each GPU based on its type after the above node split. We categorize the sparse multi-GPU GNN computation into two categories. The first type of aggregation involves only the local GPU device memory. The key character of processing these types of neighbors is the low-cost neighbor access, leading to shorter execution latency. The second type of aggregation triggers remote access for non-local neighbors, which features high latency and overhead. To delicately handle these two types of workloads, we group the same types of neighbors together (Figure 4(a)-1) to build two separate CSR for local and remote virtual graphs, respectively. The aggregation will be conducted on local and remote virtual graphs in parallel, and the partial aggregation result of the same node in both local and remote virtual graphs will be accumulated to generate the final output embedding.

**Workload-aware Neighbor Split**: This step is to handle the workload imbalance among nodes within each virtual graph. Different nodes would have a different number of neighbors from each other in the virtual local and remote graphs. Therefore, the aggregation workload among different nodes would also be largely diverse. This makes it challenging for massively parallel GPU devices to harvest the real performance gains due to the imbalance workload and diverged execution flow. Our neighbor partitioning strategy is
Algorithm 1: Range-constrained Binary Search.

```plaintext
input : Graph node pointer array (nPtr), edge list array (eList), and the number of GPUs (numGPUs).
output : list of graph edge split points (numGPUs - 1).
outList = [] lastPos = 0;
// Compute approximated edges per GPU.
/*
  ePerGPU = (len(eList) + numGPUs - 1)/numGPUs;
for std in [0, ..., numGPUs - 1] do
  nid = binSearch(nPtr, ePerGPU, lastPos, numNodes);
  lastPos = nid;
  outList.append(nid);
end
return outList;
// Search split points on nPtr.
/*
Function binSearch(nPtr, ePerGPU, lastPos, numNodes):
  i = lastPos; j = numNodes;
target = min(nPtr[i] + ePerGPU, nPtr[numNodes]);
while i < j do
  mid = (nPtr[i] + nPtr[j])/2;
  if mid > target then
    j = (i + j)/2;
  else
    i = (i + j)/2;
end
return i;
```

Figure 4: (a) Illustration of Pipeline-aware Workload Management. (b) Conceptual exemplification of workload decomposition and interleaving/pipelining. “RNP”/“LNP” are the remote/local neighbor partitions. Local neighbor access is omitted in (b).

3.2. Hybrid GNN Data Placement

In collaboration with our workload management strategy to facilitate efficient communication-computation pipelining (Figure 4(b)), we introduce a hybrid GNN data placement strategy that can exploit the benefits of different types of memory in SHMEM-enabled multi-GPU systems. Specifically, we enforce two types of strategies, as exemplified on the left of Figure 5. For node embeddings (NE), we leverage NVSHMEM “shared” global memory to store the whole graph embeddings, which essentially distributes node embeddings to different GPUs’ global memory space. We first partition the input graphs into n partitions (where n is the number of GPUs) and each partition is placed in one GPU’s “shared” global memory space, created by nvshmem_malloc API. Compared to the traditional cudaMalloc that allocates the “private” global memory space dedicated for the current GPU, the global memory space allocated by nvshmem_malloc can be accessed by all GPUs involved in the current NVSHMEM context via GPU device IDs and memory address offsets. Our key design insight is that node embedding vectors (NE) (i) are usually large (high dimensionality) and have to be distributed among different GPUs, and (ii) require remote access support when stored on different GPUs. Therefore, shared global memory space in NVSHMEM is a good fit for NE since it provides (i) a large space (by aggregating device memory of different GPUs) and (ii) direct remote access support across GPUs.

On the other hand, for storing partitioned graph structure (GP) data (e.g., the edge list), we use cudaMalloc to allocate the “private” global memory space that is only visible to the current GPU. Considering that NVSHMEM “shared” global memory offset would start from zero for each GPU, the original global node ID in the edge list should be converted to a GPU local memory index for accessing the correct neighbor embeddings according to the node-ID range on different...
3.3. Warp-based Mapping & Pipelining

In addition to effective workload management and data placement, the next key step is to map such logically partitioned workloads to the low-level GPU programming abstractions (e.g., GPU threads/warps/threadblocks) for efficient computation-communication pipelining.

Firstly, we choose GPU warp as the basic working unit for handling the workload of each partition. This is because threads in a warp can collaboratively work on different dimensions of a node embedding simultaneously. Whereas using a single or several threads (less than the size of a warp, 32 threads) would hardly exploit the computation parallelism and would cause warp-level divergence. Besides, NVSHMEM remote access initiated by a warp of threads would merge the requests into one remote memory transaction to reduce the overhead. The method we choose for remote access is GET, which is initiated by the GPU kernel that requests certain neighbor embeddings for aggregation. Compared with the PUT method, GET will simplify the overall design. When using PUT, we have to employ a complex receiver-side synchronization mechanism to consistently check the local memory buffer for making sure that the required node embedding arrives before its aggregation begins. This would lead to extra computation costs that would degrade the performance. Secondly, we will decide how to map each workload to the underlying GPU warp. The most straightforward way is to continuously map the neighbor partitions from the local and remote workload list to GPU warps with continuous IDs, as shown in Figure 6. However, this strategy would easily suffer from workload imbalance among GPU SMs. Because warps with continuous IDs are more likely to be placed into the same thread block, which is assigned to one SM for processing. Therefore, SMs assigned with warps for handling remote neighbor partitions would lead to much longer latency than SMs assigned with warps for processing local neighbor partitions. Such a workload imbalance would lead to poor GPU utilization and runtime execution performance.

To this end, we introduce our novel workload interleaving strategy to balance the workload among SMs on GPUs. Each warp of threads running on GPU would handle one or more pairs of local/remote workload partitions. We introduce a new metric – interleaving distance to more precisely calibrate the warp-to-SM mapping for different pipeline stages to achieve efficient pipelining. We give examples with the interleaving distance equals 1 and 2 in Figure 6 for illustration. The major design insight is that by mixing different types (local/remote) of workload together, we can achieve better GPU utilization since when one warp is blocked for high-cost remote access, other warps that are working on local computation can still be served by the SMs warp scheduler for filling up these idle GPU cycles. Such a design would also improve the design flexibility: given an input graph with a selected neighbor partition size, we can adjust the size of interleaving distance and the workload per warp so that waiting cycles of the remote access can be hidden by the computation cycles of the neighbor aggregation. Thus, each warp can be fully utilized while the overall design can achieve sufficient parallelism.

3.4. Specialized Memory Design & Optim.

To achieve highly efficient communication-computation pipelining at the GPU kernel level, it is indispensable to carefully manage the high-bandwidth shared memory of GPU SMs for high data access efficiency and asynchronized primitives for exploiting intra-warp operation pipelining.

GPU SM Shared Memory Layout: Based on our MGG’s warp-based workload design, we propose a block-level shared memory orchestration to maximize the performance gains. We have several key insights for such a dedicated memory layout design within each thread block. First, our neighbor-partition-based workload will generate the intermediate results that can be cached at the high-speed shared memory for reducing the frequent low-speed global memory access. Second, NVSHMEM-based remote data access demands a local scratch-pad memory to hold the remote data for local op-
There are several steps for us to utilize the block-level shared memory. For the local neighbor aggregation, we reserve a shared memory space \((4 \times Dim)\) bytes for floating-point embeddings) for the target node of each neighbor partition so that threads from a warp can cache the intermediate results of reduction in shared memory. For the remote neighbor aggregation, the shared memory space is doubled \((2 \times nps \times D)\). The reason is that we need the first half \((nps \times D)\) for caching the partial aggregation results of each warp but also the second half \((nps \times D)\) for the remotely accessed neighbor embeddings. The detailed customization procedure is described in Listing 2. For each MGG kernel design, we will first identify the warp-level information at Line 3 to 10, such as the warp IDs. Then within each thread block, we define the customized shared memory layout by splitting the contiguous shared memory address into three different parts for neighbor ids \((\text{partial\_ids})\), partial aggregation results \((\text{partial\_results})\), and the remotely-fetched node embeddings \((\text{tmp\_local})\), at Line 12 to 18. We also calculate the relative address offset for each warp within each part of shared memory space, at Line 20 to 22. Note that we use the dynamic shared memory technique in MGG for design flexibility, since those parameters \((\text{part\_Size}, \text{warpPerBlock}, \text{dim})\) can only be determined at runtime. We will first calculate the shared memory size (Line 32) and then pass it as a kernel launching parameter (Line 34).

**Pipelined Memory Operation:** In §3.3, we have discussed assigning local (LNP) and remote (RNP) neighbor aggregation workload to warps so that different warps can overlap their computation and communication to fully saturate the active cycles of the GPU SM scheduler. However, only exploiting the inter-warp communication-computation overlap is not enough to maximize the utilization of GPU resources. We further explore the overlapping of the computation and communication at the intra-warp level by carefully scheduling the memory operations. As shown in Figure 7(a) for the case with two LNPs and two RNPs by using the synchronized remote access, we can just sequentially process the two LNPs and the two RNPs. The long-latency remote access can happen only after the completion of its preceding LNP. This could lead to a longer GPU stall for memory operations and low GPU SM utilization. Based on our profiling, we find that without overlapping, the remote access usually dominates the overall execution (around 60% of overall latency) compared to the time for local data access plus the time for aggregation computation (around 40% of overall latency). Such an observation also motivates our current design to mainly hide the remote access latency. To amortize the cost of remote access for each warp, we introduce the *asynchronized remote memory operations* (Figure 7(b)).

This improved design consists of two major steps. *First*, we can simultaneously launch the local memory access while initializing the remote memory access for fetching the node embedding (1), therefore, the time for remote access can be amortized by the processing of LNP. *Second*, once the remote access is completed, the current warp will start aggregation on the remotely-fetched node embedding data (2). The next step will start the new iteration of the previous two steps, which will process a new pair of LNP and RNP.

## 4. Modeling and Design Optimization

In this section, we will discuss our performance/resource analytical modeling and design optimization strategy.
Analytical Modeling: The performance/resource model of MGG has two variables: workload per warp (WPW) and shared memory usage per block (SMEM), which can be measured by the following formulas

\[ WPW = 2 \cdot ps \cdot D \cdot \text{dist}, \]
\[ SMEM = ps \cdot wpb \cdot \text{IntS} + 2 \cdot wpb \cdot D \cdot \text{FloatS} \]

where \( ps \), \( wpb \), and \( D \) are the sizes of neighbor partition, warp per block, and node embedding dimension, respectively; \( \text{dist} \) is the interleaved distance of local/remote workloads (§3.3); \( \text{Dim} \) is the node embedding dimension; \( \text{IntS} \) and \( \text{FloatS} \) are both 4 bytes on GPUs. To determine the value of the \( ps \), \( wpb \), and \( dist \) of a given input graph, we will first compute the total number of warps by using

\[ \text{numWarps} = \frac{\max\{\text{local, remote}\}}{\text{dist}} \]

where \( \text{local} \) and \( \text{remote} \) are the number of local and remote partitions, respectively. Then we compute the total number of blocks and the estimated block per SMs by using

\[ \text{numBlocks} = \frac{\text{numWarps}}{wpb}, \]
\[ \text{blocksPerSM} = \frac{\text{numBlocks}}{\text{numSMs}} \]

Later, based on our micro-benchmarking results on diverse datasets, we define our parameter search space and constraints: 1) \( ps \in [1 \ldots 32] \) to balance the computation parallelism and synchronization overhead; 2) \( \text{dist} \in [1 \ldots 16] \) to effectively overlap the computation and remote memory access; 3) \( wpb \in [1 \ldots 16] \) to maintain SM warp scheduling flexibility for high occupancy and throughput; 4) \( \text{numSMs} \leq c_1, \text{SMEM} \leq c_2 \), where \( c_1 \) and \( c_2 \) are hardware constraints [52], e.g., NVIDIA A100 GPU has 108 SMs and 164KB shared memory per SM.

Cross Iteration Optimization \( ps \), \( dist \), and \( wpb \) are initialized as the value 1 at the beginning. Then we optimize one parameter in each of the following iterations. First, we increase the \( ps \) to maximize the warp utilization. When further increasing the \( ps \) would also increase the latency, we would stop the search on \( ps \) and switch to \( dist \). Second, we apply a similar strategy to locate the value of \( dist \) that can maximize the overlap of local computation and remote access. Third, we increase \( wpb \) to maximize the utilization of the entire SM. If any increase of \( wpb \) would increase the latency, we know that there may be too large thread blocks or too heavy workloads on individual warps that lower SM warp scheduling efficiency or computation parallelism. We would “retreat” (i.e., decrease) \( ps \) to its second-highest value if necessary and restart the increase of \( wpb \). This optimization algorithm will stop when any decrease of \( ps \) and increase of \( wpb \) would lead to higher latency than the top-3 lowest latency. The latency of each iteration during the optimization will be recorded by a configuration lookup table. At the end of the optimization, the configuration with the lowest latency will be applied for all following iterations.

This particular optimization order of parameters (\( ps \), \( dist \), and \( wpb \)) is based on two major aspects: (i) Spatially speaking, the granularity is from coarse-grained algorithm-level partitioning through \( ps \), to medium-grained pipeline construction through \( dist \) (according to the partition plan), to fine-grained pipeline-to-warp fine-tuning through \( wpb \) (according to the pipeline design). (ii) Temporally speaking, the three optimizations are applied at loading-time (\( ps \) to decide layout), kernel initialization (\( dist \) to decide pipeline), and runtime (\( wpb \) to decide pipeline mapping), respectively.

5. Evaluation

Benchmarks & Datasets We choose two representative GNN models for node classification tasks to cover different types of operations in aggregation:

1) Graph Convolutional Network (GCN) [28] is one of the most popular GNN architectures. It is also the key backbone network for many other GNNs, such as GraphSAGE [23], and Differentiable Pooling [55]. Improving the performance of GCN will also benefit a broad range of GNNs. We use the setting: 2 layers with 16 hidden dimensions for GCN, which is also the setting from the original paper [28]; The computation of a 2-layer GCN can be expressed as

\[ Z = \text{Softmax}(\hat{A} \text{ReLU}(\hat{A}W^1)W^2). \]

where \( \hat{A} \) is the adjacent matrix of the input graph with self-loop edges, and \( X \) is the input node embedding matrix, where \( X \in \mathbb{R}^{N \times D} \), \( N \) is the number of nodes in a graph; \( D \) is the size of node embedding dimension. \( W^1 \) and \( W^2 \) are trainable weight matrices in the layer-1 and layer-2, respectively.

2) Graph Isomorphism Network (GIN) [54] is another typical type of GNN, which aims to distinguish the graph-structure that cannot be identified by GCN. Each layer of GIN can be expressed as

\[ h_{v}^{l+1} = MLP^{l}(1 + \epsilon^{l})h^{l} + \sum_{u \in N(v)} h^{l}_{u}. \]

where \( l \) is the layer ID and \( l \in \{0, 1\} \), MLP is a fully-connected neural network, \( h_{v} \) is the node embedding for node \( v \), and \( N(v) \) stands for the neighbors of node \( v \). GIN mainly differs from GCN in its aggregation function, which introduces a weight parameter as the ratio of contribution from its neighbors and the node itself. In addition, GIN is the reference architecture for many other advanced GNNs with more edge properties, such as Graph Attention Network [48]. Note that for GIN

| Dataset        | #Vertex | #Edge   | #Dim | #Class |
|----------------|---------|---------|------|--------|
| reddit (RDD)   | 232,965 | 114,615,892 | 602  | 41     |
| enwik-2013 (ENWIKI) | 4,203,323 | 202,623,226 | 96   | 128    |
| ogbn-products (PROD) | 2,449,029 | 61,859,140  | 100  | 64     |
| ogbn-proteins (PROT)       | 132,534  | 39,561,252  | 128  | 112    |
| com-orkut (ORKT)          | 3,072,441 | 117,185,083 | 128  | 32     |
evaluation, we use the setting: 5 layers with 64 hidden dimensions, which is also the setting used in the original paper [54]. Graphs used in our evaluation [30, 28] are large in their number of nodes and edges that demand multi-GPU capability for effective GNN computation. Details of the above datasets are listed in Table 3. #Class is the dimension of the output layer and is used for the node classification task.

Baselines We choose several representative implementations for comparison. 1) **UVM-based Design** has been highlighted in recent work [27] in handling irregular graph computations (such as PageRank) on out-of-GPU-memory graphs. Note that [27] is not open-sourced, we implement the UVM-based kernel design by following the design strategies from [27] and incorporating optimizations from MGG (§3) except the hybrid GNN data placement (which is specific to SHMEM-based design) and hierarchical workload management (since all graph structural data, e.g., edge lists, and node embeddings are maintained in the same unified virtual memory space regardless of their physical location); 2) **DGCL** [4] is the state-of-the-art system work that extends DGL [50] for full-graph GNNs on the multi-GPU platform. The core of DGCL is GCCL [4] (graph collective communication library), a distributed graph communication library with GNN-tailored optimizations. DGCL also stores the partitioned subgraphs with their node embeddings in the device memory of different GPUs. DGCL will first apply the graph-based Allgather to fetch the remote node embedding to local GPU memory. It then applies a local neighbor aggregation by leveraging the single-GPU GNN kernel in DGL. Additional multi-GPU designs, such as NeuGraph [34] and P³ [15], are not publicly available. We initially plan to evaluate our design on AMD ROC_SHMEM [2]. However, as indicated in its document and email responses from its authors, the existing ROC_SHMEM is an experimental prototype and is not officially ready to be applied in practice due to very strict limitations on software (e.g., only supports ROCm v2.10) and hardware (e.g., only supports AMD GFX9 GPUs), which are quite challenging to find and hard to deploy. We believe that once ROC_SHMEM becomes ready and generally applicable, MGG can be easily migrated to the AMD multi-GPU platform.

Platforms & Tools Our major evaluation platform is an NVIDIA DGX-A100 platform with dual AMD Rome 7742 processors (each with 64 cores, 2.25 GHz base clock), 1TB host memory, and 8×NVIDIA Ampere A100 GPUs (each with 40 GB device memory) connected via NVSwitch, which comes with 600 GB/s GPU-to-GPU bi-directional bandwidth. For the modeling study, we also leverage the NVIDIA DGX-1 platform with 4×NVIDIA Tesla V100 GPUs connected via NVLINKs. We use CUDA (v11.7) and NVSHMEM (v2.6.0) for building our MGG design. Other NN operators (such as the fully-connected layer and softmax layer) use cuBLAS [37] and cuDNN (v8.4) [36] library for implementation. For kernel-level profiling, we use NVIDIA NSight Compute to get the detailed performance metrics. We calculate the averaged speedup based on 100 runs of each setting.

5.1. Compared with UVM-based GNN

We comprehensively compare MGG with UVM-based design on the DGX-A100 for the end-to-end GNN computation. For UVM-based design, we put graph and embedding data in a global virtual memory space spanning across CPUs and GPUs without knowing its underlying layout and management strategy. Figure 8 shows that MGG achieves 3.16× speedup and 4.15× speedup on average compared to UVM-based design on GCN and GIN, respectively. It is mainly because MGG can fetch remote node embeddings through NVSHMEM-based fine-grained remote access. Such remote access can also fully overlap with the local aggregation computation to fully utilize the GPU resources. Comparing among different datasets, we can observe that for graphs (e.g., ogbn-products) with a more edges, MGG would demonstrate more speedup under the same number of GPUs. This is because our hierarchical workload management can manage to create an appropriate size of workload for each warp, meanwhile achieving sufficient computation parallelism among different warps. Comparing among different numbers of GPUs, An overall trend that when increasing the number of GPUs, MGG would achieve higher speedup. This is because of our effective usage of fine-grained data transfer in NVSHMEM. In contrast, UVM-based design leverages the page-faulting-based remote data access that is more coarse-grained (around 64 KB) in comparison with a single node embedding size (less than 4KB), which leads to higher overhead and lower bandwidth usage. This would also make UVM-based design challenging for GPU SM schedulers to effectively dispatch instructions for the next available warps since most of the warps are waiting for the long-cycle page-faulting and page-migration operations. To gain more insights from the performance strength of MGG, we further measure two performance-critical GPU kernel metrics: Achieved Occupancy and SM utilization, where the former is the utilization of all available SMs on a single GPU while the latter is the ratio of the average active warps per active cycle to the maximum num-
number of warps supported in an individual SM. MGG achieves an average of 21.15% better SM utilization and an average of 39.20% higher achieved occupancy and compared with UVM-based design, which indicates that neighbor partitioning and workload interleaving can 1) effectively distribute workload to more SMs to improve the overall GPU computing resource utilization, and 2) overlap the remote access and local aggregation computation from different warps to maximize the utilization of individual SMs.

5.2. Compared with DGCL

In this section, we compare our design with DGCL [4]. We build DGCL [4] from their source. We select the 8-GPU setting (the major setting used in their paper) on DGX-A100 and 1-layer GCN model with 16 hidden dimensions for comparison. Table 4 shows that MGG can outperform DGCL with an average 7.38× speedup on GCN computation. This is mainly because 1) MGG can effectively overlap the computation and the fine-grained remote memory access, whereas DGCL has to fully complete the communication for fetching the remote neighbor embeddings before its local neighbor aggregation computation starts. And 2) our hierarchical workload management strategy can maximize the utilization of the available GPU resources, whereas DGCL relies on the offline-optimized single-GPU kernel design that cannot adapt towards different GNN inputs. Another evident drawback of the DGCL is its extremely long data prepossessing time (Table 4 at Column-2) which limits its practical usage in many real-world settings. This is because DGCL requires applying its dedicated algorithm to generate communication-optimized partitioning and device mapping for each input graph. This algorithm comes with high overhead, making their design scales poorly when the incoming graph is large. In contrast, the graph partition and workload balancing in our MGG design is lightweight, which is much faster (more than 100× speedup) compared with DGCL during the graph preprocessing phase.

5.3. Additional Studies & Analysis

Neighbor Partitioning We compare MGG with a baseline design without applying the neighbor partitioning technique (i.e., each aggregation workload consists of all local/remote neighbors) on 4 GPUs. We apply the workload interleaving for both implementations and fix the warp-per-block size to 2 to eliminate the impact from other performance-related factors. Figure 9(a) shows higher latency (3.47× on average) for designs without applying neighbor partitioning, since the workload imbalance becomes more severe across different warps without neighbor partitioning, especially for those graphs with many remote access demand, leading to limited computing parallelism and underutilization of GPU resources.

Workload Interleaving We also compare MGG with a baseline design without workload interleaving (i.e., remote neighbor aggregation and local neighbor aggregation are mapped separately to the GPU warps. We fix the size of the neighbor partition to 16 and the warp-per-block size to 2. Figure 9(b) shows that MGG consistently outperforms the non-interleaved baseline with an average of 1.32× speedup. Since without interleaving the local/remote workload, the workload distribution would be highly skewed, where the heavy and intensive remote aggregation would be gathered on certain warps close to each other while the lightweight local aggregation would be gathered on some other warps close to each other. This leads to inflexible warp scheduling and higher latency.

Modeling and Optimization We further analyze the effectiveness of our lightweight analytical model for design space search. Specifically, three key parameters are studied, the size of neighbor partitioning, the interleaving distance, and the warps per block. Specifically, we consider three different settings: I: Reddit GCN on 4×A100 as the basic setting. II: Reddit GCN on 8×A100 to demonstrate the adaptability toward the different number of GPUs. III: Reddit GCN on 4×V100 [42] to demonstrate the adaptability toward the different types of GPUs. As shown in Figure 10, we decompose searching results into two parts corresponding to the output of the second and third step of the optimization discussed in §4: 1) searching for the “optimal” combination of partition size (ps) and interleaved distance (dist). The initial value of ps, dist, and wpb is set to all ones; and 2) searching for the “optimal” value of warp-per-block (wpb) based on the ps and dist. ps could be adjusted if necessary depending on specific problem settings and here we show the final value of ps for simplicity. From the result, we observe that our performance modeling and parameter selection strategy can pinpoint the low-latency design for the above three settings. The overall searching process only requires about 10 iterations to reach final “optimal” settings. Note that in this study, we show latency results for all possible settings for comparison to our
Accuracy would make significant profit gains when deploying services at scale while the latency penalty is relatively minor for non-sampling GNNs.

6. Discussion

Graph Partitioning: Our NVSHMEM-based designs/optimizations could also support other graph partitioning strategies from prior graph processing and GNN work. There are several major categories. 1) Locality-driven partitioning (e.g., Rabbit order [3]) minimizes the communication/synchronization cost in distributed graph processing/GNN computing. MGG can effectively accommodate such reduced-communication cases through dynamic kernel re-configuration (e.g., finetuning the interleaving distance and warp-to-block mapping) to maximize the communication and computation efficiency. 2) Workload-driven partitioning (e.g., NeuGraph [34]) balances the irregular graph/GNN workload among different devices. Our current design be easily adapted to handle such cases by inserting device synchronization primitives (NVSHMEM collective communication primitives, such as nvshmem_float_sum_reduce) for maintaining data consistency among different replicas.

Application Generality: Besides our current demonstration on GNN-based computation, our design could also be generalized to other applications and hardware platforms. For instance, in the deep-learning recommendation model (DLRM) [58, 21], the large embedding tables could be partitioned by rows/columns and stored in shared multi-GPU memory space and training/inference embedding access queries can be evenly distributed among GPUs for balancing workload. Our pipelined design could be used to overlap embedding collecting and the embedding interaction with associative operators (e.g., sum/min/max reduction) to reduce the overall computing latency and improve system utilization. However, for embedding iterations with non-associative operators (e.g., concatenation with orders), such computation-communication overlapping design would be less effective due to the necessary synchronization to guarantee the output correctness.

Hardware Generality: Our design can also be adapted toward other hardware platforms with similar communication support. For instance, on the multi-CPU based platform with OpenSHMEM [6], our current GPU kernel design can be rewritten as regular C++ functions mixed with OpenSHMEM primitives (in place of NVSHMEM primitives) to be executed on CPU-based distributed platforms. On the CPU, since there is no notion of thread warp/block, the program mainly relies on thread/process-level parallelism. Thus, we need to determine the runtime configurations (e.g., the total number of CPU threads) so that we can balance the computation parallelism and the computation-communication pipelining efficiency. We need to do additional profiling to get the relative latency cost of computation and communication on multi-CPU platforms and adjust the way/pattern of overlapping the computation and

Table 5: Accuracy-Latency of GNNs w/ and w/o sampling.

| Dataset | Accuracy w/ sampling | Accuracy w/o sampling | Latency (w/o vs. w/sampling) |
|---------|----------------------|-----------------------|-----------------------------|
| RDD     | 0.937                | 0.957                 | 1.07×                       |
| PROT    | 0.776                | 0.825                 | 1.25×                       |

searched design points. Whereas in the actual cross-iteration optimization phase, we only need to traverse a small part of the whole design space. By comparing the final optimal runtime configuration setting and the initial configuration, we can see that modeling and cross-iteration optimization can decrease the execution time by up to 68%. In the end-to-end GNN training which usually consists of more than 100 iterations, such a latency saving in the later iterations would also be significant. This experimental study demonstrates the effectiveness of our analytical modeling in assisting parameter selection.

Accuracy-latency Tradeoff This study will analyze the accuracy-latency tradeoff between GNNs w/ and w/o sampling on 8 × A100. Table 5 shows an evident node classification accuracy increase (2% to 5%) of GNN w/o sampling over GNN w/ sampling. The accuracy of sampling-based GNN would be affected by many factors (e.g., sampling rate at each GNN layer and graph structure). Therefore, it is highly tricky to choose the “optimal” value for those factors. Here we follow the conventional way for GNN sampling [50]. The accuracy difference agrees with previous GNN algorithmic work [23]. In many real-world applications (e.g., e-commerce), such an accuracy advantage of non-sampling GNN would be much more favorable to users. This is because even 1%
communication (e.g., the interleaving distance).

7. Conclusion

In this paper, we introduce MGG, a novel multi-GPU system design and implementation to exploit the potential of GPU-based software pipeline for accelerating GNNS. MGG consists of a pipeline-aware workload management technique to tackle irregular GNN workload, a highly optimized pipeline-centric kernel to effectively overlap the decoupled communication and computation, and lightweight analytical modeling and optimization heuristics to dynamically improve the GNN run-time performance. Comprehensive experiments demonstrate that MGG outperforms state-of-the-art multi-GPU systems across various GNN settings: on average 7.38× faster than multi-GPU systems with a unified virtual memory design and on average 3.65× faster than multi-GPU systems with a unified virtual memory design and on average 3.65× faster than DGCL framework.

References

[1] AMD. Rcm communication collective library (rccl). github.com/ROCmSoftwarePlatform/rccl.
[2] AMD. Rcm openshmem. github.com/ROCm-Developer-Tools/ROC_SHMEM.
[3] J. Arai, H. Shikawa, T. Yamamuro, M. Onizuka, and S. Iwamura. Rabbit order: Just-in-time parallel reordering for fast graph analysis. In 2016 IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2016.
[4] Zhenkun Cai, Xiao Yan, Yidi Wu, Kaihao Ma, James Cheng, and Fan Yu. Dgcl: an efficient communication library for distributed gnn training. In Proceedings of the Sixteenth European Conference on Computer Systems (EuroSys), pages 130–144, 2021.
[5] Zixian Cai, Zhengyang Liu, Saeed Maleki, Madanlal Musuvathi, Todd Mytkowicz, Jacob Nelson, and Olli Saarikivi. Synthesizing optimal collective algorithms. In Proceedings of the 26th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PoPP), pages 62–75, 2021.
[6] Barbara Chapman, Tony Curtis, Swareep Pophale, Stephen Poole, Jeff Kuehn, Chuck Koelbel, and Lauren Smith. Introducing openshmem: Shmem for the pgas community. In Proceedings of the Fourth Conference on Partitioned Global Address Space Programming Model, PGAS 10, 2010.
[7] Heinchun Chen, Xin Li, and Zan Huang. Link prediction approach to collaborative filtering. In Proceedings of the 5th ACM/IEEE-CS Joint Conference on Digital Libraries (JCDL), IEEE, 2005.
[8] Jie Chen, Tengfei Ma, and Cao Xiao. Fastgcn: fast learning with random-walk based graph embedding. In Proceedings of the 25th ACM SIGKDD Conference on Knowledge Discovery & Data Mining, pages 685–695, 2021.
[9] Zhihao Jia, Sina Lin, Mingyu Gao, Matei Zaharia, and Alex Aiken. Improving the accuracy, scalability, and performance of graph neural networks with roc. In Proceedings of the 3rd MLSys Conference, 2020.
[10] Thomas N Kipf and Max Welling. Semi-supervised classification with graph convolutional networks. In ICLR, 2017.
[11] Jérôme Kunegis and Andreas Lommatzsch. Learning spectral graph representations on Knowledge graph learning at scale. In Proceedings of the 46th International Conference on Knowledge Discovery and Data Mining (SIGKDD), 2020.
[12] Swapnil Gandhi and Anand Padmanabha Iyer. P3: Distributed deep graph learning at scale. In Proc. 15th USENIX Symposium on Operating Systems Design and Implementation (OSDI 21), pages 551–568. USENIX Association, July 2021.
[13] Prasun Gera, Hyojong Kim, Piyush Sao, Hyesoon Kim, and David Bader. Traversing large graphs on gpus with unified memory. Proceedings of the VLDB Endowment, 13(7):1119–1133, 2020.
[14] Aditya Grover and Jure Leskovec. node2vec: Scalable feature learning on large networks. In Proceedings of the 22nd ACM international conference on Knowledge discovery and data mining (SIGKDD), 2016.
[15] Mark Hempstead, Bill Jia, Hsien-Hsin S. Lee, Andrey Malevich, Dheevadhara Mudigere, Liang Xiao, Rami Melhem. Adaptive page migration for irregular data-intensive applications under gpu memory oversubscription. In 2020 IEEE International Parallel and Distributed Processing Symposium (IPDPS), pages 451–461.
[16] Debashis Ganguly, Saurav Bhattacharya, and M. Baig. A broader picture of graph neural networks with roc. In Proceedings of the 3rd MLSys Conference, 2020.
[17] Prasun Gera, Hyeji Kang, and Rami Melhem. Interplay between hardware prefetcher and page eviction policy in cuda-gpu unified virtual memory. In Proceedings of the 46th International Symposium on Computer Architecture (ISCA), pages 224–235, 2019.
[18] Debashis Ganguly, Ziyu Zhang, Jun Yang, and Rami Melhem. Interplay between hardware prefetcher and page eviction policy in cuda-gpu unified virtual memory. In Proceedings of the 46th International Symposium on Computer Architecture (ISCA), pages 224–235, 2019.
[19] Gaia Bresolin, Michele Zorzi, and Federico Fagnani. A broader picture of graph neural networks with roc. In Proceedings of the 3rd MLSys Conference, 2020.
[20] Prasun Gera, Hyeji Kang, and Rami Melhem. Interplay between hardware prefetcher and page eviction policy in cuda-gpu unified virtual memory. In Proceedings of the 46th International Symposium on Computer Architecture (ISCA), pages 224–235, 2019.
[21] Jie Chen, Tengfei Ma, and Cao Xiao. Fastgcn: fast learning with random-walk based graph embedding. In Proceedings of the 25th ACM SIGKDD Conference on Knowledge Discovery & Data Mining, pages 685–695, 2021.
[22] Zhihao Jia, Sina Lin, Mingyu Gao, Matei Zaharia, and Alex Aiken. Improving the accuracy, scalability, and performance of graph neural networks with roc. In Proceedings of the 3rd MLSys Conference, 2020.
[23] Thomas N Kipf and Max Welling. Semi-supervised classification with graph convolutional networks. In ICLR, 2017.
[24] Jérôme Kunegis and Andreas Lommatzsch. Learning spectral graph representations on Knowledge graph learning at scale. In Proceedings of the 46th International Conference on Knowledge Discovery and Data Mining (SIGKDD), 2020.
[36] Nvidia. Cuda deep neural network library (cudnn). developer.nvidia.com/cudnn.
[37] Nvidia. Dense linear algebra on gpus. developer.nvidia.com/cublas.
[38] Nvidia. Nvidia collective communication library (nccl). developer.nvidia.com/nccl.
[39] Nvidia. Nvidia dgx a100. www.nvidia.com/content/dam/en-xx/Solutions/Data-Center/nvidia-dgx-a100-datasheet.pdf.
[40] Nvidia. Nvidia nsight systems. developer.nvidia.com/nsight-systems.
[41] Nvidia. Nvshmem communication library. developer.nvidia.com/nvshmem.
[42] Nvidia. Tesla v100. www.nvidia.com/en-us/data-center/v100/.
[43] NVIDIA. Unified memory for cuda. developer.nvidia.com/blog/unified-memory-cuda-beginners/.
[44] Bryan Perozzi, Rami Al-Rfou, and Steven Skiena. Deepwalk: Online learning of social representations. In Proceedings of the 20th ACM International Conference on Knowledge Discovery and Data Mining (SIGKDD), 2014.
[45] Erich Strohmaier, Jack Dongarra, Horst Simon, and Martin Meuer. Top500 the list. https://www.top500.org/.
[46] Tomasz Tylenda, Ralitsa Angelova, and Srikanta Bedathur. Towards time-aware link prediction in evolving social networks. In Proceedings of the 3rd workshop on social network mining and analysis, 2009.
[47] Brian Van Essen, Hyojin Kim, Roger Pearce, Kofi Boakye, and Barry Chen. Lbann: Livermore big artificial neural network hpc toolkit. In Proceedings of the Workshop on Machine Learning in High-Performance Computing Environments, MLHPC ’15, New York, NY, USA, 2015. Association for Computing Machinery.
[48] Petar Veličković, Guillem Cucurull, Arantxa Casanova, Adriana Romero, Pietro Liò, and Yoshua Bengio. Graph attention networks. In International Conference on Learning Representations (ICLR), 2018.
[49] Guanhua Wang, Shivaram Venkataraman, Amar Phanishayee, Jorgen Thelin, Nikhil Devanur, and Ion Stoica. Blink: Fast and generic collectives for distributed ml. arXiv preprint arXiv:1910.04940, 2019.
[50] Hanjie Wang, Liuming Gao, Hu Jiang, Quan Gan, Yu Gai, Zhiwu Li, Ziyue Huang, Qipeng Guo, Hao Zhang, Huijin Lin, Junbo Zhao, Jinyang Li, Alexander Smola, and Zheng Zhang. Deep graph library: Towards efficient and scalable deep learning on graphs. ICLR Workshop on Representation Learning on Graphs and Manifolds, 2019.
[51] Yuke Wang, Boyuan Feng, Gushu Li, Shuangchun Li, Lei Deng, Yuan Xie, and Yufei Ding. Gnnadvisor: An efficient runtime system for gnn acceleration on gpus. In USENIX Symposium on Operating Systems Design and Implementation (OSDI), 2021.
[52] wikipedia. Nvidia gpu micro-architecture. en.wikipedia.org/wiki/CUDA.
[53] Frank Wilczek. Qcd made simple. Phys. Today, 53(8):22–28, 2000.
[54] Keyulu Xu, Weihua Hu, Jure Leskovec, and Stefanie Jegelka. How powerful are graph neural networks? In International Conference on Learning Representations (ICLR), 2019.
[55] Rex Ying, Jiaxuan You, Christopher Morris, Xiang Ren, William L. Hamilton, and Jure Leskovec. Hierarchical graph representation learning with differentiable pooling. In The 32nd International Conference on Neural Information Processing Systems (NeurIPS), 2018.
[56] Qi Yu, Bruce Childers, Libo Huang, Cheng Qian, and Zhiyi Zhang. Hierarchical page eviction policy for unified memory in gpus. In 2019 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), pages 149–150. IEEE, 2019.
[57] Haoning Zeng, Hongkuan Zhou, Ajitesh Srivastava, Rajgopal Kannan, and Viktor Prasanna. Graphsaint: Graph sampling based inductive learning method. In International Conference on Learning Representations (ICLR), 2020.
[58] Shuai Zhang, Lina Yao, Aixin Sun, and Yi Tay. Deep learning based recommender system: A survey and new perspectives. ACM Computing Surveys (CSUR), 52(1):1–38, 2019.
[59] Yufeng Zhang, Xueli Yu, Zeyu Cui, Shu Wu, Zhongzhen Wen, and Liang Wang. Every document owns its structure: Inductive text classification via graph neural networks. Proceedings of the 58th Annual Meeting of the Association for Computational Linguistics (ACL), 2020.