Abstract—Responding to the “datacenter tax” and “killer microseconds” problems for datacenter applications, diverse solutions including Smart NIC-based ones have been proposed. Nonetheless, they often suffer from high overhead of communications over network and/or PCIe links. To tackle the limitations of the current solutions, this paper proposes ORCA, a holistic network and architecture co-design solution that leverages current RDMA and emerging cache-coherent off-chip interconnect technologies. Specifically, ORCA consists of four hardware and software components: (1) unified abstraction of inter- and intra-machine communications managed by one-sided RDMA write and cache-coherent memory write; (2) efficient notification of requests to accelerators assisted by cache coherence; (3) cache-coherent accelerator architecture directly processing requests received by NIC; and (4) adaptive device-to-host data transfer for modern server memory systems consisting of both DRAM and NVM exploiting state-of-the-art features in CPUs and PCie. We prototype ORCA with a commercial system and evaluate three popular datacenter applications: in-memory key-value store, chain replication-based distributed transaction system, and deep learning recommendation model inference. The evaluation shows that ORCA provides 30.1–69.1% lower latency, up to 2.5× higher throughput, and ~3× higher power efficiency than the current state-of-the-art solutions.

I. INTRODUCTION

The datacenter network has evolved at a fast pace. Currently, 100 Gbps Ethernet is widely adopted by datacenters, and 400 Gbps Ethernet is not far on the horizon [121]. At these rates, a server may be tasked with processing hundreds of millions of packets per second. However, single-thread performance of CPUs has remained comparatively stagnant, requiring the CPUs to spend more cores and their cycles for network processing— a major component of the “datacenter tax” [79]. Besides, as identified in the “killer microsecond” problem [12] [12], it is not suitable to offload these applications to conventional accelerators such as GPU as they are not efficient to process many small, μs-scale tasks which are common in modern datacenter applications [132]. This makes offloading/acceleration of such μs-scale datacenter applications challenging.

Current solutions for the two problems offload network and/or application processing from the server CPU using one of the three strategies listed in Tab. I. The first strategy is kernel-bypass networking, including user-space stack [14] [62] [71] [132] and two-sided Remote Direct Memory Access (RDMA) [73–78] [99] [128]. It reduces the performance overhead imposed by packets going through the kernel space by delivering the data directly to the user space. Nonetheless, the server CPU still needs to do network processing from the user space (i.e., user-space stack) and application processing (i.e., both user-space stack and two-sided RDMA) that still demand many CPU cores to achieve required performance [75–78] [99] [128]. The second strategy is one-sided RDMA. It allows clients to do application processing as they can bypass the server CPU and directly read from or write to the server memory. However, the limited semantics of one-sided RDMA operations require multiple network round trips to serve a single request from a client. For example, Pilaf [113] performs a key-value lookup by reading a remote hash table to retrieve a pointer, then placing a second RDMA request to read the corresponding data. The third strategy addresses this problem by using a Smart NIC that can perform more sophisticated remote operations in a single network round trip [7] [16] [84] [94] [134] [150] [158]. Nevertheless, such a solution sometimes entails lower performance than the first and second solutions [7] [118] because of two reasons. First, accessing the server memory is inevitable and expensive when the application’s data is not cached in the Smart NIC’s small local memory (Sec. II-B). This is common since modern datacenter applications typically have large working sets, often requiring not only DRAM but even high-capacity byte-addressable NVM such as Intel Optane Persistent DIMM [66] in the host memory system to cost-effectively provide necessary memory capacity [10] [17] [85]. Second, the Smart NIC’s specialized accelerator or energy-efficient but wimpy CPU may not be powerful enough to provide the required end-to-end performance for applications. As such, it needs to participate the (beefy) server CPU for application processing, but it will often require frequent communications between the server CPU and the Smart NIC over slow PCIe links, which becomes a performance bottleneck.

The three strategies above pose a dilemma to system designers: whether to use expensive and precious CPU cores for application processing, or to suffer from the performance overhead incurred by multiple round trips over network or PCIe links. Tackling the limitations of the current solutions, this paper proposes ORCA (Offloading with RDMA and CC-Accelerator), a holistic modularized solution to cost-effectively and efficiently serve μs-scale datacenter applications. Specifically, ORCA proposes a server with a standard RDMA NIC (RNIC) and a cache-coherent accelerator (cc-accelerator) [28] [68] connected to an emerging cache-coherent off-chip interconnect (cc-interconnect) such as CXL [31]. The RNIC, cc-accelerator, and the server CPU work synergistically...
TABLE I: Taxonomy of hardware-based µs-scale datacenter applications offloading/acceleration.

| Optimization | Net. Overhead | PCIe Overhead | CPU Overhead | Flexibility | Perf. | Stability |
|--------------|---------------|---------------|--------------|-------------|-------|-----------|
| Two-sided RDMA/kernel-bypass with multi-core | Low | Low | High | High | Low |
| One-sided/mixed RDMA | High | High | Low | Low | Low |
| (SmartNIC offloading) | Low | Low | Low | Low | Low |
| ORCA | Low | Low | Low | High | High |

ORCA consists of four software and hardware components that are tightly coupled and synergistically interacting with each other to cost-effectively and efficiently serve datacenter applications. Specifically, we propose: (1) a unified abstraction for inter- and intra-machine communications where lockless ring buffers facilitate inter-machine communications with one-sided RDMA write and CPU-accelerator communications with \texttt{load/store}; (2) a fast and efficient mechanism for notification of requests to cc-accelerator exploiting the coherence information exposed to the cc-accelerators; (3) a cc-accelerator architecture for processing the requests and handling interactions among RNIC, CPU and cc-accelerator; and (4) an adaptive device-to-host data transfer mechanism for a server with a heterogeneous memory system consisting of DRAM and NVM.

We prototype ORCA with a commercial system based on an Intel Xeon 6138P CPU that integrates an FPGA device in the same package and communicates with the FPGA device through a UPI link. Subsequently, we evaluate three popular µs-scale datacenter applications: (1) in-memory KVS to show a case fully offloading requests and bypassing the CPU; (2) chain replication-based distributed transaction processing system to show a case considering a latency-sensitive system with NVM; and (3) deep learning recommendation model (DLRM) inference to show a case processing application requests through collaboration between a server CPU and a cc-accelerator. We show that ORCA provides 30.1×–69.1% lower latency, up to 2.5× higher throughput, and ∼3× higher power efficiency than the current state-of-the-art solutions. In addition, we demonstrate that a cc-accelerator with its local memory as part of a server’s unified memory space can further improve the latency and throughput by 11.2% and 62.1×, respectively.

II. BACKGROUND AND MOTIVATION

A. RDMA Primer

RDMA is an advanced kernel-bypass network concept that allows machines to access the memory of remote machines at high bandwidth and low latency. RDMA has now been widely deployed by datacenters [48, 53, 54, 171, 182] and used to build various research and production systems. RDMA offloads the network transport stack and link-layer operations to RNIC hardware and supports one- and two-sided operations that can be accessed directly from the user space. One-sided RDMA operations (e.g., read/write/atomics) completely bypass the remote server’s CPU for remote memory accesses. Meanwhile, two-sided RDMA operations (e.g., send/receive) are similar to conventional network communications (e.g., TCP/UDP) as they involve the CPUs of both clients and servers for data transmission.

The key data structures in RDMA programming are queue pair (QP) and completion queue (CQ), shared between the host (user space) and the RNIC. A QP consists of two work queues (WQs): a send queue (SQ) and a receive queue (RQ), both of which are ring buffers in the host memory. To post an RDMA operation, the user writes to a work queue entry (WQE) at the tail of the WQ with a pre-defined device-specific format and rings the RNIC’s doorbell register using an MMIO write. Upon completion of the RDMA operation, the RNIC (optionally) writes to a completion queue entry (CQE) at the tail of the CQ (also a ring buffer in the host memory) associated with the QP. By polling the CQ, the host can be aware of the completion of operations.

B. Memory Capacity vs. Communication Overhead over PCIe: Dilemma of Using Smart NIC

Recent Smart NICs integrate either FPGA or customized low-profile CPU with NICs. Prior work has shown that Smart NICs running datacenter applications can offer higher performance and energy efficiency than host CPUs [85, 94]. However, Smart NICs have limited memory capacity (O(10 GB)) [101] under cost, power, and form factor constraints. As such, they often need to access the host memory when running applications with large working sets. Unfortunately, such host memory accesses are not cheap, primarily because they must go through PCIe links. Specifically, the PCIe links add non-trivial latency (e.g., at least 1µs) to the access latency of the host memory and can incur performance bottlenecks [118], especially when the Smart NIC needs to frequently synchronize its local memory with or retrieve data from the host memory. This has been identified by multiple system designs [18, 85, 94, 118, 147], and we also observe the same phenomenon on a BlueField-2 Smart NIC; for a Smart NIC application accessing both its...
We depict a high-level system architecture of ORCA, envisioning a system comprising an emerging cc-accelerator, a standard RNIC, and a conventional powerful server CPU, each of which plays indispensable roles for efficient network and application processing. Specifically, (1) the cc-accelerator not only offloads accelerator-friendly part of application processing from the server CPU but also directly communicates with clients through the RNIC, i.e., receiving requests and sending responses from/to clients without involving the server CPU; (2) the standard RNIC handles network processing; and (3) the server CPU tackles accelerator-unfriendly (irregular and branch-rich) part of application processing in addition to initialization, control, and management of hardware resources, applications and network connections. The synergistic orchestrations among (1) – (3) are facilitated by the ORCA’s four software and hardware components described in this section.

### III. ORCA System Architecture

We depict a high-level system architecture of ORCA in Fig. 1. ORCA envisions a system comprising an emerging cc-accelerator, a standard RNIC and a conventional powerful server CPU, each of which plays indispensable roles for efficient network and application processing. Specifically, (1) the cc-accelerator not only offloads accelerator-friendly part of application processing from the server CPU but also directly communicates with clients through the RNIC, i.e., receiving requests and sending responses from/to clients without involving the server CPU; (2) the standard RNIC handles network processing; and (3) the server CPU tackles accelerator-unfriendly (irregular and branch-rich) part of application processing in addition to initialization, control, and management of hardware resources, applications and network connections. The synergistic orchestrations among (1) – (3) are facilitated by the ORCA’s four software and hardware components described in this section.

### A. Inter- and Intra-machine Communication

ORCA proposes a communication abstraction to (1) accomplish fast and efficient communications not only between a server and clients (i.e., inter-machine communications) but also between a CPU and a cc-accelerator in a server (i.e., intra-machine communications) and (2) unify the programming model for both inter- and intra-machine communications, based on lock-free ring buffers. For each client-server connection we establish a pair of a request ring buffer (in the server memory) and a response ring buffer (in the client memory) for inter-machine RDMA communications. One-sided RDMA write is used by both servers and clients for high-performance inter-machine communications through message passing where all the underlying network transport processing is offloaded to the RNIC. For the intra-machine communications, leveraging the shared coherence domain, the server CPU or cc-accelerator directly writes to or reads from the ring buffers.

Note that we do not share the ring buffers (and the underlying RDMA QPs for the inter-machine communications) across different client-server connections, to avoid performance overheads with atomic updates or consistency issues at the head/tail of the buffer without atomic updates. However, we do allow sharing the ring buffers (and the RDMA QPs) across threads on the same machine for better scalability, as a software layer/library can manage cross-thread contentions with slight performance overheads. Specifically, we employ the Flock’s method, i.e., one dedicated thread on the client for request synchronization and dispatch, so that there is only one request-response buffer pair (and QP) per client-server pair per application and observe no performance loss compared to native RDMA primitives.

The client is responsible for tracking the tail of the request buffer in the server memory and the head of the response buffer in its local memory, similar to the credit-based flow control. Whenever it writes a message to the request buffer, it will update its local record of the request buffer’s tail; whenever it receives a message in the response buffer (by polling), it will update its local record of the response buffer’s head and reset the buffer entry to “0”. Only if the request buffer’s tail is behind the response buffer’s head can the client issue a request. Otherwise, it knows that the buffer is full of on-the-fly requests and should not send more requests. A similar mechanism is applied to the server for request buffer’s head and response buffer’s tail. This guarantees that any message can be passed by only one network trip without any conflict.

### B. Coherence-assisted Accelerator Notification

Since a client and a server CPU directly write messages to inter- and intra-machine communication request buffers in the server memory, respectively, the ORCA cc-accelerator needs to proactively get the message from the request
buffers. Typically, a spin-polling mechanism can be deployed. However, the bandwidth of the cc-interconnect and the coherence controller is precious. Frequently polling the request buffers, the cc-accelerator has little bandwidth left for application processing, i.e., accessing the server’s memory to serve requests. Besides, polling has high power consumption [13, 42, 51, 98], fast transistor aging [124], and poor scalability with many queues [51]. Hence, we propose a coherence-assisted notification mechanism, called cpoll.

Conceptually and semantically, cpoll is similar to Mwait in the x86 architecture [64], QMAIT in HyperPlane [111], and PCIe’s lightweight notification (LN) proposal [50, 136]. Nonetheless, cpoll differs from them because it is designed to be portable and platform/CPU-agnostic for off-chip devices. Specifically, we insert a cpoll checker in the datapath of the coherence controller’s port connected to the cc-interconnect. During initialization, we first allocate the inter- and intra-machine communication request buffers (Sec. III-A) in a contiguous address region of the server memory (i.e., cpoll region), and register this region to the cc-accelerator’s cpoll checker for snooping, as depicted in Fig. 2(a). Then, when the cc-accelerator’s coherence controller receives a coherence signal from the registered address region (e.g., Modified → Invalid), it will notify the cc-accelerator of arrival of a request. The cpoll checker will only need to monitor a single address region illustrated in Fig. 2(a). If the address of a coherence signal falls into this region, the cpoll checker can identify which request buffer (associated with a specific client or the server CPU) that received a new request by determining the address offset from the starting address of the region as the size of buffers is fixed after the initialization. Hence, there will be no scalability concern for the cpoll mechanism. Even if the buffers are not allocated consecutively in the memory, the overhead of address lookup should not be a concern as well (to $O(1K)$ level buffers at least), as demonstrated by HyperPlane [111].

To implement the cpoll mechanism, we propose two approaches. First, we allocate the cpoll region to the memory attached to the CPU, and then pin the region on the cc-accelerator’s local cache. Note that the cc-accelerator resets the request buffer entry associated with a cpoll signal after it completes processing the request. This makes the cc-accelerator’s local cache always own the cpoll region from the cache coherence viewpoint, and any change to the cpoll region by clients or the server CPU trigger a coherence signal. Alternatively, we allocate the cpoll region to the memory attached to the cc-accelerator. As such, any request from the RNIC to the request buffers in the server memory space (consisting of CPU and cc-accelerator memory regions) will go through the cc-interconnect. Subsequently, they will be delivered to the cc-accelerator’s coherence controller that is responsible for monitoring any change to the cpoll region.

The first approach is feasible with our prototype platform (Sec. V), but the size of request buffers is constrained by the cc-accelerator’s local cache size, limiting its scalability at the moment. When the scale of the system is large (i.e., many request buffers) or each request itself is large (i.e., large buffers), we cannot pin the entire cpoll region on the cc-accelerator’s cache. To tackle this scalability issue in our setup, we introduce a data structure called pointer buffer where each 4-byte entry corresponds to each inter- or intra-machine request buffer and stores a pointer (or index) to an entry in the request buffer, as depicted in Fig. 2(b). Subsequently, we register the pointer buffer allocated to a contiguous address space as the cpoll region. When writing a new request to a request buffer in the server memory, a client or the server CPU will also increment the value of the pointer buffer entry corresponding to the request buffer such that the pointer buffer entry points to the request buffer tail. For a remote client, this can be efficiently done by posting two contiguous WQEs (only the second one is signaled) with a batched doorbell to the RNIC [77] or remapping/interleaving the two buffers with user-mode memory registration (UMR) [123] and only posting one WQE.

Note that one additional small PCIe write to the server side is inevitable in both ways. However, since ORCA has already reduced the PCIe traffic and mainly leverages the coherence traffic, such overhead will not notably hurt the overall performance, which is confirmed by our experiments in Sec. VI. In addition, as a 4-byte pointer buffer entry covers an entire request buffer, which can be as large as several MBs for some applications such as the one described in Sec. LV-B, it can substantially reduce the memory space requirement for the cpoll region. Finally, coherence signals are not guaranteed to come in the order of actual data writes. However, this does not affect the correctness of cpoll because it is designed to be used with a ring buffer, and leverages the semantics of the ring buffer, i.e., request buffer entries are written in order.

C. ORCA cc-accelerator Architecture

We depict ORCA cc-accelerator architecture in Fig. 3. The coherence controller handles all the coherence traffic (both
regular read/write and cpoll) to/from the cc-accelerator, as well as the virtual-physical address translation (i.e., TLB). The local cache is also in the coherence domain and handled by the coherence controller. The ORCA cc-accelerator may have its own local memory controller and memory [28] [30] that constitutes the unified memory space with the CPU memory. In such an architecture, the CPU may allocate application data to the cc-accelerator’s local memory, as the NUMA-aware memory management does in the modern Linux kernel.

The scheduler fetches cpoll signals associated with different request buffers based on a given scheduling algorithm. Due to the nature of the coherence implementation, cpoll signals can be coalesced. For example, if we update the same entry in the pointer buffer twice in a short period, there can be only one cpoll signal generated. However, leveraging the semantics of the ring buffer, i.e., a pointer value only increments (including mod), we introduce a ring tracker to the cc-accelerator to track the previous tail of the request buffer. It tells the application processing unit (APU) how many new requests are received since the last notification based on the difference between the recorded tail pointer value and the incoming pointer value.

The RDMA SQ handler is responsible for assembling the response information into the format of the RNIC’s WQE and ring the RNIC’s doorbell register in its PCIe BAR. Since polling the CQ is not on the critical datapath, we do not process it with the cc-accelerator. Instead, we use a single CPU core to handle all the CQs polling and bookkeeping. Unsignaled WQE [27] is applied here so that only the selected operations will notify the CQ of their completion. This can alleviate the overhead of RNIC-CPU communication when the CPU is polling multiple CQs. Besides, this helps reduce unnecessary traffic on the cc-interconnect.

The APU is the only application-specific part in the entire ORCA architecture, yielding a fine balance between ORCA programmability and user implementation complexity. It provides the user with standard interfaces for (1) cpoll signal reception, (2) coherent data read/write, and (3) RDMA WQE output. First, a (de)serializer can be optionally used, if the application uses an RPC protocol for inter-machine communications [90]. Then, to process requests, we typically need a data structure walker [52] [86] [105] [173] [176] to find the location of the target data of the request. To maximize the memory-level parallelism and hide the memory access latency, multiple outstanding requests and out-of-order execution should be supported. Inspired by the stateful network function accelerator [137], we employ a table-based finite state machine for this purpose, where the outstanding request status is stored in a TCAM or cuckoo hash table [179] for fast lookup. Upon the arrival of a new request or intermediate result, the corresponding TCAM or hash table entry is updated and then the next-step action is issued to a corresponding functional unit (e.g., ALU or coherence controller).

The APU should invoke the CPU in two scenarios. The first scenario is when a library call or OS syscall is needed. For example, if the user space memory pool has been pre-allocated by the CPU (malloc/mmap), the APU itself can allocate objects for new data in the memory pool [94]; if not, malloc is called each time when a new object is needed. The second scenario is when CPU is more suitable than the APU for a certain part of application processing. For example, in a recommender inference system (see Sec. IV-C), while the APU can handle the embedding reduction and fully-connected layers, the request preprocessing (e.g., transforming a human-readable request to a model input) should still run on the CPU due to its irregularity and complexity. In these scenarios, the cc-accelerator and CPU interact with low latency in a fine-grained manner described in Sec. III-A.

### D. Optimizing Device-host Data Transfer: Adaptive DDIO

Having the ORCA system design, we finally consider the optimization of device-memory-cache interaction inside a single machine, or specifically, how to choose between the cache and memory as the data destination for optimal device-host data transfer. Given the data-intensive nature of ORCA’s usage scenarios, this optimization is notably important for the entire system. As the device I/O speeds increase, Intel introduced data-direct I/O (DDIO) [70], a CPU-wide technology, to allow the device to directly inject data to the CPU’s last level cache (LLC) instead of main memory. This reduces memory bandwidth consumption and latency required by I/O.

DDIO has been proven to be effective [4] [19] [45] [74] [88] [107] [135] [146] [157] [166] [175], improving the performance of DRAM-based systems [4] [19] [88]. However, it does not always improve performance of NVM-based systems [74] [166], which is increasingly deployed by datacenters to cost-effectively provide large memory capacity for applications such as in-memory database [10] [17]. This is mainly because of two reasons. (1) NVM has a larger access granularity than DRAM and cache. For example, the access granularity of the Intel Optane DIMM is 256 bytes while that of DRAM and cache is 64 bytes in Intel-based system [172]. When the DDIO-ed data is evicted from LLC to NVM, the write-back to the NVM will be randomized because of the cache replacement policies. As a result, write amplification wastes the bandwidth of NVM [74], which is already lower than that of DRAM. (2) CPU caches are typically not persistent; Intel eADR [63] makes cache as part of the persistency domain but it requires a large battery and has high power consumption [6] [15]. As such, applications often have to flush data in cache to NVM to remain correct in case of a crash, with performance cost [155].

To tackle the aforementioned limitation, we propose to exploit a rarely-discussed field in the PCIe packet header, TLQ processing hints (TPH). It is the 16th bit in the PCIe header and a

![Fig. 4: Memory bandwidth consumption by PCIe-bench’s DMA write with different DDIO/TPH settings.](image-url)
Fig. 5: DDIO/TPH configurations in the system with NVM.

performance feature that allows the CPU to prefetch or keep certain PCIe writeback data in LLC for quick consumption by CPU cores [125]. To our best knowledge, no current commercial I/O device (including SSD and NIC) uses the TPH bit; it is always set to 0 as a placeholder in both hardware and device drivers.

Our experiment confirms that changing the TPH bit allows us to control the destination of data to either LLC or memory per PCIe packet. Being the first to clarify the DDIO-TPH relationship with modern server platforms, we perform an experiment running PCIe-bench [118] on a Xilinx VC709 FPGA board [170] in which we implement a module that allows an API to set the TPH bit on-the-fly for each PCIe packet. The FPGA DMAs (random write) data to the (DRAM-based) host at a constant speed of 3.5GB/s. We measure the memory bandwidth consumption on the host side in four configurations (DDIO on/off + TPH on/off) in Fig. 4. Only when both DDIO and TPH are off, we observe large memory bandwidth consumption (i.e., ~3.5GB/s for both read and write), which is aligned with the DMA throughput reported by the FPGA. This indicates that all DMA data is sent to the main memory. Otherwise, if either DDIO or TPH is on, there will be little memory bandwidth consumption, meaning data is sent to the LLC directly.

Since TPH is applicable to each PCIe packet, we propose two guidelines for future systems with heterogeneous memory, as depicted in Fig. 5. (1) DDIO should be disabled globally on the CPU by default. (2) The device should expose the knob of changing the TPH bit for the programmer. Taking RNIC as an example, one way to do this would be to make it a configuration parameter set when registering a memory region as an example, one way to do this would be to make it a configuration parameter set when registering a memory region (DDIO on/off + TPH on/off) in Fig. 4. Only when both DDIO and TPH are off, we observe large memory bandwidth consumption (i.e., ~3.5GB/s for both read and write), which is aligned with the DMA throughput reported by the FPGA. This indicates that all DMA data is sent to the main memory. Otherwise, if either DDIO or TPH is on, there will be little memory bandwidth consumption, meaning data is sent to the LLC directly.

Upon arrival of a request, a hash value is calculated based on the requested key. Based on the hash value, a specific hash table entry/bucket is accessed for data retrieval/update/insert. To avoid hash collisions, chaining [99] or cuckoo hashing [43] can be leveraged, both of which often increase the number of memory accesses. In addition to software optimizations, researchers have leveraged all the three directions mentioned in Sec. I and Tab. I for further KVS acceleration. The major requirements of KVS is high memory access parallelism across requests.

An ORCA design for KVS, dubbed ORCA KV aims to fully offload request processing to the cc-accelerator. At the algorithm/data structure level, ORCA KV is similar to MICA [99], but ORCA KV follows the architectural description of Sec. II-C at the hardware level, including a pipelined hash unit for hash value/index calculation. ORCA KV performs a GET/UPDATE request by calculating the hashed key value and finding the corresponding entry in the set-associated hash table’s bucket. The entry contains a pointer to the actual key-value data. For PUT requests, after finding the address where a new key-value pair should be allocated (i.e., an empty entry in the bucket), the slab allocator will simply put it in the pre-defined memory pool. If the bucket indexed by the hashed key is full (i.e., hash collision), another bucket with the same format will be allocated and linked to the existing bucket by a pointer. Similar to KV-Direct [94] and MICA [99]’s study, on average, each GET request requires three memory accesses and each PUT request requires four.

B. Distributed Transaction with NVM-based Chain Replication

Distributed transactional systems are widely used by datacenters to provide the ACID feature for distributed storage systems. To this end, cross-machine protocols for data replication is usually needed, and chain replication [5] [8] [11] [21] [40] [49] [110] [116] [126] [133] [143] [154] [156] [160] [180] is a popular primary-backup replication protocol. In chain replication, machines are virtually organized into a linear chain. Any change to the data will begin at the head of the chain and pass through the chain. When the last machine in the chain makes the change in its log, it will back-propagate the ACK signal through the chain so that each machine can locally commit the transaction. When the head of the chain commits the transaction, it sends the ACK signal back to the client, marking the end of the transaction.

The state-of-the-art work, HyperLoop [84], leverages the RNIC and NVM to achieve low-latency chain replication with little CPU involvement. Specifically, it proposes and implements group-based RDMA primitives, which can be triggered
automatically by the RNIC. One key-value pair (addressed by the offset in the NVM space) is modified in the entire chain once the client initiates a group-based RDMA operation. However, to process multi-value transactions, the client needs to sequentially issue RDMA operations for each key-value pair, which often leads to long latency in the network and PCIe link.

An Orca design for such a distributed transaction system, dubbed Orca TX is similar to Orca KV with respect to request processing, but it additionally implement a concurrency control unit in the APU. That is, any single key-value pair can only be accessed by one outstanding transaction, and the other related transactions will be buffered in the queue in the order of arrival. The concurrency control unit is a small hash table, and its entries are indexed by the key of the key-value pair. Key-value pairs are stored in the NVM and accessed by the address offset relative to the starting address, which is the same as HyperLoop. Also, it adds the functionality of chain-based communication across replica machines. The inter-machine communications still rely on ring buffers described in Sec. II-A but the ring buffers are allocated in the NVM as the redo-log for failure recovery. One log entry (transaction) can contain multiple (data, len, offset) tuples, and the first byte of the log entry indicates the number of tuples. One exception is pure read transactions. Similar to HyperLoop, since the chain replication protocol already provides data consistency, a client can conduct a pure read transaction by directly accessing the chain’s head/tail machine with one-sided RDMA read.

C. DLRM Inference

DLRMs have received much attention by Internet giants [2, 24, 56, 57, 58, 82, 117] as they can offer more revenue and better user experience. In an end-to-end recommender system, the most expensive part of serving an inference request is the embedding reduction step, consuming huge memory capacity [117, 177, 178] and $\frac{1}{2}$ – $\frac{3}{4}$ of the inference time [38, 58, 60, 82, 92]. The embedding reduction operation processes queries on a set of features. It finds a (sparse) embedding vector in the embedding table (a high-dimension matrix) and aggregates a value. The values of all features are assembled as the result. Also, the embedding reduction is bounded by memory bandwidth and exhibits poor data locality [82, 92]. Last but not least, it also incorporates routines like request parsing and transforming (pre-processing), which are irregular and branch-rich. As such it is not suitable for hardware accelerators. These characteristics make it unsuitable, if not impossible, to be fully offloaded to any Smart NIC or cc-accelerator. In addition to acceleration with specialized hardware like in-memory processing [9] [82, 89, 131], MERCI [92] takes an algorithmic way to memoize sub-query grouped results to reduce memory pressure on the commodity server platform.

Different from Orca KV and Orca TX, we design Orca DLRM as an example of CPU-accelerator collaboration for request processing. Upon receiving a request from a client, the cc-accelerator first goes through the RPC stack, and then pass the request to the CPU through the ring buffer, where the request is parsed and transformed to model-ready input. Now, the input (request) is passed again to the cc-accelerator’s APU, where the full inference, especially embedding reduction, is done. Finally, the cc-accelerator sends result (response) back to the client through the RNIC. Empirically, we observe that one CPU core with 60% usage can already keep up with the network and the cc-accelerator processing rate. In DLRM, not all memory accesses in a single query need to be serialized. Hence, in the APU, we issue 64 memory requests for each query’s iteration so that the memory bandwidth can be fully utilized and the memory access latency can be hidden. Lastly, the ALU is enhanced to support various aggregation operators (e.g., max/min/inner product).

V. ORCA IMPLEMENTATION AND EVALUATION SETUP

We prototype Orca with a commercial system consisting of two Intel Xeon Gold 6138P CPUs at 2.0GHz [68] and 192GB DDR4 memory. The configurations of the system are listed in Tab. II. Specifically, we use the in-package FPGA (Intel Arria 10GX@400MHz [65]) of the CPU to implement the cpoll mechanism and a cc-accelerator. The FPGA has a 64KB local cache and is connected to the CPU through a UPI link, typically used in NUMA systems to connect CPUs. The UPI link has one read channel and one write channel, each with 10.4GT/s bandwidth. It can also issue sfence signal and cpoll message. For intra-machine communication, since HyperPlane’s qwait and x86’s user space mwait is unavailable on our platform, we use spin-polling for CPU to fetch requests in the request ring buffers from the cc-accelerators.

We implement a round-robin algorithm in the scheduler. The APU can support 256 outstanding requests. Each request buffer has 1024 entries. We adopt the HERD’s RPC protocol [76, 77] for its simplicity, but any advanced RPC stack can also be applied [90]. The resource utilization numbers in Tab. II reflect our Orca key-value store accelerator (Sec. IV-A). The utilization results for the other applications we have built are similar, because ~80% of used resource is for the coherence controller and the local cache, which are common components.

The current implementation has two major limitations. The first one is the performance of the coherence controller. As a soft design in the programmable fabric of the FPGA, it suffers...
from synthesis constraints and can perform at most 400 MHz, incurring limited data access performance, which has also been observed by prior work \cite{90}). However, its counterparts on a regular server CPU can operate at \(\sim 2\) GHz \cite{1}. We expect such infrastructural parts can be fixed by hard IPs in the future FPGA, offering performance of the accelerator’s coherence controller comparable to that of the CPU’s \cite{67}. The second is that the FPGA lacks local memory that exists in the same coherence domain and has comparable capacity to CPU-attached memory. Consequently, most memory requests for application request processing will need to go through the cc-interconnect (due to the large working set of the target applications), similar to cross-NUMA memory access. Besides, the cpoll region must be pinned in the cc-accelerator’s local cache. We expect that such limitations will be effortlessly tackled when ORCA is implemented in CXL-based devices \cite{30} or Enzian \cite{28}.

Since the in-package FPGA is not extendable, to explore the potential of ORCA’s performance on future platforms, we also use a stand-alone Xilinx U280 FPGA card \cite{169} with 32 GB DDR4 memory and 8 GB HBM2 to emulate a cc-accelerator with local coherent memory \cite{28,30}. Prior work \cite{162} has shown that these two types of memory can achieve \(\sim 36\) GB/s and \(\sim 425\) GB/s throughput, respectively. Specifically, we adapt the APU to the U280 card with either DDR4 or HBM2 controller. The application data is mapped and initialized in the FPGA’s local memory. Rather than interacting with a real RNIC, we emulate arrival of RDMA requests by generating requests within the FPGA with the RDMA write rate measured on the testbed. We believe this emulation methodology offers correct and convincing results since coherence (of the application data) makes no big difference here after the data has been allocated and initialized in the FPGA-attached memory; during request processing, most memory traffic does not need to go across the cc-interconnect. For throughput experiments, we measure requests processed on the FPGA per second. For latency experiments, we compute the emulated end-to-end latency by combining application processing time measured on the U280 with the average latency of the rest of the stack. Specifically, we measure the average latency from a request’s generation to its completion on the U280, then add the average full-system end-to-end latency without an APU – measured on the client machine. Note that this approach emulates average latency, so does not apply to tail latency measurements. In the following sections, we note the U280 DDR4-based results as “ORCA-LD (local DDR4)” and HBM2-based results as “ORCA-LH (local HBM2)”.

Lastly, we use the NVIDIA ConnectX-6-based BlueField-2 DPU \cite{122} as the RNIC. It also provides eight ARM A72 cores at 2.5 GHz, which we use to compare against a conventional Smart NIC approach.

VI. EVALUATION

A. Notification Latency: cpoll vs. Conventional Polling

To demonstrate the advantage of cpoll over conventional spin-polling, we perform a local ping-pong test. Specifically, we allocate a 1 KB request buffer shared between the CPU and the FPGA. The CPU first starts a timer to measure round-trip latency, writes the buffer’s first byte, and then spins to poll the buffer’s last byte. After detecting a change in the last byte, the CPU stops the timer. The FPGA polls or cpoll the buffer’s first byte. When it detects any change in the first byte, it immediately writes the buffer’s last byte. With this setup, we test cpoll and polling with different polling intervals in FPGA cycles for 60K times. This is to measure notification latencies perceived by (1) the FPGA when the CPU sends a request with both cpoll and polling and (2) the CPU when the FPGA sends a request with polling.

We plot the one-direction CPU-to-FPGA latency CDF in Fig. 7. First, cpoll always has a better average and tail latency than conventional polling, which can be as high as \(\sim 30\%\). Second, cpoll consumes less bandwidth of the interconnect (UPI in our case). Take polling-15 (15 FPGA clock cycles per polling) as an example: it may generate \(64B \times 400\) MHz/15 \(\approx 1.6\) GB/s traffic on the UPI link and coherence controller for a single request buffer, which affects the normal operations of the applications. Note that due to the frequency limitations of the FPGA, the latency’s absolute value is not extremely low. Since the UPI link may only consumes \(~50\) ns latency \cite{151}, we expect that the coherence controller in the FPGA can be a hard-IP in future products to achieve higher performance \cite{67}.

B. In-Memory Key-Value Store

Due to the limited availability of devices, we run ORCA KV on one server and one client \cite{62} see Sec. VII for scalability discussion. We compare ORCA with two state-of-the-art baselines: open-source two-sided RDMA-RPC (MICA-backed) \cite{76,77} (noted as “CPU”) and Smart NIC \cite{94,150}. For CPU, we use ten threads (cores) on the testbed to maximize the KVS throughput. Each thread is fed with requests by one client instance (each with two dedicated Skylake cores) on the client machine (also equipped with the BlueField-2 DPU). For ORCA, we also use 10 client instances to feed requests that are processed on the same ORCA accelerator. For Smart NIC, we use DPU’s all eight ARM cores to emulate the behavior of the specialized hardware in KV-Direct \cite{94} and StRoM \cite{150}. The ARM cores process the request, which is sent from the client Intel CPU by RDMA. Besides, the ARM cores communicate with the server host through RDMA (direct verbs) for necessary data

\[\text{Fig. 7: Latency distribution of cpoll and conventional polling with different polling intervals (cycles).}\]
Throughput (Mrps)

Throughput (Mrps)

Latency (us)

| Batch Size | Smart NIC | CPU | ORCA | ORCA-LD | ORCA-LH |
|------------|-----------|-----|------|---------|---------|
| 1          | 0         | 5   | 0    | 0       | 0       |
| 4          | 10        | 10  | 15   | 20      | 20      |
| 16         | 20        | 20  | 25   | 30      | 30      |
| 32         | 40        | 40  | 50   | 50      | 50      |

Fig. 8: Peak throughput performance of different KVS designs. The batch size of 32 is applied.

The batch size of 32 is applied.

Latency (us)

| Batch Size | Smart NIC | CPU | ORCA | ORCA-LD | ORCA-LH |
|------------|-----------|-----|------|---------|---------|
| 0          | 10        | 20  | 25   | 30      | 30      |
| 10         | 20        | 30  | 35   | 40      | 40      |
| 50         | 50        | 60  | 65   | 70      | 70      |
| 100        | 100       | 110 | 115  | 120     | 120     |

Fig. 9: Latency performance of different KVS designs on the 100% GET workload. The batch size of 32 is applied. ORCA-LD/LH’s tail latency is inapplicable.

Fig. 10: The impact of batch size on throughput and latency (100% GET workload, Zipfian 0.9 distribution). ORCA-LD/LH’s tail latency is inapplicable.

that the request distribution significantly affects Smart NIC’s performance. Smart NIC’s throughput with uniform distribution (i.e., more than 90% memory accesses are to the host via PCIe) is 27.2%–28.6% of that with a skewed Zipfian distribution (i.e., most memory accesses are local). And even the throughput with Zipfian distribution is only ∼60% of that with pure on-board memory accesses. On the other hand, the distribution does not affect CPU and ORCA’s performance, since even with the Zipfian distribution, the KVS’s memory footprint is still larger than the CPU or FPGA’s cache. Second, we observe that ORCA’s peak throughput is 2.3%~8.3% higher than CPU. This is because the peak KVS throughput is bounded by the network bandwidth now, and ORCA’s one-sided RDMA performs a little better than CPU’s two-sided RDMA, which is aligned with prior studies [75, 120]. The throughput of ORCA-LD and ORCA-LH can prove this as well – extra memory bandwidth does not help improve the performance (in fact, the UPI link is not saturated), since the network has reached its limit.

Regarding the latency, taking the 100% GET workload as an example (Fig. 5), the Smart NIC’s performance is again affected by the request distribution, since the PCIe link adds significant latency, even if the accesses are batched. Meanwhile, we observe that ORCA’s average latency is a bit higher than CPU. This is mainly because, unlike CPU, ORCA needs to access data through the UPI link, adding more time on the request processing critical path. This deficiency is overcome with ORCA-LD/LH’s accelerator-attached memory – it only goes through the UPI to interact with the RNIC. Note that due to HBM’s nature, ORCA-LH has a higher average latency than ORCA-LD since the workload is not bounded by memory bandwidth now. For tail latency, ORCA is 52.0% lower than Smart NIC and 30.1% lower than CPU, because it not only significantly remove the PCIe overhead, but also has more stable behavior than the CPU core, whose performance is affected by multiple factors like OS scheduling and CPU resource contention.

We also investigate the impact of the batch size on each design and demonstrate the results in Fig. 10 (since the KVS throughput is now network-bound, we do not include ORCA-LD/LH’s throughput as they are the same as ORCA). For CPU and Smart NIC, batching can significantly improve their throughput performance (i.e., ∼12×) – by batching the data accesses across requests, the memory bandwidth is efficiently utilized and the memory/PCIe latency is hidden.

retrieval. Admittedly, the ARM core is not as efficient as the specialized FPGA designs [94, 150] when processing KVS and accessing host memory. However, the ARM cores’ frequency is ∼10× higher, alleviating the efficiency gap. Also, we use direct verbs [142] to minimize the overhead imposed by the RDMA software stack. Based on our measurement, when running KVS entirely on the Smart NIC’s on-board DRAM, the eight ARM cores’ peak throughput is equivalent to six Intel CPU cores.

We pre-load 100M key-value pairs (64 B size, ∼7 GB memory in total) and then access them using uniform and Zipfian 0.9 distributions. We test two types of workloads: read-intensive (100% GET), and write-intensive (50% GET, 50% PUT). Note that the MICA-based mechanism [76, 77], which we use in this experiment, eliminates the concurrency issue (i.e., only allowing the “owner core” to read/write the data partition). As such, the performance of heavy PUT workload does not differ much from the GET only workload, which is aligned with the results in prior work [77, 94].

In CPU and ORCA, both the hash table and key-value pairs are stored in the host memory; in Smart NIC, we allocate a 512 MB space on the DPU’s on-board DRAM as the cache to store the most recently accessed hash entries and key-value pairs. The cache-total ratio (512 MB : 7 GB) is roughly the memory capacity ratio (16 GB : 192 GB). We also test the impact of batching. In CPU and Smart NIC, batching means processing requests in a batch to improve the memory access efficiency [99]. In ORCA, since the APU can already exploit the memory-level parallelism across requests [86, 105, 173, 176], there is no need for request batching. Hence, we batch the doorbell signals to the RNIC [77] when posting RDMA operations for response. These settings and configurations resemble prior work [77, 90, 94, 99].

We first show each design’s peak performance (with batch size 32). Regarding the throughput in Fig. 8 we first find...
TABLE III: Overall power efficiency of different KVS approaches with GET operations in uniform distribution.

|       | CPU       | Smart NIC  | ORCA |
|-------|-----------|------------|------|
| Kop/W | 130.4     | 25.2       | 188.7|

ORCA’s throughput also benefits from batching \((i.e., \sim 2\times)\), which is because of the reduction of MMIO-based doorbell access \([3] [47] [77]\), and MMIO’s surrounding \textit{s}fence signals from the ORCA cc-accelerator, which is relatively expensive. On the other hand, unlike CPU and Smart NIC, ORCA’s latency sub-linearly increase with the batch size. This is because ORCA does not need to wait for the batch size of arrived requests to start processing, and the RNIC may execute the WQE promptly before the doorbell is rang \([108]\).

Finally, we use Intel RAPL interface \([130]\) (for CPU and DIMMs), IPMI tool (for the entire server box), and the FPGA’s firmware (for the FPGA chip) to measure the power consumption of the evaluated approaches. Take the case in Fig. 8 as an example. We find that the CPU and Smart NIC’s Intel/ARM CPUs consume \sim 90 Watts and \sim 15 Watts respectively when fully loaded, while ORCA’s FPGA power is in the range of 24–27W to achieve the peak throughput. This demonstrates ORCA cc-accelerator’s \sim 3\times power efficiency than the beefy Intel CPU to achieve comparable performance, leading to \sim 38\% power consumption reduction of the entire server box, as demonstrated in Tab. III.

C. Distributed Transaction with NVM-based Chain Replication

According to the HyperLoop paper \([84]\), HyperLoop mechanism always outperforms CPU-based chain replication implementations, especially in the multi-tenant cloud environment, so we compare ORCA only with HyperLoop. Same as the HyperLoop paper, we adopt RocksDB \([41]\), a persistent key-value database, to use the NVM as the persistent storage medium and to apply ORCA and HyperLoop. Since HyperLoop modifies RNIC’s firmware, which is not open-source, we use the ARM cores on the DPU to emulate its behavior. Since the (Skylake) CPU with in-package FPGA does not support Intel Optane DIMM, we emulate NVM’s behavior by adding latency and throttling memory bandwidth in the FPGA and the ARM emulation program. We follow the NVM’s characteristics in recent Optane-based studies \([74] [72]\) to calibrate our emulation. We disable DDIO on the server.

Having the same device limitation, we run the experiments on one client and one server. We make use of the two ports on the DPU to have two replica machines (instances) in the same physical server, and the transaction will be forwarded across the two ports, as shown in Fig. 9. The client’s host CPU will initiate a transaction and send it to the server’s port 0 (1). The corresponding processing unit instance (either a DPU ARM core or ORCA) will forward the transaction to the client’s DPU ARM via port 0, which is attached to a RocksDB instance (2). The client’s DPU ARM simply routes the transaction to the server’s port 1, where another RocksDB instance (and the corresponding processing unit) serves as the second replica machine (3). Finally, the transaction will be sent back to the client’s host CPU (4). According to our measurement, the ARM-based routing will add 2~3\mu s overhead, which resembles the network latency in the real datacenter.

We initiate the RocksDB instance with 100K key-value pairs and issue 100K transactions from the client to measure the end-to-end latency. We test two key-value pair sizes (64B and 1024B) and two types of transactions with different \((read, write)\) counts \((0,1)\) and \((4,2)\), representative in real-world transactional systems \([78]\). Since the ORCA Tx and HyperLoop has the same mechanism for pure-read transactions, we exclude such transactions from the evaluation.

We demonstrate the latency results of HyperLoop and ORCA in Fig. 11 (note that since the transactions are issued by the client one by one, the latency improvement can also reflect the throughput improvement). For the \(0,1\) transaction, ORCA’s performance does not differ from HyperLoop, since they experience the same overhead – one PCIe round-trip per replica machine and one round-trip over the 2-machine replication chain, and ORCA may even be a bit (less than 3\%) slower than HyperLoop since it also has the overhead of UPI link. However, when the transaction contains multiple operations, ORCA begins to show its advantage. Unlike HyperLoop, ORCA’s client only needs to issue one combined transaction request to the replication chain, and the ORCA accelerator will handle the transaction execution and chain replication protocol itself in a near-data manner – still one PCIe round-trip per machine and one round-trip over the chain. This saves the network and PCIe latency, offering a 63.2\%~66.8\% reduction for average end-to-end latency and 64.5\%~69.1\% for 99th

Fig. 11: Latency comparison with different key-value pair size and transactions with different numbers of \(read,write\).

Fig. 12: MERCI-based DLRM inference throughput on the Amazon Review dataset.
tail latency. Note that ORCA’s latency can be further reduced with accelerator (FPGA) that can directly attach NVM [67].

D. DLRM Inference

We follow MERCI [92] and facebook’s DLRM model [117] to build our test program. Since their open-source implementations only include single-machine version, we extend them to a RDMA-based end-to-end datacenter application (the networking part is similar to the optimized HERD [77]) to reflect the real datacenter environment. The client send the query request to the server for inference.

We follow the configurations in the MERCI paper [92] to perform the evaluation. We compare ORCA’s performance with the CPU-based software version on the popular Amazon Review dataset [59] (electronics, clothing-shoe-jewelry, home-kitchen, books, sports-outdoors, and office-products). Both the native embedding reduction and MERCI reduction are evaluated. The data is clustered and loaded into embedding tables and memoization tables by the CPU in MERCI’s way. The embedding dimension is set to the default value of 64; for MERCI reduction, we build memoization tables with 0.25× the size of the original embedding tables.

Since each query’s length (number of features) in a dataset is diverse, it is unfair to measure the per-query latency, so we only measure the throughput. For brevity, we only show the results of inference with MERCI reduction in Fig. [12] because the ones with native reduction show the same trend. For CPU-based version, MERCI scales linearly until eight cores (threads), which is bounded by the host memory bandwidth. For ORCA, however, we find poor throughput performance over all the datasets – only 19.7%∼31.3% throughput of a single CPU core. After further analysis, we find this phenomenon is because (1) unlike KVS, the nature of the embedding reduction in DLRM (i.e., pure and dense memory accesses within nested “for” loops, few branches, thousands of memory accesses per query) makes it relatively efficient on the CPU core – the instruction window and the load-store queue can be fully utilized; (2) the CPU core can leverage the entire bandwidth of the memory channels (i.e., ∼120GB/s on our testbed) with good parallelism, while the ORCA cc-accelerator can only leverage the cc-interconnect’s bandwidth, and the memory requests have to be issued serially from the FPGA’s wimpy coherence controller; (3) the compute-intensive fully connected layer is relatively lightweight in the model, making ORCA’s hardware acceleration only a small portion in the end-to-end inference. Hence, with higher frequency and memory bandwidth, CPU outperforms the ORCA cc-accelerator. This deficiency can be solved by ORCA-LD and ORCA-LH. Fully utilizing the two DDR4 channels (∼1/2 of the CPU memory channels’ bandwidth), ORCA-LD is able to achieve 52.8%∼95.3% throughput of the eight CPU cores. Furthermore, the 32-channel HBM2 eliminates the memory bandwidth bottleneck in the reduction, leading to ORCA-LH’s 1.6× ∼3.1× throughput improvement over the CPU, and the RDMA network becomes the limiting factor for higher end-to-end throughput. Note that, CPU with integrated HBM2 [29] in the near future may also achieve similar throughput compared to ORCA-LH; but similar to KVS (see Sec. VI-B, even with the same memory bandwidth (and thus the inference throughput), ORCA cc-accelerator shows better power efficiency over the CPU-based reduction.

VII. Discussion

Scalability with faster network. As the speed of network is growing fast, a critical question is whether ORCA will keep up with the speed of future network (e.g., 400Gbps). First, as mentioned before, the UPI’s bandwidth is not saturated in ORCA KV and ORCA TX. Furthermore, as demonstrated by ORCA DLRM, accelerator-attached memory with comparable capacity to the CPU [28, 30, 67] will further librate the bandwidth of the cc-interconnect from application-related memory requests. Hence, the cc-interconnect can better serve the RNIC/CPU-cc-accelerator interaction. This means ORCA will be bottlenecked by the network bandwidth and can achieve higher performance with newer network technologies (also note that the cc-interconnect performance will evolve as well).

Scalability with larger cluster. Prior work has stated that one-sided RDMA operations, relying on reliable connection, cannot scale well to hundreds of machines [75, 77, 78]. This is mainly due to the limited size of on-chip cache of the RNIC, which stores the necessary connection information. However, this has been alleviated with the advance in technologies [120]. For instance, as the latest NIC product, the blueField-2 DPU has ∼10MB cache for its 8-core ARM system on the SoC [122], which also integrates the ConnectX-6 controller. We expect that the ConnectX-6 part on the SoC has comparable cache size (e.g., 5∼10MB) for connections. Based on the previous calculation [75], such on-chip cache can support more than 10K connections without performance loss by cache miss, which is enough for most clusters in modern datacenters. Also note that, ORCA design itself does not worsen the RDMA’s scalability problem.

VIII. Related Work

Accelerating µs-scale datacenter applications with emerging devices. In modern datacenters, commodity networking devices, especially programmable switches and Smart NICs, have been leveraged to accelerate datacenter applications. Such approaches include caching [73, 94, 102, 148], compute offloading [7, 16, 56, 93, 94, 109, 144, 145, 150], protocol offloading [44, 85, 72, 84, 91, 95–97, 138, 147, 161, 174, 181], load balancing [81, 104], etc. However, due to the limited memory capacity of such devices (e.g., O(10MB) of on-chip SRAM for programmable switches [11] [83] and O(10GB) of on-board DRAM for Smart NICs [107, 122]), they may fall short of efficiently handling datacenter applications requiring large memory footprints. To tackle such a challenge, TEA [83] proposes to let the switch retrieve data from the affiliated servers by low-latency RDMA read. TEA uses algorithm design (i.e., linear probe in its hash table) to reduce the required network round-trips to get the desired data, but it cannot always do so for all applications/data structures (e.g., B-tree based KVS [163]).

To alleviate the interconnect (PCIe) overhead, a line of research integrates the entire NIC or accelerator to/near the
CPU package \([3,32,33,55,61,80,100,119,139]\). Enjoying the benefit of fast NIC-core interaction, this approach has (1) high cost of designing and manufacturing them and (2) low flexibility of usage and maintaining. For example, a typical NIC ASIC’s die area can be more than 60mm\(^2\) \([1]\), which is roughly the area of four server CPU cores \([168]\). Also, to upgrade the datacenter network infrastructure, the entire server CPU needs to be replaced, leading to high total cost of ownership (TCO).

Dagger \([90]\) also leverages cc-accelerator for NIC design, but it still involves the server CPU for request processing, and only uses the cc-interconnect for its lower latency over PCIe. Compared to these works, ORCA takes a modularized design with low TCO, while still leveraging cache coherence feature to more efficiently handle applications with irregular/uniform memory access patterns. Besides, for workloads with highly-skewed access patterns, ORCA only adds one PCIe round-trip to the end-to-end latency than its counterparts. They are complementary and thus they can work together.

There is prior effort on accelerating applications in datacenter with cc-accelerator \([20,60,90,106,129,149]\), but they either accelerate single-machine applications/operations or a specific routine/layer in the system. ORCA takes a holistic cross-stack approach to achieve end-to-end datacenter application offloading at \(\mu s\)-scale.

**NIC-host co-design framework.** With the growing popularity of the Smart NIC, researchers have developed frameworks to schedule/offload datacenter applications to the Smart NIC’s processors \([101,103,134]\). However, they are still constrained to separate the Smart NIC and host’s memory to two domains and suffer from a high cost of communications over PCIe links when memory-intensive code segments are offloaded. ORCA tackles these challenges with its unique near-data processing capability, while keeping the networking part offloaded on the RNIC for low cost and flexibility. ORCA can also be included to these co-design frameworks as another compute resource. Lynx \([158]\) proposes Smart NIC-based communication offloading for accelerator-rich systems, and FlexDriver \([39]\) proposes PCIe-based NIC control by accelerator. ORCA takes one step further to let the client directly communicate with the accelerators, which also controls the NIC more efficiently in the coherence domain.

**IX. CONCLUSION**

We present ORCA, a holistic system design to offload modern \(\mu s\)-scale datacenter applications. It leverages the RDMA and cc-accelerator technologies to achieve high throughput and low latency performance with the CPU’s involvement only when necessary. We apply ORCA to three representative datacenter applications, each with its unique characteristics. Our evaluation on a real system shows that, compared to the CPU-based software solutions and the (Smart) NIC offloading solutions, ORCA is able to achieve better and more stable performance with higher power efficiency.
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