Push–pull mode digital control for LLC series resonant dc-to-dc converters

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Abstract: This study presents the design and performance evaluation of the digital control adapted to an LLC series resonant dc-to-dc converter operating with wide input and load variations. The proposed control design correctly incorporates the wide-varying power stage dynamics and variable small-signal gain of a digitally controlled oscillator, thereby offering satisfactory converter performance for all the operational conditions. The proposed digital controller adopts the push–pull mode control scheme, which executes the control action two times in one switching period, to minimise the time delay and enhance the performance. Using a 150 W experimental converter, the performance of the proposed push–pull mode digital control is demonstrated in comparison with that of the conventional complementary mode digital control, which performs the control action only once in one switching period.

1 Introduction

Digital control has emerged as a viable alternative to the conventional analog control for pulsewidth modulated (PWM) converters and resonant converters. The digital control of PWM converters has been extensively studied in past researches, yielding many useful results [1–7]. The digital control of resonant converters also acquired an ever-increasing attention because of the rapid development of the digital signal processor (DSP). The digital control of resonant converters can be divided into two groups. The first group is the non-linear control schemes, such as geometric boundary control [8, 9], observer-based control [10], sliding mode control [11] and optimal trajectory control [12–14]. These control schemes directly monitor and control the resonant tank waveforms using high-performance DSPs or field-programmable gate array. These non-linear controls do not rely on the small-signal models or small-signal dynamics of converters for the execution of their control functions.

The second group is the digital controls based on the emulation method [15–17], which transforms an s-domain linear compensation into the z-domain counterpart. The emulation-based digital controls are entirely based on the small-signal dynamics of the resonant converters. Although these control schemes presume relatively small variations in the operating point, some protective measures are embedded into the controller for safe operations of the converter during large transitional periods. This paper presents a new emulation-based digital control for LLC resonant converters, which can be implemented with a cost-effective 16-bit DSP while offering considerable improvements over earlier emulation-based digital controls.

There exist several challenges for the implementation of the emulation-based digital control for resonant converters. One challenge would be the variations in both the power stage dynamics of the converter and small-signal gain of a counter-based digitally controlled oscillator (DCO). The power stage dynamics are sensitively affected by operational conditions [18–22]. The small-signal DCO gain varies as a quadratic function of the switching frequency. The digital control should be designed in consideration of these wide-varying power stage dynamics and DCO gain.

Another important issue of the emulation-based digital control is the time delay between the analog-to-digital converter (ADC) sampling and the switching period updating. The time delay is converted into the phase delay in the frequency responses, which could lower the phase margin of the loop gain and induce an unexpected oscillation in the output voltage.

In the conventional digital control for resonant converters, the ADC sampling is performed once in one switching period and the period updating is delayed at least half the switching period. This control scheme has been known as the complementary mode control [16]. This paper proposes a digital control scheme which employs two ADC samplings in one switching period: one ADC sampling during the first half of the switching period and another ADC sampling during the remaining half of the switching period. This control scheme is referred to as the push–pull mode control. In this control scheme, the two ADC samplings are individually used to immediately update the duration of the ensuing half of the switching period. The proposed control scheme substantially reduces the time delay and enhances the performance, compared with the case of the conventional complementary mode control.

This paper will show that the push–pull mode digital control outperforms the analog control, implemented with a fixed-gain voltage controlled oscillator (VCO) [18–21]. Initially, the analog control might be designed for a large loop gain magnitude, sufficient stability margins and wide control bandwidth. However, when the operating point moves into the region where the power stage transfer functions vary into an undesirable direction, the converter performance will be degraded. In contrast, the DCO-based digital control exploits the non-linear DCO gain to compensate for unwanted variations in power stage transfer functions. This paper will demonstrate that the digital control could offer the superior loop gain characteristics and transient responses, compared with VCO-based analog controls.

The proposed push–pull mode control also possesses the general merits of the digital control, such as design flexibility, cost-effectiveness, enhanced noise immunity and higher power density [15, 23–25].

This paper addresses the design and performance evaluation of the push–pull mode digital control for LLC series resonant dc-to-dc converters. The current paper adopts the standard emulation method for the digital compensation design, nonetheless, the compensation design incorporates the variations in the power stage dynamics and DCO gain. Design procedures and performance evaluation of the proposed digital control are illustrated using a 150 W experimental LLC converter. The performance of the
push–pull mode digital control is compared with that of the complementary mode digital control. This paper reveals that the push–pull mode control outperforms the complementary mode control, because of a reduced time delay and enhanced feedback gain. This paper also shows that the push–pull mode digital control offers the closed-loop performance that favourably compares with the performance of the conventional analog control.

2 Design of push–pull mode digital control for LLC converter

This section presents the design of the proposed push–pull mode digital control, adapted to a 150 W experimental LLC converter. The digital compensation design is based on the standard emulation method, nonetheless, it considers the wide-varying power stage dynamics and DCO gain, to obtain good performance for the entire operational range.

2.1 Converter configuration

Fig. 1 is a simplified circuit diagram of the experimental LLC converter employing a push–pull mode digital control. As a typical case of off-line power supplies, the converter receives the input voltage of \( V_s = 340–390 \) V and produces \( V_o = 24 \) V at the load current of \( I_o = 1–6 \) A. The output voltage is sensed by an anti-aliasing low-pass filter and fed to a 16-bit DSP: dsPIC33FJ16GS from Microchip [16]. Procedures for DSP selection for the given application are presented in Appendix. The 10-bit ADC inside the DSP accepts the sensed output voltage in the range of \( \text{v}_{\text{sense}} = 0–3.3 \) V. The digital compensation \( F_v(z) \) receives the error signal \( e[n] \) from ADC and provides the input signal \( c[n] \) for the DCO. The DCO operates with a counter-based digital-PWM scheme [3]. The DCO outputs derive two MOSFET switches, \( Q_1 \) and \( Q_2 \), in a push–pull mode of operation [16], where the turn-on durations of the two switches are individually controlled by the two DCO outputs.

2.2 Operational region

Fig. 2a shows a family of the input-to-output curves of the experimental LLC converter, each with a different load condition. The frequency \( f_{o\infty} = 1/(2\pi\sqrt{CpL_m}) \) denotes the short-circuit resonant frequency of the LLC tank. On the other hand, the frequency \( f_{o\infty} = 1/(2\pi\sqrt{Cp(L_m+L_n)}) \) is the open-circuit resonant frequency of the LLC tank.

For the given input and load specifications, the operational region of the converter can be defined on the voltage gain curves, as

![Fig. 1 150 W LLC series resonant dc-to-dc converter with push-pull mode digital control: \( V_s = 340–390 \) V, \( V_o = 24 \) V, \( I_o = 1–6 \) A, \( C_s = 47 \) nF, \( L_n = 160 \) \( \mu \)H, \( L_m = 1.24 \) mH, \( n = 0.14 \), \( C = 2 \) mF, \( R_s = 6.6 \) m\( \Omega \), \( R_o = 250 \) \( \Omega \), \( C_o = 2.2 \) nF, ADC resolution is 3.22 mV and DCO counter period is 1.04 ns](image)

![Fig. 2 Input-to-output voltage gain curves and operational region of experimental LLC converter](image)

\( a \) Input-to-output voltage gain curves: \( f_o = 58 \) kHz and \( f_{o\infty} = 20 \) kHz

\( b \) Expanded view of operational region
highlighted in Fig. 2a. Fig. 2b shows the expanded view of the operational region in which all the operating points of the LLC converter could locate for the given input and load conditions. On the operational region, the four extreme operating points (Points A, B, C and D) are shown; Point A: 340 V/6 A, Point B: 390 V/6 A, Point C: 340 V/1 A and Point D: 390 V/1 A.

For the given LLC converter, the operating point normally lies on the curve between Point A and Point B: \( V_S = 340 \sim 390 \) V with \( I_D = 6 \) A. Accordingly, the dynamic analysis and control design will be mainly focused on Points A and B. Nonetheless, the converter performance will be evaluated for the entire operational region.

2.3 Power stage dynamics

The earlier studies [18-22] proved that small-signal dynamics of LLC converters vary substantially as operational conditions are altered. The major result of these analyses is shown in Fig. 3 in conjunction with the small-signal dynamics of the experimental LLC converter. Fig. 3 depicts the pole/zero trajectory of the frequency-to-output transfer function with respect to the input voltage variation. The trajectory portrays the locations of poles and zero as the input voltage decreases from \( V_S = 390 \) V, represented by Point B in Fig. 3, to \( V_S = 340 \) V, denoted as Point A, while delivering the load current of \( I_D = 6 \) A. Detailed analyses for the locations of poles and zero at Point A and Point B were given in [18-22].

Fig. 3b displays the measured Bode plot of the control-to-output transfer function, \( G_{vc}(s) \), at Point A and Point B. For the \( G_{vc}(s) \) measurement, an analog control is employed to the experimental converter. The transfer function exhibits notable changes, in the exact same manner as predicted from the pole/zero trajectory in Fig. 3a. It is observed that Point B has a single pole \( \omega_{pl} \) at low frequencies and shows the first-order system behaviour from low- to mid-frequencies. In contrast, Point A reveals the second-order behaviour with rapid-declining phase characteristics because of the two neighbouring poles, \( \omega_{pl} \) and \( \omega_{zp1} \). Point A presents the worse small-signal dynamics and thus becomes a logical target for the compensation design.

From Fig. 3b, an approximated expression for the control-to-output transfer function at Point A is determined as

\[
\tilde{G}_{vc}(s)_A = K_{vc0} \frac{1 + s/\omega_{esr}}{(1 + s/\omega_{pl})(1 + s/\omega_{zp1})} \tag{1}
\]

where \( K_{vc0} \) is the gain of the analog VCO at Point A and \( K_{esr} \) is the low-frequency gain of the frequency-to-output transfer function at Point A. Although the expression (1) does not account for the high-frequency dynamics, it adequately describes the converter dynamics up to mid-frequencies and thus can be used as a basis for the compensation design.

The esr zero in (1) is calculated as \( \omega_{esr} = 1/(CR) = 7.5 \times 10^4 \) rad/s. The neighbouring poles in Fig. 3b are estimated as \( \omega_{pl} = 5.0 \times 10^3 \) rad/s and \( \omega_{zp1} = 7.0 \times 10^3 \) rad/s. The low-frequency asymptote of Fig. 3b is observed as \( 20 \log (K_{vc0}K_{esr}) = 20 \) dB. The analog VCO gain at Point A was measured as \( K_{vc0} = 2\pi \cdot 6.10 \times 10^4 \). The low-frequency gain of the frequency-to-output transfer function at Point A is now determined as \( K_{esr} = 10/K_{vc0} = 2.61 \times 10^{-3} \).

2.4 s-Domain compensation formulation

An s-domain compensation is initially formulated and later converted into the z-domain compensation using the emulation method. The s-domain compensation is designed using the control-to-output transfer function at Point A, \( G_{vc}(s)_A \), to secure stability and performance for the entire operational range.

An earlier publication [18] showed that a three-pole two-zero compensation provides good dynamic performance for the experimental converter over the entire operational range

\[
F_v(s) = \frac{K_v(1 + s/\omega_1)(1 + s/\omega_2)}{s(1 + s/\omega_{pl})(1 + s/\omega_{zp1})} \tag{2}
\]

Fig. 4a shows the asymptotic plots for the control-to-output transfer function \( |\tilde{G}_{vc}(s)_A| \) and the loop gain \( |\tilde{T}_{vc}(s)_A| = |\tilde{G}_{vc}(s)_A|F_v(s) \) at Point A. The loop gain plot in Fig. 4a is constructed by placing

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**Fig. 3** Power stage dynamics of experimental LLC converter

a Pole/zero trajectory of frequency-to-output transfer function

b Experimental Bode plot of control-to-output transfer function \( G_{vc}: \omega_{pl} = |\omega_{pl}|, \omega_{zp1} = |\omega_{zp1}| \)

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the \( \omega_{z1} = \omega_{z2} = 5.0 \times 10^3 \) rad/s, \( \omega_{z2} = \omega_{z3} = 7.0 \times 10^3 \) rad/s, \( \omega_{c1} = 7.5 \times 10^4 \) rad/s and \( \omega_{c2} = 9.5 \times 10^4 \) rad/s. For a practical design implementation, the integrator gain \( K_v \) is determined after the selection of loop gain crossover frequency, \( \omega_c \) [26]. The loop gain crossover frequency is selected at \( \omega_c = 2 \pi \cdot 2.3 \times 10^3 \) rad/s for a sufficient phase margin. The evaluation of the required integrator gain \( K_v \) will be discussed later.

Fig. 5 depicts the equivalent \( s \)-domain representation of the push–pull mode digital control. Referring to Fig. 5, the sensing gain of the anti-aliasing filter is evaluated as \( H = R_1/(R_1 + R_x) = 0.125 \), the ADC gain is calculated as \( K_{ADC} = 1/3.3 = 0.3 \) with the \( v_{sense} = 0 - 3.3 \) V, and the low-frequency gain \( G_{vf} (s) \) at Point A was evaluated as \( K_{vfA} = 2.61 \times 10^{-5} \) in the previous section. The total time delay between the ADC sampling and the period updating, \( t_d \), is discussed in Section 3.2. The sampling time period, \( t_{samp} \), employed in the \( s \)-to-\( z \)-domain compensation conversion is discussed in 2.5. The gain of the DCO employed in the experimental converter is calculated as \( f_{DCOA} = 1.5 \times 10^7 \) at Point A. Details about the DCO gain evaluation are given in Section 3.1.

The integrator gain \( K_v \) in the \( s \)-domain compensation is determined as explained below. Referring to the loop gain plot \( |T_m(s)| \) in Fig. 4a and the \( s \)-domain small-signal block diagram in Fig. 5, the following relation is derived

\[
20 \log \frac{H K_{ADC} K_v^2 f_{DCOA} K_{vfA} v_c}{\omega_c} = 0 \text{ dB (3)}
\]

where \( \omega_c \) is the loop gain crossover frequency and \( K_v \) is the integrator gain. The required \( K_v \) for the desired \( \omega_c \) is now determined as

\[
K_v = \frac{\omega_c}{20 \log 2 \pi f_{DCOA} K_{vfA}} = \frac{2 \pi \cdot 2.3 \times 10^3}{0.125 \cdot 0.3} = 1.56 \times 10^4
\]

The final expression for the \( s \)-domain compensation is given by

\[
F_v(s) = \frac{1.56 \times 10^4(1 + s/5 \times 10^7)(1 + s/7 \times 10^7)}{s(1 + s/5 \times 10^8)(1 + s/9.5 \times 10^4)}
\]

Fig. 4 s-domain compensation design at Point A

Fig. 5 s-domain equivalent small-signal block diagram of push–pull mode digital control
2.5 Conversion to z-domain compensation

The s-domain compensation (5) is converted into the z-domain compensation through the bilinear transform using MATLAB software. For the push–pull mode control with two ADC samplings in one switching period, the sampling time period for the s-to-z-domain compensation conversion, \( t_{\text{samp}} \), is given by \( t_{\text{samp}} = 1/(2f_{\text{sw}}) \) where \( f_{\text{sw}} \) denotes the switching frequency at Point A. The bilinear-transformed z-domain expression of (5) is determined as

\[
F_v(z) = F_v(s) \bigg|_{s=(z-1)/(z+1)(2/t_{\text{samp}})} = \frac{8.3058(z + 1)(z - 0.9512)(z - 0.9324)}{(z - 1)(z - 0.4545)(z - 0.3559)}
\]

and later converted into the parallel structure

\[
F_v(z) = 7.8(1.0648 + \frac{0.02}{z - 1} - \frac{0.7834}{z - 0.4545} + \frac{7.801}{z - 0.3559})
\]

Fig. 6 is the simulation block diagram of (7), which can readily be converted into the C-code programming. Fig. 4b shows the measured and simulated Bode plots for \( G_{\text{vcl}} \) and \( T_{\text{rel}} \) of the experimental LLC converter at Point A with the proposed digital control. The time-domain simulation method [18] using PSIM software is employed to generate the simulated Bode plots. Fig. 4b closely resembles Fig. 4a, thereby validating the proposed design procedures.

3 DCO gain and total time delay of digital control

This section analyses the small-signal gain of the counter-based DCO and the total time delay in digital control. The current section also addresses the features of the push–pull mode control in comparison with those of the complementary mode control.

3.1 DCO and small-signal gain

Figs. 7a and b show the timing diagram of a counter-based DCO for the complementary mode control and push–pull mode control. In the complementary control where the ADC sampling is performed only once in one switching period, the DCO receives the command \( c[n] \) from the digital compensation and multiplies it with a prefixed constant \( K_{\text{DCO}} \) to yield an intermediate variable \( N = K_{\text{DCO}} c[n] \). The variable \( N \) is then multiplied with a prefixed DCO clock, \( t_{\text{clk}} \), to update the switching period of the two complementary-driven MOSFET switches. This operation is illustrated in Fig. 7a. The frequency of the period updating is given by

\[
f_{\text{update}} = \frac{1}{N'_{\text{clk}}} = \frac{1}{K_{\text{DCO}} c[n]t_{\text{clk}}}
\]

For this case, the period updating frequency is the same as the switching frequency: \( f_{\text{update}} = f_{\text{sw}} \).

The operation of the push–pull mode control is illustrated in Fig. 7b, where the ADC sampling is performed twice in one switching period. For this case, the intermediate variable is calculated as \( N' = 0.5K_{\text{DCO}} c[n] \) and subsequently multiplied with the \( t_{\text{clk}} \) to determine the duration of the ensuing half of the switching period, thus enabling to immediately use the result of the accelerated ADC sampling. The period updating frequency now becomes

\[
f_{\text{update}} = \frac{1}{N''_{\text{clk}}} = \frac{2}{K_{\text{DCO}} c[n]t_{\text{clk}}}
\]

For this case, the period updating frequency is double the switching frequency: \( f_{\text{update}} = 2f_{\text{sw}} \). The input variable of the DCO is the \( c[n] \) and its output variable is the frequency of the period updating, \( f_{\text{update}} \). Thus, the small-signal gains of DCO for the two different operational modes are evaluated as (see (10))

\[
f_{\text{DCO}} = \frac{\Delta f_{\text{update}}}{\Delta c[n]} = \begin{cases} \frac{1}{t_{\text{clk}}K_{\text{DCO}} c[n]} & : \text{for complementary mode control} \\ \frac{2}{t_{\text{clk}}K_{\text{DCO}} c[n]} & : \text{for push – pull mode control} \end{cases}
\]

where \( f_{\text{sw}} = 1/(K_{\text{DCO}} c[n]t_{\text{clk}}) \) is the switching frequency.

As shown in (10), the DCO gains in both the cases increase as a quadratic function of the switching frequency. More importantly,

\[\begin{align*}
\text{(10)}
\end{align*}\]
the DCO gain of the push–pull mode control is two times larger than that of the complementary mode control.

The DCO gain in (10) contains the two constants, \( t_{\text{clk}} \) and \( K_{\text{DCO}} \). These constants are determined as follows. First, the DCO clock in dsPIC33FJ16GS is given by \( t_{\text{clk}} = 1.04 \times 10^{-9} \) s. As demonstrated in Fig. 2b in 2.2, the switching frequency of the experimental converter varies between \( 50 < f_{\text{sw}} < 110 \) kHz. The lower limit of the switching frequency is set at \( f_{\text{sw lower}} = 35 \) kHz to secure a 15 kHz margin from the minimum switching frequency of 50 kHz. The constant \( K_{\text{DCO}} \) is determined such that the DCO generates the upper limit of the switching period when the ‘digital-equivalent’ value of ‘1’ appears as the input signal \( c[n] \). The upper limit of the switching period is then determined as \( t_{\text{sw upper}} = 1/f_{\text{sw lower}} = 1/35 \times 10^3 = 28.6 \) μs. Thus, \( K_{\text{DCO}} \) is calculated as

\[
K_{\text{DCO}} = \frac{t_{\text{sw upper}}}{t_{\text{clk}}} = \frac{28.6 \times 10^{-6}}{1.04 \times 10^{-9}} = 2.8 \times 10^4
\]

Fig. 7c shows the DCO gain curves evaluated using (10) with \( K_{\text{DCO}} = 2.8 \times 10^4 \) and \( t_{\text{clk}} = 1.04 \times 10^{-9} \). The DCO gain at Point A with \( f_{\text{sw}} = 50 \) kHz is calculated as

\[
f_{\text{DCO A}} = 2(50 \times 10^3)^2 \cdot 2.8 \times 10^4 \cdot 1.04 \times 10^{-9} = 1.5 \times 10^5
\]

which was used in (4) to determine the integrator gain \( K_v \).

3.2 Total time delay

Fig. 8 depicts the power stage and control waveforms of the complementary mode control and push–pull mode control. The tank current \( i_T \), output of the anti-aliasing filter \( v_{\text{sense}} \), MOSFET drive signal \( v_{Q1} \) and ADC interrupt signal \( v_{\text{int}} \) are shown in Fig. 8. The total time delay \( t_d \) refers to the duration between the ADC sampling and the switching period updating. The total time delay \( t_d \) includes the ADC conversion time, \( t_{\text{ADC}} \), the computational delay \( t_c \) and the spare time \( t_{\text{sp}} \). As shown in Fig. 8a, the complementary mode control, which executes the ADC sampling only once in one switching period, has a longer spare time \( t_{\text{sp}} \), resulting in the total time delay of \( t_d = 4.0 \) μs at Point A and \( t_d = 10.8 \) μs at Point B. In contrast, in push–pull mode control where the ADC sampling is done twice in one switching period, the spare time is virtually eliminated and the total time delay is reduced to \( t_d = 4.0 \) μs at both Point A and Point B. In the proposed digital control, the ADC sampling instant is adaptively adjusted by the C-code program to minimise the spare time. As will be shown in Appendix, the headroom for the computational delay is minimal, but it never vanishes as far as the switching frequency remains lower than 120 kHz.

4 Performance of push–pull mode digital control

The performance of the proposed push–pull mode digital control is evaluated, in comparison with the performance of the
complementary mode digital control and also with that of the analog control. The loop gain and step load response are analysed to assess the performance of the control schemes.

4.1 Comparison with complementary mode digital control

The push–pull mode control and complementary mode control produce the different DCO gain and total time delay. The performance of the experimental LLC converter is investigated with the two control schemes, to assess the merits of the respective control scheme.

4.1.1 Loop gain characteristics: Fig. 9 shows the measured and simulated loop gain characteristics of the experimental LLC converter. The thick solid line displays the loop gain characteristics of the push–pull mode control with the integrator gain of $K_v = 1.56 \times 10^4$. The loop gain crossover occurs at the target frequency with sufficient phase margin at both Point A and Point B. Now, the complementary mode control is adapted with the same integrator gain, $K_v = 1.56 \times 10^4$, but $t_{\text{samp}} = 1/f_{\text{sw}}$ is used as the sampling time period in the s-to-z-domain compensation conversion. The loop gain characteristics of the resulting complementary mode control are shown with the thin solid line. The loop gain magnitude is uniformly decreased by 6 dB because the DCO gain is reduced to half the push–pull mode control case. More importantly, the phase curve reveals much increased phase delay at the high frequencies, as a direct consequence of the longer time delay in the complementary mode control. This indicates that the push–pull mode control provides an exact 6 dB gain boost over the conventional complementary mode control, as predicted from the DCO gain expression in (10). In addition, the push–pull mode control significantly improves the phase characteristics at high frequencies because of the reduced time delay.

To compensate for the DCO gain reduction, the integrator gain is doubled, $K_v = 3.12 \times 10^4$, for the complementary mode control and the resulting loop gain characteristics are shown with the dashed line. Although the loop gain magnitude is restored to the value of the push–pull mode control, the phase curve still shows an excessive high-frequency phase delay.

4.1.2 Step load change responses: Fig. 10 illustrates the transient waveforms of the output voltage and tank current in response to a series of step changes in the load current, $I_0 = 6 \ A \Rightarrow 1 \ A \Rightarrow 6 \ A$, at Point A and Point B. The push–pull mode control with $K_v = 1.56 \times 10^4$, shown in Fig. 10a, exhibits well-controlled transient waveforms. On the other hand, the complementary mode control with $K_v = 1.56 \times 10^4$, Fig. 10b, reveals stable responses but only with inferior transient behaviour because of the reduced loop gain magnitude. More significantly, the complementary mode control with the doubled integrator gain $K_v = 3.12 \times 10^4$, shown in Fig. 10c, generates oscillatory waveforms because of the excessive phase delay. This analysis indicates that the push–pull mode control outperforms the complementary mode control and offers better transient responses.

4.2 Comparison with analog control

Fig. 11 illustrates the comparison of performances of the proposed push–pull mode digital control with the case of the conventional analog control. The potential merit of the proposed digital control using a counter-based DCO is highlighted.

4.2.1 Loop gain characteristics: Fig. 11a depicts the measured and simulated loop gain characteristics of the push–pull mode digital control in comparison with those of the analog control. The analog control is optimally designed based on the design procedures proposed in [18]. The digital control nearly duplicates the loop gain characteristics of the analog control at Point A.

At Point B, the loop gain of the digital control exhibits a 7 dB magnitude boost, compared with that of the analog control. The magnitude boost is an outcome of the non-uniform DCO gain. As shown in Fig. 7c, the DCO gain at Point B is larger than the DCO gain at Point A by a factor of $(75 \times 10^3/50 \times 10^3)^2 = 2.25$. The
larger DCO gain raises the loop gain magnitude of the digital control by $20 \log_{10} 2.25 = 7$ dB, compared with the analog control case where the VCO gain remains constant. The above analysis hints the potential merit of the digital control with a counter-based DCO. The non-uniformity in the DCO gain can be exploited to compensate for unwanted and undesirable variations in power stage dynamics; the magnitude of the frequency-to-output transfer function is inversely proportional to the switching frequency. This gain decrease can be cancelled with an increased DCO gain at high frequencies.

Fig. 9  Loop gain characteristics with push–pull mode and complementary mode controls

a Point A  
b Point B

Fig. 10  Step-load transient response waveforms of push–pull mode and complementary mode controls

a Push–pull mode control with $K_v = 1.56 \times 10^4$

b Complementary mode control with $K_v = 1.56 \times 10^4$

c Complementary mode control with $K_v = 3.12 \times 10^4$
4.2.2 Step load response: Fig. 11b shows the measured transient responses of the output voltage and tank current in response to \( I_L = 6 \text{ A} \rightarrow 1 \text{ A} \rightarrow 6 \text{ A} \) changes in the load current. The digital control and analog control both produce largely the same responses at Point A. However, at Point B, the digital control shows superior transient responses because of the improved loop gain characteristics, thereby supporting the potential merit of the proposed digital control.

5 Conclusions

This paper presented the design and performance evaluation of the push–pull mode digital control, adapted to an LLC series resonant dc-to-dc converter operating with wide input and load variations. The non-iterative compensation design procedures are proposed. Although the standard emulation method is employed, the design procedures correctly incorporate the variations in the
frequency-to-output transfer function and DCO gain, and offer satisfactory performance for the entire operational range.

The design procedures and performance of the proposed digital control are validated using a 150 W experimental LLC converter. The performance of the push–pull mode digital control is compared with that of the complementary mode digital control and conventional analog control. With an advanced ADC sampling rate and integrator gain, the push–pull mode digital control revealed the superior performance over the other two control schemes, thereby demonstrating the application potential of the proposed digital control for resonant dc-to-dc converters.

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8 Appendix: Selection procedures for DSP

As shown in Fig. 2b in 2.2, the switching frequency of the experimental converter varies between 50–110 kHz. The upper limit of the switching frequency is selected as \(f_{\text{sw upper}} = 120 \text{kHz}\), to provide a 10 kHz buffer from the maximum switching frequency of 110 kHz. For the proposed push–pull mode control, the minimum process time from the ADC sampling to the period updating is given by \(t_{\text{process min}} = 0.5/f_{\text{sw upper}} = 0.5/120 \times 10^3 = 4.2 \mu \text{s}\).

The three-pole-two zero digital compensation used for this application requires 125 instruction cycles. Thus, any DSP chip which could complete the AD conversion plus 125 instruction cycles within 4.2 \(\mu \text{s}\) is suited for this application. The 16-bit dsPIC33FJ16GS from Microchip [16] is selected as the most cost-effective solution. The total process time for dsPIC33FJ16GS is given by

\[
t_{\text{process}} = t_{\text{ADC}} f_{\text{ADC}} + t_{\text{comp}} \frac{MIPS}{10^{-6}}
\]

where \(t_{\text{ADC}} = 18\) is the ADC clock cycles of the DSP, \(f_{\text{ADC}} = 50 \times 10^9\) is the ADC clock period of the DSP, \(t_{\text{comp}} = 125\) is the total instruction cycles of the three-pole-two zero compensation, \(MIPS = 40\) is the DSP spec in the unit of Million Instructions Per Second.

Evaluation of (11) with the given data yields

\[
t_{\text{process}} = 18 \times 50 \times 10^9 + 125 \times 4 \times 10^{-6} = 0.9 \times 10^{-6} \\
+ 3.13 \times 10^{-6} = 4.03 \mu \text{s} < 4.2 \mu \text{s}
\]

thereby confirming the proper operation for the entire operational range of the converter.