Performance Evaluation of Junctionless FinFET using Spacer Engineering at 15 nm Gate Length

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Abstract
In this proposed work, performance of junctionless transistor with the use of spacers has been evaluated at 15 nm gate length in Cogenda TCAD tool. This work is implemented as variation in four parts: changing the spacer extension length, placement of spacers having dual-κ, proportion of low and high-κ spacers, and value of high-κ dielectric constant. Impact of all these parameters is considered on the output of proposed device in terms of various output parameters like on-current (I\text{ON}), off-current (I\text{OFF}), subthreshold swing (SS), drain-induced barrier lowering (DIBL), transconductance (g_m), transconductance generation factor (TGF), output conductance (g_d), early voltage (V\text{ea}) and intrinsic gain (A\text{v}). From the simulations, it has been observed that placing spacers of dual-κ along the left and right sides of gate region has improved device performance in terms of output parameters. Due to increased gate capacitances, the increase in dielectric constant value has degraded the device performance for longer spacer extension length. However, for shorter spacer extension length, the device characteristics are improved as the value of dielectric constant is increased. Therefore a trade-off is required to get the optimum results of the device.

Keywords Junctionless transistor · Dual-κ spacer · Spacer engineering · Subthreshold swing · Short channel effects

1 Introduction
CMOS technology has grown tremendously over the past few years. The process of Scaling allows more numbers of components to be accommodated over the given chip area. This growth in number of transistor over an IC was well predicted by Gordon E. Moore in 1965 [1]. Below 20 nm technology, it is difficult to form sharp source and drain junctions in planar MOS transistor. For creating these junctions, doping concentration gradient needs to be high and should be processed at low temperatures. Different structures like Fin shaped FET (FinFET) and Double-gate MOSFET (DG-FET) provide superior immunity against adverse effects occurring at short channel, commonly known as SCEs [2]. More than one gate allows better gate control and lowers drain-induced barrier lowering (DIBL) [3]. Junctionless transistor (JLT) was invented by researchers to avoid formation of sharp junctions and cost annealing problems [4]. This kind of structure doesn’t have any junctions between source-channel-drain regions. All these regions have same doping type and concentrations. The JLT can act like a resistor where gate voltage controls the drive current [5]. JLT has advantages of being simple from fabrication point of view and requires low thermal budget [6]. Compared to inversion-mode (IM) FETs, junctionless (JL) FET has more reliability which was demonstrated by Toledano-Luque et al. [7]. Junctionless accumulation mode (JAM) FinFET based on Bulk isolated junctions was demonstrated in 2013 for the first time [8]. This structure has lower cost of substrate than Silicon on insulator (SOI) and was compatible with existing CMOS technology.

The effect of high-κ material as spacer in Junctionless transistor was investigated which showed the improvement in device performance and has lesser short channel effects [9]. Dual-κ spacers are combination of low and high-κ materials acting as spacers. High dielectric spacers are generally used nearer the fin, which lowers the leakage current and hence lesser SCE due to increased fringe field coupling between gate and region of underlapping [10].

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Dual-κ spacer impact was demonstrated on double gate FET that controls the direct tunneling between source and drain [11]. Dual-κ spacer gives better results than the low-κ spacers in junctionless transistor [12]. Length of spacer and value of dielectric constant (κ) also play significant role in device performance [13].

Different dielectric spacers with different proportion and configurations can be used for better device characteristics as compared to the conventional FET [14–17]. Recently, the significant power reduction has been examined in performance of JLT and improved using spacer engineering. Dual-κ spacer length was optimized to improve the subthreshold performance [18]. Impact of Spacer extension length (L_{ext}) and placement of spacers on only drain side, both sides, only source side on Trigate FET was explored by [19] to enhance the analog performance.

Therefore proposed work is aimed at demonstrating the impact of spacer engineering on junctionless transistor design. The whole work has been carried out by varying L_{ext}, dielectric value of high κ spacer, placement and proportion of dual-κ spacers.

This paper has been divided into following sections: Next Section describes the design setup of the proposed device. In Section 3, various simulated results have been discussed and the conclusion of the work is presented in Section 4.

## 2 Design Setup

Junctionless device with dual-κ spacer at 15 nm length of gate (L_{g}) is designed using Cogenda TCAD software. Height of fin (H_{fin}) is 20 nm and width of fin (W_{fin}) is taken as 20 nm and 10 nm. Tungsten with 4.96 eV work function is used for gate terminal. Source region and drain region are doped with concentration of $1 \times 10^{21}$ cm$^{-3}$ while channel doping is $1 \times 10^{18}$ cm$^{-3}$ [20]. Spacer extension length (L_{ext}) is fixed at 1.5 \times L_{g} i.e. 22.5 nm and 2 \times L_{g} i.e. 30 nm respectively. The proportion of high-κ material in dual-κ spacers has been taken as 4:1 (L_{lk}:L_{hk}) 1:4, 3:2, 2:3 where L_{lk} and L_{hk} represents the low-κ and high-κ materials respectively [14].

Equivalent oxide thickness (EOT) [21] is defined in (1) which calculates the values of SiO$_2$ and HfO$_2$ thickness as 0.7 and 3.1 nm resulting in overall value of 1.25 nm. SiO$_2$ has been used as interfacial layer below HfO$_2$.

$$\text{EOT} = T_{\text{SiO}_2} + T_{\text{HfO}_2} \times \left( \frac{\kappa_{\text{SiO}_2}}{\kappa_{\text{high-κ}}} \right)$$

For dual-κ spacers, SiO$_2$ was used as low-κ material and high-κ material has been changed to 30, 22.3 and 15 respectively. Under-fin doping concentration value is $5 \times 10^{17}$ cm$^{-3}$. Other important design parameters of the designed device are:

| Parameter | Value |
|-----------|-------|
| Length of Spacer extension region (L_{ext}) | 1.5x, 2x gate length |
| Dielectric constant of high-κ spacer | 15, 22.3, 30 |
| Proportion of low and high-κ spacer | 4:1, 1:4, 2:3, 3:2 |

Placement of spacers with dual dielectrics is aligned in three formats: (i) on source side, (ii) on drain side, and (iii) on both sides.

Figure 1a and b shows the 3D picture of designed junctionless transistor with dual-κ spacers on two sides of gate region for different spacer extension length. Figure 2b shows the internal structure of designed device where fin was covered with EOT.

Selection of fin height/gate length and fin width/gate length has been taken as 1.3 and 0.6 respectively [22]. Being a junctionless device, fabrication of this structure benefits from...
one reduced step of forming junction. Buried oxide layer is formed on substrate of silicon material. Silicon layer after being formed on BOX, dopants are diffused. Gate oxide stack layer is accumulated, and beneath gate oxide, active fin area is present with sufficient doping and width for full flow of charge carriers. Source and drain regions are placed on the either side of fin. After that, traditional way of fabrication is followed [23].

3 Simulation Methodology

To check the validation of Cogenda TCAD tool, experimental results obtained by Choi et al. in [20] and simulated results junctionless accumulation mode (JAM) FinFET have been plotted as shown in Fig. 3a which are close in agreement with each other.

Methodology opted for the work as shown in Fig. 3b depicts the step-by-step process.

ION denoting ‘On current’ and IOFF denoting ‘off current’ are calculated at gate supply voltage of 1 V and 0 V respectively while keeping drain supply fixed at 0.05 V. Drain-induced barrier lowering current is measured by \( \left( \frac{W_{\text{eff}}}{L_g} \right) \times 10^{-7} \) A i.e. \( 4 \times 10^{-7} \) A at \( V_d \) of 20 mV and 1 V respectively. \( W_{\text{eff}} \) denotes effective channel width and is defined in Eq. (2) [24].

\[
W_{\text{eff}} = 2H_{\text{fin}} + W_{\text{fin}} \quad (2)
\]

Lombardi mobility model has been applied to incorporate various factors which contribute towards degradation of mobility of charge carriers. These include scattering mechanisms caused due to surface roughness, phonon and ionized impurities. Matthiessen’s rule combines these three factors and accurately assesses its impact. For carrier transport modeling, instead of applying classical model, quantum confinement effects which are dominant in nanoregime, have been incorporated into the classical model [25, 26].

Case I. When \( L_{\text{ext}} = 1.5 \times L_g \)

For this case, spacer extension length \( L_{\text{ext}} \) has value of 22.5 nm i.e. \( 1.5 \times L_g \) as shown in Fig. 1a.

(a) Effect of variation in spacer placement

In this, dual-κ spacers are kept on the side of source, both sides and on the drain side respectively. Dual-κ spacers on drain side resulted in minimum DIBL of 98 mV/V, output conductance \( (g_d) \) of \( 9.78 \times 10^{-6} \) S and maximum early voltage \( (V_{ea}) \) of 4.02 V due to improved gate fringing coupling towards the drain side for \( L_{\text{ext}} = 1.5 \times L_g \). However, metrics (i) \( I_{\text{ON}}/I_{\text{OFF}} \), (ii) subthreshold swing (SS), (iii) transconductance \( (g_m) \), (iv) transconductance generation factor \( (TGF = g_m/I_d) \), (v) intrinsic gain \( (A_v = 20 \log (g_m/g_d)) \) are better for dual-κ (both sides) structure.

(b) Effect of variation in proportion of spacers

Variation in proportion of low- and high-dielectric spacers (4:1, 1:4, 3:2 and 2:3) has been done. From the
simulations, it has been concluded that for 2:3 ratio of low and high-κ spacers, almost all parameters of the designed device were improved. But maximum gain of 56.73 dB was observed for 3:2 ratio of dual-κ (both sides) device for κ = 30.

(c) Effect of variation in κ-value of high dielectric material in spacer region

Dielectric value of high-κ material in dual dielectric spacers has been changed to 15, 22.3 and 30. As the κ value of high-κ material is increased, an improvement in performance parameters of device has been observed as shown in Figs. 4, 5 and 6.
Fig. 4  a Variation of $I_{ON}/I_{OFF}$ b $A_v$ with respect to value of high-$\kappa$ material in dual-$\kappa$ spacers for 2:3 ratio

Fig. 5  Variation of $g_d$ and $g_m$ with respect to value of high-$\kappa$ material in dual-$\kappa$ spacers for 2:3 ratio

Fig. 6  Variability of (a) TGF and (b) $V_{ea}$ versus dielectric value of high-$\kappa$ material in dual-$\kappa$ spacers for 2:3 ratio
Table 1  Performance parameters of dual spacers on source, both-sides and drain side respectively for $\kappa = 15, 22.3, 30$

| Parameters | Source side | Both sides | Drain side |
|------------|-------------|------------|------------|
| $\kappa = 15$ | 4:1 | 1:4 | 3:2 | 2:3 | 4:1 | 1:4 | 3:2 | 2:3 | 4:1 | 1:4 | 3:2 | 2:3 |
| $I_{\text{OFF}}(A)$ | 1.62e-13 | 1.09e-13 | 9.76e-14 | 9.78e-14 | 1.53e-13 | 9.70e-14 | 1.21e-13 | 1.21e-13 | 2.75e-13 | 2.96e-13 | 1.38e-13 | 1.58e-13 |
| $I_{\text{ON}}(A)$ | 8.24e-06 | 9.29e-06 | 9.01e-06 | 9.22e-06 | 8.94e-06 | 6.84e-06 | 9.58e-06 | 1.02e-05 | 5.67e-06 | 6.11e-06 | 6.48e-06 | 6.01e-6 |
| $I_{\text{ON}}/I_{\text{OFF}}$ | 5.07e07 | 8.47e07 | 9.02e07 | 0.94e08 | 5.82e07 | 0.70e08 | 7.88e07 | 0.84e08 | 2.06e07 | 2.05e07 | 4.80e07 | 3.79e07 |
| $\text{DIBL}(\text{mV/V})$ | 151 | 146 | 146 | 144 | 150 | 154 | 148 | 148 | 162 | 175 | 160 | 160 |
| $\text{SS}(\text{mV/dec})$ | 76 | 75 | 74 | 75 | 76 | 75 | 75 | 75 | 77 | 78 | 76 | 76 |
| $g_m(S)$ | 1.95e-05 | 2.22e-05 | 2.17e-05 | 2.22e-05 | 2.12e-05 | 1.64e-05 | 2.32e-05 | 2.45e-05 | 1.25e-05 | 1.34e-05 | 1.47e-05 | 1.37e-05 |
| $\text{TGF}(V^{-1})$ | 26.19 | 26.51 | 26.66 | 26.58 | 26.44 | 26.38 | 26.56 | 26.52 | 25.94 | 25.81 | 26.46 | 26.36 |
| $\text{V}_{\text{ea}}(V)$ | 2.74 | 2.51 | 2.63 | 2.51 | 2.67 | 2.60 | 2.72 | 2.70 | 2.74 | 2.93 | 3.07 | 2.99 |
| $\text{V}_{\text{ea}}(V)$ | 42.03 | 41.72 | 42.22 | 41.62 | 42.63 | 42.38 | 43.17 | 43.54 | 40.65 | 41.92 | 43.67 | 42.99 |

Table 2  Performance parameters for 4:1 spacer proportion for $\kappa = 15$

| Dual-Spacer Placement | $I_{\text{ON}}(A)$ | $I_{\text{OFF}}(A)$ | $I_{\text{ON}}/I_{\text{OFF}}$ |
|-----------------------|---------------------|----------------------|--------------------------|
| Source Side           | 3.994e-06           | 1.149e-13            | 3.476e07                 |
| Drain Side            | 3.52743e-06         | 1.84394e-13          | 1.913e07                 |
| Both sides            | 4.354e-06           | 6.74e-14             | 0.646e08                 |

Table 3  Performance parameters for 3:2 spacer proportion for $\kappa = 15$

| Dual-Spacer Placement | $I_{\text{ON}}(A)$ | $I_{\text{OFF}}(A)$ | $I_{\text{ON}}/I_{\text{OFF}}$ |
|-----------------------|---------------------|----------------------|--------------------------|
| Source Side           | 4.423e-06           | 7.501e-14            | 0.589e08                 |
| Drain Side            | 3.649e-06           | 1.584e-13            | 2.3036e07                |
| Both sides            | 4.993e-06           | 3.52e-14             | 1.418e08                 |
Table 1 shows the device parameters obtained for dual-κ spacer placement along source, both-sides and drain respectively.

Proposed FinFET structure has been designed keeping fin width as 10 nm and spacer engineering has been executed. Tables 2, 3, 4, 5, 6, 7, 8, 9 and 10 demonstrate the performance for different k-values.

Case II. When $L_{ext} = 2 \times L_{g}$

Variation in dielectric value of high-κ in dual-κ spacers, placement of dual-κ spacers (source side, both-sides and drain side) and proportion of low and high-κ materials (4:1, 1:4, 3:2 and 2:3) has been implemented taking spacer extension length twice the gate length i.e. 30 nm. For all the cases, simulations have been done and various short channel effects and analog parameters are obtained.

(a) Effect of variation in spacer placement

Out of three cases, dual-κ (both-sides) structure has better performance parameters like $I_{ON}$, $I_{OFF}$, $I_{ON}/I_{OFF}$, SS, $g_m$, TGF, and $A_v$ than the other two designed devices for $L_{ext} = 2 \times L_{g}$ due to longer effective gate length ($L_{eff}$) as shown in Figs. 9 and 10. Performance parameters of Spacer placement along source and drain sides are also shown in Figs. 7, 8, 11, 12 respectively.

Table 4 Performance parameters for 2:3 spacer proportion for $k = 15$

| Dual-Spacer Placement | $I_{ON}$ (A) | $I_{OFF}$ (A) | $I_{ON}/I_{OFF}$ |
|-----------------------|--------------|---------------|------------------|
| Source Side           | 4.553e-06    | 7.033e-14     | 0.647e08         |
| Drain Side            | 3.749e-06    | 1.481e-13     | 2.53e07          |
| Both sides            | 4.937e-06    | 5.789e-14     | 0.853e08         |

Table 5 Performance parameters for 4:1 spacer proportion for $k = 22.3$

| Dual-Spacer Placement | $I_{ON}$ (A) | $I_{OFF}$ (A) | $I_{ON}/I_{OFF}$ |
|-----------------------|--------------|---------------|------------------|
| Source Side           | 4.132e-06    | 9.478e-14     | 0.436e08         |
| Drain Side            | 3.635e-06    | 1.466e-13     | 2.4795e07        |
| Both sides            | 4.517e-06    | 4.92e-14      | 0.918e08         |

Table 6 Performance parameters for 3:2 spacer proportion for $k = 22.3$

| Dual-Spacer Placement | $I_{ON}$ (A) | $I_{OFF}$ (A) | $I_{ON}/I_{OFF}$ |
|-----------------------|--------------|---------------|------------------|
| Source Side           | 4.593e-06    | 6.269e-14     | 0.733e08         |
| Drain Side            | 3.781e-06    | 1.185e-13     | 3.19e07          |
| Both sides            | 4.834e-06    | 5.186e-14     | 0.932e08         |

Table 7 Performance parameters for 2:3 spacer proportion for $k = 22.3$

| Dual-Spacer Placement | $I_{ON}$ (A) | $I_{OFF}$ (A) | $I_{ON}/I_{OFF}$ |
|-----------------------|--------------|---------------|------------------|
| Source Side           | 4.733e-06    | 5.888e-14     | 0.804e08         |
| Drain Side            | 3.897e-06    | 1.057e-13     | 3.6868e07        |
| Both sides            | 5.201e-06    | 4.375e-14     | 1.188e08         |

Table 8 Performance parameters for 4:1 spacer proportion for $k = 30$

| Dual-Spacer Placement | $I_{ON}$ (A) | $I_{OFF}$ (A) | $I_{ON}/I_{OFF}$ |
|-----------------------|--------------|---------------|------------------|
| Source Side           | 4.227e-06    | 8.25e-14      | 0.512e08         |
| Drain Side            | 3.708e-06    | 1.25e-13      | 2.9664e07        |
| Both sides            | 4.227e-06    | 8.25e-14      | 0.512e08         |

Table 9 Performance parameters for 3:2 spacer proportion for $k = 30$

| Dual-Spacer Placement | $I_{ON}$ (A) | $I_{OFF}$ (A) | $I_{ON}/I_{OFF}$ |
|-----------------------|--------------|---------------|------------------|
| Source Side           | 4.711e-06    | 5.503e-14     | 0.856e08         |
| Drain Side            | 3.872e-06    | 9.678e-14     | 0.4001e08        |
| Both sides            | 5.419e-06    | 2.013e-14     | 2.692e08         |

Table 10 Performance parameters for 2:3 spacer proportion for $k = 30$

| Dual-Spacer Placement | $I_{ON}$ (A) | $I_{OFF}$ (A) | $I_{ON}/I_{OFF}$ |
|-----------------------|--------------|---------------|------------------|
| Source Side           | 5.212e-06    | 2.505e-14     | 2.081e08         |
| Drain Side            | 3.997e-06    | 8.26e-14      | 0.4839e08        |
| Both sides            | 5.381e-06    | 3.531e-14     | 1.524e08         |
(b) Effect of variation in proportion of dual-$\kappa$ spacers

Simulated results shows that the 2:3 ratio of dual-$\kappa$ spacers has minimum $I_{OFF}$ of $8.96 \times 10^{-15}$ A, maximum $I_{ON}/I_{OFF}$ of order $10^9$ and minimum SS of 67.5 mV/dec for lower dielectric value of high-$\kappa$ material i.e. $\kappa = 15$ with dual-$\kappa$ spacers on both-sides.

(c) Effect of variation in high dielectric material

For $L_{ext} = 2 \times L_g$, improved parameters like $I_{OFF}$, $I_{ON}/I_{OFF}$ were obtained with dual-$\kappa$ spacer placement on
both sides for $\kappa = 15$ as shown in Fig. 9a. High gain of 50.21 dB is achieved for 2:3 proportion as demonstrated in Fig. 10b. Moreover, 112 mV/V value for DIBL is acquired for this ratio with improvement in parameters like early voltage, TGF and higher on-off current ratio than dual-$\kappa$ (source) and dual-$\kappa$ (drain) sides (Figs. 11 and 12).

4 Conclusion and Future Scope

In this work, the influence of spacer engineering in junctionless transistor has been analyzed. The proposed device was designed and simulated using Cogenda TCAD tool at 15 nm gate length. Through this work, effect of varying spacer extension length, placement of dual-$\kappa$ spacers, proportion of dual-$\kappa$ spacers and dielectric value of high-$\kappa$ has

![Fig. 9](image1.png)  
**Fig. 9** a Transfer characteristics b Variation of $g_{m}$ and TGF versus gate voltage by placing dual-$\kappa$ spacers on both sides for $\kappa = 15$

![Fig. 10](image2.png)  
**Fig. 10** a Plot of $g_{d}$ and $V_{eo}$ versus drain voltage b $A_{v}$ plot with respect to gate source supply of dual-$\kappa$ spacers (both-sides) for $\kappa = 15$
been studied. Simulated results shows that due longer effec-
tive gate channel length, dual-κ (both-sides) structure has
minimum short channel effects and its other parameters were
enhanced from the other two structures. However, dual-κ
spacer placement on drain side minimizes the fringing field
effect on drain side and this resulted in DIBL of 98 mV/V,
$V_{ea}$ of 4.02 V and $g_{d}$ of $9.78 \times 10^{-6}$ S. As the proportion of
high-κ spacer increases, on-off current ratio and intrinsic
gain increase as well as DIBL decrease. For short spacer
extension length i.e. 1.5 times gate length, as the dielectric
value of high-κ was increased, the short channel effects gets
reduced and better performance parameters like $I_{ON}$, DIBL
and $A_v$ were obtained. For longer spacer extension length
(twice the gate length), improvement in device characteris-
tics such as $I_{OFF}$ of $8.96 \times 10^{-15}$ A, $I_{ON}/I_{OFF}$ ratio of $0.67\times$
$10^{6}$, SS of 67.5 mV/dec, TGF of 30.12 $V^{-1}$ was observed

Fig. 11  a Drain current versus gate voltage b $g_{m}$ and TGF versus gate voltage by employing dual-κ spacers on drain side only for $\kappa = 15$

Fig. 12  a Plot of $g_{d}$ and $V_{ea}$ with respect to drain voltage (on y-axis) b $A_v$ plot with respect to gate voltage of dual-κ spacers on drain side for $\kappa = 15$
for low value of high-κ dielectric. Therefore, to get the optimum parameters of the device, a trade-off is required for low leakage applications.

This work can be extended by implementing and analyzing the concept of spacer engineering in rectzoid fin shaped transistors [27] which proved to be effective in controlling short channel effects and providing better analog performance at nanoscale.

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Author Contributions All authors contributed in the preparation of final manuscript.

Data Availability Results have been extracted by work done on TCAD tool. Data is available with authors and can be provided to Journal when needed.

Declarations

Consent to Participate All the authors give consent to submit paper in this journal.

Consent for Publication The authors have agreed for submitting this manuscript in Silicon Journal and agree to publish, if accepted. It has not been sent elsewhere for consideration.

Conflict of Interest Authors does not have any conflicts of interest.

Ethics Approval This work complies with the ethical standards.

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