Trusted IP Solution in Multi-tenant Cloud FPGA Platform

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Abstract—Because FPGAs outperform traditional processing cores like CPUs and GPUs in terms of performance per watt and flexibility, they are being used more and more in cloud and data center applications. There are growing worries about the security risks posed by multi-tenant sharing as the demand for hardware acceleration increases and gradually gives way to FPGA multi-tenancy in the cloud. The confidentiality, integrity, and availability of FPGA-accelerated applications may be compromised if space-shared FPGAs are made available to many cloud tenants. We propose a root of trust-based trusted execution mechanism called TrustToken to prevent harmful software-level attackers from getting unauthorized access and jeopardizing security. With safe key creation and truly random sources, TrustToken creates a security block that serves as the foundation of trust-based IP security. By offering crucial security characteristics, such as secure, isolated execution and trusted user interaction, TrustToken only permits trustworthy connection between the non-trusted third-party IP and the rest of the SoC environment. The suggested approach does this by connecting the third-party IP interface to the TrustToken Controller and running runtime checks on the correctness of the IP authorization/Token signals. With an emphasis on software-based assaults targeting unauthorized access and information leakage, we offer a noble hardware/software architecture for trusted execution in FPGA-accelerated clouds and data centers.

Index Terms—FPGA, multi-tenant, cloud, TrustToken, cloud FPGA, IP

I. INTRODUCTION

FPGAs are being introduced into the cloud and data center platforms for increased performance, computation, and parallelism benefits over existing accelerators such as GPUs. Technology has increased the demand for high-speed cloud computation over the last few years. Commercial and public cloud providers initiated using FPGAs in their cloud and data centers to provide tenants to customize their hardware accelerators in the cloud. The integration of FPGAs in the cloud was initiated after Microsoft published its research on Catapult in 2014 [1]. Since then, it has become a niche technology for cloud service platforms, and major cloud provider giants, e.g., Amazon [2], Alibaba [3], Baidu [4], etc., have integrated FPGAs into their platforms. For computationally intensive loads like machine learning, digital image processing, extensive data analytics, genomics, etc., users can exploit FPGA acceleration in cloud platforms. By mentioning three concrete examples, we can express the unique advantages of FPGAs over traditional accelerators. 1. Microsoft Bing search engine experienced a 50 percent increase in throughput, or a 25 percent reduction in latency by using FPGAs in their data centers [1]. 2. Using Amazon AWS FPGA F1 instance, the Edico Genome project has over ten times the speed and performance increase for analyzing genome sequences. and 3. Introduction of Xilinx Versal FPGAs for real-time video compression and encoding in the cloud platform has significantly reduced the operating cost by reducing the encoding bitrate by 20%, [5].

Multi-tenant FPGA platforms have multiple security concerns even after improving performance significantly. Cloud FPGAs allow tenants to drive their custom hardware designs on cloud FPGA fabric, potentially exposing multiple security risks for the adversaries, unlike CPUs and GPUs. Multi-tenancy in cloud FPGAs can create some unique hardware-related security risks such as side-channel attacks [6] where sensitive information of the hardware surface is leaked or transferred by invasive/non-invasive probing, or covert channel creation between the tenant’s fabric which attacker can create a hidden channel layer between each other to transmit confidential information [7]. Malicious adversaries can also launch Denial of Service (DOS) in any layer of the cloud system, including user or infrastructure level [7]. Malicious bitstream upload into the FPGA fabric is one of the major attacks besides traditional cloud FPGA attacks, which can lead to shutdown or faulty results [8]. Due to hardware fabric intervention and manipulation, short circuits fault, performance degradation, or shutdown major public cloud provides, e.g., Amazon only offers single bitstream deployment for each FPGA board. Whereas, in academics, multi-tenancy is under active research. In the case of multi-tenant cloud, FPGA security risk is more severe and intensive, as the same FPGA board fabric is shared among different tenants, which exposes the hardware surface more openly. In many reconfigurable SoCs sandboxing architecture, e.g., Xilinx Zynq - 7000 SoC, UltraScale+ [9], ARM TrustZone the secure key is stored in battery-backed RAM (BBRAM) or eFuse medium. However, these methods have the following disadvantages: 1) They still need some secure random key generation methods like random number generator (RNG) as a source of the root of trust. 2) eFuse is a fixed, non-update-able memory. 3) A physical battery is required for the BBRAM method. 4) Storing secret keys in
the non-volatile memory of the cloud FPGA boards seems impracticable as the boards are rented for a specific period, and retrieving the keys from the NVM would be impossible after the tenant lease is expired. In this study, a cutting-edge method for creating identity tokens in a multi-tenant cloud FPGA platform without requiring non-volatile memory (NVM) is proposed. In order to address the aforementioned issues with the multi-tenant cloud platform, we present a brand-new, effective, and trusted solution in this paper called the TrustToken. Without employing non-volatile memory or a secure boot mechanism, we created identity tokens during runtime using an asymmetric cryptographic method. We are motivated and inspired by the Google Chromium sandboxing [10] concept to create a secure execution environment in the background of a multi-tenant platform by allocating Tokens for each IP core. To create distinct token environment in the ARM TrustZone architecture, we are susceptible to rowhammer attacks and denial-of-service attacks [16]. Weak and inefficient authentication mechanisms are the primary security concern of ARM TrustZone technology. Several research works have reported unauthorized kernel-level privilege gain on ARM TrustZone platforms in normal world environments [16]. Also, a trusted kernel region can have several vulnerabilities which can damage the whole TEE. [16]. Benhani et al. [17] have published a paper demonstrating several attacks on TrustZone from the simple CAD command with some simple lines of code.

III. BACKGROUND

A. Multi-tenant Cloud FPGA

FPGAs have mostly been used in the verification phase of ASIC designs over the previous ten years, where the ASIC design was implemented for validation and verification phases before it was actually produced. Additionally, specialized markets and research programs had some other applications. However, FPGAs are gaining popularity as an alternative for CPUs and GPUs due to high performance processing and parallelism. FPGA boards are both available on the market today as supported devices that may be connected by PCIe ports or as part of the same System-on-Chip (SoC). The integration of FPGA in cloud computing platforms to enable customers to create their hardware accelerators is one of the most recent trends in FPGA dominance. There are typically four basic methods for deploying FPGA boards in cloud data centers. As follows: 1. Coprocessor (FPGA is coupled with CPU by PCIe cards) 2. Distinct (FPGA is deployed as a standalone component) 3. Bump-in-the-wire (FPGA is positioned between the NIC and the internet) System-on-chip, and 4. (FPGA is fabricated in same chip die along with CPU). A cloud FPGA design known as multi-tenancy rents out the FPGA fabric to many users or tenants within the same time period. The concept of spatial silicon FPGA device sharing among several tenants is integrated into multi-tenancy.

B. Physical Unclonable Function

In order to produce distinctive and unique ubiquitous used keys, Physical Unclonable Function uses the manufacturing variation of a silicon nanocircuit [18]. PUF can be used
for a variety of cryptographic tasks, including authorization, random number generation, and authentication. The PUF theory states that even if two or more devices are identical in design, manufacturing variance will cause them to have distinct electrical properties. This variation is unpredictable and can not be estimated through observation, neither optical nor SEM. A PUF can be considered a black box, where an input challenge pair generates an output response pair. Due to manufacturing variation, the generated output response should be unique and can be used as a unique ID or authentication key. The most common existing PUF designs are Arbiter PUF, Ring Oscillator, XOR, SRAM, etc. The three most popular indicators are employed to assess the performance of PUF produced keys. They are uniqueness, randomness, and bit error rate.

C. ARM TRUSTZONE

In order to isolate trusted and untrusted software and hardware, ARM TrustZone refers to a secure execution environment (SEE) [19]. It also goes by the name Trusted Execution Environment (TEE), and it contains a monitor that manages how these two different worlds communicate with one another. TEE TrustZone is an embedded security technology that uses two physically independent processors for the trusted and untrusted worlds. This architecture’s primary flaw is the fact that similar peripherals like Ethernet, DRAM, UART, etc. are shared. Combining a few IP blocks, ARM TrustZone enables the division of groups of I/O Peripherals, Processors, and Memory into two distinct universes. Two NS bit registers on the ARM TrustZone platform are dedicated to implementing the isolation of a software process. [19].

![Fig. 1. The architecture of the ARM Trustzone](image)

D. Hardware Trojan and Design For Trust

According to [20], a hardware Trojan (HT) is defined as a malicious attacker who has knowingly altered a system circuit and caused a change from intended behavior when the circuit is implemented. Because it can leak private information or alter a circuit’s specifications during operation, HT poses a serious threat to SoC design. By reducing the circuit’s total system functionality, HT can cause an emergency. It is exceedingly challenging to monitor this HT’s negative effects during the verification stage because it is frequently deployed in stealth mode and only activated under unusual circumstances.

IV. THREAT MODEL AND SYSTEM PROPERTIES

Our threat model can be separated into two distinct explicit scenarios: Hardware Trojan and Illegal software access. Every IP is viewed as untrusted and capable of having dangerous Trojan components concealed inside it when we consider the likely first threat model. They can act under unusual circumstances. We assume that they are only used in run-time environment circumstances and are secretly carried out from the IP’s internal architecture. The SoC IP integrator division is regarded to be reliable. In this case, the TrustToken can offer defense against unwanted data access, access control, alterations, and the leakage of any sensitive data from the IP core to the outside world. In the second scenario, we consider a malevolent attacker who can steal, modify, or leak sensitive information by obtaining unauthorized software access from the embedded SoC world. Figure 2, as an illustration, depicts an instance of malevolent unauthorized access. In this diagram, two different CPUs that are a part of the same SoC system are powering four software-level apps. In the hardware level design, four special IPs are added in the tenant fabric. These IPs are accessible from the software side and are identified by the same color as the related application. By using the suggested architecture model, an access request made by software Application 3 (three) to IP Core 4 (four) can be marked as unauthorized and isolated.

![Fig. 2. Illegal software access request by Application 3 running on CPU](image)

The physical assaults carried out by physical apparatus were not taken into account in this essay because they fell outside of its scope. Attacks against hardware such as side-channel, probing, snooping, timing, denial-of-service, fault injection, etc. were not included in the attack scenarios. To summarize, we have considered the following threat models when describing our architecture:

1) Any malicious HT attempting to execute in runtime environments while hiding inside an IP core. We presume that concealed HT can evade detection by current CAD tools and remain undiscovered up until the payload condition is activated.

2) Any malevolent HT attempting to control access or transfer data without authorization. We take into account the possibility that attackers could purposefully alter
the computing result by overwriting the data on a particular communication channel. We also consider that a malicious attacker could potentially cause data leakage by altering the IP core’s operating mode.

3) Any malicious attacker trying to access other programs’ sensitive data without authorization or leak it from the CPU core.

A. Design assumptions

While developing our proposed solution, we have taken some key points under consideration.

1) Multi-tenancy. Our proposed protocol targets the multi-tenant cloud FPGA platform and observe the implementations on this platform. We assume that our proposed protocol is designed to perform in run time environment.

2) Adaptability. Although this article insist on building Token based security features for non-trusted IPs in multi-tenant cloud FPGA platform, this protocol can be easily adapted only in re configurable Programmable Logic (PL) fabric-based system without the use of processor system.

3) Bus Specification. For developing our protocol, we have considered all the interfaces established by AMBA bus specifications. We predict that our security protocol will adopt all necessary standard AMBA interfaces like AXI, AHB, APB, etc.

V. PROPOSED ARCHITECTURE

With the help of the TrustToken, a SoC owner will be able to offer safe and adaptable IP core communication without the need for any additional secure storage services or systems. The TrustToken Controller, TrustWrappers, and TokenGenerator are the three parts that make up the detailed architecture of our suggested solution, which is shown in Figure 3.

a) TrustToken Controller: A separate centralized IP called the TrustToken controller is responsible for creating special Tokens/IDs for the IPs and upholding the security norms in the networked environment. To assert the validity check, any IP Integrator must modify the value of the token’s parameter designated as integrity (Fig 4). The isolation feature will be disabled when this value is set to LOW. When HIGH, it will enforce the IP’s isolation mechanism and, following a successful authorisation, execute the IP in a non-trusted zone. The Central TrustToken Controller receives the keys once they have been generated by the PUF module and uses them to assign token IDs. The central security command center of the entire SoC system, the Central TrustToken Controller is in charge of distributing all Token IDs provided by the integrated PUF module. The TrustToken controller verifies the Token ID received with the list of securely stored Tokens whenever any IP wants a READ/WRITE access. It will immediately allow the data channel for communication after a successful permission or immediately disable it.

b) Trust Wrapper: Every IP in our suggested design will be protected by a security wrapper called TrustWrapper. There are two distinct operating interfaces for TrustWrapper: Secured and Non-secured. The bus signals ID and Token will be added to every non-trusted IP core that is marked as non-secured. We rely on adding additional bus signals to the current AMBA bus protocol specifications in place of providing any register level isolation method or separate bus protocol for the secure isolation. It might be necessary to change the interconnect bridge mechanism for security check activities if a separate bus protocol for isolation is added. This could lead to new vulnerabilities. Additionally, in order to convey IPs ID and Token information uniformly and uniquely, a bus protocol would need to handle all conceivable bus protocol parameters, such as bandwidth, channel length, burst size, streaming techniques, etc. The Central TrustToken Controller will issue an authorization request for each data transaction started by the untrusted IP core. The controller block should receive valid and recent security data (IDs and Tokens) from non-trusted IPs via the security wrapper.

c) Token Generator: The enhanced Ring Oscillator-based PUF, which is more stable than the original Ring Oscillator PUF, is implemented due to its low overhead and latency. Comparing Ring Oscillator-based PUF to SRAM PUF, Arbiter PUF, TRNG, or other crypto cores, the results for latency and resource consumption are encouraging. Our unique Ring Oscillator-based PUF system can produce keys with a 256-bit width. It satisfies our requirement for offering heterogeneous SoC security by having an acknowledged uniqueness and randomization. Strong PUF is characterized as having the following security qualities in one of the fundamental studies on PUF [21], 1. The PUF circuit cannot be physically duplicated. 2. It will enable a large number of Challenge-Response Pairs (CRPs), preventing the adversary from launching a brute force assault in a reasonable amount of time. According to the Strong PUF definition, the suggested work qualifies as a strong PUF and will be the best option to implement for the suggested SoC security justification.

VI. PROPOSED PROTOCOL EVALUATION

The protocol robustness in the outlined attack scenarios was our goal in this section.

A. Case 1: ID signals being compromised

We described a potential attack scenario where a software level attack was introduced from an arbitrary application core in section IV. By launching a transaction request from another IP core, the malicious adversaries configure a secured IP core and try to access the victim IP. All assigned IDs and Tokens, as well as their corresponding source and destination IPs, are nevertheless recorded by Central Trust Controller. Since the attacker tried to get access illegally from a different IP core, this attempt will be checked against the saved credentials and blocked if they don’t match.

B. Case 2: Insecure access control

At the AXI interconnect level security check is carried out in the case of Xilinx TrustZone, [9], and it plays a crucial part
in the security. There is a significant security risk because this Interconnect crossbar is also in charge of determining the security state of each transaction on the associated AXI bus. By altering a few security signals, any hostile attacker wishing to breach the security layer can simply control the AXI connection crossbar. This flaw was fixed with the suggested secure architecture, which imposed a strong and secure system that makes it very impossible for any access control attack to take control of the internal signals of the Central TrustToken Controller. With a PUF-based Token ID key, the Central TrustToken Controller encrypts itself, and as a result prevents any illegal use of this IP’s access control.

C. Case 3: Comprising INTEGRITY LEVEL

The status of the INTEGRITY LEVEL signals determines whether any non-trusted IP is connected to the Central TrustToken Controller for secure isolation. Only an IP Integrator can declare the INTEGRITY STATUS at the hardware level, as was previously indicated in the thread model section. This provides defense against any CAD or RTL script attack by requiring adequate authorisation for any alteration of this signal under runtime conditions. Additionally, any malicious attacker must display their PUF-based Token ID of the untrusted IP in order to change the status of the protection level. Benhani et al. [17] demonstrated in their work that a malicious attacker could only significantly disrupt the Arm TrustZone AWPROT/ARPROT signal to cause a Denial of Service (DoS) disruption in the SoC. The suggested secure transition paradigm, which stipulates that a change request should additionally go into an additional authorisation layer, can be used to avoid this situation.

VII. TRUSTTOKEN IMPLEMENTATION IN MULTI-TENANT CLOUD

The experimental setup and overhead calculations needed to create our suggested architecture and assess the robustness of the suggested TrustToken framework are described in this section. The primary setup involved calculating overhead and latency for data exchanges as well as effectively implementing the design.

A. Cloud FPGA Setup

The cloud is configured on a Dell R7415l EMC server with an AMD Epyc 7251 processor clocked at 2.09GHz and 64GB of RAM. The node is running CentOS-7 with a 3.10.0 kernel. The Dell Server and the Xilinx Alveo u50 board were linked by PCIe express. Xilinx Runtime Library (XRT) was used to initiate multi-tenant domains in the FPGA and reconfigure the regions to different tenants.

B. Proposed Protocol Performance

By implementing and synthesizing our proposed TrustToken protocol on an Alveo u50 board, we evaluated its performance. Four symmetric crypto IP cores have TrustWrappers attached around them for evaluation (AES,DES,TRNG and RSA). For the purpose of evaluating the suggested architecture model, each TrustWrapper was given a HIGH integrity state assignment. Additionally, we launched five distinct ARM-based programs to access the computational output from the crypto cores. We successfully implemented a trusted execution environment using the TrustToken concept in our implementation and tracked the outcomes. We discussed a potential software level attack scenario in section IV where a hostile attacker from Application 3 (mapped to TRNG hardware IP core) tries to create an approved access path to RSA IP core. We put this scenario into action, and the TrustToken module stopped the attack. We also created a Xilinx TrustZone enclave using the VIVADO CAD tool, based on the work Xilinx [22], to compare the protocol performance with the proposed TrustToken protocol. We successfully launch a straightforward CAD Tool attack against the Xilinx TrustZone by changing the AWPROT signal in a runtime circumstance scenario. Similar to how the attack attempt in the suggested technique failed, the protocol’s resistance to attack by CAD tools is clearly demonstrated.

C. The effectiveness of the generated keys

The results of the hamming distance calculation using the PUF keys are shown in Fig. 5. The hamming distance is
closely rounded between 40 and 60 percent, as seen in the figure, demonstrating the keys’ stability and efficacy and being extremely similar to the ideal properties of PUF [18]. The general characterizations of the PUF were compiled in Table I. Our internal PUF architecture has 512 oscillators and is capable of producing keys that are 256 bits wide.

![Figure 5. Hamming Distance between the PUF keys.](image-url)

**Table I**

| Characterizations of the Ring Oscillator PUF |
|--------------------------------------------|
| **Properties** | **Value** |
| Oscillators Numbers | 512 |
| Number of Keys | 256 |
| Single Key Length | 256 bits |
| single Challenge Input Length | 2 bytes |
| Randomness | 46.62% |
| Uniqueness | 48.18% |
| Reliability | 100% |

VIII. CONCLUSION

In a multi-tenant cloud FPGA platform, this study suggests a Token-based secure cloud architecture for untrusted IP. Using a root of trust-based security module, the TrustToken architecture adds an extra layer of security against unwanted access control and assaults in multi-tenant platform. The protocol can take advantage of the reconfigurable features of the SoC-based FPGA platform and uses a bespoke Ring Oscillator-based PUF module to create keys. Our method eliminates the uses of NVM memory for secure storage of keys as they are uncertain in context of multi-tenant platform.

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