Challenges toward the application of high-speed digital signaling to multi-drop transmission system with reflection compensation lines

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Abstract: Waveform distortion due to reflections in high-speed digital signaling is a classical issue of the signal integrity especially for the multi-drop transmission system. In general, the reflection characteristics and improvement measures of the multi-drop transmission strongly depend on the topology of the system in question, such as bus-configuration, star, ring, and so on. In this paper, we discuss a method of RCL (Reflection Compensation Line), formally reported in [6] as a reflection cancelling scheme, that can be applied to the bus-type multi-drop transmission system, whose length of main bus segments and stub lines are all isometric. Assuming practical application of our RCL technique to high-speed digital signaling, data rate of over 10 Gbps, the optimal set of transmission parameters are deduced by means of numerical optimization algorithm, and the performance of the RCL is discussed.

Keywords: multi-drop transmission system, impedance matching, impulse response, reflection compensation line, signal integrity

Classification: Electromagnetic Compatibility (EMC)

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1 Introduction

A multi-drop transmission is one of common signaling configuration for backplane system [1, 2, 3] or DDR-SDRAM wiring [4]. A main challenge for high-speed signal transmission in the multi-drop transmission system is degradation of the signal integrity due to reflections caused by the impedance mismatch at the branch points of the stub lines. In order to reduce the reflection, one basic approach of Asymmetrical Power Splitter (APS), which is based on an impedance matching scheme, is detailed in [1, 2]. Although the APS does not suffer from the issue of reflections, the disadvantage is that the required trace impedance becomes excessively low, and this makes the system very power consuming, even with a moderate number of receivers.

For another approach, Stub Series Terminated Logic (SSTL) is a method well-known for DDR SDRAM wiring [5], in which series resistance elements are connected in each stub line to reduce the reflection. The STTL also does not suffer from the issue of reflections, but the drawback is power and amplitude loss due to the resistive elements.

In order to achieve high-speed digital signaling, data rate of over 10 Gbps, avoiding those drawbacks seen in the past works, a methodology of reflection compensation line (RCL) is discussed in this paper. A typical configuration of bus-type multi-drop transmission system with four receiver nodes (#1–#4) is shown in Fig. 1(a). Every segment of the main bus and the stub line is constructed in an isometric length of $L$. Both ends of the main bus are terminated in a matched impedance of $Z$. The characteristic impedance of the stub lines is $Z_0$ and the termination resistance of the $i$-th node is $R_i$ ($R_i > Z_0$). Two RCLs, reported in [6], are placed to both ends of the main bus line. The purpose of the RCLs is to intentionally cause the multiple reflections and cancel the wave distortion to restore the ideal waveform at the receivers. The appropriate amplitude of the reflection is optimally designed by the termination resistors placed at each of the receiver node.

Fig. 1(b) shows the contribution of the individual reflection waves observed at the receiver node $i$. A typical 1st order delayed reflection wave $R_i^{(1st)}$ at the receiver node $i$ is formed by superposition of the positive reflections (①, ④) and the negative reflections (②, ③), and the overall amplitude and polarity of $R_i^{(1st)}$ is determined by all possible combinations of those individual reflections.

This situation is also indicated in Fig. 1(c) as an impulse response at the receiver node. It should be noted that the delay time of all reflection waves at the receivers will be aligned in discrete multiples of round-trip time of each segment ($\tau_{2L}$), since
the main bus segments and the stub lines are all constructed in an isometric length of L.

2 Evaluation of the reflections with numerical optimization

As shown in Fig. 1, the trace impedance of the main bus segments and the stub line is $Z$ and $Z_0$, respectively. In this case, the reflection coefficient $\Gamma$ and the transmission coefficient $T$, which are seen from the main bus to the stub line, are

$$\Gamma = \frac{(Z_0 \parallel Z) - Z}{(Z_0 \parallel Z) + Z}, \quad T = \frac{2(Z_0 \parallel Z)}{(Z_0 \parallel Z) + Z} \tag{1}$$

respectively, and the coefficients $\Gamma_s$ and $T_s$, which are seen from the stub line to the main bus, are

$$\Gamma_s = \frac{Z/2 - Z_0}{Z/2 + Z_0}, \quad T_s = \frac{Z}{Z/2 + Z_0} \tag{2}$$

respectively. Also, the reflection coefficient $\Gamma_i$ at the receiver terminal of the stub line #i is

$$\Gamma_i = \frac{R_i - Z_0}{R_i + Z_0} \tag{3}$$

if the terminal resistance of the stub line is $R_i$.

With these transmission and reflection coefficients, the transfer coefficient of the 1st order delayed reflection (Fig. 1(c)) observed at the receiver node #i is expressed as

$$R_i^{(1st)} = \frac{2R_i}{Z_0 + R_i} \cdot \sum_{j=0}^{i-1} T^{(i-j)} \cdot (\Gamma T T) \cdot T^{(j-1)}$$

$$+ \frac{2R_i}{Z_0 + R_i} \cdot \sum_{j=0}^{i-1} T^{(i-j)} \cdot (T_s \Gamma T T) \cdot T^{(j-1)}$$
\[
\frac{2R_i}{Z_0 + R_i} \cdot (T^i \Gamma T) \cdot T^{(i-1)} + \frac{2R_i}{Z_0 + R_i} \cdot (F_i \Gamma T) \cdot T^{(i-1)},
\] (4)

The first row of (4) is the contribution of the multiple reflection generated at the main bus segment of the upstream side of the \( #i \) junction, which is shown by \( \mathbb{1} \) in Fig. 1(b). The second row of (4) is the reflections generated at the terminals of the stub lines of the upstream side of the \( #i \) junction, which is shown by \( \mathbb{3} \) in Fig. 1(b). Finally, the third and the fourth row of (4) are the reflections shown by \( \mathbb{2} \) and \( \mathbb{3} \) in Fig. 1(b), respectively. The transfer coefficient of the 2nd order delayed reflection \( R_i^{(2nd)} \) can be considered in same manner and the precise expression is discussed in [6].

The performance of the multi-drop transmission system indicated in Fig. 1 is evaluated by means of numerical optimization. The objective function \( f(x) \) is designed to be

\[
f(x) = f(Z_0, R_0, R_1, \ldots, R_3)
= \Delta_1 + \Delta_2,
\] (5)

\[
\Delta_1 = \sum_{i=1}^{4} (S_{\text{target}} - S_i)^2,
\] (6)

\[
\Delta_2 = \sum_{i=1}^{4} \left\{ \left( R_i^{(1st)} \right)^2 + \left( R_i^{(2nd)} \right)^2 \right\},
\] (7)

where \( \Delta_1 \) is the square sum of variance from the target amplitude of the main wave. The transfer coefficients of main waves \( S_i \) \( (i = 1, \ldots, 4) \) are expressed as,

\[
S_i = \frac{2R_i}{Z_0 + R_i} \cdot (T)^i,
\] (8)

and target value of the coefficient \( S_{\text{target}} \) in (6) is assumed to be 0.8 in this paper. Also, \( \Delta_2 \) is the square sum of coefficients of the reflection waves observed at each receiver device. The contribution of 1st and 2nd order delayed reflections are considered in this paper since the higher order delays are assumed to be small and negligible.

The optimal set of the transmission parameters are deduced by numerical optimization. The characteristic impedance \( Z = 50 \Omega \) for the main bus line, and a constraint of \( Z_0 \leq 85 \Omega \) for the stub line is assumed for practical PCB implementation. By evaluating the objective function (5), the optimal values of \( Z_0 \) and \( R_i \) are deduced by Genetic Algorithm (GA). The results are shown in Table I. For comparison, results of some other types of algorithm, such as the simulated annealing (SA) and the Gradient Descent (GD) are also shown in Table I.

Although similar performance is gained with GA and SA, GD tend to stuck at local minimum depending on the initial value. This indicates that the escaping mechanism from local minimum, implemented in GA and SA, is critical for this kind of problem. We choose a result of GA for further evaluation of the SPICE simulation in this paper.
Table I. Optimal set of parameters

| Parameter | GA | SA | GD | Fixed |
|-----------|----|----|----|-------|
| $Z$       | 50Ω | 50Ω | 50Ω | 50Ω   | Trace Impedance of the Main bus. |
| $Z_0$     | 85Ω | 85Ω | 85Ω | 78Ω   | 50Ω   | Trace Impedance of the Stub Lines |
| $R_1$     | 94Ω | 98Ω | 108Ω | 88Ω   | 1kΩ   | Termination of the Receiver #1 |
| $R_2$     | 148Ω | 141Ω | 157Ω | 94Ω   | 1kΩ   | Termination of the Receiver #2 |
| $R_3$     | 287Ω | 267Ω | 236Ω | 133Ω  | 1kΩ   | Termination of the Receiver #3 |
| $R_4$     | 2kΩ | 2kΩ | 2kΩ | 744Ω  | 1kΩ   | Termination of the Receiver #4 |
| $R_5$     | 182Ω | 107Ω | 123Ω | -     | -     | Termination of the RCL #0 |
|           | 323Ω | 330Ω | 126Ω | -     | -     | Termination of the RCL #5 |

3 Waveform analysis and validation of the RCL

Fig. 2 shows the results of SPICE simulation with the transmission parameters indicated in Table I. For the simulation, the amplitude of the signal source is $V_{SRC} = 1 \text{ V}$ at $50\Omega$ load. All the length of the stub lines and main bus segments are aligned to $\tau_{2L} = 120\text{ ps}$ of propagation delay. The lossless condition for all the transmission lines are assumed throughout the simulation.

If we focus on the result of receiver node #1 in Fig. 2(a-1), a $1^{st}$ order delayed reflection with large negative polarity in conventional system (without RCL, fixed termination) is observed. This negative peak comes from the reflection from the
downstream side of main bus, indicated as ② and ③ in Fig. 1(b). In comparison to this, the 1st order delayed reflection in the proposed system (with RCL, GA optimization) is greatly reduced. This is because, the effect of cancellation with the positive reflections from upstream side, shown as ① and ④ in Fig. 1(b), is gained by the RCL.

Fig. 2(b) shows the results of 10 Gbps eye-diagram in the multi-drop configuration with the RCLs and the parameters deduced by GA. Since the arbitrary waveform of signal source is expressed as the convolution of the impulse response, the performance of the signal transmission observed by the 10 Gbps signal source is intrinsically the same as those obtained by the impulse response. This result indicates the availability of applying 10 Gbps signaling to the multi-drop transmission system with the RCL.

Fig. 2(c) shows the comparison of 10 Gbps eye-diagram observed at the node #1 in condition of with/without RCLs. A result of the standard deviation of the jitter is $\sigma = 4.2$ ps (with RCL, GA optimization) in Fig. 2(c-1) and shows better performance if compared to $\sigma = 7.3$ ps (without RCL, GA optimization) in Fig. 2(c-2). Also, Fig. 2(c-3) is a result with the fixed parameters $R_i = 1 \, k\Omega$ (without RCL), shown in Table I, and the data rate of 10 Gbps is not possible due to the waveform distortion by the reflection.

4 Conclusion

In order to achieve high-speed signaling, data rate of over 10 Gbps, a methodology of reflection compensation line (RCL) that can be applied to the bus-type multi-drop transmission is discussed. By virtue of the RCLs, placed at both end of the main bus, the multiple reflection waves are intentionally generated to cancel the distortion at the receivers. The optimal set of transmission parameters is determined by means of numerical optimization, and the performance of the reflection cancelling is confirmed using SPICE simulation. The simulation results showed the availability of applying 10 Gbps signaling to the multi-drop transmission system with the RCL.

Although the application of the RCL is restricted to multi-drop configuration consisting of isometric lengths of segments, the method is still expected to be useful for the high-speed backplane systems or the DDR SDRAM wiring. Our future work toward the practical application of the RCL is to demonstrate the actual multi-layered PCB design and verify the performance of the RCL using test board measurements including transmission loss or unwanted parasitic effects of PCB.