FPGA based Green Digital Clock Design for Network Synchronization using LVCMOS I/O Standard

Deepa Singh*

Atal Bihari Vajpayee-Indian Institute of Information Technology, Gwalior - 474001, Madhya Pradesh, India; deepa@iiitm.ac.in

Abstract

The idea is to develop a green digital clock design that consumes least amount of power for its network specific operation. Low Voltage complementary metal oxide semiconductor i.e. LVCMOS IO standard is used at fixed temperature and changing output load at various frequencies. FPGA family used is Virtex-6 and software used of simulation of proposed algorithm for digital clock is Xilinx. Coding is done using Verilog. The results are taken for LVCMOS at frequency of 0.1GHz, 1GHz, 10GHz and 100 GHz and data is collected to prove it green digital clock. For making any device green means the amount of power consumed by it should be small with desirable output. There is 89.60%, 98.56%, 99.46% and 99.56% saving in IOs power when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively.

Keywords: Digital Clock, Energy Efficient, FPGA, LVCMOS25, Low Power

1. Introduction

In this paper default I/O standard i.e. LVCMOS25 is used for calculating total power consumed for FPGA based low power digital clock when virtex6 family of FPGA is used. At different frequencies power consumption for LVCMOS25 is calculated by varying the output load between 5pF to 5000pF. We notice that the value of clock, logic and signal don't change for different output load and have minute difference at different frequencies only. The results are also represented by graphs for more clear view. It is also clear that variation in output load makes a large difference in the I/O and total power consumed and small difference in leakage. Family of FPGA used is Virtex6 and sub families of Virtex-6 FPGA are:

*Author for correspondence
Above shown is Schematic of the digital clock for which the total power dissipated is calculated. Total power constitutes many factors and adding up all these gives the total amount of power consumed for the design. These factors are:

1. Clock  
2. Logic  
3. Signal  
4. I/Os  
5. Leakage

These five factors add up to give the total amount of power. Values of all these five factors are calculated and saving in total power is for digital clock are calculated.

2. Related Work

We have used LVCMOS for our work which is not limited to single frequency but at different frequencies and varying the output load. So there are some papers that are related to our work and helpful in studying more about the work and also helpful in studying the work already done in this area. Some of the work studied by us is mention in following text. LVCMOS I/O standard is used in million MHz green counter on FPGA\(^1\). LVCMOS based energy efficient solar charge sensor is design on FPGA\(^2\). A cost-effective high-power S-band 6-bit phase shifter is implemented with integrated LVCMOS control logic\(^3\). LVCMOS I/O Standard and Drive Strength are main basis of Green Design on FPGA\(^4\). Generic robust LVCMOS-compatible control logic is developed for GaAs HEMT switches\(^5\). LVCMOS is used to deliver Energy Efficient Vedic Multiplier Design on FPGA\(^6\). Aspects and solutions for designing standard LVCMOS I/O buffers in 90nm process is under consideration in\(^7\).

3. Role of LVCMOS in Digital Clock

There is 89-99 % saving in the clock power when we reduce frequency from 100GHz to 10GHz, 1GHz and 0.1GHz. There is 60-100 % reduction in the logic power, when we scale down frequency from 100GHz to 10GHz, 1GHz and 0.1GHz. There is 90-100 % saving in the signal power, when we reduce frequency from 100GHz to 10GHz, 1GHz and 0.1GHz as shown in Table 1 and Figure 4.

| Frequency (GHz) | 0.1 | 1   | 10  | 100 |
|-----------------|-----|-----|-----|-----|
| Clock Power     | 0.003 | 0.021 | 0.201 | 1.987 |
| Logic Power     | 0.000 | 0.002 | 0.012 | 0.030 |
| Signals Power   | 0.000 | 0.002 | 0.023 | 0.236 |

Table 1. Clock, logic and signals power in watt at different frequencies

![Graphical representation of clock, logic and signals power.](image)

![Graphical representation of I/Os, leakage and total power.](image)

Table 2. I/Os, Leakage and power in watt at frequency 0.1GHz

| Output Load(pF) | 0.5 | 5  | 50  | 500 | 5000 |
|-----------------|-----|----|-----|-----|------|
| I/Os            | 0.019 | 0.023 | 0.062 | 0.448 | 4.315 |
| Leakage         | 0.712 | 0.712 | 0.713 | 0.722 | 0.822 |
| Total Power     | 0.734 | 0.738 | 0.778 | 1.174 | 5.140 |
There is 89.61%, 98.56%, 99.46% and 99.55% reduction in IOs power when we reduce output load from 5000pF to 500pF, 50F, 5pF and 0.5pF respectively. There is 12.16%, 13.26%, 13.38% and 13.38% reduction in Leakage power when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively. There is 77.15%, 84.86%, 85.64% and 85.71% reduction in total power when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively as shown in Table 2 and Figure 5.

Table 3. I/Os, leakage and total power in watt at frequency 1GHz

| Output Load(pF) | 0.5 | 5  | 50 | 500 | 5000 |
|----------------|-----|----|----|-----|------|
| I/Os           | 0.182 | 0.223 | 0.594 | 4.310 | 41.464 |
| Leakage        | 0.716 | 0.717 | 0.726 | 0.823 | 1.029 |
| Total Power    | 0.922 | 0.965 | 1.345 | 5.157 | 42.518 |

There is 89.60%, 98.56%, 99.46% and 99.56% reduction in IOs power when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively. There is 20.01%, 29.44%, 30.32% and 30.41% reduction in Leakage power when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively. There is 87.87%, 96.83%, 97.73% and 97.83% reduction in Total power when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively as shown in Table 3 and Figure 5.

Table 4. I/Os, leakage and total power in watt at frequency 10GHz

| Output Load(pF) | 0.5 | 5  | 50 | 500 | 5000 |
|----------------|-----|----|----|-----|------|
| I/Os           | 1.780 | 2.184 | 5.824 | 42.228 | 406.260 |
| Leakage        | 0.761 | 0.771 | 0.873 | 1.029 | 1.029 |
| Total Power    | 2.777 | 3.192 | 6.934 | 43.493 | 407.526 |

There is 89.60%, 98.56%, 99.46% and 99.56% reduction in IOs power, when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively. There is 0%, 0%, 0% and 0% reduction in Leakage power, when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively. There is 89.53%, 98.48%, 99.38% and 99.48% reduction in Total power, when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively as shown in Table 4 and Figure 7.

Table 5. I/Os, leakage and power in watt at frequency 100GHz

| Output Load (pF) | 0.5 | 5   | 50  | 500 | 5000 |
|------------------|-----|-----|-----|-----|------|
| I/Os             | 17.958 | 22.041 | 58.785 | 426.231 | 4100.691 |
| Leakage          | 1.029 | 1.029 | 1.029 | 1.029 | 1.029 |
| Total Power      | 21.240 | 25.323 | 62.067 | 429.513 | 4103.973 |

There is 89.60%, 98.56%, 99.46% and 99.56% reduction in IOs power, when we decrease output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively. There is 0%, 15.16%, 25.07% and 26.04% reduction in Leakage power, when we reduce output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively. There is 89.32%, 98.29%, 99.21% and 99.31% reduction in Total power, when we decrease output load from 5000pF to 500pF, 50pF, 5pF and 0.5pF respectively as shown in Table 5 and Figure 8.
4. Conclusion

All the data collected at different output loads can have great impact on the power consumption of the digital clock. The results are plotted successfully and family used is Virtex6. LVCMOS25 is default I/O which is used for calculating the efficiency of the system. The whole idea revolves around making a digital clock that is most efficient that means consumes very less amount of power. For getting better results output load in pF is varied at different frequencies for same I/O standard. The code for the digital clock is written in Verilog and simulated using Xilinx. It is concluded that there is 80-99% reduction in the total power consumed when output load is varied at different frequencies for low voltage complementary metal oxide semiconductor.

5. Future Scope

For implementation of low power design many factors can be varied not only output load and frequency and better results can be obtained. Apart from virtex-6 other families of FPGAs like Virtex-6 lower power, Spartan-6, Spartan-3E etc can be used and results can be noted down.

It is possible that more efficient design than we have tried can be mode from those results. We can also redesign the digital clock by analyzing power at various energy efficient techniques like thermal scaling, clock with different frequencies like 2000MHz, 1800MHz, 1600MHz or any other frequency range that gives us better results. Collecting results by varying the junction temperature can also make the digital clock efficient. These all techniques can be implemented in future to have better results.

6. References

1. Singh PR, Pandey B, Kumar T, Das T. LVCMOS I/O standard based million MHz high performance energy efficient design on FPGA. 2013 International Conference on Communication and Computer Vision (ICCCV); 2013 Dec. p. 1–4.
2. Singla A, Kaur A, Pandey B. LVCMOS based energy efficient solar charge sensor design on FPGA. 2014 IEEE 6th India International Conference on Power Electronics (IICPE); 2014 Dec. p. 1–5.
3. deHek AP, Rodenburg M, van Vliet FE. A cost-effective high-power S-band 6-bit phase shifter with integrated LVCMOS control logic. Proceedings of the 37th European Microwave Conference-EuMC on European Microwave Week EuMW 2007- 2007; 2007 Oct 8-12. Munich, Germany. p. 1261–4.
4. Kumar T, Pandey B, Das T. LVCMOS I/O standard and drive strength based green design on ultra scale FPGA. IEEE International conference on Green Computing, Communication and Conservation of Energy (ICGCE); 2013 Dec. p. 12–4.
5. Van Wanum M, van der Bent G, Rodenburg M, de Hek AP. Generic robust LVCMOS-compatible control logic for GaAs HEMT switches. Louvain-la-Neuve: EuMA; 2006.
6. Goswami K, Pandey B. LVCMOS based thermal aware energy efficient vedic multiplier design on FPGA. IEEE 2014 International Conference on Computational Intelligence and Communication Networks (CICN); 2014.
7. Kannan P, Raghunathan KS, Jayaraman S. Aspects and solutions to designing standard LVCMOS I/O buffers in 90nm process. AFRICON 2007; 2007 Sep. p. 1–7IEEE.