A Comprehensive Study on Tunneling Field Effect Transistor using Non-local Band-to-Band Tunneling Model

Sazzad Hussain, Nafis Mustakim, Showmik Singha and Jibesh K Saha
Department of Electrical and Electronic Engineering, Shahjalal University of Science and Technology, Sylhet-3114, Bangladesh
E-mail: jksaha14@gmail.com

Abstract. In this research work, a n-type silicon tunneling field effect transistor (TFET) has been designed and investigation has been carried out on its performances by altering different device parameters such as gate insulator dielectric constant, channel thickness, gate geometry, and channel length. The performances have been evaluated based on subthreshold swing, threshold voltage and $I_{on}/I_{off}$ ratio of the devices. The goal is to find a device which would simultaneously have a low subthreshold swing (SS), low threshold voltage, and a high $I_{on}/I_{off}$ ratio. It has been observed that having a double gate, short channel length, high-$\kappa$ dielectric, and low channel thickness leads us towards a compact design and the device exhibits very promising values of the aforementioned performance criteria. The most attractive proposition about a TFET is its ability to have a subthreshold swing lower than 60 mV/dec which is the theoretical limit of a MOSFET. In this study, an optimized device is obtained which has a subthreshold swing (point) of around 26 mV/dec and an $I_{on}/I_{off}$ ratio in the order of $10^{13}$. In addition, an inverter has been designed using a n-type TFET and a resistor to show the potential of TFETs to be used in logic circuits.

Keywords: SOI-TFET, DG-TFET, Non-local BTBT, Subthreshold swing, $I_{on}/I_{off}$, Inverter.

1. Introduction
As the scaling down of conventional CMOS technology continues leading the present-day transistors to approach its fundamental limit, the requisite for a new device is significantly growing. A tunneling Field-effect transistor (TFET) is one of the most prominent candidates of replacing current CMOS technology due its low subthreshold swing and suitability for ultra low power device [1–5]. Moreover, the fundamental limit of subthreshold swing for the MOSFET is 60 mV/dec due to Boltzmann distribution of carrier [2]. But the subthreshold swing of TFET is not limited to 60 mV/dec [6]. As Subthreshold swing greatly influences the leakage power, TFET exhibits much lower leakage power compared to MOSFET [7]. On top of that, similar $I_{on}/I_{off}$ ratio like MOSFET can be obtained in TFET at lower $V_{DD}$ for its lower subthreshold swing [5]. TFET has a diode like built-in barrier. So, they can also achieve very low OFF current as compared to a MOSFET [8].

In recent years, extensive research is going on TFET to improve it’s ON current and $I_{on}/I_{off}$ ratio [9]. Chen et al. has proposed a highly scalable vertical silicon nanowire TFET of gate length $\sim$ 200 nm, has a subthreshold swing of 70 mV/dec and $I_{on}/I_{off} \sim 10^{7}$ [10]. Choi et
al. has reported a silicon TFET with subthreshold swing of 52.8 mV/dec [6]. Furthermore, Lattanzio et al. has proposed a novel TFET structure named as electron-hole bilayer TFET with a subthreshold swing of 12 mV/dec and \(I_{on}/I_{off} \sim 10^8\) [11]. Boucart et al. in their paper showed that \(I_{on}/I_{off}\) of a double gate TFET (DG-TFET) can be of order \(10^{11}\).

In this study, some optimization approaches have been shown for silicon TFET design on the basis of varying different structural parameters such as high-\(\kappa\) dielectric, the addition of an extra gate, low channel thickness, etc to enhance the performance of a TFET. Following these optimization schemes, an optimized double gate TFET (DG-TFET) has been proposed in which subthreshold swing (point) is 26 mV/dec and \(I_{on}/I_{off}\) ratio is in order of \(10^{13}\). In addition, it has also been shown the transient analysis of an inverter using n-TFET.

### 2. Device Structure

In the designed TFET structure, source is highly doped p\(^{+}\)(8×10\(^{19}\)cm\(^{-3}\)) region. Source doping is kept high because tunneling takes place in the source-channel junction. Intrinsic channel is lightly doped n\(^{-}\)(1×10\(^{15}\)cm\(^{-3}\)) region and, drain is doped with n\(^{+}\)(5×10\(^{18}\)cm\(^{-3}\)). The higher levels of doping in the drain and source region compared with that of a conventional MOSFET is necessary to produce degenerate semiconductors essential for tunneling. Uniform doping is maintained in all regions of source, drain, and channel. The workfunction of the gate is set to 4.4 eV. The schematic of a typical double gate TFET that has been designed is shown in Figure 1.

In the ON state, it has been observed that there is high non local band-to-band tunneling (BTBT) rate in the junction region between the source and the channel. On the other hand, tunneling rate is negligible over other regions of the device which is evident from the BTBT rate of the device as shown in Figure 2.

**Figure 1.** Schematic of the Double gate TFET.

**Figure 2.** Band to band tunneling rate over the length of the device.

### 3. Methodology

Some of the models incorporated in the study are as follows- Shockley-Read-Hall recombination (srh), Concentration Dependant Mobility (conmob), Band Gap Narrowing (bgn), Fermi-Dirac Statistics and Fermi statistics was used to calculate intrinsic carrier concentrations required for
evaluation of SRH recombination. Most important model in this study is the non-local band to band tunneling model which accurately models the physics of the device.

The non-local band to band tunneling model used in the simulation provides a more precise picture compared to the local method. In the local band to band tunneling model, generation and recombination rates and consequently, the tunneling current are calculated based upon the value of the electric field at each mesh point. However, tunneling current depends on the tunneling barrier width and the presence of states on either side of the tunneling barrier. As tunneling is itself a non-local process depending on the aforementioned factors, it is more reliable to use a non-local method. To use the non-local band to band tunneling model in the simulation, it is essential to provide the tunneling direction and set up another mesh to create tunneling slices where tunneling can take place. During the course of the research work, the simulation has been carefully set up to take into account these various factors in order to obtain accurate results.

To implement inverter, a SPICE-like code describing the n-type TFET inverter (n-TFET with resistive load) has been written along with the TFET device specifications. Moreover, input and output relationships have been monitored over many periods of the input waveform.

For all the simulations, drain voltage is fixed to 1 V (except when we sweep the drain voltage to obtain output characteristics). A constant current method has been used to calculate threshold voltage in this work. The constant current is chosen to be $10^{-7}$ A/µm based on the data. Subthreshold swing (point) and $I_{on}/I_{off}$ have been calculated using the well-known definitions.

4. Results and discussion

4.1. Performance Analysis of SOI-TFET

The study was started with a typical SOI-TFET with SiO$_2$ as the gate insulator. The channel length and channel thickness are set to 90 nm and 10 nm respectively. BOX thickness of the device is 50 nm. The $I_D$ vs $V_{GS}$ graph of the SOI-TFET is shown in Figure 3. Subthreshold swing obtained for this structure is only 55.6 mV/dec and $I_{on}/I_{off}$ is $1.80 \times 10^{11}$. The OFF current in this structure is in picoampere range and the ON current is near microampere range.

![Figure 3. $I_D$ vs $V_{GS}$ of SOI-TFET.](image)

4.2. Effects of High-κ Gate Dielectrics

Improved ON current and decreased subthreshold swing can be achieved if the gate dielectric material is chosen carefully [12]. The same trend has been observed in this simulation result using three different dielectric materials such as SiO$_2$ ($κ = 3.9$), Si$_3$N$_4$ ($κ = 7.5$) and, HfO$_2$ ($κ$
In consistent with the work of Ning et al., simulation result of this work also shows that $I_{on}$ and subthreshold swing improves when high-$\kappa$ gate dielectric material is used as illustrated in Figure 4 [13]. Even though having the same gate thickness, high-$\kappa$ dielectrics have smaller EOT (Equivalent Oxide Thickness) compared to low-$\kappa$ dielectric materials. As a result, gate has more control over the channel when high-$\kappa$ dielectric material is used [12; 13]. As shown in Figure 4, ON current improves as the gate dielectric strength, $\kappa$ increases. Table 1 shows the effect of $\kappa$ on device performance.

| $\kappa$ | Subthreshold swing (mV/dec) | Threshold voltage (V) |
|----------|-----------------------------|-----------------------|
| 3.9      | 55.77                       | 1.68                  |
| 7.5      | 43.55                       | 1.67                  |
| 21       | 33.74                       | 1                     |

4.3. Effects of Channel Thickness
TFET is sensitive to silicon body thickness ($t_{si}$) because scaling down of device always improves its performance[12]. In this study, subthreshold swing, threshold voltage, and $I_{on}/I_{off}$ have improved with thinner channel thickness as shown in Figure 5.

As shown in Table 2, decrease in $t_{si}$ improves both Subthreshold swing and $I_{on}/I_{off}$. $SiO_2$ has been used as gate oxide to carry these simulations. Ranjan et al. have also found results with similar trend in their work [14].
Table 2. Effect of channel thickness on subthreshold swing and threshold voltage.

| $t_{si}$ (nm) | Subthreshold swing (mV/dec) | Threshold voltage (V) |
|---------------|-----------------------------|-----------------------|
| 50            | 64.8                        | 1.92                  |
| 30            | 64.2                        | 1.90                  |
| 10            | 55.77                       | 1.68                  |

Table 3. Comparison of DG-TFET and single gate SOI-TFET.

| Performance criterion | DG-TFET | SOI-TFET |
|-----------------------|---------|----------|
| Subthreshold swing (mV/dec) | 41.50   | 55.77    |
| Threshold voltage (V)    | 1.16    | 1.68     |
| $I_{on}/I_{off}$          | $1.7 \times 10^{12}$ | $8.6 \times 10^{10}$ |

4.4. Comparison of Double gate TFET and Single Gate SOI-TFET

When an extra gate is added to the TFET, it’s ON current enhances as shown in Figure 6, while the OFF current still remains in the fA range. Simulation of a single gate SOI-TFET and DG-TFET with equal structural parameters as shown in Figure 6, shows a remarkable difference in the ON current. DG-TFET takes advantage of an extra gate that eventually increases the ON current. The simulation result is coherent with the result found by Verhulst et al. [15]. Double gate also improves subthreshold swing, threshold voltage and, $I_{on}/I_{off}$ as illustrated in Table 3.

4.5. Effects of Length Scaling on TFET with High-$\kappa$ Dielectric

The length scaling of TFET is much more different than MOSFET. Constant field scaling is not applicable for scaling of silicon TFET [16]. No significant effect of length scaling could be reported while keeping other parameters as optimized as possible. Similar trend has been observed by Boucart et al. and Bal et al. in their DG-TFET structure [17] and [18] respectively. This is a very significant difference of TFETs and MOSFETs. TFET is much more intolerable to length scaling than MOSFET. Subthreshold swing, $I_{on}/I_{off}$, the threshold voltage is not affected much due to length scaling. Figure 7 shows the effect of channel length on DG-TFET.

4.6. Optimized TFET

When all the optimization approaches are applied together subthreshold swing obtained from the device is only 26.02 mV/dec, $I_{on}/I_{off}$ ratio is in the order of $10^{15}$ and threshold voltage is reduced to 0.713 V. In the optimized TFET channel length is 30 nm and channel thickness ($t_{Si}$) is 10 nm. Moreover, oxide thickness ($t_{OX}$) and dielectric strength ($\kappa$) is 3 nm and 21 respectively.

Till now only the dc transfer characteristics of TFET have been analyzed. But for circuit-level implementation, ac switching performance plays a vital role. Mookerjea et al. have shown that enhance gate to drain Miller capacitance ($C_{gd}$) effect limits the performance of TFET by leading to overshoot or undershoot of voltage [19]. In the small-signal analysis simulation, as shown in 8, the miller capacitance effect has been observed. $C_{gg}$ has been obtained by adding $C_{gs}$ and $C_{gb}$ and the result is coherent with [19].
Figure 6. Comparison of $I_D$ vs $V_{GS}$ of SOI-TFET and DG-TFET. $I_D$ improves almost two times for double gate structure.

Figure 7. Change of $I_D$ vs $V_{GS}$ for different channel length. $I_D$ is not much affected by channel length scaling.

4.7. Transient analysis of n-TFET Inverter
Lastly, an inverter logic has been implemented using TFET. From Figure 9, it can be seen that the input signal, $V[1]$ is inverted but there are voltage overshoots on both the positive and negative side. The overshoots can be explained with the aid of the Miller effect. Because of the Miller effect, the transient signal from the drain node (output) is fed back into the gate node (input). This evident from the C-V curve in Figure 8 for a TFET where the $C_{gd}$ is greater than $C_{gs}$. The performance of inverter is degraded because of these overshoots which result in high dynamic power loss and long delay time.

Figure 8. Small-signal analysis of the optimized TFET.

Figure 9. Transient response of n-TFET inverter.
5. Conclusion
The research work has focused on creating an optimized Tunneling Field Effect Transistor (TFET) which would have superior characteristics to existing MOSFETs. It has been found that having a high-$\kappa$ dielectric, lower channel thickness of 10 nm, a short channel of 30 nm length, and double gate along with abrupt doping profile gives rise to a device which has an excellent subthreshold swing of around only 26 mV/dec, an $I_{on}/I_{off}$ ratio of $4.33 \times 10^{13}$ and a threshold voltage of 0.71 V. The significant improvements in $I_{on}/I_{off}$ and subthreshold swing compared with the present-day MOSFET devices make TFET an attractive alternative to MOSFET. The inverter simulation shows that improvements need to be made to mitigate the voltage overshoot problems. Since TFETs can be fabricated with the existing technology available for MOSFETs, it is a viable option to replace MOSFET in the near future.

References
[1] Reddick W M and Amaratunga G A 1995 Applied Physics Letters 67 494–496
[2] Seabaugh A C and Zhang Q 2010 Proceedings of the IEEE 98 2095–2110
[3] Hu C, Patel P, Bowonder A, Jeon K, Kim S H, Loh W Y, Kang C Y, Oh J, Majhi P, Javey A et al. 2010 Prospect of tunneling green transistor for 0.1 v cmos 2010 International Electron Devices Meeting (IEEE) pp 16–1
[4] Strangio S, Palestri P, Esseni D, Selmi L, Crupi F, Richter S, Zhao Q T and Mantl S 2015 IEEE Journal of the Electron Devices Society 3 223–232
[5] Ionescu A M and Riel H 2011 nature 479 329
[6] Choi W Y, Park B G, Lee J D and Liu T J K 2007 IEEE Electron Device Letters 28 743–745
[7] Khatami Y and Banerjee K 2009 IEEE Transactions on Electron Devices 56 2752–2761
[8] Trivedi A R, Amir M F and Mukhopadhyay S 2014 Ultra-low power electronics with si/ge tunnel fet 2014 Design, Automation & Test in Europe Conference & Exhibition (DATE) (IEEE) pp 1–6
[9] Baravelli E, Gnani E, Guindi A, Reggiani S and Baccarani G 2014 IEEE Transactions on Electron Devices 61 473–478
[10] Chen Z, Yu H, Singh N, Shen N, Sayanthan R, Lo G and Kwong D L 2009 IEEE Electron Device Letters 30 754–756
[11] Lattanzio L, De Michielis L and Ionescu A M 2011 Electron-hole bilayer tunnel fet for steep subthreshold swing and improved on current 2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC) (IEEE) pp 259–262
[12] Boucart K and Ionescu A M 2007 IEEE transactions on electron devices 54 1725–1733
[13] Ning C, Renrong L, Jing W, Wei Z and Jun X 2012 Journal of Semiconductors 33 084004
[14] Ranjan R, Pradhan K, Sahu P et al. 2016 Advances in Natural Sciences: Nanoscience and Nanotechnology 7 035009
[15] Verhulst A S, Sorée B, Leonelli D, Vandenbergh W G and Groeseneken G 2010 Journal of Applied Physics 107 024518
[16] Saha P, Kumari T and Sarkar S K 2019 IETE Technical Review 36 17–26
[17] Boucart K and Ionescu A M 2007 Solid-State Electronics 51 1500–1507
[18] Bal P, Akram M, Mondal P and Ghosh B 2013 Journal of Computational Electronics 12 782–789
[19] Mookerjea S, Krishnan R, Datta S and Narayanan V 2009 IEEE Electron Device Letters 30 1102–1104