Memristor-based Deep Convolution Neural Network: A Case Study

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Abstract—In this paper, we firstly introduce a method to efficiently implement large-scale high-dimensional convolution with realistic memristor-based circuit components. An experiment verified simulator is adapted for accurate prediction of analog crossbar behavior. An improved conversion algorithm is developed to convert convolution kernels to memristor-based circuits, which minimizes the error with consideration of the data and kernel patterns in CNNs. With circuit simulation for all convolution layers in ResNet-20, we found that 8-bit ADC/DAC is necessary to preserve software level classification accuracy.

Keywords—Memrisor, Crossbar, CNN

I. Introduction

Convolutional Neural Networks (CNN) have led to many performance breakthroughs in image classification, video object tracking, and audio processing applications\cite{1}. Since AlexNet won the ILSVRC 2012 and is more than 10\% lower than other contemporary competitors on top-5 error rate\cite{2}, CNN evolved into many different models, such as GoogLeNet\cite{3}, VGG\cite{4}, ResNet\cite{5}. Using Graphics Processing Unit (GPU) to accelerate convolution computations plays an important role in CNN’s success, since convolution is the most time-consuming part in CNN, and the throughput of convolution is prior than accuracy\cite{6}. However, for large scale Convolutional Neural Networks (CNN), modern computing hardware often encounter on-chip memory bottleneck when dealing with high volume convolution calculations\cite{7, 8}.

Recently, many researchers show interest on emerging memristor crossbar for its computing-in-memory feature\cite{9, 10, 11, 12, 13, 14}. A memristor crossbar can carry out large-scale analog vector matrix multiplication in one step by collecting analog output with input signal flowing through the array, where weights are stored non-volatilely at cross-point memristor devices. Since weight storage and weighted summation both happen at the same location of memristors, it enables ultra-high computing efficiency as well as low communication requirement. Overall, memristor crossbar-based implementation may overcome von-Neumann architecture’s shortage and are suitable for deep learning inference functions.

However, integrating analog memristor crossbars with digital circuits is not trivial. One of the key issues is that a rigorous circuit simulation is still missing for memristor-based CNN implementations, especially on the modeling of analog memristor crossbar behavior. As SPICE is too slow on simulating large-scale memristor crossbar arrays, specific tools have been developed to investigate memristor-based neural network (NN) implementations\cite{15, 16}. Although they provide accurate estimation for speed, area and power, the prediction of functionality is questionable due to over-simplified memristor crossbar models, which is also lack of experiment verification at large scale. It leads to a serious question: if we implement state-of-the-art CNNs with memristors, will it really work? This question can only be addressed with an analog circuit simulation for all the memristor crossbars in CNNs, since it is the most immature part in the whole system.

In this paper, we investigate memristor-based large-scale CNN implementation with experiment verified memristor crossbar simulators. Our contributions are listed as below:

- First, we provided an efficient mapping method to map high dimension kernels to 2-D memristor crossbars using realistic circuit components.
- Second, we developed an improved conversion algorithm to convert kernel to crossbar conductance with consideration of non-ideal hardware as well as data/kernel patterns.
- Third, we addressed the aforementioned question with ResNet-20 on cifar-10. A careful simulation is done at all convolution layers to capture the error propagation in CNN. Our result shows that 8-bit ADC/DAC quantization is necessary to preserve the classification accuracy.

II. Preliminary

A. Deep Residual Neural Network

Deep residual neural network (ResNet) was firstly introduced in ILSVRC 2015\cite{5}. So far, ResNet is the state-of-the-art CNN on image classification problems. An ensemble of residual nets up to 152 layers achieves 3.57\% error on the ImageNet test set and won the 1st place on the ILSVRC 2015 classification competition. To evaluate how state-of-the-art CNNs perform on memristor crossbar arrays, ResNet is an ideal case study.

Fig.1 shows the basic block diagram of ResNet. It combines multiple convolution, batch normalization, and rectified linear units (ReLU) together as its basic building block. Different from other CNNs, ResNet uses a shortcut to add input data to the output result of a block. If two data inputs have different dimensions at the summation stage, a 1 × 1 convolution layer will be introduced in shortcut to match the dimension. The summation result is sent to ReLU and pass to the next Block. At the end of ResNet, pooling layer, one or more Fully Connected (FC) layers, and a softmax layer are used in sequence to generate final classification result.
2. 1T1M crossbar for VMM

Fig. 2(a) shows the general structure of a one-transistor-one-memristor (1T1M) crossbar for vector matrix multiplication (VMM). In this structure, memristor crossbar is the core component as it enables analog current weighted summation, which leads to ultra efficient VMM operation. A \( m \times n \) memristor crossbar is made by \( m \) row and \( n \) column metal wires where memristors formed at intersecting points. Each memristor can be tuned to arbitrary conductance within its programmable range. To enable precise, non-disturbing tuning in large crossbar arrays, 1T1M cell (Fig. 2(b)) is necessary to program the entire array with arbitrary conductance matrix \( G \). By applying voltage inputs \( V \) at the rows simultaneously and read current outputs \( I \) from the columns, analog weighted summation is achieved through Kirchhoff’s Current Law and Ohm’s Law. In an ideal crossbar, input-output relationship can be represented as below:

\[
I = VG
\]

By mapping input vector \( X \) to input voltage \( V \), matrix \( A \) to conductance \( G \), and output current \( I \) back to output result \( Y \), a memristor crossbar can be regarded as an analog VMM module to realize \( Y = XA \) in one step. Note that \( I = VG \) is only valid for ideal crossbar while wire resistance cannot be ignored and device conductance is independent of voltage/current. In real crossbars, the input-output relationship is far more complex and needs analog circuit simulation.

Fig. 2(c) illustrates a ramping ADC design[17], it uses a shared ramping signal generator and counter to support multiple channels simultaneously. The ramping signal generator produces increasing/decreasing analog voltage signal to all comparators, and its analog value is synchronized with the digital representation in the counter. Comparators compare the crossbar output to the ramping signal. Once a flip is detected, comparator captures the current value in the counter, which is the corresponding digital representation of crossbar output. This concept can be applied to DAC design as well. Overall, The ramping ADC/DAC design can achieve lower area and power for multi-channel applications, and it is a suitable digital interface for crossbar-based accelerators.

C. Experiment-Verified Crossbar Simulator and The Conversion Algorithm

So far, simulation tools like MNSIM and NeuroSim provide excellent architecture-level analysis. However, their memristor crossbar models are over simplified. In MNSIM[15], an estimated behavior model is used instead of solving node equations; In NeuroSim[16], the impact of wire resistance is simplified by adding wire resistance to cross-point devices. All of these over-simplifications result in unignorable error between predicted output to real output of crossbars. And this error become even more severe in large scale implementations. In short, coarse modeling of crossbar may be acceptable on power/area/speed estimations, but is questionable on functionality evaluations, such as computing accuracy at layers, or classification accuracy of NN implementations. After all, to evaluate NN’s functionality on memristor-based implementations, an accurate crossbar simulator is necessary.

An accurate crossbar simulator should use realistic device models, solve node equations with consideration of wire resistance and other circuit parameters, then finally verified with experiment result at large scales. Here We adapt the experiment-verified memristor crossbar simulator from [11]. Fig. 3 illustrates the simulation result of the memristor crossbar simulator, which is verified with experiment up to \( 128 \times 64 \).

Besides the simulator, the conversion algorithm, as a mapping method is employed to improve VMM computing accuracy with consideration of wire resistance and device nonlinearity[18]. The conversion algorithm uses a conversion signal \( V_{conv} \) to find a new conductance mapping \( G' \), so that

\[
VG \approx \text{CrossbarSim}(V, G')
\]

where CrossbarSim() is the realistic crossbar model. Although the original conversion algorithm provides 7~8 bit-accuracy result for general VMM, it does not consider im-
Fig. 3: 1T1M simulation and experiment result [11]. Wire segment resistance is calibrated to 1Ω, transistor and memristor models are calibrated with in-array device test.

impact of data/weight patterns in specific applications, which may affect its performance significantly.

III. Methodology

In this work, we take ResNet-20 as our case study for memristor-based CNN implementation. We first provide a dense mapping method to map high dimension kernels onto 2-D memristor crossbar arrays efficiently. By doing a near full circuit simulation of memristor-based implementation for ResNet-20, we explain how to optimize the conversion signal for each layer based on its corresponding convolution kernel and data pattern. Moreover, we introduce an additional calibration step to further improve the performance and robustness of the circuit. Our memristor-based CNN implementation can give precise convolution result for each layer, and its precision is independent of data sparsity and kernel types.

A. Dense mapping for crossbar-based convolution

In ResNet, each convolution layer has a 4-D kernel, as illustrated in Table I. For example, the 3*3*3*16 kernel of 'Conv0' means it has 16 sets of 3*3*3 3-D kernels, and each 3-D kernels contains 3 2-D kernels for the 3 channels (RGB) of color images. To perform convolution on memristor crossbar, we need convert high dimensional convolution into 2-D VMM. It is well known that 2D convolution can be implemented using matrix multiplication by converting kernel to a Toeplitz matrix. Toeplitz matrices are sparse matrices which contains many zeros, so we named this method as sparse mapping.

However, sparse mapping has three major issues: First, memristor crossbar is by nature a dense array structure with positive values, not efficient for sparse matrix implementation. Mapping a sparse matrix to crossbar means that the memristors assigned with zero entries would do nothing but adding error to the final result due to leakage current, as well as waste circuit area. Second, sparse mapping requires a huge crossbar array, which is not always feasible, and vulnerable to noise and defects. third, sparse mapping requires a large peripheral circuit to support the huge array. Since peripheral circuit dominates the total power/area, the hardware implementation of sparse mapping would be too costly to afford.

Fig. 4 illustrates the concept of dense mapping. In contrast to sparse mapping, we developed a new method, named as dense mapping, targeting on using small and dense representations to implement convolutions on memristor crossbars efficiently. Each 2-D kernel is unrolled to a vector and mapped to the column of crossbar so that one crossbar can implement multiple 2-D kernels as long as it has enough columns. For input signal, only data within the convolution window is converted to the row inputs of crossbar arrays. For data with multiple channels, 2-D kernels for different channels are stacked into the same column, as input from different channels can be supplied to different rows and weighted summed together. An input shift register stores the input data within convolution window at the current iteration, and updates its storage as window moves through the entire data space. The convolution result for data within the convolution window are collected at the column outputs of crossbar. In this way, a single memristor-based convolution kernel needs \( j \times k \) iterations for input data with size \((j, k, p)\), where \( j, k, p \) means data height, width, and channel, respectively. The circuit needs \( j \times k \) iterations to process the input data.
TABLE I: Dense mapping of ResNet-20 convolution layers for 32 × 32 color image classification from cifar-10 dataset

| Layer name | Kernel size | Crossbar Size | Iteration per. class. |
|------------|-------------|---------------|-----------------------|
| Conv0      | 3*3*3*16   | 27*16         | 1024                  |
| Conv1-2    | 3*3*16*16  | 144*16        | 1024                  |
| Sum1       | 1*1*16*16  | 16*16         | 1024                  |
| Conv3-6    | 3*3*16*16  | 144*16        | 1024                  |
| Sum2       | 1*1*16*32  | 16*32         | 256                   |
| Conv7      | 3*3*32*32  | 144*32        | 256                   |
| Conv8-12   | 3*3*32*32  | 288*32        | 256                   |
| Sum3       | 1*1*32*64  | 32*64         | 64                    |
| Conv13     | 3*3*32*64  | 288*64        | 64                    |
| Conv14-18  | 3*3*64*64  | 576*64        | 64                    |
| FC         | 1*1*64*10  | 64*10         | 1                     |

TABLE II: Explanations for functions in algorithm 1

| Function      | Explanation                                                                 |
|---------------|-----------------------------------------------------------------------------|
| CrossbarSim   | Experiment verified crossbar simulator from [11]                             |
| Conversion    | Solve \( v_{conv} \cdot G = \text{CrossbarSim}(V_{conv}, G') \) to get \( G' \). |
| GetCaliPara   | Get 1st order poly fitting result \( P \) by fitting crossbar output to ideal output of calibration samples. |
| Calibration   | Use \( P \) and \( InputVector[i] \) to map \( I_{out}[i] \) to \( Output[i] \). Here \( InputVector[i] \) is needed, because in VMM \( Y = XA \), if \( A \) contains negative values, \( Y \) can be calculated by \( Y = X(A+c) - c*\text{sum}(X) \), while \( c \) is a large enough scalar to shift \( A \) to all positive. |

Algorithm 1 Crossbar-based convolution with improved conversion algorithm

1: Initialization: setup crossbar parameters (wire resistance, memristor conductance range, etc...)
2: Get a batch of input data
3: If kernel \( K \) is mapped and converted, jump to computing
4: Dense mapping kernel \( K \) to conductance matrix \( G \)
5: Optimize conversion signal
6: \( InputVectors \leftarrow \) Partition input data
7: \( CaliSample \leftarrow \) Random pick from \( InputVectors \)
8: \( G' \leftarrow \) Conversion(\( G' \), \( CaliSample \))
9: \( P \leftarrow \) GetCaliPara(\( G' \), \( CaliSample \))
10: Begin computing
11: \textbf{while} \( \sim \) end of \( InputVectors \) \textbf{do}
12: \( V_{in}[i] \leftarrow InputVector[i] \)
13: \( I_{out}[i] = \text{CrossbarSim}(G', V_{in}[i]) \)
14: \( Output[i] = \text{Calibration}(I_{out}[i], InputVector[i], P) \)
15: \( i \leftarrow i + 1 \)
16: Convolution result \( \leftarrow \) reshape(\( Output \))
17: End computing

Fig. 5: Input data sparsity at each convolution layer of ResNet-20

B. Improved conversion algorithm

Algorithm I summarizes the flow of crossbar-based convolution with the improved conversion algorithm. Table II explains the important functions in the algorithm. After initialization, if the kernel is already mapped and converted onto crossbars, it will directly jump to the computing step to simulate crossbar-based convolution. So to implement ResNet-20 with multiple convolution layers, we only need to do mapping/conversion once for inferencing.

B.1 Data and kernel pattern in ResNet

Data in ResNet has high sparsity due to ReLU. Fig. 5 shows the data sparsity at each convolution layer of ResNet-20. The impact of data sparsity should be considered when choosing conversion signal as well as gathering calibration samples.

Similarly, we found that kernels in CNN have different distributions. In Fig. 6 we list three typical kernel types regarding to their weight value distributions. Usually there are three typical kernel types: Kernel type 1 refers to a weight distribution close to Gaussian, usually it happens when training algorithms put no limitation on weight values, such as ResNet. Kernel type 2 refers to training algorithm that preventing weight values goes near zero [19]. Kernel type 3 refers to Binary Neural Networks where weights can only be -1, 0 (sparse), or 1 [20]. It worth investigating how different kernel types in CNN impact the quality of crossbar-based convolution.

B.2 Optimize conversion signal

To better quantize the computing accuracy, we define relative error as below:

\[
\text{Relative Error} = \frac{\text{Absolute Error}}{\text{Output Range}}
\]
While Absolute Error is the absolute error of crossbar output, and Output Range is the ideal convolution output range for each kernel. Relative error can be converted to output bit accuracy as below:

\[
\text{Bit Accuracy} = \log_2\left(\frac{1}{\text{Relative Error} + 1}\right)
\]

The original conversion algorithm takes the maximum input vector as its conversion signal, which works well with dense matrix and dense input signals. However in CNN, we need to consider the sparsity of data to optimize the conversion signal. By testing various different conversion signals across different kernels, we notice that the amplitude of conversion signal is critical, while the sparsity of conversion signal is not as important. Fig.7 shows the relative error distribution with different conversion signal amplitudes in crossbar with size 144×16. We found that a conversion signal with too large amplitude (all 1) will cause over compensation in the signal loss due to wire resistance, and a too small conversion signal (all 0.001) do have enough compensation and both of them result in large error in output. So for crossbar size 144×16, all 0.1 signal appears to be the best conversion signal, and other conversion signal close to it generate similar error distribution.

B.3 Calibration

In addition to original conversion algorithm, we add a calibration stage to further improve the result. It randomly picks 10 samples from the input data set, and runs a 1st order polynomial fit to fit crossbar output to ideal output. The generated fitting vector \( P \) is fixed per crossbar, and can be easily embedded in ADC/DAC configurations. Fig.8 shows the relative error with different calibration signals, and here using shuffled input can achieve the best result.

IV. Result

A. Simulation setup

In our work, convolution and fully-connected (FC) layers are implemented by analog memristor crossbars with digital interface. Other functions, such as pooling, ReLU, batch normalization, etc., are processed by digital circuits. The CNN is offline-trained, then its kernels are converted to the conductance of memristors for inference. Our crossbar simulator is configured as below: Lowest memristor resistance \( R_{on} = 15k\Omega \), Highest memristor resistance \( R_{off} = 300k\Omega \), wire resistance per segment is set to 1Ω, sensing voltage = 0.2V. Input/Output resistance of crossbar are set to 1Ω. Input voltage range is [0, 0.2V]. The crossbar simulation tool is adapted from [11].

B. Individual convolution layer simulation

We first run circuit simulation at individual convolution layers to understand the impact of input data sparsity, kernel type and size on convolution accuracy. Fig.9 illustrate the impact of input data sparsity. There are three observations: first, our method provides \( \sim 50\% \) better overall accuracy than the original conversion algorithm. Second, our method gives lower relative error when ideal value is small. Third, our method minimizes the impact of data sparsity comparing to original conversion algorithm. Fig.10 summarizes the mean/worst relative error across three types of kernels with different input sparsity and crossbar sizes. It shows that our method is independent of kernel type and data sparsity.
C. End-to-end simulation for ResNet

It is more important to predict how errors propagate and accumulate in deep neural networks, and evaluate its impact on the final classification result. Fig. 11 shows the error propagation at each convolution layer in ResNet-20. Fig. 12 shows the classification result. Different ADC/DAC quantization settings are applied and we can see that 8-bit quantization is necessary to prevent error accumulation. Without quantization, the error will propagate from beginning to the end and affect the classification result, which is also not practical for large-scale implementation. Due to long simulation time (15mins/image), we used a subset of cifar-10 containing 150 testing images. It appears that 8-bit quantization is a good balance between error suppression and information preservation, as it achieves even slightly better classification result than software. 6-bit or 4-bit quantization cause error accumulate through all layers and lead to a significant drop in classification accuracy. With 6-bit, error rate increased by 73% from 10% to 17.3%.

V. Conclusions

In this work, We take ResNet as case study to investigate how modern CNN performs on memristor-based implementations. Our methods includes an dense mapping and an improved conversion algorithm, which can achieve 0.25% mean relative error (≈ 8.6 bits) or 1.2% worst relative error (≈ 6.4 bits) for crossbar size 576 × 64. We performed a rigorous analog simulation for every convolution layers to give an accurate prediction of error propagation in ResNet. We find that 8-bit ADC/DAC is necessary to prevent classification degradation. Our method can be applied to general CNNs due to its independence of input data sparsity and kernel types.

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