Yield and leakage current of organic thin-film transistor logic gates toward reliable and low-power operation of large-scale logic circuits for IoT nodes

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This paper reports on a strategy for yield improvement and static leakage current reduction by a standard cell design for large-scale organic thin-film transistor (OTFT) circuits. Print-on flexible devices are suitable for IoT nodes, and digital OTFT circuits comprise the peripheral circuits of such devices. Sufficiently high yields and low static power consumptions are essential for battery operations of IoT nodes having functional digital circuits. Our design method addresses the weak n-type OTFT on-current results in improved logic gate yields without any cell area increase. We improved the yield of the inverter, NAND, and NOR gates using a standard cell design, and achieved a 100% yield for the inverter and NOR gates and 88% yield for the NAND gates. Signal propagations with the rail-to-rail operation were measured on test chips. Leakage currents of 585 pA and 2.94 nA were achieved for the inverter and NOR gates, respectively.© 2022 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

1. Introduction

Organic devices are regarded as prospective new devices in the emerging IoT era because of desirable features such as low weight, flexibility, printability, reduced complexity, and large area implementation. Implementation of large-scale logic circuits facilitates digital signal processing and communication. Further, peripheral circuits, in addition to analog amplifiers and sensor elements, can be implemented as flexible and printable circuits. Given the aspects of reduced complexity and low weight, the integrated logic circuit with organic devices can accelerate the development of wearable applications. The implementation of organic thin-film transistor (OTFT) circuits and its applications have recently been reported, e.g. transistor chips for radio frequency identification tags, static random-access memories (SRAMs), CMOS analog circuits such as amplifiers, analog-to-digital (A/D), and digital-to-analog (D/A) converters, CMOS digital circuits such as microprocessors, artificial skin using thermal and pressure sensors, braille displays using SRAM, and wearable electrochemical sensor. Nevertheless, more extended functional large-scale digital circuits with low-voltage and low-power operation are expected to facilitate sensor applications for IoT nodes. The yield and low static power consumption of OTFT logic gates is a critical issue associated with large-scale digital circuits. The contribution of this paper is the achievement of a high yield and minimization of static leakage current of the OTFT logic gates by improving the OTFT standard cell design.

The carrier mobility in organic semiconductors is lower than that of silicon. Extensive studies have been performed on the improvement of carrier mobility in organic semiconductors. In recent studies, a hole mobility of 30 cm² V⁻¹ s⁻¹ and an electron mobility of 3 cm² V⁻¹ s⁻¹ were achieved.

Recent research on OTFT logic circuits is focused on lowering the operation voltages for low power consumption. A prior study on OTFT logic gate reported 5 V inverter operation and 15 V NAND, NOR, OR, and XOR gates operation with a complementary structure. Further, 501-stage ring oscillator operation has also been reported. However, the ring oscillator in this study results in a 1.8 V output “1” level at 6 V supply voltage (Vdd), and the output “1” level was lower than half of Vdd. A programmable logic circuit with 1260 p-type organic transistors, which operate at over 10 V, has also been reported. Microprocessors operating at 12 V have also been realized. For a single inverter gate, pA-class leakage was achieved with state-of-the-art materials and fabrication technologies. Generally, the intermediate gate input voltage causes significant through-currents, resulting in a severe static leakage current. Previously, evaluated the feasibility of security components using the OTFT logic circuits at Vdd = 3.3 V with the complementary gate structure. These security components called buskeeper physically unclonable functions generate random IDs unique to each chip, utilizing the power-on initial value of the buskeeper cell. However, sufficient rail-to-rail output voltage swing cannot be obtained. The rail-to-rail output voltage swing is essential for the reliable operation of logic paths, because attenuation of output voltage swing results in signal propagation failure. In addition, for sensor node applications that require long-term battery operations, a static leakage current caused by the intermediate gate voltage can be a critical design issue. In previous studies on the pA-class leakage current, rail-to-rail operation with a single gate was observed. For large-scale low-power OTFT digital circuits, obtaining a reliable yield and realizing rail-to-rail operations of logic gates are essential. Based on our preliminary study on a rail-to-rail operation of the inverter gate and µA class static leakage current, we address the high yield, the rail-to-rail operation, and nA class leakage current of inverter, NAND, and NOR circuits for reliable operation and low static power consumption of large-scale logic circuits in this study.

The impact of standard cell designs with an organic transistor on the yield and the low static leakage current for large-scale functional OTFT digital circuits for low-voltage and low-power operation was examined in this study. We
adopted a complementary structure for the low static leakage current of the inverter gates. Yield improvement is necessary to implement large-scale logic circuits with organic transistors. The output voltage swing from $V_{ss}$ to $V_{dd}$, signal propagations with an inverter, NAND, and NOR gates, and the low leakage currents while using organic printable transistors leading to a reliable operation of the large-scale OTFT logic circuits were evaluated.

2. Device structure, performance, and leakage issue

In this study, semiconductor materials of p-type OTFT (pOTFT) and n-type OTFT (nOTFT) are DNTT and TU-1, respectively. Figure 1 shows the cross-sectional structures of p-type and n-type devices. These devices consist of Al gate electrode layer (gate), AlO$_x$ insulator layer, self-assembled monolayer (SAM), organic semiconductor, and Au top source or drain electrode. As AlO$_x$ and SAM layers are sufficiently thin (4 nm and 2 nm thickness, respectively), devices operate at 3 V or lower, which is the nominal operation voltages on printed carbon boards or integrated circuit chips. Though we fabricated TFT devices with thermal deposition in this paper, the fabrication process can be replaced with printing technologies in the future as materials are developed considering compatibility with printing technologies.

We designed an inverter test element group (TEG) to evaluate the yield and the signal propagation of the logic gate path for reliable operation, and the rail-to-rail operation for low static power consumption. However, in our previous study on the 90-bit security component TEG, the outputs of “0” bits were not sufficiently close to the ground ($V_{ss}$) level, and on-currents of nOTFTs were estimated to be insufficient.

On the security component TEG, the channel lengths ($L$) of pOTFT and nOTFT were 50 $\mu$m, and the channel widths ($W$) were 200 $\mu$m and 800 $\mu$m, respectively. We designed four inverter TEGs, five NAND TEGs, and two NOR TEGs having different cell designs. The device parameters of TEGs are described in Table I. In this chip, we changed the channel length to compensate for the weak nOTFT on-current. Although the enhancement of the nOTFT can be easily achieved by adopting a larger nOTFT width, further extension of nOTFT width causes the implementation area issue. In our chip, too small OTFT width makes external probing of the output signal difficult because of too small on-current, and we defined minimum pOTFT width as 400 $\mu$m (two-finger 200 $\mu$m width). We adopted the longer channel length for pOTFT and weakened the pOTFT on-current to compensate for the weak nOTFT on-current without resulting in an excessively large nOTFT size. We also attempted a 30 $\mu$m channel length for the nOTFT with a metal mask fabricated via the additive method to enhance nOTFT on-current. The shorter nOTFT channel length also enables the implementation of longer channel width in the same area and a further increase in nOTFT on-current.

The inverters #1 and NOR #1 TEGs have identical OTFT sizes for comparison. In the NAND #1 TEG, nOTFT width is extended to 4800 $\mu$m because nOTFTs are stacked and further weakened in the NAND gate. The longer pOTFT channel lengths were adopted in the inverter #2, #3, and NAND #2-#4 TEGs to weaken the pOTFT on-current. A shorter nOTFT channel length was adopted in the inverter #3, #4, NAND #4, #5, and NOR #2 TEGs to enhance the nOTFT on-current.

Figure 2 shows the circuit diagram at the transistor level of the inverter, NAND, and NOR gate used in the TEGs. The inverter gate has input (“A”), and an output (“Y”) ports, and the NAND and NOR gates have two input ports (“A”, “B”) and an output port (Y). The circuit structure of the inverter, NAND, and NOR TEGs are depicted in Fig. 3. Each input and output of the serially connected gates are connected to the pad and can be observed from the external instruments. The numbers of serially connected gates were 14, 8, and 8 for the inverter, NAND, and the NOR gates, respectively. In Fig. 3, “I00” port is an input port, “Y00”, “Y10”, “Y01”, “Y11” in NAND and NOR TEGs) ports can be used as signal inputs or observation of the output, and “Y13” (“Y07”) in NAND and NOR TEGs) port is an output port. “B” input port of NAND and NOR gates are connected to $V_{dd}$ or $V_{ss}$ and one of the stacked nOTFT or pOTFT in NAND or NOR are always ON-state. With this design, we verify the NAND or NOR operation; output if both input ports are 1, or if either of the two input ports are 1.

3. Measurement results and discussion

This section describes the measurement results of the fabricated chips. As the focus of this study included the yield issue, we measured two test chips that were fabricated with identical masks and fabrication processes to obtain reliable measurement results. Figure 4 depicts the micrograph of the 2nd test chip. The chip size is 5 cm × 5 cm.

3.1. Transistor characteristics

OTFTs with several channel lengths were implemented on the test chips, and we measured five pOTFTs and twenty-three nOTFTs with $L=50$ $\mu$m, Six pOTFTs with $L=100$ $\mu$m, seven pOTFTs with $L=150$ $\mu$m, and twenty-three nOTFTs with $L=30$ $\mu$m. The value of W for all pOTFTs and nOTFTs was 400 $\mu$m on the 2nd test chip. Figures 5 and 6 show the

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**Table I. Design parameters of standard cell TEGs and measured yields.**

| TEG | pOTFT $L/W$ ($\mu$m) | nOTFT $L/W$ ($\mu$m) | Chip 1 | Chip 2 | Yield |
|-----|----------------------|----------------------|-------|-------|-------|
| Inv. No.1 | 50/400 | 50/3200 | 50% (7/14) | 50% (7/14) |
| Inv. No.2 | 100/400 | 50/3200 | 75% (12/14) | 100% (14/14) |
| Inv. No.3 | 100/400 | 30/5600 | 50% (7/14) | 88% (12/14) |
| Inv. No.4 | 50/400 | 30/5600 | 75% (11/14) | 57% (8/14) |
| NAND No.1 | 50/400 | 50/4800 | 75% (6/8) | 88% (7/8) |
| NAND No.2 | 100/400 | 50/4800 | 0% (0/8) | 0% (0/8) |
| NAND No.3 | 150/400 | 50/4800 | 0% (0/8) | 0% (0/8) |
| NAND No.4 | 100/400 | 30/8000 | 63% (5/8) | 75% (6/8) |
| NAND No.5 | 50/400 | 30/8000 | 38% (3/8) | 38% (3/8) |
| NOR No.1 | 50/400 | 50/3200 | 75% (6/8) | 88% (7/8) |
| NOR No.2 | 50/400 | 30/5600 | 38% (3/8) | 100% (8/8) |
The relation between gate-source voltage ($V_{gs}$) and the drain-source current ($I_{ds}$) of the fabricated pOTFT and the nOTFT when drain-source voltage ($V_{ds}$) = 2.5 V was measured on the 2nd test chips. A Keysight B2912A source measure unit (SMU) was used to measure OTFT characteristics. The average on-currents of the pOTFT with $L = 50, 100, 150 \, \mu m$ and nOTFT with $L = 50, 30 \, \mu m$ at $V_{gs} = V_{ds} = 2.5 \, V$ are 10.3 $\mu A$, 5.73 $\mu A$, 4.54 $\mu A$, 1.98 $\mu A$, and 2.56 $\mu A$, respectively. The on-current is commonly inversely proportional to the channel length. There are big differences between the on-current of $L = 150 \, \mu m$ pOTFT or $L = 30 \, \mu m$ nOTFT and 1/3 or 5/3 of on-current of $L = 50 \, \mu m$. However, the on-current of $L = 100 \, \mu m$ pOTFT is also larger than the 1/2 of the on-current of $L = 50 \, \mu m$ pOTFT. This relation between the on-current and the channel length, which is not a simple inverse proportion, was also observed in past work. The tendency can be caused by an increase of the threshold voltage or a decrease of mobility on the short channel devices.

The average off-currents of the pOTFT and the nOTFT with $L = 50, 100, 150 \, \mu m$ and nOTFT with $L = 50, 30 \, \mu m$ at $V_{gs} = 0 \, V$ and $V_{ds} = 2.5 \, V$ are 1.70 nA, 1.62 nA, 2.52 nA, 0.642 nA, and 0.442 nA, respectively. The off-current is not necessarily inversely proportional to the channel length. The variability of the off-current is more significant than on-current, and the number of samples might be small in this investigation. The ratio of the on- and off-currents are between 1728 and 6051 and are sufficiently large for logic gate operations.

Here, we observe an increase in the leakage current in Figs. 5(a) and 6(a) when the gate-source voltage ($V_{gs}$) is not close to $V_{ss}$ or $V_{dd}$. The subthreshold leakage current of nOTFT is 0.642 nA and 2.69 nA for $V_{gs} = 0.0 \, V$ and 0.2 V, respectively, which is over four times higher than the static leakage current. The pOTFT has about 0.3 V margin from $V_{gs} = 0.0 \, V$, but the leakage current increases from 1.12 nA

Fig. 2. The schematic of the inverter (a), NAND (b), NOR (c).

Fig. 3. The circuit structure of the (a) inverter, NAND(b), and NOR (c) test element group (TEG). The input and output of each inverter can be probed.

Fig. 4. (Color online) Micrographs of the test chip.
at $V_{gs} = 0.3$ V to 1.67 nA at $V_{gs} = 0.5$ V. The rail-to-rail operation is effective in reducing the static leakage current.

3.2. Yield

3.2.1. Measurement results. We measured the voltage transfer curve (VTC) of the inverters to observe the yield of the implemented logic gates on the TEGs. The output voltage was observed with the SMU set to the current source mode with the current value as low as possible to achieve virtually high impedance. The on-current of the OTFT is on the order of micro-amperes and is vulnerable to the leakage current of the proving instruments. Keysight U2722A SMU was used to supply $V_{dd}$, and Keysight B2912A SMU was used to observe the VTC of the inverters.

The measured yields of the logic gates implemented on the two test chips are summarized in Table I. When the output "1" level is lower than 70% of $V_{dd}$ or output "0" level is higher than 30% of $V_{dd}$, the gate is regarded as failed. The inverter #1 TEG, which did not adopt a long channel length, showed a relatively worse yield than the other inverter TEGs. The best yield was observed for the inverter #2 TEG among the inverter TEGs. The weakening of the pOTFT by adopting the long channel length was effective. The inverter #4 TEG, which adopted a shorter nOTFT channel length, slightly improved the yield compared to the inverter #1 TEG; however, the improvement was not notable compared with the inverter #2 TEG. The impact of the enhancement of the nOTFT on-current by shortening the channel length from 50 to 30 $\mu$m was weaker than that of weakening of the pOTFT on-current by adopting a channel length of 100 $\mu$m as described in Sect. 3.1. The measurement result of the yield of the inverter #4 TEG is consistent with the transistor characteristics. The inverter #3 TEG adopted both the long channel length of the pOTFT and the short channel length of the nOTFT; however, the yield improvement was smaller than that on the inverter #2 TEG. This result implies that the gate design caused an excessively nOTFT on-current on the inverter TEG #4.

NAND #1 and #3 TEGs exhibited almost zero yield; however, improvements in the yield were observed for NAND #2, #4, #5 TEGs. On NAND #5 TEG, which adopted a short nOTFT channel length, slightly improved the yield was observed; however, the yield was still low. On the NAND #4 TEG, which adopted both the long pOTFT channel length and short nOTFT channel length, we observed a 60%–75% yield and the improvement of the yield was notable. As the NAND gate has the stacked nOTFT structure, it is natural that further enhancement of the nOTFT than the inverter is required. However, for the NAND #3 TEG, which adopted the longest pOTFT channel length, the yield was 0%, and 150 $\mu$m of the pOTFT channel length would be excessively long, while the on-current of the pOTFT was considerably weakened. On the NAND #2 TEG, the yield was 0% on the 1st chip and 88% on the 2nd chip. NAND #1 TEG had a strong pOTFT, while pOTFT of NAND #3 TEG was considerably weak. As the pOTFT of NAND #2 TEG is intermediate channel length between the channel lengths of NAND #1 TEG and NAND #3 TEG, NAND #2 TEG is estimated to have a balanced channel length. The yield results on the 2nd chip are consistent with the other NAND TEGs. The yield on the 1st chip may be caused by defective transistor characteristics due to the intra-chip variability of the transistor unique to the 1st chip. The intra-chip variability was covered by our redundant measurement with the two chips.

Fig. 5. (Color online) $I_{ds}$–$V_{gs}$ measurement results of (a) five pOTFT $L = 50$ $\mu$m devices, (a) six pOTFT $L = 100$ $\mu$m devices, (a) seven pOTFT $L = 150$ $\mu$m devices.

Fig. 6. (Color online) $I_{ds}$–$V_{gs}$ measurement results of (a) twenty-three nOTFT $L = 50$ $\mu$m devices, (b) twenty-three nOTFT $L = 30$ $\mu$m devices.
NOR #1 TEG showed over 70% yield on both the test chips. 100% yield was observed on the NOR #2 TEG, although the yield of the NOR #2 TEG on the 1st chip was low(38%). As the NOR gate has a stacked pOTFT, the pOTFT is weakened without a long channel length, the yield of the basic structure of this paper is high, and notable improvement was not observed.

Transistor characteristics of twenty pOTFTs and forty-six nOTFTs were measured for each chip in Sect. 3.1, and the yield of the single pOTFT and nOTFT were 88.9% (17/20) and 85.0% (43/46) on the 1st chip, and 80.0% (16/20) and 82.6% (38/46) on the 2nd chip. These transistor yield results are consistent with the measurement results of the TEG yield variability on two chips. The TEGs where high yields were obtained did not necessarily show 100% yield on both chips because of the limitation of the transistor yield. For example, the probability of all of 14 pOTFT on inverter TEG operates with 85% yield either on two chips is about 19.5%. nOTFT has many fingers, and stack-at-1 failure (an inverter output is fixed to “1”) can be covered with other fingers. In addition, when the area-dependent variability does not affect a TEG, that TEG is free from the impact of the area-dependent variability, and the yield will be higher. Observations of 100% yield on a few conditions are reasonable even if the yields of the single transistors are considered.

3.2.2. Discussion. In the case of silicon integrated circuits, the adjustment of the channel width was adopted for optimization of the operation speed, the power consumption, and the duty cycle, but not notably for the yield. The channel circuits, the adjustment of the channel width was adopted for the NAND #1 TEG, the pOTFT is weakened without a long channel length, the yield of the basic structure of this paper is high, and notable improvement was not observed.

In this study, we adjusted the channel length to balance the on-currents of the pOTFT and the nOTFT. In contrast, the general standard cell design focuses on optimizing the channel width, and the channel length is fixed. For instance, we designed an \( L/W = 50 \, \mu m/400 \, \mu m \) pOTFT and \( L/W = 50 \, \mu m/4000 \, \mu m \) nOTFT for NAND #1 TEG. The channel length of the pOTFT was adjusted for the NAND #4 TEG, which resulted in considerable yield improvement.

In addition, adjusting the channel length effectively reduces the standard cell area, which has a considerable impact on the circuit area. The area consumption of the pOTFT and the nOTFT was 0.1 mm\(^2\) and 1 mm\(^2\) on the NAND #1 TEG, and 0.14 mm\(^2\) and 0.984 mm\(^2\) on the NAND #4 TEG. Assuming that modifying only channel width to balance on-currents of the pOTFT and the nOTFT, nearly 2.3 \times area of nOTFT would be required because the pOTFT and the nOTFT on-currents were decreased or increased to 56% and 129%, as indicated by the measurement results in Sect. 3.1. Further, the 2.3 \times area of nOTFT is almost equal to the 2.3 \times channel area because 90% of the total OTFT area is occupied by the nOTFT. However, by adjusting the channel length, we successfully improved the yield without increasing the OTFT area. Figures 7 and 8 show the layout of the NAND cell used on NAND #1 and #4 TEGs. The cell size was 2400 \( \mu m \times 1950 \, \mu m \) for both NAND TEGs. Consequently, adjusting the channel length to improve the yield is effective for reducing the area consumption of the circuit.

3.3. Signal propagation, operation voltage and rail-to-rail operation

We evaluated the signal propagation and the rail-to-rail operation for the large-scale and low-power OTFT digital circuits. We successfully obtained the best yield on inverter #2, NAND #2, and NOR #2 TEGs on the 2nd chip for each gate type. We adopted these TEGs to evaluate the signal propagation and rail-to-rail operation. Figure 9 depicts the VTCs of each stage gate measured on the inverter #2, NAND #2, and NOR #2 TEGs at \( V_{dd} = 2.5 \, V \). In Fig. 10, the VTCs when the input signal was input to 1st stage gate (2nd stage gate for NAND because the 1st stage gate did not operate) and the last stage output was measured at \( V_{dd} = 2.5 \, V \), and 14-stage, 7-stage, 8-stage signal propagations were observed for the inverter, NAND, and NOR TEGs. We successfully achieved the signal propagation at 2.5 \( V \). Figure 11 depicts the VTCs with the 1st gate input and the last gate output at \( V_{dd} = 1.75 \, V \). The minimum operation voltages of these TEGs were 1.75 \( V \).

We also confirmed the rail-to-rail operation for these TEGs. Figures 12 and 13 depict the \( V_{(V_{dd} \text{ level})—(logic \text{ 1 level})} \) voltage and the (logic “0” level)—\( V_{(V_{ss} \text{ level})} \) voltage at each stage at \( V_{dd} = 2.5 \, V \) and 1.75 \( V \), and \( V_{ss} \) levels was not observed. There were notable increases in the difference between the \( V_{dd} \) and \( V_{ss} \) levels and the 10th and 11th stage of the inverter TEG at \( V_{dd} = 2.5 \, V \) and 1.75 \( V \), and the 5th stage of the NAND TEG at \( V_{dd} = 1.75 \, V \), which indicates that the intermediate voltage was output as a “0” or “1” logic value. However, these intermediate voltages were mitigated at the later stages, and the rail-to-rail operations were recovered. Consequently, no attenuation and recovery tendencies of the rail-to-rail operation were observed on the test chip. This indicates that the standard cells designed in this study can achieve the rail-to-rail operation on large-scale circuits if the
sufficient yield of the transistor itself is obtained, thus demonstrating the feasibility of large-scale and low-power OTFT digital circuits.

3.4. Static power consumption
We observed the static leakage current on the inverter TEG #2(100%), NAND TEG #2(88%), and NOR TEG #2(100%), achieved the best yield for each gate type. The input voltage of the 1st gate in the inverter and the NOR TEG and the 2nd gate in the NAND TEG was fixed to 0 V. The 1st gate of the NAND gate was the only gate that did not operate in the NAND #2 TEG. The static leakage currents were 8.19 nA, 3.08 μA, and 23.5 nA at \( V_{dd} = 2.5 \) V in the inverter, NAND, and the NOR TEGs, respectively. The leakage current of the single inverter gate corresponds to the 585 pA on average, achieving the sub-nA-class leakage current. The off-leakage currents of the pOTFT and the nOTFT in this study were between 0.1 and 1 nA, thus successfully minimized the leakage currents of the inverters. By optimizing the inverter design parameter, we maximized the ratio of rail-to-rail operation cells, and minimized the number of intermediate-voltage-output cells which cause serious static through-currents or operation failure. Finally, we achieved a 100% yield for these fourteen inverters and minimized leakage current.

As the NAND and NOR TEGs contain eight gates, the leakage currents of the single NAND or NOR gate on average were 385 and 2.94 nA. The observed leakage current on the NAND #2 TEGs is considerably larger than that of the inverter. In the NAND #2 TEG, we hypothesized that a defective NAND gate could cause a large leakage current. In the NOR #2 TEG, the leakage current was approximately five times larger than that of the inverter #2 TEG. Simple multiplication of the parallel nOTFT structure (2\times increase of the leakage) and an increase of channel width (1.75\times (5600/3200) increase) results in a 3.5\times increase of the leakage. The increase in the leakage current in the NOR gate can be explained by these factors. Further, in the NOR gate, the design optimization successfully reduced the leakage current of the NOR gates as well as that of the inverter gates.

As described in Sect. 3.3, the inverters #2 TEG and NOR #2 TEG include gates that do not achieve rail-to-rail operation but propagate the switching signal. Such gates may increase the leakage current and must be reduced. The leakage current of inverter #2 TEG and NOR #2 TEG were successfully lowered, and the number of gates that output the intermediate voltage sufficiently were reduced. The NAND #2 TEG included a failed gate, which did not propagate the signal, and a considerable leakage current was observed. Though the failed gate must be removed from the circuit, the gates that produce the intermediate voltage as output are acceptable if their rate is sufficiently reduced.

3.5. Delay
This section presents an evaluation of the signal propagation delay with the inverter #2, NAND #2, and NOR #2 TEGs wherein we observed the best yields among the TEGs for each gate type. The pulse signal was the input to the 1st stage of the TEG, and the output of each gate was observed. The input pulse signal is generated with the pattern generator, and the output signal is measured with the oscilloscope. On the NAND #2 TEG, the 2nd gate is used as the input gate because the 1st gate does not operate. On the inverter #2 TEG, the 1st gate was broken during this measurement, because of the high voltage due to signal reflection at the capacitive terminal, and the 2nd gate was used instead of the 1st gate as the input gate.

Table II summarizes the measured gate delay. The gate delay is defined by the delay from the time when the rise or fall input signal reaches 50% of \( V_{dd} \) to the timing when the output signal reaches 50% of the output “1” level. The output signal observed on the oscilloscope frequently did not reach the \( V_{dd} \) level because 0.1 μA leakage current of the oscilloscope pulls down the output signal, and the timing that defines the delay is set to 50% of the output “1” level. The rise signal was not observed at the 7th and 13th stages on the inverter TEG, and the delay could not be measured. The missing of the rising waveform is because the weak on-current is overwhelmed by the oscilloscope leakage current.
and cannot pull up the signal. When the VTC was measured, as mentioned in Sect. 3.3, the output was observed using the SMU, and the leakage current was set to below 1 nA; the inverter operation of the 7th and 13th stages was confirmed on the basis of the measured VTCs described in Sect. 3.3.

When the oscilloscope probe is set to the later stage than the 7th stage and there was no leakage path on the 7th gate, the signal transitions at the later stage were successfully measured, and the 7th gate was estimated to work.

Figure 14 depicts the histograms of the single-stage delay calculated from Table II. The delays of the 1st to 6th gates are emphasized in Fig. 14(a). The delay was categorized by the (a) (b) (c) levels and “1”/“0” levels on (a) the inverter #2 TEG, (b) the NAND #2 TEG, (c) the NOR #2 TEG. $V_{dd} = 2.5$ V.

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Figure 14 depicts the histograms of the single-stage delay calculated from Table II. The delays of the 1st to 6th gates are emphasized in Fig. 14(a). The delay was categorized by the (a) (b) (c) levels and “1”/“0” levels on (a) the inverter #2 TEG, (b) the NAND #2 TEG, (c) the NOR #2 TEG. $V_{dd} = 2.5$ V.
The delay tendency appears to have a log-normal distribution. The tendency of the OTFT mobility is also a log-normal distribution, and the measured delay is consistent with the common mobility tendency. Therefore, although the inverter delay does not appear to have a log-normal tendency, the histograms of the 1st–6th gate delay are relatively close to the log-normal distribution. At the 8th–12th stage, negative delays were frequently observed on the inverter TEG. This negative delay is estimated to be observed when a relatively fast inverter with 10–100 ms delay is placed after the slow inverter with over 1000 ms delay, as the fast inverter switches before the former-stage slow inverter. The actual delay of the inverters where the negative delays were observed is estimated to be tens or hundreds of milliseconds because the delays of such inverters are faster than slow inverters with a thousand milliseconds delay. However, we could not identify to which bin these delays should be set. As these uncertain negative delays are removed from the histogram, the observation of inverter delay distribution at the 1st–6th stage is reasonable.

Table II. Measured gate delay on inverter #2, NAND #2, NOR#2 TEGs. Path delays observed at the 2nd–14th inverter, 2nd–8th NAND, and 1st–8th NOR gates when the pulse waveform was input to the input of the 2nd gate of the inverter TEG, the 2nd gate of the NAND TEG and the 1st gate of the NOR TEG are described. At the 8th and 14th gates (7th and 13th stages on the table) on the inverter TEG, the low on-current of the pOTFT was overwhelmed by the oscilloscope leakage current, and output pulse waveform could not be observed.

| Stage | Rise input Delay (ms) | Fall input Delay (ms) |
|-------|-----------------------|-----------------------|
| 1     | 14.7                  | 13.0                  |
| 2     | 15.7                  | 30.1                  |
| 3     | 223                   | 270                   |
| 4     | 926                   | 305                   |
| 5     | 1317                  | 1120                  |
| 6     | 1328                  | 1102                  |
| 7     | 6831                  | 7353                  |
| 8     | 4456                  | 7237                  |
| 9     | 10 596                | 12 170                |
| 10    | 29 890                | 4890                  |
| 11    | 9400                  | 17 381                |
| 12    | 29 890                | 4890                  |
| 13    | —                     | —                     |

| Stage | Rise input Input | Fall input Input |
|-------|------------------|------------------|
| 1     | 1.55             | 8.20             |
| 2     | 44.1             | 24.5             |
| 3     | 59.4             | 167              |
| 4     | 138              | 198              |
| 5     | 154              | 636              |
| 6     | 247              | 769              |
| 7     | 278              | 1648             |
| 8     | 440              | 2376             |

4. Conclusion

This paper presents the standard cell designs of OTFT and the yield and static power consumption based on the measurements of the test chips. Our design method involves adjusting the channel length and avoiding the increase of the standard cell area due to weak nOTFT on-current, thus improving the yield of the inverter, NAND, and NOR gates. The rail-to-rail operation and signal propagation of the logic gates were confirmed with serially connected logic gates, and the designed standard cells can be applied to large-scale OTFT logic circuits. Owing to the rail-to-rail operation of the logic gates, nA to sub-nA class leakage current per gate was achieved on the inverter and NOR TEGs, where a 100% yield was achieved, and low static power consumption was attained using our standard cell designs.

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