Realizing a robust, reconfigurable active quenching design for multiple architectures of single-photon avalanche detectors

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ABSTRACT

Most active quench circuits used for single-photon avalanche detectors are designed either with discrete components which lack the flexibility of dynamically changing the control parameters, or with custom ASICs which require a long development time and high cost. As an alternative, we present a reconfigurable and robust hybrid design implemented using a System-on-Chip (SoC), which integrates both an FPGA and a microcontroller. We take advantage of the FPGA’s speed and configuration capabilities to vary the quench and reset parameters dynamically over a large range, thus allowing our circuit to operate with a wide variety of APDs without having to re-design the system. The microcontroller enables the remote adjustment of control parameters and re-calibration of APDs in the field. The ruggedized design uses components with space heritage, thus making it suitable for space-based applications in the fields of telecommunications and quantum key distribution (QKD). We characterize our circuit with a commercial APD cooled to -20°C, and obtain a deadtime of 35ns while maintaining the after-pulsing probability at close to 3%. We also demonstrate versatility of the circuit by directly testing custom fabricated chip-scale APDs, which paves the way for automated wafer-scale testing and characterization.

Keywords: single photon avalanche detectors, System on chip SoC, FPGA, active quenching, chip-scale APD, reconfigurable quenching circuit, automated wafer-scale testing

1. INTRODUCTION

Single photon detection is used widely in quantum optics technology. Increasing the rate and efficiency of single photon detection is a fundamental way to improve the overall efficiency of optical systems. The most popular method to detect single photons is by using Geiger-mode Avalanche Photo Diodes (GM-APD) in which photon absorption triggers a current due to avalanche multiplication process. This avalanche current needs to be stopped quickly and the APD needs to be restored to its normal operating mode before it can detect the next photon. This process is called \textit{quenching} and can be done either passively or actively. Although \textit{passive quench} (PQ)\textsuperscript{1,2} circuits are simple to implement they do not reset the diode quickly to its nominal state which limits their detection efficiency. \textit{Passive Quench Active Reset} (PQAR)\textsuperscript{3} circuits can provide shorter and well-defined reset times but fail to restrict the after-pulsing probability of the APD within acceptable bounds if the reset times set are too short. \textit{Active quench} (AQ)\textsuperscript{4} circuits on the other hand provide fast response and reset times while limiting the after-pulsing probability of the APDs and hence are most suitable for high detection rate applications.

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**Motivation**

In several active quenching circuit designs, generation of the quench and reset signals for the APD is done using only discrete hardware components.\(^5\)\(^7\) Such designs are cheaper to manufacture but critical parameters such as the quench and reset times are hard bound and cannot be changed dynamically. Changing the quench and reset time can compensate for deviation in APD performance at run-time occurring due to factors such as temperature variation. As an alternative to discrete systems, monolithic integrated\(^6\)\(^12\) active quench circuits have been developed which offer flexibility to change parameters dynamically while also reaching very high count rates and detection efficiency. However, fabricating custom ICs is a complex process requiring long development cycles and a very high manufacturing cost.

In this paper we describe a hybrid design for active quenching of Geiger-Mode APDs (GM-APD) comprising of minimal discrete components and a commercially available System-on-Chip (SoC)\(^13\) which has both an FPGA and a micro-controller integrated on the same chip. The active quench control logic is implemented on the FPGA which allows to dynamically change typical active quench parameters such as quench width, reset width, deadtime, etc. The microcontroller interfaces with a PC and provides remote access to the FPGA registers which allows to re-calibrate the APDs deployed in the field during run-time. Only a few discrete components need to be placed close to the APD head while the SoC can be placed farther away without compromising the performance and detection efficiency. We present results to show that our system can achieve a deadtime of 35ns despite the APD head located \(\approx 15\)cm away from the SoC, thus allowing to reach count rates of \(>28\)Mcps. Although our system is mainly designed for active quenching, we show how it can also be reconfigured to work in either passive quench or PQAR configurations.

The tunable parameters in our design can be varied over a wide range allowing operation with APDs from several manufacturers without modifications. We demonstrate this versatility by simultaneously operating our system with a commercial APD\(^14\) and our in-house custom fabricated chip-scale APD,\(^15\) both of which have different characteristics in terms of breakdown voltage, over-voltage, etc. We present some preliminary results for breakdown voltage and dark counts obtained with the custom fabricated chip-scale APDs which further validates our design. In principle, the flexibility in our system would be useful both in a research setup comprising of multiple device variants and in mass production for doing direct wafer-scale testing.

**2. DESIGN AND IMPLEMENTATION**

Similar to conventional active quenching circuits, our system operates in two phases in response to the occurrence of an avalanche: 1) **quench** - reduce the bias voltage of the diode below its breakdown voltage for a few nanoseconds and 2) **reset** - restore the bias voltage above the breakdown for a few nanoseconds while bypassing the ballast resistor at the same time. After the reset phase, the ballast resistor is reconnected and the APD returns to the nominal state. The main functional blocks of our system are shown in figure 1. The ZedBoard\(^13\) development kit with a Zynq-7000 based SoC is used for realizing the FPGA and microcontroller modules. The GM-APD is connected with the quench/reset generator on the FPGA using a custom PCB with minimal discrete components. We use the LT6752-3 high speed comparator (COMP) which produces complementary outputs after detecting the avalanche pulse across sense resistor \(R_S\). The feedback path for doing the quench comprises of a fast AND gate, P-MOSFET \(P_1\) and N-MOSFET \(N_1\). Reset is done through N-MOSFET \(N_2\). The values of \(R_4\) and \(C_1\) are set such that the D-FlipFlop (D-FF) trims the comparator output to 20ns pulses (OUT) which are used for characterizing the deadtime and after-pulsing probability. Matsusada high voltage DC-DC converters are used to derive a bias voltage \((V_{BIAS})\) between 0-500V while quench voltage \((V_{QUENCH})\) is derived from an external power supply.

**2.1 Operation in active quench configuration**

The design and operation is better understood with the timing diagram shown in figure 2. The avalanche current in the APD causes the voltage at the APD anode (GM-APD_{ANODE}) to rise and consequently the voltage across \(R_S\) exceeds the comparator reference voltage \((V_{REF})\), which is typically set to \(\approx 17\)mV. In response the comparator (COMP) toggles the complementary output pulses \(Q\) to high and \(\bar{Q}\) to low. Output \(Q\) is fed back to one of the inputs of the AND gate while the FPGA keeps the other input of the AND gate
(QUENCH_ENABLE) high before the avalanche occurs. So the AND gate output (QUENCH) goes high to turn ON $N_1$ which subsequently turns ON $P_1$ to initiate quenching. As a result of this, the anode voltage of GM-APD reaches the quench voltage ($V_{QUENCH}$) which effectively reduces the voltage across the APD below its breakdown voltage and brings it into the quench state. Until then the APD is passively quenched and the avalanche current is limited by the ballast resistor ($R_B$). This feedback path is kept as short as possible to reduce the response time and after-pulsing probability.\textsuperscript{16}

The other comparator output $\overline{Q}$ is inverted (APD_PULSE) and fed into the quench/reset logic to register the occurrence of an avalanche and into a 24-bit counter to record the total number of avalanches per second. The duration for which the APD stays in the quench state is configurable and after this duration the FPGA sets the QUENCH_ENABLE signal to low, as shown in figure 2. This drives the output of the AND gate to low which turns OFF $N_1$ and $P_1$. The FPGA then initiates the reset state by setting the RESET signal high to turn ON $N_2$. The GM-APD_ANODE voltage then dips to 0 which brings the relative bias voltage of the APD above its breakdown voltage. This also makes the comparator output $Q$ to go low and $\overline{Q}$ to go high after which $N_2$ is turned OFF by setting the RESET signal low. The duration of reset is configurable and typically kept as short as possible. To ensure that both $P_1$ and $N_2$ are not ON at the same time, the FPGA inserts a tiny configurable delay between end of the quench and start of the reset. The total duration from the start of the avalanche to the completion of the reset constitutes the deadtime of the system. After reset the QUENCH_ENABLE signal is driven high again to keep the system ready for the next detection event.
The operation of our system is verified with a commercial SAP500-TO8 APD,\textsuperscript{34} biased with an excess voltage of 10V. \(V_{\text{QUENCH}}\) is set to 15V, which potentially allows to operate the APD up to an excess voltage 12V. Figure 3 shows the GM-APD ANODE voltage (C2) captured with a LeCroy Waverunner 610Zi oscilloscope. After the avalanche starts, the activation of quench occurs at \(\approx 9\text{ns}\). Referring to figure 1, this delay is incurred in the quench feedback path which is the sum of propagation delays through the comparator, AND gate and the switch ON delays for \(N_1\) and \(P_1\). After quench is activated, the GM-APD ANODE voltage rises rapidly to \(V_{\text{QUENCH}}\) within 2ns. The OUT signal (C1) is delayed by \(\approx 6\text{ns}\) due to the propagation delays through the comparator, inverting buffer and D-Flipflop (D-FF).

The minimum quench duration is then decided by the propagation delay of the APD PULSE signal from the comparator through the FPGA logic to drive QUENCH ENABLE signal and AND gate output to low. In our case this is 10ns despite the physical separation of \(\approx 15\text{cm}\) between the APD head and the SoC. The delay between quench and reset is typically set to 5ns to account for switch OFF delays of \(N_1\) and \(P_1\). So in figure 3 it can be observed that the reset is activated 15ns after GM-APD ANODE reaches \(V_{\text{QUENCH}}\). The reset pulse duration is kept as small as possible and is typically between 5ns-10ns depending on the value of \(V_{\text{QUENCH}}\). Table 1 shows the list of configurable parameters in our design along with their range. The FPGA module for quench/reset generation runs on an internal 200MHz clock which allows to increase/decrease the timing parameters with a minimum step size of 5ns.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|}
\hline
Parameter & Min. & Max. & Units & \hline
Quench duration & 10 & 1000 & ns & \\
Reset duration & 5 & 1000 & ns & \\
Deadtime & 35 & 1000 & ns & \\
Quench voltage & 0 & 30 & V & \\
Bias voltage & 0 & 500 & V & \\
\hline
\end{tabular}
\caption{Reconfigurable parameters and their range of supported values}
\end{table}
2.2 Operation in PQAR and PQ configurations

Our system operates in PQAR mode when the FPGA is configured to keep the QUENCH_ENABLE signal low at all times. This disables the AND gate shown in figure 1 and the QUENCH signal is never triggered, keeping $N_1$ and $P_1$ always OFF. So when the APD avalanche occurs it is quenched passively through ballast resistor $R_B$ for a designated duration, after which the FPGA only drives the RESET signal to high and turns ON $N_2$. This restores the relative reverse bias voltage of the GM-APD to $V_{BIAS}$. For passive quenching (PQ) mode, the FPGA is configured to keep both the QUENCH_ENABLE and RESET signals low at all times. As a result $P_1$, $N_1$ and $N_2$ are never turned ON and so the APD is both quenched and reset passively. However in both modes the comparator still continues to detect APD avalanches and toggles the OUT and APD_PULSE signals which can be counted by the FPGA.

3. PERFORMANCE CHARACTERIZATION WITH COMMERCIAL APD

We characterize our system with the SAP500-T8 APD which has a built-in TEC (Thermo-electric cooler) to vary the temperature. For this APD, we present results for the lowest achievable values for deadtime, after-pulsing and operating temperature at an excess voltage of 10V for any given temperature.

![Figure 4](image.png)

Figure 4. Deadtime of $35\text{ns}$ is observed with accumulated OUT pulses (C1) captured on the oscilloscope in persistent mode at a background rate of $\approx 66\text{Kcps}$

3.1 Deadtime

Once an avalanche is detected, the APD cannot detect another avalanche until the first avalanche is completely quenched and the APD is reset back to its original state. This constitutes the deadtime and as shown in figure 2. We capture the accumulated OUT pulses on the oscilloscope in persistent mode. It can be observed in figure 4 that the deadtime (time interval between the rising edge of the first pulse and the rising edge of the earliest subsequent pulse) is $35\text{ns}$ which in-principle allows for detection rates of $>28\text{Mcps}$ with our system.

3.2 After-pulsing probability and temperature

It is beneficial to operate the APD at lower temperatures as it reduces dark counts (occurring due to thermal excitation) but doing so increases after-pulsing. The probability of after-pulsing also increases when the deadtime of the circuit is reduced. We measure the after-pulsing probability for the SAP500-T8 using our system for different deadtime and temperature. This is done by computing the second order auto-correlation $g^{(2)}$ of the OUT pulses using an external time-tagger module (with 2ns time resolution). One such instance is shown in figure 5(a) where the deadtime $(Dt)$ is $35\text{ns}$, the APD temperature is $253\text{K}$ ($-20\text{°C}$) and over-voltage is $10\text{V}$. 

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BIAS is derived from a bench-top power supply. To prevent the breakdown voltage BIAS, so as to always keep it 2V above $V_{0}$. Although $V_{QUENCH}$ for both APDs was derived from the BIAS, the $V_{QUENCH}$ for both APDs was maintained between 18V to 27V in conjunction with BIAS. The background rate is $\approx 30$Kcps and the timestamps are recorded for 10 seconds which gives more than 300,000 data samples ($C_{Total}$) of arrival times in total. The $g^{(2)}$ auto-correlation is then computed at a time resolution of 2ns. In figure 5(a) it can be seen that there is a high degree of correlation of arrival times immediately after the deadtime and the counts here constitute after-pulses as highlighted in the graph. After reaching a peak the counts drop exponentially until they flatten out to an average value which we call ‘floor’, beyond which the correlation is weak or nil. Theoretically, the after-pulse probability $P_{ap}$ is defined as:

$$P_{ap} = \frac{\sum_{\tau=0}^{\infty} C_{\tau} - floor}{C_{Total}} \tag{1}$$

where $C_{Total}$ is the total number of events and $C_{\tau}$ is the count value at each time bin $\tau$. Using this approach, the percentage of after-pulsing probability for SAP500-T8 obtained with our system is shown in figure 5(b) for four operating temperatures (-20$^\circ$C, -10$^\circ$C, 0$^\circ$C and +20$^\circ$C). The deadtime is varied in steps of 5ns by changing only the quench duration while keeping all other parameters constant. W.r.t. Eqn. 1, for our data we consider $Dt$ as time bin of the first observed correlation event and 10$\mu$s as the upper limit for $\tau$. It is observed that $P_{ap}$ at the lowest temperature (-20$^\circ$C) and lowest deadtime (35ns) is 2.95±0.08% and remains below this value for all other settings of deadtime and temperature. For most practical applications such as QKD, it is desirable to keep the after-pulsing probability below 5%.7,11

4. INTEGRATION WITH CUSTOM CHIP-SCALE APD

After validating the performance of our active quench system with a widely used commercial APD (SAP500-T8), we further use it for testing our custom fabricated chip-scale APDs in Geiger mode. These are Si waveguide APDs integrated with on-chip photonic waveguides and are interfaced with the active quench system using RF probes. The active quench system shown in figure 1 was modified to include a second identical active quench channel so that both the SAP500 and custom chip-scale APD can be simultaneously connected and operated in parallel. Both GM-APDs are controlled by only one SoC through replication of the quench/reset generator and the counter modules on the FPGA. The SAP500 was operated at room temperature while the temperature of the chip-scale APD was varied between -20$^\circ$C and +50$^\circ$C using a TEC. To rule out the presence of any stray light in the setup, the count rate of the SAP500 was monitored closely during the experiments to ensure that the dark counts always remained at $\approx 20$Kcps, which is the expected value for this APD at room temperature when operated at an excess voltage of 10V. The breakdown voltage of the chip-scale APDs are typically between 16V to 25V and their $V_{BIAS}$ is derived from a bench-top power supply. To prevent the breakdown voltage of the chip-scale APDs from drifting,15 $V_{QUENCH}$ was maintained between 18V to 27V in conjunction with $V_{BIAS}$, so as to always keep it 2V above $V_{BIAS}$. Although $V_{QUENCH}$ for both APDs was derived from the
same bench-top power supply, any changes in $V_{\text{QUENCH}}$ does not affect the operation of the SAP500 since $V_{\text{QUENCH}}$ is always greater than 15V for all tests. Considering these high voltage values, the durations of quench, reset and deadtime for both channels were set conservatively higher so as to provide sufficient time for the MOSFETs to switch ON/OFF. So for both channels, the quench duration was set to 25ns, the reset duration to 15ns and a delay of 10ns between quench and reset, giving a total deadtime of $\approx 65$ns (inclusive of initial response time and all other delays) for all experiments. $V_{\text{QUENCH}}$ and $V_{\text{BIAS}}$ of the chip-scale APD were changed at run-time using scripts running on a laptop PC, while the other parameters in Table 1 remained fixed. Figure 6 shows variation in dark count and breakdown voltage w.r.t. temperature for one chip-scale APD. To check for hysteresis in breakdown voltage, the temperature of the APD was changed in three continuous phases. It was first cooled from +20°C to -20°C, then warmed up from -20°C to +50°C and again cooled down from +50°C to +20°C. In each phase temperature was changed in steps of 10°C. At each temperature, $V_{\text{BIAS}}$ was initially set to a value well below the breakdown voltage and the detected counts were ensured to be 0. $V_{\text{BIAS}}$ was then increased in steps of 0.05V every 2 seconds until the SoC started measuring counts, which indicated the breakdown voltage. $V_{\text{BIAS}}$ was then kept constant and the dark counts were recorded. Before each new measurement the APD was reset by switching off $V_{\text{BIAS}}$. It can be observed that the variation of breakdown voltage and dark count w.r.t. temperature follows a well known trend as seen with existing commercial devices.

4.1 Advantage of using SoC based active quenching for testing chip-scale APDs

For preliminary tests, only dark counts and breakdown voltage of one chip-scale APD have been recorded. Future tests will involve characterizing the after-pulsing probability (like shown in figure 5) of each APD for at least 10 different deadtimes, 5 different temperatures and 3 different excess voltages, which amounts to a minimum of 150 test cases per APD. There are more than 400 variants of our custom chip-scale APDs with each differing in channel length, width, doping concentration etc. So characterizing after-pulse probability for all of them requires 60,000 tests in total. This means the active quench system needs to be re-configured 60,000 times for executing the complete test set. Using hard-wired fixed active quench circuits for this purpose is impractical since it requires a lot of manual intervention for changing parameters, which is both laborious and error prone. Using our SoC based active quench system instead paves way for making these adjustments instantly with script-based automation thus saving both cost and time.
5. CONCLUSION AND FUTURE WORK

We have described a hybrid design for a re-configurable active quench system which can be used to characterize multiple APD architectures. We have implemented the design with readily available components and characterized it with the SAP500 commercial APD cooled to -20°C and achieved a deadtime of 35ns while limiting the after-pulsing probability to ≈3%. We have also integrated our active quench system directly with custom chip-scale APDs and presented preliminary results for variations in their breakdown voltage and dark counts w.r.t. temperature. Our active quench system can also be used in other experiments and commercial applications such as Quantum information processing, random number generators, time-correlated single photon counting (TCSPC) and range measurement applications such as LIDAR. Looking ahead, the deadtime of the quenching system can be reduced further by using faster MOSFETs which will increase the detection rate and efficiency. The SoC firmware can be upgraded to directly compute after-pulse probability without additional equipment.

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