A Novel Design of Mach-Zehnder Modulator Bias Controller Based on Pilot Tone Method

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Abstract. The Mach-Zehnder (MZ) modulator is a widely-used electro-optic modulator, but its operation point drifts with time and temperature, making the modulation performance worse. Therefore, a bias controller is needed to suppress drift. MZ modulator bias control method based on pilot analysis has good robustness and thus has many practical applications. However, many of the circuit designs based on the pilot method of the MZ modulator bias controller (MBC) are complicated, and the flexibility of the pilot generation is not satisfying. In response to these shortcomings, the paper introduces a new MZ modulator bias controller design. The bias controller uses the internal timer and DAC resources of the MCU to form a DDS generator instead of the traditional external oscillator, which makes the generation of the pilot frequency more flexible, and the signal conditioning circuit is improved. Test results show that the proposed MZ bias controller can achieve an extinction ratio of more than 30dB, and can finish the lock process at the Quad point within 20 seconds.

1. Introduction
The transmission curve of the MZ modulator is as shown in figure 1, and the half-wave voltage $V\pi$ is the difference between the driving voltages of the adjacent maximum point and the minimum point on the transmission curve [1]. In a pulsed light modulation system, the bias voltage of the electro-optic modulator needs to be controlled at a minimum value of the transmission curve. At this time, the electro-optic modulator outputs pulse light of a high extinction ratio [2]. However, the actual operating point deviates from the set working point with time and temperature, which decrease the extinction ratio performance. Therefore, it is necessary to introduce an automatic control system to lock the operating point of the modulator.

Common optical modulator bias control methods are average optical power method and the pilot method. Initially, the method of detecting the average optical power is used, but it will fail when the attenuation changes [3]. In recent years, it has also been proposed to use the first-order and the second-order derivatives of average optical power, which makes the detection parameters unaffected by optical power, but the demanded sensitivity of the detection circuit is too high [4]. Using pilot is the most mature method. Due to modulation effect, at the peak or null point, the first harmonic of the output pilot is zero, while the second harmonic is the largest. It’s opposite at the $Q+/Q-$point. Therefore, it can be used as the discriminating basis. Its processing is based on frequency domain analysis and requires lower signal to noise ratio [5].
2. Hardware design for bias controller

2.1 Overall Hardware design

The pilot method has been introduced in the foregoing. It’s obvious that the pilot signal is the core of the entire system. The digital technology is applied in pilot signal processing and control, so a microcontroller is introduced. Actually, it is a typical embedded hardware design architecture mixed with both Analog part and digital part. The overall hardware structure is shown in figure 2.

After the pilot signal is generated by the MCU, it is signal conditioned and added with the bias signal. It is then loaded onto the bias port of the MZ modulator. The optical power is detected by a photodiode to capture the modulated pilot signal. ADC is applied to conduct A/D conversion and sends data back to the MCU. Thus, there build a close loop for pilot signal to check the modulator work point.

In our design, MCU STM32F406RGT6 from STMicroelectronics is introduced. The STM32F4 family of microcontrollers is a series of 32-bit high performance microcontroller based on the ARM Cortex-M4 core with FPU. It supports DSP instructions and has a wealth of on-chip resources [6].

For this design, the floating-point computing power and operation speed of this type of MCU can meet the requirements of real-time processing. The built-in memory and the integrated components such as TIM, DAC, USART and SPI satisfy our needs. It is more conducive to circuit simplification and cost control.

2.2 Pilot signal conditioning circuit

The pilot frequency of 1 kHz is output by the 12bits DAC inside the microcontroller. To fully utilize to take advantage of each bit of DAC, the amplitude of the input pilot signal is set to half the reference voltage. In order to attenuate the pilot signal to a reasonable amplitude of about 60 mV, we construct a pilot signal conditioning circuit. The schematic diagram of the pilot signal conditioning circuit is shown in the following figure 3.
The implementation of the attenuation circuit is mainly based on an active reverse proportional circuit. Before the signal passes through the attenuation circuit, the pilot signal within a voltage ranging from 0V to 3.3V through the DAC is first buffered to compensate for the driving capability. Finally, it passes through a low-pass filter. The pilot signal will be added to the bias output through a coupling capacitor in a subsequent circuit.

2.3 Bias voltage conditioning circuit

The original bias voltage is generated by the external 16-bits DAC8551 chip under control of the MCU through SPI interface. The initial output signal amplitude ranges from 0 to 3.3V, while the actual desired bias control output range is from -10V to +10V, which requires signal conditioning. The signal conditioning circuit mainly realizes three functions. The first is transformation of the single-ended signal range to the balanced signal range. Then is the proportional amplification and the last is superposition of the pilot signals. The schematic diagram of the bias conditioning circuit is shown in figure 4.

2.4 Optical power and pilot detection circuit

This part of the circuit consists of the pre-stage TIA amplifier, feedback network, buffer amplifier stage, channel switching and anti-aliasing filter circuit. In view of the high input impedance and low noise requirements, the op amp AD8605 is selected. The chip is a JFET op amp with GBW of 10MHz, supporting voltage supply from 2.7V to 5.5V [7]. Most notable is the chip's input bias current of only 1pA, which is ideal for the construction of TIA amplifiers [8]. In addition, in order to expand the dynamic range of the entire amplifier circuit, a feedback network is designed in the system. Each channel of this part is controlled by the switching signal from MCU. The Analog switch is used to change the transimpedance of the TIA amplification and thus the modified the gain. The reason why the programmable gain amplifier is not considered in the latter stage is to achieve a low noise level when most gain is realized in the front stage. The following figure 5 shows the circuit block diagram.
Figure 5. Optical power and pilot detection circuit

Although the system utilizes pilots for bias point locking, it also needs to measure the average optical power. It is worth noting that the pilot signal is very weak relative to the DC signal. The DC component will be saturated before the AC signal reaches a suitable amplitude for the ADC range. Therefore, here an additional AC amplification circuit is designed. Although linear amplification does not improve the SNR, it can make full use of the ADC range when performing AC measurement, resulting in reduction on the quantization error. Finally, the anti-aliasing circuit uses a Sallen-Key filter circuit with a cut-off frequency of half the sampling rate.

3. Software design

3.1 Function definition and the workflow

Software design is also part of embedded development. The software structure includes DDS generator module, SPI driver and ADC data buffer module, instruction interaction module, signal processing module, execution control module and exception information processing module. The first two implement the input and output of the signal. The instruction interaction module provides a host computer interaction interface and abstracts the instructions into an enumerated type. The signal processing module is responsible for extracting the required information such as harmonics and optical power. The last two control the execution of other modules. The workflow is shown in figure 7.

Figure 6. main software workflow

Figure 7. Locking steps
Figure 6 shows the execution flow of each loop. The execution process has modular features that facilitate collaborative development and post-maintenance. The image on the right shows the workflow for locking the work point after the initial power-on. The sweeping refers to sweeping the entire bias range when no pilot is applied, and recording the average optical power curve. Its role is to determine the approximate working point location information and speed up the next locking process.

3.2 DDS design built in MCU
The pilot signals required are generated by DDS. DDS is short for direct digital frequency synthesis. Conventionally, a frequency generating circuit using a crystal oscillator has a high frequency accuracy, but usually a low frequency such as 1 kHz cannot be generated directly. Most modulator bias controllers are designed using the Venturi bridge method, which is essentially the principle of RC oscillation and has poor frequency accuracy [9]. DDS can generate the signal of wide range frequencies and cover the required range [10]. At the same time, its initial clock comes from the crystal oscillator circuit, so the frequency accuracy is consistent with the crystal oscillator. This design uses the internal clock source of the MCU and a programmable timer to obtain the reference clock. Unlike the classic DDS, our design does not design a phase accumulator, but uses the original waveform table to generate waveform data at different frequencies available for DAC. Although this approach takes up more storage space, the benefits outweigh the disadvantages. Combined with the internal DMA resources of the MCU, the data refresh work is completely taken over by the DMA manager, and does not occupy any processing time of the main CPU, so the program execution efficiency is higher.

4. Test and analysis
The designed MZ modulator bias controller is implemented in a laboratory environment. In order to facilitate debugging, the component package and spacing are large, and the whole board size is 5*7mm. In fact, the hardware circuit design is relatively compact. If the board is redesigned for production, the board size is expected to be reduced by half. Figure 8 and figure 9 show the designed board and the modulator under test.

The designed bias control and the actual light modulator are also coordinated. The light source uses a 1550 nm laser. The modulator used in the test was the Fujitsu FTM7927, a 10 GHz single-arm fiber intensity modulator. The test used an external 1:99 fiber coupler and a photodiode produced by Beijing Minguang Technology Co., Ltd. to detect the optical power. The main path of the modulator output is connected to an optical power meter to monitor the working point. Under the same conditions, it is compared with the bias controller produced by PlugTech Co., Ltd. as comparison, which also uses the pilot method.

It can be seen from table 1 that two bias controllers both have achieved close extinction ratio under almost identical conditions. However, thanks to the advancement of the sweeping process, the modulator
bias control proposed in this paper takes less time to lock. Simultaneously, the pilot frequency of this design can be flexibly adjusted in a wide range, so the applicable scene is extended.

| Test Item                  | Proposed bias controller | PlugTech bias controller |
|----------------------------|--------------------------|--------------------------|
| Pilot frequency            | 1.5 kHz                  | 1 kHz                    |
| Dither amplitude           | 0.1% Vπ at Peak/Null, 2% Vπ at Q+/Q- |                        |
| Optical Power at peak point| -2.75 dBm                | -2.75 dBm                |
| Optical Power at null point| -29.80 dBm               | -30.25 dBm               |
| Optical Power at Q+/Q-     | -5.75 dBm                | -5.75 dBm                |
| Extinction Ratio           | 27.05 dB                 | 27.5 dB                  |
| locking time for peak/null point | 8 s                     | 12 s                     |
| locking time for Q+/Q- point | 20 s                    | 30 s                     |

5. Summary
The paper describes the design of an MZ modulator bias controller. The design applies the pilot method to achieve a feedback loop to check the working point. On the hardware, an optical power detection circuit is built. A bias signal output conditioning circuit that meets the requirements is also constructed. Finally, relying on the STM32F4 microprocessor signal analysis and control are realized digitally. This design innovatively applies DDS as a pilot signal generator, which makes the signal amplitude frequency arbitrarily programmable, which improves the flexibility of the system and reduces the complexity of the circuit. The design also uses a method of scanning the approximate working point, thus significantly optimizing the speed of the lock. Finally, this paper compares the designed bias controller. The system performance of this design is better than the current commercial modulator bias controller. In summary, the proposed bias controller has great engineering practical significance.

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