A Dual-Mode Control Scheme to Improve Light Load Efficiency for Active-Clamp Flyback Converter

Thanh Nhat Trung Tran 1, Hung-Chia Wang 2 and Jian-Min Wang 2,*

1 Department of Power Mechanical Engineering, National Formosa University, No. 64, Wunhua Rd., Huwei Township, Yunlin County 632, Taiwan; trungtranspk@gmail.com
2 Department of Vehicle Engineering, National Formosa University, No. 64, Wunhua Rd., Huwei Township, Yunlin County 632, Taiwan; 10758103@gm.nfu.edu.tw
* Correspondence: jmw@nfu.edu.tw; Tel.: +886-5-631-5692

Abstract: A novel dual-mode control scheme is proposed in this paper that permits the active-clamp flyback (ACF) converter to operate in both the quasi-resonant (QR) mode under light load and the active-clamp mode under medium or heavy load. The mode transition is performed based on the external dual-mode control circuit. In addition, the proposed converter incorporates a new QR mode valley switching (VS) control circuit that reduces switching loss in the main switch by achieving VS. Under medium to full load, the proposed converter becomes an ACF converter designed to achieve zero-voltage switching (ZVS), which reduces switching losses in both power switches. The proposed dual-mode control ACF converter has the following advantages: (1) compared with conventional ACF converters, the proposed ACF converters minimize switching losses by combining VS and ZVS; (2) under light load conditions, the frequency-limiting QR control mechanism is used to avoid disadvantageous switching losses caused by high switching frequencies. The 65 W ACF converter prototype with a DC 155 V input and a DC 19 V/3.42 A output under 65 kHz switching frequency was implemented. The experimental results demonstrate the feasibility of the proposed control scheme. The efficiency of the proposed converter reached 79% at a load of 3.5 W, which is 11% higher than the conventional ACF converter.

Keywords: active-clamp flyback; dual-mode control; light load; valley switching; zero-voltage switching

1. Introduction

The flyback converter architecture, as shown in Figure 1, extended from the buck-boost converter, is one of the most popular converters in the power electronics industry. This type of converter is characterized by its simple structure, few components, and easy compliance with electrical isolation safety specifications. Due to the fact of these advantages, flyback architecture is widely used in converters with output power levels less than 100 W such as light-emitting diode (LED) indoor lighting and portable chargers. However, in the transformer of the flyback converter, energy is stored in an air gap in the core. To store enough energy for the transformer, the size of the air gap must be increased with a corresponding increase in the leakage inductance of the transformer, resulting in a voltage spike on the switching device when it is turned off. The snubber circuit is a popular solution for suppressing this voltage spike; however, it lowers converter efficiency.

In recent years, numerous researchers have proposed efficiency improvements for flyback converters. Generally, these improvements can be classified into two major categories: constant-frequency control and variable-frequency control. In constant-frequency control, the active-clamp technique has been widely used in flyback converters. The ACF converter structure and key waveforms are presented in Figure 2a. In this technique, a circuit loop, comprising an auxiliary switch (Q2) and a capacitor (C_clamp), is added at the two terminals...
on the primary side of the transformer. This loop is used to perform ZVS at the main switch, improving converter efficiency and avoiding the high voltage spikes generated when the main switch is turned off [1–7]. However, conduction loss caused by resonant circulating current and additional switching in the \( Q_2 \) switch induces high power loss under light load [8]. Numerous studies [8,9] have described methods for addressing this drawback. Reference [8] employs a secondary-side post-regulator for minimizing power consumption. Consequently, this method requires an external post-regulator, resulting in a circuit with increased cost and size. In [9], a dual-mode control method was adopted in which the operation mode of the ACF converter was divided into two modes based on the load: the conventional flyback mode and the active-clamp mode. Briefly, the proposed converter works as a conventional flyback converter with the auxiliary switch turning off to decrease the converter’s switching and conduction losses under no-load conditions but turns into an ACF converter under normal-load/full-load conditions. However, this method is only effective for reducing the power consumption of the ACF converter under no-load conditions. In categories of variable-frequency control, quasi-resonant (QR) control is the mainstream technique [10–14]. The quasi-resonant flyback (QRF) converter structure and key waveforms are presented in Figure 2b. In the QR control technique, the resonance signal generated by the parasitic capacitance of the switch, \( C_{OSS} \), and the magnetizing inductance of the transformer, \( L_m \), are used to turn on the main switch when its drain-source voltage reaches a minimum valley point. Hence, switching loss is significantly reduced. However, this technique cannot achieve ZVS.

![Figure 1. Flyback converter topology.](image1)

![Figure 2. (a) Active-clamp flyback converter structure and key waveforms; (b) quasi-resonant flyback converter structure and key waveforms.](image2)
Thus, as summarized above, constant-frequency and variable-frequency control have advantages and disadvantages. By combining the advantages of ACF and QRF, a novel dual-mode control scheme combining ZVS and VS is proposed in this paper. Based on the structure of the ACF converter, in this dual-mode control scheme, an external logic circuit, called a dual-mode switching circuit, is integrated for switching the converter to the QR mode under light load adopting VS for the main switch to substantially reduce switching surges. However, the converter operating in the QR mode may cause high switching frequency and increased switching losses. Thus, the frequency-limiting QR control technology is combined to avoid the disadvantage of the increased switching frequency. This technique limits the maximum switching frequency during light load operation to allow the converter to achieve the frequency-limiting function. Under heavy load, the dual-mode switching circuit switches the converter back to the conventional ACF converter (active-clamp mode) to enable both power switches to achieve ZVS to obtain high efficiency.

2. Proposed Novel Dual-Mode ACF Converter Structure

2.1. The Proposed Circuit Structure and Principle of Operation

Figure 3 presents the block diagram of the proposed dual-mode control scheme and the related control sequence diagram under different load conditions. The control circuit consists of the current-mode controller UC3843 produced by STMicroelectronics (Geneva, Switzerland), a QR control circuit, and a dual-mode switching circuit. Among these components, the current mode controller UC3843 plays a critical role in stabilizing the output voltage. The QR control circuit and dual-mode switching circuit are the core circuits of the active-clamp and QR modes, respectively, as shown in Figure 3a. The working principle of the control circuit is explained in terms of two states: light load and heavy load.

2.1.1. Light Load

Under light load, the controller proposed in this paper controls the ACF converter operating in the QR mode, and the related control sequence diagram is illustrated in Figure 3b. In this case, the output signal \( V_C \) of the hysteresis comparator is low; thus, the high-side drive circuit is disabled, turning off the auxiliary switch \( Q_2 \) of the converter. At this moment, the feedback voltage signal \( V_{FB} \) at the converter output is then compared with the internal reference voltage of the feedback circuit to generate the error signal \( V_{Comp} \), which is sent to the current mode controller. The controller processes error signals and generates the control driving signal \( V_{PWM} \). Notably, the QR mode controller used in this paper has a mechanism to limit the maximum switching frequency, which is different from the conventional first VS method (as indicated by the red dashed circle in Figure 3b); this mechanism avoids disadvantageous switching losses due to the high switching frequencies.

2.1.2. Heavy Load

When the converter transitions from light to heavy load, the operation mode of the converter is switched from the QR mode to the active-clamp mode by the controller. Figure 3c depicts the related control sequence diagram. At this moment, the magnitude of the error signal \( V_{Comp} \) generated by the feedback circuit increases, simultaneously increasing the duty cycle of the drive signal \( V_{PWM} \) generated by the current mode controller. Due to the hysteresis comparator output signal \( V_C \) in this state being high, the high-side drive circuit is enabled. Consequently, the auxiliary switch of the ACF \( Q_2 \) is activated in accordance with the drive signal of \( V_{Q2} \). In other words, the driving signals \( V_{Q1} \) and \( V_{Q2} \) are complementary operation signals.
Figure 3. Cont.
2.2. The Control Circuit of the Proposed Novel Dual-Mode ACF Converter

This section describes the control circuit of the dual-mode ACF proposed in this paper.

2.2.1. Dual-Mode Switching Circuit

The gray block in Figure 4 is a dual-mode switching circuit. When the converter is operating under light load, the hysteresis comparator output ($V_C$) is low, since the output voltage of the current sensor ($V_{sense2}$) is less than the reference voltage ($V_{REF}$). Therefore, the drive signal ($V_{Q2}$) of the high-side auxiliary switch remains low. The input signal ($V_{pulse}$) of the second AND gate (AND2) determines the state of the valley trigger signal ($V_{reset}$) because the voltage signal ($V_C$) becomes high after the NOT gate. The valley trigger signal ($V_{reset}$) resets the main controller, which can precisely control the low-side main switch ($Q_1$) to achieve VS and to enable the converter to operate in the QR mode.

![Dual Mode Switching Circuit](image)

**Figure 4.** Dual-mode switching circuit structure.
When the converter is operating under heavy load, the hysteresis comparator output \( (V_C) \) is high; thus, the output state of the first AND gate (AND1) is determined by the voltage signal, \( V_{GS2} \). At this moment, the high-side auxiliary switch begins to operate. For the second AND gate (AND2), the output voltage signal \( (V_{reset}) \) is low since the signal \( (V_C) \) is high, and the main controller is not affected by the reset signal. In this stage, the QR control circuit is disabled, enabling the transition of the converter to the active-clamp mode.

2.2.2. Proposed QR Control Circuit

Before introducing the QR control technique proposed in this paper, the disadvantages of the conventional QRF converter are discussed. Conventional QR control methods rely on the phenomenon of resonance generated by the parasitic capacitance of the main switch and the magnetizing inductance of the transformer to turn on the main switch at the first resonance valley, which can reduce switching loss. However, as the output load increases, the switching frequency also increases, which leads to canceling out the advantages of VS as illustrated in Figure 5.

One popular solution to overcome these inadequacies is the use of a frequency-limiting mechanism. In this paper, a control technology similar to that in [13] is adopted in which only pulse signals are used to adjust the maximum frequency of the oscillator. The operating principle of the proposed converter is divided into two parts: the operating principle of the ACF converter operating in the QR mode and the operating principle of the QR control circuit that limits the maximum switching frequency.

- The operating principle of the ACF converter operating in the QR mode:

  The operating principle of the ACF converter in the QR mode is described as follows. This operation mode is divided into three states as shown in Figure 6, and the complete
key waveforms are presented in Figure 7. The following assumptions are used to simplify the analysis:

1. The main switch \((Q_1)\) and the auxiliary switch \((Q_2)\) have no leakage current and forward resistance;
2. The leakage inductance \((L_r)\) is negligible;
3. The parasitic capacitances, \(C_{oss1}\) and \(C_{oss2}\), are much smaller than \(C_{clamp}\);
4. Non-ideal characteristics, such as the forward voltage drop and the resistance effect of the secondary-side rectifier diode, are ignored;
5. The output capacitance is large enough to be considered as a constant voltage source;
6. The turn ratio \(n = N_p/N_s\).

Figure 6. (a–c) Three operating states of the ACF converter in the QR mode.

Figure 6. (a–c) Three operating states of the ACF converter in the QR mode.
The energy stored in the transformer is then transferred to the output capacitor and the parasitic capacitor (presented in Figure 6a. For the auxiliary winding on the secondary side of the transformer, the inductor current (presented in Figure 6a. For the auxiliary winding on the secondary side of the transformer, is in the resonant state due to the voltage output filter capacitor (transformer have opposite polarity, the output rectifier diode (Do) is reverse-biased. The input source begins to supply energy to the transformer, and the magnetizing time, the magnetizing inductance (Lm) increases linearly. Since the primary and secondary sides of the transformer have opposite polarity, the output rectifier diode (Do) is reverse-biased. The output energy is supplied by the output filter capacitor (Co). The detailed current path is presented in Figure 6a. For the auxiliary winding on the secondary side of the transformer, the voltage V_ZCD remains low because the voltage VS is less than zero.

State 1 (t₀ ≤ t < t₁):
When t = t₀, the main switch (Q₁) is turned on, and the auxiliary switch (Q₂) is turned off. The input source begins to supply energy to the transformer, and the magnetizing inductor current (Iₘ) increases linearly. Since the primary and secondary sides of the transformer have opposite polarity, the output rectifier diode (Dₒ) is reverse-biased. The output energy is supplied by the output filter capacitor (Cₒ). The detailed current path is presented in Figure 6a. For the auxiliary winding on the secondary side of the transformer, the voltage V_ZCD remains low because the voltage VS is less than zero.

State 2 (t₁ ≤ t < t₂):
When t = t₁, the main switch (Q₁) and the auxiliary switch (Q₂) are turned off. At this time, the magnetizing inductance (L_m) then begins to charge the parasitic capacitor (Cₚₛₜ₁) of the main switch (Q₁). As a result, the drain-source voltage (V_DS) of Q₁ on the primary side of the transformer increases rapidly. When V_DS ≥ V_in + nVₒ, the diode, Dₒ, conducts. The energy stored in the transformer is then transferred to the output capacitor and the output load. The detailed current path is shown in Figure 6b. For the auxiliary winding on the secondary side of the transformer, the voltage V_ZCD changes from low to high due to the transient transition of V_s. 

State 3 (t₂ ≤ t < t₃):
When t = t₂, the energy stored in the transformer has been completely transferred to the secondary side, and the current I_Dₒ decreases to zero. The converter is thus operating in the discontinuous conduction mode (DCM). The magnetizing inductor (L_m) and the parasitic capacitor (Cₚₛₜ₁) begin to resonate. The detailed current path is shown in Figure 6c. In the QR mode, when the voltage drops to the valley, the main switch (Q₁) turns on to reduce switching loss. At this time, the output energy is provided to the load by the output load.
filter capacitor ($C_o$). The auxiliary winding on the secondary side of the transformer is in the resonant state due to the voltage $V_s$, resulting in a square wave signal at the output of the comparator with the same resonant frequency.

- The operating principle of the QR control circuit with the maximum switching frequency-limiting function:

This section explains the operating principle of the QR control circuit with the maximum switching frequency-limiting function. Figure 8 depicts the QR control block with the maximum switching frequency-limiting function and related key waveforms. Notably, the circuit only operates when the ACF converter is in the resonant state. When voltage $V_{DS1}$ resonates through point 0 at $t_0$, the voltage $V_{ZCD}$ transientsly changes from high to low. After being processed by the RC delay circuit, the voltage $V_{ZCD1}$ will be delayed for a period $\Delta t$. The falling edge of this square wave may coincide with the valley of the switching voltage $V_{DS}$. Therefore, the pulse generator and the gain controller can generate an adjustable pulse signal $V_{pulse1}$ at time $t_1$. To control the maximum switching frequency limit, the original oscillator signal ($V_{OSC}$) must be obtained from the current mode controller. After processing by the squarer, this signal becomes a triangular signal at the same frequency, $V_{OSC1}$. This method is used to accentuate the peak voltage of $V_{OSC}$. The multiplier is the main focus of this control strategy. The input voltages of the multiplier are $V_{OSC1}$ and $V_{pulse1}$; thus, the peak value of the output voltage $V_{pulse2}$ gradually increases. Finally, the voltage $V_{sum}$ is generated by adding $V_{OSC}$ to $V_{pulse2}$. As the number of resonances increases, the peak value of $V_{sum}$ also increases. When the voltage value of $V_{sum}$ is higher than the reference voltage $V_{TH}$ of comparator CMP1 at $t_2$, the output signal $V_{reset}$ of CMP1 triggers the current mode controller to reset the oscillator. This technique enables the converter to achieve maximum switching frequency limiting. Thus, controlling the magnitude of the reference voltage $V_{TH}$ determines the valley point of the converter.

![Current Mode Controller](image)

**Figure 8.** Cont.
Figure 8. (a) QR control block with the maximum switching frequency-limiting function and (b) key waveform sequence diagram.

3. Design of the Proposed Novel Dual-Mode ACF Converter

The converter structure and operating principles have been described in detail in the previous section. This section describes the design of the proposed dual-mode ACF converter. A 65 W power supply is used in the following example calculations and the description of the component design of the converter. The specifications of the prototype converter are listed in Table 1.

In the following, the design procedure of the converter is briefly presented.

Step 1:
Given that the maximum output power $P_{o,\text{max}} = 65$ W and the efficiency $\eta = 0.9$, the magnetizing inductance ($L_m$) of the transformer can be determined [15]:

$$L_m = \frac{\eta \times (V_{\text{in,min}} \times D_{\text{max}})^2}{2 \times f_{\text{sw}} \times P_{o,\text{max}}} = 409 \, \mu\text{H} \quad (1)$$
Table 1. Specifications of the proposed ACF converter.

| Parameters            | Value     |
|-----------------------|-----------|
| Input voltage, $V_{in}$ | 155 V     |
| Maximum output power, $P_{o,max}$ | 65 W     |
| Output voltage, $V_{out}$ | 19 V     |
| Output current, $I_{out}$ | 3.42 A  |
| Switching frequency, $f_{sw}$ | 65 kHz |
| Maximum duty cycle, $D_{max}$ | 0.4 |
| Efficiency, $\eta$ | 90%        |
| Maximum magnetic flux density, $B_{max}$ | 2000 G  |

Step 2:
After the magnetizing inductance ($L_m$) of the transformer is known, the peak current of the transformer primary side winding can be calculated:

$$I_{pp} = \frac{P_{o,max}}{\eta \times V_{in} \times D_{max}} + \frac{V_{in,min} \times D_{max}}{2 \times L_m \times f_{sw}} \approx 2.357 \text{ A} \quad (2)$$

Step 3:
The maximum output power ($P_{o,max}$) of the converter is 65 W, and the switching frequency is 65 kHz. In this paper, the PQ26/20 iron core produced by TDK (Tokyo, Japan) was used to calculate the primary winding turns of the transformer. Based on the actual design considerations, the magnetizing inductance ($L_m$) is 400 $\mu$H. From the core datasheet, the effective cross-sectional area of the core ($A_e$) is 1.19 cm, and the maximum magnetic flux density ($B_{max}$) is 2000 G. The primary winding turns of the transformer ($N_p$) can be calculated as follows:

$$N_p = \frac{L_m \times I_{pp}}{A_e \times B_{max}} \times 10^8 \approx 39 \quad (3)$$

Step 4:
The secondary winding turns ($N_s$) can also be calculated:

$$N_s = \frac{V_o \times (1 - D_{max}) \times N_p}{V_{in} \times D_{max}} \approx 7 \quad (4)$$

Step 5:
The output diode must be selected considering the maximum output current and the withstand voltage. The withstand voltage and withstand current of the diode are calculated as follows:

$$V_{D,max} = \frac{V_{in,max}}{N_p} + V_o \approx 46.82 \text{ V} \quad (5)$$

$$I_{sec,peak} = I_{L,peak} \times n \approx 13.22 \text{ A} \quad (6)$$

$$I_{sec,rms} = I_{sec,peak} \sqrt{\frac{1 - D_{max}}{3}} \approx 5.912 \text{ A} \quad (7)$$

In accordance with the results of Equations (5)–(7), the ultrafast rectifier diode BYV32E-150 produced by NXP Semiconductors (Eindhoven, Netherlands) was selected as the output rectifier diode with a peak reverse voltage of 150 V and a peak forward current of 20 A.

Step 6:
To achieve ZVS for the ACF converter power switch, enough energy must be stored in the resonant inductance ($L_r$) to completely discharge the parasitic capacitance ($C_r$) of the power switch; the calculations of this energy are as follows:

$$E_{Lr} \geq E_{Cr} \quad (8)$$

$$(I_{pp})^2 \times L_r \geq C_r \times (V_{in} + n \times V_o)^2 \quad (9)$$
where $E_L$ and $E_C$ are resonant inductance energy and parasitic capacitance energy, respectively.

Step 7:
After the resonant inductance has been determined, the appropriate value of the clamping capacitor ($C_{\text{clamp}}$) can be calculated as follows:

$$C_{\text{clamp}} = \frac{(1 - D_{\text{max}})^2}{\pi^2 \times L_r \times f_{\text{sw}}}$$

(10)

4. Experimental Results

In this experiment, the control IC UC3843 was used as the main controller. The proposed dual-mode ACF converter had the following specifications: the input voltage was 155 VDC, the output voltage was 19 VDC, and the maximum output power was 65 W. The experimental data included the measured critical switching waveforms, control signal waveforms, dual-mode switching waveforms, ZVS waveforms, and other key parameters. Finally, the comparison of efficiency between the conventional ACF converter and the proposed dual-mode ACF converter is presented in this section. The slope shape of the oscillator waveform is critical for the control technique proposed in this paper, because more precise slope changes result in more accurate VS. Generally, the traditional oscillator is an RC circuit; thus, the slightly curved slope causes the failure of frequency-limited VS. To overcome this challenge, a squarer was used to convert the oscillator waveform into a triangular waveform with a linear slope, improving the accuracy of VS. The relevant waveform is presented in Figure 9.

![Figure 9. Oscillator waveform with (Ch4) and without (Ch3) the frequency-limiting control mechanism.](image)

Figure 10a shows that when the voltage $V_{\text{DS1}}$ voltage starts to resonate generating a valley, a voltage pulse signal is generated. Through the multiplier, a linearly rising voltage pulse signal $V_{\text{pulse2}}$ is then generated. Next, the oscillating voltage signal $V_{\text{OSC}}$ and the voltage signal $V_{\text{pulse2}}$ are added by the adder to generate the voltage signal $V_{\text{sum}}$. Finally, the voltage signal $V_{\text{sum}}$ is compared with the reference voltage $V_{\text{TH}}$ to generate a reset voltage signal $V_{\text{reset}}$, which restarts the control IC UC3843 to complete the frequency-limiting VS as shown in Figure 10b. In other words, the voltage level of the reference voltage $V_{\text{TH}}$ determines the VS point, and higher $V_{\text{TH}}$ values cause a slower system switching frequency. Conversely, lower $V_{\text{TH}}$ causes a faster system switching frequency.
Figure 10. (a) Power switch voltage waveform and its generated signal waveforms; (b) key control signal waveforms of the proposed ACF converter in QR mode.

Figure 11 presents the key voltage waveforms of the converter operating at different output powers. If the converter operates was at an output power of 6.5 W, the switching frequency of the converter was approximately 70 kHz as presented in Figure 11a. For an output power of 19.5 W, the switching frequency of the converter decreased to approximately 68 kHz as presented in Figure 11b. Although the output power of the converter varied, the switching frequency of the circuit can be limited within a fixed range by the frequency-limiting QR control function of the QR control circuit proposed in this paper. If the output power increased above 19.5 W, the converter changed the operation mode from the QR to the active-clamp mode as presented in Figure 12. Figure 13 shows the ZVS waveforms of the power switches of the proposed converter. The figure shows that before the main switch \((Q_1)\) was turned on, the drain-source voltage of the main switch \(V_{\text{DS1}}\) decreased to zero. The same principle was applied to the auxiliary switch \((Q_2)\); thus, both power switches achieved ZVS.

Figure 11. Key voltage waveforms of the proposed ACF converter operating at (a) 6.5 W and (b) 19.5 W. The converter is in the QR mode.

Figure 14 presents the key waveforms for switching between the two modes of the converter according to the change in output power when the input voltage \(V_{\text{in}} = 155\) VDC. If the output power was 6.5 W, the driving signal \(V_{\text{GS2}}\) of the auxiliary switch \((Q_2)\) was off, and the driving signal \(V_{\text{GS1}}\) of the main switch \((Q_1)\) adjusted the pulse width modulation in accordance with the load. At this time, the converter operated in the QR mode. If the
output power increased from 6.5 to 65 W, the drive signal $V_{GS2}$ of the auxiliary switch ($Q_2$) entered a working state, and the main switch ($Q_1$) and the auxiliary switch ($Q_2$) operated in a complementary manner to enable the converter to operate in the active-clamp mode as presented in Figure 14a. By contrast, if the output power decreased from 65 to 6.5 W, the driving signal $V_{GS2}$ of the auxiliary switch ($Q_2$) changed from the working state to the off state, and the operation mode of the converter changed from the active-clamp mode to the QR mode as shown in Figure 14b. These experimental data demonstrated that the converter proposed in this paper can switch between the two modes.

![Figure 12](image12.png)

**Figure 12.** Waveforms of the main switch and auxiliary switch of the proposed ACF converter under medium- to full-load conditions (above 19.5 W). The converter is in the active-clamp mode.

![Figure 13](image13.png)

**Figure 13.** ZVS waveforms of the power switches of the proposed ACF converter in the active-clamp mode.
Table 2 presents the efficiency measurement data for the dual-mode ACF converter. In the table, input current, output current, output voltage, and efficiency are presented under different load conditions with a voltage of 155 VDC as the input power supply. Figure 15 provides a comparison of the efficiency curves of the conventional ACF converter and the dual-mode ACF converter at different output power levels. The curve comparison diagram reveals that for an output power of 3.5 W, the efficiency difference between the two converters is at a maximum of 11%. If the output load increases, conduction losses gradually increase; thus, the efficiency difference between the two converters decreases. Table 2 and Figure 15 show that the control technique proposed in this paper has good performance under light load conditions. In addition, Table 3 presents the load regulation measurement data. Based on the measurement results, it can be seen that the minimum load regulation value is 1.09% at the output power of 65 W (i.e., full load).

**Table 2. Efficiency of the proposed dual-mode ACF converter.**

| Input Voltage, $V_{\text{in}}$ | Input Current, $I_{\text{in}}$ | Output Voltage, $V_o$ | Output Current, $I_o$ | Efficiency, $\eta$ |
|-------------------------------|-------------------------------|-----------------------|-----------------------|-------------------|
| 155 V                         | 0.030 A                       | 19.3 V                | 0.19 A                | 79%               |
| 155 V                         | 0.052 A                       | 19.3 V                | 0.34 A                | 82.5%             |
| 155 V                         | 0.075 A                       | 19.3 V                | 0.51 A                | 84.6%             |
| 155 V                         | 0.098 A                       | 19.3 V                | 0.68 A                | 85.7%             |
| 155 V                         | 0.119 A                       | 19.3 V                | 0.84 A                | 87.5%             |
| 155 V                         | 0.229 A                       | 19.2 V                | 1.67 A                | 90.3%             |
| 155 V                         | 0.349 A                       | 19.2 V                | 2.55 A                | 90.6%             |
| 155 V                         | 0.464 A                       | 19.2 V                | 3.41 A                | 90.7%             |

**Table 3. Load regulation measurement data of the proposed dual-mode ACF converter.**

| Output Power, $P_o$ | Output Voltage, $V_o$ | Load Regulation, $LR$ |
|---------------------|-----------------------|-----------------------|
| 3.5 W               | 19.289 V              | 1.52%                 |
| 6.5 W               | 19.303 V              | 1.59%                 |
| 13.0 W              | 19.304 V              | 1.60%                 |
| 19.5 W              | 19.305 V              | 1.61%                 |
| 26.0 W              | 19.293 V              | 1.54%                 |
| 32.5 W              | 19.258 V              | 1.36%                 |
Table 3. Cont.

| Output Power, $P_o$ | Output Voltage, $V_o$ | Load Regulation, $LR$ |
|---------------------|-----------------------|-----------------------|
| 39.0 W              | 19.236 V              | 1.24%                 |
| 45.5 W              | 19.226 V              | 1.19%                 |
| 52.0 W              | 19.227 V              | 1.19%                 |
| 58.5 W              | 19.222 V              | 1.17%                 |
| 65.0 W              | 19.207 V              | 1.09%                 |

Efficiency

Figure 15. Efficiency curves of the conventional ACF converter and dual-mode ACF converters at different output powers.

5. Conclusions

This paper presented a new dual-mode switching control strategy for the ACF converter working in DCM, which can switch to the QR mode at light loads to improve overall efficiency. This paper proposed a new dual-mode switching control strategy for an ACF converter operating in DCM to enable operation in the QR mode under light load to optimize the overall operation. The control techniques and operating principles were described in detail. The operating principles and the results of an analysis of the control techniques were carefully discussed. A prototype of the 65 W dual-mode ACF converter was developed, and experiments provided satisfactory results. Experimental results revealed that the auxiliary switch of the resonant tank closed when the dual-mode ACF converter was under light load, which enabled the main switch to perform VS and achieve QR mode control. On the contrary, the converter operated in the active-clamp mode under medium and heavy load conditions, thereby achieving ZVS for both power switches to maintain the high efficiency of conventional ACF. In other words, the proposed dual-mode ACF converter uses QR mode VS characteristics to improve the poor efficiency of conventional ACF under light load. However, the switching frequency of the QR mode is critical to determining the light load efficiency. In general, it is recommended to design the QR mode switching frequency as close to the active-clamp mode switching frequency as possible, because excessively high switching frequencies increase switching losses at light loads. This proposed dual-mode control ACF topology is suitable for applications with relatively low power consumption (under 200 W).

Author Contributions: Conceptualization, J.-M.W. and T.N.T.T.; methodology, H.-C.W. and J.-M.W.; validation, T.N.T.T., H.-C.W. and J.-M.W.; resources, J.-M.W.; writing—original draft preparation, J.-M.W. and T.N.T.T.; writing—review and editing, J.-M.W. and T.N.T.T. All authors have read and agreed to the published version of the manuscript.
**Funding:** This research was funded by the Ministry of Science and Technology, R.O.C. (grant number: MOST 110-2622-E-150-002).

**Data Availability Statement:** Not applicable.

**Conflicts of Interest:** The authors declare no conflict of interest.

**References**

1. Watson, R.; Hua, G.C.; Lee, F.C. Characterization of an active clamp flyback topology for power factor correction applications. *IEEE Trans. Power Electron.* 1996, 11, 191–198. [CrossRef]

2. Watson, R.; Lee, F.C.; Hua, G.C. Utilization of an active-clamp circuit to achieve soft switching in flyback converters. *IEEE Trans. Power Electron.* 1996, 11, 162–169. [CrossRef]

3. Papanikolaou, N.P.; Tatakis, E.C. Active voltage clamp in flyback converters operating in CCM mode under wide load variation. *IEEE Trans. Power Electron.* 2004, 51, 632–640. [CrossRef]

4. Liu, P.-H. Design consideration of active clamp flyback converter with highly nonlinear junction capacitance. In Proceedings of the 2018 Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018; pp. 783–790.

5. Wu, S.-T.; Cheng, Y.-T. Design and Implementation of a Single-Stage PFC Active-Clamp Flyback Converter with Dual Transformers. *Electronics* 2021, 10, 2588. [CrossRef]

6. Leng, C.-M.; Chiu, H.J. Three-Output Flyback Converter with Synchronous Rectification for Improving Cross-Regulation and Efficiency. *Electronics* 2021, 10, 430. [CrossRef]

7. Medina-Garcia, A.; Schlenk, M.; Morales, D.P.; Rodriguez, N. Resonant Hybrid Flyback, a New Topology for High Density Power Adaptors. *Electronics* 2018, 7, 363. [CrossRef]

8. Jung, J.; Ahmed, S. Flyback converter with novel active clamp control and secondary side post regulator for low standby power consumption under high-efficiency operation. *IET Power Electron.* 2011, 4, 1058–1067. [CrossRef]

9. Kim, J.h.; Ryu, M.-H.; Min, B.d.; Song, E.-H. A Method to Reduce Power Consumption of Active-Clamped Flyback Converter at No-Load Condition. In Proceedings of the IECICON 2006—32nd Annual Conference on IEEE Industrial Electronics, Paris, France, 6–10 November 2006; pp. 2811–2814.

10. Wang, C.; Xu, S.; Shen, W.D.; Lu, S.I.; Sun, W.F. A Single-Switched High-Switching-Frequency Quasi-Resonant Flyback Converter. *IEEE Trans. Power Electron.* 2019, 34, 8775–8786. [CrossRef]

11. Li, J.T.; van Horck, F.B.M.; Daniel, B.J.; Bergveld, H.J. A High-Switching-Frequency Flyback Converter in Resonant Mode. *IEEE Trans. Power Electron.* 2017, 32, 8582–8592. [CrossRef]

12. Park, H.P.; Jung, J.H. Design Methodology of Quasi-Resonant Flyback Converter With a Divided Resonant Capacitor. *IEEE Trans. Power Electron.* 2021, 68, 10796–10805. [CrossRef]

13. Wang, J.; Lin, C.-W.; Huang, K.-Y.; Wong, J.-S. The Novel Quasi-Resonant Flyback Converter With Autoregulated Structure for Parallel/Serial Input. *IEEE Trans. Power Electron.* 2020, 67, 992–1004. [CrossRef]

14. Jeng, S.-L.; Peng, M.T.L.; Hsu, C.Y.; Chieng, W.H.; Shu, J.P.H. Quasi-resonant flyback DC/DC converter using GaN power transistors. *World Electr. Veh. J.* 2012, 5, 567–573. [CrossRef]

15. Pressman, A.I. *Switching Power Supply Design*; McGraw-Hill: New York, NY, USA, 1998.