Removal of Side-gating Effects in GaAs Quantum Nanodevices with Nano-Schottky Gates by Surface Passivation Using Si Interface Control Layer∗

Rui Jia,† Nanako Shiozaki, Seiya Kasai, and Hideki Hasegawa
Research Center for Integrated Quantum Electronics (RCIQE) and Graduate School of Information Science and Technology, Hokkaido University, North-13, West-8, Sapporo 060-8628, Japan
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For ultra-high-density integration ofgate-controlled quantum devices, one possible phenomenon limiting the ultimate integration density is a side-gating effect which has not been properly addressed so far for nanodevices. The purpose of this paper is to attempt to remove the side-gating effect from the GaAs quantum wire transistors where we recently have found presence of anomalously large side-gating effect. We first present data on the side-gating and we explain its mechanism in terms of tunneling injection of electrons by field concentration at gate edges caused by Fermi level pinning. Then, we apply our Si interface control layer (Si ICL) passivation process to reduce the pinning. By applying the Si ICL technique via thin GaAs cap layer, the anomalously large side-gating was completely suppressed, and only electrostatic side-gating theoretically expected from the device structure remained.

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I. INTRODUCTION

The Si CMOS technology has been continuously making progress, following the Moore’s law, up to date mainly by the aggressive reduction of device feature sizes. Owing to this, various electronic systems including computers have been realized, and their performances have been improved. However, it is anticipated now that the scaling limit of the Si CMOS technology is likely to come in the near future.

In order to continue the development of electronics and information technology, extensive research is currently being made on Si on insulator (SOI)-based, III-V-based and carbon nanotube-based nanodevices as candidates [1] for future high-density, high-speed and low-power LSIs beyond the scaling limit of the Si CMOS LSIs. Particularly, quantum nanodevices seem to very promising, because the size of the quantum nanodevices is essentially small, and because dissipative quantum switches such as single electron transistors (SETs) and quantum wire transistors (QWRTrs) can operate near the quantum limit of power-delay product (PDP) [2]. To realize ultra-high density and ultra-low power consumption quantum (Q-) LSIs in a realistic way, our group has recently proposed a hexagonal binary decision diagram (BDD) quantum circuit approach [3, 4], where the BDD logic architecture is implemented utilizing closely packed hexagonal III-V semiconductor nanowire networks controlled by nano-Schottky wrap gates (WPGs).

However, for high-density integration of III-V gated quantum nanodevices, one critical issue that has not been addressed so far is the side-gating effect related to the device isolation. This is a phenomenon that the current in one device is unintentionally modulated by gates of another nearby devices. It is known that the side-gating effect limits the achievable integration density for classical LSIs based on Si-based and III-V based FETs. However, side-gating behavior in the quantum nanodevices controlling a single or a few electrons for digital processing has never been investigated so far. In this connection, we have recently found that GaAs QWR FETs show anomalously large device interference [5].

The purpose of this paper is to attempt to remove the anomalously large side-gating behavior observed in GaAs quantum wire transistors (QWRTrs) having nanometer-scale Schottky wrap gate (WPGs) by our surface passivation technique based on Si interface control layer (Si-ICL) [6] for future realization of ultra-high density hexagonal BDD quantum LSIs.

II. EXPERIMENTAL

The device structure of the GaAs QWRTr with a nanometer-scale Schottky WPG used in this study is schematically shown in Fig. 1(a). A nanometer scale Schottky side-gate is placed with a distance, $d_{sg}$, from the edge of the nanowire of the QWRTr. The devices were fabricated on an AlGaAs/GaAs HEMT wafer whose structure is shown in Fig. 1(b). The nanowires were formed by electron beam (EB) lithography and wet chemical etching by etching the wafer to a depth of $t_e = 95$ nm to the bottom AlGaAs surface. The typical nanowire width, $W$, was 300-500 nm at the mesa top. After the formation of ohmic contacts for source and drain electrodes, a nanometer scale WPG electrode with $L_G = 170 - 250$ nm and a side gate electrode having the same gate length were formed by EB lithography, vacuum deposition of Cr/Au metals and lift-off process. An example of a plan view SEM image of a fabricated device is shown in Fig. 1(c).

The important parameter for the side-gating study is the side gate-to-nanowire distance, $d_{sg}$. For high-density integration, it is desirable to have smaller values of $d_{sg}$. However, this is limited by the onset of side-gating which cause serious device interference. In this study, the value of $d_{sg}$ was changed from 200 nm to 1,000 nm.

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†Corresponding author: jiarui@rciqe.hokudai.ac.jp
investigated in this study to remove the side-gating effect is schematically shown in Fig. 2. The details of the Si ICL passivation process has been published elsewhere [6]. Such a process has recently realized large increase of photoluminescence intensity from the GaAs quantum wires [7] similar to those used in this study. In the present study, Si ICL is formed on a regrown thin GaAs cap layer, as seen in Fig. 2. During device fabrication, this surface passivation process was applied to the unfinished device structure in an ultra-high vacuum (UHV) multi-chamber system which includes MBE, X-ray Photoelectron Spectroscopy (XPS), ECR CVD chamber and others. Namely, the AlGaAs/GaAs/AlGaAs samples after formation of nanowires by wet etching to a depth of \( t_e = 95 \) nm reveal the bottom AlGaAs surface was put into the MBE chamber. After thermal cleaning of the surface, a thin cap layer of 5 nm GaAs was regrown. Subsequently, 1 nm Si ICL was grown on top of the regrown GaAs at substrate temperature \( T_{sub} = 300°C \). After the Si ICL growth, the partial nitridation of Si ICL by nitrogen radicals was performed without breaking UHV. Finally, 30 nm SiO\(_2\) was deposited on the sample by a standard CVD process. For comparison, the samples without any passivation (bare surface), with only GaAs cap layer, with only Si ICL without GaAs cap were also prepared, respectively.

Electrical characteristics of the fabricated devices were measured using an Agilent 4156A semiconductor parameter analyzer. The measurements were carried out from room temperature (RT) to 100 K using cryostats. All the measurements were performed in the dark condition.

III. RESULTS AND DISCUSSION

A. Side-gating effect in QWRTrs and its mechanism

1. Dependence of side-gating on \( d_{sg}\)

All the fabricated devices showed good gate control characteristics as shown in Fig. 3(a). However, by applying negative side-gate voltage, \( V_{sg}\), the drain current exhibited substantial decreases as shown in Fig. 3(b), showing strong modulation of current by a far away side gate. A plot of the drain current vs. the side gate voltage, \( V_{sg}\), at a constant main gate voltage is shown in Fig. 4. It is seen that the side gate can control the drain current down to complete pinch-off like the main gate in spite of the fact that it lies far away.

At low temperature fabricated devices showed clear conductance quantization, as shown in Fig. 5. However, the voltage corresponding to conductance step showed shifts with the application of \( V_{sg}\). Namely, a large side-gating effect can take place even in the quantum regime where a very small current was controlled by a small volt-
FIG. 3: Examples of $I_{DS} - V_{DS}$ curves without and with side-gate voltages at room temperature: (a) $V_{sg} = 0 \text{ V}$ and (b) $V_{sg} = -1 \text{ V}$.

age in the device. Since the experiments indicated that the mechanism causing side-gating is common to the classical regime and the quantum regime. All the following measurements were carried out in the classical field effect transistor mode.

In order to summarize the side-gating behavior more systematically with the change of $d_{sg}$, the side-gate transconductance, $g_{msg}$, was defined by the following formula.

$$g_{msg} = \frac{dI_{DS}}{dV_{sg}} \quad (V_G, V_{DS} = \text{const}),$$

where $I_{DS}, V_{DS},$ and $V_G$ are the drain current, drain voltage and gate voltage, respectively. The strong side-gating should obviously result in a large value of $g_{msg}$. Figure 6 summarizes the values of side-gate transconductance evaluated from the measured $I_{DS} - V_{sg}$ curves at RT. It is seen in Fig. 6 that the side-gating behaves very differently, depending on the value of $d_{sg}$. Namely, when $d_{sg}$ was larger than 500 nm, the effect was weak and its $d_{sg}$-dependence was small. For convenience, let us call this region as Region A. On the other hand, when $d_{sg}$ was smaller than 500 nm, $g_{msg}$ increased rapidly with decrease of $d_{sg}$, leading to anomalously large side-gating effect. The region where the strong side-gating takes place is called in this paper as Region B.

In addition, in order to see the effect of gate length, we fabricate a device with $L_G = 4000 \text{ nm}$ having $d_{sg} = 500 \text{ nm}$ and $t_e = 95 \text{ nm}$, with its SEM image and $I_{DS} - V_{sg}$ curve as shown in Fig. 7(a) and Fig. 7(b), respectively. In this device, no large side-gating effect was observed. Therefore, the large side-gating effect in Region B is an unique phenomenon in nanometer-size WPG devices, and it is a very serious effect against large-scale integration of the present GaAs QWRTrs.

FIG. 4: $d_{sg}$ dependences of $I_{DS} - V_{SG}$ curves for devices with $t_e = 95 \text{ nm}$.

FIG. 5: At low temperature, the QWRTr’s conductance quantization shifts with the application of side gate voltage.
2. Mechanism of the side-gating

Since the side-gate locates very close to the nanowire, one possible mechanism of the side-gating effect was electrostatic side-way depletion, where the depletion region extending from the side-gate reaches the nanowire region and it directly modulates the electron density in the nanowire. In order to see whether such an electrostatic model can explain the observed side-gating, a theoretical analysis based on potential simulation was performed by numerically solving two-dimensional Poisson’s equation. The result showed that the behavior of Region A can be explained by such a model, as indicated by a solid curve in Fig. 6 showing a result of theoretical simulation. However, the much more serious behavior in Region B is too large to be explained by such a model.

Another possibility is impact ionization and related carrier transport and trapping which are the main side-gating mechanisms in the classical GaAs FETs [8–11]. However, it is obvious that the operation voltage is too small to cause impact ionization in the present QWRTr devices.

In order to clarify the anomalously large side-gating effect in our QWRTrs, we have carried out a detailed analysis of device and side gate currents over a wide temperature range. The details of this investigation are beyond the scope of this paper, and will be presented elsewhere [12]. This effort has led to the following novel surface-related side-gating mechanism schematically shown in Fig. 8:

(1) Strong surface Fermi level pinning by surface states produces high electric field at the nanometer-scale side gate periphery.

(2) This causes lateral tunneling injection of electrons.

(3) The resultant leakage current causes charging and discharging of traps near the heterointerface of nanowire.

(4) This modulates the nanowire potential and causes side-gating.

This is a novel mechanism of side-gating applicable to nanodevices. It is perhaps not peculiar to GaAs nanodevices, but a general mechanism which can happen in any of above candidates for LSIs where field concentration in metal periphery takes place and where some kinds of deep levels exist.

B. Attempt to remove side-gating effect by Si ICL-based surface passivation

As already mentioned, elimination of the observed large side-gating effect is vitally necessary for large scale inte-
integration of our QWRTrs. Of course, one possible approach to eliminate this effect is to increase the mesa heights by deeper etching and to keep a long distance between nanowire and side-gate, namely, to increase the values of $t_e$ and $d_{sg}$. However, for the high-density integration of quantum nanodevices, it is quite necessary to realize smaller values of $t_e$ and $d_{sg}$.

On the other hand, the brief discussion given in the previous section indicates that the strong surface Fermi level pinning is responsible for the large side-gating effect. Thus, for removing it, the most essential way is to passivate the surface by a suitable passivation scheme which removes the strong surface Fermi level pinning.

Regarding this, it is well known that high density gap states tend to exist at surface and interfaces of III-V materials, and pin the Fermi level at charge neutral level, $E_{CNL}$. This adversely affects the performances of advanced electronic and optical devices. The problem will become severer as the devices feature sizes are reduced deep into the nanometer region [13]. From such a viewpoint, our group has proposed [14] and has been investigating the Si ICL-based surface passivation technique [6, 15]. Thus, we decided to apply this Si ICL technology for possible removal of the observed anomalously large side-gating effect.

Figure 9 shows $I_{DS} - V_{sg}$ curves for the samples with various surface passivation conditions related to the Si ICL passivation, including the one having both of a GaAs cap and Si ICL as shown in Fig. 2. Here, $t_e$ was kept to be 95 nm for all the samples. It was found that the side-gating effect was sensitive to the passivation. We can see that passivation by only the regrowth of 5 nm GaAs cap layer reduces passivation, but cannot totally eliminate the side-gating effect. On the other hand, the result of the passivation only with only Si ICL without a GaAs cap shows that it is remarkably effective in reducing the side-gating effect, but the side-gating effect still slightly remains. This may be because the etched AlGaAs surface contains a small amount of oxides and it is difficult to remove them completely. Thus, surface cleaning process of AlGaAs should be further optimized, if Si ICL is directly put on the air-exposed AlGaAs surface. On the other hand, it is obviously more desirable if the Si ICL is grown on the fresh epitaxial surface. Thus, by applying the Si ICL passivation onto the regrown thin GaAs cap layer, we could obtain a surprisingly large reduction of side-gating as seen in Fig. 9. The value of the side-gate transconductance value, $g_{msg}$, was also evaluated by using Eq. (1), and the result is shown in Fig. 10 together with the side-gate transconductance values without passivation shown in Fig. 6. From the comparison, it can be seen that even when $d_{sg}$ is smaller than 500 nm, $g_{msg}$ values in the Region B are remarkably reduced and they actually follow the theoretical curves by the electrostatic effect. Thus, the anomalous side-gating effect is completely suppressed, and only the electrostatic side-gating theoretically expected from the device structure remains.

From the above results, it could be concluded that surface states and defects play the important roles in inducing the large side-gating effect for QWRTrs having nano-Schottky gates. An appropriate surface passivation scheme such as application of Si ICL on to regrown thin cap GaAs layer is very effective to remove the anomalous side-gating for the QWRTrs.
IV. CONCLUSIONS

This paper discussed a hitherto unaddressed very critical issue for ultra-high-density integration of gate-controlled quantum nanodevices, namely the side-gating effect which may limit the ultimate integration density.

More specifically, an attempt was made to remove a side-gating effect from the GaAs quantum wire transistors where we recently have found presence of the anomalously large side-gating effect. We first presented data on the side-gating where small electrostatic side-gating effects as well as anomalously large side-gating effects were observed. We then explained the mechanism of the anomalous side-gating in terms of tunneling injection of electrons by field concentration at gate edges caused by Fermi level pinning. Finally, we applied our Si interface control layer (Si ICL) passivation process to reduce pinning. By applying the Si ICL technique via thin GaAs cap layer, the anomalously large side-gating was completely suppressed, and only electrostatic side-gating theoretically expected from the device structure remained.

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