Low-loss silicon nitride photonic ICs for single-photon applications

KIRILL A. BUZAVEV,1,2 ALEKSANDR S. BABURIN,1,2 EVGENY V. SERGEEV,1 SERGEY S. AVDEEV,1 EVGENY S. LOTKOV,1 MIHAEL ANDRONIK,1 VICTORIA E. STUKALOVA,1 DMITRY A. BAKLYKOV,1 IVAN V. DYAKONOV,3 NIKOLAY N. SKRYABIN,3 MIKHAIL YU. SAYGIN,3 SERGEY P. KULIK,3 ILYA A. RYZHIKOV,1 AND ILYA A. RODIONOV1,2,*

1FMN Laboratory, Bauman Moscow State Technical University, Moscow 105005, Russia
2Dukhov Research Institute of Automatics (VNIIA), Moscow 127055, Russia
3Quantum Technology Center, Faculty of Physics, Lomonosov Moscow State University, Moscow 119991, Russia
*irodionov@bmstu.ru

Abstract: Low-loss photonic integrated circuits (PICs) are the key elements in future quantum technologies, nonlinear photonics and neural networks. The low-loss photonics circuits technology targeting C-band application is well established across multi-project wafer (MPW) fabs, whereas near-infrared (NIR) PICs suitable for the state-of-the-art single-photon sources are still underdeveloped. Here, we report the labs-scale process optimization and optical characterization of low-loss tunable photonic integrated circuits for single-photon applications. We demonstrate the lowest propagation losses to the date (as low as 0.55 dB/cm at 925 nm wavelength) in single-mode silicon nitride submicron waveguides (220x550 nm). This performance is achieved due to advanced e-beam lithography and inductively coupled plasma reactive ion etching steps which yields waveguides vertical sidewalls with down to 0.85 nm sidewall roughness. These results provide a chip-scale low-loss PIC platform that could be even further improved with high quality SiO2 cladding, chemical-mechanical polishing and multistep annealing for extra-strict single-photon applications.

© 2022 Optica Publishing Group under the terms of the Optica Publishing Group Open Access Publishing Agreement

1. Introduction

Photic integrated circuits (PICs) are under focused attention due to their high potential for future applications in telecom and datacom [1-3], LiDAR [3, 4], biophotonics [3, 6], nonlinear photonics [8, 9], neural networks [10-12] and quantum technologies [13-19]. In a wide variety of material platforms suitable for photonic integration, scalable and power-efficient solutions nowadays are driven by Si [20, 21], InP [22, 23] and Si3N4 [24, 25]. Despite current technology limitations on active elements and modulation speeds, silicon nitride platform exploits the advantage of passive components with lowest losses in a wide wavelength range from visible to mid-IR in integrated circuits [26]. Using hybrid assembly, flip-chip integration and wafer bonding with A1B2 or SOI platforms [27, 28], silicon nitride photonic platform could be equipped with all the necessary tools for fully integrated optical signal processing.

Ultra-low (<0.01 dB/cm) propagation losses are the key to high-efficiency devices on PICs. To achieve such low values, three major origins of losses have to be considered. The origins are absorption, radiation and scattering losses. Using high quality wet and dry oxidation with LPCVD SiO2 and stoichiometric Si3N4 films together with high temperature annealing, absorption losses could be lowered down to less than 0.1 dB/m [29]. With advanced bends optimization techniques, radiation losses due to mode mismatch can be reduced to 0.012 dB/90° bend values [30, 31]. Thus, scattering losses from bottom, sidewalls and upper surfaces roughness are the main source of light attenuation in waveguides. Compared to upper and
bottom surfaces roughness reduction methods (usually chemical-mechanical polishing [32]), reduction of waveguide sidewall roughness still remains the primary technological challenge [29, 33].

There are three main fabrication processes proposed for effective minimization of propagation losses in silicon nitride photonic integrated circuits. The first one is the photonic Damascene reflow process, which allows to fabricate circuits with crack-free silicon nitride films up to 1.5 μm thickness [33]. Using stress management, SiO2 preform reflow and high precision chemical-mechanical planarization, silicon nitride microresonators with quality factor up to $32 \cdot 10^4$ (equal to 1 dB/m at 1550 nm wavelength) were fabricated [34]. However, extremely high annealing temperatures lead to silicon diffusion in SiO2, degrading optical properties of both materials. Thicker layers of silicon dioxide are required to prevent absorption losses [34]. It was also found out that SiO2 preform reflow may introduce transition metals (Cr, Fe, Cu) impurities and enhance their diffusive redistribution [35], which causes wavelength-independent absorption losses. The above limitations together with high requirements for chemical-mechanical planarization constrain the application of the Damascene reflow process in R&D laboratories for experimental and small-scale batches of devices.

The second one is the classic subtractive process. It is an alternative to the photonic Damascene fabrication process [36]. Proper optimization of individual fabrication steps (mainly lithography and etching steps) results in circuits with low losses (microresonators with quality factor up to $70 \cdot 10^6$, equivalent to 0.4 dB/m at 1550 nm wavelength). The technology utilizes Si3N4 thicknesses up to 1 μm with multistep LPCVD deposition process without long extremely high-temperature annealing and high precision chemical-mechanical planarization steps.

The third one is the silicon nitride TriPleX® waveguide technology [37]. It is a variation of subtractive process for fabrication of ultralow-loss silicon nitride waveguides. Using waveguides with high-aspect ratio core (single or double stripe, up to 100 nm thickness, up to 10 μm width) record propagation losses in silicon nitride based photonic circuits are achieved (microresonators with quality factor up to $422 \cdot 10^6$, equivalent to 0.06 dB/m at 1550 nm wavelength [37]). The approach is characterized be very low mode confinement and weak interaction of mode with waveguide surfaces roughness [26]. However, low confinement requires very thick lower SiO2 layers (up to 15 μm) and also imposes restriction on critical bending radius of waveguides and microresonators (up to 1 cm), which limits scalability of the technology [38].

The above results are obtained at infrared C-band which is actively used in telecommunications, LiDAR, and quantum technologies. However, there are many applications where ultralow losses at wavelengths from 900 to 940 nm are crucial [17, 18, 39, 40]. In this wavelength range single-mode waveguides have to be significantly narrower down to 600 nm width with upper SiO2 cladding (versus several microns width at 1550 nm wavelength), leading to higher interaction of waveguide mode with inhomogeneities and surfaces roughness, and thus to higher propagation losses. The lowest propagation losses of 0.6-1.5 dB/cm have been reached in silicon nitride waveguides with the classic subtractive fabrication process [41-43]. With silicon nitride TriPleX® technology the first 12-mode quantum photonic processor was fabricated demonstrating propagation losses less than 0.3 dB/cm at 940 nm operation wavelength [17]. In [18] silicon nitride PICs with on-chip quantum single-photon source are fabricated, reaching the lowest propagation losses to date – 0.01 dB/cm at 920 nm wavelength. Despite ultralow losses, authors declared very low single-photon coupling efficiency due to low mode confinement. To achieve higher coupling efficiency with medium and high mode localization in silicon nitride waveguides, comparable to the C-band, further improvement of the fabrication processes is required with an emphasis on studying the effect of their parameters on the reduction of surface roughness.

In this work, we report on the fabrication and optical characterization of low-loss silicon nitride photonic integrated circuits, with propagation losses less than 0.6 dB/cm at 925 nm
wavelength. We perform the first in-depth, to the best of our knowledge, study of the influence of e-beam lithography and reactive ion etching parameters on the roughness of waveguide sidewalls. The study formulates rules to fabricate low-loss waveguides with smooth sidewalls. Using classic subtractive fabrication process based on optimized e-beam lithography and inductively coupled plasma reactive ion etching (ICP-RIE), we fabricated 550 nm-width single-mode submicron waveguides with sidewall roughness less than 1 nm and near 90º sidewalls angle, directional couplers with a gap down to 100 nm, grating and 120 nm-width taper couplers with insertion losses less than 8 dB and 4 dB, respectively. In this paper we propose the numerical solution for Payne-Lacey model, which allows accurate modeling of propagation losses in waveguides taking into account all three standard sidewall roughness parameters (standard deviation, correlation length and roughness exponent).

The paper is organized as follows. Section 2 presents modern methods for sidewall roughness measurement and explains the measurement technique used in this work. Section 3 presents the fabrication process of low-loss silicon nitride photonic integrated circuits with in-depth analysis of e-beam lithography and inductively coupled plasma reactive ion etching processes. Section 4 presents up-to-date approaches for propagation losses modeling in waveguides with proposed numerical solution taking into account roughness exponent in Payne-Lacey model. Finally, section 5 presents optical characterization of photonic integrated circuits elements – propagation and coupling losses are measured with “cut-back” technique.

2. Sidewall roughness measurement

There are two commonly used methods for sidewall roughness measurements: specialized atomic force microscopy (AFM) and scanning electron microscopy (SEM). The first one with rotated scanning axis and customized AFM tips allows to carefully measure sidewall roughness with atomic-scale sensitivity and resolution approximately 0.1 nm [44]. However, this technique is very expensive, time consuming and nonstandard for most R&D laboratories. Recently, the method for direct sidewall roughness measurement of waveguides with standard AFM was presented. It is based on Bosch deep silicon etching to fabricate a tall and thin silicon pillar with waveguide on top [45]. The above techniques require specialized metrology tools or high precision fabrication process with optimization of several photolithography and deep silicon etching steps. We choose scanning electron microscopy for sidewall roughness measurement, as this is a straightforward and convenient method. It is less accurate compared to AFM due to noise, aberrations, and charge accumulation [46]. However, for SEM based sidewall roughness measurement, the only requirement is algorithm for edge detection and roughness parameters extraction (Fig. 1).

Fig. 1. (a) SEM image of waveguide sidewall (with resist on top). (b) Detected edge on SEM image of e-beam resist (blue line). (c) Detected edge on SEM image of etched silicon nitride waveguide (blue line).

In this work, we develop the sidewall roughness measurement algorithm using MATLAB software and methodology from [47-50]. It includes waveguide edge detection based on SEM
image which requires no image filtration and frequency-domain analysis of obtained data for eliminating noise and extraction of three main roughness parameters – root-mean-square (RMS) roughness \( \sigma \), correlation length \( \xi \) and roughness exponent \( H \) (more information about roughness parameters measurement could be found in Supplementary materials). Figure 1 demonstrates waveguide edges detection from SEM images with developed algorithm.

3. Fabrication of low-loss silicon nitride photonic integrated circuits

Fabrication process of low-loss silicon nitride photonic integrate circuits with light coupling through grating couplers is shown in Figure 2. Although grating couplers provide access to any location in the PIC and do not require complex post-fabrication processing, they provide coupling efficiency up to 60% [51]. For higher coupling efficiency, which is critical for single-photon applications, much more complicated fabrication process and optimized coupling structure can be used. This purpose requires developing optical grade quality multistep deep reactive ion etching techniques to form precise edge of waveguides for coupling to photonic integrated circuit. [36, 52-54].

![Fig. 2. The fabrication process of silicon nitride photonic integrated circuits. Inset: Mode simulation of a single-mode 220 nm tall and 550 nm wide waveguide at 925 nm wavelength.](image)

We use commercially available 525 um thick silicon wafers with 2.5 um thickness of wet SiO\(_2\) and 220 nm thickness of stoichiometric LPCVD Si\(_3\)N\(_4\) from Silicon Materials Inc. (USA). In our circuits we use single-mode silicon nitride waveguides with 550 nm width and 220 nm height (Fig. 2). The wafers are diced into standard 25x25 mm\(^2\) dies, which are then cleaned from organic, mechanical and metal residues. After that, e-beam lithography and inductively coupled plasma reactive ion etching are used for waveguides patterning with subsequent upper SiO\(_2\) cladding deposition. For tunable beam splitters (Mach-Zehnder interferometers with thermo-optic phase shifters) we fabricate heaters and wiring with laser lithography and lift-off processes. After final cleaning, we bond the fabricated photonic integrated circuit to printed circuit board (PCB) and package for further testing. In next sections, we focus on in-depth study and optimization of e-beam lithography and ICP-RIE steps of the above fabrication process.

3.1 Electron-beam lithography and development

Electron-beam lithography was done using a beam with current of 400 pA to direct-write our circuits into a MaN-2403 negative resist. While direct writing by e-beam is a powerful and flexible method for fabricating features with the critical dimension less than 100 nm, its drawback is appearance of stitches at working fields boundaries due to lens aberrations and
motorized stage instability. Also, due to statistical errors (fluctuations of beam current, vibrations, jitter), sidewall roughness of features could be increased [55, 56]. Using substrates with dielectric materials (SiO$_2$, Si$_3$N$_4$), accumulation of charge leads to increased sidewall roughness and decreased resolution [57]. These limitations lead to topology defects (Fig. 3) and dramatic increase in PICs loss, thus requiring the optimization of e-beam lithography parameters.

For stitching error reduction, a multipass e-beam writing and conductive polymer are the most effective techniques [58, 59]. In this work we optimize number of writing passes, the size of working field (WF) and conductive polymer development temperature for stitching error and resist sidewalls roughness reduction. To estimate the stitching error, more than 200 measurements for each specimen were carried out. Sidewall roughness was evaluated from 18 SEM images of waveguide edges with a length of 1 μm. Figure 4 shows stitching error and resist sidewall RMS roughness dependence versus different exposure parameters (number of writing passes and WF size).

Difference between one pass and multipass writing is observed in reducing the average stitching error modulo from $55.17 \pm 11.41$ nm to $21.90 \pm 6.00$ nm. Decreasing working field
allows further reduction of the stitching error modulo down to $1.04 \pm 1.35$ nm. Statistical exposure errors, such as current fluctuations, jitter and beam drift, as well as mechanical vibrations and positioning errors are reduced with above techniques, leading to a significant reduction of stitching error. Also, multipass writing lithography and decreased working field allowed to reduce average RMS roughness from $2.63 \pm 0.34$ nm to $2.15 \pm 0.24$ nm. Multipass writing reduces the beam dwell time, thereby reducing charge accumulation and primary electron beam deflection, which has a positive effect on the roughness. The choice of a reduced working field reduces the distortion of the electron beam as it deviates from the optical axis, which also improving RMS sidewall roughness of e-beam resist.

Additionally, we studied RMS roughness changing from conductive polymer development temperature. In the experiments, we varied the development temperature in deionized water from 20 ºC to 60 ºC. As shown in Figure 5, the temperature change reduces the average RMS roughness from $2.63 \pm 0.34$ nm to as low as $1.17 \pm 0.13$ nm with one pass exposure with increased working field. We assume that conductive polymer development in warm deionized water leads to it complete removal from resist surface, thereby smoothing resist sidewalls. Multipass lithography with reduced working field and warm conductive polymer development significantly reduces stitching error and RMS sidewall roughness of e-beam resist, thus can be used for smooth and precise mask layers fabrication.

### 3.2 Inductively coupled plasma reactive ion etching

Dry etching is one of the key technology issues for nanofabrication, capable to provide smooth surfaces and anisotropic etch profiles, with accurate control of process parameters [60]. In the reactive ion etching experiments RMS sidewall roughness, sidewall angle and $\text{Si}_3\text{N}_4$ to resist etching selectivity were optimized by varying RF bias power (HF), coil power (ICP), platen temperature (T), working pressure (p), and composition of gas mixture. In this case we first check the influence of parameters that directly affect the energy of particles in plasma. Figure 6 shows experimental results for RMS sidewall roughness, sidewall angle and etching selectivity (defined as the ratio of the etch rate of $\text{Si}_3\text{N}_4$ to the etch rate of resist) with $\text{Si}_3\text{N}_4$ and resist etching rates versus HF power for different etching regimes. HF power reduction from 250 W to 75 W shows a downwards trend for RMS roughness with sidewall angle improvement (blue and green line in Fig. 6a), due to lowering the energy of ions in discharge. Further
reduction to 40 W leads to enhanced polymerization with formation of thin C(H,F)N passivation film [61] and increase in roughness (purple and orange line in Fig. 6a). We should note that more active isotropic etching occurs with higher platen temperature (purple line in Fig. 6a), leading to lateral etching of sidewalls and passivation film partial removal. This effect provides lower roughness and better angle of sidewalls compared to etching at lower temperatures. As shown in Figure 6b, change in platen power simultaneously changes etching rates of Si$_3$N$_4$ and resist with no change in etching selectivity for most regimes. One can see, that etching selectivity reaches higher values for lower platen temperature and HF power, possible due to higher plasma resistance of e-beam resist. Such an effect can stem from the formation of denser chemical bonds in the resist structure.

![Graph showing waveguides parameters versus platen power](image)

![SEM images](image)

Results of optimization parameters on ICP power for various etch regimes are shown in Figure 7. Increasing ICP power from 300 W to 700 W at lower working pressures leads to higher RMS roughness with improved sidewalls angle due to higher energy ions and higher anisotropy of etching (green line in Fig. 7a). We observed strong damage of resist profile together with notching effect at ICP power above 500 W (SEM images inset in Fig. 7). At higher working pressures an opposite trend occurs with increase in roughness at lower ICP power (purple and orange lines in Fig. 7a) due to enhanced sidewalls passivation. Similar to selectivity dependence on HF power, there is no significant change in selectivity at lower pressure (Fig. 7b). At higher pressure selectivity decreases with higher ICP power as resist etch rate is higher compared to Si$_3$N$_4$ etch rate in discharge with high energy ions.
At the next step platen temperature was varied (Fig. 8). Etching with lower temperature causes sidewalls with higher roughness and worse sidewall angle for all regimes. At lower pressure this effect is associated with higher temperature gradient and stronger ion bombardment. At higher pressure, deposited passivation film becomes more plasma resistant at low temperature and cause rough sidewalls formation. The selectivity also increases with low temperature etching for all regimes. As mentioned earlier, this effect may be associated with a change in the resist structure during cooling, which is confirmed by a decrease in the resist etching rate.
It can be noticed that most etching processes, providing sidewall roughness decrease, have high etching rate, low selectivity and strong deviation of sidewalls angle from 90°. For further Si₃N₄ ICP-RIE process optimization the variation of working pressure were carried out to increase etching selectivity. It was found, that RMS sidewall roughness dependence on working pressure has an extremum at 30 mTorr (Fig. 9a). This effect can be explained by the fact that with an increase in pressure, the amount of gas particles increases, while power fed in the discharge is sufficient to ensure bombardment. At pressures above 30 mTorr the input power becomes insufficient for effective bombardment, and reactive etching mechanism begins to dominate in the etching process. This is confirmed, firstly, by the appearance of a strong lateral etching during the process (SEM images inset in Fig. 9), and secondly, by a sharp increase in the etching selectivity to 2.2 (Fig. 9b). In order to achieve low RMS sidewall roughness while keeping high selectivity and vertical sidewalls we carried out additional optimization of our etching process (see Supplementary materials).

![Graph](image)

**Fig. 9.** Waveguides parameters versus working pressure: (a) RMS sidewall roughness (solid lines) and sidewalls angle of inclination (dashed lines). (b) Etching selectivity, Si₃N₄ and resist etching rates (dashed and dotted lines, respectively). Cross-section of waveguides, fabricated with various etching processes are shown on SEM images.

Finally, we optimized etching chemistry. We used CF₄ as the etchant. For slight passivation of sidewalls, we used CHF₃. Unlike common chemicals for etching Si₃N₄ like CHF₃/O₂ or CHF₃/O₂/N₂ [26, 43, 57], we removed oxygen as it limits selectivity to resist. Etching and passivation balance was achieved with optimized CF₄ and CHF₃ ratio at certain values of etching parameters. As a result of experiments, we developed ICP-RIE of Si₃N₄, which allows achieving almost vertical (89.5°) sidewalls with decrease in RMS sidewall roughness from 1.85 ± 0.21 nm to 1.08 ± 0.06 nm and to as low as 0.85 ± 0.06 nm with optimized e-beam lithography. The selectivity of developed ICP-RIE process was increased from 0.8 to 1.4.
With the optimized technology, we are able to fabricate photonic integrated circuits consisting of single-mode submicron waveguides, $y$-splitters, microring resonators, grating and taper couplers, tunable beam splitters (Mach-Zehnder interferometers with thermo-optic phase shifters) and directional couplers. Images of fabricated photonic circuits and structures are shown in Figure 10.

4. Waveguide propagation losses modeling

To obtain propagation losses due to scattering one commonly uses the analytical approach by Payne and Lacey and the following expression [62]:

$$\alpha \left[ \frac{dB}{cm} \right] = 4.34 \frac{\sigma^2}{K_0 \sqrt{2}d^4n_1^4}gf,$$

where $\alpha$ is the waveguide scattering loss in dB per unit length, $\sigma$ is the RMS deviation, $K_0$ is the free space wave vector, $d$ and $n_1$ are the waveguide half width and refractive index of Si$_3$N$_4$ core, respectively. Function $g$ is determined purely by the waveguide geometry, and $f$ is a function of correlation length and other parameters as defined by Payne and Lacey [63].

Payne-Lacey model provides rapid calculation of losses having good agreement with fully three-dimensional FDTD simulation and experimental results [64, 65]. However, it is impossible to estimate the influence of the roughness exponent $H$ on scattering losses with classical analytical approach. In this work, we propose the numerical solution for the Payne-Lacey model, which provides estimation of the influence of three main roughness parameters, measured with AFM or SEM – root mean square roughness $\sigma$, correlation length $\xi$ and roughness exponent $H$ (more information about our numerical approach could be found in Supplementary materials).

Figure 11 shows the calculation results for propagation losses from scattering for single-mode waveguides with 550 nm width at 925 nm wavelength.
Based on the numerical simulation results, the following conclusions were made.

1. High RMS roughness leads to increase of waveguide mode field interaction with sidewalls roughness, thus to higher scattering losses.

2. As correlation length tends to zero, mode field is less sensitive to changes in roughness at this frequency and is less scattered, even at large values of $\sigma$, which leads to low propagation losses. However, at very short wavelengths, low correlation length can bring higher impact. With an increase in $\xi$, an extremum is observed, indicating an increase in the interaction of the mode field with sidewalls and an increase in losses. As $\xi$ tends to infinity, implying no roughness, the loss tends to zero, since the frequency of the change in the roughness amplitude is also tends to zero.

3. At higher roughness exponent values, the mode field sensitivity to amplitude roughness is at maximum, leading to high scattering losses. However, when roughness exponent is low, that corresponds to high-frequency sidewall roughness, at our wavelength of interest the mode field is insensitive to such high-frequency profile variations, leading to low propagation losses, even at high RMS roughness. Same as correlation length, roughness exponent can have a higher impact on propagation losses at shorter wavelengths.

5. **Optical characterization**

The “cut-back” propagation loss analysis [66, 67] in fabricated Si$_3$N$_4$ waveguides has been performed using the optical characterization setup shown in Fig. 12a. The light from a continuous wave (CW) laser source at 925 nm wavelength was first coupled in single-mode fiber. TE-polarized light was formed with fiber polarization controller (FPC). Using 6-axis micrometer coupling stages, light from fiber was then coupled to waveguides through on-chip grating couplers. After propagating in photonic integrated circuit, the light was coupled out to power detector (PD). Propagation losses were measured on test photonic integrated circuits with various lengths of waveguides, fabricated with initial fabrication process, optimized e-beam lithography and optimized fabrication process (optimized e-beam lithography and ICP-RIE).
Figure 12b shows measured propagation losses in waveguides versus waveguide length. With the initial fabrication technology, a large spread of losses is observed at measured waveguides due to the presence of large stitches between the working fields and high sidewall roughness (blue line in Fig. 12b). As a result of e-beam lithography optimization, stitching error was greatly reduced, leading to decrease in coupling losses from 10.92 dB to 7.27 dB. Resist roughness improvement with optimized lithography shows reduction in propagation losses from 3.08 dB/cm to 1.10 dB/cm (orange line in Fig. 12b). Optimization of the ICP-RIE further reduced the RMS sidewall roughness of the waveguides, leading to propagation losses as low as 0.55 dB/cm (green line in Fig.12b). This result confirms that the main contribution to the propagation losses at 925 nm wavelength is made by scattering from waveguide bottom, sidewalls and upper surfaces roughness. Fabrication process optimization leads to roughness of waveguide sidewalls reduction by factor of 2, resulting in 6 times improvement in losses. Thermo-optic light switching with fabricated tunable beam splitters is shown on Figure 12c, demonstrating high quality and energy-efficient heaters fabrication process.

The results for scattering losses calculation with proposed numerical method are shown in Fig. 12d. Taking into account the roughness parameters measured on waveguides with initial fabrication process, the optimized e-beam lithography and the optimized fabrication process (for more information see Supplementary materials) we compared experimentally obtained propagation losses with calculated ones. The proposed numerical solution allows fairly accurate simulation of propagation losses in waveguides based on data from roughness parameters measurement, obtained with AFM or SEM with less than 10% deviation from experiment.

6. Conclusion

In this work we developed the fabrication process of low-loss silicon nitride photonic integrated circuits with in-depth study of e-beam lithography and inductively coupled plasma reactive ion etching steps for sidewalls roughness and profile angle improvement. The optimized multipass
e-beam lithography process with reduced working field and warm development of conductive polymer results in stitching error reduction down to 1.04 ± 1.35 nm, vertical (89.5°) resist sidewalls and resist sidewall roughness as low as 1.17 ± 0.13 nm. The optimized ICP-RIE process based on the combination of etching and passivation effects of CF₄ and CHF₃ allows to reduce the final waveguide sidewalls roughness down to 0.85 ± 0.06 nm. With the optimized fabrication process, propagation losses in silicon nitride waveguides were reduced from 3.1 dB/cm to 0.55 dB/cm at 925 nm wavelength, which is the lowest demonstrated to date losses for single-mode submicron waveguides [15, 16, 38, 39, 40]. We proposed the enhanced Payne-Lacey analytical model for waveguide propagation losses modeling, which allows taking into account all the measured roughness parameters (σ, ζ and H) for much more accurate loss estimation. Our result demonstrates the high potential for further improvements of propagation losses below 0.1 dB/cm by employing high optical quality SiO₂ cladding, chemical-mechanical polishing and multistep annealing of silicon nitride stack.

Acknowledgments

Samples were made at the BMSTU Nanofabrication Facility (FMN Laboratory, FMNS REC, ID 74300) and measured at MSU Quantum Technology Centre.

Disclosures

The authors declare no conflicts of interest.

Data availability

The data that supports the findings of this study are available from the corresponding author upon reasonable request.

Supplemental document

See Supplemet 1 for supporting content.

References

1. J. Zhang, A. De Groote, A. Abbasi, R. Loi, J. O’Callaghan, B. Corbett, A. J. Trindade, C. A. Bower, and Gunther Roelkens, “Silicon photonics fiber-to-the-home transceiver array based on transfer-printing-based integration of III-V photodetectors,” Opt. Express 25, 14290-14299 (2017).
2. Y. Liu, S. Wang, J. Wang, X. Li, M. Yu, Y. Cai, “Silicon photonic transceivers in the field of optical communication,” Nano Communication Networks 31, 100379 (2022).
3. E. S. Lotkov, A. S. Baburin, I. A. Ryzhikov, O. S. Sorokina, A. I. Ivanov, A. V. Zverev, V. V. Ryzhkov, I. V. Bykov, A. V. Baryshev, Y. V. Panfilov, and I. A. Rodionov, “ITO film stack engineering for low-loss silicon optical modulators,” Sci Rep 12, 6321 (2022).
4. C. Adamopoulos, A. Gharia, A. Niknejad, V. Stojanovic, and M. Anwar, “Microfluidic Packaging Integration with Electronic-Photonic Biosensor Using 3D Printed Transfer Molding,” Biosensors 10(11), 177 (2020).
5. E. A. Rank, R. Sentosa, D. J. Harper, M. Salas, A. Gaugutiz, D. Seyringer, S. Nevlasil, A. Maese-Novo, M. Eggeling, P. Mueller, R. Hainberger, M. Sagmeister, J. Kraft, R. A. Leitgeb, and W. Drexler, “Toward optical coherence tomography on a chip: in vivo three-dimensional human retinal imaging using photonic integrated circuit-based arrayed waveguide gratings,” Light Sci. Appl. 10, 6 (2021).
6. X. Sun, L. Zhang, Q. Zhang, and W. Zhang, “Si Photonics for Practical LiDAR Solutions,” Applied Sciences 9(20), 4225 (2019).
7. Y. Guo, Y. Guo, C. Li, H. Zhang, X. Zhou, and L. Zhang, “Integrated Optical Phased Arrays for Beam Forming and Steering,” Applied Sciences 11(9), 4017 (2021).
8. J. W. Choi, B. -U. Sohn, E. Sahin, G. F. R. Chen, P. Xing, D. K. T. Ng, B. J. Eggleton, and D. T. H. Tan, “An optical parametric Bragg amplifier on a CMOS chip,” Nanophotonics 10(13), pp. 3507-3518 (2021).
9. P. Marin-Palomo, J. Kemal, M. Karpov, A. Kordts, J. Pfeifle, M. H. P. Pfeiffer, P. Trocha, S. Wolf, V. Brasch, M. H. Anderson, R. Rosenberger, K. Vijayan, W. Freude, T. J. Kippenberg, and C. Koos “Microresonator-based solitons for massively parallel coherent optical communications,” Nature 546, 274-279 (2017).
10. A. Katumba, M. Freiberger, F. Laporte, A. Luginna, S. Sacksen, C. Ma, J. Dambre, and P. Bienstman, “Neuromorphic Computing Based on Silicon Photonics and Reservoir Computing,” IEEE Journal of Selected Topics in Quantum Electronics, 24(6), pp. 1-10 (2018).
11. Y. Shen, N. C. Harris, S. Skirlo, M. Prabha, T. Baehr-Jones, M. Hochberg, X. Sun, S. Zhao, H. Larochele, D. Englund, and M. Soljačić, “Deep learning with coherent nanophotonic circuits,” Nature Photon. 11, 441-446 (2017).
Selected Topics in Quantum Electronics

M. Lipson, M. Nelson (2022).

Hybrid Integration Offered by Silicon Nitride Photonics

Lightwave Technology

S. I. Bogdanov, M. Y. Shalaginov, A. S. Lagutchev, C. Blumenthal, K. Epping, H. P. Epping, R. C. G. H. Roeloffzen, J. J. Renema, I. A. Walmsley, P. W. H. Pinkse, and K. C. Emmerick, "Strongly radiative antennas," A. R. Gabidullin, I. A. Ryzhikov, I. A. Rodionov, A. V. Kildishev, S. I. Bozhevolnyi, A. Boltasseva, V. M. Shalaev, and J. B. Khurghin, "Ultrafast quantum photonics enabled by coupling plasmonic nanocavities to strongly radiative antennas," Optica 7, 463–469 (2020).

C. Taballione, T. A. W. Wolterink, J. Lugani, A. Eckstein, B. A. Bell, R. Grootjans, I. Vischer, D. Geskus, C. G. H. Röföldy, J. J. Renema, I. A. Walmsley, P. W. H. Pinkse, and K. J. Boller, "8×8 reconfigurable quantum processor based on silicon nitride waveguides," Opt. Express 27, 26842-26857 (2019).

C. Taballione, R. van der Meer, H. J. Snijders, P. Hoijtschuur, J. P. Epping, M. de Goede, B. Kassenberg, P. Venderbosch, C. Toebes, H. van den Vlekkert, P. W. H. Pinkse, and J. J. Renema, "A universal fully reconfigurable 12-mode quantum photonic processor," Mater. Quantum Technol. 1, 035002 (2021).

C. Taballione, M. Anguita, M. de Goede, P. Venderbosch, B. Kassenberg, H. Snijders, N. Kannan, D. Smith, J. P. Epping, R. van der Meer, P. W. H. Pinkse, H. van den Vlekkert, and J. J. Renema, "20-Mode Universal Silicon Nitride Photonic Processor," arXiv:2203.01801 [quant-ph] (2022).

M. de Goede, H. Snijders, P. Venderbosch, B. Kassenberg, N. Kannan, D. H. Smith, C. Taballione, J. P. Epping, H. van den Vlekkert, and J. J. Renema, "High Fidelity 12-Mode Quantum Photonic Processor Operating at InGaAs Quantum Dot Wavelength," arXiv:2204.05768 [quant-ph] (2022).

A. Chanana, H. Larocque, R. Moreira, J. Carolan, B. Guha, V. Anant, J. D. Song, D. Englund, D. J. Blumenthal, K. Srinivasan, and M. Davanco “Triggered single-photon generation and resonance fluorescence in ultra-low loss integrated photonic circuits,” arXiv:2202.04615 [physics.optics] (2022).

S. I. Bogdanov, M. Y. Shalaginov, A. S. Lagutchev, C.-C. Chiang, D. Shah, A. S. Baburin, I. A. Ryzhikov, I. A. Rodionov, A. V. Kildishev, A. Boltasseva, and V. M. Shalaev, "Ultra-bright Room-temperature sub-nanoscond emission from single nitrogen-vacancy centers coupled to Nanopatch antennas," Nano Letters 18, 4837–4844 (2018).

W. Bogarts, and S.K. Selvaraja, “Silicon-on-insulator (SOI) technology for photonic integrated circuits (PICs),” Silicon-On-Insulator (SOI) Technology, O. Kononchuk, and B. -Y. Nguyen, eds. (Woodhead Publishing, 2014), pp. 395-434.

S. Y. Siew, B. Li, F. Guo; H. Y. Zheng, W. Zhang, P. Guo, S. W. Xie, A. Song, B. Dong, L. W. Luo, C. Li, X. Luo, and Q. Lo, "Review of Silicon Photonics Technology and Platform Development," Journal of Lightwave Technology 39(13), pp. 4374-4389 (2021).

Z. Yan, Y. Han, L. Lin, Y. Xue, C. Ma, W. K. Ng, K. Si. Wong, and K. M. Lau, “A monolithic InP/SOI platform for integrated photonics,” Light Sci. Appl. 10, 200 (2021).

M. Smit, K. Williams, and J. van der Tol, “Past, present, and future of InP-based photonic integration,” APPLIED PHYSICS 4, 050901 (2019).

T. Sharma, J. Wang, B. K. Kaushik, Z. Cheng, R. Kumar, Z. Wei, and X. Li, “Review of Recent Progress on Silicon Nitride-Based Photonic Integrated Circuits,” IEEE Access 8, pp. 19.054-19.0546 (2020).

F. Gardes, A. Shooa, G. De Paoli, I. Skandalos, S. Ilie, T. Rutarawut, W. Talataisong, J. Faneca, V. Vitali, Y. Hou, T. D. Bucio, I. Zeimpekis, C. Lacava, and P. Petropoulos, “A Review of Capabilities and Scope for Hybrid Integration Offered by Silicon-Nitride-Based Photonic Integrated Circuits,” Sensory 22(11), 4227 (2022).

M. W. Puckett, K. Liu, N. Chauhan, Q. Zhao, N. Jin, H. Cheng, J. Wu, R. O. Behunin, P. T. Rakich, K. D. Nelson, and D. J. Blumenthal, “422 Million intrinsic quality factor planar integrated all-waveguide resonator with sub-MHz linewidth,” Nat. Commun. 12, 934 (2021).

M. Theurer, M. Moehrle, A. Sigmund, K.-O. Velthaus, R. M. Oldenburg, L. Wevers, F. M. Postma, R. Materman, F. Schreuder, D. Geskus, K. Wörhoff, R. Dekker, Rene G. Heideman, and M. Schell, “Flip-Chip Integration of InP to SiN Photonic Integrated Circuits,” Journal of Lightwave Technology 38(9), pp. 2630-2636 (2020).

P. Wang, G. Luo, Y. Xu, Y. Li, Y. Su, J. Ma, R. Wang, Z. Yang, X. Zhou, Y. Zhang, and J. Pan, “Design and fabrication of a SiN-Si dual-layer optical phased array chip,” Photon. Res. 8, 912-919 (2020).

X. Ji, F. A. S. Barbosa, S. P. Robit, A. Dutt, J. Capdenas, Y. Okawachi, A. Bryant, A. L. Gaeta, and M. Lipson, “Ultra-low-loss on-chip resonators with sub-milliwatt parametric oscillation threshold,” Optica 4, 619-624 (2017).

J. Hwan Song, T. D. Kongnyuy, P. De Heyn, S. Lardenois, R. Jansen, and X. Rottenberg, “Low-Loss Waveguide Bends by Advanced Shape for Photonic Integrated Circuits,” Journal of Lightwave Technology 38(12), pp. 3273-3279 (2020).

X. Ji, J. Liu, J. He, R. N. Wang, Z. Qiu, J. Riemensberger, and T. J. Kippenberg, “Compact, spatial-mode-interaction-free, ultralow-loss, nonlinear photonic integrated circuits,” Commun. Phys. 5, 84 (2022).

M. J. Shaw, J. Guo, G. A. Vawter, S. Habermehl, and C. T. Sullivan, “Fabrication techniques for low-loss silicon nitride waveguides,” Proc. SPIE 5720, 1 (2005).

M. H. P. Pfeiffer, C. Herkommer, J. Liu, T. Morais, M. Zervas, M. Geiselmüller, and T. J. Kippenberg, “Photonic Damascene Process for Low-Loss, High-Confinement Silicon Nitride Waveguides,” IEEE Journal of Selected Topics in Quantum Electronics 24(4), pp. 1-11 (2018).
34. H. El Dirani, M. Casale, S. Kerdiles, C. Socquet-Clerc, X. Letartre, C. Monat, and C. Sciancalepore, “Crack-Free Silicon-Nitride-on-Insulator Nonlinear Circuits for Continuum Generation in the C-Band,” *IEEE Photonics Technology Letters* **30**(4), pp. 355-358 (2018).

35. M. H. P. Pfeiffer, J. Liu, A. S. Raja, T. Morais, B. Ghadiani, and T. J. Kirpenhoff, “Ultra-smooth silicon nitride waveguides based on the Damascene reflow process: fabrication and loss origins,” *Optica* **5**, 884-892 (2018).

36. X. Ji, S. Roberts, M. Corato-Zanarella, and M. Lipson, “Methods to achieve ultra-high quality factor silicon nitride resonators”, *APL Photonics* **6**, 071101 (2021).

37. C. G. H. Roeloffzen, M. Hoekman, E. J. Klein, L. S. Wevers, R. B. Timens, D. Marchenko, D. Geskus, R. Dekker, A. Alippi, R. Grootjans, A. van Rees, R. M. Oldenbeuving, J. P. Epping, R. G. Heideman, K. Wörhoff, A. Leins, D. Geuzebroek, E. Schreuder, P. W. L. van Dijk, J. Visscher, C. Taddei, Y. Fan, C. Taballione, Y. Liu, D. Marpaung, L. Zhuan, M. Benelaja, and K.-J. Boller, “Low-Loss Si3N4 TriPlex Optical Waveguides: Technology and Applications Overview,” *IEEE Journal of Selected Topics in Quantum Electronics* **24**(4), pp. 1-21 (2018).

38. W. Jin, Q.-F. Yang, L. Chang, B. Shen, H. Wang, M. A. Leal, L. Wu, M. Gao, A. Feshali, M. Paniccia, K. J. Vahala, and J. E. Bowers, “Hertzian-semiconductor lasers using CMOS-ready ultra-high-Q microresonators,” *Nat. Photonics* **15**, 346–353 (2021).

39. T. Verduin, D. Fowler, S. Malhouitre, S. Garcia, P. Grosse, W. Rabaud, and B. Szegel, “SiN integrated optical phased arrays for two-dimensional beam steering at a single near-infrared wavelength,” *Opt. Express* **27**, 5851-5858 (2019).

40. K. Erotkriotou, R. M. Heath, G. G. Taylor, C. Tian, A. Banerjee, A. Casaburi, C. M. Natarajan, S. Miki, H. Terai, and R. H. Hadfield, “Nano-optical photoresponse mapping of superconducting nanowires with enhanced near infrared absorption,” *Supercond. Sci. Technol.* **31**, 125012 (2018).

41. X. Lu, Q. Li, D. A. Westly, G. Mollé, A. Singh, V. Anant, and K. Srinivasan, “Chip-integrated visible–telematong photon pair source for quantum communication,” *Nat. Phys.* **15**, 373–381 (2019).

42. A. Z. Subramanian, P. Neutens, A. Dhakal, T. Claes, X. Rottenberg, F. Peyeskas, S. K. Selvaraja, P. Helin, B. Dubois, K. L. Helvig, S. Severi, P. Deshpande, R. Baets, and P. Van Dorpe, “Low-Loss Singlemode PECVD Silicon Nitride Photonic Wire Waveguides for 532–900 nm Wavelength Window Fabricated Within a CMOS Pilot Line,” *IEEE Photonics Journal* **5**(6), pp. 2202809-2202809 (2013).

43. Q. Wilmart, H. El Dirani, N. Tyler, D. Fowler, S. Malhouitre, S. Garcia, M. Casale, S. Kerdiles, K. Hassan, C. Monat, X. Letartre, A. Kamel, M. Pu, K. Yvind, L. K. Oxenløwe, W. Rabaud, C. Sciancalepore, B. Szegel, and S. Olivier, “A Versatile Silicon-Silicon Nitride Photonics Platform for Enhanced Functionality and Applications,” *Applied Sciences* **9**(21), 255 (2019).

44. N. G. Orji, V. V. Voroburger, J. Fu, R. G. Dixson, C. V. Nguyen, and J. Raja, “Line edge roughness metrology using atomic force microscopes,” *Meas. Sci. Technol.* **16**, 2147 (2005).

45. S. Roberts, X. Ji, J. Cardenas, M. Corato-Zanarella, and M. Lipson, “Measurements and modeling of atomic-scale sidewalk roughness and losses in integrated photonic devices,” *arXiv:2105.11477 [physics.optics]* (2022).

46. A. Yamaguchi, and J. Yamamoto, “Influence of image processing on line-edge roughness in CD-SEM measurement”, *Proc. SPIE* **6922**, 1 (2008).

47. T. Verduin, P. Knitt, and É. W. Hagen, “Determination of line edge roughness in low dose top-down scanning electron microscopy images,” *Proc. SPIE* **9050**, 1 (2014).

48. C. A. Mack, “Analytic form for the power spectral density in one, two, and three dimensions,” *Journal of Micro/Nanolithography, MEMS, and MOEMS* **10**(4), 040501 (2011).

49. C. A. Mack, “Systematic errors in the measurement of power spectral density,” *Journal of Micro/Nanolithography, MEMS, and MOEMS* **12**(3), 033016 (2013).

50. C. A. Mack, “More systematic errors in the measurement of power spectral density”, *Proc. SPIE* **9424**, 1 (2015).

51. E. W. Ong, N. M. Fahrenkopf, and D. D. Coolbaugh, “SiN bilayer grating coupler for photonic systems,” *OSA Continuum* **1**, 13-25 (2018).

52. A. Begović, L. G. Carpenter, S. K. Binti, M. R. Uddin, A. Dikshit, C. Baiocco, G. Leake, Z. R. Huang, N. M. Fahrenkopf, and David Haremme, “Facet optimization for edge-coupling of fiber to foundry fabricated SOI waveguides,” *Proc. SPIE* **12004**, 2610538 (2022).

53. A. S. Baburin, E. S. Loktev, E. V. Sergeev, M. Andronic, D. A. Baklykov, V. E. Stukalova, K. A. Buzaverov, S. S. Avdeev, I. A. Ryzhikov, I. V. Dyakonov, N. Skryabin, M. Ya. Saygin, S. P. Kukis, and I. A. Rodionov, “Tunable low-loss silicon nitride integrated circuits,” in *2022 International Conference Laser Optics (ICLO)* (2022), pp. 1-1.

54. D.A. Baklykov, M. Andronic, O. S. Sorokina, S. S. Avdeev, K. A. Buzaverov, I. A. Ryzhikov, and I. A. Rodionov, “Self-Controlled Cleaving Method for Silicon DRIE Process Cross-Section Characterization,” *Micromachines* **12**(5), 534 (2021).

55. A. L. Bogdanov, J. Lapointe, and J. H. Schmid, “Electron-beam lithography for photonic waveguide fabrication: Measurement of the effect of field-stitching errors on optical performance and evaluation of a new compensation method,” *Journal of Vacuum Science & Technology B* **30**, 031606 (2012).

56. D. M. Tennant, R. Fullowan, H. Takemura, M. Isobe, and Y. Nakagawa, “Evaluation of a 100 kV thermal field emission electron-beam nanolithography system,” *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **18**, 3089-3094 (2000).
57. P. Muñoz, Y. S. Yong, M. Dijkstra, F. B. Segerink, and S. M. García-Blanco, “Double metal layer lift-off process for the robust fabrication of plasmonic nano-antenna arrays on dielectric substrates using e-beam lithography,” Opt. Mater. Express 9, 2046-2056 (2019).

58. R. K. Dey, and B. Cui, “Stitching error reduction in electron beam lithography with in-situ feedback using self-developing resist,” Journal of Vacuum Science & Technology B 31, 06F409 (2013).

59. M. Muhammad, S. C. Buswell, S. K. Dew, and M. Stepanova, “Nanopatterning of PMMA on insulating surfaces with various anticharging schemes using 30 keV electron beam lithography,” Journal of Vacuum Science & Technology A 29, 06F304 (2011).

60. A. A. Dobronosova, A. I. Ignatov, N. A. Orlikovskiy, M. Andronik, K. O. Buzaverov, D. A. Ezenkova, S. A. Avdeev, D. A. Baklykov, V. V. Ryzhkov, A. M. Merzlikin, A. V. Batyshev, I. A. Ryzhikov, and I. A. Rodionov, “Low-damage reactive ion etching of nanoplasmonic waveguides with Ultrathin Noble Metal Films,” Applied Sciences 9, 4441 (2019).

61. M. Schaepkens, T. E. F. M. Standaert, N. R. Rueger, P. G. M. Sebel, G. S. Oehrlein, and J. M. Cook, “Study of the SiO2-to-Si3N4 etch selectivity mechanism in inductively coupled fluorocarbon plasmas and a comparison with the SiO2-to-Si mechanism,” Journal of Vacuum Science & Technology A 17, 26-37 (1999).

62. F. Grillot, L. Vivien, S. Laval, and E. Cassan, “Propagation loss in single-mode ultrasmall square silicon-on-insulator optical waveguides,” Journal of Lightwave Technology 24(2), pp. 891-896 (2006).

63. F. P. Payne, and J. P. R. Lacey, “A theoretical analysis of scattering loss from planar optical waveguides,” Opt. Quant. Electron. 26, 977-986 (1994).

64. K. P. Yap, A. Delage, J. Lapointe, B. Lamontagne, J. H. Schmid, P. Waldron, B. A. Syrett, and S. Janz, “Correlation of Scattering Loss, Sidewall Roughness and Waveguide Width in Silicon-on-Insulator (SOI) Ridge Waveguides,” Journal of Lightwave Technology 27(18), pp. 3999-4008 (2009).

65. E. Jaberansary, T. M. B. Masaud, M. M. Milosevic, M. Nedeljkovic, G. Z. Mashanovich, and H. M. H. Chong, “Scattering Loss Estimation Using 2-D Fourier Analysis and Modeling of Sidewall Roughness on Optical Waveguides,” IEEE Photonics Journal 5(3), pp. 660101-6601010 (2013).

66. Z. Liao, and J. S. Atchison, “Precision etching for multi-level AlGaAs waveguides,” Opt. Mater. Express 7, 895-903 (2017).

67. W. D. Sacher, X. Luo, Y. Yang, F.-D. Chen, T. Lordello, J. C. C. Mak, X. Liu, T. Hu, T. Xue, P. G.-Q. Lo, M. L. Roukes, and J. K. S. Poon, “Visible-light silicon nitride waveguide devices and implantable neurophotonic probes on thinned 200 mm silicon wafers,” Opt. Express 27, 37400-37418 (2019).