Design of sweep frequency signal source in residual stress detection platform based on Zynq

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Abstract. The signal generator based on DDS technology has high frequency and resolution, and is widely used in many fields such as instrument technology, radar, satellite timing, remote control and telemetry, and is one of the important directions of current signal generator research. In order to achieve a cost-effective, high frequency resolution signal source to stimulate the sensors in the residual stress detection system, this paper selects the Zynq-7020 on-chip system to control the 14-bit direct digital frequency synthesis chip AD9954 to obtain a 40Hz~1MHz sinusoidal signal output. Finally, the performance and technical parameters of the system are tested experimentally. The output signal of the signal source is stable, the signal-to-noise ratio is high, and the frequency error is within 0.1%.

1. Introduction
Residual stress is a kind of stress that keeps the internal balance of the specimen without external stress. Metal components are commonly used parts in engineering applications. They are currently widely used in machinery, electric power, aviation, aerospace, transportation and other fields. Their safety and durability directly affect the performance of equipment. Various mechanical manufacturing processes (such as casting, cutting, welding, heat treatment, assembly, etc.) will cause different degrees of residual stress inside the workpiece. Residual stress will have a huge impact on the physical and mechanical properties of the material, and will cause great harm to the strength of the structure. Therefore, it is of great significance for the detection of residual stress.

Eddy current detection method is an important method of residual stress detection, which is mainly based on the change of material conductivity and magnetic permeability caused by residual stress[1-3]. It has the advantages of low cost, simple equipment and convenient operation. The overall structure of the residual stress detection platform is shown in Figure 1. The residual stress is mainly divided into four modules. The first part is the excitation source module, which mainly realizes the generation of multi-frequency excitation signals and provides excitation signals for planar array sensors. The second part is the signal conditioning circuit, which mainly realizes the amplification and filtering of the detection signal. The third part is the data acquisition module, including single-ended to differential circuit, and high-precision data acquisition circuit. The fourth part is an information processing platform based on FPGA and ARM, which completes the information processing algorithm and human-computer interaction of the entire system. The frequency sweep signal source can generate a sinusoidal excitation signal with adjustable frequency and amplitude. It is an important functional module of the residual stress detection platform. Its accuracy and stability directly affect the accuracy and stability of the entire detection platform[4]. Therefore, the development of a high-performance signal source is very important for the eddy current method to achieve residual stress detection.
With the continuous advancement of science and technology, the performance requirements of dedicated signal sources in various application fields are getting higher and higher. Traditional implementation methods cannot meet people's needs for signal sources, and direct digital frequency synthesis (DDS) technology emerges at the historic moment. Compared with traditional frequency synthesis technology, it has the advantages of high frequency resolution, wider output signal frequency band, fast frequency switching time, and continuous phase during frequency switching. Since the 1980s, direct digital frequency synthesis technology has developed rapidly. Representative manufacturers include TI, Analog Device and Stanford in the United States. Among them, Analog Device’s DDS integrates on-chip comparators, RAM, PLL, and mixers. With features such as registers and registers, it occupies the largest market share. There are as many as 32 DDS chips on sale. The input clock frequency ranges from 16M to 3.5GHz, and the output data bit width ranges from 10 bits to 14 bits, which can meet various applications.

2. Signal source design

In order to meet the needs of residual stress detection, it is necessary to provide an excitation signal with an excitation frequency of 40 Hz to 1 MHz, and the frequency can be continuously adjusted. The DDS chip in this design uses AD9954 chip of ADI Company, its power consumption is only 200mW, and the volume is small, the advantage is remarkable. AD9954 integrates a 14-bit DAC, which can generate sine wave signals up to 200MHz. AD9954 is programmed through a high-speed serial I/O port and can load 32-bit frequency control words. In this system, the Zynq-7020 chip is selected as the control chip, and the dual-core ARM Cortex processor and Artix-7FPGA are integrated on the zynq[5-6], which not only has the flexible and efficient data computing capabilities of the ARM processor, but also has the advantages of high-speed parallel processing of FPGA. Meet the high performance, low power consumption and multi-core processing capability requirements of complex embedded systems.

AD9954 is connected with the expansion I/O on the zynq development board, the clock signal is provided by the crystal oscillator on the zynq development board, and the hardware connection between the development board and the AD9954 is shown in Figure 2. Because the digital ground (current) has a large interference, the digital circuit itself has strong anti-interference ability, and the analog circuit has weak anti-interference ability. Therefore, in the design, the digital ground and the analog ground are separated by a 0R resistor, and at the same time, the digital power and analog power supply is separated by magnetic beads, which can greatly reduce interference. The AD9954 output is a differential current signal, and the full-scale output current is controlled by an external resistor REST. The relationship is:

\[ I_{OUT} = \frac{39.19}{REST} \] (1)
According to the chip manual, limiting the output current to 10mA can get the best spurious-free output dynamic range performance, so the resistance of REST is set to 3.9K. The output current signal is pulled up to AVDD through a 120Ω resistor to realize I/V conversion to output a voltage signal.

Since the DDS output signal contains a lot of high-frequency noise, it is necessary to set a low-pass filter to filter the output signal to improve the signal purity. In this paper, a seventh-order low-pass elliptic filter with a cutoff frequency of about 1M is designed. The circuit diagram is shown in Figure 3. The voltage follower has an isolation effect to avoid the back-end circuit from affecting the AD9954 chip. Based on the simulation of the multisim software, the Bode plot is shown in Figure 4. It can be seen from the Bode plot that the attenuation of the elliptic filter is less than 2.666dB in the range of 40Hz~1MHz, and the attenuation is less than 3dB when the frequency is greater than 1MHz. Faster and meet the design requirements.
Figure 4. Bode plot of the seventh-order elliptic filter.

3. DDS algorithm implementation
The signal source clock is provided by the Zynq development board. The system clock of the development board is 50MHz. In order to avoid signal integrity problems during high-frequency signal transmission, the frequency divider provides the AD9954 with a 10MHz input clock and sets the PLL frequency multiplication factor to 19 Times, a 190MHz clock is generated inside the DDS chip. The relationship between the output frequency of DDS, the frequency control word FTW and the system clock $f_s$ is:

$$f_o = \frac{(FTW)\ (f_s)}{2^{32}}, \ (0 \leq FTW \leq 2^{31}) \quad (2)$$

$$f_o = f_s \times (1-(FTW/2^{32}) \ ), \ (2^{31} < FTW < 2^{32} - 1) \quad (3)$$

When DDS works, in each clock cycle, the frequency control word (FTW) is accumulated with the phase accumulator once in each clock cycle to obtain the phase value, which provides the addressing address for the memory. The ROM look-up table outputs the corresponding amplitude according to the addressing address output by the phase accumulator, and then realizes the conversion from digital signal to analog signal through DAC. The step sequence wave output by the DAC is passed through a low-pass filter to obtain a pure sine wave.

Among them, the AD9954 register configuration process is shown in Figure 5.
4. System test
Set the frequency to 40Hz, 2kHz, 10kHz, 100kHz, 1MHz respectively, and observe the output of the signal source with a Tektronix MDO4034C oscilloscope. The result is shown in Figure 6.

(a) 40Hz sine wave. (b) 2kHz sine wave.
Figure 6. The output results of the signal source at different frequencies.

The experimental results show that the signal source can output a sine wave in the frequency range of 40 Hz to 1 MHz, with smooth waveform, stable signal, and no obvious jitter. Compare the measured frequency $f_0$ with the set frequency $f$. The results are shown in Table 1. The frequency error is:

$$\delta = \frac{f - f_0}{f_0}$$

It can be seen from the table that the output frequency accuracy of the signal source is high, and the frequency error is within 0.1%, which meets the design requirements.

Table 1. Comparison of measured frequency and set frequency.

| $F$(Hz) | $F_0$(Hz) | Relative error(%) |
|--------|----------|-------------------|
| 40     | 40.00    | 0                 |
| 2k     | 1.999k   | 0.05              |
| 100k   | 100k     | 0                 |
| 1M     | 1.001M   | -0.1              |

5. Concluding remarks

The signal source uses the zynq development board to control the AD9954 chip, which has high integration and good scalability. Compared with the signal generators on the market, the volume and power consumption are small, and the cost is low. The output signal frequency can be continuously adjusted. After actual testing, the output signal frequency of the signal source is 40Hz~1MHz, which meets the signal source requirements of the residual stress detection platform. The output signal of the signal source has high stability, smooth waveform, and high frequency accuracy, which provides a strong support for realizing high-precision residual stress detection.

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