Understanding the Interactions of Workloads and DRAM Types: A Comprehensive Experimental Study

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ABSTRACT

Due to a number of fundamental changes, it has become increasingly difficult to understand the complex interaction between modern applications and main memory, composed of Dynamic Random Access Memory (DRAM) chips. Manufacturers are now selling and proposing many different types of DRAM, with each DRAM type catering to different needs (e.g., high throughput, low power, high memory density). At the same time, the memory access patterns of prevalent and emerging workloads are rapidly diverging, as these applications manipulate larger data sets in very different ways. As a result, the combined DRAM–workload behavior is often difficult to intuitively determine today, which can hinder memory optimizations in both hardware and software.

In this work, we identify important families of workloads, as well as prevalent types of DRAM chips, and rigorously analyze the combined DRAM–workload behavior. To this end, we perform a comprehensive experimental study of the interaction between nine different DRAM types and 115 modern applications and multiprogrammed workloads. We draw 12 key observations from our characterization, enabled in part by our development of new metrics that take into account contention between memory requests due to hardware design. Notably, we find that (1) newer DRAM technologies such as DDR4 and HMC often do not outperform older technologies such as DDR3, due to higher access latencies and, in the case of HMC, poor exploitation of locality; (2) there is no single memory type that can cater to all of the SoC accelerators (e.g., GDDR5 significantly outperforms other media for multimedia, while HMC significantly outperforms other memories for networking); and (3) there is still a strong need to lower DRAM latency, but unfortunately the current design trend of commodity DRAM is toward higher latencies to obtain other benefits. We hope that the trends we identify can drive optimizations in both hardware and software design. To aid further study, we plan to release our extensively-modified simulator, as well as a benchmark suite containing all of our applications.

1 INTRODUCTION

Main memory in modern computing systems is built using Dynamic Random Access Memory (DRAM) technology. As the memory footprint of workloads continues to increase, the performance of DRAM is an increasingly critical factor in overall system and application performance. As modern DRAM designers strive to improve performance and energy efficiency, they must deal with three major issues. First, DRAM consists of capacitive trench cells, and the process to access data from within these DRAM cells requires an access latency that is roughly two orders of magnitude greater than a CPU add instruction [44, 71]. Second, while the impact of long access latency can potentially be overcome by increasing data throughput, DRAM chip throughput is also constrained because conventional DRAM modules are discrete devices that sit off-chip from the CPU, and are connected to the CPU via a narrow, pin-limited bus. For example, Double Data Rate (e.g., DDR3, DDR4) memories exchange data with the CPU using a 64-bit bus. DRAM data throughput can be increased by increasing the DRAM bus frequency and/or the bus pin count, but both of these options incur a significant cost in terms of area and energy. Third, DRAM power consumption is not scaling as the memory density increases. Today, DRAM consumes as much as half of the total power consumption of a system [18, 32, 62, 68, 74, 92, 93]. As a result, the amount of DRAM that can be added to a system is now constrained by its energy consumption.

Further complicating the design space is a large change in the way that applications access memory. Memory systems must now serve an increasingly diverse set of applications, sometimes concurrently. For example, workloads designed for high-performance and cloud computing environments process very large amounts of data that do not always exhibit high reuse or spatial locality. In contrast, network processors exhibit very bursty memory access patterns with low temporal locality. It is becoming increasingly difficult for a single point in the memory design space (i.e., one type of DRAM interface and chip) to perform well under such a diverse set of applications. In response to these key challenges, DRAM manufacturers and standards bodies have been developing a number of different types of DRAM types over the last decade, such as Wide I/O [43] and Wide I/O 2 [45], High-Bandwidth Memory (HBM) [1, 59], and the Hybrid Memory Cube (HMC) [33, 42, 75, 81].

With the increasingly-diversifying application behavior and the wide array of available DRAM types, it has become very difficult to identify the ideal DRAM type for a given workload, let alone for a system that is running a number of workloads. Much of this difficulty lies in the complex interaction between memory access latency, bandwidth, energy consumption, and application memory access patterns. Importantly, changes made by manufacturers in new DRAM types can significantly affect the behavior of an application in ways that are often difficult to intuitively and easily determine. In response, prior work has introduced a number of detailed memory simulators (e.g., [54, 82]) to model the performance of different DRAM types, but this requires end users to set up and simulate each workload that they care about, for each individual DRAM type. Our goal in this work is to comprehensively study the strengths and weaknesses of each DRAM type based on the access patterns of each workload.

Prior studies of memory behavior (e.g., [7, 16, 17, 27, 29, 30, 54, 65, 82, 95, 96]) focus on a single type of workload (e.g., desktop/scientific...
(1) Despite having 50% higher memory bandwidth than DDR3, the newer DDR4 rarely outperforms DDR3 on the applications we evaluate, as DDR4’s access latency is 11–14% higher.

(2) The high-bandwidth HMC does not outperform DDR3 for most single-thread workloads and many multithreaded applications. This is because HMC’s design trade-offs fundamentally limit opportunities for exploiting spatial locality (due to its 97% smaller row width than DDR3), and these applications are unable to exploit the additional bank-level parallelism provided by HMC. For example, single-thread desktop and scientific applications actually perform 5.8% worse with HMC than with DDR3, on average, even though HMC offers 87.4% more memory bandwidth.

(3) While low-power DRAM types typically perform worse than standard-power DRAM for most memory-intensive applications, some of the types perform well when bandwidth demand is very high. For example, on average, LPDDR4 performs only 7.0% worse than DDR3 for multithreaded desktop workloads, while consuming 68.2% less energy. Similarly, we find that Wide I/O 2, another low-power DRAM type, actually performs 2.3% better than DDR3 on average for multimedia applications, as Wide I/O 2 increases I/O parallelism while maintaining low memory access latencies.

(4) The ideal DRAM for a specialized compute device depends heavily on the predominant function(s) performed by the device. Multimedia applications for SoCs benefit most from high-throughput memories with high spatial locality, running up to 21.6% faster with GDDR5 and 14.7% faster with HBM than DDR3, but only 5.0% faster with HMC (due to its limited ability to exploit spatial locality). Network accelerators are highly bursty and do not exhibit significant spatial locality, allowing them to effectively take advantage of HMC’s very high bank-level parallelism (with a mean performance increase of 88.4% over DDR3). GPGPU applications exhibit a wide range of memory intensity, but memory-intensive GPGPU applications typically also take advantage of spatial locality due to memory coalescing [5, 12], making HBM (26.9% higher on average over DDR3) and GDDR5 (39.7%) more effective for GPGPU applications than DRAM types such as DDR3.

(5) Several common OS routines (e.g., file I/O, process forking) exhibit extremely high spatial locality, and do not benefit from high amounts of bank-level parallelism. As a result, they perform better with memories such as DDR3 and GDDR5, which have lower access latencies than the other memory types that we study. Since OS routines are used across most computer systems in a widespread manner, DRAM designers must provide low-latency access, instead of the current trend increasing the latency in order to deliver greater throughput.

We hope and expect that the results of our rigorous experimental characterization will be of broad use to application developers, systems architects, and DRAM architects alike. To foster further work in both academia and industry, we plan to release all 115 applications and multiprogrammed workloads that we study as a new memory benchmark suite, along with our heavily-modified simulator.

This paper makes the following contributions:

- We perform the first comprehensive study of the interaction between modern DRAM types and modern workloads. Our expansive study covers the interactions of 115 applications and workloads from six different application families with nine different DRAM types. We are the first, to our knowledge, to (1) quantify how new DRAM types (e.g., Wide I/O, HMC) compare to commonplace DDRx and LPDDRx DRAM types across a wide variety of workloads, and (2) report surprising findings where newer memories often perform worse than older ones.

- To our knowledge, we are the first to perform a detailed comparison of the memory access behavior between desktop applications, server/cloud workloads, SoC and mobile workloads, GPGPU applications, and OS kernel routines. These insights can help DRAM architects and system designers pinpoint bottlenecks in existing systems, and can inspire new memory and system designs.

- We make several new observations about the combined behavior of various DRAM types and different families of workloads. In particular, we find that new memory types such as DDR4 and HMC make a number of underlying design trade-offs that cause them to perform worse than older DRAM types such as DDR3 for a large number of applications. In order to aid the development of new memory architectures and new system designs based on our observations, we plan to release our extensively-modified memory simulator and a memory benchmark suite consisting of all 115 of our applications and workloads.
2 BACKGROUND & MOTIVATION

In this section, we provide necessary background on basic DRAM design and operation (Section 2.1), and on the evolution of new DRAM types (Section 2.2).

2.1 Basic DRAM Design & Operation

Figure 1 (left) shows the basic overview of a DRAM-based memory system. The memory system is organized in a hierarchical manner. The highest level in the hierarchy is a memory channel. Each channel consists of its own bus to the host (e.g., processor), and has a dedicated memory controller that interfaces between the DRAM and the host device. A channel connects to one or more dual inline memory modules (DIMMs). Each DIMM contains multiple DRAM chips. A DRAM row typically spans across several of these chips, which requires the chips containing the row to perform all operations in lockstep with each other. Each group of chips operating in lockstep is known as a rank. Inside each rank, there are several banks, where each bank is a DRAM array. Each of the banks within a memory channel can operate concurrently, but as the banks share a single memory bus, a memory controller must coordinate operations to keep bank accesses from interfering with each other.

A DRAM bank typically consists of thousands of rows of cells, where each cell contains a capacitor and an access transistor. To start processing a request, the controller issues a command to activate one row (i.e., open the row to perform reads and writes), as shown in Figure 1 (right). The row buffer latches the opened row, at which point the controller sends read and write commands to the row. Each read/write command operates on one column of data at a time. Once the read and write operations to the row are complete, the controller issues a precharge command, to prepare the bank for commands to a different row. For more detail, we refer the reader to [55, 60, 61].

2.2 Modern DRAM Types

We briefly describe several popular and emerging DRAM types, all of which we evaluate in this work. Table 1 summarizes the key properties of each of these DRAM types. We provide more detail about each DRAM type in Appendix A.

- DDR3 and DDR4. DDR3 [44] is the third generation of DDRx memory, where a burst of data is sent on both the positive and negative edge of the bus clock to double the data rate. DDR3 contains eight banks of DRAM in every rank. DDR4 [49] increases the number of banks per rank, to 16, by introducing bank groups, a new level of hierarchy in the memory. Due to the way in which bank groups are connected to I/O, a typical memory access takes longer in DDR4 than it did in DDR3, but the bus clock frequency is significantly faster in DDR4, which increases its bandwidth.

- GDDR5. Similar to DDR4, Graphics DDR5 (GDDR5) [47] memory doubles the number of banks over DDR3 using bank groups. However, unlike DDR4, GDDR5 does so by increasing the die area and energy over DDR3 instead of the memory latency. GDDR5 also increases memory throughput by doubling the amount of data sent in a single clock cycle, as compared to DDR3.

- HBM. High Bandwidth Memory (HBM) [1] is a 3D-stacked memory [59, 66] that provides high throughput for devices such as GPUs. Unlike GDDR5, which uses faster clock frequencies to increase throughput, HBM connects 4–8 memory channels to a single DRAM device to service many more requests in parallel.

- Wide I/O and Wide I/O 2. Wide I/O [43] and Wide I/O 2 [45] are 3D-stacked memories that target low-power devices such as mobile phones. Similar to HBM, Wide I/O and Wide I/O 2 connect multiple channels to a single DRAM device [52], but have fewer (2–4) channels than HBM and contain fewer banks (8) than HBM and GDDR5 in order to lower energy consumption.

- HMC. The Hybrid Memory Cube [33, 42, 75, 81] is a 3D-stacked memory with more radical design changes compared to HBM and Wide I/O. An HMC device (1) performs request scheduling inside the device itself, as opposed to relying on an external memory controller for scheduling; and (2) partitions the DRAM array into multiple vaults, which are small, vertical slices of memory of which each contains multiple banks. Vaults increase the amount of bank-level parallelism significantly inside the DRAM device, but greatly reduce the size of a row (to 256 bytes) due to memory density limitations. The HMC specification [33] provides an alternate mode, which we call HMC-Alt, that attempts to use a different address mapping than the default mapping to maximize the limited locality available in the smaller DRAM rows.

- LPDDR3 and LPDDR4. LPDDR3 [46] and LPDDR4 [48] are low-power variants of DDR3 and DDR4, respectively. These DRAM types lower power consumption by using techniques such as a lower core voltage, two voltage domains on a single chip, temperature-controlled self refresh, deep power-down modes, reduced chip width, and fewer (1–2) chips per DRAM module [69]. These trade-offs increase the memory access latency, and limit the total capacity of the low-power DRAM chip.

![Figure 1: Memory hierarchy (left) and bank structure (right).](image-url)

Table 1: Key properties of the nine DRAM types evaluated in this work.

| DRAM Type | DDR3 | DDR4 | GDDR5 | HBM | HMC | LPDDR3 | LPDDR4 | Wide I/O | Wide I/O 2 |
|-----------|------|------|-------|-----|-----|--------|--------|----------|------------|
| Data Rate (Mi/s) | 2133 | 3200 | 7000 | 1000 | 2500 | 2133 | 3200 | 266 | 1067 |
| Clock Frequency (MHz) | 1067 | 1600 | 1750 | 500 | 1250 | 1067 | 1600 | 266 | 533 |
| Maximum Bandwidth (GBps) | 68.3 | 102.4 | 224.0 | 128.0 | 328.0 | 68.3 | 51.2 | 17.0 | 34.1 |
| Channels/Ranks per Channel | 4/1 | 4/1 | 4/1 | 8/1 | 1/1 | 4/1 | 4/1 | 1/1 | 4/2 |
| Banks per Rank | 8 | 16 | 16 | 16 | 256 (32 vaults) | 8 | 16 | 4 | 8 |
| Channel Width (bits) | 512 | 512 | 512 | 512 | 512 | 512 | 512 | 512 | 512 |
| Row Buffer Size | 8KB | 8KB | 8KB | 8KB | 8KB | 2KB | 2KB | 2KB | 4KB |
| Row Hit/Miss Latencies (ns) | 15.0/26.3 | 16.0/30.0 | 13.0/25.1 | 18.0/32.0 | 18.0/30.4 | 21.6/40.3 | 26.9/45.0 | 30.1/38.9 | 22.5/41.3 |
2.3 Motivation
As DRAM scaling continues to fall behind processor scaling, there is a growing need to improve DRAM performance. Today, conventional DDRx DRAM types suffer from three major bottlenecks. First, prior works have shown that the underlying design used by DDR3 and DDR4 remains largely the same as earlier generations of DDR memory, and as a result, the DRAM access latency has not changed significantly over the last decade [11]. Second, it is becoming increasingly difficult for DRAM vendors to scale up the size of the DRAM array, which in turn limits the density of the memory chip [71]. Third, DDRx connects to the host processor using a narrow, pin-limited off-chip channel, which restricts the available memory bandwidth.

As we describe in Section 2.2, new DRAM types contain a number of key changes to work around these bottlenecks. Due to the non-obvious impact of these changes, there is a need to perform careful characterization of how various workloads perform under each new type, and how this compares to the workload performance under conventional DDRx architectures. Our goal in this paper is to rigorously characterize the complex interactions between these DRAM types and a diverse set of modern applications, through the use of detailed simulation models and new metrics that capture the sources of these interactions.

3 METHODOLOGY
We characterize the nine different DRAM types on 87 different applications [3, 4, 7, 9, 13, 15, 20, 21, 23, 29, 31, 40, 73, 83, 85, 90, 91, 94] and 28 multiprogrammed workloads using a heavily-modified version of Ramulator [54], a detailed and extensible open-source DRAM simulator. We make several modifications to Ramulator to improve the fidelity of our experiments. We describe our modifications, all configuration details, and list all workloads in Appendix B. As we discuss in Appendix B, with our modifications, Ramulator provides near-identical results to a simulator with a detailed, rigorously-validated out-of-order processor core model [8], while being significantly faster. We plan to open-source our modified version of Ramulator.

We collect traces using the Intel Pin dynamic binary instrumentation tool [67] and the Bochs system emulator [57]. For our single-thread and multiprogrammed CPU workloads, we collect traces using system with a four-core Intel Core i7-975k processor [36], and we model this processor in Ramulator. For our multithreaded applications, we collect traces using a system with dual Intel Xeon E5-2630 v4 processors [37], allowing us to execute up to 40 threads concurrently, and we model this processor in Ramulator. We chose system architecture parameters (e.g., miss status holding registers, last-level cache size) such that (1) they are not favorable to any one DRAM type, and (2) they are representative of a modern system.

4 CHARACTERIZATION METRICS
Performance Metrics. We measure single-thread application performance using instructions per cycle (IPC). For multithreaded applications, we show parallel speedup (i.e., the inverse of execution time) to account for synchronization overheads. For multiprogrammed workloads, we use weighted speedup [84], which represents the job throughput [22]. We verify that trends for other metrics (e.g., harmonic speedup) are similar. To quantify the memory intensity of an application, we use the number of misses per kilo-instruction (MPKI) issued by the last-level cache for that application to DRAM.

Our network accelerator workloads were collected from a commercial network processor [73], and thus do not correspond to a traditional processor pipeline. Thus, we instead present performance results for the network accelerator in terms of accelerator bandwidth.

Parallelization Metrics. Prior works have used either memory-level parallelism (MLP) [14, 26, 78, 89] or bank-level parallelism (BLP) [58, 70, 88] to quantify the amount of parallelism across memory requests. Unfortunately, neither metric fully represents the actual parallelism exploited in DRAM. MLP measures the average number of outstanding memory requests for an application, but this does not capture the amount of parallelism offered by the underlying hardware. BLP measures the average number of memory requests that are actively being serviced for a particular thread, to compare parallelism across multiple threads, but BLP does not capture the total bank parallelism exploited by all concurrently-executing threads or hardware limits to bank parallelism.

We define a new metric, called bank parallelism utilization (BPU), which quantifies the average number of banks in main memory that are being used concurrently. To measure BPU, we sample the number of active banks for every cycle that the DRAM is processing a request, and report the average utilization of banks:

$$BPU = \frac{\sum_{i} \#\text{active banks in cycle } i}{\#\text{cycles memory is active}}$$

A larger BPU indicates that applications are making better use of the bank parallelism available in a particular DRAM type. Unlike MLP and BLP, BPU fully accounts for (1) whether requests from any thread are contending with each other for the same bank, and (2) how much parallelism is offered by the memory device. As we see in our analysis, BPU helps explain why some memory-intensive applications do not benefit from high-bandwidth memories such as HMC, while other memory-intensive applications do benefit.

Contention Metrics. An important measure of spatial and temporal locality in memory is the row hit rate. To quantify the row hit rate, prior works count the number of row buffer hits and the number of row buffer misses, which they define as any request that does not hit in the currently-open row. Unfortunately, this categorization does not distinguish between misses where a bank does not have any row open, and misses where a bank is currently processing a request to a different row (i.e., a row buffer conflict). This distinction is important, as a row buffer conflict typically takes longer to service than a row buffer miss, as a conflict must wait to issue a precharge operation, and may also need to wait for an earlier request to the bank to complete. In the worst case, a row buffer conflict takes double the row miss latency, when the conflicting request arrives just after a request with a row miss starts accessing the DRAM.

To accurately capture row buffer locality, we introduce a new characterization where we break down memory requests into: (1) row buffer hits; (2) row buffer misses, which only include misses for a DRAM request where the bank does not have any row open; and (3) row buffer conflicts, which counts the number of misses where another row is currently open in the bank and must be closed (i.e., precharged) first. Row buffer conflicts provide us with important information about how the amount of parallelism exposed by a
DRAM type can limit opportunities to concurrently serve multiple memory requests, which in turn hurts performance.

5 SINGLE-THREAD/MULTIPROGRAMMED DESKTOP AND SCIENTIFIC PROGRAMS

We first study the memory utilization, performance, and DRAM energy consumption of our tested DRAM types on single-thread desktop and scientific applications from the SPEC 2006 benchmark suite [85], and on multiprogrammed bundles of these applications.

5.1 Workload Characteristics

Using the DDR3 memory type, we study the memory intensity of each workload. The workloads encompass a wide range of intensity, with some CPU-bound applications (e.g., games, calculix) issuing memory requests only infrequently, and other memory-bound applications (e.g., mcf) issuing over 15 misses per kiloinstruction (MPKI). The workloads also exhibit a large range of row buffer locality, with hit rates falling anywhere between 2.4–53.1% (see Appendix C.1).

We study the relationship between the performance (IPC) and memory intensity (MPKI) of the desktop and scientific applications (see Appendix C.1 for details and plots). In general, we observe that the IPC decreases as the MPKI increases, but there are two notable exceptions: namd and gobmk. To understand these exceptions, we study the amount of parallelism that an application is able to exploit by using the BPU metric we introduced in Section 4 (see Appendix C.1 for BPU values for all applications). In our configuration, DDR3 has 32 banks spread across four memory channels. For most applications with low memory intensity (i.e., MPKI < 4.0), the BPU for DDR3 is very low (ranging between 1.19 and 2.01) due to the low likelihood of having many concurrent memory requests. The two exceptions are namd and gobmk, which have BPU values of 4.03 and 2.91, respectively. The higher BPU values at low memory intensity imply that these applications exhibit more bursty memory behavior, issuing requests in clusters. Thus, they could benefit more when a DRAM type offers a greater amount of bank parallelism (as opposed to providing higher bandwidth or reduced latency).

From the perspective of memory, we find that there is no discernible difference between applications with predominantly integer computation and applications with predominantly floating point applications (see Appendix C.1). As a result, we do not distinguish between the two in this section.

5.2 Single-Thread Performance

Figure 2 (top) shows the performance of the desktop workloads under each of our standard-power DRAM types, normalized to the performance of each workload when using a DDR3-2133 memory. Along the x-axis, the applications are sorted by MPKI, from least to greatest. We make two observations from these experiments.

OBSERVATION 1: DDR4 does not perform better than DDR3 for the vast majority of our desktop/scientific applications.

As we see in Figure 2 (top), even though DDR4 clocks its memory channel 50% faster than DDR3 and contains double the number of banks, DDR4 performs 0.2% worse than DDR3, on average across all of our desktop and scientific applications. The best improvement is for mcf, with a performance improvement of only 0.5%. We find that both major advantages of DDR4 over DDR3 (i.e., greater bandwidth, more banks) are not useful to our applications. Figure 3 shows the BPU for three representative workloads (libquantum, mcf, and namd). Across all of our applications, we find that there is not enough BPU to take advantage of the 32 DDR3 banks, let alone the 64 DDR4 banks. mcf has the highest BPU, at 5.33 in DDR4, still not enough to benefit from the additional banks. Instead, desktop and scientific applications are sensitive to the memory latency. Figure 4 breaks down the average memory request latency for our representative workloads into two components: (1) the queuing latency (i.e., the amount of time a request waits before the first DRAM command to service that request is issued), and (2) the access latency (i.e., the time between the issuing of the first DRAM command for that request and the completion of the request). As we observe for DDR4, the queuing latency does not change over DDR3, as the applications cannot exploit more parallelism. Instead, applications are hurt by the increased access latency in DDR4, which is a result of the bank group organization (which does not exist in DDR3; see Section 2.2).

OBSERVATION 2: HMC performs significantly worse than DDR3 when a workload without a very high memory intensity can exploit row buffer locality.

From Figure 2 (top), we observe that few standard-power DRAM types can improve performance across all desktop and scientific applications over DDR3. Notably, we find that HMC actually results in significant slowdowns over DDR3 for most of our applications. Averaged across all workloads, HMC performs 5.8% worse than DDR3. To understand why, we examine the row buffer locality of our applications. Recall from Section 2.2 that HMC reduces row buffer locality in exchange for a much greater number of banks (256 in HMC vs. 32 in DDR3) and much greater bandwidth (4.68x the bandwidth of DDR3). We already see in Figure 3 that, with the exception of mcf, HMC cannot provide significant BPU increases for our applications, indicating that the applications cannot take advantage of these benefits.
Figure 2 (bottom) shows the performance of the desktop and scientific applications when we use low-power or mobile DRAM types. In general, we note that as the memory intensity (i.e., MPKI) of an application increases, its performance with low-power memory decreases compared to DDR3. In particular, LPDDR3 and LPDDR4 perform worse because they take longer to complete a memory request, increasing the latency for a row miss over DDR3/4 by 53.6% and 50.0%, respectively. Wide I/O DRAM performs significantly worse than the other DRAM types, as its much lower clock frequency greatly restricts its overall throughput. Wide I/O 2 offers significantly higher row buffer locality than Wide I/O, as shown in Figure 5. As a result, applications such as namd and libquantum, which both exhibit very high spatial locality, perform well under Wide I/O 2.

We conclude that even though single-thread desktop and scientific applications display a wide range of memory access behavior, they generally need DRAM types that offer (1) low access latency and (2) high row buffer locality.

### 5.3 Multiprogrammed Workload Performance

We combine the single-thread workloads into 20 four-core multiprogrammed workloads (see Table 4 in Appendix B.2 for workload details), to study how the memory access behavior changes. Figure 6 shows the performance of the workloads with each DRAM type. Recall from Section 5.2 that HMC did not improve single-thread performance because it was unable to exploit row buffer locality well. For multiprogrammed workloads, HMC performs better than the other DRAM types despite its significantly smaller row width. On average, HMC improves the weighted speedup over DDR3 by 17.0%. Note that while some workloads do very well under HMC (e.g., bundle D7, with a weighted speedup of 83.1%), workloads with lower memory intensity (i.e., MPKI < 80) still perform worse than DDR3 (with the greatest slowdown being 6.3%).

Figure 3: BPU for representative desktop/scientific applications.

Figure 4: Memory request latency breakdown for representative desktop/scientific applications.

Figure 5 shows the row buffer locality (see Section 4) for our three representative applications. As we observe from the figure, HMC eliminates nearly all of the row hits that other memories can attain. This is a direct result of the row size in HMC, which is 97% smaller than the row size in DDR3. This causes many more row misses to occur, without significantly affecting the number of row conflicts that take place. As a result, the average access latency in HMC is 25.6% higher than the DDR3 access latency, as shown in Figure 4. HMC expects that the increased latency due to the greater number of row misses should be offset by the greater number of banks and bandwidth, but poor BPU prevents our applications from being able to do so. The one exception is mcf, which is the only application that sees a significant speedup with HMC (with a 63.4% speedup over DDR3), because its memory access pattern leads to the majority of memory requests being row conflicts in all memory types (see middle graph in Section 5).

Figure 5: Breakdown of row buffer locality for representative single-thread desktop/scientific applications.

Unlike HMC, GDDR5 successfully improves the performance of all of our desktop and scientific applications with higher memory intensity. This is because GDDR5 delivers higher bandwidth without increasing its access latency, as we see in Figure 4. This allows GDDR5 to successfully reduce the queuing latency compared to DDR3, which translates into an average performance improvement of 6.4%. In particular, for applications with high memory intensity (i.e., MPKI > 15.0), GDDR5 has an average speedup of 16.1%, as these applications benefit most from a combination of increased bandwidth and low memory request latencies.

Figure 6: Performance of multiprogrammed desktop and scientific workloads for standard-power (top) and low-power (bottom) DRAM types, normalized to DDR3. MPKI listed in parentheses.
**OBSERVATION 3:** Multiprogrammed workloads with high aggregate memory intensity benefit significantly from HMC, due to a combination of high BPU and poor row buffer locality.

First, the row buffer locality of the multiprogrammed workloads is much lower than the single-thread applications. Figure 7 shows row buffer locality for three representative workloads. For *bundle D9*, which has an MPKI of 167.4, the row buffer hit rate never exceeds 5.6% on any DRAM type. We observe that for all of our workloads, the vast majority of memory accesses are row conflicts. This is because individual applications of the multiprogrammed workloads work in different memory address spaces, and can often induce interference while they compete for banks within the shared DRAM, leading to a much higher rate of conflicts than for single-thread applications.

![Figure 7: Breakdown of row buffer locality for representative multiprogrammed desktop/scientific workloads.](image)

Second, we find that highly-memory-intensive workloads can achieve high BPU values. Figure 8 shows the BPU for the representative workloads. For *bundle D11*, which has an MPKI of 71.3, the workload does not issue enough parallel memory requests, limiting its BPU. For *bundle D7*, which has a much higher MPKI of 229.3, concurrent memory requests are distributed across the memory address space, as three out of the four applications in the workload (*libquantum, mcf, and milc*) are memory intensive. As a result, with HMC, the workload achieves 2.05× the BPU that it does with DDR3.

![Figure 8: BPU for representative multiprogrammed desktop/scientific workloads.](image)

While multiprogrammed workloads perform well under HMC only when the workload is highly memory intensive, GDDR5 can deliver speedups for all 20 of our multiprogrammed workloads. This is because GDDR5 provides a balanced combination of low memory latencies, bank parallelism, and high bandwidth. However, GDDR5’s balance is not enough to maximize the performance of our highly-memory-intensive workloads, and thus its average improvement over DDR3 is lower than HMC, at 13.0%.

From Figure 6 (bottom), we observe that LPDDR4 and Wide I/O 2 perform competitively with DDR3 for highly-memory-intensive workloads. This is because both DRAM types provide high amounts of parallelism, and the high memory intensity allows them to more successfully trade off memory latency for bandwidth.

We conclude that for multiprogrammed workloads, DRAM types that provide high bank parallelism and bandwidth can significantly improve performance when a workload exhibits (1) high memory intensity, (2) high BPU, and (3) poor row buffer locality.

### 5.4 DRAM Energy Consumption

We characterize the energy consumption of our desktop workloads for the DRAM types that we have accurate power models for (i.e., datasheet power values provided by vendors for actual off-the-shelf parts). Figure 9 shows the average DRAM energy consumption by DDR3, DDR4, GDDR5, LPDDR3, and LPDDR4 for our single-thread and multiprogrammed applications, normalized to the energy consumption of DDR3. We make two key observations from the figure.

![Figure 9: Mean DRAM energy consumption for single-thread (left) and multiprogrammed (right) desktop and scientific applications, normalized to DDR3.](image)

**OBSERVATION 4:** LPDDR3/4 can reduce DRAM energy consumption by 54–68% over DDR3/4, but the performance worsens for single-thread applications as the memory intensity increases.

There is a significant difference in the energy consumed by each of the DRAM types. For all of our desktop/scientific workloads, LPDDR3/4 consume significantly less energy than DDR3/4, due to the numerous low-power features incorporated in their design (see Section 2.2). In particular, as we discuss in Appendix D.1, standby power is the largest single source of power consumption for these workloads, and LPDDR3/4 incorporate a number of optimizations to reduce standby power. Unfortunately, as Figure 4 shows, these optimizations lead to increased memory request latencies. This in turn hurts the overall performance of single-thread applications, as we see in Figure 2 (bottom). GDDR5 makes the opposite trade-off, with reduced memory request latencies and higher performance, but at the cost of 2.15× more energy than DDR3 for single-thread applications. Due to the high memory intensity of multiprogrammed workloads, the workloads complete much faster with GDDR5 than DDR3, and thus consumes only 25.6% more energy on average.

**OBSERVATION 5:** For highly-memory-intensive multiprogrammed workloads, LPDDR4 provides significant energy savings over DDR3 without sacrificing performance.

For multiprogrammed workloads, LPDDR4 delivers a 68.2% reduction in energy consumption, on average across all workloads, while losing only 7.0% of the performance of DDR3. This is because LPDDR4 compensates for its higher memory request latency by delivering high bandwidth and having a greater number of banks. As we discuss in Section 5.3, highly-memory-intensive multiprogrammed workloads can achieve a high BPU, which allows them to take advantage of the increased bank parallelism available in DDR4. As a comparison, LPDDR3 still performs poorly with these workloads because it has a lower bandwidth and a lower bank count.

We conclude that (1) the performance improvements of GDDR5 come with a significant energy penalty; and (2) low-power DRAM
variants are effective at reducing overall DRAM energy consumption, especially for applications that exhibit high BPU.

6 MULTITHREADED DESKTOP AND SCIENTIFIC PROGRAMS

Many modern applications, especially in the high-performance computing domain, launch multiple threads on a machine to exploit the parallelism available in multicore systems. We evaluate the following applications:

- blackscholes, canneal, fluidanimate, raytrace, bodytrack, facesim, fregmine, streamcluster, and swaptions from PARSEC 3.0 [7], and
- miniFE, quicksilver, and pennant from CORAL [90]/CORAL-2 [91].

6.1 Workload Characteristics

The multithreaded workloads often work on very large datasets (e.g., several gigabytes in size) that are partitioned across the multiple threads. A major component of multithreaded application behavior is how the application scales with the number of threads. This scalability is typically a function of (1) how memory-bound an application is, (2) how much synchronization must be performed across threads, and (3) how the work done by each thread is balanced.

We provide a detailed experimental analysis of the IPC and MPKI of the multithreaded applications in Appendix C.2. From the analysis, we find that these applications have a narrower IPC range than the single-thread desktop applications. This is often because multithreaded applications are designed to strike a careful balance between computation and memory usage, which is necessary to scale the algorithms to large numbers of threads. Due to this balance, memory-intensive multithreaded applications have significantly higher IPCs compared to single-thread desktop/scientific applications with similar MPKI values, even as we scale the number of threads. For example, the MPKI of miniFE increases from 11.5 with only one thread to 68.1 with 32 threads, but its IPC remains around 1.5, indicating that the application is not completely memory-bound.

6.2 Performance

To study performance and scalability, we evaluate 1, 2, 4, 8, 16, and 32 thread runs of each multithreaded application on each DRAM type. All performance plots show parallel speedup, normalized to one-thread execution on DDR3. For brevity, we do not show individual results for each application. We find that the applications generally break down into one of three categories: (1) memory-agnostic, where the application is able to achieve near-linear speedup across most thread counts and DRAM types; (2) throughput-bound memory-sensitive, where the application is highly memory-intensive, and has trouble approaching linear speedup for most DRAM types; and (3) irregular memory-sensitive, where the application is highly memory-intensive, but its irregular memory access patterns allow it to benefit from either lower memory latency or higher memory throughput.

Six of our applications are memory-agnostic: blackscholes, raytrace, swaptions, quicksilver, pennant, and streamcluster. Figure 10 shows the performance of quicksilver across all thread counts, which is representative of the memory-agnostic applications. Memory-agnostic applications have relatively low MPKI values (Appendix C.2), even at high thread counts, and therefore do not benefit significantly from one DRAM type over another. Because of its somewhat-higher MPKI (20, 9), quicksilver does not have a fully-linear speedup at 32 threads, as we observe in Figure 10. However, we see that the application still scales well regardless of the DRAM type, with no tapering of performance improvements except under Wide I/O (due to its combination of poor access latency and bandwidth). This is because even at high thread counts, several memory-agnostic applications can maintain higher row hit rates, as shown for pennant in Figure 11.

Figure 10: Performance of quicksilver for standard-power (left) and low-power (right) DRAM types, normalized to single-thread performance with DDR3.

Figure 11: Breakdown of row buffer locality for multithreaded applications.

Five of our applications are throughput-bound memory-sensitive: bodytrack, canneal, fluidanimate, facesim, and fregmine. Figure 12 shows the performance of facesim across all thread counts, which is representative of the throughput-bound memory-sensitive applications. These applications become highly memory-intensive (i.e., they have very high MPKI values) at high thread counts. This occurs because as more threads contend for the limited shared space in the last-level cache, the cache hit rate drops, placing greater pressure on the memory system. This has two effects. First, since the memory requests are being generated across multiple threads, where each thread is operating on its own working set of data, there is little spatial locality among the requests that are waiting to be serviced by DRAM at any given time. As we see in Figure 11, facesim does not exploit row buffer locality at 32 threads. Second, because of the high memory intensity of these applications, and due to the poor spatial locality, the applications benefit greatly from a memory like HMC, where locality and latency are sacrificed in order to deliver additional memory-level parallelism. As Figure 12 shows, none of the other memories can scale at the rate that HMC does at higher thread counts, and HMC outperforms even GDDR5 and HBM.

Only one application is irregular memory-sensitive: miniFE. Figure 13 shows the performance of miniFE across all thread counts.
miniFE operates on sparse matrices, which results in irregular memory access patterns that compilers cannot easily optimize. One result of this irregular behavior is low BPU values at all thread counts, corroborating similar observations by prior work [88] for miniFE and other irregular multithreaded workloads. As a result, throughput-oriented memories such as HMC and HBM do not deliver significant benefits, as Figure 13 shows, and miniFE becomes memory-latency bound. Thus, much like our single-thread desktop applications in Section 5, miniFE benefits most from traditional, low-latency memories such as DDR3/4 and GDDR5. In fact, just as we see for memory-agnostic applications, many of the low-power memories outperform HMC and HBM at all thread counts. We do note that as the core count increases, miniFE benefits more from high memory throughput and high bank-level parallelism. As a result, while the performance with memories such as GDDR5 and HBM levels off after 16 threads, the performance with HMC continues to scale well.

**Observation 6:** For multithreaded applications with irregular memory access patterns, low-latency memories such as DDR3/4 outperform throughput-oriented memories such as HMC and HBM. These applications can also make effective use of low-power DRAM without sacrificing significant performance.

We conclude that the ideal DRAM type for a multithreaded application is highly dependent on the application behavior, and that for many such applications, such as memory-agnostic or irregular memory-sensitive applications, low-power DRAM types provide a promising alternative to standard-power memories without sacrificing performance.

### 7 Server and Cloud Workloads

Server and cloud workloads are designed to accommodate very large data sets, and can often coordinate requests between multiple machines across a network. We evaluate the following workloads with representative inputs:

- the `map` and `reduce` tasks [19] for `grep`, `wordcount`, and `sort`, implemented using Hadoop [3] for scalable distributed processing;
- YCSB [15] OLTP (OnLine Transaction Processing) server workloads A–E, and the background process forked by workload A to write the log to disk (`bgsave`), executing on the Redis in-memory key-value store [94],
- an Apache server [4], which services a series of `wget` requests from a remote server;
- Memcached [21], using a microbenchmark that inserts key-value pairs into a memory cache; and
- the MySQL database [20], using a microbenchmark that loads the sample `employeedb` database.

#### 7.1 Workload Characteristics

From our analysis, we find that while server and cloud workloads tend to work on very large datasets (e.g., gigabytes of data), the workloads are written to maximize the efficiency of their on-chip cache utilization. As a result, these applications only infrequently issue requests to DRAM, and typically exhibit low memory intensity (i.e., MPKI < 10) and high IPCs. We show IPC plots in Appendix C.3.

#### 7.2 Single-Thread Performance

Figure 14 shows the performance of single-thread workloads for server and cloud environments when run on our evaluated DRAM types, normalized to DDR3. We find that none of our workloads benefit significantly from using HBM, HMC, or Wide I/O 2. These DRAM types sacrifice DRAM latency to provide high throughput. Since our workloads have low memory utilization, they are unable to benefit significantly from this additional throughput.

**Observation 7:** Due to their low memory intensity and poor BPU, most of the server and cloud workloads that we study do not benefit significantly from high-throughput memories.

To understand why high-throughput memories do not benefit these applications, we focus on YCSB (the leftmost six workloads in Figure 14). For these workloads, we observe that as the memory
intensity increases, HMC performs increasingly worse compared to DDR3. We find that the YCSB workloads exhibit low BPU values (never exceeding 1.80). Figure 15 shows the BPU (left) and row buffer locality (right) for workload A: server, as a representative YCSB workload. We observe that HBM, HMC, and Wide I/O cannot improve on the workload’s poor BPU, eliminating the DRAM types’ advantages. HMC also destroys the row hits (and, thus, lower access latencies) that other DRAM types provide, resulting in a significant slowdown of 11.6% over DDR3, on average across the YCSB workloads. HMC only avoids slowdowns for applications such as the map process for grep, which demonstrates high BPU (18.3; not shown), but such BPU values are not typical for server and cloud workloads.

![Figure 15: BPU (left) and row buffer locality (right) of workload A: server.](image)

We find that due to the low memory intensity and BPU, server and cloud workloads are highly sensitive to memory request latency, as the limited memory-level parallelism can cause a single long-latency memory request to stall the processor pipeline [24]. One advantage to the low memory intensity is that it limits the slowdowns of LPDDR3/4, since there is no need to provide high throughput to these applications.

7.3 Multiprogrammed Performance

Figure 16 shows the performance of executing four-core multiprogrammed workloads for our YCSB and Hadoop applications with each DRAM type. These workloads are assembled by randomly selecting bundles of the single-thread applications and executing them concurrently. We make two findings from the figure.

First, much like single-thread YCSB, the multiprogrammed YCSB workloads continue to see little benefit from high-throughput memories. One exception is GDDR5, where YCSB is able to attain a mean speedup of 10.2% over DDR3 due to the increased memory intensity of the multiprogrammed workloads. On low-power DRAM types, YCSB sees even worse performance than it did in the single-thread case, with its performance ranging between 14.5% and 17.2% lower with LPDDR3, LPDDR4, and Wide I/O 2 than DDR3. Wide I/O fares even worse, with an average performance drop of 33.3%

For Hadoop, we find that the working sets of each application within the workload begin to conflict with each other in the cache, in turn increasing the last-level cache miss rate and significantly increasing the memory intensity with respect to the single-thread applications. As a result, the queuing latency of the workloads begins to make up a significant fraction of the DRAM access latency. For workload H0 on DDR3, queuing accounts for 78.2% of the total DRAM access latency (not shown). As we saw with the multiprogrammed desktop workloads in Section 5.3, HMC is able to alleviate queuing significantly for the multiprogrammed Hadoop workloads compared to DDR3, on average achieving 2.62× the BPU, with an average performance improvement of 9.3%.

7.4 DRAM Energy Consumption

**Observation 8:** For server and cloud workloads, LPDDR3 and LPDDR4 greatly minimize standby power consumption without imposing a large performance penalty.

Figure 17 shows the DRAM energy consumption for the single-thread and multiprogrammed server and cloud workloads. As we found for the desktop workloads, GDDR5 consumes a significant amount of energy, and is especially unsuitable for a datacenter setting, where energy is a critical resource. In contrast, we find that LPDDR3 and LPDDR4, despite showing only small performance degradations with respect to DDR3, save a significant amount of DRAM energy (ranging between 60% and 70%). We believe this makes LPDDR3 and LPDDR4 very competitive candidates for the server and cloud environments, as they have much higher memory energy efficiency than DDR3 offers, without a high impact on response time.

![Figure 17: Mean DRAM energy consumption for single-thread (left) and multiprogrammed (right) server/cloud applications, normalized to DDR3.](image)

8 HETEROGENEOUS SYSTEM WORKLOADS

In this section, we study the performance and energy consumption of workloads that are representative of three major types of processors and accelerators in heterogeneous systems, such as systems-on-chip (SoCs) and mobile processors: (1) multimedia acceleration, which we approximate using benchmarks from the Mediabench II suite for
JPEG and H.264 video encoding and decoding [23]; (2) network acceleration, for which we use data collected from a commercial network processor [73]; and (3) general-purpose GPU (GPGPU) workloads.

8.1 Multimedia Workloads

Multimedia accelerators are designed to perform high-throughput parallel operations on media content, such as video, audio, and image processing [23]. Often, the content is encoded or decoded in a streaming manner, where pieces of the content are accessed from memory and processed in order. Multimedia accelerators typically work one file at a time, and tend to exhibit high spatial locality due to the streaming behavior of their algorithms. The algorithms we explore are often bound by the time required to encode or decode each piece. We find that for JPEG processing and H.264 encoding, the applications are highly compute-bound (i.e., MPKI < 5.0), and exhibit very slow streaming behavior. However, H.264 decoding exhibits a highly memory-bound streaming behavior, with an MPKI of 124.5.

OBSERVATION 9: While compute-bound multimedia applications are memory agnostic, multimedia applications with high memory intensity benefit from high-throughput DRAM types with wide rows.

Figure 18 shows the performance of the multimedia applications on each DRAM type, normalized to DDR3. Due to their low memory intensity, JPEG encoding/decoding and H.264 encoding do not benefit from any of the high-throughput DRAM types, and are actually hurt significantly by HMC, due to HMC’s small row size and high access latencies. In contrast, the larger row width of Wide I/O 2 allows these applications to experience modest speedups, by increasing the row hit rate.

![Figure 18: Performance of multimedia applications for standard-power (left) and low-power (right) DRAM types, normalized to performance with DDR3. MPKI listed in parentheses.](image)

Unlike the other applications, H.264 decoding performs significantly better with high-throughput memories, due to its high memory intensity. For example, GDDR5 improves the performance of H.264 decoding by 21.6% over DDR3, and HBM improves performance by 14.7%. However, due to its streaming nature, H.264 decoding still relies heavily on DRAM types with wide rows, which can take advantage of spatial locality. As a result, HMC does not provide large performance improvements over DDR3, despite increasing the BPU by 177.2%. The streaming behavior is heavily localized, which results in DDR4 hurting its performance by 2.6% over DDR3. This is because the highly-localized streams cannot distribute memory requests across the additional DDR4 banks, evidenced by the fact that the BPU actually decreases by 3.2% over DDR3.

8.2 Network Accelerators

The network accelerators we study handle a number of data processing tasks (e.g., processing network packets, handling any required responses, storing the data in an application buffer). Such network accelerators can be found in dedicated network processing chips and in SoCs [73]. Unlike multimedia accelerators, which exhibit regular streaming access patterns, network accelerator memory access patterns are dependent on the rate of incoming network traffic. A network accelerator monitors traffic entering from the network adapter, performs depacketization and error correction, and transfers the data to the main memory system. As a result of its dependency on incoming network traffic, the network accelerator exhibits highly bursty behavior, where it occasionally writes to DRAM, but has a high memory intensity during each write burst.

OBSERVATION 10: Network accelerators experience very high queuing latencies at DRAM even at low MPKI, and benefit greatly from a high-throughput DRAM such as HMC.

Figure 19 shows the throughput of the network accelerators normalized to DDR3. We sweep the number of network accelerator requests that are allowed to be in flight at any given time, to emulate different network injection rates. We find that the network accelerator workloads behave much differently than our other applications. Thanks to the highly-bursty nature of the memory requests, the queuing latency accounts for 62.1% of the total request latency, averaged across our workloads. Here, HMC’s combination of high available bandwidth and a very large number of banks allows it to increase the BPU by 2.28× over DDR3, averaged across all of our workloads. This reduces the average queuing latency by 91.9%, leading to an average performance improvement of 63.3%. HMC-Alt combines HMC’s low queuing latencies with improved locality, which is amenable to the multi-cache-line size of network packets. As a result, HMC-Alt performs 88.4% better than DDR3, on average.

![Figure 19: Network accelerator bandwidth (BW) for standard-power (left) and low-power (right) DRAM types, normalized to BW with DDR3. MPKI listed in parentheses.](image)

We conclude that SoC accelerators can benefit significantly from high-throughput memories (e.g., HMC, GDDR5), but that the diverse behavior of the different accelerators makes it difficult to identify a single DRAM type that performs best across the board.
8.3 GPGPU Applications

Figure 20 shows the performance of several GPGPU applications. We study ten applications from the Mars [29], Rodinia [13], and Lonestar [9] suites. These applications have MPKIs ranging from 0.005 (dmr) to 25.3 (sp).

![Figure 20: Performance of GPGPU applications for standard-power (left) and low-power (right) DRAM types, normalized to DDR3. MPKI in parentheses.](image)

Overall, we find that for our applications that are not memory intensive (MPKI < 1, as GPUs issue many more instructions per cycle than a CPU), all of our DRAM types perform near identically. Six of our applications are memory intensive, and benefit significantly from executing on a system with HBM or GDDR5 memory. On average, the IPC of memory-intensive GPGPU applications increases over DDR3 by 26.9% for HBM, and by 39.7% for GDDR5. Unlike the other applications that we study, the memory-intensive GPGPU applications also see significant performance improvements with DDR4 over DDR3, with an average performance improvement of 16.4%.

A large reason for the high speedups is the ability of these applications to take advantage of memory coalescing [5, 12]. In a GPU, the memory controller coalesces (i.e., combines) multiple memory requests that target nearby locations in memory into a single memory request. This is particularly useful for GPU and GPGPU applications, where a large number of threads operate in lockstep, and often operate on neighboring pieces of data. Memory coalescing exploits the spatial locality between multiple threads, in order to reduce pressure on the memory system and reduce queuing delays. The coalesced memory requests take significant advantage of the high bandwidth available in GDDR5, and the additional bank parallelism available in DDR4. Coalescing is particularly helpful for sp, where the memory requests are highly bound by the available memory bandwidth [56]. This leads to very high speedups on GDDR5 (253.6%) for the application over DDR3.

Unlike the other memory-intensive applications, memory requests from sp are typically not coalesced [12] (i.e., requests from multiple threads cannot be combined easily to exploit locality). This causes the application to issue many requests at once, forcing it to require both high throughput and high bank-level parallelism. As a result, sp takes advantage of the high bank-level parallelism available at a low access latency in HBM, causing HBM to outperform GDDR5 by 8.3%.

8.4 DRAM Energy Consumption

OBSERVATION 11: For accelerators with high memory throughput requirements, GDDR5 provides much higher performance than DDR3 without consuming additional energy.

Figure 21 shows the normalized energy consumption for the accelerators. We find that GDDR5 actually consumes approximately the same amount of energy as DDR3 whenever the memory throughput required by the accelerator is high (e.g., H.264 decode, network). This is in stark contrast to the observations in Sections 5.4 and 7.4, where GDDR5 consumed significantly greater energy. We find that such accelerators are most energy efficient with a combination of high memory throughput and high spatial locality. This makes the accelerators ideal for GDDR5, as they make efficient use of the additional energy required to clock the memory faster.

![Figure 21: Mean DRAM energy consumption for multimedia (left) and network (right) acceleration, normalized to DDR3.](image)

9 OS KERNEL MICROBENCHMARKS

We collect several traces capturing common OS activities of kernel-mode behavior for different benchmarks:

- **iozone** [40], a file system benchmark suite that tests a number of I/O performance tasks (Tests 0–12);
- **Netperf** [31], which tests TCP/UDP network calls (UDP_RR, UDP_STREAM, TCP_RR, TCP_STREAM);
- **bootup** [83], a representative phase of the boot operation in the Debian operating system;
- **forkbench** [83], a microbenchmark trace that creates a 64MB array of random values, forks itself, and has its child process update 1K random pages; and
- **shell** [83], a microbenchmark trace of a Unix shell script that runs find on a directory tree and executes 1s on each subdirectory.

9.1 Workload Characteristics

While the OS routines that we study perform a variety of different tasks, we find that they exhibit very similar behavior. We study the row buffer locality of the routines with DDR3 DRAM, as shown in Figure 22. We find that most of the routines have exceptionally high row buffer locality, with row buffer hit rates greater than 75%. This behavior occurs because many of the OS routines are based on files and file-like structures, with these files often being read or written in large sequential blocks. This causes the routines to access most, if not all, of the data mapped to an OS page (and therefore to the open DRAM row). We also observe that these requests reach the DRAM at regular time intervals, which, as a result, reduces the throughput burden on DRAM.
9.2 Performance

Figure 23 shows the performance of the OS routines on standard-power DRAM types, normalized to their performance under DDR3. (We discuss low-power DRAM types in Appendix C.4.) We find that the overall performance of the routines is similar to the performance observed for server and cloud workloads (see Section 7.2), where only GDDR5 memory outperforms DDR3 for the majority of routines. The other high-throughput memories are unable to significantly improve the performance, and in many cases actually hurt performance.

Figure 22: DDR3 row buffer locality for OS routines.

Figure 23: Performance of common OS routines for standard-power DRAM types, normalized to performance with DDR3. MPKI listed in parentheses.

OBSERVATION 12: OS routines benefit most from DRAM types with low access latencies that exploit spatial locality (e.g., GDDR5).

The root cause of this is the serialized access behavior of most of the routines, which when combined with the regular time intervals between DRAM requests (see Section 9.1) prevents excessive queuing in DRAM. This behavior causes high-throughput DRAM types to suffer in terms of performance, as they require larger access latencies and, in the case of HMC, sacrifice row buffer locality to alleviate queuing bottlenecks. As we show in Figure 23, if we employ our locality-aware addressing mode for HMC (HMC-Alt), the performance of HMC improves for some (but not all) of the routines. GDDR5 provides the highest performance across all OS routines because it achieves high throughput without sacrificing the access latency of the DRAM.

9.3 DRAM Energy Consumption

Due to space limitations, we summarize our DRAM energy characterization for OS routines in this section, and provide a detailed analysis in Appendix D.2. Though their performance differs significantly, we find that the DRAM energy consumption of the routines is very similar to the trends that we observed for desktop workloads in Section 5.4. Without a large average improvement in performance, GDDR5 consumes 2.1x more energy than DDR3, while LPDDR4 consumes only 42.0% of the energy of DDR3. Due to the low memory intensity and high locality of the OS routines, LPDDR4 incurs a much smaller average performance loss (9.6%; see Appendix C.4) over DDR3 for OS routines than for desktop applications.

10 RELATED WORK

To our knowledge, this is the first work to uncover new trends about and interactions between different DRAM types and the performance and energy consumption of modern workloads. We do so by developing accurate, efficient modeling tools, and by incorporating new metrics that capture low-level interactions in hardware. No prior work presents a comprehensive study across such a wide variety of workloads and DRAM types. We briefly discuss the most closely related works.

Cuppu et al. [16] present a holistic view of several DRAM types. Their work, almost two decades old now, noted several characteristics emerging from then-contemporary DRAM designs, and made recommendations based on these insights. Zhu and Zhang [96] study how various DRAM types can be optimized to work with SMT processors, but do not perform a broad characterization. Zheng and Zhu [95] compare the performance of DDR3 DRAM to DDR2 and FB-DIMM. Gomony et al. [27] characterize DRAM types for mobile systems, and propose a tool to select the right type for real-time mobile systems. All of these studies predate the emergence of many of the DRAM types that we characterize, do not evaluate energy consumption, and focus only on a limited set of applications. Li et al. [65] evaluate the performance and power of several modern DRAM types, including HMC and HBM, but do so for only 10 desktop and scientific applications. Furthermore, their memory configuration uses row interleaving, which reduces the memory-level parallelism compared to modern systems that use line interleaving [50, 55].

Several works study the impact of memory controller policies on performance. Notably, Rixner et al. [80] explore the impact of various scheduling policies. Many subsequent works explore new scheduling policies (e.g., [24, 41, 53, 70]); these works are orthogonal to our study, which keeps controller policies constant and explores the effect of the underlying DRAM type. Other works have profiled the low-level behavior of DRAM types by characterizing real DIMMs (e.g., [11, 60]), but these works focus on a single DRAM type (DDR3), and do not use real-world applications to perform their characterization.

A number of works study the memory access behavior of benchmark suites (e.g., [7, 29, 30]). These works focus on only a single DRAM type. Conversely, several works on DRAM simulation study the memory access behavior of a limited set of workloads on several memory types [2, 25, 54, 64, 79, 82, 87]. None of these studies (1) take a comprehensive and widespread look at the range of workloads and DRAM types as we do, or (2) evaluate energy consumption.

11 CONCLUSION

Due to the emergence of many new DRAM types, each catering to different target objectives, and of new applications that are often data-intensive, it has become very difficult to intuitively understand how a particular performs with a particular DRAM type. This is because of the complex interaction between memory latency, throughput, energy consumption, and memory access patterns. In this work, we perform a comprehensive experimental study to analyze these
interactions, by characterizing the behavior of 115 applications and workloads with nine DRAM types. With the help of new metrics that capture the interaction between memory requests and hardware-level contention, we make 12 key observations about the combined DRAM—workload behavior. We hope that our observations can inspire many memory optimizations in both hardware and software. We plan to release our extensively-modified simulator and a benchmark suite with all 115 applications to help foster further studies.

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APPENDIX

A  BACKGROUND ON MODERN DRAM TYPES

**DDR3.** Double Data Rate (DDR3) [44] memory is the third generation of DDR DRAM. Each rank in DDR3 consists of eight banks, which at a high level allows eight memory requests to be performed in parallel in a rank. All of the banks share a single memory channel, and the memory controller must synchronize parallel memory requests to ensure that each read request has exclusive access to the channel when the request response is being sent from DRAM to the processor. In order to reduce memory channel contention and increase memory throughput, DDR3 transmits data on both the positive and negative edges of the bus clock, which doubles the data rate by allowing a data burst (i.e., a piece of data) to be transmitted in only half a clock cycle. In DDR3, eight 64-bit data bursts are required for each 64-byte read request [44]. DDR3 was first released in 2007 [44], but continues to be one of the most popular types of DRAM available on the market today due to its low cost. However, with the limited number of banks per rank, along with the monolithic approach to banking (i.e., each bank is an equal peer in the structural hierarchy), manufacturers no longer aggressively increase the density of DDR3 memories.

**DDR4.** DDR4 [49] has evolved from the DDR3 DRAM type as a response to solving some of the issues of earlier DDR designs. A major barrier to DRAM scalability is the eight-bank design used in DDR3 memories, as it is becoming more difficult to increase the size of the DRAM array within each bank. In response to this, DDR4 employs bank groups [49], which enable DDR4 to double the number of banks in a cost-effective manner. A bank group represents a new level of hierarchy, where it is faster to access two banks in two different bank groups than it is to access two banks within the same group. This is a result of the additional I/O sharing that takes place within a bank group. One drawback of the DDR4 implementation of bank groups is that the average memory access takes longer in DDR4 than it did in DDR3. DRAM vendors make the trade-off of having additional bank-level parallelism and higher bus throughput in DDR4, which can potentially offset the latency increase when an application effectively exploits bank-level parallelism.

**GDDR5.** Like DDR4, Graphics DDR5 (GDDR5) [47] memory uses bank groups to double the number of banks. However, GDDR5 does so without increasing memory latency, instead increasing the die area and energy. Due to these additional costs, GDDR5 is currently unable to support the memory densities available in DDR4. GDDR5 increase memory throughput significantly over DDR3 by quad pumping its data (i.e., it effectively sends four pieces of data in a single clock cycle, as opposed to the two pieces sent by DDR3) [47]. In addition, GDDR5 memories are clocked at a faster frequency. This aggressive throughput is especially helpful for the GPUs that tend to use GDDR5 memory, as they often perform many data-parallel operations that require a high memory throughput.

**3D-Stacked DRAM.** Thanks to recent innovations in circuit lithography, manufacturers are now able to build 3D-stacked memories, where multiple layers of DRAM are stacked on top of one another. A major advantage of 3D stacking is the availability of through-silicon vias [59, 66], vertical interconnects that provide a high-bandwidth interface across the layers. The High Bandwidth Memory (HBM), Wide I/O, and Wide I/O 2 DRAM types exploit 3D stacking for different purposes. HBM [1] is a response to the need for improved memory bandwidth for GPUs without the high power costs associated with GDDR5. HBM DRAM is clocked much slower than GDDR5, but connects four to eight memory channels to a single DRAM device. The large number of memory channels allows each HBM device to service a large number of requests in parallel without I/O contention. Wide I/O [43] and Wide I/O 2 [45] apply the same principle while targeting low-power devices (e.g., mobile phones) [52]. As mobile devices are not expected to require as much throughput as GPUs, Wide I/O and Wide I/O 2 have fewer memory channels connected to each stack, and use fewer banks than HBM and GDDR5.

The Hybrid Memory Cube (HMC) [33, 42, 75, 81] makes more radical changes to the memory design. HMC is a 3D-stacked memory designed to maximize the amount of parallelism that DRAM can deliver, with the trade-off that a significant increase in throughput can offset the penalties associated with increasing the parallelism. Instead of employing a traditional on-chip memory controller, a processor using an HMC device simply sends requests in FIFO order to the memory, over a high-speed serial link, and performs scheduling in a dedicated logic layer inside the memory. Unlike other DRAM types, all scheduling constraints in HMC are handled within the memory itself. To keep this scheduling logic manageable, HMC partitions its DRAM into multiple vaults, which consist of a small, multi-bank vertical slice of memory. As part of the move to vaults, HMC reduces the size of each row in memory from the typical 4–8 kB down to 256 bytes.

**LPDDR3 and LPDDR4.** In order to decrease the power consumed by DDR DRAM, manufacturers have created low-power (LP) variants, known as LPDDR3 and LPDDR4. LPDDR3 [46] reduces power over DDR3 by using a lower core voltage, employing deep power-down modes, and reducing the number of chips used in each DRAM module. One drawback of the lower core voltage and the deep power-down mode is that memory accesses take significantly longer on low-power memories (see Table 1). LPDDR4 [48] achieves even greater power savings by cutting the width of each chip in half with respect to LPDDR3. A smaller chip consumes less power, but this requires LPDDR4 to perform double the number of data bursts for each request.

B  DETAILED CHARACTERIZATION

**METHODOLOGY**

**B.1 Modeling Tools**

We characterize the different DRAM architectures using a heavily-modified version of Ramulator [54]. Ramulator is a detailed and extensible DRAM simulator. We make several modifications to Ramulator to improve the fidelity of our experiments. First, we implement a shared last-level cache, to ensure that the initial contention between memory requests from different cores takes place before the requests reach memory, just as they would in a real computer. Second, we add support for virtual-to-physical address translation. Third, we implement a faithful model of HMC version 2.1 [33]. Our model accurately replicates the high-speed serial link in HMC, and includes a logic layer where DRAM commands are scheduled.
Table 2 shows the system configuration parameters. For all of the memories, we use the widely-used FR-FCFS memory scheduler [80, 97], with 32-entry read and write queues. We use cache line interleaving [50, 55] for the physical address, where consecutive cache lines are interleaved across multiple channels to maximize the amount of memory-level parallelism. Cache line interleaving is used by processors such as the Intel Core [38], Intel Xeon [39, 63], and IBM POWER9 [34] series. For each architecture currently in production, we select the fastest frequency variant of the architecture on the market today, as we can procure reliable latency and power information for these products. As timing parameters for HMC have yet to be publicly released, we use the information provided in prior work [42, 51] to model the latencies.

Table 2: Evaluated system configuration.

| Processor | x86-64 ISA, 128-entry instruction window, 4-wide issue single-thread/multiprogrammed: 4 cores, 4.0 GHz | multithreaded: 20 cores, 2 threads per core, 2.2 GHz |
|-----------|---------------------------------------------------------------------------------------------------|-------------------------------------------------|
| Caches    | per-core L1: 64kB, 4-way set associative per-core L2: 256kB, 4-way set associative | shared L3: 2 MB for every core, 8-way set associative |
| Memory Controller | 32/128-entry read/write request queues, FR-FCFS [80, 97], cache line interleaving |

Our modifications allow us to use the simple core model built into Ramulator, as opposed to using a detailed CPU timing simulator, without losing accuracy. We simulate a 4 GHz, 4-issue processor with a 128-entry reorder buffer, and an 8MB, 8-way set associative shared last-level cache. We validate our results by comparing the simple core model results to results generated when we combine Ramulator with gem5 [8]. We find that normalized results from our simple core model differ by only 6.1% from the gem5 results, and that the relative trends are identical between the two. We will release our modified and validated version of Ramulator at the time of publication.

**Power Modeling.** We integrate DRAMPower [10], an open-source DRAM power profiling tool, into Ramulator such that it can perform power profiling while Ramulator executes. To isolate the effects of DRAM behavior, we focus on the power consumed by DRAM instead of total system power. We perform power profiling for all of our DRAM architectures where vendors have publicly released power consumption specifications, to ensure the accuracy of the results that we present.

### B.2 Workloads

We study 87 different applications, spread over a diverse range of uses. In our characterization, we categorize our applications into one of six families: desktop/scientific [7, 85, 90, 91], server/cloud [3, 4, 15, 20, 21, 94], multimedia [23], network [73], GPGPU [9, 13, 29], and OS routines [31, 40, 83]. We study the categories one at a time, and describe the applications belonging to each category in the beginning of each section. These applications have been collected from a wide variety of sources. Table 3 lists all of our evaluated applications.

Aside from our GPGPU applications, we collect detailed CPU traces of each application, which capture the delays incurred by each CPU instruction during execution, and replay these traces with our core model in Ramulator. For the majority of our applications, we collect per-core traces using Intel’s Pin [67], which uses dynamic binary instrumentation to capture CPU behavior. These traces were collected using a machine containing an Intel Core i7-975K processor [36] and running Ubuntu Server 14.04. Our network accelerator workloads were collected from a commercial network processor [73].

In order to accurately capture the behavior of multithreaded applications, we make use of a modified Pintool [76], which accurately captures synchronization behavior across threads. We modify this Pintool to capture traces that are compatible with Ramulator, and to capture an independent trace per thread. In order to test the scalability of the multithreaded applications that we study [7, 90, 91], we run the applications and our modified Pintool on a machine that contains dual Intel Xeon E5-2630 v4 processors [37], providing us with the ability to execute 40 threads concurrently. These machines run Ubuntu Server 14.04, and contain 128 GB of DRAM. We plan to release our modified Pintool along with our modified version of Ramulator.

One limitation of using Pin is that it cannot capture kernel-level operations. Though prior studies often overlook kernel-level behavior, recent studies reveal that many programs spend most of their execution time in kernel mode [77, 86]. Thus, to capture this behavior, we use the Bochs full system emulator [57] to collect traces of OS kernel routines, as well as traces for kernel-mode-heavy applications (e.g., Apache, memcached, and MySQL). As we are constrained to using the processor models available in Bochs, we choose the Intel Core i7-2600K [35], which is the closest available to the i7-975K processor [36] we used with Pin. The emulator runs the Ubuntu Server 16.04 operating system.

We run our workloads to completion, with two exceptions. For our desktop benchmarks, we identify a representative phase of execution using Simpoint [28]. During simulation, we warm-up the caches for 100 million instructions, and then run a 1-billion instruction representative phase. For Netperf, we emulate 10 real-world seconds of execution time for each benchmark.

In addition to our 87 applications listed in Table 3, we assemble 28 multiprogrammed workloads for our desktop (Table 4) and server/cloud (Table 5) applications by selecting bundles of four applications to represent varying levels of memory intensity. To ensure that we accurately capture system-level contention, we restart any applications that finish until all applications in the bundle complete. Note that we stop collecting statistics for an application once it has restarted.
Table 4: Multiprogrammed workloads of desktop and scientific applications. For each application, we indicate what fraction of the applications in the workload are memory intensive (i.e., MPKI > 15.0).

| Name  | Applications in Workload | % Mem Intensive |
|-------|--------------------------|-----------------|
| bundle D0 | mill, GemsFDTD, mf, libquantum | 100% |
| bundle D1 | bware, omnetpp, mf, libquantum | 100% |
| bundle D2 | libquantum, bware, soplex, GemsFDTD | 100% |
| bundle D3 | soplex, mf, omnetpp, mill | 100% |
| bundle D4 | mf, mf, GemsFDTD, h264ref | 75% |
| bundle D5 | soplex, omnetpp, mill, namd | 75% |
| bundle D6 | libquantum, omnetpp, bware, povray | 75% |
| bundle D7 | libquantum, mf, mill, zeusmp | 75% |
| bundle D8 | omnetpp, GemsFDTD, cactusADM, hmer | 50% |
| bundle D9 | GemsFDTD, mf, games, zeusmp | 50% |
| bundle D10 | mf, mf, bejw2, h264ref | 50% |
| bundle D11 | bware, soplex, games, namd | 50% |
| bundle D12 | omnetpp, seng, namd, gcc | 25% |
| bundle D13 | GemsFDTD, hmer, zeusmp, astar | 25% |
| bundle D14 | GemsFDTD, povray, sphinx3, calculix | 25% |
| bundle D15 | soplex, zeusmp, sphinx3, gcc | 25% |
| bundle D16 | povray, astar, gobmk, perlbench | 0% |
| bundle D17 | povray, bejw2, sphinx3, cactusADM | 0% |
| bundle D18 | astar, seng, gcc, cactusADM | 0% |
| bundle D19 | calculix, namd, perlbench, games | 0% |

Table 5: Multiprogrammed workloads of server and cloud applications.

- **YCSB + Redis**
  - bundle Y0: workload A: server, workload B: server, workload C: server, workload D: server
  - bundle Y1: workload A: server, workload B: server, workload C: server, workload D: server
  - bundle Y2: workload A: server, workload B: server, workload C: server, workload D: server
  - bundle Y3: workload A: server, workload B: server, workload C: server, workload D: server

- **Hadoop**
  - bundle H0: four grep: map processes with different inputs
  - bundle H1: four wc: count: map processes with different inputs
  - bundle H2: four sort: map processes with different inputs

For GPGPU applications, we integrate Ramulator into GPGPU-Sim [5], and execute the applications using the NVIDIA GeForce GTX 480 [72] configuration. We execute each GPGPU application until the application completes, or until the GPU executes 100 million instructions. We plan to open-source our integrated version of GPGPU-Sim and Ramulator.

C.1 Single-Thread Desktop/Scientific Applications

Figure 24 shows the instructions per cycle (IPC) for each of the desktop applications when run on a system with DDR3 memory. The benchmarks along the x-axis are sorted in ascending order of MPKI (i.e., memory intensity). As we discuss in Section 5.1, our desktop applications consist of both applications with predominantly integer computations and applications with predominantly floating point computations. Prior work shows that when the CPU, there is a notable difference in the behavior of integer applications (typically desktop and/or business applications) from floating point applications (typically scientific applications) [30]. From Figure 24, we observe that the performance of the two groups is interspersed throughout the range of MPKIs and IPCs. Thus, we conclude that there is no discernible difference between integer and floating point applications, from the perspective of memory.

Figure 24: IPC for desktop and scientific applications executing on a system with DDR3-2133 memory. In parentheses, each benchmark includes its MPKI, and whether the benchmark consists of predominantly integer (INT) or floating point (FP) operations.

We observe from Figure 24 that the overall IPC of desktop and scientific applications decreases as the MPKI increases in general, but that there are two notable exceptions: namd and gobmk. We discuss how these exceptions are the result of bank parallelism utilization (BPU) in Section 5.1. Figure 25 shows the BPU of each application when run with the DDR3 DRAM type. Note that our DDR3 configuration, with four channels, and eight banks per channel, has a total of 32 banks available. Thus, the theoretical maximum BPU is 32, though this does not account for (1) request serialization for banks that share a shared memory channel, or (2) maintenance operations such as refresh. As we observe from the figure, none of our desktop and scientific applications come close to the maximum BPU. We find that namd and gobmk exhibit much higher BPU values than other applications with similar MPKI values. This indicates that these two applications often issue their memory requests in clusters, indicating bursty memory access patterns. As a result, these two applications exploit better memory-level parallelism, where the latencies of multiple memory requests are overlapped with each other. This overlapping reduces the application stall time [24], which in turn increases the IPC of the application.

Figure 25: DDR3 BPU for single-thread desktop/scientific applications.

Figure 26 shows the row buffer locality of each single-thread desktop/scientific application when run on DDR3. We do not see a correlation between the memory intensity of an application and its row buffer locality. This suggests that the locality is predominantly
a function of the application’s memory access patterns, and is not limited by the underlying DRAM type. We corroborate this by comparing the row buffer locality under DDR3 to the row buffer locality with our other DRAM types (not shown for brevity). We find that, with the exception of HMC (which reduces the row width by 97%), row buffer locality trends remain similar across different DRAM types.

Figure 26: DDR3 row buffer locality for single-thread desktop/scientific applications.

C.2 Multithreaded Desktop/Scientific Applications

To gain insight on limiting factors on the scalability of our multithreaded applications (see Section 6), we study the MPKI and IPC of each application when run using DDR3-2133, when the application runs with 1, 2, 4, 8, 16, and 32 threads. Figure 27 shows the single-thread IPC for all 12 applications, and lists both the single-thread and 32-thread MPKI (which quantifies the memory intensity of the application). We observe from the figure that our multithreaded applications have a narrower IPC range than our single-thread desktop applications. This is often because multithreaded applications are designed to strike a careful balance between computation and memory usage, which is necessary to scale the algorithms to large numbers of threads. Even then, we notice that as a general trend, multithreaded applications with a higher MPKI tend to have a lower IPC relative to multithreaded applications with a lower MPKI. Note that memory-intensive multithreaded applications have significantly higher IPCs compared to single-thread desktop/scientific applications with similar MPKI values.

Figure 27: Single-thread IPC for multithreaded applications executing on a system with DDR3-2133 memory. In parentheses, each benchmark includes its single-thread MPKI followed by its 32-thread MPKI.

As an example, we see that miniFE becomes more memory-intensive as the number of threads increases, with its MPKI increasing from 11.5 with only one thread to 68.1 with 32 threads. Despite this increase in memory intensity, its IPC remains around 1.5, indicating

that the application is not completely memory-bound. Prior work [6] corroborates this behavior, with an analysis of miniFE showing that in its two hotspot functions, the application spends about 40% of its time on load instructions, but also spends about 40% of its time on integer or floating-point instructions. This exemplifies the balanced approach between computation and memory that most of our multithreaded applications take, regardless of their memory intensity.

C.3 Server and Cloud Workloads

To characterize our server and cloud workloads (see Section 7), we study their performance and memory intensity using the DDR3 DRAM type. Figure 28 shows the performance of each application (IPC; see Section 4), and lists the MPKI. As we see from the figure, the IPC of all of the applications is very high, with the lowest-performing application (Apache2) having an IPC of 1.90. The high performance is a result of the low memory utilization of server and cloud workloads, which are often dominated by compute and are highly optimized to take advantage of on-chip caches.

Figure 28: IPC for server/cloud applications executing on a system with DDR3-2133 memory. In parentheses, each benchmark includes its MPKI.

C.4 OS Kernel Microbenchmarks

Figure 29 shows the performance of the common OS routines (see Section 9) on low-power DRAM types. For comparison, Figure 23 in Section 9.2 shows the performance of the routines for standard-power DRAM types. We make four observations from the figure. First, we observe that aside from a few exceptions, performance losses from using low-power DRAM types, compared to DDR3, are relatively small. For example, LPDDR3 has an average slowdown

Figure 29: Performance of common OS routines for low-power DRAM types, normalized to performance with DDR3. MPKI listed in parentheses.
of only 6.6% over DDR3. Second, we observe that due to the high sensitivity of OS routines to DRAM access latency (see Section 9.2), LPDDR4 has a larger slowdown (9.6% on average over DDR3) than LPDDR3 due to its higher access latency. Third, we observe that there are four routines where Wide I/O 2 provides significant performance improvements over DDR3: Test 12, Test 2, Test 0, and Test 6. This is because Wide I/O 2 significantly increases the row hit rate. As Figure 22 shows (Section 9.1), these four routines have much lower row hit rates (an average of 56.1%) than the other routines in DDR3. Under Wide I/O 2, the average row hit rate for these four routines jumps to 91.0% (not shown). Fourth, we observe that the forkbench routine performs significantly worse than the other routines, due to the fact that forkbench is significantly more memory intensive (with an MPKI of 49.5) than the other OS routines.

D Detailed Power and Energy Results

D.1 DRAM Power Breakdown

Figure 30 shows the breakdown of power consumed by these DRAM types, averaged across all of our single-thread applications and across our multiprogrammed workloads from Section 5. We observe that all of our DRAM types consume a large amount of standby power, with DDR3’s standby power representing 77.8% of its total power consumption. As the density of DRAM continues to increase, the standby power consumption is expected to grow as well. However, the total power consumed varies widely between DRAM types. For example, GDDR5 consumes 2.33x the power of DDR3, while LPDDR3 consumes only 41.4% of the DDR3 power.

Across all of our workloads (including other workload categories, not shown for brevity), we observe three trends: (1) standby power is the single biggest source of average power consumption in standard-power DRAM types; (2) LPDDR3 and LPDDR4 cut down standby power consumption significantly, due to a number of design optimizations that specifically target standby power (see Appendix A); and (2) workloads with a high rate of row conflicts and/or row misses spend more power on activate and precharge commands, as a new row must be opened for each conflict or miss.

D.2 DRAM Energy Consumption for OS Kernel Microbenchmarks

Figure 31 shows the energy consumed by each of the DRAM types that we have accurate power models for, normalized to DDR3 energy consumption, and averaged across all of the OS routines (see Section 9). We observe that the energy consumption behavior is similar to our single-thread desktop and scientific applications (see Section 5.4). This is because OS routines exhibit similar memory access patterns, with high row buffer locality and low memory intensity, as many of our desktop applications. However, unlike desktop applications, OS routines attain much higher average performance on low-power DRAM types (see Appendix C.4). As a result, LPDDR3 and LPDDR4 strike a better compromise of performance and energy consumption for OS routines than they do for desktop applications. We conclude that OS routines work efficiently for memories that provide large rows for high locality, and low access latencies.