Switched LC Network-Based Multi-Stage Ultra Gain DC-DC Converter

Seshagirirao Vemparala\(^1\), Student Member, IEEE, Pavithra T.\(^2\), and Kumaravel S.\(^3\), Senior Member, IEEE

\(^1\)Electrical Engineering Department, National Institute of Technology Calicut, Kerala, 673601 India
\(^2\)Electrical Engineering Department, National Institute of Technology Calicut, Kerala, 673601 India
\(^3\)Electrical Engineering Department, National Institute of Technology Calicut, Kerala, 673601 India

Corresponding author: Kumaravel S. (e-mail: kumaravel_s@nitc.ac.in).

This paragraph of the first footnote will contain support information, including sponsor and financial support acknowledgment. For example, “NaMPET, MEITY, Govt. of India under Grant NaMPET Ph-III/SP13/NH-Exp-01/Rev04.”

ABSTRACT A multi-stage active switched inductor-capacitor network (SLCN)-based high gain DC-DC converter structure with a single switch is proposed in this paper. The idea of utilizing multiple number of SLCN networks to achieve an ultra-voltage gain is proposed. The achievement of ultra-gain helps to operate the converter at lower duty ratio. Hence, a reduction of conduction loss, improvement in efficiency and elimination of core saturation are attained in the proposed bi-quadratic converter compared to the conventional converters. The performance of a biquadratic boost converter which is formulated from the \(n\)-stage SLCN converter for \(n=2\), is analyzed. To reduce the effect of parasitic elements of the semiconductor devices, the SiC-based devices are selected. The small-signal model of the biquadratic converter is derived, and a PI controller is designed to regulate the output voltage. The designed controller is implemented using XSGi platform. Experimental waveforms for 650 V output voltage, 500 W output power and 50 kHz switching frequency are presented. The performance of the proposed converter with similar recently reported topologies is compared. Simulation results of the biquadratic converter interfaced solar PV panel with P&O algorithm are presented to assess the feasibility of the proposed converter in solar PV application.

INDEX TERMS DC-DC converter, high voltage gain, switched LC network, wide bandgap devices

I. INTRODUCTION

More than three decades, the high and medium voltage DC systems have been utilized successfully to transmit the power collected from the renewable energy sources (RESS). But, the output voltage produced by these RESs like solar PV module and fuel cell is lower. The modules are used to connect in series to enhance the solar PV panel voltage. Whereas, the output power produced by the panel is affected due to hot spot, partial shading, etc. Hence, a parallel connected PV panel gives better performance compared to the series connected PV panel. In conventional approach as shown in Fig. 1(a), a step-up transformer is used along with the boost converter to integrate this low voltage RES to improve the voltage level of the load. However, this step-up transformer gives poor performance in the PWM power topologies, and also it is bulk in size and more in weight. To overcome the demerits of using transformer in the RES integration application, DC-DC converters with a high DC-voltage gain are proposed as an alternative approach in Fig. 1(b). A complete removal of the transformer [1-2] is achieved in this approach, so the overall system size is reduced. Apart from the aforementioned RES integration, these converters are used in the applications such as medical X-ray, electrostatic precipitation, high-energy physics, [3] telecommunication equipment, etc. In addition, these converters are employed in the offshore wind farms to convert low voltage DC to medium voltage DC [4][5]. The classical boost converter is widely used in some of the applications to enhance the output

![FIGURE 1](https://example.com/figure1.png)
voltage. But, it has a voltage gain of \(1/(1-D)\). To increase the voltage gain, the concepts based on switched inductors and switched capacitors are introduced [6][7]. A wide voltage range DC-DC converter using a switched capacitor (SC) is presented with a gain of \(2/(1-D)\) in [8]. A modified SEPIC converter with a gain of \((1+3D)/(1-D)\) is reported in [9]. The converter utilizes ten components, and produces the maximum gain of seventeen. By combining the switched inductor (SL) and SC, active switched LC network-based high gain DC-DC converters are reported in [10][11]. But, these converters produce the maximum voltage gain \(G < 30\).

A high gain converter is presented by incorporating the charge pump concept, self-lift circuit and voltage multiplier (VM) cells [12][13][14][15]. Using a capacitor clamped sub-module, a high gain converter is presented for the HVDC application [16]. The converter achieves a gain of \(n/(1-D)\). An \(n\)-stage high gain converter using SL concept is presented in [17]. The converter achieves a gain of \([1+(2n+3)]/(1-D)\). Few more \(n\)-stage high gain DC-DC converters [18-19] [25] and single stage [21-24] are reported in the literature. As the number of stages increases, the components count also increases. Some of these converters utilize more components when the converter extended to next stage, that increases the converter losses, bulkiness of the converter, etc. Some of the high gain DC-DC converters are reported in [27-30]. These converters use 2 switches in the topological structure; moreover, the converter [28] has a limitation in the operating when duty ratio \(D > 0.5\) (ideally). As shown in Fig. 1, the high gain non-isolated DC-DC converters are proposed to replace the transformer. The transformer is used to step-up the voltage and to provide the galvanic isolation. For the applications where the galvanic isolation is not mandatory like stand-alone solar PV, portable devices, high voltage test equipment, etc, the voltage gain provided by the transformer is met by the non-isolated DC-DC converter. The suppression of the leakage current is facilitated by the inverter unit which is coupled with the dc-dc converter [32].

A novel \(n\)-stage high gain DC-DC converter structure, which is basically derived from the boost converter, is presented in this paper. Fig. 2(a) shows the structure of the boost converter [26]. By replacing the inductor \(L\) (across terminal \(a\)-\(b\)) by an active switched inductor-capacitor network (SLCN), a high gain DC-DC converter [Fig. 2(b)] is reported with a voltage gain of \(1/(1-D)^2\) [20]. The active SLCN has two inductors, a capacitor and two diodes, and it has three terminals such as \(a\), \(b\) and \(S_0\). Here, \(S_0\) represents the drain terminal of the MOSFET. By replacing the inductors \(L_1\) and \(L_2\) by dedicated active SLCNs, a biquadratic high gain DC-DC converter which is shown in Fig. 2, is proposed with a voltage gain of \(1/(1-D)^4\) in this paper. The converter can be extended to any number of stages by replacing the inductors by dedicated SLCNs as an \(n\)-stage converter to achieve a voltage gain of \(1/(1-D)^{2n}\), as shown in Fig. 2(c). The \(n\)-stage converter requires \((4n-1)\) diodes, \(2n\) inductors, \(2n\) capacitors and a single semiconductor switch. One of the key features of the proposed \(n\)-stage SLCN-based DC-DC converter is the utilization of single switch irrespective of the number of stages of the converter. Compared to the aforementioned converters, the proposed bi-quadric converter produces higher dc-voltage gain. Typically, it produces the voltage gain of 625 at \(D = 80\%\).

II. PROPOSED BIQUADRATIC DC-DC CONVERTER

The circuit diagram of the proposed biquadratic high gain DC-DC converter is derived from Fig. 2(c) when \(n=2\). It consists of a switch \(SW\), four inductors \(L_1\), \(L_2\), \(L_3\) and \(L_4\), four capacitors \(C_1\), \(C_2\), \(C_3\) and \(C_6\) and seven diodes. The energy present in the inductor \(L_1\) is recycled in the capacitor \(C_1\). The energy present in \(C_1\) and \(L_2\) is recycled in the capacitor \(C_2\). Further, the energy present in \(L_3\) is recycled in the capacitor \(C_3\). Such a cascaded recycling process helps the proposed biquadratic DC-DC converter to achieve a high DC-voltage gain. The operation of the biquadratic high gain DC-DC converter in continuous conduction mode (CCM) is discussed in the below section.

Mode 1: In this mode, the semiconductor switch \(SW\) is turned on at the instant \(i_0\), and all the inductors are in the charging state. The inductor \(L_1\) charges from the source voltage \(V_s\). At the same time, \(L_2\) charges with the source

![Figures](image1.png)

**FIGURE 2.** (a) Boost converter (b) Quadratic boost converter for \(n = 1\) (c) Proposed \(n\)-stage SLCN-based DC-DC converter
voltage $V_s$ along with the capacitor voltage $V_{C1}$, where the input source and the capacitor $C_1$ are connected in series. This series connection causes a voltage of $V_s + V_{C1}$ across the inductor $L_2$. The inductor $L_3$ charges from the source voltage $V_s$ and the capacitor voltage $V_{C2}$, i.e., $V_s + V_{C2}$. The inductor $L_4$ charges with a voltage of $V_s + V_{C2} + V_{C3}$. Here, the diodes $D_1$, $D_2$, and $D_3$ are in forward biased condition, and the remaining diodes are in reverse biased condition. The operation of the converter in mode 1 is depicted in Fig. 3. The current of the inductors increases with a positive slope, as shown in the analytical waveform Fig. 5. The voltage across the inductors are expressed as,

$$V_{L1} = V_s; \quad V_{L2} = V_s + V_{C1} \quad \text{(1)}$$

$$V_{L3} = V_s + V_{C2}; \quad V_{L4} = V_s + V_{C2} + V_{C3} \quad \text{(2)}$$

Mode 2: In this mode, the semiconductor switch $SW$ is turned on from $t_1$ to $T_s$. The capacitor $C_1$ starts charging from stored energy of the inductor $L_1$ through the diode $D_2$. Similarly, the other capacitors $C_2$ and $C_3$ also start charging, as shown in Fig. 4. Along with the charging of these capacitors, the inductors $L_1$, $L_2$, $L_3$ and $L_4$ form a series path with the input source $V_s$, as shown in Fig. 4, and discharge power into the load side. Here, the diodes $D_2$, $D_3$, $D_4$ and $D_7$ are in forward biased condition, and the remaining diodes are in reverse biased condition. The current of the inductors decreases to a finite value with a negative slope, as shown in Fig. 5. The voltage across the inductors during this mode is:

$$V_{L1} = -V_{C1}; \quad V_{L2} = -V_{C2} \quad \text{(3)}$$

$$V_{L3} = -V_{C3}; \quad V_{L4} = V_s + V_{C2} + V_{C3} - V_0 \quad \text{(4)}$$

From (3-4), the voltage of the capacitors and the voltage gain during CCM mode are obtained as given in (5) and (6).

$$V_{C1} = \frac{V_s D}{1-D}; \quad V_{C2} = \frac{V_s D (2-D)}{(1-D)^2}; \quad V_{C3} = \frac{V_s D}{(1-D)} \quad \text{(5)}$$

$$G_{CCM} = \frac{V_s}{V_o} = \frac{1}{(1-D)^4} \quad \text{(6)}$$

By substituting $D = 80\%$ duty ratio in (6), the voltage gain is obtained as 625. Achieving such a high voltage gain using 16 components, including a single semiconductor switch is one of the merits of the proposed biquadratic converter.

**FIGURE 5.** Analytical waveforms of biquadratic converter in CCM

### III. DESIGN AND COMPONENTS SELECTION

The output power of 500 W is considered for the design, and the value of other parameters are given in Table I.

**i) Inductors selection:** Using the expression of the current ripple $\Delta I_L$ of the inductors, the inductance values of the inductors are derived as,

$$L_1 \geq \frac{V_s D}{f_c \Delta I_L}; \quad L_2 \geq \frac{V_s D}{f_c \Delta I_{L2}(1-D)} \quad \text{(7)}$$

$$L_3 \geq \frac{V_s D}{f_c \Delta I_{L3}(1-D)}; \quad L_4 \geq \frac{V_s D}{f_c \Delta I_{L4}(1-D)} \quad \text{(8)}$$

The average current through each inductor is expressed as,

$$I_{L1} = \frac{I_0}{(1-D)^2}; \quad I_{L2} = \frac{I_0}{(1-D)}; \quad I_{L3} = \frac{I_0}{(1-D)^2}; \quad I_{L4} = \frac{I_0}{1-D} \quad \text{(9)}$$

**ii) Capacitors selection:** The capacitors are charged in mode 2. Using the expression of energy stored in the capacitors, the final expressions of the capacitors are derived as,

$$C_1 \geq \frac{V_s D}{(1-D) R_0 f_c \Delta V_{C1}}; \quad C_2 \geq \frac{V_s D}{(1-D)^2 R_0 f_c \Delta V_{C2}} \quad \text{(10)}$$

$$C_3 \geq \frac{V_s D}{(1-D)^2 R_0 f_c \Delta V_{C3}}; \quad C_4 \geq \frac{V_s D}{(1-D)^3 R_0 f_c \Delta V_{C0}}$$

where $\Delta V_C$ is the ripple voltage across the capacitor.

**iii) Power switch and diodes selection:** The appropriate switch and diodes are selected based on the converter specifications given in Table I. The voltage and the current stresses of the switch and the diodes are given as,

$$\frac{V_{SW}}{V_s} = \frac{1}{(1-D)^4}; \quad I_{SW} = \frac{\sqrt{D} I_0}{(1-D)^3}; \quad V_{D1} = \frac{-D}{(1-D)^3}; \quad I_{D1} = \frac{\sqrt{D} I_0}{(1-D)^3} \quad \text{(11)}$$

$$\frac{V_{D2}}{V_s} = \frac{1}{1-D}; \quad I_{D2} = \frac{\sqrt{D} I_0}{(1-D)^3}; \quad V_{D3} = \frac{D(D-2)}{(1-D)^4}; \quad I_{D3} = \frac{\sqrt{D} I_0}{(1-D)^3} \quad \text{(12)}$$
\[
\begin{align*}
V_{DL} &= \frac{-1}{(1-D)^2} \cdot I_{PD} = \frac{-D}{(1-D)^2} \cdot \sqrt{-D I_D}, \quad V_{DS} = \frac{-D}{(1-D)^2} \cdot \sqrt{-D I_D} \\
V_{DS} &= \frac{-1}{(1-D)^2} \cdot I_{PD} = \frac{-D}{(1-D)^2} \cdot \sqrt{-D I_D}, \quad V_{DS} = \frac{-D}{(1-D)^2} \cdot \sqrt{-D I_D}
\end{align*}
\]

Using (23), the variation of the output voltage with respect to the duty ratio \( D \) is drawn, as shown in Fig. 6 for (i) ideal and (ii) \( R_0 = 845 \, \Omega \) and (iii) \( R_0 = 2000 \, \Omega \). Fig. 6 shows the output voltage of the biquadratic converter and the converters reported in [20][25]. The output voltage is significantly affected by the parasitic elements. To reduce the effect of parasitic elements, the SiC-based semiconductor devices are used.

### IV EFFECT OF PARASITIC ELEMENTS ON CONVERTER PERFORMANCE

A detailed investigation is conducted to study the effect of the parasitic elements on the output voltage of the converter. The winding resistance of the inductor is denoted by \( R_L \). The series equivalent resistance of the capacitor is denoted by \( R_C \). The forward voltage drop and the internal resistance of the diode are expressed as \( V_D \) and \( R_D \), respectively. The input source resistance is expressed as \( R_S \). A detailed investigation is conducted to study the effect of the parasitic elements on the output voltage of the converter.

The total ohmic loss of the inductors, capacitors, diodes and switch is derived, respectively as given in (24).

\[
P_L = \sum_{i=1}^{4} I_{L_i,RMS} R_L, \quad P_C = \sum_{i=0}^{3} I_{C_i,RMS} R_C, \quad P_{D,C} = \sum_{i=1}^{2} I_{Di,RMS} R_D
\]

The switching loss of the switches is expressed as,

\[
P_{SW,S,W} = \frac{1}{2} V_{SW,S,W} I_{SW,S,W} (t_{on} + t_{off}) f_s
\]

where \( V_{SW} \) - the maximum voltage across the switch, \( I_{SW} \) - the maximum current flowing through the switch, \( t_{on} \) - the summation of rising time and turn-on delay time, and \( t_{off} \) - the summation of fall time and turn-off delay time. The diode conduction loss associated with the diodes is derived as in (26).

\[
P_{D,S,W} = \sum_{i=1}^{7} I_{Di,RMS} V_{FD}
\]

By solving (15) – (22), the final expression of the output voltage with the parasitic elements is derived as,

\[
V_0 = \frac{V_{FD} (D + 9D^2 - 5D^3 - 1D^4)}{(1-D)^4 + a D^6 + b D^4 + c D^2 - d D^3 + e D + f D^5 + g D^6 + h D^7 + i D^8}
\]

where

\[
\begin{align*}
a &= \frac{1}{(1-D)^4} \\
b &= \frac{-D^3 + 4D^2 - 5D + 3}{(1-D)^4} \\
c &= \frac{-D^3 + 4D^2 + 7D - 6D^3 + 3}{(1-D)^4}
\end{align*}
\]

### TABLE I PARAMETERS OF BIQUADRATIC CONVERTER

| Parameters | Value |
|------------|-------|
| Output power | 500 W |
| Voltage \( V_S \) & \( V_D \) | 48 V and 650 V |
| Switching frequency \( f_s \) | 50 kHz |
| Capacitors \( C_1, C_2, C_3 \) & \( C_0 \) | 100 \( \mu F \), 47 \( \mu F \), 22 \( \mu F \) & 22 \( \mu F \), respectively. |
| Inductors \( L_1, L_2, L_3 \) & \( L_4 \) | 1 mH, 2 mH, 3 mH & 5 mH |
| Switch SW | C2M0040120D |
| Diodes \( D1 \) & \( D2 \) | FFSH4065A & FFSH30120A |

FIGURE 6. Output voltage with parasitic elements

This article has been accepted for publication in IEEE Access. The author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3183015
$P_{D(V)}$, as shown in Fig. 7. The losses of the diodes $D_1$ and $D_2$ are 2.56 W and 2.79 W, respectively and these losses are more compared to other diodes. Hence, the diodes $D_1$ and $D_2$ affect the efficiency compared to the other diodes. Compared to the quadratic converter which operates at $D = 73\%$, the operation of the biquadratic converter at $D = 48\%$, i.e., operation at lower duty ratio for $V_0 = 650$ V and $V_s = 48$ V reduces the switch loss significantly.

Fig. 8 shows the analytical and the experimental efficiency profiles of the biquadratic converter and the quadratic converter. The biquadratic converter produces the analytical efficiency of $95.48\%$ at 500 W for $V_0 = 650$ V, $V_S = 48$ V. The analytical efficiency profiles of the biquadratic and the quadratic converters at $V_0 = 1000$ V and $V_s = 48$ V are also marked in Fig. 8. At this operating point, the quadratic boost converter produces significantly lower efficiency compared to the biquadratic converter.

V. SMALL-SIGNAL MODEL
Using the state-space averaging, the small-signal model of the biquadratic converter is developed. The on-state resistance and the forward voltage drop of semiconductor devices and the parasitic resistance of reactive elements are not considered in the circuit to reduce the calculation complexity. Instead, a loop resistance of $r$ which exist in every loop is considered. The voltage across the inductors and the current through the capacitors for mode 1 are:

$$
\begin{align*}
\hat{v}_{L_1} &= \hat{v}_{S} - \hat{i}_{L_1}r, \\
\hat{v}_{L_2} &= \hat{v}_{S} + \hat{i}_{L_2}r + \hat{V}_{C_3} - \hat{i}_{L_3}r, \\
\hat{v}_{L_3} &= \hat{v}_{S} + \hat{i}_{L_3}r - \hat{V}_{C_3} - \hat{i}_{L_3}r, \\
\hat{v}_{C_1} &= \hat{v}_{C_2} + \hat{i}_{C_2}r, \\
\hat{v}_{C_2} &= \hat{v}_{C_3} - \hat{i}_{C_3}r,
\end{align*}
$$

(28)

Similarly, necessary equations for mode 2 are derived. Using these equations, the state-space average model is:

$$
\dot{x} = A_x x + B_u u, \\
y = C_x x
$$

(29)

FIGURE 8. Output power versus efficiency

FIGURE 9. Dynamic response (a) step response (b) Bode plot

where $x = [i_{L_1} i_{L_2} i_{L_3} i_{C_1} i_{C_2} i_{C_3} v_{C_1} v_{C_2} v_{C_3}]^T$, $u = [v_s i_0]$, $y = [v_0]$. By applying the AC perturbations on the above state-space...
average model, the final small-signal model of the biquadratic converter is obtained, as expressed in (30)-(31). Using the small-signal model, the transfer functions are derived as expressed in (32)-(34) for the specifications given in Table I. The eight poles of the transfer function are located in the left-hand side of the s-plane. Hence, the proposed biquadratic converter is stable. The Bode plot and the step response of the transfer function are shown in Fig. 9. The step response of the biquadratic converter shows that response settle down with a finite gain.

\[ v_s = \left[ \begin{array}{c} v_{s1} \\ v_{s2} \\ v_{s3} \end{array} \right] = \left[ \begin{array}{c} \frac{-r_{L1}}{L_1} \\
\frac{-r_{L2}}{L_2} \\
\frac{-r_{L3}}{L_3} \\
\frac{-r_{L4}}{L_4} \\
\frac{-r_{L5}}{L_5} \\
\frac{-r_{L6}}{L_6} \\
\frac{-r_{L7}}{L_7} \\
\frac{-r_{L8}}{L_8} \end{array} \right] \left[ \begin{array}{c} \frac{D-1}{L_1} \\
\frac{D-1}{L_2} \\
\frac{D-1}{L_3} \\
\frac{D-1}{L_4} \\
\frac{D-1}{L_5} \\
\frac{D-1}{L_6} \\
\frac{D-1}{L_7} \\
\frac{D-1}{L_8} \end{array} \right] \left[ \begin{array}{c} i_{c1} \\
\frac{1}{C} \\
\frac{1}{C} \\
\frac{1}{C} \\
\frac{1}{C} \\
\frac{1}{C} \\
\frac{1}{C} \\
\frac{1}{C} \end{array} \right] \left[ \begin{array}{c} v_{c1} \\
v_{c2} \\
v_{c3} \\
v_{c4} \end{array} \right] \left[ \begin{array}{c} \frac{1}{RC} \end{array} \right] \]

The schematic diagram of the closed-loop system of the proposed biquadratic is shown in Fig. 10. A PI controller is designed to regulate the output voltage when there is a disturbance in the source side and load side. The proportional gain \( K_P \) and integral gain \( K_I \) are designed using Ziegler-Nichols method. The obtained values are \( K_P = 0.015 \) and \( K_I = 1.42 \). The designed controller has been successfully implemented in Xilinx System Generator (XSG). The implemented program is realised in the real time by using Zynq 7000 FPGA module which operates at the 40 MHz clock period. Based on the feedback output voltage, a protection scheme is developed to disable the control signal when the output voltage exceeds 750 V.

FIGURE 10. Closed loop system of biquadratic converter

VI. BIQUADRATIC CONVERTER INTERFACED SOLAR PV PANEL

To assess the feasibility of the biquadratic converter in solar PV application, a simulation study has been conducted on the biquadratic converter interfaced solar PV panel. The Perturb & Observe (P&O) algorithm [30] is used for tracking the maximum power from the solar PV panel. The block diagram of the biquadratic converter interfaced solar PV panel with MPPT controller is shown in Fig. 11.

FIGURE 11. Biquadratic converter interfaced solar PV panel

The current \( \text{versus} \) voltage and power \( \text{versus} \) voltage characteristics of the solar panel of GSM 500-96 is shown in Fig. 12. The considered solar panel has the maximum power of 500 W with the open circuit voltage of 58.95 V and the short circuit current of 10.87 A. The panel produces the output voltage of closely 48.63 V at the maximum power point (MPP), as shown in Fig. 18(b). The simulation of the biquadratic converter interfaced solar PV panel has been conducted, and the simulation waveforms are shown in Fig. 19. The input solar radiation is varied from 1000 W/m² to various levels as given in Fig. 13(a). The \( V_{PV} \) and \( I_{PV} \) of the solar panel are sensed and given to the P&O algorithm. The control duty ratio given by the algorithm is given to the PWM unit, and the control pulse for the switch SW of the biquadratic converter is generated. The \( V_{PV} \) and \( I_{PV} \) of the solar panel observed from the simulation are shown in Fig. 19(b-c). When the input solar radiation is changed from 1000 W/m² to 800 W/m² at 0.5 sec, as shown in Fig. 13(a), the power produced by the solar PV panel is changed from 500 W...
The output power shown in Fig. 13(d) witnesses that the biquadratic converter tracks the MPP from the solar panel with help of the P&O algorithm for the variation in the solar radiation.

VII. EXPERIMENT RESULTS AND DISCUSSIONS

A 500 W laboratory prototype of the biquadratic converter is fabricated, as shown in Fig. 14. The components are selected according to the proper design as explained in section III. For the experimental validation, the switching frequency of 50 kHz is considered. The input voltage source is realized using a programmable voltage source of GWINSTEK, and it is set to 48 V. To generate the switching pulse of 48% duty ratio for the switch SW, Tektronix TPS 2024B pulse generator is used. Using Digital Storage Oscilloscope (DSO), the hardware results are captured under the steady-state in CCM, as shown in Fig. 15. Fig. 15(a) shows that the inductor L1 is charged with a voltage \( V_S \) of 48 V, and it is discharged with a voltage of \( V_{C1} \) of 44 V. Fig. 15(b) shows the voltage and current waveforms of the L2. The L2 charges with a voltage \( V_{C1}+V_S \) of 92 V, and it discharges with a voltage of \( V_{C2} \) of 44 V. Fig. 15(b) shows the voltage and current waveforms of the L2. The L2 charges with a voltage \( V_{C1}+V_S \) of 92 V, and it discharges with a voltage of \( V_{C2} \) of 44 V. The voltage values of both the capacitors C2 and C3 become 126 V and 160 V, respectively. Fig. 15(c) shows the voltage and current waveforms of the L3. The experimental waveforms of each inductor closely match with the analytical waveforms, which are shown in Fig. 5. Fig. 15(d) shows the voltage waveforms captured from the inductor L4 and the capacitor C3. The waveforms confirm that the inductor L4 charges with a voltage of 340 V, and it discharges with 291 V. The capacitor C3 holds energy with a voltage of 160 V. Fig. 15(e) presents the voltage and current waveforms of the input source and the load. Although the input current has
The experiment on the biquadratic converter has been done in the closed-loop condition. The output voltage across the load is fed into the Zynq controller, and the control signal derived from the controller is given to the gate driver. The higher ripple content, the ripple can be reduced by changing the connection of the negative terminal of the capacitor $C_1$ to the source negative terminal. However, the voltage stress of the capacitors $C_1$, $C_2$ and $C_3$ will be increased.
dynamic response of the biquadratic converter for the step-change in the input voltage and the output load is observed, and the experimental results are presented in Fig. 16. Fig. 16(a) shows the response of the converter when load current is changed from 0.15 A to 0.46 A by keeping the V_S constant. The output waveforms confirm that the controller regulates the V_o at 650 V. Similarly, the response of the converter for the step change in source is also shown in Fig. 16(b). Here, the input voltage is changed from 48 V to 30 V.

VIII. PERFORMANCE COMPARISON

The performance of the proposed biquadratic converter is compared with the similar recent reported topologies, as given in Table II. The comparison of dc-voltage gain in terms of duty ratio for the biquadratic converter with the conventional converters (given in Table II) is shown in Fig. 17. This plot shows that the proposed biquadratic converter produces more dc-voltage gain compared to other dc-dc converters. Although [22] with n=2 produces slightly better dc-voltage gain, as shown in Fig. 14 for D ≤ 0.52, it uses 33 components including 4 semiconductor switches. Compared to some of the existing converters [4][15-18][21] and [22], the proposed SLCN-based converter requires only one semiconductor switch. Also, the comparison of the biquadratic converter in terms of dc-voltage gain/number of components is shown in Fig. 18. As given in Table II, though the number of components of [4] with n=3, [15], [16] with n=4, [18] with n=3, [21] and biquadratic converter is close to each other, the biquadratic converter has more voltage gain/number of components, as shown in Fig. 18.

The maximum potential of the proposed biquadratic converter shall be extracted when the converter is operated at a higher output voltage. The proposed bi-quadratic converter achieves the output voltage 1000 V from 48 V at D = 53.2% with help of a single semiconductor switch. Whereas, the other converters achieve the same output voltage at the higher duty ratio, as given in Table II. However, [22] achieves this output voltage at D = 47.2%. But, it uses 33 components. The comparison of switch stress for various converters is given in Table II. Fig. 19(a) shows the comparison of switch voltage and current stress of the high gain converters which use a single switch. Although the switches present in [11] with n=2 and [23] have lower voltage stress of 806 V and 612 V respectively, to produce V_o = 1000 V; they have more current stress of 10.26 A and 14.07 A, respectively. When the biquadratic converter is operated at lower duty ratio, i.e., at D = 53.2%, the current stress is significantly reduced (i.e., 5.54 A) compared to the other converters. Accordingly, the switching loss is also reduced, and the volume of the heat sink for the switch can be minimized. Compared to the biquadratic converter, the converters [17] with n=2, [19] with n=2 and [22] with n=2 use more diodes, i.e., 16, 10 and 12, respectively. Whereas, the other converters use six or lesser number of diodes. The voltage stress of the diodes D_1-D_3 of the quadratic converter [20] is exactly equal to the voltage stress expressions of D_1-D_8 of [25]. Similarly, the voltage stress expressions of D_1-D_2 of the biquadratic converter is exactly equal to D_1-D_2 of [25]. However, the voltage stress of D_1 and D_2 of the biquadratic converter and [25] is lesser compared to their respective diode D_1 as given in Table II. An extensive analysis has been conducted to assess the performance for

![FIGURE 17. Voltage gain comparison of biquadratic converter](image)

![FIGURE 18. Comparison in terms of voltage gain/number of components](image)
biquadratic converter gives better efficiency in the high voltage region compared to [20] and [23].

The analytical efficiency profiles of the above three converters at $V_0 = 1000 \text{ V}$ and $V_S = 48 \text{ V}$ are shown in Fig. 16(h). The extensive analysis proves that the biquadratic converter gives a better performance in the high voltage region compared to the conventional converters. The operation of the converter at lower duty ratio, lower current stress, continuous source current, improved efficiency, the requirement of a single control signal and a single driver circuit are the attractional features of the proposed biquadratic converter.

**FIGURE 19.** Performance comparison (a) switch stress (b) duty ratio Versus $P_0$ and $V_0$ (c) Switch current Versus $P_0$ and $V_0$ (d) Switching loss Versus $P_0$ and $V_0$ (e) Switch loss Versus $P_0$ and $V_0$ (f) Diode loss Versus $P_0$ and $V_0$ (g) Efficiency Versus $P_0$ at $V_0 = 1000 \text{ V}$ and $V_S = 48 \text{ V}$ (h) Efficiency Versus $P_0$ at $V_0 = 1000 \text{ V}$ and $V_S = 48 \text{ V}$.
IX. CONCLUSION

The structure formulation of an active SLCN-based high gain DC-DC converter with n-stage was proposed. From the n-stage structure, the biquadratic converter was derived for n = 2, and its operation was discussed in the CCM. The design of various components of the biquadratic converter was carried out. The effect of parasitic elements of the components of the biquadratic converter was investigated, and an attempt was made to reduce the parasitic effect using SiC-based semiconductor devices. The utilization of the SiC devices enhances the overall efficiency of the converter to 95.48% at 500 W output power. The experimental waveforms of the laboratory prototype of the converter for \( P_o = 500 \) W, \( f_s = 50 \) kHz and \( V_s = 48 \) V were observed by considering \( V_o = 650 \) V. The small-signal model of the biquadratic converter was developed, and the transfer functions were derived. A PI controller was designed, and the designed controller was implemented in XSG. The dynamic response of the converter was observed for the closed loop system. Simulation results of the bi-quadratic converter interfaced solar PV panel with P&O algorithm were presented to assess the feasibility of the proposed converter in solar PV application. The performance comparison of the proposed n-stage SLCN-based converter with the similar recently reported topologies shows that the operation of the converter at lower duty ratio, lower current stress, improved efficiency, the requirement of a single control signal and a single driver circuit are the attractive features of the proposed bi-quadratic converter. Hence, the biquadratic converter is a suitable candidature for the applications such as integration of solar PV and fuel cell, high voltage test equipment, medical X-ray, electrostatic precipitation, high-energy physics, telecommunication equipment, medium/high voltage wind farms, etc.

ACKNOWLEDGMENT

This work has been done for the project “GaN-Based High Gain DC/DC Converter Fed Multi-Level Inverter for UPS Application, by NaMPET, MEITY, Govt. of India.

REFERENCES

[1] T. Steiner, R. Prietsch, U. Kaltenborn and M. Hensel, "Modular DC Test System," 2019 IEEE PES GTD Grand International Conference

This article has been accepted for publication in IEEE Access. This is the author’s version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3183015.


V. Garcia, M. Rico, J. Sebastian, M. M. Hernando and J. Uceda, “An optimized DC-to-DC converter topology for high-voltage pulse-load applications,” Proceedings of 1994 Power Electronics Specialist Conference - PESC’94, Taipei, Taiwan, 1994, pp. 1413-1421, vol.2

Q. Xu, X. Zhang, W. Zhou and S. Zuo, “Development of Portable Digital HVDC Generator Based on MCU and CPLD,” 2012 Asia-Pacific Power and Energy Engineering Conference, Shanghai, 2012, pp. 1-5.

B. Zhu, S. Liu, D. M. Vilathgamuwa and Y. Li, “High step-up SVM-based DC/DC converter for offshore wind farms,” in IET Power Electronics, vol. 12, no. 6, pp. 1445-1454, 29 5 2019.

H. Krishnamoorthy, M. Daniel, J. Ramos-Ruiz, P. Enjeti, L. Liu and E. Aeloa, “Isolated AC–DC Converter Using Medium Frequency Transformer for Off-Grid Wind Turbine DC Collection Grid,” in IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 8939-8947, Nov. 2017.

B. Axelrod, Y. Berkovich, and A. Ioinovic, “Switched-capacitor switched-inductor structures for getting transformerless hybrid DC–DC PWM converters,” IET Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 2, pp. 687-696, Mar. 2008.

Wu, G., Member, S. Ruan, X., Member, S., Ye, Z.: Nonisolated High Step-Up DC – DC Converters Adopting Switched-Capacitor Cell IEEE Trans. Ind. Electron., 2015, 62, (1), pp. 383–393.

Y. Zhang, L. Zhou, M. Sumner and P. Wang, “Single-Switch, Wide Voltage-Gain, Range Boost–DC/DC Converter for Fuel Cell Vehicles, in IEEE Transactions on Vehicular Technology, vol. 67, no. 1, pp. 134-145, Jan. 2018.

S. A. Ansari and J. S. Moghiani, “A Novel High Voltage Gain Noncoupled Inductor SEPIC Converter,” in IEEE Transactions on Industrial Electronics, vol. 66, no. 9, pp. 7069-7108, Sept. 2019.

Gu, Y., Chen, Y., Zhang, B., Member, S., Qiu, D., & Xie, F. (2019). High Step-Up DC – DC Converter With Active Switched LC - Network for Photovoltaic Systems. IEEE Transactions on Energy Conversion, 34(1), 321–329.

G. Gurukumar, Kumaravel Sundaramoorthy, V. Karthikeyan and E. Babaei, “Switched Capacitor-Inductor network based Ultra-Gain DC-DC Converter using Single Switch,” in IEEE Transactions on Industrial Electronics, doi:10.1109/TIE.2019.2962406.

T. Jalilzadeh, N. Rostami, E. Babaei and M. Maalandish, “Ultra-step-up dc–dc converter with low voltage stress on devices,” in IET Power Electronics, vol. 12, no. 3, pp. 345-357, 20 3 2019.

A. Alzahrani, M. Ferdowsi and P. Shamsi, “High-Voltage-Gain DC-DC Step-Up Converter With Bifold Dickson Voltage Multiplier Cells,” in IEEE Transactions on Power Electronics, vol. 34, no. 10, pp.9732-9742, Oct.2019.

V. Karthikeyan, Kumaravel Sundaramoorthy, G. Guru Kumar and E. Babaei, “Regenerative switched-inductor-capacitor type DC–DC converter with large voltage gain for PV applications,” in IET Power Electronics, vol. 13, no. 1, pp. 687-71 20 2020.

Y. Zhang, H. Liu, J. Li, M. Sumner and C. Xia, “DC-DC Boost Converter With a Wide Input Range and High Voltage Gain for Fuel Cell Vehicles,” in IEEE Transactions on Power Electronics, vol. 34, no. 5, pp. 4100-4111, May. 2019.

Z. Xiong and T. C. Green, “The Modular Multilevel Converter for High Step-Up Ratio DC–DC Conversion,” in IEEE Transactions on Industrial Electronics, vol. 62, no. 8, pp. 4295-4296, Aug. 2015.

E. Babaei, H. Mashinchi Maheri, M. Sabahi and S. H. Hosseini, “Extendable Nonisolated High Gain DC-DC Converter Based on Active–Passive Inductor Cells,” in IEEE Transactions on Industrial Electronics, vol. 65, no. 12, pp. 9478-9487, Dec. 2018.

H. Mashinchi Maheri, E. Babaei, M. Sabahi and S. H. Hosseini, “High Step-Up DC-DC Converter with Minimum Output Voltage Ripple,” in IEEE Transactions on Industrial Electronics, vol. 64, no. 5, pp. 3568-3575, May 2017.

T. Nouri, S. H. Hosseini, E. Babaei and J. Ebrahimi, “Generalised transformerless ultra step-up DC–DC converter with reduced voltage stress on semiconductors,” in IEEE Power Electronics, vol. 7, no. 11, pp. 2791-2805, 11 4 2014.

Y. Ye and K. W. E. Cheng, “Quadratic boost converter with low buffer capacitor stress,” in IEEE Power Electronics, vol. 7, no. 5, pp. 1162-1170, May. 2014.

T. Jalilzadeh, N. Rostami, E. Babaei, and M. Maalandish, “Non–Isolated Topology for High Step-Up DC-DC Converters,” IEEE J. Emerg. Sel. Top. Power Electron., vol. no. c. p. 1, 2018.

M. Maalandish, S. H. Hosseini and T. Jalilzadeh, “High step-up dc/dc converter using switch-capacitor techniques and lower losses for renewable energy applications,” in IET Power Electronics, vol. 11, no. 10, pp. 1718-1729, 28 8 2018.

V. F. Pires, A. Cordeiro, D. Foito and J. F. Silva, “High-Step-Up DC– DC Converter for Fuel Cell Vehicles Based on Merged Quadratic Boost–Cuk,” in IEEE Transactions on Vehicular Technology, vol. 68, no. 8, pp. 7521-7530, Aug. 2019.

V. N. Kumar, N. Babu P, R. Kiranmayi, P. Siano and G. Panda, “Improved Power Quality in a Solar PV Plant Integrated Utility Grid by Employing a Novel Adaptive Current Regulator”, in IEEE Systems Journal, vol. 14, no. 3, pp. 4308-4319, Sept. 2020.

G. K. Gomes, M. V. S. Krishna, S. Kumaravel and E. Babaei, “Multi-stage DC-DC Converter using Active LC2 Network with Minimum Component,” in IEEE Transactions on Circuits and Systems II: Express Briefs, doi: 10.1109/TCSI.2020.3021609.

S. R. Pendem, S. Mikkilä and P. K. Bonthagorla, “PV Distributed-MPP Tracking: Total-Cross-Tied Configuration of String-Integrated-Converters to Extract the Maximum Power Under Various PSCs”, in IEEE Systems Journal, vol. 14, no. 1, pp. 1046-1057, March 2020, doi: 10.1109/JSYST.2019.2917606.

Zaid, M., Khan, S., Siddique, M. D., Sarwar, A., Ahmad, J., Sarwer, Z., & Iqabal, A. (2021). A transformerless high gain dc–dc boost converter with reduced voltage stress. International Transactions on Electrical Energy Systems, 31(5), doi:10.1002/2050-7038.12877.

Mahnood, A, Zaid, M, Khan, S, Siddique, MD, Iqbal, A, Sarwer, Z. A non-isolated quasi-Z-source-based high-gain DC–DC converter. Int J Circ Theor Appl. 2022; 50 (2): 653-662. doi:10.1002/cta.3162.

Ahmad, J., Siddique, MD, Sarwar, A, Lin, CH, Iqbal, A. A high gain noninverting DC–DC converter with low voltage stress for industrial applications. Int J Circ Theor Appl. 2021; 49 (12): 4212–4230. doi:10.1002/cta.3129.

R. Rahimi, S, Habibi, M, Ferdowsi and P. Shamsi, “Z-Source-Based High Step-Up DC-DC Converters for Photovoltaic Applications,” in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi:10.1109/JESTPE.2021.3131996.

S. Khan et al., “A New Transformerless Ultra High Gain DC–DC Converter for DC Microgrid Application,” in IEEE Access, vol. 9, pp. 124560-124582, 2021, doi:10.1109/ACCESS.2021.3101668.

B. M. J., & Anjumol, C. S. (2014). Leakage Current Elimination in Single Phase Transformer less Grid Connected Power Systems. Int J Innovative research in electrical, electronics, instrumentation and control engineering 2(3), 1266–1271.

Vemparala Seshagiri Rao, completed his B.Tech degree in Electrical Engineering from ALIET, Vijayawada in 2015. He completed M.Tech degree in Industrial Power and Automation from NIT Calicut in 2019 where he is pursuing PhD at present. His research interests include high gain dc–dc converters and multi input dc–dc converters.

Pavitra T, completed her B.Tech degree in EEE from NSSCE Palakkad in 2016 and completed M.Tech degree in Industrial Power and Automation from NIT Calicut in 2020. Her research interests include high gain dc–dc converters.

Kumaravel Sundaramoorthy (M’2009, SM’15) received the B.E. (EEE) from Bharathidasan University, Tiruchirappalli, in 2002, M.Tech. (Power Systems) from the National Institute of Technology (NIT) Tiruchirappalli, in 2007, and Ph.D. degree in Electrical Engineering from NIT Calicut, India, in 2012. He has completed the PDF from University College Dublin, Ireland. Since 2008, he has been with NIT Calicut. His area of research includes dc–dc converters, microgrid, etc.