In this article we study measurement circuit effects in three-terminal electrical transport measurements arising from finite line impedances. We provide exact expressions relating the measured voltages and differential conductances to their values at the device under test, which allow for spurious voltage divider effects to be corrected. Finally, we test the implementation of these corrections with experimental measurements.

I. MEASUREMENT CIRCUIT EFFECTS

Three-terminal devices are a powerful tool for studying electrical transport in nanoscale systems. Three-terminal devices have been used to split Cooper pairs, characterize end-to-end state correlations in nanowires, study the local charge character of Andreev bound states, and have been proposed as probes for topological bulk properties. In cryogenic experimental setups for electrical transport measurements, it is common for the measurement circuit to include filters, which give rise to finite line impedances. Such line impedances may give rise to spurious effects arising from voltage divider effects, particularly when studying the nonlocal conductance (cross-conductance) between terminals. These effects have been previously noted in the literature, and sometimes corrected to first order, see for example Ref. [6]. The goal of this work is to give exact expressions relating the measured electrical quantities to the corresponding quantities at the device under test. These expressions allow to correct for voltage divider effects even in the regime where the device impedances are comparable to the line impedances, as long as the latter are well known.

We consider a device under test with three terminals: left (l), right (r) and ground (g). The device terminals are connected through line impedances \( Z_l \), \( Z_r \) and \( Z_g \) to external measurement terminals and an external reference ground, respectively. The line impedances are part of the measurement circuit, and are assumed to be constant and linear. At the measurement terminals we apply voltages \( V_l \), \( V_r \) with respect to the external reference ground voltage \( V_g \). The voltages at the (internal) device terminals are denoted \( U_l \), \( U_r \) and \( U_g \) respectively. All the voltages may in general be time-dependent, and are assumed to have a DC component for biasing the device and AC components for lock-in differential conductance measurements. Typically the line impedances originate from low-pass filters, which also have capacitive shunts to ground. The results in this paper hold for signal frequencies much lower than the filter cut-off frequency, since above this frequency the setup effectively has more than three terminals.

The voltages \( U_l \) at the device terminals are related to the voltages \( V_l \) applied at the measurement terminals by:

\[
U_l = V_g + V_l - I_l Z_l \quad (1)
\]

\[
U_r = V_g + V_r - I_r Z_r \quad (2)
\]

\[
U_g = V_g + (I_l + I_r) Z_g \quad (3)
\]

Since only relative voltages are physically meaningful, we can define as the voltage reference the ground terminal at the device instead of the external measurement ground, that is, \( U_g = 0 \). Combining the previous expressions and eliminating \( V_g \) we get:

\[
U_l = V_l - I_l Z_l - (I_l + I_r) Z_g \quad (4)
\]

\[
U_r = V_r - I_r Z_r - (I_l + I_r) Z_g \quad (5)
\]

or in vector form, where \( \mathbf{V} = (V_l, V_r)^T \) and likewise for \( \mathbf{U} \) and \( \mathbf{I} \):

\[
\mathbf{U} = \mathbf{V} - \mathbf{Z} \mathbf{I}, \quad (6)
\]
where $Z$ is a matrix with the line impedances:
\[
Z = \begin{pmatrix} Z_l + Z_g & Z_g \\ Z_g & Z_r + Z_g \end{pmatrix}.
\] (7)

Eq. (6) is particularly useful to calculate the DC voltage biases $U$ at the device from the DC voltages $V$ applied at the measurement terminals and the measured DC currents $I$, by taking the zero-frequency component.

The electrical behavior of any device in a particular configuration is fully characterized by its differential conductance matrix. Measuring terminals and the measured DC currents $I$, by taking the zero-frequency component.

Both conductance matrices $G$ and $G'$ agree for zero line impedances. But in the typical case of finite line impedances, we need to measure as well the AC voltage amplitudes $dV$ at the device terminals. In order to directly measure the conductance matrix $G'$, we need to measure the conductance matrix $G$ at the device under test. Only these 2 x 2 elements are required to completely determine the conductance matrix of the device, since the rest of its elements are determined by conservation of current and the choice of reference voltage.

In order to optimize signal-to-noise ratio it is usual to measure differential conductance using low-frequency lock-in techniques. AC voltage excitations $dV$ with different frequencies are applied at the left and right measurement terminals, and the resulting AC currents $dI$ are measured on both terminals at both frequencies, as explained in ref.[9]. In order to directly measure the conductance matrix $G'$, we need to measure the conductance matrix $G$ with respect to the AC voltage excitations applied at the external measurement terminals, which is defined as:
\[
G(V) = \frac{\partial I}{\partial V} = \begin{pmatrix} \partial_l / \partial V_l & \partial_l / \partial V_r \\ \partial_r / \partial V_l & \partial_r / \partial V_r \end{pmatrix}.
\] (9)

Both conductance matrices $G$ and $G'$ agree for zero line impedances. But in the typical case of finite line impedances, the measured conductance matrix $G$ may show spurious effects that do not relate to the behavior of the device under test.

We now want to convert the measured conductance matrix $G$ to the matrix $G'$ at the device. Applying the chain rule on $G$:
\[
G'(U) = \left( \begin{array}{cc} \partial_l / \partial U_l & \partial_l / \partial U_r \\ \partial_r / \partial U_l & \partial_r / \partial U_r \end{array} \right) \cdot \left( \begin{array}{cc} \partial V_l / \partial U_l & \partial V_l / \partial U_r \\ \partial V_r / \partial U_l & \partial V_r / \partial U_r \end{array} \right) = G(V) \left( \begin{array}{cc} \partial V_l / \partial U_l & \partial V_l / \partial U_r \\ \partial V_r / \partial U_l & \partial V_r / \partial U_r \end{array} \right).
\] (10)

\[
G'(U) \approx G(V) \left( \begin{array}{cc} 1 & Z \end{array} \right).
\] (11)

The conductance matrix $G'$ at the device is evaluated at the voltages $U$ corresponding to the applied voltages $V$ through Eq. (6). Note that, in general, setting one of the $V$’s to be constant and varying the other will vary both $U_l$ and $U_r$. If one seeks to measure the conductance matrix at particular values of $U$, the applied voltages $V$ have to be chosen using Eq. (6) such that at each measurement point $U$ has the desired value.

The Jacobian matrix $\partial U / \partial V$ in Eq. (11) relates the voltages outside of the measurement setup to the voltages at the device. We can calculate it by differentiating (6) with respect to $V$:
\[
\frac{\partial U}{\partial V} = 1 - Z \frac{\partial I}{\partial V} = 1 - Z G(V).
\] (12)

Finally, inverting the previous expression using the inverse Jacobian rule:
\[
\frac{\partial V}{\partial U} = (1 - Z G(V))^{-1}.
\] (13)

Plugging (13) into (11) we obtain the main result of this paper, the transformation from the raw conductance matrix $G(V)$ at the measurement terminals to the corrected conductance matrix $G'(U)$ at the device:
\[
G'(U) = G(V) \left( \begin{array}{cc} 1 & Z \end{array} G(V) \right)^{-1}.
\] (14)

Note that the transformation in Eq. (14) is exact, and holds even when all the measured conductances are large compared to the line resistances. This is experimentally relevant since it is often convenient to measure a device in a highly conductive regime for signal-to-noise purposes. In particular, the expression in Eq. (14) is more general than the first-order voltage divider effects that are sometimes corrected for in the literature, e.g. [10], which hold when the conductances $G(V)$ are small compared to the line resistances $Z$. In order to derive the first-order corrections from the exact transformation we can expand Eq. (14) as a function of the product $Z G(V)$. The corrections are small if all the elements $(Z G(V))_{ij} < 1$, that is:
\[
|Z_l| \ll |G_{ll}|^{-1},
\]
\[
|Z_r| \ll |G_{rr}|^{-1},
\]
\[
|Z_g| \ll |G_{lg}|^{-1},
\]
for $i, j = l, r$. If this is the case, we can expand the factor $(1 - Z G(V))^{-1}$ in Eq. (14) as a geometric series, obtaining to first order:
\[
G'(U) \approx G(V) \left( 1 + Z \right).
\] (15)

If the nonlocal conductances are much smaller than the local conductances, i.e. $|G_{lr}|, |G_{rl}| \ll |G_{ll}|, |G_{rr}|$, to zeroth order the correction can be written as:
\[
G'(U) \approx G(V) + \left( \begin{array}{ccc} Z_l + Z_g & Z_g G_{ll} G_{rr} & Z_g G_{rl} G_{rr} \\ Z_g G_{lr} G_{rr} & Z_r + Z_g & \end{array} \right).
\] (16)

Assuming that the local conductances are real and positive, the local conductances $G_{ll}, G_{rr}$ at the device are larger than...
the measured ones by a correction quadratic in the conductance and proportional to the line impedance. This correction arises from the drop of the excitation voltages on the line impedances. Meanwhile, the nonlocal conductances \( G'_{rl}, G'_{lr} \) at the device get a positive correction term proportional to the ground line impedance and both local conductances. This correction can be interpreted as a voltage divider effect: if the ground line impedance is finite, at the device ground there is a residual voltage excitation proportional to the conductance of one side, which then drops over the opposite side. This is the first-order effect corrected for in ref.\[1\]. Note that this voltage divider effect is an attenuated mirror image of the local conductances. This has an important consequence for experiments: if a nonlocal conductance signature is not proportional to the local conductances, then it cannot be attributed to voltage divider effects.

II. EXPERIMENTAL VALIDATION

To validate experimentally the implementation of the measurement circuit effect corrections, we measured a three-terminal test resistor network using the measurement circuit depicted in Fig. 2. The currents are measured using a Basel 983 I/V converter on each of the left and right measurement terminals. AC voltage excitations at 15 Hz and 25 Hz are applied at the voltage bias terminals of the left and right I/V converters, respectively. The excitation frequencies were chosen to be much lower than the I/V converter low-pass cutoff frequency of 1 kHz to avoid finite frequency effects. The I/V converters have an input impedance of 33Ω that contributes to the total line resistances.

Fig. 2b–e show both the raw values of the measured conductance matrix \( G(V) \) and the transformed conductance matrix \( G'(U) \). The first effect of the correction is to rescale the voltage axis to account for voltage drops over the line resistances, which result in a reduced DC voltage bias at the device. As discussed in the previous section, the measured local conductances in Fig. 2b–d (blue dots) are smaller than the conductances at the device, since the AC voltage excitations at the device are smaller than those applied at the measurement terminals. The corrected local conductances (red dots) agree with those expected from the nominal \( Z_{lg} \) and \( Z_{rg} \) resistor values (solid grey lines). Finally, the raw measured nonlocal conductances in Fig. 2b, d (blue dots) have a spurious contribution arising from voltage divider effects. The finite ground resistance gives rise to a finite AC voltage excitation at the device ground terminal when exciting from either of the sides. The corrected nonlocal conductance (red dots) takes these effects into account, yielding values in good agreement with the nominal \( Z_{lg} \) resistor value (solid grey lines).

In Fig. 3 we show conductance measurements at 20 mK on a hybrid superconducting-semiconducting three-terminal device (Fig. 3b). An InAs nanowire (light grey, center) is contacted on its lower facet by an epitaxially-grown Al lead (blue). Gold ohmic contacts (yellow) are deposited on both ends of the nanowire, and electrostatic gates (red) are deposited on top: left/right cutters (lc/rc) and plunger (p). The line resistances are \( Z_l = Z_r = 1830 \, \Omega \) and \( Z_g = 915 \, \Omega \) and primarily originate from low-pass filters in the cryostat DC lines. The raw measured data (Figs. 3b, c) shows superconducting coherence peaks, typical for tunneling spectroscopy of these devices, whose energy fluctuates as a function of the cutter gate voltage, moving outwards whenever the conductance \( G_{ll} \) increases\[12\]. In Fig. 3d, e the raw nonlocal conductance \( G_{rl} \) shows voltage divider artifacts in the form of a suppressed mirror image of the local conductance \( G_{ll} \), as discussed in Section I1. Note that, like the local conductance \( G_{ll} \), the voltage divider effects are symmetric as a function of bias voltage. In the corrected datasets (Fig. 3d, e) the energy of the superconducting coherence peaks is nearly constant as a function of cutter gate voltage. As shown in Fig. 3e, the corrected nonlocal conductance at the device \( G_{rl} \) no longer shows voltage divider artifacts, and is predominantly anti-symmetric as a function of bias voltage.

In order to illustrate the dependence of \( G \) and \( G' \) on \( U \) and \( V \), we depict a measurement of \( G_{rl}(V) \) and \( G_{lr}(V) \) together with the transformed matrix elements \( G'_{rl}(U) \) and \( G'_{lr}(U) \) as a function of both left and right bias in Fig. 4. The measurement is from a superconductor-semiconductor hybrid device identical to the one in Fig. 1. \( G_{rr} \) and \( G_{ll} \) depend on both \( V \) and \( V' \) as a result of voltage divider effects. The nonlocal conductance \( G_{rl} \) shows artifacts stemming from voltage di-
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FIG. 3. a Three-terminal device micrograph and measurement circuit. b, c, Raw measured local (b) and nonlocal (c) conductances $G(V)$ when exciting the left measurement terminal, as a function of the applied DC voltage bias $V_l$ and left cutter gate voltage $V_{lc}$. d, e, Respective measurements corrected for measurement circuit effects. The vertical voltage axis has been transformed to the DC voltage $U_l$ at the left device terminal using Eq. (6). The conductances $G'_l(U)$ are now calculated with respect to the AC voltage excitation $dU_l$ at the left device terminal using Eq. (14).

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In summary, we have derived exact expressions (Eqs. 6 and 14) for correcting measurement circuit effects arising from finite line impedances in three-terminal electrical measurements, and validated them experimentally. These corrections, to first order, re-scale voltage biases and local conductance to account for voltage drops on the line impedances, as well as eliminate artifacts in the nonlocal conductance arising from voltage divider effects. This makes it possible to measure three-terminal devices in larger conductance regimes than otherwise possible, which is important for maximizing the signal-to-noise ratio of the nonlocal conductance.
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