Research On FPGA-based High-speed Data Optical Fiber Transmission

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Abstract—This article briefly introduces the principles and advantages of optical fiber transmission and the characteristics of the integrated IP core developed by Xilinx. Aiming at the advantages of optical fiber communication, Xilinx ZYNQ7000 series FPGA chips are used to design a high-speed data optical fiber transmission scheme based on FPGA. This solution uses the method of creating Block Design for design and development. It uses Verilog hardware description language and Vivado development software for experimental verification. In the FPGA simulation environment, the code is converted into a binary file and written to the chip through the JTAG interface for testing, and the experimental data is analyzed. As a result, it meets the design requirements of high-speed data transmission, which is of great significance to the research of high-speed data optical fiber transmission.

1. Introduction
With the rapid development of modern science and technology, people have made more in-depth research on communication technology. The high speed of communication and the high quality of communication are more important aspects. In future communication, whether it is wired communication or wireless communication, there are higher requirements for data exchange and processing capabilities. Optical fiber communication has the advantages of fast transmission speed, low loss, low capacity, low occupied bandwidth, and anti-electromagnetic interference. It is very suitable for high-speed data transmission. This article mainly uses the Aurora 64/66B IP core developed by Xilinx company to realize the fiber loopback communication of different interfaces on the board under the environment of the FPGA tool Vivado2018.3 software, the rate can reach 10Gbps, and the bit error rate test is carried out on this.

2. Optical fiber transmission
Optical transmission is a communication method that uses optical fibers as the propagation medium and light waves as carrier waves to transmit information, so it can also be called optical fiber transmission. Its transmission principle is to first convert the modulated electrical signal into an optical signal through a photoelectric conversion module, and then use light waves as the carrier in the entire optical fiber transmission system for information transmission. In optical fiber communication, the entire optical fiber system not only works It is only a single optical fiber, but many optical fibers gather to transmit information in the form of optical cables [1][2]. Optical fiber transmission has been developed for nearly a hundred years. Optical fiber transmission mainly takes large-capacity, high-speed, and long-distance transmission as the development advantages, which can be the only way out for data communication systems after the 21st century.
3. **Aurora 64 / 66B IP core**

There are multiple versions of Aurora. According to the differences in encoding methods, the most popular ones are 8B10B and 64B66B\textsuperscript{[3][4]}. Different encoding methods have different natural throughput rates. Among them, the 64/66B version has a different throughput rate. Highest.

### 3.1 Interface signal

Aurora IP is an IP packaged by Xilinx and available to users, as shown in Figure 1; there are many clock interfaces, data interfaces, and status signals. Among them, the physical layer reference clock refclk1\_in and init\_clk need to be based on the clock provided by the development board. The frequency is determined, and user\_clk and sync\_clk are generated by the shared clock logic module; GT\_AERIAL\_RX and GT\_AERIAL\_TX are the data transceiver interface of the module; in addition, CORE\_STATUS is the status signal of the module.

Aurora64B/66B is a communication protocol with multiple links. At the same time, the serial communication technology using the Aurora64/66B protocol can solve the problems of parallel communication technology such as multiple lines, complex wiring, and low anti-interference ability. The Aurora protocol can be used to transmit data between devices with GTX transceivers. The Aurora IP core released by Xilinx can use 16 effective continuous GTX, GTH or GTY transceivers at any supported line rate. Run to provide a low-cost, universal data channel. The integration of FPGAs is getting higher and higher thanks to the rapid development of chip manufacturing processes. Each high-speed serial transceiver can have one channel, and in units of blocks, each block contains a four-channel phase-locked loop and four serial ports. High-speed transceiver, four transceivers share the same reference clock\textsuperscript{[5][6]}.

### 3.2 Interface signal

Xilinx's aurora IP provides two different usage modes, one is the frame interface mode, and the other is the data stream interface mode. The frame interface mode is that all data is valid only when it is framed. At the same time, the Aurora interface can indicate the transmission and end of frame data through the tready, tvalid and tlast signals; the data stream interface mode is a streaming data transmission, as long as the tready and tvalid signals At the same time, the Aurora core is ready for data transmission, and in order to avoid data loss, when the data reaches rx, it must be read immediately. Here, the Aurora interface adopts the frame interface mode.

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**Fig.1** Aurora 64B/66B IP
4. Design
The overall solution includes a ZYNQ module, two cache modules, and two Aurora modules. Among them, the ZYNQ module has a data movement module, which can move data from the source address to the destination address. The logical relationship between them is shown in Figure 2.

![Scheme design drawing](image)

Fig.2 Scheme design drawing

It can be seen from Figure 2-1 that the ZYNQ module acts as a data processing center. Data is generated in the ZYNQ module. Cache module 1 and Aurora module 1 together form a data sending module, and cache module 2 and Aurora module 2 together form a data receiving module. The data received by ZYNQ can be compared with the data sent.

In the environment of FPGA tool Vivado2018.3 software development, create a Block Design, add ZYNQ7 Processing System and DMA module to it. It should be noted that there are multiple DMA modules packaged by Xilinx, and AXI Direct Memory Access IP should be selected here. The AXI interface can make development more efficient and more convenient for later development. Also add the FIFO module as a buffer module, and for the FIFO module, you can choose AXI4-Stream Data FIFO IP, which also uses the AXI interface protocol. In addition, Aurora 64B66B IP must be added. The IP setting parameters here should be selected according to the clock provided by the specific development board, and the interface mode should be frame mode. Finally, create a top-level file, loop back the high-speed interface, and instantiate the Block Design into the top-level file.

5. Bit error rate test
ChipScope Pro integrated bit error rate test core controller IP core is designed for different FPGA series and is customizable to evaluate and monitor the working status of GTX/GTH/GTP transceivers[7]. The bit error rate test is the IBERT test. IBERT is a tool provided by Xilinx to test high-speed serial transceivers. We can use the IBERT IP in Vivado 18.3 to generate IBERT test projects and perform IBERT tests on selected solutions.

6. Test results and analysis
From the IBERT test result Figure 3, it can be seen that there are two channels in the Link state, corresponding to each Aurora module having one receiving and one sending, so it is two Link states; in addition, you can see that the rates of the two Link states are both It is 10.000Gbps, and the bit error rate is $10^{-13}$, which meets the design requirements.

![IBERT test chart](image)

Fig.3 IBERT test chart
7. Conclusion
This article is based on the FPGA environment and uses the IP construction mode to create a Block design in Vivado 18.3 for development. The development efficiency is greatly improved, and the Aurora interface protocol is briefly introduced, the high-speed data fiber transmission scheme is designed, and the design verification is carried out at the same time to realize the difference in the board. Optical fiber transmission of high-speed data between interfaces is of great practical value to optical fiber high-speed data transmission.

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