Upgrade of the ALICE Inner Tracking System

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Abstract

The Inner Tracking System (ITS) is the key ALICE detector for the study of heavy flavour production at LHC. Heavy flavor can be studied via the identification of short-lived hadrons containing heavy quarks which have a mean proper decay length in the order of 100-300 \( \mu m \). To accomplish this task, the ITS is composed of six cylindrical layers of silicon detectors (two pixel, two drift and two strip) with a radial coverage from 3.9 to 43 cm and a material budget of 1.1 \% X0 per layer.

In order to enhance the ALICE physics capabilities, and, in particular, the tracking performance for heavy-flavour detection, the possibility of an ITS upgrade has been studied in great detail. It will make use of the spectacular progress made in the field of imaging sensors over the last ten years as well as the possibility to install a smaller radius beam-pipe. The upgraded detector will have greatly improved features in terms of: the impact parameter resolution, standalone tracking efficiency at low \( p_t \), momentum resolution and readout capabilities.

The usage of the most recent monolithic and/or hybrid pixel detector technologies allow the improvement of the detector material budget and the intrinsic spatial resolution both by a factor of three with respect to the present ITS. The installation of a smaller beam-pipe reduces the distance between the first detector layer and the interaction vertex. Under these assumptions, simulations show that an overall improvement of the impact parameter resolution by a factor of three is possible.

The Conceptual Design Report, which covers the design and performance requirements, the upgrade options, as well as the necessary R&D efforts, was made public in September 2012. An intensive R&D program has been launched to review the different technological options under consideration. The new detector should be ready to be installed during the long LHC shutdown period scheduled in 2017-2018.

Keywords: ALICE, Inner Tracking Systems, Silicon Detectors.

1. Introduction

The general upgrade plans for the ALICE experiment, its experimental strategy and the long-term physics goals are discussed in [1]. As described there, future physics topics require a significant improvement of the measurements of heavy-flavour hadrons, quarkonia and low-mass dileptons at low transverse momenta. Furthermore, the upgraded ALICE detector will be able to make full use of a high-luminosity LHC \((L = 6 \times 10^{27} \text{ cm}^{-2}\text{s}^{-1})\) for Pb–Pb through the improvement of the readout-rate capabilities. The upgraded detector system will allow the inspection of up to 50 kHz Pb–Pb and 200 kHz pp interactions.

The upgrade of the Inner Tracking System (ITS) is an essential ingredient for the improved resolution of the distance of closest approach between a track and the primary vertex (impact parameter resolution), the standalone ITS tracking performance as well as the readout-rate capabilities. The Conceptual Design Report for the Upgrade of the ALICE ITS detector [2] covers the current status, the ongoing R&D efforts, the design options, the choice and ongoing tests of the different technological options as well as the expected detector and physics performance.

2. Current and Upgraded Inner Tracking System

The current Inner Tracking System (ITS) of ALICE is composed of six cylindrical layers of silicon detectors placed around the LHC beam-pipe and covers the central rapidity region \(|\eta|<1\) [3]. Three different technologies are in use: two layers of Silicon Pixel Detector (SPD), two layers of Silicon Drift Detector (SDD) and two layers of double sided Silicon Strip Detector (SSD). The geometrical parameters of the layers (radial position, length along beam axis, spatial resolution) and the material budget are summarized in Tab. [1].

The present ITS was designed and optimized mainly to obtain a good track extrapolation to the vertex for tracks reconstructed in the surrounding detector, the Time Projection Chamber (TPC). Therefore, the ITS improves significantly the impact parameter resolution \(d_0\) which is a prerequisite for accessing decay channels with a short decay length. Furthermore, the four layers equipped with drift and strip detectors provide a measurement of the specific energy loss \(dE/dx\) and are therefore used for particle identification.

As described in great detail in [2] chap. 3, the proposed upgrade of the ITS will make use of the foreseen reduction of

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the LHC beam-pipe radius from currently 2.94 cm to 1.98 cm which will allow a significant decrease of the distance between the first detector layer and the interaction vertex. The material budget can be significantly reduced by using ultra-thin hybrid pixel detectors or monolithic silicon pixel detectors allowing X/X₀ = 0.5% or X/X₀ = 0.3% respectively. Furthermore, state-of-the-art hybrid pixel detectors would allow smaller pixel sizes of e.g. 30×30 µm², while monolithic pixel detectors are currently featuring pixel sizes of 20×20 µm², both significantly smaller than the current size of 50×425 µm².

Both semi-analytical and Monte-Carlo methods have been exploited to estimate the transverse momentum (p_t) dependence of the impact parameter resolution in azimuth (r_θ) and beam (z) direction, the p_t resolution, as well as the tracking efficiency by varying the number of layers, their radii, material budget and their intrinsic resolutions.

Different design options are currently being reviewed and compared in terms of space, design feasibility, integration, manufacturing costs, as well as standalone tracking efficiency and capability. Furthermore, an increase of the read-out rate requires a complete redesign of the current ITS due to the rate limitations of the current SDD (read-out time approx. 1 ms). The characteristics of the most promising upgrade scenario are given in Tab. 2.

The performance of the current ITS is compared against the expected performance of the proposed upgrade scenario in the Figs. 1, 2 and 3 for both, the ITS stand-alone and ITS-TPC combined tracking mode. Figure 1 displays the pointing resolution to the vertex for charged pions. Both the r_θ and z components are shown in the plots. The pointing resolution is mostly determined by the properties of the first layers. As an example, at p_t of about 400 MeV/c, an improvement of 3 and 5 is achieved for the r_θ and z components respectively. It should be noted that for the present ALICE set-up the ITS-TPC combined tracking provides at high p_t a sizeable improvement with respect to the ITS stand-alone tracking. In the case of the upgrade ITS, adding the information of the TPC does not yield any further improvement.

Figure 2 illustrates the improvements in the transverse momentum for the current ITS and the upgrade scenario.

Figure 3 shows the tracking efficiency for charged pions for the current ITS and the upgrade scenario.
mentum ($p_t$) resolution. For the ITS stand-alone tracking mode, the upgrade scenario yields a dramatic improvement (at least a factor 3). The improvement in the ITS-TPC combined tracking mode is due only to the reduction of the material budget in the innermost layers.

Finally, figure 5 exhibits a comparison of the tracking efficiency between the current ITS and the upgrade scenario in a central Pb–Pb collision at maximal LHC energy ($\sqrt{s_{NN}} = 5.5$ TeV, $dN_{ch}/dp_t = 2000$). The stand-alone tracking efficiency of the upgrade scenario will surpass the achievable efficiencies of the current ITS design in ITS-TPC combined tracking mode. Especially towards lower $p_t$, a significant enhancement in terms of statistics can therefore be expected.

3. Technical Implementation

An R&D program has been launched to study the various technical options, such as choice of technology and architecture. More details can be found in [2, chap. 4].

As described in the previous section, the new ITS will consist of seven layers of silicon tracking detectors. The two options currently under study are:

- **Layout 1**: All seven layers are built using silicon pixel detectors.
- **Layout 2**: The innermost three layers are equipped with silicon pixel detectors followed by four (outer) layers of silicon strip detectors.

Table 3 summarizes the technical specifications for the inner and outer layers:

| Parameter             | Inner layers | Outer layers |
|-----------------------|--------------|--------------|
| Chip Size             | (15 × 30) mm |              |
| Pixel Size (r-φ)      | 20–50 µm     | ≤ 70 µm      |
| Pixel Size (z)        | 20–50 µm     | ≤ 2 cm       |
| Readout Time          | ≤ 30 µs      | ≤ 30 µs      |
| Hit Density           | 150 hits/cm$^2$ | 1 hit/cm$^2$ |
| Radiation Levels      |              |              |
| 700 krad (TID)        | 10 krad (TID) |              |
| 1 × 10$^{13}$ n$_{eq}$/cm$^2$ (NIEL) | 3 × 10$^{11}$ n$_{eq}$/cm$^2$ (NIEL) |

Two pixel detector technologies are under consideration, namely hybrid and monolithic silicon pixel detectors.

**Monolithic sensors** embed the sensing diode and front-end electronics on the same silicon chip. They are produced using commercial CMOS technologies that are optimized for large volumes and are therefore very cost-effective. The sensor can be thinned down to 50 µm, offering a significant reduction in material budget. Pixel sizes of 20 µm × 20 µm or less are standard with these technologies. The quadruple-well CMOS Imaging Sensor (CIS) process provided by TowerJazz was identified as the most promising candidate and has thus been selected for a dedicated R&D within ALICE.

One key question to be addressed within such R&D is the radiation hardness of CMOS sensors in view of the expected radiation levels foreseen in ALICE. Additional issues are the design of an optimized pixel cell and of a low power readout architecture.

**Hybrid pixels** are a mature technology presently employed in all four major LHC experiments. In a hybrid detector, the sensor and the front-end electronics are fabricated on two separate chips and then mated with the bump bonding technique. This offers the advantage of optimizing the sensor and its front-end electronics separately at the expense of extra thickness and cost. The radiation load foreseen in the ALICE ITS does not present a concern for this type of sensors. State-of-the-art hybrid pixels have a cell size of 50 µm × 50 µm, but the evolution of the interconnection technology is expected to put cell sizes of 30 µm × 30 µm soon within reach. In the recent months the focus on the hybrid pixel detectors was on the production of assemblies with the final thicknesses and the completion of the production of the first edgeless epitaxial silicon sensors.

Two readout architectures are under study:

The first architecture is based on the **rolling shutter technique**. The time between two consecutive readouts of the same row defines the integration time, which is of the order of 100 µs for state of the art CMOS sensors. This time must be significantly reduced to comply with the 50 kHz interaction rate. A sensor with an extension of the rolling shutter, based on the low power architecture of ULTIMATE [4], is under development for the ITS upgrade. This new sensor, called MISTRAL, is intended to increase the readout speed by a factor of at least four and to improve the radiation tolerance by one order of magnitude. The estimated power density for these chips is ≤ 400 mW/cm$^2$.

The second topology employs a **sparsified readout** of the pixel matrix, so that only zero-suppressed data are transferred to the periphery. For a scenario of 100 tracks per cm$^2$ per event and a cluster multiplicity of eight, the readout requires 300 ns.

Even considering some inhomogeneity in the hit distribution, the transfer of only zero suppressed data from the matrix to the periphery allows a full scan in a time on the order of 1 µs. It has been estimated that the power consumption of this priority encoding scheme is less than 30 mW/cm$^2$.

A design and prototyping effort is underway to identify the most suitable readout approach. The choice between the two schemes will depend on readout speed, power consumption, and noise of the prototypes.

To simulate the impact of the expected radiation levels systematic irradiation tests using X-rays, protons and neutrons were carried out throughout 2012 and onwards on various sensor, analog and digital test structures. To disentangle the various radiation-induced effects, three types of structures are currently under investigation:

- Basic structures (diodes and transistors): 2 test structures were designed and implemented in TowerJazz 0.18 µm CMOS technology in order to study basic operational parameters such as threshold voltage, transconductance, and dark current as a function of radiation type and dose as

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2TowerJazz, [http://www.jazzsemi.com](http://www.jazzsemi.com)
well as of the layout. Test structures containing various types of NMOS and PMOS transistors and capacitors for different epitaxial thicknesses have already been produced in earlier runs and are available for radiation tests (RAL structures). Special test structures (TID_TJ180) consisting of various transistor types as well as breakdown diodes were developed and produced in the first half of 2012 (ALICE_ITS_TJ180).

- Digital structures: a test chip for dedicated SEU tests has been designed and implemented in TowerJazz 0.18 µm CMOS technology (SEU_TJ180) consisting of various RAM structures and shift registers to test the stability and reliability of switching states during irradiation with charged particles (see Fig. 4).

- Full sensor structures (including analog and digital front end electronics): MIMOSA32 prototype matrices were produced in TowerJazz 0.18 µm CMOS technology containing both analog and digital elements that allow the characterization of full sensor prototypes under irradiation and test beam conditions.

Figure 4: Picture of the SEU_TJ180 structure indicating the dimensions and different blocks (right) and picture of one SEU_TJ180 structure mounted on the test socket (left).

Beam tests were performed in summer 2012 at the CERN-SPS with 60-120 GeV particles, which allowed evaluating the chip detection performances at two different coolant temperatures ($T_c = 15^\circ$C and $30^\circ$C), before and after a combined radiation load of 1 Mrad and $10^{13}$ $n_{eq}$/cm$^2$. The study is based on different MIMOSA32 dies, tested individually on a beam telescope composed of four pairs of microstrip detectors. The detection performances (e.g. signal charge collected, pixel noise, signal-to-noise ratio (SNR), hit cluster properties, detection efficiency) were derived from a total sample of about 50,000 tracks reconstructed in the beam telescope and traversing the pixel array under test.

As an example, the hits reconstructed in the square pixels exhibited a typical cluster charge of ~1100-1200 electrons, essentially concentrated in 2 to 4 pixels, about 40-50 % of the charge being collected by the seed pixel. Figure 5 displays the distribution of the charge collected by the cluster seed pixel in the deep pwell case. The measurements were performed at $T_c = 30^\circ$C before and after irradiation. The radiation gives no observable effect on the charge collection efficiency, but increases the noise by more than 50%.

The noise values observed reproduce those measured in the laboratory ($\lesssim 20$ $e^-$ ENC before irradiation and $\lesssim 30$ $e^-$ ENC after irradiation, at $T_c = 30^\circ$C). The SNR varies accordingly from 30-35 (MPV) before irradiation, depending on the pixel variant, to 20-25 for the aforementioned combined radiation load. The detection efficiency, which is about 100% before irradiation, remains nearly unchanged after irradiation (e.g. the deep pwell pixels exhibits still a detection efficiency of $99.87 \pm 0.07%$(stat)).

Furthermore, an important aspect of the implementation will be the layout of the modules for the inner and outer pixel layers. First proposals for the data and power connection schemes have been worked out and are under investigation. Special emphasis is laid on the design and interconnection of a low mass bus cable which will provide power and data connections.

Progress has also been made in the development of hybrid pixel assemblies and strip detectors. Specifically, a production of thin hybrid assemblies with a total thickness of 150 µm has been demonstrated using dummy components. Furthermore, silicon strip sensors for the ALICE ITS upgrade have been designed and first prototypes have been produced, which will be used for module assembly and TAB-bonding tests.

The main objectives in the coming months are the completion of the radiation hardness studies of the TowerJazz struc-
tures and performance tests of pixel sensor prototypes, both in laboratory and test beam. Furthermore, the studies on the module layout and the data and power transmission scheme will be continued.

4. Mechanical layout and Cooling

The design of the mechanical support structure and the services are driven by external constraints like required detector layout (layer grouping in three barrels, see Tab. 2 and rapid accessibility for the installation. At the same time, inner constraints like sensor size (and choice), power dissipation and therefore cooling choice, and the total material budget have to be considered. A summary is given in Tab. 4.

The ITS mechanical design is conceived as a two-barrel structure: Inner Barrel and Outer Barrel (see Fig. 6). The design effort has been concentrated so far on the Inner Barrel due to the more stringent requirements in terms of material budget. The Inner Barrel has a modular structure consisting of 3 concentric layers, each segmented in the azimuthal direction in modules referred to as “staves” (see Fig. 7).

The stave is the smallest operable part of the detector. It is formed by 9 silicon pixel chips (15 mm × 30 mm × 50 µm thick) aligned in z to form a detection area of 15 mm × 270 mm, which are flip-chip bump bonded on a flex-cable bus. The stave includes a carbon fiber support structure, which provides a light and stiff frame for the sensors and the electrical bus. Additionally this support integrates the cooling interface to remove the dissipated heat.

The different stave layouts which have been investigated can be divided in two groups that refer to two different cooling concepts under study: cold plates and cooling pipes.

In the cold plates concept the cooling is provided by a refrigerant fluid (monophase or biphase) flowing in a microchannels structure, which is either in a silicon (microchannel section area 0.04 mm²) or in a polyimide (microchannel section area 0.16 mm²) substrate. The plate is in thermal contact with the front-end electronics while the mechanical structure has to support the sensors with the bus and the cold plates.

In the cooling pipes option the cooling is provided by a refrigerant fluid (monophase or biphase) flowing in 1.5 mm outer diameter tube (0.035 mm wall thickness). The tube is embedded in the mechanical structure to which the sensors are glued.

Heat is transferred from the sensors to the pipes by the highly thermally conductive structure.

Different prototypes of the mechanical structures for the two stave concepts have been produced, as for example Open Shell structures as well as Wound Truss Structure (see chap. 5 for details). The prototypes were tested regarding their stiffness and weight, ease of assembly and handling. The weight varies from 0.6 g to 1.4 g, for the structures produced from materials like carbon fiber T300 prepreg and M60J 3k (3000 filaments). Structural simulations and deformation tests resulted in a reasonable sag of below 6 µm over a total length of 127 mm at twice the expected load factor. The first natural frequency was found at 596 Hz which proves the stiffness of the structure.

Several cooling schemes fully integrated in the support structure and based on different refrigerant media (air, liquid and two-phase) have been studied.

A solution using microchannels etched on a silicon substrate has been prototyped on a 4 inch silicon wafer with a thickness of 380 µm and 0.1 - 0.5 Ω-cm p-type. The microchannels are covered with a silicon layer 50 µm thick. The preliminary criteria adopted to choose the size of the silicon microchannels (200 µm × 200 µm) are based on the studies published in [7]. The test performed so far, focused on thermal characterization of the single frame, confirmed the high potentiality of this cooling concept when applied to the ALICE requirements.

| Parameters                          | Inner Barrel | Outer Barrel |
|-------------------------------------|--------------|--------------|
| Beampipe outer radius (mm)          | 20           | -            |
| Beampipe wall thickness (mm)        | 0.8          | -            |
| Detector Technology                 | Pixel        | Pixel–Strip  |
| Number layers                       | 3            | 4            |
| Mean radial positions (mm)          | 22, 28, 36   | 200, 220, 410, 430 |
| Stave length in z (mm)              | 270, 270, 270 | 843, 843, 1475, 1475 |
| Power consumption (W/cm²)           | 0.3 ± 0.5    | ≤ 0.5 mW/strip |
| Material per layer (% of X)         | 0.3          | ≤ 1.0        |
| Working temperature (°C)            | 30           | 30           |

Figure 6: ITS modular mechanical structure.

Figure 7: Drawings of the three innermost layers of the new ITS: from single stave to barrel.
Another option is a Polyimide based Micro-Channels Heat Sink (MCHS) [8]. An analytical thermo-fluid dynamic study has been carried out to find the best microchannel section (800 μm × 200 μm) fulfilling the operational requirements. First prototypes were tested regarding their thermal behavior using PT100 sensors as well as thermographic imaging and a kapton heater. Tests revealed a uniformly increasing temperature along the flow direction. In particular at a water flow rate of 2 l/h and with a heat flux of 0.3 W/cm², the average temperature is less than 23°C with a maximum value of 25.4°C.

A third option is the usage of cooling pipes suitable for either single phase or evaporative cooling. Two different prototypes have been tested: a) Wound truss structure with pipes and uniform carbon plate b) Wound truss structure with only pipes. As an example, option b) is shown in Fig. 9 where the thermal contact is enhanced by a graphite foil wrapped all around the pipes. The thermal results obtained with option b) are shown in Figure 9. The test has been carried out using the flow rate of 8 l/h with the water temperature at the inlet of 14.8°C. The power density applied is 0.3 W/cm². The average temperature is less than 31°C with a maximum value of 33°C.

![Figure 8: Picture of the wound truss structure with pipes (right) and schema of the section view (left).](image)

![Figure 9: Thermographic images of the heater surface with water flow rate of 8 l/h and power consumption of 0.3 W/cm². The temperature profile is taken along the center the structure.](image)

The material budget estimated for the stave prototypes as mentioned above fulfill the mechanical and thermal requirements of the new ITS, although further studies and optimization are still needed. All prototypes results in a mean value of the material budget below 0.31X/Xo.

As an example, the material budget of the prototype using carbon fiber wound structure with embedded polyimide tubes are reported in Tab. 5. It accounts for the percentage of surface covered by both top and bottom carbon fibers. The wall of the polyimide tube is 35 μm thick and the water has been considered as coolant. In addition we accounted for 2 layers of glue 100 μm thick assuming a coverage of 50% for the layer between the structure and the silicon.

The mean value for this prototype is approximately 0.26X/Xo. It is important to point out that this structure is slightly lighter than the other options mentioned above, but it has reduced thermal performance. The R&D activity on this structure is important because it will allow us to further reduce the material budget if a low power density (≤0.3 W/cm²) chip is chosen for the final design.

### Table 5: Wound truss structure with pipe prototype: list of components and their contribution to the mean material budget estimate.

| Material                       | Surface (%) | Thickness (μm) | Xo (cm) | X/Xo (%) | x (%) |
|--------------------------------|-------------|----------------|---------|----------|-------|
| CFRP filament                  | 100         | 70             | 25      | 0.035    | 12.6  |
| Polyimide Tubes                | 19          | 70             | 28.6    | 0.005    | 1.8   |
| Water                          | 19          | 1450           | 36.1    | 0.06     | 22.8  |
| Glue (CFRP - silicon)          | 50          | 100            | 44.4    | 0.01     | 4.4   |
| Silicon                        | 100         | 50             | 9.36    | 0.054    | 20.7  |
| Glue (silicon - bus)           | 100         | 100            | 44.4    | 0.022    | 8.7   |
| Electrical bus                 | 100         | -              | -       | 0.075    | 29.0  |
| Total                          |             |                |         | 0.26     |       |

∗ Contribution to the total X/Xo (%)

More details regarding the planned mechanical layout, the material budget contributors, the services, the integration procedure and the different cooling options can be found in [2] chap. 5.

### 5. Time Schedule

Although the ALICE ITS upgrade schedule is not linked directly to the LHC upgrade and its schedule, the installation of a new ITS will require a long shutdown (LS) and, therefore, will naturally have to be in phase with the installation of upgrades for the other LHC experiments, planned as of today for the 2013/14 and 2017/2018 shutdowns.

In this respect, the ALICE ITS upgrade will use the time between 2012 and 2014 for the R&D phase, for prototyping and for testing. The production and pre-commissioning phase will start in 2015. The commissioning and the installation is planned for the long LHC shutdown period in 2017/2018. Details are given in Tab. 6.

### Acknowledgment

The content of this contribution represent only a superficial overview on the studies unveiled in the Conceptual Design Report [8]. Therefore, I would like to express my gratitude to the various contributors of the CDR.
| Year       | Activity                                                                 |
|------------|---------------------------------------------------------------------------|
| 2012 – 2014| **R&D**                                                                   |
| 2012       | finalization of detector specifications; evaluation of detector technologies (radiation and beam tests); first prototypes of sensors, ASICs, and ladders (demonstrators); |
| 2013       | selection of technologies and full validation; engineering design for sensors, ASICs, ladders, data links; engineering design for support mechanics and services; Technical Design Report; |
| 2014       | final design and validation                                               |
| 2015 – 2018| **Construction and Installation**                                         |
| 2015 – 2016| production, construction and test of detector modules                     |
| 2017       | assembly and pre-commissioning in clean room                              |
| 2018       | installation in the cavern                                                |

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