DIFFERENTIABLE NETWORK PRUNING FOR MICROCONTROLLERS

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ABSTRACT

Embedded and personal IoT devices are powered by microcontroller units (MCUs), whose extreme resource scarcity is a major obstacle for applications relying on on-device deep learning inference. Orders of magnitude less storage, memory and computational capacity, compared to what is typically required to execute neural networks, impose strict structural constraints on the network architecture and call for specialist model compression methodology. In this work, we present a differentiable structured network pruning method for convolutional neural networks, which integrates a model’s MCU-specific resource usage and parameter importance feedback to obtain highly compressed yet accurate classification models. Our methodology (a) improves key resource usage of models up to 80\(\times\); (b) prunes iteratively while a model is trained, resulting in little to no overhead or even improved training time; (c) produces compressed models with matching or improved resource usage up to 1.7\(\times\) in less time compared to prior MCU-specific methods. Compressed models are available for download.\(^1\)

1 INTRODUCTION

There’s an increasing interest in bringing on-device neural networks to what is arguably the smallest-scale viable compute platform: microcontroller-powered IoT devices. The roadblock to this, however, is the limited compute power. Microcontroller units (MCUs) are single-chip systems, typically consisting of a single-core processor (such as ARM M-series), on-chip persistent Flash and temporary SRAM memories, other peripherals (e.g. sensors, microphones, radio). Table 1 compares technical specifications of MCUs against data center, mobile and micro-computer hardware. MCUs are designed with cost and power-efficiency in mind, which is primarily achieved by reducing the on-board memory and compute resources. The data shows that, even when compared to micro-computers like Raspberry Pi, MCUs have orders of magnitude less storage and SRAM (GBs vs 100s KB) and a slower processor (GHz vs 100s MHz).

For many practitioners, it is not trivial to work around the resource scarcity of microcontrollers. As a result, applications choose to offload the execution of neural networks to a more capable device, such as a smartphone or a remote “cloud” backend server. This brings numerous disadvantages, such as a lowered degree of privacy, complete reliance on a working communication link, increased response latency, and increased power usage for radio communication.

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Figure 1. Deep learning inference on an MCU illustrated using relevant components. A flat memory hierarchy and its limited capacity impose significant constraints on the network architecture.

To see what properties the resource scarcity imposes on neural networks, let us take a more detailed look at how a neural network’s execution may be mapped to a microcontroller (Fig. 1), such as via the TensorFlow Lite Micro runtime (David et al., 2020):

- Each layer of a neural network will be executed in some predefined order, one at a time and in its entirety.
- A layer is executed by loading its parameters (weights) from Flash, loading its input from SRAM and writing the output back to SRAM.
- All constant data, such as weights of a neural network and program code, are stored in the read-only Flash memory. Therefore, the size of a neural network is limited by Flash (e.g. \(\leq 64\text{KB}\)).
As a compute platform for deep learning, microcontrollers are the most resource-constrained yet the most power-efficient and cheapest platform. The contributions of this work are as follows:

- All temporary intermediate data, including activation matrices, will be stored in SRAM. Therefore, a neural network’s peak activation size / memory usage is limited by the amount of SRAM (e.g. ≤ 64 KB).

As a compute platform for deep learning, microcontrollers pose unique challenges that do not similarly manifest on other platforms. The need to constrain SRAM usage, a relatively slow processor and orders of magnitude less resources requires further specialist research than what is typically explored in GPU/mobile-scale neural network design and compression. In fact, the need for MCU-specific methodology has spawned a research subfield called TinyML, which includes runtime design (David et al., 2020; Liberis & Lane, 2019), optimised layer implementations (Lai et al., 2018) and task-specific MCU-sized model discovery (Fedorov et al., 2019; Liberis et al., 2021; Banbury et al., 2020).

In this work (Figure 2), we tackle this problem through the use of budgeted differentiable network pruning. We employ bi-level gradient descent optimisation to learn the sizes of each layer in the network, resulting in iterative compression that is interleaved with network training and has little overhead. Our methodology formulates model size, peak memory usage and latency constraints as resource budget requirements and incorporates them into pruning as differentiable objectives. This achieves MCU specialisation currently absent from pruning literature and, compared to other MCU-level compression methods, the use of pruning and precise objectives achieves faster compression while correctly targeting resource bottlenecks.

The contributions of this work are as follows:

- We devise a pruning method suitable for finding MCU-sized models. Compared to related MCU specialist work, our methodology is unique in precisely targeting resource usage for arbitrary convolutional neural networks and offering fast compression with little to no overhead during training (or even accelerating it).
- We perform ablation and comparison studies, showing that each aspect of MCU specialisation is essential for achieving performant MCU-sized models.
- We present highly compressed models for eight architecture and dataset combinations at a variety of MCU-friendly resource usage vs. accuracy trade-off points.

We improve key resource usage up to 1.7× compared to related work and up to 80× compared to original models. TensorFlow Lite-compatible compressed models are freely available for download.

## 2 RELATED WORK

This section will describe how our methodology fits within the wider taxonomy of pruning algorithms and compare it to existing methods for MCU deep learning.

Our work has several methodological specifics, which complicate a direct comparison to most related pruning work. Ideally, we would compare against a structured pruning method that works during training (same mode), targets user-specified resource budgets, achieves high compression ratios and considers peak memory usage to produce MCU-compatible models. Seeing as our work is unique in this, we are only able to compare against other MCU-specific work for TinyML datasets, against other GPU-/mobile-level structured budgeted pruning methods for CIFAR-10, and address remaining evaluation through ablation studies.

### 2.1 Network pruning

Network pruning removes parameters from a network that are deemed the least important for generalisation. This inherently introduces a trade-off between a network’s predictive performance (here, classification accuracy) and its resource footprint. Given a wide variety of pruning methodology available (Blalock et al., 2020), comparison can be made not only by the degree of compression achieved but also mode, speed, and other aspects.

We classify our methodology as structured, during-training, iterative, budgeted and differentiable pruning, with each category explained below.

**Structured vs unstructured pruning.** Pruning is often used to obtain sparse models, which require sparse multiplication implementations or hardware to execute efficiently. (Anwar et al., 2015) In contrast, we use structured pruning, which removes entire channels/filters in convolutional layers and units/neurons in fully-connected layers. This effectively performs hyperparameter adjustment, resulting in a dense model that can be executed efficiently.

| Device          | Cores | Freq. (GHz) | RAM (GB) | Storage (GB) | Power (W) | Price ($) |
|-----------------|-------|-------------|----------|--------------|-----------|-----------|
| NVIDIA A100 GPU| 6912  | 1.4         | 40       | —            | 400       | 12,500    |
| Galaxy S7 Smartphone | 4  | 1.6–2.3     | 4        | 32/64        | 11.5      | 850       |
| Raspberry Pi 3B+ | 4    | 1.4         | 1        | 32–512       | 2.3       | 40        |
| NUCLEO-F767ZI (M7) | 1   | 0.216       | 0.000512 | 0.002        | 0.3       | 9         |
| NUCLEO-F446RE (M4) | 1   | 0.180       | 0.000128 | 0.000512     | 0.1       | 3         |

Table 1. Specifications of a high-end GPU server, a smartphone, a micro-computer and Nucleo development boards with ARM’s Cortex M7 and M4 microcontrollers.
Budgeted vs “opportunistic” pruning. Resource usage-unaware pruning methods typically use sparsity (the proportion of channels/units removed) to describe the extent of model compression. In practice, this is too coarse to target resource constraints: the same level of sparsity can yield different model sizes, FLOPs, etc. A popular way to achieve resource-awareness is to add sparsifying group $L_1$ regularisation (Gordon et al., 2018; Liu et al., 2017), followed by tuning its strength until desired resource usage is reached. Purpose-made budgeted pruning (Lemaire et al., 2019; Ning et al., 2020), such as this work, allocates resources outside of training loss, and thus does not rely on remaining channels to generalise in spite of extra regularisation or subsequent fine-tuning. Learning individual layer sizes also allows us to target bottleneck layers for peak memory usage.

Pre-, during- and post-training pruning. Post-training methods use a converged model, often followed by fine-tuning to recover any lost accuracy. “During-training” methods do not require a converged model, thereby combining fine-tuning and training into the same process, saving time. Pre-training methods use weight initialisation and gradient-flow information (Wang et al., 2020) to decide what to prune before training or very early on. This also reduces training costs, albeit at the cost of a lower final model performance.

Differentiable vs non-differentiable pruning. Differentiable pruning methods allow for efficient iterative bi-level optimisation: both pruning and training are performed using gradient descent. (Ning et al., 2020) Alternatives, such as evolutionary search, are inevitably more costly or need to rely on a proxy for a network’s accuracy. (Liu et al., 2019)

Iterative vs single-shot pruning. Incremental pruning was shown to allow the model to better recover from parameter loss at high pruning ratios (Han et al., 2015). Differentiable pruning happens iteratively which allows this recovery to happen during training, not at subsequent fine-tuning.

2.2 Deep learning for microcontrollers

Designing MCU-compatible neural network architectures is a challenging task due to the need to obtain a sufficiently high predictive performance while maintaining a sufficiently small resource footprint. Existing MCU-specific deep learning methods that achieve this can be classified into (a) model compression methods applied to manually designed networks, such as weight quantisation or binarisation (Zhang et al., 2017; Mocerino & Calimera, 2019), pruning (this work) or channel search (Banbury et al., 2020); (b) neural architecture search (NAS) methods that change the connectivity of the network’s layers (Lin et al., 2020a). Search methods can leverage simple pruning as a nested step to further reduce resource footprint of a candidate network (Liberis et al., 2021; Fedorov et al., 2019).

Out of all prior methods, the closest work to ours is “MicroNets” (Banbury et al., 2020), which uses differentiable architecture search to find layer sizes for particular task-specific architectures. Provided with a backbone architecture, the method works by masking each layer at a pre-defined set of widths (10%, 20%, ..., 100%)—eventually, only one will be included in the final architecture, followed by fine-tuning. Experimentally, we find that both methods can discover models with similar classification accuracy and resource usage given the same baseline architecture. Our method, however, offers several additional benefits: (1) we use a precise peak memory usage calculation which is accurate for network architectures with branches/parallel paths (see Section 3.1); (2) improved running time: compared to architecture search, the pruning has negligible overhead, requires no fine-tuning and happens during training; (3) more efficient allocation of the resource budget by operating at a per-channel granularity, not increments of 10%.

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Here, we describe (a) the neural network resource usage calculation for MCUs; (b) the task-specific pruning objective; (c) how the two are combined into a differentiable function of a network’s layer sizes; (d) how the latter is used to create a differentiable budgeted pruning algorithm. The unique

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In fact, pruning can even improve training time by switching to training a pruned model after channel-wise masks have converged.
addition of MCU-specific resource usage to pruning allows for the fast discovery of MCU-friendly models.

### 3.1 Execution constraints

We formulate model latency, peak memory usage and size constraints that are both differentiable and faithful to the real resource usage of a neural network, which efficiently guides pruning towards MCU-compatible models.

**Model latency.** To ensure that the pruning algorithm creates models that run sufficiently quickly, we implement a model latency constraint. For GPU-powered systems, model latency can be either directly measured or predicted using sophisticated models. (Chau et al., 2020) However, on MCU-powered systems, model latency can be predicted using simple metrics, such as the number of floating-point operations (FLOPs) or multiply-accumulate operations (MACs), due to the lack of any performance-enhancing features, like parallelism or caching (Liberis et al., 2021). Latency has also been shown to be a good predictor of power consumption on MCUs (Banbury et al., 2020), due to the processor staying the highest power state throughout the inference.

**Peak memory usage.** Peak memory usage at inference is an uncommon resource property to target in model compression. Most consumer hardware, such as devices presented in Table 1, have a multi-level memory hierarchy, with each layer offering more capacity at a slower access speed: multiple levels of fast but small SRAM data and instruction caches co-located with the CPU, followed by at least 1 GB of RAM. The latter is sufficient for most compressed neural networks. MCUs, on the other hand, lack a memory that resides on the same capacity vs. access cost trade-off as RAM, which forces applications and the operating system to work within the SRAM (here, ≈64–512 KB). Additionally, it is prohibitively expensive to use persistent storage, such as an SD card, for storing temporary results. (Liberis & Lane, 2019) Thus, to produce MCU-compatible architectures, we must ensure that the size of activation matrices at its largest remains below the SRAM capacity.

In the MCU network execution pipeline described earlier, the network’s layers are executed one by one, following a predetermined order, which is a valid topological ordering of layers (nodes) in a computation graph. However, not all topological orders yield the same peak memory usage: whenever the runtime has multiple layers that are ready to be executed (i.e. all of their inputs have been computed), the choice of which layer to execute determines which tensor memory buffers are allocated and deallocated at any given time, which affects the peak memory usage. Thus by considering different topological orders, we can compute the minimum attainable peak memory usage.

Computing the minimum achievable peak memory usage is not straightforward for arbitrary neural network computation graphs. In fact, the few previous works (Banbury et al., 2020; Fedorov et al., 2019) which have explored this problem, resorted to an imprecise under-approximation, which computes the maximum total size of input and output buffers for each operator individually, which does not consider their position within the execution order.\(^3\)

Instead, we adopt a precise approach based on dynamic programming, which efficiently enumerates all topological orderings of the computation graph (feasible for most CNNs) to find the one with the smallest peak memory usage (Liberis & Lane, 2019). In practice, to obtain gradients of layer sizes with respect to peak memory usage, it is sufficient to only run this algorithm on the forward pass of computing the objective and record which tensors formed the memory bottleneck—the peak memory usage is given by the sum of bottleneck tensor sizes, which is differentiable.

Using a precise computation makes a practical difference for networks that contain branches, which are commonplace in state-of-the-art convolutional networks (Sandler et al., 2018; Tan & Le, 2019; Cheng et al., 2019; He et al., 2016). In Section 4, we will empirically show that the two options for calculating peak memory usage—precise and imprecise—differ during pruning on MobileNet-v2 and ResNet networks, with the imprecise objective causing a violation of resource budget constraints.

**Model size.** All constant data, including program code and the weights of a neural network, are stored in the Flash memory. The small amount of storage available (<64–128 KB) imposes a significant constraint on model design.

Our methodology uses quantisation to reduce the storage requirement of a network. Due to its widespread support, we employ affine quantisation (Jacob et al., 2018), which reduces the per-parameter memory requirement to 8-bits; however, other types of quantisation can be used instead. Therefore, the model size objective is the sum of all weight tensor sizes at 1 byte per parameter.

Here, quantisation plays a dual role: in addition to reducing the storage usage, it enables execution on the most underpowered microcontrollers, which do not support floating-point computation. Using 8-bits, in particular, is a convenient choice for most compute platforms, as it is a natively supported data type—compared to <8-bit or variable encoding schemes, it does not require any decoding at runtime.

### 3.2 Pruning objectives

To accurately model resource constraints, our method sets the width of each prunable layer individually. As layers have

\(^3\)This under-approximation is only correct for linear model graphs, i.e. graphs that only have a single topological order.
We seek to minimise (or improve upon) the difference between the classification loss of the unpruned and the pruned network on a validation dataset $\mathcal{D}$, while only adjusting elements of the binary mask $\mathbf{M}$:

$$\arg\min_{\mathbf{M}}[\mathcal{L}_{ce}(f^{\mathbf{M}}, \mathcal{D}) - \mathcal{L}_{ce}(f, \mathcal{D})] = \arg\min_{\mathbf{M}}\mathcal{L}_{ce}(f^{\mathbf{M}}, \mathcal{D})$$

where $\mathcal{L}_{ce}$ stands for classification loss (cross-entropy). Thus $\mathcal{P}_{\text{TSK}} = \mathcal{L}_{ce}(f^{\mathbf{M}}, \mathcal{D})$. We approximate $\mathcal{D}$ with a single mini-batch of validation set data.

**Channel importance.** Pruning algorithms typically use a weight salience (aka importance) criterion to determine which weights to keep. Both for sparse (unstructured) and structured pruning, popular choices include magnitude-based (Han et al., 2015), norm-based ($L_1$ or $L_2$) (Lin et al., 2020b), Hessian-based (Theis et al., 2018), batch normalisation (BN)-specific (Liu et al., 2017), or gradient flow-based (Lee et al., 2018; Wang et al., 2020) salience metrics.

Here, we consider modern CNNs, assembled out of ‘Conv-BatchNorm (BN)-ReLU’ blocks or fully connected (FC) layers (and other parameter-free layers). In the former case, we choose salience $s$ to be scaling coefficients $\gamma$ within batch normalisation, and in the latter case, the $L_2$ norm of weights of a neuron. More specifically, the importance of a particular channel/neuron $i$ is $s_i$, given by:

$$\text{Conv-BN-ReLU}(x) = \text{ReLU}[\gamma \text{Norm}(K \ast x) + \beta]$$

$$s_i = ||W_i||_2$$

where $x$ is the input tensor, $K$ and $W$ are weight matrices, $\ast$ is a convolution operation and “Norm” is a mean-zero variance-one normalisation function, $b$ and $\beta$ are biases.

**Pruning by salience.** Suppose that within a layer with $C$ output channels (or units/neurons), a proportion $\pi_i$ is set to be kept and not pruned. To perform pruning, all channels are ranked according to their salience ($s$) and top $\pi_i, (\pi_i^{th} \text{ quantile})$ are kept (entries in $\mathbf{M}$ are set to 1) and bottom $1 - \pi_i$ are discarded ($\mathbf{M}$ set to 0).

For a given layer, this makes $M$ a hard threshold function of channel salience $s_i$, with the salience threshold $s_0$ picked to satisfy the constraint that only $\pi_i$ proportion of channels have salience $s > s_0$.

**Differentiable pruning.** To calculate gradient updates to $\pi_i$, we use a continuous relaxation of this hard threshold function on the backwards pass only. Following DSA (Ning et al., 2020), we use a sigmoid function in the log-domain of saliences, which is differentiable w.r.t. $s_0$:

$$M(s_i, s_0) = \frac{1}{1 + e^{-\ln s_i - \ln s_0}} = \frac{1}{1 + s_0/s_i} \quad (3)$$

For differentiable pruning, we are interested in designing a suitable loss $P$, such that we can compute $\frac{\partial P}{\partial \pi}$ and adjust all layerwise $\pi_i$’s using gradient descent. We will use a linear combination of (a) a resource constraint loss $P_{\text{RES}}$, which models the extent to which resource budget is violated, thereby treating budget constraints as extra objectives (as opposed to equality constraints); (b) a task loss $P_{\text{TSK}}$ which encourages maintaining a low classification loss:

$$P = P_{\text{RES}} + \alpha P_{\text{TSK}} \quad (1)$$

Note that $P$ is not a part of a network’s training loss and is not a regulariser directly, since pruning is carried out in parallel to network training as an outer-level optimisation. The hyperparameter $\alpha$ is set depending on the extent of constraint violation and is constant throughout training.

The three aforementioned resource usage objectives can be expressed in terms of and differentiated with respect to the layerwise multipliers $\pi$. We collapse all objectives into one through the use of random scalarisations (Paria et al., 2020) to randomly prioritise different objectives at each update iteration ($i$) while maintaining a bias towards constraints that are violated to a greater extent. Coefficients $\lambda^i = (\lambda^i_1, \lambda^i_2, \lambda^i_3)$ are sampled randomly $\lambda_i \sim \frac{1}{\text{Uniform}(0,1)}$:

$$P_{\text{RES}}^i(\pi) = \max\left\{ \lambda^i_1 \text{PEAKMEMUSAGE}(\pi)/b_1, \lambda^i_2 \text{MODEL SIZE}(\pi)/b_2, \lambda^i_3 \text{MACS}(\pi)/b_3 \right\} - 1 \quad (2)$$

where $b_i$ is a user-specified budget constraint (upper bound) for a particular resource. If randomness is undesirable, the budget-scaled objectives may also be combined via an unweighted sum. For implementation purposes, coefficients $\lambda^i$ are only used to choose the objective within “max” and do not scale the gradients, and $P_{\text{RES}}$ is clipped to be $> 0$.

### 3.3 Pruning algorithm

The pruning of a neural network’s weights is simulated by applying channel-wise binary masks $\mathbf{M}$ to each layers’ output. This effectively sets specific output channels of a layer to all 0, allowing both the weights that compute and consume the masked out channels to be safely removed from the network. We denote an unpruned neural network as $f$ and its pruned counterpart as $f^{\mathbf{M}}$.

We seek to minimise (or improve upon) the difference between the classification loss of the unpruned and the pruned network on a validation dataset $\mathcal{D}$, while only adjusting elements of the binary mask $\mathbf{M}$:

$$\arg\min_{\mathbf{M}}[\mathcal{L}_{ce}(f^{\mathbf{M}}, \mathcal{D}) - \mathcal{L}_{ce}(f, \mathcal{D})] = \arg\min_{\mathbf{M}}\mathcal{L}_{ce}(f^{\mathbf{M}}, \mathcal{D})$$
and enforce a constraint that the proportion of kept channels should equal to the desired channel width multiplier $\pi_i$:

$$\frac{1}{C} \sum_j M(s_j, s_0) = \pi_i$$  \hspace{1cm} (4)$$

Differentiating Eqn. 4 w.r.t. $\pi_i$ and rearranging gives:

$$\frac{1}{C} \sum_j \frac{\partial M(s_j, s_0)}{\partial s_0} \frac{\partial s_0}{\partial \pi_i} = 1$$  \hspace{1cm} (5)$$

$$\frac{\partial s_0}{\partial \pi_i} = \frac{1}{\frac{1}{C} \sum_j \frac{\partial M(s_j, s_0)}{\partial s_0}}$$  \hspace{1cm} (6)$$

This allows to connect task loss gradients with respect to the mask $M$ back to each $\pi_i$:

$$\frac{\partial P_{TSK}}{\partial \pi_i} = \left[ \frac{\sum_j \frac{\partial P_{TSK}}{\partial M(s_j, s_0)} \frac{\partial M(s_j, s_0)}{\partial s_0}}{\sum_j \frac{\partial M(s_j, s_0)}{\partial s_0}} \right] \frac{\partial s_0}{\partial \pi_i}$$  \hspace{1cm} (7)$$

Focus regime for bottleneck objectives. One out of three resource usage objectives we consider is a bottleneck objective: only a few layers (the bottleneck) contribute to peak memory usage at a time. This is in contrast to model size and MACs, to which all layers contribute to a certain extent.

As per Eqn. 1, gradients from both $P_{TSK}$ and $P_{RES}$ are combined to update $\pi$, which may needlessly shrink layers that are not in the bottleneck when other resource constraints are already satisfied. To prevent this, we only update $\pi_i$s for bottleneck layers, i.e. layers for which $\frac{\partial P_{RES}}{\partial \pi_i} > 0$.

![Figure 3. Three examples of pruning over Add, such as residual connections. All summands share the same pruning mask.](image-url)

Pruning residual connections. To correctly preserve the addition of pruned feature maps, their surviving (unpruned) channels must have matching positions, i.e. their pruning masks have to be equal (van Amersfoort et al., 2020). It is also possible to work around this requirement with padding and channel rearrangement, albeit at extra implementation overhead (Lemaire et al., 2019).

We opt to use mask matching: Figure 3 shows examples of tying pruning masks in practice, including residual connections (He et al., 2016). Groups of layers that share the pruning mask are pre-computed in advance using connected components search; the shared $\bar{s}$ is the element-wise maximum of saliences of a group’s layers.

### 3.4 Implementation

Network pruning is interleaved with iterations of model training, which allows us to achieve model compression with little to no overhead and no subsequent fine-tuning.

Layer masks and layerwise multipliers $\vec{\pi}$ are updated using functions in Algorithm 1 every 20 training steps: $\vec{\pi}$ is updated using SGD with learning rate $\eta_{\pi}$ within WIDTH UPDATE, followed by recalculating masks using MASK (without computing $\frac{\partial M}{\partial s_0}$). To enforce $\pi_i \in (0, 1)$ and maintain an S-shaped “sparsity” schedule (Lin et al., 2020b), $\vec{\pi}$ is stored as an unconstrained real variable vector internally with a “sigmoid” function applied to it. The pruning losses effectively act as an $L_1$ regulariser/sparsifier for $\vec{\pi}$, which is not beneficial in our case. We mimic $L_2$ regularisation instead, via a smoothing step $\frac{\partial P}{\partial \vec{\pi}} \leftarrow 2\pi \frac{\partial P}{\partial \vec{\pi}}$.

**Algorithm 1** A high-level implementation of the update procedure for width multipliers $\pi$, $P_{RES}$, $P_{TSK}$, $D$, $s$, $s_0$ as defined in Sections 3.2 & 3.3. DIFF($f$, $x$) computes $\frac{\partial f}{\partial x}$.

```
function MASK(L, $\pi_i$)
    $\bar{s} \leftarrow$ SALIENCE(L.weights)  \hspace{1cm} ▶ as per Section 3.3
    $s_0 \leftarrow$ PERCENTILE($\bar{s}$, $\pi_i$)  \hspace{1cm} ▶ $\pi_i$th percentile of $\bar{s}$
    $\vec{M} \leftarrow (\bar{s} > s_0)$
    $\frac{\partial M}{\partial s_0} \leftarrow$ DIFF($\bar{M}$, $\bar{s}$, $s_0$)  \hspace{1cm} ▶ Eqn. 3
end function

function WIDTH UPDATE($f$, $\vec{\pi}$, $D$)
    $\vec{M}, \frac{\partial M}{\partial s_0} \leftarrow$ [MASK(Layer$_i$, $\pi_i$) for Layer$_i$ $\in$ $f$]
    $\frac{\partial P_{TSK}}{\partial \vec{\pi}} \leftarrow$ DIFF($\partial P_{TSK}(\vec{M}, D)$, $\vec{M}$)
    $\frac{\partial P_{RES}}{\partial \vec{\pi}} \leftarrow$ use Eqn. 7 with $\frac{\partial P_{RES}}{\partial M_k}$ and $\frac{\partial M}{\partial s_0}$
    $\frac{\partial P_{RES}}{\partial \vec{\pi}} \leftarrow$ DIFF($\vec{P}_{RES}(\vec{\pi})$, $\vec{\pi}$)  \hspace{1cm} ▶ Eqn. 2
    $\frac{\partial P}{\partial \vec{\pi}} \leftarrow \frac{\partial P_{RES}}{\partial \vec{\pi}} + \lambda \frac{\partial P_{TSK}}{\partial \vec{\pi}}$  \hspace{1cm} ▶ Eqn. 1
    $\vec{\pi} \leftarrow \vec{\pi} - \eta_{\pi} \frac{\partial P}{\partial \vec{\pi}}$  \hspace{1cm} ▶ SGD update with learn. rate $\eta_{\pi}$
end function
```

Pruning stops, that is, channel width multipliers are no longer updated, when the user-specified resource usage bounds have been reached; however, channel masks are not frozen until the final quantisation-aware stages of training.
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4 Evaluation

In this section, we:

1. Validate the addition of MCU-specific resource objectives to pruning through ablation studies, showing they are needed for finding MCU-compatible models;
2. Show that a precise peak memory usage computation is essential for correctly allocating the SRAM budget;
3. Show pruning allocates resources better than popular manual uniform scaling on MobileNet-v2;
4. Show that training can be accelerated by terminating pruning early compared to training without pruning;
5. Present improved models for eight architecture and task pairs, compared against prior specialist work.

To evaluate differentiable pruning, we consider Google Speech Commands (Warden, 2018), CIFAR-10 (Krizhevsky, 2009) and Visual Wake Words (VWW) (Chowdhery et al., 2019) (“person” vs object classification on ImageNet) datasets. For the “backbone” models to be pruned, we consider VGG-16 (Simonyan & Zisserman, 2014), ResNet-18 (He et al., 2016), MobileNet-v2 (Sandler et al., 2018), EfficientNet-B0 (Tan & Le, 2019), DS-CNN (Zhang et al., 2017) and RES8/15 (ResNet-like) (Tang & Lin, 2018).

Baseline comparisons. As we established in Section 2, to our best knowledge, there is no directly comparable MCU specialist network pruning method in prior work. Thus, we separately establish the competitiveness of the pruning methodology alone, followed by evaluating MCU-specific aspects. Namely, we: (a) verify that our compressed models have comparable or better resource usage than GPU/mobile-level differentiable budgeted pruning methods DSA (Ning et al., 2020) and AutoCompress (auto filter pruning, Liu et al., 2019) for CIFAR-10; (b) show that our methodology can produce comparable or better models than the closest MCU specialist work, MicroNets (Banbury et al., 2020), for other datasets, and do so faster due to the use of pruning; (c) through ablation studies, show that the MCU specialisation using peak memory usage and other resource objectives is necessary to produce viable MCU-compatible models.

Unless otherwise specified, we have reimplemented baseline models and recalculated their resource usage within our framework to facilitate a fair comparison. VWW inputs are in colour, as we do not find it violates the SRAM constraint. All models use the same training and data augmentation protocols and are quantized, as set out in Section 3.1. We do not use distillation, fine-tuning using the validation set, or other adjustments which may confound the results.

4.1 Ablation studies

Task-only or resource-only pruning. To explore the impact of the two driving objectives within pruning, we prune networks using either only task loss ($P_{\text{RES}} = 0$) or only resource-constraint loss ($P_{\text{TSK}} = 0$). We compare EfficientNet-B0 (Tan & Le, 2019) and MobileNet v2 (Sandler et al., 2018) networks on a Visual Wake Words (50x50) dataset using structured sparsity (the proportion of channels removed) and final classification accuracy.

Pruning with $P_{\text{TSK}}$ relegates our methodology to a class of resource-unaware structured pruning methods. Having curbed the ability to target resource-heavy layers first, we would expect more channels to be pruned away (higher sparsity) until desired resource usage is eventually reached.

Pruning with $P_{\text{RES}}$ results in an iterative layer adjustment in proportion to constraint violation, with no awareness of which layers contribute more to generalisation. As a result, we would expect a lower level of sparsity required to achieve desired resource usage but a lower classification accuracy.

Table 2. Pruning loss ablation study results. Models are targeting the resource usage of the MicroNets VWW-2 baseline. Results show that both losses are required to achieve top accuracy.

| Model for VWW (50x50) | Sparsity | Acc. |
|-----------------------|----------|------|
| EfficientNet-B0 (both) | 53.91% | 72.33% |
| EfficientNet-B0 (only $P_{\text{TSK}}$) | 50.38% | 81.33% |
| MobileNet v2 (only $P_{\text{TSK}}$) | 78.31% | 70.61% |
| MobileNet v2 (only $P_{\text{RES}}$) | 53.80% | 82.70% |

Table 2 confirms the above justification, and we observe that both losses are required to correctly prioritise unimportant and resource-expensive channels for removal.

Usefulness of peak memory usage. One of the essential MCU resource constraints to be addressed, which does not arise on other platforms, is peak memory usage.

To verify the usefulness of using a precise peak memory usage calculation, we perform network pruning in three settings: (a) no peak memory usage objective, leaving only MACs and model size; (b) using an imprecise peak memory usage objective, used by MicroNets (Banbury et al., 2020) and SpArSe (Fedorov et al., 2019); (c) full set of resource objectives, as described in Section 3.1. We expect to see a gap between the precise and the imprecise (under-approximation) measurements of PMU; only pruning with the precise PMU objective should produce a model whose true memory usage lies within a memory budget.

Figure 4 shows the change of PMU measures during pruning. The data shows that: (a) using an under-approximation to PMU would cause pruning to be terminated early, potentially while the true memory usage still exceeds the memory budget; (b) the two PMU measures may diverge as the net-
work’s architecture changes; (c) using PMU as a pruning objective is necessary to ensure that the final memory usage lays within the budget; that is, the peak memory usage requirement is not satisfied via other objectives.

**Comparison to uniform scaling.** To support a variety of applications, many popular CNNs, such as MobileNet-v2 and EfficientNet, are already offered at a range of manually-engineered resource usage (or size) vs. accuracy trade-off points. These are typically defined by uniformly scaling the widths of a model’s layers. Pruning a neural network to different sparsity levels also produces a range of trade-off points. We expect pruning to perform better due to the ability to adjust each layer individually.

To compare pruning and uniform scaling, we consider different scalings of the MobileNet v2 model: ×0.75, ×0.50, ×0.25 as given by the authors. For each uniformly scaled model, we aim to discover a smaller resource usage footprint using pruning while still matching or improving upon the classification accuracy. That is, a more efficient resource budget allocation should be possible with pruning.

Figure 5 shows the accuracy and resource usage of scaled MobileNet v2 and matching models obtained by pruning. The results confirm the hypothesis that pruning can find a more efficient resource budget allocation, reducing the size of the final model by up to 50%.

### Table 3. MCU-sized architectures discovered by differentiable network pruning vs. others. The last column compares a baseline to our pruned model in the group (in light grey). “unk.” denotes data not reported by the authors. “Relative speed” is the estimated speed of a compression method relative to training a full model from scratch, with MACs used as a proxy for training time. ‘INT8’ represents a reimplemented quantised model, ‘FP32’ denotes a full precision model as reported by its authors.

| Backbone | Model | Rel. speed | Acc. (%) | Size    | PMU     | MACs    | Difference |
|----------|-------|------------|----------|---------|---------|---------|------------|
| VWW (50x50) on MobileNet v2 | MobileNet v2 (unpruned) | ×1.00 | 84.93 | 2.32 M | 76.2 KB | 22.58 M | ↑ MAC 8.9× |
|         | MicroNets VWW-2 | ×1.15 | 82.82 | 103 K | 27.9 KB | 3.383 M | ↑ MAC 1.3× |
|         | ours (matching VWW-2) | ×1.00 | 82.70 | 101 K | 25 KB | 2.528 M |            |
|         | ours (early termination) | ×0.30 | 82.30 | 96.4 K | 27.5 KB | 2.467 M |            |
| VWW (50x50) on EfficientNet-B0 | EfficientNet-B0 (unpruned) | ×1.00 | 86.08 | 366 K | 300 KB | 9.468 M | ↑ PMU 11× |
|         | ours (matching VWW-2) | ×1.00 | 81.33 | 97.9 K | 27.8 KB | 2.929 M |            |
| VWW (160x160) on MobileNet v2 | MobileNet v2 (unpruned) | ×1.00 | 90.13 | 2.32 M | 768 KB | 164.8 M | ↑ MAC 3.2× |
|         | MicroNets VWW-1 | ×1.43 | 88.01 | 616 K | 200 KB | 71.58 M | ↑ MAC 1.4× |
|         | ours (matching VWW-1) | ×1.00 | 88.04 | 602 K | 197 KB | 51.44 M |            |
|         | ours (early termination) | ×0.49 | 88.08 | 600 K | 197 KB | 49.87 M |            |
| VWW (160x160) on EfficientNet-B0 | EfficientNet-B0 (unpruned) | ×1.00 | 88.93 | 3.66 M | 768 K | 187.6 M | ↑ Size 5.9× |
|         | ours (matching VWW-1) | ×1.00 | 86.95 | 616 K | 175 KB | 25.51 M |            |
| CIFAR10 on VGG-16 | VGG-16 (unpruned) | ×1.00 | 93.29 | 14.7 M | 131 KB | 313.3 M | ↑ Size 80× |
|         | A/C (from 93.7% acc.) | ×1.00 | 88.78 | 311 K | 4.2 KB | 22.38 M | ↑ Size 1.7× |
|         | ours (matching A/C) | ×1.00 | 89.91 | 184 K | 62.5 KB | 22.16 M |            |
|         | DSA (from 93.5% acc.) | ×1.00 | 90.16 | 184 K | 62.5 KB | 22.16 M |            |
|         | ours (matching DSA) | ×1.00 | 89.17 | 502 K | 43.0 KB | 15.34 M |            |
| CIFAR10 on ResNet-18 | ResNet-18 (unpruned) | ×1.00 | 94.63 | 11.4 M | 197 KB | 555.9 M | ↑ Size 5.2× |
|         | DSA (from 94.0% acc.) | ×1.00 | 93.10 | unk. | unk. | 97.51 M |            |
|         | ours (matching DSA) | ×1.00 | 94.07 | 2.21 M | 86.0 KB | 97.40 M |            |
|         | ours (MCU-sized) | ×1.00 | 90.86 | 191 K | 76.8 KB | 28.84 M |            |
| KWS on DS-CNN | DS-CNN (MN-L, unpruned) | ×1.00 | 96.42 | 582 K | 170 KB | 74.27 M | ↑ Size 14% |
|         | MicroNets KWS-L | ×1.89 | 96.26 | 512 K | 170 KB | 65.75 M | ↑ Speed 89% |
|         | ours (matching KWS-L) | ×1.00 | 96.52 | 511 K | 167 KB | 65.56 M |            |
|         | DS-CNN (MN-M, unpruned) | ×1.00 | 96.16 | 420 K | 170 KB | 54.61 M | ↑ MAC 3.6× |
|         | MicroNets KWS-M | ×1.29 | 95.30 | 117 K | 86.1 KB | 15.58 M | ↑ Speed 29% |
|         | ours (matching KWS-M) | ×1.00 | 95.85 | 115 K | 78.1 KB | 15.14 M |            |
|         | MicroNets KWS-S | ×1.15 | 95.28 | 63.6 K | 51.7 KB | 8.351 M | ↑ Speed 15% |
|         | ours (matching KWS-S) | ×1.00 | 95.36 | 63.5 K | 47.4 KB | 7.809 M |            |
| KWS on RES-8/15 | RES-15 (unpruned) | ×1.00 | 96.48 | 240 K | 66.1 KB | 116.4 M | ↑ MAC 7.8× |
|         | ours (matching KWS-M) | ×1.00 | 95.42 | 32.4 K | 27.4 KB | 14.96 M |            |
|         | RES-8 (unpruned) | ×1.00 | 93.25 | 112 K | 23.7 KB | 4.162 M | ↑ PMU 73% |
|         | ours (matching KWS-S) | ×1.00 | 92.78 | 63.2 K | 13.7 KB | 2.354 M |            |
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Figure 4. Peak memory usage calculated using precise (solid) and imprecise (dashed) methods during pruning on MobileNet v2 and RES15 (ResNet-like) backbones. The three colours represent different pruning experiments which have different PMU objectives: the imprecise calculation, the precise calculation and no PMU objective. In all cases, the imprecise objective underapproximates the true peak memory usage.

4.2 Early termination

We can control at which stages of network training the layer sizes $\pi$ are learned by adjusting the epoch at which the learning starts and the learning rate. Once the architecture satisfies the resource constraints, the learning stops, however, the pruning masks $M$ can continue to change. That is, previously pruned channels can be re-enabled if their importance becomes greater than the pruning threshold $s_0$.

The ability to continue updating pruning masks is a feature of dynamic pruning algorithms and has been shown to be beneficial for maintaining the classification accuracy (Lin et al., 2020b). This continuing change is akin to structured Dropout (Dropout probability proportional to inverse salience) or noise injection, which may both improve or hinder performance, making it difficult to make a definitive judgement for all cases. In our initial experiments, we observed that the differentiable pruning yields the best results when applied early in the training (from the first epoch) for a limited number of epochs (most $\pi$ converge within 10–20 epochs). The majority of mask $M$ change occurs as soon as $\pi$ are learned (or soon after). This can be exploited by switching to training the pruned model once the masks are deemed to have sufficiently converged, in order to save computational resources and make training faster.

Figure 5 shows that freezing pruning masks as soon as learning of layer sizes has completed yields similar results to full pruning for larger models, and a worse accuracy vs. size trade-off for smaller models.

4.3 Discovered models

Models obtained via differentiable pruning are presented in Table 3. For each dataset and architecture (backbone) combination, we present an estimated compression speed, accuracy and resource usage of the unpruned full model, a baseline compressed model from prior work and our pruned model. All compressed models have a matching accuracy loss ($\pm 1\%$); we see that differentiable pruning is able to improve upon the resource usage or the speed of compression compared to baseline methods, esp. with early termination.

5 DISCUSSION

Channel size learning dynamics. To investigate how pruning affects the training of the network, we plot the progression of the training loss and the percentage of channels/units that have changed their mask value since the previous update in Figure 7. The pruning is shown in two modes: starting at the 1st epoch (early) and 11th epoch (late).

We observe that: (a) For the same learning rate $\eta_\pi$, early pruning is quicker to achieve the desired research usage. This is due to $\mathcal{P}_{TSS}$ being a cross-entropy loss which produces higher magnitude gradients at the start of training. (b) In both cases, pruning eventually removes channels that
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Contribution to generalisation, resulting in a spike in training loss. Early pruning, however, has more epochs to recover. (c) Early pruning has relatively unstable pruning masks, until late in the training process. This is due to less knowledge of which layers are more important at the start of training (significance values are closer to uniform).

From the above, we can conclude that (a) early pruning is the preferred mode, and (b) in that mode, results of early termination may vary due to a sizeable fraction of mask change happening after the layer size learning has stopped.

Model compression for Visual Wake Words. Figure 6 plots the Pareto trade-off between accuracy and resource usage, namely accuracy vs latency (MACs) and accuracy vs peak memory usage. The data reveals that: (a) better classification can be achieved by increasing the input resolution, although, predictably, this increases resource usage to process more pixels; (b) differences in performance between different models are more pronounced than differences between pruning methods on the same backbone model, as also observed by Blalock et al. (2020).

Broader applicability. Differentiable pruning is a worthwhile addition the model compression toolkit for MCU application developers. While it can produce models with comparable or improved resource usage to the current state-of-the-art, we believe the core strengths lie in its speed and specialisation to the resource usage of the neural network execution runtime. This allows practitioners to introduce differentiable pruning to their model development pipeline with little to no overhead, and request models just by specifying available computational resources.

Despite having been designed for microcontrollers, we believe this methodology has applications to other target platforms, such as SRAM-only inference on custom accelerators or neural processing units (NPUs), or L1-/L2-cache-only inference on CPUs. The resource-awareness also allows pruning to be used within resource-constrained neural architecture search algorithms for MCUs (Liberis et al., 2021): the search for layer sizes can be separated from the search for layer connectivity with the former delegated to pruning.

6 Conclusion

Differentiable network pruning enables on-device deep learning inference on extremely resource-constrained platforms, such as IoT devices. Through microcontroller specialisation and accurate resource budgeting within pruning, our methodology achieves high model compression rates and improves upon the model resource usage or compression speed, compared to prior work.
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