Gd$_2$O$_3$ High-K gate dielectrics deposited by magnetron sputtering

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Gd$_2$O$_3$ High-K Gate Dielectrics Deposited by Magnetron Sputtering

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Abstract: Gd$_2$O$_3$ thin films as high-K gate dielectrics were deposited on Si substrates by magnetron sputtering at 550 °C and 13 Pa. X-ray diffraction and cross sectional high-resolution transmission electron microscopy studies revealed that the Gd$_2$O$_3$ film was crystalline and it was consisted of a mixture of cubic and monoclinic phases. And the film show preferential orientation growth: (111)$_{cubic}$//(001)$_{Si}$ and (401)$_{monoclinic}$//(001)$_{Si}$. The Gd$_2$O$_3$ thin film presented acceptable electrical properties such as low leakage current density of $3.6 \times 10^{-5}$ A/cm$^2$ at +1 V with capacitance equivalent SiO$_2$ thickness of 2.54 nm. Rapid thermal annealing in N$_2$ atmosphere can passivate a large amount of oxygen vacancy and improve the electrical properties.

Key words: Gd$_2$O$_3$ thin film; high-K gate dielectric; magnetron sputtering

1. Introduction

Aggressive scaling of device dimensions in the silicon based complementary metal-oxide-semiconductor (CMOS) technology demands the replacement of conventional silicon dioxide (SiO$_2$) gate dielectric by a higher permittivity (high-K) material [1, 2]. In recent years, rare earth oxides have formed an interesting group as high-K candidates based on their thermodynamic stability with Si and high conduction band offset over 2 eV.

Among the rare earth oxides, gadolinium oxide (Gd$_2$O$_3$) has attractive features for high-K applications. It exhibits a suitable permittivity, a wide band gap ($E_g = 5.4$ eV) and high band offsets with respect to Si ($\Delta E_C = 3.2$ eV, $\Delta E_V = 3.9$ eV) [3]. Thus, Gd$_2$O$_3$ has been widely investigated and showed promising results [4-10]. It is interesting to note that crystalline Gd$_2$O$_3$ thin films are usually formed with cubic structure. This observation may be understood on the basis that cubic phase is stable at room temperature while monoclinic phase is stable at higher temperature over 1200 °C [11]. However, A. Fissel et al. deposited Gd$_2$O$_3$ thin films on 6H-SiC(0001) substrates at 670 °C by MBE technique and observed the formation of Gd$_2$O$_3$ thin films in a mixture of [111]-oriented cubic bixbyite and monoclinic structure [12]. According to our literature survey, such orientation textures in Gd$_2$O$_3$/Si system by magnetron sputtering are truly seldom observed.

In present work, Gd$_2$O$_3$ thin films were deposited directly on Si(001) substrates by magnetron sputtering at 550 °C and a structure similar to reference [12] was observed. Pt/Gd$_2$O$_3$/Si MOS capacitors were fabricated and measured. The structure of Gd$_2$O$_3$ thin films was studied using X-ray
diffraction (XRD) and transmission electron microscopy (TEM). The electrical properties of Pt/Gd₂O₃/Si MOS capacitors were investigated by basic MOS electrical characterization.

2. Experimental
The Gd₂O₃ ceramic target with a purity of 99.95% was obtained by conventional sintering method. The Si substrate with a resistivity of 2-5 Ω·cm is n-type and (001)-oriented. After standard RCA (Radio Corporation of America) cleaning and a buffered HF strip for 60 seconds to remove the native surface oxide, the Si substrates were immediately moved into the vacuum chamber and heated in situ to 550 °C to acquire a clean Si surface. Then Gd₂O₃ thin films (~15 nm) were deposited by radio frequency (rf) magnetron sputtering at a low pressure of 13 Pa in Ar ambient with target-substrate distance of 50 mm and sputtering power of 30 W. After deposition, the films were cooled down to room temperature. Subsequent postdeposition annealing (PDA) process was carried out at 600 °C for 30 seconds in N₂ (or O₂) atmosphere by rapid thermal annealing (RTA). For electrical measurements, circular platinum (Pt) dots of 300 μm in diameter as electrodes were deposited on the surfaces of Gd₂O₃ thin films through a shadow mask.

The Gd₂O₃ film thickness was determined by ellipsometry. The crystal structure was characterized by XRD and cross sectional high-resolution transmission electron microscopy (HRTEM). For electrical measurement of the Pt/Gd₂O₃/Si MOS capacitors, I-V and C-V curves were taken by Keithley 2400 source meter and Agilent 4284A LCR analyzer respectively in a probe station. The two probes were placed on the top of Pt electrode and the back of Si substrate respectively for both I-V and C-V measurements.

3. Results
Fig.1 shows a typical XRD (θ-2θ scan) pattern of a Gd₂O₃ thin film grown on Si(001). Besides the Si diffraction peaks, there were four broad peaks indicating that the Gd₂O₃ thin film was crystalline. The polycrystalline Gd₂O₃ film was composed of two phases as indicated by the marks of C for cubic phase and M for monoclinic phase. Diffraction peaks were identified according to PDF card 88-2165 and 43-1015. The peak around 28° corresponded to C(222), and the ones around 59°, 30°, 62° corresponding to C(444), M(401), M(802) respectively. And we noted that the intensities of cubic peak and monoclinic peak were comparable.

![XRD pattern of the 15 nm Gd₂O₃ film grown on Si(001) by magnetron sputtering. C and M denote cubic and monoclinic, respectively.](image-url)
Another structural feature is that the film showed preferential orientation growth since the C(222), C(444), M(401) and M(802) were the only diffraction peaks, other peaks were not evident or relatively too weak. This suggested the following growth orientation relationships: (111)\textsubscript{C}//(001)\textsubscript{Si} and (401)\textsubscript{M}//(001)\textsubscript{Si}. Similar relationships have also been found in the Gd\textsubscript{2}O\textsubscript{3} films grown on 6H-SiC(0001) substrates by MBE. It is believed that the C(111) plane with the highest atomic density is usually the surface plane for some other oxide films, because such an oriented growth could minimize the total surface energy.

The interface and structure of the Gd\textsubscript{2}O\textsubscript{3}/Si heterostructure was further investigated by cross sectional TEM. The TEM images of Gd\textsubscript{2}O\textsubscript{3}/Si are shown in Fig.2 and 3. Fig.2 is a low resolution TEM image showing that the as-grown Gd\textsubscript{2}O\textsubscript{3} film is 15 nm thick. HRTEM image of the Gd\textsubscript{2}O\textsubscript{3} film (Fig.3) indicated that an amorphous oxide layer between Gd\textsubscript{2}O\textsubscript{3} and Si. The image clearly shows that both cubic and monoclinic phases existed in the film and they are well oriented.

![Fig.2](image1.png)  
**Fig.2** Cross-sectional TEM image of the Gd\textsubscript{2}O\textsubscript{3} thin film grown on Si(001). The bar scale corresponds to 20 nm.

![Fig.3](image2.png)  
**Fig.3** Cross-sectional HRTEM image of the Gd\textsubscript{2}O\textsubscript{3} thin film grown on Si(001). The bar scale corresponds to 5 nm.
The electrical properties of Gd$_2$O$_3$ films as gate bias were also investigated. The dependence of leakage current density ($J_L$) on bias for Gd$_2$O$_3$ thin films is shown in Fig. 4. It was noted that the as grown film showed a relatively low $J_L$ of about $10^{-6}$ A/cm$^2$ at zero bias and $3.6 \times 10^{-5}$ A/cm$^2$ at +1 V. The breakdown field was 3.5 MV/cm. The $J_L$ result was acceptable in the bias range below 5 V in microelectronic industry. After PDA process, the leakage current density of Gd$_2$O$_3$ film decreased for RTA in N$_2$ but increased for RTA in O$_2$. This indicated that nitrogen incorporation can passivate a large amount of oxygen vacancy and improve the electrical properties. The asymmetry noted in $J_L$-V data is possibly due to the effects of air exposure before the electrode was deposited and interacted with the electrode interface [4, 5].

![Fig.4 $I-V$ characteristic of the 15 nm Gd$_2$O$_3$ films including the one as grown (○), the one after N$_2$ RTA at 600 °C for 30 s (△) and the one after O$_2$ RTA at 600 °C for 30 s (□). The positive bias means that the top Pt electrode was positive with respect to the Si substrate.](image)

The dependence of capacitance on bias at a frequency of 500 kHz for Pt/Gd$_2$O$_3$/Si MOS capacitors is shown in Fig. 5. The transition from accumulation to depletion was evident for the MOS capacitor with as grown Gd$_2$O$_3$ film. And the C-V curve didn’t present a noticeable shift relative to the ideal one. The capacitance equivalent SiO$_2$ thickness (CET) estimated directly from the accumulated capacitance was 2.54 nm and the effective permittivity of the overall capacitor was 23. However, the accumulation was not saturated implying that a large amount of oxygen vacancy existed in the film. After PDA process in N$_2$, the accumulation became saturated and the effective permittivity of the overall capacitor became 16. However, the C-V curve for the Gd$_2$O$_3$ film after PDA process in O$_2$ presented a shift of about +1 V implying a large amount of negative fixed charge existed in the film [1]. This is consistent with the results of $I$-$V$ curves.
Fig. 5 High frequency (500 kHz) C-V characteristic of the Pt/Gd$_2$O$_3$/Si MOS capacitors with Gd$_2$O$_3$ film as grown (○), after N$_2$ RTA at 600 °C for 30 s (△) and after O$_2$ RTA at 600 °C for 30 s (□). The area of top Pt electrodes was 7.1×10$^{-4}$ cm$^2$.

4. Summary

In summary, both cubic and monoclinic phases co-existed in Gd$_2$O$_3$ thin film grown by magnetron sputtering at 550 °C. These two phases presented preferential orientation growth with regard to Si(001) substrate. The Gd$_2$O$_3$ thin film presented acceptable electrical results and RTA treatment in N$_2$ atmosphere can passivate a large amount of oxygen vacancy and improve the electrical properties. Considering the commercial application, the low-cost Gd$_2$O$_3$ thin film grown by magnetron sputtering could be a promising candidate as high-K gate dielectric in CMOS devices. Further work is in process to improve the electrical properties of the Gd$_2$O$_3$ thin films.

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