Accelerating Implicit Finite Difference Schemes Using a Hardware Optimized Tridiagonal Solver for FPGAs

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Abstract—We present the design and implementation of the Thomas algorithm optimized for hardware acceleration on an FPGA. The hardware based algorithm combined with the custom data flow and low level parallelism available in an FPGA reduces the overall complexity from 8N down to 5N serial arithmetic operations and almost halves the overall latency by parallelizing the two costly divisions. Combining this with a data streaming interface, we reduce memory overheads to only 2 N-length vectors per N-tridiagonal system to be solved. The Thomas Core developed allows for multiple independent tridiagonal systems to be continuously solved in parallel, providing an efficient accelerator for many computations. Finally we present applications for derivatives pricing problems using implicit finite difference schemes on an FPGA accelerated system and investigate the use and limitations of fixed-point arithmetic in our algorithm.

I. INTRODUCTION

A. FPGAs

Field programmable gate arrays (FPGAs) provide an integrated circuit that can be reconfigured on the fly or ‘in the field’ in the form of a chip. FPGAs provides a flexible and cost effective way to develop and implement custom hardware designs. The core component that allows an FPGA to be reconfigurable is a look-up table (LUT). A LUT produces an output/outputs as a function on the digital inputs, these functions are determined when the FPGA is configured and provides the desired logic by the inputs controlled via the programmable cells. The other key component that helps to increase the performance of FPGAs are on-chip block memory (BRAM) which can provide fast local memory caches. Some FPGA chips may also offer other additional features such as high speed digital signal processors (DSP) and multipliers. The FPGA chip is then usually placed on a circuit board and connected to additional peripherals such as DDR memory, USB ports, ethernet, PCI express and VGA ports to provide the complete heterogeneous computing system.

B. Finite Difference Schemes and Tridiagonal Systems

Finite difference schemes begin by discretising the problem domain into a mesh/grid over the time interval [0, 1] and in basic cases, the asset price interval [0, S_max]. The domain is discretised into N asset price steps and M time steps, given by:

\[ \Delta S = \frac{S_{\text{max}}}{N} \]  
\[
\Delta t = \frac{1}{M}
\]

The spatial derivative terms are approximated using central difference and backward difference for the time derivative. These discretizations are then substituted into the PDE to produce the discrete difference equation, for example the BSE equation gives:

\[ V_n^m = a_n V_{n-1}^{m-1} + b_n V_n^{m-1} + c_n V_{n+1}^{m-1} \]  

with problem dependant stencil coefficient values \( a_n, b_n, c_n \). This is the basic implicit scheme used for one dimensional problems, the resultant system of equations can be written in matrix form and needs to be solved for the price vector at the current time-step, \( V^{t-1} \), where the vector \( V^t \) is known from the previous implicit step.

\[ AV^{t-1} = V^t \]

or more generally written as the matrix inversion problem \( Ax = y \), where the coefficient matrix \( A \) takes on the banded tridiagonal form shown below:

\[
A = \begin{bmatrix}
    b_0 & c_0 & 0 & 0 & 0 & \ldots \\
    a_1 & b_1 & c_1 & 0 & 0 & \ldots \\
    0 & a_2 & b_2 & c_2 & 0 & \ldots \\
    0 & 0 & a_3 & b_3 & c_3 & 0 & \ldots \\
    \vdots & \ddots & \ddots & \ddots & \ddots & \ddots & \ddots \\
    0 & \ldots & 0 & a_N & b_N & \end{bmatrix}
\]
or under stochastic volatility, another class of finite difference schemes known as alternating-direction-implicit schemes [2] may be used. These schemes solve the PDE in an implicit manner within multiple dimensions. These methods can be computational challenging as they require the solution to multiple tridiagonal systems at each time step, thus a lot of effort has gone into creating fast parallel solvers on devices such as GPUs [3] [4].

C. Thomas Algorithm

Algorithm 1 Thomas Algorithm (a,b,c,y) Pseudo Code

```
d[0] = b[0]
z[0] = y[0]
for i = 1 to N do
  prev = i - 1
  l_i = a[i]/d[prev]
  d[i] = b[i] - l_i*c[prev]
  z[i] = y[i] - l_i*z[prev]
end for
z[N] = z[N]/d[N]
for i = N-1 to 0 do
  x[i] = (z[i] - c[i]*x[i+1])/d[i]
end for
return x[i]
```

The Thomas algorithm [5] is the simplest method used to solve a tridiagonal system of equations and is commonly employed on serial devices such as a CPU. The Thomas algorithm is a specialised case of gaussian elimination and can be derived from the LU decomposition of the matrix $A$. This reduces the system down to the solution of two bi-diagonal systems which can then be solved via gaussian elimination. The first system is solved via forward substitution and the second system is solved via backward substitution. These two stages will be referred to as the forwards and backwards iterations. The Thomas algorithm is given in algorithm 1, it has a complexity of $O(N)$ and requires a total of $8N$ arithmetic operations to solve an $N$-tridiagonal system.

In parallel computing the Thomas algorithm is usually less favoured than algorithms such as recursive-doubling [6], cyclic-reduction [7] and parallel cyclic-reduction [8], since although these algorithms have a larger number of arithmetic operations some of the operations can be parallelised on devices such as GPUs [9] resulting in an overall lower algorithmic complexity. With a recent increased interest in FPGA acceleration attempts have been made to port tridiagonal solvers onto FPGAs [10][11][12][13]; in this application the simplicity of the Thomas algorithm makes it well suited to the task when compared to cyclic-reduction which maybe too complex for efficient data flow FPGA implementation.

II. ALGORITHMIC OPTIMIZATION AND LOW LEVEL PARALLELIZATION

Figures 1 and 2 depict the data dependency of the Thomas algorithm; it can be observed that in the forward iteration there are two separate branches of computation, one for calculating $d_n$ and the other for $z_n$ and hence this provides the first level of parallelism extracted. A similar approach has been taken by both Oliveira et al [10] and Warne et al [11]. This optimisation reduces the effective serial arithmetic operations down from $8N$ to $6N$.

The problem with this simple optimisation is that although there is a reduction in serial operations, it has only reduced a multiply and a subtract which are computational cheap when compared to divisions. Consequently a competitive speed-up over faster clocking devices such as CPUs may not be obtained [11]. We thus introduce a simple algorithmic rearrangement that can allow for the two divisions from the backwards and forward iterations to be effectively parallelised. Equation 6 shows the factorisation of the backwards iteration calculation where we now treat the divisions of $z_n$ and $c_n$ by $d_n$ individually.

$$\frac{z_n - c_n V_{n+1}}{d_n} = \frac{1}{d_n} z_n - \left(\frac{1}{d_n} c_n\right) V_{n+1}$$  \hspace{1cm} (6)$$

In a serial implementation this would add an extra division to the total number of arithmetic operations, which is not usually desirable, but as shown in figure 3 the data dependence is in fact here reduced, we can now treat these two divisions in
parallel with each other whilst also performing them in parallel with the forward iteration calculations. This reduces the serial arithmetic operations down from the original 8N to 5N.

For FPGA implementations this rearranged algorithm has two advantages:

1) Total latency of the algorithm is almost halved by parallelising the two lengthy divisions.
2) Memory requirements are reduced from the need to save three intermediate data vectors \((c, z\) and \(d\)) to two \((c/d\) and \(z/d\)).

A. Pipelining

Further to the low level algorithmic optimisations higher level parallelism can be achieved in two ways: pipelining the data through the computation of the forward and backward iterations; and pipelining the sets of data between the forward and backward iterations, which has commonly been implemented for multiple CPU versions to parallelise the Thomas algorithm [14].

Firstly the computational units themselves can be deeply pipelined, an approach used by Olivera et al. [10], which allows for multiple independent tridiagonal systems to be computed in the same iteration cycle. For example, if the forward iteration computational unit has \(P_F\) pipeline stages then throughout one iteration it is possible to fill each stage of the pipeline with a computation allowing for \(P_F\) independent tridiagonal systems to be computed.

The second type of pipelining of the algorithm means that given a set \(T\) of pipelined tridiagonal systems for either iteration, as discussed above, we can simultaneously compute the forward and backwards iterations of the two different sets (given the first set has already been through the forward iterations) independently in one Thomas solver. In [12] they look at using OpenCL and Xilinx HLS to build the Thomas solvers, but do not obtain this level of parallelism due to the complex scheduling involved for the pipelines. As such this design has been made in VHDL allowing this desired low level control to be obtained.

B. Hardware Architecture

The input to the solver core consists of 5 data items \(a,b,y\) and \(id\) where \(id\) is the local id of the system to be solved, this acts as a thread id and is important for addressing the correct memory stacks in the solver. The hardware architecture consists of four main components, the forward iteration core, the d-divider, the backwards iteration core and the stack array.

The forward and backward cores contain the pipelined arithmetic for the stages of the algorithm, and the d-divider consists of two dividers to carry out the \(c/d\) and \(z/d\) computations.

Connecting the forward iterations to the backwards iterations is a queue. This queue allows the problem index to be passed onto the backwards core for computation once the forward iterations have finished, this system allows for efficient independent operation of the forwards and backward iterations. The backwards core checks for space in the pipeline, and reads in the problem to begin computing if there is space, otherwise it remains queued.

In addition to the main Thomas algorithm core, the core has been placed in a wrapper allowing for easy usability. The wrapper consists of fifo queues for the input data and output results, allowing for variable read and time to and from the core, as well as the option for floating-point to fixed-point converters for input data and vice-versa for results.

When changing the arithmetic only the arithmetic cores are changed, and the architecture remains constant. The only variability with the arithmetic cores is the pipelining due to the differing latencies, but this is managed via adjustable parameters within the solver VHDL.

III. Design Analysis

Here we theoretically analyse the performance of the solver for solving multiple independent tridiagonal systems \(T = \{T_1^{N_1}, T_2^{N_2},...,T_M^{N_M}\}\), where \(M\) is the total number of independent tridiagonal systems to be solved and \(N_m\) is the size of the \(m\)th system. The notation is used in this work as follows:

- \(T_m^{N_m}\) is the size of the \(m\)th tridiagonal system to be solved of size \(N_m\).
- \(T^N\) is a special case where for all \(T_m \in T\), \(N_m = N\).
- \(C_D^{\{+,-,\div,\times\}}\) is the number of clock cycles taken for that arithmetic operation using data format \(D\).

![Data dependency graph for the proposed Thomas algorithm structure optimised for FPGA implementation.](image)
is the number of clock cycles taken for a single forwards, \( F \), and backwards, \( B \), iteration and administration costs \( A \).

- \( f \) is the clock frequency of the FPGA system.

The number of cycles taken for the iteration stages are:

\[
C_F = C^D_F + C^D_X + C^D
\]

\[
C_B = C^D + C^D_x + C^D
\]

with \( C_A \) being a constant determined by the programming of the algorithm.

To fully harness the power of the pipelined design it is desired that maximal throughput should be achieved by scheduling groups of independent computations.

**Definition 1.** The number of computational blocks, \( B \), is defined as the number of subsets of independent tridiagonal systems to be solved. The set of of blocks given by \( B = \{ b_1^{m_1}, b_2^{m_2}, \ldots, B_B^{m_b} \} \), where \( b_i^{m_i} \subset T \) of size \( m_i \) such that:

\[
\cup_{i=1}^{B} b_i^{m_i} = T ; \cap_{i=1}^{B} b_i^{m_i} = \emptyset
\]

Thus for a given \( M \) the time to compute \( T^N \) is then given by:

\[
t_{T^N} = \frac{NB(C_F + C_A) + BC_F + NC_F + 2 \sum_{b=1}^{B} (m_b - 1)}{f}
\]

for \( f = 1 \) the partitioning of \( T \) into the set of blocks \( B \) can be effected by the data transfer rate \( r_d \) between the solver and the host system. The rate of computation, \( r_c \), of the Thomas solver is given by:

\[
r_c = \frac{5D}{f}
\]

where \( D \) is the number of bits used to represent a number in the given format. This value is the rate at which data can be processed by the Thomas solver, the solver requires 5 inputs, \( a, b, c, y \) and \( id \) and can process a row every clock cycle.

The optimal number of blocks \( B \) can be obtained if the rate of transfer is quicker than the rate of computation, i.e. the solver can receive all the 5 values in one clock cycle or less:

\[
B_{\text{opt}} = \text{floor}(\frac{M}{C_F}) ; r_d \geq r_c
\]

It maybe the case that the data transfer rate is slower than the rate of computation and hence the solver has to be stalled whilst waiting for the data. It is therefore desirable to compute the maximum number of tridiagonal systems in a block \( b \) in the pipeline without stalling for data. The number of blocks \( B \) is given by:

\[
m_{\text{opt}} = \text{ceil}(\frac{r_c}{r_d}) ; r_d < r_c
\]

\[
B = \text{floor}(\frac{M}{m_{\text{opt}}})
\]

Maximum throughput for the solver can be obtained if the set of tridiagonal systems to be solved completely fills the pipeline of the solver:

\[
M \% C_F = 0
\]

\[
B > 1
\]

**IV. FIXED-POINT ARITHMETIC ANALYSIS**

**A. Numerical Bounds**

To maximise performance it maybe required that custom data formats are used in the FPGA design. Fixed-Point arithmetic often provides faster and smaller FPGA designs, for example [15][16], but at the cost of the loss of some precision in the results and a higher risk arithmetic overflow. Therefore it is important to know the range of values the solver is expected to use in the algorithm to allow for the custom data formats to be optimised for the problem. The preceding theorems presented require additional conditions that \( b(n) \) is a positive monotonically increasing function of the row index, \( n \) i.e. \( b_n < b_{n+1} \) and \( |a_n| < 1 \) and \( |c_n| < 1 \) \( \forall i \leq N \). These theorems will be useful later for range bounding the implicit pricing problem. In these following results the \( L \)-Infinity norm of the set of coefficients \( a, b \) or \( c \), denoted by \( \| x \|_\infty \), is used, the value of this norm is the largest absolute value in a set.

**Theorem 1.** Given \( A \) is diagonally dominant by row or columns, and let \( A \) have LU factorisation \( A = LU \). Then \( \|l\|_\infty \leq 3\|b\|_\infty \)

**Proof:**

Given in the proof of \( |L||U| \leq 3|A| \) found in [17] pg.175 the following result is used:

\[
|l_n c_{n-1}| + |d_n| \leq 3|b_n|
\]

Simple rearrangement and the observation that the max will occur at the maximum absolute value gives the result of theorem 1.

**Theorem 2.** Given \( A \) is diagonal dominant by row, and let \( A \) have LU factorisation \( A = LU \) then \( |d_n| > |b_0| - \frac{\|a\|_\infty \|c\|_\infty}{|b_0|} \) \( \forall n \), given that \( b(n) \) is a positive monotonically increasing function of the row index, \( i \) and \( \Delta b \leq \|c\|_\infty \).

**Proof:**

\[
d_0 = b_0
\]

\[
d_1 = b_1 - \frac{a_1}{b_0} a_0
\]

\[
b_1 - \frac{\|a\|_\infty}{|b_0|} \|c\|_\infty \leq d_1
\]

Under the assumption that \( b(n) \) is a positive monotonically increasing function then

\[
b_0 - \frac{\|a\|_\infty}{|b_0|} \|c\|_\infty \leq b_1 - \frac{\|a\|_\infty}{|b_0|} \|c\|_\infty \leq d_1
\]

finally for this to hold over all cases it must enforced that \( \|l\|_\infty \leq \frac{\|a\|_\infty}{|b_0|} \), which implies that:

\[
b_0 \leq b_1 - \frac{\|a\|_\infty}{|b_0|} \|c\|_\infty
\]
thus for this hold \( \Delta b \leq \|c\|_{\infty} \), given that \( \|a\|_{\infty} < |b_0| \).

A more general theorem for all functions of \( b(n) \) will be investigated, though theorem 2 currently suffices for this work as will be seen later. The approach for finding a more general theorem will look at conditions for when a certain sequence of \( b \) provides a minimum for \( d_0 \) when compared to all other possible permutations.

**Theorem 3.** Given \( A \) is diagonal dominant by row, and let \( A \) have LU factorisation \( A = LU \) then \( \|l\|_{\infty} < \|a\|_{\infty} \), given that \( b(n) \) is a positive monotonically increasing function of the row index, \( n \).

**Proof:** Using theorem 2, the maximum value of \( l \) must be achieved when the largest value of \( a \) is divided by the smallest value of \( d \).

In fact, although theorem 1 provides an upper bound for the value of \( d \), using the previous theorems a tighter more accurate bound can now be defined.

**Theorem 4.** Given \( A \) is diagonal dominant by row, and let \( A \) have LU factorisation \( A = LU \) then \( d \leq \|b\|_{\infty} + \|l\|_{\infty} \|c\|_{\infty} \), given that \( b(n) \) is a monotonically increasing function of the row index, \( n \).

1) Bounding the Thomas Algorithm:

The first section describes various bounds for the LU decomposition of a matrix \( A \). This forms the basis of the well known Thomas Algorithm used for solving tridiagonal inversion problems of the form \( Tx = y \), where \( T \) is a tridiagonal matrix. The first stage of the algorithm is to apply LU decomposition to the matrix and then solve to auxiliary equations using forwards and backwards substitution.

**Theorem 5.** Given a tridiagonal matrix \( T \) is diagonally dominant by row and let \( T \) have LU factorisation \( T = LU \) with \( \|l\|_{\infty} < 1 \), then solving the first auxiliary equation of the inversion problem \( Lz = y \); \( z = Ux \), then \( \|x\|_{\infty} < \|y\|_{\infty}(1 - \|l\|_{\infty})^{-1} \)

**Proof:** First the term for \( z_N \) is expanded and using theorem 3 it is possible to replace the individual \( l_i \) terms with the upper bound \( \|l\|_{\infty} \).

\[
\|x\|_{\infty} \leq |y|_N + \sum_{k=1}^{N-1} \|l\|_{\infty} |y_k| \tag{23}
\]

In fact we can further loosen the bound by assuming that all values are the max, so

\[
\|x\|_{\infty} \leq |y|_N + \sum_{k=1}^{N-1} \|l\|_{\infty} |y_k| \leq \|y\|_{\infty}(1 + \sum_{k=1}^{N-1} \|l\|_{\infty}^k) \tag{24}
\]

using the formulas for the sum of a geometric sequence the max bound becomes

\[
\|x\|_{\infty} \leq \|y\|_{\infty}(1 + \sum_{k=1}^{N-1} \|l\|_{\infty}^k) \leq \|y\|_{\infty} \frac{1}{1 - \|l\|_{\infty}} \tag{25}
\]

and finally in the case that \( \|l\|_{\infty} < 1 \) a simpler form using the infinite geometric sum can be used:

\[
\|x\|_{\infty} \leq \|y\|_{\infty} \frac{1}{1 - \|l\|_{\infty}} \tag{26}
\]

The hardware optimised algorithm presented here requires the calculation of two additional intermediates \( \tilde{x}_d \) and \( \tilde{x}_n \).

**Theorem 6.** Given a tridiagonal matrix \( T \) is diagonally dominant by row and let \( T \) have LU factorisation \( T = LU \) with \( \|l\|_{\infty} < 1 \), and previously stated conditions the intermediate value \( \|\tilde{x}_d\|_{\infty} \leq \|c\|_{\infty} \).

**Theorem 7.** Given a tridiagonal matrix \( T \) is diagonally dominant by row and let \( T \) have LU factorisation \( T = LU \) with \( \|l\|_{\infty} < 1 \) the intermediate value \( \|\tilde{x}_d\|_{\infty} \leq \|\tilde{x}_n\|_{\infty} \).

Finally it is possible to then derive the bounds for the final values.

**Theorem 8.** Given a tridiagonal matrix \( T \) is diagonally dominant by row and let \( T \) have LU factorisation \( T = LU \) with \( \|l\|_{\infty} < 1 \), and previously stated conditions with \( b_n > 1 \) and \( c_n > 1 \forall n \leq N \) then \( \|v\|_{\infty} \leq \|z\|_{\infty} \frac{|N|}{|b_0|} \).

**Proof:**

\[
v_N = \frac{z}{d} \tag{27}
\]

\[
|v_N| < \frac{|z|_{\infty}}{|b_0|} \tag{28}
\]

the recursion begins at \( v_{N-1} \), it is possible to see that

\[
|v_{N-1}| < \frac{|z|_{\infty}}{|b_0|} + V_N \tag{29}
\]

\[
\frac{\|z\|_{\infty} \|c\|_{\infty}}{|b_0|} \leq \frac{|z|_{\infty}}{|b_0|} + \|z\|_{\infty} \|c\|_{\infty} \tag{30}
\]

expanding the recursion in this manner the result for a sequence given by

\[
|v_n| < \sum_{i=0}^{N-n} \frac{|c|_{\infty}}{|b_0|^{i+1}} \tag{31}
\]
then assuming \(|b_0| > 1\) and \(\|c\|_\infty < 1\) the limit of this sequence is given by:

\[
|v_n| < \sum_{i=0}^{N-n} \frac{||c||_\infty^i \|z\|_\infty}{|b_0|^i+1} < \frac{||z||_\infty}{|b_0| - 1} \tag{32}
\]

Combining the previous theorems it is now possible to define a set of conditions that can ensure the absolute value of any variable in the algorithm does not exceed a certain bound. This will prove extremely useful when applying the fixed-point designs to given problems.

**Proposition 1.** For a given integer \(Z\) ; \(0 < Z\) there exists a set of conditions such that all intermediate variables in the Thomas algorithm can be bounded by \(Z\), given that \(b(n)\) is a positive monotonically increasing function of the row index, and \(|a_n| < 1\), \(|c_n| < 1\) and \(|b_n| > 1\) \(\forall n \leq N\). The following conditions are sufficient but not necessary:

1. \(\|l\|_\infty < 1\) this implies \(\|a\|_\infty < |b_0|\)
2. \(\|y\|_\infty < Z \cdot \|b-\|l\|_\infty\)
3. \(\|c\|_\infty < |b_0|\)
4. \(\Delta b \leq \|c\|_\infty\)

V. HARDWARE IMPLEMENTATION

A. FPGA Resource Usage

The Thomas Solver hardware will be tested using the ZedBoard Xilinx Zynq7020 Evaluation Kit. The Zynq7020 is a system-on-chip which consists of two ARM-A9 processors connected to Xilinx Artix-7 FPGA fabric, allowing a high-speed interface between CPU and FPGA. Using the Zynq7020 the system of equations will be formulated in floating-point on the ARM-A9 CPU, these will then be transferred to the FPGA via AXI interfaces and solved using the FPGA Thomas solver. The fixed-point results are then converted back to floating-point and compared to the results for the same problem solved using floating-point arithmetic.

The results in table V-A were obtained post-implementation from the Vivado Design Suite, the base design used has \(N_{max} = 512\) with 10 threads \((M_{max} = 10)\), and variable arithmetic. A floating-point design and three fixed-point solvers with the following data representation, [integer bits, fractional bits], are tested, 32bit[2,30], 24bit[2,22], 16bit[2,14]. For the arithmetic cores the provided Xilinx base IP cores were used, and set to make maximum usage of DSPs, and the Radix-2 divider algorithm is used for as part of the fixed-point divider.

Each of the solver designs have the same magnitude of latency, with the floating-point design providing the lowest total latency, although the fixed-point designs maybe sped up by using higher radix divider algorithms. The disadvantage of the higher radix divider algorithms is that the maximum throughput is reduced due to the iterative nature of the algorithms, but this is useful if it is not possible to achieve maximum throughput of processing on tridiagonal system per clock. The main advantage of the fixed point solvers is the reduced resource usage, which provides the opportunity to maximise coarse grain parallelism by allowing more solver cores to fit onto a device and also increasing the maximum number of pipelined tridiagonal systems each core can solve. As can be expected the amount of memory resources is proportional to the total data width used for the fixed-point designs, whilst the floating-point solver, although 32bits wide, uses significantly more memory resources (BRAM and memory LUTs).

B. Performance

The latency performance of the solver can be evaluated using equation 10 once the implemented FPGA clock speed is known. The floating-point was only able to achieve a maximum clock frequency of 100MHz whilst the fixed-point designs where able to achieve double this at 200MHz. Therefore although the fixed-point designs may have slightly higher latency in terms of clock cycles, the speed of computation is considerably faster due to this higher clock rate.

The average time in milliseconds per tridiagonal system is shown in table V-B for minimum throughput, a single tridiagonal system, and maximum throughput, where the pipeline is completely full. These results are compared to the average time taken for a 2.6GHz on a top of the range desktop machine. If the solver was to be used for single tridiagonal systems the speed is fractionally less than a top of the range 2.6GHz CPU, but this is not taking advantage of the pipelined design. At maximum throughput it is possible to achieve up to a 36x
speed-up and 16x speed-up over a 2.6GHz CPU for FPGA fixed-point and floating-point designs respectively. In terms of cost of computing power the basic $200 FPGA board used here can outperform, in terms of speed, a $1000+ desktop computer, as well as also using considerably less power. This is due to the deep pipelining and custom data paths possible on an FPGA.

VI. IMPLEMENTATION FOR IMPLICIT FINITE DIFFERENCE SCHEMES

Here it is intended to evaluate the accuracy of the fixed-point Thomas solvers within the context of options pricing. When pricing options via implicit finite difference methods it often results in a tridiagonal or many systems of tridiagonal equations to be solved. As an example the solver will be used for solving tridiagonal systems arising in implicit finite difference scheme for European options using the Black-Scholes model.

A. Scaling For Fixed-Point Designs

The motivation is to use fixed-point arithmetic as previously discussed is that it results in smaller and faster designs when compared to floating-point. The tridiagonal coefficients for pricing a European option via implicit finite difference are given by:

\begin{align}
  a_n &= -(n^2 \sigma^2 - nr) dt \\
  b_n &= 1 + (n^2 \sigma^2 + r) dt \\
  c_n &= -(n^2 \sigma^2 + nr) dt \\
  a_N &= N r dt \\
  b_N &= 1 - (N r - r) dt \\
  y_n &= \text{payoff}(S_n)
\end{align}

where \( y \) is defined by the initial boundary condition of the problem, in this case the payoff function of the option.

Observe the coefficients \( b_n > 1 \forall i \leq N \), as such two integer bits will be used for the fixed-point representation and a \( Z = 2 \) to ensure no arithmetic overflow. Using proposition 1 it is possible to show that the coefficients of implicit Black-Scholes pricing can be bounded so that \( Z = 2 \) after applying and basic grid constraint to bound coefficient values and an appropriate transformation for the \( y \) values to meet condition 2 of proposition 1. This is more formally expressed in theorem 9.

**Theorem 9.** Given a Black-Scholes Implicit pricing problem, \( A_f \), it is possible to ensure that the supremum of the algorithm i.e. all values calculated in the algorithm \( \sup(|A_f|) \) \( < Z \), given the following grid constraint and suitable linear transform on the problem domain.

\begin{align}
  dt &< \frac{1}{\sigma^2 N^2} \\
  \hat{y}_n &= f(y_n) \\
  f(y_n) &= y_n Z \left[ \|b_0\| + \|a\| \right] \infty \|y\| \infty
\end{align}

Table VI-B gives the expected rounding error for the number of fractional bits used in the fixed-point design. The expected rounding error \( e_{\text{rnd}}(x, f) \), where \( e_{\text{rnd}} \) is the rounding error and \( f \) is the number of bits, for rounding a floating-point number \( x \) to a fixed-point representation is given by:

\[ E(e_{\text{rnd}}(x, f)) = \frac{2^{f-1}}{2} ; x \in [0, \infty] \]

It has been assumed that the rounding error is uniformly distributed white noise over \( x \in \mathbb{R} \) [18]. If an error obtained is smaller than this value indicates that the fixed-point value was rounded to 0, and the actual value is smaller than is possible to represent in the fixed-point representation. Errors within a similar magnitude as the magnitude of the expected error indicate that the fixed-point result is on average as accurate as is possible for the given fixed-point representation.

Table VI-B shows the absolute error with respect to the floating point result for the fixed-point solver using 30 fractional bits. The most striking feature of this plot is how the error resembles the shape of the payoff function indicating that the magnitude of the option price plays a role in the error function. A worst case error function has been derived from the observation that an option price, \( V \); \( V < S_n \), i.e. the European option price must be at least less than the asset price due the the effect of the strike. The maximum error is then a function of the asset price, minimum expected rounding error and \( n \) to take into account error prorogation factors through the iterations.

\[ E(S_n) = n S_n \frac{2^{f-1}}{2} \]

Table IV

| Fractional Width | Expected Rounding Error | Maximum FPGA Error |
|------------------|-------------------------|--------------------|
| 30               | 2.33E-10                | 4.06E-08           |
| 22               | 5.95E-08                | 4.88E-07           |
| 14               | 1.52E-05                | 1.23E-04           |

B. Fixed-Point Solver Accuracy

The fixed-point solver designs are tested over a sample of 5000 randomly selected tridiagonal equations generated by random option pricing problems. The two market dependant parameters, interest rate \( r \) and volatility \( \sigma \), are randomly chosen for each option sample to generate new sample of tridiagonal equations to solve; \( r = U[0.01, 0.05] \), \( \sigma = U[0.10, 0.30] \). The finite difference grid parameters are selected to meet the constraint in equation 39 in the case of maximum market parameter values, this resulted in \( dt = 0.001 \). Finally to meet the final for \( \| y \| \) a linear transform constant of \( 0.45 Z \| y \| \infty \) was used, calculated using equation 41, to meet this condition the problem was chosen so that \( S_N = 2 \) and \( K = 1 \).

Figure VI-B shows the absolute error with respect to the floating point result for the fixed-point solver using 30 fractional bits. The most striking feature of this plot is how the error resembles the shape of the payoff function indicating that the magnitude of the option price plays a role in the error function. A worst case error function has been derived from the observation that an option price, \( V \); \( V < S_n \), i.e. the European option price must be at least less than the asset price due the the effect of the strike. The maximum error is then a function of the asset price, minimum expected rounding error and \( n \) to take into account error prorogation factors through the iterations.

\[ E(S_n) = n S_n \frac{2^{f-1}}{2} \]
Fig. 4. Average absolute error over 5000 tridiagonal systems of the fixed-point results using 30 fractional bits with respect to floating-point results. -x- estimated maximum error bound using equation 43.

Fig. 5. Average absolute error over 5000 tridiagonal systems of the fixed-point results using 22 fractional bits with respect to floating-point results.

Fig. 6. Average absolute error over 5000 tridiagonal systems of the fixed-point results using 14 fractional bits with respect to floating-point results.

their respective absolute errors with respect to their minimum fractional resolution is a lot better, with the largest magnitude of error being of the same order, this is up to 100 times smaller in magnitude than the error predicted by equation 43.

These results show that the fixed-point arithmetic is accurate up to a given decimal place, which then after the accuracy begins to degrade. This explains why the 30 fractional bit errors were a lot larger than its respective minimum fractional resolution and not so for the 22 and 14 fractional bits.

VII. CONCLUSIONS AND FUTURE RESEARCH

This work has proposed and introduced a prototype design for a high performance FPGA based tridiagonal solver. Fixed-point designs can be used to minimise resource usage and obtain higher clock rates compared to floating point designs. When compared to a 2.6GHz CPU on a top of the range desktop it was possible to achieve up to a 36x speed-up and 16x speed-up for the fixed-point and floating-point designs respectively. For the fixed-point designs the errors introduced in the results due to the limited fractional resolution was investigated. Overall in the implicit option pricing example the errors were well behaved with the maximum for the 22 and 14 bit fractional representations only being 10x that of the expected rounding error, and 50x for 30 fractional bits. It is intended that this work is further integrated into a larger FPGA based implicit pricing system to achieve a high speed and low cost solution for accelerating options pricing. Future work will look at improving the accuracy whilst trying to retain high clock rates and low FPGA resource usage by using mixed-precision architectures; for example computing the forward iterations in 16bit fixed-point and the backwards in 32bit floating-point. Following up from the theoretical analysis further work with affine arithmetic techniques [19] it is possible to develop a deeper understanding of the fixed-point error behaviour and propagation in the algorithm. Advancing from this work it would be enlightening to also investigate the performance of more inherently parallel algorithms such as parallel cyclic reduction on an FPGA.

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