A Serial-Timing Multi-Channel CMOS Charge Readout ASIC for X-Ray Detectors

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Abstract This paper presents a serial multi-channel front-end readout ASIC with a novel architecture and timing control scheme, for the application of flat-panel X-ray, linear detectors and other similar fields. The proposed architecture features the single multi-range selectable integrator, two multiplexed correlated double sampling (CDS) circuits, and the differential buffer output. With the proposed sequential timing control, each channel can output data to the corresponding CDS circuit with no delay when the integration state is ended. So, the channel circuit is simplified. In addition, the proposed architecture and timing control scheme enables the readout ASICs to be cascaded for more channels with tunable conversion rates. To verify the proposed architecture and timing control scheme, a 32-channel readout ASIC was fabricated in TSMC 250nm mixed CMOS signal process. The die size is 2.8 \( \times \) 2mm\(^2\). At room temperature, the measured equivalent input noise (EIN) is 25ppm of full-scale value (FSR) with an integration range of 12\( \mu \)C. The measured integral non-linearity is less than 0.04\%, and the average power consumption is 2mW per channel. When four ASICs are cascaded, 128 channels are achieved, and a conversion rate over than 30kS/s is measured.

key words: CMOS Circuits, Correlated Double Sampling X-ray Imaging, Front-end Readout ASIC, X-ray Detectors

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

X-RAY ray detector is becoming more and more important in the imaging field. It is also widely used in medical imaging [1–4], material property analysis [5–7], high-energy physics [8–12], etc. With the development of the digital imaging sensor technology, to achieve high-quality images and higher integration with low power consumption and low cost, the acquisition and processing of the detector output signals need to be improved. Therefore, the front-end readout circuit of the detector becomes a prime design issue.

Figure 1 shows the traditional structure of the readout circuit with 32 channels [10]. In each channel, several capacitors and sub-circuits are needed, which consists a front-end charge-sensitive amplifier (CSA), a low pass filter, a CDS circuit, and a track-and-hold (T/H) circuit. The multiple capacitors and sub-circuits increase the power consumption, silicon area and complexity of each channel, making it difficult to integrate more channels on an ASIC. During operation, all the channels start to integrate the weak current signal from the imaging pixels simultaneously. When the integration is completed, each channel data has to be held temporarily in the corresponding large capacitors, \( C_1-C_{32} \), waiting for the following ADC conversion. With more channels, the difference between the hold time of each channel data becomes greater, leading to the inconsistent data variation among channels and degrading the resolution of the X-ray detector. In addition, more channels require more paralleled ADCs or higher speed ADC, causing to a higher cost [13–18]. What’s more, due to the simultaneous convert and reset operation, greater driving capability is required on the external reference \( V_{REF} \), and thus internal pre-charging circuit has to be used, which not only increases the power consumption, but also brings extensive digital noise to the system [19].

To overcome the drawbacks of the traditional structure, a novel circuit architecture and timing control scheme is proposed in this paper, which features small chip area, low power consumption and low cost. In addition, the proposed readout ASIC supports simple multi-chip cascading, extending the number of channels without more post-stage ADCs. In previous articles [19–24], the
detection-related noise analysis has been described in great detail, including detection-semiconductor material noise, transmission line noise, readout circuit noise and other aspects [25-27]. So, this paper will mainly focus on the features of the proposed circuit structure and the timing sequence control, as well as the improvement of the linearity.

The rest of the paper is organized as follows: Section II introduces the architecture characteristics and timing control scheme of the proposed readout circuit structure. Section III explains the function and test cases, and Section IV summarizes the conclusions.

2. Proposed Circuit structure and Characteristics

Figure 2 shows the basic block diagram of the proposed serial readout circuit (SRD), which mainly includes 32 input channels, a digital logic unit, and two multiplexed CDS circuits, CDS1 and CDS2. Compared with the traditional structure shown in Fig. 1, only one CSA circuit is used in each channel, greatly simplifying the circuit complexity. In this paper, CDS1 and CDS2 are reused respectively by the odd-numbered and even-numbered channels, with the time-division multiplexing timing. As shown in Fig. 2, CDS1 and CDS2 can eliminate the inherent noise and the reset noise of the channel, and are designed to output differential driving signals, VOUT and VOUTN, directly driving the external ADC circuit. VREF is the external reference. As VREF only drives one channel in one clock cycle, extra pre-charging circuit is no longer necessary for driving capability enhancement.

During operation, the timing of one channel is delayed by t0 compared to the one of the previous channel. To complete the data acquisition and output, each channel needs to go through three states: integrate, convert and reset. In one clock cycle, the convert and reset of each channel are completed independently. At the end of the integrate state of the ith channel, CDS1 or CDS2 is activated by the sequential control circuit and begins to work immediately. Then the channel data S[i]

![Fig. 2](image-url)  
**Fig. 2** Basic structure diagram of the proposed SRD.

is sampled and differentially output without additional T/H circuit or holding capacitor. From the perspective of structural characteristics, to integrate more channels, all we need to do is to add more channel integrators. As for the point of view of serial timing, it overcomes the complexity increasing in timing control brought by more channels, and the requirements on ADC and other circuits doesn’t increase, which helps to achieve higher integration level and lower power consumption.

2.1 High Linearity Integrator

The proposed readout circuit in this paper is based on charge integration, and Fig. 3 shows the integrator proposed in this paper, which is composed of a charge-sensitive amplifier (CSA) and the feedback capacitor array. The output voltage of the integrator, \( V_{CSA} \), is proportional to the input charge, and thus high linearity and sensitivity are required. The input terminal, \( I_N \) (IN), is connected with the pixel circuit of the X-ray detector. \( C_1-C_4 \) are the feedback capacitors, and the corresponding capacitances are 1pF, 2pF, 4pF and 8pF, respectively. \( S_1-S_4 \) is used to tune the total feedback capacitance, represented as \( C_{INT} \), in a range of 1pF to 15pF, with a step of 1pF. \( SZ \) is the reset signal to reset \( V_{IN} \) and \( V_{CSA} \). The integrator can transform the current signal from the pixel circuit to a voltage signal, \( \Delta V_{CSA} \), which can be given by

\[
\Delta V_{CSA} = \frac{Q_{DE}}{C_{INT}} \times \frac{1}{1 + \frac{1}{A}}
\]

(1)

where \( Q_{DE} \) is the total input charge integrated on \( C_{INT} \), and \( A \) is the DC gain of the CSA. Only when \( A \) is infinitely large, equation (1) can be simplified as

\[
\Delta V_{CSA} = \frac{Q_{DE}}{C_{INT}}
\]

(2)

For a given \( Q_{DE} \), the finite gain of the CSA affects the
linearity of the integrator output. Therefore, the folded-cascade amplifier [28, 29] is used in this paper.

Except for a high gain of the CSA, an accurate QDET is also essential for the linearity of the integrator. As the process size shrinks, the influence of various leakage currents in the integrator cannot be ignored, such as the leakage current from the transistor switch and thin gate oxide [30]. Usually when the transistor switch is off, the PN junctions between the source, drain and the substrate are reversely biased, causing a reverse saturation current flowing into the substrate. The higher the reverse bias voltage is, the greater the leakage current is. In other words, when the transistor is turned off, the gate voltage is 0V, and different drain voltage will result in different channel current. When the gate to drain voltage changes, the leakage current of the transistor also changes. In this paper, S1-S4 are the main leak current sources. In the integration process, VCSA is changing constantly. In different integration cycles and channels, VCSA has different voltage change slope. Therefore, a simple P/N MOS transistor switch pair cannot meet the requirement of high linearity. Based on above leakage current analysis, this paper proposes a novel switch structure, as shown in Fig. 3(c). Compared with the traditional switch structure, a transistor NM1 is added. When SW1 is turned off, NM1 is turned on, pulling the voltage of node B to 0 or VREF, and keeping the voltage at both terminals of SW1 equal. However, the existence of NM1 makes the feedback capacitor the load capacitor of CSA. So, another switch is added on the right side of feedback capacitor to maintain the load capacitance of CSA.

2.2 Correlated Double Sampling Circuit

As shown in Fig. 2, there are two CDS circuits in the proposed readout circuit. One is connected to odd-numbered channels, and the other one is connected to even-numbered channels. The schematic of the CDS circuit is shown in Fig. 4, which consists of two switched capacitor amplifiers for differential output. The ratio of C6/C5 and C3/C7 is the voltage gain of the CDS circuit. A detailed description is as follows:

Before one channel finishes the integration, SX keeps on, S1 and SC keep off. The output voltage of the channel is directly connected with C5 and C6, realizing the first sampling. The charge distribution on C5 and C6 are:

\[ Q1(01) = \frac{I_{\text{DET}}}{C_5} \]  
\[ Q2(01) = \frac{I_{\text{DET}}}{C_6} \]  

where Vref is the reference voltage. When the integrate state ends, SX keeps on for next one clock cycle, S1 keeps off, while SC turns on. Thus, the CDS circuit completes the second sampling and realizes the differential data output simultaneously. Now, the total charges on C5 and C6 are:

\[ Q1(02) = \frac{I_{\text{DET}}}{C_5} + \frac{I_{\text{DET}}}{C_3} \]  
\[ Q2(02) = \frac{I_{\text{DET}}}{C_6} + \frac{I_{\text{DET}}}{C_7} \]  

where Vref is the output noise signal of the channel, VO3 and VO5 are the offset of A1 in the first and second sampling, respectively. According to the conservation of charge [28]:

\[ \Delta Q1 = \Delta Q2, \]  
\[ V_{O+} = V_{\text{REF}} + (V_{\text{REF}} - V_{\text{CSA}}) + (V_{\text{OS1}} - V_{\text{OS2}}), \]  
\[ V_{O-} = V_{\text{REF}} - (V_{\text{REF}} - V_{\text{CSA}}) + (V_{\text{OS3}} - V_{\text{OS4}}). \]  

2.3 Serial Sequential Logic Circuit Design and Analysis

In this paper, the serial timing control is adopted to realize the function of multi-channel data acquisition and output, without sacrificing the pixel accuracy of the X-ray detector. In addition, the serial timing control is also the reason why the structure of the proposed readout circuit can be simplified.

As shown in Fig. 5, CLK is the external clock and C1 is a trigger pulse signal. The pulse width of C1 is larger.

\[ \frac{V_{\text{CSA}}}{I_{\text{CSA}}} = \frac{V_{\text{REF}}}{I_{\text{REF}}} \]  
\[ V_{\text{CSA}} = \frac{V_{\text{REF}}}{I_{\text{CSA}}} C_{\text{CSA}} \]  
\[ V_{\text{CSA}} = \frac{V_{\text{REF}}}{I_{\text{CSA}}} C_{\text{CSA}} \]  
\[ V_{\text{CSA}} = \frac{V_{\text{REF}}}{I_{\text{CSA}}} C_{\text{CSA}} \]  
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As shown in Fig. 5, CLK is the external clock and C1 is a trigger pulse signal. The pulse width of C1 is larger.
than the clock period. CLK samples $C_I$ through a register to generate a synchronized square wave. Then through the shift register, the 32 square wave pulse signals, $S_X[1]-S_X[32]$, are generated. As depicted in Fig. 2, $S_X[i]$ selects the $i^{th}$ channel to be connected with the corresponding CDS circuit. In addition, other control timing signals are generated based on $S_X[1]-S_X[32]$, such as the integrator reset signal $S_Z$, the control signal $S_I$, $S_C$ in the CDS, and so on.

Figure 6(a) shows the working timing of the integrator in single channel. The integrator has three working states, the integrate state, the data convert state, and the reset state. When $S_Z$ is high, the integrator enters the reset state, and the output terminal of the integrator is connected to $V_{REF}$. When $S_Z$ is low, the integrator enters the integrate state, and the output voltage decreases monotonically with the accumulation of input charge. In one clock cycle before the end of the integration, $S_X$ changes from low to high, and the output voltage of the integrator is output to the CDS circuit. Simultaneously, the CDS circuit is now in the first sampling stage. And the switching noise of the integrator will not be transmitted to the CDS. When $S_Z$ changes from low to high, the integrator enters the convert state, and $S_X$ maintains the high level for another period. When the data converting is completed, $S_X$ turns from high to low and the reset state starts, while $S_Z$ keeps high. After resetting, $S_Z$ changes from high to low, and the next round of integration begins.

Figure 6(b) shows the timing diagram of the 32 channels. $S_X$ and $S_Z$ of adjacent channels are delayed by $t_D$. $S_I$ and $S_C$ are CDS control signals. The 32 channels are reset by $S_Z$ one by one. After each channel is reset, integration starts immediately. The first cycle before the end of the first channel integration, $S_I$ and $S_X$ change from low to high and the output terminal of the channel integrator is connected to the CDS circuit. When $S_Z$ is high and $S_C$ is high, the output voltage of the integrator is reversed and output by the CDS circuit. Whenever the $S_C$ is high, there is a channel of data output. The $S_C$ remains low while all channel outputs are complete.

The CDS circuit is controlled by $S_I$ and $S_C$. A complete data conversion requires two phase changes of the $S_I$ and $S_C$. In order to ensure continuous output without interval between channels, two CDS circuits are used. The odd-numbered channels share one CDS, and the even-numbered channels share the other CDS, continuously sampling and converting alternatively, so that each channel can complete data output within one clock cycle.

Figure 7 shows the channel data convert and output at the end of the integrate state. When the integration of the
first channel is over, the $S_C$ control signal is activated. When it is high, the data of the odd-numbered channels is converted and output, and when it is low, the data of the even-numbered channels are converted and output. When the data of all channel is output, $S_C$ and $S_l$ keep at ‘0’ until the end of the next integrate state.

2.4 Serial Cascade
To increase the number of channels, N chips can be directly cascaded for $32*N$ channels without additional control signals and ADC circuits. It should be noticed that there is a delay of $32*N*t_0$ between the first channel and the last channel, in which $t_0$ refers to the delay between adjacent channels and can be adjusted by the external clock. Delays may affect image quality, especially when the object under test is moving rapidly. To avoid this situation, the integration time of a single channel is usually much greater than the total delay. So, in real application, the number of chip cascades should be carefully selected on request of the delay tolerance.

3. Prototype and Measurement
The Serial-Timing prototype readout ASIC was fabricated in TSMC Foundry 2P4M 0.25μm mixed CMOS technology and the chip micrograph is shown in Fig. 8. Its size is $2.8 \times 2$ mm$^2$. The measured power consumption is 2 mW/ch with a 2.5V/5 V supply.

3.1 Measurement Results of ASIC

\[
\text{The measured noise level of ADC standardized quantization}
\]

\[
\begin{array}{c|c|c}
\text{High energy} & \text{Low energy} \\
\hline
\text{Fitting value I} & \text{Fitting value II} \\
\end{array}
\]

Fig. 10 Multichip cascading noise floor test diagram with high energy and low energy X-ray. (a) The standardized quantized minimum noise value of the 16-bit ADC without PD connection, and (b) the standardized quantized minimum noise value of the 16-bit ADC with PD connection.

\[
\text{The measured noise level of ADC standardized quantization}
\]

\[
\begin{array}{c|c|c}
\text{High energy} & \text{Low energy} \\
\hline
\text{Fitting value I} & \text{Fitting value II} \\
\end{array}
\]

Fig. 11 The measured linearity of the single channel. (a) Test 32 steps, showing the fitted value I using the traditional switch F1, the fitted value II using the proposed switch F2 in Fig. 3 linear chart, and (b) INL for F1 and F2 switch in Fig. 3 throughout the input dynamic range of ASIC.
### Table 1 Performance summary

| Technology | TSMC 250nm 2p4M |
|------------|-----------------|
| Number of channels | 32 |
| Power supply | 2.5/3V |
| Power consumption | 2mW/channel |
| Maximum input charge | 12pC |
| EIN with tPD with PD | 155μV |
| EIN with PD | 35μV |
| ADC resolution (external) | 16bit |
| INL | 0.04% |
| Die size | 2.8 x 2mm² |

### Conclusions

In this paper, an X-ray detector readout circuit with novel architecture and serial timing is presented. Each channel is simplified, reducing area and power loss. The two CDS circuits not only eliminate part of the noise, but also realize differential output, continuous alternating work and serial timing control, so that there is no waiting time for each channel to switch between the three working states. In application, the cascading of the ASICs increases the channel number. In order to make the proposed architecture and serial timing more flexible for different applications, the series-parallel conversion and ADC integrated chip will be integrated on a single chip in further work.

### References

[1] C. Chaussat, et al.: “New CsI/a-Si “17 x17” X-ray flat panel detector provides superior detectivity and immediate direct digital output for general radiography systems,” in Proc. SPIE, 3336 (1998) 45 (DOI: 10.1117/12.317049).

[2] T. Ottaviani and K. S. Karim: “Custom column readout circuitry to extend the dynamic range of a-Si:H current mediated pixel amplifiers for large area diagnostic X-ray imaging applications,” IEEE Cat. 3 (2004) 1711 (doi: 10.1109/CCECE.2004.1349743).

[3] M. Choquette, et al.: “Performance of a real time selenium based x-ray detector for fluoroscopy,” in Proc. SPIE, 4320(2001) 501 (DOI:10.1117/12.430873).

[4] P. R. Granfors, et al.: “Performance of a 41x41 cm amorphous silicon flat panel x-ray detector designed for angiographic and R&F imaging applications,” Med. Phys. 30 (2003) 2715 (DOI:11.1118/1.1609151).

[5] V. Tsenov: “Methodology for analysis of defects in electronic assembly using X-ray,” IEEE, ISCE, Paper (2018) 1 (DOI: 10.1109/ETC.2018.8549637).

[6] A. P. Dhawan: “Medical Imaging Modalities: X-ray Imaging,” (John Wiley & Sons, Ltd. 2010) ch4.

[7] R. Ning, et al.: “Flat panel detector-based cone-beam volume CT angiography imaging: system evaluation,” IEEE. Medical Imaging 1 (2004) 949 (DOI: 10.1016/S1076-6332(03)00519-1).

[8] J. Luo, et al.: “Development of a low noise readout ASIC for CZT detectors,” Journal of Instrumentation 7 (2012) 8030 (DOI: 10.1088/1748-0221/7/08/P08030).

[9] M. Manghisoni, et al.: “Introducing 65nm CMOS technology in low-noise read-out of semiconductor detectors,” Nuclear Inst & Methods 624 (2010) 373 (DOI: 10.1016/j.nima.2010.02.266).

[10] E. Beuville, et al.: “A high performance, low-noise 128-channel readout integrated circuit for instrumentation and X-ray applications,” IEEE NSS 1 (2004) 142 (DOI: 10.1109/1462169).

[11] O. Gevin, et al.: “A CMOS ASIC for the Readout of CdTe and CdZnTe Detectors for High Resolution Spectroscopy,” in IEEE Transactions on Nuclear Science 56 (2009) 2351 (DOI: 10.1109/TNS.2009.2023989).

[12] M. Porro et al.: “A 128-Channel ASIC for the Readout of PNCCDs and DEPFET Arrays for X-Ray Imaging, Spectroscopy and XFEL Applications,” in IEEE Transactions on Nuclear Science 60 (2013) 446 (DOI: 10.1109/TNS.2012.2228410).

[13] S. Lee, et al.: “A 5.2-Mpixel 88.4-DB DR 12-in CMOS X-Ray Detector With 16-bit Column-Parallel Continuous-Time Incremental ΔΣ ADCs,” IEEE J. Solid-State Circuit 55 (2020) 2878 (DOE: 10.1109/JSSC.2020.3011967).

[14] J. Kim, et al.: “A High-Speed Wafer-Scale CMOS X-Ray Detector With Column-Parallel ADCs Using Oversampling Binning Method,” IEEE Transactions on Electron Devices 62 (2015) 888 (DOI: 10.1109/TED.2014.2386533).

[15] Z. Zhenwei, et al.: “A 16-bit 8-MS/s SAR ADC with a foreground calibration and hybrid-charging-supply power structure,” IEICE Electron. Express 17 (2020) 2020097 (DOI: 10.1587/elex.17.2020097).

[16] Y. Tang, et al.: “A Low-Power 16-Channel Sipm Readout Front-end with a Shared SAR ADC in 180 nm CMOS,” IEEE ICSICT (2020) (DOI: 10.1109/ICSICT94987.2020.9278142).

[17] E. Beuville, et al.: “High performance, low-noise, 128-channel readout integrated circuits for flat panel x-ray detector systems,” in Proc. SPIE, 5368 (2004) 2 (DOI: 10.1117/12.535842).

[18] J. Y. R., et al.: “CMOS Flat-Panel X-Ray Detector with Dual-Gain Active Pixel Sensors and Column-Parallel Readout Circuits,” IEEE Transactions on Nuclear Science 61 (2014) 2472 (DOI: 10.1109/TNS.2014.2343549).

[19] S. Adachi, et al.: “A 128-Channel CMOS Charge Readout ASIC for Flat-Panel X-Ray Detectors,” IEEE Transactions on Nuclear Science 55 (2009) 3673 (DOI: 10.1109/TNS.2008.205105).

[20] W. Sansen and Z. Y. Chang: “Limits of low noise performance of detector readout front ends in CMOS technology,” IEEE Trans. Circuits Syst. 37 (1990) 1375 (DOI: 10.1109/31.62412).

[21] S. Adachi, et al.: “Noise properties of a Se-based flat-panel x-ray detector with CMOS readout integrated circuits,” in Proc. SPIE 4682 (2002) 580 (DOI: 10.1117/12.465003).

[22] S Y. Vuk, et al.: “Design and Evaluation of a 2D Array PIN Photodiode Bump Bonded to Readout IC for the Low Energy X-ray Detector,” 1 (2006) 1986 (DOI: 10.1109/2006.260570).

[23] S. Adachi, et al.: “Noise properties of a Se-based flat-panel x-ray detector with CMOS readout integrated circuits,” in Proc. SPIE 4682 (2002) 580 (DOI: 10.1117/12.465003).

[24] B. C. Kim, et al.: “Temporal Noise Analysis and Reduction Method in CMOS Image Sensor Readout Circuit,” IEEE Trans Electron Devices 56 (2009) 2489 (DOI: 10.1109/20.2036019).

[25] A. Tetsuya, et al.: “Modulation transfer function analysis of silicon X-ray sensor with trench-structured photodiodes,” IEICE Electron. Express 15 (2018) 20180177 (DOI: 10.1587/elex.15.20180177).

[26] G. F. Moroni et al.: “Interleaved Readout of Charge-Coupled Devices for Correlated Noise Reduction,” IEEE Trans Instrum Meas 69 (2020) 7580 (DOI: 10.1109/TIM.2020.2980461).

[27] G. Zentai, “Comparison of CMOS and a-Si flat panel imagers for X-ray imaging,” IEEE Imaging Systems and Techniques Paper (2011) 194 (DOI: 10.1109/IST.2011.5962217).

[28] P. Gay and R. Meyer: Analysis and Design of Analog Integrated Circuits (New York: Wiley, 1993) 3rd ed.

[29] W. Sansen: Analog Design Essentials (Springer, Boston, 2006) 149.

[30] B. G. Streetman Sanjay Banerjee “Solid State Electronic Devices” (Prentice-Hall, 1980) 6th ed. 257.