Design of Compact and Smart Full Adders for High-Speed Nanometer Technology IC’s

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Abstract: It is intensely acknowledged that the key handing out unit of any device competent of carrying out computations is the CPU (Central Processing Unit) and one of the most elementary and central parts of CPU is an ALU (Arithmetic and Logical Unit). The ALU is primarily responsible for carrying out the logical operation, arithmetic operations etc. The proposed full adder has low power consumption and better area efficiency. Post layout simulations using the Mentor graphics tool have been evaluated. The circuits proposed are extremely optimize in terms of transistor switching power and latency, due to small load capacitance and low dissipation of short circuit electricity. Each of the suggested and simulated circuits has its own benefits of speed, power Dissipation, Power Delay Product (PDP), and driving capability. The circuits proposed are studied in terms of voltage input and threshold voltage variations, output load variations, signal to ratio with respect to transistor scaling.

Key words: Full Adder, Power Delay Product (PDP) and Field, CMOS logic, Low power, Configuration Transistor, X-OR, X-NOR.

1. Introduction

omnipresent electronic systems, nowadays became indivisible part of daily life. Digital circuits, such as microprocessors, Smart electronic devices, form significant proportion of electronic systems[1-4]. With increase in integration scaling, circuit utility is limited by the increasing amounts of transistor switching and layout consumption. So with rising reputation and requirement for portable wireless driving devices such as cellular phone’s and laptops while maintaining their swiftness, designers are trying to increase battery usage and size of such systems. The performance of numerous electronic applications appertain to the efficient execution of the arithmetic circuit. Even though much efforts are put on designing adders with minimal and small size transistors VLSI designing is still under progressing stage. Effective adder structures have been configured to explore, example carry pick, conditional number, and carry look-ahead summers. At the centre of attention is the 3-bit adder as the elementary block of these structures[3],[4]. The addition is one of the basic arithmetic operations and is commonly used in many VLSI systems.

In most of those systems, it is the core element of complicated arithmetic circuits that is the adder portion of the essential path that defines system performance and hence the complete adder. Full adders are generally designed using gates X-NOR and X-OR. With complete adder, the major power user is the X-OR or X-NOR circuit. Thus the power consumption of the complete adder can be minimized by reducing X-OR or X-NOR circuit power consumption to a minimum. X-OR or X-NOR gate is also used in many other circuits, such as circuits and comparators for parity tests. X-OR, X-NOR and simultaneous high speed and low power[5-7].

Basic structures of X-OR and X-NOR gates. The X-OR/X-NOR gates are the chief components for energy consumption of a Full-Adder cell. The power consumed by Full-Adder cell may be trim down by best possible design of X-OR/X-NOR gates. The X-OR/X-NOR gates have many
functionalities in electronic chip designs. Many circuits have been anticipated to realize X-OR/X-NOR gate. Many hybrid full adders are proposed using X-OR and X-NOR gates. Two new methods for applying the transistor-level exclusive-OR and exclusive-NOR functions are suggested. The first approach uses non-complementary inputs of signal and the fewest number of transistors. The other one increases the efficiency of the preceding process but uses two more transistors. The expressions for the X-OR and X-NOR gates are shown in equation (1) and (2):

Here we consider the inputs as A and B then,

\[\text{XOR} = A \cdot \overline{B} + A \cdot \overline{B} \]  \hspace{1cm} (1)
\[\text{XNOR} = A \cdot B + \overline{A} \cdot \overline{B} \]  \hspace{1cm} (2)

Complete Adder is the adder that adds 3 inputs and generates 2 outputs. The first two inputs are A and B, and the third is a carrying input as \(C_{-\text{IN}}\). The carry output is \(C_{-\text{OUT}}\) and the usual output is S which is SUM. A complete adder logic is designed in such a way that eight inputs can be taken together to construct a byte-wide adder and cascade the carry bit from one adder to another[7-9].

\[
\text{Adder}_{\text{sum}} = ((A \oplus B) \oplus \overline{C_{\text{in}}}) \\
\text{Adder}_{\text{carry}} = AB + (A \oplus B)C_{\text{in}}
\]  \hspace{1cm} (3)
\hspace{1cm} (4)

There are different types of full adders using transistor design like 20 Transistors (20T), 14 Transistors (14T) and 22 Transistors (22T). It is based on the 4-transistor implementations of the XOR and XNOR functions. It balances the generating delay, which leads to fewer glitches at the output. This eliminates the short-circuit power component within the cell (normally 5\%–20\% of the dynamic power).

The CMOS devise approach is not an proficient area in large fan-ins with complex gates for 28T full added cell. So when choosing a inactive logic approach to understand a logic function, lot of care is necessary. The Method of Pseudo NMOS is straight forward. The pass semiconductor rationale style is known to be a famous technique for executing some particular circuits, for example, multiplexers and XOR-based circuits, similar to adders. The circuit of HFA-20T is less power efficient as inverters through significant pathway contains of 20 MOS devices[10]. The advantages of this structure are complete logic swing output, high energy consumption and very high pace, heftiness next to external deliver, voltage And transistor scaling. The difficulty of HF-A-20T is diminution of load pouring competency for ripple structure adders.

The circuit HFA-19T design is constructed with less number of transistors. XOR and XNOR along with C input are used to generate Sum output. If the C signal generates SUM, transmission gates are not driven by XOR-XNOR gates, instead the gates drive the data and select lines of 2X1 Multiplexer[9-11]. So the capacitance of XOR and XNOR hubs end up being more modest and the execution season of the circuit will be improved. The circuit HFA-19T have been made by applying the above plan to HFA-20T individually. It is normal that the force utilization and deferral of the HFA-19T FA circuits are diminished than that of HFA-20T correspondingly (in spite of having one more semiconductor), because of the more modest bordering capacitance of XOR and XNOR. Contrasted with the past works in the full snake, the improvement of the 14 T full adders prompted better outcomes for the deferral just as force utilization. Elite multipliers with less force dissemination performed well with 14 T full adders[12-14]. Notwithstanding, the snake didn't show improvement in edge power failures.
2. Proposed Adders
The choice of a suitable adder with mandatory assets is at most given priority for the proficient running of the circuit[21-25]. In this section, two new hybrid full adders are proposed. First, the 10T adder is a combination of CMOS with transmission gates. Later the completely enhanced version of 10T full adder is 6T which is purely a mixed logic style.

2.1. Static Power Revitalization Full adder (10 T) 1-bit Adder
Static Power Revitalization Full adder (SERF) design is presented by using 10 number of transistors, which does not require inverted inputs. 10T FA consists of two 4-transistor XNOR circuits constructed using CMOS like structure and one 2-to-1 multiplexer using transmission logic style. This circuit reduces the static power dissipated by stage-1 of XNOR circuit by reutilizing the energy as power rails to the next state of XNOR logic.

2.2. 6T Proposed 3-bit Adder.
Here a 2 semiconductor XNOR door is the fundamental part and subsequently two XNOR entryways have been utilized. And furthermore a multiplexer has been utilized. Subsequently the quantity of required semiconductors for full adders has been diminished to six and its circuit. Because of the use of less number of semiconductors, it has demonstrated a striking improvement in zone and postponement. Despite the fact that the depicted circuit gave less force utilization and expanded postponement, we can see from the reproduction results that there are a few contortions at the yield. In our proposed plan we use Pass semiconductor rationale and we have additionally taken consideration to decrease the quantity of semiconductors. By lessening the quantity of semiconductors utilized, a speed up in dataflow has
been accomplished. Additionally, the decrease in semiconductor use has lead to a decrease in the territory and force utilization.

3. Results and Discussions

Analysis of 14T, 10T and 6T Adders are performed in mentor graphics using 45nm technology. The Dynamic power dissipation of proposed 10T and 6T adders are compared with existing 14T for 1-bit, 16-bit and 32-bits. Table: 1 is tabulated by calculating switching power dissipation by varying supply voltage from 0.8V to 1.2V for the 3-techniques. The power dissipation is defined by two dynamic components one is power due to load capacitance and secondly short-circuit power [15-17],[26]. The effect of capacitance is directly proportional to power and defined by following equation (5).

\[ \text{PT-Switching} = \eta CV_s^2f \]  
(5)

Where PT-Switching = Transistor switching Power Dissipation, \( \eta \) = Switching Activity factor, 
\( C \) = Varying Capacitance, \( V_s \) = Source Voltage, \( f \) = frequency of operation

Transistor switching power can be a greatly reduced by cutting short the number of transistors, scaling down the devices, reducing source voltage without effecting logic swing and by low frequency of operation which now a days is a tradeoff. In CMOS technology when transistor switches from ON to OFF or vice versa. Due to this switching a small amount of leakage current flows between power rails[18-23]. As the duration of leakage current flows this may lead to degradation of multiplier overall performance. In this paper the leakage power (PL) is calculated based on the mathematical formula given in equation (6),(7),(8).

\[ \text{PL} = V_T^2E_1E_2 \]  
(6)

Where \( V_T \) is the voltage dependent on Temperature (\( KT/q \))
And $E_1$ and $E_2$ are exponential constants expressed as

$$E_1 = \exp \left( \frac{(V_{GS}-V_{th})}{\alpha V_T} \right) \quad (7)$$

$$\alpha = \text{Constant}, \ V_{th} = \text{Threshold Voltage} \ V_{GS} = \text{Gate-Source Voltage} \ V_{DS} = \text{Drain-Source Voltage}$$

$$E_2 = 1 - \exp \left( \frac{-V_{DS}}{V_{TH}} \right) \quad (8)$$

**Table 1**: Comparison of power dissipation between 6T, 10T and 14T FA using 1-bit, 16-bit and 32-bit adders

| Voltage $V_{DD}$ (V) | Power Dissipation 6T (mW) | Power Dissipation 10T (mW) | Power Dissipation 14T (mW) |
|----------------------|---------------------------|---------------------------|---------------------------|
|                      | 1-bit | 16-bit | 32-bit | 1-bit | 16-bit | 32-bit | 1-bit | 16-bit | 32-bit |
| 1.000                | 7.82  | 15.64  | 29.71  | 0.012 | 0.025  | 0.050  | 0.212 | 3.229  | 9.687  |
| 1.200                | 9.16  | 18.55  | 30.05  | 0.0132| 0.037  | 0.074  | 0.247 | 4.159  | 10.477 |
| 1.400                | 13.45 | 31.20  | 61.15  | 0.0158| 0.058  | 0.116  | 0.445 | 7.314  | 12.157 |
| 1.600                | 17.23 | 36.18  | 68.38  | 0.0167| 0.084  | 0.169  | 0.682 | 11.019 | 19.23  |
| 1.800                | 19.30 | 42.46  | 73.19  | 0.0180| 0.104  | 0.209  | 0.921 | 14.793 | 21.33  |
| 2.000                | 21.64 | 43.49  | 78.54  | 0.025 | 0.267  | 0.533  | 1.060 | 17.025 | 28.31  |
| 2.200                | 25.77 | 59.27  | 82.39  | 0.051 | 0.823  | 1.646  | 1.227 | 19.689 | 32.65  |
| 2.400                | 29.16 | 61.23  | 88.17  | 0.083 | 1.335  | 2.669  | 1.409 | 22.160 | 35.12  |
| 2.600                | 33.22 | 68.10  | 92.13  | 0.120 | 1.915  | 3.830  | 1.600 | 25.660 | 39.34  |
| 2.800                | 36.50 | 74.05  | 97.89  | 0.103 | 1.647  | 3.293  | 1.793 | 28.749 | 46.13  |
| 3.000                | 39.91 | 79.82  | 102.81 | 0.104 | 2.145  | 3.339  | 1.988 | 31.869 | 49.56  |
| 3.200                | 42.67 | 84.54  | 109.32 | 0.106 | 3.133  | 3.382  | 2.183 | 34.974 | 55.14  |

### 3.1 Slew Rate Calculations

Slew rate comparison for rise time and fall time are done by taking 10% to 90% of the rise from 0 to 1of maximum supply value, and fall time as 90% to 10% of minimum supply value. Table 2 and Table: 3 exhibits $T_{\text{rise}}$ and $T_{\text{fall}}$ for 1-bit, 16-bit and 32-bit for 14T, 10T and 6T adders.

**Table 2**: Comparison of rise transition delay for 6T, 10T and 14T FA using 1-bit, 16-bit and 32-bit adders

| Capacitance (pF) | Rise Delay of 10T (ns) | Rise Delay of 14T (ns) | Rise Delay of 6T (ns) |
|------------------|------------------------|------------------------|-----------------------|
|                  | 1-Bit | 16-Bit | 32-Bit | 1-Bit | 16-Bit | 32-Bit | 1-Bit | 16-Bit | 32-Bit |
| 0.000            | 7-9   | 7-6    | 8-6    | 9-12  | 22-40 | 24-42 | 2.9   | 5-9    | 11-12.3 |
| 15.000           | 19-23.4 | 9-26 | 9-24 | 42-49 | 24-42 | 26-47 | 11-21.2 | 10-15 | 11.3-18.5 |
| 30.000           | 24-265 | 11-32 | 9-26 | 70-85 | 26-44 | 31-52 | 18-22.4 | 8-15.5 | 12.3-23.4 |
| 45.000           | 28-396 | 12-38 | 10-29 | 98-121 | 28-46 | 33-50 | 23-29.6 | 12-21.3 | 13.2-24.1 |
| 60.000           | 28-527 | 13-45 | 11-32 | 126-157 | 31-48 | 34-52 | 24-42.5 | 11-9.31.7 | 14.4-26.5 |
| 75.000           | 26-658 | 13-52 | 11-35 | 154-193 | 33-50 | 37-55 | 20-51.8 | 14.5-33.6 | 14.8-29.3 |
| 90.000           | 21-788 | 14-60 | 12-38 | 181-230 | 35-52 | 36-59 | 19.8-65.2 | 14.8-41.3 | 15.6-33.9 |
Table: 3 Comparison of fall transition delay for 6T, 10T and 14T FA using 1-bit, 16-bit and 32-bit adders

| Capacitance (pF) | 1-Bit Fall Delay of 10T (ns) | 16-Bit Fall Delay of 10T (ns) | 32-Bit Fall Delay of 10T (ns) | 1-Bit Fall Delay of 14T (ns) | 16-Bit Fall Delay of 14T (ns) | 32-Bit Fall Delay of 14T (ns) | 1-Bit Fall Delay of 6T (ns) | 16-Bit Fall Delay of 6T (ns) | 32-Bit Fall Delay of 6T (ns) |
|-----------------|-----------------------------|-------------------------------|-------------------------------|-----------------------------|-------------------------------|-------------------------------|-----------------------------|-------------------------------|-------------------------------|
| 0.000           | 0.007-0.004                 | 0.007-0.006                  | 0.007-0.004                  | 0.009-0.012                 | 0.022-0.040                  | 0.010-0.015                  | 0.004-0.002                 | 0.005-0.003                  | 0.012-0.020                  |
| 15.000          | 0.019-0.136                 | 0.009-0.026                  | 0.019-0.136                  | 0.042-0.049                 | 0.024-0.042                  | 0.019-0.044                  | 0.016-0.116                 | 0.007-0.016                  | 0.014-0.022                  |
| 30.000          | 0.024-0.265                 | 0.011-0.032                  | 0.024-0.265                  | 0.070-0.085                 | 0.026-0.044                  | 0.023-0.046                  | 0.014-0.135                 | 0.009-0.022                  | 0.016-0.034                  |
| 45.000          | 0.028-0.396                 | 0.012-0.038                  | 0.028-0.396                  | 0.098-0.121                 | 0.028-0.046                  | 0.025-0.049                  | 0.018-0.166                 | 0.010-0.028                  | 0.020-0.036                  |
| 60.000          | 0.028-0.527                 | 0.013-0.045                  | 0.028-0.527                  | 0.126-0.157                 | 0.031-0.048                  | 0.026-0.051                  | 0.020-0.247                 | 0.013-0.035                  | 0.022-0.038                  |
| 75.000          | 0.026-0.658                 | 0.013-0.052                  | 0.026-0.658                  | 0.154-0.193                 | 0.033-0.050                  | 0.029-0.055                  | 0.016-0.258                 | 0.013-0.042                  | 0.023-0.040                  |
| 90.000          | 0.021-0.788                 | 0.014-0.060                  | 0.021-0.788                  | 0.181-0.230                 | 0.035-0.052                  | 0.026-0.061                  | 0.018-0.288                 | 0.012-0.048                  | 0.025-0.045                  |

From table: 1 it is observed that the rise in dynamic power dissipation from 1-bit to 32-bit full adder designed using 14T is 52.957 at 3.2V and 9.475 at 1V. 10T shows a rise in the value of 3.276mW from 1-bit to 32-bit at 3.2V and 0.038mW at 1V. 6T 1-bit adder shows more efficient results because the rise in power dissipation from 1-bit to 32-bit adder is only 66.65nW at 3.2V and 21.89nW at 1V.

In table: 2 and table: 3 rise time and fall time are tabulated it is clear that delay for 6T full adder from 1-bit to 32-bit is less when compared with 14T and 10T. The percentage reduction in delay for 6T 32-bit is 25.6% when compared with 32-bit 14T full adder. Delay contributed by 18.3%.

![Fig: 4 Power Delay Product of 32-bit adder](image-url)
4. Conclusion

Among the 1-bit adder proposed and presented in this paper, 6T full adder shows optimized results at a single bit, 16-bit and 32-bit adders. The percentage reduction in PDP for 32-bit adder designed using 6T FA is reduced by 27.3% and for 32-bit adder designed using 10T PDP is reduced by 19.75%. Switching power dissipation analysis is done from 1V to 3.2V of power supply. The proposed design displays very less transition delay which claims to be speed efficient in comparison with the other two designs. In the new era of VLSI and ULSI designs for accurate and high-speed processors, 6T adder is one of the optimized solutions.

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