An Improved Overmodulation Strategy for a Three-Level NPC Inverter Considering Neutral-Point Voltage Balance and Common-Mode Voltage Suppression

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Abstract: The three-level neutral-point clamped voltage source inverter (3L-NPC-VSI) is widely used in the maglev traction systems due to its high output voltage, large output capacity and low output current harmonics. In order to improve the utilization of the DC-bus voltage, an overmodulation strategy is necessary. This paper proposes an improved overmodulation strategy based on the minimum amplitude error method for a 3L-NPC-VSI. Compared with the conventional overmodulation strategy based on the minimum amplitude error method, the utilization of the DC-bus voltage is higher. Meanwhile, a virtual space vector modulation strategy is adopted for inverter neutral-point (NP) voltage balance and common-mode voltage (CMV) suppression. Furthermore, the suppression of leakage current also has been verified. Furthermore, the implementation details of the proposed overmodulation strategy based on minimum amplitude error method is elaborated. The effectiveness of the proposed method is verified by simulation and experimental results.

Keywords: three-level neutral-point clamped voltage source inverter (3L-NPC-VSI); maglev traction systems; overmodulation; virtual space vector

1. Introduction

The three-level neutral-point clamped voltage source inverter (3L-NPC-VSI) is widely used, not only in the industrial drives systems, but also transportation fields. It is preferred in many high-power scenarios, such as high-speed maglev traffic linear motor drive system [1–3]. This is due to its advantages such as simple topology, lower ripple and total harmonic distortion of output voltage and current compared to the two-level VSI [4–6].

Typically, an inverter can operate in the overmodulation region to fully exploit the DC-bus voltage, which can provide significant voltage improvement in many applications [7,8]. This is crucial for improving the output performance of the inverters, especially in the motor drive systems [9]. Therefore, the overmodulation strategy should be adopted to improve the inverter output performance. Furthermore, the effective usage of the overmodulation algorithm still guarantee the original performance when the DC-bus voltage drops. Commonly, overmodulation strategies is divided into two types, one is single-mode overmodulation strategy, the other is dual-mode overmodulation strategy. Except for the minimum angle error algorithm, some other single-mode overmodulation strategies, such as the minimum amplitude error method and the minimum vector error method, were proposed to increase the amplitude of output voltage vectors. The voltage projection of the minimum amplitude error algorithm is perpendicular to the hexagon boundary, while the voltage projection of the minimum vector error algorithm is parallel.
to the relative voltage vector with higher modulation index (MI) [9–11]. If the reference voltage vector is high enough, six-step operation will be achieved after voltage correction using these two improved algorithms, i.e., the output voltage vectors are the basic voltage vectors [12].

Considering classical dual-mode overmodulation strategy in [13], only the amplitude of reference voltage vector is modified based on the minimum angle error method in the first part of the overmodulation region. The amplitude and the angle of the reference voltage vector are both modified in the second part of the overmodulation region. A modified dual-mode algorithm has been presented in [14,15] to obtain the better harmonic performance. However, the dual-mode overmodulation strategy generally requires significant computational effort due to different variables and calculation procedures [16]. In [17], a novel overmodulation strategy based on voltage vector space division has been proposed to solve the problem that the voltage jumps between output voltage vectors in high overmodulation regions cause the deterioration of current performance and loading capability.

The algorithm complexity of single-mode overmodulation strategy is lower than that of the dual-mode overmodulation algorithm. In [18], the correction of the voltage vector is realized based on the minimum amplitude error method. Two implementation approaches, modulated model predictive control and space vector pulse width modulation (SVPWM), was provided to verify the overmodulation strategy on a two-level VSI with RL load. However, when the reference voltage vector operates in the overmodulation region in steady state, the method in [18] does not compensate for the output voltage defect caused by the overmodulation. Thus, its DC-bus voltage utilization is lower than that of the dual-mode overmodulation strategy. In general, the algorithm complexity of the single-mode overmodulation algorithm based on the minimum amplitude error method is almost the same as that of the dual-mode strategy, because the amplitude and angle usually need to be corrected [17].

The balance of the neutral-point (NP) voltage is important for the 3L-NPC-VSI, which is the premise of operation. The unbalancing of the NP voltage will increase harmonics, reduce output power quality and damage switching devices in power systems [19–21]. Shaft voltage and bearing current will be generated by the common-mode voltage (CMV), which may destroy the motor insulation in motor drive applications and increase the leakage current in the distributed generation applications [22–25]. Virtual space vector PWM (VSPWM) provides a new idea for the NP voltage control and the CMV suppression [26–33]. A novel VSPWM considering NP voltage balance and CMV suppression is proposed in [23]. In [26], a control strategy to realize the asymmetric control of the DC-bus voltages with VSPWM is studied. In [29], a switched-capacitor multilevel inverter with voltage boosting and CMV reduction capabilities has been studied. In [31], a novel modulation method has been proposed to reduce the CMV and balance the NP voltage and apply to the line voltage coordinate system.

The main contributions of this work are summarized as follows:

- An overmodulation strategy based on minimum amplitude error method is proposed to improve the utilization of DC-bus voltage;
- A VSPWM strategy is adopted to balance the NP voltage and suppress the CMV, and the leakage current has also been effectively suppressed;
- The difficulty of obtaining key variables in the overmodulation strategy is simplified by fitting.

The rest of paper is organized as follows. Section 2 presents the basic model of the 3L-NPC-VSI system. The principle of the proposed method is given in Section 3. Section 4 presents the VSPWM strategy considering the NP voltage balance and CMV suppression. Simulation and experimental results are shown and analyzed in Section 5. Finally, the conclusions are drawn in Section 6.
2. Model of 3L-NPC-VSI

For a 3L-NPC-VSI, the MI of the reference voltage vector can be expressed as:

$$MI = \frac{|\mathbf{u}_{ref}|}{2V_{dc}/3}$$  \hspace{1cm} (1)

where $u_{ref}$ represents the amplitude of the reference voltage vector, and $V_{dc}$ is the DC-bus voltage.

Figure 1 shows the topology of a 3L-NPC-VSI and its load. The 3L-NPC-VSI has 27 different switch states that together with the dc voltage can generate 19 voltage space vectors, as presented in the following:

$$\mathbf{u}_s = \frac{V_{dc}}{6} \begin{bmatrix} 2 & \frac{1}{2} - j\frac{\sqrt{3}}{2} & \frac{1}{2} + j\frac{\sqrt{3}}{2} \\ -1 & -1 + j\sqrt{3} & \frac{1}{2} + j\frac{\sqrt{3}}{2} \\ -1 & 1 + j\frac{\sqrt{3}}{2} & -1 - j\frac{\sqrt{3}}{2} \end{bmatrix} \mathbf{S}$$  \hspace{1cm} (2)

where $u_s$ are the voltage vectors; $\mathbf{S} = [S_a\ S_b\ S_c]^T$ is the switching state vector of the inverter, and $S_x \in \{2, 1, 0\}$ is the switching state of phase $x \in \{a, b, c\}$. Take A-phase as an example, $S_x = 2$ means that switch $S_a$ and $S_c$ are closed, $S_x = 1$ means that switch $S_b$ and $S_a$ are closed, while $S_x = 0$ means that switch $S_c$ and $S_a$ are closed.

![Figure 1. 3L-NPC-VSI and its load.](image)

3. Proposed Overmodulation Strategy

This section proposes an improved dual-mode overmodulation strategy based on the minimum amplitude error method.

According to Figure 2, the space voltage vector diagram is divided into linear modulation region (LMR), overmodulation region I (OMR-I) and overmodulation region II (OMR-II). The LMR is the inscribed circle of the large regular hexagon of the inverter, and the maximum MI in the LMR is 0.866. The maximum MI in the OMR-I is determined by the voltage-area equivalence. The amplitude of the voltage vector within the boundary of the hexagon will increase to compensate for voltage loss caused by overmodulation. The final result is that, in one electrical cycle, the area of the ideal reference voltage vector circle is equal to the area enclosed by the corrected voltage vector. Therefore, the maximum MI satisfying the voltage-area equivalence principle is 0.909. The maximum MI in the OMR-II is 0.955, which is limited by the fundamental voltage output capability of the inverter.

As shown in Figure 2, the LMR, the OMR-I and the OMR-II corresponds to the MI range [0, 0.866], [0.866, 0.909] and [0.909, 0.955], respectively.
According to the MI of reference voltage vector, the region where the reference voltage vector is located is determined. When the reference voltage vector $u_{\text{ref}}$ is located in the LMR, the synthesis of voltage vector is based on the nearest three vectors principle.

### 3.2. OMR-I

In this work, when the reference voltage vector is located in the OMR-I ($0.866 \leq MI \leq 0.909$), the voltage defect caused by the overmodulation is compensated by increasing the voltage amplitude. As shown in Figure 3a, the orange arc $S_1$ represents the theoretical reference voltage trajectory, the defect voltage generated by overmodulation causes that the fundamental voltage of the inverter cannot reach the reference voltage amplitude. The defect voltage is compensated by increasing the reference voltage vector circle to $S_2$ according to the area equivalent principle. The blue curve in Figure 3a is the actual reference voltage vector trajectory, which will not cause any voltage loss. The $u'_{\text{ref}}$ in Figure 3 represents the modified voltage vector.

The mathematical relationship between the $MI$ and the $MI'$ of $S_2$ can be expressed as:

$$MI'^2 = \frac{3\sqrt{12 \cdot MI^2 - 9} + 12MI^2\gamma}{2\pi}$$

(3)
However, Formula (3) is a transcendental equation and cannot be solved directly. In this work, piecewise linear fitting is performed on the functional relationship between the\( MI \) and the\( MI^* \), and the expression of\( MI^* \) is obtained as follows:

\[
MI^* = \begin{cases} 
29.855 \times M1^2 - 50.9 \times M1 + 23, & 0.866 < M1 \leq 0.897 \\
126.5 \times M1^2 - 224.233 \times M1 + 100.3, & 0.897 < M1 \leq 0.905 \\
1029 \times M1^2 - 1859 \times M1 + 841, & 0.905 < M1 \leq 0.909 
\end{cases}
\]

(4)

The OMR-I is divided into compensation region and equivalent region according to the angle\( \theta \) in this article. As shown in Figure 3a, S\(_2\) intersects the hexagon boundary at point\( d \), and \( |ed| \) intersects \( S_1 \) at point\( f \), \( |ed| \perp |dh| \). \( |ed| \) is the boundary between the equivalent region and the compensation region. It should be noted that\( \alpha_r \) varies with the\( MI \). When the\( MI \) changes, the\( \alpha_r \) needs to be recalculated to prevent the utilization of DC-bus voltage from dropping. The\( \alpha_r \) can be expressed as:

\[
\alpha_r = \frac{\pi}{6} - \arcsin\left(\frac{|oe|}{2MI}\right)
\]

(5)

Where,

\[
|oe| = \sqrt{4MI^*2 - 3}
\]

(6)

The reference voltage vector\( u_{ref} \) will locate in the compensation region if the angle\( \theta \) satisfies \( 0 \leq \theta \leq \alpha_r \) or \( \pi/3 - \alpha_r \leq \theta \leq \pi/3 \), otherwise in the equivalent region.

3.2.1. Vector Correction of Equivalent Region

In this work, when the reference voltage vector\( u_{ref} \) is located in the equivalent region, the correct rule of\( u_{ref} \) based on minimum amplitude error method. As shown in Figure 3b, the correction rules do not change whether the reference vector\( u_{ref} \) falls inside the hexagon boundary.

If the reference voltage vector\( u_{ref} \) is located outside of hexagon, as shown in Figure 3b, the VSI works in the overmodulation zone. In this case, the VSI is not able to synthesize the reference vector without distortions by using the basic voltage vectors. However, it is still possible to synthesize another reachable voltage vector that has the least distance from the reference vector for a minimum tracking error based on minimum amplitude error method.

According to Figure 3b, it is easy to obtain:

\[
|ab| = \frac{\sqrt{3MI \cdot \cos(\theta) - MI \cdot \sin(\theta)} + \sqrt{3}}{2}
\]

(7)

\[
|ac| = \sqrt{(MI \cdot \cos(\theta) - 1)^2 + (MI \cdot \sin(\theta))^2}
\]

(8)

\[
|bc| = \sqrt{|ab|^2 + |ac|^2}
\]

(9)

where\( \theta \) is the angle of reference voltage vector, as shown in Figure 3b.

The\( M1^* \) of the modified voltage vector\( u_{ref}^* \) can be solved according to the trigonometric function relationship and the Pythagorean theorem accurately. The\( M1^* \) can be expressed as:

\[
M1^* = \sqrt{|bc|^2 - |bc| + 1}
\]

(10)

Similarly, the corrected reference voltage vector angle\( \theta^* \) can be solved by the triangular relationship and be expressed as:

\[
\theta^* = \arctan\left(\frac{\sqrt{3}|bc|}{2 - |bc|}\right)
\]

(11)
3.2.2. Vector Correction of Compensation Region

As shown in Figure 3c, if the reference voltage vector is located in the grey region, i.e., \( 0 \leq \theta \leq \alpha_r \) or \( \pi/3 - \alpha_r \leq \theta \leq \pi/3 \), it will be the compensation region. In this work, the calculation of \( M_\text{I}^* \) is based on Equation (5) to compensate for the voltage loss caused by overmodulation. In the OMR-I, in order to realize the smooth transition of the vector trajectory between the equivalent region and the compensation region, the vector angle \( \theta \) needs to be corrected.

According to Figure 3c, the blue curve represents the actual voltage vector trajectory. \( |ed| \) is the boundary between the equivalent region and the compensation region, and \( |ed| \perp |dh| \). The location of point \( e \) can be determined by the \( M_\text{I} \) and calculated by Equation (6). The \( \text{u}_{\text{ref}} \) represents the reference voltage vector. \( |eg| \) is extended and it intersect with the actual reference voltage trajectory at \( v \). The calculation process of the new angle \( \theta^* \) of the \( \text{u}_{\text{ref}} \) is as follows.

According to Figure 3, it is easy to obtain:

\[
|eg| = \sqrt{M_\text{I}^2 + |oe|^2 - 2M_\text{I}|oe| \cos(\theta)} \tag{12}
\]

\[
|ev| = \frac{|eg|}{R} \tag{13}
\]

where \( R \) represents the similarity ratio between \( \triangle eg s \) and \( \triangle ev t \).

The \( R \) can be expressed as:

\[
R = \frac{M_\text{I} - |oe|}{M_\text{I}^* - |oe|} \tag{14}
\]

In \( \triangle oev \), the new angle \( \theta^* \) can be expressed as:

\[
\theta^* = \arccos\left(\frac{M_\text{I}^* + |oe|^2 - |og|^2}{2M_\text{I}^*|oe|}\right) \tag{15}
\]

Substituting Equations (6), (12), (13) and (14) into Equation (15), the new angle \( \theta^* \) of the reference voltage vector in the compensation region can be obtained.

It is worth noting that the corrected result of reference voltage vector in the common boundary are consistent, so the transition of the reference voltage vector between the two regions is smooth and continuous.

3.3. OMR-II

When the \( M_\text{I} \) exceeds 0.909, the reference voltage vector is located in the OMR-II, the voltage defect caused by the overmodulation cannot be compensated completely similar to OMR-I. Therefore, in order to maximize the utilization of DC-bus voltage, the proposed method divides OMR-II into equivalent region and holding region.

As shown in Figure 4a, take the first sector as an example, the division of the equivalent region and the holding region is based on the holding angle \( \alpha_h \). In order to simplify the calculation of \( \alpha_h \), this paper obtains \( \alpha_h \) by the method of piecewise linear fitting. The \( \alpha_h \) can be expressed as:

\[
\alpha_h = \begin{cases} 
6.702 \times M_\text{I} - 6.09, & 0.909 < M_\text{I} \leq 0.936 \\
12.305 \times M_\text{I} - 11.34, & 0.936 < M_\text{I} \leq 0.953 \\
51.27 \times M_\text{I} - 48.43, & 0.953 < M_\text{I} < 0.955
\end{cases} \tag{16}
\]
When synthesizing virtual vectors, the basic voltage vectors which generate a CMV exceed-
vector will locate in the holding region, otherwise in the equivalent region.

3.3.2. Vector Correction of Equivalent Region

As shown in Figure 4, the correction rule of the reference voltage vector located in
the equivalent region of the OMR-II does not change compared with that in the OMR-I.
The new modulation index $M_I^{*}$ of corrected reference voltage vector can be calculated by
Equation (10) and the new angle $\theta^{*}$ of corrected reference voltage vector can be calculated
by Equation (11).

3.3.2. Vector Correction of Holding Region

In order to ensure the maximum utilization of the DC-bus voltage, the nearest large
basic voltage vector will be kept output when the reference voltage vector is located in
the holding region, as shown in Figure 4a.

In this paper, the working region of the inverter is judged according to the magni-
tude of $M_I$ as shown in Figures 3 and 4. It is worth noting that in the overmodulation
strategy proposed in this paper, the $M_I$ is calculated by the reference voltage according to
Equation (1), and $\theta$ depends on estimation or measurement.

4. NP Voltage Balance and CMV Suppression

In this section, a virtual space vector method considering NP voltage balance and
CMV suppression is introduced. The small virtual vector and medium virtual vector can be
constructed by three adjacent basic vectors [22].

As shown in Figure 5a, the 3L-NPC-VSI has a total of 27 basic switching states vectors.
When synthesizing virtual vectors, the basic voltage vectors which generate a CMV exceed-
ing $V_{dc}/6$ are not used [27]. Therefore, the small virtual vector $V_{VS1}$ and $V_{VS2}$ constructed
by three adjacent small basic vectors with a low CMV (CMV $\leq V_{dc}/6$) can be expressed as:

$$V_{VS1} = \frac{1}{3}V_{(110)} + \frac{1}{3}V_{(110)} + \frac{1}{3}V_{(110)}$$  \hspace{1cm} (17)

$$V_{VS2} = \frac{1}{3}V_{(211)} + \frac{1}{3}V_{(110)} + \frac{1}{3}V_{(121)}$$  \hspace{1cm} (18)
The medium virtual vector $V_{VM1}$ constructed by three adjacent basic vectors with a low CMV can be expressed as:

$$V_{VM1} = \frac{1}{3}V_{(120)} + \frac{1}{3}V_{(210)} + \frac{1}{3}V_{(201)}$$  \hspace{1cm} (19)

The average value of the NP current of $V_{VS1}$, $V_{VS2}$ and $V_{VM1}$ in one switching cycle can be expressed as:

$$i_{VS1} = \frac{1}{3}(-i_b - i_c - i_a) = 0$$  \hspace{1cm} (20)

$$i_{VS2} = \frac{1}{3}(-i_a - i_c - i_b) = 0$$  \hspace{1cm} (21)

$$i_{VS1} = \frac{1}{3}(i_a + i_b + i_c) = 0$$  \hspace{1cm} (22)

where $i_a$, $i_b$ and $i_c$ represent the NP current produced by the fundamental voltage vector participating in the synthesis of virtual vector [23].

According to Equations (20)–(22), the constructed virtual vectors with zero NP current does not affect the NP voltage. Figure 5b shows the division of the virtual space vector diagram considering NP voltage balance and CMV suppression.

5. Simulation and Experimental Results

The effectiveness of the proposed method has been validated using the simulation studies in the MATLAB/Simulink. The experimental test bench of the 3L-NPC-VSI with RL load is built to verify the proposed method. The parameters of 3L-NPC-VSI with RL load are listed in Table 1.

Table 1. Parameters of the 3L-NPC-VSI.

| Parameters                   | Values |
|------------------------------|--------|
| DC-bus voltage $V_{dc}$      | 540 V  |
| DC-bus capacitors $L_{c1}$, $L_{c2}$ | $2100 \times 10^{-6}$ F |
| Output resistance $R$        | 8 Ω    |
| Output inductance $L$        | 23 mH  |
| Switching frequency $f_s$    | 5 kHz  |
| Parasitic capacitance        | 10 nF  |
5.1. Simulation Results

5.1.1. NP Voltage Balance and CMV Suppression

Figure 6 shows the simulation results of proposed strategy in the LMR \((0 < MI < 0.866)\). Figure 6 shows the simulation results when the \(MI\) is equal to 0.3 and 0.8, respectively. From top to bottom are the a-phase current \(i_a\) (p.u.), output voltage, NP voltage and CMV.

![Figure 6](image)

**Figure 6.** Output characteristics in the simulation (a) \(MI = 0.3\); (b) \(MI = 0.8\).

According to Figure 6, when the reference voltage vector is located in the LMR, the CMV of the 3L-NPC-VSI with RL load is suppressed effectively, and its peak-to-peak value is equal to 180 V. At the same time, the voltage of the upper and lower capacitors on the DC-bus also achieves excellent balance effect.

The simulation results of leakage current and CMV when the \(MI\) is equal to 0.8 are shown in Figure 7, from top to bottom are the leakage current waveform, the Fast Fourier Transformation (FFT) result of the leakage current, the CMV waveform and the FFT result of the CMV. The traditional SVPWM method and VSVPWM method considering common-mode voltage rejection in [28] are adopted for comparison. As shown in Figure 7a, when the SVPWM method is adopted, the magnitude of the leakage current reaches 400 mA, which fails to comply with the standard level of 300 mA [29]. When the other two methods are adopted, the magnitude of the leakage current is limited effectively within the 300 mA. According to the FFT results of leakage current as shown in Figure 7, the high-frequency components around 5 kHz are slightly reduced compared with the SVPWM method when the VSVPWM method in [28] is adopted. When the VSVPWM method in this paper is adopted, the high-frequency components around 5 kHz are reduced greatly compared with those of the other two methods. This also means that power losses are significantly reduced [33]. Therefore, the power losses can be inferred based on the high-frequency components according to the simulation results. The comparison of different methods is listed in Table 2.
According to the waveforms of the CMV and FFT results of the CMV in Figure 7, both VSVPWM methods achieve CMV suppression effectively. However, the high-frequency components around 5 kHz and 10 kHz are obviously decreased when the VSVPWM method in this paper is adopted. As shown in Figure 7, the FFT results of leakage current and the FFT results of CMV show consistency when the three methods are adopted. In addition, the high-frequency components around 5 kHz in the leakage current spectrum and CMV spectrum are lower than those of the other methods obviously when the VSVPWM method in this paper is adopted.

Figure 7. the simulation results of leakage current and CMV (a) SVPWM; (b) VSVPWM in [28]; (c) VSVPWM in this paper.

Table 2. Leakage current comparison with different methods.

| Method                        | CMV Suppression | $I_{leak}$ | High-Component around 5 kHz | Power Losses |
|-------------------------------|-----------------|------------|------------------------------|--------------|
| SVPWM                         | No              | 410 mA     | high                         | high         |
| VSVPWM in [28]                | Yes             | 199 mA     | medium                       | high         |
| VSVPWM in this paper          | Yes             | 200 mA     | low                          | medium       |

According to the waveforms of the CMV and FFT results of the CMV in Figure 7, both VSVPWM methods achieve CMV suppression effectively. However, the high-frequency components around 5 kHz and 10 kHz are obviously decreased when the VSVPWM method in this paper is adopted. As shown in Figure 7, the FFT results of leakage current and the FFT results of CMV show consistency when the three methods are adopted. In addition, the high-frequency components around 5 kHz in the leakage current spectrum and CMV...
spectrum are lower than those of the other methods obviously when the VSVPWM method in this paper is adopted.

5.1.2. Improvement of DC-Bus Voltage Utilization

The overmodulation strategy mentioned in [18] is a classic overmodulation strategy based on the minimum amplitude error method, which is called the conventional overmodulation strategy in this article. Its defect is that the utilization of DC-bus voltage will be decreased when the reference voltage vector is located in the OMR-I. The overmodulation strategy proposed in this paper improves this deficiency.

A new correction method for the reference voltage vector located in the OMR-I is proposed. It is worth noting that when the MI exceeds 0.909, there is no difference in the correction rule between conventional overmodulation strategy and proposed strategy.

Figure 8 shows the α-axis voltage correction waveforms in an electrical cycle of the conventional overmodulation method and the proposed strategy in this paper when the MI is equal to 0.9. Figure 9 shows the magnitude of the reference voltage vector after correction in an electrical cycle. It can be seen that the curve part is the amplitude of equivalent voltage vector based on the minimum amplitude error method. Meanwhile, the voltage vector operates on the hexagonal boundary, and the minimum voltage vector amplitude is 311 V. According to Figure 9, the maximum amplitude of corrected voltage vector is 324 V when the conventional overmodulation strategy is adopted. However, when the proposed strategy is adopted, the maximum amplitude of corrected voltage vector is 334 V. It can be seen that the higher utilization of DC-bus voltage has achieved when the proposed method is adopted.

![Figure 8](image1.png)

Figure 8. Comparisons of the α-axis voltage amplitude (a) conventional strategy; (b) proposed strategy.

![Figure 9](image2.png)

Figure 9. Comparisons of the amplitude of corrected voltage vector (a) conventional strategy; (b) proposed strategy.
According to Figures 11 and 12, the experimental results verify the effect of the method in the VSVPWM method in [28] and 295.7 W for the SVPWM method when the output current is increased to 30 A. Therefore, the power loss of the proposed method is 5.7% less than that of the conventional VSVPWM and 24.8% less than that of the SVPWM.

The effectiveness of the proposed overmodulation strategy based on minimum amplitude error and considering NP voltage balance and CMV suppression is verified on a 3L-NPC-VSI platform. The DC-bus voltage is set to 540 V. The proposed overmodulation algorithm is implemented on a TMS320F28335 DSP. The PWM frequency is set to 5 kHz.

Figure 11 presents the experimental results of the proposed method in the LMR, from top to bottom are the voltage \(V_{ab}\), voltage \(V_{ao}\), output a-phase current \(i_a\), CMV and CMV spectrum. Figure 11a,b shows the experimental results when the MI is equal to 0.3 and 0.8, respectively. Figure 12 presents the experimental results of the proposed method in the OMR-I and OMR-II, from top to bottom are voltage \(V_{ab}\), voltage \(V_{ao}\), output a-phase current \(i_a\), CMV and CMV spectrum. Figure 12a,b shows the experimental waveforms when the reference voltage vector is located in the OMR-I (MI = 0.9) and OMR-II (MI = 0.95), respectively. The amplitude of CMV is suppressed effectively when the proposed method is adopted, as shown in Figures 11 and 12. According to the CMV spectrum shown in Figures 11 and 12, as the MI increases, the high-frequency components of CMV increases. Compared with the results shown in Figure 7c, the FFT results of CMV are same basically. According to Figures 11 and 12, the experimental results verify the effect of the method in this paper on the suppression of the CMV, the reduction of leakage current and the validity of the proposed overmodulation strategy.

Figure 13 shows the power losses of the 3L-NPC-VSI with the SVPWM, VSVPWM in [28] and VSVPWM in this paper, where the output current varies from 5 to 30 A. The power losses for the VSVPWM method in this paper is 237 W while it is 250.6 W for the VSVPWM method in [28] and 295.7 W for the SVPWM method when the output current is increased to 30 A. Therefore, the power loss of the proposed method is 5.7% less than that of the conventional VSVPWM and 24.8% less than that of the SVPWM.

5.2. Experimental Results

Figure 10 shows the comparison of RI by the conventional strategy versus the proposed strategy when MI increases from 0.866 to 0.909. The RI can be expressed as:

$$RI = \frac{S_{\text{corrected}}}{S_{\text{fundamental}}}$$

where \(S_{\text{corrected}}\) is the area of the region enclosed by the corrected voltage vector trajectory in one electrical cycle; \(S_{\text{fundamental}}\) is the area enclosed by the voltage vector trajectory when the MI is equal to 0.866.

According to Figure 10, the RI increases with the MI. When the MI is equal to 0.909, the RI of the proposed strategy is 1.1, which increases by 3.77% compared with the conventional strategy. Notably, this illustrates the improved utilization of the DC-bus voltage.
Figure 11. Experimental results of the proposed method in the LMR (a) \( MI = 0.3 \); (b) \( MI = 0.8 \).

Figure 12. Experimental results of the proposed method in the OMR (a) OMR-I, \( MI = 0.9 \); (b) OMR-II, \( MI = 0.95 \).

Figure 13. Power losses under various output current.
Figure 14 shows the efficiency comparison among the SVPWM, VSVPWM in [28] and VSVPWM in this paper under different output current, in which the input power is calculated by multiply DC-bus voltage with current. Then efficiency is calculated by the ratio of input power and output power. When output current ranges from 5 to 30 A, the SVPWM has the lowest efficiency due to high leakage current. The VSVPWM method in this paper has the highest efficiency, which is followed by conventional VSVPWM method. This is because the high-frequency components around 5 kHz are greatly reduced compared with those of the other two methods when the VSVPWM method in this paper is adopted.

![Figure 14](image_url)

**Figure 14.** Efficiency comparison between the SVPWM, VSVPWM in [28] and VSVPWM in this paper.

6. Conclusions

This paper discusses the implementation details of the proposed overmodulation strategy considering the NP voltage balance and CMV suppression. In order to improve the utilization of DC-bus voltage, an improved overmodulation strategy based on the minimum amplitude error method for a 3L-NPC-VSI is proposed. Compared with the conventional overmodulation strategy based on the minimum amplitude error method, the utilization of the DC-bus voltage is increased. The VSVPWM method is adopted for the balance of NP voltage and the suppression of CMV. The leakage current is also limited effectively within the standard value according to the simulation results. Eventually, experimental and simulation results verify the effectiveness of the proposed method.

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