Abstract—The rise of new dc technologies is pushing the development of highly efficient dc-dc converters, especially at high voltage and high step ratio. Modular multilevel converters (MMCs) are an attractive alternative because they can manage medium and high dc voltages with standard semiconductor devices with high efficiency if they employ soft-switching techniques. However, the latest soft-switching techniques have been proposed for fixed voltage range, limiting their operation. This paper proposes a soft-switching modulation for the high step ratio Modular Multilevel dc-dc Converter in extended voltage range. The proposal achieves zero-current switching and regulates the voltage balance among the floating cell capacitors, while using a simple control scheme to regulate the output voltage. The theoretical analysis has been verified with full-scale simulations, demonstrating excellent dynamic response and reduced rms current.

Index Terms—dc-dc conversion, modular multilevel converter, high step ratio conversion, triangular current mode, trapezoidal current mode.

I. INTRODUCTION

The latest developments in power electronics have allowed the rise of new technologies and the resurgence of dc power systems, due to their increased use in HVDC transmission systems [1], photovoltaic solar power [2], offshore wind farms [3], battery energy storage systems [4], data centers [5], electric vehicles [6] and fast chargers [7]. In this scenario, the dc-dc converters are the enabling technology for the development of the new electrical infrastructure and the establishment of dc grids.

For high power, the front-to-front Modular Multilevel Converter (MMC) [8] stands out for its modularity and flexibility. This solution provides bidirectional operation thanks to the two MMCs and galvanic isolation due to the medium-frequency transformer at the ac-link. However, the hard-switching operation dramatically increases the power losses. For this, resonant topologies [9] has been proposed for high step voltage ratio. These topologies are composed of a resonant tank, which is excited by a square wave voltage at the resonant frequency to achieve soft-switching. Thus, control through the variation of the operating frequency allows to control the transferred power, but it limits soft-switching range, and consequently a high-efficient operation.

Alternatively to the resonant operation, trapezoidal/triangular current modulations (TCM) approaches are presented in [10], [11]. TCM achieves the balance of the voltages among cell capacitors and maintains the soft-switching without resonance. However, the proposed works assume fixed voltages at input and output ports, limiting the analysis to a specific operation point.

This paper proposes a zero-current switching (ZCS) modulation for the high step ratio Modular Multilevel dc-dc Converter, extending TCM to a variable output voltage operation and a flexible stack modulation. The proposed modulation method achieves ZCS and maintains the voltage balance among the cell capacitors over a wide voltage range. The proposal has been verified with full-scale simulations.

II. HIGH STEP RATIO MODULAR MULTILEVEL DC-DC CONVERTER

The topology of the high step ratio dc-dc MMC is formed by a stack of $N$ half-bridge cells which support the high-voltage port $V_{HV}$, while an active full-bridge converter connects the low-voltage port $V_{LV}$, as is shown in Fig. 1. Both subsystems are connected through an inductor $L$ generating an ac low-voltage link. The converter achieves high-step voltage ratio without the need for a transformer; however it could be added to provide galvanic isolation and additional voltage gain. Furthermore, filters are placed at both sides to decrease voltage and currents ripple, but these are not considered in the following work due to their null impact in the modulation analysis.
The current through the inductor is controlled by the voltages $v_{L1}$ and $v_{L2}$ following (1). The voltage $v_{L1}$ is the difference between the high-voltage $V_{HV}$ and the total voltage in the stack $v_{stack}$, given by the sum of the half-bridges output voltages $v_i$. Thus, $v_{stack}$ is controlled by the switching states of each cell $S_{i \in \{1,0\}}$. On the other hand, $v_{L2}$ is determined by the full-bridge switching state and the low-voltage $V_{LV}$. The inductor current $i_L$, the commutation state $S_{i \in \{1,0\}}$ and the capacitance $C_i$ of each cell capacitor defines the capacitor voltage waveform $v_{ci}$ in each half-bridge cell (2), determining their ripple, mean value and dynamic behaviour.

$$L \frac{di_L}{dt} = v_{L1} - v_{L2} \quad (1)$$

$$C_i \frac{dv_{ci}}{dt} = i_L \cdot S_{i \in \{1,0\}} \quad (2)$$

If it is assumed that the cells have the same capacitance $C$, their capacitors are controlled to the desired value $V_C^*$ and neglecting internal losses, the relationship between the capacitor voltages and the total stack power $P_{stack}$ yields to

$$C \sum_{i=1}^{N} v_{ci} \approx \frac{P_{stack}}{V_C^*} \quad (3)$$

Therefore, the current across the inductance $L$ is controlled by the difference of the voltages $v_{L1}$ and $v_{L2}$ at each side of it in order to control the power flow between both ports. Finally, the direction and magnitude of power is controlled directly with the inductor current.

III. ASYMMETRICAL TRAPEZOIDAL CURRENT MODE

The trapezoidal current mode requires that the voltages $v_{L1}$ and $v_{L2}$ be precisely time coordinated. The full-bridge works with unipolar modulation, generating an asymmetrical square waveform $v_{L2}$ defined by the transition times $(t_2, t_4, t_6, t_8)$ in a period $T_s$, as is shown in (4).

$$v_{L2}(t) = \begin{cases} V_{LV} & t_2 \leq t \leq t_4 \\ -V_{LV} & t_6 \leq t \leq t_8 \\ 0 & 	ext{Otherwise} \end{cases} \quad (4)$$

On the other hand, $v_{L1}$ is a three-level voltage defined by the commutation times $(t_1, t_3, t_5, t_7)$, if a proper three-level modulation is applied to the $v_{stack}$ and all the capacitor voltages in the cells are balanced and equal to $V_C$. If the stack modulation is centered in $N_o$ cells and the voltage amplitude is generated by $N_o$ cells, the stack voltage $v_{stack}$ can be expressed as

$$v_{stack}(t) = \begin{cases} (N_o - N_a) V_C & t_1 \leq t \leq t_3 \\ (N_o + N_a) V_C & t_5 \leq t \leq t_7 \\ N_o \cdot V_C & 	ext{Otherwise} \end{cases} \quad (5)$$

Therefore, $v_{L1}$ is a three-level centered on zero voltage if (6) holds and the high-voltage Kirchhoff’s loop is considered ($v_{L1} = V_{HV} - v_{stack}$).

$$V_C = \frac{V_{HV}}{N_o} \quad (6)$$

Thus, the stack modulation defines the step-down voltage ratio $r_S$ (7) between the maximum ac-link voltage $\hat{v}_{L1}$ and the high-voltage $V_{HV}$.

$$r_S = \frac{\hat{v}_{L1}}{V_{HV}} = \frac{N_o}{N_o} \geq \frac{1}{N - 1} \quad (7)$$

The highest voltage step conversion is achieved when this ratio is minimized (with $N_o = 1$ and $N_o = N - 1$), considering...
the restrictions of minimum number of cells feasible for the modulation ($N_a \geq 1$) and the maximum limit of N cells available ($N_0 + N_a \leq N$). However, it is possible to adjust $N_a$ and $N_0$ to different values for voltage reconfiguration, redundant operation or in case of failure in any cell.

The voltage balance among cells can be achieved through a sorting modulation or a time-controlled phase-shift modulation [10]. The phase-shift modulation waveforms for each cell are illustrated in Fig. 2, taking $N = 5$ and the highest voltage stack conversion as an example.

Considering the previous stack modulation, a trapezoidal current through the inductor could be generated by managing the commutation times $t_i$ as is shown in Fig.3(a) and it achieves ZCS for half of the commutations ($t_1, t_4, t_5$ and $t_8$) if

$$D_{i+1} \cdot r_V = D_i \quad i = 1, 3$$

(8)

with the duties cycles $D_i$ defined as in Fig.3(a) and

$$r_V = \frac{V_{LV}}{V_{HV} \cdot r_S}$$

(9)

The ac link voltage ratio $r_V$ represents the ratio between the amplitude of the voltages at both sides of the inductor ($v_{L1}$ and $v_{L2}$) and it needs to be $r_V = 1$ for a perfect trapezoidal current. However, in the following analysis it is considered as a parameter for a general operation.

IV. DYNAMIC BALANCE OF POWER

To modeling exchange of power between the high-voltage port, the low-voltage port and the cell stack, the area covered for the inductor current in the positive ($A^1_{TRAP}$) and negative ($A^2_{TRAP}$) cycles of the switching cycle $f_s$ are illustrated in Fig. 3 (a). These areas can be defined as function of the phase shift $\Phi_i$ and the cycle $D_i$ (10), if the ZCS condition (8) holds.

$$A^1_{\Delta} = \int_{t_1}^{t_4} i_L \cdot dt = \frac{V_{HV} \cdot r_S}{2 f_s L} \left(2D_1 \Phi_1 + D_2^2 \left(\frac{1}{r_V} - 1\right)\right)$$

$$A^2_{\Delta} = \int_{t_5}^{t_8} i_L \cdot dt = -\frac{V_{HV} \cdot r_S}{2 f_s L} \left(2D_3 \Phi_2 + D_3^2 \left(\frac{1}{r_V} - 1\right)\right)$$

(10)

The average power delivered by the high-voltage port at one switching cycle $P_{HV}$ is determined by the high voltage $V_{HV}$ and the sum of the areas $A^1_{TRAP}$ and $A^2_{TRAP}$ due to the inductor current waveform is the same as in the high-voltage port if filters are not considered. The expression for the high-voltage power $P_{HV}$ is shown in (11) using the relation (10).

$$P_{HV} = \frac{V_{HV}^2 \cdot r_S^2}{2 f_s L} \left(2D_1 \Phi_1 - 2D_3 \Phi_2 + (D_1^2 - D_3^2) \left(\frac{1}{r_V} - 1\right)\right)$$

(11)

From (11), the high-voltage average power $P_{HV}$ is null with symmetric operation ($D_1 = D_3$ and $\Phi_1 = \Phi_2$), leading to a non-feasible operation. Therefore, the asymmetrical operation is a requirement to achieve a steady-state power balance between ports. On the other hand, the average power in the low-voltage port at one switching cycle $P_{LV}$ is determined in (12), using the same method.

$$P_{LV} = \frac{V_{LV}^2 \cdot r_S^2}{2 f_s L} \left(2D_1 \Phi_1 + 2D_3 \Phi_2 + (D_1^2 + D_3^2) \left(\frac{1}{r_V} - 1\right) - \Phi_1^2 - \Phi_2^2\right)$$

(12)

Thus, it is possible to control the power transfer between high-voltage and low-voltage ports through (11) and (12), keeping the voltage balance in the capacitors. The steady state balance is achieved if it is imposed that the powers remain identical at both sides of the converter without considering the power losses ($P_{HV} = P_{LV}$), and the difference between these powers allows to charge or discharge the capacitors. A similar analysis can be performed for negative power flow inverting the phase-shift of voltages $v_{L1}$ and $v_{L2}$ ($\Phi_1$ and $\Phi_2$) as is illustrated in Fig. 3 (b). Therefore, these relationships allow full bidirectional control of the power flow maintaining the ZCS.
and voltage balance in the converter. The trapezoidal current mode provide a set of general solutions \((\Phi_1, \Phi_2, D_1, D_3)\) for a specific power transfer, which has two degrees of freedom. Thus, an optimisation problem can be defined for a given state to find the best solution from all feasible alternatives.

V. OPTIMIZATION

Because the soft-switching operation of the trapezoidal current mode naturally leads to reduced switching losses, the minimisation of the conduction losses rises as an attractive objective of the optimisation problem in order to reduce the total power losses and to achieve high efficient operation. Thus, the optimization problem is set to minimise the square of the rms inductor current per-unit \(i_{L,p}^{rms}\), due to the conduction losses of the passive elements and devices are proportional to the square of this rms current. The derivation of this rms inductor current per-unit as function of \((\Phi_1, \Phi_2, D_1, D_3, r_v)\) yields to (13), considering the current base as \(I_{base} = \frac{V_{DC}}{3fHV}\).

\[
i_{L,p}^{rms} = 12 \left( \frac{(r_v-1)^2}{3r_v} (D_1^3 + D_3^3) - \frac{r_v}{3} (\Phi_1^3 + \Phi_2^3) + r_v \left( \Phi_1 D_1 (\frac{1}{r_v} - 1) + \Phi_2 D_3 (\frac{1}{r_v} - 1) \right) \right)^{0.5}\]

(13)

Since the rms inductor current \(i_{L,p}^{rms}\) is nonlinear, a non-linear optimisation problem (NLP) is defined in (14) to find the optimal solution \((\Phi_1, \Phi_2, D_1, D_3)^{opt}\) which produce the minimal conduction losses. The constraints of this optimisation problem are the power conditions and the feasible range of the solution. The power constraints are defined by the power references \(P_{HV,p}^{*}\) and \(P_{LV,p}^{*}\) required for the power balance between ports, whilst the set of possible solutions are restricted to positive solutions and fitted to the maximum time-window \(T_s\).

\[
\begin{align*}
\min_{\Phi_1, \Phi_2, D_1, D_3} & \quad J = (i_{L,p}^{rms})^2 \\
\text{subject to} & \quad P_{HV,p} = P_{HV,p}^{*} \\
& \quad P_{LV,p} = P_{LV,p}^{*} \\
& \quad \Phi_1 + \Phi_2 + \frac{D_1}{r_v} + \frac{D_3}{r_v} \leq 1 \\
& \quad \Phi_1, \Phi_2, D_1, D_3 \geq 0
\end{align*}
\]

(14)

This NLP is numerically solved in MATLAB using an interior point algorithm [12] for a wide range of the parameters \((r_v, r_S)\) and power references. Thus, a lookup table can store the optimised results for future utilization and comparison.

A. Analytical approach at steady-state with \(r_v \approx 1\)

A significant analysis of the NLP problem is required to explain their results due to the solution of the problem is highly dependent on \(r_v\). Thus, an analytic approach to the NLP problem is subsequently made for some representatives cases.

For the case \(r_v \approx 1\), the problem of minimise \((i_{L,p}^{rms})^2\) is equivalent to the minimisation of \(\Phi_1 + \Phi_2\) or the maximisation of \(D_1 + D_2\), as is demonstrated in [11]. This can be interpreted as the minimising problem of \((i_{L,p}^{rms})^2\) is equivalent to the maximising of the current utilization in the time-window \(T_s\). If the current does not fit the entire time-window (Fig. 3 (a)), this pulsating current generate higher rms inductor current than an equivalent current which utilize the full time-window (Fig. 4 (c)). Therefore, the solution of the NLP is allocated in the superior limit of the inequality constriction for \(D_1\) and \(D_3\). Thus, it is possible to find the optimized solution if this constraint is considered as equality. Hence, the power function per-unit \(P_{pu}\) can be found as a function dependent of \(\Phi_1\) and \(\Phi_2\), solving the system of equations (15) which considers the steady-state constriction \((P_{HV,p}^{*} = P_{LV,p}^{*} = P_{pu}\)) and the time-window maximisation.

\[
\begin{align*}
P_{HV,p} &= P_{pu} \\
P_{LV,p} &= P_{pu} \\
\Phi_1 + \Phi_2 + \frac{D_1}{r_v} + \frac{D_3}{r_v} &= 1
\end{align*}
\]

(15)

The power function \(P_{pu}\) which solves (15) is illustrated in Fig. 4 (a) considering the more straightforward case to analyze \((r_v = 1)\) and \(r_S = 1/9\) as example. The contours lines of this surface and the numeric solutions of the NLP for different power references \(P_{pu}^{*}\) are shown in Fig. 4 (b), confirming that the optimal solution is allocated in these contours lines. The comparison of three feasible solutions for a reference of power \(P_{pu}^{*} = 0.8\) is shown in Fig. 4 (c) to illustrate the negative impact on the inductor current of the non-optimal solutions (cases 1 and 2). From Fig. 4 (b), the NLP numerical solutions are allocated near the curve \(\Phi_1 = \Phi_2\). Thus, if the approximation \(\Phi_1 = \Phi_2\) is imposed, the optimal power function can be simplified to

\[
P_{pu,\Phi_2=\Phi_1} = 12 \cdot \Phi_1 (1 - 3\Phi_1).
\]

(16)

The maximum power transfer for this case is shown in (17), noticing that it is obtained at \(\Phi_1 = 1/6\). Also, this maximum power is considered as the power base per-unit \(P_{base}\) for all power expression in per-unit.

\[
P_{base} = \frac{V_{HV}^2 \cdot r_S}{12fL}
\]

(17)

A similar analysis can be performed for the case \(r_v < 1\). Following the same idea, it is possible to find a power function dependant of \(\Phi_1\) and \(\Phi_2\). The contours lines of the power function per-unit surface and the numeric solutions of the NLP for different power references \(P_{pu}^{*}\) are shown in Fig. 5 (a) for the case \(r_v = 0.85\). As in the previous case, the NLP numerical solutions are allocated near the curve \(\Phi_1 = \Phi_2\), allowing simplify the problem.

However, there is a limit for the power range which is possible to find feasible solutions using the contours lines. The new superior limit of this power range is determined by the limitation of the parameter \(r_v\) due the power is almost proportional to \(r_v\), as can be seen in (12). This limit case is illustrated in Fig. 5 (c) considering \(r_v = 0.85\) and...
$r_S = \frac{1}{9}$ as example, generating a maximum power transfer of $P^* = 0.844$. On the other hand, the inferior limit is achieved when the current is no longer trapezoidal at $\Phi_1 = 0$ and $P^* = 0.326$. At this limit case (Fig. 5 (b)) the current starts to be triangular, enabling the asymmetric triangular current mode (ATCM) with $r_V < 1$ for power references lower than the inferior limit [13]. Thus, ATMC is able to modulate through the duty cycle beyond this limit if the time-window restriction (15) is released. Furthermore, the ATCM is also the solution of the NLP problem, achieving the minimal rms inductor current in this power range.

The analysis for the case $r_V > 1$ is similar. The contours lines of the power function per-unit surface and the numeric solutions of the NLP for different power references $P_{pu}^*$ are shown in Fig. 6 (a) for the case $r_V = 1.15$. As in the previous case, the NLP numerical solutions are allocated near the curve $\Phi_1 = \Phi_2$, and the limit cases are illustrated in Fig. 5 (b)(c). The inferior limit for the power $P_{pu}$ is achieved when the current is no longer trapezoidal at $P^* = 0.392$. At this limit case (Fig. 6 (b)) the current starts to be triangular, enabling the asymmetric triangular current mode (ATCM) with $r_V > 1$ for power references lower than this limit.

Therefore, trapezoidal and triangular current modes are complementary modes for an optimized modulation. This general approach allows incorporate ATCM in the analysis, noticing that the ATCM are particular cases of the trapezoidal current mode when some conditions are achieved. The ATCM waveforms for both cases are shown in Fig. 7, noticing that the ATCM is a particular case of the trapezoidal current mode when $\Phi_1 = \Phi_2 = 0$ for $r_V < 1$ or $\Phi_1 = D_1 - D_2$ and $\Phi_2 = D_3 - D_4$ for $r_V > 1$.

Thus, it is possible to create a control map (Fig. 8 (a)) for a wide $r_V$ range. This map defines three complementary modes: trapezoidal, triangular $r_V < 1$ and triangular $r_V > 1$ if the previous analysis of the power range in term of $r_V$ is extended for the interval (0,2). The set of steady state equations for the per-unit power $P_{pu}$ considering this three different modes are summarized in the Table I. These equations allow to obtain the optimized operation point $(\Phi_1, \Phi_2, D_1, D_3)$ for each power reference $P_{pu}^*$.

**B. Control scheme**

Fig. 8 (b) shows the proposed control scheme, which can be implemented with two control-loops for the output voltage $V_{LV}$ and the mean value of the stack capacitor voltages $V_C$. To regulate the output voltage, a PI controller is considered due to the linear relation between the power $P_{LV}$ and the output voltage $V_{LV}$ given by the output filter. The mean value of the stack capacitor voltages $V_C$ is also controlled through a PI controller, which set the power in the stack to keep this voltage in the required value $V_{C}^*$ of the stack modulation.
controller tuning can be done considering the plant presented in (3).

The parameter \( r_V \) is calculated using the equation (8) and \( r_S \) is determined by the stack modulation. Both parameters plus the power references \( P_{LV}^* \) and \( P_{HV}^* \) define the NLP problem to minimise the rms inductor current, which is solved by the NLP solver block in order to calculate the duty cycles. This NLP solver block could be implemented as a look-up table that stores the results of the optimisation problem previously solved offline or as a set of equations (Table I) and the control map which select the operation mode at steady-state.

The voltage balance among cells is achieved through a time-controlled phase-shift modulation [10], which is implemented in the modulation block.
Fig. 7. Current and voltage waveforms for converter under ATCM with: (a) \( r_V < 1 \). (b) \( r_V > 1 \).

Fig. 8. (a) Control map for \( r_S = \frac{1}{9} \), (b) Control scheme.

VI. RESULTS

The high step ratio MMC dc-dc converter with single-pole configuration is simulated at full-scale, considering the parameters listed in Table II. The NLP solver block of the control scheme is implemented as a set of equations (Table I) and the control map which select the operation mode at steady-state.

Table II

| Description           | Parameter | Value |
|-----------------------|-----------|-------|
| Power rate            | \( P_{\text{base}} \) | 1 MW  |
| HV side Voltage       | \( V_{HV} \) | 10 kV |
| LV side Voltage       | \( V_{LV} \) | 1.1 kV |
| Number of cells       | \( N \)   | 10    |
| Stack voltage ratio   | \( r_S \) | 1/9   |
| Inductor inductance   | \( L \)   | 102 \( \mu \)H |
| Capacitance of cell capacitors | \( C_i \) | 50 mF |
| Output capacitor      | \( C_o \) | 10 mF |
| Output load           | \( R_o \) | 1.3 \( \Omega \) |
| Switching frequency   | \( f_s \) | 1 kHz |
| IGBTs ABB 5SNA3600E17000 | V / I | 1.7 kV / 3.6 kA |

VI. RESULTS

The high step ratio MMC dc-dc converter with single-pole configuration is simulated at full-scale, considering the parameters listed in Table II. The NLP solver block of the control scheme is implemented as a set of equations (Table I) and the control map which select the operation mode at steady-state.

Fig. 9 (a) shows the \( V_{LV} \) step response of the converter emulating a black start operation until reach the output voltage reference \( V_{LV}^* \). The dynamic behaviour of the duty cycles (Fig. 9 (b)) shows a soft response even in the triangular-trapezoidal transition (this transition occurs when \( \Phi_i \) start to be different of zero at \( 19 \) [ms]). Also, the MMC capacitor voltages are balanced even under different capacitance in the cell capacitors, as is shown in Fig. 9 (c). Finally, the ac-link waveforms show the current and voltages at the inductor (Fig. 9 (d)), verifying the reduced rms current operation. The zoomed captures confirm the soft-switching operation of the converter regardless of the value of the output voltage \( V_{LV} \).

The overall simulated efficiency is over 98% at nominal power. The following power losses were taken into account: (i) IGBT conduction losses; (ii) IGBT turn-on and turn-off switching losses; (iii) diode reverse recovery losses; and (iv) diode conduction losses. The power losses in the cells stack at full power represents 81.3% of total losses and are composed mostly by conduction losses (94%) due to the ZCS operation. The power losses in the low voltage full-bridge at full power represent the other 18.7% of total losses and are distributed more evenly between conduction (73%) and switching losses (27%).
VII. CONCLUSIONS

A ZCS modulation for the high step ratio MMC dc-dc converter in a wide voltage operation has been presented. A simple control scheme is proposed to control output voltage, implementing the analytical results of the minimum peak-peak current optimization problem. Theoretical analysis has been verified with full-scale simulations, showing excellent dynamic response and voltage balance under transient conditions. The experimental validation will be carried out over the next few months.

ACKNOWLEDGMENT

The authors acknowledge the financial support provided by ANID/PIA/ACT192013, by ANID/FONDECYT/1171142, by ANID/FONDAP/15110019 (SERC Chile), and the UC Energy Research Center of Pontificia Universidad Católica de Chile.

REFERENCES

[1] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, “Vsc-based hvdc power transmission systems: An overview,” IEEE Transactions on Power Electronics, vol. 24, pp. 592–602, March 2009.

[2] L. Zhang, K. Sun, Y. Xing, L. Feng, and H. Ge, “A modular grid-connected photovoltaic generation system based on dc bus,” IEEE Transactions on Power Electronics, vol. 26, pp. 523–531, Feb 2011.

[3] P. Bresesti, W. L. Kling, R. L. Hendriks, and R. Vailati, “Hvdc connection of offshore wind farms to the transmission system,” IEEE Transactions on Energy Conversion, vol. 22, pp. 37–43, March 2007.

[4] K. Sun, L. Zhang, Y. Xing, and J. M. Guerrero, “A distributed control strategy based on dc bus signaling for modular photovoltaic generation systems with battery energy storage,” IEEE Transactions on Power Electronics, vol. 26, pp. 3032–3045, Oct 2011.

[5] A. Pratt, P. Kumar, and T. V. Aldridge, “Evaluation of 400v dc distribution in telco and data centers to improve energy efficiency,” in INTELEC 07 - 29th International Telecommunications Energy Conference, pp. 32–39, Sep. 2007.

[6] A. Emadi, S. S. Williamson, and A. Khaligh, “Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems,” IEEE Transactions on Power Electronics, vol. 21, pp. 567–577, May 2006.

[7] S. Rivera, B. Wu, S. Kouro, V. Yaramasu, and J. Wang, “Electric vehicle charging station using a neutral point clamped converter with bipolar dc bus,” IEEE Transactions on Industrial Electronics, vol. 62, pp. 1999–2009, April 2015.

[8] T. Luth, M. M. Merlin, T. C. Green, F. Hassan, and C. D. Barker, “High-frequency operation of a dc/ac/dc system for hvdc applications,” IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4107–4115, 2013.

[9] X. Zhang, T. C. Green, and A. Junyent-Ferré, “A new resonant modular multilevel step-down dc-dc converter with inherent-balancing,” IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 78–88, 2014.

[10] C. Pineda, J. Pereda, F. Rojas, C. Cerda, X. Zhang, and A. Watson, “Asymmetrical triangular current mode (atcm) for bidirectional high step ratio modular multilevel dc–dc converter,” IEEE Transactions on Power Electronics, pp. 1–1, 2019.

[11] Y. Qiao, X. Zhang, X. Xiang, X. Yang, and T. C. Green, “Trapezoidal current modulation for bidirectional high-step-ratio modular dc–dc converters,” IEEE Transactions on Power Electronics, vol. 35, pp. 3402–3415, April 2020.

[12] R. H. Byrd, J. C. Gilbert, and J. Nocedal, “A trust region method based on interior point techniques for nonlinear programming,” Mathematical programming, vol. 89, no. 1, pp. 149–185, 2000.

[13] C. Pineda, J. Pereda, X. Zhang, and F. Rojas, “Triangular current mode for high step ratio modular multilevel dc–dc converter,” in 2018 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 5185–5189, IEEE, 2018.