Performance optimization of convolution calculation by blocking and sparsity on GPU

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Abstract—Convolution neural network (CNN) plays a paramount role in machine learning, which has made significant contributions in medical image classification, natural language processing, recommender system and so on. A successful convolution neural network can achieve excellent performance with fast execution time. The convolution operation dominates the total operation time of convolution neural network. Therefore, in this paper, we propose a novel convolution method on Graphic Processing Units (GPUs), which reduces the convolution operation time and improves the execution speed by approximately 2X than the state of the art convolution algorithm. Our work is based on the observation that the sparsity of the input feature map of convolution operation is relatively large, and the zero value of the feature map is redundancy for convolution result. Therefore, we skip the zero value calculation and improve the speed by compressing the feature map. Besides, the shape of the feature map for the deep network is small, and the number of threads is limited. Therefore, for a limited number of threads, it is necessary to reduce the amount of calculation to increase the calculation speed. Our algorithm has a good effect on the convolution operation for the feature map of the deep network with large sparsity and small size.

In this work, our contributions can be summarized as follows: 1) A novel store format for high-sparsity feature map. 2) A novel convolution algorithm based on block compression and shared memory is proposed. 3) A feature map data-set for convolution algorithm optimization. 4) We compared the performance of single-layer convolution with CuDNN for different models, and can achieve 3.5X speedup. We also implemented the algorithm on the VGG-19 model, which can achieve 1.3X~2.9X speedup for convolution layer in deep convolution operation, and the entire network can achieve 2.3X speedup.

Index Terms—Convolution Neural Networks, Graphic Processing Units, Optimization, Sparse, Shared memory, Sparse Matrix-Vector Multiplication

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I. INTRODUCTION

Convolution neural network (CNN) has played a crucial role in machine learning, which facilitated the development of the medical image classification [1], [2], natural language processing [3], [4] and recommender system [5] etc. Improving the execution speed of CNN is of great significance for promoting the development of machine learning. The convolution operation time usually dominates the total execution time. Therefore, the importance of convolution and its huge computation cost demonstrates that we need to optimized for high-performance. The convolution operation in convolution neural network refers to the process in which the convolution kernel samples on the feature map. In the sampling process, the convolution kernel is required to carry out a weighted summation operation on the sampling area, and the entire feature map is sampled according to the stride size. The process of convolution operation requires a lot of multiplication and addition, so optimizing the convolution process is a vital task.

From the hardware perspective, designing an FPGA or ASIC architecture suitable for convolution computation to achieve acceleration is a feasible strategy [6]. Furthermore, Tensor Cores have been incorporated into the new Volta GPU Architecture, which delivers several times of the convolution performance over the previous architecture [7]. From the software perspective, a series of algorithmic level optimization techniques were developed, such as im2col-based method which converted the convolution operation to matrix multiplication [11]. FFT-based method which transforms convolution computation into multiplication computation by frequency domain transformation [9]. Winograd-based method which uses ancient Chinese mathematical methods to reduce the number of multiplication and increase the speed of calculation [10]. Above of these software acceleration methods have been integrated into CuDNN library by NVIDIA, which is state-of-the-art acceleration library for deep learning on GPU [8]. Also, a series of methods to optimize batch and tiling are proposed to accommodate small-scale convolution matrix multiplication
and parallel optimization methods are adapted to GPUs to speedup convolution operation \[13\].

For the traditional optimization method of convolution operation, it is usually designed based on the versatility of the algorithm and does not combine the characteristics and development direction of the deep neural network. Since network pruning operations and RELU activation function operations are joint operations in deep neural networks, which results in a large number of zero values in the network. For the feature map that needs to be calculated for the convolution operation, it can be found in the previous study that the zero value in feature map can achieve a ratio of of 0.7 after multiple epochs of the depth networks. The calculation of these zero values, however, is redundant for the convolution result \[14\].

In other words, if we can skip the zero value calculation in the convolution operation, this will reduce multiplication and addition by 50%. Therefore, for this reason, many efforts have focused on reducing the calculation of zero value in neural networks \[18\], such as SqueezeFlow employs a PTOS-sparse dataflow that removes the ineffective computations while maintaining the regularity of CNN computations \[15\]. SCNN uses a novel data stream that maintains sparse weights and activation with compression coding, eliminating unnecessary data transfers and reducing storage requirements \[16\], \[17\]. proposed a new FPGA hardware architecture that uses algorithmic pre-determined structured sparsity to significantly reduce memory and computational requirements, etc. These efforts have much promoted the acceleration of deep neural networks. However, some work does not apply to all network models, and some work designed new architectures cannot be quickly integrated into existing chips, so there is a limited substantial contribution to the development of deep neural networks. Besides, some computational algorithms for compressing convolutions on the CPU are being proposed \[14\], \[18\], \[19\], \[31\], \[32\], but for general deep neural networks, GPU computing is universal, so it has certain limitations. For the development trend of deep neural networks, the pursuit of precision in deep neural networks leads to dozens of iterations, so the weight in the network and the large sparsity in the feature map are inevitable, so convolution algorithms that can be widely applied through sparse design are feasible.

To solve the above the circumstances, we propose a novel method to accomplish the convolution operation, which based on GPUs to implements multi-threaded computing. Our contributions can be summarized as follows:

- A novel store format for high-sparsity feature map, which makes non-zero values continuous on GPUs.
- Propose a convolution algorithm based on block compression and shared memory, which calculates the convolution by skipping zero and reduces the amount of computation.
- Provides a data-set with multiple common network model feature maps that can be used for convolutional computational optimization research.
- Evaluate the proposed algorithm and compare it with mostly related works on GPUs. The result shows that our method can achieve 3.5X speedup by CuDNN.

The rest of this paper can be organized as follows: Section II presents the background of optimization for convolution operation. Section III introduces the motivation of our convolution method. Section IV describe the details of the proposed method. Section V introduces the new data-set of multiple common network model feature maps and evaluates the proposed method, respectively. Section VI discuss the related work. Section VII concludes this paper.

II. BACKGROUND

In this section, we will introduce the elementary knowledge about GPUs and CUDA platform. Moreover, we also elaborate on some work of convolution operation on GPU.

A. Graphic Processing Units and CUDA platform

As computing demands continue to increase, data is required to be calculated in a limited amount of time, so the demand for parallel computing is also increasing. In turn, the performance requirements of the processor have also been greatly improved. In order to meet the needs of parallel computing, Graphic Processing Units have begun to be used in a large number of data processing industries.

GPU is a Streaming Multiprocessor (SM) array structure, and each SM contains multiple Streaming Processes (SP) \[22\]. Therefore, data can be processed in parallel with multiple SPs. Each SM can access a register file that works at the same speed as the SP \[23\], and accessing its storage unit requires little waiting time. Further, the Fermi architecture, for each SM contains L1-cache, all SMs shared an L2-cache. Each SM has a shared memory that is similar to the cache in the CPU \[24\], but its data replacement is wholly controlled by the engineer, with no corresponding data to replace the hardware logic.

For the SP inside the SM, the shared memory can be accessed, and the access is shared only within the SM. The L1-cache in each SM shares a 64K memory segment with shared memory \[25\]. It is also worth noting that for the number of threads in the SM higher than one, there should be a synchronization mechanism for access to the shared memory to avoid the generation of thread branches \[26\].

Constant memory is a form of virtual address for global memory and is a type of read-only memory that is often limited to 64K. Besides, constant memory also supports broadcasting a single value to each thread in the warp. Global memory is a storage structure for data communication between the GPU and the CPU. The CPU can write to the global memory and access it through the PCI-E bus. However, the global memory access time is limited. It is also a fundamental optimization method to process global memory data and utilize shared memory \[26\], \[27\].

Compute Unified Device Architecture (CUDA) is a computing platform designed by NVIDIA in conjunction with the GPU architecture. Using CUDA platform to develop parallel tasks makes GPU programming more acceptable and promotes the development of parallel tasks. CUDA platform combines threads into a thread network. A thread network consists of multiple thread blocks, each of which shares a shared memory.
Multiple thread blocks can form a grid. Besides, due to the GPU’s characteristics, access to memory is usually in the order of the warp, generally a warp size of 32 threads [26], [27].

B. Convolution operation

The GPU is very mature for the correlation calculation of the matrix. The hardware architecture of the SP array can be used to perform related calculations on the matrix so that the speed required for a specific calculation can be satisfied.

In recent years, convolution calculations have also been converted to matrix multiplication calculations. As shown in Fig. 1, the values in the convolution window are expanded to one row of the matrix, and the convolution kernel is expanded into vectors. In doing so, the convolution calculation is converted to a matrix multiplication calculation, and the value of the matrix multiplication each time the tile is calculated corresponds to a value that the convolution will result in, so that the calculation speed is substantially increased [28], [29].

In recent years, there have been many optimizations for GPUs for convolution in neural networks, which we will discuss in Section VI.

III. Motivation

Convolutional neural networks is an important machine learning tool that extracts the characteristic information of input data through multi-layer convolution. Convolution is a complex task, however, which requires sampling the entire feature map. Wherefore, it requires the convolution kernel to do multiplication operations and addition operations in the sample area, which operate throughout the feature map, so the number of additions and multiplications is enormous. For the size of feature map is \( i_w \times i_h \) and kernel size is \( k_w \times k_h \), a convolution operation of stride is \( s \) requires \((i_w-k_w+1)(i_h-k_h+1)(k_wk_h-1)\) additions and \((i_w-k_w+1)(i_h-k_h+1)(k_wk_h)\) multiplications.

Besides, for the feature map of the depth convolution layer in the deep neural network becomes smaller, and the size of the feature map is usually \( 11 \times 11 \) or \( 5 \times 5 \), etc. Since GPUs computing convolution calculation generally converted into matrix multiplication, the number of threads is small due to the limited size of the feature map, and the GEMM also has limited effect on small matrix multiplication.

As mentioned in section I, the sparsity of the deep feature map is relatively large due to the existence of RELU activation and pruning operations. We can see from Fig. 2, the sparsity of the feature map that will enter the convolution layer can reach more than 0.7 in the deep network. When converted to matrix multiplication, the calculated matrix is more sparse. The usual calculation method will calculate these zero values, which is redundant for the final convolution result. In other word, the useless calculations will account for more than 70%, so we need to avoid this part of the calculation.

To address the above challenges, we reduce the multiplication and addition operations in the convolution operation by compressing the feature map. In order to reduce the time consumption in the compression process, we transform the traditional matrix conversion operation into a compression operation. After compression, the convolution calculation is converted into sparse matrix-vector-multiplication calculation (SpMV) [21], which reduces the calculation of redundant zero values.

The convolutional compression process increases the consumption of memory access. We limit the time consumption by partitioning ideas and rational allocation of shared memory and designing new storage formats. The details are described in detail in section IV.

IV. Proposed Convolution Method

In this section, we will introduce our convolution method for convolution neural network. In two subsections. The first subsection describes an innovative feature map storage format suitable for GPUs computing, under the design characteristics
of the convolution calculation. In the second subsection, we will describe our calculation algorithm in detail.

A. Novel storage format for GPUs computing

Converting the feature map used for the convolution operation into matrix that can be used for the sparse matrix multiplication operation requires format conversion of the original feature map. However, the traditional sparse matrix storage format is not suitable for data storage of convolution operations, such as [19] work done is converted to CSR format, which consumes many times accessing global memory. Therefore, we designed a sparse storage format for feature maps for GPUs computing.

In contrast to the CSR storage format, we reduce the storage of useless data index values and store the values of the convolution kernel that are useful for convolution results. In this way, the storage format stores only its non-zero value for the feature map, which reduces 50% accesses to global memory. Besides, the number of calculations required for each thread is specified based on the value in $\text{Ptr}$. If there is no non-zero value in a thread, it should be stored as $-1$ for markup.

In the process from the feature map to sparse memory map, the number of memory accesses is increased. Theoretically, the conversion time is increased. Therefore, we use the method of blocking and shared memory in the algorithm to reduce time consumption. Blocking is primarily used to improved data locality by enhancing the reuse of data in GPUs. Each block corresponds to a thread block on the GPUs. The resources in the block are shared, and the threads in each thread block correspond to a convolution window. The feature map in global memory is downloaded into the sparse memory matrix in the shared memory of the block. Improve the access speed, and the non-zero value is continuous, increase the locality, and facilitate the use of the next calculation.

As shown in Fig. 4, To reduce to access memory time in the calculation, we load the non-value of feature map to shared memory. Feature map is stored in global memory as a single array for continuous access by adjacent threads. However, this advantage is only limited to when the convolution stride is 1.

For a single feature map, you need to allocate $\frac{i_k - k_i}{s_i} + 1$ blocks, which contain $\frac{i_s - s}{s} + 1$ threads. In the algorithm implementation, we need to judge the data with the index value of $\text{thread_idx} \times \text{stride} + \text{block_idx} \times \text{nozero} + \text{pos} + \text{pos}$ is the relative position in the convolution window; if it is non-zero, store the position in $F_{\text{data}}$ to the index value of $\text{thread_idx} \times k_k \times k_i + \text{num} \times \text{nozero}$. Simultaneously, the value of the storage $\text{pos}$ location convolution kernel is stored in the corresponding position in $K_{\text{data}}$, and store $\text{num} \times \text{nozero}$ into $\text{Ptr}$.

As shown in Algorithm [1], a single-threaded algorithm is described for converting an input feature graph to the storage format described above. Where $F_{\text{data}}$ and $K_{\text{data}}$ are declared Shared memory, the whole process is a process of transforming the feature graph accessed from global memory into the new format of shared memory storage. The fourth line of code sets the starting address that this thread needs to access. The fifth line begins to determine if it is a non-zero value, and if it is a non-zero value, it is stored in the corresponding $K_{\text{data}}$ vector and $F_{\text{data}}$ vector. After the end of the loop, store the position where the non-zero value ends in the $\text{Ptr}$ vector, and store -1 if there is no non-zero value.
Algorithm 1 Storage Format Algorithm

1: \(\text{temp} \leftarrow 0\)
2: for \(i = 0\) to \(k_h\) do
3:   for \(j = 0\) to \(k_w\) do
4:     \(\text{offset} \leftarrow \text{thread}_{-}\text{idx} \times \text{stride} + \text{block}_{-}\text{idx} \times i \_w + i \_w \times j\)
5:     if \(\text{input}[\text{offset}] == 0\) then
6:       \(F\_\text{data}[\text{thread}_{-}\text{idx} \times k\_w \times k_h + \text{temp}] \leftarrow \text{input}[\text{offset}]\)
7:     \(K\_\text{data}[\text{thread}_{-}\text{idx} \times k\_w \times k_h + \text{temp}] \leftarrow \text{kernel}[i + j \times k_w]\)
8:   end if
9: end for
10: end for
11: if \(\text{temp} == 0\) then
12:   \(\text{ptr}[\text{thread}_{-}\text{idx}] \leftarrow \text{thread}_{-}\text{idx} \times k\_w \times k_h + \text{temp} + 1\)
13: else
14:   \(\text{ptr}[\text{thread}_{-}\text{idx}] \leftarrow -1\)
15: end if

B. Blocking and sparsity convolution algorithm

In this subsection, we will describe the algorithm for sparse convolution calculation based on the above storage format and use Fig. 3 as an example to analyze the reduced computational multiplication and addition times.

In the previous subsection, we obtained a compressed feature matrix containing \(F\_\text{data}\) of feature data and \(K\_\text{data}\) containing kernel data, and a \(P\_\text{ptr}\) vector containing the amount of data. As shown in Fig. 5, we can consider \(F\_\text{data}\) and \(K\_\text{data}\) as two matrices according to the values in \(P\_\text{ptr}\), and multiply the matrix, that is, reduce the redundant zero value calculation and obtain the lossless convolution result.

As shown in algorithm 2, the algorithm pseudo-code of a single thread for a convolution result is described. The first line of code is to access the corresponding \(P\_\text{ptr}\) vector in the shared memory to determine whether a non-zero value is stored in the stored procedure. If no non-zero value is stored (when \(P\_\text{ptr}=-1\)), it is immediately judged that no convolution is needed. This time the convolution value is 0. If a non-zero value is stored, we need to access the values in \(K\_\text{data}\) and \(F\_\text{data}\) in shared memory in turn and perform a multiply-add operation. The convolution result is finally obtained.

Algorithm 2 Convolution Algorithm

1: if \(\text{ptr}[\text{thread}_{-}\text{idx}] == -1\) then
2:   \(\text{output}[\text{thread}_{-}\text{idx} \times \text{block}_{-}\text{idx} \times \text{blockDim}_{\cdot}x] \leftarrow 0\)
3: else
4:   for \(i = \text{thread}_{-}\text{idx} \times k\_w \times k_h\) to \(\text{ptr}[\text{thread}_{-}\text{idx}]\) do
5:     \(\text{output}[\text{thread}_{-}\text{idx} \times \text{block}_{-}\text{idx} \times \text{blockDim}_{\cdot}x] += F\_\text{data}[i] \times K\_\text{data}[i]\)
6:   end for
7: end if

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Algorithm extension analysis

In this paper, we describe in detail the implementation of a sparse block compression algorithm for a single feature map. However, in the actual application process, multiple feature maps in one layer require convolution calculation. So the feature map required to be calculated can be increased in an integrated manner. This approach increases the number of computed GPU threads and increases parallelism. Our method can also be extended to the above method. Since the amount of calculation in a single thread is reduced, the calculation speed is also much improved in the multi-threaded calculation. In the next section, we will illustrate the experimental effects of our new algorithm on various models and compare them with CuDNN. Our algorithm code is open source and is located at https://git@github.com:milk2we/bell.git.

V. EXPERIMENTS AND DATA-SET

In this section, first, we introduce a new data-set for convolution optimization. Then, we introduce our experimental environment. At last, we present the speed comparison experiment, memory consumption comparison experiment, and power consumption comparison experiment.
TABLE I
SINGLE LAYER ACCELERATION EFFECT TABLE

| Network   | Layer | Size  | Sparsity | New Speedup | CuDNN Speedup | Speedup |
|-----------|-------|-------|----------|-------------|---------------|---------|
| LeNet     | Conv2 | 11x11 | 0.95     | 1.096       | 1.691         | 1.54    |
| AlexNetC  | Conv3 | 6x6   | 0.9      | 0.804       | 1.64          | 2.04    |
| AlexNetI  | Conv4 | 5x5   | 0.9      | 4.435       | 15.103        | 3.40    |
| GoogLeNet | Inception4a.1 | 14x14 | 0.9 | 2.034 | 4.938 | 2.42 |
| GoogLeNet | Inception4a.2 | 14x14 | 0.9 | 1.017 | 2.409 | 2.42 |
| GoogLeNet | Inception4e.3 | 14x14 | 0.9 | 3.602 | 12.380 | 3.57 |
| GoogLeNet | Inception5a.1 | 7x7 | 0.95 | 2.733 | 6.579 | 2.40 |
| GoogLeNet | Inception5a.2 | 7x7 | 0.9 | 1.831 | 4.122 | 2.25 |
| GoogLeNet | Inception5b.3 | 7x7 | 0.95 | 4.421 | 15.168 | 3.43 |
| GoogLeNet | Inception4a.7 | 7x7 | 0.95 | 1.576 | 3.284 | 2.08 |

Fig. 6. Comparison of convolution calculation time for VGG-19 between different methods. Stride is 1. The left axis represents time (ms), and the right axis represents sparsity.

A. New data-set for convolution optimization

We provide this new data-set for convolution optimization, which is a collection of all input feature maps of the convolutional layer. The data-set is obtained by having a picture of a cat through the entire network architecture, ensuring the authenticity of the data. Therefore, using this data-set to optimize the convolution calculation is more convenient and faster, hence improves work efficiency, compared with the previous method of modifying the already integrated network framework.

The current data-set contains all the feature maps of VGG-19 that require convolution calculations. It also contains a file-list of convolution layer file name and a size file for all feature maps. This data set is open source and placed in https://git@github.com:milk2we/feature_map_dataset.git. In future work, we will continue to add more network models.

B. Experiment platform

As shown in Table. II, the operating system environment is ubuntu18.04, the CPU is Intel(R) Xeon(R) CPU E5 v3 @ 2.40GHz. The GPU is GeForce GTX 1080T, and the memory is 128G. Besides, the CUDA environment is CUDA-10.0 and the corresponding CuDNN version is 7.6.1.

TABLE II
EXPERIMENT RUNNING GPU ENVIRONMENT

| OS         | CPU            | GPU              | Memory |
|------------|----------------|------------------|--------|
| ubuntu18.04| Intel(R) Xeon(R) CPU E5v3 @ 2.40GHz | GeForce GTX 1080T | 128G   |
|            |                | CUDA             | CuDNN  |
| Version    | 10.0           | 7.6.1            |

C. Convolution calculation speed comparison experiment

In this subsection, we conducted a speed comparison experiment. First, we recorded a single-layer speed comparison experiment on the single-layer feature map and CuDNN in some network models. Then we used the data set to carry out the VGG-19 convolution speed comparison experiment and analyzed the experimental results.

As shown in Table. II we can see that the convolution speed of some layers can be up to 3.5X of CuDNN. For feature maps in deep networks, the size is 7 × 7, which is very small comparing with the initial input feature map. However, the traditional GEMM is not suitable for matrix multiplication calculations with small feature maps. Therefore, our algorithm performs further compression for small feature
mapping according to the principle of large sparsity, which reduces the calculation amount of a single thread, thereby improving the calculation speed.

As shown in Figure 6 in the VGG-19 model, our algorithm always has very good performance as the depth of the network deepens. Compared with the CuDNN algorithm, the new algorithm can achieve 2X speedup, and it is also faster than other algorithms. In all, compared with the CuDNN algorithm, our algorithm can achieve up to 2.9X speedup, and the entire network running time can achieve 2.3X speedup.

As shown in Fig. 7(a) and Fig. 7(b), we performed experiments with strides of 2 and 3 using the VGG-19 feature map data-set. Our method can achieve 1.8X and 1.75X speedup by CuDNN. Therefore, it can be seen from the experimental results that our algorithm has a good advantage in calculation speed. It is suitable for convolution calculation of deep networks with large sparsity and small feature map.

D. Memory consumption comparison experiment

The technology of compressed storage computing is used in the new algorithm, so the memory used in the calculation process is also improved for deep convolution layers of convolution neural network. As shown in Fig. 9, our algorithm saves 35% of memory consumption compared with CuDNN, and saves 17% of memory compared with im2col. However, for some convolutional layers with low sparsity, the memory usage is relatively high, and there are certain limitations on the use of shared memory. Therefore, designing a more efficient storage format is the focus of our future work.

Fig. 7. Comparison of convolution calculation time for different strides on VGG-19. The left axis represents time (ms), and the right axis represents sparsity.

Fig. 8. Relationship between sparsity, size and speedup over CuDNN on VGG-19.

In addition, we propose a quantized value $\Theta = \text{Sparsity/Size}$. For VGG-19, the larger the Sparsity value, the smaller the Size value. The larger the $\Theta$ value, the higher the depth of the network. As shown in Fig. 8, we can see that the speedup has the similar trend to $\Theta$. In other words, our algorithm is suitable for convolution calculations of deep networks with small feature map and large sparsity.

As shown in Fig. 7(a) and Fig. 7(b), we performed experiments with strides of 2 and 3 using the VGG-19 feature map data-set. Our method can achieve 1.8X and 1.75X speedup by CuDNN. Therefore, it can be seen from the experimental results that our algorithm has a good advantage in calculation speed. It is suitable for convolution calculation of deep networks with large sparsity and small feature map.
VI. RELATED WORKS

Convolution operation is an important operation for many deep neural networks in a broad range of domains \[30\]. Meanwhile, many research works focus on its optimization from the algorithm level and architecture level. Some optimization techniques have been integrated into CuDNN.

**im2col+GEMM** As mentioned in Section II, the im2col algorithm is an algorithm based on linear expansion and combined with GEMM to calculate convolution, such as the previous version of CuDNN and the open source framework Caffe. This method can get a good acceleration effect according to GEMM, but because of the limitations of GEMM for small matrix, the algorithm has reached the bottleneck \[28\], \[29\].

**FFT** Fast Fourier Transform (FFT) is a computational tool commonly used for signal analysis, such as digital signal processing lamps. Fast Fourier Transform is a fast method for calculating discrete Fourier transform samples (called time series) of a series of data. It uses this relationship to convert the time domain correlation calculation to the frequency domain calculation between the time domain and the frequency-domain and converts the time-domain convolution calculation into the frequency domain matrix multiplication calculation \[9\].

**Winograd** Winograd algorithm is a method based on the Winograd kernel algorithm, which was initially proposed to calculate in matrix multiplication, which dramatically reduces the time complexity of matrix multiplication. This algorithm is superior to the small kernel and small-batch algorithms because they compute the smallest arithmetic complexity convolution data on the small input kernel. The use of small blocks also reduces the size of the algorithm's workspace, making the algorithm more efficient \[10\].

The above software optimization methods are all absorbed into CuDNN \[8\], which makes CuDNN more advantageous for convolution calculation.

VII. CONCLUSION

Convolution operations have a wide range of applications in machine learning, such as image recognition. However, due to the inherent nature of the convolution operation, its computational effect on the GPU is not ideal. The existing optimization method calculates a large number of zero values in the input feature map, which is redundant for the final convolution result. Therefore, we skipped these zero values and designed a new storage format to reduce the number of accesses to global memory when the feature map was transferred to the GPU-side shared memory. In addition, the locality principle of the data is also utilized, which further improves performance. Since the calculation amount of a single thread is reduced, the calculation time of a single thread is greatly improved. The acceleration effect on the small feature map is more obvious. The final experimental results show that the VGG19 model has a 2.3X speedup over CuDNN. In addition, the speedup for the deep convolutional layers of some network models can reach 3.5X.

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