Synaptic Plasticity in Semiconducting Single-Walled Carbon Nanotubes Transistors

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Recently, a significant amount of attention went toward the development of artificial neural networks, as these promise efficient computation for specific tasks that are expensive or even impossible for von Neumann architecture-based computers. A considerable amount of research is conducted to develop materials in which layered neural networks are easily implemented. Herein, the use of high-quality semiconducting single-walled carbon nanotube (s-SWCNT) inks to fabricate artificial synapses using simple bottom-gate field-effect transistors (FETs) is reported. The synapse utilizes the otherwise often dreaded hysteresis, the characteristic of the device structure, and the materials used therein. This hysteresis spans several orders of magnitude. The SWCNT synaptic transistor exhibits a clear spike-time-dependent plasticity (STDP), indicating the ability to achieve learning, following a mechanism similar to biological systems: asymmetric anti-Hebbian learning. The very well-defined STDP shape, together with the use of a simple pulse shape to obtain it, has not been reported previously for synaptic transistors. This represents a crucial step for further development of actual hardware implementation of artificial synapses in a more extensive, layered network. Interestingly, the time response of the device is very similar to the one of biological synapse, opening opportunities unavailable to CMOS emulations.

1. Introduction

One of the most sophisticated and specialized computers nowadays is still of biological origin: the human brain. It efficiently conducts massive parallel computing, using only 20 W of power. The brain has a computational power far beyond anything artificially developed; in particular, it is much more efficient in processing complex and unstructured data than von Neumann computers. Neurons are processors in the brain, which can communicate in parallel with each other through synapses. The average human brain consists of about $10^{12}$ neurons and $10^{15}$ synapses, these large numbers give redundancy and therefore the very much desired fault tolerance.

The realization of artificial computers capable of competing with the brain is of great interest for a large number of applications of vast complexities such as image classification and always-on life-long (unsupervised) learning. However, it appears as a task of enormous difficulties in particular if the power consumption of the biological brain should also be achieved. In addition, size and thus portability can also be an issue as many AI algorithms are rather heavy and rely on cloud computing. If an application is required to run on a portable device without internet access, no solution is available at the moment.

One of the most interesting approaches is to devise hardware components to fabricate artificial neural networks. As the synapses are the functional connections between the neurons and are believed to be the units enabling learning and computing, hardware implementations able to emulate biological synaptic functions are of fundamental importance in the pathway to brain-like computers. One of the most significant challenges lies within the synaptoplastic nature of these communication points. The efficiency of signal transfer between neurons, which is often referred to as synaptic weights, depends on the history of the activity of the pre- and postsynaptic neurons. This activity-dependent variation of the synaptic weights is called, collectively, synaptic plasticity. The synaptic plasticity is classified into short-term plasticity (STP) and long-term plasticity (LTP). The first occurs in the millisecond-to-minutes range and is at the basis of critical computations conducted by the brain.
The second includes changes that last several hours or even longer and are at the foundation of learning and memory.

Earlier attempts to mimic brain-like behavior and spiking neurons were demonstrated using conventional CMOS technology. Different types of synaptic behaviors are demonstrated in these works, such as spike-time-dependent-plasticity (STDP) and paired pulse facilitation (PPF). However, these approaches generally require a large number of transistors and large capacitors for their operation, increasing power consumption and lowering efficiency and integrability with respect to the von Neumann approach.

Often memristors are mentioned as prime candidates to address these requirements. A memristor is a resistor with a built-in memory effect, exhibiting a history-dependent resistance. This resistance can be varied using a variety of external stimuli in a specific sequence, e.g., by application of succession of voltage pulses. Furthermore, they are made of a large variety of materials, and different underlying working mechanisms have been reported. However, next to the many advantages, memristors also show a large number of limitations. Few examples are device variability, operational instability, and the challenge in downscaling their size.

Synaptic transistors or memtransistors are exciting alternatives to memristors. Among the several expected advantages are 1) the natural pathway to downscale their size, which is necessary to scale up the dimensions of the overall neural network; 2) the more extensive range of possible conductance values, which makes neural networks more robust and reliable; 3) that the control circuitry, otherwise required to realize learning behavior in two-terminal devices, can be omitted; and 4) that signal transmission and unsupervised learning can be obtained simultaneously.

Even though synaptic transistors have been much less investigated than memristors, several examples utilizing electrochemical gating and ion diffusion, charge-trapping memory, floating gate structures, ferroelectric gate, and optoelectronic actuation have been reported.

Semiconducting single-walled carbon nanotubes (s-SWCNTs) have recently been used as active semiconductors of synaptic transistors. Due to their individual sizes being \( \approx 1.0 \) nm in diameter, devices fabricated from s-SWCNTs can offer the desired density and compactness. Also, their solution processability allows for the easy and inexpensive fabrication techniques and the formation of extended nanonetworks. Furthermore, s-SWCNTs have excellent semiconducting properties, and their use in specific device structures can provide a memory mechanism. Therefore, in principle s-SWCNTs would allow for the fabrication of a hybrid hardware type where the transistor can work as a digital building block, but also as a neuromorphic element.

The combination of SWCNT and conjugated polymers was reported to result in synaptic behavior. It has also been shown that SWCNT gated by electrolytes exhibits both STP and LTP. Furthermore, floating gate structures and charge-trapping mechanisms have proven to perform well in simulated neuromorphic circuitry.

In this work, we demonstrate an artificial synapse utilizing hysteresis in polymer-wrapped s-SWCNT transistors with SiO\(_2\) as the gate dielectric. Neuromorphic plasticity is extensively examined using different pulse shapes (square wave, sinusoidal, sawtooth wave), all highly symmetrical with respect to their half period. These waveforms have been selected looking at the simplicity of implementation in an electronic circuit, such as a neural network composed of our synaptic devices. Avoiding the requirement for complex signals would considerably reduce the number and complexity of electronic components required for a functional neural processor, therefore simplifying the design, enhancing robustness, and reducing overall costs.

The unsupervised learning capability of our synapse is verified based on STDP measurements carried out with the selected pulse shapes, showing the presence of an asymmetric anti-Hebbian learning rule. Interestingly, our synapses, at the opposite of CMOS emulations, show response times very close to the ones of biological synapses. This is a fact that can open opportunities not only for using them for experiments aimed at a better understanding of biological brains but also for the integration of artificial devices with the brain.

2. Results and Discussion

Figure 1a shows a schematic representation of a biological neuron. Neurons are interconnected by an interface between their axon terminals and dendrites, where the axon side is the presynaptic or signal-releasing end and the dendrites are the postsynaptic or signal-receiving end. This interconnection is called a synapse and works, in general, but not exclusively, with a chemical communication protocol, which is also the one most often mimicked in artificial synapses. The efficiency of information transfer depends on synaptic weights; this synaptic weight is established by the history of transmission between the two terminals. Therefore, there must be a biological protocol able to potentiate (increase its weight) or depress (reduce its weight) the connection. One of the protocols that have been proposed and observed in biological systems is STDP, the principle of which is schematically shown in Figure 1b. This protocol is based on the fact that the synaptic weight can be changed by the temporal relation of the presynaptic and the postsynaptic pulses (see Figure 1b). STDP is one of the learning algorithms, which is also successfully implemented for pattern recognition. The interaction between different neurons can be represented as that in the example in Figure 1c. Axon terminals \( x_b \) are connected through weighed synapses \( w_b \) to the neuron B. The nucleus of neuron B sums up all pulses received through the synapses, and, when a threshold \( V_{th} \) is reached, neuron B fires a pulse to the next neuron.

As mentioned earlier, s-SWCNTs are very interesting semiconductors for the development of synaptic transistors. Their dimensionality (with a diameter in the 1.0 nm range) allows the manufacturing of very dense networks of synapses, which is a fundamental precondition for the fabrication of a viable brain-like-computer.

For the fabrication of our synaptic transistors, we utilize the dispersion of polymer-wrapped s-SWCNTs of high purity deposited on the device structure by a blade-coating technique. A schematic is shown in Figure 2a. The device structure and the connection for the presynaptic and postsynaptic signals are shown in Figure 2b. The drain terminal is grounded, and the gate is biased in a pulsed mode. In the case of STDP
measurements, the prepulse is sent to the source electrode and the postpulse to the gate electrode. The current flowing in the channel is measured under different bias conditions, representing the current conductance state (“synaptic weight”). An example of a traditional transfer characteristic measurement, displaying significant hysteresis between forward and reverse sweep is shown in Figure 2c. This hysteresis is used to achieve different conductive states and “synaptic weights” by measuring $I_{SD}$ at

Figure 1. Schematic representation of a) neuron comprising the neural system. b) Details of the relevant area around the synapse, and schematic of the potentiation and depression mechanism. The time difference between pulses from the neuron A to neuron B is given by $\delta t$, and synaptic weight varies by $\Delta W$. c) Schematic representation of the connection between different layers of neurons in a feed-forward neural network.

Figure 2. a) Display of the blade-coating procedure. First, the substrate is placed on a heated surface, after which a droplet of ink is deposited next to the blade. Subsequently, the blade is mechanically moved in a forward direction, distributing the ink evenly. b) Schematic representation of the bottom-gate device geometry used and of the terminal used for the presynaptic and the postsynaptic signal. c) Transfer characteristics of the transistor operating in an inert atmosphere, a pronounced hysteresis is shown depending on the voltage scanning direction.
given $V_{SD}$. Here it is important to underline that the high voltages used are simply a limit of the device geometry, namely of the gate dielectric chosen and its thickness. The use of a different dielectric can bring the bias to only a few volts and to a variation of the hysteresis\cite{35,36}. Additional characterization data are found in Figure S1, Supporting Information.

In Figure 3, we report measurements to investigate the plasticity of our synaptic transistor. In Figure 3a, a pulse of 25 V is applied to the gate electrode for a duration of 50 ms. Transient current over this pulse is measured using 1 V source-drain bias. Due to the p-type characteristics of the polymer-wrapped SWCNTs, the majority charge carriers at this bias are holes.

![Figure 3](image)

**Figure 3.** Plasticity measurements. a) Transient behavior of the source–drain current when a 25 V pulse of 50 ms width is applied to the gate. The inset shows a close-up of the data in a plot in linear scale, showing electron trapping during the pulse. b) The same pulse as in panel (a) is applied but for 2 s, showing more pronounced electron trapping during the pulse. c) Source–drain current measurements for 2000 consecutive positive pulses (potentiation), followed by 2000 negative pulses (depression). One dot represents a current measurement, directly followed by a pulse and a delay before the next measurement. d) Source–drain current after a pulse train of 2000 consecutive positive pulses (potentiation), followed by 1500 s delay (no pulses, only measurements), followed by a train of 2000 negative pulses (depression). The red and black dots represent a current measurement directly followed by a pulse and a small delay before the next current measurement takes place. The turquoise dots are current measurements without any pulse applied. e) Current measurements as after a slow delay (1.5 s) between identical voltage pulses. A single positive pulse is directly followed by a negative pulse, after each pulse the current is measured. f) Current measurements after a fast delay (0.001 s) between identical voltage pulses.
However, during every positive pulse on the gate electrode, electrons are induced in the channel, and various mechanisms are gradually trapping these electrons. The mechanisms that play a significant role are 1) the presence of hydroxyl groups at the dielectric s-SWCNT interface; 2) the polymer energy levels; and 3) defects of the SWCNTs. Due to the electron trapping, we observe a small current decrease during application of the pulse, as shown in the inset of Figure 3a. Upon ending the pulse, a spike in current is observed, which is caused by trapped electrons attracting holes to the channel and by the charging/discharging of the gate dielectric itself (see inset in Figure 3a). This (hole) current subsequently drops quickly, indicating a fast detrapping of the majority of the electrons. However, as shown in Figure 3a, after 30 s, the current remains relatively high, compared with the initial state. This effect indicates that the operation of biasing the gate in a pulsed mode introduces a memory effect, which can consequently prove to be valuable as short-term potentiation (STP) of our artificial synapse.

Next, the effect of the applied pulse width on the transient behavior of the synaptic weight is examined (see Figure 3b). The current drops over a pulse width of 2 s, which indicates that electron trapping is not saturated in the pulse width time. This prolonged saturation time is in contrast with observations from Park et al., who reported saturated trapping after 100 ms.[37]

While the slow reaction time of these devices could appear to be a negative feature at first glance, it provides a very interesting opportunity to study the dynamics of the brain processes. Biological time constants are long and challenging to achieve in CMOS, which is designed to be fast. The integration of our device into an artificial neural network could be easily accessible and, due to the nature of the material, bear a close resemblance to biological neural networks.

The essential aspect of our devices is that different trap states are accessed by mere variation of the pulse width or the number of pulses. These plasticity effects can be used for achieving STDP, as learning protocol. At this stage, a discussion on the retention time seems to be premature, also because the necessary retention times are extremely dependent on the application of the neural network.

To further investigate the plasticity of our device, a consecutive train of 2000 positive pulses, followed by 2000 negative ones was applied. Figure 3c shows that the device can cycle through different conductance states, demonstrating both potentiation and depression over almost six orders of magnitude of the current. This behavior showing analogue-like memory is not unlike the one showed by memristors of different types,[38] however, the range of conductance states spanned by our devices is many orders of magnitude larger. When the data are plotted in a linear scale (see Figure S2a, Supporting Information), it becomes apparent that the synaptic transistor under inert atmosphere has a stronger nonlinearity. This could pose difficulties for implementation in neuromorphic hardware, as the change in conductance is not, as ideally would be, proportional to the number of input pulses.[39] This nonlinearity can most probably be counteracted by the application of different pulse intensities in the potentiation and depression tasks, even if this will severely complicate the driving electronics. At this point, it is essential to underline that the choice for 25 V pulses was initially based on literature reports,[23] where the pulse voltage was scaled to our dielectric thickness of 230 nm. Indeed, the hysteresis shown by the transfer characteristics of the synapse (Figure 2c) is the largest when pulsing at this voltage, while probing at \( V_G = 0 \) V.

In Figure 3d, the nonvolatile characteristics of the device are shown. The pulse train is applied analogously to the measurements shown in Figure 3b. However, this time between each potentiation and depression, the conductance is measured for almost half an hour without modulation of the synapse. After stopping with pulsing the current gradually falls back, showing the STP nature of the states again. It is important to note that the current is plotted in absolute scale. During depression pulsing with \(-25 \) V, a sudden increase in current is seen. However, the polarity of the current has changed, showing that our synapse switched from holes to electrons as the major charge carriers.

In Figure 3e (slow) and f (fast), the synapse is measured in between being consecutively modulated between single positive and negative pulses. These results suggest that after some initial “activation,” stable on and off states are reached for both slow (1.5 s delay between the pulses) and fast (0.001 s delay) modulation. After each modulation pulse, the conductance of our synapse can be reverted to the previous state. As a modulation delay of 0.001 s corresponds to a frequency higher than 1 Hz, the synaptic transistor has a retention time useful for some neuromorphic computing applications.[40] Interestingly, the introduction of oxygen in the measuring chamber at the level of 3–10 ppm shifts both the on and off states. The on/off ratio is kept identical (see Figure S3, Supporting Information).

Here it is essential to underline that the functioning of the synaptic devices depends heavily on sweeping history. Therefore, before proper characterization, a resetting sequence should be implemented in an attempt to set the device in a specific initial state. In addition, the measurement direction should be carefully considered. Because our device is a transistor, the sequence of applied pulses to (different) electrodes matters. If the gate is modulated before a source–drain current flows, different results can be expected as charge-trapping mechanisms are varied.

If the gate bias is applied as first, charge traps at the oxide interface are gradually filled. After that, the energy levels are better, or better, band bending, is modified. Alternatively, when a source–drain current is applied first, the charge traps on the electrode–semiconductor interface are first filled. Therefore, the dynamics of the overall charge trapping and hysteresis are different. In addition, it is crucial to keep in mind that the surface traps, originating from hydroxyl groups, are trapping electrons. If a protective layer of PMMA is added, the ester groups would act as hole trapping sites, again changing the dynamics and potentially reversing the hysteresis.[41]

The demonstration of synaptic plasticity in the form of STDP is often considered evidence of the relevance of synaptic devices for the fabrication of neural networks.[42] In Figure 4, the various STDP measurements carried out with different pulse shapes are summarized. For each measurement, the inset shows the used pulse shape with the green and blue color, indicating the pulse applied to the source electrode and the gate electrode, respectively. The specific frame shown in the inset is the one obtained for the timing difference between \( V_{\text{post}} \) and \( V_{\text{pre}} \), being \( \Delta t = 0.02 \) s. The ‘final bias’ over the source and gate electrodes is depicted as the red dashed curve in the insets. The change in
synaptic weight $\Delta W$ is defined by $\frac{W_{\text{after}} - W_{\text{before}}}{V_{\text{before}}}$. More detailed information about pulse shapes is shown in Figure S4, Supporting Information.

Figure 4a shows the results obtained by a first STDP measurement under pristine, ideal conditions. It is apparent that upon approaching $\delta t = 0$ from $\delta t = 0.1$ s, the synaptic weight is depressed. While for $\delta t < 0$, the synaptic weight is potentiated. This behavior is known as the asymmetric anti-Hebbian learning rule. Our synaptic transistor operates with a simple square-shaped, sinusoidal, and symmetric sawtooth pulse, in contrast to what is shown in the report of S. Kim et al.[23] The use of these simple shapes significantly improves the ease of implementation in integrated neural circuitry. Furthermore, in contrast with the approach of Kim et al., where a net bias is given to one electrode, in our measurements, the postpulse and prepulse are applied individually over two different terminals. This method, in turn, allows for probing the effects of sequentially pulsing the gate or source electrode first. Interestingly, synaptic behavior is achieved at low timings of $|\delta t| < 50$ ms, coinciding with the applied pulse widths. We are confident that by further tuning the parameters even faster timings could be achieved, opening up the possibility for high-frequency, fast-performing neural networks.

It is important to note that the STDP results of a new measurement carried out at a later stage, after a reset scheme, on the same device utilizing the same pulse shape are shown in Figure 4b. Again an asymmetric anti-Hebbian behavior is visible, illustrating the repeatability of our synaptic operation. Figure 4c–f shows the results of measurements obtained with various pulse shapes. Unfortunately, no proper reset scheme was found for these pulse shapes, as perhaps the charge trapping became too deep. With every pulse used, we found evidence of STDP learning rules. However, all learning rules were of the anti-Hebbian type. Interestingly, Kim et al.[23] also reported STDP behavior but in their case of the Hebbian type. This difference in results could be ascribed to the shape of the pre- and postpulses utilized, which in their case are bipolar (asymmetric) saw-edge pulses.

3. Conclusion

We demonstrated that when utilizing the hysteresis, which is commonly found in bottom-gate structure SWCNT field-effect transistors (FETs), sufficient plasticity arises to obtain a working artificial synapse using simple pulse shapes. The mechanism behind the hysteresis, and therefore the working principle of our synapse, is based on the charge carrier trapping at the interface between the dielectric and the semiconductor itself. To our knowledge, our devices show some of the best-defined STDP shapes reported up until now for SWCNTs-based synapses. More importantly, the anti-Hebbian learning is obtained, operating our synaptic devices using simple real-time square-shaped (sinusoidal and sawtooth) pulses, therefore lowering the technical barrier for integrated hardware implementation. These results represent a substantial leap forward for implementation of synapses based on s-SWCNTs into artificial neural networks.
4. Experimental Section

Preparation and Characterization of Semiconducting SWCNT Dispersion: HiPCO SWCNT inks were prepared and characterized as described in our previous work.\[43\]

Field-Effect Transistor Fabrication and Electrical Characterization: FETs were fabricated on silicon substrates with a thermally grown SiO₂ layer of about 230 nm in thickness. Source and drain bottom electrodes (10 nm ITO/30 nm Au) were lithographically defined. The s-SWCNT active material was deposited in a nitrogen-filled glovebox by a blade-coating method using a Zehntner ZAA 2300 automatic film applicator coater. The deposition procedure was repeated at least two times to achieve a good s-SWCNT density. After deposition, samples were annealed at 160 ºC for 60 min to evaporate the left-over solvent.

Electrical measurements were carried out using a probe station placed in a nitrogen-filled glove box at room temperature in the dark unless otherwise specified. The probe station was connected either to an Agilent E5270B Semiconductor Parameter Analyzer or a Keysight B2912A SMU, depending on which measurement was carried out. A specialized software, using Python 3.7, to have reasonable flexibility and speed in controlling the SMU for the plasticity and STDP measurements, was made.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest
The authors declare no conflict of interest.

Keywords
field-effect transistors, neural networks, polymer wrapping, single-walled carbon nanotubes, spike-time-dependent plasticities

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