Abstract—Tensor network methods are incredibly effective for simulating quantum circuits. This is due to their ability to efficiently represent and manipulate the wave-functions of large interacting quantum systems. We describe the challenges faced when scaling tensor network simulation approaches to Exascale compute platforms and introduce QuantEx, a framework for tensor network circuit simulation at Exascale.

Index Terms—quantum circuit, tensor network, exascale, HPC

I. INTRODUCTION

The ability to simulate quantum circuits is essential for the design and development of quantum computing hardware and algorithms. A common method to simulate quantum circuits with a small number of qubits is to store and evolve the state vector of the circuit’s qubits [1]–[3]. However, for circuits with a larger number of qubits, such as those considered for Noisy Intermediate Scale Quantum (NISQ) devices [4], [5], it can be intractable to directly evolve the full quantum wave-function, even on the largest supercomputers [6]. This is due to the memory requirements to store the wave function which grows exponentially with the number of qubits in the circuit.

Alternative simulation methods for quantum circuits, which attempt to mitigate the exponential memory issue, are those based on tensor networks. With these methods, quantum circuits are represented as networks of tensors, enabling output probability amplitudes to be calculated by contracting the network [7], [8]. This approach has achieved state of the art performance when simulating Random Quantum Circuits (RQC) [9] as part of the recent quantum advantage experiments [6].

Despite these impressive results, tensor network methods are not competitive for simulating all circuit types. In particular, for very deep/highly entangled circuits, the tensor network representation can require the same amount of memory as full wave-function methods. In these cases, full wave-function approaches with simpler memory management and fewer overheads are generally more efficient. For circuits targeting NISQ devices, with moderate depth/entanglement and where approximate results suffice, tensor network approaches can offer significant advantages as illustrated in Fig. 1.

The aim of this paper is to describe some of the challenges faced in utilising distributed platforms to simulate quantum circuits with tensor network methods and to present QuantEx, an open source quantum circuit simulation framework designed to be scalable and extensible. The paper is structured as follows: In Section II we provide an overview of the main tasks of a tensor network simulator and outline how tensor network methods can be used to simulate a quantum circuit. In Section III we describe the challenges encountered when implementing an efficient tensor network simulator capable of leveraging distributed compute resources. We also provide some information on some of the commonly used methods for dealing with these challenges. We then present our own
tensor network based quantum circuit simulator, QuantEx, in Section IV before concluding with an outlook on future work for the QuantEx project.

II. OVERVIEW OF A TENSOR NETWORK SIMULATOR

Quantum circuit simulators are used to perform two important tasks. Namely, validating the correctness of quantum hardware and simulating the execution of a quantum algorithm as if it was executed on a real quantum device. Depending on which task the simulator is being used to do, the output of a simulator can either be a list of probability amplitudes, corresponding to a predefined list of possible output bitstrings, or a set of random bitstrings, which are distributed according to the output wavefunction of the simulated circuit. For instance, to validate the output from Google’s Sycamore circuit, the authors of [10] had to compute the probability amplitudes for a list of bitstrings which were output from their circuit. To sample random bitstrings from a circuit, a version of rejection sampling is often used [11]–[13] where a candidate bitstring $x$ is generated, usually with a uniform distribution, and is randomly accepted as a sample from the circuit with a probability proportional to the probability the circuit would output $x$ when measured. To do this, a probability amplitude for $x$ needs to be computed. These examples highlight the main job of a quantum circuit simulator which is to compute probability amplitudes for measurement outcomes of a predefined quantum circuit.

In order to produce probability amplitudes for different measurement outcomes, a simulator needs to store a representation of the simulated circuit’s output state or wavefunction. Full state simulators do this by storing in memory a vector, representing the initial state of the circuit’s qubits, and applying a sequence of unitary matrices, representing quantum gates in the circuit, to transform the initial state into the final state of the circuit’s qubits. The desired probability amplitudes can then be read from this final vector. As mentioned in the introduction, a drawback of this method for larger circuits is that the size of the vector that needs to be stored grows exponentially with the number of qubits in the circuit. More precisely, a vector representing the state of $n$ qubits in a circuit needs to store $2^n$ probability amplitudes corresponding to the $2^n$ possible measurement outcomes. For large circuits, where the size of circuit’s state vector exceeds the available memory resources, a tensor network representation of the circuit’s output state can be used and is straightforward to create as we describe below after briefly introducing tensor networks.

A tensor network is a tensor expression involving the product of several tensors, or multi-dimensional arrays of complex numbers, of varying rank or dimension. For example, in the following expression the right hand side is an example of a tensor network:

$$T_{lm} = \sum_{ghijk} A_{gh} B_{hi} C_{ij} D_{jk} E_{jklm} \quad (1)$$

However, tensor networks typically refer to such expressions involving a large number of tensors such that a graphical notation is often used in place of the more traditional notation used above [7]. The graphical notation can be summarized as follows: Tensors in the tensor expression are depicted by nodes in a graph and indices in the expression are depicted by edges in the a graph. If two tensors share a common index then both tensors are connected by the edge representing that index. Indices that are unique to a tensor are depicted by an open edge. In graphical notation, equation (1) can be written as shown in figure Fig. 2.

![Fig. 2. A tensor network example.](image)

Given a complete description of a quantum circuit, a tensor network representing the output state of the circuit can be created using the matrix representation of the quantum gates used in the circuit [14]. To give a brief description of the process, each matrix of a gate can be used as a building block to piece together the desired network. In graphical notation, the $2 \times 2$ matrix of a single qubit gate is depicted by a single node with two adjoining edges. Likewise, the $4 \times 4$ matrix of a two qubit gate is reshaped into a rank 4 tensor of dimension $2 \times 2 \times 2 \times 2$ and depicted by a single node with four adjoining edges. If each qubit in the circuit has an initial state given by a two dimensional complex vector (usually the “zero” state $\left( \begin{array}{c} 1 \\ 0 \end{array} \right)$), the initial state of the $n$-qubit circuit is given by a network consisting of $n$ disjoint nodes with a single edge attached to each. Each qubit has a corresponding open index associated with it. To apply a gate to one or two of the qubits one needs only to adjoin the corresponding gate tensor to the network by attaching it to the open indices of the network corresponding to the target qubits. By adjoining gate tensors to the network in the order in which they appear in the quantum circuit, a tensor network representing the output state is constructed and should resemble a circuit diagram such as the one shown in Fig. 2.

The memory required to store the described tensor network structure grows linearly with the total number of qubits and gates in the circuit making it possible to represent states from large quantum circuits on a computer.

The price to be paid for such a memory efficient representation of the output state is a potentially large amount of computation to do whenever a probability amplitude is requested from the state. Namely, to retrieve a component from the output state, all tensors in the tensor network need to be multiplied together to compute the an expression analogous to equation (1). This computation is referred to as “contracting” the network and can be prohibitively expensive if not done carefully which we will elaborate on in the next section. Furthermore, contracting the network with $n$ open indices results in $2^n$ amplitudes being computed and stored in memory raising the same memory issue plaguing full wave function
To it corresponding to the different outcomes. Contracting the network with different output tensors adjoined storing the output state of the circuit and then repeatedly using a description of the circuit to build a tensor network measurement outcomes of a quantum circuit. This is done by computing probability amplitudes for various possible outcomes occurring when the output of the circuit is measured.

To summarise, the main function of a tensor network simulator is to compute probability amplitudes for various possible measurement outcomes of a quantum circuit. This is done by using a description of the circuit to build a tensor network storing the output state of the circuit and then repeatedly contracting the network with different output tensors adjoined to it corresponding to the different outcomes.

III. SCALING CHALLENGES

When attempting to execute a large tensor network simulation of a quantum circuit on a distributed system, a number of challenges arise which we discuss in the subsections below. We loosely categorise these challenges as high and low level challenges to reflect when these challenges arise. High level challenges can be dealt with before the simulation begins (i.e. before any probability amplitudes are computed) while low level challenges occur during the simulation. We now describe these challenges and some of the solutions that can be used to overcome them.

A. High-level challenges

The main high level challenge for a tensor network simulator is to plan exactly how it will contract a network. Contracting a tensor network involves multiplying all of its tensors together which can always be done as a sequence of pairwise tensor contractions \[7\], an operation which replaces two tensors in the network with their product. The computational cost of contracting a network typically depends on the sequence of pairwise contractions used to contract it. However, for a network consisting of \(N\) tensors, there are \(N!(N-1)!/2^{N-1}\) possible contraction orders and the majority of these can be very inefficient making it difficult to identify an optimal order. In fact, finding the optimal contraction order is equivalent to finding the tree decomposition of a graph with minimal treewidth \[14\], a problem which is believed to be NP-complete \[15\]. While finding the optimal order may be intractable, many algorithms exist to find “good” contraction orders in bounded time \[15\], [16].

To determine an efficient contraction order, the method employed by the authors for the QuantEx simulator is described in \[16\] and is based on computing a tree decomposition with minimal treewidth for the network’s line graph before converting it into a contraction order. In terms of tensor network contraction, the treewidth of a tree decomposition of a network’s line graph is the rank of the largest intermediate tensor created when the network is contracted according to the order determined by the decomposition. Thus, minimising the treewidth is akin to minimising the largest intermediate tensor produced by the contraction process. An algorithm called FlowCutter \[17\] is used to construct tree decompositions with optimal treewidth of a graph by iteratively partitioning it using maximal flows on the graph.

Another high level challenge for a tensor network simulator is in deciding how to fit the network contraction into available memory resources. Even when an optimal contraction order is found for a network, the memory requirements for contracting a network may exceed the limits of the platform running the simulation due to large intermediate tensors being created during network contraction. A common method for tackling this issue is that of slicing \[18\] which allows the simulator to reduce the memory requirements of a contraction in exchange for more network contractions. Slicing works by replacing the contraction of the original network with the contraction of several networks with less indices and summing the results. The contraction of the smaller networks are independent and can be done in parallel. The smaller networks are created from the original by choosing an index of the original network and fixing it to one of its values. In mathematical notation we can write this as follows:

\[
\sum_{ghij} A_{gh}B_{hi}C_{ij}D_{gj} = \sum_{g} \left( \sum_{hijk} A_{gh}B_{hi}C_{ij}D_{gj} \right),
\]

where the expression in parentheses on the right hand side is that of a smaller tensor network as depicted in Fig. 2. In order for this technique to adequately reduce the memory requirements of the simulation, the largest intermediate tensor produced by contracting the smaller networks must be smaller than the largest tensor created by contracting the original network. This may not be the case if indices are chosen to be sliced which are irrelevant to the size of the largest intermediate tensors. Thus, the ability to identify indices in the network which reduce the size of the largest intermediate tensors when sliced is integral to effectively using the method of slicing to reduce the memory requirements of a contraction. In graph theoretic terms, this problem translates into identifying edges...
of a graph which reduce the treewidth of the graph when removed, another NP-complete problem [19].

A novel algorithm for identifying efficient indices to slice in a tensor network was proposed in [19] and was shown to perform well. Their greedy “tree trimming” algorithm always chooses to slice indices that reduce the size of the largest intermediate tensor and therefore the treewidth. When there are several largest tensors, it aims to choose an index which reduces the size of not just one of the largest tensors but also the greatest number of intermediate tensors. In the special case where there exist several such options, it chooses an index which reduces the overall memory resources of the network contraction the most, randomly breaking ties when no unique option exists.

B. Low-level challenges

The primary low level challenge of a tensor network simulator is to perform the basic operations constituting the task of contracting a network. For instance, while the challenge of effectively slicing a tensor network is classified as a high-level challenge, the operations required for its implementation may require efficient memory management and inter-node communication. Therefore, to facilitate tensor network slicing and contraction on a distributed system, it is necessary to implement tensor primitives that are capable of permitting a sliced network to be contracted in parallel, such as tensor slicing and recomposition. Furthermore, tensor primitives for contracting, reshaping and permuting tensors are needed to perform a network contraction. With the emergence of Exascale systems, making efficient use of accelerators and CPU features is also crucial. While GPUs can offer impressive speedups, they also incur a second, tighter, memory bottleneck, adding further complexity to memory management.

As mentioned in Sec. II to simulate a quantum circuit, random bitstrings need to be generated which are distributed according to the output state of the circuit. To achieve this, rejection sampling techniques can be employed. Optimising these methods can either be done by reducing the number of network contractions that need to be performed or by reducing the average cost of a network contraction [11]–[13], raising yet another low level challenge. One issue with using a basic rejection sampling technique, or the frugal rejection method from [12], is that it requires setting a parameter \( M \) which determines the average number of candidate probabilities computed before a candidate bitstring is accepted as an output bitstring. Setting \( M \) to an optimal value requires prior knowledge of the simulated circuit’s output distribution which may not be available for the user’s circuit of interest. To avoid this issue, we chose to implement an alternative rejection method for QuantEx which was proposed in [20]. The empirical supremum rejection method follows the same recipe as the basic and frugal rejection methods but initially chooses \( M = 1 \). Then, after each iteration of the algorithm, \( M \) is updated according to

\[
M = \max(M, p(X)N),
\]

where \( X \) was the candidate bitstring in that iteration and \( N \) is the number of possible bitstring candidates. The authors of [20] suggest that \( M \) tends to converge quickly and suggest the use of a warm up period before using the algorithm, where several iterations of the algorithm are executed and their outputs discarded, to find a good estimate of the optimal \( M \). A big advantage of this method is that it requires no prior knowledge of the circuit output distribution to find a value for \( M \). This makes it ideal for sampling from a general quantum circuit.

IV. QuantEx

A. The QuantEx Tensor Network Simulator

In this section, we introduce a tensor network based quantum circuit simulator referred to as QuantEx. It was developed by the authors and designed to be extensible, scalable on Exascale compute platforms and utilise the solutions to the high and low level challenges discussed in Sec. III. The QuantEx framework consists of several special purpose software packages aiming to address different issues that arise in tensor network simulations. These are QXTools, QXTns, QXGraphDecompositions and QXContexts, each of which we described below and are available on github under the JuliaQX organisation [2]. The packages are also registered in the Julia package registry making them easily accessible. Julia [21] is used as the primary language, because of its flexible type system, the ability to wrap components in other languages while also providing native performance and native support for GPGPU programming. A domain specific language (DSL) is also used to represent a simulation as a set of primitive tensor operations. This separates the high level index accounting and contraction planning from the low level implementation of the tensor network operations and makes it easier to support new hardware and network architectures.

QXTools is the main QuantEx package for orchestrating a tensor network simulation of a quantum circuit. It can be used to create a tensor network for a quantum circuit, identify an efficient contraction scheme for the network and generate simulations files, including tensor data files and DSL files, that describe how the simulation should be executed on a cluster. It provides a quantum circuit simulation workflow which consists of the following steps:

1) Circuits are built and represented as QXZoo circuits.
2) The QXZoo circuit is converted to a QXTns tensor network.

\[1\]QuantEx Team, [https://github.com/JuliaQX](https://github.com/JuliaQX)

Fig. 4. Decomposing a tensor network as a sum of sliced networks.
3) This network is converted to a graph data structure provided by QXGraphDecompositions and a suitable tree decomposition and set of edges to slice are identified.
4) Using the tree decomposition and set of edges to slice a DSL representation of the computation is generated. This is then used as input to QXContexts to perform the computation using the context and settings that make the best use of the available resources.

**QXZoo** Provides data structure and functions for representing and generating quantum circuits.

**QXTns** is a Julia package with data structures and utilities for manipulating tensor networks. As well as a generic tensor network data structure, it also contains specific data structures for handling tensor networks derived from quantum circuits.

**QXGraphDecompositions** is a package for analysing and manipulating graph structures describing tensor networks. It provides data structures and functions for analysing and manipulating graph representations of tensor networks. In particular, it provides functions for finding efficient tree decompositions and for identifying sets of indices which when sliced can reduce the treewidth of the selected tree decomposition. This makes it possible to distribute computations across multiple processes/nodes.

**QXContexts** is designed to parse the simulation files created by QXTools and perform the tensor contractions that constitute the circuit simulation making use of distributed compute resources via MPI as well as hardware accelerators. It provides implementations of the tensor primitives mentioned as one of the low level challenges in Sec. III and uses the Julia package CUDA.jl to provide NVIDIA GPU support. It also provides an implementation of the sampling algorithm discussed in the low-level challenges section of Section III which can be used to generate random bitstrings which are distributed according to the output state of the simulated quantum circuit.

Three levels of parallelism are used by QXContexts to decompose the computation. At the highest level, computing probability amplitudes for different bitstrings is embarrassingly parallel and is distributed across multiple processes using a MPI communicator. A second level of parallelism is available if slicing is used to avoid large memory requirements. A MPI sub-communicator is used to perform the tensor contractions in the subtasks created by slicing across processes. Finally, the lowest level of parallelism is in utilising GPU hardware to perform tensor contractions which can be mapped to matrix multiplications.

**B. Initial Performance Results**

Work is ongoing to procure performance results for QuantEx on PRACE tier-0 and pre-Exascale HPC systems and to optimise the framework. In preparation for this, smaller scale tests were conducted to test scaling, support for different CPU architectures and GPU acceleration. We present these results in this section. To evaluate the performance of the QuantEx software, we use as a test case the problem of computing probability amplitudes for a list of possible bitstring outputs of a quantum circuit. The quantum circuits we use in these test cases are instances of random quantum circuits (RQC) defined in [9] and used in Google’s quantum advantage experiments [10]. These circuits consist of a 2 dimensional array of qubits with several layers of quantum gates acting on all qubits. For our initial scaling calculations, simulation files were generated for a RQC with a 5 by 5 grid of qubits and 24 layers of gates.

Initial scaling results were computed on ICHEC’s Kay cluster of 336 nodes where each node has 2x 20-core 2.4 GHz Intel Xeon Gold 6148 (Skylake) processors, 192 GiB of RAM, a 400 GiB local SSD for scratch space and a 100GiB OmniPath network adaptors. For Fig. 5 we take the case of computing 2048 amplitudes for the 5x5x24 RQC, with a single sliced bond, on 4 nodes with an increasing number of processes. The trend shown by these strong scaling results are expected to carry over to larger platforms given the embarrassingly parallel nature of how the simulation is decomposed.

Given that HPC systems are becoming increasingly heterogeneous, it is necessary for a viable simulator to run on various architectures in order to leverage novel HPC machines. To demonstrate that QuantEx is capable of this, additional tests of other HPC architectures have been performed on the BEAST system at LRZ. Small test quantum circuits consisting of 12 and 24 qubits were used in this case. The Bavarian Energy Architecture and Software Testbed (BEAST) is a collection of systems for the research and evaluation of new hardware technologies. Currently BEAST consists of three different CPU architectures: AMD X86, and Arm Fujitsu A64fx. An additional system segment is equipped with Arm ThunderX2, but the LIKWID tool was not fully functional on this architecture at the time of testing and therefore we leave it for future investigation. The AMD systems consists of two node Rome.
GPU 2U servers, with two AMD EPYC 7742 with 64 cores along with 512GB of DDR4-3200, two 1.9 Terabyte SSD and two AMD Radeon MI-50 GPUs with 32 Gigabytes of high bandwidth memory (HBM). The interconnections between the nodes are Mellanox InfiniBand: HDR 200Gb/s. Finally, the Fujitsu A64fx system is an eight node HPE system consisting of Arm Fujitsu A64fx CPUs with 64 cores and two 512 bit vector units and 32 gigabytes HBM2 memory that is connected with a Mellanox InfiniBand EDR interconnect.

The table lists the key features of the different architectures evaluated on BEAST. A point of reference (third column) is provided by the Intel Xeon Scalable Processors (“Skylake”) of SuperMUC-NG. The table also presents some performance diagnostics collected using LIKWID, namely run time, arithmetic throughput, and measured memory bandwidth of our architecture.

QuantEx’s NVIDIA GPU support was tested using a 16GB NVIDIA Volta V100 GPU on Cineca’s Marconi100 system. Here, we measured the time to compute a single amplitude on both a GPU and on one of Marconi100’s 16-core IBM POWER9 processors. The time was measured for several, progressively difficult, quantum circuits and the results are displayed in Table I. Each row contains the results of a different circuit with the first column giving the name of the circuit. The second column contains the treewidth of the simulation which is a proxy for how difficult the simulation is as the complexity of the simulation is exponential in the treewidth. The memory column shows the maximum memory footprint of the simulation. The measured time is the time to complete one of these subtasks.

V. Conclusion and Outlook

We have provided a high level overview of the key challenges faced when scaling tensor network circuit simulation methods to Exascale and the some of the available solutions to those challenges. We also introduced the QuantEx simulation framework as a viable open source quantum circuit simulation tool and demonstrated it is capable of scaling on distributed systems and utilise GPU accelerators. The software was successfully tested on Intel and AMD CPUs and on NVIDIA GPUs and future work includes expanding the supported hardware to include AMD GPUs and Intel GPUs. While work is currently ongoing to benchmark and optimise the QuantEx simulator, it is the author’s hope that the work presented here establishes QuantEx as an open source quantum circuit simulator with the potential to compete with state of the art simulators such as CoTenGra and QTensor in the near future.

Future work on QuantEx the project includes further optimising circuit simulations and testing the software on the forthcoming European pre-Exascale and Exascale machines. Optimizing simulations may be achieved via improved network contraction planning capabilities and better bitstring sampling methods. One method for improving a contraction plan for a tensor network is that of local optimization. This involves replacing subsections of a contraction plan with optimal alternatives found using an exhaustive search and potentially offers significant improvements in computational cost of a simulation. An approach to optimising bitstring sampling using memoization was also proposed recently and offers large reductions in the time complexity of a simulation. The method consists of designing a contraction plan for a tensor network with a natural checkpoint which a simulation can return to between samples to avoid recontracting a large portion of the network. A rewarding direction of future work would be to integrate this technique with QXContexts to greatly improve efficiency and possibly generalise the method to identify optimal checkpoints in arbitrary contraction plans, let alone carefully designed plans, broadening the contraction planning algorithms that can be used with this technique.
Furthermore, efforts are ongoing to identify suitable opportunities to integrate the developed tools into commonly used quantum circuit simulation frameworks. One particular direction the QuantEx team is exploring is the possibility of integrating quantex as a backend for the popular Yao.jl framework. The Julia package YaoQX JULIA was developed with the hope of enabling Yao.jl users to take advantage of distributed systems and pre-Exascale and Exascale HPC clusters to simulate quantum circuits.

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REFERENCES

[1] G. G. Guerreschi, et al., “Intel Quantum Simulator: A cloud-ready high-performance simulator of quantum circuits”, [arXiv:2001.10554] [quant-ph] (2020)

[2] T. Jones, et al., “Quest and High Performance Simulation of Quantum Computers”, [arXiv:1802.08032] [quant-ph] (2018)

[3] M. Smelyanskiy, et al., “qHiPSTER: The Quantum High Performance Software Testing Environment”, [arXiv:1601.07195] [quant-ph] (2016)

[4] J. Preskill, “Quantum Computing in the NISQ era and beyond”, Quant. 2, 79 (2018), doi: https://doi.org/10.22331/q-2018-08-06-79.

[5] M. Brooks, “Beyond quantum supremacy: the hunt for useful quantum computers “, Nature 574, 19-21 (2019), doi: https://doi.org/10.1038/s41586-019-02936-3.

[6] B. Villalonga et al., “Establishing the Quantum Supremacy Frontier with a 281 Pfpop Simulation”, Quantum Sci. and Tech., 5 034003, (2020).

[7] J. C. Bridgeman and C. T. Chubb, “Hand-waving and interpretive dance: an introductory course on tensor networks.” Journal of Physics A: Mathematical and Theoretical, 50(22):223001, (2017).

[8] J. Biamonte and V. Bergholm, “Tensor networks in a nutshell,” 2017, arXiv:1708.00006.

[9] T. Boixo, et al., “Characterizing quantum supremacy in near-term devices”, Nature Phys 14, 595–600 (2018) doi: https://doi.org/10.1038/s41567-018-0124-x

[10] Arute, F., Arya, K., Babbush, R. et al. Quantum supremacy using a programmable superconducting processor. Nature 574, 505–510 (2019). https://doi.org/10.1038/s41586-019-1666-5

[11] Villalonga, B. and Boixo, S. and Nelson, B. et al., “A flexible high-performance simulator for verifying and benchmarking quantum circuits implemented on real hardware”, npj Quantum Inf. 5, 86 (2019), doi: 10.1038/s41534-019-0196-1. Repository: https://github.com/ngnrsaa/qflex.

[12] I. Markov, et al., “Quantum Supremacy Is Both Closer and Farther than It Appears”, [arXiv:1807.10749] [quant-ph] (2018)

[13] P. Feng, et al., “Simulating the Sycamore quantum supremacy circuits”, [arXiv:2103.03074] [quant-ph] (2021)

[14] I. Markov, et al., “Simulating quantum computation by contracting tensor networks”, [arXiv:quant-ph/0511069] (2009) doi: 10.1137050644756

[15] E. S. Fried et al., “Torch: The quantum tensor contraction handler”, PLoS ONE, vol. 13, no. 12. (2018), doi: 10.1371/journal.pone.0208510.

[16] J. Gray and S. Kourtis, “Hyper-optimized tensor network contraction”, 2020, arXiv:2002.01935

[17] M. Hamann, B. Strasser, “Graph Bisection with Pareto-Optimization”, Proceedings of the 18th Meeting on Algorithm Engineering and Experiments (ALENEX’16).

[18] C. Huang, et al., “Efficient parallelization of tensor network contraction for simulating quantum computation”, Nat Comput Sci 1, 578–587 (2021) doi: https://doi.org/10.1038/s43588-021-00119-7

[19] R. Shutski et al., “Simple heuristics for efficient parallel tensor contraction and quantum circuit simulation”, Phys. Rev. A 102, 062614, (2020). Doi: https://doi.org/10.1103/PhysRevA.102.062614.

[20] B. Caffo, et al., “Empirical supremum rejection sampling”, Biometrika, Volume 89, Issue 4, December 2002, Pages 745–754, (2002) doi: https://doi.org/10.1093/biomet/89.4.745

[21] J. Bezanson et al., “Julia: A Fresh Approach to Numerical Computing.”, SIAM Review, 59(1):65–98, (2017). Publisher: Society for Industrial and Applied Mathematics.

[22] https://eurohpc-ju.europa.eu/discover-eurohpc-ju

[23] https://www.bmbf.de/bmbf/sharedocs/pressemitteilungen/de/2021/07/130721-EuroHPC.html

[24] C. Huang, et al., “Classical Simulation of Quantum Supremacy Circuits”, [arXiv:2005.06787] [quant-ph] (2020)