Design and application of digital phase locked loop based on Quartus II

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Abstract. The traditional phase locked loop (PLL) is realized by analog circuit. Compared with PLL realized by traditional analog circuit, digital phase locked loop (DPLL) has the advantages of high precision, not affected by temperature and voltage, adjustable loop bandwidth and center frequency, and easy to construct high-order PLL. With the rapid development of communication technology and integrated circuit technology, DPLL will be more widely used. In this paper, the PLL macroblock is used to design and realize the functions of frequency division, frequency doubling and phase locking in Quartus II development environment. The validity of the design and application of the DPLL is verified by practical verification.

1. Introduction

Phase locked loop (PLL) technology has been widely used in many fields. Such as signal processing, modulation and demodulation, clock synchronization, frequency doubling, frequency synthesis and so on are all applied to the PLL technology. The traditional PLL is realized by analog circuit. Compared with PLL realized by traditional analog circuit, digital phase locked loop (DPLL) has the advantages of high precision, not affected by temperature and voltage, adjustable loop bandwidth and center frequency, easy to construct high-order PLL, and it does not need A/D and D/A conversion when applied in digital system. With the rapid development of communication technology, integrated circuit technology and in-depth study of system-on-chip (SOC), DPLL will be more widely used in it [1-3].

Quartus II is an integrated development software for programmable logic devices (PLD) launched by Altera company in the early 21st century. This software is an updated product of its previous generation of programmable logic integrated development software MAX + PLUS II. Quartus II integrated development software supports the whole process of programmable logic devices. It provides a design environment independent of device structure. The interface of the software is friendly, which makes it convenient for the designer to input, process and program the device. QuartusII integrated development software provides a complete multi-platform design environment, which can meet the needs of various specific designs. Quartus II design tool supports VHDL, Verilog HDL hardware description language design environment. It is also an integrated design environment for system on a programmable chip (SOPC). In addition, Quartus II integrated development software can also use the results of third-party software and support the work of third-party software [4-5].

In this paper, the PLL macroblock is used to realize the functions of frequency division, frequency doubling and phase locking based on Quartus II. Two macroblocks are mainly called. The first macroblock divides the 50M clock by 10 to generate a 5M reference clock signal. The C0 port of the
second macroblock performs frequency division for 5M clock and C1 port performs frequency doubling for 5M clock. There is no phase offset between them. The C2 port has a 90 degree phase offset based on the frequency division of 5M clock.

2. Creating digital phase locked loop (DPLL) macroblocks for engineering projects
Firstly, open the Quartus II project that needs to apply digital phase locked loop. Click Tools in the main menu bar and select "MegaWizard Plug-In Manager", as shown in Fig.1(a). In the following window, select "Create a new custom megafuction variable", and then click "next", as shown in Fig.1(b). Open the IO folder in the left menu bar and select the macroblock "ALTPLL". The device type on the right is Cyclone IV E, the output file is Verilog HDL, and the file name is pll. Click "next", as shown in Fig.1(c).

Set the input clock frequency inclk0 to 5MHz, and then click "next", as shown in Fig.2 (a). Add the "areset" signal to remove the lock on the output, as shown in Fig.2 (b).
On the CLK C0 page, we check use this clock to enable CLK C0 port and set the output clock frequency and phase parameters as follows: clock multiplication factor is set to 2 and clock division factor is set to 1, which means that the input clock is frequency doubled. You can also select enter output clock frequency to directly output the required clock frequency value, and click "next". On the CLK C1 page, we check use this clock to enable the CLK C1 port and set the output clock frequency and phase parameters as follows: the clock multiplication factor is set to 1, and the clock division factor is set to 2, which means that the input clock is divided into two frequencies. You can also select enter output clock frequency to directly output the required clock frequency value, and click "next". On the CLK C2 page, we check use this clock to enable CLK C2 port and set the output clock frequency and phase parameters as follows: clock multiplication factor is set to 1, clock division factor is set to 2, which means that the input clock is divided into two frequencies. You can also select enter output clock frequency to directly output the required clock frequency value. In the clock phase shift column, the default value is 0. Fill in 90, which mean the phase difference of 90 degrees. Click "next".
Finally, select generate *.bsf and *.v files, as shown in Fig.3(d), and click finish. At this time, the pll macroblock is added.

In Quartus II's Project Navigator window, we can see that macroblock file pll.qip is added to the project automatically. The addition process of macroblock clk.qip is the same as pll.qip.

3. Application test of DPLL
In order to verify the working characteristics of this digital phase-locked loop, we draw the principle block diagram of digital phase-locked loop as shown in Fig.4.
Fig. 4 Principle block diagram of digital phase locked loop

After compiling the project program, download it to the development board AC101, open the "SignalTap II Logic Analyzer" to analyze and verify the function of DPLL. The digital waveform is shown in Fig. 5.

In Fig. 5(a), fout0 is the reference clock, fout1 is the frequency doubling signal of fout0, and fout2 is the frequency division signal of fout0.

In Fig. 5(b), fout0 is the reference clock, fout2 and fout3 are frequency division signals of fout0. Fout3 has a 90 degrees phase shift based on fout2, which is consistent with the setting when adding "PLL phase shift ".

4. Conclusion
With the development of modern integrated circuit technology, PLL has become a very important part of IC design, so the research of PLL has positive practical significance.

In this paper, PLL macroblock is used to realize the functions of frequency division, frequency doubling and phase locking. Two macroblocks are generated.

(1) The first macroblock, CLK macroblock, divides the 50M clock by 10 to generate a 5M reference clock CLK signal.

(2) The second macroblock, pll macroblock, its C0 port divides the 5M clock 2 times and C1 port doubles the 5M clock, both of which have no phase offset. The C2 port has a 90 degrees phase offset based on the frequency division of 5M clock.

Through the analysis of logic analyzer, it has better digital waveform output results.

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