Multi-Layer High-K Gate Stack Materials for Low $D_{it}$ 4H-SiC Based MOSFETs

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**Abstract.** Metal-oxide-semiconductor capacitors with single and multi-layer high-K gate dielectrics on Si (0001) face of n-type 4H-SiC substrates have been investigated. Multi-layered nanolaminated gate-stack comprises alternating ultrathin (6nm) $\text{Al}_2\text{O}_3$ and $\text{HfO}_2$. A 5nm thick interfacial silicon oxynitride is deposited prior to laminated films to investigate interface trap properties and tuning of flat band voltage. Total thickness of gate-stack films including interfacial layer is 55nm. The thermal stability of multi-layered nanolaminated film is investigated using XTEM. Localized crystallization of $\text{HfO}_2$ is visible after RTA at 900°C while $\text{Al}_2\text{O}_3$ remains fully amorphous. Some of $\text{HfO}_2$ grains have extended into $\text{Al}_2\text{O}_3$ layer but was not able to crossover. The measured accumulation capacitance of 55nm thick gate dielectric shows a capacitive effect. The effective dielectric constant value of 9.6 and an equivalent oxide thickness of 22nm from high-frequency capacitance-voltage measurements. A positive flat band voltage ($V_{FB}$) of 12.2V and 10.6V are observed from both single layer $\text{HfO}_2$ and $\text{Al}_2\text{O}_3$ dielectrics, respectively due to presence of negatively charged oxygen interstitial defects generated during atomic layer deposition process. However, $V_{FB}$ shifted towards negative voltage -7.6V for multi-layered $\text{Al}_2\text{O}_3/\text{HfO}_2$ stacks probably associated with positive Al and Hf interstitials at interface of $\text{Al}_2\text{O}_3/\text{HfO}_2$. Ultrathin interfacial oxynitride films is effective to reduce $D_{it}$ to 3x$10^{11}$/eVcm$^2$ and tuning of $V_{FB}$. The breakdown field of stacked gate dielectric on 4H-SiC is 10.0 MV/cm.

**Introduction**

Silicon carbide is one of the most promising semiconductor materials used commercially for fabrication of high-power, high frequency, and high-temperature MOSFETs because of its wide band gap, high breakdown field, high thermal conductivity and ability to grow thermal $\text{SiO}_2$ for gate insulator. However, high temperature thermal oxidation processes cause residual carbon related defects at and near the $\text{SiO}_2/\text{SiC}$ interface leading to high interface state density ($D_{it}$) and mobility degradation [1]. In addition, 2.5 times higher dielectric constant of SiC than $\text{SiO}_2$ predominantly increases electric field at gate insulator by the same order. These issues can be resolved through integration of high-K gate stacks with dielectric constant higher than that of SiC so that the electric field at the gate stack will be lower than the adjacent SiC and thus reduces dielectric stress. Lori et al. studied several high-K gate stacks on SiC using MOCVD and PVD techniques but all the gate stack materials resulted in high gate leakage current [2]. Recent studies on (AlN) shows N-related defects leading to significant hole conduction. Hf was then incorporated into AlN to form HfAlN to reduce N-related defects and to improve insulating properties of the dielectric [3-4]. In this work, we developed multi-layer high-K gate dielectrics for 4H-SiC MOSFETs applications.
Experiment

Metal-oxide-semiconductor (MOS) capacitors were fabricated on Si-face (0001) n-type 4H-SiC substrates with 10-µm thick epitaxial layer. The samples were cleaned using piranha solution (H₂SO₄:H₂O₂=3:1) at 130°C for 10 minutes followed by rinsing with DI water and drying using N₂ gun. Native oxide was removed using dilute HF (DI:HF=50:1) for 60 sec prior to dielectric deposition. Multiple stacks of Al₂O₃/HfO₂ with an interfacial oxynitride (SiOₓNᵧ) layer were deposited in different combinations using atomic layer deposition (ALD). Fig.1 shows a physical cross-section view of stack of the gate laminate (A/B/A/B type) along with its corresponding band-diagram.

The atomic layer deposition (ALD) process involved cycling of precursor and reactant to achieve deposition of controlled and highly conformal layers at the atomic level. Cyclic nature of the deposition with alternate switching between Al₂O₃ and HfO₂ is thought to minimize pinhole defects in the film. MOS capacitors were then fabricated on a (0001) Si-face of 4H-SiC with 10µm thick N-doped homo-epilayer deposited on highly doped n-type substrate. A stack of Ni/Ti/Ni metal was evaporated on front side using a shadow mask to create MOS capacitor top electrodes, with blanket metal deposition on the substrate backside for the back contact. Samples were annealed at different temperatures to study the temperature stability of the gate stack and effect on Dᵦ. Temperature stability is absolutely needed as silicide formation on SiC MOSFET is a high-temperature step (900 to 1000°C) and that occurs after gate stack formation.

Results and Discussions

The microstructural analysis to examine the interfaces of laminated multi-layered stacks after fabricaion of MOSCAP devices annealed at 900°C using transmission electron microscopy (TEM). The interfaces of alternating stacks of materials are distinctly maintained as illustrated in cross-sectional TEM images in Fig. 2 (a). The localized lattice fringes due to the crystallization of HfO₂ after RTA is observed in higher magnification TEM image (Fig 2(b)) while Al₂O₃ remained fully amorphous. Some of the grains extended towards Al₂O₃ layer but were not able to crossover the Al₂O₃ layer. The bottom SiOₓNᵧ layer remains smooth and amorphous.

Fig.3 shows the high frequency capacitance-voltage (C-V) characteristcs of several dielectric films. The slow rise of capacitance from inversion to accumulation is contributed by several bulk charges and interface traps, and further development work is required to mitigate this issue. The measured
accumulation capacitance of 55 nm thick gate dielectric gives an effective dielectric constant value of 9.6 and an equivalent oxide thickness of 22 nm using high frequency C-V data as shown in Fig. 3.

Fig. 3. Normalized C-V char. of different high-K gate stacks on 4H-SiC measured at 100 kHz.

Fig. 4. Plot of \( \left( \frac{C_{di}}{C_m} \right)^2 - 1 \) vs VG to extract \( V_{FB} \).

\( V_{FB} \) is extracted from experimental CV curve using the relationship in equation (1)

\[
\left( \frac{C_{di}}{C_m} \right)^2 - 1 = \frac{C_{di}^2}{qN_{DE} \varepsilon_0} (V_G - V_{FB})
\]

where \( C_{di} \) is the dielectric capacitance at accumulation and \( C_m \) the measured capacitance of the gate-stacks [5]. The plots of \( \left( \frac{C_{di}}{C_m} \right)^2 - 1 \) vs \( V_G \) for different gate stacks are shown in Fig. 4. The intersection with \( V_G \) axis of the linear extrapolation of the graph corresponds to \( \left( \frac{C_{di}}{C_m} \right)^2 - 1 = 0 \) giving \( V_G = V_{FB} \). The single HfO\(_2\) and Al\(_2\)O\(_3\) dielectrics show positive \( V_{FB} \) which indicates presence of negative charges in the films. Oxygen interstitial defects in dielectric oxide films generated during the ALD process are known to be negatively charged and could possibly be the reason for high fixed negative charges in the film [6]. A high negative \( V_{FB} \) is then observed for A/B/A/B type Al\(_2\)O\(_3\)/HfO\(_2\) stacks. The nano laminate stacks with mild intermixing/doping at the interface of Al\(_2\)O\(_3\)/HfO\(_2\) generate more positive Al and Hf interstitial causing \( V_{FB} \) shifts in the negative direction. It was presumed that the \( V_{FB} \) shift is largely controlled by interfacial trap charges. To solve the large \( V_{FB} \) shift issue an interfacial SiO\(_x\)N\(_y\) layer was introduced on the SiC surface before deposition of multilayer stacks. As a result, a significant recovery in \( V_{FB} \) was observed, as shown in Fig 4. The \( V_{FB} \) tuning process demonstrated here is an important step towards implementation of high-k gate stacks on SiC substrate.

The interface state density is extracted using Hill–Coleman conductance method [7,8]

\[
D_{it} = \frac{2}{qA} \left( \frac{G_{m,\text{max}}}{\omega C_{di}} \right)^{\frac{1}{2}} \left( 1 + \frac{C_m}{C_{di}} \right)^{\frac{1}{2}}
\]

where \( G_{m,\text{max}} \) is the peak conductance value, \( C_m \) the corresponding capacitance at the peak gate bias, and \( C_{di} \) is dielectric capacitance at accumulation. Fig. 5 shows the \( G_g-V_g \) characteristics of different dielectric stacks used to extract interface traps.
The interface state density extracted using equation (2) from the measured values of capacitance and conductance for different high-K stacks are compared with other reported results and illustrated in Fig. 6. The SiOxNy interfacial layer with Al2O3/HfO2 laminate is effective to reduce D_{it} to 3x10^{11}/eVcm^2, which is an order of magnitude lower than D_{it} values previously reported on high-K [7-11] and other gate stacks in this work.

Fig. 7 shows the Jg-Vg characteristics of different gate stacks measured under accumulation. Low gate leakage current density of 0.1µA/cm^2 at V_G = 50V demonstrates high gate dielectric integrity. The breakdown field of stacked gate dielectrics on 4H-SiC is 10.0 MV/cm. The thermal stability of SiOxNy/Al2O3/HfO2 gate stack was investigated by post deposition rapid thermal anneal in N2. It was found that the gate stack is fully stable up to 800°C with slight degradation of flat band voltage (V_{FB}) at 900°C probably due to the localized crystalization of HfO2 as seen in TEM. No gate leakage current degradation was observed after post deposition high temperature annealing (Fig. 8), demonstrating robust thermal stability against high-temperature RTA.

Summary

The effect of ultrathin SiOxNy interfacial layer with multi stack nanolaminated HfO2/Al2O3 films and standalone Al2O3 and HfO2 gate stacks were systematically investigated. Excellent thermal stability was observed for the multilayer nano laminated film. The interfacial oxynitride film is effective to reduce D_{it} to 3x10^{11}/eVcm^2 and tuning of V_{FB}. In summary, we developed multi-layered high-K gate stack technology with tuneable V_{FB} and low D_{it} for high-performance SiC power MOSFETs.

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