Synthesizing Number Generators for Stochastic Computing using Mixed Integer Programming

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Abstract—Stochastic computing (SC) is a high density, low-power computation technique which encodes values as unary bitstreams instead of binary-encoded (BE) values. Practical SC implementations require deterministic or pseudo-random number sequences which are optimally correlated to generate bitstreams and achieve accurate results. Unfortunately, the size of the search space makes manually designing optimally correlated number sequences a difficult task. To automate this design burden, we propose a synthesis formulation using mixed integer programming to automatically generate optimally correlated number sequences. In particular, our synthesis formulation improves the accuracy of arithmetic operations such as multiplication and squaring circuits by up to 5x and 20x respectively. We also show how our technique can be extended to scale to larger circuits.

I. INTRODUCTION

Stochastic computing (SC) is an emerging computation technique which offers a low power, compact, and error tolerant alternative to conventional binary-encoded (BE) computation. In SC, values are encoded as unary bitstreams (time series of 1s and 0s). The value \( p_X \) of a bitstream \( X \) is interpreted as the sum over the weights of each position in the bitstream divided by the bitstream length. For instance, the bitstream \( X = 10100100 \) has value \( p_X = 0.375 \) if we weight 1s as +1 and 0s as 0. This unary encoding allows for compact implementations of arithmetic operations such as multiplication. For instance, given two input bitstreams \( X \) and \( Y \), a multiplier can be implemented using a two-input AND gates since the resulting bitstream \( Z \) has value \( p_Z = p_X p_Y \). The multiplier is only accurate if \( X \) and \( Y \) are uncorrelated otherwise the fundamental assumption that \( p_Z = p_X \wedge p_Y = p_X p_Y \) does not hold.

To generate bitstreams, we use stochastic number generators (SNGs). An SNG is realized by a comparator that takes a number sequence and compares it against the target value to be encoded. Original definitions of SC assume number sequences are generated using purely random noise sources \[7\]. However, practical implementations of SC use deterministic or pseudo-random sources which yield more accurate results than purely random noise sources \[8, 13\]. The selection of number sequences for SNGs is important since correlated or uncorrelated number sequences will generate correlated or uncorrected bitstreams respectively. The correlation between bitstreams governs the functionality and accuracy of arithmetic operations in SC, and each arithmetic operation in SC has a correlation under which it is most accurate.

The key challenge is that manually engineering optimally correlated SNGs requires exploration of an exponentially large design space. For instance, exhaustively searching through all number sequences of length of 16 would mandate evaluating \( 16! \approx 20 \) trillion potential number sequences. As a result, existing work relies on a handful of number sequences with desirable correlation properties and reasonable implementation costs such as low discrepancy sequences, linear feedback shift registers (LFSRs), and pulse-width modulated analog signals \[14\]. This leaves a large space of number sequences which may yield more accurate results than known number sequence combinations.

This paper proposes an automated method for synthesizing SNG number sequences using mixed integer programming to synthesize accurate arithmetic operations. Our synthesis formulation generates optimally accurate number sequences for arithmetic operations such as multiplication and squaring. More importantly, our technique eliminates the design burden of selecting properly correlated number sequences for SC circuits. Our synthesis formulation can also be extended to synthesize RNG number sequences for larger circuits.

Our contributions are as follows: (1) A general mixed integer program formulation for synthesizing optimal SNG number sequences. (2) More accurate SC multiplication, and squaring circuits using synthesized number sequences. (3) Synthesis extensions to improve scalability to larger circuits.

II. BACKGROUND

This section provides background on stochastic computing, impact of correlation, and the role of SNGs.

A. Stochastic Computing Basics

Stochastic computing (SC) is a computing technique proposed in the 1960s by Gaines \[7\]. Unlike binary-encoded (BE) computation, SC relies on unary bitstreams (time series of 1s and 0s) or stochastic numbers (SNs) to encode values. Given an SN \( X \), the encoded value of the SN \( p_X \) is defined as the sum over each position in the SN length divided by the total length of the SN \( N \).

SNs typically either use unipolar or bipolar encodings. In unipolar encodings, zeros in the SN are weighted as 0 and ones are weighted as +1; this limits unipolar encodings to the positive range \([0, 1]\). For instance, the SN \( X = 10100000 \) has value \( p_X = 0.25 \) since there are six 0s, two 1s, and the SN length \( N = 8 \). In contrast, bipolar encodings weight zeros as \(-1\) and ones as \(+1\), allowing them to encode the range \([-1, +1]\). For example, the same SN \( X = 10100000 \) has value \( p_X = -0.5 \).
A typical end-to-end computation pipeline using SC is shown in Fig. 1. In order to generate SNs, BE values are first processed by a stochastic number generator (SNG) which consists of a number sequence generator and digital-to-stochastic (D/S) converter. The number sequence generator is responsible for producing the number sequence that drives digital-to-stochastic (D/S) converters to generate SNs. D/S converters are commonly implemented by a comparator which takes the target BE value and the number sequence generator output to construct an SN of the target value. It is worth noting that the comparators can be replaced by other probability shaping circuitry (e.g., chain of multiplexors) with equivalent results. Once SNs are generated, they can be used to perform arithmetic in the SC domain before they are converted back to the BE domain. To convert from SC to BE, we use stochastic-to-digital (S/D) converters which are implemented by a counter.

Unipolar multiplication in SC is implemented using a two-input AND gate (Fig. 1b). Notice that the multiplication is only accurate because the inputs are uncorrelated. Using correlated input SNs results in errors which illustrate one of the principles design challenges of SC: mitigating errors due to unfavorable correlation (discussed next). Finally, what SC gains in lower power and higher density, it loses in terms of run time since SNs take multiple cycles to process.

The choice of number sequence when generating an SN is important as it governs the initial correlation between SNs. Two SNs generated using the same number sequence will be positively correlated while two SNs generated from uncorrelated number sequence will be uncorrelated. Since number sequence generators are more expensive than individual SC arithmetic operations designers often amortize their cost by exploiting application data reuse and generating many SNs from the same SNG [8].

**B. Correlation and the Role of Number Sequences**

Correlation between SNs is one of the principle sources of errors in SC. Most SC circuits have an input SN correlation under which they function optimally. For instance, the SC multiplier introduced earlier has an affinity for uncorrelated SNs, otherwise the assumption that $p_{Z} = p_X \wedge p_Y = p_X p_Y$ does not hold and the computation results in errors. Correlation between bitstreams is measured using the stochastic computing correlation (SCC) $\rho$. Given two bitstreams, an SCC of $+1.0$ indicates maximum positive correlation, an $−1.0$ indicates maximum negative correlation, and an SCC of $0.0$ indicates uncorrelated. In general, the closer the correlation of the input bitstreams are to the optimal SCC, the more accurate the computation will be.

As a result, managing and mitigating the impact of unwanted correlation between SNs is a key design challenge in SC. There are three principle methods for controlling correlation in SC: (1) using correlation insensitive circuits, (2) using correlation manipulating circuits [11], and (3) judiciously selecting number sequences for SNGs (this work). The first method - using correlation insensitive circuits - relies on special variants of each arithmetic circuit which are immune to correlation levels such as the adder proposed in [12]. Correlation insensitive circuits trade higher power and area for accuracy, and do not exist for all SC arithmetic operations. The second correlation engineering technique is to insert correlation manipulating circuits between arithmetic operations such as isolators [16], synchronizers, desynchronizers, decorrelators [11], and regenerators. Correlation manipulating circuits are primarily used to change correlation of existing SNs.

The third correlation engineering technique is to judiciously select number sequences for SNGs. Recent work has shown that low discrepancy sequences such as Van der Corput (VDC), Halton [3], and Sobol [13] sequences are desirable since they have good correlation properties. Other useful sequences include linear feedback shift registers (LFSRs), and ramp sequences [11], [6]. In addition, there are several unconventional SNGs such as pulse-width modulated signals [14], rotated bitstreams [9], and pre-generated bitstreams [4]. Beyond known techniques and sequences, there are few general methods for designing deterministic number sequences for SC circuits. Automatically synthesizing number sequences for a target function and circuit in SC is the focus of this paper.

Finally, for combinational SC circuits, it is also possible to rotate or swap number positions within each number sequence to yield equivalently correlated bitstreams and identical computation accuracy. For instance, two number sequences $S_X = 0, 1, 2, 3$ and $S_Y = 0, 3, 1, 2$ would produce iso-accurate results as the number sequences $S'_X = 3, 0, 1, 2$ and $S'_Y = 2, 0, 3, 1$ (rotated versions). We can also swap the number positions (ex. $S''_X = 0, 2, 1, 3$ and $S''_Y = 0, 1, 3, 2$) and obtain equivalently accurate results. As long as the relative position of numbers between the number sequences are preserved, the sequences produce iso-accurate results since correlation between the number sequences is preserved. We refer to this property as relative ordering invariance between two number sequences which will become important later. This property does not hold for sequential circuits since state elements are sensitive to autocorrelation which is not preserved under these transformations.

**III. Synthesis Formulation**

This section outlines our mixed integer programming (MIP) problem formulation used to synthesize number sequences.
We now define the MIP constraints used in our synthesis which maximize or minimize the objective function. If no values constraints this set of constraint as the formulation to generate number sequences. Instead of directly produce two integer number sequences \( h(X, Y) \) into its equivalent MIP formulation and set the objective to minimize absolute error. We assume a set of constraints \( H_{X,Y} \) that enforces the hardware functionality of \( h(X, Y) \). MIP formulations of Boolean logic gates such as AND, OR, NOT, and XOR are shown in Table I multiplexors (MUX) use compositions of basic logic gates. State elements like D-flip-flops (DFFs) are implemented by passing the previous cycle variable in the SN. New indicator variables are introduced as necessary to express each constraint. The error is captured by:

\[
\forall n, m \in [0, N] : H_{n,m} = \sum_{j=0}^{N-1} h(X_{n,j}, Y_{m,j})
\]

\[
\forall n, m \in [0, N] : C_{n,m} = H_{n,m} - \text{enc}(f(\text{dec}(n), \text{dec}(m)))
\]

Where \( C_{n,m} \) captures the error between the target functionality and the resulting SNs of the synthesis formulation. An encoding function \( \text{enc}(pZ) \) converts the function result \( pZ = f(pX, pY) \) to the number of 1-bits expected in the output SN \( Z \). Similarly, an inverse function \( \text{dec}(pZ) \) converts the number of expected 1-bits in an SN \( Z \) back to a value \( pZ \). For unipolar circuits, \( \text{enc}(p) = N \cdot p \) because \( p \in [0, 1] \) whereas \( H_{n,m} \) is in the range \([0, N]\). For bipolar circuits, \( \text{enc}(p) = N \cdot (p + 1)/2 \) because \( p \in [-1, 1] \). We then minimize the cost over the absolute error as the objective function.

\[
\text{minimize } \sum_{n=0}^{N} \sum_{m=0}^{N} |C_{n,m}|
\]

The absolute value function is implemented using two auxiliary variable per term. Given a cost term \( C_{n,m} \), we define two auxiliary variables \( t_{n,m,+} \) and \( t_{n,m,-} \) and impose the constraints:

\[
\forall n, m \in [0, N] : t_{n,m,+} - t_{n,m,-} = C_{n,m}
\]

1Mean squared error (MSE) formulations are realized using quadratic programming but are much slower. We find that average absolute error approximates MSE well.

2An auxiliary variable is a new temporary variable.

### A. Problem Formulation

Linear Programming (LP) is an optimization technique that models a problem as a set of linear constraints over symbol variables, and a linear objective function. We use a variant known as Mixed Integer Programming (MIP) where variables are restricted to be either integer or real-valued. The LP solver attempts to assign values to variables so that they satisfy the constraint set. Feasible solutions are variable assignments which satisfy all constraints; optimal solutions are feasible solutions which maximize or minimize the objective function. If no possible solution exists, the solver returns infeasible.

Our synthesis formulation defines a MIP problem that takes two input specifications: (1) a real-valued function specification, \( f(pX, pY) \), and (2) a hardware specification \( h(X, Y) \). The function specification \( f(pX, pY) \) defines the expected value of the output SN given the input SN values. In contrast, the hardware specification, \( h(X, Y) \), is a Boolean function that specifies the behavior of the underlying hardware circuit. Given these specifications, the goal of our synthesis formulation is to produce two integer number sequences \( S_X = \{x_1, ..., x_N\} \) and \( S_Y = \{y_1, ..., y_N\} \) for the SNGs of \( X \) and \( Y \) respectively. Each \( x_i, y_i \in \mathbb{N} \) is within the range \([0, N]\) and is unique within its sequence. We would like \( S_X \) and \( S_Y \) to approximate \( f(pX, pY) \) when used to generate the SNs \( X \) and \( Y \) for the hardware circuit described by \( h(X, Y) \). For instance, to synthesize the optimal number sequences for SC multiplication using a two-input AND gate, we would specify \( f(pX, pY) = pXpY \) and \( h(X, Y) = X \land Y \). Finally, we use real-valued variables because we found the ILP solver performance to be better when using integer values.

### B. Solver Constraints

We now define the MIP constraints used in our synthesis formulation to generate number sequences. Instead of directly synthesizing the number sequence itself, we synthesize the actual SNs that correspond to each value. To encode the number sequences \( S_X \) and \( S_Y \), we define two symbolic matrices of Boolean variables denoted \( X_{i,j} \) and \( Y_{i,j} \) where \( i \) denotes the row index and \( j \) denotes the SN offset. These two symbolic matrices will encode the number sequences for the \( X \) and \( Y \) SNGs and are constrained such that:

\[
\forall i \in [0, N], j \in [0, N] : X_{i,j} \in \{0, 1\}, Y_{i,j} \in \{0, 1\}
\]

The \( i \)th row of each matrix effectively encodes the SN encoding for the value \( i/N \). Under this encoding, the sum of each row must equal \( i \) since, under unipolar SC representations, each position that is 1 in the SN has a weight of +1. We refer to this set of constraint as the value constraints which are:

| Gate | Constraint Encoding |
|------|---------------------|
| \( X = \text{AND}(X, Y) \) | \( Z \geq X + Y - 1, Z \leq X, Z \leq Y, 0 \leq Z \leq 1 \) |
| \( X = \text{OR}(X, Y) \) | \( Z \leq X + Y, Z \geq X, Z \geq Y, 0 \leq Z \leq 1 \) |
| \( X = \text{XOR}(X, Y) \) | \( Z \leq 2 \cdot X \cdot Y, 0 \leq Z \leq 1 \) |
| \( X = \text{NOT}(X) \) | \( Z = 1 - X, 0 \leq Z \leq 1 \) |

### TABLE I: Constraint encodings for basic logic gates.

| Gate | Constraint Encoding |
|------|---------------------|
| \( Z = \text{AND}(X, Y) \) | \( Z \geq X + Y - 1, Z \leq X, Z \leq Y, 0 \leq Z \leq 1 \) |
| \( Z = \text{OR}(X, Y) \) | \( Z \leq X + Y, Z \geq X, Z \geq Y, 0 \leq Z \leq 1 \) |
| \( Z = \text{XOR}(X, Y) \) | \( Z \leq 2 \cdot X \cdot Y, 0 \leq Z \leq 1 \) |
| \( Z = \text{NOT}(X) \) | \( Z = 1 - X, 0 \leq Z \leq 1 \) |

We also introduce monotonicity constraints which require the values in each column of \( S_X \) and \( S_Y \) to increase monotonically. Suppose two SNs \( X_i \) and \( X_{i+1} \) encoding the values \( i/N \) and \( (i+1)/N \) respectively and are generated from the same number sequence \( S_X \). The key insight is that if a bit at position \( n \) in \( X_i \) is 1, then the bit at position \( n \) must also be 1 in \( X_{i+1} \). This is because if \( S_X[n] < i/N \) for a given position \( n \), then it must be the case that \( S_X[n] < (i+1)/N \). Therefore:

\[
\forall i \in [0, N], j \in [0, N] : X_{i,j} \leq X_{i+1,j}, Y_{i,j} \leq Y_{i+1,j}
\]

This constraint is a consequence of choosing comparator as the probability shaping circuit within the SNG. The monotonicity constraint combined with the value constraints enforces uniqueness that (1) no two SNs encode the same value, and (2) each encoded number within each sequence is unique.

To encode circuit functionality, we convert the hardware specification \( h(X, Y) \) into its equivalent MIP formulation and set the objective to minimize absolute error. We assume a set of constraints \( H_{X,Y} \) that enforces the hardware functionality of \( h(X, Y) \). MIP formulations of Boolean logic gates such as AND, OR, NOT, and XOR are shown in Table I multiplexors (MUX) use compositions of basic logic gates. State elements like D-flip-flops (DFFs) are implemented by passing the previous cycle variable in the SN. New indicator variables are introduced as necessary to express each constraint. The error is captured by:

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Where \( C_{n,m} \) captures the error between the target functionality and the resulting SNs of the synthesis formulation. An encoding function \( \text{enc}(pZ) \) converts the function result \( pZ = f(pX, pY) \) to the number of 1-bits expected in the output SN \( Z \). Similarly, an inverse function \( \text{dec}(pZ) \) converts the number of expected 1-bits in an SN \( Z \) back to a value \( pZ \). For unipolar circuits, \( \text{enc}(p) = N \cdot p \) because \( p \in [0, 1] \) whereas \( H_{n,m} \) is in the range \([0, N]\). For bipolar circuits, \( \text{enc}(p) = N \cdot (p + 1)/2 \) because \( p \in [-1, 1] \). We then minimize the cost over the absolute error as the objective function:

\[
\text{minimize } \sum_{n=0}^{N} \sum_{m=0}^{N} |C_{n,m}|
\]

The absolute value function is implemented using two auxiliary variable per term. Given a cost term \( C_{n,m} \), we define two auxiliary variables \( t_{n,m,+} \) and \( t_{n,m,-} \) and impose the constraints:

\[
\forall n, m \in [0, N] : t_{n,m,+} - t_{n,m,-} = C_{n,m}
\]

1Mean squared error (MSE) formulations are realized using quadratic programming but are much slower. We find that average absolute error approximates MSE well.

2An auxiliary variable is a new temporary variable.
TABLE II: Number sequence synthesis benchmarks, specifications, and average absolute error (lower is better). Synthesized solutions are as accurate or more accurate than baseline solutions. † indicates feasible but not optimal solutions.

| Function | Encoding | Function | Hardware | Synthesized Error (Our Work) | Baseline Error (Prior Work) |
|----------|----------|----------|----------|----------------------------|-----------------------------|
| Multiplier | Unipolar | $f(p_X, p_Y)$ | $Z = h(X, Y)$ | $N=16$ $N=32$ $N=64$ $N=128$ | $N=16$ $N=32$ $N=64$ $N=128$ |
| Adder | Bipolar | $(p_X + p_Y)$ | $Z = XNOR(X, Y)$ | 0.016 0.0092 0.0049† 0.0027† | 0.032 0.020 0.012 0.0068 |
| Squarer | Unipolar | $p_X^2$ | $Z = MUX(X, Y, R)$ | 0.016 0.0078 0.0039 0.0020 | 0.016 0.0078 0.0039 0.0020 |
| Saturating Adder | Unipolar | $\min(1, p_X + p_Y)$ | $Z = OR(X, Y)$ | 0.015 0.0076 0.0036 0.0020† | 0.030 0.030 0.034 0.040 |

∀$n, m \in [0, N] : |C_{n,m}| = t_{n,m}^+ + t_{n,m}^-$

∀$n, m \in [0, N] : t_{n,m}^+ \geq 0, t_{n,m}^- \geq 0, C_{n,m} \geq 0$

If $C_{n,m}$ is positive then $t_{n,m}^+ = C_{n,m}$ and $t_{n,m}^- = 0$, otherwise $t_{n,m}^+ = 0$ and $t_{n,m}^- = -C_{n,m}$. The absolute value of this cost component is then expressed as $t_{n,m}^+ + t_{n,m}^-$. Since we minimize over the cost terms, the solver forces either $t_{n,m}^+$ or $t_{n,m}^-$ to zero since other assignments would be suboptimal.

The resulting number sequences $S_X$ and $S_Y$ are recovered from the variables $X_{i,j}$ and $Y_{i,j}$ by summing over each column and subtracting the sum from $N$. Recall that SNs are generated by taking the number sequence value $s$ and checking if it is less than the target value $x$. If $s < x$, the D/S converter emits a 1 otherwise it emits a 0 which means the number of zeros is proportional to the number of values where $s < x$. More precisely:

∀$i \in [0, N] : S_X[i] = N - \sum_{j=0}^{N} X_{i,j}, S_Y[i] = N - \sum_{j=0}^{N} Y_{i,j}$

C. Optimization Constraints

We now introduce two constraint optimizations to improve the run time of the synthesis formulation.

**Initial and Final Sequences:** Recall that the sum of each row is equal to the row index; thus the sum of row 0 must also be zero and the sum of row $N$ must be $N$. The only way to enforce the constraints $\sum_{j=0}^{N-1} X_{0,j} = 0, X_{N,j} = 1$ is $\forall j \in [0, N] : X_{0,j} = 0, X_{N,j} = 1$ since variables are either 0 or 1, and there are $N$ positions in the row. This modestly improves solver time by reducing the number of variables.

**Relative Ordering Invariance:** Recall that, for combinational circuits, numbers in two number sequences can be rotated or swapped as long as the relative pairing of numbers is preserved. This means there are many equivalent solutions with the same objective function value. This can be problematic for the solver since it must expend time exploring each equivalent solution and deduce that they all have the same objective function value.

Fortunately, we can exploit relative ordering invariance to eliminate equivalent solutions by initializing one of the number sequences $S_X$ to any number sequence (ex. ramp sequence {0, 1, 2, 3, ..., N-1}). This reduces the number of symbolic variables to solve for by half since it is no longer necessary to solve for $\forall i, j : X_{i,j}$. Once a solution $S_Y$ is synthesized, we can rotate the number sequences or swap the number positions to transform them into solutions with the same correlation.

IV. Evaluation

This section defines methodology, presents accuracy results, and evaluates the power and area of the synthesized number sequences.

A. Methodology

We evaluate synthesis problems for known arithmetic SC circuits to verify that our synthesis formulation is correct and synthesizes more accurate number sequences for existing arithmetic operations. Our synthesis formulation is implemented on top of IBM CPLEX version 12.8.0. We ran our benchmarks on Microsoft Azure F72 v2 virtual machines running Ubuntu 16.04. To evaluate correctness, we use the synthesized number sequences to evaluate the average absolute error across all possible input value combinations. We compare the average absolute error against those produced by using known number sequences in prior work.

For “difficult” synthesis instances that take intractable amounts of time, we either relax the optimality gap $g$ or bound the computation time. The optimality gap $g$ is an ILP solver parameter that allows it to return a feasible solution within $g$ of the estimated optimal objective function value. For instance, setting $g = 0.05$ expresses that it is acceptable to return a solution within 5% of optimal. We also restrict computation times. In these cases, the solver returns a feasible solution and the estimated optimality gap between the returned solution and the optimal solution. Both these techniques trade off optimality for speed for “difficult” instances.

B. Results

We now present accuracy results for our synthesized sequences. For SC circuits like maximum, division, and minimum, our synthesis formulation generates positively correlated results and match the known optimal solutions in the literature [5], [2]. For saturating addition, our formulation correctly identifies maximally negatively correlated number sequences which results in no accuracy errors. For multiplication, the synthesis formulation finds number sequences which yields in more accurate results for both unipolar and bipolar encoding cases (Table II). While our formulation optimizes average absolute error, our results are still comparable or more accurate than...
prior work \cite{12} in terms of mean squared error (MSE). Finally, we find that synthesis times generally increase exponentially with search space size.

Examples of synthesized sequences for multipliers with SN length of \( N = 16 \) are shown in Table \( \text{III} \). Our synthesized results for multiplication achieve better overall accuracy by \( 2.5 \times \) over previously solutions using a ramp, Van der Corput, or Halton sequences \cite{12} \( \text{Fig. 2} \). Our results also show we can generate more accurate bitstreams for the squaring function by up to \( 20 \times \) \( (N = 128) \) which is better than using existing number generators.

The key strength of our formulation is that provided sufficient computation resources it can automatically identify optimally correlated deterministic number sequences. Table \( \text{III} \) compares the SCC for unipolar and bipolar multiplication and shows that the average SCC across all SNs generated by synthesized number sequences is better than using the ramp and Halton sequences proposed in \cite{12}.

### C. Power, Area, and Energy

We evaluate the power, area, and energy cost of our synthesized number sequence generators by using Synopsys Design Compiler, IC Compiler, and PrimeTime Power using a 65 nm TSMC library. We compare VDC, Halton3, and LFSR sequences with a lookup table architecture for synthesized number sequences since synthesized sequences have no obvious efficient hardware implementation. For a two-input function, we only need one lookup table to generate \( S_Y \) since we can initialize \( S_X \) to a ramp function and use it to also drive the lookup table. The architecture for this pair of number sequence generators is shown in Fig. 4.

To compare scalability, we evaluate number sequence generators for \( N = 4, 8, 16, 32, 64, 128, 256 \). Fig. 3 shows the power and area comparison of several known number generators. Compared to existing number sequence generators, individual synthesized number sequence generators consume more power and area for \( N = 128 \) length SNs by up to \( 4.7 \times \) and \( 2.5 \times \) respectively; for shorter bitstream lengths, this gap quickly closes. While the relative gaps may appear large, in the context of an end-to-end accelerator, this power and area differential has limited impact.

To measure the overall power and area overhead of our number generators, we evaluate a convolution and matrix-vector multiply kernel. For convolution, we assume a \( 8 \times 8 \) input tile and \( 5 \times 5 \) kernel window. For matrix-vector multiplication, we

![Fig. 2: Multiplication accuracy. Our synthesized number sequences are optimally accurate.](image)

![Fig. 3: Power and area of number generators for \( N = 4, 8, 16, 32, 64, 128, 256 \).](image)

![Fig. 4: (a) Lookup table number generator for synthesized number sequences. (b) A counter serves as both a number generator and lookup table driver.](image)
TABLE III: Synthesized number sequences compared to existing solutions (N=16). Our multiplier sequences on average are more optimally uncorrelated.

| Functionality | Synthesized Sequences (Our Work) | Baseline Sequences (Prior Work) | Synthesized SCC | Baseline SCC |
|---------------|----------------------------------|-------------------------------|----------------|--------------|
| Unipolar      | [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15] | [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15] | 0.0 | 0.45 |
| Multiply      | [6, 13, 1, 10, 8, 3, 15, 4, 11, 0, 12, 7, 5, 14, 2, 9] | [8, 4, 12, 2, 10, 6, 14, 1, 9, 5, 13, 3, 11, 7, 15, 0] | 0.0 | 0.23 |
| Bipolar       | [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15] | [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15] | 0.0 | 0.23 |
| Multiply      | [6, 13, 1, 10, 8, 3, 15, 4, 11, 0, 12, 7, 5, 14, 2, 9] | [0, 5, 11, 2, 7, 12, 4, 9, 14, 1, 6, 11, 2, 8, 13, 4] | – | – |
| Square        | [2, 0, 8, 12, 11, 7, 6, 1, 4, 13, 14, 5, 9, 10, 3, 15] | [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15] | 0.0 | 0.45 |

Fig. 5: Circuit decomposition into subproblems. (a) Fused multiply-add with three inputs decomposed into (b) two subproblems.

since it occurs first in the circuit’s topological order. Given $X_0$ and $X_1$, we exhaustively generate all possible output SNs from the multiplier and record them in a $(N + 1) \times (N + 1) \times N$ dimensional matrix $Y$. Each row in matrix $Y$ corresponds to a possible SN output from subproblem 0.

To synthesize $X_2$ we construct a second synthesis problem. Unlike subproblem 0, we use the output SNs in $Y$ from subproblem 0 as one of the inputs instead of a symbolic matrix corresponding to a number sequence. We still assign a matrix of symbolic variables for $X_2$ and synthesize it. One drawback is that the number of resulting SNs generated by subproblem 0 increases quadratically with SN length. To mitigate this, we deduplicate the rows in $Y$; the key insight is that the first subproblem may generate redundant SNs (identical SNs). The degree of redundancy depends on the encoded computation and hardware specification.

Decompositions present their own trade offs. Using decompositions trades global optimality guarantees for scalability; solutions for each individual gate are still locally optimal. By partially calculating the resulting values after subproblems 0, we eliminate the need to solve for all input number sequences at the same time which improves scalability by reducing the search space size. Unfortunately, the synthesized number sequence results are only optimal for each subproblem and does not guarantee that the synthesized number sequences are optimal for the original circuit.

V. RELATED WORK

Designing number generators for SC has typically been a manual design task that relies on designer insight. Ichihara et al. [8] propose sharing rotated versions of LFSRs to amortize implementation cost over two SNs. Neugebauer et al. [13] propose a new number sequence generator SBoNG which improves autocorrelation and cross correlation of generated SNs. Zhakatayev et al. [17] improve SN implementation cost by using even distribution coding. Kim et al. [10] proposes an SNG that uses an auxiliary RNG to shuffle bits of an existing SN to generate a new SN. However, most of these prior works concentrate on improving implementation cost and/or randomness of number generators, not exploiting the remaining space of number generators. To our knowledge, this work is the first to automatically synthesize optimally correlated, deterministic number sequences for SNs.

VI. CONCLUSIONS

We presented a mixed integer program synthesis formulation for automatically generating optimally correlated number sequences to improve the accuracy of stochastic circuits. Our formulation generalizes to any circuit and removes the design burden of identifying optimally correlation number sequences from the design process. In particular, we show that it yields more accurate multiplication and squaring circuits, and show how it can be extended to larger multiple input circuits.

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