Silicon carbide planar junctionless transistor for low-medium voltage power electronics

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Abstract

This paper proposes a Silicon Carbide (SiC) based planar junctionless transistor (JLT), designed and simulated for low to medium power electronic applications, with a calibrated deck of SiC parameters. The simple structure of this device avoids the fabrication complexity associated with intricate junction geometries of vertical power devices and growth challenges of lateral heterostructure ones. Because of the wide bandgap (WBG) of SiC, the device exhibits a breakdown voltage of 100 V at channel length of 0.1 μm, which may be enhanced, at the cost of operating speed, by increasing the channel length. Compared to commercial enhancement-mode GaN (e-GaN) devices with similar breakdown voltage specification, the proposed device offers lower specific on-resistance ($R_{on,sp}$), and a significant reduction in capacitance due to its naturally self-aligned structure, leading to higher operating speed concluded from the mixed-mode simulations.

1. Introduction

Over the last few decades, new device designs and fabrication techniques have been explored to expand the applicability of SiC-based power devices. The superior material properties of SiC make it an interesting choice especially for high-voltage, high-temperature, and high-frequency applications [1].

On the other hand, Silicon vertical metal-oxide-semiconductor (MOS) transistors and GaN planar transistors are generally used for medium breakdown voltage (<900 V) applications such as LED drivers. Between them, e-GaN planar devices have an edge over their Silicon counterparts [2–4], owing to the high switching frequency, low $R_{on}$, low capacitance, and high breakdown voltage offered by the former. The vertical structure also poses a problem for monolithic integration as all the terminals are not on the same surface [3]. In this regard, the planar device explored in this work might be a preferred choice for LED driver applications. A fully integrated driver and switch with necessary protection circuits can significantly increase the overall speed of the chip, which is in the MHz range for commercial high-frequency drivers today [6].

SiC-based vertical power MOS devices promise very high breakdown voltages [7–9], yet the ON current does not scale up with the breakdown voltage as the channel resistance ($\sim$65% of the on-resistance) is relatively high. This high channel resistance (low channel mobility) is primarily due to the poor quality of the interface between SiC and Silicon Dioxide ($SiO_2$) [10,11]. The reported interface trap density for the SiC/$SiO_2$ interface is $3 \times 10^{11}$ to $9 \times 10^{11}$ eV$^{-1}$ cm$^{-2}$ in the range of 0.2 to 0.6 eV from the conduction band edge [12], which is significantly higher than the Si/$SiO_2$ interface. As mentioned above, a vertical SiC device structure also makes the overall integration more expensive. This can be eliminated with a planar architecture.

JLTs have been widely explored in recent years to tackle the complexity of scaling MOS Field Effect Transistors (FETs) [13]. JLTs eliminate various problems associated with engineering the source/drain, threshold-adjust, retrograde, and pocket implants, such as the difficulty of controlling the doping pattern around junctions of depth 10 nm and beyond, for cutting edge digital logic and other applications [14, 15]. A well-designed JLT also offers a near-ideal subthreshold slope, low leakage current, and low mobility degradation.

In this work, we have used a commercial Technology Computer-Aided Design (TCAD) framework to design and simulate a planar SiC power JLT for low to medium breakdown voltage applications, such as driver circuits...
for LEDs, Single-Photon Avalanche Diodes (SAPD), x-ray detectors, and sensors [16], as well as DC microgrids [17], and auxiliary devices of EVs [18].

2. Simulation setup and device design

Figure 1 shows the structure and design parameters considered for the proposed planar JLT device. The device is doped with n-type dopants of $1 \times 10^{18}$ cm$^{-3}$ concentration, so as to avoid stacking faults [19]. SiO$_2$ dielectric with 1 nm thickness [13] is used as the gate oxide. A p-substrate with a similar doping concentration as the n-layer and a thickness of 10 nm is taken beneath the n-layer to replicate a real fabrication scenario.

We have used the commercial 2D Sentaurus Device (Sdevice) simulator for the device simulations. We have calibrated the SiC parameter deck by matching the experimental transfer characteristic (at $V_{ds} = 0.1$ V) with the device simulation in logarithmic scale (a) and the decreasing trend of field-effect mobility (at $V_g = 18$ V) obtained from simulation which is in line with experimental substrate doping dependence trend (b) [21] for a NO annealed SiC planar MOSFET.

The physical models used for the simulation of the device include Shockley-Read-Hall (SRH) and Auger in the recombination module. The dependence of mobility on temperature, doping, and electric field are incorporated in these simulations. The application and description of the physics models can be found in Sentaurus manual and in the workbench examples for SiC-based devices. The default parameter file for SiC is modified to incorporate the best available experimental data from the literature [22, 23]. The modified equations used for bandgap and auger recombinations are given below.

$$E_g = E_{g0} - \frac{\alpha \times T^2}{\beta + T}$$

where,

$\alpha = 6.5 \times 10^{-04}$ eV K$^{-1}$

$\beta = 1.3 \times 10^5$ K

$E_{g0} = 3.285$ eV

$\chi_0$ (electron affinity) = 3.65 eV
Table 1. SiC material parameters used in this work (where the asterisk denotes modification from the default value).

| Parameter | Quantity | Value |
|-----------|----------|-------|
| $\epsilon$ | Dielectric constant | 9.66 [24] |
| $E_{g00}$ (eV)* | Band gap at 300 K | 3.285 [25] |
| $A_{UGP}$ (cm$^3$/s)$^*$ | Auger-recombination parameter for hole | $2 \times 10^{-31}$ [25] |
| $A_{UGP}$ (cm$^3$/s)$^*$ | Auger-recombination parameter for electron | $5 \times 10^{-31}$ [25] |
| $N_{A0}$ (cm$^{-3}$)$^*$ | SRH concentration dependent lifetime model for electron | $3 \times 10^{17}$ [24] |
| $N_{A0}$ (cm$^{-3}$)$^*$ | SRH concentration dependent lifetime model for hole | $3 \times 10^{17}$ [24] |
| $kappa^{-1}(K \times cm/W)$ | Lattice thermal conductivity | $-0.0327$ [24] |
| $kappa_{e}^{-1}(cm/K)$ | Lattice thermal conductivity | $5.5850e-04$ [24] |
| $kappa_{p}^{-1}(cm/K)$ | Lattice thermal conductivity | $7.7660e-07$ [24] |
| $E_{B00}$ (eV)* | Bandgap narrowing | $9.0000 \times 10^{-3}$ [24] |
| $N_{ref}$ (cm$^{-3}$)$^*$ | Fitting parameter of the impurity scattering | $3.1620 \times 10^{18}$ [25] |
| $N_{300}$ (cm$^{-3}$)$^*$ | Effective density of states (CB) at 300 K | $2.8900e+19$ [24] |
| $N_{300}$ (cm$^{-3}$)$^*$ | Effective density of states (VB) at 300 K | $3.1400e+19$ [24] |
| $\mu_{max}$ (cm$^2$/Vs)$^*$ | Constant mobility model | 950, 124 [26] |
| $\mu_{ref}$ (cm$^2$/Vs)$^*$ | reference mobility in Masetti Model | 40, 15.9 [26] |

Figure 3. Transfer characteristics of the power device at a $V_{ds}$ of 1 V, for the varied thickness of $n$-layer ($X_n$).

$$R_{Auger} = (C_{n,n} + C_{n,p}) \times (n \times p - n_{eff}^2)$$

(2)

$$C_{n,p} = A + B \left( \frac{T}{T_0} \right) + C \left( \frac{T}{T_0} \right)^2$$

(3)

where,

$A = 5 \times 10^{-31}, 2 \times 10^{-31}$ cm$^6$/s

$B = 0.0, 0.0$ cm$^6$/s

$C = 0.0, 0.0$ cm$^6$/s

The parameter values (where the asterisk denotes modification from the default value) that are used for the present simulations are tabulated in table 1.
3. Device results and discussion

The operation of the device shown in figure 1 is controlled with the help of the gate bias. The device is said to be OFF when the thin n-layer is fully depleted of carriers, ideally due to the workfunction difference between the gate electrode and the semiconductor. When the gate voltage is increased, the depletion region narrows, opening up a bulk-like conduction ‘channel’ in the n-layer. It is worth noting that besides the gate voltage, the substrate p–n junction also contributes in controlling the depletion region thickness, and thereby the flow of carriers through the n-layer channel. The n-layer thickness is thus a key design parameter for this device. We have performed simulations for various thicknesses of the n-layer ($X_j$), considering the n-doped region as bulk. The critical thickness of SiC for exhibiting the 2D effects is estimated to be 12 nm using the De Broglie wavelength formula [27, 28], thus $X_j$ is varied from a minimum of 20 nm in our design, so as to preserve the bulk properties of SiC and preclude variability due to quantization. For this calculation, the effective mass of electrons at the bottom of the conduction band is taken as $0.37 \times m_0$ [29].

![Figure 4. Transfer characteristics of the power device at a $V_{ds}$ of 1 V, for varied substrate voltage ($V_{sb}$). The negative increment in $V_{sb}$ increases the reverse bias at the p–n junction thereby decreasing the ON current ($I_{ON}$) and increasing the threshold voltage ($V_{th}$).](image)

The simulated transfer characteristic of the device for various thicknesses of the n-layer ($X_j$) is plotted in figure 3. The plot shows increasing drive current and decreasing threshold voltage with increased $X_j$ value. These results are in agreement with previously reported work [13]. The obtained threshold voltages for various $X_j$ values of the device are tabulated in table 2. Here, they are represented by the upper case alphabets A, B, C, and D, corresponding to the $X_j$ values 20 nm, 30 nm, 50 nm, and 80 nm, respectively. The device ‘D’ has a negative $V_{th}$ (i.e. ON at $V_{gs} = 0$ V), hence it would not be an ideal choice for practical applications owing to the heavy loss possible at zero gate voltage. Thus, we adhere to device ‘C’, a positive threshold voltage device with a relatively large drive current, for further simulations.

We start by looking at the effect of the substrate bias. Figure 4 shows the transfer characteristics of device ‘C’ for different substrate biases (0 V, $-0.5$ V, $-1$ V). A negative increment in $V_{sb}$ increases the reverse bias at the p–n junction, thereby increasing the depletion thickness in the n-layer, increasing the $V_{th}$, and decreasing the $I_{ON}$. The results indicate a scope to tune the effective $X_j$ of the device (viz. the thickness of the bulk-like, non-depleted part of the n-layer) by applying a substrate voltage. Since the $V_{th}$ increases with the negative substrate voltage, it may be possible to have a larger physical $X_j$ without letting the threshold voltage slip into negative values, which

| Device | Thickness of n-layer (nm) | $V_{th}$ (V) |
|--------|--------------------------|-------------|
| A      | 20                       | 0.9         |
| B      | 30                       | 0.7         |
| C      | 50                       | 0.4         |
| D      | 80                       | Negative    |

Table 2. $V_{th}$ of the power device for different thicknesses of the n-layer.
in turn can increase the drive current of the device. Note that the philosophy here is the same as in the standard technique of Active Well Biasing [30].

The output characteristics of the device ‘C’ for different gate biases have been plotted in figure 5. The on-resistance of the device is obtained from the linear region of the output characteristic and the device area

Figure 5. Output characteristics of the power device ‘C’ for different gate biases.

Figure 6. (a) Avalanche increase in current of device ‘C’ shown for three different channel lengths. (b) The electric field in the channel (c) Breakdown voltage of the device ‘C’ with respect to the channel length at \( V_{gs} = 0 \) V. Increased channel length will decrease the drive current, hence the breakdown voltage increases.
(width = 1 μm, length of the device = 0.3 μm) is 3 × 10⁻⁹ cm². The $R_{on,sp}$ of the device is calculated as 0.1 mΩ × cm², three times smaller than an equivalent e-GaN device (detailed comparison is given later) considering the same gate overdrive voltage ($V_{gs} - V_{th}$).

Breakdown simulation (External Resistor Method) of the device has been carried out to estimate the limit of safe device operation. Figure 6(c) shows the estimated breakdown voltage with respect to the channel length simulated for zero $V_{gs}$ voltage. The drain current decreases with an increase in channel length which is evident from the characteristic shown in figure 6(a), therefore the device breakdown voltage increases. The field in the channel at the breakdown voltage is shown in figure 6(b). The breakdown voltage ($V_{br}$) for device ‘C’ of length 0.1 μm is observed to be around 100 V. This increases with the channel length with operating frequency trade-off.

The commercial e-GaN device having a $V_{br}$ of 100 V is reported to have a $R_{on,sp}$ of 0.3 mΩ × cm² approximately [31]. In comparison, for the proposed SiC device with the same $V_{br}$, the $R_{on,sp}$ is three times smaller. The detailed comparison of the proposed SiC-based power device with the existing commercial e-GaN device with similar $V_{br}$ specification [32] is presented in table 3. The input (sum of $C_{gs}$, $C_{gd}$, and $C_{gg}$) and output (sum of $C_{ds}$, $C_{gd}$, and $C_{dd}$) capacitances are obtained from the mixed-mode simulation at the rated voltage. We note that for the purpose of comparing the capacitance, we scale the width of the SiC JLT by a factor of 6 × 10³, so as to match the rated drive current of the e-GaN device for bias voltages $V_{gs} = 2$ V and $V_{ds} = 1$ V. The Baliga figure of merit (BFOM) [33] of the device has improved a factor of 3 and the values are tabulated in Table 3. The FOM ($Q_g \times R_{on}$) [31] is found as 462 pC-K.

From the comparison (table 3), the proposed SiC JLT possesses lower specific-on-resistance, threshold voltage, and capacitance (input and output), and higher intrinsic switching frequency than the commercial e-GaN power device. We find (from mixed-mode simulations of the device) that the input and output capacitance of the SiC JLT power device, in particular, is significantly lower than that of the e-GaN device. As we will see in the next section, this also translates to correspondingly higher intrinsic switching frequency. The

| Parameter                      | e-GaN device | SiC JLT |
|--------------------------------|--------------|---------|
| Input capacitance (pF)        | 14           | 1.5     |
| $(V_{ds} = 50 \text{ V}, V_{gs} = 0 \text{ V})$ |              |         |
| Output Capacitance (pF)       | 6.5          | 0.3     |
| $(V_{ds} = 50 \text{ V}, V_{gs} = 0 \text{ V})$ |              |         |
| Specific-on-Resistance (mΩ × cm²) | 0.3          | 0.1     |
| $(V_{gs}, V_{th} = 3.5 \text{ V})$ |              |         |
| Threshold Voltage (V)         | 1.5          | 0.4     |
| (Range: 0.8 to 2.5 V)         |              |         |
| Intrinsic frequency (GHz)     | 0.7 ($I_{D}/Q_{g}$) | 5       |
| BFOM (MW/cm²)                 | 0.03         | 0.1     |

Figure 7. Schematic of the circuit used for the mixed-mode simulations.
Transfer characteristics [Input (black) and output (red)] of SiC JLT (Device ‘C’) for different periods, rise and fall times of the input pulse ($V_{in}$). The period is 2 ns (for a), 0.2 ns (for b), and 0.02 ns (for c); whereas the rise and fall times are kept at 1 ps (for a and b), and 0.1 ps (for c).

Figure 8.
smaller capacitance of the proposed JLT is due to its simple, naturally self-aligned, structure, sans the field plate overlap that is probably present in the e-GaN device. Thus, the charge (input and output) calculated from the capacitance $C_{gg}$ and $C_{gd}$, and thereby the figure of merit (charge × on-resistance), is smaller. The thermal conductivity ($W/cm \times K$) of SiC material (3.3–4.5) is nearly 3 times higher than both Si (1.5) and GaN (1.3) [34], which may be expected to be a benefit for SiC JLT based devices and modules from a packaging perspective.

4. Circuit results

In order to evaluate the proposed SiC JLT (shown in figure 1) from a circuit perspective, we have performed mixed-mode simulations for the simple test circuit depicted in figure 7. Here, the device is connected in a common-source configuration, such that the circuit (figure 7) acts as a resistive load inverter. The supply voltage ($V_{DD}$) is kept at 10 V, and a square wave of amplitude -5 V to +10 V is applied at the input. The period, as well as the rise and fall times of the input signal, are varied for the simulation. The circuit is simulated to estimate the upper limit of input signal frequency for which the intrinsic device can offer faithful switching. The input signal frequency is varied from 0.5 GHz to 50 GHz with the rise and fall times kept at 1 ps and 0.1 ps. The transfer characteristics of the circuit plotted in figure 8 offer an output voltage swing of $(V_{max}, V_{min}) = (10, 0.23)$ with the chosen resistance. The circuit switches properly for input frequencies up to 5 GHz, but not beyond that. This is due to the low resistive path to the output provided by the parasitic capacitance ($C_{gd}$) at high frequencies, which prevents the device from clean switching (see figure 8(c)) above 5 GHz. Further, we do not observe any change in the maximum switching frequency when we simulate for higher $V_{DD}$ (100 V) with the same circuit (results not shown here). We note that this intrinsic limit of switching frequency of about 5 GHz is almost an order of magnitude greater than that of the benchmark e-GaN device (which we estimate to be about 0.7 GHz from the ratio of drive current to the gate charge). This appears to be consistent with its lower capacitance and on-resistance.

Lastly, the device, as well as the circuit, have also been simulated with the inclusion of trap states (Acceptor type: $1 \times 10^{12} eV^{-1} \text{cm}^{-2}$) [12], with a density that is realistic for the SiC/SiO$_2$ interface. From the device simulation, we observe a positive shift of 0.14 V in the threshold voltage (not shown here). The influence on the circuit is assessed by plotting the switching characteristics over an input voltage (ramp) of -10 V to +10 V (see figure 9), where the output with and without traps follow a similar pattern with negligible deviation. Thus, it can be concluded that the presence of traps does not significantly affect the performance of SiC JLT devices and circuits.

5. Conclusion

In this work, a SiC-based bulk, planar, junctionless power transistor has been designed and simulated with a calibrated deck of parameters. Its planar junctionless architecture avoids the fabrication complexities associated
with the vertical devices and junction geometries. The device offers a breakdown voltage of 100 V at a channel length of 0.1 μm, which can be further enhanced by increasing the channel length. Compared to a commercial e-GaN power device with similar breakdown voltage specification ([31]), the proposed device exhibits lower specific on-resistance, threshold voltage, as well as input and output capacitance, leading to a much higher intrinsic speed of operation. Moreover, the threshold voltage can be adjusted by varying the n-layer thickness and the substrate bias. The order-of-magnitude smaller capacitance for the proposed device in comparison to the commercial e-GaN device, due to its naturally self-aligned structure, leads to a better (lower) figure of Merit (charge × resistance). The mixed-mode simulations reveal an intrinsic switching frequency as high as 5GHz for the device. The inclusion of a realistic trap density at the SiC/SiO₂ interface is seen to have a negligible influence on the device and circuit performance. The large thermal conductivity of SiC, 3 times higher than Si and GaN, may enable monolithic integration of this switching device with the gate driver, and improved packaging. In summary, the proposed planar SiC-based JLT power device might be preferred over commercial e-GaN power devices for some high-speed applications in the low (28V) to medium (900V) voltage ranges, owing to advantages such as ease of fabrication, enhanced packaging density, lower specific on-resistance and capacitances [35].

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