Novel 14-nm Scallop-Shaped FinFETs (S-FinFETs) on Bulk-Si Substrate

Weijia Xu, Huaxiang Yin*, Xiaolong Ma, Peizhen Hong, Miao Xu and Lingkuan Meng

Abstract

In this study, novel p-type scallop-shaped fin field-effect transistors (S-FinFETs) are fabricated using an all-last high-k/metal gate (HKMG) process on bulk-silicon (Si) substrates for the first time. In combination with the structure advantage of conventional Si nanowires, the proposed S-FinFETs provide better electrostatic integrity in the channels than normal bulk-Si FinFETs or tri-gate devices with rectangular or trapezoidal fins. It is due to formation of quasi-surrounding gate electrodes on scalloping fins by a special Si etch process. The entire integration flow of the S-FinFETs is fully compatible with the mainstream all-last HKMG FinFET process, except for a modified fin etch process. The drain-induced barrier lowering and subthreshold swing of the fabricated p-type S-FinFETs with a 14-nm physical gate length are 62 mV/V and 75 mV/dec, respectively, which are much better than those of normal FinFETs with a similar process. With an improved short-channel-effect immunity in the channels due to structure modification, the novel structure provides one of possibilities to extend the FinFET scalability to sub-10-nm nodes with little additional process cost.

Keywords: FinFET; Field-effect transistors; Si nanowire; Drain-induced barrier lowering; Subthreshold swing

PACS: 85.30

Background

To overcome serious scaling issues, multi-gate fin field-effect transistors (FinFETs) with 3D fin-shaped channels have been extensively explored for many years as a new device platform and have been recently introduced into mass production with cutting-edge process technologies [1, 2]. Excellent short-channel-effect (SCE) immunity is achieved for FinFETs owing to the strong gate control of the double gates in the fully depleted fin channels. In addition, the fabrication technology of FinFETs is a quasi-planar process and more compatible with the conventional planar process than previous vertical double-gate devices.

To increase the scalability of a conventional SOI FinFET with double gates on the rectangular fins, tri-gate FETs, a FinFET variant with triple gates on the fins, were developed [2]. In this technology, a trapezoidal fin on a normal bulk-Si substrate is implemented to decrease process integration issues and the cost of mass production. As CMOS technology continuously scales to the 10-nm node and beyond, the nearly perfect electrostatic integrity in the fin channels due to the double or triple gates is degraded, leading to stronger SCE in the ultimate short channels [3, 4]. Some new technologies such as the skinny fin channel with a high fin height-to-width ratio and the fin channel with novel gate electrodes, such as the Π-gate or the Ω-gate, have been developed to increase the scalability of FinFETs [5, 6].

Moreover, devices with a surrounding gate, such as gate-all-round (GAA) devices or nanowire (NW) transistors, are widely recognized as the definitive solution to suppress the SCE for the strongest gate control during Si FET scaling [7, 8]. However, although GAA or NW devices have the best scalability, they suffer from the process integration challenges for large-scale CMOS production. The challenges of the surrounding gate etch and the film-gap fill beneath the NW channels prevent the implementation of state-of-the-art high-k/metal gate (HKMG) stacks and the landing pads to anchor the stacked NWs, which pose limitations on device pitch scaling for high density circuit applications [9].

In this study, to combine the scaling advantage of the surrounding gate of NW devices with the normal bulk-Si FinFET process for future mass production, a novel HKMG FinFET with a scallop-shaped fin is proposed for

* Correspondence: yinhuaxiang@ime.ac.cn
Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

© 2015 Xu et al. This is an Open Access article distributed under the terms of the Creative Commons Attribution License (http://creativecommons.org/licenses/by/4.0), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly credited.
the first time. The structural advantages and fabrication flow are presented. The electrical characteristics and excellent SCE immunity for 27-nm and 14-nm devices are analyzed in details.

**Methods**

The proposed novel FinFET with a special fin structure is shown in Fig. 1a. Based on the normal FinFET structure, the sidewall profiles of the rectangular fin are modified to form continuously curved surfaces on both sides. The modified profile is similar to a scallop edge; therefore, the novel device is called a scallop-shaped FinFET (S-FinFET). The main fabrication process flow of the S-FinFETs on bulk-Si substrates is also proposed in Fig. 1a.

The entire integration flow of the S-FinFETs is fully compatible with the mainstream all-last HKMG FinFET process [2], except for a modified fin etch process.

Three different channel profiles for a normal FinFET, a stacked NW device, and an S-FinFET are shown in Fig. 1b. The S-fin has an embossed body region with a large fin width ($W_{1S-fin}$) and an incurved neck region with a small fin width ($W_{2S-fin}$). The stacked body channels are similar to the stacked quasi-NW channels joined together with a string. The stacked body channels with semi-surrounding gate electrodes provide stronger gate electric-field control than those of normal FinFETs or tri-gate FETs. Meanwhile, the narrow neck region has an ultrathin channel thickness, resulting in stronger gate control than conventional depletion devices with single or double gates.

In Fig. 1b, $W_{1S-fin}$ and $W_{2S-fin}$ of the S-FinFET are chosen as 15 and 5 nm, respectively, which are similar to the structure parameters of the fabricated S-FinFET devices presented in later paragraphs. To compare channel electrostatic integrity between different devices with a similar gate area, both the fin width ($W_{fin}$) of normal vertical FinFET and the channel diameter ($D_{nanowire}$) of NW device are defined as 10 nm in Fig. 1b. TCAD simulations are performed for these structures with gate length ($L_G$) of 14 nm. The mapping images of the simulated leakage density ($V_{GS} = 0 \text{V}, V_{DS} = 0.8 \text{V}$) across different fin channels are shown in Fig. 1b. The S-FinFET demonstrates a smaller leakage distribution than normal FinFET, but is a little worse than NW device. It indicates improved channel control for the new structure over normal FinFETs.

The process flow for a scallop-shaped fin formation is shown in Fig. 2.

All process is carried out on our experimental fab-line. The general spacer image transfer (SIT) technique is used to create a fine 3D fin structure on the Si substrate with well doping of $1.1 \times 10^{17} \text{cm}^{-3}$. The sacrificial core material of amorphous silicon (a-Si) is deposited on the pad oxide and patterned into multiple narrow bars by optical lithography and plasma etching. A thin conformal nitride layer is then deposited over the patterned core layer, and an anisotropic etch is subsequently performed to form a nitride/oxide spacer hard mask.

After removal of the core material, a newly developed Bosch process [10] is applied to etch Si between the spacer hard masks and to fabricate the fin array with a scallop-shaped profile. In Fig. 2, the HBr/Cl₂ plasma is used for the initial anisotropic Si etch (step-I), following by a special O₂/N₂ plasma to protect the straight fin surface (step-II); thirdly, the Cl₂ plasma is performed in next isotropic etch to form incurved fin (step-III). The chamber

![Fig. 1 Schematic illustrations of S-FinFET design and channel control capability.](image-url)
pressure and power are strictly controlled to precisely define the lateral etch depth. By repeating the sandwich-like etch process, the S-fin is created after a rounding and surface repairing process of a 5-nm liner oxidation (step-VII). Similar to the mainstream bulk-Si FinFET process for mass production, oxide shallow trench isolations (STI) are formed in the sequential steps (step-IX).

After S-fin formation, channel doping by punch-through stopping (PTS) implantation, dummy gate stacking, source/drain (S/D) engineering, and all-last HKMG processing are

---

**Fig. 2** Schematic illustrations of S-fin fabrication with modified process flow. Fabrication process for forming special S-Fin with stacked fin body and fin neck channels in the traditional integration flow.

**Fig. 3** Cross-sectional TEM images of S-FinFET along different axis. 

- **a** The cross-sectional views of fabricated S-Fin and conventional Fin in the inset with multi-layer HKMG stack.
- **b** The cross-sectional views of HKMG S-FinFETs with $L_G$ of 27 nm and $L_G$ of 14 nm.
performed for the fabrication of the transistors. The conditions of PTS implantation are carefully designed for a low doping (~3 × 10^{17} \text{ cm}^{-3}) in the top channel. The shallow extension regions of S/D are formed with twice 3 keV BF^+ implantations with tilted angle of 30° against to the direction of channel followed by a spike annealing. As a reference, FinFETs with conventional trapezoidal fins are fabricated with the same process, except for the special Si fin etch process.

**Results and discussion**

The cross-sectional views of the fabricated P-type $S$-FinFET along the directions of the gate and fin are shown in Fig. 3a, b, respectively. Because the fabricated N-type transistors in our lab have the gap filling issues of MGs, this letter focuses on results and discussion of P-type devices.

In Fig. 3a, the curved surface of the fin sidewall is clearly different from the straight sidewall of the conventional fins in the inset of Fig. 3a. The etched S-fin has three body and neck regions stacked from the top to the bottom of the fin, whereas two body and neck regions are above the STI oxide layer to form the fin channel of the transistor. The entire height of the S-fin channel is approximately 55 nm, deeper than the height (~40 nm) of a conventional fin for reference. $W_{1S-fin}$ and $W_{2S-fin}$ of the first fin body and first neck are 15 and 5 nm, respectively. $W_{3S-fin}$ of the first fin body is slightly smaller owing to the process variations.

The cross-sectional views of the gate stacks created by the all-last HKMG process for the scallop-shaped fins with physical $L_G$ of 27 and 14 nm are shown in Fig. 3b.

In these gate stacks, the multilayered film structure of the interface oxide/Hf-based high-k dielectric (0.7/2.3 nm) and the TiN/TaN/TiN/W (1.2/1.5/2.5/100 nm) metal gates are similar to the state-of-the-art mainstream HKMG process [2]. The film stack demonstrates good filling capability for the 27-nm gate structure. However, a filling

![Fig. 4](image-url) Transfer characteristics of fabricated S-FinFETs with different $L_G$s and reference device. **a** $I_{DS}-V_{GS}$ transfer curves of HKMG S-FinFETs with $L_G$ of 27 nm and $L_G$ of 14 nm. **b** $I_{DS}-V_{GS}$ transfer curves of an S-FinFET and a normal FinFET with $L_G$ of 14 nm and similar process.

![Fig. 5](image-url) Improved SCE control parameters of DIBL and SS as the gate length scaling for fabricated S-FinFETs. **a** DIBL and SS are shown as a function of gate length for S-FinFETs and normal FinFETs. Simulated DIBL variations are included. **b** Simulated electrostatic potential as well as $dE/dx$ in different channels for explaining the improved DIBL in S-FinFETs.
issue for the top W metal in the 14-nm gate structure occurs, leading to a small variation in the gate’s effective work function (EWF), though both the work-function TiN layers near the gate/Fin interface are keeping good. The extracted effective oxide thickness (EOT) and EWF from measured capacitance-voltage curves on thousands of S-fins are 0.9 nm and 5.05 eV, respectively. In this figure, the interface oxide thickness is relatively uniform even on the curved surface of S-fins because the oxide is very thin (0.7 nm) and grown on them after the corner rounding process with a chemical method.

Furthermore, the gate stack in Fig. 3a demonstrated good film uniformity and conformation to the curved surface of the scallop-shaped fin. It is shown that the distribution variation of the MG EWF along the surface of the curved channel is suppressed, which is often observed in nanowire devices owing to the film-filling issues underneath the nanowire channels.

Figure 4a shows the $I_{DS}$–$V_{GS}$ characteristics of fabricated p-type S-FinFETs with 27-nm and 14-nm gate lengths at a supply voltage ($V_{DD}$) of 0.8 V. Both saturated ($V_{DS} = -V_{DD} = -0.8$ V) and linear ($V_{DS} = -0.05$ V) transfer curves are shown for each device. The transfer curves are normalized by the actual channel width, which is defined as the perimeter (~118 nm/per fin) of channel cross-sectional area of two S-fins. The value of actual channel width in the S-FinFET is obviously larger than that of normal FinFET with similar fin width and height.

The $I_{DS}$–$V_{GS}$ curves of the reference 14 nm normal FinFET are shown in the Fig. 4b in comparison with those of S-FinFETs.

The critical electrical parameters such as drain-induced barrier lowering (DIBL) and subthreshold swing (SS) for evaluating SCE immunity of scaled transistors are defined as:

\[
\text{DIBL} = \frac{|V_{TH, \text{sat}} - V_{TH, \text{lin}}|}{|V_{DD} - 0.05V|} \\
\text{SS} = \frac{dV_{DS}}{d\log(I_{DS, \text{sat}})}
\]

where $V_{TH,\text{sat}}$ and $V_{TH,\text{lin}}$ are threshold voltages of the device under saturated and linear conditions, respectively. Both are the mean value of devices across the wafer.

The DIBL and SS are 21 mV/V and 65 mV/dec for a 27-nm $L_G$ and 62 mV/V and 75 mV/dec for a 14-nm $L_G$ S-FinFET. These parameters are excellent and approximately maintained the same level as 22-nm tri-gate devices ($L_G = 30$ nm) for mass production [2], even with a smaller physical $L_G$.

From Fig. 4b, it is found that $V_{TH}$s of these fabricated S-FinFETs and normal FinFETs are relatively small, showing that the devices are more like depletion devices. This behavior may be due to a relatively low channel doping and an extremely band-edged MG (EWF~5.05 eV) integrated on very short channels.

Although DIBL and SS are much improved, the drain current of the fabricated S-FinFET is smaller than that
of reference normal FinFET in Fig. 4b. This may result from the large series resistance in S/D regions without selective epitaxy process due to the limited process capability in our lab-line. The thinner fin structure of S-FinFET has a more serious series resistance effect. As a result, it induces a smaller driving current. Another reason is perhaps due to the degraded carrier mobility for serious electrical field scattering or stress effect in the corner of the scalloped fins. The plasma damage on S-fin surface with more etch process may also induce a degradation on carrier mobility in the channel.

The dependencies of DIBL and SS on the $L_G$ scaling for the fabricated S-FinFETs and normal FinFETs are shown in Fig. 5a. For long channels, both S-FinFETs and normal FinFETs have a similar DIBL and SS. As the gate length scales into the sub-40-nm range, the DIBL and SS for normal FinFETs clearly increase owing to the stronger SCE, whereas there is a slight increase for the S-FinFETs. For a 27-nm $L_G$, the decrease of DIBL and SS for S-FinFETs over normal FinFETs are 27 mV/V and 9 mV/dec, respectively. For a 14-nm $L_G$, the decrease of DIBL and SS are 48 mV/V and 17 mV/dec, respectively.

Because the S-FinFET and normal FinFET have similar channel PTS doping (peak concentration of $3 \times 10^{19}$ cm$^{-3}$ located below STI surface), S/D doping, activation process (1050 °C Spike RTA), and MG EWF, the improvements of DIBL and SS are mainly attributed to the channel structure modification via the introduction of an enhanced gate electric field in the special fin channel. As shown in Fig. 5a, the DIBL and SS of the S-FinFETs are slightly degraded but still do not exceed the minimum acceptable criteria for low-power CMOS circuit applications as $L_G$ continuously scales down 14 nm, which is the critical specifications of the sub-10-nm CMOS process node. However, the parameters of the normal FinFET are greatly degraded, much worse than those of the S-FinFET, far away from the acceptable level for CMOS circuit applications. The simulated DIBL variations with $L_G$ for these two devices are also shown in Fig. 5a. The trends are very close to these experimental results, which confirmed the structure advantage of S-FinFET.

To insightfully illustrate the physical reason of improved DIBL in S-FinFET, the simulated electrostatic potential profiles in the channels by TCAD are shown in Fig. 5b. In this figure, with the same drain voltage of 0.8 V, the energy barrier (0.30 eV) in the source for S-FinFET is larger than that (0.27 eV) for normal FinFET. Meanwhile, in the inset of Fig. 5b, the gradient of lateral electrical field ($dE_y/dx$) in S-FinFET channel is obviously smaller than that in normal FinFET channel. These parameter differences decide the parasitic charges controlled by drain electrical field in the channel of S-FinFET fewer than those of normal FinFET, which causes the device to have a smaller DIBL value [11].

The variability of $V_{TH,lin}$ and on-state current ($I_{on}$) for 50 nm S-FinFETs and normal FinFETs are shown in Fig. 6. From these figures, the variation $\sigma$ of fabricated S-FinFETs is similar to those of normal FinFETs. The reason maybe the variability of FinFETs are mainly determined by four sources [12]: variation of (a) gate length, (b) fin thickness or width, (c) channel doping, and (d) EWF of MG. The variations of (b) in S-FinFETs are increased for scalloped channel shape, but those of (c) are decreased due to attenuated heavily doping region near and on-state current ($I_{on}$) for 50 nm S-FinFETs and normal FinFETs are shown in Fig. 6. From these figures, the variation $\sigma$ of fabricated S-FinFETs is similar to those of normal FinFETs. The reason maybe the variability of FinFETs are mainly determined by four sources [12]: variation of (a) gate length, (b) fin thickness or width, (c) channel doping, and (d) EWF of MG. The variations of (b) in S-FinFETs are increased for scalloped channel shape, but those of (c) are decreased due to attenuated heavily doping region near fin bottoms. In addition, the most important factor of the variation in EWF of MGs is the same for both devices. As a result, the variability in fabricated S-FinFETs demonstrates no obvious degradations.

These results indicate that the S-FinFET demonstrates an obvious scaling advantage over the normal FinFET for sub-10-nm node CMOS process applications.

Conclusions

Novel S-FinFETs with mainstream all-last HKMG technology using special fin channels have been reported. By slightly modifying the fin etching process of the normal FinFET process, the new devices have achieved excellent DIBL and SS as $L_G$ scaled down below 20 nm. The variability has no obvious degradation. Our results are promising for helping general FinFET technology extend into the sub-10-nm node.

Competing interests

The authors declare that they have no competing interests.

Authors' contributions

WX participated in the fabrication of the S-FinFETs, measured the electrical properties of the transistors, and drafted the manuscript. HY designed the S-FinFET, analyzed the results, and wrote the manuscript. XM helped the fabrication of the S-FinFETs and finished the device simulations. PH and LM developed the process of the sub-10-nm node. All authors read and approved the final manuscript.

Acknowledgements

This work was supported by "16/14nm Basic Technology Research" of the national 02 IC projects in China (No. 2013ZX0203). The authors would like to thank engineers in Integrated Circuit Advanced Process Center, IMECAS for their support in wafer processing.

References

1. Lindert N, Chang L, Choi Y-K, Anderson EH, Lee W-C, et al. Sub-60-nm quasi-planar FinFETs fabricated using a simplified process. IEEE Electr Device Lett. 2001;22:487–9.
2. C-H Jan, U Bhattacharya, R Brain, S-J Choi, G Curelo, G Gupta, et al. A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications. Proceeding Int Electron Devices Meet Tech Dig. 2012; doi:10.1109/IEDM.2012.6478969.
3. Sun X, Lu Q, Moroz V, Takeuchi H, Gebara G, Wertzel J, et al. Tri-Gate bulk MOSFET design for CMOS scaling to the end of the roadmap. IEEE Electr Device Lett. 2008;29:491–3.
4. B Yu, L Chang, S Ahmed, H Wang, S Bell, C-CY, et al. FinFET Scaling to 10nm Gate Length. Proc Int Electron Devices Meet Tech Dig. 2002; doi:10.1109/IEDM.2002.1175025.
5. Jovanovic V, Suligoj T, Poljak M, Civale Y, Nanver LK. Ultra-high aspect-ratio FinFET technology. Solid-State Electr. 2010;54:870–6.
6. Rathod SS, Saxena AK, Dasgupta S. Electrical performance study of 25 nm Omega-FinFET under the influence of gamma radiation: A 3D simulation. Microelectron J. 2011;42:165–72.
7. Ng RMY, Wang T, Liu F, Zuo X, He J, Chan M. Vertically stacked silicon nanowire transistors fabricated by inductive plasma etching and stress-limited oxidation. IEEE Electr Device Lett. 2009;30:520–2.
8. C Dupré, A Hubert, S Bécu, M Jublot, V Maffini-Alvaro, C Vizioz, et al. 15nm-diameter 3D stacked nanowires with independent gates operation: ΦFET. Proc Int Electron Devices Meet Tech Dig. 2008; doi:10.1109/IEDM.2008.4796805.
9. S Bangsaruntip, K Balakrishnan, S-L Cheng, J Chang, M Brink, I Lauer, et al. Density scaling with gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond. Proc of Int Electron Devices Meet Tech Dig. 2013; doi:10.1109/IEDM.2013.6724667.
10. Chang C, Wang YF, Kanamori Y, Shih JJ, Kawai Y, Lee CK, et al. Etching submicrometer trenches by using the Bosch process and its application to the fabrication of antireflection structures. J Micromech Microeng. 2005;15:580–5.
11. Shih C-H, Chen Y-M, Lien C. An analytical threshold voltage roll-off equation for MOSFET by using effective-doping mode. Solid-State Electr. 2005;49:908–12.
12. Matsukawa T, O’uchi S, Endo K, Ishikawa Y, Yamauchi H, Liu YX, et al. Comprehensive analysis of variability sources of FinFET characteristics. Proc Symp VLSI Technology Tech Dig. 2009;VLSIT09:118–9.