6 transistors and 1 memristor based memory cell

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ABSTRACT
Area efficient and stable memory design is one of the most important tasks in designing system on chip. This research concentrates in designing a new type of hybrid memory model by using only nMOS transistors and memristor. The proposed memory cell is very stable during successive read operates and comparatively faster and also occupies less amount of silicon area. The stability of the data during successive read operation and noise margin are in the promising range. Extensive simulation results using LTspice and Cadence software tools demonstrate the validity and competency of the proposed model.

Keywords:
Memory cell
nMOS
SRAM
Static noise margin
Successive read

1. INTRODUCTION
Density of transistors in integrated circuit is increasing rapidly for low cost, better operation and high performance. Now a days, electrical devices have been transformed from wired to wireless portable and those are in high demand for minimum time delay and less power. In most of the electrical devices, memories are contemplated as a vital building block in various applications [1]. Static random access memory (SRAM) plays an important role in building memory system. SRAM occupies almost 90% of die area in some system [1-3]. The conventional 6T SRAM is constructed with two cross coupled inverters and two access transistors [3] but has some limitations while reading and writing data, especially at low supply voltage. Stability of data also hampers due to leakage current [4, 5]. Several models [6-12] have been proposed to overcome the problem of malfunctioning of 6T SRAM. A group of researcher [6] proposed to increase the threshold voltage in order to stable operation. Another design was shown by estimating a perfect 200mV sub-threshold voltage [7]. But their design increases time delay during write operation. And the longer time delay consumes more power [8]. So the SRAM is designed with 7 to 8 transistors are also proposed [9-12] to achieve better performance, but those models require extra hardware overhead of about 30%.

As the new technology emerges, along with transistor some other component like memristor is also used to build memory. A nonvolatile characteristic of this device is an interesting topic for research [13] in designing memory cell. Among several proposed models using memristor, 1-transistor 2-memristors based model [1] occupies less area and single reference voltage is needed for operation, whereas the write process takes place into two steps: fully discharging 2M devices and charging them back with the required voltage (Data). Also longer read operation might affect the stored data to flip. Another 4T2M nvRAM cell [3] is
designed and elaborated its better performance in both read and write operation but consumes more power. Another design of memristor based memory is 7T2M model [14], where along with 7 transistors 2 memristors are used but the cell requires 16-20% more time to read data at nominal voltage as compared to 6T conventional SRAM. Fast operation and less power consumption was achieved in 8T2R memristor based memory [15] but the model shows poor signal to noise margin during read operation (RSNM) at low Vdd [16]. Another 8T2M architecture [17] has been proposed for high speed and low power operation but contains large proposed for low power consumption and fastest operation under ultra-low Vdd, but that cell require large amount of area and have a limited write margin.

The present research proposes a 6-transistors and 1-memristor based memory cell. In this architecture, all the pMOS transistors of conventional SRAM are replaced by nMOS transistors and a memristor is added as the footer. The proposed model performs better in terms of time delay, the noise margin and power consumption. The construction of the proposed cell is very much alike with the memory cell proposed in ref [18] with one nMOS has been replaced by memristor for better performance. The paper is organized in the following manner: section II describes some fundamentals of memristor, proposed memory model is explained in detail in section III. In section IV, simulation results are discussed while section V concludes the outcome of this research.

2. BACKGROUND

In 1971, Leon Chua theoretically described memristor as the fourth fundamental element of electrical circuit after resistor (R), capacitor (C) and inductor (L) [19] as shown in Figure 1. According to him, from four fundamental circuit variables: voltage (V), current (I), flux (Φ) and charge (Q), six possible combinations of relationships should be existed. With respect to time, flux (Φ) and charge (Q) are integration of voltage (V) and Current (I) respectively. Three other relations are: Q=CV, Φ=LI and V=IR. Therefore the missing sixth possible combination was made between charge (Q) and flux (Φ) i.e.

\[ M = \frac{\partial \Phi}{\partial Q} \]

Figure 1. The existence of memristor along with resistor (R), capacitor (C) and inductor (L) as a fourth fundamental circuit element

Memristor is a bipolar resistive switch constructed as TiN/TiOx/HfOx/TiN metal-oxide structure is considered as a vital component in memory design. These memories are also known as resistive RAM (RRAM). For write ‘0’, SET operation is performed, which is known as Low resistance state (LRS) and for write ‘1’, RESET operation is executed also known as High resistance state. RRAM can also store multiple bits of data in a single memory cell. This is a non-volatile memory (NVM) can hold the data while turning off the device [15, 20].

The basic device structure of a memristor is shown in Figure 2. When positive voltage is applied at the doped terminal of the device then the length of the doped layer (w) extends towards the undoped area. But if positive voltage is applied at the undoped side then the length (w) decreases. If the ratio of w/D = 1, which means the doped region extends fully towards the total length D, the resistivity of the device would be considered as lowest (Ron). Likewise, when the ratio of w/D = 0 which means the undoped region extends fully towards length D, the total resistance would be the highest (Roff). The mathematical model of memristor or memristance can be represented as [13]:

\[ M (w) = [\text{Ron} \cdot \frac{w}{D} + \text{Roff} \cdot (1-\frac{w}{D})] \]
3. THE PROPOSED 6T1M CELL

Figure 3 shows the proposed circuit of 6T1M nvSRAM. It is constructed with 6 nMOS transistors and 1 memristor. The two pMOS of conventional 6T SRAM are replaced by two nMOS (T1, T2), where the gate of the transistors are connected with storage node Q and Qbar respectively. The source of T3 and T4 transistors are connected with low resistance terminal of memristor (M1). The high resistance terminal of memristor is connected to ground.

In write operation, data is stored in Q and Qbar storage nodes with the help of bitline (BL) and inverted bitline (BLBar) through access transistors (T5, T6). For example, after a write operation if Q node stores ‘1’ whereas node Qbar stores ‘0’, transistor T1 and T4 will be on but transistor T2 and T3 will be off, then the current from Vdd will follow through T1 and helps to maintain the high voltage at node Q. Whereas Qbar cannot get charged and also finds a memristor barrier to discharge, so the data remains unchanged. Similarly if node Q stores ‘0’ and Qbar stores ‘1’ all the transistors state will be inverted. Transistors T2 and T3 will be on but transistors T1 and T4 will be off. Thus the data from storage node is ready to read from the voltage at nodes Q and Qbar.

4. SIMULATION RESULTS AND DISCUSSIONS

Considerable simulation experiments are carried out using LTspice and Cadence simulation software by employing PTM (Predictive Technology Model) transistors and memristor model of Biolek [21]. Results of successive read/write operations of proposed cell as well as comparative analysis with the conventional 6T, 7T SRAM cell in terms of time delay, static noise margin (SNM) and power consumption are presented. PTM transistors model of 16nm and 22nm and 0.7v supply voltages and 0.3v threshold voltage are used in most of the simulation experiments. However, some other supply voltage of 0.5v, 0.9v and 1.2v are also used in some cases.

4.1. Write ‘0’ overwriting ‘1’ operation

Figure 4 shows the simulation results obtained after storing ‘0’ by overwriting ‘1’. The results clearly demonstrate that the bitline (BL) and inverse bitline (BLBar) voltages are inter changed and remain unchanged during the hold period. It is also clearly seen that the voltage (about 0.6 v) at BL during write ‘1’ remains as it is during the read ‘1’ operation though the voltage drops a little bit during the intermediate hold time.
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4.2. Successive read operation

Error free successive read operation is one of the most vital characteristics of memory circuit. Figure 5 depicts the simulation results of write ‘1’ and then successive read operations. It is confirmed that the bitline voltages of BL and BLB remain within the limited range during successive read operation. The voltage difference \( V_d = V_{\overline{Q_{bar}}} - V_Q \) also remains same throughout successive read operation.

4.3. Time delay calculation

Time required to write and read operations are obtained [22]. For both ‘1’ and ‘0’ data value in order to compare the competency of the proposed model. Table 1 exhibits the comparative results of the proposed cell along with other models, which are calculated from different memory models along with our proposed memory cell by considering exactly the same parameters. The results demonstrate that the write ‘0’ operation is almost 3 times faster than conventional 6T SRAM cell. And the write ‘1’ operation is about five times faster than that. However, read ‘0’ operation is taking more or less same amount of time as conventional 6T SRAM but the proposed model is taking a bit more time than that.

| Time delay (ps) | 6T | 7T | Ref [5] | Proposed Cell |
|----------------|----|----|---------|----------------|
| Write ‘0’      | 42.8 | 405.9 | 23.59 | 13.74 |
| Read ‘0’       | 8.35 | 4454 | 31.32 | 10.20 |
| Write ‘1’      | 62.1 | 50.1 | 50.81 | 11.99 |
| Read ‘1’       | 5.36 | 3968 | 19.70 | 61.84 |
4.4. Variation of input voltage

The time required to write a data into the memory and retrieving the stored data from the memory cell depend on the supply voltage value. In order to examine that dependency, the proposed 6T1M cell is operated at three different voltages as: 0.7v, 0.9v and 1.2v supply. Figure 6 depicts the simulated results, where we can see that write ‘1’ operation does not depend on the variation of supply voltage. But the read ‘1’ operation takes more time for higher supply voltage. On the other hand Figure 7 demonstrates that, both the write ‘0’ and read ‘0’ operations become faster with the increase of supply voltage.

Simulations are also carried out for investigating the dependency of transistor sizes. Figure 8 shows the time required for write and read ‘0’ operations in case of 16nm and 22 nm transistor sizes. And Figure 9 presents the same for write and read ‘1’ operations. It is clearly seen from those two figures that the larger transistor takes more time to operate.
4.5. Static noise margin

Static noise margin (SNM) is the stability of a circuit. The maximum noise voltage which can be tolerated by static RAM without inverting the stored data. There are two techniques for calculating SNM, one is drawing butterfly curve and try to collect the large square inside its wing whereas the other method is by applying external noise source on the storage nodes with opposite polarities and collecting its optimum voltage, where the data of storage node gets inverted [23, 24]. In this proposed research, SNM is detected by using external noise source. It would be consider a better SRAM when it can bare much amount of noise without distorting the stored value. Figure 10 presents the calculated SNM of the proposed cell along with several other conventional memory cells. And the proposed cell shows a significantly higher amount of noise margin as compared with others. Simulation results also demonstrates that the increased transistor size of the proposed memory cell provides higher level of SNM.

4.6. Power consumption

Power consumptions are estimated during write and read operations as well as during standby mode for the proposed cell. Powers dissipations are estimated while operating the proposed memory cell at two different voltages as: 0.5v and 0.7v and CMOS transistor sizes of 16nm and 22nm.

Figures 11 and 12 present the result of power requirement during write/read ‘1’ and write/read ‘0’ respectively for 16 nm technology node. From the results, it seems like power consumption for read ‘1’ remains almost same in both operating voltages whereas the power consumption during write ‘1’ reduces at higher voltage. It is also seen that the write ‘0’ power remains almost same for both operating voltage whereas read ‘0’ power increases significantly for higher voltage. Figures 14 and 15 depict the similar results of Figures 11 and 12 for 22 nm transistor size. It is clearly seen that power consumption for both write and read ‘1’ and ‘0’ operations are increases with increased operating voltage of 0.7v as compared to 0.5v.
After each and every read and write operations, there is an idle state which is known as static mode. Figures 13, 14 and 15 demonstrate the results of power required for different operations at 22 nm and 16 nm transistor sizes. It is obvious that the static power consumption remains almost same after both the write ‘1’ and write ‘0’ operations. However it is increased with the increases of operating voltage level.
It is also noticed that the static power dissipation increases with the increased size of the transistors. Table 2 demonstrates the comparative analysis of power dissipation in different memory models. And it is clearly seen that the proposed cell consumes less power for both write ‘1’ and ‘0’ operations as compared to others recently proposed models.

Table 2. Comparison of power (micro watt) dissipation in different models

| Mode      | 6T SRAM | 7T SRAM | Ref [5] | Ref [14] | Proposed Cell |
|-----------|---------|---------|---------|----------|---------------|
| Write 1   | 5.08    | 5.89    | 3.51    | 5.97     | 3.41          |
| Write 0   | 6.39    | 6.28    | 1.18    | 3.14     | 1.13          |

4.7. Number of transistor

Number of transistors required to design a memory cell is a vital parameter while fabricating an IC. Compared to most recently developed memristor based SRAM cells, the proposed cell contains less number of transistors and memristors (6 nMOS transistors and 1 memristor) as shown in Table 3. There is no pMOS transistor in in the proposed cell which provides better results in terms of silicon area.

Table 3. Comparison of total component for different mode

| Parameter   | 6T   | 7T   | Ref [18] | Ref [16] | Ref [15] | Proposed Cell |
|-------------|------|------|----------|----------|----------|---------------|
| No. of pMOS | 2    | 2    | 0        | 2        | 2        | 0             |
| No. of nMOS | 4    | 5    | 7        | 6        | 6        | 6             |
| No. of memristor | 0  | 0    | 0        | 2        | 2        | 1             |
| Total component | 6  | 7    | 7        | 10       | 10       | 7             |

4.8. Silicon area requirement

The layouts of the proposed memory cell is designed with Cadence software tool using 45nm technology nodes is shown in Figure 16. Table 4 shows the silicon area required to design the proposed cell along with some other memory cells [25-26] for comparison. Although it is clearly observed from the simulated results that the proposed cell requires slightly more area in 45 um technology as compared to the conventional 6T SRAM cell. But it needs significantly less area in 90 um technology and consumes almost 20% power than the 6T and 7T SRAM cell.

Table 4. Comparison of area in according to length of the transistors

| Length of Transistors | 6T SRAM | 7T SRAM | Proposed 6T1M SRAM |
|-----------------------|---------|---------|--------------------|
| 45nm                  | 3.438um² | 4.41um² | 3.8801um²          |
| [Ref. 25]             | [Ref. 25]|         |                    |
| 90nm                  | 12.35mm² | -       | 8.28um²            |
| [Ref. 26]             |         |         |                    |
4.9. Guard ring in memory cell

When voltage or current fluctuates at input or output node, then parasitic coupled BJT inside of the CMOS structure can be turned on and a low impedance path can be formed. This situation can produce either a momentary or a permanent loss of circuit operation. Several techniques are introduced to reduce this type of phenomena such as: guard ring, use of an epitaxial layer, deep trenches, etc. In this work, an analysis of these phenomena with the use of guard ring is presented. Guard rings are used to decouple the parasitic bipolar transistors. Two guard ring structures are employed: one for minority carriers and another for majority carriers connected to VDD and VSS metal lines in order to collect Carriers.

5. CONCLUSION

A new memory model of 6T1M SRAM cell is proposed and the cell performs better in terms of data stability during both write and read operations. Only nMOS transistors are used along with a memristor and require less amount of area. The time required for write and read operations are less and the noise margin level for both write and read operations are better as compared to recently proposed modes. Also the layout of the proposed model demonstrates the requirement of less silicon area. The proposed cell may be considered as a competent candidate for the memory used in system on chip design.

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