Interface traps density of anodic porous alumina films of different thicknesses on Si

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Abstract. Impedance Spectroscopy was employed in order to investigate the electrical properties of thin porous anodic alumina films on Si, of thicknesses in the range of 50-200 nm, fabricated by anodization in sulfuric acid. C-V and G-V measurements were performed in the voltage range +5.0V to –10.0 V and the frequency range 1MHz to 100Hz. The typical form of C-V and G-V curves of a Metal-Insulator-Semiconductor (MIS) structure was obtained. The effective dielectric constant $\varepsilon$ was calculated with a typical value of 6.5, in good agreement with previous published results. C-\omega and G-\omega measurements were performed as a function of the applied gate voltage in the depletion region in order to calculate the interface trap density $D_{it}$ and interface trap time constant $\tau_{it}$. $D_{it}$ and $\tau_{it}$ were evaluated following the Conductance Method. The evaluated $D_{it}$ values are of the order of $10^{12}$eV$^{-1}$cm$^{-2}$ and their observed thickness dependence is rather attributed to differences of the porous alumina/p-Si interface, introduced during the formation process, than to sample thickness.

1. Introduction
Porous alumina films on Si show great technological interest for their use as templates for nanofabrication [1], due to the self-formation during anodization of ordered vertical pores of diameter of few tens of nanometers and a density of the order of $10^{11}$ pores/cm$^2$. It is also an interesting material to be used as gate dielectric [2]. The fabrication conditions of anodic alumina films on aluminum are well known and there is extensive literature describing the properties of the obtained films. However, the fabrication of very thin anodic porous alumina films on Si is still an open area for investigation [2-4]. The films used in this work were fabricated by anodization in sulfuric acid, and they showed regular vertical pores, separated from the Si substrate by a thin alumina membrane over a cavity. C-V and G-V measurements were used to characterize the alumina/Si interface.

2. Experimental Details
Aluminium films of thickness 30, 50 and 100nm were deposited on p-type<100> oriented silicon substrates by electron gun evaporation. An ohmic contact was formed on the back side of the wafers. Anodization was performed in a conventional electrochemical cell with a platinum electrode used as cathode, while the anode was contacted at the backside of the silicon wafer. For the anodization process, sulfuric acid, 10% in weight, under constant voltage of 20 V, was used. After anodization the thickness of the samples was 55, 95 and 190nm respectively. Porous density was equal to $8x10^{10}$
pores/cm² and pore size 16 nm in average. A gate aluminium electrode was deposited and patterned on top of the porous anodic alumina films for the electrical characterization. The capacitors area was 1.6x10³ cm².

All samples were characterized through bias and frequency dependent capacitance and conductance measurements at room temperature using an Alpha-N High Resolution Dielectric Analyzer in a parallel mode, controlled by the WinDeta software. The applied gate voltage followed a loop from 5.0 V to −10.0 V with a step of 0.1 V, in the frequency range from 1MHz to 100Hz. Leakage currents were investigated from static \( I-V \) measurements by applying forward and reverse bias voltage, using a Keithley 617 Programmable Electrometer connected with an Oltronix power supply. The voltage range was −8.0V to +8.0V. In order to calculate the interface trap density \( D_{it} \) and interface trap time constant \( \tau_{it} \), \( C-\omega \) and \( G-\omega \) measurements were performed as a function of the applied gate voltage in the depletion region. The frequency range was from 1MHz to 1Hz.

3. Experimental Results and Discussion

\( I-V \) measurements were performed in order to determine leakage currents and the corresponding conduction mechanisms. Results are depicted in figure 1 for the 55nm thick samples. For positive bias voltage applied on the top Al electrode the slope is almost equal to 1, which implies that an ohmic mechanism is responsible for the leakage current. In the opposite case the slope is almost equal to 2 for an applied voltage greater than 1.0V, which implies that these currents are space charge limited. Thicker samples exhibit negligible leakage currents.

Figure 2 presents the measured capacitance as a function of gate voltage for frequencies 10³, 10⁴ and 10⁵Hz and 1MHz for the 190nm thick sample. The three distinct regions of a typical MIS structure [5] are observed: The inversion region (I), the depletion region (II) and the accumulation region (III). The observed curves showed a frequency dispersion in both depletion and accumulation regions. Specifically the capacitance increases with decreasing frequency. In accumulation the rise of capacitance is attributed mainly to the series resistance effect, while in depletion it is mainly attributed to frequency dependent capacitive response of interface states (recombination-generation in interface states).

![Figure 1. Current as a function of the applied DC voltage. Solid symbols correspond to positive bias voltage on the top Al electrode, while open symbols correspond to the opposite.](image1)

![Figure 2. Measured capacitance versus bias voltage as a function of frequency (■1x10⁴Hz, ▲1x10⁵Hz, ◆1x10⁶Hz, ▶1x10⁷Hz).](image2)

From \( C-V \) and \( G-V \) measurements presented in figures 3(a) and 3(b) it is obvious that conductance shows a maximum in the middle of the depletion region, for the 190nm thick sample. The same result, which is typical for a MOS structure, has also been observed for the 95nm thick samples. On the other
hand this behavior is not observed in the 55nm thick samples (fig. 3(b)). This could be attributed to leakage currents, which were of the order of $10^{-5}$A for an applied gate voltage of 1.0V, while thicker samples exhibit negligible leakage currents, of the order of $1x10^{-12}$A.

Figure 3. Capacitance and Conductance as a function of bias voltage, at 1MHz for (a) 55nm and (b) 190nm.

From C-V and G-V measurements in strong accumulation the oxide capacitance $C_{ox}$ and the series resistance $R_s$ were calculated [5] through the relations:

$$ R_s = \frac{G_{acc}}{G_{acc}^2 + \omega^2 C_{acc}^2}, $$

$$ C_{ox} = C_{acc} \left[ 1 + \left( \frac{G_{acc}}{\omega C_{acc}} \right)^2 \right], \tag{1} $$

where $C_{acc}$ and $G_{acc}$ are the measured capacitance and conductance in strong accumulation. Table 1 shows the calculated values of $R_s$ and $C_{ox}$ for all samples. These $R_s$ values are used to correct the measured C-V, G-V curves. From $C_{ox}$ the effective dielectric constant was calculated. For all samples the effective dielectric constant evaluated is 6.5, which is in good agreement with previously published experimental results [8].

In order to calculate the interface trap density $D_{it}$ and interface trap time constant $\tau_{it}$, C-$\omega$ and G-$\omega$ measurements were performed as a function of the applied gate voltage in the depletion region. For the evaluation of $D_{it}$ and $\tau_{it}$ the Conductance Method was used. The corrected capacitance $C_c$ and conductance $G_c$ for series resistance were evaluated from the relations:

$$ C_c = \frac{G_m^2 + \omega^2 C_m^2}{\alpha^2 + \omega^2 C_m^2} C_m, $$

$$ G_c = \frac{G_m^2 + \omega^2 C_m^2}{\alpha^2 + \omega^2 C_m^2} G_m, \quad \alpha = G_m - \left( G_m^2 + \omega^2 C_m^2 \right) R_s \tag{2} $$

where $C_m$ and $G_m$ are the measured capacitance and conductance.

If leakage currents $I_{DC}$ are present, the static conductance $G_{DC}$ is determined by differentiating the leakage current versus voltage, $dI / dV$, and this static conductance $G_{DC}$ must be subtracted from the corrected conductance $G_c$:

$$ G_{CDC} = G_c - G_{DC} \tag{3} $$

This procedure [5-7] has been followed for all samples of 55nm thickness. Note that samples of 90nm and 190nm thickness exhibit negligible leakage currents.

The interface trap conductance $G_{it}$, $D_{it}$ and $\tau_{it}$ were then evaluated from the relations [9]:

$$ G_{it} = \frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_{CDC}}{G_{CDC}^2 + \omega^2 (C_{ox} - C_c)^2}, \quad D_{it} = \frac{2.5}{qA} \left( \frac{G_p}{\omega} \right)_{max}, \quad \tau_{it} = \frac{2}{\omega} \tag{4} $$

where $A$ is the area of the capacitor and $q$ the electron charge. Note that values of $D_{it}$ and $\tau_{it}$ evaluated from more explicit models [5] yield, within experimental error, the same results. Figures 4(a) and 4(b) present $G_{it}$ vs. $\omega$, in the depletion region, for the 190nm and 55nm thick samples, respectively. It is
obvious that with decreasing negative gate voltage, the maximum in $G_p/\omega$ decreases and shifts to lower values of $\omega$. The same behavior is observed for all samples.

Figure 4. $G_p/\omega$ versus $\omega$ as a function of gate voltage in the depletion region for the sample (a) of 190nm and (b) 55 nm thick.

The $D_n$ levels are determined by using the maxima $G_p/\omega$ of the $G_p/\omega$ vs $\omega$ curves and equations (4). Table 1 shows the values of $D_n$ and $\tau_n$ for all samples.

Table 1. Calculated values of $R_s$, $C_{ox}$, $D_n$ and $\tau_n$ for samples of different thickness.

| Thickness | $R_s$ (Ohm) | $C_{ox}$ (F) | $D_n$ (eV$^{-1}$cm$^{-2}$) | $\tau_n$ (s) |
|-----------|-------------|-------------|----------------------------|-------------|
| 55 nm     | 370         | 1.52 $10^{-10}$ | 1.5 $10^{12}$          | 2.5 $10^{-6}$ |
| 95 nm     | 58          | 1.05 $10^{-10}$ | 3.0 $10^{12}$          | 1.0 $10^{-3}$ |
| 190 nm    | 60          | 4.7 $10^{-11}$  | 6.0 $10^{12}$          | 1.5 $10^{-3}$ |

4. Conclusions

Thin porous anodic alumina films on Si exhibit a typical behavior of a MIS structure. The effective dielectric constant of porous alumina was calculated to be 6.5. The values obtained for $D_n$ are of the order of $10^{12}$ eV$^{-1}$cm$^{-2}$. Differences in $D_n$ between the different samples and their observed thickness dependence are attributed to the porous alumina/p-Si interfaces introduced during the formation process [10]. Further experimental work is in progress, in order to improve these interfaces and thus lower the density of interface states, since the obtained values of $D_n$ are rather high for technological applications.

5. References

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