MiniFloat-NN and ExSdotp: An ISA Extension and a Modular Open Hardware Unit for Low-Precision Training on RISC-V Cores

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Abstract—Low-precision formats have recently driven major breakthroughs in neural network (NN) training and inference by reducing the memory footprint of the NN models and improving the energy efficiency of the underlying hardware architectures. Narrow integer data types have been vastly investigated for NN inference and have successfully been pushed to the extreme of ternary and binary representations. In contrast, most training-oriented platforms use at least 16-bit floating-point (FP) formats. Lower-precision data types such as 8-bit FP formats and mixed-precision techniques have only recently been explored in hardware implementations. We present MiniFloat-NN, a RISC-V instruction set architecture extension for low-precision NN training, providing support for two 8-bit and two 16-bit FP formats and expanding operations. The extension includes sum-of-dot-product instructions that accumulate the result in a larger format and three-term additions in two variations: expanding and non-expanding. We implement an ExSdotp unit to efficiently support in hardware both instruction types. The fused nature of the ExSdotp module prevents precision losses generated by the non-associativity of two consecutive FP additions while saving around 30% of the area and critical path compared to a cascade of two expanding fused multiply-add units. We replicate the ExSdotp module in a SIMD wrapper and integrate it into an open-source floating-point unit, which, coupled to an open-source RISC-V core, lays the foundation for future scalable architectures targeting low-precision and mixed-precision NN training. A cluster containing eight extended cores sharing a scratchpad memory, implemented in 12 nm FinFET technology, achieves up to 575 GFLOPS/W when computing FP8-to-FP16 GEMMs at 0.8 V, 1.26 GHz.

I. INTRODUCTION

With machine learning becoming ubiquitous, the demand for neural network (NN) training has increased exponentially. Today’s NN models require up to three orders of magnitude more total compute than only two years ago [1]. To efficiently compute these workloads, hardware architectures for NN training need to evolve very rapidly, especially since the required increase in performance and efficiency cannot be achieved by technology scaling alone and requires algorithmic and architectural improvements. The exponential growth of machine learning, and the need to train NN models, also translates into ever higher energy and carbon impacts [2], which further motivates investments toward cutting-edge energy-efficient architectures.

More compact data types have recently driven fundamental breakthroughs for efficient NN training and inference [3]. These new low-precision formats greatly improve the memory footprint of the NN models and reduce the datapath size of the processing elements (PEs), thereby improving the overall power consumption. NN algorithms have shown to be particularly resilient to the noise introduced by employing lower-precision formats. Especially, narrow integer data types for inference – even as low as ternary and binary formats [4], [5] – have been extensively researched. NN training, however, demands the higher dynamic range provided by floating-point (FP) formats and is usually performed using at least 16-bit FP data types. Only recently, 8-bit formats have been explored in a mixed-precision setup with 16-bit formats [6], [7].

Further performance and efficiency improvements can be achieved by matching algorithmic advancements in mixed, low-bitwidth training with microarchitectural enhancements, e.g., developing new functional units and accelerators. Most modern CPUs already support fused multiply-add (FMA) operations, which are more precise than performing separate FP multiply and add instructions. As a fundamental operation for both inference and training of NN models, the sum of dot products is another ideal candidate for a dedicated hardware block.

Fusing multiple FMA into a single sum of products – or dot product – unit allows for a single normalization and rounding step, thereby improving the precision, area, timing, and power consumption of the functional unit. Even higher gains can be achieved by designing specialized matrix-multiplication accelerators in which dot-product modules are scaled out, as in the case of tensor cores [8]. For NN-oriented workloads, dot-product operations are particularly interesting when the accumulation result is returned in a wider format, which allows for retaining a higher computational precision. In this paper, we refer to such operations as expanding operations.

Such a trend can already be observed in today’s industry-leading architectures, where the A64FX [9], the H100 GPU [8], and the IBM training accelerator presented in [10] provide three examples of systems with an increasing level of specialization. The first architecture is the most flexible and targets high-performance computing with a 512-bit SIMD floating-point unit (FPU) capable of vectorial FMA. The GPU further specializes in data-parallel computation by reducing the control overhead even more than vector processors. It contains a large set of CUDA cores, capable of computing one FMA instruction per cycle, and a number of large tensor cores, each capable of performing up to 1024 dot-product operations per cycle with 8-bit FP precision. The third design is fully specialized for efficient NN training and inference. It implements two 8 × 8 arrays of mixed precision elements, each one supporting eight

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expanding dot products using 8-bit FP formats or eight 16-bit FMAs per cycle.

Focusing on RISC-V-based open-source academic designs, an interesting point in the design space is provided by Manticore [11], a chiplet-based hierarchically-scalable architecture that builds upon the replication of clusters where eight compute and one DMA cores share a scratchpad memory. Here, a tiny RISC-V core [12] is coupled to a large FP accelerator [13] and enhanced with instruction set architecture (ISA) extensions that maximize the FPU utilization. Manticore does not support the currently trending low-precision key FP formats, nor a fused operation unit for the fundamental operation of NN computation, i.e., the expanding sum of dot products.

In this paper, we present a novel parameterized FP SIMD unit supporting the core operations of NN training with support for two 8-bit and two 16-bit formats (Fig. 1). New formats for the unit can be rapidly defined thanks to its easy parameterization scheme. We evaluate this hardware unit standalone and in the context of an open-source RISC-V core cluster derived from Manticore, where we integrate the novel NN training capabilities. The main contributions of this work are the following:

1) We design an open-source parameterized multi-format unit supporting expanding sum-of-dot-product (ExSdotp) instructions, as well as non-expanding and expanding three-operand additions, called vector inner sum (Vsinn) and expanding vector inner sum (ExVsum). The hardware unit enables a 2x speedup with respect to computing on expanding FMAs (ExFMAs) while reducing the area and critical path by 30% compared to a cascade of two ExFMA units and preventing precision losses due to the non-associativity of two consecutive FP additions. We integrate the ExSdotp unit into an open-source multi-format FPU called FPnew [13].

2) We specify MiniFloat-NN: a RISC-V ISA extension for low-precision FP training on many-core architectures exploiting the new computational units. We integrate the enhanced FPU into an open-source RISC-V 8-core cluster based on Snitch cores [12] supporting the new ISA extension and sharing a fast-access software-managed scratchpad memory.

3) We carry out a detailed evaluation of the standalone ExSdotp unit and the enhanced compute cluster, providing area, performance, energy efficiency, and accuracy results.

II. RELATED WORK

A. Floating-Point Formats for NN Training

The shift towards less-than-32-bit formats for training – which started with the FP16 data type – witnessed a quite large set of new proposed formats. An overview of the relevant FP formats in the context of NN training is provided in Fig. 1. As many training algorithms benefit from a higher dynamic range than the one provided by FP16, TensorFloat-32 (TF32) [14] and bfloat16 [15] recently gained traction. Both formats preserve the 8-bit exponent and the corresponding dynamic range of FP32 while reducing the number of mantissa bits to 10 bits in the first case and 7 bits in the second case.

As the mantissa datapath dominates the area and power consumption of FP engines, reducing the mantissa width allows placing more computational units at the same area cost and enables larger efficiency improvements than lowering the number of exponent bits. Additionally, bfloat16 has been further optimized by handling rounding and special cases differently from the IEEE-754 directives, e.g., by flushing subnormals to zero [15]. On the A100 GPU, TF32 enabled a 10x performance speedup with respect to FP32 computations on its predecessor, the V100 GPU [14], while using bfloat16 on the NVIDIA A100 rather than TF32 enables a 2x higher performance. However, due to the low number of mantissa bits, the accumulation of bfloat16 products is usually performed in FP32. To mitigate the need for larger-precision accumulation, IBM introduced DLFloat [16], a 16-bit format composed of a 6-bit exponent and a 9-bit mantissa, thereby providing an intermediate dynamic range and precision with respect to FP16 and bfloat16. Finally, as different applications benefit more from different data types, Nannarelli proposed a variable precision 16-bit format [17] that can be set to represent FP16, bfloat16, DLFloat, and an additional data type with 7-bit exponents and a 9-bit exponent.

The significant benefits of using low-precision formats pushed researchers to investigate and demonstrate the feasibility of training models with 8-bit FP formats [6], [7]. Two formats, which we call FP8 and FP8alt, have gathered particular interest. FP8 consists of a 5-bit exponent, thus providing the same dynamic range as FP16, and a 2-bit mantissa, while FP8alt features a 4-bit exponent and a 3-bit mantissa. Sun et al. [7] demonstrated considerable improvements for a large set of NN training tasks by employing FP8alt in the forward propagation and FP8 in the backward pass. However, these studies relied on software emulation and were not reproduced on hardware platforms. NVIDIA recently released the H100 GPU [8], where these 8-bit formats are supported and provide a 2x speedup with respect to 16-bit data types. Nonetheless, hardware architectures supporting such formats are still rare and not well studied from the application viewpoint.

The vast set of FP data types being investigated and proposed motivates the need for a flexible open-source hardware platform in which new formats could be rapidly explored and supported.

B. Related Architectures

As a critical operation for a wide set of kernels, most modern processors provide support for FMA instructions, usually in a
non-expanding fashion. However, in the context of NN training, expanding operations get particularly interesting, as they allow using low-precision formats while retaining high accuracy [18]. To address this need, various ExFMA implementations have been investigated. Brunie [19] proposed an ExFMA unit multiplying FP16 inputs and accumulating in larger precision, while Mach et al. [13] designed an FPU for transprecision computing, containing a multi-format FMA capable of computing ExFMAs on a wide set of FP formats. However, ExFMAs do not use the FP register file efficiently, as shown in the left part of Fig. 2. Due to their unbalanced nature, they access only half of the data in two source registers, thus not fully exploiting all the information that can be packed into those registers while entirely using the third source register and the destination register. Furthermore, to use the entire register file space, subword accesses would be needed, as well as multiple instructions to cover all possible source locations. An ExSdotp instruction would instead consume all the available data, as shown in the right half of Fig. 2, preventing these drawbacks.

An expanding dot-product unit with accumulation computing \(a \times b + c \times d + e\) can be designed in a discrete or fused fashion. The first one places two consecutive ExFMA modules in a cascade, as shown in Fig. 3. A fused design requires more engineering effort, as it involves implementing the non-trivial three-term FP addition [20]. However, as a fused design allows for a single normalization and rounding step, improving the module’s area, timing and accuracy, it is often the best choice.

Sohn and Swartzlander [21] developed a fused FP dot-product unit computing \(a \times b + c \times d\). Additionally, they designed a non-expanding three-term FP adder [22], which, merged with their dot-product unit, can generate a dot-product unit with accumulation. These two designs were only implemented for single precision and double precision, and were not designed for expanding operations. Intel designed a fused floating-point many-term dot-product unit [23] computing 32 products and accumulating them in higher precision for the Nervana NN processor. The unit computes the products in bfloat16 and accumulates the result in single precision. However, it does not support 8-bit formats, which are now getting traction in the context of NN training. The Nervana dot-product unit increases its internal datapath to reduce, but not fully prevent, precision losses when cancellation causes a large normalization shift. Such losses would have a higher impact on low-precision FP formats, as their final results are more sensitive to small variations.

Zhang et al. [24] and Mao et al. [25] proposed two academic designs with multiple-precision dot-product capabilities. However, also these modules do not support 8-bit FP data types. On the contrary, the IBM AI chip [10] supports FP8 and FP8alt expanding dot products but is only capable of DLFLOAT FMA.

As low-precision data types present a high tradeoff between accuracy and dynamic range, supporting multiple formats allows for dynamically adapting to the application requirements. The FPU developed by Nannarelli [17] addresses this by defining a new variable-precision data type that can be set to FP16, bfloat16, DLFLOAT, and a fourth 16-bit custom format. However, no support for 8-bit formats was considered.

Finally, FPnew [13], being highly parameterized, can work on a wide set of FP data types, from 8-bit to 64-bit, and allows for a fast definition of new formats. Nonetheless, it does not provide support for dot-product instructions. Due to its highly configurable environment, we took the open-source FPnew as a starting point for our work. FPnew also provides a second advantage: it is included in a flexible and highly efficient compute cluster [12] that can be hierarchically replicated to form a large many-core system [11], enabling a fast exploration of our extensions on a real hardware platform.

In this work, we develop an open-source ExSdotp unit working on two 8-bit and two 16-bit formats and accumulating in higher precision, 16 bits and 32 bits, respectively. Our design is highly parameterized so that new formats can be easily defined and explored. We integrate a SIMD ExSdotp module in a lightweight open-source RISC-V processor called Snitch [12] to create a compute cluster with low-precision NN-training capabilities and extend its ISA with a custom RISC-V extension that we named MiniFloat-NN. Although ISA extensions for NN training have already been employed in commercial products, as in the Habana Gaudi2 [26], they are mostly closed-source and lack open information on the implementation breakdown costs and design tradeoffs. In this paper, we provide a detailed description and evaluation of the proposed hardware unit and ISA extension.

### III. Architecture

In the following, we discuss the supported FP formats in Section III-A and describe the architecture of our new FP ExSdotp unit capable of computing ExVsum and Vsum on the same datapath in Section III-B and III-C. The unit’s integration into an open-source modular energy-efficient multi-format FPU is discussed in Section III-D, while the architecture of our evaluation PE with the MiniFloat-NN extension and using our enhanced FPU with SIMD ExSdotp capabilities is introduced in Section III-E.
A. Supported FP Formats

The high parametrization of the open-source FPnew unit allows designers to select a specific set of supported FP formats, and quickly define new formats, thereby enabling fast research on new data types. For this work, we add the FP8alt definition and enable the following FP formats:

- FP64: 11-bit exponent, 52-bit mantissa
- FP32: 8-bit exponent, 23-bit mantissa
- FP16: 5-bit exponent, 10-bit mantissa
- FP16alt: 8-bit exponent, 7-bit mantissa
- FP8: 5-bit exponent, 2-bit mantissa
- FP8alt: 4-bit exponent, 2-bit mantissa

FP16alt matches the exponent and mantissa widths of widely-used bfloat16 but follows the IEEE-754 directives for rounding and subnormal number handling.

The extended FPU supports all the RISC-V FP instructions, except division and square root, for all the enabled formats. For our ExSdotp unit, we focus on low-precision formats. The expanding operations compute from 8 to 16-bit and from 16 to 32-bit formats, while the non-expanding Vsum is implemented for 8, 16, and 32-bit FP formats, as summarized in Table I.

B. ExSdotp Unit

The ExSdotp unit takes five operands, four inputs expressed in a w-bit source format (src fmt), and an accumulator input in a 2w-bit destination format (dst fmt) to compute a sum of dot products in the 2w-bit destination format:

\[ \text{ExSdotp}_{2w} = a_w \times b_w + c_w \times d_w + e_{2w} \] (1)

The ExSdotp module handles subnormals as all the other IEEE-754 operations and supports a parametric number of pipeline stages. Each instance of the ExSdotp unit is constrained by the largest exponent and mantissa widths enabled by the source and destination format parameterization. Enabled formats with narrower exponent and/or mantissa fields are mapped to the lower and upper bits of the wider exponent and mantissa field, respectively. This mapping scheme allows performing lower-precision computations on the same datapath, as well as adding new slightly different FP formats at a very low area overhead. A 16-to-32-bit module can support all the format combinations specified in Table I, while a narrower 8-to-16-bit unit can support all the combinations for ExSdotp but \{src fmt: FP16/FP16alt, dst fmt: FP32\}.

The data flow in the ExSdotp unit is shown in Fig. 4. For the sake of simplicity, the diagram does not depict the exponent datapath, which is responsible for computing the exponent differences used to sort the two products and the accumulator and to calculate the shift amounts. The maximum number of mantissa bits plus one (the hidden one) is called \( p_{\text{src}} \) and \( p_{\text{dst}} \) for source and destination formats, respectively.

Initially, the two mantissa products are computed, producing \( 2 \times p_{\text{src}} \)-wide results. Note that \( 2 \times p_{\text{src}} \) might differ from \( p_{\text{dst}} \). To match the same precision as the accumulator \( e_{\text{p.dst}} \), the mantissa products are padded with zeroes.

\[ \text{prod}_{\text{ab}}(p_{\text{dst}}) = \{a(p_{\text{src}}) \times b(p_{\text{src}}), 0(p_{\text{dst}} - 2 \times p_{\text{src}})\} \] (2)

After that step, what is left is a three-term addition. Three-term fused FP additions present additional challenges due to FP additions being non-associative [20]. As such, two consecutive FP additions might produce different results if performed in different orders. Higham [27] showed that arranging operands in increasing order before the summation is favorable in the case of one-signed data, while the decreasing ordering is preferable in the case of heavy cancellation. Focusing on our specific use case, Demmel and Hida [28] proved that the decreasing ordering reaches high accuracy when used with a wider accumulator and for a limited number of addends. In our hardware unit, we tackle precision losses by sorting the three
addends in decreasing order, increasing the internal precision, and implementing a single normalization and rounding stage.

To implement the three-term addition, we first sort the three addends, finding the maximum \( \max(p_{\text{dest}}) \), the intermediate \( \text{int}(p_{\text{dest}}) \), and the minimum absolute value \( \min(p_{\text{dest}}) \). After being zero-padded to match the increasing internal precision (e.g., \( \{\text{int}(p_{\text{dest}}), 0_{p_{\text{dest}+3}}\} \)), the intermediate and the minimum addends are right-shifted by their exponent difference to the maximum addends (exp_max – exp_int).

\[
\text{sum}(2_{p_{\text{dest}+3}}) = \max(2_{p_{\text{dest}+3}}) + \text{int}(2_{p_{\text{dest}+3}}) \tag{3}
\]

After summing the maximum and intermediate addends (3), an additional \( p_{\text{src}} \) bits are added by zero-padding \( \{\text{sum}(2_{p_{\text{dest}+4}}), 0_{p_{\text{src}}}\} \) to prevent catastrophic cancellations when the maximum addend is the result of a product between a normal and a subnormal value. In the last step before the normalization and rounding, the minimum addend is accumulated to the padded sum.

\[
\text{sum}_{\text{final}}(2_{p_{\text{dest}+p_{\text{src}}+4}}) = \text{sum}_{\text{max}}(2_{p_{\text{dest}+p_{\text{src}}+4}}) + \min(2_{p_{\text{dest}+p_{\text{src}}+4}}) \tag{4}
\]

Summing the addends with the largest absolute values first and gradually increasing the bitwidths at each step allows us to prevent precision losses that could occur when performing two FP additions. If the first sum produces a non-zero value, the increased precision will ensure enough precision bits even in case of cancellation in the second addition. Else, if the first sum produces an exact zero result, the possibly useful shifted-out bits of the minimum addend are recovered by directly assigning the minimum addend to the result of the second sum.

C. \text{ExVsum} and \text{Vsum} on the \text{ExSdotp Datapath}

By setting the inputs \( b_w \) and \( d_w \) to one, the ExSdotp unit can perform an ExVsum (5).

\[
\text{ExVsum}_{2w} = a_w + c_w + e_{2w} \tag{5}
\]

As discussed in Section III-B, the unit already contains all the logic necessary to perform a non-expanding three-term addition. To enable non-expanding Vsum (6) in the larger \( dst_{\text{fmt}} \), we increase the size of two inputs, operand \( a \) and \( c \), to the \( dst_{\text{fmt}} \) width by extending them with the \( a_{\text{vs}} \) and \( c_{\text{vs}} \) fields. The support for Vsum is added by bypassing the two mantissa multiplications, as shown in Fig. 4.

\[
\text{Vsum}_{2w} = a_{2w} + c_{2w} + e_{2w} \tag{6}
\]

Such an operation can be used to reduce and accumulate the results packed in a register after SIMD ExSdotp executions (see Fig. 2).

D. \text{SIMD Wrapper and Integration into FPnew}

FPnew is natively organized in modules, each one responsible for one operation group: ADDMUL, DIVSQRT, COMP (comparison), and CONV (conversion). When instantiating the top level, each module can be deactivated through a parameter. The configuration of the FPU coupled to Snitch has the DIVSQRT disabled, thus not containing the correspondent module. For our evaluation PE, we integrate an ExSdotp SIMD wrapper into FPnew as a new operation group module, SDOTP. Since the proposed PE supports double-precision instructions, the FP register file contains 64-bit entries. That allows for packing two FP32, four FP16/FP16alt, or eight FP8/FP8alt values in a single FP register. The FPnew interface accepts up to three 64-bit input operands and produces one 64-bit output per cycle. Therefore, we organize our SIMD wrapper in two 16-to-32-bit and two 8-to-16-bit ExSdotp, which means it will compute up to two 16-to-32-bit or four 8-to-16-bit ExSdotp operations each cycle. The SIMD wrapper is also responsible for unpacking the five operands from the 64-bit input and packing the result into 64-bits, as shown in Fig. 5.
We build our evaluation PE upon Snitch [12], a tiny open-source 32-bit RISC-V processor coupled with an FPU [13] instance supporting single and double-precision FP through a latency-tolerant acceleration interface. Snitch uses two custom ISA extensions to enable an FPU utilization of above 90%. The stream semantic register (SSR) extension maps a regular load or store access pattern to fixed floating-point registers, effectively eliminating most of the implicit load and store instructions; while the floating-point repetition instruction (FREP) extension allows to buffer and repeat a sequence of FPU instructions to prevent the loop overhead caused by branching instructions, and to relieve pressure on the instruction cache.

To build the MiniFloat-NN PE, we replace the native FPU instance with our enhanced FPU and extend the Snitch decoder to support the new instructions. We set the levels of pipeline registers to 3 for the SDOTP operation group, 3 for the ADDMUL, 2 for the CAST, and 1 for the COMP. Due to the limited encoding space, we did not replicate the same instruction for different FP formats sharing the same width. Instead, the alternative formats – FP16alt and FP8alt – are controlled by two additional bits, src_is_alt and dst_is_alt, in the FP control and status register (CSR). An FP16alt kernel will then differ from an FP16 kernel by a single CSR write. The MiniFloat-NN extension augments the smallFloat3 extension by adding ExSdotp, ExVsum, and Vsum SIMD instructions:

- exsdotp rd, rs1, rs2
- exvsum rd, rs1, rs2
- vsumm rd, rs1

For all the three instruction types rd also behaves as rs3/rs2, being the accumulator, and contains packed data in higher precision than the ones packed in rs1/rs2.

To evaluate our extensions, we replace the native Snitch core with the proposed MiniFloat-NN-capable PE in a Snitch cluster, where a set of eight such compute PEs share a 32-bank scratchpad memory, a DMA core, and an L1 instruction cache, as shown in Fig. 6.

IV. EXPERIMENTAL RESULTS

We evaluate the proposed ExSdotp unit and the enhanced compute cluster for area, performance, energy efficiency, and accuracy, and compare them against related state-of-the-art (SoA) architectures.

A. Area and Timing

We use SYNOPSYS FUSION COMPILER 2021.06 to synthesize the ExSdotp unit and synthesize, place, and route the Minifloat-NN-capable cluster in GLOBALFOUNDRIES’ 12 nm FinFET technology. First, we consider the ExSdotp unit standalone, without any pipeline stage, and target a relaxed clock period of 333 MHz in a worst-case corner (0.72 V, 125°C). Since two ExFMA modules, arranged in a cascade, can perform a dot product, we compare our 16-to-32-bit and 8-to-16-bit units against a set of two ExFMA modules supporting the same data types. Note that the cascade of ExFMA units will not compute exactly the same operation as it rounds twice and does not mitigate potential adverse effects of the non-associativity of FP additions. Furthermore, a cascade of ExFMA cannot compute Vsum. Since the second ExFMA unit in the cascade requires the output of the first as an input, in an implementation with no pipeline registers, each ExFMA instance is required to work at 667 MHz to ensure that the cascade will run at 333 MHz as the ExSdotp unit. We synthesize the FPnew ExFMA unit with such a constraint and provide the area results in Fig. 7a. The ExSdotp occupies around 30% less area than two ExFMAs and shows around 30% of critical path reduction. Then, we synthesize, place and route the extended Snitch cluster, targeting 950 MHz in the worst-case scenario. To achieve the higher frequency, we insert in the enhanced FPU 3 levels of pipeline registers for the SDOTP operation group, 3 for the ADDMUL, 2 for the CAST, and 1 for the COMP. The extended computing cluster occupies 4.3 MGE and, in a typical corner (0.8 V, 25°C), achieves 1.26 GHz. The ExSdotp
SIMD module occupies 44.5 kGE, amounting to 27% of the overall area of the FPU, which occupies 165 kGE (Fig. 7b).

B. Performance

We implement and measure a collection of FMA and ExSdotp-based general-matrix-multiplication (GEMM) kernels for different formats and problem sizes. We consider only GEMM sizes that fit entirely into the 128 kB local scratchpad memory. The kernels are compiled with an extended LLVM-12 compiler using intrinsics for our new instructions. All implemented kernels make use of the SSR and FREP custom ISA extensions of Snitch [12]. We run the kernels on the enhanced Snitch cluster and measure the execution cycles in cycle-accurate RTL simulation using MENTOR QUESTASIM.

Using our new expanding instructions allows reducing the memory footprint remarkably. We can fit up to $128 \times 256$ GEMMs into the memory when leveraging the new 8-to-16-bit ExSdotp support, while FP16-only and FP64 kernels fit a size of $128 \times 128$ and $64 \times 64$, respectively.

The MiniFloat-NN extension enables a peak utilization of 8 FLOP/cycle for 16-to-32-bit GEMMs, and 16 FLOP/cycle for 8-to-16-bit GEMMs. That doubles the peak performance achievable with ExFMAs whose SIMD implementation suffers from inefficient register file usage, see Fig. 2. Moreover, it doubles the peak utilization compared with non-expanding FMAs computing in the dst_fmt, and matches the peak performance for the non-expanding FMAs computing in the src_fmt while providing higher internal precision.

The total execution cycles and achieved performance are reported in Table II and Fig. 8, respectively. Using a 16-to-32-bit ExSdotp reduces the number of cycles by up to 10% compared to the FP16 FMA kernel. This benefit comes from the expanding operation, which halves the number of intermediate results that get reduced at the end of the computation compared to the FMA-based kernel.

With a constant problem size, the speed-up when halving the format size is, in the worst case, $1.56 \times$ instead of the ideal $2 \times$. The reason for this overhead is the overhead generated by setting up the SSR streams and initializing registers, which stays largely the same while the number of compute instructions inside the repeated loop is halved. Such overheads impact less and less on the results when increasing the problem size. The $128 \times 256$ FP8-to-FP16 GEMM achieves 1.96× and 7.23× the FLOP/cycle of the $128 \times 128$ FP16-to-FP32 GEMM and the $64 \times 64$ FP64 GEMM, respectively. Note that the FP64 kernel, as non-expanding and non-SIMD, does not suffer from these additional overheads.

C. Power and Energy Efficiency

To assess the power consumption and energy efficiency of the placed-and-routed extended cluster, we simulate an ExSdotp-based GEMM with MENTOR QUESTASIM, annotating the switching activity data. We extract the average power consumption with SYNOPSYS PRIMEPOWER under typical conditions (0.8 V, 25 °C). When computing $128 \times 256$ FP8-to-FP16 GEMMs at 1.26 GHz, the MiniFloat-NN cluster achieves 128 GFLOPS consuming 224 mW, thus achieving 575 GFLOPS/W (where 1 ExSdotp is counted as 4 FLOP).

Our extended cluster compares favorably with the native Snitch system, which, implemented in a 22 nm technology (at 1 GHz, 0.8 V, 25 °C) in [12], reaches 80 GFLOPS/W when computing FP64 GEMMs. Our extended cluster working on FP8-to-FP16 kernels reaches 7.2× the efficiency of the native Snitch system computing in double precision. We summarize the benefits introduced at a system level by our MiniFloat-NN RISC-V extension by comparing the extended cluster against its baseline version in the bottom two rows of Table III.

D. Accuracy

To evaluate the accuracy of the proposed ExSdotp unit, we accumulate an increasing number of dot products. We generate

| Design          | Technology | Voltage | Frequency | Area | DotP | Performance [FLOP/cycle] | Peak Throughput [GFLOPS] | Efficiency [GFLOPS/W] |
|-----------------|------------|---------|-----------|------|------|--------------------------|-------------------------|-----------------------|
| ExSdotp FPU     | 12 nm      | 0.8 V   | 1.26 GHz  | 0.019 mm² | yes | 8/8 8/8 16/16 16/16 | 20.2 (exFP32) 1631 (exFP32) |
| FPnew [13]      | 22 nm      | 0.8 V   | 0.923 GHz | 0.049 mm² | no  | 4/8 4/8 8/16 8/16 | 14.8 (FP32) 1245 (FP32) |
| Miao et al. [25] | 28 nm | 1.0 V   | 1.43 GHz  | 0.013 mm² | yes | -/- -/- 20/- 20/- | 28.6 (FP32) 975 (FP32) |
| Zhang et al. [24] | 90 nm | 1.0 V   | 667 GHz   | 0.19 mm²  | yes | -/- 8/8 -/- -/-  | 5.3 (FP16) 113 (FP16) |

TABLE III
COMPARISON OF FPUS SUPPORTING LOW-PRECISION FORMATS (TOP FOUR ROWS) AND EVALUATION OF THE MINIFLOAT-NN EXTENSION (BOTTOM TWO ROWS)

| Operation     | Format       | n = 500 | n = 1000 | n = 2000 |
|---------------|--------------|---------|----------|----------|
| ExSdotp       | FP8-to-FP16  | 0.11 x 10^7 | 5.4 x 10^7 |          |
| ExFMA         | FP8-to-FP32  | 7.6 x 10^7  | 1.8 x 10^7 | 9.9 x 10^7 |
| ExSdotp       | FP8-to-FP16  | 5.9 x 10^4  | 2.7 x 10^4 | 3.9 x 10^3 |
| ExFMA         | FP8-to-FP32  | 5.9 x 10^4  | 8.2 x 10^3 | 1.2 x 10^2 |

TABLE IV
ACCURACY COMPARISON BETWEEN EXSDOTP AND EXFMA

\* The golden FP64 result is converted to FP32/FP16 for the error calculation.
the inputs randomly, with a Gaussian distribution, in the source precision. We then perform the accumulations using: (i) low-precision ExSdotps, (ii) low-precision ExFMAs, and (iii) FP64 ExFMAs. We report the comparison result of the ExSdotp unit against the ExFMA in terms of relative error against the FP64 golden model in Table IV.

As different errors can compensate during the accumulation, the precision results vary with the selected number of inputs. However, the ExSdotp unit consistently shows better accuracy than the ExFMA for FP16-to-FP32 and FP8-to-FP16 workloads. The absolute accuracy improvement grows when the input operands have smaller bitwidths.

E. SoA comparison

We compare our enhanced FPU against its baseline counterpart, FPnew, and two recent SoA architectures with low-precision support in Table III. The PEs proposed by Mao et al. [25] and Zhang et al. [24] compute SIMD FMA or dot-product operations with different precisions, 16-bit and higher, while FPnew also supports FP8. However, none of them can work with FP8 data. Our extended FPU, thanks to the proposed ExSdotp SIMD unit, achieves the highest energy efficiency among the selected mixed-precision PUs. It outperforms the modules developed by Zhang et al. [24] by 14.4×, and the multiple-precision PE by Mao et al. [25] by 1.7×. Furthermore, it provides 30% higher efficiency than FPnew working with FP8 data and doubles its peak performance when using expanding operations.

V. CONCLUSION

We presented an ISA extension for low-precision NN training on RISC-V cores. The new instructions are carried out on the proposed SIMD unit composed of a set of modules computing expanding FP dot products and reusing the same hardware to calculate expanding and non-expanding three-term additions. The ExSdotp unit supports two 16-bit and two 8-bit input formats. Thanks to the module’s parameterization, new formats can be rapidly defined and explored. The proposed ExSdotp module performs twice the computations and exploits the FP register file more efficiently than an expanding FMA while providing higher accuracy. The ISA extension has finally been implemented in an open-source PE, composed of a tiny RISC-V processor coupled with an FPU enhanced with our SIMD ExSdotp unit. A cluster containing eight of such extended PEs implemented in 12 nm technology achieves 160 GFLOPS of peak performance and 575 GFLOPS/W of energy efficiency when computing FP8-to-FP16 GEMMs at 1.26 GHz, 0.8 V.

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