A fully integrated digital LDO with voltage peak detecting and push-pull feedback loop control

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Abstract: A push-pull multi-loop architecture for the digital low drop-out (D-LDO) regulators is presented with small variations of output voltage and 200 mA load capacity. The propose D-LDO adopts voltage peak detector (VPD) to observe the output voltage ripples. Once undershoot or overshoot on output voltage is detected, the push-pull feedback loop is quickly triggered, which minimizes the voltage shoots even if the load current changes abruptly. Meanwhile, the shift register (S/R) feedback loop regulates the output voltage to desired value with high accuracy. Hence the D-LDO recovers steady state with greatly small voltage spikes. The proposed D-LDO is designed and simulated in SMIC 65 nm CMOS process with a 0.42 mm\(^2\) active area. The simulated voltage overshoot and undershoot are 27 and 26 mV respectively, with load step of 20 to 200 mA with a 10-ns edge time. The max load current and quiescent current are 200 mA and 400 \(\mu\)A, respectively, and the peak current efficiency is 99.8%.

Keywords: low drop-out (LDO) regulator, voltage peak detector (VPD), shift register (S/R), push-pull feedback loop

Classification: Integrated circuits

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1 Introduction

Systems-on-Chips (SoCs) integrating many individual blocks (such as memory, digital circuits, analog-to-digital converters among others) becomes more widely used in different applications. Power management circuit like LDO is becoming critical to provide a clean and regulated power supply for each individual block in SoCs [1]. LDO can be classified into analog LDO (A-LDO) [2] and digital LDO (D-LDO) [3, 4]. Digital LDOS are gaining more attention since they have the advantages of suitable for low operating voltages [3], easy integration, small size, programmability, high stability over a wide range of load current variations and a lower sensitivity to process variations [4]. A baseline discrete-time digital LDO usually consists of a comparator, a serial-in parallel-out bidirectional shift register (S/R), and a P-channel MOSFET (PMOS) array acting as the power transistors [5]. In these discrete-time digital LDOS, S/R shifts the control signal according to the result of voltage comparator to turn on/off PMOS transistors and regulates the
output voltage with a master clock. Thus the generation and propagation of control signal will be synchronous. Due to their synchronous and sequential nature of switching, the baseline digital LDOs suffer from slower transient responses to large load current steps resulting in a large voltage undershoot/overshoot and show a tradeoff between steady-state stability and transient response [6].

Several previous works have been proposed to tackle this issue. A gated voltage controlled oscillator (GVCO) with counters is used in [7] to provide more “continuous” information of the digitalized output voltage level. Based on that information, the D-LDO in [7] controls multiple power transistors concurrently and the transient performance is improved. However, the inherent sensitivity to PVT variations limits its applications. Asynchronous control and adaptive sizing that changes resolution are applied in the D-LDO, targeting at a balance in high speed and fine resolution in [8]. Similarly to [7], the PVT variations become a headache too. The D-LDO presented in [9] using a SAR-type ADC and a separate DAC driving a single power transistor. But, this design is not power-efficient since its complex design consumes additional quiescent current. Another work shown in [10] adopts a TDC-based 4-b ADC and a PID controller for stability compensation. In that design, the performance of fast transient response is achieved through dynamic clock scaling from normally 250 MHz to 1 GHz. However, it consumes large quiescent current of 2.5 mA. To trade-off between transition response and steady performance, the coarse-fine tuning technique is widely used such as in [5, 11]. Briefly, coarse-fine tuning technique mainly includes two aspects, namely the coarse-tuning and fine-tuning. The coarse-tuning with more power MOS units and high sampling frequency enhances transient performance while the fine-tuning with small power MOS units and slow sampling frequency achieves high steady and low quiescent current. Unfortunately, the coarse/fine-turning algorithm leads to complexity of controlled block.

In this paper, a novel all digital LDO (D-LDO) with voltage peak detecting and push-pull feedback loops is presented. The proposed D-LDO can achieve small voltage spikes, low quiescent current, and up to 200-mA load current capacity. This brief is organized as follows. The architecture and core circuit of our proposed D-LDO is illustrated in Section 2. Steady and small signal model analysis is presented in Section 3. Simulation results are shown in Section 4. Finally, conclusions are made in Section 5.

2 Implementation and design considerations

2.1 Architecture of proposed D-LDO
The architecture of the proposed digital LDO is presented in Fig. 1. Push-pull topology as in [12] is used for multi-loop operation. Generic digital LDO is comprised of load RC network, clock comparator CMP2, shift register S/R and P-channel MOSFET (PMOS) array (PG0 to PG159) acting as the power transistors. In the proposed architecture, a push-pull feedback loop trigger (PP-FLT) scheme is embedded in the generic digital LDO to control the push-pull output stage that consists of PMOS array (PG0 to PG159) and N-channel MOSFET (NMOS) transistor NG. As shown in Fig. 1, there are three feedback loops in the proposed
architecture, namely \( L_{SR} \), \( L_P \) and \( L_N \). The shift register (S/R) feedback loop \( L_{SR} \) that includes load RC network, clock comparator CMP2, shift register S/R and the PMOS array is widely used in generic D-LDO to regulate the output voltage to a desired value under difference load conditions, while the proposed push-pull feedback loops \( L_P \) and \( L_N \) consisting of load RC network, PP-FLT scheme and the push-pull output stage are employed to reduce the variations of \( V_{OUT} \).

The undershoot and overshoot detection boundaries are \( (2V_{REF} - \Delta V_L) \) and \( (2V_{REF} + \Delta V_H) \), where \( 2V_{REF} \) denotes the desired value of \( V_{OUT} \) in steady state, \( \Delta V_L \) is the predetermined undershoot detection threshold, and \( \Delta V_H \) is the overshoot detection threshold. When \( V_{OUT} \) is within the range between \( (2V_{REF} - \Delta V_L) \) and \( (2V_{REF} + \Delta V_H) \), the D-LDO works only at \( L_{SR} \)-turning mode, at which only shift register (S/R) feedback loop \( L_{SR} \) is available to ensure that \( V_{OUT} \) incessantly tracks the desired voltage. On the other hand, once \( V_{OUT} \) exceeds undershoot or overshoot detection boundaries \( (2V_{REF} - \Delta V_L) \) or \( (2V_{REF} + \Delta V_H) \), the \( L_P \)-turning or \( L_N \)-turning mode is quickly triggered while \( L_{SR} \)-turning mode is always available. In this scenario, the push-pull feedback loop \( L_P/L_N \) is enable to prevent a large undershoot/overshoot on \( V_{OUT} \) while the \( L_{SR} \) regulates the \( V_{OUT} \) to \( 2V_{REF} \) with a desired load current.

To achieve wide bandwidths of push-pull feedback loops \( (L_P, L_N) \), a high frequency (1 GHz) clock (\( CK_{HF} \)) is employed in the PP-FLT scheme, in addition, the push-pull output stage is directly controlled by PP-FLT scheme. Though a high frequency clock is needed, it is only used to trigger two clock comparators in PP-FLT scheme. Thus the increment of power consumption caused by the high frequency clock is negligible. For lower quiescent current and higher accuracy in
steady state, the D-LDO operates only on the LSR-turning mode, with a small power MOS strength and low frequency (50-kHz clock (CKLF). Therefore, with the proposed PP-FLT scheme, the D-LDO could effectively improve transient response and achieve low quiescent current simultaneously.

2.2 Push-pull feedback loop trigger (PP-FLT) scheme

As shown in Fig. 2, the PP-FLT scheme includes a voltage peak detector (VPD), a 2-input OR gate, a 2-input INAND gate and a 2-input AND gate, whereas VPD is composed of 2 clock comparators (CMP0, CMP1) and a 2-input XNOR gate. The VPD is used to detect the undershoot/overshoot on VOUT, which outputs 1 if VOUT is not within the range between \((2V_{\text{REF}} - \Delta V_L)\) and \((2V_{\text{REF}} + \Delta V_H)\). With the output of VPD (PPFL\(_{\text{EN}}\)) becoming high, the signal DIRE\(_{\text{HF}}\) generated by the OR gate indicates whether undershoot on VOUT was detected or overshoot. Then signals PPFL\(_{\text{EN}}\) and DIRE\(_{\text{HF}}\) are fed to the INAND gate as well as AND gate to generate the control signals CTRL\(_P\) and CTRL\(_N\). The signals CTRL\(_P\) and CTRL\(_N\) determine which feedback loop of LP and LN will be triggered after undershoot/overshoot on VOUT has been detected.

![Proposed push-pull feedback loop trigger (PP-FLT) scheme with voltage peak detector (VPD).](image)

The operation processes of PP-FLT scheme are given in Fig. 3. In the first case [see Fig. 3(a)], under certain disturbances, the output voltage decreases by \(\Delta V_L\), resulting in a variation \(\Delta V_{\text{FBH}}\) of feedback voltage \(V_{\text{FBH}}\). When the \(V_{\text{FBH}}\) drops below reference voltage \(V_{\text{REF}}\), the output of CMP0 (denoted as \(q_0\)) changes from 1 to 0 while the output of CMP1 (marked by \(q_1\)) remains constant 0 since the \(V_{\text{FBL}}\) is always below \(V_{\text{REF}}\). Once \(q_0\) becomes low, the output of VPD (illustrated as PPFL\(_{\text{EN}}\)) flips from 0 to 1 while signal DIRE\(_{\text{HF}}\) changes to 0, indicating that undershoot on VOUT has been detected. Then, the signal CTRL\(_P\) becomes 0, which will trigger the push pull feedback loop LP to suppress the undershoot voltage. The process of deriving \(\Delta V_L\) is shown below.

Both of the \(V_{\text{FB}}\) and \(V_{\text{FBH}}\) come from the load bias resistor ladder consisted of \(R_1\) and \(R_2\), hence \(V_{\text{FBH}}\) is a function of VOUT, as given by

\[
V_{\text{FBH}} = \frac{2R_1 + R_2}{2(R_1 + R_2)} V_{\text{OUT}}.
\]
At time $t_0$, Eq. (1) is expressed as

$$V_{FBH|t_0} = (V_{FBH@SS} - \Delta V_{FBH}) = \frac{2R_1 + R_2}{2(R_1 + R_2)} (V_{OUT@SS} - \Delta V_L),$$  

(2)

where $V_{OUT@SS}$ and $V_{FBH@SS}$ denote the values of $V_{OUT}$ and $V_{FBH}$ at beginning steady state, respectively. The $V_{OUT@SS}$ is given by

$$V_{OUT@SS} = 2V_{REF},$$  

(3)

while the $V_{FBH@SS}$ is given by

$$V_{FBH@SS} = \left(\frac{2R_1 + R_2}{2(R_1 + R_2)}\right) V_{OUT@SS} = \left(\frac{2R_1 + R_2}{2(R_1 + R_2)}\right) 2V_{REF},$$  

(4)

hence $V_{FBH@SS}$ becomes

$$V_{FBH@SS} = k_1(2V_{REF}),$$  

(5)

where

$$k_1 = \frac{2R_1 + R_2}{2(R_1 + R_2)}.$$  

(6)

In order to trigger the push-pull feedback loop $L_P$, the feedback voltage $V_{FBH}$ needs to satisfy the following condition

$$V_{FBH} < V_{REF}.$$  

(7)

At time $t_0$, Eq. (7) becomes

$$V_{FBH|t_0} = \frac{2R_1 + R_2}{2(R_1 + R_2)} (V_{OUT@SS} - \Delta V_L) < V_{REF}.$$  

(8)

By solving the Eq. (3) and Eq. (8), $\Delta V_L$ is calculated as

$$\Delta V_L > \frac{1}{2 + \frac{R_2}{R_1}} (2V_{REF}).$$  

(9)
The undershoot detection threshold is defined as
\[ \Delta V_L = \frac{1}{2 + R_2/R_1} (2V_{REF}). \]  
(10)

On the other hand [see Fig. 3(b)], the output voltage \( V_{OUT} \) increases by \( \Delta V_H \), leading to a variation \( \Delta V_{FBL} \) of feedback voltage \( V_{FBL} \). Once the \( V_{FBL} \) is higher than \( V_{REF} \), the CTRL\(_N\) thus changes from 0 to 1, which enables LN-turning mode to reduce the overshoot on \( V_{OUT} \). Similarly to \( k_1 \), parameter \( k_2 \) shown in Fig. 3(b) as well as Fig. 3(a) is expressed as
\[ k_2 = \frac{R_2}{2(R_1 + R_2)}. \]  
(11)

Analogously to \( \Delta V_L \), the overshoot detection threshold \( \Delta V_H \) is defined as
\[ \Delta V_H = \frac{R_1}{R_2} (2V_{REF}). \]  
(12)

Therefore the voltage shoot detection thresholds (marked by \( \Delta V_L \), \( \Delta V_H \)) are proportional to the \( R_1/R_2 \). In this Letter, \( V_{REF} = 0.5 \) V, \( R_1 = 0.1 \) K\( \Omega \), \( R_2 = 4.9 \) K\( \Omega \) and \( R_1/R_2 = 1/49 \). Thus \( \Delta V_L \approx 19.6 \) mV, \( \Delta V_H \approx 20 \) mV.

### 2.3 Clocked comparator and S/R

As given in Fig. 4(a), the clocked comparator scheme introduced in [5] is used in the proposed D-LDO. A latch following the first stage restores the output signal. The comparator operates with two phases, namely pre-charge phase and regenerative phase. When CLK signal is low (pre-charge phase), the internal nodes are pulled to high while the latch outputs keep unchanged; when CLK rises to high (regenerative phase), the comparator accumulates the difference between \( V_{INP} \) and \( V_{INN} \) and rapidly amplifies the small difference to full swing, then the output latch will restore the output signal. Table I is the true table of the clocked comparator.

| \( V_{INP} \) | \( V_{INN} \) | CMPOUT |
|-----------|-----------|--------|
| \( V_{INP} \lt V_{INN} \) | “1”       | |
| \( V_{INP} \gt V_{INN} \) | “0”       | |

Table I. True table of clocked comparator

Fig. 4(b) shows the scheme of the 160-bit shift register (S/R), which consists of D-type flip-flops and multiplexers. The \( Q[159:0] \) are the outputs of S/R, which control the PMOS array PG\(_{159}\sim\)PG\(_0\). When DIRE is low, all the bits Q are shifted to the right by one count at the rising edge of the sampling clock CLK and vice versa, indicating one more PMOS transistor to turn on/off.

### 2.4 Operation principles

The operation principles of the proposed D-LDO are depicted in Fig. 5. In steady state, the D-LDO works only at L\(_{SR}\)-turning mode, with a small PMOS transistor step and low frequency clock \( CK_{LF} \). As shown in Fig. 5(a), when the load current \( I_L \) changes abruptly from 20 to 200 mA, \( V_{OUT} \) starts to drop. The S/R feedback
loop (LSR) senses the V_{OUT} drop and generates more logic low control signal among Q[159:0], which will turn on more extra PMOS transistors to suppress V_{OUT} drop. However, since the transition speed of LSR is quite slow, V_{OUT} keep going downward. At time t_0, when V_{OUT} exceeds the undershoot detection boundary (2V_{REF} - \Delta V_L), the output of PP-FLT scheme (i.e. CTRL_P) immediately set to logic 0. So, L_P-turning mode is triggered and all of the PMOS transistors (PG_0 to PG_{159}) are turned on to charge the C_L with theatrically strength current. Then V_{OUT} recovers to the level above (2V_{REF} - \Delta V_L) quickly. As thus, signal CTRL_P reset to logic 1 disabling L_P-turning mode at time t_1, which leads V_{OUT} to go downward and exceed (2V_{REF} - \Delta V_L) once more at time t_2. Then, L_P-turning mode is enabled and regulates V_{OUT} to the level above (2V_{REF} - \Delta V_L) again. Next, L_P-turning mode is disabled and enabled alternately to limit V_{OUT} drop until enough PMOS transistors are turned on by S/R. Hence the V_{OUT} successfully recovers to common level with greatly small undershoots. Finally, S/R keeps regulating V_{OUT} closer to the desired value and makes the D-LDO enter steady state.

Fig. 5(b) shows the case of load current decreasing abruptly from 200 to 20 mA. Once V_{OUT} exceeds the overshoot detection boundary (2V_{REF} + \Delta V_H), the PP-FLT scheme triggers the L_N-turning mode by setting CTRL_N to 1, which turns on the NMOS transistor N_Q to discharge the C_L with strength current, hence, V_{OUT} immediately drops to below level of (2V_{REF} + \Delta V_H). To limit the overshoots on V_{OUT}, the L_N-turning mode toggles between on and off alternatively depending on whether V_{OUT} exceeds (2V_{REF} + \Delta V_H) or not. Simultaneously, L_{SR}-turning mode is available and S/R generates more logic high control signal among Q[159:0] to turn off extra PMOS transistors. After most of the extra PMOS transistors have been turned off, L_N-turning mode is not need to be triggered any more. Finally, D-LDO continues to work at L_{SR}-turning mode which adjusts V_{OUT} closer to 2V_{REF} and steady state is hence achieved.
These operations prevent large spikes on $V_{OUT}$ and significantly improve transition response.

### 3 Steady analyses

Fig. 6 is the illustration of unsteady push-pull feedback loop control. The region from $t_0$ to $t_1$ depicts that all PMOS transistors are turned on at time $t_0$ to charge $C_L$ with charged current $I_{PGMAX}$ and pull $V_{OUT}$ up. However, since either the $C_L$ is too small or $I_{PGMAX}$ is too strong, $V_{OUT}$ quickly goes upward to $(2V_{REF} + \Delta V_H)$ within a period of $C_{KF}$. At time $t_1$, the D-LDO directly toggles from LP-turning mode to LN-turning mode without entering steady state. Hence, with $L_P$ releasing control of PMOS array, NMOS transistor $N_G$ is turned on immediately by feedback loop $L_N$ to discharge $C_L$ with discharged current $I_{NGMAX}$, leading to $V_{OUT}$ goes downward. Unfortunately, the $V_{OUT}$ unexpectedly drops to $(2V_{REF} - \Delta V_L)$ at next clock rise edge (namely at time $t_2$) leading to $L_P$-turning mode be enable again. As thus, $C_L$ is charged and discharged alternatively within adjacent clock period of $C_{KF}$. $V_{OUT}$
thus oscillates between \((2V_{\text{REF}} - \Delta V_L)\) and \((2V_{\text{REF}} + \Delta V_H)\) with a period of \(2T_{\text{HF}}\), resulting in unsteady problems. To avoid that unwanted unsteady state, the variation of charged and discharged voltage \((\Delta V_{\text{CL}})\) within a period \((T_{\text{HF}})\) of \(\text{CK}_{\text{HF}}\) should be smaller than \((\Delta V_L + \Delta V_H)\). Hence the steady conditions of push-pull feedback loop control are given as follows

\[
\frac{I_{\text{PGMAX}}T_{\text{HF}}}{C_L} \leq (\Delta V_L + \Delta V_H) \quad (13)
\]

\[
\frac{I_{\text{NGMAX}}T_{\text{HF}}}{C_L} \leq (\Delta V_L + \Delta V_H) \quad (14)
\]

where \(I_{\text{PGMAX}}\) and \(I_{\text{NGMAX}}\) are maximum current available to charge and discharge the \(C_L\), respectively. The value of \(C_L\) can be given by solving Eq. (13) and Eq. (14).

\[
C_L \geq \max \left\{ \left( \frac{I_{\text{PGMAX}}T_{\text{HF}}}{\Delta V_L + \Delta V_H} \right), \left( \frac{I_{\text{NGMAX}}T_{\text{HF}}}{\Delta V_L + \Delta V_H} \right) \right\} \quad (15)
\]

In the proposed D-LDO, the \(I_{\text{PGMAX}}\) and \(I_{\text{NGMAX}}\) are approximately 200 mA, \(T_{\text{HF}}\) is 1 ns, and \((\Delta V_L + \Delta V_H)\) is approximately 40 mV. Thus \(C_L\) becomes as follows

\[
C_L \geq 5 \text{ nF} \quad (16)
\]

The small signal model of S/R feedback loop \(L_{\text{SR}}\) in the proposed D-LDO is shown in Fig. 7(a) which is made up of a sampled comparator CMP2, a shift register (S/R), a zero-order hold (ZOH), and a first-order plant representing the continuous time plant consisting of the PMOS transistor array and the RC load. A feedback coefficient \(\beta = 1/2\) has been inserted into the feedback loop because the feedback voltage \(V_{\text{FB}}\) is generated by the load bias resistor ladder and \(V_{\text{FB}} = 1/2V_{\text{OUT}}\). The open-loop transfer function \(G(z)\) is written as Eq. (17) according to [13]

\[
G(z) = K_{\text{DC}}(1 - e^{-\alpha T}) \frac{z}{(z - 1)(z - e^{-\alpha T})} \quad (17)
\]

where \(K_{\text{DC}}\) is the loop \(DC\) gain, \(\alpha\) is the time constant of the output pole, and \(T\) is the sampling time interval of \(S/R\). In the synchronous S/R feedback loop, sampling time interval \(T\) equals to the period of \(\text{CK}_{\text{LF}}\) which is 20 µs. Since the feedback coefficient \(\beta = 1/2\), the overall closed loop transfer function of the digital LDO in the \(z\)-domain can be written as Eq. (18)
\[ H(z) = G(z) \left( 1 + \frac{1}{2} G(z) \right). \] (18)

Eq. (18) provides insight into the stability of the proposed D-LDO. The root loci of this system can be plotted in Fig. 7(b). All of the poles in z-domain are within the unit circle to guarantee the steady of the proposed D-LDO system under the heavy and light load conditions.

4 Simulated results

The proposed D-LDO has been designed and simulated in the SMIC 65 nm process with 1.2 V supply and 1.0 V output voltage. The HSIM is chosen as the SPICE simulator. According to the transistor level simulation results shown in Fig. 8, the output overshoot and undershoot voltages are 27 and 26 mV, respectively, with load steps of 20 to 200 mA with a 10-ns edge time, while they are 183 and 1363 mV, respectively, when the push-pull feedback loop is not engaged. On the other hand, with the push-pull feedback loop control, the steady voltage ripples are not degraded, which are simulated to be 15 and 7 mV under 20 and 200 mA load current, respectively. And the setting time is approximately 1.25 ms. In addition, the quiescent current is only 400 µA with maximum load current up to 200 mA. When \( I_L = 200 \) mA, the current peak efficiency is 99.8%. The output capacitance is 1 µF.

With the help of Layout XL in Virtuoso, the estimated layout area is around 0.42 mm\(^2\) except for output capacitor.

The proposed D-LDO is compared with prior arts, as shown in Table II. The output voltage variation (\( \Delta V_{\text{OUT}} \)) enhancement over previous work is notable. In order to compare the key performances of the proposed D-LDO with other state-of-art designs, the figure-of-merit for response time (FOM\(_{\text{RESP}}\)) presented in [14] is employed. A larger FOM\(_{\text{RESP}}\) implies faster response performance.
5 Conclusions

This paper presents a novel D-LDO with voltage peak detecting and push-pull feedback loop operation. The proposed D-LDO operates at 1.2 V supply and 65 nm technology. The simulation results show that the proposed D-LDO’s transient response performance has been significantly improved owing to the proposed voltage peak detecting technique and push-pull feedback loop control. In addition, the proposed D-LDO achieves maximum load capability up to 200 mA.

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