Optimizing FPGA-based Accelerator Design for Large-Scale Molecular Similarity Search

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Abstract—Molecular similarity search has been widely used in drug discovery to identify structurally similar compounds from large molecular databases rapidly. With the increasing size of chemical libraries, there is growing interest in the efficient acceleration of large-scale similarity search. Existing works mainly focus on CPU and GPU to accelerate the computation of the Tanimoto coefficient in measuring the pairwise similarity between different molecular fingerprints. In this paper, we propose and optimize an FPGA-based accelerator design on exhaustive and approximate search algorithms. On exhaustive search using BitBound & folding, we analyze the similarity cutoff and folding level relationship with search speedup and accuracy, and propose a scalable on-the-fly query engine on FPGAs to reduce the resource utilization and pipeline interval. We achieve a 450 million compounds-per-second processing throughput for a single query engine. On approximate search using hierarchical navigable small world (HNSW), a popular algorithm with high recall and query speed. We propose an FPGA-based graph traversal engine to utilize a high throughput register array based priority queue and fine-grained distance calculation engine to increase the processing capability. Experimental results show that the proposed FPGA-based HNSW implementation has a 103385 query per second (QPS) on the Chembl database with 0.92 recall and achieves a 35× speedup than the existing CPU implementation on average. To the best of our knowledge, our FPGA-based implementation is the first attempt to accelerate molecular similarity search algorithms on FPGA and has the highest performance among existing approaches.

I. INTRODUCTION

In drug discovery, molecular similarity search [1] has been widely used to identify structurally similar compounds from large molecular databases rapidly. Unlike image or document search in multimedia data retrieval, chemists often compute the Tanimoto or Jaccard similarity coefficient to measure the pairwise similarity. The distance between a query and a known molecule database can be measured through the K nearest neighbor (KNN) similarity search. In general, there are two types of search methods, exhaustive search, and approximate search. Exhaustive KNN search requires a linear scan through the entire database. Approximate methods reduce search complexity in exchange for search precision. As the size of compound libraries increases, efficient similarity search techniques are highly desired. Existing works mainly focus on using CPU and GPU to accelerate the computation of the Tanimoto similarity coefficient. For instance, the BitBound algorithm [2] and the modulo-M BitBound algorithm [3] were developed for high-performance cheminformatics fingerprint computation on the CPU. GPUSimilarity [4] provides the modulo-OR-compression (folding) algorithm implementation for the database compression on GPU.

Due to extremely low latency, high energy efficiency, and flexible programmability for easy prototyping, FPGAs have received much attention as an alternative accelerating solution for various data analytics applications [5]–[10]. However, there are few reports about the acceleration of molecular similarity search using FPGAs; in particular, the hardware-algorithm co-design exploration on FPGAs remains unknown.

In this work, to efficiently explore the FPGA design space, we propose an analytical design scheme. We design and optimize the representative algorithm in exhaustive search (BitBound & folding algorithm) and approximate search (HNSW), respectively. The overall of our design flow is shown in Fig. 1. Our proposed method outperforms existing approaches for two reasons. Firstly, work [11] separates the distance calculation and the top-k sort operation, leading to high memory bandwidth consumption and low throughput. Second, the work [12] utilizes a parallel priority queue for the top-k search, but the scaling of k size will degrade the kernel frequency and lead to extensive resource usage. While we leverage the fine-grained data movement scheme to reduce the pipeline interval and uses top-k merge sort and top-k priority queue for the sorting. Our proposed design has a much higher kernel throughput and better scalability for the similarity search application.

Our contributions are summarized as follows:

- We propose and optimize FPGA-based accelerator de-

![Fig. 1: Overview of FPGA-based Molecular Similarity Search.](image-url)
On exhaustive search using BitBound & folding, we propose a scalable on-the-fly query engine on FPGAs to reduce the resource utilization and pipeline interval, and achieve a 450 million compounds/s processing throughput for a single query engine. For Chembl database, our accelerator has 1638 QPS throughput for brute-force search and 25403 QPS throughput for BitBound & folding design with 0.97 recall.

We propose an FPGA-based graph traversal engine for HNSW approximate search. We explore the relationship between the returned element size, adjacent list size, and processing throughput and develop a Pareto frontier. The proposed FPGA-based HNSW implementation has a 103385 QPS with 0.92 recall on Chembl database and achieves a 35x speedup than CPU on average.

To the best of our knowledge, our FPGA-based implementation has the highest performance among existing approaches on molecular similarity search.

II. BACKGROUND AND RELATED WORKS

A. Jaccard/Tanimoto similarity

There are ECFP, Morgan circular [13], and MACCS structural keys [14] fingerprints to measure molecular similarity. In this study, we adopt the 1024-bit Morgan binary fingerprint [15]. For two given binary molecular fingerprints, \( \vec{A} = (a_1, a_2 \ldots a_{1024}) \) and \( \vec{B} = (b_1, b_2 \ldots b_{1024}) \) \((a_i, b_i \in \{0, 1\})\), their Jaccard/Tanimoto similarity [16] is the division of their intersection and union number of 1s (denoted using \( \sum \)):

\[
S(\vec{A}, \vec{B}) = \frac{\sum (\vec{A} \cap \vec{B})}{\sum (\vec{A} \cup \vec{B})}
\]  

B. Existing Works

There are several existing frameworks for KNN search in image or document similarity search. Faiss [17], [18] is a popular dense vector KNN search framework for HNSW implementations on CPU and GPU platforms. NMSLib [19], [20] is focused on providing support for distance measures in non-metric spaces. FALCONN [21], [22] utilizes locality-sensitive hashing for approximate distance calculations.

For the molecule similarity search application, Chemfp [2] and FPSim2 [3] implement the modulo-M BitBound algorithm, offering a tight bound on similarity score between a query and the database. A benchmark [23] is conducted for existing similar search algorithms implementation on Intel Xeon E5-2690 CPU platform. The benchmark on the Chembl database shows exhaustive search algorithms, such as brute-force and BitBound algorithms, have throughputs of 23 QPS and 46 QPS; the approximate search algorithms, such as HNSW and folding algorithms, have 950 QPS and 121 QPS throughputs while the recall is 0.9. GPUsimilarity [4] provides a GPU implementation of brute-force chemical similarity search and has a throughput of 570 QPS on chembl database.

III. INDEXING ALGORITHMS

In this section, we will first discuss the algorithm selection process and criteria for molecular similarity search on the FPGA. Secondly, we will provide a detailed analysis of the presented Bitbound & Folding and HNSW algorithms.

A. Algorithm selection

The molecule similarity search normally requires algorithms to have a high accuracy rate. BitBound [24] algorithm provides an \( O(\alpha^{0.6}) \) speedup by reducing the search space and is an exhaustive similarity search algorithm. For the large fingerprint database, a compression scheme is needed. The modulo-OR-compression (folding) algorithm is the most commonly used algorithm in molecule similarity search [3], [25]. Those algorithms are combined as BitBound & folding algorithm.

Besides the above algorithm, the HNSW index algorithm performs excellently in recall and query speed [23], [26] and is used for the approximate KNN search. The HNSW constructs a hierarchical graph index for approximate nearest neighbor search with poly-logarithmic construction complexity and logarithmic search complexity. Since the HNSW algorithm was introduced in 2016, it has been one of the fastest high precision approximate nearest neighbors techniques. The high recall of the HNSW algorithm is because it constructs a relative neighborhood graph, which has a heuristic algorithm for neighbor selection. The heuristic keeps a long-range link to help prevent a search from getting stuck in local optima.

B. Analysis of BitBound and Folding Algorithms

This section uses the Chembl 27.1 database [27] with 1.9 million molecules for the analysis. The RDKit toolbox is used for fingerprint generation. The accuracy (recall) is defined as the Top-K search matching rate between the proposed and brute-force algorithms.

The BitBound algorithm record the number of bits for each database fingerprint and query fingerprint and use the similarity cutoff \((S_c)\) and bound inequality to reduce the search space. For query compound fingerprint \(\vec{A}_i\), only the database query \(\vec{B}_j\) which satisfies the following inequation is searched:

\[
\text{Cnt}(\vec{A}_i) \cdot S_c \leq \text{Cnt}(\vec{B}_i) \leq \text{Cnt}(\vec{A}_i)/S_c
\]  

The bit count probability distribution of the Chembl database is modeled as Gaussian distribution \(x \sim N(\mu, \sigma^2):\)

\[
f_x(x) = \frac{1}{\sqrt{2\pi\sigma^2}}e^{-\frac{(x-\mu)^2}{2\sigma^2}}
\]  

Variables \(x\), \(\mu\), and \(\sigma\) represent the fingerprint bit count, the average bit count, and the standard deviation. The pruned search space for similarity cutoff \(S_c = 0.3\) and \(S_c = 0.8\) comparisons are given in Fig. [25] and Fig. [26]. The final speedup vs. similarity cutoff relationship is given in Fig. [24]. The actual speedup increase with the increase of the similarity cutoff.

There are two types of folding schemes. Assuming the fingerprint length is \(L\) and the folding level is \(m\). The first scheme conducts the bitwise OR between \(L/m\) section, and the second scheme conducts the bitwise OR between \(L/m\) section, and the bitwise OR between \(L/m\) section. The second scheme has a high accuracy rate. BitBound [24] algorithm provides an \( O(\alpha^{0.6}) \) speedup by reducing the search space and is an exhaustive similarity search algorithm. For the large fingerprint database, a compression scheme is needed. The modulo-OR-compression (folding) algorithm is the most commonly used algorithm in molecule similarity search [3], [25]. Those algorithms are combined as BitBound & folding algorithm.
Fig. 3: 2 compression schemes example (L = 8, m = 2).

second scheme conducts the bitwise OR between every nearby m bits. An example is shown in Fig. 3. A 2-stage folding algorithm [4] is used to retain the accuracy. The first search is conducted on the compressed database, and the top k_r1 results are returned. The second search is conducted on returned indices from the first round and the uncompressed database, and k elements are returned. The relationship between k_r1, k, and m can be expressed as k_r1 = k \cdot \text{mlog}_2(2m). The final accuracy test results of Top-20 search can be found in Table 1 and compression scheme 1 has higher accuracy than compression scheme 2. Thus the compression scheme 1 is used.

TABLE I: Accuracy vs. folding level (m)

| m  | Folding 1 accuracy (%) | Folding 2 accuracy (%) | mlog_2(2m) |
|----|------------------------|------------------------|------------|
| 1  | 100                    | 100                    | 1          |
| 2  | 99.3                   | 91.5                   | 4          |
| 4  | 99.1                   | 92.1                   | 12         |
| 8  | 97.3                   | 89.2                   | 32         |
| 16 | 84.4                   | 76.2                   | 80         |
| 32 | 31.7                   | 31.1                   | 192        |

C. Analysis of HNSW Algorithm

The HNSW uses two tuning parameters to control the quality of the constructed index: returned elements count E_f adjacency list size and M. A larger value E_f may help the search escape local optima by requiring the search to select a compulsory E_f element into a candidate list. A greater value of M will give higher recall but will be required up to 2M distance calculations per iteration in the graph traversal, which will affect the overall throughput of search. The Hnswlib implementation also provides a parallel construction algorithm that allows for multiple elements to be inserted into the graph simultaneously. Due to memory bandwidth limitations and the need for parallel guards, the parallel construction algorithm achieves logarithmic scaling. KNN search can be performed on the constructed graph index. Search can use the E_f parameter similarly to construction to control the batch quality at the cost of longer search times. However, a high-quality graph index, a graph built with higher E_f, may provide sufficiently high recall in search with E_f < E_fconstruction.

IV. Optimizing Indexing Algorithms on FPGA

This section will demonstrate the proposed FPGA designs to optimize the indexing algorithms for molecule similarity search. We target two categories of indexing algorithms and select one typical algorithm for each category: (1) the combination of BitBound and Folding Algorithm (denoted as BitBound & folding) [24], which can support the exhaustive search; and (2) Hierarchical Navigable Small World (HNSW) [26], which is a representative of approximate search. Kindly note that the proposed FPGA design can be easily extended to other algorithms in the same category.

A. FPGA design to support exhaustive search

Figure 4 demonstrates the overview of the FPGA design for the exhaustive similarity search algorithm. The full design can be divided into two sub-systems: (1) the communication sub-system and (2) the computation sub-system. Unlike the existing design applying the sequential process between two sub-systems [29], we propose the design to enable the computation and communication to be conducted in a pipelined fashion for the similarity search, which is called “on-the-fly” design in this paper. We adopt the FPGA boards with high bandwidth memory (HBM) to resolve the communication bottleneck in this work. For the computation sub-system, we develop three components to support the indexing algorithm: 0 Bit Count module, denoted as BitCnt, 0 Tanimoto Factor Calculation module, denoted as TFC, and 0 Top-K module.
Fig. 5: FPGA design of indexing algorithm for the approximate similarity search based on the HNSW algorithm.

1. **BitCnt**: The BitCnt kernel counts the number of bits for the input binary fingerprint. The resource utilization of the BitCnt kernel will scale linearly with the binary fingerprint length.

2. **TFC**: The Tanimoto factor calculation (TFC) module calculates the similarity score between query and database. In order to reduce the computation and storage overhead without loss of accuracy, the Tanimoto score information is stored as 12 bits fixed-point. According to Eq. 1, the Tanimoto factor calculation includes 2 bit count accumulation kernels and 1 fixed-point division operation.

3. **Top-K merge**: The top-k merge is built with FIFO and comparator. Unlike the existing top-K module, which is typically based on the parallel priority queue [12], our proposed top-k is based on the merge sort structure. As such, we can fully utilize HBM for fast memory access. In addition, we can achieve higher throughput and low resource utilization with the scaling of the k size (observation 2).

   The Top-K sorter utilizes $\log_2 K + 1$ comparators and $\log_2 K + 2K$ FIFO capacity. The small size FIFO can be built upon the register, and the large size FIFO can be built BRAM block. The pipeline interval is tuned as 1 for high throughput, and the entire implementation has a latency of $N + \log_2 K$ with $N$ input sequence size. The resource utilization roughly scales in a $O(log(k))$ size. For all different k values, the critical path has been tuned to achieve a 450 MHz clock frequency.

   **Put it all together**: The computing Engine in Fig. 4 shows how these components work together. Specifically, the fingerprint fetch, TFC kernel, and top-k merge sort kernel are cascaded to achieve an on-the-fly data movement structure. With the fine-grained TFC and top-k merge sort kernel design, the overall implementation achieves a pipeline interval as 1 for the cascaded structure. In order to achieve a high query speed, the HBM is utilized for the data movement. The top-k search kernel can run at a high frequency (450MHz) and consumes 57.6 GB/s memory bandwidth in our implementation.

**B. FPGA design to approximate search**

We adopt a similar FPGA architecture in the design of the accelerator for the approximate molecule similarity search.

Figure 5 demonstrates our proposed design. In such a design, we adopt the proposed TFC module in Figure 4 and proposed Priority Queue (PQ) module, which will be the basic component to support the computing engine. On top of this, we further propose two modules to support the HNSW algorithm: Search-Layer-Top module and Search-Layer-Base module.

4. **PQ**: Instead of merge sort, the priority queue is another method to support the Top-k operation. Our design philosophy is to achieve a high throughput design without frequency degradation. In consequence, we employ the register array structure to implement the priority queue. The compare and swap operation is done between even and odd entries for each clock cycle, and the kernel operation achieves a pipeline interval as 1 for both enqueue and dequeue operation. Thus, the throughput of the hardware priority queue is as high as clock frequency. The number of comparators scales linearly with the size of the priority queue. Thus the register array design is not favored when the priority queue size is large.

Assuming the entry size of the top-k priority queue is a 12 bit fixed-point number, the resource utilization with a different scale of k can be obtained. The resource utilization of the top-k priority queue is bounded most heavily by the LUT. The FF and LUT utilization scales linearly with the size of k.

5. **Search-Layer-Top module**: HNSW graph construction is based on the randomly shuffled database with index, and then the graph adjacent lists information will be used for the HNSW search step. The constructed HNSW comprises multiple layers, and each layer will have its own set of adjacency lists. During the HNSW graph search, the graph traverse Algorithm 1 will traversal all the layers except the base layer.

**Algorithm 1 SEARCH-LAYER-TOP(q_r, e_p, l_i)**

**Input**: query fingerprint $q_r$, entry point fingerprint $e_p$, layer number $l_i$

**Output**: Closest neighbor to query top

1. $C = ep$ // Candidate element
2. $C_n = q_p$ // Next candidate element
3. while $C \neq C_n$
4. $C = C_n$
5. for each $e$ in neighbourhood($C$) at layer $l_i$
6. $//$ distance function utilizes TFC kernel
7. if distance($C, q_r$) > distance($e, q_r$)
8. $C_n = e$
9. end if
10. end for
11. end while
12. $top = C$
13. return $top$

6. **Search-Layer-Base module**: The graph traversal Algorithm 2 will be conducted on the base layer, and top Ef results will be returned. The final results will be obtained from the top-k result of the Ef returned results using a simple top-k search.

**Put it all together**: The FPGA hardware design of the HNSW index algorithm can be found in Fig. 5 Algorithm 2 utilizes 2 register arrays based priority queue, and both of the
Algorithm 2 SEARCH-LAYER-BASE($q_r$, $e_p$, $e_f$)

Input: query fingerprint $q_r$, entry point fingerprint $e_p$, number of returned elements $e_f$
Output: $e_f$ nearest neighbors to query

1: $v ← e_p$ // $v$: visited elements set
2: $C ← e_p$ // $C$: candidates set
3: $M ← e_p$ // $M$: returned elements set
4: // $M$ and $C$ are built upon hardware priority queue
5: while size($C$) > 0 do
6:  $top ←$ get and pop closest element between $C$ and $q_r$
7:  $fur ←$ get furthest element between $M$ and $q_r$
8:  if distance($top$, $q_r$) < distance($fur$, $q_r$) then
9:     // distance function utilizes TFC kernel
10:     break // no further traversal is required
11: end if
12: for each $e ∈$ neighbourhood($top$) do
13:  if $e ∉ v$ then
14:       $v ← v ∪ e$
15:       $f ←$ get furthest element between $M$ and $q_r$
16:       if distance($e$, $q_r$) < distance($f$, $q_r$) or size($M$) < $e_f$ then
17:           // distance function utilizes TFC kernel
18:           $C ← C ∪ e$
19:           $M ← M ∪ e$
20:       if size($W$) > $e_f$ then
21:             pop furthest element between $M$ and $q_r$
22:       end if
23: end if
24: end for
25: end while
26: return $M$.

Priority queues are sized as $e_f$. Both algorithm 1 and algorithm 2 utilize only a single TFC kernel.

V. EXPERIMENTAL AND DESIGN EXPLORATION

In this section, the experiment setup is firstly introduced. Then, we report the results on the design exploration and cross-platform comparison. Results will show that our optimized FPGA accelerator can achieve a $35×$ speedup over the existing acceleration on the general-purpose computing platform.

A. Experimental Setup

The Chembl 27.1 database [27] with 1.9 million molecules is used for the similarity search. The RDkit toolbox [15] is used for binary fingerprint generation.

The FPGA designs are implemented in Vivado HLS v2020.1. The FPGA hardware platform is the Alveo U280 board. Alveo U280 board is equipped with 8 GB HBM, and its maximum memory bandwidth is 460 GB/s. The memory bandwidth for linear memory access has been limited to under 410 GB/s to provide suitable overhead. Alveo U280 on-chip resource includes 960 URAM blocks, 4032 BRAM blocks, 9024 DSP48E, 2.6M FF, and 1.3M LUT. With the abundant HBM memory bandwidth and on-chip resources, more kernels can improve overall throughput. Thus, design space exploration is needed to reveal the trade-off between different design parameters.

B. FPGA Design Exploration and Cross-work Comparison

1) FPGA Design Exploration: The brute force similarity search kernel consumes around 0.4% of the total LUT resource. The memory bandwidth requirement for a single brute force search kernel is 57.6 GB/s, and 7 kernels can be used to accelerate the single query request. The memory bandwidth bounds the maximum throughput for the brute-force similarity search. Each kernel runs at 450 MHz frequency, and the entire FPGA-based query engine achieves a 1638 QPS throughput.

For the BitBound & folding algorithm, the resource utilization of a single kernel can be extracted from the Vivado HLS toolbox. The resource utilization (Bounded by LUT & BRAM) vs. folding level can be found in Fig. 6a. With the increase of the folding level, resource utilization firstly decreases and then increases. The later increase in resource utilization is due to the growing size of the merge sort circuit. The memory consumption can be found in Fig. 6b. The memory consumption decreases with the increase of the folding level.

![Resource utilization and memory bandwidth requirement for the BitBound & folding algorithm.](image)

Fig. 6: Resource utilization and memory bandwidth requirement for the BitBound & folding algorithm.

The search space reduction of the BitBound algorithm can be found in Fig. 2. Thus, the BitBound & folding algorithm throughput on the FPGA platform can be found in Fig. 7. With the increase of the folding level, the query speed increases.

![QPS for BitBound & folding algorithm on FPGA.](image)

Fig. 7: QPS for BitBound & folding algorithm on FPGA.

The LUT resources majorly dominate the resource usage of the HNSW query engine. With the increase of the number of returned elements $e_f$, the LUT resource usage increases. The input parameter $m$ for HNSW is the maximum size of the adjacent list within the upper layers of the graph. The base layer of the graph provides every element up to $2M$ adjacency list elements, of which a minimum of $M$ adjacency list items are filled after a vertex is inserted. Both of the parameters above, $e_f$ and $m$, will affect the throughput of the query engine. A design exploration study is conducted based
on different $e_f$ and $m$ parameters. The QPS vs. $m$ and $e_f$ can be found in Fig. 8. The design exploration reveals that the query speed increases with the decrease of both $m$ and $e_f$ design parameters.

![Fig. 8: QPS for HNSW algorithm.](image)

2) Algorithms Performance on FPGA Platform: To reveal the true performance of the HNSW algorithm on the FPGA platform, a grid search for $e_f$ and $m$ is conducted. The $m$ is set to be 5, 10, 20, ..., 50, and $e_f$ is set to be 20, 40, 60 ..., 200. For all of the hyperparameter combinations, the QPS and recall are recorded. The design space exploration is conducted, and the QPS vs. recall for different hyper-parameters is shown in Fig. 9.

![Fig. 9: Design exploration for HNSW algorithm.](image)

As shown in Fig. 10, the Pareto frontier is generated based on the design exploration of the above algorithms. The similarity cutoff of BitBound & folding algorithms is set at 0.8. While the recall is high, the QPS for BitBound & folding algorithm is better. With a lower recall requirement, the HNSW algorithm has a much better performance.

![Fig. 10: Pareto frontiers of different algorithms on FPGA.](image)

C. Cross-platform Comparison

The CPU implementation in this section is based on Intel Xeon Gold 6244 CPU platform, and GPU implementation in this section is based on two NVIDIA Tesla V100.

The CPU implementation of brute force, BitBound & folding, and HNSW algorithms can be found in [23]. We utilize the code and method to run on our platform. The same as the FPGA implementation, the design exploration is conducted on the CPU platform. The GPU implementation of the brute-force similarity search method [4] is also included. The fingerprint database is loaded into the main memory for both implementations, and the search will be conducted.

The Pareto frontier obtained from the design space exploration is shown in Fig. 11. The GPU platform outperforms the CPU platform on the brute force search algorithm. However, the CPU platform achieves similar performance to the GPU platform without much recall degradation when the BitBound & compression algorithm is implemented. When the recall requirement is lower, the HNSW algorithm on the CPU platform has a much higher throughput than the BitBound & folding compression algorithm.

![Fig. 11: Pareto frontier for different CPU/GPU platforms.](image)

Comparing the FPGA platform implementation (Fig. 10) and CPU/GPU platform implementation (Fig. 11), we find out the FPGA implementation achieves more than 25× speedup on brute force algorithm over CPU platform and more than 3× speedup than the GPU platform. For the BitBound & folding compression index algorithm, the FPGA implementation achieves an average 30× speedup than the CPU platform. For the HNSW index algorithm, the FPGA implementation achieves an average 35× speedup than the CPU platform.

VI. Conclusion

The paper proposes the design and exploration for the different molecule similarity search algorithms on FPGAs. We design and optimize the two representative works in exhaustive search, BitBound & Folding algorithms and approximate search, HNSW, respectively. More specifically, on BitBound & folding, we analyze the similarity cutoff and folding level relationship with search speedup/accuracy and propose a scalable on-the-fly query engine on FPGAs to reduce the resource utilization and pipeline interval. On approximate search using HNSW, we propose an FPGA-based graph traversal engine to utilize high throughput register array based priority queue and fine-grained distance calculation engine to increase the processing capability. We further explore the relationship between the returned element size, adjacent list size, and the processing throughput and develop a Pareto frontier based on the design space exploration. Experimental results show that our FPGA-based implementation, to the best of our knowledge, is the first attempt to accelerate molecular similarity search on FPGA and achieves the highest performance among existing works.
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