10 orders of magnitude current measurement digitisers for the CERN beam loss systems

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ABSTRACT: A wide range current digitizer card is needed for the acquisition module of the beam loss monitoring systems in the CERN Injector Complex. The fully differential frequency converter allows measuring positive and negative input currents with a resolution of 31 nA in an integration window of 2 \( \mu \text{s} \). Increasing the integration window, the dynamic range covers \( 10^{10} \) were the upper part of the range is converted by measuring directly the voltage drop on a resistor. The key elements of this design are the fully differential integrator and the switches operated by an FPGA. The circuit is designed to avoid any dead time in the acquisition and reliability and failsafe operational considerations are main design goals. The circuit will be discussed in detail and lab and field measurements will be shown.

KEYWORDS: Analogue electronic circuits; Control and monitor systems online; Front-end electronics for detector readout; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases)

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1 Introduction

A current digitizer card capable of fulfilling a wide range of requirements is needed for the upgrade of the Beam Loss Monitoring systems in the CERN Injector complex, which includes: LINAC4, the Proton Synchrotron Booster (PSB), the Proton Synchrotron (PS) and their various transfer lines. The system should provide the possibility to connect several detector types with positive or negative input current polarity. The system will be used as monitoring and protection system, necessitating a high reliability design. However, as the electronics will be placed in protected areas, no radiation tolerance is required. Table 1 gives a summary of the main specifications for the acquisition system’s design.

1.1 Implementation

To reach such a high dynamic range of $2 \times 10^{10}$, a mixed measurement technique has been implemented in a new card (BLEDP). This combination of measurement techniques is done by two separate circuits referred hereafter as the Fully Differential Frequency Converter (FDFC), and the Direct ADC (DADC). The measurement range is split into two overlapping ranges: the FDFC is used in the range 10 pA–10 mA and the DADC in the range 100 µA–200 mA.

The front-end automatically switches between the two modes depending on the input current value. The control of the measurement techniques as well as the collection and transmission of the data for further processing is realised with the use of a Field Programmable Gate Array (FPGA) device.
Table 1. Acquisition system’s main specifications.

| Specification                                      | Value          |
|----------------------------------------------------|----------------|
| Measurement range (> 6ms integration time)         | 10 pA to 200 mA |
| Error                                              | $< \pm 10\%$  |
| Minimum integration period                         | 2 $\mu$s       |
| Input range with minimum acquisition period        | 31 nA to 200 mA |

Figure 1. A — FDFC block diagram. B — Integrator analogue output and comparator signal.

The DADC activation and de-activation thresholds can be set by the FPGA. The required time to switch between FDFC and DADC is less than 100 ns so in the minimum acquisition period of 2 $\mu$s it is possible to follow the input signal switching adequately.

The passage between the two ranges is managed by the FPGA. When the FPGA observes a signal above the DADC activation threshold, it switches the circuit to the DADC acquisition. When the value of the DADC returns a signal below the de-activation threshold, the FPGA switches the circuit to the FDFC acquisition.

2 FDFC & DADC functionality

2.1 Fully Differential Frequency Converter — FDFC

The FDFC circuitry is based on a fully differential integrator as shown in figure 1. A status signal is used to select in which branch of the fully differential stage the input current is integrated. Two comparators are used to check the differential output voltage against a threshold. Whenever the limit is exceeded, the status signal toggles to the complementary value (from 0 to 1 or from 1 to 0) and the input current is integrated in the other branch.

All electrical characteristics needed to create the FDFC circuitry will be explained in detail in section 3.1.

2.2 Direct Acquisition Digital Converter — DADC

The DADC is implemented by splitting the 50 $\Omega$ input resistor in two resistors: $47 \Omega + 3 \Omega$, as shown in figure 2. The 3 $\Omega$ resistor is used as a shunt and the current input flowing-in is measured directly by the A/D converter. In order to use the same components, the same ADC used for the FDFC is routed directly on the 3 $\Omega$ resistor through analogue switches.
2.3 Electronics architecture

As shown in figure 3 which represents the block diagram of the Input Monitor interface, the input current flows into the Fully Differential Frequency Converter (FDFC), passing an input filter, and a switch (1), and limited by clamping diodes. The FDFC is composed by: an input multiple-switch, a double polarity integrator, two analogue comparators, and a NOR gate.

The pulses generated by the FDFC are acquired by an FPGA, as described in section 2.1. At the same time the Integrator analogue signal is acquired by the FPGA, through a switch (2), a buffer amplifier and a 10 Msp, 16-bit ADC. A digital combination of the information coming from pulses and analogue signal allows a high resolution acquisition.

When the DADC configuration is activated, the switch (1) connects the output of the input filter to the ground. The switch (2) reconnects the ADC acquisition on the input resistor, using it...
as a shunt. At this time, the FDFC is completely disconnected and reset. The voltage drop on the 3 ohm shunt is acquired as measurement of the input current.

A digital potentiometer is managed by the FPGA to set the analogue comparator threshold, in order to calibrate the interface. Another digital potentiometer channel is used to inject a constant offset current, used to compensate the current leakage of the entire system (cabling + backplane + components leakage) and verify the functionality of the acquisition channel.

If a pulse exceeding the safety range of the FDFC is applied to the input, a hardware protection circuit called “Saturation Monitor” automatically switches from FDFC to the DADC, clamping the current peak to the ground. The FPGA receives a feedback from the Saturation Monitor which allows it to act several recovery strategies.

The BLEDP card has 8 channels where the power is supplied in group of 4 from different failsafe circuit breakers in order to guarantee the continuity of the main functionality in case of failure. Each function of the card is checked by self-diagnosis, and the result is treated as safety critical function or as monitoring function.

3 Electrical schematics

3.1 Schematic

In order to achieve a resolution of 10 pA, the implementation of the analogue circuitry has required special attention to current leakage effects.

For this reason the Fully Differential Integrator has been implemented using a fully differential amplifier filtered and buffered by High-Z input Operational amplifiers.

To globally increase the input impedance of the circuit, without losing speed and precision, two OPA659 have been used as input buffers with gain of 2.

Figure 4 shows main blocks needed to create the Fully Differential Frequency Converter.

The main guideline for the circuit implementation was the use of fast components with high impedance and low leakage current.

Main mandatory characteristics for each block are the following:

a) Input Switches — Ultralow on-resistance (< 1Ω); Fast operation (TON and TOFF < 20 ns) Low distortion.

b) Buffers: Low Input Bias Current (< ±10 pA); High Bandwidth (> 300 MHz); High Slew Rate (> 2500 V/µs).

c) Fully Differential Amplifier: Ultrafast Settling time to 0.01% (< 10 ns); High Bandwidth (> 300 MHz); High Slew Rate (> 2500 V/µs); Power supply rejection (±PSRR); Low Distortion.

All selected components have high speed characteristics in order to reduce the Commutation Delay error, which affects the analogue range of the FDFC.

The Commutation Delay error is the sum of all commutation delays, which are introduced by: the NAND, the flip-flop and the Input Switch. In addition the Input Switch and the Fully
Differential Amplifier have a settling time. The commutation delay to switch the input from one side to the other side of the integrator affects the output integrator analogue range.

For example a simple delay of 14 ns can introduce a voltage error of 29 mV which corresponds to 229 bits. Figure 5 shows a representation of the Commutation Delay error.

3.2 Simulation model

A mixed technique simulation has been implemented matching the functionality of PSPICE and MATLAB. The main reason for this approach has been to validate the analogue circuitry and to test the Data Merger algorithm used to match ADC measurement and digital pulses, which is implemented in the FPGA. The FDFC is based on commercial of the shelf components for which PSPICE models are made available by their manufacturers. The PSPICE model for the entire FDFC
A circuit was created combining the PSPICE models of the individual commercial components. The high matching accuracy between simulation model and the real circuit has been verified. Figure 6 shows the summary of the Simulation Model results.

3.3 PCB implementation

A special attention has been dedicated to the layout implementation, because the low leakage design requires high insulation between input lines and other signals e.g. power supplies.

This has been done creating special VIAs with increased distance between inner layers and the metalized holes, routing optimized paths, and creating holes below the integration capacitor. To guarantee low noise design, several ground areas have been created. Figure 7 shows an example of layout solutions.

Figure 6. Simulation model.

Figure 7. Extract from BLEDP Layout showing key solutions realised for improving the leakage current of the module.
4 Performance verification

Performance of the entire Acquisition System has been verified through several laboratories tests and a dedicated installation in the PS accelerator as summarised in the following sections.

4.1 Laboratories tests

Several tests have been executed to simulate the installation conditions. In order to show the system performance, some examples are reported below.

1) Acquisition of a 12 pC signal corresponding to the loss of 2.5E+11 Protons [5].

This test has been done setting the Integration Time=1.2 s, because it is the minimum duration of the signal required for the CERN Booster Accelerator.

A dedicated setup, composed by a Hewlett Packard 33120A function generator and several high attenuation resistances, has been used to inject pulses with several widths and amplitudes.

In that way, various losses during different machine cycles have been simulated, always maintaining 12 pC as injected charge.

During these tests campaign, one setup has been particularly important, because a pulse of 6 μA amplitude and 2 μs width has been injected in the BLEDP card, when it collects 600000 samples in 1.2 s. That 2 μs pulse has been correctly acquired also if it was averaged by all the other samples. Figure 8 shows the summary of the test results.
2) Verification of the operation area of the acquisition card located in the crate, with several settings for the integration time.

This test has been executed with the same setup described above, but changing several amplitudes and integration times, in order to verify the entire operation area of the BLEDP. In particular, using an integration time of 1.2 s it has been possible to measure a signal of 1 pA. Figure 9 shows the verification of the Acquisition Crate Operation Area.

3) Crosstalk test between acquisition channels. The execution of these tests required to inject in one channel of the BLEDP sinusoidal waves, square waves (at several frequencies), and fast pulses, leaving the other channels unconnected. Then the 2 \( \mu \text{s} \) samples collected by the BLEDP card have been treated in MATLAB to make a FFT analysis.

The worst case crosstalk is 130 dB at 10 kHz with a square wave signal injection. In figure 10 it is possible to see the result of the crosstalk performance when several current frequencies are injected (on the top side), or the crosstalk performance converting the injected current at certain frequency in loss Protons per time (on the bottom side).

4.2 Test installation in the PS accelerator

The acquisition channels have been tested acquiring several monitors e.g. Ionization Chambers, Secondary Emission Monitors, Diamond Detectors, PEP.
Figure 10. Crosstalk tests.

Figure 11 shows an example of Ionization Chamber signal acquisition by means of the Graphic User Interface. In particular the top window shows the measurement summary obtained averaging $510^5$ samples in one second. This plot represents an overview of the Accelerator activity during a machine cycle.

In the lower window of the same figure it is shown the zoomed in acquisition of the ionization chamber signal with a resolution of 2 $\mu$s.

As conclusion, the BLEDP performance is fully compatible with CERN specification.

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Figure 11. Ionization Chamber acquisition with Test Software Interface.

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