A Graph-based Model for GPU Caching Problems

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1. INTRODUCTION

A GPU is a massively parallel computational accelerator that is equipped with hundreds or thousands of cores. A single GPU can provide more than 4 Teraflops single precision performance at its peak, however, the maximum memory throughput of a GPU card is around 200 GB/s. Such a gap usually prevents GPU’s computation power from being fully harnessed.

A cache is a layer in between GPU’s computation units and memory units, which is a fast but (relatively) small storage for frequently accessed data. The modern GPUs are equipped with cache to improve program performance [27], [28], [30]. The throughput of the first level cache on GPUs is close to the throughput of computation unit and thus effective use of cache is critical to performance. While regular applications can take advantage of cache by classical transformations such as loop tiling and pipelining, instruction scheduling and etc, it is not so straightforward how irregular applications can best utilize cache.

In this paper, we look at irregular GPU applications and focus on improving shared cache performance. A GPU consists of a set of streaming multiple processors (SMs or SXMxs). Every SM has a fast shared cache. Threads that run on a SM can maximize data sharing in cache and minimize communication to off-chip memory. We show an example of how threads can be effectively scheduled to minimize off-chip memory communication in Figure 1.

We use the computation fluid dynamics (CFD) application [9] [8] as an example (Figure 1). In cfd, the main computation is to calculate interaction between two adjacent particles and apply the interaction information to obtain the state of the particles in the next time step. Figure 1 shows the interaction among six particles as a graph on the left. Each node in the graph represents a particle. Each edge represents an interaction, which is taken care of by one thread. Figure 1(a) shows one way to schedule the threads, with interactions e1,e2,e3 mapped to one SM, requiring 9 loads from the memory (assuming one load is for every distinct particle). In this case, three particles need to be fetched twice from memory. However, the thread schedule in figure 1(b) indicates that, with e1,e2,e4 mapped into one SM, only one particle needs to be fetched from memory twice, and the particle that is shared by e1, e2, e4 only needs to be fetched into cache once. All together the second case requires 7 loads from memory. According to our study, for all three inputs of CFD from the Rodinia benchmark suite [6], an average of 73.4% of all particle loads are redundant under the default task scheduling. This example demonstrates that there is a great potential to improve data sharing through careful task scheduling.

The graph-based model is used and extensively studied in the past [13] [15] for irregular application on parallel CPU processors, due to its efficiency in capturing the relationship between data and computation. In this paper, we also used a graph-based model to tackle the shared cache problem for irregular GPU applications.

The GPU shared cache problem brings several new challenges which cannot be handled well by previous graph-based methods. First of all, the expected task partitioning algorithm must have low time overhead, due to the high computation throughput of GPU. This constraint makes complex schemes like hypergraph partitioning [15] infeasible. Secondly, we expect high partition equality in terms of task schedule (partitioning), since up to thousands of concurrent threads share only a few KB of cache space, making random or greedy partitioning methods (e.g., techniques in PowerGraph [13]) impractical. Thirdly, the task partition results should be highly balanced because of the GPU’s single instruction multiple thread (SIMT) execution model, in which every thread executes the same code but on different input. The execution time of a parallel program depends
on the execution time of the longest task. Imbalanced task schedule may cause significant slowdown. This is different from CPU processors, which can typically tolerate a relatively higher degree of imbalance because of limited amount of parallelism.

To address the above problems, we propose to use an edge-centric graph-based model and we propose a fast task partition algorithm for the edge-centric model. Our partition algorithms have low overhead compared with vertex-centric model and yet provides high quality balanced partition results. Our contributions can be summarized as follows:

- This is the first edge-centric model for GPU cache performance. It overcomes the problems of traditional vertex-centric model and captures communication volume accurately.
- We propose a task partition algorithm for the edge-centric model. Our algorithm gives the best approximation bound we know so far.
- Our task partition algorithm is fast, often of orders of magnitude faster than previous hypergraph model and other edge-centric partition algorithm.
- Our algorithm is robust. It provides steady performance improvement regardless of the type of cache that is used: software cache or hardware cache, and regardless of the thread block sizes (work group size).

The rest of the paper is organized as follows. Section 2 describes the background of this paper. Section 3 introduces our task partition model and algorithm. Section 4 describes how to apply our model in GPU programs. Section 5 shows our experimental environment and evaluation results. Section 6 discusses the related work, and Section 7 concludes the paper.

2. BACKGROUND

We first describe the abstract memory model for a GPU architecture. As mentioned earlier, a GPU is composed of a number of streaming multiprocessors (SMs or SMXs). There is a cache on every SM, and threads running on the same SM share this cache. For a GPU program, the minimal unit of threads that run on one SM is called a thread block, also called cooperative thread arrays (CTAs) using NVIDIA CUDA terminology. The GPU threads are divided into blocks of the same size. One thread block can run at most on one SM at one time. Multiple thread blocks can run simultaneously on one SM. A thread block would acquire one SM and hold the SM until all its threads are finished. As one thread block releases the SM, another thread block (if there is any) will acquire the SM. As such, a thread block is also the minimal thread work group that share cache. We show the abstract cache sharing model in Figure 2. Every thread block uses a partition of the cache on one SM and would release it when the thread block is finished. Therefore, there are as if as many virtual cache as the number of thread blocks.

There are two types of caches on the SM: software cache and hardware cache. Software cache is scratch-pad memory, which is also referred to as shared memory in NVIDIA CUDA terminology. Software cache requires explicit load/store instructions to move frequently used data from/into memory. Every thread block gets an exclusive and even partition of shared memory. Similarly, the acquired partition of the software cache will not be released until the owner thread block finishes. A thread block cannot see another thread block’s software cache (shared memory) partition.

Hardware caches can be further classified into several categories based on their usage. In recent GPU architectures, the L1 cache is only used to store local variables that are private to each thread [25, 30]. The texture cache can store shared data objects after the data objects are binded with texture memory. Thus we use texture cache as the hardware cache to evaluate our task schedule/partition algorithms. The hardware cache does not require software to explicitly load frequently used data into cache, and has good programmability. However, it may not always keep the right data in cache since it does not have as much knowledge about the program as the programmer. Therefore, there is the trade-off between programmability and performance. We show the comparison between software cache and hardware cache in the evaluation section.

Finally, there is a L2 cache which is shared by all SMs on a GPU. A L2 cache has a typical hit latency of hundreds of cycles (close to memory access latency on GPU). Because of its long latency and also because it is unified across all SMs like the main memory, we only focus on optimization of the first level cache on every SM.

3. EDGE-CENTRIC MODEL

3.1 Problem Definition

We build an edge-centric graph model to describe the relationship between data objects and tasks. In our model, we describe a data object as a vertex and a task as an edge.

DEFINITION 1. We define a data-affinity graph \( D = (V, E) \) with the set of vertices \( V \) and the set of edges \( E \subset V \times V \).

Let \( n \) and \( m \) denote the number of vertices and the number of edges, respectively. A vertex \( v \in V \) represents a data object. An edge \( e \in E \) with \( e = (v, v) \) denotes a computation task that uses the two data objects \( u \) and \( v \).

Here every data object has the same attribute and size. The definition of a data object typically depends on the semantics of the program. One task could correspond to one or a group of operations in the program based on the semantics. For instance, cfd calculates the interaction of two particles based on their density, energy, and momentum variation. We group these three attributes of one particle into one data object. Thus one task is defined as the calculation based on these two aggregate data objects corresponding to this pair of particles.

Our goal is to partition all \( m \) edges in the data-affinity graph evenly into \( k \) clusters, such that every edge (task) is assigned to exactly one cluster (thread block). In short, this
is a balanced edge partitioning (EP) problem. The optimization objective is to maximize data reuse, which is equivalent to minimizing the number of times a vertex (data object) appears in different clusters (thread blocks).

**Definition 2.** A vertex $v$ is cut if its incident edges belong to more than one cluster. We define $c_v$ as the cost that $v$ is cut, which is the number of unique clusters that $v$’s incident edges belong to $p_v$, subtracted by $1$, $c_v = p_v - 1$. We define a total vertex-cut cost $C$ which has to be minimized under the condition of edge balancing. Let $C = \sum_{v \in V}(p_v - 1)$ and let $L_i$ denote the number of edges in cluster $i$, the $k$-way balanced edge partition (EP) problem is defined as:

$$
\begin{align*}
\min \ C(x) = \sum_{v \in V}(p_v - 1) \\
\text{s.t.} \forall i \in [1...k] \quad L_i(x) = \frac{x}{k} \\
x \text{ is a valid edge partitioning}
\end{align*}
$$

We use the same cfld example from Section 1 to illustrate the edge partition model. Figure 3(a) shows an example of the data affinity graph for cfld. In this example, there are 6 interactions to be computed. Assume a two-way balanced edge partition, i.e., $k=2$. The total vertex cut cost of the partition in Figure 3(e) is one, since one vertex (data object) appears in two edge clusters.

The number of times the data objects appear in different edge partitions represents how often a data object is loaded into different thread blocks. In the ideal case, each data object appears in only one partition. In such scenarios, threads sharing data all reside in one thread block, and thus there is no redundant data access. Each time one data object is shared by another thread block, one extra redundant data access is required. Therefore, the total vertex cut cost $C(x) = \sum_{v \in V}(p_v - 1)$ represents the number of redundant data accesses. We also refer to it as the data reuse cost, which we use to evaluate the quality of partitioning.

## 3.2 Problem Transformation

It can be easily proved that the problem of balanced edge partitioning in Definition 2 is NP-complete by reduction from existing NP-hard partition problems. For lack of space, we omit the proof here.

The edge partition problem is a non-traditional graph partition problem, and it lacks sophisticated solutions. On the other hand, there is a rich exploration on both a theoretical foundation and practical solutions for the vertex partition problem. We will show that we can convert the proposed balanced edge partition problem into the balanced vertex partition problem to leverage sophisticated vertex partition algorithms for efficient edge partitioning. As far as we know, our work is the first to map a balanced edge partition problem into a balanced vertex partition problem. We will prove that, not only does our solution work fast in practice, but also guarantees a polynomial algorithm with an worst case approximation factor of $(d_{\text{max}} - 1)O(\sqrt{\log m \log k})$, which is the best bound we know by far.

To convert the edge partition problem to a vertex partition problem, we first transform the data-affinity graph. We replace every vertex in the graph with a set of new cloned vertices such that every cloned vertex is connected to one unique incident edge of the original vertex. The cloning process is shown in Figure 3(b). Next, assuming the degree of the original vertex is $d$, we add $d-1$ auxiliary edges to connect the set of $d$ cloned vertices to form a path. This process of adding auxiliary edges is shown as an example in Figure 3(c).

Formally,

**Definition 3.** We define a graph transformation as a clone-and-bridge transformation if it satisfies following conditions. Assume $t$ is a legal clone-and-bridge transformation and $D \xrightarrow{t} D'$, where $D = (V, E)$ and $D' = (V', E')$. The transformed graph $D'$ needs to maintain the following characteristics. For every vertex $v \in V$ of degree $d$, there are $d$ corresponding cloned vertices $v'_1, \ldots, v'_d \in V'$. For every edge $e \in E$ with endpoints $u, v \in V$, there is a corresponding edge $e' \in E'$ with endpoints $u', v' \in V'$ such that $u'$ is the $i$-th cloned vertex of $u$, $v'$ is the $j$-th cloned vertex of $v$, and no cloned vertex is connected to more than one original edge. For every original vertex $v$ of degree $d$, its cloned set of vertices $v_i, i = 1 \ldots d$ in $D'$ are connected into a path using $d-1$ auxiliary edges, where a path is defined as a tree that contains only vertices of degree 2 and 1.

By Definition 3, a cloned vertex is connected to exactly one original edge, and no two original edges share a cloned vertex as shown in Figure 3(b). Therefore, we can get the total number of cloned vertices by doubling the total number of original edges. If we evenly partition the vertices in the converted graph into $k$ clusters and make sure no original edge is cut, we can ensure the two endpoints of any original edge belong to the same partition, and thereby we can determine the corresponding original edge belongs to that partition, too. In the meantime, we ensure that the number $d_{\text{max}}^2$ is the maximum vertex degree in the data-affinity graph.
of original edges is balanced across all partitions, since every partition has the same number of vertices. Formally,

**Definition 4.** Assume a clone-and-connect transformation $t$ transforms graph $D = (V, E)$ to $D' = (V', E')$, $D \xrightarrow{t} D'$, we perform vertex partition on $D'$ and obtain a vertex partition solution $VP_{D'}$ such that no original edge is cut. From $VP_{D'}$, we can reconstruct an edge partition solution of $D$, $EP_D$. We define a reconstruction process $m$ such that $VP_{D'} \xrightarrow{m} EP_D$ as follows. For every original edge $e \in E'$ with $e = (u', v')$ in $D'$, assume both $u'$ and $v'$ fall into the $i$-th partition; then its corresponding edge $e \in D$, falls into the $i$-th partition as well.

As shown in Figure 3(d), the edges $A, B, C$ are in the same cluster since their endpoints are all in the partition on the left. Using this approach, we can map the vertex partition back to the edge partition by checking every edge on which partition its endpoints fall into (shown in Figure 3(e)).

To ensure no original edge is cut in the vertex partition, we assign a very large weight to all original edges in the converted graph so that the vertex partition process will only cut auxiliary edges. Also note that in the conversion process described in Definition 3 there are several different ways to connect cloned vertices to form a path. We choose to connect them in index order in practice. Any other way to connect cloned vertices is fine, since auxiliary edges are used to represent data sharing relationship between original edges (tasks).

The balance degree of $D'$’s edge partition is equal to that of $D$’s vertex partition. We find that existing vertex partition algorithms can produce rather balanced results. The balance factor is used to measure the balance degree of partition, which is calculated by dividing maximum partition size by average partition size. It is typically less than 1.03 in practice.

We will show the mapping relationship between the optimum vertex partition and the optimum edge partition with rigorous analytical results in Section 3.4.

### 3.3 Comparison with Other Methods

Figure 6 compares our proposed conversion based edge partition model (EP model) with other existing task partition methods. The experimental environment is introduced in Section 5.1. For the vertex partition of the converted problem in our EP model, we use METIS library. Five data-affinity graphs are constructed using representative input matrices selected from the Florida matrix collection and matrix market (note that a sparse matrix usually represents a graph in or is used in sparse matrix vector kernels). We show the degree distribution for the data-affinity graphs in Figure 4. We did not show the degree of the mc2depi data set, since its pattern is relatively simple, with degree 2 of 5.70532e-04% occurrence, degree 3 of 0.583654% occurrence, and degree 4 of 99.4158% occurrence.

The selected data-affinity have different degree distribution patterns. The degree of the cant data-affinity graph is between 0 and 40. The circuit5M has a more random degree distribution and we only show part of the x range for readability. The mc2depi data set has nodes of degree 2 to 4, resembling the meshes (at most 4 neighbour particles) in computation fluid dynamics. Two of the data sets exhibit the power-law pattern: the in2004 data set and the scircuit distribution. We further show the log–log scale for these two data sets in Figure 5. Regardless of the type of degree distribution, our algorithm always outperforms the classical vertex-centric algorithm.

**Comparison with hypergraph model [15].**

A hypergraph is a special type of graph where an edge may connect more than two vertices. Therefore an edge is also called a hyperedge. In the hypergraph task partition model, unlike our EP model, a vertex represents a task, and a hyperedge represents a data object where it covers all vertices (tasks) that share that data object. The goal of maximizing data sharing is equivalent to partitioning vertices (tasks) into $k$ clusters so that the number of times hyperedges are cut is minimized. Figure 7 shows an example to compare the hypergraph model with the EP model. We also show the optimum partition for both models. In Figure 7(a) one hyperedge is cut, which corresponds to the one cut vertex in Figure 7(b).

For the hypergraph partition, we use hMETIS, a multilevel hypergraph partition tool, and PaToH, the fastest hypergraph partition implementation we are aware of.

From Figure 8 we see that PaToH is faster than hMETIS in the hypergraph model, and our basic EP model is significantly faster than both of them in all cases. The partition quality, measured as the data reuse cost in Definition 2 shows that our EP model generates similar quality of partitions as PaToH and hMETIS. The quality of both the
hypergraph model and our EP model are better that of the default task scheduling shown in the “default quality” column, which indicates that data sharing within each thread block is improved significantly after partitioning. Overall, our basic EP model is faster than the fastest hypergraph partition model and yet produces high quality results.

Another important thing to notice is that our EP model scales better compared to the hypergraph model with respect to graph size. For small graphs such as scircuit, our EP model is about 4 times faster, while for large graphs such as circuit5M and in-2004, the EP model is tens of times faster.

**Comparison with other edge partition methods.**

PowerGraph proposes two edge partition based task scheduling methods. Both methods go through all edges linearly to distribute them among partitions. The random based method randomly assigns edges into partitions. The greedy based method prioritizes choosing partitions that already possess the endpoints of the to-be-assigned edge. If no such partition is found, then the partition with the fewest edges is selected to ensure balance. Figure 6 shows the partition quality of both methods. We do not show the partition time since both methods are expected to be fast. Compared with hypergraph and our EP models, both of them have significantly worse partition quality because of their random or greedy nature. In many cases, their quality is worse than that of the default scheduling. In such scenarios, rescheduling tasks only degrades the performance. Therefore, we conclude that these two partition methods are not applicable for complicated data sharing patterns exhibited in GPU programs.

**3.4 Approximation Bounds**

Our EP model is not only good in practice, but also strong in theory. We provide the proof for approximation factor between $O(\sqrt{\log m \log k})$ and $(d_{max} - 1)O(\sqrt{\log m \log k})$. We describe it in two steps.

**Theorem 1.** With the clone-and-connect transformation $t$ such that $D \xrightarrow{t} D'$ where $D = (V, E)$ and $D' = (V', E')$, the edge cut cost of the vertex partition of $D'$ is greater than or equal to the vertex cut cost (in Equation 7) of the corresponding edge partition of $D$, $C_{ep}(D') \geq C_{ep}(D)$.

First recall that in Section 3.2, we have ensured in the vertex partition of $D'$ that only auxiliary edges are cut. For every set of cloned vertices $v'_i, i = 1, d$ in $D'$ that corresponds to the vertex $v$ of degree $d$ in $D$, they are connected with $d - 1$ auxiliary edges to form a path. If $l$ out of the $d - 1$ auxiliary edges are cut, the total number of distinct edge clusters $v$ fall into in $D$, is at most $l + 1$. Therefore, the cut cost of $v$ in the edge partition of $D$ is at most $l$. When converting the vertex partition of $D'$ into the edge partition of $D$, we sum up the total vertex cut cost and thus the total number of auxiliary edges cut in $D'$ is greater than or equal to the vertex cut cost in $D$.

**Theorem 2.** There exists a clone-and-connect transformation $t, D \xrightarrow{t} D'$ such that the edge cut cost of the optimal vertex partition of $D'$ is the same as the vertex cut cost of the optimal edge partition of $D$. For all legal clone-and-connect transformations $t \in T$, in the worst case, the edge cut cost of the optimal vertex partition of $D'$ is $d_{max} - 1$ times of the vertex cut cost of the optimal edge partition of $D$, while $d_{max}$ represents the maximum degree of the graph $D$.

The first task is to prove that there exists a clone-and-connect transformation $t$ such that the transformed vertex partition problem is the dual of the original edge partition problem. We construct such a transformation using an optimal edge partition $E_{opt}$ on the graph $D = (V, E)$. Using the optimal edge partition solution, we know which edges are grouped to the same partition. Then we determine the transformation $t$ as follows. First, the cloning process is the same as in Definition 3. In the connecting phase, for every set of cloned vertices $v'_i, i = 1, d$ that connect to every original edge, we first divide each set into $k$ groups with respect to which partition their incident original edges belong to. Within every set of cloned vertices, within every group, we connect the cloned vertices to form a path, then we connect all $k$ groups into one path. Such a transformation $t$ is constructed. It is easy to see that if we reverse this path connecting process, we can obtain a balanced vertex partition of $D'$ that can be mapped to the optimum edge partition solution of $D$, which is $E_{opt}$ we defined earlier.

Since we do not a priori know the optimal edge partition of the original graph $D$, when connecting the cloned vertices into a path, we connect them arbitrarily. Assuming the converted graph with a priori knowledge of optimal partition of $D$ is $D'_{opt}$, the second task is to prove that with an arbitrary connecting process, the edge cut cost of the optimum vertex partition of the converted graph $D'$ is at most $d_{max} - 1$ times the edge cut cost of the vertex partition of $D_{opt}$ since $D_{opt}$ maps directly back to $D_{opt}$ ($D_{opt}$ is the optimal edge partition of the original problem). This step is easy to prove as well, since for every set of $d$ cloned vertices that correspond to the cut vertex in the optimal edge partition solution of $D$, at most all auxiliary edges are cut ($d - 1$ cuts) and in the best case, at least one auxiliary edge is cut, the edge cut cost in the vertex partition of $D'$ is thus at most $d_{max} - 1$ the edge cut cost in the vertex partition of $D'_{opt}$. According to Theorem 1 in the reconstructed edge partition of $D$ from the vertex partition of $D'$, the vertex cut cost of $D$ is less than or equal to the edge cut cost of $D'$, $C_{ep}(D) \leq C_{ep}(D')$. Thus the reconstructed edge partition...
solution from the optimum vertex partition of \( D' \) is at most \( d_{max} - 1 \) times the optimum solution of edge partition of \( D \).

The vertex partition problem can be approximated with a factor of \( O(\sqrt{\log n \log k}) \) for a graph with \( n \) vertices and \( k \) partitions \cite{23}. Therefore we can approximate our solution by a factor of \( (d_{max} - 1)O(\sqrt{\log m \log k}) \) since our converted graph has \( 2m \) vertices where \( m \) is the number of edges in the original graph.

![Code transformation example](image)

Figure 8: Example of code transformation.

4. PROGRAM TRANSFORMATION

In this section, we will introduce how to apply the partition result of our EP model to GPU programs for data sharing optimization. Figure 8 shows an example of original and transformed code that enables data sharing optimization.

For the host function on the CPU side in Figure 8(b), it first spawns a separate CPU thread to perform data sharing optimization. The optimization process will be introduced in Section 4.1. We use a separate thread for optimization to prevent it from adversely affecting the performance of the main program. Assume the GPU kernel is called multiple times. Before every kernel call, we check if the optimization process has been completed. If so, the optimized kernel will be called with the optimized input. Otherwise, the original kernel is called as usual. The details of how we control optimization overhead, as well as the situation when the GPU kernel is only called once, will be discussed in Section 4.2.

If the target cache for data sharing optimization is texture cache, the host function binds the optimized data layout to texture memory using the CUDA built-in function `cudaBindTexture()`. The GPU kernel prefixes every data reference using `text1Dfetch()` as shown in Figure 8(c) so that referenced data will be cached automatically by texture cache.

If the target cache is software cache, the kernel function on the GPU side in Figure 8(d) requires three major modifications in order to leverage optimized input. First, an array local_arrayA is created in software cache to store shared data. Then, each thread block loads its shared parts from the input array (opt_arrayA) into the local_arrayA. To minimize memory divergence \cite{34, 33}, memory accesses are coalesced into as few contiguous memory segments as possible. At last, we replace the reference of the original input array with that of the local array which resides in software cache.

4.1 Optimization Process

Figure 9 illustrates the working process of data sharing optimization. The data access pattern of a GPU program is determined by both program semantics and input data. Therefore, we extract the data access pattern to build the data-affinity graph at first.

![Optimization workflow](image)

Figure 9: Optimization workflow.

After data-affinity graph is built, we examine the graph before actually partitioning it using EP model. First, we check if there is enough data reuse by checking the degree frequency of the data-affinity graph. If there is little data reuse, then we omit the partition process and use the original input. Secondly, we check if the graph follows a special pattern such as clique, path, complete bipartite, etc. For these special graphs, we have a preset optimal partitioning schedule using the EP model offline, and thus we use the preset partition pattern.

If we determine that task partitioning/reschedule is necessary for the generated data-affinity graph, we apply the EP algorithm to perform task partitioning as described in Section 3.

At last, we reorganize tasks among thread blocks based on the partition result and we reorganize data layout as well. We use the cpack algorithm \cite{12} to perform data layout transformation based on our task schedule. After the data layout is transformed (from arrayA to opt_arrayA in Figure 8), the data references need to be updated as well and the new index array (opt_indexA in Figure 8) is passed to the optimized kernel.

4.2 Adaptive Overhead Control

To reduce overhead at runtime, we perform data sharing optimization using a separate thread on the CPU while kernel is executed on the GPU, so that the optimization process can run asynchronously. We utilize a CPU-GPU pipelining technique to overlap computation and optimization for GPU programs \cite{34, 33}.

In real GPU programs, a kernel is usually called within a loop, especially in scientific computation programs. In such scenarios, We check if the asynchronous optimization is completed before calling the kernel and apply the optimization so if. If the optimization thread does not complete when the program finishes, we terminate it to guarantee no slowdown.

If a kernel is only called once, we perform kernel splitting \cite{34} which breaks one execution of a kernel into multiple executions of the same kernel with a smaller number of threads. Then we can apply the asynchronous optimization method.
It is, however, possible that the transformed kernel runs slower than the original kernel. To prevent such cases from degrading performance, we record the transformed kernel runtime the first time it runs, and compare it with the original kernel runtime. If the first run of the transformed kernel is slower, then we fall back to the original kernel in the next iteration.

5. EVALUATION

5.1 Experiment Setup

Our hardware platform is a machine with an NVIDIA GeForce GTX680 GPU with CUDA computing capability 3.0. It includes 8 streaming multiprocessors (SMs) with 192 cores on each of them and 1536 cores in total. On each SM there is 64 KB of L1 cache and shared memory (i.e., software cache), shared by its 192 cores. There are three size configurations of L1 cache and shared memory: 16KB/48KB, 32KB/32KB and 48KB/16KB. Since L1 cache in GTX680 is allowed for local memory data only, we always configure shared memory to be 48KB. There is also 48KB texture cache per SM. The CPU is Intel Core i7-4790 at 3.6 GHz with 8MB last-level cache.

We use seven applications from various domains including data mining, computation biology, object tracking, scientific simulation, and graph traversal. This set of benchmarks are representative of important contemporary workloads that can benefit from cache locality enhancement. The benchmarks are listed in Table 1.

Six applications are from the Rodinia benchmark suite [6]. We also evaluate an important kernel, the sparse matrix vector multiplication (SPMV) kernel, which is widely used in different types of applications including machine learning and numerical analysis. The SPMV kernel is also frequently used for evaluating graph partition models on parallel CPUs [21, 22]. We report the performance of SPMV kernel and the task scheduling overhead. We also evaluate the asynchronous optimization method. We run the SPMV kernel in the context of the conjugate gradient (CG) [10] application. The CG application calls SPMV iteratively until the solution converges. All benchmarks are compiled on a system that runs 64-bit Linux with kernel version 3.1.10 and CUDA 5.5.

We use the input sets bundled with the benchmark suite or real-world input sets. For example, the cfd benchmark from Rodinia benchmark suite [6] has three input meshes: fc-corr.domn.097K, fc-corr.domn.193K and missile.domn.0.2M. The sparse matrix inputs to CG come from the University of Florida sparse matrix collection [11] and market [9].

In the rest of this section, we first evaluate the performance of sparse matrix vector kernel over a large number of sparse matrices and various configurations. Then we show the evaluation results of the six applications from Rodinia.

5.2 Sparse Matrix Workloads

Conjugate gradient (CG) method [17] is an important algorithm for solving linear systems, whose matrices are usually large and sparse. The conjugate gradient method is an iterative process that repeated invokes sparse matrix vector multiplication until the result converges. We focus on the total amount of time for sparse matrix vector multiplication in CG in the following discussion.

We partition the sparse matrix workload with our edge partition model and hypergraph model to maximize data reuse and compare their performance with the popular SPMV implementation from CUSP [10] and CUSPARSE [29]. The CUSP spmV kernel orders the data layout such that all non-zero elements are sorted by row indices and then it distributes the non-zero elements evenly to threads. We are not aware of CUSPARSE’s task distribution scheme since it is not open source, however since it is faster than CUSP for most inputs, we include CUSPARSE for comparison.

In the data-affinity graph of SPMV, there is a vertex for every element in the input vector \( x \) and output vector \( y \). For each non-zero element \( A[i, j] \) in the input matrix \( A \), an edge is added to connect vertex \( j \) in the input vector and vertex \( i \) in the output vector, since a non-zero \( A[i, j] \) implies a multiplication with \( x_j \) to get \( y_i \). The data-affinity graph of SPMV is naturally a bipartite graph. With the data-affinity graph, we perform edge partition and let one thread block be mapped to one partition. We use software cache for the corresponding shared input and output vector elements within each thread block. We will also show the results of using texture cache later.

We use 8 matrices with different data access patterns to show the applicability of our EP model. These matrices are shown in Table 2. \( \text{Nnz} \) represents the total number of nonzero elements. \textit{CUSPARSE time} column shows total SPMV kernel execution time of CUSPARSE. \textit{EP time} and \textit{HP time} show the total kernel execution time of our EP model and hypergraph model respectively. \textit{EP partition} and \textit{HP partition} show their partition time. All times are measured in seconds.

In Table 2, we first observe similar kernel execution time for EP and HP models, which confirms our EP model can produce similar partition quality compared to hypergraph partition model. (Note that in Table 2 we show the partition time and kernel execution time without applying the asynchronous optimization method – the overhead control. We will show the results with overhead control later.) On the other hand, hypergraph partitioning incurs much larger partition overhead compared to our EP model. Its partition time occupies 205% of the total kernel time of CUSPARSE on average, which means the hypergraph partition model could not finish optimization for most matrices before program ends. On the other hand, the partition time of our EP model only occupies 22.7% of total time on average. Therefore, hypergraph partitioning is infeasible for GPU applications due to its large overhead. Other edge partition methods have been proved to have worse quality than the default scheduling in Figure 6. Thus we focus on
the study of our EP model in the rest of this paper.

Figure 10 compares the performance of four versions of SPMV kernel execution, including CUSPARSE, CUSP, our EP model that does not consider optimization overhead (EP-ideal), and the one that takes overhead into consideration (EP-adapt). We set the thread block size to be 1024. We use CUSPARSE kernel time as the baseline, since it is faster than CUSP for most matrices.

In Figure 10 we can see that CUSP is slower than CUSPARSE except in two cases, circuit5M and in-2004. However, our EP model based approach is faster than both of them except for cant, where the quality of default scheduling is similar to that of our EP model as shown in Figure 6. When using EP-adapt for cant, there is almost no slowdown for cant. That is because adaptive overhead control checks if optimization is beneficial and if not it would stop using the optimized kernel. EP model is slightly worse than CUSP for in-2004 because there is very limited data reuse, which causes EP model to use a large amount of software cache, adversely affecting occupancy. We also observe that in most cases, the performance of EP-adapt is similar to that of EP-ideal except for Ga41As41H72, where the partition time occupies most kernel execution time and we can only optimize a small portion of SPMV invocations.

Figure 11 shows the normalized memory transaction number for three spmv kernels. All results are normalized to that of CUSPARSE. We observe that memory transaction number is reduced significantly for all matrices except cant and Ga41As41H72. There is no memory traffic reduction for cant and Ga41As41H72 due to the same reasons we have explained above. Overall, the transaction reduction maps well to the performance results.

Software cache v.s. texture cache.

Here we study the performance difference when using software and texture caches to optimize the data sharing of input vector in SPMV. Since the output vector is write-shared, texture cache cannot be used to store it. Figure 12 compares their performance; EP-text represents the texture cache version and EP-smem represents the software cache (i.e., shared memory) version. Again, the baseline is the performance of CUSPARSE. Software cache version outperforms texture cache version for almost all matrices except in-2004, in which case the large shared memory usage of EP-smem degrades thread level parallelism significantly as stated above. Note that EP-text outperforms CUSP in Figure 10 where in-2004 is the only case our optimized kernel using software cache is not as good as CUSP. Compared to CUSP and CUSPARSE, EP-text also has better performance. In general, the texture cache based approach could potentially pollute cache by evicting data before it gets fully reused, while using software-managed cache does not have such a problem. On the other hand, using texture cache can reduce programming overhead since it requires less effort for program and data transformation, and there is still sufficient performance improvement. Thus there is a trade-off between programmability and performance. In practice, we can choose either version based on programmability and

Table 1: Benchmark summary.

| Benchmark | Application Domain | Input | Cache type |
|-----------|--------------------|-------|------------|
| b+trees   | Tree data structure| One-million size database query | Software |
| bfs       | Breadth first search| One-million node graph | Texture |
| cfd       | Computation fluid dynamics | 97K, 193K, and 0.2M node meshes | Software |
| gaussian  | Gaussian elimination | Linear system with 1024 unknown variables | Software |
| particlefilter | SMC for posterior density estimation | Tracking of 1000 particles | Software |
| streamcluster | Sparse matrix multiplication | 65,536 data points | Various size input matrices |

Table 2: Matrix Information.

| Name          | Dimension | Nnz | CUSPARSE time | EP time | EP partition | HP time | HP partition |
|---------------|-----------|-----|---------------|---------|--------------|---------|--------------|
| cant          | 62K*62K   | 2.0M| 2.53          | 2.89    | 1.702        | 2.92    | 11.66        |
| circuit5M     | 5.6M*5.6M | 59.5M|21599         | 783.2   | 67.157       | 784.2   | 2250         |
| cop20k_A      | 121K*121K | 1.4M| 25.93         | 20.17   | 1.457        | 19.99   | 5.76         |
| Ga41As41H72   | 268K*268K | 9.4M| 19.37         | 15.29   | 17.922       | 15.26   | 194.5        |
| in-2004       | 1.4M*1.4M | 16.9M|430.9         | 359.4   | 17.889       | 355.7   | 413.6        |
| mac2depi      | 207K*207K | 1.3M| 31.54         | 18.29   | 1.342        | 18.14   | 5.04         |
| mc2depi       | 526K*526K | 2.1M| 36.45         | 28.31   | 1.436        | 28.36   | 4.87         |
| scircuit      | 171K*171K | 0.96M|20.42         | 13.62   | 0.642        | 13.51   | 2.91         |

Figure 11: Normalized transaction number of spmv.

Figure 12: Texture cache v.s. software cache.
| Block size | 256 | 512 | 1024 |
|------------|-----|-----|------|
| cant       | 310 | 279 | 313  |
| circuit5M  | 8312| 7349| 8524 |
| cop20kA    | 208 | 186 | 211  |
| Ge41A*     | 1353| 1196| 1378 |
| in-2004    | 2471| 4472| 2492 |
| mac*       | 190 | 174 | 191.4|
| mc2depi    | 332 | 284 | 307  |
| circuit    | 143 | 130 | 144  |

Table 3: Performance on different thread block sizes.

Figure 14: Application performance summary.

Figure 15: Read transaction number.

performance preference.

**Thread block size.**

Finally, we show the sensitivity of our graph partition approach with respect to different thread block sizes. Table 3 shows the performance of our EP model without overhead control (EP-ideal) under different thread block sizes for both software and texture caches. At every thread block size, the performance difference between software and texture caches is similar to the observation we made earlier. The results suggest for all shared memory kernels, the performance at small thread block size is slightly better than (or the same as) that of the larger thread block size except in-2004, where shared memory version performs badly because of limited data sharing and low concurrency. However, smaller block size implies larger block number, and thus longer partition time of EP model. Taking both kernel performance and partition overhead into consideration, the performance using smaller block size is similar to that using large block size. Therefore, we still choose 1024 as the default block size in our experiments.

### 5.3 General Workloads

Figure 13 shows the performance of the six Rodinia applications under various thread block sizes. For every benchmark, we test performance using four thread block sizes, 128, 256, 384 and 512, unless the program does not allow such a thread block size. For instance, gaussian only allows square thread block sizes. The original runtime is denoted as original in Figure 13. The runtime of our EP model with overhead control is denoted as EP-adapt.

First, we can see that in most cases our optimized version outperforms the original version when the thread block size is fixed. The maximum speedup is 1.97 times for gaussian at the thread block size 256. For streamcluster, the maximum speedup 1.7% is for thread block size 1024, which is lower than that of other benchmarks. This is because streamcluster has less data sharing compared to other benchmarks at runtime. In streamcluster, every thread holds a unique data point, and a set of threads access the same center point to perform distance calculation, which makes the average degree of data-affinity graph to be $\leq 2$ (average data reuse).

Enlarging thread block size typically would enlarge the amount of sharing since more threads imply more data sharing opportunities. This is particularly true for cfd. The larger the thread block size is, the better performance it is for the EP model. However, it is not the case for all benchmarks. For instance, the best performance of EP-adapt is not achieved at the largest thread block size for particle-filter and b+tree. This is because the GPU performance is determined by many factors besides data sharing. Many of these factors change with the thread block size, such as occupancy, cache contention, etc. For instance, cfd suffers from performance degradation at a block size of 384 because 384 is non-integral power of 2, and thus it is impossible to achieve the best potential occupancy of 2048 threads.

In Figure 14, we show the comparison between the best EP-adapt version and the best original version in terms of performance across different thread block sizes. The data is normalized to the runtime of the best original version. Note that the execution time of EP-adapt version includes the optimization overhead. We have significant performance gains, or at least no performance degradation, for all benchmarks with adaptive overhead control.

Figure 15 shows the normalized off-chip read transaction number measured by CUDA profiler for this set of benchmarks. The reason why we do not show write transaction number is that there is no write sharing in these benchmarks. All results are normalized to that of the original version at the same thread block size. The results show that our technique can reduce off-chip memory transactions significantly, since more memory requests are satisfied by on-chip software or texture caches.

We also observed that using texture cache does not perform as well as software cache in most cases, which is similar to the observation for SPMV.

### 6. RELATED WORK

**CPU task partition for communication reduction.**

Some models have been proposed to model data communication in traditional CPU parallel systems, and these models are used to reduce communication among processors through task scheduling. Hendrickson et al. use vertex-partition based graph models where vertices represent tasks [10,15]. The vertex-partition model cannot measure data communication accurately, and thus we use edges to repre-
sent tasks instead. Hypergraph models can model communication cost accurately. The main drawback of the hypergraph model is its large overhead, as we demonstrate in Section 3.3 which makes it infeasible for GPU computing. Pregel and GraphLab introduce two parallel computation models based on message passing and shared memory, respectively. They always assign all computation of one vertex to one processor due to limitations of the programming model, while our model allows computation to be scheduled arbitrarily to achieve better partition quality and balance. PowerGraph can distribute the computation of one vertex into several processors and proposes two edge partition methods for task scheduling. One is to randomly assign edges, and the other, greedy based method assigns an edge to those partitions which already possess its endpoints. These simple edge partition schemes produce low-quality partitions and are thus inapplicable for GPU task partitioning, as demonstrated in Section 3.3.

Ding and Kennedy propose using runtime transformation for improving memory performance of irregular programs, but it is heuristics based and there is no rigorous model for data reuse. Bondhugula et al. introduce an automatic source-to-source transformation framework to optimize data locality, and they formulate data locality problem with polyhedral model, which only works for regular applications with affine memory indices.

**GPU task partition for divergence elimination.**

The dynamic task scheduling work for GPU memory performance optimization is mainly in memory coalescing rather than data sharing. Zhang et al. propose to dynamically reorganize data and thread layout to minimize irregular memory accesses. Wu et al. also propose two data reorganization algorithms to reduce irregular accesses. However, these papers do not address the data sharing problem in GPU caches.

**Other GPU software optimization techniques.**

Many compiler techniques are proposed to achieve better utilization of GPU memory. For affine loops, Baslaran et al. use a polyhedral compiler model to reduce non-coalesced memory accesses and bank conflicts in shared memory. Jia et al. propose to characterize data locality and then guide GPU caching. The limitation of these compiler methods is that they cannot address global data sharing among threads.

Some research uses hints provided by programmers to help compilers improve GPU memory performance. CUDA-lite tunes shared memory allocation via annotations. hiCUDA seeks to automate shared memory allocation with the help of programmer specified directives.

There are also application-specific studies for sparse matrix vector multiplication. Bell and Garland discuss data structures of SPMV for various sparse matrix formats. Choi et al. propose an automatic performance tuning framework for SPMV. Volkov and Demmel analyze the bottleneck in dense linear algebra and optimize its performance by improving on-chip memory utilization and etc. But none of this handles the fundamental task scheduling problem for SPMV locality enhancement. Nonetheless, these techniques are complementary to our technique. For instance, we can use auto-tuning to find out whether to use texture cache or software cache.

**7. CONCLUSION**

In this paper, we propose a task partition technique to improve data sharing among different GPU threads. We use data-affinity graphs to model data sharing and map task scheduling problem to an edge partition problem. This is the first time the edge-centric model is used for GPU cache performance modeling. We propose a novel partition algorithm based on the edge-centric model, and our algorithm provides high quality task schedule and yet is low-overhead. We also provide rigorous proof for the analytical bound of our algorithm. Our experiments show that our method can improve data sharing and thus performance significantly for various GPU applications.

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