Retraction

Retraction: Design and analysis of 32 bit high speed carry select adder (J. Phys.: Conf. Ser. 1916 012006)

Published 23 February 2022

This article (and all articles in the proceedings volume relating to the same conference) has been retracted by IOP Publishing following an extensive investigation in line with the COPE guidelines. This investigation has uncovered evidence of systematic manipulation of the publication process and considerable citation manipulation.

IOP Publishing respectfully requests that readers consider all work within this volume potentially unreliable, as the volume has not been through a credible peer review process.

IOP Publishing regrets that our usual quality checks did not identify these issues before publication, and have since put additional measures in place to try to prevent these issues from reoccurring. IOP Publishing wishes to credit anonymous whistleblowers and the Problematic Paper Screener [1] for bringing some of the above issues to our attention, prompting us to investigate further.

[1] Cabanac G, Labbé C and Magazinov A 2021 arXiv:2107.06751v1

Retraction published: 23 February 2022
Design and analysis of 32 bit high speed carry select adder

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Abstract. In the area of VLSI design, the focus is on reducing delays, power consumption and space, and improving speed. This paper presents the design of 32-bit modified-HSCSA using parallel prefix adder in which the basic design is based on Binary to Excess-1 Converter (BE1C) and also handouts brief review on traditional techniques used in standard BE1C, Brent-Kung (BK), Lander-Fischer (LF) and Kogge-Stone (KS). The performance of the presented 32 bit modified –CSA using parallel prefix adder is compared with traditional techniques and observed reduced delay. Verilog HDL is used to design the structure and the simulation and synthesis is carried out using Xilinx.

Keywords: High Speed Carry Select Adder(HSCSA), Binary to Excess-1 converter, Parallel Prefix Adder, verilog HDL, Xilinx

1. Introduction

The addition operation is the primary and important function in all arithmetic computation in digital systems. This operation is performed by a binary adder. In digital systems, binary adders are present in arithmetic and logical unit (ALU), dividers, multipliers and also the memory address generation perform summing operation. The performance of digital systems depends on the operating speed of the adder. The propagation delay is the significant challenge for the binary word addition. The length of the carries obtained will depends upon the width of the input data. In serial adder, delay is very high when compared to parallel adder.

A complex digital system design is depended on factors such as area, power and delay. Achieving a high speed adder is a challenging task. Processors performance of a system is decided by these digital systems’ speed [1].

One of the simplest adders is Ripple Carry Adder (RCA). A RCA consists of full adders in cascade. An n-bit RCA requires an n number of FAs to carry out addition of two n-bit numbers. In RCA lower bits carry propagates to next higher bits i.e. adders of present stage are dependent on the previous stage adder’s output. This increases delay to the adder circuit. Thus propagation delay (PD) is high in RCA. The performance of any circuit is improved by reducing the propagation delay of the circuit [2].

The PD is reduced in Carry Look Ahead (CLA) but in terms of increased area. It can also be obtained by using prefix adders. In prefix adders, the output depends upon every input. The combination of RCA and CLA is a prefix added. It incorporates the advantages of both adders i.e. RCA and CLA. Further this research article is arranged into various sections as the following: section
‘2’ is basic over view of conventional carry select adder and parallel prefix adder. Followed by section ‘3’-literature survey, section ‘4’- design methodology and section ‘5’ hand-outs the simulation results and finally conclusions are given in fifth section.

2. Overview of Traditional Carry Select Adder (TSLA) and Parallel Prefix Adder

2.1. Traditional carry select adder
TSLA is configured with a RCA which is dual as well as multiplexer. This architecture reduces PD but increased area. The dual RCA structure provides a couple of sums its and the output carry bits are the preceded input carry where $C_{in} = 0$ and $1$, the only one out of the two is selected for the final sum and also the final output carry [3]. TSLA within the input-operand bit-width is shown in figure 1. It consists of “sum and the carry generator unit (SCGu)” and the sum and “carry selection unit (SCSu)”. The SCGu consists, the dual RCAs and occupies the logical resource of TSLA and also contributes considerably critical path. Many logical designs are suggested by the researchers for an efficient implementation of the SCG unit. In literature, high-speed adders with different architectures are designed. Among these architectures, parallel-prefix adders (PPA) whose structure is a tree, have are faster computation time. By replacing dual RCA with PPA and BEJC results CLSA structure. This minimizes carry propagation throughout the adder structure [4].

![Figure 1. Traditional carry select adder (TSLA).](image)

2.2. Parallel Prefix Adder (PPA)
The flexible feature of a PPA results in high speed addition of binary numbers, thus are found in arithmetic circuits in industries where high speed operations are required [5]. The logical function of PPA determines if carry is generated, propagated or killed at each bit position [6].

The structure of PPA has three stages which are shown in figure 2, pre-processing is the first stage, carry generation is the second stage and final stage is post-processing stage.

![Figure 2. Parallel Prefix Adder(PPA) Structure.](image)
Stage One: This is pre-processing stage, propagates as well as generates signals (Pi and Gi respectively) computed for each pair of inputs A and B. The logic equations (1 and 2) represents these signals [7] (note the functional symbol & denotes AND, ^ denotes XOR).

\[ P_i = A_i \land B_i \]  
\[ G_i = A_i \land B_i \]  

Stage Two: In this carry generation network stage, carries which are equivalent to each of the bits are generated. This operation is executed in parallel. Once the carriers paralleled computed these are divided into smaller segments. Two intermediate signals carry propagate and carry generators are used represented by the logical equations (3 and 4) [8] (note the functional symbol & denotes AND, | denotes OR). Figure 3 demonstrates the operations involved in carry network.

\[ C_{P_{i:j}} = P_{i:k+1} \land P_{k:j} \]  
\[ C_{G_{i:j}} = G_{i:k+1} \lor (P_{i:k+1} \land G_{k:j}) \]  

Figure 3. Carry Network (CN).

Stage Three: This is the post processing stage, where the input bits are summed up and in found in all adders. The logic equations (5 and 6) represents these signals [9] (note the functional symbol & denotes AND, ^ denotes XOR, | denotes OR).

\[ C_{i-1} = (P_i \land C_{in}) \lor G_i \]  
\[ S_i = P_i \land C_{i-1} \]  

2.3. Binary to Excess-1 Converter (BE1C)
In conventional TSLA, one from two RCA is replaced by BE1C. The equation (7, 8, 9, 10) it contributes to achieve reduction in area and power, as BE1C has less number of logical gates than i the RCA structure. BE1C replaces RCA with C_{in}= 1 in the conventional TSLA. An n+1 bits BE1C is needed in place of n tuple-bit RCA [10]. 4 bits BE1C structures along with the functional table are illustrated in figure 4 and Table 1 respectively. The Boolean form of 4-bit BE1C are given below (note the functional symbol ~ NOT, & AND, ^ XOR).

\[ X_0 = \sim B_0 \]  
\[ X_1 = B_0 \lor B_1 \]  
\[ X_2 = (B_0 \lor B_1) \land B_2 \]  
\[ X_3 = (B_0 \lor B_1 \land B_2) \land B_3 \]
3. Literature Survey

In [11] a 16-bit CSA model is proposed using parallel prefix adder based on BE1C. The performance parameters of CSA was improved by modifying its structure. The RCA block positioning in the top was compensated by modified parallel prefix tree(MPPT) where RCA block positioning in the bottom was withheld. The Group-PG logic of parallel prefix tree(PPT) design were modified as shown in figure 5 to accelerate the speed and reduce the area consumed.

The author proposed an 8-bit linear Brent Kung CSA using BE1C. The proposed design uses BK adder design for first 4 bits, $C_{in}=0$ and the BE1C for $C_{in}=1$ and also a multiplexer which can select the sum-bits based on the carry-bits as shown in the figure 6. This has reduced delay and area.
The new design proposed by the author is Manchester carry chain (MCC) in multi-output domino-CMOS which has implemented 16-bit as well as 32-bit CSA. This approach resulted in increased speed and reduced PDP and hardware requirement. The proposed MCC blocks are utilized in building 32-bit CSA as shown in figure 7 consisting of two levels. The first level is implemented using six proposed MCC blocks having 4, 5, 5, 6, 6 and 6 as block size starting from the LSB to MSB and utilizes six bit MCC-block at level two. The design downside is the clock signal required pre-charging and evaluation at level 1 and 2 and two control clocks at level 1 for the transmission gates.

The author proposed new design with 8, 16, 32, 64 bit CSLA using SQRT, which has reduced area compared to typical SQRT TSLA shown in the figure 8. In this model delay increased by 3.76% and in 64-bit SQRT CSLA has reduced area by 17.4% and power by 15.4% compare to regular SQRT TSLA. Then 16 bit SQRT TSLA was modelled with BE1C replacing of RCA with the Cin=1. This approach resulted in the reduction of area and power.
4. Design Methodology

In a 16-bit modified CSA is designed. Referring the 16-bit CSA, a 32-bit modified-HSCSA using parallel prefix adder in which the basic design is based on Binary to Excess-1 Converter (BE1C) is designed and presented in this research paper. The designed HSCSA is illustrated in the figure 9. In the figure HSCSA, the final sum as well as the carry out (C_{out}) is obtained by taking the partial output of BE1C structure using MUX.

5. Simulation Result
The proposed design methodology for 32-bit Carry select adder circuit with BEC has been synthesized in XILINX program. The simulation results using Modelsim simulator are shown in the figure10 and figure11. Since the CSA is designed using parallel prefix tree, yielded a high performance. The proposed implementation of 32-bit CSA circuit results in 124.25% ADP. The result shows that the proposed method using BE1C, reduces the delay to 3.502ns. Table 2 shows a comparison of the simulation result for delay in CSA implementations.

Figure10. Simulation result of CLSA using BE1C using for delay.

Figure11. Simulation result of 32-bit Carry select adder.

Table 2. Comparison of existing CSLAS with proposed.

| Bit Size | Adder Scheme          | Technology | Area(μm²) | Power(μW) | Delay(ns) |
|----------|-----------------------|------------|-----------|-----------|-----------|
| 4-Bit    | Conventional CSLA     | CMOS       | 669       | 33.56     | 1.36      |
|          | BK-Carry Select Adder | CMOS       | 293       | 15.35     | 1.26      |
6. Conclusion
This paper has presented a design methodology for architecture of 32-bit HSCSA. The design is based on BE1C. Simulation results show that the BE1C based 32-bit HSCSA design has reduced number of gates, delay and area and enhanced speed. The high performance is achieved through parallel prefix tree. The proposed design provides an increase in flexibility due to decrease in area due to reduced number of gates. The future scope of the presented method can be extended to 64 bit and 128 bit.

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