Transient Process Optimization for Dual-Arm Cluster Tools With Wafer Revisiting

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ABSTRACT

In wafer fabrication, it is imperative to minimize the transient process of cluster tools for the sake of on-demand and preventive maintenance. Due to the trend of multi-type and small-batch production, transient processes appear more and more frequently. Thus, the optimization problems of transient processes have gained increasing attention from both industry and academia. The requirement for wafer revisiting tend to complicate this problem significantly. However, only a few studies take such a challenge for cluster tools with wafer revisiting. This paper focuses on the schedule optimization of transient processes for dual-arm cluster tools with wafer revisiting. To accelerate transient processes, including both start-up and close-down ones, we adopt a program evaluation and review technique to analyze and harness a cluster tool’s state evolution. We then propose computationally efficient algorithms to speed up transient processes. Finally, we provide illustrative examples to show their applications and validate their effectiveness.

INDEX TERMS

Cluster tool, semiconductor manufacturing, wafer fabrication, scheduling, transient process, wafer revisiting.

NOMENCLATURE

- $N_n = \{1, 2, \cdots, n\}$
- $N_i \setminus N_j$
- $N_i : N_m \cup \{0\}$
- PM Process module.
- SACT Single-arm cluster tool.
- DACT Dual-arm cluster tool.
- ALD Atomic layer deposition.
- WRP Wafer revisiting process.
- $k$-WRP $k$-time Wafer revisiting process.
- 1-WCS One-wafer cyclic scheduling.
- 3-WCS Three-wafer cyclic scheduling.
- VWM Virtual wafer method.
- SUTP Start-up transient process.
- CDTP Close-down transient process.
- PERT Program evaluation and review technique.
- $\Theta$ A state at which a PM or the robot is empty.
- $M$ The system state.
- $W_p(q)$ The $p$th wafer that is released to the system with its $q$th operation being processed, $p \in N_n, q \in N_{2k+1}, k \in N_5^1$.
- $R_b(W_p(q))$ The $p$th wafer is being held by the robot and will be delivered into process step $b$ for its $q$th operation, $b \in \Omega_3, p \in N_n, q \in N_{2k+1}, k \in N_5^1$.
- $\alpha$ Time taken for the robot to unload a wafer from the PM or loadlock.
- $\beta$ Time taken for the robot to load a wafer into the PM or loadlock.
- $\mu$ Time taken for the robot to move among two different modules.
- $\lambda$ Time taken for the robot to execute swapping operation at a process step.

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\[ \omega_{ij} \] Robot waiting time before its unloading operation at process step \( i \) during the transit from \( M_{j-1} \) to \( M_j \).

\( a_i \) Wafer processing time in \( PM_i \), \( i \in \mathbb{N}_3 \).

\( T_k \) Time taken from the idle state at Node 0 to the terminal state at Node \( k \) in the PERT model of the SUTP.

\( \Gamma_k \) Time taken from the initial state at Node 1 to the terminal state at Node \( k \) in the PERT model of the CDTP.

\( \phi_0 \) Time taken from the idle state to the first target steady state by the PERT-based method.

\( \phi_V \) Time taken from the idle state to the first target steady state by the VWM-based method.

\( \phi_{O} \) Time taken for completing the CDTP by the PERT-based method.

\( \phi_{V} \) Time taken for completing the CDTP by the VWM-based method.

I. INTRODUCTION

To achieve higher quality, productivity, and yield, cluster tools with the single-wafer processing technology are widely applied in numerous semiconductor wafer fabrication processes, such as etching, chemical vapor deposition, and rapid processing technology with high temperature. In particular, cluster tools occupy an essential place in large-size wafer fabrication. A cluster tool compactly integrates several process modules (PMs), input/output loadlocks, and a wafer-handling robot with a radial way and holds no intermediate buffer. After being loaded into a cluster tool through loadlocks, raw wafers are delivered into PMs for processing in sequence according to pre-specified order, and finally return to loadlocks when all necessary processes are completed. All these operations are dominated by the wafer-handling robot. The robot is equipped with one or two arms fixed in an opposite direction, leading to the single-arm cluster tool (SACT) and dual-arm cluster tool (DACT, see Fig. 1).

For instance, in the wafer fabrication process of low-pressure chemical vapor deposition, the completed wafer must be unloaded from the PM within a restricted time in case of its degradation. This temporal restriction is called the wafer residency time constraint (WRTC). Kim et al. [2] propose a systematic modeling, analysis, and scheduling method for the DACT with WRTCs. Lee and Park [3] derive necessary and sufficient conditions to verify the schedulability of the time-constrained DACT by using the negative event graph. Based on the resource-oriented Petri nets (ROPNs) model, Wu et al. [4], Wu and Zhou [5] present efficient algorithms to find the optimal steady state periodic schedule for the SACT and DACT with WRTCs, respectively. When the residency time is tight, there may not be a feasible schedule under conventional robot strategies. To deal with such a particular issue, Lim et al. [6] develop a novel robot strategy based on the interference-free sequence. Yang et al. [7] provide a general framework to find the optimal schedule for the time-constrained SACT within both process- and transport-bound regions. In order to reduce quality variability in wafer fabrication and guarantee high-quality output, Zhu et al. [9], [52] and Xiong et al. [10] propose efficient methodologies to regulate robot waiting times for reducing the wafer delay time in each process step.

Due to exceptional events, such as processing delay, communication delay, or wafer alignment failure, the activity time is practically subject to random variation [2]. The activity time variation (ATV) may make the wafer residency time delay in PMs exceed reasonable bounds such that the schedule obtained under the assumption of deterministic activity time become infeasible. Thus, it requires that the schedule for cluster tools should possess sufficient adaptiveness and robustness [11]–[15]. Kim and Lee [16] develop a necessary and sufficient condition for identifying the always schedulable case and never schedulable case. A graph-based computational procedure is presented to find the satisfied schedule if the system state belongs to the always schedulable case. However, the criterion concerning the never schedulable case is somehow conservative. Wu and Zhou [17]–[19] design a real-time control strategy to dynamically regulate the robot waiting time to maximally compensate the impact of activity time variations on the wafer residency time fluctuation in PMs. By using this strategy, some never schedulable cases identified in [16] are schedulable in fact. Besides, a real-time scheduling approach with two-level operational architecture is proposed, exhibiting its optimality in terms of productivity. Based on the idea of [17]–[19], Qiao et al. [20], [21] present efficient algorithms for scheduling the SACT with WRTCs and ATV. Nevertheless, the upper bound of wafer residency time delay provided in [20], [21] is overestimated, which may impede the schedulability test of some cases. Pan et al. [22] obtain the exact bound by several polynomial algorithms. With the unfixed conventional backward strategy, Yang et al. [23] provide an efficient method to calculate the upper bound of wafer residency time delay for the SACT with WRTCs and ATV. By the mixed-integer programming method,

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig1.png}
\caption{A dual-arm cluster tool with four PMs.}
\end{figure}
Lim et al. [24] present an adaptive scheduling approach to cluster tools with tight wafer residency time constraints and large processing time variations.

In the above discussion, we focus on the cluster tool with nonrevisiting processes, whereas there are still quite a few revisiting ones. For instance, the atomic layer deposition (ALD) is a typical wafer revisiting process (WRP) in semiconductor manufacturing [25]. Wafers in the ALD process require to visit some process steps multiple times such that the film thickness can be precisely controlled. Due to the wafer revisiting, PMs are shared by multiple operations, being prone to deadlocks, which further complicates the scheduling and control of cluster tools. Lee and Lee [26] investigate the scheduling problem of SACTs with WRP for the first time. They develop a mixed-integer programming model to find the deadlock-free optimal schedule. However, the presented method is computationally inefficient due to its exponential complexity. To cope with this issue, Wu et al. [27] adopt ROPNs to describe the ALD process. They propose a necessary and sufficient deadlock avoidance policy and analytical expression to calculate the optimal schedule. Further, Yang et al. [28] develop efficient algorithms to find the optimal scheduling of SACTs with WRP and WRCTs.

For the DACT with WRP, Wu et al. [29] find that the system presents three wafer cyclic process including three local and global cycles if the conventional swap strategy is applied. Based on the ROPN model, they obtain conditions to find the optimal 3-wafer cyclic schedule (3-WCS). Due to the delay at the revisiting process step in each switching operation from local to global cycle, the system may always be in the transient state, i.e., the lower bound of the systematic cycle time cannot be reached. By reducing the number of local and global cycles, Wu et al. [30] propose a 2-WCS method. Qiao et al. [31] extend the results in [29], [30] and propose a method to calculate the cycle time of the DACT with multiple revisiting times. As verified in [29]–[31], it remains inefficient that scheduling the DACT with ordinary swap strategy, especially the revisiting time $k > 2$ cases. To overcome this limitation, Qiao et al. [32] present a modified swap-based strategy and derive a 1-WCS. Based on the results in [29], [30], [32], Qiao et al. [33]–[36] propose efficient methods to find the optimal 1-WCS of DACTs under WRCTs and ATV, respectively.

It should be noted that the majority of studies mentioned above are devoted to the steady state scheduling. Nevertheless, as the wafer lot size contracts continuously, transient processes scheduling plays an increasingly important role due to new wafer fabrication requirements such as lot switching operations [37]–[39] and concurrent processing of multiple wafer types [40]–[44]. For the DACT, Kim et al. [45] prove that the latest/earliest starting policy can minimize its start-up/close-down transient process (SUTP and CDTP for short), respectively. Kim et al. [46] further present a max-plus algebra method to optimize the transient process of DACTs. Based on the ROPN model, Qiao et al. [47] and Zhu et al. [48] propose efficient algorithms to find the optimal schedule of SACTs with WRCTs during the SUTP and CDTP, respectively. Note that in [47], [48], each process step is configured with only one PM. Considering the SACT with parallel PMs, Kim et al. [49] develop a generalized backward strategy. Subsequently, Yang et al. [50] extend the results in [49] and present linear programs to search the optimal feasible schedule for the SACT with WRCTs and parallel PMs. For the SACT with a failure CDTP, Qiao et al. [51] propose efficient response policies. For the linear dual-arm multi-cluster tool subject to WRCTs, Zhu et al. [52] present efficient algorithms to find the optimal integrated schedule for the whole process covering the steady state and transient processes.

Although great efforts [45]–[52] concerning the transient process scheduling have been conducted, these studies are unfortunately focused on the nonrevisiting processes, i.e., inapplicable to the transient process with wafer revisiting. In our previous work [53], we propose efficient algorithms to optimize the SUTP of DACTs with WRP for two times. As for the optimization to more general cases, for instance, transient processes with wafer revisiting for multiple times, including both the SUTP and CDTP, there is no research reported on this problem yet. Thus, our major motivation is to tackle the transient optimization problem for DACTs with wafer revisiting. In this paper, we build an analysis framework based on the program evaluation and review technique to investigate the temporal properties of DACTs with WRP during transient processes. With the system network model, we present computationally efficient algorithms to find the optimized transient process schedule for DACTs under diverse wafer revisiting cases.

The subsequent sections are organized as follows. In Section II, we briefly introduce the ALD process and notations of corresponding activity representations and definitions. In Section III and IV, we analyze the SUTP and CDTP comprehensively and propose optimization algorithms to minimize transient processes, respectively. Section V provides case studies. Finally, Section VI concludes this paper.

II. PRELIMINARIES
A. ATOMIC LAYER DEPOSITION PROCESS

In semiconductor manufacturing, the raw wafer needs to undergo a number of process steps. In general, each process step demands a unique operation. If the wafer fabrication process necessitates the visit of the same process steps for more than one time, this is called revisiting process; otherwise, it is called nonrevisiting one. According to the manufacturing requirement, the revisiting process may contain only one process step or more than two process steps. In practice, the revisiting process with two process steps is widely applied in wafer fabrication. ALD is such a typical revisiting process that the film thickness can be controlled by repeating the deposition operation. Since the ALD with two revisiting steps is a typical wafer fabrication process that is commonly adopted in cluster tools, the results derived from the two-step revisiting process
are useful for the other cases. Therefore, for the sake of simplicity, this paper only consider the ALD with two-step revisiting process. In the ALD process, as shown in Fig. 3, there are generally three steps (i.e., Al₂O₃ deposition, TiO₂ deposition, and oxidation), and the last two of them are the revisiting process, which will be repeated several times, even more than five times [26]. Let \( m_i \) and \( k \) be the number of parallel PMs for process step \( i \) and the number of revisiting times, respectively. Then, the ALD process can be denoted as \((m_1, m_2, m_3)^k\), where \( m_i \) denotes the robot task time for unloading, loading, moving, and the swapping operation, respectively. Likewise, wafer \( i \) denotes the system resources’ activities, we use \( \alpha \)

\[ W_i = \{W_1(1), W_1(2), W_1(3), R_1(W_1(1))\} \]

and the swapping operation, respectively. Likewise, wafer \( i \) denotes the system states. After that, the ALD process can be denoted as \((m_1, m_2, m_3)^k\). For the sake of the consistency of wafer fabrication within the ALD process, each step normally is composed of a single PM, i.e., \( m_1 = m_2 = m_3 = 1 \). Thus, the wafer flow pattern of the ALD process can be denoted as \((PM_1, PM_2, PM_3)^k\) with \((PM_2, PM_3)^k\) being a \( k \)-time wafer revisiting process (\( k \)-WRP).

**B. DESCRIPTION OF SYSTEM STATE AND ACTIVITY**

Cluster tools are a type of highly automated manufacturing systems containing complex discrete state evolution and temporal properties. Let \( N_d = N_d = \{1, 2, \cdots, n\} \) and \( \Omega_n = \N_d \cup \{0\} \), where \( \N_d = \{1, 2, \cdots, n\} \). For the state description, we use \( W_p(q), p \in \N_d, q \in \N_{2k+1}, k \in \N_d \), to represent the \( p \)th wafer that is released to the system with its \( q \)th operation being processed, and \( R_p(W_p(q)) \) represents the \( p \)th wafer being held by the robot and will be delivered into process step \( b \) for its \( q \)th operation, where \( b \in \Omega_n, p \in \N_d, q \in \N_{2k+1}, \) and \( k \in \N_d \). In particular, process step 0 denotes the loadlock. Then, a state of the system can be denoted as \( M = \{S_1, S_2, S_3, S_4\} \), where \( S_d = W_p(q), d \in \N_d \) and \( S_4 = R_p(W_p(q)) \). For instance, \( M = \{W_3(1), W_2(2), W_2(3), R_1(W_2(1))\} \) represents that the first, second, and third wafers (i.e., \( W_1, W_2, \) and \( W_3 \)) are being processed in PM3, PM2, and PM1, respectively, whereas the fourth wafer is being held by the robot and will be delivered into PM1 for its first operation at process step 1. There is no doubt that the first operation must be executed in PM1, i.e., the robot is at PM1, preparing for swapping. Therefore, the definition of the system state results in no confusion or misunderstanding. As for the temporal aspects of the system resources’ activities, we use \( \alpha, \beta, \mu, \) and \( \lambda \) to denote the robot task time for unloading, loading, moving, and the swapping operation, respectively. Likewise, wafer processing time in PM\( i \) is indicated as \( a_{ij}, i \in \N_d \).

**C. CYCLIC SCHEDULING OF STEADY STATE**

The SUTP starts from the idle state \( \{\Theta, \Theta, \Theta, R_0(\Theta)\} \), where \( \Theta \) indicates that the PM or the robot arm is empty. The challenge lies in reaching the target state quickly as possible. The CDTP starts from the steady state under a given cyclic schedule. That is, the steady state schedule has a significant impact on both the SUTP and CDTP. Therefore, it is necessary to know the cyclic scheduling strategy under the steady state. For the DACT with 2-WRP, a 1-WCS method is proposed in [32]. As for the 3-WCS with \( k > 2 \), it remains unclear whether exist an unified 1-WCS. Instead, Qiao et al. [31] investigate this with the framework of 3-WCS.

According to the 1-WCS presented in [32] for DACTs with 2-WRP, in the steady state, the system starts from state \( M_1 = \{W_3(1), W_1(2), W_2(3), R_1(W_2(1))\} \) and then evolves as \( M_1 \rightarrow M_2 = \{W_4(1), W_1(4), W_2(3), R_3(W_2(3))\} \) to \( M_3 = \{W_4(1), W_3(2), W_3(2), R_2(W_4(2))\} \) to \( M_4 = \{W_4(1), W_2(1), W_1(5), R_2(W_4(2))\} \) to \( M_5 = \{W_4(1), W_2(4), W_3(3), R_2(W_3(3))\} \) to \( M_6 = \{W_4(1), W_2(4), W_3(3), R_3(W_5(3))\} \) to \( \cdots \) to \( M_{3k-1} = \{W_4(1), W_2(2k), W_1(2k + 1), R_2(W_4(2k + 1))\} \) to \( M_{3k} = \{W_4(1), W_3(2k), W_3(2k + 1), R_1(W_3(2k + 1))\} \) to \( M_{3k+1} = \{W_4(1), W_4(2), W_3(2k + 1), R_1(W_4(1))\} \) to \( M_{3k+2} = \{W_4(1), W_2(2), W_3(3), R_1(W_7(1))\} \) to \( M_{3k+3} = \{W_7(1), W_6(2), W_3(3), R_3(W_5(3))\} \). It is obvious that \( M_1 \) and \( M_{3k+2} \) and \( M_2 \) and \( M_{3k+3} \) are equivalent, respectively. This means that the evolution from \( M_1 \) to \( M_{3k+2} \) or \( M_2 \) to \( M_{3k+3} \) forms a periodic work cycle. It should be noted that the state transit from \( M_{3k-1} \) to \( M_{3k} \) involves the revisiting process, whereas the others do not, such as transit from \( M_1 \) to \( M_2 \) or from \( M_{3k} \) to \( M_{3k+1} \). Therefore, the state transformation from \( M_1 \) to \( M_{3k+2} \) or from \( M_2 \) to \( M_{3k+3} \) forms a periodic work cycle containing \( 3k - 3 \) local cycles and three global ones.

**D. SCHEDULING STRATEGY OF TRANSIENT PROCESSES**

Assume that the cluster tool operates with a cyclic schedule during the steady state. When the system reaches its full work cycle, we must ensure the state is compatible with the steady state schedule. That is, the SUTP scheduling shall adapt to the steady state. Similarly, the CDTP is subject to the steady state scheduling. As revealed in [1], [4], [5], [47], [48], [51], the virtual wafer method (VWM) has advantages in a variety of scheduling problems of cluster tools, such as steady state scheduling implementation, PM failure response, and transient processes scheduling. Within the VWM-based scheduling framework, each PM is assumed to be occupied by a virtual wafer when the cluster tool boots up, and the virtual wafer will be loaded into the tool system following the last actual wafer \( W_n \). In both the SUTP and CDTP, the system
will be manipulated by the cyclic scheduling as it is executed in the steady state. In this way, cluster tools can be efficiently operated in accordance with the steady state during both the SUTP and CDTP.

The virtual wafer scheduling method provides a simple and efficient implementation framework for the transient process. However, some extra activities containing both the robot and PMs are performed due to the processing of virtual wafers. In other words, we can remove these redundant activities by manipulating the actual wafers only; that is, no virtual wafer is loaded into the system. There is no doubt that the transient process can be accelerated after eliminating unnecessary activities. To analyze temporal properties during the transient processes, we adopt a network technique, namely the program evaluation and review technique (PERT) that has been applied in the transient process scheduling for cluster tools [45]. In the PERT paradigm, the precedence relationships of the robot tasks and PMs can be expressed graphically as a network model. This means that we can find the optimized transient schedule by searching the critical path of the network. Consequently, in the subsequent parts of this paper, we will adopt the PERT-based approach to conduct the property and scheduling analysis for the DACT with WRP during transient processes, including both the SUTP and CDTP.

III. START-UP TRANSIENT PROCESS SCHEDULING

Within the scheduling framework of 1-WCS and 3-WCS proposed in [31], [32], the target steady state of DACTs with 2-WRP is \(\{W_3(1), W_1(4), W_2(3), R_1(W_4(1))\}\), while for the case of \(k\)-WRP with \(k > 2\) it is \(\{W_3(1), W_2(2), W_1(3), R_1(W_4(1))\}\). For the scheduling and control of DACTs with WRP in the SUTP, the crucial problem is how to reach the first target steady state from the idle state in the shortest time. We will discuss how to achieve this goal in subsequent parts.

A. 2-WRP

For 2-WRP, the SUTP consists of two stages. One is the initial stage from the idle state to the first full work cycle state; the other is the regulation one from the first full work cycle state to the target steady state. In the initial stage, the system state evolves as \(M_0 = \{\Theta, \Theta, \Theta, R_0(\Theta)\} \rightarrow M_1 = \{W_1(1), \Theta, \Theta, R_1(\Theta)\} \rightarrow M_2 = \{W_2(1), W_1(2), \Theta, R_2(\Theta)\} \rightarrow M_3 = \{W_3(1), W_2(2), W_1(3), R_3(\Theta)\}\). As indicated by [53], due to the difference of wafer processing time between PM2 and PM3, in the regulation stage, there are two evolution paths: one (denoted as Path A) is \(M_{41} = \{W_3(1), W_1(4), W_2(3), R_3(\Theta)\} \rightarrow M_{51} = \{W_3(1), W_1(4), W_2(3), R_1(W_4(1))\} \rightarrow M_{61} = \{W_4(1), W_2(3), W_1(5), R_2(W_3(3))\} \rightarrow M_{71} = \{W_4(1), W_2(4), W_1(3), R_1(W_5(1))\}\), the other (denoted as Path B) is \(M_{42} = \{W_3(1), W_1(4), W_2(3), R_2(\Theta)\} \rightarrow M_{52} = \{W_3(1), W_1(4), W_2(3), R_1(W_4(1))\} \rightarrow M_{62} = \{W_4(1), W_1(4), W_2(3), R_2(W_5(3))\} \rightarrow M_{72} = \{W_4(1), W_2(4), W_1(5), R_3(W_3(3))\} \rightarrow M_{82} = \{W_4(1), W_2(4), W_3(3), R_1(W_5(1))\}\).

We use \(\omega_{ij}\) to indicate the robot waiting time before its unloading operation at process step \(i\) during the transit from \(M_{j-1}\) to \(M_j\). Then, to reach \(M_3\) from \(M_0\), the robot performs the following activities: \(\text{unloading } R_1 \text{ from the loadlock} \rightarrow \text{moving to PM}_1 \rightarrow \text{loading } W_1(1) \rightarrow \text{PM}_1 \rightarrow \text{moving to the loadlock} \rightarrow \text{unloading raw } W_2 \text{ from the loadlock} \rightarrow \text{moving to PM}_1 \rightarrow \text{waiting } (\omega_{12}) \text{ for } W_1(1) \text{ at PM}_1 \rightarrow \text{swapping at PM}_1 \rightarrow \text{moving to PM}_2 \rightarrow \text{loading } W_1(2) \rightarrow \text{PM}_2 \rightarrow \text{moving to the loadlock} \rightarrow \text{unloading raw } W_3 \text{ from the loadlock} \rightarrow \text{moving to PM}_1 \rightarrow \text{waiting } (\omega_{13}) \text{ for } W_1(1) \text{ at PM}_1 \rightarrow \text{swapping at PM}_1 \rightarrow \text{moving to PM}_2 \rightarrow \text{loading } W_1(3) \rightarrow \text{PM}_2 \rightarrow \text{moving to the loadlock} \rightarrow \text{loading completed } W_1 \text{ into the loadlock} \rightarrow \text{unloading raw } W_3 \text{ from the loadlock} \rightarrow \text{moving to PM}_1 \rightarrow \text{waiting } (\omega_{18}) \text{ for } W_1(1) \text{ at PM}_1\) for PMs.

To reach \(M_{81}\) from \(M_3\) through Path A, the robot performs the following activities: \(\text{moving to PM}_2 \rightarrow \text{waiting } (\omega_{24}) \text{ for } W_2(1) \text{ at PM}_2 \rightarrow \text{moving to PM}_2 \rightarrow \text{swapping } W_3(1) \text{ at PM}_2 \rightarrow \text{waiting } (\omega_{25}) \text{ for } W_2(1) \text{ at PM}_2 \rightarrow \text{moving to PM}_3 \rightarrow \text{moving to PM}_2 \rightarrow \text{unloading raw } W_4 \text{ from the loadlock} \rightarrow \text{moving to PM}_1 \rightarrow \text{waiting } (\omega_{15}) \text{ for } W_1(1) \text{ at PM}_1 \rightarrow \text{moving to PM}_1 \rightarrow \text{waiting } (\omega_{26}) \text{ for } W_2(1) \text{ at PM}_2 \rightarrow \text{swapping } W_3(1) \rightarrow \text{PM}_3 \rightarrow \text{moving to PM}_2 \rightarrow \text{swapping at PM}_2 \rightarrow \text{waiting } (\omega_{36}) \text{ for } W_2(1) \text{ at PM}_2 \rightarrow \text{swapping at PM}_3 \rightarrow \text{moving to PM}_2 \rightarrow \text{swapping at PM}_2 \rightarrow \text{moving to PM}_3 \rightarrow \text{waiting } (\omega_{17}) \text{ for } W_1(5) \text{ at PM}_3 \rightarrow \text{waiting } (\omega_{37}) \text{ for } W_2(1) \text{ at PM}_3 \rightarrow \text{loading } W_4 \text{ from the loadlock} \rightarrow \text{loading completed } W_1 \text{ into the loadlock} \rightarrow \text{unloading raw } W_3 \text{ from the loadlock} \rightarrow \text{moving to PM}_1 \rightarrow \text{waiting } (\omega_{18}) \text{ for } W_1(1) \text{ at PM}_1\) for PMs.

To reach \(M_{82}\) from \(M_3\) through Path B, the robot performs the following activities: \(\text{moving to PM}_2 \rightarrow \text{waiting } (\omega_{24}) \text{ for } W_2(2) \text{ at PM}_2 \rightarrow \text{moving to PM}_2 \rightarrow \text{swapping at PM}_2 \rightarrow \text{waiting } (\omega_{25}) \text{ for } W_2(2) \text{ at PM}_2 \rightarrow \text{moving to PM}_3 \rightarrow \text{moving to PM}_2 \rightarrow \text{unloading raw } W_4 \text{ from the loadlock} \rightarrow \text{moving to PM}_1 \rightarrow \text{waiting } (\omega_{15}) \text{ for } W_1(1) \text{ at PM}_1 \rightarrow \text{moving to PM}_1 \rightarrow \text{waiting } (\omega_{26}) \text{ for } W_2(2) \text{ at PM}_2 \rightarrow \text{swapping at PM}_2 \rightarrow \text{waiting } (\omega_{36}) \text{ for } W_2(2) \text{ at PM}_2 \rightarrow \text{swapping at PM}_3 \rightarrow \text{moving to PM}_2 \rightarrow \text{swapping at PM}_2 \rightarrow \text{moving to PM}_3 \rightarrow \text{waiting } (\omega_{17}) \text{ for } W_1(5) \text{ at PM}_3 \rightarrow \text{waiting } (\omega_{37}) \text{ for } W_2(2) \text{ at PM}_3 \rightarrow \text{swapping at PM}_2 \rightarrow \text{swapping at PM}_3 \rightarrow \text{moving to PM}_2 \rightarrow \text{moving to PM}_3 \rightarrow \text{waiting } (\omega_{18}) \text{ for } W_1(5) \text{ at PM}_1\) for PMs.

We use U, L, M, and S to denote the robot activities of unloading, loading, moving, and swapping operation, respectively. Similarly, \(P_i, i \in \mathbb{N}_3\), indicates the wafer fabrication in PMi. Based on the above robot tasks and PM activity sequences, we can build the PERT model of the transient process scheduling as shown in Fig. 3. In this PERT model, Nodes 0, 1L, 3L, and 6L respectively correspond to states \(M_0, M_1, M_2,\) and \(M_3\). For the Path A, Nodes 8L1, 4L1, 8L1, 11L1, and 9L1 represent states \(M_{41}, M_{51}, M_{61}, M_{71},\) and \(M_{81}\), respectively. For the Path B, Nodes 8L2, 4L2, 7L2,
11_{2U}, and 9_{2U} represent states M_{42}, M_{52}, M_{62}, M_{72}, and M_{82}, respectively.

Let \( \phi_0 \) denote the minimum time taken for the DACT with WRP to reach the first target steady state from the idle state. Correspondingly, the minimum time taken based on the VWM is denoted as \( \phi_V \). With the PERT model, we can calculate \( \phi_0 \) by searching the critical path in the network. We use \( T_k \) to indicate the time taken from the idle state \( \{\theta, \theta, \theta, R_\theta(\theta)\} \) (represented by Node 0) to the terminal state (Node \( k \)). Observing the system PERT model, our eventual goal is to identify which secondary end Node (i.e., Nodes 9_{1U} and 9_{2U}) will be reached first. By searching the PERT model, we can recursively calculating \( T_k \) from the initial Node 0 to the final node. From Node 0 to Node 1L, there is only one operation sequence (represented by U \( \rightarrow \) M \( \rightarrow \) L). This takes at least \( \alpha + \mu + \beta \) time units. Then, we have \( T_{1L} = T_0 + \alpha + \mu + \beta \). However, to reach its succeeding node (i.e., Node 1L), there are two operation sequences. One executes wafer processing in PM1, taking \( a_1 \) time units; the other performs a series of robot tasks (represented by M \( \rightarrow \) U \( \rightarrow \) M), taking \( 2\mu + \alpha \) time units. Thus, we have \( T_{1L} = \max\{T_{1L} + a_1, 2\mu + \alpha\}. Similarly, we can recursively calculate \( T_{2U}, T_{3U}, \ldots, T_{9U} \). Finally, we have \( \phi_0 = T_{1L} = \min\{T_{9_{1U}}, T_{9_{2U}}\} + \lambda \). Therefore, we have the following algorithm.

**B. k-WRP WITH k > 2**

Due to the multiple revisiting processes, the state evolution of DACTs with k-WRP during the SUTP is more complex than 2-WRP. Under the operation mechanism of 3-WCS, it can be divided into three main stages from the idle state to the first target steady state. In the first stage, the system evolves as \( M_0 = \{\theta, \theta, \theta, R_\theta(\theta)\} \rightarrow M_1 = \{W_1(1), \theta, \theta, R_\theta(\theta)\} \rightarrow M_2 = \{W_1(1), W_1(2), \theta, R_\theta(\theta)\} \rightarrow M_3 = \{W_3(1), W_2(2), W_1(3), R_\theta(\theta)\} \rightarrow M_4 = \{W_4(1), W_1(4), W_2(2), W_3(3), R_\theta(W_3(3))\} \). When \( M_4 \) is reached, the system will enter a repeated revisiting processes work cycle, i.e., \( M_4 \rightarrow M_5 = \{W_4(1), W_1(4), W_2(3), R_\theta(W_3(3))\} \rightarrow M_6 = \{W_6(1), W_2(4), W_3(3), R_\theta(W_1(5))\} \rightarrow \cdots \rightarrow M_{3k+1} = \{W_4(1), W_3(6), W_1(7), R_\theta(W_2(7))\} \). In the final stage, the system undergoes two global work cycles and then reaches the first target steady state. That is, \( M_{3k+1} \rightarrow M_{3k+2} = \{W_4(1), W_3(6), W_2(7), R_1(W_3(1))\} \rightarrow M_{3k+3} = \{W_5(1), W_2(4), W_2(7), R_1(W_3(1))\} \rightarrow M_{3k+4} = \{W_6(1), W_2(5), W_3(4), R_1(W_1(5))\} \).

To reach \( M_4 \) from \( M_0 \), the robot performs the following activities: (unloading raw W_1 from the loadlock \( \rightarrow \) moving to PM_1 \( \rightarrow \) loading W_1(1) into PM_1 \( \rightarrow \) moving to the loadlock \( \rightarrow \) unloading raw W_2 from the loadlock \( \rightarrow \) moving to PM_1 \( \rightarrow \) waiting (\( \omega_1(2) \)) \( \rightarrow \) waiting at PM_1 \( \rightarrow \) moving to PM_2 \( \rightarrow \) loading W_2(1) into PM_2 \( \rightarrow \) moving to the loadlock \( \rightarrow \) unloading raw W_3 from the loadlock \( \rightarrow \) moving to PM_1 \( \rightarrow \) waiting (\( \omega_1(3) \)) \( \rightarrow \) unloading W_3 \( \rightarrow \) swapping at PM_3 \( \rightarrow \) moving to PM_3 \( \rightarrow \) loading W_3(1) \( \rightarrow \) moving to PM_3 \( \rightarrow \) moving to the loadlock \( \rightarrow \) unloading raw W_4 \( \rightarrow \) waiting (\( \omega_2(4) \)) \( \rightarrow \) waiting (\( \omega_2(4) \)) \( \rightarrow \) PM_3 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(4) \)) \( \rightarrow \) PM_3 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(4) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_2(4) \)).

To reach \( M_{3k+1} \) from \( M_4 \), the robot performs the following activities: (swapping at PM_3 \( \rightarrow \) moving to PM_2 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_2 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)) \( \rightarrow \) PM_3 \( \rightarrow \) waiting (\( \omega_3(5) \)).

To reach \( M_{3k+4} \) from \( M_{3k+1} \), the robot performs the following activities: (swapping at PM_3 \( \rightarrow \) moving to the loadlock \( \rightarrow \) loading completed W_1 into the loadlock \( \rightarrow \) unloading raw W_5 from the loadlock \( \rightarrow \) moving to PM_1 \( \rightarrow \) waiting (\( \omega_1(3,k+2) \)) \( \rightarrow \) PM_1 \( \rightarrow \) swapping at PM_1 \( \rightarrow \) moving to PM_2 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)) \( \rightarrow \) PM_2 \( \rightarrow \) moving to PM_3 \( \rightarrow \) waiting (\( \omega_2(3,k+3) \)).

**FIGURE 3.** PERT model for the SUTP with 2-WRP.
from the loadlock → moving to PM1 → waiting (ω_{1,3k+3}) for W_{3}(1) at PM1 → swapping at PM1 → moving to PM2 → waiting (ω_{2,3k+4}) for W_{4}(2) at PM2 → swapping at PM2 → moving to PM3 → waiting (ω_{3,3k+4}) for W_{5}(2k+1) at PM3 → swapping at PM3 → moving to the loadlock → loading completed W_{3} into the loadlock → unloading raw W_{7} from the loadlock → moving to PM1 → waiting (ω_{1,3k+4}) for W_{6}(1) at PM1.

According to the system state revolution process as well as corresponding operation sequences, we can build the PERT model (shown in Fig. 4) of the DACT with k-WRP from the idle state to the first target steady state. In this PERT model, Nodes 0, 1, 2, 3, 4, and 6 correspond to states M_{0}, M_{1}, M_{2}, M_{3}, and M_{4} during the first stage, respectively. Since M_{4}, the system starts to execute the revisiting process (i.e., the local work cycle) multiple times. Accordingly, in the local work cycles, states M_{5}, M_{6}, ..., M_{3k+2}, M_{3k+3}, and M_{3k+4} correspond to states N_{9}, N_{10}, ..., (6k + 1)l_{2}, and (6k + 7)l_{2}. In the final stage containing two global work cycles, states M_{3k+2}, M_{3k+3}, and M_{3k+4} correspond to states N_{7}, N_{8}, and N_{9}. For the DACT with k-WRP under k > 2, similar to Algorithm 1, we have the following algorithm.

**IV. CLOSE-DOWN TRANSIENT PROCESS SCHEDULING**

The CDTP starts when the last wafer of a batch is loaded into PM1 and terminates after the last wafer is completed and loaded into the loadlock. For the DACT with 2-WRP, according to the paradigm of 1-WCS, the system reaches \{W_{n}(1), W_{n-3}(4), W_{n-2}(3), R_{1}(W_{n-1}(2))\} when the last wafer W_{n} is loaded into PM1, when W_{n} is completed and delivered to the loadlock, the system reaches \{θ, θ, θ, R_{0}(θ)\}. Consequently, the CDTP of the DACT with 2-WRP starts from \{W_{n}(1), W_{n-3}(4), W_{n-2}(3), R_{1}(W_{n-1}(2))\} and ends up with \{θ, θ, θ, R_{0}(θ)\}. For the DACT with k-WRP, k > 2, based on the 3-WCS, when W_{n} is loaded into PM1, the system reaches \{W_{n}(1), W_{n-2}(2), W_{n-3}(3), R_{1}(W_{n-1}(2))\}. Therefore, the CDTP of the DACT with k-WRP, k > 2, is determined from \{W_{n}(1), W_{n-2}(2), W_{n-3}(3), R_{1}(W_{n-1}(2))\} to \{θ, θ, θ, R_{0}(θ)\}. Note that there are four wafers in the DACT during the CDTP. Consequently, the CDTP of DACTs with WRP can be divided into four stages according to the time point when the completed wafer is loaded into the loadlock.

**A. 2-WRP**

In the first stage, i.e., after the beginning of CDTP while before W_{n-3} is completed and loaded into the loadlock, the system state evolves as: M_{1} = \{W_{n}(1), W_{n-3}(4), W_{n-2}(3), R_{1}(W_{n-1}(2))\} → M_{2} = \{W_{n}(1), W_{n-1}(2), W_{n-2}(3), R_{3}(W_{n-3}(5))\} → M_{3} = \{W_{n}(1), W_{n-2}(4), W_{n-3}(5), R_{3}(W_{n-3}(5))\} → M_{4} = \{W_{n}(1), W_{n-2}(4), W_{n-3}(3), R_{0}(θ)\}. During such a state transition, the robot performs the following activities: (moving to PM2 → waiting (ω_{2,5}) for W_{n-3}(4) at PM2 → swapping at PM2 → moving to PM1 → waiting (ω_{2,6}) for W_{n-2}(4) at PM2 → swapping at PM2 → moving to PM3 → waiting (ω_{3,5}) for W_{n-3}(3) at PM3 → swapping at PM3 → moving to PM2 → waiting (ω_{2,8}) for W_{n-3}(5) at PM2 → swapping at PM2 → moving to PM1 → unloading W_{n} from PM1 → moving to PM2 → waiting (ω_{2,9}) for W_{n-2}(4) at PM2 → swapping at PM2 → moving to PM3 → waiting (ω_{3,8}) for W_{n-3}(3) at PM3 → swapping at PM3 → moving to PM2 → loading W_{n}(4) into PM2 → moving to PM3 → waiting (ω_{3,9}) for W_{n-1}(3) at PM3 → unloading W_{n-1} from PM3 → moving to the loadlock → loading completed W_{n-1} into the loadlock).

In the second stage, i.e., after W_{n-2} is loaded into the loadlock, the system state evolves as: M_{4} → M_{5} = \{θ, W_{n}(2), W_{n-1}(3), R_{3}(W_{n-2}(4))\} → M_{6} = \{θ, W_{n-1}(4), W_{n-3}(5), R_{3}(W_{n-3}(5))\} → M_{7} = \{θ, W_{n-1}(4), W_{n}(3), R_{0}(θ)\}. During this process, the robot performs the following activities: (moving to PM1 → waiting (ω_{1,5}) for W_{n}(1) at PM1 → unloading W_{n} from PM1 → moving to PM2 → waiting (ω_{2,5}) for W_{n-2}(4) at PM2 → swapping at PM2 → moving to PM3 → waiting (ω_{3,5}) for W_{n-3}(3) at PM3 → swapping at PM3 → moving to PM2 → waiting (ω_{2,6}) for W_{n} at PM2 → swapping at PM2 → moving to PM3 → waiting (ω_{3,6}) for W_{n-2}(3) at PM3 → swapping at PM3 → moving to the loadlock → loading W_{n-2} into the loadlock).

In the third stage, i.e., after W_{n-1} is loaded into the loadlock, the system state evolves as: M_{7} → M_{8} = \{θ, W_{n}(3), R_{3}(W_{n-1}(5))\} → M_{9} = \{θ, W_{n}(4), θ, R_{0}(θ)\}. During this process, the robot performs the following activities: (moving to PM2 → waiting (ω_{2,8}) for W_{n-3}(4) at PM2 → unloading W_{n-1} from PM2 → moving to PM3 → waiting (ω_{3,8}) for W_{n}(3) at PM3 → swapping at PM3 → moving to PM2 → loading W_{n}(4) into PM2 → moving to PM3 → waiting (ω_{3,9}) for W_{n-1}(3) at PM3 → unloading W_{n-1} from PM3 → moving to the loadlock → loading completed W_{n-1} into the loadlock).

In the final stage, i.e., after M_{9} while before W_{n} is loaded into the loadlock, the system state evolves as: M_{9} → M_{10} = \{θ, θ, θ, R_{0}(θ)\}. During this process, the robot performs the following activities: (moving to PM2 → waiting (ω_{2,9})
for $W_n(4)$ at PM$_2$ → unloading $W_n(4)$ from PM$_2$ → moving to PM$_3$ → loading $W_n(4)$ into PM$_3$ → waiting ($\omega_{3,10}$) for $W_n(5)$ at PM$_3$ → unloading $W_n(5)$ from PM$_3$ → moving to the loadlock → loading completed $W_n$ into the loadlock).

Up to now, we have provided the operation sequence across the entire CDTP. This allows us to easily build the PERT model for the DACT with 2-WRP during the CDTP, which is shown as Fig. 5. During the first stage, states $M_1$ and $M_3$ respectively correspond to Nodes 1$_L$ and 3$_L$, and state $M_7$ corresponds to 8$_U$'s preceding node. In the third stage, state $M_8$ and state $M_9$ correspond to Node 9$_U$ and Node 11$_U$'s preceding node, respectively. Finally, state $M_{10}$ corresponds to the terminal Node 13. We use $\Gamma_k$ to indicate the time taken from the initial state of CDTP (represented by Node 1), i.e., $\{W_n(1), W_n(4), W_n(3), R_1(W_{n-1}(2))\}$ for 2-WRP and $\{W_n(1), W_n(2), W_n(3), R_1(W_{n-1}(2))\}$ for $k$-WRP with $k > 2$ to the terminal state (Node k). Let $\Phi_0$ indicate the time taken to complete the CDTP of the DACT with WRP. Similarly, the same time
**Algorithm 3** \( \Phi_0 \) Computation for 2-WRP

1. \( \Gamma_{L_1} \), the system starts to switch from the steady state to the CDTP;
2. \( \Gamma_{L_2} = \Gamma_{L_1} + \mu + \lambda; \)
3. \( \Gamma_{L_3} = \Gamma_{L_2} + \mu + \lambda; \)
4. \( \Gamma_{L_4} = \max(\Gamma_{L_2} + a_2, \Gamma_{L_3} + \mu); \)
5. \( \Gamma_{L_5} = \Gamma_{L_4} + \mu + \lambda; \)
6. \( \Gamma_{L_6} = \max(\Gamma_{L_3} + a_3, \Gamma_{L_4} + \mu); \)
7. \( \Gamma_{L_7} = \Gamma_{L_6} + \mu + \lambda; \)
8. \( \Gamma_{L_8} = \Gamma_{L_7} + \mu; \)
9. \( \Gamma_{L_9} = \Gamma_{L_8} + \mu + \lambda; \)
10. \( \Gamma_{L_{10}} = \Gamma_{L_9} + \mu + \lambda; \)
11. \( \Gamma_{L_{11}} = \Gamma_{L_{10}} + 2 \mu + \beta; \)
12. \( \Gamma_{L_{12}} = \Gamma_{L_{11}} + \mu + \lambda; \)
13. \( \Gamma_{L_{13}} = \Gamma_{L_{12}} + 2 \mu + \beta; \)
14. \( \Gamma_{L_{14}} = \Gamma_{L_{13}} + \mu + \lambda; \)
15. \( \Gamma_{L_{15}} = \Gamma_{L_{14}} + 2 \mu + \beta; \)
16. \( \Gamma_{L_{16}} = \Gamma_{L_{15}} + \mu + \lambda; \)
17. \( \Gamma_{L_{17}} = \Gamma_{L_{16}} + 2 \mu + \beta; \)
18. \( \Gamma_{L_{18}} = \Gamma_{L_{17}} + \mu + \lambda; \)
19. \( \Gamma_{L_{19}} = \Gamma_{L_{18}} + 2 \mu + \beta; \)
20. \( \Gamma_{L_{20}} = \Gamma_{L_{19}} + \mu + \lambda; \)
21. \( \Gamma_{L_{21}} = \Gamma_{L_{20}} + 2 \mu + \beta; \)
22. \( \Gamma_{L_{22}} = \Gamma_{L_{21}} + \mu + \lambda; \)
23. \( \Gamma_{L_{23}} = \Gamma_{L_{22}} + 2 \mu + \beta; \)
24. \( \Gamma_{L_{24}} = \Gamma_{L_{23}} + \mu + \lambda; \)
25. \( \Gamma_{L_{25}} = \Gamma_{L_{24}} + 2 \mu + \beta; \)
26. **Stop.**

Based on the VWM is denoted as \( \Phi_V \). Therefore, we can calculate \( \Phi_0 \) for the DACT with 2-WRP according to the following algorithm.

**B. k-WRP with** \( k > 2 \)

In the first stage, i.e., after the beginning of CDTP while \( W_{n-3} \) is completed and loaded into the loadlock, the system state evolves as: \( M_1 = \{ W_{n}(1), W_{n-2}(2), W_{n-3}(3), R_{1}(W_{n-1}(2)) \} \rightarrow M_2 = \{ W_{n}(1), W_{n-1}(2), W_{n-3}(3), R_{3}(W_{n-2}(3)) \} \rightarrow M_3 = \{ W_{n}(1), W_{n-1}(3), W_{n-2}(3), R_{3}(W_{n-3}(3)) \} \rightarrow M_4 = \{ W_{n}(1), W_{n-3}(4), W_{n-4}(4), R_{3}(W_{n-5}(5)) \} \rightarrow \cdots \rightarrow M_{3k-2} = \{ W_{n}(1), W_{n-2}(2k), W_{n-1}(2k-1), R_{3}(W_{n-3}(2k+1)) \} \rightarrow M_{3k-1} = \{ W_{n}(1), W_{n-1}(2k), W_{n-2}(2k+1), R_{3}(W_{n-3}(2k+1)) \} \rightarrow M_{3k} = \{ W_{n}(1), W_{n-1}(2k), W_{n-2}(2k+1), R_{0}(\theta) \} \). During this process, the robot performs the following activities: (moving to PM2 \( \rightarrow \) waiting \( \omega_{2,2} \) for \( W_{n-2}(2) \) at PM2 \( \rightarrow \) swapping at PM2 \( \rightarrow \) moving to PM3 \( \rightarrow \) waiting \( \omega_{3,2} \) for \( W_{n-3}(3) \) at PM3 \( \rightarrow \) swapping at PM3 \( \rightarrow \) moving to PM2 \( \rightarrow \) waiting \( \omega_{2,3} \) for \( W_{n-1}(2) \) at PM2 \( \rightarrow \) swapping at PM2 \( \rightarrow \) moving to PM3 \( \rightarrow \) waiting \( \omega_{3,3} \) for \( W_{n-2}(3) \) at PM3 \( \rightarrow \) swapping at PM3 \( \rightarrow \) moving to PM2 \( \rightarrow \) waiting \( \omega_{2,4} \) for \( W_{n-3}(4) \) at PM2 \( \rightarrow \) swapping at PM2 \( \rightarrow \) moving to PM3 \( \rightarrow \) waiting \( \omega_{3,4} \) for \( W_{n-2}(2) \) at PM3 \( \rightarrow \) swapping at PM3 \( \rightarrow \) moving to PM2 \( \rightarrow \) moving to PM3 \( \rightarrow \) waiting \( \omega_{3,5} \) for \( W_{n-1}(1) \) at PM3 \( \rightarrow \) swapping at PM3 \( \rightarrow \) moving to the loadlock \( \rightarrow \) loading complete \( W_{n-1}(2k-1) \) into the loadlock).

In the second stage, i.e., after \( M_{3k} \) while before \( W_{n-2} \) is loaded into the loadlock, the system state evolves as: \( M_{3k} \rightarrow M_{3k+1} = \{ \theta, W_{n}(2), W_{n-1}(2k+1), R_{0}(\theta)\} \). During this process, the robot performs the following activities: (moving to PM1 \( \rightarrow \) waiting \( \omega_{1,3k+1} \) for \( W_{n}(1) \) at PM1 \( \rightarrow \) unloading \( W_{n} \) from PM1 \( \rightarrow \) moving to PM2 \( \rightarrow \) waiting \( \omega_{2,3k+1} \) for \( W_{n-1}(2k) \) at PM2 \( \rightarrow \) swapping at PM2 \( \rightarrow \) moving to PM1 \( \rightarrow \) waiting \( \omega_{3,3k+1} \) for \( W_{n-1}(3) \) at PM3 \( \rightarrow \) waiting \( \omega_{2,4k+1} \) for \( W_{n-2}(2) \) at PM2 \( \rightarrow \) moving to PM3 \( \rightarrow \) waiting \( \omega_{3,5k+1} \) for \( W_{n-1}(1) \) at PM3 \( \rightarrow \) swapping at PM3 \( \rightarrow \) moving to the loadlock \( \rightarrow \) loading complete \( W_{n-1}(2k-1) \) into the loadlock).

In the third stage, i.e., after \( M_{3k+1} \) while before \( W_{n-1} \) is loaded into the loadlock, the system state evolves as: \( M_{3k+1} \rightarrow M_{3k+2} = \{ \theta, \theta, W_{n}(3), R_{0}(\theta)\} \). During this process, the robot performs the following activities: (moving to PM2 \( \rightarrow \) waiting \( \omega_{2,3k+2} \) for \( W_{n}(2) \) at PM2 \( \rightarrow \) moving to PM3 \( \rightarrow \) waiting \( \omega_{3,3k+2} \) for \( W_{n-1}(2k+1) \) at PM3 \( \rightarrow \) swapping at PM3 \( \rightarrow \) moving to the loadlock \( \rightarrow \) loading complete \( W_{n-1}(2k-1) \) into the loadlock).

In the final stage, i.e., after \( M_{3k+2} \) while before \( W_{n} \) is loaded into the loadlock, the system state evolves as: \( M_{3k+2} \rightarrow M_{3k+3} = \{ \theta, \theta, W_{n}(3), R_{3}(W_{n}(4)) \} \rightarrow M_{3k+4} = \{ \theta, \theta, W_{n}(5), R_{3}(W_{n}(6)) \} \rightarrow \cdots \rightarrow M_{4k+1} = \{ \theta, \theta, W_{n}(2k-1) \} \rightarrow R_{3}(W_{n}(2k)) \rightarrow M_{4k+2} = \{ \theta, \theta, W_{n}(2k+1) \} \rightarrow R_{3}(W_{n}(0)) \rightarrow M_{4k+3} = \{ \theta, \theta, \theta, R_{0}(\theta)\} \). During this process, the robot performs the following activities: (moving to PM3 \( \rightarrow \) waiting \( \omega_{3,4k+3} \) for \( W_{n}(3) \) at PM3 \( \rightarrow \) unloading \( W_{n}(3) \) from PM3 \( \rightarrow \) moving to PM2 \( \rightarrow \) loading \( W_{n}(4) \) into PM2 \( \rightarrow \) waiting \( \omega_{2,3k+4} \) for \( W_{n}(4) \) at PM2 \( \rightarrow \) unloading \( W_{n}(4) \) from PM2 \( \rightarrow \) moving to PM3 \( \rightarrow \) loading \( W_{n}(5) \) into PM3 \( \rightarrow \) waiting \( \omega_{3,4k+4} \) for \( W_{n}(5) \) at PM3 \( \rightarrow \cdots \rightarrow \) unloading \( W_{n}(2k-1) \) from PM3 \( \rightarrow \) moving to PM2 \( \rightarrow \) loading \( W_{n}(2k) \) into PM2 \( \rightarrow \) waiting \( \omega_{2,4k+2} \) for \( W_{n}(2k) \) at PM2 \( \rightarrow \) unloading \( W_{n}(2k) \)
from PM2 → moving to PM3 → loading \( W_3/(2k + 1) \) into PM3 → waiting \((\omega_3, 4k + 2)\) for \( W_n/(2k + 1) \) at PM3 → unloading \( W_3/(2k + 1) \) from PM3 → moving to the loadlock → loading completed \( W_n \) into the loadlock).

Based on the above operation sequence, we can build the PERT model as shown in Fig. 6. In the first stage, state \( M_1, M_3, M_4, \cdots, M_{3k-2} \), and \( M_{3k-1} \) correspond respectively to Nodes 1, 3, 5, 2, \( (6k - 7) \), \( (6k - 5) \), M2, while M2 and M3 correspond to 2's succeeding node and 1's preceding node, respectively. During the rest stages, states \( M_{3k+1}, M_{3k+2}, M_{3k+3}, M_{3k+4}, \cdots, M_{4k+1}, M_{4k+2}, \) and \( M_{4k+3} \) correspond to \( (6k - 2) \)'s succeeding node, \( (6k - 1) \)'s preceding node, Nodes \( (6k)U, (6k + 2)U, \cdots, (8k - 4)U, (8k - 2)U, \) and \( 8k - 1 \), respectively. To calculate \( \Phi_0 \) of the DACT with \( k \)-WRP under \( k > 2 \), we have the following algorithm.

V. ILLUSTRATIVE EXAMPLES

In this section, several examples are provided to demonstrate the preceding section results. In the following examples, the time unit is second, abbreviated as s.

**Example 1:** The wafer processing time at process steps 1-3 are 76 s, 43 s, and 32 s, i.e., \( a_1 = 76 \) s, \( a_2 = 43 \) s, and \( a_3 = 32 \) s. The robot task times of unloading, loading, moving, and swap operation are \( \alpha = \beta = \mu = 4 \) s, and \( \lambda = 10 \) s, respectively.

In this case, the bottleneck of the revisiting process is the second process step. For 2-WRP, by combining the VWM-based 1-WCS in [32], it will take 446 s and 410 s to reach the first target steady state and complete the CDTP. However, it takes 402 s and 341 s to do so via Algorithms 1 and 3, respectively. For \( k \)-WRP with \( k > 2 \), with the VWM-based 3-WCS in [31], it will take 1106 s, 1424 s, and 1742 s to reach the first target steady state and 898 s, 1216 s, and 1534 s to complete the CDTP, when \( k = 3, 4, \) and 5, respectively. By using Algorithms 2 and 4, it takes 814 s, 963 s, 1122 s, and 688 s, 946 s, 1204 s, respectively. Algorithms presented in this paper obtain a great reduction in transient processes schedule.

**Example 2:** The wafer processing time at process steps 1-3 are 110 s, 45 s, and 80 s, respectively; and \( \alpha = \beta = 4 \) s, \( \mu = 2 \) s, and \( \lambda = 8 \) s.

In this case, different from Example 1, \( a_3 > a_2 \), i.e., the third process step is the bottleneck of the revisiting process. For 2-WRP, it takes 515 s and 468 s to reach the first target steady state and finish the CDTP, respectively, according to Algorithms 1 and 3, whereas it takes 614 s and 551 s respectively by using the VWM-based 1-WCS. For \( k \)-WRP when \( k \) are respectively 3, 4, and 5, it takes 1536 s, 1986 s, and 2212 s to reach the first target steady state by the VWM-based 3-WCS, whereas it merely needs 1098 s, 1280 s, and 1551 s respectively by Algorithm 2. As for the CDTP, according to Algorithm 4, it will take 961 s, 1318 s, and 1675 s, respectively, while it takes 1312 s, 1762 s, and 2212 s by the
TABLE 1. Comparison of the experimental results.

| No. | Manufacturing Parameters | Start-Up Process | Close-Up Process |
|-----|--------------------------|------------------|------------------|
|     | α/β μ λ a1 a2 a3 k | ϕV | ϕO | Reduction (%) | ϕV | ϕO | Reduction (%) |
| 1   | 4 4 10 76 43 32 | 2 446 | 402 | 9.87 | 410 | 341 | 16.83 |
|     |                  | 3 1106 | 814 | 26.4 | 898 | 688 | 23.39 |
|     |                  | 4 1424 | 963 | 32.37 | 1216 | 946 | 22.2 |
|     |                  | 5 1742 | 1122 | 35.59 | 1534 | 1204 | 21.51 |
| 2   | 4 2 8 110 45 67 | 2 614 | 515 | 16.12 | 551 | 486 | 11.8 |
|     |                  | 3 1536 | 1098 | 28.52 | 1312 | 961 | 26.75 |
|     |                  | 4 1986 | 1280 | 35.55 | 1762 | 1318 | 25.2 |
|     |                  | 5 2436 | 1551 | 36.33 | 2212 | 1675 | 24.28 |
| 3   | 3 3 8 320 180 210 | 2 1758 | 1356 | 22.87 | 1554 | 1344 | 15.31 |
|     |                  | 3 4378 | 2999 | 31.5 | 3518 | 2801 | 20.38 |
|     |                  | 4 5686 | 3653 | 35.75 | 4826 | 3863 | 19.95 |
|     |                  | 5 6994 | 4299 | 38.53 | 6134 | 4925 | 19.71 |
| 4   | 4 3 10 450 260 190 | 2 2177 | 1851 | 14.97 | 1923 | 1579 | 17.89 |
|     |                  | 3 5637 | 3981 | 29.38 | 4460 | 3325 | 25.45 |
|     |                  | 4 7257 | 4781 | 34.12 | 6080 | 4607 | 24.23 |
|     |                  | 5 8877 | 5601 | 36.9 | 7700 | 5889 | 23.52 |

VWM-based 3-WCS, respectively. Algorithms proposed in this paper outperform appreciably beyond the VWM-based scheduling approach for the transient processes with WRP.

We also provide two cases (No. 3 and 4 in TABLE 1) with significant differences between the robot task time and processing times. Details of these cases provided in this section can refer to TABLE 1. Compared with the VWM-based scheduling approach in [31], [32], the PERT-based method achieves significant time reduction. Especially as the increase of k, the time taken for the SUTP decreases more significantly than the VWM-based schedule. As a whole, in terms of time, the PERT-based scheduling method for the transient process is superior to the VWM-based cyclic scheduling approach, even though the latter one is easier to implement.

VI. CONCLUSION
As the growing tendency of high-mix and low-volume production, the wafer lot size decreases steadily, leading to an increasing number of the transient process. In particular, wafer revisiting makes this scheduling problem more complicated. This paper is concerned about the transient process scheduling problems for DACTs with WRP. For the sake of the simplicity of cyclic scheduling in implementation, existing research tends to adopt a virtual wafer scheduling method to operate transient processes for DACTs with WRP, resulting in extensive redundant activities. To resolve such a problem, we adopt a PERT-based model to analyze transient processes of DACTs with WRP comprehensively. Moreover, we present computationally efficient algorithms to optimize transient processes. The numerical experimental results indicate that the proposed approach performs much better than the virtual wafer scheduling method. Future studies are expected to extend the proposed method to transient process scheduling for cluster tools with WRP and WRTCs. It is also meaningful to investigate parallel PMs and other complex cases caused by disruptive events reported in [17]–[21].

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