Collaborative Distillation Meta Learning for Simulation Intensive Hardware Design

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Abstract

This paper proposes a novel collaborative distillation meta learning (CDML) framework for simulation intensive hardware design problems. Deep reinforcement learning (DRL) has shown promising performance in various hardware design problems. However, previous works on DRL-based hardware design only dealt with problems with simplified objectives, which are not practical. In fact, the objective evaluation of real-world electrical performance through simulation is costly in terms of both time and computation, making DRL scheme involving extensive reward calculations not suitable. In this paper, we apply the CDML framework to decoupling capacitor placement problem (DPP), one of the significant simulation intensive hardware design problems. The CDML framework consists of a context-based meta learner and collaborative distillation scheme to produce a reusable solver. The context-based meta learner captures the location of probing port (i.e., target circuit block) and improves generalization capability. The collaborative distillation scheme with equivariant label transformation imposes the action-permutation (AP)-equivariant nature of placement problems, which not only improves sample efficiency but also improves generalization capability. Extensive experimental results verified that our CDML outperforms both neural baselines and iterative conventional design methods in terms of real-world objective, power integrity, with zero-shot transfer-ability.

1 Introduction

With the CMOS technology shrink and increasing data rate, the design complexity of very large-scale integrated (VLSI) has increased. Human experts are no longer able to design hardware without the help of electrical design automation (EDA) tools, and EDA tools now suffer from time complexity of simulations and insufficient computing power, making machine learning (ML) application to hardware design inevitable. ML functionalities such as decision-making, performance prediction, black-box optimization, and automated design play important roles in hardware design [1].

Many studies have already shown that deep reinforcement learning (DRL), one of the representative ML method for sequential decision making, is applicable to various tasks in modern chip design; chip placement [2, 3], routing [4, 5], circuit design [6], logic synthesis [7, 8] and bi-level hardware optimization [9]. However, most DRL-based hardware design methods used simplified objectives. For example, DRL-based placement and routing works [2, 4, 5] took wire-length and congestion as objectives for fast computations, instead of actual electrical performance.

Hardware design with simplified objectives is, in fact, insufficient for practical industrial application. Firstly, real-world hardware design involves a number of electrical simulations to evaluate objectives that require extensive computing power and time; high sample efficiency should be achieved. Secondly, hardware design flow involves multi-level optimization of various problems such as layout, floor-
planning, chip placement, routing, and decap placement. That means the constraints and requirements of a problem vary according to higher-level problems in the design flow: generalization capability is needed to adapt to new constraints and requirements of the problem with few-shot inferences. We define these real-world hardware design characteristics as simulation intensive hardware design. This paper extends ML method into a simulation intensive hardware design, which can make a groundbreaking contribution to the semiconductor industry and, at the same time, promote the development of practical ML-based design solvers.

**Target Problem.** This paper focuses on decoupling capacitor placement problem (DPP), one of the essential simulation intensive hardware design problems. Decoupling capacitor (decap) is a hardware component that reduces noise along with the power distribution network (PDN) of hardware devices. With transistor scaling and continuously decreasing supply voltage margin [10], power noise has become a huge technical bottleneck of high-speed computing systems. Generally, the more decaps are placed, the more reliable the power supply is. However, adding more decaps requires more space and is costly. Thus, finding optimal placement of decaps is important in terms of hardware performance and cost/space-saving.

DPP is formulated as a combinatorial optimization problem with simulated electrical performance in terms of power integrity (PI) as the objective and the number of decaps as the constraint. Probing port is a port on PDN, where PI is evaluated and keep-out regions refer to decap-prohibited ports. DPP consists of probing port and keep-out region locations that are determined by higher-level problems in the hardware design process such as chip placement and routing; generalization capability is needed.

Power integrity of a design is evaluated by the impedance at the probing port (i.e., target circuit location) over a wide frequency range, and this requires costly simulations; high sample efficiency is required. Thus, PI evaluation cannot be formulated as a closed analytical form, making conventional mixed-integer linear programming (MILP)-based combinatorial optimization approaches not applicable. Therefore, classical genetic algorithm (GA)-based methods [11, 12, 13, 14], black-box optimization methods, have long been used to solve DPP. Despite its effectiveness and efficient exploration over a huge design space, GA unavoidably requires many simulations and is not reusable; GA undergoes massive iterations for each given DPP task (i.e., sample inefficient). To overcome such limitations, there have been attempts to use DRL-based reusable policy training to solve DPP [15, 16]. However, training with DRL methods is still limited by poor sample efficiency and unsatisfactory performance on generalization.

**Contributions.** To tackle the simulation intensive hardware design, we propose a novel collaborative distillation meta-learning (CDML) framework to overcome the limitations of GA and DRL in terms of sample efficiency and generalization capability. Our CDML was verified on a real-world chip-package hierarchical PDN model [17, 18]. Fig. 1 shows the overall illustration of our method. Technical novelties of CDML are summarized below:

**Novel Meta Learning Architecture.** We suggest a context-based meta learner that is a modified attention model (AM) architecture [19]. To accelerate the problem adaptation of AM to varying probing port locations, we specifically devised (1) probing port context network (PCN) and (2) recurrent context network (RCN), which are integrated into the AM-based sequential design policy. PCN was designed so that the learned solver can adapt well to new problems and derive high-quality solutions through zero-shot transfer-ability (i.e., adaptation over problems). RCN was designed so that the learned solver can contextualize the current design stage and adapt its sequential decision-making scheme, given the recognized contexts (i.e., adaptation over the design stages within a problem).
Novel Collaborative Learning Scheme. We present a collaborative distillation scheme with equivariant label transformation. Equivariant properties are universal meta-features that can improve generalization capability, when properly imposed. DPP has an action-permutation (AP)-equivariance, a nature of placement problem; the order of placement does not affect the overall performance. We imposed AP equivariance of DPP through both expert distillation and self-distillation to greatly improve generalization capability with sparse training samples.

- **Expert Distillation** imitates high-quality expert labels generated by a genetic algorithm (GA). To increase sample efficiency and impose label equivariance, we transform the expert labels by permuting the order of decap placement and using both the original and the transformed labels for supervised imitation learning.
- **Self-Distillation** supports the expert distillation process to further improve generalization capability by imposing universal label equivariance over wider action space. We maximize the similarity between the probabilities of the self-generated labels and their transformed labels. Because the quality of self-generated labels gradually increases over the phase of training, self-distillation allows generalization over actions with diverse quality.

2 Related Works

Previous works on DPP are briefly introduced. Detailed literature reviews are provided in Appendix A.

**Genetic Algorithm-based Methods.** The most competitive non-learning method for DPP is the genetic algorithm (GA) [11, 12, 13, 14]. GA is easy-to-implement in black-box optimization tasks. However, GA needs a massive iteration of objective evaluation per each DPP task to obtain a near-optimal solution.

**Deep Reinforcement Learning-based Methods.** Several DRL methods to solve DPP were proposed since the work of [20] using Q-learning and several approaches with convolutional neural network (CNN)-based Q approximator were proposed by [21, 22] later. However, their methods were sample inefficient and their trained policies were non-reusable; if the DPP task changes, they must be re-trained. In an effort to overcome the reusability limitation, [15, 16] implemented promising neural combinatorial optimization (NCO) models, the attention model [19] and pointer network [23], to construct a reusable policy without iterative exploration and domain knowledge. However, their methods still showed poor sample efficiency and unsatisfactory generalization performance.

3 Collaborative Distillation Meta Learning (CDML) Framework

This section provides technical details of the collaborative distillation meta learning (CDML) framework for training a reusable DPP solver. Each subsection discusses problem formulation, proposed neural architecture, and the training methodology.

3.1 Parameterized Sequential Decision-Making Process

Decap Placement Problem (DPP) benchmark is defined as finding the best placement of a given number of decaps on a PDN with a probing port and keep-out regions [16]. Probing port refers to the critical point on PDN, where operating ICs are located or close to; thus, the impedance must be suppressed for reliable power supply. Keep-out regions are action-prohibited areas, where decaps cannot be placed as a design constraint. The ports on PDN are represented as $N_{\text{row}} \times N_{\text{col}}$ grids, and the number of decaps is denoted by $K$. See Appendix B.2 for details in modeling of PDN and decap.

The procedure of solving DPP is modeled as a sequential decision-making process. Each grid (i.e., port) on PDN is represented as a three-dimensional feature vector $x = (\text{coord}_x, \text{coord}_y, \text{type})$, where type indicates whether the port belongs to a probing port $p$ (type = 2), keep-out regions $ko$ (type = 1), or decap allowed ports $d$ (type = 0). Note that $ko$ and $d$ represent a vector consisting of indices corresponding to keep-out regions and decap allowed ports, respectively. $p$ refers to an index of probing port. For the details of the indexing rule for DPP dataset, see Appendix B.3.

The design process sequentially places decaps on the available PDN ports until planning all the designated $K$ decaps. We model this sequential decision-making process with state, action, and policy as follows:
Figure 2: Illustration of DPP’s sequential decision making process using meta learner.

State $s$ is represented as $s = \{s_t\}_{t=1}^K$ where: $s_t = \{p, k_o, a_{1:t}\}$.

Action $a_t \in \{1, ..., N_{row} \times N_{col}\} \setminus s_{t-1}$ is defined as an allocation of a decap to one of the available ports on PDN. The available ports are the ports on PDN except for the probing port, keep-out ports, and the previously selected ports. The concatenation of sequentially selected actions $a = a_{1:K}$ indicates the final decap placement design.

Policy $\pi_\theta(a|p, k_o)$ is the probability of producing a specific design $a = a_{1:K}$, given the probing port index $p$ and keep-out port indices vector $k_o$, and is factorized as:

$$\pi_\theta(a|p, k_o) = \prod_{t=1}^K p_\theta(a_t|s_{t-1})$$

where $p_\theta(a_t|s_{t-1})$ is the segmented one-step action policy parameterized by the neural network.

The objective of DPP is to find the optimal parameter $\theta^*$ of the policy $\pi_\theta(\cdot|p, k_o)$ as:

$$\theta^* = \arg\max_{\theta} \mathbb{E}_{(p, k_o) \sim \rho} \left[ \mathbb{E}_{a \sim \pi_\theta(\cdot|p, k_o)}[\text{Obj}(a)] \right]$$

where $\rho$ is the probability distribution for varying initial state $s_0 = (p, k_o)$. Finding the optimal policy for various DPPs is a multi-task learning problem, in which each DPP is a distinct task. Once the task $s_0$ is specified by $\rho$, the state-action space with complexity of $\left( N_{row} \times N_{col} - 1 - k_o \right)$ is determined. Thus, an efficient policy $\pi_\theta(a|p, k_o)$ should capture the meta-features among varying tasks $s_0 = (p, k_o)$ that have varying state-action space.

### 3.2 Neural Network Architecture of Meta Learner

Our meta learner is a meta-learning expansion of the neural network architecture, attention model (AM) [19], which was designed to generate a sequential route for the vehicle to complete the distributed tasks. We modified the AM architecture to effectively generate a decap placement design, given the initial problem contexts, i.e., the probing port and keep-out ports.

The decision-making procedure consists of two main components: (1) encoder capturing initial design conditions while contextualizing the probing port through the probing port context network (PCN), and (2) decoder sequentially allocating decaps on PDN while contextualizing the stages of the partial solution through the recurrent context network (RCN). See Appendix D for detailed implementation of each component in our neural network architecture. Fig. 2 illustrates the overall design process.

**Encoder.** Our encoder consists of multi-head attention (MHA) and feedforward (FF), similar to the transformer network [24]. The initial state $s_0$ representing the $N_{row} \times N_{col}$ ports of DPP are converted into vectors from top left to bottom right. The encoder takes these vectors as an input and outputs node embedding $h$ for all ports. Encoding is processed once at the initial state, $t = 0$. The node embedding $h$ is time-invariant (i.e., fixed after the encoding process) and is used in the decoding process.

We proposed a novel probing context network (PCN) in the encoding process so that the learned solver can adapt well to a new task and derive a solution well through zero-shot transfer-ability. PCN
is a simple but effective two-layer perceptron model with a ReLU activation layer that takes $h_p$ as an input and outputs the probing port contextual vector $c(p)$.  

**Decoder.** With the node embedding $h$ generated by the encoder, decoder sequentially selects an action $a_t$, given the current design solution $s_t$ until placing all $K$ decaps.

At each step $t$, the decoder takes (1) the node embedding $h$ (static information), (2) the previous partial solution $s_{t-1}$, and (3) the action context embedding $c_{a_{t-1}}$ generated by the recurrent context network (RCN) as inputs and outputs a new action $a_t$. To leverage sequential state transitions in decoder, we devised the recurrent context network (RCN). RCN is a two-layer perceptron model with a ReLU activation layer that embeds the previously selected node's embedding $h_{a_{t-1}}$ at step $t$ into $c_{a_{t-1}}$. Then, context embedding $c = c(p) + c_{a_{t-1}}$ is generated for MHA in decoding process.

### 3.3 Collaborative Distillation Learning Scheme

We devised a collaborative distillation loss term by adding the expert distillation loss and the self-distillation loss to generate a high-quality solver. AP-equivariance of DPP was imposed on the learned model through AP-transformation $T_{AP}$, which permutes the order of placement.

The proposed collaborative distillation loss is given as:

$$
L := L_{Expert} + \lambda L_{Self}
$$

$$
L_{Expert} = -E_{a^*,s_0 \sim D}[\log p_\theta(T_{AP}(a^*)|s_0)]
$$

$$
L_{Self} = E_{a',s_0 \sim U}[||p_\theta(a'|s_0) - p_\theta(T_{AP}(a')|s_0)||_1]
$$

The $L_{Expert}$ is a cross-entropy loss defined with the learnable policy $p_\theta$ and expert labels ($a^*$); similar to the teacher-forcing approach for imitation learning [25]. $L_{Self}$ is a consistency loss defined by the difference between self-generated labels $a'$ and their transformed labels $T_{AP}(a')$. Note that $\lambda$ is a hyperparameter that adjusts the weighted ratio between $L_{Expert}$ and $L_{Self}$.

**Expert Distillation.** Firstly, a genetic algorithm (GA) generates expert labels through several iterations (i.e., simulations). See Appendix C for details. Then, we implement AP-transformation $T_{AP}$ to augment the expert labels $a^*$, which not only reduces the number of simulations during the label collection phase but also imposes an inductive bias on the neural network model. $P$ is a hyperparameter referring to the number of transformed labels per each expert label. We later use the augmented expert labels to learn a policy that generates high-quality solutions by a single inference.

Note that GA is not the only choice for generating expert labels. Expert policy can be substituted by human experts, existing data from industries, or any other algorithms. We took GA as an expert policy just for a benchmark to measure CDML's sample efficiency and performance.

**Self-Distillation.** We impose an inductive bias not only through supervised expert signal but also through self-supervised signal, which is the self-generated labels $a'$ sampled by a fixed copy of policy $p_\theta$ during the training. The quality of the sampled labels is poor at the beginning but improves over the phase of training. Self-distillation learning with the AP-transformation of self-generated labels $a'$ imposes an inductive bias (i.e., AP-equivariance) and thus improves generalization capability in a wider action space. As a result, the trained model has a greater generalization ability in comparison to the model trained only with high-quality expert labels.

### 4 Experimental Results

This section reports the experimental results of the proposed CDML on DPP. The performance of our learned policy was compared to learning-based methods and search-heuristic methods. Then, the results are analyzed through various ablation studies. Performance was evaluated with real-world chip-package hierarchical PDN and decap models.

#### 4.1 Setup

**Expert Label Generation.** GA was used to generate expert labels in this study. We denote $N$ as the number of expert labels for training CDML and investigate how the proposed CDML performs depending on $N$, which refers to sample efficiency of training. In addition, we represent the quality...
Z-parameter of target PDN.

We used the number of decap 100 with batch size Z where gives a N sized PDN give reasonable verification of CDML on simulation intensive hardware design.

To investigate the effectiveness of CDML components compared to the same imitation learning instead of reinforcement learning, whose methods are denoted respectively as AM-IL and Arb-IL, performance on the same setup. In addition, we modified AM-RL and Arb-RL with imitation learning based baselines, AM-RL [15] and Arb-RL [16]. We reproduced these two methods to compare the of simulations (i.e., M > 100) algorithm (i.e., expert policy). Since these methods are iterative solvers, they require a large number

For search heuristic baseline methods, we implemented random search and genetic baselines. For training, we generate three transformed labels per one expert label. We set the distribution ρ = 3 as the number of AP-transformed labels per expert label. Thus, the total number of guiding labels becomes N × (P + 1). For instance, P = 3, N = 50 makes total 50 × 3 + 50 = 200 guiding labels. We set the distribution ρ, described in Section 3.1, as uniform distribution for training.

For the learning algorithm, we used ADAM [26] with a learning rate of 10⁻⁵. We trained our model with batch size 100 for N < 200 and batch size 1,000 for N = 1, 000 and 2, 000. We trained for a maximum of 200 epochs for each model; we used the model with the best validation score for CDML and other ML baselines to evaluate performance. See Appendix E for detailed setup.

### Baselines

For search heuristic baseline methods, we implemented random search and genetic algorithm (i.e., expert policy). Since these methods are iterative solvers, they require a large number of simulations (i.e., M ≥ 100). See Table 1). For learning-based solvers, we reported two RL-based baselines, AM-RL [15] and Arb-RL [16]. We reproduced these two methods to compare the performance on the same setup. In addition, we modified AM-RL and Arb-RL with imitation learning instead of reinforcement learning, whose methods are denoted respectively as AM-IL and Arb-IL, to investigate the effectiveness of CDML components compared to the same imitation learning.
Table 1: Performance evaluation with the average score of 100 PDN cases (the higher the better).

| Method               | Method Type     | PI Simulations/Inference (M) | Avg. Score |
|----------------------|-----------------|-----------------------------|------------|
| Random Search        | Search          | 10,000                      | 12.70      |
| Genetic Algorithm    | Search          | 100                         | 12.56      |
| Genetic Algorithm    | Search          | 500                         | 12.79      |
| AM-RL [15]           | Pretrained      | 1                           | 11.71      |
| Arb-RL [16]          | Pretrained      | 1                           | 9.60       |
| AM [15]-IL {N = 2,000} | Pretrained      | 1                           | 12.06      |
| Arb [16]-IL {N = 2,000} | Pretrained      | 1                           | 10.80      |
| CDML {N = 100, P = 3} (ours) | Pretrained      | 1                           | 12.73      |
| CDML {N = 1,000, P = 3} (ours) | Pretrained      | 1                           | 12.81      |

Table 2: Ablation study on CDML components trained with $N = 100$ (the higher the better).

|                  | Validation Score | Test Score |
|------------------|------------------|------------|
| AM-IL (baseline policy) | 11.49            | 10.93      |
| + Meta Learner    | 12.28            | 12.01      |
| + Expert Distillation | 12.69            | 12.48      |
| + Expert Distillation + Self Distillation | 12.78 | 12.50 |
| + Meta Learner + Expert Distillation | 12.97 | 12.73 |
| + Meta Learner + Expert Distillation + Self Distillation (CDML) | **12.98** | **12.73** |

approaches with different architecture/learning strategies. Implementation details of baselines are provided in Appendix E.2 and Appendix E.3.

4.2 Performance Evaluation

For fair performance comparison, each method is given the same 100 PDN cases, described in Section 4.1. Performance is measured by taking the average objective value $Obj$ on the 100 PDN cases, evaluated after allocating 20 decaps ($K = 20$) on each PDN case.

Fig. 4 shows the resulting impedance suppression on one of the 100 PDN cases. The lower the impedance, the higher the objective value $Obj$. Corresponding objective values for the PDN case are 8.86 for AM-RL and 10.40 for AM-IL, 12.49 for GA{100}, 12.71 for GA{500}, 12.65 for RS{10,000}, and 12.83 for CDML. See Appendix F for more PDN cases.

As shown in Table 1, our CDML significantly outperformed all baselines in terms of average design performance. Search-based meta heuristics generally produce decap placement solutions that give a very high average performance. This is due to a large number of searching iterations $M$, which incurs the same number of PI simulations. On the other hand, the learning-based baselines and CDML do not require PI simulations to generate decap placement solutions; once trained, they only require a single PI simulation to evaluate the performance. Although the learning-based methods can easily find such a solution, CDML is the only method capable of finding a solution that outperforms the highly iterative meta-heuristic methods by a single inference.

Among the RL-based methods (AM-RL, Arb-RL) and their imitation learning versions (AM-IL and Arb-IL), RL-based methods showed poorer performance due to their inefficiency in exploring over extremely large combinatorial action space of DPP. We believe that imitation learning approach, fitting policy with expert data, saves unnecessarily massive exploration of RL, achieving higher sample efficiency and performance.

Among the imitation learning approaches, CDML showed the best sample efficiency and performance. It only requires $N = 100$ expert labels to learn a design policy that beats the policies trained by other imitation learning methods with $N = 2,000$ expert labels. We believe this performance improvement
comes from the newly devised learning schemes of CDML: (1) context-based meta-learning makes the policy easily adapt to new problems, and (2) collaborative distillation scheme with equivariant label transformation increases sample efficiency not only by the increased number of labels but also by the imposed label equivariance of the policy.

Lastly, we would like to mention one more surprising fact. The CDML policy trained with expert labels generated by the expert policy, GA\{100\}, outperformed GA\{500\}, with zero-shot transfer-ability. That is, the CDML policy trained with low-quality expert labels produced higher-quality designs. We believe this was possible because we trained a factorized form of policy that does not predict labels in a single step but produces a solution through a serial iterative roll-out process, during which a good strategy for placing decaps can be identified. In addition, collaborative distillation with equivariant label transformation has further guided the policy to learn such an effective decap placement design scheme.

4.3 Ablation Studies

We analyzed the factors contributing to CDML’s significant performance improvement and scalability with extremely high sample efficiency through ablation studies on its components. There are three main components in CDML: Meta learner, Expert Distillation (ED), and Self-Distillation (SD).

As shown in Table 2 and Fig. 5a, all three CDML components contributed to significant performance increments to the baseline AM-IL. Meta learner successfully captured the meta-features of DPP from high-quality labels and improved generalization capability. Expert distillation scheme showed the greatest performance improvement, verifying that AP-equivariance imposition through transformation greatly contributed to the performance improvement. Self-distillation scheme prevented over-fitting of training process for sparse dataset \(N = 100\). In addition, we carried out CDML component analysis on AM-RL baseline. According to Fig. 5b, even if we imposed AP-equivariance with the self-distillation scheme to AM-RL, there was not much performance improvement in comparison to AM-IL because reinforcement learning already explores wide action space.

Fig. 5c shows an ablation study on CDML trained with different number of samples \(N\). Our proposed CDML trained with \(N = 100\) outperformed the AM-IL baseline trained with \(N = 2,000\). The performance of CDML continuously improved with the increase of \(N\) while the performance of AM-IL saturated at \(N = 500\). This verifies that CDML components clearly contributed to the sample efficiency. See Appendix G.1 for numerical experimental results on \(N\) variations.

Analysis on Action-Permutation (AP)-Equivariance. We measured the AP-equivariance of our CDML and AM-IL through the loss term \(L_{\text{self}}\), Eq. (5). The AP-equivariant loss for AM-IL was \(8.70 \times 10^{-21}\) while for CDML was \(1.25 \times 10^{-28}\). The extremely lower AP-equivariant loss implies that CDML successfully imposes AP-equivariance to improve generalization capability.

Analysis on Hyperparameters \(\lambda\) and \(P\). We also carried out ablation studies on \(\lambda\) and \(P\). CDML showed the highest performance with \(\lambda = 8\) and \(P = 3\) at \(N = 100\); performance was not very sensitive to \(\lambda\) and \(P\) variations. See Appendix G.2 and Appendix G.3 for details.

4.4 Scalability Test

For scalability verification, learning-based DPP methods were trained for a fixed scale PDN, \((10 \times 10)\), and a fixed number of decaps, \(K = 20\). We evaluated the scalability of the pre-trained model by varying \(K \in \{12, 16, 20, 24, 30\}\) for \((10 \times 10)\) PDN and \(K \in \{20, 40\}\) for \((15 \times 15)\) PDN without

![Figure 5: Ablation study on CDML components](image)
Table 3: Scalability evaluations on larger PDN scale and varying number of decap $K$.

| Scale Variables | Methods       | PDN Scale | Number of Decap $K$ | GA {100} | AM [15]+IL | CDML (ours) |
|-----------------|---------------|-----------|---------------------|----------|------------|-------------|
|                 |               | 10×10     |                     |          |            |             |
|                 |               | 12        | 11.77               | 10.22    | 12.23      |             |
|                 |               | 16        | 12.25               | 11.13    | 12.60      |             |
|                 |               | 20        | 12.53               | 11.71    | 12.81      |             |
|                 |               | 24        | 12.79               | 12.20    | 12.95      |             |
|                 |               | 30        | 13.02               | 12.62    | 13.11      |             |
|                 |               | 15×15     |                     |          |            |             |
|                 |               | 20        | 7.61                | 6.23     | 8.47       |             |
|                 |               | 40        | 7.69                | 7.75     | 8.54       |             |

additional training (i.e., zero-shot). We chose two baseline methods for comparison: GA {100} and AM-IL. As shown in Table 3, our CDML outperformed GA {100} and AM-IL for all scales. Furthermore, CDML achieved greater performance with fewer decaps. Since hardware devices are mass-produced, reducing a single decap saves enormous fabrication costs.

5 Conclusion

In this paper, we proposed a collaborative distillation meta learning (CDML) framework for decap placement problem (DPP), one of the simulation intensive hardware design problems. The proposed CDML outperformed both learning-based and search-heuristic methods, showing significant sample efficiency in both training and inference phases. The learned policy constructed by CDML can generate a high-quality decap placement design considering power integrity (PI) without massive simulations; generalization capability allows high-quality design with a zero-shot inference.

We expect CDML would have two major influences. First, our method can be applied to other simulation-intensive placement tasks. Second, the learned policy from CDML can be used for multi-objective optimization of simulation intensive hardware design flow.

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A Extended Related Works

Machine Learning for Hardware Design Many studies have already shown that ML is applicable to various tasks in modern chip design; chip placement [27, 3, 28], floor planning [29], routing [30, 31], layout design [32], logic synthesis [7, 8], circuit design [33, 34], physical design [35], fabrication optimization [36, 37], chip test [38, 39] and bi-level optimization of placement and routing [9]. Most hardware design optimization with ML used simplified formula-table objective function for fast training of deep neural network (DNN). Because simplified formula-table objective function cannot reflect electrical performance in practical point of view, these methods are limited for industrial applications.

Among ML-based hardware design methods, Google’s deep reinforcement learning (DRL)-based chip placement method [2] has gained a considerable attention. Their method is applied to the real-world TPU design. They used graph convolutional network (GCN) [40] as the policy network and trained the GCN with proximal policy optimization (PPO) [41]. However, their study only consider simplified objective function, which is a linear combination of wire-length and congestion. Although their simplified objective function may reflect power consumption, their objective function cannot guarantee the actual electrical performance, which must be computed through intensive simulations. On the other hand, We devised a learning framework specifically designed for simulation-intensive hardware design problems, which can deal with simulation-intensive objective functions for practical use.

Moreover, while Google’s use of transfer learning allowed fast adaptation to new tasks, their method still needs massive additional fine-tuning process. The massive additional fine-tuning process is not applicable in the simulation-intensive hardware design problems. On the other hand, our proposed context-based meta learning scheme can overcome such limitation of transfer learning scheme as our method does not require additional fine-tuning for new tasks; our method shows zero-shot transfer-ability.

Genetic Algorithm-based Methods for DPP. Genetic algorithm (GA) has long been a popular method to solve decap placement problem (DPP) since the 1990s because GA is easily implementable. Despite GA being capable of narrowing down the solution space and effectively finding near-optimal solutions, its performance highly depends on the number of iterations for each given problem. Thus, most works achieved high performance in the devised problems only but did not quantitatively evaluated sample-efficiency. Most of the previous GA-based DPP works [11, 13, 14] have contributions regarding the objective function rather than the method itself. [12] proposed a GA method that finds the placement of decaps with minimum number that meets an arbitrary target impedance. However, [12] did not mention specific genetic operators such as the size of population, number of generations, mutation method, elitism method. Since GA involves iterations whenever the problem changes, any GA can find a solution with respect to an arbitrary target impedance just by modifying the objective function.

Machine Learning-based Methods for DPP. Among various machine learning (ML)-based methods, [16] first defined the DPP as a combinatorial optimization problem and proposed a DRL-based method. [16] implemented the pointer network [23], a promising neural combinatorial optimization (NCO) model, to construct a reusable DPP solver but showed poor generalization capability and required sampling of the pre-trained policy to achieve sufficient performance. [15] then implemented another representative NCO model, the attention model (AM) [19] that has the better generalization capability using the transformer [24], to solve DPP. However, the context embedding of AM could not fully capture the meta-feature of DPP as it was originally devised for TSP-variant problems.
B Domain Details and Electrical Modeling of PDN and Decap

This section provides domain details on power distribution network and role of decoupling capacitors as well as electrical modeling details of the PDN and decap used for verification. Note that these electrical models can be substituted by those of your interest.

Decap placement problem (DPP) is a simulation intensive hardware design problem. There are two methods to extract PDN and decap models that are also used for objective evaluation; 3D EM simulation tool, circuit simulation tool. For each method, there exists a trade-off between time complexity and accuracy. Table 4 provides time complexity of each method for simulating \{10 \times 10\} PDN over 201 frequency points. Time taken increases by a square of the size of PDN unit-cells and by the number of frequency points. Simulation time was evaluated using the same PDN model on Intel i7.

Table 4: Time Taken for an Objective Evaluation of a PDN model described in Appendix B.2

| Simulation Method                  | Time Taken |
|-----------------------------------|------------|
| HFSS 3D EM Simulation Tool        | \approx 10 hours |
| Ansys ADS Circuit Simulation Tool | 23.58 sec  |

B.1 Domain Details of PDN and Decap

The development of AI has led to an increased demand for high-performance computing systems. High-performance computing systems not only require precise design of hardware chips such as CPU, GPU and DRAM, but also require stable delivery of power to the operating integrated circuits. Power delivery has become a huge technical bottleneck of hardware devices due to the continuously decreasing supply voltage margin along with the technology shrink of CMOS transistors [10].

![Hierarchical power distribution network (PDN).](image)

![Electrical circuit model of the hierarchical PDN in (a).](image)

![Water supply chain from the source to households.](image)

Figure 6: Hierarchical power distribution network (PDN) and its analogy to water supply chain

Fig. 6 (a) shows the power distribution network (PDN) consisting of all the power/ground planes from the voltage source to operating chips. Power is generated in VRM and delivered through electrical
interconnections of PCB, package and chip. Finding ways to meet the desired voltage and current from the power source to destinations along the PDN is detrimental because failure in achieving power integrity (PI) leads to various reliability problems such as incorrect switching of transistors, crosstalk from neighboring signals, and timing margin errors [42]. Decoupling capacitors (decaps) placed on the PDN allows the reliable power supply to the operating chips, thus improving the power integrity of hardware. As shown in Fig. 6 (b)-(c), the role of decap is analogous to that of water storage tanks, placed along the city, apartment, and household, that can provide water uninterruptedly and reliably. As if placing more water tanks can make the water supply more stable, placing more decaps can make power supply more reliable. However, because adding more decaps requires more space and is costly, optimally placement of decaps is important in terms of PI and cost/space-saving.

B.2 PDN and Decap Models for Verification

Unit-Cell Segmentation Method [17] is a simple and fast way to generate approximated electrical models of PDN. Because the analysis of the full electrical model using EM simulation is very time-consuming, we divided the full PDN model into smaller unit-cells and constructed the full PDN model using the unit-cell segmentation method. For fast simulation, we used equation-based python implemented segmentation method, illustrated in Fig. 7.

Figure 7: Segmentation Method Implemented for PDN Generation and Decap Placement on PDN.

Segmentation method was used for generation of PDN model consisting of a chip layer and a package layer for verification as illustrated in Fig. 7 (a). The segmentation method was also used for objective evaluation of DPP. When a solution for DPP is made, decaps are placed on the corresponding ports on PDN using the segmentation method as illustrated in Fig. 7 (b).

The PDN model we used for verification has a two-layer structure; a package layer at the bottom and a chip layer on top of it as illustrated in Fig. 8. The PDN was modeled through the unit-cell segmentation method. Package layer was composed of \{40 \times 40\} package unit-cells and chip layer was composed of \{10 \times 10\} (i.e, \(N_{row} \times N_{col}\) chip unit-cells. Because the DPP benchmark places
MOS type decaps, which are placed on chip, ports are only available on chip. Thus, we extracted \(10 \times 10\) ports information from the chip layer. See Fig. 11 (a), illustrating the chip PDN divided into \(10 \times 10\) units and each unit-cell numbered.

![Top-View of PDN model.](image1)

![Side-View of PDN model.](image2)

Figure 8: Top-view and Side-view of PDN Model used for Verification

The electrical models of package and chip unit-cells that are used to build the PDN model for verification are described in Fig. 9. The chip layer is composed of \(10 \times 10\) unit-cells, and the package layer is composed of \(40 \times 40\) unit-cells using the segmentation method. The corresponding values of electrical parameters are listed in Table 5.

![Balanced Transmission Line Model of Chip Unit-Cell.](image3)

![Balanced Transmission Line Model of Package Unit-Cell.](image4)

Figure 9: Electrical Modeling of Chip and Package Unit-Cells for PDN Model generation.

| Unit-Cell Model | W  | R   | L   | G   | C     |
|----------------|----|-----|-----|-----|-------|
| Chip           | 300 \(\mu m\) | 0.26 \(\Omega\) | 22pH | 1.2mS | 0.77pF |
| Package        | 0.5mm | 0.093 \(\Omega\) | 0.25nH | 5.4\(\mu S\) | 0.045pF |

Table 5: Width and Electrical Parameters for Chip and Package Unit-Cells used for Verification

We implemented MOS type decap for verification. Decap model and its electrical parameters are shown in Fig. 10. As mentioned in Appendix A.1 Fig. 7 (b), the solution to DPP is evaluated using the segmentation method.
B.3 Input Problem PDN and Output Decap Placement Data Structure

Each unit-cell (i.e., port) of the PDN model described in Appendix B.2 is represented as a 3D vector composed of x-coordinate, y-coordinate and a number representing port state: 1 representing keep-out region, 2 representing a probing port and 0 for the rest. Total \(10 \times 10\) (i.e, \(N_{\text{row}} \times N_{\text{col}}\)) 3D vectors represent the problem PDN. The solution to DPP is the placement of decaps. As illustrated in Fig. 11 (b), the solution is given as port numbers corresponding to each decap location.

B.4 DPP Case Generation

To generate unseen decap placement problems (DPPs) cases, \(s_0 = \{p, ko\}\), for training, test and validation, a probing index \(p\) is selected randomly from a uniform distribution of \(\{1, ..., N_{\text{row}} \times N_{\text{col}}\}\). Then keep-out region indices \(ko\) are randomly selected through the following two stages: the number of keep-out regions \(|ko|\) is randomly selected from a uniform distribution of \(0 \sim 15\). Then, a vector containing indices of keep-out ports \(ko\) is generated by random selection from the uniform distribution of \(\{1, ..., N_{\text{row}} \times N_{\text{col}}\}\). We generated 100 test problems and 100 validation problems for \(10 \times 10\) PDN and 50 test problems and 50 validation problems for \(15 \times 15\) PDN. We made sure the training, test, and validation problems do not overlap.
We used a genetic algorithm (GA) as the expert policy to collect expert guiding labels for imitation learning. GA is the most widely used search heuristic method for DPP [11, 12, 13, 14]. We devised our own GA for DPP, the objective of which is to find the placement of given number \(K\) of decaps on PDN with a probing port and 0-15 keep-out regions that best suppresses the impedance of the probing port.

**Notations.** \(M\) is the number of samples to undergo an objective evaluation to give the best solution. The value of \(M\) is defined by the size of population \(P_0\) times the number of generation \(G\). \(K\) refers to the number of decaps to be placed. \(P_{elite}\) is the number of elite population.

**Guiding Dataset.** To generate expert labels, guiding problems were generated in the same way test dataset was generated. We made sure the guiding data problems do not overlap with the test dataset problems. Also, we made sure each guiding problem does not overlap with each other. Each guiding data problem goes through the following process described in Fig. 12 to collect the corresponding expert label.

**Population and Generation.** For GA \(\{M = 100\}\) (expert policy), we fixed the size of population as \(P_0 = 20\) and the number of generation as \(G = 5\), which makes up total number of samples to be \(M = P_0 \times G = 100\). Each solution in the initial population is generated randomly. As described in Fig. 11 (b), each solution consists of \(K\) numbers, each representing a decap location on PDN. Note that each solution consists of random numbers from 0 to 99 except numbers corresponding to probing port and keep-out region locations.

Once the initial population is generated randomly, a new population is generated through elitism, crossover, and mutation. This whole process of generating a new population makes one generation; the Generation process is iterated for \(G - 1\) times.

**Elitism.** Once initial population is formulated, the entire population undergoes objective evaluation and gets sorted in order of objective value. The size of elite population is pre-defined as \(P_{elite} = 4\) for GA \(\{M = 100\}\) (expert policy). That means the top 4 solutions in the population become the elite population and are kept for the next generation.

**Crossover.** Crossover is a process by which new population candidates are generated. Each solution of the current population including the elites is divided in half. Then, as described in Fig. 13 (c), half the solutions on the left and the other half on the right go through random crossover for \(P_0\) times to generate a new population. If the elite population is available, \(P_0 - P_{elite}\) random crossover takes place so that the total population size becomes \(P_0\), including the elite population.
(a) Initial Population Generation.

(b) Elitism.

(c) Crossover.

(d) Mutation.

Figure 13: Illustration of each GA Operators used for DPP Guiding Data Generation.

**Mutation.** According to Fig. 13 (d), there may exist solutions with overlapping numbers after the random crossover. We replace the overlapping number with a randomly generated number, and we call this mutation.

**Select Best.** When $G$ is reached, the final population is evaluated by the performance metric. Then, a solution with the highest objective value becomes the final guiding solution for the given DPP.

The guiding problems and corresponding solutions generated as a result of GA are saved and used as guiding expert labels for imitation learning.
D Details of Neural Architecture Design

Our neural architecture has the AM [19] with context modification. The AM is a transformer-based encoder-decoder model designed to solve combinatorial optimization problems. We used conventional notations from transformer [24] and AM [19], including multi-head attention (MHA), feed forward (FF), query, key and value (Q, K, V). Because their terminologies are well organized, we tried to keep every notation as possible. In this paper, we focused on presenting the main differences between AM and our architecture. See [19] for detailed mechanism of AM.

D.1 Change of Notations.

There are small revisions we made from [19]. In AM, TSP nodes are presented as $x_i$, $i \in \{1, \ldots, N\}$, where $N$ refers to the number of TSP nodes. This paper uses $x_p$ for node of the probing port, $x_{1:d}$ for nodes of the keep-out regions and $x_{1:d}$ for nodes of the decap available place.

[19] denotes action as $\pi$ (for representing permutation action), but we denoted action as $a$.

In, [19], the notation, $h_i(N)$, refers to $N$ times MHA in encoder; we denoted this notation as $h$ just for readability.

There are two additional notations: $c_{(p)}$ is the probing context embedding from the probing port context network (PCN in section 3.2) and $c_{a_{t-1}}$ is the recurrent context embedding from the recurrent context network (RCN in section 3.2) for step $= t$.

![Figure 14: Overview of main difference between AM and modified version of AM.](image)

D.2 Highlight of modifications: Context Embedding.

The main difference between the AM and ours is the context embedding and is illustrated in Fig. 14. AM’s [19] context embedding is presented as follows:

$$h_{(c)} = MHA(h_{(g)}, h_{a_{t-1}}, h_{a_{t-1}})$$  \(7\)

Context embedding of AM. Since the AM was originally designed for TSP and its invariant problems, AM’s context embedding is implemented for capturing the entire graph by taking the average of all node embedding, $h_{(g)}$, state-transition with $h_{a_{t-1}}$, and final destination with $h_{a_{t-1}}$. Note that TSP is a routing problem, where it must return to the first node (i.e, destination node is first visited node).
Context embedding of AM for DPP (AM-RL [15]). [15] also used the AM for decap placement with modification of context embedding. [15] tried to add \( h^p \) to capture the location of probing port as follows:

\[
h_{(c)} = MHA(h_{(a)}, h_{a_{t-1}}, h_{p}) \tag{8}
\]

Context embedding of Ours. We observed that \( h_{(a)} \) degrades the performance of the model for DPP. DPP is different from TSP; we need a new DPP-specific context embedding strategy. Therefore, we tried to focus on the probing port more than others by proposing the PCN. We excluded \( h_{(a)} \) and \( h_{a_{t}} \) from the context embedding and replaced them with our newly designed context embedding. Our context embedding is described as follows:

\[
h_{(c)} = MHA(c_{(p)} + c_{a_{t}}) \tag{9}
\]

\[
c_{(p)} = MLP_{PCN}(h_{p}) \tag{10}
\]

\[
c_{a_{t}} = MLP_{RCN}(h_{a_{t}}) \tag{11}
\]

Note that both \( MLP_{PCN} \) and \( MLP_{RCN} \) are two-layer perceptron models with ReLU activation, where input and output dimensions are identical \((d = 128\) in all experiments).

D.3 Calculation of Probability.

Probability calculations using \( h_{(c)} \), and \( h_{i}, i \in \{1, ..., N \times M\} \) in (11-14) are exactly identical to (5-8) in [19] except the masking mechanism in equation 13 and equation 14. Because [19] solves TSP, so they mask the previously selected actions by forcing \(-\infty\) as compatibility \( u_{(c)} \). For DPP, we mask not only the previously selected actions \( a_{1:t-1} \) but also the probing port index \( p \) and the keep-out region indices \( k_o \); it is forbidden to choose the indices in current state \( s_{t-1} = \{p, k_o, a_{1:t-1}\} \).

Query, key and value are computed by:

\[
q_{c} = W^Q h_{(c)}, k_{i} = W^K h_{i}, v_{i} = W^V h_{i} \tag{12}
\]

Note that \( W^Q, W^K \) and \( W^V \) are 128-to-128 linear projections.

After that, compatibility \( u_{(c)} \) is computed by the dot product of query and key, with masking mechanism (setting \(-\infty\) not to select actions in \( s_{t-1} \)).

\[
u_{(c)j} = \begin{cases} 
\frac{q_{c}^T k_{j}}{\sqrt{128}} & \text{if } j \notin s_{t-1} \\
-\infty & \text{otherwise}
\end{cases} \tag{13}
\]

The \( \tanh \) clipping is done following [43] and [19].

\[
u_{(c)j} = \begin{cases} 
10 \cdot \tanh \left( \frac{q_{c}^T k_{j}}{\sqrt{128}} \right) & \text{if } j \notin s_{t-1} \\
-\infty & \text{otherwise}
\end{cases} \tag{14}
\]

Finally, probability can be computed using softmax function as follows:

\[
p_{\theta}(a_t = i | s_{t-1}) = \frac{e^{u_{(c)i}}}{\sum_{j} e^{u_{(c)j}}} \tag{15}
\]
E Detailed Experimental Settings

E.1 Training Hyperparameters.

There are several hyperparameters for training; we tried to fix the hyperparameters as [19] did for showing their frameworks’ practicality. We then provided several ablation studies on each hyperparameter to analyze how each component contributes to performance improvement.

Training hyperparameters are set to be identical to those presented in AM for TSP [19] except learning rate, unsupervised regularization rate $\lambda$, the number of expert data $N$, number of action permutation transformed data per expert data $P$ and batch size $B$.

| Hyperparameter | Value     |
|----------------|-----------|
| learning rate  | 0.0001    |
| $\lambda$     | $8 \times 10^{-2}$ |
| $N$            | 1000      |
| $P$            | 3         |
| $B$            | 1000      |

Table 6: Hyperparameter setting for training model.

E.2 Implementation of ML Baselines.

There are two main ML baselines, Arb-RL [16] and AM-RL [15].

**Arb-RL.** Arb-RL is a PointerNet-based DPP solver proposed by [16]. However, reproducible source code was not available. Therefore, we implemented the Arb-RL following the implementation of [43] and paper of [16]. We set the training step 1,600 with batchsize $B = 100$ that makes total 160,000 PI simulation.

**Arb-IL.** Arb-IL is an imitation learning version of Arb-RL trained by our training data. We set $N = 2000$, $B = 1000$ for training Arb-IL.

**AM-RL.** AM-RL is a AM-based DPP solver proposed by [15]. We reproduced AM-RL by following implementation of [19] and paper of [15]. We set the training step 1,600 with batchsize $B = 100$ that makes total 160,000 PI simulation.

**AM-IL.** AM-IL is an imitation learning version of AM-RL trained by our training data. For experiments in Table 1, we set $N = 2000$ and $B = 1000$ for training. For ablation study, we mainly ablate $N$, when $N = 100$ we set $B = 100$. Here is the training sample complexity (the number of PI simulations during training) of each ML baselines and CDML:

| Methods          | The Number of PI simulations for Training |
|------------------|------------------------------------------|
| Arb-RL           | 160,000                                  |
| AM-RL            | 160,000                                  |
| Arb-IL ($N = 2000$) | 200,000 ($N = 2000$, $M = 100$ from GA expert) |
| AM-IL ($N = 2000$) | 200,000 ($N = 2000$, $M = 100$ from GA expert) |
| CDML ($N = 100$) (ours) | 10,000 ($N = 100$, $M = 100$ from GA expert) |
| CDML ($N = 1000$) (ours) | 100,000 ($N = 1000$, $M = 100$ from GA expert) |

During the inference phase, each learned model produces a greedy solution from their policy (i.e., $M = 1$) following [19].

---

1 https://github.com/pemami4911/neural-combinatorial-rl-pytorch

2 https://github.com/wouterkool/attention-learn-to-route
E.3 Implementation of Meta-Heuristic Baselines.

**Genetic Algorithm (GA).** GA \( \{M = 100\} \) and GA \( \{M = 500\} \) are implemented as baselines. For detailed procedures and operators used for GA, see Appendix.B. GA \( \{M = 100\} \) is the expert policy used to generate expert data for imitation learning in CDML. For GA \( \{M = 100\} \), the size of population, \( P_0 \), is 20, number of generation, \( G \), is 5 and elite population, \( P_{elite} \), is 4. For GA \( \{M = 500\} \), \( P_0 \) is 50, \( G \) is 10 and \( P_{elite} \) is 10.

**Random Search (RS).** The random search method generates \( M \) random samples for a given problem and selects the best sample with the highest objective value.

![Figure 15: Performance of GA and RS with varying number of iterations (M) in comparison to CDML at M = 1.](image)

Fig. 15 shows the performance of GA and RS depending on the number of iterations (\( M \)). The performance was measured by taking the average of 100 test data solved by each method at each \( M \). GA outperformed RS at every \( M \), and the performance increased with increasing \( M \) for both methods. However, the gradient of performance increment decreased with increasing \( M \). On the other hand, our CDML showed higher performance than GA \( \{M = 100\} \) and RS \( \{M = 10,000\} \) with a single inference \( M = 1 \).
Extended Experimental Results

The objective of DPP is to suppress impedance of the probing port as much as possible over a specified frequency range and is measured by the objective metric, \( \text{Obj} := \sum_{f \in F} (Z_{\text{initial}}(f) - Z_{\text{final}}(f)) \cdot \frac{1}{{10^3}} \). Performance of CDML was evaluated in comparison to GA \( \{ M = 100 \} \) (expert policy), GA \( \{ M = 500 \} \), RS \( \{ M = 10,000 \} \), AM-RL and AM-IL on unseen 100 PDN cases. Each method was asked to place 20 decaps \( (K = 20) \) on each test.

### F.1 Impedance Suppression Plots

Figure 16: Impedance suppressed by each method, GA \( \{ M = 100 \} \) (expert policy), GA \( \{ M = 500 \} \), RS \( \{ M = 10,000 \} \), AM-RL, AM-IL and CDML (Ours) for 6 example PDN cases out of 100 test dataset. (The lower the better.)
F.2 Decap Placement Tendency Analysis

Figure 17: Corresponding decap placement solutions to Fig. 16 by each method. Red represents probing port, black represents keep-out ports and blue represents decap locations.

Fig. 17 shows the decap placement solutions of 6 PDN cases plotted in Fig. 16. The solutions by the search-heuristic methods, GA and RS, tend to be scattered while the solutions by learning-based methods, AM-RL, AM-IL and CDML, are clustered. Since search-heuristic methods are based on
random generations, they do not show clear tendency. On the other hand, learning based methods are based on a policy so that they have distinct tendency in placing decaps.

The role of placing decaps in hardware design is to decouple loop inductance of PDN. In terms of PI, analysis of loop inductance is critical, but at the same time, is complex [44]. The loop inductance distribution of PDN highly depends on various design parameters such as the location of probing port, spacing between power/ground, size of PDN, and hierarchical layout of PDN [45]. When human experts place decaps on PDN, there are too many domain rules to consider. On the other hand, CDML understands the PDN structure and its electrical properties by data-driven learning. According to Fig. 17, CDML tends to place decaps near the probing port, which is a well-known expert rule in the PI domain.
G  Further Ablation Studies

This section reports ablation studies on action permutation invariance and hyperparameters $N$ (number of guiding samples), $\lambda$ (weight of self-distillation loss term), and $P$ (number of permutation transformed labels).

G.1  Ablation Study on $N$

$N$ is the number of expert labels generated by the expert policy, GA $\{M = 100\}$. We ablate $N \in \{100, 500, 1000, 2000\}$ with fixed $P = 3$ and $\lambda = 8$ and compare to AM-IL baseline for all $N$. As shown in Table 8, CDML with $N = 2000$ gives the best performance and CDML outperforms AM-IL for all $N$ variations. Performance of AM-IL is saturated at $N > 500$ while the performance of CDML continuously increases with the increase of $N$.

| Validation Score |
|-------------------|
| AM-IL ($N = 100$) | 11.60 |
| CDML (ours) ($N = 100$) | 12.98 |
| AM-IL ($N = 500$) | 12.37 |
| CDML (ours) ($N = 500$) | 12.99 |
| AM-IL ($N = 1000$) | 12.23 |
| CDML (ours) ($N = 1000$) | 13.09 |
| AM-IL ($N = 2000$) | 12.32 |
| CDML (ours) ($N = 2000$) | 13.13 |
G.2 Ablation Study on $\lambda$

$\lambda$ refers to the weight of self-distillation loss term $L_{Self}$, in the collaborative learning loss $\mathcal{L} := \mathcal{L}_{Expert} + \lambda L_{Self}$. To set $\lambda \times L_U$ be $0.1 \sim 1$, we first multiplied $10^{32}$ to $\lambda$ because the probability of a specific solution is extremely small. Then, we ablated for $\lambda \in \{1, 2, 4, 6, 7, 8, 9, 10\}$ ($10^{32}$ is omitted) with fixed $N = 100$ and $P = 3$. For every $\lambda$, it prevents overfitting of the model in comparison to the baselines trained only with $L_{Expert}$ (see Fig. 18). According to the Table 10, $\lambda = 8$ gives the best validation scores.

| $\lambda \times 10^{32}$ | Validation Score |
|-------------------------|------------------|
| 1                       | 12.96            |
| 2                       | 12.96            |
| 4                       | 12.94            |
| 6                       | 12.96            |
| 7                       | 12.98            |
| 8                       | 12.98            |
| 9                       | 12.97            |
| 10                      | 12.96            |

Only IL, $\lambda = 0$ 12.97

Figure 18: Validation graph of $\lambda \in \{1, 2, 4, 6, 7, 8, 9, 10\}$ on fixed $P = 3$ and $N = 100$. 
G.3 Ablation Study on $P$

$P$ is the number of permutation transformed labels per each expert label used for expert distillation imitation learning. We ablate $P \in \{3, 5, 7\}$ with fixed $N = 100$ and $\lambda = 8$ and compared collaborative distillation (i.e., both expert and self-distillation) to only expert distillation training case. As shown in Table 10, $P = 3$ with \{Expert distillation + Self-distillation\} give best performances. For every $P$, \{Expert distillation + Self-distillation \} gives the better performances, indicating self-distillation scheme well prevents overfitting of training process for sparse dataset.

Table 10: Ablation study on $P$ with and without unsupervised loss term.

| Validation Score | Expert distillation \{$P = 3$\} | 12.97 |
|------------------|--------------------------------|-------|
|                  | + Self-distillation \{$\lambda = 8$\} | \textbf{12.98} |
| Expert distillation \{$P = 5$\} | 12.95 |
|                  | + Self-distillation \{$\lambda = 8$\} | \textbf{12.95} |
| Expert distillation \{$P = 7$\} | 12.93 |
|                  | + Self-distillation \{$\lambda = 8$\} | \textbf{12.95} |

Figure 19: Validation score of $P$ ablation with and without Unsupervised Loss term.