Asynchronous Memory Access Unit for General Purpose Processors

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ABSTRACT
In future data centers, applications will make heavy use of far memory (including disaggregated memory pools and NVM). The access latency of far memory is more widely distributed than that of local memory accesses. This makes the efficiency of traditional blocking load/store in most general-purpose processors decrease in this scenario. Therefore, this work proposes an in-core asynchronous memory access unit.

1. INTRODUCTION
In recent years, more and more technologies aimed at improving the utilization of resources in cloud data centers have been proposed. More and more resources are organized into resources pool. Memory resources may be the next resources organized as a pool. Memory resources pool is similar to an old idea: distributed shared memory. However, the application of this idea at that time was limited due to the huge gap between network and memory in delay and bandwidth. At present, with the rapid development of network technology, these ideas are becoming increasingly attractive. However, nowadays the remote memory systems usually provide software interfaces (such as key-value, RDMA, files, etc) rather than load/store [1].

Recently, new interconnect technologies and protocols (such as OpenCAPI, Gen-Z, CXL, etc) enable the construction of load/store interface disaggregated memory pool that contains multiple nodes. Prototypes of such systems have already been constructed by researchers [4]. It is foreseeable that complex disaggregated memory pools using load/store interface may emerge. However, the load/store interfaces are still not efficient enough.

On the other hand, Non-volatile Main Memory(NVMM) is starting to emerge, offering higher memory density and lower standby power consumption. However, it faces similar challenges as remote memory systems. Compared to traditional DRAM, NVMM has high latency and a wide range of latency variation (6x-30x higher write latency and 5x-10x higher read latency) [3]. Currently, there is not an efficient access interface for accessing NVM. Commercial products, such as Intel’s Optane DC, still provide a synchronous load/store interface. There is no mechanism provided for reacting to memory latency variation.

There are two main differences in accessing far memory compared to accessing traditional local memory.

Widely distributed latency The memory allocated from a disaggregate memory pool may locate on some faraway remote nodes. Furthermore, applications may use memory from DRAM, NVM, or other emerging memory devices. As a result, access latency becomes uncertain. Latency may distribute over a wide range.

Potential large aggregated bandwidth As memory may come from multiple different machines, the aggregated bandwidth can increase significantly compared to local memory, making it a challenge of how to make use of the abundant bandwidth.

Access latency in traditional memory systems is also uncertain because of the multi-level cache hierarchy. However, the distribution of latency is relatively limited. The latency of a single access memory request is around 1ns (when L1 hits) to 200ns (when accesses local DRAM). Modern processors can tolerate this difference in latency by out-of-order execution and non-blocking cache. Fig 1 shows the limitations of current Out-of-Order processors in far memory scenarios. The range of latency they can tolerate is restricted by the number of entries in the instruction queue, ROB, and MSHRs. Once one of these resources is exhausted, the OoO processor cannot issue any more memory access requests. Moreover, once a long latency memory access instruction locates at the head of ROB, critical resources(such as ROB, IQ, etc.) will be occupied by it for a long time, which will cause degradation of the performance. Thus, it is difficult for modern processors to cope with the latency fluctuations (300ns-10us) caused by accessing far memory.

Although improving the out-of-order execution capability of traditional general-purpose processor cores (e.g., increasing the number of entries of MSHRs and ROB, using multi-level MSHRs and ROB, etc.) can also improve the performance of load/store in this scenario. But from such an improvement, even if it is feasible, it requires significant hardware resources. Another way is to use prefetching and multi-threading/coroutines techniques to hide access latency. However, the effectiveness of this approach is limited by the unavailability of observing access latency. In summary, the existing techniques have limited performance improvements for accessing far memory.

One approach to address this problem is asynchronous memory accessing. A similar predicament has already existed in network programming, where applications call blocking
2. ASYNCHRONOUS MEMORY ACCESS UNIT

Asynchronous Memory access Unit is inspired by the Vector Processing Unit (VPU) of modern processors. The VPU is a separate functional unit in the CPU. Applications use the VPU through a standalone instruction set, which contains a set of extra registers (i.e., vector registers) to hold the wide data to be processed. Besides, vector instructions are scheduled together with scalar instructions. Vector registers and scalar registers can exchange data efficiently.

Similarly, several asynchronous memory access instructions are designed for using AMU. The instruction that invokes a request can immediately be committed, once AMU receives the request. Thus, applications can continue to execute other operations rather than wait for memory access instructions to finish. Then, applications can poll whether there is a completed request.

Furthermore, each processor core is equipped with a Scratch-Pad Memory (SPM), which acts like vector registers in a vector instruction set. The reason for using SPM instead of register files is that the capacity and granularity of register files are limited. Therefore, SPMs are needed to hold the data for asynchronous memory accesses.

Data is moved asynchronously between SPM and memory by AMU. To initiate asynchronous memory access requests, applications can write several configuration registers, executing asynchronous memory access instructions. After receiving the request, AMU will move the data between memory and SPM in background.

For an application, the SPM is private memory space. Applications can use load/store instructions to load the data in the SPM into registers and process them with regular instructions. In addition, applications can copy data from local memory to the SPM and vice versa. The SPM is fully compatible with the processor's original data access and processing mechanisms.

2.1 Instructions

There are three core instructions of AMU. These instructions enable the most basic asynchronous memory access.

Asynchronous load/store instructions: In AMU, a load/store instruction invokes a data movement request between SPM and memory. These two instructions have three operands (aload astore Rd, Rs1, Rs2). Operand Rs1 represents an SPM address. Rs2 represents a memory address. Memory accessing accelerator will move data between the provided SPM address and memory address. The request’s id is stored into Rd.

Instruction for getting a finished request’s id: We propose getfin for getting a completed request’s id. If there is no finished request, the instruction returns a failure code. This design does not block execution regardless of whether there is a completed request or not.

2.2 Registers

Due to the limited length of instructions, some complex access memory settings cannot be encoded in the instructions. To solve this problem, we designed several configuration registers, which contain advanced configurations.
Memory Access Configuration Register: This register contains advanced memory access configurations, including granularity, QoS labels, etc.

Default Configuration Register: Due to the limited encoding space of some instructions, it is not possible to encode all configurations. In particular, many asynchronous memory access instructions need to specify a memory access configuration register. For the case where the corresponding memory access configuration register cannot be specified in the instruction, the system automatically selects the configuration register specified in this register.

Access Pattern Register: The access pattern register is used to initiate complex asynchronous memory access. It contains the access pattern (such as stride, stream, etc.) of a complex memory access request.

In addition, some registers can be used to store software-defined configuration information. This is because, for a message interface based memory system [2], some software-defined information can be encoded in the message. These registers can increase the flexibility of the software.

2.3 Programming Model

Listing 1 shows a basic example of asynchronous memory accessing. The code initiates an asynchronous memory access request with the `aload` instruction. The code then keeps trying to execute the `getfin` instruction to get the id of a completed request and can do other work while the request is pending. After the request completes, the code then reads the data from the SPM with the `load` instruction.

Listing 1: Asynchronous Memory Access Basic Example

```c
int memory_need_to_be_accessed;
int *spm_space = (int*) A_SPM_ADDR;
// Using load to invoke an
// asynchronous memory access
// requests. The request’s id
// is ignored here.
aload(spm_space,
    &memory_need_to_be_accessed);
while ((rd = getfin()) != 0) {
    // Do something else before
    // the request is finished.
    }
// Access data from SPM via standard
// load/store instruction
printf("%d\n", *spm_space);
```

AMU instructions can support a variety of programming paradigms.

2.3.1 Vector Model

Vector instructions and vector processors are very early techniques for exploiting data-level parallelism. The SIMD instruction set, which is commonly supported in modern processors, uses a similar idea. As a technique to improve data-level parallelism, AMU instructions have many similarities in design ideas to vector instructions. Thus, it is possible to use AMU instructions for vector processing scenarios.

2.3.2 Event-Driven Model

The event-driven model is a common paradigm in single-thread non-blocking network programming. Furthermore, the `aload/astore` instructions are like non-blocking socket `read()/write()`. `getfin` instructions are like the `select()` in network programming. Thus, the event-driven model can be naturally applied to asynchronous memory accesses.

2.3.3 Coroutin model

For asynchronous access requests with complex access patterns, coroutines are a more suitable programming paradigm. Coroutines can easily work with high-performance concurrent data structures.

3. ARCHITECTURE DESIGN

Fig 2 shows the architecture design of AMU. There are three key features of the architecture design:

CPU Pipeline Integration: To support complex memory accessing scenarios, many configuration registers are integrated into CPU core’s pipeline. Some of these registers indicate the accelerator’s status, which allows programmers to rapidly gather the status of the accelerator. In addition, for the performance of asynchronous memory access instructions, the pipeline of the processor core needs to be modified to support the speculative execution of these instructions.
Reconfigurable Cache/SPM Space  AMU provides interfaces for applications to dynamically configure a part of the Cache as SPM. This design allows more flexibility for the software to decide how to use the accelerator. Applications can adjust the size of Cache and SPM themselves based on the workload.

Integrated with L2 Controller  AMU’s logic is integrated with the L2 controller. This logic implements the management and execution of asynchronous access requests and the movement between SPM and far memory.

4. FUTURE WORK

In this paper, only the basic instructions and structures are presented. However, this design can easily support more memory extensions. For example, we can add some configuration registers and instructions for issuing processing-in-memory related requests. In addition, it can combine with message-based interface memory systems [2]. It is possible to provide more configuration registers to issue memory access requests with richer semantics.

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