Merged-element transmons on Si fins: the FinMET

A. Goswami,1 A.P. McFadden,2 H.S. Inbar,3 R. Zhao,2,4 C.R.H. McRae,2,4 C.J. Palmstrøm,1,3 † and D.P. Pappas2

1 Electrical and Computer Engineering Department, University of California, Santa Barbara, Santa Barbara, CA 93106
2 National Institute of Standards and Technology, Boulder, Colorado 80305, USA
3 Materials Department, University of California, Santa Barbara, Santa Barbara, CA 93106
4 Department of Physics, University of Colorado, Boulder, Colorado 80309, USA

(Dated: September 6, 2021)

A merged-element transmon (MET) device, based on Si fins, is proposed and the steps to form such a “FinMET” are demonstrated. This new application of fin technology capitalizes on the anisotropic etch of Si(111) relative to Si(110) to define atomically flat, high aspect ratio Si tunnel barriers with epitaxial superconductor contacts on the parallel side-wall surfaces. This process circumvents the challenges associated with the growth of low-loss insulating barriers on lattice matched superconductors. By implementing low-loss, intrinsic float-zone Si as the barrier material rather than commonly used, lossy Al2O3, the FinMET is expected to overcome problems with standard transmons by (1) reducing dielectric losses; (2) minimizing the formation of two-level system spectral features; (3) exhibiting greater control over barrier thickness and qubit frequency spread, especially when combined with commercial fin fabrication and atomic-layer digital etching; (4) reducing the footprint by four orders of magnitude; and (5) allowing scalable fabrication. Here, fabrication of Si fins on Si(110) substrates with shadow-deposited Al electrodes is demonstrated. The formation of FinMET devices is expected to allow tunnel junction patterning with optical lithography. This facilitates uniform fabrication on Si wafers based on existing infrastructure for fin-based devices while simultaneously avoiding lossy amorphous dielectrics for tunnel barriers.

The invention of the transmon qubit has fueled the rapid development of quantum-information research over the past decade [1], and landmark breakthroughs have been achieved with this technology [2]. Modern transmons are typically based on some variant of a small, thermally oxidized Al/AlOx/Al tunnel junction in parallel with a large shunt capacitor. A variety of methods exist for defining the Josephson junctions (JJs) to obtain a nonlinear inductance, such as Dolan bridges [3], the Manhattan shadow evaporation process [4], and overlap designs [5, 6]. However, these devices are difficult to scale for a couple of reasons. First, the associated shunt capacitors are typically defined as planar structures grown on a low-loss substrate. While very low-loss substrates (i.e., intrinsic, float-zone silicon (i-Si)) with loss tangent in the low 10−7 range can be obtained [7], it is well known that the interfaces and surfaces of the shunt capacitor participate significantly in the total loss [8, 9]. In general, while it has been observed that increasing the size of the shunt capacitor can dilute the high loss contributions [10], this results in very large structures, with dimensions of the order of 100s of micrometers. This is problematic for scaling up to systems with many qubits. Second, the frequency allocations of transmons using thermally oxidized aluminum have a significant spread [11]. While there have been advances on this front using post-processing, i.e. laser-annealing of individual devices [12], this remains a significant obstacle to large-scale integration of transmon. To this end, better control of the tunnel-barrier thickness and interfaces in the fabrication process is desired.

Recently, an alternative approach to scaling these circuits was demonstrated [13], i.e. the merged-element transmon (MET). The MET minimizes the transmon qubit size and radiation while providing an avenue to potentially reduce losses due to surfaces and interfaces. This design entails engineering the junction itself to satisfy the transmon requirements for frequency, anharmonicity, and charge noise by merging the external shunt capacitor and the JJ inductance into a single element. This design is constructed from a superconductor–insulator-superconductor trilayer where the insulator is made from a dielectric material that has a low barrier height, and may even be a semiconductor at room temperature. This design has several advantages over the traditional transmon. First, the MET allows a significant reduction, on the order of 104, in the device area [13]. Second, the resulting small qubit

![FIG. 1. 3D schematic of the FinMET and cross-section with corresponding circuit diagram of MET (inset).](image-url)
dimensions effectively suppress unwanted radiation and qubit-qubit coupling through direct interactions or box modes. Third, the MET frequency should be less susceptible to the variation in lithography because the associated capacitive and inductive contributions toward the qubit frequency cancel out to first-order [11,13]. Moreover, one may choose a low-barrier-height material as the junction tunnel barrier. This enables the use of a relatively thick tunnel barrier that may reduce the percentage variation in junction inductance, potentially alleviating the frequency allocation problem.

The energy-level transitions of a MET device, from two-tone spectroscopy measurements confirmed that the MET is indeed operating in the transmon qubit regime [13]. Furthermore, the spectra obtained with various pumping powers were described well with a master-equation simulation. An in-depth TLS-loss analysis identified the lossy amorphous silicon tunnel barrier and surrounding interfaces as the major limiting factor for the qubit relaxation time. Coherence times in excess of 100 μs were predicted given improved fabrication and interface engineering. Subsequently, Mamin et al. (and the IBM team) demonstrated METs with coherences on up to 41 and 234 μs, respectively, using as-grown- and annealed-AlOx overlap junctions [13].

While the MET demonstration from Ref. [14] confirmed the possibility of obtaining long coherence times in selected devices, the extreme oxidation and annealing conditions resulted in significant frequency spread for the devices. This is reminiscent of conventional transmons and is most likely due to several problems. First, the tunneling critical current varies exponentially with the tunnel barrier thickness, which is difficult to control in a 2 nm thick tunnel barrier formed by thermal oxidation. In addition, there are tunneling hotspots due to the barrier being structurally and chemically inhomogeneous, resulting in only a small percentage of the 2 nm thick AlOx barrier actually contributing to the tunneling [13]. Second, the critical current can be affected by atomic-level defects in and around the barrier and wiring [16]. These can cause two-level-system spectral features that are detrimental to the operation of the devices. This illustrates the importance of developing a more robust method of defining the tunnel junction. Specifically, we note that a low barrier height, crystalline tunnel barrier can mitigate this problem because it can be thicker, making monolayer scale thickness variations less significant.

Here, we propose the concept of a FinMET device that can overcome a number of the problems discussed above. This process capitalizes on the fact that crystalline Si fins can be formed on the surface of a wafer using an anisotropic wet etch (Fig 1). These Si fins act as tunnel barriers for the MET. The fin walls can, in principle, be atomically flat, parallel, and engineered to be a very specific thickness. For amorphous-Si barriers, for example, the small band gap compared to that of AlOx results in a low tunnel-barrier height [13]. This allows the use of a relatively thick fin, on the order of 5-10 nm, leading to a natural extension of the MET to a more scalable geometry.

Proposed processes for realizing the fins and metallizing them are presented here. We demonstrate both the fabrication of high aspect ratio Si fins that are needed for loss measurements and the self-aligned process to deposit superconductors on such fins. These scalable techniques are unique in that both capacitive elements and METs can be formed from the low-loss Si substrate. In this case, it is critical to have low loss, epitaxial interfaces for the fin metallization layer. This can be achieved using careful surface cleaning and growth methods, as shown by Place, et al. [17]. Provided these conditions can be met, the fin-based devices will have parallel-plate electrodes that can be optically defined, fabricated with standard processing techniques, and capacitively coupled through the low-loss substrate in order to form cells for VLSI circuits.

Based on the modeling from Ref. [13], the optimal dimensions for the FinMET will require Si fin structures on the order of 5-10 nm thick with areas of approximately 10 μm². Structures of such extreme aspect ratios are on the cutting edge of modern fin technologies [18].

The FinMET devices are comprised of a Si fin [18,19] with superconducting electrodes grown on both the surfaces of the fin, effectively forming a horizontal superconductor-semiconductor-superconductor junction, as illustrated in Fig. 1. The Si fin is formed by top-down etching of a commercial intrinsic Si substrate, which are commonly grown using float-zone technique and exhibit high resistance and low loss. To achieve atomically flat surfaces, we start with a Si(110) substrate and use anisotropic wet etching to fabricate Si fins with smooth (111) surfaces. For the anisotropic wet etch, a SiNx hard mask is used. The SiNx layer is deposited using a low-
pressure chemical vapor deposition technique which results in a high density, low stress nitride layer on top of the silicon substrate. This mask is lithographically defined using electron beam lithography (EBL) and plasma based dry etching. Alternatively, there exist methods based on SiNx deposited on step edges \[20\] that can form SiNx masks with similar dimensions using only photolithography.

The wet etch is performed using potassium hydroxide (KOH) or tetramethyl ammonium hydroxide (TMAH) at elevated temperatures. Figure 2 shows fin structures defined on a Si(110) substrate. Further thinning of the fins can then be achieved, if necessary, by timing an additional wet etch and/or subsequent atomic-layer-digital-etching (ALE). The ALE process is typically achieved by oxidizing the Si(111) surface using O\(_2\) plasma at room temperature to form an oxide layer that is approximately 5-7nm thick. This oxide can then be etched away using HF and the process repeated to achieve the desired fin thickness. The second envisioned process to thin the fin involves using atomic layer etching with a O\(_2\), HF, and Al(CH\(_3\))\(_3\) chemistry \[21\]. A final wet etch in KOH can then be used to regain the smooth Si(111) surface followed by a HF dip to remove any oxides, prior to Al metal deposition.

By using the intrinsically parallel crystallographic \{111\} faces that are exposed by the anisotropic etch, the tunnel junction can be expected to have well-defined, homogeneous tunneling currents. In addition, the low-tunnel-barrier-height material can be much thicker than standard junction material and thus mass-fabricated with better margins. Metallization of the fins can be accomplished by cleaning the exposed \{111\} faces and then epitaxially growing a a superconducting metal, such as Al. Prior to Al growth, an HF etch followed by high temperature annealing of the Si fin is expected to result in a pristine interface, thus optimizing coherence. Additionally, since the bottom edge is surrounded by low-loss substrate a reduced participation of the Al-air exposed interface is expected.

We envision two different process flows, either self-aligned or planarized, as illustrated in Fig. 3. Both processes start by etching Si fins as described previously, using a SiNx hard mask and a combination of dry and wet etches.

The first process flow involves retention of the SiNx hard mask that was initially used to etch down the Si fins. Using the overhang in the SiNx on top of the fin, an angled deposition of aluminum can lead to a break in the metal layer at the top of the fin. This shadow-evaporation technique therefore enables direct creation of a fin capacitor using a self-aligned process. This eliminates the need to etch off Al from the top of the fin to electrically disconnect the pads on either side of the fin (Fig. 3A). Contact pads can then be patterned using optical lithography. It should be noted here that, prior to Al deposition, the SiNx is selectively wet etched on other parts of the sample (excluding the SiNx on top of the fin) to reveal the clean, intrinsic silicon for fabricating feedlines and RF circuitry.

The second possible process flow, planarization, (Fig. 3B) involves removing the SiNx hard mask and then depositing a layer of aluminum onto the fins. Back-etching of a subsequent resist layer, either by dry etching or chemical mechanical polishing (CMP), can thereafter be used to expose the metal at the top of the fin and a wet or dry etch is used to remove the top aluminum. Contact pads would then be patterned in a way similar to the previous process flow. Figure 4 shows fin structures coated with Al, as described below. In this work, we employed the first, self-aligned method. Fins were fabricated according the the above recipe and the Al was shadow deposited with an effusion cell in a molecular beam epitaxy chamber. The substrate temperature was maintained close to 0 °C (Fig. 4 A-F). Smoother Al films can be grown by performing the deposition in a cryogenic cold stage maintained at -196 °C following a process similar to Ref. \[22\]\[25\]. Connection to other parts of the circuit, for

\[3\]
\[\text{SiN}_x\]
\[\text{Al}\]
\[\text{Si}\]
\[\text{PR}\]

FIG. 3. Schematics of (A) self-aligned process and (B) planarization process.
FIG. 4. Metallized fin structure illustrating the self-aligned process and growth of Al on the Si{111} surfaces with a SiN\(_x\) hard mask. (A) side view of the fin, (B) shows zoomed in area of (A) with the SiN\(_x\) hard mask on top of the fin, extending out to the left, (C) shows a zoomed in area of (B) with the area where the Al is shadowed. (D) High angle dark field scanning transmission electron microscopy image of a fin cross-section with SiN\(_x\) hard mask and shadow deposited Al. (E) and (F) shows energy-dispersive x-ray scans highlighting the Al and Si areas respectively (G) illustrates a metallized fin in a Si trench and Nb superconductor wiring connecting the top of the substrate, down a flat, \{111\} face, to the skirts of the evaporated Al at the bottom of the Si trench. (H) a zoomed up SEM image of the \{111\} face (white box in (G)).

example Nb resonators and wiring, can be accomplished using the Al pads on the sides of the fins using standard processing techniques, with Nb connecting to the Al pads at the bottom of the fin trench (Fig 4G). However, the step between the un-etched Si(110) surface and the bottom of the trench is the same as the height of the fins (> 1µm), much thicker than the metallization layers. To ensure the continuity of the wiring as it crosses this large topography, the side walls around the fin should be oriented in specific crystallographic axes (Fig 4G-H) in order to provide a continuous, smooth surface connecting the top surface and the trench.

The use of amorphous-AlO\(_x\) Josephson junctions for quantum computing transmon applications is challenged by frequency allocation, frequency stability, and loss issues. In addition, the large size of shunt capacitors required to dilute the two-level states (TLS) losses at surfaces and interfaces severely limits the scalability. However, the ease of fabrication and just-good-enough performance perpetuates this technology at present and into the near future.

In order to transition to a robust and more scalable technology, a significant effort on the front-end is required in order to bootstrap a completely new junction fabrication process and device design. To this end, we have proposed and demonstrated the primitive elements of a new FinMET technology. These include the basic wiring and structures needed to develop a more scalable system. The next steps include demonstration of low-loss capacitors and tunnel junctions. While this is feasible to demonstrate at the small scale, the importance of these developments is that it should be possible to scale up significantly by decreasing the yield variation and materials defects based on existing Si-fin infrastructure and expertise in the field.

The data that support the findings of this study are available from the corresponding author upon reasonable request.

We acknowledge the support of the NIST Quantum Initiative, the U.S. National Science Foundation (Grant No. 1839136), the new and emerging qubit science and technology (NEQST) program initiated by the US Army Research Office (ARO) under Grant No. W911NF1810114, UCSB NSF Quantum Foundry through Q-AMASE-i program award number DMR-1906325 and the U.S. Department of Energy (Grant No. de-sc0019199). We also acknowledge the use of shared facilities of the UCSB MRSEC (NSF DMR 1720256) and the Nanotech UCSB Nanofabrication facility. We thank Dustin Hite and Mike Vissers for valuable feedback on the manuscript. This material is not subject to copyright protection within the United States.

The authors have no conflicts to disclose.

[1] J. Koch, M.Y. Terri, J. Gambetta, A.A. Houck, D.I. Schuster, J. Majer, A. Blais, M.H. Devoret, S.M. Girvin, and R.J. Schoelkopf. Charge-insensitive qubit design derived from the cooper pair box. Phys. Rev. A, 76(4):042319, 2007.
[2] F. Arute, K. Arya, R. Babbush, D. Bacon, J.C. Bardin, R. Barends, R. Biswas, S. Boixo, F. GSL Brandao, D.A. Buell, et al. Quantum supremacy using a programmable superconducting processor. Nature, 574(7779):505–510, 2019.
[3] G. J. Dolan. Offset masks for lift-off photoprocessing. Applied Physics Letters, 31(5):337–339, 1977.
[4] Marius V. Costache, Germán Bridoux, Ingmar Neumann, and Sergio O. Valenzuela. Lateral metallic devices made
by a multistep shadow evaporation technique. *Journal of Vacuum Science & Technology B*, 30(4):04E105, 2012.

5. X. Wu, J.L. Long, H.S. Ku, R.E. Lake, M. Bal, and D.P. Pappas. Overlap junctions for high coherence superconducting qubits. *Appl. Phys. Lett.*, 111(3):032602, 2017.

6. Alexander Stellii, Jan David Brehm, Tim Wolz, Paul Baity, Sergey Danilin, Valentino Seferai, Hannes Roztinger, Alexey V. Usinov, and Martin Weides. Coherent superconducting qubits from a subtractive junction fabrication process. *Applied Physics Letters*, 117(12):124005, 2020.

7. W. Woods, G. Calusine, A. Melville, A. Sevi, E. Golden, D.K. Kim, D. Rosenberg, J.L. Yoder, and W.D. Oliver. Determining interface dielectric losses in superconducting coplanar-waveguide resonators. *Phys. Rev. Appl.*, 12(1):014012, 2019.

8. David S. Wisbey, Jiansong Gao, Michael R. Vissers, Fabio C. S. da Silva, Jeffrey S. Kline, Leila Vale, and David P. Pappas. Effect of metal/substrate interfaces on radio-frequency loss in superconducting coplanar waveguides. *Journal of Applied Physics*, 108(9):093918, 2010.

9. G. Calusine, A. Melville, W. Woods, R. Das, C. Stull, V. Bolkhovskiy, D. Braje, D. Hover, D.K. Kim, X. Miloshi, et al. Analysis and mitigation of interface losses in trenced superconducting coplanar waveguide resonators. *Appl. Phys. Lett.*, 112(6):062601, 2018.

10. J.M. Gambetta, C.E. Murray, Y-K-K Fung, D.T. McClure, O. Dial, W. Shanks, J.W. Sleight, and M. Steffen. Investigating surface loss effects in superconducting transmon qubits. *IEEE Trans. Appl. Supercond.*, 27(1):1–5, 2016.

11. J M Kreikebaum, K P O’Brien, A Morvan, and I Siddiqi. Improving wafer-scale josephson junction resistance variation in superconducting quantum coherent circuits. *Superconductor Science and Technology*, 33(6):06LT02, may 2020.

12. Jared Hertzberg, Eric Zhang, Sami Rosenblatt, Easwar Magesan, John Smolin, Jeng-Bang Yau, Vivekananda Adiga, Martin Sandberg, Markus Brink, Jerry Chow, and Jason Orcutt. Laser-annealing josephson junctions for yielding scaled-up superconducting quantum processors. *arXiv:2009.00781v4*, 09 2020.

13. R. Zhao, S. Park, T. Zhao, M. Bal, C.R.H. McRae, J. Long, and D.P. Pappas. Merged-element transmon. *Phys. Rev. Applied*, 14:064006, Dec 2020.

14. H. Mannin, E. Huang, S. Carnevale, Charles Rettner, N. Arellano, M. Sherwood, C. Kurter, B. Trimm, M. Sandberg, R. Shelby, Muhammad Mueed, B. Madon, A. Pushp, M. Steffen, and D. Rugar. Merged-element transmons: Design and qubit performance. *arXiv:2103.09163v1*, 03 2021.

15. L J Zeng, S Nik, T Greibe, P Krantz, C M Wilson, P Delsing, and E Olsson. Direct observation of the thickness distribution of ultra thin AlOx barriers in Al/AlOx/Al josephson junctions. *Journal of Physics D: Applied Physics*, 48(39):395308, sep 2015.

16. Steffen Schlör, Jürgen Lisenfeld, Clemens Müller, Alexander Bilmes, Andre Schneider, David P. Pappas, Alexey V. Usinov, and Martin Weides. Correlating decoherence in transmon qubits: Low frequency noise by single fluctuators. *Phys. Rev. Lett.*, 123:190502, Nov 2019.

17. A.P.M. Place, L.V.H. Rodgers, P. Mundada, B.M. Smitham, M. Fitzpatrick, Z. Leng, A. Premkumar, A Byron, J. Vrajioarea, S. Sussman, G. Cheng, T. Madhavan, H. K. Babla, X.H. Le, Y. Gang, B. Jäck, A. Gynis, N. Yao, R. J. Cava, de Leon N. P., and A.A. Houck. New material platform for superconducting transmon qubits with coherence times exceeding 0.3 milliseconds. *Nat Commun.*, 12:1779, 2021.

18. M.L. Chen, X. Sun, H. Liu, H. Wang, Q. Zhu, S. Wang, H. Du, B. Dong, J. Zhang, Y. Sun, S. Qiu, T. Alava, S. Liu, DM. Sun, and Han Z. A finet with one atomic layer channel. *Nat Commun.*, 11(1):1205, 2020.

19. Patrick S. Finnegan, Andrew E. Hollowell, Christian L. Arrington, and Amber L. Dagel. High aspect ratio anisotropic silicon etching for x-ray phase contrast imaging grating fabrication. *Materials Science in Semiconductor Processing*, 92:80–85, 2019. Material processing of optical devices and their applications.

20. V. Jovanović and L.K. Suligoj, T.and Nanver. Crystallographic silicon-etching for ultra-high aspect-ratio finfet. *ECS Trans.*, 13(3):313–320, 2008.

21. Aziz I. Abdulagatov and Steven M. George. Thermal atomic layer etching of silicon using o2, hF, and al(ch3)3 as the reactants. *Chemistry of Materials*, 30(23):8465–8475, 2018.

22. R. W. Simmonds, D. A. Hite, McDermott R., M. Steffen, K. B. Cooper, K. M. Lang, J. M. Martinis, and D.P Pappas. Josephson junction Materials Research Using Phase Qubits, chapter 11, pages 86–94. Kluwer Academic Publishers” ISBN = 13:978-0387-26332-8, 2006.

23. Brian M. McSkimming, Ashish Alexander, Margaret H. Samuels, Bruce Arey, Ilke Arslan, and Christopher J. K. Richardson. Metamorphic growth of relaxed single crystalline aluminum on silicon (111). *Journal of Vacuum Science & Technology A*, 35(2):021401, 2017.

24. L. Aballe, C. Rogero, P. Kratzer, S. Gokhale, and K. Horn. Probing interface electronic structure with over-layer quantum-well resonances: Al/Si(111). *Phys. Rev. Lett.*, 87:156801, Sep 2001.

25. Hong Liu, Y.F. Zhang, M.H. Pan, J.F. Jia, and Q.K. Xue. Two-dimensional growth of al films on si(111)-7 at low-temperature. *Surface Science*, 571(1-3):5–11, 2004.

26. F. C. S. da Silva, S. T. Halloran, L. Yuan, and D. P. Pappas. A z-component magnetoresistive sensor. *Applied Physics Letters*, 92(14):142502, 2008.