LETTER

Mitigating Multi-Cell Upsets Impacts on Approximate Network on Chip through Unequal Message Protection

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Abstract Approximate Network on Chip (NoC) is being considered as a good solution to reduce power consumption and improve the communication efficiency. However, increasing Multi-Cell Upsets (MCU) is seriously threatening the approximate NoC reliability and causes output far away from guaranteed quality of results. In this paper, we propose an unequal message protection framework with same coding length for mitigating MCU impacts on approximate NoC. The proposed framework makes good use of side information to select the special messages from normal messages and embeds same length coding scheme for all messages while providing stronger protection capability for special messages in approximate NoCs. The effectiveness of proposed methodology is evaluated by complete fault injection, which captures the dual-voltage approximate technique, unequal message protection mechanism and MCU error propagation in a joint manner. The cycle-accurate simulation using synthetic (e.g., Transpose, Uniform) and realistic benchmarks (e.g., VOPD and MWD) show that, compared with the state-of-the-art approximate NoC architecture, the proposed unequal message protection framework can achieve up to average 84.9% reliability improvement with 6.25% power consumption 6.9% area overhead, and 15.38% latency increase.

Key words: approximate communication, network on chip, multi-cell upsets, unequal message protection, dual-voltage supply

Classification: Integrated circuits (logic)

1. Introduction

The approximate computing applications like image processing, data mining, pattern recognition, can tolerate modest errors while yielding acceptable results [1, 2]. Approximate communication techniques for the approximate computing applications are receiving more research attention [3, 4]. Using these techniques, approximate Network on Chip (NoC) [5] can achieve higher performance [6, 7, 8] or lower power consumption [9, 10, 11] through actively giving up reliability degradation in chip multiprocessors (CMP). ABNoC, an approximate bufferless NoC achieves an average 83.6% retransmission reduction via decreasing transmission accuracy [6]. Dapper increases NoC throughput by up to 21% and reduces latency by up to 45.5% by using single cycle overlay circuits [7]. APPROX-NoC, a hardware data approximation framework facilitates approximate matching of data patterns and reduces data movement across the chip, up to 9% latency reduction and 60% throughput improvement [8]. DEC-NoC reduces the amount of error checking and correction in packet transmission for 58% dynamic power saving [9]. A dual-voltage approximate NoC (AxNoC) uses a per-flit look ahead power management so that headers and important data flits are transferred at a high voltage, achieving 43% power consumption with 6.2% area overhead [10]. A hardware-based quality management framework employs a configuration algorithm to continuously adjust based on the application's quality requirement, up to dynamic power consumption reduction by 59% [11]. These works focus on performance improvement or power saving via relaxing transmission accuracy actively. However, the scaling technology makes soft error dominate in the reliable NoCs [12, 13, 14, 15]. Due to the increasing error rate and complex patterns of Multi-Cell Upsets (MCU), the more and more concern on soft error also have received from the academic and industry [16, 17, 18, 19]. Particularly MCU spoils the typical Error Correction Coding (SECDED, Single Error Correction Double Errors Detection) of Virtual Channels in NoC routers [20]. Consequently, cost-effective protection is critical for approximate NoC to balance the power or performance benefits with MCU impacts well. To address this issue, we propose an unequal message protection framework with the same coding length for mitigating MCU impacts on approximate NoC. The major of this work are as follows:

1) The fault injection based evaluation of MCU impacts on dual voltage approximate NoC (AxAxNoC) with no protection motivates a cost-effective NoC architecture design.

2) An unequal message protection enhanced approximate NoC (UMP-AxNoC) is designed for mitigating MCU impacts using equal coding length with two different protection levels through using side information.

3) Comprehensive results demonstrate that the effectiveness of proposed UMP-AxNoC achieves up to 95-99% quality of result and 84.9% higher...
reliability than state-of-the-art approximate NoC architecture with 6.25% power consumption, 6.9% area cost, and 15.38% latency increase.

2. Motivation

A dual-voltage approximate NoC (AxNoC) [10] as a representative of latest approximate architectures, uses a per-flit look ahead power management so that headers and important data flits are transferred at a high voltage while the remaining flits transmission at a lower supply voltage. We use AxNoC to be the basic Approximate NoC architecture for further optimization in the paper. To evaluate the MCU impacts on AxNoC, we use fault injection method and classify the results into four cases: {masked, approx, unapprox}. MCU fault model is instanced as 48% Single Bit Upsets (SBU) and 52% MCUs from 2 bits upset to 9 bits upset caused by neutrons for SRAM in 45nm as Fig1 shows [21]. There are 9 physical patterns for 2 bits upset and 18 patterns for 3 bits upset. These varieties of faults are injected a cycle-accurate simulator for reliability assessment.

Fig.1 Fault model of neutrons for SRAM in 45nm (a) bits upset distribution. SBU is only a single bit upset while the realistic MCU, i stands for i bits upset occurring simultaneously. SBU takes up 52% while all of MCU cases share 48%. (b) physical MCU error maps for 2 and 3-bit upset. There are 9 patterns of MCU_2 and 18 patterns of MCU_3.

Fig.2 show the importance of mitigating MCU impacts on AxNoC. The synthetic benchmarks TRANSPOSE, UNIFORM are set to low approximate while the realistic benchmarks VOPD and MWD have high approximate rate 80% like streamcluster and sobel. Fig.2(a) shows TRANSPOSE, Uniform behaves high unapprox_error_rate, respectively while VOPD and MWD are 4.2% and 5.4%. All of the cases are indeed far away from high quality of result (QoR). A cost-effective protection approach is needed to mitigate MCU impacts on AxNoC.

3. Proposed UMP-AxNoC architecture

This section details UMP theory description in subsection 3.1 and UMP-AxNoC router in subsection 3.2.

3.1 Unequal message protection

UMP [22] is fundamentally different from unequal error protection, where all codewords have extra protection for specific bit positions or certain patterns [23]. UMP is an extremely useful approach when special messages are selected with regard to both the relative frequency and meaning of the stored data. For example, the fraction of top 2 frequently access instruction code with highest 6 bits equal to 0 is up to 56% while that of highest 6 bits equal to 0 data access is up to 99% [24]. The side information determines a message special or normal. UMP alternative code can sacrifice the universal double-bit protection in order to grant double-bit correction to special codewords. Therefore, UMP has potential to mitigate MCU impacts on AxNoC better than typical SECDED. A crucial property of UMP scheme is two types of messages (special and normal) have the same coding length, which is suitable for fixed bit-length virtual channels of NoC router design. A UMP based SECDED, denoted as SEC-(sm)DEC can be in favor of granting special messages double-error-correction via giving up all messages double-error-detection[25]. SEC-(sm)DEC definition and construction are as follows.

Definition 1. A SEC-(sm)DEC code is a code whose codewords are partitioned into \( M_1, M_2 \) with the following distance properties:

\[
\begin{align*}
\text{min}_{x,y \in M_1} d_H(x,y) & \geq 3, \\
\text{min}_{x \in M_1,y \in M_2} d_H(x,y) & \geq 4, \\
\text{min}_{x \in M_2,y \in M_1} d_H(x,y) & \geq 5.
\end{align*}
\]

where \( d_H \) is the hamming distance.
Parameters \((k+\log(k)+2,k)\) and logarithms are base \(2\) in the paper. E.g., 32 bits data requires 39 bits to achieve SEC-(sm)DEC. First step to SEC-(sm)DEC construction is creating 2 bits correction hamming code with parameters\((2k-1,2k-2\log(k)-3)\). The generator polynomial for the BCH code is to generate \(G_2\). And then, shorten \(G_2'\) from a \((2k-1,2k-2\log(k)-3)\times(2k-1)\) matrix to a \((k-\log(k)-1)\times(k+\log(k)+1)\) matrix \(G_2\) by removing the bottom rows and right columns. The other hand is to build \(\log(k)+1\) rows to generate \(G_1\). Finally, combine \(G_1\) with \(G_2\) for the overall generator matrix:

\[
G = \begin{bmatrix} G_1 & 1 \\ G_2 & 1 \end{bmatrix}
\]

**Theorem 1.** Let \(\mathcal{M}_2\) be the set of codewords corresponding to the set of messages that begin with \(\log(k)+1\) 0’s. Then, \(G\), from the above construction is the generator matrix for a \((k+\log(k)+2,k)\) SEC-(sm)DEC code.

The perfect match between above theory of UMP and application characteristics provides the critical base for SEC-(sm)DEC code in mitigating MCU impacts on AxNoC architecture. E.g., the mean fraction of 32bits data access beginning with 6 0’s is 86%, 89% for Axbench and SPEC CPU2006 respectively. Therefore, 32 bits flit in NoC transmission has more than 80% probability to be a special message. Consequently, we adopts SEC-(sm)DEC for approximate NoC architecture in the paper.

### 3.2 UMP-AxNoC router

Like the mainstream academic research and industry products (e.g., Intel’s SCC, Tilera’sTile64 [26]) of many-core processor, we choose a 2D Mesh wormhole switching mechanism and Virtual Channel (VC) configuration. Fig.3 gives a five-port UMP-AxNoC router in the Mesh center. Note that each dash-dotted box is duplicated five times in a complete router. Each input port in a router consists of basic VCs, a RC unit, a VCA and additional level shifter, voltage switch, power controller and encoder, while an output port includes output registers, a controller and additional level shifter, voltage switch. Each VC also has its own status registers (named VC.RC, VC.VCA and VC.Utilization) to store the results of RC, VCA allocation, and VC utilization state. The encoder and decoder are used to setup SEC-(sm)DEC unequal message protection for alleviating MCU impacts on VCs. OC (Output Controller) integrates the function of switch allocation (SA).

The extra level shifter and voltage switch modules are used to support dual voltage dynamic configuration. To manipulate the two modules, a power management controller is also required. If a flit is critical such as head flit or critical message, it will transmit in a high voltage supply. Otherwise, pull down to the low voltage for saving power. It is noted that the SEC-(sm)DEC encoder and decoder working voltage is also determined by the transmitted flit critical or not. This simplified design can reduce voltage switch frequency and save area overhead. RC and VCA are only designed for the head flit, and thus the flit type is a key point to make a decision. RC extracts the flit type information of a coming flit in VCs and determines the next-hop output port based on the corresponding destination address. Similarly, the VCA grants an available VC in the next hop from available CREDIT information. Unlike VCA, SA is used by all the flits to grant the switch. Then, the flit in an output register is transmitted to the next router through an inter-router link. Finally, repeat the above transmission process hop by hop until flits arrive at their destinations.

### 4. Experiments configuration

The diverse simulation results of five different NoC architectures {basic NoC without protection, basic NoC with SECDED[20], AxNoC without protection [10], AxNoC with SECDED, UMP-AxNoC}, are obtained from the cycle-accurate NoC simulator Nirgam [27]. To support MCU fault model evaluation and characterize the error impact quantitatively, we also implemented fault injection and plugged into Nirgam. Table I details...
of benchmarks, and parameters configuration for NoCs. To estimate power and area, we integrate the open source estimation tool Orion [28]. Table II lists the critical parameters configuration. Due to not support left shifter, voltage switch and power controller in Orion, we compared basic router area of ST28nm synthesized results 852846 µm² [10] with 45nm estimation results 58869µm² for the same NoC architecture (4 128-bit virtual channels with depth 4) in Orion and calculate the equivalent area of left shifter, voltage switch and power controller respectively. Similarly, we also compare the 28 LUTs for encoder and 83 LUTs [29] for decoder with about 1600 LUTs for a five-port router with 4 32-bit virtual channels with depth 4 [30] in Xilinx FPGA to calculate the equivalent area consumption. This can provide unified estimation of five NoC routers in Orion.

### Table I. Simulation parameters configuration in Nirgam

| Parameters | Value |
|------------|-------|
| Basic topology | 3X 4 Mesh |
| Routing algorithm | XY |
| Data/Tail flit payload size | 32 bits |
| Packet payload size | 32 bytes(cache line) |
| Packet occurring strategy | CBR(Contant Bit Rate) |
| Traffic trace | { TRANSPOSE, UNIFORM, VOPD, MWD} |
| VC Buffer size (depth) | 4 |
| VC number per port | 4 |
| Fault injection samples | 2000 |
| Each Simulation Time | 10000 cycles |
| Protection scheme | [no protection, SECDED, SEC-(sm)DEC] |

### Table II. Power and area estimation configuration in Orion

| Parameters | Value |
|------------|-------|
| Technology | 45nm |
| Voltage | 1.1, 0.7 |
| Flit width No protection of input buffer | 32 bits data |
| Flit width SECDED of input buffer | 32 bits data + 6 bits information redundancy |
| Flit width SEC-(sm)DEC of input buffer | 32 bits data + 7 bits information redundancy |
| Flit width of output buffer | 32 bits data |
| Left shifter | 134.49µm² |
| Voltage switch | 36.86µm² |
| Power management controller | 3686.42µm² |
| Encoder | 542.67µm² |
| Decoder | 1608.62µm² |

### 5. Results and analysis

This section verifies the proposed cost-effective UMP-AxNoC architecture from area cost, power consumption, performance and reliability perspectives.

#### 5.1 Area cost

Table III details the absolute and relative area cost of five different NoC architectures. Obviously, basic NoC without protection has the lowest area due to no protection and no approximate support, 11% area saving over AxNoC. This value is higher than 6.2% provided in [9]. Because, this design uses 32 bits flit instead of 128 bits flit in [9] so that the base (or divisor) becomes smaller. Particularly, 32bits flit width is selected for more specific messages (highest 6bits 0’s) in UMP-AxNoC. If 128 bits, the condition is more strict and requires highest 8 bits 0’s. Basic NoC with SECDED has the nearly same area with AxNoC protection, which shows equal overhead of single error correction and dual-voltage configuration. To alleviate MCU influencing in AxNoC, SECDED requires 6.2% extra area cost while UMP-AxNoC consumes 6.9% extra area over AxNoC. 0.7% more area overhead of proposed UMP-AxNoC mainly results from additional one bit flit width in VCs.

### Table III. Area comparison between five NoC architectures

| Configuration | basic NoC without protection | basic NoC with SECDED | AxNoC without protection | AxNoC with SECDED | UMP-AxNoC |
|---------------|-----------------------------|-----------------------|--------------------------|------------------|-----------|
| Router        | √                           | √                     | √                        | √                | √         |
| Level shifter | √                           | √                     | √                        | √                | √         |
| Voltage switch | √                           | √                     | √                        | √                | √         |
| Power controller | √                           | √                     | √                        | √                | √         |
| Encoder       | √                           | √                     | √                        | √                | √         |
| Decoder       | √                           | √                     | √                        | √                | √         |

#### 5.2 Power consumption

Fig4 shows the power consumption results of five different NoC architectures for four benchmarks. Approximate NoCs including AxNoC with protection or not achieve a lot of power saving due to low voltage configuration for approximate flits transmission over basic NoCs. This trend is more pronounced for realistic image applications because of more approximation transmission in NoCs. VOPD, MWD has a higher approximate rate 80% while TRANSPOSE, UNIFORM has a lower approximate rate 20% so that the former image processing applications have more power reduction, up to 73.6% and 76.1% over basic NoC with no protection respectively.

![Fig.4 Power comparison between five different NoC architectures](image)

Meanwhile, the extra logic units for dual-voltage configuration in AxNoC also bring extra power consumption. Therefore, the actual power reduction is lower than the approximate rate. Similar to AxNoC with
SECDED, our proposed UMP-AxNoC brings more power consumption because of extra encoder, decoder and wider flit width in VCs. UMP-AxNoC have an average 6.25% power overhead over AxNoC, still keeps the advantage of 33.51% power saving over basic NoCs.

5.3 Performance
Due to the encoder and decoder to protect router VCs against MCUs, the extra two cycles/stages are required in the fault tolerant NoCs. Table IV shows the performance comparison between five NoC architectures. The pipeline depth (D) and packet length (L) both have fixed values. Waiting time (W) between sources to destinations for each packet is varying with the packet injection rate and communication patterns. The ideal case is zero cycle waiting under a small load. The maximum latency increment of protected NoCs is equal to 15.38% (2/13). If in a heavy load, longer waiting time will further shrink the latency gap between raw AxNoC and protected UMP-AxNoC architectures. Therefore, the proposed UMP-AxNoC has more 15.38% latency than basic AxNoC for mitigating MCU impacts at most.

| Configuration | basic NoC without protection | basic NoC with SECDED | AxNoC without protection | AxNoC with SECDED | UMP-AxNoC |
|---------------|-----------------------------|-----------------------|--------------------------|-------------------|-----------|
| Pipeline depth (D) | 3 | 5 | 3 | 5 | 5 |
| Packet Length (L) | 11 | 11 | 11 | 11 | 11 |
| Waiting time (W) | ≥0 | ≥0 | ≥0 | ≥0 | ≥0 |
| Packet Latency (D+L+W-1) | 13+W | 15+W | 13+W | 15+W | 15+W |
| Normalized Packet Latency | $1 + \frac{2}{13+W}$ | $1 + \frac{2}{15+W}$ | $1 + \frac{2}{13+W}$ | $1 + \frac{2}{15+W}$ | $1 + \frac{2}{15+W}$ (≤1.15) |

5.4 Reliability
Fig 5 depicts reliability comparison between five different NoC architectures. Firstly, we can figure that approximate NoC architectures have a special error distribution approx_error_rate while basic NoCs have not. This kind of error rate is the fraction of the flit error carrying approximate data payload overall total flits, which cannot be masked or corrected during transmission. The higher approximate rate results in higher approxim_error_rate. E.g., the approxim_error_rate of TRANSPOSE is 7.38% while that of VOPD is 10.27% in AxNoC without protection.

The protection schemes also turn out to shrink the approx_error_rate and unapprox_error_rate via increasing the corrected_rate. AxNoC with SECDED reduces unapprox_error_rates to 15.9%, 14.2% from original 34.1% and 28.3% for TRANSPOSE, Uniform in Fig5(a). Similarly, the unapprox_error_rates of VOPD and MWD decreases by 44%. The stronger protection of proposed UMP-AxNoC makes unapproximate_error rates down to 0.92-4.8% and improves reliability by 84.9% over AxNoC on average, which can satisfy the acceptable 95-99% QoR well. Because the proposed UMP-AxNoC handles two bits error recovery for about 80% special flits and correct 1 bit error for the rest normal flits through SEC-(sm)DEC. In other words, the extra one bit coding in UMP-AxNoC brings 34.38% more errors recovery than AxNoC with SECDED protection. From a joint perspective, the proposed UMP-AxNoC achieves 95% QoR and improves 84.9% reliability with only 6.25% power consumption and 6.9% area cost over AxNoC. What’s the more, it has 34.38% more reliability enhancement than AxNoC with SECDED protection with only 0.685% power consumption and 0.71% area cost. All in all, the proposed UMP-AxNoC provides a cost-effective design for mitigating MCU impacts well.

![Fig.5 Reliability comparison between five different NoC architectures](image-url)

6. Conclusion
This paper proposes an unequal message protection based approximate NoC architecture to mitigate MCU impacts. It makes good use of the side information to correct two bits error in flits carrying special message with highest 6 0’s while handles with one bit error correction for the rest normal flits. This approach exploits the fine-grain reliability improvement through adding one extra bit to the typical hamming code SECDED. The cycle-accurate results show that the proposed UMP-AxNoC improves reliability by 84.9% with 6.25% power consumption, 6.9% area cost and 15.38% latency increase over state-of-the-art dual voltage AxNoC.
Acknowledgments

This work was supported by National Natural Science Foundation of China, numbered 61502298 and 71702100.

References

[1] Han J, Orshansky M. Approximate computing: An emerging paradigm for energy-efficient design[C]//2013 18th IEEE Europe Test Symposium (ETS). IEEE, 2013: 1-6,(DOI: 10.1109/ETS.2013.6569370).
[2] Xu Q, Mytkowicz T, Kim N S. Approximate computing: A survey[J]. IEEE Design & Test, 2015, 33(1): 8-22,(DOI: 10.1109/MDAT.2015.2505723).
[3] Betzel F, Khatamifard K, et al. Approximate communication: Techniques for reducing communication bottlenecks in large-scale parallel systems[J]. ACM Computing Surveys (CSUR), 2018, 51(1):1,(DOI: 10.1145/CSUR.2018.3145812).
[4] Bhamidipati P. RETUNES: Reliable and Energy-Efficient Network-on-Chip Architecture using Adaptive Routing and Approximate Communication[D]. Ohio University, 2019.
[5] Reza M F, Ampadu P. Approximate Communication Strategies for Energy-Efficient and High Performance NoC: Opportunities and Challenges[C]//Proceedings of the 2019 on Great Lakes Symposium on VLSI. ACM, 2019: 399-404,(DOI: 10.1145/ GLSVLSI.2019.3299874.3319455).
[6] Wang L, Wang X, Wang Y. An Approximate Bufferless Network-on-Chip[J]. IEEE Access, 2019, 7: 141516-141532.
[7] Raparti V Y, Pasricha S. Approximate NoC and Memory Controller Architectures for GPGPU Accelerators[J]. IEEE Transactions on Parallel and Distributed Systems, 2019,(DOI: 10.1109/ACCESS.2019.2943922).
[8] Boyapati R, Huang J, Majumder P, et al. Approx-noc: A data approximation framework for network-on-chip architectures[C]//ACM SIGARCH Computer Architecture News. ACM, 2017, 45(2): 666-677,(DOI: 10.1145/3079856.3080241).
[9] Chen Y, Reza M F, Louri A. DEC-NoC: An Approximate Framework Based on Dynamic Error Control with Applications to Energy-Efficient NoCs[C]//2018 IEEE 36th International Conference on Computer Design (ICCD). IEEE, 2018: 480-487,(DOI: 10.1109/ICCD.2018.00078).
[10] Ahmed A B, Fujiki D, Matsutani H, et al. AxNoC: Low-power approximate network-on-chips using critical-path isolation[C]//Proceedings of the Twelfth IEEE/ACM International Symposium on Networks-on-Chip. IEEE Press, 2018, 6,(DOI: 10.1109/NOCS.2018.8512158).
[11] Chen Y, Louri A. An online quality management framework for approximate communication in network-on-chips[C]//Proceedings of the ACM International Conference on Supercomputing. 2019: 217-226,(DOI: 10.1109/ICS.2019.3330245.3330265).
[12] Kim J, Park D, Nicopoulos C, et al. Design and analysis of an NoC architecture from performance, reliability and energy perspective[C]//2005 Symposium on Architectures for Networking and Communications Systems (ANCS). IEEE, 2005: 173-182.
[13] Neishaburi M H, Zilic Z. ERAVC: Enhanced reliability aware NoC router[C]//2011 12th International Symposium on Quality Electronic Design. IEEE, 2011: 1-6,(DOI: 10.1109/ISSUED.2011.5770788).
[14] Dang K N, Okuyama Y, Abdallah A B. Soft-error resilient network-on-chip for safety-critical applications[C]//2016 International Conference on IC Design and Technology (ICICDT). IEEE, 2016: 1-4,(DOI: 10.1109/ICICDT.2016.7542073).
[15] Chang Y C, Gong C S A, Chiu C T. Fault-Tolerant Mesh-Based NoC with Router-Level Redundancy[J]. Journal of Signal Processing Systems, 2019: 1-11.
[16] Gasiot G, Giot D, Roche P. Multiple cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering[J]. IEEE Transactions on Nuclear Science, 2007, 54(6): 2468-2473,(DOI: 10.1109/TNS.2007.908147).
[17] Kiani V, Reviriego P. Improving Instruction TLB Reliability with Efficient Multi-bit Soft Error Protection[J]. Microelectronics Reliability, 2019, 93: 29-38,(DOI: 10.1016/j.microrel.2018.12.011).
[18] Kato T, Yamazaki T, et al. Neutron-Induced Multiple-Cell Upsets in 20 nm Bulk SRAM: Angular Sensitivity and Impact of Multi-Well Potential Perturbation[J]. IEEE Transactions on Nuclear Science, 2019,(DOI: 10.1109/TNS.2019.2900629).
[19] Chabot A, Alouani I, Niar S, et al. A new memory reliability technique for multiple bit upsets mitigation[C]//Proceedings of the 16th ACM International Conference on Computing Frontiers. ACM, 2019: 145-152,(DOI: 10.1145/CF.2019.3310273.3321564).
[20] Jiao J, Fu Y, Wen S. Accelerated assessment of fine-grain AVF in NoC using a Multi-Cell Upsets considered fault injection[J]. Microelectronics Reliability, 2014, 54(11): 2629-2640,(DOI: 10.1016/j.microrel.2014.06.008).
[21] Alexandrescu D. A comprehensive soft error analysis methodology for SoCs/ASICs memory instances[C]//2011 IEEE 17th International On-Line Testing Symposium. IEEE, 2011: 175-176,(DOI: 10.1109/IOLTS.2011.5993833).
[22] Shkel Y Y, Tan V Y F, Draper S C. Unequal message protection: Asymptotic and non-asymptotic tradeoffs[J]. IEEE Transactions on Information Theory, 2015, 61(10): 5396-5416,(DOI: 10.1109/TIT.2015.2462846).
[23] Borade S, Nakiboglu B, Zheng L. Unequal error protection: An information-theoretic perspective[J]. IEEE Transactions on Information Theory, 2009, 55(12): 5511-5539,(DOI: 10.1109/TIT.2009.2028219).
[24] Alam I, Schoeny C, Doleck L, et al. Parity++: Lightweight error correction for last level caches[C]//2018 48th Annual IEEE/IFIP International Conference on Dependable Systems and Networks Workshops (DSN-W). IEEE, 2018: 114-120,(DOI: 10.1109/DNS- W.2018.00048).
[25] Schoeny C, Sala F, Gottschio M, et al. Context-aware resiliency: Unequal message protection for random-access memories[J]. IEEE Transactions on Information Theory, 2019,(DOI: 10.1109/TIT.2019.2918209).
[26] Bell S, Edwards B, Amann J, et al. Tile64-processor: A 64-core soc with mesh interconnect[C]//2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers. IEEE, 2008: 88-98,(DOI: 10.1109/ISSCC.2008.4523070).
[27] NIRGAM: A Simulator for NoC Interconnect Routing and Application Modeling, 2007. Available in: http://nirgam.ecs.soton.ac.uk/.
[28] Kahng A B, Lin B, Nath S. ORION3. 0: a comprehensive NoC router estimation tool[J]. IEEE Embedded Systems Letters, 2015, 7(2): 41-45,(DOI: 10.1109/LES.2015.2402197).
[29] Xilinx LogiCORE™ IP ECC core support hamming code in FPGA - ECC v2.0 Product Guide (v2.0), 2017. Available in: https://www.xilinx.com/products/ip-products/ intellectual-property/ecc.html#documentation
[30] Papamichael M K, Hoe J C. CONNECT: re-examining conventional wisdom for designing nocs in the context of FPGAs[C]//Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays. ACM, 2012: 37-46,(DOI: 10.1145/FPGA.2145694.2145703).