Computing in Memory with Spin-Transfer Torque Magnetic RAM

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Abstract—Spin-transfer torque magnetic RAM (STT-MRAM) is considered a promising candidate for future on-chip memories due to its non-volatility, density, and near-zero leakage. We explore computation-in-memory with STT-MRAM, which is a promising approach to reducing the time and energy spent on data transfers between the processor and memory subsystem, and has a potential to alleviate the well-known processor-memory gap. We show that by employing suitable modifications to peripheral circuits, STT-MRAM can be enhanced to perform arithmetic, bitwise and complex vector operations. We address a key challenge associated with these in-memory operations, i.e., computing reliably under process variations. We integrate the proposed design Spin-Transfer Torque Compute-in-Memory (STT-CiM) in a programmable processor based system by enhancing the instruction set and the on-chip bus to support compute-in-memory operations. We also present data mapping techniques to increase the efficiency of our proposed design. We evaluate STT-CiM using a device-to-architecture modeling framework, and integrate cycle-accurate models of STT-CiM with a commercial processor and on-chip bus (Nios II and Avalon from Intel). At the array level, we demonstrate that compute-in-memory operations in STT-CiM are 38% more energy efficient compared to standard STT-MRAM. Our system-level evaluation shows that STT-CiM provides improvements upto 12.4x (average of 3.83X) and upto 10.4x (average of 3.93X) in the total memory energy and system performance, respectively.

I. INTRODUCTION

The growth in data sets and increase in the number of cores place high demands on the memory subsystems of modern computing platforms. Consequently, a growing fraction of the chip transistors, area and power are utilized towards on-chip memories. CMOS memories (SRAM and embedded DRAM) have been the mainstays of on-chip memory for the past several decades. However, recent technology scaling challenges in CMOS memories, along with an increased demand for on-chip memory, have fueled an active interest in alternative on-chip memory technologies.

Spintronic memories have emerged as a promising candidate for future on-chip memories due to several desirable attributes such as non-volatility, high density, and near-zero leakage. Over the years, Spin Transfer Torque Magnetic RAM (STT-MRAM) has garnered significant interest with various prototype demonstrations and early offerings [1]–[5]. There have been several research efforts to boost the efficiency of STT-MRAM memories at the device, circuit and architectural levels [4]–[26]. In this work, we explore a complementary direction — by leveraging a unique attribute of STT-MRAMs, i.e., the resistive nature of the bit-cells, and employing novel peripheral modifications, we show that STT-MRAMs can be enhanced to perform a range of arithmetic, bitwise and complex vector operations. However, realizing these in-memory operations reliably under process variations in STT-MRAMs is quite challenging. This is due to the fact that STT-MRAMs are known for being prone to various failures [13]–[16] under process variations. In this work, we analyze the challenges posed by process variation in the context of in-memory operations and demonstrate techniques to mitigate them, thereby ensuring reliable computations.

In-memory computation is motivated by the observation that the movement of data from bit-cells in the memory to the processor and back (across the bit-lines, memory interface, and system interconnect) is a major bottleneck to performance and energy efficiency of computing systems [27].

Efforts that have explored the closer integration of logic and memory are variably referred to in the literature (logic-in-memory, compute-in-memory, processing-in-memory, etc.), and may be classified into three categories — moving logic closer to memory [28]–[40], performing computations within memory structures [41]–[47], and embedding nonvolatile storage elements within logic [48]–[50]. The first two approaches address the processor-memory gap during active computation, whereas the third addresses the challenge of efficient transition between shut down and active states.

Our proposal addresses the problem of in-memory computation with spintronic memories, to improve performance and energy efficiency without adversely impacting density or efficiency as a conventional memory. We are aware of only one other effort that addresses this challenge [43]. While [43] proposal requires the addition of a transistor to each bit-cell (resulting in a 2T-1R cell) [43], our approach differs significantly in that it requires no changes to the bit-cells and core array, enabling it to be used without sacrificing memory density. Our proposal is based on the observation that by enabling multiple wordlines simultaneously[1] and sensing the effective resistance of all the enabled bit-cells in each bit-line, it is possible to directly compute logic functions of the values stored in the bit-cells. Pinatubo [44] proposed this mechanism of enabling multiple wordlines for Non-Volatile Memories (NVMs) which is applicable to spintronic memories as well.

Note that this will lead to short circuit paths in SRAMs, but not in STT-MRAM due to the resistive nature of bit-cells.
Although our work leverages the same mechanism of enabling multiple wordlines as Pinatubo, we differ from it in several key aspects. First, unlike Pinatubo we address a key challenge of process variation associated with in-memory operations realized by enabling multiple wordlines. Second, we propose different peripheral modifications that enables us to realize operation beyond bitwise operations, i.e., arithmetic as well as complex vector operations. Our choice of peripheral modification is also a key to realizing the proposed failure mitigation mechanism for in-memory operations. Finally, unlike Pinatubo that focuses on off-chip memories, we explore architectural extensions (bus interface support and ISA extensions), and data mapping techniques to enable in-memory computation in context of on-chip memories.

In this work, we propose STT-CiM, an STT-MRAM memory with enhanced read peripheral circuits that is capable of performing a range of arithmetic, bitwise, and vector operations in memory. In STT-CiM, the core data array is the same as standard STT-MRAM, hence the density and efficiency of regular read and write operations are maintained. In order to make STT-CiM robust under process variations we embed error correction mechanisms capable of correcting errors for in-memory operations in our design. To evaluate the benefits of STT-CiM, we utilize it as a scratchpad in the memory hierarchy of the Intel Nios II [51] processor. We propose enhancements to the on-chip bus and extend the instruction set of the processor to support compute-in-memory operations and expose them to software. We also present suitable data mapping techniques to maximize the benefits of STT-CiM.

In summary, the key contributions of this work are as follows:

- We explore compute-in-memory with spintronic memories as an approach to improving system performance and energy.
- We propose STT-CiM, an enhanced STT-MRAM array that can perform a range of bitwise, arithmetic, and vector compute-in-memory operations without modifying either the bit-cells or the core data array.
- We address a key challenge in STT-CiM, i.e. reliably performing in-memory operations under process variation, by demonstrating suitable error correction mechanisms.
- We propose extensions to the instruction set and on-chip bus to integrate STT-CiM into a programmable processor system and demonstrate the viability of these extensions using Intel’s Nios II processor and Avalon on-chip bus.
- We evaluate the performance and energy benefits of STT-CiM, achieving average improvements of 3.83x (upto 12.4X) and 3.93x (upto 10.4X) in the total memory energy and system performance, respectively.

The rest of the paper is organized as follows. Section II presents an overview of prior research efforts related to in-memory computation. Section III provides the necessary background on STT-MRAM. Section IV describes the proposed STT-CiM design and how it supports compute-in-memory operations. Section V outlines the architectural optimizations and support for STT-CiM. Section VI describes the experimental methodology and the application benchmarks. Experimental results are presented in section VII. Section VIII concludes the paper.

II. RELATED WORK

Efforts related to our work can be broadly classified into three categories, as shown in Figure 1. We note that subsets of these efforts are variably referred to in the literature as logic-in-memory, processing-in-memory and computing-in-memory.

Near-memory computation refers to placing logic or processing units next to memory. It has been explored at various levels of the storage hierarchy [28]-[40]. Intelligent RAM (IRAM) [28] was an early effort that explored integration of the processor and DRAM in the same chip to improve bandwidth. Embedding simple processing units within each page of main memory [29] and within secondary storage [30] enables computations to be performed near memory. An application-specific example of near-memory computation is memory that can generate interpolated values, enabling the evaluation of complex mathematical functions [38]. Near-memory computation has gained significant interest in recent years, with industry efforts like Hybrid Memory Cube (HMC) [39] and High Bandwidth Memory (HBM) [40].

Memory-in-logic is an alternative approach that involves embedding non-volatile memory elements into a logic circuit [48]-[50]. The objective here is typically to provide non-volatility, enabling the system to efficiently transition from shut-down to active state.

In-memory computation [41]-[47] fundamentally differs from the above approaches since it integrates logic operations into the memory array itself, thereby achieving higher efficiency. Moreover, it is also complementary to the aforementioned efforts, since it does not preclude additional computations being performed near memory or non-volatile storage elements being embedded into the logic. The key challenge of in-memory computation is to realize it without impacting the desirability of the resulting design as a standard memory (i.e., density or efficiency of standard read and write operations).

We can classify previous efforts on in-memory computation based on whether they target application-specific or general-purpose computation, and based on the underlying memory technology that they consider. Application-specific examples of in-memory computation include sum-of-absolute difference [42] and dot-product [47] computation. Ternary content-addressable memory [41], ROM-embedded RAM [52], AC-DIMM [46] and Micron’s automata processor [53] can also be viewed as examples of in-memory computation that target specific operations such as pattern matching.
Unlike these application-specific designs, we focus on embedding a broader class of operations (such as ADD, AND, OR, XOR and arithmetic operations) in-memory. Pinatubo [44] and bulk bitwise in-DRAM [45] explored bitwise in-memory computations for off-chip main memory using Phase Change Memory (PCM) and DRAM, respectively. Our work differs from these efforts in several important aspects. First, we focus on in-memory computation for on-chip spintronic memory that involves a fundamentally different design space. We propose architectural extensions (bus interface support and ISA extension) and data mapping techniques to enable in-memory computations in context of on-chip memories. Second, our design is not restricted to bitwise operations and realizes arithmetic as well as complex vector operations. As compared to Pinatubo [44], we use a different sensing circuitry (consisting of 2 sense amplifiers) and reference generation circuitry which enables us to realize a wider variety of operations. Third, the proposed design requires only one array access to perform bit-wise XOR operations (unlike two in the case of [44]) and the proposed operations are not destructive to the contents stored in the accessed bit-cells (unlike [45]). Finally, unlike Pinatubo we also address a key challenge associated with in-memory computations performed by enabling multiple wordlines in NVMs, *i.e.*, performing these operations reliably under process variations. One other recent effort that addresses computing with spintronic memories [43] uses an extra transistor in each bit-cell (2T-1R cells), which sacrifices the density benefits of standard (1T-1R) STT-MRAM. In contrast, our proposal (STT-CiM) enables in-memory computation within a standard STT-MRAM array with no changes to the bit-cells. We also propose architectural support for STT-CiM and evaluate its performance and energy benefits in the context of a processor-based system.

III. BACKGROUND

![STT-MRAM bit-cell](image)

Fig. 2: STT-MRAM bit-cell

A standard STT-MRAM bit-cell consists of an access transistor and a magnetic tunnel junction (MTJ), as shown in Figure 2. An MTJ in turn consists of a pinned layer that has a fixed magnetic orientation and a free layer whose magnetic orientation can be switched, separated by a tunnelling oxide. The relative magnetic orientation of the free and pinned layers determines the resistance offered by the MTJ (the resistance for the parallel configuration, \(R_P\), is lower than the anti-parallel resistance, \(R_{AP}\)). The two resistance states encode a bit (we assume that parallel represents logic “1”, and anti-parallel represents logic “0”). A read operation is performed by applying a bias \(V_{read}\) between the bitline (BL) and the source line (SL), and enabling the wordline (WL). The resultant current flowing through the bit-cell (\(I_P\) or \(I_{AP}\)) is sensed against a global reference to determine the logic state stored in the bit-cell. A write is performed by passing a current greater than the critical switching current of the MTJ. The logic value written in the bit-cell is dependent on the direction of the write current as shown in Figure 2. The write operation in STT-MRAM is stochastic in nature, and the duration and magnitude of the write current determines the write failure rate. Apart from write failures, STT-MRAM may also be subject to read decision failures, where the value stored in a bit-cell is incorrectly read due to process variations, and read disturb failures where a read operation ends up writing into the cell. Similar to CMOS memories, these failures are addressed through a range of techniques including device and circuit optimization, manufacturing test and self-repair, and error correcting codes.

IV. STT-MRAM BASED COMPUTE-IN-MEMORY (STT-CiM)

In this section, we describe STT-MRAM based Compute-in-Memory (STT-CiM), which enhances a standard STT-MRAM array to enable in-memory computation.

A. STT-CiM overview

The key idea behind STT-CiM is to enable multiple wordlines simultaneously in an STT-MRAM array, leading to multiple bit-cells being connected to each bitline. With enhancements that we propose to the sensing and reference generation circuitry, we can directly compute logic functions of the enabled words. Note that such an operation is feasible in STT-MRAMs since the bit-cells are resistive. In contrast, enabling multiple wordlines in SRAM can lead to short-circuit paths through the memory array, flipping the logic state stored in the bit-cells.

Figure 3 explains the concept of Compute-in-Memory (CiM) operation in STT-MRAM. First, consider the resistive equivalent circuit of a single STT-MRAM bit-cell shown in Figure 3(a). \(R_t\) represents the on-resistance of the access transistor and \(R_i\) the resistance of the MTJ. When a voltage bias \(V_{read}\) is applied between the bitline and the source line (SL), the net current \(I_i\) flowing through the bit-cell can take two possible values depending on the MTJ configuration, as shown in Figure 3(b). A standard read involves using a sensing mechanism to distinguish between these two current values.

Figure 3(c) demonstrates a Compute-in-Memory (CiM) operation, where two wordlines (\(WL_i\) and \(WL_j\)) are enabled, and a voltage bias \(V_{read}\) is applied to the bitline. The resultant current flowing through the SL (denoted \(I_{SL}\)) is a summation of the currents flowing through each of the bit-cells (\(I_i\) and \(I_j\)), which in turn depends on the logic states stored in these bit-cells. The possible values of \(I_{SL}\) are shown in Figure 3(d). We propose enhanced current-based sensing mechanisms to distinguish between these values and thereby compute logic functions of the values stored in the enabled bit-cells. We discuss the details of these operations in turn below.
Bitwise OR (NOR). In order to realize logic OR and NOR operations, we use the sensing scheme shown in Figure 3(a), where $I_{SL}$ is connected to the positive input of the sense amplifier and a reference current $I_{ref-or}$ is fed to its negative input. We choose $I_{ref-or}$ to be between $I_{AP-AP}$ and $I_{AP-P}$, as shown in Figure 3(c). As a result, among the possible values of $I_{SL}$ [Figure 3(d)], only $I_{SL} = I_{AP-AP}$ is less than $I_{ref-or}$. Consequently, only the case where both bit-cells are in the AP configuration, i.e., both store “0”, leads to an output of logic “0” (“1”) at the positive (negative) output of the sense amplifier, while all other cases lead to logic “1” (“0”). Thus, the positive and negative outputs of the sense amplifier evaluate the logic OR and NOR of the values stored in the enabled bit-cells.

### Table I: Possible outputs of various sensing schemes

| $I_{SL}$ | $O_{OR}$ | $O_{NOR}$ | $O_{AND}$ | $O_{NAND}$ | $O_{XOR}$ |
|----------|----------|----------|-----------|------------|------------|
| $P_{AP}$ | 0        | 1        | 0         | 1          | 0          |
| $P_{P}$  | 1        | 0        | 1         | 0          | 1          |
| $P_{AP}$ | 1        | 0        | 1         | 0          | 1          |

### ADD Operation

An ADD operation is realized by leveraging the bitwise logical operations, as illustrated in Figure 5. Suppose $A_n$ and $B_n$ (the n-th bits of two words, $A$ and $B$) are stored in two different bit-cells of the same column within an STT-CiM array. Suppose that we wish to compute full-adder logic function (n-stage of an adder that adds words $A$ and $B$). As shown in Figure 5, $A_n$ and $B_n$ are not required individually; rather, knowing $A_n$ XOR $B_n$ and $A_n$ AND $B_n$ suffices to compute $S_n$ (the sum) and $C_n$ (the carry out) given $C_{n-1}$ (carry input from the previous stage). Note that, the sensing schemes discussed, enable us to perform the bitwise XOR and AND operations simultaneously, thereby performing an ADD operation with a single array access. Figure 5 also illustrates the computation of the ADD operation using $O_{AND}$ and $O_{XOR}$ outputs of the sense amplifiers. Three additional logic gates are connected to the outputs of the sense amplifier to enable this computation.

### B. STT-CiM array

In this section, we present the array-level design of STT-CiM using the mechanisms described above. As shown in Figure 6, the proposed STT-CiM memory array takes an additional multi-bit input signal (CiMType) that indicates the type of compute-in-memory operation that needs to be performed for every memory access. An operation decoder interprets this input and generates appropriate control signals to perform the desired logic operation. In order to enable compute-in-memory operations, the read peripheral circuits present in each column (sensing circuit and global reference generation circuit in Figure 6) are enhanced, while the core data array remains the same as in standard STT-MRAM. The write peripheral circuits also remain unchanged, as write operations are identical to standard STT-MRAM. We next describe the enhancements to the read peripheral circuits.

### Sensing circuitry

Figure 6 shows the sensing circuit enhanced to support all the logic operations discussed in Section IV-A. It consists of two sense amplifiers, a CMOS-based NOR gate, three multiplexers and a Peripheral Logic Unit (PLU). We note that the area and power overheads associated with the
sensing circuit are minimal since the sensing circuit constitutes
a small fraction of the total memory area. As shown in
the figure, the reference currents ($I_{ref1}$, $I_{ref2}$) produced by
the global reference generation circuit are fed to the two sense
amplifiers in order to realize the sensing schemes discussed in
Section [IV-A]. The PLU contains the logic gates necessary to
calculate the ADD operation as shown in Figure 5. The three
MUX control signals ($sel_0$, $sel_1$, $sel_2$) are generated by the
operation decoder to select the desired compute-in-memory
operation.

![Fig. 6: STT-CiM array structure](image)

**Reference generation.** Figure 6 illustrates the modified refer-
cence generation circuit used to produce the additional refer-
cence currents necessary for the proposed sensing schemes.
It includes two reference stacks, one each for the two sense
amplifiers in the sensing circuit. Each stack consists of
three bit-cells programmed to offer resistances $R_1$, $R_2$ and
$P_{AP}$, respectively. $R_{P}$ represents the read reference
MTJ used in a standard STT-MRAM memory array. The
operation decoder generates control signals ($rwl_0$, $rwl_1$, ....
$rwl_n$) that are used to enable a subset of these bit-cells
in the reference stacks, which in turn produces the desired reference
currents.

The STT-CiM array can perform both regular memory
operations and a range of CiM operations. The normal read
operation is performed by enabling a single wordline and
setting $sel_0$, $sel_1$, and $rwl_0$ to logic ‘1’. On the other hand,
a CiM operation is performed by enabling two wordlines and
setting CiMType to the appropriate value, which eventually
results in computing the desired function of the enabled words.

**C. CiM operation under process-variations**

The STT-CiM array suffers from the same failure mech-

anisms, *viz.* read disturb failures, read decision failures and
write failures, that are observed in a standard STT-MRAM
memory array. In this section, we compare the failure rates in
STT-CiM with that of a standard STT-MRAM. A normal read
(write) operation in STT-CiM will have the same failure rate as

\[ R_{AP} > R_{REF} > R_P \]

\[ 2 \times R_{AP} > R_{REF} > R_P \]

in an STT-MRAM based memory array, since the read (write)
mechanism is identical. However, CiM operations differ in
their failure rates, since the currents that flow through each
bit-cell differ when enabling two wordlines simultaneously.
In order to analyze the read disturb and read decision failures
under process variation for CiM operations, we performed a
detailed circuit-level simulation on 1 million samples using the
variation parameters specified in section [VI] Figure 7 shows
the probability density distribution of the possible currents
obtained during read and CiM operations on these 1 million
samples.

![Fig. 7: Probability density distribution of possible $I_{SL}$
current under process variation during read and CiM
operations](image)

**Read disturb failures.** As shown in Figure 7, the overall
current flowing through the source line is slightly higher in
case of a CiM operation as compared to a normal read.
However this increased current is divided between the two
parallel paths, and consequently the net read current flowing
through each bit-cell (MTJ) is reduced. Hence, the read disturb
failure rate is even lower for CiM operations than normal read
operations.

**Read decision failures.** As shown in Figure 7(b) the net
current flowing through the source line ($I_{SL}$) in case of a
CiM operation can have 3 possible values, *i.e.*, $I_{P}−P_-, I_{AP}−P_-
(I_{AP−P})$. A read decision failure occurs during
a CiM operation when the current $I_{P}−P_-$ is interpreted as
$I_{AP−P}−$ (or vice versa), or when $I_{AP−P}$ is inferred as $I_{AP−P}−$
(or vice versa). In contrast to normal reads, CiM operations
have two read margins (shown in Figure 7(b)), one between
$I_{P}−P_-$ and $I_{AP}−P_-$ and another between $I_{AP−P}$ and $I_{AP−P}$.
Our simulation results show that the read margins for CiM
operations are lower as compared to normal reads, therefore
they are more prone to read decision failures. Moreover, the
read margins in CiM operations are unequal\(^2\) thus we have
more failures arising due to the read margin between $I_{P}−P_-$
and $I_{AP−P}−$.

\(^2\)This is due to asymmetric nature of parallel resistive circuits
ECC for STT-CiM. In order to mitigate these failures in STT-MRAM, various ECC schemes have been previously explored [13], [14]. We note that ECC techniques that uses extended Hamming codes such as single error correction and double error detection (SECDED) and double error correction and triple error detection (DECTED) can be used directly without any modification to address the read decision failures in CiM operations as well. This is feasible because the codeword properties for these codes are retained for a CiM XOR operation. Figure 8 shows the codeword retention property of a CiM XOR operation using a simple Hamming code. As shown in the figure, $word_1$ and $word_2$ are augmented with ECC bits ($p_1$, $p_2$, $p_3$) and stored in memory as $InMemW_1$ and $InMemW_2$ respectively. A CiM XOR operation performed on these stored words ($InMemW_1$, $InMemW_2$) results in the ECC codeword for $word_1$ XOR $word_2$, therefore the codewords are preserved for CiM operations. We propose to leverage this retention property of CiM XORs to detect and correct errors in all CiM operations. This is enabled by the fact that our design STT-CiM always computes bitwise XOR (CiM XOR) irrespective of the desired CiM operation. We next demonstrate error detection and correction mechanism for CiM operations using Figure 9 that employs a simple Hamming code based ECC scheme. Let us assume that $d_1$ data bit suffers from the read decision failure during CiM operations, as shown in the figure. As a result, logic ’11’ ($I_{P=1-P}$) is inferred as logic ’10’ ($I_{AP=1-P}$) which leads to erroneous CiM outputs. An error detection logic operating on the CiM XOR output (shown in Figure 9) detects an error in the $d_1$ data bit which can be corrected directly for a CiM XOR operation by simply flipping the erroneous bit. However for other CiM operations that do not retain codewords, we perform two sequential normal reads on words $InMemW_1$ and $InMemW_2$, and correct the erroneous bits by recomputing them using near memory computation unit (discussed in section V). Note that, such 2 normal reads based corrections lead to overheads, as we need to access memory array 3 times (compared to 2 times in STT-MRAM), thereby reducing the efficiency of STT-CiM. However, our variation analysis show that corrections on CiM operations are infrequent, and occurs with a probability of 0.1.

Methodology for computing ECC requirement. We use the methodology employed in [13] to determine ECC requirements for both STT-MRAM (baseline) as well as proposed STT-CiM design. The approach uses circuit level simulations to determine the bit-level error probability, which is then used to estimate the array level yield. Moreover, the ECC scheme is selected based on the target yield requirement. Our simulation shows that 1 bit failure probability of normal reads and CiM operations are $4.2 \times 10^{-8}$ and $6 \times 10^{-5}$ respectively. With these obtained bit-level failure rates and assuming a target yield of 99%, the ECC requirement for 1MB STT-MRAM is single error correction and double error detection (SECDED), whereas for 1MB STT-CiM is three error correction and four error detection (3EC4ED). Note that the overheads of the ECC schemes are considered and reflected in our experimental results. Moreover, our simulation shows that the probability of CiM operations having errors is 0.1, i.e., 1 in 10 CiM operations will have an error, which will always be detected by using 3EC4ED code on CiM XORs. Further, these errors are directly corrected for CiM XORs using 3EC4ED code, whereas are corrected via sequential accesses for other CiM operations.

Fig. 8: Example demonstrating codeword retention property of CiM XOR

V. ARCHITECTURE FOR STT-CiM

In order to evaluate the application-level benefits of STT-CiM, we integrate it as a scratchpad in the memory hierarchy of a programmable processor [51]. This section describes optimizations to increase the efficiency of STT-CiM and architectural enhancements required to expose it to software.

A. Optimizations for STT-CiM

In order to further the efficiency improvements obtained by STT-CiM, we propose two additional optimizations. Vector CiM operations. Many modern computing workloads exhibit significant data parallelism. To further enhance the efficiency of STT-CiM for such applications, we introduce Vector Compute-in-Memory (VCiM) operations. The key idea behind VCiM operations is to exploit the internal memory bandwidth to perform CiM operations on the elements of a vector simultaneously. Figure 10 shows how the internal memory bandwidth (32xN bits) can be significantly larger than the limited I/O bandwidth (32 bits) visible to the processor. We exploit this internal bandwidth to perform vector operations (N words wide) within STT-CiM. However, the computed vector cannot be directly transferred to processor in one access due to I/O limitations. To address this issue, we leverage the reduction computation patterns commonly observed in several applications and introduce a Reduce Unit (RU) shown in Figure 10. The RU takes an array of data elements as inputs and reduces it to a single data element. A reduce unit can support various reduction operations such as summation, zero-compare (shown in Table II). The overheads of the RU depend on two factors: (i) the number of different reduction operations supported, and (ii) the maximum vector length allowed (can be between 2 to N words). In our evaluation, we have included...
the timing and area overheads associated with the proposed RU. To limit the area overheads, we support two reduction operations, i.e., summation and zero-compare, and evaluate our design for vector lengths of 4 and 8. Consider an example VCiM operation which computes \( \sum_{i=1}^{N} A[i] + B[i] \), where arrays A and B are stored in rows i and j respectively (shown in Figure 10). To compute the desired function using VCiM operation, we activate rows i and j simultaneously, and configure the sensing circuitry to perform an ADD operation and the RU to perform accumulation of the resulting output. Note that the summation would require 2N memory accesses in a conventional memory. With STT-CiM (but not the proposed vector operations) it requires N memory accesses. With the proposed VCiM operations, only a single memory access is required.

**Near memory computation.** To realize a wider variety of in-memory operations, we introduce a low overhead Near Memory Compute (NMC) unit to the proposed STT-CiM. Specifically, the NMC unit enables operations such as Euclidean distance and L1/L2 norms to be computed by the STT-CiM memory. It also enables correction of erroneous bits for CiM operations using an Error Detection and Correction (EDC) unit which implements the 3EC4ED ECC scheme. The EDC unit checks for errors using the CiM XOR output and signals the controller (shown in Figure 10) on detection of erroneous computations. The controller on receiving this error detection signal performs the required corrective actions.

**TABLE II: Examples of reduction operation**

| Type          | Function                          |
|---------------|-----------------------------------|
| Summation     | \( \text{RuOut = } \sum_{i=1}^{N} A[i] + B[i] \) |
| Zero-Compare  | \( \text{RuOut}[k] = \left( I N_k = 0 \right) ? 0 : 1 \) |

**B. Architectural Extensions for STT-CiM**

To integrate STT-CiM in a programmable processor based system, we propose the following architectural enhancements.

**ISA extension.** We propose extensions in the ISA of a programmable processor to support CiM operations. To this end, we introduce a set of new instructions in the ISA (CiMXOR, CiMNOT, ... CiMADD) that are used to invoke the different types of operations that can be performed in the STT-CiM array. In a load operation, the requested address is sent to the memory, and the memory returns the data stored at the addressed location. However, in the case of a CiM operation, the processor is required to provide addresses of two memory locations instead of a single one, and the memory operates on the two data values to return the final output.

**Format:** Opcode Reg1 Reg2 Reg3

Example: CiMXOR \( R_{ADD1}, R_{ADD2}, R_{DEST} \)

**Instruction format.** Equation 1 shows the instruction format of a CiM instruction with an example. As shown in the example, both the addresses (ADDR1 and ADDR2) required to perform CiMXOR operations are provided through registers. The format is similar to a regular arithmetic instruction that accesses two register values, performs the computation, and stores the result back in a register.

**Load \( R_{ADD1}, R_{ADD2}, R_{DEST} \), Transformation \( \rightarrow \text{CiMXOR} \) \( R_{ADD1}, R_{ADD2}, R_{DEST} \), \( R_{DEST} \rightarrow R_{OUT} \), \( \text{XOR} \) \( R_{DEST}, R_{OUT} \), \( R_{OUT} \rightarrow R_{DEST} \)**

**Fig. 11: Opcode transformation for CiMXOR**

**Program transformation.** To exploit the proposed CiM instructions at the application-level, an assembly-level program transformation is performed, wherein specific sequences of instructions in the compiled program are mapped to a suitable CiM instruction in the ISA. Figure 11 shows an example transformation where two load instructions followed by an XOR operation can be mapped to a single CiMXOR operation.

**Bus and interface support.** In a programmable processor based system, the processor and the memory communicate via a system bus or on-chip network. This makes it essential to analyse the impact of CiM operations on the bus and the corresponding bus interface. As discussed above, a CiM operation is similar to a load instruction with the key difference that it sends two addresses to the memory. Conventional system buses only allow sending a single address onto the bus via the existing address channel. In order to send the second address for CiM operations, we utilize the unused writedata channel of the system bus, which is unutilized during a CiM operation. Besides the two addresses, the processor also sends the type of CiM operation (CIMType) that needs to be performed. Note that it may be possible to overlay the CIMType signal onto the existing bus control signals; however, such optimizations strongly depend on the specifics of the bus protocol being used. In this work, we assume that 3 control bits are added to the bus and account for the resulting overheads in our experiments.

**C. Data Mapping**

In order to perform a CiM instruction, the locations of its operands in memory must satisfy certain constraints. Let us consider a memory organization consisting of several banks

\[ \text{While we consider the case of a shared bus for illustration, the same enhancements can be applied to more complex networks.} \]
where each bank is an array that contains rows and columns. In this case, a CiM operation can be performed on two data elements only if they satisfy three key criteria: (i) they are stored in the same bank, (ii) they are mapped to different rows, and (iii) they are aligned and placed in the same set of columns.

Consequently, a suitable data placement technique is required that maximizes the benefits of the proposed STT-CiM. We observe that the target applications for STT-CiM have well defined computation patterns, facilitating such a data placement. Figure 12 shows three generalized computation patterns observed in these target applications. We next discuss these compute patterns and the corresponding data placement techniques in detail.

**Type I.** This pattern, shown in the top row of Figure 12 involves element-to-element operations (OPs) between two arrays, e.g., A and B. In order to effectively utilize STT-CiM for this compute pattern, we utilize the **array alignment** technique (shown in Figure 12(a)) that ensures alignment of elements A[i] and B[i] of arrays A and B for any value of i. This enables the conversion of operation A[i] OP B[i] into a CiM operation. An extension to this technique is the **row-interleaved placement** shown in Figure 12(b). This technique is applicable to larger data structures that do not fully reside in the same memory bank. It ensures that both the elements, i.e., A[i] and B[i], are mapped to the same bank for any value of i, hence satisfying the alignment criteria for a CiM operation.

**Type II.** This pattern, shown in the middle row of Figure 12 involves a nested loop in which the inner loop iteration consists of a single element of array A being operated with several elements of array B. For this one-to-many compute pattern, we introduce a **spare row** technique for STT-CiM data alignment. In this technique, a spare row is reserved in each memory bank to store copies of an element of A. As shown in Figure 12(c), at the kth iteration of the outer for-loop, a special write operation is used to fill the spare rows in all banks with A[k]. This results in each element of array B becoming aligned with a copy of A[k], thereby allowing CiM operations to be performed on them. Note that the special write operation introduces energy and performance overheads, but this overhead is amortized over all inner loop iterations, and is observed to be quite insignificant in our evaluations.

**Type III.** In this pattern, shown in the bottom row of Figure 12 operations are performed on an element drawn from a small array A and an element from a much larger array B. The elements are selected arbitrarily, i.e., without any predictable pattern. For example, consider when a small sequence of characters needs to be searched within a much larger input string. For this pattern, we propose a **column replication** technique to enable CiM operations, as shown in Figure 12(d). In this technique, a single element of the small array A is replicated across columns to fill an entire row. This ensures that each element of A is aligned with every element of B, enabling a CiM operation to be utilized. Note that the initial overhead due to data replication is very small, as it pales in comparison to the overall number of memory accesses, which is determined by the larger array.

**VI. EXPERIMENTAL METHODOLOGY**

In this section, we discuss the device-to-architecture simulation framework (shown in Figure 13) used in our experiments to evaluate the performance and energy benefits of STT-CiM at the array-level and system-level.

**Device/Circuit modeling.** We first characterize the bit-cells using SPICE-compatible MTJ models that are based on self-consistent solution of Landau-Lifshitz-Gilbert (LLG) magnetization dynamics and Non-Equilibrium-Green’s Function (NEGF) electron transport [54]. Table III shows the MTJ device parameters [55] used in our experiments. Using 45nm bulk CMOS technology and the MTJ models, the memory array along with the associated peripherals and extracted parasitics was simulated in SPICE for various operations (read, write and CiM operations) to obtain array-level timing and energy characteristics. The obtained characteristics were then used as technology parameters in a modified version of CACTI [56] that is capable of estimating system-level properties for a spin-based memory. The variation analysis to compute failure rates was done considering variations in MTJ oxide thickness (σ/µ = 2%), transistor V_T (σ/µ = 5%), and MTJ cross sectional area (σ/µ = 5%).

**System level simulation.** We evaluated STT-CiM as a 1MB scratchpad for an Intel Nios II processor [51]. Figure 14 shows the integration of STT-CiM in the memory hierarchy...
of the programmable processor. In order to expose the STT-CiM operations to software, we extend the Nios II processor’s instruction set with custom instructions. The Avalon on-chip bus was also extended to support CiM operations. Cycle-accurate RTL simulation was used to obtain the execution time and the memory access traces for various benchmarks. These traces along with the energy results obtained through the modified CACTI tool were used to estimate the total memory energy.

### TABLE III: Device parameters

| Material System | TaCoFeB/MgO |
|-----------------|------------|
| MTJ Type        | PMA        |
| Saturation Magnetization ($M_S$) | 1.58T |
| Damping Factor, ($\alpha$) | 0.028 |
| Polarization    | 0.62       |
| Interface Anisotropy | 1.3mJ/m² |
| MTJ Dimension   | 40nm x 40nm x 1.32nm |
| Oxide Thickness ($t_{ox}$) | 1.1nm |
| Energy Barrier  | 65KT       |
| $T$             | 300K       |
| RA Product      | 10ohm-µm²  |
| TMR             | 124%       |
| CMOS Technology | 45nm Bulk CMOS |
| Assumed Variation ($\sigma/\mu$) | $t_{ox} = 2\%$, MTJ Area = 5% transistor $V_T=5\%$ |

### TABLE IV: Benchmark applications

| Applications | Domain                          |
|--------------|---------------------------------|
| Aho-Corasick (AHC) | String matching                 |
| Knuth-Morris-Pratt (KMP) | String matching                 |
| Edit Distance (EDIST) | Spelling correction, Computational biology |
| Bit-Blit (BITL) | Low-level graphics              |
| Longest Common Subsequence (LCS) | Data compression, Bio-informatics |
| Rivest Cipher 4 (RC4) | Cryptography                     |
| IMGSEG | Image segmentation              |
| GLVQ | Eye detection                    |
| K-means clustering (KMEANS) | Digit recognition               |
| Optical Character Recognition (OCR) | Character recognition          |
| Multi Layer Perceptron (MLP) | Protein structure classification |
| Support Vector Machines (SVM) | Text classification            |

**Benchmark applications.** We evaluate STT-CiM on a suite of twelve applications drawn from various domains (Table IV).

### VII. Results

In this section, we first present an array-level analysis of STT-CiM and then quantify its benefits through system-level energy and performance evaluation.

#### A. Array-level analysis

**Energy.** Figure 15 shows the energy consumed by standard read and a representative CiM operation (XOR) in a 1MB STT-CiM array (second and third bars). Each bar shows the energy breakdown into the major components, i.e., peripheral circuitry (PeriphCkt), wordline (WordL), bitline (BitL), reference generation circuitry (REF), sense amplifier (SenseA), and error correction circuitry (ECC). For reference, we provide the read energy for an STT-MRAM array of the same capacity (first bar) and all energy numbers are normalized to this value. A normal read operation in STT-CiM incurs energy overheads of about 4.4%, which arise primarily due to the extra peripheral circuits (PeriphCkt) and more stringent ECC requirements. Our STT-CiM design uses a 3EC4ED ECC scheme (as compared to SECDED in STT-MRAM) that results in about 3% of the net 4.4% energy overhead. The XOR CiM operation consumes higher energy than a standard read operation mainly due to the charging of multiple wordlines and a slightly higher source line current. Since a CiM operation substitutes two normal read operations, we also present the energy required for two reads in a standard STT-MRAM (last bar). Note that an array-level comparison greatly understates the benefits of STT-CiM. Nevertheless, it is worth noting that even at the array level, STT-CiM consumes 38.2% less energy. The benefits mainly arise from a lower bitline dynamic energy (BitL), since only a single access to the memory array is required for STT-CiM.

**Area and access time.** Figure 16 shows the area breakdown for two STT-CiM designs that support vector operations of length 4 and 8 (VEC4 and VEC8 respectively). As compared to our baseline the area overheads for VEC4 and VEC8 designs, are 8.4% and 9.1% respectively. As shown in the Figure 16 ECC storage and ECC Logic forms the major component of the obtained area overheads (3.7% and 3.2% respectively). Note that, for STT-CiM designs the total area is dominated by the core array which remains unchanged.

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It does not consider the major impact of reduced data transfers between the processor and memory, which is considered in the system-level results presented in the next subsection.
Finally, the access time overhead for STT-CiM was found to be $\sim 0.8\%$, because the wordline and bitline delays dominate the total memory latency.

The speedup shown in the figure is with respect to the baseline design, i.e., the processor system integrated with a standard STT-MRAM based memory. As discussed in Section V-B, CiM lowers the total number of memory accesses as well as the number of instructions executed, which leads to performance benefits at the system level. Overall, for STT-CiM without vector operation, we observe performance benefits ranging from 1.07X to 1.36X. With vector operations, the average speedup increased to 3.25x and 3.93x for vector lengths of 4 and 8, respectively. Comparing Figures 18 and 20, we see that the factors that indicate higher energy savings for an application (large fraction of memory accesses are CC-Reads, opportunities for vectorization exist) are also predictive of higher performance improvements.

In order to demonstrate the performance sensitivity to memory latency, we vary the memory latency and evaluate the execution time for each application. Figure 19 shows the sensitivity analysis of STT-CiM without vector operations for range of applications. On the Y-axis, we have the speedup, and on the X-axis the memory latency. We observe that increasing memory latency yields higher performance benefits for the STT-CiM design. This is expected because the CiM operations lower the number of total memory accesses, as a result, a higher memory latency will result in a larger performance benefit. On an average, we achieve 1.13x speedup for a memory latency of 1 cycle, and 1.26x speedup for a memory latency of 16 cycles, thereby illustrating the effectiveness of the proposed approach.

VIII. CONCLUSION

STT-MRAM is a promising candidate for future on-chip memories. In this work, we proposed STT-CiM, an enhanced STT-MRAM that can perform a range of arithmetic, bitwise and vector compute-in-memory operations. We addressed a key challenge associated with these in-memory operations, i.e. reliable computations under process variations. We utilized the proposed design (STT-CiM) as a scratchpad in the memory hierarchy of a programmable processor, and introduced ISA extensions and on-chip bus enhancements to support in-memory computations. We proposed architectural optimizations and data mapping techniques to enhance the efficiency of our proposed design. A device-to-architecture simulation framework was used to evaluate the benefits of STT-CiM. Our experiments indicate that STT-CiM achieves substantial improvements in energy and performance, and shows considerable promise in alleviating the processor-memory gap.

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Fig. 17: Application-level memory energy

![Normalized Energy vs. Application](chart)

- Baseline
- WRITE
- STT-CiM
- READ
- STT-CiM+VEC4
- CiM
- STT-CiM+VEC8
- NMCorrection

Fig. 18: Memory access breakdown

![Memory Access Breakdown](chart)

- KMP
- AHC
- RC4
- BLIT
- LCS
- GLVQ
- KMEANS
- EDIST
- OCR
- IMGSEG
- MLP
- SVM

Fig. 19: Performance sensitivity to memory latency

![Speedup vs. Memory Latency](chart)

**LAT = 1**  **LAT = 4**  **LAT = 8**  **LAT = 16**

- KMP
- AHC
- RC4
- BLIT
- LCS
- GLVQ
- KMEANS
- EDIST
- OCR
- IMGSEG

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Fig. 20: Application-level system performance

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