Wafer-scale low-disorder 2DEG in $^{28}$Si/SiGe without an epitaxial Si cap

Degli Esposti, Davide; Paquelet Wuetz, Brian; Fezzi, Viviana; Lodari, Mario; Sammak, Amir; Scappucci, Giordano

DOI
10.1063/5.0088576

Publication date
2022

Document Version
Final published version

Published in
Applied Physics Letters

Citation (APA)
Degli Esposti, D., Paquelet Wuetz, B., Fezzi, V., Lodari, M., Sammak, A., & Scappucci, G. (2022). Wafer-scale low-disorder 2DEG in $^{28}$Si/SiGe without an epitaxial Si cap. Applied Physics Letters, 120(18), Article 184003. https://doi.org/10.1063/5.0088576

Important note
To cite this publication, please use the final published version (if applicable). Please check the document version above.
Green Open Access added to TU Delft Institutional Repository

'You share, we take care!' - Taverne project

https://www.openaccess.nl/en/you-share-we-take-care

Otherwise as indicated in the copyright section: the publisher is the copyright holder of this work and the author uses the Dutch legislation to make this work public.
Wafer-scale low-disorder 2DEG in $^{28}\text{Si}/\text{SiGe}$ without an epitaxial Si cap

Cite as: Appl. Phys. Lett. 120, 184003 (2022); https://doi.org/10.1063/5.0088576
Submitted: 18 February 2022 • Accepted: 27 April 2022 • Published Online: 04 May 2022

Davide Degli Esposti, Brian Paquelet Wuetz, Viviana Fezzi, et al.

ARTICLES YOU MAY BE INTERESTED IN

Lightly strained germanium quantum wells with hole mobility exceeding one million
Applied Physics Letters 120, 122104 (2022); https://doi.org/10.1063/5.0083161

Quantum dot arrays in silicon and germanium
Applied Physics Letters 116, 080501 (2020); https://doi.org/10.1063/5.0002013

Self-aligned gates for scalable silicon quantum computing
Applied Physics Letters 118, 104004 (2021); https://doi.org/10.1063/5.0036520
Wafer-scale low-disorder 2DEG in $^{28}$Si/SiGe without an epitaxial Si cap

Cite as: Appl. Phys. Lett. 120, 184003 (2022); doi: 10.1063/5.0088576
Submitted: 18 February 2022 · Accepted: 27 April 2022 ·
Published Online: 4 May 2022

Davide Degli Esposti,$^{1}$ Brian Paquelet Wuetz,$^{1}$ Viviana Fezzi,$^{1}$ Mario Lodari,$^{1}$ Amir Sammak,$^{2}$ and Giordano Scappucci$^{1,2}$

AFFILIATIONS
$^{1}$QuTech and Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, Netherlands
$^{2}$QuTech and Netherlands Organisation for Applied Scientific Research (TNO), Stieltjesweg 1, 2628 CK Delft, The Netherlands

$^{a}$Author to whom correspondence should be addressed: g.scappucci@tudelft.nl

ABSTRACT
We grow $^{28}$Si/SiGe heterostructures by reduced-pressure chemical vapor deposition and terminate the stack without an epitaxial Si cap but with an amorphous Si-rich layer obtained by exposing the SiGe barrier to dichlorosilane at 500 °C. As a result, $^{28}$Si/SiGe heterostructure field-effect transistors feature a sharp semiconductor/dielectric interface and support a two-dimensional electron gas with enhanced and more uniform transport properties across a 100 mm wafer. At $T = 1.7$ K, we measure a high mean mobility of $(1.8 \pm 0.5) \times 10^5$ cm$^2$/V s and a low mean percolation density of $(9 \pm 1) \times 10^{10}$ cm$^{-2}$. From the analysis of Shubnikov–de Haas oscillations at $T = 190$ mK, we obtain a long mean single particle relaxation time of $(8.1 \pm 0.5)$ ps, corresponding to a mean quantum mobility and quantum level broadening of $(7.5 \pm 0.6) \times 10^6$ cm$/V$ s and $(40 \pm 3) \mu$eV, respectively, and a small mean Dingle ratio of $(2.3 \pm 0.2)$, indicating reduced scattering from long range impurities and a low-disorder environment for hosting high-performance spin-qubits.

Published under an exclusive license by AIP Publishing. https://doi.org/10.1063/5.0088576

Strained $^{28}$Si/SiGe heterostructures are a compelling platform for scalable qubit tiles based on gate-defined quantum dots. In these $^{28}$Si buried quantum wells, electron spins experience a quiet electrical and magnetic environment. The electronically noisy semiconductor/dielectric interface is far away, separated from the quantum well by a SiGe epitaxial barrier, and the nuclear spins have been removed by isotopic enrichment. Continuous advances in the materials science of $^{28}$Si/SiGe and improved device fabrication have enabled quantum logic with spin qubits crossing the surface code threshold, and CMOS-based cryogenic control of quantum circuits. In the mainstream approach to quantum dot fabrication, the last step in the heterostructure growth cycle comprises the heteropitaxial deposition of a thin epitaxial Si cap on the SiGe barrier. This is to avoid the formation of low-quality Ge-based oxides upon exposure of SiGe to air. After the Si cap deposition, a high-$\kappa$ dielectric is deposited ex situ and at low-temperature ($\sim$300 °C) to insulate the gate from the buried and undoped quantum well. This low-temperature process preserves the strain in the quantum well but induces large concentrations of impurities at the critical semiconductor/dielectric interface. These impurities can influence the electrostatic confining potential landscape induced by the gates, leading to the formation of unintentional quantum dots and are a source of charge noise limiting qubit performance. While efforts have focused on achieving uniform and high-purity $^{28}$Si quantum wells with sharp interfaces now much attention is needed to optimize the step, which terminates the heterostructure deposition cycle and has a critical role in defining the semiconductor/dielectric interface.

In this Letter, we explore $^{28}$Si/SiGe heterostructures terminated by exposure to dichlorosilane (DCS) gas at a temperature well below the threshold for epitaxial growth of Si. By avoiding the growth of an epitaxial Si cap altogether, we obtain $^{28}$Si/SiGe heterostructure field effect transistors (H-FETs) with a sharp semiconductor/dielectric interface. We show that the $^{28}$Si quantum well supports a two-dimensional electron gas (2DEG) with less disorder and improved quantum transport properties compared to heterostructures with an epitaxial Si cap.

Figure 1(a) illustrates the workflow to fabricate $^{28}$Si/SiGe H-FETs. We grow $^{28}$Si/SiGe heterostructures on 100 mm Si(001) wafers using an Epsilon 2000 (ASMI) reduced-pressure chemical vapor deposition reactor. We use isotopically enriched $^{28}$SiH$_4$ for growing the $^{28}$Si quantum well [residual $^{28}$Si concentration of 0.08% (Refs. 3, 7, and 15)] and DCS (H$_2$SiCl$_2$) and GeH$_4$ for all other layers. The heterostructure comprises a 3 µm step-graded Si$_{1-x}$Ge$_x$ layer...
Figure 1. (a) Schematics of the Si/SiGe heterostructure and formation of the dielectric interface in a Hall-bar heterostructure field effect transistor. z indicates the heterostructure growth direction. The heterostructure is terminated by exposure to dichlorosilane (DCS) gas at a temperature below the threshold for growing an epitaxial SiGe barrier. (b) BF-STEM image of the active layers of the Si/SiGe heterostructure field effect transistor showing, from left to right, the SiGe quantum well, the SiO$_2$ strain-relaxed buffer layer, the tensile-strained Si$_{1.7}$Ge$_{0.3}$ quantum well, the Si$_{1.7}$Ge$_{0.3}$ barrier, followed by the SiO$_2$/Al$_2$O$_3$ dielectric stack. (c) Electron energy loss spectroscopy (EELS) quantititative concentration proﬁles using the Si–K (1839–2084 eV), Al–K (1560–1700 eV), O–L (532–660 eV), and Ge–L (1220–1400 eV) edges. To recognize differences between the different bonding states, we use the low-energy edges to recognize differences between the different bonding states: Si (blue), SiO$_x$ (magenta), and AlO$_x$ (green). We do not detect any Cl or H signal above the background noise in our EELS data.

We characterized the H-FETs by magnetotransport measurements at a temperature of 1.7 K and 190 mK (Ref. 32) in refrigerators equipped with cryo-multiplexers. With this approach, we measure...
multiple devices from a wafer in the same cooldown. The devices are operated in accumulation mode in which electrons populate the undoped $^{28}$Si quantum well by applying a positive DC gate voltage ($V_G$). We measure the longitudinal and transverse components of the resistivity tensor, $\rho_{xx}$ and $\rho_{xy}$, by using standard four-probe lock-in techniques at fixed AC source-drain bias of 100 $\mu$V. We calculate the longitudinal $\sigma_{xx}$ and transverse $\sigma_{xy}$ conductivity via tensor inversion. We measure electron density ($n$) and mobility ($\mu$) with the classical Hall effect at low perpendicular magnetic field $B$.

Figure 2(a) shows for a typical device the turn-on and pinch-off source-drain current $I_{SD}$ as a function of increasing and decreasing $V_G$, respectively. Above a threshold voltage ($V_{Gt} = 350$ mV), the current starts flowing in the channel and increases monotonically. If the gate voltage is operated within the operational gate voltage range $\Delta V_G$ (red curve), $I_{SD}$ is stable and the threshold and pinch-off voltages overlap. At higher $V_G$, $I_{SD}$ saturates due to charge build-up at the semiconductor/dielectric interface, triggering hysteresis and, consequently, a shift in pinch-off voltage. As shown in Fig. 2(b), if $V_G$ is swept within the operational gate voltage range, $n$ increases linearly with $V_G$ up to $6 \times 10^{11}$ cm$^{-2}$. From the slope $\frac{dn}{dV_G}$, we derive an effective capacitance per unit area $C \approx 205$ nF/cm$^2$ using the relationship $C = \varepsilon_r \varepsilon_0 \frac{d}{dV_G}$.

This capacitance characterizes the parallel-plate capacitor where the 2DEG in the $^{28}$Si quantum well and the metallic top gate are insulated by a SiGe/SiO$_x$/AlO$_x$ dielectric stack. Figure 2(c) shows the density-dependent mobility measured in the same density range as in Fig. 2(b). In the low density regime ($n \leq 3 \times 10^{11}$ cm$^{-2}$), the mobility rises steeply due to the increasing screening of Coulomb scattering from remote charged impurities located at the semiconductor/dielectric interface. At higher density ($n \geq 5 \times 10^{11}$ cm$^{-2}$), the mobility approaches saturation at a value above 2.5 $\times$ 10$^5$ cm$^2$/Vs. This weaker density-dependence is typical of a high-quality 2DEG, where the mobility maximum is limited by short-range scattering from impurities within or near the quantum well.

In Figs. 2(d)–2(f), we plot the distributions of the maximum electric field ($E_{2max}^\text{max}$), the percolation density ($n_p$), and the mobility at high density for heterostructures terminated with an amorphous Si-rich layer (blue) and, as a benchmark, for heterostructures with an epitaxial Si cap (red). These three metrics are obtained from the analysis of measurements in Figs. 2(a)–2(c), repeated on multiple H-FETs on dies that are randomly selected from different locations across the 100 mm wafer. $E_{2max}^\text{max}$ is calculated as $C \Delta V_G/e \varepsilon_r$, where $\varepsilon_r = 11.68$ is the dielectric constant of Si, indicates the maximum electric field that we can apply to the quantum well in the H-FETs before hysteresis. Large $E_{2max}^\text{max}$ are desirable for device stability, increased tunability, and large valley splitting. $n_p$ characterizes disorder in low density regime, relevant for quantum dot operation, and is obtained by fitting the density-dependent $\sigma_{xx}$ to percolation theory. Finally, the mobility at high density is a probe for disorder arising from within or nearby the

![Figure 2](https://example.com/figure2.png)

**FIG. 2.** (a) Source–drain current $I_{SD}$ measured at $T = 1.7$ K as a function of gate voltage $V_G$ for a typical Hall bar heterostructure field effect transistor (H-FET). The operational gate voltage range $\Delta V_G$ indicates the range over which an $I_{SD}$-$V_G$ curve (red line) can be measured repeatedly without hysteresis and drift. (b) Density $n$ as a function of gate voltage $V_G$ and (c) electron mobility $\mu$ as a function of $n$ measured within the operational gate voltage range. (d)–(f) Distributions of maximum electric field applicable before hysteresis $E_{2max}^\text{max}$, percolation density $n_p$, and $\mu$ measured at $n = 6 \times 10^{11}$ cm$^{-2}$ for heterostructures terminated by a Si-rich amorphous layer obtained exposure to DCS at 500 °C (blue, 14 H-FETs measured) and for heterostructures with an epitaxial Si cap grown by exposure to DCS at 675 °C (red, 16 H-FETs measured). Quartile box plots, mode (horizontal line), means (diamonds), outliers (circles), and 99% confidence intervals of the mean (dashed whiskers) are shown.
quantum well. Overall, H-FETs perform better when the SiGe barrier is terminated with an amorphous Si-rich layer. We measure a 9% increase in mean $F_{max}$, a 7% decrease in mean percolation density, and a 40% increase in mean mobility. Most importantly, we observe a reduction in the spread of $F_{max}$, $n_p$, and $\mu$ of $\approx 300\%$, $\approx 200\%$, and $\approx 30\%$, respectively, pointing to an increased uniformity on a 100 mm wafer scale.

We further characterize disorder in the $^{28}$Si/SiGe heterostructure at 190 mK by measuring the single-particle relaxation time $\tau_q$ in the quantum Hall regime. From $\tau_q$, we derive the quantum mobility $\mu_q = e\tau_q/m^*$, where $e$ is the elementary charge and $m^*$ is the effective mass, and the quantum level broadening of the momentum eigenstates $\Gamma = h/(2\tau_q)$, where $h$ is the reduced Planck constant. $\mu_q$ associated with $\tau_q$ is influenced by all scattering events and is different from the mobility $\mu = e\tau/m^*$, where the scattering time $\tau$ is unaffected by forward scattering. Therefore, $\tau_q$ and $\mu_q$ qualify the disorder in the heterostructure more comprehensively than $\tau$ and $\mu$.

Figure 3(a) shows for the H-FET with the highest mobility a measurement of $\rho_{xx}$ plotted for clarity against the Landau level filling factor $\nu = ln(eB)/h$, where $h$ is the Plank constant. This measurement was performed at fixed density $n = 4.75 \times 10^{11}$ cm$^{-2}$ by keeping $V_G$ constant and sweeping $B$. Onset of Shubnikov–de Haas oscillation, Zeeman splitting, and valley splitting occurs at 0.125, 0.43, and 1.15 T, respectively, corresponding to $\nu = 152$, 42, and 17. The observation of Shubnikov–de Haas oscillations, Zeeman, and valley splitting at these high filling factors indicates a very low level of disorder. Figure 3(b) shows the normalized oscillation amplitude $\Delta \rho_{xx}/\rho_0 = (\rho_{xx} - \rho_0)/\rho_0$ in the low magnetic field regime after polynomial background subtraction. $\rho_0 \approx 63 \Omega$/square is the longitudinal resistivity at zero magnetic field from which we extract a mobility of $2.7 \times 10^5$ cm$^2$/V s.
We estimate $\tau_s = (7.4 \pm 0.1)$ ps from a fit of the Shubnikov–de Haas oscillation envelope to the function $\Delta \rho_{xx} = 4 \rho_0 \chi(T) \exp(-\pi/\omega_s \tau_s)$, where $\chi(T) = (2\pi k_B T / \hbar \omega_c) / \sinh(2\pi k_B T / \hbar \omega_c)$. Here, $T = 190$ mK, $\rho_0$ is the Boltzmann constant, and $\omega_c$ is the cyclotron frequency calculated using a fixed $m^* = 0.19 m_e$. From $\tau_\eta$ we derive $\mu_\eta = (6.8 \pm 0.1) \times 10^4$ cm$^2$/V s, $\Gamma = (44 \pm 1)$ $\mu$eV, and find a Dingle ratio $\tau_s/\tau_\eta \approx 3.8$. The Dingle plot of Fig. 3(c) highlights the high number of oscillation maxima and minima used in the fitting procedure.

In Figs. 3(d)–3(f), we plot the distributions for $\tau_\eta$ and $\mu_\eta$, $\Gamma$, and the Dingle ratio $\tau_s/\tau_\eta$ measured in the high density regime $[n = (5 - 6) \times 10^{11}$ cm$^{-2}$]. As in Figs. 2(d)–2(f), we consider heterostructures terminated with an amorphous Si-rich layer (blue, $5$ H-FETs measured) and heterostructures with an epitaxial Si cap (red, $7$ H-FETs measured). Heterostructures with an amorphous Si-rich layer have a mean $\tau_\eta$ of $(8.1 \pm 0.5)$ ps and consequently a mean $\mu_\eta$ of $(7.5 \pm 0.6) \times 10^4$ cm$^2$/V s and $\Gamma$ of $(40 \pm 3)$ $\mu$eV, representing a $\pm 2 \times$ improvement compared to heterostructures with an epitaxial Si cap. Consistent with the trend in Figs. 2(d)–2(f), we find a significant reduction in spread for $\tau_\eta$ (30%) and $\Gamma$ (58%). Furthermore, in heterostructures with an amorphous Si-rich layer, we find a mean Dingle ratio of $(2.3 \pm 0.2)$. This mean value is $\approx 300\%$ smaller and has an $80\%$ reduction in spread compared to heterostructures with an epitaxial Si cap. This low value of the Dingle ratio indicates that short-range scattering from impurities within or near the quantum well is the dominant scattering mechanism, in agreement with the analysis of the mobility-density curve. Scattering from remote impurities is reduced thanks to a better semiconductor/dielectric interface. Our mean value for $\tau_\eta$ in $^{28}$Si/Ge is also on par with the best value reported in Ref. 35 from H-FETs in Si/Ge heterostructures featuring an epitaxial Si cap. However, in our samples, the semiconductor/dielectric interface is much closer to the channel ($30\,\text{nm}$ compared to $50\,\text{nm}$ in Ref. 35). Therefore, this comparison confirms that scattering from remote impurities is limited in our devices as a consequence of a high-quality and uniform semiconductor/dielectric interface associated with the termination process at $500\,\text{C}$.

In summary, we challenged the mainstream approach to deposit an epitaxial Si cap on $^{28}$Si/Ge heterostructures and, instead, we terminated the SiGe barrier with an amorphous Si-rich layer, obtained by exposure to DCS at $500\,\text{C}$. Compared to previous heterostructures that feature an epitaxial Si cap and that have already produced high performance spin qubits, we demonstrate an improvement in performance of H-FETs in terms of mean value and spread of mobility, percolation density, maximum electric field before hysteresis, and single particle relaxation time (and hence quantum mobility). We speculate that performance improves because the amorphous Si-rich layer gets completely oxidized compared to the epitaxial Si cap (supplementary material), thereby creating a more uniform $\text{SiO}_2$ layer with less scattering centers. By having a better semiconductor/dielectric interface and wafer-scale uniformity, we expect that this material stack may lead to Si spin qubits with improved yield and performance. In this direction, charge noise measured in quantum dots on these heterostructures will be very informative as these measurements probe the dynamics of charge fluctuations that transport experiments are not very sensitive to. These results motivate new studies, for example, by varying the temperature and/or time of exposure to DCS to understand in detail the nature of the amorphous Si-rich layer on the SiGe barrier, the role of Cl and H upon oxidation in air, and to use this knowledge as a tool for further optimizing the semiconductor/dielectric interface.

See the supplementary material for an extended Fig. 1 and measurements of the electron temperature.

This research was supported by the European Union’s Horizon 2020 research and innovation programme under the Grant Agreement No. 951852 (QLSI project) and in part by the Army Research Office (Grant No. W911NF-17-1-0274). The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Army Research Office (ARO), or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein.

AUTHOR DECLARATIONS
Conflict of Interest
The authors have no conflicts to disclose.

DATA AVAILABILITY
The data that support the findings of this study are available within the article and its supplementary material.

REFERENCES
1. M. K. Vandersypen, H. Buhlm, J. S. Clarke, A. S. Dzurak, R. Ishihara, A. Morello, D. J. Reilly, L. R. Schreiber, and M. Veldhorst, npj Quantum Inf. 3, 34 (2017).
2. R. Li, L. Petit, D. P. Franke, J. P. Dehollain, J. Helsen, M. Steudtner, N. K. Thomas, Z. R. Yoscovits, K. J. Singh, S. Wehner, L. M. K. Vandersypen, J. S. Clarke, and M. Veldhorst, Sci. Adv. 4, eaaar3960 (2018).
3. X. Xue, M. Russ, N. Samkharadze, B. Undseth, A. Sammak, G. Scappucci, and L. M. Vandersypen, Nature 601, 343 (2022).
4. A. Noiri, K. Takeda, T. Nakajima, T. Kobayashi, A. Sammak, G. Scappucci, and S. Tarucha, Nature 601, 338 (2022).
5. A. Mills, C. Guinn, M. Gallans, A. Sigillito, M. Feldman, E. Nielsen, and J. Petta, arXiv:2111.11937 (2021).
6. B. Harvey-Collard, J. Dijkema, G. Zheng, A. Sammak, G. Scappucci, and L. M. K. Vandersypen, arXiv:2108.01206v1 (2021).
7. X. Xue, B. Patra, J. P. van Dijk, N. Samkharadze, S. Subramanian, A. Corna, B. P. Wuetz, C. Jeon, F. Sheikh, E. Jurecz-Hernandez et al., Nature 593, 205 (2021).
8. W. Lawrie, H. Ennink, N. Hendrickx, J. Boter, S. Amitonov, M. Lodari, B. Paquelet Wuetz, C. Volk, S. Philips et al., Appl. Phys. Lett. 116, 085010 (2020).
9. T. Thorbeck and N. M. Zimmerman, AIP Adv. 5, 087107 (2015).
10. E. J. Connors, J. Nelson, H. Qiao, L. F. Edge, and J. M. Nichol, Phys. Rev. B 100, 165305 (2019).
11. T. Strack, A. Hollmann, F. Schauer, O. Fedorets, A. Schmidbauer, K. Sawano, H. Riemann, N. V. Abrosimov, L. Cywinski, D. Bougeard, and L. R. Schreiber, npj Quantum Inf. 6, 40 (2020).
12. B. Paquelet Wuetz, M. P. Lorest, S. Koelling, E. Stein, M. J. Zwerver, S. G. Philips, M. T. Madzik, X. Xue, G. Zheng, M. Lodari et al., arXiv:2112.09606 (2021).
13. E. H. Chen, K. Rie, A. Pan, A. A. Kiselev, E. Acuna, J. Z. Blumoff, T. Brecht, M. D. Choi, W. Ha, D. R. Hulbert, M. P. Jura, T. E. Keating, R. Noah, B. Sun, B. J. Thomas, M. G. Borselli, C. Jackson, T. M. Rakher, and R. S. Ross, Phys. Rev. Appl. 15, 044033 (2021).
14. A. Hollmann, T. Strack, V. Langrock, A. Schmidbauer, F. Schauer, T. Leonhardt, K. Sawano, H. Riemann, N. V. Abrosimov, D. Bougeard, and L. R. Schreiber, Phys. Rev. Appl. 13, 034068 (2020).

Applied Physics Letters 120, 184003 (2022); doi: 10.1063/5.0088576
A typical secondary ions mass spectrometry of our heterostructures is reported in Fig. S13 of Ref. 12. The oxygen concentration in the $^{28}$Si quantum well is $4 \times 10^{17}$ cm$^{-3}$.

The electron temperature $T = 190$ mK is the electron temperature obtained by fitting Coulomb blockade peaks (supplementary material) measured on quantum dot devices fabricated on a similar heterostructure. The electron temperature is higher than the temperature of 70 mK measured by a thermometer located on the mixing chamber of the dilution refrigerator.