A Wide Dynamic Range Read-out System For Resistive Switching Technology

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Abstract—The memristor, because of its controllability over a wide dynamic range of resistance, has emerged as a promising device for data storage and analog computation. A major challenge is the accurate measurement of memristance over a wide dynamic range. In this paper, a novel read-out circuit with feedback adjustment is proposed to measure and digitise input current in the range between 20nA and 2mA. The magnitude of the input currents is estimated by a 5-stage logarithmic current-to-voltage amplifier which scales a linear analog-to-digital converter. This way the least significant bit tracks the absolute input magnitude. This circuit is applicable to reading single memristor conductance, and is also preferable in analog computing where read-out accuracy is particularly critical. The circuits have been realized in Bipolar-CMOS-DMOS (BCD) Gen2 technology.

Index Terms—memristor, wide range, read-out, I-to-V

I. INTRODUCTION

Memristors, known as resistive memory devices, were conceptually proposed by Chua in 1971 [1]. In theory, the resistance of the two-terminal memristor can be adjusted by voltages applied on it. This theory came into reality in 2008 with the birth of the first memristor [2], which works as an access device in a crossbar. Since then, memristors have drawn substantial interest, developing from atomic switches [3] to random resistive access memory (RRAM) [4] and multi-bit memory storage [5]. Besides, on-going tests on employing memristors as electronic synapses_PROCESSORS in neural networks [6] [7] [8] manifest the capability of in-memory computing.

However, challenging issues are still encountered in precisely reading-out the memristor conductance or the current flowing through memristors. Firstly, only a low read voltage can be applied to the memristor to ensure minimal changes to its conductance. Although [5] allows a large read voltage with compensation pulses for the conductance restoration, this approach works only for low-bit precision. Thus most read-outs in analog computing still require a low read voltage. Secondly, memristors have a large current range of multiple orders of magnitude, which is a great challenge for conventional read-out circuits. [9] utilises a transimpedance amplifier (TIA) to provide a virtual ground and realizes I-to-V conversion. However, if the input current is extremely low then the converted voltage is too small to be read with high accuracy; If the current is extremely high, then the TIA cannot guarantee that the virtual ground is stable. Besides, the requirement for reading accuracy is made stricter in neural networks where memristors are performing dot-product calculation [10]. The dot-product in neuromorphic networks implements analog computing, obtaining the exact current value as the result. Recent approaches [11] [12] employ the integrator for I-to-V conversion, but the integrated voltage inevitably reduces the read voltage and jeopardises computing performance. In consequence, a dynamic read-out circuit which can be adaptable to various conductance orders of magnitude is highly desired in memristor applications.

This paper provides a novel method to read out and digitise the input current flowing through the measured memristor with high accuracy and linearity under feedback control. An input current ranging from 20nA to 2mA can be converted to a voltage bounded in an appropriate range. This is achieved by using the logarithmic resistor bank which has 5 logarithmic resistance values corresponding to 5 orders of input current magnitudes. The feedback control can select the most suitable resistor for I-to-V conversion. The converted voltage is amplified to meet the input range of the analog-to-digital converter (ADC) and then be digitised. This read-out method performs an adaptable I-to-V conversion and offers negligible corruption to the read voltage between the measured memristor, minimising error introduced by the measurement circuit. This read-out circuit is a promising candidate in both measuring single memristor conductance and processing of dot-product engine. Section II provides the architecture of the read-out circuit and the principle of design implementation. Section III presents the simulation result analysis and the
circuit layout.

II. DESIGN OVERVIEW

The monolithic circuit (Fig. 1) consists of a memristor to be measured, a resistor bank, a switched capacitor amplifier, a comparator, a digital selector, and an ADC. When the read-out circuit operates, a read voltage \( V_{\text{read}} \) is applied at the top electrode of the measured memristor. The bottom electrode of the memristor is connected to a resistor bank which has 5 logarithmic resistors. The selected resistor is negligible compared to the memristor resistance, minimising disruption to the input current \( I_{\text{in}} = \frac{V_{\text{read}} - V_{\text{bottom}}}{R_{\text{mem}}} \). This resistor bank, with the lowest resistor selected initially, converts the input current to a voltage \( V_{\text{bottom}} = I_{\text{in}} \times R_{\text{bank}} \) which is then amplified by the switched capacitor amplifier. The amplified voltage \( V_{\text{out}} \) needs to be compared with a reference voltage via the comparator, checking if \( V_{\text{out}} \) reaches the input range of ADC. If \( V_{\text{out}} \) is higher than the reference voltage, then \( V_{\text{out}} \) and the selected resistor can be digitised. Otherwise, the digital selector is triggered to activate the selection of the higher resistor. By tuning up the resistance of the resistor bank, a higher \( V_{\text{out}} \) can be obtained and sent to be compared. This process repeats until \( V_{\text{out}} \) is high enough to be digitised.

A. Resistor Bank

The resistor bank (Fig. 2) contains 5 NMOS resistors working in triode region. These resistors offer a dynamic I-to-V conversion. NMOS resistors are preferred than passive resistors due to the following reasons. Firstly, the NMOS transistor does not need extra switches as it intrinsically is a switchable resistor. Thus it can be reliably switched between off-resistance (high) and on-resistance (low) which can be controlled as \( R_{\text{on}} = \mu_n C_{\text{ox}} \left( \frac{W}{L} \right) \left( V_{\text{GS}} - V_{\text{TH}} \right)^{-1} \). Secondly, extra switches are detrimental to the read-out accuracy because the read voltage inevitably decreases due to the voltage drop across the switch. The decrease is significant when the input current is so large that much of the read voltage is applied to this switch. Besides, NMOS resistors occupy less chip area compared to their passive counterpart. Although NMOS transistors are easier affected by foundry process that the practical on-resistance may suffer from fabrication mismatch, NMOS transistors are still suitable resistors in this design. This design does not strictly require the resistance to be absolutely accurate because resistors are used to define dynamic measuring scales. In addition, the deviated on-resistance can be compensated back by varying \( V_{\text{GS}} \) and other calibrations.

By fine-tuning the transistor size, five logarithmic resistance states around R, 10R, 10^2R, 10^3R, 10^4R are required. Only one resistor can be selected at a time and by default the lowest resistor is selected first. Starting from the lowest value, the bottom voltage of the memristor is sent to be amplified and compared. If the amplified voltage is less than the ADC input threshold (157.3mV), the negative comparison result enables the digital selector to work. The digital selector, formed by shift registers, switches off R and switches on 10R. If the comparison result is still negative, 10^2R is selected. This process continues until the positive result is given. The positive result terminates the resistor switching process and outputs the 5-bit resistor number.

B. Switched Capacitor Amplifier

For precisely amplifying the low voltage \( V_{\text{bottom}} \) to a relatively large value thus utilising the full input range of the ADC, a switched capacitor amplifier (Fig. 3) is exploited. A gain around 34 is offered by the capacitor ratio which can be accurately controlled with appropriate sizing and layout.
methodology. Two-phase switches operate to suppress the charge accumulated at the input node of the OTA, minimizing the amplification error. Besides, this amplifier can be directly connected to the resistor bank with negligible interference due to the insulation of the capacitor.

C. 12-bit Analog-to-digital Converter

A 12-bit SAR ADC is designed to digitise the input voltage ranging from 0.1V to 1.7V. This proposed ADC employs a differential architecture and capacitor array bottom-plate sampling to offset and reduce parasitic capacitance. For suppressing the charge/discharge power consumption as well as kickback and thermal noise, a split capacitor array structure with a unit capacitor of $\approx 30fF$ is utilised.

The energy efficiency, conversion speed, and digitisation precision can be substantially improved on each down (discharge) transition. This power saving (37%) is achieved by splitting the most significant bit capacitor into the copy of remaining capacitors [13] with the cost of more control signals needed. The simplified 3-bit comparison between this proposed method and the conventional counterpart is shown in Fig. 4. Take the first conversion as an example, the conventional C2C structure needs to discharge the 4C capacitor ($4CV_{ref}$) and then charges the 2C capacitor ($CV_{ref}^2$), with total power consumption $E_1 = 5CV_{ref}^2$. However, the proposed structure only needs to discharge a 2C capacitor ($E_2 = CV_{ref}^2$) to finish the charge redistribution.

III. Results

A. Memristance-to-voltage Conversion

This section gives the improved current-to-voltage conversion performance. The traditional one-resistor method for I-to-V conversion uses a large resistor if the input current is too small. However, this large resistor inevitably affects the conversion accuracy when the input current is large. To address this issue, the resistor bank is used, showing improved accuracy and linearity explained below.

The improved accuracy is due to the bounded and relatively low voltage level at the bottom terminal of the memristor.

![Fig. 5. Memristance-to-voltage conversion. This work (blue): converted results are between 3mV and 35mV; Conventional design (yellow): extremely low/high converted voltage when input is low/high.](image)

![Fig. 6. Memristance-to-current linearity. Ideally (purple), the converted current is perfectly linear with memristor conductance; This design (blue) drops only a little linearity, and the linearity range is within yellow; The conventional design (orange) greatly loses linearity.](image)

It avoids that the memristor loses much read voltage when the resistor is large. The comparison between employing this proposed resistor bank and using a single 10R NMOS resistor is shown in Fig. 5. With a 0.2V read voltage applied at the top terminal of the measured memristor which varies substantially from 100nS to 5mS, the bottom plate of the memristor is bounded between approximately 3mV and 35mV. This bounded voltage level minimises the variation of voltage drop between the memristor, and reduces the impact of $V_{ds}$ variation on NMOS resistance.

The linearity of memristance-to-current conversion (Fig. 6) is also improved significantly by utilising the resistor bank. Inevitably the practical linearity (blue) is worse than the ideal one (purple) as the voltage drop across the memristor is not exactly $V_{read}$ and it varies with the input. Yellow gives a linearity range of the proposed design, the boundary (upper/lower) is met when $V_{read}$ is 3mV/35mV. The resistor bank can still maintain a high linearity compared to the single
NMOS resistor (orange) which continuously loses linearity with growing memristor conductance.

B. Successive Resistor Control Timing

This section gives the operation of one single read-out process. Fig. 7 presents the successive resistor control in the resistor bank. An example of 355.66nA input is given. In this I-to-V process, $V_{\text{bottom}}$ starts from the lowest value (5.641µV) with the lowest resistance (00001) selected by default. As a 10 times larger resistor (00010) is chosen in next stage, the converted voltage (57.291µV) increases almost 10 times. The amplified voltage also increases as $\Delta V_{\text{out}} = A \times \Delta V_{\text{bottom}}$. In this case, the process continues until the second largest resistor (01000) is controlled. At this moment, the converted voltage (6.031mV) is amplified to 250mV, which is above the threshold voltage 157.3mV and ready for digitisation. Besides, the successive searching time varies from 1 to 5 cycles. Fewer cycles are needed for deciding the resistor if the input current is larger.

C. Full-range Digitisation

This section provides the final result for full-range input currents. Upper of Fig. 8 shows that the amplified output voltage varies between 160.5mV and 1.205V as the input current ranges from 20nA to 2mA. This current range is logarithmically divided into 5 domains with each domain corresponding to a different resistor. Lower of Fig. 8 provides the digitised result which can be used as a look-up table for measuring the input current. Each 12-bit digital output, assisted with a 5-bit resistor representation, reflects one exact input current. Every domain performs similar output ranges, monotonicity and linearity, guaranteeing that the input current can be digitised precisely.

$V_{\text{out}}$ Variability due to process and local mismatch is around 20%. So the input of ADC is set from 0.1V to 1.7V to give extra input margin. In addition, this error can be eliminated in post-calibration.

D. Layout

This section shows the final layout (Fig. 9) of the read-out circuit done in Cadence with TSMC 180nm technology. The height is unified so that the two blocks can be combined and put in the same row/column, paving the path for integrating multiple read-out circuits onto a memristor crossbar.

CONCLUSION

Conventional circuits encountered the issue of reading-out and digitising the wide-ranging memristor conductance/current with high accuracy and linearity. This issue is solved by a novel read-out circuit proposed in this paper. Input currents (20nA-2mA) can be dynamically divided into 5 measuring scales, converted and amplified to voltages (160mV-1.2V), and digitised. This self adjusting read-out circuit significantly reduces errors and non-linearity especially when the measured current is too small or too large. The read-out accuracy and linearity can be further improved with more resistors in the resistor bank with the price of longer operating time and more energy. In summary, this proposed design is promising in memristor based memory and computing which requires large output range and high precision.

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