A new design for 4-bit RCA using quantum cellular automata technology

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Abstract
Since the scaling of transistors is growing rapidly, the need for an efficient alternative for the Complementary Metal-Oxide-Semiconductor (CMOS) technology to obtain further and extra processes in the circuits has been known as the main problem. Over the last decade, Quantum-dot Cellular Automata (QCA) technology has been recognized as a suitable replacement for CMOS technology due to its excellent potential in developing designs with low-power consumption, high speed, and high density. In this regard, lowering the number of gates, the amount of cell count, and delay has been emphasized in the design of QCA-based circuits. As the main unit in logic circuits and digital arithmetic, adders play an important role in constructing various effective QCA designs. In this regard, Ripple Carry Adder (RCA) is a simple form of adders and, due to its remarkable features, can be useful to reach circuits with the minimum required area and power consumption. Therefore, this study recommends a new design for RCA in QCA technology to reduce the cell count, amend the complexity, and decrease the latency. To verify the correctness of the suggested circuit, the QCADesigner-E version 2.0.3 as a well-known simulator has been used. The evaluation results confirm that the proposed design has approximately 28.6% improvement in cell count compared to the state-of-the-art four-bit coplanar RCA designs in QCA technology. Also, the obtained results designate the effectiveness of the advised plan.

Keywords QCA technology · Ripple carry adder · QCADesigner-E · Quantum cost

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1 Introduction

Over the last decades, the Complementary Metal-Oxide-Semiconductor (CMOS) has been a key technology in designing integrated circuits. Since this technology faces many limitations, such as hard lithography, limited power, and short channel effects, researchers have made many efforts to introduce an alternative technology (Majeed et al. 2019). Recently, Quantum-dot Cellular Automata (QCA) has been known as promising nanotechnology and has become a possible replacement for CMOS technology (Bahar et al. 2018). Its main aim is to implement rapid processing and very low power designs for nano-sized circuit systems (Ahmadpour and Mosleh 2020). The designed circuits based on QCA technology have lower power consumption, less occupied area, and lower density (Mosleh 2019). Since the demands for new electronic products with more features are increasing day by day, the importance of density, power consumption, processing power, occupied area, and speed should be considered in the construction and design of this tool (Amirzadeh and Gholami 2020). By positioning QCA cells in suitable architectures, which are able to perform computational functions, QCA-based circuits are designed (Abutaleb 2018; Seyedi and Navimipour 2021a).

In order to construct efficient QCA designs, different logical devices such as sequential circuits (Abdullah-Al-Shafi and Ziaur 2019), adders (Seyedi and Navimipour 2018a), memory (Fam and Navimipour 2019), counter (Divshali et al. 2019), shifter (Divshali et al. 2018), and ALU (Oskouei and Ghaffari 2019) have been developed. Adders are the main and integral parts of any digital information processing system, especially logic and arithmetic unit. Generally, unified hardware with the capability of not only decreasing complexity (cell count) and the area of circuits but also increasing the operation speed is always preferred (Marshal and Lakshminarayanan 2020). Also, Ripple Carry Adder (RCA), as a simple form of an adder, is pretty flexible and straightforward to any desired size (Sasamal et al. 2018; Roshany and Rezai 2019). Nevertheless, these adders are relatively slow because carries may propagate across the full adders. Considering its notable features, it can be useful in designing circuits with the less critical area and power (Labrado and Thapliyal 2016). Since the RCA has gained tremendous importance in improving QCA designs, the current paper aims to introduce a new design of QCA-based RCA. The major contributions of the suggested design are as follows:

- Decreasing the amount of consumed space in RCA designed by QCA technology;
- Reducing the complexity and latency in RCA designed by QCA technology;
- Decreasing the number of cells in RCA designed by QCA technology.

The content of the paper is planned in the following way. The QCA basics and previous works are investigated in the next section. In Sect. 3, a new design of RCA is presented. The simulation results are outlined in Sect. 4. Finally, Sect. 5 specifies some hints for upcoming studies and concludes the paper.
2 Basics of QCA technology

A square nanostructure with four quantum dots and two extra electrons is commonly referred to as a "standard" semiconductor cell. Tunnel barriers connect quantum dots, and each one can only hold one electron (Safaiezadeh et al. 2021). The two electrons in a cell tend to occupy antipodal positions due to Coulombic repulsion. The two states encode binary values “0” and “1”, respectively. In addition, the majority gate and inverter are two basic logic gates in QCA that are produced from these cells and may execute any logic function (Rahmani et al. 2021).

In addition to the items mentioned, the timing adjusts the tunnel walls of cells to govern when they respond to neighbors. For example, a wire with four adjacent clock zones 0, 1, 2, and 3 is constructed in a circle. Relax, Switch, Hold, and Release are the four phases of the clock signals for the clock zones (Seyedi and Jafari Navimipour 2022). A phase shift exists between signals from two adjacent zones. Cells typically accept data at the Switch stage before latching it at the Hold stage. Then, they release the information in the Reveal stage while remaining in a null condition in the Relax stage. As a result, information flows unidirectionally along the QCA wire, with the clock number weighing the propagation delay (Seyedi and Navimipour 2022).

Information transit has become a key challenge with QCA technology since cells can interact with all of their neighbors (Seyedi and Navimipour 2021b). Wire crossing is necessary for the systematic construction of logic circuits in QCA. During the design of complex circuits, binary wires are required to have crossovers in order to lessen the circuit’s complexity. Because of the potential to build co-planner crossovers, single-layer circuit designs using QCA are possible. Coplanar and multi-layer crossovers are the two types of crossovers available in QCA. Multilayer QCA cells’ fabrication capability is still in question, and they are nearly impossible to make. From a practical standpoint, the coplanar crossing is frequently preferred. In this approach, the cells are in a single plane (Seyedi and Navimipour 2021c). There are three techniques to construct circuits with coplanar crossover in QCA. The first approach uses both rotated and simple cells, the second way uses cells from clock zones 0 and 2, and the third method uses cells from clock zones 1 and 3. Multilayer QCA cells’ fabrication capability is still under question, and they are nearly impossible to make (Seyedi et al. 2021).

2.1 Related work

This section aims to review the previous designs in the field of RCA in QCA technology and specify their main features and weaknesses.

The major concepts of QCA and existing logic designs based on QCA technology have been outlined by Chan et al. (2013a). They have studied and implemented the main QCA logic circuits, including a five-input majority gate, three-input majority gate, and inverter. To highlight the practical use of QCA in logic designs, they have proposed a 4-bit RCA using a combined concept from the conventional CLA and RCA using 12 inverters, four five-input majority gates, and 20 three-input majority gates. The suggested 4-bit RCA includes three key blocks, namely, sum block, carry logic block, and propagate and generate a block. They have developed a form of a 4-bit RCA by modifying the carry logic functions by combining three-input and five-input majority gates. The offered adder uses 1246 cells with an area of 1.75 μm² × 1.43 μm², and latency of 5.75 clock cycles.
Also, Chudasama et al. (2018) have proposed an effective structure of $8 \times 8$ Vedic multiplier using urdhva-tiryagbhyam sutra, which has been developed using a structure of $4 \times 4$ Vedic multiplier as the main block and RCA in QCA. Urdhva-Tiryagbhyam refers to a crosswise and vertical method to find the product of two numbers. The proposed design uses one 8-bit full adder, four $4 \times 4$ multipliers, one 3-bit RCA, and one 8-bit RCA. The first 8-bit RCA of multipliers is replaced with an 8-bit full adder to specify the outputs of four $4 \times 4$ multipliers. The suggested $8 \times 8$ Vedic multiplier requires an area of 18.44 $\mu$m$^2$ with 13533 QCA cells and 10.75 clock cycles delay. It requires less cell count and area, but its high complexity remains a problem.

Safoev and Jeon (2018) have utilized a one-bit full adder to present a 4-bit RCA. It has been designed in a multi-layer manner; the layer of the primary cells, in which a majority gate has been placed, and the top layer of the cell, in which an XOR gate has been located. The input and output cells have been placed very smoothly. It means that the proposed design can be simply combined with other circuits. Moreover, the suggested circuit has better performance in terms of time and area size. The proposed RCA requires 184 QCA cells, 0.1 $\mu$m$^2$ area, and 5 clock phases.

Roshany and Rezai (2019) have proposed two novel multi-layer QCA architectures, 1-bit full adder and 4-bit RCA. A new XOR gate architecture has been taken into account to construct the suggested full adder architecture. Moreover, the designed 1-bit full adder has been utilized to develop 4-bit QCA RCA. The outcome of the QCA-Designer tool confirms that the designed architecture for 4-bit multi-layer QCA RCA needs an area of 0.17 $\mu$m$^2$, 125 QCA cells, and 5 clock phases. Moreover, the proposed QCA RCA outperforms previous designs regarding cost, cell count, and area size.

Aiming to improve the number of cells, the area size, and the amount of delay, a novel multi-layer design of QCA-based RCA has been proposed by Seyedi et al. (2019). The proposed RCA has been designed by cascading several 1-bit full adders, which have been presented in Seyedi and Navimipour 2018b. The utilized full adder contains four main components, two inverter gates, a five-input majority gate, and a three-input majority gate. The proposed 4-bit QCA RCA consists of 112 QCA cells with an area of 0.13 $\mu$m$^2$, and a latency of 1 clock cycles.

### 3 Proposed design

In this section, we use a one-bit full adder as a basic module, which has been proposed by Balali et al. (2017). The logical diagram of the full adder is shown in Fig. 1. In cryptography (Narmadha and Balasubadra 2016), the three arithmetic operations (addition, multiplication, and division) in prime and binary extension fields have a variety of applications, including RSA algorithm decipherment (Quisquater and Couvreur 1982), elliptic curve cryptography, Diffie-Hellman key exchange algorithm, and digital signature standard, including elliptic curve digital signature algorithm (Menezes 1993). Adder is one of the

![3-input XOR](image)

**Fig. 1** Logical diagram of the QCA-based full adder in (Balali et al. 2017)
most significant operations (similar to RCAs, Carry save adders, full-adders, and Carry Select Adder). For limited precision operands, many algorithms and hardware implementations are offered (Barker 1994). The most efficient approach is the RCA, which is best suited for use on general-purpose computers. Adders are required for the final reduction step of algorithms, and they make up the majority of the code. In fact, the sum-based adder is recommended to perform the final addition process, and it outperforms other types of adder circuits in terms of multiplication. Moreover, the full adder design by QCA technology with a three-input XOR implemented by explicit interactions and half space between QCA-based cells and 3-input majority gates is illustrated in Fig. 2 (Balali et al. 2017). The full adder is designed by 29 cells in a coplanar layer and uses 0.5 clock cycles to produce outputs with a 0.04 μm² area. It uses conventional QCA-based cells and explicit interactions and half space between QCA-based cells in a coplanar layer. A, B, and Cin denote input cells while SUM and CARRY are output cells.

Actually, full adders and RCA circuits are fundamental units in logic circuits and digital arithmetic. RCA’s layout is designed and implemented simply, but it is quite slow since each full adder has to wait for the calculated carry bit from the previous one. To overcome this problem, we can reduce the delay in RCAs by decreasing the delay of full adders. The structure of the proposed four-bit RCA architecture is shown in Fig. 3. Also, Fig. 4 indicates the proposed four-bit RCA designed with QCA technology, which has used four full adders. To design the RCA QCA-based circuit, we use coplanar-designed technology and direct interactions and half-space between QCA-based cells. Actually, in this design, the
coplanar crossing allows for mono-layered circuits. This circuit is designed with a single layer, and all inputs and outputs are located in one layer. This layer has nine inputs \((A_0-A_3, B_0-B_3, Cin)\) and five outputs \((S_0-S_3, Cout)\). In this scheme, the outputs are not surrounded by other cells, and therefore, they can be accessed easily. In other words, this design does not require a wire to transmit the output signal. Thus, the outputs can easily be fed to another QCA-based circuit’s input.

### 4 Experimental results

A comparative study is done in this section to verify the effectiveness of the proposed RCA circuit. First, the simulation tools and parameters are described, and then the simulation results are investigated.

#### 4.1 Simulation tool

To implement, test, and simulate the proposed four-bit RCA circuit with QCA technology, we used the QCADesigner-E (Patidar and Gupta 2021). Also, to create test vectors, we used “Coherence Vector” and “Bistable Approximation” engines, which have attained identical outcomes (Walus et al. 2004). In addition, QCADesigner-E with the coherence vector (w/ Energy) simulation engine is used to calculate energy usage. The number of majority gates and inverters in any nano communication-based quantum dot circuit determines the overall power dissipated. The loss of information causes energy dissipation. The overall energy dissipation of the recommended RCA circuit is \(6.09e-002\) eV, with an average energy dissipation per cycle of \(5.53e-003\) eV.

#### 4.2 Simulation parameters

Simulation parameters are set at their default values in the QCADesigner-E tool. Table 1 summarizes the QCADesigner-E parameters required to simulate the circuits in QCA technology by “Coherence Vector” and “Bistable Approximation” engines.

#### 4.3 Accuracy analysis and comparisons

Figure 6 illustrates the simulation outcomes of the proposed 4-bit RCA circuit in QCA technology by test vectors for \(A_0, A_1, A_2, A_3, B_0, B_1, B_2, B_3,\) and Cin using the values that
are shown in Fig. 5. Due to a large number of entries in this test, we tested some samples. The output of $SUM_0$ by applying inputs $A_0$, $B_0$, and $Cin$ (these inputs are applied to the circuit at 0.25 clock cycles) after 0.5 clock cycles is marked with the red rectangle in Fig. 6. Moreover, the $SUM_1$ output based on $A_1$ and $B_1$ inputs (applied to the circuit at 1 clock cycle) is produced after 1.25 clock cycles and is indicated with a blue rectangle in Fig. 6. $SUM_2$ output by employing inputs $A_2$ and $B_2$ (these inputs are applied to the circuit at 1.75 clock cycles) is produced after 2 clock cycles and is illustrated by a green rectangle in Fig. 6. Eventually, the outputs of $SUM_3$ and $CARRY$ using inputs $A_3$ and $B_3$ (these inputs are applied to the circuit at 2.5 clock cycles) after 2.75 clock cycles are produced.
and marked with a black rectangle in Fig. 6. The proposed four-bit RCA in QCA technology has 125 cells with a 0.17 μm² area and a latency of 2.75 clock cycles. The results have confirmed by Fig. 6, where the designed four-bit RCA in QCA technology runs completely and provides suitable proficiency.

Also, the measurement outcomes are described in Table 2. The proposed RCA in QCA technology is better regarding complexity, power consumption, and cell count than previous designs. The design owns nearly 28.6% betterment in cell count compared to the best-presented four-bit coplanar RCA designs in QCA technology.

5 Conclusion and future research directions

Over the last decade, to overcome the limitations of CMOS technology, QCA, due to its ability to construct digital circuits with high-speed, high-density, and less energy consumption on the nano-scale has been recognized as a proper replacement. In this regard,
full adders are known as widely used circuits in QCA-based designs. Various types of adders such as RCA can be utilized to obtain circuits with the minimum required area and power consumption. The current paper proposed a new coplanar design of a four-bit RCA aimed to reach a design with less area size, energy consumption, complexity, and QCA cells. We used both “Coherence vector” and “Bistable approximation” simulation engines in QCADesigner-E software to simulate this design. The simulation outcomes using these simulator engines show that the new four-bit RCA design in QCA technology has approximately 28.6% vantage in cell count compared to previous coplanar structures. The proposed RCA circuit in QCA technology can be employed to design n-bit RCA and high-performance QCA technology circuits at the nano-scale. Researchers, engineers, and designers can also use the coplanar crossing, multi-layer crossing, and logical crossing in QCA technology to use the inside cells. Therefore, the proposed scheme can be a fundamental impression of the design of high-speed circuits and other types of adders such as carry save adder and full subtractor.

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**Data availability**  The paper includes all data.

**Declarations**

**Conflict of interest**  The authors declare no conflict of interest.
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