Abstract—The development and validation of an advanced two-level Voltage Source Back-to-Back Converter model, considering its multi-physics operation, is presented in this paper. Based on a set of input parameters, the proposed model evaluates the converter in terms of input current ripples, transient performance, losses, and total volume. The model is discussed separately in three parts: modulation and control analysis, semiconductor loss estimations and heatsink sizing, and passive components sizing, i.e. for the boost inductors and DC-link capacitor. The performance analysis and loss calculations are verified to be accurate using time-domain simulations and experimental loss measurements. Due to its computational efficiency and accuracy, the proposed model is suitable for use within an optimization design environment.

Keywords—Voltage-source back-to-back converters, three-phase ac-ac converter modelling, Inductor modelling, Capacitor modelling

I. INTRODUCTION

To maximize a specific feature or performance, modern system design typically involves an optimization process [1]. In power converter design, the performance indices are often identified as volume, weight, cost, and power loss [2].

Considering the multi-disciplinary nature of power converter operations, its performance is often evaluated using different finite element models. Despite their accuracy, the challenge with this approach lies in its complexity and demand for high computational resources. During an early design phase, analytical models are usually preferred as they are more computationally efficient.

In [3] and [4], systematic modelling approaches are introduced for different three-phase AC-AC converter topologies, with an emphasis on comparing their efficiency and power density. On the other hand, several DC-DC converter topologies are compared in [5], with a modelling framework that also considers cost as a performance criterion. In [6], component models for a three-phase two-level DC-AC converter system are proposed and employed within a system level design tool that optimizes power density.

In motor-drive applications, a widely used converter for AC-AC power conversion is the two-level Voltage Source Back-to-Back Converter (VSBBC) topology [7], as depicted in Fig. 1(a). Despite its popularity, there are only a handful of publications targeting its modelling and design. This paper proposes a comprehensive two-level VSBBC model, as shown in Fig. 1(b), to evaluate its performance, losses and total volume. A modulation and control analysis of the converter is first presented for the calculation of average component currents and transient performances. Semiconductor loss calculations and a suitable heatsink sizing model are discussed next. Finally, sizing methods for the main passive components, i.e. boost inductors and DC-link capacitor, are proposed. To verify the models, time-domain simulations and experimental loss measurements are performed and their results are presented. This proposed model is fast and accurate, allowing it to be incorporated within a motor-drive system optimization design tool [1] [8].

II. INPUT PARAMETER DEFINITIONS

The main input parameters to the converter model are:

\[ D_{\text{in}} \equiv \{D_{\text{grid}}, D_{\text{mach}}, V_{\text{dc}}, f_{\text{sw}}^{(\text{VSI})}, f_{\text{sw}}^{(\text{AFE})}, C_{\text{dc}}, L_{\text{b}}\} \]  

(1)

where \(D_{\text{grid}}\) and \(D_{\text{mach}}\) are grid and machine related parameters, respectively, \(V_{\text{dc}}\) is the DC-link voltage, \(f_{\text{sw}}^{(\text{VSI})}\) and \(f_{\text{sw}}^{(\text{AFE})}\) are the Voltage Source Inverter (VSI) and Active Front End (AFE) rectifier switching frequencies, respectively, \(C_{\text{dc}}\) is the DC-link capacitance, and \(L_{\text{b}}\) is the boost inductance.
III. CONVERTER ANALYTICAL MODELLING

The converter analytical model is described separately in three: 1) modulation and control, 2) losses and thermal management and 3) sizing of passive components.

A. VSBBBC Modulation and Control

In this section, converter modulation and the employed control strategies are considered.

1) Modulation and Current Analysis

Modulation is the process of switching semiconductor devices within a power converter from one state to another. The basic operation and electrical properties of the VSBBBC are significantly determined by its modulation parameters, i.e. modulation index, switching frequency, etc.

Standard modulation schemes are mostly either continuous, such as the symmetrical Space Vector Modulation (SVM), or discontinuous, e.g. DPWM [9]. Fixed switching frequency pulse width modulation (PWM) enables a mathematical representation of the power converter operation, not included here for the sake of brevity [9].

a) Device Average and RMS Currents

The mathematical analysis of converter modulation allows average duty-cycle references over switching period \(d_{ph,ref(S/D)}\) to be calculated and average device currents \(i_{S/D}\) over switching period, can be determined using (2).

\[
i_{S/D}(\theta) = d_{ph,ref(S/D)}(\theta) \cdot i_{ph}(\theta)
\]

where \(i_{ph}\) is the instantaneous phase current and \(\theta\) is the electrical angle. Subsequently, average and rms device currents over fundamental period (\(i_{S/D,avg}\) and \(i_{S/D,rms}\)) can be computed as in (3) and (4).

\[
i_{S/D,avg} = \frac{1}{2\pi} \int_{0}^{2\pi} i_{S/D}(\theta) d\theta
\]

\[
i_{S/D,rms} = \frac{1}{2\pi} \int_{0}^{2\pi} i_{S/D}(\theta)^2 d\theta
\]

Based on (3) and (4), closed-form analytical expressions for \(i_{S/D,avg}\) and \(i_{S/D,rms}\) are derived for different modulation schemes, allowing them to be written as a function of modulation index, peak phase current value, and power factor.

b) Maximum Input Current Ripple

When connecting the AFE rectifier to the grid, boost inductors attenuate the switching ripples present in the input current waveform to ensure power quality compliance with industry standards. These switching ripples are caused by discrete changes in the voltage drop across the boost inductors and at any point in time, peak-to-peak current ripple can be calculated as in (5).

\[
\Delta i_{pp} = \frac{1}{L_p} \int_{0}^{t_{on}} V_L dt
\]

where \(V_L\) is the voltage drop across the inductor applied over a continuous 'turn-on' period of \(t_{on}\).

To simplify the analysis, phase \(a\) current ripple at reference voltage angle \(\theta_g = 0^\circ\) is considered to be maximum. This simplification is justified as inductors are often designed near saturation limits. For a unity input power factor operation, \(\theta_g = 0^\circ\) corresponds to phase \(a\) peak fundamental current, when drop in \(L_p\) from its nominal value, due to magnetic saturation, is expected to be most significant. Consequently, this leads to current ripples typically being largest.

At \(0^\circ\) reference vector angle, \(V_L\) is calculated as in (6).

\[
V_L(0^\circ) = \theta_{pnn} - \theta_s = \frac{2}{3} V_{dc} - \theta_g
\]

(6)

where \(\theta_{pnn}\) is the voltage magnitude when switches \(S_{ph}, S_{nh}\), and \(S_{ac}\) from Fig. 1 are turned on, and \(\theta_s\) is the magnitude of input grid voltage. As determined by the modulation index, \(c\) is calculated using (7).

\[
d_{pnn}(0^\circ) = \frac{\sqrt{3}}{2} M \cos \left(\frac{\phi}{6}\right)
\]

(7)

where \(M\) is the modulation index.

c) DC-link Capacitor RMS Current

For appropriate thermal sizing of the DC-link capacitor, its rms current \(i_{crms}\) is calculated using the analytical method in [10]. For each converter, \(i_{crms}\) is calculated as in (8), assuming a sinusoidal AC current and constant DC-link voltage, neglecting high frequency switching components.

\[
i_{crms} = i_{ph, rms} \left[2M \sqrt{\frac{\sqrt{3}}{4\pi}} \cos^2(\phi) \left(\frac{\sqrt{3}}{8} - \frac{9}{16} M\right)\right]
\]

(8)

where \(M\) is the modulation index and \(\phi\) is the AC side power factor angle. In this work, the worst-case rms current on the VSBBBC DC-link capacitor \(i_{crms}\) is considered to be an average of current ripple harmonics from the AFE and VSI. This is a conservative approach as with appropriate synchronization, their current ripple harmonic contributions can be made to cancel out each other [11].

2) Control of VSBBBC

The simplicity and robustness of a standard VSBBBC control, due to its two-stage conversion, makes it an attractive topology compared to direct AC-AC power conversion topologies [12]. Independent cascaded control schemes are employed for the AFE and VSI, as illustrated in Fig. 2 and Fig. 3. The VSI controller aims to regulate the machine torque and speed while the AFE controller is responsible for maintaining unity power factor at the grid terminals and tracking the DC-link voltage reference.

a) DC-link Voltage Overshoot

In a VSBBBC operation, the DC-link capacitor acts as an energy damper that absorbs or supplies power during output load transients. During a worst-case load transient, which is defined as an externally triggered step removal of rated load, the AFE \(d\)-axis current reference reacts immediately with the
help of a feed-forward power signal, also shown in Fig. 3, causing the AFE controller output to saturate. When this happens, energy stored in the boost inductors continue to flow into the converter, causing the DC-link voltage to rise (or ‘overshoot’).

To calculate the maximum DC-link voltage overshoot \( V_{dc,\text{max}} \) during this period of time, the boost inductors and DC-link capacitor can be considered as an uncontrolled, second-order LC-circuit. Thus, \( V_{dc,\text{max}} \) is calculated as in (9).

\[
V_{dc,\text{max}} = \sqrt{\left(V_{dc} - \sqrt{3} \bar{V}_g\right)^2 + \frac{2L_b}{3C_{dc}} \left(\frac{P_0}{\bar{V}_g}\right)^2 + \sqrt{3} \bar{V}_g} \tag{9}
\]

where \( \bar{V}_g \) is the peak grid input voltage and \( P_0 \) is the output load power that is abruptly removed. It is important to note that these calculations do not account for delays due to sampling and PWM. In practice, \( V_{dc,\text{max}} \) is expected to be slightly higher than calculated in (9).

B. Semiconductor Losses and Heat-sink Modelling

Semiconductor switching devices account for a large portion of the overall VSBBC losses and an adequate cooling system must be in place to dissipate these losses [13]. Semiconductor loss models and a simple heat-sink sizing model is described in this section.

1) Semiconductor Losses

Semiconductor losses are typically considered separately as conduction and switching losses. Conduction losses \( P_{\text{cond}} \) occur during the device ‘on-state’ and are calculated with device average and rms currents from (2) and (3), as in (10).

\[
P_{\text{cond}} = V_f \cdot I_{\text{avg}} + R_{on} \cdot I_{\text{rms}}^2 \tag{10}
\]

where \( V_f \) and \( R_{on} \) are device forward drop and ‘on-state’ resistance obtained by linearizing the manufacturer-provided

\[\text{Fig. 2. Control scheme for VSI driving a PMSM as load.}\]

\[\text{Fig. 3. Control scheme for AFE rectifier powering a resistive load.}\]

On the other hand, switching losses \( P_{sw} \) occur during switching transitions and are a function of the instantaneous switching energy dissipation \( E_{sw} \) and switching frequency \( f_{sw} \), as in (11).

\[
P_{sw} = f_{sw} \int_0^{2\pi} E_{sw}(i_{s/d}(\theta), V_{dc}) \, d\theta \tag{11}
\]

The dependency of \( E_{sw} \) on \( i_{s/d} \) can be found in the manufacturer data sheet while its dependency on \( V_{dc} \) can be modelled based on recommendations from [14].

2) Semiconductor Heat-sink Modelling

For devices housed inside a power module, a two-node Lumped Parameter Thermal Network (LPTN) is employed to describe its thermal behavior. This simplified approach assumes that heat energy is dissipated only in one direction and that devices share the same junction temperature. For a maximum steady-state junction temperature \( T_{j,max} \), the maximum cooling system thermal resistance \( R_{th,sa,max} \) can be calculated as in (12).

\[
R_{th,sa,max} = \frac{T_{j,max} - T_{amb}}{P_{tot}(T_{j,max})} - R_{th,js} \tag{12}
\]

where \( T_{amb} \) is the ambient temperature, \( P_{tot} \) is the total semiconductor losses, and \( R_{th,js} \) is the junction to heat-sink surface thermal resistance.

A forced-air convection cooling system model is developed based on commercially available LA series cooling systems from Fischer Electronics and theoretical relationships in [15]. For a fixed height and length-width ratio, a cooling system’s thermal resistance can be expressed as a function of volume as in (13).

\[
R_{th,sa}(Vo_{lcs}) = \frac{k_{1,hs}}{Vo_{lcs}} + \frac{k_{2,hs}}{\sqrt{Vo_{lcs}}} + \frac{k_{3,hs}}{\sqrt[3]{Vo_{lcs}}} \tag{13}
\]

where coefficients \( k_{1-3,hs} \) are found by performing a curve-fit on manufacturer data. Fig. 4 shows a plot of the volume against thermal resistance relationship for the LA series cooling systems obtained using (13) and compares it against...
that for customized heat-sinks with a Cooling System Performance Index (C SPI) of 17.7 W/Kdm$^2$ reported in [15].

C. Passive Component Modelling

Besides the semiconductor heat-sink, passive components also contribute to a significant portion of the total converter volume. For a VSBBBC system, the main passive components are boost inductors and the DC-link capacitor, which sizings are discussed in this section.

1) Boost Inductor

The soft saturation characteristics of toroidal powder cores makes them an appropriate choice for boost inductor applications. These cores are usually designed assuming thermal, geometrical, and magnetic constraints:

1. Thermal constraints: a minimum wire diameter $\phi_{w,\min}$ is needed for acceptable winding losses and temperature.
2. Geometrical constraints: a maximum number of winding turns $N_{t,\max}$ is set based on the available inner core window area.
3. Magnetic constraints: the powder core material permeability drop characteristics determines the maximum magnetic force $H_{\max}$ allowable in the core, to limit permeability drop due to saturation.

To design the toroidal core inductor, manufacturer data of commercially available cores of a selected material are first compiled into a database. From this data, nominal inductance factor $A_{L0}$ allows the required number of turns $N_t$ for inductance $L_r$ to be calculated for each core:

$$N_t = \frac{L_r}{A_{L0} \gamma_\mu}$$  \hspace{1cm} (14)

where $\gamma_\mu$ is the permeability drop, which can be initially set as 1. Next, the resulting magnetic force $H$ in the core can be determined as in (15).

$$H = \frac{N_t I_L}{I_e}$$  \hspace{1cm} (15)

where $I_e$ is the magnetic path length, and $I_L$ is the rms inductor current. Based on $H$, a new $\gamma_\mu$ can be interpolated from the core material permeability drop characteristics and brought into (14) to calculate a new $N_t$. The process is stopped after a few iterations and the final design is evaluated against $N_{t,\max}$ and $H_{\max}$ constraints.

With the Mega Flux 60 core material (Chang-Sung Corp.) volume of smallest core designs, which are feasible, is plotted against inductance and current in Fig. 5. In this figure, the circled dots represent core designs with the highest inductance-current product per volume $L/I/\text{Vol}_L$. Assuming a thermally limited design with fixed magnetic properties, minimum inductor volume can be modelled as in (16).

$$\text{Vol}_L(I_L, L_r) = (k_{1,\text{L}} I_{L0}^2 + k_{2,\text{L}} I_L + k_{3,\text{L}}) \cdot L_r + (k_{4,\text{L}} I_L^2 + k_{5,\text{L}} L_r + k_{6,\text{L}})$$  \hspace{1cm} (16)

where the coefficients $k_{1-6,\text{L}}$ are found by performing a least squares approximation on core designs with the highest $L/I/\text{Vol}_L$ as found before.

2) DC-link Capacitor

For DC-link applications, polypropylene film capacitors are favorable due to their low dielectric loss tangents and better current ripple tolerances. In this work, manufacturer data for film capacitors of the same material and topological shape are compiled and fitted into a volume model [16]. This volume model is based on energy storage requirements and is a function of capacitance $C$ and voltage $V$, as shown in (17).

$$\text{Vol}_{c,\text{ES}}(C, V) = k_{1,\text{c}} CV^2 + k_{2,\text{c}} CV + k_{3,\text{c}} V + k_{4,\text{c}}$$  \hspace{1cm} (17)

where parameters $k_{1-4,\text{c}}$ are estimated by performing a least mean-square approximation method on manufacturer data.

Meanwhile, minimum capacitor volume, due to thermal constraints, is modelled as in (18).

$$\text{Vol}_{c,\text{thermal}}(C, V, I_{c,\text{rms}}) = \left(\frac{I_{c,\text{rms}}^2 R_{\text{esr}}(C, V)}{k_{\text{c}} P_{\text{perArea}}} \right)^{3/2}$$  \hspace{1cm} (18)

where $R_{\text{esr}}$ is the capacitor’s equivalent series resistance, $P_{\text{perArea}}$ is the heat dissipation per area, and $k_{\text{c}}$ is estimated also by performing a least mean square approximation on manufacturer data.

Lastly, $\text{Vol}_{c,\text{ES}}$ and $\text{Vol}_{c,\text{thermal}}$ are compared and the larger value is determined as the required capacitor volume.

IV. MODEL VALIDATIONS

The converter modulation and control analysis is verified using a time-domain simulation study [17], while semiconductor loss models are validated with loss measurements for a prototype hardware converter. As heatsink and passive component sizing models are based on commercial products, no further verifications are performed.

A. Time-Domain Simulation Study

The simulations are carried out for a VSBBBC driving a PM machine using the PLECS standalone tool and parameters for the study are listed in Table I [18].
Fig. 6(a) shows the start-up response of the motor drive. Initially, at $t = 0.0s$, all controllers are disabled and the modulating pulses to both converters are blocked. The input grid voltage is ramped up from 0 to 100V and the AFE operates in diode rectification mode, charging the DC-link capacitor to about 173V. The AFE is enabled at $t=0.1s$ and it controls the DC-link voltage to a reference value of 200V. Subsequently, the VSI is enabled at $t=0.2s$ at it also controls machine speed to a reference value of 1500rpm. At $t=0.3s$, load torque of 8.5Nm is added to the machine and the converter controls respond instantly to maintain DC-link voltage and speed. Due to the limited bandwidth, a slight dip in rotor speed and DC-link voltage results. Finally, load is removed in a step at $t=0.4s$, simulating a trip of the VSI converter (worst-case transient).

Under rated torque and speed operation, input phase $a$ current can be seen in Fig. 6(b). The peak-to-peak current ripple at 0° reference voltage vector is determined in the converter analytical model as 2.50A, matching well with the simulation which gives 2.44A. The capacitor current is also shown in the figure. The capacitor rms current calculated in the model to be 4.48A while in the simulation it is 4.45A, also revealing a good match.

At $t=0.45s$, when the load is removed, the simulated voltage overshoot and saturation of modulation index can be seen in Fig. 6(c). The converter analytical model computes a maximum overshoot of 202.30V, while the recorded value in the simulation is 203.61V. The small differences are due to PWM delays in the switching model.

### B. Experimental Analysis

To experimentally verify the loss and heatsink thermal model, a prototype converter was built. The semiconductor devices are realized with an Infineon FS50R12KT4B15 power module, which is directly mounted onto a Fischer Electronics LA6 cooling system. Device junction temperatures are measured via NTC thermistors integrated within the power module.

The converter is operated as a VSI to power a resistive-inductive load ($L_{ph} = 3mH$, $R_{ph} = 5.3Ω$). Converter losses are measured at various DC-link voltages, switching frequencies and currents using a Kinetic PPA2530 precision power analyzer. Results from the measurements are shown in Fig. 7.

Initially, loss estimations from the model were found to be significantly lower than measured values. There are several reasons to this: firstly, parasitic DC-link and emitter inductances in the commutation circuit greatly affects switching losses and consequently, real switching energy dissipate in the implemented circuitry can differ from the datasheet specifications. Secondly, the effect of junction temperature on switching losses is not accounted for in the model. Lastly, contact and cable resistances in the test setup can add to the ohmic losses measured.

To take these factors into consideration, device switching energies from (11) are corrected by a factor of 1.5 and ohmic losses due to extra contact resistances of 0.05Ω are included in the model. The corrected loss model, as can be seen in Fig. 7, is significantly more accurate in predicting the converter losses.

![Diagram of Simulated motor drive operation](image)

To verify the thermal models, the cooling system’s thermal resistance is calculated as in (19).

$$R_{th,hs} = (T_j - T_{hs})P_{loss} - R_{th,js}$$  \hspace{1cm} (19)

where $R_{th,js}$ is the junction-to-baseplate thermal resistance provided by the device manufacturer, $T_j$ is the junction
temperature measured using the internal thermistor, and $T_{hs}$ is the heatsink surface temperature measured with a thermocouple. A thermal resistance of 0.25 K/W is obtained from the analytical thermal model, while it is calculated to be 0.28 K/W. This is a reasonable match considering the simplifications made in the thermal model.

V. CONCLUSIONS

This paper presented an advanced VSBBCC model against measurements (before and after correction) for different (a) DC-link voltages, (b) switching frequencies, and (c) phase currents.

ACKNOWLEDGMENTS

This project has received funding from the Clean Sky 2 Joint Undertaking under the European Union’s Horizon 2020 research and innovation programme under grant agreement no. 807081.

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