A smart primary side current sensing strategy for single stage isolated PFC controller

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Abstract: A novel primary side current sensing strategy is presented in this paper, which is especially suitable for the primary side controlled high power factor single-stage flyback LED controller. In order to avoid the constant-current regulation accuracy error caused by electromagnetic interference (EMI) issue, the proposed current sensing technique utilizes the switched-capacitor interleaved sample and hold circuit to obtain the middle point of the primary side current sensing period. The single-stage LED driver utilizing the proposed current sensing scheme has been implemented in CZ6H 0.35um standard CMOS process, simulation results show that load regulation and line regulation accuracy can be improved greatly.

Keywords: flyback, LED driver, PFC, regulation accuracy

Classification: Integrated circuits

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1 Introduction

Recently high-brightness light emitting diode (LED) technology has become more and more attractive due to their some excellent characteristics [1, 2, 3, 4, 5], such as high power efficiency, longevity and low maintenance requirements. One of the popular solutions to precisely regulate LED current constant is the single-stage primary side controlled flyback converter [6, 7, 8], which is more and more adopted in general lighting applications because of its favorable electrical isolation and small compact volume.

The proposed topology shown in Fig. 1(a) is based on the discontinuous conduction mode (DCM) operation of the PFC controller. The output current estimator calculates the output current based on the primary-side sensed voltage signal $V_{CS}$, switching cycle $T_S$ and secondary diode conduction period $T_{OFF}$. The error amplifier $EA$ is utilized to regulate the calculated output current $I_{EST}$ to the pre-set point $I_{REF}$. The PFC controller adjusts the duty ratio of power switch based on the output voltage of error amplifier and line voltage information to obtain both desired output current value and high power factor. According to Reference [1], the ideal average LED output current $I_{LED,AVG}$ can be expressed as

$$I_{LED,AVG} = \frac{1}{\pi} \int_0^{\pi} I_{out}(\theta)d\theta = \frac{1}{\pi} \int_0^{\pi} \left[ \frac{1}{2} \frac{N_P}{N_S} \frac{V_{CS,PK}(\theta)}{R_S} \frac{T_{OFF}(\theta)}{T_S} \right]d\theta$$

(1)

Where $N_P$ and $N_S$ represent primary side transformer [9, 10] turns and secondary side transformer turns, respectively. Variable $T_{OFF}(\theta)$ denotes the secondary diode conduction period and $T_S$ is the switching cycle of the PWM operation.

2 $R_S$ effects on regulation accuracy

Variable $V_{CS,PK}(\theta)$ reflecting the primary-side peak inductor current is usually derived by detecting the potential $V_{CS}$ at the end of power switch turn-on period. However, as shown in Fig. 1(b), because of the fast switch on and off of MOSFET, voltage overshoot and dip at node $V_{CS}$ would occur through the coupling path of...
parasitic capacitance $C_{GS}$, called as the electromagnetic interference (EMI) problem. The interfered sampling voltage $V_{CS,pk}$ is then transferred to the output current estimator, thus, the accuracy of the LED output current [2, 3] is seriously deteriorated. Usually, the resistor $R_G$ is utilized to slow down the switch speed of MOSFET for most of the primary-side controlled LED driver. Fig. 2(a) illustrates the voltage dip at node $V_{CS}$ with different values of $R_G$, which reveals the point that increasing the resistor value of $R_G$ can effectively reduce voltage dip value, however, the total delay time $T_d$ is also increased.

Supposed that the value of $R_G$ is determined, delay time $T_d$ is almost the same for the universal-line input voltage. Different rising slope of inductor current would cause the overshot current $\Delta i_{p, pk}$ not constant in the universal-line system and worsen the line regulation accuracy, which is shown in Fig. 2(b). The expression of overshot current $\Delta i_{p, pk}$ related with line voltage $V_m$ and delay time $T_d$ is obtained as

$$\Delta i_{p, pk} = \frac{V_m |\sin \omega T|}{L_o} T_d$$

(2)

It is obvious that it’s not very feasible to solve the EMI problem by just introducing resistor $R_G$, because line regulation performance is also sacrificed by the longer delay time $T_d$.

3 Middle-point current sensing scheme

Since the voltage dip [4] at $V_{CS}$ is inevitable and the actual peak voltage value is invisible, directly detecting voltage $V_{CS}$ at the end of turn-on period is infeasible. In order to overcome the problem, as shown in Fig. 2(a), this paper proposes a middle-point current sensing (MPCS) scheme, which estimates the primary-side peak current [5, 6, 7] by detecting voltage $V_{CS}$ at the middle point of turn-on period $T_{ON}$. As shown in Fig. 3, the proposed half turn-on period generator is used to obtain the middle sample point of the actual turn-on period of MOSFET. The sample switch $M_S$ turns on in the preceding half turn-on period to sample the voltage $V_{CS}$ and turns off in the subsequent half turn-on period to hold the peak
voltage $1/2V_{CS,Pk}$ at capacitor $C_{HOLD}$. Consequently, at the end of power switch turn on, the sample switch $M_S$ has been completely turned off to avoid the interfered voltage $V_{CS}$ to flow into the hold capacitor $C_{HOLD}$.

Fig. 3. (a) Main concept of the proposed middle-point current sensing scheme. (b) Timing diagram of key waveforms.

Fig. 4. (a) Equivalent AC model with conventional peak current sensing scheme. (b) Equivalent AC model with proposed MPCS scheme.

Since MOSFET and sample resistor $R_S$ are usually off-chip components and the sample switch and hold capacitor are integrated into a chip, the off-chip sample voltage signal $V_{CS}$ must pass through the bonding wire path before flowing into the on-chip sample and hold circuit. Fig. 4(a) illustrates the equivalent AC model at the end of power switch turning on with conventional peak current sensing scheme, the stepped-down signal $V_i$ at the gate of MOSFET regarded as the EMI noise source can be expressed as

$$V_i(t) = -V_p * u(t - t_0)$$  \hspace{1cm} (3)

The transfer function $H(s)$ from $V_i$ to $V_o$ is obtained as

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{sR_SC_{GS}}{(sR_SC_{GS} + 1)(sR_{ON}C_{HOLD} + 1)(s^2L_bC_b + 1)}$$  \hspace{1cm} (4)

Fig. 4(b) illustrates the equivalent AC model at the end of power switch turn on with the proposed MPCS scheme, the noise coupling path has been cut off by the sample switch, thus, the proposed sample and hold circuit can be completely shielded from the EMI noise by the turn-off sample switch.
4 Circuit implementation of the half turn-on period generator

Fig. 5 shows the circuit implementation of the proposed middle turn-on period generator, which utilizes the basic operation principle of interleaved switched capacitor sample and hold circuit. The PWM pulse is converted by clock frequency divider to obtain the alternate odd and even PWM phases, i.e. $\Phi_{\text{odd}}$ and $\Phi_{\text{even}}$.

![Circuit diagram]

**Fig. 5.** Circuit implementation of the proposed half turn-on period generator

In the PWM phase of $\Phi_{[2n-1]}$, $\Phi_{\text{odd}} = 1$ and $\Phi_{\text{even}} = 0$, current source $I_0$ is activated and sensing capacitor $C_{S0}$ is charged, as a result, the sensing voltage $V_{\text{Sam,odd}}$ at the inverted input of comparator COMP linearly rises up, which can be expressed as

$$V_{\text{Sam,odd}}(t_0) = \frac{I_0}{C_{S0}} t_0$$  (5)

Meanwhile, the charge $Q_{H1}$ ($I_0 T_{ON}$) preserved in capacitor $C_{S1}$ in the previous even PWM phase $\Phi_{[2n-2]}$ completes charge-sharing between capacitor $C_H$ and $C_{S1}$ at the initial period of $\Phi_{[2n-1]}$, the potential of the non-inverting input of comparator COMP keeps hold as reference voltage $V_{\text{Hold,odd}}$, which can be expressed as

$$V_{\text{Hold,odd}} = \frac{I_0 T_{ON}}{C_{S1} + C_H}$$  (6)

During the phase of $\Phi_{[2n-1]}$, once the voltage value of $V_{\text{Sam,odd}}$ exceeds that of $V_{\text{Hold,odd}}$, the output of comparator COMP is then instantly triggered to be low voltage level. The trigger instant $t_0$ occurs at

$$V_{\text{Sam,odd}}(t_0) = V_{\text{Hold,odd}}$$  (7)

As a result, the turn-on period $T_{ON,\text{Middle}}$ of signal $\Phi_{\text{Middle}}$ can be expressed as

$$T_{ON,\text{Middle}} = \frac{C_{S0}}{C_H + C_{S1}} T_{ON}$$  (8)

Similarly, in the PWM phase of $\Phi_{[2n]}$, $\Phi_{\text{odd}} = 0$ and $\Phi_{\text{even}} = 1$, the sample node has been transferred to the non-inverted input of comparator COMP and the sample voltage $V_{\text{Sam,even}}$ can be expressed as

$$V_{\text{Sam,even}}(t_0) = \frac{I_0}{C_{S1}} t_0$$  (9)

The hold voltage $V_{\text{Hold,even}}$ during the phase of $\Phi_{[2n]}$ is represented by
\[ V_{\text{Hold\_even}} = \frac{I_0 T_{\text{ON}}}{C_{S0} + C_H} \]  

Thus, in the even PWM phases, the turn-on period \( T_{\text{ON\_Middle}} \) of signal \( \Phi_{\text{Middle}} \) can be expressed as

\[ T_{\text{ON\_Middle}} = \frac{C_{S1}}{C_H + C_{S0}} T_{\text{ON}} \]  

Since all of capacitors \( C_{S0}, C_{S1} \) and \( C_H \) share the same capacity value, accurate proportionality coefficient one-half can be derived by dummy capacitance and cross match technique between the three capacitors.

5 Post-simulation results

The chip is designed and post-simulated with 0.35 um standard CMOS process and Fig. 6(a) shows the layout view of the proposed dc-dc converter, which totally occupies an area of 1.22 mm\(^2\). The proposed PFC controller is designed to drive from five to eighteen LEDs in series with AC input ranging from 85 V to 285 V.

![Layout view of the proposed PFC controller](image)

**Fig. 6.** (a) Layout view of the proposed PFC controller. (b) Overshoot and undershoot phenomenon at node \( V_{CS} \) caused by PWM pulse.

![Steady-state waveforms of inductor current, half turn-on period 1/2T_{ON} and sample and hold voltage 1/2V_{CS,PK}](image)

**Fig. 7.** Steady-state waveforms of inductor current, half turn-on period \( 1/2T_{ON} \) and sample and hold voltage \( 1/2V_{CS,PK} \).

Fig. 6(b) shows the steady-state waveforms of PWM pulse and voltage \( V_{CS} \) in a switching cycle. The rising time \( T_r \) and falling time \( T_f \) of PWM pulse are around 55 ns and 85 ns, respectively. The overshoot trace of voltage \( V_{CS} \) follows with the rising edge of PWM pulse while the undershoot trace follows with the falling edge of PWM pulse. It is sure that the inevitable undershoot voltage with conventional
peak current sensing technique would greatly deteriorate the accuracy of LED current.

Fig. 7 illustrates the waveforms of inductor current, half turn-on period $1/2T_{\text{ON}}$ and sample and hold voltage $1/2V_{\text{CS,PK}}$ in the steady state. Results show that the peak inductor current arrives at 895 mA in the peak waveform, thus, the estimated peak sensed voltage $V_{\text{CS,PK}}$ is calculated at 895 mV ($R_S$ is selected as 1 Ω). Since the turn-on period $T_{\text{ON}}$ of PWM pulse is detected to be around 11.6 us, the expected half turn-on period $1/2T_{\text{ON}}$ should be 5.8 us, which is very close to the actually detected period 5.5 us. As a result, the detected half peak sensed voltage $1/2V_{\text{CS,PK}}$ (439 mV) can well be used to reflect the actual peak voltage $V_{\text{CS,PK}}$. Fig. 8 shows that using the proposed MPCS technique can improve both the line regulation and load regulation greatly.

Table I. Main parameter comparison between the conventional peak current sensing scheme and the proposed MPCS scheme.

| AC input (V) | Peak inductor current at the peak envelope /Expected peak voltage | $T_{\text{ON}}/(1/2T_{\text{ON}})$ | $V_{\text{CS,PK}}/(1/2V_{\text{CS,PK}})$ | Sample error without MPCS/with MPCS |
|--------------|-------------------------------------------------|-----------------------------------|--------------------------------|-----------------------------------|
| 85           | 1.6 A/1.6 V                                     | 12 us/5.6 us                      | 1.415 V/0.772 V               | 11.6%/3.5%                       |
| 140          | 1.36 A/1.36 V                                   | 9.8 us/4.7 us                     | 1.175 V/0.651 V               | 13.6%/4.3%                       |
| 180          | 1.08 A/1.08 V                                   | 7.6 us/3.6 us                     | 0.895 V/0.514 V               | 17.1%/4.8%                       |
| 220          | 0.78 A/0.78 V                                   | 5.8 us/2.7 us                     | 0.595 V/0.370 V               | 23.7%/5.1%                       |
| 285          | 0.56 A/0.56 V                                   | 4.5 us/2.1 us                     | 0.375 V/0.261 V               | 33.1%/6.7%                       |

Table I shows that the sample error with the conventional peak current sensing scheme ranges from 11.6% to 33.1% when the line input voltage rectifying from 85 V to 285 V, which is mainly resulted from EMI noise effect. In the high-line system, the sample error is obviously higher, because the turn-on period $T_{\text{ON}}$ is shorter and the slope of inductor current is larger. Comparatively, the sample error with the proposed MPCS scheme is greatly reduced to from 3.5% to 6.7% when the line input voltage rectifying. It’s evident that the sample error of the proposed
MPCS scheme is much lower than that of the conventional peak current sensing scheme. The main performance comparison between the proposed LED driver with MPCS scheme and other design cases with conventional peak current sensing scheme is illustrated in Table II.

### Table II. Performance summary of the proposed LED driver

| Control method          | Reference [1] | Reference [4] | This paper          |
|-------------------------|---------------|---------------|---------------------|
| AC Input voltage        | 90~265Vac (RMS) | 90~265Vac (RMS) | 90~265Vac (RMS)    |
| Magnetizing inductance  | 1 mH          | 1 mH          | 1.8 mH              |
| Transformer turns-ratio | Np:Ns:Na = 90:30:15 | Np:Ns = 83:28 | Np:Ns:Na = 144:40:27 |
| Operation Mode          | CRM           | DCM           | DCM                 |
| Maximum output power    | 27 V/500 mA   | 25 V/340 mA   | 66 V/310 mA         |
| Switching frequency     | \             | 67 KHz        | 40 KHz              |
| Line regulation accuracy with varied delay time Td | 1.8% @Td = 0.25 us (Without MPCS) | 11.7% @Td = 0.2 us (Without ALC and MPCS) | 1.5% @Td = 0.2 us (With MPCS) |
|                         | 2.2% @Td = 0.5 us | 17.6% @Td = 0.5 us | 2.2% @Td = 0.5 us |
|                         | 4.5% @Td = 1 us (Without MPCS) |                         | 2.6% @Td = 1 us (With MPCS) |

### 6 Conclusions

This paper proposes a smart primary-side current sensing strategy for single stage isolated PFC controller to achieve both high line regulation and load regulation performance. The related theoretical analysis and detailed circuit implementation are illustrated in this paper. The simulation results show that the LED current accuracy can achieve within 3%. As a result, the proposed isolated primary-side controlled LED driver is very suitable for many lighting applications in the universal line supply systems.

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