HELP: Hardware-Adaptive Efficient Latency Prediction for NAS via Meta-Learning

Hayeon Lee1*, Sewoong Lee1*, Song Chong1 Sung Ju Hwang1,2
KAIST1, AITRICS2, Seoul, South Korea
{hayeon926, dltpnd21, songchong, sjiang82}@kaist.ac.kr

Abstract

For deployment, neural architecture search should be hardware-aware, in order to satisfy the device-specific constraints (e.g., memory usage, latency and energy consumption) and enhance the model efficiency. Existing methods on hardware-aware NAS collect a large number of samples (e.g., accuracy and latency) from a target device, either builds a lookup table or a latency estimator. However, such approach is impractical in real-world scenarios as there exist numerous devices with different hardware specifications, and collecting samples from such a large number of devices will require prohibitive computational and monetary cost. To overcome such limitations, we propose Hardware-adaptive Efficient Latency Predictor (HELP), which formulates the device-specific latency estimation problem as a meta-learning problem, such that we can estimate the latency of a model’s performance for a given task on an unseen device with a few samples. To this end, we introduce novel hardware embeddings to embed any devices considering them as black-box functions that output latencies, and meta-learn the hardware-adaptive latency predictor in a device-dependent manner, using the hardware embeddings. We validate the proposed HELP for its latency estimation performance on unseen platforms, on which it achieves high estimation performance with as few as 10 measurement samples, outperforming all relevant baselines. We also validate end-to-end NAS frameworks using HELP against ones without it, and show that it largely reduces the total time cost of the base NAS method, in latency-constrained settings. Code is available at https://github.com/HayeonLee/HELP.

1 Introduction

Neural Architecture Search (NAS) [72, 21, 52, 47, 46, 66, 25], which aims to search for the optimal architecture for a given task, has achieved a huge practical success by overcoming the sub-optimality of manual architecture designs. However, for NAS to be truly practical in real-world scenarios, it should be hardware-aware. That is, we need to search for the neural architectures that satisfy diverse device constraints (e.g., memory footprint, inference latency, and energy consumption). Due to the practical importance of the problem, many existing works propose to take into account the hardware efficiency constraints (mostly latency) in the search process [57, 23, 63, 60, 28, 22, 67, 24, 61].

However, one of the main challenges with such hardware-aware NAS is that collecting training samples (e.g., architecture-latency pairs on each target device) to build reliable prediction models for the efficiency metrics, is computationally costly or requires the knowledge of the hardware devices. Existing hardware-aware NAS methods usually require a large number of samples (e.g., 5k) and train metric predictors for each device from scratch. Additionally, most works [57, 23, 63, 60, 28] are task-specific, and thus such collection of performance samples should be done from scratch, for a new task. Thus, the sample collection process is prohibitively costly when we consider real-world

*These authors contributed equally to this work.
deployment of a model to a large number of hardware devices, for any tasks. OFA [24] alleviate the search cost by utilizing a high-performance network trained on ImageNet as the supernet, which does not require training the models from scratch. Yet, they are still sub-optimal since building device-specific predictors for metric still requires a large number of samples to be collected, to build a layer-wise latency predictor for each device. This could take multiple hours depending on the task and the device, and becomes a bottleneck for latency-constrained NAS. BigNAS [69] considers FLOP as the efficiency metric, but this is a highly inaccurate proxy since latency of an architecture could differ based on its degree of parallelism and memory access cost, for the same FLOP.

To overcome such limitations, we propose a novel sample-efficient latency predictor, namely Hardware-adaptive Efficient Latency Predictor (HELP), which supports the latency estimation for multiple devices with a single model, by allowing it to rapidly adapt to unseen devices with only a few latency measurements collected from each device. Specifically, we formulate the latency prediction problem as a few-shot regression task of estimating the latency given an architecture-device pair, and propose a novel hardware embedding that can embed any devices by utilizing the latencies of the reference architectures on each device as its embeddings. Then, we propose a meta-learning framework which combines amortized meta-learning with gradient-based meta-learning, to learn the latency predictor to generalize across multiple devices, utilizing the proposed hardware embeddings. This allows the model to transfer knowledge learned from known devices to a new device, and thus to achieve high sample efficiency when estimating the latency of unseen devices.

HELP is highly versatile and general, as it is applicable to any hardware platforms and architecture search spaces, thanks to our device-agnostic hardware embeddings. Also, HELP can be coupled with any NAS frameworks to reduce its computational bottleneck in obtaining latency-constrained architectures. Especially, when coupled with rapid NAS methods such as MetaD2A [41], OFA [24] and HAT [61], HELP can perform the entire latency-constrained NAS process for a new device almost instantly. We validate the latency estimation performance of HELP on the NAS-Bench-201 space [31] with various devices from different hardware platforms, utilizing the latency dataset for an extensive device pool in HW-NAS-Bench dataset [43]. The results show that our meta-learned predictor successfully generalize to unseen target devices, largely outperforming baseline latency estimation methods using at least 90× less measurements. Then, we combine HELP with existing NAS methods [24, 61] and show that our meta-latency predictor largely reduce their total search cost.

To summarize, the main contributions of this paper are as follows:

- We formulate the latency estimation of a neural architecture for a given device as a few-shot regression problem, which outputs the latency given an architecture-device pair as the input.
- To represent heterogeneous hardware devices, we propose a novel device-agnostic hardware embedding, which embeds a device by its latencies on reference architectures.
- We propose a novel latency predictor, HELP, which meta-learns a few-shot regression model to generalize across hardware devices, that can estimate the latency of an unseen device using only few measurements. HELP obtains significantly higher latency estimation performance over baselines with minimal total time cost.
- We further combine HELP with existing NAS frameworks to show that it leads to find latency-constrained architectures extremely fast, eliminating the latency-estimation bottleneck in the hardware-constrained NAS.
2 Related Work

Latency Prediction in NAS Hardware-aware NAS [57, 23, 24, 63, 60, 36, 61, 53] aims to design neural architectures that achieve a good trade-off between accuracy and latency for efficient deployment to target devices. While they need to consider the actual latencies of the architectures on a target device, evaluating them while searching for architectures is costly. Thus, most existing works replace it with proxies, such as FLOPs [69], but they are inaccurate measure of latencies. Earlier hardware-aware NAS methods have been used a layer-wise latency predictor (lookup table) [57, 23, 24, 63] which sums up the latencies measured for each operation in the given neural networks. While this is better than FLOPs, they do not accurately capture the complexities of multiple layer execution on real hardware devices. Thus, recent methods use an end-to-end latency predictor [32, 61] that is trained with the latency measurements from the target device, to improve the latency prediction accuracy. BRP-NAS [32], which is a GCN-based model, is currently the state-of-the-art end-to-end latency predictor. However, this method is also limited in that it requires a large number of architecture-latency pairs for each device. Since the latency estimator cannot generalize to a new device, whenever a new device is given, the NAS system needs to build a new latency estimator, which may take hours to finish. The proposed method significantly reduces the total building cost of the latency predictor for each device, by using a single meta-learned predictor and adapting it to a new device with only a few measurements from it.

Meta-learning and Meta-NAS Meta-learning (learning to learn) [58] aims to learn a model that generalizes over a distribution of tasks rather than a single task, such that the model meta-learned over a large number of tasks rapidly adapts to an unseen task. The performance of existing methods [59, 56, 34, 49, 42] is usually evaluated on few-shot classification tasks, where the model classifies between instances of unseen classes given only a few training examples. Recently, several works have proposed to utilize meta-learning for NAS. Most of them focus on few-shot classification tasks to search for the architectures and parameters that can generalize well to a new task [33, 45, 54] with gradient-based meta-learning. However, they have limited practical applicability since the computational cost of meta-learning is prohibitively large, for NAS under a standard many-shot setting. A recently proposed meta-NAS framework with amortized meta-learning, MetaD2A [41], which utilizes a set encoder to encode a task and uses a graph decoder to generate a task-adaptive architecture, obtained state-of-the-art performance on unseen datasets, with minimal search cost. We also propose a similar amortized meta-learning framework, for hardware-adaptive NAS, based on a novel hardware device embedding. However, after obtaining the device-conditioned initialization parameters, we perform further inner gradient steps for device-specific adaptation, unlike MetaD2A [41].

3 Method

Our goal is to design a prediction model that can accurately predict the efficiency metric for a novel architecture-device pair, using a small number of performance samples from the device. While our method is generally applicable to any efficiency metrics that can be measured from the device (e.g. latency, energy consumption, and memory footprint) we focus on the latency prediction in this work.
3.1 Problem Definition

Assume that we are given a task specification \( \tau = \{ h^\tau, X^\tau, Y^\tau \} \) where \( h^\tau \in \mathcal{H} \) is a hardware device, \( X^\tau \subset \mathcal{X} \) is a set of neural architectures, and \( Y^\tau \subset \mathcal{Y} \) is a set of latencies of \( X^\tau \) directly measured on the hardware device \( h^\tau \). Then, our goal is to learn a regression model \( f(x; \theta) : \mathcal{X} \to \mathbb{R} \) parameterized by \( \theta \) that estimates the latency \( y \in Y^\tau \) of a neural architecture \( x \in X^\tau \) for a given hardware device \( h^\tau \) by minimizing empirical loss \( \mathcal{L} \) (e.g., mean squared error) on the predicted values \( f(X^\tau; \theta) \) and actual measurements \( Y^\tau \) as follows:

\[
\min_{\theta} \mathcal{L}(f^\tau(X^\tau; \theta), Y^\tau)
\]

Learning such a regression model seems like a simple problem, since we can collect any number of measurements from any devices. However, this is a more challenging problem than it seems:

1. Since we cannot generalize across devices, we need to learn \( N \) predictors \( \{ f^\tau(\cdot; \theta) \}_{\tau=1}^{N} \) for \( N \) devices, collecting performance samples and training the performance predictor separately for each device, which requires prohibitive computational costs with large number of devices.

2. Even when assuming that we learn a device-specific predictor, in order not to overfit the regression model, we need to collect a large number of architecture-latency sample pairs for each device (e.g. \( 2k \) [61], \( 5k \) [48] samples) to achieve reliable prediction performance.

3. With lack of generalization ability across devices and architectures, the NAS framework needs to repeat the time-consuming sample collection process whenever a new device is given, that may take hours to complete. This will become a computational bottleneck even for a rapid meta-NAS framework such as MetaD2A [41].

To overcome such limitations, we propose a single predictor \( f(\cdot; \theta) \) which can generalize across devices and architectures by fast adapting to a new target device and architecture that are unseen during training, by collecting only a small number of architecture-latency pairs from the device \( (X^\tau \ll X^\tau, Y^\tau \ll Y^\tau) \). We achieve this goal with a meta-learning framework that can transfer knowledge obtained from the device and architecture pool \( \rho(\tau) \).

3.2 Hardware-adaptive Latency Prediction with Device Embeddings

While the measured latency \( y \leftarrow (x, h) \) is dependent on both the device type \( h \) and the architecture \( x \), existing latency prediction models take the form of \( f(x; \theta) \), ignoring the device-specific constraints, since the latency predictor is learned for each device separately. This results in poor performance when learning a single latency predictor to perform metric estimation on multiple devices, including unseen ones, which is our main objective. Thus, we propose hardware-conditioned prediction model:

\[
f(x, h; \theta) : \mathcal{X} \times \mathcal{H} \to \mathbb{R}
\]

that can predict the latency differently depending on the device type \( h \), even for the same architecture \( x \). A crucial challenge of our hardware-conditioned prediction model is how to represent the hardware device \( h \), for all devices regardless of their platform types. This is not a trivial problem since the physical architecture of hardware devices could be very different (e.g. CPU vs FPGA). Thus, we simply consider the device as a black box function which outputs the inference latency given an architecture, instead of directly modeling the hardware devices. Then, we obtain the latencies of the device on a fixed set of reference neural architectures as follows:

\[
V_h = \{ y_1(x_1, h), y_2(x_2, h), ..., y_d(x_d, h) \}
\]

where \( \mathcal{E} \) is the set of the reference neural architectures \( \{ x_1, x_2, ..., x_d \} \subset \mathcal{X} \), fixed across all tasks for both meta-training and meta-test, and \( d \) is the number of the reference architectures; in our experiments, we set \( d = 10 \). Further, \( y_i(x, h) = (y_i(x_1, h) - min(V_h^{(0)}))/(max(V_h^{(0)}) - min(V_h^{(0)})) \) are standardized latency values ranging from 0 to 1, where \( V_h^{(0)} = \{ y_1(x_1, h), y_2(x_2, h), ..., y_d(x_d, h) \} \).

Since this set of reference devices should be representative, we select them to be diverse and heterogeneous. As for the reference architectures, we randomly sample them from the search space. For more detailed descriptions of the reference devices and architectures, please see the supplementary file.

The proposed black-box treatment of hardware devices, and the latency-based hardware embedding allows us to embed a new device without considering its detailed hardware specification.
3.3 Meta-Learning the Hardware-adaptive Latency Predictor

To tackle the few-shot regression problem for multiple devices by utilizing the collected pool of devices and architectures \( p(\tau) \), we propose a novel hardware-adaptive meta-learning framework of the latency predictor that meta-learns \( f(x, h; \theta) \) across a task distribution \( p(\tau) \) to rapidly adapt the predictor \( f(x, h; \theta^\tau) \) to an unseen neural architecture \( x \) given the task specification \( \tau = \{h^\tau, V_h, X^\tau, Y^\tau\} \). During the meta-training phase, we leverage the episodic training strategy, in which we simulate a few-shot regression task for each iteration by randomly sampling task \( \tau \) from the device-architecture pool \( p(\tau) \) and splitting \( \tau \) as training set \( D = \{h^\tau, X^\tau, Y^\tau\} \) and test set \( \tilde{D} = \{h^\tau, \tilde{X}^\tau, \tilde{Y}^\tau\} \) where \( X^\tau \subset X \) and \( \tilde{X}^\tau \subset X \) denote sets of neural architecture samples, \( X^\tau \) is the set of few-shot samples \( |X^\tau| \ll |X| \). Note that there is no overlap between them; that is, \( X^\tau \cap \tilde{X}^\tau = \emptyset \). \( Y^\tau \subset Y^\tau \) and \( \tilde{Y}^\tau \subset Y^\tau \) denote the sets of corresponding latency values of neural architectures \( X^\tau \) and \( \tilde{X}^\tau \), measured on device \( h^\tau \), respectively. Basically, for each task \( \tau \), we obtain the hardware-adaptive prediction model \( f(X, V_h^\tau; \theta^\tau) \) as a function of \( V_h^\tau \). Formally, we meta-train the latency predictor to minimize the test loss \( L(\cdot; \tilde{D}^\tau) \) by optimizing the following task-adaptive meta-learning objective:

\[
\min_{\theta} \sum_{\tau \sim p(\tau)} L(f(\tilde{X}^\tau, V_h^\tau; \theta^\tau), \tilde{Y}^\tau) \quad (4)
\]

We can simply use the task embedding \( V_h^\tau \) to obtain a task-conditioned latency predictor, in which case we are using an amortized metalearning framework similar to one proposed in Lee et al. [41], which aims to meta-learn a dataset-adaptive performance predictor and a NAS framework. However, we can further perform few-shot adaptation with the few latency measurements collected from the target device, by conducting inner gradient updates with them as follows:

\[
\theta^\tau_{t+1} = \theta^\tau_t - \alpha \nabla_{\theta^\tau_t} L(f(X^\tau, V_h^\tau; \theta^\tau_t), Y^\tau) \quad \text{for} \quad t = 1, \ldots, T \quad (5)
\]

where \( t \) denotes the \( t_{th} \) inner gradient step, \( T \) is the total number of inner gradient steps, and \( \alpha \) denotes the multi-dimensional global learning rate vector [44]. This meta-learning formulation allows us to adapt to a new device rapidly, by using the knowledge of the devices used for meta-training. However, when we are encountered with a completely new device that has little relatedness to any devices from the meta-device pool, it will be helpful to deviate more from the meta-knowledge captured by \( \theta^\tau_{(0)} \) [40]. To this end, we introduce a hardware-adaptive modulator \( z^\tau = g(V_h^\tau; \phi): \mathbb{R}^d \rightarrow \mathbb{R}^{dz} \) parameterized by \( \phi \) to modulate the initial parameter as \( \theta^\tau_{(0)} = \theta \ast z^\tau \), where \( \theta^\tau_{(0)} \) is the new initialization for hardware \( h^\tau \). Following [40], we set \( \theta^\tau_{(0)} \leftarrow \theta \ast z^\tau \) for weights and \( \theta^\tau_{(0)} \leftarrow \theta + z^\tau \) for biases with an element-wise multiplication operator \( \ast \). This leads to the following update rule:

\[
\theta^\tau_{(0)} = \theta \ast z^\tau \quad (6)
\]

\[
\theta^\tau_{t+1} = \theta^\tau_t - \alpha \nabla_{\theta^\tau_t} L(f(X^\tau, V_h^\tau; \theta^\tau_t), Y^\tau) \quad \text{for} \quad t = 1, \ldots, T \quad (7)
\]

where \( T \) is the number of inner gradient steps. Then, the final meta-learning objective is as follows:

\[
\min_{\theta, \phi} \sum_{\tau \sim p(\tau)} L(f(\tilde{X}^\tau, V_h^\tau; \theta^\tau_{(T+1)}), \tilde{Y}^\tau) \quad (8)
\]

Thus, we meta-learn both the model parameters for the hardware-adaptive latency predictor, and the modulator for the shared initial parameters.

**Few-shot Adaptation to Unseen Devices (Meta-Test)** We now describe how to use our meta-learned latency prediction model \( f(\cdot; \theta) \) to estimate the latency of an architecture on a novel device \( h^\nu \) that is unseen during meta-training. The task-specific predictors [61, 24, 48] need a large amount of latency measurements from an unseen device \( h^\nu \), over diverse architectures in order not to overfit, which may take an excessive time to collect. However, our model is able to measure the latency values \( y^\nu \) of a new architecture \( \tilde{x}^\nu \) by collecting only few latency measurements from it (we use 10 or 20), using the device-conditioned meta-learning. Given a latency prediction task of an architecture \( \tilde{x}^\nu \) on a novel device \( h^\nu \), \( \nu = \{h^\nu, X^\nu\} \), we first obtain its hardware device embedding \( V_h \) by obtaining its latencies on a fixed set of reference architectures, following Equation (3). Then we use the device embedding \( V_h \) to obtain the device-optimized parameters of the latency predictor \( \theta^\nu_{(T+1)} \), following Equation (6) and (7). Then, we use the device-optimized latency predictor \( f(\cdot, V_h^\nu; \theta^\nu_{(T+1)}) \) to measure the latency of \( \tilde{x}^\nu \). We can further combine this meta-latency predictor with a NAS method to perform latency-constrained NAS for a novel device.
Figure 3: Latency estimation performance as a function of the number of samples collected.

Computational Complexity of HELP. The meta-training of the latency predictor is done only once, and once done, we can adapt the meta-latency estimator for the latency estimation of any number of devices. Since conventional approaches require to collect a large number of samples and train a device-specific latency estimator for each target device, while HELP only needs to collect 10 samples per device. HELP reduces the time complexity of obtaining latency estimations from $O(DN)$ to $O(D)$, where D is the number of devices and N is the number of samples to sufficiently train each latency estimator.

4 Experiment

In this section, we first verify the efficacy of our meta-learning scheme on the latency prediction of architectures on unseen devices, in Section 4.1. In this section, we also validate the sample-efficiency and the performance of HELP against existing latency prediction models, and a predictor trained with conventional meta-learning. Then, in Section 4.2, we validate HELP’s effectiveness and efficiency on the full latency-constrained NAS for novel devices, by combining it with existing NAS methods.

Search Space Following the evaluation procedure of HW-NAS-Bench [43], we consider two search spaces, NAS-Bench-201 [31] and FBNet [63]. Additionally, we consider MobileNetV3 [36, 24] and HAT [61] search space for end-to-end latency-constrained NAS in Section 4.2. For a detailed description, refer to the supplementary file.

Meta-Training Pool/Meta-Test Pool To construct the Meta-Training Pool, we collect the latency measurements from 18 heterogeneous devices, including GPUs, CPUs, mobile devices (NVIDIA 1080ti, Titan X, Titan XP, RTX 2080ti, Xeon Silver 4114, Silver 4210r, Samsung A30, S7, Google Pixel3, Essential Ph 1). For GPUs, we consider three different batch sizes [1, 32, 256(64)] and for all other hardware devices, we use the batch size of 1. We collect 900/4000 (architecture, latency) pairs of each training device for NAS-Bench-201 and FBNet search space, respectively. As for the Meta-Test Pool, we consider Unseen Devices and Unseen Platforms. Unseen Devices include NVIDIA GPU Titan RTX, Intel CPU Xeon Gold 6226, and Google Pixel2, which are different from the devices in the meta-training pool but belong to the same categories (GPU, CPU, mobile device). On the other hand, Unseen Platforms include Jetson AGX Xavier, Raspi4, ASIC-Eyeriss, and FPGA, which are completely unseen categories of devices. For Raspi4, ASIC-Eyeriss, FPGA and Pixel3, we use the latency measurements provided in the HW-NAS-Bench [43]. For the implementation details of our model, please refer to the supplementary file.

Baselines We compare our framework against relevant baselines. 1) MAML [34]: A few-shot regression baseline which meta-learns the initial parameters over multiple tasks via bi-level optimization. 2) Meta-SGD [44]: An extension of MAML with the meta-learned learning rate for the inner-gradient step. 3) ANP [39]: A few-shot regression model implemented with Attentional Neural Processes, which uses differentiable attentions to attend to the relevant contexts for the given query. 4) BRP-NAS† [32]: A predictor-based NAS method with a graph convolution neural network-based latency predictor. This baseline achieves the previous state-of-the-art performance on latency prediction in the NAS-Bench-201 search space. 5) MetaD2A [41]: This is a meta-NAS framework without a latency predictor which enables rapid architecture search (a few GPU seconds) for unseen datasets, which obtains state-of-the-art performance on multiple datasets in the NAS-Bench-201 search space.

† For experiment on LatBench provided by BRP-NAS, please refer to the supplementary file.

| Method | Unseen Platform | Architecture Search Cost | Latency Estimator Building Cost |
|--------|-----------------|--------------------------|-------------------------------|
| MAML [34] | | O(DN) | O(DN) |
| ANP [39] | | O(D) | O(D) |
| Meta-SGD [44] | | O(D) | O(D) |
| HELP (Ours) | | O(D) | O(D) |

Table 1: Cost of NAS and latency estimation.

| Method | Task-specific NAS | + Few-Shot Adapt | + HW-Condition | Amortization |
|--------|-------------------|------------------|---------------|-------------|
| HELP (Ours) | 0.568 | 0.539 | 0.568 | 0.568 |
| MetaD2A [41] | 0.853 | 0.861 | 0.872 | 0.885 |
| MetaD2A + HELP | 0.904 | 0.889 | 0.913 | 0.942 |

Table 2: The correlation of the estimated latency with HELP to the actual latency, on unseen devices with 10 measurement samples from each device (FBNet space).
Table 3: Comparison of the latency estimators on unseen devices and platforms on NAS-Bench-201.

| Method                        | Transfer | Sample | Unseen Device | Unseen Platform |
|-------------------------------|----------|--------|---------------|-----------------|
|                               |          |        | GPU        |      | CPU       |   | Pixel2   |   | CPU      |   | Pixel2   |   | Mean   |
| FLOPS                         |          | -      | 0.950      | 0.846 | 0.826    | 0.765 | 0.437  | 0.900 | 0.787 |
| Layer-wise Predictor          |          | -      | 0.667      | -    | 0.866    | -    | -      | -    | 0.767 |
| BRP-NAS [32]                  |          | 900    | 0.814      | 0.847 | 0.796    | 0.666 | 0.811  | 0.801 | 0.789 |
| BRP-NAS (+extra samples)      |          | 3200   | 0.822      | 0.853 | 0.805    | 0.693 | 0.830  | 0.828 | 0.805 |
| HELP (Ours)                   | ✓        | 10     | 0.987      | 0.890 | 0.989    | 0.802 | 0.940  | 0.985 | 0.932 |

Figure 4: Comparison of the estimated and measured latencies on a Titan RTX GPU and Intel Xeon Gold CPU. While BRP-NAS requires 900 samples to train the latency predictor, our meta-latency predictor requires only 10 samples for adaptation, and significantly outperforms it in the estimation performance.

4.1 Efficacy of HELP on Few-shot Latency Estimation for Novel Devices

We first validate whether the transferring the meta-knowledge obtained over a meta-training pool to an unseen meta-test device helps to improve the sample efficiency and prediction performance of the latency predictor. We adapt the meta-latency predictor on 10 architecture-latency pairs of 6 unseen meta-test devices, and report the Spearman’s rank correlation (higher the better) between the estimated latencies and actual latencies on 1,000 neural architectures from the test set in FBNet search space, over 5 random runs. (Figure 3, Table 2, and Figure 5).

Latency Estimation Performance for Unseen Devices Figure 3 reports the average value of correlation scores of different predictors as a function of the number of architecture-latency pairs from meta-test devices. Shaded regions are the range of standard deviation of 5 runs with random seeds. HELP and Meta-SGD uses the initial parameters that are meta-learned over a large meta-training pool, and fine-tunes its parameter with given training samples. On the other hand, Scratch means to simply train a regression model from scratch with a given samples. The result shows that using meta-knowledge (HELP and Init. of Meta-SGD) consistently outperforms the model trained from scratch. Specifically, HELP’s latency predictor with hardware-adaptive initial parameter \( \theta_0 \) achieves significantly larger performance gain over baselines when the number of samples is smaller (e.g., 10 and 50). Such sample-efficiency allows HELP to search for architectures that satisfy the latency constraints with orders of magnitudes shorter time compared to existing methods.

Effect of the Hardware-adaptive Meta-learning We analyze the effect of hardware-adaptive meta-learning in Table 2. We observe that the meta-latency predictor using the proposed modules largely outperforms the other ones trained with other meta-learning baselines that are hardware-independent, which shows the effectiveness of our hardware-adaptive meta-learning on unseen platforms. This is due to the heterogeneity of the tasks (devices) in the meta-training dataset, in which the task-conditioning becomes more important.

Effect of the Size of the Device Pool We further analyze the effect of the size of the meta-training pool, on the performance of the meta-latency predictor. Figure 5 reports the performance of our latency predictor over different sizes of the randomly sampled device pool. In particular, when the number of devices in the meta-training pool is 10 or more, our model achieves over 0.9 correlation on unseen devices using only 10 samples of the unseen target device, regardless of the device types of the meta-training pool. Contrarily, Meta-SGD does not yield meaningful performance gains even with large meta-training pools.

Sample-efficiency of HELP To demonstrate the sample-efficiency of our meta-learned latency predictor, we compare against three baselines: 1) a proxy predictor using number of FLOPs 2) a layer-wise predictor and 3) the latency predictor from BRP-NAS [32] (Table 3 and Figure 4). The results show that FLOPs, although easy to compute, is an inaccurate proxy for latency estimation.
Table 4: Performance comparison of different latency estimators combined with MetaD2A for latency-constrained NAS, on CIFAR-100 dataset with NAS-Bench-201 search space. For the building time and the total NAS cost of MetaD2A+HELP, we report only time and cost during the meta-test time. The meta-training time of HELP is 25 hours and the time to meta-train the MetaD2A is 46 GPU hours, which is conducted only once across all unseen devices.

| Device          | Model                                      | Const (ms) | Latency (ms) | Accuracy (%) | MACs (M) | Latency Model Building Time | Total NAS Cost (Wall Clock) | Speed Up |
|-----------------|--------------------------------------------|------------|--------------|--------------|-----------|-----------------------------|----------------------------|----------|
| Unseen Device   | MetaD2A + BRP-NAS [32]                      | 14         | 14           | 66.9         | 79        | 10                          | 120s                       | 1.0      |
|                 | MetaD2A + HELP (Ours)                      | 22         | 19           | 70.6         | 55        | 10                          | 125s                       | 9.8      |
|                 | MetaD2A + Layer-wise Pred. (Ours)          | 34         | 34           | 73.5         | 185       | 10                          | 125s                       | 9.8      |
| Google Pixel2   | MetaD2A + BRP-NAS [32]                      | 13         | 67.4         | 47           | 10        | 25s                         | 1220s                      | 1.0      |
|                 | MetaD2A + HELP (Ours)                      | 13         | 70.6         | 55           | 10        | 25s                         | 125s                       | 9.8      |
|                 | MetaD2A + Layer-wise Pred. (Ours)          | 34         | 34           | 73.5         | 185       | 10                          | 125s                       | 9.8      |
| Unseen Device   | Titan RTX (Batch 256)                       | 25         | 23           | 70.7         | 82        | 10                          | 125s                       | 9.8      |
|                 | MetaD2A + BRP-NAS [32]                      | 21         | 19           | 71.5         | 55        | 10                          | 125s                       | 9.8      |
|                 | MetaD2A + HELP (Ours)                      | 21         | 19           | 71.6         | 55        | 10                          | 125s                       | 9.8      |
|                 | MetaD2A + Layer-wise Pred. (Ours)          | 34         | 34           | 73.5         | 185       | 10                          | 125s                       | 9.8      |

Figure 6: The accuracy-latency trade-off of the NAS framework with an oracle accuracy predictor, combined with the oracle latency estimator (yellow star), BRP-NAS (green square), layer-wise predictor (blue triangle), and HELP (Ours - red circle), on various devices in NAS-Bench-201 space. HELP, with its accurate latency estimation, obtains Pareto-frontier models, while baselines yield sub-optimal architectures.

The layer-wise predictor also achieves poor performance, because it cannot reflect the complexity and the holistic effect of the network architecture. The latency predictor from BRP-NAS [32], which is a 4-layer GCN with 600 hidden units followed by a fully connected layer to produce a scalar output, achieves significantly better estimation compared to the first two baselines. However, this model requires 900 samples from each architecture-device pair, as described in [32]. Finally, our HELP predictor achieves the best performance, achieving the Spearman’s rank correlations of 0.987 on GPU and 0.989 on CPU, using only 10 latency measurements of the architecture on each device. This shows the clear advantage of our method, in terms of the estimation accuracy and sample-efficiency.

4.2 End-to-end Latency-constrained NAS with HELP

To show that HELP does help NAS frameworks rapidly obtain latency-constrained/optimal architectures for a novel device, we combine HELP with existing NAS methods, namely MetaD2A [41], OFA [24] and HAT [61], and validate the performance on the latency-constrained NAS tasks.

In Table 4 and Table 5, besides latency and accuracy, we additionally report the time-efficiency of the latency estimators with three different measures. First, we use the number of samples which are the number of architecture-latency pairs obtained from the target device, that are used to build or train the latency estimator. We also report the building time, which is the total wall clock time to build the latency estimator, including the time required for sample collection, architecture compilation on the target devices, transmitting the architecture to the target device, and measuring the latency on the device. Finally, we report the total NAS cost, which is the sum of both the estimator building time and the architecture search time, on a target task. After obtaining the architecture, we measure the actual latency of the architecture on the target device and report it as latency (ms). For the building time and the total NAS cost, we exclude the cost of any procedures that are not done during the meta-test time, such as the meta-training of MetaD2A model (46 GPU hours) and HELP (25/18 hours for MetaD2A and OFA), as well as the time to train the supernet for OFA (1,200 GPU hours).

We first combine HELP with MetaD2A and compare it with the MetaD2A combined with other latency predictors. We conduct NAS on NAS-Bench-201 [31] benchmark for the CIFAR-100 dataset,
Table 5: The results of the latency constrained-NAS experiment for ImageNet-1k with MobileNetV3 search space. For the building time and the total NAS cost of OFA+HELP, we report only time and cost during the meta-test time. The meta-training time of HELP is 18 hours and the time to train the supernet for OFA is 1,200 GPU hours, which is conducted only once across all unseen devices.

| Device | Model | MACs (M) | Latency (ms) | Accuracy (%) | Latency Model Building Time | Total NAS Cost (Wall Clock) | Speed Up |
|--------|-------|----------|--------------|--------------|----------------------------|-----------------------------|----------|
| Unseen Device Titan RTX (Batch 64) | MobileNetV3-Large [36] | 219M | 22.1 | 75.2 | - | - | - |
| | MnasNet-A1 [57] | 312M | 20.0 | 75.2 | 8k | 4.5h | 40,004.5h | 1.0x |
| | FBNet-C [61] | 375M | 27.5 | 74.9 | 7.5k | 4.2h | 580.2h | 69x |
| | ProxylessNAS-GPU [23] | 465M | 22.0 | 75.1 | 5k | 2.8h | 502.8h | 80x |
| | OFA+Layer-wise Pred. [24] | 397M | 21.5 | 76.4 | 27k | 15h | 15h | 2667 |
| | OFA + HELP (20ms) | 230M | 20.3 | 76.0 | - | - | - |
| | OFA + HELP (23ms) | 268M | 23.1 | 76.8 | 10 | 26s | 0.007h | 5.7Mx |
| | OFA + HELP (28ms) | 366M | 28.6 | 77.9 | - | - | - |
| Unseen Platform Intel Xeon Gold 6226 | MobileNetV3-Large [36] | 219M | 132 | 75.2 | - | - | - |
| | MnasNet-A1 [57] | 312M | 212 | 75.2 | 8k | 35.6h | 40,035.6h | 1.0x |
| | FBNet-B [63] | 295M | 212 | 74.1 | 7.5k | 33.3h | 609.3h | 66x |
| | ProxylessNAS-CPU [23] | 465M | 200 | 75.1 | 5k | 22.2h | 522.2h | 77x |
| | OFA+Layer-wise Pred. [24] | 301M | 167 | 74.6 | 27k | 120h | 120h | 334x |
| | OFA + HELP (170ms) | 336M | 147 | 77.6 | 20 | 300s | 0.008h | 0.5Mx |
| | OFA + HELP (190ms) | 375M | 171 | 78.1 | - | - | - |
| Unseen Platform Jetson AGX Xavier (Batch 16) | MobileNetV3-Large [36] | 219M | 70.8 | 75.2 | - | - | - |
| | MnasNet-A1 [57] | 312M | 71.6 | 75.2 | 8k | 24.9h | 40,024.9h | 1.0x |
| | ProxylessNAS-GPU [23] | 465M | 82.6 | 75.1 | 5k | 15.6h | 515.6h | 78x |
| | OFA+Layer-wise Pred. [24] | 349M | 69.2 | 75.8 | 27k | 84h | 84h | 476x |
| | OFA + HELP (65ms) | 243M | 67.4 | 75.9 | - | - | - |
| | OFA + HELP (70ms) | 279M | 76.4 | 76.7 | 10 | 112s | 0.03h | 1.3Mx |

Figure 7: HELP reduces the total NAS cost by 2140x on Titan RTX. The total NAS cost is represented on a log-scale.

In Table 5, we validate HELP on a large-scale dataset, ImageNet [29], against state-of-the-art NAS methods. In this experiment, we only consider GPUs with various batch sizes (1, 32, 64) as the meta-training devices, and Titan RTX GPU, Xeon CPU and Jetson Edge GPU as unseen devices. We combine HELP with OFA by training the accuracy predictor on the pre-trained OFA network, and conducting predictor-guided evolutionary architecture search to fit the latency constraint. The result shows that, while searching for competitive architectures, HELP significantly reduces the total NAS cost of the baseline NAS methods which builds a new latency estimator for each target device. Figure 7 shows that OFA+HELP reduces the total NAS cost on a target device by 2140x, when compared with the OFA + layer-wise predictor. This allows us to benefit from the rapid search speed of OFA, since the total NAS cost is only tens or hundreds of seconds, while the OFA + layer-wise predictor takes 15 hours, which is impractical. The details of the searched architectures are provided in the supplementary file.

ProxylessNAS has roughly 42 unique blocks (7 different operations per 6 different input shapes) and use 5k architecture samples to build a layer-wise latency predictor. Thus, we proportionally estimate the number of samples to train its latency estimator for the FBNet and OFA supernet as 7.5k and 27k, which have 63 and 225 unique blocks, respectively. MnasNet does not have a latency estimator, but directly measures the latency of every architecture in the search process (8k architectures).

Hardware-aware Transformer Architecture Search To demonstrate the task-level generality of HELP, we further conduct end-to-end latency-constrained Transformer architecture search experiments on machine translation task, WMT’14 En-De, by combining HELP with HAT [61], which is hardware-aware NAS method for Transformer. For WMT’14 En-De, we follow [61, 64] for training.

Supplementary File For more results on various devices, please check the supplementary file.
Table 6: Results of hardware-aware Transformer architecture search on WMT’14 En-De. By combining HAT with HELP, 200 × fewer samples are used to train latency predictor while achieving competitive performance.

| Target Device        | Model                     | Constraint | Latency    | Number of Samples | BLEU score |
|----------------------|---------------------------|------------|------------|-------------------|------------|
| Unseen Device        | HAT+End-to-End Pred.      | 90ms       | 73.9ms     | 2000              | 27.08      |
|                      | HAT+HELP (Ours)           | 90ms       | 74.0ms     | 10                | 27.19      |
|                      | HAT+End-to-End Pred.      | 150ms      | 108.4ms    | 2000              | 27.04      |
|                      | HAT+HELP (Ours)           | 150ms      | 106.5ms    | 10                | 27.44      |
| GPU NVIDIA Titan RTX | HAT+End-to-End Pred.      | 200ms      | 159.6ms    | 2000              | 27.20      |
|                      | HAT+HELP (Ours)           | 200ms      | 159.6ms    | 10                | 27.20      |
|                      | HAT+End-to-End Pred.      | 400ms      | 369.4ms    | 2000              | 28.09      |
|                      | HAT+HELP (Ours)           | 400ms      | 343.2ms    | 10                | 27.52      |
| Unseen Platform      | HAT+End-to-End Pred.      | 200ms      | 159.6ms    | 2000              | 27.20      |
|                      | HAT+HELP (Ours)           | 200ms      | 159.6ms    | 10                | 27.20      |
|                      | HAT+End-to-End Pred.      | 400ms      | 369.4ms    | 2000              | 28.09      |
|                      | HAT+HELP (Ours)           | 400ms      | 343.2ms    | 10                | 27.52      |

validation, test setting of datasets. The meta-training device pool is configured only with GPUs such as NVIDIA Titan X, 1080ti, 2080ti, and the unseen devices are Titan RTX GPU and Intel Xeon CPU. As a baseline model, we train the end-to-end latency predictor (End-to-End Pred.) using 2000 architecture-latency pair samples for each device following HAT [61]. Table 6 shows the results of NAS with different latency constraints, and BLEU score of searched models. HAT+HELP, which replaces a latency predictor of HAT with HELP, successfully obtains the competitive Transformer models while using 200 × fewer samples for training latency predictor than the original HAT.

5 Discussion

Limitation The proposed hardware-conditioned meta-learning framework allows HELP obtain an optimal latency-constrained network within few seconds, when combined with rapid NAS methods such as [41, 24, 61], since building a latency estimator is often a bottleneck for them. However, combining HELP with slower NAS methods based on RL, gradient-based search, and evolutionary algorithms will be less effective since the total NAS cost is dominated by the architecture search cost, rather than the time required to build the latency estimator. Yet, since mainstream NAS research nowadays is focusing more on the reduction of the architecture search cost [52, 47, 30, 24, 41], we believe that the latency estimation will become more of a bottleneck, and our sample-efficient latency estimator will become even more useful for latency-constrained NAS.

Societal Impact Since our method requires to build a meta-training pool only once, and meta-latency estimator can rapidly adapt to a new device with as few as 10 samples, we can largely reduce the waste in the computational resources required for obtaining the latency measurements. Since the repeated measurements require large energy consumption that also yields high CO2 emissions, and reduce devices’ lifetime, our method is more environment-friendly than existing methods that require a large number of measurements from each device.

6 Conclusion

We proposed a novel meta-learned latency predictor, that can estimate the latency of an architecture on a novel device, using only a few measurements from it. While conventional latency prediction methods are inefficient since they cannot generalize across devices, and require a large number of latency measurements for each device, our latency predictor is meta-learned to rapidly adapt to an unseen device by utilizing the meta-knowledge accumulated over a device pool. Using a novel hardware embedding function that embeds each device based on its latencies on a set of reference architectures, we conducted hardware-conditioned meta-learning to obtain a device-specific initial parameters, and further took inner gradient steps to adapt to a new device. We validated our meta-latency predictor by measuring its latency estimation performance on unseen devices, on which it outperforms baselines, using only 10 to 20 samples per device. Furthermore, we combined our latency predictor with three rapid NAS methods, to show that it performs latency-constrained NAS on unseen devices extremely fast and accurately.

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**Organization** In this supplementary file, we provide in-depth descriptions of the materials that are not covered in the main paper, and report additional experimental results. The document is organized as follows:

- **Section A** - We elaborate on the detailed experiment setups, such as search space, reference devices, reference architectures, and latency measurement pipeline.
- **Section B** - We provide the implementation and training details, such as model structure, learning rate and hyper-parameters of learning the proposed hardware-adaptive latency prediction model.
- **Section C** - We provide the results of additional experiments and visualization of the obtained architectures on different devices.

## A Experimental Setups

### A.1 Search Space

**NAS-Bench-201** search space contains cell-based neural architectures which represent an architecture as a graph, where each cell consists of 4 nodes and 6 edges and each edge has 5 operation candidates, such as zerorize, skip connection, 1-by-1 convolution, 3-by-3 convolution, and 3-by-3 average pooling, which leads to the total of 15626 unique architectures. The macro skeleton is stacked with one stem cell, three stages of 5 repeated cells each, residual blocks [35] between the stages, and final classification layer consisting of a average pooling layer and a fully connected layer with softmax function. The stem cell consists of a 3-by-3 convolution with 16 output channels followed by a batch normalization layer [38], each cell with three stages has 16, 32 and 64 output channels, respectively. The intermediate residual blocks have convolution layers with the stride 2 for down-sampling.

| Candidates | Kernel size | Expansion ratio | Group |
|------------|-------------|-----------------|-------|
|            | 3           | 3               | 1     |
|            | 1           | 3               | 2     |
| k3_e3      | 3           | 3               | 1     |
| k3_e6      | 6           | 3               | 1     |
| k5_e1      | 1           | 5               | 1     |
| k5_e1_g2   | 1           | 5               | 2     |
| k5_e3      | 3           | 5               | 1     |
| k5_e6      | 6           | 5               | 1     |
| skip       | -           | -               | -     |

**FBNet** search space is a layer-wise space with a fixed macro-architecture, which is choosing a building block among 9 pre-defined candidates per 22 unique positions and the rest is fixed, resulting in $9^{22} \approx 10^{21}$ unique architectures. The block structure is inspired by MobileNetV2 [53] and ShiftNet [62], which adopts both mobile-block convolutions (MBConv) and group convolution. The configurations of 9 candidate blocks are provided in Table A.1.

**MobileNetV3** search space is also layer-wise space, where a building block adopts MBConvs, squeeze and excitation [37], and modified swish nonlinearity to build more efficient neural network. The search space consists of 5 stages, and in each stage, the number of building blocks ranges across {2, 3, 4}. For each block, the kernel size should be chosen from {3, 5, 7}, and the expansion ratio should be chosen from {3, 4, 6}. This leads the search process to a choice out of around $10^{19}$.

### A.2 Reference Device Details and Latency Measurement Pipeline
Table A.2: Specifications of reference devices used in the paper. We consider 17 hardware devices from 7 representative platforms such as Desktop GPU, Edge GPU, Server CPU, Mobile phone, Raspberry Pi, ASIC, and FPGA.

| Platform     | Name                        | Micro Architecture | The Number of Cores | Memory     |
|--------------|-----------------------------|--------------------|---------------------|------------|
| Desktop GPU  | NVIDIA GTX 1080ti [8]       | Pascal             | CUDA 3584           | 11GB GDDR5 |
|              | NVIDIA GTX Titan X [11]     | Pascal             | CUDA 3584           | 12GB GDDR5 |
|              | NVIDIA GTX Titan XP [12]    | Pascal             | CUDA 3584           | 12GB GDDR5 |
|              | NVIDIA RTX 2080ti [9]       | Turing             | CUDA 4352           | 11GB GDDR6 |
|              | NVIDIA Titan RTX [10]       | Turing             | CUDA 4068           | 24GB GDDR6 |
| Edge GPU     | NVIDIA Jetson AGX Xavier [6]| Volta              | CUDA 512            | 32GB LPDDR4|
| Sever CPU    | Intel Xeon Silver 4114 [4]  | Intel P6           | CPU Core 10         | Cache 13.75MB |
|              | Intel Xeon Silver 4108 [5]  | Intel P6           | CPU Core 10         | Cache 13.75MB |
|              | Intel Xeon Gold 6226 [3]    | Intel P6           | CPU Core 12         | Cache 19.25MB |
| Mobile Phone | Samsung Galaxy A50 [16]     | Samsung Exynos 9610| 4 Cortex-A73 & 4 Cortex-A53 | 4GB LPDDR4 |
|              | Samsung Galaxy S7 [17]      | Samsung Exynos 8890| 4 Exynos M1 & 4 Cortex-A53 | 4GB LPDDR4 |
|              | Essential PH-1 [13]         | Qualcomm Snapdragon835 | 8 Kryo 280 | 4GB LPDDR4 |
|              | Google Pixel2 XL [14]       | Qualcomm Snapdragon855 | 8 Kryo 280 | 4GB LPDDR4 |
|              | Google Pixel3 [15]          | Qualcomm Snapdragon845 | 8 Kryo 280 | 4GB LPDDR4 |
| Raspberry Pi | Raspberry Pi 4 [43]         | Broadcom BCM2711   | 4 ARM A72           | 4GB LPDDR4 |
| ASIC         | Eyeriss [43]                | Please refer to sections of Section A.2|
| FPGA         | FPGA [43]                   | Please refer to descriptions of Section A.2|

In this paper, we consider a wide variety of hardware devices of 7 representative platforms such as Desktop GPU, Edge GPU, Server CPU, Mobile Phone, Raspberry Pi, ASIC, and FPGA. Each device has different hardware structure and specification even in the same hardware platform, thus, we report hardware specification of all hardware devices except ASIC-Eyeriss and FPGA in Table A.2. In the case of ASIC, we use Eyeriss, which is a state-of-the-art accelerator [26] for deep CNNs. For FPGA, we use Xilinx ZC706 board with the Zynq XC7Z045 SoC which includes 1 GB DDR3 memory SODIMM [7]. For 4 devices such as Google Pixel3, Raspberry Pi 4, ASIC-Eyeriss, and FPGA, we use the latency data provided from HW-NAS-Bench [43], and for other devices, we directly measure the latency values to collect meta-training data on three search space such as NAS-Bench-201 space, FBNet space, and MobileNetV3 space.

In addition, we briefly describe how the latency data were collected in HW-NAS-Bench, please refer to original paper [43] for the details. In the case of ASIC-Eyeriss, the latency values are estimated from two simulator, Accelergy [65]+Timeloop [50] and DNN-Chip Predictor [71], each automatically identifying the optimal algorithm-to-hardware mapping methods for the architecture. For Raspi 4, all architectures are converted into Tensorflow Lite [20] (TFLite) format and executed with the official interpreter which is preconfigured in the Raspi 4. Similarly, all architectures are converted into TFLite format, and the official benchmark binary files are used for latency measurement on Pixel 3. For the last, to obtain the latency on FPGA, they implement a chunk-based pipeline structure [55, 70] and compile architectures using the Vivado HLS toolflow [1].

Now, we describe the latency measurement pipeline for desktop GPUs, Jetson, server CPUs, and mobile phone. Note that, throughout all hardware devices, latency data is collected averaging 50 times after 50 times initial runs to activate the device.

**Desktop GPU, Jetson and Server CPU:** To directly measure the latency of architectures from considered search space and baselines on these devices, the neural networks are implemented with PyTorch 1.8.1 [51] and executed with cuDNN [27] for desktop GPUs and Jetson, and with MKL-DNN for server CPUs.

**Mobile Phone:** (1) We load a neural architecture from architecture configuration with PyTorch [51] framework. (2) We serialize the neural architecture using TorchScript library [19]. (3) We build Android application with PyTorch Android library 1.9 [18] that measures the inference time of a serialized architecture on a target mobile phone and collects latency data by running the application.

**Measurement Details** We used latencies provided from the HW-NAS-Bench dataset itself for FGPA, ASIC, Raspi4, Pixel3. For other devices, we directly measured latencies, by discarding the first ten...
measurements and removing the top 10% and the bottom 10% values. Then we measured the latency of architecture on the target device 50 times and averaged the results.

To collect layer-wise latency data, following [23], we sample appropriate numbers of full architectures and run each full architecture while recording the time taken for each block type and input image size, not run each block piece respectively. A latency of each block and input image size pair is averaged over the number of sampled architectures which contains it, as well as 50 time runs.

### A.3 Correlation between Devices

Table A.3: Spearman’s rank correlation coefficient of collected latencies among 8 representative devices in NAS-Bench-201 search space. 1080ti_1 means 1080ti GPU with batch size 1.

| Device       | 1080ti_1 | 1080ti_256 | 2080ti_1 | 2080ti_256 | Silver4114 | Gold6226 | Pixel2 | Pixel3 |
|--------------|----------|------------|----------|------------|-------------|----------|--------|--------|
| 1080ti_1     | 1.00     | 0.74       | 0.96     | 0.78       | 0.83        | 0.96     | 0.80   | 0.59   |
| 1080ti_256   | 1.00     | 0.72       | 0.82     | 0.76       | 0.78        | 0.77     | 0.74   |        |
| 2080ti_1     | 0.99     | 0.76       | 0.81     | 0.94       | 0.79        | 0.79     | 0.57   |        |
| 2080ti_256   | 1.00     | 0.95       | 0.88     | 0.88       | 0.91        | 0.87     | 0.81   |        |
| Silver4114   | 1.00     | 0.98       | 0.91     | 0.87       | 0.97        | 0.86     | 0.71   |        |
| Gold6226     | 0.97     | 0.91       | 0.87     | 0.81       | 0.97        | 0.94     | 0.76   | 1.00   |
| Pixel2       | 0.94     | 0.94       | 0.86     | 0.71       | 0.94        | 1.00     |        |        |
| Pixel3       | 0.59     | 0.81       | 0.87     | 0.81       | 0.71        | 0.94     | 1.00   |        |

To show how much the latencies of the same architectures on different devices are correlated, we report the Spearman’s rank correlation coefficient among measured ground truth latencies of multiple hardware devices from each hardware platform on the same set of architectures in Table A.3. To reflect a measurement error, we collect two sets of latencies to compute the correlation coefficient of the device itself. As shown in Table A.3, the measured latencies on the same set of architectures are largely different (e.g., pixel2 vs pixel3, GPU 1080ti vs 2080ti with batch size 256). Furthermore, even with the same GPU device, the correlation scores are not high if the batch sizes are different. Therefore, the result shows that one cannot simply use a latency estimator from a device for a latency estimation of another device from the same platform and expect it to have high accuracy.

### A.4 Reference Architecture Details

To handle various devices with a single prediction model, we introduced reference neural architectures that enable hardware condition prediction, in Section 3.2 of the main paper. We considered a
device as a black-box function that takes such reference architectures as an input and outputs a latency set of reference architectures as a hardware embedding. We randomly selected 10 reference architectures for each search space (NAS-Bench-201, FBNet, and MobileNetV3) and used them across all experiments and devices of the same search space. In Figure A.1, we visualize 10 reference architectures that we used in NAS-Bench-201 search space. Reference architectures have diverse structures as shown in Figure A.1 and their latency values cover a wide range, for example, latency values of such reference architectures measured on NVIDIA Titan RTX (batch 256) are \{5.9, 8.5, 11.8, 14.1, 15.5, 16.6, 17.6, 19.1, 28.5, 44.3\}. Reference architecture indices in NAS-Bench-201 are 11982, 13479, 14451, 1462, 431, 55, 6196, 8636, 9, 9881. We include example reference architectures of all search spaces that we used in the experiments and their measured latency values on target devices, in the code and dataset that we submit.

B Implementation and Training Details

| Common Setting                              |       |
|---------------------------------------------|-------|
| Meta-batch size                             | 8     |
| The number of inner update                  | 2     |
| The number of episode                       | 2000  |
| Dimension of hardware input                 | 10    |
| Dimension of hidden layer of architecture encoder | 100   |
| Dimension of hidden layer of device encoder | 100   |
| Dimension of hidden layer of header         | 200   |

| NAS-Bench-201 search space                  |       |
|---------------------------------------------|-------|
| Meta-learning rate                          | 1e-4  |
| Dimension of architecture input             | 8     |
| The number of GCN                           | 4     |

| FBNet search space                          |       |
|---------------------------------------------|-------|
| Meta-learning rate                          | 1e-3  |
| Dimension of architecture input             | 132   |

| MobileNetV3 search space                    |       |
|---------------------------------------------|-------|
| Meta-learning rate                          | 1e-3  |
| Dimension of architecture input             | 145   |

Table B.1: Hyperparameter settings of HELP

In this section, we describe the details of HELP implementation and hyperparameters that we used in the experiments. HELP consists of four main modules such as an architecture encoder, a device encoder, and a header for output, and an inference network for \(z\). By combining the first three modules, we construct \(f\) and the last module is \(g\). While the architecture encoder has a different structure dependent on search space, all other modules have the same structure for all search spaces. Specifically, we use a 4-layers GCN to encode graph-based architectures of NAS-Bench-201 and use two multi-layer perceptrons (MLPs) to encode one-hot based flat topology of architectures of FBNet space and MobileNetV3 space. For the one-hot encoding, we follow OFA [24]. As the device encoder, we use two MLPs that take a latency set of reference architectures measured on a target device as an input and output a hardware embedding. By concatenating the architecture embedding and the hardware embedding, we feed it into the header that consists of three MLPs to output the estimated latency, in a scalar value. The inference network takes the reference latency set as an input and outputs scaling parameters with 603 dimensions which are equal to the number of weights and biases of the header. All dimension of hidden layers is 100 and we denote the hyperparameters for HELP as shown in Table B.1. We use Adam optimizer and mean square error as a loss function for all experiments.
C Additional Experiments

C.1 Experiment on NAS-Bench-201 Search Space

Table C.1: Performance comparison of different latency estimators combined with MetaD2A for latency-constrained NAS, on CIFAR-100 dataset with NAS-Bench-201 search space. We use Eyeriss (top) and FPGA (middle) as unseen platforms and Xeon CPU (bottom) as an unseen device. We exclude the layer-wise predictor for Eyeriss and FPGA since we use the latency measurements from HW-NAS-Bench [43] for this device, and it does not provide block information for the layer-wise predictor to use.

| Device          | Model                                      | Const (ms) | Latency (ms) | Accuracy (%) | Latency Model Sample Efficiency |
|-----------------|--------------------------------------------|------------|--------------|--------------|----------------------------------|
| Unseen Platform | MetaD2A + BRP-NAS [32]                     | 5          | 4.7±0.8      | 900          | 900                              |
| Unseen Platform | MetaD2A + HELP (Ours)                      |            | 4.1±0.6      | 69.8±19      | 10 ± 0.0                         |
| Unseen Platform | MetaD2A + BRP-NAS [32]                     | 7          | 9.1±0.0      | 900          | 900                              |
| Unseen Platform | MetaD2A + HELP (Ours)                      |            | 5.5±0.8      | 71.9±92      | 10 ± 0.0                         |
| Unseen Platform | MetaD2A + BRP-NAS [32]                     | 9          | 9.1±0.0      | 900          | 900                              |
| Unseen Platform | MetaD2A + HELP (Ours)                      |            | 9.1±0.0      | 73.5±85      | 10 ± 0.0                         |
| Unseen Platform | MetaD2A + BRP-NAS [32]                     | 11         | 11.0±9.0     | 70.0±92      | 10 ± 0.0                         |
| Unseen Platform | MetaD2A + HELP (Ours)                      |            | 11.0±9.0     | 70.0±92      | 10 ± 0.0                         |
| Unseen Platform | MetaD2A + Layer-wise Pred.                | 13         | 14.1±4.0     | 71.8±95      | 10 ± 0.0                         |
| Unseen Platform | MetaD2A + BRP-NAS [32]                     | 14         | 17.0±8.0     | 73.0±99      | 10 ± 0.0                         |
| Unseen Platform | MetaD2A + HELP (Ours)                      |            | 13.9±6.4     | 72.1±105     | 10 ± 0.0                         |

In Table 4 of the main paper, we show how the proposed HELP effectively reduces NAS costs of latency-constrained NAS tasks on two representative devices such as Google Pixel2 phone and NVIDIA Titan RTX GPU with NAS-Bench-201 search space. By attaching meta-trained HELP to the rapid NAS method, MetaD2A, the total NAS costs on Pixel2 and Titan RTX are only 125s and 111s, respectively. As in Table 4, we validate the efficiency of HELP on additional various devices such as Eyeriss and FPGA as unseen platforms and Xeon CPU Gold 6226 as an unseen device in Table C.1. We exclude the layer-wise predictor for Eyeriss and FPGA since we use the latency measurements from HW-NAS-Bench [43] for this device, and it does not provide block information for the layer-wise predictor to use. We report an average of the results of 3 runs using random seeds for each experiment, with 95% confidence intervals. Following the experiment settings in the paper of BRP-NAS [32], we train the baseline models using 900 architecture-latency sample pairs per device. To meta-train our HELP model, we consider 7 devices as reference devices such as NVIDIA Titan 1080ti, Intel Xeon Silver 4114, Intel Xeon Silver 4210r, and Samsung A50 phone, Samsung S7 phone, Google Pixel3 phone, Essential Ph 1 phone and use batch size 1, 32, 256 for Titan 1080ti and 1 for other devices and collect 900 samples per device. After meta-training HELP with collected data samples, we rapidly adapt HELP to target devices (Eyeriss, FPGA, and Gold 6226) with 10 reference architecture-latency pairs measured on each target device.

As shown in Table C.1, HELP adapted only with 10 samples obtains neural architectures where latency measured on the target devices are closer to latency constraints (Const) than the baselines in 6 out of 9 cases across various devices. For example, for latency constraints 5 (ms) and 6 (ms) of FPGA, MetaD2A + HELP provides neural architectures with 4.7 (ms) and 5.9 (ms) latencies, respectively, while latencies of architectures obtained by MetaD2A + BRP-NAS exceed far from latency constraints, as 7.2 (ms) and 7.5 (ms), respectively. The proposed method searches for architectures that satisfy a given constraint by responding sensitively even if the interval between
constraints is small. Similarly with the results of FPGA, for the unseen device, Intel Xeon CPU Gold 6226 with constraints 8 (ms), 11 (ms), 14 (ms), MetaD2A + HELP provides architectures that meet constraints such as 7.7 (ms), 11.0 (ms), and 13.9 (ms), respectively, and have high performance. The obtained architectures by the baselines either exceed constraints or have lower performance than ours. For various devices, HELP shows reliable prediction with only 10 measurements on a target device in the latency-constrained NAS tasks.

Table C.2: Mean of Spearman’s rank correlation coefficient when the meta-training devices and the meta-test devices of Table 3 in the main paper are swapped.

| Methods              | FLOPs | Layer-wise Predictor | BRP-NAS [32] | BRP-NAS (+extra samples) | HELP (Ours) |
|----------------------|-------|----------------------|---------------|--------------------------|-------------|
| Samples from Target Devices |       |                      |               |                          |             |
| Mean Corr. Coeff.   | 0.747 | 0.858                | 0.773         | 0.793                    | 0.940       |

In Table 3 in the main paper, we report the correlation between real-measured latency and latency estimated by HELP that meta-trained with 18 devices for 6 target devices. In this experiment, we swap meta-training devices and meta-test devices to show a flexibility of choice of meta-training and meta-test device pool. We meta-train HELP with 6 devices, GPU Titan RTX, CPU Intel Xeon Gold, Mobile phone Pixel 2, Raspberry Pi, ASIC Eyeriss, and FPGA, then meta-test on 17 devices that are originally used as meta-training device. Pixel 3 is excluded from the test device since HW-NAS-Bench [43] does not provide the latency values of architecture blocks to build a layer-wise predictor. We reports the average values of Spearman’s rank correlation coefficient on 17 devices in Table C.2. HELP consistently shows a high correlation coefficient value, even if we use much less number of meta-training device.

C.2 Searched Architecture Visualization on MobileNetV3 Space

Figure C.1: Visualization of architectures searched by OFA+HELP on MobileNetV3 space. 20.3ms latency on Titan RTX GPU (batch size = 64) (top). 147ms latency on Xeon Gold 6226 CPU (batch size = 1) (middle). 67.4ms latency on Jetson AGX Xavier (batch size = 16) (bottom).

C.3 Experiment on LatBench Dataset

LatBench Dataset is the latency dataset for various devices in the search space that is modified from the NAS-Bench-201 search space [31], provided by BRP-NAS [32]. Specifically, BRP-NAS simplifies
Table C.3: Performance comparison of FLOPs, BRP-NAS, and HELP on LatBench dataset, which has modified architecture space from NAS-Bench-201.

| Method     | Samples from Target Devices | desktop cpu | mobile dsp 855 | mobile gpu 450 | Mean  |
|------------|------------------------------|-------------|----------------|----------------|-------|
| FLOPs      | -                            | 0.706       | 0.803          | 0.955          | 0.821 |
| BRP-NAS    | 10                           | 0.701       | 0.308          | 0.775          | 0.594 |
| BRP-NAS    | 900                          | 0.991       | 0.959          | 0.961          | 0.970 |
| HELP (Ours)| 10                           | 0.990       | 0.958          | 0.956          | 0.968 |

the search space by removing "zero" and "skip-connect" operations from operation candidate set of NAS-Bench-201 to make consistency to NAS-Bench-101 [68]. Latencies are averaged over 1,000 latency samples while removing the lower and higher quartile values. Further, BRP-NAS removes 341 architectures that output zero in LatBench. On the other hand, when we construct our latency datasets, following HW-NAS-Bench [43], the full NAS-Bench-201 search is considered without any modification.

**Experimental Results** We validate the performance of our method on LatBench. The results in Table C.3 show that on the LatBench dataset, BRP-NAS indeed performs well, achieving high Spearman’s correlation scores of 0.970 averaged on 3 test devices, and largely outperforming FLOPs. Since BRP-NAS achieves a high correlation score, HELP does not beat its performance, but still achieves a similar correlation score (0.968), using only 10 latency measurements, while BRP-NAS trained with 10 samples, on the other hand completely fails. Although HELP does not significantly outperform baseline on LatBench, our goal is not improving the accuracy of a device-specific latency predictor, but is in eliminating the main computational bottleneck of hardware-aware NAS, by proposing a latency predictor that is extremely sample-efficient and generalizes well to any hardware devices without requiring any knowledge of the target hardware devices.