Towards Memristive Deep Learning Systems for Real-time Mobile Epileptic Seizure Prediction

Corey Lammie¹, Wei Xiang², and Mostafa Rahimi Azghadi¹

¹College of Science and Engineering, James Cook University, Queensland 4814, Australia
Email: {corey.lammie, mostafa.rahimiazghadi}@jcu.edu.au
²Department of Computer Science and Information Technology, La Trobe University, Victoria 3086, Australia
Email: w.xiang@latrobe.edu.au

Abstract—The unpredictability of seizures continues to distress many people with drug-resistant epilepsy. On account of recent technological advances, considerable efforts have been made using different hardware technologies to realize smart devices for the real-time detection and prediction of seizures. In this paper, we investigate the feasibility of using Memristive Deep Learning Systems (MDLSs) to perform real-time epileptic seizure prediction on the edge. Using the MemTorch simulation framework and the Children’s Hospital Boston (CHB)-Massachusetts Institute of Technology (MIT) dataset we determine the performance of various simulated MDLS configurations. An average sensitivity of 77.4% and a Area Under the Receiver Operating Characteristic Curve (AUROC) of 0.85 are reported for the optimal configuration that can process Electroencephalogram (EEG) spectrograms with 7,680 samples in 1.408ms while consuming 0.0133W and occupying an area of 0.1269mm² in a 65nm Complementary Metal–Oxide–Semiconductor (CMOS) process.

Index Terms—RRAM, Deep Learning, Seizure Prediction

I. INTRODUCTION

The backbone of smart healthcare is the Internet of Medical Things (IoMT), which is an amalgamation of medical devices and applications that connect through the internet to healthcare Information Technology (IT) [1] to overcome the shortcomings of traditional healthcare. The IoMT has the potential to give rise to many medical applications, including mobile epileptic seizure prediction, which is the primary focus of this paper.

IoMT edge devices can be used to perform computations locally, reducing latency and alleviating privacy concerns when sensitive medical data is processed. Moreover, they can be used to realize closed-loop systems, which are highly desirable for patient monitoring and treatments [2]. In Fig. 1 we depict three different application scenarios of our proposed seizure prediction system. To enable such a smart Deep Learning (DL)-based system to operate in real-time at the power-constrained edge, Resistive Random Access Memory (RRAM)-based in-memory DL computing architectures [3] could be used [2]. In this paper, we investigate the feasibility of using MDLSs to perform real-time epileptic seizure prediction at the edge to enable a mobile solution. Our specific contributions are as follows:

1) We are the first to investigate an in-memory DL approach to epileptic seizure prediction;
2) We explore a variety of weight-representation schemes while accounting for some device nonidealities, and compare the performance of our approach to other DL approaches;
3) We determine the power and area requirements for the optimal configuration, and investigate its feasibility for eventual hardware realization.

II. RELATED WORK

To the best of our knowledge, all existing hardware implementations tasked for epileptic seizure detection and prediction have been realized using Field Programmable Gate Array (FPGA), CMOS and Very-large-scale Integration (VLSI) technologies. Most existing hardware implementations detect epileptic seizures using traditional Machine Learning (ML) algorithms such as Linear Least Squares (LLS) [7], Support Vector Machines (SVMs) [8], and k-nearest neighbors (kNN) [9]. We refer the reader to [10] for a comprehensive survey of epileptic seizure detection and prediction systems. While
Artificial Neural Networks (ANNs) have previously been used for epileptic seizure detection [11] and prediction [12] on FPGA, no previous work has investigated the use of memristors for the detection or prediction of epileptic seizures using DL, which could drastically improve the performance on the IoMT edge.

III. PRELIMINARIES

A. Seizure Forecasting Systems

There is emerging evidence [13] that the temporal dynamics of brain activity of people with epilepsy can be classified into 4 states: interictal (between seizures, or baseline), preictal (prior to seizure), ictal (seizure), and post-ictal (after seizures). Seizure forecasting or predictive systems aim to classify the preictal brain state.

B. Memristive DL Systems

Memristive devices can be arranged within crossbar architectures to perform Vector Matrix Multiplications (VMMs) in-memory, in \(O(1)\) [14], which are used extensively in forward and backward propagations within Convolutional Neural Networks (CNNs) to compute the output of fully connected and unrolled convolutional layers. Scaled weight matrices can either be represented using two crossbars per layer, \(g_{pos}\) and \(g_{neg}\), to represent positive and negative weights, respectively, or using a singular crossbar per layer with current mirrors, so that the effective conductance of each device is offset by a fixed value, \(g_m\), that can be determined using (1) [15]

\[
g_m = -2/(R_{ON} + R_{OFF}),
\]

where crossbar column currents can be multiplied by a layerspecific scaling parameter, \(K\), to determine layer outputs. When a single device is to represent each parameter, constant currents to mirror can easily be realized using a diode-connected NMOSFET by adjusting the NMOSFET channel width so that it has a passive conductance \(g_m\). Given scalability issues, large crossbars can be split into smaller ones, referred to as either modular crossbar arrays, or crossbar tiles [16] to compute the output of linear and convolutional layers with a large number of weights.

IV. PROPOSED SYSTEM

A simplified block diagram of the proposed system is provided in Fig. 2. We confine the scope of this paper solely to the memristive DL system component depicted in Fig. 2(d), and only consider instances where learning is performed offline.

A. Network Architecture

The network architecture used is summarized in Table I, where \(n\) is the number of electrodes that are used to sample EEG signals, \(t\) is the window size in seconds, and \(p\) can be determined using (2)

\[
p = t f_s / k_s = 2t,
\]

where \(k_s\) denotes the number of overlapped samples, which for all cases in this paper is fixed to 128, i.e., half the sampling frequency, \(f_s\). Batch normalization and the ReLU activation function is applied to the output of all convolutional layers and the first fully connected layer. The output of the last fully connected layer is fed through a Softmax activation function. In contrast to other architectures used in related works [6], [17], [18], our architecture uses only linear, 2d-convolutional, max pooling, and batch normalization layers.

B. Training and Validation Datasets

For training and validation of our MDLS, we used the CHB-MIT [19] dataset, which consists of EEG recordings from 22 pediatric subjects with intractable seizures. For our preliminary study reported in this paper, 5 random patients were chosen. We leave evaluation using all subjects from the...
Consequently, seizures that occur in close proximity to each other. For seizure prediction, we are interested in predicting leading seizures. Consequently, seizures that occur $< T$ minutes after a previous seizure are not considered, where $T$ denotes the SOP. All time-series EEG signals are translated into time-frequency signals using STFTs with a window length of $t$ seconds (Fig. 2(e-f)). Similarly to [6], power line noise was removed by excluding components in the frequency ranges of 57–63 Hz and 117–123 Hz. The DC component (at 0 Hz) and components of frequencies above 114 Hz were also removed.

D. Training and Validation Methodologies

On account of the large class imbalance between preictal and interictal samples, we use an overlapped sampling technique, which was originally proposed in [6], to train the adopted network architecture. This is depicted in Fig. 2(t). Extra preictal samples are generated by sliding a $t$ second window along the time axis at every step, $S$, over preictal samples, which is chosen so that there are a similar number of samples per class (preictal or interictal). The Negative Log Likelihood Loss (NLL) function was used in conjunction with the DiffGrad optimization algorithm, which has been shown to outperform other optimizers [20], to train the networks with an initial learning rate of $1e^{-4}$ and batch size of 256 for 50 epochs, when performance stagnated. For a correct prediction, a seizure onset must be after the SPH and within the SOP, as depicted in Fig. 2. The metrics used to test the proposed approach are the accuracy, sensitivity, AUROC, and the FPR, as shown in Table I. For each subject, performance is reported using $k = 5$ stratified K-fold cross validation, where synthetic samples are discarded during evaluation. All implementations adopted the following parameters: $T = 30$ minutes, $t = 30$ seconds, and a SPH of 35 minutes.

V. PERFORMANCE EVALUATION

The MemTorch [15] simulation framework was used to simulate RRAM devices during inference using the VTEAM [21] model. Performance metrics for our trained convolutional and equivalent MDLS are reported in Table I. When predicting EEG seizures, it is common to have isolated false positives during interictal periods [6]. In recent works, discrete-time Kalman filters and least-$k$-prediction post-processing techniques have been adopted, however, they introduce a significant hardware overhead.

In Fig. 3, we report the sensitivity and FPR for all simulated configurations adopting a double column weight-representation scheme, as the performance of all configurations adopting a single column weight-representation scheme is insignificant. Consequently, we determine the optimal config-

---

**TABLE I: Network architecture employed.** For each convolutional and pooling layer, $f$ is the number of filters, $k$ determines the filter size, and $s$ denotes the stride length. For each fully connected layer $N$ denotes the number of output neurons.

| Layer                  | Output Shape          |
|------------------------|-----------------------|
| Convolutional, $f = 16$, $k = (5, 5), s = (2, 2)$ | $(16 \times [p-3]/2 \times 55)$ |
| Max Pooling, $k = (2, 2)$ | $(16 \times [p-3]/4 \times 27)$ |
| Convolutional, $f = 32$, $k = (3, 3), s = (1, 1)$ | $(32 \times [p-11]/4 \times 25)$ |
| Max Pooling, $k = (2, 2)$ | $(32 \times [p-11]/8 \times 12)$ |
| Convolutional, $f = 64$, $k = (3, 3), s = (1, 1)$ | $(64 \times [p-27]/8 \times 10)$ |
| Max Pooling, $k = (2, 2)$ | $(64 \times [p-27]/16 \times 5)$ |
| Fully Connected, $N = 256$ | $(256)$ |
| Fully Connected, $N = 2$ | $(2)$ |
TABLE II: Patient information and performance metrics across all folds for our trained conventional CNNs and their equivalent MDLSs adopting a double-column parameter-representation scheme.

| Patient | Seizures | Interictal Duration (h) | S | Accuracy (%) | Sensitivity (%) | AUROC | FPR (/h) |
|---------|----------|--------------------------|---|--------------|----------------|-------|---------|
| 1       | 7        | 17.0                     | 7.122 | 94.36±0.99  | 79.72±0.01 | 0.97±0.01 | 0.014±0.2 |
| 2       | 3        | 22.9                     | 1.684 | 94.36±1.40  | 93.41±0.01 | 0.97±0.01 | 0.016±0.4 |
| 5       | 5        | 13.0                     | 5.060 | 74.16±1.82  | 80.42±0.01 | 0.85±0.01 | 0.08±0.5  |
| 19      | 3        | 24.9                     | 1.687 | 96.33±0.66  | 54.72±0.00 | 0.50±0.00 | 0.20±0.00 |
| 23      | 5        | 3.0                      | 7.244 | 94.43±3.08  | 79.51±0.02 | 0.96±0.02 | 0.07±0.44 |

A. Comparison to Other DL Models

Since previous related works [6], [18] do not use a consistent testing methodology, we can only roughly compare our results to them using the sensitivity and FPR metrics from cross-validation. We report total sensitivities of 81.2% and 87.8%, and FPRs of 0.16/hr and 0.14/hr, respectively. In [18] clinical considerations were discarded and a zero SPH was used. Consequently, the reported performance is likely inflated. Nevertheless, as we did not perform any data post-processing, compared to both works, all of our networks have significantly larger FPRs. In Table II we report an average sensitivity of 77.74%, which is lower than that reported in [6] and [18]. Our result is still significant, because we use 2d-convolutional layers, max pooling, and fully-connected layers, and perform minimal data processing, while [6] used 3d-convolutional layers and [18] performed hyper-parameter optimization to obtain the lowest average validation loss over a 10 fold cross-validation.

B. Power, Area, and Delay Analysis

To determine the power and area requirements as well as the latency, which dictates the inference time of the optimal configuration, we map each layer of our deep network to a modular 128×128 crossbar tiles with no shared weights between layers using parameters for 65nm technology from [24]. The area and power of each ADC (8-bit) is, therefore, calculated to be 3×10^{-3}mm^2 and 2×10^{-4}W, and the area of each RRAM cell is estimated to be 1.69×10^{-7}mm^2. During inference, we assume constant operation at V = 0.3V per active cell, the largest voltage used to encode inputs, and an average cell resistance of (R_{OFF} + R_{ON})/2. All ADCs are assumed to operate at 5 MHz, and the number of tiles used for each network is assumed to be the exact number required to balance the latency among layers. RRAM read latency is considered negligible compared to ADC readout.

Table III shows the power, area, latency, and energy of our optimal configuration for configurations where samples are continuously fed to the network from a First-In First-Out (FIFO) buffer. We compare requirements for implementations for which each tile contains one ADC, and Time-Division Multiplexing (TDM) is used to read out column currents (denoted TDM), and for which each tile contains one ADC per column to read out column currents in parallel (denoted Parallelized). Given the large window length used, further duplication of crossbar tiles to improve throughput was deemed unnecessary.

VI. Conclusion

We investigated the potential of memristors to contribute to the design of a DL-based seizure prediction device. Our findings demonstrate that MDLS holds great promise for developing a compact epileptic seizure prediction architecture capable of low-power and real-time mobile operation. Our optimal configuration exhibits comparable performance to existing DL works in the literature while consuming significantly lower power.
less power than current Mobile Graphics Processor Units (mGPUs) and edge processors [2]. In future, the longevity and reliability of such a system should be properly investigated.

References

[1] D. V. Dimitrov, “Medical Internet of Things and Big Data in Healthcare,” Healthcare Informatics Research, vol. 22, pp. 156–163, Jul. 2016.

[2] M. Rahimiazghadi, C. Lammie, J. K. Eshraghian, M. Payvand, E. Do-nati, B. Linares-Barranco, and G. Indiveri, “Hardware Implementation of Deep Network Accelerators Towards Healthcare and Biomedical Applications,” IEEE Transactions on Biomedical Circuits and Systems, vol. 14, no. 6, pp. 1138 – 1159, Dec. 2020.

[3] M. Rahimi Aghachi, Y.-C. Chen, J. K. Eshraghian, J. Chen, C.-Y. Lin, A. Amirsoleimani, A. Mehonic, A. J. Kenyon, B. Fowler, J. C. Lee et al., “Complementary metal-oxide semiconductor and memristive hardware for neuromorphic computing,” Advanced Intelligent Systems, vol. 2, no. 5, p. 1900189, 2020.

[4] T. Tsai, J. Hong, L. Wang, and S. Lee, “Low-Power Analog Integrated Circuits for Wireless ECG Acquisition Systems,” IEEE Transactions on Information Technology in Biomedicine, vol. 16, no. 5, pp. 907-917, Sep. 2012.

[5] H. K. Lin, P. H. Lin, and C. W. Liu, “Design of a High-Throughput and Area-Efficient Ultra-Long FFT Processor,” in Proceedings of the International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, Taiwan, Aug. 2020.

[6] N. D. Truong, A. D. Nguyen, L. Kuhlmann, M. R. Bonyadi, J. Yang, S. Ippolito, and O. Kavehei, “Convolutional Neural Networks for Seizure Prediction using Intracranial and Scalp Electroencephalogram,” Neural Networks, vol. 105, pp. 104–111, Sep. 2018.

[7] T. Chen, C. Jeng, S. Chang, H. Chiueh, S. Liang, Y. Hsu, and T. Chien, “A Hardware Implementation of Real-time Epileptic Seizure Detector on FPGA,” in Proceedings of the IEEE Biomedical Circuits and Systems Conference (BioCAS), La Jolla, CA., Nov. 2011.

[8] H. Wang, W. Shi, and C. Choy, “Hardware Design of Real Time Epileptic Seizure Detection Based on STFT and SVM,” IEEE Access, vol. 6, pp. 67277–67290, Sep. 2018.

[9] A. Page, C. Sagedy, E. Smith, N. Attaran, T. Outes, and T. Mohsenin, “A Flexible Multichannel EEG Feature Extractor and Classifier for Seizure Detection,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 2, pp. 109–113, Dec. 2015.

[10] T. N. Alotaiby, S. A. Alshebeili, T. Alshawi, I. Ahmad, and F. E. Abd El-Samie, “EEG Seizure Detection and Prediction Algorithms: A Survey,” EURASIP Journal on Advances in Signal Processing, vol. 1, no. 183, Dec. 2014.

[11] M. U. Saleheen, H. Alenazadeh, A. M. Cheriyani, Z. Kalbarczyk, and R. K. Iyer, “An Efficient Embedded Hardware Approach for High Accuracy Detection of Epileptic Seizures,” in Proceedings of the International Conference on Biomedical Engineering and Informatics (BMEI), Yantai, China., Oct. 2010.

[12] H. Daoud, P. Williams, and M. Bayoumi, “IoT based Efficient Epileptic Seizure Prediction System Using Deep Learning,” in Proceedings of the IEEE World Forum on Internet of Things (WF-IoT), Aug. 2020.

[13] S. J. M. Smith, “EEG in the Diagnosis, Classification, and Management of Patients with Epilepsy,” Journal of Neurology, Neurosurgery & Psychiatry, vol. 1, no. 76, pp. ii2–ii7, Jun. 2005.

[14] M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, J. J. Yang, Q. Xia, and J. F. Strachan, “Memristor-Based Analog Computation and Neural Network Classification with a Dot Product Engine,” Advanced Materials, vol. 30, no. 9, p. 1705914, Jan. 2018.

[15] C. Lammie, W. Xiang, B. Linares-Barranco, and M. R. Aghachi, “MemTorch: An Open-source Simulation Framework for Memristive Deep Learning Systems,” ArXiv, vol. abs/2004.10971, Apr. 2020.

[16] D. J. Mountain, M. R. McLean, and C. D. Krieger, “Memristor Crossbar Tiles in a Flexible, General Purpose Neural Processor,” IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 8, no. 1, pp. 137–145, Oct. 2018.

[17] I. Kiral-Kornek, S. Roy, E. Nurse, B. Mashford, P. Karoly, T. Carroll, D. Payne, S. Saha, S. Baldassano, T. O’Brien, D. Grayden, M. Cook, D. Freestone, and S. Harrer, “Epileptic Seizure Prediction Using Big Data and Deep Learning: Toward a Mobile System,” EBioMedicine, vol. 27, pp. 103–111, Jan. 2018.

[18] H. Khan, L. Marcuse, M. Fields, K. Swann, and B. Yener, “Focal Onset Seizure Prediction Using Convolutional Networks,” IEEE Transactions on Biomedical Engineering, vol. 65, no. 9, pp. 2109–2118, Sep. 2018.

[19] A. H. Shoeb and J. V. Guttag, “Application of Machine Learning to Epileptic Seizure Detection,” in Proceedings of the International Conference on Machine Learning (ICML), Haifa, Israel., Jun. 2010.

[20] S. R. Dubey, S. Chakraborty, S. K. Roy, S. Mukherjee, S. K. Singh, and B. B. Chaudhuri, “diffGrad: An Optimization Method for Convolutional Neural Networks,” IEEE Transactions on Neural Networks and Learning Systems, vol. 31, no. 11, pp. 4500–4511, Nov. 2019.

[21] S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, “VTEAM: A General Model for Voltage-Controlled Memristors,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 8, pp. 786–790, Aug. 2015.

[22] E. Yalon, A. Gavrilov, S. Cohen, D. Mistele, B. Meyer, J. Salzman, and D. Ritter, “Resistive Switching in HfO2 Probed by a Metal–Insulator–Semiconductor Bipolar Transistor,” IEEE Electron Device Letters, vol. 33, no. 1, pp. 11–13, Nov. 2012.

[23] A. Mehmonic, D. Joksas, W. H. Ng, M. Buckwell, and A. J. Kenyon, “Simulation of Inference Accuracy Using Realistic RRAM Devices,” Frontiers in Neuroscience, vol. 13, no. 593, Jun. 2019.

[24] Q. Wang, X. Wang, S. H. Lee, F. Meng, and W. D. Lu, “A Deep Neural Network Accelerator Based on Tiled RRAM Architecture,” in Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA., Dec. 2019, pp. 14.4.1–14.4.4.