Low Power Self disabling Comparator for Asynchronous ADC

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Abstract— A low power single channel ADC with high sampling rate is designed in this work. The low power is accomplished by utilizing a self-disabling continuous time comparator those outcomes in less delay cells. The proposed ADC executed and simulated in 180nm CMOS technology. The possibility of 1.8 V supply in this technology provides improvement in step size and the improved delay cells yields increased sampling rate. The decision of asynchronous ADC is because of the way that it eliminates complicated correction methods to acquire better execution, as in flash, pipelined and SAR ADC. Asynchronous digital slope ADC, accomplishes power lower than the synchronous ADC. It does not need the complex alignment and can accomplish low power utilization. So to improve speed of sampling, improvisation of delay cell and shortening of delay time is done. In this paper an improvised design of the StrongARM comparator having faster performance, smaller area, and higher power efficiency is designed.

Index Terms— continuous-time comparator, strong-arm comparator, Asynchronous digital slope, delay cell, sampling rate

1. Introduction
The forthcoming ultra-wideband wireless communication requirements will broadly undertake decision and high speed analog-to-digital converters (ADC). In the flash ADC execution the input signal is applied to 2N-1 comparators, where N depicts the goals of the ADC. Each comparator is associated with a reference voltage which is produced by using a resistive ladder. High output for the comparator is obtained if the input voltage is found to be bigger than the reference voltage. On the other hand, an Asynchronous Digital Slope ADC achieves reasonable power efficiency with lesser complexity in alignment but fails to fulfill the required speed. A slope based ADC makes use of only one comparison per conversion and aids importance in application for two reasons. Great power efficiency is possible due to only one comparison is required per transformation and complexity of the design architecture is less. Since there is only one comparator included while a linear ramp can be executed precisely, thus demand for calibration is reduced alternatively; the comparator offset can be adjusted. Since this is a single point alignment which can be possible with an input reference of zero. Instead of the adjustments methods for flash or pipelined converters the alignment can be actualized effectively on chip.

The single-channel ADC has a sampling rate of 125MS/s thus making it inappropriate for
some application. Furthermore, it demands a lot of delay cells. Several modifications are made in this design based on the digital slope ADC. The sampling speed may substantially increase by making the delay time of single delay cell as 50ps. Comparator is used as an essential basic cells for various mixed-signal circuits. Nowadays, along with electronic science advancement some circuits are needed to make relationship between the analog and digital world in digital domain. Achieving this aim, therefore, the more comparators are needed. Demand for the low energy consumption, small area for the electronic chipsets.

The Strong ARM comparator topology is widely used as sense amplifier, comparator or latch having higher sensitivity. Strong ARM comparator because of its important features is unique as 1) Static power is not consumed 2) rail-to-rail output is produced 3) Offset referred from input is small 4) Input impedance is high. Low-power IC design has received booming interest in the past few years. Because high power accompanies a lot of problems such as wastage of energy, more heat dissipation, electromagnetic interference, security risks and lower stability. Power consumption is the main focus to all design. Considering any hand-held wireless devices, or computing solutions with higher performance. IC designs provide a sustainable influence on factors such as cost, time to market, functionality, reliability and power.

Comparators are basic building blocks with applications involving ADCs and focuses on performance of comparator especially the speed, utilization of power and delay in propagation. The demand in voltage comparators in recent years are low-power utilization as well as short delay in propagation. A lot of methodologies for low power are available. Traditionally, low power methods focus improvising at gate and physical level and at the RTL and system decreasing power level is obtained. Various advancements and strategies for low-power configuration are made and applied in the real time designs. Utilizing frequency scaling, dynamic voltage properties in devices of low-power mode of working is done. Different applications make use of unique procedures in order to utilize less power.

2. Existing Method
2.1. Strong ARM Comparator
The first Strong ARM comparator by Kobayashi et al in 1993 was introduced as shown in Figure 1. Ever since, modifications have been done to improve the circuit’s robustness of the circuit. Consequently, the speed, size and efficiency of the latch were compromised. Figure 2 shows a schematic of the conventional StrongARM latch proposed. The latch consists of 11 transistors CT1, CT2, CT3, and CT4 are charging transistors, T1, T2, T3 and T4 are cross coupled transistors, input transistors T5 and T6 are input transistors and tail current transistor T7.

The lock operation has three stages: Reset, Amplification, and Regeneration as shown in Figure 3. When CLK goes Low reset is implied, and therefore the internal capacitors at the nodes A, A’, B and B’ attains VDD through the charging capacitors. Amplification stage starts as the CLK goes high, turns off all CTs and the capacitors discharge through T7, T5 and T6. Which in turn is biased using constant common mode voltage (VCM). Therefore, these transistors are in ON condition. Differential voltage (Vdiff) is present between the gates of transistor T5 and T6 due to the reason that different current flows through these two transistors. Thus, the capacitors at node B and B’ discharge at different speeds resulting in the voltage at such nodes to drop at different rates when T3 and T4 transistors are
ON.

![Diagram](image1)

**Figure 1.** Original design introduced by [11]

When voltage values at nodes B and B' attain (VDD - \( V_{thn} \)), still at nodes A and A' voltage starts to drop at different rates. When at either A or A' voltage drops to (VDD - \( V_{thp} \)) either T1 or T2 are turned ON, whereas rest of the transistors remain in OFF condition owing to its cross-coupled design. Therefore, lastly voltages attain VDD in either node A or A' and zero volt at the left out node based on Vdiff polarity. The output taken from nodes A and A' are given to inverters, such nodes to drop at different rates when T3 and T4 transistors are ON.

![Diagram](image2)

**Figure 2.** Conventional design proposed by [12]
2.2 Continuous time Comparator

The schematic of conventional comparator as shown in Figure 4, symbolizes a symmetrical Op-Amp. The primary schematic consists of one differential pair and three current mirror circuits. The input of the differential pair is given with two equivalent current mirrors having current gain. B is said to be current ratio of M4 and M3. An inverter is connected to the output node.

This conventional comparator allows adaptability in common mode range at the input side. Transistors M3-M4 and M5-M6 reflect the current created by inputs and is given to the drain part of M8 and M9 respectively. Good CMRR and low offset are essential characteristics of this circuit.
3. Proposed method

3.1 Strong ARM Comparator

Performance of any circuit can be generally improved by increasing the current which is done by incrementing the transistor’s width. Expanding the width in turn increases the total capacitance of any given circuit. Thus, to improve the performance of any latch, the total capacitance in the circuit should be reduced without decreasing the current, or vice versa.

![Schematic of the proposed Strong ARM comparator](image)

**Figure 5.** Schematic of the proposed Strong ARM comparator

The proposed design, which consists of 13 transistors, is shown in Figure 5. The key advantage of this design is reducing the total internal capacitance in the circuit without compromising the current. This is achieved by placing the input transistors in the middle between the cross-coupled transistors. Since the input transistors are always ON, the need for the CT3 and CT4 is eliminated and nodes B and B’ are recharged through the transistors T5 and T6. Therefore, the performance and the energy efficiency of the latch are improved, while the area and the clock feedthrough issue are reduced.

3.2 Continuous time comparator

Power utilization is reduced when compared with the conventional comparator. The new proposed comparator as shown in Figure 6, can work with smaller average current than conventional one. The auxiliary branch (M13-M18) helps in identifying the flip point to create enhancement in current. Gates of PMOS Transistors (M13-M16) are cross connected. M18 obtains it’s from M17 and adds current to M7. When estimations of Vn and Vp are closer the voltages at node 2 and 3 are similar which results in large current flow through M13-M14. In saturation, NMOS current can be given as:

$$I_D = \frac{1}{2} \cdot gm \cdot (V GS - V T)$$

$$\Delta V = V_P - V_N$$

In case where $V_P$ is larger than $V_N$ and their difference is $\Delta V$, ID2 increases by $gm \cdot \Delta V/2$ and...
ID1 decreases by \( g_m \Delta V/2 \).

\[
I_{D4} = I_{D8} = I_{D9} = -B_{gm} \Delta V/2 \quad (3)
\]

\[
I_{D6} = B_{ID5} = B_{gm} \Delta V/2 \quad (4)
\]

Vn2 as a result increases \( \Delta V \) and substantially Vn3 reduces \( \Delta V \). The cross connection limits the current ID17. When \( \Delta V \) is found to be small, ID17 is large, and later ID18 copies ID17 and facilitates large current to ID7 thus implying that when the input voltages are different the consumption of current by the comparator is also different. When value ID7 is huge, the comparator functions at a high speed and only the tail current at the flip-point determines the comparator signal propagation. For getting the equivalent propagation delay, the proposed comparator has same tail current in comparison with the conventional comparator at the flip point. Moreover, it consumes smaller current than conventional comparator when \( \Delta V \) is enormous thus lesser power utilization.

Main circuit (M1-M10) of proposed comparator is same as conventional comparator. We only need to design the auxiliary branch to improve the performance of comparator. Assuming that tail current is \( I \) at the flip point, M18 needs add current IS to M7.

\[
I = i + I_s \quad (5)
\]

\[
I_s = k (i + I_s / 2) \quad (6)
\]

Where \( k \) is current ratio of M13 and M3

\[
I_s = (i/2-k) \quad (7)
\]

![Schematic of the proposed Continuous time comparator](image-url)
current of $M_{13}$ is $(i + I_s)/4$. We design it as two branches, so the current of $M_{17}$ is $(i + I_s)/2$. Also, we designed that the size of $M_{18}$ is double the size of the $M_{17}$. So we get $I_s$ that guarantee the tail current of proposed comparators is $I$ at the flip point.

4. Simulation Results

The Strong ARM Comparator and Continuous time Comparator is simulated with a power supply voltage of 1.5V. The proposed comparator executed and simulated in LT Spice. The waveform of strong arm comparator and continuous time comparator is as shown in Figure 7, Figure 8 and Figure 9.

![Figure 7. Output of strong arm comparator](image)

![Figure 8. Transient waveform of strong-arm comparator](image)
5. Conclusion
The decision of asynchronous ADC is because of the way that it eliminates complicated correction methods to acquire better execution, as in flash, pipelined and SAR ADC. Asynchronous digital slope ADC accomplishes lesser power than the synchronous ADC. Thus to improve the sampling speed, the delay cell is in turn improved, and the delay time is shortened extensively. The StrongARM Comparator and Continuous time Comparator is simulated with a power supply voltage of 1.5V. The proposed comparator executed and simulated in LT Spice.
6. References
[1] C Vudadha et al. 2012 Low-power self-reconfigurable multiplexer based decoder for adaptive resolution flash ADCs Proc. 25th Int. Conf. VLSI Design, pp. 280–85.
[2] P J A Harpe, C Zhou, K Philips and H de Groot 2011 A 0.8-mW 5-bit 250-MS/s time-interleaved asynchronous digital slope ADC IEEE J. Solid-State Circuits, pp. 2450–57.
[3] M Ding et al. 2012 A 5bit 1GS/s 2.7mW 0.05mm2 asynchronous digital slope ADC in 90nm CMOS for IR UWB radio Proc. IEEE Radio Frequency Integer, Circuits Symp., pp. 487–90.
[4] Y Shu, F Mei, Y Yu and J Wu 2018 A 5-bit 500-MS/s Asynchronous Digital Slope ADC with two Comparators IEEE Transactions on Circuits and Systems II: Express Briefs pp. 426-30.
[5] B Razavi, 2015 The strong ARM latch IEEE Solid State Circuits Mag. pp. 7–12.
[6] J Montanaro, R Witek, K Anne, and A Black 1996 A 160- MHz 32-b 0.5-W CMOS RISC microprocessor, IEEE J. SolidState Circuits, pp. 1703–14.
[7] H Wang, Y Du, X Jia and Y Fan 2015 A low-power continuous-time comparator with enhanced bias current at the flip point, IEEE 11th International Conference on ASIC(ASICON) Chengdu, pp. 1-4.
[8] Hattori and Toshihiro 2007 Challenges for Low-power Embedded SOC’s, VLSI design, Automation and Test, VLSI-DAT, International Symposium on IEEE, p.1.
[9] A Mathur and Q Wang 2009 Power Reduction Techniques and Flows at RTL and System Level, Proceedings of the 2009 22nd International conference on VLSI Design IEEE Computer Society, p.28.
[10] R Radzuan, 2012 The designs of low power AC-DC converter for power electronics system applications, Computer Applications and Industrial Electronics (ISCAIE), IEEE Symposium p.113.
[11] A Almansouri, A Alturki, A Alshehri, T Al-Attar and H Fariborzi, 2017 Improved StrongARM latch Comparator :Design,analysis and performance evaluation,3rd conference on ph.D. Research in Microelectronics and Electronics (PRIME),Giardini Naxos, pp.89-92.
[12] Y T Wang and B Razavi, 2000 An 8-Bit 150-MHz CMOS A/D Converter, IEEE Journal of Solid-State Circuits, pp.308-17.
[13] J Montanaro, R T Witek, K Anne, A J Black, E M Cooper, D W Dobberpuhl, et al., 1996 A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor, IEEE Journal of Solid-State Circuits, pp. 1703-14.