High mobility two-dimensional electron system on hydrogen-passivated silicon(111) surfaces

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We have fabricated and characterized a field-effect transistor in which an electric field is applied through an encapsulated vacuum cavity and induces a two-dimensional electron system on a hydrogen-passivated Si(111) surface. This vacuum cavity preserves the ambient sensitive surface and is created via room temperature contact bonding of two Si substrates. Hall measurements are made on the H-Si(111) surface prepared in aqueous ammonium fluoride solution. We obtain electron densities up to $6.5 \times 10^{11}$ cm$^{-2}$ and peak mobilities of $8000$ cm$^2$/V s at 4.2 K.

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Electron inversion or accumulation layers on a low disorder semiconductor surface can potentially be a new high quality two-dimensional electron system (2-DES) and could present a new technique in the development of atomic-scale electronic devices, where electrons are coupled to single atoms and molecules positioned on the surface. However, creating a 2-DES on a semiconductor surface is non-trivial due to the usual presence of dangling bonds and surface contamination. Such disorder creates surface states (within the semiconductor’s band gap) which may trap charge carriers. An ideal surface would be clean of contamination and have all its dangling bonds passivated.

Initial studies$^1, 2$ of Si(111) surfaces chemically treated with hydrofluoric acid (HF) established nearly ideal electronic properties: these surfaces exhibit both low surface-recombination velocity and low surface state densities ($\leq 10^{10}$ cm$^{-2}$)$^1$. Subsequent infrared absorption measurements$^3, 4$ showed that the dangling bonds on the Si surface are passivated by hydrogen. It was also discovered that buffering HF with ammonium fluoride ($\text{NH}_4\text{F}$) produces a more anisotropic Si etchant, where the (111) planes etch more slowly than other crystallographic planes. The Si(111) surface is thus unique in that such a simple wet chemical treatment can produce an ideal H-passivated Si surface which is atomically flat and defect free.$^5$. In addition, the H-Si(100) surface has been utilized recently as a resist for controlling the placement of individual atoms.$^6, 7$ Unfortunately H-passivated surfaces are sensitive to ambient conditions (oxidizes $\sim$ hours) and elevated temperatures ($T \geq 300^\circ\text{C}$). Hence, previous measurements$^1, 2, 8$ on H-Si surfaces have been constrained to controlled environments, and to date this surface has not been incorporated into practical devices. However, preservation of the H-passivated surface has been demonstrated by contact bonding two H-Si(111) substrates together at room temperature.$^9$. In this letter we describe the fabrication of a H-passivated Si field effect transistor (FET) which allows a 2-DES to be gated on a H-Si(111) surface through an encapsulated vacuum cavity, and we report the first electron transport measurements on H-Si(111) surfaces at 4.2 K.

Fabrication of the device begins with two individual Si substrates ($\sim 1$ cm$^2$), each having a distinct function. One is the H-passivated Si(111) substrate with source and drain contacts (Fig. 1a). It is at this surface where the 2-DES will be created. The other is a silicon-on-insulator (SOI) substrate which acts as the “remote gate” (Fig. 1b), where an electric field can be controlled within an etched cavity. These two substrates are contact-bonded in vacuum, and they adhere to one another due to local van der Waals forces between the two mating surfaces. Successful bonding requires these surfaces to be flat and clean of particle contamination before contact.$^8$. The bonding not only creates the FET, where the “remote gate” can induce electrons on the H-Si(111) surface, but also encapsulates the air sensitive surface in a vacuum cavity (Fig. 1a).

The H-passivated Si surface is fabricated on a 16 mm $\times$ 7 mm p-type Si(111) substrate (FZ, $\rho \sim 200$ $\Omega$ cm, $\leq 0.2^\circ$ miscut). First, a 5 $\mu$m deep Si mesa is dry-etched around the edges of the sample (Fig. 1a & Fig. 2a) along with alignment marks via reactive ion etching (RIE). This mesa prevents particles from accumulating on the surface while handling the substrate and ensures a clean edge for bonding. Next, a sacrificial SiO$_2$ layer ($\sim 300$ Å) is thermally grown on top of the Si(111) substrate for ion implantation. Photoresist is applied and patterned to expose four contact regions where 50 keV P ions (dose of $4.5 \times 10^{14}$ cm$^{-2}$) are implanted through the SiO$_2$. The implantation is activated by a 30 min 950$^\circ\text{C}$ anneal in dry N$_2$. Since the oxidation and etch rates of Si depend strongly on the doping level, these implantation and annealing parameters are optimized in such a way as to minimize surface topography differences around the edges of the implanted regions and at the same time maintain a contact resistance ($\rho \sim 100$ $\Omega/\square$ at $T = 4.2$ K) which is still metallic. As shown in Fig. 2b, each of the four n$^+$ contacts approaches a corner of a 1 mm wide square at the center of the Si(111) substrate in order to facilitate Van der Pauw measurements.

Fabrication of the “remote gate” starts with a 8 mm
$\times 12$ mm p-type SOI substrate (SOITEC UNIBOND), which consists of 3400 Å thick p-Si(100) (FZ, $\rho > 2000 \ \Omega \ cm$) on top of a 4000 Å thick insulating SiO$_2$ film. First, two conducting layers are created by B implantation in both silicon layers within the SOI: 250 keV at 4 $\times$ 10$^{14}$ cm$^{-2}$ and 100 keV at 2 $\times$ 10$^{14}$ cm$^{-2}$. As shown in Fig. 1(b), these degenerately p$^+$ doped Si layers form the gate and shield respectively. The purpose of the shield is to restrict the action (electric field) of the gate to a well defined region exposed by an etched cavity within the SOI (Fig. 1). The B dopants are annealed at 950$^\circ$C for 30 min in dry O$_2$, which adds a 250 Å SiO$_2$ layer on top of the SOI. This SiO$_2$ layer electrically isolates the shield from the n$^+$ contacts on the H-Si(111) substrate. The SOI substrate then goes through a series of three lithography steps using RIE. A mesa is defined around the edges of the substrate by etching away the top SiO$_2$ and Si layer of the SOI. Contacts to the shield layer are then exposed by etching $\sim$ 2700 Å of p-Si. Lastly, a 2 $\times$ 2 mm$^2$ cavity (depth $\sim$ 7600 Å) at the center of the SOI substrate is etched to the gate layer (Fig. 1b, & Fig. 2a).

Before bonding, both Si(111) and SOI substrates are cleaned of particles and organic contamination. The sacrificial SiO$_2$ film on top of the Si(111) substrate is removed in 10% HF and then the surface is H-passivated by immersion in a N$_2$ sparged (40%) NH$_4$F aqueous solution for 4 min.

Since the flatness of the H-Si(111) and SOI surfaces is critical for bonding and encapsulating the H-Si(111), both mating surfaces were investigated through (ex situ) atomic force microscopy (AFM). The inset of Fig. 2 shows an AFM image of a H-Si(111) surface prepared in N$_2$-sparged NH$_4$F solution, where the atomic step widths agree with the wafer miscut angle. The average rms roughness of the H-Si(111) surface is 1.5 Å and the SiO$_2$ surface (on the SOI) is $\leq$ 2 Å. Although the micro-roughness of these surfaces makes them suitable for bonding, fabricating an atomically flat H-Si(111) surface with electrical contacts (Fig. 2a) is non-trivial due to inherent surface height differences between the n$^+$ contact regions and the surrounding p-type Si(111). Our implantation and NH$_4$F etching parameters have minimized such height differences to $\leq 5$ Å.

Within $\sim$ 5 min of preparing the H-Si(111) surface, both substrates are placed in vacuum of a base pressure of $\leq 10^{-6}$ Torr. They are then contacted at room temperature, and visual confirmation of the bonding is made through an infrared camera (similar to Fig. 2c). The bond is then tempered in vacuum at 100$^\circ$C for $\sim$ 12 hours.

After tempering the bond, the encapsulated H-Si(111) FET is characterized by Hall mobility and density mea-
measurements at 4.2 K using standard Van der Pauw techniques. Contacts to the shield layer are grounded throughout the measurements. Hall data from a representative H-Si(111) FET, shown in Fig. 6, follows theoretical predictions \[10\] of a parallel-plate capacitor where the electron density on the H-Si(111) surface is linearly dependent on the gate voltage. From the linear fit shown in Fig. 3, the dielectric of the cavity is calculated to be within 5% of the expected value for a vacuum cavity with our dimensions. Due to the device architecture, the maximum electron density which can be induced on the H-Si(111) surface is limited by the dielectric breakdown voltage of the 4000 Å SiO$_2$ layer within the SOI. This breakdown voltage can be as high as 130 V, but the device in Fig. 3 has a peak density of \(\sim 6.5 \times 10^{11} \text{ cm}^{-2}\) at 100 V.

Because inversion layers in Si are thin \((\sim 100 \text{ Å})\), the electron mobility is sensitive to scattering associated with the surface \[11\] and thus provides a simple tool for analyzing the quality of our prepared H-Si(111) surfaces. The peak electron mobility on our H-Si(111) surface is \(\sim 8000 \text{ cm}^2/\text{V s}\) at 4.2 K (Fig. 8). Compared to previous peak electron mobility measurements in Si(111) metal oxide semiconductor (MOS) FETs \((\sim 2500 \text{ cm}^2/\text{V s})\) \[11, 12\], this is the highest electron mobility recorded on a Si(111) surface. In conjunction with the high mobility, the threshold of this device is 15 V, which indicates that the number of trapped electrons is \(\sim 10^{11} \text{ cm}^{-2}\) at 4.2 K. If we assume these are due to surface states arising from dangling bonds on the Si(111) surface, then it demonstrates that our chemically prepared surfaces (in a cleanroom environment) remain H-passivated during measurements. It is also interesting to note that the mobility is linear with density above \(3 \times 10^{11} \text{ cm}^{-2}\).

In summary, we have presented a new technique for gating air sensitive surfaces or materials through an encapsulated vacuum cavity. Utilizing vacuum as a gate dielectric, we have fabricated a 2-DES on a H-Si(111) surface which exhibits higher mobilities than previous Si(111) MOSFETs. Further electron transport measurements on such H-Si FETs can potentially make important contributions to 2-D physics. In addition, this experimental technique has potential toward the development of atomic-scale electronic devices, where electrons are coupled to specific molecules or single atoms positioned on the hydrogen-passivated Si surface.

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