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Photovoltaic field effect transistor (PVFET)-based Ge/Si photodetector for low-power silicon photonics

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ABSTRACT
We propose a Ge/Si photodetector based upon photovoltaic field effect transistor (PVFET) for low-power silicon photonics. The device realizes detection by modulating the conductivity of the FET channel through photo-induced gate voltage, exhibiting ultra-high responsivity. The responsivity can reach about $10^4$ A/W at operating voltages lower than 1.5 V. Furthermore, its light-to-dark (on/off) current ratio and temporal response characteristics are studied numerically. A maximum on/off ratio up to 193 can be obtained by optimizing the doping concentration of Ge gate.

I. INTRODUCTION
Silicon Photonics, owing to their particular advantages in power-consumption, performance, reliability and scalability, have become one of the most promising technologies for integrated photonics that target applications such as optical communications, high performance computing (HPC), optical sensors, on-chip optical interconnects, quantum technology and artificial intelligence (AI). Thanks to the advances in the growth of high-quality Ge film on Si or insulator, Ge/Si photodiodes (PDs) or avalanche PDs (APDs) with high quantum efficiency have been reported. However, none of them can concurrently meet the requirement of both high responsivity and low operating voltage.

Using a photodetector based on field-effect transistor (FET) structure may be able to mitigate this issue. In fact, several attempts have been made in the design and fabrication of photodetectors with different device configurations including MOSFETs, JFETs. As a subdivision of photo-MOSFET, the photovoltaic FET (PVFET) is one of the most promising solutions since it can realize photodetection with ultra-high responsivity at low voltage and may achieve monolithic integration with CMOS in the future.

Even though there have been several reports on PVFET-based photodetectors, some issues need to be further analyzed. First of all, the working mechanism of PVFET-based photodetectors still remains controversial—whether it is an effect caused by photo-induced carries injection, or it is due to photovoltaic field effect, remains unclear; Secondly, the temporal response of PVFET-based photodetector is not explained well by that of traditional MOSFETs. Furthermore, the light-to-dark current performance is not good enough and few work focused on this performance improvement.

In this paper, we aim to address the above issues theoretically through a PVFET-based Ge/Si photodetector. We unambiguously demonstrate that this device realizes detection by modulating the conductivity of the FET channel through photo-induced gate voltage. We find it exhibits ultra-high responsivity ($10^4$ A/W), but yet with very low operating voltage (~1.5 V), and large light-to-dark current ratio (maximum $I_{\text{light}}/I_{\text{dark}} = 193$). The mechanisms behind the improved device performances are analyzed numerically.

II. DEVICE AND METHOD DETAILS
The proposed structure of the PVFET-based Ge/Si photodetectors is similar to the FETs commonly used in microelectronics, except that the n-Ge is used instead of the poly-Si gate, as schematically show in Figure 1(a). The device is fabricated on the
boron-doped SOI substrate. High quality SiO$_2$ fabricated by thermal oxidation in dry O$_2$ is used as the gate dielectric layer. The crystalline Ge gate layer on insulator can be obtained through rapid melt growth (RMG) by LPCVD,$^{13,18}$ wafer bonding,$^{19}$ or epitaxial overgrowth.$^{20}$ The n-type source/drain and gate contact region are formed by conventional phosphorus implant doping, followed by rapid thermal anneal (RTA) process to activate the dopant and recrystallize the germanium as in the RMG technique. The light is evanescently coupled into the Ge absorption gate, which is a conventional form in silicon photonics and can reduce the thickness of the Ge absorption layer to 0.3 $\mu$m, as shown in Figure 1(b).

Two-dimensional numerical analysis of the PVFET-based photodetectors is conducted by using Sentaurus TCAD. The simulations lay emphasis on the principle of the PVFET by solving the Poisson equations coupled with the carrier continuity equations and transport equations, therefore, some parameters are simplified or approximated. For example, normal incident is used in the device simulation, so the light field in the absorption layer is assumed to be uniform rather than the attenuation distribution as in Figure 1(b); the defects in the Ge layer are simplified and characterized only by the carriers lifetime, which is about 1ns.$^{21}$ Detailed information of the simulations is listed in Table I.

### III. RESULTS AND DISCUSSION

#### A. Characterization of the PVFET-based Ge/Si photodetector

Figure 2 illustrates the drain current $I_{DS}$ as a function of the drain voltage $V_{DS}$ and the gate voltage $V_G$ either in darkness or under different incident power density of 1310 nm. The plotted characteristics are for a PVFET-based photodetector with W/L=25 ($L = 0.6 \mu$m) and n+ type (doping concentration 1e18 cm$^{-3}$) Ge gate. The $I_{DS}$ increases as the incident power increases, exhibiting an optical response characteristic. Larger optical response occurs at higher $V_{DS}$ and $V_G$. The dark current at $V_{DS} = 1.5$ V and $V_G = 1.2$ V is 179 $\mu$A, and the light current under 100 W/cm$^2$ incident light at this point is boosted to 242 $\mu$A. The $I_{DS}$-$V_{DS}$ photo-response characteristics and light-to-dark current ratio are consistent well with the published experimental results.$^{12,13}$

To clearly reveal the reason of PVFET’s photocurrent, the electron density distributions in the silicon channel under different gate bias $V_G$ and incident light densities are shown in Figure 3. Both the incident light and the gate voltage can lead to an increase in the electron density, and the distributions of electron densities under these two effects are quite similar, indicating that the incident light plays a similar role as the gate bias. Moreover, since there is a gate dielectric layer and no obvious current (as shown in Figure 10 in the Temporal response section) in the gate electrode, the variation of the electron density is not caused by photo-generated carriers injection but by photo-voltage in the Ge gate.

The Ge absorption gate acts like an open circuit solar cell,$^{13}$ whose photovoltage $V_{ph}$ satisfies the following formula

$$V_{ph} = \frac{n k T}{q} \ln \left( \frac{I_P}{I_d} + 1 \right) \propto \ln P,$$

where $I_P$ and $I_d$ are the photocurrent and dark current of the solar cell, $P$ is the incident light power. The photovoltage is linearly proportional to the logarithm of incident light intensity, which is consistent well with the extracted photovoltage from the PVFET-based

### TABLE I. Structure parameters of the device in simulation.

| Parameter             | Value       |
|-----------------------|-------------|
| Gate length           | 0.6 $\mu$m  |
| p-Si doping           | $5 \times 10^7$ cm$^{-3}$ |
| Ge thickness          | 0.3 $\mu$m  |
| Source/Drain doping   | $1 \times 10^2$ cm$^{-3}$ |
| Oxide gate thickness  | 0.015 $\mu$m |
| Ge doping             | $2 \times 10^1$ – $1 \times 10^2$ cm$^{-3}$ |
Having clarified that the device’s light detection is based on the photovoltaic effect rather than the photo-induced carriers injection, we now reveal the corresponding energy band diagram shown in Figure 5. The gate voltage induces an inverted n-type conductive channel under the oxide layer of p-Si. Upon optical (1310 nm) illumination, photo-induced carriers are generated exclusively within the Ge gate and holes are drifted toward the oxide/Ge interface under the applied gate voltage. The accumulated holes will attract electrons in the p-Si conductive channel, leading to the increase in the electron density. As a result, the conductivity of the Si channel is modulated by the incident light. This process is equivalent to generating an additional photovoltage on the oxide gate and causing the energy band of the conductive channel bent more sharply. The conductive channel, however, does not respond to the illumination itself, which is the main difference between photo-FETs and PVFETs.

B. Light-to-dark current ratio

Optimizing the doping of the Ge absorption gate can effectively improve the light-to-dark current ratio ($I_{\text{light}}/I_{\text{dark}}$), as shown in Figure 6. The doping of Ge absorption layer is uniform in the n+ gate device, this doping concentration is usually above 1e18 cm$^{-3}$ to form ohmic contact gate electrode. The light and dark current at $V_G = 1.5$ V are 606 µA and 415 µA, respectively. The $I_{\text{light}}/I_{\text{dark}}$ is only 1.46, and no high $I_{\text{light}}/I_{\text{dark}}$ zone exists below threshold ($V_G < V_T$). However, for the nn+ gate devices, the doping of the Ge absorption layer is divided into a high concentration n+-doping region close to the gate electrode and a low concentration n-doping region close to the channel. The n+ doping concentration of the two nn+ gate devices in Figure 6(b) is the same as 1e18 cm$^{-3}$, and the n doping is 5e17 cm$^{-3}$ and 2e17 cm$^{-3}$, respectively. The light-to-dark current ratio increases as the doping concentration of the Ge absorption gate decreases. For the n+ gate device with a doping concentration of 2e17 cm$^{-3}$, the light and dark current at $V_G = 1.5$ V are 527 µA and 213 µA, respectively. In addition, there is a high $I_{\text{light}}/I_{\text{dark}}$ zone in the subthreshold region, in which the largest $I_{\text{light}}/I_{\text{dark}}$ can reach 193.

The mechanism of the effect of doping concentration on light-to-dark current ratio can be illustrated by the energy band diagram from the Si-channel to the Ge-gate, as shown in Figure 7(a). Significant differences in conduction band under illumination and dark conditions appear only in the nn+ gate device. For the n+ gate device, the conduction band difference appears only after the gate voltage $V_G$ above 1.2 V. Obviously, the voltage actually applied on the dielectric gate under dark condition is equal to the gate voltage $V_G$ minus the voltage $V_{Ge}$ that is consumed on the space charge region of the Ge absorption layer. Since the space charge region of the nn+ gate device is wider than that of the n+ gate device ($W_1 > W_2$ as in Figure 7(a)), the nn+ gate device has a larger $V_{Ge}$ and a lower voltage applied on Si channel, thereby resulting in a smaller current $I_{DS}$ and a higher threshold voltage, as shown in Figure 6.
FIG. 6. $I_{DS} - V_G$ characteristics of the PVFET-based photodetectors with n+ and nn+ gate under 100 W/cm$^2$ illumination, (a) linear plot and (b) semilog plot.

In addition, the hole density in the Ge space charge region of the nn+ gate device is much higher than that of the n+ gate device since the energy band bent more sharply, due to the lower doping concentration and the wider space charge region in the nn+ gate, which results in a larger photo-voltage $V_{ph}$ for the nn+ gate device, as illustrated in Figure 7(b). These two factors mentioned above result in a better $I_{light}/I_{dark}$ performance of the nn+ gate device.

It would be suitable to use these PVFET-based photodetectors for low-power silicon photonics applications due to their high responsivity and CMOS-compatible operating voltage. Figure 8(a) is the responsivity characteristic of the nn+ gate PVFET versus incident light intensity at different $V_G$. Waveguide PDs’ responsivity, usually less than 1 A/W, does not change since the net photocurrent of PDs is proportional to the light intensity ($I_{ph} \propto P$). The PVFET-based photodetector’s responsivity decreases as the gate voltage $V_G$ decreases or the light intensity increases. The role of $V_G$ on the net photocurrent and responsivity is played by modulating the conductivity of Si channel. As for the influence of light intensity, the net photocurrent of the PVFET can be expressed as:

$$I_{ph} \propto \frac{\partial I_{DS}}{\partial V_G} \Delta V_G = g_m \cdot V_{ph} \propto \ln P \quad (V_G > V_T),$$

where $g_m$ is the transconductance, $V_T$ is the threshold gate voltage ($g_m$ is approximated as a constant independent of $V_G$ only at $V_G > V_T$). The linear proportion between the net photocurrent and the logarithm of light intensity is consistent well with Figure 8(b), and this logarithmic relationship results in the characteristic that PVFET’s responsivity, which is proportional to $I_{ph}/P$, decreases with increasing light intensity. Although the PVFET’s responsivity may be inferior to waveguide PDs under low gate bias or high intensity illumination, it has great advantage in weak light detection with a proper gate bias. The responsivity can reach about $1 \times 10^4$ A/W at $V_G = 1.5$ V, as shown in Figure 8(a). Of course, for the actual devices their performance may be affected by various factors, such as the defects in the Ge gate which would resulting in a drop of photocurrent through the reduction of carriers lifetime.

Based on the linear proportion between $I_{ph}$ and $g_m \cdot V_{ph}$, the photocurrent also can be increased by boosting the $g_m$, such as increasing the bias voltage, widening W/L, reducing the gate oxide
thickness, and using materials with higher mobility. However, the increment in photocurrent by these methods does not necessarily lead to an improvement in light-to-dark current ratio. The \( \frac{I_{\text{light}}}{I_{\text{dark}}} \) performance is related to the sub-threshold slope \( (1/S) \) and can be written as

\[
\frac{1}{S} = \frac{\partial \log I_{DS}}{\partial V_G} = \frac{q}{2.3kTn} \propto \frac{C'_{OX}}{C'_{ox} + C'_{b} + C'_{T}},
\]

where \( C'_{OX}, C'_{b} \) and \( C'_{T} \) are the oxide capacitance, bulk capacitance and interface traps capacitance per unit area, respectively. Therefore, decreasing the doping concentration of the p-Si bulk and reducing the interface traps, which respectively result in a lower \( C'_{b} \) and \( C'_{T} \), are two methods for improving the \( \frac{I_{\text{light}}}{I_{\text{dark}}} \). Compared with these conventional methods by increasing the sub-threshold slope of FET, optimizing the Ge gate doping concentration is the most effective way for light-to-dark current ratio performance.
C. Temporal response

Temporal response is an important characteristic of the PVFET-based Ge/Si photodetector and can be used to obtain the intrinsic speed. Figure 9 reveals the temporal response to a square wave light signal of 1310 nm. Higher drain voltage $V_{DS}$ can result in faster response time until reaching the saturation zone of $I_{DS}$, as shown in Figure 9(a). However, as the gate voltage $V_G$ increases, the rise time changes slightly, while the fall edges of the signal become slower (Figure 9(b)), indicating that the increase of gate voltage leads to a longer response time and lower bandwidth. It fails to explain this phenomenon by the frequency response $f \propto g_m/C_{TOT}$, where $C_{TOT}$ is the total capacitance. Because $g_m$ increases with the increment of gate voltage $V_G$, the response time should be faster in this case according to the frequency response criterion.

The slower fall edges under higher $V_G$ can be well explained by the time response of the electron and hole currents of the gate, as shown in Figure 9(c). The hole current in Figure 9(c) is negative, indicating that the holes and electrons flow in the same direction. Therefore, the overall current on the gate electrode is ignorable. Since the flow direction of holes is inconsistent with the electric field due to the presence of the gate dielectric layer, as shown in Figure 9(d), the fall edge of the hole current is slower than that of the electron current, and this inconsistency will be more severe under higher gate voltage $V_G$ to result in a slower response time.

In addition, the accumulation of holes under illumination can be realized detection by modulating the conductivity of the FET channel through photo-induced gate voltage. Besides, the light-to-dark current ratio performance can be improved by optimizing the doping concentration of Ge gate. Temporal response time is a drawback for these PVFET-based photodetector and trade-off has to be considered between the responsivity and bandwidth.

IV. CONCLUSION

In summary, we have proposed a Ge/Si PVFET photodetector with high responsivity and its operating voltage is compatible with CMOS. Different from traditional PDs and APDs, the device realizes detection by modulating the conductivity of the FET channel through photo-induced gate voltage. Besides, the light-to-dark current ratio performance can be improved by optimizing the doping concentration of Ge gate.

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