Modification of the Terman method for determination of interface states in metal–insulator–semiconductor structures

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Keywords: metal–insulator semiconductor structures, interface state densities, oxide charge, high-κ dielectrics

Abstract

In this work a modification of Terman method for determination of interfacial energy states located in the forbidden energy gap of the semiconductor (interface states) convenient for application in metal—high-κ—Si structures is proposed and explained in details. It has been found that usually observed presence of tails in the distribution of interface states towards the band edges is an artifact due to the method of determination of interface state densities. While excluding the contribution of quantum charge in semiconductor close to the interface with dielectric, these tails in the distribution disappear. Simple efficient method for determination of total density of interface states over the silicon bandgap is proposed.

1. Introduction

Interface states at the contact between the dielectric and semiconductor substrate substantially influence the characteristics of electron devices containing metal–insulator–semiconductor (MIS) structures. Many methods of determination of the distribution of interface states through the bandgap have been developed and are in use. Standard methods are described in several textbooks [1–3]. Downscaling of dielectric layers required for novel technologies, introduces several effects causing the standard methods to be not enough efficient. The issue of the use of these methods has been discussed in several works [4–10].

In our previous work [11], we proposed a compact method for correction of the measured $C–V$ and $G–V$ curves at various frequencies ($f$) for the effect of leakage currents and serial resistance. Thus corrected curves were subsequently used for extraction of interface state densities by three different methods: low–high frequency, admittance and Terman method. Determination methods were presented in a practical form enabling easy computation and comparison of the results obtained by different methods, without compromising the accuracy of the obtained results usually obtained by the considered methods.

In the present work we pay further attention to the Terman method, reconsidering its basics in the case where quantum charge in silicon near the interface with dielectric is taken into account. Influence of the quantum charge on $C–V$ characteristics has been exhaustively studied with numerical methods using basic principles in conjunction with the standard expressions describing characteristics of MIS structures [12–15]. Using such methods low frequency gate $C–V$ characteristics of MIS structures are simulated [13] and the density of interface states and flat–band voltages of MIS structures simultaneously effectively extracted [14]. In [15], modified Terman method is proposed using theoretical $C–V$ curve obtained by quantum mechanical numerical calculations. In the present work we intend to describe $C–V$ characteristics of MIS structures using analytical expression containing parameters that can be empirically extracted from the measured $C–V$ characteristics.

2. Theoretical basics

In [11] we have shown that under usual conditions for considered in this work layers optimal solution for measurement mode is the serial $C–V$ mode for given frequency ($f$), from which measured capacitance $C_{ms}$ and
measured resistance $R_{sm}$ in serial mode are obtained. Quantity required for further calculations, capacitance of the dielectric layer ($C$), is obtained using following expression:

$$C = C(V, \omega) = \frac{C_{sm}}{1 + \omega^2 C_{sm}^2 (R_{sm} - R_s)^2},$$  

(1)

where $\omega = 2\pi f$ is the cyclic frequency of the measurement signal. The value of the external serial resistance, $R_s$, is determined from extrapolation of measured serial resistance ($R_{sm}$) to infinite frequency ($f \to \infty$).

Capacitance of the insulating layer itself ($C_{ox}$) here is determined using the extrapolation method proposed by Kar [16, 17], using the value of the intercept ($\frac{1}{C_{sm}}$) of the fitting line for the part in strong accumulation obtained in a $\left(\frac{d}{dv} \frac{1}{C} + \frac{1}{C}\right)$ plot with the $\frac{1}{C}$ axes.

Equivalent oxide thickness ($d_{eq}$) of the dielectric is calculated using the expression

$$d_{eq} = \frac{\varepsilon_{so} S_s}{C_{ox}},$$  

(2)

where $S$ is the surface area of the capacitor and $\varepsilon_{so}$ is the dielectric permittivity of SiO$_2$.

Flatband voltage ($V_{fb}$) and oxide charge ($Q_{ox}$) were determined using standard methods described in details in [2, 3].

Electric field in the dielectric at the contact with the substrate is determined as [2]

$$E_{ox} = \frac{\varepsilon_{so}}{\varepsilon_{ox}} \left( \frac{2kT}{q} \frac{P_0}{\varepsilon_{so}} q \right)^{1/2} \left( \exp \left( \frac{-qV_s}{kT} \right) + \frac{qV_s}{kT} - 1 + \left( \frac{n_i}{P_0} \right)^2 \left( \exp \left( \frac{qV_s}{kT} \right) - 1 \right) \right)^{1/2},$$  

(3)

where $\varepsilon_{ox}$ is the effective dielectric permittivity of the dielectric, $V_s$ is the surface potential and $n_i$ is the intrinsic carrier density is silicon.

Oxide voltage $V_{ox}$ is

$$V_{ox} = E_{ox} d_{ox}.$$  

(4)

where $d_{ox}$ is the physical thickness of the dielectric.

The equivalent oxide thickness ($d_{eq}$) of the high-$\kappa$ dielectric, is calculated as

$$d_{eq} = \frac{\varepsilon_{so}}{\varepsilon_{ox}} d_{ox}.$$  

(5)

Oxide voltage (voltage of dielectric layer) is given by

$$V_{ox} = V_s - V_{fb} - V_s.$$  

(6)

Surface potential is determined using following implicit relation [11]:

$$V_s = V_b - V_{fb} - \varepsilon_{so} \left( \frac{2kT}{q} \frac{P_0}{\varepsilon_{so}} q \right)^{1/2} d_{eq} \left( \exp \left( \frac{-qV_s}{kT} \right) + \frac{qV_s}{kT} - 1 + \left( \frac{n_i}{P_0} \right)^2 \left( \exp \left( \frac{qV_s}{kT} \right) - 1 \right) \right)^{1/2}.$$  

(7)

Energy in the bandgap corresponding to given $V_s$ is calculated as

$$E = qV_s + kT \ln \left( \frac{P_0}{n_i} \right).$$  

(8)

Ideal capacitance of the MIS structure, $C_{ide}$, is calculated as explained in [2, 11].

Terman method is particularly efficient for practice since the distribution of the interface states is determined using a single high frequency $C$–$V$ curve [18]. Using enough high frequency fast interface states densities are determined, allowing slow states and border traps to be studied separately. The effect of transition and leakage currents that can substantially alter the measured characteristics is also avoided.

Standard Terman method uses following expression for determination of interface state densities

$$D_i = D_i(V_s) = \frac{C_{ox}}{q^2 S} \frac{d(V_b - V_{fb,I})}{dV_s} = \frac{C_{ox}}{q^2 S} \frac{d\Delta V_g}{dV_s},$$  

(9)

where $V_{g,I}$ is the gate voltage in the point on the ideal $C$–$V$ curve with the same capacitance as the capacitance of the structure at a given value $V_b$. 

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This page contains a detailed explanation of the methodology used in determining the capacitance, oxide thickness, and surface potential of a dielectric layer in a metal-insulator-semiconductor (MIS) structure. The formulae provided allow for the calculation of various parameters, including the equivalent oxide thickness ($d_{eq}$), oxide voltage ($V_{ox}$), and interface state densities ($D_i$). The Terman method is highlighted as a particularly efficient practice for determining these parameters, especially when considering the effects of interface states and leakage currents on the measured characteristics.
3. Application of the standard Terman method

Samples used in the first part of this study were Ag–Hf:Ta$_2$O$_5$/SiO$_2$/Si structures, obtained as it was described in details in [11], having square gates of active areas of 2.5 $\times$ 10$^{-3}$ cm$^2$. $C_{V}$ and $R_{C}$ characteristics (serial mode) were measured in the voltage range from $-1.0$ V to $+1.0$ V at the frequency of 100 kHz with the use of a HP 4284A LCR meter.

Below we describe step by step the procedure for determination of the interface state densities for a given sample (Ag–Hf:Ta$_2$O$_5$/SiO$_2$/Si), starting from $C–V$ characteristics and finishing with $D_n$ distribution over the forbidden energy gap of silicon.

First we show the plot of $\frac{d}{dV} \left[ \frac{1}{C_{V}} \right]$ versus $\frac{1}{C}$ (figure 1) from which the capacitance in accumulation ($C_{ox}$ = 3099 pF) is determined. Using expression (2) equivalent oxide thickness ($d_{eq}$ = 2.79 nm) is calculated.

Second, flatband voltage value $V_{fb}$ = $-0.022$ V is found. Further, oxide charge $Q_{ox}$ = 3.7 $\times$ 10$^{11}$ cm$^{-2}$ is calculated using the value of work function $\Phi_{ms}$ = $-0.35$ eV.

Third, using the results for $d_{eq}$ and $V_{fb}$, surface potential ($V_s$) is computed for all measurement points ($V_g$). Variation of the surface potential with applied gate voltage ($V_g$) is shown in figure 2. It is seen that at the borders of the measurement region (from $-1$ V to $+1$ V), $V_s$ reaches almost saturated values ($-0.27$ V in accumulation and $0.83$ V in inversion).

Fourth, the ideal $C–V$ curve is determined using standard method. Thus obtained ideal curve is shown in figure 3 as one with the measured $C–V$ curve.

Stretch-out of the measured compared to the ideal $C–V$ curve ($\Delta V_g = V_{g,eq} - V_{g}$), as illustrated in figure 3, is further determined for each measurement point ($V_{g,eq}$, $C(V_{g,eq})$) (full circles in figure 3), after numerically determining corresponding value of $V_g$ (ideal gate voltage) for the value of the ideal capacitance $C(V_g)$ equal to the measured value $C(V_{g,eq})$ at the given measurement point. Stretch-out ($\Delta V_g$) versus ideal gate voltage ($V_g$) is depicted in figure 4.

Next, the stretch-out ($\Delta V_g$) as a function of the surface potential ($V_s$) is determined. The result is shown in figure 5. Surface potential for a given value of $\Delta V_g$ (and hence of the capacitance $C(V_{g,eq})$) is computed numerically using expression (7) involving the value of the ideal gate voltage ($V_{g,eq}$) determined as it was explained in the previous paragraph.

Next step is numerical computation of the derivative function $d(\Delta V_g)/dV_s$, giving the derived curve (figure 6) of the curve shown in figure 5.

Interface state densities ($D_n$) are finally calculated replacing the derivative function $d(\Delta V_g)/dV_s$ in expression (9). Distribution of $D_n$ versus energy ($E$) inside the forbidden energy gap of Si, where $E$ is determined using expression (8), is shown in figure 7. Logarithmic scale is used in order to demonstrate the existence of exponential tails towards the band edges. It is to be noted that these tails extend roughly over energy regions about 0.1 eV large.
4. Modified Terman method

Due to the bending of zones in silicon near the interface with dielectric, a quantum well is obtained. Electrons in the case of gate positively biased (figure 8(a)) or holes in the case of gate negatively biased (figure 8(b)) captured on these levels contribute to an additional effective surface charge (quantum charge, $Q_q$); this charge is negative for gate positively biased and positive for gate negatively biased. In existing methods quantum charge is determined by numerical solving of quantum mechanical differential equations [19]. Here, we develop a method where quantum charge contribution is determined from the C–V curve itself.

In the case when there is a quantum charge confined within a well (figure 8) on the interface between the silicon and dielectric ($Q_q$), for the same surface potential $V_s$ as in (7), the value of the filed in oxide will be modified ($\mathcal{E}_{\text{ox},q}$)

$$
\mathcal{E}_{\text{ox},q} = \delta \mathcal{E}_{\text{ox}} + \mathcal{E}_{\text{ox},1}
$$

Figure 2. Variation of the surface potential ($V_s$) with applied gate voltage ($V_g$).

Figure 3. Ideal C–V curve (empty circles) as one with the measured (close circles).
in accordance with expression (Gauss law)

\[ 
\varepsilon_{ox} E_{ox,q} - \varepsilon_{Si} \left( \frac{2kT}{q} \right) \left[ \exp \left( -\frac{qV_g}{kT} \right) + \frac{qV_s}{kT} - 1 + \left( \frac{n_t}{p_0} \right)^2 \left( \exp \left( \frac{qV_s}{kT} \right) - \frac{qV_s}{kT} - 1 \right) \right]^{1/2} = Q_{q'} \quad (11a) 
\]

\[ 
\varepsilon_{ox} \sigma E_{ox} + \varepsilon_{ox} E_{ox} 
\]

\[ 
-\varepsilon_{Si} \left( \frac{2kT}{q} \right) \left[ \exp \left( -\frac{qV_s}{kT} \right) + \frac{qV_s}{kT} - 1 + \left( \frac{n_t}{p_0} \right)^2 \left( \exp \left( \frac{qV_s}{kT} \right) - \frac{qV_s}{kT} - 1 \right) \right]^{1/2} = Q_{q'} \quad (11b) 
\]

Taking into account that

\[ 
\varepsilon_{ox} E_{ox} = \varepsilon_{Si} \left( \frac{2kT}{q} \right) \left[ \exp \left( -\frac{qV_s}{kT} \right) + \frac{qV_s}{kT} - 1 + \left( \frac{n_t}{p_0} \right)^2 \left( \exp \left( \frac{qV_s}{kT} \right) - \frac{qV_s}{kT} - 1 \right) \right]^{1/2} = 0, \quad (12) 
\]
one obtains

\[ \varepsilon_{\text{ox}} \delta E_{\text{ox}} = Q_q. \tag{13} \]

As a result, the voltage drop on the oxide in presence of quantum charge is

\[ V_{\text{ox},q} = d_{\text{ox}} E_{\text{ox},q} = d_{\text{ox}} E_{\text{ox}} + d_{\text{ox}} \delta E_{\text{ox}} = V_{\text{ox}} + \frac{d_{\text{ox}}}{\varepsilon_{\text{ox}}} Q_q. \tag{14} \]

In the regions close to band edges it is expected that dominant contribution in the charge accumulation comes from the quantum charge. For these regions one can therefore write:

\[ \Delta V_g = V_{g,q} - V_g = V_{\text{ox},q} + V_{fb} + V_c - (V_{\text{ox}} + V_{fb} + V_c) \]

\[ = V_{\text{ox},q} - V_{\text{ox}} = \delta V_{\text{ox}} = \frac{d_{\text{ox}}}{\varepsilon_{\text{ox}}} Q_q, \tag{15} \]
where $V_{g,q}(V_s) = V_{ox,q}(V_s) + V_{fb} + V_s$ is the gate voltage for a given value of voltage in silicon ($V_s$) in presence of interfacial charge.

Otherwise written

$$\Delta V_g = \delta V_{ox} = \frac{d_{ox}}{\varepsilon_{ox}} Q_q,$$

meaning that close the band edges the stretch-out of the real $C-V$ curve from the theoretical is equal to the change of the oxide voltage due to the quantum charge at given voltage $V_s$ in Si and is proportional to this charge.

In figure 9 the plot of $\Delta V_g$ versus $V_{ox}$ (oxide voltage that would be obtained if there was no quantum charge) is shown. It is seen that for ultrathin dielectrics ($d_{eq} = 2.79$ nm, $d_{eq} < 4$ nm) single linear dependence is obtained. The slope of the line is close to unity and ($k_q \approx 1$) and the regression coefficient is 0.9998. For thicker films the behavior in inversion is the same, while in accumulation smaller slope is obtained; for the case of nanosized dielectrics ($d_{eq} = 8.00$ nm, $d_{eq} > 10$ nm), after a gradual change in a region about 1 V, a linear slope $k_q \approx 0.55$ is obtained. For thicker dielectrics ($d_{eq} = 13.54$ nm, $d_{eq} > 10$ nm) the slope in accumulation is $k_q \approx 0.06 \approx 0$. Based on this finding we can calculate the quantum charge using a simple expression:

$$Q_q = \frac{\varepsilon_{ox}}{d_{ox}} \Delta V_g = k_q \frac{\varepsilon_{ox}}{d_{ox}} V_{ox},$$

where $k_q$ is the slope determined from the plot shown in figure 9, separately for accumulation and inversion.
For films thicker than 10 nm slope in accumulation is \( k_q \approx 0 \), in accordance with the usual assumption that there is no quantum charge in such cases. This is due to the low value of electric field \( E_{ox} = V_{ox}/d_{ox} \) at the contact with substrate for \( d_{eq} > 10 \) nm. In this case shallow quantum well is obtained without bound states. For a given gate voltage, while decreasing dielectric thickness the well becomes more and more deep and several bound states appear. For \( d_{eq} < 4 \) nm the number of bound levels becomes enough high to rich the value \( k_q \approx 1 \).

In inversion for all the cases considered here value of the slope \( k_q \approx 1 \) is obtained. This can be explained by the fact that the value of the voltage in silicon in inversion is much higher than in accumulation. Hence, the quantum well is enough deep to provide several bound energy states even for substantially thicker than 10 nm. Above finding seems to be unusual, since no quantum charge has been reported in literature for films substantially thicker than 10 nm. However, our finding is not in contradiction with the reported experimental results. Namely, the effect of quantum charge in inversion on the measured capacitance is small and can be neglected when considering \( C-V \) curve only.

Further, for ultrathin dielectrics we use expression for quantum charge (17). When plotting \( \Delta V_g \) versus oxide voltage in presence of quantum charge, a curve with marked jump \( \Delta V_g(0+) - \Delta V_g(0-) = 0.41 \) V close to the flatband voltage condition \( (V_{ox,q} = 0) \) is obtained (figure 10).

In order to exclude the effect of quantum charge on stretch out, we calculate further the difference

\[
\delta \Delta V_g = \Delta V_g(V_{ox,q}) - \frac{d_{ox}}{\varepsilon_{ox}} Q_q \approx \Delta V_g(V_{ox,q}) - k_q V_{ox}.
\]

(18)

The plot \( \delta \Delta V_g \) versus surface potential is shown in figure 11. Two almost flat parts are obtained, close to the band edges. Distance between these two horizontal lines corresponds to the integral

\[
\int_{E_c}^{E_v} \frac{d\delta \Delta V_g}{dV_s} dV_s = 0.41 \text{ V}.
\]

(19)

In this work we propose to use modified method where contribution of the quantum charge is excluded from the stretch out using expression (11b). After replacing \( \Delta V_g \) with \( \delta \Delta V_g \) in (15), one obtains the following corrected expression for the interface state density

\[
D_{it}(V_s) = \frac{C_{ox}}{q^2 S} \frac{d\delta \Delta V_g}{dV_s}.
\]

(20)

and the total density of interface states is

\[
D_t = \frac{C_{ox}}{q^2 S} \int_{E_c}^{E_v} \frac{d\delta \Delta V_g}{dV_s} dV_s.
\]

(21)

The integral in expression (21) can be determined either by numerical integration of (20) or by determining the jump of \( \Delta V_g \) in flatband point. Both methods give practically same result.
Distribution of thus corrected densities of interface states over the silicon bandgap obtained for the structure containing ultrathin dielectric—Ag–Hf:Ta2O5/SiO2/Si is shown in figure 12. No tails are obtained near the band edges.

Thus obtained value of interface state density at midgap is $D_{itm} = 2.6 \times 10^{12} \text{eV}^{-1} \text{cm}^{-2}$ while the total density integrated over the entire bandgap is $D_i = 3.2 \times 10^{12} \text{cm}^{-2}$.

For comparison, in figure 13 the distribution of corrected densities of interface states over the silicon bandgap obtained as one with the distribution obtained without correction is displayed in. Tails towards the band edges large about 0.1 eV are present in the uncorrected curve. In the central part of the region the two curves closely overlap.

It is seen that the $D_i$ minimum in the case of standard method ($1.9 \times 10^{12} \text{eV}^{-1} \text{cm}^{-2}$) is obtained at $E = 0.573 \text{eV}$, approximately at the middle of the Si forbidden gap ($E = 0.57 \text{eV}$), usually denoted as $D_{itm}$.

Corrected Terman method for the same point gives slightly lower value ($1.7 \times 10^{12} \text{eV}^{-1} \text{cm}^{-2}$). Therefore, for determination of the most often used $D_{itm}$ value, both the standard and the modified method give similar results. Two clear maxima are observed in the case of the modified method while in the case of standard method sharp increases of $D_i$ towards band edges cover these maxima.
Further we show a comparison of the results obtained by the standard and modified Terman method for the case of metal–insulator–silicon structures containing various metal gates. Previously, we studied in details the effect of metal gate on the dielectric and electrical properties of metal–insulator–silicon structures, where dielectric was high-κ Ta2O5. Details on fabrication and characterization methods can be found in [20].

The studied structure is metal (Au, W, TiN, Al)–Ta2O5/SiO2–Si, where the thickness of the Ta2O5 layer is 46 nm and that of interfacial SiO2 layer is 2.7 nm.

Results for distributions of interface states over the forbidden gap of silicon, for various metal gates (Au, W, TiN, Al) as obtained by the standard Terman method are displayed in figure 14. In all four cases exponential tails towards the band edges are present. As it was observed in the case of extremely thin dielectrics, these tails also extend roughly over energy regions about 0.1 eV large. Furthermore, in the region of inversion, it is seen that the tails closely overlap each other. Above finding strongly supports the interpretation that the presence of this tail is
result of the determination method used rather than to intrinsic properties of the dielectric. In accumulation the tails are somehow shifted one from other, while the slopes obtained in lin-log plot are practically the same. The observed shift between the tails is of order of 50 meV and can be attributed to the errors of determinations of the parameters involved in calculations: oxide thickness and metal work function. Based on these findings we suggest that the tails obtained while using standard Terman method can be attributed to effect of quantum charge that is not taken into account in the standard method.

Further, in figure 15, we show the results for distributions of interface states over the forbidden gap of silicon, for various metal gates (Au, W, TiN, Al) as obtained by the modified Terman method. No exponential tails towards the band edges are observed. It is to be noted that the curves for TiN and W closely overlap each other, having two peaks, at 0.3 and 0.9 eV. Interface state densities for Al are systematically higher then these of TiN and W for about $1 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$; in addition, a sharp peak at 1 eV with value $3.2 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$ is observed. Such a behavior is expected since it is known that the Al gate is reactive with Ta$_2$O$_5$ [21], while TiN, W and Au are not. Value of equivalent oxide thickness ($d_{ox}$), flatband voltage ($V_{fb}$), oxide charge ($Q_{ox}$), interface state density at midgap ($D_{itm}$) and total interface states density over the forbidden gap of Si ($D_n$), as one with the work function differences ($\Phi_{ms}$) used in calculations, are shown in table 1.

6. Discussion on exponential tails and distribution patterns

Particularly important issue in determination of distribution of interface states through the bandgap of silicon is the presence of exponential tails towards the band edges (bottom of the conduction band, $E_c$, and top of the valence band, $E_v$), while using standard Terman method. Similar tails are obtained when using high-frequency quasistatic method [20, 22]. When comparing results from different methods, in [23] it has been found that such tails appearing in the case of high-frequency quasistatic method do not appear if more selective methods are used, such as: deep level transient spectroscopy, three-level charge pumping and spectroscopic charge pumping. These findings support the use of here proposed modified Terman method using single high-frequency $C$–$V$ curve for determination of distribution of interface states through the bandgap of silicon.

The issue of band tails was studied in [24] using electron spin resonance; it has been shown that exponential tails occur in tight region of about 2 meV close to the band edge. These regions are two orders of magnitude smaller that the regions of exponential tails observed in Terman method without modification, and hence we conclude that they have the same origin. Therefore, we conclude that it is not correct to attribute the exponential tails obtained by standard Terman method to an U-shaped continuum of states close to band edges, even in the cases where such tails can be observed by other, more selective methods.

Shapes of $D_n$ distributions are similar for all the structures considered in this paper. First the case of nonreactive Ag gate is shown. As is clearly seen in figure 12, for Au–Ta$_2$O$_5$/SiO$_2$–Si structures two broad peaks, at 0.29 eV and at 0.87 eV, with half-width of 0.35 eV and with almost equal maxima ($4.8 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$ and $3.2 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$) are present. These maxima closely correspond to the positions of two peaks in EPR spectra: at 0.32 and at 0.83 eV [25]. These peaks in EPR spectra are attributed to $P_b$ defects at the SiO$_2$–Si
interface. Thus, we found that the shapes of Dit distributions are not modified with the presence of high- 

$k$ layer itself, and for an SiO$_2$–Si interface with ultrathin SiO$_2$ (about 2 nm) layer remain similar to that of thick SiO$_2$ layers (about 200 nm). The shape for the case of nonreactive Ag gate (figure 15) is quite similar to above described case of Au gate.

In the case of TiN, W and Al gates, Dit distribution shapes are significantly modified (figure 15); peaks at about 0.8 eV have increased amplitude while the peaks at about 0.3 eV have reduced amplitudes, compared to the case of nonreactive Au gate. In the case of highly reactive Al gate, an additional sharp peak at around 1.0 eV is clearly observed.

Another issue related to the exponential tail in Dit distributions in accumulation observed in ultrathin dielectrics is that of the correctness of the Kar method for determination of the capacitance of the insulating layer itself (C$_{ox}$), used in this study. Crucial step in the foundation of the Kar method is the assumption that the differential capacitance in accumulation varies as exponential function of the surface potential ($V_s$). This assumption is equivalent to the assumption used in this study that the quantum charge varies as a linear function of the oxide voltage. Therefore the assumption used in the method of Kar is supported by the presence of quantum charge in accumulation at the contact of ultrathin dielectrics with semiconductor.

Above findings are most probably not limited to the structures containing SiO$_2$–Si interface. For illustration, determination of the Dit distribution for Pt–Al$_2$O$_3$/GeO$_2$–Ge structures (containing GeO$_2$–Ge interface) using the reported results in literature [26]. Distributions obtained by standard and by modified method are shown in figure 16.

7. Conclusions

Here proposed modified Terman method using single high-frequency C–V curve for determination of distribution of interface states through the bandgap of silicon provides an efficient tool for characterization of dielectric/semiconductor interfaces. The method is fully analytical and all the steps have clear physical meaning.
It has been clearly shown that exponential tails towards band edges observed in the results of standard Terman method result from the presence of quantum charge at the interface dielectric/silicon rather than from a U-shaped continuum of interface states. The use of the modified method allows to extract the contribution of the quantum charge and to determine interface states density from the charge located on interface traps only.

Acknowledgments

The author is exceptionally grateful to professor Elena Atanassova from the Institute of Solid State Physics, Bulgarian Academy of Sciences, for providing the samples of very high quality studied in this work.

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Figure 16. Distribution of densities of interface states ($D_{it}$) at GeO$_2$–Ge interface through germanium bandgap versus energy ($E$) obtained by standard (open circles) and by modified Terman method (modified method, close circles).
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