Silicon Photonic Architecture for Training Deep Neural Networks with Direct Feedback Alignment

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Abstract: There has been growing interest in using photonic processors for performing neural network inference operations; however, these networks are currently trained using standard digital electronics. Here, we propose on-chip training of neural networks enabled by a CMOS-compatible silicon photonic architecture to harness the potential for massively parallel, efficient, and fast data operations. Our scheme employs the direct feedback alignment training algorithm, which trains neural networks using error feedback rather than error backpropagation, and can operate at speeds of trillions of multiply-accumulate (MAC) operations per second while consuming less than one picojoule per MAC operation. The photonic architecture exploits parallelized matrix-vector multiplications using arrays of microring resonators for processing multi-channel analog signals along single waveguide buses to calculate the gradient vector for each neural network layer in situ. We also experimentally demonstrate training deep neural networks with the MNIST dataset using on-chip MAC operation results. Our novel approach for efficient, ultra-fast neural network training showcases photonics as a promising platform for executing AI applications.

1. Introduction

Propelled by recent advances in deep learning [1], the fields of artificial intelligence (AI) and neuromorphic computing (neuro-biological computer architectures) have seen a renaissance over the past decade [2]. Today, the software implementations of AI algorithms are executed on traditional computers based on the von Neumann architecture [3]. However, this architecture faces inherent data-transfer speed limitations due to the separation of memory and processor unit, known as the von Neumann bottleneck. Neuromorphic computing seeks to eliminate this constraint by exploiting the underlying elementary physics of hardware systems to create an isomorphism with AI algorithms [4]. As Moore’s law (which claims that the number of transistors on a microchip doubles every two years) approaches saturation and with the exponentially increasing needs of advanced machine learning algorithms [5,6], neuromorphic computing has attracted renewed interest as an alternative to the standard electronic digital computer architectures [7].

Silicon photonics has shown to be a promising platform for developing neuromorphic systems due to its compatibility with the mature silicon integrated circuit industry and the availability of high-quality silicon-on-insulator (SOI) wafers [8,9]. Monolithic silicon photonics
enables the integration of active photonic and electronic components onto a single photonic integrated circuit (PIC), including modulators, detectors, amplifiers, complementary metal-oxide-semiconductor (CMOS) control circuits, and optical multiplexers [10, 11]. Compared to their electronic counterparts for neuromorphic applications, photonic systems offer low-latency, high-bandwidth density and baud rates, low-cost communication, and inherent parallelism using optical multiplexing [12, 13].

One area of machine learning that would benefit from the low-power consumption and high-information processing bandwidth enabled by photonics is the training of large neural networks. Several photonic architectures have been proposed for executing in-memory computation of neural network inference [19–23]. However, for neural networks to perform useful tasks, the optimal network parameters (weights and biases) must first be determined using deep learning training algorithms. These algorithms have high-computation and memory costs that pose challenges to the current hardware platforms executing them [24], and the substantial energy consumption required to train large neural networks using standard von Neumann architectures presents a significant financial and environmental cost [25]. Currently, analog hardware-based neural networks are primarily trained offline (see Fig. 1(a)) using training algorithms implemented on digital platforms (optimized for executing sequential, procedure-based programs) which model the analog system and then map the optimized network parameters to the hardware platform for inference. However, the models may not capture all the manufacturing imperfections and variations of the physical neurons and their interconnections, including the inherent noise in the system. Additionally, the computational overhead required to accurately model the physical system can result in slow execution times compared to in situ training (see Fig. 1(b)).

The recently proposed direct feedback alignment (DFA) [26] supervised learning algorithm has gathered interest as a bio-plausible alternative to the popular backpropagation training algorithm [27]. The DFA algorithm, shown in Fig. 2 and further described in Supplement 1, is a supervised learning algorithm that propagates the error through fixed random feedback connections directly from the output layer to the hidden layers during the backward pass [26].
Unlike backpropagation, the DFA algorithm does not require network layers to be updated sequentially during the backward pass, enabling the algorithm to be a suitable candidate for efficient parallelization using photonics. The algorithm has been used to train neural networks using the MNIST, CIFAR-10, and CIFAR-100 datasets, and yields comparable performance to backpropagation [26]. As well, the DFA algorithm has been shown to obtain performances comparable to fine-tuned backpropagation in applications requiring state-of-the-art deep learning networks, including click-through rate prediction with recommender systems and neural view synthesis with neural radiance fields [28]. A recent theory suggests that training shallow networks with the DFA algorithm occurs in two steps: the first step is an alignment phase where the weights are modified to align the approximate gradient with the true gradient of the loss function, which is followed by a memorization phase where the model focuses on fitting the data [29].
the network’s inference step is encoded on multi-channel optical inputs. The electro-optic circuit then calculates the gradient vector for each hidden layer, which is used to update the network parameters stored in memory using an external digital control system. We also demonstrate training feed-forward neural networks on the MNIST dataset using experimental on-chip results to validate the photonic architecture.

2. Multiply-accumulate operations in photonics

The proposed architecture uses microring resonators (MRRs), which are closed-loop waveguides that use codirectional evanescent coupling between the ring and adjacent bus waveguides, as tunable filters to weight photonic signals through amplitude modulation [30]. Modulating the transmission of optical signals for specified wavelengths using silicon-based MRRs is achieved by changing their refractive index which tunes the resonance peaks. The refractive index can be changed by either varying the concentration of carriers through external biasing (e.g., carrier depletion in a PN-junction, carrier injection in a PIN junction) or by exploiting the thermo-optic effect [31]. In this paper, we experimentally demonstrate thermally tuned MRRs using in-ring N-doped photoconductive heaters; however, we also discuss the implementation of efficient, high-speed MRRs tuned using carrier depletion. In our proposed architecture, the MRRs that perform multiply-accumulate (MAC) operations are arranged in add-drop geometries coupled to two waveguide buses, known as the through and drop ports, as shown in Fig. 3(a). Tuning the MRR’s resonance to control the amount of light transmission through the two ports effectively weights the input optical signal.

The inner product operation, which consists of a series of MAC operations $\mathbf{x} \cdot \mathbf{w} = \sum x_i w_i$, is executed in photonics using an array of MRRs and a balanced photodetector (BPD) [19, 32].
Using wavelength-division multiplexing (WDM) techniques to process multi-channel analog signals along the same waveguide bus, where each optical signal with wavelength $\lambda_i$ is amplitude encoded with a value $x_i$, each MRR in the array is tuned with a specified weighting value $w_i \in [-1, 1]$ for the corresponding optical input wavelength $\lambda_i$. The through and drop port transmission spectrums, $T_p$ and $T_d$, of each MRR as a function of round-trip phase shift are Lorentzian-shaped and centered at the resonance phase with the incoming light. When the coupling losses between the MRR and bus waveguides are negligible, the relationship between the through and drop ports transmission for each MRR is $T_p = \frac{1}{T_d}$. These two ports are connected into a BPD which implements an electro-optic transfer function proportional to $|E_0|^2 (T_d - T_p)$, where $E_0$ is the amplitude of the input optical signal. Thus, the assigned weighting value $w_i$ of each MRR is given by $T_d - T_p$. Using this scheme, external biasing of the MRR tunes the resonance peak to correspond with the desired weighting for a selected optical wavelength, as shown in Fig. 3(b). Finally, the inner product between two vectors of size $N$ can be executed using an array of $N$ MRRs that are coupled to the same through and drop ports, as shown in Fig. 3(d).

Experimental multiplication operation results using a single MRR are shown in Fig. 3(c). The experimental data were collected by varying the encoded input signal and MRR weighting values across random combinations while measuring the optical power in the drop and through ports ($P_d$ and $P_t$) using a power meter. The output optical power for each combination was measured three separate times and the average value was recorded. The multiplication results from the two operands were determined by calculating $P_d - P_t$ off-chip, and the results were scaled to match the expected output range of values between $-1$ and $1$.

The continuous and multi-channel control of MRR arrays based on feedback control is an ongoing area of research, and a record-high accuracy of 9 bits for a single MRR using thermal tuning has recently been observed with negligible inter-channel crosstalk [33]. Due to precision limitations in PIC manufacturing leading to device-to-device variations, the relationship between the applied MRR bias and the change in weighting value for a specified optical wavelength must be determined experimentally [34, 35]. The current tuning approach relies on feedforward control to calibrate the MRRs, as well as feedback control for sensing the state of the system and correcting for any changes due to dynamic variability, such as ambient environmental fluctuations [36].

### 3. Photonic deep learning architecture

The proposed architecture for executing the DFA training algorithm exploits MAC operations performed in photonics (as discussed in the previous section) to execute matrix-vector multiplications in the analog domain during the backward pass, which are the most computationally expensive operation performed during training. For each training example during the backward pass, the architecture calculates the gradient vector $\delta^{(k)}$ for the hidden layer $k$ in a single operational cycle. The gradient vector (see Fig. 4(a)) is given by

$$\delta^{(k)} = B^{(k)} e \odot g'(a^{(k)})$$

where $B^{(k)}$ is a fixed random weight matrix with appropriate dimensions for the hidden layer $k$, $e$ is the error from the gradient of the loss function, $\odot$ is the Hadamard product (element-wise multiplication operator), and $g'$ is the derivative of the activation function with respect to $a^{(k)}$, which is the sum of the weighted input signals in the hidden layer $k$. The network’s weights and biases are then updated using the calculated gradient vector $\delta^{(k)}$ for each hidden layer $k$. The cost of updating the network’s parameters can be amortized using mini-batches during training.

A schematic of the proposed silicon photonic DFA architecture, which can be implemented on a PIC, is shown in Fig. 4(b). The DFA architecture requires a digital control system to tune the active electro-optic components on-chip, which include the MRRs that modulate the incoming
Fig. 4. Schematic of our proposed photonic DFA architecture. (a) Equation defining the gradient vector $\delta^{(k)}$ for the hidden layer $k$. (b) Silicon photonic architecture for calculating the gradient vector $\delta^{(k)}$ for the hidden layer $k$. The output layer gradient vector $e$ is amplitude encoded onto $N$ different wavelengths using an array of MRRs, and the matrix-vector product of the $M \times N$ matrix $B^{(k)}$ and vector $e$ is performed in the photonic weight bank. The Hadamard product between the vectors $B^{(k)}e$ and $g'(a^{(k)})$ is executed using TIAs in the electrical domain, yielding the desired vector $\delta^{(k)}$ which is converted to the digital domain using ADCs. At each time step, the control signals that encode the MRRs and TIAs are fetched from memory.

To calculate the gradient vector $\delta^{(k)}$ using the electro-optic circuit, WDM is used to combine $N$ laser signals with different wavelengths onto a single waveguide. The element values in the error vector $e$ are amplitude encoded onto the $N$ optical signals using an array of $N$ all-pass MRRs, where each MRR is tuned for a corresponding optical wavelength. The intensities of the input optical signals are identical to allow an encoding scheme that linearly maps the amplitude modulation value to the through port transmission. The modulated optical signals representing the error vector $e$ are then coupled into arrays of parallel MRRs, herein referred to as the photonic weight bank, which perform the required matrix-vector product with the matrix $B^{(k)}$ [21]. The photonic weight bank consists of $M$ rows of MRR arrays with $N$ MRRs per row, where the incoming signals are coupled evenly into each row using $1 \times M$ symmetrical optical splitters [37]. As discussed in the previous section for performing MAC operations in photonics, each MRR in the photonic weight bank is arranged in an add-drop configuration coupled to two separate

laser light with the error vector $e$ and the transimpedance amplifiers (TIAs) with tunable gain to convert photocurrent to voltage and scale it to implement the Hadamard product. To execute the DFA algorithm, a training example is first propagated through a neural network of variable size. This inference operation can be performed using an analog photonic circuit [19] or a separate digital processor. The error vector $e$ from the derivative of the loss function is then calculated using a dedicated CMOS processor that can be integrated on-chip. Finally, the electro-optic circuit calculates the DFA gradient vector $\delta^{(k)}$ for each hidden layer $k$, which is used to update the network parameters.
waveguide buses connected to a BPD. To perform the matrix-vector product, each column of MRRs in the photonic weight bank is tuned for the corresponding optical wavelength $\lambda_n$, and thus the element $B^{(k)}_{m,n}$ is mapped to the MRR in the $m$th row and $n$th column. Using the add-drop configuration, the incoming optical signals, which correspond to the error vector $e$, are weighted by modifying the optical transmissions, $T_p$ and $T_d$, for the through and drop ports of the MRRs. Summing the two transmission ports in the electrical domain allows the MRRs to be encoded with a weighting $w \in [-1, 1]$, assuming there is negligible loss in the system [38]. If the size of the photonic weight bank is larger than the dimensions of the matrix $B^{(k)}$, the redundant MRRs can be tuned with a weighting of zero. A negative value in the error vector can be encoded in the architecture by inverting the sign of the inscribed weighting values of the corresponding column of MRRs in the photonic weight bank.

Finally, the Hadamard product between the two vectors $B^{(k)}e$ and $g'(a^{(k)})$ is performed using a set of TIAs, where each BPD output is connected to a TIA. The vector $g'(a^{(k)})$ is calculated by the dedicated monolithic CMOS processor (the vector $a^{(k)}$ is known from the inference step) and encoded onto the voltage signals, supplied by the digital control system, that set the gain of the TIAs. The elements in the vector $g'(a^{(k)})$ are binary (0 or 1) when the ReLU function is used for the activation function $g(\cdot)$. Since the vector $a^{(k)}$ was previously calculated during the forward inference process, setting the gain does not impede the system’s maximum operating speed. The analog electrical signals are then converted to digital values with analog-to-digital converters (ADCs) and are used by the digital control system to update the neural network’s parameters.

The size of the photonic weight bank is physically bounded by the dimensions of the PIC and the maximum number of supported WDM channels in a single waveguide. The WDM channel limit is dependent on the finesse of the MRRs and the channel spacing, and an optimized design of the MRRs with a finesse of 368 could support up to 108 distinct channels [32]. However, the dimensions of the photonic weight bank do not restrict the size of the neural network being trained: a customized general matrix multiplication (GeMM) compiler can be used to subdivide the matrix $B^{(k)}$ such that the matrix-vector product is determined over multiple operational cycles by calculating a subset of the output vector at each cycle [39, 40]. Indeed, the compatibility of GeMM compilers with the photonic DFA circuit could enable on-chip training of large state-of-the-art neural network architectures by reducing the required mathematical operations at each cycle based on the topology of the PIC.

The co-integration of active on-chip silicon electronics with silicon photonics is crucial for the calibration and control of the photonic components in the proposed architecture [10]. Monolithic fabrication processes, which integrate electronics and photonics on the same substrate, are being investigated as the demand for silicon photonics technology grows [41]. An alternative near-term implementation of the photonic architecture could use flip-chip bonding by fabricating two dies (one optimized for silicon photonics and the other for CMOS electronics) and soldering them together. Another challenge facing silicon photonic computational architectures is their current reliance on off-chip light sources connected through fiber packaging. Several recent approaches have been proposed to integrate light sources directly onto silicon waveguide layers, including strain engineering of germanium and all-silicon emissive defects and rare-earth-element doping [42, 43]. An alternative approach, which is well suited for our highly-parallelized photonic architecture and has recently been experimentally demonstrated for performing photonic in-memory computing [44], is the use of an on-chip frequency comb source that generates evenly spaced emission wavelengths [45]. However, the optical source must be highly efficient while producing enough power for the entire system, which includes the requirement to overcome the capacitance and shot noise of the photodetectors.
Fig. 5. Experimental demonstration of neural network training on the MNIST dataset using two photonic circuits with different characteristic noise. (a) Two separate sets of 5000 photonic inner product measurements using $1 \times 4$ MRR arrays connected to both off-chip and on-chip BPD circuits. The error, defined as the measured minus expected values, from the off-chip BPD (on-chip BPD) has a standard deviation of 0.098 (0.202) and mean of 0.003 (0.003), yielding an effective resolution of 4.35 bits (3.31 bits). The accuracy of the on-chip BPD circuit measurements could be improved using a correctly configured BPD control circuit, as demonstrated using the off-chip BPD from Thorlabs. (b) Validation accuracy during training on the MNIST dataset using experimental inner product operation results, as well as without noise. (c) Test accuracy on the MNIST dataset as a function of the effective resolution used in the gradient calculations. The dashed red and green lines are the effective resolutions achieved by the off-chip BPD circuit (test accuracy of $97.41 \pm 0.15\%$) and on-chip BPD circuit ($96.33 \pm 0.16\%$), respectively.
4. DFA training experiment

We performed two sets of photonic inner product operation measurements using two similar circuits (with inherently different noise) to validate our proposed architecture. We then used these results to train feed-forward neural networks on the MNIST dataset in a Python simulation. Both circuits contain identical $1 \times 4$ MRR arrays with coupled through and drop ports; the ports in one circuit connect to an on-chip BPD (shown in Fig. 3(d)), while the ports in the other circuit connect to grating couplers for off-chip photodetection using a 5 GHz BPD from Thorlabs (part BDX1BA). The MRRs are thermally tuned using in-ring N-doped photoconductive heaters [36,46] and their add-drop configuration enables positive and negative weighting value encoding, as described in Sec. 2. We used four external cavity laser sources with different wavelengths (1546.558 nm, 1548.675 nm, 1549.595 nm, and 1551.480 nm) modulated directly by the laser source using embedded electronic modulation, and the different optical power levels were mapped to the expected range between 0 and 1. The integrated BPD, which consists of two germanium doped PIN photodiodes [21,47], is connected to a control circuit that only allows sensing and sourcing to occur at the same circuit location. This configuration results in an incorrect biasing voltage across the photodiodes which leads to larger noise in the output photocurrent compared to the off-chip BPD measurements. The signal fidelity of the on-chip BPD could be improved using a custom-designed circuit board that allows sensing and biasing from different locations within the circuit, similar to the design of the off-chip BPD.

We recorded two separate sets of 5000 photonic inner product measurements using the off-chip and on-chip BPD circuits by randomly varying the input vectors from the four laser sources (by modulating the signal amplitude) and the weight values of the MRRs (by tuning the resonance peaks using an applied current). The MRRs were initially calibrated to determine the mapping between the applied heating current and the corresponding optical weighting value. At each time step, the output photocurrent from the BPD was measured after all four channels were modulated with their corresponding inputs and weights. This experiment is representative of typical dense matrix multiplication operations as all elements in the weight and input vectors were updated simultaneously. It accurately accounts for the device-to-device variability of the system, optical and electronic noise, crosstalk between neighboring MRRs, and propagation loss throughout the system. The measured output photocurrents for both circuits, scaled between –1 and 1, as functions of the expected multiplication output are shown in Fig. 5(a). The error in the experimental inner product operations of the off-chip photodetection circuit has a standard deviation of 0.098 (4.35 bits) and mean of 0.003, while the integrated BPD circuit has a larger standard deviation of 0.202 (effective resolution of 3.31 bits) and mean of 0.003. Further details concerning our experimental procedures are given in Supplement 1.

We then used Python simulations to train neural networks with the photonic inner product operation results from our two sets of measurements. The simulations add accurately scaled Gaussian noise, which represents the error in our experimental inner product measurements, to the output of each MAC operation in the matrix-vector multiplication for calculating the gradient $\delta^{(k)}$. The inference and weight update steps were performed using full-precision data operations as these can be executed using digital circuitry in our proposed architecture. Using a neural network of size $784 \times 800 \times 800 \times 10$, the simulation added Gaussian noise to the output of the matrix-vector multiplications between the fixed random matrix $B^{(k)}$ ($800 \times 10$) and error vector $e$ ($10\times1$). Therefore, each matrix-vector multiplication performed 800 inner product operations between the error vector $e$ and each row in the matrix $B^{(k)}$. We trained this neural network on the MNIST dataset using ReLU activations in the two hidden layers and a softmax activation at the output. We used the cross-entropy loss function and the stochastic gradient descent optimization algorithm with a constant learning rate of 0.01, a momentum value of 0.9, and a mini-batch size of 64. Each simulation was run 10 times using different randomly initialized network parameters, and the mean results were recorded. The implementation of the
Python simulation is further described in Supplement 1.

The validation accuracy during training using the experimental results, as well as without injecting noise, is shown in Fig. 5(b). The simulations using the off-chip and on-chip BPD circuits achieved test accuracies of $97.41 \pm 0.15\%$ and $96.33 \pm 0.16\%$, respectively, while a test accuracy of $98.10 \pm 0.13\%$ was achieved without injecting noise. The test accuracy as a function of the effective resolution used in the matrix-vector multiplication operations is shown in Fig. 5(c). These simulation results demonstrate that the DFA algorithm is remarkably robust to noise and low-precision computations. Indeed, competitive performance using the DFA algorithm has even been shown using error values ternarized to $\{-1; 0; 1\}$ compared to full-precision training [48]. A similar technique of adding gradient noise when training very deep architectures with backpropagation has shown to avoid overfitting and lower the training loss by encouraging active exploration of the parameter space [49]. The remarkable robustness of neural networks to distortions against additive and multiplicative noise during inference and training [50] establishes analog photonic hardware as a promising platform for executing in situ training.

5. Energy and speed analysis

This section evaluates our proposed architecture’s expected energy consumption and speed using high-performance electronic and optical components (in contrast, our current experimental system has an estimated energy consumption of $\sim 2.0 \mu J$ per MAC operation as the thermally-tuned MRR weights have a slow tuning speed of $170 \mu s$ [30]). Matrix-vector multiplications are the fundamental operation performed during neural network training, and although they are computationally expensive to perform in digital electronics, they can be executed in a single operational cycle in photonics. The power efficiency and speed of the photonic architecture are dependent on the size of the photonic weight bank and the maximum operational rate $f_s$, which is limited by the electronic device on-chip with the lowest throughput [38]. Defining an operation as either a multiplication or addition of two inputs, the maximum number of operations per second (OPS) computed by the photonic architecture scales linearly with the size of the weight bank ($M \times N$):

$$\text{OPS} = 2f_s MN.$$

The lower bound on the required optical power per laser supplied to the photonic weight bank to overcome both the capacitance of the photodetectors with $N_b$ bits of fixed precision and the shot noise is given by

$$P_{\text{laser}} \geq M \frac{\hbar \omega}{\eta} \max \left( 2^{2N_b+1}, \frac{CV_d}{e} \right),$$

where $\hbar \omega$ is the photon energy, $\eta$ is the combined quantum efficiency of the laser, photodetector, and optical system loss through the waveguide, $C$ and $V_d$ are the capacitance and driving voltages of the photodetectors, and $e$ is the elementary charge [51].

During training, the tunable MRRs in the architecture are inscribed with a different value at each operational cycle. The values in the error vector $e$, which can be stored in static random-access memory (SRAM), are fetched and converted into analog voltage signals for tuning the designated MRRs using digital-to-analog converters (DACs). Unlike the dynamic $e$ vectors that change at each operational cycle, the inscribed weighting values of the MRRs in the photonic weight bank cycle through a set of known, unchanging values from the matrices $B^{(k)}$ for each hidden layer $k$. The control system for these MRRs can be made highly efficient by storing the set of weight values in an analog memory architecture, such as using resistive random-access memory (RRAM) or optical memories based on phase change materials [52, 53], where the energy consumption required to access and switch between weights is negligible compared to the energy cost of modulating the input optical signals with the error vector.
The power required to control the transmission state of a single MRR, $P_{\text{MRR}}$, includes two components: the power required to tune the MRR on and off-resonance to achieve the desired weighting value and the power required to lock the MRR weight onto resonance. The first component is negligible when using carrier depletion for high-speed tuning (~120 µW) [54, 55]. The second component is necessary due to fabrication nonidealities which cause a resonance shift; this shift can be greater than the tuning range allowed via carrier depletion, so embedded N-doped heaters are often used for thermal locking [13, 56]. However, heaters require ~14 mW, which can result in significant overall energy consumption [46, 54]. Alternatively, post-fabrication non-volatile phase trimming techniques can be used to correct for fabrication variations by modifying the refractive index of the waveguide or cladding, eliminating the need for thermal locking [57].

The estimated wall-plug power required by the DFA architecture with a photonic weight bank of size $M \times N$ is given by

$$P_{\text{total}} = N P_{\text{laser}} + N (M + 1) P_{\text{MRR}} + N P_{\text{DAC}} + M (P_{\text{TIA}} + P_{\text{ADC}}).$$  \hspace{1cm} (4)

The first term is the minimum necessary optical power, as shown in Eq. (3). The second term is the heating power required to tune the MRRs in the architecture as previously discussed. The third term accounts for the power required to convert the $e$ vector values into analog control signals using DACs ($P_{\text{DAC}}$), and we assume that the energy required to fetch the data from the SRAM is negligible compared to the other components in the architecture [58]. The final term corresponds to the power from the TIAs ($P_{\text{TIA}}$) and ADCs ($P_{\text{ADC}}$).

Using Eqs. (2) and (4), the expected optimal energy consumption per operation $E_{\text{op}}$, defined by $P_{\text{total}}/\text{OPS}$, as a function of the number of MAC cells in the photonic weight bank is shown in Fig. 6. The energy consumption using both embedded heaters for MRR locking (14.12 mW per MRR), as well as post-fabrication trimming of the MRRs (120 µW per MRR), is shown. To achieve an operational rate in the GHz range with low-power consumption, our calculations assume the use of efficient, high-speed MRRs with small footprints that are tuned using carrier depletion in an embedded reverse-biased PN-junction [59, 60]. The power and performance speed of the photonic architecture were calculated assuming the use of the ReLU activation function and
the following energy consumptions for the active electronic components: 180 mW per DAC (12 bit, 10 GS/s, Alphacore D12B10G), 13 mW per ADC (6 bit, 12 GS/s, Alphacore A6B12G), and 2.4 pJ/bit per TIA (20 GS/s) [61]. The throughput of the DAC limited the maximum operational rate $f_s$ to 10 GHz. We assumed an efficiency $\eta$ of 0.2 for the laser source, photodetector, and optical system loss through the waveguide. The calculations assume the use of an optical signal with a wavelength of 1550 nm and a high-performance photodetector with a capacitance of 2.4 fF and a driving voltage of 1 V [44]. Using a photonic weight bank of size $50 \times 20$, we can achieve speeds of 20 teraoperations per second (TOPS) and an energy consumption $E_{op}$ of 1.0 pJ per operation using MRRs with thermal heaters and 0.28 pJ per operation using post-fabrication trimming of the MRRs. The estimated compute density, defined by the OPS divided by the chip area, is 5.78 TOPS/mm². We assume a photonic MAC cell of size $47 \mu m \times 73.0 \mu m$, which accounts for the overhead waveguide and electronic routing, bonding pads for MRR control, and sufficient spacing between MRRs to eliminate crosstalk (see Fig. 3(a)).

6. Discussion

The recent proliferation of analog hardware-based neural networks has resulted in several proposed photonic architectures that have the potential to outperform state-of-the-art digital systems for inference computations [44, 62–64]. However, these photonic architectures are primarily trained offline using algorithms implemented on conventional digital platforms that attempt to simulate the analog hardware, resulting in longer training times due to the significant computational overhead. Additionally, the simulations may not accurately model all the nonidealities and noise sources in the photonic system, resulting in lower on-chip inference accuracy than expected by the simulated models. Motivated by these constraints, we have introduced a silicon photonic architecture that executes the fundamental operations of the DFA algorithm in the analog domain, including matrix-vector multiplication and the Hadamard product, to calculate the gradient vector for each neural network layer. Our proposed approach enables in situ training directly on a PIC, which can inherently account for nonidealities in the analog hardware while taking advantage of the high-bandwidth and low-energy consumption offered by photonics. Additionally, in situ training with photonic hardware can enable training with data signals originally generated in the optical domain, eliminating the need for optical-to-electronic conversions.

The photonic architecture is highly scalable for training neural networks of variable sizes due to its compatibility with GeMM compilers, which subdivide and process the on-chip matrix-vector operations based on the integrated photonic weight bank dimensions. Although analog photonic circuits inherently contain noise and cannot match the precision offered by digital electronics, neural networks exhibit remarkable robustness to distortions against additive and multiplicative noise during inference and training [50]. Indeed, as demonstrated by our simulation results, the DFA training algorithm performs well even with added noise during the calculation of the gradient vector (0.69% and 1.77% drop in accuracy on the MNIST dataset using inner product operation measurements from the off-chip and on-chip BPD circuits, respectively). The DFA algorithm is particularly well suited for implementations with analog hardware as the gradient vector is calculated by propagating the error through fixed random feedback connections directly from the output layer to each hidden layer, which is advantageous as noise does not accumulate between layers [26]. This is unlike the backpropagation algorithm, where the error is back-propagated layer by layer from the output layer to the hidden layers.

Integrated photonics is a promising platform for implementing machine learning algorithms as the high-throughput and low-latency offered by PICs could enable the implementation of ultra-fast and highly efficient analog neural networks. Our proposed architecture can perform the gradient vector computation in a single time step by incorporating WDM techniques to process multi-channel analog signals along the same waveguide bus. Using a weight bank of size $50 \times 20$ with high-performance photonic and electronic components, the architecture is expected to
perform up to 20 TOPS (limited by the signal modulation and detection speeds) while consuming less than 1 pJ per MAC operation and can be scaled up in terms of wavelength parallelization, number of vector multipliers, and signal baudrate. The expected improvements in training time and energy efficiency offered by our proposed architecture could enable the development of innovative neural network applications that cannot operate on current generation hardware. Future work includes demonstrating a complete integrated system with a dedicated CMOS processor capable of operating at high-speeds for neural network training without requiring any data processing off-chip.

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Disclosures

The authors declare no competing interests.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Supplemental document

See Supplement 1 for supporting content.

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