Memristor-based cryogenic programmable DC sources for scalable in-situ quantum-dot control

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Current quantum systems that are based on spin qubits are controlled by classical electronics located outside the cryostat at room temperature. This approach creates a major wiring bottleneck, which is one of the main roadblocks toward truly scalable quantum computers. Thus, we propose a scalable memristor-based programmable DC source that can be used to perform biasing of quantum dots inside the cryostat (i.e., in-situ). This novel cryogenic approach would enable us to control the applied voltage on the electrostatic gates by programming the resistance of the memristors, thus storing in the latter the appropriate conditions to form the quantum dots. In this study, we first demonstrate multilevel resistance programming of TiO2-based memristors at 4.2 K, which is an essential feature to achieve voltage tunability of the memristor-based DC source. We then report hardware-based simulations of the electrical performance of the proposed DC source. A cryogenic TiO2-based memristor model fitted on our experimental data at 4.2 K was used to show a 1 V voltage range and 100 µV in-situ memristor-based DC source. Finally, we simulate the biasing of double quantum dots, enabling sub-2 minutes in-situ charge stability diagrams. This demonstration is a first step towards more advanced cryogenic applications for resistive memories, such as cryogenic control electronics for quantum computers.

I. INTRODUCTION

Silicon quantum dots (QDs) are among the leading candidates for large scale integration of qubits given their compatibility with industrial semiconductor fabrication processes [1, 2], which may enable mass production and easier co-integration with control electronics. Moreover, semiconductor qubits benefit from a small qubit pitch, a long coherence time, and high gate fidelity [3–6]. However, quantum error correction and millions of physical qubits will be required to enable key industrial applications, such as encryption, quantum machine learning, or drug synthesis. The current approach to realize a quantum dot-based computer requires the qubit chips to be operated at 1 K or below [7, 8], while its control charge carriers for state manipulation and readout are placed outside of the dilution refrigerator (see Fig. 1a). In particular, the number of quantum-dot gates that are required to properly confine the charge carriers can range from one to up to six for specific quantum dot designs [9], and as many dedicated DC sources and cables per qubit. Although the control approach that is depicted in Fig. 1a has enabled important demonstrations over the past 20 years, it will become very cumbersome for few hundred qubits and may even be unachievable for the million of physical qubits that are required for fault tolerant quantum computing [10]. To avoid this wiring bottleneck, integrated cryogenic control platforms are being developed to control a larger number of spin qubits [9–14], while limiting the control electronics required at room temperature (See Fig. 1b).

To identify and reach the correct electronic regime, it is necessary to individually tune all of the quantum-dot gate biases (see Fig. 1a and b) using DC signals, typically in the ±1 V range with at least a 100 µV resolution, while maintaining a thermal budget in the order of a milliwatt or below per DC source [9, 11]. A first integrated solution based on switched-capacitor circuits and charge-locking, which is conceptually close to dynamic random access memories (DRAMs), has been proposed to perform simultaneous charge carrier confinement for several quantum dots[12, 15]. However, this approach requires qubits that have similar electrical behaviour, which has yet to be demonstrated for silicon spin qubits. To maintain the desired bias voltage applied to the quantum-dot gate, the switched-capacitor charge needs to be refreshed periodically. Meanwhile, TiO2-based memristors [16, 17] exhibit promising features, such as non-volatility, multilevel resistance state programming [18] and CMOS-compatible fabrication processes [19]. The memristor is used as the core component of the DC source. Its resistance value depends on its internal state. This resistance state has the particularity of being adjustable by external stimuli, such

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as DC sweeping or voltage pulses [20, 21], which enables the
voltage programmability of the DC source. Moreover,
the conduction mechanisms and temperature dependent
DC behavior of memristors based on transition metal ox-
ides have been studied at cryogenic temperatures down
to 1.5 K [22–28], hinting at hybrid CMOS-memristor con-
trol circuits for quantum systems. The co-integration of
a memristor-based biasing circuit and QDs will benefit
from the recently demonstrated operation of spin qubits
at 1 K [7, 8] relaxing the power dissipation restrictions.
This approach would make it possible to control the ap-
plied voltage on the gates by changing the resistance of
the memristors in a non-volatile manner, thus storing in
the latter the appropriate conditions for the QDs to be
formed. This on-chip co-integration would require a sin-
gle I/O to bias several quantum dots, thus paving the
way for scalable quantum computers on silicon.

In this paper, we propose a memristor-based DC source
set to operate at 4 K to first control the voltage bias ap-
plied to the gates of a silicon quantum dot cooled to
\(~10\) K. However, the perspective of spin qubits at
4.2 K in the near future would allow a co-integration
with the memristor-based DC source enabling scalabil-
ity as both technologies are CMOS-compatible [19, 29].
Using a feedback resistance tuning algorithm, we ex-
perimentally demonstrate the multilevel resistance pro-
grammability of CMOS-compatible Al2O3/TiO2−x mem-
ristor crosspoints [19] at 4.2 K. In addition, we conduct
extensive hardware-based simulations of a memristor-
based programmable gain amplifier (PGA) to optimize
the design of the memristor feedback resistor, and show
that this approach meets the voltage range and resolution

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**Fig. 1:** The memristor-based programmable DC source

**a.** Schematic view of a quantum dot based quantum
computer that is strictly limited to the QD biasing. The qubit chip is placed at the lower stage of a dilution
refrigerator at 10 mK. The DC signals that are required to control the qubits are generated by DC sources at room
temperature and routed by coaxial cables to base temperature. Attenuators and filters are fitted on the routing
cables to improve the noise to signal ratio. Each quantum dot requires up to six DC cables, each of which is often
connected to a dedicated tunable DC source at 300 K, which leads to a wiring bottleneck. **b.** Schematic view of a
quantum dot based quantum computer using the proposed memristor-based DC source at 4 K and supplied by a
single DC source delivering a fixed voltage \( V_\text{in} \), replacing all of the required DC sources at room temperature.
An additional RF line is required to tune the memristors. **c.** Zoom-in on a single DC line supplying the voltage bias
to a single QD gate. The green-framed variable resistor is the memristor circuit that is used as a tunable feedback
resistor in a programmable gain amplifier circuit (framed in grey). **d.** Circuit diagram of a memristor-based variable
resistor. Memristors are fabricated at the intersection of word lines and bit lines in a crossbar array. This
architecture is able to address a larger number of memristors. By individually tuning the resistance of each
memristor, we can vary the total resistance \( R_\text{tot} \) of the crossbar and thus the output voltage \( V_\text{out} \) of the DC source.
criteria for in-situ biasing of quantum dots.

II. CONCEPT

Figure 1a shows a typical experimental setup for solid-state spin qubits that operate at a temperature of 1K or below with optimal operation in the tens of millikelvins. DC biases are generated by rack-sized electronics at room temperature and transported by DC lines to the qubits in the dilution refrigerator. This approach imposes a limit on the number of biasing lines that can be integrated. We propose a programmable gain amplifier (PGA) as a biasing solution where the variable feedback resistor is based on a memristor circuit (See Fig. 1c, d). The resistance of each memristor can be finely tuned individually due to the analog behaviour of resistive memories. Write pulses are used to accurately program the resistance of the memristors. In the context of the PGA, these pulses can be applied using a low-dissipation cryogenic FPGA [30]. A single DC source that provides a fixed voltage at room temperature is required to supply multiple PGA circuits placed at the 4K-stage (See Fig. 1b, c) limiting the control electronic that is required at room temperature and thus limiting the number of cables going in the cryostat.

Based on the circuit parameters in Fig. 1c, we can fully determine the theoretical electrical characteristics of the memristor-based DC source. The output voltage of the PGA is determined by the amplification factor \( A_R = R_{tot}/R_L \), where the load resistor \( R_L \) is constant. With a common supply voltage \( V_{in} \) supplied to all of the horizontal lines of the memristor crossbar array, the total resistance of the crossbar is given by \( R_{tot} = \left( \sum_{i,j} G_{ij} \right)^{-1} \), where \( i,j \) represent the position of a memristor in the crossbar (see Fig. 1d). By programming \( N_s \) distinct resistance states for each memristor, the feedback resistor \( R_{tot} \) can take a maximum of \( N_s^{N_m} \) distinct resistance values, where \( N_m \) is the number of memristor in the crossbar circuit. Finally, we can define the theoretical voltage range \( \Delta V \) and the optimal voltage resolution \( \delta V \) of the memristor-based DC source:

\[
\Delta V = V_{max} - V_{min} = V_{in} \frac{R_{HRS} - R_{LRS}}{R_L N_m} \tag{1}
\]

\[
\delta V = \Delta V / N_s^{N_m} \tag{2}
\]

where \( R_{LRS} \) and \( R_{HRS} \) are the resistance of the memristor in the lowest resistance state and the highest resistance state, respectively.

III. THERMAL BUDGET AND POWER DISSIPATION

The power dissipated by the circuit in the dilution fridge is an important consideration when designing cryogenic control electronics for quantum systems. For the memristor-based DC source, the two sources of dissipation are the operational amplifier and the memristors in the feedback loop placed at 4.2K (see Fig. 1c). On the one hand, the most recent custom cryogenic operational amplifier from Ref. [31] dissipates 1\( \mu \)W, while commercial amplifiers characterized at 4.2K are expected to dissipate \( \approx 50 \mu \)W [32]. On the other hand, the power dissipated by the memristors is introduced by the Joule heating proportional to the current flowing \( V_{in}/R_L \) in the feedback loop. This dissipation is maximized when the memristor-based DC source delivers the maximum output voltage:

\[
P_{max}^\text{mem} = \left( \frac{V_{in}}{R_L} \right)^2 R_{tot}^{\max} \tag{3}
\]

where \( R_{tot}^{\max} = R_{HRS}/N_m \) the maximum feedback loop resistance. Our current memristors feature a 16k\( \Omega \)-HRS, leading to a power dissipation of 1.77\( m \)W for a supply voltage \( V_{in} = 1 \text{nW} \) required to achieve a 1V supply range. Hence, the total power dissipation of a single memristor-based DC source is in the order of a milliwatt. If we assume that this power is entirely dissipated on-chip, then an approximately 800 memristor-based DC source could be placed at the 4.2K stage assuming 1.5\( W \) cooling power. This number is currently bottlenecked by the low HRS reachable with our memristor devices. Increasing the HRS would allow us to reduce the input voltage \( V_{in} \), and thus the power dissipated, while keeping a 1V-range.

IV. EXPERIMENTAL RESULTS

Demonstrating reversible, non-volatile, and linear resistance programming of resistive memory devices at cryogenic temperatures would offer opportunities for hybrid memristor–CMOS cryogenic electronics. To accurately tune resistance states, we use a simple feedback algorithm from Ref. [18]. At each step, we apply a 200\( \text{ns} \) write pulse of negative amplitude to increase the resistance of the device or a positive amplitude to decrease its resistance, followed by a 1\( \mu \text{s} \)/200\( \mu \text{V} \) read pulse to evaluate the current resistance state of the memristor (see Fig. 2d). The write pulse amplitude is increased linearly by 20\( \text{mV} \)-step, starting from an initial positive amplitude \( V_{r}^{\text{min}} \) or negative amplitude \( V_{r}^{\text{min}} \) depending on the initial resistance state of the memristor. Once the desired resistance state is reached within a chosen tolerance, the resistance is read 20 times to ensure state stability (see insets of Fig. 2a, b).
Fig. 2: Multilevel resistance state programming of a TiO$_2$-based memristor. a. Programming 11 distinct resistance states within an accuracy of 1% at 4.2 K. Negative pulses are applied to the memristor electrodes to increase its resistance, while positive pulses decrease its resistance. These operations are, respectively, defined as RESET and SET. $V_{p}^{\min} = 0.4$ V and $V_{n}^{\min} = -0.6$ V were chosen as initial pulse amplitudes for the multilevel programming, along with an amplitude step of 0.02 V. The inset is a zoom-in of the 4.56 kΩ resistance state using the same axis of the main plot. b. Multilevel programming of 11 distinct resistance states within an accuracy of 1% at room temperature. The initial pulse amplitudes that were chosen are $V_{p}^{\min} = 0.7$ V and $V_{n}^{\min} = -0.9$ V, with an amplitude step of 0.02 V. The inset is a zoom-in of the 4.56 kΩ resistance state showing sub-1% reading variability. c. Simulation of a multilevel resistance state programming of a memristor placed at 4.2 K based on the Data-Driven model [33] fitted on our cryogenic experimental data. We used $V_{p}^{\min} = 0.5$ V, $V_{n}^{\min} = -0.7$ V and an amplitude step of 0.02 V. d. Typical pulse scheme used for the multilevel programming. The pulse width is fixed to 200 ns for write pulse (green or blue pulses) and to 10 μs for reading pulse (red pulses). The writing amplitude varies linearly based on the previous measured resistance, while the reading amplitude is set to 0.2 V.

Measurements were conducted on the same sample at 4.2 K and room temperature using a Keysight B1500A semiconductor analyzer with a 200 Msamples/s waveform generator module (WGFMU) coupled with a Lakeshore CRX-VF cryogenic probe station (see Fig. 2a and b). The TiO$_2$-based memristors were formed beforehand at 300 K. We demonstrate 11 distinct resistance states at 4.2 K and 300 K, with approximately 50 write pulses for each state with a programming accuracy of 1%. We observe that the resistance can decrease instead of increasing when applying negative write pulses during the multilevel programming. This phenomenon is more important at larger resistance values and can be defined as write variability. Cryogenic multilevel programming of the memristor (See Fig. 2b) shows a larger resistance decrease, which could be imputed to the larger temperature gradient in the vicinity of the conductive filament [34]. Moreover, at cryogenic temperatures, the competition between thermal- and field-activated effects is increased and could lead to additional variability during the thermally-activated RESET operation (increasing of the memristor resistance) [35, 36]. One can also note reading variability from the inset of Fig. 2a and b, which can be associated with thermal noise induced by the memristor conduction modes. We evaluate a sub-1% read variability on our devices, which allows for precise and stable resistance states (see Supplementary Fig. 3 for the characterization of the reading variability). A better programming accuracy can be reached using a smaller voltage step for pulse amplitude at the cost of programming time (i.e., more write pulses). Finally, we simulated the multilevel programming of our TiO$_2$-based memristors (See Fig. 2c) by fitting a Data-Driven model [33] replicating the pulsed response transient of a resistive memory (see Supplementary Fig. 3 for the characterization of the reading variability).
Fig. 3: Simulated performances of the memristor-based programmable DC source. a. Evolution of the voltage resolution of the memristor-based DC source with respect to the number of states and the number of memristors in the circuit. The horizontal dashed-black line highlights the 100 µV resolution target set to correctly reach an electronic regime in a quantum dot. A supply voltage $V_{\text{in}} = 1 \text{ mV}$, a resistance load $R_L = 1 \Omega$, a minimum resistance $R_{LRS} = 1.8 \kOmega$ and a maximum resistance $R_{HRS} = 16 \kOmega$, both inherited from the fitted cryogenic model, were used for these simulations. b. Maximum voltage range and optimal resolution for a given number of memristors. The number of distinct resistance states is set to five states for each memristor. As the number of memristors in the circuit increases, the voltage range shrinks while the voltage resolution improves leading to a resolution/range trade-off. c. Impact of the memristor variability on the DC source voltage resolution using a circuit of nine memristors with five states. The simulations were repeated 100 times for each variability value to allow for statistical analysis. The voltage resolution decreases logarithmically with the variability. The bottom inset shows the evolution of the standard deviation with respect to the memristor variability, which also follows a logarithmic dynamic.

V. SIMULATIONS AND DISCUSSIONS

Using the Data-Driven memristor model [33] parameters fitted on our experimental data at 4.2 K, we will next benchmark the performance of the memristor-based DC source by varying the number of memristors in the circuit and the number of distinct resistance states. We initially consider the circuit with no read or write variability to assess the optimal voltage resolution and range achievable.
Fig. 4: Simulation of the co-integration of a double quantum dot and the memristor-based DC source. Stability diagram acquisition time required with respect to the voltage resolution using two memristor-based cryogenic DC sources. The three color-framed insets show, respectively, the stability diagram obtained for a 10 µV, 100 µV and 1 mV voltage resolution. The co-integration simulations were conducted with a double quantum dot placed at 10 mK to take into account thermal noise and the DC source at 4 K using the cryogenic Data-Driven memristor model depicted in the inset. The parameters used for this set of simulations are summarized in Table I for the double quantum dot and Table II for the memristor in the Supplementary materials.

range decreases while the resolution increases exponentially. To comply with the 100 µV voltage resolution and 1 V-range requirements for quantum dot biasing, a circuit of at least eight memristors is needed if the number of states is fixed to five, which eases the multilevel programming operation. In the remainder of this paper, we consider a nine-memristor circuit to utilize the denser and more common 3×3 memristor-crossbar footprint.

To properly evaluate the memristor-based DC electrical specifications, we investigated the impact of memristor non-idealities [37] on the DC source output voltage. Figure 3c shows the voltage resolution of a nine-memristor five-state circuit with respect to the memristor variability. We chose the memristor variability as the combination of the read and write variabilities observed with our devices and implemented it as a percentage error of the resistance for each memristor. As this simulated memristor variability increases, the voltage resolution of the DC source remains almost constant. This suggests that the memristor’s variability has a negligible impact on the voltage resolution of the memristor-based DC source. We also note a decrease in the reproducibility of the constant step size between two consecutive output voltages (see inset of Fig. 3c). We can compare the averaged error induced by the memristor variability to the voltage noise of DC sources that are used in quantum dot setups, typically in the order of 1 to 5% of the target voltage (2.0% for the Tektronix 5014C).

The proposed DC source was programmed by reaching target resistance states for each memristor, leading to an associated output voltage. In the preceding simulations, we chose to consider the memristors as discrete multistate resistors. This allowed for efficient programming because a simple feedback resistance algorithm can be used, as in [18], to tune the whole crossbar array. Using this discrete programming approach, the output voltages depend on the resistance targets that we initially set, thus limiting our control of the output voltage. Instead, the memristor-based DC source can be controlled to reach an arbitrary target voltage to enable a more precise control of the PGA output voltage by exploiting the fully analog behaviour of the memristors. We propose
a servo algorithm, which will program the memristor crossbar to reach the target voltage accordingly. The crossbar resistance configuration is chosen in a pre-computed dataset, where the keys are target output voltages. We converge towards this optimal resistance configuration by performing a first coarse round of programming for each memristor to roughly reach the attributed resistance using the feedback algorithm for multilevel programming (see Fig. 2a, b and c). During a second round of programming, the resistance of the last memristor of the crossbar is finely tuned with a smaller voltage step and programming tolerance to a new target resistance that is specifically computed to balance the programming inaccuracy of the initial fast programming made on the other memristors. This fine tuning method allows for memristor variability robustness and a constant 100 µV step size within a 2.5% voltage error using a nine-memristor circuit. Controlling the memristor-based DC source to reach an arbitrary voltage offers a smaller voltage resolution when compared to the resistance-driven operation mode. However, the proposed memristor-based programmable DC source still satisfies the 100 µV for the same circuit parameters—that is, nine memristors and a supply voltage V_{in} = 1 mV—and is more suitable for in-situ use of the DC source.

Now that we have explained the working principle of our memristor-based DC source and demonstrated how it can be operated to reach a target voltage, we will next simulate its co-integration with a double quantum dot to validate its compatibility with quantum systems. Stability diagrams are used as a standard benchmark measurement to verify the basic performance of a quantum dot system. We simulated the electron transport through a double quantum dot (DQD) with respect to the voltages applied to its gates while biased by two memristor-based cryogenic DC source using equations from [38] (see Methods). Two important metrics to consider for a QD biasing solution are the voltage resolution and the stability diagram acquisition time, which is estimated by counting the number of write and read pulses needed to program the memristor circuit during the simulation of the charge stability diagram. This acquisition time increases with better voltage resolution, leading to a trade-off between speed and accuracy (see Fig. 4). The insets of Figure 4 show the derivative of a charge stability diagram to highlight the transition between the electronic regimes of the simulated DQD. We can identify the transition and occupations of the DQD for the three voltage resolutions—that is, 1 mV, 100 µV and 10 µV—, thus demonstrating the control of a simulated DQD by the proposed memristor-based DC source. Although the DC source can conveniently deliver voltage resolution from 10 mV to below 1 µV, a 100 µV resolution is sufficient to clearly observe the honeycomb pattern and its triple-point. It also allows for a fast 70 s-scanning of the DQD stability diagram. Moreover, when scaling up the DC-sources for a large number of double quantum dots, the stability diagram measurement can be performed in parallel. This allows us to scan all double quantum dots within 70 seconds using a 100 µV resolution.

VI. CONCLUSION

In conclusion, we propose a memristor-based cryogenic programmable DC source for scalable in-situ quantum-dot control. We demonstrate that this control approach fulfills the baseline requirements for quantum dot biasing (i.e., a 100 µV-resolution over a 1 V range) while keeping a limited number of memristors, allowing for a scalable biasing solution. We demonstrated the effective biasing of a simulated double quantum dot using a non-ideal TiO₂/Al₂O₃ memristor model, pointing out that memristor variability will not cause electronic regime changes that would be detrimental to quantum computation. We reported successful multilevel pulsed programming of TiO₂-based memristor at 4.2 K. This demonstration is a first step towards more advanced cryogenic applications for resistive memories, such as cryogenic control electronics for quantum computers using this proposed in-situ memristor-based DC source. Moreover, the scalability of this solution is limited by the total power dissipation of the DC source but still hints at a feasible integration of a few hundred of DC sources at 4.2 K, where the cooling power is on the order of a watt. More resistive memristors would allow us to decrease the power dissipation by limiting the current flowing in the feedback loop. Further works remain to be done regarding the thermal load introduced by memristors while they are being programmed to ensure cryo-compatibility. However, this additional heat load is limited to the bias tuning phase because memristors are non-volatile and the supply is maintained once programmed. Furthermore, the recent demonstrations of silicon spin qubits operated at temperatures above 1 K [7, 8] paves the way towards on-chip co-integration of ‘hot’ quantum dots and memristor-based control electronics. This approach would allow us to overcome the wiring bottleneck that the community will face when scaling-up quantum computers.

Data availability

The code to control the Keysight B1500 that was used to perform the measurements is available at GitHub [39] and the Python library that was developed to simulate the control performed by the proposed DC source is available at GitHub [40]. The figures were created using Matplotlib [41] Data supporting this work will be uploaded to an online repository.

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**Author contributions** P.A.M. and S.G. performed the experiment. A.E.M., R.D., P.G. and S.E. fabricated the memristor devices. P.A.M. analysed and post-processed the measurement and simulation data. P.A.M., S.G. and M.A.R. developed the simulation framework Y.B., D.D. and M.P.L. conceived and supervised the project. P.A.M. wrote the manuscript with input from all of the authors.

**Competing interests** The authors declare no competing interests.

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METHODS

Fabrication of a TiO$_2$-based memristor. The sample that was used for the measurements presented in this article followed our fabrication process of CMOS-compatible Al$_2$O$_3$/TiO$_2$-$x$ memristor devices described in [19], with two main differences: the TiO$_2$ layer is 15 nm thick, and the electrodes are 200 nm wide.

Electrical characterizations. All of the electrical characterizations were conducted on a Keysight B1500 using the WGFMUs module enabling the generation of the 200 ns write pulses paired with a Lakeshore CRX-VF probe station allowing for measurements down to approximately 2 K. The WGFMUs are controlled using a GPIB-USB connection along with a custom C++ script based on a Keysigh library [39]. The script allows us to perform multilevel resistance programming, as well as the measurement required for the fitting of our simulation model.

Read variability assessments. The read variability of a memristor is measured by biasing the device at the voltage that is typically used for read pulse (i.e., 0.2 V). The current flowing through the memristor is measured every 10 ps (sampling rate $f_s = 100$ kHz) for 10 s because the B1500 analyzer is limited to a maximum of four MSamples. Each sample point is the result of an averaging over 10 ps. This approach allows us to smooth the read variability leading to a smaller standard deviation in the Gaussian fit, while replicating the action of a read pulse used in multilevel programming measurements. The experimental data can be fitted by a Gaussian to estimate the reading variability of the device. We conducted these measurements on the same memristor at room temperature and 4 K (see Supplementary Fig. 3). The coefficients extracted from the linear regression applied to the post-processed measurement data are used to complete our simulation model and implement variability to the emulated memristor.

Simulations. The simulation framework was developed as a two parts (classical electronics and quantum) simulator. The classical simulations are based on Kirchhoff’s laws, the differential amplifier equation and the data driven model giving the memristor resistance with respect to the write pulse applied [33]. We added additional parameters to the data driven model to replicate basic non-idealities of the memristor, such as read and write variability, to more accurately predict the DC source behaviour. The quantum simulations are limited to the plotting of stability diagrams. We used the equations of the electron transport through a double quantum dot in reference [38] to determine the double quantum dot occupation with respect to the gate voltages ($V_g1$ and $V_g2$) under the assumption of solely Coulomb blockade. The stability diagrams presented in this article are plotted by derivating the dot occupation with respect to both variables ($V_g1$ and $V_g2$). The quantum simulation can be ran for different existing quantum dots. We used capacitance parameters from the University of New South Wales from reference [42] as a standard but implemented quantum dot parameters from other leading groups [13, 43–46]. These parameters were extracted by post-processing available stability diagrams using electron transport equations. The quantum simulation is temperature-dependent, which allows for the simulation of hot silicon quantum dots [7, 8]. The memristor model can also be changed according to the working temperature, either at 4 K or at room temperature (all of the simulation results that are presented in this article used the 4 K memristor model).

| Parameter | Value       | Unit |
|-----------|-------------|------|
| $C_{g1}$  | $1.03 \times 10^{-18}$ | F    |
| $C_{g2}$  | $1.03 \times 10^{-18}$ | F    |
| $C_m$     | $4.0 \times 10^{-19}$ | F    |
| $C_L$     | $5.0 \times 10^{-18}$ | F    |
| $C_R$     | $5.0 \times 10^{-18}$ | F    |
| $T$       | $10^{-3}$   | K    |

**TABLE I: Parameters of the double quantum dot for the simulation.** The quantum dot parameters were extracted by post-processing stability diagrams from reference [42].

| Parameter | Value       |
|-----------|-------------|
| $R_{on}$  | $1.8 \times 10^3 \Omega$ |
| $R_{off}$ | $16.0 \times 10^3 \Omega$ |
| $A_p$     | $2.57 \times 10^2$ |
| $A_n$     | $-1.01 \times 10^2$ |
| $t_p$     | $-1.81$ |
| $t_n$     | $-5.53 \times 10^{-1}$ |
| $a_p$     | $3.33 \times 10^{-1}$ |
| $b_p$     | $1.87$ |
| $a_n$     | $3.33 \times 10^{-1}$ |
| $b_n$     | $1.87$ |
| $r_p0$    | $9.23 \times 10^3$ |
| $r_p1$    | $-6.34 \times 10^3$ |
| $r_n0$    | $-4.59 \times 10^3$ |
| $r_n1$    | $-1.60 \times 10^4$ |

**TABLE II: Fitted parameters of a memristor.** These parameters were fitted on a 4.2 K pulsed measurement performed on a memristor. The fitting of this Data-driven model is presented at the Supplementary Figure 2 and extensively presented in Reference [33].
Supplementary Fig. 1: Voltage output of the memristor-based DC source. a. Detailed voltage output of a 9-memristor DC source with a five-state unique distribution for each memristor. The voltage step between consecutive voltages is not constant, as the zoom-in in the bottom inset emphasizes. b. Schematic representation of a five-state unique distribution for a four-memristor DC source. The minimum and maximum target resistance are equal for all of the distributions because these values are tied to the memristor’s properties. The distribution of memristor 1 (down triangle) represents the default distribution when the memristors share the same distribution.

Supplementary Fig. 2: Fitting of the data driven memristor model [33] on measurements performed at 4.2 K. We apply multiple pulse trains of N write/read pulse sequences to the memristor. The pulse amplitude is increased linearly after each pulse train. During a pulse train, the polarity of the pulse is changed after N/2 write/read sequences. The fitting allows us to extract the parameters that were used to model the memristor pulsed behaviors used in our simulations. We used a write pulse width $t_w = 200$ ns and a write pulse amplitude $A_w \in [0.8, -0.8, 0.9, -0.9, 1.0, -1.0, -1.1]$. 350 read/write pulse sequences were applied for each amplitude. We used the same read pulses parameters as the multilevel programming: $t_r = 10$ µs and $A_r = 0.2$ V. The fitted parameters are used in the simulations presented in this article and are available on our GitHub repository [40] and at Table II.
Supplementary Fig. 3: Reading variability of a memristor crosspoint a. Gaussian fit of a read variability measurement at 300K. From this fit, we can extract the read variability of the memristor for a given resistance state. b. We can fit the variability by reproducing the previous measurement and fit for various resistance states of a single memristor, which increases linearly with the resistance between the LRS and HRS resistance states. One can notice a slight offset in read variability between cryogenic and room temperatures, suggesting that cooling down memristors will not decrease the read variability.