Development of a simulated trigger generator for the ALICE commissioning

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Abstract. This paper will describe the hardware and the software developed to build a random trigger simulator used to test the detectors of the ALICE experiment. It will also describe the tests performed in our laboratory at CERN on the random trigger generator to confirm its correct behavior and its installation details in one of the counting rooms of ALICE, where it provides the triggers for all the sub-detectors.

1. Introduction
ALICE (A Large Ion Collider Experiment)[1] is one of the six experiments constructed at the Large Hadron Collider (LHC) optimized for the study of heavy-ion collisions.

Figure 1. The ALICE detector.

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The main aim of the experiment is to study the behavior of strongly interaction matter and quark gluon plasma.

Before the real physic interactions, that will take place with the start-up of the LHC, the 18 sub-detectors composing ALICE have been extensively tested using the cosmic rays flux and a random trigger generator. The Random Trigger Generator (RTG) has been used to generate the same trigger frequencies foreseen during Pb-Pb and heavy ion interactions, up to 40 MHz, in order to verify the capability of the whole ALICE detector to collect data during the most delicate phase of its life.

The RTG is able to provide 6 trigger sequences, defined as a bit streams of 0 and 1, at the same time with different probabilities. These 6 different sequences are combined together by the Central Trigger Processor (CTP)[2]. When the CTP receives in input a bit equal to 1, it generates a trigger and sends it to all the sub-detectors involved in the data acquisition. The data obtained using the random trigger contains the noise of each sub-detectors.

The RTG system is composed by:

- a software part that generates the binary files containing the bit streams used to produce the trigger and that provides a control interface of the RTG board;
- an hardware part, the RTG board, that generates the trigger sequences and sends them to the CTP.

2. The RTG board

The RTG board is composed by three different type of cards connected together (Fig. 2):

- one D-RORC card (DAQ Read-out Receiver Card)[3],
- one daughter card,
- two TTCrq cards(Timing Trigger Control)[4].

![Figure 2](image.png)  
**Figure 2.** D-RORC card (a), daughter card (b), TTCrq cards (c), the assembled RTG board (d).
2.1. The D-RORC card
The D-RORC[3] (Fig. 2a) is the main component of the RTG board. It is an high speed readout PCI-X based card that can provide a throughput of 400 MB/s using DMA (Direct Memory Access) access to the PC memory.

Because of the firmware and the hardware of D-RORC are well known within the ALICE DAQ[5] collaboration, indeed this card is already used in ALICE to receive all the data coming from the detectors, with a firmware modification has been possible to use it for the purpose.

2.2. The daughter card
The daughter card (Fig. 2b) provides all the additional inputs/outputs needed by the RTG board to work properly. This board can be easily plugged to the D-RORC card via the four connectors present on one side (see Fig. 2a highlighted in red). Through these connectors the daughter card receives in input all the trigger information, read from the PC memory. Then there are two additional inputs dedicated to the LHC clock, necessary to synchronize the trigger sequences with the LHC clock. Finally two LVDS (Low-voltage differential signaling) outputs provide two trigger sequences to the CTP system.

2.3. The TTCrq board
The TTCrq[4] (Fig. 2c) is a board that hosts a custom IC (Integrated Circuit) designed by CERN, the TTCrx, that acts as interface with the Timing Trigger Control of the LHC experiment. TTCrx provides the clock and all the necessary control/synchronization information, such as:

- the 40.08 MHz LHC clock signal,
- the trigger signals (L0, L1, L2),
- its associated bunch and event numbers.

2.4. The RTG board
The RTG (Fig. 2d) board needs to be plugged into a PCI-X slot to get:

- power supply (+3.3V) from the PCI bus lines,
- access to the DMA, to retrieve binary files (containing the bit pattern used as trigger sequence) stored in the PC memory.

![Figure 3. The RTG board installed in a PCI-X slot.](image)
The RTG board receives in input two LHC clock signals through optical fibers from the TTCrq boards, and it uses them to serialize the bit pattern necessary to generate the trigger sequence.

It generates as output two LVDS trigger signals connected via lemo cables to the CTP. Using the LHC clock signal of 40MHz, the RTG board is able to provide in input to the CTP a maximum trigger rate frequency of 40MHz.

In figure 3 the RTG board installed in the PCI-X slot together with the input LHC clock signals and the LVDS trigger output are shown.

![Figure 3. The RTG board installed in the PCI-X slot.](image)

In figure 4 the main components of the RTG board (D-RORC, daughter card and TTCrq cards), with its PCI interface, optical inputs and its LVDS output signals are shown.

![Figure 4. The RTG main components.](image)

3. The RTG firmware
As ALICE readout DAQ board, the main task of the D-RORC is to receive the serial data from different detectors and to store them in the PC memory waiting to be processed. The D-RORC firmware uses DMA operations through the PCI bus, to store the data into memory pages. The DMA reduces the overhead of the software and the installation of extra buffers on the board, indeed as soon the software provides a free memory page the D-RORC writes in it. Using D-RORC in RTG applications, the algorithm is almost the same but it is executed in the opposite direction: instead to fill free memory pages with the data, as during the DAQ operations, the RTG board receives memory pages already filled by the software and has to transmit them in serial way. While the random trigger software loads the binary file, containing the trigger sequences in the memory, the RTG board reads them from the memory pages (Fig. 5) and serializes these sequences at 40MHz providing a throughput of 40Mbit/s.
4. The RTG software
The RTG software, all written in C language, has been developed to pilot the RTG board. It is essentially composed by two main parts:

- the RTG control software: its main target is to start and to stop the generation of the trigger or to enable/disable the outputs to the CTP;
- the Sequence generator: that creates the binary file with the desired characteristics to be used as trigger.

Moreover a very useful GUI (Graphic User Interface), written in TCL/TK, permits even to the less expert users to operate the system without problems generating the desired triggers (Fig. 6).

4.1. The RTG control software
This part of the software handles all the communications with the RTG board. A software layer, the rorc-driver, provides all the necessary API (Application Program Interface) to communicate and control the D-RORC board. The main tasks of this software are (Fig. 7):

- to check if the board is properly installed and available to be used;
- to initialize the board;
- to load the binary file containing the trigger sequence in the PC memory,
- to start and to stop the generation of trigger,
- to enable or disable the different outputs of the board.
4.2. Sequence generator
This software has been developed to create custom trigger sequences with different probabilities. It takes in input several parameters and it generates a binary file containing the desired sequence, it needs:
- number of bunch crossing to generate,
- a random generator seed,
- a bunch crossing schedule file: describing time moments in the orbit cycle at which physics bunch crossing are possible. They are defined by LHC, by default there are 3564 bunch crossings in the orbit.

Once the program has finished to generate the binary file, this is loaded directly into the PC memory waiting to be read out by the RTG board.

5. Commissioning of the RTG
Before installing the RTG system at Point 2, where the ALICE experiment takes place, it was tested to verify its correct behavior. The first step was to verify that the trigger signals were correctly generated. A LVDS/CMOS (Complementary Metal Oxide Semiconductor) converter was connected to the output of the RTG board and this signals were observed to the oscilloscope.

Once verified that the board was able to provide clean and correct signals, the RTG test set-up has been connected to the CTP system installed in the trigger laboratory in order to verify that the RTG board provided the right trigger sequence.

As last test the RTG board has been integrated in the ALICE experiment. Three RTG boards, installed in the ALICE counting room named CR1 (Counting Room), have been connected.
through 6 LEMO cables (one for each trigger sequence), to the CTP system situated in the experiment cavern (Fig. 8).

Figure 8. The RTG system installed in the ALICE experiment.

After the installation, the RTG system has been successfully used for 880 runs, for a total of 228 hours. The RTG has been used to test all the ALICE detectors, during the commissioning phase in 2008. During that period more than 40 trigger sequences with different probabilities have been created using the RTG software.

6. Conclusions
The Random Trigger Generator has been developed to generate the same trigger frequencies foreseen during Pb-Pb and heavy ion interactions.

The RTG is able to provide 6 trigger sequences with different probabilities.

The RTG board provides a throughput of 40Mbit/s, that corresponds to a maximum trigger frequency of 40 MHz.

The RTG works and well, it has been used to test all the ALICE detectors, during the commissioning phase in 2008. More than 40 trigger sequences with different probabilities have been created during the 880 working hours. The RTG is still in use and will be used during all the commissioning phase in 2009.

References
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