Research on Fault Injection Method for Testability Verification Test

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Abstract. Aiming at the problems of weak generality of fault injection method and inaccurate reproducibility of fault signal caused by abstract failure simulation method when fault injection is applied to complex equipment with high integration, a general fault injection method is proposed. Firstly, the principle and effectiveness of fault injection are analysed, and the mode and purpose of fault injection are defined. Then, the basic principles of three fault injection methods are studied to provide a basis for the research of general injector. Finally, a failure simulation method based on mixed signal model is proposed to achieve more accurate and simple fault reproduction. The fault injection method is applied to a certain type of control system. The results show that the method can provide comprehensive and accurate elements for fault signals to be simulated in the fault signal simulation stage, and improve the injection efficiency of fault samples in testability verification test.

1. Introduction

Testability is a design characteristic that can determine the working state of the product in time and accurately and effectively isolate its internal faults [1]. It is an important part of the general quality characteristics of equipment, and the better testability design is the premise and key to improve the maintenance and support level of electronic equipment [2]. Testability verification test is the basis of evaluating the testability level of equipment, which is widely concerned by design, development and finalization. Testability verification test based on fault injection is an effective means to evaluate the testability level of equipment [3]. Fault injection refers to the use of specific equipment to generate fault signals that may occur in the operation of equipment, and load them to a designated location to simulate the typical fault mode of equipment. Compared with simulation-based and usage-data-based testability verification tests, the fault injection method is applied to the actual installation, and the complex simulation model is not needed. It can simulate the equipment failure mode quickly and comprehensively, and can effectively save the test cost and improve the test accuracy.

With the continuous updating of equipment, large-scale integrated circuits and ultra-high-speed integrated circuits gradually occupy the dominant position in electronic equipment. Compared with traditional systems with discrete components, integrated circuit systems are tightly packaged, highly
integrated and have complex functional structure, which makes failure simulation and fault injection more difficult. Literature [4] studied the testability verification system of radar equipment based on virtual instrument, and used virtual environment to inject fault. Literature [5] designed the fault injection system of board level circuit. Literature [6] studied the fault injection system of fire control system. Most of the above fault injection methods are aimed at specific injection objects, and failure simulation lacks consideration of UUT test implementation mechanism.

2. Fault injection principle

2.1. Basic principle of fault injection

The principle of fault injection is shown in Figure 1. A system is composed of N units under test. During the testability verification test, according to the fault samples determined by the verification test scheme, the fault injection system is used to inject the fault into the corresponding parts of the system to cause the system failure, and then to verify the testability indexes of automatic test equipment (ATE) or built-in test equipment (BITE) of the system.

2.2. Effectiveness analysis of fault injection

The purpose of fault injection is to simulate the faults in the actual operation of equipment by loading fault signals. The effectiveness of fault injection depends mainly on two factors: (1) whether the simulated fault signal can be loaded to the correct location, that is, whether the physical location can be accessed by hardware injection and whether the specified location can be read and written by software injection. (2) Whether the injection can be accurately located or not, the so-called accurate injection indicates that after loading the simulated fault signal into the tested equipment, the fault behavior or the state of the equipment is close to the actual fault behavior or the state of the equipment.

Minimum complete detection/isolation state set refers to the minimum state set that can correctly detect/isolate the occurrence of a fault for a specific fault mode. If the state space after fault injection can contain minimal complete detection/isolation state set, it is considered that the injection of the fault mode is effective. The injection rate of fault samples can be used as a mathematical model to quantitatively express the effectiveness of fault injection, such as equation (1).

\[
R_{FSI} = \frac{N_{IF}}{N_F} \times 100\%
\]

Where, \(R_{FSI}\) is the injection rate of fault samples, \(N_{IF}\) is the effective injection sample size, and \(N_F\) is the selected fault sample size. \(R_{FSI}=1\) is the ideal injection result.
3. Research on fault injection method

3.1. Hardware fault injection
Hardware fault injection method refers to the introduction of fault signals into the test object through additional hardware, mainly including the following.

(1) Fault injection based on probe mainly uses the probe to contact the pin and pin connection of the injected device, and realizes on-line or off-line failure simulation by changing the pin output signal or pin interconnection structure. The principle is shown in Figure 2.

![Figure 2. Fault injection principle based on probe.](image)

(2) Fault injection based on adapter boards is mainly to add an exclusive adapter board between two or more circuit board interfaces, which realizes on-line or off-line simulation of faults by changing the link physical structure, signals and data in the circuit board interconnection links. The principle is shown in Figure 3.

![Figure 3. Fault injection principle based on adapter board.](image)

(3) Fault injection based on plug-in, the failure is simulated by plug-in components, circuit boards, wires, cables and so on, on the premise of ensuring that no irrecoverable impact is caused.

(4) Fault injection based on bus, system bus fault injection method can be used for failure mode of board interface or bus. The essence of system bus fault injection is to disconnect the original transmitted signal at the desired address and replace the original message with fault signal according to the requirements of injection conditions, and transmission to the lower circuit. The principle is shown in Figure 4.
3.2. Simulation fault injection
The simulation fault injection technology is the process of system simulation modeling, and modifying the component model specified in the normal state circuit under the simulation environment to form the simulation fault model (component model reorganization), so as to make the system model fail. Its working principle is shown in Figure 5.

3.3. Software fault injection
Software fault injection is mainly used in software programs or systems. The object of software fault injection can be either an operating system or an application program. Both of them are implemented in the form of embedded fault injection. According to injection time, it can be divided into compile-time fault injection and run-time fault injection. The injection principle is shown in Figure 6.
4. Failure simulation based on mixed signal model

In order to implement accurate fault injection test, the subjects in the test must establish an appropriate simulation test environment, provide excitation signals including working environment signals and cross-linking signals between components, and drive the corresponding LRU to run. The external working conditions and internal working characteristics of the subjects in the fault injection test need to be simulated. Signal is the basic element of establishing injection system and automatic test system. The basic characteristic information of signal includes: 1) signal function (such as signal source, sensor, load, etc.); 2) signal type (such as DC signal, AC signal, etc.); 3) signal parameters: function of parameters, range of parameters, resolution or accuracy. 4) Signal connection: wire and port.

The existing signal-oriented failure simulation lacks consideration of the test implementation mechanism of the subject, and the fault model is too abstract to reproduce accurately. Therefore, in testability verification test, failure simulation should fully consider the test implementation mechanism. In order to simulate and reproduce the fault signal accurately, a failure simulation method based on mixed signal model is proposed, that is, a fault model driven by the basic characteristic information of the signal and the test and diagnosis information is established, which is realized by software or hardware. The mixed signal model of failure simulation is shown in equation (2).

$$ F = I[f(S_a, S_t, S_p, S_j), L, F_B] $$  

Where, $$ f(S_a, S_t, S_p, S_j) $$ is the basic characteristic of the fault signal, that is, the signal part that the fault injector must simulate. $$ S_a $$ is the fault signal, $$ S_t $$ is the fault signal type, $$ S_p $$ is the fault signal parameter and $$ S_j $$ is the connection relationship. $$ L $$ is the location of the fault injection point, which can lead to the desired fault mode. There are more than one alternative location of $$ L $$, which can be optimized by the relationship between the top event and the minimum cut set in the fault tree. $$ F_B $$ is the fault behavior vector, which is used to characterize and verify the accuracy of failure simulation.
According to the failure mode, effect and criticality analysis, the failure sample library of the system can be obtained. 63 failure samples to be injected are selected, including 47 failure modes. Because the bus definition of the system is known, the fault injection method based on bus is mainly adopted. For hardware failures which are difficult to simulate and physically accessible, other methods such as probe-based fault injection are adopted. Fault injection tests are carried out on 63 fault samples of the system. For space limitation, taking the A/D conversion module as an example, the failure model obtained from equation (2) is shown in Table 1.

Table 1. Failure model based on signal basic characteristic information.

| Failure mode                          | Fault model parameters |     |     |     |     |     |
|---------------------------------------|------------------------|-----|-----|-----|-----|-----|
| Channel switching failure             | short circuit          | alternating current | -   | -   | Interface | (0,1,0,1) |
| Decoding Control Function Failure      | Open circuit           | on-off         | -   | -   | Interface | (0,0,1,1) |
| Input voltage cannot be amplified     | Open circuit           | on-off         | -   | -   | Interface | (1,1,1,1) |
| D/A Conversion Fault                  | Fixed low              | direct-current | -   | -   | Interface | (0,0,0,1) |
| A/D Conversion Fault                  | short circuit          | alternating current | -   | -   | Interface | (0,1,1,1) |

The same failure simulation method is used to inject the fault into the system, and 82.35% fault injection rate can be obtained by equation (1). This is due to the complexity of fault propagation of new equipment and highly integrated design, which results in limited access depth of fault injector and relatively low fault injection rate.

5. Conclusion
Aiming at the problem of weak universality of fault injection method, a general fault injection method is studied in this paper. According to the correlation between the basic characteristic information of fault signal and the test diagnostic information in fault injection test, a fault simulation method based on mixed signal model is proposed to realize more accurate and simple fault reproduction. Example shows that this method can provide comprehensive and accurate elements for failure signals in the failure signal simulation stage, and improve the injection efficiency of failure samples in testability verification test.

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