A Multi-Gbps Unrolled Hardware List Decoder for a Systematic Polar Code

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Abstract—Polar codes are a new class of block codes with an explicit construction that provably achieve the capacity of various communications channels, even with the low-complexity successive-cancellation (SC) decoding algorithm. Yet, the more complex successive-cancellation list (SCL) decoding algorithm is gathering more attention lately as it significantly improves the error-correction performance of short- to moderate-length polar codes, especially when they are concatenated with a cyclic redundancy check code. However, as SCL decoding explores several decoding paths, existing hardware implementations tend to be significantly slower than SC-based decoders. In this paper, we show how the unrolling technique, which has already been used in the context of SC decoding, can be adapted to SCL decoding yielding a multi-Gbps SCL-based polar decoder with an error-correction performance that is competitive when compared to an LDPC code of similar length and rate. Post-place-and-route ASIC results for 28 nm CMOS are provided showing that this decoder can sustain a throughput greater than 10 Gbps at 468 MHz with an energy efficiency of 7.25 pJ/bit.

I. INTRODUCTION

Polar codes were recently selected for the next-generation mobile communications standard that is currently under development by the 3GPP due to their excellent error-correction performance at short to moderate blocklengths under SC decoding [1, p. 123]. Unfortunately, most SCL decoder implementations in the literature still suffer from low throughput and high decoding latency [2–5]. Several algorithmic and architectural improvements have been proposed in order to remedy this situation. For example, multi-bit SCL decoding [3] can significantly reduce the decoding latency of SCL decoding, but at a very large cost in terms of the required hardware resources. A similar approach, which groups multiple bits into symbols and transforms the SCL decoder to a symbol-based SCL decoder was presented in [6] and is shown to offer similar decoding throughput improvements compared to standard multi-bit SCL decoding, but with lower decoding complexity. A different approach was taken in [7] where the proposed Fast-SSC-List decoding algorithm employs specialized decoding units for smaller sub-codes of the polar code in order to reduce the decoding latency.

Unrolled decoders are known for their tremendous throughput [8–11]. They offer at least one order of magnitude improvement in throughput with respect to standard decoders at the cost of larger area requirements. While this unrolling technique has been applied to SC-based polar decoders before [9, 10], it has not yet been applied to a hardware successive-cancellation list (SCL)-based decoder. Applying the technique to the original SCL decoding algorithm [12] would result in a hardware implementation with very high area complexity. Thus, in this paper, we propose an unrolled hardware implementation of the Fast-SSC-List decoding algorithm [7]. We show that, for a (512, 427) systematic polar code, the throughput is an order of magnitude higher than the state of the art, while the error-correction performance is better than that of the (576, 480) low-density parity-check (LDPC) code from the IEEE 802.16e standard [13].

Outline: The remainder of this paper starts with Section II by providing the necessary background, consisting of a brief review of polar codes and an introduction to SCL-based decoding algorithms. Moreover, we present a comparison of the error-correction performance of an SCL-decoded polar code against that of an LDPC code from the IEEE 802.16e standard. Section III also briefly reviews the Fast-SSC-List decoding algorithm. Section IV describes our adaptation of the fully-unrolled and pipelined hardware architecture to SCL decoding. Section V discusses implementation details and provides post-place-and-route (PAR) ASIC area, timing, and power results for the 28 nm UTBB-FD-SOI CMOS technology from ST Microelectronics. A comparison against the state-of-the-art SCL-based decoder implementations from the literature is also carried out in Section V. Finally, Section V concludes this paper.

II. BACKGROUND

A. Polar Codes

In his original work, Arıkan used a linear transformation of a vector of bits that can be shown to lead to a polarization phenomenon, meaning that some of these bits experience almost noiseless transmission channels while the remaining bits experience almost completely noisy transmission channels. Polar codes exploit this polarization phenomenon to achieve the symmetric capacity of memoryless channels as the code...
length goes to infinity. More specifically, to construct an \((N, k)\) polar code, the \(N - k\) least reliable bits (i.e., the bits that experience the \(N - k\) worst transmission channels), called the frozen bits, are set to zero and the remaining \(k\) bits are used to carry actual information.

Polar codes provably achieve capacity when decoded using the low-complexity successive-cancellation (SC) algorithm [14]. However, with SC decoding, the error-correction performance of polar codes at short to moderate length is in general worse than the error-correction performance of other modern channel codes. It was shown that decoding polar codes using an SCL-based decoding algorithm significantly improves the situation [12], especially when concatenating the polar code with a cyclic redundancy check (CRC) [12, 15].

It was shown in [16] that polar codes can be encoded and decoded systematically, leading to an improved bit-error rate (BER) without affecting the frame-error rate (FER). In this work, systematic polar codes are used.

### B. Successive-Cancellation List Decoding

The SC decoding algorithm is a greedy algorithm: it uses the channel output \(y_{n+1}\) and the previous bit estimates \(\hat{u}_i\) to estimate the value of bit \(\hat{u}_i\). Therefore, as soon as an error occurs a frame will inevitably be in error as past decisions are never revisited. SCL-based decoding algorithms for polar codes are also greedy in the sense that they sequentially build the most likely codewords. However, at each step, instead of considering only the most likely bit value, both possible bit values—0 and 1—are considered. Thus, as the decoding proceeds a constrained list of up to \(L\) potential candidate codewords is built, and a reliability metric is calculated for each path along the way. At the very end, the most likely codeword among the candidates in the list is selected. In the case of the CRC-aided SCL (CA-SCL) decoding algorithm the polar code is concatenated with a CRC and when decoding ends the CRC is calculated for all \(L\) candidate codewords. The most likely codeword with a calculated CRC that matches the expected CRC is selected as the estimated codeword. If none of the CRCs matches the codeword with the best reliability is selected.

Fig. 1 shows the error-correction performance of a (512, 427) systematic polar code decoded using the SCL and the CA-SCL algorithm with \(L = 2\). An 8-bit CRC is used for the CA-SCL decoding algorithm. The performance is simulated for random codewords, using a binary phase-shift keying (BPSK) modulation over an additive white Gaussian noise (AWGN) channel. Both FER and BER of the (576, 480) LDPC code from the IEEE 802.16e standard [13] are included for comparison. The LDPC code is decoded with a layered schedule using the self-corrected min-sum algorithm [17]. It can be seen that the chosen polar code compares favorably against an LDPC code of similar length and rate even with a list size as small as \(L = 2\). It should also be noted that, in this particular scenario, for a targeted FER of \(10^{-3}\), it is beneficial to not concatenate the polar code with a CRC. This observation was also made in [2] i.e., in some cases, it is more beneficial—error-rate wise—to not concatenate a polar code with a CRC.

Unfortunately, SCL decoding involves the exploration of multiple decoding paths simultaneously as well as a costly path metric sorting step. Thus, hardware implementations of SCL decoding are typically much slower than state-of-the-art SC-based decoders. As mentioned in the introduction, multiple algorithms employing multi-bit decisions have been proposed [3–7] to significantly reduce the decoding latency and increase the decoding throughput of SCL decoding. The hardware implementation presented in this paper is based on the Fast-SSC-List decoding algorithm proposed in [7].

### C. Fast-SSC-List Decoding

SCL decoding uses the SC decoding algorithm, a sequential algorithm proceeding bit by bit, which effectively limits the achievable speed of hardware implementations. Recognizing that a polar code is the concatenation of smaller constituent codes, it was shown in [18] that many constituent codes could be more efficiently estimated with dedicated decoders compared to using the processing elements implementing the SC algorithm. This led to the Fast-SSC decoding algorithm, where multiple bits are estimated simultaneously. In [7], it was proposed to adapt the Fast-SSC algorithm to SCL decoding.

Fast-SSC-List decoding provides algorithms for four different constituent codes: Rate-1, Rate-0, Repetition, and single-parity check (SPC). Each algorithm consists of two parts. The first part is the candidate generation, it consists of creating the \(L\) most likely bit estimate vectors \(\beta\). The second part consists of computing the corresponding path reliability metrics \(PM\).
Note that for a Rate-0 constituent code, only one path reliability metric is computed as there is only one possible candidate estimated bit vector, the all-zero vector.

While the proposed algorithms for the Rate-0 and Repetition codes are exact, approximations are used for Rate-1 and SPC codes. Thus, although it can be kept small, there is some coding loss inherent to the Fast-SSC-List decoding algorithm compared to the SCL algorithm.

III. UNROLLED AND PIPELINED SCL DECODER ARCHITECTURE

As we have already mentioned, unrolled decoder architectures provide extremely high decoding speeds. In an unrolled decoder architecture, each and every operation required is instantiated in hardware so that data can flow through the decoder with minimal control. An unrolled and pipelined architecture for SC-based polar decoding was first described in [9], and later improved and generalized in [11]. In this section, we explain how the unrolled fast-SC decoder architecture of [11] can be extended to Fast-SSC-List decoding [7] by means of a small example.

Fig. 2 shows an implementation example of a fully-unrolled deeply-pipelined Fast-SSC-List-based decoder for an (8, 4) polar code with \( L = 2 \). The \( F \) and \( G \) blocks, generating the soft-input log-likelihood ratios (LLRs) to the constituent decoders, implement the same functions as in the SC algorithms using the min-sum approximation [19]. The \( \text{Combine} \) block corresponds to one stage of a polar encoder. The “&” blocks are bit-vector joining operators, and registers are shown in light gray, a Repetition node in green and SPC nodes in orange.

Each register denoted \( \ell \) is used to store one of the paths that survived, expressed as a partial sum. The \( \ell \)-registers at the output of a concatenation block “&” have the surviving paths concatenated with the \( L \) new bit estimate vectors \( \beta \) coming out of the constituent decoders. Thus, at the output of a sorting step—denoted \( L \)-Best Candidate in Fig. 2—a register \( \ell \) contains the \( L \) paths that survived, also expressed as a partial sum. Thus a \( \text{Combine} \) block updates the partial sum by operating on the right hand side bits of an \( \ell \)-register.

In this example, the \( G \) functions are calculated preemptively as a Repetition node allows for only 2 possible outcomes and as the first path fork occurs there, the generated paths at the output of the Repetition node will necessarily be retained among the \( L = 2 \) best candidates. For the general case however, this cannot be applied as the newly estimated paths (or partial sums) may be combined with different path sources before entering a \( G \) function.

While not illustrated in Fig. 2, a figure depicting a very small polar code, as soon as LLRs \( \alpha \) need to be retained past a sorting step, multiplexers have to be inserted after each sorting block. Those multiplexers allow the decoder to select the LLR values corresponding to the surviving path sources.

IV. IMPLEMENTATION AND RESULTS

For this paper, we have implemented a fully-unrolled partially-pipelined Fast-SSC-List decoder with an initiation interval \( I = 20 \) and a list size \( L = 2 \). An initiation interval \( I = 20 \) means that a new frame is fed into the decoder every 20 clock cycles. It also means that a new estimated codeword is available at the output of the decoder every 20 clock cycles. The Rate-0, Repetition, and SPC nodes were constrained to a maximum length of 8, 8, and 4, respectively. The information (i.e., rate-1) nodes were not constrained and as a result, the largest one has a length of 128. The SPC node is pipelined over 2 clock cycles to shorten its longest path.

The critical path of the decoder is the sorting block—denoted “\( L \)-Best Candidates” in Fig. 2—; it starts from the output of a register storing a path metric, then through 2 levels of 7-bit comparators and ends into another register storing one of the 2 best path metrics. The clock frequency was selected to obtain an information throughput of 10 Gbps.

A. Methodology

ASIC post-PAR results are for the 28 nm UTBB-FD-SOI CMOS technology from ST Microelectronics using the RVT standard-cell library. Synopsys Design Compiler and Cadence Innovus were used for synthesis and PAR, respectively. Clock
gating was used in order to reduce power consumption. The post-PAR netlist has been simulated for verification as well as for the generation of vectors. These latter ones have then been used to annotate the design data with toggle rates that correspond to steady state operation—i.e. a filled pipeline—in order to extract a meaningful estimation of the average power consumption of 250 random frames. In our results, the decoding latency includes the time required to load the channel LLRs, decode a frame and output the best estimated codeword.

B. Impact of Quantization

All LLRs and path metrics are expressed using the two’s complement representation. The LLR value quantization is denoted as $Q_c, Q_i, Q_f$, where $Q_c$ is the total number of bits used to store a channel LLR. $Q_i$ is the total number of bits used to store internal LLRs and $Q_f$ is the number of fractional bits in both types of LLRs. The number of bits used to represent a path metric is $Q_i + 1$, and path metrics are normalized after each sorting step in order to avoid overflows.

Fig. 3 shows the effect of quantization on the error-correction performance of List-based decoding of a (512, 427) systematic polar code with list size $L = 2$. It can be seen that the coding loss at a FER of $10^{-3}$ or a BER of $10^{-5}$ can be kept under 0.25 dB with many different configurations. Notably, with $Q_c, Q_i, Q_f = 7.6.1$ and 6.5.0, the coding loss at a BER of $10^{-5}$ is approximately 0.10 dB and 0.15 dB, respectively. Thus, the proposed implementation uses $Q_c, Q_i, Q_f = 6.5.0$ and the path metrics are represented using 7 bits.

C. Comparison with the State of the Art

Table I shows the post-PAR results along with the power consumption estimations for our Fast-SSC-List unrolled decoder implementation. Unfortunately, we could not find implementation results of SCL-based decoders for a frame length $N = 512$ in the literature. Thus, the state-of-the-art works included in Table I for comparison are decoders for the closest frame length i.e. $N = 1024$. Their list size, however, is identical. It should also be noted that the other works only present synthesis results and their post-PAR results would most likely be slightly worse both in terms of area and in terms of operating frequency. Since our decoder is for a polar code of higher rate than the other works, we list the coded throughput for fair comparison. Similarly, we also present technology-scaled results, using Dennard scaling laws [20], for fair comparison.

From Table I it can be seen that the coded throughput of the proposed decoder is from 5 to 21 times higher than that of the other works. Latency is from 32% to 74% lower than the other decoders. As the timing constraint was easily met, the clock frequency could be increased to improve throughput and latency at the cost of power consumption. The area of the proposed decoder however is approximately 4 times higher than the normalized area of the $L = 2$ List decoders of [3–5] for $N = 1024$. Nonetheless, the post-PAR area efficiency of our decoder is 1.3 to 5.4 times greater than the normalized post-synthesis area-efficiency results of the other works. This efficiency comes at the cost of reduced flexibility: the proposed decoder only supports one specific polar code i.e., the code length or its frozen bit locations cannot be modified at run time. However, the multi-mode idea for unrolled decoders described in [11] is also applicable to our proposed SCL-based decoder and support for a few more polar codes could be added. Lastly, the power consumption of our proposed decoder is estimated to be of 87 mW, leading to an energy efficiency of 7.25 pJ/bit.

![Figure 3: Effect of quantization on the error-correction performance of Fast-SSC-List-based decoding of a (512, 427) systematic polar code with list size $L = 2$.](image-url)

**TABLE I: Comparison with state-of-the-art List-based polar decoders. Technology-scaled area results for 28 nm CMOS are included at the bottom.**

| Implementation | this work* | [3]* | [4]* | [5]* |
|----------------|------------|------|------|------|
| **Code Length** | 512        | 1024 | 1024 | 1024 |
| **Rate**       | 0.83       | 0.5  | 0.5  | 0.5  |
| **List Size**  | 2          | 2    | 2    | 2    |
| **Algorithm**  | Approx.    | Exact| Approx.| Approx. |
| **Technology** | 28 nm      | 65 nm| 90 nm | 90 nm |
| **Area (mm²)** | 0.87       | 1.06 | 1.98 | 2.32 |
| **Supply (V)** | 1.1        | N/A  | N/A  | N/A  |
| **Frequency (MHz)** | 468 | 500 | 423 | 409 |
| **Latency (µs)** | 0.54       | 2.04 | 0.79 | 0.87 |
| **Coded T/P (Gbps)** | 12.0 | 0.5 | 1.3 | 2.4 |
| **Area Eff. (Gbps/mm²)** | 13.79 | 0.47 | 0.67 | 1.04 |
| **Power (mW)** | 87         | 395  | N/A  | N/A  |
| **Energy Eff. (pJ/bit)** | 7.25 | 790 | N/A  | N/A  |

*Post-layout results, 80% utilization and timing is met. *Synthesis results.
V. Conclusion

In this paper, we proposed a List-based decoder hardware implementation for a systematic polar code with better error-correction performance than an LDPC code of similar length and rate from the 802.16e standard. Post-PAR ASIC results for the 28 nm UTBB-FD-SOI CMOS technology from ST Microelectronics demonstrated that the proposed decoder is capable of sustaining a throughput greater than 10 Gbps with an energy efficiency of 7.25 pl/bit at a clock frequency of 468 MHz. These results show excellent energy efficiency at the cost of increased area with respect to existing implementations. Yet, the post-PAR area efficiency was shown to be 28% better than the normalized post-synthesis area efficiency of the best state-of-the-art SCL-based decoder in the literature. The key ingredients to achieve these results were to adopt the Fast-SSC-List decoding algorithm to reduce complexity, to adapt the unrolling technique to List-based decoding to increase speed, and to use clock gating to greatly reduce the power consumption.

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