Delta-Sigma Digital Current Sensor Based On GMR

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Abstract. This paper presents an integrated delta-sigma digital current sensor. With high sensitivity and good linearity, GMR sensor is a good choice for current measurement application. In this design, a GMR sensor which is configured as a Wheatstone bridge of four spin-valve sensing elements is integrated with CMOS signal processing circuit together, and the output signal is converted to digital domain by an on-chip 10-bit delta-sigma ADC. The whole circuit is designed and simulated using CSMC standard 0.5 μm process.

1. Introduction

Current sensors are widely used as feedback devices in field industrial equipment, power system protection and various test-controlled systems. Defined by the working principle, current sensors could be classified as traditional current transformer, current shunt, Rogowski current sensor, fluxgate current sensor and Hall-effect current sensor, AMR current sensor and GMR current sensor etc. [1].

Nowadays, the most commonly used current sensor is hall-effect current sensor, which is usually used to measure large current. However, due to the low sensitivity and poor temperature stability of hall-effect sensors [2], it could not meet the requirement for precise measurement, especially for low current measurement.

These shortcomings could be overcome by use GMR sensor. Single-module integrated GMR current sensor is tiny. In order to fit for small size sensors, a delta-sigma AD converter using over sampling technology is employed, which provides high resolution and excellent linearity without using precise or trimmed components [3].

In this work, a GMR sensor and a second-order delta-sigma modulator are integrated together. Standard 0.5 μm process is adopted, with the whole system operating under ±2.5 V supply voltage. The simulation shows the sensor could achieve a resolution of 0.5 mA in the operation range of ±80 mA.

2. Integrated digital GMR current sensor design

2.1. Structure and principle
The linear spin-valve sensor [4] is very suitable for small current sensing as it has desired high sensitivity and good linearity. The sensor is with an operation magnetic range of +15 Oe to -15 Oe, no visible hysteresis and the sensitivity is 0.094%/Oe. The designed digital current sensor is shown in Figure 1.
Figure 1. Architecture of current sensor

Shown in Figure 1 are 4 identical spin-valve resistors making up a Wheatstone bridge. The advantage of this configuration is providing temperature compensation. A current wire is placed along with the resistors of the Wheatstone bridge, and the output of the bridge is conditioned and magnified by the conditioning circuit, and then the signal is converted to digital by a 10-bit delta-sigma ADC. According to Ampere Circuit Theorem, when electricity current flowing through an infinitely long wire, the magnetic field strength H induces at the distance r from the wire is \( H = \frac{I}{2\pi r} \). Therefore, if the sensors bridge is put at the place 100 μm to the current wire, a -10 Oe to +10 Oe magnetic field will be induced when the current I varies from -80 mA to +80 mA, and the output of the bridge can reflect the current perfectly.

2.2. Signal conditioning circuit

In order to make the sensor sensitive and accurate, following the Wheatstone bridge a signal conditioning circuit is designed.

The output of the Wheatstone bridge is

\[
\Delta V = V1 - V2 = \frac{V_{dd} - V_{ss}}{R1(1 + \Delta) + R3(1 + \Delta)} - \frac{V_{dd} - V_{ss}}{R2(1 + \Delta) + R4(1 - \Delta)} = (V_{dd} - V_{ss}) \cdot \Delta
\]

here \( \Delta \) is the change rate of the resistors, and it will be zero in ideal case with no current input. In fact, since it is difficult to match the GMR resistors perfectly in the fabrication, plus the interference of ambient magnetic field, output offset is inevitable. It is the main factor that influences the precision of the GMR sensor. Meanwhile, according to the study in [4], the bridge sensor could reach almost 50 mV signal output in the magnetic range of ±10 Oe. In order to convert it into digital signal accurately, a conditioning circuit is used to adjust the bridge sensor signal. From the above discussion, here a two-op-amp instrumentation amplifier and another amplifier are incorporated as the conditioning circuit to compensate the offset [5].

The conditioning circuit is shown in Figure 2. A1, A2 and A3 are three identical amplifiers. A1 and A2 constitute a two-op-amp instrumentation amplifier. V1, V2 are the outputs of Wheatstone bridge, hence

\[
V_{out1} = (V1 - V2) \left( 1 + \frac{R2}{R1} + \frac{2 \cdot R2}{Rg} \right) + V_{ref} \text{ when } R1 = R2 = R4.
\]

With the amplifier A3, Vout2 is opposite with Vout1 referenced to ground when \( R5 = R6 \).
Here, $R_g$ is an external resistor employed to adjust the gain of the circuit. And $V_{ref0}$ is the external reference voltage which is used to compensate the offset of the bridge and keep the output of the sensor zero when there is no signal input.

It requires high stability and low power consumption in the application of the current sensor, hence, a simple two-stage OTA (Operational Transconductance Amplifier) is chosen to realize the modules A1, A2 and A3 in Figure 2.

The two-stage OTA is shown in Figure 3. The circuit operates with $\pm 2.5$ V voltage supply. The pins labeled “In+” and “In-” correspond to the positive input and negative input respectively. Resistor $R_2$ and capacitor $C_1$ are used to optimize the phase margin of the OTA. In order to insure the performance of the circuit, the gain of the OTA should be more than 70 dB, and phase margin more than 60°.

Figure 4 shows the simulation result of the two-stage OTA with CSMC standard 0.5 $\mu$m process. From it we can see the gain is 78dB, phase margin is 65° and bandwidth is more than 100MHz, which are more than satisfactory.
2.3. Second-order delta-sigma AD converter

Delta-sigma AD converter has simple structure and high accuracy, so it is very suitable for using in single-module sensors.

The block diagram of a second-order delta-sigma AD converter is shown in Figure 5. It consists of two parts, one is delta-sigma modulator, and the other is digital filter. Modulator is the hard-core of the delta-sigma AD converter. It consists of two integrators, a 1 bit ADC (a comparator) and a 1 bit DAC (switches). The closed loop forces the value of the feedback signal to track the input value of the modulator. Any difference between feedback and input is accumulated in the integrator until the flip of the ADC output that makes the sign of feedback-input change [3] [6].

![Figure 5. Second-order delta-sigma AD converter](image)

In the current sensor, the expected operation range is ±80 mA and the expected resolution is 0.5 mA, $2^1 \times \frac{160}{0.5} < 2^9$, so a delta-sigma modulator with 9-bit ENOB (Effective Number of Bits) is enough. However, considering there will be some errors, in order to insure the resolution and linearity a 10-bit one is chosen [7] [8].
The circuit schematic of the second-order delta-sigma modulator is shown in Figure 6. Two fully differential folded-cascode amplifiers are used to realize the modules A1 and A2, and a comparator with latch follows the second integrator. In order to avoid the clock feed-through of the switched-capacitor integrator[9], \( \phi_1 \) and \( \phi_2 \), \( \phi_1d \) and \( \phi_2d \) are two-phase non-overlapping clocks, \( \phi_1d \), \( \phi_2d \) are the signal \( \phi_1 \), \( \phi_2 \) with delay respectively. The q is the output of the comparator. When q is high, Vrefh is connected to ip, Vrefl is connected to in, and when q is low, Vrefl is connected to ip, Vrefh is connected to in. Here, Vrefh is 1.5 V and Vrefl is -1.5 V. The sampling capacitor Cs and Cfb both are 1 pf, integrating capacitor Ci is 2 pf.

3. Simulation results
The delta-sigma modulator is simulated based on MATLAB with the output of the instrumentation amplifier as input. Figure 7 shows the model of second-order white noise delta-sigma modulator based on MATLAB SIMULINK. The model includes many non-ideal effects, such as clock jitter, switch nonlinearity, \( kT/C \) noise and amplifier noise etc.

When a 50 Hz, amplitude of 80 mA AC current flowing through the current wire, according to the sensitivity of the spin-valve resistor, the output of the Wheatstone bridge is
\[
\Delta V_{out_{max}} = (V_{id} - V_{ss}) \cdot \Delta H_{max} = 5V \cdot 0.094\% / Oe \times 100 Oe = 47 mV
\]
here \( \Delta \) is the change rate of the resistors. So it would be a sine curve with the same frequency and amplitude of 47 mV. By adjusting the external resistor Rg and external reference voltage Vref, the output of the instrumentation amplifier is in the range \( \pm 2 V \) with no offset.

With the OSR (Over Sampling Ratio) of 128, sampling frequency of 12.5 KHz, the simulation results
of the delta-sigma modulator input and output are displayed in Figure 8. And the power spectral
density of the modulator is shown in Figure 9, from which we can see the SNDR of the modulator is
65.0 dB, i.e. ENOB is 10.49 bits.

![Figure 8. Transient waveforms of Δ-Σ modulator input and output](image)

![Figure 9. PSD of the delta-sigma modulator](image)

4. Conclusions
A delta-sigma digital current sensor with GMR sensing element integrated with an AD converter has
been designed and simulated. In this work, the un-negligible bridge offset is compensated with an
external voltage, and then the output signal is converted to digital with an on-chip 10-bit delta-sigma
ADC.Simulation shows that the power dissipation of the OTA is 369 μW, the calculated power of the
Wheatstone bridge is 5 mW, so the whole dissipation of the sensor should be less than 100 mW. And the
sensor would have the resolution of 0.5 mA which is expected.

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