Characterization of the Outer Barrel modules for the upgrade of the ALICE Inner Tracking System

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ABSTRACT: ALICE is one of the four large detectors at the CERN LHC collider, designed to address the physics of strongly interacting matter, and in particular the properties of the Quark-Gluon Plasma using proton-proton, proton-nucleus, and nucleus-nucleus collisions. Despite the success already reached in achieving these physics goals, there are several measurements still to be finalized, like high precision measurements of rare probes (D mesons, Lambda baryons and B mesons decays) over a broad range of transverse momenta. In order to achieve these new physics goals, a wide upgrade plan was approved that combined with a significant increase of luminosity will enhance the ALICE physics capabilities enormously and will allow the achievement of these fundamental measurements. The Inner Tracking System (ITS) upgrade of the ALICE detector is one of the major improvements of the experimental set-up that will take place in 2019–2020 when the whole ITS sub-detector will be replaced with one realized using a innovative monolithic active pixel silicon sensor, called ALPIDE. The upgraded ITS will be realized using more than twenty-four thousand ALPIDE chips organized in seven different cylindrical layers, for a total surface of about ten square meters. The main features of the new ITS are a low material budget, high granularity and low power consumption. All these peculiar capabilities will allow for full reconstruction of rare heavy flavour decays and the achievement of the physics goals. In this paper after an overview of the whole ITS upgrade project, the construction procedure of the basic building block of the detector, namely the module, and its characterization in laboratory will be presented.

KEYWORDS: Heavy-ion detectors; Particle tracking detectors; Particle tracking detectors (Solid-state detectors)
1 Introduction

ALICE (A Large Ion Collider Experiment) [1] is a CERN experiment, located in one of the interaction point of the LHC collider, designed to address the physics of heavy ions and strongly interacting matter, using nucleus nucleus (A-A) collisions. For these studies proton-proton (p-p) collision analyses are also required as baseline reference, and proton-nucleus (p-A) to discriminate between initial and final state effects. Despite the success already reached in achieving these physics goals, there are several measurements still to be finalized, like high precision measurements of rare probes (D mesons, Lambda baryons and B mesons decays) over a broad range of transverse momenta. The achievement of these goals requires a wide upgrade plan of the ALICE experiment [2] combined with a significant increase of luminosity of the LHC collider. This upgrade plan was already approved and will enhance the ALICE physics capabilities enormously allowing the achievement of these fundamental measurements. The ALICE Inner Tracking System (ITS) detector will play a key role in these studies, and for this reason a wide upgrade program was designed [3] and already started. The plan is to replace completely the present ITS detector with a new one in 2019–2020 during the Long Shutdown 2 (LS2) using an innovative Monolithic Active Pixel silicon Sensor (MAPS), called ALPIDE [4]. The main features of the new ITS are a low material budget, high granularity and low power consumption. All these peculiar capabilities will allow for full reconstruction of rare heavy flavour decays and the achievement of the physics goals. In this contribution there is an overview of the whole ITS upgrade project focusing mainly on the construction and functional characterization procedure of one the basic building block of the new detector, namely the Outer Barrel Hybrid module (OB-HIC).

2 The ALPIDE chip

The new ALICE ITS detector will be realized using a MAPS chip sensor suitably designed for this upgrade. The Pixel Chip of the upgraded ALICE ITS will be produced using the TowerJazz [5] 180 nm CMOS imaging process. It is composed by a high-resistive epitaxial layer on a p-substrate.
Being a quadruple-well process, it offers a deep PWELL, which can be used to shield the NWELL of PMOS transistors. This makes the use of full CMOS circuitry in the pixel area possible without the drawback of parasitic charge collection by those NWELLs. In addition, applying a moderate negative voltage to the substrate can be used to increase the depletion zone around the collection diode and this way improve both the charge collection and the signal-to-noise ratio by decreasing the pixel capacitance. The interconnections between transistor and diodes will be realized using six different metal layers, allowing the integration in the single pixel of a large number of control functions. Data can be transmitted on two different readout ports. A 1.2 Gb/s serial output port with differential signaling is intended to be the largest capacity data readout interface. A bidirectional parallel data port with single-ended signaling is also present, with a capacity of 320 Mb/s. The ALPIDE chip measures 15 mm by 30 mm and includes a matrix of $512 \times 1024$ pixel cells, each one measuring roughly $30 \times 30 \, \mu m^2$. Analog biasing, control, readout and interfacing functionalities are implemented in a peripheral region of $1.2 \times 30 \, mm^2$ (see figure 1).

![Figure 1. Architecture of the ALPIDE chip.](image)

### 3 The new ALICE ITS structure

The new ALICE ITS will have a cylindrical structure organized in seven different layers as described in figure 2 and a coverage described in table 1. The R coordinate is the radial distance from the beam-line, Z is the length along the beam-line centered in the interaction point. The seven ITS layers will be organized in modules or HIC (read-out units) and staves (mechanical units). The three innermost layers will be composed by staves, each one composed by one Inner Barrel Module (IB-HIC). Each IB-HIC will be organized in a row of nine chips. The two outer (middle) layers will be composed by staves built by two rows of seven (four) Outer Barrel Modules (OB-HIC). Each OB-HIC will be composed by two rows of seven chips. In table 2 there is a summary of the elements in each layers. Each module (both inner and outer) will be realized gluing the chips on
expressly designed Flexible Printed Circuit (FPC) containing the data and control buses. Chips pads will be wire bonded to the FPC bus. In the three inner layers, where a high hit density is expected, all the chips in every module will have the same role, while in the four outer layers, where the hit density will be lower, the architecture will be different. For the OB-HIC, only a chip in every row, the master, will collect the data from the other six slaves, sending the output to the external DAQ using a unidirectional High Speed Data (HSD) serial line. The detail of modules interconnection is described in figure 3.

4 The prototype module construction and test

The outer (inner) module construction will be realized in a four step operation: at first fourteen (nine) ALPIDE chips are aligned with a expressly designed automatic machine called Alicia, with a space precision below 5 μm. After that, glue balls are deposited on the corresponding FPC trough a laser drilled mask (see figure 4), and then the FPC is glued on the aligned chips. After the glue
polymerization, the interconnections between the FPC bus and the chip pad is performed with a vertical wire bonding connection. As an additional protection every FPC ring is bonded to the corresponding pad with at least 2 wires (see figure 5). Between May and July 2016 a first serie of few OB-HIC was realized and tested in order to define the module assembling procedure. After
the operation of gluing and bonding the modules were tested using a setup expressly realized. The test setup is based on a high speed communication board called MOSAIC [6] that, using a specific software, acts as DAQ interface with the modules. The produced modules will be tested and validate performing threshold scan and dinamic noise measurements using this setup. Figure 6 shows the result of these measurements realized in one prototype module.

![Figure 6. Prototype Outer Barrel Module threshold and noise measurement.](image)

5 Conclusion

The ALICE ITS upgrade program requires the mass production of ∼ 1700 Outer Barrel modules, spares included. A procedure was defined in order to perform a fast functional characterization of the produced modules. This procedure will be implemented in the production of the next final version of the modules.

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