In-memory Multi-valued Associative Processor

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Abstract—In-memory associative processor architectures are offered as a great candidate to overcome memory-wall bottleneck and to enable vector/parallel arithmetic operations. In this paper, we extend the functionality of the associative processor to multi-valued arithmetic. To allow for in-memory compute implementation of arithmetic or logic functions, we propose a structured methodology enabling the automatic generation of the corresponding look-up tables (LUTs). We propose two approaches to build the LUTs: a first approach that formalizes the intuition behind LUT pass ordering and a more optimized approach that reduces the number of required write cycles. To demonstrate these methodologies, we present a novel ternary associative processor (TAP) architecture that is employed to implement efficient ternary vector in-place addition. A SPICE-MATLAB co-simulator is implemented to test the functionality of the TAP and to evaluate the performance of the proposed AP ternary in-place adder implementations in terms of energy, delay, and area. Results show that compared to the binary AP adder, the ternary AP adder results in a 12.25% and 6.2% reduction in energy and area, respectively. The ternary AP also demonstrates a 52.64% reduction in energy and a delay that is up to 9.5x smaller when compared to a state-of-art ternary carry-lookahead adder.

Index Terms—Associative Processor, Multi-valued Logic, Ternary, Adder, In-memory Computing, Compute-in-Memory.

I. INTRODUCTION

MANY applications in Machine Learning, big data analysis, search engines, and network routing require massive parallelism. As the amount of data to be analyzed continues to grow, power dissipation and data transfer between memory and processing units have limited the scalability of parallel architectures [1].

This has led researchers to consider Associative Processors (APs) as in-memory platforms for carrying-out massively parallel computations inside the memory without the need to move the data [2]. The ability of APs to unify data processing and data storage has drastically decreased compute energy and latency cost. An AP constitutes of an array of Content Addressable Memories (CAMs) which are storage devices that allow concurrent access to all data rows. A CAM searches for a stored word based on an inputted search key. The AP improves its functionality by allowing parallel writing into masked bits of the matching CAM rows [3].

While binary CAMs perform exact-match searches for ‘0’ and ‘1’ bits, a more powerful ternary CAM (TCAM) can search a third “don’t care” value, allowing for very flexible pattern matching between search keys and stored values [3]. Considering its promising applications potential, different implementations for the TCAM have been proposed including SRAM-based TCAM [4], [5]. However, they were not widely adopted due to their low density and nonvolatility [6]. Nowadays, emerging devices such as resistive memories have relaxed these constraints, leading to the revival of the TCAM-based AP approach in the research community [7]. New TCAM implementations based on resistive random access memory (ReRAM) have been proposed [8], [9] to reduce power and improve area density in comparison to the conventional complementary metal-oxide semiconductor (CMOS) solutions.

Memristive-based TCAM (MTCAM) designs have been proposed to build 1D and 2D in-memory computing architectures based on AP [6], [10]. The AP architecture presented in [6] was designed to perform in-memory compute in the context of the binary full adder. It relies on a look-up table (LUT)-based 1-bit addition that employs four compare and write operations applied in parallel to the different rows, resulting in significant runtime savings.

Recently, ternary logic has gained interest among the circuit design community for its ability to increase power efficiency and reduce the complexity of arithmetic circuit designs. However, the implementation of ternary logic circuits requires the use of devices with multiple threshold voltages which is difficult to accomplish with the current CMOS technology with reasonable devices’ area and latency [11], [12]. Therefore, recent studies have shed light on alternative devices for the design of ternary arithmetic circuits such as carbon nanotube field-effect transistors (CNTFETs) [11]–[13] and memristors [14], [15].

In order to carry-out ternary addition, different approaches were adopted in the literature. In [11], authors included a ternary-to-binary decoder stage for the inputs, and the addition was performed using binary logic gates before converting back the outputs to ternary logic. In [12], the authors expressed the arithmetic function using a K-Map, and they used the obtained equations to determine the logic gates needed for the CNTFET-based implementation. In [13], the authors custom-designed the desired arithmetic function and implemented it using ternary logic gates composed of both memristors and CNTFETs.

In this paper, we propose a scalable CAM cell design and methodology for purposes of multi-valued logic AP applications. To enable the implementation of in-memory compute operations, we propose two novel algorithms that guide the automatic generation of the LUT for in-place multi-valued arithmetic or logic functions. The first relies on a depth-first search exploration of the state diagram obtained from the function’s truth table, and the second capitalizes on common outputs to reduce the number of required write cycles. The proposed methodology is universal and can be employed for different logic or arithmetic functions such as NOR, XOR,
AND, multiplication, addition and subtraction. To illustrate, we present a novel implementation of a ternary AP (TAP) architecture based on a novel quaternary CAM (QCAM) design. We demonstrate the proposed design in the context of a LUT-based ternary full adder application. Specifically, our contributions are as follows:

1) We propose a “nTnR” CAM cell for multi-valued AP (MvAP) arithmetic and logic operations. To exemplify our design, we present a TAP architecture using a “3T3R” QCAM cell as a building block.

2) We propose a scalable cycle-free state diagram mapping of the multi-valued arithmetic or logic function’s truth table. The state diagram forms the core data structure to implement the proposed algorithms. These algorithms build on the states’ connectivity along with other relevant attributes to structurally traverse the state diagram for a systematic generation of the LUTs.

3) A first approach that relies on depth-first search (DFS) parsing of the state diagram to determine the order of the passes.

4) A second optimized approach that exploits common write actions to reduce the number of required write cycles. It relies on breadth-first search (BFS) parsing and a grouping heuristic for the different state diagram nodes.

5) We test the algorithms for implementing a LUT-based ternary full adder (TFA) relying on a TAP architecture. We evaluate the energy, delay and area efficiency of the ternary adder implementations using the first and second approaches and compare them against each other as well as to the binary adder and other ternary full adder implementations.

The rest of this paper is organized as follows. Section II proposes the multi-valued AP architecture and discusses the CAM implementation and operation. Then, an illustrative example of ternary AP is discussed in Section III. The extended functional operations from binary AP is proposed utilizing a novel state diagram interpretation in Section IV and an optimized version is introduced in Section V. Experimentation results and analysis are performed on a novel ternary AP full adder implementation in Section VI. Finally, the conclusion of this work is given.

II. PROPOSED MvAP ARCHITECTURE

Traditionally, digital arithmetic computation is performed using two-valued logic: ‘0’ or ‘1’. However, in modern digital design, researchers are increasingly looking into multi-valued logic (MVL) as a way to replace the classical binary characterization of variables. MVL, notably ternary logic, constitutes a promising alternative to the traditional binary logic [16] as it provides multiple advantages such as reduced interconnects, smaller chip area, higher operating speeds and less power consumption [17]. The voltage levels for multi-valued logic of radix-$n$ are $n$ levels spanning from $0$ to $V_{DD}$. Hence, the $i^{th}$ logic value is realized with $i \times V_{DD}/(n-1)$ where $i \in [0, n-1]$. For instance, ternary logic system uses $\{0, 1, 2\}$ logic values with $\{0, V_{DD}/2, V_{DD}\}$ voltage levels, respectively. This representation is referred to as the unbalanced representation unlike the balanced which uses $\{-1, 0, 1\}$ logic values and is realized with $\{-V_{DD}, 0, V_{DD}\}$ voltage levels [18]. In this paper, we focus on the unbalanced ternary logic system.

Table I presents an illustration of the MvAP architecture comprised of a multi-valued CAM (MvCAM) array, a controller, a decoder and a set of Key, Mask and Tag registers. A MvCAM array consists of multiple rows containing MvCAM cells where $n$-valued digits (nits) are stored. The following sections present the proposed implementation of the different components.

A. MvCAM Cell

A compact design of a memristor-based MvCAM cell with $n$ transistors and $n$ memristors (“nTnR”) is presented as a natural extension to the “2T2R” TCAM cell designated for binary AP applications [19]. The proposed design is illustrated in the context of a multi-valued AP in Fig. I. The memristors in the cell function as storage elements whose states determine the stored nit value. The stored value is obtained by setting only one of the memristors to the low resistance state $R_{LRS}$ and maintaining the other $(n-1)$ memristors in the high resistance state $R_{HRS}$, as indicated in Table I. Without loss of generality, the location of the single $R_{LRS}$ among the $(n-1)$ remaining $R_{HRS}$ memristors determines the logic state stored in the cell. Specifically, to store nit value $i$, memristor $M_i$ is the one set to $R_{LRS}$. A “don’t care” state is represented by all memristors set to $R_{HRS}$. To test the functionality of the “nTnR” cell, the matchline (ML) is initially precharged high. The signal vector $(S_{n-1}, S_{n-2}, ..., S_1, S_0)$ illustrated in Fig. I is then sent to check for a specific stored nit value in the cell. When searching for nit value $i$, signal $S_i$ is set to low while the other signals are set to high. The search outcome results in a match only when memristor $M_i$ is in the $R_{LRS}$ and the other memristors are in the $R_{HRS}$. Otherwise, the search outcome results in a mismatch. In the case of a match, the voltage of the ML discharges slowly and is hence preserved high, whereas in the case of a mismatch, the ML discharges quickly to ground.

B. Search Key $n$-ary Decoder

The $n$-ary decoder allows mapping the key-mask pair to the signal vector $(S_{n-1}, S_{n-2}, ..., S_1, S_0)$. Table II presents the truth table for the $n$-ary decoder. The inputs to the decoder are a binary mask and nit-valued key. In the signal outputs of the decoder, the place of the signal set to zero is equal to the search key value. Specifically, to search for logic value $j$, the signal $S_j$ is the one set to zero. It is worth noting that the decoder logic is inverting since the target signal is set to low whereas all other signals are set to high. When the key

| Logic value | $M_{n-1}$ | $M_{n-2}$ | ... | $M_1$ | $M_0$ |
|-------------|-----------|-----------|-----|-------|-------|
| $x$          | $H$       | $H$       | ... | $H$   | $H$   |
| 0           | $H$       | $H$       | ... | $H$   | $L$   |
| 1           | $H$       | $H$       | ... | $L$   | $H$   |
| ...         | ...       | ...       | ... | ...   | ...   |
| $n-2$       | $H$       | $L$       | ... | $H$   | $H$   |
| $n-1$       | $L$       | $H$       | ... | $H$   | $H$   |

TABLE I Mapping between the nit value stored in the MvCAM cell and the corresponding $n$ memristor states.
is masked, i.e., the mask bit is a zero, all decoded signals are set to zero. One simple and generic way to implement such decoder is with simple successive approximation ADC with modified operation. But, in the case of the ternary decoder, it will be shown in the next section that it can be realized with some ternary logic circuits.

**TABLE II**

| Mask | Key | Decoded signals |
|------|-----|-----------------|
| 0    | 0   | 0 0 0 0         |
| n-1  | 1   | 0 1 0 1         |
| n-1  | n-2 | n-1 0 0 0       |
| n-1  | n-1 | 0 0 n-1 0       |

**C. MvCAM Array**

A MvCAM array consists of several MvCAM rows. A MvCAM row contains several “nTnR” cells along with a sensing circuit to distinguish between the full match and the mismatch states. A full match state is obtained when all cells in the row match the searched nits, while a mismatch is obtained when at least one cell in the row does not contain the searched nit. An essential requirement for the array is to concurrently compare the stored data in all rows with an inputted key and mask pair. For purposes of in-memory compute, we overwrite the activated columns of the matched rows with new data. The key determines the nit value to be searched for, while the mask determines the columns of interest to be separately activated during each of the compare and write operations. The nit key and its binary mask are inputted to a decoder that generates the corresponding signal vector \((S_{n-1}, S_{n-2}, ..., S_1, S_0)\), as indicated in Table II.

1) **Compare:** The compare operation includes a precharge and an evaluate phase (see Fig. 2). During precharge, the capacitor is charged high, then a masked key is applied to the array in the evaluate phase. This leads the capacitor of each MvCAM row of cells to discharge through a resistor whose value is equal to the equivalent resistance of the corresponding row. In the case of a full match (fm), the capacitor retains most of its charges due to the presence of only high-resistance paths. In the case of one mismatching cell per row (1mm) or more (2mm, 3mm, etc.), the capacitor discharges quickly through one, two or more low-resistance paths.

2) **Write:** After the compare operation, the sense amplifier connected to the output of the matching circuit senses the voltage across the capacitor and generates correspondences between a row match and logic ‘1’, and a row mismatch and logic ‘0’. Hence, all matching rows are “tagged”, meaning their Tag field is set to logic ‘1’. For example, in Fig. 1 cells in the first row match the masked key and the row is tagged, whereas cells in the last row do not match the masked key. We note that the sensing amplifier is followed by a latch that holds the Tag bit throughout the write action. The write enable signal is asserted to overwrite the new masked columns of the tagged MvCAM rows with new data. Each write action for an “nTnR” cell triggers one memristor set and one memristor reset, except for writing to (from) a “don’t care” state which only requires one reset (set). This is attributed to the fact that each stored nit is associated with a distinct memristor set to \(R_{LRS}\), except for the “don’t care” value in which no memristor is set to \(R_{LRS}\).

Finally, we note that in an optimized architecture, the precharge phase can be performed in parallel with the write operation to reduce the combined compare and write cycle time. As such, a transmission gate powered by the write
enable signal is used to relay to the ML the proper programming voltage to program the memristors, while another pass gate powered by the inverse of the write enable isolates the precharge capacitor from the programming voltage, as illustrated in Fig. 1. The ML programming voltage is set to high during reset, and to low during set. The “nTnR” virtual ground is set to zero during reset, and pulled high during set.

III. ILLUSTRATIVE TAP ARCHITECTURE

In [20], the author analyzed the number system to find the best radix in terms of the economical perspective (i.e., number of computations). The optimal radix is found to be the natural number $e = 2.718$ [21]. So, the ternary logic system is adopted as the best number system since the integer 3 is the nearest to $e$. Herein, we illustrate the MvAP architecture with a ternary AP (TAP) relying on a “3T3R” quaternary CAM (QCAM) cell. The “3T3R” cell is built using three transistors and three memristors and stores the ternary logic values ‘0’, ‘1’ and ‘2’ in addition to a “don’t care” value. Tris are stored in the form of one memristor set to $R_{LRS}$ and two memristors set to $R_{HRS}$. For example, the combination $(M_2, M_1, M_0) = (R_{HRS}, R_{HRS}, R_{LRS})$ indicates a logic ‘0’ since $M_2$ is the memristor which is set to $R_{LRS}$ as shown in Table III. For the same stored value, when the decoded signal triplet sent is $(S_2, S_1, S_0) = (2, 2, 0)$, ML discharges very slowly since only high-resistance paths will connect ML to ground either through $R_{HRS}$ or $R_{off}$, thus resulting in a match. For all other decoded signal combinations, ML discharges quickly to ground through a low-resistance path, thus resulting in a mismatch.

For the TAP, as is the case for the MvAP, the Key register contains the ternary values to be searched for inside the QCAM array, while the Mask register indicates which column or columns of the array are activated during comparison or writing. Upon compare, each key-mask pair generates a decoded signal triplet in which only one of the signals is set to zero, while the others are set to $V_{DD}$, i.e., logic value $n−1 = 2$ for the case of ternary logic. For example, to search for logic ‘0’, the decoded signal triplet is $(S_2, S_1, S_0) = (2, 2, 0)$ as shown in Fig. 3. Equations (1a), (1b) and (1c) represent the corresponding logic functions for the signal values obtained based on the truth table of Fig. 3. The figure also presents the decoder circuit for the case of ternary logic comprising positive ternary inverters (PTIs), negative ternary inverters (NTIs) [22], binary AND, binary OR and binary inverter gates. The truth tables for the ternary inverters are depicted in Table IV [22].

$$S_2 = Mask \cdot PTI(Key)$$

$$S_1 = Mask \cdot NTI(Key) + PTI(Key)$$

$$S_0 = Mask \cdot NTI(Key)$$

For purposes of in-memory compute, matching rows are overwritten by new data. Each write operation of a ternary logic value includes one memristor set and one memristor reset, except for writing to (from) a “don’t care” state which only requires one memristor reset (set).

To implement a specific ternary arithmetic function, we iterate through the LUT entries for 1-trit operation, and the process is repeated to perform multi-trit operations. For each 1-trit operation, the Key register is set to the corresponding LUT input values and applied concurrently to all rows of the ternary inverters (PTIs), negative ternary inverters (NTIs) [22], binary AND, binary OR and binary inverter gates. The truth tables for the ternary inverters are depicted in Table IV [22].

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array in the columns specified by the Mask register. These represent the operand columns. Each key-mask pair is fed to a decoder that generates the signal triplet \((S_2, S_1, S_0)\). After the compare operation, the rows of the QCAM array will generate either a match or a mismatch. Then, the write operation is performed on the matching rows of the array. New data consisting of the LUT output for the corresponding input replaces the stored value in the newly masked columns of the array. Table VII illustrates an example where the state diagram representation to identify the proper processing order of the function’s truth table and, accordingly, generate its LUT. The elements of the state diagram can be best described as follows:

- **Directed edge**: application of the arithmetic function under consideration.
- **State**: stored input to be operated upon.
- **Next state**: corresponding output as per the LUT.
- **noAction state**: state that remains the same upon in-place operation, that is, the LUT input is identical to its corresponding LUT output.

Without loss of generality, Fig. 4 first illustrates the state diagram of the binary adder’s truth table. In this example, the edge corresponds to the binary add operation, the state corresponds to the 1-bit input triplet \((A_i, B_i, C_{in})\) and the next state corresponds to the output triplet \((A_i, S_i, C_{out})\). Finally, the noAction state is the one pointing to itself, indicating that it remains the same upon in-place addition, that is, \((A_i, S_i, C_{out}) = (A_i, B_i, C_{in})\). The binary adder state diagram in Fig. 4 is also labeled with the LUT pass order [6]. An analysis of the pass order shows that they were ordered to avoid erroneously performing multiple consecutive additions on the same entry. This translates in the state diagram to the first pass writing ‘110’ by ‘101’, and the second pass writing ‘100’ by ‘110’. No other pass can overwrite these outputs once their respective inputs are visited. On the other hand, if passes 1 and 2 are exchanged, ‘100’ results in ‘110’ after the first pass, which will be overwritten by ‘101’ after the second pass as indicated by the directional flow of the state diagram. Such a domino effect is not desired. Therefore, it is evident that to construct the LUT for a generic arithmetic function, the order of the passes must be determined through a structured traversal of the directed state diagram.

### IV. AP Operation

A general-purpose AP enables the implementation of arithmetic functions such as addition, subtraction, multiplication and division as well as logical operations by relying on the truth tables of the desired function applied in a specific order. We refer to this as the look-up table based approach. The process is performed digit-wise and is repeated for multi-digit operations. The rows of the MvCAM array store the input vectors. For in-place operation, the output is written back to some or all of the input locations. All rows of the data array are processed in parallel. Each digit-wise operation is comprised of consecutive compare and write steps.

1) **Compare**: For every pass of the LUT, a masked key takes on the input vector values of this pass (see Table VII for the example of binary AP addition [6]). The masked key is applied to all rows of the array and compared against the stored input data.

2) **Write**: A match for a row sets its Tag bit to ‘1’, while a mismatch for a row sets its Tag bit to ‘0’. Tagged rows are overwritten by the corresponding output from the LUT consisting of a new masked key. For the example of the binary AP, the sum bit \(S\) and the carry-out bit \(C_{out}\) are written back to the input locations \(B\) and \(C_{in}\) respectively, keeping \(A\) untouched. The in-place write-back of the output dictates the order of the passes in the LUT. This is required to avoid mistakenly revisiting in future passes rows that have already been overwritten, as will be discussed later.

#### A. Proposed State Diagram for LUT Generation

The proper pass order for a given arithmetic function can be ensured as follows. Consider that \(x\) appears in the truth table of the function as both an input in one entry and an output in some other entry, then the order of processing \(x\) as an input must satisfy one of the two properties below:

1) The pass in which \(x\) appears as an input must be tested before the pass in which \(x\) appears as an output.

2) \(x\) as an input results in ‘No action’, i.e., the output to be overwritten is identical to the stored input. Such an input has no pass number because no action is needed, hence it will never be tested after the pass in which \(x\) appears as an output. This implies that the order of the pass in which \(x\) appears as an output is independent of the pass in which \(x\) appears as an input.

These properties ensure that the resulting passes are visited correctly.

Herein, we propose a directed state diagram representation of the truth table of the arithmetic or logic function to be implemented using AP. Our objective is to rely on this state diagram representation to identify the proper processing order of the function’s truth table and, accordingly, generate its LUT. The elements of the state diagram can be best described as follows:

- **Directed edge**: application of the arithmetic function under consideration.
- **State**: stored input to be operated upon.
- **Next state**: corresponding output as per the LUT.
- **noAction state**: state that remains the same upon in-place operation, that is, the LUT input is identical to its corresponding LUT output.

### Table V

A write example for the ternary “3T3R” cell. ‘X’, ‘R’ and ‘S’ mean no change, reset and set, respectively.

| Current state | \(A\) | \(B\) | \(C_{in}\) |
|---------------|------|------|----------|
| Next state    |      |      |          |
| Next stored   |      |      |          |
| Action        |      |      |          |

### Table VI

Look-up table of the binary AP adder.

| Input | Output | Pass order |
|-------|--------|------------|
| \(A\) | \(B\) | \(C\) |          |
| \(A\) | \(B\) | \(C\) |          |
| \(A\) | \(B\) | \(C\) |          |

| Input | Output | Pass order |
|-------|--------|------------|
| \(A\) | \(B\) | \(C\) |          |
| \(A\) | \(B\) | \(C\) |          |
| \(A\) | \(B\) | \(C\) |          |
B. Automated LUT Generation

Herein, we build upon our state diagram interpretation of the truth table to guide the automatic development of a general-purpose LUT. As we note from Fig. 4, the state diagram comprises of a collection of trees whose roots are noAction states. We note that the input-output pairs are connected through backward edges propagating to the roots. Our objective is to identify the proper order of passes for in-place operation so that no pass overwrites the outcome of earlier ones. This can be guaranteed if and only if the following holds for the state diagram:

1) The state diagram is a uni-directional graph with no cycles, i.e., no forward edges.
2) If the state diagram has cycles, then we should be able to break these cycles by redirecting forward edges backwards. If in the original state diagram input vector $x = (x_1, x_2)$ has its output $y = (x_1, y_2)$ creating a forward edge, we search for an alternate output $y' = (y_1, y_2)$ that forms a backward edge and breaks the cycle. $y'$ is a valid output so long $y_2$ remains unchanged since $y_2$ represents the output digit to be overwritten as per the LUT, while $y_1$ is a dummy extra written digit. Therefore, we need to invoke a larger vector write post the compare operation. This will be illustrated in the following example.

For example, we implement the state diagram for the LUT-based ternary full adder (TFA) in the context of TAP. Fig. 5 presents the state diagram of the TFA’s truth table. We perform in-place ternary addition with inputs $(A, B, C_{in})$. The outputs $(S, C_{out})$ overwrite $(B, C_{in})$, while $A$ is kept untouched. In the state diagram, if the input triplet $(A, B, C_{in})$ whose output $(A, S, C_{out})$ represents a forward edge forming a cycle, we search for an alternate output $(y_1, S, C_{out})$ that forms a backward edge and breaks the cycle. We then invoke a 3-trit write post the compare operation instead of the standard 2-trit write. Specifically, as illustrated by the dashed red edge in Fig. 5, a direct implementation of the in-place ternary addition state diagram results in one cycle: state ‘101’ leads to ‘120’ and state ‘120’ leads back to ‘101’. To resolve this problem, we overwrite the A trit value to a ‘0’ for the input ‘101’. Hence, input ‘101’ now results in ‘020’ as an output (see green edge in Fig. 5 and input ‘120’ results in ‘101’ as an output. This incurs a minor cost consisting of an extra trit to be written for one of the passes. However, it eliminates the cycle and enables a smooth implementation of the LUT-based approach for the TFA.

With a cycle-free state diagram, i.e., a backward propagation based input-output relation (left to right), we devise that the passes should progress to visit the trees of the state machine from right to left in a depth-first search (DFS) approach, starting from the root of each tree. Since the roots are noAction nodes, we do not assign pass numbers to them and, hence, do not include them in the ordering of the passes. Algorithm 1 presented herein details the traversal scheme of the state diagram which ultimately determines the proper order of the passes for in-place operation. Table VII presents the resulting LUT for the TFA after applying Algorithm 1.

Algorithm 1 Ordering of the passes for the LUT-based ternary full adder following the non-blocked approach.

\begin{algorithm}
  1: Global pass number $p = 0$
  2: Global LUT length $L = length(LUT)$
  3: for all $T_i$ do
  4:    buildLUT($T_i$, root)
  5:  end for
  6: return

procedure buildLUT(state $j$)
  1: if $j$.noAction $== 0$ then
  2:      $p + +$
  3:      $j$.passNum $= p$
  4:  end if
  5: for all $v \in j$.child do
  6:    buildLUT($v$)
  7:  end for
  8: return
\end{algorithm}

V. OPTIMIZED AP OPERATION

In the first approach, hereafter referred to as the non-blocked approach, similar to traditional AP operation, each
TABLE VII
Look-up table of the LUT-based TFA.

| Input | Output | Pass order |
|-------|--------|------------|
| A B C | A B C  |            |
| 0 0 0 | 0 0 0  | No action  |
| 0 0 1 | 0 1 0  | 1          |
| 0 1 0 | 0 1 0  | 21         |
| 0 1 1 | 0 1 0  | 10         |
| 0 1 2 | 0 0 1  | 2          |
| 0 2 0 | 0 2 0  | No action  |
| 0 2 1 | 0 0 1  | 3          |
| 0 2 2 | 0 1 1  | 11         |
| 1 0 0 | 1 0 0  | 15         |
| 1 0 1 | 0 2 0  | 12         |
| 1 0 2 | 1 0 1  | 16         |
| 1 1 0 | 1 2 0  | 14         |
| 1 1 1 | 1 0 1  | 17         |
| 1 1 2 | 1 1 1  | 18         |
| 1 2 0 | 1 0 1  | 13         |
| 1 2 1 | 1 1 1  | 19         |
| 1 2 2 | 1 2 1  | 20         |
| 2 0 0 | 2 0 0  | 8          |
| 2 0 1 | 2 0 1  | No action  |
| 2 0 2 | 2 1 1  | 5          |
| 2 1 0 | 2 0 1  | 9          |
| 2 1 1 | 2 1 1  | No action  |
| 2 1 2 | 2 1 1  | 4          |
| 2 2 0 | 2 1 1  | 7          |
| 2 2 1 | 2 2 1  | No action  |
| 2 2 2 | 2 0 2  | 6          |

TABLE VIII
State attributes definitions for the blocked and non-blocked algorithms.

| Attribute | Definition |
|-----------|------------|
| noAction  | Determines the type of the state: 1 for a No Action state, 0 for an Action state. |
| grpNum    | Specific write group of the state |
| level     | State level as indicated in Fig. 5 |
| outVal    | "n-ary"-to-decimal conversion of the state vector |
| writeDim  | Write-back dimension for the output vector of the state |
| parent    | Pointer to the parent of the state which is accessible from the state through a backward edge |
| child     | Pointer to the child of the state which is accessible from the state through a forward edge |
| passNum   | Pass order assigned to the state in the LUT |

To implement the algorithm for the automatic generation of the LUT using the blocked approach, we consider that each node in the state diagram represents an input or output vector depending on whether the node is subject to or the result of an add operation, respectively. Each node is also associated with a set of attributes detailed in Table VIII. One of the attributes is writeDim representing the dimension of the output vector to be written when the node is regarded as an input state. Another attribute is the outVal array whose entries represent the "n-ary"-to-decimal value of the node’s write action when it is regarded as an output state. The need for the outVal array of entries is explained as follows using the TFA as an example. For the TFA, when the node is the result of a 2-trit write-back, outVal(writeDim = 2) stores the ternary-to-decimal conversion of the written BC value. In the event of breaking cycles, we may add an extra dummy dimension and invoke a 3-trit write-back. The node that is regarded as the input of the operation will have writeDim = 3 and the node that is regarded as the output will have outVal(writeDim = 3) store the corresponding equivalent decimal written ABC value. Note that these values will be adjusted as explained later to avoid overlap between the different decimal value conversions. For example, ABC = 000 will be mapped to a different number than BC = 00 as indicated in line 5 of Algorithm 2. This will help in properly differentiating grouping of nodes that have the same parent but different write action dimensions. Thus, nodes at the same level having the same writeDim and parent outVal share the same write action. As such, for a specific node, we rely on its parent outVal(writeDim) value for the grouping and use it as a key component of the dynamic grpLvl table that we rely on to guide the BFS-like traversal algorithm. The table stores the number of nodes belonging to the same group, i.e., having a similar write action, in each level of the tree. The algorithm performs pass ordering and grouping by updating the grpLvl table after each determined block to reflect updates to the state diagram. The algorithm proceeds as follows.

1) grpLvl initialization: To populate the initial grpLvl table, we apply Algorithm 2. Table IX represents the initial grpLvl table for the TFA state diagram corresponding to Fig. 5. For each state which is an Action state, we find l, the level of the node as indicated by Fig. 5, and g, the outVal(writeDim) value of the node’s parent. For example, the group number g for node ‘011’ in the TFA state diagram of Fig. 5 is outVal(3) of its parent node ‘020’. This corresponds to the adjusted value $6 + \sum_{i=0}^{2} 3^i = 19$, where ‘6’ is the ternary-to-decimal conversion of the vector ‘020’. Whereas the group number g for node ‘011’ is outVal(2) of its parent node ‘020’, corresponding to the adjusted value $6 + \sum_{i=0}^{1} 3^i = 10$, where ‘6’ is the ternary-to-decimal conversion of the vector ‘20’. Accordingly, for each Action node in level l, an initial group number grpNum = g is assigned to the node, and the entry corresponding to group g and level l in the grpLvl
table is incremented. Entries in the \textit{grpLvl} table thus reflect the number of nodes that share the same level and write action. For example, 5 nodes in Level 2 share the same write action \( BC = 013 = 1_{10} \), having an adjusted value of \( 1 + \sum_{i=0}^{1} 3^i = 5 \). Thus, \( \text{grpLvl}[2][g = 5] = 5 \) as shown in Table \ref{table:grplvl_initial}

**Algorithm 2** Initializing the \textit{grpLvl} table.

Global pass number \( p = 0 \)

1. \( S \) is the set of all states \( \forall T_i \)
2. \( \text{for all states } j \in S \text{ do} \)
3. \( \text{if } j.\text{noAction} == 0 \text{ then} \)
4. \( \text{Level } l = j.\text{level} \)
5. \( \text{Group number } g = j.\text{parent.outVal}(\text{writeDim}) + \sum_{i=0}^{\text{writeDim}-1} (n^i) \)
6. \( j.\text{grpNum} = g \)
7. \( \text{grpLvl}[l][g] ++ \)
8. \text{end if}
9. \text{end for}
10. \( G = \text{max}(g) \)
11. \( L = \text{max}(l) \)

\# Use \textit{grpLvl} table to build LUT for Action states

12. \text{BUILDLUTBLOCKED}(S, \text{grpLvl}, G, L)
13. \text{return}

\(2) \text{ Selecting the next block/group:} \) At each iteration, our objective is to find the next target block/group \( g_{tgt} \) for an adequate ordering of the passes in the LUT. We keep in mind the following. Nodes that reside in Level 1 must be processed first from a pass ordering perspective (these qualify as nodes whose parents have already been processed or whose parents are \text{noAction} states). For purposes of grouping, we must therefore look for groups that are fully or maximally residing in Level 1. In fact, we consider the following two cases as indicated in Algorithm \ref{algorithm:grplvl_initial}

- In an ideal scenario, there exists a group that has nodes belonging to the top level (Level 1) and no nodes in lower levels. This group would qualify as the next target group \( g_{tgt} \).
- Another possible scenario is that no group has all its nodes in the top level. In this case, we choose the group that has a maximum number of nodes in the top level as \( g_{tgt} \). However, we need to break this group since we can only process states belonging to the top level. We split \( g_{tgt} \) by creating a new group for the remaining states present in lower levels. In this way, the total number of groups \( G \) is incremented, and \( g_{tgt} \) will only contain nodes that are in the top level.

To illustrate, initial \textit{grpLvl} values shown in Table \ref{table:grplvl_initial} indicate that Group 19, should be processed first. It is the only group that has entries in the top level and no entries in lower levels. Supplementary Tables 1, 2 and 3 present \textit{grpLvl} tables for the following three iterations, and at each iteration, we identify all possible new \( g_{tgt} \) groups. We continue until all the entries in the \textit{grpLvl} table at the top level become zero.

**Algorithm 3** Finding the next block/group \( g_{tgt} \).

\textbf{procedure BUILDLUTBLOCKED}(\( S, \text{grpLvl}, G, L \))

1. \( \text{topLevel} = 1 \)
2. \text{while} \( \text{grpLvl}[\text{topLevel}][\cdot] \neq \text{zeros}(1,G) \) \text{do}
3. \( \text{found} = -1 \)
4. \text{for } \( g = 0 \rightarrow G \) \text{do}
5. \( \text{cond}_1 = (\text{grpLvl}[\text{topLevel}][g] > 0) \)
6. \( \text{cond}_2 = (\sum_{l=2}^{\text{grpLvl}}[l][g] == 0) \)
7. \text{if} \( \text{cond}_1 \text{ and } \text{cond}_2 \text{ then} \)
8. \( g_{tgt} = g \)
9. \text{UPDATELUT}(g_{tgt})
10. \( \text{found} = 1 \)
11. \text{end if}
12. \text{end for}
13. \text{if} \( \text{found} == -1 \) \text{then}
14. \( [g_{tgt}, \text{max}_{\text{grpLvl}}] = \text{max}(\text{grpLvl}[\text{topLevel}][\cdot]) \)
15. \# Create new group for remaining states of \( g_{tgt} \) in lower levels
16. \( G++ \)
17. \text{for } \( l = 2 \rightarrow L \) \text{do}
18. \( \text{grpLvl}[l][G] = \text{grpLvl}[l][g_{tgt}] \)
19. \( \text{grpLvl}[l][g_{tgt}] = 0 \)
20. \text{end for}
21. \text{for all states } j \text{ do}
22. \text{if} \( (j.\text{grpNum} == g_{tgt}) \text{ and } (j.\text{level} > 1) \text{ then} \)
23. \( j.\text{grpNum} = G \)
24. \text{end if}
25. \text{end for}
26. \text{UPDATELUT}(g_{tgt})
27. \text{end while}
28. \text{return}

\(3) \text{ Updating grplvl and assigning pass numbers:} \) We rely on Algorithm \ref{algorithm:grplvl_initial} to order the passes and build the LUT. In each iteration, once the next \( g_{tgt} \) is identified, we extract the nodes with \( \text{grpNum} = g_{tgt} \) from the state diagram and assign them as the next block to be processed in the LUT. We label them accordingly with their corresponding pass number. Note that within the \( g_{tgt} \) group, passes can be numbered arbitrarily. For example, in Group 2 shown in Table \ref{table:grplvl_initial} triplet ‘102’ order.

\begin{table}[h]
\centering
\caption{GrpLvl table initial values corresponding to Fig. \ref{fig:grplibl_initial}. It indicates that Group 19 should be processed first since it is the only group that has no entries beyond Level 1. Note that for the TFA example, writeDim = 1 does not exist, and thus by default, no nodes can have grpNum = \{1, 2, 3\}.}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline
\textit{grpNum} & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 & 16 & 17 & 18 & 19 \\
\hline
\textit{level} & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 & 16 & 17 & 18 & 19 \\
\hline
\text{parent.outVal}(1) & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 2 & 0 & 2 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \\
\hline
\text{parent.outVal}(2) & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 2 & 0 & 2 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
\hline
\sum_{i=0}^{\text{writeDim}-1} 3^i & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 2 & 0 & 2 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
\hline
\text{parent.outVal}(3) & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 2 & 0 & 2 & 1 & 0 & 0 & 0 & 0 & 0 \\
\hline
\sum_{i=0}^{\text{writeDim}-1} 3^i & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 2 & 0 & 2 & 1 & 0 & 0 & 0 & 0 \\
\hline
\end{tabular}
\end{table}
TABLE X
LOOK-UP TABLE OF THE LUT-BASED TFA FOLLOWING THE BLOCKED APPROACH.

| Input | Output | Pass order | Group number | Write action |
|-------|--------|------------|--------------|--------------|
| A | B | C | A | B | C |               |               |               |
| 1 | 0 | 1 | 0 | 2 | 0 | 1 | 1 | W020 |
| 1 | 0 | 2 | 1 | 0 | 1 | 2 | No action |   |
| 1 | 1 | 1 | 1 | 0 | 1 | 3 | No action |   |
| 1 | 2 | 0 | 1 | 0 | 1 | 4 | No action |   |
| 2 | 1 | 0 | 2 | 0 | 1 | 5 | No action |   |
| 1 | 2 | 2 | 1 | 1 | 1 | 6 | No action |   |
| 1 | 2 | 1 | 1 | 1 | 2 | 7 | No action |   |
| 2 | 0 | 2 | 2 | 1 | 1 | 8 | No action |   |
| 2 | 2 | 0 | 2 | 2 | 1 | 9 | No action |   |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | No action |   |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | No action |   |
| 0 | 2 | 0 | 0 | 2 | 0 | 2 | No action |   |
| 2 | 0 | 0 | 0 | 2 | 0 | 3 | No action |   |
| 2 | 1 | 2 | 2 | 1 | 4 | 14 | No action |   |
| 2 | 2 | 2 | 2 | 2 | 1 | 15 | No action |   |
| 0 | 0 | 1 | 0 | 0 | 1 | 16 | No action |   |
| 1 | 0 | 0 | 1 | 1 | 0 | 17 | No action |   |
| 2 | 2 | 2 | 2 | 0 | 2 | 18 | No action |   |
| 0 | 1 | 2 | 0 | 0 | 1 | 19 | No action |   |
| 0 | 2 | 1 | 0 | 0 | 1 | 20 | No action |   |
| 0 | 2 | 1 | 0 | 1 | 2 | 21 | No action |   |

Algorithm 4 Updating the grpLvl table and ordering the passes of the LUT.

procedure UPDATELUT(gtgt)
1: topLevel = 1
2: for all states j do
3: if j.grpNum == gtgt then
4: p++
5: j.passNum = p
6: end if
7: for all v ∈ tree whose root is j do
8: grpLvl[v.level - 1][v.grpNum]++
9: grpLvl[v.level][v.grpNum]--
10: v.level --
11: end for
12: end for
13: grpLvl[topLevel][gtgt] = 0
14: return

Circuits to Enable the Blocked Approach: We note that there is a minimal cost overhead for blocking to delay the write action until the end of the block. Our proposed solution is to add to each row a D flip-flop clocked by the Tag bit. Prior to processing a block, write enable signals are discharged. Hence, as we traverse the LUT to process the passes of the block, a match for a row will have its Tag bit toggle from ‘0’ to ‘1’, setting the write enable signal at the output of the flip-flop to a ‘1’. At the end of each block, the rows for which the flip-flop outputs are ‘1’ are overwritten. This ensures that all rows that have matches within the block will be overwritten together by the same output. The flip-flop is reset after every block. Timewise, the flip-flop’s toggling time cost can be hidden, whereas storage wise, one extra flip-flop per row is needed.

VI. RESULTS AND ANALYSIS

In this section, we study the proposed ternary adder implementations (non-blocked and blocked) in terms of energy, delay and area, and we compare them against the binary AP adder and other ternary adder implementations. First, we study the characteristics of the “3T3R” cell. For our experimental results, we rely on 45nm predictive technology model [23] for our simulations. The transistor threshold voltage is $V_t = 0.4V$, and $V_{DD} = 0.8V$.

A. Design Space Exploration: QCAM Cell Dynamic Range and Energy Analysis

In our ternary AP adder design, a 1-trit addition involves the comparison of the key-mask pair with three stored triplets of memristor states ($M_1, M_2, M_3$), where each triplet corresponds to one of the trits $A, B$ and $C_m$. The outcome of the comparison can result in a: full match (fm), one mismatch (1mm), two mismatches (2mm) or three mismatches (3mm).

For purposes of the analysis of the “3T3R” cell, we define the dynamic range (DR) as the maximum voltage difference between the fm and the closest mismatch case which is 1mm [24], [25], measured after 1ns of evaluation time of the $(S_h, S_x, S_L)$ signal triplet as indicated below.

$$DR = V_{fm} - V_{1mm}$$  \hspace{1cm} (2)

where, $V_{fm}$ and $V_{1mm}$ represent the ML voltages for the fm and 1mm states, respectively. Typically, for accurate sensing of the comparison outcome, we aim for a high dynamic range. However, a high DR comes at the expense of increased compare energy consumption. To further assess this, we define for purposes of the add operation the compare energies $E_{fm}$, $E_{1mm}$, $E_{2mm}$, $E_{3mm}$ corresponding to the fm, 1mm, 2mm and 3mm states, respectively. We rely on HSPICE simulations to study the dynamic range and compare energies for the “3T3R” cell in the context of the LUT-based ternary adder. We assess these metrics for the following design space parameter combinations. Without loss of generality, we set the total number of cells per row $N = 41$ to enable 20-trit addition, where each of the $A$ and $B$ vectors have 20 cells per vector, and we have one extra cell for the $C_m$ trit. We also sweep $R_L \in \{20, 30, 50, 100\} \Omega$, and set $R_H = \alpha \ast R_L$ where $\alpha \in \{10, 20, 30, 40, 50\}$. A capacitive load $C_L = 100fF$ is used for the comparator to properly latch $V_{ML}$ and distinguish between the fm and 1mm states due to fast discharge. Fig. [6] presents the corresponding dynamic range values for the

Table X: Look-Up Table of the LUT-based TFA following the blocked approach.
"3T3R" cell for 20-trit addition as a function of $R_L$ and $\alpha$. The maximum, thus, best dynamic range is observed for lowest $R_L$ values. For example, $DR \approx 240mV$ when $R_L = 20K\Omega$ and $\alpha = 50$. The compare energy for the "3T3R" cell for 20-trit addition as a function of $R_L$ and $\alpha$ is plotted in Fig. 7. For the same $R_L = 20K\Omega$, the lowest energy is obtained at the highest $\alpha = 50$. In fact, for $R_L = 20K\Omega$, when $\alpha$ increases from 10 to 50, $E_{fm}$ drops by 71.61%, $E_{1nm}$ drops by 22.27%, $E_{2nm}$ drops by 9.45% and $E_{3nm}$ drops by 4.37%. As such, for the remaining experiments, we adopt the memristor values ($R_L, R_H = (20K\Omega, 1M\Omega)$ which provides the best dynamic range with the corresponding lowest compare energy consumption for this $R_L$ value.

B. Evaluation Against Binary System

As previously mentioned, the optimal number system is found to be $e$ which lies in between binary and ternary system. Hence, we evaluate the TAP performance against the Binary AP. Herein, we compare the ternary LUT-based addition to the respective binary LUT-based addition in terms of energy and area. For this, we employ the non-blocked approach since these metrics are common to both the blocked and non-blocked approaches. The following section analyzes the delay of the different proposed approaches.

Thus, in our experiments, we study the average energy for $p$-trit addition in comparison to the equivalent $q$-bit addition for different $p$ and $q$ values, where $p \in \{5t, 10t, 20t, 32t, 40t, 80t\}$ and $q \in \{8b, 16b, 32b, 51b, 64b, 128b\}$, respectively. For example, we compare $p = 20t$ representing 20-trit addition to the equivalent $q = 32b$ representing 32-bit addition.

We rely on HSPICE to characterize the compare energy for 1-bit (1-trit) addition in the context of LUT-based binary (ternary) adder for the 2T2R [19] (3T3R) cell with $R_L = 20K\Omega$ and $R_H = 1M\Omega$. We adopt $C_L = 100fF$ to correctly latch $V_{ML}$, and the number of cells per row is equal to $2q + 1$ ($2p + 1$). We set the evaluate time to $1ns$ for which we observe a $DR$ approximately equal to 200mV for the different simulations, allowing for good differentiation between the match and mismatch cases. The precharge time is also set to $1ns$.

We developed a functional simulator using MATLAB to obtain the average for the compare energy and write energy for both the ternary and binary LUT addition, relying on a total of 10,000 $p$-trit and $q$-bit additions. The functional simulator estimates the number of set/reset operations taking into consideration whether we are writing only one, two, or all three ($A, S, C_{out}$) cells based on the different LUTs and number of sets/resets required per cell (see Table XI). We assume the memristor write energy per set or reset operation to be on average around 1nJ as was stated in [26] for different programming and initial memristor conditions. The functional simulator also utilizes the 1-bit and 1-trit compare energy values obtained using HSPICE to estimate the $q$-bit ($p$-trit) compare energy based on the different match/mismatch combinations. For purposes of area comparison, we rely on the number of cells per row for the $q$-bit ($p$-trit) addition assuming that the “2T2R” cell area is 0.67x the area of one “3T3R” cell. Results are indicated in Table XI. Overall, compared to the LUT-based binary addition, the LUT-based ternary addition results in about 12.6% reduction in the total number of sets/resets needed, 12.25% reduction in total energy and 6.2% area reduction.

C. Performance Comparison to Other Ternary Adder Designs

In this section, we compare the proposed ternary LUT-adder approaches against other ternary adder implementations. Particularly, we compare the total energy consumed by the proposed ternary AP (TAP) adder implementations against hybrid CNTFET and memristor-based implementations of the carry-ripple adder (CRA), carry-skip adder (CSA) and carry-lookahead adder (CLA) [15]. We also conduct a delay analysis for the TAP blocked and non-blocked approaches in comparison to the LUT-based binary adder and the CLA.

Our comparison is based on extrapolating the authors’ 4-bit adder’s power and delay simulations to reflect energy consumption and delay values for 20-trit addition at $V_{DD} = 0.8V$. For our adder implementation, the consumed energy does not differ between the non-blocked and blocked approaches. We thus rely on Table XI to obtain the total energy for our TAP implementation. Fig. 8 presents the energy for the different ternary adder implementations as function of the number of rows (#Rows, i.e., number of parallel additions). TAP consumes about 52.64% less energy than the CLA, which in turn demonstrated lower energy consumption compared to the CSA and CRA. We note that for all adder implementations, the energy grows linearly with the number of add operations.

We define the delay as the number of clock cycles needed to concurrently compare and write multiple rows within the data array. While in the non-blocked approach every compare is followed by a write action, the blocked approach delays the write action until the end of the sequence of block compares, thus improving the overall delay of the adder. Note that,
irrespective of whether a match occurs or not, we account for the write cycle. Fig. 9 shows the delay for the LUT ternary adder using the non-blocked and blocked approaches, along with the CLA and the binary AP adder as a function of the number of rows (#Rows). Compared to the CLA, the non-blocked (blocked) TAP demonstrates lower runtime starting when the number of p-trit add operations (i.e., #Rows) exceeds 64 (32). At 512 rows, the non-blocked and blocked TAP approaches demonstrate a 6.8x and 9.5x reduction in delay compared to the CLA, respectively. The blocked approach further shows a 1.4x reduction in delay compared to the non-blocked approach for all #Rows. These results assume a traditional precharge cycle similar to Fig. 2.

In an optimized implementation where the precharge is embedded within the write cycle, the TAP adder is 9x smaller than the CLA and the blocked TAP approach introduces around 1.2x improvement compared to the non-blocked TAP approach. This is due to the need for precharge post evaluate for the compare cycles that are not followed by a write action.

Finally, it is worth noting that the binary AP adder demonstrates the lowest delay at 2.3x savings compared to the ternary TAP in lieu of increased area and energy.

### VII. Conclusion

In this paper, we proposed a novel multi-valued associative processor with illustrative example on ternary-radix. In addition, we proposed efficient LUT-based ternary full adder methodology in the context of AP. The AP implementation relies on a novel quaternary CAM “3T3R” cell. Novel algorithms are used to build the ternary adder LUT following two approaches: a first non-blocked approach that formalizes the intuition behind LUT pass ordering and a second blocked approach that targets latency reduction in terms of capitalizing on common write action cycles. The efficiency of the proposed approaches is proven by a formal simulator built using MATLAB in which we incorporate HSPICE simulations. Results show that the ternary AP has lower energy and area compared to the binary AP, albeit higher delay. Moreover, compared to other hybrid CNTFET and memristor implementations of the ternary adder, the proposed ternary AP adder has lower energy and delay. Furthermore, the results demonstrate performance efficiency for the blocked AP approach. In order to improve the performance of MvAP, multi-valued CAM cell would need to be optimized with less number devices and with more efficient write techniques.

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