ExPAN(N)D: Exploring Posits for Efficient Artificial Neural Network Design in FPGA-based Systems

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Abstract—The recent advances in machine learning, in general, and Artificial Neural Networks (ANN), in particular, have made smart embedded systems an attractive option for a larger number of application areas. However, the high computational complexity, memory footprints, and energy requirements of machine learning models hinder their deployment on resource-constrained embedded systems.

Most state-of-the-art works have considered this problem by proposing various low bit-width data representation schemes, optimized arithmetic operators’ implementations, and different complexity reduction techniques such as network pruning. To further elevate the implementation gains offered by these individual techniques, there is a need to cross-examine and combine these techniques’ unique features. This paper presents ExPAN(N)D, a framework to analyze and ingather the efficacy of the Posit number representation scheme and the efficiency of fixed-point arithmetic implementations for ANNs. The Posit scheme offers a better dynamic range and higher precision for various applications than IEEE 754 single-precision floating-point format. However, due to the dynamic nature of the various fields of the Posit scheme, the corresponding arithmetic circuits have higher critical path delay and resource requirements than the single-precision-based arithmetic units. Towards this end, we propose a novel Posit to fixed-point converter for enabling high-performance and energy-efficient hardware implementations for ANNs with minimal drop in the output accuracy. We also propose a modified Posit-based representation to store the trained parameters of a network. Compared to an 8-bit fixed-point-based inference accelerator, our proposed implementation offers \( \approx 46\% \) and \( \approx 18\% \) reductions in the storage requirements of the parameters and energy consumption of the MAC units, respectively.

Index Terms—Computer Arithmetic, Deep Neural Networks, Energy Efficient Computing, Posits, FPGA, High-level Synthesis

1 INTRODUCTION

MACHINE learning algorithms have become an essential factor in various modern applications, such as scene perception and image classification [1]–[3]. Over the past few years, these algorithms have mainly relied on the performance of modern computing systems to support the increasing complexity of the algorithms. For example, the massively parallel architectures, such as Graphics Processing Units (GPUs), and cloud-based computing have been traditionally used to train these algorithms. However, to utilize these trained machine learning models on resource-constrained embedded systems, the computational complexity and storage requirements of these algorithms must be reduced.

Many recent works have considered this problem to define various optimization techniques to reduce the complexity of machine learning models, such as Artificial Neural Networks (ANN). For example, the techniques used in [4] and [6] have employed the sparsity of Deep Neural Networks (DNN) to reduce the total number of trained parameters. The works in [7], [8] and [9] have explored other number representation techniques, such as \( \text{bf}loa16, \ Posit \) and \( \text{Fixed Point (FxP)} \) to overcome the storage requirements of single-precision \( \text{IEEE-754 Floating Point (FP32)} \). Depending on the configuration used, each of these number representation techniques provides different dynamic range to represent the parameters (weights and biases) of a network. For example, Fig. 1(a) shows the FP32-based distribution of the pre-trained weights of the Conv2_1 layer of VGG16 DNN. The pre-trained weights have a dynamic range between −0.3 to +0.3, with most of the weights clustered around ‘0’. To reduce the memory footprint of the weights and associated computational complexity, Fig. 1(b)

![Fig. 1: Distribution of pre-trained weights of Conv2_1 layer of VGG16 DNN. (a) Single-precision floating-point, (b) 8-bit linear fixed-point quantization: average absolute relative quantization-induced error=0.295 (c) Posit (8, 2)-based quantization: average absolute relative quantization-induced error=0.052.](image)

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The rest of the paper is organized as follows. In Section 2, we provide the relevant background and brief overview of related work. The system model used for the evaluation of the proposed methods is presented in Section 3. In Section 4, we explain the proposed methodology for exploring the use of Posit representation for ANNs, along with the proposed hardware designs. In Section 5, we discuss the results from the experimental evaluation of the different components of the proposed methodology. Finally, we conclude the article in Section 6 with a summary and a discussion on the scope for related future research.
2 BACKGROUND AND RELATED WORKS

2.1 Posit Number System

The IEEE 754-2008 compliant floating-point (floats)-based arithmetic has become ubiquitous in modern-day computing and is deeply embedded in compilers and low-level software routines. However, the floats have several limitations, such as non-identical results across systems, redundant/wasted bit patterns, and a limited dynamic range. The Posit number scheme overcomes these limitations by offering a better dynamic range and portability across various computing platforms. Fig. 3 shows the various fields (sign, regime, exponent, and fraction) of the Posit number scheme. A Posit configuration is characterized by its total bit length ($N$) and the number of bits reserved for exponent ($ES$). Utilizing the four fields of the Posit scheme, Eq. 1 defines the computation of a Posit value. The regime field, in Fig. 3, is utilized to compute the value of $k$ in Eq. 1. The regime field is terminated when an inverted bit ($\bar{r}$) is encountered, and the associated value of $k$ is determined by the number of identical bits ($m$); if the identical bits are a string of 0s, then $k = -m$; if they are a string of 1s, then $k = m - 1$. Next, the exponent ($e$) and fraction values ($f$) are determined using the remaining bits. The utilization of regime field provides a better dynamic range to Posit number scheme. For example, the authors in [10] have reported that for some applications, the $n$-bit floats can be replaced by $n$-bit Posit-based numbers (where $m < n$) to achieve comparable output accuracy.

\[
\text{Posit value} = s \times (2^{E_S})^k \times 2^e \times 1.f
\] (1)

Compared to the floats and fixed-point number representation schemes, Posit requires more computational resources. In the following section, we summarize the state-of-the-art works related to hardware implementation of Posit-based arithmetic circuits.

2.2 Posit Arithmetic Hardware

The major challenges faced while developing an efficient hardware implementation for Posit arithmetic involve-(1) handling run-time length variation in individual Posit fields, (2) extraction of Posit components to facilitate further manipulation and, (3) implementation of rounding algorithms as proposed in the Posit standard. TABLE I presents an overview of the state-of-the-art work related to Posit-based arithmetic and highlights our proposed framework’s key focus. These works are summarized below.

The authors in [10] tackle run-time varying field length by developing hardware arithmetic architectures for conversion from Posit to floating point and vice-versa. The work in [13] proposes a tool to generate pipelined Posit operators to be used as a drop-in replacement in processing units. In [11], authors present the architecture of a parameterized Posit arithmetic unit to generate posit adders and multipliers of any bit-width. Similarly, PACoGen [12] employs a three-stage process which involves Posit data extraction, core arithmetic processing and Posit construction to perform parameterized Posit arithmetic including multiplication and division. It proposes improvements in Posit data extraction methodology and a pipelined architecture for Posit ($N=32$, $ES=6$). Posit arithmetic has also been integrated into Clarinet [21] which is a RISC-V ISA based processor that supports the use of a Posit arithmetic core. However, the RISC-V implementations are not capable of handling large-scale applications.

2.3 Arithmetic Hardware for ANN Inference

A plethora of recent works have considered different quantization schemes to reduce the memory footprints and computational complexity of [DNNs] for resource-constrained embedded systems and edge devices for IoT. These techniques can be categorized into (a) in-training quantization, and (b) post-training quantization schemes. For example, the techniques proposed in [23]-[25] have considered various fixed-point schemes for in-training quantization. The in-training quantization schemes can overcome most of the quantization-induced errors. However, these techniques cannot be utilized for the quantization of the parameters of pre-trained DNNs. For example, for the quantization of pre-trained DNNs, [9], [26]-[28] have proposed different schemes. The techniques presented in [27], [28] have focused on the utilization of logarithmic data representations to avoid the computationally expensive multiplication operations. However, some recent works, such as [29]-[31] have utilized fixed-point quantization schemes to employ the well-explored high-performance and energy-efficient approximate adders and multipliers. The utilization of approximate arithmetic units [32]-[35] provides another degree of freedom for achieving the accuracy, performance, and energy constraints of DNNs for IoT. For example, the authors of [29] have utilized the library of approximate multipliers [33] to provide approximate accelerators for reduced-precision DNNs.

Some recent works have also explored the utilization of Posit numbers for training and inference phases of [ANN]. For example, the work in [16] has used ARM scalable vector extension SIMD engine to present vectorized extensions for the cppPosit C++ posit arithmetic library. The authors of [14] have proposed an exact multiply and accumulate (EMAC) for implementing the MAC operations in [ANN]. Their results show that the Posit-based representation of networks’ parameters performs better than fixed-point-based representation in retaining the output accuracy of [ANN]. However, the Posit-based EMACs have significantly higher resource utilization and energy-delay product (EDP) than the fixed-point-based MAC operations. In [20], the authors have also proposed a parametrized Posit MAC generator to produce the HDL code of a Posit MAC unit. However, they do not present the efficacy of their proposed design in any real-world application. In [18], the authors have also used the EDP metric to compare their proposed Posit-based framework with the [FP32] and [Exp] based implementations; the [Exp] based implementations always produce lower EDP.
values than the corresponding Posit-based designs. Further, they do not report the overall resource utilization of their presented designs. The work in [19] and [15] have considered Posits for storing the trained weights of ANN and then utilizing the Posit-based operations to compute output values.

Currently, the Posit numerical scheme’s utilization in implementing accelerators for various applications is hampered by the unavailability of resource-optimized and energy-efficient Posit arithmetic units. In our proposed work, we aim to leverage the useful storage capability of Posit by modifying the Posit number representation to store numbers within the sub-normal region and the compute efficiency of Posit-based arithmetic by implementing a PoF32 converter.

### 3 System Model

#### 3.1 Application Model

The hardware designs proposed in our current work can be used for any arbitrary application that needs to communicate and/or store a large number of parameters. However, in this article, we limit our exploration to ANN. Fig. 4(a) shows one of the more widely used ANN—the VGG16—in research. As shown in the figure, VGG16 is composed of 16 layers of 4 different types—convolutional, max pooling, fully connected and softmax. Although we use the VGG16 as the application for evaluating our proposed methodology, the methods are applicable to any arbitrary ANN as most networks are composed of a subset of these types of layers. Fig. 4(a) also shows the dimension of the parameters that are used in each of the layers. Using accelerators for inference usually involves communicating and storing these large number of trained parameters—138 million for VGG16. Consequently, the quantization methods used for the parameters can influence the corresponding storage and communication overheads. Similarly, given the large number of MAC operations involved in the inference of a single input—15.5 billion for VGG16—the speed and power dissipation of the MAC unit determines the throughput and energy consumption of ANN inference.

#### 3.2 Architecture Model

Fig. 4(b) shows the architecture model used in this article. As shown in the figure, we assume an FPGA-based System-on-Chip (SoC) as the hardware platform. It contains an embedded processor along with reconfigurable logic similar to the Zynq EPP [36]. We assume that the accelerators for different types of layers of an ANN are executed on the reconfigurable logic and can implement the proposed hardware designs. For any accelerator, we assume that the parameters of the corresponding layer are fetched from the main memory through streaming interfaces with the on-chip AXI interconnect [37]. Similarly the input and output activations are transferred from and to the main memory using AXI streaming interfaces as well. Hardware platforms based on the Zynq EPP, such as the Ultra96-V2 [38], are being widely marketed as edge processing devices for Internet of Things (IoT).

### 4 Design Methodology

The top-level view of ExPAN(N)D is shown in Fig. 5. The Hardware design and characterization of the MAC units for various quantization schemes forms the central theme around which the other two methods—Behavioral analysis and Accelerator design—are implemented. Behavioral analysis enables the estimation of quantization-induced errors in a given ANN using the proposed hardware designs. Similarly, Accelerator design allows the designer to estimate the performance-resource trade-offs resulting from implementing various quantization schemes in an accelerator for a given layer of the ANN. The results from each of the three methods can be used to constraint the search space in the design of an efficient ANN using successive design
4.1 Hardware Design

4.1.1 Normalized Posit Representation
The Posit representation is inherently designed to encode numbers in the range $(-\infty, \infty)$. However, due to their tapered accuracy, numbers near $\pm 1$ have better accuracy in comparison to extremely small or large numbers. Thus, low-precision Posit numbers perform better than an equivalent linear fixed-point representation during the quantization of normalized ANN weights. While processing normalized numbers, sub-optimal utilization of all possible Posit bit-patterns leads to half of them being unused. This can translate to communication and storage overheads, as more than required bits are being transferred around. Similarly, a higher number of bits, than that required for storing the information, are processed during each computation. Hence, we propose normalized Posit—an alternative representation based on Posits which preserves its encoding efficiency, hardware realization and tapered accuracy while doubling the usable bit patterns within the normalized range. This normalized Posit representation is a logical subset of Posits that is customized for the representation of normalized numbers. For example, Table 2 shows all the possible bit-patterns and their equivalent real values for a Posit configuration of $N = 4, ES = 0$. The highlighted rows in the table show the bit-patterns which represent normalized numbers. It is evident that the two leading bits of the Posit representation are identical when the bit pattern denotes a normalized number; we leverage this finding to drop the leading Posit bit in our proposed normalized Posit representation.

This Posit representation helps us encode $N$-bit Posit functionality within the normalized range with $N - 1$ bits. This leads to a reduction in storage requirement while still being able to reuse existing Posit arithmetic hardware by replicating the leading bit near the processing unit. However, existing hardware implementations are not optimized to perform normalized Posit-only arithmetic. Existing implementations do not take complete advantage of the benefits arising as a consequence of the potentially unidirectional nature of bit shifts required to extract normalized Posits. To this end, we propose a novel parameterized Posit-to-Fxp converter, PoFx, that implements an optimized extraction for normalized Posit numbers.

4.1.2 PoFx Normalized Posit to Fixed-Point Converter
Most Posit-based computations require a decode stage to extract the value before arithmetic operations. Currently, Posit-based arithmetic relies heavily on extraction of Posit numbers to a floating point like representation before operating on them, which leads to increased resource utilization.
Algorithm 1 Posit (N,ES) to FxP (M,F)

Require: 
\(N, ES, M, F\)
\(\triangleright N\): Input Posit Bit Length
\(\triangleright ES\): Maximum Exponent Bit Length
\(\triangleright M\): FxP Output Length
\(\triangleright F\): Fraction length in FxP Output

\[\begin{align*}
1: \text{S} &= \text{POSIT} \left[ N - 1 \right] \\
2: M\text{AG}\left[ F \right] &= 1 \quad \triangleright \text{Set Leading Bit}
\end{align*}\]

\[\begin{align*}
\triangleright \text{A1: Extract Sign Component to FxP Output} \\
1: & \quad \text{S} = \text{POSIT} \left[ N - 1 \right] \\
2: & \quad M\text{AG}\left[ F \right] = 1 \quad \triangleright \text{Set Leading Bit}
\end{align*}\]

\[\begin{align*}
\triangleright \text{A2: Implement conditional Two’s Complement} \\
3: & \quad \text{if POSIT}\left[ N - 1 \right] == 1 \text{ then}
4: & \quad \text{POSIT}\left[ N - 2 : 0 \right] = \text{POSIT}\left[ N - 2 : 0 \right] + 1
\end{align*}\]

\[\begin{align*}
\triangleright \text{A3: Implement Modified Leading Zero Detector} \\
5: & \quad \text{if POSIT}\left[ N - 2 \right] == 0 \text{ then}
6: & \quad P\left[ N - 2 : 0 \right] = \text{POSIT}\left[ N - 2 : 0 \right]
\end{align*}\]

\[\begin{align*}
\triangleright \text{B1: Evaluate Regime Value} \\
10: & \quad V = \# 1’s \text{ In LZD} \\
11: & \quad \text{if POSIT}\left[ N - 2 \right] == 0 \text{ then}
12: & \quad K = V \quad \triangleright \text{Always 1}
13: & \quad \text{else}
14: & \quad K = V - 1
\end{align*}\]

\[\begin{align*}
\triangleright \text{B2: Extract Exponent and Fraction Fields} \\
15: & \quad E = \left[ e_{ES-1}, ..., e_1, e_0 \right] = 0 \\
16: & \quad \text{for } i = N - 4 \text{ do}
17: & \quad \text{EXT}[i] = \text{LZD}[i + 1] \quad \triangleright \text{To Generate Silhouette ST for Extraction}
18: & \quad \text{ST}[N - 4] = \text{EXT}[N - 4] \\
19: & \quad \text{for } i = N - 5 \text{ do}
20: & \quad \text{ST}[i] = \text{EXT}[i + 1] \quad \triangleright \text{Do } i < i + 1
\end{align*}\]

\[\begin{align*}
\triangleright \text{C: Shift Calculation} \\
21: & \quad \text{SHIFT} = 2^{E_{ES}} \ast K + E \\
22: & \quad \text{SHIFT} \text{ register size } = \left[ \log_2\left( M \right) \right]
\end{align*}\]

\[\begin{align*}
\triangleright \text{D: MAG < SHIFT} \\
31: & \quad \text{-ve Value = Right Shift}
\end{align*}\]

\[\begin{align*}
\triangleright \text{E: Sign Magnitude to Two’s Complement Block} \\
\end{align*}\]

The proposed PoFx converter can be adapted to perform normalized PoFx conversion which leads to lower resource utilization and improved performance in ANNs. This is primarily due to the drastic simplification of Stage C and Stage D as in this case the shifts are unidirectional, that is towards the right, making the value smaller. For normalized Posits we set \(\bar{F} = M - 1\) as all but one bit would be used for the sign. The first bit is replicated within Stage A followed by simplified extraction in Stage B1 as the regime bit would always begin with zero thus \(K\) would store only magnitude. We use an optimized algorithm to evaluate the modified shift equation \(2^{E_{ES}} \ast K - E\) in Stage C which is illustrated in Fig. 6. We store 1 after the assumed decimal point in normalized PoFx extraction and thus always need to right shift one time less. This is achieved implicitly by adding the one’s complement of \(E\) to \(2^{E_{ES}} \ast K\); further we will
set the overflow flag (OF) if the required number of shifts exceeds the width of the MAG field. Stage D is replaced with a standalone right bit-shifter while Stage E remains unchanged.

The five stages in our proposed design can be pipelined to further improve the throughput of the PoFx converter as there are no feedback paths between the stages, thus eliminating data hazards. We note that though normalized Posit representation can represent the value $-1$, the normalized PoFx cannot extract the same due to its implicit storage in sign-magnitude format. For the rest of the article, the term PoFx will be used to denote the normalized PoFx. Similarly, Posit($N, E_S$) and Posit($N - 1, E_S$) will be used to denote Posit and normalized Posit respectively.

### 4.1.3 MAC Unit with PoFx Converter

The PoFx converter can be used for any application that can benefit from storing a large number of parameters efficiently. As a special case for ANN, we integrate the normalized PoFx into MAC units to facilitate the use of our proposed optimizations for improving low-precision ANN inference. Fig. 7 shows the schematic of a parameterized PoFx converter based MAC along with ReLU activation function. As shown in the figure, the weights/biases are assumed to be stored/communicated as Posit($N - 1, E_S$) numbers. These values are then converted to their corresponding $M$-bit Fxp representations and multiplied with the $M$-bit input activation values. To accommodate the overflows resulting from the accumulation of a large number of $2M$-bit values, we propose to use a $3M$-bit adder. After accumulating all the values, for a single node in a layer of an ANN, we pass the $3M$-bit result to the activation function.

It can be noted that the PoFx based MAC unit allows the designer to represent the weights/biases with a fewer number of bits while still being able to implement different kinds of Fxp-based arithmetic optimizations, such as precision-scaling, approximations, etc. However, the effect of such a reduced bit representation on the ANN's behavior, and the corresponding reduction in the compute and communication/storage overheads of the associated accelerators for each layer needs to be estimated. The next two subsections provide the details of our contributions regarding these aspects of designing a PoFx-based ANN.

### 4.2 Behavioral Analysis

To evaluate the impact of various quantization schemes on the output accuracy of a DNN, we have utilized TensorFlow for implementing a high-level behavioral framework, as shown in Fig. 8. It evaluates each quantization scheme's efficacy by analyzing its impact on (a) accuracy of the quantized parameters, (b) errors generated in the output activations of each layer due to quantized parameters, and (c) the accuracy of the final output of the quantized DNN compared to FP32-based output. The multi-level analysis of the quantization-induced errors helps in the early elimination of the infeasible configurations. For this work, we have considered various configurations of the Fxp-based linear quantization and Posit-based representations, denoted by the Quantization Schemes in Fig. 8. However, our proposed framework is generic and allows the integration of other types of quantization schemes. Our proposed workflow performs a thorough analysis of the inter-conversions of these schemes to evaluate the impact of the available quantization step sizes and the dynamic ranges offered by each scheme. For example, the Fxp-based representation of an FP32-based parameter can be achieved as shown by paths in the figure. As shown by the classification accuracy results in Section 5, the utilization of each of these schemes has a distinct impact on the final output accuracy. After providing the description of an ANN and the various quantization schemes, the proposed framework provides quantization configurations fulfilling the desired accuracy constraints. These selected configurations are then used by our proposed Accelerator Design tool flow to compute their respective performance metrics.

### 4.3 Accelerator Design

The HLS-based design flow, shown in Fig. 9, is used for evaluating the associated trade-offs between computation overhead and communication/storage gains offered by the PoFx-based MAC units. The design choices tree originating from HLS directives shows the various degrees of freedom (not exhaustive) associated with the design of an accelerator for a fully-connected layer. We assume a weight-stationary, [40] design, where a set of weights for a subset of the artificial neurons in the layer are transferred once to the hardware accelerator. Subsequently, each input activation vector is transferred and the corresponding output activation of each neuron is computed. Therefore, the computation of each output activation vector can be seen as the multiplication of a matrix (weights) by a vector (input activations).
Consequently, HLS directives of pipelining and loop unrolling can be applied to the computation of the Dot Product (evaluation of the output activation of each node) and the Outer Product (evaluation of all output activations) for obtaining designs with varying performance and resource utilization. Similarly, the type of resources allocated for the weights matrix, BRAMs or LUTRAMs, and the associated array-partitioning choices can affect the accelerator characteristics.

The design decisions associated with the quantization schemes are integrated into the HLS-based flow. The computation mode, Posit- or FxP-based, and the associated bit-widths impact the accelerator performance considerably. The proposed accelerator allows the designer to send and store the weights in Posit($N - 1, ES$) or FxP format. If the weights are moved and stored as Posit($N - 1, ES$), the MAC units need to have the PoFx unit integrated into it (similar to Fig. 7). However, if the weights are moved as Posit($N - 1, ES$) and stored as FxP (using PoFx), the MAC units do not require the run-time conversion during each computation. However, this approach increases the storage requirements compared to storing as Posit($N - 1, ES$). It must be noted that the joint exploration across HLS directives and quantization schemes is necessary for a good estimation of accelerator characteristics. Performance improvement using HLS directives usually involves replicating compute and memory resources which are in turn dependent upon the choices related to the quantization schemes.

5 EXPERIMENTS AND RESULTS

5.1 Experiment Setup

The proposed PoFx converter and the associated computer arithmetic blocks were implemented using Verilog HDL. Python-based scripts were used for automating the generation of the parameterized designs. SmallPosit HDL [41] was used for generating the Posit-based arithmetic designs. The hardware designs were characterized using Xilinx Vivado Design Suite. For the calculation of the dynamic power of all implementations, Vivado Simulator and Power Analyzer tools have been utilized. All designs have been implemented on Xilinx Zynq UltraScale+ MPSoC (xczu3eg-sbv484-1-e device). The behavioral analysis was achieved using Python-based implementations and used TensorFlow [42] for estimation of various quantization induced error metrics. Xilinx Vivado HLS 18.3 was used as the High-level Synthesis tool for accelerator design. While the results for the behavioral analysis correspond to the experiments using VGG16 as the test application, all the proposed methods can be used for any arbitrary application.

5.2 Hardware Design

5.2.1 Normalized PoFx

We analyze the impact of varying output bit-width ($M$) of the PoFx converter on the overall performance of PoFx for a given configuration of Posit. Fig. 10 presents the results of the analysis for Posit ($N - 1 = 5, ES = 1$) configuration.

The variation in $M$, for a fixed Posit configuration, has an insignificant impact on the converter’s CPD. For a specific value of $\lceil \log_2(M) \rceil$, the overall LUT utilization also remains relatively unchanged. For example, the total number of utilized LUTs by PoFx for $M = 9$ is approximately 2.3 times the total number of utilized LUTs for $M = 8$. The total number of utilized LUTs also directly affects the dynamic power consumption of the PoFx. The minor variations in the Power metric of the PoFx is a result of the optimizations performed by the synthesis tool. Compared to resource utilization of Posit-based arithmetic units (discussed in the following sections), the PoFx has an insignificant contribution to the overall resource utilization of FxP-based arithmetic units.

Fig. 11 compares the impact of various Posit configurations, varying $N - 1$ and $ES$, on the performance metrics of PoFx for a fixed bit-width ($M$) of the output. The critical path delay follows an increasing trend with an increase in the values of $ES$ and $N - 1$. This trend is primarily due to an increase in the logic required for Posit extraction due to increased variability in the individual field length. The designs with $ES = 0$ have minimum resource utilization. The absence of the exponent field results in significant simplification of the overall extraction circuit. However, the designs with $ES \in \{2,3\}$ have comparably higher resource utilization. A similar trend is also observed for the

1. Similar results are obtained for other Posit configurations.
2. As described in Algorithm 1, the $\lceil \log_2(M) \rceil$ is used to calculate the size of the shift register for computing the corresponding FxP value.
dynamic power consumption of the PoFx for various Posit configurations.

5.2.2 MAC Design Analysis
The proposed PoFx allows the utilization of resource-efficient and high-performance Fxp-based arithmetic units for Posit number systems. To evaluate the efficacy of the proposed approach and estimate the associated overheads of the PoFx, we compare PoFx-based 8-bit MAC units with a traditional Fxp-based MAC unit. The results of these comparisons for various configurations of Posit are presented in Fig. 12. The critical path delay and resource utilization of the MAC follow a gradually rising trend with both N and ES values. It can be noted that in a few cases, especially for ES = 0, the PoFx-based MAC provides better performance across critical path delay, power dissipation, and LUT utilization than the Fxp-only MAC. For ES = 0, the Posit scheme’s dynamic range is limited, and the PoFx does not utilize the complete dynamic range of the Fxp. The limited number of unique Fxp values, after conversion, allows the synthesis tool to optimize the overall design of the PoFx-based MAC to improve the associated performance metrics. The power metrics do not follow a well-defined trend as they are generated based on the bit switches required to obtain the correct bit-sequence as the output. Compared to the Fxp-only MAC, we report worst-case overheads of 22.8%, 5.0%, and 15.5% for critical path delay, power dissipation, and LUT Utilization, respectively. Similar trends are observed in Fig. 13, which compares the same performance metrics for a 16-bit Fxp MAC.

To further evaluate the efficacy of the PoFx-based MAC design, we compare it with Fxp-only MAC, Posit-only MAC, and Posit-based 3-input Fused Multiply Add (FMA) [41]. Moreover, for a thorough exploration of the Fxp, FxP, and Posit-based designs, we have synthesized two types of designs—one that allows the synthesis tool to optimize across the constituent blocks (converters, multipliers, and adders) and the other that performs optimization for the constituent blocks separately. Fig. 14 and Fig. 15 show the comparison of the power-delay-product (PDP) and the LUT utilization of these designs for 8- and 16-bit designs, respectively. Posit-only MAC, which has been implemented by using a standalone N-bit Posit adder and N-bit Posit Multiplier, has significantly higher PDP and LUT utilization as a result of the extraction and packaging of Posits between stages. The Posit-based FMA, though optimized, requires more hardware resources for implementation. It can be observed that the PoFx-based MAC designs fall closely within the range of the Fxp-only MAC. Further, the Posit-only MAC and Posit-based FMA designs generate an N-bit output whereas, the proposed design generates a more precise 3N-bit output once extracted. This can lead to lower inter-layer losses in ANNs as we can ascertain the type of rounding mechanism at the output based on the network to retain as much precision as possible before transferring the value to the next stage.

5.3 Behavioral Analysis
We have considered DNNs as a test case to show the impact of various number representation schemes on the output accuracy of high-level applications. For this work, we have
and 0.001 only. We also evaluate the interconversions of various schemes to identify feasible configurations for PoFx-based hardware. For example, the Posit(N − 1 = 7, ES = 2) → 8-bit FxP scheme produces an average absolute error of 0.003, whereas the 8-bit FxP → Posit(N − 1 = 7, ES = 2) → 8-bit FxP generates an average error of 0.002 only. Fig. 16 also reveals that Posit(N − 1 = 3, ES = 2)-based configurations can be eliminated in the first step due to large quantization-induced errors. We have performed a similar analysis for all layers of the VGG-16 network by exploring all combinations of Posit(N, ES) where \( N \in \{4, 5, 6, 7, 8\} \) and \( ES \in \{0, 1, 2, 3\} \), and 8-bit FxP. The analysis identifies the quantization schemes producing the minimum average absolute error and the maximum absolute error for each layer of the network. For each \( N \)-bit Posit scheme, the quantized parameters are analyzed to identify the values of \( ES \) inducing minimum quantization errors.

![Fig. 14: Comparison of various 8-bit MAC implementations: for Posit(N − 1, ES) \( N − 1 \in \{4,..,7\} \) and \( ES \in \{0,1,2\} \)](image)

![Fig. 15: Comparison of various 16-bit MAC implementations: for Posit(N − 1, ES) \( N − 1 \in \{4,..,15\} \) and \( ES \in \{0,1,2,3\} \)](image)

used a pre-trained VGG16 network for the classification of the ImageNet dataset. The VGG16 network mainly consists of 13 convolution layers and 3 fully connected layers. The very large number of the network’s trained parameters, 138 million, makes it a sound candidate for hardware. For example, the Posit(N = 4, \( ES = 2 \)) scheme produces an average absolute error of 0.004 for all configurations. Maximum absolute quantization-induced error of each configuration is shown above the corresponding average relative error bars.

### TABLE 3

| VGG16 Layer | Number of points on Pareto front | % Improvement in hypervolume due to PoFx-based MAC |
|-------------|----------------------------------|-----------------------------------------------|
| MAC Type    | PoFx-based | Posit-based | FxP-based | Max Bits | 8 | 16 | 8 | 16 | 8 | 16 | 8 | 16 | 8 | 16 | 8 | 16 |
| conv1_1     | 9          | 7           | 7           | 1          | 0          | 173       | 74       |
| conv1_2     | 8          | 4           | 4           | 3           | 11          | 1          | 25       |
| conv2_1     | 9          | 3           | 3           | 2           | 8           | 10         | 194      |
| conv2_2     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv3_1     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv3_2     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv3_3     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv4_1     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv4_2     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv5_1     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv5_2     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv5_3     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv6_1     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv6_2     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| conv6_3     | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| fc1         | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| fc2         | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| fc3         | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| fc4         | 8          | 2           | 2           | 2           | 8           | 10         | 194      |
| fc5         | 8          | 2           | 2           | 2           | 8           | 10         | 194      |

In our current work we focus only on the quantization of weights and biases. The use of a specific quantized representation of the weights and biases will require the use of a compatible MAC design for inference. Hence, we performed a joint analysis of the performance of the various MAC designs and the errors induced in the parameters by the corresponding quantization scheme. The various MAC designs are grouped under three categories — PoFx-based, Posit-based (that includes both multiply and adder)

4. As shown in Fig. 8
5.3.2 Output Activation Error Analysis

In the second step of behavioral analysis, our framework utilizes the quantized parameters to evaluate each configuration’s impact on the output activations of each layer. The computation of the output activation involves using a MAC design that is compatible with the chosen quantization scheme. Similar to the analysis presented in Fig. 17 for the errors induced in the parameters, Fig. 18 shows the design space while considering the errors in the output activations for the first layer—Conv1_1—of VGG16. The 3D scatter plot shows the various design points corresponding to the three categories of MAC designs, PoFx-, Posit- and FXP-based. It can be observed from Fig. 18 that the PoFx and FXP-based designs’ contribution to the Pareto-front is mainly due to better hardware performance—lower PDP and reduced number of utilized LUTs. Similarly, Posit-based designs’ contribution is mainly due to lower average error, albeit at high hardware costs. The resulting Pareto-front in Fig. 18 has 7, 13 and 1 points from PoFx, Posit- and FXP-based designs respectively, with 12.4% improvement in the hypervolume over the collection of only Posit- and FXP-based designs. It must be noted that since we focus on combination and FMA-based designs) and FXP-based. For the PoFx-based and Posit-based designs, lower bit-width input designs were also considered. For example, for 8-bit quantization, N was varied from 5 to 8. Similarly, for 16-bit quantization, N was varied from 5 to 16. Table 3 shows the Pareto analysis results for 8- and 16-bit MACs with the three objectives—PDF, average quantization-induced error and the LUT utilization. We report the number of dominating points for each of the three types of quantization schemes used for the parameters of each layer of VGG16. As shown in the table, using PoFx-based designs contribute significantly to the number of points on the Pareto-front for 8-bit precision. We also report the percentage increase in the Pareto-front hypervolume due to the usage of PoFx-based designs over the collection of Posit and FXP-based designs only. As seen in the table, using PoFx-based designs we report up to 173% increase in the hypervolume for 8-bits precision. Fig. 17 shows the dominating and dominated points for each of the three categories in the corresponding design space for 8-bit precision MACs for the first layer (Conv1_1) of VGG16. It can be observed that the Posit- and FXP-based designs contribute one point each to the resulting Pareto-front, compared to 9 PoFx-based points.

The improvements for 16-bit precision are lower compared to 8-bits. However, as shown in Table 4 if we also consider the bits-width of the parameters as a design objective in the analysis, we report consistent improvements using PoFx-based designs for both 8- and 16-bits precision. Since the number of input bits is an indicator of the communication power dissipation (and energy consumption) for moving weights, using PoFx-based quantization can result in reducing the overall power dissipation during DNN inference.

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the quantization schemes for only the parameters, during the behavioral analysis, the input activations for each of the layers are kept at \(\text{FP32}\) precision. After computing the output activations, they are quantized using the configuration employed to quantize the respective parameters. This lets us evaluate the impact of the proposed methods and designs while other aspects are kept unchanged.

### 5.3.3 Classification Error Analysis

Finally, the behavioral analysis involves estimating the impact of the proposed methods on the classification accuracy. \(\text{TABLE 5}\) shows the percentage Top-1 and Top-5 classification accuracies of the ImageNet validation dataset \([43]\) using different quantization schemes. For this experiment, the activations have \(\text{FP32}\) precision, and the parameters (weights and biases) are quantized using various 8-bit schemes. For comparison, we also show the classification accuracy using 7-bit and 16-bit \(\text{FP}\)-based quantization techniques. The \(\text{FxP-16}\) and \(\text{Posit}(N = 8, ES = 2)\) produce similar classification results by reducing the final output accuracy by only 0.06 and 0.07, respectively when compared with \(\text{FP32}\)-based results. The \(\text{FxP-8}\)-based configuration reduces the Top-1 and Top-5 classification accuracy by 5.01 and 2.83, respectively. However, the \(\text{Fxp-7}\)-based quantization significantly drops the final classification accuracy. For the \(\text{PoFx}\)-based schemes, we consider the normalized \(\text{Posit}(N-1, ES)\) configurations for N-bit Posit numbers. \(\text{TABLE 5}\) reveals that the direct conversion of Posit numbers to \(\text{Fxp}\) scheme (\(\text{Posit-Fxp}\)) significantly diminishes the final output accuracy. However, utilizing \(\text{Fxp}\) → Posit→ \(\text{Fxp}\)-based conversion, the \(\text{Posit}\) has an insignificant impact on the final output. For example, compared to the \(\text{Fxp}\)-based results, the \(\text{Fxp-8} \rightarrow \text{Posit}(N-1 = 6, ES = 2) \rightarrow \text{Fxp-8}\) decreases the Top-1 and Top-5 classification accuracy by only 0.35 and 0.26.

\(\text{TABLE 5}\) shows the joint analysis of the ImageNet and MAC hardware characteristics for a subset of the configurations. It contains only those configurations from \(\text{TABLE 5}\) that have comparable accuracy and having feasible hardware designs. For instance, arithmetic blocks for \(\text{Posit}(N = 6, ES = 3)\) could not be generated using SmallPosit HDL \([41]\). Similarly, as shown in \(\text{TABLE 5}\), the \(\text{Posit-Fxp}\) modes have much lower accuracy than similar configurations for \(\text{Fxp}\) → Posit → \(\text{Fxp}\) while requiring the same \(\text{Posit}\)-based MAC, and are hence omitted from the analysis. The PDP and LUT utilization values for each configuration in \(\text{TABLE 6}\) are obtained from the lowest PDP design for that configuration. The PDP and LUT metrics shown in the table correspond to values relative to the maximum shown in the table’s top row. The highest value of PDP and LUT utilization occurs for the configurations \(\text{Posit}(N = 8, ES = 1)\) and \(\text{FxP-16}\) respectively. The highest and lowest values of the performance metrics for each of the two categories – \(\text{Posit}\) and \(\text{PoFx}\) are highlighted in bold text in \(\text{TABLE 6}\). It can be observed that the Posit configuration for the highest Top-1 accuracy, \(\text{Posit}(N = 8, ES = 2)\), corresponds to the MAC design with highest LUT utilization. Similarly, the Posit configuration with highest Top-5 accuracy, \(\text{Posit}(N = 8, ES = 1)\) (and \(\text{Posit}(N = 8, ES = 2)\)), corresponds to highest (and relatively higher) PDP value. The Posit configuration with the lowest accuracy, \(\text{Posit}(N = 6, ES = 2)\), corresponds to the design with lowest PDP and LUT utilization among Posit-based MACs.

Similar correlations were also observed in the case of \(\text{PoFx}\)-based designs. Designs with higher PDP usually result in better accuracy. Compared to \(\text{Fxp}\)-based designs the \(\text{PoFx}(N-1 = 7, ES = 1)\) achieves similar accuracy with lower PDP (≈ 5%) and slightly higher LUT overhead (≈ 15%). Similarly, \(\text{PoFx}(N-1 = 6, ES = 2)\) achieves comparable accuracy with even lower PDP (≈ 18%) and less LUT overheads (≈ 8%). Additionally, these \(\text{PoFx}\)-based designs requires less bits for representing the parameters.
of a network. This can result in lower communication and storage overheads in the accelerator design for each layer of the network.

5.4 Accelerator Design Analysis

In order to estimate the system-level impact of using the proposed PoFx methodology, we integrated the candidate solutions in the design of an accelerator for a fully-connected layer of a DNN. The accelerator was designed using C++ and synthesized using Xilinx’s Vivado HLS. To keep the design generic, we implemented a matrix-vector multiplication. The matrix, representing the weights of the fully-connected layer, was of size $64 \times 10$. Each vector, representing an input activation, is of size $1 \times 64$. One thousand input activations were used to estimate the switching activity in order to compute the power dissipation. The implemented accelerator uses ReLU activation function.

5.4.1 Accelerator DSE

In Section 4.3, we presented some of the degrees of freedom in the design of an accelerator that can result in varying performance metrics and resource requirements. Fig. 19 shows the resulting metrics from seven different implementations of the accelerator under test using 8-bit FxP parameters and activations. The base implementation refers to the basic design without using any HLS directives. As shown in Table 7, the other implementations vary in terms of the optimization goals, and the type and partitioning of the memory used for storing weights and activations. As seen in Fig. 19, the optimizations of fullOpt result in the lowest latency implementations. However, it also results in the highest power dissipation and maximum resource utilization. Also it can be noted from the figure that using BRAMs results in lower total power dissipation than using LUTRAMs for both fullOpt and dotOpt implementations.

Further, it can be observed that the CPD varies with the optimization modes, even with the usage of the same arithmetic hardware, as the implementation of multiple parallel operators spreads the designs spatially and the routing delays tend to increase accordingly. It must be noted that Fig. 19 shows only a subset of the possible implementations using the various degrees of freedom. While it is possible to generate many more design points using various types of array partitioning and loop-related HLS directives, we limit our evaluation to these seven types of implementations for showing the impact of our proposed designs.

5.4.2 Accelerator Resource Requirements

In order to compare the effect of using Posit-based, PoFx-based and FxP-based MAC units, we implemented the following four accelerator designs:

1) **Posit**: The accelerator stores and computes all operations in Posit($N, ES$) format.
2) **PoFx(Move)**: The weights are moved to the accelerator in normalized PoFx($N-1, ES$) representation, converted to FxP and stored as FxP($M = 8$) numbers. During computations, the FxP($M = 8$) weights are fetched from local memory and used directly for arithmetic.
3) **PoFx(Move & Store)**: The weights are moved from main memory and stored in local memory in normalized PoFx($N-1, ES$) format. During computation, the weights are fetched from local memory, converted to FxP($M = 8$) and used in the computation of the output activation values.
4) **FxP(8)**: The weights are moved from main memory to accelerator and stored in the local memory of the accelerator as FxP($M = 8$) numbers. Similar to PoFx(Move), the computation stage does not involve any conversions between number representations.

Fig. 20 shows the comparison of the performance metrics of these four designs for base, dotOpt and fullOpt implementations. The configurations used for representing the weights in these designs are Posit($N = 6, ES = 0$), PoFx($N-1 = 5, ES = 0$) and FxP($M = 8$). It can be observed that the Posit-based design has higher CPD, power dissipation and LUT utilization for almost every implementation. For instance, we report $\approx 80\%$ reduction in the CPD with the PoFx(Move & Store)-based design for the fullOpt implementation. The latency metric is similar in case of each implementation type across the four design types. It can be observed that the PoFx(Move & Store) has higher CPD than PoFx(Move) for base implementation, but lower CPD for dotOpt and fullOpt implementations.

In the base implementation of PoFx(Move & Store), the additional overhead of the PoFx(Mac) conversion during computation increases the CPD. However, in the dotOpt and fullOpt implementations, the additional interfaces of the

![Fig. 19: Hardware metrics for accelerator design implementing FxP-based MAC using different optimization modes.](image-url)

![Table 7: Accelerator implementations used for analysis.](table-url)
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Fig. 20: Relative hardware metrics for accelerator using base, dotOpt and fullOpt implementations for four types of designs. The quantization configurations used are Posit(N = 6, ES = 0), PoFx(N = 1, ES = 0) and FxP(M = 8).

Fig. 21: Variation in the relative resource utilization of BRAM-based accelerator (fullOpt_BRAM) implemented with varying Posit and PoFx designs compared to FxP(8)-based designs.

Fig. 22: Variation in the relative resource utilization of LUTRAM-based accelerator (fullOpt_LRAM) implemented with varying Posit and PoFx designs compared to FxP(8)-based designs.

partitioned, higher bit-width \(\text{FxP}\) weights-array dominates the low-cost \(\text{PoFx}\) converter delay. Since in the absence of any memory-specific HLS directives, the LUTs are used to store the weights, the LUT utilization of \(\text{PoFx}(\text{Move & Store})\) design is the lowest for each implementation type. We report \(\approx 60\%\) reduction in the LUTs utilization with the \(\text{PoFx}(\text{Move & Store})\)-based design over the Posit-based design for the fullOpt implementation. Further, BRAMs are not instantiated in the dotOpt and fullOpt implementations in any of the designs. However, as shown in Fig. 19, BRAMs present a more power-efficient alternative.

We explored the impact of using memory-related HLS directives in the four designs for the fullOpt and dotOpt implementations. Fig. 21 shows the accelerators’ relative resource requirements for the fullOpt_BRAM implementation of the four designs with varying configurations of Posit\((N, ES)\) and \(\text{PoFx}(N - 1, ES)\). It can be observed that the LUT utilization of Posit is much higher in all cases. This can be attributed to the high hardware costs of the Posit arithmetic blocks. Similarly the RegFF utilization of \(\text{PoFx}(\text{Move & Store})\) is lower than that of \(\text{PoFx}(\text{Move})\) designs for most cases. However, the BRAM utilization
remains constant for all the designs across all configurations. This is due to the granularity of the BRAM memory. Even if weights are stored as values lower than 8-bits, equal number of instances of BRAMs are used. However, as shown in Fig. 22 if LUTRAMs are used for storing the weights and activations (fullOpt_LRAM implementation), lower LUTRAM utilization is observed in $\text{PoF}_{\text{X}}$ (Move & Store) than $\text{PoF}_{\text{X}}$ (Move). For instance, compared to the Posit($N = 7$, $ES = 0$) we report $\approx 46\%$ reduction in LUTRAM utilization with the $\text{PoF}_{\text{X}}$($N - 1 = 6$, $ES = 0$) design. This difference is reduced to zero in $\text{PoF}_{\text{X}}$($N - 1 = 7$, $ES = 0$). Similarly, the difference in RegFF utilization of $\text{PoF}_{\text{X}}$ (Move) and $\text{PoF}_{\text{X}}$ (Move & Store) reduces with increasing value of $N - 1$. Therefore, the proposed $\text{PoF}_{\text{X}}$ representation results in reduction in the accelerator’s overall resource consumption.

6 Conclusion

To implement machine learning applications on resource- and energy-constrained embedded systems with limited computational power, it is imperative to consider the unique features of various optimization techniques together. This paper proposes the ExPAN(N)D framework for analyzing and combining the number representation efficacy of the Posit scheme and the resource- and compute-efficiency of the $\text{F}x\text{P}$-based schemes. ExPAN(N)D utilizes a modified and novel representation of Posit numbers systems to represent the trained parameters of the DNN. Using the proposed scheme, we use $\hat{N}$ - 1 bits for an $N$-bit Posit configuration to reduce the storage requirements. For performing arithmetic operations on trained parameters, stored in Posit format, ExPAN(N)D proposes and utilizes a resource-efficient Posit to $\text{F}x\text{P}$ converter $\text{PoF}_{\text{X}}$. Using $\text{PoF}_{\text{X}}$, all arithmetic operations are performed using $\text{F}x\text{P}$-based arithmetic operators.

Compared to 6-bit Posit-based implementation, our proposed 8-bit Posit-based ANN accelerator provides up to 80% and 60% reduction in overall resource utilization and critical path delay, respectively for the highest throughput design. Further, compared to an 8-bit $\text{F}x\text{P}$-based implementation, the 8-bit $\text{PoF}_{\text{X}}$ based accelerator provides up to 46% reduction in storing the trained parameters. ExPAN(N)D utilizes a TensorFlow-based behavioral framework to evaluate the impact of different quantization configurations on the final output accuracy of the DNN. We intend to extend the proposed framework by incorporating other networks’ optimization techniques such as approximate arithmetic operators and various other quantization schemes.

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