NetReduce: RDMA-Compatible In-Network Reduction for Distributed DNN Training Acceleration

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Abstract

We present NetReduce, a novel RDMA-compatible in-network reduction architecture to accelerate distributed DNN training. Compared to existing designs, NetReduce maintains a reliable connection between end-hosts in the Ethernet and does not terminate the connection in the network. The advantage of doing so is that we can fully reuse the designs of congestion control and reliability in RoCE. In the meanwhile, we do not need to implement a high-cost network protocol processing stack in the switch, as IB does.

The prototype implemented by using FPGA is an out-of-box solution without modifying commodity devices such as NICs or switches. For the coordination between the end-host and the switch, NetReduce customizes the transport protocol only on the first packet in a data message to comply with RoCE v2. The special status monitoring module is designed to reuse the reliability mechanism of RoCE v2 for dealing with packet loss. A message-level credit-based flow control algorithm is also proposed to fully utilize bandwidth and avoid buffer overflow.

We study the effects of intra bandwidth on the training performance in multi-machines multi-GPUs scenario and give sufficient conditions for hierarchical NetReduce to outperform other algorithms. We also extend the design from rack-level aggregation to more general spine-leaf topology in the data center. NetReduce accelerates the training up to 1.7x and 1.5x for CNN-based CV and transformer-based NLP tasks, respectively. Simulations on large-scale systems indicate the superior scalability of NetReduce to the state-of-the-art ring all-reduce.

1 Introduction

Over the last decade, numerous Artificial Intelligent (AI) applications, such as computer vision (CV) [21, 27, 49] and natural language processing (NLP) [30, 50], have benefited from the rapid development of Deep Neural Networks (DNNs).

However, DNN training remains time-consuming due to the growing size of training datasets and models. Since 2012, the computing requirement of AI training has been increasing exponentially with a 3.4-month doubling time [38], which is much faster than the observation described by Moore’s Law (i.e., 2-year doubling period). Therefore, the scale-up techniques [20, 26, 37] concentrating on the computing capability of a single device cannot fulfill the requirement. In this paper, we focus on the scale-out strategy, distributed system, for DNN training.

Distributed DNN training with synchronous data parallelism is commonly employed in practice. Each computing node has an entire model replica and cannot iterate until the model parameters are synchronized. Unfortunately, this is increasingly a network-bound workload since communication becomes a bottleneck at scale [10, 31, 47]. The extra communication overhead caused by parameter synchronization makes it difficult for the system to achieve linear scaling. Moreover, the commonly used communication strategies have low efficiency. For example, the approaches based on Parameter Server (PS) [9, 11, 28] easily lead to the incast of network traffic and wasted resources. All-reduce approaches [15, 46] decentralize the workload by using a peer-to-peer communication pattern but require to transmit the data with twice the original model size (§2.1).

Recently, a new direction to accelerate distributed DNN training by using in-network aggregation has been explored [18, 45]. Compared to the state-of-the-art all-reduce strategy, this approach reduces nearly half the aggregation data by offloading gradients aggregation from end-hosts to the network switch (§2.2). Two important issues arise upon practical implementation of in-network aggregation. First, the network should provide efficient and robust transport to fulfill the high requirement of end-to-end throughput in distributed DNN training. Second, in-network aggregation as an add-on function of the switch should be implemented considering the balance between the induced cost and the processing efficiency in the critical forwarding path.

Unfortunately, existing designs [18, 45] are far from the
above-mentioned requirements. SwitchML [45] uses the User Datagram Protocol (UDP) for network transport which cannot provide congestion control of the traffic. When facing packet loss, the system solely relies on application-layer timeout to trigger retransmission which introduces extra latency. Additionally, SwitchML uses programmable switch Application-Specific Integrated Circuit (ASIC), Tofino [5], to implement in-network aggregation. Such ASIC chip is incapable of processing full-length Ethernet frames due to its limited register resource in the match-action pipeline and thus results in an end-to-end throughput reduction. SHARP [18], on the contrary, employs reliable connection (RC) transport by using Remote Direct Memory Access (RDMA) technology, InfiniBand (IB) [3], which is more robust. However, instead of those for existing Ethernet, IB relies on specific hardware (e.g., host channel adapter, new optical module) to establish connections between the end-host and the network switch, which is not cost-effective. In this paper, we utilize RDMA over Converged Ethernet (RoCE) protocol which encapsulates the IB transport packet over Ethernet for balancing the robustness and the cost of the in-network aggregation system. Specifically, we focus on RoCE v2 [2] which exists on top of either IPv4 or IPv6 protocol. We will further describe the details in §2.3.

In this paper, we present NetReduce, an RDMA-compatible in-network reduction solution to accelerate distributed DNN training. Unlike that existing designs offload the PS into the network directly, NetReduce maintains a reliable connection between end-hosts in the Ethernet and does not terminate the connection in the network. The advantage of doing so is that we can fully reuse the designs of congestion control and reliability in RoCE v2. In the meanwhile, we do not need to implement a high-cost network protocol processing stack in the switch, as IB does.

We implement NetReduce via Field Programmable Gate Arrays (FPGA), without any modification to commodity Ethernet Network Interface Controller (NIC) or switch. In SwitchML, a single packet carries only 128 bytes of gradients which cannot fully exploit the packet processing capability of the NIC and the switch. On the contrary, NetReduce by using FPGA is capable of processing a packet with a payload size of 1024 bytes, increasing the end-to-end throughput. Very little previous work aims to optimize the aggregation of the long message which faces the challenge of addressing a huge amount of data in a single collective operation. For example, in SHARP [17], a piece of the message only contains one packet. Nevertheless, the NetReduce switch can handle the message with 170 KB, which introduces less than 3 µs extra Round-Trip Time (RTT) latency with additional FPGA operations.

The contributions of this paper are summarized as follows:
1. We present NetReduce, the first implementation of RoCE-compatible in-network aggregation in the field, to the best of authors’ knowledge. NetReduce cost-effectively realizes in-network aggregation by not terminating the end-to-end connection. A recovery algorithm (§4.3.1) is proposed and a status monitoring module (§4.3.2) is designed to support native RoCE v2 protocol. We also extend the design from rack-level aggregation to more general spine-leaf topology in the data center (§4.5).
2. At the host side, we design a new transport layer protocol to coordinate end-hosts with the switch (§4.1). We also propose a message-level credit-based flow control algorithm to fully utilize bandwidth and avoid the overflow of switch buffer (§4.2).
3. We develop communication cost models of different training algorithms in multi-machines multi-GPUs scenario. Based on the developed models, we give sufficient conditions that hierarchical NetReduce is more communication-efficient than other algorithms (§3.2).
4. We implement a NetReduce prototype by using FPGA. The experimental results in both multi-machines single-GPU (§5.2) and multi-machines multi-GPUs (§5.3) cases show that NetReduce provides a larger data processing throughput than traditionally used algorithms. Additionally, NetReduce with fixed-point arithmetic does not impact the training convergence compared with floating-point arithmetic.
5. We perform simulations based on the aforementioned models to evaluate the communication cost of different algorithms, in large-scale distributed DNN training systems involving up to thousands of GPUs. The simulation results are consistent with previous research and indicate the superior scalability of NetReduce to ring all-reduce (§5.4).

2 Background and Motivation

2.1 Parameter Synchronization

In general, methods of parameter synchronization in distributed DNN training can be classified into two categories: PS and all-reduce. The PS-based approaches generally work in a “push + pull” way. At each iteration, all workers first push their computed gradients to PSs. Then PSs aggregate the gradients and update the model with new weights. Finally, workers pull the updated weights from PSs and start the next computing iteration. PS can easily become a bottleneck: the push phase leads to the traffic incast and the pull phase results in data redundancy in the network. Moreover, the benefits by using PSs depend on the additional CPU resources provided [4, 8]. Assume a homogeneous training system (i.e., all the machines are equipped with the same number of GPUs), the PS does not save anything.

An all-reduce operation performs reductions on data across nodes and writes the result to each node. This process consists of two phases: scatter-reduce and all-gather, where each node ends up with partial and global aggregation data, respectively. An all-reduce operation can be implemented in different ways. A halving/doubling algorithm is employed in [16] which has
two major drawbacks: 1) the overhead of data transfer is doubled for non-power-of-two case [53]; 2) the communication pattern involved may lead to network contention [39]. Baidu [15] introduces ring all-reduce which has become the most popular algorithm ever since. This implementation is bandwidth-optimal since contention-free communication can be achieved.

2.2 In-Network Aggregation

In-network aggregation accelerates distributed DNN training by offloading gradients aggregation into the network switch. For example, SwitchML [45] shows that using a programmable data plane [5, 7, 24, 25, 44] to aggregate gradients on-path reduces the amount of data transferred. SHARP [17, 18] is an IB-compatible hardware architecture for in-network aggregation which relies on fixed-function ASIC. In addition to DNN, iSwitch proposed in [29] accelerates reinforcement learning which generates more frequent gradient aggregations with smaller sizes by using NetFPGA [51].

Suppose that a homogeneous distributed DNN training system has $P$ ($P \geq 2$) GPUs and each machine is equipped with one GPU. To synchronize data with size $M$ amount transmitted by each node is reduced from $O(2P)$ times, in-network aggregation only transmits once, reducing the complexity from $P$ to $O(1)$. Additionally, the data amount transmitted by each node is reduced by using ring all-reduce in the multi-machines single-GPU case.

When $P \geq 2$, Eq.(3) > 0, which means that in-network aggregation always takes less communication time than ring all-reduce in the multi-machines single-GPU case.

2.3 Why RoCE Matters

SwitchML [45] is built upon UDP for network transport. One issue of using UDP lies in the I/O performance since using UDP solely cannot fully use network bandwidth, e.g., 100 Gbps. Therefore, SwitchML employs Data Plane Development Kit (DPDK) [14] to bypass the kernel for increasing port throughput (i.e., packets per second). To achieve full 100 GE bandwidth, many CPU cores need to be bound to a specific port by using DPDK, which wastes lots of CPU cycles. We aim at the real-world Data Center Network (DCN) environment where CPU resources matter.

Another issue is that UDP cannot handle transport-level congestion control and retransmission. In typical distributed DNN training jobs, network transportation is in RC mode. However, SwitchML relies on application-level timeout to deal with packet loss which again occupies extra CPU cycles. This may not be a severe problem if a clean slate network dedicated to AI training is assumed. But in a real DCN environment with tremendous background traffic, only application-level flow control is not enough.

The state-of-the-art DCN employs RoCE v2 protocol for transportation [19]. RoCE v2 increases I/O throughput by a kernel-bypassing technique which reduces CPU overhead and processing latency. Additionally, the NIC supporting RoCE has a complete mechanism of congestion control and reliability assurance.

In terms of low latency, IB suits well in SHARP, which aggregates relatively-small messages/packets in High-Performance Computing (HPC) scenario [17]. However, distributed DNN training requires high throughput where RoCE v2 does not lose to IB. More importantly, RoCE v2 supports a larger network in a more cost-effective manner than IB. SHARP terminates the end-to-end connection in the network by using special devices such as Target Channel Adapter (TCA), which is not compatible with ordinary Ethernet. On the contrary, NetReduce as an add-on function that supports RoCE v2 does not modify Ethernet commodity devices such as NIC or switch.

3 NetReduce Overview

In this section, we first describe the fundamental operation principle of NetReduce and then present a theoretical analysis of communication cost in comparison to other approaches. For easy understanding, we start to introduce NetReduce from a simple multi-machines single-GPU scenario (i.e., each machine is equipped with only one GPU) before discussing the more general case.
3.1 Single GPU in A Machine

Similar to ring all-reduce, NetReduce forms a logical ring (colorful dashed curves in Figure 1) where each node only communicates to its neighboring nodes. This is because RoCE v2 only supports a point-to-point connection and the maintenance of such a connection minimizes the number of state machines implemented in the switch. In ring all-reduce, each node receives different data (colorful dash-dotted lines in Figure 1(A)) from the other node, which is unaggregated and the same as what its neighbor sends (colorful solid lines in Figure 1(A)). In NetReduce, on the contrary, different nodes receive the same data, which is the aggregation result from all nodes (bold solid lines in Figure 1(B)). When the packets from different nodes arrive at the NetReduce switch, the switch aggregates the gradients at the same neural network layer, replaces the payload of the packets with the aggregation result, and forwards them.

Another difference of NetReduce from ring all-reduce lies in the sending order of the data. In ring all-reduce, different nodes need to transmit the data in different layers to optimize bandwidth utilization. After receiving the data block, the nodes aggregate the corresponding gradients themselves. Instead, NetReduce offloads the gradients aggregation from end-hosts to network switches and ensures the aggregation correctness by letting different nodes send the same piece of data.

3.2 Multiple GPUs in A Machine

A straightforward approach in the multi-machines multi-GPUs scenario is to consider every GPU as homogeneous, regardless of the intra ones (connected via expansion bus inside a single machine) or the inter ones (connected via computer network between different machines). All GPUs are hence connected through a big flat ring but there would be a bandwidth gap between the intra ring (e.g., PCIe or NVLink) and the inter ring (e.g., Ethernet or InfiniBand).

Another strategy, called hierarchical all-reduce, first aggregates parameters inside every single machine and then exchanges the aggregation results between the machines. Tencent proposed a three-phase hierarchical all-reduce algorithm in [23], of which the process is as shown in Figure 2(A). In the first phase, GPUs in the intra rings perform reduce operation. Unlike that all-reduce operation writes data to every GPU, reduce operation writes the local aggregation result only to a single master GPU. In the second phase, the master GPUs among different machines form an inter ring and perform all-reduce operation. At the moment, the master GPUs get the global aggregation result from all GPUs. Finally, each master GPU broadcasts the global aggregation result to the other local GPUs inside the same machine. In this approach, the master GPUs face a heavy burden while the computation resource of the other GPUs is wasted.

Hierarchical NetReduce, on the contrary, fully utilizes all GPUs. Suppose that a homogeneous distributed system has a total of $P$ GPUs, and each machine is equipped with $n$ ($n \geq 2$) GPUs where $P$ is an integer multiple of $n$. Therefore, the number of machines $H$ equals $P/n$. The process of hierarchical NetReduce is shown in Figure 2(B) which also consists of three phases. In the first phase, NetReduce performs scatter-reduce operation in the intra ring, with each GPU having a partial aggregation result of a different data block (with a size of $\frac{M}{n}$) from any other one in the same machine. In the second phase, the GPUs corresponding to the same data block in different machines form multiple inter rings, performing in-network reduction simultaneously. The number of inter rings equals $n$. At the moment, each GPU has a global aggregation result on a specific data block whose size is $\frac{M}{H}$. In the third phase, NetReduce performs all-gather operation in the intra ring that all GPUs finally obtain the global aggregation result on the data with an amount of $M$. 

Figure 1: Distributed DNN training strategies: (A) ring all-reduce: different nodes receive different unaggregated data from the other node; (B) NetReduce: different nodes receive the same aggregated data from all nodes.

Figure 2: Hierarchical all-reduce: (A) Tencent all-reduce: red and white circles refer to master and slave GPUs, respectively; (B) NetReduce: circles with the same color belong to the same aggregation ring.
In the multi-machines multi-GPUs scenario, the communication time taken by using the flat ring all-reduce algorithm is modeled as

$$T_{fr} = 2(P - 1)\alpha + 2\frac{P - 1}{P} M B_{inter}$$

(4)

where $B_{inter}$ refers to the bandwidth in the inter ring where machines are connected via computer networks such as Ethernet or InfiniBand.

For Tencent all-reduce, consider Rabenseifner’s reduce algorithm [41] and Van de Geijn’s broadcast algorithm [6], and assume $n$ is a power of 2, the communication cost can be modeled as

$$T_{tr} = T_{tr1} + T_{tr2} + T_{tr3}$$

$$= \left[ 2\alpha \log_2(n) + \frac{2(n - 1)M}{n B_{intra}} \right] + \left[ \frac{2(P - 1)}{P} \alpha + \frac{2(P - 1)/n - 1}{P/n} M B_{inter} \right] + \left[ (\log_2(n) + n - 1)\alpha + \frac{n - 1}{n} M B_{intra} \right]$$

$$= \frac{n^2 + 3n \log_2(n) - 3n + 2P\alpha}{n} + \frac{4(n - 1)PB_{inter} + 2(P - n)B_{intra}}{nPB_{intra}B_{inter}} M$$

(5)

where $B_{intra}$ refers to the bandwidth of the intra ring where GPUs are connected via expansion bus such as PCIe or NVLinks.

The communication cost of hierarchical NetReduce is given as

$$T_{nh} = T_{nh1} + T_{nh2} + T_{nh3}$$

$$= \left[ (n - 1)\alpha + (n - 1) \frac{M}{n B_{intra}} \right] + \left( \alpha + \frac{M}{B_{inter}} \right)$$

$$+ \left[ (n - 1)\alpha + (n - 1) \frac{M}{n B_{intra}} \right]$$

$$= (2n - 1)\alpha + \frac{2(n - 1)B_{inter} + nB_{intra}}{nB_{intra}B_{inter}} M$$

(6)

When $n = 1$, $B_{intra} = B_{inter} = B$, Eq. (6) reduces to Eq. (2). Eq. (5) subtracting Eq. (6) gives

$$\Delta T_{tr-nh} = T_{tr} - T_{nh}$$

$$= \left[ \frac{2P/n + 3\log_2(n) - n - 2}{n} \alpha \right] + \frac{(P - n)B_{intra} + 2(n - 1)PB_{inter}}{nPB_{intra}B_{inter}} M$$

(7)

When $P > 3n$, (7) is always larger than 0, considering $n$ is usually no larger than 16.

Eq. (4) subtracting Eq. (6) gives

$$\Delta T_{fr-nh} = T_{fr} - T_{nh}$$

$$= \left[ \frac{2P - 2n - 1}{n} \alpha \right] \frac{+ (P - 2)B_{intra} + 2(n - 1)PB_{inter}}{nPB_{intra}B_{inter}} M$$

(8)

Figure 3: NetReduce protocol: (A) NetReduce header format; (B) an RDMA data message; (C) corresponding packets of the message after segmentation.

Similarly, we can obtain a relaxed sufficient condition from (8) that hierarchical NetReduce outperforms flat ring all-reduce on communication as follows

$$\frac{B_{intra}}{B_{inter}} < \frac{2P}{P - 2} \quad (P > n \geq 2)$$

(9)

4 NetReduce Design

4.1 Network Protocol

A NetReduce protocol is designed to enable the coordination between the end-host and the network switch. The new protocol can be regarded as an L4.5 protocol embedded in the L4 payload. NetReduce uses existing L2/L3 routing protocols to forward packets.

The NetReduce protocol is placed after the IB Base Transport Header (BTH), and the header format is shown in Figure 3(A). The major fields consist of InetTag, RingID, MsgID, MsgLen. InetTag marks the aggregation packet. RingID indicates in which specific ring that the current packet participates. For example, there are multiple rings between different machines in the multi-machines multi-GPUs scenario discussed in §3.2. Only the message with the same MsgID in the same ring from different computing nodes can be aggregated since they contain the same gradient variables at the same neural network layer. MsgLen denotes the number of packets per message after NIC segmentation.

Note that not every aggregation packet contains such a NetReduce header. The NetReduce header is inserted at the beginning of each RDMA message as shown in Figure 3(B). To comply with the Maximum Transmission Unit (MTU) in the Ethernet link layer, a to-be-sent message is segmented into multiple packets by NIC according to the Path MTU (PMTU). Suppose that the size of the message is PMTU+k, the message will then be segmented to $k$ packets as shown in Figure 3(C). Among all the $k$ packets in the message, the NetReduce header only appears in the first one. We do not
modify the segmentation behavior of NIC. For those packets without the NetReduce header, we recover their corresponding NetReduce information which will be described in detail in §4.3.

4.2 Message-Level Flow Control

To prevent buffer overflow, SwitchML sends messages one-by-one, i.e., keeping only one message unacknowledged and sending the next message after receiving the acknowledgment. However, this stop-and-wait transmission makes it difficult to achieve full bandwidth utilization [40]. NetReduce introduces a message-level credit-based flow control mechanism by using a sliding window. The credit is the aggregation result of the previous message. The basic idea is that end-hosts first send \( N \) (refers to the window size) pieces of message concurrently to fully utilize bandwidth. They will not send the \((N + i)^{th}\) message until the aggregation result of the \(i^{th}\) message is received. For example, if \( N = 3 \), end-hosts do not send the \(4^{th}\) messages until the aggregation result of the \(1^{st}\) message is received. Similarly, they can only send the \(5^{th}\) messages until they receive the aggregation result of the \(2^{nd}\) messages and so on.

Algorithm 1 describes the processing algorithm of end-hosts which deals with the message-level data. Basically, the “send-receive” processes appear \( NumMsg \text{-times} \), i.e., every time a node sends out a message it would expect to receive the corresponding aggregation result from all nodes on this message. For each sending, a message, \( msg \), will be assigned a NetReduce header, including \( InetTag \), \( RingID \), \( MsgID \) and \( MsgLen \). The window size, \( N \), can be theoretically calculated based on the buffer size that the switch is able to provide as follows

\[
N \times MsgLen \times pktSize \geq RTT \times PortRate
\]

\[
N \geq \frac{RTT \times PortRate}{MsgLen \times pktSize}
\]

(10)

where \( RTT \) and \( PortRate \) refer to the time taken by completing the transmission of a single packet in the system and the bandwidth of NIC bandwidth at the end-host, respectively.

4.3 In-Network Reduction Accelerator

The in-network reduction accelerator is designed as a middlebox attached to the Ethernet switch which we do not modify. We describe the accelerator architecture in Figure 4. When a packet arrives, a \( Parser \) identifies the aggregation packet or directs the other kinds of the packet to the output port directly. The \( Parser \) further feeds the NetReduce header to a \( State Manager \) which tracks the arrival states of the packets.

A \( Separator \) will separate the protocol headers (including Ethernet, IP, UDP, BTH, and NetReduce) from the payload. The headers are then fed to a \( Header Manager \) which decides on single-switch aggregation or multi-switches aggregation (See §4.5). Once the arrival states of packets from all workers are valid, the \( Aggregator \) begins to sum the payload at the granularity of packets and writes the aggregation result to a buffer which stores the history results. The \( Combinator \) finally merges original headers and updated payload to one complete packet, and sends it out.

### Algorithm 1

The end-host processing algorithm.

**Require:**
- Total number of messages to be transmitted, \( NumMsg \);
- Number of messages per sliding window, \( N \);

1. if \( NumMsg \leq N \) then
2. \( N = NumMsg \);
3. end if
4. /* Send the first \( N \) messages */
5. for \( i \) in 0 : \((N - 1)\) do
6. \( msg.InetTag = InetTag; \)
7. \( msg.RingID = RingID; \)
8. \( msg.MsgID = MsgID; \)
9. \( msg.MsgLen = MsgLen; \)
10. \( msg.Params = Tensor[RingID][MsgID]; \)
11. send(msg);
12. end for
13. /* Send \((N + i)^{th}\) message after \(i^{th}\) message is received */
14. for \( i \) in \( N : (NumMsg - 1)\) do
15. receive(msg);
16. \( Tensor[msg.RingID][msg.MsgID] = msg.Params; \)
17. \( msg.InetTag = InetTag; \)
18. \( msg.RingID = RingID; \)
19. \( msg.MsgID = msg.MsgID + N; \)
20. \( msg.MsgLen = MsgLen; \)
21. \( msg.Params = Tensor[msg.RingID][msg.MsgID]; \)
22. send(msg);
23. end for
24. /* Receive the last \( N \) messages */
25. for \( i \) in 0 : \((N - 1)\) do
26. receive(msg);
27. end for

#### 4.3.1 Header Recovery for Non-First Packets

As mentioned in §4.1, only the first packet in a message contains the NetReduce header due to the NIC segmentation. We propose an algorithm to recover the header information for those non-first packets. NetReduce uses a three-element tuple \( \{SrcIP, DstIP, DstQP\} \) to uniquely determine an RDMA connection where \( SrcIP \) (Source IP Address) and \( DstIP \) (Destination IP Address) are in the IP header, \( DstQP \) (Destination Queue Pair) is in the IB BTH. Since the packets in the same message belong to one single RDMA connection, the non-first packets are thus connected to their first packets via the tuple.

The \( Parser \) maintains a two-level LUT (lookup table) as
shown in Figure 5. LUT#1 and LUT#2 recovers the ring and the message information, respectively. When a first packet marked by InetTag arrives, the Parser locates the end-host in the ring (identified by RingID) by assigning a HostID to the three-element tuple of the packet. Note that the RingID is assigned by end-hosts but the HostID is counted by the switch. Then LUT#1 records the tuple and the corresponding RingID and HostID. The number of entries in LUT#1 is \( n \times H \), where \( n \) is the number of GPUs in a single machine (equals the number of rings performing all-reduce) and \( H \) refers to the number of machines per ring. Since one tuple-defined RDMA connection corresponds to only one ring, the RingID can be recovered solely by the tuple.

Since an RDMA connection may consist of multiple pieces of message, solely using the tuple cannot recover MsgID. To map a packet into a specific message, NetReduce uses Packet Sequence Number (PSN) in the IB BTH and MsgLen in the NetReduce protocol. Suppose the PSN of a first packet in a message is \( PSN0 \), then the PSN of packets with the same tuple falling in the range of \( [PSN0, PSN0 + MsgLen - 1] \) belongs to the same message. LUT#2 records the PSN and MsgLen of the first packets and recovers the MsgID for non-first packets by locating the entry where the \( PSN \) belongs. The number of the LUT#2 entries is \( n \times H \times N \), where \( N \) refers to the sliding window size (number of messages per window). The values of \( n \), \( H \), and \( N \) are determined via the control plane at the job initialization period.

The recovery algorithm works in a lossy network. The RDMA RC mode guarantees strictly ordered transmission. If the first packet is lost or out-of-ordered, the sender retransmits the whole message. The receiver does not receive the packets belonging to the same RDMA connection until the previous lost first packet successfully arrives. The whole recovery algorithm is summarized in Algorithm 2.

Algorithm 2 Recovery algorithm of NetReduce header.

1: if the packet is marked by InetTag then
2: Assign HostID to \([SrcIP,DstIP,DstQP]\);
3: Create entries in LUT#1 and LUT#2, respectively;
4: else
5: if \([SrcIP,DstIP,DstQP] \) has been recorded in LUT#1 previously then
6: Recover RingID and HostID from LUT#1;
7: Recover MsgID from LUT#2 by looking up which range \([PSN0, PSN0 + MsgLen - 1] \) the current \( PSN \) belongs to;
8: else
9: Direct the packet to output port;
10: end if
11: end if

Figure 4: The accelerator architecture of in-network reduction (red and black arrow lines refer to control and data flows, respectively).

Figure 5: A two-level lookup table to recover ring (LUT#1) and message (LUT#2) information, respectively.

\[
\begin{array}{|c|c|}
\hline
\text{Key} & \text{Value} \\
\hline
(SrcIP, DstIP, DstQP), (RingID, HostID) & \cdots \\
(SrcIP, DstIP, DstQP), (RingID, HostID) & \cdots \\
\hline
\end{array}
\]
4.3.2 Aggregation and Dealing with Packet Loss

The accelerator does not start to aggregate gradients until the corresponding packets from all end-hosts arrive. The aggregation packets are aligned with the same RingID, MsgID and PSN offset from PSNO. The State Manager assigns a bit to each packet in the sliding window to indicate the arrival state of the packet, resulting in a bitmap for each ring shown in Figure 6. The bitmap contains packet states in \((N+1)\) pieces of message. When an aggregation packet arrives, the State Manager first locates the specific bitmap based on RingID and then set the state according to the index \([HostID, PSN-PSNO+\((MsgID + 1)%(N+1) - 1\)]\) in the matrix. Once all the elements in a column equal 1, the Aggregator aggregates the corresponding gradients and writes the aggregation result to a history buffer.

When the aggregation completes, the states are not set to 0 immediately. The states of the \(i^{th}\) message cannot be updated until the aggregation results of the message are received by end-hosts (i.e., when the \((N+i)\)th message arrives). Specifically, the State Manager not only sets the state at \([HostID, PSN-PSNO+\((MsgID + 1)%(N+1) - 1\)]\) to 1 but also updates the state at \([HostID, PSN-PSNO+\((MsgID + 1)%(N+1) - 1\)]\) to 0. This is to ensure that a packet state will not be updated before its aggregation result is successfully received by end-hosts. Then the State Manager can identify retransmitted packets by checking the corresponding arrival states in the bitmap. If the value of the state is 1 already, the State Manager knows it is a retransmitted packet. Then the State Manager makes a decision depending on whether this packet has been aggregated previously (i.e., if all elements in the corresponding column equal to 1). If yes, the accelerator replaces the packet payload with the aggregation result in history record and directs it to the output port. On the other hand, if the parameter has not been aggregated, the accelerator simply discards the packet.

4.4 Implementation

We develop a prototype by using a 100 GbE commodity switch for basic forwarding as shown in Figure 7. A self-developed FPGA board with NetReduce capability is attached to the switch. The FPGA board is equipped with a Xilinx Virtex Ultrascale chip [55] which is able to support at most 100 Gbps \(\times 6\).

We configure the switch ACL rules to redirect all RoCE v2 packets to FPGA and forward other packets directly. The FPGA further differentiates the aggregation packets (including the first and non-first packets in an RDMA message) from the other RoCE v2 packets if there exists any. In this way, we do not need to augment the switch capability and a commodity switch would work. The FPGA then processes aggregation packets with the NetReduce logic and send the packets with aggregation results back to the switch. The switch then forwards those packets to proper end-hosts by using existing L2/L3 routing protocols. The switch needs to process the packets twice, thus increasing the latency. Nevertheless, our evaluation shows the additional FPGA operations add less than 3 \(\mu s\) extra RTT compared with that the original RTT is 2 \(\mu s\).

4.5 Extension to Spine-Leaf Topology

In this subsection, we extended the in-network operations from the rack-level cluster to a more general spine-leaf topology as shown in Figure 8. Figure 8 shows an example where packets from 6 workers are aggregated via two-level switches.

The major difference in this topology from the rack-scale aggregation is that NetReduce modifies not only the payload but also the header.

During the job initialization period, an aggregation tree is formed by binding a spine to the leaves. For example, a spine can be selected with the smallest value of IP address. The control plane informs the values of two state variables to the Header Manager (Figure 4) in the leaf: \(LocalSize\) and \(GlobalSize\), which refer to the numbers of local machines under the leaf and global machines in the whole training job, respectively. Specifically, there are two different settings: \(LocalSize = H = GlobalSize\) and \(LocalSize = H < GlobalSize\) for only Top-on-Rack (ToR) switch aggregation and two-level switches aggregation, respectively. The operation process of the Header Manager is described in Algorithm 3.

Lines 1 to 5 in Algorithm 3 apply to the leaf switch only, which differentiate the ToR aggregation and the
Algorithm 3 Processing algorithm of Header Manager.

1: if $\text{LocalSize} == \text{GlobalSize}$ then
2:     Does not change the packet headers;
3: else if $\text{LocalSize} < \text{GlobalSize}$ then
4:     Send the packet headers to the destination leaf;
5:     Change the original $[\text{SrcMAC}, \text{DstMAC}, \text{SrcIP}, \text{DstIP}]$ to $[\text{SrcMAC}_{\text{leaf}}, \text{DstMAC}_{\text{spine}}, \text{SrcIP}_{\text{leaf}}, \text{DstIP}_{\text{spine}}]$;
6:   end if
7:   if $[\text{DstMAC}, \text{DstIP}]$ belongs to the switch itself then
8:     For spine, swap $[\text{SrcMAC}_{\text{leaf}}, \text{SrcIP}_{\text{leaf}}]$ and $[\text{DstMAC}_{\text{spine}}, \text{DstIP}_{\text{spine}}]$;
9:     For leaf, replace the headers with the ones previously stored based on DstQP and PSN;
10:  end if

of changing headers are triggered by detecting whether the destination address belongs to the switch itself.

5 Evaluation

5.1 Methodology

We compare the proposed NetReduce with ring all-reduce and SwitchML. The ring all-reduce is implemented by NCCL-2.4.7 [34], a commonly used collective communication library for distributed DNN training, while SwitchML is implemented by using a programming switch equipped with a Tofino chip. We modify the primitive in NCCL-2.4.7 and create a new GenericOp to comply with the NetReduce function.

In multi-machines single-GPU scenario, we use 6 servers. Each server is equipped with two 10-cores CPUs (Intel Xeon E5-2664 2.4 GHz), 32 GB*3 DDR4 memory, one NVIDIA Geforce RTX 2080 8 GB GPU [33], and a Mellanox ConnectX-5 [32] 100 GbE NIC. Multi-machines multi-GPUs, we use 4 servers. Each server is equipped with two 18-cores CPUs (Intel Xeon Gold 6154 3.00 GHz), 1 TB (64 GB*16) DDR4 memory, eight NVIDIA Tesla V100 SXM2 32 GB GPUs [37] and a Mellanox ConnectX-5 100 GbE NIC. A hybrid cube-mesh network topology [35] is used for 8-GPU interconnection via NVLink [36] inside each single machine.

We evaluate the systems in typical image training workload, ImageNet [12]. Three representative Convolutional Neural Network (CNN) models are chosen: AlexNet [27], VGG-16 [49], and ResNet-50 [21]. We leverage Horovod-0.16.0 [46] to support TensorFlow-1.12.0 [52]. We also evaluate NetReduce on NLP tasks by using PyTorch-1.5.1 [1]. We pretrains transformer-based models (BERT [13] and GTP [42]) and fine-tunes the model for GLUE [54] and SQuAD [43] tasks by using the approach provided in [48] and [22], respectively. In the experiments, the sliding window size $N = 2$, the message size is 170 KB, and each packet delivers 1 KB of payload data.

5.2 Multi-Machines Single-GPU Scenario

We plot the speedup of in-network aggregation over ring all-reduce by using 6 GeForce RTX 2080 GPUs in Figure 9, where the image training throughput of SwitchML and NetReduce is normalized to that of ring all-reduce. SwitchML improves the baseline on the three models by 17.5%, 14.4%, and 4.4% respectively while the percentages by using NetReduce are 45.0%, 20.2%, and 4.9%, respectively. The larger performance gain of NetReduce than SwitchML mainly comes from two points: processing full-length Ethernet frame by using FPGA and offloading the network stack processing to RDMA NIC. However, NetReduce and SwitchML have similar performance on ResNet-50. This is due to that the end-to-end throughput depends on how much computation and communication overlap. In computation-intensive models such as two-switches aggregation. For the latter case, in the upstream flow, the leaves first send the packet headers to the destination leaf as shown in Figure 8(A). L1, L2, and L3 store the headers of (W6→W1,W1→W2), (W2→W3,W3→W4), (W4→W5,W5→W6), respectively. These headers are used by the leaves to distribute packets back to workers in the downstream flow. Then the leaves send the local aggregation results to the spine with source and destination addresses replaced by the ones of the leaves themselves and the spine, respectively, as shown in Figure 8(B). In the downstream flow as shown in Figure 8(C), the spine swaps source and destination addresses and sends the packets with global aggregation results to the leaves. The leaves replace the headers with the previously stored ones and send the whole packets to the workers. These actions
Table 1: Training performance per GPU with BS=32, FP16 by using 4 NVIDIA Tesla V100.

| Model   | Throughput (images/s) | Iteration (ms) | Communication (ms) |
|---------|-----------------------|----------------|--------------------|
| AlexNet | Ring all-reduce       | 527.9          | 60.62              | 47.12(77.7%)     |
|         | NetReduce ↑           | 716.0          | 44.69              | 31.10(69.6%)     |
|         |                       | 35.6%          | 26.3%              | 34.0%            |
| VGG-16  | Ring all-reduce       | 172.9          | 185.08             | 111.98(60.5%)    |
|         | NetReduce ↑           | 215.3          | 148.63             | 74.64(50.2%)     |
|         |                       | 24.5%          | 19.7%              | 33.3%            |
| ResNet-50| Ring all-reduce     | 358.8          | 89.19              | 23.04(25.8%)    |
|         | NetReduce ↑          | 383.6          | 83.42              | 19.29(23.1%)    |
|         |                       | 6.9%           | 6.5%               | 16.3%            |

As shown in Figure 10(A), NetReduce always trains images faster than ring all-reduce for both FP32 and FP16 cases. When increasing the BS, the absolute improvement of throughput first increases and then decreases after passing some certain thresholds in the models as shown in Figure 10(B), except AlexNet. This is because AlexNet is a communication-intensive model and has less requirement of GPU memory than the other models. For AlexNet, GPU can consume more data which means the “up-down” phenomenon would occur beyond BS=256.

In Figure 10(B), using FP16 gives larger absolute improvement than FP32. This is because FP16 takes less computation time than FP32, reducing the overlap between communication and computation. Therefore, the benefits brought by NetReduce based on the reduction of communication time becomes more obvious. Take BS=32 with FP16 as an example and summarize the training performance in Table 1. Among the models, NetReduce improves AlexNet on the throughput by 35.6%, which is the most. This is because when using ring all-reduce, the communication accounts for 77.7% (=47.12/60.62 as shown in the 5th column in Table 1) of the whole iteration time, which has a significant potential to improve. On the contrary, although VGG-16 is improved on communication by 33.3% which is similar to AlexNet (34.0%), the communication accounts for 60.5% which is smaller than AlexNet, resulting in a less improvement on throughput (24.5%). For ResNet-50 which is a computation-intensive model, with 16.3% improvement on the communication which accounts for only 25.8% of the iteration time, we have 6.9% improvement on the throughput.

Convergence with fixed-point arithmetic. Typically, the end-host aggregates parameters by using floating-point numbers but most current commodity switches only support fixed-point arithmetic, which may vanish parameters during the training process. Our developed FPGA board indeed can support both floating-point and fixed-point arithmetic and we are interested to explore whether NetReduce with fixed-point arithmetic would impact the training convergence. We convert the floating-point parameters to the fixed-point ones in end-hosts by keeping the original significant digits of the parameters.
We explore the absolute loss difference between NetReduce with fixed points and ring all-reduce with floating points, and developed a metric, $\frac{|\text{LOSS}_{\text{net}} - \text{LOSS}_{\text{ring}}|}{\text{LOSS}_{\text{ring}}}$, as shown in Figure 11. Despite the initial value, the loss difference accounts for no more than 0.01% of the baseline for AlexNet and VGG-16. ResNet-50 seems to be more sensitive to fixed-point arithmetic and the loss difference vibrates during the training process. Nevertheless, the largest loss difference accounts for less than 0.08% of the baseline. Therefore, we can conclude that NetReduce operation with fixed-point arithmetic does not impact the training convergence.

Models other than CNN. Besides CNN models, we also use NetReduce to pretrain and fine-tune transformer-based models for NLP jobs. We pretrain the famous BERT and GPT-2 and further fine-tunes BERT for tasks including the General Language Understanding Evaluation (GLUE) and Stanford Question Answering Dataset (SQuAD). The GLUE is a collection of tasks for evaluating natural language understanding systems. We select three corpora for the evaluation of NetReduce, MNLI, QNLI, and QQP. The SQuAD is a reading comprehension dataset for question answering, combining the 100,000 questions with over 50,000 unanswerable questions. The speedup of NetReduce over ring all-reduce on the tasks is shown in Figure 12, where NetReduce improves BERT pretraining, GPT-2 pretraining, GLUE-MNLI, GLUE-QNLI, GLUE-QQP, and SQuAD by 34.6%, 24.8%, 27.3%, 29.6%, 22.2%, and 42.5%, respectively.

5.3 Multi-Machines Multi-GPUs Scenario

In this scenario, 4 machines equipped with 8 Tesla V100 GPUs respectively are used. We compare the training performance of hierarchical NetReduce (HN) with that of flat ring all-reduce (FR) and Tencent all-reduce (TA) as shown in Figure 13. Various BSs are chosen: 32, 64, 128, and 256. The absolute improvement pattern in Figure 13(B) is similar to that in Figure 10(B). To sort the algorithms by training speed from fast to slow, we have the following ranking: hierarchical NetReduce, Tencent all-reduce, and flat ring. The training performance using BS=32, FP16 is summarized in Table 2. Hierarchical NetReduce improves flat ring by 68.8%, 50.7% and 15.1% for AlexNet, VGG-16, and ResNet-50, respectively. Compared with Tencent all-reduce, hierarchical NetReduce speeds up training by 57.9%, 42.1% and 12.3% for the three models respectively.

It is reported in [23] that Tencent hierarchical algorithm only brings performance gain for tensors with smaller sizes. For relatively larger tensors, the flat ring algorithm still out-
performs the hierarchical algorithm. Recall in §3.2, the communication cost consists of two items: message processing latency item with $\alpha$ and tensor transmission item with $M$. The $\alpha$ item is mostly affected by the number of GPUs participating in training, $P$. With increased $P$, the $\alpha$ item accounts for a larger proportion in flat ring all-reduce, resulting in poor scalability. Hierarchical approaches reduce the impact of $\alpha$ item by dividing a big ring into multiple small intra rings, improving the scalability. Therefore, for small tensors where the $\alpha$ item accounts for most communication costs, hierarchical approaches give superior performance. However, for big tensors where the $M$ item accounts for most communication costs and the system becomes less sensitive to $P$, hierarchical approaches bring fewer benefits.

Nevertheless, when the bandwidth of intra and inter rings fulfill certain conditions, hierarchical approaches can outperform the flat ring regardless of tensor size. Specifically, hierarchical NetReduce would always outperform flat ring if condition (9) holds. Considering our hardware prototype, substituting $P=32$ and $n=8$ into (9) gives $B_{\text{intra}} \geq 2.3$. Indeed intra and inter nodes being connected via NVLink and 100GbE, gives $B_{\text{intra}} = 150$ GB/s and $B_{\text{inter}} = 12.5$ GB/s, respectively. Therefore, in our hardware prototype, $\frac{B_{\text{intra}}}{B_{\text{inter}}} = 12 > 2.3$. In the next subsection, we will further explore different ratios of intra and inter rings bandwidth in the situation involving up to thousands of GPUs.

5.4 Large-Scale System Simulation

Recall Eqs.(4) to (8) back in §3.2, the major factors affecting communication cost includes processing latency per message ($\alpha$), tensor size ($M$), number of GPUs ($P$), intra ring bandwidth inside one single machine ($B_{\text{intra}}$). We conduct simulations on these metrics to explore what effects they would bring to the system.

The simulation results are shown in Figure 14, where $n = 8$ and $B_{\text{intra}} = 12.5$ GB/s by using 100 GbE NIC. $B_{\text{intra}}$ are chosen from 15.75 GB/s (PCIe) to 150 GB/s (NVLink). Figure 14(A), (B), and (C) show the result of communication time vs. $M$, $P$, and $\alpha$, respectively. As expected, when increasing $B_{\text{intra}}$, hierarchical NetReduce consumes less time as shown in Figure 14, leading to larger throughput gain. However, the gain does not always rise that fast. It saturates when hitting a certain threshold of the bandwidth, e.g., increasing $B_{\text{intra}}$ from 100 GB/s to 150 GB/s does not bring that much benefit as increasing from 50 GB/s to 100 GB/s, as shown in Figure 14(A) and (B).

In Figure 14(A), $P$ and $\alpha$ are fixed to 2048 and 1 $\mu$s respectively. When $B_{\text{intra}}=15.75$ GB/s, hierarchical NetReduce is only better than flat ring all-reduce for tensors smaller than a threshold around 130 MB. This is consistent with the observation reported in [23] that the benefit brought by hierarchy cannot cover the tensor transmission cost of a relatively larger $M$. Nevertheless, this can be indeed overcome by increasing the value of $B_{\text{intra}}$, e.g., to 50 GB/s, 100 GB/s, and 150 GB/s as shown in Figure 14(A) (See the explanation in §5.3).

The communication cost of hierarchical NetReduce is independent of $P$ as shown in Figure 14(B), where $M$ and $\alpha$ are fixed to 250 MB and 1 $\mu$s respectively. Flat ring all-reduce takes more latency when more GPUs participating in the training job as increased $P$ leads to a higher number of transmissions. On the contrary, communication time in NetReduce is a constant regardless of the value of $P$. Similarly, as shown in Figure 14(C), flat ring all-reduce is more easily affected by increased $\alpha$. This is because the coefficient $2(P-1)$ amplifies the impact of $\alpha$ (Eq.(4)) while NetReduce reduces $2(P-1)$ to 1 (Eq.(6)).

In summary, hierarchical NetReduce can cover the transmission cost of large $M$ by using larger intra bandwidth. With increased $P$ and $\alpha$, hierarchical NetReduce shows better scalability than flat ring all-reduce as the performance of NetReduce is independent of the number of GPUs.

6 Conclusion

In this paper, we present NetReduce, a novel RDMA-compatible in-network reduction architecture to accelerate distributed DNN training. Compared with existing designs, NetReduce maintains reliable connections between end-hosts in the Ethernet to avoid implementing high-cost network protocol stack in the switch. The prototype implemented by using FPGA is an out-of-box solution without modifying commodity devices such as NICs or switches. NetReduce improves the training up to 1.7x and 1.5x for CNN-based CV and transformer-based NLP tasks, respectively. We find that NetReduce with fixed-point arithmetic does not impact the training convergence. Simulations on large-scale systems indicate the superior scalability of NetReduce to the state-of-the-art ring all-reduce.
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