Effect of physical parameters on the drain characteristics of Double gate MOSFET incorporating Quantum Mechanical Effects

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Abstract. Scaling of bulk MOSFETs in nanometre regime has several disadvantages. The electrical behaviour of the devices doesn’t show the anticipated characteristics if scaling is done beyond certain point. But in order to have smaller devices with higher density on chips, it is necessary to avoid short channel effects (SCE) which lead to unexpected electrical features. One of the methods to avoid SCE is to have multi-gate architecture of MOSFET. This paper investigates the behaviour of double-gate MOSFETs with respect to the variation of their physical dimensions. The analyses have been done taking into notice the quantum mechanical effects due to dimensions in nanometre scale. The results obtained highlight how subthreshold and above threshold regions are impacted due to the various physical quantities that have been varied.

1. Introduction

By reducing the dimensions of MOSFETs, more number of components can be incorporated on a VLSI [1, 2] chip to have diversified applications. Adjusting short-channel effects (SCE) is the major issue during scaling down of conventional MOSFETs. There are several ways through which SCE can be lessened while reducing the dimensions of a device. There are many prominent techniques to overcome these shortcomings. Use of strain as reported in [3-5] alleviates SCE and boosts electrical integrity. Similar advantages have been found through the use of junctionless transistors [6-8]. Use of multiple gates has been reported in [9-12]. The core theme of all these methods is to enable gate electric field to be more dominant in the channel region. Proper lithographic techniques are used to enable these methods.
In multi-gate MOSFETs, there is more than one gate and all gates are maintained at the same potential through the application of gate voltage. The role of gate is to govern the electrons in the channel. Due to multi-gate, the channel electrons are better controlled [13] and exhibit superior properties than single gate transistors.

In this work the electrical behaviour of Double-Gate (DG) MOSFET as shown in figure 1 has been examined by varying the physical parameters of the device. The subthreshold characteristics denote the region of MOSFET operation when gate voltage is smaller than the required turn-on voltage. Subthreshold region determines the power consumption of the device when it is supposedly in off state. In the nanometre range, the energy levels redistribute and it impacts the threshold voltage of the given device. In our calculations we have taken into this consideration which is known as quantum mechanical effect (QM) [14].

2. Theoretical details

The potential in the channel and its charges are related through the Poisson expression written as
\[ \frac{d^2 \phi}{dx^2} = \frac{q}{\varepsilon_{Si}} n_i e^{\frac{\phi - V}{kT}} \]
where \( \phi \) is the potential in the channel, \( q \) is charge, \( \varepsilon_{Si} \) is the silicon permittivity, \( n_i \) is the doping concentration, \( V \) is the quasi-Fermi potential, and \( kT/q \) is the thermal potential. The solution of this equation can be found using boundary conditions [15]

\[ \frac{q(V_g - \Delta \phi - V)}{2kT} - \ln \left( \frac{2}{t_{Si}} \sqrt{\frac{2e_{Si}kT}{q^2 n_i}} \right) = \ln \beta - \ln(\cos \beta) + \frac{2e_{Si} t_{ox}}{e_{ox} t_{Si}} \beta \tan \beta \]

(1)

The drain current expression is given as [16]

\[ I_{ds} = \mu \frac{W}{L} \int_{0}^{V_d} Q(V) dV \]

(2)

The current in the linear, saturation and subthreshold regions are given as [15]

\[ I_{ds, Lin} = 2\mu C_{ox} \frac{W}{L} \left( V_g - V_t - \frac{V_{ds}}{2} \right) V_{ds} \]

(3)

\[ I_{ds, Sat} = \mu C_{ox} \frac{W}{L} \left( V_g - V_t \right)^2 - \frac{8r_k^2 T^2}{q^2} e^{\frac{V_{ds} - V_t - V_{th}}{kT}} \]

(4)
\[ I_{ds,\text{Sub}} = \mu \frac{W}{L} kT n_i^* e^{q(V_g - \Delta \phi) / kT} \left( 1 - e^{-q(V_g) / kT} \right) \]  

(5)

where \( \mu \) is the mobility, \( C_{ox} \) gate oxide capacitance, \( W \) is channel width, \( L \) is channel length, \( V_g \) is applied gate voltage, \( V_{ds} \) is drain to source applied voltage and threshold voltage \( V_t \) is expressed as [15]

\[ V_t = \Delta \phi + \frac{2kT}{q} \ln \left[ \frac{2}{t_{Si}} \left( \frac{2e_S^0 kT}{q^2 n_i^*} \right) + \frac{2kT}{q} \ln \left( q \frac{(V_g - V_0)}{4rT} \right) \right] \]  

(6)

where \( \Delta \phi = \phi_m - \phi_s \), the difference of metal and semiconductor work function, \( t_{Si} \) is channel thickness, and \( r = \varepsilon_{Si} t_{Si} / \varepsilon_{ox} t_{Si} \). Due to QM effect, the increase in threshold voltage is given as [17]

\[ \Delta V_{th} = \left( \frac{h^2}{4q m^* t_{Si}^2} \right) \left( \Delta t_{Si} / t_{Si} \right) \]  

where \( h \) denotes Planks constant and additional symbols have traditional implications.

3. Results and Discussion

The calculation results are presented in Fig. 2–7. The channel length used is 1 \( \mu \)m and oxide thickness as 1.5 nm for all calculations otherwise it has been stated.

**Figure 2.** Drain current versus gate to source voltage for different oxide thickness.

Fig. 2 shows the variations of current with respect to applied gate voltage for different gate oxide thickness. The oxide thickness has been varied from 1.5 nm to 4.5 nm. The effect of oxide thickness variation is negligible in subthreshold region while it considerably affects the above threshold region. In Fig. 3, silicon channel thickness has been changed to get the current variation. Here \( t_{Si} \) affects subthreshold characteristics more than above threshold and it is as per the observations in [15]. The channel thickness near 5 nm contributes more to the elevation in threshold voltage arising due to QM effect.
The effect of change of channel width on the drain current is shown in Fig. 4. Current increases with width $W$. In this case, $W$ has relatively more effect on above threshold area. Drain current can be increased by increasing $W$, but then it increases the size of the device.

The outcome of altering the doping concentration can be seen from Fig. 5. Increase in doping raises the work function of silicon and in subthreshold region current increases.

By changing the metal work function, desired threshold voltage can be obtained and accordingly the drain current is also affected. It can be observed from figure 6 that metal work function affects both
the regions of MOSFET operation. Threshold voltage decreases if metal work function is decreased. But one of the disadvantages is that smaller metal work function increases subthreshold current and hence the leakage current. Leakage current must be kept at minimum level. From this graph the optimum value of metal work function can be inferred.

![Figure 6](image)

**Figure 6.** Drain current versus gate to source voltage for different metal work function.

The effect of mobility on current can be visualized from Fig. 7. Mobility shows more impact in the above threshold area. Therefore techniques that increase mobility may be incorporated in DG MOSFETs to increase drain current.

![Figure 7](image)

**Figure 7.** Drain current versus gate to source voltage for different mobility.

4. **Conclusion**

In this work the sensitivity of drain current of DG MOSFET for device dimension changes have been explored. It may be concluded that constraints exist for the selection of proper parameter so as to get maximum current and minimum dimension. Subthreshold current determines the off-state of the device and therefore it should be as low as possible. In the on-state, i.e., when the gate voltage is greater than the threshold voltage, larger current is expected. Selection of metal gate work function also plays very important role in the optimum performance of the device. As a future work, the effect of variation of channel length would be explored.

5. **References**

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