Medium Voltage Flying Capacitor DC–DC Converter
With High-Frequency TCM-Q2L Control

Rafał Kopacz ©, Student Member, IEEE, Michał Harasimczuk ©, Przemysław Trochimiuk ©, Student Member, IEEE, Grzegorz Wrona ©, and Jacek Rąbkowski ©, Senior Member, IEEE

Abstract—This article presents a novel control method for a multilevel dc–dc flying capacitor converter for applications in medium voltage range. Quasi-two-level modulation provides the possibility to obtain low flying capacitance even below 1 µF, whereas the triangular current mode controller part enables to achieve zero voltage switching at turn-on for a wide operating range, lowering power losses, and providing the possibility to operate at higher frequencies. The proposed novel control converges the advantages of these both methods leading to very high efficiency with high power density. Performance of the flying capacitor converter with the proposed control method is illustrated with a model-based Saber simulation at first, and then, an experimental model operating at wide frequency range (40 ÷ 250 kHz) and in medium voltage range was designed and constructed. A series of laboratory tests at up to 1.5 kV dc and 10 kW confirmed the noteworthy characteristics of the converter. The voltage between the power devices is balanced and the efficiency achieved reached as high as 99.1%. Therefore, the proposed converter can be competitively employed against classical two-level, as well as three-level and series connection-based counterparts.

Index Terms—Dc–dc power conversion, power converter, power electronics, power MOSFETs, silicon compounds, voltage control.

I. INTRODUCTION

IN THE recent years, the environmental requirements to limit the fossil fuel usage and its consequences demand worldwide employment of RES and further improvements in the department of electrical energy conversion, especially in terms of efficiency, power density and cost. In order to achieve these prerequisites, extension to MV range for these systems has been suggested as a prominent solution [1], [2] that is intensively studied by researchers and have already been utilized in the industry. The main applications for dc–dc converters in this voltage range include: dc microgrids for future energy distribution systems as well as for EV charging stations [3]; auxiliary traction converters; and, finally, PV applications [4], [5], which have also adopted 1.5 kV dc voltage rating [6]. Furthermore, some applications in the MV range may additionally require the possibility to convert the energy bidirectionally, such as in ESS, which are vastly used nearly in every type of microgrids. Therefore, there is a great need to provide highly-efficient and low-cost dc–dc converters within the MV level so that all the advantages of this voltage range could be fully utilized.

The main challenge in terms of low-loss MV dc–dc converter construction and design is nested within the core component of each power electronics system, the power switch. In the low voltage area SiC power devices, in particular SiC MOSFETs [7], have already been successfully adopted as they are characterized by superior performance in comparison to standard Si counterparts, especially in regard to high switching speed and low power loss [8], [9]. However, when MV range is considered the blocking voltage of SiC power transistors, even if notably higher than its Si MOSFET equivalents, still is not sufficient for direct application in MV converters, as the widely used Si IGBTs that can reach as high as 6.5 kV. This is an issue, as even though power semiconductor devices with blocking voltages at 10 kV have been presented, their use is still restrained due to complications in regard to driving circuitry, reliability, and very high cost [10]. Moreover, alas, the commonly-available SiC MOSFETs are still limited to just 1.2–1.7 kV. Hence, in order to apply the vast benefits of SiC power devices in MV power converters more sophisticated approach to power switch utilization has to be employed. One method to achieve this is to use multilevel topologies, which in general provides low device voltage stress, low harmonic, and high power capability [11], [12]. Nevertheless, another classic approach in the form of series connection of power devices is very well known as well and, in general, provides superior efficiency and lower cost with limited number of elements [13]. However, since voltage imbalances among the series connected power devices occur, mainly due to mismatches in device parameters and driving circuits [14], in order to operate properly, the final systems require further attention in the form of supplementary voltage balancing circuits, such as passive snubbers [15], or active driving methods [16], [17], which lead to enlarged cost and complexity of the system [18], diminishing some of the advantages in comparison to multilevel topologies. Thus, so that the combination of the best features of these two approaches can be utilized, Q2L approach, presented in [19]–[22], is considered beneficial as it provides the possibility to execute series connection using basic multilevel
topology—by employing a significantly reduced flying capacitor for minimal amounts of time, just to balance the voltages between the devices. Hence, series-connection-like performance can be reached, using a simple control system and well-known topology with only one additional component.

Since dc–dc converters have been widely used for many years a large variety of topologies and approaches have been presented in the literature [23], also specifically in regard to bidirectional systems [24]. When nonisolated topologies are considered, which are the most common in RES and ES systems, applied in MV range, multilevel [25]–[27], switched capacitor [28], and interleaved [29], [30] systems appear to be one of the most common solutions since they are characterized by high blocking voltage and high power capabilities along with limited power losses. Furthermore, since efficiency is key, especially for higher power systems, approaches utilizing ZVS or ZCS are also often considered as in [31]. However, such converters usually require supplementary circuits, resulting in higher component count, or more advanced control patterns. Furthermore, resonance-based converter topologies are often bound to one operating point, thus, noteworthy efficiencies cannot be reached for wide load range and/or transformation ratios.

In this article, a novel TCM-Q2L control method for a well-known three-level FCC [32]–[34] is proposed. It is based on the convergence of Q2L approach [19]–[22], and TCM [35]–[38] providing the possibility to achieve ZVS at turn-ON for all power transistors without any auxiliary circuits. The converter with the proposed control pattern can be competitively employed in MV range in comparison to other approaches. In particular, when compared with standard two-level dc–dc converters lower stresses are achievable and lower-rated power devices may be applied (1.2 kV SiC MOSFETs for 1.5 kV voltage in this case). Moreover, in contrast to standard approach to series connection the need to employ supplementary voltage compensation methods is omitted, as the balancing is guaranteed with the use of the flying capacitor. Finally, when comparison with classic three-level dc–dc topologies is considered, the converter with the proposed control method is identified by significantly lower volume of the flying capacitor due to the Q2L modulation and higher possible frequencies through the use of the TCM control. Moreover, when high-power systems are considered, the efficiency of the proposed system can reach or even surpass conventional 3L and 2L systems and is comparable both in terms of efficiency and power density with 3L-operated TCM-based converters. Furthermore, the proposed converter is capable of operation in a wide load and voltage gain range.

The rest of this article is organized as follows. A list of abbreviations and symbols used is shown in Table I. After a brief introduction showcasing other solutions for dc–dc converters in MV range, in Section II, operation principles of the converter are shown and described, including basic FCC operation, flying capacitor voltage balancing and, finally, Q2L and TCM control description and synthesis. Furthermore, in Section III, simulation study of the converter is shown. Design and practical issues of constructing a prototype model of the proposed converter are shown in Section IV, whereas the experimental validation of the noteworthy characteristics of the proposed system are presented in Section V. A comparison is given in Section VI. Finally, Section VII concludes this article. It is confirmed that the proposed TCM-Q2L control method for a 3L FCC provides a possibility to construct highly efficient dc–dc converters with low passive component volume that is comparable or even surpasses conventional and state-of-the-art solutions in this power/voltage range in terms of performance. This article is an extension of...
be elaborated on further in the article. The inductor voltage in supplementary states is variable, depending on current circuit state, and equal to either \( V_H \), \( V_{FC} \) or 0.

**B. TCM-Q2L Operation**

In a conventional approach to dc–dc FCC control the 3L states F1 and F2 (see Table II) are employed for a considerable amount of time in order to provide the third level of the \( v_M \) voltage and reduce \( di/dt \) stress of the inductor. Thus, the required capacitance and, in consequence, the total volume of the flying capacitor have to be relatively high. Using the converter with Q2L control these states are mainly used so that the voltages across the transistor pairs \( (T_{H1}/T_{H2}) \) and \( (T_{L1}/T_{L2}) \) can be balanced through the flying capacitor. Therefore, since the 3L times are much shorter, resulting in shorter spans of time in which the capacitor \( C_F \) conveys the current, the capacitance and its current stress can be substantially reduced in comparison to the standard 3L approach.

In order to describe the Q2L operation more clearly level ratio \( D_{LVL} \), describing the relation between the 2L and 3L operation is introduced as in (1), where \( t_{B1} \) and \( t_{B2} \) are the times of the basic two-level states B1 and B2 shown in Table II and \( T_S \) is the switching period (transition DT states are omitted)

\[
D_{LVL} = \frac{t_{B1} + t_{B2}}{T_S}. 
\]

For 2L mode, since the 3L states are only used for a brief amount of the whole cycle, just to sustain constant voltage equal to \( V_H/2 \) on the flying capacitor, the ratio \( D_{LVL} \) is close to unity (in the prototype \( D_{LVL} > 0.99 \)), which will be elaborated on further in the article.

When we consider the most basic approach the Q2L modulation pattern only employs the switching states (B1, B2, F1, and F2). However, in an actual real-life system, in which switching time delays have to be considered, the inclusion of supplementary transition states (DT1-4) in order to protect the transistors from short-circuiting via the flying capacitor is necessary. Each of the DT states represents a situation in which only one transistor is turned-on at a time and it is required, for safety measures, to apply the corresponding DT state in between every state change. Normally, the length of these states \( T_{DT} \) is set arbitrarily at a constant value so that safe switching conditions are acquired. However, when MOSFETs are employed as the power devices, carefully choosing the minimum time of these states can be further employed in order to assure ZVS at turn-on for all the transistors by proper manipulation of the length of the converter states and the switching frequency. In order to achieve ZVS at turn-on for all voltage gains, the control method is described for both \( G_V \geq 0.5 \) (mode A) and \( G_V \leq 0.5 \) (mode B), where \( G_V \) is the voltage gain of the converter \( (G_V = V_L/V_H) \), as the current values at which the switching processes occur are different for each mode. Moreover, since DT states, depending on the circuit state, can be used to employ the flying capacitor and balance the voltage among the transistor pairs, in the theoretical analysis the use of states F can be omitted in an ideal case \( (D_{LVL} = 1) \).

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**II. TCM-Q2L CONTROL FOR DC–DC FCC**

**A. Basic FCC Operation Principles**

The topology is a classic three-level flying capacitor leg applied in a direct dc–dc converter, as shown in Fig. 1. The converter can operate bidirectionally with the proposed control method. However, for the sake of simplicity, in this article, only buck mode is considered in regard to the theoretical analysis, as well as to the experimental verification.

The switching states of the converter are presented in Table II. States B1 and B2 are used in regard to 2L operation in which the inductor voltage drop is the same as in a classic 2L buck converter, whereas states F1 and F2 correspond to the 3L states employing the flying capacitor. Furthermore, supplementary switching states DT1 to DT4 can be also employed as transitions in-between other converter states. Evidently, in order to use the 3L states as intended, the voltage at the flying capacitance \( V_{FC} \) has to be kept constant and equal to \( V_H/2 \). Therefore, special measures to balance the voltage have to be applied, which will

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**Fig. 1.** Scheme of a three-level dc–dc FCC in buck mode

![Diagram](image-url)
To explain the idea of TCM in this converter transistor switching states and an exemplary modulation pattern of one of the two sequences with the proposed control method converging TCM and Q2L and focusing on transition between states B2 – F1 – B1 will be considered - see Figs. 2 and 3 for mode A ($G_V \geq 0.5$) and Figs. 4 and 5 for mode B ($G_V \leq 0.5$). In these figures two of the zoomed patterns [see Figs. 3(b), (c) and 5(b), (c)] are shown for theoretical analysis ($D_{LVL} = 1$), whereas the other two [see Figs. 3(d) and (e) and 5(d) and (e)] are presented in regard to a situation in which additional F states are used for flying capacitor voltage balancing purposes – (d) low current transition and (e) high current transition.

In order to simplify the circuit analysis constant voltage equal to half of the input voltage on output and flying capacitor during one switching period is assumed. Voltage drop on conducting diodes and transistors, as well as parasitic parameters, except for transistor output capacitances as these are crucial in order to explain the soft-switching mechanism in the proposed converter, of all components, as well as the turning time of switches, are omitted. Furthermore, transistor output capacitances $C_{OSS}$ are assumed constant and equal for all the switches.

The thought process for all the equations for all the intervals is as follows: the system consists of a resonance circuit containing the inductor $L$ and two parallel-connected transistor output capacitances $2C_{OSS}$ (e.g., $C_{OSS(TH1)}$ and $C_{OSS(TL2)}$, where...
\( C_{OSS(TH1)} = C_{OSS(TL2)} = C_{OSS} \). Thus, resonance impedance \( Z \) and resonance angular frequency \( \omega_r \) can be described as follows:

\[
Z = \sqrt{\frac{L}{2C_{OSS}}}
\]

\[
\omega_r = \frac{1}{\sqrt{2LC_{OSS}}}
\]

The said resonant circuit is supplied by the main capacitors of the system \( C_H, C_L, C_F \), which are assumed to have constant voltage and are equal to, subsequently, \( V_H, V_L, V_F \). Thus, an equivalent circuit, consisting of inductance \( L \), capacitance \( 2C_{OSS} \) and, depending on the specific interval, a combination of capacitances modelled as constant voltage sources \( (V_H, V_L, V_F) \), can be derived and then used to describe the inductor current, and the duration of a specific interval as further shown in the Section.

Interval 1 \((t = 0 \rightarrow t_1)\), Figs. 2(a), 3(b) (mode A); 4(a), 5(b) (mode B):

In the time before the considered interval transistors \( T_{L1} \) and \( T_{L2} \) are turned ON and conduct, whereas transistors \( T_{H1} \) and \( T_{H2} \) are turned OFF. At time \( t_0 \) inductor current \( i_L \) is equal to zero.

In mode A, at time \( t_0 \) transistor \( T_{L2} \) is turned-ON and the resonant operation starts between inductor \( L \) and output capacitances \( C_{OSS(TH1)} \) and \( C_{OSS(TL2)} \). During this interval capacitance \( C_{OSS(TH1)} \) is discharging and capacitance \( C_{OSS(TL2)} \) is charging. Inductor current in the considered interval can be described by the following equation:

\[
i_{L(A)}(t) = -\frac{V_L}{Z} \sin(\omega_r t).
\]

In mode A, the interval ends when capacitance \( C_{OSS(TH1)} \) is fully discharged, which allows to turn-on transistor \( T_{H1} \) at zero voltage. On the basis of (4) the duration of the interval can be calculated

\[
t_{1(A)} - t_0 = \cos^{-1}\left(\frac{G_V - 1/2}{G_V}\right) \frac{1}{\omega_r}.
\]

Unlike in mode A, in mode B transistor \( T_{L2} \) is turned-OFF at current lower than zero. Thus, for this mode, the interval starts when inductor current \( i_L \) reaches zero, while both \( T_{L1} \) and \( T_{L2} \) are still ON. Inductor \( L \) current is this interval is given by

\[
i_{L(B)}(t) = -V_L \cdot t/L.
\]

The length of the considered interval in mode B can be computed as

\[
t_{1(B)} - t_0 = -\frac{i_{L}(t_{1(B)}) \cdot L}{V_L}.
\]

Interval 2 \((t_1 \rightarrow t_2)\), Figs. 2(b), 3(b) (mode A); 4(b), 5(b) (mode B):

At the beginning of the interval in mode A transistor \( T_{H1} \) is turning ON at zero voltage and transistor \( T_{L1} \) is turning OFF, which enables resonant operation between inductor \( L \) and transistor output capacitances \( C_{OSS(TH2)} \) and \( C_{OSS(TL1)} \). The interval ends when capacitance \( C_{OSS(TH2)} \) is fully discharged and can be described by following equations:

\[
i_{L(A)}(t) = -\frac{V_L}{Z} \sin\left(\omega_r \left[ t + (t_{1(A)}) \right] \right)
\]

\[
t_{2(A)} - t_{1(A)} = \cos^{-1}\left(\frac{G_V - 1}{G_V}\right) \frac{1}{\omega_r}.
\]

At the end of the interval in mode A, transistor \( T_{H2} \) is turned ON at zero voltage.

In mode B, on the other hand, transistor \( T_{L2} \) is turned OFF at the start of the interval, which initiates resonant operation between inductor \( L \) and output capacitances \( C_{OSS(TH1)} \) and \( C_{OSS(TL2)} \). The interval ends when capacitance \( C_{OSS(TH2)} \) is fully discharged and can be described by following equations:

\[
i_{L(B)}(t) = -\frac{V_L}{Z} \sin\left(\omega_r (t) + \sin^{-1}\left[-i_{L}(t_{1(B)} - t_0)\right]\right)
\]

\[
t_{2(B)} - t_{1(B)} = \cos^{-1}\left(\frac{G_V}{G_V - 1}\right) \frac{1}{\omega_r}.
\]

Interval 3 \((t_2 \rightarrow t_3)\), Figs. 2(c), 3(b) (mode A); 2(c), 5(b) (mode B):

In mode A, the interval starts when transistor \( T_{H2} \) is turning ON at zero voltage. Current in inductor \( L \) rises linearly in accordance to the following equations:

\[
i_{L(A)}(t) = i_{L}(t_{2(A)}) + (V_H - V_L) \cdot t/L.
\]

The interval ends when inductor current is equal to zero and the length of this interval can be given by

\[
t_{3(A)} - t_{2(A)} = -\frac{i_{L}(t_{2(A)}) \cdot L}{V_H - V_L}.
\]

In mode B, the interval begins when transistor \( T_{L1} \) is turning OFF, transistor \( T_{H1} \) turns-ON at zero voltage and inductor \( L \) and capacitances \( C_{OSS(TH2)}, C_{OSS(TL1)} \) resonate. Inductor \( L \) current is given by

\[
i_{L(B)}(t) = -\frac{V_L}{Z} \sin\left(\omega_r (t) + \sin^{-1}\left[i_{L}(t_{2(B)})\right]\right).
\]

The considered interval length is given by the following equation:

\[
t_{3(B)} - t_{2(B)} = \cos^{-1}\left(\frac{1/2 - G_V}{1 - G_V}\right) \frac{1}{\omega_r}.
\]

Interval 4 \((t_3 \rightarrow t_4)\), Figs. 2(d), 3(c) (mode A); 4(d), 5(c) (mode B):

During this interval high side transistors \( T_{H1} \) and \( T_{H2} \) remain ON, low side transistors \( T_{L1} \) and \( T_{L2} \) remain OFF. The energy from input voltage source \( V_H \) is transferred to the inductor \( L \) and load consisting the parallel connection of output resistance \( R \) and output capacitor \( C_L \). Inductor current \( i_L \) rising linearly and can be described by the following equation:

\[
i_{L}(t) = \frac{V_H - V_L}{L} t.
\]

Interval 5 \((t_4 \rightarrow t_5)\), Figs. 2(e), 3(c) (mode A); 4(e), 5(c) (mode B):

At the beginning of the interval the transistor \( T_{H2} \) is turned OFF. Capacitance \( C_{OSS(TH2)} \) is charging and capacitance \( C_{OSS(TL1)} \)
is discharging. Assuming that inductor current is constant in the considered interval, its length can be described by

$$t_5 - t_4 = \frac{V_H \cdot C_{OSS}}{i_L(t_4)}.$$  \hspace{1cm} (17)

Interval 6; (t 5 - t 6 ); Figs. 2(f), 3(c) (mode A); 4(f), 5(c) (mode B):

At the beginning of the interval the transistor $T_{L1}$ is turning ON at zero voltage and transistor $T_{H1}$ is turning OFF. Capacitance $C_{OSS(TH1)}$ is charging and capacitance $C_{OSS(TL2)}$ is discharging. When constant inductor current is assumed in the interval, the length is calculated by

$$t_6 - t_5 = \frac{V_H \cdot C_{OSS}}{i_L(t_5)}.$$  \hspace{1cm} (18)

Interval 7; (t 6 - t 0 ); Figs. 2(g), 3(c) (mode A); 4(g), 5(c) (mode B):

At the start of the considered interval transistor $T_{L2}$ is turning ON at zero voltage. Energy accumulated in the inductor is transferred to the load. Inductor current $i_L$ reduces linearly and can be described by the following equation:

$$i_L(t) = i_L(t_6) - \frac{V_L}{L} \cdot t.$$  \hspace{1cm} (19)

Thus, one switching sequence is concluded. However, in order to maintain the natural flying capacitor voltage balancing, which is elaborated on further in the article, the full modulation sequence includes other transitions, in which the soft switching conditions are analogous to these shown in Figs. 3 and 5. Therefore ZVS at turn-ON for all the transistors is achieved. Moreover, since DT intervals are very short, their impact on the inductor current can be omitted, and, in consequence, on the output voltage as well. However, DT states are still crucial for achieving proper voltage on the flying capacitor.

C. Voltage Gain and Switching Frequency

In the proposed converter, the control parameters, such as switching frequency and duty cycle, are determined by voltage gain $G_V$ and output resistance $R$ according to the principle operation described by (4)–(19). Furthermore, switching frequency and duty cycle differ based on the voltage gain—mode A ($G_V \geq 0.5$) and mode B ($G_V \leq 0.5$)—and can be calculated based on the following equations, where $D$ ($D_A$ for mode A and $D_B$ for mode B) is the duty of the converter defined as the ratio between the time in which the converter operates in state B1 ($T_{H1}$ and $T_{H2}$ are ON) and the switching period $T_S$

$$D_A = \frac{G_{V(A)} \left\{ 1 - \frac{1}{2\pi} \cos^{-1} \left[ \frac{1 - G_{V(A)}}{G_{V(A)}} \right] \right\} \cdot \frac{f_s}{f_r} + 1}{2\pi}.$$  \hspace{1cm} (20)

$$D_B = \frac{G_{V(B)} \left\{ 1 - \frac{1}{2\pi} \cos^{-1} \left[ \frac{1 - G_{V(B)}}{G_{V(B)}} \right] \right\} \cdot \frac{f_s}{f_r} + 1}{2\pi}.$$  \hspace{1cm} (21)

Voltage gain $G_V$ and duty cycle $D$ were determined on the basis of (2)–(19). To achieve soft switching, converter should operate with a specific frequency and particular duty cycle depending directly on load resistance $R$ and voltage gain $G_V$. According to the analysis, for certain $R$ and $G_V$ there is one, specific frequency that ensures optimal conditions so that ZVS can be achieved. The control characteristics plotted for the converter on the basis of the presented formulas are shown in Fig. 6. The transformation ratio dependence on frequency for various load resistance is displayed in Fig. 6(a), whereas Fig. 6(b) presents the load resistance in function of the switching frequency for a few voltage gains $G_V$.

D. Soft Switching Conditions

In the proposed converter to achieve zero-voltage at turn-ON for all the transistors, these have to switch at certain conditions. Each transistor turn-ON process must be initiated when its output capacitance has already been discharged, which is assured through providing specific length of the DT states and with certain minimal inductor current at which the turn-ON process will occur according to equations in the previous section. This is realized via variable frequency control depending on the load parameters and the voltage gain.

To be more specific, soft turning-ON of transistors $T_{H1}$ and $T_{H2}$ require to turn-ON $T_{L1}$ and $T_{L2}$ transistors at certain times in order to provide enough current to discharge capacitances $C_{OSS(TH1, TH2)}$. Formulas for the specific times are presented in Section II-B. In mode A, transistor $T_{L2}$ has to be turned-OFF at the time when the inductor current reaches $0$. However, in order to provide full ZVS at turn-ON in mode B ($G_V \leq 0.5$) transistor $T_{L2}$ should be turned OFF at specific current, in accordance with the following equation:

$$i_L(t_{1(B)}) = -\frac{V_H \sqrt{1 - 2G_V}}{Z}.$$  \hspace{1cm} (24)

Capacitances $C_{OSS}$ of transistors $T_{L1}$ and $T_{L2}$ are discharging in intervals 5 and 6, which allows to achieve ZVS at turn-ON similarly as for the high-side transistors $T_{H1}$ and $T_{H2}$, but since
the inductor current value is much higher, the interval lengths are much shorter and thus it is assumed that the currents for both these transitions are constant throughout the whole DT state and identical for both DT1 and DT3. Moreover, both low-side transistors $T_{1,1}$ and $T_{1,2}$ are turning-OFF at very low current values (ZCS).

The analysis of the converter operation was carried out with the assumption that the value of current flow from the load to the circuit is minimized. However, since this current is required to enable soft turn-ON for the transistors, it is still apparent. Thus, it is worth noting that when this modulation method is employed the conduction losses rise slightly in comparison to a more common approach with positive inductor current throughout the whole switching cycle (CCM). Thus, low conduction loss power devices should be considered. Nevertheless, the DT time interval should be minimized to just enough to provide the possibility to reach ZVS at turn-ON but not extend this time excessively in order to maximize the efficiency.

Furthermore, even though in order to assure ZVS conditions for the transistors the inductor current $i_L$ must reach negative values (near-CRM) the output capacitor $C_L$ must be charged and discharged with the same amount of current within all the devices and equal to

$$V_{DS_{max}}(TH_1, TH_2, TL_1, TL_2) = V_H/2. \quad (25)$$

RMS currents were calculated excluding the resonant operation between inductor $L$ and transistors output capacitances $C_{OSS}$ and assuming that $G_V = D$. In that case, rms currents in transistors are given by

$$I_{rms(TH_1, TH_2)} = 2I_O \sqrt{G_V/3} \quad (26)$$
$$I_{rms(TL_1, TL_2)} = 2I_O \sqrt{(1 - G_V)/3}. \quad (27)$$

And the rms inductor current is

$$I_{rms(L)} = 2I_O / \sqrt{3}. \quad (28)$$

### F. Voltage Ripple on the Flying Capacitor

In a basic buck–boost three level converter, as noted in Section II-B, flying capacitor $C_F$ conducts through a significant part of the converter cycle, which has a substantial effect on capacitor voltage ripple and, thus, requires using a capacitor with high value of capacitance. In the proposed operation method, flying capacitor is employed only in intervals when output capacitances of transistors are charging/discharging and during transition DT states. Voltage ripple on the flying capacitor can be described based on the following equation (assuming identical output capacitance for all the transistors):

$$I_{FC \text{(disch.)}} = \frac{\int_{t_0}^{t_2(A)} i_L(t) dt}{t_2(A) - t_0} = \frac{2C_{OSS}V_H}{t_2(A) - t_0} \quad (29)$$

$$\Delta V_{FC} = \frac{I_{FC \text{(disch.)}}(t_2(A) - t_0)}{C_F} = \frac{2V_HC_{OSS}}{C_F}. \quad (30)$$

However, this equation was synthesized for the theoretical modulation pattern employing only states B and DT [see Figs. 3(b) and (c) and 5(b) and (c)]. When actual operation of the converter with additional flying capacitor voltage balancing via states F [see Fig. 3(d), (e) and 5(d), (e)] is considered the ripples may be slightly higher.

### G. Flying Capacitor Voltage Balancing

As mentioned before, in order to have the converter operate properly, the voltage on the flying capacitor $V_{FC}$ must be constant and equal to $V_H/2$. There have been many different flying capacitor voltage balancing methods proposed [11], [19]. In general, these can be divided into two main groups: classic active methods employing closed loop control systems, based on either voltage measurement [40] or more sophisticated sensorless approach [33], and suitable alteration in the modulation pattern to ensure stable flying capacitor voltage; and natural balancing methods [41] that generally operate in open loop, which rely on having the average current in the flying capacitor equal to zero during the whole switching cycle. Moreover, it can be noted the model predictive control-based methods can be used with either approach (e.g., active [42] or natural [43]). In this article, the proposed control method includes flying capacitor voltage balancing based on the convergence of conventional voltage measurement-based active and natural balancing, where stability of operation with zero average FC current in steady state is ensured through natural balancing, whereas the robustness in terms of parameter mismatches, such as differences in transistor output capacitances $C_{OSS}$ or delays in the signal paths, is assured through the active controller part.

First OFF, the system operates using two state sequences (31), (32) alternately, as shown in Fig. 7, so that the capacitor gets charged and discharged with the same amount of current within
these two sequences

\[
\text{SEQ1} = \text{B1} \rightarrow \text{DT1} \rightarrow \text{DT3} \rightarrow \text{B2} \rightarrow \text{DT4} \rightarrow \text{DT2}[31]
\]

\[
\text{SEQ2} = \text{B1} \rightarrow \text{DT2} \rightarrow \text{DT4} \rightarrow \text{B2} \rightarrow \text{DT3} \rightarrow \text{DT1}[32]
\]

In order to justify such approach, a situation in which only SEQ1 is used may be showcased as an counterexample. Then, the capacitor would be always discharged (state F2) with high inductor current (I_{\text{MAX}}) whereas the charging (state F1) would occur with lower inductor current (I_{\text{MIN}}) described by equations from (4) to (15). Therefore, the capacitor would draw less energy than it would receive resulting in an unbalanced voltage below the desired level (V_{\text{FC}} < V_{H}/2). Thus, applying the presented sequence order guarantees (assuming constant inductor current) that the same amount of energy is transferred from and into the flying capacitor and, therefore, will result in natural voltage balancing.

However, when the converter conditions shift, for example due to change in supply voltage or load values, the inductor current fluctuates and the natural balancing sequence will not be sufficient. Therefore, second balancing measure, in form of a closed-loop controller shown in Fig. 8 is applied as well. Based on the measurement of the voltages V_H and V_{\text{FC}} it is known whether the flying capacitor is balanced at V_{H}/2 and further the error signal can be applied in a PI controller, which regulates the value of D_{\text{LVL}}, applying additional intervals and its converter states F1 and F2 according to Table II in-between the transition states, as shown in Figs. 3(d) and (e) and 5(d) and (e). Furthermore, depending whether the flying capacitor voltage is too high or too low, either discharging state F2 or charging state F1 is applied for the amount of time defined by D_{\text{LVL}}.

Moreover, as in any FCC, additional, well-known start-up measures are required in order to assure stable FC voltage during system initialization, e.g., using precharging [44].

### III. Simulation Study

In order to initially validate the proposed TCM-Q2L control method for a FCC a simulation study in Synopsys Saber was conducted, so that the power MOSFET modeling tool could be employed for semiconductor power transistors ensuing highly accurate results, as simulating the resonance between the output MOSFET capacitances and the inductor requires precise switching models.

Since the converter was to operate at a maximum of 1.5 kV of dc voltage 1.2 kV SiC MOSFETs (FF11MR12W1M1_B11) from Infineon were chosen as the power devices based on preliminary power loss estimations and further selection among the state-of-the-art semiconductors. The parameters of the converter for both simulation and experimental study are shown in Table III.

![Fig. 9](image-url) Exemplary results of the converter operation with the proposed TCM-Q2L control method from the simulation study. Simulation performed at 1500 V dc input voltage, voltage gain G_V at 0.2 with a load resistance of 17.2 Ω. From the top: inductor voltage (v_{IND}) and current (i_L); flying capacitor voltage (V_{FC}); gate-source voltages of high-side transistors (v_{GSTH1}, v_{GSTH2}); MOSFET currents (i_{MOSTH1}, i_{MOSTH2}) and transistor drain-source voltages (v_{DSTH1}, v_{DSTH2}) of high-side switches; gate-source voltages of low-side transistors (v_{GSTL1}, v_{GSTL2}); MOSFET currents (i_{MOSTL1}, i_{MOSTL2}) and transistor drain-source voltages (v_{DSTL1}, v_{DSTL2}) of low-side switches.

![Fig. 9](image-url) Exemplary results of the converter operation with the proposed TCM-Q2L control method from the simulation study. Simulation performed at 1500 V dc input voltage, voltage gain G_V at 0.2 with a load resistance of 17.2 Ω. From the top: inductor voltage (v_{IND}) and current (i_L); flying capacitor voltage (V_{FC}); gate-source voltages of high-side transistors (v_{GSTH1}, v_{GSTH2}); MOSFET currents (i_{MOSTH1}, i_{MOSTH2}) and transistor drain-source voltages (v_{DSTH1}, v_{DSTH2}) of high-side switches; gate-source voltages of low-side transistors (v_{GSTL1}, v_{GSTL2}); MOSFET currents (i_{MOSTL1}, i_{MOSTL2}) and transistor drain-source voltages (v_{DSTL1}, v_{DSTL2}) of low-side switches.

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| Table III Parameters of the Converter |
|--------------------------------------|
| Parameter                            | Description                      |
| Max DC voltage                       | 1500 V                           |
| Switching frequency                  | 40 \( \times \) 260 kHz          |
| Voltage gain                         | 0 \( \times \) 1                 |
| SiC power transistors                | 1.2 kV and 11 mΩ                 |
| Inductor                             | FF11MR12W1M1_B11                 |
| Flying capacitor                     | 330 nF/1000 V                    |
| Output/input capacitors              | 6 μF/1600 V                      |
a load resistance of 17.2 Ω, in which the switching frequency settled at roughly 121 kHz. The presented results and conducted simulation tests confirm the theoretical presumptions on the converter operation. On the first waveform from the top characteristic shape of the inductor voltage and current can be observed, where voltage $v_{\text{IND}}$ resembles classic two-level solution but with extended slopes, whereas current $i_L$ is characterized by visible resonant influence near $I_{\text{MIN}}$ value. Further on Fig. 9, flying capacitor voltage is showcased to be balanced at 750 V and with minimal ripples, which assures balanced voltage distribution among transistor pairs ($v_{\text{DSTH1}}, v_{\text{DSTH2}}$ and $v_{\text{DSTL1}}, v_{\text{DSTL2}}$), which is also visible on the next waveforms. Moreover, the figure showcases ZVS operation at turn–ON for all the power semiconductor devices through $i_{\text{DOS}}, v_{\text{DS}}$, and $v_{\text{GS}}$ curves. Furthermore, near-ZCS transition for the turn–OFF process for the low-side transistors can be noted as well.

IV. LABORATORY MODEL

The next step was to design and construct a MV prototype of the FCC with the proposed TCM-Q2L control method based on electro-thermal calculation using the simulation study outcomes and datasheets. The main parameters of the experimental system are identical as in the simulation study and are showcased in Table III. As the converter operates in Q2L mode the flying capacitor $C_F$ could be set to only 330 nF in order to achieve voltage ripples $\Delta V_{\text{FC}}$ below 5% of $V_{\text{FC}}$ voltage, which is notably less than in standard multilevel approach. Moreover, in order to sustain manageable voltage ripples at the input and the output of the converter $6 \mu \text{H}/1600 \text{ V}$ capacitance was applied for both ends of the system ($C_H$ and $C_L$). Furthermore, a 30 $\mu \text{H}$ inductor was used so that roughly 100 kHz operating frequency at 17.2 Ω load resistance and voltage gain $G_V$ of 0.5 could be achieved as nominal parameters.

Moreover, since the converter was to operate at notable frequencies even up to 250 kHz and with voltage of 1500 V dc resulting in high $dv/dt$ rates, special care was given to the design of the power circuit. The path length of the main power loops and gate connections were minimized so that the parasitic inductances between the switching components could be reduced. The applied isolated gate drivers were self-made based on UCC21750 chip and suggestions from [45], providing suitable protection measures for safe operation of the converter and satisfactory switching performance as 5 Ω gate resistances were used. Furthermore, Fischer LA V 8 with forced air convection was used as the heatsink. The required measurements of voltages $V_H$ and $V_F$ were delivered using analog circuits based on isolated voltage followers. Finally, the whole system was controlled through a control board, based on floating-point DSP (TMS320F28379D), and mounted on a grounded cover on the side of the converter in order to shield it from the interferences generated by the system. The constructed converter prototype is presented in Fig. 10.

V. EXPERIMENTAL STUDY

In order to fully validate, the proposed control method for the FCC a series of experimental tests was performed with up to 1500 V dc voltage and up to 10 kW power with the constructed prototype. The main purpose of this article was to plot experimental characteristics of the TCM-Q2L control method along with the measurements of component stresses and the system efficiency for various loads $R$ and voltage gain $G_V$ ratios. The experimental system consisted of the FCC with a resistive load supplied by a dc power supply from Magna-Power. The power and efficiency measurements were performed using Norma LEM 6000 power analyzer, whilst the oscillograms were acquired by Tektronix MSO56 oscilloscope with isolated voltage probes (Tektronix THDP0100 and P2505A) and a current probe (Tektronix TCP303). The scheme of the experimental setup is shown in Fig. 11.

At first, the converter was tested with nominal input voltage of 1500 V and load resistance of 17.2 Ω. Due to limitations in regard to the power supply capabilities (2 kV, 5 A) the power for the experiment was constrained to roughly 5.5 kW with limited voltage gain $G_V$ at 0.2 (mode B). Such parameters resulted in the system to operate at 122 kHz switching frequency. The results from this test are showcased in Fig. 12. As shown on the top oscillogram [see Fig. 12(a)] the flying capacitor voltage $V_{\text{FC}}$ is balanced with limited ripples below 5% of the nominal voltage equal to 750 V. Furthermore, the inductor voltage $v_{\text{IND}}$ has characteristic Q2L-control shape, where the 3L state is employed
only for a very brief moment ($D_{LVL}$ in this test settled close to 0.995). Inductor current $i_L$ reached roughly 27 A rms value with peak-to-peak current at 70 A. The oscillogram in Fig. 12(b) presents the results from another test with the same parameters. Gate-source voltages are shown next to drain-source voltages in order to showcase ZVS at turn-ON for the devices, and, as the drain-source voltages clearly reach 0 before the gate-source voltage achieve its threshold value, ZVS is confirmed. Moreover, even though voltage oscillations are clearly visible at turn-OFF, the peak drain-source voltage values settled below 900 V, with OFF values equal to $V_{FC}$, therefore, the transistors operated within safe conditions throughout the whole test.

In order to validate the converter operating at higher power and with higher voltage gain, the rest of the experimental tests were performed using another power supply, also from Magna-Power (800 V, 12.5 A), with capabilities of up to 10 kW. The load resistance $R$ in this tests varied from 10 up to 200 Ω with diverse voltage gains from 0.15 up to 0.75, which resulted in operating frequency of 40 to 250 kHz.

The next Fig. 13 presents results from a test conducted at 800 V dc input voltage, mode A (voltage gain $G_V$ at 0.7) with a load resistance of 34.6 Ω - roughly 10 kW power at 116 kHz switching frequency—(a) general view, (b) top transistor pair-focused view and (c) low transistor pair-focused view. From the top: input voltage ($V_{H}$); flying capacitor voltage ($V_{FC}$); gate-source voltages of top-side transistors ($v_{GSTH1}, v_{GSTH2}$); transistor drain-source voltages ($v_{DSTH1}, v_{DSTH2}$) of top-side switches; gate-source voltages of low-side transistors ($v_{GSTL1}, v_{GSTL2}$); transistor drain-source voltages ($v_{DSTL1}, v_{DSTL2}$) of low-side switches. In this experiment, the inductor current established at 24 A rms and 50 A peak-to-peak values and the flying capacitor voltage ripples settled below 5%. Moreover, ZVS turn-ON transition can be observed for all the devices. Furthermore, near-ZCS turn-OFF for the low-side transistor pair ($T_{L1}, T_{L2}$) can be observed as well.

Fig. 14(a) showcases results from an experiment performed at 800 V dc input voltage, mode C (voltage gain $G_V$ at 0.5) with a load resistance of 34.6 Ω, which lead to 5.2 kW power at 178 kHz.
Fig. 14. Experimental results from an experiment performed at 800 V dc input voltage. From the top: input voltage \( V_H \); inductor voltage \( V_{\text{IND}} \) and current \( i_L \); flying capacitor voltage \( V_{\text{FC}} \). (a) Voltage gain \( G_V \) at 0.5 with resistance of 34.6 \( \Omega \) - 5.2 kW power at 178 kHz switching frequency. (b) Mode B (voltage gain \( G_V \) at 0.4) with a load resistance of 34.6 \( \Omega \) - roughly 3.5 kW power at 189 kHz switching frequency. The oscillogram shows balanced \( V_{\text{FC}} \) voltage, inductor current \( i_L \) and voltage \( V_{\text{IND}} \) and input voltage \( V_H \). In this experiment, the inductor current established at 18 A rms and 39 A peak-to-peak values and the flying capacitor voltage ripples settled below 5%. (c) Mode B (voltage gain \( G_V \) at 0.4) with a load resistance of 10.4 \( \Omega \) - roughly 10 kW power at 86 kHz switching frequency. Again, the exposition is identical as before. The inductor current established at 13 A rms and 33 A peak-to-peak values and the flying capacitor voltage ripples established below 5%. (d) Mode B (voltage gain \( G_V \) at 0.4) with a load resistance of 69.2 \( \Omega \) - roughly 2.4 kW power at 254 kHz switching frequency.

Based on the experimental data acquired from the tests, a series of converter characteristics were plotted and are shown in Fig. 15. At first, in Fig. 15(a) the control characteristics showcasing the dependence between voltage gain \( G_V \) and switching frequency \( f_S \) for constant load resistances 17.2 and 34.6 \( \Omega \) are presented and the experimental results are compared to theoretical values calculated for the same operating parameters. As can switching frequency. At this \( G_V \) formulas for both modes are applicable and result in a situation where \( t_{DT1} = t_{DT3} \) (see Figs. 3 and 5), thus resulting in near-sinusoidal shape of the inductor current near \( I_{\text{MIN}} \) value. The oscillogram shows balanced \( V_{\text{FC}} \) voltage, inductor current \( i_L \) and voltage \( V_{\text{IND}} \) and input voltage \( V_H \). In this experiment, the inductor current established at 18 A rms and 39 A peak-to-peak values and the flying capacitor voltage ripples settled below 5%.

In the final test, performed at the same resistance (34.6 \( \Omega \)), and at this voltage (800 V), presented in Fig. 14(b), the converter operated in mode B (voltage gain \( G_V \) at 0.4) at roughly 3.5 kW power and 189 kHz switching frequency. The presentation is identical as before. The inductor current established at 13 A rms and 33 A peak-to-peak values and the flying capacitor voltage ripples established below 5%.

The next oscillogram, shown in Fig. 14(c), presents a test in which the converter operated at lower resistance of 10.4 \( \Omega \). The experiment was performed at 800 V dc input voltage, in mode B (voltage gain \( G_V \) at 0.4) resulting in roughly 10 kW power at 860 kHz switching frequency. Again, the exposition is similar, with the image showcasing balanced \( V_{\text{FC}} \) voltage, inductor current \( i_L \) and voltage \( V_{\text{IND}} \), as well as input voltage \( V_H \). The inductor current established at 41 A rms and 82 A peak-to-peak values and the flying capacitor voltage ripples established below 5%.

The last oscillogram, presented in Fig. 14(d), depicts a test with the highest tested frequency (254 kHz). The experiment was performed at 800 V dc input voltage, in mode B (voltage gain \( G_V \) at 0.4) and with a resistance of 69.2 \( \Omega \) resulting in roughly 2.4 kW. The inductor current established at 11 A rms and 25 A peak-to-peak values and the flying capacitor voltage ripples established below 5%.
be seen, these are highly comparable, with slight differences in regard to voltage gain values. Nevertheless, the validity of the theoretical analysis of the converter and the control method is confirmed. In such conditions, the converter can operate at any voltage gain adopting proper frequency in range from dc to roughly 200 kHz for 34.6 \( \Omega \), and from dc to approximately 150 kHz for 17.2 \( \Omega \). In Fig. 15(b), the dependence between switching frequency \( f_s \) and resistances \( R \) for constant voltage gain of 0.4 (mode B) and 0.7 (mode A) is shown. Similarly to the situation before, the results from the experimental study are akin to the theoretical values. Furthermore, it should be noted that for such inductor (30 \( \mu \)H) higher resistance will result in very high operating frequencies leading to possible practical issues.

Next on, efficiency curves of the converter were plotted as well for the results from the experimental study and also according to theoretical derivations. Driving, control and forced ‘cooling power losses settled at roughly 15 W and were omitted for efficiency characteristics for both theoretical and experimental cases, as these systems were supplied from a different source in the prototype tests. Furthermore, capacitor power losses were omitted as well.

The theoretical efficiency can be calculated as shown below, again with the omission of transition DT states. First, the inductor power losses was estimated as conduction wire loss \( P_{C(L)} \) using dc inductor resistance measured experimentally and (28) along with the inductor core loss \( P_{core(L)} \), which according to the software from the core manufacturer Ferroxcube can be estimated as constant 15 W, as variances for different operating points were minimal. As the inductor was constructed using Litz wires with high strand number, and to simplify the equations, other power losses, e.g., these caused by skin effect, were omitted

\[
P_L = P_{C(L)} + P_{core(L)} = R_{dc(L)}I_{rms(L)}^2 + P_{core(L)}.
\] (33)

The other crucial source of the converter power losses are semiconductor power devices. Since low-pair transistors \( T_{L1} \) and \( T_{L2} \) are fully soft switched at turn-OFF, and achieve near-ZCS at turn-on, their power loss is limited to conduction loss and using \( R_{DS(on)} \) from the datasheet at junction temperature of 100 \( ^\circ \)C and (27), it can be described as

\[
P_{TL} = P_{C(TL)} = R_{DS(on)}I_{rms(TL)}^2.
\] (34)

When high-pair transistors are considered the conduction loss can be calculated using analogous relationship of \( R_{DS(on)} \) and (26). However, these power devices are hard-switched at turn-OFF and, thus, switching power loss at turn-OFF is added as well using the calculation based on datasheet values

\[
P_{SW-OFF(TH)} = \frac{V_{DS}}{V_{d(th)}}I_{MAX}E_{OFF}f_s.
\] (35)

\[
P_{TH} = R_{DS(on)}I_{rms(TH)}^2 + P_{SW-OFF(TH)}.
\] (36)

Finally, the converter theoretical efficiency can be calculated as

\[
\eta = \frac{P_{conv}}{P_{conv} + (2P_{TH} + 2P_{TL} + P_L)} \times 100\%.
\] (37)

Fig. 16(a) presents the dependence between converter efficiency \( \eta \) and voltage gain \( G_V \) for constant load resistances of 17.2 and 34.6 \( \Omega \). As can be seen, the higher the gain, the higher the efficiency, reaching as high as 99.1%. The performed tests from \( G_V \) at 0.15 to 0.75 resulted in efficiencies in the range of 95.4 to 99.1%. The second characteristic, shown in Fig. 16(b), presents the dependence between converter efficiency \( \eta \) and converter power \( P_{conv} \) for constant voltage gains of 0.4, 0.5 and 0.7. For such operating conditions, for which the system was designed, the efficiency ranged from roughly 98% to 99% with peak efficiency of 99.1% at \( G_V = 0.7 \) and \( P = 5 \) kW, which is a noteworthy value in comparison to other converters with similar voltage/current conditions, especially considering that the converter can operate for various voltage gains and a wide load range. When we compare the experimental results with the theoretical curves we can see that, similarly to the case before, these are in accordance as well.

VI. COMPARISON

A comparison of the FCC with the proposed TCM-Q2L control method with classic and state-of-the-art dc–dc converter topologies is presented in Table IV. When compared in terms of power semiconductor devices, even in unidirectional mode, four transistors are used. Furthermore, since the system is 3L, the voltage stress on the transistors is limited to \( V_{th}/2 \). However, since the flying capacitor is used only for very brief moments of the switching cycle, the capacitance and the current flowing through the FC are greatly reduced in comparison to classic 3L FCC systems [33]. Moreover, even if the converter operates at very high frequency, due to the TCM-Q2L modulation pattern, the efficiency is at a very high level, which is comparable, or even surpasses the other approaches. Additionally, it is worth noting that this system does not require any additional components—the basic topology is identical as in a standard 3L FCC. Also, in order to facilitate the TCM-Q2L method and achieve soft switching it is required that the converter operates in near-CRM mode, thus, rms current values are quite high in comparison to the converters operating in CCM resulting in higher conduction loss.
TABLE IV

| Parameter                      | Basic 2L converter | CL-TCM converter [31] | 3L FCC in CCM [33] | TCM-3L FCC [34, 36] | Proposed TCM-Q2L FCC |
|--------------------------------|--------------------|------------------------|--------------------|---------------------|----------------------|
| MOSFET no.                    | 1                  | 3                      | 2                  | 4                   | 4                    |
| Diode no.                     | V_d                | V_d                    | V_d/2              | V_d/2               | V_d/2                |
| Switching frequency           | Medium             | Medium                 | Medium             | Very high           | Very high            |
| Conduction mode               | All                | near-CRM               | CCM                | near-CRM            | near-CRM             |
| Soft switching                | None               | Full                   | None               | Full at turn-on     | Full at turn-on      |
|                              |                    |                        |                    | partial at turn-off | partial at turn-off  |
| Additional soft switching     | Yes                | -                      | -                  | No                  | No                   |
| components                    |                    |                        |                    |                     |                      |
| Flying capacitance            | -                  | High                   | High               | Very low            |                      |
| Choke inductance              | -                  | High                   | Low                | Low to medium       | Medium to high       |
| RMS choke current             | -                  | Low                    | Low                | High                | High                 |
| Efficiency                    | Medium             | High                   | High               | High                |                      |

Fig. 17. Waveforms for conventional 3L buck converter with flying capacitor for $G_V < 0.5$ and $G_V > 0.5$.

Furthermore, the third level of voltage is employed only to balance the FC voltage and achieve soft switching and not to lower the inductor current derivative as it is the case for a conventional 3L converter. Moreover, the methodology for achieving soft switching is similar as in a TCM-3L converter [34], [38], but in that solution the inductor value will be lower than in TCM-Q2L. However due to Q2L operation both current and the capacitance of the FC is reduced.

In order to compare these two systems more comprehensively further theoretical analysis was conducted. The assumption is that, in order to simplify the equation derivation, the TCM intervals, in which the resonance occurs, are omitted for both converters, as the length of these intervals is highly comparable for both Q2L and 3L converters and their impact on system operating frequency and RMS currents is limited for high output power. The voltage and current waveforms for a conventional 3L converter operating in CRM are shown in Fig. 17. It can be noted that depending on the voltage gain $G_V$ the modulation is different. For $G_V < 0.5$

$$\Delta i_L = \frac{(1/2V_H - V_L) d_L T_S}{L}$$  \hspace{1cm} (38)

$$d_L (1/2V_H - V_L) = (1 - d_L) V_L.$$  \hspace{1cm} (39)

For $G_V > 0.5$

$$\Delta i_L = \frac{(V_H - V_L) d_H T_S}{L}$$  \hspace{1cm} (40)

$$d_H (V_H - V_L) = (1 - d_H) (V_L - 1/2V_H).$$  \hspace{1cm} (41)

While for the Q2L operated converter, under the previously mentioned assumptions, the ripples are regardless of the voltage gain and the switching frequency and can be described as

$$\Delta i_L = I_{MAX} = 2I_O.$$  \hspace{1cm} (42)

In CRM, the ratio between the output current $I_O$ and max inductor current $I_{MAX}$ is constant for all operating points and equal to 1:2 and the output power of the system is controlled by its operating frequency. Assuming that $\Delta i_L/I_O = 2$, the inductor ripple frequency (which is doubled in comparison with the switching frequency in the conventionally operated 3L converter) can be described as

$$f_{\Delta i_L} = \frac{R(1 - 2G_V)}{2L} \text{ for } G_V \leq 0.5$$  \hspace{1cm} (43)

$$f_{\Delta i_L} = \frac{R(1 - G_V)(2G_V - 1)}{2LG_V} \text{ for } G_V \geq 0.5.$$  \hspace{1cm} (44)

For the proposed TCM-Q2L converter, omitting the resonance intervals, the inductor ripple frequency can be described by the same equation as for a conventional 2L buck converter operating in CRM

$$f_{\Delta i_L} = \frac{R(1 - G_V)}{2L}.$$  \hspace{1cm} (45)

According to the characteristics shown in Fig. 18 3L-based converter operates at much lower inductance with the same inductor current ripples. However, it does not necessarily eliminate the Q2L method. First, the regulatory characteristic (effectively frequency) of the 3L system is highly nonlinear for $G_V \geq 0.5$,
Moreover, Fig. 19(b) showcases further comparison between voltage ripples and voltage gain and various values of $RC_F$. As shown, the flying capacitance in the Q2L system is very low and constant regardless of load resistance $R$. On the other hand, in the 3L system it is dependent on the operating point and much higher for most of the range. This is especially visible for low load resistances, where the difference is very significant. Moreover, near $G_V = 0.5$ the 3L system requires very high flying capacitance $C_F$ for lighter loads, thus imposing whether 3L systems can be practically used for such voltage gains, whereas for the Q2L system this is a nonexistent issue. Furthermore, using a flying capacitor with lower capacitance provides the possibility to reduce the stray inductance of the switching loop connections, which will improve the switching processes of the hard-turned-off transistors $T_{H1}$ and $T_{H2}$. According to this comparison TCM-Q2L will be superior for high-power application with light loads and for voltage gains close to $G_V = 0.5$, as compared with TCM-3L the increase in terms of inductance $L$ is not as high as the possible gain based on lowering the flying capacitance.

Moreover, since both solutions operate on a very similar basis in terms of TCM and variable operating frequency the efficiency should be similar as well. In regard to the rms currents, since the current waveforms are alike in both systems, (26) and (27) are true for TCM-3L as well, thus the semiconductor power loss is highly comparable. The differences can be observed in FC power loss, as in the TCM-Q2L system the FC current is minimal, however the impact of FC loss is not a significant factor compared to semiconductor and inductor losses.

The case is alike in comparison to the system shown in [37], since the TCM operation is very similar here and the characteristics in shown in Fig. 18 are applicable as well. The difference comes in a fact that the system in [37] has a different topology, as it essentially is a doubled 2L buck converter, and the difference comes in a fact that the system in [37] has a different topology, as it essentially is a doubled 2L buck converter, and thus, there is no flying capacitor. Moreover, there are two high voltage side capacitors instead of one, however rated at a lower voltage of $V_{DC}/2$. Finally, the converter in [37] operates without capacitor voltage measurement.

Altogether, when compared with other conventional and state-of-the-art solutions the TCM-Q2L converter can match or even surpass its competitors in terms of performance and is a noteworthy solution in high-power dc–dc energy conversion.

VII. CONCLUSION

In this article, a novel TCM-Q2L control method for a flying capacitor converter have been proposed. Based on an extensive theoretical analysis, simulation study, and experimental tests on the constructed prototype up to 1500 V voltage and up to 10 kW power the proposed system has been successfully validated. The efficiency of the converter peaked at 99.1% for 5 kW output power, voltage gain of 0.7 and very high operating frequency at 189 kHz, while maintaining the efficiency above 97.8% for most of the operating range. Furthermore, Q2L operation mode have provided the possibility to use fast, affordable and widely available 1200 V SiC MOSFETs at 1500 V input voltage with intensively reduced flying capacitance, to just 330 nF, which is
a minimal value in comparison with more standard approaches. Moreover, the proposed TCM-Q2L modulation pattern introducing full-ZVS conditions for turn-on provides the possibility to operate at very high frequencies, even as high as 250 kHz, thus maintaining a low value of inductance, while keeping the efficiency very high. Finally, the system is capable of operation for a wide variety of voltage gains and loads.

Thus, applying the proposed TCM-Q2L control for the FCC may be a noteworthy solution to convert energy in MV range with high efficiency and relatively high power density, and may be competitively used against classical two-level, as well as three-level and series connection-based dc–dc converters.

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Michał Harasimeczuk was born in Białystok, Poland. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Białystok University of Technology, Białystok, Poland, in 2013 and 2019, respectively.

He is currently with the Institute of Control and Industrial Electronics, Warsaw University of Technology, Warszawa, Poland. His research interests include power electronics, namely, dc–dc soft-switching converters, battery charging systems, and ac–dc converters.

Rafał Kopacz (Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering in 2018 and 2019, respectively, from the Warsaw University of Technology, Warszawa, Poland, where he is currently working toward the Ph.D. degree.

He is currently a Research Assistant with the Institute of Control and Industrial Electronics, Warsaw University of Technology. In 2019, he spent a few months with Sintef Energy and Norwegian University of Science and Technology, Trondheim, Norway, where he was working on semiconductor reliability issues in power electronics. His main research interests include SiC-based power converters, energy conversion in MV range with series connection and multilevel topologies, as well as dc–dc converters for EV fast charging stations, traction applications, and renewable energy sources.

Przemysław Trochimuk (Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering in 2017 and 2018, respectively, from the Warsaw University of Technology, Warszawa, Poland, where he is currently working toward the Ph.D. degree with the Institute of Control and Industrial Electronics.

His main research interests include SiC-based power converters, energy conversion in MV range with series connection, active gate drivers of power SiC MOSFETs, as well as power converters for EV fast charging stations and renewable energy sources, and also include magnetic issues in power electronic converters and, recently, on EMC concerns in power supply units.

Grzegorz Wrona received the M.Sc. degree in electrical engineering in 2010 from the Institute of Control and Industrial Electronics, Warsaw University of Technology, Warsaw, Poland, where he is currently working toward the Ph.D. degree with the Electrical Engineering Faculty.

His research interests include power converters applied to renewable energy applications, control of power electronic converters and industrial drives, power quality in renewable generation plants, and DSP microcontroller.

Jacek Rąbkowski (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees in electrical engineering from the Warsaw University of Technology, Warszawa, Poland, in 2000 and 2005, respectively.

In 2004, he was with the Institute of Control and Industrial Electronics, Warsaw University of Technology, where he is currently a Professor of power electronics. During the years 2010–2013, he was also with the Laboratory of Electrical Energy Conversion, KTH Royal Institute of Technology in Stockholm, Sweden, and 2015–2016 with Power Electronics Group, Tallin University of Technology, Tallin, Estonia. He has coauthored more than 190 scientific papers and two books. Moreover, he works in the area of medium voltage power conversion and, recently, on power converters for EV charging.

His current research interests include power converters based on wide band-gap devices: topologies, design aspects, pulsewidth modulation techniques, and, especially, gate and base drivers.

Dr. Rąbkowski was a Chairman of the Joint Industrial Electronics Society/Energy Electronics Society Chapter in the frame of the IEEE Poland Section in 2012–2015. He has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2015. He is also a member of the European Power Electronics and Drives Association, involved with the International Scientific Committee.