Impact of geometry and non-idealities on electron ‘optics’ based graphene p-n junction devices

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We articulate the challenges and opportunities of unconventional devices using the photon like flow of electrons in graphene, such as Graphene Klein Tunnel (GKT) transistors. The underlying physics is the employment of momentum rather than energy filtering to engineer a gate tunable transport gap in a 2D Dirac cone bandstructure. In the ballistic limit, we get a clean tunable gap that implies subthermal switching voltages below the Boltzmann limit, while maintaining a high saturating current in the output characteristic. In realistic structures, detailed numerical simulations and experiments show that momentum scattering, especially from the edges, bleeds leakage paths into the transport gap and turns it into a pseudogap. We quantify the importance of reducing edge roughness and overall geometry on the low-bias transfer characteristics of GKT transistors and benchmark against experimental data. We find that geometry plays a critical role in determining the performance of electron optics based devices that utilize angular resolution of electrons.

In recent years, there has been a number of proposals [1–7] of graphene devices that rely on transport gaps [8] instead of bandgaps exploiting the unique properties of Dirac cone systems at p-n junctions. Some of these initial device ideas relied on negative refractive index and Veselago lensing resulting from the conservation of transverse quasi-momentum at the junction [9, 10]. However, the switching properties of such waveguide-like devices are likely to be very modest, even for perfect geometries in scaled devices [1, 11], due to the need for sharp injectors and detectors. Angle dependent transmission of Dirac fermions [12] in graphene p-n junction (GPNJ), on the other hand, potentially offers more robust solutions with macroscopic gates and contacts.

A perfect match of the pseudospin structure at the interface causes a GPNJ to become completely transparent to normally incident electrons (Klein tunneling [13, 14]) while it becomes more opaque as the incident angle increases. Ramping up the voltage barrier across the junction collimates the electrons by narrowing the distribution of their transmission angles. This collimation can be further enhanced with a smoothly varying barrier of finite width spanning a split gated junction, which imposes an added Gaussian distribution around normal incidence [12]. Subsequently, putting a second junction at a relative angle (δ) rejects most of the electrons as long as δ exceeds the maximum critical angle (θC) of the filtered and collimated electrons [4]. This two junction device, analogous to a polarizer/analyzer in optics, is broadly referred to as Graphene Klein Tunnel (GKT) transistor (Fig. 1).

Angle dependent transmission is key to getting a tunable resistance in a GKT, achieved by controlling the gate voltage. Sajjad et al. have shown that such a GKT transistor would show a clean transport gap in the off state leading to a nearly ideal transfer characteristic consisting of low off current, high on-off ratio

![Graphene Klein Tunnel transistor using electron optics.](image)

**FIG. 1.** Graphene Klein Tunnel transistor using electron optics. (A) 3D schematic. The polar plots in inset show angle dependent transmission probability of electrons at each junction in the off state (n-p-n). First junction only permits normal incident electrons. Second junction, tilted at |δ| = 45°, is allowing only electrons close to -45°, thereby filtering most of the electrons. (B) Top view. Off state electron paths are shown in red color and white color path shows non-specular reflection from rough edge resulting in leakage in off state. (C) Potential profile in on (n-n-n) and off (n-p-n) state. Here, d is the junction width.

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(I_{on}/I_{off}=R_{off}/R_{on}=10^4) and steep subthreshold swing (SS) lower than the Boltzmann limit of 60 mV/decade [2, 4]. Beyond a desirable gate transfer characteristic, the GKT transistor was also shown to have an excellent output characteristic with a high saturating on current retaining a high mobility in the on state [7, 15]. In these calculations [2, 4, 15] however, non-idealities such as momentum scattering, in particular at the edges were not considered.

Edge scattering of rejected electrons or holes at the second junction compromises the off state leakage current, as the charge carriers keep bouncing around until some of them find themselves in the narrow transmission lobe of the second junction. Indeed, considering edges and secondary bounces, a more realistic calculation using both quantum and semi-classical models showed that the on-off ratio degrades to \( \sim 10^2 \) for perfect edges at widths of \( \sim 1 \mu m \) [3, 5, 16]. Based on the initial two junction device idea [3, 4], Morikawa et al. [6] and Wang et al. [17] reported experimental on-off ratios of 1.3 and 6-13 respectively, but these on-off ratios are low compared to predictions. Multiple experiments have now confirmed the basic physics of angle dependent transmission at a single tilted junction [18, 19], and impact of Klein tunneling in a graphene quantum dot [20], yet no rigorous study has been found explaining the poor on-off ratio in double junction devices in general.

In this paper, we explain the existing discrepancy between simulations (on-off ratio \( \sim 10^2 \)) [3, 5, 16] and experiments (on-off ratio \( \sim 10 \)) [17] of GKT devices. We find that in addition to the electrons suffering multiple bounces around the wedge shaped region between junctions, non-specular (diffusive) scattering by rough edges, shown by white arrow in Fig. 1B, plays an important role in degrading the on-off ratio by transforming the transport gap to a pseudogap with a non-zero floor (Fig. 2A). We see dips at \( E = \pm 0.3 \) eV due to Dirac points. As shown in Fig 2B, edge roughness degrades the off state performance (\( V_G \sim -10 \) V) for any given \( \delta \). We also show that \( \delta = 45^\circ \) gives the lowest off current even in the presence of edge roughness, as suggested earlier [21]. Here, local gate dielectric (hexagonal boron nitride, hBN) thickness is 32 nm. To discuss the effect of edge roughness in detail as well as the dependence on device geometry, we analyze a variety of structures in this paper (Fig. 3).

In this study, we adopt semiclassical ray tracing approach [16, 19] based on a billiard model [22–24] that has been benchmarked against experiments [19]. A charge carrier hitting a perfect edge reflects back with an angle equal to the incident angle (specular reflection). In presence of edge roughness, a Gaussian distributed random angle of reflection with standard deviation \( \sigma_e \) (higher \( \sigma_e \) denoting rougher edges) is added. The transmission probability (T) for each electron across a junction is calculated analytically, using a generalized version [4] (eqn. S1 [25]) of the well-known equation [12] for symmetrical junction, \( T \sim e^{-\pi k_F \sigma_e \sin^2 \theta} \). Here, \( k_F \) is the magnitude of the Fermi wave vector on each side for a symmetric p-n junction, \( d \) is the junction width, and \( \theta \) is the incident angle at the junction. We calculate channel resistance \( R_{CH} \) for low-bias and total resistance using \( R_T = R_{CH} + 2 R_C \), where \( R_C \) is the contact resistance between graphene and source/drain electrodes [25]. To explain experimental data [17], contact resistance \( R_C \sim 100 \Omega \mu m \) and non-specular edge scattering are included.

![FIG. 2. DJT Device characteristics. (A) Conductance of p-n junction devices in off state (n-p or n-p-n). Transport gap between -0.67 eV and +0.3 eV arises due to electron filtering in ideal n-p-n device with \( \delta = 45^\circ \). Adding edge roughness increases the floor value of the gap shown by dashed line. For comparison we also show single n-p junction conductance (abrupt and smooth with junction width \( d = 70 \) nm). (B) Transfer characteristics from semiclassical ray tracing simulation with source-drain voltage \( V_{DS}=0.1 \) V.](image-url)
Edge roughness tends to decrease the on-off ratio of these devices by diffusive scattering of the reflected electrons providing a leakage path to the drain as shown in Fig. 3(C, E) by the white dashed lines. Thus the transport gap turns into a pseudo gap with a finite floor (Fig. 4B) with increasing edge roughness. For ideal edges we see a transport gap spanning -0.67 eV to +0.3 eV. With increasing edge roughness, the floor value of the gap also increases (other than at \( E = -0.3 \) eV due to a clear Dirac point, which in turn could be washed out by impurity scattering and puddles), thus increasing off state conductance and decreasing resistance. In Fig. 4C, we show the evolution of resistance characteristics of the DS device with increasing edge roughness. Here we use device parameters \( d = 60 \) nm, width=800 nm, and voltages \( V_G = -6 \) V to 6 V, \( V_{BG} = 60 \) V, emulating a local gate voltage of 6 V, as in the experiment. In Ref. [17], all the regions (n-n-n/p-n) are controlled by local gates whereas in our simulation only the middle region is controlled by a local gate (\( V_G \)) while other regions are controlled by back gate (\( V_{BG} \)). We match the on state (\( V_G = 6 \) V) result by fitting a contact resistance (\( R_C = 117 \Omega \mu m \)) and off state (\( V_G = -6 \) V) resistance by fitting edge roughness parameter \( \sigma_e = 15^\circ \). We see a mismatch between our simulation and experiment at \( V_G \sim 0 \) V due in our semiclassical simulation model. The local gate dielectric (hBN) thickness is 32 nm, junction width \( d \) is 70 nm, temperature is 50 K, and device width is 1 \( \mu m \) unless otherwise mentioned. The main advantage of ray tracing over the Non-equilibrium Greens function (NEGF) formalism is its computational practicality.

We now discuss the impact of gate geometry on various flavors of ballistic, perfect edge GKT transistors, as quantified by their low-bias resistances and on-off ratios. Figure 4A shows the results of the low-bias on and off state resistances for each geometry. The back gate voltage is kept fixed to \( V_{BG} = 100 \) V (corresponding to charge density \( n_1 \sim 6.63 \times 10^{12} \) cm\(^{-2} \) for SiO\(_2\) thickness of 300 nm in addition to 32 nm hBN) for all these devices while we sweep the local gate \( V_G \) to vary the corresponding charge density of middle gate region (\( n_2 \)) from negative (p-type) to positive (n-type), giving us the off and on states respectively. Our first structure, an SJ device (Fig. 3A) filters out carriers at angles other than normal incidence, exhibiting Klein tunneling. Adding another junction aligned to the first one (Fig. 3B, DJ) does not help in increasing on-off ratio significantly, but instead adds another comparable resistance along the path. With a tilted second junction (Fig. 3C, DJT with \( \delta = 45^\circ \)), we can achieve orders of magnitude larger off state resistance for ballistic flow. Next the TG device (Fig. 3D) uses the second junction to reflect back strongly collimated carriers towards the source away from the edges. However, it has a poorer performance in the off state than DJT structure because it allows electrons to Klein tunnel through its vertex on the first try. The DS device [17] (Fig. 3E) has an overall L-shape, so that each segment of the split source recaptures carriers injected from the other segment and rejected by the tilted junction, without letting them bounce again at the edges. As a result, its off state performance is superior to the DJT device. Finally, the EL (Fig. 3F) device capitalizes on a structure that is free from edge effects. In the EL structure shown, electrons enter along one axis from both sources, while the drains are along a perpendicular axis with the gate induced p-n junctions sitting in between. Such EL structures reduce the off current because most electrons incident at the junction are at large angles. Compared to an ideal DJT device, the off state resistance is still low as it uses only one junction. Moreover, the on state current of the EL, determining its device speed, is compromised by the right angle separating source and drain - moving the drain away from the natural ‘line of sight’ of the injected source electrons. The low on current degrades the overall on-off ratio of the EL device.
with increasing edge roughness. Contact resistance (\(117 \, \Omega\)) for different geometries. (A) Low-bias resistance characteristics of DS device (experiment).

In a DS device, transport gap turns in to a pseudo gap having higher nonzero floor value due to additional leakage path. (B) With increasing edge roughness, the on-off ratio degrades significantly. Im-
 triggering transport gap in SJ and DJ, but in the presence
of an order of magnitude increment in \(r_{\text{out}}\) (output resistance) without hurting the mobility. Devices like this with high mobility and output resistance can be quite useful for analog RF applications, delivering a high \(f_T\) (unity current gain cutoff frequency) and \(f_{\text{max}}\) (unity power gain cutoff frequency) [7]. To improve device performance, a super-lattice potential may be incorporated into the device to create an anisotropic band structure and create a much more aggressive collimation of electrons [27, 28]. Further improvements may be possible with abrupt junctions if doping can be improved in the first region, so that the reflected electrons at the second junction are no longer stopped by an abrupt first junction on their way to the source (recall that total internal reflection only works one way like a diode, from a denser to a rarer medium). A major factor in determining the overall performance of all these structures is edge roughness, included here as a phenomenological parameter, the standard deviation \(\sigma_e\) of a Gaussian angular smear. The relationship between \(\sigma_e\) and physical roughness parameters, as well as decay rates extracted from magnetoconductance measurements is out of scope of this study and will be reported elsewhere.

As a transistor, a ballistic GKT greatly outperforms wave-guided structures based on the Veselago effect. However, even a GKT faces challenges arising from the presence of edges - in particular rough ones, together with contact resistance and finite doping of graphene by metal contacts. A 1 \(\mu\text{m}\) wide structure with perfect edges is predicted to have a gate transfer characteristic with an on-off ratio \(\sim 10^2\), but current technology limits the edge smoothness and degrades the on-off ratio to \(\sim 10\), demonstrated experimentally [17]. Such a low on-off ratio is not yet suitable for digital logic.

The output characteristic, however, bears more promise. At high drain bias (\(V_{DS}\)), a small transport gap (\(n^-\text{n-n}^+,\) on state) at energies far from the equilibrium Fermi level is predicted to produce a strongly saturating \(I_D-V_D\) that is robust against edge roughness [7]. Even cases with an on-off ratio \(\sim 10\) can result in an order of magnitude increment in \(r_{\text{out}}\) (output resistance) without hurting the mobility. Devices like this with high mobility and output resistance can be quite useful for analog RF applications, delivering a high \(f_T\) (unity current gain cutoff frequency) and \(f_{\text{max}}\) (unity power gain cutoff frequency) [7]. To improve device performance, a super-lattice potential may be incorporated into the device to create an anisotropic band structure and create a much more aggressive collimation of electrons [27, 28]. Further improvements may be possible with abrupt junctions if doping can be improved in the first region, so that the reflected electrons at the second junction are no longer stopped by an abrupt first junction on their way to the source (recall that total internal reflection only works one way like a diode, from a denser to a rarer medium). A major factor in determining the overall performance of all these structures is edge roughness, included here as a phenomenological parameter, the standard deviation \(\sigma_e\) of a Gaussian angular smear. The relationship between \(\sigma_e\) and physical roughness parameters, as well as decay rates extracted from magnetoconductance measurements is out of scope of this study and will be reported elsewhere.

In summary, the performance challenges of a GKT transistor are outlined in this paper. Although junction line-edge roughness [29] and other scattering events are expected to play a role, we focused here on edge roughness that is expected to be the most deleterious to the on-off ratio through momentum redirection. We quantified the role of graphene-edge roughness and attempted to design around it, such as the EL device. We analyzed a family of devices and find that TG, DS_{imp} and EL device are less susceptible to edge roughness. We further showed that an angle of 45\(^\circ\) between collimator and re-
flector gives the best performance even in the presence of edge roughness. Our analysis shows that even with geometry optimization the on-off ratio may not be enough for scaled digital switching, but may still offer advantages for high frequency RF analog applications [7].

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S1. SIMULATION METHOD

Semiclassical ray tracing model relies on the assumption that the most relevant quantum effects in GKT devices manifest during tunneling at the junctions, while for large-scale devices with rough edges, interference effects are expected to be washed out under the gated regions. Accordingly, we throw electrons from a source with random injection angles following a cosine distribution function [S1], and evolve each electronic trajectory with constant speed $v_F$ (Fermi velocity) and band effective mass, $m = (E_F - qV)/v_F^2$, following classical trajectories. The transmission probability ($T$) of electrons at the junction is calculated [4, 21] using

$$T(E_F, \theta_1) = \begin{cases} \Theta(\theta_C - \theta_1) \frac{\cos(\theta_1) \cos(\theta_2)}{\cos^2\left(\frac{\pi d}{2\lambda_f}\right)} e^{\frac{-\pi d k_{F1} k_{F2}}{k_{F1} + k_{F2}} \sin(\theta_1) \sin(\theta_2)}, & \text{for p-p’ or n-n’} \\ \Theta(\theta_C - \theta_1) \frac{\cos(\theta_1) \cos(\theta_2)}{\cos^2\left(\frac{\pi d}{2\lambda_f}\right)} \exp \left[ -\pi d k_{F1} k_{F2} \sin(\theta_1) \sin(\theta_2) \right], & \text{for p-n’ or n-p’} \end{cases}$$

(S1)

where $\theta_1$ and $\theta_2$ are the incident and refraction angle, $\theta_C$ is the critical angle from Snell’s Law, $d$ is the junction width, and $k_{F1}$ and $k_{F2}$ are the Fermi wave vectors on the incident and transmitted side respectively.

Assuming non-interacting charge carriers, we consider a fraction $T$ of each electron at the junction that passes through, while a fraction $1-T$ is reflected back to the incident region. The trajectories of the reflected and transmitted fractional electrons are allowed to evolve once again through multiple such transmission-reflection events until they end up either at the source or the drain. The average transmission probability ($T_{ij} = N_j/N_{Total}$) from contact $i$ to contact $j$ is calculated by counting electrons ($N_j$) that eventually make it to the contact $j$ for a given total number $N_{Total}$ of carriers injected from contact $i$. Thereafter the Landauer-Büttiker formalism at low-bias is used to calculate channel conductance ($G_{Ch}$) by summing up the terminal transmissions.

$$G_{Ch}(E_F) = \frac{4e^2}{h} \int M(E)T(E) \left( -\frac{\partial f_0}{\partial E} \right) dE$$

(S2)

where $E_F$ is the Fermi energy, $M$ is the number of modes, $T$ is the sum over all transmissions, and $f_0 = f(E - E_F)$ is the equilibrium Fermi function.

S2. GEOMETRY IMPROVEMENT OF DOUBLE SOURCE (DS) DEVICE

The main motivation behind DS device in Ref. [17] was to use only junction in filtering procedure at the local gated region. In Fig. S1A, we can clearly see that this region is not free from edges and can be further optimized. Fig. S1B shows the structure ($DS_{imp}$) to improve the device performance in presence of edge roughness. $L_{ext}$ is kept to have feasible smooth electrostatics for both junction and reduce leakage path at the corners. Figure S1C shows comparison between DS and $DS_{imp}$ structure in terms of on-off ratio and we clearly see that $DS_{imp}$ is less sensitive to edge roughness.
FIG. S1. **Improving DS device geometry.** (A) Device structure from Ref. [17]. (B) Improved device structure (DS$_{\text{imp}}$) to reduce edge roughness for reflected electrons from second junction. Ideally, the local gate should be restricted within the triangle enclosed by green dash line to make the region free from edges and electrons can be redirected to the other source by second junction shown by white dash lines. However, it is impossible to maintain smooth potential at the corners. Therefore, the left and bottom sides are kept extended ($L_{\text{ext}} = 100$ nm). (C) Comparison of on-off ratio of DS vs. DS$_{\text{imp}}$. DS$_{\text{imp}}$ shows less sensitivity to edge roughness.

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