Practical Dynamic SC-Flip Polar Decoders: Algorithm and Implementation

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Abstract—SC-Flip (SCF) is a low-complexity polar code decoding algorithm with improved performance, and is an alternative to high-complexity (CRC-aided SC-List (CA-SCL) decoding. However, the performance improvement of SCF is limited since it can correct up to only one channel error ($\omega = 1$). Dynamic SCF (DSCF) algorithm tackles this problem by tackling multiple errors ($\omega \geq 1$), but it requires logarithmic and exponential computations, which make it infeasible for practical applications. In this work, we propose simplifications and approximations to make DSCF practically feasible. First, we reduce the transcendental computations of DSCF decoding to a constant approximation. Then, we show how to incorporate special node decoding techniques into DSCF algorithm, creating the Fast-DSCF decoding. Next, we reduce the search span within the special nodes to further reduce the computational complexity. Following, we describe a hardware architecture for the Fast-DSCF decoder, in which we introduce additional simplifications such as metric normalization and sorter length reduction. All the simplifications and approximations are shown to have minimal impact on the error-correction performance, and the reported Fast-DSCF decoder is the only SCF-based architecture that can correct multiple errors. The Fast-DSCF decoders synthesized using TSMC 65nm CMOS technology can achieve a 1.25, 1.06 and 0.93 Gbps throughput for $\omega \in \{1, 2, 3\}$, respectively. Compared to the state-of-the-art fast CA-SCL decoders with equivalent FER performance, the proposed decoders are up to 5.8× more area-efficient. Finally, observations at energy dissipation indicate that the Fast-DSCF is more energy-efficient than its CA-SCL-based counterparts.

Index Terms—Polar codes, 5G, energy efficiency, Dynamic SCFlip, wireless communications, hardware implementation.

I. INTRODUCTION

The 5th generation wireless mobile communications standard (5G) creates a vast infrastructure that enhances the existing communications platforms and enables new technologies. Among the 5G use cases, massive machine-type communications (mMTC) [1] prioritize enhanced connectivity and energy efficiency.

Polar codes are a class of forward error-correcting codes that asymptotically achieve the channel capacity [2]. They have been selected as the coding scheme for the control channel for 5G eMBB [3], and are being evaluated for 5G URLLC and mMTC use cases [4, 5]. Even though the successive cancellation (SC) decoding algorithm of polar codes enables to prove the capacity achieving property, its error-correction performance is mediocre at practical code lengths.

In order to improve the error correction performance of polar codes, SC-List (SCL) decoding was proposed [6]. SCL uses $L$ SC decoders in parallel to maintain a list of candidate codewords which improves the error-correction performance at the cost of increased implementation complexity [7]. SC-Flip (SCF) decoding [8] is another SC-based polar decoder algorithm that uses several SC decoding attempts when an initial SC decoding fails due to a single channel-induced error. Compared to SC decoding, SCF has improved error-correction performance at the cost of variable decoding latency. The average computational complexity of SCF decoding is similar to that of SC decoding at medium-to-high signal-to-noise ratio (SNR) regions. However, the improved performance with the SCF decoding is limited and can only match to its SCL counterparts with small list sizes. The limited performance improvement of the SCF is due to two main issues. The first problem is that SCF cannot correct more than one channel-induced error. The second problem is that the metric used to identify the error is suboptimal.

Dynamic SC-Flip (DSCF) decoding [9] proposes a solution to address both of these problems, by extending the search to more than one channel-induced errors, and by proposing an enhanced metric that is significantly more efficient on locating the erroneous locations in the codeword. In return, the logarithmic and exponential calculations involved in the DSCF decoding make it challenging for practical hardware implementations.

Our goal in this work is to make the DSCF algorithm practically feasible, so that it can be implemented in hardware at low cost to become an alternative for existing high-performance polar decoder architectures. State-of-the-art decoder architectures for polar codes either require substantial amount of resources (e.g. Fast-SSCL decoding [10]), or have limited error-correction performance improvement (e.g. Fast-SCF decoding [11]). Accordingly, our contributions are summarized as follows:

- First, we show that the logarithmic and exponential computations in the DSCF algorithm can be replaced by a simple constant approximation. We show that the proposed approximation does not incur any significant loss in error-correction performance.
- Then, we propose novel methods to implement decoding of special nodes under DSCF algorithm. We reformulate the original computations of the DSCF decoding to accommodate special nodes, and we show that it is possible to maintain similar error-correction performance. Moreover, we show that the achievable error-correction performance
can in fact be improved with one of the special nodes.

- We show how to reduce the computational complexity further associated with two special nodes. Using a mathematical framework, we first find the theoretical frame-error rate (FER) for these special nodes with and without error-correction. Then, we show the achievable performance approximations when the computational effort in these nodes are intentionally reduced. Under the light of these findings, we limit the computational effort in the hardware architecture that follows.

- Finally, we show how to implement the proposed Fast-DSCF algorithm in hardware. The proposed hardware takes advantage of all the proposed simplifications. In addition, we present further simplifications, such as metric normalization and sorter length reduction. There are several SCF-based algorithms that describe multiple bit-flipping operations, but to the best of our knowledge none of them describe a hardware architecture. Therefore, the proposed Fast-DSCF decoder is the first reported SCF-based decoder architecture that can correct more than a single-channel-induced error.

Simulation results show that Fast-DSCF decoder using all the simplifications, approximations and quantizations maintains similar error-correction performance to the baseline DSCF-based SC decoder with up to 65% reductions in TSMC average computational complexity similar to that of a single SCL-based decoder. Synthesis results in TSMC 65nm CMOS technology show that the proposed Fast-DSCF decoders is able to achieve an average throughput of up to 1.25 Gbps, while being up to 5.8x more energy-efficient compared to the fast CA-SCL decoders with equivalent FER performance. Finally, observations at the increase trends in energy consumption with improved performance indicate that the Fast-DSCF is more energy-efficient than its CA-SCL-based counterparts.

The structure of this paper is as follows: Preliminaries are described in Section II. Approximations to replace the transcendental computations in DSCF decoding are explained in Section III. Fast decoding techniques for DSCF decoding are detailed in Section IV. Reducing the computational effort for fast decoding techniques is discussed in Section V. The hardware architecture for the Fast-DSCF decoding is explained in Section VI followed by simulation and implementation results in Section VII. Conclusions are drawn in Section VIII. Note that, a portion of this study has been discussed previously in [12].

II. PRELIMINARIES

Vectors and matrices are denoted with bold letters (v), an index of a vector is denoted with a subscript (vi), a range of indices from i to j for a vector is denoted as v[i,j]. For LLRs (L) and partial sums (β) at decoding tree stage S are denoted using a superscript (LS, BS). Eωdenote the set of bit-flipping indices for the DSCF algorithm, and Lω|Eω denote the LLR at stage S and at index i when the decisions at indices in Eω are flipped.

![](image.png)

Fig. 1. Successive cancellation decoding tree for PC(16, 8). LLR (L) and partial sum (β) vectors of parent node v and of child nodes are represented with superscripts that indicate the direction (l for left, r for right) and not with their in-text superscripts for simplicity. Stages (S) for each level and the sub-codes with special frozen bit-patterns (Rate-0, Rate-1, Rep, SPC) are outlined for reference.

A. Polar Codes

A polar code PC(N, K) splits N channels into K reliable ones that are used to transmit the information bits, and N − K unreliable ones, which are frozen to a known value (usually to 0). The set of frozen and non-frozen indices are denoted with A̅C and A, respectively. The encoding of a polar code is a linear transformation, such that x = uG⊗n, where x is the encoded vector, u is the message vector, and the generator matrix G⊗n is the nth Kronecker product (⊗) of the polar code kernel G = [I | I] and n = log2 N, n ∈ Z+. The decoding schedule of SC can be interpreted as a binary tree search that starts from the root node (that contains the channel observation), and with priority given to the left branch. An illustration of the SC decoder tree is shown in Fig. 1 for PC(16, 8). Each stage in the tree is defined by the inverse of its depth from the root node, which is denoted by S where 0 ≤ S ≤ n. Each node contains Nv = 2S soft information, interpreted in log-likelihood ratio (LLR) form (LS) that are propagated to their child nodes. In return, each child node propagates Nv hard information (βS) to their parent nodes, called partial sums. As illustrated in Fig. 1 from a node v that has L̂v LLRs, the LLRs at the left child (L̂l) and the right child (L̂r) are calculated as

\[
L̂l_i = \text{sgn}(L^v_i) \text{sgn}(L^v_{i+2^{S-1}}) \min(|L^v_i|, |L^v_{i+2^{S-1}}|),
\]

\[
L̂r_i = L^v_i + (1 - 2\beta^v_i)L^v_i.
\]

Given that the hard decision information from the left child (β̂l) and the right child (β̂r) of node v are available, the β̂v for node v is calculated as

\[
\beta^v_i = \begin{cases} 
\beta^v_i \oplus \hat{\beta}^v_i, & \text{if } i \leq 2^{S-1} \\
\beta^v_{i-2^{S-1}}, & \text{otherwise}.
\end{cases}
\]

The bit estimations are performed at leaf node stage S = 0 sequentially, starting from the leftmost index. Estimation of each bit ūi depends on the channel observation y and previously decoded bits ū0:i−1, such that

\[
\hat{u}_i = \begin{cases} 
0, & \text{if } \Pr[y, \hat{u}_{0:i-1}|u_i = 0] \geq \Pr[y, \hat{u}_{0:i-1}|u_i = 1]; \\
0, & \text{if } i \in A̅C; \\
1, & \text{otherwise}.
\end{cases}
\]
It was shown in [13] and [14] that nodes in the SC decoding tree with special frozen bit patterns are not needed to be explicitly traversed; dedicated fast decoding techniques for such special nodes improves the throughput of the decoding substantially. Among these special nodes, decoding of Rate-0 (where all indices are frozen) Rate-1 (where no indices are frozen), repetition (Rep, where only the rightmost index is non-frozen) and single-parity check (SPC, where only the leftmost index is frozen) are within the scope of this work. An example for each of the considered nodes are highlighted with the dashed lines in Fig. 1.

B. SC-Flip and Dynamic SC-Flip Decoding

In a failed SC decoding, the incorrect bit estimations (e.g. errors) could occur in two different ways. The first way is due to the noise present in the channel, this type of errors is called a channel-induced error. The second way to incur an error is due to a previously made error during the sequential schedule of SC decoding [4], which we call a propagated error. Since the first error in the codeword cannot be propagated from a previously made error, it is a channel-induced error. Therefore, if this error is found and corrected, then its associated propagated errors – if there are any – also disappear. In this context, while propagated errors are dependent on their associated channel errors, the channel errors are independent from one another.

The observation above was originally made in [8], and it was also observed that most of the decoding failures are due to a single channel-induced error. Hence, if a single channel-induced error was avoided, then the error-correction performance would improve. Aided by an outer cyclic redundancy check (CRC) code for detecting whether an initial SC decoding has failed, SCF decoding first creates a list of bit-flipping positions using non-frozen leaf indices sorted according to their LLR magnitudes. Then, the SC decoding process is relaunched but the hard decision at the index that holds the last index of \( E \) is flipped. This is repeated until no errors are detected or until all positions in the list have been considered. When SCF decoding fails, it is either due to: (i) a wrong codeword with a valid CRC, or (ii) not locating the correct erroneous index within a maximum number of additional attempts \( T_{\text{max}} \), or (iii) having more than one channel-induced error in the codeword.

The performance improvement in error-correction introduced by the SCF decoding algorithm is limited due to two different problems. The first problem is that the SCF algorithm cannot correct more than a single channel-induced error. Even though several attempts lead to improvements in the SCF decoding [15]–[19], they are unable to tackle more than one channel-induced error. An alternative approach that segments the codeword into multiple partitions, and applying SCF decoding to each partition separately is also shown to have limited performance improvements [20]–[22]. The second problem is that the decision metric used in the SCF decoding is not able to distinguish channel-induced errors from propagated errors. Indeed, we have observed that the propagated errors may also carry small LLR magnitudes [16] which is the only parameter that the SCF decoding relies on for identifying channel-induced errors.

The proposals that address the limited performance improvement problem of SCF decoding in the literature can be classified into two different techniques. The first technique is to merge the SCF algorithm with the SCL algorithm [23]–[25]. This approach has shown to improve the decoding performance at the cost of an increased computational complexity. The second technique is to create combinations of bit-flipping positions to tackle more than one channel induced error [9], [26]–[31]. Among these, the Dynamic SCF (DSCF) algorithm [9] tackles both of the problems associated with the SCF decoding simultaneously: (i) the search for bit-flipping is not limited to a single channel-induced error, and (ii) the decision metric is more efficient in identifying the correct bit-flipping positions than the SCF algorithm.

To identify more than one channel-induced error, DSCF updates the set of flipping indices progressively over the course of each decoding attempt: Let \( \mathcal{E}_\omega = \{i_1, \ldots, i_\omega\} \) denote the set of bit-flipping indices at an additional decoding attempt, where \( i_1 < \cdots < i_\omega \) and \( 0 \leq \omega \leq K + C \). Note that here, \( C \) is the CRC remainder length. In this sense, \( \omega \) is the number of attempted channel-induced errors, which is referred to as the decoding order. \( \mathcal{E}_\omega \) is built progressively over a prior additional decoding attempt with \( \mathcal{E}_{\omega-1} = \{i_1, \ldots, i_{\omega-1}\} \).

Unlike in the SCF decoding, the decision metric of DSCF decoding for non-frozen indices does not only depend on their LLR magnitudes. Instead, all the decisions that were made at the prior non-frozen indices are also considered to calculate a more comprehensive decision metric. In this sense, let \( \Pr(\mathcal{E}_\omega) \) be the probability of SC decoding being successful after flipping the bits in \( \mathcal{E}_\omega \). It was shown in [9] that \( \Pr(\mathcal{E}_\omega) \) can be formulated as

\[
\Pr(\mathcal{E}_\omega) = \prod_{j \in \mathcal{E}_\omega} p_e(\hat{u}[\mathcal{E}_{\omega-1}]_j) \times \prod_{j < \omega, j \in \mathcal{A} \setminus \mathcal{E}_\omega} (1 - p_e(\hat{u}[\mathcal{E}_{\omega-1}]_j)) \tag{5}
\]

where \( p_e(\hat{u}[\mathcal{E}_{\omega-1}]_j) \) is the probability of incurring an error at index \( j \), such that

\[
p_e(\hat{u}[\mathcal{E}_{\omega-1}]_j) := \Pr(\hat{u}[\mathcal{E}_{\omega-1}]_j \neq u_j | y, \mathcal{E}_{\omega-1} = u_{0:j-1} = u_{0:j-1}). \tag{6}
\]

Let us elaborate on the computation of (5) with a simple example. Assume that the estimations \( \hat{u}_7 \) and \( \hat{u}_{12} \) in the PC(16, 8) polar code in Fig. 1 have channel-induced errors. Let a specific \( \mathcal{E}_\omega \) include the erroneous indices, i.e. \( \omega = 2 \) and \( \mathcal{E}_2 = \{7, 12\} \). By the successive course of the decoding, \( \hat{u}_7 \) is flipped first. The probability of a bit-flip at index 7 yielding the correct decision is equal to the probability of index 7 incurring a channel-induced error originally. The bit estimations that follow (i.e. at indices 9, 10, 11) are impacted by the first bit-flip and therefore denoted as \( \hat{u}[\mathcal{E}_1]_j \). Consequently, their associated probability of correct estimation are represented as \( (1 - p_e(\hat{u}[\mathcal{E}_1]_j)) \). Finally, the probability of error at the last index of \( \mathcal{E}_2 \) (which is index 12), is the same as the probability of incurring an error when it is not corrected, which is \( p_e(\hat{u}[\mathcal{E}_1]_{12}) \). The product of all these probabilities creates...
the probability of the successful decoding after flipping the indices of $E_w$, which is summarized in (5).

It can be seen in (6) that $p_e(\hat{u}|E_{w-1})$, depends on all the previous bits decoded correctly, which cannot be granted in practice. Hence, an approximation to $p_e(\hat{u}|E_{w-1})$, that depends on all the previously decoded bits, regardless of them being correctly decoded, can be used instead:

$$q_e(\hat{u}|E_{w-1}) = \frac{1}{1 + \exp(\langle L_0^w|E_{w-1} \rangle)}, \forall j \in A$$  \hspace{1cm} (7)

where $L_0^w|E_{w-1}$ is the LLR at index $j$ of the current decoding attempt. Hence, approximating (6) with (7) and thus substituting (7) into (5) yields the decision metric $m$ for the bit-flipping set $E_w$:

$$m(E_w) = \prod_{j \in E_w} \frac{1}{1 + \exp(\langle L_0^w|E_{w-1} \rangle)} \prod_{j \in E_w, j < \omega} \left(1 + \exp(\langle L_0^w|E_{w-1} \rangle)\right)$$

Using the fact that $\frac{1}{1 + \exp(x)} = \frac{\exp(-x)}{1 + \exp(-x)}$ (8) can also be written as

$$m(E_w) = \prod_{j \in E_w} \exp(-\langle L_0^w|E_{w-1} \rangle) \prod_{j \in E_w, j < \omega} \frac{1}{1 + \exp(-\langle L_0^w|E_{w-1} \rangle)}$$

For numerical stability, the metric is converted to the logarithmic domain using $M(E_w) = -\log(m(E_w))$ as

$$M(E_w) = \sum_{j \in E_w} \langle L_0^w|E_{w-1} \rangle + S(E_w),$$

where

$$S(E_w) = \sum_{j \in E_w} \log(1 + \exp(-\langle L_0^w|E_{w-1} \rangle)).$$

Finally, in order to approximate the value of $q_e(\hat{u}|E_{w-1})$, close to $p_e(\hat{u}|E_{w-1})$, a perturbation parameter $\alpha$ was defined in (9) and used, such that

$$M_\alpha(E_w) = \sum_{j \in E_w} \langle L_0^w|E_{w-1} \rangle + S_\alpha(E_w),$$

and

$$S_\alpha(E_w) = \frac{1}{\alpha} \sum_{j \in E_w} \log(1 + \exp(-\alpha\langle L_0^w|E_{w-1} \rangle)).$$

The value of $\alpha$ can be optimized via Monte-Carlo simulations [9] or machine learning [12].

The procedure of the DSCF decoding is summarized in Algorithm 1. Required inputs are the channel LLRs, maximum number of iterations $T_{max}$, maximum bit-flipping order $\omega$ and $A$. The received codeword is initially decoded with the SC algorithm (line 3). Here, the input for SCF algorithm is the bit-flipping indices, hence SCF with an empty input is equivalent to SC decoding. If the CRC on the estimated information bits fails and if there is room for additional bit-flips (line 4), then an initial list of bit-flipping indices are created using leaf LLRs (lines 5-8). Here, a special data structure ($V$) is used to encode the bit-flipping order ($v^w$), bit-flipping indices ($v^{\text{idb}}$) and the metric ($\omega$). The created vector of $V$ is then sorted with respect to their metric value (indicated with $\to$) in ascending order (line 9). Following, a series of decoding iterations is initiated that is conditioned on the CRC output and $T_{max}$ (lines 10-21). At each iteration, the decoding order and the bit-flipping indices are obtained from the next item in $V$ (lines 12-13). The used entry from $V$ is discarded from the list ($\text{pop}(\cdot)$ in line 14). The indices are used as an input to the new SCF decoding attempt (line 15). If the new decoding attempt allows for further bit-flipping investigations over the newly created decoding trajectory (line 16), then new bit-flipping indices are built on top of the current bit-flipping attempt (note the $E_w \cup \{i\}$ in line 20), and the updated vector is re-sorted before the next iteration begins. Here, the evaluated bit-flipping indices must be greater than the last index at $E_w$ (obtained by $\text{back}(\cdot)$ operation at line 18), following the definition of $E_w$. If the initial SC decoding has a valid CRC, or when at least one loop condition is broken, the bit estimation is reported (line 22).

To gain an in-depth theoretical background on the derivation of Algorithm 1 and the DSCF algorithm, the readers are strongly encouraged to refer to Section V-A and Section VI-A of [9], respectively.

\begin{algorithm}
\caption{Dynamic SCF Algorithm}
\begin{algorithmic}[1]
\Procedure{DSCF}{$y_{0..N-1}, T_{max}, \omega, A$}
\Initialize{$t \leftarrow 0$, $w \leftarrow 0$, $E_w \leftarrow \emptyset$, $V = \{v^w \leftarrow w; v^{\text{idb}} \leftarrow \emptyset; \omega \leftarrow +\infty\}$.}
\For{$(\omega \leftarrow \text{FRS}(\emptyset))$}
\For{$(i \in A)$}
\State compute $M_\alpha(E_i)$ (Eq. (11))
\EndFor
\EndFor
\If{$(\text{CRC}(\hat{u}_{0..N-1}, A) \& T_{max} > 0 \& \omega > 0)$}
\State $V_{\text{new}} \leftarrow \emptyset$
\For{$i \in A$}
\State compute $M_\alpha(E_i)$ (Eq. (11))
\EndFor
\State $V_{\text{new}} \leftarrow \text{pop}(V_0)$
\State $u_{0..N-1} \leftarrow \text{SCF}(E_w)$
\EndIf
\While{$(!\text{CRC}(\hat{u}_{0..N-1}, A) \& t < T_{max}$)}
\State $t \leftarrow t + 1$
\State $w \leftarrow V_0(v^w)$
\State $E_w \leftarrow V_0(v^{\text{idb}})$
\State $V_{\text{new}} \leftarrow \text{pop}(V_0)$
\State $u_{0..N-1} \leftarrow \text{SCF}(E_w)$
\EndWhile
\State $V_{\text{new}} \leftarrow \emptyset$
\For{$i > \text{back}(E_w), i \in A$}
\State compute $M_\alpha(E_{w+1})$ (Eq. (11))
\EndFor
\State $V_{\text{new}} \leftarrow \text{pop}(V_0)$
\State $u_{0..N-1} \leftarrow \text{SCF}(E_w)$
\EndIf
\State $V_{\text{new}} \leftarrow \emptyset$
\State $V_{\text{new}} \leftarrow \text{pop}(V_{\text{new}} \cup V \to \omega^{\text{idb}}, \text{ascending})$
\EndIf
\State return $u_{0..N-1}$
\EndProcedure
\end{algorithmic}
\end{algorithm}
builds a bit-flipping set exercise, the SCF algorithm is enhanced to tackle higher order errors when the SCF is modified to correct higher order errors, the aided decoder, called SC-Oracle (SCO) [8]. Observe that even in this sense, SCF with \( \omega \in \{1, 2, 3\} \) the decision metric of DSCF reverts to the SCF decoding with higher error order. Fig. 2 illustrates the differences in FER performance using the metric of SCF and DSCF, at error orders \( \omega \in \{1, 2, 3\} \) using \( PC(1024, 512) \) and \( C = 16 \). For this exercise, the SCF algorithm is enhanced to tackle higher order errors by updating the set of flipping indices progressively similar to that of DSCF algorithm. In other words, SCF builds a bit-flipping set \( E_\omega \), however it uses only the LLR magnitude values of the flipping indices while building it. In this sense, SCF with \( \omega = 1 \) is the original SCF decoding. For each error order, the dashed lines depict the ideal decoding performance when all \( \omega \) errors are corrected using a genie-aided decoder, called SC-Oracle (SCO) [8]. Observe that even when the SCF is modified to correct higher order errors, the associated performance improvement is fractional such that the FER of SCF with \( \omega = 3 \) is worse than that of DSCF with \( \omega = 1 \). This implies that the metric computation of DSCF algorithm is more efficient, and essential for tackling higher-order errors. On the other hand, although DSCF has superior error-correction performance due to the \( S_\alpha(E_\omega) \) term, its required logarithmic and exponential operations make DSCF inconvenient for efficient hardware implementations.

We reformulate \( S_\alpha(E_\omega) \) in (12) as

\[
S_\alpha(E_\omega) = \sum_{f \leq E_\omega} f_\alpha(|L^{0}[E_\omega-1]|),
\]

where

\[
f_\alpha(x) = \frac{1}{\alpha} \log \left( 1 + \exp(-\alpha x) \right).
\]

Following the Monte-Carlo optimizations from [9], \( \alpha = 0.3 \) is used throughout this paper. Interestingly, it was shown that a similar expression, \( f(x) = \log \left( 1 + \exp(-x) \right) \), used in the soft-input soft-output decoding algorithm of turbo codes, can be approximated in different ways without adversely affecting the decoding performance [33], [34]. Inspired from the constant log-MAP approximation in [33], we use a similar approximation to simplify \( f_\alpha(x) \) as:

\[
f_{\alpha=0.3}^*(x) = \begin{cases} \tfrac{x}{3}, & \text{if } |x| \leq 5 \\ 0, & \text{otherwise}. \end{cases}
\]

The values of \( \frac{x}{3} \) and 5 in (15) are selected to ensure both an easy future hardware implementation and a reduced fitting error. For illustration purpose, Fig. 3 plots the original function \( f_\alpha \) and its proposed approximation \( f_{\alpha=0.3}^* \), with \( \alpha = 0.3 \). Note that in [33], a linear approximation to \( f_\alpha \) was used following [34] to reduce its complexity. An illustration for the linear approximation is also depicted in Fig. 3 labeled as \( f_{\alpha=0.3}^{lin} \). However, our approach to approximate \( f_\alpha(x) \) is simpler as it only involves a constant value. Fig. 3 compares the FER performance of DSCF decoding with the constant and linear approximations against its original approach from [9], using length-1024 polar codes with different rates. The polar codes are constructed using the 5G reliability sequence [3]. The length-16 CRC defined in [3] is serially concatenated with the polar code. A BPSK modulation and an AWGN channel are considered. Note that the same settings are used for all the following Monte-Carlo simulations. Three error orders \( \omega \in \{1, 2, 3\} \) are targeted, corresponding to \( T_{max} \in \{10, 40, 200\} \), respectively. The decoding performance with SC-Oracle for each \( \omega \) value is also shown. Observe that in the considered cases, the approximated DSCF curves achieve similar decoding performance as the original approach but without transcendental computations. As the constant approximation is more favorable for reduced complexity, we choose to replace \( f_\alpha(x) \) with \( f_{\alpha=0.3}^*(x) \).

IV. FAST-DSCF DECODING

A. Achievable Performance by the Fast-SCF-based Decoders

We introduce the concept of Fast-SCO decoder to depict the ideal limit on the achievable performance by SCF-based decoders when special nodes that enclose more than one non-frozen index are incorporated. The modified SCO decoder works exactly as a Fast-SSC decoder, except that it is able to identify and correct up to a certain number of channel-induced errors at the top-level of the special nodes. The introduction of Fast-SCO is essential towards the performance evaluation of the proposed Fast-DSCF decoder.

The two special nodes of our interest, which involves more than a single non-frozen index, are Rate-1 and SPC nodes. Note that the FER value of Fast-SCO is the same as SCO.
In the following, we present how to perform the metric computations for each special node. Note that the following approaches can be applied to DSCF decoding with or without the approximation presented in Section III

Let us split the metric calculation of DSCF into two parts, such that:

\[
M_{\alpha}(E_{\omega}) = \left( \sum_{j \in E_{\omega-1}} |L^0_{\omega-1}[E_{\omega-1}]_j| + S_{\alpha}(E_{\omega}) \right) \cdot \frac{1}{M_{\alpha}''(E_{\omega})}.
\]  

Observe that \(M_{\alpha}'(E_{\omega})\) takes a value only if the index \(i_{\omega}\) is a candidate for bit-flipping during a future decoding iteration. \(M_{\alpha}'(E_{\omega})\) contains the instantaneous value at the index \(i_{\omega}\) and used for the metric computation of the index \(i_{\omega}\) only. On the other hand, \(M_{\alpha}''(E_{\omega})\) is the accumulative part that is used for the next possible set of bit-flips throughout the decoding attempt. \(M_{\alpha}''(E_{\omega})\) is set to 0 at the beginning of any extra decoding attempt and accumulated for each non-frozen leaf index \(j\) as follows:

\[
M_{\alpha}''(E_{\omega})_j = M_{\alpha}''(E_{\omega})_{j-1} + |L^0_{\omega-1}[E_{\omega-1}]_j| \quad \text{if } j \in E_{\omega-1}
+ f_{\alpha}(|L^0_{\omega-1}[E_{\omega-1}]_j|) \quad \text{if } j \in A.
\]  

We now provide a way to compute \(M_{\alpha}'(E_{\omega})\) and \(M_{\alpha}''(E_{\omega})\) when special nodes are encountered during DSCF decoding. First, we redefine the set \(E_{\omega}\) to hold the information of the special nodes as well as the flipping indices. Let us define the notation \(\{j, i\}\) as the coordinate in a polar code tree where \(j\) denotes the special node index and \(i\) denotes a set of top-node indices that belongs to \(j\). Accordingly, let \(E_{\omega} = \{j_1, i_1\}, \ldots, \{j_{\omega}, i_{\omega}\}\) denote the set of flipping coordinates at special nodes \(\{j_1, \ldots, j_{\omega}\}\) \((j_1 \leq \cdots \leq j_{\omega})\). In this context, a flipping coordinate \(\{j, i\}\) becomes a subset of the set \(E_{\omega}\). Depending on the type of the special node, the cardinality of \(i\) can vary. As we will see, the instantaneous component of the metric computation \(M_{\alpha}'(E_{\omega})\) depends on the subset \(\{j, i\}\), whereas the accumulative component \(M_{\alpha}''(E_{\omega})\) is updated at once at each special node \(j\).
The decoding of Rate-0 nodes for DSCF decoding is the same as [13] since their LLR magnitudes are not evaluated towards metric updates; this has been addressed previously in [36] for SCF-based algorithms.

Repetition (Rep) nodes contain a single non-frozen instance located at the rightmost index at the leaf node. From the top-level perspective, the information of the non-frozen index is distributed amongst all indices of the top node. In other words, the LLR in the last leaf node obtained through SC decoding is equal to the sum of all LLRs in the root node; and there is only one possible flipping-event. Therefore, for a Rep node \( j \) of size \( N_v \), at decoding tree stage \( S \), we can write

\[
M'_\alpha(\mathcal{E}_\omega)_{(j,\varnothing)} = \sum_{i \in N_v} L^S[\mathcal{E}_{\omega-1}]_i,
\]

and the update for \( M'_\alpha(\mathcal{E}_\omega) \) at a Rep node can be expressed as

\[
M''_\alpha(\mathcal{E}_\omega) = f_\alpha\left( \left| \sum_{i \in N_v} L^S[\mathcal{E}_{\omega-1}]_i \right| \right)
+ \left| \sum_{i \in N_v} L^S[\mathcal{E}_{\omega-1}]_i \right| \text{ if } \{ j, \varnothing \} \subset \mathcal{E}_{\omega-1}.
\]

If a flipping event for a Rep node is selected during an extra decoding attempt, all the \( N_v \) partial sums at level \( S \) have to be flipped. Accordingly, there is no index information required for Rep nodes \( (i = \varnothing \text{ in } \{ j, i \}) \). Note that the proposed metric calculation and update for Rep nodes are exact to the baseline DSCF decoding.

By definition, Rate-1 nodes do not involve any frozen bits. Thus, they correspond to an uncoded sequence and all the indices at the top of the node are evaluated for bit-flipping. We therefore use the top-level LLRs directly in metric calculations for the prospective flipping indices. For a Rate-1 node \( j \) of size \( N_v \), at decoding tree stage \( S \), \( M'_\alpha(\mathcal{E}_\omega) \) is calculated for each index \( i \) \( (0 \leq i < N_v) \) within the node, such that

\[
M'_\alpha(\mathcal{E}_\omega)_{(j,i)} = |L^S[\mathcal{E}_{\omega-1}]_i|.
\]

Note that, the LLR values at the top of a Rate-1 node do not have any dependencies on one another. Therefore, \( M''_\alpha(\mathcal{E}_\omega) \) is updated at once for the entire Rate-1 node, such that

\[
M''_\alpha(\mathcal{E}_\omega) = \sum_{i \in N_v} f_\alpha\left( |L^S[\mathcal{E}_{\omega-1}]_i| \right)
+ \left| \sum_{i \in N_v} |L^S[\mathcal{E}_{\omega-1}]_i| \right| \text{ if } \{ j, i \} \subset \mathcal{E}_{\omega-1}.
\]

If the flipping subset \( \{ j, i \} \) corresponds to a Rate-1 node at an additional decoding attempt, its top-node index \( i \) is flipped.

The proposed metric for Rate-1 nodes is not exact to the baseline DSCF decoding. In return, Fig. 6 depicts how the FER proceeds with \( T_{max} \), using two polar codes \( PC(1024, 512) \) and \( PC(1024, 896) \), evaluated at error orders \( \omega \in \{1, 2, 3\} \) and simulated at six different SNR points each. The non-frozen set \( A \) associated with these polar codes exhibit 95% and 99% of the indices that fall under Rate-1 nodes. It can be seen that the error-correction performance with Rate-1 nodes is similar to that of the original DSCF algorithm. In return, the decoding tree does not need to be traversed at Rate-1 nodes.

As mentioned in Section [IV.A], an even number of bit-flips have to take place at SPC nodes in order to keep their even parity constraint. Accordingly, for each attempted error order, two indices are considered, which leads to \( \binom{N_v}{2} \) combinations for an SPC node of size \( N_v \). Therefore, for an SPC node \( j \) of size \( N_v \), at decoding tree stage \( S \), \( M'_\alpha(\mathcal{E}_\omega) \) is calculated for each \( \{ j, i \} \) \( (i = \{i_1, i_2\}, 0 \leq i_1 < N_v, 0 \leq i_2 < N_v, i_1 \neq i_2) \), such that

\[
M'_\alpha(\mathcal{E}_\omega)_{(j,\{i_1,i_2\})} = \sum_{i \in \{i_1,i_2\}} \left( |L^S[\mathcal{E}_{\omega-1}]_i| - \gamma |L^S[\mathcal{E}_{\omega-1}]_{i_{\text{min}}} | \right),
\]

where \( i_{\text{min}} \) denotes the top-node index with the minimum LLR magnitude and \( \gamma \) is the initial parity.

As noted in (12), only the non-frozen index LLR magnitudes are used towards the calculation of \( S_\alpha(\mathcal{E}_\omega) \). Thus, the index \( i_{\text{min}} \) is excluded in the calculation of \( S_\alpha(\mathcal{E}_\omega) \) in SPC nodes. Instead, its LLR magnitude is applied as an offset to all other indices, such that

\[
M''_\alpha(\mathcal{E}_\omega) = \sum_{i \in N_v \setminus i_{\text{min}}} f_\alpha\left( |L^S[\mathcal{E}_{\omega-1}]_i| + (1 - 2\gamma)|L^S[\mathcal{E}_{\omega-1}]_{i_{\text{min}}} | \right)
+ \sum_{i \in \{i_1,i_2\} \setminus \{i_{\text{min}}\}} \left( |L^S[\mathcal{E}_{\omega-1}]_i| - \gamma |L^S[\mathcal{E}_{\omega-1}]_{i_{\text{min}}} | \right).
\]

If the flipping subset \( \{ j, i \} \) correspond to an SPC node at an additional decoding attempt, then the two top node indices
A. Reducing the Search Span in Rate-1 Nodes

Assuming an all-zero codeword with BPSK signaling, the LLRs can be expressed as Gaussian random variables, such that

\[ L_i^0 \sim \mathcal{N}(\mu_i, \sigma^2_i), i \in [0; N). \]  

(24)

As the variance \((\sigma^2)\) and the mean \((\mu)\) of the random variable model are coupled \((\sigma^2 = 2\mu)\), it is sufficient to track the mean for each channel \([37]\). Then, the probability of error \((\pi_i)\) associated with each leaf node index can be approximated by the Q-function \(Q(x)\), which is referred to as the tail probability of a Gaussian distribution. The Q-function can be described using the complementary error function \([38]\):

\[ \pi_i \approx Q \left( \frac{\mu_i}{\sigma_i} \right) = Q \left( \sqrt{\frac{\mu_i}{2}} \right) = \frac{1}{2} \text{erfc} \left( \sqrt{\frac{\mu_i}{2}} \right). \]  

(25)

Recall that \(\Pr(\mathcal{E}_\omega)\) is the probability of SC decoding being successful after flipping the indices in \(\mathcal{E}_\omega\) \([5]\). Here, let us define a slightly different probability, \(\Pr(\tilde{\mathcal{E}}_\omega)\), as SC decoding being successful after flipping \(\omega\) indices. Differently than \(\Pr(\mathcal{E}_\omega)\), \(\Pr(\tilde{\mathcal{E}}_\omega)\) does not involve a specific set of indices but only concerns the number of flipped indices. In this sense, when \(\omega = 0\), then \(\Pr(e_0)\) is the probability of SC decoding being successful, and can be expressed in terms of \(\pi_i\) as

\[ \Pr(e_0) = \prod_{i \in A} (1 - \pi_i), \]  

(26)

Accordingly, the FER of SC can be easily computed by taking the complement of \(\Pr(e_0)\) \([59]\), such that

\[ \text{FER}_{\text{SC}} = 1 - \Pr(e_0) = 1 - \left[ \prod_{i \in A} (1 - \pi_i) \right]. \]  

(27)

It is worth to mention that, the theoretical FER of SC when an error (or more) is corrected \((\omega > 0)\) can be derived similarly \((\text{e.g. } 1 - \Pr(e_0) - \Pr(e_1))\). However, the derived performance does not correlate well with the simulated performance. This is because of the propagated errors that occur at the leaf nodes. Since no systematic model is derived to explain the behavior of the propagated errors, they are assumed unpredictable. The correlation between channel errors and propagated errors have a negative impact on the accuracy of the performance estimation. This behavior was also addressed shortly in Section IV-B of \([2]\). On the other hand, we show that there is a way to estimate the performance for \(\omega > 0\) accurately for Rate-1 and SPC nodes.

In this Section, we attempt to reduce the search span for bit-flipping within Rate-1 and SPC nodes without introducing significant degradation in error-correction performance using a theoretical framework. This study is divided into three parts. First, we derive the theoretical FER bounds for Rate-1 nodes for any error order via density evolution using Gaussian approximation \([27]\). Then, we attempt to approach to the derived bounds using a reduced number of elements within the Rate-1 nodes. Finally, we extend our study towards SPC nodes.

Note that these derived theoretical computations are not exclusive to the DSCF algorithm, and can be used for other algorithms and purposes. This study is carried out using BPSK modulation, it can be extended to higher-order modulation scenarios.

V. REDUCING THE BIT-FLIPPING SEARCH SPAN IN FAST-DSCF DECODING

Fig. 7 compares the FER performance of our approach with SC nodes \([22, 24]\) against the baseline DSCF algorithm for \(\omega \in \{1, 2, 3\}\). As in the Rate-1 study, \(PC(1024, 512)\) and \(PC(1024, 896)\) are used: their associated non-frozen set exhibit 68% and 65% of the indices that fall under SPC nodes, respectively. For both polar codes, it is observed that their FER performance are able to reach lower FER values when SPC nodes are involved as outlined by the Fast-SCO estimation. This bevahior was also addressed shortly in Section IV-B of \([9]\). On the other hand, we show that there is a way to estimate the performance for \(\omega > 0\) accurately for Rate-1 and SPC nodes.

Based on \([27]\), the FER for a Rate-1 node under SC decoding can be derived using its top-node LLRs rather than its leaf node LLRs, by exploiting the fact that there are no frozen (parity) bits involved \([28]\). This means that, the FER computation of a Rate-1 node can also be computed using the top-node LLRs instead of using its leaf node LLRs. As such, for a Rate-1 node at stage \(S\) and of size \(N_v\), \([27]\) can be adapted into

\[ \text{FER}_{\text{Rate-1, SC}} = 1 - (1 - \pi^S)^{N_v}, \]  

(28)
where \( \pi^S \) is derived by substituting the mean value at stage \( S \) \((\mu^S)\) into \([25]\). Note that, this derivation is possible because all variables at the top-level of a node have the same mean and variance. Similarly, we can derive the FER for higher error orders for Rate-1 nodes. Unlike the case in SC, the theoretical FER for Rate-1 nodes is accurate if it is calculated using their top-node LLRs, because channel-induced errors at top-level indices does not yield error propagation. In other words, the independent top-node errors in Rate-1 nodes is the key for obtaining accurate theoretical FER calculation. For instance, for a Rate-1 node of size \( N_v \) and at stage \( S \), the probability of a channel-induced error at a top-node index is \( \pi^S \). To compute \( \text{Pr}(e_1) \), we must ensure that all other indices are error-free \((1 - \pi^S)^{N_v-1}\), and know that the channel error can occur in \( N_v \) different indices:

\[
\text{Pr}(e_1) = N_v \times \pi^S(1 - \pi^S)^{N_v-1}.
\]

The FER for a Rate-1 node with correcting one error at the top-level can be expressed as \(1 - \text{Pr}(e_0) - \text{Pr}(e_1)\):

\[
\text{FER}_{\text{Rate-1,}\omega=1} = 1 - \left((1 - \pi^S)^{N_v}\right) - \left(N_v \times \pi^S(1 - \pi^S)^{N_v-1}\right).
\]

To generalize, the probability of error for a Rate-1 node of size \( N_v \) at a target error order \( \omega \) can be expressed as

\[
\text{FER}_{\text{Rate-1,}\omega} = 1 - \sum_{i=0}^{\omega} \text{Pr}(e_i), \quad (29)
\]

which can be expanded into

\[
\text{FER}_{\text{Rate-1,}\omega} = 1 - \sum_{i=0}^{\omega} \left(\frac{N_v}{i}\right) \times \left(\pi^S\right)^i(1 - \pi^S)^{N_v-i}. \quad (30)
\]

As the theoretical achievable FER limit for Rate-1 nodes is identified as a function of \( N_v \), \( \omega \) and \( \mu^S \), we now attempt to approximate this with an artificially reduced size. We claim that the Rate-1 top-node indices with the lowest LLR magnitudes become far more susceptible to incur errors than others. Since the lowest LLR magnitudes at a parent node are propagated to its left child nodes using \([1]\), the FER of a Rate-1 node can be approximated by using its left child nodes instead of the root node. For example, the lowest LLR magnitude at the top of the Rate-1 node is also found at the leftmost leaf node \((S = 0)\), with a different mean value \( \mu^0 \). Similarly, the two lowest LLR magnitudes at the top of the Rate-1 node are also found at the leftmost node at \( S = 1 \) with mean value \( \mu^1 \). Accordingly, we use the size and mean values of the left nodes of a Rate-1 node to obtain an approximated achievable FER limit to the original one in \([30]\).

Let \( \delta \) denote the number of indices within a search span of a node which comprises the lowest LLR magnitudes at a Rate-1 node, where \( N_v \geq \delta \geq \omega \). If \( \delta < \omega \), then the number of errors cannot fit within the search span and a failed decoding is guaranteed. Accordingly, the achievable FER can be approximated as

\[
\text{FER}_{\text{Rate-1,}\omega} \approx 1 - \sum_{i=0}^{\omega} \left(\frac{\delta}{i}\right) \left(\pi^*\right)^i(1 - \pi^*)^{\delta-i}. \quad (31)
\]

where \( \pi^* \) is the mean value calculated by the mean of the leftmost child at stage \( S = \log_2 \delta \). It should be noted that a similar study has been carried out in \([23]\) but it is limited to \( \omega = 0 \) and \( \delta = 1 \), which cannot be used for higher order FER approximations.

Fig. 8 depicts the exact achievable FER for Rate-1 nodes \((30)\) compared to the approximated versions \((31)\) using four different \( \delta \) values, four different node sizes and four error orders. It can be observed that, the approximations follow a closer trend to the original \( \text{FER}_{\text{Rate-1,}\omega} \) with increasing \( \delta \). At large node sizes and higher error orders, the approximations begin to diverge from the original achievable FER but they may still be considered within an acceptable domain, at a wide range of mean values. A reduced bit-flipping search span will be introduced for Rate-1 nodes based on the presented approximations at Section VI.

B. Reducing the Search Span in SPC Nodes

At the top-level of an SPC node, all indices but one carry information and one bit carry the parity of all the other indices. This allows the SPC node to correct one erroneous index naturally, but certain conditions must be met. These conditions can be described as two probabilistic events: the probability of only one bit estimation is incorrect, and the probability of the incorrect bit containing the lowest absolute LLR value among all indices. If the incorrect bit does not have the lowest absolute LLR, then the correction mechanism of the SPC node causes an additional erroneous index instead of the correction. We denote the probability of a naturally correctable error with \( \text{Pr}(e^*_1) \).

The associated events are visualized in the Gaussian probability density function in Fig. 8 and explained next. Consider an SPC node of size \( N_v \) at stage \( S \) with top-level LLR values \( L_i^S \). Consider an all-zero codeword, a BPSK modulation and the AWGN channel. The probability of an SPC index \( i \) is erroneous and naturally correctable can be described as the probability of index \( i \) containing the LLR value of \( L_i^S = x \)
probability density function:

\[ f(x; \mu, \sigma) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}}, \quad x \in \mathbb{R}. \]  

On the other hand, the second event can be described in terms of a Q-function with mean value shifted by \( x \). Finally, since the two described events are statistically independent, we can apply \( \Pr(A \cap B) = \Pr(A) \times \Pr(B) \); leading to

\[ \Pr(e_i^*, L_i^S = x) = f(x; \mu, \sigma) \times \left[ 1 - Q\left(\frac{\mu + x}{\sigma}\right)\right]^{N_v - 1}. \]  

Finally, taking into account that the described event in (32) may occur at any index, and for any \( x < 0 \), we get

\[ \Pr(e_i^*) = \left(\frac{N_v}{1}\right) \int_{-\infty}^{0} f(x; \mu, \sigma) \left[ 1 - Q\left(\frac{\mu + x}{\sigma}\right)\right]^{N_v - 1} dx. \]  

Accordingly, the theoretical FER for an SPC node under SC decoding can be computed as:

\[ \text{FER}_{\text{SPC}, \omega = 0} = 1 - \Pr(e_0) - \Pr(e_1^*), \]  

where \( \Pr(e_0) \) and \( \Pr(e_1^*) \) can be substituted from (26) and (35). Now we show how to extend this computation for SPC nodes with higher error orders. Recall that two SPC indices are corrected per attempted error order. Hence, for \( \omega = 1 \), two channel-induced errors are corrected, and a third error if it is correctable by the parity check (\( \Pr(e_3^*) \)). For the all-zero codeword scenario, given that an SPC index \( i \) with an LLR value of \( L_i = x \) (\( x < 0 \)), the remaining two erroneous indices must have lower values than \( x \) and all other indices must have higher values than \( -x \) so that index \( i \) becomes correctable by the parity check. Considering all combinations of the described scenario and integrating for the range of \( x \) yields

\[ \Pr(e_3^*) = \int_{-\infty}^{0} f(x; \mu, \sigma) \left(\frac{N_v}{2}\right) Q\left(\frac{\mu + x}{\sigma}\right)^2 \times \left[ 1 - Q\left(\frac{\mu + x}{\sigma}\right)\right]^{N_v - 3} dx. \]  

Following (29), (36) and (37) the theoretical FER of SPC nodes for any error order can be generalized as follows:

\[ \text{FER}_{\text{SPC}, \omega} = 1 - \sum_{i=0}^{2\omega} \Pr(e_i) - \Pr(e_{2\omega+1}^*), \]  

where

\[ \Pr(e_{2\omega+1}^*) = \int_{-\infty}^{0} \left(\frac{N_v}{1}\right) f(x; \mu, \sigma) \left(\frac{N_v}{2}\right) Q\left(\frac{\mu + x}{\sigma}\right)^{2\omega} \times \left[ 1 - Q\left(\frac{\mu + x}{\sigma}\right)\right]^{N_v - 2\omega - 1} dx. \]  

Our next and final goal is to approximate to the theoretical FER trend lines of SPC nodes with a limited search span. To do this, we perform a similar approach to the study in Rate-1 nodes: A search span that comprises \( \delta \) lowest LLR magnitudes at an SPC node, where \( N_v \geq \delta \geq \max(2, 2\omega + 1) \), \( \delta \in \mathbb{Z}^+ \) is defined for SPC nodes. If \( \delta < \max(2, 2\omega + 1) \), then the number of errors cannot fit within the search span and a failed decoding is guaranteed. Accordingly, the achievable FER for SPC nodes within a limited search span can be expressed as

\[ \text{FER}_{\text{SPC}, \omega} \approx 1 - \sum_{i=0}^{2\omega} \left(\delta\right) \left(\frac{\pi^*}{\pi^*}\right)^{i} \left(1 - \pi^*\right)^{\delta - i} \times \int_{-\infty}^{0} f(x; \mu^*, \sigma^*) \left(\frac{\mu^* + x}{\sigma^*}\right)^{2\omega} \times \left[ 1 - Q\left(\frac{\mu^* + x}{\sigma^*}\right)\right]^{\delta - 2\omega - 1} dx. \]  

where \( \mu^* \) is obtained from the leftmost node at stage \( S = \log_2 \delta \), and \( \pi^* \) and \( \sigma^* \) are calculated using \( \mu^* \). 

Fig. 10 depicts the exact achievable FER for SPC nodes compared to the approximated version using three different \( \delta \) values where applicable, four different node sizes and three error orders. Similar observations to the case of Rate-1 nodes can also be made for the SPC nodes: Considered approximations follow a close trend to the exact derivation, with higher \( \delta \) values are in favor of a better approximation at the cost of higher search span. Similar to Rate-1 case, a reduced bit-flipping search span is created for SPC nodes based on the presented approximations at Section VI.
VI. HARDWARE ARCHITECTURE

The architecture for a typical SCF-based polar decoder comprises the following main components: An SC decoder core where the decoding iterations are carried out, a CRC unit that works in parallel with the SC core to validate the output, and a sorter datapath to collect and regulate the bit-flipping information for possible additional decoding attempts. For this work, the SC decoder core is derived from the Fast-SCF decoder reported in [11], which is based on a semi-parallel polar decoder architecture [40] with a parallelization factor of $P_c = 64$. Other than the branch operations, the modified decoder supports only Rep, Rate-1 and SPC instructions. Since Rate-0 nodes are always followed by a right branch (G) operation [1], Rate-0 nodes are merged with right branch operations to reduce latency [41]. A highly-parallelized CRC processor for the polynomial $x^{1021}$ is implemented after [42] to validate the decoder output.

Compared to the state-of-the-art Fast-SCF decoder architectures, the main difference of the proposed Fast-DSCF architecture is on the sorter datapath, which includes generation of the decision metrics for bit-flipping candidates, followed by sorting and storing of the candidates. The architecture for the proposed sorter datapath is visualized in Fig. [11].

A. Metric Normalization and Quantization

The $M'_n(\mathcal{E}_\omega)$ component of the decision metric is accumulative as mentioned in Section VI-B, which is not a desired property for quantization. When an accumulative component is quantized, it carries the risk of saturating over the course of the decoding, which disorganizes the sorted order of the bit-flipping indices and therefore may degrade the error-correction performance. One way to get around this problem is to increase the number of quantization bits at the cost of an increased latency, area and power consumption. Another way is to normalize the metric update by identifying and eliminating the computations that are performed more than once so that the risk of saturation could be minimized, as explained next.

Recall that the $M_\alpha(\mathcal{E}_\omega)$ is computed as described in (16), in which $M'_n(\mathcal{E}_\omega)$ is expressed as:

$$M'_n(\mathcal{E}_\omega) = \sum_{j \in \mathcal{E}_{\omega-1}} |L^0[\mathcal{E}_{\omega-1}]_j| + \sum_{j \leq \omega \leq \omega-1, \forall j \in A} f_\alpha(|L^0[\mathcal{E}_{\omega-1}]_j|).$$ (41)

Note that, a part of this computation can be found in the preceding metric $M'_n(\mathcal{E}_{\omega-1})$. Following (11) and (13), $M_\alpha(\mathcal{E}_{\omega-1})$ can be expressed as:

$$M_\alpha(\mathcal{E}_{\omega-1}) = \sum_{j \in \mathcal{E}_{\omega-1}} |L^0[\mathcal{E}_{\omega-2}]_j| + \sum_{j \leq \omega-1, \forall j \in A} f_\alpha(|L^0[\mathcal{E}_{\omega-1}]_j|).$$ (42)

Given that $L^0[\mathcal{E}_{\omega-2}]_j = L^0[\mathcal{E}_{\omega-1}]_j$ for $j \leq \omega-1$, $M'_n(\mathcal{E}_\omega)$ can be normalized by $M_\alpha(\mathcal{E}_{\omega-1})$:

$$M'_n(\mathcal{E}_\omega) - M_\alpha(\mathcal{E}_{\omega-1}) = \sum_{i \leq \omega-1, \forall j \in A} f_\alpha(|L^0[\mathcal{E}_{\omega-1}]_j|).$$ (43)

Therefore, the normalized $M'_n(\mathcal{E}_\omega)$ can be initiated at $0$ at the beginning of any extra decoding attempt and remains unchanged until the last flipped index, and is updated only after the last flipped index as:

$$M'_n(\mathcal{E}_\omega)_j = + f_\alpha(|L^0[\mathcal{E}_{\omega-1}]_j|) \text{ if } j \in A, j \geq \omega-1.$$ (44)

The normalization of $M'_n(\mathcal{E}_\omega)$ is not only in favor of quantization, but it also helps to reduce the computational effort by avoiding redundant calculations. Note that, this normalization procedure is extended to the computation of $M'_n(\mathcal{E}_\omega)$ at the special nodes that are detailed in [19], [21], [23] for the hardware implementation.

For quantization of Fast-DSCF decoding with $\omega = 1$, 5 bits and 6 bits are set for the channel and internal LLRs, respectively, with 1 bit reserved for the fractional part. A quantization of 5 bits for the metric is shown to be sufficient to obtain a well-approximated performance to the floating-point decoding. On the other hand, these quantization schemes are not shown to be sufficient for higher order decoding: one extra bit is required for the fractional part of the LLRs which impacts channel and internal LLRs, and the metric. Moreover, another extra bit is required for the metric to sort the bit-flipping indices efficiently. Hence, 6 and 7 bits are set for the channel and internal LLRs, and 7 bits are set for the metric quantization at $\omega > 1$.

B. Decision Metric Generation

The $M'_n(\mathcal{E}_\omega)$ and $M'_n(\mathcal{E}_\omega)$ components of the decision metric are generated simultaneously, then summed to acquire the desired $M_\alpha$ for each bit-flipping candidate. During the execution of each special node, their top-node LLR values (shown as $L$ in Fig. [11]) are forwarded to the decision metric generator with the associated control signals, such as the instruction, parity information, last flipping location (if any), and the stage size. The upper datapath in Fig. [11] visualizes the signal flow on the generation of $M'_n(\mathcal{E}_\omega)$: the $f_\alpha(x)$ function from (15) is applied to the absolute top-node LLRs, which are...
then summed together and forwarded to the register that holds the current \( M_\alpha^\omega (E_\omega) \). The \( M_\alpha^\omega (E_\omega) \) component of the metric is updated based on the rule described in (44), and the control signals are not shown for a simplified view. Following the discussions on reducing the bit-flipping search span from Section \( \text{V} \), the \( M_\alpha^\omega (E_\omega) \) component of the decision metric should only involve a predetermined number of indices. Following the studies in Fig. 8 and Fig. 10, we reduce the search span for Rate-1 and SPC indices to 2 and 4, respectively. It can be seen from Fig. 10 that limiting the search span to 4 for SPC nodes results in some performance degradation for larger node sizes at higher orders. On the other hand, increasing the search span for SPC nodes increases the complexity of the sorting process drastically. In order to minimize the performance degradation, the maximum size for SPC nodes are limited for higher order decoding. Namely, the maximum SPC node sizes are set to 8 and 4 for \( \omega = 2 \) and \( \omega = 3 \), respectively.

The lower path in Fig. 11 shows the \( M_\alpha^\omega (E_\omega) \) generation followed by the bit-flipping candidate generation. The \( \text{findmin}() \) function in Fig. 11 finds the four indices with the minimum LLR magnitudes, with which \( 2 \) and \( \frac{\lambda}{2} = 6 \) bit-flipping candidates are generated with their \( M_\alpha^\omega (E_\omega) \) values for Rate-1 and SPC nodes, respectively. The generated candidates are pre-sorted (\( \text{presort}() \)) in Fig. 11, which will greatly help with actual sorting process. The generated candidates are then assembled with the \( M_\alpha^\omega (E_\omega) \) component and with the current bit-flipping information (\( \text{join}() \)) in Fig. 11. Hence, up to six bit-flipping candidates are generated that are forwarded to the sorter architecture.

### C. Sorter Architecture

Since there is always at least one branch operation in between any two leaf node operations due to the sequential tree traversal \([41]\), the newly created sorting items can be processed in two clock cycles. Since up to six new sorting elements are created, up to three elements can be sorted at a clock cycle. This is achieved by inserting a dedicated shift register before the sorter architecture, that takes up to 6 elements and sends 3 elements to the sorter at a time.

Let us denote a sorting element by \( \lambda \), which contains the information of \( \{ \omega, M_\alpha^\omega (E_\omega), E_\omega \} \). The sorter architecture keeps an array of \( \lambda \) items, \( \Lambda \), with their metrics in increasing order. Let us further denote the newly generated sorting elements by \( \Lambda^* = \{ \lambda_0^*, \lambda_1^*, \lambda_2^* \} \). Note that the items in \( \Lambda^* \) are also sorted in increasing order due to the \( \text{presort}() \) function in Fig. 11. Since the length of \( \Lambda^* \) is far greater than the size of \( \Lambda^* \), together they form a nearly sorted array, that needs to be fully sorted. The insertion sort method is an algorithm that is in favor of nearly sorted lists \([43]\), therefore we create an insertion sorter that is able to insert up to three new elements in a single clock cycle. Fig. [12] depicts the proposed insertion sorter architecture for Fast-DSCF decoding: The elements can shift back up to three places based on the places of the newly inserted values. The elements are also capable of shifting forward by one place, which is performed at the beginning of an additional decoding iteration. That way, the current bit-flipping information is always stored at \( \lambda_0 \). Based on the normalization procedure described in Section \( \text{VI-A} \), the metrics at each element of the sorter are normalized by the metric value of the current \( \lambda \) (denoted as \( \lambda_0 (M) \)) every time the sorter shifts its elements forward.

With the increasing error order, the size of the sorter architecture increases in two dimensions: the cardinality of \( E_\omega \) within the sorting element (\( \lambda \)) increases and therefore more bits are required to describe a flipping event, and the length of the sorter increases linearly with \( T_{\text{max}} \). Hence, the complexity of the sorter increases dramatically with \( \omega \), requiring a substantial portion of the overall decoding architecture. To illustrate, for the Fast-DSCF decoder with \( \omega = 1 \) and \( T_{\text{max}} = 10 \), assuming 5 bits for metric quantization, 2 bits for order information, 9 bits for the special node and 6 bits for each stored index, 300 bits are required for the sorter. On the other hand, assuming the same quantization numbers, \( 5, 100 \) and \( 28,800 \) bits are required for the sorter for \( \omega = 3 \) with \( T_{\text{max}} = 400 \) and \( \omega = 2 \) with \( T_{\text{max}} = 100 \), respectively. In other words, the sorter complexity for \( \omega = 3 \) would be about 5 times of the LLR memory, and about 60 times of the partial sum memory. Therefore, it is essential to reduce the sorter complexity for higher error orders as much as possible.

For SCF architectures that feature \( \omega = 1 \) only and not higher order error-correction, the sorter length must match the \( T_{\text{max}} \) since the bit-flipping indices are calculated only once during the initial decoding attempt. On the other hand, for architectures that feature higher-order error-correction, the last elements at the sorter are most likely to be shifted out when the sorter gets updated with the higher-order bit-flipping information. Inspired from this event, we propose a sorter length \( l \leq T_{\text{max}} \). When \( l = T_{\text{max}} \), the error-correction performance of the Fast-DSCF algorithm is preserved. When \( l < T_{\text{max}} \), the original error-correction performance is not guaranteed; however, an opportunity is created to reduce the sorter length at the expense of a preferably negligible loss in error-correction performance. Accordingly, empirical studies with \( \omega = 2 \) and \( \omega = 3 \) have shown that setting the sorter length to 50% of the \( T_{\text{max}} \) value has minimal impact on error-correction performance, while it greatly helps with reducing the computational complexity of the decoder.

### VII. Results

The following results for the proposed Fast-DSCF decoder uses all the simplifications, optimizations and approximations discussed throughout this work. The constant approximation from \([15]\), and all the special node decoding techniques from \([18]-[23]\) are used. Furthermore, following the discussion in Section \( \text{V} \) the search span for Rate-1 and SPC nodes are
This work fast-SSCL-SPC [10], DSCF [9] and CRC-aided Fast-SSCL-SPC (Fast-SSCL) proposed Fast-DSCF decoding, against baseline DSCF decoder are set to 10, 100, 400 for $\omega \in \{1, 2, 3\}$ for both DSCF and Fast-DSCF decoders. The Fast-SSCL-SPC and the Fast-DSCF decoders are quantized, whereas DSCF decoder is simulated using floating-point.

- Reduced to 2 and 4, respectively. The maximum node size for SPC nodes is set to $\{64, 8, 4\}$ for $\omega \in \{1, 2, 3\}$, respectively. The metric normalization and quantization schemes following Section VI-A are employed. For both DSCF and Fast-DSCF decoders, $T_{\text{max}}$ values are set to 10, 100 and 400 for $\omega \in \{1, 2, 3\}$, respectively. The sorter lengths of the Fast-DSCF decoder are set to 10, 50 and 200 for $\omega \in \{1, 2, 3\}$, respectively. A FER value of $10^{-5}$ is targeted for comparison.

A. Error-Correction Performance

Fig. 13 presents the error-correction performance of the proposed Fast-DSCF decoding, against baseline DSCF decoding from [9] and CRC-aided Fast-SSCL-SPC (Fast-SSCL) decoding with $L \in \{2, 4, 8, 16\}$ [10], using $PC(1024, 512)$ and $C = 16$ from [8]. Note that the Fast-DSCF is simulated using the quantization schemes presented in Section VI-A whereas the DSCF decoder is simulated using floating point numbers, and the Fast-SSCL decoder is quantized with the scheme presented in [10].

According to Fig. 13, the Fast-DSCF decoder equipped with all the simplifications exhibits similar performance to the baseline DSCF decoder at all error orders and SNRs. It can be observed that the Fast-DSCF decoder has similar performance to DSCF even though the Fast-DSCF is quantized. At $\omega = 2$ and high SNR, Fast-DSCF shows a slight performance loss compared to the DSCF; this is mostly due to the reduced search span in SPC nodes. This means that a better SPC node approximation could be required at FER values targeting beyond $10^{-6}$.

At the target FER of $10^{-5}$, the proposed Fast-DSCF at $\omega = 1$ depicts 0.18 dB gain over Fast-SSCL-SPC with $L = 2$. At $\omega = 2$, Fast-DSCF is 0.21 dB better than Fast-SSCL-SPC with $L = 4$ and is only 0.08 dB away from the Fast-SSCL-SPC performance with $L = 8$. Compared to Fast-SSCL-SPC with $L = 16$, proposed Fast-DSCF performs slightly better than Fast-SSCL-SPC, by 0.03 dB. In the following comparison schemes, based on these performance results Fast-DSCF is compared against its Fast-SSCL-SPC counterparts that yield the closest error-correction performance at target FER $= 10^{-5}$. That is, Fast-DSCF with $\omega = 1, 2, 3$ are compared against Fast-SSCL-SPC (and other state-of-the-art SCL-based decoders) with $L = 2, 8, 16$, respectively.

B. Average Computational Complexity

Fig. 14 compares the average computational complexity of Fast-DSCF decoder against state-of-the-art Fast-SSCL-SPC decoders from [10] and [44], at medium-to-high SNR regime. The computational complexity is measured via the average number of cycles, which is obtained by taking the product of the average number of decoding iterations with the total number of clock cycles per iteration, for each decoder. It is essential to note that, the number of cycles are obtained with using the same polar code ($PC(1024, 512)$) and using the same number of parallel processing elements ($P_e = 64$) for all considered decoders. While latency of the Fast-SSCL-SPC decoder from [10] is fixed at each list size, the decoder from [44] uses early termination logic and its latency is dependent on the SNR. The Fast-DSCF decoder has large computational complexity at low SNR regions, but saturates quickly around our FER performance of interest.

At medium-to-high SNR regimes, the Fast-DSCF with $\omega = 1$ requires up to 16% more clock cycles than the its counterparts with $L = 2$. On the other hand, for $\omega = 2$ and $\omega = 3$, Fast-DSCF requires 15.6% and 21.7% less cycles on average than the Fast-SSCL-SPC decoders with $L = 8$ and $L = 16$, respectively. Therefore, we can claim that the proposed Fast-DSCF decoding for higher order error correction requires less amount of operations on average compared to Fast-SSCL-SPC decoding, which makes it favorable for applications that require improved FER performance with less average computational complexity.

C. ASIC Synthesis Results

The proposed Fast-DSCF decoder has been implemented in VHDL, validated with test benches and synthesized using TSMC 65nm CMOS technology node through Cadence Genus RTL compiler. To assure accuracy in our power measurements, switching activities from real test frames are extracted for the three architectures. The non-frozen bits for the test frames are generated using Bernoulli distribution equal probability.
Table I presents the ASIC synthesis results of the Fast-DSCF decoder implemented separately for each considered error order, and compared against other available SCF-based decoders and best available SCL-based decoders. The results from [45], [46] and [47] are scaled to 65nm CMOS technology, based on the presented scaling techniques in [46]. The latency and the throughput for this work are calculated based on their average values at target FER = $10^{-5}$. On the other hand, the worst-case latency values are also presented for a fair comparison. The quantization values are presented for the channel ($Q_{chn}$) and internal LLRs ($Q_{lm}$) and for the metric ($Q_{m}$).

The latency and the average throughput of the Fast-DSCF decoder is different for each implementation; that is because their different quantization schemes lead to different operating frequencies, and different SPC node sizes lead to different number of clock cycles per decoding iteration. On the other hand, the power consumption and the area increases with the number of clock cycles per decoding iteration. On the other hand, the fast decoding techniques used in the Fast-DSCF ($\omega = 1$) decoder yields 15.4× more throughput than the regular SCL implementation from [45]. Finally, compared to the Fast-SSC-SPC decoder with $L = 2$ [10], the proposed decoder has 32% less throughput but uses 1.9× less area, leading to 27.5% better area efficiency.

The Fast-DSCF decoder with $\omega = 2$ demonstrates 11.5% to 30.5% less throughput than its SCL-based counterparts with $L = 8$ [10], [46]. On the other hand, the required area for the SCL-based decoders is 3.4× to 5.8× more than that of Fast-DSCF. Therefore, the Fast-DSCF decoder with $\omega = 2$ is 2.4× to 5.1× more area-efficient than the reported fast SCL decoders. The Fast-DSCF decoder with $\omega = 3$ reports 46.8% more throughput than the SCL-based decoder in [47], but is 30% less than that of [46] with $L = 16$. On the other hand, similar to the $\omega = 2$ case, the Fast-DSCF decoder has significantly less area, and therefore is up to 5.8× more area-efficient. In return, due to the iterative nature of the SCL algorithm, proposed decoder has larger worst-case latency than its SCL-based counterparts.

As a result of the increased latency and power at higher error orders, it can be claimed that improving the FER costs more energy per decoded information bit; an increase of 37% for $\omega = 2$ and another 69% for $\omega = 3$ is observed. Since the synthesis results for the operating voltage and power consumption are not provided for the architectures described in [10], [19], [46], [49], we are not able to directly compare our results on power density and energy efficiency against the state-of-the-art. The only available results on energy consumption for SCL-based decoders have been carried out in [2] for polar codes of shorter lengths (i.e. $N = 256$ and $N = 512$), and it was...
shown that the increase in energy consumption is supralinear. For example, for the Fast-SSCL decoder for \( PC(512,256) \), the difference in energy consumption between \( L = 2 \) and \( L = 8 \) is 6.68×. Note that, the energy consumption of Fast-SSCL decoding is the best among all the considered SCL-based algorithms in [7]. Assuming that a similar increasing trend should be observed for the polar codes used in this work, the proposed Fast-DSCF decoder is expected to be much more energy-efficient than its fast SCL-based counterparts given the increase in energy consumption remains at 37% between \( \omega = 1 \) and \( \omega = 2 \).

The proposed Fast-DSCF implementations at \( \omega > 1 \) have greater worst-case latency compared to their SCL-based counterparts. The worst-case latency increases with \( T_{\text{max}} \), which is a major drawback for communications that prioritize low latency, including applications with FPGA. On the other hand, proposed implementations demonstrate improved area and energy efficiency as a trade-off, and have similar average latency and throughput compared to the state-of-the-art. Therefore, the proposed Fast-DSCF implementations are in favor of use cases where area and energy efficiency are prioritized over worst-case latency, such as massive machine-type communications [11].

VIII. CONCLUSION

In this work, we showed how to make the Dynamic SC-Flip decoding practical. We replaced the transcendental computations of the DSCF algorithm with a constant, and showed how to implement fast decoding techniques. Then, we further reduced the computational effort by employing a theoretical framework, which is later exploited in a hardware implementation. We showed further simplifications on metric updates and sort complexity in hardware. Proposed approximations and simplifications do not alter the error-correction performance significantly but make the DSCF decoding practically feasible. The proposed Fast-DSCF decoders synthesized using TSMC 65nm CMOS technology demonstrate 1.25, 1.06 and 0.93 Gbps throughput for \( \omega \in \{1,2,3\} \), respectively. For \( \omega = 3 \), the Fast-DSCF decoder is up to 5.8× more area-efficient than state-of-the-art fast CA-SCL decoders with equivalent FER performance at \( L = 16 \). Compared to the state-of-the-art fast CA-SCL decoders with equivalent FER performance, the proposed decoders are up to 5.8× more area-efficient. Finally, observations at energy dissipation indicate that the Fast-DSCF is more energy-efficient than its CA-SCL-based counterparts.

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