A high-gain \( \Gamma \)-source hybrid single-phase multilevel inverter for photovoltaic application

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Abstract
Impedance-based step-up converters are widely developed for photovoltaic applications due to providing single-stage conversion, high-efficiency, low voltage and current stresses, and high boost-factor. An improved \( \Gamma \)-source (\( \Gamma \)-source) single-phase hybrid multilevel inverter is proposed. This structure has a better voltage gain characteristic, high-efficiency, multilevel output voltage, low output current total harmonic distortion (THD), and continuous input current. It is extensible for attaining higher voltage levels. Furthermore, higher non-shoot-through modulation indexes are obtainable by this topology in comparison with previous works due to performing higher gains in lower shoot-through duty cycles. Also, the output harmonics are reduced because of applying lower shoot-through duty cycles. This article demonstrates the operating principle of this hybrid multilevel inverter in detail. Simulation and experimental results are exhibited to evaluate the performance of this converter. Results confirm the proposed \( \Gamma \)-source hybrid multilevel inverter, its operating principle, and the modulation strategy.

1 | INTRODUCTION

Manufacturing PV power stations are rapidly increasing to generate green power, reduce air pollution concerns, and a sudden shortage of fossil fuels. Additionally, in some areas, distributing the facilities of conventional power distribution is difficult or maybe too expensive. As a result, employing stand-alone power stations is a convenient solution. Amongst various independent power generation systems, the PV technology is widely propagated [1]. One critical part of a PV system, in terms of power electronics, is its inverter section. Preparing a pure AC voltage with an appropriate and standard value from low-voltage PV arrays is a great challenge. Several methods presented for implementing a stand-alone PV plan, as shown in Figure 1. The DC/DC and DC/AC blocks, in each concept of Figure 1, could be replaced by power electronic converters. Today, the design and development of step-up converters are the most interesting topic, which incorporates not only DC/AC converters but also DC/DC, AC/DC, and AC/AC converters. Especially, impedance-based converters are broadly developed for PV application due to providing single-stage conversion ability, high-efficiency, low voltage and current stresses, and high-gain.

Different impedance networks such as Z-source and its derivations [2–4], quasi-Z-source (qZS) [5–15], common grounded Z-source [16], Y-source [17, 18], X-source [19], \( \Gamma \)-source and improved \( \Gamma \)-source [20], trans-Z-source [21], LCGT-Z-source [22], \( \Sigma \)-Z-source [23], A-source [24], and switched Z-source [25] have been presented and evaluated until now. Each impedance network includes magnetic and capacitive components, along with a specific configuration that possesses different pros and cons. Ellabban and Abu-Rub [26] reviewed and compared a lot of impedance-based inverters. Also, Siwakoti et al. [27] and Forouzesh et al. [28] reviewed recent techniques in designing impedance-based converters. Recently, the application of impedance networks for designing multilevel step-up inverters (MLSI) is another topic of interest. Most of MLSIs have been developed based on conventional MLIs like those called neutral-point clamped (NPC) [8], T-type [7], and cascaded H-bridge (CHB) [29] inverters. Also, MLSIs have been designed based on hybrid structures [30, 31]. Most of impedance-based MLIs provide better efficiency in comparison with switched-capacitor based MLIs [32] due to fewer numbers of power switches and capacitors. Husev and Roncerio-Clemente [8] used the conventional quasi-Z-source network at the input of the...
traditional NPC inverter. However, the resulted topology does not provide high boost-factor compared with the latest topologies. Pires and Cordeiro [7] have executed a similar concept on T-type inverters. However, the voltage gain is still low, so that the control system forces to apply higher ST duty ratios. This problem increases the output harmonics and limits the NST modulation index. Nguyen and Tran [29] proposed a novel impedance-based single-phase MLI based on the CHB configuration. Although, this converter has solved the drawbacks of previous CHB-based step-up MLIs in terms of the number of components, using floating capacitors reduces the reliability of this topology. Also, the boost factor is still low. Recently, multi-level inverters with boost feature and self-balancing capacitors have been presented [33–37]. Most of them have a ladder based structure, like those presented in [35] with 19 power switches. All of them provide the step-up feature. Most of switched-capacitor based inverters do not require magnetic components.

An improved Γ-source single-phase hybrid multilevel inverter is proposed, which is originated from developing and integrating two topologies: the Γ-network and the hybrid structure of [30]. As a result of this new idea, this new topology performs the same output multilevel voltage with a better boost-factor, high-efficiency, low output current total harmonic distortion (THD), and continuous input current. This topology has a modular and extensible structure. Furthermore, higher NST modulation indexes are obtainable in comparison with previous works due to generating higher gain in lower ST duty cycles. Moreover, the value of output harmonics is diminished due to applying lower ST duty cycles. This paper explains the operating principle of this HMLI comprehensively. Simulation and experimental results are presented in order to examine the performance of the proposed topology. Results confirm the proposed IΓ-source HMLI, its operating principle, and the implemented modulation strategy. This paper is organised as follows: the operating principle of the proposed inverter is explained in Section 2. Then, comprehensive analysis and comparative evaluation are proposed. Simulation and experimental results are presented and assessed in Section 3. Achievements are summarised in conclusion.

2 OPERATING PRINCIPLE OF THE IΓ-SOURCE HMLI

Figure 2 shows the structure of IΓ-source HMLI. In Figure 2(a), the three-level configuration is depicted, and in Figure 2(b), the five-level configuration from this structure is illustrated. This structure is composed of two improved Γ-source-based switching cells, which require a particular modulation strategy. Each cell comprises of four power switches and an improved Γ-source network. These cells are cascaded together, and their output terminal is linked to an H-Bridge inverter. As shown in Figure 2(b), it is feasible to increase the number of switching cells, and this case yields more output voltage levels. Producing more output voltage levels reduce output voltage and current harmonics further. Each cell has two possible switching states, which are called ST and NST events. Positive and negative cycles
of the output voltage depend on the switching states of output H-Bridge inverter. In the following, switching modes are described.

2.1 The inverter status in ST and NST events

In order to analyse the proposed inverter, the following assumptions are considered:

(i) The converter operates in continuous current mode.
(ii) All components are assumed to be ideal.
(iii) The three-level converter is surveyed, and then, its theory is developed for the five-level inverter.
(iv) The Π-source network has symmetry. So, only the upper side is investigated.

2.1.1 Shoot-through states

The shoot-through state occurs whenever the control system applies one of the states of Figure 3. Figure 3(a) and (b) illustrate the converter status in the positive cycle of the output voltage. Q5 and Q8 are turned on to prepare a positive cycle. In this status, Q1 and Q2 (or Q3 and Q4) are turned on. If upper power switches perform the ST event, as represented by Figure 3(a), diodes D1, D3, D4, and D7 are turned off. If lower switches provide this case, diodes D2, D5, D6, and D8 are kept off, as shown in Figure 3(b). Based on the equivalent circuit of Figure 3(a), the following equations are obtained.

$$V_{L1-sh} = V_i$$

$$V_{L2-sh} = V_{C1} + V_{C3}$$

$$V_{Lm1-sh} = V_{Lm2-sh} - V_{C2}$$

$$V_{Lm2-sh} = \frac{n_2}{n_1} V_{Lm1-sh} = n V_{Lm1-sh}$$

$$V_{Lm1-sh} = \frac{V_{C2}}{1 - n}$$

Also, according to the equivalent circuit of Figure 3(b), the Equations (6)–(9) can be determined.

$$V_{L3-sh} = V_{C5} + V_{C6}$$

$$V_{Lm3-sh} = V_{Lm4-sh} - V_{C4}$$

$$V_{Lm3-sh} = \frac{n_3}{n_2} V_{Lm4-sh} = n V_{Lm3-sh}$$

$$V_{Lm3-sh} = \frac{V_{C4}}{1 - n}$$

2.1.2 Non-shoot-through states

Four possible switching states can afford the NST state, as illustrated in Figure 4. In those states, diodes D1, D4, D5, and D6 are on. Figure 4 is relevant to the positive output cycle. In the negative cycle, those four events repeat, while the Q6 and Q7 are turned on instead of Q5 and Q8. The voltage across the load is zero in state 4, as shown in Figure 4(d). This mode happens during the simultaneous operation of Q2 and Q3. Usually, in ST states, the magnetic components store the specific amount of energy, and at the end of ST states, they deliver it to the load or other parts. The following equations can represent the status of magnetic components for NST mode.

$$V_{Lm2-nsh} = -V_{C3}$$

$$n V_{Lm1-nsh} = -V_{C3}$$

$$V_{L2-nsh} = -V_{C1} - V_{C3} + V_{pn1}$$

$$V_{Lm2-nsh} = V_{Lm1-nsh} + V_{C2} - V_{pn1}$$

$$V_{L1-nsh} = -V_i + V_{C1}$$
In each mode shown, the connected impedance network to the output has precisely the same equations. Hence, there is no need to write similar equations. The switching event of Figure 4(c) produces the maximum amplitude of the output voltage. The equivalent circuits of Figure 4(a) and (b) generate half of the maximum attainable amplitude across the output load. As a result, the output voltage has the following values according to each state.

\[
V_o = V_{pn1} \quad \forall \text{ State} = 1 \quad (15)
\]

\[
V_o = V_{pn1} \quad \forall \text{ State} = 2 \quad (16)
\]

\[
V_o = 2V_{pn1} \quad \forall \text{ State} = 3 \quad (17)
\]

\[
V_o = 0 \quad \forall \text{ State} = 4 \quad (18)
\]

### 2.2 Output voltage gain

In order to obtain the output voltage gain of this topology, the volt-second principle of Equation (19) is applied to Equations (1)–(5) and Equations (10)–(14). Consequently, Equations (20)–(23) are determined.

\[
\int_0^{d_{th}T_s} v_{L1-sh}(t) \, dt = \int_0^{d_{th}T_s} v_{L1-nsh}(t) \, dt \quad (19)
\]

\[
\begin{aligned}
&d_{sh}V_{L1-sh} = (1 - d_{sh})V_{L1-nsh} \\
&V_i - (1 - d_{sh})V_{C1} = 0 \\
&V'_{C1} + V_{C3} - (1 - d_{sh})V_{pn1} = 0 \\
\end{aligned} \quad (20)
\]

\[
\begin{aligned}
&d_{sh}V_{L2-sh} = (1 - d_{sh})V_{L2-nsh} \\
&V_{C1} + V_{C3} - (1 - d_{sh})V_{pn1} = 0 \\
\end{aligned} \quad (21)
\]

\[
\begin{aligned}
&d_{sh}V_{Lm1-sh} = (1 - d_{sh})V_{Lm1-nsh} \\
&\frac{1 - s + nd_{sh}}{1 - s}V_C + (1 - d_{sh})V_{C2} = (1 - d_{sh})V_{pn1} \\
&d_{sh}V_{Lm2-sh} = (1 - d_{sh})V_{Lm2-nsh} \\
&nd_{sh}V_{C1} + (1 - d_{sh})V_{C2} = 0 \\
\end{aligned} \quad (22)
\]

\[
\begin{aligned}
&d_{sh}V_{Lm1-sh} = (1 - d_{sh})V_{Lm1-nsh} \\
&\frac{1 - s + nd_{sh}}{1 - s}V_C + (1 - d_{sh})V_{C2} = (1 - d_{sh})V_{pn1} \\
&d_{sh}V_{Lm2-sh} = (1 - d_{sh})V_{Lm2-nsh} \\
&nd_{sh}V_{C1} + (1 - d_{sh})V_{C2} = 0 \\
\end{aligned} \quad (23)
\]

By inserting \( V_{pn} \) from Equation (22) into Equation (23), the voltages of capacitors \( C_2 \) and \( C_3 \) are determined. Also, the voltage of \( C_1 \) can be deduced from Equation (20) by inserting Equations (1) and (14) to Equation (20).

\[
V'_{C1} = \frac{V_i}{1 - d_{sh}} \quad (24)
\]
\[ V_{C2} = \frac{(n - 1)(1 - d_{sh})}{n(1 - 2d_{sh}) - 1 + d_{sh}} V_{C1} \]  
\( (25) \)

\[ V_{C3} = \frac{n d_{sh}}{n(1 - 2d_{sh}) - 1 + d_{sh}} V_{C1} \]  
\( (26) \)

Equations (24)–(26) must be substituted into Equation (21) to calculate the voltage gain of the impedance network. As a result, Equation (27) expresses the voltage gain of the impedance network.

\[ V_{pn1} = \frac{(n - 1)(1 - 2d_{sh}) - 1 + d_{sh}}{1 - d_{sh}} V_i \]  
\( (27) \)

As depicted in Figure 2(a), this \( \Gamma \)-source network has symmetry, so, the overall voltage gain on the output of this network is twice of \( V_{pn1} \). So, the voltage gain can be expressed as Equation (28).

\[ V_{pn} = 2V_{pn1} = \frac{2(n - 1)}{n(1 - 2d_{sh}) - 1 + d_{sh}} V_i \]  
\( (28) \)

The maximum output voltage level depends on the number of \( \Gamma \)-source cells and the modulation index \( M_i \). The modulation index (or NST index) also affects the RMS value of output voltage and the total boost-factor. If it is assumed the modulation index to be \( M_i \), the maximum achievable modulation index can be acquired by Equation (29). As an example, if \( d_{sh} \) is assumed to be 0.1 in nominal condition, the \( M_i \) can be reached up to 0.9. Hence, the value of \( d_{sh} \) can deteriorate \( M_i \).

\[ M_i \leq 1 - d_{sh} \]  
\( (29) \)

For the five-level hybrid inverter of Figure 2(b), two \( \Gamma \)-source cells exist. As a result, the maximum output voltage level is calculated by Equation (30). The output voltage reaches to Equation (30), whenever the state 3 from NST states is applied to both cells.

\[ V_{\text{omax level}} = \frac{4M_i(n - 1)}{n(1 - 2d_{sh}) - 1 + d_{sh}} V_i \]  
\( (30) \)

The maximum output voltage level for an \( m \)-level inverter with this configuration can be obtained by Equation (31).

\[ V_{\text{omax level}} = \frac{M_i(m - 1)(n - 1)}{n(1 - 2d_{sh}) - 1 + d_{sh}} V_i \]  
\( (31) \)

Figure 5 shows different graphs that help to understand the status of this topology and its components for various ST duty ratios. Figure 5(a) depicts the effect of turns-ratio ‘\( n \)’ on the gain produced by each \( \Gamma \)-source cell. ‘\( n \)’ is equal to \( n_2/n_1 \) and \( n_4/n_3 \). Figure 5(b) shows the maximum obtainable output gain for the five-level converter of Figure 2(b). Figure 5(c) illustrates the effect of the ST duty cycle on the voltage of capacitors for \( n = 1.24 \). Figure 6 compares the proposed inverter with some other five-level inverters in terms of the maximum obtainable gain. Additionally, the boost factors of these topologies are listed in Table 1. As can be inferred, the proposed inverter has better gain characteristics. Moreover, the proposed \( \Gamma \)-source network has a higher boost-factor than transformer-based Z-source networks, as listed in Table 2 and shown in Figure 6(c). One crucial term in Equations (30) and (31) is \((1 - d_{sh})\), which is placed in the denominator of Equations (30) and (31). As can be seen, this term is equal to the \( M_i \), and as a result, this \( \Gamma \)-source cancels the influence of modulation index on the main boost factor.
**FIGURE 6** Comparative evaluation between the proposed inverter and some other topologies. (a) For \( n = 5 \), (b) for \( n = 1.24 \), (c) comparative analysis between the boost factor of the proposed network and other trans-based networks (turns ratio = 1.24)

**TABLE 1** The boost factor for different step-up multilevel inverter

| Converter          | qZS HMLI-5L [30] | qCHB-5L [29] | qZS T-Type-3L [7] | Conv. CHB-5L [29] | Γ-ZS-NPC-3L [26] | Proposed-5L | Proposed-3L |
|-------------------|-----------------|--------------|------------------|------------------|----------------|-------------|-------------|
| Output gain       | \( \frac{4}{1+2d_{sh}} \) | \( \frac{2}{1+2d_{sh}} \) | \( \frac{1}{1+d_{sh}} \) | \( \frac{2(\text{or}1)}{1+4d_{sh}} \) | \( \frac{2(\text{or}1)}{1+6d_{sh}} \) | \( \frac{4(\text{or}1)}{1+8d_{sh}} \) | \( \frac{2(\text{or}1)}{1+4d_{sh}} \) |

\( k_0 = 1 - 2d_{sh} \)

\( 1 \text{L} = 3 \text{ Level,} \ 2\text{L} = 5 \text{ Level.} \)

**TABLE 2** A comparative analysis between the boost factor of the proposed network and other trans-based networks

| Impedance networks | Trans-ZS [20] | Improved Trans-ZS [20] | Improved Γ-ZS [20] | Proposed IF-Source |
|--------------------|---------------|------------------------|---------------------|-------------------|
| Boost-factor       | \( \frac{1}{1+(N+1)d_{sh}} \) | \( \frac{1}{1+(N+2)d_{sh}} \) | \( \frac{2(\text{or}1)}{(1+4d_{sh})} \) | \( \frac{2(\text{or}1)}{(1+6d_{sh})} \) |
| \( k_0 = 1 - 2d_{sh} \) | \( k_0 = 1 - 2d_{sh} \) |

\( N = \text{turns-ratio and equal to} \ 1:n. \)

Figure 7 illustrates the impact of the ST duty cycle on the voltage pressure on power components. Figure 8 compares the output voltage gain of some other HMLI with the proposed three-level and five-level inverter in terms of modulation index. For the three-level version of the proposed IF-source HMLI, six power switches are required. Moreover, eight power diodes are needed. Table 3 lists the voltage stresses on the semiconductors of the three-level version. In order to calculate the current stress of each component, the average and ripple values of inductor currents are required. The average value of the current of \( L_1 \) is equal to the input current. So, by using \( \frac{P_o}{P_i} = \frac{V_o}{V_i} \cdot \frac{I_o}{I_i} = 1 \) and the Equation (31), the

**FIGURE 7** The voltage stress on power components for \( n = 1.24 \)

**FIGURE 8** The effect of \( M_i \) on the output gain (turns-ratio = 1.24)
The implemented modulation strategy

The boost-factor function of the \( \Gamma \)-source network has two influential parameters on the gain of this network, as shown by

\begin{align*}
\Gamma_{\text{source}} & = \left( \frac{n}{1+\frac{d_{sh}}{d_{th}}} \right) \left( \frac{1}{1+\frac{d_{sh}}{d_{th}}} \right) \frac{I_0}{I_{\text{in}}} 
\end{align*}

where, \( V_{C1} \) and \( V_{C2} \) are equal to Equations (24) and (26), respectively. Similar equations can be obtained for the coupled inductor \( L_{m1} \) by analysing the instantaneous current, which passes through capacitor \( C_2 \).

\begin{align*}
\Delta I_{L_{m1}} d_{sh} &= -(1 - d_{sh}) I_{L_{2}} \\
\Delta I_{L_{m1}} &= \frac{V_{C2} d_{sh} T_s}{(1 - n) I_{mn1}}
\end{align*}

The converter has a symmetrical structure; therefore, it is not required to find the current values for lower-side components.

2.3 The implemented modulation strategy

Similar to other inverters, the proposed topology needs a particular modulation strategy to generate an alternative voltage at the output. In order to produce a multilevel voltage, all employed \( \Gamma \)-source cells must have phase-shift respect to themselves. The power switches \( Q_5-Q_8 \) must turn on and off according to a 50 Hz/60 Hz sinusoidal reference. For producing a positive cycle, the \( Q_2 \) and \( Q_3 \) turn on. \( Q_1 \) and \( Q_2 \) turn on whenever the sinusoidal reference is in the negative cycle. For other power switches \( (Q_1-Q_4) \), many shoot-through and non-shoot-through states must be applied. Also, these power switches must be turned on/off with a sinusoidal pattern. In this case, some triangular waveform with the appropriate phase-shift is generated. The absolute value of the sinusoidal reference is compared with a triangular waveform for generating non-shoot-through signals. Identical DC values are compared with those triangular waves to produce the shoot-through state. Figure 9 depicts the block diagram of this modulation method, which can be implemented in TMS320F28335 digital signal processors. Also, Figure 10 shows the relevant waveforms of this modulation method.

2.4 Sensitivity analysis of \( \Gamma \)-source network

The boost-factor function of the \( \Gamma \)-source network has two influential parameters on the gain of this network, as shown by

| Part   | Voltage stress                                                                 | Current stress |
|--------|--------------------------------------------------------------------------------|----------------|
| Q1–Q4 | \((v_{C1} - v_{C2}) + v_{C3} + v_{C4}\)                                       | \(I_{L_{2}}\)  |
| D1, D2| \(v_{C1} + v_{C2}\)                                                           | \(I_{L_{m1}}\) |
| D3    | \(v_{C3} + v_{C4}\)                                                           | \(I_{L_{1}}\)  |
| D4    | \(v_{C1} + v_{C2} - v_{C3}\)                                                  | \(I_{L_{m1}}\) |
| D5    | \(v_{C4} + v_{C3} - v_{C1}\)                                                  | \(I_{L_{m1}}\) |
| D6    | \(v_{C1} + v_{C2} - v_{C3}\)                                                  | \(I_{L_{m1}}\) |
| Q5–Q8 | \((v_{C1} - v_{C2}) + v_{C3}\) \(\frac{1}{n}\)                               | \(I_{L_{1}}\)  |

The following formula is deduced.

\[ I_{L_{1}} = I_o = \frac{M_n (n - 1) (n - 1)}{(1 - 2 d_{sh}) - 1 + d_{sh}} I_o \] (32)

Also, the current ripple of the inductor \( L_1 \) is obtained by using \( V_{L_{1}} = I_o \Delta h \).

\[ \Delta I_{L_{1}} = \frac{V_{L_{sh}} T_s}{L_{L_{1}}} \] (33)

According to Figures 3(a) and 4(a), the following expression determines the instantaneous current that passes through the capacitor \( C_1 \).

\[ i_{L_{1}} = \begin{cases} -i_{L_{2}} & 0 \leq t < d_{sh} T_s \\ -h_{L_{1}} - i_{L_{2}} d_{sh} T_s & d_{sh} T_s \leq t < T_s \end{cases} \] (34)

By applying the ampere-second principle to Equation (34), the relation between the average current of \( L_1 \) and \( L_2 \) is determined by Equation (35).

\[ I_{L_{2}} = (1 - d_{sh}) I_{L_{1}} \] (35)

Also, the current ripple of the inductor \( L_2 \) is:

\[ \Delta I_{L_{2}} = \frac{V_{C1} + V_{C3}}{L_{L_{2}}} d_{sh} T_s \] (36)

where, \( V_{C1} \) and \( V_{C2} \) are equal to Equations (24) and (26), respectively. Similar equations can be obtained for the coupled inductor \( L_{m1} \) by analysing the instantaneous current, which passes through capacitor \( C_2 \).

\[ \Delta I_{L_{m1}} d_{sh} = -(1 - d_{sh}) I_{L_{2}} \] (37)

\[ \Delta I_{L_{m1}} = \frac{V_{C2} d_{sh} T_s}{(1 - n) I_{mn1}} \] (38)
Equation (28). This section presents the sensitivity of the boost-factor to the turns ratio of coupled inductors and the shoot-through duty cycle. For this purpose, the differential sensitivity analysis principle is employed. Equation (39) shows this well-known principle. Figure 11(a) and (b) show the sensitivity analysis results. Figure 11(a) relates to Equation (40), and Figure 11(b)

\[ \Delta (BF) = \frac{\partial (BF)}{\partial n} \Delta n + \frac{\partial (BF)}{\partial d_{st}} \Delta d_{st} \]  

(39)

By applying Equation (32) to Equation (28), the following expressions are obtained.

\[ \frac{\partial (BF)}{\partial n} = \frac{2d_{st}}{(d_{st} - 1)(d_{st} + n - 2nd_{sh} - 1)^2} \]  

(40)

\[ \frac{\partial (BF)}{\partial d_{sh}} = \frac{2(n - 1)(2d_{sh} + 3n - 4nd_{sh} - 2)}{(d_{sh} - 1)^2(d_{sh} + n - 2nd_{sh} - 1)^2} \]  

(41)

It can be inferred from Figure 11, the turns ratio of coupled inductors has a significant effect on the gain. Thus, by choosing an appropriate number for it, it is possible to achieve high gains with lower duty cycles. This feature helps to reduce the ST modulation index. Therefore, the non-shoot-through modulation index can be varied in a wide range.

**TABLE 4**  The converter specifications

| Components         | Value     |
|--------------------|-----------|
| Input voltage      | 20 V      |
| Output voltage     | 400 V\(_{pk-pk}\) |
| Output power       | 250 W     |
| Switching frequency| 5 kHz     |
| Turns ratio        | 1.24      |
| L\(_1\)            | 150 \(\mu\)H |
| L\(_2\), L\(_3\)   | 300 \(\mu\)H |
| L\(_m1\), L\(_m3\) | 400 \(\mu\)H |
| All capacitors     | 2200 \(\mu\)F |
| Power diodes       | MUR1560   |
| Power switches     | IRFP460A  |

**FIGURE 12**  Five-level \(\Gamma\)-source HMLI prototype and its components

corresponds to Equation (41).
FIGURE 13  The simulation and experimental results. (a) The output voltage and current, (b) the signals of power switches in one $\Gamma$-source cell, (c) the output voltage of $\Gamma$-source cell.
FIGURE 13(a) shows the output voltage and current waveform in both simulation and experimentation. The output voltage amplitude reaches to 200 V with five voltage levels in both simulation and experimentation. The output load consumes 250 W. The load is inductive ($R = 40 \, \Omega$, $L = 150 \, \text{mH}$). So, the high-frequency harmonics are omitted from the output current, and the output current is sinusoidal. There is a phase difference between the output voltage and output current due to supplying an inductive load. The output current has been measured using LEM LA-55 current transducer. Figure 13(b) represents the pulses of Q1–Q4. As can be seen, similar to the simulation result, the power switches Q1 and Q3 contain shoot-through command. The shoot-through duty cycle is 0.1. Also, the deduced signals validate Figure 10. Figure 13(c) presents the output voltage of IF-source cell. These two cells are identical, and their output voltage is equal. Figure 14 incorporates the waveforms of capacitors in one IF-source module. Figure 14(a) illustrates the voltage of C1 and C6. As can be seen, the voltage of these capacitors is equal to 11.8 V in both simulation and experimentation. Figure 14(b) represents the voltage of capacitors C2 and C3, which is equal to 42.5 and 30 V, respectively. Also, the voltage of C4 and C5 are identical to C2 and C3, respectively, that are not presented again. The voltage stress on the power switches Q1–Q4 are depicted by Figure 15 with respect to their gate signals. These results confirm the

3 RESULTS AND ANALYSIS

This section presents and evaluates the simulation and experimental results. Simulations have been done by MATLAB/Simulink software, and experiments have been executed using a five-level prototype. Table 4 shows the converter specifications and Figure 12 displays the prototype. The TMS320F28335PGFA digital signal processor generates convenient command signals for the power converter based on the algorithm shown by Figures 9 and 10. Inductors are prepared with EER2834 ferrite core. The switching frequency is 5 kHz. The input voltage of each module is connected to a 20 V power supply, as illustrated in Figure 12. The turns ratio for coupled inductors is 1.24. Figure 13(a) shows the output voltage and current waveform in both simulation and experimentation. The output voltage amplitude reaches to 200 V with five voltage levels in both simulation and experimentation. The output load consumes 250 W. The load is inductive ($R = 40 \, \Omega$, $L = 150 \, \text{mH}$). So, the high-frequency harmonics are omitted from the output current, and the output current is sinusoidal. There is a phase difference between the output voltage and output current due to supplying an inductive load. The output current has been measured using LEM LA-55 current transducer. Figure 13(b) represents the pulses of Q1–Q4. As can be seen, similar to the simulation result, the power switches Q1 and Q3 contain shoot-through command. The shoot-through duty cycle is 0.1. Also, the deduced signals validate Figure 10. Figure 13(c) presents the output voltage of IF-source cell. These two cells are identical, and their output voltage is equal. Figure 14 incorporates the waveforms of capacitors in one IF-source module. Figure 14(a) illustrates the voltage of C1 and C6. As can be seen, the voltage of these capacitors is equal to 11.8 V in both simulation and experimentation. Figure 14(b) represents the voltage of capacitors C2 and C3, which is equal to 42.5 and 30 V, respectively. Also, the voltage of C4 and C5 are identical to C2 and C3, respectively, that are not presented again. The voltage stress on the power switches Q1–Q4 are depicted by Figure 15 with respect to their gate signals. These results confirm the
FIGURE 15  The simulation and experimental results. (a) The voltage stress of Q_1 and Q_4, (b) the voltage stress of Q_2 and Q_3.

FIGURE 16  The voltage stress on the power switches of H-bridge circuit. (a) Simulation, (b) experimental.
information in Table 3 and Figure 7. Both IΓ-source cells are identical. Hence, the presented voltage stresses on Q1–Q4 are repeated for the other IΓ-source cell. Figure 16 shows the voltage stress on one power switch of the H-bridge section. Also, its gate-source voltage is illustrated. When the power switch is on, the voltage drop is too low. During off-state, each power switch of the H-bridge circuit exposes to the maximum output voltage amplitude. In these simulation and experimental tests, the maximum output voltage is equal to 200 V, which is placed on level five. So, the application of this structure is limited to photovoltaic systems, fuel cells, batteries, and other low voltage systems.
TABLE 5 Comparative analysis

| Parameter | Ref. [30] | NPC qZSI [8] | The proposed |
|-----------|-----------|--------------|--------------|
| Inductors | 4         | 4            | 10           |
| Capacitors | 8        | 4            | 12           |
| Switches  | 12        | 16           | 12           |
| Diodes    | 4         | 14           | 16           |
| Efficiency | 92%       | 94%          | 95.8%        |
| THD       | 3.6%      | 7%           | 2.73%        |

Figure 17 displays other results, including the input current, the experimental converter efficiency, and the output current THD. This topology has an inductor on the input terminal. Therefore, it guarantees continuous input current if an appropriate inductance value for inductors is chosen. The inverter operates in the continuous current mode operation (CCM). Figure 17(a) confirms the CCM operation of this topology. Similar to other hybrid multilevel inverters, the proposed inverter provides high efficiency. The efficiency is measured by using the formula \( P_o \). The input power is obtained by using \( V_{dc}I_{dc} \), and the output power is calculated by \( V_{rms}I_{rms} \). The switching frequency is low. Consequently, the switching losses of the converter have not significant value. Figure 17(b) illustrates the variations of efficiency subject to the variations of the output power. The shoot-through time is low because the converter can provide high voltage gain with lower shoot-through ratios. The main contribution of this paper regarding the previous research is the need to lower shoot-through time, which increases efficiency and reduces the losses. Furthermore, reducing the shoot-through time without affecting the gain characteristics helps to improve the output current THD. In lower output powers, the conduction losses are significantly diminished, but the switching losses are not altered. Consequently, the efficiency drops to 93%. The full-load efficiency is 95.8%. Two cases have been investigated for efficiency analysis. Figure 17(b) confirms that if shoot-through increases, the efficiency reduces. This result validates the performance of the proposed topology, in which it needs a lower shoot-through duty cycle for its operation. Table 5 compares the efficiency of the proposed topology with some other similar topology in full-load condition. Figure 17(b) also displays how the losses are distributed. Figure 17(c) represents the output current THD in both simulation and experimentation, which is relevant to \( M = 0.9 \) and \( D = 0.1 \). The experimental output current data has been captured, and it is analysed by MATLAB. Figure 17(d) shows the THD variations subject to the modulation index change. Two items are essential in reducing the current harmonics. First, the topology, which is multilevel. The proposed topology produces 9 levels from the negative peak to the positive peak. Second, the shoot-through duty cycle. Increasing the shoot-through reduces the modulation index. So, the number output level is reduced, and the THD is increased. Figure 17(d) validates this subject. It can be inferred from Figure 17(c), when the modulation index is reduced, the number of output levels is decremented. Accordingly, the output current THD is increased. This phenomenon could be seen in all multilevel inverters. Table 5 also compares the number of components for generating 9-level peak-peak voltage with different techniques. Although the proposed topology requires more components than [30] and [8], it produces the output voltage with a lower THD and higher efficiency than those converters. Since, in [8] and [30], higher boost-factor is obtained by higher shoot-through modulation indexes, the non-shoot-through modulation index is reduced. In multilevel inverters, the number of output voltage level is relevant to the non-shoot-through modulation index. Therefore, reducing this index decreases the number of output levels, which lead to increasing harmonics. So, if the duration of the shoot-through event is reduced, the voltage and current distortions are reduced too. In the proposed topology, the structure produces higher voltages with lower shoot-through duration. The number of components does not guarantee low efficiency or high efficiency. In this case, efficiency has been increased by reducing the required ST duty cycle.

4 | CONCLUSION

This paper proposes a multilevel hybrid inverter based on an improved \( \Gamma \)-source network. By using a new impedance network, the traditional H-bridge inverter is equipped with the step-up feature. Also, by using a modular cascade structure, a multilevel output voltage is generated. As a result, the proposed converter provides higher output voltages with lower duty cycles. Also, unlike other impedance-based inverters, the modulation index is less limited to the shoot-through modulation index, which leads to better harmonic characteristics at output current. The proposed converter need little shoot-through event time. So, the amount of conduction loss is reduced. As a result, the efficiency is increased. The presented topology operates in continuous current mode. Compared to previous similar inverters, this inverter requires a lower number of power switches; nevertheless, it requires more diodes, capacitors, and inductors than them. Simulation and experimental results confirm the theory, the operating principle and all claims.

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