Towards a Domain Specific Solution for a New Generation of Wireless Modems:
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1 Introduction

At the end of Moore’s Law, we find ourselves with an unwavering demand for more processing power. This is especially true in the realm of wireless communications, which is experiencing unprecedented growth in the areas of data rates, devices, and services. Fifth generation (5G) wireless technologies require a massive number of antennas and sophisticated signal processing to improve bandwidth and spectral efficiency [26]. The Internet of Things (IoT) is causing an enormous proliferation in the number of connected devices, predicted to exceed 30 billion devices by 2025 [20]. And new service categories, such as ultra-reliable low latency communications (uRLLC), will produce new use cases, such as self-driving cars, robotic factories, and remote surgery [2]. Addressing these challenges in the “post Moore’s Law” era requires a novel approach to computer design. Architects can no longer rely on faster cores, or even more silicon, to save the day. An effective design requires an understanding of the dataflow and processing requirements of a particular application. It appears that we have entered the era of Domain Specific Architectures (DSA) [17].

1.1 A Brief Taxonomy of Domain Specific Languages and Architectures

DSAs are far from a new concept. In the last decade, the emergence of Domain Specific Languages (DSLs) paired with DSAs has produced a new revolution in architecture design [17], but even this has some much earlier examples. In what follows we will recognize the strong connection by using the term DSL/DSA to describe such holistic architectures. For DSAs, some of the earliest and best-known examples are the fixed function pipelines of early graphics subsystems [9]. These specialized systems often required a DSL such as Iris GL and later OpenGL [24] to facilitate programming. With the help of Moore’s Law, these rigid systems were eventually displaced by more general and flexible graphics processing units (GPUs) [54]. However, widespread adoption of GPUs for general purpose computing did not occur until the arrival of a more flexible DLS called CUDA [50]. GPU’s eventually found use in a wide variety of applications, including a new “killer app” called deep convolutional neural networks [25]. While GPU’s proved to be an excellent platform for neural network training, they lacked the speed and efficiency for neural network inference. This led to a new, more specialized class of processors called TPU’s (tensor processing units) [22], which could be easily programmed with a specialized DSL (Tensorflow) [15]. In all of these cases, a DSL abstracted the complexity of the underlying hardware and alleviated the burden of optimizing performance.

While GPUs and TPUs may be the best-known examples of DSAs, there are numerous other examples which may give us inspiration. In the field of molecular simulation, the Anton 2 supercomputer outperforms general-purpose hardware by two orders of magnitude [12]. This is achieved through a combination of specialized processing elements, compute tiles, and interconnection networks. Another excellent example is the Eyeriss 2 flexible accelerator for neural networks on mobile devices [8]. Mobile neural network models tend to be sparse and have irregular access patterns. In addition, mobile devices tend to have extremely constrained power budgets, so energy efficiency is of paramount importance. In order to address these challenges, Eyeriss 2 uses specialized processing elements, minimizes data movement, and implements a flexible hierarchical mesh network for different operating modes. A third example, similar in many aspects to the wireless processing domain, is the Barefoot Tofino domain specific processor for networking [6]. This packet processor contains configurable match and action pipelines that can be programmed using a specialized DSL called P4 [36]. By eschewing the von Neumann processing model, minimizing control area, and maintaining a regular structure, the Tofino processor can achieve performance comparable to fixed function switches. In each of these examples, tradeoffs were made at every level of the hierarchy with a thorough understanding of the dataflow and processing requirements for that domain.

1.2 Wireless Baseband as a ”Dataflow Domain Specific Architecture”

In the domain of wireless communications, and especially in the area of wireless baseband processing, there are certain concepts that help us define the architectural requirements. One of the most important concepts is that of a service. From the network operator’s perspective, a service refers to a particular use case scenario, with well-defined bandwidth and quality of service (QoS) requirements. However, from a modem developer’s perspective, a service implies a predefined set of dataflows with well understood, or at least well bounded, processing, storage and timing requirements. In this context, dataflows refer to the abstract dataflow model described in [12], where nodes denote operations, and arcs denote data dependencies between operations. Dataflows may be static (known before run time) or dynamic (known at run time). Many variants of dataflow models exist, including synchronous dataflow [28], dataflow process networks [27], and scenario aware dataflow [44], with each model having its own mathematical tools for analysis.

In wireless communications, flows may be considered semistatic, where the dataflow patterns are known in advance and remain stable for a reasonable length of time. Additionally, 5G wireless communication systems have different real-time constraints for different services. The real-time requirements for enhanced mobile broadband (eMBB) are certainly different from the requirements for uRLLC or massive machine type communication (mMTC) [7]. The complexity of
wireless communications processing combined with the multiplicity of services and the varying goals of stakeholders makes it a most challenging area for architecture exploration. We would argue that an efficient solution would be difficult, if not impossible, to achieve without a deep understanding of the application domain.

At the highest level, wireless base station modem consists of an uplink flow and a downlink flow [29]. To minimize power and cost, in a cellular system multiple spectrum channels of this flow are implemented simultaneously on a baseband L1 System on Chip (SoC). This provides some unique challenges to the system designer.

1. Each channel is a dataflow system with strong dependencies along a flow of data from the antenna to the layer 2 processing in uplink and in the reverse in downlink.

2. They are Firm Real Time (FRT) Systems in that there is no point in continuing to process a flow once it becomes apparent it will not make its deadline. But a flow can be occasionally dropped (leading to an occasional loss of a user packet or a slightly degraded estimate) without harm to the performance of the SoC as long as it does not lead to an avalanche effect through the system [41]. So flows must maintain real time isolation.

3. Streams have different QoS levels both because of the different types of channels in the modem (such as PUSCH, PDSCH, PRACH [29]) and also because different use cases require different data rates and QoS (such as video streaming versus Industrial control).

4. Channel density requirements are very aggressive so high levels of parallelism are required on the SoC and hence the dataflow must be represented in a Model of Computation (MoC) that allows for parallelism.

5. Every transmission slot the Layer 2 spectral management algorithm will choose a new set of users to transmit and receive, changing the dataflow requirements. Slots can be sub millisecond in size. This leads to a challenging runtime scheduling problem in time and across resources.

6. The SoC must be highly reliable and withstand Heisenbugs in the field at a rate of less than one crash in the lifetime of the SoC [14].

5th Generation cellular wireless (5G) exacerbates these problems with an even more varied and flexible set of potential modes of operation at higher data rates with more independent users on SoC. As a result the development of 5G baseband software has become tremendously difficult and error prone if done by hand.

1.3 Achieving Automation with Efficiency in 5G Modems

Currently, the modem SoC used in 3G, 4G and now 5G systems are highly optimized SoC with high potential capacity and many accelerators [35] as well as specialized Digital Signal Processors (DSPs) optimized for fixed point and floating point, and with specialized instructions for modem operations. Essentially the embedded system space, and modem development in particular, has been developing DSA for many years now. The missing link between modem development and the new philosophy of DSL/DSA is that the current modems remain hard to program with much detailed hardware architecture knowledge required by the programmer. Once a modem has been programmed and tested the process of upgrading or modifying is difficult and time consuming and this limits innovation. So a DSL could be used to simplify this process. But to develop a successful DSL for 5G modem design the DSA must also be modified to be an efficient target for the tool chain supporting the DSL. Therefore the development of a successful DSL/DSA solution requires a holistic approach to the DSL/DSA that supports

1. the DSL that describes the requirements in a suitably abstracted and hardware independent manner.

2. the toolchain that automates translation of those requirements in an efficient and robust manner, provides formal guarantees against Heisenbugs, and recovers rapidly from dropped dataflows while continuing to achieve the real time requirements of most flows.

3. the DSA that is the target that supports the toolchain output with specialized processing, data management and control features with high performance and low power.

One of our chief concerns in development of this DSA is to make sure the architecture can be formally checked to remove Heisenbugs that can occur when real time constraints interact with limited memory and functional run time uncertainty. Uncertainty in the data flow is the result of many practical issues:

- Limited memory is a direct side effect of power and latency requirements that force data to be stored on the SoC in physical locations. Virtualization of memory is often not possible due to the dramatic latency hit that will occur in the event of a page miss.
• Real time constraints force data to be dumped in memory by a certain time so the resources can be reused for another part of the data flow but if the memory is full at that time there will be a real time failure or a write before read error that can be hard to debug in a lab environment.

• Run time uncertainty occurs because the functions have many parameters that directly impact the complexity of the computation or the size of buffers to be processed. To create unique dataflow for every parameter combination is impossible so there will be run time uncertainty as well as data buffer size uncertainty associated with any dataflow node in the system.

• Competition for resources among data flow is a necessity to ensure efficient use of resources in the SoC. But when combined with run time uncertainty and local scheduling (a necessity to keep control overhead under control) it leads to uncertainty in the temporal ordering of dataflow node processing. Scheduling is generally an NP complete problem and so only a heuristic solution is possible.

This issues will worsen for 5G due to tighter latencies and a much larger set of requirements and use cases and then become much worse for 6G as can be seen in Figure 1.1.

![Figure 1.1: 5G to 6G requirements change highlighting latency and security as issues (Source [1])](image)

**1.4 What is wrong with current SoC solutions**

Today the SoC solutions for baseband modems are dominated by OEM developed SoC and there is little information made public as to how they are programmed. However the public information that we have reveals that they are all built on what could be called a "Semi-coherent Global Virtual Memory" domain specific architecture which for brevity we shall call the GCM-DSA. An example of such an SoC is shown in [35]. SoC development in OEMs relies heavily on existing IP including memory controllers, crossbars and caches. These are hard to specify and verify and the IP provided by 3rd parties is configurable to allow for a wide variety of solutions. 3rd party code development and debug tools are also used and the expertise of the engineers tends to be in the development and maintenance of code in a global memory mapped system. Engineers will worry that debug will be difficult unless every register is exposed for peek and poke.

All of these practical constraints push the system designer toward a classic three layer coherently cached system out to DDR. But this leads to all sorts of timing uncertainty in turn leading to performance losses and tricky Heisenbugs. Maintaining latency constraints is then dealt with by exposing the L2 memory in the memory map or even exposing the L1 memory and hand managing the movement of data directly to and from the compute elements. Indeed for hardware accelerators caching is often not an option at all. This will lead to a complicated mixture of uncached compute elements, compute elements that are cached to and exposed L2 and some that cache all the way to DDR. Data movement is a
mixture of hand managed using DMA and caching. ARM, the leader in embedded system SoC IP, has extended its coherent bus “Corelink” specification to support a smorgasbord of cached and uncached transactions but turning these into a workable system requires experience and care.

In summary, modem SoC are built as a GCM-DSA using IP that is not intended for the modem use case and it leads to many practical difficulties in programming these devices:

- Cached systems lead to timing uncertainty and Heisenbugs.
- Mixtures of cached, uncached, coherent, noncoherent regions are left to the programmer to manage for correctness.
- Global memory exposure leads opens the system up to tricky Heisenbug problems due to read before write and write before read errors and buffer overflow errors.
- Maintaining latency is done in an informal way by individual programmers and can break down when the system is integrated.
- Hand management of data movement using a “distant” control processor in a cached region can lead to significant control overhead and latency.

In we outlined the “Russian Doll” methodology often employed to manage the SoC but this “super set of worst case” design approach has become highly inefficient because there are so many new use cases that use the system in significantly different ways.

1.5 Summary of the goals and flow of this report

In this report we describe the progress towards a Domain Specific Solution for modems in 5G and beyond. We use Dataflow as the basis to develop a DSL for the modem and show that an accelerator architecture can be developed to efficiently support this new language. That is, we develop a DSA suitable for our DSL. We then show that this DSL/DSA combination can be formally checked for the kinds of difficult bugs we described in this introduction.

We start in Section 2 with a description of how to apply dataflow methodology as a DSL for baseband modems introducing the concepts of DataFlow (DF), DataFlow Fragments (DFF) and MicroFlows (MF). In Section 3 we provide a top level description of our DSA and the overall tool flow that we are heading towards. In Section 4 we describe the DSA in detail. In Section 5 we describe the formal checking aspects of the toolflow with detailed examples of how we modeled the DSA/DSL and applied formal checks to the dataflows. We conclude and describe the work currently being planned and in progress in Section 6.

The report has two Appendices giving more detail of a detailed simulation model in the Mirabilis tool and details of the Message Formats used to manage dataflows in the DSA.

2 Wireless Baseband Dataflows

2.1 Dataflow Graphs

Wireless baseband processing, like many other real-time workloads, can be modeled as a dataflow graph. In a dataflow graph, processing is modeled by “actors”, which are represented by circles, and communication is modeled by “edges” or lines. Actors produce and consume “tokens”, which are units of granularity of data along an edge. An example of a dataflow graph is shown in Figure 2.1.

![Figure 2.1: Dataflow Graph](image-url)
In more complicated dataflows, such as those required for wireless baseband processing, tasks may be decomposed into large granularity subtasks, which we refer to as dataflow fragments DFFs. Dataflow fragments may, in turn, be further decomposed into kernels, or tightly coupled collection of kernels, which we refer to as microflows. An example of a hierarchical decomposition of a dataflow graph into dataflow fragments, and subsequently into microflows is shown in Figure 2.2.

The reason for the introduction of new terminology is to provide a precise mapping between an abstract level of hierarchy in a dataflow graph, and a concrete level of hierarchy in the actual hardware. In our architecture, a DFF is an actor at the top level of the dataflow and executes on a dataflow accelerator called a Service Resource Element (SRE), which will be described in detail in Section 4. A microflow is an actor within a DFF and executes on a single stage of the SRE. A stage is both a logical and physical partitioning of the SRE that contains the actual kernels and computational units needed to execute a microflow. The dataflow to hardware mapping is summarized in Table 2.1.

| Dataflow Abstraction Level | Hardware Mapping |
|---------------------------|------------------|
| Dataflow Graph            | Single or Multiple SREs |
| Dataflow Fragment (DFF)   | Single SRE       |
| Microflow                 | Single SRE Stage |

Table 2.1: Dataflow to Hardware Mapping

The following section gives an example of how an essential wireless baseband function, channel estimation, can be mapped to our architecture.

2.2 Channel Estimation Decomposition

Channel estimation is a fundamental operation in wireless communications. Before a message can be transmitted over a channel, the properties of the channel must be determined. In 5G communications, the transmitter sends out known reference signals over multiple antennas at various frequencies and time intervals. The receiver can compare the actual received reference signals with the known transmitted reference signals and use this information to construct a channel model. A detailed discussion of channel estimation can be found in [29].

The channel estimation function is represented in our architecture as a dataflow fragment (DFF), as shown in Figure 2.3. A DFF is a directed, acyclic graph that defines the connectivity between microflows. The microflows are the actual kernels that execute on compute elements.
DFFs are created statically (offline) for different scenarios. Because it is impractical to precompute all scenarios of a DFF, a number of commonly used scenarios are defined. We refer to a specific DFF scenario as a “container”. In order to run a particular DFF, we must select the appropriate container in which our DFF fits. Figure 2.4 shows four different scenarios for channel estimation, while Figure 2.5 shows the corresponding container for scenario 1. In scenario 1, the input data size varies from 768 to 960 bytes, and the output data varies from 1536 to 1920 bytes. Hence, for scenario 1, we define a container that processes the worst case input size of 960 bytes and the worst case output size of 1920 bytes. With careful selection of containers, we can minimize the over allocation of resources. The advantage of containers is that we can accurately predict the resource requirements of a new DFF request, and whether it will interfere with DFFs that are already running on the machine. We can choose to reject a new DFF if it will cause other DFFs to miss their deadlines, thus providing isolation between DFFs.

Once a DFF as been accepted into the SRE, its microflows are loaded from memory. Each microflow contains producer and consumer information, the kernel to be executed, and the stage on which the microflow runs. All microflows belonging to the same DFF inherit a global tag from the DFF, which uniquely identifies each DFF instance in the system. Additionally, each microflow within a DFF has a unique local tag which has been precomputed. The (global tag, local tag) tuple uniquely identifies any microflow within the system.

For the channel estimation example in Scenario 1, the microflow decomposition is shown in Figure 2.6. Notice that microflow 0 (i.e., the microflow with local tag 0) is always reserved to represent the DFF container. Hence, one can think of all microflows within a DFF as living inside the container boundary of microflow 0. This creates a simple numbering system for any microflow to communicate with the top level ports of the DFF. For instance, microflow 1, CHEST1_L1metaDataExtractor, gets its input, L1metaDatafromDW_perSegment_src, from input port 1 on microflow 0. Similarly, microflow 6, CHEST6_dataMove_FP2SRE1, sends its output, outChannelEstmAllLayerPerLU, to output port 0 on microflow 0. A microflow will fire (begin execution) when all of its inputs are ready, and will retire when all of its outputs have been consumed.

In this example we have shown how channel estimation can be represented as a dataflow fragment (DFF), which can
be subsequently decomposed into microflows. We believe this methodology can be extended to many different functions in wireless baseband processing, as well as other application domains.

3 A Novel Architecture and Toolchain Approach to Modem DSS

In order to deal with these issues outlined in Section 1 we propose a general philosophy of:

- "Dataflow Native" hardware that
  - supports complete DFFs efficiently mixing in shared memory and compute resources.
  - enforces stateless representation of flow, with all records erased locally on completion.
  - simplifies Heisenbug management through stateless DFF management.
  - simplifies security via containerization of DFF (memory management stateless operation)
  - maximizes functional flexibility with minimal control overhead using a hardened “OS”

- “Firm Real Time Native” hardware that uses a policy based “pause, run, drop” strategy to removed the avalanche effect if a flow fails real time.

- “Energy Management Native” hardware that
  - supports tooling for formal checking of performance.
  - manages the flow of data thru memory as first class citizen.
  - formally checks flows to manage energy rather than using speculation
  - maximizes processing near/in memory

3.1 Hierarchical SoC decomposition and Formal Analysis

In order to allow a formal check of the SoC and also to make each layer as stateless as possible we propose a hierarchical decomposition. The top level of the SoC architecture is the cloud. Recognizing that all devices will be connected to the cloud we propose to use the cloud for long term control and configuration of the SoC for energy efficiency and formal verification of dataflow mixtures as part of the admission process for the SoC. Unlike previous generations, to our knowledge, the SoC is “dead in the water” without cloud connectivity with the cloud playing a critical low rate but continuous role in the reconfiguration of the SoC as shown in Figure 3.1. The cloud will set parameters related...
to performance such as policy and scheduling (to be described in next Technical Report) that are used over a long configuration period during which time a certain mixture of DFF arriving within a know range of patterns is present in the SoC. Performance feedback at this level is also possible and can be used to tune policy.

The SoC itself is an array of loosely connected DFF processing elements called Service Resource Elements (SRE) that are inspired by the Channel Elements from CDMA. The operation of the SRE is a critical component of our overall SoC strategy and we focus on it in this report. Its most salient top level features, seen from the SoC level are:

- The SRE receive DFF control packets and then DFF data inputs, which they process to produce data outputs for the next DFFs.
- Each DFF is a self contained DAG and is processed to “stateless” completion leaving only its outputs are result.
- There is a SoC level model for the arrival pattern of DFFs of each DFF flow. A flow of DFFs simply being a continuous arrival of DFFs at an SRE that is grouped for analysis convenience.
- The SRE is not allowed to back pressure a flow. This means that the arrival pattern is maintained and can be formally analyzed.
- The SRE must also produce output data from a flow within the bounds of an SoC level departure pattern. SRE will be formally checked to make sure it achieves the pattern.

Once the input and output patterns are formally verified for an SRE it becomes a black box for SoC level checking of dataflow. The three concepts or input and output flow patterns and formal checking of each SRE to these patterns allows a hierarchical decomposition of the behavior of the SoC. The toolchain we present is therefore a critical aspect of this decomposition as it provides for a formal checking of the SRE when it experiences a set of flow patterns. The Complete formal toolchain is shown in Figure 3.2. The flow is as follows:

1. The Application engineer provides a set of DF along with the pattern of creation for each DF type.
2. The DF are partitioned into DFF using a dataflow tool such as the open source tool PREESM (see Section 3). This produces DFF with derived creation patterns.
3. Based on the DFF patterns each DFF type is statically mapped to one or more SRE. We have used spectral graph theory and an edge weight based heuristic to perform this and get intuitive results and have also used SAT and ILP. The static mapping allows us to develop patterns of DFF arrival for each DFF type for each SRE, though we have not automated this process yet.
4. The DFF DAG along with its data packet and runtime ranges is converted to a model in a formal analysis tool. We use a Timed Automata (TA) metamodel converting from the xml output from PREESM to a format suitable for the UPPAAL TA analysis tool using a Python program (see section 5).

5. The patterns of arrival and the DFF DAG are combined with a TA model of the SRE architecture and the complete SRE model is formally checked using a set of queries. If all queries pass the DFF loading on the SRE is considered to be formally feasible. If it fails the query(s) that fail will pinpoint the reason for failure and human intervention will be required to adjust the input real time application requirements. How to automate the process of relating the query failure to suggestions for how to modify the requirements is a topic for future research.

3.2 The Service Resource Element

The service resource element (SRE) is the fundamental building block of our domain specific architecture. It was designed from the ground up to address the challenges encountered with current modem implementations. It was architected to work specifically with our tool flow and our application development philosophy. A high level view of the SRE and its internal structure is shown in Figure 3.3.

3.2.1 SRE basic structure

In an SRE-based modem design, multiple SREs will be connected together using a network-on-chip (NoC). Each SRE is a computing cluster that can process several dataflow fragments (DFFs). An SRE is further partitioned into stages, where each stage processes individual microflows (refer to Section 2 for a more detailed description of microflows).

3.2.2 SRE interface to processing flows, Policy and Control

When a DFF needs to be processed, an external host, which could be another SRE, sends the SRE a control packet to request the necessary resources. The control packet generates a request to the director (the top level controller of the SRE), which applies a policy to determine if the request will be rejected or accepted. The policy is a set of rules that determines if any predetermined resource allocation strategies, which we refer to as "Tetris" blocks, can be safely deployed given the current system load. If the request is rejected, the director tells the packet processor to discard the corresponding data packets and to inform the initiator that the request was denied. However, if the request is accepted, the director informs the packet processor that the corresponding data packets may be stored in the data buffer.
3.2.3 SRE DFF decomposition and Microflow processing

As the data arrives, the director dispatches microflow descriptors to one or more stages. A microflow descriptor tells a stage everything it needs to know about how to execute a particular microflow, including where to get its input data, what kernel(s) to use, and where to send the output data.

During execution, microflows in a DFF consume, process, and produce tokens. A microflow fires when all of its inputs are ready, and retires when all of its outputs have been consumed. Microflows may send and receive tokens within the same stage, or may be required to send and receive tokens across stages. However, microflows that produce final output tokens (i.e., tokens that are the outputs of the DFF itself) send their output tokens back to the data buffer. Multiple microflows may be in flight at the same time on the same stage and a DFF may spread across multiple stages.

3.2.4 SRE DFF completion

Once the packet processor has received all output tokens for a DFF, it sends the output data onto the next assigned processing block (this could be the same SRE, a different SRE or a SoC level control block) as one or more data packets. In keeping with our robust design philosophy, any microflow that fails to meet its deadline, or malfunctions in some other way, should not cause unrelated microflows to fail. If a microflow times out or fails, it deallocates its resources, cleans up its state, and generates an error code (see Section 3.2).

The following sections describe the SRE architecture and formal toolchain in more detail.

4 The SoC Architecture of an SRE

Fig. 4.1 is the SoC block diagram of an SRE. The SRE has been architected to be highly configurable driven by the real system requirements imposed by the application, in our case wireless baseband modem. The SRE can be reconfigured during two different points in time. The first one is during integration time where we can configure it with static system specifications such as number of sectors or number of antennas, these usually represent a typical base setting of base stations; these static configuration requirements and can be obtained once an SoC specification is derived.

The second one is the run-time reconfiguration enabled by the run-time selection of the number of stages, and reconfiguration of the processing engine called SHOC, SHOC will be covered in great details in section 4.2.

Though we have architected the SRE to be highly adaptive and flexible, it is also architected to support temporal composability without losing the need to satisfy the real-time QoS (Quality of Service) requirements mandated by wireless baseband processing. By its intrinsic nature a PRET (PREcision Time system) [31] tries to improve overall resources utilization to further reduce the costs. It is therefore treated as a template for the SoC integration and development, which consists of the following key elements:
The Director and Packet Processing Subsystem: This subsystem is responsible for the control and data interfaces between an SRE and the rest of the SoC. It receives and interprets control and data packets, and generates, populates and terminates DFF information to the stages assigned. It also co-ordinates data packets’ admission, sets up necessary data triggering information to the assigned stages that have ingress and egress interfaces, and orchestrates data movement once a DFF flow is completed.

The Flexible Stage Subsystem: This subsystem consists of multiple identical collections of resources as shown inside the dash line plus the dependency resolver with the token table and actor list shown in Fig. 4.1. It is the working engine of the overall architecture and it can be dynamically triggered based on relationships defined by data flow graphs with the combination usage of the data dependency resolver, the actor list and token table inside of a stage. Also, the SHOC(s) is(are) can be re-configured during run-time by the stage manager and depends on the functions defined by the data flow fragments assigned for a specific stage. SHOC (Scalable Hybrid and Organizational Computing) element will be described in greater detail in a later section and consists of heterogeneous components that meet the high PPA efficiency required by the baseband processing system.

The Control and Data Infrastructure: This subsystem consists of three switching interconnects: one is the control and management crossbar located in the top of the figure and is dedicated to control information exchange inside of an SRE; the second one is the data-flow based interconnect reserved for the NoC interface; The third one is located at bottom right of the figure and works together with the shared buffer and memory subsystem.

The Shared Buffer and memory Subsystem: This subsystem takes the lion share of the area inside of an SRE. It is a distributed and shared memory subsystem [33] and it basically has interfaces to all the other architectural components for data exchange purposes.

The DMA Subsystem: This subsystem is under the supervision of the stage manager(s), the director and packet processor inside an SRE so to efficiently move data across multiple stages and to the rest of SoC.
4.1 Functional and Operation Description of an SRE

4.1.1 The Director and Packet Processing Subsystem

The director and packet processor are two different cores that work in tandem to provide top level control for the SRE (Figure 4.2). The packet processor’s primary responsibility is to keep track of control and data messages, while the director handles policy implementation, descriptor creation, and supervisory functions. Both processors are expected to be RISC V based cores with instruction set extensions and specialized coprocessors.

The general steps for executing a DFF on an SRE are:

1. Request DFF resources
2. Wait for input data to arrive
3. Execute DFF
4. Send back output data

When the host wants to process a DFF, it first sends the SRE a control packet, which tells the SRE which resources it requires (Figure 4.3). The control packet contains a global tag, which identifies the unique instance of a DFF in the system, and a container id that specifies the type of graph that best matches the DFF to be executed. The control packet is forwarded to the director as a DCT (container type) request. If the particular container type is supported by the SRE, then the director sends a DFF descriptor back to the packet processor so that it can begin receiving data packets. However, at this point, the director has not yet accepted the request as it has not yet determined resource requirements.

The director applies a policy to the request to determine if it can be accepted by the SRE. In order to avoid being a computational bottleneck, resource requirements of a container are pre-computed in one or more “feature vectors”. The director examines several feature vectors associated with a DFF container to see if any mapping will fit inside the machine given the current system load. We refer to this step as playing “Tetris”. If no mapping can be found, the director reports an error and instructs the packet processor to discard the DFF descriptor and any corresponding data. However, if a mapping can be found, the director sends a mapping ready signal back to the packet processor and begins to load the graph from external memory.

Note that the graph is not loaded explicitly, in the form of nodes and edges, but implicitly as microflow descriptors. Each microflow descriptor contains information about its inputs, outputs, kernel(s) to be executed, and the stage on which the microflow executes. Microflows within a DFF are identified using a local tag, which is statically determined. When the director reads a microflow descriptor during run time, it appends the DFF global tag to the microflow descriptor. This allows a microflow instance to be uniquely identified using a (global_tag, local_tag) tuple. The complete microflow
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Figure 4.3: Requesting DFF Resources

descriptor is then sent to the appropriate stage where it will be executed. Once all microflow descriptors in a container have been sent to their appropriate stages, the director sends a microflow ready signal back to the packet processor.

While the director reads microflow descriptors and dispatches them to the appropriate stages, the packet processor is collecting data in its ingress buffer (Figure 4.4). The packet processor sends a pointer descriptor to the appropriate stages indicating where the DFF inputs are arriving. Once all input data for a dataflow fragment has arrived, and all microflow descriptors have been dispatched by the director, the packet processor sends a data ready message to the appropriate stages, indicating that the DFF is ready to execute.

Once the input data is ready, all awaiting microflows are activated and execute the DFF. Microflows within a DFF continue to pass intermediate tokens within a stage or between stages until a DFF output token is produced (Figure 4.5). When a DFF output token is written back to the egress buffer, a DFF output ready signal is also sent back to the packet processor so it can keep track of the output tokens. Once the packet processor receives all output tokens for a DFF, it sends the output data back to the host in the form of data packets. The packet processor also sends a DFF release message to the director and all stages indicating that the DFF has completed execution.

4.1.2 The Flexible Stage Subsystem

Multiple homogeneous stages can be instantiated during the integration time. As shown in Fig. 4.6, every stage is activated and triggered by the input token(data) and works on the granularity of a microflow/kernel. It is passively driven by the microflow/kernel assignments deployed by the director. Once the director has finished to assign the miroflow/kernels of a DFF to a particular stage via control messages. The token table and actor list for a stage are populated to capture the connection information of data flow graphs, microflow/kernel trigger conditions and dependency information among

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them. The data dependency resolver is triggered by any control message sent from the director and other stages or data triggering events generated inside the same stage.

The data dependency resolver is responsible for interpreting the control messages from outside a stage and any relevant events generated inside the same stage. It can be implemented by a group of finite state machines to fulfill table searching and condition evaluations as shown in Fig. 4.8.

Once one or multiple DFFs are triggered and ready to run after the evaluation of the data dependency resolver, it(they) will be presented to the stage manager via the ready list of the DFFs, which is normally implemented by a queue. The stage manager is responsible for the following tasks inside a stage even though its functionalities are captured in two separated boxed in Fig. 4.6

- **Miscellaneous Managements Tasks Inside a Stage:**
  - Taking the relevant information from the input arcs such as the size of input tokens of a microflow/kernel that is ready to run
  - Preparing a DMA transfer parameter list if a DMA is required to move the input tokens from other stages.
  - Checking the available buffer space for a stage and presenting the information to the scheduler and pool manager for further decision making
  - Maintaining and updating the ready queue list based on a microflow/kernel completion status
  - Sending necessary control message to the other stage(s) or generating the necessary event for the same stage once a microflow/kernel is completed successfully

- **Run-time Scheduling:** It is a very important role for the stage manager to apply different scheduling algorithms such as Early Deadline First, round robin based on the timing information carried in the meta-data sub-field in the actor list as shown in Fig. 4.8.

- **Resource Pool Management and Allocation:** Once a micro-flow is scheduled, the stage manager acts as a pool manager to reserve output tokens from the shared buffer memory inside a stage. It also reserves the computing resource (SHOC in this case) so the scheduled microflow/kernel has the necessary resources to finish on time.

- **SHOC Reconfiguration:** It is responsible for re-configuring a SHOC(s) during run-time if and when a new SHOC image is required to perform a different function than the one it is currently assigned. This task is called upon once a DFF is scheduled and the pool manager has reserved the necessary resources for the scheduled microflow/kernel.

Fig. 4.7 shows the operation flow of a typical stage. We need to cross-reference the definitions of Actor List and Token Table shown in Fig. 4.8 to understand how it works. Fig. 4.8(b) shows an example snippet of a DFF. Microflow A and I are input arcs to trigger the microflow H, and microflow B is triggered by the completion of the microflow H afterwards.
As shown in Fig. 4.6(a), there are multiple entries in the actor list inside Stage I and II. The actor list consists of multiple uniform-sized entries, each entry is employed to describe one microflow/kernel out of many assigned to a stage. Because each microflow/kernel might have a different number of input and output arcs, we employ a second table called token table to handle the irregularity. In each actor list entry, there is a subfield called Entry-depen-loc, this is the pointer to locate the full definition of all the input and output arcs of a microflow/kernel defined in the corresponding actor list.

As mentioned previously, the data dependency resolver evaluates the readiness of all microflow/kernels assigned in a stage once a control message is received from other stages or an internal data event is generated. Please note the definition of ready is the availability of tokens for all input arcs of a specific microflow/kernel. With that, we called the microflow H is ready only when both the input tokens of input arc A and I are available for microflow H in stage Stage I. The data dependency resolver sets the Rdy bit in entry of microflow H and pushes relevant information to the ready queue in a stage.

As described in Fig. 4.7, the stage manager takes over beyond this point. It prepares all the necessary information such as the timing information carried in meta-data of the actor list, and the loading of a stage and the configurations of a SHOC(s) etc. to the scheduler so that it can make an optimal decision. Once a microflow/kernel is scheduled, the Sched bit in the corresponding entry of the actor list will be set. At the same time, the scheduled task is passed to the pool manager so it can allocate the buffers/tokens for all the output arcs. The pool manager also needs to reserve the computing resource (SHOC in this case) so the microflow/kernel can be accommodated. The pool manager notifies the stage manager if a re-configuration to the allocated/reserved SHOC(s) is(are) required.

The last step before a microflow/kernel runs is to wait till the re-configuration to a SHOC(s) is(are) completed. The stage manager monitors the re-configuration and it also sets up the necessary parameters to SHOC(s) so it(they) can run properly once it triggers the SHOC(s) to run. The corresponding RUN bit for a scheduled entry in the actor list will
Once the SHOC has completed an assigned microflow/kernel, it triggers a data dependency resolver and stage manager in the same stage so that the data dependency resolver(s) located in other stages can start to evaluate any other microflow/kernel dependencies based on the completed microflow/kernel. For example, for microflow A and H, they both belong to stage I. Therefore, once microflow A is completed, an internal event will be created and it triggers the data dependency resolver in stage I to evaluate whether microflow H can be ready to run or not. In another scenario, microflow/kernel I belongs to stage II as shown in Fig. 4.8, the stage manager located in stage II is responsible for sending a control message to stage I once microflow I is completed. The corresponding control message routed from stage II to stage I via the control and management crossbar triggers the data dependency resolver located in stage I to evaluate all microflows/kernels that depend on the microflow I. Then the operation flow chart described in Fig. 4.7 starts.

As the very last step of the operation flow, and after a microflow/kernel is completed, the stage manager removes...
the corresponding entry from the ready queue list, resets the corresponding Rdy, Sched, RUN bits for a completed microflow/kernel in the actor list. The same microflow/kernel now is back to the normal waiting state and waits for further data triggering. The stage manager also needs to release the input buffers reserved for the completed task and be ready to give the ownership of all the output buffers for the relevant triggered microflow/kernel(s).

If the running microflow/kernel is the last segment within a complete DFF, it needs to send a control message to the director/packet processor to notify the completeness of the whole DFF. This way, they can take further actions with regard to the whole DFF for things include but not limited to the following:

- Set up DMA parameters to move the final results of a DFF to the rest of SREs on the SoC. Release the output token buffer spaces once the data is moved out completely
- Retire the completed DFF entry deployed across multiple stages if the same DFF will not be run beyond this point

4.1.3 The Shared Buffer and Memory Subsystem

The SRE is a native dataflow architecture, thus it works on the granularity of a token, which is directly mapped to a buffer or FIFO in the SoC micro-architecture. During the run-time, buffers that hold tokens are created and released along with a dataflows that are activated or completed on the fly. The size of a token varies a lot and it could have multiple producers and consumers to access it at any time. Also many producers and consumers spread across multiple stages, spatially all need to access the shared buffer(s).

This dictates that the memory architecture be shared and distributed in nature. It also needs to accommodate multiple shared buffers with different sizes that can be accessed from many ports. This brings up a difficult challenge to the overall memory subsystem inside an SRE. Therefore, we need to apply our latest shared memory techniques described in [33].
and aided with the window-access technique described in [18] as the starting point for the next level of micro-architecture.

4.1.4 The Data and Control Infrastructures

Inside of an SRE, there are three switching networks in Fig. 4.1 to support the following needs:

- **The SRE Internal Control and Management Crossbar**: It is responsible for the control message communications among the director, packet processor and stage managers inside the SRE. The interconnect carries short control messages and needs to have very short reactive time to make sure all important messages can be routed from source to destination as quick as possible. It also needs to have properly acknowledgment sent from the recipient to make sure no important information gets dropped.

- **The NoC Interface Crossbar**: It is responsible for the data exchanges between the rest of SoC and the shared buffers inside of an SRE. It often carries big and long data packets, however, any connected route has a much longer live time than that of the control and management crossbar because director/packet processor sets up the connections on a granularity of a dataflow. It can be treated as a slower switching network inside of an SRE.

- **The Dataflow Mapped Distributed Buffer Network**: It can be considered as part of the overall shared buffer memory subsystem. Once again, it works at the granularity of a dataflow and it carries the bursty and windowed traffics to a portion of a shared buffer(s) most of the time. The access protocol is a very simple since it directly interfaces with single or two port SRAM.

We have considered TileLink [42] as the basis to implement all of the three switching networks described because it offers multiple protocols with the same foundation but at different level of implementation complexity. With that, the SRE internal control and management and NoC interface crossbar are based on TileLink Uncached Heavyweight (TL-UH) protocol because it provides robust handshake scheme to guarantee that no information gets lost; and the dataflow mapped distributed buffer network is based on TileLink Uncached Lightweight (TL-UL) protocol for the purpose of easy implementation. One more reason why TileLink is considered is because a couple of open-source RISC-V cores are evaluated for the implementation of the director, packet processor and stage managers. They all support TileLink interfaces so TileLink enables a fast prototype and smooth integration capability.

4.1.5 The DMA subsystem

There isn’t any special requirements to the DMA engine from the SRE perspective. The only requirement is that it can support multiple “data moving engines” that understand the nature of multiple dataflows moving tokens in and out any stage, or in and out of the SRE simultaneously. There are many choices for this sub-system.

4.2 The Scalable, Hybrid and Organizational Computing (SHOC) Architecture for Multi-Application Domains

4.2.1 Introduction to Scalable Compute

Until breakthroughs of computing technologies such as quantum computing and/or graphene/CNT processors are productized, CMOS based technology remains the only choice for the chip processor industry. Therefore, effectively using existing technologies to build PPA efficient products, that need to meet exponentially increasing computing demands, remains a big challenge which is faced by the entire chip industry in the post-Moore’s law era. Particularly in the wireless industry, as we evolve from 5G to 6G, not only will the computing demand increase dramatically, but the variety of application domains will no longer just be wireless modem applications, these would be extended to other domains like AI/ML and applications like sensing and positioning. This requires a “6G modem” that’s more flexible and generic than conventional wireless modems, in addition to having much higher PPA efficiency and supporting hard real time requirements than previous generations (4G/5G) systems. An efficient and flexible computing system is a must for future 6G computing.

Since Dennard scaling ended in 2004, the clock rate could no longer be raised, and computing components can only be spatially expanded, from single core to multi-core, and then to many cores. Around 2008, the concept of “dark silicon” started getting popular, it claimed some parts of the chip would have to be powered off to avoid high power consumption and excess heat generation. However, one might ask the question, if silicon is partially used, why put it in
in the first place? perhaps re-usability would be a better solution. In the end, there is little clarity on how to deal with the post-Moore’s Law era and most chip companies continue to rely on scale rather than efficient use.

Scientist and engineers realized long time ago that a single technology cannot meet computing demands, and that different computing technologies should be combined to meet the challenges for low power and area designs, particularly in post Moore’s Law era. For many years, the GPP industry has been trying to solve these problems by adding more programmable and customized accelerators to the main CPU/DSP cores; the FPGA industry has been taking the approach of embedding more pre hard-wired DSP/CPU blocks with fixed bit precision, which sacrifices the FPGA’s fine grained flexibility that supposedly could generate arbitrary types and precision computing elements; GPUs, originally designed for video processing, have been modified to support more generic applications and integrate TPUs to improve the compute efficiency for neural networks. The recent NVIDIA plan to acquire ARM confirmed this direction. Since Google’s TPUv2 published stunning energy and performance numbers over CPU and GPU in 2017, TPUs have been evolving from a programmable ASIC processor to a more flexible and higher performance processor to cover ML training tasks, (not just inferencing as in TPUv2) and hoping to be used for an expanding set of applications. In the recent two years, the top two processor manufacturers, Intel and AMD each acquired the two largest FPGA companies, hoping to increase the computational efficiency of GPPs through the flexibility of FPGA. The decisions seem largely impacted by the research results of Microsoft’s Catapult project, which claimed that at a cost of 10% power increase brought by FPGA boards they could gain 90% throughput improvement for their search infrastructures [40].

We have observed in past several years that there isn’t a single technology, or multiple technologies for that matter, that can use a brute force approach in single or multi die chiplet, to dominate the industry as a mainstream general purpose processor with wide acceptance. Particularly in the wireless industry, where energy and area are extremely sensitive, GPP processors do not fit the requirement of low power and area, let alone meet the requirements for hard real time and latency. We have to consider a less general purpose architecture targeting the wireless application domain, enter DSA for wireless or WDSA. And for future 6G, we have to also support additional domains as discussed earlier in this section. In the rest of this section, we propose a computing architecture that can support multi-application domains but still meet the high PPA efficiency required by those applications.

### 4.2.2 Design Considerations for SHOC

The industry is moving towards more heterogeneous computing on a single die or multi dies to meet the challenges in post Moore’s Law era. Although different technologies can be packaged into a chip, there still exist large data movement, which not only increases latency, but also consumes too much energy not used for computing.

SHOC is hybrid and organizational, by which we mean there is no clear cut boundary between different technologies and/or computing structures, some part of the structure could change its functional roles and become a sub structure of another part in the structure at run time. With this method, we could let the computing system minimize data move and keep the processing locally as much as possible, and make the entire computing system more harmonious among each sub-system to achieve high utilization of the actual computing operators. After all, it is those operations that are useful for solving practical problems.

- **Configurable coupling (tightly/loosely) co-processors**: By tightly coupled co-processor, we mean that the host processor is dedicated to the co-processor for control and/or data LD/ST; loosely coupled means that the co-processor and the host can execute independently of each other after the co-processor is configured. In loosely coupled mode, the co-processors are acting like regular hardware accelerators.

- **Complementary of all aspects**: Real world problems are not so neat and tidy to fit in a pre-designed computing systems. People must partition and formulate the problems into computable equations that may have all large mix of the algorithms, operator types, precision, sizes, etc. On the other hand, the compute architecture should also provide sufficient flexibility and capability to efficiently solve the problems. Therefore, we need to consider different complementary pairs in computing systems: time-space, big-little, complex-simple, tightly-loosely, local-global, and so on. The complementary structure should also adhere to the 80-20 rule, which indicates the large part of a the computing problem can be solved with simpler and regular computing structures. However, one shall not let the 20% complex part stall the 80%. The SHOC architecture fully takes these considerations into account as part of its design.

- **X-architecture co-designs**: It is well known in the industry that 80% energy optimization is from algorithms and architecture co-design. In their 2018 Turing award lecture, Hennessy and Patterson also mentioned the benefits
of HW/SW co-design for high level languages, and compiler-architecture co-design for C-compiler and RISC architectures. They also predicted that new compilers for DSA could raise 10X computing efficiency [17]. In addition to this, SHOC also takes an approach of scheduling-architecture co-design, the figure below illustrates an example of how the latency could be reduced by the flexibility of SHOC.

4.2.3 The SHOC architecture

It is physically difficult and area/power cost prohibiting to try to build a fully connected network for all components even in a medium sized compute unit, say one with 16 CMAC (Complex MAC) and 32 memory banks. Therefore, a locally dense globally sparse interconnect scheme is used for SHOC. It takes a hierarchical structure and uses a full cross bar interconnect for local small Compute Element (CE) group and uses a less dense cross bar for high level interconnect. The gray cross boxes in Figure 4.10 show the interconnect top level.

Each CE group contains 4 CMACs of FP16 and configurable for a 2x2 array or a 4x1 vector. Four CE groups comprise a CE tile, and each tile is connected to the scratch buffers via a two stage cross bar. In between, a sharable thin slice of simple operators that can, on the fly, perform operations like data scaling, shifting or add/sub etc. for the data that passed through the two stages of interconnect, if being configured to do so. This way, the expensive CMAC operators can avoid performing simple real number operations, while the computing stages are reduced and the latency and storage could be significantly decreased.

The tiny cores and some of the special functional units and CE groups can be tightly or loosely coupled depending on the algorithms and performance needs to improve computing resource utilization. All the interconnects support neighboring sharing for computing and memory resources. Most of the CE groups are semi statically configured and operated like ASIC, thus SHOC can achieve close to ASIC performance. (A design comparison indicated SHOC is even better than ASIC for some applications.

In Figure 4.10, there are 128 CMACs, and the SHOC can be scaled up to larger system horizontally and/or vertically. The green arrow buses support control/configuration loading in addition to data from/to outside, and the red arrow buses support data transfer only from/to outside world. The tiny cores take care of the control/configuration in addition to computing.

4.2.4 Some performance analysis and comparisons

Because the majority of computing elements in SHOC execute like ASIC after configurations, which is a significant difference from the conventional programmable CGRA [39], we expect SHOC to achieve close to ASIC PPA performance. It is all about improving the utilization rate of computing elements that are actually needed to solve algorithms in applications. SHOC takes this as a key design criteria.

As SHOC is targeted for real time application domains, we mainly tackle single block data (batch 1) or small batch sized data blocks (batch 4). The reader should note that, it is not fair to compare parallelism in small batch processing to that in large batch sized processing, often used in offline computing, as it is much more difficult to apply parallel processing on a single data block (batch 1) where the parallelism must come from within the block in order to reduce
processing time for real time applications, rather than from an average over many blocks processing in parallel. However, processing fast for a single data block is important, and it can also significantly save areas and power, for instance in NN inferencing. In general, large batch sizes are easier to implement and can achieve higher utilization rate but cost more for data storage and data movement. Even TPUs can only achieve less than 50% utilization rate for training of NN with large batch sizes. GPUs do not fair any better \cite{47}. Here are some examples of SHOC performance.

- **FFT/IFFT functions**: In SHOC, there does not exist a dedicated module for FFT Special Functional Unit (SFU). Instead, we separate the butterfly structures and the twiddle MUL vectors such that only the butterflies are designed as configurable SFU (so the butterflies can be used for other functions if FFT is not needed) and the MUL vectors could be used as regular CMAC operations. This way, we saved significant computing areas and memory buffers for dedicated FFT hardware accelerators. Furthermore, the scalability of SHOC can combine smaller FFT components to support larger radix FFTs to achieve much better PPA performance. Based on a paper from Microsoft \cite{15}, the performance for SHOC is more than two orders of magnitude that of the GTX280 for a single 4096 point FFT, since SHOC as a DSA has much less area and power, the energy and area efficiency for SHOC would be much higher. Also, in the cases of smaller than 4096 FFT sizes, GTX280 would even be worse. (see the left curve diagram in Figure 4.11) From Figure 4.11, GTX280 utilization rate is less than 0.72% for FFT4096 and smaller (close to 0 for FFT16), and those size FFTs are the one required in 5G infrastructure applications. In the best case of large batch and large sized FFTs, the utilization rate is still less than 11%, while SHOC could reach above 90% utilization rate. This result is mainly achieved by algorithm-architecture co-designs. In SHOC, its FFT configurations runs like an ASIC, and use large radices as much as possible to improve parallelism and performance. If radix 3 and radix 5 need to be supported, we would expect GPU performance to be even worse. (For an early version of SHOC compared to a CGRA FFT configuration, SHOC achieved 100X energy efficiency for a 256 point FFT.)

- **Cholesky decomposition**: Cholesky decomposition is a widely used algorithm in matrix linear algebra, and heavily used in wireless baseband processing. It is highly spatially structured and highly data dependent. And its irregular matrix computation usually causes low utilization rate for many parallel processing systems on a single matrix (batch 1), which is preferred for our targeted application domain (here again the idea of DSA comes into play). Again, we applied algorithm-architecture co-design to take the advantages of SHOC’s spatial and temporal flexibility. We experimented on SHOC architecture for different matrix sizes ([8x8], [16x16] and [32x32]), and different parallel levels (CMAC vector [4x1], [8x1] and [16x1]). With the same number of parallel levels, SHOC achieved 5X ~ 8X performance efficiency on internal data comparisons and the utilization rate ranged
from 38% to 98% for this data set. Based on these numbers from different combinations of cycle-CMAC number pairs, the scheduler would choose the right parallel level based on available CMAC resources and load balancing considerations, thanks to the capability of SHOC’s variable length SIMD support.

- **Scheduling-architecture co-design:** A problem is usually partitioned into multi data flows (or micro flows), and then multi data blocks are fed in for processing. It is hoped that those data blocks could be processed in a way that they would start at the same time and finish at the same time, such that computing resources assigned to these data flows can be all ready for the next set of data flows. Otherwise, the processing latency would be dependent on the largest data flow processing time and those resources of early completed data flows would be wasted. Unfortunately, this is real world applications, and nothing is ever perfect. To deal with this issue, SHOC provides a switching mechanism that can facilitate the scheduler to find the best job sequencing to reduce the total latency.

Figure 4.12 illustrates this scheme, which is an example of temporal tessellation. The four colored data flows started at the same time from the bottom. They completed at different times (along the vertical axis). If all the four flows do not change their CE group assignments, as the new data blocks continue to be fed in, the green flow would complete first, and would be sitting there until the red flow completed last, and the idle time would be accumulated if many data blocks need to be processed. By switching their resource assignment, the idle time would not accumulate, the total latency will be significantly reduced, and utilization rate improved. The cost is more reconfiguration times, but it is acceptable because this is not cycle based dynamic reconfiguration, and it is only switching, no new different control bits need be loaded.

In a real modem algorithm of 3 matrices MUL case, this scheme can achieve 100% utilization rate and ideal latency, while a system without this method resulted in 75% utilization rate and longer processing time, given the condition that both cases have the same amount of resources.

- **Image processing examples:** The SHOC design considerations and architecture were also tested for the ISP (Image Signal Processing) domain, where the area and energy are very sensitive. We tested two algorithms and both comparisons showed SHOC is even better than ASIC designs on both area and energy thanks to the algorithm-architecture codesign and flexibility for area reuse (50% and 30% smaller areas respectively).
4.2.5 Challenges of next stages

We still have much work ahead. We need continue to work on the compiler-architecture co-design such that an automatic compiler tool can ease the use of SHOC. We will leverage existing high level languages and tools to speed up the development. Also, more features like variable precisions will be considered to support AI/ML domain, which is expected to have a high demand in 6G modems.

4.3 SRE Architectural Modeling and Explorations

4.3.1 Overview of the Mirabilis SRE Model

Mirabilis VisualSim Architect [19] is deployed to do the SRE architectural modeling and explorations. Fig. 4.13 is the top level view of the model and it has one-to-one mapping to the key components shown in Fig. 4.1. The very leftmost submodule in Fig. 4.13 is the stimulus generator that feeds in necessary control and data packets to the SRE. The rest is the full comprehension of an SRE. The model is realized to follow the operation flow described in Fig. 4.7. The details of the overall SRE model are described in Appendix A.

4.3.2 Early Results of the Architectural Modeling and Explorations

The SRE Mirabilis model is ready to produce some earlier results based on the Channel Estimation Dataflow Fragment described in Fig. 2.3. This DFF is used to bring-up the whole integration of the SRE model and is able to identify memory leakage issue exists earlier in the architectural exploration as shown in Fig. 4.14.

The x-axis represents the execution time of four DFFs, they are input to the SRE one by one with some overlaps among them. The y-axis logs the buffer usages along the dataflow execution against the time. The correct memory usage is that the buffer is being allocated after a microflow/kernel is triggered and should be released once a kernel is completed. And the memory usage should be back to zero once all DFFs are completed. However, one can observe that the memory usage keeps going up even though all of the four DFFs are completed in Fig. 4.14. The memory leakage issue is resolved after the relevant stage and memory subsystem is re-architected. As observed from Fig. 4.15 the memory usage returns back to zero once all DFF flow are completed so we can conclude the memory leakage issue is cleanly resolved.
Figure 4.13: Top Level Mirabilis Model for An SRE

Figure 4.14: Memory Leakage Issue Observed with Four DFFs Running Together

Figure 4.15: Memory Leakage Issue Corrected with Four DFFs Running Together
Other useful information such as DFF execution time/latency as shown in Fig. 4.16 can be observed to help fine tune the overall SRE architecture. This is the simulation result where the same DFF has been executed over twenty times. The x-axis indicates the run time from start to finish, the y-axis logs the individual DFF execution time for every iteration. We can observe that the DFF execution time is quite consistent with a small range of variation, which hints we have a solid start point for further architectural explorations.

5 Automated Formal Checking of 5G and next generation Base-station Modem SoC Functionality

In wireless infrastructure, modem requirements are regularly updated in software, and simulation is not sufficient to ensure fault tolerance for the wide variety of scenarios. As a result, leakage of Heisenbugs through integration testing and into field deployment is a real concern. As mentioned in earlier chapters, we outline an architecture that is designed to allow practical formal checking for Heisenbugs and performance guarantees, and demonstrate how formal checking of blocks can be automated at the dataflow specification level.

Figure 3.2 shows an highlevel overview of our Formal Toolchain methodology. In this chapter we describe that methodology in detail starting from how to automate the process from algorithm and requirements specification thru mapping to the SoC with formal checking of performance and correctness.

- We start by describing the algorithms as Directed Acyclic Graphs (DAGs) using a Parameterized and Interfaced Meta-Model (PiMM) Model of Computation (MoC) [11] using the PRESSM [37] tool. This tool allows us to manipulate the complicated dataflows into a series of loosely connected, generic DAGs, which we call Data Flow Fragments (DFFs), to run on the SoC, that are mapped at runtime to achieve the desired flow.

- We defined a template for the DFF representation of any application (including Wireless Baseband Applications) in PREESM, and developed Python scripts to translate those templates into UPPAAL’s Timed Automata (UTA) meta-model format. We call these generated UTA meta-models as untimed Behavioral Automata (BA) meta-model since they are not timed. Generated BA meta-model can then be automatically manipulated within the UPPAAL tool [4] to provide guarantees of performance, correctness and other desired properties. Section 5.3 describes the use of PREESM to generate BA models of DFFs that can be integrated with fixed hardware models in UPPAAL. Section 5.3.1 describe the generation of an untimed BA for one of the 5G Dataflow Graphs, called Channel Estimation DFF.

- We developed an UTA model of SoC architecture model based on an array of “DFF acceleration” IP, called a Service Resource Element (SRE) each receiving a stream of DFFs for processing. Section 5.4 present the target architecture and the Hardware Models that represent it in UTA metamodel. Inspired by [23] we reduce the complexity of the formal check by checking the operation of an SRE in isolation with models for DFF arrival patterns formally defined as TA. We found that the TA models must be carefully designed to prevent an explosion of the search space resulting in hours/days to finish the formal verification and we share our philosophy for efficient model design in section 5.5.1 as well as formal verification runtime results in section 5.8.
Section 5.7 outlines how to test the resulting TA for robustness and correctness and in section 5.8 we demonstrate the performance of the automated formal tooling.

5.1 Why formal methods based checking & verification approach?

Mapping of many DFF simultaneously onto 5G SoC must occur at runtime because, each symbol period, different DFFs are used to achieve the goals of the chosen users and rates. Static mapping strategies do not allow for such flexibility. Our tool permits runtime flexibility while maintaining high reliability by applying formal methods designed specifically for flexible FRT operation to verify that the recombination of DFFs for an assumed pattern of DFF arrival can achieve the desired QoS for a given SoC.

Using a single, DFF, or “generic DAG” with runtime, data buffer size and resource requirement ranges to represent DFFs that have a similar structure, we can keep the number of DFF to be analyzed formally to a manageable number.

Though there are numerous papers on scheduling multiple DAGs of different shape/size onto multi-core SoC [38] [48] [16], these papers address only one or two cases, usually worst case scenarios, and do not check for correctness and robustness (from effects such as Heisenbugs, Liveloop, buffer overflow and so on) at the architecture level. Correctness and robustness are usually checked via extensive simulation during integration testing but the complexity of 5G operations and the regularity of feature additions and modifications makes this an increasingly impractical methodology that often leads to Heisenbugs in the field.

Our goal is to demonstrate a path toward automating and formalizing the correctness and robustness checking as well as the mapping of the algorithms to the SoC such that a high degree of flexibility and continuous integration of new features is possible.

5.2 Overview of the UPPAAL Tool

Uppaal is a toolbox for verification of real-time systems jointly developed by Uppsala University and Aalborg University. It has been applied successfully in case studies ranging from communication protocols to multimedia applications. The tool is designed to verify systems that can be modelled as "networks of timed automata" extended with integer variables, structured data types, and channel synchronisation. These systems are called Uppaal Timed Automata (UTA) metamodel in Uppaal toolbox.

A timed automaton is a finite-state machine extended with clock variables. It uses a dense-time model where a clock variable evaluates to a real number. All the clocks progress synchronously. In Uppaal, a system is modelled as a network of several such timed automata in parallel. The model is further extended with bounded discrete variables that are part of the state. These variables are used as in programming languages: they are read, written, and are subject to common arithmetic operations. A state of the system is defined by the locations of all automata, the clock constraints, and the values of the discrete variables. Every automaton may fire an edge (sometimes misleadingly called a transition) separately or synchronise with another automaton, which leads to a new state.

The model-checker Uppaal is based on the theory of timed automata and its modelling language offers additional features such as bounded integer variables and urgency. The query language of Uppaal, used to specify properties to be checked, is a subset of CTL (computation tree logic).

Purpose of this chapter is to explain the novel techniques we developed to represent dataflow models and SoC architecture (with FRT) as Networks of Timed Automata in Uppaal toolbox and formally verified to provide guarantees of performance, correctness and other desired properties.

Disclaimer: This section does not explain the concept of Time Automata and the usage of Uppaal toolbox. Refer [5].

5.3 Overview of the auto-generation of behavioral TA models from LTE/5G algorithms

Translating LTE applications into Dataflow models using the PREESM tool is covered in [11]. Figure 5.1 shows an example of representing LTE’s PUSCH’s Bit Level processing (BLP) applications as Dataflow models. For details on algorithms mentioned in Figure 5.1 refer [29].

Similarly 5G physical layer algorithms can be translated into Dataflow models and appropriate DAGs can be generated. Therefore how to develop DFFs of LTE/5G physical layer algorithms is not covered and a simple DFF example is used to explain the TA auto-generation mechanism followed by an overview of auto-generated TA model for Channel Estimation dataflow shown in figure 2.3. Figure 5.2 shows a PREESM’s PiMM MoC representation of a DFF with two nodes, connected by an edge. Note that the PREESM tool was designed for analyzing PiMM MoCs [11] but we are using its graphical interface to draw DFF.

Figure 5.3 shows the auto-generated (via python script) untimed Behavioral Automata (BA) model of the example 2-node DFF shown in figure 5.2. We take the approach laid out in [46], separating the system into hardware TA (which
Figure 5.1: LTE’s Bit Level Processing representation as Dataflow models (PiMM MoC) in PREESM tool (inspired by source: [11])

Figure 5.2: A simple DFF example with two Nodes

are referenced in this paragraph and described in section 5.4 and untimed BA models, connected by well defined interfaces. This allows us to generate the behavior of the modem algorithm as DFF without having to touch the timed models of the hardware it is running on. All behavioral DFF models use a one to many Receive_DFF edge to handshake a DFF descriptor from the Director. The DFF model uses internal token passing to create a pattern of kernel descriptors in the correct order for the DAG and finally the DFF model handshakes a return DFF descriptor using a many to one Terminate_DFF edge. This allows many DFF to be connected to a single Director with the correct DFF being chosen based on the guard pattern of the edge.

All other edges in the DFF behavioral model either fire or end the running of a kernel inside the DFF. In the example this adds four edges for two nodes. The fire edges create a kernel descriptor and handshake it into the Scheduler. The end edges handshake a kernel descriptor back from the Pool manager. Any DFF developed in PREESM is automatically converted into the BA format and is included in the list of DFF in the UPPAAL model. As hook up is directly to the Director and Pool manager interfaces it is also be easily automated.

5.3.1 5G Channel Estimation auto-generated untimed Behavioral Automata

Figure 5.4 shows the auto-generated untimed BA of the Channel Estimation DAG dataflow shown in figure 2.3 in the form of PREESM’s PiMM MoC representation with six nodes (aka actors). The auto-generated Channel Estimation BA preserves the unique name of each actor from the PREESM model, for example, CHEST1_L1metaDataExtractor actor name in figure 2.3 is preserved as CHEST1 in generated BA in figure 5.4.

5.4 Breakdown of the SRE Architectural Model and Timing

The architectural model used in this paper is based on an array of SRE each receiving a stream of DFFs for processing. The top level SRE architecture is shown in Figure 3.3. For this paper we focus on automated analysis of the ability of an SRE to support streams of DFFs from multiple sources. Each source sends a control packet to the Director, to be described, and the pattern of arrival of the DFFs is modeled by a TA that represents a jittered periodic arrival in the same way that [23] used a real time calculus source to model the input stream to the IP under analysis. We can use
any arrival model that can be represented as a TA, though some will lead to state space explosions and therefore careful thought as to the correct model is needed. Note that the model of arrival can be a superset of the actual arrival pattern as the formal checker will check all possible patterns within the model. This allows for TA models to be used even if the actual arrival cannot be modeled as a TA. However a very generic arrival model will cause an increase in the state of the system so more accurate is generally better.

As DFFs are large elements of compute, consisting of several dependent kernels and running for tens of thousands of clock cycles (cc), modeling only their arrival pattern limits the complexity of the IO model for the SRE and allows the formal checker to evaluate complex and highly parallel flows on the SRE. A DFF is processed in the Director using a received control packet, setting up the control structures to run the DFF. The SRE does not trigger the DFF until all the required data packets arrive. Currently we only model the arrival of the complete, ready to run, DFF, but we will extend this to comprehend the arrival of control and data packets separately in the future. The DFF is broken down into kernels by the control structure which may be spread across multiple stages of the SRE, each of which has multiple pools of resources (for this paper we model memory and compute pools) which are assigned when the kernel is triggered to run. The stages control the triggering of kernels in the correct order and this is modeled by the DFF BA described in section 5.3.

The hardware model described in this report models the Director and a single stage of the SRE. Its goal is to formally check the policy of the Director and the scheduling strategy of the Stage when presented with time jittered, quasi periodic DFFs of multiple types arriving at the SRE. It consists of the following elements:

- The Director which receives a trigger when a DFF is ready to run, along with details on the type of DFF. The Director runs a policy to determine if the DFF should be run and also how it should be staged. The Director can maintain several different staging strategies (modelled by different DFF BA) and can also reject the DFF entirely, reporting it as a dropped DFF to the higher layers. As the policy is still under development the Director currently runs the DFF in a FCFS manner.

- A Stage Scheduler that receives kernels when they are ready to run and time schedules their initiation in the Stage. This scheduler can prioritize more urgent DFFs for instance. Currently the Stage also runs a FCFS schedule.

- a pool manager that receives a scheduled kernel and implements its resource use on a stage, reporting completion to the DFF behavioral model. Currently each pool is a “pure” pool with equal and homogeneous access to all resource in the pool. More complicated pool structures are easily modeled.

5.5 A brief Review of the Formal Models

Without going into the details of how these formal models work we point out the main features of the models that together make up the SRE formal model. Some knowledge of the input formal for UPPAAL would be helpful when reading this section, though not necessary.
5.5.1 Model design philosophy

This is a model of a processing system and as such events commence as soon as the conditions are satisfied. Therefore urgent channels are extensively used to align edges in TA. In a TA there is generally no requirement that an edge is taken once it is valid unless it is explicitly required to do so. Urgent channels cannot remain valid if time increments and must either become invalid immediately (due to an action as the result of the choice of another path) or must be taken. This models how a real-time system works in practice and we therefore use urgent channels as much as possible. We also use multiple "its urgent" automata that are a single loop connected to a single state with an urgent channel to force edges to complete without any more time being consumed. This allows us to accurately model a program flow which proceeds without timing uncertainty once it is triggered. It also reduces the state space size of the model by removing behavior that simply doesn’t reflect the real system. Another modeling technique we use extensively is the committed node. This node type must be left on the next transition, before anything else happens. It allows us to force sequences of events to happen in an atomic manner.

Data passing between processing elements is generally passed using a handshake where an urgent channel represents a semaphore. The transmitting model places the data in a global variable once the edges are synchronized (so the semaphore is locked) and the receiving model picks up the data on the next edge using a committed node and its urgent channel to ensure this happens immediately. If multiple writers are trying to lock the semaphore then the checker will try all orderings of locking. We use queues to enforce ordering of handshakes whenever possible as this reduces the number of choices for the checker leading to significant speed up of the formal checking. Generally we use urgent channels and committed nodes as often as possible to minimize the number of path choices available to the checker while maintaining correct behavior. Non determinism in the model is created due to uncertainty in runtime of functions, which happens because parameters in the data and input buffer sizes can change processing runtime in a real system, and because of uncertainty in the arrival time of the DFF due to uncertainty in runtime in the rest of the SoC.

We track DFF through the system by assigning a unique instance number to each DFF as it arrives. This number is picked deterministically as the lowest currently available instance number to minimize the number of paths that need to be traversed by the checker. We set a maximum number of DFF that can be active in the system so there is a DFF_MAX_PAR constant that defines the maximum index number. In a DFF behavior each kernel is given a unique,
hardwired number and for any system we calculate and set a constant MAX_NUMBER_KERNELS that is the maximum number of kernels in any DFF. We then use 2D arrays of size DFF_MAX_PAR by MAX_NUMBER_KERNELS to keep track of booleans and clocks and descriptors associated with each kernel. This use of large, sparsely used and redundant arrays is also used successfully in [21] [13] and reduces the formal checking time by providing a deterministic location for each kernel.

5.5.2 The Director Model

The Director Model is shown in Figure 5.5. It consists of three main loops. The loop on the left receives a DFF event and adds time to a variable that monitors how much time the Director has left to complete the processing of all outstanding DFFs. The Director will not trigger the functional behavior of a DFF until it has completed all outstanding processing of incoming DFFs. The Director Processing Model shown in Figure 5.6 is used to model this processing time. The Director pushes the DFF request onto a queue and this is done by a function that can choose to reorder DFFs if there is a backlog, to prioritize certain DFF over others. More generally the Director can run a policy to accept or reject DFFs if there are too many arriving to meet its policy. This allows a distributed management of the modem functionality that reduces the control overhead of the modem. The Director never back pressures the DFF source and this simplifies the formal checking process as well orthogonalizing the formal checking of one SRE from its neighbors. If the SRE receives more DFF than it can handle the DFF queue will overflow and there is a formal check for this error.

The lower loop in Figure 5.5 pushes the chosen DFF into the appropriate DFF BA that then breaks it down into individual kernels in the correct order and these kernels are passed on to the scheduler model. The right loop in the Director model is used to receive completed DFF events from the Pool Manager and removes them from the model. Note that each DFF is assigned a unique instance number by the director and that a timer is started for this instance number to track the lifetime of this DFF. This timer is switched off when the completed loop cancels the DFF. As pointed out in [13] this translates the schedulability analysis problem into a reachability problem for TA. The Director model has a terminal state that can be reached if any of the DFF violates its’ timeout. This terminal state is tested for reachability to test the correct real time functionality of the system. The Director only allows a certain number of DFF in flight at the same time and the model also has a terminal state that is reached if a DFF arrives when the maximum number of DFF are still in flight.

5.5.3 The Scheduler Model

The Scheduler Model is shown in Figure 5.7. The scheduler model simply receives kernels descriptors and pushes them onto a queue. It also pops kernels off the queue and pushes them at the pool manager as the next kernel to allocate. The function that pops the kernels can be used to implement a scheduling policy based on deadline information in the kernel descriptor. The scheduler model has a terminal state that is reached if the queue overflows.
Figure 5.6: Director Processor Model

Figure 5.7: Scheduler Model
5.5.4 The Pool Manager Model

The Pool Manager Model is shown in Figure 5.8. It has two main loops to allocate and free resources. The allocation loop, the three nested loops on the right, reacts to a kernel arrival event and tries to allocate the resources in a pool. If it fails to find the resources it needs it will wait for another kernel to complete to free up some resources and try again. Until it has allocated this kernel no other kernel arrival event can occur. Once a kernel is allocated, and the remaining resource count adjusted, the kernel is assigned a unique timer with a minimum and maximum runtime that is taken from the kernel descriptor. The free resources loop on the left is triggered by a complex invariant on the central node in the graph which kicks the model out of the central node if at least one kernel timer reaches its maximum runtime. The loop also becomes enabled once any kernel has reached its minimum runtime. This pattern means that any active kernel must leave the central node and complete sometime between its minimum and maximum runtimes. If the loop is traversed the kernel in question is deleted from the model and a completion event is activated that allows the DFF BA to progress to the next kernel.

![Figure 5.8: Pool Manager Model](image)

5.6 The Complete SRE Formal Model

The formal model used in this report is made up of a single director (there can only be one director in the current model) and a single stage (there could be multiple stages hooked up) that consists of a scheduler and pool manager. Any number of DFF models can be added to the Director. Finally, for each DFF model there is an arrival pattern generator. When the formal model runs the checker tries all combinations of arrival patterns possible from all the DFF for all possible runtime variations of all compute elements. An example of this hook up from the main UPPAAL window is shown in Figure 5.9. In this example there are three sources of DFF, a Director (with its urgent channel TA and its processor TA), three DFF behavioral models, one for each source (each the same model in this case but they can be different), the stage scheduler (with its urgent channel TA) and the pool manager (with its urgent channel TA). At the bottom of the screenshot you see the system deployment of these individual TA into a single connected model. When we run the model we use queries to check that the model behaves correctly under all conditions.

5.7 Classes of Queries for Formal Checking

Any formal checker is only as good as the queries developed to extract information from the design. This model is focused on finding Heisenbugs that are difficult to identify using simulation and are likely to survive through unit test and even...
integration test into the product. For our system level checking there are three classes of queries we need to consider:

- Functional correctness. These queries ensure that the hardware accesses resources in a certain order at all times or that correct timing is maintained for operations. Such queries are developed when checking basic hardware modules, the most obvious being a check for Deadlock or Livelock in the system. An example of this is in the Pool manager where we formally check that a kernel that is currently active is not activated again.

- Runtime Errors. These queries check for buffer overflow, parameter initialization errors and system overload. They are a side effect of “operator error” in setting up and running the system. Usually they are hard to find with static checks. Runtime should not cause system error but the generation of error message feedback. Runtime errors in our system occur when we overflow queues. We cannot back pressure queues as it breaks our system analysis model.

- Performance checks. These queries check that performance timing is met for the real time system so that deadlines are not missed in the SoC.

For the examples in this report we perform the following checks. The true system list is considerably larger:

- Run time check for each DFF (Performance check)
- Deadlock (Functional correctness)
- Director queue overflow (Runtime Error)
- Scheduler queue overflow (Runtime Error)
- Pool Manager Node Assignment (Functional Correctness)
- Livelock of node assignment (Functional Correctness)
- DFF activity level (Performance check)

5.8 Results

For the model checking we used uppaal64-4.1.24 running on an Intel(R) Xeon(R) CPU E5-2695 v3 @ 2.30GHz, supported by Ubuntu 18.04.4 LTS and 94G of usable memory. As UPPAAL cannot fork multiple queries in parallel, the timing we quote is for the complete query list running serially. Based on the query classification in Section 5.7 we developed a basic query list shown in Figure 5.10. The Performance checker tested to make sure each DFF achieved its runtime...
and monitored the number of DFF that could be in flight at any moment. The Runtime error checking monitored the maximum queue size for the director to make sure the DFF did not back up into the system. The Functional Correctness tested that a node was not assigned while still in process, a kernel once activated will eventually complete, and that there is no deadlock across the whole model. Obviously many more checks would be included for a full analysis of the model, but these form a representative set of the kind of checks we would like to perform.

Refering to Figure 3.3, the hardware is modeled so that the Director takes 100cc to process a DFF into the stage manager. This processing includes running the behavioral model of the DFF and setting up the kernels to be run in the stage manager. The stage manager consists of a scheduler to order the kernels and a pool manager to allocate the resources in the pool as described in Section 5.5. The scheduler takes 123cc to schedule each kernel into the pool manager. The input DFFs arrive as several sources from other parts of the SoC as a control packet followed by some data packets. We currently model the arrival of the control packet at the director and assume that the data can arrive before the DFF is triggered in the pool manager. In future work we will add a packet processor model. The arrival of the control packet at the Director is modeled by a quasi periodic source that has a specific average period about which it is jittered up to a maximum number of clock cycles. We model a single pool manager in this paper.

- **Simple Tests:** We ran some initial burn tests to make sure the model functioned correctly and that no state space explosion was slowing down the checker. We set the time out for all DFFs to be a healthy 100000 cc. We set up three DFF sources with period of 5000cc and no jitter and spaced the arrival of the DFF by 1000cc so that they did not overlap. The DFF flow was the same for each source and consisted of two kernels in a chain, each taking exactly 200cc per kernel. The checking was near instantaneous due to the lack of resource contention and any runtime variation in timing. Adding a runtime range to the kernels of [200,300] did not change the checking time as it does not add to the number of states in the TA of this very mildly loaded system.

- **Overlapping DFF of different types:** Changing this model so that the sources were offset by 200cc allows the sources to bunch up and overlap periodically. This produces a more complex resource usage pattern increasing the total checking time to about one minute. The maximum number of DFF in flight changed from 1 (as shown in lines 4 and 5 of the query list in Figure 5.10 to 3, as would be expected as each of the three DFF run their kernels one at a time. Different types of DFF were then tested with 2 or 3 kernels in different configurations and we found that with runtime variation of 50% and three kernels, the checking time might increase to closer to 1 hour. The worst case backlog of the Director queue remained small for all of these DFF combinations showing that the checking time was due to the combinatorial number of ways that a larger number of overlapping kernels with significant runtime jitter can combine.

- **DFF Arrival Jitter** Adding jitter of 10% of the DFF start time separation (so 20cc of jitter to a 200cc arrival gap
between DFF types) to the overall arrival time of the DFF didn’t not change the checking time, adding jitter of 25% of the separation took the checking time to about 30 minutes, and increasing this jitter to 50% did not allow even a single query to complete in 24 hours. Clearly the uncertainty in arrival time of the DFF is adding a lot of new potential orderings of operations within the hardware and this is having a dramatic impact on the search space. Note that most time is spent in the Livetock and deadlock testing.

- **Running close to runtime requirements** We simplified the model back to 3 sources of 2 kernel DFFs at 200cc spacing with 10% jitter in arrival time and a runtime range for the kernels of [200, 300]. This example checks in about 3 minutes with most of the checking time in deadlock and livelock. Counting the time consumed in the path of a single DFF, the time to complete a DFF is best case in the range [623, 823]. Focusing on the timeout check only we see that the system actually fails at 1750 and the trace of this timeout involves 3 DFFs and 6 kernels which, due to runtime range, complete in a different order to the one in which they were submitted, but also partially in parallel with each other so that it is hard to break down the 176 state change steps in the formal checker that led to this state into a series of time updates. The timeout check takes longer as we change the timeout value to be close to the edge of failing, but it remains less than 15 seconds.

- **Using all the Pool resources** We kept the same simulation as in the previous step but increased the timeout check to 1800cc. We then reduced the number of compute and memory resources in the pool. In our simulation we require 1 compute element and 3 internal memory resources from the pool for each kernel in this example. If we allocate 4 compute resources and 13 memory resources to the pool we successfully achieve our timeout goal. But a reduction to 12 memory elements causes a timeout failure which requires an increase in timeout to 1807 to fix. The formal checking again shows the subtlety of the failure in resource allocation. It might be expected that a lack of resources would stall a DFF by a time somewhere close to the runtime of a kernels (so 100s of cc). But in this case the stall was less than 10cc. These subtle corner cases are practically impossible to analyze by hand.

5.9 Conclusions and Future Work

5.9.1 What have we demonstrated so far?

The above results show that we can develop a formal model of a large processing engine, the SRE, and check its behavior for critical heisenbug generating properties with reasonable compute time. This is true because the SRE is being developed in a hierarchical structure where lower level functional blocks, such as the Director and the SHOC have specific interfaces that can be modeled formally. The SRE processes in a RESTful manner and this keeps the total state space down to a minimum. Essentially, the SRE has been designed with one of its goals to be formally checked at the system level. This is critical in the 5G wireless space (and even more so in future 5.5 to 6G modems) which is a Firm Real Time problem requiring high availability of real time flows.

5.9.2 How do we improve the formal tooling?

There remains plenty of room to scale this result to more complicated cases as most checking times were relatively small. But there is also much research to be completed in order to develop a formal checking strategy that can deal with state space explosions caused by the setting of parameters in a way that the complexity of operation of the SRE expands dramatically. In such cases the UPPAAL tool will just sit and process for a long time and may run out of memory. Rather we need new techniques that recognize state space explosion and either report it back to the operator or fall back to a simpler, if more pessimistic, model of formal checking. Improvement to the SRE architecture may also allow us to control the state space under most parameter settings.

The speed of the formal check can be improved using better compute platforms. Queries can be run in parallel with either multiple UPPAAL licenses or by using the multi-core OPAAL+LTSMIN tool [10].

5.9.3 A next generation of formal checking for SRE

Eventually a TA checker can be written specifically for this class of architecture speeding up checking enormously because there are invariants in the architecture that are hard to communicate to the general UPPAAL checker. By using flows of DFFs without back pressure we can orthogonalize the checking, vastly simplifying the formal checking of the SoC.

The formal check of the runtime of a complete dataflow, spanning multiple SRE is not addressed in this report. We use the same technique as in [23] to check that the output DFF flow of an SRE matches its intended quasi periodic pattern and this allows us to check formal properties at the SoC level and SRE level separately.

In the model presented in this paper we model time consumed by the Director and the Scheduler and assume it is constant, though this could be easily changed to be a range of timing. As in the PRET processing philosophy [32]
it is important that bounds on the runtime of each component can be enforced, in our case to formally guarantee the correct operation of the SRE (for instance that it is deadlock free) as well as to ascertain that it meets its performance requirements for a given mixture of DFF arrivals.

Some further study is required on this system level formal checking and this may also impact the architecture. We have seen that the formal check can cope with complicated overlapping patterns of DFF processing in an SRE, even with significant runtime uncertainty in the kernels, which is a natural effect in parameterized processing of blocks of data that may vary in size. But if there is significant jitter in the arrival time of the DFFs at the SRE there is an explosion in the number of possible state sequences that have to be checked. This implies we may want to control the arrival jitter by delaying and buffering the DFF before releasing them into the SRE. Such a strategy would add to the total latency of a flow but would allow for higher utilization of the SRE and therefore better overall performance and is for further study.

6 Conclusions and Next Steps

In the course of this research we have developed a new, dataflow based architecture for efficient implementation of the diverse use cases that mix together in 5G modems while setting the foundation for future generations of wireless modems. The architecture was based on a hierarchical decomposition of the large dataflow problem into

1. a top level SoC view where DFF flow through a network of SREs, the DFFs being processed and triggering each other. The network maintains a leaky bucket type of flow control managing the rate at which DFF arrive at each SRE
2. SRE Director/Packet Processor control and policy management of nodes from the DFF onto Stages
3. Stage level scheduling and management of multiple nodes in flight
4. SHOC level computation of nodes

6.1 SRE architecture progress and next steps

We focus on the design of the SRE and describe the packet protocol that allows all levels of the hierarchy within the SRE to communicate with each other in a logical manner. There is no sense of a global memory map, or a global scheduling and real time management strategy. For the SRE architecture we present a detailed breakdown of the packet protocol as well as the operation of the Director, Packet Processor and Stages. All of this is simulated at an event driven level in VisualSim.

In the coming months we plan to continue to test the SRE at the event driven level using more complicated and realistic DFF mixtures as well as experiment with new policies to maximize the capacity of the SRE. We will also examine the complexity of the SRE in critical sections of the architecture.

6.2 Toolchain progress and next steps

We have developed a prototype formal checking tool for the SRE that we hope can be a model and an inspiration for others to do the same. Because of the hierarchical architecture, the SRE can be formally checked separately from the rest of the SoC provided the flow patterns are agreed upon.

However there is more work to be done to make the formal tool robust to a wide range of DFF flow parameters. We also have to align the model with the latest version of the SRE detailed specification. There are some features that are not presently modeled and these need to be added. We expect that we will eventually move to an in house formal checking program and away from UPPAAL, as the design get more specific and to allow increased robustness and speed. In particular we need a methodology for coping with operator error, for instance an incorrect or infeasible set of patterns being input. Though most checking times were relatively small, some scenarios exhibited state space explosion and failed to complete formal checking. Understanding and managing this problem for the SRE is clearly an important medium term goal.

More effort needs to be put on developing a comprehensive set of queries to maximize the value of the formal checking and minimize any Heisenbugs.

We did not go into detail in this report on our efforts to use Spectral graph theory and SAT and ILP to provide options on how to map map DFF nodes to stages and also map DFF to SREs but we will report on this in the next technical report. Our strategy is to provide several different ways of mapping a DFF on an SRE (which we call "tetris blocks") and then use a policy running on the Director to choose the best one of these tetris blocks, with appropriate
time offset, given the current loading of the SRE. The Policy can be formally checked in the toolchain but development of the policy is a subject for further study.

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A Mirabilis Model Details

The top level SRE Mirabilis model is shown in Fig. 4.13. The below describes the details of each important component.

![Diagram](image)

**Figure A.1: Mirabilis Model of the Director and Packet Processing Subsystem**

Fig. A.1 shows the model of the director and packet processing subsystem, it interprets the control and data packets from the NoC interface, generates and dispatches the microflow descriptors to different stages. Microflow descriptors not only describe a complete data flow graph, but also data dependencies among multiple segments of a data flow. This way, the token table and actor list can be built properly to run a data flow seamlessly once this process is completed.

Each stage has its own actor list and token that are built upon the microflow descriptors received from the director and packet processing subsystem as shown in Fig. A.2. They are modeled as databases in Mirabilis VirtualSim to hold multiple entries of microflow/kernels as shown in Fig. A.4 and Fig. A.3.

Please note that, the director and packet processing also generates and dispatches pointer descriptor to describe those segments that have ingress and egress interfaces of an SRE. They are modeled as separate databases for the easy bring-up purpose now, however the necessary pointers information can be comprehended as mem-ptr subfield in the token table as shown in Fig. A.4 later on. The Token-Entry that exists in the actor list in Fig. A.3 and token table Fig. A.4 is the link that connects the both tables as described as the Entry-depen-loc in Fig. 4.8.

The current model supports maximum three dynamic stages. The director can assign up to three stages depends on the overall loading and other QoS requirement to conduct architectural exploration and analysis. As shown in Fig. A.5, each stage has separate submodule for the scheduler and the pool manager to comply the architectural considerations described in Fig. 4.6. The data dependency resolver automatically selects and searches its own set of token table and actor list whenever a relevant microflow/flow in the same stage or from other stage is completed. The evaluation result is passed to the scheduler and the pool manager for further actions by following the flow chart illustrated in Fig. 4.7.

The Mirabilis TileLink module is instantiated to model the dataflow mapped distributed buffer network as shown in Fig. A.6 for further architectural trade-off and data-traffic analysis.

As mentioned previously, any conventional DMA can be leveraged for the quick SRE architectural exploration, the Mirabilis DMA engine with simple configuration of four channels shown in Fig. A.7 is instantiated to complete the SRE.
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Figure A.2: Model of Token Tables and Actor Lists for All Stages

Figure A.3: Mirabilis Model of the Actor List

Figure A.4: Mirabilis Model of the Token Table

architectural model.
Figure A.5: Mirabilis Model of the Dynamic Stage Subsystem

Figure A.6: Mirabilis Model of the Dataflow Mapped Distributed Buffer Network
Figure A.7: Mirabilis Model of the DMA Subsystem
B  Message Formats and Error Codes

B.1  Message Formats

The following section describes internal and external message formats used by the SRE.

**Control Packet**

**Message Type:** External  
**Source:** SRE  
**Dest:** SRE  
**Description:**  
The DFF control packet requests resources for processing a DFF instance.  
The `sre_id` field identifies destination of the packet (for routing purposes).  
The `pctype` field contains information about the packet type.  
The `global_tag` indicates the particular instance of the DFF.  
The `diff_type` specifies a DFF container type (predefined DFF type) in which the actual DFF to be processed must fit.

```
sre_id  pctype  global_tag  diff_type
8       8       16         16
```

**Data Packet**

**Message Type:** External  
**Source:** SRE  
**Dest:** SRE  
**Description:**  
The DFF data packets contain actual data tokens to be processed.  
The `sre_id` field identifies destination SRE of the packet (for routing purposes).  
The `pctype` field contains information about the packet type.  
The `global_tag` indicates the particular instance of the DFF.  
The `error_code` field contains an error code (0 means no errors)  
The `size` field indicates the size of the data packet payload.  
The `payload` field contains DFF operand inputs.

```
sre_id  pctype  global_tag  error_code  size  payload
8       8       16         16         16          8 x size
```

```
num_token  op_config[0]  op_data[0]  ...  op_config[num_token-1]  op_data[num_token-1]
8
```

```
port  seq_id  token_size
8     8     16
```
**Error Packet**

Message Type: External  
Source: SRE (Packet Processor)  
Dest: Data Warehouse, SRE  
Description:  
Error packets are used to report errors to higher layers  
- The `src_id` indicates the destination SRE of the packet.  
- The `ptype` indicates the packet type  
- The `global_tag` indicates the DFF instance.  
- The `time` field contains a timestamp of when the error was detected.  
- The `error_code` indicates the type of error.

| src_id | ptype | global_tag | time | error_code |
|--------|-------|------------|------|------------|
| 8      | 8     | 16         | 64   | 16         |

**DCT Request**

Message Type: Internal  
Source: Packet Processor  
Dest: Director  
Description:  
The DCT request is the internal version of the control packet.  
- The `mtype` field indicates the message type.  
- The `global_tag` indicates the particular instance of the DFF.  
- The `dff_type` specifies a *DFF container type* (predefined DFF type) in which the actual DFF to be processed must fit.

| mtype | global_tag | dff_type |
|-------|------------|----------|
| 8     | 16         | 16       |
**DFF Descriptor**

**Message Type:** Internal  
**Source:** Director  
**Dest:** Packet Processor, Stage Manager(s)  
**Description:**  
The DFF Descriptor describes the top-level structure of the DFF  
- The `mtype` field indicates the message type  
- The `global_tag` indicates the particular instance of the DFF.  
- The `size` field refers to the payload size.  

The DFF Descriptor `payload` contains the following fields:  
- The `num_inputs` field indicates the number of inputs  
- The `inputs` field indicates the token size and number of tokens for each input  
- The `num_outputs` field indicates the number of outputs  
- The `outputs` field indicates the token size and number of tokens for each output  

| mtype | global_tag | size | payload |
|-------|------------|------|---------|
| 8     | 16         | 15   | 8 x size |

| num_inputs | inputs[0] | inputs[1] | ... | num_outputs | outputs[0] | outputs[1] | ... |
|------------|-----------|-----------|-----|-------------|------------|------------|-----|
| 8          |           |           |     |             |            |            |     |
| token_size | num_token |           |     |             |            |            |     |
| 16         | 8         |           |     |             |            |            |     |

**DFF Release**

**Message Type:** Internal  
**Source:** Director, Packet Processor  
**Dest:** Director, Packet Processor, Stage Manager(s)  
**Description:**  
The DFF Release indicates the DFF Descriptor has been invalidated  
- The `mtype` field indicates the message type  
- The `global_tag` indicates the particular instance of the DFF.  

| mtype | global_tag |
|-------|------------|
| 8     | 16         |
**Pointer Descriptor**

**Message Type:** Internal  
**Source:** Packet Processor  
**Dest:** Stage Manager(s)  
**Description:**  
The Pointer Descriptor sends the pointers for each DFF input and output  
- The `mtype` field indicates the message type  
- The `global_tag` indicates the particular instance of the DFF  
- The `size` field refers to the payload size.

| mtype | global_tag | size | payload |
|-------|------------|------|---------|
| 8     | 16         | 16   | 8 x size|

The DFF Pointer Descriptor payload contains the following fields:  
- The `num_iptrs` field indicates the number of input pointers  
- The `iptrs` field indicates the 32-bit pointer for each input  
- The `num_optrs` field indicates the number of output pointers  
- The `optrs` field indicates the 32-bit pointer for each output

**Microflow Descriptor**

**Message Type:** Internal  
**Source:** Director  
**Dest:** Token Table / Stage (Distributed Implementation)  
**Description:**  
The Microflow Descriptor contains information on how to execute a microflow  
- The `mtype` field indicates the message type  
- The `global_tag` indicates the particular instance of the DFF  
- The `size` field refers to the payload size.

The Microflow Descriptor payload contains the following fields:  
- The `stage` indicates which stage the microflow executes on  
- The `local_tag` is the unique ID of the microflow within the DFF  
- The `kernel_id` indicates the kernel to execute  
- The `num_inputs` field indicates the number of inputs  
- The `inputs` field indicates the \{`src_tag`, `src_port`, `src_seq`, `src_size`\} for each input  
- The `num_outputs` field indicates the number of outputs  
- The `outputs` field indicates the \{`dest_stage`, `port`, `seq`, `size`\} for each output

| mtype | global_tag | size | payload |
|-------|------------|------|---------|
| 8     | 16         | 16   | 8 x size|

| stage | local_tag | kernel_id | num_inputs | inputs[0] | inputs[1] | ... | num_outputs | outputs[0] | outputs[1] | ... |
|-------|-----------|-----------|------------|-----------|-----------|-----|------------|-----------|-----------|-----|
| 8     | 8         | 8         | 8          | 8         | 8         |     | 8          | 8         | 8         | 16 |
### DFF Input Ready

**Message Type:** Internal  
**Source:** Packet Processor  
**Dest:** Token Table / Stage (Distributed Implementation)  
**Description:**  
The DFF Input Ready message indicates that all DFF inputs have arrived  
- The `mtype` field indicates the message type  
- The `global_tag` indicates the particular instance of the DFF  
- The `time` field indicates the time at which the DFF became ready.

| mtype | global_tag | time |
|-------|------------|------|
| 8     | 16         | 64   |

### DFF Output Ready

**Message Type:** Internal  
**Source:** Stage  
**Dest:** Packet Processor  
**Description:**  
The DFF output ready indicates when a DFF output token is generated  
- The `mtype` field indicates the message type  
- The `global_tag` indicates the particular instance of the DFF  
- The `port` field refers to the DFF output port

| mtype | global_tag | port |
|-------|------------|------|
| 8     | 16         | 8    |

### Error Message

**Message Type:** Internal  
**Source:** Any  
**Dest:** Packet Processor  
**Description:**  
Error messages are used to report errors to the packet processor  
- The `mtype` indicates the message type  
- The `global_tag` indicates the DFF instance.  
- The `time` field indicates the time at which the error was detected  
- The `error_code` indicates the type of error.

| mtype | global_tag | time | error_code |
|-------|------------|------|------------|
| 8     | 16         | 64   | 16         |

### B.2 Error Codes

This section describes a list of basic error codes. All consumers inherit the error code of their producer in order to facilitate debug. A time stamp is also appended to the error message (see Error Message format in subsection B.1).

| Error Code | Source               | Description                  | Category  |
|------------|----------------------|------------------------------|-----------|
| 0          | ---                  | No Error                     | ---       |
| 1          | Director             | DCT not found                | Fatal     |
| 2          | Packet Processor     | DFF descriptor not ready     | Fatal     |
| 3          | Stage                | Microflow not found          | Error     |
| 4          | Stage                | Microflow timed out          | Error     |