Mitigation of Motor Overvoltage in SiC-Based Drives Using Soft-Switching Voltage Slew-Rate \( (dv/dt) \) Profiling

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Abstract—In silicon carbide (SiC) device based motor drives, the high-voltage slew-rate \( (dv/dt) \) associated with the fast-switching transitions results in excessive motor overvoltage, due to the reflected wave phenomenon, which increases the motor winding insulation stress and causes premature failure while raising electromagnetic interference (EMI) problems. This article proposes a soft-switching voltage slew-rate profiling approach to mitigate the motor overvoltage in SiC-based cable-fed drives. The proposed approach optimizes the rise/fall time of the output voltage according to the cable length, without altering the switching speed of the SiC devices. Since increasing the switching rise/fall time using conventional approaches, such as increasing the gate resistance, results in an increased switching power loss, the proposed profiling approach is implemented using a soft-switching inverter. The optimum rise/fall time that can significantly mitigate the overvoltage is derived using frequency- and time-domain analysis. The auxiliary resonant commutated pole inverter (ARCPI) is adopted as an example of the soft-switching inverter to experimentally verify the proposed slew-rate profiling approach for the overvoltage mitigation. The analysis and experimental results show that the motor overvoltage is fully mitigated when the output voltage rise/fall time is set as the cable antiresonance period, i.e., four times of the wave transmission time along the cable. Furthermore, the slew-rate profiling approach along with the ARCPI reduces the switching loss and improves the EMI performance at the high-frequency region, compared with the conventional hard-switching converter. Specifically, the maximum efficiency of the ARCPI is about 99%.

Index Terms—Auxiliary resonant commutated pole inverter (ARCPI), \( dv/dt \) profiling, inverter-fed motors, motor overvoltage, reflected wave phenomenon, silicon carbide (SiC) MOSFET, soft-switching inverter.

I. INTRODUCTION

Driven by technological advancements in the wide bandgap (WBG) power semiconductor devices, such as silicon carbide (SiC) MOSFETs, power electronics is undergoing transformative enhancements in existing and emerging applications due to the superior characteristics of WBG material [1]. Compared with silicon (Si) insulated gate bipolar transistors, SiC MOSFETs can operate at faster switching speeds, higher operating temperatures, and higher voltage levels [2]. Among these advantages, the fast-switching speed plays a crucial role in reducing the switching loss and increasing the switching frequency [3]. As a result, using SiC MOSFETs in adjustable-speed drives can significantly improve the system efficiency, control accuracy, and dynamic response while reducing the torque ripple, when compared with Si-based counterparts [4].

While the adoption of SiC MOSFETs in motor drive applications brings exciting opportunities, the fast-switching speed results in several technical issues and design challenges for both the inverter and motor [1]. One specific serious challenge is the overvoltage oscillations across the motor terminals in cable-fed drives as a consequence of the reflected wave phenomenon across power cables [5]. This is due to the impedance mismatch between the cable and motor, which causes back and forth voltage reflections between them, resulting in motor overvoltage oscillations [6].

The overvoltage magnitude depends on the cable length and the rise/fall time of the inverter output voltage [7], as illustrated in Fig. 1. With shorter switching rise time of SiC MOSFETs, which can be as little as tens of nanoseconds, the motor overvoltage is more common and severe in SiC-based drives when compared with the Si-based counterparts, where the motor voltage can be twice the inverter voltage with few meter cables, as evidenced in Fig. 1. Furthermore, a greater than twice or even four times the inverter voltage can be observed at the motor side when the switching frequency and/or the modulation index are sufficiently high, i.e., the switching instances of the inverter voltage are very closely spaced [8]. This is denoted as the double pulsing effect, where a second voltage pulse is applied to the motor terminals before the first reflected pulse is fully decayed [9]. The resultant motor overvoltage increases the possibility of winding insulation partial discharge, leading to an accelerated aging and ultimate failure of the motor [10].

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Several approaches have been adopted to mitigate the motor overvoltage in SiC-based drives [10]. The mainstream mitigation approach is employing filters to tackle the root causes of the voltage reflection, i.e., the high $dv/dt$ and the impedance mismatch. The filters can be generally categorized into $dv/dt$ filters [11]–[16] and impedance matching filters [17]–[19]. The $dv/dt$ filters suppress the overvoltage by limiting the voltage slew-rate applied to the system [11]. Several passive and active $dv/dt$ filter approaches have been proposed in the literature. For example, [12] uses an active gate driver to control the $dv/dt$ of switching transitions but at the expense of increasing the switching loss. The passive $dv/dt$ filter approach uses different combinations of passive components ($R$, $L$, and $C$) to limit the inverter output $dv/dt$. The commonly used passive $dv/dt$ filters include the $L$ filter [13], $RLC$ filter [14], $LR$ filter [15], and $L/RC$ filter [16]. Although the $L$ filter is the simplest passive filter approach, it is not applicable to motor drives because the motor overvoltage suppression is directly proportional to the inductance size, and a high inductance will increase the drive cost and weight and deteriorate the drive system’s power factor [8]. The $RLC$ filter is commonly used to mitigate the motor overvoltage by alleviating the output $dv/dt$, but it reduces the system efficiency due to the power loss in the inductor and damping resistor [11]. However, the impedance matching filters reduce the overvoltage by including an $RC/RLC$ network at the motor side to alleviate the impedance mismatch between the cable and motor [18], [19]. However, the high $dv/dt$ imposed by the SiC switching devices may interact with the filter parasitic causing high-frequency impedance mismatch, which triggers higher peak motor voltage [17]. In addition, the filters have disadvantages in which they are bulky and increase the system power loss and cost.

A filter-less mitigation approach, denoted as the quasi-three-level pulse width modulation (PWM) scheme, was investigated in [20]. The approach is realized based on the understanding that the voltage reflection can be canceled by splitting the rising/falling switching transitions into two equal-voltage steps separated by a proper dwell time. This approach can effectively mitigate the motor overvoltage, overcoming the filters’ disadvantages [21]. However, the motor winding can still encounter high $dv/dt$ stress since the motor voltage has a steep-fronted two-level waveform. This results in uneven voltage distribution across the motor winding turns, where the first few turns can endure higher voltage than others, which potentially results in partial discharge and/or progressive insulation aging. Furthermore, the high $dv/dt$ at the motor terminals adversely impacts the electromagnetic interference (EMI) performance of the motor drive system [22], [23].

This article proposes a soft-switching voltage slew-rate profiling approach to mitigate the motor overvoltage while improving the EMI performance of SiC-based motor drives. The article extends the authors’ earlier conference paper [24] which preliminarily showed the effectiveness of using soft-switching inverters to eliminate the motor overvoltage with a sufficiently long rise/fall switching time, without increasing the switching power loss. As a rule of thumb, increasing the rise/fall time can mitigate the motor overvoltage. However, how to select the optimum rise/fall time for different cable lengths? What is the limitation of the slew-rate profiling approach? These questions are not clearly answered in the literature.

In this article, an optimal slew-rate of the output voltage switching transitions is derived for the first time in literature using the frequency- and time-domain analysis. The results show that the optimum slew-rate is pertinent to the cable antiresonance frequency. This article reveals that the essence of the motor overvoltage mitigation is because there is no exciting source for the overvoltage oscillations when the rise/fall time is set as $4t_p$, where $t_p$ is the wave propagation time from the inverter side to the motor side. It provides a new perspective of mitigating the motor overvoltage by shaping the inverter output voltage; i.e., as long as the component of the exciting source at the antiresonance frequency is zero, the motor overvoltage can be mitigated completely.

The auxiliary resonant commutated pole inverter (ARCP) is used as an example of the soft-switching inverter to experimentally verify the effectiveness of the proposed voltage slew-rate profiling approach. Besides the effective overvoltage mitigation, the voltage slew-rate profiling provides further advantageous features for the employed soft-switching inverter, including improving the system efficiency and the EMI performance. This is because the current and voltage of the switching devices are decoupled with reduced switching loss, and the output voltage slew-rate is flattened with reduced high-frequency spectral contents.

The rest of this article is organized as follows. Section II provides a brief modeling of the voltage reflection phenomenon in adjustable-speed drives as a basis for the derivation of the optimum slew-rate. Through frequency- and time-domain analysis, Section III derives the optimum rise/fall time to mitigate the motor overvoltage. Section IV presents the ARCP and its operation principle as the hardware platform for experimental verification. Section V experimentally compares the performance of the ARCP, the conventional hard-switching inverter, and the hard-switching inverter + $RLC$ $dv/dt$ filter. The remarks
are provided in Section VI. Finally, Section VII concludes this article.

II. VOLTAGE REFLECTION PHENOMENON IN ADJUSTABLE-SPEED DRIVES

A. Modeling of Adjustable-Speed Drives

Fig. 2 demonstrates the main components of a typical SiC-based adjustable-speed drive which encompasses a dc-link voltage $V_{dc}$, a voltage source inverter (VSI), power cables, and an ac electric motor [25]. The inverter generates a high-frequency PWM voltage with a rise/fall time that is generally in the range of $10^{-100}$ ns, depending on the switching device characteristics, load current conditions, and employed gate drivers.

The motor drive system, shown in Fig. 2, can be represented using the equivalent circuit elaborated in Fig. 3. The motor is modeled as an impedance $Z_m$, which represents the equivalent leakage inductance of the stator winding, the parasitic resistance and capacitance between the stator winding and motor frame, and the parasitic resistance and capacitance between the stator neutral and motor frame [26]. The inverter is modeled as a PWM voltage source with an impedance $Z_s$ that is typically neglected since the inverter’s dc-link capacitor behaves as a short circuit to the fast-rising pulses. The power cable is modeled as a lossless transmission line with an impedance $Z_c$, which is calculated based on the per-unit length cable inductance $L_c$ and capacitance $C_c$, as [25]

$$Z_c = \sqrt{L_c/C_c}. \quad (1)$$

B. Modeling of Voltage Reflection

In adjustable-speed drives, the PWM voltage generated by the VSI propagates through power cables in the same way as that of traveling waves in transmission lines, where the impedance mismatch between the power cable and the motor results in successive voltage reflections [8]. Fig. 4 depicts the voltage reflection process through a bounce diagram along with the inverter and motor voltage waveforms. It is assumed that the rise time $t_r$ of the voltage pulse is much shorter than the wave propagation time $t_p$ (i.e., $t_r \ll 3t_p$). Note that $t_p$ denotes the time that the voltage pulse travels from one end of the cable to the other [13].

The propagation time $t_p$ is calculated based on the cable length $l_c$ as

$$t_p = l_c\sqrt{L_c/C_c}. \quad (2)$$

The reflection coefficients at the inverter side $\Gamma_s$ and at the motor terminals $\Gamma_m$ are defined as

$$\Gamma_s = \frac{Z_s - Z_c}{Z_s + Z_c} \quad (3)$$

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c}. \quad (4)$$

Since the inverter impedance is typically near zero ($Z_s \approx 0$) and the motor impedance is usually much higher than the cable impedance ($Z_m \gg Z_c$), the reflection coefficients at the inverter and motor sides are almost unity (i.e., $\Gamma_s = -1$ and $\Gamma_m = 1$) [13]. It should be noted that $\Gamma_s = -1$ means the voltage is fully reflected at the inverter side with an inverted phase, while $\Gamma_m = 1$ means the voltage is fully reflected at the motor side with the same phase.

Referring to Fig. 4, at $t = 0$, a voltage pulse $V_s$ propagates from the inverter side through the cable to the motor side, where the motor voltage is initially at 0 V. When $t = t_p$, the inverter voltage pulse arrives at the motor side and experiences a backward voltage reflection to the inverter. The reflected voltage
$V_{m1}^-$ is calculated as

$$V_{m1}^- = \Gamma_m V_s.$$  \hspace{1cm} (5)

Therefore, after a wave propagation cycle, the motor voltage can be written as

$$V_{m1} = (1 + \Gamma_m) V_s.$$  \hspace{1cm} (6)

When $t = 2t_p$, the reflected voltage $V_{m1}^-$ arrives at the inverter side and experiences a forward voltage reflection to the motor terminals, as shown in Fig. 4. The reflected voltage $V_{s2}^+$ can be given as

$$V_{s2}^+ = \Gamma_s V_{m1}^-.$$  \hspace{1cm} (7)

At $t = 3t_p$, the incident voltage $V_{s2}^+$ arrives at the motor terminals and experiences another backward voltage reflection to the inverter side, where the motor voltage is expressed as [20]

$$V_{m2} = (1 + \Gamma_s \Gamma_n^2) V_s.$$  \hspace{1cm} (8)

Thereafter, the voltage reflections continue until the motor voltage oscillations are damped to the inverter voltage which is equal to $V_{dc}$. The damping time depends on the ac skin resistance of the motor and cable and the proximity effect in the cable. According to Fig. 4, the oscillation frequency of the motor overvoltage $f_{osc}$ can be given as

$$f_{osc} = 1/4t_p.$$  \hspace{1cm} (9)

It should be noted that the oscillation frequency is equal to the cable antiresonance frequency, which can be characterized by measuring the cable impedance at different operating frequencies [27].

Fig. 5 shows the experimentally obtained frequency response of a 1-m long four-core 13 AWG polyvinyl chloride (PVC) cable, where the antiresonance frequency is about 40.5 MHz. According to (9), for this 1-m cable, the theoretical overvoltage frequency is 40.5 MHz, which is equal to the cable’s antiresonance frequency. Therefore, the overvoltage oscillation frequency can be obtained by either theoretical calculation using (9) or experimental measurement of the cable impedance.

Referring to Fig. 1, the peak motor overvoltage significantly depends on the rise/fall time of the inverter voltage. Generally, when the switching rise/fall time is prolonged, the motor overvoltage can be alleviated, however, at the expense of the switching power loss. In this section, a voltage slew-rate profiling approach is proposed to mitigate the motor overvoltage using soft-switching inverters with comparable efficiency to the conventional hard-switching inverters. An optimal rise/fall time of the inverter voltage switching transitions, which results in a regulated motor voltage, is mathematically analyzed in the frequency domain with further illustration in the time domain.

### A. Frequency-Domain Analysis

The inverter output voltage can typically be represented by a trapezoidal pulse-train, as shown in Fig. 6, where $A$ is the pulse voltage amplitude, $\tau$ is the average pulsewidth measured at half the pulse amplitude, $T$ is the fundamental cycle, and $t_r$ and $t_f$ are the pulse rise and fall times, respectively. For simplicity, the trapezoid is assumed to be symmetrical (i.e., $t_r = t_f$) with a constant duty ratio ($D = \tau/T$).

According to Fourier analysis, the trapezoidal waveform described by Fig. 6 can be expressed as [28]

$$V(t) = \sum_{n=-\infty}^{n=\infty} c_n e^{jn\omega t}$$  \hspace{1cm} (10)

where $\omega$ is the angular frequency of the waveform and $c_n$ is the Fourier series coefficient which is given as

$$c_n = AD \text{sinc} \left( \frac{n\pi T}{2} \right) \text{sinc} \left( \frac{n\pi \tau}{2} \right) e^{-jn\omega \left( \frac{\tau + \tau}{2} \right)}.$$  \hspace{1cm} (11)

where $\text{sinc}(x) = \sin(x)/x$.

At the antiresonance frequency of the cable, the Fourier series coefficient is

$$c_n = AD \text{sinc} \left( \frac{n\pi f_{osc}\tau}{2} \right) \text{sinc} \left( \frac{n\pi f_{osc}t_r}{2} \right) e^{-jn\pi f_{osc}(\tau + t_r)}.$$  \hspace{1cm} (12)

From (12), it can be derived that $c_n = 0$ when $t_r = 1/f_{osc}$ where, at this rise/fall time setting, there is no inverter voltage excitation for the cable antiresonance, i.e., the motor overvoltage is ideally eliminated. Recalling (9), the optimal rise/fall time for the inverter voltage is

$$t_{r,\text{opt}} = 4t_p.$$  \hspace{1cm} (13)
The overvoltage mitigation with the proposed slew-rate profiling approach can be further illustrated in the time domain, as depicted in Fig. 7. An inverter voltage pulse \( V_s \) is assumed to propagate through a cable that has a length \( l_c \) and a propagation time \( t_p \), which can be calculated using (2). To mitigate the motor overvoltage at the cable end-side, the rise time of the inverter voltage pulse is set to the optimal value given by (13). The resultant motor voltage waveform can be derived using the superposition principle, where the inverter voltage pulse is split into two identical voltage pulses \( V_{s1} \) and \( V_{s2} \), as given by (14), with equal magnitude and a time displacement of \( 2t_p \).

\[
V_s = V_{s1} + V_{s2}.
\]  

Accordingly, the resultant motor voltage \( V_m \) is given as

\[
V_m = V_{m1} + V_{m2}
\]

where \( V_{m1} \) and \( V_{m2} \) are the consequent motor voltages due to the propagation of the inverter voltages \( V_{s1} \) and \( V_{s2} \), respectively.

With unity reflection coefficients at the inverter and motor sides, the voltage pulses \( V_{s1} \) and \( V_{s2} \) experience full voltage reflection when arriving at the motor side. Therefore, the voltage magnitude of \( V_{m1} \) and \( V_{m2} \) is \( V_{dc} \) (i.e., double the voltage magnitude of \( V_{s1} \) and \( V_{s2} \)), while the oscillation frequency is \( 1/4t_p \). Since \( V_{m2} \) lags \( V_{m1} \) by \( 2t_p \), the overvoltage oscillations of the reflected waves \( V_{m1} \) and \( V_{m2} \) are counterbalanced altogether, as demonstrated in Fig. 7. Thus, the motor voltage waveform \( V_m \) is regulated at the inverter rated voltage. Referring to Fig. 7, it is worth noting that at the switching rise time midway, \( V_m \) crosses \( V_s \) at half the voltage level (i.e., \( V_m = V_s = 0.5V_{dc} \) at \( 2t_p \)). This is a necessary condition to counterbalance the overvoltage oscillations associated with the voltage reflection.

Although Fig. 7 validates the concept of the overvoltage mitigation at a rising switching transition with \( t_r = 4t_p \), the same results can be obtained at the falling switching transitions when \( t_f = 4t_p \).

C. Simulation Case Study

To verify the proposed optimal voltage slew-rate for overvoltage mitigation, a MATLAB/Simulink model is used to emulate the overvoltage phenomenon in a cable-fed motor drive system at different inverter switching rise times. The detailed cable simulation model and parameters can be found in Appendix I. It should be noted that to emulate the worst case, the motor side is regarded as an open circuit, where the reflection coefficient is unity. Fig. 8 shows the inverter and motor voltage waveforms when the switching rise time is set as integer multiples of the wave propagation time.

When the rise time equals the wave propagation time (i.e., \( t_r = t_p \)), the inverter voltage experiences full voltage reflection, where the peak motor voltage is 2 p.u., as shown in Fig. 8(a). When the switching rise time is increased to triple the wave propagation time (i.e., \( t_r = 3t_p \)), the peak motor voltage can be reduced to 1.4 p.u., as shown in Fig. 8(b). With the optimal setting of the rise time (i.e., \( t_r = 4t_p \)), the motor voltage is regulated at the inverter nominal voltage with negligible oscillations, as shown in Fig. 8(c). However, with the rise time further increasing to five times the wave propagation time (i.e., \( t_r = 5t_p \)), the overvoltage is partially attenuated to 1.25 p.u., as shown in Fig. 8(d).
The variation of the motor peak voltage with different rise times is shown in Fig. 9. Overall, the motor overvoltage decreases when the rise time is increased. Importantly, there is almost no motor overvoltage when $t_r = 4n t_p$ ($n = 1, 2, 3, \ldots$), where, at these specific rise times, the inverter voltage does not excite the cable antiresonance.

IV. IMPLEMENTATION OF SLEW-RATE PROFILING WITH THE ARCPI

As analyzed in Section III, setting the rise/fall time of the inverter output voltage as $4n t_p$ can entirely mitigate the motor overvoltage. In this section, the proposed slew-rate profiling approach is implemented using a SiC soft-switching inverter which is denoted as the ARCPI.

A. ARCPI

The ARCPI was first proposed in the 1990s [30] and has been a popular soft-switching inverter topology due to its simple structure, high degree of PWM compatibility, and independent phase control [31]. In addition, the output voltage waveform can be effectively profiled with controllable $\frac{dv}{dt}$ using a resonant circuit [23]. Therefore, the ARCPI is selected herein as a candidate topology to implement the proposed voltage slew-rate profiling approach.

Fig. 10 shows the circuit diagram of a single-phase SiC-based ARCPI, where a standard half-bridge phase-leg, formed by two switching devices ($S_1$ and $S_4$), is incorporated with an auxiliary resonant circuit between the output node A and the dc bus middle point O [30]. The auxiliary resonant circuit is composed of two auxiliary switches ($S_2$ and $S_3$), a resonant inductor ($L_r$), and two snubber capacitors ($C_{r1}$ and $C_{r4}$). It should be noted that two clamping diodes ($D_{c1}$ and $D_{c2}$) are used to protect the auxiliary switches against overvoltage due to the resonance between the parasitic capacitance of the auxiliary switching devices and the resonant inductor ($L_r$) [31]. The three-phase ARCPI version is realized by employing three phase-legs with the three auxiliary resonant circuits sharing the same dc bus middle point O.

B. Principle of Operation

The ARCPI operation process has been extensively described in pieces of literature [22], [23], [30], and [31]. Here, only some basic operation processes will be recalled with the intent of making the article almost completely self-contained.

Fig. 11 shows waveforms of the gate signals, the resonant inductor current $i_{Lr}$, and the output voltage $V_{pole}$ during switching transitions when the phase current $i_{phase} > 0$, where Fig. 11(a) elucidates the turn-ON process of the main switch $S_1$, while the opposite case is shown in Fig. 11(b). The phase current $I_{phase}$ is considered constant during the switching transitions. Note that the auxiliary switch $S_2$ is involved in the switching commutation from the bottom main switch $S_4$ to top main switch $S_1$, while the auxiliary switch $S_3$ is involved in the opposite switching commutation process.

Referring to Fig. 11(a), the turn-ON switching transitions of the main switch $S_1$ start with the auxiliary switch $S_2$ turning ON at $t_1$. The resonant inductor current $i_{Lr}$ increases linearly with time, depending on the resonant inductance $L_r$ and the dc-bus voltage $V_{dc}$. The inductor current can be calculated as

$$i_{Lr} = \frac{V_{dc}}{2L_r} t. \quad (16)$$
At $t_2$, the inductor current equals the phase current and then continues to ramp up to the prescribed trip current $I_{\text{trip, on}}$. The additional inductor current exceeding the phase current is called the boost current $I_{\text{boost, on}}$, which is necessary to guarantee the success of the imminent resonance process.

According to (16), the ramp up time $t_{\text{ramp, on}}$ can be calculated as

$$t_{\text{ramp, on}} = \frac{2L_r I_{\text{trip, on}}}{V_{\text{dc}}}.$$  \hfill (17)

The boost current $I_{\text{boost, on}}$ can be given as [23]

$$I_{\text{boost, on}} = I_{\text{trip, on}} - I_{\text{phase}}.$$  \hfill (18)

With the main switch $S_4$ turning OFF at $t_3$, $L_r$ resonates with the two snubber capacitors $C_{r1}$ and $C_{r4}$, where they are charged and discharged in a sinusoidal manner, respectively. Thus, the output voltage $V_{\text{pole}}$ swings from zero to $V_{\text{dc}}$ in a resonant way until it is clamped by the antiparallel diode of the main switch $S_1$ at $t_4$. Since the voltage across the main switch $S_1$ is clamped to zero by its antiparallel diode, $S_1$ can be turned ON under zero-voltage switching with zero switching loss, theoretically.

Finally, the inductor current $t_{Lr}$ decreases in a linear manner. Once the inductor current reaches zero, the auxiliary switch $S_3$ can be turned OFF to complete the commutation process.

The resonant interval $t_{\text{res, on}}$ can be calculated as [23]

$$t_{\text{res, on}} = \frac{2}{\omega_r} \tan^{-1} \left( \frac{V_{\text{dc}}}{2Z_r (I_{\text{trip, on}} - I_{\text{phase}})} \right)$$  \hfill (19)

where $\omega_r$ and $Z_r$ are the resonant angular frequency and resonant impedance of the ARCPI, respectively, and are given as

$$\omega_r = \sqrt{1/2L_r C_r}.$$  \hfill (20)

$$Z_r = \sqrt{L_r/2C_r}.$$  \hfill (21)

Similar commutation processes apply to the turn-OFF switching transitions of the main switch $S_1$, as demonstrated in Fig. 11(b). The resonant interval during the turn-OFF switching process can be calculated as

$$t_{\text{res, off}} = \frac{2}{\omega_r} \tan^{-1} \left( \frac{V_{\text{dc}}}{2Z_r (I_{\text{trip, off}} + I_{\text{phase}})} \right)$$  \hfill (22)

where $I_{\text{trip, off}}$ is the tripped current for the turn-OFF process.

Note that the boost current $I_{\text{boost, off}}$ during the turn-OFF process is different from that of the turn-ON process, where $I_{\text{boost, off}}$ is given as [23]

$$I_{\text{boost, off}} = I_{\text{trip, off}} + I_{\text{phase}}.$$  \hfill (23)

Overall, all the main switches of the ARCPI achieve zero-voltage switching and all the auxiliary switches achieve zero-current switching. The voltage and current of the main switches are decoupled and the output voltage waveform is smoothed and slowed down in a sinusoidal manner, which is realized using the auxiliary resonant circuit.

The ARCPI can be controlled using two classical control methods: fixed-timing control and variable-timing control [32]. Fig. 12 compares the two control methods in terms of the trip current $I_{\text{trip, on}}$ and the resonant interval $t_{\text{res, on}}$ during the turn-ON transitions when $t_{\text{phase}} > 0$.

Referring to Fig. 12(a), the variable-timing control approach adjusts the trip current according to the load current, which would increase the control complexity. On the other hand, the variable-timing control has a constant resonant time as a benefit, as demonstrated in Fig. 12(b). Since the voltage slew-rate profiling approach needs to set the rise time as the optimum time $4t_p$, only the variable time control is suitable to carry out the slew-rate profiling approach.

C. Selection of Design Parameters

In this section, a design procedure for the experimental ARCPI prototype is presented. The design flow diagram is shown in Fig. 13, where the process begins by the specification defining (e.g., the dc-link voltage and cable length) and ends with the resonant parameters, including the resonant inductance and the snubber capacitance.

A case study for a three-phase 5-kW SiC ARCPI supplying an ac motor from a 500-V dc-link through a 12-m long cable is considered. The wave propagation time $t_p$ is about 73 ns. The maximum modulation index is 0.83, where such a circuit condition leads to a maximum load current $I_{\text{peak}} = 18$ A.

1) Selection of the Rise/Fall Time: According to the analysis in Section III, the optimum rise time $t_{\text{opt}}$ is $4t_p$ (i.e., $t_{\text{opt}} = 292$ ns). Note that, in addition to the rise time, the fall time can...
also affect the voltage reflection [20]. Thus, the fall time is set as 4\(t_p\) as well.

2) Selection of the Trip Current: In the ARCPI, the switching devices in the auxiliary branches experience the highest current stress during the switching commutation process. The maximum current in the auxiliary branch \(I_{aux.pk}\) is calculated as

\[
I_{aux.pk} = I_{peak} + \sqrt{\left(\frac{V_{dc}}{2Z_r}\right)^2 + (I_{trip.on} - I_{phase})^2}. \tag{24}
\]

The amplitude \(I_{aux.pk}\) is an indicator for the current stress and power loss in the auxiliary branches during the switching commutation process of the ARCPI. A larger trip current will result in higher current stress and conduction loss in the auxiliary branches. Therefore, a smaller trip current is recommended to reduce the current stress of the switching devices and the power loss in the auxiliary branches.

According to (19) and (22), the output voltage with the same rise and fall time can be achieved by meeting the following condition:

\[
I_{trip.on} - I_{phase} = I_{trip.off} + I_{phase}. \tag{25}
\]

Since the trip current should be larger than zero, the minimum boost current at the maximum load condition \(I_{peak}\) can be given as

\[
I_{boost.on} = I_{boost.off} = I_{peak}. \tag{26}
\]

3) Selection of the Resonant Circuit Parameters: According to the commutation process in Section IV-B, the resonant inductance can be designed as

\[
L_r = \frac{V_{dc}t_{ramp.on}}{4I_{phase\_max}}. \tag{27}
\]

According to (27), the resonant inductance is determined by the dc-link voltage \(V_{dc}\), the load current \(I_{phase\_max}\), and the ramp-up time \(t_{ramp.on}\). Therefore, when \(t_{ramp.on} = 400\) ns, the resonant inductance is \(L_r = 2.7\) \(\mu\)H.

Substituting the optimum rise time \(t_{opt} = 292\) ns and \(I_{boost.on} = 18\) A, and \(L_r = 2.7\) \(\mu\)H into (19)–(21) results in \(C_r = 9.2\) nF. Due to the availability of the capacitor, the capacitance of 8.2 nF is selected. Note that the resonant circuit parameters are designed under the ideal conditions. However, the parasitic resistance in the resonant circuit and the turn-ON and turn-OFF delays of the switches would affect the resonant interval. Therefore, the boost current should be tuned during the experiment.

V. EXPERIMENTAL RESULTS

In order to verify the proposed approach, a three-phase ARCPI based on SiC MOSFETs from Wolfspeed is used to supply a three-phase four-pole 2.2-kW motor through 12-m long 12 AWG PVC cable, as shown in Fig. 14. It should be noted that at the high-frequency region, the magnetic flux is confined in the semiclosed slot region and no flux links the rotor. Therefore, the impedance characteristics are the same as the standard motor even without the rotor [27], [35]. Henceforth, only the stator winding is used to perform the experiment. Table I presents the main parameters of the experimental prototype. The results are shown for a relatively short cable (12 m) to emphasize that the voltage reflection issue is more common and severe in SiC-based drives when compared with the Si-based counterpart due to the faster switching speed, where the motor voltage can be doubled using few meter cables, as evidenced in Fig. 1. The effectiveness of the proposed slew-rate profiling approach can be invariably extended to longer cable lengths (tens of meters or hundreds of meters) as long as the rise/fall times equal \(4t_p\). The ideal rise time can be determined through offline methods which are given in Appendix II.

The results obtained under the ARCPI are compared with the hard-switching inverter and the hard-switching inverter + RLC \(dv/dt\) filter case. The hard-switching inverter can be easily realized by removing the auxiliary circuit branch of the ARCPI. The RLC \(dv/dt\) filter is installed at the inverter side, as shown in Fig. 15. The filter parameters \((L_f, C_f, R_f)\), shown in Table I, are designed according to the method presented in [14].
The SiC MOSFETs are driven using gate drivers with 25-Ω gate resistance. In this case, the switching time for the hard-switching inverter is nearly 50 ns. The inverter is controlled by a digital signal processor (DSP) (TI TMS320F28335) and an field-programmable gate array (FPGA) (XILINX XC3S400).

The ARCPI is modulated using the variable-timing control approach with 20 kHz and 50 Hz as the switching and fundamental frequencies, respectively. Fig. 16 shows the flowchart for the variable-timing control approach based on the DSP/FPGA board for one phase. Note that the ramp times \( t_{ramp, on} \) and \( t_{ramp, off} \) are calculated in the DSP based on (17) and (18) for a given load current. Since the variable-timing control approach has a fixed rise/fall time, the rise time \( t_r \), shown in Fig. 16, is set as a constant. The auxiliary time \( t_{aux} \) is the total commutation time during the switching transient. The PWM signals for the switches in the ARCPI are generated by the FPGA.

The hard-switching inverter is modulated with the sinusoidal pulse width modulation (SPWM) with the same frequencies as the ARCPI. To limit the maximum phase current flowing through the stator, the inverter is supplied from 300-V dc-link and the modulation index is set to 0.2. The experimental results are presented in Figs. 17–25.

Fig. 17 shows the inverter output currents of phases A and B (\( I_A \) and \( I_B \)), the inverter output line voltage from phase A to phase B (\( V_{s} \)), and the corresponding line voltage at the motor terminals (\( V_m \)), for two fundamental cycles. Note that the phase currents are measured at the inverter output nodes. The experimental results for the hard-switching inverter, the hard-switching inverter + \( dv/dt \) filter, and the ARCPI are shown in Fig. 17(a)–(c), respectively.

As can be noticed in Fig. 17(a), a significant overvoltage, which is about 2.0 p.u., exists across the motor terminals for the hard-switching inverter due to the voltage reflections. Referring to Fig. 17(b), the motor overvoltage can be attenuated when the \( dv/dt \) filter is used, where the maximum overvoltage is about 1.35 p.u. In contrast, the motor overvoltage is entirely mitigated when the ARCPI is used, as shown in Fig. 17(c). Both the \( dv/dt \) filter and the ARCPI can mitigate the motor overvoltage due to prolonged rise/fall times, which will be analyzed in the following section.

While the \( dv/dt \) filter can effectively mitigate the motor overvoltage, it results in higher output current at the inverter side. Compared with the output currents of the hard-switching inverter in Fig. 17(a), the currents of the hard-switching inverter + \( dv/dt \) filter in Fig. 17(b) have larger spikes. The reason is that during the switching transient, a large current flows through the \( dv/dt \) filter. This can be further illustrated in Fig. 18, where it shows the load current \( I_{load} \), the inverter output current \( I_A \) for phase A, the inverter output voltage \( V_s \), and the filter output voltage \( V_f \) during the switching transient. Referring to Fig. 18, the inverter output current is much higher than the load current, where the additional current flows through the capacitor and damping resistor of the \( dv/dt \) filter. Since the \( dv/dt \) filter results in higher inverter output current, the inverter power loss will be accordingly increased. It is worth noting that current flowing through the filter can be reduced by increasing the inductance of the RLC \( dv/dt \) filter. However, the voltage drop across the filter is proportional to the inductance, i.e., a larger inductance will result in larger voltages drop, which will reduce the effective voltage applied to the load. Considering the tradeoff between the voltage drop and the current flowing through the filter, the inductance is selected as 2.7 \( \mu \)H [14].

In contrast, referring to Fig. 17(c), the inverter output current of the ARCPI is cleaner than those of the hard-switching inverter and the hard-switching inverter + \( dv/dt \) filter. This is because the ARCPI is a soft-switching inverter with a slowed and smoothed output voltage. Therefore, when compared with the hard-switching inverter + \( dv/dt \) filter, the ARCPI can reduce the main switching devices’ current stress. The high-frequency harmonics of the current for the hard-switching inverter shown in Fig. 17(a) are due to the high \( dv/dt \) charging and discharging of the cable parasitic capacitance.

Figs. 19–21 provide experimental results for one switching cycle for the hard-switching inverter, the hard-switching inverter + \( dv/dt \) filter, and the ARCPI, respectively.

### Table I: Experimental Prototype Parameters

| Symbol               | Value       |
|----------------------|-------------|
| Switching Device     | C2M0040120D |
| Resonant inductance   | 2.7 \( \mu \)H |
| Snubber capacitance  | 8.2 nF     |
| Gate driver resistance | 25 \( \Omega \) |
| Switching frequency  | 20 kHz     |
| Fundamental frequency | 50 Hz      |
| Control method       | Variable timing control |
| \( dv/dt \) filter   |             |
| Filter inductance     | 2.7 \( \mu \)H |
| Filter capacitance    | 22 nF      |
| Filter damping resistance | 25 \( \Omega \) |
| Cable                |             |
| Cable length         | 12 m       |
| Cable gauge          | 12 AWG     |
| Cable per-unit inductance | 0.26 \( \mu \)H |
| Cable per-unit capacitance | 104.7 pF  |
| Motor                |             |
| Motor type           | Induction motor |
| Phase number         | 3          |
| Pole number          | 4          |
| Power rating         | 2.2 kW     |
| Controller           |             |
| DSP                  | TI TMS320F28335 |
| FPGA                 | XILINX XC3S400 |

Fig. 15. RLC \( dv/dt \) for SiC-based adjustable-speed drives.
In Fig. 19(a), the motor voltage oscillates in a damped manner, where the maximum overvoltage is 1.95 p.u. for both the rising and falling edges. The high voltage oscillation is due to the reflected wave phenomenon caused by the fast voltage slew-rate and the impedance mismatch, as previously analyzed. The enlarged views of this switching cycle during the rising and falling transitions are presented in Fig. 19(b) and (c), respectively.

Referring to Fig. 20(a), with the adoption of the $\frac{dv}{dt}$ filter, the inverter output voltage $V_s$ is smoothed as $V_f$, where the rise/fall times are about 400 ns. However, the filter output voltage is a bit higher than that of the converter, which is about 1.32 p.u. Since the rise/fall time of the inverter output voltage is slowed, the motor overvoltage is limited to 1.35 p.u. This is highlighted in Fig. 20(b) and (c).

With the adoption of the ARCPI, Fig. 21(a) shows that the motor voltage oscillation is entirely eliminated due to the prolonged rise/fall time of the output voltage. This is highlighted in Fig. 21(b) and (c), showing the enlarged view of this switching cycle during the falling and rising transitions, where the rise and falling times are about 400 ns. The inverter voltage $V_s$ equals $V_m$ at the midway. If the rise time is faster than the optimum rise time, partial overvoltage can only be achieved as shown in Fig. 22, where Fig. 22(a) and (b) shows the rise and fall edges, respectively. Common to both figures, the motor overvoltage is about 1.33 p.u. and the inverter voltage $V_s$ equals $V_m$ after the midway.

In addition to mitigating the overvoltage, the slew-rate profiling inherits the benefits of the ARCPI, such as the better EMI performance. Fig. 23 shows the frequency spectrum of the motor terminal voltage under the hard-switching and the ARCPI. As can be noticed, using the ARCPI attenuates the high-frequency harmonics (1 MHz onward) due to the prolonged rise/falling times of the output voltage of the ARCPI as seen in Fig. 21, when compared with that of the hard-switching inverter, as seen in Fig. 19. In addition, the high-frequency voltage oscillations caused by the reflected wave phenomenon in the hard-switching inverter further deteriorate the EMI. For example, the protuberances of the frequency spectrum at 2.7 MHz are caused by the high-frequency oscillations, as seen in Fig. 19, and the ARCPI can successfully attenuate it, which is further highlighted in Fig. 23.

On comparing with the hard-switching converter, the device voltage and current in the ARCPI are decoupled during the switching transient, which can reduce the switching loss as shown in Fig. 24. This significantly increases the system efficiency. Fig. 25 compares the efficiency of the ARCPI and the hard-switching inverter $+\frac{dv}{dt}$ filter. It should be noted that the efficiency is measured with a three-phase RL load, where, for each phase, the load resistance is 11 Ω and the load inductance is 5 mH. Since the output voltage and current have very high $\frac{dv}{dt}$ and oscillations, the conventional method to calculate the efficiency using a power analyzer will be inaccurate. Hence, high bandwidth current and voltage probes and oscilloscopes are used to capture the accurate waveforms and work out the efficiency in this article. The efficiency is calculated offline by measuring the instantaneous three-phase load voltages ($v_a$, $v_b$, and $v_c$) and currents ($i_a$, $i_b$, and $i_c$) and the dc-link voltage $V_{dc}$ and current $I_{dc}$. The voltages and currents are measured by high bandwidth and high sampling rate oscilloscope HD80000 from Teledyne LeCroy (1 GHz; 2.5 GSa/s). The differential voltage probes from Pico Technology (TA042, 100 MHz, 1 kV) and the current probe from Agilent Technologies (N2783A, 100 MHz, 30 A) are utilized for the voltage and current measurement, respectively. To ensure the measurement accuracy, all the channels are de-skewed and the offset is compensated before the measurement. Note that other measurements, such as the calorimeter, can be used to improve the measurement accuracy [33].

Referring to Fig. 25, the efficiency of the ARCPI is much higher than that of the hard-switching inverter $+\frac{dv}{dt}$ filter,
where the maximum efficiency of the ARCPI is about 99%, while the maximum efficiency of the hard-switching inverter + $dv/dt$ is about 95%. The ARCPI shows higher efficiency at a different operation range because the ARCPI is a soft-switching inverter where the switching loss is significantly reduced as evidenced in Fig. 24(b). For the hard-switching inverter + $dv/dt$ filter, the power loss is mainly caused by the damping resistor in the $dv/dt$ filter. According to [14], increasing the inductance of the filter can reduce the power loss in the damping resistor since the power loss is inversely proportional with the inductance when the rise time is fixed. However, larger inductance will result in high power loss in the inductor since the full load current will flow through the inductor. In addition, the filter results in higher current in the converter as shown in Fig. 18, which will further increase the power loss in the converter.

VI. REMARKS

A. Applications and Power Level

Generally, the reflection coefficient at the motor terminal decreases with the power rating because the motor characteristic impedance decreases with the power rating [34]. Therefore, the effectiveness of the motor overvoltage mitigation is more pronounced in the low power range.
While the motor overvoltage in the high-power application is not as serious as that of the low power application, the efficiency improvement is very fascinating. Compared with the conventional hard-switching inverter + $dv/dt$ filter approach, the ARCPI has higher efficiency owing to its soft-switching characteristics, as evidenced in Section V. Therefore, the size of the heatsink would be decreased significantly, which can improve the power density of the system. For example, for high-power motor drives such as a 1-MW converter, if the efficiency increases from 98% to 99%, the power loss would decrease from 20 to 10 kW, which would significantly reduce the cooling requirement.

Therefore, there are no limitations for the ARCPI regarding the power level in theory. The ARCPI has better performance than the conventional hard switching + $dv/dt$ filter in terms of the motor overvoltage mitigation and the system efficiency.

However, when compared with the two-level inverter + filter approach, the ARCPI uses more switching devices, which would reduce the reliability and increase the control complexity.

### B. Impact of the Cable Length on the Parameters of the ARCPI

In general, the propagation time $t_p$ for a 1-m cable is about 5 ns [6]. So, for a 100-m cable-fed motor drive system, the ideal rise time $4 t_p = 2 \mu s$. If the cable length increases to several hundred meters, the required rise time is extremely long which can adversely affect the dc-link voltage utilization and the switching frequency. In this case, the slew-rate profiling is not practical where new approaches such as integrating the inverter into the motor housing [36] may be used. Therefore, the
following section will analyze the impact of cable length on the design of the resonant inductor $L_r$ and capacitor $C_r$ when the cable length is less than 100 m.

According to (27), the resonant inductance is independent of the resonant interval. Taking the 500-V, 5-kW ARCPI as an example, the resonant inductance is 2.7 $\mu$H, i.e., the size of the inductor remains constant regardless of the cable length.

According to (19)–(21), when the resonant inductance is 2.7 $\mu$H, the resonant capacitance increases with the rise time as shown in Fig. 26. Specifically, the resonance capacitance is 106 nF when the rise time is 2 $\mu$s. Since the capacitance is less than 106 nF, the capacitor size does not increase too much.

In summary, the proposed voltage slew-rate profiling approach is suitable for cable lengths that are not longer than a few hundreds of meters. The size of the inductor remains fixed and the size of the capacitor does not increase too much with the cable length.

C. Control Flexibility

Fig. 27 illustrates the resonant time during the turn-ON commutation at different boost currents under the circuit and loading conditions as discussed in Section IV-C. It shows that the resonant interval decreases with the boost current. Therefore, we can tune the boost current to adjust the resonance interval to be the optimum rise time in response to cable parameters varying, without redesigning the resonant circuit.

D. Impact of the ARCPI on the Double Pulsing Region

Fig. 28 shows the simulation results for voltages at the inverter side $V_s$ and the motor side $V_m$ at the double pulsing region. Referring to Fig. 28(a), when the motor is supplied by the
Fig. 27. Resonant interval at different boost current levels during the turn-ON transitions.

Fig. 28. Impact on the double pulsing region for (a) hard-switching inverter and (b) ARCPI.

The hard-switching inverter and the pulse duration is very small, the second voltage pulse is applied to the motor terminals before the first reflected pulse is fully decayed, resulting in about 2.9 p.u. overvoltage. In contrast, using the ARCPI, the double pulsing effect can be effectively mitigated, as evidenced in Fig. 28(b).

In summary, the ARCPI is an active control method to mitigate the motor overvoltage. It can completely mitigate the motor overvoltage due to the reflected wave phenomenon. It offers flexible control ability and improves the efficiency and the EMI performance of the adjustable-speed drives.

VII. CONCLUSION

This article has proposed a slew-rate profiling approach to mitigate the motor overvoltage in SiC-based cable-fed motor drives due to the reflected wave phenomenon. A general idea of oscillation mitigation in the motor drives has been discussed from the perspective of frequency domain and time domain. It provides a novel point of view to understand the overvoltage mitigation. The optimum rise/fall time is quantitatively identified for the first time in the literature. The theoretical analysis shows that in addition to the impedance mismatch between the cable and the motor, the fast rise/fall time of the inverter output voltage affects the peak motor voltage when the cable length is fixed. By actively profiling the rise/fall time as the cable antiresonant period, i.e., $4t_p$, the motor overvoltage can be fully mitigated. The philosophy used to solve the overvoltage problem is to eliminate the exciting source for the overvoltage by shaping the inverter output voltage, i.e., the component of the exciting source at the antiresonance frequency is zero. The effectiveness of the slew-rate profiling has been experimentally verified with the SiC ARCPI cabled-fed drives. The experimental results show that the SiC ARCPI can completely eliminate the motor overvoltage and improve the efficiency and the EMI performance at the high-frequency region due to the prolonged rise/fall time of the output voltage, when compared with the conventional hard-switching inverter.

APPENDIX I

THE SIMULATION MODEL

The cable model presented in [29] is used to simulate the reflected wave phenomenon. Fig. 29 shows the model for a 1-m long cable. The long cable model can be obtained by cascading the 1-m cable model multiple times depending on the required cable length. To emulate the worst case, the motor side is regarded as an open circuit, where the reflection coefficient is unity. The cable parameters are listed in Table II.
### APPENDIX II

**THE IDEAL RISE TIME CALCULATION METHODS**

There are three common offline methods to calculate the ideal rise time.

1) The first is using an oscilloscope to measure the propagation delay between the incident voltage (inverter voltage $V_s$) and the resultant voltage (motor terminal voltage $V_m$). Since the time shift is the wave propagation time ($t_p$), the ideal rise time can be calculated as $4t_p$. Note that this method can be used in the lab before the deployment of the drives since the inverter and the motor are usually placed in separate locations in real applications, where it is difficult to measure the inverter voltage and the motor voltage at the same time. In general, the long cable is looped together to calculate the wave propagation time due to the limited space in the lab. In fact, there is no significant difference between the looped cable and straight cable. Fig. 30 compares the experimental results for the long cable-fed motor drive system when the cable is looped and not looped, where $V_{m-ring}$ and $V_{m-straight}$ are the motor voltages using the ring-coiled (looped) cable and straight cable, respectively. As shown, the wave propagation time $t_p$ does not vary too much for the two cases. To further illustrate the characteristic impedance difference between the ring-coiled cable and straight cable, the common mode (CM) impedance of a 12.5-m long four-coil 13 AWG unshielded PVC cable is measured using an impedance analyzer (WAYNE KERR 6500B) for the two cases, as shown in Fig. 31. As can be noticed, the CM impedance of the straight cable is slightly larger than that of the ring-coiled cable, and the antiresonance frequency for both cases are the same. Therefore, the wave propagation time remains the same.

2) The second is by measuring the cable’s first antiresonance frequency, which corresponds to $1/4t_p$, as shown in Fig. 31, and then the optimal time can be calculated. Note that the cable’s first antiresonance frequency can be obtained by measuring its CM impedance using an impedance analyzer. Fig. 32 shows how to measure the CM impedance, where Fig. 32(a) and (b) show the single-phase and three-phase cases, respectively. Referring to Fig. 32(a), for the single-phase case, the live and neutral terminals are short-circuited into a common terminal from both ends, while the cable CM impedance is obtained by measuring the impedance between the common terminal and the cable earth wire in open-circuit configuration. Referring to Fig. 32(b), for a three-phase case, the equivalent CM circuit is formed as a two-port network with the paralleled three-phase and ground wire [37]. Therefore, the CM impedance can be obtained by measuring the impedance of the two-port network in open-circuit configuration, as shown in Fig. 32(b).

3) Finally, it is achieved by calculating the propagation time $t_p$ based on the cable length $l_c$, the per-unit length cable inductance $L_c$, and capacitance $C_c$ according to (2). The ideal rise time can be calculated as $4t_p$. In general, the cable’s $L_c$ and $C_c$ are not listed in the datasheet. These parameters can be extracted from the short-circuit and open-circuit impedance measurements. Fig. 33 illustrates the measurement schematics,

### TABLE II

**CABLE PARAMETERS USED IN SIMULATION**

| Symbol | Value   | Symbol | Value   |
|--------|---------|--------|---------|
| $R_{c1}$ | 0.017 Ω | $R_{c2}$ | 0.143 Ω |
| $L_{c1}$ | 0.38 μH | $L_{c2}$ | 0.16 μH |
| $R_{p4}$ | 34.75 MΩ | $C_{p1}$ | 64 pF   |

Fig. 30. Voltages of the inverter and motor when the cable is straight and looped.

Fig. 31. CM impedance of ring-coiled cable and straight cable.

Fig. 32. Cable CM impedance measurement schematic for (a) single-phase case and (b) three-phase case.

Fig. 33. Measurement schematics,
where Fig. 33(a) and (b) shows the measurement schematics for short-circuit and open-circuit, respectively.

Fig. 34 shows the impedance for a 1-m sample cable, where Fig. 34(a) and (b) shows the impedance for short-circuit and open-circuit, respectively. $L_c$ can be determined from the 20 dB/decade slope of short-circuit impedance as shown in Fig. 34(a). However, $C_c$ can be determined from the –20 dB/decade slope of open-circuit impedance as shown in Fig. 34(b) [29].

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