Implementation of the 2-D Wavelet Transform into FPGA for Image

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Abstract. This paper presents a hardware system implementation of the discrete wavelet transform algorithm in two dimensions for FPGA, using the Daubechies filter family of order 2 (db2). The decomposition algorithm of this transform is designed and simulated with the Hardware Description Language VHDL and is implemented in a programmable logic device (FPGA) XC3S1200E reference, Spartan IIIE family, by Xilinx, taking advantage the parallel properties of these which gives us and speeds processing that can reach them. The architecture is evaluated using images input of different sizes. This implementation is done with the aim of developing a future images encryption hardware system using wavelet transform for security information.

1. Introduction

The innovative techniques used for digital image processing enable improvements in image quality. As is the case of the mathematical technique discrete wavelet transforms (DWT). This transform is capable of providing time and frequency information simultaneously [1]. The image is filtered through a series of low-pass filters and high-pass, gaining lots of high and low frequency of the image. The interest in the wavelet transform has increased substantially in recent years for its large number of applications including signal analysis, signal compression and telemedicine.

This article presents an implementation of the discrete wavelet transform using the tool of FPGA hardware design (Field Programmable Gate Array), which can reduce development time considerably, taking advantage of the properties in parallel that this offers, that is to say; they can make agile the time of process of many applications similar in implementations in software tools.

Because of its reconfigurable nature, the tasks multiples developed in the FPGA’s different times can implement, reason why the systems can be scalable[2], be of great interest because of its potential of application in communication systems, specifically for audio compression of and video.

The discrete wavelet transform is described in section 2, in the section 3 illustrates the hardware architecture the implemented algorithms. Section 4 and 5 is shown the results and conclusions of the project.
2. Wavelet transform The Discrete Transform Wavelet

A wavelet function basic family can be generated by translation and dilation the mother wavelet that correspond the family [3]. The DWT coefficients can be obtained by taking the inner product between the input signal and the wavelet functions [4, 5].

2.1. Two Dimensions Wavelet Analysis Transform

The wavelet decomposition produces a family of organized hierarchically decompositions; it mean, a signal is decomposed into hierarchical set of approximations and details. From a point of view of analysis of signals, is signal decomposition in a family of analytical signals, which are usually an orthogonal function method. This paper uses the Discrete Wavelet Transform Two-Dimensional, which can be defined as:

\[ C(a, b) = \sum_{x \in \mathbb{Z}} \sum_{y \in \mathbb{Z}} f(x, y)g_{j,k}(x, y) \]

whit \( a = 2^j \), \( b = k2^j \), \( j \in \mathbb{N} \)

Where \( f \) it is the original image, \( g \) is the wavelet function, \( a \) is scale factor of the function, \( b \) is a location parameter of the wavelet to function, and \( C(a, b) \) is the set of obtained coefficients.

The inverse process is obtained by:

\[ f(x, y) = \sum_{j \in \mathbb{Z}} \sum_{k \in \mathbb{Z}} C(j, k)\psi_{j,k}(x, y) \]

Where \( \psi \) is the wavelet function used to reconstruct the image.

2.2. Process of Decomposition Two Dimensions Wavelet

An efficient way to implement the discrete wavelet transform is with the use filters developed by Mallat [7,8]. The Mallat algorithm, for the discrete wavelet transform (DWT) is in fact, a classical scheme in the signal processing community, known as a two subband channel coder or quadrature mirror filters (QMF). All the filters used in DWT are intimately related to the sequence \((W_n)_{n \in \mathbb{Z}}\), the sequence \((W_n)\) is finite and can be viewed as a filter. The filter \( W \), which is called the scaling filter (no normalized), is of Finite Impulse Response (FIR), length \( 2N \), of norm 1, and a low-pass filter [9]. The four filters are computed using the figure 1.

![Figure 1: Calculation of the four filters of Daubechies.](image)

Where \( \text{qmf} \) is such that \( Hi_R \) and \( Lo_R \) are quadrature mirror filters.
The wavelet transform 2-D is implemented using analysis filters a bank of 1-D lowpass \((L_0,D)\) and highpass \((H_1,D)\), as seen in Figure 2.

![Wavelet Transform Diagram](image)

**Figure 2**: Process to calculate the TWD in two dimensions.

The multiresolution representation carried out by the discrete wavelet transform Two-Dimensional, is the frequency spectrum fragment of image into a sub-band low-pass \(cA_j\) and a set of images high-pass with sub-band horizontal orientation \(cDH_j\), vertical orientation \(cDV_j\), diagonal orientation \(cDD_j\), \(j = 1, L\), where \(L\) denote the number of levels for a representation [6]. The sub-band \(cA_j\) contains the smooth information of the image, and the subbands \(cDH_j\), \(cDV_j\) and \(cDD_j\) contain the detail information of the image [10]. Figure 2 shows the implementation of a one-level \((L = 1)\). In Literature different types from families wavelet exist, among them are had: Haar, Daubechies (dbN), Symlets (symN), Meyer (meyr). In this work the Daubechis family was used order 2(db2) [11].

3. Architecture Hardware
Algorithm was used in a design methodology (Top Down), in which all the blocks are individually implemented and analyzed and then combining them into one system. In Figure 3, illustrates the general block diagrams of the digital hardware architecture implemented.

The complete system comprises a general control block that determines when each block is activated, thereby generating system monitoring and synchronization of each stage of design. Each design stage has its own control block to its internal functions, and executed in a serial process. The program was developed in VHDL (Very Hardware Description Language.) combining all the styles of description.

The size of the input image is transparent change image, and the input image is a vector of gray scale that is stored in the external memory to be processed, where positions depend the size of the input image with a width of 32 bits, as the external memory according to your specifications is organized in a width of 16 bits, the data is stored in two memory positions. The 32 bits to the IEEE754 representation of floating point binary data as it is necessary.
represent the obtained data by the image in a binary format. By such reason is implementing an additional block that is the charge to realize this conversion binary floating number [12]. Additionally is developed addition, subtraction and multiplication algorithms to floating point numbers represented in IEEE 754 format [13]-[14], because in the overall process using these operations.

Figure 3: Description of the hardware architecture implemented the discrete wavelet transform.

It performs three stages to obtain the decomposition algorithm for dwt, the etapa 2 and etapa 3 is performed in parallel form. To facilitate the process control and management implemented algorithms in terms of speed in processing time. Divided into:
This external RAM Micron 128Mbit M45W8MW16 organized as 8Mbytes x 16bits, integrated into the FPGA NEXYS 2, all the processed images are stored as vector; the acquired image is stored in the top position, after convoluted images of etapa_1 of convolution and finally the images obtained from the convolution etapa_2 and etapa_3, which are the images details of the input image and is performed in parallel. In internal RAM is performed a temporary storage of data in the device after the process of convolution (depending on the stage of convolution being processed). The data processed in floating numbers is store in the external memory.

The system has been mapped on the Nexys-2 is a powerful digital system design platform built around a Xilinx Spartan 3E FPGA. Distributed by Digilent [15]. The architecture was implemented using Xilinx ISE software, version 11.2, which provides several tools for design synthesis, techniques configuration, performance analysis, including resources, speed and power consumption.
4. Results
The implemented block of discrete wavelet transform of the Daubechies family of order two at a level of decomposition is shown in Table 1.

| Hardware Resources | Number of Slices | 3842 out of 8672 | 44.3% |
|--------------------|-----------------|------------------|-------|
| Number of Slices   | 1608 out of 17344 | 9.3%             |       |
| Number of Slices   | 6589 out of 17344 | 44.3%            |       |
| Number of Slices   | 10 out of 24     | 44.3%            |       |
| Clock Rate         | 50MHz%           |                   |       |

Given that this implementation has the conversion algorithms of data in IEEE754 format, in assessing the results of the hardware architecture implemented a graphical interface was developed in Matlab, which are loaded with images to be processed and sent to storage memory serially. The Figure 6 shows an original image used for processing.

![Original image to be processed.](image)

After applying the wavelet transform algorithm (for a single level of decomposition) to the original image on the FPGA, we obtained the decomposition shown in Figure 7. This decomposition is sent after performing the reverse process of the IEEE 754 format to Matlab, which compares the four images obtained by decomposition with dwt2 command and then perform the calculation of the Mean Square Error described thus:

\[
MSE_{cA} = \frac{1}{MN} \sum_{x=1}^{M} \sum_{y=1}^{N} [I[x, y] - I_1[x, y]]^2
\]  \hspace{1cm} (3)

\[
MSE_{cDH} = \frac{1}{MN} \sum_{x=1}^{M} \sum_{y=1}^{N} [I[x, y] - I_1[x, y]]^2
\]  \hspace{1cm} (4)
\[ MSE_{CDV} = \frac{1}{MN} \sum_{x=1}^{M} \sum_{y=1}^{N} [I[x, y] - I_1[x, y]]^2 \] (5)

\[ MSE_{CDD} = \frac{1}{MN} \sum_{x=1}^{M} \sum_{y=1}^{N} [I[x, y] - I_1[x, y]]^2 \] (6)

Where \( M, N \) are the height and width of the processed image, \( I[x, y] \) and \( I_1[x, y] \) is the matrices element of each digital image thrown by the command \textit{dwt2} and decomposition thrown by the FPGA at the pixel \([x, y]\), respectfully. Given to every detail of one \( MSE \) of the processed image:

\[ MSE_{cA} = 4.483e^{-16} \] (7)
\[ MSE_{cDH} = 3.258e^{-14} \] (8)
\[ MSE_{CDV} = 8.659e^{-17} \] (9)
\[ MSE_{CDD} = 5.785e^{-14} \] (10)

Figure 7: Result of applying the algorithm implemented in the FPGA on the image of Figure 5.
5. Conclusions
We developed a tool for digital image processing which used a transformation algorithm, which is implemented on a programmable logic device such as FPGA taking advantage processing speeds of these devices. The architecture was tested with images of different characteristics and each case presents the expected result.

This system can be used for applications where you needed to do multiresolution representations from hardware platforms. The implementation of TDW in FPGA reduces development time, thus inferring the processing time of a complete image stored in memory 256 x 256 pixels in 36 mseg with a working frequency of 50MHz.

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