Radiation hard pixel sensors using high-resistive wafers in a 150 nm CMOS processing line

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Abstract: Pixel sensors using 8″ CMOS processing technology have been designed and characterized offering the benefits of industrial sensor fabrication, including large wafers, high throughput and yield, as well as low cost. The pixel sensors are produced using a 150 nm CMOS technology offered by LFoundry in Avezzano. The technology provides multiple metal and polysilicon layers, as well as metal-insulator-metal capacitors that can be employed for AC-coupling and redistribution layers. Several prototypes were fabricated and are characterized with minimum ionizing particles before and after irradiation to fluences up to $1.1 \times 10^{15} \text{n}_{eq} \text{cm}^{-2}$. The CMOS-fabricated sensors perform equally well as standard pixel sensors in terms of noise and hit detection efficiency. AC-coupled sensors even reach 100% hit efficiency in a 3.2 GeV electron beam before irradiation.

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1 Introduction

Hybrid pixel detectors [1] have matured to a level that they are the main contenders for tracking and vertexing near the interaction point at experiments of the planned LHC upgrade (HL-LHC, [2]). The surface covered by pixel detectors will likely increase from less than 2 m$^2$ at present to 10–20 m$^2$ in the future. The detectors will be arranged in several concentric cylindrical layers, with radii between 3–30 cm, and many square meters of disk layers in the forward and backward region of the detectors.

Industrial CMOS processes on large, high-resistive wafers enable sensor designs with high yield and high throughput at comparatively low cost. This technology is therefore of interest also for large area pixel or strip detectors, not only for readout IC fabrication but also for the particle sensing elements, the sensors. Furthermore, various parts of the CMOS processing technology like multiple metal layers, polysilicon layers, as well as metal-insulator-metal (MIM) capacitors can be employed for special sensor features that are otherwise mostly not available. Examples are AC-coupling of the sensor to the readout electronics or obtaining a significant module simplification by implementation of redistribution layers for signals and service voltages on the sensor itself rendering a module flex much simpler or even obsolete. A redistribution of bump connections by a dedicated metal layer can decouple the sensor pixel pitch from the readout pixel pitch thus enabling a module design without elongated inter-gap pixels. As the CMOS sensors include no active electronic circuitry (transistors), they are termed passive CMOS sensors.

In this paper we present radiation hard passive CMOS pixel sensors fabricated in a 150 nm CMOS process offered by LFoundry [3] on high-resistive wafers (> 2 kΩ-cm). A number of prototypes have been characterized with respect to production quality, depletion depth, signal and noise levels, pixel capacitance, and detection efficiency before and after irradiation up to fluences of $1.1 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$. 

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2 Pixel sensor design

Prototype n-in-p pixel sensor matrices have been produced in the LFoudnry 150 nm CMOS process on Czochralski p-type wafers having a foundry specified resistivity of typically 4–5 kΩ-cm (minimum 2 kΩ-cm). The pixel matrix measures 1.8 × 4 mm$^2$ and is divided into 16 × 36 pixels with a size of 50 × 250 μm$^2$. The matrix is surrounded by an n-implantation bounding the active volume of the edge pixels, followed by seven p-implantation guard rings to isolate the electrodes from the high voltage at the sensor edge (figure 1). Half of the pixels are DC coupled with punch-through biasing and the other half is AC coupled by a 3.2 pF MIM capacitor. AC pixels are biased via a 15 MΩ polysilicon resistor present in each pixel. The pixel layout follows a standard planar pixel design used, for instance, for the ATLAS IBL planar sensors [4], with a 30 μm wide n-implantation as readout electrode and a 20 μm gap between pixels to all sides. For the two outermost columns of the DC half, the n-implantation width has been varied in the range between 15 μm and 30 μm, to allow for optimization studies of the fill factor with respect to input capacitance and charge-collection efficiency. All pixels are isolated by a 4 μm p-stop grid implemented below field plates made of a low resistive polysilicon layer. The intention of the field plates is to flatten spikes in the electric field occurring after irradiation, hence improving the breakdown behavior [5]. A high resolution mask set was used for processing as the submission was shared with other monolithic active CMOS devices (DMAPS [8]). The use of such (expensive) mask sets is likely not needed in a dedicated

Figure 1. Pixel sensor matrix with 576 pixels surrounded by an n-well ring and subsequently 7 p-type guard rings (top). The bottom shows 4 edge pixels with bump pads. (left) Pair of AC pixels with a large area fraction filled by MIM layers providing the capacitive coupling; (right) pair of DC pixels containing dedicated implants for punch through biasing (bias dots).
passive sensor production run. The sensors have been thinned to 100 µm and 300 µm and then backside processed providing a p-implant and a metallization layer to allow bias voltage application from the backside. The very thin 100 µm wafer was processed by IBS in France [6] including a thinning step in a TAIKO process [7]. In this process the wafer edge is left thicker to create a self-sustainable wafer for further processing without the need of a handling wafer.

3 Device assembly and characterization procedures

The sensor was bonded to the ATLAS FE-I4 pixel readout-chip [9] via fine pitch solder bump bonding at Fraunhofer IZM in Berlin [10]. The FE-I4 chip was tuned to threshold values similar to those used for the IBL layer of the ATLAS pixel detector corresponding to approximately 3000 e−. The chip was readout with the USBpix 2.0 hardware [11] in combination with pyBAR software, a Python based readout- and test-system for the ATLAS FE-I4 [12]. The FPGA firmware modules and interfaces were provided by basil, a modular data-acquisition and system-testing framework [13].

The sensor efficiencies were determined in several test-beam campaigns using minimum ionizing particles. Electrons were used with energies between 2.5 GeV and 3.2 GeV at the electron stretcher accelerator (ELSA) in Bonn [16] and 120 GeV pions at the super proton synchrotron (SPS) at CERN [17]. A fast particle telescope based on two ATLAS FE-I4 modules [18] was used for high-rate test-beams at ELSA to determine the detection and charge collection efficiencies for different bias and threshold settings with high statistics. A high resolution telescope (EUDET [19]) based on six Mimosa26 planes [20] and one FE-I4 hybrid pixel time-reference plane was used for the high-energy test-beam setup at CERN to map with sub-pixel resolution. The synchronization between data from FE-I4 telescope planes and Mimosa26 planes was established by means of the JUDITH software [21]. This synchronization is difficult and error prone, since the event integration time of the Mimosa planes is much longer than the integration time of the ATLAS FE-I4 (115 µs vs. 0.4 µs). A mismatch between tracks recorded in the Mimosa telescope with hits in the FE-I4 time reference plane assigns a wrong time stamp to these tracks during reconstruction. Every mismatched track artificially decreases the determined absolute efficiency. Consequently, the absolute efficiency quoted in this work was always determined with the FE-I4 based telescope, where synchronization issues due different event integration times do not exist.

The subsequent steps of a test-beam analysis involving hit clustering, track finding and fitting were carried out using testbeam analysis [22], a novel python package. The performance of testbeam analysis was verified by simulation as well as by analyzing test-beam data from well understood and formerly characterized ATLAS IBL pixel modules [18].

To determine the charge spectra of the sensor a new charge reconstruction method was developed (TDC method). This method overcomes the limitation of the front-end to measure charge spectra with sufficient resolution by sampling the charge signal with a faster external clock utilizing the FPGA of the readout system [23].

One sensor has been irradiated with 24 MeV protons at the Birmingham irradiation facility [14] in steps to $0.18 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ and $1.14 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$. After each step the sensor was annealed for 80 minutes at 60°C. The total fluence was measured with about 10% uncertainty by post-irradiation dosimetry on nickel foils attached to the device during irradiation [15].
4 Results

4.1 I-V curves

To examine the process- and design quality I-V curves (current versus reverse-bias voltage) of 114 sensors have been obtained. The sensors were located on one wafer half of a 300 µm thin wafer and were contacted at the bias grid by needles on a probe station. The curves in figure 2 (left) show very similar electrical characteristics for all sensors. The breakdown requires bias voltages in excess of 100 V for all 114 sensors and is independent of the sensor’s position on the wafer. Only one sensor showed a short due to a processing error. The location of the breakdown was determined via emission microscopy on 5 sensors of the same wafer after dicing and it occurs at the bias dots of the DC pixels. The right side of figure 2 depicts results of the IV measurements of two fully assembled

Figure 2. I-V measurements of LFoundry CMOS sensors: (left) I-V curves before irradiation and dicing of 114 sensors located on the same wafer thinned to 300 µm. One sensor suffering a short circuit due to a processing error has been excluded from the plot. (right) I-V curves of two pixel module assemblies. I-V measurements for two different thicknesses (100 µm (dark dashed line) and 300 µm (dark solid line) and two different irradiation levels (0.18 × 10^{15} n_{eq} cm^{-2} (dash-dotted line) and 1.14 × 10^{15} n_{eq} cm^{-2} (light solid line)) are shown. The light dashed line shows an unbonded test structure treated with plasma etching after backside grinding to mitigate the current increase at full depletion. The results are normalized to 20°C temperature.

pixel modules after thinning, backside processing, and solder bonding to the ATLAS FE-I4 chip. Backside processing after thinning included a p+ implantation plus metallization, but was done without an etching step after backside grinding. It has been observed before [24] that excessive leakage current can be mitigated by applying etching after grinding. The absence of this treatment is likely the cause for the observed behavior at 24 V for the 100 µm device (figure 2, arrow full depletion). At this voltage the depletion region reaches the backside, in agreement with calculations assuming a resistivity of about 5 kΩ-cm (see section 4.3). In order to prove this hypothesis a dedicated test structure with the same pixel pitch, guard rings, and implantations was designed and thinned to 100 µm and the backside was treated with plasma etching. It can be seen in figure 2 (test structure) that the additional current increase is not occurring anymore when the depletion zone touches the backside. The additional current increase at about 160–180 V for the unirradiated 100 µm and 300 µm is likely a breakdown at the bias dots of the DC pixels. After irradiation of the
sensor assembly the breakdown voltage increases. At an irradiation level of $1.14 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$ voltages in excess of 700 V have been applied without observing any breakdown.

### 4.2 Signal and noise

Figure 3 (left) shows single pixel charge distributions of the 300 $\mu$m thick sensor obtained in test-beams (3.2 GeV electrons) before irradiation at 160 V bias and after $0.18 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$ at 250 V. A similar measurement at the highest fluence of $1.14 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$ suffered an electric discharge disabling the FE-I4 readout chip functionality, and is thus not available.

![Figure 3](image)

**Figure 3.** Signal and noise for a 300 $\mu$m thick LFoundry passive pixel sensor at 160 V bias bump bonded to the ATLAS FE-I4. (left) Measured charge distributions (normalized) of single hit clusters of 3.2 GeV electrons before irradiation and after $0.18 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$. The charge was measured using the TDC method (see text) and fitted with a Landau-Gauss convolution to determine its MPV. (right) The equivalent noise charge distributions for AC (dark) and DC (light) coupled pixels. The mean noise for these coupleings is stated in the legend.

Figure 3 (right) shows distributions of the noise for AC and DC coupled pixels determined using the internal charge injection circuitry of the ATLAS FE-I4 when a 300 $\mu$m sensor at 160 V bias is attached. The distributions have mean values of $\text{ENC} = 117 e^{-}$ (DC) and $132 e^{-}$ (AC). This should be compared to the noise performance of planar IBL sensors ($\text{ENC} \approx 120 e^{-}$ [18], $C_D = 117 \text{fF}$ [25]) and IBL 3D-Si sensors ($\text{ENC} \approx 140 e^{-}$ [18], $C_D = 180 \text{fF}$ [25]) showing that the noise performance of the passive CMOS sensor investigated here is comparable. Hence we conclude that the DC coupled pixels have an input capacitance less than 120 fF and the AC coupled pixel less than 180 fF. The larger value for the AC coupled sensors arises from the parasitic capacitance of the polysilicon layer by which the bias resistor is implemented. The values for the bias resistor and coupling capacitance were not optimized in the design, but chosen as large as possible, leaving room for input capacitance optimization in future designs.

### 4.3 Depletion depth

Assuming that in silicon a minimum ionizing particle creates about 71 e/h pairs per micron (most probable value, from GEANT4 simulation) and that only the depleted volume of the sensor contributes to the charge signal (due to the fast response time of the FE-I4) we determine the depletion
depth and thus the p-type bulk resistivity of the passive CMOS sensors using

\[
d = \sqrt{\frac{2e_0\epsilon_r}{eN_{eff}} (V_{bi} + V_{bias})} \quad \Rightarrow \quad d [\mu m] \approx 0.3 \sqrt{\rho [\Omega \cdot cm] \cdot V_{bias} [V]}
\]  \tag{4.1}

where \(d\) is the depletion depth, \(N_{eff}\) the effective doping concentration, \(\epsilon_0\) the vacuum permittivity and \(\epsilon_r\) the relative permittivity of silicon.

Figure 4 shows the measured depletion depth assuming 71 e/h pairs created per micron using the most probable value of measured charge distributions as in figure 3 (left) extracted by a fit to a so-called Langau distribution [26], a Landau distribution [27] folded with a Gaussian. The measured depletion depths at different bias voltages are compared to theoretical curves obtained from (4.1) assuming three different values for the (p-type) bulk resistivity. The error bars of the measurements are defined by the fit error and the uncertainty of the calibration of the charge-injection circuitry of the ATLAS FE-I4. One can conclude that the resistivity of the bulk material of the measured wafer is at least 4–5 k\(\Omega\)-cm, a value compatible with the range quoted by the vendor.

4.4 Hit detection efficiency

The hit detection efficiency has been determined using 3.2 GeV electrons for sensors thinned to 100 \(\mu\)m (unirradiated) and 300 \(\mu\)m (three levels of radiation: 0, \(0.18 \times 10^{15}\) \(n_{eq}\) cm\(^{-2}\) and \(1.14 \times 10^{15}\) \(n_{eq}\) cm\(^{-2}\)). The results are shown in figure 5. The hit efficiency reaches values of 98.7%/99.8% for the DC/AC coupled 100 \(\mu\)m sensor pixels at a standard threshold of about 3000 electrons and increases to 99.8%/> 99.9% after reducing the threshold to about 1500 electrons. After irradiation the efficiency reaches values > 99.9% for AC coupled sensors at bias
Figure 5. Hit detection efficiency of 100/300 µm thick pixel sensors for different bias voltages and different levels of radiation damage. Each point represents the mean efficiency of at least 50 center pixels. The statistical error bars are too small to visualize and are thus not shown.

Figure 6. Hit detection efficiency map of the LFoundry passive pixel sensor with 300 µm thickness at 160 V bias. Bins of 10 µm x 10 µm size have been used and are labeled by a white color where the efficiency determination is not possible due to low statistics. The efficiency is not correct on an absolute scale (see section 3), but shows the efficiency loss at the location of the bias dots. The upper left inefficient area are two disabled pixels during analysis and the inefficient area to the right marks the edge of the active sensor area.

Voltages above 350 V. The DC coupled sensor efficiency is somewhat lower (> 99% at 450 V) due to the ‘blind’ area taken by the punch-through biasing dot. This effect can be seen in figure 6, showing the efficiency map over all pixels determined with 120 GeV pions. The map depicts a histogram with 10 µm x 10 µm bins of the intersection points of reconstructed particles tracks with
the sensor. The ratio of tracks that created a hit in the sensor, within an association distance of 500 µm, divided by the total number of tracks gives the efficiency per bin. While the efficiency of the AC coupled pixels is homogenous, it is possible to observe an efficiency loss at the bias dots located in the DC coupled pixels. The absolute efficiency is underestimated (see section 3) explaining a lower efficiency in comparison to figure 5.

### 5 Conclusions

In this paper we presented pixel sensors fabricated in a CMOS process line using high ohmic (∼5kΩ-cm) substrate wafers. Employing CMOS technology provides several benefits for large area pixel detectors such as those planned for the HL-LHC upgrade at CERN, namely: low cost, large through-put production on 8″ or even 12″ wafers, and design flexibility (e.g. AC coupling, routing) while keeping the charge collection properties of standard sensors. The wafers were fabricated using LFoundry 150 nm technology. The sensors were thinned to 300 µm and 100 µm thickness and were backside processed. A sensor breakdown after irradiation to more than $10^{15}$ n$\text{eq}$ cm$^{-2}$ did not occur up to a maximum applied voltage of 700 V. Measured signal and noise performance was found to be very similar to those of planar pixel sensors currently used in the ATLAS experiment. The hit-efficiency after irradiation was measured in an electron test-beam to be above 99.9% (99.1%) for AC- (DC)-coupled sensor-chip assemblies.

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