GATSPI: GPU Accelerated Gate-Level Simulation for Power Improvement

Yanqing Zhang, Haoxing Ren, Akshay Sridharan, Brucek Khailany
NVIDIA Corporation
{yanqingz, haoxingr, asridharan, bkhailany}@nvidia.com

Abstract
In this paper, we present GATSPI, a novel GPU accelerated logic gate simulator that enables ultra-fast power estimation for industry-sized ASIC designs with millions of gates. GATSPI is written in PyTorch with custom CUDA kernels for ease of coding and maintainability. It achieves simulation kernel speedup of up to 1668X on a single-GPU system and up to 7412X on a multiple-GPU system when compared to a commercial gate-level simulator running on a single CPU core. GATSPI supports a range of simple to complex cell types from an industry standard cell library and SDF conditional delay statements without requiring prior calibration runs and produces industry-standard SAIF files from delay-aware gate-level simulation. Finally, we deploy GATSPI in a glitch-optimization flow, achieving a 1.4% power saving with a 449X speedup in turnaround time compared to a similar flow using a commercial simulator.

1 Introduction
Gate-level logic simulation plays an important role in the design and signoff of integrated circuits. Simulation is used in many steps such as power analysis, design-for-test (DFT) pattern generation, DFT power analysis, and fault simulation. However, gate-level simulation, and especially delay-accurate glitch-enabled simulation for power estimation, can exhibit long runtimes on conventional simulators, prohibiting its widespread adoption in chip design flows. Today's highly complex SoCs have hundreds of partitions, each with millions of gates and numerous testbenches running for thousands of cycles to simulate. Accurate results can take many hours to days across hundreds of servers to produce. Thus, there is a desire to accelerate this simulation task. Faster alternatives such as probability-based switching activity estimators can also produce toggle counts/rates for power purposes, but they are inaccurate. Typically, when running delay-aware and glitch-enabled gate-level simulation, correct waveforms of sequential elements are already known in advance from previous RTL simulation results, automatic test pattern generation (ATPG) vectors, or scan test. These cases, where the input stimuli to the logic cones in the digital design from primary inputs and pseudo-primary inputs (register and RAM outputs) are known, have been called logic ‘re’-simulation[1] (Fig. 1(Left)). Logic re-simulation is beneficial for turnaround time, since a re-simulator can forego functional simulation of the sequential elements. What’s more, in re-simulation, the known sequential element waveforms break the cycle-to-cycle dependency so that multiple cycles of the testbench can be simulated in parallel. Modern day parallel computing architectures, such as GPUs, provide an opportunity for speedups[2–7] through parallelization across cycles (stimuli) as well as the design (gates within the same logic level can be simulated in parallel), as depicted in Fig. 1(Right).

However, GPUs also present challenges to re-simulation acceleration, such as the development cost for writing and maintaining a separate code base in GPU programming languages such as CUDA. Other challenges include minimizing the communication overhead between host and device (CPU and GPU), efficient scheduling, and avoiding memory bandwidth bottlenecks to keep the Streaming Multiprocessors (SMs) occupied with sufficient data. Fortunately, newer GPUs have features that help overcome these challenges, most notably plentiful memory bandwidth and expanded GPU memory capacity that rivals some system memory capacities (Table 1).

In addition, the emergence of deep learning (DL) has helped foster a rich software ecosystem for programming GPUs. Popular DL frameworks such as PyTorch[10] lower the barrier for developing GPU code that operates efficiently on matrices and tensors. Graph learning packages such as DGL[11], built on top of PyTorch, provide APIs for various graph algorithms and partitioning methods. Since digital logic circuits can be naturally represented as graphs, these frameworks can be exploited for productive GPU programming on logic re-simulation and other related tasks.

In this work, we build upon these recent developments in GPU software and hardware platforms with a new GPU-accelerated gate-level re-simulator called GATSPI (which stands for GPU Accelerated GaTe-level Simulation for Power Improvement). The novel contributions of this work are:
- GATSPI achieves up to 1668X re-simulation kernel speedup on a single A100 GPU and up to 7412X on 8 V100 GPUs when compared to a commercial simulator across a diverse set of industry benchmarks with no accuracy loss. It also achieves up to 680X speedup when considering end-to-end application tasks, such as waveform loading and writing results to file.
- To the best of our knowledge, GATSPI is the first GPU accelerated re-simulator that supports full logic cell types, all SDF conditional delay statements, multiple-simultaneous-input (MSI)
switching resolution, and inertial delay filtering on both gates and intersect and interconnect—without need for calibration runs.

- For ease of coding, GATSPI is novely implemented in PyTorch, DGL, and with only 2 PyTorch custom CUDA kernels.
- Through GPU profiling, we show analysis for ‘hyperparameter’ tuning (amount of cycle-level parallelism, registers/thread, threads/block) for the GATSPI kernels.
- We deploy GATSPI in a glitch-optimization flow, achieving a 1.4% power saving with a 449X speedup in turnarounds compared to a similar flow using a commercial CPU-based simulator.

2 Related Work

Prior work has explored GPU accelerated gate-level simulation. Early efforts explored a mostly oblivious simulator approach, evaluating every gate at every cycle or timestamp regardless of input activity [4, 5]. These oblivious simulators are computationally inefficient at low activity factors, and require massive amounts of memory to log every gate at every timestamp, achieving 2-45X simulation kernel (only actual simulation runtime is measured) speedup [4, 5]. Another approach used an event-based simulator approach and a sophisticated memory paging technique to perform re-simulation for 1-270X speedup [3]. Event-based simulation only performs evaluation on specific gates when changes on their inputs occur. As stated in [3], the speedups depend on the activity factor of the testbench.

The best ‘class’ of GPU accelerated re-simulators have been hybrid event/oblivious simulators [2, 6, 7]. The general idea of hybrid approaches is that each gate’s simulation advances in time based on events on its inputs, but the scheduling and launching of threads on the GPU for each gate is oblivious. Each gate will always have a simulation thread assigned to it, and threads whose gate has little or no activity simply finish earlier. One recent work implemented such an approach on industry-sized designs with multi-millions of gates and achieved 23-44X speedup on end-to-end application runtimes (measured from loading the testbench waveforms until result file dumping) [6]. Holst et al. implemented a hybrid 2-value re-simulator with a novel memory management scheme which requires calibration loops, and they achieved large simulation kernel speedups of 21-1090X for long-duration scan testbenches on experimental(<550k 2-input only gates) circuits [2]. Another recent work implemented a 4-value re-simulator that achieved 2-44X application speedup on the ICCAD 2020 Design Contest [1] benchmarks [7]. The contest[1] asks for an implementation of transport delays instead of inertial delays, and [7] cleverly used this deviation in gate delay processing to implement another degree of parallelism—event parallelism. They simulate each intra-cycle event in parallel. This is unique to transport delay processing because there is no pulse filtering, so same-value output events and delay collision events can be invalidated after the parallel simulation of individual events is completed.

These hybrid simulators typically partition the design netlist by logic level, which is a convenient and straightforward way to access design parallelism [2, 7], and GATSPI similarly adopts this approach. Simulation only advances to the next logic level partition if the current level has completed, which ensures input/output waveform dependencies are always met. In comparison to [2, 3], GATSPI aims to use the expanded memory capabilities of newer GPUs without memory management schemes. Similar to [2], GATSPI implements 2-value re-simulation, since gate re-simulation for power analysis scarcely produce x/z values. However, [2] only supports 2-input gates, whereas GATSPI supports all boolean logic gate types and conditional SDF delay statements. These features are important for targeting industry-standard libraries. In contrast to [7], GATSPI processes inertial delays. While simpler to implement, transport delay processing will lead to overestimates of glitches, the inaccuracy of which is not conducive in power analysis settings.

Finally, similar to DREAMPlace [12], GATSPI leverages DL framework software packages such as PyTorch and DGL along with several custom CUDA kernels to ease the software development and maintenance effort.

3 GATSPI Implementation

Fig. 2 shows the overall application workflow of GATSPI compared to a commercial simulator flow. Our starting points are a gate-level netlist, corresponding SDF file, and primary/pseudo-primary input waveforms.

We employ the same waveform format as [2] for efficient storage, shown in Fig. 3. We use a Python script to translate SDF delay statements and logic function truth tables into the array format described in Fig. 4. We translate the netlist into a PyTorch/DGL graph object in a manner similar to [13]. The DGL graph object retains netlist information such as connectivity, gate and interconnect delays (edge features), and cell logic function (node feature) by using DGL’s graph node/edge attribute annotation. Finally, GATSPI loads the DGL graph object and input array waveforms, performs logic levelization, and launches the CUDA kernels to complete simulation. The resulting SAIF file for downstream power analysis or other applications can be dumped asynchronously as the CUDA kernels are running [7].

Fig. 5 provides an overview of GATSPI’s simulation approach. It first loads the input waveforms and pre-allocates one chunk of device memory for storing all the waveforms of the simulation. For example, when using an NVIDIA V100 GPU with 32GB device

Figure 2: Overview of tool flow for commercial tools and GATSPI.

Figure 3: Array format of signals in GATSPI taken from [2].
Algorithm 1: Per-gate, per-cycle parallelism re-simulation

1. **Input**: 1-D array of all waveforms allW. Number of pins n.
2. **Output**: Output waveforms stored in allW.
3. For each i: allW[p_i] = -1 ? p_i + +: null /* initial value */
4. colInd = \sum_{i=1}^{n} (p_i \% 2) * 2^{i-1} /* % is the modulo operator */
y = Y[colInd]
5. y == 0 ? allW[p_0] = 0: (allW[p_0] = -1; allW[p_0 + +] = 0)
6. while t_{i!} = EOW do
7. t_{i} = EOW /* EOW is INT_MAX(Fig. 3) */
8. for each i do
9. netDelay = (p_i \% 2) * \delta^f \cdot \delta^r
10. if allW[p_i + 2] = netDelay - allW[p_i + 1] < 0 then
11. p_{i-+} = 2; continue
12. t_{i} = min(t_{i}, allW[p_i + 1] + netDelay)
13. if t_{i!} = EOW then
14. for each i do
15. if transition time of pin i == t_{i} then
16. p_{i} + +
17. update colInd; update y; set gateDelay indexing \delta_i using p_i \% 2 and colInd
18. if y_! = p_0 \% 2 then
19. t_0 = t_i + gateDelay
20. if t_0 - allW[p_0] < gateDelay then
21. p_0 =
22. else
23. p_0 + +
24. allW[p_0] = t_0

GATSPI is conveniently written in PyTorch and DGL, which has many advantages. Many issues such as indexing of multi-dimension arrays are made convenient through PyTorch, and graph netlist manipulation is made convenient through DGL. Only the re-simulation kernels of Algo. 1 are written in CUDA, integrated as custom PyTorch CUDA calls. Each thread in the kernel simulates one independent cycle/stimuli of one gate in the current logic level. Algo. 1 implements a delay-aware algorithm for logic gate simulation with inertial delay filtering on both gates and wire interconnect, processing of conditional SDF delay statements, and MSI switching resolution.

Algo. 1 describes the second iteration of re-simulation in GATSPI where the TC values are known and the output waveforms are to be stored in memory. The first iteration’s algorithm is very similar. After resolving the gate’s initial value, lines 8-13 determine the truth of the delay according to the truth table.
timestamp of the next earliest input transition to process. Of note, lines 10-12 perform interconnect inertial delay filtering. Also of note, lines 8-13 only determine the next timestamp, not which pin is switching. This is because lines 14-18 loop through all input pins to find all MSI switching conditions, and resolve them before updating gate output value $y$ and $gateDelay$. Algo. 1 will only trigger its inertial delay filtering logic (lines 21-25) if a change on output value $y$ is detected (line 19). Algo. 1 assumes a simulation constraint of $PATHPULSEPERCENT=100$. Other constraint values can be easily implemented by editing line 21.

We followed the CUDA tuning principles outlined in [15] where possible during implementation of GATSPI's CUDA kernels. As a result, we make use of asynchronous memory copy and we pin the pointer variables $p_g$ and $p_t$ to registers for 2% kernel speedup compared to kernel performance prior to tuning.

4 Experiments and Results

We perform GPU accelerated gate simulation with GATSPI on the benchmarks listed in Table 2. Benchmarks were chosen to provide diversity in design netlist size/structure, testbench activity factor, and simulation length. Of note, many benchmarks are chosen from industrial-scale designs with millions of gates and testbenches from power windows that informed power signoff for tapeout. We compare GATSPI’s execution time against the baseline of a commercial simulator, which is a commonly used baseline [1, 2, 6, 7]. Both application runtime[6, 7](i.e. contents of Fig. 5) and simulation kernel runtime[2](i.e. contents of Algo. 1) is compared. Simulation correctness is verified in two ways: the resulting SAIF files are compared, and ‘spot-checks’ of full waveforms of some random signals are compared for each benchmark between baseline and GATSPI. All GATSPI experiments in Table 2 were performed on a system with a 32 GB NVIDIA Quadro GV100 and 30 GB system memory. Cycle-parallelism is set to 32 (32 independent cycles are re-simulated in parallel). Baseline experiments with a commercial simulator were performed on an Intel Xeon single E5@2.70GHz CPU core with 64 GB system memory. Re-simulation is implemented in the commercial tool by making use of the force keyword of SystemVerilog.

Table 2 also reports the activity factor of each benchmark. Hybrid simulators on GPUs tend to have a maximum throughput measured in total events simulated/second, so including the activity factor metric provides a clearer assessment of throughput achieved. GATSPI achieves 28-1198X simulation kernel speedup, or 5-680X application speedup across a diverse set of design size, testbench activity factor, and testbench lengths. The application overheads, such as re-structuring the input waveforms to match the cycle-parallelism schema and dumping the result file, take up most of the application runtime. Unsurprisingly, largest speedups are achieved for long durations of high activity, since more time is spent within the re-simulation kernels, and simulation speedup is not hurt as much by Amdahl’s law. Though not experienced in our benchmarks, in cases where the number of re-simulation events to be stored in device memory surpass its capacity, the testbench can be compiled into shorter segments, GATSPI can be invoked several times in sequence, and dump files can be combined to achieve the full simulation results.

We also evaluate GATSPI in a multi-threaded CPU environment by modifying GATSPI’s code to support an equivalent OpenMP implementation. For brevity, we choose a few typical representative benchmarks to perform these experiments on (Table 3). We consider the three listed benchmarks as representative: a small design whose workload barely saturates the max thread count on our GPU platform, an industrial design with long testbench but low activity and highly unbalanced workload between different gate instances/threads, and an industrial design with long testbench and relatively high activity and somewhat balanced workload between different gate instances/threads. Similarly, we compare GATSPI against a commercial simulator’s multi-threaded CPU implementation (Table 4) running on Intel Xeon E5 CPUs in a server farm. In this case, benchmarks are chosen because they did not segfault. GATSPI substantially outperforms both scenarios.

Finally, to demonstrate the utility of GATSPI in a VLSI optimization flow, we incorporated GATSPI into a glitch-power-reduction tool flow on an industry design. We first re-simulated a 1.3M gate design to attain its activity. Custom scripts then perform glitch activity/design analysis before designer-informed glitch-fixing transformations are made to the netlist. Often glitch fixes at one testbench can lead to power changes in other testbenches. The updated netlist is then re-simulated to assess power savings. GATSPI reduced the turnaround time of re-simulation from 1459.6 minutes to 3.25 minutes, a 449X speedup, confirming the 1.4% design (1% whole chip) power savings. Such fast turnaround times can improve chip designers’ productivity and enable future automation. Furthermore, GATSPI’s fast simulation throughput can enable efficient mass simulation data collection for other use cases requiring accurate delay-annotated gate simulation. Examples may include crosstalk analysis, IR drop analysis, power-aware logic synthesis, or DFT.

5 GPU Profiling and Analysis

GPU Profiling — We used NVIDIA’s Nsight [17] to profile the GATSPI full application and simulation kernel to provide insight into achieved performance and identify areas of possible improvement. We again used the 3 representative benchmarks for brevity in our analysis experiments. Table 5 shows the results of application profiling, which reveal that data loading from host to device is not a major contributor to overall application runtime. Most of the initialization stage of GATSPI is spent re-structuring the input waveforms’ format, needed for exploiting cycle parallelism. There is also a static cost for stream synchronization and kernel launch time based on the logic level structure of the netlist, determined by the logic level partitioning.

Table 6 shows kernel profiling results for the second GATSPI CUDA kernel where output waveforms are stored in memory, and for the widest logic level in the design. Several bottlenecks can be identified. First, Algo. 1 contains many loops and memory access is highly irregular. Though high memory bandwidth is beneficial, compute throughput is restricted by waiting for memory responses (low L2 Hit Rate, high Cycle per Issue). Memory throughput is restricted by the algorithm fetching singular data (the next transition timestamp on each non-consecutively stored input pin waveform), as evidenced by uncoalesced memory accesses.

Kernel profiling also informs GPU application ‘hyperparameter’ tuning—in the case of GATSPI, these parameters include: amount of cycle parallelism, threads/block, and registers/thread. For reasons we explain below, we chose a configuration of [32,512,64] for
Table 2: Benchmarks and results on V100. Industry designs in grey. Open source benchmarks from [16]. Speedups in parentheses.

| Design (Configuration) | Testbench | Gate Count | Activity Factor | Cycles | OpenMP Kernel Runtime(s) | Baseline App. Runtime(s) | Baseline Re-sim. Kernel Runtime(s) | GATSPI App. Runtime(s) | GATSPI Re-sim. Kernel Runtime(s) |
|------------------------|-----------|------------|----------------|--------|--------------------------|--------------------------|-------------------------------|---------------------|-------------------------------|
| Industry Design A      | functional 1 | 7.7k | 0.094 | 9.4k | 670 | 635 | 4.05 (165X) | 0.79 (808X) |
| Industry Design B      | functional 2 | 2M | 0.013 | 78k | 16060 | 14924 | 41.76 (385X) | 14.55 (1026X) |
| Industry Design B      | high activity long test | 2M | 0.183 | 32k | 49230 | 46617 | 72.35 (680X) | 18.27 (40X) |
| Industry Design C      | functional 2 | 1.9M | 0.015 | 32k | 6224 | 5065 | 38.91 (160X) | 5.91 (160X) |
| Industry Design D      | functional 3 | 2.3M | 0.024 | 62k | 10638 | 8896 | 68.12 (156X) | 180 (116) |

Table 3: GATSPI comparison to its OpenMP implementation. Speedups vs. OpenMP in parentheses.

| Design(Testbench) | GATSPI Kernel Runtime (s) | OpenMP Kernel Runtime (s) | # CPUs Used |
|-------------------|---------------------------|---------------------------|-------------|
| Design A(func. 1) | 0.79(12.8X)               | 10.10                     | 32          |
| Design B(func. 2) | 14.55(9.4X)               | 136.09                    | 40          |
| Design B(high activity) | 38.90(14.4X)            | 558.94                    | 64          |

Table 4: GATSPI comparison to multi-threaded commercial tool. Speedups vs multi-threaded tool version in parentheses.

| Design(Testbench) | GATSPI App. Runtime (s) | Baseline App. Runtime (s) | Multi-thread Runtime (s) |
|-------------------|-------------------------|---------------------------|--------------------------|
| Design A(func. 1) | 4.05(63.7X)             | 670                       | 258                      |
| NVDLA_m(large)    | 18.27(50.0X)            | 3211                      | 914                      |

Table 5: Nsight profiling of application runtime, in units of seconds.

| Design(Testbench) | Host to Device Data Transfer | Stream Synchronize + Kernel Launch | Kernel Execution |
|-------------------|------------------------------|----------------------------------|------------------|
| Design A(func. 1) | 0.68                         | 0.24                             | 0.52             |
| Design B(func. 2) | 3.40                         | 3.50                             | 10.80            |
| Design B(high activity) | 7.82                         | 3.50                             | 31.34            |

parameters (Cycle parallelism, threads/block, registers/thread) to optimize GATSPI runtime.

For cycle parallelism, we undoubtedly wish to set this parameter to at least 32. There are 32 threads to a warp on the GPU, and instructions are issued per warp. So, setting cycle parallelism to a multiple of 32 causes each warp to simulate one gate instance, which helps limit code divergence. We may assume the greater the cycle parallelism, the faster the runtime, but Table 6 reveals otherwise. In the case where the design is small, initially higher cycle parallelism lowers latency. But, eventually the L2 reaches capacity, and its hit rate decreases leading to longer stalls and increased latency. In the more typical case of large industrial-scale designs, higher cycle parallelism leads to denser issuing of memory instructions that memory cannot fully keep up with, which drastically lowers memory throughput, leading to increased latency. GATSPI sets cycle parallelism to 32, sacrificing some flexibility for robust behavior.

A CUDA block is a programming abstraction that represents a group of threads. Typically, a low threads/block setting will incur more natural barrier synchronizations that lead to higher latency, while too high threads/block invites higher communication overhead between threads within the block. In Fig. 4 to implement GATSPI with partial SDF capabilities. Table 7 assesses the overheads incurred from these key functional features, which is 5-13% of total kernel runtime. Thus, it is a good tradeoff to include these features considering the accuracy requirements of industrial-grade power analysis.

Table 8 shows GATSPI performance across different NVIDIA GPUs, an A100 and a T4. Using a single GPU on an NVIDIA DGX Station A100 (with 40 GB memory), we find that A100 provides a 1.2-1.5X speedup over V100, scaling some benchmarks by more than the increase in SM count, likely due to larger increases in memory bandwidth and L2 cache size (Table 6 shows L2 hit rate is low). This is beneficial for industry-sized benchmarks, especially as designs become larger and testbenches more numerous, since these benchmarks are able to take advantage of memory capability improvements. When scaling down to lower-cost GPUs (benchmarking on an NVIDIA T4 in an AWS g4dn.xlarge instance[1]), we find that GATSPI runs 4.2-6.7X slower on a T4 than a V100. The NVDLA(large),scan results show a 4.2X slowdown, exhibiting similar scaling to typical deep learning performance benchmarks[18]. The Design B experiments slow down more because they require multiple sequential invocations of GATSPI—the full testbench waveforms did not fit in device memory.

Lastly, we benchmark performance of GATSPI in multi-GPU systems. We chose to implement a simple workload distribution strategy by distributing cycle parallelism across the GPUs. Namely, cycle parallelism is set to 32n, where n is number of GPUs, and each GPU is responsible for simulating 32 independent cycles in
Table 6: Nsight profiling of re-simulation kernel on V100. Throughput % numbers relative to maximum capability of GPU. Memory Throughput % is a compound metric encasing L1, L2, and Global memory performance.

| Design/Testbench | Config. (Cycle, parallelism, threads/block, reg$$/thread) | Threads | Compute/ Memory Throughput (%) | Occupancy (%) | Global Memory Throughput (GB/s) | L1/L2 Hit Rate (%) | Cycles per Scheduler Issue | Ultraaccelerated Memory Accesses (%) | Elapsed GPU Cycles | Latency (ms) |
|------------------|----------------------------------------------------------|---------|---------------------------------|---------------|---------------------------------|--------------------|--------------------------|------------------------------------|-----------------|-------------|
| Design A (func. 1) | 32,512,64 | 170k | 10.4/12.1 | 28.8 | 7.0 | 92.4/94.4 | 2.4 | 48 | 6.6M | 6.00 |
| Design A (func. 1) | 128,512,64 | 680k | 32.7/32.9 | 38.7 | 28.5 | 94.8/87.6 | 2.0 | 18 | 3.3M | 3.28 |
| Design A (func. 1) | 256,512,64 | 1.36M | 44.5/46.1 | 41.8 | 39.5 | 96.2/82.0 | 2.0 | 12 | 3.8M | 3.29 |
| Design B (func. 2) | 32,512,64 | 4.1M | 33.8/44.6 | 42.9 | 44.2 | 91.5/60.0 | 2.8 | 23 | 380.7M | 357.56 |
| Design B (high activity) | 32,512,64 | 4.1M | 28.4/38.4 | 48.0 | 281.1 | 84.5/47.0 | 3.5 | 41 | 788.3M | 696.36 |
| Design B (high activity) | 64,512,64 | 8.2M | 33.1/40.8 | 48.3 | 241.4 | 86.8/52.4 | 3.0 | 23 | 871.6M | 772.96 |
| Design B (high activity) | 128,512,64 | 16.3M | 39.5/47.1 | 48.8 | 158.1 | 90.9/55.7 | 2.6 | 12 | 1.1B | 993.69 |
| Design B (high activity) | 32,1024,64 | 4.1M | 27.6/37.1 | 49.8 | 270.8 | 87.1/49.9 | 3.5 | 52 | 878.8M | 776.85 |
| Design B (high activity) | 32,512,32 | 4.1M | 15.4/46.1 | 94.4 | 402.8 | 68.1/52.2 | 6.4 | 42 | 1.5B | 1350.00 |

Table 7: Kernel runtimes (s) and speedups without key features.

| Design/Testbench | Full Features | No Net Delay | No Net Delay + No Full SDF |
|------------------|---------------|--------------|---------------------------|
| Design A (func. 1) | 0.79(808X) | 0.79(808X) | 0.70(907X) |
| Design B (func. 2) | 14.55(1026X) | 14.19(1052X) | 13.80(1081X) |
| Design B (high activity) | 38.90(1198X) | 36.03(1294X) | 33.65(1385X) |

Table 8: Kernel runtimes (s) and speedups for different GPUs.

| Design/Testbench | T4 | V100 | A100 |
|------------------|----|------|------|
| NVDA.large(scan) | 42.53(60X) | 9.99(254X) | 6.59(385X) |
| Design B (func. 2) | 76.56(195X) | 14.55(1026X) | 12.11(1232X) |
| Design B (high activity) | 320.15(179X) | 38.90(1198X) | 36.03(1294X) |
| Design B (high activity) | 64,512,64 | 128,512,64 | 32,512,32 |

6 Conclusions and Future Work

In this paper, we presented GATSPI, a novel PyTorch-written GPU accelerated logic gate re-simulator that enables ultra-fast power estimation (28-1198X kernel speedup, 5-680X application speedup) across a diverse set of benchmarks. Re-simulation results match a commercial simulator baseline for accuracy, an important criteria in industry power analysis use cases. GATSPI incorporates important re-simulator functional features such as support for a wide range of cell types, SDF statements, and inertial delay filtering. With no calibration, GATSPI exhibits robust runtimes across benchmarks. These advantages motivate GATSPI to be deployed in real-world applications such as glitch-optimization loops, where we demonstrate 1.4% power savings with 449X speedup.

Our analysis provides insight and opportunities for future work. Inclusion of sequential element simulation can be explored to see if full logic simulation could provide similar acceleration potential. Memory management techniques can be incorporated to alleviate memory pressure for further scaling. Optimizations to exploit design parallelism, such as more sophisticated netlist partitioning techniques may help benchmarks with unbalanced activity workloads [19] and shift GPU accelerated simulation more towards the event-based paradigm. Finally, GATSPI’s ultra-fast speeds open the door for exploration of its usefulness in additional applications, such as crosstalk analysis, IR drop analysis, and fault simulation. GATSPI could also be a valuable tool in the development of GPU-accelerated AI-assisted EDA algorithms.

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