GaAs diode structures with n+-p junction on Ge/Si templates

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Abstract. GaAs layers were grown by metalorganic epitaxy on Ge/Si(001) substrates, which
were formed by chemical vapor deposition with decomposition of GeH₄ on a hot wire. High
structural quality of thin Ge layers (0.2 - 0.3 µm) on a silicon substrate made it possible to
grow high-quality GaAs layers. The resulting n'-GaAs/p-GaAs/p-Ge/p'-Si diode structures
demonstrate low reverse currents.

1. Introduction

The growth of epitaxial layers of germanium on silicon substrates has recently attracted great attention
of researchers with regard to their potential use in photonics and electronics devices [1-3]. It is
especially important that Ge technology is compatible with Si technology, and Ge can be used in
standard technological procedures for silicon for manufacturing of device structures. In addition, Ge-
on-Si substrates show great potential as templates for growing epitaxial A3B5 layers since Ge has a
lattice constant close to that of GaAs [4].

However, obtaining germanium layers on silicon is complicated by a large mismatch between the
constants of Ge and Si lattices (about 4%). This leads to a high density of defects and the formation of
a rough surface. Various techniques are used to solve this problem. The use of gradient SiGe buffer
layers with a variable composition and surface smoothing by chemical-mechanical polishing at a
composition of Si₀₅Ge₀₅ are well-known methods. Although a threading dislocation density (TDD) of
about 10⁹ cm⁻² can be achieved by this method, this requires gradient buffer layers with a significant
thickness (around 10 microns) [5, 6]. However, it is desirable to have much thinner layers for device
applications due to thermal cracks in structures with layers having different coefficients of linear
thermal expansion.

Another widely used technique for Ge/Si growth consists of a low-temperature growth phase at
330 - 400°C followed by high-temperature growth at 600 - 850°C followed by annealing [2, 7]. This
method allows one to obtain layers with a dislocation density less than 10⁶ cm⁻² [8].

We have developed a method for growing high-quality epitaxial Ge layers on silicone substrates
using hot wire chemical vapor deposition (HW CVD) [9]. Germanium layers with a thickness of
0.2 - 5 µm are grown at a constant low temperature of 350°C with an average growth speed of 1 µm
per hour. TDD of a 1.4 µm thick Ge layer is about 10⁶ cm⁻² (determined by the density of etching pits),
and the surface roughness of the layer (rms) reached down to 0.37 nanometers according to atomic
force microscopy (AFM). Thin Ge layers on Si substrates had high structural quality: according to
X-ray diffraction data, FWHM in the best samples is about 0.06°. In this work, we investigated the
structural quality of GaAs layers and GaAs diode structures grown by MOCVD on Ge/Si(001), as well as some of electrical characteristics. The following methods were used for study of Ge and GaAs layers: transmission electron microscopy (TEM), secondary ion mass spectrometry (SIMS), and X-ray diffraction (XRD).

2. Experiment

The epitaxial growth of Ge layers on Si(001) substrates was carried out by the HW CVD method with parameters close to those described in [9]. The substrates were boron-doped Si(001) wafers with a ± 4° offcut to <110> with a resistance of 0.005 Ohm·cm. The buffer Si layer was grown at a low temperature of 400°C from a sublimation Si source. That layer was also doped with boron for creating a layer with an increased concentration of boron on its surface due to a segregation of this dopant as the layer grows. A germanium layer with a thickness of 0.2 - 0.3 microns was grown at a constant low temperature of 350°C with a speed of 0.75 μm per hour. The growth of the Ge layer was initiated by decomposition of germane GeH₄ in the area of a hot tantalum wire at 1350°C.

The growth of GaAs layers was carried out at a substrate temperature of 480 - 650°C in a MOCVD system. Before growth, Ge/Si substrates were annealed at a temperature of 600 - 700°C in a hydrogen ambient. First, the p-type carbon-doped GaAs layer with a 3 μm thickness was grown at lower temperature. Then, a 0.5 μm – thick silicon-doped n-type GaAs layer was grown at 650°C temperature. The carrier concentration was 10¹⁶ cm⁻³ and 10¹⁸ cm⁻³ in p-type and n-type GaAs layers, respectively. We investigated electrical parameters of the resulting n⁺-GaAs/p-GaAs/p-Ge/p⁺-Si structure. 300 μm-mesa-structures with a were formed to measure the current-voltage characteristics.

3. Results and discussion

Figure 1 shows TEM images of a cross section of the Ge/Si(001) heterostructure. Most of dislocations are located at the Ge-Si interface (Si substrate shown on the bottom). Some of them generate threading dislocations (as can be seen in the image with a higher magnification) and then, as they advance, they meet and annihilate in the region of the Ge layer.

![Figure 1. Cross section HRTEM images of the Ge/Si(001) template. The image on the right shows the magnified region indicated on the left image.](image)

The X-ray diffraction spectrum of the epitaxial GaAs/Ge/Si(001) structure includes a GaAs peak with a FWHM of 0.091° (a typical value of the FWHM of the XRD rocking curve at the (004) GaAs position is about 0.055). A 0.3-μm-thick Ge layer used for the diode structure had a FWHM value of 0.145°. The surface roughness of the top GaAs layer was rms = 0.5 nm. The layer-by-layer elemental SIMS analysis of the investigated heterostructure is shown in figure 2. It can be seen that the distribution of Ge, As, and Ga elements is uniform, and there is significant diffusion of Ge and Ga through the GaAs/Ge boundary. To suppress this effect, we use a thin AlAs layer between the GaAs and Ge layers [10], but this method was not implemented in the samples we describe in this paper.
A test sample was grown with one layer of silicon-doped n-type GaAs on a semi-insulating Si/Ge(001) substrate. Hall effect measurements of the test sample have shown carrier concentration \( n = 1.2 \times 10^{19} \text{ cm}^{-3} \), drift mobility \( \mu = 594 \text{ cm}^2/\text{V} \cdot \text{s} \), and resistivity \( \rho = 0.0009 \text{ Ohm} \cdot \text{cm} \). The mobility of carriers in the test sample is around 4 times lower than for the GaAs sample [11] on a native substrate due to threading dislocations. Figure 3 demonstrates current-voltage characteristic of the diode structure. It can be seen that it has fairly low reverse currents and good rectifying properties even without the use of a passivating coating on the side surface of the p-n junction.

**Figure 2.** SIMS of the GaAs/Ge/Si structure.

**Figure 3.** Current-voltage characteristic of the n'-GaAs/p-GaAs/p-Ge/p'-Si diode structure.

In conclusion, the heterostructures with individual GaAs layers, as well as an n+-p GaAs junction, have been grown via MOCVD and investigated. High-quality Ge/Si(001) templates grown via hot-wire CVD were used as substrates for heterostructures. Resulting diode structures demonstrated low reverse currents. The results we obtained indicate the possibility of using these methods of epitaxial growth of GaAs/Ge/Si structures for fabrication of various applied structures, including solar cells.

**Acknowledgments**

This study was supported by the Russian Foundation for Basic Research (projects 18-32-00636 (MOCVD growth and electrical parameters measurements) and 19-32-90184).

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