A 16-Channel Low-Power Neural Connectivity Extraction and Phase-Locked Deep Brain Stimulation SoC

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Abstract—Growing evidence suggests that phase-locked deep brain stimulation (DBS) can effectively regulate abnormal brain connectivity in neurological and psychiatric disorders. This letter therefore presents a low-power SoC with both neural connectivity extraction and phase-locked DBS capabilities. A 16-channel low-noise analog front-end (AFE) records local field potentials (LFPs) from multiple brain regions with precise gain matching. A novel low-complexity phase estimator and neural connectivity processor subsequently enable energy-efficient, yet accurate measurement of the instantaneous phase and cross-regional synchrony measures. Through a flexible combination of neural biomarkers, such as phase synchrony and spectral energy, a four-channel charge-balanced neurostimulator is triggered to treat various pathological brain conditions. Fabricated in 65-nm CMOS, the SoC occupies a silicon area of 2.24 mm\textsuperscript{2} and consumes 60 \(\mu\)W, achieving over 60\% power saving in neural connectivity extraction compared to the state-of-the-art. Extensive in-vivo measurements demonstrate multichannel LFP recording, real-time extraction of phase and neural connectivity measures, and phase-locked stimulation in rats.

Index Terms—Deep brain stimulation (DBS), neural connectivity, Parkinson’s disease (PD), phase locking value (PLV), phase-amplitude coupling (PAC), psychiatric disorders.

I. INTRODUCTION

Deep brain stimulation (DBS) is a well-established therapy for movement disorders such as Parkinson’s disease (PD) and essential tremor. However, the conventional open-loop DBS causes stimulation-induced side effects, can consume high energy [1], [2], and lacks sufficient efficacy in emerging applications such as psychiatric and memory disorders [3]. It may be more efficient and effective to deliver DBS locked to the phase of ongoing neural oscillations [3], [4], an approach that has already shown promise in movement disorders [1]. Excessive interregional connectivity indicates pathological brain states in PD [5] and network-based diseases such as depression [3]. Continuous monitoring of neural connectivity and its regulation via phase-locked DBS could provide a new solution to treating such disorders.

TheCORDIC processors in [6] and [7] can accurately compute the instantaneous phase and neural connectivity measures such as phase locking value (PLV) and phase-amplitude coupling (PAC). However, the high accuracy comes at the cost of significant power consumption (>200 \(\mu\)W). Furthermore, the clock latency in the pipelined CORDIC would hinder real-time phase-locked stimulation. Delgado-Restituto et al. [8] reported a low-complexity PLV approximation algorithm based on local minima detection. While efficient, this approach compromises PLV accuracy and cannot track the instantaneous phase and amplitude in real time for oscillation-locked stimulation.

This letter extends upon our first-in-literature phase-locked DBS SoC [9] with more circuit details, analyses, and measurement results. An energy-efficient neural connectivity processor is proposed to overcome the energy-accuracy bottleneck in the existing designs. The phase-locked DBS prototype is extensively validated via benchtop and in-vivo testing.

II. SoC ARCHITECTURE

To effectively regulate cross-regional connectivity, the system must achieve: 1) low-noise multichannel local field potential (LFP) recording with precise gain matching; 2) accurate, continuous extraction of instantaneous phase and connectivity measures; and 3) charge-balanced stimulation to minimize tissue damage.

Fig. 1 presents the architecture of the proposed phase-locked DBS SoC that meets these criteria. A 16-channel chopper-stabilized analog front-end (AFE) conditions LFPs from two (or more) DBS leads with cylindrical electrodes. The digitized LFPs are sent to the proposed neural connectivity processor for phase-locked DBS control. A programmable finite impulse response (FIR) filter performs low-pass filtering (LPF) for decimation, bandpass filtering (BPF), and the Hilbert transform (HT) through hardware sharing. The filtered signals are processed in a feature extractor (FE), where the instantaneous phase and amplitude envelope are extracted per sample, and PLV, PAC, and spectral energy (SE) on a window-by-window basis. Upon detection of pathological neural activity (e.g., excessive PLV or PAC...
Fig. 2. Circuit implementation of the 16-channel chopper-stabilized AFE.

Fig. 3. Programmable threefold FIR filter architecture and timing diagram.

via feature thresholding), a four-channel high-voltage compliant stimulator delivers charge-balanced biphasic pulses to the brain, timed to a specific phase of neural oscillations.

III. CIRCUIT IMPLEMENTATION

A. Low-Noise Analog Front-End

Fig. 2 presents the circuit implementation of the 16-channel AFE. A two-stage low-noise amplifier (LNA) adopts a current-reuse topology for enhanced noise efficiency. The noise performance is further improved by chopper stabilization that suppresses flicker noise in the LFP band (1–500 Hz). A dc servo loop (DSL) cancels electrode dc offsets (≤±50 mV), and 3-bit tunable positive feedback capacitors boost the input impedance. To save chip area, the 16-channel LNA outputs are multiplexed into a programmable-gain $G_m$-C integrator followed by a 10-bit successive approximation register (SAR) analog-to-digital converter (ADC). The integrator performs charge sampling for the ADC without the need for power-demanding buffers. The closed-loop LNAs with the shared integrator achieve precise gain matching, which is crucial for cross-regional connectivity extraction. A 16-to-1 multiplexer can address the input channels in any user-defined order, allowing biomarker extraction from a flexible combination of channels. When stimulation is triggered, blanking is performed by turning off the input chopper and resetting the AFE input to prevent amplifier saturation due to stimulation artifacts.

B. Neural Connectivity Processor

The programmable threefold FIR architecture is depicted in Fig. 3. The FIR decimates the 16-channel AFE output by a factor of four and generates 16 bandpass-filtered signals and 16 analytic pairs ($Re$ and $Im$) in any preprogrammed frequency bands. Three banks of delay registers (LPF, BPF, and HT) share a single multiplier-adder chain to reduce chip area. Each delay line is individually clock-gated, reducing the effective switching frequency of registers to 4 kHz (LPF) and 1 kHz (BPF and HT) to save dynamic power.

To facilitate low-complexity phase extraction on chip, we propose a lightweight phase extractor (LPE) that achieves a superior power-accuracy tradeoff than conventional methods. Fig. 4 shows the LPE hardware implementation and underlying approximation algorithm based on first-order Lagrange interpolation [10]. Here, sign detection and magnitude comparison are used to identify the region of the input analytic pair in the complex plane. Bit-scaling and numerator-denominator selection are subsequently performed to confine the input to the [$0, \pi/4$) range. The fraction of the real and imaginary signals is then calculated using a reciprocal look-up table (LUT) and a multiplier. To improve phase accuracy, the first-order approximation errors ($\approx 4^\circ$) are corrected by a linearization LUT. Thanks to the input range reduction, the size of the reciprocal and linearization LUTs is reduced to $2^{8} \times 9$ and $2^{8} \times 7$ bits, respectively, for 10-bit phase extraction. Finally, the trigonometric periodicity identities are exploited to reconstruct the [$−\pi, \pi$] range by adding an offset value to the error-corrected fraction. The 10-bit phase outputs of LPE are last-bit accurate with respect to an ideal arctangent operator in MATLAB. Compared to an unrolled CORDIC, the LPE is 30.1% more area efficient while consuming 52.4% less power.

Fig. 5(a) shows the proposed neural connectivity extractor. In addition to the phase, the ideal PAC [11] and PLV [12] extractions involve the computation of amplitude envelope and/or magnitude. For improved hardware efficiency, the complex Euclidean norm is approximated by the $l_\infty$-norm, which takes the larger of the two absolute input values as output. To validate these approximations, we
performed a feature correlation analysis and a seizure detection task on an epilepsy dataset (iEEG.org) using the gradient boosting model proposed in [13]. Fig. 5(b) shows that the approximated features are >95% correlated with the ideal ones and only marginally affect the seizure detection performance. The neural connectivity extractor can simultaneously extract eight PAC/PLVs, 16 phases, and 16 amplitude envelopes from any combination of eight channel pairs while only dissipating 9.69 $\mu$W of power (including the FIR).

To allow flexible stimulation control for different therapeutic settings and symptoms, the SoC supports multiple stimulation modes by tracking: 1) per-sample phase or amplitude envelope; 2) windowed PLV, PAC, or SE; or 3) a combination of the two, as depicted in Fig. 5(c). For instance, stimulation can be locked to the phase crossing at a target value ($\theta_{\text{MP}}$), while cross-regional PLV or PAC lies within a predefined therapeutic range set by $\theta_{\text{WIN},L}$ and $\theta_{\text{WIN},H}$.

As a unique feature of this SoC, randomized phase locking can also be enabled using a pseudo-random binary sequence (PRBS) threshold generator in order to disrupt a target oscillation in the brain.

C. Charge-Balanced Neurostimulator

Fig. 6 depicts the four-channel high-voltage compliant, charge-balanced neurostimulator. The biasing circuit maintains the operating point of stacked transistors within a tolerance range under the 8-V charge pump output. To precisely match the anodic and cathodic phases for minimized tissue damage, an H-bridge architecture with a single current sink is adopted for the current driver. The active charge balancing (CB) circuitry adjusts the current amplitude such that the residual voltage at the electrode-tissue interface is kept below $\pm V_{\text{SAFE}}$. Any residual charges are removed through passive discharging.

IV. MEASUREMENT RESULTS

A phase-locked DBS prototype was fabricated in a TSMC 65-nm CMOS process. Fig. 7(a) presents a chip micrograph, and the SoC area and power breakdowns are illustrated in Fig. 7(b). The SoC occupies an active area of 2.24 mm$^2$ and consumes 60 $\mu$W at 1.2/0.85-V analog/digital supply voltages.

A. Benchtop Measurements

Fig. 8(a) presents the input-referred noise (IRN) performance of the AFE measured at the ADC output. Chopper stabilization reduced the IRN from 4.4 $\mu$Vrms to 0.88 $\mu$Vrms in 1–500 Hz, which translates to a noise efficiency factor of 2.32 with 2.78-$\mu$W/ch power consumption. The gain programmability (53–61 dB) is shown in Fig. 8(b). At the maximum gain setting, precise 16-channel gain matching ($\sigma$/mean < 0.1%) was achieved in the mid-band. With a 2-mVpp, 40.039-Hz sine input, the in-band SNDR and SFDR were measured at 54.5 dB and 63.4 dB, respectively, as shown in Fig. 8(c). When chopped at 64 kHz, the positive feedback loop boosted the input impedance from 1.6 M$\Omega$ (simulated) to 43.9 M$\Omega$ (measured) at 100 Hz. Fig. 8(d) demonstrates that with an intentional 50% pulse width mismatch, CB reduced the residual voltage at the stimulator output to $\pm 4 mV$. Fig. 8(e) presents a polar histogram of phase locking errors evaluated on the prerecorded LFPs of a Long-Evans rat. The stimulation trigger was locked to the 180$^\circ$ of theta-band (4–8 Hz) oscillations. To account for the FIR group delay (31 ms), the trigger was timed 67$^\circ$ ahead of the target phase, given the 6-Hz center frequency (360$^\circ \times$31 ms/166.6 ms). The phase locking error is the deviation of the ground-truth phase from the target at trigger instants, where the ground truth was computed using second-order zero-phase Butterworth BPF and ideal HT in MATLAB. The histogram shows that the errors are tightly grouped around 0$^\circ$. Fig. 8(f) demonstrates the SoC’s noise tolerance in phase locking detection. Input signals were comprised of different levels of pink noise superimposed on a 2-mVpp, 6-Hz sine wave, and phase locking errors from the 180$^\circ$ target were measured. The nearly constant error at noise levels below 10 $\mu$Vrms suggests that the AFE’s thermal noise requirements could be relaxed to save power, depending on the background noise level. This noise margin could also be used to reduce
connectivity extraction is demonstrated in Fig. 9(c) and (d). The approximated PLV and PAC closely track the ideal features. Fig. 9(e) presents closed-loop stimulation triggered by the instantaneous phase and a combination of cross-regional PLV and phase, respectively. Here, the maximum stimulation frequency was set to 6 Hz, and the stimulator controller was designed to ignore threshold crossings due to phase wrapping.

Table I compares the proposed SoC with the existing neural connectivity processors. Our SoC consumes >60.7% less power for connectivity extraction than the CORDIC processors [6], [7], while outperforming the PLV approximator [8] in accuracy. Moreover, this work presents the first phase-locked DBS SoC demonstrated to date. With flexible stimulation control and various biomarkers integrated, this approach could serve as a new stimulation paradigm for a wide range of brain disorders.

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