Neuromorphic Learning towards Nano Second Precision

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Abstract

Temporal coding is one approach to representing information in spiking neural networks. An example of its application is the location of sounds by barn owls that requires especially precise temporal coding. Dependent upon the azimuthal angle, the arrival times of sound signals are shifted between both ears. In order to determine these interaural time differences, the phase difference of the signals is measured. We implemented this biologically inspired network on a neuromorphic hardware system and demonstrate spike-timing dependent plasticity on an analog, highly accelerated hardware substrate. Our neuromorphic implementation enables the resolution of time differences of less than 50 ns. On-chip Hebbian learning mechanisms select inputs from a pool of neurons which code for the same sound frequency. Hence, noise caused by different synaptic delays across these inputs is reduced. Furthermore, learning compensates for variations on neuronal and synaptic parameters caused by device mismatch intrinsic to the neuromorphic substrate.

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1. INTRODUCTION

Phase-locking has been shown to be one approach towards precise temporal coding in neural information processing [4] and is observed in the auditory pathway of barn owls [3]. Barn owls locate sounds by measuring the difference between the respective arrival times at both ears, the so-called interaural time difference (ITD), also known as the Jeffress model [10]. A neuron in the laminar nucleus will fire at a high rate if it detects coincidences between the two periodic signals that code the same sound frequency at both ears (Figure 1B and C). In other words, the neuron will fire at a maximum rate if the signals from both ears arrive coherently. This requires spike times that are “locked” to a specific phase of the sound signal. The more precisely spikes are locked, the higher the temporal resolution for measuring ITDs is. Previous studies have shown phase-locking with precision much smaller than the membrane time constants of the involved neurons [3]. However, synaptic delays differ across the neurons that code for the same sound frequency [3]. Coherence in the arrival time of signals can be restored by learning transmission delays [20] or by selecting synapses with simultaneous activity [4].

In this study, we present an analog, neuromorphic implementation of a spiking neural network which selects inputs out of a broad distribution of transmission delays by means of an unsupervised, on-chip Hebbian learning rule. The intrinsic, high acceleration factor of the neuromorphic substrate [16] allows for learning of phase-locking with 100 ns precision in hardware time domain. Finally, the results of this on-chip synapse selection is applied to detect ITDs of less than 50 ns.

In addition to noise induced by variations in transmission delays, device mismatch in analog circuitries of neurons and synapses causes fixed-pattern noise on neural components. This means, parameters vary between neurons and synapses, as, for example, in the membrane time constant and synaptic strength.

Both types of variations can be reduced by off-chip calibration routines. In this study, they are compensated by on-chip learning mechanisms. In contrast, an implementation without plasticity, but the same variations in neural components, can barely measure any time differences between two 1 MHz signals in hardware time domain.

One of the first neuromorphic implementations for coincidence detection was a silicon replication of the auditory pathway [12]. Sound location is implemented by two synapses which transmit the signal from each ear. However, this device does not support on-chip learning, and connectivity between neurons is hard-wired. In this study, each ear is represented by a population of synapses rather than a single synapse. Inspired by the biological example [3] we add noise to the synaptic delays of this population. We demonstrate that spike-timing dependent plasticity which is implemented in our neuromorphic hardware system de-noises the input. The novelty of this system is to combine a dense integration of highly accelerated neurons with on-chip learning in each synapse [16] that allows for learning of coincidence detection with resolution higher than 50 ns. Other approaches with re-configurable connectivity and on-chip plastic synapses have lower counts of neurons and synapses [8, 1, 6], mostly optimized for low power consumption, or operate in biological real-time [21].

2. NETWORK AND HARDWARE DESCRIPTION

The neuromorphic hardware system we used is designed as a re-configurable, universal neuromorphic substrate on which neural networks operate $10^4$ times faster than biological real-time (Figure 1A, [16]). It comprises pair-wise spike-timing dependent plasticity (STDP) in each of up to 256 synapses per neuron [19]. This type of Hebbian learning rule is adapted from measurements in biological tissue [14, 2, 15] and is described later in this section.

The network model implemented in silico is inspired by the auditory pathway of barn owls [3, 4]. In this study, we investigate sound processing of a single frequency channel, exemplarily for any frequency of comparable scale. A neuron in the nucleus laminaris receives bilateral input from several neurons in the cochlear nucleus magnocellularis (Figure 2). The network selects those inputs, of which signals arrive coherently
FIGURE 2: Network implementation on the neuromorphic chip. The postsynaptic hardware neuron (black circle) receives input from 64 presynaptic spike sources, whose spike times are generated on the host computer and transferred to the chip. All inputs (black triangles) show regular spike times of identical frequency $f = \frac{1}{T} = 2\text{kHz}$, but each input is shifted in time following a Gaussian distribution with $\sigma = 300\mu\text{s}$ (blue). For simplicity we neglected $p_{\text{spike}} < 1$ and jitter on spike times in this schematic. When the postsynaptic neuron fires, each synapse (red circles) measures the correlations ($\Delta t$) between its pre- and postsynaptic spikes. During the next evaluation of these synapses, their weights $w$ are potentiated or depressed according to an additive rule ($\Delta w = \pm 1$, respectively).

at the postsynaptic neuron, in order to improve the temporal coding of sound signals which is used for sound localization.

The delay of signal transmission $\Delta d_i$ for each connection with index $i$ is Gaussian distributed with standard deviation $\sigma$ [3]. Note that $\sigma \cdot 2$ is larger than the period $T$ of the input signal and, consequently, neighboring volleys of spikes overlap (black and blue spikes in Figure 2). The postsynaptic neuron is mimicked by a hardware neuron that approximates the conductance-based, leaky integrate-and-fire model [16, 9]. The presynaptic input is modeled by individual spike trains fed into the system. Figure 2 shows the allocation of hardware resources including the synaptic nodes, each of which comprises STDP.

As the membrane time constant of hardware neurons can not be configured to values below $T_{\text{hw}} \approx 200\text{ns}$ in hardware time domain, we assume an acceleration factor of 500 throughout this study for better comparison with biological measurements. Thus, all time constants, as well as experiment time, are given in biological time domain, if not stated otherwise. For example, in the following, we use a neuron with $T_{\text{hw}} = 200\text{ns}$ in hardware time domain which translates to $T_m = 100\mu\text{s}$ in biological time domain, as suggested in [4].

We stimulate the network with a pure tone similar to [4]. For each presynaptic input spikes are drawn with probability $p_{\text{spike}} = 0.35$ from a template of regular spike times with frequency $f = 2\text{kHz}$ in biological time domain. Additionally, each spike has a jitter following a Gaussian distribution with standard deviation $40\mu\text{s}$. The individual transmission delay $\Delta d_i$ for each input with index $i$ is modeled by being added to all spike times of this input.

On hardware, the strength of a synaptic connection $g_i$ is the product of a conductance $g_{i,\text{max}}$ adjustable for each input stream (triangles in Figure 2) and a 4-bit digital weight $w_i$ stored in each synapse:

$$g_i = g_{i,\text{max}}w_i$$

While $g_{i,\text{max}}$ is static throughout an emulation run, $w_i$ is subject to STDP and can assume integer values between 0 and 15. However, $g_{i,\text{max}}$ varies between synapses. This is caused by device mismatch due to imperfections in the production process [16]. Excitatory postsynaptic potentials (EPSPs) were recorded by measuring the impact of a single spike on the resting state of the postsynaptic membrane potential $V_m$ (Figure 3A). Their time course is configured to be as short as possible, and their amplitude ($g_{\text{max}}$) is set to an intermediate value. This results in a target firing rate of approximately $1\text{kHz}$ in the final network implementation.

Synaptic weights $w_i$ are modified by on-chip learning mechanisms at accelerated runtime described as follows: The temporal correlations between spike pairs are measured and stored locally in each synapse by analog circuitry. Correlations between pre-post and post-pre spike pairs are accumulated as charge on two capacitors, respectively. In contrast to the local measurement and accumulation, the evaluation of these measurements is performed by controllers shared between synapses. Thereby, the controller compares for each synapse the amount of charge on its capacitors as follows:

$$|a_c - a_a| > a_{\text{th}}$$

FIGURE 3: EPSPs and STDP learning windows of 64 hardware synapses. (A) Each EPSPs is averaged over 100 runs. The mean and standard deviation over all synapses is depicted in black and gray, respectively. The membrane potential $V_m$ is plotted in arbitrary units. The area under these EPSPs has a ratio of standard deviation to mean of $\approx 50\%$. (B) Recording STDP learning windows (gray) is summarized as follows: The inverse number $1/N$ of spike pairs that need to be accumulated until a weight update is elicited is plotted against the time difference $\Delta t$ between the pre- and postsynaptic spike (details are described elsewhere [17]). A value of $N = 1$ means that one pre-post pair is already sufficient to mark this synapse to be updated. The mean over all synapses and errors at half maximum (0.044 $\pm$ 0.009ms and $-0.050 \pm 0.016\text{ms}$) are depicted in black.
\[ a_c - a_a > 0 \] (3)

where \( a_c \) is the charge on the capacitor for pre-post, \( a_a \) for post-pre spike pairs, and \( a_{th} \) a configurable threshold. If Equation 2 is true the synaptic weight is updated and the capacitors are discharged. Otherwise the weight stays unchanged and correlations are further accumulated without discharge of the capacitors. If a weight update is elicited, the synaptic weight will be increased by one if Equation 3 is true, otherwise it is decreased by one (in both cases with absorbing boundaries at the minimum and maximum value). In fact, hardware STDP is not limited to this additive rule, but can be configured to any rule via look-up tables. In the network presented, processing one synapse takes 1.5 \( \mu \)s in hardware time domain, which has been shown to be sufficient for coincidence detection in small networks [17]. For a detailed description of the implementation and configuration of hardware STDP see [19] and [17].

Parameters for the learning window of STDP on hardware must be adjusted to meet two criteria: On the one hand, the window should be broad in order to resolve a full period \( T \) of the input signal and to ensure a sufficiently high learning rate. On the other hand, the number \( N \) of spike pairs for close-by \( \Delta t \) should be distinguishable which is the case for overall large \( N \). In Figure 3B a trade-off between both criteria is shown, because they can not be fulfilled together on the hardware. Note that learning windows are subject to device mismatch too, due to their analog measurement and accumulation circuitry. The width at half maximum is approximately 0.05 ms in biological time domain. The time between successive weight updates for 64 inputs is 48 ms.

The experiment protocol is split into two steps. First, the network is stimulated without any interaural time difference and on-chip plasticity is activated. The network selects appropriate inputs by altering on-chip, synaptic weights. Second, these learned synaptic weights are adopted for subsequent emulations, during which plasticity is turned off. The ITD is varied and sound is located via the firing rate of the postsynaptic neuron.

In the first step, the spiking neural network shown in Figure 2 is emulated for a duration of 10 s, while spike times of the postsynaptic neuron are recorded. After emulation, the digital weights of all synapses are read out from the chip.

Network performance is measured by the vector strength \( \nu \), which quantifies the precision of phase-locking at the postsynaptic site [5]. Each spike time \( t_i \) can be considered as a vector of unit length with a phase angle \( \Theta_i = 2\pi f t_i \) as well as \( x \) and \( y \) components as follows:

\[
(x_i, y_i) = (\sin(\Theta_i), \cos(\Theta_i))
\] (4)

The vector strength is defined as the length of the mean vector across the overall number \( N \) of postsynaptic spike times:

\[
\nu = \frac{1}{N} \sqrt{\left( \sum_{i=1}^{N} x_i \right)^2 + \left( \sum_{i=1}^{N} y_i \right)^2}
\] (5)

It can assume values between 0 and 1. It is minimal for randomly distributed spikes over time, and maximal for interspike intervals that are multiples of \( T \). The angular dispersion of the mean vector translates to temporal precision [7]:

\[
\sigma_{PL} = \sqrt{\frac{2(1 - \nu)}{2\pi f}}
\] (6)

In the second step, the sensitivity of the postsynaptic neuron's firing rate to time differences between two input signals, e.g. ITDs, is determined as follows: First, signal transmission delays and synaptic weights are adopted from the learning result of an emulation described above. Second, afferent connections are randomly divided into two groups of equal size. Third, time differences are modeled by adding an additional transmission delay to one of these groups. Finally, this network is emulated with static synaptic weights, and the firing rate of the neuron is recorded.

3. HARDWARE EMULATION RESULTS

Network emulations on hardware show precise, phase-locked spiking of the postsynaptic neuron. At the beginning of an emulation, all synapses have the same weight, and the firing rate of the postsynaptic neuron is low. The firing rate increases with increasing weights of those inputs that drive the neuron most (compare Figure 4A to green traces in B). Once strong synapses have evolved, phase-locking improves (\( \nu \) increases, not shown) and synapses firing out of phase are weakened (red
vector strength of $\nu$. Postsynaptic spikes occur preferably at the same phase with a distribution is normalized such that its mean is $0$. Bottom: The same distribution after learning, but only synapses with $w > w_{\text{start}}$ are shown. The phase obtained by summing up the phase vectors (Equation 4) of all spikes is subtracted from the transmission delays after each emulation. In other words, transmission delays are normalized such that the postsynaptic neuron fires preferably at $\Delta d = 0$. The distribution of digital hardware weights $w$ after learning for the same emulations as in (A). Before learning all weights were set to $w_{\text{start}} = 7$ (arrow).

traces in Figure 4B). After approximately 3 s, the strong and weak synapses are in balance, and the postsynaptic firing rate saturates. The variance of firing rates between emulations (Figure 4A) is mostly caused by re-drawing the transmission delays for each emulation. Variations on synapses bias the learning process. For example, few strong synapses with improbable ($|\Delta d| \gg 0$ in upper plot of Figure 5A), but similar $\Delta d$ may outperform many weak synapses with probable ($\Delta d \approx 0$), but similar $\Delta d$. Nevertheless, learning compensates for these variations.

Synapses will be termed selected if their weight after emulation exceeds their initial weight. Synapses with similar transmission delays or delays which differ by multiples of $T$ are active simultaneously, and preferably drive the postsynaptic neuron. If a postsynaptic spike is elicited by these inputs, they are selected by the on-chip learning mechanism (compare Figure 5A to Figure 4B). This periodical selection scheme with period $T$ is due to the overlap of consecutive spike volleys (Figure 2). However, not all synapses saturate to the minimum or maximum weight (Figure 5B). Some synaptic weights stay at their initial value. This can be explained by the technical implementation of STDP on hardware. If both correlations, pre-post and post-pre, accumulate at the same rate, no weight update will be triggered because the update controller evaluates the difference between both accumulations (see Equation 2 and [19]).

As an application, we show the detection of ITDs. To this end, we split the resulting synapses of a single run of Figure 5 into two groups, one for the input from each ear. Both, selected and unselected synapses are adopted. The performance of phase-locking with $\Delta\text{ITD} = 0$ is shown in Figure 6A. Postsynaptic spikes occur preferably at the same phase with a vector strength of $\nu = 0.89$ which translates to a precision of $\sigma_{\text{PL}} \approx 40 \mu s$ in biological time domain. Shifting the input of one group by $\Delta\text{ITD}$ deteriorates the precision of phase-locking and consequently reduces the postsynaptic firing rate (Figure 6C). At $\Delta\text{ITD} = \frac{T}{2}$ the postsynaptic neuron receives alternating input from both groups, and the vector strength is on the same level as the control (compare Figure 6C to D). For the control we applied the same protocol as before (see Figure 6A and C), but with a uniform weight distribution instead of previously learned synaptic weights. Time differences of less than 25 $\mu$s can be resolved by the firing rate of the postsynaptic neuron (compare error bars of neighboring data points of thin red line in Figure 6C). In contrast, the firing rate of the control barely has a dependency on $\Delta\text{ITD}$ (thin red line in Figure 6D). This makes it difficult, if not impossible, to determine any time differences of 2 kHz signals.

4. CONCLUSIONS
We have presented an analog, neuromorphic network implementation that de-noises phase information and thereby learns to resolve time differences between two periodic stimuli of less than 50 ns in hardware time domain. De-noising is realized by unsupervised, on-chip spike-timing dependent plasticity that improves coincidence detection and locks spike times
to a specific phase of the input signal. This results in precise phase information at the neuron site which enables the resolution of short phase differences, as for example those of sound signals from both ears. The network performance is comparable to similar network models simulated in software (compare Figure 6C to Figure 7). However, the absolute values for firing rate and vector strength differ due to different neuron, synapse, and STDP models, variations of model parameters on hardware, as well as a higher signal frequency in the reference publication [4].

Additionally, learning does not only de-noise the input, but also compensates for variations between neural components (Figure 3). These variations are caused by device mismatch and are inherent in all neuromorphic systems with analog circuitry. Intrinsically weak synapses with simultaneous impact on the membrane potential can outperform intrinsically strong synapses. This allows the measurement of short time differences, although the input is noisy and the neuromorphic substrate has variations in its neural components. Performance may even be improved by a preceding off-chip calibration of synaptic strengths. Furthermore, population coding reduces noise within signal transmissions by averaging across many unreliable components.

Although variations of neuronal components are measured in biology [13], it is still unclear how robust a neural network has to be in order to perform computation on these components. Large-scale neuromorphic systems, as described in [18], may particularly benefit from such self-adjusting, and hence robust, network implementations. In further studies, the neuromorphic network could be embedded into robotic systems for processing sensory data of, for example, ultrasonic sound. This would exploit the high acceleration factor of the neuromorphic system and its robust capability for handling noise and variations of neural components.

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