The fabrication technology of VCSELs emitting in the 1.55 μm waveband

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Abstract. The paper presents the results on fabrication technique of a 1.55 μm wafer-fused vertical-cavity surface-emitting lasers (VCSELs) based on the InAlGaAsP/InP optical cavity and AlGaAs/GaAs distributed Bragg reflectors (DBRs) grown by solid-source molecular beam epitaxy. The optical cavity InAlGaAsP/InP contains an active region based on multiple InGaAs quantum wells, n⁺/+p⁺-In(Al)GaAs buried tunnel junction (BTJ), InGaAsP intracavity contact layers and n-InP spreading layers. The top and bottom AlGaAs/GaAs DBRs were grown on GaAs substrate, while the optical cavity InAlGaAsP/InP was grown on InP substrate. The main fabrication processes of 1.55 μm VCSELs such as: BTJ fabrication, dry etching of first mesa on top DBR, wet etching of second VCSEL mesa, forming of the ohmic contacts and passivation of the VCSEL structure were described in details.

1. Introduction

Heterostructure-based semiconductor lasers are widely used in transceivers of fiber-optic communication systems, gas sensors, and input-output devices based on optical principles. The vertical-cavity surface-emitting laser (VCSEL) is a type of semiconductor laser with beam emission perpendicular from the top surface. VCSEL are superior to other types of a diode lasers due to their lower power consumption, symmetrical radiation pattern, higher spectral quality and lower manufacturing costs [1]. The level of modern research makes it possible to fabricate a VCSELs with an effective modulation frequency of 28 GHz and to demonstrate the optical data transmission at the rate of 47 Gbit/s [2].

Long-wavelength VCSELs are interesting for optical communication systems, fiber systems and other applications connected with silicon photonics. 1.55 μm range VCSELs are of particular interest since due to the propagation losses in a quartz fiber are ten times lowers than for lasers with 0.85 μm wavelength.

In contrast to a 0.85 μm VCSEL, the fabrication of a 1.55 μm VCSEL has a number of difficulties. The key problem is the lack of an effective active region based on InAlGaAs/GaAs material system emitting at 1.55 μm. In case of InAlGaAsP/InP material system low contrast of the refractive indices of the InAlGaAs, InAlAs, InGaAsP and InP layers becomes a problem. In fact, to achieve the required reflectivity of distributed Bragg reflectors (DBR), it is necessary to use a large number of quarter-wavelength layers. However, the low thermal conductivity of InGaAs/InAlGaAs/InAlAs/InGaAsP...
layers as compared to the AlGaAs/GaAs layers lead to extra heating of the active region and negatively impact on VCSEL performance.

One of the possible approaches to solve the mentioned problems is based on wafer-fusion technique. The hybrid VCSELs heterostructure (figure 1) is formed by direct wafer bonding of the InAlGaAsP/InP optical cavity heterostructure with the active region and two AlGaAs/GaAs DBR heterostructures under pressure and elevated temperature [3]. Such approach makes it possible to combine the advantages of both material systems [4].

The basic design of wafer-fused VCSEL heterostructure emitting in the 1.55 μm spectral range is based on vertical microcavity with undoped mirrors and intracavity contact (IC) layers, see figure 1. The heterostructure consists of a GaAs substrate, a bottom AlGaAs/GaAs DBR, bottom n-InP IC-layer with the InGaAsP fusion layer and n'-InGaAsP contact layer, strained In(Al)GaAs QWs, the the n''+/p''+ -InGa(Al)As tunnel junction (TJ) with p-InAlAs emitter, top n-InP IC-layer with the n'-InGaAsP contact layer and a top AlGaAs/GaAs DBR. More details about the structure of the lasers can be found in [5].

In this work, we present the full fabrication cycle and characterization results of 1.55 μm wafer-fused VCSELs based on an InP-based active region and GaAs-based DBRs grown by molecular beam epitaxy.

Figure 1. Design of the VCSEL formed by wafer-fusion. On inset: the schematic design of the BTJ.

2. The formation of the buried tunnel junction
The most promising way to provide effective current and optical confinement is applying the concept of buried tunnel junction (BTJ) [6]. The modified TJ design based on the highly doped n''-InGaAs, p''-InGaAs and p''-InAlGaAs layers was used to enable using the solid-source MBE for mesa structure regrows. The design of the BTJ is shown in figure 1. Mesastructure within a tunnel junction was created by local chemical etching of the n''-layers down to the p''-layer in a peroxide-phosphorus solution H₃PO₄: H₂O₂: H₂O using a photoresist mask formed by contact photolithography. After forming the surface relief in TJ, the photoresist was removed and the chemical cleaning in the HCl:H₂O solution was performed to remove the natural oxide from the TJ surface. To create BTJ the surface relief was overgrown by the top 0.5 μm-thick n-InP IC-layer using solid-source MBE. The surface of the structure after etching and after epitaxial overgrowing is shown in figure 2. Despite the evidence of the surface planarization effect during MBE-regrowth, the increasing of the mesa sizes in 1.5–2 times with the smoothing of the height step of the surface relief was revealed.

Figure 2. Photo of the surface after etching (left), and after overgrowing (right).
3. Wafer fusion process

As previously noted, in order to create the hybrid heterostructure of the 1.55 μm VCSEL, it is necessary to bond three semiconductor heterostructures see figure 3. At the first stage, the direct bonding of the optical cavity InAlGaAsP grown on InP substrate with the wafer of the top AlGaAs/GaAs DBR grown on GaAs substrate was carried out. After that, the chemical etching of the InP substrate was performed. Then the resulting stack was bonded to a wafer of the bottom AlGaAs/GaAs DBR grown on GaAs substrate under same conditions as during the first wafer-fusion. The final stage was the removal of the GaAs substrate from the side of the top DBR.

![Figure 3. Design of the final VCSEL heterostructure.](image)

![Figure 4. Positioning of the wafers in the fusion unit.](image)

Technically, wafer fusion is a process of high-temperature annealing in a vacuum, with the wafers oriented with their faces facing each other, and significant pressure is applied. It is extremely important to prepare the surface of the wafers and to remove organic contaminants and oxides, as well as the chemical activation of the surfaces for the occurrence of interfacial bonds. The chemical cleaning in the HCl:H₂O and HF:H₂O solution was used to remove the oxides from the surface of GaAs and InP (InGaAsP) respectively. This cleaning contributes to the intermolecular bonding of the wafers by van der Waals forces, and the elevated temperature contributes to the chemical reaction and recrystallization [7].

The direct bonding process was carried out on an EVG 510 wafer bonder at a temperature of 600 °C. Carrying out the process in vacuum (pressure less than 10⁻⁵ mbar) was contributed to the effective removal of volatile compounds formed on the surface of the wafers when heated, without the use of a system of etched grooves. A pneumatic press with a contact force of 7 kN has provided a uniformly pressed wafer clamp. The location of the wafers in the fusion unit is shown in figure 4.

Figure 5 depicts the cross-section of the GaAs-InGaAsP fused interface, obtained by high-resolution transmission electron microscopy (HRTEM). The fused interface is predominantly an amorphous layer with thickness of about 5-8 nm consisted of the III–V oxide phases. Note that the actual thickness of the GaAs-InGaAsP fused interface is mostly determined by the initial surface roughness of the heterostructures. Despite the lattice mismatch of GaAs and InP substrates, the dislocations or other extended defects near the fused interface is not observed.
4. Dry etching of the top DBR

The first stage of the creation of 1.55 μm VCSELs is the formation of a mesastructure in the top DBR (first VCSEL mesa). This step is necessary for opening the InGaAsP contact layer of the top IC-layer.

The mesa of the top DBR should have a smooth morphology, the sidewall angle of at least 80°, while the etching depth should be controlled with an accuracy of ± 5 nm in order to provide the ohmic contact to the top IC-layer. The set of requirements for the formation of a mesastructure in the layer of the top DBR, makes preferable to use the method of plasma etching (PE), rather than wet etching. The validity of this choice was confirmed by the wide use of PE processes for microprofiling of GaAs-based structures [8, 9]. The parameters of the top DBR heterostructure layers of are shown in table 1.

Table 1. Parameters of the layers of the experimental heterostructures.

| Number of repetitions | Material         | X     | Thickness, nm |
|-----------------------|------------------|-------|---------------|
| 20                    | GaAs             | 114.6 |               |
| 20                    | AlₓGa₁₋ₓAsAs     | 0.92  | 132.0         |
| 20                    | GaAs             | 114.6 |               |

To create the topology of the first VCSEL mesa, we used a SiO₂ mask formed by plasma-enhanced chemical vapor deposition (PECVD) followed by etching of the dielectric through a photoresist mask. The local etching of the top DBR via SiO₂ mask in an inductively coupled plasma was performed by Sentech SI 500 plasma. The hybrid VCSEL heterostucture includes highly-doped n-contact layer with a thickness of several tens of nanometers, while the total thickness of the top DBR exceeds 5μm. Therefore, it is very important to monitor the process in real time in order to stop the process after the complete removal of the DBR layers and avoid the damaging of the highly doped InGaAsP contact layer. The mentioned etching system has an interferometer for in-situ control during the etching process, which allows the precise etching of the top DBR. The typical interferogram of the etching process is shown in figure 6.

Figure 6. Typical interferogram of the DBR etching.
During etching, the samples were placed on a helium-cooled silicon substrate. It is needed because the surface of the structure can heat up during the PE and, as a result, the etching rate becomes nonlinear.

The BCl3 / N2 gas mixture is widely used for etching the semiconductor multilayer structure based on AlGaAs material system [10]. Since the etching process depends on the particular implementation of the equipment, the conditions for the etching of the AlGaAs DBR were optimized to ensure acceptable selectivity of the etching of AlGaAs layers relative to InGaAsP, low roughness of the etched surface, verticality of the etched mesa sidewalls while maintaining the mask resistance to etching and to minimize lateral decreasing of the mesa size. Based on this result, the following recipe was used for the etching process: RF power = 50 W, ICP power = 300 W, BCl3 flow = 20 sccm, N2 flow = 5 sccm, P = 0.5 Pa. Figure 7 shows a SEM image of the first VCSEL mesa formed in the top DBR, obtained using scanning electron microscopy (SEM).

**Figure 7.** SEM image of the first VCSEL mesa formed in the top DBR.

5. Wet chemical etching of the VCSEL optical cavity

The VCSEL structure included a two n-type IC-layers to which ohmic contacts should be formed. The top contact layer (anode) was opened after etching the first VCSEL mesa in the top DBR. To open the surface of the bottom contact layer, it is necessary to form a second mesa. To do this, etching the optical cavity based on InP/InGaAs/InAlGaAs/InAlAs/InGaAsP compounds was carried out by a wet chemical method in selective chemical etchants via photoresist mask. To simplify the technology process of electrical isolation of the contact pads of the anode and cathode, the second VCSEL mesa is formed in two steps. Therefore, for etching n-InP IC-layers we used an InGaAs selective etchant based on inorganic acids H3PO4 and HCl, as described in [11]. While for etching of InGaAs/InAlGaAs TJ layers and InGaAs/InAlGaAs quantum wells, we use a peroxide-phosphorus solution selective for InP, which is a mixture of H3PO4: H2O2: H2O.

After the process finish, the photoresist mask was removed and the etching depth was measured using optical profilometry.

6. Passivation of the VCSEL structure

Methods of thin films depositing can be arbitrarily divided into physical vapor deposition (PVD) and chemical vapor deposition (CVD). During physical vapor deposition, the sputtering of thin films occurs due to direct condensation of steam from the particles of the deposited material in vacuum, and the process includes the following stages: the formation of a vapor flow from microparticles, the transport of the vapor flow to the substrate, the condensation of the vapor flow on the substrate and the formation of the film. From this point of view the deposition of the dielectric, ion sputtering can be attributed to the first group, when the deposited material is sprayed by ion flux bombardmen. A key drawback of physical methods of vapor deposition is the relatively low degree of conformity of the relief coating.

In chemical deposition, the deposition of thin films occurs due to the chemical reaction of gases with the formation of solid products on the surface of the substrate (often due to additional activation of the process), and by-products of the reaction are removed from the reactor by a gas flow.

The most common chemical reactions for the formation of a dielectric layer include thermal decomposition (pyrolysis or cracking), deoxidation, oxidation, and chemical exchange reactions.
The main material for dielectric insulation is silicon oxide $\text{SiO}_2$, while silicon nitride $\text{Si}_3\text{N}_4$ is widely used as a protective barrier against moisture and ionic impurities (due to its higher density). To obtain a high-quality conformal coating of the VCSEL mesa-structure, we used the thermally activated method of CVD for $\text{SiO}_2$ deposition as a result of the oxidation of monosilane by oxygen.

The second VCSEL mesa has the height difference of about 0.5 $\mu$m and 0.2 $\mu$m. In order to completely cover this relief and to avoid the appearance of discontinuities in the dielectric film at the boundaries of mesastructures, a 0.5-$\mu$m thick $\text{SiO}_2$ layer was deposited in our case. Figure 8 shows images of the cross-section of mesastructures with an etching depth of 0.2 $\mu$m and 0.5 $\mu$m, coated with the 0.5 $\mu$m-thick $\text{SiO}_2$ layer, obtained using scanning electron microscopy (SEM). SEM analysis revealed the presence of inclusions in the $\text{SiO}_2$ film, the most likely associated with the formation of fine aerosil powder. A slight thinning of the film is observed on the walls of the mesastructures. In general, no critical defects or breaks were observed, which suggests the validity of this passivation method for the VCSEL technology.

Figure 8. SEM images of mesastructures with height of 0.2 $\mu$m (top) and 0.5 $\mu$m (bottom) coated with the 0.5 $\mu$m-thick SiO$_2$ layer.

7. Formation of ohmic contacts and contact pads of the VCSEL
Since both InGaAsP contact layers have the same type of conductivity (n-type), thus it is possible to form the ohmic contacts and contact pads in one process.

A contact is ohmic if there is no potential barrier between the semiconductor and the metal. It can be achieved in several ways described in [12]. Conventionally, the ohmic contacts can be divided into two types: alloyed and nonalloyed. The use of alloyed ohmic contacts in the VCSEL design under consideration is complicated by the proximity of the upper contact layer to the tunnel junction and quantum wells. For this reason, it is necessary to use a metal system that does not require subsequent alloying.

As the metallization for creating ohmic contacts, the Ti / Pt / Au metal system was chosen. This contact does not require subsequent annealing, since the potential barrier at the metal – semiconductor interface is practically absent.

The fabricated contacts must meet a number of requirements that provides the necessary output characteristics of the laser. The interfaces of the ohmic contacts should be smooth, the surface morphology should be smooth and has not defects in the form of metal inclusions. The specific contact resistance of the ohmic contacts should be lower than $1 \cdot 10^{-5}$ Ohm-cm$^2$.

Since the selected metal system does not require annealing, the topology of ohmic contacts can be formed using the method of “lift-off” photolithography. A two-layer mask was used, consisting of a lift-off resist layer and a positive photoresist top layer. Before the deposition of metals, the surface of the structure was processed in oxygen plasma to remove the remains of the undeveloped photoresist. Then, in order to remove oxides from the surface of the contact layers and reduce the resistance of the metal-semiconductor interface, the plate was processed in hydrofluoric acid. Immediately after removal of the oxides and drying of the plate, metal layers were deposited and a subsequent “lift-off” of metallization was made.

To measure the resistivity of the fabricated ohmic contacts, a test cells were formed on the processed structures, see figure 9a. These cells are designed to measure the resistivity of the fabricated contacts by the transmission line method (TLM) [13]. The calculation of the specific resistance value for both contacts is shown in figure 9b. The values of the contact resistance for a 20-thick n-InGaAsP contact
layer with doping ~1·10¹⁹ cm⁻³ and a 10 nm-thick n-InGaAsP contact layer with doping ~6·10¹⁸ cm⁻³ were estimated to be around 1·10⁶ Ohm·cm² and 3·10⁶ Ohm·cm², respectively, which justify the effectiveness of the suggested type of metallization.

Figure 9. Control of resistivity of ohmic contacts: a) Image of a test cell; b) calculation of specific contact resistance.

8. Characteristics of 1.55 μm VCSEL crystals
Figure 10a depicts the top view of the fabricated 1.55 μm wafer-fused VCSEL with the GSG-topology of the contact pads. The VCSEL contains the first mesa formed in the top DBR, the two-step second mesa formed in the top IC-layer and the active region, and the third mesa formed in the bottom IC-layer. The surface of the mesa structure is covered by the SiO2 layer with the opening in dielectric over the surfaces of the top and IC-layers. Anode and cathode contacts are formed to the surfaces of the top and bottom highly-doped contact InGaAsP layers.

SEM-image of the cross-section for the double-fused VCSEL heterostructure near optical microcavity is shown in figure 10b. By contrast of SEM-image, one can identify not only DBRs, IC-layers, active region, but also TJ layers, contact layers and fused interfaces. Note that there are no evidences of the formation of air cavities and micro-defects at the fused interfaces and the borders of the overgrown tunnel junction.

Figure 10. SEM-images of the fabricated 1.55 μm wafer-fused VCSELs: a) top view, b) cross-section. DBR, IC, TJ and BTJ denote distributed Bragg reflector, intra-cavity contact, tunnel junction and buried tunnel junction, respectively.

Figure 11a shows the typical static and spectral characteristics for the 1.55 μm wafer-fused VCSEL with 8μm BTJ diameter, measured in CW mode at various heat-sink temperature. The devices demonstrate efficient lasing with a threshold current less than 3 mA and slope efficiency of ~0.38 W/A. The VCSELs exhibit single-mode lasing with side-mode suppression ratio (SMSR) more than 30 dB over the entire current and temperature range. Note that lasing emission is polarized with orthogonal-polarization-suppression ratio more than 20 dB. The increase of temperature results in monotonic decrease of the maximum optical output power from 4.8 mW at 20°C down to 1.4 mW at 80°C, while the threshold current rises up to 6.6 mA. The strong impact of temperature on VCSEL performance can
be associated with the thermal escape of the carriers from the thin InGaAs QWs or small gain-to-cavity detuning.

Figure 10a shows the small-signal modulation response for of the 1.55 μm wafer-fused VCSEL with 8μm BTJ diameter, measured at 20 °C and at various current. The frequency response of the high-speed photodetector is subtracted from the laser response. The fabricated wafer-fused VCSEL demonstrates the classical response with single-resonance frequency over its entire operating current range. The -3dB modulation bandwidth reaches 8 GHz with a modulation current efficiency factor of more than 3.7GHz/(mA)^1/2, quickly saturates at about 9 GHz for higher currents and then drops down to 7.6 GHz for currents above rollover.

Figure 11. 1.55 μm wafer-fused VCSELs: a) CW light-current-voltage characteristics and lasing spectra (on inset) at various heat-sink temperatures; b) Measured small-signal modulation response and -3dB modulation bandwidth (on inset) for different currents at 20 °C.
9. Conclusion
The paper presents the fabrication technology of the 1.55 μm wafer-fused VCSELs. The hybrid VCSELs heterostructure was formed by direct wafer bonding of the InAlGaAsP/InP optical cavity heterostructure with the active region and two AlGaAs/GaAs DBR, fully grown by solid-source MBE.

To form the first VCSEL mesa and precisely open the surface of the top InGaAsP contact layer the dry etching of the top DBR via dielectric mask in the inductively coupled plasma was used. The two-step wet chemical etching of the optical cavity InAlGaAsP/InP in selective chemical etchants via photoresist mask was employed to form the second VCSEL mesa. For passivation and electrical isolation of the VCSEL mesa-structure the 0.5 μm-thick SiO2 layer were deposited by the thermally activated CVD. The Ti/Pt/Au metallization was used to achieve the ohmic contact to the highly-doped InGaAsP contact layers.

The developed VCSELs demonstrated effective lasing near 1.54 μm with threshold current less than 3 mA and output optical power more than 4.8 mW at the temperature of 20°C. The lasing spectra revealed the single-mode operation with SMSR more than 30 dB over the entire current and temperature range. According the small signal modulation response, the -3 dB modulation bandwidth reached ~8 GHz at a bias current of 10 mA.

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