Ultra Low Power 3D-Embedded Convolutional Neural Network Cube Based on $\alpha$-IGZO Nanosheet and Bi-Layer Resistive Memory

Sunanda Thunder$^1$, Parthasarathi Pal$^2$, Yeong-Her Wang$^2*$, Po-Tsang Huang$^1*$

$^1$International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu, Taiwan
$^2$Institute of Microelectronics, National Cheng Kung University, Tainan, Taiwan

email: $^1$bughuang@nctu.edu.tw, $^2$yhw@ee.ncku.edu.tw

Abstract—In this paper we propose and evaluate the performance of a 3D-embedded neuromorphic computation block based on indium gallium zinc oxide ($\alpha$-IGZO) based nanosheet transistor and bi-layer resistive memory devices. We have fabricated bi-layer resistive random-access memory (RRAM) devices with $\text{Ta}_2\text{O}_5$ and $\text{Al}_2\text{O}_3$ layers. The device has been characterized and modeled. The compact models of RRAM and $\alpha$-IGZO based embedded nanosheet structures have been used to evaluate the system level performance of 8 vertically stacked $\alpha$-IGZO based nanosheet layers with RRAM for neuromorphic applications. The model considers the design space with uniform bit line (BL), select line (SL) and word line (WL) resistance. Finally, we have simulated the weighted sum operation with our proposed 8-layer stacked nanosheet based embedded memory and evaluated the performance for VGG-16 convolutional neural network (CNN) for Fashion-MNIST and CIFAR-10 data recognition, which yielded 92% and 75% accuracy respectively with drop out layers amid device variation.

Keywords—RRAM, $\alpha$-IGZO, 3D-IC, Neuromorphic Computing, CNN.

I. INTRODUCTION

The thousands of terabytes of data produced every second by trillions of internally and externally connected edge devices needs to be processed, filtered, and categorized. Therefore, the necessity of artificial intelligence has once again been reinvigorated in our daily life along with the need for data-centric computing to reduce the overheads at data centers. Software based artificial intelligence algorithm and neuromorphic system, implemented using traditional digital or mixed circuits, suffer from Von-Neumann bottleneck due to the physical separation between the computing unit and the memory, and the bandwidth limitation inhibits the performance of a powerful processor rendering it idle most of the time. Recent advents in the research of emerging non-volatile memories (eNVM) such as resistive random-access memory (RRAM), magnetic random-access memory (MRAM) and ferroelectric random-access memory (FeRAM) have accelerated the research of neuromorphic computing with an aim to alleviate memory bandwidth bottleneck in Von-Neumann computing architecture [1-12].

The invention of True-North chip by IBM [13], Loihi from Intel [14] tells the trend. Apart from this trend of building neuromorphic chips, the recent trend of monolithic 3D-IC design has also heavily impacted the IC design sector [15]. Although there have been many proposals for monolithic 3D-integration of neuromorphic chips, an integration of 3D-IC with eNVMs for neuromorphic applications is still missing.

Fig.1 Stacked nanosheet based 3D computing in memory architecture provides energy, area and throughput efficiency over conventional CIM chip.

Among a many eNVMs resistive random-access RRAMs are one of the most promising candidates for neural network applications [16-21]. In this article we propose and demonstrate by simulation $\alpha$-IGZO based novel 3D-embedded RRAM tile with common WL and SL for neuromorphic computing (Fig.1). The paper starts with a discussion of modeling the $\alpha$-IGZO based nano-sheet transistors and RRAMs. We have found that $\alpha$-IGZO based nanosheet transistors are suitable for 3D-IC demonstration for neuromorphic computing. In the following section we discuss about the experiments and results, which is followed by discussion and conclusion.

II. EXPERIMENTS AND RESULTS

The 3D-stacked $\alpha$-IGZO based nano-sheet transistors have been modeled according to [22]. The complete physical model ranging from subthreshold to strong inversion can be described as

$$I_d(j) = \frac{W}{L} \omega_0 \frac{2}{\text{ez}} \frac{T}{2T_e} \left( V_c \left( \frac{V_{GS}(j)}{V_t} \right) \left( \frac{V_{GS}(j)}{V_t} \right) \right)^{2T_e}$$

$$I_{W11} = \sum_{j=1}^{n} I_d(j)$$

Where, $V_{GS} = V_o - V_T - V_S$, $V_{GS1} = V_o - V_T - V_{SL}$, $f(x) = \log [1 + \exp (x)]$ and $V_t = V_I / (2T_e - T)$. Fig. 2(a). shows the schematic of a single column cell and Fig.2(b) and Fig.2(c) shows the drain current from a single
nano-sheet layer for linear and saturation region. We have fabricated, characterized, and modeled bi-layer RRAM with 5 nm Ta2O5 and 2 nm Al2O3. Fig. 2(d) shows the I-V curve of resistive random-access memory, which has been modeled according to [23]. The pulse program erase operation in a single RRAM device showed 32 distinct states (not shown here), however in presence of device variation with σ=0.1, 32 states merge and only 3 distinct states are available.

After the characterization and modeling of a single column cell, we have simulated the multiply-accumulate operation in a single tile. The design space of a single tile has been considered according to [24]. The BL, WL and SL resistance has been calculated according to \[ \sigma \text{= 0.1, 32} \]. The I-V curve for bi-layer RRAM devices considered in this study. (e). The device to device variation in RRAM.

Following the circuit implementation of a single tile we have used this same tile-based network for evaluating the performance of convolutional neural network for recognizing the images from the F-MNIST and CIFAR-10 data set. We have used VGG-16 model here, which has been depicted in Fig.4(a). Rectified Linear Unit (ReLU) activation function has been used to each layer so that all the negative values are not passed to the next layer. Fig.4(a). shows the architecture of the CNN used in this work for evaluating the system level performance of the proposed 3D-synaptic device. The tile-based

To facilitate low power operation, “READ” operation has been conducted by applying on 0.5 V. The maximum “ON” current is 10 µA for 2V “WRITE” and 0.5V “READ”. The “WRITE” operation has been conducted by sending pulses through switch matrix circuit depicted in [25]. The “READ” operation has performed by charging a capacitor along with a high resolution 4-bit successive approximation analog to digital converter (SAR-ADC). The 4-bit ADC reduces the complexity of the peripheral circuit and reduces the power consumption.
architecture is shown in fig.4(b). The tile-based network serves two different purposes in this works.

1. Alleviation of design space IR- drop across BL, WL and SL.
2. Implementing drop out mechanism to avoid over fitting in training data.

The drop out is also an important mechanism in CNN, which helps avoiding the overfitting of the data. Dropout is a typical and simple mechanism that will randomly drop nodes from the network during training process. This is used to avoid over-fitting during training operation. In this work instead of dropping out nodes we drop out and entire column network from a single tile. During the training process, a pseudo random numbers were generated select the drop-out column in each tile.

Prior to drop out the training accuracy for FMNIST was 98%, whereas the inference accuracy was only 91%. Post drop-out the training accuracy was 93% and inference accuracy is 92%. The CIFAR-10 training accuracy was 81% and 75% inference accuracy has been achieved. Fig. 4(c) shows the inference accuracy for F-MNIST data set and fig.4(d) shows the inference accuracy for CIFAR-10 data set.

![Architecture of CNN considered during neuromorphic simulation.](image)

![The tile-based architecture considered in this work to minimize the I-R drop across the BL, WL and SL.](image)

![Inference accuracy for VGG-16 CNN.](image)

![Neuromorphic simulation shows that the proposed architecture can detect Fashion-MNIST data set with 92% accuracy.](image)

The tile-array-based accelerator performs VGG-16 CNN. Compared to a digital accelerator with the same quantitation (8b/4b for activation/weight) and channel pruning, the accuracy for F-MNIST data recognition is 92% and CIFAR-10 data is 75%. Table-I performs the system level bench marking of this work with other state of art works.

| This Work | [26] | [12] |
|-----------|------|------|
| # States  | 3    | 2    | 27   |
| $\sigma_{D2D}$ | 10%  | 5%   | 0.57833V |
| $R_{\text{on}}/R_{\text{off}}$ | $10^6$ | $4.2 \times 10^3$ | $10^5$ |
| Dataset   | CIFAR-10/ FMNIST | MNIST | MNIST |
| Accuracy  | 75% / 92% | 97.11% | 96% |

III. CONCLUSION

The newly proposed $\alpha$-IGZO based 3D memory was demonstrated to exhibit superior performance with high speed and incremental switching. According to the excellent electrical characteristics, a mini-array-based accelerator was further demonstrated with CONV-Net for objection detection. Instead of network-level weight stationary, this accelerator utilized layer-level weight stationary to reduce both area and energy by using 3D stacking. Moreover, standard or pointwise convolutions and channel pruning were supported by the channel-based weight mapping scheme with an accuracy of 92% for FMNIST data set and 75% accuracy with CIFAR-10 dataset.

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V. REFERENCE

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