Crossover Logic: A Low-Power Topology for Unipolar Dual-Gate Thin-Film Technologies

Florian De Roose, Student Member, IEEE, Jan Genoe, Member, IEEE, Wim Dehaene, Senior Member, IEEE, and Kris Myny, Senior Member, IEEE

Abstract—Crossover logic is a new topology for thin-film unipolar circuits combining the high speed of diode load logic (DLL) and the low power consumption of zero-\(V_{GS}\) logic during operation. It demonstrates a fivefold reduction in power consumption and a threefold increase in static noise margin, compared to DLL with backgate. It shows comparable area consumption, and a speed decrease of a factor 2.1. Furthermore, the topology is fully compatible with DLL, allowing combined use within one digital system. The performance is shown in individual gates, in ring oscillators and in a 4-bit adder system with scan-chain readout.

Index Terms—a-IGZO, logic, low power, thin-film, topology.

I. INTRODUCTION

Thin-film technologies are everywhere today, ranging from the TVs at home to the display of a smartwatch. Thin-film circuits have a lot of potential as a growing field, with recently shown innovations in low-cost NFC tags [1], gate drivers for displays [2], and sensor arrays for biopotential measurements [3]. The thin-film circuits which are closest to industrial implementation, like tags and gate drivers, rely heavily on the digital circuit blocks.

One of the major concerns with respect to designs today is the large power consumption of current digital blocks. On a system level, low power is a concern to enhance battery life for mobile displays or increase reading distance of tags. On a circuit/layout level, it reduces resistive losses in supply tracks of larger digital blocks.

The current high power consumption is due to the lack of complementary thin-film devices. Realizing complementary devices is either too expensive because of the extra mask layers, or simply not possible due to a lack of suitable semiconductor materials. This implies that digital blocks must be designed using only one type of transistor. This has consequences on power and robustness of digital blocks. Zero-\(V_{GS}\) load (ZVL), shown in Fig. 1(a), provides acceptable robustness, but at the cost of speed [4]. Pseudo-CMOS [5] was introduced, providing high robustness and speed, but at the cost of high power consumption and using four large transistors. To reduce cost, the area of logical cells should be as small as possible. If a transistor can be made with another threshold voltage (\(V_T\)) however, the smaller diode load logic (DLL) with backgate can be used [6]. This is shown in Fig. 1(b). This topology reduces area by using less transistors at the cost of slightly lower speed, but still consumes a lot of power.

Other topologies have been investigated, but all have drawbacks. Kim et al. [7] proposed to use dynamic logic, which increases the speed and reduces size, but at the cost of high sensitivity to threshold voltage and timing, and requiring complex clock distribution systems. Venturelli et al. [8] proposed to use differential logic for high static noise margin (SNM), but at the cost of no less then eight transistors per inverter. Papadopoulos et al. [9] finally, proposed a bootstrapped inverter with low power consumption, but this topology also uses five transistors per inverter.

This letter proposes an alternative topology, crossover logic, for digital blocks with substantially reduced power consumption for slight reduced speed. Since speed is essential in most systems, crossover logic can be used in combination with DLL and can be used in sections that are not critical with respect to speed, thereby reducing the overall power consumption of a system without sacrificing speed.

Fig. 1. Logic style of the inverters: (a) ZVL, (b) DLL with backgate, (c) crossover logic (COL), (d) crossover logic with a low input, and (e) crossover logic with a high input.

II. TECHNOLOGY

Crossover logic can be used in any thin-film transistor technology which has devices available with both the positive and negative threshold voltage and timing, and requiring complex clock distribution systems. Venturelli et al. [8] proposed to use differential logic for high static noise margin (SNM), but at the cost of no less then eight transistors per inverter. Papadopoulos et al. [9] finally, proposed a bootstrapped inverter with low power consumption, but this topology also uses five transistors per inverter.

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negative threshold voltages. Examples of potential technologies are amorphous silicon, organic semiconductors, oxide semiconductors, or low-temperature poly silicon (LTPS). These threshold voltages can be made different because of either intrinsic properties (doping, semiconductor, length, . . .) or because of the presence of a second gate, the backgate. To demonstrate the technical feasibility, we have fabricated and compared digital blocks with diode load, pseudo-CMOS, and the new topology in a dual-gate a-IGZO process. Here, the single-gate devices have a negative \( V_{T0} \) while the \( V_T \) of dual-gate devices can be shifted by \( V_{BG} \) to any \( V_T(\text{BGS}) \). Due to the \( V_{T0} \) of around –1 V and the \( V_{DD} \) of only 5 V, the pseudo-CMOS circuits have very low-noise margin, yielded no working circuits, and are therefore disregarded.

The process has been optimized for circuits, including a thin gate dielectric (100 nm) and symmetric front- and back-gate dielectrics. More details on the dual-gate a-IGZO process can be found in [10].

### III. Design

#### A. Operation

Crossover logic is a logical topology which combines the advantages of DLL and zero-\( V_{GS} \) logic in real time. The topology is shown in Fig. 1(b). The operating mechanism crosses over from the high-speed operation of diode load to the low-power operation of zero-\( V_{GS} \). The operation will be described for both states: low and high input.

When the input is low, the inverter operates like diode load, as shown in Fig. 1(c). The drive transistor (M1) is inactive, and the output is pulled high by the load transistor (M2). The static power consumption is determined by the leakage power of the drive transistor. Therefore, the drive transistor is designed with a high (positive) \( V_T(\text{BGS}) \), and the current consumption is very small. The pull-up is strong and the speed is high, because the gate of the load is connected to the supply.

When the input is high, however, the inverter operates like a zero-\( V_{GS} \) stage, as shown in Fig. 1(d). The drive transistor is active, and provides a strong pull-down, resulting in high speed. The gate of pull-up device is now connected to the source, and provides high impedance. Since the pull-down is very strong, the power consumption is determined by the zero-\( V_{GS} \) leakage of the pull-up, and is small.

Switching between diode load and zero-\( V_{GS} \) is done by a resistive divider made by transistors M3 and M4. When the input is low, the output is high, and the gate of the pull-up is virtually connected to the supply through M4. M3 is high-resistive and does not influence operation. When the input is high, the output is low, and the gate of the pull-up connected to the output through M3, enabling zero-\( V_{GS} \) operation. M4 is high-resistive and does not influence the operation.

The limiting factor with respect to speed is the transition from a high to a low input, due to the internal feedback. When the input is high, the pull-up device is put in high impedance mode. When transitioning to a low input, the pull-down device is also high-impedant. The leakage current of the pull-up device has to recharge the output until the feedback flips the operation mode of the load transistor. Therefore, there is a tradeoff between speed and power consumption, set by the off-current of the load transistor, which is set by its \( V_{T0} \). A higher off-current can recharge the output node more rapidly, but also leaks more when the input is high, increasing static power consumption. The \( V_{T0} \) of the pull-up devices must always be negative for proper operation. This also means that this topology has a higher sensitivity to the \( V_{T0} \), since it depends on the off-current of the pull-up, compared to the on-current of the pull-up for DLL.

#### B. Design Tradeoffs

The design of crossover logic comes with a few considerations. In our implementation, we generate the second \( V_T(\text{BGS}) \) by means of a backgate at a fixed voltage. The threshold voltage of a device with backgate is shifted linearly with the source voltage (\( V_S \)). Unless \( V_S \) is connected to a fixed potential (i.e., the ground), the \( V_T(\text{BGS}) \) will change during operation. For matching front- and back-gate dielectrics, the shift with respect to \( V_S \) is one to one. If \( V_S \) of the transistor changes by \( V_{DD} \), then the \( V_T(\text{BGS}) \) of that transistor will shift by \( V_{DD} \) too, effectively turning the transistors off. Therefore, we have designed M2, M3, and M4 without backgate.

Finally, size is comparable between both topologies. In DLL, the pull-down device has to be sufficiently large compared to the pull-up device, in order to overpower it, and effectively generate a zero. This ratioed logic usually requires the pull-down device to be ten times bigger than the pull-up. Crossover logic does not have to be ratioed, since the pull-up device is actively turned off in the pull-down state. This means that minimal sizes can be maintained, and only slightly more area is used, even though the number of transistors doubles for the inverter.

### IV. Simulation: Dependence on \( V_{T0} \) and Comparison

To compare the performance of the different topologies, we have simulated their operation depending on the \( V_{T0} \). \( V_{BG} \) was changed to keep the \( V_T(\text{BGS}) \) of the transistors with backgate at 0.5 V. We estimate the \( V_{T0} \) of our technology at around –1 V. The results for SNM, gate delay, and power consumption are shown in Fig. 2. DLL
has a very wide range of operation, while PC only works for positive $V_{T0}$s and ZVL, and COL work only for $V_{T0}$s between $-1.5$ V and 0 V. COL has the lowest power consumption, and the highest gate delay. Finally, it can be observed that COL and ZVL are more sensitive to the changes in $V_{T0}$ compared to PC and DLL.

To verify the behavior of the new topology, we have fabricated inverters, ring oscillators, logic gates, and a complex digital system for both DLL and COL. Fig. 3 shows the butterfly diagram for the inverters. COL yields much better signal levels and SNM, leaving a 30.6% window compared to 9.6% window at 5-V supply. In Fig. 4, the output voltage and power consumption of DLL and COL are compared. At 5-V supply with an input of 5 V, the static current consumption of COL is only 0.466 $\mu$A, compared to 2.56 $\mu$A for DLL, reducing the power consumption with more than a factor 5. Fig. 5 compares 19-stage ring oscillators with a buffer with very small input capacitance as a load. At 5 V, the power is reduced by more than a factor 5, while the speed loss is limited to around 2. It can also be observed that the variability for the COL is bigger. This can be explained by the sensitivity of the speed and power consumption on the $V_{T0}$ of the devices, as calculated in section IV. Measurements on the logic gates confirm the conclusions above.

Finally, a 4-bit adder was designed to verify the circuit behavior on a more complex design. To facilitate readout and allow accurate timing information, a scan chain was used to clock the data in and out. Furthermore, a double input register was used to allow comparing the transition between two specific input vectors. The schematic of this chip can be seen in Fig. 6. The actual chips can be seen in Fig. 7. The crossover logic chip (8.9 mm²) was slightly larger than
the diode load chip (7.8 mm²). At 5-V supply, the crossover logic chip was slower when transitioning from the 0 + 0 addition to the 1 + 15 addition (13 µs versus 8 µs), but used only one fifth of the power (1.25 mW versus 6 mW). A final comparison between the measurement results for DLL and crossover logic can be found in Table I.

VI. CONCLUSION

In the conclusion, we presented crossover logic, a new topology for dual-gate thin-film transistor technology with low-power consumption. The topology uses elements from DLL and zero-V GS logic, to combine the speed of DLL with the low-power properties of zero-V GS logic. With respect to DLL with backgate, the SNM is increased substantially, from 0.475 V to 1.572 V for a 5-V supply. Power consumption is reduced with a factor 5, while the decrease in speed is limited to a factor 2.1. Area for an inverter increases with only 32%, whereas a NOR 4 gate has the same size. The new logic style is also fully compatible with DLL. Finally, we have compared a 4-bit adder with scan-chain readout for both topologies, showing the integratability into larger systems.

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