Distributed Processing for Encoding and Decoding of Binary LDPC codes using MPI

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Abstract—Low Density Parity Check (LDPC) codes are linear error correcting codes used in communication systems for Forward Error Correction (FEC). But, intensive computation is required for encoding and decoding of LDPC codes, making it difficult for practical usage in general purpose software based signal processing systems. In order to accelerate the encoding and decoding of LDPC codes, distributed processing over multiple multi-core CPUs using Message Passing Interface (MPI) is performed. Implementation is done using Stream Processing and Batch Processing mechanisms and the execution time for both implementations is compared w.r.t variation in number of CPUs and number of cores per CPU. Performance evaluation of distributed processing is shown by variation in execution time w.r.t. increase in number of processors (CPU cores).

I. INTRODUCTION

Low Density Parity Check (LDPC) codes are a type of Error Correcting codes which were developed by Robert Gallager in early 1960s [1]. Currently, LDPC codes are used widely for Forward Error Correction (FEC) in current and next-gen wireless standards such as 5G, 802.11, etc, as well as in video broadcasting, due to their capacity approaching performance with increase in block length. But, with increasing block length, the computation time of encoding and decoding processes of LDPC codes increases leading to high latency and limitation in throughput. Considering the increasing usage of LDPC codes, and the current focus in 'softwarization' of front-end signal processing and networking elements for wireless systems, accelerating and distributing the computation for encoding and decoding of LDPC codes becomes important to achieve practical usage in next-gen software defined communication systems.

Over the years, various methods have been used for accelerating the processing of LDPC codes using general purpose hardware such as multi-core Central Processing Units (CPUs) and General Purpose Graphics Processing Units (GPGPUs). [2]–[10] use GPGPU, or a combination of GPGPU and OpenMP for acceleration of encoding and Sum-Product decoding of Binary LDPC codes. These papers also compare the GPGPU and multi-core CPU implementations in terms of acceleration provided. But the above papers show implementation of LDPC encoding and decoding on single CPU with shared memory parallelization model, and single GPGPU. While such systems provide good acceleration, it becomes difficult to distribute the processing to multi-server and multi-CPU systems. In such cases distributed memory mechanisms with message passing models can be used for ease of processing distribution over multiple CPUs for providing acceleration. LDPC encoding and decoding using message passing model has not been implemented or evaluated as much. In [11] distributed LDPC decoding is done using MPI, but it aims at optimization of coarse grain graph search problem to select the LDPC Parity Check matrix with least Bit Error Rate (BER). It does not evaluate the computational performance of encoding and decoding LDPC codes.

In this paper, we use distributed memory message passing model by using Message Passing Interface (MPI) to distribute the encoding and Sum-Product decoding processes of LDPC codes over multiple multi-core CPUs. We perform the processing using Stream Processing and Batch Processing mechanisms. We show the acceleration provided by using message passing model for both mechanisms, and compare the execution time required for processing w.r.t. increase in number of CPUs and cores per CPU.

The paper is organized as follows. Section [II] describes the theoretical background related to encoding and decoding of LDPC codes. Section [III] describes the various components used for experimental evaluation, and it explains the distributed implementation for each part of the algorithms mentioned in Section [II]. Section [IV] shows the results of the various experiments conducted. Lastly, Section [V] concludes the paper and states future directions to be taken.

II. THEORETICAL BACKGROUND

We consider a vector \( m \) of \( k \) information bits \( [m_1, m_2, \ldots, m_k] \). Using LDPC codes, \( k \) information bits can be encoded into a vector \( p \) of \( n \) bits \( [p_1, p_2, \ldots, p_n] \), with \( n \geq k \). The \( n \) bits consist of \( k \) information bits from vector \( m \) and \( n - k \) parity bits. So the rate of code is defined as \( \text{Rate}(R) \geq k/n \). Here, \( n > k > 0 \).

The parity bits are formed by a linear combination of the \( k \) information bits known as parity check equations. LDPC codes are defined by putting these parity check equations in
LDPC codes by using the equation, the null space of the Parity Check matrix. Then, by using the sum-product algorithm description in detail. We explain the gist of the algorithm. For decoding, a bipartite graph Fig. 1: Bipartite graph for decoding of LDPC codes for a random (2, 4) Parity Check matrix with n = 8 and Rate(R) \geq 1/2 a Parity Check matrix, denoted by H, which is a \( k \times (n-k) \) matrix. Each row of H denotes a parity check equation \( c \), and each column defines whether a bit from the vector \( p \) is present in the parity check equation or not. Depending on the number of ones in each row and column, the Parity Check matrix is defined as \( (n_c, n_v) \), where \( n_c \) is the number of ones per row, and \( n_v \) is the number of ones per row. Then, the rate of code can be defined as \( \text{Rate}(R) \geq 1 - n_v/n_c \). LDPC codes with this type of matrix are known as regular LDPC codes.

A. LDPC Encoding

From Eq. 1, we can say that each codeword is present in the null space of the Parity Check matrix. So, we form the Generator matrix \( G \), which is a \( k \times n \) matrix, for encoding of LDPC codes by using the equation,

\[
H G^T = 0
\]

(1)

Where \( T \) denotes transpose of a vector or a matrix. This means that the additional parity bits must take values 0 or 1 such that each parity check equation equals 0.

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\[
H G^T = 0
\]

(2)

A Generator matrix is created by using Eq. 2 i.e. by finding the null space of the Parity Check matrix. Then, by using the Generator matrix encoding of the input information bits can be done using,

\[
m^T G = p^T
\]

B. LDPC Decoding

We have taken the steps of Sum-Product decoding algorithm from [1], [12]–[14]. The aforementioned papers contain the sum-product algorithm description in detail. We explain the gist of the algorithm. For decoding, a bipartite graph \( G(V, C, E) \) is created from the Parity Check matrix, where \( V \) is a set of \( n \) variable nodes with index \( v \), \( C \) is a set of \( n-k \) check nodes with index \( c \). If there is a 1 on the \( i^{th} \) row and \( j^{th} \) column of the Parity Check matrix, an edge connects the \( i^{th} \) check node and \( j^{th} \) variable node. An example is shown in Fig. 1. We represent the variable nodes using \( v \) and check nodes using \( c \). The variable nodes and check nodes transfer messages and update Log-Likelihood Ratio (LLR) values of each bit. These LLR values are input to the variable nodes as,

\[
L_v = R_v = \frac{\text{prob}(\text{bit}_v = 1)}{\text{prob}(\text{bit}_v = 0)} = \frac{2 y_i}{\sigma^2}
\]

(4)

where \( L_v \) is the total LLR value and \( R_v \) is the input LLR value of node \( v \), prob(.) is the probability value, \( y_i \) is the received noisy bit value, \( \sigma^2 \) is the Additive White Gaussian Noise (AWGN) power at the receiver. These LLR values are sent to all the check nodes connected to each variable nodes. After the check nodes receive the LLR values, the check node values are updated using the equation,

\[
E_{cv} = \log_e \left( \frac{1 + \sum_{\tilde{c} \in C, \tilde{c} \neq c} \tanh(L_{\tilde{c}_v}/2)}{1 + \sum_{\tilde{v} \in V, \tilde{v} \neq v} \tanh(L_{\tilde{v}_c}/2)} \right)
\]

(5)

where \( E_{cv} \) is the partial LLR update that each check node \( c \in C \) calculates for variable node \( v \), and \( L_{\tilde{c}_v} \) is the partial LLR update each variable node \( v \) calculates for check node \( c \) using the value from Eq. 5.

\[
L_{cv} = \sum_{\tilde{c} \in C, \tilde{c} \neq c} E_{\tilde{c}v} + R_v
\]

(6)

After a predefined number of iterations, using the values gained from Eq. 5, the total LLR value is calculated using equation,

\[
L_v = \sum_{c \in C} E_{cv} + R_v
\]

(7)

and then a hard-decision for each bit is made using,

\[
z_v = \begin{cases} 
1 : L_v \geq 0 \\
0 : L_v < 0 
\end{cases}
\]

(8)

where \( z_v \) is the final bit value for variable node \( v \).

III. IMPLEMENTATION DETAILS

A. Components used for implementation

1) ORBIT Testbed: Open-Access Research Testbed (ORBIT) is a large-scale academic indoor wireless testbed consisting of a 20x20 grid of computing nodes, more than 100 Software Defined Radios (SDRs), and a set of inter-connected servers for large-scale distributed computing and high performance computing applications. All components are connected to a centralized server system using which control functions and data transfer can be performed. More information related to the testbed can be found in [15], [16].
2) Intel(R) Xeon(R) CPU E5-2698 v3 @ 2.30GHz: This CPU has 16 physical cores and 32 logical cores. It has a base frequency of 2.3 GHz and max turbo frequency of 3.6 GHz, maximum memory bandwidth of 68 GBps with a 40 MB cache for fast memory access. More information can be seen at [17]. We use 2 server nodes, each consisting of 2 CPUs. These server nodes are present in ORBIT testbed. Both servers are connected using a 25 Gigabit ethernet link which will be utilized when multi-server distributed processing is implemented.

3) MPI: MPI is a standardized interface for message passing between processors in applications running on distributed memory systems. MPI can be used by processes running independently on clusters of multiple CPUs for communicating with each other and passing data using messages. We use MPICH [18], an open-source and widely portable implementation of MPI standard for distributing the processing among multiple cores and multiple servers. Some communication routines which are used in this paper for implementation are,

- **MPI_Send():** Used to send data from a specific process to another.
- **MPI_Recv():** Used to receive data from a specific process.
- **MPI_Gather():** Used to gather data from all processes to one. Each process can contain variable amount of data to be gathered.
- **MPI_Bcast():** Used to broadcast data from one process to all other processes.

### B. Distributed Stream Processing implementation

In Stream Processing, a single vector from a stream of multiple vectors is computed in a distributed manner. The data within each vector is distributed among multiple processors which perform computations and then the result is gathered in the master processor. We assume the availability of $N_{proc}$ processors denoted by Proc(0), Proc(1), ..., Proc($N_{proc}$−1), where Proc(x) means processor with index x. The division of elements to be processed among the processors is done in the following manner,

$$\text{NumElems}(q) = \left\{ \begin{array}{ll}
\text{floor}(N_{proc}/l) + 1 & : x < N_{proc} \% l \\
\text{floor}(N_{proc}/l) & : x \geq N_{proc} \% l
\end{array} \right. \quad (9)$$

where $\text{NumElems}(q)$ represent the number of elements to be given to processor $q$, $a \% b$ means the remainder of $a/b$, and $l$ is the total number of elements to be divided.

1) **Encoding:** For encoding, we use the Generator matrix which is converted to standard [I_k : P] where I_k sub-matrix is a $k \times k$ identity matrix formed by column permutations of Generator matrix, and P is a sub-matrix consisting of remaining $k \times (n-k)$ values of the Generator matrix. The input information bits $m_1, \ldots, m_k$ are first copied to the output vector bits $p_1, \ldots, p_k$ for each processor. Then, the columns of the P sub-matrix of the Generator matrix are divided among the $N_{proc}$ processors using Eq. (9) An example of division of 4 columns of the P matrix is shown in Fig. 2 Each processor selects a subset of columns from the $k$ columns of sub-matrix $P$. Each processor then takes the input vector $m$ and multiplies it with the columns of sub-matrix $P$ selected by that processor. The partial output calculated by each processor is then gathered at the master processor by using the **MPI_Gather()** command for further processing. The encoded bits are then converted to Binary Phase Shift Keying (BPSK) form for transmission through AWGN channel. For BPSK, we convert the 0 bits to −1 and 1 bits remain as 1.

2) **Decoding:** For Sum-Product Decoding, we create a graph and an adjacency list of the H matrix as shown in Section 4B. Now, for each iteration of the decoding algorithm, we first divide the variable nodes and check nodes among all processors in an interleaved manner. For each iteration the processors calculate the partial LLR values $E_{cv}$ of check nodes for which the check node index $c \% N_{proc} = x$ using Eq. (5) Then, after all processors have calculated their respective updated values, each processor sends the updated value of check nodes only to the processor with variable node index $v \% N_{proc} = x$. In the same way, the variable node LLR values are updated and sent. An example of communication between processors to update LLR values is shown in Fig. 5. The decoding algorithm runs for preset number of iterations after which the variable nodes update their final LLR values and hard decision decoding is done using Eq. (8) The complete Distributed Sum-Product Decoding is shown in Algorithm 1. The LLR updation steps and the LLR transfer steps are...
Algorithm 1 Distributed Sum-Product Decoding using MPI

1: Define \( V \) and \( C \) as sets containing variable nodes \( v \) and check nodes \( c \) respectively, \( E_{cv}, L_{vc}, L_v, R_v, z_v, N_{proc}, \) \( Proc(x) \)
2: Divide the check and variable nodes to all processors in an interleaved manner
3: for \( v \in V \) do
4:   Find the initial LLR values \( L_v \) and \( R_v \) and broadcast to all processors using \( MPI_{Bcast}(\)\)
5: end for
6: for \( i = 1 \) to \#iterations do
7:   // Updating LLR values at check nodes
8:   for \( (c = 0; c < |C|; c = c + N_{proc}) \) do
9:     Find \( E_{(c+x)c} \)
10: end for
11: for \( (c = 0; c < |C|; c = c + 1) \) do
12:   Send to processor which has the variable node \( v \) in its list, (i.e. \( Proc(v\%N_{proc}) \), using \( MPI_{Send}(\)\)
13: end for
14: end for
15: // Updating LLR values at variable nodes
16: for \( (v = 0; v < \text{size of } V; v = v + N_{proc}) \) do
17:   Find \( L_{(v+x)c} \)
18: end for
19: for \( (v = 0; v < |V|; v = v + 1) \) do
20:   Send to processor which has the check node \( c \) in its list, (i.e. \( Proc(c\%N_{proc}), \) using \( MPI_{Send}(\)\)
21: end for
22: // Calculating final LLR values and then performing hard-decision decoding
23: end for
24: for \( (v = 0; v < |V|; v = v + N_{proc}) \) do
25:   Calculate \( L_v+v \)
26: end for
27: Broadcast output to all processes using \( MPI_{Bcast}(\)\)
28: Calculate \( z_v+v \) value
29: Gather at master processor using \( MPI_{Gatherv}(\)\)
30: end for

separate for all processors. This separation ensures minimum switching between computation and communication for all processors.

C. Distributed Batch Processing implementation

Batch Processing here means each processor takes a batch of vectors for encoding or decoding, and the number of total vectors of information bits is greater than the number of processors.

1) Encoding: Now, for encoding, we assume an input vector \( M \) which is a \( kN_c \) length input vector consisting of \( k \) length vectors. Here \( N_c \) is the number of \( k \) length vectors to be encoded. The \( M \) vector divided into smaller vectors of size \( k \) which are then distributed among all processors. Each processor then uses Eq. \( 3 \) to encode the batch of \( k \) length \( m \) vectors. The output of the batch of vectors at each processor is then gathered in the master processor using \( MPI_{Gatherv}(\)\). The distribution of vectors is done using Eq. \( 9 \) where \( l = N_c \).

2) Decoding: For decoding, a noisy vector of length \( nN_d \) is taken, where \( N_d \) is the number of vectors to be decoded. This vector is then divided into multiple \( n \) length vectors which are distributed to multiple processors using Eq. \( 9 \) Then, each processor performs Sum-Product decoding, as shown in Section II-B, on the batch of \( n \) length vectors in a serial manner. The decoded output is then gathered in the master processor using \( MPI_{Gatherv}(\)\).

IV. EXPERIMENTS AND RESULTS

The parameters used for performing experiments are shown in Table I. For the experiments, we design the Parity Check
We design \( (N_c, 12) \) Parity Check matrix where \( N_c \) is dependent on the code rate. Based on the designed matrix, encoding and decoding is performed as shown in previous sections. We conduct experiments in two parts. Firstly, we distribute the processing on a single server consisting of two CPUs. Secondly, we distribute the processing among all processors of two such servers. For both cases, we compare Stream Processing and Batch Processing based on the execution time taken for processing of a single input vector. To get per-vector execution time, the total execution time is divided by the number of vectors.

### A. Single server case

The execution time for distributed processing on multiple processors of a single server consisting of two CPUs is shown in Fig. 4. The difference in execution time between Stream and Batch Processing starts increases as the number of processors increase. Batch Processing starts performing better than Stream Processing because the processors only communicate for taking the input vector and giving the output vector. While for Stream Processing, the processors communicate after encoding each vector, and during each iteration of decoding of each vector. Also, when the number of processors is increased beyond the maximum logical cores per CPU, the performance of Stream Processing either saturates or worsens due to the added latency of inter-CPU communication.

Even though Batch Processing has lesser execution time per vector, if high efficiency in utilization of hardware resources is to be maintained, the number of vectors to be processed must always be greater than the number of processors. So, the initial latency of Batch Processing can be higher than Stream Processing when higher utilization efficiency is to be
maintained.

B. Two server case

The execution time for distributed processing on multiple processors of two servers, with two CPUs each, is shown in Fig. 5. For two servers case, the x-axis of Fig. 5 shows the number of processors used per server. Which means that if the x-axis shows 4 then 4 processors are being used per server i.e. total of 8 processors are being utilized. It can be seen that Batch Processing performs better than Stream Processing, especially for decoding, due to the minimal communication latency between processors. Also, the performance of Stream Processing using two servers for decoding is approximately an order of magnitude worse than performance of Stream Processing using a single server, and for encoding the performance worsens with increase in number of processors. So, for multi-server scenario, due to the high communication latency between servers, Stream Processing performance is dependent on the speed of inter-server communication link.

Since the communication between processors in Batch Processing is much slower than the computation per processor, its dependence on the type of inter-server communication link is lesser as compared to that of Stream Processing, giving higher acceleration. Performance for decoding using Distributed Processing for two server case is either similar to or better than that of single server case with increase in number of processors. Performance of encoding using Distributed Processing for two server case is still worse than that of single server case. This is due to the computation time being negligible as compared to communication time.

V. CONCLUSION AND FUTURE WORK

Considering the intensive computation required for processing of LDPC codes, we used MPI to distribute the processing over LDPC codes over multiple multi-core CPUs. Using the distributed implementation, acceleration was provided for encoding and decoding processes of LDPC codes. Evaluation and comparison for Stream processing and Batch Processing based mechanisms for distributed processing of LDPC codes was done, and the advantages and limitations of both methods were shown.

While using a distributed memory based message passing model for distributed processing provides acceleration, increasing the number of processors to more than the logical cores in the system adds high processing latency as well as inter-processor communication latency due to context switching between processes. Also, for multi-server systems, the processing latency is highly dependent on the type of communication link between servers. So, to decrease the dependence on communication between CPUs, combination of shared memory and distributed memory based systems will be considered for distributed processing of LDPC codes.

REFERENCES

[1] https://web.stanford.edu/class/ec388/papers/ldpc.pdf