Diffusion Stop-Layers for Superconducting Integrated Circuits and Qubits with Nb-based Josephson Junctions

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Abstract—New technology for superconductor integrated circuits has been developed and is presented. It employs diffusion stop-layers (DSLs) to protect Josephson junctions (JJ) from interlayer migration of impurities, improve JJ critical current ($I_c$) targeting and reproducibility, eliminate aging, and eliminate pattern-dependent effects in $J_c$ and tunneling characteristics of Nb/Al/AlO$_x$/Nb junctions in integrated circuits. The latter effects were recently found in Nb-based JJs integrated into multilayered digital circuits. E.g., it was found that Josephson critical current density ($J_c$) may depend on the JJ’s environment, on the type and size of metal layers making contact to niobium base (BE) and counter electrodes (CE) of the junction, and also change with time. Such $J_c$ variations within a circuit reduce circuit performance and yield, and restrict integration scale. This variability of JJs is explained as caused by hydrogen contamination of Nb layers during wafer processing, which changes the height and structural properties of AlO$_x$ tunnel barrier. Redistribution of hydrogen impurities between JJ electrodes and other circuit layers by diffusion along Nb wires and through contacts between layers causes long-term drift of $J_c$.

At least two DSLs are required to completely protect JJs from impurity diffusion effects – right below the junction BE and right above the junction CE. The simplest and the most technologically convenient DSLs we have found are thin (from ~ 3 nm to ~ 10 nm) layers of Al. They were deposited in-situ under the BE layer, thus forming an Al/Nb/Al/AlO$_x$/Nb penta-layer, and under the first wiring layer to junctions’ CE, thus forming an Al/Nb wiring bi-layer. A significant improvement of $J_c$ uniformity on 150-mm wafer has also been obtained along with large improvements in $J_c$ targeting and run-to-run reproducibility.

Index Terms—Nb Josephson tunnel junctions, superconducting digital circuits, superconducting integrated circuits, superconducting qubits, hydrogen in niobium

I. INTRODUCTION

SUPERCONDUCTING digital electronics is predominantly based on Rapid Single Flux Quantum (RSFQ) logic. Performance and operation margins of RSFQ circuits are very sensitive to circuit parameter spreads, especially to variations in the values of critical currents of Josephson junctions comprising the circuits. Therefore, the main requirement to high-yield manufacturing technology for superconducting digital circuits is to reproducibly deliver Josephson junctions having minimal deviations of critical currents, $I_c$, from the $I_c$ required by the circuit design and optimization. The most advanced fabrication technology capable of superconducting very large scale integrated (VLSI) circuits has been Nb-based technology that utilizes Nb/Al/AlO$_x$/Nb Josephson junctions and multiple layers of Nb for circuit inductors, interconnects, and signal routing.

It has been found recently that in Nb circuits, in addition to small and random variations of critical currents of JJs, there can exist large and systematic deviations of critical currents of JJs from the expected (design) values [1]-[4]. The former are caused by statistical fluctuations in the junction area and tunnel barrier transparency, and can be characterized by a standard deviation, $\sigma_{I_c}$. The latter means that the value of $I_c$ deviation in a specific junction or a group of junctions, though varies from run to run, many times exceeds $\sigma_{I_c}$, so the probability of this happening as a result of random fluctuations is statistically negligible. For instance, we have found that the $J_c$ in a JJ may depend on how the junction is connected to other circuit layers and on the area and shape of the contacting layers [1]-[2], whether the junction base electrode (BE) or counter electrode (CE) makes contact to Nb ground plane layer M0 [1]-[2], on the distance between the junction and the contact hole to other layers, and on the number of contact holes [3]. We have also found recently that the critical current density and the gap voltage increase over time in junctions stored at room temperatures if one or both of the junction electrodes are connected by Nb wire to Ti/Au or Ti/Pd/Au contact pads or just covered by a layer of Ti [4]. The effect is larger if CE is connected to a Ti-coated layer than if BE is connected.

The described above dependences of Josephson junction properties on the junction’s environment and circuit patterns have been explained as resulting from hydrogen contamination...
of Nb circuit layers during wafer processing, with its subsequent migration towards or away from the AlOₓ tunnel barrier during the manufacturing cycle and later on upon its completion [3]-[6]. Long-term changes in Ic were first found in Nb circuits with Pd coating [5],[6] and were suggested to be caused by hydrogen absorption and desorption.

It is well known that bulk Nb and Nb films can dissolve large amounts of hydrogen at room temperature, up to c_{H} \sim 50 atomic percent, where c_{H} is the hydrogen content (H/Nb ratio). Hydrogen is the most mobile impurity [7]. Its diffusion coefficient in Nb at 300 K is D \sim 10^{-5} cm²/s; and diffusion activation energy is 0.106 eV, the lowest of all impurities (next is oxygen with the activation energy \sim 1 eV [8]).

Dissolved hydrogen changes many physical properties of Nb, e.g., it increases the lattice constant, resistivity, etc. (for a review, see [9]). Most importantly, it increases the work function of hydrogen-contaminated niobium, Nb(H), with respect to the clean Nb [10],[11]. As a result, the average height of the tunnel barrier in Nb/Al/AlOₓ/Nb junctions and the barrier asymmetry become dependent on the c_{H} in the CE near the tunnel barrier, as was proposed in our work [4] (see also [6]). As was also emphasized in our previous works, Nb base electrode in real Josephson junctions is coated by a thin Al layer which is only partially consumed by the oxidation forming AlOₓ tunnel barrier. As a result, the tunnel barrier in Nb/Al/AlOₓ/Nb junctions is asymmetric (trapezoidal). The barrier height on the BE side, \phi_{BE}, is determined by the work function of Al, and the barrier height on CE side, \phi_{CE}, is determined by the work function of Nb, resulting in \phi_{CE} > \phi_{BE}. [12]-[14]. Therefore, the presence of hydrogen in Nb base electrode has no effect on the tunnel barrier height and hence has much less effect on the critical current density of Josephson junctions than hydrogen dissolved in Nb counter electrode, as was explained in our work [4] (see also [6] and our work [15] in the present issue).

In addition to a reversible effect on Nb work function, it is possible that hydrogen can chemically react with the AlOₓ barrier and cause irreversible changes to its properties, e.g., create states with high transmission probability. Because diffuson of dissolved hydrogen in an integrated circuit occurs on a complex network of Nb wires interconnecting multiple junctions, resistors, and inductors, all with different diffusion coefficients and cross sections, complex concentration distributions may appear and depend on details of a particular circuit design. This can affect different circuits in a different, though always negative, and quite reproducible manner.

Obviously, in ideal technology hydrogen poisoning of Nb circuits should never happen. However, developing and maintaining this ideal technology can be very costly or it may not exist. Therefore, in this paper we propose and demonstrate a new technology in which Josephson junctions are protected from the effects of hydrogen (and other impurity) poisoning and interlayer migration by diffusion stop-layers.

In the following sections we discuss how and when hydrogen contamination of Nb layers of integrated circuits can happen during wafer processing. Then we describe our innovation and present experimental results demonstrating its success in eliminating pattern-dependent effects and variability of Josephson junctions as well as improving Jc uniformity on 150-mm wafers and run-to-run reproducibility.

II. HYDROGEN CONTAMINATION OF Nb CIRCUITS: HOW, WHERE AND WHEN

Theoretically, H₂ concentration in air at atmospheric pressure is sufficient to saturate Nb with hydrogen at room temperature. The Nb surface presents a potential barrier for H₂ molecules and the native oxide on the surface works as a diffusion barrier, both prevent hydrogen absorption. However, in all situations when the surface oxide is removed hydrogen can easily dissolve in Nb. Hydrogen contamination can also occur because of the reaction with water molecules (in water, aqueous solutions, and moist air)

\[
\text{Nb} + \text{H}_2\text{O} = \text{NbO} + \text{H}_2, \tag{1}
\]

and due to a charge transfer process on a clean Nb surface

\[
\text{H}_2\text{O} + e^- \rightarrow \text{OH}^- + \text{H}, \tag{2}
\]

forming highly active atomic hydrogen which easily dissolves in Nb. Processes such as chemical etching, reactive ion (plasma) etching, chemical mechanical polishing (CMP), ion milling of Nb remove surface oxide and, hence, can produce hydrogen contamination.

During Nb film deposition by sputtering or other methods, hydrogen contamination can easily occur if there is sufficient residual hydrogen or water pressure in the vacuum chamber. After the deposition, hydrogen contamination is possible upon removing the deposited Nb film from the vacuum chamber because the clean surface of a freshly deposited film can readily react with air moisture.

In order to determine which integrated circuit fabrication steps result in hydrogen contamination of Nb layers in our process, we employed the following monitoring methods:

a) residual stress, \sigma, measurements of all metal layers after each process step;

b) electrical resistivity, \rho, measurements of all metal layers after each processing step;

c) optical emission spectroscopy (OES) of hydrogen lines during reactive ion etching (RIE) of all metal layers;

d) mass spectrometry during argon ion milling;

e) post-processing electrical characterization of test junctions and arrays of junctions with various connections to circuit layers, in the superconducting state at 4.2 K.

Absorption of hydrogen causes lattice expansion. Because Nb films are clamped to the substrate, absorption of hydrogen creates residual stress. For a clamped, (110)-textured Nb (as our films) the theoretical compressive biaxial stress increase is \Delta \sigma/c_{H} = -9.6 GPa. Somewhat lower values of \Delta \sigma/c_{H} in the range from -6.5 GPa to -9 GPa were observed [9],[15], apparently due to a partial stress relaxation. Therefore, method a) allows for a nondestructive way of checking for hydrogen contamination and estimating its magnitude.

From numerous electrical measurements on bulk and thin film Nb, it is known that hydrogen impurities increase electrical resistivity of Nb with partial contribution \Delta \rho/c_{H} in the range from 0.6 to 0.7 \mu\Omega cm per at.%. Therefore, a measured change in the resistivity of Nb layer after processing
Our standard 11-layer fabrication process was described in detail in [16], [17]. Its cross-section is presented in Fig. 1 for a resistively-shunted JJ. In Table 1, we list the sequence of processing steps and show the parameters which were monitored (marked with + sign) in order to detect possible hydrogen contamination, and mark those processing steps after which substantial changes were detected either in the properties of the layers or in the tunneling characteristics of JJs.

![Resistively-shunted Josephson junction. JJ is biased via a resistor connected by M2 and M3 wires to contact pads. JJ's BE is connected to Nb ground plane layer M0.](image)

A small change in the residual stress was observed after counter electrode etching, which defines junctions, in comparison with the wafer state after Nb/Al/O₂/Nb quad-layer formation. No significant hydrogen optical emission intensity was observed during the RIE. Since JJs occupy a very small total area on the wafer, residual stress after etching represents mainly the stress in the base electrode plus Al/O₂ structure. Therefore, from the total stress in Nb/Al/O₂/Nb quad-layer and the observed change we can calculate individual stresses in the counter electrode and in the Nb/Al/O₂ base electrode structure. These data will be presented elsewhere.

By far the largest changes in the residual stress were observed after Ar ion milling of the ~36-nm-thick anodization layer on the surface of junction base electrode layer, as shown in Fig. 2. This anodization layer is formed all over the exposed wafer area right after CE etching and is needed to seal junctions’ interior and form a protective layer of Nb₁₀/O₅ around junctions’ perimeter. Since only a small area of anodization around the junctions is needed (defined by Al layer photolithography), the rest of the anodized area is removed using a neutralized beam of Ar ions (ion milling). This process is done in a cryopumped chamber with base pressure lower than 1x10⁻⁷ Torr using a Kaufman source and rotating wafer for uniformity.

The change in the stress after anodization is consistently small and reproducible with the average increase of only 18.0

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**TABLE 1 Fabrication Steps and Monitored Parameters**

| Step | Processing Step Description | Monitored Parameters | Change Anode Ge S | OES | y/n |
|------|----------------------------|---------------------|------------------|-----|-----|
| 1    | Nb ground plane deposition, layer M0 | +                    | +                |   | +   |
| 2    | M0 layer photolithography and RIE in SF₆ | +                    | no               |   | -   |
| 3    | SiO₂ interlayer dielectric deposition, layer I0 | +                    | no               |   | -   |
| 4    | I0 layer photolithography and RIE in CHF₃/O₂ mixture | +                    | yes              |   | -   |
| 5    | Nb/Al/AlO₂/Nb quad-layer formation by deposition and Al oxidation | +                    | yes              |   | -   |
| 6    | Counter electrode photolithography and RIE in SF₆ | +                    | yes              |   | -   |
| 7    | Anodization in ammonium pentaborate in ethylene glycol solution, forms layer A1 | +                    | yes              |   | -   |
| 8    | A1 layer photolithography and Ar ion milling, forms layer M1 | +                    | no               |   | -   |
| 9    | Layer M1 (junction base electrode) photolithography and RIE in SF₆ | +                    | yes              |   | -   |
| 10   | SiO₂ dielectric deposition, layer 11B-1 | +                    | no               |   | -   |
| 11   | Molybdenum resistor layer deposition, layer R2 | +                    | no               |   | -   |
| 12   | Layer R2 photolithography and RIE in SF₆ | +                    | no               |   | -   |
| 13   | SiO₂ dielectric deposition, layer 11B-2 | +                    | no               |   | -   |
| 14   | Layer 11B-2 (11B-1) + (11B-2) photolithography and RIE in CHF₃/O₂ mixture, contact holes to BE and CE of JJs | +                    | yes              |   | -   |
| 15   | Nb wiring layer deposition, layer M2 | +                    | yes              |   | -   |
| 16   | Layer M2 photolithography and RIE in SF₆ | +                    | no               |   | -   |
| 17   | SiO₂ dielectric deposition, layer I2 | +                    | no               |   | -   |
| 18   | Layer I2 photolithography and RIE in CHF₃/O₂ mixture, contact holes to layer M2 | +                    | no               |   | -   |
| 19   | Nb second wiring layer deposition, layer M3 | +                    | yes              |   | -   |
| 20   | Layer M3 photolithography and RIE in SF₆ | +                    | no               |   | -   |
| 21   | Ti/Au or Ti/Pd/Au chip contacts metallization deposition and patterning by lift-off, layer R3 | +                    | yes              |   | -   |

Monitored parameters are electric resistivity, ρ, residual films stress, σ, and the intensity of optical emission spectra (OES) of hydrogen. By bold “yes” shown steps after which substantial changes in the properties of circuit layers and/or Josephson junctions have been observed.
The thickness of the removed layer is \( \approx 40 \text{ nm} \).

After its anodization at 21 V (●), we get a somewhat larger average value of \( \rho \) compared to using the theoretical value of \( \Delta \sigma/c_H = -65 \text{ MPa per at.\%} \) [15], we get a somewhat larger average value of \( c_H \). This clearly indicates that something happens to Nb films during Ar ion milling and that the amount of this something varies from run-to-run.

We assume that the increase in compressive stress after Ar ion mill is the result of hydrogen absorption by Nb layers. Then, using the theoretical value of \( \Delta \sigma/c_H = -96 \text{ MPa per at.\%} \), we get a somewhat larger average value of \( c_H \) than the estimate from the compressive stress induced by anodization. The thickness of the removed layer is \( \approx 40 \text{ nm} \).

The thickness of the removed layer is approximately 40 nm. After removing this anodization layer by Ar milling, the stress in the remaining Nb film moves towards highly compressive, independently of the initial stress in the Nb/Al/AlO\(_x\) multilayer. The average increase is -65.6 MPa and run-to-run variation is very large, \( sd = 47.7 \) MPa (73%). This clearly indicates that something happens to Nb films during Ar ion milling and that the amount of this something varies from run-to-run.

Fig. 2. Change in the residual stress in Nb/Al/AlO\(_x\) (BE+barrier) structure after its anodization at 21 V (●), and after Ar ion milling that removes the anodized layer from \( \approx 95\% \) of the wafer area, leaving it only around JJs (■). The thickness of the removed layer is \( \approx 40 \) nm.

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**III. DIFFUSION STOP-LAYERS FOR INTEGRATED CIRCUITS**

Examining the process cross-section in Fig. 1, we see that there are two major diffusion phases which may affect JJs and create pattern-dependent changes in \( J_c \) – from BE to contacting layers and from CE to contacting layers. Impurity diffusion effects on JJs can be substantially reduced or eliminated if we can prevent or impede diffusion of impurities to and from junction electrodes. This can be done by using a diffusion barrier (stop-layer) – a material with much smaller diffusion coefficient and impurity solubility than the host material it protects. For protecting Nb layers from hydrogen diffusion, there is a big choice of metals and dielectrics satisfying these requirements. However, we need to maintain a good superconducting contact between Nb layers in the contact holes and vias. This eliminates all dielectric materials from consideration. Among metals, we can use only those which would superconduct by proximity with Nb and provide high critical current for contacts holes with minimum size used in the process, e.g., \( I_c > 2 \) mA (the higher the better). Also, they should be compatible with the existing deposition systems. From these considerations we have chosen Al and Mo, also because they are used in the process anyway.

Al has extremely low solubility of hydrogen, \( \sim 6 \times 10^{-6} \text{ at.\%} \) at room temperatures. Hydrogen diffusivity in Al at room temperatures can vary by a few orders of magnitude according to different data, being in the range from \( 10^{-10} \text{ cm}^2/\text{s} \) to \( 10^{-5} \text{ cm}^2/\text{s} \) [22]-[24]. Even in the worst case, it is at least two orders of magnitude lower than in Nb. Combined with the extremely low solubility, this makes Al a very efficient diffusion barrier for hydrogen.

We placed the first DSL between junctions’ base electrode and Nb ground plane to prevent in- and out-diffusion to/from the BE. The second DSL was placed between junctions’ counter electrode and Nb wiring layer M2 to prevent in- and out-diffusion of hydrogen to/from CE. The third DSL was placed between wiring layers M2 and M3. The third DSL serves for extra protection of JJs and for protecting Nb inductors which are made mainly in M2 layer: changes in impurity concentration in Nb inductors may change magnetic field penetration depth and thus sheet inductance, which would have a negative effect on circuit performance.

All DSLs were deposited in-situ with the corresponding Nb layer on the surface of the previously processed layers. Ar sputter etching was used to remove native oxide from the Nb/Al/AlO\(_x\) layer before Ar ion milling.
surface of the bottom Nb layers in the contact holes and vias. The first (aluminum) DSL was deposited in-situ with the JJ layer, which now was deposited as Al/Nb/Al/AlOx/Nb pentalayer. The second DSL was deposited in-situ with the first wiring layer, thus forming Al/Nb or Mo/Nb bi-layer. In the same manner, the third DSL was deposited in-situ with the second wiring layer M3. The cross-section of the new process with three DSLs is shown in Fig. 3.

The minimum thickness of DSLs was determined by observing the reduction in pattern-dependent effects in $I_c$ of JJs with various connections to circuit layers. For Al it was found to be $\approx 3$ nm and $\approx 5$ nm for Mo. The maximum thickness is determined by the desired level of the critical current of Nb/DSL/Nb contacts. We set this level at $\approx 30$ mA for circular contacts of 2-μm diameter. This gave $\approx 10$ nm upper limited for Al DSL thickness and less for Mo. From these considerations, the thickness was chosen to be $\approx 5$ nm for both materials.

The best results were obtained with aluminum DSLs which completely eliminated effects of BE connection to M0 layer studied in [1]-[3] and effects of CE to Ti/Au contact pad connections studied in [4]-[6],[15]. With molybdenum DSLs we found a substantial reduction in the value of the second effect but it was not completely eliminated, apparently due to a higher diffusivity and solubility of H in molybdenum than in aluminum.

![Fig. 3. Cross-section of the new process employing three diffusion stop layers: under BE, under the first wiring layer, and under the second wiring layer. Resistively-shunted junction is shown as in Fig. 1. All superconducting contacts between Nb layers have now structure Nb/DSL/Nb, e.g. Nb/Al/Nb. All junctions are connected to other layers as Nb/DSL/JJ/DSL/Nb. The DSLs are shown 10 times thicker than their actual thickness to be visible in this scale.](image)

The described DSL method can be applied to any process layer structure and also to planarized processes with CMP, and to processes with any number of Nb layers. Just each pair of Nb layers should be separated by a DSL. The minimum number of required DSLs is twice the number of JJ layers (making it two in the present technology).

It is possible to deposit both DSLs protecting JJ in-situ with the JJ layer as DSL/Nb/Al/AlOx/Nb/DSL multilayer. However, we found the processing in this case to be somewhat more difficult than when the top DSL is deposited separately, under the next wiring layer. Similarly, a less convenient way was found to be the process when the first DSL is deposited in-situ on top of Nb layer below the junction layer (M0 ground plane in our case).

Each DSL was patterned along with the Nb layer underneath which it is located, using the same photoresist mask (otherwise it would short the circuit). Aluminum DSLs were either etched in tetrachloroethylene or dry etched in Cl2/BCl3 mixture, or Ar ion milled. No difference was found in the results. Molybdenum DSLs were dry etched in SF6 plasma in-situ right after Nb etching.

### IV. Experimental Results

Fig. 4 shows the typical effect of junction BE connection to Nb ground plane (layer M0) through a contact hole in I0 layer. The cross-section of this type of connection was shown in Fig. 1. This result is very similar to the previously presented [1]-[4]. The critical currents of two junctions deviate significantly from all other junctions – the grounded JJ and its nearest neighbor because they are the closest to the contact hole in I0.

![Fig. 4. Current-voltage characteristics of a series array of 20 identical junctions with the last JJ (#20) connected by its BE to Nb ground plane through a contact hole. Two junctions (#20 and #19) closest to this I0 contact hole change their critical current significantly during the processing as a result of this proximity (solid line). No changes in the critical current at any distance to the contact hole was observed if a DSL (4-nm layer of Al) was placed underneath the BE (dash line), as indicated by uniform switching of all 20 JJs.](image)
fabricated close to 30 wafers with this second DSL, and in only a few observed a small effect associated with hydrogen migration into the Ti layer of contact pads. It is possible that in these few wafers the surface roughness was such that 5-nm thick Al layer did not cover the surface of junctions’ CE completely or had some pinholes. In this case, the diffusion of hydrogen was impeded but not completely prevented. Therefore, a slightly thicker DSL might be needed. This will be further investigated.

Overall, the addition of DSLs has been found to have a very positive effect also on $J_c$ targeting and run-to-run reproducibility as shown in Fig. 6 – Fig. 8. The critical current density was measured in five fixed locations on each wafer, using the same test structure. These locations are the center of the wafer (0,0) and centers of each of the four quadrants (+,+), (–,+), (–,–), (+,–). It can be seen that on many parts of the wafers the $J_c$ targeting improved substantially, and run-to-run reproducibility improved by almost a factor of 10 (the standard deviation decreased by almost tenfold).

Fig. 6. Run-to-run reproducibility of $J_c$ in the first (+,+) quadrant of 150-mm wafers for 4.5-kA/cm² process. The targeted margin imposed by the circuit design requirements is ±10% shown as horizontal dash lines. Two vertical dash lines indicate when the first DSL (under BE) and the second DSL (between CE and Nb wiring layer M2) were introduced. The average critical current and its standard deviation are shown before and after the DSLs introduction.

The addition of the DSLs also resulted in the overall

**Fig. 7.** Run-to-run reproducibility of $J_c$ in the fourth (+,–) quadrant of 150-mm wafers for 4.5-kA/cm² process. All notations are the same as in Fig. 6. The $J_c$ targeting and reproducibility (standard deviation $\sigma$) improved significantly after the introduction of the DSL layers.

**Fig. 8.** Run-to-run reproducibility of $J_c$ in the second (–,+) quadrant of 150-mm wafers for 4.5-kA/cm² process. All notations are the same as in Fig. 6. The $J_c$ targeting and reproducibility dramatically improved (more than 6-fold for standard deviation $\sigma$) after the introduction of the DSL layers (especially of the first, under BE).

**Fig. 9.** Uniformity of the critical current density, $\sigma_J/J_c > \%$, on 150-mm wafers. Here $\sigma_J$ is the standard deviation, $J_c$ is the average $J_c$. Significant improvement of uniformity was achieved by adding the DSL layers.

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improvement in $J_c$ uniformity across the wafers as shown in Fig. 9.

V. CONCLUSION

In conclusion, we have developed a new technology for Nb integrated circuits that employs diffusion stop-layers between contacting Nb layers in order to prevent interlayer migration of impurities and their effect on tunnel barrier. These DSLs were deposited in-situ along with Nb Josephson junctions and wiring layers. Complete elimination of circuit pattern-dependent and contacting-layer-dependent effects on $J_c$ of JJ was found with this technology. These effects were associated with interlayer migration of hydrogen impurities and its effect on the tunnel barrier height. Long-term drift of $J_c$ related to diffusion of hydrogen impurities from junctions’ BE into Ti and (or) Pd layers of contact pads can of course be eliminated by simply removing Ti and Pd layers from the contact metallization stack. In cases when Ti and Pd layers are needed (e.g., for wafer bumping for flip chip bonding) their effect can be eliminated by placing a DSL under the stack (between the uppermost Nb layer and contact metallization).

The described DSL approach can be easily extended to planarized processes with CMP and to processes with any number of superconducting and junction layers. We also applied it to superconducting qubits with Nb junctions to protect their surface from oxidation and/or formation of two-level systems (TLS) on their surface and at the interfaces between different layers, and with the substrate. As a DSL material we extensively studied Al and Mo, and found Al to work better. Different materials may be required if the Josephson junction material is not Nb.

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