Linear Delay-cell Design for Low-energy Delay Multiplication and Accumulation

Aditya Shukla, Student Member, IEEE

Abstract—A practical deep neural network’s (DNN) evaluation involves thousands of multiply-and-accumulate (MAC) operations. To extend DNN’s superior inference capabilities to energy constrained devices, architectures and circuits that minimize energy-per-MAC must be developed. In this respect, analog delay-based MAC is advantageous due to reasons both extrinsic and intrinsic to the MAC implementation – (1) lower fixed-point precision requirement for a DNN’s evaluation, (2) better dynamic range than charge-based accumulation, for smaller technology nodes, and (3) simpler analog-digital interfacing. Implementing DNNs using delay-based MAC requires mixed-signal delay multipliers that accept digitally stored weights and analog voltages as arguments. To this end, a novel, linearly tunable delay-cell is proposed, wherein, the delay is realized using an inverted MOS capacitor’s ($C^*$) steady discharge from a linearly input-voltage dependent initial charge. The cell is analytically modeled, constraints for its functional validity are determined, and jitter-models are developed. Multiple cells with scaled delays, corresponding to each bit of the digital argument, must be cascaded to form the multiplier. To realize such bitwise delay-scaling of the cells, a biasing circuit is proposed that generates sub-threshold gate-voltages to scale $C^*$’s discharging rate, and thus area-expensive transistor width-scaling is avoided. For 130nm CMOS technology, the theoretical constraints and limits on jitter are used to find the optimal design-point and quantify the jitter versus bits-per-multiplier trade-off. Schematic-level simulations show a worst-case energy-consumption close to the state-of-art, and thus, feasibility of the cell.

Index Terms—Analog-computing, delay-cell, mixed-signal delay multiplier, multiply-and-accumulate

I. INTRODUCTION

RECENT advances in machine learning algorithms and, particularly, deep neural networks (DNNs), have equipped portable computing devices with human-like inferencing, classifying and planning capabilities. Enormous sizes of these networks, with number of operations per evaluation often running into millions, make remote computing servers indispensable. Reliance on servers increases inference latency, communication energy, risk of privacy loss, traffic, and needs a perpetual connection to the server. Some of these metrics are critical in applications like self-driven cars, that cannot afford delays while making decisions. Delocalizing computational effort for evaluating ML models, away from server and towards the leaf nodes, requires ML-specific energy-efficient computing architectures [1]. Many such architectures have been proposed to greatly accelerate the training and inference speed of DNNs [2]–[4], but much work is needed to efficiently run these networks under severe energy restrictions many portable devices operate under.

The computing-energy’s problem [5] is tackled by: (1) using simpler data-types: these algorithms do not require a large precision and continue to provide similar accuracy with simpler data-types and restricted widths [6]–[11] (2) minimizing data-transfer: the number of data-fetches shoots up for human-level, large-scale applications of these algorithms causing significant non-compute (latent) energy losses [2], [4], [12].

Relative robustness of DNNs to precision-loss, together with a limitation on energy, motivates the use of analog computing systems, wherein, the loss of information due to noise and process-variability can effectively be modeled as the loss in precision. To maintain the energy-efficiency without an excessive (counter-productive) precision-loss, these systems constitute both analog and digital computing units. The computational roles are distributed such that the multiply-and-accumulate (MAC) operations, which form the bulk of a DNN’s evaluation, are executed in an analog domain, while other operations (e.g. control-flow, data-communication and storage) are done using binary voltages. Superposable electrical variables like charge [13], [14] and current [15]–[17] physically represent partial sums of a MAC, with a capacitor as an accumulator to store the sum of physical variables.

Recently, time was proposed as an accumulation variable, as it is better than charge and current in following regards: (1) time-to-voltage/digital converters (TDC, and vice versa DTC) are more area and power-efficient than voltage-based converters [18], [19]. For instance, both DTC and TDC can be realized out of clocked counters, while voltage ADC/DACs require area and energy-expensive operational amplifiers; (2) while the noise-floor is relatively constant, the supply voltage, $V_{DD}$, drops with technology nodes. Thus, the dynamic-range of accumulation of voltage, current or charge gets increasingly limited; (3) the transition frequency of the FETs, which dictates the temporal resolution of a TDC, increases with tech. nodes.

Within the purview of time-based accumulation, pulse-width [20], [21] and pulse-delay [18], [22], [23] are the two modulation schemes that have been demonstrated on-chip. Of these, pulse- (or, event) delay is more promising for MAC applications due to (1) free addition/subtraction in case of delay, and (2) requirement of peripheral pulse re-routing circuitry requirements in the prior.

A practical delay-MAC must meet following specifications: firstly, it must accept mixed-signal arguments – one analog while other digital, for locally stored weights; secondly, it
should posses linear voltage-delay (transfer) characteristics to accept externally sensed analog voltages and allow cascading of multiple layers of MACs. To implement a low-energy mixed-signal delay-multiplier, major challenge is the design of a tune-able delay-cell, having linear transfer characteristics. Miyashita et al. [18] first proposed the use of analog-digital mixed signal delay-MAC. Common mathematical operations like addition, subtraction, multiplication, and max-/minimization were demonstrated in a clocked time-domain. However, the multiplication using clocked time-to-digital converters negated power-savings expected from an analog processor. Clock-less tune-able delay-cells for MACs were later proposed in [22], where the accumulation after each dot-product in a binary convolutional neural network was carried implicitly by the delays of a series of nMOS resistor-based delay-cells. However, the use of resistors for enabling scaling of delay, lead to an area-expensive solution.

Delay-modulation via programming voltages, for both low-power front-end analog processing and approximate-computing acceleration, was demonstrated in [23]. Applying a small-signal analog input to the back-gate of the transistor modulated the threshold voltage and hence, the delay. Since the threshold voltage varies with the input in a square-root fashion, the delay is inherently non-linear. Also, variation in the threshold voltage across a chip can introduce non-homogeneity in the multiplier.

In this work, a novel CMOS referential delay-cell, based on a steady discharge of a MOSCAP ($C^*$) via a constant current ($I^*$), is proposed. Block-diagram in Fig. 1 depicts three sequential processes that $C^*$ undergoes, from $t = 0$:  

1) instantaneous pre-charge to $V^*_0$ (colored red)  
2) steady discharge, through a constant current $I^*$ (blue)  
3) thresholding of $V^*$ at $V^*_th$, using a threshold detector (green).

With these three processes, time taken for $V^*$ to reach $V^*_th$ is:

$$T_d = \frac{C^*}{I^*}(V^*_0 - V^*_th).$$  

If $V_0$ is a linear function of $V_A$, then time taken to discharge to $V^*_th$ (or simply, the delay) becomes a linear function of $V_A$. This forms the basis of the proposed delay-cell. For use within a multiplier, its delay is exponentially scaled through gate-voltages of the source of $I^*$, rather than transistor widths. Next, analytical models for all the sub-processes in the delay-cell are developed, key sources of jitter identified and a model for the net jitter is formed. From these models, constraints on $C^*$ and $I^*$ for the usability of delay-cells in a multiplier are found, and it’s shown that the multiplier cannot accommodate more than 5 bits of (signed) digital-input. Biasing circuits that generate the gate-voltages to scale $I^*$ and the delay exponentially, are then proposed and validated.

The paper is divided as follows: in Sec. II necessary but brief background on mixed-signal delay multipliers, delay-MACs and how multiple delay-cells together constitute a multiplier, is presented. In Sec. III the concept behind the proposed delay cell is presented in more details. For each of the three sub-processes, CMOS implementation details are presented and constraints for a linear delay transfer characteristics developed. Jitter-models are then developed for the two sub-processes that contribute most to the jitter. In Sec. IV the constraints and jitter model developed are employed to find the minimum latency and maximum number of bits that can be accommodated within the multiplier. Also, a biasing circuit that enables an accurate exponential scaling of delays of cells within a multiplier is presented. In Sec. V we discuss about the chosen noise-floor and its connection with the maximum number of bits, and input dependence of energy consumption. Next, the proposed delay-cell is compared with the state-of-art, before concluding in Sec. VI.

II. BACKGROUND

A delay-MAC comprises of several delay multipliers, whose delays serially accumulate, before undergoing further non-linear processing. The multiplier accepts a time-referenced event signal, which it propagates forward as-is, but after a delay in proportion to the product of its arguments. When several such multipliers are placed in series, and a reference event is applied to the first, then, the ref. event is propagated forward, and the net (accumulation of) delay models the dot-product of inputs. By using delays, the need of adders is eliminated, because the delays are summed up naturally. Since negative numbers cannot be represented using individual events, a pair of events is used, where, the time of instance of one’s occurrence referred to the other’s, is called referential delay (Fig. 2).

A delay multiplier, besides two input arguments, has a pair of a variable and a reference event-sIGNALS (henceforth called referential events) at its input and output. For a mixed-signal multiplier, a signed, fixed-point weight vector ($S$ and an n-bit wide vector $W$) and an analog scalar ($V_A$) form the argument, and a pair of rising (or, falling) edges of voltages form referential event-signals (Fig. 2). To accommodate negative weights,
symmetric 2:2 multiplexers (or, relays) are placed within each multiplier that are realized using transmission-gates. The relay ensures that for each negative weight, the referential events are swapped before multiplication (Fig. 3b).

Each multiplier consists of smaller referential delay-cells that correspond to each bit of \( W \) and create a referential delay equaling \( 2^iD \), where, \( D \) is the common delay-factor and \( i \in \{0, 1, 2n - 1\} \). The common delay-factor, \( D \), is a linear function of \( V_{A} \). For reasons explained Sec. III-C, two, \( V_{DD} \rightarrow 0 \) falling edges, as referential event signals, are propagated through the multiplier. Weight bits, \( w_i \), individually determine whether reference-event signals are delayed by \( 2^iD \) or not, by making the falling-edge pass or skip a delay-cell.

Each referential delay-cell has a pair of identical and parallel, linearly tunable delay-cells. One delay-cell inputs \( V_A \) and outputs the falling-edge after delay linearly dependent on \( V_A \). The second cell inputs a constant reference voltage, \( V_{A0} \), and outputs the event after a fixed time. If \( V_A > V_{A0} \), then variable event gets more delayed compared to the reference, which represents a positive partial sum. A negative partial sum is produced if \( V_A < V_{A0} \) and zero, if \( V_A = V_{A0} \). Thus, using a pair of delay-cells homogenises the multiplier with respect to the multiplicand and allows negative weights and referential delays.

For illustration, a 1-bit multiplier is shown in Fig. 3a. The multiplier comprises of a 2:2 relay and a referential delay cell. \( S = 1 \) implies a negative weight which causes the falling-edges to get swapped. The referential delay-cell further contains two delay-cells, with one variable input (\( V_A \)) and the other with a reference input (\( V_{A0} \)). When \( W = w_0 = 0 \), cell-bypassing MUX is enabled leading to both negligible delay and ref. delay. Next, 3-bit multiplier is shown in Fig. 3b. The referential delays are scaled in the ratio 1, 2 and 4, by scaling the absolute delays in the ratio 1, 2 and 4.

One may also use differential mode of operations, where, the referential-delay cell is replaced with differential delay-cell. In this mode, the analog input are changed from \( V_A \) and \( V_{A0} \) to \( V_A + V_{A0} \) and \( V_A - V_{A0} \). This may remove second order distortion terms of the multiplier without changing the multiplier’s circuitry.
Once the voltage across $C_S$ is set, $S_1$ is opened and $S_2$ is closed causing $C^*$ to spontaneously discharge via $I^*$, at a constant rate (Fig. 4). The steady discharge process can be described as:

$$\Delta V^*(t) = \Delta V^*_0 + \frac{I^*}{C^*}(t - t_0),$$

where, $\Delta V^*$ is the drop in $V^*$ below $V_{DD}$. Next, a threshold-detector, with a threshold $V_{th}^*$, outputs a falling-edge once $V^*$ drops below $V_{th}^*$. Time taken for $\Delta V^* (= V_{DD} - V^*)$ to reach a given threshold $\Delta V_{th}^* (= V_{DD} - V_{th}^*)$, called the absolute delay ($T_d$), is given by:

$$T_d = \frac{C^*}{I^*} \left[ \Delta V_{th}^* - \Delta V^*_0 \right] \approx \frac{C^*}{I^*} \left[ \Delta V_{th}^* - \frac{C_S}{C^*}(V_A - V_{th}) \right]$$

This is a linear function of $V_A$. So, the delay can be adjusted linearly with the input (Fig. 5). As discussed in II to homogenize the delay-input relationship, referential delay is used. For a pair of steady discharge based delay-cells, the referential delay $\Delta t_D$ is:

$$\Delta t_D = T_d - T_{d,REF} = -\frac{C_S}{I^*}(V_A - V_{A0}),$$

which is independent of $C^*$. In case $C^*$ varies with $V^*$, the referential delay may be written as:

$$\Delta t_D = \frac{1}{I^*} \int_{V_A^0}^{V_A} C(v)dv.$$  

(6)

For $\Delta t_D$ to be a linear function of $V_A$, $C(V^*)$ needs to be maximally constant for the range of $V^* \in [V_A^0, V_{th}]$. If $I^*$ is scaled (exponentially) by factor of 2 (Fig. 5), then a delay multiplier with a digital input vector $\tilde{W} = \{w_i, \forall i = 1, 2, ... n\}$ will yield the following referential delay:

$$\Delta t_D = \sum_{i=1}^{n} \frac{w_i}{2^n} \left[ \Delta t_{D,i}(V_A) \right],$$

where, $\Delta t_{D,i}$ is the ref. delay from the delay cell $i$. This forms the basis of our mixed-signal delay multiplier.

The schematic of the delay-cell in CMOS is given in Fig. 6, detailed design methodology of which, is discussed next.

**B. CMOS implementation: $C^*$**

Later in Sec. IV -A, it is shown that $C^*$ of approximately $2fF$ is optimal for minimizing energy, latency and jitter. An inverted MOSCAP, steadily discharging towards depletion, reliably provides capacitance in this range. Since an n-type MOSCAP has a larger inversion capacitance-density than p-type (Fig. 7), the prior is used.

**C. CMOS implementation: Voltage initialization**

This stage comprises of min. sized transistors $M_{1-3}$ and pMOSCAP $C_S$ in Fig. 6, key design considerations of which are discussed next:

1) **Input nFET $M_A$ ($M_2$):** To nullify effect of process variations (PV), the $V_A$-accepting nFET is unique to a multiplier, i.e. it is shared by all delay-cells within a multiplier. Specifically, random dopant-fluctuation, oxide-thickness variations and other process-related non-idealities may offset $V_{th}$, that may in-turn offset output ref. delay by:

$$\Delta t_D = -\frac{C_S}{I^*} \Delta V_{th},$$

where, $\Delta V_{th}$ models effect of PV

2) **$C_S$:** This capacitor is unique to a delay-cell, and a min. sized pFET is assigned to each cell. The pFET...
stays in the inversion regime regardless of $V_A$, because $V_S$ saturates to a value that is at least $V_{thn}$ less than $V_{A,max}(=V_{DD})$

3) Switch S-1 ($M_1$): In the relevant regime of operation, $V^*$ remains close to $V_{DD}$, necessitating a p-type FET. The switch is unique to each delay-cell, as it isolates $C^*$ of each cell from a shared $M_2$ of the multiplier

4) Reset switch ($M_2$): A switch to reset the $V_S$ to zero before each computation is kept common to all cells within a multiplier

If the initial charge on $C_S$ is zero, then, $\Delta V^*_0$ can be expressed as a linear function of $V_A$ and an offset term:

$$\Delta V^*(V_A) = \frac{C_S + C_{ps}}{C^*}(V_A - V_{thn}) + \frac{\Delta Q_{of}}{C^*}$$  \hspace{1cm} (9)

Here, $C_{ps}$ is the parasitic capacitors, arising from $M_2$ and $M_3$; $\Delta Q_{of}$ models the zero-offset at $V_A = V_{thn}$ dependent on several parameters: $C^*$, $M_2$’s width and other parasitic effects like feed-forward of input falling-edge into $C^*$. Note that $\Delta Q_{of}$ has two distinct values: first is defined within the discharge-pulse application (MD) and it contains a feed-forward component of the falling-edge. The second is defined after the discharge-pulse application (PD), and is slightly less than MD.

To quantify linearity, $\Delta V^*$ is plotted in Fig. 8 against $V_A$ and its derivative w.r.t. $V_A$ in Fig. 8 for $V_A$ ranging between 0.3V and 1.2V, with $W^*$ (or $C^*$) as parameters of design. For this range, less than 10% variation is seen. The figure shows that larger capacitors can provide better linearity.

Fig. 8 plots the $\Delta V^*_0$ for and its average derivative, versus $W^*$ ($\propto C^*$), in a log-log fashion. Both plots have a constant slope of $-1$ for sufficiently large $W^*$, validating Eq. 9 as a model for the discharge process. $C_S + C_{ps}$ and $\Delta Q_{of}$ are then empirically determined by fitting the model of Eq. 9 yielding $C_S + C_{ps} = 0.23fF$ and $\Delta Q_{of} = 0.5fC$ (MD).

Eq. 9 is only valid when the $C^*$’s voltage is big enough to charge up $C_S$. Mathematically,

$$V_{DD} - \Delta V^*(V_A) > V_A - V_{thn}$$ \hspace{1cm} (10)

For $V_A = V_{DD}$, we get:

$$\Rightarrow C^* > \frac{(C_S + C_{ps})(V_{DD} - V_{thn}) + \Delta Q_{of}}{V_{thn}}$$ \hspace{1cm} (11)

This sets the lower limit on $C^*$, which is employed later in Sec. [IV-A]

To slightly enhance the linearity without adding to the area, one in every 5 pMOSCAP of the $C_S$ is replaced by an nMOSCAP. For $V_S < V_{DD} - V_{thp}$, PFET is inverted and provides a close to a constant cap. For $V_S > V_{DD} - V_{thp}$, PFET’s capacitance diminishes but nFET offsets the loss. Since NMOS is smaller, it does so, only to a small extent.

D. CMOS implementation: Steady discharge

This part of the delay-cell consists of transistors $M_{4-6}$ in Fig. 6 key design considerations of which are discussed next:

1) $I^*(M_4 - M_3$): This is realized using bi-cascoded nFET current source, with the FETs at their min. widths. The exponential current scaling is done via an external biasing circuit, that generates gate-voltages for both $M_4$ and $M_5$. The biasing circuits are discussed in Sec. [IV-B]

2) Switch S-2 ($M_6$): An NMOS switch is placed in series with the current-source. Unlike S-1, the switch was placed away from $C^*$, preventing the feed-forward through the parasitic capacitors.

For $W_S$ ($\propto C_S$) at its minimum value ($160nm$) and $W^*$ ($\propto C^*$) = $640nm$, $C^*$’s discharge transient is shown in Fig. 10. Referring back to Fig. 6, the switch ($M_2$) is turned ON at $t = 25ns$, by ramping-up $IFE'$, the input to $M_6$. As expected, $I^*$ discharges $C^*$ at a near-constant rate (Fig. 10b). Its constancy depends solely on output resistance of the current source. Kinks observable in the transients are caused by the feedback from the half-latch and do not practically affect the performance. The absolute delay for various $R$ (= $I^*/C^*$), spaced exponentially with a factor of 2, is plotted in Fig. 10b.
E. CMOS Implementation: Threshold detector

It comprises of $M_{7-14}$ as the falling-edge, uni-polar threshold detectors, half-latch and other switches for resetting. Details and design consideration are discussed next:

1) *Falling-edge inverter* ($M_{8}$): To minimize the area requirements, the width of $M_{8}$ is kept minimum. As discussed below, under certain constraints on $C^{*}$, this inverter contributes to a $V_{A}$-independent delay, thus keeping distortion negligible.

2) *Leak-prevention switch* ($M_{7}$): It prevents the sub-threshold $M_{8}$ from leaking and set-up the latch prematurely. It inputs the falling-edge of the previous delay cell.

3) *Half-latching inverter* ($M_{11,13}$): These transistors latch $V_{RE}$ to $V_{DD}$ and the OFE-node to 0, once $V_{RE}$ reaches $V_{thn}$.

4) *Latch-en/Disable switches* ($M_{10, M_{14}}$): These switches enable the half-latch operation when closed and otherwise, disable it, reducing the energy required to reset the half-latch.

5) *Reset-FETs* ($M_{9,12}$): $M_{9}$ resets node $V_{RE}$ to 0. $M_{12}$ sets the OFE node to $V_{DD}$ before the start of computation. These transistors are shared within the multiplier.

A CMOS inverter can serve as a low-energy threshold detector, whose switching-voltage can be set by designing the ratio of sizes of pMOS and nMOS. However, it consumes short-circuit energy ($E_{SC}$) given by:

$$E_{SC} = \frac{V_{DD}}{6R} \mu \frac{W}{L} C_{ox} (V_{DD} - V_{thp} - V_{thn})^{3}$$  (12)

where $R = I^{*}/C^{*}$ and,

$$\mu \frac{W}{L} = (\mu_{p}(W/L)_{p} + \mu_{n}(W/L)_{n})^{1/2}$$.

Since $R$ decreases exponentially, $E_{SC}$ increases exponentially. Hence, a delay-cell implementing the n-th exponent will expend $2^{n} \times E_{SC}$ of the cell implementing the first. For a n-bit multiplier, the total short-circuit energy lost is $(2^{n+1} - 1) E_{SC}$. Thus, an exponential requirement in energy consumption motivates an alternative inverting mechanism.

The low-energy alternative to the CMOS inverter is a standalone pFET ($M_{8}$ in Fig. 6), due to its switch-like I-V relationship. If it were an ideal switch, with a switching voltage $V_{S}$ ($> \Delta V_{0, max}$), $V_{RE}$ would jump to $V_{DD}$ after a fixed delay following $\Delta V^{*}(t) = V_{thp}$. This would conserve the linearity of Eq. 5 with respect to $V_{A}$, as it only adds a constant delay. However, a real PFET has a close to exponential I-V relationship and conservation of linearity needs to be established, or at least constraints for maximal linearity determined.

With the assumption of exponential I-V characteristics and large output-resistance ($g_{DS}$), the sub-threshold current can be expressed as a function of the gate-source voltage ($= \Delta V_{0}^{*}$) using the following equation:

$$I = I_{0} \exp \left( \frac{\Delta V_{0}^{*}}{V_{T}} \right),$$  (13)

where, $V_{T}$ is the thermal voltage. Eq. 13 is valid only for $\Delta V_{0}^{*} < V_{thp}$; for $V_{GS} > V_{thp}$, I-V relationship is usually degree-2 or less polynomial, moving the switch away from an ideal behavior.

For a $V_{A}$ that linearly decreases from $\Delta V_{0}^{*}$ with a steady rate $R$, $V_{RE}$ (Fig. 6) can be expressed as a function of time using:

$$V_{RE}(t) = \frac{I_{0} V_{T}}{C^{*}} \exp \left( \frac{\Delta V_{0}^{*}}{V_{T}} \right) \left( \exp \left( \frac{R t}{V_{T}} \right) - 1 \right),$$  (14)

where, $R = \frac{I^{*}}{C^{*}}$ is the rate of change of $V^{*}$ with time, and $C^{*}$ is net capacitance at the drain of M8. When $V_{RE}(t) = V_{thn}$, the half-latch is set up and the voltage at OFE node (Fig. 6) falls to 0. Thus, the time taken from the start of discharge ($t = 0$) to the drop in OFE-node voltage to zero ($t = T_{d}$) is:

$$T_{d} = \frac{V_{T}}{R} \ln \left( \frac{RCV_{thn}}{I_{0}V_{T}} \exp \left( -\frac{\Delta V_{0}^{*}}{V_{T}} \right) + 1 \right).$$  (15)

$T_{d}$ becomes a linear function of $\Delta V_{0}^{*}$ under the constraint:

$$\frac{RCV_{thn}}{I_{0}V_{T}} \exp \left( -\frac{\Delta V_{0}^{*}}{V_{T}} \right) \gg 1$$  (16)

Putting $R = \frac{I^{*}}{C^{*}}$, this inequality may alternatively be written as:

$$\frac{I^{*}}{C^{*}} = \frac{C}{I_{0} \exp \left( \frac{\Delta V_{0}^{*}}{V_{T}} \right)} \gg 1$$  (17)

Since $\Delta V_{0}^{*}$ varies inversely with $C^{*}$ (from Eq. 9), the denominator in Eq. 17 is a monotonically decreasing function of $C^{*}$. Then, as per this inequality, $C^{*}$ should be greater than a critical capacitance $C_{min}^{*}$. This inequality is used in Sec. IV-A for establishing constraints on $C^{*}$ and $n$.

Under the validity of this inequality, $T_{d}$ can be expressed as:

$$T_{d} = \frac{V_{T}}{R} \ln \left( \frac{RCV_{thn}}{I_{0}V_{T}} \right) - \frac{\Delta V_{0}^{*}}{R},$$  (18)

matching the expectation of $T_{d}$’s linearity with $\Delta V_{0}^{*}$, or $V_{A}$. Note that the latch-point, or, the value of $V^{*}$ when $V_{RE} = V_{thn}$ is a constant, independent of $V_{0}^{*}$ (or $V_{A}$), and expressible as:

$$\Delta V_{th}^{*} = \Delta V_{0}^{*} + RT_{d} = V_{T} \ln \left( \frac{RCV_{thn}}{I_{0}V_{T}} \right).$$  (19)

Though an exponential I-V characteristics is assumed for $M_{8}$, in reality, it is exponential only for sub-threshold gate voltages. For devices with power-I-V relations, Eq. 14 is re-derived with the modified I-V, and constraints of Eq. 11 re-determined. For $p - 1$ power current-voltage relationship,

$$\frac{I^{*}}{C^{*} I(V_{A}, C^{*}) V_{RE}} \gg 1.$$  (20)

For an ideal switch ($p \rightarrow \infty$), the constraint is trivially satisfied and TD stage doesn’t contribute to distortion. As the I-V relationship of the pFET moves away from step-like behaviour towards linearity ($p \rightarrow 0$), ensuring linearity from delay-$V_{A}$ characteristics becomes harder.
F. Noise-modelling

The delay-cell essentially consists of two current-integrators that accumulate the accompanying noise-current, starting from the arrival of falling-edge \((t = 0)\) to the latch-up \((t = T_d)\). This leads to a net temporal shift in the falling-edge, or a jitter in the output falling-edge. To enable design of the delay-cell and multiplier, the two jitter components are modeled as a function \(C^*\) and \(I^*\) (the design variables) and an upper limit on jitter is set, yielding constraints on the design variables and \(n\). For simplifying jitter-modeling, it is assumed that:

1) Out of the three, only two processes contribute to the jitter: steady discharge and threshold-detection. (Initial discharge occurs much faster than \(T_d\), so it contributes negligibly to the net jitter.)

2) The net jitter is much smaller than \(T_d\)

1) Jitter from steady discharge: For this stage, the primary contributor of jitter is the channel noise-current from \(M_{4-5}\) accumulating in \(C^*\). To simplify the model, it is assumed that the noise-current out of \(M_4\) circulates within itself, and hence contributes negligibly to the jitter. With this assumption, the stage reduces to a noisy FET discharging a fixed capacitor, jitter modelling for which was done for ring oscillators in [24]. For an inverter-type ring-oscillator, the jitter-per-stage is modeled as:

\[
\Delta t_{Dn}^2 = \frac{4kT\gamma g_{d0}}{2T^2} T_d, \tag{21}
\]

where, \(\gamma\) is the excess noise factor, \(g_{d0}\) is the drain-source conductance at \(V_{DS} = 0\). This naturally extends to the proposed delay-cell, with the exception that \(T_d\) is variable, dependent on the rate of discharge and \(V_A\). Using Eq. 4 the expression for jitter becomes:

\[
\Delta t_{Dn}^2 = \frac{4kT\gamma g_{d0}}{2T^3} C^* (\Delta V_{th}^* - \Delta V_n^*) \tag{22}
\]

To further simplify, the dependence of jitter on \(\Delta V_{th}^*\) and \(\Delta V_n^*\) is neglected and a constant jitter, for a \(V_D D/2\) drop in \(V^*\), is defined and used. Owing to the fact that \(g_{d0}\) has a linear dependence on current, jitter from this stage is compactly express-able as:

\[
\Delta t_{Dn}^2 = K \frac{C^*}{T^2}, \tag{23}
\]

where, \(K\) is a temperature and technology dependent constant. For model validation, the jitter is simulated in software, for IBM’s 130nm technology. Resulting \(\Delta t_{Dn}^2\), with only \(M_{4-5}\) noise turned on, versus \(C^*\) and \(I^*\) is plotted in Fig 11.

Instead of Eq. 23, the following model is used as it fits the experimental data better (R-sq. of 0.982, from 10 iterations):

\[
\Delta v_{n}^2 = K \frac{C^*}{I^p}, \tag{24}
\]

where, \(K = 2.95 \times 10^{-16}\) and \(p = 2.46\).

2) Jitter from threshold detector: Since the input gate-source voltage (\(\Delta V^*\)) of \(M_8\) increases linearly with time and drain-current exponentially, it is assumed that RMS channel noise-current \((i_n)\) out of \(M_8\) increases exponentially. Thus, at any given instant of time post falling-edge’s arrival, noise current from only the past 3-4 \(V_T\)-drops in \(\Delta V^*\), contributes to this stage’s jitter.

If \(\Delta v_n\) is the deviation in \(V_{RE}\) at \(t \rightarrow T_d\), then for a constant \(i_n\), we have:

\[
\Delta v_{n}^2 \propto \frac{i_n^*}{\Delta T_d} \frac{T_d}{C^*}. \tag{25}
\]

Since \(i_n^*\) varies exponentially over the duration \(t_{Dn}\), this equation cannot be applied without adjustments. Thus, the following equation is used:

\[
\Delta v_{n}^2 \propto \int_0^{T_d} 4kT\gamma g_{d0}(t) dt \frac{T_d}{C^*} \tag{26}
\]

Letting \(g_{d0} = G_0 \exp \left(\frac{\Delta V_{th}^* + R_t}{V_T}\right)\), we get:

\[
\Delta v_{n}^2 \propto \int_0^{T_d} 4kT\gamma G_0 \exp \left(\frac{\Delta V_{th}^* + R_t}{V_T}\right) dt = \beta \frac{V_T}{R} \exp \left(\frac{\Delta V_{th}^*}{V_T}\right) \tag{27}
\]

where, \(\beta = 4kT\gamma G_0\). This equation establishes an independence of \(v_n\) on \(R\), which is confirmed from Fig. 12. In the figure, \(R\) is varied by a factor of more than 10x, but less than 2x rise is seen in \(\Delta v_{n}^2\).

Next, the relationship between \(\Delta t_{Dn}\) and \(R\) is determined. Similar to the approach adopted in [24], \(\Delta t_{Dn}\) can be found.

![Fig. 11. steady discharge-stage’s jitter](image_url)

![Fig. 12. Variance in \(V_{RE}\) and jitter due to \(M_8\)’s noise-current](image_url)
by extrapolating noisy $V_{RE}$ along the noise-less $V_{RE}$, to the point of latch-up:

$$
\Delta t_{Dn}^2 = \left( \frac{dV_{RE}}{dt} \right)^2 \Delta v_n^2,
$$

(28)

$$
\propto \frac{v_n^2}{R^2},
$$

where, Eq. 14 was used for $dV_{RE}/dt \propto R$. Simulated jitter, with only $M_{8}$'s noise turned on, is plotted in Fig. 12.

For minimally sized $M_{7-14}$, the fitted model from 10 iterations of (noisy) simulations is:

$$
\Delta t_{Dn}^2 = K_2 \frac{1}{R^{1.5}},
$$

(29)

where, $K_2 = 1.29 \times 10^{-10}$. Thus, the actual exponent is less than predicted.

IV. MIXED-SIGNAL DELAY MULTIPLIER

With the delay-cell design considerations discussed, next, the necessary steps to employ the cells within a multiplier are presented: (1) use of constraints to find the valid region of design and operation (2) bias-circuit design for $I^*$'s exponentiation. Lastly, through simulations, the functionality of cascaded delay-cells as multiplier is validated and the key energy components for each multiplication operation are identified.

A. Optimizing $C^*$ and No. of Bits

Using the inequalities involving $C^*$, developed in Sec. III-C and the noise models of Sec. III-F, the constraints on $C^*$ and $I^*$ are determined. Note that these are valid only for the IBM's 130nm technology, but may similarly be determined for other CMOS technology nodes.

1) Linearity of voltage-initialization: In the inequality of Eq. 13, replacing model-parameters extracted from the data of Fig. 8(b) gives constraint 1,

$$
C^* > 2.2 f,
$$

(30)

which, corresponds to an inverted nMOSCAP single-finger width of 1.28$\mu$m. This constraint is marked by '1' in Fig. 13-a-c.

2) Linearity of threshold detection: Since $I^*$ of the slowest cell is $2^n$ times smaller than that of the fastest cell ($I_f^*$), constraint 2 from Eq. 17 becomes:

$$
\frac{2^{-n} I_f^*}{I_0 \exp(\frac{\Delta V_0^*(V_A, C^*)}{V_T})} \frac{V_{thn}}{V_T} > 1
$$

(31)

Only $C^*$ and $I_f^*$ are designable; the rest − $C, V_{thn}, V_T$ and $I_0$, are constant. To simplify the analysis, the denominator is maximized over $V_A$ and the uni-variate $\Delta V_0^*(V_A = 1.2, C^*)$ used. Though the argument of the exponential in Eq. 31, $\Delta V_0 (V_A, C^*)$, was modeled in Sec. III-C actual data of Fig. 8 is used. This constraint is marked by '2' in Fig. 13-b-c.

3) Upper limit on jitter: The referential delay of the fastest cell, from Eq. 5 is:

$$
\Delta t_D = -\frac{C^*}{I_f^*} (V_A - V_{A0})
$$

If jitter from steady discharge is denoted by $\Delta t_{Dn,1}$ and from TD by $\Delta t_{Dn,2}$, the constraint on the net jitter is such that it is to be smaller than the maximum ref. delay of the fastest cell. For a $V_{A0} = 0.75V$,

$$
3 \sqrt{\Delta t_{Dn,1}^2 + \Delta t_{Dn,2}^2} \leq 0.4 \frac{C^*}{I_f^*}
$$

(32a)

$$
3 \left[ \frac{C^*}{(2^{-n} I_f^*)^{2.46}} + K_2 \left( \frac{C^*}{2^{-n} I_f^*} \right)^{1.5} \right] \leq 0.4 \frac{C^*}{I_f^*}.
$$

(32b)

With its LHS being monotonic function of $C^*$, Eq. 32 gives an upper limit on $C^*$ for a given $n$. This constraint is marked by '3' in Fig. 13-b-c.

Fig. 13 plots the constraints for a 4, 5 and 6-bit multiplier. For 4 and 5 bits, the valid region of operation, marked by double-sided arrows, lies between the curves corresponding to constraints 1, 2, and 3. For 6 bits, no solution exists for the chosen constraints. Thus, the 5-bit multiplier with

$$
C^* = 2.2 f F,
$$

and

$$
I_f^* = 1 \mu A
$$

emerges as the point of design, as it works for all multipliers with less than 6 bits, minimizes the multiplication latency and energy consumption.
B. Biasing circuit

Accurate biasing for the current sources is required to ensure low output distortion. As discussed below, its behavior must meet two specifications:

1) As discussed in Sec. IV-A, $I_T^*$ is achievable only for the sub-threshold transistors with the employed VLSI node. Hence, the biasing circuit is designed only for sub-threshold currents and works well in this regime only.

2) The current source within each cell consists of a pair of series NFETs ($M_4$ and $M_5$ in Fig. 6). $M_5$’s gate-voltage (primary bias) is such that it sinks $2^{-n}I^*$ and its drain-voltage is fixed close to $100mV$ ($\approx 4V_T$). The drain voltage is maintained by $M_4$ gated with a secondary bias approximately $100mV$ above $M_5$.

The circuit (Fig. 14) has two branches: source and scaling. Source branch ($M_{1-6}$) generates biasing voltages dependent on a programmable voltage, $V_{REF}$. Scaling branch ($M_{7-12}$) first uses those biasing voltages to generate current in the exponents of 2 (using transistor widths) and then generates the bias for the cells’ current-source using self-biasing. Here, the primary bias out of $M_{12}$ is denoted as $V_{B1}$ and the secondary out of $M_{10}$ as $V_{B2}$.

In the source branch, $M_1$ converts the reference voltage $V_{REF}$ into current $I_{BIAS} = I_T^*$. $M_2$ and $M_3$, being self-biased in the saturation regime, push up the gate voltages of the tri-cascode, enough to keep mirror transistors ($M_{10-11}$) of the scaling branch saturated. $M_{4-6}$ produce the multiplier-cascode’s bias.

In the scaling branch, $M_{7-9}$’s widths are down-scaled by $2^{-n}$ w.r.t. the source cascode’s width, which down-scale the current in the same proportion. $M_{12}$ is self-biased to accept the current and generates the primary bias $V_{B1}$. The gate voltage of the FET with the largest current exponent (or, the smallest delay exponent) is:

$$V_{B1,i} \approx V_{REF}$$

Its drain-voltage is maintained at $100mV$ using a fixed biased $M_{11}$. After down-scaling $M_{11}$’s size (by $2^{-i}$, $i$ being the exponent), its source voltage is maintained at a constant value. $M_{10}$, also a down-scaled transistor, is used to generate the secondary bias ($V_{B2}$). $M_{10}$’s width is adjusted using parametric analysis to keep its self-bias above $V_{B1}$ by $100mV$. An additional exponent-dependent scaling for the $M_{10}$ is needed, given by:

$$W_{M_{10,i}} \approx (1.3)^{-i}W_{M_{10,max}},$$

6 to counter the lower turn-on voltages is required for the scaling branches. The response of the bias circuit is plotted in Fig. 15 as $V_{REF}$ varies, the bias current input to the multiplier’s cascode is plotted in Fig. 15 $V_{B1}$, $V_{B2}$ and $V_{B2} - V_{B1}$ of down-scaled multiplier branches (upto 8 bits) is plotted in Fig. 15.

To minimize distortion, it is essential that $M_5$’s corresponding to all exponents are applied the same drains-source voltage. Besides using a 3-level cascading, the length of all transistors within the cascode is increased by $10\times$ over the minimum to minimize the CLM and short-channel effects that shoot-down the $\tau_{D,S}$. The sizes of all transistors are summarized in Table I.

C. Multiplier Simulation

Using the peripheral elements described in Sec. III the multiplier is simulated using transient simulators, for IBM 130nm technology.

1) Functionality test: A 5-bit multiplier, composed of delay-cells cascaded as described in Sec. III was simulated. Letting $V_{A0} = 0.75V$, Fig. 15a plots the ref. delay of the multiplier as it varies with $V_A$, with weight ($W$) as a parameter. Conversely, ref. delay with $W$ as the independent variable and $V_A$ as parameter is plotted in Fig. 15b. Since the output ref. delay is distorted for $V_A < 75mV$, the valid range of inputs for the multiplier is $75mV$ to $1.2V$.

2) Energy analysis and simulation results: Within a delay cell, the key components of energy are:

1) $E_{C*}$: Energy used up in charging $C^*$ for each compu-
Comparing their sum with the simulated total, it is concluded that the listed components account for almost all the expended energy.

Next, value of these metrics is determined by simulating once 

where, \( C_{RE} \) is the net capacitance at the node. Part of it comes from the thresholding-pFET \( M_8 \) (\( E_{TD1} \)) and other comes from latching-pFET, \( M_{11} \) (\( E_{TD2} \))

3) \( E_{PU} \): Energy used in pull-up of the event-propagating wires of the delay cell (\( OFE \) node in Fig. 6)

4) \( E_{INV} \): Energy used up in inverting the input falling-edge, to a rising edge (\( IFE' \), input to \( M_6 \) in Fig. 6)

Next, value of these metrics is determined by simulating the 5-bit multiplier (schematic) for one cycle of computation, with arguments \( V_A = 1.2V \) and \(|W| = 31 \). \( E_{TD}, E_{PU} \) and \( E_{INV} \) is determined during the computation-phase and \( E_{C^*} \) and \( E_{PU} \) are determined during pre-charge phase. The energy components and their simulated values are listed in Table II Comparing their sum with the simulated total, it is concluded that the listed components account for almost all the expended energy.

V. DISCUSSION AND BENCH-MARKING

In Sec. IV-A3 constraint on jitter was chosen such that the peak-jitter (3\( \Delta t_{DN} \)) from the slowest delay-cell, is less than the maximum referential delay of the fastest delay-cell.

However, for certain inputs, the net output referential delay of a multiplier can be zero, which makes it impossible for the noise to ever be smaller than the output signal. Thus, the chosen constraint is a practical as it grants the benefit of lower energy consumption by delay-based analog computing and simultaneously prevents excessive signal corruption by the noise. Depending on the signal-to-noise specification for an application, much tighter constraint on noise may be placed, which, in effect, reduces the maximum number of bits accommodable. Fig. 17 plots the number of bits possible within a multiplier, as a function of excess jitter margin (\( \epsilon \)), where, \( \epsilon \) is the ratio of maximum ref. delay of the fastest cell and peak-jitter. At \( \epsilon = 1 \), the number of bits is the highest, and decreases to 1 at \( \epsilon \approx 14 \).

Note that the multiplier’s \( E_{C^*} \), given in Table II is computed for the case when all weight bits are set to 1 (\( W=31 \)). Otherwise, this components of energy depends on (1) the input weight and (2) number of computations being done by the MAC, per second. If the multiplier is used in a sense, or, one-time-use mode, then, the listed \( E_{C^*} \) is accurate, as all the charged-up energy leaks out eventually. Any new MAC cycle would require the same energy to charge-up \( C^* \) from the point of no charge. However, for acceleration mode, where same weights are used with variable \( V_A \), \( C^* \) of the cells with \( w = 0 \) never get an opportunity to discharge completely, since all falling-edges bypass the cell. Before it fully discharges, a new MAC cycle’s pre-charge step would charge-up \( C^* \) to \( V_{DD} \) from intermediate voltage.

In Table III two simulated performance metrics are compared with the state-of-art: (1) energy consumption per multiply-accumulate, reported above, and (2) multiplication latency (from absolute delay of the delay-cell). We also compare whether the multiplier allows negative weights and

### Table I

**FET sizes for the biasing circuit**

| FET Label | Width (/160nm) | Length (/120nm) |
|-----------|----------------|-----------------|
| \( M_1 \) | 1              | 1               |
| \( M_{2-3} \) | 2\( n \)      | 1               |
| \( M_{4-6} \) | 10 \times 2\( n \) | 10              |
| \( M_{7-9} \) | 10 \times 2\( i \) | 10              |
| \( M_{10} \) | 2.6\( i \)    | 10              |
| \( M_{11} \) | 2\( i \)      | 10              |
| \( M_{12} \) | 1             | 1               |

### Table II

**Delay-cell energy components**

| Component | Energy/MAC (fJ) | Energy/MAC/bit (fJ) |
|-----------|----------------|---------------------|
| \( E_{C^*} \) | 34.0          | 6.8                 |
| \( E_{TD1} \) | 5.6          | 1.1                 |
| \( E_{TD2} \) | 8.8          | 1.7                 |
| \( E_{PU} \) | 46.0          | 9.0                 |
| \( E_{INV} \) | 16.0          | 3.0                 |
| Total     | 110           | 22                  |
| Total (sim.) | 116          | 23                  |

![Figure 16. 5-bit multiplier transfer characteristics](image)

![Figure 17. Number of bits vs. excess jitter margin](image)
the maximum number bits accommodable for various mixed-signal MACs. From the table, it is seen that:

1) The delay cell consumes $23\text{fJ}$ per bit of digital argument/input, which is more than lowest-reported state-of-art energy consumption. Our energy metric is at $130\text{nm}$, and the lowest-state-of-art metric at $65\text{nm}$. Assuming that the energy scales by $L^2$, the scaled energy consumption approaches that of the state-of-art

2) In [23], linearity of the delay-cell is based on back-body biasing, which is theoretically non-linear. In the proposed cell, the output-input characteristics are linear, due to the linear voltage-initialization step

3) Despite noise limitations, the number of bits that can be accommodated in the mixed-signal multiplier is higher than state-of-art. All reported mixed-signal MACs use an exponential scaling of transistor widths, as a way to convert digital signals to analog. In this work, we proposed a biasing circuit that exponentially scales the currents via gate-voltages and avoid area expensive width-scaling

VI. CONCLUSION

In this work, a linearly tunable delay-cell is proposed that realizes the analog input-dependent delay using three sequential sub-processes: (1) an input-dependant charge-up of $C^*$ (2) its steady discharge, via current $I^*$ (3) thresholding of its voltage. Each of the sub-processes is then analytically modeled, using which, constraints on the $C^*$ and $I^*$ for linearity are found. Jitter models, based on prior ones developed for CMOS inverter ring-oscillator, were modified and validated for the proposed cell. To form a multiplier, delay-cells with same analog input and $I^*$ scaled in the exponents of 2, must be cascaded to form a multiplier. Since $I^*$ is scaled using gatesource voltages, a biasing circuit that accept a ref. voltage and generates gate biases for delay cells corresponding to all exponents, is proposed and validated. From the constraints on $C^*$ for linearity and noise, the minimum $C^*$ was found to be around $2fJ$ and maximum bits supportable to be five. Lastly we also identify key energy components of the multiplier, which sum up to be $20\text{fJ/MAC/bit}$ for IBM’s $130\text{nm}$ technology.

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