Recent Developments of Modulation and Control for High-Power Current-Source-Converters Fed Electric Machine Systems

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Abstract—The pulse-width-modulated (PWM) current-source converters (CSCs) fed electric machine systems can be considered as a type of high reliability energy conversion systems, since they work with the long-life DC-link inductor and offer high fault-tolerant capability for short-circuit faults. Besides, they provide motor friendly waveforms and four-quadrant operation ability. Therefore, they are suitable for high-power applications of fans, pumps, compressors and wind power generation. The purpose of this paper is to comprehensively review recent developments of key technologies on modulation and control of high-power (HP) PWM-CSC fed electric machines systems, including reduction of low-order current harmonics, suppression of inductor–capacitor (LC) resonance, mitigation of common-mode voltage (CMV) and control of modular PWM-CSC fed systems. In particular, recent work on the overlapping effects during commutation, LC resonance suppression under fault-tolerant operation and collaboration of modular PMW-CSCs are described. Both theoretical analysis and some results in simulations and experiments are presented. Finally, a brief discussion regarding the future trend of the HP CSC fed electric machines systems is presented.

Index Terms—Current source converter (CSC), high power (HP) applications, electric machine system, inductor–capacitor (LC) resonance, low-order current harmonics, common-mode voltage (CMV), modulation, control.

I. INTRODUCTION

POWER converters have been highly adopted in both the high-power (HP) drive and generation system for more cost-effective and advanced industrial processes [1-2]. The medium-voltage range (several kV) HP drive applications could achieve lower current ratings, higher efficiency and lighter cables [3]. The voltage-source converters (VSCs) have been widely studied and used in industrial sectors. Different from VSC that utilizes capacitor on the DC link, the current-source converter (CSC) employs the high-reliable inductor as the DC-link energy storage components [3]. This paper will present a comprehensive review on recent developments of modulation and control schemes of pulse width modulated (PWM) CSCs based electric machine systems for HP industrial applications.

Generally speaking, PWM CSC features a simple converter configuration, low dv/dt of output voltage, four-quadrant operation, reliable overcurrent and inherent short-circuit protection. Those features make PWM CSC technology well suited for HP drives [4]. Fig. 1 shows configuration of the four-quadrant PWM CSC based electric machine system, where active front-end converters such as PWM current-source rectifier (CSR) can be utilized at the grid side to improve the harmonics performance and control the power factor (PF) flexibly [4]. Apart from being applied in HP drives, the PWM CSCs have also been studied intensively in wind energy conversion system (WECS) [5], superconductor magnetic energy storage (SEMS) system [6] and high voltage direct current (HVDC) transmission system [7], etc.

The low-order current harmonics, the inductor–capacitor (LC) resonance and the common-mode voltage (CMV) problem are always considered as the challenges and research hotspots for the HP CSC based electric machine systems [10-34]. High-magnitude low-order harmonics in modulated currents resulted from the discretization error and overlapping period effect are important issues in CSC-based systems. Those generated harmonics degrade the harmonic profile of line currents and machine currents and deteriorate the LC resonance if the damping suppression is inadequate [10-16]. The LC resonances, excited by either the grid-side LC filter or motor-side filter capacitors and motor inductors, may deteriorate the power quality and cause system instability. To avoid the possible steady-state and transient LC resonance,
II. FUNDAMENTAL KNOWLEDGE

The trapezoidal pulse-width modulation (TPWM), the space vector modulation (SVM), and the selective harmonics elimination (SHE) are three major modulation schemes used for PWM CSCs [4]. The SHE is able to eliminate a specific set of undesired harmonics with low switching frequency. The switching angles $\theta_1$, $\theta_2$, ..., $\theta_N$ indicate the $N$ degrees of freedom for eliminating $N$-1 harmonics, and $2N+1$ pulses are required per half cycle consequently. These switching angles of SHE are calculated offline by mathematical equations for harmonics elimination. But the computation process is complex and there will be no solution when the pulse number per cycle increases. The SHE schemes with three pulses and five pulses per half cycle are exemplified in Fig. 2 [8].

In contrast to SHE, SVM and TPWM are two online schemes that feature better dynamic performance. But they exhibit larger low-order harmonics. The TPWM requires a special design, where no switching signal is generated in the center $\pi/3$ interval of both half cycles of modulated waves, to meet the gating constraints of PWM CSC. The modulating wave and carrier wave needed to generate TPWM pulses are illustrated in Fig. 2 (a) and (b). Proper design of LC filter size as well as the optimized modulation and control schemes should be considered [17-27]. The CMV problem generated by high-frequency switching actions of power devices, is the main concern for both the CSC and VSC based HP drives due to the high system voltage level. If not well mitigated, the CMV would result in the premature failure of motor stator winding insulation. An effective way to mitigate the CMV is to modify the pulse patterns of modulation schemes [29-34].

In addition, with increasing requirements of high power capacity and high reliability in the HP industrial applications, the modular CSCs fed electric machine systems have drawn great attention recently [35-45]. Based on the aforementioned scenarios, the succeeding scripts are organized as following: the fundamental modulation and control schemes for PWM CSC fed electric machine systems are briefly introduced in Section II. Section III and Section IV introduce the modulation and control techniques to suppress the low-order harmonics and the LC resonance, respectively. The CMV issues of CSC fed drives are discussed in Section V. Section VI presents the application of modular CSCs and the future trend of HP PWM CSCs fed machine systems. Finally, conclusions are drawn in Section VII.

Fig. 2. SHE modulation schemes. (a) Three pulses; (b) Five pulses.

Because of the better harmonics performance under low switching frequency, SHE is dominantly employed in grid-side converter, while the SHE, TPWM and SVM are hybrid used by motor-side converter to achieve both the improved current harmonic performance and dynamic performance under a wide speed range. In the practical applications, SHE is used under the high-speed range, and TPWM and SVM are implemented under the low-speed range [3].

As for the control schemes, PWM CSR can be operated with either the fixed-unity modulation index with delay-angle control or modulation index control to regulate the DC-link current. Normally, the delay-angle control is used for PWM CSR on grid side due to the implementation of SHE [4]. While in the CSC based WECS system, the grid voltage-oriented control (VOC) is utilized for the grid-side CSR. Modulation index and delay-angle controls are implemented to satisfy the requirements of DC-link current regulation and PF control according to the grid code [5, 8]. In the motor side, the field-oriented control (FOC) scheme is mainly used to control the flux and torque independently. The speeds $\omega_r$ and rotor angle $\theta_r$ of electric machine are fed back to the CSI controller to track the speed reference. Under a certain power condition,
smaller DC-link current ripples and lower conducting losses can be achieved with the minimized DC-link current, which can be obtained by applying the fixed unity modulation index strategy on the motor-side CSC [8]. This control strategy is a tradeoff between the system efficiency and dynamic response. The DC-link current reference is calculated from the CSIs and the actual DC-link current is regulated by the grid-side CSRs. The overall control strategies for the CSC fed drives are illustrated in Fig. 4.

III. LOW-ORDER HARMONICS REDUCTION

The maximum switching frequency is normally set around several hundred Hz in the industrial HP CSC drives for the permitted power losses. However, high-magnitude low-order harmonics, including 5th, 7th, 11th and 13th, are generated in modulated converter currents due to the discretization error in the digital realization [10]. In addition, large overlapping period will also increase the low-order harmonics and reduce the fundamental in the modulated converter currents [15-16]. The input line currents are strictly regulated by the harmonic requirements set by IEEE Standard 519 [9]. However, those generated harmonics will not only degrade the grid-side power quality, but also produce the excessive torque ripples on the motor and even excite the LC resonance, which bring great challenges to the CSC based electric machine system. Therefore, operation of HP CSC energy conversion system with low switching frequency requires appropriate modulation and control techniques to contain the steady-state low-order current harmonics.

A. Mitigation of Discretization Error

The SHE provides superior harmonic performance than TPWM and SVM at low switching frequency, but suffers from limited dynamic performance and is difficult to be used in low speed range. The implementation of TPWM should meet special requirements to satisfy the switching constrains for CSC, which is also difficult to improve the harmonic performance. On the other hand, SVM features flexibility of sequence arrangement and easy digital implementation. Therefore, this section mainly focuses on the SVM techniques to eliminate the low-order harmonics.

Modulation schemes based on the natural sampling (NS) technique generate the modulated waveforms with superior harmonic performance due to the accurate dwell time calculation. However, the discretization error always exists in digital implementation of conventional SVM due to the low sampling frequency. Fig. 5 illustrates the dwell time calculation and vector selection in sector I based on NS SVM and conventional SVM, respectively. As can be seen, the dwell times of the conventional SVM are calculated once in the beginning of the sampling period and are maintained fixed within the whole period, while NS SVM calculates the dwell time on a basis of a continuous approach so that the compared dwell time is more accurate. From the vector arrangements at the bottom in Fig. 5, it can be observed that deviation of dwell time of space vectors exists in the conventional SVM, which is the reason why distinct low-order harmonics are generated in the modulated converter currents [10].

Many research works have been conducted to reduce the low-order harmonics under low switching frequency by using the SVM. Different vector sequences of conventional SVM combining with the synchronization method are investigated in [11] to generate the minimum magnitudes of the low-order (mainly 5th and 7th order) harmonics. It is indicated that harmonic performance of modulated currents can be improved by selecting two vector sequences under different modulation indexes. However, this method depends on the conventional SVM and the overall performance is still limited. A minimum harmonics tracking technique, which utilizes a feedback concept and calculate the dwell time four times in one sampling period, is proposed in [12] to minimize the 5th and 7th order harmonics. This method can improve the low-order harmonics performance to some extent, but suffers from complex digital implementation online.

The multisampling SVM is proposed for PWM CSC in [13]. A sampling ratio is defined by dividing the sampling frequency by the fundamental frequency. With higher sampling ratio, the calculated dwell time is closer to that of the NS-based technique so as to reduce the deviation error of dwell time. However, the switching frequency may be slightly increased with this method due to the sector transition and
multi-intersection between the discrete dwell time wave and the carrier wave. In order to achieve an approximate NS effect under the limited several-hundred-Hz switching frequency, Wei et al. [14] derived the precise equations on the basis of the Newton–Raphson iteration algorithm to solve the nonlinear calculation of dwell time and obtain the dwell time of space vectors accurately, which gives the good low-order harmonics performance.

Comparing the four optimized modulation schemes, it is indicated that the combined schemes [11] is simple but the harmonic performance is limited. The minimum harmonics tracking technique [12] and the multisampling SVM [13] need to calculate the dwell time multi-times within one switching period, which features for complex digital implementation. The natural-sampling-based SVM [14] only need to calculate the dwell time once, but nonlinear equations that based on the theory derivation are needed to be solved, which may requires the high performance digital processor. Therefore, the SVM scheme featuring good harmonic performance with easy digital implementation should be further investigated.

B. Mitigation of Overlapping-period Effect

On the other hand, the generated low-order harmonics in modulated currents due to the overlapping-period effect is recently investigated and solved in [16]. Overlapping periods are normally placed at the end of switching signals to ensure the proper switching commutations. The ideal commutation situations of power switches are shown in Fig. 6(a), where \( t_d \) denotes the overlapping period. The dwell time \( T_1 \), \( T_2 \) and \( T_0 \) are expected to remain as calculated during the whole switching periods. However, the real commutation processes of power switches are decided by different AC-side three-phase voltages

\[
U_a > U_b > U_c > U_d
\]

of PWM CSCs. For instance, the switching situations of power switches \( S_1, S_2, S_4 \) and \( S_6 \) of PWM CSR under the three-phase voltages of \( U_a > U_b > U_c \) in sector I are shown in Fig. 6(b)-(1). During the whole sampling period, \( S_1 \) remains on state while \( S_5 \) and \( S_4 \) turn on in sequence. During the first overlapping period, both \( S_2 \) and \( S_4 \) receive the turn-on signal. However, \( S_2 \) will turn off due to the biased voltage \( U_a > U_b \) so \( S_5 \) will keep on state until the end of dwell time \( T_1 + t_d \). Commutations of \( S_2 \) and \( S_4 \) are similar during the second overlapping period. It indicates that the dwell time of \( S_2 \) remains unchanged as \( T_2 \), but the dwell time of \( S_4 \) has a deviation of \( t_d \) under voltage relation of \( U_a > U_c \), which are different from that of the ideal situations. The commutation processes under other voltages relations can be derived accordingly, as shown in Fig. 6(b)-(2) to Fig. 6(b)-(4). Those dwell time deviation results in the low-order harmonics in the modulated converter currents.

An optimal overlapping-period distribution method is introduced in [16] to solve the overlapping effect. Different from placing the overlapping period at the end of switching signal with the traditional SVM scheme, the proposed method distributes the overlaps depending on the measured AC-side capacitor voltage information. The switching commutations of \( S_1 \), \( S_2 \), \( S_4 \) and \( S_6 \) with the proposed method under the voltage relations of \( U_a > U_b > U_c \) are exemplified in Fig. 6(c)-(1). As can be seen, the overlapping period is distributed ahead of the turn-on signal of \( S_5 \) and \( S_4 \), which is different from that of traditional SVM in Fig. 6(b)-(1). Under this circumstance, the conductions of \( S_2 \) and \( S_4 \) is hindered by reverse voltages during commutations. It is indicated that the dwell time of space vectors remains the same as calculated under all voltage relations with the proposed method as shown in Fig. 6(c)-(1) to Fig. 6(c)-(4). Therefore, the harmonic performance of modulated converter currents is effectively improved.

The harmonic performance of converter currents \( i_{na} \) with both the traditional SVM and the proposed SVM scheme have been conducted in experiments, as shown in the Fig. 7(a) and Fig. 7(b), respectively. \( Pat \) indicates the switching patterns of
the proposed method. With the traditional SVM, the Pat keeps zero to assign the overlaps at the end of switching signals. As can be seen, the 5th and 7th order harmonics of $i_{sa}$ are -8.24dBm and -26.5dBm. On the other hand, the Pat of the proposed method changes according to the AC-side voltage information as presented in Fig. 7(b). The 5th and 7th order harmonics are reduced correspondingly, which verifies the effectiveness of the proposed distribution method.

IV. LC RESONANCE SUPPRESSION

In the CSCs fed electric machine systems, three-phase capacitors ($C_{g}$ and $C$) are required on ac sides of both CSR and CSI to assist switching commutations and filter high-frequency current harmonics. However, the LC resonance problem can be caused from either the grid side or machine side due to the LC filters, as shown in the single-phase equivalent circuits of grid and machine side in Fig. 8. The series and parallel LC resonances happen when the low-order harmonics are contained in the modulated converter currents and line voltages, resulting in the issues of distorted line and machine currents and even the system instability [17]. Previous researches of LC resonance suppression are mainly studied under the normal operation conditions for CSC-based system [17-26]. Recently, the LC resonance suppression under the fault-tolerant operation conditions of current source drives has also been conducted in [27, 45] to improve the phase currents quality of the electric machine.

A. LC Resonance Suppression Under Normal Conditions

In the HP CSC based electric machine system, the capacitor is usually in the extent of 0.3p.u. to 0.6p.u. and the filter inductor ranges from 0.1p.u. to 0.15p.u. in the grid side. The grid-side LC filter forms the resonant frequencies varying from 3.3p.u. to 5.8p.u., which covers the 5th order harmonic and may arouse the LC resonance if system is insufficient damped [10]. On the machine side, the filter capacitor and the stator inductance have values of 0.3p.u. to 0.6p.u. and 3p.u. to 5p.u., respectively. The resultant resonant frequencies vary from 0.6p.u. to 1.0p.u., which is within the motor operation frequency and may result in the system instability [14].

Take the LC resonance of PWM CSR, as shown in Fig. 8(a), for example, the grid-side transfer function of series and parallel LC resonances can be derived as:

$$I_{g} = G_{s}(s)I_{sa}(s) + G_{v}(s)U_{j}(s)$$

$$= \frac{1}{s^{2}L_{g}C_{g} + sR_{g}C_{g} + 1}I_{sa}(s) + \frac{sC_{g}}{s^{2}L_{g}C_{g} + sR_{g}C_{g} + 1}U_{j}(s)$$

(2)

It indicates in (2) that the LC filter forms a second-order system and the corresponding resonant frequency is $\omega_{r} = \sqrt{L_{g}C_{g}}$. The magnitude-frequency characteristics of transfer function $G_{s}(s)$ from rectifier current and transfer function $G_{v}(s)$ from grid voltage with 3.3p.u. and 5.8p.u. resonance frequencies are presented in Fig. 9 (the series resistor $R_{g}$ is set at 0.05p.u. in this case). It is illustrated that the PWM CSR suffers severe parallel LC resonances arising from the harmonics of modulated rectifier currents.

The passive damping resistors are always avoided particularly in HP applications mainly due to the cost of power losses [17]. Active damping methods based on the virtual resistor are preferred to damp the possible resonance and maintain the efficiency at the same time. A number of active damping strategies have been studied to suppress the LC resonance either from the grid side or the machine side in the CSCs fed drive. Generally speaking, the virtual resistors of active damping methods can be connected in series or in parallel with the LC filter, as shown in Fig. 10. Active damping methods using the proportional capacitor-voltage feedback (CVF) and the derivative inductor-current feedback (ICF) are introduced for HP PWM CSR in [17] and [18], respectively. It is indicated that both methods can effectively suppress both parallel and series resonances. Li et al. [19] proposed a hybrid method combining the CVF and three-step modulation signal regulator to suppress both the transient and steady state LC resonance. Bai et al. [20] comprehensively investigated and analyzed different variables feedback controls to damp the LC resonance of CSR. It indicates that the damping effect can be effectively improved with a combination of different state variables.

As for the CSI-fed drives, a simple CVF is used to damp the possible multiple LC resonances for the CSI based multi-motor applications in [21]. The dynamic capacitor voltage control (DVC) method and the hybrid modulation strategy (SHE and
SVM) under low switching frequencies are designed for the HP CSC fed drives in [22-23]. This DVC method utilizes the fundamental capacitor voltage closed-loop control to suppress the steady and transient LC resonance. Furthermore, Zhang et al. [24] investigated the system resonance caused by the distortion of DC-link current due to the small DC-link inductor and the low switching frequency. Harmonics and interharmonics with a set of possible frequencies are generated by the harmonics interaction between the CSR and CSI through DC-link inductor. The damping method of DC-link virtual impedance is introduced to suppress the resulted harmonics and system instability.

In terms of the more commonly used SHE scheme, Zhou et al. [25] presents the selective harmonics compensation (SHC) technique to realize the active damping of grid current harmonics introduced by the background harmonics of grid voltages. Different sets of switching angles should be off-line calculated and saved in lookup tables with the SHC. However, there exist drawbacks in this method: (1) both calculation and storage are challenging considering the mitigation of multi-harmonics; (2) the compensation effect may be limited due to the one sampling delay of compensation signals. Different from SHC, Zhang et al. [26] directly modified SHE to realize the real-time harmonic compensation. This is realized by adjusting the phase angle with compensation signals, which can be calculated with algebraic equations. This method does not require establishing lookup tables and the online active harmonic compensation can be achieved using SHE technique.

**B. LC Resonance Suppression Under Fault-Tolerant Operation Conditions**

Recently, the LC resonance suppression under the fault-tolerant operation has been investigated in the CSC based six-phase permanent-magnet synchronous motor (PMSM) drives [27, 45]. The dq-axis current values of CSIs under normal operation conditions are DC quantities to generate the steady electrical torque. Three-phase currents references can be obtained by applying the reverse park transformation to the dq-axis current references. It is expected that only the fundamental components are contained in the three-phase currents of machine, so that no LC resonance would be excited due to the harmonics.

The system structure of the cascaded CSCs fed machine system with the phase-D opening fault occurring in one set of stator winding is illustrated in Fig. 11, where the set of stator winding with phase-ABC is defined as the healthy stator winding and the set of winding with phase-DEF is called the faulty stator winding. The phase angle of phase-E current should be controlled the same as that of phases-EF back EMF to generate the maximum electrical torque under phase-D open-circuit fault condition [28]. Under such conditions, the electrical torque generated by the faulty stator winding of machine is a double-frequency fluctuated component. The faulty inverter CSI1 can be operated as a single-phase inverter with one-phase opening fault. The compensation of capacitor current in CSI1 needs to be considered because the motor currents are coupled with inverter currents through capacitor currents. However, the LC resonance is not a big concern for CSI1 since only fundamental components are contained in the phase-E current of faulty stator winding.

As for the healthy inverter CSI2, the q-axis current value of the healthy stator winding is set as the periodic quantity superimposed by constant component to compensate the electrical torque fluctuation generated by the faulty stator winding. Under such condition, the design of d-axis current value of machine should be considered carefully because of the existence of the LC filter. Normally, the d-axis current value is set as zero to minimize the copper losses [28]. However, the low-order (mainly the third order) harmonics appear in the phase-ABC currents of the healthy stator winding with this setting of dq-axis current values, as shown in Fig. 12(a). Therefore, this d-axis current reference cannot be applied for the CSC module because the low-order current harmonics will stimulate the LC resonance between the filter capacitors and the motor inductors. To avoid this situation, a sine-function component with the same amplitude and frequency as the cosine-function component in q-axis current value is used in the d-axis current with the proposed reference design. As shown in Fig. 12(b), the phase-ABC currents of the healthy stator winding are sinusoidal with the special design of d-axis and q-axis current references. In addition, the
proportional-integral-resonant (PIR) controllers are used to track the periodical $d$-axis and $q$-axis current reference values of the healthy winding. Thus, the $LC$ resonance problem is prevented. More details of the reference design can be referred in [27, 45].

V. COMMON-MODE VOLTAGE MITIGATION

The CMV is generated by the rectification and inversion process in the current source drives. The CMV will appear between the neutral point of the stator windings of electric machine and the ground. Due to the existence of parasitic capacitance between the stator windings and the ground, the bearing current will be induced [29]. Fig. 13 shows the configuration of a kind of transformerless PWM CSC based drives [30]. The key is to invent an integrated DC-link choke, which includes the common-mode inductance of $L_{cm}$ and the differential-mode inductance of $L_{d}$. The neutral points of the grid-side and the machine-side filter capacitors are connected, in such a way that the stator winding of electric machine will not bear the CMV. Instead, the integrated DC-link choke will bear the CMV, so the isolation transformer in the traditional CSC fed drive system is saved. The size of the integrated DC-link choke can be further reduced when the CMVs from CSR-side and CSI-side are minimized. One effective way to realize the CMV mitigation is optimized design of the pulse patterns of modulation schemes [29-34].

As shown in Fig. 13, the CMVs in CSCs based system consist of the CSR-side CMV $CMV_{CSR}$ and the CSI-side CMV $CMV_{CSI}$, which are defined as following:

$$CMV_{CSR} = \frac{V_{pr-g} + V_{nr-g}}{2} \tag{3}$$

$$CMV_{CSI} = \frac{V_{pl-o} + V_{nl-o}}{2} \tag{4}$$

where $V_{pr-g}$ and $V_{nr-g}$ are the voltages at the CSR DC-link positive terminal ($p_r$) and negative terminal ($n_r$) with respect to the three-phase neutral $g$ of the grid; $V_{pl-o}$ and $V_{nl-o}$ are the CSI-side voltages with respect to the three-phase neutral $o$ of the machine. If the differential inductance $L_{d}$ in the positive DC link is equal to that in the negative DC link, the total CMV of the whole current-source drive $CMV_{o,g}$ can be defined by following.

$$CMV_{o,g} = CMV_{CSR} - CMV_{CSI} \tag{5}$$

![Fig. 13. Definition of CMV in transformerless current source drive system.](Image)

Various CMV mitigation methods have been designed for the current source drives, which mainly focused on the SVM scheme due to its flexibility of space vector arrangement and continuous modulation index adjustment [29]. The CMV values generated by different space vectors are given in Table I, where the CMV peaks can be up to the peak values of line voltages when zeros states of space vector are used. It is indicated in [30] that the peaks of CMV are mainly generated by the zero-states vectors, while the third-order harmonics in CMV are caused by the active-state vectors of the SVM scheme for CSCs. The peak value of CMV can reach as high as the sum of the CSR-side CMV peaks and CSI-side CMV peaks when their polarities are opposite.

Some of methods have been proposed to reduce the CMV without using the zero-state vectors of SVM. For example, Zhu et al. [29] introduced the nonzero-state modulation concept in VSC, such as the nearest three states (NTS) and the active-zero-state (AZS) modulation technique, for CSCs to reduce the CMV. Although these methods can effectively mitigate the CMV to some extent, they suffer from the reduced range of modulation index, higher switching frequencies and deterioration of power quality [30]. Therefore, CMV mitigation strategies with the zero-state vector selection have been proposed in [30-31], which allows the use of zero-state vectors. Minimization of CMV peak value or reduction of CMV average value is realized without affecting the modulation index range of SVM and the harmonics profile of modulated currents. A CMV reduction method based on the model-predictive control is introduced in [32], aiming at reducing the CMV peak value with optimal selection of space vectors on CSR-side and CSI-side simultaneously. However, higher sampling frequency or multisampling methods are required to achieve the reference track.

These methods [29-32] can be generally summarized as adjusting the pulse sequences to achieve the CMV mitigation. However, as low switching frequencies are used in HP CSC system, the harmonic performance of modulated converter currents are inevitably affected due to the adjustment of the pulse patterns [11]. On the other hand, considering low switching frequencies applied in HP drives, the low-order harmonic performance of the converter currents should be improved while the CMV mitigation is considered. The reference-trajectory-optimized SVM [33] and the NS SVM based CMV mitigation methods [34] are two methods proposed to realize the reduction of both the CMV and the low-order harmonics of modulated converter currents. The former one
implements the SVM-derived SHE scheme by incorporating relevant concepts from SVM into SHE, while the latter applies the NS-based SVM [14] scheme to mitigate the CMV of the CSR. However, investigations of improving both the harmonics and CMV performance are still rare, more researches should be encouraged as these two aspects are both important for the HP CSC fed electric machines.

VI. MODULAR CSCS FED SYSTEMS AND FUTURE TREND

A. Modular CSCs Fed Systems

With the increasing requirements of higher power capacity and reliability in HP industrial applications, the topologies of modular CSCs have been considered due to their advantages of high power capacity and module redundancy [35, 43]. There are two kinds of commonly used modular CSC topologies, namely, the parallel CSCs and the cascaded CSCs. The configurations of parallel CSCs and the cascaded CSCs with a single DC current source are shown in Fig. 14 as the exemplification. The parallel and cascaded CSC topology can increase the system power region without the connection of power switches in series or in parallel, thus eliminating the transient/steady-state voltage-sharing problem of series-connected and parallel-connected switches. In other words, low voltage/current rated power switches can be easily applied in the HP applications with these two topologies.

The parallel CSCs, also known as multilevel current source converters, offers several advantages in terms of high power capability and excellent quality of output current waveform under low switching frequency [35]. The parallel CSCs can be further divided into two types: The first type is direct parallel connecting of two back-to-back CSCs, which has independent DC current source for each paralleled CSI. In the second type, the paralleled CSCs share one DC current source, which can reduce the size and cost of the system [37]. However, the DC-link current balancing and the circulating current issue are challenging for the second type, as paralleled CSCs share the same DC current source and three-phase filter capacitors as shown in Fig. 14. Appropriate modulation and control strategies should be developed to solve these concerns of the parallel CSCs based system [36-37].

On the other hand, the cascaded CSCs share the common DC-link current, and thus the DC-link regulation is a challenge as each converter may have different DC-link requirements [38]. So far, some research works focusing on applying the cascaded CSCs to the WECs have been conducted. In [38], the cascaded PWM CSCs are applied on both offshore side and onshore side of WECs. This simple system topology can help eliminate the use of bulky and costly concentrated offshore converters required in the VSCs based counterparts. In [39], a novel medium-frequency isolated structure is proposed in the cascaded CSCs based offshore WECs to improve the power density and the system operation efficiency.

In addition, not only the power converters but also the electric machines have used the concept of redundant modules to increase the reliability and performance of HP generation and drive systems [40-45]. Multiphase machine is one typical candidate for the high-reliability HP applications, offering advantages of lower electrical torque ripple, higher power rating and fault tolerant capability [40]. Therefore, the multiphase machine systems fed by modular converters have attracted great attentions in some industry fields, for instance, ship propulsion, aerospace, electric vehicles and elevator traction system [42]. Many research works have been developed for the modular VSCs fed multiphase drives to improve the system performance and obtain high reliability with proper modulation and control schemes [40-42].

Recently, the coordinated strategies of modulation and control have been studied for cascaded CSCs fed multiphase machine systems in [44-45]. Fig. 15 shows the system structure of cascaded CSCs fed dual three-phase PMSM drive, where several CSCs are connected in cascade to convert power between the grid and the electric machine. The DC-link current ripple is an important factor in the CSC based drive system, since it will introduce extra power losses, low-order harmonics,
torque ripple and even system instability [46]. As shown in Fig. 16(a), the severe DC-link current ripple is generated in the back-to-back CSC fed drive systems operated under the low-speed region with low back-EMF. The reason lies in the large voltage difference between the voltage peak on the CSR side and the voltage peak on the CSI side. In Fig. 15, $V_{rd}$ and $V_{id}$ are the DC-link voltages on the sides of CSR and CSI, respectively. An improved pulse patterns arrangement has also been proposed to reduce the DC-link current ripple by collaborative SVM strategies of CSR and CSI in [46]. The good performance is obtained in suppression of DC-link current ripple under the similar AC voltages on CSR side and CSI side. But the AC terminal voltages on CSI side are variable while the AC terminal voltages on CSR side are constant for the applications of WECS. Therefore, the voltage difference between the CSR side and the CSI side will be large under the low-speed operation of WECS, and the collaborative design of SVM strategies on CSR side and CSI side is not enough to suppress the DC-link ripple. On the other hand, the cascaded CSC configuration presents an opportunity to optimize the SVM strategy of each CSC module on the single side of CSR or CSI, as shown in Fig. 16(b). Thus, the suppression of DC-link current could be achieved under various operation speeds of electric machine.

Fig. 17(a) and Fig. 17(b) show the comparison of experimental results with the traditional modulation and the proposed modulation, respectively. It can be observed in Fig. 17(a) that the CSR-side DC-link voltage changes from 0 to 150V, while the CSI-side DC-link voltage changes from 0 to 90V during the 200us sampling period. The obvious DC-link current ripple is produced consequently due to the large DC-link voltage difference between the voltage peaks on CSR side and CSI side. In Fig. 17(b), both the DC-link voltages of the cascaded CSRs and CSIs become smoother by using the collaborative SVM on the single side of CSR and CSI in [44-45]. Consequently, the DC-link current ripple is reduced significantly in Fig. 17(b).

B. Future Trend and Challenges

The PWM CSCs fed drives have been widely used in HP applications with low dynamic requirements, for example, fan and pumps. This is due to the low switching frequency and the dominant use of SHE scheme [1, 3]. However, with the development of power devices and the implementation of advanced modulation and control schemes, the PWM CSCs are regarded as the promising and competitive alternatives in other industrial applications, such as WECS [2, 5] and HVDC [7], due to the increased flexibility and dynamic performance. On the other hand, as the requirements of higher power capacity and reliability for HP industrial applications is increasing, the topology combining the modular CSCs with multiphase machines is regarded as an emerging trend, as discussed in Section VI-A.

In terms of the modulation and control scheme, the choice between the dynamic response and the harmonic performance a tradeoff in today’s HP CSCs fed drives. There are three possible technical solutions: the first solution is considering the harmonic modification of the traditional SVM scheme, which can take full use of the flexibility and easy digital implementation of SVM [10]; the second solution is combining the offline optimized modulation with advanced control scheme like stator flux trajectory control to achieve both good harmonic and dynamic performance under low switching frequency [47-48]; the last one is applying the model predictive control (MPC) to achieve the multi-objectives (low-order harmonic distortion and dynamic performance) optimization [32, 49]. However, researches regarding these three aspects for the HP CSC system is rare are present, more efforts should be made to improve the low-order harmonic performance and dynamic performance of the HP PWM CSC fed electric machines system.

VII. Conclusion

This paper presents a comprehensive review of recent developments of modulation and control schemes for HP PWM CSCs based electric machine systems, which are considered as a high-reliability system with the long-life DC-link choke and high immunity for short-circuit faults. The challenging issues in LC resonance suppression, low-order harmonics reduction, CMV mitigation and modular CSCs are discussed in PWM CSCs fed systems. In particular, the overlapping effects during
commutation, fault-tolerant operation and collaboration of cascaded PMW-CSCs are described. Finally, a brief discussion of the future trend and challenges of the HP PWM CSC fed electric machines system are presented. An overview of control and modulation schemes and related references are summarized in Table II for fast indexing.

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