A new interleaved ultra-large gain converter for sustainable energy systems

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Abstract
By inserting the secondary windings of the coupled inductors in series with the primary of the built-in transformer at the middle branch, a new concept is introduced for achieving ultra large voltage gain. The secondary and tertiary windings of the built-in transformer are inserted in the voltage multiplier cell. This configuration not only extends the voltage gain and minimises the voltage stress across power MOSFETs, but also gives a more flexibility to increase the voltage gain by the turns ratios of the built-in transformer and coupled inductors. Hence, high duty cycle is avoided and low voltage switches can be adopted which reduces the conduction losses. Also, the regenerative diode in each of the phases is connected to the other phase to improve equal current sharing performance. The energy of the leakage inductances is recycled by passive clamps and the high voltage spikes are avoided. Meanwhile, due to the leakage inductances of the magnetic means, the zero current switching of semiconductor devices is provided and the reverse recovery problem is alleviated. Finally, a 600 W prototype with 28–400 V voltage conversion and 97% conversion efficiency is built to demonstrate the performance of the converter.

1 INTRODUCTION

Ever increasing consumption of the fossil fuels leads to the problems such as shortage of these energy sources, global warming and air pollution. Sustainable clean energies such as photovoltaic (PV), fuel cell (FC) and wind have been attracted the engineers to provide a part of the consumed energy by local load and AC/DC grids. However, PV and FC have low DC output voltage that is usually lower than 50 V which demands for high step-up DC-DC converters to match with the demanded voltage of single phase inverters (around 400 V), three inverters and typical DC grids. However, PV and FC have low DC output voltage that is usually lower than 50 V which demands for high step-up DC-DC converters to match with the demanded voltage of single phase inverters (around 400 V), three inverters and typical DC grids. The duty cycle should be shifted to high values and the narrow OFF time decreases the controllability of the converter [1, 2]. Conventional boost converter cannot be considered as a suitable solution for high voltage gain applications. The duty cycle should be shifted to high values and the narrow OFF time decreases the controllability of the converter [1, 2]. On the other hand, the applied power switches suffer from hard switching and high voltage stress that is equal to the high output voltage. Therefore, power switches with high voltage ratings should be implemented. All of these factors increase the conduction losses and decreases the performance of the converter for high step-up applications. Step-up DC-DC converters assisted with the switched capacitor and switched inductor voltage multiplier cell (VMC) can obtain high voltage gains with lower duty cycles [3–11].

The VMCs are applied to the Luo converter in [3] to obtain high voltage gain and the generalised structure of this converter with lift stages and VMCs is proposed in [4] to achieve ultra-high voltage conversion ratio. However, the power MOSFET is in series with the input power source and as a result a pulsating current is drawn from the input. The conduction losses of the MOSFET is increased which decreases the efficiency, as well. Moreover, in the generalised structure, the voltage of the capacitors differs with each other which makes the design a bit complex. A dual inductor high step-up DC-DC converter based in Cockcroft–Walton VMCs is proposed in [5]. This converter merits the equal capacitor voltages in the VMCs and low input current ripple. However, the power switch is float and the common line-load ground is lost. A cascaded step-up DC-DC converter is proposed in [6] which utilises two units of switched-capacitors (SCs) to extend voltage gain. Although a quadratic...
voltage gain is achieved; however, due to cascaded power processing, the conversion efficiency is deteriorated. Moreover, too many components are required and the common line-load ground is lost. A family of expandable high voltage gain DC-DC converter with SC and switched inductor (SI) VMCs is proposed in [7]. The introduced converter utilises low number of passive components and the voltage stress across the semiconductors is considerably lower in comparison with the transformer less converters in the state-of-the-art. However, two switches are adopted without achieving the advantageous of the interleaving effect and the common line-load ground is lost. Another way to achieve high voltage gain and to reduce voltage stress across the MOSFETs is to implement active SI (ASI) network with SC VMC. In this way, two switches are synchronised and when the switches are in ON state, two inductors are charged in parallel and they are discharged in series while the switches are in OFF state [8]. However, the input current is pulsating and the common line-load ground is lost in this technique. The introduced converter in [9] adopts the similar concept in [8] with active SC (ASC) network and without the SC VMC. A quadratic voltage gain higher than its counterpart in [8] is achieved by compound structure of ASI and ASC. However, the main disadvantages pointed in [8] still exist. To decrease the input current ripple, sepic-based converters can be mentioned as a suitable alternative. The introduced sepic-based converter in [10] integrates discontinuous-current quazi Z-source converter with the SC VMC to increase voltage gain, reduce voltage stress across the semiconductors. However, too many reactive and semiconductor components should be implemented and the common line-load ground is lost.

Generally, in the converters of [3–11], the high output voltage is clamped by the capacitors of the VMC and the voltage stress across the power MOSFETs is decreased. However, to extend the voltage gain, the number of VMC modules should be increased which increases the converter complexity and decreases the conversion efficiency. To extend the voltage gain without increasing of VMCs, the coupled inductors are mixed within the VMC [11–20]. In such a case the voltage gain can be increased considerably by the turns ratio of the coupled inductor and the voltage stress across the power MOSFETs is decreased. Passive clamps are used in these converters to recycle the leakage energy of the coupled inductors which avoids high voltage spikes across the switches. Meanwhile, due to the leakage inductances, the zero current switching (ZCS) of the power switches is provided naturally that decreases the switching loss and alleviates the reverse current recovery problems of the diodes. The proposed converter in [11], replaces the inductor in conventional boost converter with the coupled inductor and two modules of SC VMCs are inserted in series with the coupled inductor boost converter. Also the voltage gain is increased; however, too many capacitors are diodes are needed and the input current ripple is pulsating. A high step-up converter with three-winding coupled inductor and SC VMC is proposed in [12]. By implementing of dual-switches technique with synchronised gate pulses, the voltage gain is increased and the voltage stress across the MOSFETs is decreased. However, as a single-phase structure, the number of the components is very high and the common line-load ground is lost. Moreover, the isolated gate drive circuits should be implemented that increases the system cost. The proposed converter in [13] integrates an autotransformer and a coupled inductor to further increase the voltage gain with low number of components. A boost-zeta converter based on VMC mixed with coupled inductors is introduced in [14]. The main drawback of such integrated topologies is the balancing of the output capacitors which increases the control complexity. To increase the voltage gain while maintaining the low number of diodes and capacitors, the capacitor and diode of the VMC share the load ground in the introduced topology in [15] which instead the common ground between source and load is lost with this technique. A family of module integrated step-up converters with dual coupled inductors are introduced in [16]. The voltage gain can be flexibly increased by the turn ratios of the coupled inductors and the voltage stress across the active switches is decreased, considerably. However, the main drawback of large input current ripple is still existing. An ultrahigh voltage gain converter is proposed in [17] with hybrid combination of SC VMC and coupled inductors. Unfortunately, too many components are needed which considerably increases the cost and control complexity. Symmetrical SC VMC is successfully integrated in an expandable structure assisted with coupled inductor to achieve high voltage gain in [18]. The voltage stress across the MOSFET is considerably decreased due to the clamp of the output voltage by the capacitors of VMCs. To further improve of the voltage gain, the number of VMC modules can be increased. However, high inrush current due to charging of different SCs should be taken into account during start-up stage. To decrease the input current ripple, the primary winding of the coupled inductors is inserted within the VMC and the secondary winding is placed is series with the output diode in the converter of [19]. The input boost inductor reduces the power source current ripple, effectively. However, the voltage gain extension is limited in comparison with the previously discussed converters with coupled inductors.

Unfortunately, single switch converters can't handle high power levels with high efficiency. Another shortcoming of the single switch converters is high input current ripple that deteriorates the life time of the PV panel and FC. The interleaved converters are the promising solution for high efficiency and high power applications [20–43]. Due to current distribution between the two phases of the interleaved converters, the thermal stress and current stress of the component is decreased considerably and the input current ripple is minimised by 180° phase shift of the gate pulses of the power MOSFETs. Interleaved converters with built-in transformer VMC have been proposed in [20–22]. Due to the balanced flux in the magnetic core of the built-in transformer, the high DC magnetising current does not exist and the saturation is avoided even with low size of the cores. The turns ratio of the built-in transformer is the key parameter to extend the voltage gain in these converters. A modular high step-up converter with coupled inductor has been proposed in the [23] to handle high power levels. However, the input current is not shared equally between the inductors and despite of using too many components the voltage is not increased considerably in this converter. Cross coupled
winding architecture has been proposed in [24–28] to increase current sharing performance and voltage gain. Two or three sets of three winding coupled inductors are implemented in these converters in which the tertiary winding is placed in the other phase. However, too many components are needed to extend the voltage gain. By integrating the interleaved boost converter with forward-flyback concept, the voltage gain increased in the converters of [29–32]. However, balancing of the output stacked capacitors makes the control system more complex and also the common line-load ground is missed in [32]. Asymmetric coupled inductor VMC scheme has been introduced in [33, 34] to extend voltage gain. Although the number of the components is decreased in such structures, unfortunately, the input current is shared between the primary windings of the couple inductors, unequally. An ultra-high step-up converter assisted with coupled inductors and voltage quadrupler is proposed in [35, 36]. The main shortcoming of this converter is the lost common ground between input power source and the output which may result the leakage current to pass along with the circuit in the case of PV applications. The proposed converter in [37] utilises the input parallel and output series scheme to extend the voltage gain. However, too many diodes and capacitors should be applied which increases the volume, cost and control design of this converter. Moreover, the input current ripple is high which cancels out the major benefits of interleaved characteristics. A high voltage gain converter with coupled inductor is introduced in [38]. Due to share of the VMC between the two phases and voltage doubler scheme at the output side of the converter, the voltage gain is considerably extended with low number of the components. An ultra-high step-up converter with multiple coupled inductors has been proposed in [39]. The passive clamp circuit is integrated in the switched capacitor VMC and the secondary sides of the first and second sets of the coupled inductor are inserted in series with the primary side of the third coupled inductor. In such a case the voltage gain is increased considerably and the voltage stress across the power switches is minimised.

To obtain an extra degree of freedom for voltage gain extension, better device utilisation and power density improvement, the coupled inductor and built-in transformer can be utilised simultaneously to extend voltage gain [40–42].

This paper proposes a novel high step-up interleaved converter with the following features:

1. By inserting the secondary windings of the coupled inductors in series with the primary of the built-in transformer at the middle branch, ultra large voltage gain is achieved
2. Due to the fact that the voltage gain can be extended with the turns ratios of the coupled inductor and built-in transformer simultaneously, an extra degree of freedom is yield in comparison with the converters with just coupled inductors or built-in transformer
3. The number of the component is low
4. Improved current sharing performance is achieved
5. The switching devices are operated with ZCS
6. The input current ripple is minimised
7. High efficiency

This paper is organised as follows. In Section 2, the proposed converter and operational principle is discussed. In Section 3, the steady-state analysis along with the performance comparison is given. In Section 4, the design considerations are described. In Section 5, the experimental verification is provided that is followed by the conclusion in Section 6.

## 2 | PROPOSED CONVERTER AND OPERATING PRINCIPLE

The power circuit of the proposed converter along with its equivalent circuit is shown in Figure 1. It consists of two sets of coupled inductor, a three winding built-in transformer, two power MOSFETs $S_1$, $S_2$; two clamp diodes $D_{C1}$, $D_{C2}$; two clamp capacitors $C_{C1}$, $C_{C2}$; two regenerative diodes $D_{r1}$, $D_{r2}$; two multiplier capacitors $C_{m1}$, $C_{m2}$; two output diodes $D_{o1}$, $D_{o2}$ and an output capacitor $C_o$. $C_{S1}$, $C_{S2}$ are the intrinsic parallel capacitors of the power MOSFETs; $I_{m1}$, $I_{m2}$ are the magnetising inductance of the coupled inductors; $I_{L1}$, $I_{L2}$, $I_{L3}$, $I_{L4}$ are the leakage inductances of the coupled inductors and $I_{L1}$, $I_{L2}$, $I_{L3}$ are the leakage inductances of the built-in transformer. The turns ratio of the coupled inductors and built-in transformer are defined as $n = n_2/n_1$ and $N = N_2/N_1$, respectively. The secondary windings of the coupled inductors are connected in series with the primary winding of the built-in transformer while the secondary and tertiary windings of the built-in transformer are inserted in with the VMGs. The branches are...
more cross coupled to each other by connecting the regenerative diodes of each VMC in the other phase which improves the current sharing performance.

The key waveforms of the proposed converter and the equivalent circuits in each of the operational modes are shown in Figure 2 and Figures 3 and 4, respectively. There are twelve modes of operations in one switching period. Due to the symmetry of the operations only six modes are described.

Mode 1 \( [t_0 - t_1] \): During this mode, power MOSFETs \( S_1 \) and \( S_2 \) are in ON state and all of the diodes are reverse biased. The magnetising inductances, \( L_{m1} \) and \( L_{m2} \), are being charged in a linear way by the input voltage. The current that passes through the leakage inductances and the power MOSFETs is equal to the current of the magnetising inductances. The output capacitor is supplying the load during this mode.

\[
i_{Lm1}(t) = i_{Lk11}(t) = i_{S1}(t) = \frac{V_{in}}{L_{m1} + L_{k11}} (t - t_0) + i_{Lm1}(t_0).
\] (1)

Mode 2 \( [t_1 - t_2] \): At time \( t_1 \), MOSFET \( S_2 \) is turned OFF. \( S_1 \) is in ON state and all of the diodes are reverse biased. The parallel
capacitor \(C_{S2}\) is charged rapidly by the current of \(i_{m2}(t)\) and the drain-source voltage of MOSFET \(S_2\) is increased in an approximately linear way. \(L_{m1}\) continues charging by the input voltage. Due to the increasing of the \(v_{CS2}(t)\), the voltage of \(L_{m2}\) is decreased which consequently decreases its charging rate.

\[
r_{CS2}(t) = r_{DS2}(t) = \frac{i_{m2}(t)}{C_{S2}} (t - t_1) \quad \text{AE-3}. \tag{3}
\]

Mode 3 \([t_2 - t_3]\): At time \(t_2\), the voltage of the \(r_{DS2}(t)\) is high enough to turn ON the clamp diode \(D_{C2}\) and the output diode \(D_{o2}\). Accordingly, \(S_1, D_{C1}\) and \(D_{o2}\) are in ON state and \(S_2, D_{C2}\) and \(D_{o1}\) are in OFF state. The energy of the leakage inductance \(L_{k21}\) is recycled by the \(D_{C2}\) to the clamp capacitor \(C_{C2}\) avoiding high voltage spikes on MOSFET \(S_2\). Moreover, the energy of the magnetising inductance \(L_{m2}\) transfers to the secondary sides of the coupled inductors. As a result, the passing current through the tertiary winding of the built-in transformer reflected from its primary side, discharges the multiplier capacitor \(C_{m2}\) and is delivered to the load via \(D_{o2}\).

\[
\dot{i}_{m2}(t) = \frac{V_{m} - V_{CC2}}{L_{m2}} (t - t_2) + \dot{i}_{m2}(t_2). \tag{4}
\]

\[
i_{D_{o2}}(t) = \frac{[N(n + 1) + 1]V_{CC2} + V_{Cm2} - V_{out}}{L_{k3b}} (t - t_2). \tag{5}
\]

\[
\dot{i}_{l_{kl1}}(t) = \dot{i}_{l_{m1}}(t) + nN\dot{i}_{D_{o2}}(t). \tag{6}
\]

\[
\dot{i}_{l_{kl2}}(t) = \dot{i}_{l_{m2}}(t) - nN\dot{i}_{D_{o2}}(t). \tag{7}
\]

\[
\dot{i}_{l_{kb1}}(t) = -N\dot{i}_{D_{o2}}(t). \tag{8}
\]

\[
i_{DC2}(t) = \dot{i}_{l_{m2}}(t) - [N(n + 1) + 1]\dot{i}_{D_{o2}}(t). \tag{9}
\]

\[
r_{CS2}(t) = r_{DS2}(t) = \frac{1}{C_{S2}} \int_{t_2}^{t} \dot{i}_{DC2}(t) dt + r_{CS2}(t_2) \quad \text{AE-3}. \tag{10}
\]

Mode 4 \([t_3 - t_4]\): At time \(t_3\), the energy of the leakage inductance is fully released to the clamp capacitor \(C_{C2}\) and the clamp diode \(D_{C2}\) is turned OFF. \(S_1, D_{C2}\) and \(D_{o2}\) are in ON state and \(S_2, D_{C1}, D_{C2}, D_{o1}\) and \(D_{o2}\) are in OFF state. The stored energy of \(C_{C2}\) is transferred to the multiplier capacitor \(C_{m1}\) via the secondary winding of the built-in transformer and \(D_{o2}\). Similar to the previous mode, the magnetising inductances \(L_{m1}\) and \(L_{m2}\) are being charged and discharged, respectively.

\[
i_{D_{o2}}(t) = \frac{[N(n + 1) + 1]V_{CC2} - V_{Cm1}}{L_{k2b}} (t - t_3). \tag{11}
\]

\[
i_{l_{o2}}(t) = \frac{i_{m2}(t_3)}{N(n + 1) + 1} - \frac{N(n + 1) + 1}{N(n + 1) + 1} i_{D_{o2}}(t). \tag{12}
\]

\[
i_{l_{m1}}(t) = \dot{i}_{m1}(t) + [N(n + 1) + 1]\dot{i}_{D_{o2}}(t). \tag{13}
\]

\[
i_{l_{l_{k11}}}(t) = \dot{i}_{l_{m1}}(t) + nN[\dot{i}_{D_{o2}}(t) + \dot{i}_{D_{o2}}(t)]. \tag{14}
\]

\[
i_{l_{l_{k21}}}(t) = \dot{i}_{l_{m1}}(t) - nN[\dot{i}_{D_{o2}}(t) + \dot{i}_{D_{o2}}(t)]. \tag{15}
\]

\[
i_{l_{l_{k1b1}}}(t) = -N[\dot{i}_{D_{o2}}(t) + \dot{i}_{D_{o2}}(t)]. \tag{16}
\]

Mode 5 \([t_4 - t_5]\): At time \(t_4\), the current that flows through the output diode \(D_{o2}\) reaches to zero and it is turned OFF with ZCS. \(S_1\) and \(D_{o2}\) are in ON state and \(S_2, D_{C1}, D_{C2}, D_{o1}\) and \(D_{o2}\) are in OFF state, during this mode. No current passes through the tertiary winding of the built-in transformer and its secondary winding transport the current. The energy of the clamp capacitor is still transferring to the multiplying capacitor \(C_{m2}\).

\[
i_{D_{o2}}(t) = \frac{\dot{i}_{m2}(t)}{N(n + 1)}. \tag{17}
\]
Mode 6 \([S_2 - t_6]\): At time \(t_6\), the gate pulse for MOSFET \(S_2\) comes and turns it ON with ZCS performance. \(S_1\) and \(S_2\) are in ON state and \(D_{C1}, D_{C2}, D_{o1}\) and \(D_{o2}\) are reverse biased, during this mode. The current of the leakage inductance \(L_{k21}\) increases rapidly and consequently the currents that pass through the windings of the built-in transformer and the secondary windings of the coupled inductors are decreasing during this mode. The falling current rate of \(D_{o2}\) is controlled by the leakage inductance and the reverse recovery current is alleviated. At time \(t_6\), these currents reach to zero and \(D_{o2}\) is turned OFF with ZCS.

\[
\frac{dI_{D22}(t)}{dt} = \frac{V_{CC2} - V_{Cm1}}{L_{t2}}.
\]

(19)

3 | STEADY-STATE ANALYSIS AND PERFORMANCE COMPARISON

To simplify the analysis, the leakage inductances of the magnetic devices and the parallel capacitors of the power MOSFETs are neglected. Also, all capacitors are large enough and their associated voltage ripple is assumed to be zero. Due to the symmetry of the operation it can be considered that \(V_{CC1} = V_{CC2} = V_{CC}\); \(V_{Cm1} = V_{Cm2} = V_{Cm}\); and \(I_{Lm1} = I_{Lm2} = I_{Lm}\). In which \(I_{Lm1}\) and \(I_{Lm2}\) are the average value of the current that passes through the magnetising inductances of the coupled inductors.

3.1 | Voltage gain expression and the average value of the current that passes through the magnetising inductances

When \(S_2\) is on, the voltage across the \(L_{m1}\) is the input voltage \(V_{in}\). When \(S_2\) is OFF, this voltage is \(V_{in} - V_{CC}\). By applying the vold-second balance principle to \(L_{m1}\), the voltage of the clamp capacitors is obtained as

\[
V_{CC1} = V_{CC2} = V_{CC} = \frac{V_{in}}{1 - D}.
\]

(20)

During modes 3 and 4, the following equations can be written

\[
V_{out} = [N(n + 1) + 1]V_{CC2} + V_{Cm2}.
\]

(21)

\[
V_{Cm1} = [N(n + 1) + 1]V_{CC2}.
\]

(22)

According to Equations (20)–(22), the voltage gain of the proposed converter can be expressed as

\[
M = \frac{V_{out}}{V_{in}} = \frac{2[N(n + 1) + 1]}{1 - D}.
\]

(23)

Figure 5 shows the voltage gain of the proposed converter versus duty cycle. It is seen that the voltage gain is increased considerably by increasing of the turns ratios of the magnetic devices and high voltage gains can be achieved at moderate duty cycles.

The average value of the current that passes through diode \(D_{o2}\) is half of the output current. Hence, according to Figure 2 we have

\[
I_{Lm1} = I_{Lm2} = I_{Lm} = \frac{N(n + 1) + 1}{1 - D}I_{out}.
\]

(24)

The average current that passes through the clamp diodes is half of the input current. Therefore; using Equation (24), one can obtain the time duration of Mode 3 \((\Delta t_{23})\) as below

\[
\Delta t_{23} = \frac{I_{out}}{I_{Lm}} I_S \{R3\}.
\]

(25)

3.2 | Voltage stresses of switching devices

The voltage stresses of the switching devices are given as below

\[
V_{DS1} = V_{DS2} = V_{DC1} = V_{DC2} = V_{CC} = \frac{V_{out}}{2[N(n + 1) + 1]}.
\]

(26)

\[
V_{Ds01} = V_{Ds02} = V_{Ds1} = V_{Ds2} = V_{out} - V_{CC} = \frac{2[N(n + 1) + 1]}{2[N(n + 1) + 1]}V_{out}.
\]

(27)

Figure 6 shows the normalised voltage stress across the power MOSFETs and the diodes versus turns ratio. It is clear that the voltage stress across the MOSFETs and the clamp diodes is substantially lower that the output voltage and decreased considerably by increasing of the turns ratios of the
magnetic means. Also, the voltage stress across the regenerative and output diodes is lower than the high output voltage. Therefore, low voltage rated switching devices can be adopted that reduces the conduction losses and improves the circuit performance.

### 3.3 Current stresses of the components

The current stresses of the components are obtained as below

\[
i_{\text{DC,Max}} = i_{\text{M,Max}} = \frac{N(n+1) + 1}{1-D} \frac{I_{\text{out}}}{2I_{\text{m}}}.
\]

\[
i_{\text{Dr,Max}} \approx \frac{N(n+1) + 1}{[N(n+1)](1-D)} I_{\text{out}}.
\]

\[
i_{\text{Do,Max}} \approx \frac{I_{\text{out}}}{1-D}.
\]

\[
i_{\text{DC,RMS}} = I_{\text{out}} \sqrt{\frac{N(n+1) + 1}{3(1-D)}}.
\]

\[
i_{\text{Dr,RMS}} = I_{\text{out}} \sqrt{\frac{N(n+1) + 1}{3[N(n+1)](1-D)}}.
\]

\[
i_{\text{Do,RMS}} = I_{\text{out}} \sqrt{\frac{1}{3(1-D)}}.
\]

\[
i_{\text{SRMS}} = I_{\text{out}} \sqrt{M^2 \left[ \frac{1}{4} + \frac{1-D}{12N(n+1)} \right] + \frac{2MN(n+1)}{3} + \frac{N(n+1)}{3(1-D)}}.
\]

\[
i_{\text{CC,RMS}} = \sqrt{i_{\text{DC,RMS}}^2 + i_{\text{Dr,RMS}}^2}.
\]

\[
i_{\text{CM,RMS}} = \sqrt{i_{\text{Dr,RMS}}^2 + i_{\text{Do,RMS}}^2}.
\]

\[
i_{\text{Co,RMS}} = \sqrt{2i_{\text{Do,RMS}}^2 - I_{\text{out}}^2}.
\]

\[
i_{\text{Lk1,1,RMS}} = N \sqrt{2i_{\text{CM,1,RMS}}^2 + \frac{I_{\text{out}}^2}{3(1-D)}}.
\]

\[
i_{\text{Lk2,1,RMS}} = \sqrt{i_{\text{Lm}}^2 + n^2 i_{\text{Lk1,1,RMS}}^2}.
\]

### 3.4 Input current ripple analysis

During mode 1, the ripple contents of the magnetising inductances currents are given by

\[
\Delta i_{\text{Lm1}} = \frac{D - 0.5}{I_{\text{m}}} V_{\text{in}}.
\]

\[
\Delta i_{\text{Lm2}} = \frac{D - 0.5}{I_{\text{m}}} V_{\text{in}}.
\]

Hence, considering \( I_{\text{m1}} = I_{\text{m2}} = I_{\text{m}} \), we have

\[
\Delta i_{\text{m}} = \Delta i_{\text{Lm1}} + \Delta i_{\text{Lm2}} = \frac{(2D - 1)V_{\text{in}}}{I_{\text{m}}}.
\]

\[
\Delta i_{\text{m}} = \frac{(2D - 1)(1-D)}{2[N(n+1) + 1]I_{\text{m}}} V_{\text{out}}.
\]

It is seen that the input current ripple is decreased considerably by increasing of the turns ratios of the magnetic means.

### 3.5 Soft switching of MOSFETs and diodes {R1-8}

In fact, natural ZCS turn-ON for MOSFETs and natural ZCS turn-OFF for diodes is realised by the leakage inductances of the magnetic means. During mode 5 (Figure 4(a)) the current of \( i_{\text{Lk21}} \) is equal to \( i_{\text{Lk22}} \). At the instant \( t_s \) while the gate pulse of \( S_2 \) comes, the current that passes through \( S_2 \) gets \( i_{\text{Lk21}} = i_{\text{Lk22}} \). Hence, due to the fact that the current of the leakage inductances cannot change suddenly, \( S_2 \) turns ON with natural ZCS performance. The slope of the rising current through the MOSFET can be controlled by the leakage inductances. According to the Figure 2, during modes 4 and 8, \( i_{\text{Do1}} \) and \( i_{\text{Do2}} \) are softly reaching zero and their falling rates are given in Equations (12) and (13). Moreover, during modes 6 and 12, the falling rates of
currents of $i_{Dr1}$ and $i_{Dr2}$ are limited by the leakage inductances to achieve ZCS at the turn-OFF instant whose equation is given in Equation (19).

According to Equations (12),(13),(19), the value of the leakage inductances $L_{k1}=L_{k2}$ can be effectively determined by specifying the corresponding falling rates of diodes, especially for regenerative diodes $D_{r1}$ and $D_{r2}$.

### 3.6 Efficiency analysis {R4-3}

In fact, the parasitic characteristics of the components affect the conversion efficiency and the voltage gain. Figure 7(a) shows the equivalent circuit of the proposed converter considering the parasitic resistors and forward voltage drops.

The MOSFETs losses are associated to the switching losses and conduction losses. Due to ZCS turn ON of the MOSFETs, the total losses of them can be expressed as

$$P_S = P_{OFF} + P_{Conduction} = \frac{k_BT}{2} \frac{P_{out}}{1-D} + (r_{S1} + r_{S2})i_{s,RMS}^2,$$

where $t_{f}$ is the fall time of the MOSFETs.

The forward voltage drops and the ON state resistances of the diodes dissipate some power while the diode is conducting. It is worth to mention that the switching losses of the diodes are negligible due to ZCS operation.

$$P_D = \frac{(V_{FDC1} + V_{FDC2} + V_{FD1} + V_{FD2} + V_{FDo1} + V_{FDo2})I_{out}}{2} + \frac{(r_{DC1} + r_{DC2})i_{D,RMS}^2 + (r_{Dr1} + r_{Dr2})i_{Dr}^2}{2} + \frac{(r_{Do1} + r_{Do2})i_{Do}^2}{2} i_{s,RMS},$$

The losses of the capacitor are associated to their equivalent series resistor

$$P_C = (r_{CC1} + r_{CC2})i_{CC,RMS}^2 + (r_{Cm1} + r_{Cm2})i_{Cm,RMS}^2 + r_{Co}i_{Co,RMS}^2,$$

The winding resistors of the magnetic windings cause a power dissipation that can be obtained by

$$P_{Wire} = (r_{l1} + r_{l2})i_{l,11,RMS}^2 + (r_{l2} + r_{l2} + r_{l22})i_{l,bb1,RMS}^2 + (r_{l3} + r_{l3})i_{l,bb2,RMS}^2.$$

The total losses of the proposed converter can be written as

$$P_{Loss} = P_S + P_D + P_C + P_{Wire}.$$

Therefore, the conversion efficiency and the voltage gain of the proposed converter are given by

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}},$$

$$M = \frac{2N(u + 1) + 2}{1 - D}.$$

The conversion efficiency and the voltage gain of the proposed converter are shown in Figure 7(b). The experimental specifications have been used for parasitic components that are given by:

$$V_{in} = 28 \text{ V}, V_{out} = 400 \text{ V}, f_s = 50 \text{ KHz}, R_o = 266 \Omega;$$

$$r_{S1} = r_{S2} = 4.5 \text{ m} \Omega, \ k_{OFF} = 88 \text{ ns};$$

$$N = u = 1; n_{l1} = n_{l21} = n_{l12} = n_{l22} = 12 \text{ m} \Omega;$$

$$n_{l2b} = n_{l3b} = 22 \text{ m} \Omega;$$

$$r_{DC1} = r_{DC2} = r_{Dr1} = r_{Dr2} = r_{Do1} = r_{Do2} = 0.01;$$

$$V_{FDC1} = V_{FDC2} = 1 \text{ V},$$

$$V_{FD1} = V_{FD2} = V_{FDo1} = V_{FDo2} = 1.2 \text{ V};$$

$$r_{CC1} = r_{CC2} = r_{Cm1} = r_{Cm2} = 20 \text{ m} \Omega; r_{Co} = 24 \text{ m} \Omega;$$
3.7 Performance comparison

A comparison between the proposed converter and some recently published interleaved converters has been done in the terms of number of the components, voltage gain, which is summarised in Table 1. All of the competitors utilise two power switches and have the merits of equal current sharing performance and common ground between input and output. Figure 8 shows the result of the comparison. It is seen from Figure 8(a) that the proposed converter and the converter of [42] have the highest voltage gain for \( n = N = 1 \). However, it is clear from Table 1 that the proposed converter has higher voltage gain than the one in [42] for \( N > 1 \). According to Figure 8(b), the voltage stress across the MOSFETs is the lowest in the proposed converter which facilitates utilisation of devices with lower ON-state resistance and cost. For all of the converters a diode with the highest voltage stress has been selected for the sake of comparison. Unfortunately, one can see from Figure 8(c) that the normalised maximum voltage stress across the diode in the proposed converter is the highest of all. However, all diodes in the proposed converter tolerate a voltage stress lower than the output voltage.

Another comparison is made between the RMS current stresses of the MOSFETs that is given in Table 2. To have a fair comparison, the turns ratio of the competitors is selected in such a way to achieve equal voltage gains and equal duty cycles. Figure 9 shows the result of this comparison. It is clear that at equal voltage gain, the normalised RMS current passing through the MOSFETs of the proposed converter is the lowest of all and the one in [37] has the highest value. Therefore, one can conclude that due to lower voltage stress and RMS current of the MOSFETs in the proposed converter, the MOSFETs utilisation factor that is defined by \( \frac{P_{out}}{\sum_{j=1}^{2} (V_{DS} \times i_{Sj,RMS})} \), is the lowest for the proposed converter in comparison with its competitors.

Although the proposed converter utilises a greater number of the components in comparison with the converters of [21, 28, 30], however, the voltage gain is considerably higher, the voltage stress across the power MOSFETs is effectively lower and the input current ripple is minimised. Also, in comparison with the ultra-large gain converters of [37, 40, 42], the proposed converter obtains the mentioned advantages with the lowest number of components. This is mainly due to the inserting of the secondary windings of the coupled inductors in series with the primary winding of the built-in transformer, in the middle branch. Low voltage rated semiconductors can be used which helps to decrease of the conduction losses and to increase the performance operation. Therefore, the proposed converter is suitable for high voltage and high power sustainable energy systems applications.

| Converters | Technique | M = \( \frac{V_{out}}{V_{in}} \) | \( V_{out}/V_{in} \) | \( I_{out}/I_{in} \) | Total | Input current ripple |
|------------|-----------|-----------------|-----------------|-----------------|-------|---------------------|
| Ref. [21]  | BT + VMC  | \( 2N + 2 \)    | \( \frac{1}{1-D} \) | \( \frac{1}{1-D} \) | Low  | Low                |
| Ref. [28]  | CI + VMC  | \( 2N + 2 \)    | \( \frac{1}{1-D} \) | \( \frac{1}{1-D} \) | Low  | Low                |
| Ref. [30]  | CI + VMC  | \( 2N + 2 \)    | \( \frac{1}{1-D} \) | \( \frac{1}{1-D} \) | Low  | Low                |
| Ref. [37]  | CI + VMC  | \( 2N + 2 \)    | \( \frac{1}{1-D} \) | \( \frac{1}{1-D} \) | Low  | Low                |
| Ref. [40]  | CI + BT + VMC | \( 2N + 2 \) | \( \frac{1}{1-D} \) | \( \frac{1}{1-D} \) | Low  | Low                |
| Ref. [42]  | CI + BT + VMC | \( 2N + 2 \) | \( \frac{1}{1-D} \) | \( \frac{1}{1-D} \) | Low  | Low                |
| Proposed   | CI + BT + VMC | \( 2N + 2 \) | \( \frac{1}{1-D} \) | \( \frac{1}{1-D} \) | Low  | Low                |

CI: coupled inductor, BT*: built-in transformer.
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FIGURE 8 Performance comparison of the proposed converter. (a) Voltage gain, (b) normalised voltage stress across MOSFETs (c) normalised voltage stress across diodes

TABLE 2 Comparison of the RMS currents of the MOSFETs

| Converter | RMS currents of the MOSFETs ($i_{\text{RMS}}$) |
|-----------|-----------------------------------------------|
| Ref. [21] | $I_{\text{out}} \sqrt{\frac{(2D-1)M^2 + (M + \frac{2N + 1}{1-D})^2}{4}} (1-D)$ |
| Ref. [28] | $I_{\text{out}} \sqrt{\frac{(2D-1)M^2 + (M + \frac{2x + 1}{1-D})^2}{4}} (1-D)$ |
| Ref. [30] | $I_{\text{out}} \sqrt{\frac{DM^2}{4} + \left(\frac{2x + 1}{3(1-D)} + M\left(\frac{1}{2}\right)\right)}$ |
| Ref. [37] | $(M-1)I_{\text{out}} \sqrt{\frac{1}{4D}}$ |
| Ref. [40] | $I_{\text{out}} \sqrt{\frac{DM^2}{4} + \frac{(3N + 2x + 2)M}{4} + \frac{(3N + 2x + 2)^2}{12(1-D)}}$ |
| Proposed | $I_{\text{out}} \sqrt{\frac{M}{4} \left[\frac{1}{4} + \frac{1-D}{12N(x+1)} + \frac{2MN(x+1)}{3} + \frac{N(x+1)}{3(1-D)}\right]}$ |

FIGURE 9 Comparison of the normalised current stresses of the MOSFETs

The value of the magnetising inductances is obtained based on the desired input current ripple which is given by

$$L_{m1} = L_{m2} = \frac{(2D-1)(1-D)}{2[N(x+1) + 1]\Delta_{\text{in}}f_s} V_{\text{out}}.$$  \hspace{1cm} (51)

Therefore, value of $n_1$ is yield from

$$n_1 = \frac{L_{m1}\Delta_{\text{in}}\Delta_{\text{out}}}{B_{\text{Max}}A_C}.$$  \hspace{1cm} (52)
where $I_{lm,\text{Max}}$ is the maximum value of the current through magnetising inductance, $B_{\text{Max}}$ is the maximum of the magnetic flux density and $A_C$ is the core cross-sectional area of the coupled inductors. From $n$ and $n_1$, the value of $n_2$ is obtained.

The voltage across the primary winding of the built-in transformer can be expressed as below

$$V_{\text{P,Built-In Transformer}} = \frac{V_{in}}{1-D} = \frac{N_p \Delta B A_C}{(1-D) F_s}.$$  \hspace{1cm} (53)

where $\Delta B$ is the variation of the magnetic flux density and $A_C$ is the equivalent area of the magnetic core of the built-in transformer. After selecting the proper $N_p$, the value of $N_s = N_t = N_p N$ is obtained, accordingly.

Proper selection of the wires of the magnetic devices depends on the RMS current that passes through each of them. These RMS values are given in Equations (36),(38),(39).

### 4.2 Design of the semiconductors

The voltage stress, maximum current and RMS current are three factors that should be taken into account while selecting the switching devices. These values are given in Equations (26)--(34).

### 4.3 Design of the capacitors

The capacitors are designed based on their voltage ripple.

\[ C_m = \frac{P_{out}}{2 F_s V_{out} \Delta V_{Cm}}. \] \hspace{1cm} (54)

\[ C_C = \frac{P_{out}}{2 F_s V_{out} \Delta V_{CC}}. \] \hspace{1cm} (55)

where $\Delta V_{Cm}$ and $\Delta V_{CC}$ are the voltage ripple across $C_m$ and $C_C$, respectively.

### 5 EXPERIMENTAL RESULTS

In order to better explore the merits of the proposed converter, a 600 W prototype with the 28 V input voltage to the 400 V output voltage conversion is built and tested in the laboratory. Figure 10 shows the photographs of the fabricated converter and experimental set-up. The specifications of the fabricated converter are given in Table 3. The experiments are carried out for full load (Figures 11–13) and half load (Figures 14 and 15).

Figure 11(a) shows the experimental result of the output voltage and the output current for full load condition. It is seen that a high output voltage of 400 V is achieved from the low input voltage of 28 V. Figure 11(b) shows the experimental results of the input current and the currents of the leakage

**TABLE 3** Specifications of the proposed converter

| Components | Parameters |
|------------|------------|
| Full load power ($P_{\text{out}}$) | 600 W |
| Nominal duty cycle | 60% |
| Input-output voltages ($V_{in} - V_{out}$) | 28 – 400 V |
| Switching frequency ($f_s$) | 50 kHz |
| Power MOSFETs ($S_1, S_2$) | IRFb4110PbF (100V, 4.5 mΩ) |
| Diodes ($D_{Cl(2)}$) | Schottky MBR20200 |
| Diodes ($D_{Di(2)}, D_{Dii(2)}$) | MUR1540 |
| Capacitors ($C_{Cl(2)}$) | 10 µF, 100 V |
| Capacitors ($C_{m(2)}$) | 10 µF, 250 V |
| Capacitor ($C_o$) | 10 µF, 500 V |
| Coupled inductors | $n = 1, L_m = 100 \mu H, L_{Lk} = 1 \mu H$ |
| Built-in transformer | $N = 1, L_m = 800 \mu H, L_{Lkb} = 5 \mu H$ |
inductances ($L_{k11}$ and $L_{k21}$) of the coupled inductors. Due to the interleaved operation of the MOSFETs, the input current ripple is minimised that is about 1 A (4.5% of the 22.1 A averaged input current). One can obtain the conversion efficiency of 97% from the measured input and output waveforms. Meanwhile, it is seen that the input current is shared relatively equally between the phases. Figure 11(c) shows the experimental results of the current that flows through the primary winding of the built-in transformer that is consistent with the key waveform of Figure 2. The correlated currents passing through $S_1$ and $S_2$ are shown in Figure 11(d). The maximum current flowing through the MOSFETs is about 24.3 A. Figure 12(a) shows the experimental results of the current and the voltage of the MOSFET $S_1$. The switch is turned ON with ZCS that reduces the switching losses. It is seen that the voltage stress of the power MOSFET is clamped successfully to the voltage of about 70 V that is substantially lower than the high output voltage. Hence, low power rated switches can be adopted with low on-state resistances which decreases conduction loss and improves circuit performance. The correlated currents of the $D_{C1}$ and $S_1$ are shown in Figure 12(b). The maximum
current of the $D_{C1}$ is about 13 A that is consistent with Equation (28). Figure 13(a)–(c) shows the experimental results of the current and voltages of the diodes. The maximum currents of the diodes $D_{r1}$ and $D_{o1}$ are about 3.5 and 4 A that are consistent with the mathematical analysis in Equations (29) and (30). Due to the leakage inductances of the magnetic devices, all of the diodes are turned OFF with ZCS and the reverse recovery problem is alleviated. Meanwhile, the measured voltage stresses of the diodes are about 70 V for $D_{C1}$ and 335 V for $D_{r1}$ and $D_{o1}$ that are consistent with the mathematical analysis in Equations (26) and (27). Therefore, low forward voltage drop diodes can be adopted in the proposed converter. The correlated currents of the $D_{o1}$ and $D_{o2}$ are shown in Figure 13(d) to verify the satisfactory interleaved operation of the proposed converter.

Figure 14(a) shows the experimental result of the output voltage and the output current for half load condition. The output voltage is 400 V and the output current is 0.75 A which yields 300 W output power. Figure 14(b) shows the experimental results of the input current and the currents of the leakage inductances ($I_{Lk11}$ and $I_{Lk21}$) of the coupled inductors. The input current ripple is minimised that is about 1 A (8.9%) of the
11.1A averaged input current). Accordingly, through the measured waveforms the conversion efficiency of 96.3% is achieved, as well.

Moreover, the equal current sharing performance can be again verified from the currents passing through $I_{L11}$ and $I_{L21}$. Figure 15 shows the experimental results of the voltage and current of each of the semiconductor devices. The voltage stresses are the relatively similar to the obtained ones in full load experimentations. Also, the ZCS turn-ON of the MOSFETs and ZCS turn-OFF of the diodes are again realised at half load conditions.

Figure 16 shows the dynamic performance of the proposed converter between full load and half load. It is seen that by introducing load step change, the output voltage is well regulated at 400 V with a proper settling time and low over/under shoot values.

Figure 17 shows the calculated (through Section 3.6) and measured experimental efficiency of the proposed converter. We used HIOKI 3256 DIGITAL HiTESTER (made in JAPAN), KYORITSU KEW MATE MODEL 2000 (made in JAPAN) and FUKIE FK9205X DIGITAL MULTIMETER for measurement of input and output power, then the efficiency obtained as $\eta = \frac{V_o I_o}{V_i I_i}$. It is seen that the

**FIGURE 15** Experimental results of the proposed converter at half load. (a) The voltage and current of $S_1$, (b) Voltage and current of $D_{c1}$, (c) voltage and current of $D_{d1}$, (d) voltage and current of $D_{o1}$

**FIGURE 16** Dynamic performance of the proposed converter between full load and half load

**FIGURE 17** Measured and calculated efficiency of the proposed converter
maximum efficiency is 97.3% that is obtained at about 500 W output power and the full load efficiency is 97%. At lower power values, the fixed iron losses of the magnetic devices degrade the measured experimental efficiency in comparison with the calculated efficiency. However, the calculated and measured efficiencies match each other by increasing of the load power. The detailed calculated loss break down of the components for 300 W (half load), 500 W (maximum achieved experimental efficiency) and 600 W (full load) are given in Table 4 along with their corresponding pie graphs in Figure 18. It is seen that the switching devices have the dominant dissipation is the proposed converter.

### 6 Conclusion

A high step-up interleaved DC-DC converter has been proposed in this paper. By integration of the coupled inductor and built-in transformer VMC in the proposed converter a flexible high voltage gain can be achieved while comparing with the converters with only one of these magnetic devices. The main advantages of the proposed converter are the high voltage gain, minimised voltage stress across the switching devices, enhanced current sharing performance, minimised input current ripple, ZCS operation of the switching devices. All of these factors contribute to enhance the circuit performance and to improve the conversion efficiency. Therefore, the proposed converter can be regarded as a suitable alternative when high step-up and high efficiency is required such as integration of the sustainable energy sources to the grid or local load. Finally, a 600 W prototype, with the 28 V input voltage to the 400 V output voltage and full load conversion efficiency of 97% has been built to demonstrate the effectiveness of the proposed converter.

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