Design of low noise electrical system for uncooled long wave infrared imaging

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Abstract. The research and design of low-noise imaging circuit is of great significance to enhance the imaging quality of the detector. To improve the imaging quality of an uncooled infrared imaging system, a low noise imaging circuit is designed. The generation scheme of bias voltage is emphasized, and the design methods of timing drive module and ADC conversion module are briefly described. A filter with a pass-band cutoff frequency of 1 Hz is designed at the bias voltage output to filter out high-frequency noise. The experimental results show that the precision of bias voltage is over 98% and the RMS noise of bias voltage below 1kHz is 1.4uV. The feasibility of other modules is verified by simulation and experiment.

1. Introduction

Since uncooled infrared imaging systems have many functions and features that cannot be achieved by refrigeration, it has been widely used in military and civil fields [1]. However, uncooled detectors are far less effective than refrigeration-type infrared detectors in terms of noise equivalent temperature difference (NETD) and response time. The imaging circuit of the uncooled infrared detector has a great influence on the performance of the imaging system [2, 3]. To solve the influence of the imaging circuit bias voltage on the detector, the researchers designed a low-noise power supply circuit with a power supply noise of less than 22uV [4]. For the uncooled infrared imaging system, a high signal-to-noise ratio acquisition circuit with an average NETD value of 223mK (with an integration time of 64us) has been designed [5]. Although the designed bias voltage circuit suppresses some power supply noise, it still does not meet the detector's requirements for a bias voltage noise.

Uncooled infrared detectors themselves have blind elements and non-uniform characteristics. The image quality of uncooled infrared imaging systems can be improved from the aspects of algorithms and data processing. However, if there is no low noise imaging circuit as the basis, this will make data processing very difficult and even impossible to obtain a complete infrared image.

Therefore, the research and design of low-noise imaging circuit is to fundamentally improve the imaging quality of the system [6,7]. A low noise imaging circuit based on UL04371-042 uncooled infrared detection of ULIS company is designed, and a practical imaging system is developed.
2. Imaging System

The imaging principle of uncooled infrared imaging system is shown in Figure 1. The infrared radiation emitted by the object is transmitted through the atmosphere and beamed on the focal plane of the detector. Driven by the readout circuit of the detector, the space and spectral information data of the target are got, and then displayed after data processing.

![Figure 1. Imaging principle of uncooled infrared imaging system.](image)

The readout circuit of uncooled infrared detector comprises four parts: bias voltage module, ADC module, TEC temperature control module and detector drive timing module.

Power module is the energy source of the whole imaging circuit system, and also the main source of noise. Hence, it is necessary to ensure both the driving capability of the power supply and the low noise of the power supply. In the design of power supply module, LDO chips are used to get the voltage needed by each module in the circuit.

The low noise bias voltage is the basis of the detector working in the best state. The low noise bias voltage circuit is composed of low noise LDO, reference voltage source, precise DAC and operational amplifier. The detector’s high-precision drive timing signal is provided by the FPGA. Digital timing signals are also a key factor in the operation of the detector. Using a low temperature drift active crystal as a clock source. The FPGA generates the signal required by the normal operation of the detector. The AD conversion module uses a 14-bit AD conversion to convert the analog signal output from the detector into a digital signal [8]. Second-order low-pass filtering is added to the analog output to reduce the high-frequency noise. Adjust the input range of the ADC chip to the output range of the detector (1.0V–4.2V).

3. Acquisition circuit design and noise suppression

The acquisition circuit is designed for ULIS’s UL04371-042 uncooled infrared detector. The acquisition circuit provides a bias voltage, drive timing, TEC temperature control and ADC for the detector.

3.1. Bias voltage focus plane performance impact

The noise equivalent temperature difference and detection rate (D*) are the main indicators of the performance of uncooled focal plane arrays (UFPA) [9]. The relationship between NETD \( \Delta T \) \( \text{D}^* \) and noise voltage are:

\[
NETD = \frac{4P_{\text{no}} \sqrt{V^2}}{A \pi R_T (dP/dT_i)}
\]
\[ D^* = \frac{R_V\sqrt{A\sqrt{f_U-f_L}}}{\sqrt{V^2}} \]  

\( \sqrt{V^2} \) is the rms noise voltage, \( A \) is the area of the pixel, \( \varepsilon \) is the emissivity, \( F_{no} \) is the F-number of the optical system, \( dP/dT_e \) is the derivative of the target radiation at temperature \( T_e \), \( f_U \), \( f_L \) is the upper and lower limit frequency, \( R_V \) is the voltage response rate.

The relationship between the voltage response rate(\( R_V \)) and the radiant flux(\( L \)) of the uncooled focal plane array is [10]:

\[ R_V = \frac{dV}{dQ} = V_b \frac{R_{Uf} \alpha}{(R + R_L)2g} \frac{1}{y} \left( 1 + \beta \frac{R - R_L}{R + R_L} \right)^{-1} \]  

\[ L = 2hc^2 \varepsilon \int_{\lambda_L}^{\lambda_H} \frac{d\lambda}{\lambda 5(\exp(hc/\lambda KT_e) - 1)} \]  

\( V_b \) is the bias voltage, \( \alpha \) is the resistance temperature coefficient of UFPA, \( \beta = \alpha \Delta T \), \( g \) is the thermal conductivity of UFPA, \( R \) and \( R_L \) are the impedance and load resistance of UFPA.

The noise of UFPA is diverse and complex. Among them are Johnson noise, 1/f noise and thermal noise. Finally, all noise is expressed in the form of electrical noise. Each UFPA cell requires a bias voltage for proper operation. Therefore, the noise in the UFPA is mainly derived from the focal plane array itself and the bias voltage.

**Figure 2.** Relationship between bias voltage and noise.

Figure 2 shows the curves of three kinds of noise and total noise of UFPA with bias voltage. As the bias voltage increases, thermal noise, and 1/f noise increase linearly. Johnson noise as a Gaussian white noise does not change with the bias voltage.

**Figure 3.** Relationship between bias voltage and NETD.

**Figure 4.** Relationship between bias voltage and \( D^* \).
Figures 3 and 4 are the relationship between noise equivalent temperature difference, detection rate and bias voltage. As the bias voltage increases, NETD and D* gradually decreases, but the rate of change gradually slows down. When the bias voltage is increased to a certain extent, NETD and D* no longer change. Therefore, to get better NETD and D*, the bias voltage needs to be the largest. However, the total noise increases rapidly with increasing bias voltage. Through the actual circuit experiment, when the bias voltage is $3 \sim 5V$, the comprehensive performance of uncooled focal plane array is best.

### 3.2. DC bias circuit

Through the above analysis, the low noise bias voltage is the basic condition for the detector to work well. It determines the quality of the detector's output signal. The DC bias voltage requirements of UL04371-042 are shown in Table 1. DC bias voltage has higher requirements for accuracy. Therefore, it is necessary to design a circuit with low noise.

| Electrical function name | Bias type | Optimum value @300K | Maximum current | Maximum RMS noise |
|--------------------------|-----------|----------------------|-----------------|-------------------|
| VBUS                     | Fixed     | $2.8V \pm 25mV$     | $1mA$           | $<100uV$          |
| GSK                      | Fixed     | $2.2V \pm 50mV$     | $1mA$           | $100uV\ (1Hz \sim 10MHz)$ |
| GFID                     | Tunable   | $0V \sim 5V \pm 5mV$ | $1mA$           | $100uV\ (1Hz \sim 10MHz)$ |
| VSK                      | Tunable   | $2.0 \sim 5.5V \pm 5mV$ | $5mA$           | $100uV\ (1Hz \sim 10MHz)$ |

UL04371-042 requires four bias voltages, including VBUS, GSK, GFID, and VSK. VSK and VBUS are fixed voltages, and GFID and GSK are adjustable voltages. VSK provides bias for uncooled focal plane array blind resistors, GSK and GFID control the current of the blind resistor and the sensitive resistor. VBUS is the reference voltage of the inverting terminal of the integrator.

The detector bias voltage circuit performs noise reduction from the following three aspects. Use a low noise chip to control the noise; a filter is used to suppress noise from the source; perform precise board-level design to control noise paths.

The DAC circuit uses a low temperature coefficient and a highly accurate reference voltage source. The maximum temperature coefficient does not exceed 5ppm/℃. Using 12-bit precision DAC. Ability to achieve rail-to-rail output swing, output voltage range up to 5V. The minimum resolution is 1.22mV, which meets the detector's DC bias voltage requirements. The DAC ideal output voltage (VOUT) is:

$$V_{OUT} = 2 \times V_{REFOUT} \times \frac{D}{2^N} \quad (5)$$

$V_{REFOUT}$ is determined by the chip type selected, $V_{REFOUT}=2.5V$; N is the DAC resolution, $N=12$; D is the binary equivalent of the binary code loaded into the DAC register, $D \in [0,4095]$.

The voltage follower uses a high-precision, low-noise, rail-to-rail output operational amplifier. The maximum offset voltage is only $65\mu V$ and the noise is less than $8nV/Hz^{1/2}$.

To reduce the influence of high frequency noise on the DC bias voltage, a second order RC low pass filter is designed after the voltage follower.

The second-order RC low-pass filter transfer function is:

$$H(jw) = \frac{1}{1 - w^2 R^2 C^2 + j3wRC} = |H(jw)| \angle \theta(w) \quad (6)$$

$$|H(jw)| = \frac{1}{\sqrt{(1 - w^2 R^2 C^2)^2 + (3wRC)^2}} \quad (7)$$

$$\theta(w) = -\arctan\left(\frac{3wRC}{1 - w^2 R^2 C^2}\right) \quad (8)$$
is an imaginary unit, \( \sqrt{-1} = \pm j \).

Set the passband cutoff frequency to \( w_p, \ |H(j\omega)| = 1/\sqrt{2} \).

\[
(1 - w^2 R^2 C^2)^2 + 9 w^2 R^2 C^2 = 2
\]  \( (9) \)

From the above formula: \( w_p = 1/2.6721 RC \). This formula shows the relationship between the passband cutoff frequency and R and C. The bandwidth of the filter can be set by adjusting the values of R and C. The DC voltage high frequency noise is required to be as small as possible. Set the low pass filter cutoff frequency to 1 Hz, \( f_p = 1Hz \). \( w_p = 2\pi f_p = 6.28Hz \). \( RC \approx 0.06 \) is calculated.

Circuit parameter selection \( R=6K\Omega, \ C=10\mu F \). High frequency noise above 1 Hz can be effectively filtered out.

The DC bias circuit comprises a DAC, a voltage follower, and a second-order low-pass filter circuit. As shown in Figure 5.

![Figure 5](image)

### 3.3. Timing control circuit

The response output of the detector is affected by the bias voltage, the integration time of the integrating capacitor and the external clock. The integration time of the integrating capacitor and the size of the external clock depend on the precise control of the digital timing signal. The detector external inputs include: main clock signal, integral time signal, reset signal, and serial control signal.

According to the input signal timing requirements, the detector MC has a fixed frequency of 9MHz and a duty cycle of 50%. The detector reset signal must be held high for at least 1 clock cycle to reset the detector. The integrated signal must be at least 15 clock cycles low until the rising edge of the detector reset signal arrives; it can only change the reset signal and the integrated signal when the rising edge of the clock signal comes. The integrated signal must be at least 15 clock cycles high and 640 clock cycles maximum. The integrated signal must be low for at least 2 clock cycles.

The digital timing circuit takes the FPGA chip of Altera company as the core, providing the detector with the main clock signal, integral time signal, reset signal, and serial control signal. Designing a detector timing generator based on the Verilog language on the Quartus II platform, and design the simulation script file. Timing simulation is performed on the Modsim platform. It shows the timing generator output signal in Figure 6.

![Figure 6](image)
3.4. ADC module

The analog voltage signal output by the detector is digitized using an ADC after being signal-conditioned and filtered. Then, it is input to the FPGA system for signal processing and transmission. The selected infrared detector response rate is 4mV/K, and the noise equivalent temperature difference is less than 80mK. The analog voltage dynamic range of the detector output is 1.0V to 4.2V. The detector's analog voltage output frequency is consistent with the detector's MC frequency (9MHz). Therefore, the maximum sampling rate of the selected AD conversion chip should be greater than 9MHz. To meet the performance requirements of the detector, the 14-bit ADC chip AD9240 was selected. The chip has an adjustable analog input range with a maximum input range of 0 to 5V. Its maximum sampling rate is 10MHz, with overflow sign indication, which meets the basic requirements of the detector. In actual use, the accuracy and temperature drift of the reference voltage source inside the chip will affect the AD conversion. Therefore, an external reference voltage source is needed in the design.

Sampling timing uses a single clock to control all conversions inside the chip. It only needs to input the clock signal to complete the sampling, conversion and data output. The sampling of the AD9240 is done on the rising edge of the clock. It takes one sample value per clock cycle. The chip adopts a four-stage pipeline structure. The sampling starts from the rising edge of the first clock, and the data will be output only after the rising edge of the fourth clock arrives. As shown in Figure 7. This sampling method can achieve higher resolution, but the data output is delayed by three clock cycles relative to the analog signal sampling. Pay attention to this problem in data processing and timing control.

![Figure 7. AD9240 timing diagram.](image)

4. Experimental results

At ambient temperature, the imaging circuit is externally supplied by a 12V DC power. The voltage values of the two adjustable bias voltages are set to 2.5V and 4.14V. All bias voltages were tested using a 6-digit half-meter (DM3068) manufactured by RIGOL. It shows the test results in Table 2. The RMS noise analysis of the bias voltage is shown in Figure 8.

| Bias voltage | Optimum value | Actual measured value | Voltage accuracy |
|--------------|---------------|-----------------------|-----------------|
| VDDA         | 5.0V          | 4.98298V              | 99.659%         |
| VDDL         | 3.3V          | 3.29901V              | 99.97%          |
| VBUS         | 2.8V          | 2.79197V              | 99.713%         |
| GSK          | 2.2V          | 2.19923V              | 99.965%         |
| GFID         | 2.5V          | 2.48021V              | 99.208%         |
| VSK          | 4.14V         | 4.13927V              | 99.982%         |
According to the analysis of the experimental results, the accuracy of the bias voltage is greater than 98%, and the RMS noise of bias voltage below 1kHz is only 1.4uV. The experimental results meet the requirements of the detector for the bias voltage.

The signal output from the timing control module is tested by the embedded logic analyzer (signal tap II) of Quartus II. The experimental results are shown in the figure below.

In Figure 9, the reset signal changes to a high level at the rising edge of the master clock signal and lasts for two master clock cycles. In Figure 10, the integral signal becomes a high level on the rising edge of the main clock. In Figure 11, both pulse signals of the configuration signal change at the rising edge of the master clock, and the data of the SERDAT signal is in accordance with the requirements given in the detector manual.

5. Conclusion

A low-noise imaging circuit is designed for uncooled infrared detectors. The imaging quality of the detector is related to the bias voltage of the focal plane, timing control and acquisition circuits. The imaging circuit uses DAC, voltage follower and low-pass filter to provide accurate bias voltage for the detector. FPGA is selected to generate the driving sequence of focal plane. High performance and low noise ADC is used to digitize the analog output of the detector. Based on the above circuit, the readout
circuit of the detector is designed. In the bias voltage and signal acquisition circuit, a lot of methods are adopted to reduce the noise, and the signal-to-noise ratio of the output signal is greatly improved. The experimental results show that the designed bias voltage circuit fully meets the requirements of the detector. Compared with the previous acquisition circuit, the bias voltage adjustable function is added to get the most suitable voltage. The RMS noise of bias voltage below 1kHz is only 1.4uV, and the voltage accuracy is greater than 98%.

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