Auto Gain Control Technique Realizing Wide-Range and Precise A/D Conversion for Dynamic Signal Sensing

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Abstract: There is a trade-off between resolution and acquisition range of voltage while performance of feedback control depends on the resolution. Many signals in motion control change quickly with various range and hence both of saturation avoidance and high-resolution data-acquisition are one of the challenges. This research proposes a multi-amplification technique which provides a wide-range and high-resolution A/D conversion. A high-frequency-operated circuit and a fast processor on an FPGA are developed and then a signal-processing module is designed. Experimental results show the validity of the module.

Key Words: measurement, auto gain control, systems and information, system integration, industrial applications.

1. Introduction

Sensor systems are widely applied into social and industrial field and play a lot of roles such as monitoring, and fault-detection. In recent times, data-based control, which utilizes stored data, has attracted a lot of attention combined with machine learning techniques. As wide spread and rapid development of an internet technology has led to the change of industrial and system management structures, sensing process will play a lot of significant roles. Such sensing-then-sharing process is a part of a framework such as Industry 4.0, and further demands for the sensor systems will appear along with this rapidly-evolving framework [1], [2].

The sensor system is one of the most important components for a feedback control system because control performance depends on the performance of sensing. Concretely, the bandwidth of feedback control, the precision of the control, and the adaptability to an external environment are determined by the sensing performance [3], [4]. The bandwidth is important index since a feedback controller easily destabilized by a phase-lag in a control loop [5], and hence human interfaces which require wideband control should have a fast sensing unit [6]. On the contrary, the precision is also important to construct the feedback controller. There are many cases when a controller requires a differential value of a sensor output and hence noise reduction is also important. Therefore, the performance of an analog/digital (A/D) converter (ADC) is remarkably important in control design. Here, many attentions should be paid for appropriate utilization of such devices. Figure 1 shows outputs of amplifiers having different gains when inputted a sinusoidal wave of 1 kHz. Because a small signal input into the ADC is easily affected by quantization noise, thermal drift and fluctuation of reference voltage of the ADC is a serious problem even if a circuit has a high performance ADC like delta-sigma type. On the other hand, a large signal may include overrange of the ADC. Saturation at data-acquisition leads to destabilization of the feedback control and hence should be avoided. Hence, there is a trade-off between the spatial-resolution and safety. Moreover, we also could find a trade-off between time-resolution and spatial-resolution, i.e., high-precision ADCs tend to spend long time while high-speed ADCs have low-precision [7]. However, only few researches to overcome these trade-offs are reported. Under such a situation, a demand for feedback control in precise measuring is emerging, and high-speed and high-precision sensing is strongly required in electronics industry field and precise measuring or motion control field, which handle both AC and DC signals. Although delta-sigma ADCs or dual-slope ADCs are classical powerful tools, it is difficult to meet emerging demands because these have slow sampling rate in principle. Similarly, a time-interleaved type ADC [8], which has the good time resolution, has been widely studied but it can not address the saturation effect and requires conservative design. While the subranging type ADC [9], which has good spatial resolution, improves the resolution of data acquisition and enables to use wide range input, its design is difficult because the performance of first-stage ADC and DAC determine the basic performance of this technique. It is difficult to improve an effective number of bits of the ADC and the DAC due to the noise from other instruments. To elicit high performance, it takes a lot of cost for ICs and effort for substrate wiring. Also, high-speed operating wideband delta-sigma ADCs are emerging and acquiring a high-resolution. However, they should be driven

![Fig. 1 Outputs of parallely-operated amplifiers.](image-url)
by very fast signals and require a designated ADC driver and refined board-wiring. Then, introducing them is practically difficult because it takes large cost for parts and board design. It is important for the improvement of versatility to design a board with cheap ICs with simple board design. To overcome this problem, a system which combines a fast successive approximation (SAR) ADC and a programmable gain amplifier (PGA) has been proposed in [10]. Although there are many filtering approaches, the fundamental filtering performance depends on the amount of noise, as can be seen in a Riccati equation of a Kalman filtering problem [11], [12]. Thus, the hardware approach can be a good solution. That system has an automatic gain controller (AGC), which includes a linear predictor and a hysteresis band for the gain switching condition, and shows a good result in terms of the dynamic-range. However, there are problems in terms of an implementation difficulty and the adaptability against environment. This research has concluded that the performance of the system depends on an algorithm of gain switching and switching conditions. The paper tackles to expand this AGC system to handle a wide-band signal.

Then, this paper designs an AGC system handling a steep signal while reducing implementation cost. Since the conventional method utilized a linear prediction and a simple hysteresis comparator to control the amplifier gain, it is not good to handle a high-frequency signal. As pillars of the proposed module, design methods of prediction filter design and chopping avoidance modules are described. Remarkable advantages are that the design process is quantitative and the characteristics of the designed filters are easily confirmed. These advantages provide a simplicity and an aggressiveness on the design of the switching condition. Then, a specific calculation-circuit is designed on a field-programmable gate array (FPGA) while modifying the calculation process.

A main target is the feedback control or a monitoring system in industry whose sensory system should have high dynamic range. Then, a target bandwidth is almost 500 Hz. The system must take less conversion time than high-resolution ADCs and have lower cost than pipeline ADCs. A concept is to achieve the practicality while saving the cost. Of course, this system also can be applied to many types of ADCs as an auxiliary amplifier. In the experiment, the paper uses an acceleration sensor which is the one of the wideband sensors in industry.

2. System Architecture

This section shows the architecture of the system including an auxiliary circuit and an FPGA. Before explaining the architecture, the paper introduces the problem to be handled. Let us assume the following system

\[ \dot{x} = Ax + Bu + v, \]  

(1)

where \( A, B, x, u, \) and \( v \) stand for the system matrix, the input matrix, the state vector, the input vector and the process noise vector. To observe the state \( x \) with using sensors, the dynamics of amplifiers and ADCs are added into an observation equation as

\[ z = g(x + w_1), \]  

(2)  

\[ y = g^{-1}(z + w_2), \]  

(3)

where \( z, y, g, w_1, \) and \( w_2 \) denote the amplified state-vector, the observed state-vector, the gain vector of the amplifiers, and the observation noises penetrate into the amplifiers and ADCs, respectively. The above equation can be transformed as

\[ y = x + w_1 + g^{-1}w_2. \]  

(4)

Equation (4) denotes that the \( w_2 \) can be reduced by appropriate amplifying while \( w_1 \) uniformly superimposes on the observed state-vector, despite of the amplifier gain. As shown in Fig. 1, \( w_1 \) is smaller than \( w_2 \), and the paper aim to reduces \( w_2 \). In classical design, a fixed-gain amplifier is chosen with considering a maximum amplitude of a sensor output. Hence, a resolution of data acquisition inevitably decreases when a sensor output changes in various range. This problem makes controller design conservative. One of the solution is to embed plural circuits including pre-amplifiers and ADCs. However, this technique requires a large-scale circuit which takes high cost. Further, it has low extensibility as for a settable gain. A multiplexer (MUX) is actually a good tool to reduce the number of parts, but simultaneously switching takes a lot of time for settling. Hence, it does not have enough extensibility and disturbs a data-acquisition in high frequency domain. Then, the paper aims to design a single-path data-acquisition system using the PGA with the AGC system. A function block diagram of the designed system is shown in Fig. 2. Since this structure does not have a channel switching, it shortens a processing time. However, this structure inherently causes a downsampling of the data sampling because the ADC should wait for the end of a calculation process and a settling of the PGA. To suppress the downsampling, the calculation circuit is implemented on an FPGA. A theoretical validity is discussed in Section 4 while discussing both of a contribution of the AGC system and a damage by the downsampling. Main roles of the calculation circuit are (i) to predict an sensor output to avoid an over-ranging and (ii) to abstract the envelop of a high-frequency signal to avoid an excessive switching. A design method of a controller providing these function is shown in Section 3.

3. Controller Design

A fast processing unit is required for this research since both of prediction and gain control should be finished in one period. To realize speeding up of the calculation, the paper implements application-specific arithmetic circuits on the FPGA. A block diagram of the control system is shown in Fig. 3, where \( N \) and \( P \) denote the number of bits of the ADC and the settable gains of the PGA. This AGC system is composed of (1) a prediction filter, (2) a gain controller with a hysteresis comparator with

- **Fig. 2** System architecture.

- **Fig. 3** Block diagram of the control system.
a first-in first-out (FIFO) buffer, and (3) a gain converter with glitch avoidance. (1) The prediction filter works to predict the saturation of the ADC. (2) The gain controller changes the gain of the PGA depending on a situation. (3) The gain converter set the internal conversion gain on the FPGA and the actual gain of the PGA with considering latency from command to the PGA to gain change of the PGA. This can be easily implemented by preparing a delay buffer storing past gains of the PGA. Then, the paper describes the design methods of the prediction filter and the gain controller in this section and confirms the necessity of the gain converter in an experimental section. Although this control structure has feedback loop for gain adaptation, this system does not aim to reduce a noise by oversampling technique like a delta-sigma modulator [13], [14]. In this control system, double precision floating point numbers are adopted to ensure a high dynamic-range in calculation.

3.1 Prediction Filter

The paper designs the prediction filter to avoid the saturation at A/D conversion. Now the first-order approximation filter expressed as

\[ y[k] = \hat{x}[k + n] = x[k] + nT_s \hat{x}[k] \]  

is designed. Here, a superscript \(^\dagger\) represents a predicted value and \(x, y, n, \) and \(T_s \) stand for the acquired state value, the predicted value for saturation avoidance, the step size, and the sampling time, respectively. This filter provides a predicted value after \(n \) steps and is able to be regarded as a decimated prediction filter by the factor \(n \). This factor dictates the degree of phase-lead and hence the capability of the saturation avoidance. Although acquired signal contains noise, \(\hat{x}[k]\) should not be filtered as a filter delays a signal and makes a predictor unable to evaluate quantitatively. Here, the paper shows the advantage of the implemented prediction filter compared with the conventional method [10]. The conventional research uses a linear prediction method. A remarkable advantage is the smallness of the number of calculation. This feature enables fast processing and hence is good at high-frequency signal processing. In addition, the number of prediction step is programmable by setting coefficients of the filter. As discussed above, one-step prediction in the high frequency domain is not useful and ensuring a design freedom is important. Also, the characteristics of the designed filter is easily checked by the Bode plot and can be evaluated quantitatively.

Fig. 4 Bode plot of the prediction filters.

Here, the paper shows the advantage of the implemented prediction filter compared with the conventional method [10]. The conventional research uses a linear prediction method. A remarkable disadvantage of the method is difficulties in design, especially about the decision of the number of regressors and the plant model which is selected while surveying the system in advance. A simple linear-prediction method assumes the system can be modeled as an autoregressive exogenous (ARX) model like

\[ y[k] = B(z)A^{-1}(z)w[k] + A^{-1}(z)\hat{u}[k], \]  

\[ A(z) = 1 + a_1z^{-1} + a_2z^{-2} + \cdots + a_nz^{-n}, \]  

\[ B(z) = b_1z^{-1} + b_2z^{-2} + \cdots + b_mz^{-m}. \]  

Here, \(A, B, u, w, z, a_i, \) and \(b_j (i = 1, \ldots, n, j = 1, \ldots, m)\) are the output regressor, the input regressor, a white noise, the shift operator, and the coefficients of the regressors, respectively. Optimal coefficients of the regressed parameters are obtained by the recursive least squares method (RLS). An algorithm of the RLS is as follows:

\[ E[k] = y[k] - \varphi^T[k]\hat{\theta}, \]  

\[ \hat{\theta}[k] = \hat{\theta}[k - 1] + kE[k], \]  

\[ P[k] = \frac{1}{\lambda} \left( I + k \varphi^T[k] \right) P[k - 1], \]  

where

\[ \hat{\theta} = \begin{bmatrix} -a_1 & \cdots & -a_n & -b_1 & \cdots & -b_m \end{bmatrix}^T, \]  

\[ \varphi = \begin{bmatrix} y & u \end{bmatrix}^T, \]
When noise a
pling time and the number of regressors require pre-tuning.

Persistently excitation by the input should be ensured
precautions related to estimation performance:

covariance matrix, respectively. The RLS method has some
sampling time due to discretization. To see the di
width to be precisely expressed by the model depends on the

sors, pseudo pole-zero cancellation occurs. In addition, band-
it should be designed carefully. If there are redundant regres-
ber of regressions determines the numbers of zeros and poles,
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expression ability is not so high. Non-negligible problems are
(ARARX) model, and the RLS cannot be directly applied.

The ARX model is referred to as an all-pole model and its
expression ability is not so high. Non-negligible problems are
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ber of regressions determines the numbers of zeros and poles,
if there are redundant regres-
sors, pseudo pole-zero cancellation occurs. In addition, band-
width to be precisely expressed by the model depends on the
sampling time due to discretization. To see the difficulty, we
prepare a plant simulator which has two poles and no zero on the
continuous-time domain as follows:

\[ P(s) = \frac{900}{s^2 + 0.03s + 900}. \] (22)

The frequency responses of the identified models are checked
while changing the number of the regressors and the sampling
time. Figures 5 and 6 show system-identification results ob-
tained by injecting an M-sequence which generated by an 18th
order primitive polynomial on the Galois field. Since initial
time-series of the M-sequences are fixed in all simulation, gen-
erality is ensured. The numbers of the output regressors and
input regressors are 2 and 1 or 7 and 1. The sampling time is
set at 10 ms, 1 ms, 100 μs. It should be noted that the resonant
frequencies of the model is varying depending on the sampling
time even if the numbers of zeros and poles are matching be-
tween the simulator and the model. It means that the model
performance depends on the sampling time and the prediction
using the linear prediction requires appropriate decimation of the
time-series. It is difficult to use this system in an unknown
environment because such a setting requires pre-identification.
On the other hand, large phase lags are confirmed when the
numbers of zeros and poles of the simulator and the model are
not matched. The phase lag is almost equal to time delay and
makes prediction difficult. Furthermore, the calculation cost is
high.

Compared with this method, the proposed method easily
compensates the phase-lag by tuning the number of prediction
step. As discussed above, this feature is effective for handling
the high-frequency signal since the one-step prediction in the
high frequency domain is not always useful. Further, the de-
signed filter can be used for any system while the linear predic-
tion is able to be applied only to the AR model. Therefore, the
designed prediction filter is better in terms of generality.

3.2 Gain Controller

The gain controller is designed to adjust the gain of the PGA.
The gain of the PGA is controlled by an external logic signal
and a role of this control block is to output proper logic
signals. Here, as switching operation leads to a slight distor-
tion, excessive switching should be avoided. The conventional
method [10] uses only a hysteresis comparator, but we found
that it leads to a lot of gain changes against high-frequency in-
put. To meet such a condition, a hysteresis and an additional
FIR filter are implemented on this controller; the control logic
signal is updated through the chattering avoidance filter as

\[
L[k + 1] = \begin{cases} 
L[k] + 1'b & \left( x[k - r + 1] < V_{\text{th}} \right), \\
L[k] - 1'b & \left( w[k] > V_{\text{th}} \right), \\
L[k] & \text{(otherwise)},
\end{cases}
\] (23)

\[ w[k] = G_{PGA}[k]y[k]. \] (24)

where \( L \in [0, p] \) (p: the number of the settable gains), \( G_{PGA} \), \( r \), \( w \), and \( x \) stand for the gain address, the gain of the PGA which
is controlled by \( L \), a design parameter of the chattering avoid-
ance filter, a predicted input value into the ADC and amplified
sensor output by the PGA, equal to the input to the ADC. The
number format \( X' \times Y' \) represents \( X \) bit binary of \( Y \). Now, \( L \) is
defined as an increase and a decrease of \( L \) determine the change of
\( G_{PGA} \). This value is converted into a binary code and is transfer
to the PGA as the command determining the gain. The con-
stants \( V_{\text{th}} \) and \( V_{\text{th}} \) are the threshold values for switching condi-
tions including the hysteresis. These design parameters and \( r \)
determine the capability of the saturation avoidance and the
noise reduction at A/D conversion. The chattering avoidance
filter has a role to abstract an envelope for a high frequency
signal and suppresses the number of switching caused by the
steep signal, while not disturbing a switching caused by a gen-
tle signal. To obtain the amplitude of the signal, sampled-data
of half a period is required. Namely, a condition to abstract the envelope of the amplitude is

\[ rT_s > \frac{T_Q}{2}, \tag{25} \]

where \( T_s \) and \( T_Q \) are the sampling period and the period of a signal, respectively. The filter catches an envelope of a high frequency signal satisfying (25) and avoid the switching caused by such a signal. Therefore, \( r \) determines the bandwidth of the gain switching controller, which mainly switches the gain along the in-band signal. The buffer \( w[k] \) is prepared because \( x_c \) has discontinuity due to a variable gain and there is possibility for the prediction filter to oscillate when inputting \( x_c \) to that filter. The chattering avoidance filter prevents excessive gain switching caused by a sudden drop of the input to the ADC. Compared with the case using only the hysteresis band for the switching condition, the additional switching condition simplifies the design of \( V_{th} \) and enables aggressive controller design.

### 3.3 Circuit Design

The calculation circuit is designed on the FPGA to achieve the speed-up of the calculation. Advantages of the FPGA are to embed any arithmetic logic units on a single chip and rigorous timing control of I/O pins at high frequency domain. These features simplify the control design and shorten the sampling time. A time-chart of the control system is shown in Fig. 7. The prediction filter and the chattering avoidance filter can be easily implemented by using state machines and an FIFO buffer to store judgment results of the switching condition. Here, optimization of each block is important since the system has a pipeline process including all blocks. Especially, the calculation process should be modified before implementation of the hardware circuit to eliminate wasteful processing and reduce used logic elements; since a dominant block taking a large time is settling of the PGA, parallel calculations in the prediction filter and the gain controller are not always necessary. The number of embedded arithmetic logic units should be decided considering the sampling frequency of the ADC and the whole process.

### 4. Theoretical Verification

The paper shows validity of the control system. The control system requires downsampling compared with the classical single ADC, but the system has possibility to reduce noise. Now the paper puts the assumption that noise which superimposes on digital data at the A/D conversion is white noise; the noise power is piecewise flat within the Nyquist frequency. The power \( P_f \) of in-band noise which is sampled at interval of \( T_s \) is calculated as

\[ P_f = \int_0^f \Phi(f) \, df, \tag{26} \]

\[ \Phi(f) = P_n/(f_c/2) = 2T_sP_n, \tag{27} \]

where \( f, f_c, \Phi, \) and \( P_n \) denote the bandwidth, the sampling frequency, the power spectrum, and the total amount of noise power which does not depend on the sampling frequency, respectively. When setting the sampling period equal at \( mT_s \), the in-band noise power is calculated as

\[ P_i = \int_0^f m\Phi(f) \, df = mP_f. \tag{28} \]

Here, \( m \) is called the downsampling rate. This result is obtained from Parseval’s equality. It represents the benefit of time-resolution, which remarkably contributes to delta-sigma ADCs. Although the designed control system degrades time-resolution, it enhances spatial-resolution. Since the noise superimposed on the digital data does not depend on the amplitude of an input to the ADC, noise level can be reduced as

\[ P_s = P_n/G_{PGA}^2, \tag{29} \]

\[ \Phi_s(f) = 2mT_sP_s = \frac{m}{G_{PGA}^2} 2T_sP_n, \tag{30} \]

\[ \therefore P_i = \int_0^f \Phi_s(f) \, df = \frac{m}{G_{PGA}^2} P_f. \tag{31} \]

where subscript \( s \) represents the value of the designed system. Here, putting the maximum power of readable signals by the ADC as \( P_m \), the signal-to-noise ratios (SNR) are expressed as

\[ \text{SNR}_s = 10 \log \frac{P_m}{P_i}; \tag{32} \]

\[ \text{SNR}_s = 10 \log \frac{P_m}{P_i} \]

\[ = \text{SNR}_s + 20 \log G_{PGA} - 10 \log m. \tag{34} \]

When the oversampling ratio (OSR) becomes one half, the SNR decreases by \(-3 \text{ dB}\). On the other hand, when the gain of the PGA doubles, it enhances by 6 dB. This equation shows that the designed system has the capability to compensate a downsampling effect or more. In a practical situation, small input is easily affected by thermal or quantization noise and hence ensuring the spatial-resolution is important. As long as a noise caused by the gain switching is small, the AGC provides good performance for the data acquisition.

### 5. Performance Tests

The paper shows an ideal performance of the designed system in a noiseless environment. Here, the gain-switching characteristics and the input to the ADC is checked mainly by focusing on whether exceeding switching and saturation occur or not.

#### 5.1 Setup

The controller is implemented on an FPGA board which mounts a Cyclone III by Altera, device name of EP3C120F780C8N. This board has an external clock of 50 MHz, and the FPGA is driven by this signal. First, the paper checks the operation while generating a wave on the FPGA and regarding it as an imaginary input to an ADC. The wave generator changes the frequency at 100 Hz, 500 Hz, or 2 kHz every 50 ms and the amplitude at 1.5 or 0.75 every 25 ms. The whole data processing is finished in 2 \( \mu \)s and the sampling time \( T_s \) is set at 25 \( \mu \)s. In this time, latency of the gain switching by the PGA is not considered. Design parameters in this evaluation are set as shown in Table 1. Data in the operation are acquired by SignalTap II.
5.2 Results

The obtained data are enumerated in Fig. 8. Here, each figure shows (a) the sensor output, (b) the amplifier gain of the PGA, (c) the amplified sensor output, namely the input to the ADC, and (d), (e), and (f) enlarge the obtained and the predicted sensor outputs focusing on the wave frequency of 2 kHz, 100 Hz and 500 Hz, respectively, while including a gain switching point. In these figures, the figures (a) and (c) denote signals on the analog circuit. The figure (b) shows the output of the gain controller shown in Fig. 3-(2). In the figures (d), (e), and (f), black lines show the output of the gain converter shown in Fig. 3-(3) and the gray dashed-lines show the predicted value output by the predictor shown in Fig. 3-(1). Although spikes can be found in the figure (c), it can be removed by filtering the signal with using the gain converter. Then, the figures (d), (e), and (f) show that the phase lead effect with a little gain amplification is obtained and prediction of the sensor output is correctly conducted. Since the differential operation in the prediction is executed against a converted signal \( x \), which has no discontinuity, the output of the prediction filter does not have intermittent change. As a result, the over-ranging does not occur as shown in the figure (c). The figure (b) shows that the gain switching caused by a high-frequency signal is suppressed. In this design, buffering time of the chattering avoidance filter is \( rT_s = 250 \mu s \), and the filter abstracts the envelope of a signal whose frequency is more than or equal to 2 kHz. The switching caused by the 2 kHz signal is fully stopped and that caused by the 500 kHz signal is fewer than that caused by the 100 Hz signal. On the other hand, the gain controller does not restrict the gain switching for the low-frequency signal. This result indicates that the designed system actively improves the SNR against the low-frequency signal. The figure (c) shows that the sensor output properly amplified regardless of the signal amplitude. Surges caused by the gain switching are found but surges effect can be removed by dividing by \( \frac{G_{PGA}}{k} \). From these results, both of the proper amplification and the over-ranging are achieved while preventing the excessive switching.

6. Experiments

6.1 Setup

The paper shows experiments using the designed AGC system. In this section, fundamental performance is checked with using a function generator (33622A; Keysight Technologies Inc.), and an acceleration excited by a stage-type positioner is measured. The experimental setup is shown in Fig. 9. The stage-type actuator has shaft motors (S200D; GMC Hillstone) and position encoders (RGH24H15A30A; Renishaw). In this time, a reciprocating motion on one axis was performed. The acceleration is sensed by an acceleration sensor (NP-3211; Ono Sokki Technology, Inc.). The sensor output is amplified by the pre-amplifier (SR2210; Ono Sokki Technology, Inc.) and a PGA (AD8253; Analog Devices Inc.), and then it is converted into digital data by an ADC (AD 7980; Analog Devices Inc.). AD8253 has logarithmic gains 1, 10, 100, and 1000. The input range of the ADC was set from \(-5\) to \(5\) V with using the ADC driver (ADA4941; Analog Devices Inc.). Along with this, the

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Table 1: Parameters used in the evaluation.

| Module            | Symbol | Description | Value   |
|-------------------|--------|-------------|---------|
| Prediction filter | \( n \) | Prediction step | 2       |
|                   | \( g_{pd} \) | Cutoff frequency | 1000π   |
| Chattering filter | \( r \) | Buffer size of FIFO | 10      |
| Gain controller   | \( G_{PGA} \) | Gain set | \( 1/2/4/8 \) |
|                   | \( V_{h+} \) | Threshold voltage+ | 4.8     |
|                   | \( V_{h−} \) | Threshold voltage− | 1.5     |
threshold voltages $V_{th^+}$ and $V_{th^-}$ are set at 0.5 V and 4.0 V. In this time, a control period and a sampling period were set to $10 \mu s$. For the verification, the developed system is compared with a system which has a constant gain (without PGA).

6.2 Glitch Avoidance by Delay Compensation

Although delays on wires, noise filters and internal signal on the FPGA are not considered in the simulation, they must be taken into controller design in practical situation. In this system, the gain switching by the PGA and the internal registers on the FPGA which manage the gain command are not synchronized due to the wiring delay and switching delay. Then, such a mismatch makes the system abnormal. Here, the glitch avoidance is presented with using the function generator. A 1 kHz sinusoidal wave with amplitude 40 mV was generated and input to the ADC board. Figure 10 shows results without delay compensation. This figure includes (a) the obtained data and (b) the gain of the PGA. The obtained data has many peaks when excessive switching occurs. This excessive switching is excited by the mismatch of the signals between analog circuit and the FPGA. Concretely, even though the gain switching of the PGA takes little time, the internal signal on the FPGA immediately changes. Then, the conversion (24) operates incorrectly. This causes abnormal operation of the predictor which contains a differentiator and excessive gain switching. Especially, this phenomena excites a two-step gain drop and a large peak due to the limitation of throughput. To avoid this, the internal gain on the FPGA should be delayed by using a buffer. Figure 11 shows results with delay compensation. Owing to the synchronization of the PGA gain and the internal signal, the glitch is eliminated. In addition, the steep change of the gain can not be confirmed. Since the propagation delay of a command signal to the PGA rarely fluctuates, the glitch can be removed once the buffer is adjusted.

6.3 Noise Reduction by Signal Amplifying

Next, noise reduction against small-level signal was confirmed. Here, a 1 kHz sinusoidal wave with amplitude 20 mV was input to the system. The obtained data and the gain of the PGA are shown in Fig. 12. When not using the PGA, voltage drift was confirmed and the wave was distorted. On the other hand, the data acquisition with the PGA did not have voltage drift and there is little distortion. Here, the gain of the PGA was settled to 100 and hence there is safety margin for input satura-
Fig. 13 Power spectra of the results in Fig. 12.

Fig. 16 Power spectra of the results in Fig. 15.

Fig. 14 Position response of the large motion.

Fig. 17 Position response of the small motion.

Fig. 15 Acceleration obtained from the large motion.

Fig. 18 Acceleration obtained from the small motion.

Fig. 19 Power spectra of the results in Fig. 18.

tion. To check the noise reduction performance, power spectra were prepared as shown in Fig. 13. Compared with the fixed gain system, the designed system reduces a noise level $-20\,\text{dB}$ in almost the whole bandwidth, while securing the safety margin against input saturation. These results indicates that the designed AGC system enable to acquire the small-scale signal.

### 6.4 Acceleration Measurement

This section presents acceleration measurement for the stage-type positioner. In this time, the one-axis acceleration excited by the motor and mechanical vibration was measured. In accordance with a practical situation, large motion and small motion were performed. In performing the large motion, the stage moved 11 mm, while it moved 0.5 mm in the small motion. Figure 14 shows the position response of the large motion. The acceleration obtained in this test is shown in Fig. 15 and its $G[k]$ are shown in Fig. 16. These results showed that there is little difference in performing the large motion, because the noise is comparatively small than the measured signal. On the other hand, Fig. 17 shows the position response of the small motion. The acceleration obtained in this test is shown in Fig. 18 and its $G[k]$ are shown in Fig. 19. Without the PGA, a voltage drift was confirmed in the obtained data. On the other hand, the PGA eliminates the voltage drift by setting the high amplifier gain. Moreover, Fig. 19 showed that the designed AGC system decreases noise level in high frequency domain. Because the system measured a dynamic signal, large suppression shown in Fig. 13 was not attained, but suppression of $-6\,\text{dB}$ was achieved. It should be noted that the safety margin of the input voltage is secured as shown in the experiment of the large motion. Considering these experiments, the AGC system can acquire the wide-range data.

### 7. Conclusions

The paper proposed the design method of the AGC which has the very few calculation steps and the capability to avoid the excessive switching caused by a high-frequency signal. To
reduces the calculation process, the first-order approximation filter was introduced. The remarkable advantages of this filter are the ease of implementation and design. This filter is easily adjustable while considering the effects of the aperture and the noise filter. Further, the chattering avoidance filter was imposed on the gain-switching condition. This filter avoids the excessive gain-switching caused by the high-frequency signal while not disturbing a switching against the low-frequency signal. Due to this filter, the AGC system came to be able to handle the steep signal. Although these additional modules can be easily implemented, they simplify the design of the AGC system such as setting of threshold. The proposed AGC system will contributes to the wide-band control system.

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