High Performance Wallace Tree Multiplier Using Majority Gate Based Adders

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Abstract. An area efficient high performance Wallace Tree Multiplier using Majority Gate based Adders is presented in this paper. The proposed Wallace tree multiplier is designed using 9T majority function based full adder. Design is implemented in Cadence Virtuoso® using a 180nm technology library. The design and analysis of the proposed design offers reduced delay of 33.12% while compared to the conventional wallace tree multiplier design using 16T full adder. The design also offers reduced transistor count of 208 which is minimal compared to that of the conventional design.

Keywords—High speed performance, Wallace Tree Multiplier, Full Adder.

1. INTRODUCTION

One of the fundamental building blocks of many VLSI applications are multipliers. To enhance the performance of circuit and system the design of multipliers is very important. Adders are also considered as the major block of many applications, in the proposed design majority gate based adder is used.

A majority gate returns true if and only if more than 50% of its inputs are true[1]. Majority gate adders have the advantage of reducing the power consumption and complexity of the design.

High Speed computation especially in digital signal processing applications demands high speed arithmetic circuits. The recent trends in the VLSI circuit regime paves various methods to achieve the same. It also poses lots of difficulties and challenges in optimizing the architectures with respect to all the performance metrics. The demand for circuits which consume less power with reduced area occupancy and increased operating speed are of greater demand in the real time applications. The design of Wallace Tree multiplier caters to achieve the later two metrics to a greater extent [2]. Furthermore, the design using majority gate based adder in multiplier architecture offers multi-fold advantages.

2. LITERATURE REVIEW

Speed of the processors is mainly determined by the speed of the multipliers used in the processor. Hence, multiplication is one of the most important and fundamental operations in various applications. Various researches had been carried out to obtain high speed, low power consumption and reduced area occupancy in the multiplier architectures. The common multiplication operation is performed using addition and shifting operations. Hence, multiplier design incorporates shifter unit and adder unit as
major sub-unit. This leads to the necessity in having the adder unit also to offer high speed operation with reduced power consumption. When the performance of the adders improves it enhances the performance of the multiplier circuit.

The design of the full adders using majority gate function reduces the number of transistors when analogized with the full adders designed using conventional methods. In addition, the critical path delay is also found to be minimal. The proposed design is a Wallace tree multiplier by using adders realised with 9T(transistor) majority gate function.

2.1. Array Multiplier
In digital and signal processing methods multipliers play a major role. Conventional multipliers include the logic gate like AND and adders such as half adder and full adder. An array multiplier is realized using an array of full adders and half adders. Partial products computation unit incurs major part of the multiplier area. In the case of having N partial products, it requires N-1, M-bit adders. The shifting of the partial products is performed by simple routing and without the requirement of any logic. It reveals the ease in realising a very efficient transistor level schematic design[1].

2.2. Wallace Tree Multiplier
The key design specification for designing a good chip is to make it low power and high speed. Since multipliers and adders are the prime features for any DSP application, designing a low power and high calibre multiplier will highly augment the throughput of the design. Many Research prove that the wallace tree being a high calibre and area efficient multiplier, it can be highly used as an alternative to conventional array multiplier. The Wallace tree is a variant of long multiplication. The multiplication process in wallace tree multiplier involves three steps, The first step is to multiply each bit of the multiplier with the multiplicand. The weights of the wire relies on the multiplied bits position. In the second step the number of partial products is reduced to two by layers of full and half adders and finally, the wires should be grouped into numbers, and add them using Fulladder.

2.3. Design of Full Adder using Majority Function
Full adder circuit is basically 2 half adders connected together. They are used to add three 1 bit binary numbers for example A,B,C. They have 2 output states: sum and carry. Sum performs the xor operation of A,B and C. Carry performs the and operation between the inputs A,B and C. In the proposed full adder Sum is generated by majority gate function which reduces the number of transistors. Majority gate is a function that outputs a HIGH when the majority of the inputs are HIGH, else it outputs a LOW. So by majority gate transistor count gets reduced which results in low switch capacitance reduction and
also it results in working at ultra low supply voltage. Only 2 transistors are needed from Vdd to ground instead of 6 transistors to make it useful in low power design. Majority (minority) network synthesis utilizes majority (minority) gates as logic elements. A majority (minority) function has got three inputs and one output which produces an output value 1 when a majority (minority) of input values are 1. Thus, the majority functions, $M$, corresponding to a majority function is given by

$$M(A, B, C) = AB + BC + CA$$

Sum is calculated with cout compliment

$$SUM = A \oplus B \oplus Cin = Maj(A, B, Cin). (A + B + Cin) + A.B.Cin$$

$$= Cout(A + B + Cin) + ABCin$$

(2)

3. DESIGN AND ANALYSIS

Wallace tree multiplier with 9T full adder design and simulations are performed in Cadence® Virtuoso with 180nm technology library. The circuit design is carried out in the Spectre environment and the simulations are performed in ADEL environment at a temperature of 27°C.

Fig. 2 depicts the design of full adder using majority function. It incurs 9 transistors which is much less than the conventional full adder. Design of the proposed circuit consists of 3 input capacitors, they have been designed using the NMOS transistor available in the 180nm technology by tying the drain and source of the MOSFET.

![Diagram of 9T Full adder design based on majority function](image)

The design of Wallace tree multiplier consisting of full adders and half adders is designed with 3 stages of addition. Table 1 depicts the comparative analysis of the performance metrics with the conventional multiplier unit. The depiction of the delay in Fig. 3, demonstrates the delay incurred by the Wallace tree multiplier using majority function to be 1.05ns, which is 0.52 less than the Wallace tree multiplier with 16T adder.

| Performance metrics | Wallace tree multiplier with 16T full adder [1] | Wallace tree multiplier using 9T majority gate adder [proposed] |
|----------------------|-------------------------------------------------|---------------------------------------------------------------|
| Transistor Count     | 262                                             | 208                                                           |
| Power(μW)            | 136.4                                           | 85.1                                                          |
Fig 3. Comparison of delay in Wallace tree multiplier with 9T adder and 16T adder

4. Conclusion

A 4-bit high calibre Wallace tree multiplier using majority function is designed and implemented. The design and analysis using Cadence® Virtuoso with a 180nm technology library offers a reduced transistor count of 208 and power consumption of 85.1μW. It also demonstrates 33.12% reduction in delay while compared to Wallace tree multiplier with 16T full adder.

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