Toward an Abstract Model of Programmable Data Plane Devices

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Abstract SDN divides the networking landscape into 2 parts: control and data plane. SDN expanded it’s foot mark starting with OpenFlow based highly flexible control plane and rigid data plane. Innovation and improvement in hardware design and development is bringing various new architectures for data plane. Data plane is becoming more programmable then ever before. A common abstract model of data plane is required to develop complex application over these heterogeneous data plane devices. It can also provide insight about performance optimization and bench-marking of programmable data plane devices. Moreover, to understand and utilize data plane’s programmability, a detailed structural analysis and an identifiable matrix to compare different devices are required. In this work, an improved and structured abstract model of the programmable data plane devices is presented and features of its components are discussed in detail. Several commercially available programmable data plane devices are also compared based on those features.

Keywords Programmable data plane · Abstract model · Hardware abstraction layer · P4 · Software Defined Network (SDN)

1 Introduction

From the very beginning, behavior of data plane devices were rigid and ruled by TCP/IP protocol stack. Different efforts [21] for making this rigid environment more programmable haven’t gain momentum until OpenFlow protocol [12] came to the theater. But, with it’s ever growing protocol field set, OpenFlow can not achieve the goal of real programmable network [5]. For true network programmability, data plane hardware architecture should be decoupled from protocol and programmable in nature. Various technologies [25, 23, 31, 22, 24, 10, 11, 9, 12] have been developed to program the run time behavior of a data plane device ‘on the fly’. They are becoming more computationally capable and various complex application layer processing tasks are being pushed to data plane [59, 19, 38]. This is enabling emergence of a new paradigm ‘in-network computation’ [54, 3]. Enabling such cross layer behavior and protocol independence in data plane makes OSI layer based definition of switch (L2, L3, L4 switch etc.) obsolete. This raises the necessity of structured discussion on: how to define programmable switch/data plane device and how to define it’s programmability features? (Through rest of the paper, programmable switch and programmable data plane (PDP) device, these two terms are used interchangeably.)

Programmable switch needs a software stack for programming the data plane. Abstraction layer (Device and resource Abstraction Layer (DAL)) [28] is one of the key component of these stacks. It provides a uniform view of the hardware and a convenient way to develop complex constructs rather than directly dealing with actual hardware instructions. Prominent programmable data plane technologies have heterogeneous hardware internals and corresponding hardware abstraction layer (HAL). They are different from each other (Fig. [1]). But, without a common abstraction layer both data and control plane application become tightly bound to target architecture. For example, a program developed for RMT based architectures can not be executed...
directly over a DPDK based smart-NIC. Lack of common abstraction layer increases cost and complexity of development, testing, performance bench-marking and formal verification of any novel network functionality built over it. Besides this, a well designed hardware abstraction layer (Logical Forwarding Plane [1]) is center piece for successful use of network virtualization, network function virtualization and service chain composition [8]. Though a common abstraction layer over heterogeneous hardware architecture has various advantages, but restricting to a single abstract model of hardware closes the door for future innovation in both hardware and abstraction layer design. PDP programming stacks should be decoupled from hardware architecture and capable of accommodating multiple hardware architectures.

Majority of the data plane programming stacks are tightly coupled with their own abstraction. Whereas, P4 (dominant data plane programming language) decoupled hardware architecture definition from packet processing behavior in it’s latest version (P416 [16]). P416 separates abstract hardware architecture and develop program based on those architectures. Taking advantage of this feature, most of the data plane programming stacks have already developed interface with P4 [11, 62, 60, 71, 74, 56]. Besides this, several other architectures are also being proposed [17, 27, 12, 62, 30]. PSA [27] is one of the most matured among them. But majority of them lacks programmability of two important components: buffer and scheduler. Moreover, these hardware architecture definitions and how they process a packet are described in an informal language. It creates several issues. Most important among them are: 1) identifying clear definition of various components of a hardware architecture become hard 2) boundary between 2 components and how they connect with each other become unclear 3) exact details of how a packet is processed inside a component may differ from one hardware vendor to another 4) developing a formal structure or framework for data plane programs become hard. As consequence of 1) and 2), modular hardware/simulator/test-bed design become hard. As consequence of 3) application layer suffers. For example, if 2 hardware architecture not agree about packet processing states inside the components, taking snapshot of a network or testing/validating a data plane program for multiple architecture become extremely hard. As a result of 4), understanding and comparing various PDP devices and their programmability features become difficult. Moreover without a structural notion, formal analysis of data plane programs become hard. To tackle these challenges, a generalized but flexible yet abstract model of the programmable data plane is necessary. It should be modular in nature with well defined structure of the components. Besides this, well defined interface among the components are necessary for independent development and designing new packet processing architectures based on these components. Moreover, there should be a high level work flow of the components for ensuring uniform behavior across different hardware architectures.

Considering importance of an abstract model and current technology landscape, we think it is important to start discussion on a better model of abstraction layer for programmable switches. In this work, we have attempted to shed light on this topic. In doing so, we make a number of important contributions. After discussing background and related state of the art (in sec. 2), we provided a unified definition of programmable switch (in sec. 3) which is independent of any protocol stack. Then we presented the design of AVS, an example model of Device and resource Abstraction Layer (DAL)/Hardware Abstraction Layer (HAL) for programmable data plane devices (in sec. 4). It is modular in design and components are defined with a uniform and structured functional interface. In discussing details of the components (in sec. 5), at first a generic structure for the components with well defined type of programmability features (Compile Time Programmability (CTP) and Run Time Configurability (RTP)) are laid out. Then a detailed analysis of structure, workflow and programmability features of each components are discussed (in sec. 5.2 - 6.13). To present their workflow in a unambiguous and hardware independent manner, we have followed EFSM approach. After discussing components of AVS in details, a novel approach to compare programmability level of selected set of PDP devices based on programmability features of AVS components are also presented (in sec.
We do not claim the novelty of underlying components design. We are influenced by several existing work on this domain. We believe our achievement is providing a broader picture with an improved and structured abstract model for the programmable switches.

2 Background and Related Works

OpenFlow protocol is the most successful name in SDN paradigm. It is described over an abstract model of switch named ‘OpenFlow Logical Switch’ [25]. OpenFlow decoupled control plane (CP) and data plane (DP). It provides limited programmability in data plane by controlling DP behavior from CP through dynamically configuring a broad set of protocol header fields. Soon academia and industry realized that, with it’s ever growing protocol field set OpenFlow can not achieve the goal of true programmable network. True potential of SDN can be leveraged only if data plane is fully programmable.

After the initial wave of OpenFlow based switches, work on programmable data plane device has gained significant momentum [11, 33]. The first consolidated effort for data-plane programmability can be attributed to RMT [6], which proposed an architecture for programmable data plane devices. Based on RMT’s architecture, an ‘abstract forwarding model’ for data plane devices has been presented in [5]. In this work, authors have also presented a data plane programming language named P4 [5] to write program for RMT based programmable switches. Based on success of RMT and P4, several commercial programmable data plane devices has been emerged in the market [16, 19, 20, 29]. In initial version (version 14) of P4 (P4\textsubscript{14}) [15], data plane programs (DPP) were developed based on ‘abstract forwarding model’ of [5]. P4\textsubscript{14} was strictly coupled with the proposed abstract forwarding model. Although P4\textsubscript{14} came out with an abstract model and related programming construct to program them, it’s high cohesion with proposed hardware with limited programmability made it unsuitable for design of new data plane hardware architectures. This clearly shows the requirement of disaggregation between hardware architecture and programming language for programmable data plane devices.

Currently RMT is the dominant programmable data plane architecture. But it has few limitations. each pipeline stage of RMT architecture can only access memory allocated for it. As a result cross component access of memory/data is also not possible [12]. Moreover, as components of RMT pipeline are connected linearly, a packet can not skip unnecessary stages in the pipeline. To overcome these limitations, authors have proposed dRMT architecture in [12]. It improves RMT architecture by dis-aggregating memory and compute resources inside switch. In [52] authors presented a conceptual model of data plane for supporting parallel processing. It is heavily based on RMT and dRMT architecture. But these works, do not provide concrete hardware abstraction layer.

Efforts for making server based networking environment more programmable have also seen massive growth. DPDK [22] and eBPF/XDP [21] are the two major framework for userspace and in-kernel packet processing. They rely on two abstraction layers: EAL for DPDK and in-kernel virtual machine for eBPF/XDP. Though they are able to work in conjunction with smart-NIC but they are not suitable for core switches. Another important category of programming stack is API based abstraction layer [23, 41]. Instead of providing an abstraction layer they provide an API through which data plane can be programmed. These APIs do not provide any guideline about how to implement a feature. All conforming hardware vendors provide their own implementation of the API. As a result [13] (sec. 1) is not solved by API based solutions. Moreover to interface with data plane programming language (ex. P4), it needs more than one step. At first step, P4 codes are transformed to abstraction layer [23, 41]. At second step, resulting code is transformed to hardware specific instructions. Thus this style abstraction increases complexity.

Among all those data plane programming technologies, P4 and relevant tool-sets emerged as the most dominant programming stack. Nearly all the major programmable data plane platform have a P4 implementation or P4 interfacing [11, 24, 25, 51, 62, 64]. As P4 is becoming more mature, several works [32, 40, 41, 44, 50, 51, 61] focusing on various high level aspects of data plane is rolling out. But, as all of these works depends on P4, they are limited by the abstract forwarding model of P4\textsubscript{14} or few of the present hardware model [17] supported by P4\textsubscript{16}.

Initial version of P4 (P4\textsubscript{14}) was strictly coupled with the proposed ‘abstract forwarding model’ and RMT architecture. But later, P4 community have taken a clean state approach and followed the proven path of virtual machine world. In current version (version 16) of P4 (P4\textsubscript{16}) [16] language constructs for expressing data plane device architecture and hardware specific features are decoupled from the constructs for expressing packet processing logic. Currently in a P4\textsubscript{16} based data plane program, developer needs to define a model of hardware (in form of include file) and the actual packet processing
logic separately. This decoupling gives 4 crucial advantage: a) new hardware architecture can be supported any time b) common hardware architecture or abstraction layer can be created by all relevant stake holders c) top down design of programmable data plane hardware become possible d) high level language constructs for packet processing can be developed independently from hardware design . As a result, P4 can keep the path open for hardware innovation yet promoting interoperability through common hardware architectures. On the other hand P4 enables writing data plane behavior in a flexible and portable manner based on abstraction layers.

P4 community is actively working toward developing a common hardware architecture that can cover various programmable data plane devices ranging from core switches to smart-NIC. PSA [27] is the most matured attempt from P4 community toward that goal. It aims to list several common packet processing paths inside programmable switch and smart-NIC. These paths are composed from multiple programmable P4 blocks. It also lists several related stateful data structure and functions for use in data plane. PSA can be identified as the first structured effort toward a standard abstraction layer of data plane. But PSA specification describes the components and their work flow in a descriptive way. As a result there is always chance of confusion among various implementation of PSA and it suffers from problem 1,2,3 (section 1). Besides, PSA has no option of programmability for buffer and scheduler in the architecture. In this work, we intend to overcome these limitations by proposing a better abstract model (AVS) for programmable data plane devices by extending PSA architecture.

Our approach is aligned with P4 community, as the proposed abstract model (AVS) is inspired by PSA and P4. It also enhances the PSA architecture, firstly by adding programmability to buffer and scheduler components. Secondly, by providing a common functional structure for each components and expressing work flow of each components as hardware architecture agnostic extended finite state machine. These enhancements can help in designing various innovative applications (sec. 8 [33]). Moreover, P4 doesn’t impose any restriction on use of hardware architecture and it has decoupled hardware dependent compiler back end for various architectures. Hence, use of AVS like abstract model doesn’t restrict use of other hardware architectures and the scope of innovation in hardware design remains wide open.

3 Programmable Switch
A packet (PKT)’s life inside a switch starts with reaching through incoming (ingress) port as few bits of data and ends with exiting through outgoing (egress) port.

\[ PKT = \{Bit_1, Bit_2, Bit_3, \ldots, Bit_{\text{Packet Length}}\} \]

How a data plane device acts is defined by

- **S1- Interpreting Packet**: how to interpret incoming set of bits (PKT) as different meaningful fields.
- **S2- Packet Metadata**: a data plane device keeps few hardware dependent information about a packet (metadata) for use in different stages of the packet’s life cycle. Example: arrival time of a packet, this is necessary for packet scheduling.
- **S3- Packet Processing Work-flow**: Set of operations executed based on different fields of packet and various data structures.
- **S4- Control Plane Configuration Parameters**: data plane lacks of global knowledge about the network. Control plane needs to configure parameters so that S3 can be adapted with dynamic network conditions.
- **S5- Emitting Packet**: What’s the structure of the packet emitted by the device.

In legacy switches, S1-S3 & S5 are static. Though S4 is available, they are rather configuring parameters for fixed S3. Hence, in legacy switches, once S1-S5 are loaded, they can’t be changed. These switches are optimized for specific protocol. But in programmable switch, S1-S5 are not static and they can be modified at switch lifetime. Formally, any combination of hardware and/or software is a programmable switch or programmable data plane device, if it fulfills following properties

- **P1**: Not bound to any specific protocol
- **P2**: Can execute any program, which
  - **P2-1**: contains logic and interface for S1-S5
  - **P2-2**: is not coupled to hardware architecture
  - **P2-3**: can be loaded and unloaded at runtime

Any logical abstraction that can provide an uniform view and functionality of a ‘programmable switch’ can be termed as an abstract model of programmable switch.

4 The Abstract Model (AVS)
Processing path of a packet inside a programmable switch can be modeled as an abstract pipeline of serially connected programmable components. Our proposed pipeline based abstract model of programmable switch (**Abstract
**Simple State**: A state representing a stable situation of the workflow.

**Complex State**: A state which refers to an entire State Machine. This sub state machine is shown as separate state machine in next parts.

**Final State**: A special kind of State (not Pseudo State) represents “a workflow has been completed”.

**Trigger**: An event causing transition from one state to another.

**Guard**: A Boolean expression, which enables the trigger when evaluated TRUE.

**Behavior-expression**: An expression specifying what happens when transition occurs.

**Output**: is any kind of data structure or value that is passed as result of trigger action to next state

If any of these 4 is not present for a transition, it is marked as "-".

**Virtual Switch (AVS)** is represented along with other components of SDN stack in Fig. 2 Components (C) of AVS are a) ingress port \( (P_{in}) \) b) ingress parser \( (PR_{in}) \) c) ingress buffer engine \( (BE_{in}) \) d) ingress match action unit \( (MAU_{in}) \) e) ingress deparser \( (DPR_{in}) \)

f) buffer and replication engine \( (BRE) \) g) egress parser \( (PR_{E}) \) h) egress match action unit \( (MAU_{E}) \) i) egress deparser \( (DPR_{E}) \) j) scheduler \( (S) \) k) egress port \( (P_{out}) \).

Based on egress port selection for a packet, the AVS pipeline is logically divided into 2 stages: **ingress stage**- before selecting the egress port and **egress stage**-after selecting egress port. After entering egress stage a packet’s egress port can not be changed. This is particularly important when packets are replicated (clone, broadcast, multicast etc.) in egress stage. On such cases, packets may require further match action processing in egress stage. For example, traffic rate controlling at each outgoing port requires action at egress stage. If egress processing is not required in a hardware implementation, vendors may skip that part.

**AVS** may represent a single non virtualized programmable switch or a slice in a virtualized programmable switch or just a software switch. It is compiler’s duty to map components of AVS to actual hardware resources. AVS provides a uniform view of data plane over heterogeneous programmable switches. How the data plane will behave is defined by data plane program (DPP) (Fig. 2). Management plane handles (un)loading of DPP. On the other hand control plane controls runtime behavior of AVS by configuring parameters.
5 AVS Components

5.1 Generic Structure Of The Components

Each component (C) of AVS represents a programmable unit and they are needed to be programmed from outside before a packet processing starts. These are supplied as DPP. On the other hand CP controls each component’s behavior by configuring parameters through southbound interface. Degree of programmability of AVS and it’s components depend on following 2 kind of features.

- Compile Time Programmability (CTP) Features: Set of instructions a programmable component can execute (comparable to cpu instruction set). How C will behave at run time is defined through these features.

- Run Time Configurability (RTC) Features: Capability of adjusting run-time behavior of CTP features through configuring parameters. Control plane uses these to manage the behavior of a component C.

Irrespective of hardware implementation, CTP and RTC features can be exposed to upper layer as an uniform API. Compiler translates these API call to actual hardware instruction. DPP is a program expressed through CTP features and contains runtime processing logic of a component C. And control plane application controls behavior of those processing logic at run time through RTC features. DPP also contains data structures for facilitating control plane communication with C through RTC features.

Formally, a component (C) can be represented as a component function f_c:

\[ f_c : I \rightarrow O \ni f_c(X, ProcLogic, Conf_{param}) = Y \]  \hspace{1cm} (1)

Here,

- \( I \) is the domain of \( f_c \), it represents the set of all possible values that \( C \) accepts.
- \( O \) is the co-domain (range) of \( f_c \), it represents the set of all possible values that \( C \) can return as output.
- ProcLogic is the processing logic to be executed by the component. It is represented using CTP, RTC and control flow
- \( X \) is the input to the component, \( X \in I \)
- \( Y \) is the output of the component, \( Y \in O \). If \( C \) modifies \( X \) and returns the result as variable of \( X \), \( Y = X \) notation is used. Ex. ingress match action unit (sec. 6.4) take PHV as input and returns result as a modified PHV.
- Conf_{param} is the set of parameters CP can configure to control the behavior of the component at run time. This is a subset of CTP features

5.2 Related Terminology

Before driving into details of each component, few relevant terminologies and notations are discussed in this section.

5.2.1 Bit Space (BS)

Upon receipt a packet (PKT) is a sequence of one and zero.

\[ PKT = \{Bit_1, Bit_2, Bit_3, \ldots, Bit_{Packet\ Length}\} \]

Formally, a packet (PKT) is a point in the space

\[ BS = \{0, 1\}^{Maximum\ Packet\ Length} \]

5.2.2 Header Definition (HDefinition)

To do meaningful operation on a PKT, it is needed to be interpreted as fields of different protocols. Header definition provides structure of these fields. Definition of i’th header field

\[ H_i = (unique\ ID/name, \ starting\ position\ in\ packet, \ length) \]
Fig. 4: Packet’s Life Cycle EFSM

Fig. 5: A sample packet format

Here,

\( 1 \leq i \leq q \) and

\( p = \text{total number of fields in } H_{definition} \)

Starting position of \( H_{j}^i \) provides relative order of the field in packet. All \( H_{j}^i \) together from packet header,

\[
PKT_{header} = \bigcup_{i=1}^{p} H_{j}^i
\]

Rest of the packet is considered as payload.

5.2.3 Packet Metadata (PKT\_Metadata)

Depending on actual hardware implementation, switches maintain some metadata (PKT\_Metadata) about a packet

\( (\text{ingress or egress port, time of arrival, packet unicast or multicast type etc.}) \). \( i \) th metadata field

\[
M_{j}^i = (\text{uniqueID/name, data type/length})
\]

Here,

\( 1 \leq i \leq q \) and

\( q = \text{total number of fields in } PKT_{Metadata} \)

All \( M_{j}^i \) together from packet metadata,

\[
PKT_{Metadata} = \bigcup_{i=1}^{q} M_{j}^i
\]

A sample packet format is shown in Fig. 5 corresponding header definition & a packet metadata are shown in Fig. 5 (a).

5.2.4 Packet Header Vector (PHV) and Space (PHVS)

Header definition and metadata defines a \( p + q \) dimensional space named Packet Header Vector Space (PHVS). Each point in this space is termed as packet header vector (PHV). PHV can be considered as a container for all the attributes of a packet in key-value format. Where, key represents a header field (\( H_{j}^i \)) or metadata field (\( M_{j}^i \)) or any other field derived in the pipeline and value represents corresponding data.

\[
PHV = PKT_{header} \cup PKT_{Metadata}
\]
Header Definition
< Dest MAC, 0, 6 Bytes >
< Source MAC, 6, 6 Bytes >
< VLAN Tag, 12, 2 Bytes >
< Total Length, 14, 3 Bytes >
< Proto Type (IPv4/IPv6), 13, 1 Byte >
< Payload ..........>

Packet Metadata
< Ingress Port, 2 Bytes >
< Egress Port, 2 Bytes >
< Arrival Time, – 8 Bytes >
< Unicast/Manycast Type – 1 Byte >
< Manycast Group ID – 1 Byte >
< Scheduling Order – 2 Bytes >

Fig. 6: (a) Header definition and metadata for the sample packet of Fig. 5(b) Parse graph for sample packet of Fig. 5 (only "Proto Type" node is shown in expanded format)

5.2.5 Ordered PHV Set (PHV \_set, <)

Let PHV \_set is a set of PHV. An ‘Ordered PHV Set’ is an ordered pair (PHV \_set, <) of set PHV \_set and the binary relation < contained in PHV \_set × PHV \_set, such that

- Reflexive: \(\forall PHV \in PHV \_set : PHV < PHV\)
- Transitive: \(\forall PHV_i, PHV_j, PHV_k \in PHV \_set : [(PHV_i < PHV_j) \&\&(PHV_j < PHV_k)] \Rightarrow (PHV_i < PHV_k)\)
- Anti-symmetry: \(\forall PHV_i, PHV_j \in PHV \_set : [(PHV_i < PHV_j) \&\&(PHV_j < PHV_i)] \Rightarrow (PHV_i = PHV_k)\)

Here the relation is defined based on one or more fields of PHV such that, for a field \(x \in PHV\) and 2 elements of the set \(PHV_m, PHV_n \in PHV \_set, (PHV_m.x.value < PHV_n.x.value) \Rightarrow (PHV_m \leq PHV_n)\). If \((PHV_m.x.value = PHV_n.x.value)\) then another filed \(y \in PHV\) can be used to break tie. As packets received from each port have distinct arrival time, and each port has different number in a switch, a total order on a set of PHV is always possible.

6 Analysis of Components

6.1 Ingress Port (Port_in)

In AVS, sole task of an ingress port (Port_in) is to receive a set of bits (PKT) and store as a PHV. How a hardware level frame is received and format of the frame is out of the scope of our discussion. After receiving, a new PHV is initiated and PKT is stored in data_buffer variable of PHV. data_buffer is a storage for an array of bits. In this phase, necessary metadata (ingress port, arrival time etc.) are also stored in the PHV. Then the PHV is passed to next component in pipeline. In AVS, ingress ports do not have any kind of programmability in terms of CTP and RTC features.

\(f_{port_in} : BS \rightarrow PHVS\)
\(f_{port_in}(PKT, Null, Null) = PHV,\)
6.2 Ingress Parser (PR_{In})

PR_{In} parses array of bits stored in PHV.data.buffer to different header fields. Parsing logic is provided through parse graph (G_{p}^{In}). Each node (N') \in G_{p}^{In} contains:

a) Header field information: H_{j}^{f} \in PHV to be parsed, starting position in PKT and length of (L(H_{j}^{f}))

b) Parse table (Table 2) (T(H_{j}^{f})): Lists possible values of H_{j}^{f} and corresponding next node. Work-flow of a programmable parser is shown in Fig. [7] as EFSM. After parsing, PHV is passed to next component in pipeline.

\[ f_{PR_{In}} : BS \rightarrow PHVS \]

\[ f_{PR_{In}}(PHV.data.buffer, G_{p}^{In}, Null) = PHV^{*} \]

**CTP features:**
a) maximum length limit: maximum length of PKT that can be parsed by PR_{In}. This limit is important for bounded runtime.
b) supported data types: different data types (including all the standard primitive data types: int, float, char etc) that can be supported by the parser

c) granularity of field parsing: can the parser circuit parse individual bit or variable number number of bits to a field.

**RTC features:**
a) modifiability of G_{p}^{In}: is the parse graph (G_{p}^{In}) and it’s nodes contents are modifiable at runtime by CP.

6.3 Ingress Buffer Engine (BE_{In})

General role of a buffer is to temporarily hold packets. Though a programmable buffer can be expressed under match-action semantics, but its significance in various important applications warrants a separate component for buffer. Ingress buffer engine (BE_{In}) consists of a set of buffer (B_{set}). Assuming n individual buffers (B_{i}) in the engine, B_{set} = \bigcup_{i=1}^{n} B_{i}. Their size may be fixed or programmable. CP can control these sizes through configuring \textbf{‘Buffer Parameter Table (BPT)’} (Table 3). There are 2 possible positions of BE_{In} in AVS. Any one or both can be used.

First one (BE_{1}^{In}) is just after the Port_{In}. BE_{1}^{In} holds PHV received from ports. CP controls PHV from which ingress port should be stored to which buffer through \textbf{‘Buffer Configuration Table (BCT)’}.

Second one (BE_{2}^{In}) is after ingress parser. This is a more generalized and useful implementation which can store PHV to a buffer based on PHV fields. Here, instead of only ingress port, CP configures based on which header/metadata field, a PHV should be sent to which buffer through \textbf{‘Buffer Configuration Table (BCT)’} (Table 2). Priority for matching PHV’s also can be assigned through BCT.

| VLAN Tag | PHV field Name | PHV field Value | Buffer ID | Priority |
|----------|----------------|-----------------|-----------|----------|
| 0 0 15 25| 0x VLAN Tag    | 00              | 3         | 1        |
| 0 45 25 | 0x VLAN Tag    | 00              | 6         | 0        |

| Buffer ID | Size | RX | TX |
|-----------|------|----|----|
| 1         | 2048 | True | False |
| 5         | 3072 | False | True |

Buffer engine’s work-flow can be expressed as 2 threads: a) \textbf{Receiver Thread (Fig. 8):} for inserting PHV in buffers and b) \textbf{Sender Thread (Fig. 9):} for moving out PHV from buffers and sending to next component in pipeline. These 2 threads behavior are controlled by 2 separate state variable for each of the buffer (B_{i} \in B_{set}). These are configurable from control plane via \textbf{‘Buffer Parameter Table (BPT)’}.

Receiver thread of buffer engine can be expressed as

\[ f_{BE_{receiver}} : PHVS \rightarrow B_{set} \]

\[ f_{BE_{receiver}}(PHV, Null, \{BPT, BCT\}) = B_{set}; (PHV inserted in B_{set}) \]

and sender thread as (assuming a round-robin order for selecting next buffer from where next PHV will be peeked)

\[ f_{BE_{sender}} : B_{set} \rightarrow PHVS \]

\[ f_{BE_{sender}}(Null, Null, Null) = PHV \]

**CTP features:**
a) buffer size & number controlling: number of buffers and corresponding size are programmable or not b) BCT creation: is BCT fixed or can be declared (size and definition) in compile time c) global access of buffer property: can other components of AVS access buffer properties?

**RTC features:**
a) BPT modifiability: can CP manipulate buffer size through BPT b) BCT modifiability: can CP add, modify or delete entry in BCT table.
6.4 Ingress Match Action Unit (MAU\textsubscript{In})

This component can be considered as the computational unit of a data plane device. What is cpu in a server, match-action unit can be considered as that unit for programmable data plane devices. Increasingly, more complex and generalized processing units (FPGA, CPU, GPU) are being proposed as the main computational unit for PDP devices, but match-action base hardware are still dominating. In this work, we have expressed the generic packet header based computations in match-action semantics. hardware implementations may use CPU/GPU/RMT circuit for implementing the actual logic. But the concept is generalized for the component.

In this component, values of PHV field or any other data derived from them are matched with either a) control plane configured data or b) data collected by data plane itself. Based on matching result different actions are executed. Control plane configured data are kept in a table like data structure. Control plane can store, modify or delete data from these tables at runtime through southbound API. Data plane’s collected(or derived) data can be of 3 types a) stateful information about a flow(meter, register, counter etc.) b) stateless metadata about a packet and c) any constant value supplied at compile time in DPP.

Programmability and performance of a switch mostly depends on the set of actions it allows programmer to use. Actions can be of different types : stateless - only access and modify current PHV fields, stateful - access and update previously stored data about a flow and use them to to update PHV.

Different data plane programming language may represent match action semantics in different syntax. But fundamentally, match-action block requires 4 information, a) name/id of the PHV field which will be matched/compared b) control or data plane supplied value, against which PHV field values are matched or compared c) match/comparison method (exact, ternary, <, >, != etc.) d) one or more action(action block) to execute based on comparison result.

Without losing generality, here we assumed that, storing computational logic for packet processing can be represented as graph. In current literature, generic data structure for storing processing logic information is termed as Match – Action – Table(MAT) \cite{6}. Processing logic for a match-action-unit can be represented as a match-action graph (G\textsubscript{MAU}\textsubscript{In}), where each node(N\textsubscript{i}) represents match-action logic for a specific field in PHV and edges are control flow. Let, a protocol field p\_f \in PHV, it’s value in PHV is p\_f.value and data structure for storing it’s match-action information is MAT\textsubscript{p\_f}. 

| Match Type | Values to be Matched | Action[s] |
|------------|----------------------|-----------|
| Exact      | 4                    | Increase IPv4 counter |
| Exact      | 6                    | Drop Packet |
| ...        | ...                  | ...       |

Table 4: A sample MAT for ‘Proto Type’ field in sample packet of Figure 5.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{buffer_receiver_thread_efsm.png}
\caption{Buffer Receiver Thread EFSM}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{buffer_sender_thread_efsm.png}
\caption{Buffer Sender Thread EFSM}
\end{figure}
\[ MAT_{p,f} = \{ \text{match type} \times \text{values to be matched with } p_f \times \text{action}[s] \} \]. Corresponding \( N^i \) is a tuple \((p_f, MAT_{p,f})\). Result of matching-action processing for each field can be stored in stateful memory in case of stateful operations. Or they can simply update some fields in PHV(ex. updating destination port according to routing table). An example \( MAT \) for ‘Proto Type’ field of sample packet (Figure 9) is presented in Table 4. Let, \( MAT\_SET_{In} = \text{Set of } MAT \text{ for all the nodes}(N^i) \text{ in } G_{In}^{MAU}. \) Formally,

\[
\begin{align*}
& f_{MAU_{In}} : PHVS \rightarrow PHVS \\
& f_{MAU_{In}}(PHV, G_{In}^{MAU}, MAT\_SET_{In}) = PHV^* 
\end{align*}
\]

Work-flow of ingress match action unit(MAU_{In}) is presented in Fig. 10.

**CTP features**: a) data type support in MAT: data types (int, float, bit pattern, string etc.) allowed for lookup in MAT  b) matching type support in MAT: type of look ups (longest prefix match, ternary, exact, range etc.) are supported c) MAT size & number controlling: MAT size are fixed length or their size can be declared in compile time d) availability of stateful action: is it possible to maintain state information about the flows e) availability of stateful data structure: what are the data structures for keeping state information about the flows (register, counter etc.). Custom data structure can be created or not f) state sharing among different components: are the flow states shareable among different components of AVS. g) MAT modifiability from DPP: is the MAT tables modifiable from the data plane program. This is necessary for advanced and faster decision making in data plane 61. h) available action types: what are the different type of actions that can be done on the fields of a PHV.

**RTC features**: a) MAT controlling: can the CP add/ remove/update match-action tables entries b) stateful data access from CP: can the CP read/write stateful data of a flow from/to the DP.

6.5 Ingress Deparser(DPR_{In})

This component deserializes a PHV. All the fields of a PHV may not be necessary for emitting to next component. Some may be dropped or some may be included more than once. Moreover all the header fields declared in PHV may not be valid for all the packets. In deparser definition, it is defined which of the valid header fields will be included in the outgoing packet. Besides the PHV fields, constant data also can be included in the packet. Deparser definition is transformed to a graph\((G_d^{In})\) in compilation stage. In this graph each node represents a field of PHV or any arbitrary data to be emitted. DPR_{In} checks validity of each node and concatenates the field data in data_buffer(a per packet buffer for storing bits). This also inherently defines each fields relative position in the packet to be emitted. After deparsing all the nodes of \(G_d^{In}\), payload is concatenated to the data_buffer. Work-flow of an ingress deparser unit is represented as EFSM in Figure 11.

\[
f_{DPR_{In}} : PHVS \rightarrow PHVS \\
N^{P}^{f} = N^{P}^{f}\_\_Null \\
N^{P} = Null \\
N^{P} = Null \\
\text{MA Processing Completed}
\]

**CTP features**: a) maximum length limit: maximum length of a packet that can be created through the deparser unit b) data type support: data types that can be emitted by the deparser.

**RTC features**: a) \(G_d^{In}\) modifiability: can CP modify \(G_d^{In}\) at run time.

6.6 Buffer and Replication Engine(BRE)

**BRE** is the bridge between ingress and egress stage. It contains buffer for each egress port. These buffers can be just simple FIFO buffer or fully programmable buffer (sec. 6.3). But header/metadata based buffer assignment of programmable buffer (BRE^{2}_{In}, section 6.3) is not needed here, because we assume BRE buffers will be reserved as per port resource. Moreover, adding extra
programmable circuit increases the packet processing delay.

\[ BRE.B_{set} = \bigcup_{i=1}^{n} B_i, n = \text{total number of egress port} \]

For a PHV, egress port selection is done in ingress match action unit. After ingress deparser, the PHV may be destined toward either a single egress port (unicast) or more than one egress port (manycast - multicast, broadcast).

- For unicast port, PHV is simply moved to egress port’s buffer with all of its metadata.
- For manycast port, control plane needs to configure group membership of the ports through ‘Manycast Group Table (MGT)’. BRE will make necessary number of copies of the PHV for each member of the group. Those PHV are placed to buffer of relevant egress ports.

Insertion of PHV to port buffer \((B_p)\) are handled by receiver thread of buffer. Sender thread of buffer removes PHV from port buffer \((B_p)\) and either drops or passes to egress stage. Work-flow of these 2 threads are same as of ingress buffer engine discussed in section 5.2.5.

Formally

\[ f_{BRE} : PHVS \rightarrow PHVS^* \]

\[ f_{BRE}(PHV, Null, MGT) = n \text{ copies of PHV} \]

Here, \(n = \text{total number of egress port in a manycast group. For unicast packets } n = 1.\)

**CTP features:** a) all of the CTP features of \(BE_{in}\) (except \(BCT\))

**RTC features:** a) all of the RTC features of \(BE_{in}\) (except \(BCT\) configuration) b) Manycast group membership table configuration: can CP modify manycast group and their members at runtime.

6.7 Egress Parser (\(PR_E\))

After PHV are removed from \(BRE\), they are sent to egress parser. Structurally it is same as ingress parser. Only difference is, after finishing egress parsing of packet header, instead of sending to a buffer, PHVs are sent to egress match-action unit.

\[ f_{PR_E} : BS \rightarrow PHVS \]

\[ f_{PR_E}(PHV.data_buffer, G_E^E, Null) = PHV^* \]

6.8 Egress Match Action Unit (\(MAU_E\))

Same as ingress match action. Only restriction is, egress port can not be changed in this stage. Formally ,

\[ f_{MAU_E} : PHVS \rightarrow PHVS \]

\[ f_{MAU_E}(PHV, G_E^{MAU}, MAT_\text{SET}_E) = PHV^* \]

6.9 Egress Deparser (\(DPR_E\))

Same as ingress deparser. Only difference is, after egress deparser a PHV is sent to scheduler instead of buffer and replication engine.

\[ f_{DPR_E} : PHVS \rightarrow PHVS \]

\[ f_{DPR_E}(PHV, G_E^d, Null) = PHV^* \]

6.10 Scheduler(S)

After egress processing is complete, a PHV is passed to Scheduler(S) for transmission to next hop. Scheduling defines order and time \([57]\) of a PHV’s transmission. To achieve these goals, PHV is needed to be stored in specified order (according to scheduling algorithm) inside an appropriate scheduler data structure \((SDS)\) (i.e. Queue, collection of queue, tree etc.). Different hardware implementation can use different data structure. From an abstract point of view, \(SDS\) maintains an ordered PHV Set (Section \([5.2.2]\)). From \(SDS\) PHV’s are selected according to scheduling algorithm for transmission at appropriate time. As there is no universal scheduling algorithm \([55]\) to match all kind of...
application goals, there is no common implementation of scheduler unit also.

To create a common and generalized abstract model, 2 abstract interfaces are assumed in conjunction with SDS. Different scheduling algorithm will implement these 2 interfaces differently based on data structures provided by the hardware. CP can adjust behavior of S through configuring scheduling algorithm parameters(Sparam). Example: table for configuring weights of weighted fair queuing algorithm. These 2 abstract interface are following:

- **Insert(PHV)**: Implementation of this interface calculates the relative order of a PHV inside SDS and places it in corresponding position. Let, SchedulingOrder is the metadata field that contains the PHV’s order in SDS. Now assume, PHV_SET’ is a set of PHV ordered by SchedulingOrder (in reality this order may depend in more than one field) stored in SDS.

  \[PHV\_SET' = \{PHV_1, PHV_2, PHV_3, .. \]

  

  Finding a new PHV(PHV_new)'s scheduling order requires computation of PHV_new.SchedulingOrder from following types of data.

  - value in PHV_new’s header fields(Hf) and/or metadata(Mf)
  - stateful information about the flow, computed and stored by switch
  - CP configured parameter such as weight for a weighted fair queuing scheduling

  Insert interface provides a total order (Section 5.2.5) on (PHV_SET, <) based on SchedulingOrder where,

  \[PHV\_SET = PHV\_SET' \cup \{PHV\_new\}\]

  \[(PHV\_SET, <) = \{PHV_1, PHV_2, PHV_p, PHV\_new, PHV_q, ..........., PHV_n\}\]

  Therefore, insert interface can be functionally represented as

  \[f_{insert}: PHVS \rightarrow Ordered PHV Set(SDS, \leq)\]

  \[f_{insert}(PHV, Insert Interface Implementation, S_{param}) = PHV\_SET\]

  Computing PHV_new.SchedulingOrder can be done either in match-action stage and result can be carried to scheduler unit through PHV. Or also can be computed in scheduler unit alone. After that, scheduler will insert the packet at appropriate location in the data structure. In case of storage shortage a low priority packet can be dropped or the packet in consideration itself can be dropped depending on scheduling algorithm.

- **Remove()**: This interface’s implementation picks the next PHV to be transmitted from SDS and decides when the packet will be actually transmitted through Port_egress.

  \[f_{remove}: PHV\_SET \rightarrow PHVS\]

  \[f_{remove}(Null, Remove Interface Implementation, S_{param}) = PHV\]

  **CTP features**: a) custom insert and remove interface: is it possible to provide implementation of these 2 interfaces for custom scheduling algorithm b) custom SDS creation: custom SDS can be created for complex scheduling algorithm or not c) cross component access: can other components in the pipeline access SDS (ex. clear a queue based on certain event detected at match action unit) or it’s properties (occupancy rate, priority etc.).

  **RTC features**: a) insert and remove interface parameter modifiability: can the control plane configure parameters for controlling behavior of insert and remove functions b) SDS property access: can control plane access SDS properties c) S_{param} controlling: can CP control scheduling algorithm parameters at runtime.

6.11 Egress Port (PortE)

After a PHV is selected for emitting, egress port (PortE) transmits the content of PHV.data_buffer. How a hardware level frame is created and transmitted is out of the scope of our discussion. Like ingress ports, egress ports also do not have any kind of programmability in terms of CTP and RTC features.

\[f_{PortE}: PHVS \rightarrow BS\]

\[f_{PortE}(PHV, Null, Null) = PKT,\]

7 Programmability Level Comparison

PDP devices enables complex computation on packets in data plane. But limited memory, limited set of actions and requirement of maintaining line rate makes core switches unsuitable for complex algorithm. On the other hand, smart-NIC based packet processing in slow path (cpu based processing) provides opportunity for more complex computation. But achieving high speed line rate in such environments still remains a big issue. To understand what kind of algorithms can be implemented in data plane with available programmable switches in the current market, we have selected following representative platforms for comparison. FlexPipe[18] is Intel’s Openflow supported programmable
switching platform. It is selected as one of the early generation programmable switch of recent times. Tofino is the most prominent and commercially successful programmable switching chip based on RMT architecture. It is being used by various switch vendors. It’s various features are protected under barefoot non disclosure agreement. For comparison, we have chosen Arista 7170 platform. It is based on Tofino chip and supports P4. Netronome Agilio Cx (with 4000/6000 family NFP) is selected as a smart-NIC based programmable switching platform. It can be programmed using micro-C and P4.

In table 5 we have listed few important types of algorithms, what are their crucial tasks that needs support from programmable switches (not achievable with traditional switches) and whether these tasks are supported by selected set of devices. From table 5 it is clear that, all the devices in the market are not equally programmable. To better understand their programmability level, we have scored those selected platforms in table 6 considering AVS components as base. Besides the selected programmable data plane platforms we have also included PSA. PSA is the most matured switch architecture by P4 community and it is based on Tofino chip and supports P4. Netronome Agilio Cx (with 4000/6000 family NFP) is selected as a smart-NIC based programmable switching platform. It can be programmed using micro-C and P4.

Table 5: Few important algorithms and availability of relevant programmability features

| Application                                      | Required Programmability Features                                                                 | Relevant AVS Component                                                                 | FlexPipe | Arista 7170 | Agilio CX |
|--------------------------------------------------|-------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------|----------|-------------|-----------|
| New protocol; Telemetry;                         | On the fly configuration of packet parsing and de-parsing logic                                | Parser and deparser                                                                  | No       | Yes         | Yes       |
| 5g connectionless communication; Mobility management; | Pausing packets at intermediate switches of a path                                            | Ingress buffer engine (programmable buffer)                                           | No       | Partial     | Yes       |
| Congestion Control; Traffic engineering;         | Programmable packet scheduling                                                                | Scheduler                                                                              | No       | No          | No        |
| Video streaming;                                 | Manycast packet transfer                                                                       | Buffer and replication engine                                                         | Partial  | Partial     | Yes       |
| Traffic monitoring; Flow tracking;               | Flow Identification; Flow statistics;                                                         | Match-action unit with Stateful Data Structure;                                       | Partial  | Yes         | Yes       |

switching platform. It is selected as one of the early generation programmable switch of recent times. Tofino is the most prominent and commercially successful programmable switching chip based on RMT architecture. It is being used by various switch vendors. It’s various features are protected under barefoot non disclosure agreement. For comparison, we have chosen Arista 7170 platform. It is based on Tofino chip and supports P4. Netronome Agilio Cx (with 4000/6000 family NFP) is selected as a smart-NIC based programmable switching platform. It can be programmed using micro-C and P4.

Table 6 gives a 2-dimensional comparison among the selected platforms. Firstly, each component of AVS provides a specific type of programmability in data plane. Comparing any platform on the basis of whether equivalent AVS components exists or not says whether equivalent functionality can be achieved in a platform or not. Secondly, eqn. 1 gives a functional structure for each of the component. Scoring the platforms based on parameters (I, O, ProcLogic and Conf_param) of this equation gives a fine grained view of each platform’s programmability level. Details comparison behind the scoring can be found in our full technical report.

The scoring system is following: I, O and Conf_param represents some abstract data types.

- **NA**: Programmability is not applicable here. Example: for all of the selected platforms, input (I) to ingress parser is a set of bits (PHV.data_buffer). Programmability is not needed for input to an ingress parser.

- **0**: The component is non programmable (ex. T-switch).

- **1**: Selectable from a set of predefined data types. Example: FlexPipe hardware can only parse selected set of L2-L4 header fields.

- **2**: New abstract data type (i.e. struct. class etc.) can be created. Example: in P4 supported devices, packet header definition can be created from struct, enum etc.

FOR ProcLogic:

- **NA**: Programmability is not applicable here. Example: PSA has no provision for ingress buffer engine.

- **0**: Non programmable component. Ex, traditional switch not supports any programmability for match-action units.

- **1**: Only selectable from a set of pre-implemented logic /algorithm. Ex, in Flexpipe logic for match-
### Table 6: Eq. 1 Based Programmability Comparison Matrix

| Component          | Products          | $E_1$ | $E_2$ | $E_3$ | $E_4$ |
|--------------------|-------------------|-------|-------|-------|-------|
| Parser             | FlexPipe          | NA    | 1     | NA    | 1     |
|                    | Arista 7170       | NA    | 2     | NA    | 2     |
|                    | Agilio Cx         | NA    | 2     | NA    | 2     |
|                    | PSA               | NA    | 2     | NA    | 2     |
|                    | T-switch          | NA    | 0     | 0     | 0     |
| Ingress Buffer Engine | FlexPipe        | 1     | 1     | 1     | 1     |
|                    | Arista 7170       | 2     | 2     | 1     | 0     |
|                    | Agilio Cx         | 2     | 2     | 2     | 2     |
|                    | PSA               | NA    | 2     | NA    | NA    |
|                    | T-switch          | 0     | 0     | 0     | 0     |
| Ingress Match Action Unit | FlexPipe    | 1     | 1     | 1     | 1     |
|                     | Arista 7170       | 2     | 2     | 2     | 3     |
|                     | Agilio Cx         | 2     | 2     | 2     | 3     |
|                     | PSA               | 2     | 2     | 2     | 3     |
|                     | T-switch          | 0     | 0     | 0     | 0     |
| Deparser           | FlexPipe          | 1     | 2     | NA    | 1     |
|                    | Arista 7170       | 2     | 2     | NA    | 2     |
|                    | Agilio Cx         | 2     | 2     | NA    | 2     |
|                    | PSA               | 2     | 3     | NA    | 2     |
|                    | T-switch          | 0     | 3     | NA    | 0     |
| Buffer & Replication Engine (BRE) | FlexPipe | 1     | 1     | 1     | 1     |
|                      | Arista 7170       | 2     | 2     | 1     | 0     |
|                      | Agilio Cx         | 2     | 2     | 2     | 2     |
|                      | PSA               | 2     | 2     | 1     | 0     |
|                      | T-switch          | 0     | 0     | 0     | 0     |
| Scheduler          | FlexPipe          | 1     | 1     | 1     | 1     |
|                    | Arista 7170       | 2     | 2     | 1     | 1     |
|                    | Agilio Cx         | 2     | 2     | 2     | 3     |
|                    | PSA               | 2     | 2     | 1     | 1     |
|                    | T-switch          | 0     | 0     | 0     | 0     |

- New algorithms ($ProcLogic$) can be implemented with stateful actions support. Ex. P4 supported switches can perform action and store results in counter or register.

### 8 Motivating Use Cases

Abstraction plays very important role in SDN [28]. Abstractions used in SDN are hierarchical in nature and used in different layers [5]. Hardware abstraction layer is placed over programmable hardware layer and provides a uniform view to other layers (‘Device and resource Abstraction Layer (DAL)’ [28]). As an instance of hardware abstraction layer, AVS hides low level hardware complexity and it can provide a uniform view of hardware layer to both control plane and data plane application. Hence its use cases can be found in every aspect of a truly programmable data plane device. We are mentioning few important use cases here.

#### 8.1 Modular Architecture Design & Development

Modular architecture design is the goal of good design. But majority of programmable data plane architecture in literature are expressed in informal language. This makes modular design harder for 3 major reasons: a) lack of clear description about the role of a component b) lack of clear boundary between 2 components c) how the components connect with each other in pipeline. These shortcomings create bottleneck in independent design and optimization of components. It also brings disadvantages in designing new pipeline based on reuse of those components. A modular abstraction layer can solve these issues.

Consider a PDP architecture, where boundary between **Ingress Buffer Engine** ($BE_{In}$) and **Ingress Match Action Unit** ($MAU_{In}$) is not clear. As both the components have match-action semantics, $BE_{In}$ can be designed as a part of $MAU_{In}$. After header matching, storing in and removing packet from buffer can be designed as one of the actions of $MAU_{In}$. Now, consider a smart-NIC based packet processing architecture, where packets are moved to userspace and processed in CPU and/or GPU. Also assume $MAU_{In}$ is implemented on CPU and GPU. GPUs perform better in parallel and batch processing, where buffering is a per packet processing task not best suitable for GPU. Implementing buffer engine as part of match-action unit using GPU needs costly data transfer to and from memory to GPU. Or for smart-NIC based environments packets are needed to be moved from smartNIC buffer to GPU. This data movement often loses the
GPU performance gain. Hence it is better to implement buffer engine as a separate component. If buffer engine functionality is merged with MAU, optimal hardware performance can not be achieved in this case. In this example, if AVS like abstraction layer is used, data plane application developers can write logic without thinking about underlying CPU and/or GPU based implementation. AVS components to actual hardware mapping is done by the compilers. Thus tasks of BE\textsubscript{In} can be executed on CPU only and MAU\textsubscript{In} can be mapped to CPU and/or GPU depending on performance goal. Moreover, new hardware (ex. specialized chip or FPGA) can be designed and optimized independently for each of the components.

8.2 Virtualization & New Pipeline Design

Equation 1 provides a structured framework for each component. It clearly defines the input, output, packet processing logic and parameters for how to configure run-time behavior of a component through control plane \(\text{Conf}_{\text{param}}\). Communication among the components is only through passing parameters. It removes control dependency among components. This gives several advantages: 

a) AVS gives a hardware independent and portable representation of data plane device which can be used to slicing the hardware layer b) DPPs can be developed based on machine model provided by AVS c) AVS can be used to create a virtual switch (VM like entity) for data plane d) switch hypervisor like entities can execute or migrate same DPP to different hardware architecture.

Consider a smart-NIC based scenario where the datapath is moved to userspace using DPDK. Also assume, the data plane prorgam (DPP) is assigned to do both IPv4/6 packet processing and running an algorithm for accelerating ML algorithms through in network aggregation technique [55, 63]. Aggregation is basically mathematical processing and computationally intensive which can be executed in parallel fashion. Let, IPv4/6 packet processing is expressed as \(\text{MAT}_{\text{IP}}\) and aggregation based packet processing logic is expressed as \(\text{MAT}_{\text{AGG}}\). Now, to make packet aggregation faster, \(\text{MAT}_{\text{AGG}}\) is assigned to be executed on GPU. And IPv4/6 packet processing (\(\text{MAT}_{\text{IP}}\)) tasks are executed on CPU. Also assume, CPU can process IPv4/6 packet in 1 cycle while as GPU can aggregate 10 packets in a single cycle and produce result of aggregation as one packet. As CPU and GPU run in different speed, synchronizing and scheduling the packet processing over them is very important. Without a clear definition and structure of \(\text{MAT}_{\text{IP}}\) and \(\text{MAT}_{\text{AGG}}\), synchronizing packet processing over CPU and GPU is not possible. Moreover based on underlying server capability number of CPU cores may differ and GPUs may not be available at certain time. To handle these kind of scenarios, a VM like entity for data plane is mandatory. AVS can works as a virtual switch for data plane. Moreover, modular representation provided by AVS, can also enable switch hypervisors to assign and synchronize execution of DPP over various types of hardware.

8.3 Testing & Verification

Earlier data plane devices were mainly designed for executing network protocol. But in programmable data plane devices, more and more application layers tasks are pushed toward data plane. These devices can be loaded with new data plane program at any period of their life time. Testing them or validating some property at run time over these programs are very important. Without a common abstraction layer and workflow, testing programs and verifying properties over heterogeneous hardware architecture increases the cost and complexity. To write test cases, a common set of packet processing state among switches are required. Without a common abstraction layer and a common set of packet processing states, how various hardware vendors implements packet processing logic can differ.

Consider client-server scenario of Fig. 12. At a certain time \(H1\) got disconnected from server \(S\) due to \(H1-Sw\) link failure. Detecting the link failure switch \(Sw\) stores all packets directed for \(H1\) in \(B_i\) of ingress buffer engine (section 6.3, Fig. 8). When \(B_i\) becomes full, \(Sw\) sends a notification to controller. Upon receiving this notification, controller initiates migration of the whole network (migration including switch state a packet stored in buffer [35]) from one data center to another. Clearly, this kind of DPP depends on the "\(B_i\) is Full" state of buffer receiver thread (sec. 6.3, Fig. 8). For testing them and ensuring uniform behavior, switch vendor of both the data center need to support ingress buffer engine with common packet processing states. Use of AVS as an abstraction layer provides a common abstract switch over heterogeneous architecture and DPP developer gets a uniform view of the hardware. Moreover AVS expresses behavior of the components through EFSM. Common abstraction of the components and common set of packet processing states of the components can be leveraged together to write portable code and testing them.
8.4 Network Function Modeling

Eq. [1] enables representation of each components of AVS in a uniform and hardware independent manner. Composing \( f_c \) for all the components and concatenating them represents AVS as a transfer function (\( \tau \)) [34]. Compiler translates this functional representation to hardware instruction. Any network function (NF) programmed on AVS can be expressed as \( \tau \), where \( I \), \( O \), \( Conf_{\text{param}} \), \( Proc_{\text{Logic}} \)are different for each NF. Each link of a network transfers a \( PKT \) from one hop to another. Link also can be represented as a function (\( \Gamma \)) of same structure.

\[
\Gamma : BS \rightarrow BS
\]

\[
\Gamma(PKT, Medium Access Logic, Conf_{\text{param}}) = PKT
\]

\( \Gamma \) can be considered as the functional representation of data link layer. Depending on medium, corresponding Medium Access Logic, (i.e. ring/mesh/star networks, CSMA, CSMA/CD etc.) and \( Conf_{\text{param}} \) (i.e. persistent level for CSMA) can be different. Based on these, a \( PKT \)'s transmission and propagation delay can be different. These delays can be derived from time stamp (passed as \( H_f \)) at sender node and receiver node. Again applying \( \tau \) and \( \Gamma \) a whole network topology can be represented as a topology function (\( \psi \)) [33]. These functional representation are based on abstraction layer and they are hardware independent representation with well defined parameters for each component. This kind of representation provides various benefits. Few of them are

- **Network algebra:** Network algebra is an old and deeply studied topics. With rise of programmable data plane device, it is more relevant and applicable for today’s network. Expressing network functions and networks in a functional paradigm allows usage of formal methods of network algebra [2] [34].

- **Network Delay Modeling:** Time-stamping [14] packet in data plane is a strong concept with many usage [15]. But maintaining time-stamp only at entry and exit point of a switch can’t provide deep information about various type of delay. Time-stamp can be maintained at entry (\( time-stamp_{Exit}^{PKT} \)) and exit (\( time-stamp_{Entry}^{PKT} \)) point of each component in packet metadata (\( PKT_{Metadata} \)). Delay inside a component (\( C \)) can be calculated as

\[
D_C = time-stamp_{Exit}^{PKT} - time-stamp_{Entry}^{PKT}
\]

Thus, fine grained information about various delay can be collected. One of the most simple but powerful model of delay is Network Delay. It can be computed as following

\[
\text{Network Delay} = \text{Queueing Delay} + \text{Processing Delay} + \text{(Transmission Delay} + \text{Propagation Delay})
\]

\[
= D_{BE_{In}} + (D_{PR_{In}} + D_{MAU_{In}} + D_{DPR_{In}})
+ D_{BRE} + D_{PR_{Ex}} + D_{MAU_{Ex}} + D_{DPR_{Ex}}
+ D_C) + D_{PR_{In}} + D_{F}
\]

Complex data plane processing with time stamp can be used for further complex measurement of various types of delay categorized by source [7].

9 Conclusion

In this work, we proposed the design of AVS, a modular hardware abstraction layer for programmable data plane devices. We are working on a bmv2 [13] based implementation of AVS. Our work on representing components of abstraction layer for data plane devices with a well defined functional structure and their work flow in EFSM can provide a strong base for optimizing, bench marking and comparing different programmable data plane devices. We invite research community to investigate how to improve this formal structure and develop frameworks for using it. We have also analyzed the programmability features of different components and compared few important products based on them. Deriving formal relation between what set of programmability features can support a specific class of algorithms in data plane can be a promising research direction. Besides this, designing chip directly from abstract model also can be a very promising research scope.

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