Enhancement and Modeling of Drain Current in Negative Capacitance Double Gate TFET

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Abstract
The drain current improvement in a Negative Capacitance Double Gate Tunnel Field Effect Transistor (NC-DG TFET) with the help of Heterojunction (HJ) at the source-channel region is proposed and modeled in this paper. The gate oxide of the proposed TFET is a stacked configuration of high-k over low-k to improve the gate control without any lattice mismatches. Tangent Line Approximation (TLA) method is used here to model the drain current accurately. The model is validated by incorporating two dimensional simulation of DG-HJ TFET with one dimensional Landau-Khalatnikov (LK) equation. The model matches excellently with the device simulation results. The impact of stacked gate oxide topology is also studied in this paper by comparing the characteristics with unstacked gate oxide. Voltage amplification factor \( A_v \), which is an important parameter in NC devices is also analyzed.

Keywords Negative capacitance · Tunnel field effect transistors · Drain current modeling · Double gate structure · Heterojunction · Tangent line approximation

1 Introduction

The advancement in technology node has a strong impact on the performance parameter degradation in CMOS design. Power dissipation, parameter variations, increased fabrication and design cost, wire delays and input output bandwidth issues are some of the challenges that the post-CMOS era is witnessing. Transistor evolution happens to combat the aforementioned shortcomings of scaling.

The notion of steep switching transistors easily removed the Boltzmann limit of Sub-threshold Slope (SS) and attracted the semiconductor industry. Tunnel Field Effect Transistors (TFETs) are the most prominent among the steep switching transistors. Even though the mechanism of band to band tunneling (BTBT) reduces the SS to a great extend, low ON current limits its usage. Various topologies, including double gate structures, dual material structures and low bandgap materials, are introduced to overcome this hindrance. Mamidala et al. [1] provides a comprehensive review of different topologies.

The double gate configuration provides excellent gate control and drain current characteristics. This superior characteristic contributes to the industry’s extensive attention. Heterojunction TFETs are capable of producing a high BTBT rate due to reduced tunneling width induced by the low bandgap material taken as the source material. The smaller tunneling width compared to homojunction [1, 2] increases drain current. High-k dielectric materials outperform low-k materials in scaling scenario due to improved gate capacitance (caused by reduction in effective oxide thickness as well as increased dielectric value) which steers the electrical coupling between the gate and tunnel junctions. In TFETs, the tunneling generation rate has exponential relation with gate capacitance. Thus ON
current rises when low-k dielectric materials are replaced by high-k dielectric materials. Another merit of high-k dielectric engineering is the reduction of SS due to enhanced gate coupling [3]. The stacking of high-k over Silicon introduces defects and lattice mismatches [4]. One of the most promising methods to improve the performance with the help of dielectric engineering is stacking the gate oxide layer with high-k material over low-k material [4].

Negative capacitance-based TFETs [5], which have an NC layer in the baseline transistor gate stack, have recently emerged to enhance drain-current and SS. In NC TFETs, ferroelectric material in its negative capacitance mode [6] amplifies the surface potential and improves the electric field. As a result, band bending will be more which in turn reduces the tunneling width. The reduction in tunneling width increases tunneling probability and improves ON current.

Chwodhury et al. [5] modeled NC TFET for the first time with a vertical DG TFET as the baseline transistor, but the modeling approach is limited to one dimension (1-D). A more accurate NC TFET model for a single gate SOI structure is developed later [7], which neglects the effect of mobile carrier density in the Poisson equation [8] and analyses the device characteristics from OFF state to ON state alone. While the existence of mobile carriers [8] may be ignored in saturation mode, the concentration is greater in linear mode, resulting in de-biasing of the transistor. As a result, the influence of mobile charges must be addressed for high precision.

A non-hysteretic NC-GAA TFET is simulated and modeled by Jiang et al. [9] with an assumption that the channel is fully depleted and mobile charges are absent in sub-threshold regime. H.Xu [10] modeled DG TFET with NC stack incorporating the effects of mobile charges for various ferro-electric materials with varying thickness. The potential profile is accurately demonstrated with the help of non-linear Poisson equation and Landau-Khalatnikov (LK) equation [9]. But the drain current is modeled by the shortest tunneling length approach [1]. However, from the literature, it is evident that this method is not accurate at lower gate voltages where the shortest tunneling length is not too small. So it neglects the band-to-band tunneling generation rate at the source-channel junction for lower gate voltage, \( V_G \). VP Hu et al. [11] proposed NC vertical hetero-junction TFET with gate to source overlap, but it lacks an analytical model.

In this paper, a novel heterojunction NC TFET structure is proposed with dielectric stacking of high-k material over low-k material. Here, the drain current enhancement capability of source-channel heterojunction is utilized to increase the ON current of NC-DG TFET. In order to model drain current accurately, the tangent line approximation (TLA) method [1] is adopted. The model is validated against numerical device simulation, which involves LK equation along with TCAD simulation.

The paper is organized as follows. Section 2 discusses the evolvement of the new device structure and the numerical simulation method. The analytical model development of NC-DG-HJ TFET is described in Section 3, and the model is validated in Section 4.

### 2 Device Structure Development and Numerical Simulation

The NC-DG TFET introduced by H.Xu [10] has superior performance over conventional DG TFET. The drain current as well as SS shows remarkable refinement due to the NC effect. The inclusion of source-channel heterojunction further enhances the ON-current. Figure 1 compares the simulated energy band diagrams for a Ge-Si HJ. The reduced tunneling width for NC-DG-HJ TFET compared to NC-DG TFET results in an increased carrier tunneling rate for the former. Replacing \( \text{SiO}_2 \) with a high-k dielectric material can be a better solution to overcome the scaling imparted issues, but it is not preferred due to the lattice mismatches and defects [12]. Stacking high-k dielectric material above low-k dielectric material overcomes the aforementioned drawbacks of high-k material integration while improving SS and ON current to a larger extent. The increased gate capacitance, which has an exponential dependency with drain current [12], is the reason for the augmented performance. The higher gate controllability and coupling leads to electric field enhancement, and this, in turn, reduces the minimum tunneling length [4]. By incorporating the aforementioned performance

![Fig. 1 Band diagram of NC homojunction and heterojunction DG TFET](image-url)
improvement methods, a novel structure of NC-DG-HJ TFET is proposed.

The cross-sectional view of NC-DG-HJ TFET is shown in Fig. 2. The InAs (Material I) source forms heterojunction with Silicon (Material II) channel. Here, the drain region is also of Si material. The doping concentrations of heavily doped p-type source and n-type drain are \(10^{20}\, \text{cm}^{-3}\), \(5 \times 10^{18}\, \text{cm}^{-3}\) respectively. The lightly doped n-type channel is of length 50nm with a doping concentration of \(10^{16}\, \text{cm}^{-3}\). The thickness of channel (\(t_{ch}\)) and insulator layer (\(t_{ox}\)) are 15nm and 2nm, respectively. The insulator layer is made up of a stacked structure of HfO\(_2\) and SiO\(_2\) with thickness (\(t_{HfO_2}\) and \(t_{SiO_2}\) respectively) 1nm each.

Si:HfO\(_2\), being CMOS compatible is chosen as the ferroelectric material for NC property with a thickness (\(t_{FE}\)) of 5 nm. Even though H. Xu [10] concluded that conventional perovskite ferroelectric materials such as Lead Zirconium Titanate (PZT), Barium Titanate (BTO) and Strontium Bismuth Tantalate (SBT) exhibit enhanced NC properties, they have limited applications. Conventional FE materials have exceptionally high polarization charge density and channel charge density. A thicker insulating layer is necessary to balance the charge density, which results in aspect ratio problems [13].

The unstable nature of NC degrades the accuracy of ferroelectric TCAD models [9, 14]. So the simulation process of Metal-Ferroelectric-Insulator-Semiconductor (MFIS) NC TFET requires LK equation along with TCAD. The MFIS structure can be replaced by Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) structure because of their closely matching properties [9]. Thus using TCAD, the Metal-Insulator-Semiconductor (MIS) structure is simulated, and the effect of the ferroelectric layer is realized using 1-D LK equation. Once the baseline DG-HJ TFET is simulated, the charge density is extracted for different gate voltages to calculate the voltage drop across the FE layer due to the fact that an equal charge is present in the two capacitors connected in series. Using this relation, the charge through the ferroelectric layer is calculated to solve the LK equation. Equation 1 [10, 14] relates the voltage across ferroelectric, \(V_{FE}\) to charge density, \(Q\) at steady-state condition. The parameters \(a_{FE}\) and \(b_{FE}\) are LK parameters which depend on the coercive field, \(E_c\), remanent polarization, \(P_r\) and thickness of the material (\(t_{FE}\)). The parameter values are calculated from Eq. 2.

\[
V_{FE} = a_{FE} Q + b_{FE} Q^3 
\]  
(1)

\[
a_{FE} = -\frac{3\sqrt{3}E_c t_{FE}}{2P_r}, \quad b_{FE} = \frac{3\sqrt{3}E_c t_{FE}}{2P_r^3} 
\]  
(2)

The gate voltage (\(V_G\)) of the NC-DG-HJ TFET can be written in terms of voltage drop across the FE layer (\(V_{FE}\)) and gate voltage of the underlying TFET (\(V_{MIS}\)) as in Eq. 3.

\[
V_G = V_{FE} + V_{MIS} 
\]  
(3)

For a NC material, \(V_{FE}\) is negative and from Eq. 3, it is clear that the voltage input for the underlying TFET is more than that of NC-TFET. This explains the voltage amplification capability of NC based TFET.

3 Model Development

To develop a drain current model, the electric field is first obtained by differentiating the potential distribution. BTBT generation rate (\(G_{btbt}\)) which is an exponential function of
electric field is then calculated from Kane’s model [15]. The drain current is then derived by integrating $G_{bitb}$ over the tunneling region. The integration is performed by tangent line approximation (TLA) method.

3.1 Surface Potential Model

The potential profile modeling approach of H. Xu [10] is used in this paper to model the NC-DG TFET. To improve the accuracy, this analytical model considers the impact of mobile carriers, and it is included in the Poisson equation. In this model, the analysis is limited to the intrinsic body. The most significant differences between homojunction and heterojunction are the source potential $(V_s)$ at the source-channel junction and the effective energy gap. For a homojunction $V_s=-V_T \ln \frac{N_{source}}{n_1}$ and for heterojunction

$$V_s=\frac{(\chi_1-\chi_2)}{q}+(E_{g1}-E_{g2})/2q+V_T \ln \frac{N_{source}}{n_1},$$

where $\chi_1$, $E_{g1}$, $N_{source}$, $n_1$ are the electron affinity, band gap, doping concentration and intrinsic carrier concentration respectively of source material (Material I). $E_{g2}$ is the band gap and $\chi_2$ is the electron affinity of channel material (Material II). $V_T$ is the thermal voltage and $q$ is the elementary charge. The effective tunneling barrier height is less for a heterojunction than a homojunction [16].

The equivalent gate oxide capacitance with insulator stack, $C_{eq}$ can be written as

$$C_{eq} = \frac{\epsilon_{Si}\epsilon_{SiO_2}}{t_{SiO_2}+\frac{\epsilon_{SiO_2}\epsilon_{HfO_2}}{\epsilon_{HfO_2}}}$$

where $\epsilon_{SiO_2}$, $\epsilon_{HfO_2}$ are the dielectric constants of SiO$_2$ and HfO$_2$ respectively. 2-D Poisson equation of channel potential $\psi(x, y)$ is given by

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{q}{\epsilon_{ch}} n_{i2} \exp \left[ \frac{\psi(x, y) - V}{V_T} \right]$$

where $V$ is the quasi-Fermi potential of electron, $n_{i2}$ is the intrinsic carrier concentration of channel and $\epsilon_{ch}$ is the relative permittivity of channel material. The channel potential, $\psi(x, y)$ is expressed as

$$\psi(x, y) = \psi_0(y) + \psi_1(x, y)$$

where, $\psi_0(y)$ is the 1-D component which includes the potential along the channel depth and $\psi_1(x, y)$ is the 2-D component.

The 1-D potential component is the 1-D Poisson equation and is expressed as

$$\frac{\partial^2 \psi_0(y)}{\partial x^2} = \frac{q}{\epsilon_{ch}} n_{i2} \exp \left[ \frac{\psi_0(y) - V}{V_T} \right]$$

Equation 7 can be solved by considering the following boundary conditions along y-direction:

(i) Electric field at the centre of the channel is zero.

$$\frac{\partial \psi_0(y)}{\partial x} \bigg|_{y=0} = 0$$

(ii) Applying Kirchhoff’s Voltage Law (KVL), the applied $V_G$ can be written as the sum of flat band voltage, surface potential, voltage drop across the FE layer and oxide layer.

$$V_G - V_{fb} - \psi_0(t_0) = \frac{\epsilon_{Si}}{C_{eq}} \frac{\partial \psi_0(x, y)}{\partial x} \bigg|_{y=t_0} +\alpha_{FE} \frac{\epsilon_{Si}}{\epsilon_{HfO_2}} \frac{\partial \psi_0(x, y)}{\partial x} \bigg|_{y=t_0}$$

Where $V_{fb}$ is the flat band voltage. Using Eqs. 7 and 8, $\psi_0(y)$ can be written as

$$\psi_0(y) = V + V_t \ln \left( \frac{B^2}{2 \gamma \sec^2(By/t_0)} \right)$$

in which, $\gamma=\frac{q n_{i2}}{(4 \epsilon_{ch} V_T)}$ and $t_0 = \frac{t_{ch}}{2}$. The value of $V=V_{DS}$ throughout the channel except near the source-channel junction. The expression for B is obtained by combining (9) and (10).

$$\left( \frac{1}{C_{eq}} + a_{FE} \right) \frac{2 \epsilon_{ch}}{t_0} V_t \tan(B) + V_t \ln \left( \frac{B^2}{2 \gamma \sec^2(B)} \right) = (V_G - V_{fb} - V)$$

The general solution for $\psi_1(x, y)$ is given by

$$\psi_1(x, y) = (A \exp(\lambda x/t_0) + B \exp(-\lambda x/t_0)) \cos(\lambda y/t_0)$$

The boundary conditions to solve $\psi_1(x, y)$ are given in Eqs. 13–15.

$$\frac{\partial \psi_1(x, y)}{\partial x} \bigg|_{x=0} = \psi_S - \psi_0(y)$$

$$\frac{\partial \psi_1(x, y)}{\partial x} \bigg|_{x=L} = \psi_D - \psi_0(y)$$

$$-\psi_1(x, t_0) = \frac{\epsilon_{Si}}{C_{eq}} \frac{\partial \psi_1(x, y)}{\partial x} \bigg|_{y=t_0} +\alpha_{FE} \frac{\epsilon_{Si}}{\epsilon_{HfO_2}} \frac{\partial \psi_1(x, y)}{\partial x} \bigg|_{y=t_0}$$

in which, $\psi_D = V_{DS} + V_t \ln \left( \frac{N_{drain}}{n_{i2}} \right)$ and $V_s=\frac{(\chi_1-\chi_2)}{q}+(E_{g1}-E_{g2})/2q+V_T \ln \frac{N_{source}}{n_1}$ are the drain and source potential respectively. $N_{drain}$ is the drain doping concentration. $\lambda$ can be solved by combining (12) and (15).

$$\tan \lambda = \frac{C_{eq} t_0}{\epsilon_{Si}(1 + a_{FE} C_{eq})}$$

The parameters A and B are computed using Eqs. 12, 13, 14.

$$A = \frac{(V_D - V_S \exp(-\lambda L/t_0)) \sin(\lambda) - V_1 (1 - \exp(-\lambda L/t_0)))}{(\lambda + 0.5 \sin(2\lambda)) \sinh(\lambda L/t_0)}$$
Where $V_i$ is obtained from Eq. 19.

$$V_i = \lambda \cos(\lambda/2)\psi_0(y)|_{y=0.5t_0}$$  \hspace{1cm} (19)

The partial differentiation of surface potential with respect to $x$ and $y$ yields the corresponding electric fields (lateral electric field and vertical electric field respectively). The overall electric field is measured using Eq. 20 [7].

$$E(x, y) = \sqrt{E_x^2 + E_y^2}$$  \hspace{1cm} (20)

Where, $E_x$ is the lateral electric field and $E_y$ is the vertical electric field. The overall electric field is used to model the drain current.

**3.2 Drain Current Model**

$G_{btbt}$ is obtained from Kane’s model [16] and is written as

$$G_{btbt} = A \left( \frac{E(x, y)}{E_0} \right)^\gamma \exp \left( -\frac{B}{E(x, y)} \right)$$  \hspace{1cm} (21)

where $A$, $B$ are material dependent-bias independent parameters, $\gamma$ is 2 for direct BTBT and 2.5 for indirect BTBT, $E_0$=1V/cm and $E(x,y)$ is derived from Eq. 20. The drain current, ($I_d$) in a TFET is obtained by integrating $G_{btbt}$ over the entire tunneling volume which is expressed as

$$I_d = q t_{si} \int G_{btbt}(x) dx dw$$  \hspace{1cm} (22)

Hence, the rate of total carriers generated due to tunneling gives the drain current. TLA is an accurate method to find drain current [2, 16]. Figure 3 shows the pictorial representation of TLA. TLA method is explained below:

Plot the $G_{btbt}$ versus channel distance curve for the required biases using Eq. 21. Draw tangents ($t_1$, $t_2$, $t_3$) to curve and find areas under the respective tangents ($t_1$ at $T_0$, $t_2$ at the x-intercept of $t_1$, $t_3$ at the x-intercept of $t_2$). The area of overlap between $G_1$-$G_2$ and $G_2$-$G_3$ are given by Eqs. 28 and 29.

$$G_{1d} = \frac{1}{2}(T_{1d} - T_2)^2G'_{btbt}(T_0)$$  \hspace{1cm} (28)

$$G_{2d} = \frac{1}{2}(T_{2d} - T_3)^2G'_{btbt}(T_0 + T_1)$$  \hspace{1cm} (29)
The general expressions for the $n^{th}$ tangent line where $n>1$ are given by

$$T_{n-1} = \frac{G'_{btbt}(T_0 + T_1 + ... + T_{n-2})T_n}{G'_{btbt}(T_0 + T_1 + ... + T_{n-1})}$$  

(30)

$$G_n = \frac{1}{2} T_{n-1} G'_{btbt}(T_0 + T_1 + ... + T_{n-1})$$  

(31)

$$G_{n-1} = \frac{1}{2} (T_{n-1} - T_n) G'_{btbt}(T_0 + T_1 + ... + T_{n-1})$$  

(32)

The total area under $G_{btbt}$ curve gives the final analytical drain current model, $I_d$ and is obtained as

$$I_d = q_t c_h G_{sum} f_{Fermi}$$  

(33)

where $G_{sum} = G_1 + G_2 + ... + G_n - (G_{1d} + G_{2d} + ... + G_{n-1d})$ and $f_{Fermi}$ is a correction term which assures zero drain current at $V_{DS}=0$ and it is given by

$$f_{Fermi} = 1 - 2/(1 + \exp(V_{DS}/\eta V_t))$$  

(34)

Here $\eta$ is an empirical parameter.

### 4 Results and Discussions

The investigations are carried out on an n-channel NC TFET with heterojunction formed by InAs and Silicon [4, 17, 18]. A Stacked combination of HfO$_2$/SiO$_2$ is considered as the gate oxide material. TCAD simulations of the baseline DG-HJ TFET with HfO$_2$/SiO$_2$ stack are performed using Silvaco Atlas. The Non-local tunneling model, which considers the spacial profiles of energy bands is used as the tunneling model instead of the inaccurate local tunneling models [1, 10]. Auger recombination model, Shockley-Read-Hall recombination model and bandgap narrowing model are also used for simulation. The values of $P_r$ and $E_c$ for 5nm thick Si:HfO$_2$ film taken are 10.75 $\mu$C/cm$^2$ and 1.15MV/cm respectively [19–21]. For illustrating the performance improvement of the proposed structure, NC-DG-HJ TFET without gate stacking is also considered. Si:HfO$_2$ is taken as the FE material for NC property.

The numerical simulation of the underlying TFET is carried out with the help of 2-D TCAD. To include the NC effect, LK equation which relates the voltage drop and charge density across the FE layer is used. The charge density extracted from TCAD is substituted in LK equation to derive the voltage drop across FE. The model is validated against numerical device simulations, and it shows excellent matching.

The proposed structure is simulated, and the transfer characteristics in both linear and logarithmic scales are plotted in Fig. 4 for $V_{DS}=1$V. In order to observe the improvement in drain current, results of conventional HJ TFET, homojunction NC-DG TFET and heterojunction NC-DG TFET without dielectric stacking are also included. The conventional HJ TFET chosen for analysis is an InAs-Si DG TFET with SiO$_2$ as gate oxide. The homojunction NC-DG TFET is Silicon based NC-DG TFET with SiO$_2$
as dielectric material and Si:HfO₂ as FE material. The unstacked NC-DG-HJ TFET used for analysis is having the same configuration of the proposed NC TFET except for the gate insulator, which comprises SiO₂ as an insulator. From the literature, it is clear that an HJ TFET shows a better drain current performance than its homojunction counterpart due to increased tunneling rate [2] and this inference is justified in the simulated graphs. The drain current enhancement capability of NC in HJ TFET is depicted in the transfer characteristics shown in Fig. 4. The gate voltage gets amplified due to the presence of the NC layer, and it boosts drain current. The improvement of SS in the proposed structure compared to unstacked counterpart is also observed from Fig. 4. As gate voltage increases, electric field increases rapidly than that of NC-DG-HJ TFET designed without gate oxide stacking. The increased transverse electric field leads to significant reduction in minimum tunneling width and contributes steeper slopes. The superior ON current performance results in an increased $I_{ON}/I_{OFF}$ ratio in the proposed NC TFET, even though the OFF current is slightly higher than other structures under study. The $I_{ON}/I_{OFF}$ ratio for the proposed TFET is $10^9$, which is an excellent feature for a transistor. The $I_{ON}/I_{OFF}$ ratio of homojunction NC-DG TFET and NC-DG-HJ TFET without dielectric stacking are $10^8$ each. Hence the proposed NC TFET, which is a combination of NC-DG-HJ TFET and stacked gate topology, exhibits remarkable improvement in drain current, $I_{ON}/I_{OFF}$ ratio as well as SS.

### 4.1 Potential Model Validation

The surface potential profiles along the channel of NC-DG-HJ TFET for $V_{DS}=1V$ and $V_{G}=0V$, 0.5V, 1V and 1.5V is shown in Fig. 5. The surface potential increases with increasing $V_{G}$ values, and when $V_{G}$ is substantially high, the potential is independent of $V_{G}$ due to the channel pinning property of TFET. The channel pinning is the result of inversion charges in the channel, which shields the gate voltage. The model and simulation results match well across the channel, but there are certain dissimilarities at the tunneling junctions. This deviation is due to the zero voltage drop assumptions at the junctions. Compared to homojunction TFETs, heterojunction TFETs have steeper potential profiles [16]. Due to the negative capacitance effect, the potential distribution is improved further. The presence of LK parameters in NC TFET steers the potential and aids tunneling. The electric field distribution of the proposed TFET along the channel is shown in Fig. 6. Here, the deviation of the model from the simulation is due to the assumption of abrupt junctions.

### 4.2 Current Model Validation

Si and InAs are indirect and direct band-gap materials, respectively and the heterojunction formed between InAs/Si exhibits direct BTBT [22]. The values of A and B in Eq. 8 is calibrated against Silvaco Atlas TCAD. The Triangulation

![Fig. 5](image_url)
method (TLA), a graphical approach, is used for modeling drain current. To model the unstacked NC-DG-HJ TFET, $C_{eq}$ is replaced by $C_{ox}$, which is the gate oxide capacitance for SiO$_2$ based TFET.

The transfer characteristics in linear and logarithmic scales for the proposed NC TFET and NC-DG-HJ TFET without gate oxide stacking is plotted based on the simulation and model in Fig. 7 for $V_{DS}=1$V. The drain current of the proposed NC TFET exhibits an improvement of approximately $10^2$ times that of the unstacked NC TFET. As discussed in Section 1, the higher capacitive coupling due to the presence of gate oxide stacking reduces the tunneling width by enhancing electric field. The drain current in the logarithmic scale shows an increased OFF current in the proposed TFET than NC-DG-HJ TFET without gate stacking. Tunneling width reduction is considered as the primary reason for increased OFF current. Even though the OFF current is slightly higher for the proposed NC TFET, excellent $I_{ON}/I_{OFF}$ ratio is maintained due to the ON current improvement. Moreover,
the proposed NC TFET has an extremely good SS feature than unstacked NC TFET. Hence, the proposed NC TFET can be considered as a promising TFET topology for better performance.

The Triangulation approach or TLA is adopted to model the drain current in the proposed NC TFET and NC-DG-HJ TFET without gate stacking. TLA is a graphical method, and the modeling is explained in Section 3.2. The accuracy of TLA is verified in Fig. 7 by comparing it with the shortest tunneling length method, which is based on average electric field, \( E_t \). \( E_t \) is computed by calculating the shortest tunneling length, \( L_t \), as per (19) [10]. Since mean electric field is considered, this method is less accurate. A notable deviation from the simulated results is seen in the average electric field model due to the exponential dependency of electric field in Eq. 14. \( L_t \) is very high at lower \( V_G \), and it results in the reduction of \( E_t \). The reduced \( E_t \) diminishes the dominance of \( G_{btt} \) at the source-channel tunneling region and degrades the accuracy of this method. However, this model cannot be applied for lower \( V_G \), which is evident from the transfer characteristics. Once \( V_G \) reaches substantially high value so that \( L_t \) becomes less and \( G_{btt} \) will be dominant at the source-channel tunneling junction. Now the model starts to follow simulation results. Thus this model becomes accurate only at higher values of \( V_G \). The inaccuracy involved in this method leads to inefficient SS extraction. The TLA model matches excellently with the simulated results in the entire range of gate voltages.

Figure 8 shows the comparison of output characteristics of proposed NC TFET and its unstacked counterpart for \( V_G=1.2\text{V} \). It also compares the models based on TLA method and shortest tunneling approach. The saturation current is very high for the proposed NC TFET when compared to the unstacked gate oxide configuration. The accuracy of TLA is differentiated with shortest tunneling length method. TLA based drain current model matches very well with the simulation results. Since \( L_t \) remains constant for constant \( V_G \) [23] and the gate voltage chosen for the analysis is high, shortest tunneling length model is also found to be accurate.

### 4.3 Voltage Amplification Factor, \( A_v \)

FE materials coupled with FETs are specially utilized for memory applications in the positive capacitance domain due to the hysteretic nature, whereas the NC domain is used for non-memory applications. In order to achieve non-hysteretic state, the total capacitance of the whole structure must be positive for the entire range of operation [24, 25].

The voltage amplification factor, \( A_v \), experienced due to the NC effect is nothing but the derivative of \( V_{MIS} \) with respect to \( V_G \) [14] and it is given by:

\[
A_v = \frac{|C_{FE}|}{|C_{FE}| - C_{MIS}}
\]

where \( C_{FE}=2a_{FE}+3b_{FE}Q^2 \) and \( C_{MIS}=(C_{si}^{-1} + C_{ox}^{-1})^{-1} \). The graph between \( V_{FE} \) and \( V_G \) obtained from LK equation for homojunction NC-DG TFET, NC-DG-HJ TFET with and without stacking is shown in Fig. 9. The charge density across the underlying TFET is more due to
the increased oxide capacitance in the stacked dielectric structure. According to the LK equation, \( V_{FE} \) will be more for the proposed TFET than other TFET structures because of improved charge density. Hence better amplification and more drain current are obtained for the proposed TFET. The value of \( A_v \) derived from the model for a FE thickness of 5nm is 1.1194. Due to the dependency of thickness on \( C_{FE} \), \( A_v \) can be increased for thicker FE layers. The effect of varying FE layer thickness on \( A_v \) is shown in Fig. 10. As FE layer thickness, \( t_{FE} \) increases, \( a_{FE} \) and \( b_{FE} \) rises and thus the value of \( V_{FE} \) will be more negative, thereby increasing the internal voltage gain. In another perspective, the effective oxide thickness decreases while increasing \( t_{FE} \), as a result of reduction in \( a_{FE} \) (\( b_{FE} \) term is neglected for the calculation of capacitance [5]). Thus total gate capacitance raises. So for better amplification, FE thickness can be increased in such a way that it should not affect the capacitance matching criteria [26] as well as the aspect ratio of gate stack [27].

The relationship between \( A_v \) and sub-threshold slope [7] is given in Eq. 28. This depicts the significance of \( A_v \) in a transistor.

\[
SS_{NCTFET} = \frac{SS_{TFET}}{A_v} \tag{36}
\]

where \( SS_{NCTFET} \) is the SS of the proposed NC TFET and \( SS_{TFET} \) is the SS of the baseline TFET.

InAs/Si is a device which is having SS value greater than 60mV/decade. SS of the baseline TFET and proposed NC-DG TFET are 63.5mV/decade, 56.726mV/decade respectively. From these results, it is evident that the presence of NC can convert InAs/Si heterojunction TFET into a sub-60 mV/decade transistor.

### 5 Conclusion

In this paper, heterojunction at source-channel and high-k/low-k stacked gate insulator layer is introduced to improve the drain current of an NC-DG TFET. Both drain current and SS of the proposed NC-TFET are enhanced than that of homojunction NC TFET. The performance improvement capability of the dielectric stacking is verified here by
comparing the proposed structure with the performance of NC-DG-HJ TFET without gate oxide stacking. The amplification property of NC is used to reduce the SS of NC-HJ TFETs. This paper also presents an accurate drain current model of the proposed structure based on TLA method. The accuracy of the drain current model is compared with the model based on the shortest tunneling length method. The model is validated against the numerical simulation method using 2-D TCAD along with 1-D LK equation. The proposed model shows a perfect match with the device simulation results.

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Author Contributions
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2. Rekha K James: Supervision
3. Jobymol Jacob: Conceptualization, Formal analysis, Validation, Writing – original draft, Writing – review and editing
4. Anju Pradeep: Writing – review and editing

Declarations

Conflict of Interests The authors declare that they have no conflict of interest.

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