Design of a distributed synthetic instrument test equipment based on FPGA

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Abstract. In order to solve the problem that special test equipment can't test multiple or multiple devices at the same time, a distributed synthetic instrument testing device based on FPGA is designed. A synthetic instrument testing unit based on FPGA and a main control unit of synthetic instruments based on ARM are designed. The test equipment group implements the distributed test platform through the way of network sharing. The structure and working process of the distributed synthetic instrument detector are designed. Through the reset circuit of FPGA system, the functions of a single test device to detect multiple devices are realized. The system running test shows that the system runs stably, and the system design is reasonable and feasible.

1. Introduction
The traditional control device dedicated test equipment cannot meet the needs of many different types of control devices at the same time.

In this paper, based on embedded technology and synthetic instrument technology, FPGA, ARM and MCU are used to build multifunctional testing equipment based on synthetic instruments. There are two working modes of test equipment: independent testing mode and group shared testing mode. This flexible way of application has wider application prospects in equipment field repair, testing and teaching.

2. System Composition
The functional requirements of the distributed synthetic instrument test equipment: test two series of 5 types of control equipment; carry out fault diagnosis and fault location for the controlled equipment; carry out simulation operation training for special detection equipment; control equipment fault exclusion training; must be able to evaluate the training process.

The structure of distributed equipment testing and training system is shown in Figure 1. The system is composed of distributed synthetic instrument detector, training and control terminal. The two components of the system are connected through the network. The distributed synthetic instrument detector consists of display control unit, measurement unit and DC/DC module group. The terminal of training and control is made up of computer system and software. The software is composed of information display, control, fault diagnosis and training evaluation module.

3. Design of Measuring Instrument for Distributed Synthetic Instrument
The role of the distributed synthetic instrument tester is to detect the control equipment. It has two
states: independent operation and networking controlled work. When working independently, the performance of the control equipment is detected, the detection results are displayed, the fault is located in the circuit board level. When the network is controlled, all the monitoring points of the control equipment are tested under the control of the training and control terminal, and the test data are transferred to the training and control terminal.

![Diagram of distributed equipment test and training system](image1)

**Figure 1.** Structure diagram of distributed equipment test and training system

The structure of the detector is shown in Figure 2. The display control unit is connected to the measuring unit through SPI, and the control measurement unit performs the control device detection program. The data is processed, the detection results are displayed and the fault location is displayed.

![Diagram of distributed synthetic instrument detector](image2)

**Figure 2.** Structure diagram of a distributed synthetic instrument detector

### 3.1. Display Control Unit

The display control unit is made up of Tiny210 core board, LCD and input device. The core board of Tiny210 is a high-performance Cortex-A8 core board, S5PV210 is used as the main processor, and the main frequency is up to 1GHz. It is equipped with 512M memory and 2GBMLC flash memory, which fully meets the needs of the operation system software for hardware.
The display control software based on Android system is developed by using JAVA language. The software is composed of result display, fault diagnosis and control module. Fault diagnosis and fault location are carried out according to the logical relationship between signal flow and signal between control boards. The control module adopts two formats of communication frames, communicates with measurement units through SPI, and uses CRC check code to check communication errors.

The two communication frame format is shown in Figure 3. The control command frame is made up of start, end WORD, command word, parameter and CRC check code. Command words include measurement, reconfiguration, data transmission, data controlled transmission, stop, termination and reexecution, and data transmission frames are composed of start, end words, data words, and CRC check codes.

![Diagram of communication frame](image)

**Figure 3. Diagram of communication frame**

### 3.2. Measuring Unit

The system is divided into one main control unit and multiple functional units separately according to the test function. The main control unit can control the functional unit by simple command. The advantage of this design is that it reduces the complexity of system design, facilitates debugging and reduces failure rate. Based on this method, the measuring unit is designed.

The measurement unit structure is shown in Figure 2, which is composed of FPGA system, A/D conversion module, signal conditioning channel, excitation signal, interface unit and network module. The signal conditioning channel includes A/D conversion channel selection, analog signal conditioning, conditioning circuit channel selection, digital signal conditioning and channel control module, and the excitation signal module is composed of conditional signal and deviation signal generating module.

FPGA adopts ALTERA's Cyclone IV E FPGA device EP4CE15F17C8N. The measurement unit is programmed by Verilog based hardware description language, and all functional units are built inside FPGA. Among them, SPI, UART, Timer and Memory controller are designed by ALTERA IP.

The process control is the control and dispatching unit of the whole measuring unit, which is realized by the finite state machine. It is mainly responsible for the initialization and control of the external modules, such as SPI, UART and other interfaces.

The scheduling DMA transfers the data of the SPI controller directly to the DSP; controls the DSP to perform the corresponding calculation with the test project; controls the transfer and transmission of the test result data; processes the measured digital signal. Timer produces process control beat of the process. As shown in Figure 4, the finite state machine is divided into 5 states: idle, test, SPI data transmission, Net data transmission and reset wait. The state code is shown in Table 1.

![Finite state machine](image)

**Figure 4. A finite state machine controlled by a flow**

| State | Description |
|-------|-------------|
| 0     | Idle        |
| 1     | Test        |
| 2     | SPI Data Transmission |
| 3     | Net Data Transmission |
| 4     | Reset Wait  |

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|------------|-------------|
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![State code table](image)

**Table 1. State code**
Table 1. Finite state machine state table

| state | description |
|-------|-------------|
| 0     | Idle        |
| 1     | Test        |
| 2     | The test result is transmitted directly through SPI (SPI bus is idle) |
| 3     | The test result is transmitted directly through Net (the terminal can receive data immediately) |
| 4     | The test results are controlled by SPI transmission (SPI bus takes up) |
| 5     | The test results are controlled by Net transmission (the terminal can't receive data immediately) |
| 6     | FPGA system preparation reconfiguration |

The selected FPGA device resources cannot meet the design, and the test function can be divided into two separate designs, which can solve the problem of insufficient resources of FPGA devices. Therefore, the measurement unit set up the FPGA reconstruction circuit, which is composed of a controllable power on reset circuit and two 64M FLASH.

After the control process is rebuilt and waited, the functional series FLASH will be selected. Then the power on reset circuit is reset and the FPGA reconfiguration is completed.

According to the reality of the variety of the measured signals, the measuring unit sets up the A/D conversion module of 2 groups of 8 channels with AD7691 as the conversion core. One is a 4 channel single terminal input converter with ADA4941 as a buffer and the other is a 4 channel differential input converter with AD8597 as a buffer. AD7691 is a 18 bit, charge redistribution and successive approximation ADC of ADI company. The A/D conversion module communicates with the FPGA through the SPI.

Signal conditioning channel is divided into two parts: channel selection and signal conditioning. The control module of signal conditioning channel is a C8051F020 microcontroller based on Silicon Labs, which controls channel selection and signal conditioning. A cross switch network consisting of analog switches, relays and address latches is used to achieve channel selection function. Relay is mainly used for high-power signal and power channel. The signal conditioning function is accomplished by programmable partial voltage network, programmable signal amplifying circuit and shaping circuit. The signal conditioning channel communicates with the FPGA through the UART interface.

The excitation signal module uses the C8051F020 MCU of Silicon Labs as the main controller to control the state and condition signals required by the frequency division, photoelectric isolation and level conversion circuits to produce the measured control equipment, Fang Bo, the step wave datum signal, and control the AD9854 output frequency modulated sine wave signal. AD9854 digital frequency synthesizer is a highly integrated device, using advanced DDS technology, built in two high-speed, high performance orthogonal DAC, together to form a digital programmable I and Q frequency synthesizer. The excitation signal module communicates with the FPGA through the UART interface.

In the main control of signal conditioning channel and excitation signal module, the corresponding control process is designed for each test process. Each control process selects the appropriate channel for the characteristics of the measured signal, the appropriate conditioning process and the setting out of the output are measured to control the various excitation signals required for the work of the equipment. The execution of every control process is only controlled by the control commands sent by FPGA through UART, and no other external conditions are needed. The format of the control command frame is the same as that of the control command in Fig. 3.

The measurement unit communicates with the training and control terminal through the TCP/IP protocol. The data part of the TCP/IP protocol data packet uses the format of the two communication frames, as shown in Figure 3, and the advantage of this is to reduce the difficulty of the process control design. The measurement unit resolves the data part of the TCP/IP protocol packets through the decoder. The network module is the core design of CH395 Ethernet protocol by Nanjing qinheng.
company for the chip stack management.

The measurement state of the measurement unit is shown in Figure 5. The left part is the test state workflow, and the right part is the working process of the single test process. When the flow control is controlled into the test state, the following operations are performed:

1. Test state initialization. The configuration data will be read from the FLASH to the SDRAM, and the configuration data includes the number of processes, the DSP configuration data, and the external modules (channel selection and incentive signal module, etc.).

2. Perform the first test process and test the tested control equipment until the end of the test process.

3. To determine whether the test process is wrong or not, if the error is reported, the wrong error code is parsed and sent to the control device. The status code is set to "0", quit the test state; if there is no error, Continue.

4. If it is the last item of the test process, if not, continue the next test process until all the test processes are completed.

5. Send the inquiry command to the control device to determine whether the data is transmitted directly. If the data is not transmitted directly, the state code is set to "0", and the test state is withdrawn; the direct data transmission is based on the selection of the communication channel based on the type of control equipment.

6. If it is SPI direct data transmission, the state code is set to "2", exit the test state; if not, the state code is set to "3", exit test state; test state end.

The working process of the single test process is as follows:

1. Read the configuration data. The configuration data of this test process is read from SDRAM. The data includes configuration data of A/D chip, channel selection, excitation signal control command data, DSP configuration data (voltage conversion ratio, sampling point number and data processing mode, etc.).

2. Configuration module
   a. According to configuration data, AD7691 is set up through SPI controller, and there is a busy indication mode on single chip and four line.
   b. The control channel is selected through the UART transmission setting channel, and the channel selection controller is controlled.

According to the AC and DC characteristics of the measured signal, the controller selects the appropriate conditioning circuit channel and distributes it to the corresponding analog signal conditioning channel. According to the size of the signal, the programmable logic circuit is set up so that the output signal voltage is the best input voltage of A/D conversion. According to the mode of signal, we control the A/D conversion channel and assign the conditioning signal to the common mode and the differential mode converter.

c. According to the current testing process, we control the excitation signal module to select corresponding channels and generate corresponding excitation signals.

d. The DSP configuration data is written into the DSP work condition register. The working conditions include the number of acquisition points, the range of voltage, the ratio, the processing style (the peak value, the effective value and so on).

3. Determine whether there is a mistake in the process (2). If there is a mistake, report the error and end the test process; if it doesn't go on.

4. Start A/D conversion, starts collecting data, start I/O detection, detect frequency, digital status and so on. Start the DMA to transmit the A/D data directly to DSP. Start DSP, start data processing, and store data processing results in data registers.

5. Waiting for the end of DSP data processing flag, if we wait for timeout, execute the error, finish the test process; if it doesn't continue to execute.

6. The result data in the data register is transferred to the result data area of SDRAM, and the test process is finished.
4. Conclusion
According to the requirement of equipment testing and training, the distributed equipment testing and training system is designed. The design of training and control terminal software is introduced, and the design of the distributed synthetic instrument detector based on ARM and FPGA is introduced in detail. The system adopts distributed design, and realizes the function of multi terminal shared control tester set.

The test instrument is designed by the method of master and slave simple command control and the independent design of functional modules, which reduces the complexity of the system design, is easy to debug and reduces the failure rate. When the control system is tested and operated, the system runs stably and reliably. It is proved that the reasonable design of the system is feasible. Next, we will optimize the whole structure of the system and realize industrialization.

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