Design Automation for Efficient Deep Learning Computing

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Abstract—Efficient deep learning computing requires algorithm and hardware co-design to enable specialization: we usually need to change the algorithm to reduce memory footprint and improve energy efficiency. However, the extra degree of freedom from the algorithm makes the design space much larger: it’s not only about designing the hardware but also about how to tweak the algorithm to best fit the hardware. Human engineers can hardly exhaust the design space by heuristics. It’s labor consuming and sub-optimal. We propose design automation techniques for efficient neural networks. We investigate automatically designing specialized fast models, auto channel pruning, and auto mixed-precision quantization. We demonstrate such learning-based, automated design achieves superior performance and efficiency than rule-based human design. Moreover, we shorten the design cycle by 200× than previous work, so that we can afford to design specialized neural network models for different hardware platforms.

Index Terms—AutoML, Neural Architecture Search, Channel Pruning, Mixed-Precision, Quantization, Specialization, Efficient Deep Learning.

1 INTRODUCTION

Algorithm and hardware co-design plays an important role in efficient deep learning computing. Unlike optimizing on the SPEC2006 benchmark when we can treat the algorithm as a black box, there’s plenty of room at the algorithm level that can improve the hardware efficiency of deep learning. We should open the box and explore model optimization techniques. The benefit usually comes from memory saving and locality improvement. For example, model compression techniques [1] including pruning and quantization can drastically reduce the memory footprint and save energy consumption. Another example is small model design. SqueezeNet [2] and MobileNet [3] have only 4.8MB/4.2MB of model size, which can fit on-chip SRAM and improve the locality.

However, efficient model design and compression have a large design space. Many different neural network architectures can lead to similar accuracy, but drastically different hardware efficiency. This is difficult to exhaust by rule-based heuristics, since there is a shortage of deep learning and hardware experts to hand-tune each model to make it run fast. It’s demanding to systematically study how to design efficient neural network with hardware constraints. We propose hardware-centric AutoML techniques that can automatically design neural networks that are hardware efficient [4, 5, 6]. Such joint optimization is systematic and can transfer well between tasks. It requires fewer engineer efforts while designing better neural networks at low cost.

We explore three aspects of neural network design automation (Figure 1): auto design specialized model, auto channel pruning, and auto mixed-precision quantization. Each aspect is summarized as follows.

There is plenty of specialized hardware for neural networks, but little research has been done for specialized neural network architecture for a given hardware architecture (the reverse specialization). There are several advantages for a specialized model: it can fully utilize the parallelism of the target hardware (e.g. fitting the channel size with the PE size). Besides, a specialized model can fully utilize the on-chip buffer and improve locality and reuse. Specialization can also match the model’s computation intensity with the hardware’s roofline model. However, designing a specialized neural network architecture used to be difficult. First, there are limited heuristics. Second, the computation cost used to be prohibitive: even searching a model on CIFAR-10 dataset takes 10⁴ GPU hours [7, 8]. We cut the search cost by two orders of magnitude (actually more than that, since we directly search on ImageNet). The search cost is reduced by two techniques: path-level pruning and path-level binarization, which saves GPU hours and GPU memory. Cutting the search cost enables us to design specialized the model on the target task and target hardware. On the mobile phone, our searched model [4] runs 1.8× faster than the best human designed model [9].

After designing a specialized model, compression and pruning is an effective technique to further reduce the memory footprint [1]. Conventional model compression techniques rely on hand-crafted heuristics and rule-based policies that require domain experts to explore the large design space. We propose an automated design flow that leverages reinforcement learning to give the best model compression policy. This learning-based compression policy outperforms conventional rule-based compression policy by having a higher compression ratio, better preserving the accuracy and freeing human labor. We applied this automated, push-the-button compression pipeline to MobileNet and achieved 1.81× speedup of measured inference latency on an Android phone and 1.43× speedup on the Titan XP GPU, with only 0.1% loss of ImageNet Top-1 accuracy.
The last step is automatic mixed-precision quantization. Emergent DNN hardware accelerators begin to support flexible bitwidth (1-8 bits), which raises a great challenge to find the optimal bitwidth for each layer: it requires domain experts to explore the vast design space trading off among accuracy, latency, energy, and model size. Conventional quantization algorithm ignores the different hardware architectures and quantizes all the layers in a uniform way. We introduce the automated design flow of model quantization, and we take the hardware accelerator’s feedback in the design loop. Our framework can specialize the quantization policy for different hardware architectures. It can effectively reduce the latency by $1.4-1.95 \times$ and the energy consumption by $1.9 \times$ with negligible loss of accuracy compared with the fixed bitwidth (8 bits) quantization.

2 Automated Model Specialization

In order to fully utilize the hardware resource, we propose to search a specialized CNN architecture for the given hardware. The model is compact and runs fast. We start with a large design space (Figure 1(a)) that includes many candidate paths to learn which is the best one by gradient descent, rather than hand-picking with rule-based heuristics. Instead of just learning the weight parameter, we jointly learn the architecture parameter (shown in red in Figure 1(a)). The architecture parameter is the probability of choosing each path. The search space for each block $i$ consists of many choices:

- **ConvOp**: mobile inverted bottleneck conv [9] with various kernel sizes and expansion ratios
  - Kernel size: $\{3 \times 3, 5 \times 5, 7 \times 7\}$
  - Expansion ratio: $\{3, 6\}$
- **ZeroOp**: if ZeroOp is chosen at $i^{th}$ block, it means the block is skipped.

Therefore, the number of possible architectures in the design space is $\sum_{\text{ConvOp}} \sum_{\text{ZeroOp}} |N| = 7^N$ where $N$ is the number of blocks (21 in our experiments).

Given the vast design space, it is infeasible to rely on domain experts to manually design the CNN model for each hardware platform. So we need to employ automatic architecture design techniques.

However, early reinforcement learning-based [7, 8] NAS methods are very expensive to run (e.g., $10^4$ GPU hours) since they need to iteratively sample an architecture, train it from scratch and update the meta-controller. It typically requires tens of thousands of networks to be trained to find a good neural network architecture.

We adopt a different approach to improve the efficiency of model specialization [4]. We first build a super network that comprises all candidate architectures. Concretely, it has a similar structure to a CNN model in the design space except that each specific operation is replaced with a mixed operation that has $n$ parallel paths. Each path in a mixed operation corresponds to a candidate operation $\alpha_i$, and we introduce an architecture parameter $\alpha_i$ to each path to learn which paths are redundant and thereby can be pruned (i.e. path-level pruning).

In the forward step, to save GPU memory, we allow only one candidate path to actively reside in the GPU memory. This is achieved by hard-thresholding the probability of each candidate path to either 0 or 1 (i.e., path-level binarization). As such the output of a mixed operation is given as:

$$x_i = \sum_i g_i \alpha_i(x_{i-1})$$

(1)

where $g_i$ is sampled according to the multinomial distribution derived from the architecture parameters, i.e.,

$$p_i = \text{softmax}(|\alpha_i|/\sum_i \text{exp}(\alpha_i))$$

In the backward step, we update the weight parameters of active paths using standard gradient descent. Since the architecture parameters are not directly involved in the computational graph (Eq. 1), we use the gradient w.r.t. binary gates to update the corresponding architecture parameters:

$$\frac{\partial L}{\partial \alpha_i} = \sum_{j=1}^N \frac{\partial L}{\partial g_j} \frac{\partial p_j}{\partial \alpha_i} \approx \sum_{j=1}^N \frac{\partial L}{\partial g_j} \frac{\partial p_j}{\partial \alpha_i}$$

In order to specialize the model for hardware, we need to take the latency running on the hardware as a design reward. However, directly measuring the inference latency suffer from (i) slow (ii) high variance due to different battery condition and thermal throttling (iii) latency is non-differentiable and can’t be directly optimized. To address these, we present our latency prediction model and hardware-aware loss.

To build the latency model we pre-compute the latency of each operator with all possible inputs. During search we query the lookup table during the searching process. The overall latency of $i^{th}$ block is the weighted sum of the latency of each operator.
TABLE 1. ImageNet Accuracy (%) and GPU latency (Tesla V100).

| Model                  | Top-1 (%) | Top-5 (%) | GPU Latency (ms) |
|------------------------|-----------|-----------|------------------|
| MobileNet-V2 [9]       | 72.0      | 91.0      | 6.1              |
| ResNet-34 [10]         | 73.3      | 91.4      | 8.0              |
| NASNet-A [8]           | 74.0      | 91.3      | 38.3             |
| MnasNet [11]           | 74.0      | 91.8      | 6.1              |
| Specialized model for GPU | 75.1      | 92.5      | 5.1              |

TABLE 2. Hardware prefers specialized models. Models optimized for GPU does not run fast on CPU and mobile phone, vice versa. Our method provides an efficient solution to search a specialized neural network architecture for a target hardware architecture, while cutting down the search cost by 200× compared with state-of-the-arts [7, 11].

| Model                  | Top-1 (%) | GPU Latency (ms) |
|------------------------|-----------|------------------|
| Specialized for GPU    | 75.1      | 5.1ms            |
| Specialized for CPU    | 75.3      | 7.4ms            |
| Specialized for Mobile  | 74.6      | 7.2ms            |

3 Automated Channel Pruning

Pruning [13] is widely used in model compression and acceleration. It is very important to find the optimal sparsity for each layer during pruning. Pruning too much will hurt accuracy; too less will not achieve high compression ratio. This used to be manually determined in previous studies [1]. Our goal is to automatically find out the effective sparsity for each layer. We train an reinforcement learning agent to predict the best sparsity for a give hardware [5]. We evaluate the accuracy and FLOPs after pruning. Then we update the agent by encouraging smaller, faster and more accurate models.

Our automatic model compression (AMC) leverages reinforcement learning to efficiently search the pruning ratio (Figure 1(b)). The reinforcement learning agent receives an embedding state $s_t$ of layer $L_t$ from the environment and then outputs a sparsity ratio as action $a_t$. The layer is compressed with $a_t$ (rounded to the nearest feasible fraction). Then the agent moves to the next layer $L_{t+1}$, and receives state $s_{t+1}$. After finishing the final layer $L_T$, the reward
TABLE 3. AMC speeds up MobileNet. On Google Pixel-1 CPU, AMC achieves 1.95× measured speedup with batch size one, while saving the memory by 34%. On NVIDIA Titan XP GPU, AMC achieves 1.53× speedup with batch size of 50.

| Policy          | FLOPs | ∆Acc (%) |
|-----------------|-------|----------|
| uniform (75-224) [3] | 56%   | -2.5     |
| AMC (ours)      | 50%   | -0.4     |
| uniform (75-192) [3] | 41%   | -3.7     |
| AMC (ours)      | 40%   | -1.7     |

TABLE 4. Learning-based automated model compression (AMC) outperforms rule-based model compression. Rule-based heuristics are suboptimal.

MobileNet-V1

Table 4 shows the performance of different multipliers and input sizes for MobileNet-V1 and MobileNet-V2. The performance is measured in terms of TOP-1 and TOP-5 accuracy, FLOPs, and the model size. AMC (ours) consistently outperforms the baseline policies.

4 Automated Mixed-Precision Quantization

Conventional quantization methods quantize each layer of the model to the same precision. Mixed-precision quantization is more flexible but suffers from a large design space that is difficult to explore. Meanwhile, as demonstrated in Table 5, the quantization solution optimized on one hardware might not be optimal on the other, which raises the demand for specialized policies for different hardware architectures and further increases the design space. Assuming the bitwidth is between 1 and 8 for both weights and activations, then each layer has 8^2 choices. If we have M different neural network models, each with N layers, on H different hardware platforms, there are in total O(H × M × 8^2N) possible solutions. Rather than using rule-based heuristics, we propose an automated design flow to quantize different layers with mixed precision. Our hardware-aware automatic quantization (HAQ) [6] models the quantization task as a reinforcement learning problem. We use the actor-critic model to give the quantization policy (#bits per layer) (Figure 1(c)). The goal is not only high accuracy but also low energy and low latency.

An intuitive reward can be FLOPs or the model size. However, these proxy signals are indirect. They do not translate to latency or energy improvement. Cache locality, number of kernel calls, memory bandwidth, and other factors all matter. Instead, we use direct latency and energy feedback from the hardware simulator. Such feedback enables our RL agent to learn the hardware characteristics for different layers: e.g., vanilla convolution has more data reuse and locality, while depthwise convolution has less reuse and worse locality, which makes it memory bounded.

In real-world applications, we have limited resource budgets (i.e., latency, energy, and model size). We would like to find the quantization policy with the best performance given the resource constraint. We encourage our agent to meet the computation budget by limiting the action space. After our RL agent gives actions \( \{a_k\} \) to all layers, we measure the amount of resources that will be used by the quantized model. The feedback is directly obtained from the hardware simulator. If the current policy exceeds our
Inference latency on

|   | HW1  | HW2  | HW3  |
|---|------|------|------|
| Best Q. policy for HW1 | 16.29 ms | 85.24 ms | 117.44 ms |
| Best Q. policy for HW2 | 19.95 ms | 64.29 ms | 108.64 ms |
| Best Q. policy for HW3 | 19.94 ms | 66.15 ms | 99.68 ms |

**TABLE 5.** Inference latency of MobileNet-V1 [3] on three hardware architectures under different quantization policies. The quantization policy that is optimized for one hardware is not optimal for the other. This suggests we need a specialized quantization solution for different hardware architectures. (HW1: spatial accelerator[14], HW2: edge accelerator[15], HW3: cloud accelerator[15], batch = 16).

Different, since (1) the batch size on the cloud servers are larger (2) the edge devices are usually limited to low computation resources and memory bandwidth. We use embedded FPGA Xilinx Zynq-7020 as our edge device, and server FPGA Xilinx VU9P as our cloud device to compare the specialized quantization policies.

Compared to fixed 8-bit quantization (PACT [16]), our automated quantization consistently achieved better accuracy under the same latency (see Table 6). With similar accuracy, HAQ can reduce the latency by 1.4-1.95× compared with the baseline.

Our agent gave specialized quantization policy for edge and cloud accelerators (Figure 3). The policy is quite different on different hardware. For the activations, the depthwise convolution layers are assigned much less bitwidth than the pointwise layers on the edge device; while on the cloud device, the bitwidth of these two types of layers are similar to each other. For weights, the bitwidth of these types of layers are nearly the same on the edge; while on the cloud, the depthwise convolution layers are assigned much more bitwidth than the pointwise convolution layers.

We interpret the quantization policy’s difference between edge and cloud by the roofline model. Operation intensity is defined as operations (MACs in neural networks) per DRAM byte accessed. A lower operation intensity indicates that the model suffers more from the memory access. The bottom of Figure 3 shows the operation intensity (OPs per byte) of convolution layers in the MobileNet-V1. On edge accelerator, which has much less memory bandwidth, our RL agent allocates fewer activation bits to the depthwise convolutions since the activations dominates the memory access. On cloud accelerator, which has more memory bandwidth, our agent allocates more bits to the depthwise convolutions and allocates fewer bits to the pointwise convolutions to prevent it from being computation bounded. Figure 4 shows the roofline model before and after HAQ. HAQ gives more reasonable policy to allocate the bits for each layer and pushes all the points to the upper right corner that is more efficient.

Finally, we evaluate the transfer ability of our framework: first train our agent on one network (MobileNet-V1), then directly apply the agent to another network (MobileNet-V2) (see Table 7). Our quantization policy transferred from MobileNet-V1 to MobileNet-V2 performs much better than the fixed-bitwidth baseline and is only slightly worse than the quantization policy directly searched for MobileNet-V2.
This experiment validates that our RL agent generalizes well to different network architectures. That’s to say, given a new model that the agent hasn’t seen before, it can utilize its past knowledge to give a decent quantization policy, saving the design cycle.

### 5 Conclusion

We present design automation techniques for efficient deep learning computing. There’s plenty of room at the algorithm level to improve the hardware efficiency, but the large design space makes it difficult to be exhausted by human. We covered three aspects of design automation: specialized model design, compression and pruning, mixed-precision quantization. Such learning based design automation outperformed rule-base heuristics. Our framework reveals that the optimal design policies on different hardware architectures are drastically different, therefore specialization is important. We interpreted those design policies and believe the insights will inspire the future software and hardware co-design for efficient deep learning computing.

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