Abstract  Robustness is a correctness notion for concurrent programs running under relaxed consistency models. The task is to check that the relaxed behavior coincides (up to traces) with sequential consistency (SC). Although computationally simple on paper (robustness has been shown to be PSPACE-complete for TSO, PGAS, and Power), building a practical robustness checker remains a challenge. The problem is that the various relaxations lead to a dramatic number of computations, only few of which violate robustness.

In the present paper, we set out to reduce the search space for robustness checkers. We focus on store-atomic consistency models and establish two completeness results. The first result, called locality, states that a non-robust program always contains a violating computation where only one thread delays commands. The second result, called singularity, is even stronger but restricted to programs without lightweight fences. It states that there is a violating computation where a single store is delayed.

As an application of the results, we derive a linear-size source-to-source translation of robustness to SC-reachability. It applies to general programs, regardless of the data domain and potentially with an unbounded number of threads and with unbounded buffers. We have implemented the translation and verified, for the first time, PGAS algorithms in a fully automated fashion. For TSO, our analysis outperforms existing tools.

1 Introduction

Performance drives the design of computer architectures. The computation time of a task depends on the time it takes to access the memory. To reduce the access time, the idea is to place the data close to the compute unit. This idea is applied on virtually all design layers, from multiprocessors to high-performance computing clusters. Yet, the realization is different. Multiprocessors like Intel’s x86 and Sparc’s PSO implement thread-local instruction buffers that allow to execute store commands without waiting for the memory. The effect of buffered stores will be visible to other threads only when the multiprocessor decides to batch process the buffer, thus leading to a reordering of instructions. Clusters often implement a programming model called partitioned global address...
space (PGAS), either in terms of APIs like SHMEM [20], ARMCI [35], GAS-
NET [11], GPI [32], and GASPI [25], or by HPC languages like UPC [21], Ti-
tanium [26], and Co-Array Fortran [36]. The PGAS model joins the partitioned
memories of the cluster nodes into one (virtual) global memory. The selling point
of PGAS is one-sided communication: A thread can modify a part of th e global
memory that resides in another node, without having to synchroniz e with that
node. The drawback is the network delay. Although already computed, it may
take a moment to install a value in the memory of another node.

Moving the data to the computation is delicate. When the data is shared,
it has to be split into copies, one copy for each thread holding the datum. But
then, in the interest of performance, updates to one copy cannot be propagated
immediately to the other copies. This means the computations have to relax the
guarantees given by an atomic memory and captured by the notion of sequential
consistency (SC) [31]. The commands no longer take effect on the global mem-
ory in program order but may be reordered by the architecture. An important
guarantee of SC, however, remains true in all the above models: Store atomicity.
Once a store command arrives at the global memory, it is visible to all threads.

Programming a shared memory is difficult. Having to take into account the
reorderings of the architecture makes programming in the presence of relaxed
consistency close to impossible. SC-preserving compilers have been proposed as
an approach to the problem and receive considerable attention [6,14,21,33,39,40].
The idea is to let the developer implement for SC, and make it the task of the
compiler to insert synchronization primitives that justify the SC-assumption
for the targeted architecture. Algorithmically, justifying the SC-assumption
amounts to checking a problem known as robustness (against the architecture of
interest): For every relaxed computation there has to be an SC-computation
with the same behavior. The notion of behavior to be preserved typically
(and also in this work) is the happens-before traces [30]. When developing
an SC-preserving compiler, checking robustness is the main task. Inferring
synchronization primitives from indications of non-robustness is better under-
stood [1,2,3,5,7,13,27,29,34,41].

An SC-preserving compiler needs an over-approximate robustness analysis
that should be as precise as possible. Under-approximations like bounded model
checking [5,15,16], simulation [8], or monitoring [17,18] may miss non-robust
computations and insert too few fences. Over-approximations, if too coarse, lead
to over-fencing. Although decision procedures for robustness exist [14,19,23],
building an efficient and yet precise robustness checker remains a challenge. The
problem is the immense degree of non-determinism brought by the instruction
reorderings that is hard to reflect in the analysis. This non-determinism forces
over-approximations into explicitly modeling architectural details like instruction
buffers [14,22,28] (operational approaches) or right-away operating on the code
(axiomatic approaches) [3,6,59].

In this paper, we contribute two semantical results about robustness that
limit the degree of non-determinism that has to be taken into account by algo-
ithmic analyses. Both results state that robustness violations can be detected —
in a complete way — with a restricted form of reorderings. The first result, called locality, states that only one thread needs to make use of instruction reorderings. The other threads operate as if they were running under SC: A program is not robust if and only if there is a violating computation where exactly one thread delays stores. The second result, called singularity, is even stronger: A program without lightweight fence instructions is not-robust if and only if there is a violating computation with exactly one delayed store. Note that a program without delays is robust. This means the result is an optimal characterization of non-robustness. Singularity only holds in the absence of lightweight fences. We do not consider this a severe limitation. Robustness is meant as a subroutine for fence inference inside an SC-preserving compiler. In that setting, programs naturally come without fences.

Our third contribution shows that the development of specialized robustness analyses can be avoided. Utilizing locality and singularity, we give an instrumentation that reduces robustness to reachability under SC. By instrumentation, we mean a source-to-source translation of a given program P into a program P′ so that the former is robust if and only if the latter does not reach under SC a designated state. This allows us to employ for the analysis of robustness all techniques and tools that have been developed for SC-reachability. As a side-effect, we obtain the decidability of robustness for parameterized programs over a finite data domain. The restriction to finite data domains is not necessary for the instrumentation itself, but for the back-end SC-reachability analysis.

Concerning the model, we show that locality holds for virtually all store-atomic consistency models (singularity holds in the absence of dependencies). Inspired by [9], we introduce a programming language for concurrent programs that is meant to act as a programming framework for store-atomic models. The syntax of our language is an assembly dialect enriched with a variety of fence commands. The semantics is defined weak enough to support the relaxations found in the models discussed above. What makes our programming language a programming framework is that, given a program, we can add appropriate fences to obtain the behavior under SC, TSO, PSO, and PGAS. The motivation for having a programming framework is that we can show locality and singularity once for this model, and it will then hold for all instances of the framework.

For improved readability, this paper contains only a comprehensible high-level explanation of our techniques. The full technical formalizations and proofs can be found in the appendix.

2 Related Work

Robustness checks that the relaxed behavior of a program is the same as the behavior under SC. The definition is relative to a notion of behavior, and there are various proposals in the literature [1239]. To make the most of the consistency model in terms of performance, the notion of behavior should be liberal enough to equate quite distinct computations. On the other hand, it should be strong enough to be easy to check algorithmically. Equivalence of the happens-before
traces [39] appears to be a good compromise between expressiveness and algorithmics, and is the favored notion in the literature on robustness [6,13,14,17,18,19]. Abdulla et al. recently proposed an alternative that is incomparable with the happens-before traces [2]. The idea is to preserve the total ordering of all stores and drop the relations for loads. This equivalence leads to efficient algorithmics for TSO but does not seem to fit well with consistency models beyond TSO. State-space equivalence from [1] leads to non-primitive recursive lower bounds for robustness, and will therefore also not be our choice.

In our earlier work on TSO [13], PGAS [19], and Power [23], we established normal form results similar to locality and singularity and also made use of the combinatorial proof principle. We elaborate on why the reasoning in this paper is substantially different from our earlier efforts. Figure 1 summarizes the comparison. The results about PGAS [19] and Power [23] rely on a normal form (Ordered in Figure 1) for violating computations where all three delays commands. As the normal form gives weak guarantees, it can be established with a cost function that simply measures the length of violating computations. The value of these earlier results is in that they apply to all consistency models which forbid out-of-thin-air values, while giving the precise complexity (but no useful algorithms). For TSO, we proved locality in [14]. As TSO architectures have one buffer per thread, we were able to apply a cost function that only measures delays, i.e., the number of commands that are processed while a store is being buffered (Figure 1). In this paper, we also have to account for overtakes of stores in different buffers. Another aspect is that, for TSO, we managed to leave the happens-before trace unchanged. We tried to lift this strategy to PGAS but failed. Instead, we show how to construct a different computation that still is a violation. Taking apart the computation was a big step.

The instrumentation we present in Section 8 is related to our work on TSO [13]. To be precise, we adapt the instrumentation of the attacker (that delays commands) to the assumption of singularity and to the more relaxed consistency model. The instrumentation of the helper threads (that close the happens-before cycle) is the one from ESOP’13. Since our earlier work assumes locality, the new instrumentation (for singularity) is more compact (we save a linear number of auxiliary addresses). An alternative instrumentation-based
robustness analysis is presented in [4]. The instrumentation precomputes an optimized cycle and then checks robustness wrt. that cycle. The idea can be understood as trading one complex verification task (robustness) for a number of tasks (robustness wrt. a cycle) that can be solved more efficiently. A strong point is that the approach is general enough to apply to non-store-atomic consistency models, including Power. For TSO, PSO, and PGAS, also that instrumentation will benefit (in terms of size) from locality and singularity. Related is also the instrumentation in [2]. Atig et al. only have to add two variables to the program, which means the instrumentation is more compact than ours. But, as explained above, the approach does not seem to be generalizable beyond TSO.

Instrumentations that mimic the effect of instruction buffers can also be found in reachability analyses for relaxed consistency models. Bouajjani et al. apply the idea of bounded context switching to TSO [10]. Vechev et al. [22] precompute the utilization of the instruction buffers in TSO and PSO, and show how to mimic them under SC without having to shift content between variables. Common to both works is that they eagerly simulate the effect of buffers. In [12], we show how to introduce store buffering lazily, and only where needed to satisfy a TSO reachability query: The idea is to guide the store buffering by non-robust computations. Hence, also reachability analyses benefit from the improvements for robustness presented here.

In this paper, we focus on store-atomic memory models. Although store atomicity feels like a natural requirement, important multiprocessors like Power [8, 23, 37] or ARM [8] are known to be non-store atomic. There, stores to independent variables may arrive in independent threads in a different order. What remains true is coherence. All threads see the stores to each variable in the same order. A major challenge for future work is to understand whether a locality result can be established for Power, potentially under mild assumptions on the programs. With the results in this paper, singularity can be shown not to hold, Figure [1].

3 Locality and Singularity on an Example

We illustrate the concept of robustness and the main results on singularity and locality with the help of message passing, an idiom common in shared memory concurrent programming. The code is as follows:

```
program MessagePassing
thread t_w regs init l_0 begin
  l_0: mem[d_1] ← 1; goto l_1;
  l_1: mem[d_2] ← 1; goto l_2;
  l_2: mem[flag] ← 1; goto l_3;
end

thread t_r regs r init l_x begin
  l_x: r ← mem[flag]; goto l_y;
  l_y: assert r = 1; goto l_z;
  l_z: r ← mem[d_1]; goto l_t;
end
```

The task of the idiom is to signal to thread t_r (called reader) that the data written by thread t_w (called writer) is ready for use. The idiom is useful when
the data to be written cannot be updated atomically. The situation is as follows. The writer stores data in the addresses \( d_1 \) and \( d_2 \). To hand over the data to the reader, \( tw \) raises flag (initially, all addresses are 0). The reader reads the flag and finds it raised. From this, it concludes that \( d_1 \) has a new value and reads it.

For message passing to work, we need the following guarantee: Before the flag is raised, the stores to \( d_1 \) and \( d_2 \) have to be visible in memory. The guarantee holds for SC and TSO but does not hold for PGAS. Indeed, without further synchronization the above code will fail on a cluster. The stores to \( d_1 \) and \( d_2 \) may be delayed due to network latencies (they may be big packages). While these stores are being processed, the flag is successfully set. The reader sees the flag and reads the old (or broken due to an incomplete transfer) value at \( d_1 \).

The message passing idiom is not robust. It works properly under SC but fails when ported to PGAS. Formally, robustness requires that for every computation under PGAS there is a computation under SC that has the same happens-before trace. We will show that this is not the case. Consider the computation

\[
\tau = isu_a \cdot isu_b \cdot isu_c \cdot c \cdot d \cdot e \cdot f \cdot b \cdot a,
\]

where \( isu_a \) gives the moment when action \( a \) is issued and \( a \) itself gives the moment when the command is executed on memory. The meaning of the actions is given in Figure 2, which shows the happens-before trace \( Tr(\tau) \) of the computation. The happens-before trace reflects the crucial dependencies among the actions: The program order, the store order, and the source and conflict relations between loads and stores. Computations with the same happens-before trace only differ in how they shuffle independent action. For computation \( \tau \), we see that the flag raised by action \( c \) is read by action \( d \) (indicated by the source relation), but the load of \( d_1 \) in action \( f \) is overwritten by the later action \( a \) (conflict relation).

The load at \( f \) obtains an old value although the flag was raised. Under SC where commands take immediate effect this is impossible. Formally, the fundamental lemma of Shasha and Snir states that for a relaxed computation \( \tau \) there is an SC-computation \( \sigma \) with \( Tr(\tau) = Tr(\sigma) \) if and only if \( Tr(\tau) \) is acyclic [39]. As the above \( Tr(\tau) \) is cyclic, computation \( \tau \) has no SC-equivalent. Hence, message passing is not robust.

Our singularity result shows that the above computation is unnecessarily complicated. The theorem states that we need to delay only one action in order
to find a robustness violation (a computation with a cyclic trace). In the example, we can avoid the delay of action $b$. Computation

$$\tau' = \text{isu}_a \cdot \text{isu}_b \cdot b \cdot \text{isu}_c \cdot c \cdot d \cdot e \cdot f \cdot a$$

has the same (cyclic) happens-before trace as $\tau$ but only delays $a$.

To render formally the intuitive feeling that computation $\tau'$ is less relaxed than $\tau$, we associate with each computation a cost. The cost of computation $\tau$ is $\$\tau = (6, 3, 9)$. There are 6 delays. Indeed, $a$ is delayed past $\text{isu}_b \cdot \text{isu}_c \cdot c \cdot b$ and $b$ is delayed past $\text{isu}_c \cdot c$. There are 3 reordering, action $a$ is issued before $b$ and $c$ but hits the memory later. Similarly, $b$ gets reordered past $c$. Altogether there are 9 actions. For computation $\tau'$, we have $\$\tau' = (4, 2, 9)$. We compare the costs lexicographically and find $\tau'$ less relaxed.

4 Concurrent Programs

**Syntax** The syntax of our programming language is defined below. A concurrent program is identified by a name and consists of a finite set of named threads. The threads share a global memory. Moreover, each thread defines a finite set of local registers. The code is given as a finite set of labelled instructions. Each instruction includes a command and the label of the instruction to be executed next. To model non-deterministic choices, several instructions can have the same label. The instruction set includes loads from memory, stores to memory, local assignments, asserts, and two kinds of fences, SC-fences forbid relaxations altogether. The second fence command is parameterized by a set of addresses. To be more precise, the program comes with a domain $\text{DOM}$ the elements of which model the data values as well as the addresses in the global memory. We assume the domain contains a distinguished value $0 \in \text{DOM}$ that will be used for initialization purposes. Besides $\text{DOM}$, there is also a function domain $\text{FUN}$ that contains elements from $\text{DOM}^* \to \text{DOM}$. All functions that are used in expressions have to stem from $\text{FUN}$.

$$\langle \text{prog} \rangle ::= \text{program} \langle \text{pid} \rangle \langle \text{thrd} \rangle^*$$

$$\langle \text{thrd} \rangle ::= \text{thread} \langle \text{tid} \rangle$$

- $\text{reg}s \langle \text{reg} \rangle^*$
- $\text{init} \langle \text{label} \rangle$
- $\text{begin} \langle \text{linst} \rangle^* \text{end}$

$$\langle \text{linst} \rangle ::= \langle \text{label} \rangle; \langle \text{inst} \rangle; \text{goto} \langle \text{label} \rangle;$$

$$\langle \text{inst} \rangle ::= \langle \text{reg} \rangle \leftarrow \text{mem}[\langle \text{expr} \rangle]$$

- $\text{mem}[\langle \text{expr} \rangle] \leftarrow \langle \text{expr} \rangle$
- $\langle \text{reg} \rangle \leftarrow \langle \text{expr} \rangle$
- $\text{assert} \langle \text{expr} \rangle$
- $\text{scfence}$
- $\text{fence} \langle \text{expr} \rangle^*$

$$\langle \text{expr} \rangle ::= \text{fun}(\langle \text{reg} \rangle^*)$$

**Semantics** Under SC, a store command takes immediate effect on the global memory. We consider consistency models that relax the program order but preserve store atomicity. This means the effect of a store command may not become visible immediately (to the other threads), but later commands may overtake the
store and hit the memory earlier than the store. What is guaranteed, however, is that once the store is visible it is visible to all threads.

The semantics specifies $C(P)$, i.e., the set of computations for program $P$. We define the relaxed semantics of our assembly language in an operational style, in terms of a hardware architecture that processes instructions. In this model, out-of-program-order computations result from the use of instruction buffers inside the architecture. To provide an umbrella for different store-atomic models, the architecture has two types of buffers. Buffers of the first type are per thread and per address FIFO buffers that only hold stores of one thread to one address. Buffers of the second type are per thread FIFO buffers that hold stores of one thread to potentially different addresses. The per-address buffers emulate PGAS. An all-addresses buffer mimics TSO.

When a thread issues a store, the instruction is put into the corresponding per-address buffer. From the per-address buffers, the store non-deterministically advances to the all-addresses buffer of that thread. From the all-addresses buffer, the store eventually arrives at the global memory. Due to the per-address buffers, stores of the same thread to different addresses may enter the memory in an order different from the order in which they were issued.

When doing a load, a thread checks whether there is a store to the address of interest kept in one of the store buffers. If not, the thread loads the current value from the main memory. If so, the thread loads the value of the most recent store in the buffers (where stores in the per-address buffers are more recent than stores in the all-addresses buffer). The definition ensures that the thread sees its own stores in issue order. Even more, for a sequential program the architecture appears to implement SC.

To synchronize different threads, the language offers two fence instructions. The `scfence` instruction can only be executed if all buffers of the executing thread are empty. Additionally, we have the `fence` instruction that carries a list of addresses. It can be executed if the buffers for the given addresses in the executing thread are empty.

We show that the framework encompasses the consistency models we aim at. **Sequential consistency** Lamport’s SC [31] is the intuitive consistency model that reflects an atomic shared memory. Formally, the SC-computations are the valid interleavings of the computations of all threads. We can mimic SC in our framework by letting stores directly go to memory. To enforce this, one can insert an `scfence` after each store. We avoid this modification and just write $C_{SC}(P)$ to mean the set of SC-computations of program $P$.

**Total Store Ordering** TSO implements the store-to-load relaxation. Each thread has a single buffer for stores, and loads may overtake buffered stores when early reads fail. Notably, the thread-local total order of stores is preserved. Intel’s x86 architecture implements TSO [38].

The all-addresses buffers in our framework are meant to mimic TSO. To preserve the total order of stores, the per-address buffers must not be used. We can insert `fence` instructions after each store command to enforce TSO.
Partial Store Ordering  For PSO [42], there are two kinds of relaxation, the store-to-load relaxations of TSO and the store-to-store relaxation. The latter means that stores of the same thread to different addresses can be reflected in the global memory in an order that is different from the program order.

The per-address-buffers enable the additional store-to-store relaxation. As long as a store resides in its per-address buffer, stores to other addresses can be executed faster and the buffered store gets delayed. A program that is executed unmodified (without further fences) in our framework will run with PSO semantics. The benefit of PSO is that it approximates well the behavior of PGAS.

Partitioned Global Address Space  In a PGAS clusters, the cluster nodes create FIFO buffers to transfer data to and request data from neighboring nodes. The transfer itself is handled by the network infrastructure. PGAS APIs allow the user to specify the buffer that should be used for a transfer. A comparison and precise model of PGAS APIs can be found in [19]. The model presented here is designed as an approximation of PGAS that is less complex and hence easier to handle wrt. the theory we develop. Rather than assigning stores to buffers, we give each store a separate buffer, like in PSO. The user defined sharing of buffers is mimicked by the parameterized fences. The approximation is a bit weak as it forces different buffers into a total ordering.

5  Robustness

We first define the happens-before relation and, based on this, the notion of robustness. As a first step towards locality and singularity, we then work out properties of computations that violate robustness.

Given $\tau \in C(P)$, the happens-before relation highlights the crucial control and data-flow dependencies in the computation. Crucial means that an alternative computation with the same relations and valid delays is guaranteed to be executable in the program. In particular, all asserts will receive the same values. Technically, the happens-before relation $\rightarrow_{\text{hhb}} = \rightarrow_{\text{po}} \cup \rightarrow_{\text{st}} \cup \rightarrow_{\text{src}} \cup \rightarrow_{\text{cf}}$ is the union of different dependencies between two actions. The program order $\rightarrow_{\text{po}}$ denotes the control flow between actions of the same thread. The remaining orders can be summarized as follows. Whenever two actions $x$ and $y$ operate on the same address in the shared memory, follow each other in $\tau$, and at least one of them is a store, then we have $x \rightarrow_{\text{hb}} y$. It is common to distinguish the relations according to the commands. The store order $\rightarrow_{\text{st}}$ denotes the order in which two stores to the same address reach the memory. The source relation $\rightarrow_{\text{src}}$ goes from a store action to a load action of the same address and denotes the fact that the load reads the value written by that store. The conflict relation $\rightarrow_{\text{cf}}$ is a derived relation and says that a load has to happen before a store that potentially overwrites the value to be read.

The happens-before trace $\text{Tr}(\tau)$ associated with computation $\tau \in C(P)$ is the directed graph where the nodes are the actions from $\tau$. To be precise, isu, x and store or fence $x$ are represented by the same node $x$. The edges are given by the
four happens-before relations. Note that each computation induces a trace but several computations can have the same trace.

The robustness problem is to check, given a concurrent program, whether the traces obtained from the computations in the model from the previous section are included in the traces of the SC computations:

Given program $P$, does $\text{Tr}(C(P)) \subseteq \text{Tr}(C_{SC}(P))$ hold?

Algorithmically, the task is to look for violations of robustness, computations $\tau \in C(P)$ with $\text{Tr}(\tau) \notin \text{Tr}(C_{SC}(P))$. Shasha and Snir observed that violating computations are precisely those with a cyclic happens-before relation.

**Lemma 1 ([39]).** Consider $\tau \in C(P)$. Then $\text{Tr}(\tau) \in \text{Tr}(C_{SC}(P))$ if and only if $\text{Tr}(\tau)$ is acyclic.

To see this, consider an acyclic trace. It will have a linearization that forms an SC computation. In turn, every SC computation will have an acyclic trace. Under SC, all commands execute atomically and there is no chance for delays. The following development can be understood as strengthening the insight of Shasha and Snir.

### 5.1 Minimal Violations

To deepen our understanding of violating computations, we will concentrate on violations that are minimal in a carefully chosen order. The main finding is the following. In a minimal violation, *every delay is due to a cycle*. To derive this fact, we employ an interesting proof strategy that establishes properties by contradiction and that will occur in variants throughout the paper. Starting from a minimal violation, we assume the property of interest would not hold and from this deduce the existence of a smaller violation.

Technically, we define minimal violations with the help of a cost function $\$(·)$ mapping computations to a well-founded domain. Intuitively, the cost of a computation reflects its degree of relaxation. A minimal violation is then a violation that is as little relaxed as possible (while being a violation). Phrased differently, the computation is as close to SC as possible. Hence, the cost can also be understood as a penalty for deviating from SC.

The thing to note about the definition of cost is that we define it on the per-thread computations. This means that two computations $\tau_1, \tau_2 \in C(P)$ with the same per-thread computations, $\tau_1 \downarrow t = \tau_2 \downarrow t$ for all threads $t$, will have the same cost, $\$(\tau_1) = \$(\tau_2)$. Like the proof strategy, this equality will be applied over and over again. It allows us to choose between different interleavings while preserving minimality.

Technically, the cost of a computation is a triple of natural numbers:

$$\$(\tau) := (\text{delays}(\tau), \text{reorders}(\tau), \text{length}(\tau)) \in \mathbb{N}^3.$$  

We refer to the three auxiliary functions as penalty functions and define them below. Cost triples in $\mathbb{N}^3$ are compared lexicographically, so $(4, 0, 6) < (4, 1, 5)$. 

When we refer to a minimal violation, we mean a violation \( \tau \) where the cost \( \$(\tau) \) is minimal in the set of violating computations.

The intuitive meaning of the penalty functions is as follows. The function \( \text{delays}(\cdot) \) increases when actions happen between an issue and the corresponding store or fence action in memory. Such intermediary actions indicate a delay of the store. Since delays are impossible under SC, there is a penalty for them. To be precise, we only consider intermediary actions from the thread that executed the store or fence. The function \( \text{reorders}(\cdot) \) gives a penalty to reordering delayed stores. It increases when stores reach the memory in an order different from the order in which they were issued. Keeping this function value small forces stores of the same thread to different variables to respect the program order. Finally, function \( \text{length}(\cdot) \) gives the computation’s length as we would like to focus on violations that do not contain unnecessary actions. We turn to the formalization.

The length of a computation \( \tau \), denoted by \( \text{length}(\tau) \), is the number of actions in \( \tau \). The special case \( \varepsilon \) is defined to have length zero.

To define the number of delays, consider the computation \( \tau = \tau_1 \cdot \text{isu}_a \cdot \tau_2 \cdot a \cdot \tau_3 \) where \( a \) is a delayed store or fence action. Let \( \text{thread}(a) := t \). We say that \( a \) overtakes every action in \( \tau_2 \) projected to \( t \). Hence, for this one store or fence the number of delays is \( \text{delays}(a) := \text{length}(\tau_2 \downarrow t) \). The number of delays in \( \tau \) is the sum of the delays of all stores and fences:

\[
\text{delays}(\tau) := \sum_{\text{all stores and fences } a \text{ in } \tau} \text{delays}(a).
\]

A store or fence \( a \) is said to be reordered if it overtakes another issue \( \text{isu}_b \) together with the corresponding store or fence \( b \). Here, \( a \) and \( b \) are supposed to have the same thread \( \text{thread}(a) = t = \text{thread}(b) \). So we have

\[
\tau = \tau_1 \cdot \text{isu}_a \cdot \tau_2 \cdot a \cdot \tau_3 \quad \text{with} \quad \tau_2 = \tau_{2a} \cdot \text{isu}_b \cdot \tau_{2b} \cdot b \cdot \tau_{2c}.
\]

The number of reorders for the store \( a \), denoted by \( \text{reorders}(a) \), is the number of such stores or fences \( b \) in \( \tau_2 \downarrow t \). The number of reorders in a computation \( \tau \), \( \text{reorders}(\tau) \), is again the sum of the reorders of all stores and fences in \( \tau \).

### 5.2 Cycles

Our goal is to establish the following result about minimal violations. Whenever we have an action \( a \) that has been overtaken by another action \( b \), then we already find a cycle involving the two. To be more precise, either the cycle is via the intermediary actions between \( a \) and \( b \) (Proposition H(i)), or the cycle is via a dependency from \( \text{isu}_b \) to \( a \) (Proposition H(ii)). For the precise statement, we need a stronger variant of the happens-before relation.

We will often argue that some of the intermediary actions are sufficient to establish the existence of a happens-before path between two actions. To make this dependence on the intermediary actions explicit, we recall the happens-before-through relation from [1]. It can be understood as embedding the happens-before relation, or more generally the trace, into the underlying computation,
which is a linear structure. Consider the computation \( \tau = \tau_1 \cdot a \cdot \tau_2 \cdot b \cdot \tau_3 \in C(P) \). We say that action \( a \) happens before action \( b \) through \( \tau_2 \), if there is a subsequence \( a_1 \ldots a_n \) of \( \tau_2 \) so that one of

\[
a_i \rightarrow^+_{po} a_{i+1}, \quad a_i \rightarrow^+_{src} a_{i+1}, \quad a_i \rightarrow^+_{bf} a_{i+1}, \quad \text{or} \quad a_i \rightarrow^+_{cf} a_{i+1}
\]

holds for all \( 0 \leq i \leq n \) with \( a_0 := a \) and \( a_{n+1} := b \). We also refer to \( a_0 \cdot \ldots \cdot a_n \cdot b \) as a happens-before-through chain.

**Proposition 1 (Cycles).** Let \( \tau = \tau_1 \cdot a \cdot \tau_2 \cdot b \cdot \tau_3 \in C(P) \) be a minimal violation where \( a \) has been overtaken by \( b \). One of the following holds:

(i) \( b \rightarrow^+_{po} a \) and \( a \rightarrow^+_{hb} b \) through \( \tau_2 \)
(ii) \( a \rightarrow^+_{po} b \) and \( \tau_1 = \tau_1 \cdot isub \cdot \tau_1 b \) and \( isub \rightarrow^+_{hb} a \) through \( \tau_1 b \).

**Remark:** Both cases lead to a happens-before cycle with actions in \( \tau_1 \cdot a \cdot \tau_2 \cdot b \).

The proof of Proposition 1 is non-trivial and relies on a strong dichotomy result, Lemma 2. The lemma is a disjunction (i) or (ii) and should be read as two implications. If we read it as \( \neg (i) \) implies (ii), it states that given a minimal violation two actions can be swapped as long as they are not separated by a happens-before-through chain. This will allow us to modify a given computation. If we read the dichotomy as \( \neg (ii) \) implies (i), it states that given a minimal violation whenever we see two actions of the same thread we are already sure to have a happens-before-through chain between them.

**Lemma 2 (Dichotomy [14]).** In a minimal violation \( \tau = \tau_1 \cdot a \cdot \tau_2 \cdot b \cdot \tau_3 \in C(P) \) with \( \text{thread}(a) = \text{thread}(b) \) we have \( a \rightarrow^+_{hb} b \) through \( \tau_2 \).

The corollary is particularly interesting in the setting where action \( b \) has overtaken action \( a \). In this case, it states that the overtake was actually required to execute the actions in the following sense. The intermediary actions form a happens-before-through chain that prevents \( b \) from being executed before \( a \). The existence of this chain renders formally the intuition that minimal violations do not contain unnecessary delays.

To see the corollary, assume there was no happens-before-through chain. Lemma 2 would allow us to swap the actions \( a \) and \( b \) while preserving the per-thread computations — in contradiction to the fact that the actions stem from the same thread.
Proof (of Proposition 1). Since $b$ overtakes $a$, they are from the same thread and thus program-order dependent. Furthermore, $b$ is a store or a fence. If $b \rightarrow_{po}^+ a$, it is immediate to complete the cycle stated in (i): Corollary 1 yields $a \rightarrow_{hb}^+ b$ through $\tau_2$. If $a \rightarrow_{po}^+ b$, we find the issue action $isu_a$ in $\tau_1$, say $\tau_1 = \tau_{1a} \cdot isu_b \cdot \tau_{1b}$. From Corollary 1, $isu_b \rightarrow_{hb}^+ a$ through $\tau_{1b}$, as required in (ii). □

6 Locality

**Theorem 1 (Locality).** A concurrent program is not robust if and only if there is a violating computation where exactly one thread delays actions.

The difficult task is to show completeness. We can show that we only need to consider minimal violations of the form $\tau = \tau_1 \cdot x \cdot \tau_2 \cdot y \cdot \tau_3 \cdot st_y \cdot \tau_4 \cdot st_x \cdot \tau_5$ where $x$ is overtaken by $st_x$ and $y$ is overtaken by $st_y$ with $x$ and $y$ being from different threads. There are two happens-before cycles: one between $x$ and $st_x$, the other between $y$ and $st_y$. The goal is to move $st_y$ back over $y$ to save one delay while preserving the computation’s trace, or at least get another valid computation with a slightly different trace that also contains a happens-before cycle. This will be the cycle between $x$ and $st_x$. Therefore, we get a violation with less delays than the original one. This contradicts the initial assumption that the chosen computation was a minimal violation.

With locality at hand, we can constrain the shape of minimal violations. A similar normal form was presented for TSO in [13], and we can adapt it to the current setting with minimal changes.

**Proposition 2 (Witnesses [13]).** Program $P$ is robust if and only if there is no minimal violation $\tau = \tau_1 \cdot isu_A \cdot \tau_2 \cdot a \cdot \tau_3 \cdot st \cdot \tau_4 \in C(P)$, called witness computation, that satisfies the following requirements.

(W1) Only $t_A := \text{thread}(st) = \text{thread}(a)$ delays actions.
(W2) $\tau_3 \downarrow t_A = \varepsilon$.
(W3) $\tau_1$ and $\tau_2 \cdot a \cdot \tau_3$ do not contain delayed actions.
(W4) For every $b$ in $\tau_3 \cdot st$ we have $a \rightarrow_{hb}^+ b$ through the intermediary actions.
(W5) $\tau_4$ only contains delayed stores and fences of $t_A$.

Following [13], thread $t_A$ is referred to as the attacker, the remaining threads are called helpers. The computation in our running example is a witness:

$\tau' = isu_a \cdot isu_b \cdot b \cdot isu_c \cdot c \cdot d \cdot e \cdot f \cdot a$.

Here, $isu_{st}$ is $isu_a$ and the overtaken action is $c$. Part $\tau_3$ is $d \cdot e \cdot f$.

7 Singularity

Our second main result shows that it is sufficient to delay only a single store action. The theorem only holds in the absence of lightweight fence commands,
scfence is still allowed. We stress that the theorem is optimal in the sense that it characterizes the least relaxation required to violate sequential consistency. A program without delayed stores is always robust.

**Theorem 2 (Singularity).** Consider a program without fence. It is not robust if and only if there is a violation with exactly one delayed store.

The proof is short and derives a contradiction to a strong combinatorial property. The reasoning is as follows. If the program has a violation with one delayed store, it is not robust. If the program is not robust, by Proposition 2 there is a minimal violation that is a witness computation as defined in the previous section. In this computation, \( \tau_4 \) only consists of delayed stores and fences of the attacker thread. We assume the program does not contain fence commands. This means \( \tau_4 \) only consists of delayed stores of the attacker. Now, if more than one store was delayed, we would have a contradiction to the following Proposition 3 that came as a surprise to us. A minimal violation will never place two delayed stores next to each other. This already concludes the argumentation.

**Proposition 3 (Two Stores).** In the absence of fence, there is no minimal violation \( \tau_1 \cdot st_1 \cdot st_2 \cdot \tau_2 \) with \( \text{thread}(st_1) = \text{thread}(st_2) \).

### 8 Instrumentation

To check robustness, we have to look for minimal violations. Proposition 2 reduces the search space as we only have to consider minimal violations in witness form. If the program does not use the fence instruction, then also singularity holds and \( \tau_4 \) will be empty in all witness computations. Our instrumentation is an adaptation of [13].

**Attacks** An attack is a triple \( A = (t_A, stinst, lastinst) \), where \( t_A \) is a thread, \( stinst \) is a store instruction of \( t_A \), and \( lastinst \) is a store or load instruction of \( t_A \). Note that attacks are syntactic objects and there is a quadratic number of them. An attack \( A \) is feasible if there is a witness computation where \( t_A \) plays the role of the attacker, \( st \) is an instance of \( stinst \), and \( a \) is an instance of \( lastinst \). With Proposition 2 the program is robust if and only if no attack is feasible. Given an attack, we now develop an instrumentation that finds a witness for it.

The witness computation of interest has four phases:

1. In \( \tau_1 \), all issued stores are immediately written to the memory. Eventually, the attacker decides to delay a store.
2. In \( \tau_2 \), further actions of the attacker happen either without delay or they are delayed until \( \tau_4 \). The helpers execute arbitrary actions. At some point, the attacker does its last normal action \( a \), which is a load or non-delayed store.
3. In \( \tau_3 \), the helpers execute only actions that are happens-before-dependent on \( a \) while the attacker pauses.
4. In \( \tau_4 \), only the attacker’s delayed actions get executed.
We use an observation from [13] that limits the information we have to track about the delayed stores. The argumentation is as follows. If there are delayed stores to an address, the attacker will load the last value that was put into the corresponding buffer. The helpers will load the last value that was stored in memory. Combined with Property (W3) of witness computations — $\tau_2 \cdot a \cdot \tau_3$ does not contain delayed actions — the content of the buffers is not needed. All we have to track is two values per address: The current value in memory and the value of the last buffered store, if any. When the attacker executes a store that is delayed, it will set the buffered value. When the attacker executes a store without delay or the helpers execute a store, it updates the current value in memory. Loads from helpers will always read the current value from memory while loads from the attacker will prefer the buffered one, if it is set.

Recall that the values in DOM act as addresses. We extend DOM as follows: For each $x \in \text{DOM}$ we add auxiliary addresses $(x, d)$ and $(x, hb)$. The addresses $(x, d)$ hold the values of the last buffered stores. The addresses $(x, hb)$ are used to track the happens-before-dependencies required by (W4). Here, we rely on the mechanism from [13]. Furthermore, we add the auxiliary addresses $hb$ and $suc$. Flag $hb$ will tell the helpers that Phase 3 has started and they must execute $hb$-dependent actions. Flag $suc$ indicates a feasible attack.

**Instrumentation of the Attacker for Locality** The attacker operates in three modes. Initially, instructions are executed under SC (Phase 1). Upon execution of $\text{stinst}$, the attacker can decide to delay that store. If the store is to address $x$, we save the stored value to $(x, d)$ and the address $x$ to an auxiliary register $r_{stx}$. The control flow changes to a modified copy of the code for Phase 2.

During Phase 2, when the attacker has to load from address $y$, it will first check whether $(y, d)$ is set. If so, it reads that value, otherwise it reads the value of $y$. A store to address $y$ can either directly go to memory location $y$ or it is delayed and stored to $(y, d)$. If there already is a buffered value, then the store cannot be done on memory and has to update the buffered value — due to the FIFO property of buffers. Additionally, we have to delay all stores if there was a fence that had to be delayed. A fence has to be delayed if there is a buffered value for at least one of its addresses. We use an additional register $r_{fence}$ as a flag indicating that a fence has been delayed. An scfence action is not permitted in Phase 2 and will lead to a deadlock.

Upon execution of $\text{lastinst}$, the attacker can decide that this is its last action. If it is a load, we make sure that there is no buffered value for that address. Otherwise, there is no possibility for $hb$-dependent actions in $\tau_3$. We set the $hb$ flag and go to a special wait label. If $\text{lastinst}$ is a store, then we have to make sure that it can be stored directly, i.e., there is no delayed fence and no delayed store for that address. We execute the store, set the $hb$ flag, and go to the wait label.

The third mode is in the wait label. The attacker waits until a helper thread has completed the happens-before chain, in which case it sets the success flag.

Compared to [13] for TSO, what is new is the handling of non-delayed stores and fences, and the optimized detection of violations by the attacker.
Optimized Instrumentation of the Attacker for Singularity  When the program does not make use of the fence instruction, then singularity holds. We can simplify the above instrumentation as follows. As only one store is delayed, we can use a single register $r_{\text{delayval}}$ instead of the auxiliary addresses $(x, d)$ to save the corresponding value. Recall that the address is kept in $r_{\text{st}}$.

9 Discussion

We have shown that locality and singularity hold for virtually all store-atomic consistency models (singularity holds in the absence of fence instructions). Based on this, we have shown how to reduce robustness to reachability under SC. The study was motivated by our interest in PGAS clusters. The immediate next question to ask is whether similar results could hold for non-store-atomic models like Power. The answer is: We do not yet know. There is, however, a number of proof principles for relaxed consistency models that came out of this investigation. First, it seems that a dichotomy lemma is helpful: Whenever there are two actions from the same thread, there already is a happens-before path between them (Corollary 1). This, in turn, seems to hold whenever we minimize the cost of computations according to the number of delays plus the reorderings. We did not have this result in our work on Power [23] but one may be able to lift it. Another attractive result that one may want to generalize is the delay of neighboring elements, which is forbidden under minimality (Proposition 3). The ultimate goal would be to develop an understanding under which conditions a consistency model would satisfy a property like locality or singularity.
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A Details on the Semantics

Consider a program \( P \) consisting of the threads \( \text{THRD} = \{t_1, \ldots, t_n\} \). Let \( \text{LAB} \) be the set of all labels that are declared in \( P \). Assume each thread \( t_i \) has the initial label \( l_{0,i} \) and defines the registers \( r_i \). We use \( \text{VAR} := \text{DOM} \cup \bigcup_{\ell \in [1,n]} \overline{r_\ell} \) to refer to the set of all variables, i.e., the set of all addresses in the global memory and all local registers.

The operational semantics defines a transition relation between states. A state \( s = (pc, val, buf) \) consists of a program counter, a variable valuation, and some buffer content. The program counter \( pc : \text{THRD} \to \text{LAB} \) tracks for each thread the label of the instruction to be executed next. The variable valuation \( val : \text{VAR} \to \text{DOM} \) contains the value of each local register and the value of each address in the global memory. The buffer content \( \text{buf} = \text{buf}_1 \cup \text{buf}_2 \) is \( \text{buf}_1 : \text{THRD} \times \text{DOM} \to \text{DOM}^* \) and \( \text{buf}_2 : \text{THRD} \to (\text{DOM}^*)^* \). The first ones are the per-address buffers in each thread. The second are the all-addresses buffers. They contain the stores (as mappings from addresses to values in \( \text{DOM} \times \text{DOM} \)) and the fences (as sequences of addresses in \( \text{DOM}^* \)). The initial state is defined by \( s_0 := (pc_0, val_0, buf_0) \) with \( pc_0(t_i) := l_{0,i} \) for all \( t_i \in \text{THRD} \), \( val_0(x) := 0 \) for all \( x \in \text{VAR} \), and \( \text{buf}_1(t, a) := \varepsilon \), \( \text{buf}_2(t) := \varepsilon \) for all \( t \in \text{THRD} \), \( a \in \text{DOM} \). Here, we use \( \varepsilon \) for the empty word.

The transition rules are shown in Figure 3. They implement the behavior explained above. We use \( \downarrow \) for the projection of a sequence to a subset of its actions. Note that the transitions are labeled by actions from

\[
\text{ACT} := \text{THRD} \times ((\{\text{st}, \text{ld}\} \times \text{DOM}^2) \cup \{\text{isu}, \text{loc}, \text{scfence}\} \cup (\text{fence} \times \text{DOM}^*)).
\]

Every action contains its executing thread. An action can be a store or load annotated with an address and a value, an issue, local, or scfence action, or a fence action with a list of addresses. The isu action denotes the issue of a store or fence action. We use \( \text{isu}_a \) to refer to the issue that action \( a \) corresponds to.

A computation is a sequence of actions that describes a single execution of a program. The set of computations of program \( P \) is

\[
C(P) := \{ \tau \in \text{ACT}^* \mid s_0 \xrightarrow{\tau} s = (pc, val, buf) \text{ with } \forall t \in \text{THRD} : \forall a \in \text{DOM} . \text{buf}(t) = \varepsilon \land \text{buf}(t, a) = \varepsilon \}.
\]

It contains all sequences of actions following the transition relation starting at the initial state and ending at a state with empty buffers. The latter requirement does not restrict the program behavior. Buffers can always be emptied.
The rule allows for the execution of the fence command if the current thread’s buffers are empty. The order of executed stores and fences.

The all-addresses buffer and reflects its effect in the global memory. The early read rule deletes the oldest store from the all-addresses buffer.

Figure 3. Transition rules from state (pc, val, buf) with pc(t) = l and instruction l : instr; goto l’. Throughout the definition, we let pc’ := pc[t := l’]. The first three rules make sure that a read will get the value of the latest buffered store from the own thread, if any, and otherwise the value from memory. We call a read from one of the buffers an early read. The issue store rule puts a store into the thread’s per-address buffer. The advance buffer rule moves the oldest store from a per-address buffer to the all-addresses buffer. The store to memory rule deletes the oldest store from the all-addresses buffer and reflects its effect in the global memory. The scfence rule allows for the execution of the scfence command if the current thread’s buffers are empty. The issue fence rule allows for the execution of the fence command if the current thread’s per-address buffers for the given addresses are empty. The fence rule allows us to track the order of executed stores and fences.
B Happens-before Relations

The formal definition for the relations of happens-before is as follows: The program-order relation of a thread \( t \) is obtained by projecting computation \( \tau \) to the actions of this thread. For stores and fences that are subject to delays, what matters is the moment they are issued. The actual actions are also projected away, denoted by \( \text{not delayed} \):

\[
\rightarrow^t_{\text{po}} := \tau \downarrow (t, \text{not delayed}, \ast, \ast).
\]

The program-order relation of the program is then the union of the program orders relations of all threads,

\[
\rightarrow_{\text{po}} := \bigcup_{t \in P} \rightarrow^t_{\text{po}}.
\]

The store order is defined similarly. We first obtain the store order relation of each address \( a \) by projecting \( \tau \) to \((\ast, \text{st}, a, \ast)\). Then we define the store order of the program to be the union of all \( \rightarrow^a_{\text{st}} \).

The source relation is defined via the partial source function \( \text{src}_\tau \) that maps the load actions in \( \tau \) to the store actions in \( \tau \). The function returns the store that a load reads its value. If the function is undefined, the load reads the initial value. For \( \tau = \alpha \cdot \text{ld} \cdot \beta \) with \( \text{thread(ld)} = t \) and \( \text{addr(ld)} = a \), we define

\[
\text{src}_\tau(\text{ld}) := \begin{cases} 
  x, & \text{if } \alpha \downarrow \text{isu}_{(t, \text{st}, a, \ast)} \text{ in } \beta = \gamma \cdot \text{isu}_x \\
  y, & \text{if } \alpha \downarrow \text{isu}_{(t, \text{st}, a, \ast)} \text{ in } \beta = \varepsilon \land \alpha \downarrow (\ast, \text{st}, a, \ast) = \gamma \cdot y.
\end{cases}
\]

The first case looks for the latest suitable store of the same thread that is already issued but not yet stored. In this case, the load will perform an early read. If there is no such store, the second case looks for the latest suitable store on the global memory. With this, we have \( \text{src}_\tau(\text{ld}) \rightarrow_{\text{src}} \text{ld} \), provided \( \text{src}_\tau(\text{ld}) \) is defined.

The conflict relation is derived from \( \rightarrow_{\text{src}} \) and \( \rightarrow_{\text{st}} \). We have \( \text{ld} \rightarrow_{\text{cf}} \text{st} \), if there is a store \( \text{st}' \) with \( \text{st}' \rightarrow_{\text{src}} \text{ld} \) and \( \text{st}' \rightarrow_{\text{st}} \text{st} \). Moreover, we have \( \text{ld} \rightarrow_{\text{cf}} \text{st} \) if both access the same address, there is no \( \text{st}' \rightarrow_{\text{src}} \text{ld} \) and no \( \text{st}'' \rightarrow_{\text{st}} \text{st} \).

C Missing Proofs

To prove the dichotomy result, we first need to show a technical lemma. It gives information about the shape of the last action that has been overtaken by a store.

**Lemma 3.** In a minimal violation \( \tau = \tau_1 \cdot \text{isu}_{\text{st}} \cdot \tau_2 \cdot a \cdot \tau_3 \cdot \text{st} \cdot \tau_4 \in C(\mathcal{P}) \) with \( \text{thread(st)} = t = \text{thread(a)} \) and \( \tau_3 \downarrow t = \varepsilon \), action \( a \) is one of the following:

- a load of an address different from \( \text{addr(st)} \)
- a store
- a fence instruction that was issued before \( \text{isu}_{\text{st}} \).

**Proof.** We know that \( a \) is not an \textbf{scfence} instruction since \( \text{st} \) overtakes it. If \( a \) was a local or issue action, we could place it after \( \text{st} \) without changing the trace:
\[\tau' := \tau_1 \cdot \text{isu}_{\text{sc}} \cdot \tau_2 \cdot \tau_3 \cdot \text{st} \cdot \text{a} \cdot \tau_4 \] also is a violation. Since \(\text{delays}(\tau') < \text{delays}(\tau)\) we have \(\$(\tau') < \$(\tau)\). This contradicts minimality of \(\tau\).

If \(a\) was a load of \(\text{addr}(\text{st})\), we could as well place it after \(st\). We note that \(a\) performs an early read in \(\tau\). Since \(\tau_1 \downarrow \text{t}\) is empty, \(a\) reads from the same store in \(\tau\) and \(\tau'\). Therefore, the trace is preserved in this case, too. Again, \(\tau'\) has less delays than \(\tau\), which contradicts minimality of \(\tau\).

If \(a\) was a \text{fence} instruction that was issued within \(\tau_2\), then it could not contain \(\text{addr}(\text{st})\). Otherwise, the fence would have moved \(\text{st}\) to the all-addresses buffer and from there \(\text{st}\) would have hit the global memory before \(a\). This is due to the FIFO behavior of the buffer. Hence, the fence does not contain \(\text{addr}(\text{st})\).

This means we can place it after \(st\) to obtain the new computation \(\tau'\). As the delays for the fence increase by the same amount as they decrease for the store, \(\tau'\) has the same number of delays as \(\tau\). But \(\tau'\) saves one reordering of \(st\) over the fence. Therefore, we get a contradiction to minimality of \(\tau\). \(\Box\)

Proof (of Lemma 2). The lemma is equivalent to \(\neg (i) \implies (ii)\), which we prove by induction on the length of \(\tau_2\).

**Base case** If \(\text{length}(\tau_2) = 0\), we know that \(\tau = \tau_1 \cdot \text{a} \cdot \text{b} \cdot \tau_3\) and \(\neg \text{sc}_{\text{hb}} \text{b}\). If \(\text{thread}(a) = \text{thread}(b)\), then \(b \rightarrow_{p_0} a\). This means \(b\) is a store or a fence. Due to the overtime of \(b\), action \(a\) will not be an \text{scfence}. If \(a\) was an issue, a local assignment, or an assert, then we could save the overtime of \(b\) over \(a\). The resulting computation \(\tau'\) would still be violating but have a smaller cost than \(\tau\). A contradiction to minimality of \(\tau\). So \(a\) is a store, a load, or a \text{fence}. Assume \(b\) is a store. By FIFO, \(a\) is not a store to \(\text{addr}(b)\). Together with Lemma 3, we know that \(a\) is a load of an address or a store to an address different from \(\text{addr}(b)\). In both cases, we can swap \(a\) and \(b\) leading to a computation \(\tau'\) that has the same trace as \(\tau\) and therefore is a violation, too. But \(\tau'\) saves one delay (if \(a\) is a load) or one reordering while preserving the delays (if \(a\) is a store). This contradicts minimality of \(\tau\). Assume \(b\) is a \text{fence}. If \(a\) is a load, we can simply swap the commands. This saves a delay and leads to a contradiction to minimality. If \(a\) is a store or a fence, it would have entered the all-addresses buffer after the fence \(b\) and have left it earlier. This contradicts the FIFO order.

If \(\text{thread}(a) \neq \text{thread}(b)\), then we know from \(a \neq \text{sc}_{\text{hb}} b\) that \(a\) and \(b\) are not two load or store actions operating on the same address where at least one is a store. Therefore, we can swap \(a\) and \(b\) leading to a computation \(\tau'\) that has the same trace and per-thread-computations as \(\tau\). Since \(\tau_{22}\) is empty, there is nothing more to show.

**Step case** Assume the induction hypothesis holds for \(\text{length}(\tau_2) \leq n\). We consider a computation \(\tau = \tau_1 \cdot \text{a} \cdot \tau_2 \cdot \text{b} \cdot \tau_3\) with \(\text{length}(\tau_2) = n + 1\). Let \(\tau_2 = \tau_2' \cdot \text{c}\). Since \(a \neq \text{sc}_{\text{hb}} b\) through \(\tau_2\), we have \(a \neq \text{sc}_{\text{hb}} c\) through \(\tau_2'\) or \(c \neq \text{sc}_{\text{hb}} b\).

If \(a \neq \text{sc}_{\text{hb}} c\), then we can apply the induction hypothesis to \(\tau\) with respect to \(a\) and \(c\). This results in \(\tau'' = \tau_1 \cdot \tau_2' \cdot c \cdot \tau_2'' \cdot \text{b} \cdot \tau_3\). Applying the hypothesis again to \(\tau''\) with respect to \(a\) and \(b\) yields \(\tau''' = \tau_1 \cdot \tau_2' \cdot c \cdot \tau_2'' \cdot \text{b} \cdot \text{a} \cdot \tau_2'\). In both applications of the hypothesis the trace and the per-thread-computations are preserved. Furthermore, \(\tau_2'\) is a subsequence of \(\tau_2\) which is a subsequence of
There is a minimal violation \( \tau \). Assume the statement holds for length(\( \tau \)).

**Lemma 4 (Rear).** Consider a minimal violation \( \tau = \tau_1 \cdot a \cdot \tau_2 \cdot b \cdot \tau_3 \in C(\mathcal{P}) \) with \( a \rightarrow_{hb}^+ b \) through \( \tau_2 \) and \( b \rightarrow_{po}^- a \). Then \( b \cdot \tau_3 \) contains only delayed stores and fences and these actions respect program order.

**Proof.** Towards a contradiction, assume \( b \cdot \tau_3 \) contains further actions. We project \( b \cdot \tau_3 \) to the stores and fences issued in \( \tau_1 \cdot a \cdot \tau_2 \). The projection will keep \( b \) as it was issued before \( a \). Hence, the resulting computation \( \tau' \) preserves the happens-before cycle between \( a \) and \( b \) and therefore is a violation, too. Furthermore, \( \tau' \) is still a valid computation as we did not remove program-order-intermediate actions and there are no failing assertions after \( \tau_2 \). Removing actions does not increase the delays or reorderings, but it reduces the length. As \( \delta(\tau') < \delta(\tau) \), we have a contradiction to minimality of \( \tau \).

If \( b \cdot \tau_3 = a \cdot x \cdot \beta \cdot y \cdot \gamma \) with \( y \rightarrow_{po}^+ x \), we can rearrange all actions to appear in program order. Bringing actions in program order will not violate FIFO or fence restrictions. It might change the store order but it does not affect the happens-before cycle between \( a \) and \( b \). If \( b \) is moved behind program-order-earlier stores and fences of the same thread in \( \tau_3 \), the cycle remains. The reason is that the happens-before-through relation is stable under insertion of actions. Rearranging the stores and fences does not change the number of delays, but saves at least the reordering of \( y \) over \( x \). This contradicts minimality of \( \tau \).

The following normalization lemma shows that, given an action, one can remove all successors that are independent of this action. To be more precise, we move the independent successors to the left of the given action. Technically, we apply Lemma 2 to construct a new computation where the independent successors execute earlier.

**Lemma 5 (Dependence).** Let \( \tau = \alpha \cdot a \cdot \beta \cdot \gamma \in C(\mathcal{P}) \) be a minimal violation. There is a minimal violation \( \tau' = \alpha \cdot \beta' \cdot a \cdot \beta'' \cdot \gamma \in C(\mathcal{P}) \) where \( \text{Tr}(\tau') = \text{Tr}(\tau) \), \( \tau' \downarrow t = \tau \downarrow t \) for all threads \( t \), \( \beta'' \) a subsequence of \( \beta \), and where

for every action \( b \) in \( \beta'' \) we have \( a \rightarrow_{hb}^+ b \) through the part in between.

**Proof.** We proceed by induction on the length of \( \beta \). The base case of an empty sequence is trivial. Assume the statement holds for length(\( \beta \)) \leq n and consider a computation \( \tau = \alpha \cdot a \cdot \beta \cdot \gamma \) with length(\( \beta \)) = \( n + 1 \). If every action in \( \beta \) is
happens-before-through dependent on $a$, then $\tau' := \tau$ satisfies the requirements. Otherwise, we take the first action $b$ in $\beta$ so that $\tau = \alpha \cdot a \cdot \beta_1 \cdot b \cdot \beta_2 \cdot \gamma$ and $a \not\rightarrow^{+} b$ through $\beta_1$. An application of Lemma 2 gives a computation $\tau' = \alpha \cdot \beta_{11} \cdot b \cdot a \cdot \beta_{12} \cdot \beta_2 \cdot \gamma$ with the same trace and per-thread-computations as $\tau$ and $\beta_{12}$ being a subsequence of $\beta_1$. Since $\text{length}(\beta_{12} \cdot \beta_2) < \text{length}(\beta)$ (we took out $b$), we can now apply the induction hypothesis to $\tau'$. It gives another computation $\tau'' = \alpha \cdot \beta_{11} \cdot b \cdot a \cdot \beta_{12} \cdot \beta_2 \cdot \gamma$ with the same trace and per-thread-computations as $\tau$ and $\beta_{12}$ being a subsequence of $\beta_1 \cdot \beta_2$. As $\beta_{12}$ is a subsequence of $\beta_1$ and $\beta_1 \cdot \beta_2$ is a subsequence of $\beta$, we conclude that $(\beta_{12} \cdot \beta_2)''$ is a subsequence of $\beta$. As Lemma 2 and the induction hypothesis preserve the per-thread-computations and the trace, the corresponding equalities are fulfilled, too. The dependency requirement directly follows from the induction hypothesis. 

C.1 Locality

Proof (of Theorem 1).

If the program admits violations, then there is one that is local in the sense that only one thread delays actions. Towards a contradiction, we assume that in all violations at least two threads delay actions. (If no thread delays actions, the computation is SC.) Among these violations, let $\tau$ be a minimal one. We define:

- $y :=$ last isu or load action that has been overtaken by a store
- $st_y :=$ earliest store that overtook $y$
- $t_y := \text{thread}(y) (= \text{thread}(st_y))$
- $x :=$ last isu or load from a thread $t_x \neq t_y$ that has been overtaken by a store
- $st_x :=$ earliest store that overtook $x$.

Lemma 6. $x$, $y$, $st_x$, and $st_y$ exist.

We defer the proof of the lemma for the moment. Given $y$, $x$, $st_y$, and $st_x$, the computation takes one of the following forms (for some $\tau_1, \ldots, \tau_5 \in \text{ACT}^*$):

1. $\tau = \tau_1 \cdot x \cdot \tau_2 \cdot st_x \cdot \tau_3 \cdot y \cdot \tau_4 \cdot st_y \cdot \tau_5$
2. $\tau = \tau_1 \cdot x \cdot \tau_2 \cdot y \cdot \tau_3 \cdot st_y \cdot \tau_4 \cdot st_x \cdot \tau_5$
3. $\tau = \tau_1 \cdot x \cdot \tau_2 \cdot y \cdot \tau_3 \cdot st_x \cdot \tau_4 \cdot st_y \cdot \tau_5$.

The task is to show that each of the forms yields a contradiction.

Form [1]: We apply Proposition [1] to $x$ and $st_x$ and get a happens-before cycle within $\tau_1 \cdot x \cdot \tau_2 \cdot st_x$. By Lemma [4] the part starting with $st_x$ consists of stores and fences only. This contradicts the fact that $y$ is an isu or a load.

Form [2]: With Proposition [1], we get a happens-before cycle within $\tau_1 \cdot x \cdot \tau_2 \cdot y \cdot \tau_3 \cdot st_x$. By Lemma [4] the part after $st_x$ consists of delayed stores and
fences only. Proposition 11 yields a happens-before chain from $x$ to $st_x$. We can rearrange the computation as follows:

$$\tau' = \tau_1 \cdot x \cdot \tau_2 \cdot y \cdot \tau_3 \cdot (\tau_4 \downarrow t_y) \cdot st_y \cdot st_x \cdot (\tau_4 \downarrow \text{rest}) \cdot \tau_5 .$$

The happens-before chain is still present as the relation is stable under insertion. As we did not change the per-thread computations, $\tau'$ is a minimal violation, too. It has Form (2), which yields a contradiction as we will show next.

**Form (2):** We will show that there are two happens-before cycles, one between $x$ and $st_x$, the other between $y$ and $st_y$. The ultimate goal is to move $st_y$ back over $y$ to save one delay. We can do this in such a way that there remains a happens-before cycle between $x$ and $st_x$. The resulting computation is therefore a violation with less delays, which contradicts minimality of $\tau$.

By Corollary 11, we have $y \rightarrow_{hb}^+ st_y$ through $\tau_3$. With this, Lemma 4 applies and shows that $\tau_4 \cdot st_x \cdot \tau_5$ only consists of delayed stores and fences.

We apply Lemma 5 to $\tau_3$ and obtain

$$\tau' := \tau_1 \cdot x \cdot \tau_2 \cdot \tau_3 \cdot y \cdot \tau_4 \cdot st_y \cdot \tau_5 .$$

Computation $\tau'$ is again a minimal violation. It is a violation as we do not change the trace. It is minimal as we do not change the per-thread computations, and the delays and reorders are counted per thread.

By Lemma 5 every action in $\tau_3''$ is happens-before-through dependent on action $y$. By Proposition 1 we moreover have $y \rightarrow_{hb}^+ st_y$ through $\tau_3''$. This means, we find an access to $\text{addr}(st_y)$ in $\tau_3''$. Let acc be the first such access and let $\tau_3'' = \tau_3'' \cdot acc \cdot \tau_3''$. We move $st_y$ over $\tau_3''$. Since the store cannot be moved over fences due to the FIFO all-addresses buffer, we obtain the computation

$$\tau'' := \tau_1 \cdot x \cdot \tau_2 \cdot \tau_3 \cdot y \cdot \tau_3'' \cdot \tau_4 \cdot (\tau_3'' \downarrow \text{fences of } t_y) \cdot st_y \cdot (\tau_3'' \downarrow \text{delayed}) \cdot \tau_4 \cdot st_x \cdot \tau_5 .$$

Here, $\tau_3'' \downarrow \text{delayed}$ is the projection of $\tau_3''$ to the delayed stores and fences (of threads different from $t_y$). Computation $\tau''$ is executable, i.e., in the set of computations of the program. Indeed, starting from acc it does not contain any assertions that could fail. The assertions before acc continue to hold as $\tau'$ was executable. Computation $\tau''$ is a violation due to the cycle $y \rightarrow_{hb}^+ acc \rightarrow_{ct/sh} st_y \rightarrow_{po}^+ y$. It is minimal as we do not change the computation of thread $t_y$ and potentially only remove delays or reorders from the computations of the other threads. Actually, there is no removal. As we started from a minimal violation, we get that $\tau_3'' \downarrow \text{delayed}$ has to be all of $\tau_3''$ except for the fences of $t_y$.

Applying Corollary 11 we get $x$ happens before $st_x$ through

$$\tau_2 \cdot \tau_3 \cdot y \cdot \tau_3'' \cdot acc \cdot (\tau_3'' \downarrow \text{fences of } t_y) \cdot st_y \cdot (\tau_3'' \downarrow \text{delayed}) \cdot \tau_4 .$$

Our goal is to move $st_y$ before $y$ in order to save a delay. This move should preserve the relation $x \rightarrow_{hb}^+ st_x$ through 11. Moving $st_y$ also moves all fences of
The isu path. The isust forward. An application of Corollary 1 gives isust delicate. In this case, the full computation is issued in By Lemma 3, a store st. Let the last action overtaken by st be that delays actions. With the previous reasoning, the thread delay s at least one of the computation. A contradiction to minimality of \( \tau \). These actions can be dropped without changing the trace while reducing the cost thus delayed over loads, local actions, and issues only. Overtakes of fences over due to the FIFO property that forbids reorderings among fences. The fence is delayed fence, as we took the first one, and there cannot be a non-delayed fence. Furthermore, the fence cannot be delayed over other fences. There is no earlier force the stores to be delayed with the fence, but there are no delayed stores. The FIFO property of the all-addresses buffer would and the thread only delays fences. Take the first fence that gets delayed. It is that delays actions will in particular delay stores. Assume this is not the case. To argue for the existence, we first show that each thread Proof (of Lemma 6). To argue for the existence, we first show that each thread

\[
\tau''' := \tau_1 \cdot x \cdot \tau_2 \cdot \tau_3' \cdot (\tau_3'' \downarrow \text{fences of } t_y) \cdot \text{st}_y \cdot y \cdot (\tau_3'' \downarrow \text{rest}) \cdot \text{acc} \cdot (\tau_3'' \downarrow \text{delayed}) \cdot \tau_4 \cdot \text{st}_x \cdot \tau_5.
\]

The computation is executable because \( \tau_3'' \downarrow \text{rest} \) does not contain an access to addr(st_y). This is due to the choice of acc as the first access to the address.

It remains to show that \( x \rightarrow_{hb}^+ \text{st}_x \) through (3) still holds. If \( \text{st}_y \) is not on this happens-before-through chain, we are done. If the chain contains \( \text{st}_y \), we have that \( x \rightarrow_{hb}^+ a \rightarrow_{po+cf/st} \text{st}_y \rightarrow_{st} \text{st} \rightarrow_{st}^* \text{st}_x \) for some actions \( a \) and \( \text{st} \) in \( (3) \) st_x (st can be \( \text{st}_x \)). If we have a program-order dependence from \( a \) to \( \text{st}_y \), this is not changed by moving \( \text{st}_y \) back over \( y \). Computation \( \tau''' \) contains the chain \( x \rightarrow_{hb}^+ a \rightarrow_{po}^+ \text{st}_y \rightarrow_{src/st} \text{acc} \rightarrow_{cf/st} \text{st} \rightarrow_{st}^* \text{st}_x \). Indeed, as \( y \) is chosen to be a load or an issue, we know that action \( a \) (which is program-order earlier than \( \text{st}_y \)) has to lie before \( y \) in (4). If we have a conflict or a store dependence from \( a \) to \( \text{st}_y \), we know that \( a = \text{acc} \). In this case, \( \tau''' \) contains the chain \( x \rightarrow_{hb}^+ \text{acc} \rightarrow_{cf/st} \text{st} \rightarrow_{st}^* \text{st}_x \). Therefore, \( \tau''' \) contains the cycle \( x \rightarrow_{hb}^+ \text{st}_x \rightarrow_{po}^+ x \) and thus is a violation. As the rearrangement saves one delay of \( y \), \( \tau''' \) contradicts minimality of \( \tau'' \). □

Proof (of Lemma 3). To argue for the existence, we first show that each thread that delays actions work in particular delay stores. Assume this is not the case and the thread only delays fences. Take the first fence that gets delayed. It is not delayed over stores. The FIFO property of the all-addresses buffer would force the stores to be delayed with the fence, but there are no delayed stores. Furthermore, the fence cannot be delayed over other fences. There is no earlier delayed fence, as we took the first one, and there cannot be a non-delayed fence due to the FIFO property that forbids reorderings among fences. The fence is thus delayed over loads, local actions, and issues only. Overtakes of fences over these actions can be dropped without changing the trace while reducing the cost of the computation. A contradiction to minimality of \( \tau \).

To find the required \( y \) and \( \text{st}_y \) and \( x \) with \( \text{st}_x \), we project \( \tau \) to a thread \( t \) that delays actions. With the previous reasoning, the thread delays at least one store \( \text{st} \). Let the last action overtaken by \( \text{st} \) be \( a \). We thus have

\[
\tau \downarrow t = \tau_1 \cdot \text{isust} \cdot \tau_2 \cdot a \cdot \text{st} \cdot \tau_3 \quad \text{for some } \tau_1, \tau_2, \tau_3 \in \text{ACT}^*.
\]

By Lemma 3, \( a \) can be a load, a store, or a fence. In case of a load or a store issued in \( \tau_2 \), we are done. If \( a \) is a store issued in \( \tau_1 = \tau_1 a \cdot \text{isust} \cdot \tau_1b \), then \( \text{isust} \) is an issue action overtaken by the store \( a \). If \( a \) is a fence, the situation is more delicate. In this case, the full computation is

\[
\tau = \tau_1 \cdot \text{isufence} \cdot \tau_2 \cdot \text{isust} \cdot \tau_3 \cdot \text{fence} \cdot \tau_4 \cdot \text{st} \cdot \tau_5 \quad \text{for some } \tau_1, \ldots, \tau_5 \in \text{ACT}^*.
\]

An application of Corollary 1 gives \( \text{isust} \rightarrow_{hb}^+ \) fence through \( \tau_3 \). As there is no forward \( \rightarrow_{po}^+ \) relation from \( \text{isust} \) to fence, we will find actions of thread \( t \) on this path. The \( \text{isust} \) action can only have an outgoing \( \rightarrow_{po} \) dependence to a local, a
load, or an issue action in \( \tau_3 \). The load or the issue would serve as the required action overtaken by \( st \). For the local action, the same reasoning applies. Since we eventually need a \( \rightarrow_{cl} \) or \( \rightarrow_{cl} \) dependence to form a happens-before-through chain, and since local actions have no such outgoing dependencies, we are sure to find a load or an issue.

\[ \tau = \tau_1 \cdot \text{isu}_{st} \cdot \tau_2 \cdot a \cdot \tau_3 \cdot st \cdot \tau_4 \]

with \( \tau_3 \downarrow t_A = \varepsilon \). By Lemma 3, \( a \) is a load, a store, or a fence action that was issued in \( \tau_1 \). The latter one is not possible as \( st \) is the first action that was delayed. Therefore, \( a \) is either a load or a store issued in \( \tau_2 \) and we have \( st \rightarrow_{po} a \). With Corollary 1, we get \( a \rightarrow_{hb} st \) through \( \tau_3 \). Altogether, there is the happens-before cycle \( st \rightarrow_{po} a \rightarrow_{hb} st \). Lemma 4 ensures that \( \tau_4 \) consists of landing stores and fences only. As \( t_A \) is the only thread delaying actions, \( \tau_4 \) solely contains actions of thread \( t_A \).

We can show that \( \tau_2 \cdot a \) does not contain delayed actions. Towards a contradiction, assume there is a first action \( x \) in \( \tau_2 \cdot a \) that is delayed over the last action \( b \). As \( st \) is the first action that gets delayed, \( x \) is issued in \( \tau_2 \). We have \( \tau_2 \cdot a = \alpha \cdot \text{isu}_x \cdot \beta \cdot b \cdot \gamma \cdot x \cdot \delta \) with thread(\( b \)) = thread(\( x \)) = \( t_A \) and \( \gamma \downarrow t_A = \varepsilon \). We know that \( x \) has to be a store. If it was a delayed fence, we argue that we could drop a delay of \( x \). If \( b \) was a store or fence action, then it was not delayed as \( x \) is the first delayed action. This implies a reordering between \( x \) and \( b \). Reorderings between fences as well as reordering a later issued store before an earlier issued fence is not possible due to the FIFO property of the all-addresses buffer. In the remaining cases, \( b \) being an issue, local, or load action, we can drop the delay of \( x \) over \( b \), which again contradicts minimality of \( \tau \).

By Lemma 3, \( b \) is either a load, a store, or a fence issued before \( \text{isu}_x \). The latter fence is not possible as the only delayed action earlier than \( x \) is \( x \). With the same argument, we know that \( b \) will be issued in \( \beta \) if it is a store. Corollary 1 yields the cycle \( b \rightarrow_{hb} x \rightarrow_{po} b \). Applying Lemma 4, we know that the actions starting with \( x \) have to respect program order, in particular \( x \rightarrow_{po} st \). But \( x \) is issued after \( \text{isu}_x \), which contradicts that order.

Furthermore, we can assume that for every action \( c \) in \( \tau_3 \cdot st \) we have \( a \rightarrow_{hb} c \). If this is not the case, we can apply Lemma 5 to get a minimal violation that fulfills that property.

\( \Box \)

### C.2 Singularity

**Proof (of Proposition 3).** Towards a contradiction, assume there is such a computation and let \( t := \text{thread}(st_1) = \text{thread}(st_2) \). We have \( st_1 \rightarrow_{po} st_2 \), for otherwise
Lemma 7. All stores in \((\tau''')_{1b2} \downarrow t\) \cdot st_1 \cdot st_2 are to the address \(\text{addr}(acc)\).

With this result, we can move \(st_1\) before \(\text{isust}_2\) while preserving the cycle:

\[
\tau'' := \tau_{1a} \cdot \tau'_{1b} \cdot (\tau''')_{1b2} \downarrow t \cdot st_1 \cdot \text{isust}_2 \cdot \tau''_{1b1} \cdot acc \cdot st_2 \cdot (\tau''')_{1b2} \downarrow rest \cdot \tau_2 .
\]

Since there is no assertion after \(acc\) and \(acc\) is the only action that could have loaded a different value, the computation is executable. It still contains the cycle \(\text{isust}_2 \rightarrow^+_{\text{hb}} acc \rightarrow_{\text{cf/st}} st_2\). A contradiction to minimality of \(\tau''\).

Proof (of Lemma 7). We look at \((\tau''')_{1b2} \downarrow t\) \cdot st_1 first. Assume this part contains a store to a different address and take the first one. By the choice of \(acc\), \(\tau''_{1b1}\) does not contain an access by another thread to that address. We can place the store directly before \(\text{isust}_2\). The resulting computation is still executable, has the same trace, and saves one delay (over \(\text{isust}_2\)). This contradicts minimality of \(\tau''\).

Now we look at \(st_2\). Assume it is to an address different from \(\text{addr}(acc)\). If there is a first access \(acc_2\) of another thread to \(\text{addr}(st_2)\) in \(\tau''_{1b1} = \tau''_{1b1a} \cdot acc_2 \cdot \tau''_{1b1b}\), we could swap the stores violating minimality of \(\tau\). Action \(st_2\) is issued in \(\tau_{1a}\), say \(\tau_{1a} = \tau_{1a} \cdot \text{isust}_2 \cdot \tau_{1b}\). The overall strategy will be to move \(st_1\) back over \(\text{isust}_2\).

We find the first action \(acc'\) that is (i) before \(st_1\) in the relation \(\rightarrow_{\text{cf/st}} \rightarrow_{po}^+\) and (ii) placed on an \(\text{isust}_2 \rightarrow_{\text{hb}} st_1\) chain through \(\tau_{1b}\). Intuitively, action \(acc'\) is from another thread \((\rightarrow_{\text{cf/st}})\) and accesses an address that leads to a program-order dependence \((\rightarrow_{po})\). Technically, we first apply Lemma 5 to \(\tau_{1b}\) and get

\[
\tau' = \tau_{1a} \cdot \tau'_{1b} \cdot \text{isust}_2 \cdot \tau''_{1b} \cdot st_1 \cdot st_2 \cdot \tau_2 .
\]

By Corollary 1 we have \(\text{isust}_2 \rightarrow_{\text{hb}}^+ st_1\) through \(\tau_{1b}''\). This path contains an access \(acc'\) with (1) \(\text{isust}_2 \rightarrow_{\text{hb}}^+ acc' \rightarrow_{\text{cf/st}} st_1\) or (2) \(\text{isust}_2 \rightarrow_{\text{hb}}^+ acc' \rightarrow_{\text{cf/st}} st' \rightarrow_{po}^+ st_1\), respectively.

Looking at the second case, \(st'\) really has to be a store since there are only stores in \(\tau_{1b}''\) that are program-order-earlier than \(st_1\).

We are interested in the first access to \(addr(acc')\). To be precise, we consider all possible choices for \(acc'.\) For each \(acc',\) we find the first access \(acc\) to \(\text{addr}(acc')\) in \(\tau'' = \tau''_{1b1} \cdot acc \cdot \tau''_{1b2}\). Among all possible \(acc\), we take the first one.

We place all interesting actions together:

\[
\tau'' := \tau_{1a} \cdot \tau'_{1b} \cdot \text{isust}_2 \cdot \tau''_{1b1} \cdot acc \cdot (\tau''_{1b2} \downarrow t) \cdot st_1 \cdot st_2 \cdot (\tau''_{1b2} \downarrow rest) \cdot \tau_2 .
\]

Assume we projected the part after \(acc\) to landing stores. Then it is easy to see that \(\tau''\) is executable and has the same per-thread-computations as \(\tau'\) or even less delays. We have \(\text{isust}_2 \rightarrow_{\text{hb}}^+ acc, (1) acc \rightarrow_{\text{cf/st}} st_1\) respectively (2) \(acc \rightarrow_{\text{cf/st}} st' \rightarrow_{po}^+ st_1,\) and \(st_1 \rightarrow_{po}^+ st_2\). Because of this happens-before cycle, \(\tau''\) is a minimal violation. Minimality of \(\tau''\) ensures that the assumed projection was not necessary, since the part in question did not contain any non-store action. The stores after \(acc\) are consistent with the program order as rearranging the stores would keep the cycle and save some reorderings.

To conclude the argumentation, we rely on the following lemma, the proof of which we defer for the moment.

Lemma 7. All stores in \((\tau''')_{1b2} \downarrow t\) \cdot st_1 \cdot st_2 are to the address \(\text{addr}(acc)\).
we can use this access to have a cycle in a rearranged computation with less delays: \( \tau_{1a} \cdot \tau'_{1b} \cdot (\tau'_{1b2} \downarrow t) \cdot \text{st}_1 \cdot \text{isu}_{st2} \cdot \tau''_{1b1a} \cdot \text{acc}_2 \cdot \text{st}_2 \cdot \ldots \) (append the remaining actions in the order they appear in \( \tau'' \) and project them to landing stores). Here we have isu_{st2} \rightarrow_{hb} \text{acc}_2 \rightarrow_{ct/st} \text{st}_2. \) So there is no such access acc_2.

We can place action st_2 directly after isu_{st2} without changing the trace. If \( \tau''_{1b1} \) contains an action of t that is not a delayed store, this already contradicts minimality of \( \tau'' \) as we save delays. We show that isu_{st2} \rightarrow_{hb} \text{acc} through \( \tau''_{1b1} \) implies the existence of such a not-delayed-store. The path begins with isu_{st2} and has to switch to acc somewhere. The outgoing relation of an issue can only be program order. Only load and store actions create conflict or store dependencies to acc. Because of the program order, such a store would not be delayed. \( \square \)

\section{Details of the Instrumentation}

\subsection{Instrumentation of the Attacker for Locality}

To begin with, we give the instrumentation of the attacker. For a precise definition, let \( t_A \) declare registers \( r^* \), have initial location \( l_0 \), and define instructions \( \langle \text{linst} \rangle^* \) that contain \( \text{stinst} \) and \( \text{lastinst} \) from the attack. The instrumentation is

\[ [[t_A]] := \text{thread } t_A \text{ regs } r^*, r_{stA}, r_{ence} \text{ init } l_0 \]

\[ \begin{array}{c}
\text{begin } \langle \text{linst} \rangle^* [\text{stinst}]_{A1} [\text{lastinst}]_{A2} [\langle \text{linst} \rangle]_{A3} \text{ wait end}
\end{array} \]

where the functions are defined in Figure 4.

\subsection{Optimized Instrumentation of the Attacker for Singularity}

The optimized translation for singularity is

\[ [[t_A]] := \text{thread } t_A \text{ regs } r^*, r_{stA}, r_{delayval} \text{ init } l_0 \]

\[ \begin{array}{c}
\text{begin } \langle \text{linst} \rangle^* [\text{stinst}]_{A1} [\text{lastinst}]_{A2} [\langle \text{linst} \rangle]_{A3} \text{ wait end}
\end{array} \]

where the functions are defined in Figure 5.

\subsection{Instrumentation of Helpers}

The instrumentation of helpers is taken from [13]. We recall it here for completeness. Initially, a helper executes its actions normally. When the hb flag is set by the attacker, the helper executes only actions that are hb-dependent on \( a \). To decide whether an action is hb-dependent on \( a \), we use the following observation from [13]. We have to track the maximal so-called access level for each address, in the order

\[ \text{no access < load access < store access}. \]
So if an address $y$ has seen a load but no store, we will keep the value \textit{load access} in $(y, hb)$. If the address has also seen a store, we keep \textit{store access} in $(y, hb)$, even if there have been later loads. The point is that the store is guaranteed to construct a dependency with further actions, while a load will only construct a conflict with subsequent stores.

For the formal definition, let the helper thread $t$ declare registers $r^*$, have initial label $l_0$, and define instructions $(\text{linst})^*$. The instrumented thread is

$$[t] := \text{thread} \hat{t} \text{regs} \hat{r}, r^* \text{init} l_0$$

$$\begin{array}{l}
\text{begin} \langle (\text{linst}) \rangle_{t0} \langle (\text{ldstinst}) \rangle_{t1} \langle (\text{linst}) \rangle_{t2} \text{end},
\end{array}$$

where the functions are defined in Figure 6.

\section*{E Evaluation}

We have implemented our instrumentation on top of Trencher \textsuperscript{[13]} and run the resulting tool on a set of example programs. Figure 7 shows the evaluation with partial-order reduction and liveness-based optimization. Figure 8 shows the evaluation with the optimizations turned-off. The tables show how many threads, labels, and instructions the programs have, whether or not they were detected as robust, and the number of visited states for the singularity-based and locality-based analysis. The time for the SC-reachability analysis was negligible ($< 8$ seconds) in all examples.

Depending on the input program, singularity cuts down the search space to a third as compared with locality (Dekker: From 121 states with locality only 43 remain with singularity). More importantly, this is the first (and complete) robustness analysis for PGAS programs.
\[ l_1: \text{mem}[e_1] \leftarrow e_2; \text{goto } l_2; \text{A}_1 := l_1: \text{mem}[(e_1, d)] \leftarrow (e_2, d); \text{goto } \bar{l}_x; \]

\[ l_x: r_{\text{stk}} \leftarrow e_1; \text{goto } \bar{l}_2; \]

\[ l_1: r \leftarrow \text{mem}[e]; \text{goto } l_2; \text{A}_2 := l_1: \text{assert mem}[(e, d)] = 0; \text{goto } \bar{l}_{x_1}; \]

\[ \bar{l}_{x_1}: \text{mem}[hb] \leftarrow \text{true}; \text{goto } \bar{l}_{x_2}; \]

\[ \bar{l}_{x_2}: \text{mem}[(e, hb)] \leftarrow \text{lda}; \text{goto } \bar{l}_{\text{wait}}; \]

\[ l_1: \text{mem}[e_1] \leftarrow e_2; \text{goto } l_2; \text{A}_2 := l_1: \text{assert } r_{\text{fence}} = 0; \text{goto } \bar{l}_{x_1}; \]

\[ \bar{l}_{x_1}: \text{assert mem}[(e_1, d)] = 0; \text{goto } \bar{l}_{x_2}; \]

\[ \bar{l}_{x_2}: \text{mem}[e_1] \leftarrow e_2; \text{goto } \bar{l}_{x_3}; \]

\[ \bar{l}_{x_3}: \text{mem}[hb] \leftarrow \text{true}; \text{goto } \bar{l}_{x_4}; \]

\[ \bar{l}_{x_4}: \text{mem}[(e_1, hb)] \leftarrow \text{sta}; \text{goto } \bar{l}_{\text{wait}}; \]

\[ l_1: \text{mem}[e_1] \leftarrow e_2; \text{goto } l_2; \text{A}_3 := l_1: \text{assert } r_{\text{fence}} = 0; \text{goto } \bar{l}_{x_1}; \]

\[ \bar{l}_{x_1}: \text{assert mem}[(e_1, d)] = 0; \text{goto } \bar{l}_{x_2}; \]

\[ \bar{l}_{x_2}: \text{mem}[e_1] \leftarrow e_2; \text{goto } \bar{l}_2; \]

\[ \bar{l}_2: \text{mem}[(e_1, d)] \leftarrow (e_2, d); \text{goto } \bar{l}_2; \]

\[ l_1: r \leftarrow \text{mem}[e]; \text{goto } l_2; \text{A}_3 := l_1: \text{assert mem}[(e, d)] = 0; \text{goto } \bar{l}_{x_1}; \]

\[ \bar{l}_{x_1}: r \leftarrow \text{mem}[e]; \text{goto } \bar{l}_2; \]

\[ \bar{l}_2: \text{assert mem}[(e, d)] \neq 0; \text{goto } \bar{l}_{x_2}; \]

\[ \bar{l}_{x_2}: (r, d) \leftarrow \text{mem}[(e, d)]; \text{goto } \bar{l}_2; \]

\[ l_1: \text{local}; \text{goto } l_2; \text{A}_3 := l_1: \text{local}; \text{goto } \bar{l}_2; \]

\[ l_1: \text{scfence}; \text{goto } l_2; \text{A}_3 := \]

\[ l_1: \text{fence}_{a_1 \ldots a_n}; \text{goto } l_2; \text{A}_3 := l_1: \text{fence} \leftarrow \text{true}; \text{goto } \bar{l}_2; \]

\[ \bar{l}_1: \text{assert mem}[(a_1, d)] = 0; \text{goto } \bar{l}_{x_2}; \]

\[ \bar{l}_{x_2}: \text{assert mem}[(a_2, d)] = 0; \text{goto } \bar{l}_{x_3}; \]

\[ \vdots \]

\[ \bar{l}_{x(n-1)}: \text{assert mem}[(a_{n-1}, d)] = 0; \text{goto } \bar{l}_{x_n}; \]

\[ \bar{l}_{x_n}: \text{assert mem}[(a_n, d)] = 0; \text{goto } \bar{l}_2; \]

\[ \text{wait} := \bar{l}_{\text{wait}}: \text{assert mem}[(r_{\text{stk}}, hb)] \neq 0; \text{goto } \bar{l}_{x_1}; \]

\[ \bar{l}_{x_1}: \text{mem}[\text{suc}] \leftarrow \text{true}; \text{goto } \bar{l}_{x_2}; \]

**Figure 4.** Instrumentation of the attacker for locality.
\[ l_1: \text{mem}[e_1] \leftarrow e_2; \text{goto } l_2; \] \[ A_1 := l_1: r_{\text{delayval}} \leftarrow e_2; \text{goto } l_r; \] \[ (14) \]

\[ l_1: r \leftarrow \text{mem}[e]; \text{goto } l_2; \] \[ A_2 := l_1: \text{assert } r_{\text{last}} \neq e; \text{goto } l_{\text{r1}}; \] \[ l_{\text{r1}}: \text{mem}[\text{hb}] \leftarrow \text{true}; \text{goto } l_{\text{r2}}; \] \[ l_{\text{r2}}: \text{mem}[(e, \text{hb})] \leftarrow \text{lda}; \text{goto } l_{\text{wait}}; \] \[ (15) \]

\[ l_1: \text{mem}[e] \leftarrow e_2; \text{goto } l_2; \] \[ A_3 := l_1: \text{assert } r_{\text{last}} \neq e_1; \text{goto } l_{\text{r1}}; \] \[ l_{\text{r1}}: \text{mem}[e_1] \leftarrow e_2; \text{goto } l_{\text{r2}}; \] \[ l_{\text{r2}}: \text{mem}[\text{hb}] \leftarrow \text{true}; \text{goto } l_{\text{r3}}; \] \[ l_{\text{r3}}: \text{mem}[(e_1, \text{hb})] \leftarrow \text{sta}; \text{goto } l_{\text{wait}}; \] \[ (16) \]

\[ l_1: \text{mem}[e] \leftarrow e_2; \text{goto } l_2; \] \[ A_3 := l_1: \text{assert } r_{\text{last}} \neq e_1; \text{goto } l_{\text{r1}}; \] \[ l_{\text{r1}}: r \leftarrow \text{mem}[e]; \text{goto } l_2; \] \[ l_1: \text{assert } r_{\text{last}} = e; \text{goto } l_{\text{r2}}; \] \[ l_{\text{r2}}: r \leftarrow r_{\text{delayval}}; \text{goto } l_2; \] \[ (17) \]

\[ l: \text{local}; \text{goto } l_2; \] \[ A_3 := l: \text{local}; \text{goto } l_2; \] \[ (18) \]

\[ l: \text{scfence}; \text{goto } l_2; \] \[ A_3 := l: \text{local}; \text{goto } l_2; \] \[ (19) \]

\[ l: \text{scfence}; \text{goto } l_2; \] \[ A_3 := \text{wait} := l_{\text{wait}}: \text{assert } \text{mem}[(r_{\text{last}}, \text{hb})] \neq 0; \text{goto } l_{\text{r1}}; \] \[ l_{\text{r1}}: \text{mem}[\text{suc}] \leftarrow \text{true}; \text{goto } l_{\text{r2}}; \] \[ (20) \]

**Figure 5.** Optimized instrumentation of the attacker for singularity.
[l₁: instr; goto l₂]; l₀ := l₁: assert mem[hb] = 0; goto l₁;
  l₁: instr; goto l₂;

[l₁: r ← mem[e]; goto l₂]; l₁ := l₁: assert mem[(e, hb)] = sta; goto l₁;
  l₁: r ← mem[e]; goto l₂;

[l₁: mem[e₁] ← e₂; goto l₂]; l₁ := l₁: assert mem[(e₁, hb)] ≥ lda; goto l₁;
  l₁₁: mem[e₁₁] ← e₁₂; goto l₁₂;
  l₁₂: mem[(e₁₁, hb)] ← sta; goto l₁₂;

[l₁: local/scfence/fence; goto l₂]; l₂ := l₁: local/scfence/fence; goto l₂;

[l₁: mem[e₁] ← e₂; goto l₂]; l₂ := l₁: mem[e₁] ← e₂; goto l₁;
  l₁₁: mem[(e₁, hb)] ← sta; goto l₁₂;

[l₁: r ← mem[e]; goto l₂]; l₂ := l₁: r ← mem[e]; goto l₁;
  l₁₁: r ← mem[e]; goto l₁₂;
  l₁₂: mem[(e, hb)] ← max{lda, mem[(e, hb)]}; goto l₁₂;

Figure 6. Instrumentation of helpers.

| Program                        | T | L | I | Robust? | Visited States (Singularity) | Visited States (Locality) |
|--------------------------------|---|---|---|---------|------------------------------|---------------------------|
| cilk-the-wsq-wrongdoing.txt    | 3 | 80| 79| No      | 445                          | 512                       |
| Cilk’s THE WSQ (non-robust)    | 3 | 73| 72| Yes     | 71                           | 122                       |
| CLH Lock (robust)              | 3 | 42| 41| No      | 1124                         | 1358                      |
| Dekker (robust)                | 2 | 28| 34| No      | 31                           | 50                        |
| Dekker (non-robust)            | 2 | 24| 30| No      | 35                           | 83                        |
| Lamport (robust)               | 3 | 39| 42| Yes     | 12868                        | 12868                     |
| Lamport (non-robust)           | 3 | 33| 36| No      | 142                          | 162                       |
| Lock-Free Stack (robust)       | 4 | 46| 50| Yes     | 796                          | 828                       |
| MCS Lock (robust)              | 2 | 54| 58| No      | 150                          | 160                       |
| mfa.txt                        | 3 | 14| 11| No      | 122                          | 140                       |
| mp.txt                         | 2 |  6|  4| No      | 20                           | 23                        |

Figure 7. Singularity vs. locality with partial-order reduction and liveness.
| Program                        | T | L | I | Robust? | Visited States (Singularity) | Visited States (Locality) |
|-------------------------------|---|---|---|---------|------------------------------|---------------------------|
| cilk-the-wsq-wrongdoing.txt   | 5 | 80| 79| No      | 532                          | 573                       |
| Cilk's THE WSQ (non-robust)   | 3 | 73| 72| Yes     | 95                           | 150                       |
| CLH Lock (robust)             | 3 | 42| 41| No      | 1289                         | 1496                      |
| Dekker (robust)               | 2 | 28| 34| No      | 37                           | 103                       |
| Dekker (non-robust)           | 2 | 24| 30| No      | 43                           | 121                       |
| Lamport (robust)              | 3 | 39| 42| Yes     | 77657                        | 77657                     |
| Lamport (non-robust)          | 3 | 33| 36| No      | 159                          | 185                       |
| Lock-Free Stack (robust)      | 4 | 46| 50| Yes     | 5504                         | 5504                      |
| MCS Lock (robust)             | 2 | 54| 58| No      | 169                          | 176                       |
| mfa.txt                       | 3 | 14| 11| No      | 124                          | 146                       |
| mp.txt                        | 2 | 6 | 4 | No      | 22                           | 25                        |

**Figure 8.** Singularity vs. locality without partial-order reduction and liveness.