Program-to-Circuit: Exploiting GNNs for Program Representation and Circuit Translation

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ABSTRACT

Circuit design is complicated and requires extensive domain-specific expertise. One major obstacle stuck on the way to hardware agile development is the considerably time-consuming process of accurate circuit quality evaluation. To significantly expedite the circuit evaluation during the translation from behavioral languages to circuit designs, we formulate it as a Program-to-Circuit problem, aiming to exploit the representation power of graph neural networks (GNNs) by representing C/C++ programs as graphs. The goal of this work is four-fold. First, we build a standard benchmark containing 40k C/C++ programs, each of which is translated to a circuit design with actual hardware quality metrics, aiming to facilitate the development of effective GNNs targeting this high-demand circuit design area. Second, 14 state-of-the-art GNN models are tested and analyzed on the Program-to-Circuit problem. We identify key design challenges of this problem, which should be carefully handled but not yet solved by existing GNNs. The goal is to provide domain-specific knowledge for designing GNNs with suitable inductive biases. Third, we discuss three sets of real-world benchmarks for GNN generalization evaluation, and analyze the performance gap between the standard programs and the real-case ones. The goal is to provide more realistic benchmarking, and to enable transfer learning from limited training data to real-world large-scale circuit design problems. Fourth, the Program-to-Circuit problem is a representative within the Program-to-X framework, a set of program-based analysis problems with various downstream tasks. The in-depth understanding of strengths and weaknesses in applying GNNs on Program-to-Circuit could largely benefit the entire family of Program-to-X. Pioneering in this direction, we build a standard benchmark containing 40k C/C++ programs, each of which is translated to a circuit design with actual hardware quality metrics, aiming to facilitate the development of effective GNNs targeting this high-demand circuit design area. Second, 14 state-of-the-art GNN models are tested and analyzed on the Program-to-Circuit problem. We identify key design challenges of this problem, which should be carefully handled but not yet solved by existing GNNs. The goal is to provide domain-specific knowledge for designing GNNs with suitable inductive biases. Third, we discuss three sets of real-world benchmarks for GNN generalization evaluation, and analyze the performance gap between the standard programs and the real-case ones. The goal is to provide more realistic benchmarking, and to enable transfer learning from limited training data to real-world large-scale circuit design problems. Fourth, the Program-to-Circuit problem is a representative within the Program-to-X framework, a set of program-based analysis problems with various downstream tasks. The in-depth understanding of strengths and weaknesses in applying GNNs on Program-to-Circuit could largely benefit the entire family of Program-to-X. Pioneering in this direction, we expect more GNN endeavors to revolutionize this high-demand Program-to-Circuit problem and to enrich the expressiveness of GNNs on programs.

KEYWORDS

Graph Neural Network; High-Level Synthesis; Program Representation

1 INTRODUCTION

Graph Neural Networks (GNNs) have achieved significant advancements in representation learning on graph structured data, e.g., particle and high energy physics [1, 2], chemical analysis [3, 4], social networks [5, 6], and drug-target prediction [7, 8]. Most recently, there has been a surge of interest in GNNs approaches for solving electronic design automation (EDA) problems [9–12], and compiler-related problems by learning program representations [13]. In these problems, data are naturally presented as graphs. For example, circuits are usually described as netlists displaying gates/transistors and their connections, which can be converted into graphs with vertices as gates/transistors and edges as wires; the intermediate representations (IRs) of software programs after compilation can also be represented as graphs [11, 13].

Inspired by the expressiveness and representation power of GNNs, we define a new graph representation learning problem in the joint area of EDA and compiler, namely Program-to-Circuit. Striving for hardware agile development, the goal is to significantly expedite circuit quality evaluation and design via GNNs. More importantly, given a comprehensive study of capabilities and limitations of GNNs on the Program-to-Circuit problem, it would impose greater impacts of GNNs on a much broader domain, the Program-to-X problem. As depicted in Fig. 1, the Program-to-X framework involves multiple front-ends and downstream tasks, including but not limited to EDA problems and various program analysis. The Program-to-Circuit problem is one representative in this framework focusing on fast performance estimation in the EDA domain, which starts from C/C++ and exploits IR graphs to predict hardware quality after circuit translation. Other downstream tasks include program analysis on vulnerability [14] or behavior prediction [13], and CPU throughput estimation [15], etc.

Why Program-to-Circuit matters. Compared with software development, hardware/circuit design is much more time-consuming and requires extensive domain-specific expertise. Since time to market is a lifeblood for companies to keep competitive, there has been rigid demand for agile development of high quality circuits, e.g., application-specific integrated circuits (ASICs) or field-programmable gate array (FPGA) designs, which could eventually reduce the hardware development cycle from years to months or
even weeks. To enable rapid optimization-evaluation iterations in agile development, one essential requirement is to predict circuit design quality quickly and accurately. Traditional EDA tools for circuit design usually take hours to days to accurately predict circuit quality and require extensive manual efforts; however, even though high-level synthesis (HLS) tools accelerate the design process by orders of magnitude via automatic translation (a.k.a., synthesis) from behavioral languages into circuit designs, they do require minutes to hours for circuit synthesis and cannot accurately estimate circuit quality. Motivated by the strong desire for hardware agile development and productivity boost, a perfect and sound solution to Program-to-Circuit is expected to bring a huge leap in EDA domain.

**Why represent programs as graphs.** First, it is natural and easy for programs to be represented as graphs. Compilers often use IRs to represent the source code of programs [16–20], most of which are graph structured, such as data flow graphs (DFGs) or control data flow graphs (CDFGs). Similarly, during the design flow of HLS tools, C/C++ programs are firstly compiled into IR graphs and then translated into circuits. These IR graphs can be easily and automatically obtained from compiler front-ends (e.g., LLVM [19] and GCC [18]) without manual effort, and they are independent of detailed programming language grammar rules and different standards. Second, many performance predictions and design space explorations are operated on DFGs and CDFGs, for example the core HLS algorithms are largely based on the CDFGs [21].

**From Program-to-Circuit to Program-to-X.** Given that IR graphs are the common case for representing programs, the in-depth understanding of capabilities and limitations of GNNs on the Program-to-Circuit problem could not only revolutionize this high-demand circuit design area, but also largely benefit the entire family of Program-to-X. Nonetheless, there are substantial challenges due to limitations in current GNN models. First, IR graphs can largely vary in node degree, graph size, and label distribution, and their topologies are further complicated by massive loops, challenging the generalization capability of GNN models, which will be presented in this paper. Second, there is a huge gap in representation power required by classification and regression. The classification is to predict a discrete class label output for an example, while the regression aims to predict a continuous quantity output (and Program-to-Circuit is an example), which obviously needs more expressiveness in mapping functions. Another obstacle is the lack of standard benchmarks. Thus, we propose the first benchmark for the Program-to-Circuit problem, and encourage more follow-up benchmark works for various downstream tasks. We believe that addressing above challenges of GNNs on Program-to-Circuit will light up the way to follow-up researches for Program-to-X.

**Contributions.** To address the challenges of agile development for circuit design and to understand the GNN representation power on program IR graphs, in this work, we propose a standard formulation of Program-to-Circuit from C/C++ programs by representing them as DFGs and CDFGs, and exploit GNNs for solving the problem. We summarize our contributions as follows:

- **Problem Definition.** We are the first to systemically define the Program-to-Circuit problem. It broadens the application of GNNs to an extremely important problem in the hardware design community and challenges the representation power of GNNs through hardware-related features. More importantly, the understanding of GNN expressiveness on general IR graphs could benefit broader program-related problems, i.e., Program-to-X.
- **Benchmark.** We build a standard benchmark containing 40k C/C++ programs, each of which is translated to a circuit design with actual hardware quality metrics, aiming to facilitate development of effective GNNs targeting this high-demand circuit design area and provide infrastructure to build benchmarks on various program-related downstream tasks.
- **SOTA GNN analysis.** We test and analyze 14 state-of-the-art GNN models on the Program-to-Circuit mapping. Specifically, We identify key design challenges of this problem, which should be carefully handled but not yet solved by existing GNNs. The goal is to provide domain-specific knowledge for designing GNNs with suitable inductive biases.
- **Real-case generalization analysis.** We discuss three sets of real-world benchmarks for GNN generalization evaluation, and analyze the performance gap between the standard programs and the real-case ones. The goal is to provide pointers for future GNN development along this promising Program-to-X direction.

### 2 RELATED WORK

**GNNs in circuit design.** There has been signs of emergence in using GNN approaches to solving problems in circuit designs that can be naturally modeled as graphs. Circuit-GNN [10] uses GNNs to simulate electromagnetic (EM) properties of distributed circuits to replace traditional EM simulators, where each node refers to a resonator and each edge refers to the EM coupling between a pair of resonators. Another category is to model the chip placement into graph formulation and use GNNs to predict the placement quality, where the netlist of the circuit is encoded into a directed graph with cells/components as nodes and the connections between devices as edges. The prediction goals can be wirelength or chip area for digital circuits [22], and gain, bandwidth, or phase margin for analog circuits [9]. Analog circuit (transistor) sizing and symmetry annotation have also been studied [23–25], where the constraints for circuit layout are automatically annotated by GNNs. These prior arts demonstrate potentials of GNNs in circuit design.

**ML-based program analysis.** Program (code) analysis has been attracting great research interests for decades [26, 27]. Recently, Xue et al. [28] comprehensively survey ML-based approaches for program behavior and performance prediction. For instance, Ithemail [15] uses a recurrent-neural-network-based architecture with long short term memory (LSTM) for predicting the number of clock cycles that a processor takes to execute a block of assembly instructions (i.e., throughput) on a x86-64 instruction set architecture. Realizing that IRs of programs can be constructed as graphs, GNNs are employed for different purposes of program analysis. For example, Shi et al. [13] selectively build a graph from the assembly code and perform branch prediction with dynamic states of a program (i.e., the value change of a fixed set of registers) as additional inputs. Ghaffarian and Shahriari [14] apply GNNs on different IR graphs, such as control-flow graphs and abstract syntax trees, to detect
program vulnerability. IronMan [11] is a most recent work where part of it exploits GNNs for both circuit design and program analysis, closest to the Program-to-Circuit problem. It first translates programs into DFGs, and then applies GNNs to predict hardware performance. Overall, there are rapidly increasing efforts in exploring GNNs for program representation learning and analysis.

3 PROGRAM-TO-CIRCUIT PROBLEM

3.1 Graph-Structured Intermediate Representation

An intermediate representation (IR) is the data structure used internally by a compiler to represent the source code of a program, which can be used for further processing, such as optimization and translation [16, 17]. Many modern compilers transform a program into a graph-structured IR, such as the GNU Compiler Collection [18] and LLVM [19] for C/C++, and the CPython [20] interpreter for C and Python. There are various types of IR graphs, such as data flow graph (DFG), control flow graph (CFG), control data flow graph (CDFG), program dependence graph (PDG), control dependence graph (CDG), and data dependence graph (DDG). Some graphs can be constructed from others, for example, the CDFG is composed of DFG and CFG, while the PDG is composed of CDG and DDG.

In this work, we consider DFGs and CDFGs as the IR graphs. Specifically, DFGs are the graphs translated from basic blocks, a straight-line code sequence with no branches except to the entry and no branches out except at the exit [29]; CDFGs are the graphs translated from programs with loops, jumps, and branches. The major difference between DFGs and CDFGs is that, DFGs do not contain any loops, while CDFGs contain additional nodes and edges/loops for control dependency.

These IR graphs can be easily obtained by common compiler front-ends, such as LLVM and HLS tools, where HLS tools can be regarded as specialized hardware compilers. More realistic examples of programs and their extracted DFGs and CDFGs can be found in the Appendix.

3.2 Problem Formalization

Input representation. The inputs to the Program-to-Circuit problem are directed, possibly cyclic IR graphs representing programs written in behavior-level programming languages, such as C / C++ / SystemC. These IR graphs are automatically constructed from common compiler front-ends. Each node graph belongs to one of the three categories: normal operations, blocks (i.e., control signals) or ports (i.e., function arguments). Graph edges reflect either data dependency or control dependency among nodes.

Output. With the help of HLS tools, behavioral programs can be directly translated and mapped to circuit designs, either ASICs or FPGA designs. The functionality of the circuit is exactly the same as the software program, e.g., a fast Fourier transform or a convolutional neural network. Such transformations follow a set of complex but deterministic rules according to the transformation tools, e.g., program compilers and HLS tools. Although these tools differ in transformation details across different platforms, they share similar heuristics and mapping rules in both scheduling/binding and logic/physical synthesis. The goal of this work is to exploit GNNs to learn such underlying heuristics and mapping rules given the IR graphs that represents behavior-level programs, so as to quickly predict the circuit quality (e.g., chip area, resource usage, timing, total power, etc.) as accurately as possible.

Case study problem. As a case study, we take FPGAs as the target circuit platform. The translation and mapping flow of C/C++ program to circuits on FPGA is illustrated in Fig. 2. GNNs are expected to predict common hardware quality metrics, include resource usage and circuit timing (which determines its maximum working frequency). We consider five prediction tasks: DSP, FF, LUT, SLICE, CP, as summarized in Table 1. The first four are different types of resource, and the last one is circuit timing. Fig. 2 (e)-(g) provide structures of various resources and CP timing.

Program-to-X extension. Keeping the front-end graph-structured inputs unchanged while replacing the downstream prediction tasks can easily extend to other program-related problems within this framework. For instance, the software vulnerability detection problem [14] adopts similar input graphs, where the downstream task is a binary classification to decide whether the program is vulnerable or secure.

3.3 Benchmark

Benchmark generation. The benchmark for this Program-to-Circuit problem consists of synthetic C/C++ programs and real-world HLS applications. The synthetic programs fall into two categories, basic blocks that derive DFGs, and programs with control loops and branches that derive CDFGs. All of the synthetic programs are generated by a C program generator ldrgen [30], a plugin of Frama-C [31, 32]. There are 19,120 and 18,570 C programs in the DFG dataset and CDFG dataset, respectively. Each sample is arranged in the form of < program, extracted IR graph, actual resource/timing >.

In addition, we include three sets of real-world HLS applications: MachSuite [33], CHStone [34], and PolyBench/C [35], consisted of 16, 10, and 30 different applications, respectively. The real-world applications are used for generalization evaluation of different GNN models.

Node/Edge Features. There are seven features available for each node, which capture both node properties and the paths that this node participates in. Table 2 summarizes all the node features with example values. Each edge has two features, the discrete edge type in integers, and a binary signal marking whether this edge is a back edge.

By reusing the front-end IR graph construction in this work, we expect more follow-up benchmarks with different downstream tasks to be integrated into the Program-to-X framework.

3.4 Statistics of Benchmark

Statistics of Synthetic DFGs/CDFGs. Figure 3 and Figure 4 show the distribution of the number of nodes/edges among 19,120 DFGs in the DFG dataset and among 18,570 CDFGs in the CDFG dataset, respectively.

- The graph size of CDFGs is roughly two times as large as that of DFGs.

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1. To distinguish loops in programs and loops in graphs, we use control loops in the following context to represent loops in programs.
Figure 2: The Program-to-Circuit problem solved in this work. (a) The design flow starting from behavioral programs to hardware circuits. (b) An example program written in C++. (c) The intermediate representation (IR) graph extracted by front-end compilers. (d) The working flow of GNNs, predicting actual resource utilization and timing merely based on raw IR graphs. (e) The translated circuit from the example program, using resources including DSPs, LUTs, FFs, and SLICEs. (f) The detailed structure of a SLICE containing LUTs and FFs. (g) An example of critical path (CP) timing. HLS tools estimate resource utilization and timing based on RTL designs after circuit translation. GNNs are expected to learn the mapping rules (including scheduling/binding, logic and physical synthesis), so as to predict the actual resource usage and CP timing as accurate as possible.

| Resource and Timing | Description |
|---------------------|-------------|
| DSP: Digital Signal Processor |
| FF: Flip-Flop |
| LUT: Look-Up Table |
| SLICE |
| CP: Critical Path Timing |
| A small processor able to quickly perform mathematical operation on streaming digital signals. |
| A small memory component able to store a bit, typically used as a fast register to store data. |
| A set of logic gates hard-wired on FPGAs, storing predefined truth tables and performing logic functions. |
| An elementary programmable logic block that contains a set number of LUTs, FFs and multiplexers. |
| The maximum signal delay of a path from an input to an output, usually in the unit of nanoseconds. |

Table 2: Node features and example values.

| Feature                   | Description                        | Values                           |
|---------------------------|------------------------------------|----------------------------------|
| Node category             | General node type                  | operation nodes, blocks, ports, misc |
| Bitwidth                  | Bitwidth of the node               | 0~256, misc                       |
| Opcode category           | Opcode categories based on LLVM    | binary_unary, bitwise, memroy, etc. |
| Opcode                    | Opcode of the node                 | load, add, mux, xor, icmp, select, etc. |
| Is start of path          | Whether the node is the starting node of a path | 0, 1, misc |
| Is LCD node               | Whether the node uses LCD resource  | 0, 1, misc                        |
| Cluster group number      | Cluster number of the node          | -1~256, misc                      |
• There is no loop in DFGs since they are generated from basic blocks, while the majority of CDFGs has loops (due to control signals in programs) and some of the loops possess considerable loop length.

Statistics of Label Values in Synthetic DFGs/CDFGs

Table 5 shows graph information, resource utilization and timing of MachSuite. The graphs in MachSuite usually have larger size, with more number of nodes and edges.

Table 4 shows graph information, resource utilization and timing of CHStone. One characteristic of applications in CHStone is that, each application is consisted of multiple functions, whereas our synthetic programs only have one function per program.

Table 5 shows graph information, resource utilization and timing of PolyBench. Each application in PolyBench has a single function with a proper graph size, which explains the reason why GNN models generalize better on this benchmark compared to other real-world benchmarks.

We have several observations on the real-world benchmarks:

• In real-world applications, there is no significant relationship between graph size and resource usage, such as md_kernel in Machsuite, adpcm_main and sha_stream in CHStone.

• Several applications have really complicated operations, such as back_prop in MachSuite.

4 GNN MODELS

GNNs operate by propagating information along the edges of a given graph. Specifically, each node $v$ is initialized with an representation $h_v^{(0)}$, which could be either a direct representation or a learnable embedding obtained from features of this node. Then, a GNN layer updates each node representation by integrating the
GraphSage [38] can be recognized as a vari-

tuitively similar to unrolling through time steps, but increases the
gNN capacity by using different parameters in the update function
every step of message passing. An alternative is to stack several GNN layers, in-
tuitively similar to unrolling through time steps, but increases the
gNN capacity by using different parameters in the update function for each time step.

In this work, we test 14 different GNN models and analyze their
performance on the Program-to-Circuit problem. To fairly evaluate
these models, we use a general structure as shown in Fig. 8. These
14 GNN models can be roughly categorized into four groups, ac-
cording to their origins, the way to update node representations, and whether edge information is considered.

Graph Convolutional Network (GCN) and variants. GCN [36] is inspired by the first order graph Laplacian methods, and it essentially performs aggregation and transformation on node representations without learning trainable filters. GCN can be equipped with a virtual node [4]; this virtual node serves as a global scratch space that each node reads from and writes to in every step of message passing. SGC [37] is a simplified version of GCN, which reduces computation complexity through successively removing nonlinearities and collapsing weight matrices between consecutive layers, corresponding to a fixed low-pass filter followed by a linear classifier. GraphSage [38] can be recognized as a variant of GCN, which samples a fixed number of neighboring nodes to keep the computational footprint consistent. The convolution operation based on auto-regressive moving average filters (ARMA) [39] is able to offer a larger variety of frequency responses and can account for higher-order neighborhoods compared to polynomial filters with the same number of parameters. PAN [40] considers path integral information in the convolution operation, which is a
Graph isomorphism network (GIN) and variants. GIN [41] is provably as powerful as Weisfeiler-Lehman graph isomorphism test, taking advantage of sum aggregators over a countable input feature space. Similarly, GIN can also be equipped with a virtual node [4]. Principle neighborhood aggregation (PNA) [42] emphasizes the necessity to use complementary aggregators, which allows each node to better understand the graph structure and retain neighborhood information, especially under a continuous input feature space. The sum aggregator is generalized as a combination of a mean aggregation and degree-scalers, enabling the network to amplify or attenuate signals based on the degree of each node.

Employment of multi-relational information. Graph attention networks (GATs) [43] apply attention mechanisms to implicitly assign different importances to nodes in the same neighborhood. Gated graph neural networks (GGNNs) [44] have trainable edge-dependent weights with gated recurrent units. Rather than unrolling layer-wise computation through time steps as GAT and GGNN, relational GCN (RGCN) [45] utilizes edge-dependent weight with non-linearity activation, which is specifically designed to characterize multi-relational data and contextual information.

Inspired from vision tasks. Inspired by the advances in pixel-wise prediction tasks brought by encoder–decoder architectures such as the U-Net, graph U-Net [46] develops an encoder-decoder structure on graph, which can encode and decode high-level features while maintaining local spatial information. Inspired by the feature-wise linear modulation (FiLM) in the visual question answering domain, GNN-FiLM [47] makes use of hypernetworks in learning on graphs, combining learned message passing functions with dynamically computed element-wise affine transformations.

5 EXPERIMENT

5.1 Experimental Setup

Our framework is built upon Open Graph Benchmark (OGB) library [48], and the proposed benchmark datasets are compatible with OGB. All the aforementioned GNN models are implemented with Pytorch Geometric [49]. Experiments were performed on a Linux host with a 64-core Intel Xeon Gold 5218 CPU (2.30 GHz) and Nvidia RTX 2080Ti GPUs. For DFG and CDFG datasets, the data are randomly split into 80% train, 10% validation and 10% test; real-world benchmarks are only used for generalization evaluation. Each GNN model is empirically set to have 5 layers, with a hidden-dimension size of 300. For synthetic dataset, the sum pooling is used to derive graph-level representations. Since the graph scale of real-world applications are significantly larger than that of synthetic IR graphs, the mean pooling is used to guarantee better generalization. The feed-forward network has the structure 300-600-300-1. We train models using the Adam optimizer for 300 epochs. Learning rates, weight decay, dropout and other hyper-parameters are tuned on the validation set. For each model, we conduct five training runs with different random number seeds and hyper-parameters (but close to the tuned values) and report the average of three with least validation error.

5.2 SOTA GNNs on DFG and CDFG from Synthetic Programs

DFG vs. CDFG. Table 6 exhibits relative errors of predictions on DFGs and CDFGs from the synthetic programs. The error rates on DFGs are conspicuously larger than those on DFGs, due to three major reasons. First, the graph size of CDFGs is approximately twice as large as that of DFGs, increasing the difficulty of graph-level regression. Second, DFGs are extracted from basic blocks without controls and branches, so that there are no loops in the graph; by contrast, CDFGs has a considerable number of loops, as shown in Fig. 4, challenging the representation power of GNNs. Third, control signals introduce additional nodes/edges that represent control states and dependency, which are seemingly unrelated to resource usage, greatly encumbering the resource prediction; meanwhile, control signals are usually accompanied with more complex memory operations [50], such as store and alloc, further complicating the allocation of FF/LUT/SLICE.

Model Analysis. In terms of performance variance of different models, PNA and RGCN generally show superior performance, implying two takeaways. First, the relational information (i.e., edge information) is important in IR graphs, since they represent data dependency, control dependency, or a mix of these two, which is a critical basis in logic synthesis and impacts resource allocation. Second, equipped with multiple aggregators, PNA is more powerful to characterize different neighborhood information of each node, thus making better predictions. Fig. 9 shows how absolute and relative errors of PNA predictions distribute with ground truth. It is noteworthy that in the relatively small cases (with small resource usage), the absolute errors stay in a rather consistent range, which leads to decrease of relative errors in a multiplicative inverse manner; in the middle part, the absolute errors grow with the graph sizes, resulting in consistent relative errors; in the relatively large cases, the incapability of generalization across graph size is exposed.

Domain-specific Insights. Resource. Among four types of resource, DSP is mainly used for computation; FF utilization often relates to memory operations and small arrays; LUTs may appear in computation, memory or control nodes; SLICE is a functional unit that comprises multiple LUTs and FFs. The core to making precise DSP prediction is to distinguish major computation nodes that are most likely to use DSPs. For instance, a multiplication node with a large bitwidth tends to use DSPs, while divisions and bitwise operations prefer LUTs. Similarly, effective extraction of memory-related nodes would greatly benefit FF predictions. Since LUTs are involved in the entire graph (as computation units and as glue logics to connect the circuit components together), the graph-level understanding is important. The predictions of SLICE are dependent on FFs and LUTs. To briefly summarize, it is helpful to carefully characterize neighborhood information from each node’s predecessors, successors, itself, and their relations, such that the preference of resource types on different nodes can be clearly understood and the sophisticated mapping rules from heterogeneous nodes to resource usage can be quantitatively learned. Timing. Compared with resource predictions, the CP timing predictions show relatively lower error rates and better consistency between DFGs and CDFGs. A probable reason is that the CP timing is insensitive to graph sizes since it captures local information between any two FFs, as
shown in Fig. 2 (d). As long as the path segment that introduces the maximum delay is recognized, the CP timing can be accurately predicted.

5.3 From Synthetic to Real-case Generalization

Generalization Performance. Fig. 10 displays the generalization results on real-world applications. Compared with the test errors on synthetic DFGs and CDFGs, the generalization to real-case shows a large performance degradation. Several causes to blame on include the divergence in graph sizes, the drastic number of loops, more complicated operations, and appearance of peculiar cases among these real applications. First, IR graphs in real-world applications generally have a wider range of size, ranging from tens to thousands of nodes/edges. This requires GNN models to generalize effectively to much larger graphs than those appearing during the training. Second, real-world applications involve a considerable number of loops, both in the count of loops and the length of loops. This easily confuses GNN models to discriminate these graph topologies, thus unable to make proper predictions. Third, real-world applications come with more complex operations that rarely appear in synthetic programs, which confirms the necessity of our setting with null values in feature embedding and could provoke future investigations on generalization with null values. Furthermore, these real-world applications can behave wildly and counter-intuitively, where small IR graphs consume much resource yet larger graphs use little resource. These cases, as well as those extremely large IR graphs, can be recognized as out-of-distribution points.

GNN vs. HLS tools. GNN predictions are also compared with estimations from commercial HLS tools in Fig. 10. Notably, HLS tools estimate resource usage and timing based on RTL designs generated after circuit translation (see Fig. 2(a)), taking much longer time; whereas GNN models make predictions directly from raw IR graphs before the translation (see Fig. 2(b)), thus much more challenging. Fortunately, GNN models can still provide predictions comparable to HLS tools, or generally surpass HLS tools in timing prediction. Such results empirically demonstrate that given the current message passing mechanisms and model designs, GNNs are capable to learn a simplified version of the sophisticated heuristics and mapping rules used in scheduling/binding and logic/physical synthesis, at least equivalent to the rules used in HLS estimations.

5.4 Discussion.

We envision three potential directions that would benefit the Program-to-Circuit problem.

Table 6: Relative errors of predictions on DFG and CDFG datasets, among different GNN models. The top two models with least error rates are marked in bold.

| Model               | DFG          | CDFG         |
|---------------------|--------------|--------------|
|                      | DSP | LUT | FF | SLICE | CP Timing | DSP | LUT | FF | SLICE | CP Timing |
| GCN                 | 16.31% | 16.49% | 21.27% | 22.29% | **6.12%** | 25.30% | 28.64% | 38.34% | 43.63% | 8.79% |
| GCN - Virtual Node  | 15.72% | 15.93% | 21.64% | 23.21% | 6.36%   | 17.31% | 33.93% | 39.94% | 49.22% | **8.13%** |
| SGC                 | 42.12% | 14.01% | 17.11% | 15.90% | **6.12%** | 18.47% | 22.86% | 26.47% | 23.38% | 8.87% |
| GraphSage           | 15.24% | 14.13% | 17.23% | 16.49% | 6.38%   | 16.88% | 32.65% | 44.36% | 44.84% | 8.54% |
| ARMA                | 15.52% | 16.10% | 22.08% | 22.63% | 6.58%   | 15.47% | 28.48% | 38.82% | 46.12% | 8.76% |
| GIN                 | 15.04% | 16.17% | 23.09% | 24.19% | 6.40%   | 17.94% | 29.40% | 48.64% | 49.44% | 8.59% |
| GIN - Virtual Node  | 12.65% | 11.64% | **14.41%** | **14.34%** | 6.26%   | **14.71%** | **25.21%** | 32.15% | 28.31% | 8.42% |
| UNet                | 18.40% | 14.90% | 19.17% | 17.18% | 6.61%   | 18.92% | 32.65% | 44.36% | 44.84% | 8.54% |
| FiLM                | 20.05% | **12.50%** | 16.94% | 16.30% | 6.27%   | 17.42% | 26.97% | 27.35% | 31.50% | 8.67% |
Generalization across graph sizes, node degrees, and out-of-distribution cases. To impose more impact of GNNs on many EDA problems [12], GNNs are expected to effectively generalize to larger or out-of-distribution graphs, especially in the case that real-world applications greatly vary in sizes. The Program-to-Circuit problem is a starting task but also a screening test, exhibiting the current difficulty in generalizing across graph sizes and out-of-distribution cases. We also observe that in IR graphs, while most nodes have low degrees, there do exist several busy nodes with high degrees, taking the role of hubs in control and data flows. It would be interesting for GNNs to further investigate these nodes or scale-free graphs.

Structural and algorithmic innovations to process heavy-loop graph topologies. There are multiple loops in IR graphs, especially in real-world applications. From the aspect of domain knowledge, the very large loops usually relate to complex computation operations, which typically involve sharing and interference of computational resources; the small loops usually relate to memory operations, which typically involve register allocation and auxiliary computation resources. With a large number of small loops, i.e., a large number of memory operations, the register allocation becomes increasingly complicated, since different memory operations could share the same registers in different time steps, or one memory operation may occupy multiple registers simultaneously. The complexity of scheduling and binding of registers grows exponentially, which poses challenges on GNNs to understand these rules. Since memory operations often require auxiliary computations, these operations also have intricate impacts on the allocation of computation resources, which increases the difficulty of accurately estimating resource utilization. From the aspect of GNN models, the class of message-passing-based GNN models has limited expressiveness and is not better than the 1-Weisfeiler-Lehman isomorphism test [51], which is not good at handling loops. Given the current limitations, we envisage that the discernment of various loops would be beneficial to accurately predict resource usage or other tasks.

Gap from classification to regression. Existing GNN models already show excellent performance on node/graph classification or...
Figure 10: Generalization of PNA on three real-world benchmarks. Note that in Figure 10b, the stars and triangles that reside on the horizontal axis indicate either the ground truth to be zero or perfect predictions. Since HLS is not able to provide predictions on SLICE utilization, the corresponding relative error is left blank.
link prediction tasks, while there is still a long way to go in graph-level regression that demands much higher representation power. The Program-to-Circuit problem is a representative requiring predictions of exact values, which will inspire wider applications.

The Program-to-Circuit problem is a pillar stone in the EDA domain. Given that fast and accurate circuit quality estimation is the foundation for design exploration and optimization in EDA, it is hard to believe success on more challenging tasks would ever happen if we cannot properly accomplish the Program-to-Circuit problem. Thankfully, the current results are not perfect but really promising.

6 CONCLUSIONS

In this work, we defined and discussed the Program-to-Circuit problem using GNNs, which is of great importance not only in EDA domain but can also largely benefit broader program-related programs, Program-to-X. We designed a standard benchmark for the Program-to-Circuit problem, experimented 14 different GNNs, and discussed their performance variance with circuit domain-specific analysis. We further screened the generality and representation power of GNNs on real-case applications, and discussed possible limitations of current GNN models when applied to program-related problems. Pioneered in this promising direction, we expect more follow-up benchmarks and studies on GNN representation and generalization capability within the Program-to-X framework.

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