Transferred metal gate to 2D semiconductors for sub-1 V operation and near ideal subthreshold slope

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Ultrathin two-dimensional (2D) semiconductors are regarded as a potential channel material for low-power transistors with small subthreshold swing and low leakage current. However, their dangling bond–free surface makes it extremely difficult to deposit gate dielectrics with high-quality interface in metal-oxide-semiconductor (MOS) field-effect transistors (FETs). Here, we demonstrate a low-temperature process to transfer metal gate to 2D MoS2 for high-quality interface. By excluding extrinsic doping to MoS2 and increasing contact distance, the high–barrier height Pt-MoS2 Schottky junction replaces the commonly used MOS capacitor and eliminates the use of gate dielectrics. The MoS2 transferred metal gate (TMG) FETs exhibit sub-1 V operation voltage and a subthreshold slope close to thermal limit (60 mV/dec), owing to intrinsically high junction capacitance and the high-quality interface. The TMG and back gate enable logic functions in a single transistor with small footprint.

INTRODUCTION

Power-constraint application scenarios, e.g., the edge devices in Internet of Things, demand the electron devices with low-power devices (1–5). To meet these requirements, the field-effect transistors (FETs), the building block of integrated circuits, should have low operation voltage, small subthreshold slope (SS), and low leakage current. Ultrathin two-dimensional (2D) semiconductors, especially transition metal dichalcogenides (TMDs) with relatively large bandgap, have been shown with excellent electrostatic gate control for low-power electronics (6–11). The high-k dielectrics on 2D TMD FETs should be ultrathin and uniform and have weak interaction with TMDs to preserve their intrinsic properties. However, it has been proven a grand challenge to prepare high-k dielectrics on dangling bond–free surface of 2D TMDs because of the lack of nucleation sites (6, 12, 13).

To eliminate the use of high-k dielectrics in FETs, an alternative approach is to adopt junction capacitance in the gate terminals of FETs, e.g., the pn junction in junction FETs (JFETs) and Schottky junction in metal-semiconductor FETs (MESFETs), which usually have much larger capacitance than dielectric capacitance and show efficient electrostatic gate control (3, 14). The surface potential changes in JFETs and MESFETs are equal to the gate voltage (14–16). Compared with JFET, the MESFET has a simple structure and is relatively easy to fabricate. However, the Fermi level pinning and metal-induced gap states in the metal/TMD interface make it challenging to fabricate ideal Schottky junction (17–21).

RESULTS AND DISCUSSION

Figure 1A depicts cross-sectional schematics of a top-gated 2D MoS2 transistors with HfO2 dielectrics. Cross-sectional transmission electron microscopy (TEM) image (Fig. 1B) shows the interface disorder between gate dielectrics and MoS2 as well as the damages to the top layer of MoS2, which inevitably results from harsh dielectrics deposition process. These interface disorders act as charge traps and adversely affect the SS and hysteresis of the device (Fig. 1C). In addition, the carriers in top-gated FETs locate extremely close to the insulator/semiconductor interface. The interface disorders and traps strongly scatter the carrier transport and degrade the device performance (12, 13, 22). Figure S1 shows thickness-dependent electrical characteristics of the MoS2 top-gated FETs with 15-nm-thick HfO2 dielectrics grown by atomic layer deposition (ALD) process. The SS of the devices is larger than 100 mV/dec and shows large variation in the forward and reverse sweep.

In this work, we design and fabricate transferred metal gate FETs (TMGFETs) based on a transferred Pt/MoS2. By using transfer metal gate and self-assembled layer (SAL), we achieve an ideal metal/MoS2 Schottky junction. Our density functional theory (DFT) calculations reveal that the change of Schottky barrier height (SBH) is a result of the increased interfacial contact distance and reduced metal-induced gap state. Because of the optimized interface and efficient gate control, the TMGFET shows an SS approaching thermal limits of 60 mV/dec, negligible hysteresis, and ON/OFF ratio of 106 with low leakage current. We also demonstrate thickness-dependent logic functions (OR and AND) using TMG and back gate in a single transistor. Our study shows that 2D TMGFETs provide a design of simplified device structure for low-power electronics.

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junction for comparison, including electron beam evaporation and transferred metal electrode method with and without SAL.

Figure 1D is the cross-sectional schematic of a MoS₂(TMGFET) with the transferred Pt electrode. The detailed fabrication process is described in Materials and Methods and fig. S2. Benefiting from the mild transfer method of the gate electrode, the MoS₂ channel shows negligible defects (Fig. 1E). The semiconducting channel in MoS₂(TMGFET) configuration is away from the metal/MoS₂ interface (Fig. 1F). The carrier in MoS₂ channel suffers from less scattering from the metal/semiconductor interface, which allows to retain the intrinsic mobility of MoS₂.

For the MoS₂(TMGFETs) with interfacial layer, we insert a SAL at the Pt/MoS₂ interface to unpinning the Fermi level. The detailed fabrication process is schematically illustrated in fig. S3. Figure 1G and H) is the cross-sectional schematic and the TEM image at the interface of the Pt/SAL/MoS₂ interface, respectively. Similar to the Pt/MoS₂, the Pt/SAL/MoS₂ still retains the intact characteristics of MoS₂ layer without any damage. The SAL uniformly distributed between Pt and MoS₂ with a thickness of 1.5 nm. Figures S4 and S5 show the high-angle annular dark-field scanning transmission electron microscopy (STEM) image of the Pt/MoS₂ and Pt/SAL/MoS₂, respectively. We characterize the surface of the samples using atomic force microscopy (AFM) (fig. S6). It is noteworthy that the SAL only exists on the surface of MoS₂ and shows absence on the surface of SiO₂, which is possibly a result of the binding energy between the organic layer and the MoS₂ (6).

We perform temperature-dependent measurement to investigate the SBH of the Pt/MoS₂ and Pt/SAL/MoS₂ (fig. S7). The SBH is extracted by using the 2D thermionic emission equation and an Arrhenius plot (19). Figure 2 (A to C) presents the SBH of these devices with different contact configurations, including evaporated Pt electrodes and transferred Pt electrodes with and without SAL. The
Fermi level of evaporated Pt contact lies close to the conduction band of MoS$_2$, exhibiting SBH of 62 meV. For the transferred Pt/MoS$_2$, because of minimized disorder and weak interaction at the interface, the Fermi level lies close to the valence band with SBH of 147 meV. For the transferred Pt/SAL/MoS$_2$, the SAL separates the metal and MoS$_2$, reduces the metal-induced gap states, and increases the SBH (261 meV), which enables highly efficient gate control and suppresses the leakage current (24). The MoS$_2$/SiO$_2$ interface is rich with trap states and can dope the MoS$_2$ channel, thus affecting the SBH between the top metal electrode and MoS$_2$ (19, 26). To eliminate this extrinsic factor, we adopt hexamethyldisilazane as a passivation layer of SiO$_2$ to reduce the substrate doping effect (fig. S8).

Furthermore, we construct the Pt/MoS$_2$ contact model with chemical bonding and different contact distances to understand the fundamentals of the interface. Through DFT calculations, we can determine the density of state (DOS) at the interface caused by the interfacial layer (Fig. 2, D to F) (20). For the evaporated contact, the interlayer distance between Pt atom and MoS$_2$ is 2.7 Å after the relaxation, in which they form covalent bonding at the interface (Fig. 2G). The $E_F$ of the evaporated Pt contact electrode lies in the middle of the MoS$_2$ bandgap (Fig. 2D). Owing to the decay of metal wave function that penetrates to the semiconductor with nanometer depth, metal-induced gap states form in the forbidden band of MoS$_2$, thus reducing the barrier for electrons (17, 26). The first layer of MoS$_2$ is metallized under the contact electrode, leading to the Fermi level pinned close to the conduction band of MoS$_2$ (19, 26).

For the transferred Pt/MoS$_2$ contact model, the interlayer distances are fixed from 5.2 to 9.2 Å; and for the transferred Pt/SAL/MoS$_2$ model, the interlayer distance is relatively large (11.2 Å) according to the TEM characterization results (Fig. 1H). Figure 2 (E to F) shows the corresponding DOS of the transferred metal contact with and without SAL. In contrast with the direct contact model, almost no metal-induced gap states exist in the bandgap in both cases. For the Pt/MoS$_2$ contact model with the interlayer distance of 5.2 Å, the Fermi level lies close to the valence band of MoS$_2$ (Fig. 2E). For the Pt/SAL/MoS$_2$ model with the interlayer distance of 11.2 Å, the Fermi level lies close to the valence band of MoS$_2$ (Fig. 2F). Figure S9 presents the DOS of the junction with the interlayer distances of 7.2 and 9.2 Å. The Schottky barrier can be obtained by measuring the
energy difference between the Fermi level (\(E_F\)) and the original conduction band minimum (\(E_C\)) or valence band maximum (\(E_V\)). Figure 2H is the SBH corresponding to the distance between the Pt and the MoS\(_2\). With the increase of interlayer distance, the Fermi level shifts from \(E_C\) close to \(E_V\).

Figure 3A shows representative optical and AFM image of the MoS\(_2\) TMGFET. The source/drain (S/D) electrodes are transferred Ag electrode, and the gate stack is transferred Pt/SAL/MoS\(_2\). For comparison, we also fabricate MoS\(_2\) TMGFET without SAL. Ag has relatively low work function and can form ohmic contact to MoS\(_2\). Therefore, the Pt gate and Ag source electrode with MoS\(_2\) act as asymmetric contact diode. The Pt/SAL/MoS\(_2\) junction shows an ideality factor \(\eta\) of 1.18, and the Pt/MoS\(_2\) shows an ideality factor \(\eta\) of 1.83 (Fig. 3B), suggesting high interfacial quality of the interface. Considering the lower ideality factor and current, we choose Pt/SAL/MoS\(_2\) as the gate stack. Figure 3C shows the MoS\(_2\) thickness-dependent transfer characteristics of TMGFETs. For the device with monolayer MoS\(_2\), it exhibits enhanced mode with an ON/OFF ratio of about \(10^3\); for the device with 8.1 nm thickness, the ON/OFF ratio is about \(10^6\). The \(V_{th}\) shift from 0.04 to −0.21 V with thickness increase from 0.9 to 8.1 nm. Thicker MoS\(_2\) requires higher voltage to deplete the channel region and shifts the threshold voltage to the negative side.

Figure 3D presents the corresponding SS as a function of drain current. All the devices show SS close to thermal limits (60 mV/dec), which is much smaller than the top-gated MOSFET (>100 mV/dec). Benefiting from the small hysteresis, the SS for the forward and reverse sweep almost overlap in the subthreshold region. The clean interface in TMGFETs minimizes the trapping states and allows an ideal SS. In comparison with the JFET made with metallic 2D materials, the carrier concentration and conductivity of the metal electrode are much higher. The gate voltage applied to the electrode fully drops in the metal/semiconductor junction, in which any variation in gate potential is completely transferred to channel. The perfect interface, together with the high gate controllability, ensure that the SS is approaching the thermal limits.

Similar to conventional MOSFET, the transconductance can be used to extract the effective filed-effect mobility (14). The mobility of the TMGFET can be expressed according to Eq. 1

\[
\mu = \frac{L G_{\text{max}}}{W q N_d}
\]  

where \(L\), \(W\), and \(t\) are the channel length, gate width, and thickness of channel, respectively. \(G_{\text{max}}\) is the max transconductance, \(q\) is electron charge, and \(N_d\) is the carrier concentration. The \(N_d\) can be estimated by electron carrier density at zero gate voltage by Hall measurement (fig. S10)

\[
N_d = \frac{-HI}{V_{th}qt}
\]  

where \(H\) is the magnetic field, \(I\) is the current, and \(V_{th}\) is the Hall voltage. The highest effective field-effect mobility of the TMGFET is extracted as 106.1 cm\(^2\)/V·s. The high-quality Pt/SAL/MoS\(_2\) interface helps to reduce the scattering at the interface and retains the intrinsically high mobility of MoS\(_2\). Thickness-dependent field-effect mobilities of top-gated MoS\(_2\) FETs are given in fig. S1, ranging from 4.9 to 33.8 cm\(^2\)/V·s, which is much smaller than the mobility of TMGFET. Figure 3E is the temperature-dependent transfer characteristics of TMGFET. The transconductance \(G_m\) and gate leakage current are given in fig. S11. We measured the carrier density of MoS\(_2\).
from 300 to 360 K, and the corresponding mobilities of TMGFETs are 89.4, 186.1, 170.1, and 287.4 cm²/V·s under 300, 320, 340, and 360 K, respectively. The carrier of TMGFET is away from the top surface, thus reducing the surface phonon scattering. The Coulomb scattering reduces with temperature and results in high mobility (1).

Figure 3F shows the output characteristics of TMGFETs. The device shows linear behavior at the small $V_d$ region, indicating ohmic contact of the Ag/MoS₂. The output current easily saturates at various gate voltages and shows the highest output current of 3.9 $\mu$A/µm with the highest drain voltage of 2 V.

For the TMGFETs with Ag S/D electrodes, the contact between Ag and the top layer MoS₂ is ohmic. When positive voltage is applied to the gate electrode, there will be leakage current from the source to the gate electrode. To reduce the surface leakage of the TMGFET, we use the Au S/D electrode to construct Schottky contact (Fig. 4A). Compared with the Ag contact, a small Schottky barrier forms at the Au/top MoS₂ interface. When positive voltage is applied to the gate electrode, the Au/top MoS₂ acts as a reverse biased Schottky diode and decreases the surface leakage current. Figure 4B shows transfer characteristics of the Au S/D TMGFETs with different thicknesses. Although the ON-state current is much smaller compared with the Ag contact one, both OFF-state current and gate leakage show notable reduction. Figure 4C is the output characteristics with the Au S/D electrode, exhibiting much smaller output current compared with the Ag contact.

To increase the current density of the device with Au contact, we use a self-aligned surface doping method to increase the carrier concentration and reduce the access resistance. After completing the fabrication process of the TMGFETs with Au contact, polyvinyl alcohol (PVA) is spin-coated onto the device, acting as n-type dopant to increase the conductivity of MoS₂ (27). Figure S12 shows the n-type doping effect of back-gated MoS₂ FET with the use of the PVA. Figure 4D illustrates the schematic image of MoS₂ TMGFET with self-aligned doping and Au S/D. The PVA increases the carrier concentration in MoS₂ because of charge transfer. Even the carrier density of MoS₂ close to the contact region increases, the Schottky barrier at the Au/top MoS₂ still acts as a reverse diode to reduce the surface leakage. Figure 4E shows the double sweep transfer characteristics of the TMGFETs before and after the PVA doping. With the reduced contact resistance, the ON-state current shows notable improvement of over 2 decades from $7.4 \times 10^{-9}$ to $1.11 \times 10^{-6}$ A. The turn-on voltage shifts to the negative direction.

Fig. 4. Electrical characteristics of the optimized MoS₂ TMGFET. (A) Schematic illustration and (B) Transfer characteristics of MoS₂ TMGFET and Au S/D electrodes. (C) Output characteristics of MoS₂ TMGFET with Au S/D electrodes. (D) Schematic illustration of MoS₂ TMGFET with Au S/D electrodes and self-aligned doping. (E) Transfer characteristics for MoS₂ TMGFET before and after self-aligned doping. (F) Transfer characteristics of the doped TMGFET under different gate bias. (G) Hysteresis and SS of the doped TMGFET. (H) Mobility of the TMGFET with different film thicknesses. (I) Output characteristics for doped MoS₂ TMGFET in Fig. 1E.
Figure 4F shows the transfer characteristics and gate leakage under different $V_{d}$. The transistor switches ON at $-0.6$ V. The gate leakage exhibits negligible increment at $V_{d} = 0.1$ V, which is caused by the reduced reverse voltage with lower $V_{d}$. The device shows negligible hysteresis of 6 mV, and the SS approaches the thermal limits of 60 mV/dec in almost all the subthreshold region (Fig. 4G). We also investigate the effect of MoS$_2$ thickness on device SS (Fig. 4H). The device with MoS$_2$ thickness less than 9 nm shows a stable SS below 70 mV/dec. Figure 4I is the output characteristic of the device in Fig. 4D. Compared to the Au S/D one without doping, the output current increased by over 20 times to 1.5 $\mu$A/µm. The Schottky barrier at the Au/MoS$_2$ interface still retains after the doping process, showing non-linear characteristics at the low $V_{d}$ region. We summarize the key parameters compared with previous 2D JFET, as shown in table S1.

Figure 5A shows transfer curves of TMGFET with different back-gated voltages of $-20$, $0$, and $20$ V. The SS under different back gate bias is given in fig. S13. The bottom gate voltage can be further reduced with gate dielectric layer with high capacitance. Figure S14 shows the transfer characteristics with 5/70 nm Al$_2$O$_3$/Polymethyl methacrylate (PMMA) gate dielectric layer, in which the back-gated voltage can be reduced to ±2 V. The turn-off voltage shifts to the negative direction when positive back-gated voltage (+20 V) is applied.
applied. When the back-gated voltage changes from -20 to 20 V, the OFF-state current for the thick sample (11.5 nm thickness, red curve) increase from $3.3 \times 10^{-12}$ to $8.0 \times 10^{-10}$ A; for the thin sample (3.4 nm thickness, blue curve), the OFF-state current remains almost unchanged. At the same time, the ON-state current for the thick sample increases from $6.7 \times 10^{-7}$ to $1.7 \times 10^{-6}$ A; for the thin sample, its ON-state current increases from $1.7 \times 10^{-11}$ to $3.2 \times 10^{-8}$ A. These thickness-dependent characteristics are resulted from the fact that the TMG electrostatic control is limited by Debye length from top surface (14). By coupling with back gate from bottom surface of MoS$_2$, it allows more efficiently electrostatic gate control and even logic computing functions within one single transistor.

We can denote the top TMG voltage as IN A and back-gated voltage as IN B. The high- and low-output current are defined as OUT 1 and OUT 0, respectively. The thickness-dependent responses enable different logic operations. Figure 5B is a demonstration of OR and AND logic with a single transistor. The input signals of the IN A and IN B are shown in the above panel. The thick sample (11.5 nm) exhibits OR function, while the thin (3.4 nm) sample shows a AND function. Figure 5 (C and D) is the graphical demonstration of the OR and AND logic operation, where red and blue represent the ON and OFF states, respectively.

Figure 5E compares the device working mechanisms of the logic operation. When negative back gate voltage is applied to the thin device, the back gate almost depletes the entire channel regardless of the top gate voltage. For the thick device, the top gate can still tune the depletion region to control the conductivity. When positive back gate voltage is applied to the thin device, the top gate can modulate the depletion region. However, the depletion region of the thick device cannot cut off the accumulation layer away from the Debye length, thus making the device conductive regardless of the top gate voltage.

In summary, we develop a fabrication process by transferring metal gate electrodes to 2D semiconducting channel, which eliminates the use of vacuum and high-temperature process typically for preparing FETs. We also design and adopt a SAL to optimize the TMG/MoS$_2$ interface. Our experimental results and DFT calculation verify that the increase of the contact distance can reduce Fermi level pinning and metal-induced gap state. The TMGFETs show the level pinning and metal-induced gap state. The TMGFETs show the effect is of great importance.

Cross-sectional TEM sample preparation and characterization
A MultiBeam SEM-FIB system (JIB-4501, JEOL) was used for the cross-sectional sample preparation, operating using 30-keV Ga$^+$. TEM and STEM characterization was performed on a JEOL JEM-2100F TEM/STEM operated at 200 kV, equipped with an Oxford INCA Energy Dispersive Spectroscopy (EDS) detector and a Gatan Enfina Electron Energy Loss Spectroscopy (EELS) spectrometer for elemental mapping. EELS spectrum imaging was conducted in STEM mode with a 13-mrad convergence angle. The high-resolution STEM image was acquired from an aberration-corrected JEM-ARM200CF TEM/STEM.

DFT simulations
Theoretical calculations were performed using Vienna Ab initio Simulation Package code (5.4.3) with exchange-correlation energy functional, which were modeled by Perdew-Burke-Ernzerhof functional (28–32). The cutoff energy for Pt-MoS$_2$ FET-like junction was set to be 520 eV, and all structures were relaxed to an energy convergence of $10^{-4}$ eV/atom and a force convergence of 0.02 eV/Å, respectively. The k points for Pt-MoS$_2$ junction was $3 \times 3 \times 1$ in slab optimization and $5 \times 5 \times 1$ in static calculation. vdW-DF2 correction was applied to make a correction to the interfacial vdW bonding (29). The interfacial interaction between metallic Pt and MoS$_2$ was investigated by setting different interface separation distances of 3, 5, 7, 9, and 11 Å, respectively. The thickness of vacuum in all the models was set to 20 Å to eliminate the interactions between the layers caused by the periodic boundary condition.

SUPPLEMENTARY MATERIALS
Supplementary material for this article is available at https://science.org/doi/10.1126/sciadv.abf8744

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