Etching-dependent reproducible memory switching in vertical SiO$_2$ structures

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Vertical structures of SiO$_2$ sandwiched between a top tungsten electrode and conducting non-metal substrate were fabricated by dry and wet etching methods. Both structures exhibit similar voltage-controlled memory behaviors, in which short voltage pulses (1 $\mu$s) can switch the devices between high- and low-impedance states. Through the comparison of current-voltage characteristics in structures made by different methods, filamentary conduction at the etched oxide edges is most consistent with the results, providing insights into similar behaviors in metal/SiO$_2$/metal systems. High ON/OFF ratios of over $10^4$ were demonstrated.

Resistive switching materials have been studied intensively as candidates for non-volatile memories. A metal/insulator/metal (MIM) sandwich structure is usually adopted, with "M" extending to good conducting non-metals. Many oxides such as TiO$_2$, NiO, Nb$_2$O$_5$, SrTiO$_3$, and perovskites have been investigated and shown to have voltage- or current-controllable bistable low-impedance (ON) and high-impedance (OFF) states. One oxide, SiO$_2$, can work as a solid electrolyte in a metal-doped switching system. Meanwhile, the amorphous form of SiO can exhibit memory phenomena. Various models have been proposed to account for the switching behaviors, such as ion injection, a filamentary model, and defect introduction by vacancies.

In this letter, we report reproducible resistive switching behaviors in M/SiO$_2$/M vertical structures, fabricated by either wet or dry etching methods. We find that the switching in our system apparently happens at the vertical edges produced by the etching process. This constrained conduction path, dependent on the etching methods, can lead to an ON/OFF ratio exceeding $10^4$, an order of magnitude larger than that achievable in M/SiO/M systems. The particular current-voltage (I-V) characteristics in structures produced by different etching methods provide further insights into the underlying filamentary character of conduction in SiO$_2$ switching systems.

Structures with two different oxide growth methods were examined. SiO$_2$ with a thickness of 50 nm was grown by (1) thermal oxidation of a silicon substrate and (2) plasma-enhanced chemical vapor deposition (PECVD) on a TiN/Si substrate (TiN was deposited by physical vapor deposition (PVD) on Si). Likewise, vertical M/SiO$_2$/M structures were fabricated by two different approaches. In the first approach, a lift-off process was used to define circular tungsten (W) electrodes (by sputtering, with 5 nm-thick Ti adhesion layer) having thicknesses of 100 nm and diameters of 50 $\mu$m. 10:1 buffered oxide etch (BOE, J. T. Baker) was used to remove the surrounding SiO$_2$, leaving the layer underneath the W electrode protected (device type 1 or DEV-1, see inset in Fig. 1a). In the second approach, reactive ion etching (RIE) was used to define the vertical sandwich structures. 10 nm of TiN and 100 nm of W were first deposited on SiO$_2$ by PVD. A 70$\times$70 $\mu$m$^2$ photoresist area was then patterned by photolithography and used as the sacrificial mask. Corresponding etching recipes (e.g., SF$_6$/BCl$_3$/Cl$_2$ for W etching; BCl$_3$/Cl$_2$ for TiN etching; and CF$_4$/CHF$_3$ for SiO$_2$ etching) were used with the layered structure underneath the photoresist protected, thereby forming the vertical structure (DEV-2, see inset in Fig. 2a). A several-minute annealing at 600 $^\circ$C in an Ar/H$_2$ environment was performed before electrical characterizations. Measurements were done using an Agilent 4155C semiconductor parameter analyzer under a single sweep mode. Bias voltage was applied by a probe tip at the top W electrode with the conducting substrate grounded. All data was collected in vacuum (10$^{-2}$ mTorr) at room temperature, unless otherwise specified.
FIG. 2: (Color online) (a). A set of I-Vs by forward and subsequent backward sweeps in DEV-2, with black (bottom), red (middle), and blue (top) curves corresponding to sweep bias ranges of 0-10, 0-8, and 0-6 V, respectively. Inset is a device schematic. (b). A series of reading the device state by bias ranges of 0-10, 0-8, and 0-6 V, respectively. Inset is a red (middle), and blue (top) curves corresponding to sweep subsequent backward sweeps in DEV-2, with black (bottom),

The device undergoes OFF-state changes by applying erasing pulses (1 μs) of different magnitudes of +10 V, +8 V, and +7 V (with the writing pulse +4 V unchanged) as shown correspondingly in the upper panel.

Fig. 1a shows the typical I-Vs in a formed DEV-1 device under a forward (0→8 V) sweep and then a backward (8→0 V) sweep of the top electrode relative to the bottom one. The forward sweep features a high-impedance state at low bias (region "I" in Fig. 1a), with a sudden current jump at ~3.3 V and then a sudden drop at ~5 V back into a high-impedance state. The backward sweep, from high bias back toward 0 V, shows a low-impedance state at region "I". This hysteretic behavior results from a voltage-controlled resistance change in the higher bias (writing) range (region "II" in Fig. 1a), indicated by the sudden rise in current during the forward sweep. A rapid falling edge of voltage in this region can write the device into a conductance state corresponding to this ending voltage [3]. For example, a rapid voltage drop at 4 V writes the device into an ON state, while one at 8 V erases the device into OFF. The obtained state can be read out at the low bias region "I" without being destroyed, allowing the structure to act as a non-volatile memory device. Pulses as narrow as 1 μs (limited by instrumentation) were applied to read, write and erase the device (Fig. 1b), with an ON/OFF ratio over 10^4 achieved. The memory states are stable against reading, showing no degradation in ON- or OFF-state conduction after 1000 read operations.

Similarly, Fig. 2a (black curves) shows the typical hysteresis I-Vs in DEV-2 devices with bias sweeps as described above. Compared to those in Fig. 1a from the DEV-1 device, the I-Vs here have (1) higher ON and OFF currents and (2) comparatively smooth current changes in the writing region. The conductance change in this region, without a drastic rise or drop, means that the conductance state of the device can be changed semi-continuously by applying bias pulses of different amplitudes. The color curves in Fig. 2a show how different bias sweep ranges (thus different final writing voltages) change the conduction states of the device. Decreasing of the sweep range leads to a gradual decline in the ON/OFF ratio because of an increasing current in the OFF state set by the reduced final bias (the ON current tends to increase at a rate much smaller than that of increase in the OFF current). The writing region tends to shift toward low bias, indicated by the shift of the current-rise edge in the forward sweep. A multilevel or analog memory [8, 14] is demonstrated in Fig. 2b by applying erasing bias pulses of different amplitudes. The adjustable ON/OFF ratio is less than 10^3 due to comparatively large OFF currents.

To clarify where the switching takes place in these vertical devices, W or W/TiN electrodes with the same thicknesses and sizes were deposited on the (PECVD) SiO_2/TiN/Si substrate, without doing any etching of the oxide (see left schematic in Fig. 3a), or on wet-etching defined SiO_2 pillars of larger diameter on the (thermal) SiO_2/Si substrate (see right schematic in Fig. 3a). The samples were annealed under the same conditions as those adopted for the previous structures and then characterized via electrical measurements. No conduction was observed up to a bias of 25 V (~10^{-12} A). Devices with different diameters (25 μm, 50 μm, and 100 μm) were also made and the ON currents were collected for DEVs-1 and another type of wet-etching defined W/Ti/(PECVD) SiO_2/TiN/Si devices (DEVs-3, see schematic in Fig. 3b). For both DEVs-1 and DEVs-3, the ON currents scale approximately with the diameter (black dashed lines in Fig. 3d-e) rather than with the device area (red dotted lines in Fig. 3d-e). These results imply that conduction and switching only take place after the etching and are likely localized at the vertical SiO_2 edges. The I-Vs of DEVs-3 tend to have features combining attributes of DEV-1 and DEV-2. DEVs-3 typically have higher ON and OFF currents than those in DEV-1, but lower than those in DEV-2 (at the same bias sweep ranges). The forward sweep still begins with a sudden current rise in the writing region, but then follows a less intense declining tail. Fig. 3c shows three forward I-Vs from each of the three types of devices. We suspect that surface differences resulting from etching methods and oxide growth techniques are responsible for this variation.

The surface nature of the conduction is further supported by the response of devices to annealing in a reducing atmosphere. A several-minute thermal annealing at 600 °C in Ar/H_2 was necessary to observe the switching in wet etched devices. Before annealing, a majority (over 80%) of the devices was non-conducting (e.g., I~10^{-12} A at a bias up to 25V). Detectable conduction began to take place after the thermal annealing in the reducing environment. An electroforming process takes place by sweeping to high voltages (e.g., 20 V). Large current fluctuations gradually move toward lower bias voltages in subsequent sweeps. Finally, reproducible forward I-Vs as described previously are established. For the devices fabricated by dry etching (DEV-2), a similar forming process can take
Our other tests show that the switching and forming processes here. All the observed characteristics resemble those in generally have higher ON currents than those observed with non-metallic substrates of either Si or TiN/Si, metal ion migration or injection from the electrode, which would lead to the comparatively smooth I-V in DEV-2 due to a variety of current rise and drop edges. The I-V of DEV-3 in Fig. 3c is consistent with this idea, with an intermediate conductance device DEV-3 having features between the two limits of DEV-1 and DEV-2.

It is straightforward that a large number of paths with non-uniform writing/erasing biases would limit the overall ON/OFF ratio, while reducing the path number can push this ratio up, as demonstrated in DEV-1 with an ON/OFF ratio > 10^4. Currently the device size is limited due to our instrumentation (e.g., the size of probe tip for measurement). The variation in ON currents for devices with the same nominal sizes (see Fig. 3d-e) implies that the switching likely takes place locally at some parts of the SiO_2 vertical edge instead of uniformly along the entire circumference. It is thus expected that the device size could be further reduced, even down to one comparable to the actual switching region, which could be small due to the filamentary nature. Devices can have OFF currents at the noise level of our instrumentation ~ 10^{-12} A, giving an ON/OFF ratio approaching 10^6 even at the current device size. These traits indicate the possibility of high-density memory arrays based on this switching.

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15. See EPAPS Document No. *** for resistance-temperature figures and switching in a device with on-off ratio approaching $10^6$. A direct link to this document may be found in the online article’s HTML reference section. The document may also be reached via the EPAPS home-page [http://www.aip.org/pubservs/epaps.html] or from ftp.aip.org in the directory /epaps/. See the EPAPS home-page for more information.
Supplementary material for “Etching-dependent reproducible memory switching in vertical SiO$_2$ structures”

Due to space limitations in the main manuscript, here we show two supplemental figures that provide further information about the experiments.

FIG. S1: $I−V$ s measured at different temperatures for four individual DEVs-3 (D = 50 $\mu$m). The devices were set at different conducting states, from high to low (a→d). They indicate little temperature dependence for the conduction down to 100 K.
FIG. S2: Memory-state readings of a DEV-1 ($D = 25 \, \mu m$) by applying bias pulses of +1 V ($1\, \mu s$). The device was either written into an ON state by a (+5 V, 1 $\mu s$) pulse or erased into an OFF state by a (+10 V, 1 $\mu s$) pulse after every five readings. It shows that the OFF currents are at the noise level of our instrumentation ($10^{-12}$ A) and an ON/OFF ratio approaching to $10^6$. 