Automated Design Space Exploration of CGRA Processing Element Architectures using Frequent Subgraph Analysis

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Abstract—the architecture of a coarse-grained reconfigurable array (CGRA) processing element (PE) has a significant effect on the performance and energy efficiency of an application running on the CGRA. This paper presents an automated approach for generating specialized PE architectures for an application or an application domain. Frequent subgraphs mined from a set of applications are merged to form a PE architecture specialized to that application domain. For the image processing and machine learning domains, we generate specialized PEs that are up to 10.5× more energy efficient and consume 9.1× less area than a baseline PE.

I. INTRODUCTION

Coarse-grained reconfigurable arrays (CGRAs) have been widely studied in recent years and serve as a midpoint between the flexibility of an FPGA and the performance and energy efficiency of an ASIC [15]. A CGRA can achieve better performance and energy efficiency than an FPGA because its processing elements (PES) have specialized arithmetic units that operate at a word-level, rather than a bit-level, granularity. They have better reconfigurability than an ASIC due to a flexible interconnect and configurable PEs. However, CGRAs do not constitute just one point in the spectrum between FPGAs and ASICs; rather, they occupy a large design space from specialized and efficient CGRAs to flexible CGRAs that can accelerate many applications. CGRAs are useful when designed with an application domain in mind, allowing for appropriately specialized PE and memory architectures while leaving some flexibility to accommodate the evolution of the applications in the domain.

The design of CGRA PEs has a direct and significant effect on application mapping and CGRA power, performance, and area while also having an indirect effect on the CGRA interconnect. In traditional island-style FPGAs, a significant portion of the die area is dedicated to interconnect and configuration [6]. CGRAs reduce this overhead by increasing compute density [15]. To achieve even higher compute density, design space exploration (DSE) of specialized CGRA PE architectures is required.

In this paper, we present a methodology for the design space exploration of CGRA PEs. Our methodology is based on analyzing applications within an application domain to find common computational blocks that can be easily accelerated with specialized PEs. Using this methodology, we explore the space between general CGRAs that can execute many applications and specialized CGRAs that execute a more limited set but achieve high performance and energy efficiency.

Our framework encompasses application analysis, PE specification, CGRA hardware generation, and compiler creation in an easy-to-use toolchain that requires very little manual effort. Given an application or a set of applications, the framework can produce many PE architectures that explore the design space along with the rest of the CGRA and the compiler to evaluate the PE designs. Our contributions are as follows:

1) Develop a methodology to analyze applications using subgraph mining and generate candidate PEs specialized for those applications using subgraph merging.
2) Automatically generate CGRAs with specialized PEs along with a compiler to run applications on those CGRAs utilizing an agile hardware flow.
3) Evaluate the area, energy, and performance of a CGRA running a variety of applications using PEs specialized to those applications or application domains.

The rest of this paper is organized as follows: Section II introduces the design space axes of CGRA PEs. Section III describes our application analysis and PE specialization methodology. Section IV presents our DSE framework. Finally, Section V demonstrates the efficiency improvements obtained by specializing PEs using our framework for image processing and machine learning (ML) domains.

II. PROCESSING ELEMENT DESIGN SPACE

A survey of existing CGRA PE architectures indicates the presence of three design spaces axes [14] — the number and type of operations within the PE, the interconnect of the PE, and the number of inputs to and outputs from the PE (Fig. [I]).

A. Number and Type of Operations

CGRA PE architectures contain arithmetic units that can execute a number of operations, enabling a wide variety of applications to run on the CGRA. Typically, each PE contains at least one arithmetic unit that implements a handful of primitive operations such as add, subtract, shift, and comparisons. In addition, PEs may contain a multiplier and logic unit that...
can do bit operations. At one end of this design space axis are the most general PEs that contain one ALU and one multiplier. An example is the MorphoSys CGRA PE shown in Fig. 1(b). This type of design lends itself to high utilization and similar efficiency no matter the application running on the CGRA. On the other end of this design space axis are more specialized PEs that have multiple ALUs or multipliers. For example, CGRAs targeting image processing or ML are likely to have the ability to do a vector multiply-add operation. Some complex PEs contain floating point logic that, while expensive, can enable running a wider range of applications.

B. Intraconnect

The number of configurable paths through a PE affects its area and power, as well as generality. A PE that can be configured to do a larger number of operations and more complex operations will have higher area and power, but it may require far fewer PEs to map to an application. On one end of this axis are PEs that have very few configurable paths. Since CGRA PEs can execute more than one operation, at least one multiplexer is needed to route the desired operation to the PE output. On the other end of this axis are PEs that have many multiplexers that enable many different configurable paths through the PE. A common example of this is to have multiplexers at the inputs of each arithmetic unit. Each input to the PE can be routed to either input of the ALU, so non-commutative operations like shifts can be achieved regardless of the order of the operands into the PE.

C. Number of Inputs and Outputs

The number of inputs and outputs (I/O) to each PE directly affects the size and number of connection boxes (CBs) and switch boxes (SBs) in the CGRA. The CBs take inputs from the routing tracks and feed them into PEs, while the SBs take outputs from the PE and route them to other PEs. As these components of the interconnect have high area and power costs, minimizing the I/O to the PE is critical for achieving an efficient CGRA. On one end of this design space axis are PEs that have two inputs and one output (Fig. 2(a)). This enables most arithmetic operations and results in small per-PE interconnect overhead. On the other end are designs that have many inputs to enable more complex operations, for example, a three input operation like a fused multiply add (Fig. 2(c)).

III. APPLICATION ANALYSIS

All three design space axes described in Section II have many potential values, thus a naïve exploration of the design space would lead to many candidate PEs. An intelligent method for exploring this design space and selecting interesting candidate PEs is needed for efficient exploration. In this section, we introduce our application analysis methodology, which is based on frequent subgraph mining and analysis.

A. Subgraph Mining

We start with an application written in Halide, a domain-specific language (DSL) for image processing and machine learning. We use the Halide compiler from [2] to lower the application to a CoreIR dataflow graph containing compute and memory nodes. Since the compute nodes are primitive operations such as add, multiply, etc. and the edges are connections between those operations, frequent subgraphs of the application represent common (potentially complex) operations in the application. We use the frequent subgraphs as a starting point for constructing interesting PEs.

Finding, or mining, frequent subgraphs relies on the computation of subgraph isomorphisms which is an NP-complete problem. As frequent subgraph mining is very useful in a wide variety of fields, this is a well-researched problem. We use GRAMI, a subgraph mining tool for single large graphs.

GRAMI takes the application graph as an input in addition to a minimum number of times a subgraph can appear to be considered frequent. Fig. 3 gives an example of frequent subgraph mining for a simple application. Fig. 3a shows the CoreIR graph representation of a convolution 

\[ \left( (i0 * w0) + (i1 * w1) + (i2 * w2) + (i3 * w3) \right) \] 

Some frequent subgraphs of this application are in Fig. 3b, 3c, and 3d. A subgraph of a CoreIR application can be interpreted as a PE architecture. Each operation in the subgraph has
a hardware interpretation, so constructing PEs from many different subgraphs can be easily automated. However, not all frequent subgraphs are as interesting as they initially seem. Fig. 3d is an example of such a case. While the frequency is four, the occurrences overlap, and therefore, only two of the occurrences can be effectively accelerated. We use maximal independent set analysis to mitigate this issue.

B. Maximal Independent Set Analysis

Subgraphs that overlap in the application graph cannot be accelerated with fully utilized PEs that have the architecture to accelerate that subgraph. Fig. 3d shows a frequent subgraph of a convolution application. This subgraph has many occurrences in the application graph, although several of these occurrences overlap. If a PE had the architecture of this subgraph and was used to accelerate this application, it would result in underutilized PEs.

One method to find when this problem occurs is maximal independent set analysis [3], which uses the following steps:

1) Represent each occurrence of the subgraph in the application as a node in a new graph.
2) Represent overlapping subgraphs as edges between nodes. Overlapping subgraphs are those whose occurrences share any node.
3) Calculate the maximal independent set of this new graph; the size of this set is the number of times the subgraph exists in the application without overlaps.

An independent set of a graph is a set of vertices in that graph which do not share a neighbor. A maximal independent set (MIS) is an independent set which cannot be grown by adding more vertices to it. The size of MIS represents the number of fully utilized PEs with the architecture derived from the subgraph that can be used to run the application.

Fig. 4 illustrates this on a simple application graph using the subgraph from Fig. 3d. The first occurrence of the subgraphs is outlined in blue in Fig. 4a, the second in red, the third in green, and the fourth in yellow. Each of these occurrences has a corresponding node in Fig. 4b. The maximal independent set is the set of nodes that are filled with their respective color (yellow and blue). In this example, MIS size is 2, meaning this subgraph occurs twice in the application graph not including overlapping occurrences. The MIS size of a subgraph indicates how many fully utilized PEs that implement this subgraph can be used to accelerate the application. Using the size of this set, we have a better idea of which application subgraphs might be interesting starting points for PE architectures.

C. Subgraph Merging

Merging many subgraphs from one or more applications allows for the acceleration of multiple distinct parts of one application or even multiple different applications using one PE architecture. However merging subgraphs is not a trivial problem. We have taken inspiration from a set of algorithms designed for high level synthesis for automated datapath graph merging [7]. The goal of these algorithms is to create a single structure that implements all of the distinct operations in the subgraphs with minimal area overhead. It produces one datapath that can be configured to each of the operations of each of the subgraphs. As an example, Fig. 5a and Fig. 5b show two subgraphs that we want to merge together.
The first step in the subgraph merging process is to create a set of potential merging opportunities between nodes of the same operation in each subgraph. Fig. 5c shows a bipartite graph with nodes and edges in subgraph A on the left, and nodes and edges in subgraph B on the right. An edge from one node on the left to one on the right represents a potential merging opportunity. Two nodes can be merged if they are either the same operation, or can both be implemented on the same hardware block. Two edges can be merged if each of their endpoint nodes can be merged and the ports on the destination node match. Nodes and edges which do not have any potential merging opportunities in this example have been omitted from Fig. 5c for simplicity.

In this example, nodes a0 and b0 are both constants, so there is a corresponding edge in the bipartite graph. Nodes a1, a2, b2, and b3 are all add operations, so there are corresponding edges between these nodes. Finally, the edge a2 → a1 and the edge b3 → b2 start at an add operation and end at an add operation, and the ports on both a1 and b2 match, so those edges can be potentially merged as well.

Next, these potential merging opportunities are transformed into a compatibility graph, where each potential merging is represented as a node, and each compatible merging is represented as an edge. Merging opportunities are compatible if they can both be implemented at the same time. Two mergings are incompatible if they merge one node in subgraph 1, to more than one nodes in subgraph 2, or vice versa. For example, merging a1/b2 is incompatible with merging a2/b2.

Each node in the compatibility graph is given a weight, w, corresponding to the area reduction associated with applying the given merge. This area reduction is calculated by synthesizing the primitive nodes used in the subgraphs and calculating their area. For example, node a1/b2 represents merging a1 with b2. If this merging were applied, the resulting merged subgraph would only contain one adder for both of these nodes. The area reduction associated with this is the area of one adder.

To find the merging with the lowest area overhead, the maximum weight clique of this compatibility graph is calculated. The maximum weight clique of a graph is the set of fully connected nodes which have the largest sum of weights. In Fig. 5d the maximum weight clique is the set of nodes highlighted in blue. Using the maximum weight clique of the compatibility graph, the lowest cost merging of the two subgraphs can be reconstructed. This resulting merged graph is shown in Fig. 5e. Note that a multiplexer is added to enable multiple paths from nodes a0 to a1 and b1 to b2.

While this technique allows for efficiently merging frequent subgraphs from an application, there is still the question of which and how many subgraphs to merge. We can use the maximal independent set analysis to first identify the most interesting subgraphs mined from the application. The mined subgraphs are ranked by MIS size so that subgraphs that have many overlapping occurrences are considered last. Then we can use the number of subgraphs merged together as a tuning knob to adjust the specialization of the PE to the target application(s). This allows for automated design and generation of PEs, while still allowing the designer to control the generality and specialization of the CGRA.

### IV. DESIGN SPACE EXPLORATION FRAMEWORK

We build on top of an existing open-source agile hardware design flow [3] to create specialized CGRAs with PEs generated from our application analysis. Our overall DSE framework is shown in Fig. 6. Fig. 7 shows the high-level architecture of the CGRAs we generate. The CGRA contains an array of PE and memory (MEM) tiles connected through a statically configured interconnect containing horizontal and vertical routing tracks.

Our DSE framework (Fig. 6) has the following steps:
1. We start with applications from a domain written in Halide [10], a DSL for succinctly describing image processing and machine learning applications.
2. The Halide compiler from [2] converts the Halide application into a dataflow graph in CoreIR [4].
3. The application analysis flow (Section III) performs subgraph mining and maximal independent set analysis and generates an ordered list of frequent subgraphs.
4. Subgraph merging merges several frequent subgraphs to generate a candidate PE graph, which we automatically convert into a PE specification in PEarl [2] DSL.
5. The PEarl compiler generates the PE Verilog and the rewrite rules required by the application mapper. The PE RTL is fed into CGRA RTL generation to generate the final CGRA hardware.
6. Meanwhile, the application mapper, using the rewrite rules, generates a covering of the application CoreIR graph using PEs, while trying to minimize the number of PEs used. Depending on its architecture, a PE can...
execute a single operation or a small graph of operations. The result is a graph of PEs and MEMs.

7) From this mapped graph, we generate the CGRA configuration bitstream and simulate the CGRA RTL using Synopsys VCS.

8) Finally, we synthesize the CGRA Verilog in TSMC 16 nm technology and evaluate area and power for the PE and the CGRA using Synopsys Design Compiler and Synopsys PrimeTime PX.

V. RESULTS

This section presents the improvements we achieve by exploring the PE design space and specializing the PE architecture for a specific application or an application domain. Fig. 7 shows the architecture of the baseline PE from 2 that we compare with. It contains an integer arithmetic unit and can perform bit operations using a look-up table (LUT). It is a very general PE that can execute most applications and is not specialized for any particular domain. Using our framework, we generate the following PE variations for each application by indicating which subgraphs are merged together:

- PE 1: The first PE variation is the baseline PE but with only the operations necessary for the application.
- PE 2: The second variation merges the subgraph with the largest maximal independent set with PE 1.
- PEs 3 - 5: Further variations additionally merge other subgraphs into the PE architecture in the order of their MIS size. The last variation for an application is the most specialized PE possible without increasing area or energy.

A. DSE for Image Processing Applications

We focus on specializing across four imaging processing applications: Harris corner detection, Gaussian blur, camera pipeline and Laplacian pyramid.

We first analyze camera pipeline, which is the most complex application of the four. It uses all the operations in the baseline PE except for left shift (SHL) and bitwise logical operations (LUT) and needs 221 operations to compute an output pixel. Fig. 9 shows the most frequent subgraphs and the architectures of the different PE variations for camera pipeline. Fig. 8 shows the energy per operation dissipated by the PE core and total area (PE core area × number of PEs used by the application) of the different PE variants specialized for camera pipeline, swept across different synthesis frequencies. Specializing the PE for camera pipeline results in up to 8.3x and 3.4x less energy and area, respectively, on the CGRA than the baseline PE. Performance also benefits from specialization; the baseline PE has a maximum frequency of 1.43 GHz while the camera pipeline-specific PEs can operate up to 2 GHz.

Further, by merging in frequent subgraphs from all four applications we create PE IP, a PE specialized for image processing. In Fig. 10 PE IP supports all four applications, while PE Specialized (PE Spec.) is the most efficient PE created for the particular application (i.e. one of PEs 3-5). Optimizing the PE for all image processing applications (PE IP) results in a 29.6% to 32.5% decrease in PE area and 44.5% to 65.25% lower energy across all four applications. PE Spec. typically yields more benefits than PE IP; targeting the CGRA only for Laplacian pyramid, for example, further decreases area and energy from PE IP by 38.6% and 33.0%, respectively. It is interesting to note that PE IP is more energy-efficient than PE Spec. for Harris; in this instance PE IP has an architecture that reduces activity on an input to a multiplier. In general though, PEs from cross-application analysis are worse
Fig. 11: Normalized energy and area for ML kernels run on a PE specialized for ML (PE ML) and a PE specialized for the particular kernel (PE Spec).

![Diagram showing energy and area comparison]

Table I: Comparison of ML CGRA with an ASIC (Simba) and a generic CGRA.

| Tech. | PE Vector MACs Baseline PE ML |
|-------|-----------------------------|
| MHz   | 161-2001                    | 16nm |
| pJ/op | 0.105-2.15                  | 909   |

| Tech. | PE ML |
|-------|-------|
| MHz   | 16nm  |
| pJ/op | 2.25  |

VII. CONCLUSION

We have presented a design space exploration framework that allows for automated specialization of CGRA PEs to an application or an application domain, enabling the creation of complex, high-performance PEs that lower overall energy and area costs. We demonstrate that specializing PEs results in up to 9.1× and 10.5× reduction in area and energy, respectively, across a variety of image processing and machine learning applications, and a CGRA with specialized PEs approaches the efficiency of a domain-specific accelerator.

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