The paper proposed a simple and novel approach to fabricate Fin-On-Oxide (FOO) FinFETs on silicon (Si) substrates for improved electrical characteristics in scaled devices. Based on conventional bulk-Si FinFET integration flow, a special step of a fin notch etching is performed, followed by a process of liner oxidation and isolation-oxide filling and recess. The fin above the notch is physically isolated from the substrate and turns into a self-aligned FOO structure. The fabricated p-type FOO FinFETs have demonstrated excellent short-channel effect (SCE) characteristics with subthreshold slope (SS) of 69 mV/dec and drain-induced barrier lowering (DIBL) of 22 mV/V for a physical gate length (Lg) of 27 nm. For 14 nm devices, SS of 86 mV/dec and DIBL of 106 mV/V have been achieved, which are much better than those of the bulk-silicon FinFET counterpart with similar process. Meanwhile, the steady threshold voltage (Vth) shifting by the substrate biasing is realized in the FOO FinFET without performance degradations. The linearity of the Vth on the bias voltage is ~6 mV/V. The self-aligned FOO-FinFET with a simple process provides a promising method to improve the SCE immunity as well as provides the multi-Vth operation for the scaled FinFET on Si substrates for future ultra-low power circuit applications.

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With more than 10 years of continuous research and development, bulk-silicon (Si) FinFET has been commonly recognized as one of the most promising device architectures for the mass production of the most advanced CMOS integration circuits.1,2 Due to the multi-gates, such as the double or the triple gates on a narrow fin channel, FinFET has a well-controlled electrostatic integrity in the short channel even with the physical gate length (Lg) below 30 nm. However, the actual fin channel in the normal bulk-Si FinFET is within the fin body tied to the Si substrate. This requires a careful design of punch-through stopper (PTS) doping to suppress the sub-channel leakage current at the bottom of the fin.3,4 The PTS doping also causes carrier mobility degradations and serious threshold voltage (Vth) variability in transistors.5 Different from the bulk-Si FinFET, a FinFET fabricated on the SOI substrate (SOI FinFET) has an isolated fin channel naturally formed by the buried oxide. SOI FinFET has the advantages of simplified integration process, reduced leakage and improved device variability. However, it suffers from a high-cost starting wafer and a series of process issues for integrating the high-voltage or the passive components on SOI substrates. As Lg continuously scaling down, the short channel effect (SCE) and the channel substrate leakage in the transistor become more serious. The FinFETs with the physical isolation fin channels on conventional Si substrates become one of the most interesting research topics for scaling FinFETs technology in the future.

Some papers reported the fabrication process of the advanced isolated structure on Si substrates with a complicated process.6 For the first time, this letter reports a novel approach to fabricate a Fin-On-Oxide (FOO) FinFET on the Si substrate with a small modification on normal bulk-Si FinFET integration process. The fabricated FOO FinFETs with Lg of 27 nm and 14 nm demonstrated improved SCE immunity compared with the bulk-Si FinFET counterpart due to the physically isolated channel. The special Vth shifting effect controlled by substrate biasing like a SOI device is also investigated.

Device Fabrication

The fabrication process of the proposed FOO-FinFET with a small modification on conventional bulk-Si FinFET integration flow is shown in Figure 1. Starting on Si substrate with a well doping process, a general spacer image transfer (SIT) technique is applied for the patterning of fin, followed by a modified silicon etching process on the fin pattern to form a special three-dimensional (3D) fin structure with a pair of notches on fin sidewalls. The special etching process consists of three key steps. In one dry etch chamber, a general anisotropic process by Cl2/HBr plasma mixture is firstly performed for the conventional fin etch (step-I). In next step (step-II), the fin surface is lightly oxidized by the high-pressure oxygen plasma in the chamber, forming a thin layer of oxide (1~2 nm) on the etched Si surface to protect the fabricated Si fin in next etch-step. It is the critical step of the unique process approach, which removes the protective layer of nitride spacers for the formation of notches reported in reference 6 and simplifies the whole process. Subsequently, an isotropic etch by Cl2 plasma is performed to form a pair of notches in the middle of both fin sidewalls (step-III). The fin height of the novel fin is determined by the position of notches on the fin. The lateral recess depth in notches is precisely defined by adjusting a proper dry etch plasma conditions, including time, power, flow rate and pressure. The same and regular patterns on the sea of fins are applied for whole wafer to decrease the etch process variability. The residual Si thickness in the notches is ~10 nm (Figure 1) to physically support the upper fin channels in later process steps.

Next, similar to traditional bulk-Si fin process flow, the thin liner oxidation is carried out on the etched fin surface and the support part in the notches is fully oxidized; subsequently, another oxide layer is deposited and etched back for shallow-trench isolation formation between fins. In this step, the fins above the notches are totally isolated from the substrate, forming the self-aligned fin on oxide structures based on the bulk-Si substrate. Since the top fin is fully physical isolated from the substrate, the junction isolation process including the PTS doping is skipped for the FOO FinFET fabrication. In following steps, the dummy poly-Si gate, the spacers, the source/drain (S/D) doping process and the all-last high Metal Gate (HKMG) process, as well as the metal contact process, are carried out by following the integration scheme of traditional bulk-Si FinFET technology. In these devices, the nanoscale gate length is defined by E-beam lithography. Multilayered HKMG is deposited all by atomic layer deposition (ALD) process with good conformality on fins in narrow gate trenches. A large S/D contact structure is adopted for reducing the contact resistance. For comparison, the reference bulk-Si FinFET with similar process is also fabricated.

Results and Discussion

The final structures of one fabricated p-type FOO FinFET are shown in Figure 2a and Figure 2b. Figure 2a shows the cross sectional
Figure 1. The fabrication process of FOO FinFETs with minor modification on the flow of conventional bulk-Si FinFETs.

TEM image of the fin channel covered by the multilayered HKMG in the FOO FinFET. In this figure, the fin is totally isolated from the Si substrate and supported by the self-aligned oxide at the bottom of the fin. The height of main fin body in FOO FinFET is 38 nm, which is determined by both the fin etch and the liner oxidization process. The fin has a body-tail buried in the oxide with the height of 10 nm. The top width of FOO is 10 nm and it is just a little larger than that (8 nm) of normal bulk Si fin. The effective device width of FOO is 92 nm per fin. Figure 2b shows the TEM image cutting along the fin of the fabricated device with physical gate length of 14 nm. In this device, multi-layered (HfO2/TiN/TaN/TiN/W) HKMG films with all-last replacement gate process are implemented. With the good filling of work-functional layers (TiN) in narrow gate trenches, the extracted effective oxide thickness (EOT) and effective work-function (EWF) of HKMG is about 0.95 nm and 5.03 eV, respectively, which are very similar to those extracted from large area capacitors. Shown in the Figure 2b, the HKMG electrode is deeper in the substrate than the bottom of S/D regions. This is expected to provide a stronger subthreshold leakage control than a conventional structure. The S/D regions beside the gate electrodes are also isolated from the substrate.

The $I_{DS}$-$V_{GS}$ curves of the typical p-type FOO FinFETs with different gate lengths are shown in Figure 3. For the $L_G$ of 27 nm device, although the device has a small driver current due to the large S/D contact resistance on isolated fin structure, the subthreshold slope (SS) and drain-induced barrier lowering (DIBL) are 69 mV/dec and 22 mV/V, respectively. These parameters are better than those of the reference bulk-Si FinFETs with similar process, comparable with those of the state-of-the-art 22/16 nm bulk-Si FinFET technology for mass production (SS = 72 mV/dec and DIBL = 35 mV/V for devices with similar physical $L_G$ in reference 1). While $L_G$ scales to 14 nm, the SS and the DIBL of the FOO device are 86 mV/V and 106 mV/V, respectively. The parameters of the shorter device are some degraded due to stronger SCE in an extremely scaled transistor, resulting in a worse electrical potential integrity. The tendencies of SS and DIBL variations as $L_G$ scaling are shown in Figure 4. In the figure, both FOO FinFETs and normal bulk-Si FinFETs with similar process are summarized. In long channel, the DIBL and SS of FOO FinFET has about 5% improvement in average than those of bulk-Si FinFET since the subthreshold leakage distributed in sub-channels at the bottom of fins are totally removed. In short channel ($L_G < 27$ nm), the parameters of DIBL and the SS in saturation regime are greatly improved. This is because the parasitic effect of the lateral electrical field expanding into the channel at a high drain voltage is reduced due to the increased potential in floating FOO channel. Meanwhile, the subthreshold leakage from the drain junction under high voltage is also decreased due to the removal of the highly doped regions in FOO channels.

On the other hand, the floating potential in the FOO channel is affected by the substrate bias voltage stressed in substrate-well. The mechanism is similar to the back bias effect of a real SOI devices. The minimum thickness of the self-isolated oxide is ~25 nm, similar to the buried oxide thickness in FD SOI devices. The variations of $V_{TH}$ in linear regime with different substrate bias voltages ($V_{BS}$) for 27 nm FOO FinFETs and normal bulk-Si FinFETs are shown in Figure 5. The linear $V_{TH}$ of FOO FinFETs are slightly smaller than that of the reference bulk-Si FinFET due to the lower channel doping while the PTS implantation is omitted in the FOO FinFETs. The fit-lines of different $V_{TH}$s for both devices are also demonstrated in Figure 5a. A series of $I_{DS}$-$V_{GS}$ curves under different $V_{BS}$s for both devices are shown in Figure 5b. Generally, the relationships between shifting $V_{TH}$ and $V_{BS}$s are defined as:

$$V_{TH-VBS-VTH-0} \propto \delta_{bulk-Si} \times (\phi_f + V_{BS})^{1/2} \quad [1]$$

$$V_{TH-VBS-VTH-0} \propto \delta_{SOI} \times (\phi_f + V_{BS}) \quad [2]$$

where the equation 1 is for a bulk-Si device and the equation 2 is for a SOI device. $\delta_{bulk-Si}$ and $\delta_{SOI}$ are body factors for a bulk-Si device and
Figure 4. (a) The DIBL and (b) the SS as the tendency function of gate lengths for FOO FinFETs and normal bulk-Si FinFETs.

Figure 5. (a) The V_{TH} linear control by substrate bias voltages in the FOO FinFET; (b) The shifted I_{DS}-V_{GS} transfer curves under different bias voltages for the FOO FinFETs and the normal bulk-Si FinFETs.

Figure a SOI device, respectively. $\phi_f$ is the Femi level in channel. In Figure 5, while the V_{BS} increasing from $-2.0$ V to 4.0 V, the I_{DS}-V_{GS} curve of FOO FinFETs is shifted to the negative direction due to the increasing channel potential in FOO channels by the back biasing effect. The decrease of the V_{TH} is approximately linearly dependent on the V_{BS} with the extracted linearity of -6 mV/V. Other parameters such as SS and subthreshold leakage have no observable distortions. The results confirmed that the fabricated FOO FinFET is a real SOI device and demonstrates a similar substrate bias effect to a SOI device. In contrast, the relationships between the V_{TH} and the V_{BS} of normal bulk-Si FinFETs are nonlinear and the subthreshold leakage is greatly increased as the rising up of V_{BS}, which is perhaps from a large junction leakage of a big S/D contact region in the experimental devices. These results indicate that the FOO FinFET provides a novel approach for multi-V_{TH} operations with back-gate biasing in nanoscale bulk-Si FinFETs. It provides a promising approach for the fabrication of the ultra-low power circuits with the FinFETs on the Si substrate without introduction of complicate process technologies.

Conclusions

Self-aligned FOO FinFET with a simple process compatible with conventional bulk-Si FinFET flow is reported. With the physically isolated channel on the Si substrate, the new device achieves a better SCE immunity than the conventional bulk-Si FinFET. The steady multi-V_{TH} characteristics by the back biasing provide a
special advantage for FOO FinFETs applying into future ultra-low power circuits.

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