A synchronous driving approach based on adaptive delay phase-locked loop for stitching CMOS image sensor

Zhongjie Guo¹, Ningmei Yu¹, Longsheng Wu²

Abstract A synchronous driving approach for stitching CMOS image sensor is proposed. Dual row signal line driving architecture must be considered in the design of large array CMOS image sensor. However, as the size of the array increases further, the traditional synchronization technologies such as clock tree cannot be applied because of the stitch technology. Furthermore, this invalidity will cause DC shoot through and dead line. Based on the adaptive delay phase-locked loop, dual row signal line synchronous driver for pixel array is realized in a single die CMOS image sensor with 225M pixels and large area of $120 \times 120 \text{mm}^2$. Timing matching improves by two orders of magnitude, and 99.95% consistency is achieved.

Key words: CMOS image sensor, line driving, delay phase-locked loop

Classification: Integrated circuits

1. Introduction

CMOS image sensors are not only widely used in consumer electronic products such as portable digital cameras, mobile phone cameras, hand-held cameras and digital SLR cameras, but also widely used in smart cars, satellites, security, robotic vision and other fields. With the continuous pursuit of high-performance imaging systems for original high-definition images, more and larger array high resolution CMOS image sensors have appeared in the fields of biotechnology, medicine, national defense security and space applications [1-5].

Thanks to the great development of CMOS stitching technology, it provides manufacturing guarantee for the research, design and implementation of super large array CMOS image sensor [6-9]. With the increase of the sensor array size, the length of the row line and the column line through the area array increases, which makes the parasitic parameters of the line increase sharply, resulting in serious challenges to the driving of row line and the read-out time of column line[10,11].

According to the traditional design idea, the dominant factor of the row driving technology will not be proportional to the capacity of the driver, but directly determined by the parasitic signal line under the large area without buffer condition. The larger the array size, the smaller the capacity of the driver. Traditional driving technology can no longer meet the needs of large array [12-17]. Perhaps the frame rate of references is only a few frames, which is closely related to this factor.

For the current optimized column level readout circuit architecture [18-22], the simplest and most direct method is to drive the row signal line of the large array by two ends, which will reduce the time constant of parasitic parameters introduced by the driving line to one quarter of the original [23, 24]. But there is a main problem in this method, that is, the inconsistency of two drivers will cause the DC shoot through phenomenon of driving circuit. The traditional idea is to match the signal phase of two terminals through the clock tree technology in digital circuit design. However, constrained by the stitch technology of large array CMOS image sensor, the repeatability of circuit design makes clock tree technology unusable, which is worse for the already serious large array. Although shoot through can be prevented by adding switches [25], additional line redundancy time is added, which is not conducive to the increase of frame rate. Similar problems arise in time resolved CMOS image sensors and Time-Interleaved ADC, the influence of clock skew on the accuracy of time resolution is very important. To solve this problem, column parallel skew calibration circuits have been proposed and demonstrated its effectiveness [26-28]. A statistics-based background calibration and digital calibration scheme for timing skew is employed in Time-Interleaved Flash ADC [29, 30]. But these methods are not suitable for stitching large array CMOS image sensors.

Aiming at the above problems, this paper proposes an efficient, adaptive and high synchronization dual driver solution for CMOS image sensor with super large array stitch technology based on DLL [31, 32]. This method is not constrained by stitching technology, and can expand the array size arbitrarily to ensure the

¹School of Automation and Information Engineering, Xi’an University of Technology, Xi’an, Shannxi 710048, China
²Xi’an Microelectronic Technology Institute, Xi’an, Shannxi 710054, China

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complete consistency of driving timing on both sides.

2. Circuit description

Fig. 1 shows the synchronous driving principle of the small array CMOS image sensor, which ensures the timing consistency of the dual driving circuit through the clock tree layout technology in the design of digital integrated circuits [33-35]. If this idea is directly applied to the design of large array CMOS image sensor with stitching technology, as shown in Fig. 2. Areas with the same letters are modules that need to be redesigned to meet the need for efficient stitching design and manufacturing. Clock tree technology can be used in the redesigned area on both sides of the array, but the clock signal layout on the lower side of the array cannot be designed by using clock tree because of the requirements of stitching design, which will seriously lead to the difference of clock signals reaching the nodes on both sides of the array. Assuming that the clock delay of the unit stitch block is $\Delta t_d$, the clock difference between the left and right sides of the splice block with $k$ blocks will reach $k \times \Delta t_d$. It can be seen that this difference diverges with the increase of the size of the array, which will be a very serious challenge to the design of large array. At this point, the row period $T_{row}$ must be greater than $n \times \Delta t_d$, the frame frequency of the sensor $f$ is limited to some extent, as shown in the following expression, where $m$ is the number of rows of all pixel array.

$$T_{row} \geq k \times \Delta t_d$$
$$f \geq \frac{1}{m \times k \times \Delta t_d}$$

More seriously, the DC shoot through phenomenon as shown in Figure 3 will occur, which is due to the repeatability design requirements of stitching technology. This problem will not only cause the waste of DC power, but also cause the dead line of pixel array and affect the image quality. Where, the circuit with subscript L is the driving circuit on the left side of the array, and the circuit with subscript R is the driving circuit on the right side of the array, CT is the row driving control signal. For the rising edge of the control signal CT, the right driver will delay $k \times \Delta t_d$ time compared with the left driver. During $k \times \Delta t_d$ time period, the transistor M2L and M1R turn on at the same time, resulting in DC through phenomenon from power supply to ground. Similarly, for the falling edge of the control signal CT, the right driver will also delay $k \times \Delta t_d$ time compared with the left driver. During $k \times \Delta t_d$ time period, the transistor M1L and M2R turn on at the same time, the phenomenon of DC through from power supply to ground appears too.

One easy way to think of is to artificially add delay units on the shorter side of the line to ensure that the delay time on both sides is the same. However, it is
difficult to estimate the difference of time delay between two sides accurately during the design stage. If the readout error is corrected in the test stage, on the one hand, the test cost will increase, on the other hand, the correction can’t adapt to the change of phase difference caused by temperature and external environment. Therefore, an adaptive synchronous driving method proposed in this paper, as shown in Fig. 4. Two delayed phase-locked loops (DLL_L and DLL_R) are used to automatically detect the phase delays on the left and right sides of the driving circuit. The delays to the first input node of the driving circuit on the left and right sides are half the whole period relative to the input signal CT, which effectively ensures the timing consistency on the left and right sides. Where, the region A including the left side Voltage Controlled Delay Line (VCDL) is non-repetitive, and the region B including the right side VCDL is repetitive. Because of the high repeatability of VCDL module design, it is suitable for repeatability design here. Moreover, the effective delay time is exactly half of the period based on the same path.

Fig. 4 proposed synchronous driving approach with stitching technology

3. Experimental results

The synchronous driving approach for stitching design proposed in this paper has been validated in the design of a large array CMOS image sensor, based on 12 inch silicon wafer in a 55nm CMOS process. Fig. 5 shows a large array CMOS image sensor with 225M pixels, in which area A and area B are consistent with those shown in Fig. 2, the top side is the layout of the whole chip, and the bottom side is the layout of the stitching blocks in the lithography plate. The results shown in Fig. 6 are obtained by fully validating the model circuit at the temperature of -55°C to 125°C and process of slow/typical/fast corner. When synchronous driving technology is not used, the timing inconsistency is the worst, reaching about 30ns. After synchronous driving technology is used, the timing consistency is well guaranteed in all cases, and the worst case is within 1ns. This provides a basis for the design of CMOS image sensor with high frame rate and low noise, the performance of the proposed sensor is summarized in Table I.

Fig. 5 Imager array and stitching block map

Table I. the performance of the proposed sensor

| Parameter                                | Value                  |
|------------------------------------------|------------------------|
| Pixel size                               | 7.5μm                  |
| Image size                               | 15360×15360            |
| Chip size                                | 118mm×125mm            |
| Frame rate                               | 10 fps                 |
| Peak QE                                  | >90%                   |
| Full well                                 | 80,000e-               |
| Read noise                               | ≤5e-                   |
| Dark current                             | 10μA/cm²@25°C          |
| ADL                                      | Programmable 12bit/14bit/16bit |
| Conversion gain                          | 13μV/e-                |
| Windowing                                | 64×64                  |
| Output interface                         | 120 channel LVDS       |
4. Conclusion

A high synchronous driving approach for stitching CMOS image sensor with super large array is proposed. The both respective delay phase-locked loop technology is used to detect the timing mismatch between the left and right sides in real time and adjust the phase difference dynamically, so as to ensure the consistency of the driving signal between the left and right sides of the large area array. The circuit design of a 225M pixel CMOS image sensor with super large area array of 120 × 120mm² is validated. It is obvious that timing matching improves by two orders of magnitude, and 99.95% consistency is achieved.

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References

[1] Eric R. Fossom, et al.: A Review of the Pinned Photodiode for CCD and CMOS Image Sensors. IEEE Journal of the Electron Devices Society, 2014, 2(3), pp.33-43
[2] Yonggang Chen, et al.: CMOS Sensor Arrays for High Resolution Die Stress Mapping in Packaged Integrated Circuits, IEEE Sensors Journal, 2013, 13(6), pp.2066-2076
[3] Ryoshei Funatsui, et al.: 133Mpixel 60fps CMOS Image Sensor with 32-Column Shared High-Speed Column-Parallel SAR ADCs, IEEE International Solid-State Circuits Conference, 2015, pp. 112-114
[4] Toshihisa Watabe, et al.: A 33Mpixel 120fps CMOS Image Sensor Using 12b Column-Parallel Pipelined Cyclic ADCs, IEEE International Solid-State Circuits Conference, 2012, pp. 388-390
[5] Andy T. Clark, Nicola Guerrini, Nigel Allinson, et al.: 54mm ×54mm - 1.8Megapixel CMOS Image Sensor for Medical Imaging, Nuclear Science Symposium Conference Record (2008), pp. 4540-4543
[6] Jun Zhu, Donghua Liu, Wei Zhang, et al.: Systematic experimental study on stitching techniques of CMOS image sensors. 2016 EIECE Electronics Express, Vol.13, No.15, pp.1-11
[7] Zhongjie Guo, Ningmei Yu. Design Technology of High Linearity DAC for Large Array CMOS Image Sensor. 2018 IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC)
[8] Jun Zhou; Yijian Chen. A comparative study on the yield performance of via landing and direct stitching processes for 2D pattern connection. Proc. SPIE 9781(2016) 97810T
[9] Y. C. Pai, Charlie Chen, Louis Jang, et al. High-order stitching overlay analysis for advanced process control. Proc. SPIE 7971(2011) 797127
[10] Jiagtao Xu, Wei Li, Kaiming Nie, et al.: A Method to Reduce the Effect on Image Quality Caused by Resistance of Column Bus
[11] M. S. Kim, G. Kim, G. Cho, and D. Kim: Development of a 55 μm pitch 8 inch CMOS image sensor for the high resolution NDT application. J. Instrum., Vol. 11, No. 11, p. P11016, Nov. 2016
[12] Jan Bogaerts, et al.: 105 × 65mm² 391Mpixel CMOS Image Sensor with >78dB Dynamic Range for Airborne Mapping Applications, IEEE International Solid-State Circuits Conference, 2016, pp.114 - 115
[13] Suat U. Ay, et al.: A 76 × 77mm², 16.85 Million Pixel CMOS APS Image Sensor. 2006 Symposium on VLSI Circuits Digest of Technical Papers
[14] Andy T. Clark, Nicola Guerrini, Nigel Allinson, et al.: 34mm ×54mm - 1.8Megapixel CMOS Image Sensor for Medical Imaging. Nuclear Science Symposium Conference Record (2008), pp. 4540-4543
[15] Sh. E. Bohndiek, A. Blue, J. Cabello, et al.: Characterization and Testing of LAS: A Prototype ‘Large Area Sensor’ With Performance Characteristics Suitable for Medical Imaging Applications. IEEE Transactions on Nuclear Science, Vol. 56, No. 5, October 2009, pp.2938-2946
[16] Franyois Roy, Bastien Mandy, Nayera Ahmed, Arnaud Tournier, Guo-Neng Lu. Development of Small-Sized Pixel Structures for High-Resolution CMOS Image Sensors. 2017 2nd International Conference on Image, Vision and Computing, pp.494-500
[17] Mehmet Baygin and Mehmet Karakose: A New Image Stitching Approach for Resolution Enhancement in Camera Arrays. 2015 9th International Conference on Electronics and Electrical Engineering (ELECO), pp.1186-1190
[18] S. Kawahito: Signal Processing Architectures for Low-Noise High-Resolution CMOS Image Sensors. IEEE 2007 Custom Integrated Circuits Conference (CICC), pp.695-702
[19] Shang-Fu Yeh, Kuo-Yu Chou, Hon-Yih Tu, et al.: A 0.66e−rms Temporal-Readout-Noise 3-D-Stacked CMOS Image Sensor With Conditional Correlated Multiple Sampling Technique. IEEE Journal of Solid-State Circuits, Vol. 53, No. 2, February 2018, pp.527-537
[20] Sun-H Hwang, Jae-Hyun Chung, Hyeon-June Kim, et al.: A 2.7-M Pixels 64-nW CMOS Image Sensor With Multicolumn-Parallel Noise-Shaping SAR ADCs. IEEE Transactions on Electron Devices, Vol. 65, No. 3, March 2018, pp.1119-1126
[21] Xiaoliang Ge and Albert J. P. Theuwissen: A 0.66e− rms Temporal Noise CMOS Image Sensor With GM-Cell-Based Pixel and Period-Controlled Variable Conversion Gain. IEEE Transactions on Electron Devices, Vol. 64, No. 12, Dec 2017, pp.5019-5026
[22] Boyu Hu, Yuan Du, Rulin Huang, et al.: A Capacitor-DAC-Based Technique For Pre-Emphasis-Enabled Multilevel Transmitters. IEEE Transactions on Circuits and Systems—II: Express Briefs, Vol. 64, No. 9, Sep 2017, pp.1012-1016
[23] Hirofumi Totsuka, Toshiki Tsuboi, Takashi Muto, et al.: An APS-H-Size 250Mpixel CMOS image sensor using column single-slope ADCs with dual-gain amplifiers. 2016 IEEE International Solid-State Circuits Conference (ISSCC), pp.116-118
[24] Tomohiro Takahashi, Yuichi Kaji, Yasunori Tsukuda, et al.: A Stacked CMOS Image Sensor with Array-Parallel ADC Architecture. IEEE Journal of Solid-State Circuits, Vol. 53, No. 4, April 2018, pp.1061-1070
[25] Soo Takayanagi, et al.: systems, methods, and devices for preventing shoot through current within and between signal line drivers of semiconductor devices. US patent, No: US 8035718B2
[26] Kenta Yasutomi, Yushi Okura, Keiichiro Kagawa, Shoji
Kawahito: A Sub-100 μm-Range-Resolution Time-of-Flight Range Image Sensor With Three-Tap Lock-In Pixels, Non-Overlapping Gate Clock, and Reference Plane Sampling. IEEE Journal of Solid-State Circuits, 2019 Early Access Article.

[27] Lianghua Miao, Keita Yasutomi, Shoma Imanishi, et al. A column-parallel clock skew self-calibration circuit for time-resolved CMOS image sensors. 2015 IEICE Electronics Express, Vol.12, No.24, pp.1-7.

[28] Keita Yasutomi, Takahiro Usui, Sang-Man Han, et al. A 0.3mm-Resolution Time-of-Flight CMOS Range Imager with Column-Gating Clock-Skew Calibration, 2014 IEEE International Solid-State Circuits Conference, pp.132-133

[29] Manar El-Chammas, Boris Murmann. A 12-GS/s 81-mW 5-bit Time-Interleaved Flash ADC With Background Timing Skew Calibration. IEEE Journal of Solid-State Circuits, Vol. 46, No. 4, April 2011

[30] Shafiq M. Jamal, Daihong Fu, Nick C.-J. Chang, et al. A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter With Digital Background Calibration. IEEE Journal of Solid-State Circuits, Vol. 37, No. 12, Dec 2002

[31] Jinseop Noh and Dong-Woo Jee. A DLL based clock multiplier using rotational DCDL and PRNG for spur reduction. 2019 IEICE Electronics Express, Vol.16, No.3, pp.1-8

[32] K. Ryu, et al.: High-speed, low-power, and highly reliable frequency multiplier for DLL-based clock generator. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 24 (2016)

[33] Zhe Ge and Juan Fu: Improve Clock Tree Efficiency for Low Power Clock Tree Design. 2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology

[34] Te-Jui Wang, et al.: Top-Level Activity-Driven Clock Tree Synthesis with Clock Skew Variation Considered. 2016 IEEE International Symposium on Circuits and Systems (ISCAS)

[35] Subhendu Roy, et al.: Clock Tree Resynthesis for Multi-Corner Multi-Mode Timing Closure. IEEE TRANSACTIONS ON Computer-Aided Design of Integrated Circuits and Systems, Vol. 34, No. 4, April 2015, pp.599-602