NEAT: Non-linearity Aware Training for Accurate and Energy-Efficient Implementation of Neural Networks on 1T-1R Memristive Crossbars

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Abstract—Memristive crossbars have emerged as an energy-efficient component of deep learning hardware accelerators due to their compact and efficient Matrix Vector Multiplication (MVM) implementation. However, they suffer from non-idealities (such as, sneak paths) introduced by their circuit topology that degrades computational accuracy. A 1T-1R synapse, adding a transistor (1T) in series with the memristive synapse (1R), has been proposed to mitigate the non-idealities of crossbars. We observe that the non-linear characteristics of the transistor affect the overall conductance of the 1T-1R cell which in turn affects the MVM operation. This 1T-1R non-ideality arising from the input voltage-dependent non-linearity is not only difficult to model or formulate, but also causes a drastic performance degradation of deep neural networks when mapped to such crossbars. In this paper, we analyse the non-linearity of the 1T-1R crossbar and propose a novel Non-linearity Aware Training (NEAT) method to address the non-idealities. Specifically, we first identify the range of network weights, which can be mapped into the 1T-1R cell within the linear operating region of the transistor. After that, we regularize the weights of neural networks to exist within the linear operating range by using iterative training algorithm. Our iterative training significantly recovers the classification accuracy drop caused by the non-linearity. Moreover, we find that each layer has a different weight distribution and in turn requires different gate voltage of transistor to guarantee linear operation. Based on this observation, we achieve energy efficiency while preserving classification accuracy by applying heterogeneous gate voltage control to the 1T-1R cells across different layers. Finally, we conduct various experiments on CIFAR10 and CIFAR100 benchmark datasets to demonstrate the effectiveness of our non-linearity aware training. Overall, NEAT yields ∼ 20% energy gain with less than 1% accuracy loss (with homogeneous gate control) when mapping ResNet18 networks on 1T-1R crossbars.

Index Terms—Deep neural network, memristive crossbar, 1T-1R non-linearity, retraining

I. INTRODUCTION

THE last decade has seen the rise of Deep Neural Networks (DNNs) to solve many real-world problems. Their promising real-world application and growing resource requirements have lead to researchers focusing on dedicated hardware accelerators. As the CMOS digital hardware advancement cannot keep up with the growing computational needs of DNNs [1], Non-Volatile-Memory (NVM) based crossbars have emerged as a compact and efficient realization for performing the Matrix-Vector-Multiplication (MVM) operations of DNNs in the analog domain [2], [3]. Fig. 1 illustrates an $m \times n$ crossbar. Here, a $1 \times m$ input vector of voltages ($V_i$) interacts with a matrix of NVM conductances ($G_{ij}$) to produce the output current $I_j = \sum_{i=1}^{m} V_i \ast G_{ij}$. Hence, the currents from the $n$ columns of the crossbar constitute the output vector of the MVM operation. Especially, 1T-1R NVM crossbars (Fig. 1) have been widely studied since the transistor in series with the NVM device can help mitigate sneak paths and the incorrect programming of the NVM device induced by noise [4], [5].

However, the presence of a transistor in the synapse introduces various non-idealities pertaining to the non-linear I-V characteristics of a transistor. These non-idealities are data-dependent [6] and DNNs when mapped onto such crossbars suffer computational accuracy losses. Most of the previous works [3], [7]–[10] have proposed strategies and frameworks to model and mitigate data-independent non-idealities (primarily resistive non-idealities and NVM device variations) pertaining to 1R crossbar arrays to improve on the accuracy of the mapped DNNs. However, none of these works have proposed methods to mitigate the transistor-induced non-linearities (data-dependent) in 1T-1R crossbars for the weight-to-conductance mapping in an energy-efficient manner. Recent work GenieX [6] provides a neural network based framework to model both data-dependent and data-independent non-idealities for a crossbar array of 1T-1R synapses. However, it lacks transferability to crossbars with different specifi-
izations and requires re-training of the neural network to model the non-idealities. Thus, approaches towards ensuring efficient mapping of DNNs onto 1T-1R crossbars in an energy-constrained environment has not been well explored. This is highly crucial because 1T-1R crossbars are increasingly becoming prospective candidates for deployment in extremely resource-constrained environment such as IoT devices, drones among others.

In this work, we provide a new perspective on the energy-efficient implementation of DNNs on 1T-1R crossbars. Specifically, we focus on the gate-voltage of the transistor, on which the power consumption of a 1T-1R crossbar system is found to largely depend for a given set of analog input voltages. We observe that 1T-1R synapse has approximately linear characteristics when sufficiently high gate-voltage is supplied. However, if the gate-voltage is low (resource-constrained scenario for low power operation), then the synapse starts exhibiting non-linearity. This non-linearity becomes even more pre-dominant when synapses are programmed to higher conductance values. This non-linear characteristic of 1T-1R synapse degrades the accuracy of DNNs when mapped onto crossbars.

To address this problem, we propose a Non-linearity Aware Training (NEAT) technique. Given the gate-voltage and trained network weights, we first compute the range of conductances for linear operation of the 1T-1R cell via SPICE simulations. Based on this range, we force the weight parameters to be within the linear regime. To this end, we train the networks by iterative training consisting of two steps: (1) approximating the trained weight parameters in the non-linear regime to the boundary of the linear regime; (2) re-training the network with modified weights. We repeat these steps so that a greater number of weight parameters can lie in the linear regime. Also, in this work, we propose two gate-voltage settings in order to implement an energy-efficient crossbar. We can set the same gate-voltage across all layers (homogeneous) or different gate-voltage for each layer (heterogeneous) of the DNN. The homogeneous approach results in high energy gains but can incur significant accuracy losses. The heterogeneous setting addresses this problem by searching layer-wise gate-voltage that guarantees a small accuracy drop while achieving energy-efficiency. Both the settings can be applied in NEAT and we show their efficiency through extensive experiments.

In summary, we focus on mitigating the non-linear and data-dependent non-idealities introduced on addition of a transistor to the crossbar-synapses by operating with optimal selection of transistor gate-voltage. We take a device-agnostic approach assuming that the NVM device can be programmed to a given conductance. Once the non-linear effects are countered, one can use the existing methods to counter other data-independent non-idealities, such as interconnect parasitics, NVM device variations, etc. [3], [6], [7]. Thus, our proposed NEAT is complementary to prior works dealing with mitigating or modelling non-idealities in analogous crossbars.

The key contributions of this work are as follows:

- Determination of the maximum permissible value of effective synaptic conductance for linear operation for a given transistor gate-voltage. In essence, our work unleashes gate-voltage as a control knob to limit the non-idealities encountered in a 1T-1R crossbar array while yielding energy-efficiency.
- Propose Non-linearity Aware Training (NEAT) for accurate and energy-efficient implementation of DNNs on 1T-1R memristive crossbar. By using NEAT, we achieve ∼20% energy gain on ResNet18 architecture on CIFAR10, CIFAR100 datasets while having a tolerable accuracy loss (∼1%).

II. Background and Preliminary Work

To understand the effects of introducing the access transistor (or selector) in the synapse, we performed extensive SPICE simulations using the 1T-1R configuration with different input voltage, conductance and gate-voltage ranges. The selector devices are based on PTM 45nm CMOS technology model. We have considered a memristive device with $R_{ON} = 30k\Omega$ and $R_{OFF} = 300k\Omega$. For a given supply voltage $V_{supply}$, the input to any word-line ($V_{in}$) will be in the range $0 \leq V_{in} \leq V_{supply}$.

A. 1T-1R Power Analysis

Before diving into non-linearity considerations, we characterise the role of transistor gate-voltage $V_g$ in the per synapse power consumption. We performed a Monte Carlo simulation on a $8 \times 8$ 1T-1R crossbar with weights drawn drawn from a normal distribution and mapped to conductance, and inputs drawn from a uniform distribution. Average power per synapse is shown in Fig 2. The results suggest that $V_g$ plays a considerable role in determining power consumption.

B. Analysis of Transistor Induced Non-Linearity

For a crossbar in the 1R configuration, the weights $W$ of the DNN are directly mapped to a memristor conductance state ($G_M = 1/R_M$). On the other hand, in the 1T-1R configuration, $W$ is mapped to the effective conductance $G_{eff} = 1/(R_M + R_t)$, where $R_t$ is the equivalent resistance due to the transistor. The non-linearities in the 1T-1R crossbars arise due to the dependence of $R_t$ on $V_{in}$. Note, $V_{in}$ is proportional to the neuronal activation values of the DNN which varies with the input. Hence, these are referred to as data-dependent non-idealities.
Fig. 3: Characterising $G_{\text{eff}}$ for 1T-1R synapse. Variation in $G_{\text{eff}}$ with $G_M, V_{\text{in}}, V_g$ is shown.

As shown in Fig 3, the effective conductance $G_{\text{eff}}$ is a function of NVM conductance $G_M$, input voltage $V_{\text{in}}$, and gate-voltage $V_g$, i.e.

$$G_{\text{eff}} = f_1(G_M, V_{\text{in}}, V_g) \quad (1)$$

The key takeaway from Fig. 3 is that $V_{\text{in}}$ has significant influence on $G_{\text{eff}}$ for both smaller and larger $G_M$ values. For lower $V_{\text{in}}$, the $G_{\text{eff}}$ non-ideality can be attributed to the leakage current in the transistor. Thus, in low $V_{\text{in}}$ ranges, lower $V_g$ operation of transistor will nullify the leakage current. Hence, even though $G_{\text{eff}} \rightarrow \infty$ when $V_{\text{in}} \rightarrow 0$, the distortion in $G_{\text{eff}}$ is negligible for low $V_g$. On the other hand, leakage current is not negligible for higher $V_g$, hence the distortions in $G_{\text{eff}}$ cannot be neglected. Further, at higher values of $V_{\text{in}}$ and low $V_g$ operation, the transistor begins to shift its region of operation from linear to saturation, as a result of which we find deviations in the value of $G_{\text{eff}}$. At the juncture of the linear and saturation regions of operation, $R_t$ increases and thus, there is a larger voltage drop across it causing a dip in the value of $G_{\text{eff}}$. This can be seen in Fig. 3 for $V_{\text{in}} > 1$ when $V_g = 0.8$. Note, for high $V_g \geq 1$, such saturation effects occur at a much higher $V_{\text{in}} > 2$ thus making it irrelevant.

C. Finding 1T-1R Linear Regime

In the ideal scenario, we would expect $G_{\text{eff}}$ to be a horizontal line parallel to the x-axis for any given value of $G_M$ in case of Fig 3. Since we keep selector gate-voltage constant for an MVM operation, we want:

$$G_{\text{eff}} = f_2(G_M, V_g) \quad (2)$$

To omit data-dependence, our objective here is to find out the range of parameters for which Eqn. 2 is a reasonable approximation for Eqn. 1. That is, there should be a weak or no dependence of $G_{\text{eff}}$ on $V_{\text{in}}$. Once we get rid of this data-dependence, we can infer that controlling $V_g$ will allow us to operate the transistor in a linear regime where, $G_M \approx k \times G_{\text{eff}}$, where $k$ is a scalar.

Fig. 4 (Right) illustrates the 1T-1R non-linearity where we show the $G_{\text{eff}}$ values obtained for a range of $G_M$ for $0 < V_{\text{in}} < 0.5$ across different $V_g$. For a particular $G_M$ (especially larger values) we observe the spread of $G_{\text{eff}}$ becomes more prominent. Higher the spread of the blue region, higher is the data-dependence of $G_{\text{eff}}$ on $V_{\text{in}}$ for the given $G_M$. So, restricting the spread in $G_{\text{eff}}$ will curb non-linearity of the 1T-1R synapse. This will also ensure that the transistor operates in the linear regime with a constant $R_t$ (that is data-independent).

Thus, we define a tolerance metric ($tm$) to quantify the spread or deviation in $G_{\text{eff}}$ as shown in Fig. 4 (Right). Fig. 4 (Left) further illustrates the range of $V_{\text{in}}$ for which linearity can be assumed for a given $G_M$ across different $V_g$ values.

At low $V_g = 0.8V$, unavailability of higher $V_{\text{in}}$ values for higher values of $G_M$ in Fig. 4 (Left) can be attributed to transistor saturation. These results support the observations in prior work GenieX [6]. The authors found higher supply voltage ($V_{\text{supply}}$) of 0.5V (or higher $V_{\text{in}}$) yields higher non-ideality than lower supply voltage $V_{\text{supply}} = 0.25V$. As seen from Fig. 4a, we can explain this as an artefact of the 1T-1R non-linearity. At high $V_g = 1.3V$, unavailability of lower $V_{\text{in}}$ for lower $G_M$ in Fig. 4c (Left) can be attributed to high leakage current. Both of these effects are not noticed in Fig 4b (Left). To make sure that NEAT is capable of handling the worst case, we use $V_{\text{supply}} = 0.5V$ in all our experiments.

The above discussion indicates that there is an upper limit to $V_g$ for achieving desirable linear characteristics for a given $V_{\text{in}}$ range.

D. Defining Conductance cut-off ($G_{\text{eff\_cutoff}}$)

Based on our above discussion, we observe that for a given set of $V_g$, $V_{\text{supply}}$ and tolerance metric, an upper bound cut-off
value \( (G_{\text{eff cutoff}}) \) exists for which the 1T-1R synapse exhibits linear characteristics. We term the corresponding NVM device state as \( G_{M_{\text{cutoff}}} \). \( G_{M_{\text{cutoff}}} \) has been annotated in Fig. [4a] for a tolerance value < 2.5%. For \( V_g = 0.8V \) and 1V, \( G_{M_{\text{cutoff}}} \) values are around \( 1.25 \times 10^{-5} \Omega^{-1} \) and \( 3.34 \times 10^{-5} \Omega^{-1} \) respectively. For \( V_g = 1.3V \), we don’t have any cutoff for the given tolerance metric. This implies that we cannot operate the 1T-1R synapse at \( V_g = 1.3V \). Thus, from this analysis, we obtain the \( G_{\text{eff cutoff}} \) values that can be used to determine the corresponding range of software DNN weights which will ensure linear operation of 1T-1R synapse after mapping. Fig [5] shows the \( G_{M_{\text{cutoff}}} \) vs. \( V_g \) plot for 2.5% tolerance metric and \( V_{\text{supply}} = 0.25V, 0.5V \).

Note, the focus of the above analysis is on the correctness of the Multiply-and-Accumulate (MAC) operation that happens at the synapse level based on \( V_g \), \( V_{\text{supply}} \) and \( G_{\text{eff cutoff}} \) values. While extending this analysis to a crossbar, feasibility of all these parameters should be checked. For e.g. there would be a limit to leakage current permissible for each bitline dictated by the sensing device, which would in-turn set a per synapse limit on leakage current, essentially adding a constraint on \( V_g \). Thus, at an array level, new \( V_g \), \( V_{\text{supply}} \) and \( G_{\text{eff cutoff}} \) constraints need to be calculated. However, the overall methodology of obtaining the cut-off parameters for linear operation will be the same as discussed above.

III. NON-LINEARITY AWARE TRAINING (NEAT)

The non-linearity of \( G_{\text{eff}} \) can induce performance degradation in DNNs when the corresponding trained weights \( W \) are mapped onto crossbars. To mitigate performance losses, we convert \( G_{\text{eff cutoff}} \) (as determined in Section II-D) to obtain the corresponding \( W_{\text{cut}} \) for the software DNN. Then, we restrict all the weights \((W)\) of the DNN in the interval \([-W_{\text{cut}}, W_{\text{cut}}]\) as shown in Eqn. [3]:

\[
W_{\text{map}} = \begin{cases} 
W & |W| \leq W_{\text{cut}} \\
W_{\text{cut}} & W > W_{\text{cut}} \\
-W_{\text{cut}} & W < -W_{\text{cut}}.
\end{cases}
\]

From Eqn. [3] we observe that for the linear regime \((|W| \leq W_{\text{cut}})\) which corresponds to \( G_{\text{eff}} \approx G_{M} \), the software weight parameters can be mapped linearly onto the crossbars. While, for the non-linear regime \((|W| > W_{\text{cut}})\) that corresponds to deviation of \( G_{\text{eff}} \) from \( G_{M} \), \( W \) is clipped at \( W_{\text{cut}} \). The objective of NEAT is to restrict the weight parameters to be within the linear regime for the given gate-voltage \( V_g \) of the transistor. Fig. [6] illustrates the overall flow of the NEAT process.

A. Training DNNs and Obtaining \( W_{\text{cut}} \)

We train the network with cross-entropy loss on the classification dataset. From the trained networks, we can find the maximum and the minimum weight values, namely \( W_{\text{min}} \) and \( W_{\text{max}} \). After that, given all the weight parameters, we calculate the \( W_{\text{cut}} \) value for a given \( V_g \) value by determining \( G_{\text{eff cutoff}} \) using SPICE simulations as described in Section II-D. We set the search range of \( V_g \) as \([0.7, 1.0]\) with interval of 0.05.

B. \( V_g \) Control Schemes: Homogeneous and Heterogeneous

With the above-stated relationship between \( W_{\text{cut}} \) and \( V_g \), we suggest two different strategies for \( V_g \) selection.

**Homogeneous \( V_g \) control**: We use the same \( V_g \) value for \( W_{\text{cut}} \) computation across all layers of the DNN. This method ensures high energy-gains but can incur significant accuracy losses. It is hard to predict how much accuracy degradation will be incurred without accessing the validation or test dataset. In other words, for a given \( W_{\text{cut}} \) (related to a given \( V_g \)), we can identify the percentage of weights that will operate in the non-linear 1T-1R regime after mapping. But we cannot identify the accuracy drop without accessing the test dataset. This might be crucial for the applications where accuracy should be preserved.

**Heterogeneous \( V_g \) control**: To address the above-mentioned problem, we suggest a heterogeneous approach where each layer has a different \( V_g \) allocated. We observe that each layer of the DNN has a different weight distribution, as shown in Fig. [7]. Using this observation, we allocate a low value of \( V_g \) (corresponding to a smaller \( G_{\text{eff cutoff}} \) and hence, \( W_{\text{cut}} \)) for the layers having a smaller range weights (e.g., layer

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**Fig. 5**: The change of \( G_{M_{\text{cutoff}}} \) with respect to \( V_g \).

**Fig. 6**: Overall flow of NEAT.

**Fig. 7**: Illustration of layer-wise weight distribution. We use a VGG11 architecture on CIFAR10.
Improves the performance in lower experiments, we show that the iterative training significantly regime when mapped onto crossbars. By carrying out extensive number of weights in the network can be located in the linear incurred from Step 1. We repeat these two steps so that greater iteratively for a couple of epochs to recover any accuracy loss regime as per Eqn. (3). In Step 2, we retrain the networks \( W \) restricting the weights of the DNN (\( V \)).

5 ~ layer 7), otherwise, we allocate a high value of \( V \) (e.g., layer 1). By doing this, we can obtain energy-efficiency by guaranteeing that most of the weights lie in the linear regime. Note, we set the \( V \) and \( W_{\text{cut}} \) for all layers based on the weight distribution without having access to the test or validation data.

Algorithm 1 shows the strategy of selecting the optimal \( V \) for the heterogeneous approach. The purpose is to set the \( V \) configuration to extract significant energy-efficiency. Any accuracy loss incurred in the DNN with setting the \( V \) and corresponding \( W_{\text{cut}} \) is recovered by iterative training. To this end, we first define the maximum absolute value of weights in layer \( l \) (lines 1-3). Then, we search the optimal \( V \) value in ascending order. Based on the given \( V \), we calculate \( W_{\text{cut}} \). If the current \( W_{\text{cut}} \) covers all the weights values, we set the last \( V_{\text{prev}} \) as the optimal \( V \) at layer \( l \) and stop searching (lines 4-12). It is worth mentioning that setting \( V_{\text{prev}} \) or \( W_{\text{cut}} \) distorts the weight distributions that causes accuracy decline. This loss can be minimized by iterative training described in the next subsection. We further note that heterogenous \( V \) selection does not require any data.

**C. Iterative Training**

In NEAT, after setting the optimal \( V \) and \( W_{\text{cutoff}} \) values from homogeneous or heterogeneous gate control, we then transform the weights of the DNN. If we use lower values of \( V \) which do not cover all weight ranges, the weight distribution gets altered, resulting in accuracy degradation. To address this issue, we propose iterative training which consists of two steps, as shown in Algorithm 2. Step 1 is essentially restricting the weights of the DNN (\( W \)) in the suitable cut-off regime as per Eqn. (3). In Step 2, we retrain the networks iteratively for a couple of epochs to recover any accuracy loss incurred from Step 1. We repeat these two steps so that greater number of weights in the network can be located in the linear regime when mapped onto crossbars. By carrying out extensive experiments, we show that the iterative training significantly improves the performance in lower \( V \) scenarios.

**IV. EXPERIMENTAL RESULTS**

We conduct our experiments on PyTorch with VGG11 [11] and ResNet18 [12] architectures on CIFAR10 and CIFAR100 datasets [13]. For retraining process (Step 2 in Algorithm 2), we use Adam optimizer with learning rate \( 10^{-5} \). For all experiments, the number of iteration (\( N \) in Algorithm 2) is 30 which implies low overhead for retraining.

**A. Analysis on Homogeneous \( V \) Selection**

In Fig. 8 we change \( V \) from 0.75 to 1.0 and report the classification accuracy. The results show that low \( V \) induces low \( W_{\text{cut}} \) and in turn decreases performance when DNN weights are restricted to \( W_{\text{cut}} \) regime. However, using iterative training recovers the performance degradation. Especially, for a ResNet18 architecture, using iterative training shows improvement over 50% in terms of accuracy at \( V = 0.75 \). Moreover, with iterative training, VGG11 and ResNet18 networks almost maintain their classification accuracy in the range of \( V = [0.85, 1.0] \) and \( V = [0.8, 1.0] \), respectively. To further validate the effectiveness of iterative training, we provide the accuracy with respect to the number of iterations. Fig. 9 shows that the classification accuracy improves as the number of iterations (\( N \) in Algorithm 2) increases. This is because iterative training forces the weights to be in the linear regime of operation. To validate this, we plot the percentage of weights in the linear regime at the first convolution layer (\( V = 0.8 \) case). The results demonstrate that the majority of weights (\( \sim 96\% \)) are located in the linear regime after 30 iterations in case of iterative training. Other layers also show similar results.
Fig. 9: Classification accuracy with respect to the number of iterative training. We use VGG11 on CIFAR100.

TABLE I: Classification accuracy of heterogeneous setting.

| Model | Dataset | Iterative Training | Optimal $V_g$ | Optimal $V_g - 0.05$ |
|-------|---------|--------------------|---------------|----------------------|
| VGG11 | CIFAR10 | No                 | 88.05         | 78.55                |
| VGG11 | CIFAR10 | Yes                | 88.74         | 83.51                |
| Res18 | CIFAR10 | No                 | 90.60         | 55.67                |
| Res18 | CIFAR10 | Yes                | 90.58         | 59.23                |
| VGG11 | CIFAR100| No                 | 68.42         | 63.64                |
| VGG11 | CIFAR100| Yes                | 68.88         | 66.06                |
| Res18 | CIFAR100| No                 | 72.99         | 27.62                |
| Res18 | CIFAR100| Yes                | 73.60         | 29.22                |

B. Analysis on Heterogeneous $V_g$ Selection

Based on Algorithm 1, we obtain the heterogeneous layerwise $V_g$ configuration, and define this as “Optimal $V_g$”. In order to study the energy-accuracy trade-off, we conduct experiments on the more energy-efficient configuration, named “Optimal $V_g - 0.05$”. Here, we take the individual layerwise $V_g$ values obtained from Algorithm 1 and further subtract 0.05V as shown in Fig. 10. In Fig. 10, we observe that high $V_g$ values are required for the input layer, whereas low $V_g$ values are required for the intermediate layers. Table I presents the classification accuracy in case of the heterogeneous approach. Just plainly restricting the DNN weights in the cut-off range based on “Optimal $V_g$” configuration yields < 0.3% accuracy drop, even without any iterative training across all models and datasets. For “Optimal $V_g - 0.05$” (Fig. 10), drastic performance degradation is observed since most of the $V_g$ values are set to the minimum value 0.7 which lowers the $W_{cut}$. Iterative training in this case increases the accuracy by 2−5%. It is worth mentioning that we can find a more fine-grained solution by setting the search interval (in this case, 0.05) to a smaller value.

C. Analysis on Energy Efficiency

Finally, we present the energy efficiency of various configurations in Fig. 11. We measure the energy consumption in 1T-1R crossbars following previous work [14]. We use the energy computed for homogeneous gate-control scenario for $V_g = 1.0$ as baseline against which energy gain (%) are shown. For the homogeneous setting, we can achieve high energy gain by simply reducing $V_g$. Especially, we can achieve ~ 23% energy gain at $V_g = 0.8$ on ResNet18 architecture with CIFAR10 while suffering minimal accuracy loss (~1.5%). However, selecting a very low value for $V_g$ such as $V_g = 0.75$ induces huge performance degradation (Fig. 8). For the heterogeneous setting, we obtain over 10% energy gain for all experiments.

V. CONCLUSION

We propose a novel training method that takes into account the non-linear characteristics of the transistor (selector) in 1T-1R crossbars. We analyse this non-linearity in low transistor gate-voltage scenario using both algorithm and hardware perspectives. Moreover, we mitigate the effect of non-linearity by iterative training. Our experimental results demonstrate that our proposed NEAT technique achieves energy-efficiency while preserving the classification accuracy of the DNNs. Our work can impact the future deployment of 1T-1R crossbar in extremely resource-constrained environment.

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