Book Chapter

DC Performance Variations of SOI FinFETs with Different Silicide Thickness

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Abstract

DC performance and the variability of n-type silicon-on-insulator dopant-segregated FinFETs with different silicide thickness ($T_{\text{sili}}$) are analyzed. DC parameters including threshold voltage, low-field-mobility-related coefficient, and parasitic resistance are extracted from $Y$-function method for the comparison of DC performance and variability, and the correlation analysis. All the devices show similar subthreshold characteristics, but the devices with thicker $T_{\text{sili}}$ have greater threshold voltages. The devices with thicker $T_{\text{sili}}$ suffer from the DC performance degradation and its greater variations because the Schottky barrier height at the NiSi/Si interface increases and fluctuates greatly. This effect is validated by greater threshold voltages, larger parasitic resistances, and high correlations among all the DC parameters for the thicker $T_{\text{sili}}$. The devices with thicker $T_{\text{sili}}$ also has higher low-frequency noise because of larger parasitic resistances and their correlated mobility degradations. Therefore, the device with relatively-thin $T_{\text{sili}}$ is expected to have better DC performance and variability concerns.

Introduction

Silicon-on-insulator (SOI) MOSFETs maintain short channel immunity successfully due to the absence of substrate leakage current [1]. SOI-based devices having fin-shaped [2], ultra-thin-body [3], or gate-all-around [4] channel regions attain great scalability without short channel degradation. Meanwhile, dopant-segregated SOI MOSFETs have been considered as one of the promising candidates due to their several advantages over
the planar bulk MOSFETs: low Schottky barrier height (SBH) at the silicide/semiconductor interface, possibility of low-temperature process, and near-abrupt junction formation [5-9]. Not only does MOSFETs, but also tunneling FETs also utilize abrupt doping profile to enhance the band-to-band tunneling transport at the source/channel junction [10,11].

Two-step anneal process during silicidation was suggested to decrease the lateral excursion of silicide into the channel region [12]. The influence of NiPt thickness prior to silicidation on the DC performance of SOI MOSFETs has been studied [13]. Increasing the NiPt thickness increased the contact resistance due to the decreased interfacial area between silicide and semiconductor, but decreased the variations of sheet resistance due to its full silicidation. In this regard, it is necessary to analyze both DC performance and its variability in the perspective of the silicidation for the nanoscale dopant-segregated SOI MOSFETs.

Thus, DC performance and variations of SOI FinFETs with different silicide thickness ($T_{sili}$) were investigated. Then, the variability sources inducing the drain current ($I_{ds}$) variations were studied using the correlation analysis. Low-frequency noise was also measured for the detailed analysis of the devices with different $T_{sili}$.

**Materials and Methods**

(100) undoped SOI with 140-nm-thick buried oxide (BOX) and 20-nm-thick top Si region was prepared. BOX over-etching process was performed to define omega-shaped fin structure as shown in Figure 1b of [13]. After the formation of gate stack ($\text{HfO}_2$, TiN, amorphous-Si), Arsenic dopants were implanted at extension regions to reduce the underlap resistance. After defining nitride spacer regions with the spacer length ($L_{sp}$) of 20 nm, low-energy implantation and annealing at 1070 °C and 1.5 s was done for the source/drain (S/D) regions. Different from [13] where the NiPt with different thickness of 5 or 10 nm was deposited, the same 10-nm-thick NiPt (4 % Pt) was deposited and annealed under two-step rapid thermal process (RTP).
conditions to remove the unreacted NiPt in the middle. Instead, different RTP temperature and time conditions were used to form the NiSi with different $T_{\text{sili}}$ of 8 and 10 nm. Otherwise, all the measured devices have the equivalent number of fins ($N_{\text{fin}}$) of 2, fin width ($W_{\text{fin}}$) of 40 nm, fin height ($H_{\text{fin}}$) of 20 nm, extension length ($L_{\text{ext}}$) of 80 nm, and gate length ($L_{g}$) of 40 nm. The detailed process flow and device geometry are shown in [13].

Figure 1: 3D schematic diagram of the SOI FinFETs.

Geometrical parameters such as gate length ($L_{g}$), spacer length ($L_{sp}$), extension length ($L_{ext}$), silicide thickness ($T_{\text{sili}}$) are also specified. Top left figure describes the real device structure, and red-colored phrases indicate the possible variability sources.

All the devices have the active regions with equivalent size and structure, so the differences of DC performances and the variations are induced mostly by different $T_{\text{sili}}$. Figure 1 shows the possible variability sources of the S/D regions. Uneven NiSi/Si interface [14] and random dopant fluctuation (RDF) [15,16] can also fluctuate the contact resistivity and thus induce the DC performance variations. Different NiSi/Si contact area by different $T_{\text{sili}}$ would also affect the DC performance and variations because typical transfer lengths, defined as the
distances that carriers below the contact travel before entering into the contact, of SOI devices are in the order of 100 nm [17,18], which is longer than the $L_{ext}$. Different RTP conditions involved with different $T_{sili}$ can vary the device performance by statistical piping effect [19] or lateral encroachment of NiSi into the S/D extension regions [20]. To understand DC performance and its variations for different $T_{sili}$, their transfer characteristics were measured using Keithley 4200 semiconductor characterization system, whereas low-frequency noise was measured using HP 89410A vector signal analyzer.
Results and Discussion
DC Performance and Variations at Different Silicide Thickness

Figure 2: DC performance and variations of the SOI FinFETs with the $T_{sil}$ of (a) 8 and (b) 10 nm at drain voltage ($V_{ds}$) of 0.05 V and (c) 1.0 V. The number of measured devices is 50 for each $T_{sil}$. 

Ambipolar effect is negligible
$I_{ds}$ and transconductances ($g_m$) of the 50 measured devices each with different $T_{sili}$ of 8 and 10 nm are shown in Figure 2. Each wafer has a different $T_{sili}$, and the measured devices with each $T_{sili}$ are at the same position of each wafer to minimize the die-to-die variations between two different $T_{sili}$. Gate voltage ($V_{gs}$) is swept from 0.0 to 1.3 V in steps of 0.02 V, and drain voltages ($V_{ds}$) are 0.05 and 1.0 V. Red lines indicate the averages of $I_{ds}$ and $g_m$ for each $T_{sili}$. In both linear and saturation regimes, the devices with the $T_{sili}$ of 8 nm have greater DC performance by showing higher on-state currents ($I_{on}$), while the subthreshold characteristics for the $T_{sili}$ of 8 and 10 nm are similar. Figure 2c shows that all the devices with the $T_{sili}$ of 8 and 10 nm do not have ambipolar effects at high $V_{ds}$ of 1.0 V near the off-state, validating the absence of Schottky contact [13].

$R_{on}$ ($= V_{ds}/I_{on}$) values of the 20 measured devices each with different $W_{fin}$ and $T_{sili}$ are shown in Figure S1. The $I_{on}$ are extracted at the gate overdrive voltage ($V_{gs} - V_{th, CCM}$) of 1.0 V, where $V_{th, CCM}$ is the threshold voltage ($V_{th}$) extracted from constant current method (CCM) at $I_{th} = W_{eff}/L_{g} \cdot 10^{-7}$ A ($W_{eff} = N_{fin}(2H_{fin}+W_{fin})$). The devices with the $T_{sili}$ of 8 nm have smaller $R_{on}$ for all the $W_{fin}$. But the difference of $R_{on}$ between two different $T_{sili}$ is smaller for greater $W_{fin}$ because the ratio of the NiSi/Si contact area between two different $T_{sili}$ decreases. Additionally, raised S/D structure would be beneficial to improve the DC performance by increasing the NiSi/Si contact area. But for raised S/D structure, likewise, thicker $T_{sili}$ also decreases the contact area, increases the contact resistance, and thus degrades the DC performance [21].
Almost all the $Y$-functions satisfy the linearity condition in the strong inversion regime.

Several parameters from the transfer characteristics are extracted to analyze the DC performance variations: $V_{th}$, low-field-mobility-related coefficient ($X_0$), and parasitic resistance ($R_{sd}$). $V_{th}$ values are extracted using CCM or $Y$-function method \cite{16, 22}. $V_{th_{-CCM}}$ is measured at $I_{th} = W_{eff}/L_g \cdot 10^{-8}$ A, whereas $V_{th}$ from $Y$-function method ($V_{th_{-y}}$) is extracted from the x-axis intercept of the linearly-extrapolated curve as shown in Figure 3.

The simple and general expression of the $I_{ds}$ at low $V_{ds}$ in the strong inversion regime is given by

$$I_{ds} = X_0 \cdot (V_{gs} - V_{th_{-y}}) \cdot (V_{ds} - I_{ds}R_{sd})$$  \hspace{1cm} (1)$$

where $X_0$ is defined as $\mu_{eff}C_{ox}W_{eff}/L_g$ ($\mu_{eff}$ is effective mobility and $C_{ox}$ is oxide capacitance). $Y$-function is simply expressed as

$$Y \equiv \frac{I_{ds}}{\sqrt{g_m}} = \sqrt{X_0 \cdot (V_{ds} - I_{ds}R_{sd}) \cdot (V_{gs} - V_{th_{-y}})}$$  \hspace{1cm} (2)$$

According to the equation 2, $Y$-function is linear in the strong inversion regime if $X_0$ or $\mu_{eff}$ does not depend on $V_{gs}$. In other words, the $Y$-function does not satisfy the linearity condition if
the devices suffer from surface roughness scattering greatly [22]. Other assumption is that $I_{ds} \cdot R_{sd}$ is almost invariant to $V_{gs}$ and smaller than $V_{ds}$ in the strong inversion regime, which is satisfied in this study. Almost all the measured devices also meet the linearity condition at the $V_{ds}$ of 0.05 V (Figure 3) because all the devices have omega-shaped structure with ultra-thin fin channel, which induces volume inversion and thus attenuates the surface roughness scattering.

**Figure 4**: Average and standard deviations of dc parameters for the SOI FinFETs with the $T_{silicid}$ of 8 nm (black) and 10 nm (red) at different $V_{ds}$: $V_{th_y}$, $X_0$, and $R_{sd}$.

Figure 4 shows the $V_{th_y}$, $X_0$, and $R_{sd}$ of the measured devices at the $V_{ds}$ of 0.01, 0.02, 0.03, 0.04, and 0.05 V extracted from $Y$-function method. Average $X_0$ and $R_{sd}$ are independent of $V_{ds}$, whereas $V_{th_y}$ increases slightly as $V_{ds}$ increases. $V_{th_y}$ includes the band-bending by gate voltage as well as the body-effect expressed by $m/2 \cdot V_{ds}$, where $m$ is the body-effect coefficient ($m$ is simply approximated as 1 for fully-depleted devices), thus showing a slight increase of $V_{th_y}$ with the slope of $V_{ds}/2$ as $V_{ds}$ increases [23]. The devices with the $T_{silicid}$ of 8 nm show greater $X_0$ and smaller $R_{sd}$ due to greater NiSi/Si contact area.
The devices with the $T_{sil}$ of 10 nm have greater variations of $V_{th,y}$, $X_0$, and $R_{sd}$ (Figure 4). Standard deviations ($\sigma$) of $X_0$ and $R_{sd}$ for the $T_{sil}$ of 10 nm increase by 62.4 and 48.5 %, respectively, with respect to those for the $T_{sil}$ of 8 nm. Not only $V_{th,y}$ but also $V_{th\_CCM}$ variations are severer for the $T_{sil}$ of 10 nm ($\sigma = 45 \text{ mV}$) than for the $T_{sil}$ of 8 nm ($\sigma = 22 \text{ mV}$) at all different $V_{ds}$.

**DC Performance Variability Analysis**

*Figure 5*: Scatter plots of the $I_{on\_y}$ at $(V_{gs} - V_{th\_y})$ of 0.8 V with respect to the DC parameters ($I_{off}$, $V_{th\_y}$, $X_0$, and $R_{sd}$) for the SOI FinFETs at the $V_{ds}$ of 0.05 V. All the linear regressions indicate the sensitivity of the $I_{on\_y}$ with respect to the DC parameters.

To investigate why the devices with the $T_{sil}$ of 10 nm suffer from smaller DC performance and greater variations, correlation analysis of $I_{on}$ with off-state currents ($I_{off}$), $V_{th\_y}$, $X_0$, and $R_{sd}$ is done in Figure 5. Spearman’s correlation is used to calculate the correlation coefficient ($\rho$) [15]. $I_{off}$ values are the $I_{ds}$ at the $V_{gs}$ of 0.0 V, whereas all the $I_{on}$ values are extracted at the gate overdrive voltage ($V_{gs} - V_{th\_y}$) of 0.8 V ($I_{on\_y}$) to neglect the $V_{th\_y}$ effect [24]. Since all the devices have similar $SS$ and no gate-induced drain leakages, $I_{off}$ is mostly determined by $V_{th\_y}$ ($\rho = -0.781$ and -0.907 for the $T_{sil}$ of 8 and 10 nm, respectively). Due to these perspectives, therefore, a slight correlation between $I_{on\_y}$ and $I_{off}$ along with $V_{th\_y}$ is expected.

Nonetheless, there are correlations between $I_{off}$, $V_{th\_y}$, and $I_{on\_y}$ for the $T_{sil}$ of 10 nm (left of Figure 5). In addition, $V_{th\_y}$ for the $T_{sil}$ of 10 nm is correlated with $X_0$ ($\rho = -0.530$) and $R_{sd}$ ($\rho = 0.491$), whereas $V_{th\_y}$ for the $T_{sil}$ of 8 nm is independent of $X_0$ ($\rho = -0.077$) and $R_{sd}$ ($\rho = 0.200$) at all different $V_{ds}$. $X_0$ is also correlated with $R_{sd}$ for the $T_{sil}$ of 10
nm ($\rho = -0.581$), whereas the correlation is small for the $T_{sili}$ of 8 nm ($\rho = -0.162$).

These high correlations among all the DC parameters ($I_{off}$, $V_{th}$, $X_0$, $R_{sd}$) and $I_{on}$ for the $T_{sili}$ of 10 nm are related to the high SBH at the NiSi/Si interface. Higher SBH for thicker $T_{sili}$ is expected due to greater lateral encroachment of NiSi into the S/D extension regions [19,25]. Greater $V_{th,CCM}$ (or $V_{th}$) and larger $R_{sd}$ for the $T_{sili}$ of 10 nm are the indicative of higher SBH according to the equation 2 in [26] and higher contact resistivity [27], respectively. Higher SBH for thicker $T_{sili}$ requires much band-bending for the carrier injection from source (related with $I_{off}$ and $V_{th}$) as well as impedes carrier flow under operation (related with $X_0$, $R_{sd}$, and thus $I_{on}$) [28]. For the low-SBH devices, the SBH variations induce the on-state performance variations, not the $V_{th}$ variations [26]. Therefore, the $V_{th}$ variations for the $T_{sili}$ of 8 nm are dominantly induced by other variability sources (gate work function (WF) variation [24], RDF [15], interface traps [29]) except the SBH. And that is why the $V_{th}$ for the $T_{sili}$ of 8 nm is not correlated with $X_0$, $R_{sd}$, and $I_{on}$.

Greater variations of all the DC parameters for the $T_{sili}$ of 10 nm can also explain the increased SBH and its variations. The $R_{sd}$ variations for SOI FinFETs are dominantly affected by NiSi/Si contact resistance [20,27]. The NiSi/Si interface consists of NiSi crystal grains having different WF and surface roughness [14]. The extension regions suffer from RDF [15] along with the WF variations, having different SBH at each of NiSi crystal grains and also for each of the devices. And this induces the SBH variations greatly for the $T_{sili}$ of 10 nm due to smaller contact area.
Figure 6: $I_{on,y}$ variations and variations of the dc parameters ($V_{th,y}$, $X_0$, and $R_{sd}$) contributing to the $I_{on,y}$ variations for the $T_{sili}$ of 8 and 10 nm.

Figure 6 shows the relative contributions to the $I_{on,y}$ variations with respect to the DC parameters each. When the DC parameters are correlated each other, the contributions to the variations of $I_{on,y}$ for the correlated portion are calculated using the correlation coefficient, sensitivity (the slope of scatter plots in Figure 5), and standard deviations [24]. All the correlated portions are presented as the shaded area. All the three DC parameters are correlated each other and the $X_0$ variations affect the $I_{on,y}$ variations greatly for the $T_{sili}$ of 10 nm, whereas they are independent and the $R_{sd}$ variations affect the $I_{on,y}$ variations greatly for the $T_{sili}$ of 8 nm.
Low-frequency Noise Analysis

Figure 7: Drain current noise spectral density ($S_{Ids}$) measured at the $V_{ds}$ of 0.05 V and the overdrive voltage ($V_{ov} = V_{gs} - V_{th,CCM}$) of 0.3 V for the $T_{sili}$ of (a) 8 and (b) 10 nm. The number of measured devices, close to the average $I_{ds}$, is 10 each.

Low-frequency noise was measured at the $V_{ds}$ of 0.05 V and at the overdrive voltage ($V_{ov} = V_{gs} - V_{th,CCM}$) of 0.3 V (Figure 7). Frequency range was from 1 to 1000 Hz, and the 10 devices each with the $T_{sili}$ of 8 and 10 nm, closest to the average $I_{ds}$, were
measured. All the results follow the 1/f trend except at the frequency near 1 Hz where Lorentzian-type noise plateau is observed due to the small-area devices. The devices with the $T_{\text{sil}i}$ of 10 nm have greater average $S_{Ids}$ for all the frequency range.

Figure 8: Normalized $S_{Ids}$ at 10 Hz with respect to the $I_{ds}$ at different $V_{ov}$. Figure 8 shows the $S_{Ids}$ normalized by $I_{ds}^2$ of the devices with different $T_{\text{sil}i}$ at the $V_{ov}$ from 0.1 to 0.6 V in steps of 0.1 V measured at 10 Hz. In case of the $V_{ov}$ from 0.3 to 0.6 V, the normalized $S_{Ids}$ values are almost independent of $V_{ov}$, where the noise induced by $R_{sd}$ ($S_{Rsd}$) is dominant to the device [30]. The noise within the channel ($S_{Rch}$) is from the Si/SiO$_2$ interface and the channel itself, whereas $S_{Rsd}$ is from the S/D contact at NiSi/Si interface. But the quality of Si/SiO$_2$ interface is almost similar for all the devices because the only difference is RTP, performed under low temperature around 300~450 °C [13,19,20,31,32] enough not to induce the Si/SiO$_2$ interface damage. In spite of that, the devices with the $T_{\text{sil}i}$ of 10 nm have greater $S_{Rch}$ because high SBH close to the lightly-doped extension region decreases the $X_0$ (related to $\mu_{eff}$) which is correlated with the $R_{sd}$. Greater $S_{Rch}$ for the $T_{\text{sil}i}$ of 10 nm is also explained by the lateral encroachment of NiSi into the S/D extension regions. More lateral encroachment of NiSi for thicker $T_{\text{sil}i}$ induces higher SBH, which impedes the carrier flow and decreases the channel length.
These physical phenomena increase the $S_{Rch}$ according to the equation 3 of [30], thus the greater $S_{Rch}$ for the $T_{sili}$ of 10 nm is obtained (Figure 8). As a result, the devices with the $T_{sili}$ of 10 nm have greater normalized $S_{Ids}$ for all the $V_{ov}$.

**Conclusions**

DC performance and variability of the dopant-segregated SOI FinFETs with different $T_{sili}$ are analyzed in terms of the DC parameters extracted from $Y$-function method and Spearman correlation, respectively. Thicker $T_{sili}$ degrades DC performance by decreasing $I_{on}$ and $g_{m,max}$, and fluctuates $V_{th}$, $X_0$, $R_{sd}$, and $I_{on}$ greatly because the SBH increases greatly and varies along with WF variation and RDF at the S/D region. In addition, the devices with the $T_{sili}$ of 10 nm suffer from large low-frequency noise due to high SBH, which is caused by greater lateral encroachment of NiSi into the S/D extension regions and related to greater variations and correlations of $V_{th,y}$, $X_0$, $R_{sd}$, and $I_{on,y}$. Therefore, the device with relatively-thin $T_{sili}$ is promising to improve DC performance and minimize the variation.

This variability study would be helpful to design nanoscale devices having a few dopants and small contact area because the SBH values and variations of the devices depend on the $T_{sili}$ greatly.

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Figure S1: On-state resistance ($R_{on}$) as a function of fin width ($W_{fin}$) for different $T_{sili}$ of 8 and 10 nm. The number of fins ($N_{fin}$) for each device is 20. As $W_{fin}$ increases from 40 to 80 nm, the difference of $R_{on}$ between two different $T_{sili}$ decreases from 36 to 23 %.

$N_{fin} = 20$