Fault-tolerant fidelity based on few-qubit codes: Parity-check circuits for biased error channels

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In the shallow sub-threshold regime, fault-tolerant quantum computation requires a tremendous amount of qubits. In this paper, we study the error correction in the deep sub-threshold regime. We estimate the physical error rate for achieving the logical error rates of $10^{-6} - 10^{-15}$ using few-qubit codes, i.e. short repetition codes, small surface codes and the Steane code. Error correction circuits that are efficient for biased error channels are identified. Using the Steane code, when error channels are biased with a ratio of $10^{-3}$, the logical error rate of $10^{-15}$ can be achieved with the physical error rate of $10^{-5}$, which is much higher than the physical error rate of $10^{-9}$ for depolarising errors.

I. INTRODUCTION

Quantum computation has the capability to solve problems that are intractable in the conventional paradigm. The unique properties of quantum computation allow us to find quantum algorithms that are superior to classical ones, such as factorisation, search and quantum simulation algorithms [1]. Many quantum computation applications rely on the accurate manipulation of highly-entangled multi-qubit quantum states. For instance, solving the factorisation problem on the code-breaking scale requires an error rate of $\lesssim 10^{-12}$ per logical quantum gate [2, 3]. Quantum error correction is a promising approach to the high-fidelity quantum computation. Taking the surface code as an example, by encoding the logical information in a two-dimensional array of qubits, the probability of a logical fault decreases exponentially with the array size when the physical error rate is lower than the threshold of $\sim 1\%$ [4, 5]. Qubit initialisation, measurement, single-qubit and two-qubit quantum gates with sub-threshold error rates have been demonstrated with superconducting qubits and trapped ions [6–8]. Given a quantum processor with sufficient qubits operated in the sub-threshold regime, we can implement any quantum algorithm with an adequately high fidelity.

Quantum error correction is costly in the shallow sub-threshold regime. When the physical error rate is not adequately lower than the threshold, we need thousands of physical qubits for encoding one surface-code logical qubit, in order to achieve the logical error rate of $10^{-12} - 10^{-15}$ [9]. In recent years, rapid progress has been made in experiments. The qubit number and gate fidelity have been greatly improved [10], which promote the research of practical applications on intermediate-scale quantum computers in near term. Networked architectures can help to scale up the fault-tolerant quantum computer by connecting small processors using entanglement generation and distillation in addition to various codes and error models [11–13]. Besides the increment in the qubit number, the gate fidelity in various quantum computation platforms has been constantly improved in the past twenty years [14]. By exploring the physics of non-Abelian anyons in materials, theoretical studies suggest that the error rate in topological quantum computation could be much lower than in conventional approaches [15]. The development of technologies that provide lower physical error rates will reduce the encoding cost in the fault-tolerant quantum computation. In this paper, we study the quantum error correction in the deep sub-threshold regime, i.e. in which the error rate is much lower than the threshold such that the fault-tolerant-level logical error rate can be achieved with encoding in only a few qubits.

In this paper, we estimate the physical error rate required for achieving the fault-tolerant-level logical error rate using few-qubit codes. We consider the surface codes with small code distances and the Steane code for depolarising errors, and the Steane code and short repetition codes for biased Pauli-error channels. Usually, the error correction is more efficient for biased errors compared

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig1.png}
\caption{The logical error rate for varies codes and error models. In the parity check repetition, the encoding is not used, and errors are detected by repeating the two-qubit parity check measurements. The code distance of the repetition code is smaller than 22. For the error model, depol, 1-c and 3-c represent the depolarising error model, the 1-channel dominant model and 3-channel dominant model, respectively. $\eta = \epsilon/p$, is the bias ratio between the error rate of dominant errors $p$ and the error rate of other errors $\epsilon$.}
\end{figure}
with depolarising errors [16–20]. For biased channels, we focus on two cases: one or three of 15 Pauli-error channels are dominant. For the 1-channel case, we find an error-correction circuit for each of the 15 Pauli-error channels, such that the dominant errors result in only one species of errors, e.g. measurement errors. The correction of one species of errors is more efficient than general errors. Efficient circuits for the 3-error case are also identified. Using these circuits in the repetition code, the fault-tolerant-level logical error rate can be achieved with a relatively high physical error rate, but error channels need to be extremely biased. The Steane code can correct general errors. We find that error correction circuits of the Steane code are also efficient for correcting specific one-channel errors. The numerical results show that the physical error rate required by the Steane code is hundreds of times higher when the bias is of a ratio $10^{-2}$ than the rate when errors are depolarising. All results are summarised and shown in Fig. 1.

This paper is organised as follows. In Sec. II, the Pauli error model is introduced. In Sec. III, we discuss circuits that are efficient for different biased error models. In Sec. IV, the definition of logical error rate used in this paper is given. The error correction for the depolarising error model using small surface codes and the Steane code is discussed in Sec. V. The error correction for 1-channel dominant models and 3-channel dominant models are discussed in Secs. VI and VII. A summary of results is given in Sec. VIII.

II. ERROR MODEL

In this paper, we focus on the deep sub-threshold regime, in which physical error rates are much lower than the threshold. In all the computation operations, we are interested in the case that the error rate of two-qubit gates is much higher than single-qubit operations, i.e. state preparation, preparation and single-qubit gates. If errors caused by single-qubit gates are negligible, we can use the Pauli twirling [21–24] to convert errors in two-qubit Clifford gates, e.g. controlled-NOT and controlled-phase gates, into Pauli errors. Therefore, we model errors as follows: Single-qubit operations are error-free; we only use the controlled-NOT gate in the quantum error correction, and the controlled-NOT gate with error is modeled as an error-free gate followed by the erroneous operation

$$N = \sum_{\sigma_c,\sigma_t} P_{\sigma_c,\sigma_t} [\sigma_c \otimes \sigma_t],$$  \hfill (1)

where $\sigma = I, X, Y, Z$ are Pauli operators, c and t respectively denote the control and target qubits, $P_{\sigma_c,\sigma_t}$ is the rate of the Pauli channel $[\sigma_c \otimes \sigma_t]$, and $\sum_{\sigma_c,\sigma_t} P_{\sigma_c,\sigma_t} = 1$. Here, $[U]\left(\bullet\right) = U \bullet U^\dagger$. Except the channel $[I_c \otimes I_t]$, the other 15 channels cause Pauli errors. $P_{I_c, I_t}$ is the gate fidelity, and $1 - P_{I_c, I_t}$ is the total error rate. For the depolarising error, 15 Pauli errors are uniformly distributed, i.e. rates of all Pauli errors are the same, and $P_{\sigma_c,\sigma_t} = (1 - P_{I_c, I_t})/15$, where $\sigma_c \otimes \sigma_t \neq I_c \otimes I_t$. For the extremely biased error, we consider two cases. In the 1-channel case, only one of 15 Pauli error channels is dominant. In the 3-channel case, three of 15 Pauli error channels are dominant.

III. PARITY-CHECK CIRCUITS

In this section, we propose parity-check circuits tackling biased error channels, i.e. the 1-channel and 3-channel cases. We consider the measurement of two operators $Z \otimes Z$ and $Z \otimes Z \otimes Z \otimes Z$. The measurement of other two-qubit and four-qubit Pauli operators can be obtained by modifying circuits for measuring $Z \otimes Z$ and $Z \otimes Z \otimes Z \otimes Z$, by inserting single-qubit Clifford gates before and after the measurement to adapt the Pauli basis. With an ancillary qubit, we can implement a controlled-NOT gate using two projective measurements of $Z \otimes Z$ and single-qubit operators [see Fig. 2(a)]. Therefore, replacing the controlled-NOT gate with the $Z \otimes Z$ measurement, the $Z \otimes Z$ measurement and single-qubit operations form a universal gate set for the quantum computation.
The circuit for $X_t$ is constructed following the approach in Fig. 2(b). As we have discussed, $X_t$ errors can be efficiently corrected by repeating the parity check. The circuit for $Z_c$ is similar. By applying Hadamard gates before and after the controlled-NOT gate, we can realise a controlled-NOT gate with the control qubit and target qubit exchanged (See circuit-B in Fig. 4). With the Hadamard gates, $Z_c$ errors are converted into $X_t$ errors.

**A. Two-qubit parity-check circuits**

We first consider the 1-channel case, i.e. only one of 15 Pauli error channels in the controlled-NOT gate is dominant. We construct two-qubit parity-check circuits that are efficient in the error correction for each Pauli error channel as follows. The 15 channels can be divided into four groups.

The first group includes three channels: $X_t$, $Z_c$ and $Z_c \otimes X_t$. The corresponding circuits are shown in Fig. 3. The circuit for $X_t$ is constructed following the approach in Fig. 2(b). As we have discussed, $X_t$ errors do not change the state of data qubits. Therefore, under the condition that the probability of such a measurement error is lower than $1/2$, we can correct the error by repeating the measurement and determine the eventual outcome by the majority vote. Suppose that the outcome is $+1$ in $N_+$ measurements and $-1$ in $N_-$ measurements, the eventual outcome is $+1$ if $N_+ > N_-$ and $-1$ if $N_- > N_+$.

### 1-channel efficient circuits

Two errors connected by the wavy line always occur simultaneously. Circuits for $X_t$, $Y_t$, and $Z_t$ ($X_t \otimes X_t$, $Z_t \otimes Y_t$ and $Y_t \otimes X_t$) can be obtained by replacing the original controlled NOT gate in the circuit for $Z_t$ ($Z_c \otimes Z_t$) with modified controlled-NOT gates A, D, and E in Fig. 4, respectively.

![FIG. 3.](image-url) The 1-channel efficient circuits for $X_t$, $Z_c$ and $Z_c \otimes X_t$. The dashed red square denotes the error that may happen. Two errors connected by the wavy line always occur simultaneously.

![FIG. 4.](image-url) Modified controlled-NOT gates. All these six circuits are equivalent to the original controlled-NOT gate if circuits are error-free. Here, $R_z = \exp^{i \frac{\pi}{2} Z}$ and $R_x = \exp^{i \frac{\pi}{4} X}$.

| Label | Circuit | Label | Circuit |
|-------|---------|-------|---------|
| A     | ![Circuit A](image-url) | B     | ![Circuit B](image-url) |
| C     | ![Circuit C](image-url) | D     | ![Circuit D](image-url) |
| E     | ![Circuit E](image-url) | F     | ![Circuit F](image-url) |

### FIG. 5.

The 1-channel efficient circuits for $Z_t$ and $Z_c \otimes Z_t$. The dashed red square denotes the error that may happen. Two errors connected by the wavy line always occur simultaneously.
FIG. 7. The 3-channel efficient circuit for \( \{X_c, X_t, X_c \otimes X_t\} \). The dashed red square denotes the error that may happen. Two errors connected by the wavy line always occur simultaneously. Circuits for \( \{Z_c, Z_t, Z_c \otimes Z_t\} \), \( \{Y_c, X_t, Y_c \otimes X_t\} \) and \( \{Z_c, Y_t, Z_c \otimes Y_t\} \) can be obtained by using modified controlled-NOT gates B, C, and D in Fig. 4, respectively.

![Diagram](image.png)

Therefore they can be efficiently corrected. For \( Z_c \otimes X_t \), the circuit is the same as \( X_t \). The \( Z_c \otimes X_t \) error causes the measurement error and a phase-flip error on a data qubit. If we repeat the parity check, the phase-flip error does not change measurement outcomes. Therefore, we still can efficiently correct the measurement error. Given the eventual outcome, we can find out how many measurement errors have happened, which is the smaller number in \( N_+ \) and \( N_- \). Because the measurement error and the phase-flip error are associated, we can correct the phase-flip error given the measurement error number. We apply a \( Z \) gate on one of two data qubits if and only if the number is odd. We remark that phase-flip errors on two data qubits are equivalent, because the state of data qubits after the parity check is an eigenstate of \( Z \otimes Z \).

The second group includes four channels: \( Z_t, X_c, Y_t \), and \( Y_c \). The circuit for \( Z_t \) has two ancillary qubits, which are prepared in the Bell state \( \frac{1}{\sqrt{2}} (|00\rangle + |11\rangle) \) using a Hadamard gate and a controlled-NOT gate, as shown in Fig. 5(a). Two ancillary qubits are measured at the end of the circuit. If the outcome of ancillary qubits is \( |00\rangle \) or \( |11\rangle \), the outcome of the parity check is +1; and if the outcome of ancillary qubits is \( |01\rangle \) or \( |10\rangle \), the outcome of the parity check is −1. We can find that the \( Z_t \) error of the first controlled-NOT gate leads to a measurement error, and \( Z_t \) errors of other two controlled-NOT gates do not have any effect on neither data qubits nor the outcome. For \( X_c, Y_t, \) and \( Y_c \) errors, they can be converted into \( Z_t \) errors by applying appropriate single-qubit gates before and after the controlled-NOT gate,

![Diagram](image.png)
according to circuits A, D, and E in Fig. 4, respectively.

The third group also includes four channels: $Z_c \otimes Z_t$, $X_c \otimes X_t$, $Z_c \otimes Y_t$ and $Y_c \otimes X_t$. Similar to $Z_t$, the circuit for $Z_c \otimes Z_t$ also uses two ancillary qubits prepared in the Bell state, however the readout strategy is different, as shown in Fig. 5(b). When the circuit is error-free, the outcome of the upper ancillary qubit is always $|0\rangle$, and the outcome of the lower ancillary qubit indicates the outcome of the parity check. If the outcome of the lower ancillary qubit is $|0\rangle$, the outcome of the parity check is $+1$; and if the outcome of the lower ancillary qubit is $|1\rangle$, the outcome of the parity check is $-1$. We can find that the $Z_c \otimes Z_t$ error of the first controlled-NOT gate causes a pair of phase-flip errors on data qubits. Because the state of data qubits after the parity check is an eigenstate of $Z \otimes Z$, such a pair of phase-flip errors is trivial. The $Z_c \otimes Z_t$ error in the second controlled-NOT gate causes a phase-flip error on a data qubit and a measurement error on the upper ancillary qubit. It is similar for the third controlled-NOT gate. Therefore, the upper ancillary qubit can be used to detect errors. If the outcome of the upper ancillary qubit is $|1\rangle$ rather than $|0\rangle$, there must be a phase-flip error on one of two data qubits, then we can correct it by applying a $Z$ gate. We remark that phase-flip errors on two data qubits are equivalent. The fourth controlled-NOT gate leads to the measurement error on the lower ancillary qubit, i.e. measurement error of the parity check. For $X_c \otimes X_t$, $Z_c \otimes Y_t$ and $Y_c \otimes X_t$ errors, they can be converted into $Z_c \otimes Z_t$ errors by applying appropriate single-qubit gates before and after the controlled-NOT gate, according to circuits A, D, and E in Fig. 4, respectively.

The fourth group includes the last four channels: $Y_c \otimes Y_t$, $X_c \otimes Z_t$, $X_c \otimes Y_t$ and $Y_c \otimes Z_t$. For the other three groups, dominant errors in controlled-NOT gates result in measurement errors of the parity check, by using corresponding circuits. The fourth group is different, and we cannot find such measurement-error circuits. For channels in the fourth group, we find circuits that dominant errors in controlled-NOT gates result in bit-flip errors on data qubits, which can be efficiently corrected using the repetition code (see Sec. VII A). We introduce two circuits for $Z_c \otimes Z_t$, which are similar to the circuit for $Z_t$, as shown in Fig. 6. In the circuit I, we can find that the $Z_c \otimes Z_t$ error of the first controlled-NOT gate is trivial, and errors of the other two controlled-NOT gates cause the measurement error and a $Y$ error on one of two data qubits. Such correlated errors are equivalent to $Y$ errors occurring before the parity check. In the circuit II, we can find that the $Z_c \otimes Z_t$ error of the first controlled-NOT gate is still trivial, but errors of the other two controlled-NOT gates only cause $Y$ errors on data qubits, i.e. $Y$ errors occurring after the parity check. For $X_c \otimes Z_t$, $X_c \otimes Y_t$ and $Y_c \otimes Z_t$ errors, they can be converted into $Y_c \otimes Y_t$ errors by applying appropriate single-qubit gates before and after the controlled-NOT gate, according to circuits B, C, and D in Fig. 4, respectively.

Now, we consider the 3-channel case, i.e. three of 15 Pauli error channels in the controlled-NOT gate are dominant. The three channels are $\{X_c, X_t, X_c \otimes X_t\}$. The circuit for this set of three channels is the same as the circuit for $X_t$, as shown in Fig. 7. The $X_t$ errors in controlled-NOT gates cause bit-flip errors on data qubits, the $X_t$ errors cause measurement errors, and $X_c \otimes X_t$ errors cause correlated errors. These errors can be efficiently corrected using the repetition code (see Sec. VII). Similar three-error sets are $\{Z_c, Z_t, Z_c \otimes Z_t\}$, $\{Y_c, X_t, Y_c \otimes X_t\}$ and $\{Z_c, Y_t, Z_c \otimes Y_t\}$, they can be converted into $\{X_c, X_t, X_c \otimes X_t\}$ by applying appropriate single-qubit gates before and after the controlled-NOT gate, according to circuits A, C, and F in Fig. 4, respectively.

B. Four-qubit parity-check circuits

Four-qubit parity checks are used in many quantum error correction codes, e.g. the surface code and Steane code. For the surface code, we can construct the parity check circuit according to Fig. 2(b), then the error correction is efficient if the $X_t$ (or $Z_t$, up to Hadamard gates) channel is dominant in controlled-NOT-gate errors. However, for the Steane code, because the code is compact with a distance of 3, the circuit constructed according to Fig. 2(b) is not fault-tolerant. In Fig. 8, we show three fault-tolerant circuit of the Steane code, reported in Refs. [27–29], respectively. Each of the circuits is efficient for a category of 1-channel errors, as follows.

The circuit in Fig. 8(a) is formed by two parts. The first part prepares a cat state. Errors in the cat state are detected by the ancillary qubit on the bottom. If any error is detected at this stage, the cat state is discarded, and the state preparation restarts, which is repeated until the cat state is successfully prepared. The second part loads the parity of four data qubits onto the cat state. Finally, four ancillary qubits are measured in the computational basis, and the value of the parity is the eigenvalue of $Z \otimes Z \otimes Z \otimes Z$ of the four ancillary qubits. We can find that $Z_t$ errors of the first four controlled-NOT gates lead to measurement errors, and $Z_t$ errors of other controlled-NOT gates are trivial. Therefore, this circuit is efficient when $Z_t$ errors are dominant. It is similar for $X_c$, $Y_c$ and $Z_c$ errors, which can be converted into $Z_t$ errors by applying appropriate single-qubit gates before and after the controlled-NOT gate, according to circuits A, D, and E in Fig. 4, respectively.

The second circuit is similar to the first circuit but uses a different readout strategy, see Fig. 8(b). Here, only the outcome of the top ancillary qubit indicates the parity of four data qubits. If the outcome of the top ancillary qubit is $|0\rangle$ or $|1\rangle$, the parity is $+1$ or $-1$, respectively. Outcomes of other three qubits are used for detecting errors. When the circuit is error-free, outcomes of these three qubits are always $|0\rangle$. For $Z_c \otimes Z_t$ errors in the cat state preparation and the last three controlled-NOT gates for readout, we can find that they only lead to measurement
errors on the top ancillary qubit. However, $Z \otimes Z$ errors in the parity loading can cause correlated errors on data qubits and the other three ancillary qubits. By measuring the lower three ancillary qubits, these phase-flip errors on data qubits can be corrected, and only measurement errors of the parity are left. Therefore, this circuit is efficient when $Z \otimes Z$ errors are dominant. It is similar for $X \otimes X$, $Z \otimes Y$, and $Y \otimes X$ errors, which can be converted into $Z \otimes Z$ errors by applying appropriate single-qubit gates before and after the controlled-NOT gate, according to circuits A, D, and E in Fig. 4, respectively.

The third circuit is constructed using a different approach, which uses only two ancillary qubits, as shown in Fig. 8(c). The outcome of the upper ancillary qubit indicates the parity of four data qubits, and the lower qubit is used to detect weight-2 errors. Both of the two outcomes will be used in the later error correction. We can find that $X \otimes X$ errors only lead to measurement errors on the upper ancillary qubit, i.e. incorrect outcome of the parity check. Therefore, this circuit is efficient when $X \otimes X$ errors are dominant. It is similar for $Z \otimes Z$ errors, which can be converted into $X \otimes X$ errors by applying Hadamard gates before and after the controlled-NOT gate, according to the circuit A in Fig. 4.

For other five 1-channel errors, we have not found efficient fault-tolerant circuits.

IV. LOGICAL ERROR RATE

The logical error rate is the probability of errors occurring on logical qubits. In the case of 1-channel errors in the first three groups, we can use circuits in Figs. 3 and 5 to implement the two-qubit parity check. Using these circuits, the dominant errors are measurement errors of the parity check, which can be corrected by repeating the parity check without using any error correction code. With the error-corrected parity check, we can realise universal quantum computation. Therefore, in this scenario, each physical qubit is a logical qubit, and we take the error rate of the error-corrected parity check as the logical error rate.

In the case that an error correction code is used, we repeatedly measure stabiliser generators using parity checks, which are the fundamental operations of fault-tolerant quantum computation. These stabiliser measurements can correct errors generated by themselves and preserve the logical information. To actively operate logical qubits, i.e. implement logical gates, we need to modify the periodic stabiliser measurement circuit, e.g. inserting transversal gates between two stabiliser cycles. These modifications may introduce additional errors, which will be corrected by subsequent stabiliser measurements. A logical gate may contain several rounds of stabiliser measurement, for example the surface code. Because of the fundamental role of stabiliser measurements, we take the rate of logical errors per round of stabiliser measurements as the measure of performance.

V. ERROR CORRECTION FOR DEPOLARISING ERRORS

When the 15 Pauli error channels have similar rates, such as in the depolarizing error model, we need to use quantum error correction codes, e.g. the surface code and Steane code, to correct the errors. For the surface code, the logical error rate per round of stabiliser measurements is [9]

$$p_L \simeq 0.1(100p)^{\frac{4+1}{2}},$$

where $p = 1 - P_{L,I}$ is the total error rate of each controlled-NOT gate, and $d$ is the code distance. As a comparison to biased error channels, we plot the logical error rate versus the physical error rate for the surface code in Fig. 9(a).

The Steane code error correction using the circuit in Fig. 8(a) are simulated numerically, and the logical error rate is plotted in Fig. 11. The decoder will be discussed in Sec. VI B. We fit the logical error rate using the formula

$$p_L = (\alpha p)^2,$$

where fitting parameter is found to be $\alpha = 17.0914$ with the standard deviation $\sigma_\alpha = 0.8915$. The logical error rate versus the physical error rate for the Steane code, according to the fitting formula, is also plotted in Fig. 9(a). We can find that the performance of the Steane code is slightly better than the surface code with the distance $d = 3$. However, it is not a fair comparison because only two-qubit-gate errors are taken into account in our numerical simulations.

VI. ERROR CORRECTION FOR BIASED 1-CHANNEL ERRORS

In the 1-channel case, if the error rate of minor errors is on the fault-tolerant level even without using the error correction, we only need to correct dominant errors. In this case, we can use the two-qubit parity check as the building block. For the first three groups of error channels (see Sec. III A), the error can be corrected by repeating the parity check itself, and the error correction encoding is not needed. For the fourth group, dominant errors result in bit-flip errors, but the parity projection has a reliable measurement outcome. Then, we can use the parity projection to implement the classical repetition code to correct the bit-flip errors. If minor errors are not negligible, we can use a quantum error correction code, the Steane code, to correct minor errors, and we use the parity check circuit that is efficient for correcting the dominant error in the error correction. In this section, we discuss all these situations.
A. Repetition code

For the first three groups of error channels (see Sec. III A), the dominant error only results in the incorrect outcome of the parity check, which can be corrected by repeating the parity check. If the parity check is repeated \(d\) times, the eventual measurement outcome is correct if the number of measurement errors is not larger than \([d - 1]/2\). Therefore, the logical error rate of the parity check is

\[
p_l \simeq \sum_{n=[(d-1)/2]+1}^{d} \left(\frac{d}{n}\right)(Ap)^n(1 - Ap)^{d-n} + dB\frac{\epsilon}{14},
\]

where \(p\) is the error rate of the dominant error in one controlled-NOT gate, and \(\epsilon\) is the error rate of minor errors, i.e. the error rate of each minor error is \(\epsilon/14\). Here, \(A\) is the number of dominant error channels that can cause the measurement error, and \(B\) is the number of minor error channels that cause errors on two data qubits. For example, for the \(X_t\) error (see Fig. 3), the \(X_t\) errors in both of two controlled-NOT gates result in the measurement error, therefore \(A = 2\). In the total 28 minor error channels, 24 of them can cause errors on data qubits, two of them cause the measurement error (which are neglected compared with dominant error channels), and two of them are trivial, therefore \(B = 24\). To obtain Eq. (4), we have assumed that \(p \ll 1\) and \(\epsilon \ll p\).

The logical error rate for the \(X_t\)-dominant error model is plotted in Fig. 9(b). It is similar for the other ten error channels in the first three groups.

For the fourth group, the dominant error results in \(Y\) errors on data qubits but does not affect the outcome of the parity projection. Using the repetition code, we can correct these \(Y\) errors. In the repetition code of distance \(d\), two logical states are \(|0_L\rangle = |0\rangle^{\otimes d}\) and \(|1_L\rangle = |1\rangle^{\otimes d}|.
and stabiliser generators are $I \otimes Z_i \otimes Z_{i+1} \otimes I \otimes I \otimes I$, where $Z_i$ is the Pauli operator on the $i$-th qubit. The circuit for measuring stabiliser generators are shown in Fig. 10. Each full round of parity checks is formed by two layers of parity checks. For the first layer, we use the circuit-I in Fig. 6 such that $Y$ errors are effectively placed before the parity checks; for the second layer, we use the circuit-II in Fig. 6 such that $Y$ errors are placed after the parity checks. In this way, all $Y$ errors only appear between two full rounds of parity checks. Then, we can compare outcomes of the two full rounds and correct $Y$ errors. The $Y$ errors can be successfully corrected if their number is not larger than $[(d-1)/2]$. We note that other errors on data qubits and measurement errors cannot be corrected. The logical error rate can be expressed as in Eq. (4), where $A$ is the number of dominant error channels that cause the $Y$ error on a data qubit, and $B$ is the number of minor error channels that cause other errors.

### B. Steane code

For the Steane code, we take the parity-check circuit in Fig. 8(a) as an example, which can efficiently correct $Z_i$ errors in the one-channel case. It is similar for other circuits in Fig. 8. In terms of the error correction decoder, we use a message-passing scheme that maximises the chance of successfully correcting errors [30, 31]. Before each round of parity checks, there is an input list of all possible error configurations and their probabilities. After the parity checks, the list is updated, because new errors are introduced by the parity-check operations. With the measurement outcomes of parity checks, the probabilities in the list are updated again: only error configurations resulting in the outcome pattern survive, their probabilities are renormalised, and probabilities of all other error configurations are set to zero. In this way, we obtain the posterior distribution. With the posterior distribution, the correction operation is performed according to the most likely error configuration. Then, we need to update the list once more to take into account the effect of correction operations. The output list is used as the input list for the next round. We compute the logical error rates of the Steane code using Monte Carlo simulations, and plot the results in Fig. 11. In the simulations, we take $\epsilon/p = 0.003, 0.01, 0.03$. Then, we fit the logical error rates using the formula

$$p_L = (\beta \epsilon)^2,$$

where fitting parameter is found to be $\beta = 3.7815$ with the standard deviation $\sigma_\beta = 0.0985$. Using the
fitting formula, we compute the logical error rates for \( \epsilon / p = 0.001, 0.01, 0.1 \), which are plotted in Fig. 9(c). We can find that, using the Steane code, a much higher \( \epsilon \) is tolerable compared with the repetition code. This is because the Steane code can correct general errors up to the code distance of 3.

VII. ERROR CORRECTION FOR BIASED 3-CHANNEL ERRORS

In the 3-channel case, see the circuit in Fig. 7, the two-qubit parity check may cause both qubit errors and measurement error. To correct these errors, we need to use the repetition code, similar to the fourth group of error channels in the 1-channel case. As shown in Fig. 10(b), we use the circuit in Fig. 7 in both two layers of parity checks in a full round. Measurement errors are corrected in a way similar to the surface code \([2, 32]\). We use a two-dimensional error-correction lattice to represent errors, on which the vertical edges represent measurement errors. Errors are identified using the minimum-weight perfect matching algorithm \([33]\). The logical error rates are computed using numerical simulations assuming the three dominant errors have the same error rate \( p / 3 \), and the rate of other errors is zero. The results are shown in Fig. 12. We fit the logical error rates using the formula

\[
pl = p_0 (p / p_{th})^{d/2 + \delta},
\]

where fitting parameters are found to be \( p_0 = 0.7335 \), \( p_{th} = 0.0668 \) and \( \delta = 0.9743 \) with the standard deviations \( \sigma_{p_0} = 0.0856 \), \( \sigma_{p_{th}} = 0.0005 \) and \( \sigma_{\delta} = 0.0521 \), respectively. Here, \( p_{th} \) is the threshold of the code.

Similar to the repetition code in the 1-channel case, when the error rate of minor errors is nonzero, the logical error rate is

\[
p_L \simeq p_0 (p / p_{th})^{d/2 + \delta} + dB \epsilon^{12},
\]

where \( \epsilon \) is the error rate of minor errors, i.e. the error rate of each minor error is \( \epsilon / 12 \). In the two controlled-NOT gates in Fig. 7, there are 6 dominant error channels and 24 minor error channels. In minor error channels, 16 of them can cause phase-flip errors on data qubits, 6 of them only cause bit-flip and measurement errors (which are neglected compared with dominant error channels), and 2 of them are trivial. Therefore, \( B = 16 \). The logical error rate for the 3-channel case is plotted in Fig. 9(d).

VIII. SUMMARY

Our results are summarised in Fig. 1. When the error model is extremely biased, i.e. the bias ratio \( \eta = \epsilon / p = 10^{-12} \), the error correction using the repetition code with a code distance smaller than 22 is efficient even when the physical error rate is as high as \( 10^{-3} \). In this case, the difference between 1-channel and 3-channel cases is not significant. Using the Steane code, to achieve the logical error rate of \( 10^{-15} \), we need the physical error rate about \( 10^{-6} \) in the 1-channel case with the bias ratio \( 10^{-2} \), or physical error rate about \( 10^{-9} \) for depolarising errors. If a larger code, such as the surface code with the distance \( d = 7 \), is allowed, the fault-tolerant quantum computation can be realised at the physical error rate \( 10^{-6} \) even for depolarising errors. We can find that the biased error model can significantly reduce the demanding requirement for achieving fault-tolerance, which is similar to the case of the Majorana fermion quantum computation \([34]\). To realise the fault-tolerant quantum computation in the deep sub-threshold regime, we may need to either at least reduce the physical error rate to the level of \( 10^{-6} \) or developing physical systems with a highly biased error model.

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[1] M. A. Nielsen and I. L. Chuang, *Quantum Computation and Quantum Information*, Cambridge University Press, Cambridge, (2010).
