Nanosecond machine learning event classification with boosted decision trees in FPGA for high energy physics

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Abstract

We present a novel implementation of classification using the machine learning / artificial intelligence method called boosted decision trees (BDT) on field programmable gate arrays (FPGA). The firmware implementation of binary classification requiring 100 training trees with a maximum depth of 4 using four input variables gives a latency value of about 10 ns, independent of the clock speed from 100 to 320 MHz in our setup. The low timing values are achieved by restructuring the BDT layout and reconfiguring its parameters. The FPGA resource utilization is also kept low at a range from 0.01% to 0.2% in our setup. A software package called fwXmachina achieves this implementation. Our intended user is an expert in custom electronics-based trigger systems in high energy physics experiments or anyone that needs decisions at the lowest latency values for real-time event classification. Two problems from high energy physics are considered, in the separation of electrons vs. photons and in the selection of vector boson fusion-produced Higgs bosons vs. the rejection of the multijet processes.

Keywords: Data processing methods, Data reduction methods, Digital electronic circuits, Trigger algorithms, and Trigger concepts and systems (hardware and software).

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1 Introduction

Modern high energy physics experiments are saving more data at a faster rate than ever before. The combination of the Large Hadron Collider (LHC) [1] that collides proton bunches at 40 MHz and an apparatus to record the energy deposits and their patterns coming from the collisions, such as the ATLAS and CMS experiments [2, 3], leads to a large data volume at a high rate. Without a reduction of incoming data the volume is prohibitively large. Furthermore, most data acquisition systems have limitations on the readout electronics that do not allow the data to be saved at the collision rate. The combined issues of data storage and data acquisition readout limitations coupled with the fact that the collisions of interest occur at a small fraction of the total number of collisions, typically one part in a few thousand, necessitate the need of a multi-level trigger to help throttle the data [4–6].

The first level (level-1) trigger has stringent demands that it produces a decision within a few microseconds depending on the system requirements, or a fraction of the total latency budget for a given algorithm within the system. The level-1 triggers typically consist of custom electronics boards with field programmable gate array (FPGA) and/or application specific integrated circuit (ASIC) chips that process a reduced amount of the total data generated by the collision [7–10]. The algorithms on the chips are often simplified versions of what is implemented in software. For example, in the ATLAS experiment, the sliding window algorithm [7] is implemented on the chip for hadronic jet reconstruction compared to the anti-kt algorithm [11] that is implemented in software. In many of the cases, algorithms on the chip involve cut-based requirements when multiple variables are computed for a given algorithm, such as the isolation requirements for electrons [12]. There are also examples of increasingly sophisticated algorithms in the level-1 trigger. For example, the ATLAS level-1 topological trigger computes the invariant mass of the two-jet system [13]. More recently, machine learning (ML) / artificial intelligence (AI) algorithms have started to make an appearance at level-1 [14, 15].

A list of abbreviations and technical terms is given in appendix A.
Among the popular ML algorithms in high energy physics are boosted decision trees (BDT) and neural networks. For the past few decades, such methods have been used in the analysis of the data recorded by experiments [16–19], e.g., in the discovery of the Higgs boson [20, 21]. Furthermore, ML algorithms have been utilized in the reconstruction of low-level detector information to produce physically meaningful variables [22–26]. A variety of ML algorithms have been implemented in the level-1 and the subsequent software-based high level trigger of the ATLAS and CMS experiments [5, 6, 15]. This demand for ML is driven by the need for higher signal sensitivity for event classification in an environment where the signal-to-background ratios are lower. Furthermore, with the recent advancements in the FPGA size, as well as progress in ML, implementing more advanced algorithms on FPGA and ASIC chips has become an active area of research in high energy physics [14, 15, 27–36]. This area is also lively outside of high energy physics [37–45]. It is important to note that the implementations in trigger systems focus on the classification (also known as application, evaluation, or inference) of ML to use in real-time systems, rather than in the training of the ML.

We present a novel implementation of the evaluation of BDT on FPGA that focuses on speed and design simplicity. The low timing values are achieved by restructuring the BDT layout and reconfiguring its parameters after the ML training step. The software package called \texttt{fwXmachina} produces the optimized BDT for High Level Synthesis (HLS), which it subsequently converts to firmware in hardware description language.

Two binary classification problems are considered to give realistic use cases as well as to illustrate the performance of the design. The first problem is in object identification in order to discriminate electrons vs. photons. The second problem is in the event classification of the vector boson fusion-produced Higgs boson vs. the multijet process.

The paper is organized as follows. The rest of this section gives the overview of \texttt{fwXmachina}. The next three sections describe the stages of implementing a BDT in firmware and validating its results. Sections 2, 3, and 4 discuss the ML training, Nanosecond Optimization, and firmware design, respectively. Section 5 gives the physics performance and the FPGA cost of running the algorithm on the physical FPGA. Finally, section 6 concludes. Within the paper, the following parts may be of particular interest to some readers. The set of benchmark parameters are defined in section 5.1 and parameter scans in section 5.2. Comparisons with existing tools are made in section 5.4 and appendix G.

### 1.1 fwXmachina, software package for ML/AI classification on FPGA

\texttt{fwXmachina} is a software package that consists of three sequential stages: ML training, Nanosecond Optimization, and firmware design.\footnote{The source code and the technical documentation are available at fwx.pitt.edu.} The workflow showing the structure and interaction with external data and external input is shown in figure 1.

There are various approaches in the literature to optimize the result of the ML training for
efficient firmware implementation. One approach is to consider a penalty term in the feedback loop during the training process to balance the FPGA cost with physics performance [27]. Another approach is to optimize the result of the training process with firmware implementation in mind, such as to choose the precision of the input variable values [28]. We expand on the latter approach in Nanosecond Optimization.

Figure 1: Workflow diagram for the fwXmachina package. The flowchart reads from left to right following the thick arrows that connect the three main stages: ML training with the software (SW) interface, Nanosecond Optimization, and firmware (FW) design. The interactions with external inputs (shown in flat white figures) and external software packages (shown in gray cubes) are shown by thin vertical arrows. Nanosecond Optimization is shown in more detail later in figure 3. The information flow for the user input is diagrammed in the appendix (figure 24).

The first stage is ML training, where the structure of the ML and its parameters are determined. The training is done with available open source external software packages. In this paper, we use BDT as the ML method and Toolkit for Multivariate Data Analysis (TMVA) for the external software package [46]. The current version of the code supports binary classification. The user provides fwXmachina the data samples with input variables that characterize each event. The output of TMVA is handed off to the next stage.

The second stage is Nanosecond Optimization, in which the structure of the BDT and its parameters are optimized for both physics performance and FPGA cost. The physics performance is evaluated by considering the receiver operating characteristics (ROC) curves. The “FPGA cost” is evaluated by the timing values and the resource utilization using Xilinx Vivado HLS [48]. At this point, the user chooses the working point that best suits the problem at hand. The performance considerations (center circle in figure 1) and user input (diamond) is part of Nanosecond Optimization.

The third stage is firmware design. The inputs to Xilinx Vivado are created [49, 50]. The inputs are a combination of HLS and hardware description language (HDL). We target VHDL, a type of HDL, for the output. The output, after synthesizing with Vivado, is the firmware in bitstream format.

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3We plan to support scikit-learn [47] and other such packages in the near future.
to be programmed on to the FPGA. After the programming, the FPGA is prepared to repeatedly execute the algorithm on incoming unclassified events that are fed to it.

2 ML training

The ML training stage is executed by external packages as described in the previous section.

For the problem of binary classification of signal vs. background in a supervised learning environment, a given ML method needs to be trained using samples containing events labeled as “signal” or “background.” The training process starts with an initial set of parameters for the chosen ML architecture, such as the decision tree structure for BDT and layer structure for neural network, that is iteratively improved by a feedback loop consisting of a metric.

We emphasize that in the level-1 trigger for high energy physics, the training step is typically done before the real-time evaluation. The latency requirement of the level-1 trigger is not a constraint for the training step that uses training samples that are prepared beforehand. In contrast, for the operating conditions involving incoming data at high speeds, e.g., 40 MHz at the LHC, the algorithms of the level-1 trigger must make decisions at time scales of microseconds, or a fraction thereof, depending on the algorithm’s requirements within the level-1 trigger.

While the ML method of interest of this paper is BDT, comparisons are made to the cut-based method. Cut-based classification, also referred to as “rectangular cuts,” is discussed for two reasons. The first is that the BDT result is compared against cut-based results. The second is that we have implemented it in fwXmachina.

Two problems are considered. The “object identification” and the “physics trigger” are used to evaluate the firmware performance in different ways. The former is used to define the benchmark configuration (section 5.1) and to scan one parameter at a time starting from the benchmark (section 5.2). In contrast, the latter is used to evaluate configurations with many parameters far from the benchmark (section 5.3).

2.1 Electron vs. photon

The example considered for the “object identification” problem is to separate electrons vs. photons. Studies are done with the fwXmachina software to make comparisons of approximations that are made for the FPGA implementation. For example, ROC curves for varying number of bits for the input variable values are compared.

The electron-photon problem is interesting in high energy physics, especially for the level-1 trigger. Due to latency constraints the level-1 trigger typically receives only a fraction of the calorimeter data containing localized energy deposits without much, if any, additional tracker data. This is a challenge because whereas the electron leaves ionizing energy deposits in the tracker due to its electrical charge, the photon leaves no such pattern as it passes through the tracker until it hits the calorimeter. In the calorimeter, both an electron and a photon leave similar patterns
of energy deposits. Some differences arise where electrons and photons deposit energy in the calorimeter as the electromagnetic shower develops laterally through the detector material. An electron deposits energy primarily by bremsstrahlung radiation and a photon deposits energy mainly by pair production [51]. Therefore, an electron tends to deposit its energy towards the beginning of its entry to the calorimeter, while a photon deposits its energy at least one radiation length later in its passage through the detector material. These small differences are difficult to distinguish using the traditional cut-based method and may be better suited for ML [52, 53].

The BDT architecture is trained using the adaptive boost (AdaBoost) metric [54]. Since we compare our BDT results against the cut-based method, the latter is trained using the genetic algorithm [55]. The data samples of simulated events are obtained from ref. [56], with one half being used for training and the remaining half is used for testing. The BDT output score distributions for the test sample are shown in the left plot of figure 2 for the benchmark configuration described later (section 5.1). The similarity in the trend for the two distributions in the plot demonstrates that this is a difficult problem. However, the shape differences in the tails of the distributions allow for a superior separation compared to the cut-based method.

The details of the training setup, the data samples, and the input variables are given in appendix B.1.

![Figure 2: BDT output score distribution for electron vs. photon (left) and VBF Higgs vs. multijet process (right). The left figure uses the yes/no leaf metric that results in a range between −1 and 1. The right figure uses the purity metric that results in a range between 0 and 1. For the right plot, the following details are notable. One BDT is trained for the binary classification problem of VBF $H \rightarrow \text{invisible}$ vs. multijet. This BDT is then used to evaluate the output score of events in the three samples. Events with less than two jets are not plotted, but they are considered when making the ROC curves (figure 9).](image)
2.2 VBF Higgs bosons vs. multijet process

The example considered for the “physics trigger” problem is to discriminate between an event containing a vector boson fusion-produced Higgs boson (VBF Higgs) vs. multijet process. The former is considered “signal” and the latter is considered “background.”

The VBF Higgs vs. multijet problem is challenging at the LHC, especially in the level-1 trigger. We consider an algorithm to identify the signal by using the two “VBF jets,” typically with a large gap in pseudorapidity, that emerge from the process. The challenge for such an algorithm is that the two-jet sample is dominated by the multijet process at the LHC. Such an algorithm is of interest to the level-1 trigger, because it allows the selection of events containing Higgs bosons in a way that is agnostic to the decay pattern of the Higgs boson [57–60]. In particular, ref. [60] considers this problem using a neural network.

The training setup is similar to the setup for electron-photon, with 100 training trees at a maximum depth of 4. We generated the data samples using publicly available tools (appendix B). Half of the data is used for training and the remaining half is used for testing. Later in section 5.3, we compare the result of our BDT analysis against results using the cut thresholds for the ATLAS experiment. The BDT is trained for VBF $H \rightarrow \text{invisible}$ vs. multijet, but it is used to categorize VBF $H \rightarrow \text{invisible}$, and multijet. As the goal is to use only the VBF jets to identify the production of Higgs bosons, we also test the trained BDT on the signal process VBF $H \rightarrow 4b$, which contains jets in the decay process in addition to the one from the production process. The BDT output score distributions for the test sample is shown in the right plot of figure 2 for the optimized configuration described later (section 5.1). The clear shape differences between the two signal distributions and the background distribution indicate that there are powerful input variables that separate them. Moreover, the distributions demonstrate that VBF Higgs events can be separated from multijet background in a way that retains sensitivity for two different Higgs boson decays. There is a slight degradation in performance when the Higgs boson decays to a final state with jets, such as $4b$, as these jets can be miscategorized as VBF jets.

3 Nanosecond Optimization

Given the experimental constraints at the LHC and other real-time systems, such as latency and resource limitations in FPGA-based triggers, our question is how can we best implement ML in firmware to achieve the most optimal physics performance? In this section we describe the restructuring of the BDT layout as well as the reconfiguration of its parameters.

Nanosecond Optimization is done in six sequential steps: Tree Flattener, Forest Merger, Score Finder, Score Normalizer, Tree Remover, and Cut Eraser. These steps are illustrated in figure 3. The first three steps can be grouped conceptually to achieve “flattening” and the second three to achieve “optimization.” The first two steps drive the firmware design whereas the remaining four steps are not as critical to the design. Therefore, the two in the former group are explained in
more detail in the rest of the section, while those in the latter group are described in appendix C.

Figure 3: Workflow of Nanosecond Optimization. The four boxes shaded in grey denote steps that are not required to have functional firmware, but are often critical in improving the firmware’s performance.

3.1 **Tree Flattenener**

The **Tree Flattenener** converts a tree with maximum depth $D$ to a tree with depth 1.

A decision tree is characterized by a binary structure that considers $V$ variables, $\tilde{x} = \{x_0, \ldots, x_{V-1}\}$, per event.$^4$ An event recurses down the tree starting at the root node and ends in one of the terminating leaf nodes. An example graphical representation of a tree with $D = 2$ and $V = 2$ is shown in the top-left diagram of figure 4. Two comparisons $q_i$ and $q_{ii}$ place an event into one of three leaves with the corresponding BDT output scores $O$ in the following if-then-else structure:

- If $x_a \geq c_i$, then terminate at $O_1$
- Else
  - If $x_b \geq c_{ii}$, then terminate at $O_{01}$
  - Else terminate at $O_{00}$.

We note that the second if-then-else block must wait for the decision of the first if-then-else block in a sequential manner. The distribution of the events for the two variables $x_a$ and $x_b$ can be visualized as dots on a two-dimensional plane in the top-right diagram in figure 4, where the cut thresholds $c_i$ and $c_{ii}$ are represented by vertical and horizontal boundaries, respectively. In this plane three rectangular regions define $O_1$, $O_{01}$, and $O_{11}$.

$^4$More detail on the notation is given in table 5 in appendix A.
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Figure 4: **Tree Flattener** example. A tree is flattened by compressing the vertical structure into a tree of depth of 1. The conventional tree (top row) is flattened to the one depth structure (bottom row) by the insertion of “ghost” dotted lines that allow for the thresholds in each variable to be considered independently. The diagram considers an example of a one tree structure with two variables ($x_a, x_b$) and one cut threshold for each variable ($c_i, c_{ii}$). The node structure (left column) shows the decision making process, where the final terminating leaves contain the BDT output score $O$. The conventional node structure is an iterative procedure according to the number of depth of the tree. The graphical representation (right column) on the two-dimensional plane of ($x_a$ vs. $x_b$) shows the range defined by each threshold. For the graphical representation of the flattened tree (bottom right), a “ghost” dotted line is inserted—corresponding to the $O_{10}$ and $O_{11}$ terminating leaves in the node structure (bottom left).
The decision tree is flattened to be optimized for firmware implementation. The flattener extends every cut threshold through the entire $V$-dimensional hyperspace to form $V$-rectangular bins. The example above with $D = 2$ and $V = 2$ leads to the following if-then-else structure:

- If $x_a \geq c_i$ and $x_b \geq c_{ii}$, then terminate at $O_{11}$,
- Else if $x_a \geq c_i$ and $x_b < c_{ii}$, then terminate at $O_{10}$,
- Else if $x_a < c_i$ and $x_b \geq c_{ii}$, then terminate at $O_{01}$,
- Else if $x_a < c_i$ and $x_b < c_{ii}$, then terminate at $O_{00}$.

We note that, in contrast to the above if-then-else, the four comparisons are made simultaneously in parallel. There are four “bins,” $N_{bin} = B = 4$, that correspond to each BDT output score. The scores $O_{11}$ and $O_{10}$ correspond to the same value as $O_1$ in the above example. The bottom two diagrams of figure 4 illustrate the impact of flattening.

In summary, the flattener transforms the operation from a recursion problem into a binning problem. This is efficient on an FPGA because each variable can be binned in parallel. Now that a tree is flattened into one with a single depth with $B$ bins, two binning algorithms are available in *fwXmachine*. The details of the binning algorithms are given in appendix C.1.

### 3.2 Forest Merger

The Forest Merger combines multiple decision trees into one tree. Consider a forest $\phi$ that contains $T$ decision trees, $\tau = \{\tau_0, \ldots, \tau_{T-1}\}$, each with a set of corresponding boost weights, $\{W_0, \ldots, W_{T-1}\}$. It is easier to describe the procedure with an example. We consider two trees, $T = 2$, each considering two variables, $V = 2$. Suppose the first tree $\tau_\alpha$ is the same one as in figure 4 and the second one $\tau_\beta$ is similar with different cut threshold values. The graphical representation of the two-dimensional distribution is given in the first two diagrams of figure 5.

The merged tree $\tau_{\alpha\beta}$ considers the cut thresholds from both of the trees simultaneously. The combined BDT output score in each bin is the weighted sum using the normalized boost weights $w_t = W_t / \sum_{t'} W_{t'}$. The two-dimensional representation of $\tau_{\alpha\beta}$ is given on the right hand side of figure 5.

The flattened structure of a merged tree is indistinguishable from a single tree. They both consist only of the set of cut thresholds and a set of event-independent boost weights. In practice, we typically merge a forest down to a handful of trees instead of a single tree, i.e., $\phi \rightarrow \{\tau_0, \ldots, \tau_{F-1}\}$ with $F \leq T$. For example, a forest of 100 trees is often divided into ten groups of 10 trees; with each group of tree merged into a single tree. This smaller set of 10 “final trees” is fed to the Score Finder, which associates an output score to each bin of the tree.

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5 References [61, 62] describe a similar algorithm in ML theory.
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Figure 5: Forest Merger example. Visual binning example for two variables ($x_a$ vs. $x_b$) to demonstrate the merging of two flattened tree structures into one tree. The example given here continues the two-dimensional representation of figure 4. Two trees are considered ($\tau_a$, $\tau_b$), corresponding to the left and middle diagram, respectively. In each region defined by the thresholds $c$, the output scores are printed as, for instance, $O_{\alpha00}$ that correspond to tree $\tau_a$ and bin 00. The vertical and horizontal lines of $\tau_a$ and $\tau_b$ are superimposed on to one two-dimensional plane in the merged $\tau_{\alpha\beta}$ diagram on the right. The output score in each region of the merged tree is the weighted average in the rectangular region defined by the combined thresholds. The colors are shaded to suggest the output score value.

4 Firmware design

The Evaluation Processor encodes the entire forest of the BDT as illustrated by figure 6. The diagram flows from left to right with the vector of $V$ input variables $\vec{x}$ being the input to the Processor. On the other side the BDT output score $O$ exits.

First, the bus tap does the fanout of the vector $\vec{x}$ into $V$ individual values. Each flattened tree $\tau_i$ is represented by a look up table LUT$_i$ that considers the result of $V$ instances of Bin Engines. Each Bin Engine processes one of the input variables $x_v$ whose result $b_v$ is the bin index of the flattened tree $\tau_i$. Each LUT$_i$ associates the list of bin indices $\{b_0, \ldots, b_{V-1}\}$ with the output score of the tree $\tau_i$, $O_{\tau_i}$. The set of output scores from all $T$ trees is combined and transformed, if necessary, in the Score Processor, which is the firmware implementation of Score Normalizer. The transformation is a trivial one for AdaBoost whereas gradient boost (GradBoost) applies the tanh function to the sum of individual response scores [63]. A description of the tanh implementation is given in appendix C.3 (figure 21). Finally, each set is duplicated $T$ times for $T$ trees in the forest.

The heart of the Evaluation Processor is the Bin Engine, whose design localizes the data so that the output score can be assigned. Being the most important and computationally taxing component of the circuit, two Bin Engines are employed and optimized for specific situations, corresponding to the two bin algorithms mentioned in the rest of the section.
Figure 6: Example layout of the Evaluation Processor that implements the BDT. The dataflow is left to right with a set of $N$-bit integers $\bar{x}$ as input. Look up table $\text{LUT}_t$ corresponds to decision tree $\tau_t$ ($t = 0, \ldots, T - 1$); a Bin Engine obtains the bin index $b_v$ for one input variable value $x_v$ for variables $v = 0, \ldots, V - 1$. The Score Processor combines the output scores of each decision tree and transforms the result, if necessary. The thick lines and arrows indicate the latency incurred by accessing external memory, either external LUT or BRAM.
We note here that the cut-based method is implemented separately. The details are given in appendix D.1.

4.1 Bit Shift Bin Engine

The Bit Shift Bin Engine (BSBE) relies on bit shifting to achieve fast binning. The input is the value of one input variable \( x_v \). The output is the bin index \( b_v \) for that variable.

The input value is localized by decomposing a bin into the set of “grid spaces” that cover the range of the final bin. To do this the binning algorithm begins by shifting the input coordinate by various amounts to calculate its index in the many layers of grids. The BSBE yields the coordinate of the input when evaluated on the grid corresponding to the amount shifted.

The gate-level diagram at the top of figure 7 shows an example of BSBE. The numerical binning example that accompanies it illustrates this process. We follow the dataflow for an input value of \( x = 13 \). The Engine parameters are the number of bits \( N = 4 \) and the number of layers \( L = 3 \), with three layers \( \alpha, \beta, \) and \( \delta \). The Cut Eraser, in our example, eliminates many of the possible bins to arrive at total number of bins \( B = 4 \) for bins \( b = 0, 1, 2, 3 \). The erased bins are denoted by the dotted lines in the numerical example and correspond to the dotted lines in the diagram. In the diagram, we boldface AND\(_2\) and \( \text{i} \)n\(_2\) to highlight the activated path that leads to output \( b = 2 \).

In general, the location of the input is then represented as an \( L \)-dimensional vector, where \( \ell < L \) is the grid index in which the event input is evaluated. Every bin can thus be represented with a unique set of vector components. The components are compared in one of the \( L \cdot B \) comparators, where \( B \) represents the total number of bins for a given decision tree. The outputs of each \( L \) group of comparators are fed in to an AND operation that indicate the correct bin index in a “one-hot” style, where only one AND gate returns a 1 result and the rest return a 0 result. Finally, the vector of \( B \) inputs to the LUT converts the one-hot results into an output index. In the example in the figure, the array of \([0, 0, 1, 0]\) is converted to index 2 since it represents the number 0010 in binary format.

The major benefit of this approach is the extremely low latency. The parallel structure of the bit-shift divisions and of the vector comparisons trades a more quickly growing area usage for the decreased latency that it enjoys. Another reason as to why the output is ready in such a short time is the fact that no memory is directly accessed. All of the constant values that are compared to the vector components are distributed throughout the FPGA fabric and accessible without incurring access latency.

A potential limitation, depending on the use case, is that the bin boundaries, i.e., the cut threshold

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\(^6\)A short refresher of the bit shifts introduces some of the nomenclature. The bit-shift operator is equivalent to an arithmetic shift right (ASR) in standard nomenclature, i.e., the binary representation of a number is shifted to the right by a specified amount and discards the least significant bit (LSB). This operation divides the number by a factor \( r^n \), where \( r \) is the radix and \( n \) is the number of shifts. This is already common intuition in radix-10. That is, when one wishes to divide a number by a power of 10, one simply has to discard that many least significant digits. In CPU and FPGA architecture, integers are represented in radix-2, and all the same can be said about bit-shifting being used to divide by a power of 2.
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Bit Shift Bin Engine (BSBE)

Actual layout depends on ML training result

| LUT / BRAM |
|------------|
| Not explicitly used, may be used indirectly |

| LUT | active input array → output index |
|-----|----------------------------------|
| in0 | out 2 b |
| in1 |
| inB-2 |
| inB-1 |

Figure 7: Example gate-level diagram of the Bit Shift Bin Engine. The dataflow is left to right with an \( N \)-bit integer \( x \) as input. The \( x \) is binned in \( L \) binary layers via bit-shift, comparator, and \( \text{AND} \) gates. The dotted elements are not present for the example considered, but are drawn for completeness. The comparator constants that correspond to each layer (\( \ell = 0, \ldots, L - 1 \)) are denoted as \( \alpha, \ldots, \delta \), respectively. There are \( B \) copies of \( \text{AND} \) corresponding to the \( B \) bins. Since only one \( \text{AND} \) gate (say, at position \( b \)) uniquely returns \( \text{in}_b = 1 \) while all others return 0, the list of \( \text{in} \) is converted in a LUT via an active array to \( \text{out} = b \).

Numerical Binning Example

| \( x \) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|-------|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| \( \alpha \) | | | | | | | | | | | | | | | | | |
| \( \beta \) | | | | | | | | | | | | | | | | | 2 | 3 |
| \( \delta \) | 0 | 1 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |

Parameter Max Value

\( N = 4 \), input bits

\( \ell = 0 \), layer no.

\( \ell = 2 \), layer no.

\( \ell = 3 = L - 1 \), max layer

\( B = 4 \), max bin
values, are restricted to binary representation. For users who desire more flexibility in the bin boundary values, the threshold approach using the look up approach is presented next.

### 4.2 Look Up Bin Engine

The Look Up Bin Engine (LUBE) utilizes a modified linear search algorithm optimized for parallel implementation on an FPGA. A commonly used conceptual approach to the bin problem is to loop over each bin, comparing the event value to the bin edges, and breaking out of the loop when the matching bin is found. This implementation is not well suited for hardware acceleration because the number of loops performed varies based on the event and it requires a large number of comparisons. Instead we propose a solution that uses two problem-specific optimizations to achieve better performance. The gate-level diagram at the top of figure 8 shows an example of the implementation.

The first optimization for binning recognizes that LUBE always receives the bin edges in sorted order. Therefore, the problem can be reduced from a generic binning problem to a more simple search for a bin edge that is larger than the event value. When that edge is found, it is then known that the event falls in the smaller bin adjacent to that edge. This reduces the total number of comparisons required by half.

The second optimization addresses the issue of an indeterminate loop count. Instead of returning after the correct bin is found, the algorithm should always loop over the full number of bin edges. This allows more of the loop to be implemented in parallel, leading to lower latency and higher throughput. To achieve this we simply loop through the entire length of the bin edge vector and set a flag when the first valid bin is found. The rest of the bins, while valid because their upper edge is larger than the event value, will not be indicated as such due to the flag being set.

In comparison to BSBE, LUBE typically has a higher latency value due to the fact that the LUBE method is designed to accept arbitrary bin edges, whereas the BSBE method requires bin edges on certain set intervals. The LUBE approach also affords more flexibility in which resources are used to implement the Bin Engine.

Another advantage of LUBE is its ability to produce more easily synthesizable source code. The BSBE method is known to, at times, produce code that HLS struggles to synthesize. This issue arises when HLS is asked to perform excessive loop unrolling or is provided with unmanageably large source code. These cases can result from large values of $N_{\text{bin}}$ or a high dimensionality problem, e.g., a large number of input variables. Due to its structure, source code generated using the LUBE method can often be synthesized in these cases where BSBE struggles. This is a key advantage and it provides firmware designers with the added flexibility when implementing their design.

### 4.3 Firmware verification and validation

The firmware is checked using C-synthesis and RTL-level HLS co-simulation of the C code from fwXmachina. Two checks are done. First, the firmware co-simulation results are verified against
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Figure 8: Example diagram of the Look Up Bin Engine. The dataflow is left to right with an $N$-bit integer $x$ as input. The $x$ is binned by comparison with the threshold values $\alpha, \ldots, \gamma$ in the comparators gates. The NAND gate of all of the XOR results gives the result of the last $B - 1$ bin. Thick arrows indicate the latency incurred by accessing memory, either LUT or BRAM.
the results using a physical FPGA. We consider different FPGA choices, clock speeds, and versions of Vivado HLS. Second, the firmware co-simulation results are validated against the results using software simulation of the algorithm. All tests use the same benchmark configuration described in the next section (table 1).

The summary of the tests are given below. More details are given in appendix D.2, in which the test benches are also illustrated (figure 24).

**Verification against physical FPGA**

For verification, one input test vector is considered by the synthesized bitstream file, which is programmed on the physical FPGA. Two different FPGA setups are considered.

- Virtex UltraScale+ FPGA VCU118 Evaluation Kit (EK-U1-VCU118-G), our benchmark,
- Artix-7 FPGA on Zynq-7020 System on Chip (SoC), a smaller FPGA.

The Ultrascale+ is run on three clock speeds—320 MHz, 200 MHz, and 100 MHz—while the Artix-7 is run on 100 MHz. In all scenarios, the actual BDT output score from the physical FPGA matches the expected result from co-simulation. The actual latency matches the estimated result. Moreover, the latency is constant for Ultrascale+ at around 10 ns and does not depend on the clock choice. The plot of the clock independence is given in appendix D.2 (figure 25).

One notable observation regarding latency is made regarding Vivado HLS versions. For the 320 MHz clock speed, the latency using version 2019.2 confirmed the 3 clock ticks while version 2018.2 resulted in a slightly higher value at 4 clock ticks. As the BDT output score is verified for the two versions, the difference in latency is likely due to improvements in the more recent version. The actual-to-estimated ratios matched for the two tests.

The resource utilization on the actual results is generally equal to or smaller than the C-synthesis estimate. The actual-to-estimate ratio for the look up table usage range from 0.1 to 0.4. The ratios for flip flop usage range from 0.7 to 1.1 with the exception of one case for Ultrascale+ at 100 MHz, where the actual number of flip flops matches that of the other clock speeds, but is estimated to use a negligible amount. The ratios for block RAM range from 0.4 to 0.7. No ultra RAM is used and digital signal processor usage remains negligible.

In summary, the latency results match exactly while the actual resource utilization is generally smaller than what is reported by C-synthesis. This suggests that our synthesis results are conservative estimates and that the actual usage is likely to be smaller.

As for the BDT output score for a few test vectors, no difference is seen in all tests.

**Validation against software simulation**

For validation, $10^5$ input test vectors are considered for 200 different BDT configurations.

**fwXmachine** provides a software simulation that includes the conversion of floating point values to bit integers. A detailed diagram is given in appendix D.2 (figure 24).
The co-simulation results are compared to the software simulation. No difference is seen for the BDT output score.

5 Physics performance and FPGA cost

The physics performance and FPGA cost are described for a given BDT configuration.

Physics performance is measured by considering the ROC curve with two metrics, depending on the problem. The ROC curve is a representation of operating points in a two-dimensional space to display the acceptances of signal and background events. The efficiency (also called acceptance) of signal events ($\varepsilon_S$) is defined as the fraction of the number of signal events that pass the algorithm criteria divided by the total number of considered signal events. The background acceptance ($\varepsilon_B$) is similarly defined for background events. The axes of the ROC curves are chosen to suit the problem at hand. The $x$-axis shows $\varepsilon_S$ in linear scale, but the $y$-axis can be either the background acceptance $\varepsilon_B$, the background veto $(1 - \varepsilon_B)$, or the background rejection factor $(1/\varepsilon_B)$.

The first metric is the area under the ROC curve (AUC) when plotting in the $(x, y)$ plane with $(\varepsilon_S, 1 - \varepsilon_B)$. The second metric is to measure the relative change in $\varepsilon_S$ for a fixed value of $\varepsilon_B$, i.e., a “fixed background rate” study. The physics performance results are obtained using the fwXmachina simulation software to mimic the treatment of integers in firmware, such as the $N_{bit}$ parameter.

“FPGA cost” is the collective term we use to refer to the resource utilization estimates and the timing results as estimated by C-synthesis and the co-simulation of the firmware, respectively. The timing result refers to the latency and interval measurements. The resource utilization refers to the look up tables (LUT), flip flops (FF), block RAM (BRAM), ultra RAM (URAM), and digital signal processor (DSP) usage. The FPGA cost results are obtained from C-synthesis and the co-simulation. HLS programs are, in our experience, designed to be conservative with their timing and resource estimations. Timing constraints are upheld by the synthesizer by ensuring the predicted maximum possible clock speed for a given design is higher than the target clock speed by a certain uncertainty factor. This uncertainty factor is relatively large and maximum clock estimates are made conservatively, which ensures that the target clock speed is realistic for the design. In cases where the estimated clock period exceeds the target period, fwXmachina reports an error to the user. No such errors are reported in any studies in this paper.

The final considerations of the choice of the configuration parameters depend on the physics goals as well as the experimental constraints of the user. In general, the better the physics performance the higher the FPGA cost. We explain the conceptual trends by giving examples of how the optimization can be done, with an emphasis on the trade-offs between physics performance and FPGA cost.

In statistical terminology, the four quantities correspond to the true positive rate (TPR), false positive rate (FPR), true negative rate (TNR), and the inverse false positive rate (1/FPR), respectively. The FPR and FNRR are also called type I error and type II error, respectively. The correspondence of the terms are listed in appendix A (table 4).
This section is organized into four subsections. First, the benchmark configuration is defined using the electron-photon problem. Second, using this problem we scan one parameter at a time starting from the benchmark. Third, we consider configurations far from the benchmark using the VBF Higgs problem. Finally, we end the section with a comparison to previous results.

In particular, the technical terminology used for the FPGA cost are defined in appendix A (table 6); the performance metric and the BDT settings that are varied are listed in appendix A (table 7). The values reported in this section are obtained using a setup that is illustrated in more detail in appendix D.2 (figure 24).

5.1 Benchmark parameters

A benchmark configuration is defined in order to compare variations with respect to the benchmark. We choose the electron-photon problem for the benchmark. Our choice for the configuration, such as a BDT with 100 training trees and 4 input variables, is intended to reflect a realistic implementation in a high energy physics environment.

Table 1 lists the configuration parameters in three groups followed by the final group that gives the FPGA cost. The first group is for the FPGA setup. It details the hardware and development environment. It also mentions the interface protocol, a changeable option. This choice in interface can impact the reported latency, so a “none” interface is chosen to most accurately estimate the latency of the algorithm itself. The second group is for the ML training setup, which configures TMVA. The third group is the firmware-related parameters for the Nanosecond Optimization. For example, the user may choose different numbers of bits for different quantities. This variability is useful when some variables need more precision to perform well. For the benchmark, 8 bits are used for all quantities. Although the number of bins is not a configurable parameter, but rather a result of the configuration, we note the value in the table as it will be seen to scale with FPGA cost.

The final group in the table reports the FPGA cost. Algorithm latency is 3 clock ticks and the interval is 1 clock tick, which corresponds to about 10 ns and 3 ns, respectively. The other five parameters are the amount of logical units used on the FPGA. A minimal amount of LUT and BRAM is used at less than 0.2% of the available resources. A negligible amount of FF is used at 0.01% of the available resources. No URAM or DSP is used.

5.2 Results of scanning from the benchmark

Starting from the benchmark point, we scan one parameter to observe its effect on the physics performance and the FPGA cost. For the physics performance study we vary \( N = N_{\text{bit}} \), the number of bits used for the cut thresholds, input variable values, and the BDT output score. For the other parameters used to scan FPGA cost, given below, the plots of physics performance considering the AUC are given in appendix E (figure 26).

For the FPGA cost study we vary four parameters: \( N_{\text{final tree}} \), the number of final trees after the Tree Merger and Tree Remover steps; \( D \), the maximum depth of a tree; \( N_{\text{bit}} \), the number of
Table 1: Benchmark configuration and the FPGA cost. Four groups of information are given. The top-most group defines the FPGA setup. The second group defines the ML training used for the electron-photon problem. The third group defines the Nanosecond Optimization. The final group gives the results.

| Parameter                          | Value                                      | Comments                                      |
|------------------------------------|--------------------------------------------|-----------------------------------------------|
| **FPGA setup**                     |                                            |                                               |
| Chip family                        | Xilinx Virtex Ultrascale+                  |                                               |
| Chip model                         | xcvu9p-flga2104-2L-e                      |                                               |
| Vivado version                     | 2019.2                                     |                                               |
| Synthesis type                     | C-Synthesis                                |                                               |
| HLS or RTL                         | HLS                                        |                                               |
| HLS interface pragma               | None                                       |                                               |
| Clock speed                        | 320 MHz                                    | Clock period is 3.125 ns                      |
| **ML training configuration**      |                                            |                                               |
| ML training method                 | Boosted decision tree                      | Binary classification                          |
| Boost method                       | Adaptive                                   | AdaBoost with yes/no leaf                     |
| No. of trees used for training     | 100                                        | Maximum depth of 4                            |
| No. of input variables             | 4                                          |                                               |
| **Nanosecond Optimization configuration** |                                            |                                               |
| Bin Engine type                    | Bit Shift Bin Engine (BSBE)                |                                               |
| No. of bits for input variables    | 8 bits for each                           | Same for cut thresholds                       |
| No. of bits for BDT output score   | 8 bits                                    | User configurable                             |
| No. of trees after merging         | 10                                        | TREE MERGER via ordered list                  |
| No. of final trees                 | 10, none removed                          | TREE REMOVER by truncation                    |
| No. of bins                        | 26 132                                     | CUT ERASER not used                           |
| **FPGA cost**                      |                                            |                                               |
| Estimated timing values by HLS co-simulation and resource usage by HLS C synthesis |                                           |                                               |
| Latency                            | 3 clock ticks                             | 9.375 ns, see, also, appendix D.2 (figure 25) |
| Interval                           | 1 clock tick                              | 3.125 ns                                     |
| Look up tables                     | 1903 out of 1 182 240                     | < 0.2% of available                           |
| Flip flops                         | 138 out of 2 364 480                      | < 0.01% of available                          |
| Block RAM                          | 8 out of 4320                             | < 0.2% of available                           |
| Ultra RAM                          | 0 out of 960                              |                                               |
| Digital signal processors          | 0 out of 6840                             |                                               |
| Actual timing values and resource usage by RTL synthesis and implementation |                                           |                                               |
| Latency                            | 3 clock ticks                             | 9.375 ns                                     |
| Interval                           | 1 clock tick                              | 3.125 ns                                     |
| Look up tables                     | 717 out of 1 182 240                      | 0.06% of available                            |
| Flip flops                         | 147 out of 2 364 480                      | < 0.01% of available                          |
| Block RAM                          | 5.5 out of 4320                           | 0.1% of available                             |
| Ultra RAM                          | 0 out of 960                              |                                               |
| Digital signal processors          | 2 out of 6840                             | 0.03% of available                            |
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bits; and $V = N_{\text{var}}$, number of input variables. It is important to note that while $N_{\text{final\ tree}}$ can vary, the number of trees used for the ML training step is kept constant at $T = 100$. Throughout our discussion we compare the results using the two Bin Engines. Additionally, we report dependence on two derived quantities, the number of bins $N_{\text{bin}}$ and the BRAM usage.

**Physics performance**

ROC curves are considered for $N_{\text{bit}} = 3$ and $N_{\text{bit}} = 8$, and are compared to the results using floating point precision. Both BDT and cut-based results are shown in figure 9. The highest performing result uses the BDT using floating point values, as expected. This is followed closely by the BDT using 8-bit values. It is notable to see that the 8-bit BDT outperform the cut-based result using floating point values. Lastly, the 3-bit BDT is the lowest performing result.

![Figure 9: ROC curves for electron (signal) vs. photon (background) classifiers. The pair of BDT curves (curves at the top) outperform the pair of cut-based curves (dots in the middle). The x-axis shows the signal efficiency or TPR. The y-axis shows the background rejection factor, defined as the inverse of background acceptance or 1/FPR, in linear scale, so higher values are better as indicated by the arrow. For both BDT and cut-based, no noticeable difference is seen between floating point precision for input variables compared to 8-bit precision. Both sets outperform the BDT using 3-bit precision (curve at the bottom).](image)

We note that this plot shows $(x, y)$ values of $(\varepsilon_S, 1/\varepsilon_B)$. The latter shows the inverse of background acceptance because, for this physics scenario, small changes in background rejection are important.

Whereas the physics performance degradation in considering $N_{\text{bit}} = 8$ instead of floating point values is negligible, the FPGA cost is greatly reduced. This is discussed next.

The studies on the effect on AUC are given in appendix E.
FPGA cost

The latency is shown as a function of the four parameters in figure 10. There is an approximate linear dependence on the maximum depth $D$ while a flat distribution with fluctuations is observed for the other three parameters. The interval value for all sets of parameters is 1 clock tick as seen in the right plot of figure 11.

![Figure 10: Latency scaling. The left figure shows the dependence on the maximum depth $D$ (upside down triangle with dotted line) and $N_{\text{var}}$ (upright triangle with dashed line). The right figure shows the dependence on $N_{\text{bit}}$ (solid circle) and $N_{\text{final tree}}$ (open circle). The lines connecting the symbols serve as a visual guide and do not represent interpolations. The latter two curves are the same ones in the left plot of figure 11 for BSBE.](image)

The latency results for the Bin Engines are compared for $N_{\text{bit}}$ and $N_{\text{final tree}}$ in figure 11. The left plot compares the latency. The two latency curves that correspond to BSBE were shown previously in figure 10. Over the $x$-axis range, the latency values from LUBE is a factor of 1.5 to 2 higher than those from BSBE. The right plot compares the interval results. The interval curve is constant at 1 for BSBE, as stated previously, and is increased by one clock tick at 2 for LUBE.

The LUT and FF dependence on three parameters—maximum depth $D$, $N_{\text{var}}$, and $N_{\text{bit}}$—is shown in figure 12; the dependence on $N_{\text{final tree}}$ is discussed separately below. Since both the LUT and FF show similar behavior for a given parameter, it helps to discuss them in pairs. The dependence on $D$ is strong because $N_{\text{bin}}$ grows as $2^D$. For this operating point, the dependence on $N_{\text{var}}$ is weak with minor variations because it does not directly impact $N_{\text{bin}}$. The dependence on $N_{\text{bit}}$ increases until around 6, then saturates.

The resource utilization for the Bin Engines are compared for $N_{\text{final tree}}$, which was missing above, and on $N_{\text{bit}}$ in figure 13. The plots show that BSBE uses less LUT and FF by a factor of a few compared to LUBE. Both BSBE and LUBE show no dependence on $N_{\text{final tree}}$ within a factor of two. This last feature is because $N_{\text{final tree}}$ does not directly impact $N_{\text{bin}}$. The dependence on $N_{\text{bin}}$ is discussed next.

We also varied the FPGA chip choice, the clock speed, and Vivado version, all of which was
Figure 11: Latency (left) and interval (right) comparison for the two Bin Engines. For each plot, the dependence is shown for four combinations of $N_{bit}$ (solid symbols) and $N_{final\,tree}$ (open symbols) with LUBE (square) and BSBE (circle). The lines connecting the symbols serve as a visual guide and do not represent interpolations. The benchmark configuration is marked by a star. Three data points of $N_{final\,tree}$ with LUBE (at $x = 33, 50, 74$) are omitted in the plot to zoom-in on the lower range; the latency for those points remain constant at 5, as suggested by the flat line going to the right. The interval for these points remain at 2.

discussed with the firmware verification in section 4.3. We found the latency to be constant around 10 ns after changing the clock speed.

Figure 12: Resource scaling for LUT (blue lines with solid symbols) and FF (gold lines with open symbols) for three parameters: maximum depth (triangle), number of input variables (circle), and number of bits (square). The lines connecting the symbols serve as a visual guide and do not represent interpolations. The benchmark point (table 1) is marked by a star.
Dependence on number of bins and BRAM

The resource utilization (LUT, FF, DSP, and BRAM usage) vs. $N_{\text{bin}}$ is given in figure 14 for the two Bin Engines. First, the top-left plot shows that LUT usage has a slow dependence on $N_{\text{bin}}$. The LUBE result fluctuates by two orders of magnitude because the results of various configurations are shown together, but the usage typically is less than 10%. The fluctuation in LUT usage between the points with similar bin counts is largely due to the differences in the integer bit precision. All points using over 15% of the available LUT used configurations with 10 bits or higher. The BSBE result fluctuates less and grows to about 1% at a million bins. Second, the top-right plot shows that FF usage also shows the same behavior as the LUT usage, although the percentages are an order of magnitude lower. The BSBE result grows to about 0.1% at a million bins. Third, the bottom-left plot shows that DSP usage is zero until around a thousand bins then it starts to grow after around $10^5$. However, even at a million bins the usage is very low at the 0.1% level. Lastly, the bottom-right plot shows that BRAM usage shows a stronger dependence on $N_{\text{bin}}$ and, in contrast to the other three, the same result is seen for LUBE and BSBE. The same dependence and scale on $N_{\text{bin}}$ for BRAM usage for the two Bin Engines make us wonder whether latency is affected in a similar manner.

The latency dependence on $N_{\text{bin}}$ is given in figure 15. The plot on the left shows the logarithmic dependence on $N_{\text{bin}}$ with LUBE having an offset of about 2 to 4 clock ticks higher than BSBE. The fit model is

$$\text{latency in clock ticks} = c \log(N_{\text{bin}})$$

with $c$ around two thirds for LUBE and a third for BSBE.

We check the latency dependence on BRAM with the plot on the right of figure 15. The latency ranges from 0 to 3 clock ticks for no BRAM usage, while it fluctuates between 2 to 5 for $N_{\text{bin}}$ up to a million. This alleviates our potential worry that large BRAM usage blows up the latency value; no
Figure 14: Resource usage vs. number of bins for the two Bin Engines. Plots are shown for LUT (top left), FF (top right), DSP (bottom left), and BRAM (bottom right). URAM usage is not plotted because it is 0 for all configurations. One set of data from LUBE (square) is compared to the other set from BSBE (circle). The percentages are noted in plot given with respect to the total available resource for the benchmark FPGA, whose model number is also stated in the legends. The lines connecting the symbols serve as a visual guide and do not represent interpolations. The benchmark configuration is marked by a star.
such behavior is seen. We also checked the dependence on LUT, FF, and DSP, which show no such pattern.

Figure 15: Latency dependence on \( N_{\text{bin}} \) (left) and BRAM usage (right). On the left, both Bin Engines show a logarithmic dependence. The BSBE shows a slightly lower dependence than LUBE, but there is a gap of about 2 to 4 clock ticks between the methods. On the right, no BRAM usage is marked by the points at \( x = 10^{-1} \); data is separated for the number of input variables. The lines connecting the symbols serve as a visual guide and do not represent interpolations. Two outliers are indicated by the arrows corresponding to the LUBE data. The benchmark configuration is marked by a star.

5.3 Results far from the benchmark

Whereas the previous subsection varied one parameter at a time with respect to the benchmark point, we now consider configurations with many parameters that are far from the benchmark. For this we consider the VBF Higgs problem.

Two BDT configurations are considered. One is an optimized example and the other is a non-optimal example. The latter is given to show the impact on FPGA cost for an extreme case of a non-optimal choice made by the user. The configurations are listed in table 2 and described below.

The optimal configuration uses LUBE with 5 input variables, 8-bits for the cut thresholds and input variable values, and 16-bits for the BDT output score. Cut Eraser is used with a threshold of 5%, which resulted in about \( 4 \cdot 10^4 \) bins. The non-optimal configuration uses BSBE with 7 input variables, 12-bits for the cut thresholds and input variable values, and 16-bits for the BDT output score. Cut Eraser is not used, which resulted in about \( 10^6 \) bins.
Table 2: FPGA cost examples for the VBF Higgs problem. Two operating points are chosen far from the benchmark configuration. An example of the optimized configuration (left column) is compared to an example of the non-optimized configuration (right column). The parameters for the configuration at given at the top group of rows; the FPGA cost is given in the middle group of rows; and the user experience is given at the bottom.

| Quantity                        | Optimized example | Non-opt. example | Ratio |
|---------------------------------|-------------------|------------------|-------|
| Configuration                   |                   |                  |       |
| Bin engine                      | LUBE              | BSBE             | -     |
| No. of input variables          | 5                 | 7                | 1.4   |
| No. of bits for input variable values | 8              | 12               | 1.5   |
| No. of bits for cut threshold values | 8              | 12               | 1.5   |
| No. of bits for BDT output score | 16              | 16               | 1     |
| Max. depth                      | 4                 | 4                | 1     |
| No. of training trees           | 100               | 100              | 1     |
| No. of final trees              | 100               | 50               | 0.5   |
| Cut Eraser, threshold Δ         | Yes, 5%           | -                | -     |
| No. of bins                     | 39 308 ≈ 40k      | 996 710 ≈ 1M     | 25    |
| Tree Remover                    | -                 | -                |       |
| FPGA cost                       |                   |                  |       |
| Latency (clock ticks)           | 5                 | 6                | 1.2   |
| Interval (clock ticks)          | 1                 | 1                | 1     |
| LUT                             | 1.0%              | 1.5%             | 1.5   |
| FF                              | < 0.1%            | < 0.2%           | -     |
| BRAM 18k                        | 2.3%              | 32%              | 14    |
| URAM                            | 0                 | 0                | -     |
| DSP                             | 0                 | < 0.3%           | -     |
| User experience                 |                   |                  |       |
| Time to synthesize\(^8\)        | < 15 minutes      | < 30 minutes     | ≈ 2   |

Physics performance

The VBF Higgs problem contains \( J \) jet pairs per event, for which a corresponding BDT output score is produced for each pair \( \{O_0, \ldots, O_{J-1}\} \). This poses a challenge because the \( J \) copies of the BDT would have to be implemented in firmware for the maximum expected number of jet pairs per event, in order for the processing to occur in parallel. We consider the ideal scenario followed by a more realistic scenario.

First, we consider the ideal scenario in considering all jet pairs in the event using floating point precision. From the list of BDT output scores, we choose the highest value in the list to represent

\(^8\)The setup is a typical commercial PC with the following specifications. Intel Core i9 10\(^{th}\) generation processor with 10 core, 20M cache, and 3.7 GHz to 5.3 GHz. RAM with specification of 64 GB, 2x32 GB, DDR4, 2933 MHz.
the event’s BDT output score, i.e., \( O_{\text{event}} = \max\{O_0, \ldots, O_{J-1}\} \). This ideal scenario with floating point values is used to produce the plot in figure 16. The plot shows that the realistic scenario of limiting the number of \( J \) to three and using bit-integer approximations do not degrade the result. This is discussed below after a discussion of the cut-based results.

Our BDT curves are compared to two cut-based results. The latter uses the ATLAS-inspired cut thresholds from ATLAS documents, the Run-2 thresholds in [64] and the proposed HL-LHC thresholds in [65]. The list of thresholds are given in the appendix (table 9). We implement the cut-based approach using the same samples as described for the BDT training. For the cut-based classifiers, an event passes if any of the jet pairs pass the cut requirements.

The \( y \)-axis shows \( \varepsilon_B \) in a logarithmic scale because, for this physics scenario, one is interested in a very large rejection of the multijet process. A small acceptance of multijet background is needed due to the relatively large inelastic \( pp \) cross section of approximately 80 mb [66], combined with relatively high instantaneous luminosity values reaching \( 2 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1} \) [67]. In comparison, the expected inclusive signal cross sections of VBF Higgs is ten orders of magnitude smaller than the background at approximately 3.8 pb [68]. For typical use cases the most optimal combination is a point with the high value of signal acceptance and the low value of background acceptance, \( \varepsilon_B \) typically less than \( 10^{-4} \). In this representation of \( \varepsilon_S \) vs. \( \log(\varepsilon_B) \), an operating point towards the right-bottom corner of the plot offers the optimal combination.

The BDT results (curves) are compared to the results from the cut-based approach (symbols). Following the above color scheme, the right symbol in the pair in red represents the VBF \( H \rightarrow \text{invisible} \) training for the cut-based approach while the left symbol in blue represents VBF \( H \rightarrow 4b \). As opposed to the cut-based result with a particular operating point due to the set of fixed cut values, the BDT result offers a continuous curve because of the ability to scan the BDT output score.

It is notable that the BDT curves outperform the results from the ATLAS-inspired cut-based selections. For instance, considering the background acceptance level for VBF \( H \rightarrow 4b \) for HL-LHC cut-based (corresponding to signal efficiency of 3.2\%), the corresponding BDT result yields a signal efficiency of 6.6\%, a two-fold increase. This example shows the performance enhancement potential that can be realized in the level-1 trigger.

Second, a more realistic firmware implementation would not consider all \( J \) jet pairs in the event. Evaluating the BDT for each jet pair has the potential to be very resource-intensive on the FPGA, particularly in events with relatively high numbers of jets, as the number of jet pairs is \( J = N_{\text{jet}}(N_{\text{jet}} - 1)/2 \). In order to reduce the value of \( J \) considered on firmware, we considered examining only the three jet pairs with the highest \( m_{jj} \) values. We found that, for the same \( \varepsilon_S \) value, the \( \varepsilon_B \) varied by less than 2\% (figure 16), i.e., \( |1 - \varepsilon_{\text{all}}^{J}/\varepsilon_{\text{top}}^{3}| < 2\% \). We also considered using top six jet pairs, but only find a negligible improvement. The details of this study are given in appendix F. Finally, the performance results for the floating point study is compared to the results from the optimized firmware configuration (table 2); we find negligible differences between the two setup (figure 16).

Therefore, we conclude that a threefold increase in the BDT implementation is sufficient to
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Figure 16: ROC curves for the VBF Higgs (signal) vs. multijet (background) classifier. The BDT is trained for invisible vs. multijet for both curves. The x-axis shows the signal efficiency or TPR; the y-axis shows the background acceptance or FPR. The BDT results (four curves) are compared to the result of the cut-based results (four symbols); see table 9 for the cut values. For the BDT, see the text for the details on the consideration of jet pairs (all J and “top 3”) and the precision of input variable values (floating points and bit integers). For cut-based, the ATLAS-inspired Run-2 operating points [64] are given on the left bottom corner (circles) and the ATLAS-inspired HL-LHC operating points [65] are given on the middle top area (triangles). Better operating direction is indicated by the arrow. The BDT curves outperform all of the cut-based operating points. Comparison is made for the “equal rate” value, i.e., the same value of $\varepsilon_B$ at around $10^{-4}$, corresponding to the HL-LHC 4b cut-based with the BDT result. For this equal rate value, the $\varepsilon_S$ result for the cut-based point is 3.2% while for the BDT it is two-fold larger at 6.3%. A more complete table of value are given in table 3.
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Table 3: Physics performance for VBF Higgs vs. multijet background for various configurations shown in figure 16. Two groups of values are given corresponding to a fixed value of background rate, i.e., a fixed value of $\varepsilon_B$, for the ATLAS-inspired Run-2 and HL-LHC comparisons. Within each group, the cut-based values are obtained by our ATLAS-inspired implementation of the study done by the cited references. Two BDT results are given for varying precision of the input variables and the output score, as well as the number jet pairs considered. For all BDT results shown in this table, the training is done for binary classification of VBF $H_{inv}$ vs. multijet. In the case of VBF $H_{4b}$ the above-mentioned BDT is applied on the signal sample; no BDT is trained for VBF $H_{4b}$ vs. multijet nor is any multiclassification done. We note that the statistical fluctuations caused a minor dip so that the bits result is slightly higher than the float result for the Run-2 VBF $H_{4b}$ efficiency.

| Configuration          | Precision | Signal efficiency $\varepsilon_S$ | Comments                                      |
|------------------------|-----------|-----------------------------------|-----------------------------------------------|
|                        |           | VBF $H_{inv}$ | VBF $H_{4b}$ |                                                                 |
| Run-2 equal background rate |          |               |               | Operating point at FPR value of $\varepsilon_B = 2.5 \cdot 10^{-6}$ |
| Cut-based float        | float     | 0.43%          | 0.44%         | ATLAS-inspired from ref. [64], see text |
| BDT float              |           | 0.66%          | 0.57%         | Trained VBF $H_{inv}$ vs. multijet; evaluate all $J$ pairs |
| BDT bits               |           | 0.64%          | 0.65%         | Trained VBF $H_{inv}$ vs. multijet; eval. top 3 pairs |
| HL-LHC equal background rate |          |               |               | Operating point at FPR value of $\varepsilon_B = 7.9 \cdot 10^{-5}$ |
| Cut-based float        | float     | 2.81%          | 3.20%         | ATLAS-inspired from ref. [65], see text |
| BDT float              |           | 6.16%          | 6.28%         | Trained VBF $H_{inv}$ vs. multijet; evaluate all $J$ pairs |
| BDT bits               |           | 6.16%          | 6.29%         | Trained VBF $H_{inv}$ vs. multijet; eval. top 3 pairs |

achieve the ideal scenario. Furthermore, we assume that the implementation of the max function does not add much to the relative FPGA cost and that the $m_{jj}$ values are provided in sorted order.

FPGA cost

The latency is 5 clock ticks, corresponding to about 19 ns for our setup, which is the optimal configuration. The non-optimal configuration added one clock tick to bring the latency to 6 clock ticks.

The resource utilization is low for LUT, FF, and DSP at a range of 0.2% to 1.5%. No URAM is used. However, a large difference in BRAM usage is seen. The optimized configuration uses 2.3% whereas the non-optimized uses 32%.

Lastly, we note aside the user experience for the time to synthesize. The optimized configuration takes less than 15 minutes and the non-optimized less than 30 minutes for our setup.

The bottom of table 2 summarizes the above findings.

5.4 Comparisons with previous results

The hls4ml group implemented a method for evaluating the BDT on FPGA [28], with the BDT project now called Conifer. This method retains the tree structure and recurses down the binary
splits. An advantage to this method is that it does not face the issue of maintaining a reasonable number of bins, thus it can handle arbitrarily high precision and numbers of variables. Another advantage is the symmetric tree configuration that allows the user to reuse the firmware structure.

A comparison of our result with that of hls4ml/Conifer is difficult to achieve due to structural differences in the architecture of the implementation. Moreover, hls4ml/Conifer considers a five-class problem whereas fwXmachina is designed for binary classification problems. Therefore, we ran the out-of-the-box version of the hls4ml/Conifer [69] on our benchmark configuration. The results of this study are given in appendix G.

6 Conclusions

We presented a novel implementation of machine learning / artificial intelligence method of boosted decision trees in FPGA. The firmware-oriented Nanosecond Optimization stage includes restructuring the tree layout and reconfiguring the BDT parameters. Our design philosophy is to remove clocked operations in favor of combinatoric logic. The resulting design is realized by using a software package called fwXmachina, available at fwx.pitt.edu.

We used fwXmachina to investigate two physics problems for use in the real-time triggers in high energy physics experiments. The first problem is for electron vs. photon separation. The second problem is the selection of the vector boson fusion-produced Higgs boson selection and the rejection of the multijet process. It is a binary classification problem that serves as a challenging case of where ML/AI can make improvements beyond the cut-based approach. These two problems are considered as potential use cases at the LHC.

For our benchmark point of 100 training trees with a maximum depth of 4 using four input variables, we report a latency value of around 10 ns, or 3 clock ticks at 320 MHz. The resource utilization is minimal at less than 0.2% of look up tables and block RAM usage, less than 0.01% of flip flop usage, and no ultra RAM or digital signal processor usage. We studied the dependence of performance on configurable parameters. Far from the benchmark using more variables and more bit precision, we report a latency value of 16 ns with 1 to 2% resource utilization. We find that latency results in nanoseconds do not depend on the clock speed, as it is compensated by clock ticks.

By considering the physics performance and FPGA cost at the same time, the user of fwXmachina has the ability to consider the trade-offs between the two for their own use case.

fwXmachina gives users the versatility to work within various experimental constraints. In particular, this flexibility may be beneficial for trigger systems for the HL-LHC operation of the ATLAS and CMS experiments, or any such systems, that are under strict timing requirements.
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A List of terminology used in the paper

This paper uses abbreviations and technical terminology from many different fields of study. They are listed in table 4. The notation used for Nanosecond Optimization in section 3 is given in table 5. The definitions of the technical terms for firmware design in section 4 are given in table 6. The parameters used in the performance and FPGA cost evaluation in section 5 are described in table 7.

B Details of the ML training

The details of the samples and the ML training are given for the two physics problems that are considered in this paper.

B.1 Electron vs. photon

Electron and photon samples were obtained from ref. [56] described elsewhere [70, 71].

A sample of 400k positrons ($e^+$) is considered signal and 400k photons ($\gamma$) is considered as background. The detector simulation is done with GEANT4 [72], a first principles simulation that describes the interaction of each particle with the detector, to implement a $480 \text{ mm}^3$ section of a calorimeter [53] that is inspired by the ATLAS liquid argon calorimeter [73]. The calorimeter has three alternating layers of lead absorber material and active liquid argon. The variables derived from measurements in the three layers are denoted with subscripts 0, 1, and 2 in increasing distance from the collision axis.

We consider a total of eight input variables that capture the pattern of energy deposits in the calorimeter: $E_0$, $E_1$, $f_0$, $f_1$, $s_d$, $\sigma_{s_d}$, $l_d$, and $l_{d2}$. These variables are listed in table 8 [53, 74]. A subset of four of the following variables are used for the benchmark configuration: $E_0$, $f_1$, $s_d$, and $\sigma_{s_d}$. The distributions are shown in figure 18.
Table 4: List of terms used in this paper in five categories. BRAM, DSP, FF, LUT, URAM, latency, and interval are described in table 6. The latter two are illustrated in figure 17.

| Terms | Description |
|-------|-------------|
| **Physics** | |
| 2HDM | Two-Higgs doublet model, a BSM theory that extends the Higgs boson sector |
| BSM | Beyond the Standard Model, i.e., hypotheses that extend the Standard Model |
| $H$ | Higgs boson |
| HEP | High energy physics |
| HL-LHC | High Luminosity LHC, the upgrade of the LHC to start around 2026 |
| LHC | Large Hadron Collider |
| Multijet | Physics process wherein multiple “jets” are produced from the collision |
| VBF | Vector boson fusion interaction process from the collision |
| **Machine learning** | |
| AdaBoost | Adaptive boost method for BDT |
| BDT | Boosted decision tree, the type of ML used in this paper |
| GradBoost | Gradient boost method for BDT |
| ROC | Receiver operating characteristics |
| **Statistics** | |
| TPR | True positive rate, i.e., signal efficiency ($\varepsilon_S$), corresponds to correct signal inference |
| FNR | False negative rate, i.e., signal veto ($1 - \varepsilon_S$); also called type II error ($\beta$) |
| TNR | True negative rate, i.e., background veto ($1 - \varepsilon_B$) |
| FPR | False positive rate, i.e., background acceptance ($\varepsilon_B$); also called type I error ($\alpha$) |
| $1/FPR$ | Inverse false positive rate, i.e., background rejection factor ($1/\varepsilon_B$) |
| **Engineering** | |
| ASIC | Application specific integrated circuit |
| ASR | Arithmetic shift right |
| Bitstream | A file that contains the programming information for an FPGA |
| Bus tap | Taps a subset of values stored in the input bus and fans them out |
| FPGA | Field programmable gate array |
| HDL | Hardware description language |
| HLS | High Level Synthesis |
| ILA | Internal Logic Analyzer |
| IP | Intellectual Property core |
| LSB | Least significant bit |
| RTL | Register transfer level |
| VHDL | Very High Speed Integrated Circuit (VHSIC) Hardware Description Language |
| **This paper** | |
| BSBE | Bit Shift Bin Engine |
| FPGA cost | Timing (latency, interval) and resource usage (LUT, FF, BRAM, URAM, DSP) |
| LUBE | Look Up Bin Engine |
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Table 5: Notation used for Nanosecond Optimization. When appropriate the lowercase variables represent the index of the corresponding uppercase versions in this table, e.g., \( t \) as a tree index for a value from 0 to \( T - 1 \).

| Symbol | Description |
|--------|-------------|
| \( \tau, \bar{\tau} = \phi \) | Single tree, Ordered list of trees = Forest |
| \( x, \bar{x} \) | Single input variable, Ordered list of variables |
| \( D \) | Depth of the tree |
| \( V = N_{\text{var}} \) | Number of input variables |
| \( T = N_{\text{tree}} \) | Number of trees |
| \( B = N_{\text{bin}} \) | Number of bins |
| \( N = N_{\text{bit}} \) | Number of bits for input variables |
| \( L \) | Number of binary layers |
| \( O \) | BDT output score |
| \( W_t \) | Boost weight for tree \( t \) |
| \( w_t \) | Normalized boost weight, i.e., \( w_t = W_t / \sum_{t'} W_{t'} \) |

![Figure 17: Illustration of latency and interval. The top example shows that successive inputs can be sent after each clock tick with each event taking five ticks, so six events are processed in ten ticks. The bottom example shows that successive inputs can be sent every third tick with each event taking three ticks, so three events are processed in the same period. The two examples illustrate the importance of interval.](image-url)
Table 6: List of technical terms for FPGA cost and firmware test bench. Figure 17 illustrates the timing.

| Term                        | Description                                                                                                                                 |
|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| Chip information            | We use Xilinx Virtex Ultrascale+ VU9P. The Ultrascale+ series is among Xilinx’s families released starting in 2016 and manufactured with a 16 nm process. |
| High Level Synthesis (HLS)  | Software tool provided by Xilinx for converting C (or C++) code into a register transfer level (RTL) implementation that can be synthesized to run on an FPGA. The BDT implementation is largely written in HLS. |
| Pragma                      | Special commands that can be placed in your C code to give the HLS compiler directives regarding the desired hardware implementation. For example, pragma can “unroll” a loop so that its results can be computed in parallel, as opposed to in series. |
| Clock speed                 | Target clock frequency. The maximum clock speed that an FPGA design can run at depends on the design itself. For example, every logic gate has a small delay and gates strung together begin to stack up. This becomes a constraint on the maximum clock speed that the design can handle as the results of the logic need to be stored or passed to another part of the design. The synthesizer attempts to optimize the maximum clock to be higher than the target clock frequency by a certain margin. |
| Clock ticks                 | For synchronous circuits, a “clock” is required to synchronize portions of the circuit. The clock is an input that periodically goes from logical high to logical low. A “clock tick” occurs when the clock moves from low to high. |
| Latency                     | Time required for an algorithm to take an input and produce a valid output.                                                                |
| Interval                    | Time required between two successive inputs to the algorithm.                                                                               |
| Resource utilization        | FPGA chips have various different circuit elements that can be used in a design, e.g., BRAM, LUT, and FF. Resource utilization is an inclusive term that refers to these various circuit elements. It can be reported in percentage of the available element or as the total number of each element. |
| Look up table (LUT)         | Type of asynchronous memory. LUT has the benefit of quick memory accesses that do not depend on a clock, but they come at the expense of consuming more area on the FPGA die. FPGA chips have many LUT built-in for utilization in a design. |
| Flip flop (FF)              | One of the basic elements of data storage in electrical circuits. A flip flop stores one bit of information. Compared to other memory technologies, flip flops have a higher access speed, but the circuit is very large leading to poor memory density. |
| Block RAM (BRAM)            | Block of random access memory (RAM), which is a synchronous memory element. The RAM requires a clock to put data in or to get it out. Because memory can only be accessed on a clock edge, the data is not available immediately. RAM trades access speed for increased memory density. |
| Ultra RAM (URAM)            | Ultrascale+ has two types of RAM: URAM, and BRAM. URAM is a block of memory similar to BRAM, but are much larger than BRAM. The larger size making them inefficient for smaller amounts of data. |
| Digital Signal Processor (DSP) | Many applications in the field of DSP require the use of a multiply and accumulate operation. As a result, multiply and accumulate circuits are often referred to as DSP. |
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Table 7: Parameters considered when studying the FPGA cost. Some of the terms in this list correspond to terms defined in table 5.

| Quantity | Type       | Description                                                                 |
|----------|------------|-----------------------------------------------------------------------------|
| AUC      | Performance metric | Area under the ROC curve of background veto vs. signal acceptance, i.e., \(1 - \varepsilon_B\) vs. \(\varepsilon_S\). This is similar to the curves in figure 16, but with the y-axis being the complement. The higher AUC corresponds to a better performing BDT. |
| \(N_{\text{var}} = V\) | Parameter | Number of input variables for the ML method.                               |
| \(N_{\text{bit}} = N\) | Parameter | Number of bits used for cut threshold values \(N_{\text{bit,cut}}\), input variable values \(N_{\text{bit,var}}\), and BDT output score \(N_{\text{bit,score}}\). Although the number of bits can set separately for the three types of values, the studies presented in this paper set them all to the same value, i.e., \(N_{\text{bit}} = N_{\text{bit,cut}} = N_{\text{bit,var}} = N_{\text{bit,score}}\). |
| Max. depth = \(D\) | Parameter | When training the BDT, this is the maximum depth for each tree. For a maximum depth \(D\), the most cuts a tree can have is \(2^D - 1\). Training will stop when either the maximum depth is reached, or when a small enough fraction of events are in a given node. That fraction can generally be set by the user, e.g., in TMVA it is called \(\text{MinNodeSize}\) and has a default value of 5%. |
| \(N_{\text{tree}} = T\) | Parameter | Number of trees used for the BDT training stage. Some of these may be removed by \text{Ttree Remover}. |
| \(N_{\text{final tree}}\) | Derived | Number of final trees after \text{Ttree Merger} and \text{Ttree Remover}. |
| \(N_{\text{bin}} = B\) | Derived | Number of bins evaluated in the \text{fwXmachine} firmware implementation of the BDT. Tends to scale with the product of the \(N_{\text{var}}\) and \(N_{\text{bit}}\). |

Table 8: List of input variables for the classification of electron vs. photon. Four input variables are used for the benchmark BDT. Up to 8 input variables are used to study the scaling of firmware performance later in section 4. The variables are defined in ref. [53, 74].

| Variable | Description | Used as input variable for benchmark BDT | Used to study firmware cost scaling |
|----------|-------------|------------------------------------------|------------------------------------|
| \(E_0\)  | Energy deposited in the 0\textsuperscript{th} layer | yes | BDT with \(N_{\text{var}} \geq 1\) |
| \(E_1\)  | Energy deposited in the 1\textsuperscript{st} layer | - | BDT with \(N_{\text{var}} \geq 7\) |
| \(E_2\)  | Energy deposited in the 2\textsuperscript{nd} layer | - | - |
| \(E_{\text{tot}}\) | Energy deposited in all three layers | - | - |
| \(l_d\)  | Depth-weighted energy, \(\sum_{i=0}^{2} i \cdot E_i\) | - | BDT with \(N_{\text{var}} \geq 8\) |
| \(l_{d2}\) | Squared-depth-weighted energy, \(\sum_{i=0}^{2} i^2 \cdot E_i\) | - | BDT with \(N_{\text{var}} \geq 6\) |
| \(f_0\)  | Ratio of \(E_0\) and \(E_{\text{tot}}\) | - | BDT with \(N_{\text{var}} \geq 5\) |
| \(f_1\)  | Ratio of \(E_1\) and \(E_{\text{tot}}\) | yes | BDT with \(N_{\text{var}} \geq 3\) |
| \(s_d\)  | Shower depth, \((E_1 + 2 \cdot E_2)/E_{\text{tot}}\) | yes | BDT with \(N_{\text{var}} \geq 4\) |
| \(\sigma_{sd}\) | Shower depth width in standard deviations | yes | BDT with \(N_{\text{var}} \geq 2\) |
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Figure 18: Input variable distributions for the benchmark BDT to classify electron vs. photon.

B.2 VBF Higgs bosons vs. multijet process

We generated 10 million events for each of the samples below [75] with MadGraph5_aMC version 2.7.3 [76]. The computation is done at leading order in the strong coupling constant $\alpha_s$ with a minimum jet $p_T$ threshold of 15 GeV and minimum $\Delta R$ between the two jets of 0.4. The samples are created by event generation that captures the theoretical process followed by smearing that accounts for the experimental effects.

For the signal sample, two subsamples for VBF-produced Higgs are generated. Each subsample considers a different decay mode of the Higgs boson. Both subsamples were generated with MadGraph5_aMC version 2.7.3 and showered using Pythia8 [77]. The VBF $H \rightarrow invisible$ subsample simulates the Higgs boson decays to the neutrino final state, which ends up with two visible “VBF jets” and are typically not accompanied by additional jets. The VBF $\rightarrow 4b$ subsample simulates the Higgs boson decays involving a beyond-the-Standard-Model (BSM) two-Higgs doublet model (2HDM) with an additional spinless particle $a$ [78–81], which also produces two VBF jets from the production and, in this case, four $b$-quark jets from the decay. The decay with six total jets is an interesting test case to ensure that the non-VBF jets are misidentified as VBF jets whose quantities are inputs to the BDT. After event generation, smearing is done using Delphes version 3.4.2 [82, 83]. The Delphes model accounts for detector resolution and other experimental effects, such as pileup. In summary, the two VBF signal subsamples are
• “VBF $H \rightarrow invisible$” for the Higgs boson decay $H \rightarrow ZZ^{(*)} \rightarrow \nu\bar{\nu}\nu\bar{\nu}$ and
• “VBF $H \rightarrow 4b$” for the Higgs boson decay $H \rightarrow aa \rightarrow b\bar{b}b\bar{b}$, where $a$ is a hypothetical spinless particle with mass $m_a = 50$ GeV from a 2HDM model.

For the signal sample, we validate our setup by reproducing the VBF $H \rightarrow invisible$ analysis published by the ATLAS Collaboration [57] using our samples. We find the same signal efficiency value 0.7% as found by ATLAS for this validation.

For the background sample, minimum bias pileup events are generated using the minimum bias tune ATLAS AZ corresponding to Pythia pp tune 17 [84]. Showering uses the Delphes CMS with pileup card described in the Delphes documentation.

For both the signal and the background samples, a minimum bias pileup with mean pileup $\langle \mu \rangle = 50$ is specified. Jets were reconstructed after particle level smearing using the anti-$k_T$ algorithm with a radius parameter of $R = 0.4$ and a minimum jet threshold of $p_T = 20$ GeV [11]. Pileup jets are identified and removed using the CMS pileup jet removal scheme described elsewhere [85].

The classifier is trained on variables associated with dijet pairs, with the goal to discriminate VBF jet pairs from background jet pairs. For the signal, the training sample was composed of the highest $m_{jj}$ pair from each VBF $H \rightarrow invisible$ event; this is assumed to be the correctly identified VBF jet pair in those events. For the background, every possible jet pairing is trained on, as none of these are “VBF jets.” For example, if a background event has three jets ($j_1, j_2,$ and $j_3$), then the three combinations $j_1j_2, j_1j_3,$ and $j_2j_3$ are all considered as background pairs in the training.

For each dijet pair, $j_1$ is the higher $p_T$ jet and $j_2$ is the other jet. Cylindrical $\eta$-$\phi$ coordinates are used with pseudorapidity $\eta$ and azimuthal angle $\phi$. The ranges of the angles are $-4.9 < \eta < 4.9$ and $-\pi < \phi < \pi$, respectively. These define the input variables listed in table 9. The distributions are shown in figure 19.

The BDT was trained with 100 trees each with a maximum depth of 4. Given the target operating point at very low background acceptance, the background training tree was weighted by a factor of $10^5$ to strongly encourage the classifier to minimize erroneous background acceptance. The signal and background events were evenly split between training and testing sets. The BDT setup uses the AdaBoost metric in TMVA with node purity as the output score.

C Details of the Nanosecond Optimization

Details of the binning algorithms as well as for the four latter steps of the Nanosecond Optimization are described.

C.1 Binning algorithms

Two algorithms are described. The first is binning by bit shift. The second is binning by look up. These algorithms are implemented in the BSBE and LUBE Bin Engine firmware, respectively.
Figure 19: Distributions of a few characteristic variables for VBF Higgs and multijet processes. The variables are defined in table 9.
Table 9: List of input variables for the classification of the VBF Higgs boson vs. multijet process. Also given are the ATLAS-inspired cut-based offline thresholds for Run 2 [64] and HL-LHC [65]. For Run-2, differences arise with respect to the document when the $m_{jj}$ threshold is quoted as 1100 GeV for L1 MJJ-500-NFF; we use the > 99% offline efficiency point, which is achieved around $m_{jj} > 1300$ GeV. For others the offline thresholds are used. For HL-LHC, the single-level scheme values are quoted. The performance of the cut-based approach using these values is compared to the performance to the BDT result in figure 16. The non-optimized (non-opt) configuration includes the five variables from the optimized configuration.

| Input variable | Description          | ATLAS Run-2 offline cut [64], see caption | ATLAS HL-LHC offline cut [65], see caption | Used in BDT |
|----------------|----------------------|------------------------------------------|-------------------------------------------|-------------|
| $p_{T1}$       | Leading jet $p_T$    | > 90 GeV                                 | > 75 GeV                                  | -           |
| $p_{T2}$       | Subleading jet $p_T$ | > 80 GeV                                 | > 75 GeV                                  | Optimized   |
| $p_{T12}$      | Sum $p_{T1} + p_{T2}$| -                                       | -                                         | Optimized   |
| $|\eta_1|$       | Leading jet $\eta$  | < 3.2                                    | -                                         | -           |
| $|\eta_2|$       | Subleading jet $\eta$| < 4.9                                    | -                                         | -           |
| $|\Pi \eta|$     | Product $\eta_1 \cdot \eta_2$ | -                                     | -                                         | Optimized   |
| $|\Delta \eta|$  | Separation in $|\eta_2 - \eta_1|$ | > 4.0                                   | > 2.5                                     | -           |
| $|\Delta \phi|$  | Separation in $|\phi_2 - \phi_1|$   | < 2.0                                    | < 2.5                                     | non-opt     |
| $|\Delta R|$     | $\sqrt{(\Delta \eta)^2 + (\Delta \phi)^2}$ | -                                     | -                                         | non-opt     |
| $m_{jj}$       | Dijet invariant mass | > 1300 GeV                               | -                                         | Optimized   |
| $p_{Tjj}$      | Dijet $p_T$          | -                                       | -                                         | Optimized   |

Binning by bit shift achieves fast binning by taking advantage of the binary representation of numbers in hardware. For example, figure 20 demonstrates this strategy for one variable $x$ in bit-shift layers. The goal of this process is to best approximate the floating point bin boundaries from training shown at the bottom of figure 20. In the bit shift approach, cuts are added by splitting the bins from the previous layer in half whenever there is a high density of floating point cuts. When evaluated in each layer, the input value can be said to reside within a bin of a certain index. Evaluating the bin index for an event in a given layer can be accomplished by integer-dividing by the number of bins in that layer. An integer division is a standard division operation where the answer is rounded down to the nearest integer. Since each grid layer is generated by a binary split of the previous, the number of bins in every grid layer is equal to a power of two. An integer division by a power of two is equivalent to a bit shift operation by that power. Now that the bin index in each grid layer has been determined, a deterministic combination of these bin indices is used to determine the final bin index.

To begin setting up the grid layers, the first layer divides $x_a$ into two ranges 0–15 and 16–31, as seen in figure 20. Likewise, the second layer subdivides the two ranges into two further bins. The divisions start to get interesting with the third layer, where the bins are subdivided except for the first bin. That is because the bin thresholds from training do not contain a division in the first bin of layer $\ell = 3$. This process continues until $\ell = L - 1$, depending on the user’s specifications. The arrows are meant to indicate that the binary boundaries will not be as exact as the boundaries from floating
point precision from the training. We call the process of splitting each layer as “gridification.” Since we repeat the process for each layer, we call it recursive gridification, but we note that it is recursive only on the software side of **fwXmachina**, not the firmware side. In the firmware representation the method employs combinatoric logic without recursion. The gridification process creates a binary tree for each variable with cuts defined by powers of two.

Binning by look up uses a set of thresholds that were introduced and discussed in the text. The benefit of this approach, compared to by bit shift discussed above, is that it is less focused on the numbers of bits used for the input variables and the cut thresholds. This gives more flexibility for the user at the cost of latency.

### C.2 Score Finder

Once the bin boundaries are determined **Score Finder** associates an output score to it. The output score for an event is the combined score using a set of weights \( W_t \) for tree \( t \), which, e.g., for the AdaBoost boost method, is

\[
O = \frac{O_0 W_0 + O_1 W_1 + \cdots + O_{T-1} W_{T-1}}{W_0 + W_1 + \cdots + W_{T-1}} = \sum_{i=0}^{T-1} O_t w_t, \tag{2}
\]

where \( w_t = W_t / \sum_{t'=0}^{T-1} W_t \) is the normalized boost weight for tree \( t \).\(^9\)

For each bin in tree \( t \), the score \( O_t \) and weight \( W_t \) is associated to that bin. The next step is to normalize these scores.

### C.3 Score Normalizer

The **Score Finder** defined the boost-weight normalization in eq. (2). Now we discuss three aspects of normalizing the output scores by **Score Normalizer**. First, we revisit the aspect of using less precision than floating point. Second, we discuss choice of a score range because it plays an important role in the tree remover step discussed in the next subsection. Third, we describe the piece-wise approximation of a continuous function.

#### Conversion of floating point to bit integer

The initial values of the cut thresholds and the output scores from the ML training are floating point precision. But in the FPGA it is beneficial to represent data as \( N \)-bit integers, so convert the data to \( N \)-bit integers according to the user’s specification. The values are between 0 and \( 2^N - 1 \) for \( N \)-bit integers, e.g., 0 to 1023 for 10-bit integers.

---

\(^9\)The combined score formula for some of the other boost methods, such as GradBoost, uses different metrics. The treatment of the combined score for GradBoost is discussed in appendix C.3 (table 10 and figure 21).
Figure 20: Example of the binning by bit shift algorithm for one variable $x_a$. At the top row of figures, the result of the training step are three bins in the conventional bin boundaries (left-most). If the bin boundaries occur in multiples of a power of two, then bit shifting can be employed to reduce the latency to find the bin index of an event. In our example, we choose $2^2 = 4$ as the fixed bin width and arrive at six primed bins (middle). However, the binary gridification approach potentially incurs a large resource usage in cases where a large amount variation occurs in a small area. In that case, we can employ a “recursive” approach (right-most). We put quotation marks because the implementation is not recursive since it can be done by combinatoric logic as shown in figure 7. At the bottom group of figures, the “recursive” process is expanded upon in 5 layers. The 5th layer is compared to the floating point boundaries from training.
The conversion of cut threshold values from floating point $c_{\text{float}}$ to bit integers $c_{\text{int}}$ is straightforward using a linear function $f$:

$$c_{\text{int}} = f(c_{\text{float}}) = \left\lfloor \frac{c_{\text{float}} - c_{\min}}{c_{\max} - c_{\min}} \cdot (2^N - 1) \right\rfloor,$$  \hspace{1cm} (3)

where the “floor” operator is used in the final step. The difference between the maximum and minimum values in the denominator represents the range of possible values. By default for cut thresholds, this is the range of the training data, though this range can be set by the user. The flexibility allows the user to ensure that the incoming data matches the convention used in the classifier.

The conversion of output scores from floating point $v_{\text{float}}$ to bit integers $v_{\text{int}}$ needs to be treated with more care so that the operation respects addition, i.e., whether $f(v_1 + v_2) = f(v_1) + f(v_2)$ holds. It does not in the presence of a normalized boost weight $w$, so the conversion is modified as follows with transformation $g$. We take $v_{\min} = 0$ and $v_{\max} = 1$.

$$v_{\text{int}} = g(v_{\text{float}}) = \left\lfloor w \cdot v_{\text{float}} \cdot (2^N - 1) \right\rfloor,$$  \hspace{1cm} (4)

For output scores ranging from $-1$ to 1, this function provides an integer value ranging from $-(2^N + 1)$ to $2^N - 1$. For output scores ranging from 0 to 1, this provides an integer value ranging from 0 to $2^N - 1$.

Let us check the addition for the purity metric with $O = S/(S + B)$ ranging from 0 to 1. For example, two sets of purity values $O_{\text{float},1} = \{0, 0.3\}$ and $O_{\text{float},2} = \{0.1, 0.7\}$ are converted into 10-bits with normalized boost weights $w_1 = 0.2$ and $w_2 = 0.8$. Then, using eq. (4), $O_{\text{int},1} = \{\{0.2 \cdot 0.1023\}, \{0.2 \cdot 0.3 \cdot 1023\}\} = \{0, 61\}$ and $O_{\text{int},2} = \{\{0.8 \cdot 0.1 \cdot 1023\}, \{0.8 \cdot 0.7 \cdot 1023\}\} = \{81, 572\}$. The sum of the bit integers are $O_{\text{int},1} + O_{\text{int},2} = \{81, 633\}$. To compare, the weighted sum of the floating point values are $O_{\text{float},12} = \{0.2 \cdot 0.1 + 0.8 \cdot 0.1, 0.2 \cdot 0.3 + 0.8 \cdot 0.7\} = \{0.08, 0.62\}$. The conversion of the sum, with $w = 1$ since there is no weight, is $g(O_{\text{float},12}) = \{\{0.16 \cdot 1023\}, \{0.62 \cdot 1023\}\} = \{81, 634\}$, which is almost, but not exactly, what we obtained before.

This example illustrates an important aspect of the function $g$ under addition. Because of the floor function, the difference between the sum of the conversion $g(w_1 \cdot v_1) + g(w_2 \cdot v_2)$ and the conversion of the sum $g(w_1 \cdot v_1 + w_2 \cdot v_2)$ can give rise to a difference of up to one bit due to rounding. However, the ability to maintain addition is an important aspect of speeding up the firmware. This is because `fwidthmachina` does all of the conversions to provide the set of $\{g(w_i \cdot v_i)\}$ values to the FPGA. The FPGA simply has to add the scores without needing to apply any transformations.

**Output score range**

ML classifiers often report an output score, generally ranging from either 0 to 1 or from $-1$ to 1, with the lower value indicating a background-like event and the higher indicating a signal-like event.
Here we introduce three possible metrics for AdaBoost and one for GradBoost that may be chosen to optimize classifier and firmware performance.

For AdaBoost, we first consider the purity output score. Each tree provides a response value that ranges from 0 to 1 based on the ratio $S/(S + B)$ in the terminal node of a tree, where $S$ and $B$ represent the number of signal and background events, respectively. The response is converted to $N$-bit integers by eq. (4) to yield a value in the range from 0 to $2^N - 1$. Second, we consider the “adjusted purity.” We define it as $(S - B)/(S + B)$, which is just a twice the purity shifted by unity, i.e., $2 \cdot S/(S + B) - 1$. The response ranges from $-1$ to 1, which is converted to $-2^N + 1$ to $2^N - 1$ after the bit integer transformation as was done for the purity response. This adjusted value can be advantageous as it assigns indeterminate events a score near zero, which is beneficial for Tree Remover described in appendix C.4. Lastly, we consider the “yes/no leaf.” The response is determined for a terminal node under the following conditions. If $S/(S + B) \geq \gamma$, then the terminal node is assigned a score of 1. Otherwise, the terminal node is assigned a score of $-1$. The value of $\gamma$ is a user-configurable parameter; in this paper, it is set to 0.5 when yes/no leaf is used. For all three boosting algorithms mentioned above, the combined output score is the weighted sum of the response values from each of the trees. The weights are the normalized boost weights, i.e., $O_{\text{combined}} = \sum_t O_t \cdot w_t$, where $O_t$ is the response value for tree $t$. Because the combination process is a simple sum, each component of the sum is pre-computed to be hard-coded into firmware. The firmware then executes the sum without having to multiply or convert.

For GradBoost, an unbounded response value is provided for each terminal node. Rather than taking the weighted average of the scores as is done for AdaBoost, the combined output score is defined by $\tanh(\sum_t O_t)$. Since $\tanh(x_1 + x_2) \neq \tanh(x_1) + \tanh(x_2)$, this operation cannot be pre-computed as is done for AdaBoost. Therefore, we optimize it with a piece-wise approximation in firmware, which is discussed next.

A summary of the above metrics is given in table 10.

Table 10: BDT score definitions for various output boost metrics. The quantity $S$ ($B$) represents the number of signal (background) events in the terminal node. Adjusted purity is defined in this paper. One version of yes/no is given in this table; in principle, the threshold for the comparison can be changed. The range for yes/no is continuous because of weighted score sums in eq. (4). The scores from the trees in the forest are combined by using the normalized boost weight $w_t$.  

| Algorithm      | Response value per tree | Combined score            | Combined score range     |
|----------------|-------------------------|---------------------------|--------------------------|
| Purity         | $O_t = S/(S + B)$       | $O_{\text{purity}} = \sum_t O_t \cdot w_t$ | $0 \leq O_{\text{purity}} \leq 1$ |
| Adjusted purity| $O_t = 2 \cdot S/(S + B) - 1$ | $O'_{\text{purity}} = \sum_t O_t \cdot w_t$ | $-1 \leq O'_{\text{purity}} \leq 1$ |
| Yes/no leaf    | $O_t = 1$ if $S>B$, else $-1$ | $O_{\text{yes/no}} = \sum_t O_t \cdot w_t$ | $-1 \leq O_{\text{yes/no}} \leq 1$ |
| Gradient       | $O_t$, provided by the algo. | $O_{\text{grad}} = \tanh(\sum_t O_t)$ | $-1 \leq O_{\text{grad}} \leq 1$ |
Piece-wise approximation of tanh

The tanh function can be approximated in a piece-wise manner [86] as shown in figure 21. Our piece-wise implementation is to divide the x-axis range in powers of two, so that binning can be done by bit shifting. The plots show that this seven-piece piece-wise function approximates the exact value to 5% over the range. The piece-wise function becomes a look up table in the FPGA.

![Figure 21: Piece-wise approximation. The tanh function is described by a set of linear functions for the score conversion in the gradient boost method. The top plot shows the approximation in dotted red line superimposed on the solid black line. The bottom plot shows the percent error, which is accurate to 5% over the range. The vertical lines denote the bin boundaries, which are in powers of two so that binning can be achieved by bit shifting.](image)

C.4 Tree Remover

Thus far in Nanosecond Optimization, we have merged trees and converted the floating point values to bit integers. Now we take a closer look at each merged tree in the forest to remove the ones that have no impact on physics performance.

At this stage the tree remover receives the normalized score in each bin of a flattened tree $t$, i.e., $O_t \cdot w_t$. Since the sum of the normalized scores represents the final output score—with the exception of gradient boost that needs the tanh applied at the end—it is more convenient to think of
the product

\[ \alpha_t = O_t \cdot w_t \]  

so that \( O_{\text{combined}} = \sum_t \alpha_t \).

The key point is that \( \alpha_t \) is small whenever \( w_t \) is small independent of the value for \( O_t \). This is because \( O_t \) is bounded to be between 0 and 1 or \(-1\) to 1. So for trees with low relative boost weights \( w_t \), any floating point value \( \alpha_t \) is also very small. After the bit integer conversion step, such an \( \alpha_t \) will be rounded down to a bit integer output of 0. Since it can be known in advance that some trees will have only \( \alpha_t \) values of 0, the tree will have no impact on the final output score so we remove the tree from the forest.

The choice of BDT boost metric is important because 0 has a special meaning in the purity scheme, and tree remover does not work there. The 0 values represent background-like events, so removing them would influence the event distributions. The adjusted purity is developed to counter this effect so that background-like events are near \(-1\) and signal-like events are near 1. This \(-1\) to 1 range also holds for yes/no as well as gradient boosting.

In the latter three schemes the 0 score represents the perfect ambiguity of signal or background. The practical way of thinking about this is to see that the normalized weights \( w_t \) range from 0 to 1. The weights near 0 are the least important and those near 1 is the most important.

Removing entire trees saves the FPGA clock ticks associated with binning for these trees and pointlessly adding 0 in the final summation. We have developed three methods for tree remover that are listed in Table 11.

Table 11: Tree Remover (TR) methods for Nanosecond Optimization. The default choice used in this paper is the first option.

| Tree Remover Method       | Description                                                                 |
|---------------------------|-----------------------------------------------------------------------------|
| TR by Zero Suppression    | All possible output scores associated with each tree are considered. If every score is 0 in a tree, then that tree is removed. |
| TR by Bin Threshold       | All possible scores associated with each tree are considered. If a user-defined fraction \( f_{\text{score}} \) of them have a less than a user-defined impact \( f_{\text{impact}} \), then the tree is removed. For example, if \( f_{\text{score}} = 90\% \) of the bins contributes to \( f_{\text{impact}} < 3\% \) of the output score, then the tree is removed. |
| TR by Boost Threshold     | If the boost-weight falls below a user-defined threshold fraction \( f_{\text{thr}} \) of the average boost weight \( f_{\text{avg}} \), the tree is removed. For example, if the average of 100 trees’ boost weights is \( f_{\text{avg}} = 0.1 \), the user-defined threshold fraction is set to \( f_{\text{thr}} = 0.02 \), then the tree with a boost weight of 0.0001 is removed since it is less than \( f_{\text{avg}} \cdot f_{\text{thr}} \). |
C.5 Cut Eraser

The Cut Eraser removes bin boundaries if they do not affect physics performance under the user specified threshold.

When trees are merged, we may be left with what we can call “useless” cuts: cuts which have an impact in each tree independently, but, upon merging, are rendered redundant. The simplest case of this would be a cut location shared by two or more trees. Moreover, there are cases in which cuts are not redundant, but may still be irrelevant.

For a cut to be a candidate for removal, we must first show that removing it has a negligible impact on the output of the classifier. For a flattened tree, this means that there is no, or minimal, change in outcome between an event falling in the bin on the “left” or the “right” of that cut. Therefore, to determine which cuts can be removed, we scan across every cut, at each one comparing the value held by every bin bordering the cut on the “left” to the value held by its counterpart on the “right.” If for every one of these comparisons across the cut, the difference $\Delta p$ between the bin on the left and right is very small, then the cut is removed. This process is performed for each variable. Two examples are considered.

The first example is given for a two-variable case in figure 22. In this graphic the difference between the bins in $x_1$ for one bin boundary is $\leq 0.05$, which is the example threshold used, so that boundary is removed after the cut eraser step.

The second example is given for a one-variable case for the method of binary bit shift binning in figure 23. The figure continues the example of figure 20, which uses the BSBE approach. We have to be more careful with BSBE because it uses all of the cut thresholds after conversion to bit integers. Therefore, the cut eraser cannot simply scan left to right as in the first example since it may inadvertently remove a cut in the middle. So rather than scanning for bin boundaries remove, we go from the deepest bit levels to the first. In our figure, the algorithm starts at level-5 to remove the boundary between bin 01110 and 01111 and level-4 to remove the boundary between bin 110 and 111. In the second iteration, the algorithm removes the boundary between bin 0110 and 0111 in layer-4. All of the bins that are merged are marked with black background. Finally, the third diagram is the result of the cut eraser.

D Details of the firmware design

D.1 Cut-based implementation

The cut-based classification is a pass-fail algorithm that compares each variable in a set to a set of thresholds, e.g., $x_1 < c_1$ and $c_2 < x_2 < c_2'$ for variables $x_i$ and threshold values $c_i$. Conceptually this corresponds to the simplest BDT with one decision tree. However, because the number of comparisons per variables is limited to the form given in the example above, the deep-level decomposition of the two Bin Engines of the previous subsection is superfluous.
Figure 22: Example of the Cut Eraser algorithm result for two input variables with mock data. The number in each region represents the BDT output score that corresponds to that bin. The top plot shows the scores in each bin prior to the cut eraser step. Small arrows indicate the differences in the scores of adjacent bins, which is ≤ 0.05. If the threshold to remove cuts is ≤ 0.05 then the vertical boundary is removed and the result is the bottom plot.
Figure 23: Example of the Cut Eraser iterative process for one input variables with mock data. The removal occurs in two iterations represented by the top two diagrams, followed by the resulting diagram at the bottom. The top-most diagram corresponds to the final bin boundaries in the layer $\ell = 5$ of figure 20. If the threshold to remove cuts is $< 0.05$ then the vertical boundary is removed and the result is the bottom plot. This iterative procedure occurs during the optimization stage in software and not in the resulting firmware.
Instead, two comparisons are made for each variable using comparators. The AND of all of the results of the comparators gives the output score of the cut-based approach. The value of 1 designates that the event passed the criteria and 0 designates that the event failed the criteria. We note that the output score needs to be transformed from the purity formulation to the adjusted purity variant (see table 10) in order to perform the Tree Remover step.

The cut-based method is implemented in firmware independently of the BDT implementation. Two if-else statements are used in each dimension to see

- If the variable is greater than the lower bound and
- If the variable is less than the upper bound.

We note that our requirement is $c < x < c'$ rather than $c < x \leq c'$, $c \leq x < c'$, or $c \leq x \leq c'$, as the choice is arbitrary and the user can specify the bounds as needed. These comparisons can be performed for each variable in parallel on an FPGA, which allow for very low latency values. As with BDT, the cut-based method can be converted to $N$-bit integers in advance for faster processing in firmware.

### D.2 Firmware verification and validation

The test bench for the verification and validation is given in the bottom and top diagrams, respectively, of figure 24.¹⁰

To further verify the generated design, we compare the results from firmware simulation with the performance of the IP running in hardware on a physical FPGA. For the comparison two Xilinx FPGAs are chosen:

- Virtex UltraScale+ FPGA VCU118 Evaluation Kit (EK-U1-VCU118-G), our benchmark,
- Artix-7 FPGA on Zynq-7020 System on Chip (SoC), a smaller FPGA.

The Artix-7 has 53 200 LUT, 106 400 FF, 140 BRAM of 36k blocks, noURAM, 220 DSP. The clock speed on the Artix-7 is slowed to 100 MHz to meet timing. Since this change in timing was done on the FPGA and in the fwXmachina design flow, the result comparisons reflect the accuracy of the simulated results. Test are done with varying clock speed and Vivado versions. No change in latency is seen (figure 25).

[¹⁰We briefly mention the role of C-simulation. C-simulation is a test bench by using the c++ compiler. This provides functional testing of the algorithm. However, being purely based on the c++ compiler, it does not offer any insights in the hardware-level information. Therefore, C-simulation can be run without synthesis or co-simulation. In contrast, co-simulation generates an RTL test bench used to verify the RTL output of the HLS C-synthesis. This internal test bench is executed and its results are compared to the C-simulation results. Therefore, co-simulation necessarily requires C-simulation. Further testing may also be performed using Xilinx Vivado and a custom RTL test bench. This testing may be useful after the generated IP is integrated into a larger design. Because this type of testing is dependent on the use case of the IP, it is not automatically generated by the fwXmachina design flow.]
Figure 24: Diagrams of the test bench. The top setup validates the BDT output score $O$ with respect to software simulation for a large number of test vectors and configurations. The bottom setup verifies the co-simulation results against the physical FPGA. The “core” in the diagram is the output of Vivado HLS. In both setups, the HLS co-simulation that is being tested is the same; two instances are drawn for figure clarity. The dark blue boxes are part of Nanosecond Optimization (figure 1), but is included here for completeness.
The results for FPGA resource utilization shows better-than-expected results. Interestingly, the LUT usage is much lower at 13% of the simulated result. The FF and BRAM usage is also lower at 68% and 50%, respectively. This indicates that Vivado is able to significantly optimize the design that is generated by HLS. It is important to note that the resource usage generated by HLS is estimated. HLS may generate designs that are not optimized efficiently for implementation. In that case, when the design is implemented, Vivado will remove redundant or unnecessary hardware, often resulting in lower resource utilization.

Table 12: FPGA cost verification against physical FPGA. Comparison of the FPGA cost using the bitstream on the FPGA (actual), simulated timing using co-simulation and estimated resources using Vivado HLS (estimated). The actual-to-estimated ratios are given as $R$. Two FPGA choices and three clock speeds are considered; the 320 MHz group of columns represent the benchmark clock. For all other configurable parameters, see table 1. The timing values are reported in units of clock ticks. The Xilinx Vivado version used for the actual and estimated columns are noted. For the ratios, “1” signifies no difference.

| Parameter | Benchmark FPGA | Smaller FPGA |
|-----------|----------------|--------------|
| FPGA setup |                |              |
| Family    | Xilinx Virtex Ultrascale+ | Xilinx Artix-7 |
| Model     | xcvu9p-flga2104-2L-e | xc7z020-clg400-1 |
| Speed     | 320 MHz         | 200 MHz       |
|           | 100 MHz         | 100 MHz       |
| Period    | 3.125 ns        | 5 ns          |
|           | 10 ns           | 10 ns         |
| Vivado    | 2019.2          | 2019.2        |
|           | 2019.2          | 2018.2        |
|           | 2018.2          | 2018.2        |
|           | 2019.1          | 2019.2        |
| FPGA cost | actual / estim. = $R$ | actual / estim. = $R$ | actual / estim. = $R$ | actual / estim. = $R$ |
| Latency   | 3 / 3 = 1      | 2 / 2 = 1     | 1 / 1 = 1     | 4 / 4 = 1     |
| Interval  | 1 / 1 = 1      | 1 / 1 = 1     | 1 / 1 = 1     | 1 / 1 = 1     |
| LUT       | 717 / 1903 = 0.4 | 717 / 4015 = 0.2 | 717 / 4007 = 0.2 | 482 / 3572 = 0.1 |
| FF        | 147 / 138 = 1.1 | 147 / 113 = 1.3 | 147 / 2 = 73  | 245 / 362 = 0.7 |
| BRAM      | 5.5 / 8 = 0.7  | 5.5 / 15 = 0.4 | 5.5 / 15 = 0.4 | 7.5 / 15 = 0.5 |
| URAM      | 0 / 0 = 0      | 0 / 0 = 0     | 0 / 0 = 0     | NA / NA = NA  |
| DSP       | 2 / 0 = NA     | 2 / 2 = 1     | 2 / 2 = 1     | 2 / 2 = 1     |

The physics performance is validated by considering the pairs of input variable values $\bar{x}$ and the corresponding BDT output score $O_i$. The output of the HLS co-simulation and the software simulation is called $O_{\text{cosim}}$ and $O_{\text{bit-sw}}$, respectively. The differences $\Delta_{\text{bit-sw}} = O_{\text{est}} - O_{\text{bit-sw}}$ are computed to validate the result. No difference is seen.

As the firmware design operates on bit integers, the floating point input vector is modified to simulate bit integers for the software evaluation. This modification occurs in the Bit Integer Converter that serves as an interface between the input test vectors and the FwXmachine module to compute the BDT output score. The diagram of the dataflow is shown at the top diagram of figure 24.

The test bench for this project is generated in C++ along with the design itself and can be used to evaluate the design on an algorithmic level. Using C/RTL co-simulation, the synthesized can be
evaluated with the same test bench. **fwXmachina** generates a unique test bench for the user with every design that it produces, so the user may validate their own design.

We considered over 200 different configurations each corresponding to a firmware simulated “core,” which is the RTL-level output of HLS C-synthesis. For each core $10^5$ input data vectors are fed into the test bench.

The output of the HLS co-simulation and software simulation are compared. We note that the wrapper code converts the test vectors from floating point values to the corresponding bit integer values. In all of the tests we saw no difference between the firmware output and the bit-integer-simulated software output.

### E Physics performance AUC results from parameters scans

We report the relative AUC in percentage with respect to our benchmark point where we scan the four parameters. The results are plotted in figure 26. A turn-on effect is observed, wherein it rapidly plummets below some threshold value while it remains relatively flat above that value. We note that our benchmark point is well above the threshold values for each parameter.
Nanosecond ML event classification with BDT in FPGA for HEP

Figure 26: Physics performance measured with area under the ROC curve (AUC) relative to the benchmark point. Two trends are seen: the rapid fall off below the visible threshold value and the flat with fluctuations above that threshold value. The point off the chart has the value 73 for $N_{\text{bit}} = 2$. The lines connecting the symbols serve as a visual guide and do not represent interpolations. The benchmark point (table 1) is marked by a star.

F Study of the number of jet pairs for VBF Higgs vs. multijet

The classifier is trained on the highest $m_{jj}$ reconstructed jet pair with VBF $H \rightarrow \text{invisible}$ as signal and the multijet process as background. For testing the training step, the final BDT score for the event is the highest BDT score from all possible jet pairs in the event.

The number of jets ($N_{\text{jet}}$) and the number of jet pairs ($N_{\text{jet pairs}}$ or $J$) per event depend on two external factors. The first factor is the set of user-defined criteria, such as the minimum $p_T$ threshold for each jet in the event or a minimum $m_{jj}$ to be considered. Furthermore, we assume that the list of jet pairs can be sorted based on the $m_{jj}$ such that any pair below a user-defined threshold can be discarded. The second factor is the user-defined maximum value of $J_{\text{max}}$ to consider, where if the number of jet pairs $J$ exceeds $J_{\text{max}}$ those with the lowest $m_{jj}$ can be ignored.

For ROC curve comparisons, we compare the scenario with BDT output scores from all jet pairs, i.e., no limit on $J_{\text{max}}$ against BDT output scores for $J_{\text{max}} = 3$ highest $m_{jj}$ pairs. We also considered a study of 6 jet pairs, but negligible difference is seen with respect to the result for 3.

The distribution of $N_{\text{jet}}$ with $p_T > 20$ GeV is shown for the background and the signal samples in the left plot of figure 27. The number of jet pairs $J$ is the quantity of interest for performance, which is $J = N_{\text{jet}}(N_{\text{jet}} - 1)/2$. The distribution is shown on the right plot of figure 27. As events with no jet pairs are not considered, only events with $J \geq 1$ are considered.
Figure 27: Number of jets with $p_T > 20 \text{ GeV}$ (left) and number of jet pairs (right). The variable $N_{\text{jet-pairs}}$ is referred to as $J$ in the text. The negligible number of events in the overflow bin with $N_{\text{jet-pairs}} \geq 16$ for $4b$ containing $< 1\%$ of the events is omitted from the plot.

G Benchmark configuration run on hls4ml/Conifer code

We compare the result using \texttt{fwXmachina} with the result using hls4ml/Conifer, both using the same \texttt{TMVA} output file corresponding to the setup of table 1. Both results use the same BDT trained by \texttt{TMVA} for our benchmark case with the configuration parameters noted in table 13, i.e., the same physics problem of binary classification, the same number of variables, the same number of trees, and the same clock speed. We obtained the most recent git commit of hls4ml/Conifer at the time of writing this paper [69].

We note that the application of Nanosecond Optimization (section 3) and the use of Bin Engines (sections 4.1 and 4.2) are unique to the design of \texttt{fwXmachina} and cannot be applied for the inputs to and the configuration of hls4ml/Conifer. Another notable difference is in the choice of representation of variable precision. We use $N$-bit integers, where $N$ is the number of bits to represent the values ranging from $0$ to $2^N - 1$, whereas hls4ml/Conifer uses fixed point precision.

For the benchmark point, we use 8-bit integers. For hls4ml/Conifer, rather than using the code’s default choice of $(18,8)$—which represents 18 total bits to represent the values with 8 of them representing the part before the decimal point and 10 of them representing the part after the decimal point—we make a choice to approximate our 8-bit integer precision. For this consideration, we inspect the distributions of figure 18 and the ranges of the plotted variables. For example, $E_0$ ranges from 0 to 25 GeV while $f_1$ ranges from 0 to 1. The bins used for these plots can be reasonably approximated by a choice of 32 bins, as 16 bins seem too coarse to separate the two samples.

\footnote{The results for hls4ml/Conifer has been updated since the initial draft of this paper [2104.03408v1]. The revised draft [2104.03408v2] reports the results from C synthesis using the latest version of the package [69] and the associated setup file to execute the code through correspondence with one of the authors of the code. This paper updates the comparison using the results from the RTL synthesis and implementation.}
Therefore, 5 bits are chosen for the part above the decimal point to span 0 to 25 GeV with bins that are approximately 0.8 GeV, while 5 bits are also chosen for the part below the decimal point to span 0 to 1 with bins that are approximately 0.03 wide. While a more thorough study is needed, perhaps by comparing the physics performance scanning over the precision parameter space, we use the above reasoning to set hls4ml/Conifer’s precision to \(10, 5\).

While we make the above choice for the result using hls4ml/Conifer, we note the following observation regarding variable precision. If hls4ml/Conifer is run using only 8 total bits as \(8, n\) with \(n < 8\), for instance, it would sacrifice accuracy when storing the cuts of certain variables. And depending on the split between integer and decimal bits, it could significantly impact the accuracy of the output scores.

Results from two tests are reported. First, the result from the hls4ml/Conifer code using \texttt{ap\_ufixed(10, 5)}\), which represents unsigned values, is 15 clock ticks for latency and 1 clock tick for interval. Second, the result using \texttt{ap\_fixed(18, 8)}\), the default out-of-the-box setting, gives similar results. The results for \texttt{fwXmachina} and hls4ml/Conifer using \texttt{ap\_ufixed(10, 5)}\) are summarized in table 13. The table shows the FPGA cost from the results using RTL synthesis and implementation (called “actual” in table 1), where the design is programmed on the FPGA via the bitstream file. The hls4ml/Conifer-to-\texttt{fwXmachina} ratio for the latency is about five while the ratios for LUT and FF are about five and ten, respectively. The interval is the same while RAM and DSP usage is zero or negligible for both projects.

Regarding the hls4ml/Conifer results that we report, it is likely that the FPGA cost from the out-of-the-box code can be reduced, as no problem-specific optimization was done on our side.
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Table 13: Comparison of the **fwXmachina** result (from table 1) and one from hls4ml/Conifer using the out-of-the-box code [69]. The test uses the benchmark configuration listed in table 1, i.e., the same BDT configuration from **TMVA** trained on the same training samples. The first two groups of rows show the parameters for ML training, FPGA, and firmware. The bottom group of rows shows the FPGA cost. See the text for the details regarding the choice of \texttt{ap\_ufixed}(10, 5), as well as the results using other choices for the precision.

| Parameter                        | fwXmachina                  | hls4ml/Conifer       | Comments                  |
|----------------------------------|------------------------------|----------------------|---------------------------|
| ML training setup                |                              |                      |                           |
| Training software                | **TMVA**                     | **TMVA**             | same                      |
| Physics problem                  | electron vs. photon          | electron vs. photon  | same                      |
| Training samples                 | from ref. [56]               | from ref. [56]       | same                      |
| No. of event classes             | 2                            | 2                    | same                      |
| No. of training trees            | 100                          | 100                  | same                      |
| Max. depth                       | 4                            | 4                    | same                      |
| No. of input variables           | 4                            | 4                    | See figure 18             |
| Other **TMVA** parameters        | **TMVA** defaults            | **TMVA** defaults    | same                      |
| Nanosec. Optimization            | Flattened & merged to 10     | N/A                  | Unique to fwX             |
|                                  | final trees, without \texttt{Tree Remover or Cut Eraser}       |                      |                           |
| FPGA and firmware setup          |                              |                      |                           |
| Chip family                      | Xilinx Virtex Ultrascale+    | Xilinx Virtex Ultrascale+ | same                      |
| Chip model                       | \texttt{xcvu9p-flga2104-2L-e} | \texttt{xcvu9p-flga2104-2L-e} | same                      |
| Vivado HLS version               | 2019.2                       | 2019.2               | same                      |
| Clock speed, period              | 320 MHz, 3.125 ns            | 320 MHz, 3.125 ns    | same                      |
| Precision                        | \texttt{ap\_int}(8)          | \texttt{ap\_ufixed}(10, 5) | See text                   |
| BIN ENGINE                       | BSBE                         | N/A                  | Unique to fwX             |
| FPGA cost                        |                              |                      |                           |
| Actual timing values and resource usage by RTL synthesis and implementation |                              |                      |                           |
| Latency                          | 3 clock ticks, 9.375 ns      | 15 clock ticks, 46.875 ns | -                         |
| Interval                         | 1 clock ticks, 3.125 ns      | 1 clock tick, 3.125 ns | same                      |
| LUT                               | 717, 0.06% of total          | 3834, 0.3% of total  | -                         |
| FF                                | 147, < 0.01% of total        | 1966, < 0.1% of total | -                         |
| BRAM 18k                          | 5.5, 0.1% of total           | 0                    | -                         |
| URAM                              | 0                            | 0                    | same                      |
| DSP                               | 2, 0.03% of total            | 0                    | -                         |
References

[1] L. Evans and P. Bryant, *LHC Machine*, JINST 3, S08001 (2008).

[2] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST 3, S08003 (2008).

[3] CMS Collaboration, *The CMS Experiment at the CERN LHC*, JINST 3, S08004 (2008).

[4] ATLAS Collaboration, *Performance of the ATLAS Trigger System in 2010*, Eur. Phys. J. C 72, 1849 (2012).

[5] ATLAS Collaboration, *Performance of the ATLAS Trigger System in 2015*, Eur. Phys. J. C 77, 317 (2017).

[6] CMS Collaboration, *The CMS trigger system*, JINST 12, P01020 (2017).

[7] R. Achenbach et al., *The ATLAS level-1 calorimeter trigger*, JINST 3, P03001 (2008).

[8] CMS Collaboration, *The Phase-2 Upgrade of the CMS Endcap Calorimeter*, CERN-LHCC-2017-023, 2017, http://cds.cern.ch/record/2293646.

[9] CMS Collaboration, *Performance of the CMS Level-1 trigger in proton-proton collisions at \( \sqrt{s} = 13\) TeV*, JINST 15, P10017 (2020).

[10] ATLAS Collaboration, *Performance of the upgraded PreProcessor of the ATLAS Level-1 Calorimeter Trigger*, JINST 15, P11016 (2020).

[11] M. Cacciari, G. P. Salam, and G. Soyez, *The anti-\( k_t \) jet clustering algorithm*, JHEP 04, 063 (2008).

[12] ATLAS Collaboration, *Performance of electron and photon triggers in ATLAS during LHC Run 2*, Eur. Phys. J. C 80, 47 (2020).

[13] ATLAS Collaboration, *Performance of the ATLAS Level-1 topological trigger in Run 2*, 2021, [2105.01416].

[14] S. Neuhaus et al., *A neural network \( z \)-vertex trigger for Belle II*, J. Phys. Conf. Ser. 608, 012052 (2015).

[15] D. Acosta et al., on behalf of the CMS Collaboration, *Boosted Decision Trees in the Level-1 Muon Endcap Trigger at CMS*, J. Phys. Conf. Ser. 1085, 042042 (2018).

[16] Ed. C. Verkerk, *1989 CERN School of Computing, Bad Herrenalb, FR Germany, 20 Aug-2 Sep 1989: Proceedings*, http://dx.doi.org/10.5170/CERN-1990-006.

59
Nanosecond ML event classification with BDT in FPGA for HEP

[17] Ed. C. Verkerk, *1991 CERN School of Computing, Ystad, Sweden, Aug 23- Sep 2 1991: Proceedings*, http://dx.doi.org/10.5170/CERN-1992-002.

[18] D0 Collaboration, *Evidence for production of single top quarks and first direct measurement of |Vtb|*, Phys. Rev. Lett. 98, 181802 (2007).

[19] Ed. A. J. Bevan, B. Golob, Th. Mannel, S. Prell, and B. D. Yabsley, *The Physics of the B Factories*, Eur. Phys. J. C 74, 3026 (2014).

[20] ATLAS Collaboration, *Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC*, Phys. Lett. B 716, 1-29 (2012).

[21] CMS Collaboration, *Observation of a New Boson at a Mass of 125 GeV with the CMS Experiment at the LHC*, Phys. Lett. B 716, 30-61 (2012).

[22] ATLAS Collaboration, *Performance of b-Jet Identification in the ATLAS Experiment*, JINST 11, P04008 (2016).

[23] ATLAS Collaboration, *Measurements of b-jet tagging efficiency with the ATLAS detector using t\bar{t} events at \sqrt{s} = 13 TeV*, JHEP 08, 089 (2018).

[24] ATLAS Collaboration, *Convolutional Neural Networks with Event Images for Pileup Mitigation with the ATLAS Detector*, ATL-PHYS-PUB-2019-028, 2019, http://cds.cern.ch/record/2684070.

[25] ATLAS Collaboration, *Identification of hadronic tau lepton decays using neural networks in the ATLAS experiment*, ATL-PHYS-PUB-2019-033, 2019, http://cds.cern.ch/record/2688062.

[26] ATLAS Collaboration, *Deep Learning for Pion Identification and Energy Calibration with the ATLAS Detector*, ATL-PHYS-PUB-2020-018, 2020, http://cds.cern.ch/record/2724632.

[27] J. Duarte et al., *Fast inference of deep neural networks in FPGAs for particle physics*, JINST 13, P07027 (2018).

[28] S. Summers et al., *Fast inference of Boosted Decision Trees in FPGAs for particle physics*, JINST 15, P05026 (2020).

[29] V. Loncar et al., *Compressing deep neural networks on FPGAs to binary and ternary precision with HLS4ML*, 2020, [2003.06308].

[30] Y. Iiyama et al., *Distance-Weighted Graph Neural Networks on FPGAs for Real-Time Particle Reconstruction in High Energy Physics*, Front. Big Data 3, 598927 (2020).

[31] A. Heintz et al., *Accelerated Charged Particle Tracking with Graph Neural Networks on FPGAs*, 2020, [2012.01563].
Nanosecond ML event classification with BDT in FPGA for HEP

[32] C. N. Coelho, A. Kuusela, S. Li, et al., *Automatic heterogeneous quantization of deep neural networks for low-latency inference on the edge for particle detectors*, Nat. Mach. Intell. 3, (2021).

[33] J. St. John et al., *Real-time Artificial Intelligence for Accelerator Control: A Study at the Fermilab Booster*, 2020, [2011.07371].

[34] F. Fahim et al., *hls4ml: An Open-Source Codesign Workflow to Empower Scientific Low-Power Machine Learning Devices*, 2021, [2103.05579].

[35] T. Aarrestad et al., *Fast convolutional neural networks on FPGAs with hls4ml*, 2021, [2101.05108].

[36] B. Hawks et al., *Ps and Qs: Quantization-aware pruning for efficient low latency neural network inference*, 2021, [2102.11289].

[37] S. Lopez-Estrada and R. Cumplido, *Decision Tree Based FPGA-Architecture for Texture Sea State Classification* 2006 IEEE Int’l Conf. on Reconfigurable Computing and FPGA’s (ReConFig 2006), 1-7 (2006).

[38] R. Narayanan, D. Honbo, G. Memik, A. Choudhary, and J. Zambreno, *An FPGA Implementation of Decision Tree Classification*, 2007 Design, Automation Test in Europe Conference Exhibition, 1-6 (2007).

[39] Q. Li and A. Bermak, *A Low-Power Hardware-Friendly Binary Decision Tree Classifier for Gas Identification*, J. of Low Power Electronics & Applications 1, 45-58 (2011).

[40] R. Kulaga and M. Gorgoń, *FPGA Implementation of Decision Trees and Tree Ensembles for Character Recognition in Vivado HLS*, Image Processing & Commum. 19, 2-3 (2014).

[41] D. Tong, Y. R. Qu, and V. K. Prasanna, *Accelerating Decision Tree Based Traffic Classification on FPGA and Multicore Platforms*, IEEE Transactions on Parallel & Distributed Systems 28, 3046-3059 (2017).

[42] M. Owaida, H. Zhang, C. Zhang, and G. Alonso, *Scalable inference of decision tree ensembles: Flexible design for CPU-FPGA platforms*, 2017 27th Int’l Conf. on Field Programmable Logic & Applications (FPL), 1-8 (2017).

[43] K. Kara, D. Alistarh, G. Alonso, O. Mutlu, and C. Zhang, *FPGA-Accelerated Dense Linear Machine Learning: A Precision-Convergence Trade-Off*, 2017 IEEE 25th Annual Int’l Symp. on Field-Programmable Custom Computing Machines (FCCM), 160-167 (2017).
Nanosecond ML event classification with BDT in FPGA for HEP

[44] Z. Lin, S. Sinha, and W. Zhang, *Towards Efficient and Scalable Acceleration of Online Decision Tree Learning on FPGA*, 2019 IEEE 27th Annual Int'l Symp. on Field-Programmable Custom Computing Machines (FCCM), 172-180 (2019).

[45] A. Elkanishy et al., *An FPGA Decision Tree Classifier to Supervise a Communication SoC*, 2019 IEEE High Performance Extreme Comput. Conf. (HPEC), 1-6 (2019).

[46] A. Hoecker, P. Speckmayer, J. Stelzer, et al., *TMVA - Toolkit for Multivariate Data Analysis*, CERN-OPEN-2007-007, 2007, [physics/0703039].

[47] F. Pedregosa et al., *Scikit-learn: Machine Learning in Python*, J. Machine Learning Res. **12**, 2825-2830 (2011).

[48] Xilinx Inc., *Xilinx Vivado Design Suite Tutorial: High-Level Synthesis v2019.2*, https://www.xilinx.com/support/documentation/sw Manuals/xilinx2019_2/ug871-vivado-high-level-synthesis-tutorial.pdf accessed May 14, 2021.

[49] Xilinx Inc., *Xilinx Vivado Design Suite User Guide v2019.2*, https://www.xilinx.com/support/documentation/sw Manuals/xilinx2019_2/ug973-vivado-release-notes-install-license.pdf, accessed May 14, 2021.

[50] N. P. Ghanathe et al., *Software and firmware co-development using high-level synthesis*, JINST **12**, C01083 (2017).

[51] C. W. Fabjan and D. Fournier, *Calorimetry* in ed. C. Fabjan and H. Schopper, Particle Physics Reference Library, Springer, Cham., 201-280, 2020.

[52] M. Andrews, M. Paulini, S. Gleyzer, and B. Poczos, *End-to-End Physics Event Classification with CMS Open Data: Applying Image-Based Deep Learning to Detector Data for the Direct Classification of Collision Events at the LHC*, Comput. Softw. Big Sci. **4**, 6 (2020).

[53] L. De Oliveira, B. Nachman, and M. Paganini, *Electromagnetic Showers Beyond Shower Shapes*, Nucl. Instrum. Meth. A **951**, 162879 (2020).

[54] Y. Freund and R. E. Schapire, *A Decision-Theoretic Generalization of On-Line Learning and an Application to Boosting*, J. Comput. Syst. Sci. **55**, 119-139 (1997).

[55] J. Shapiro, *Genetic Algorithms in Machine Learning*, in ed. G. Paliouras, V. Karkaletsis, and C. D. Spyropoulos, Machine Learning and Its Applications, ACAA 1999, Lecture Notes in Comp. Sci., vol. 2049, Springer, Berlin, Heidelberg, 2001.

[56] B. Nachman, L. de Oliveira, and M. Paganini, *Electromagnetic Calorimeter Shower Images*, Mendeley Data, V1, 2017, http://dx.doi.org/10.17632/pvn3xc3wy5.1, accessed Mar. 30, 2021.
[57] ATLAS Collaboration, *Search for invisible Higgs boson decays in vector boson fusion at $\sqrt{s} = 13$ TeV with the ATLAS detector*, Phys. Lett. B 793, 499-519 (2019).

[58] CMS Collaboration, *Search for invisible decays of a Higgs boson produced through vector boson fusion in proton-proton collisions at $\sqrt{s} = 13$ TeV*, Phys. Lett. B 793, 520-551 (2019).

[59] ATLAS Collaboration, *Search for invisible Higgs boson decays with vector boson fusion signatures with the ATLAS detector using an integrated luminosity of 139 fb$^{-1}$*, ATLAS-CONF-2020-008, 2020, http://cds.cern.ch/record/2715447.

[60] CMS Collaboration, *The Phase-2 Upgrade of the CMS Level-1 Trigger*, CERN-LHCC-2020-004 and CMS-TDR-021, 2020, http://cds.cern.ch/record/2714892.

[61] P. J. Giabbanelli and J. G. Peters, *An Algebra to Merge Heterogeneous Classifiers*, 2015, [1501.05141].

[62] P. Strecht, *A Survey of Merging Decision Trees Data Mining Approaches*, 10$^{th}$ Doctoral Symp. in Informatics Eng. (DSIE’15), 2015.

[63] J. Friedman, *Greedy function approximation: A gradient boosting machine.*., Annals of Statistics, 29, 1189-1232 (2001), accessed May 14, 2021.

[64] ATLAS Collaboration, *Trigger menu in 2018*, ATL-DAQ-PUB-2019-001, 2019, http://cds.cern.ch/record/2693402.

[65] ATLAS Collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*, CERN-LHCC-2017-020, 2017, http://cds.cern.ch/record/2285584.

[66] ATLAS Collaboration, *Measurement of the Inelastic Proton-Proton Cross Section at $\sqrt{s} = 13$ TeV with the ATLAS Detector at the LHC*, Phys. Rev. Lett. 117, 182002 (2016).

[67] ATLAS Collaboration, *Luminosity determination in pp collisions at $\sqrt{s} = 13$ TeV using the ATLAS detector at the LHC*, ATLAS-CONF-2019-021, 2019, http://cds.cern.ch/record/2677654.

[68] D. de Florian et al. (LHC Higgs Cross Section Working Group), *Handbook of LHC Higgs Cross Sections: 4. Deciphering the Nature of the Higgs Sector*, CERN-2017-002, 2016, [1610.07922].

[69] S. Summers et al., Conifer git repository, http://github.com/thesps/conifer/releases/tag/v0.0, accessed May 7, 2021.

[70] M. Paganini, L. de Oliveira, and B. Nachman, *CaloGAN: Simulating 3D high energy particle showers in multilayer electromagnetic calorimeters with generative adversarial networks*, Phys. Rev. D 97, 014021 (2018).
Nanosecond ML event classification with BDT in FPGA for HEP

[71] M. Paganini, L. de Oliveira, and B. Nachman, *Accelerating Science with Generative Adversarial Networks: An Application to 3D Particle Showers in Multilayer Calorimeters*, Phys. Rev. Lett. **120**, 042003 (2018).

[72] S. Agostinelli et al., *GEANT4—a simulation toolkit*, Nucl. Instrum. Meth. A **506**, 250-303 (2003).

[73] ATLAS Collaboration, *Readiness of the ATLAS Liquid Argon Calorimeter for LHC Collisions*, Eur. Phys. J. C **70**, 723-753 (2010).

[74] The definition of $l_{d2}$ is found as lateralDepth2 in the CaloGAN gitlab code repository. See line 77 of http://github.com/hep-lbdl/CaloGAN/blob/79b63a71f87df5dcacb0dd511172c30b2a881943/analysis/feats1d.py, accessed Mar. 30, 2021.

[75] S. T. Roche, B. T. Carlson, and T. M. Hong, *fwXmachina example: VBF Higgs vs multijet*, Mendeley Data, V1, 2021, http://dx.doi.org/10.17632/kp3myh3v89.1, accessed May 11, 2021.

[76] J. Alwall et al., *The automated computation of tree-level and next-to-leading order differential cross sections, and their matching to parton shower simulations*, JHEP **07**, 079 (2014).

[77] T. Sjöstrand et al., *An introduction to PYTHIA 8.2*, Comput. Phys. Commun. **191**, 159-177 (2015).

[78] U. Ellwanger, J. F. Gunion, and C. Hugonie, *Difficult scenarios for NMSSM Higgs discovery at the LHC*, JHEP **07**, 041 (2005).

[79] D. Curtin et al., *Exotic decays of the 125 GeV Higgs boson*, Phys. Rev. D **90**, 075004 (2014).

[80] ATLAS Collaboration, *Search for the Higgs boson produced in association with a vector boson and decaying into two spin-zero particles in the $H \rightarrow aa \rightarrow 4b$ channel in $pp$ collisions at $\sqrt{s} = 13$ TeV with the ATLAS detector*, JHEP **10**, 031 (2018).

[81] ATLAS Collaboration, *Search for Higgs boson decays into two new low-mass spin-0 particles in the 4b channel with the ATLAS detector using $pp$ collisions at $\sqrt{s} = 13$ TeV*, Phys. Rev. D **102**, 112006 (2020).

[82] S. Ovyn, X. Rouby, and V. Lemaitre, *DELPHES, a framework for fast simulation of a generic collider experiment*, 2009, [0903.2225].

[83] DELPHES 3 Collaboration, *DELPHES 3, A modular framework for fast simulation of a generic collider experiment*, JHEP **02**, 057 (2014).

[84] ATLAS Collaboration, *Measurement of the $Z/\gamma^*$ boson transverse momentum distribution in $pp$ collisions at $\sqrt{s} = 7$ TeV with the ATLAS detector*, JHEP **09**, 145 (2014).
[85] CMS Collaboration, *Pileup Jet Identification*, CMS-PAS-JME-13-005, 2013, http://cds.cern.ch/record/1581583.

[86] R. A. Callejas-Molina, V. M. Jimenez-Fernandez, and H. Vazquez-Leal, *Digital architecture to implement a piecewise-linear approximation for the hyperbolic tangent function*, 2015 International Conference on Computing Systems and Telematics (ICCSAT), 1-4 (2015).