CBP: Coordinated management of cache partitioning, bandwidth partitioning and prefetch throttling

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ABSTRACT
Reducing the average memory access time is crucial for improving the performance of applications running on multi-core architectures. With workload consolidation this becomes increasingly challenging due to shared resource contention. Techniques for partitioning of shared resources - cache and bandwidth - and prefetching throttling have been proposed to mitigate contention and reduce the average memory access time. However, existing proposals only employ a single or a subset of these techniques and are therefore not able to exploit the full potential of coordinated management of cache, bandwidth and prefetching. Our characterization results show that application performance, in several cases, is sensitive to prefetching, cache and bandwidth allocation. Furthermore, the results show that managing these together provides higher performance potential during workload consolidation as it enables more resource trade-offs. In this paper, we propose CBP a coordination mechanism for dynamically managing prefetching throttling, cache and bandwidth partitioning, in order to reduce average memory access time and improve performance. CBP works by employing individual resource managers to determine the appropriate setting for each resource and a coordinating mechanism in order to enable inter-resource trade-offs. Our evaluation on a 16-core CMP shows that CBP, on average, improves performance by 11% compared to the state-of-the-art technique that manages cache partitioning and prefetching and by 50% compared to the baseline without cache partitioning, bandwidth partitioning and prefetch throttling.

1 INTRODUCTION
Memory access time has a significant impact on application performance. Effective utilization of the memory system is therefore necessary. Typically, resources in the memory system (e.g., last-level cache (LLC) and off-chip memory bandwidth) are shared among multiple cores as they help in improving resource utilization during workload consolidation. However, sharing can detrimentally impact average memory access time and performance due to resource contention. Prior works have proposed partitioning of shared resources – cache \cite{10, 15, 19, 26, 28} and bandwidth \cite{13, 17, 24} – and prefetching \cite{11} to mitigate contention, reduce or hide memory access time and improve performance.

Recent works have proposed combining cache and bandwidth partitioning \cite{4, 23, 27}, prefetching and cache partitioning \cite{31, 33} and bandwidth partitioning and prefetching \cite{8, 18} to provide additional performance gains. The key insight from these papers is that coordinated management of two techniques is more advantageous than considering each in isolation because of the trade-offs that are made possible. However, no study so far has considered combining all three techniques. The goal of this paper is to do so.

Coordinated management of cache partitioning, bandwidth partitioning and prefetch throttling provides the following advantages. Firstly, it makes it possible to address more applications and cover a broader range of workloads, as shown in our in-depth performance characterization (see Section 2). The results show that 90% of the applications in the SPEC CPU2006 suite have performance sensitivity (over 10% change in IPC) to at least one of the techniques, and 70% are also sensitive to multiple techniques. Secondly, managing these techniques jointly opens up the opportunity to new and improved trade-offs. There are synergistic interactions between the techniques and these cannot be realized if cache partitioning, bandwidth partitioning and prefetch throttling are not jointly managed.

As an example, consider the simple case of a workload comprising of two applications. The first application, lbm, is sensitive to bandwidth and prefetching while the second, xalancbmk, is sensitive to cache size and has lower performance when prefetching is enabled. The best solution when managing all three techniques is to give xalancbmk a large cache allocation, small bandwidth allocation and disable the prefetcher, while giving lbm a large bandwidth allocation, small cache allocation while keeping the prefetcher active. Figure 1 shows the performance from coordinated management of all three techniques (\textit{cache+bw+pref}) compared to managing a subset of the techniques. The results show that the solution that manages all three techniques is better than others that manage two of the techniques, and leads to an additional performance gain of 15%. The main challenge of coordinately managing all three techniques is the complexity of evaluating all possible allocations.

Figure 1: Workload with lbm and xalancbmk. Total bandwidth 16GB/s, total cache size 2MB. Executing applications for 1B instructions, more details in Section 4. Settings: lbm-prefetching active, 12GB/s, xalancbmk-prefetcher inactive, 4GB/s, determined from characterization (Section 2). Cache partition sizes are decided dynamically.
dynamically and determining the best possible allocation while exploiting the large number of possible trade-offs.

Guided by our characterization results, we propose CBP, a coordinated mechanism for dynamically managing cache partitioning, bandwidth partitioning and prefetch throttling for multi-programmed workloads. CBP consists of three local controllers, one for each resource that together with a coordination mechanism manages and allocates the resources. With CBP, the three techniques are dynamically tuned in an iterative fashion. First, cache space is allocated since avoiding a memory access altogether is better than reducing their latency. As a next step, bandwidth is allocated taking into consideration the impact due to cache allocation. Lastly, the prefetch setting is determined by testing the impact of prefetching on performance for the current allocation of bandwidth and cache. The prefetcher performance influences the next reallocation of cache space and bandwidth. The feedback mechanism between the different techniques dynamically adapts the allocations in order to reach a good configuration depending on the characteristics of the individual applications in the workload. Our approach of combining local controllers with a feedback mechanism reduces the complexity.

In summary, we make the following contributions:

(a) We present an in-depth characterization of the performance impact of cache, bandwidth and prefetching on the entire SPEC CPU2006 suite. Our characterisation results provide several insights: i) a majority of the applications (over 90%) are sensitive to one or multiple techniques, ii) managing cache, bandwidth and prefetch, opens up opportunities for exploiting more trade-offs and improving performance for consolidated workloads, and iii) managing cache, bandwidth and prefetch jointly has the potential to outperform combinations of two of the techniques.

(b) We propose CBP, a mechanism to dynamically manage the three resources in coordination. The solution is based on simple heuristics in order to sidestep the complexity associated with evaluating all possible configurations and choosing the most efficient configuration. CBP works by employing individual resource managers to determine the appropriate setting for each resource and a coordinating mechanism to enable inter-resource trade-offs.

(c) We evaluate our solution with multi-programmed workloads on a 16-core tiled CMP. CBP improves performance by up to 36% (geom. mean 11%) compared to the state-of-the-art technique that manages cache partitioning and prefetching in a coordinated manner and by up to 86% (geom. mean 50%) compared to an unpartitioned S-NUCA without cache partitioning, bandwidth partitioning and prefetching.

The rest of the paper is organized as follows. Section 2 motivates the need for a coordinated approach using cache partitioning, bandwidth partitioning and prefetch throttling. Section 3 describes our proposed solution in detail. We then discuss the methodology in Section 4 and Section 5 presents the evaluation of the proposal. We provide an overview of related work in Section 6 and conclude in Section 7.

2 CHARACTERIZATION

In order to motivate the need for coordinated management of cache partitioning, bandwidth partitioning and prefetch throttling, we perform a detailed characterization study of applications in the SPEC2006 CPU suite. The aim of this study is to: i) characterize applications to determine the extent to which they are performance sensitive to cache, bandwidth and prefetch settings, ii) understand the different resource interactions, their impact on performance and the inter-resource trade-offs that are possible, and iii) demonstrate the performance potential of coordinated management of all three resources over a subset of resources.

2.1 Sensitivity to cache, bandwidth and prefetch settings

To understand the sensitivity of applications to cache, bandwidth and prefetch settings we model a system consisting of one out-of-order core with a 3-level cache hierarchy using the Sniper simulator [5]. Details about the methodology are provided in Section 4. For this experiment, the baseline LLC and bandwidth allocation is 512kB and 4GB/s, respectively. We run the application in steady-state for 1B instructions and use IPC as a measure of performance.

Figure 2 shows the performance impact of changing the cache allocation, bandwidth allocation and enabling prefetching normalized to the baseline allocation without prefetching. Note that we only change the setting for one resource at a time. In Figure 2a, C-L and B-L represent low allocation settings where the cache allocation is decreased to 128kB and the bandwidth allocation is decreased to 1GB/s, respectively, while prefetching is disabled. Similarly, in Figure 2b, C-H and B-H represent high allocation settings where the cache allocation is increased to 2MB and the bandwidth allocation is increased to 16GB/s, while prefetching is disabled. Finally, P-B represents the setting where prefetching is enabled with the baseline cache and bandwidth allocation. We classify applications as performance sensitive to a specific resource if the modified allocation results in a 10% deviation from the baseline IPC. We refer to applications that are performance sensitive to change in cache allocation as cache sensitive (CS), sensitive to change in bandwidth allocation as bandwidth sensitive (BS) and sensitive to prefetch throttling as prefetch sensitive (PS).

The sensitivity results for cache size show that nearly 60% of the applications (17 out of 29) are sensitive to changes in cache allocation. The extent to which applications are performance sensitive varies greatly with a performance increase of up to 4x in some cases. Furthermore, a larger number of applications are sensitive in the low allocation setting in comparison to high allocation setting (17 compared to 11). The sensitivity results for bandwidth allocation also shows a similar trend, as more applications are sensitive in the low allocation setting compared to high allocation setting (23 compared to 15). Also, the extent of performance sensitivity varies greatly with an increase of up to 3x. The sensitivity results for prefetch throttling indicate that nearly 38% of the applications (11 out of 29) are sensitive to prefetching and experience a speedup. However, there are some applications that experience a slowdown due to prefetching. In summary, we make the following observation:

OBSERVATION 1. In SPEC CPU2006 suite 90% of the applications are sensitive to one resource, while 70% are sensitive to multiple resources and the extent of sensitivity varies greatly.
2.2 Inter-resource interactions and trade-offs

Next, we investigate inter-resource interactions and trade-offs that are enabled when jointly managing cache, bandwidth and prefetching. We focus on intra-application resource interaction initially. There are four possible types of interactions within an application: cache-bandwidth-prefetch, bandwidth - prefetch, cache - prefetch and cache - bandwidth.

Regarding the cache-bandwidth-prefetch trade-off, we want to find out how the performance impact from prefetching varies with the allocation of cache and bandwidth. Figure 3 shows the performance impact of prefetching for three different cache/bandwidth settings normalized to the respective baseline setting without prefetching. The cache and bandwidth setting for an application in a low allocation scenario (P-L) is 128kB and 1GB/s, the baseline allocation scenario (P-B) setting is 512kB and 4GB/s while the high allocation scenario (P-H) setting is 2MB and 16GB/s.

For some applications, lower bandwidth and cache allocation leads to higher sensitivity for prefetching as seen in hmmer. This is because avoiding a miss altogether, as a consequence of accurate prefetching, can have a larger impact in low allocation settings where the bandwidth is scarce and the memory queuing delays tend to be longer. Also, there are applications like gcc which experience higher prefetch sensitivity with a larger cache and bandwidth allocation. The results indicate that applications tend to be prefetch sensitive in some settings and prefetch insensitive in others. We make the following observation:

**Observation 2.** Allocation of cache and bandwidth influences prefetch sensitivity. Furthermore, applications tend to be prefetch sensitive in some settings and prefetch insensitive in others.

In the interest of space we use leslie3d as a representative example to illustrate the other pairwise resource interactions and trade-offs, since it is sensitive to all three techniques. Note that the baseline setting will be used for the resources unless specified otherwise. The bandwidth - prefetch interaction manifests in two different ways. Firstly, prefetching typically increases the number of memory accesses and this in turn increases the bandwidth pressure. In the case of leslie3d prefetching results in a 15% increase in the number of memory requests in comparison to the baseline. Note that prefetch misses, i.e. prefetched blocks that are evicted before use, can result in a further increase in pressure on the memory bandwidth. Secondly, the performance improvement from prefetching can be influenced by the bandwidth allocation. The results in Figure 4a show the performance for different bandwidth allocation with and without prefetching. We make the following observation:

**Observation 3.** A larger bandwidth allocation can compensate for increased bandwidth demands, due to inaccurate prefetches, leading to increased performance with prefetching.

The cache - prefetch interaction also manifests in two main ways. Firstly, the performance loss from reduced cache allocation can be offset if prefetching is effective. Figure 4c shows the IPC for different cache allocations with and without prefetching. The results show that the performance of 128kB allocation with prefetching is better than 512kB allocation without prefetching. Secondly, larger cache sizes (if it is used efficiently) can lead to higher speedup from prefetching. Figure 4b shows the performance improvement from prefetching with different cache allocation normalised to the respective cache allocation without prefetching. The results show that prefetching is effective with lower cache allocation and that...
its effectiveness can increase with additional allocation. The reason for this behaviour is that a larger cache reduces the number of memory accesses which has the same effect as increasing the available bandwidth, i.e. a lower queuing delay, which is more forgiving when there is an increase in memory accesses caused by inaccurate prefetches (in leslie3d there is a 15% increase in dram accesses caused by prefetching). These results lead to the following observation:

**OBSERVATION 4.** A trade-off can be made between either increasing cache size or enabling prefetching, leading to the same performance, for applications which are performance sensitive to both cache and prefetching.

As for the cache - bandwidth interaction, a lower bandwidth allocation can result in a larger sensitivity to cache size. Figure 4d shows the performance improvement from increasing the cache allocation from 512kB to 2MB with different bandwidth allocation settings. The results show that performance improvement from additional cache allocation is much higher in low bandwidth allocation settings (see the result for 1GB/s bandwidth allocation). This is because the average cost of a miss is much higher in the case of lower bandwidth allocation. The results also show that a large cache allocation can reduce the performance sensitivity to bandwidth allocation (see the result for 16GB bandwidth allocation). These results lead to the following observation:

**OBSERVATION 5.** A trade-off can be made between either increased cache space or increased bandwidth allocation, for applications which are performance sensitive to both cache and bandwidth.

We now describe how the observed intra-application interactions and trade-offs can be leveraged in the inter-application setting for multi-programmed workloads. Let us revisit the example of running a simple workload comprising two application (lbm and xalancbmk) on a dual-core system with 2MB LLC capacity and 16GB/s bandwidth, discussed in Figure 1. For achieving the best aggregate performance we expect xalancbmk to get the majority of the cache (nearly 1.75MB), while lbm is given a smaller cache allocation of 256kB. For bandwidth, we would expect lbm to have a large allocation (12GB/s) of the available bandwidth and xalancbmk to get a smaller allocation (4GB/s). This is reflected in Observation 5 about the trade-off between cache and bandwidth where we would prioritize the application that shows the highest sensitivity for the resource. Furthermore, as reflected in Observation 2, we expect prefetching to be more effective for lbm since it has a large allocation of bandwidth. In the case of xalancbmk, prefetching leads to lower performance regardless of the allocation of cache and bandwidth.

### 2.3 Potential for coordinated management

In order to show the potential for coordinated management of cache, bandwidth and prefetch we run 640 randomly generated workloads each comprising 4 SPEC 2006 CPU applications. We compare the performance of jointly managing all the three resources to other resource managers that only manage a subset of these resources. For this experiment the baseline allocation of cache and bandwidth for each application is 512kB and 4GB/s. We use an exhaustive search algorithm to find the best static configuration (over 1B instructions) for the different resources when running each workload. Figure 5a shows average (geometric mean) performance with different resource managers normalized to the baseline settings without prefetching. **equal on**, depicts the performance when prefetching is enabled for all applications and improves performance by 6% while **only pref**, depicts the performance when prefetching is selectively activated and improves performance by 9%. **cache+bw+pref** results show that coordinately managing cache partitioning, bandwidth partitioning and prefetch throttling improves performance by 5% compared to the best combination of two techniques (22% compared to 17%).

Figure 5b shows the number of workloads (among the 640 workloads considered) that experience a performance gain of at least 10% using the different resource managers discussed previously. The results show that 90% (597) of the workloads are sensitive to the resource manager that jointly manages all three techniques. A smaller fraction of the workloads are sensitive to resource managers that manage a subset of these techniques (77% are sensitive to cache+pref resource manager and 69% are sensitive to the cache+bw resource manager).

In summary, the results from the characterization study demonstrate that around 90% of applications in the SPEC 2006 CPU suite are sensitive to different resources and that coordinately managing them opens up new possibilities for improving performance.
3 CBP RESOURCE MANAGER

Section 3.1 provides an overview of the CBP resource manager. Section 3.2 discusses the individual resource controllers while Section 3.3 describes how the coordination mechanism ties the local resource controllers together. Finally, the implementation and overhead of the proposed mechanism is discussed in Section 3.4.

3.1 Overview

CBP is a coordinated management of cache partitioning, bandwidth partitioning and prefetch throttling. The design consists of one local controller for each of the three techniques, and a coordination mechanism, as shown in Figure 6.

The cache allocation controller estimates the number of misses for different cache sizes using auxiliary tag directories (ATDs) [26] and uses this as input for determining cache allocation. The cache allocation per application is determined such that it reduces the aggregate number of cache misses for the entire workload. The bandwidth allocation controller uses memory request queuing delay experienced by the applications as input and allocates the available bandwidth in proportion to the delay. The bandwidth allocation controller assigns a larger allocation of the available bandwidth to applications that experience longer queuing delay, and a comparatively lower allocation to those that experience shorter queuing delays. Lastly, the prefetch controller samples IPC with and without prefetching to determine whether the prefetcher should be enabled/disabled for each application.

The three techniques are dynamically tuned using the coordination mechanism in an iterative manner such that the local controller takes into consideration the decisions taken by the other controllers.

3.2 Local resource allocation controllers

A partitioning solution for shared resources like cache and bandwidth typically comprises two components: allocation policy, that determines how a resource is divided among multiple co-running applications, and an enforcement mechanism, that enforces the partitioning decision. Similarly, prefetch throttling involves a policy to determine the best prefetch setting to use and a mechanism implemented in hardware to enforce the setting. In the context of CBP, the policy component is of particular interest because it enables inter-resource trade-offs. We discuss the allocation policy in this section and defer the details of the enforcement mechanism to Section 3.4.

3.2.1 Cache partitioning. The cache allocation controller uses the Lookahead algorithm [26], to determine cache allocation. In a nutshell, the algorithm computes the utility for each application where utility is the measure of how many additional misses can be reduced with allocation of cache ways. It then computes the number of ways that maximizes the utility for each application (while ensuring this is less than the total number of ways available for allocation). Finally, it compares the utility values for the different applications, determines the application that has the highest utility and assigns the pre-computed number of ways that maximizes the utility for that application. The process repeats, with recomputation of utility for each application and reassignment of available cache ways to the application that has the largest utility, until the rest of the available capacity is distributed. The allocation controller relies on sampled ATDs to estimate, based on past behaviour, the number of misses that can be avoided with additional allocation of cache ways for each application. In order to adapt to an inclusive cache hierarchy, we assign a minimum allocation of cache space (min_ways) to all the applications before distributing the remaining capacity.

3.2.2 Bandwidth partitioning. We propose a bandwidth allocation algorithm, that partitions bandwidth proportional to the memory queuing delay experienced by each application. The pseudo-code for the proposed bandwidth allocation controller is outlined in Algorithm 1. The controller assigns a minimum bandwidth allocation (min_bandwidth_allocation) for each application in order to avoid unfairly giving a very low allocation to applications with a small


### 3.3 Coordination Mechanism

The goal of the coordination mechanism is to ensure that each local controller takes into account the decisions taken by other controllers. This is necessary to exploit the trade-offs outlined earlier in Section 2. There are two essential tasks carried out in order to establish this: i) controller prioritization and ii) inter-controller interaction.

**Controller prioritization:** Since the decision taken by one controller has the potential to influence those taken by others, it is important to establish priority among the different local controllers since that determines the order in which local controllers make allocation decisions. In CBP, the highest priority is given to the cache allocation controller, which first makes the allocation decision. The rationale is that avoiding a memory access is more effective for reducing average memory access time than lowering the memory access penalty. Next, priority is given to the bandwidth allocation controller since our characterization results show that applications are comparatively more sensitive to bandwidth than to prefetching. The least priority is given to the prefetch throttling controller. This is because it is important that the prefetcher setting is determined based on the current allocation of cache and bandwidth, since prefetching can have a negative impact on performance if the bandwidth allocation is insufficient.

**Inter-controller interaction:** Figure 7 provides an overview of the interactions that happen between different resource allocation controllers. Firstly, we describe how the bandwidth allocation controller takes decisions into account the decisions made by the cache and the prefetch controller. The bandwidth allocation controller, makes decisions based on the queuing delay of each application which is affected by the number of memory accesses. The cache allocation controller through a larger cache allocation can reduce the number of memory accesses (Interaction #1). This leads to a lower bandwidth allocation for applications that can efficiently use the cache. The prefetch throttling controller, influences bandwidth allocation decision mainly through prefetch misses (prefetched data that is not used) (Interaction #2). This is because prefetch misses lead to more memory requests and potentially a higher queuing delay. Next, we describe how the prefetch throttling controller takes account the decisions made by the other controllers. The prefetch throttling controller, makes decisions by sampling the IPC with different prefetcher settings over a specific interval. The sampled IPC values, used to determine the prefetcher setting, reflects the effect of cache and bandwidth allocation decisions made by the respective resource controllers (Interaction #3-4). Finally, we describe how the cache allocation controller is affected by the prefetch throttling controller (Interaction #5). If an application benefits from prefetching this reflects on the hit and miss count values.

![Figure 7: Interactions among the different resource allocation controllers in CBP.](image-url)
monitored in the ATDs. Since the cache allocation, is computed based on the counter values observed in the ATD, this end up affecting the subsequent cache allocation decision, resulting in a smaller cache allocation for prefetch sensitive applications.

**Putting it all together:** We discuss the timeline showing when the different resource allocation controllers are invoked and how they interact with each other, in an iterative manner, using an example illustrated in Figure 8. The three resource controllers, are invoked after a specific interval that we refer to as the reconfiguration_interval in the sequence shown in the figure. First cache and bandwidth are equally partitioned among all applications at time 0, since information about misses and queuing delay is initially unavailable, as shown in Step 0. This is followed by sampling the IPC of applications with different prefetch settings for a specific interval (twice the prefetch_sampling_period) as shown in Step 1. Based on the sampled IPCs the prefetch throttling controller determines the appropriate prefetcher setting for each prefetcher for the current reconfiguration_interval. Cache and bandwidth allocation controllers are again invoked after the reconfiguration_interval, as shown in Step 2. A cache allocation decision, for the next interval is influenced by the number of hits and misses observed in the previous interval. The ATD values will be halved after each reconfiguration, in order to be sensitive to changes in the last time interval while the per application queuing delays are accumulated with those from the previous interval. The bandwidth allocation decision shown in Step 3, is influenced both by the cache allocation and prefetcher setting in the previous interval as discussed previously. Finally, the prefetcher throttling controller shown in Step 4 is influenced by the new cache and bandwidth allocation. The interactions among the different resource allocation controllers, take place over multiple iterations, and is the key to finding an effective solution.

![Figure 8: Timing and interactions of CBP resource manager.](image)

**Table 1: Configuration of the simulated 16-core tiled CMP.**

| Cores | 16 cores, x86-64 ISA, 4GHz, OOO, Nehalem-like, 128 ROB entries, dispatch width 4 |
|-------|----------------------------------|
| L1 caches | 32KB, 8-way set-associative, split D/I, 1-cycle latency |
| L2 caches | 128KB private per-core, 8-way set-associative, inclusive, 6-cycle data and 2-cycle tag latency |
| LLC | 512KB per-tile, 16-way set-associative, inclusive, 9-cycle data and 2-cycle tag latency, LRU |
| Coherence protocol | MESI protocol, 64 B lines, in-cache directory |
| Global NoC | 5x4 mesh, 4-cycles hop latency (3-cycle pipelined routers, 1-cycle links) |
| Memory controllers | 4 MCUs, 1 channel/MCU, latency 80 ns, 16GB/s per channel |
| Prefetcher | stride-based, located in L2, 4 prefetches stop at page boundary, 8 flows/core |
| CBP parameters | reconfiguration_interval=10ms \(\text{prefetch\_sampling\_period}=0.5\text{ms}, \text{speedup\_threshold}=1.05,\) \(\text{prefetch\_interval}=10\text{ms}, \text{min\_bandwidth\_allocation}=1, \text{min\_ways}=4\)

3.4 Implementation

The computational overhead of CBP resource management is low since the design uses heuristics to guide the allocation decisions instead of exhaustively evaluating the different possible allocations.

The cache allocation controller needs hardware support in order to estimate the number of misses with different cache sizes. We use sampled ATDs [26] as discussed previously to compute the effect of different cache allocations on the misses. When enforcing cache partitioning there is an overhead associated with invalidations due to reconfiguration decisions. This is modelled faithfully by invalidating the addresses and re-fetching them when accessed, this includes the latency and impact on bandwidth from accessing memory. We have used the enforcement mechanism proposed by Holtryd et al. [12] since it is suitable for a modern tile-based CMP and is both fine-grained and locality aware. The enforcement mechanism uses per-core Cache Bank Tables (CBTs), where mappings between addresses and banks are recorded. When a request needs to access the LLC, the CBT is used to identify the cache bank that the address is mapped to. Inside each bank, way partitioning hardware divides the capacity. The enforcement results in a partition granularity of 32kB on our system, see Section 4. We incur hardware cost for implementing ATDs and cache partition enforcement [12, 26].

The bandwidth partition enforcement is done in likeness with Intel Memory Bandwidth Allocation (MBA) technology [1, 2] which is commercially available. The solution uses delays as a way to allocate the bandwidth. An application with a high delay has a low allocation, and experiences a longer queuing delay for each memory access. In our solution the addition is added after the LLC, instead of after the L2, as in the original proposal.

The overhead of prefetch-throttling comes from sampling an application with different prefetch settings. This is because deactivating prefetching for an application can be detrimental for its performance, especially when prefetching is effective. Likewise, it is detrimental to turn it on prefetching (for a sample period) for an application whose performance is hurt by prefetching.

4 EXPERIMENTAL METHODOLOGY

4.1 Simulated Architecture

We evaluate our proposal on a 16-core tiled CMP architecture modeled using the Sniper Simulator [5]. Each tile has an out-of-order (OOO) core with a private L1 data and instruction cache, a unified private L2 cache and an LLC bank of 512KB. The cache latencies assumed have been modelled using CACTI 6.5 [20]. Details about the baseline architecture are shown in Table 1. A sensitivity study is provided for the CBP parameters in Section 5.2.

4.2 Methodology

We use the entire SPEC CPU2006 suite in our evaluation. The applications are in the format of whole program pinballs [29]. We create
Table 2: 16-core workload.

14 workload mixes (each comprising 16 applications) by randomly selecting applications from the entire SPEC CPU2006 suite. Details about workload mixes are presented in Table 2.

We fast-forward for 16B instructions (in total) and then carry out detailed simulation until all benchmarks have completed at least 500M instructions. Statistics are reported based on the detailed simulation of 500M instructions. After this period the applications continue to run and compete for resources to avoid having a lighter load on long running applications. The methodology is in line with earlier works [3, 19, 28].

4.3 Metrics

We report normalized weighted speedup over baseline for each workload. This is computed by \( \frac{1}{N} \sum_{i=1}^{N} IPC_{RM, i} / IPC_{baseline, i} \), in order to evaluate system performance for multi-programmed workloads. RM refers to the system with a resource manager that manages cache, bandwidth and prefetcher settings and the baseline refers to a system with unpartitioned cache and bandwidth and without prefetching.

We also report average normalized turnaround time (ANTT) for each workload since this is a user-oriented performance metric which shows fairness. ANTT is given by \( \frac{1}{N} \sum_{i=1}^{N} CPL_{RM, i} / CPL_{baseline, i} \).

4.4 Comparison

Table 3 shows the resource managers we evaluate, in addition to CBP, and the corresponding settings they use for cache, bandwidth and prefetching. The baseline configuration represents a system with unpartitioned cache, unpartitioned bandwidth and with prefetching disabled. equal off configuration represents a system where cache and bandwidth are equally partitioned and prefetching is disabled. only cache represents the configuration where cache is partitioned as described in Section 3.2.1, while bandwidth is unpartitioned and with prefetching disabled. Likewise, only bw represents the configuration where bandwidth is partitioned as described in Section 3.2.2 while the cache is unpartitioned and with prefetching disabled. As for only pref, prefetch throttling is performed as described in Section 3.2.3 while cache and bandwidth remains unpartitioned. The resource managers that jointly manage two out of the three resources (bw+pref, bw+cache, cache+pref) in a coordinated manner can leverage a subset of the interactions described in Section 3.3. We also compare against CPf [33], a recently proposed technique for jointly managing prefetching and cache partitioning. In CPf, prefetch friendly applications are allocated small partition sizes (because the benefit from prefetching can offset the performance drop from small allocation) while the rest of the cache is allocated to the non prefetch friendly applications. In our implementation, we give minimum allocation to the prefetch friendly applications and use UCP (see Section 3.2.1), to partition the remaining capacity among the non prefetch friendly applications. We use UCP and per application partitioning, in order to not put CPf at a disadvantage in comparison to other schemes. Finally, CBP jointly manages all the three techniques dynamically.

5 EVALUATION

We first compare CBP to other resource managers that manage a subset of resources. Next, we carry out sensitivity analysis for the different design parameters, to understand its impact on the performance of CBP.

5.1 CBP Performance Analysis

Figure 9 shows normalized weighted speedup for each of the 14 workloads with the bars representing the different resource managers. We use normalized weighted speedup as a measure of performance for the entire workload. equal off improves performance in 12 of the mixes and improves performance by 10% on average over the baseline. only bw improves performance in 7 of the mixes and on average by 4% over the baseline. only pref improves performance
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for 12 workloads and provides an average improvement of 9%. only cache improves performance for all the workloads and provides an average improvement of around 28%.

Coordinated management of bandwidth partitioning and prefetch throttling (bw+pref) leads to higher performance in comparison to the baseline in 12 workloads and an average overall improvement of 10%. Coordinated management of bandwidth and cache partitioning (cache+bw) improves performance across all workloads and provides an average performance improvement of 37% (up to 64%). Coordinated cache partitioning and prefetch throttling (cache+pref) improves performance across all workloads on average by 39% (up to 57%). CPpf, cache partitioning influenced by prefetching, improves performance by 39% (up to 63%).

Among the resource managers that performs coordinated management of two resources, cache+pref and CPpf achieve the best performance. The results also show that the improvement achieved with coordinated management of two techniques, is larger than summing the improvements from individual techniques. This shows that coordinated management helps exploit synergistic interactions among the different techniques, which cannot otherwise be leveraged. Finally, CBP turns out to be the best performing coordinated resource manager in 14 of the 15 workloads and provides an average improvement of 50% (up to 86%). CBP improves performance by an additional 11% in comparison to the best performing resource manager that does coordinated management of two techniques, as well as state-of-the-art. In one workload, w3, CBP achieves slightly lower performance (2%) in comparison to cache+pref. This is because bandwidth partitioning is not very effective for this specific workload.

Figure 10 shows the average normalized turnaround time which shows the fairness of the different resource managers. Note that a lower value signifies greater fairness. On average, CBP shows 27% better fairness than the baseline and 4% better fairness than the best combination of two techniques, cache+pref. cache+pref has 4% better fairness than CPpf.

Case study: We investigate the performance of a single workload in detail to understand how CBP improves performance in comparison to resource managers that manage a subset of the techniques. Figure 11 shows the IPC for individual applications in a specific workload (w2) normalized to the baseline IPC. We have classified the applications in this workload into two groups. Group 1 comprises applications, from lbm to gcc (in the figure), for which the cache+pref resource manager performs better than the bw+cache resource manager. Group 2 comprises the rest of the applications in the workload, from soplex to namd, where the bw+cache resource manager performs better than the cache+pref resource manager. cache+pref resource manager provides the best performance for applications in group 1 because the applications are comparatively more memory intensive and get a larger share of the available bandwidth using this resource manager. Applications in group 2 benefit from bandwidth partitioning since they then get a fair bandwidth share, and in addition are not sensitive to prefetching. When we perform coordinated management of all the three resources, we would ideally prefer to have allocation decisions made by cache+pref resource manager for applications in group 1 and bw+cache resource manager for applications in group 2. With CBP, some applications in group 1 end up with a lower allocation of bandwidth (compared to cache+pref) which hurts their performance (see lbm, perlbench, cactusADM) while the rest of the applications in the group see a performance improvement from getting the right amount of the allocation. For the applications in group 2, CBP manages to match the performance of bw+cache resource manager. In summary, CBP enables better trade-offs resulting in a solution that improves overall performance for the workload and outperforms other resource managers that only manage a subset of the techniques.

5.2 Sensitivity analysis

We investigate the sensitivity of CBP to different design parameters in this section.

5.2.1 Impact of reconfiguration interval. The reconfiguration interval, determines how frequently the different resource allocation controllers are invoked when running a workload. We investigate the sensitivity of CBP to different reconfiguration interval values, in order to determine an appropriate interval. Figure 12a shows the average (geo. mean) performance when using three different reconfiguration intervals - 1ms, 10ms and 100ms. A shorter reconfiguration period has the potential to adapt faster to phase change behaviour. However, it also incurs a higher overhead because a larger fraction of the interval would be used up for IPC sampling (required for prefetch throttling). Overall, the results show that using a 10ms period provides a good trade-off between quick adaptation and the overhead incurred for IPC sampling.

5.2.2 Impact of cache size. The results thus far assume that each tile has a baseline cache allocation of 512kB. The total LLC capacity assuming a 16-core tiled CMP would be 8MB. We next study the
The design is motivated by our in-depth characterisation of the performance impact of cache, bandwidth and prefetch allocation among multiple resources. For instance, CLITE [25] uses bayesian optimization to provide theoretically-grounded resource partitioning to meet QoS targets of multiple resources (e.g., cores, caches, memory bandwidth, memory capacity, disk bandwidth etc.) among multiple co-located jobs. Bitirgen et al. [4] use machine learning to manage power, cache and bandwidth in a coordinated way to anticipate system-level performance impact of allocation decisions. However, in neither of these works is prefetch throttling considered, which we have shown is important in order to realise the full potential of coordinated resource management. To the best of our knowledge, CBP is the first coordinated resource manager for cache partitioning, bandwidth partitioning and prefetch throttling.

7 CONCLUSIONS

We present CBP, a mechanism for coordinated management of cache partitioning, bandwidth partitioning and prefetch throttling. The design is motivated by our in-depth characterisation of the performance impact of cache, bandwidth and prefetch allocation and their interactions. CBP combines local resource allocation controllers with a coordination mechanism that dynamically manages and allocates the resources, in a way which considers both intra- and intra-application interactions. Our evaluation, on a tiled 16-core CMP, demonstrates that CBP improves performance by up to 86% (geo. mean 50%) compared to a system without partitioning and prefetching and by up to 36% (geo. mean 11%) over the state-of-the-art technique that manages cache partitioning and prefetching in a coordinated manner.

Figure 12: Sensitivity analysis.

Impact of changing the cache capacity available for a single tile to 1MB. Figure 12b shows the average performance achieved using CBP with different per-tile capacity normalized to the baseline configuration with the same capacity. The results show that increasing the available LLC capacity leads to a 5% drop in aggregate performance with CBP. This performance drop can be attributed to an increase in cache access time for the larger cache.

5.2.3 Impact of changing bandwidth partitioning parameters. We investigate the sensitivity to the minimum bandwidth allocation, used in the bandwidth allocation algorithm presented in Section 3.2.2. Figure 12c shows the difference in performance with a minimum bandwidth allocation of 0.5GB/s and 1GB/s, normalized to the baseline. There were small variations among the different workloads and some experience a slight improvement while others workloads experience a small drop in performance. Overall, reducing the minimum bandwidth allocation did not have a considerable impact on the performance of CBP as long as it is sufficient for workloads which experience very little queuing delay.

5.2.4 Impact of changing prefetch sampling interval. We finally investigate the impact of changing the prefetch_sampling_period used in the prefetch throttling controller 3.2.3. Figure 12d shows the impact of changing the sampling period on performance normalised to the baseline. The intervals we use for evaluation are 0.25ms, 0.5ms and 1ms. The advantage of using a shorter sampling period is that it carries a lower overhead, while the drawback is the risk of over/under estimating the performance benefit from prefetching. The results indicate the sampling interval of 0.5ms achieves the best performance.

6 RELATED WORK

Isolated Management: Several techniques have been proposed in the literature that focus specifically on cache partitioning, bandwidth partitioning and prefetch throttling. Cache partitioning techniques [10, 15, 19, 26, 28] help improve performance and achieve better utilization of available cache resources, by avoiding interference among co-running applications and reducing the number of accesses to memory. Bandwidth partitioning techniques [13, 17, 24, 32], reduce average memory access penalty, by dynamically determining how bandwidth must be shared among the co-running applications. Prefetching can hide memory access latency by fetching the data before it is requested [6, 7, 14, 16, 21, 22]. However, inaccurate prefetches can impact application performance since it can increase the number and cost of demand misses [9]. Prefetch throttling [6, 30], involves adaptively tuning when and what prefetcher settings are used dynamically based on application characteristics and has been shown to provide better performance and address drawbacks of prefetching. The aforementioned works, consider each of the techniques in isolation and leaves room for improvement, as shown in this work, since they do not take the interaction between cache partitioning, bandwidth partitioning and prefetch throttling into account.

Coordinated Management: Several works have proposed combining two of the techniques in order to exploit the benefits from coordination. These works can be broadly classified into the following groups: i) coordinated cache and bandwidth partitioning [23, 27], ii) coordinated prefetching and cache partitioning [31, 33], and iii) coordinated bandwidth partitioning and prefetching [18]. Sahu et al. propose [27] a method for cache and bandwidth partitioning, using a CPI model for bandwidth and set partitioning for the cache. CoPart [23] combines bandwidth and cache partitioning using a user-level run-time. Unlike CBP, their goal is to improve fairness. Recently, CPpf [33] and Sun et al. [31] propose a coordinated approach for cache partitioning and prefetch where prefetch friendly applications where given a smaller cache allocation. Unlike CBP which maintains per-application partitions, cache partitioning in these two proposals is performed for groups of applications. Ebrahimi et al. [8] propose general mechanisms to make memory scheduling techniques prefetch aware. However, these works cannot use the additional interactions and trade-offs which are available when coordinately managing all three resources, which we have shown is important for performance.

Some works have also proposed coordinated management of multiple resources. For instance, CLITE [25] uses bayesian optimization to provide theoretically-grounded resource partitioning to meet QoS targets of multiple resources (e.g., cores, caches, memory bandwidth, memory capacity, disk bandwidth etc.) among multiple co-located jobs. Bitirgen et al. [4] use machine learning to manage power, cache and bandwidth in a coordinated way to anticipate system-level performance impact of allocation decisions. However, in neither of these works is prefetch throttling considered, which we have shown is important in order to realise the full potential of coordinated resource management. To the best of our knowledge, CBP is the first coordinated resource manager for cache partitioning, bandwidth partitioning and prefetch throttling.
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