PV based high level hybrid multilevel inverter

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Abstract - This paper presents a PV based high level hybrid multilevel inverter. SEPIC converter is the technologically advanced converter derived from the buck-boost converter. The proposed scheme is used in the SEPIC-converter to eradicate the output ripples and well enhance the output voltage level. Cascaded H Bridge and Neutral point clamped (NPC) inverter topologies are combined to obtain 127 level of output voltage using reduced number of switches and DC sources. To increasing the voltage level, Total Harmonic Distortion (THD) can be reduced and hence reduction in size of the filter. Simulation work is done using MATLAB and then to verify the performance of suggested scheme.

Keywords - SEPIC converter, Hybrid multilevel inverter, Cascaded H Bridge & NPC inverters, Total Harmonic Distortion.

1. INTRODUCTION

The constraint of conservative energy system and environmental problems equivalent to heating and pollution is prompting the planet toward the improvement of renewable energy sources. The electrical occurrence of Photovoltaic (PV) plays a very significant part in power generation among more outdated earliest energy sources corresponding to oil, coal, nuclear, hydro and wind [1]. PV array power directly feed into small loads equal to lighting systems and DC motors. Further sophisticated application required electronic converters to electricity from the PV array. These converters are used to normalize the output voltage and current in the load, to control the power flow in grid-connected systems and maximum power point tracking (MPPT) is used to obtain maximum power in the PV array panel. Converters with maximum power point tracking technique are used to detect the continuous maximum instantaneous power of the PV array. The results of suggested scheme is operating in different environment conditions of the PV array with slight modification. The entire operation of the system an MPPT procedure is required to obtain the maximum instantaneous power can be extracted and delivered to the load.

Over the few past decades, completely different MPPT techniques are implemented and proposed [2] PV system is used to track the maximum instantaneous power from arrays. The systems vary in sensors needed, complexity, cost, convergence speed, vary of effectiveness, implementation of hardware, popularity, and in other respects. The best MPPT technique is analyzed in [2], [3] and [4] in Perturb and Observe (P&O) methodology. The output of PV panel obtained from DC voltage with contains high voltage ripples and it is not constant. DC-DC converters are engaged to reduce the
ripples not withstanding alteration in load voltage. The traditional device doesn’t meet the load demand containing a lot of ripples in the output voltage and parasitic effects. To beat this drawback in advanced developed DC-DC SEPIC device was used [5]. SEPIC device is the established from buck-boost converter, that performs buck or boost operation [6], [7]. Sepic converters have some important characteristics such as high power density, high voltage transfer gain, and reduced ripple in output voltage and current in the PV array. Its further filter parts may be accustomed to eradicate the ripples in output voltage and effectively increase the output voltage level. It also overcomes the parasitic effects in the classical dc-dc device. The various electrical converter topologies for interfacing electrical phenomenon modules to the grid is bestowed in [8] that involves two major tasks. First one is used to insert a curving current into the grid and second one is used to see the PV module(s) operation at the MPP, is used to detect the operating condition and anywhere most of the energy is captured. This is often circulated by mistreatment MPP tracker. So as to attain a utilization magnitude ratio of 98% and the amplitude of the ripple voltage should be less than the 8.5% [8]. To interface the PV module(s) with the grid connected systems should maintain some standards in the electrical converter topologies. Nowadays Multi level inverter (MLI) technologies has been achieved its extensive recognition within the space of high power medium voltage energy management. It includes associate with nurturing an array of power semiconductors and DC voltage sources, the output of that generate voltages with stepped waveforms. Compared with a two-level voltage source inverter (VSI), the structure of VSI will turn out a lot of ranges in the voltage levels within the output voltage [9]. Hence, by increasing the quantity of levels in the MLI, the output voltage has more number of steps required in generating a wave with shape that includes and reduced total harmonic distortion (THD). The Diode clamped, Flying capacitor and Cascaded H-bridge inverter are the three main multilevel inverter structures that area unit employed in industrial applications with separate dc sources. In flying capacitor and diode-clamped inverter there is a problem of capacitor voltage balancing and this problem is overcome in cascaded H-bridge inverter. But in the cascaded H-bridge inverter, separate dc sources area unit required for every H-bridge. It will lead to higher range of dc input sources [10]-[12]. So as to boost power quality and scale back EMI issue, it is needed to extend the number of levels [13]. The range of the amount the quantity of switches becomes too high with higher number of voltage levels if all the DC busses area unit at same voltage; this conjointly will increases the number of gate drivers and better physical phenomenon of conduction loss of devices. All on top of issue can have negative impact on price, reliability (reliability is inversely proportional to number of components) and efficiency. The asymmetric structure of multilevel inverter can increase the number of levels without dramatic increase in number of switches [14]. So, to beat the top of mentioned the issue two structure of multilevel inverter topologies are mixed to get higher range of output voltage level by mistreatment lesser number of switches and sources [15], [16]. During this planed system in Cascaded H-Bridge & Neutral Point Clamp topologies are hybridized to form this topology. Increasing the number of voltage levels provides a lot of flexibility to scale back Total Harmonic Distortion (THD) of the system and successively reduction in cost and size of the power filter.

2. PROPOSED TOPOLOGY DESCRIPTION
In this suggested scheme the electrical phenomenon of photovoltaic (PV) is used as a DC supply. The DC-DC Sepic converter provides a constant DC source and additionally went to eliminate or reduce the output voltage and current ripples. Here, to induce a most power from the panel, to come up with a change pulse for the converter switches the MPPT with management unit is employed. A usual electrical converters only having 30 to 40 percentage of occurrence in irradiation into voltage. The most of the power from PV panels and they have to operate at their maximum power point (MPP). That’s why the controllers of all solar energy in electronic converters use some technique for maximum power point tracking (MPPT). There was a different MPPT techniques [1] are available. The Figure.1 shows the block diagram of suggested scheme.
Among the various techniques in maximum power point tracking (MPPT). In our suggested system use the process is Perturb & Observe (P&O) method. It’s the simplest and most commonly used method. In this process, the sign of the last perturbation and increment in the power are used to decide what the next perturbation should be. If there is an increment in the power, the perturbation operate should be in the same direction and if the power decreases, then the next perturbation should be in the opposite direction. Based on these facts, the algorithm is implemented. The process is repeated until the MPP is reached [4].

21. Converter circuit operation
The DC-DC change in technology is mainly used in the field of power electronics and drives. These converters are mainly used in industrial applications and computer hardware circuits. The proposed DC-DC SEPIC topology provides stable and ripple free output voltage and current [8]. DC voltage obtained from the PV panel contains high voltage ripples and it’s not constant. The traditional convertor doesn’t meet the load demand containing additional ripples on the output voltage and parasitic effects.

![Block diagram of suggested system](image1)

**Figure.1.** Block diagram of suggested system

![SEPIC converter circuit operations](image2)

**Figure.2.** SEPIC converter circuit operations
In Figure 2(b) when the switch is ON the inductor L1 and L2 gets charging in reverse flow, in that time there is no output across the load R. In Figure 2(c) when the switch is in OFF position the same current of L1 the L2 will continuous in negative direction. However the L1 being charged during the OFF cycle and L2 being discharged during the ON cycle.

2.2 Multi-level Inverter circuit operations

It has a more number of advantages it has drawbacks in the manner of higher levels because of using more number of semiconductor switches and isolated DC sources. This may leads to vast size and price of the inverter is very high. In order to overcome this problem the new multilevel inverter topology is proposed with reduced number of switches and sources. As a result it is possible to reduce or even to eliminate output ripples. The unified analysis and design consideration for hybrid multilevel inverter has been proposed in [15]. In this proposed system the Cascaded H-Bridge & Neutral Point Clamp topologies are hybridized.

In Figure 3(a) when the switch SW6 is turned ON the current flow will be in the direction of VS6 (+) – SW6-D5- D4- D3- D2- D1- SW7- RL Load (+)- RL Load (-) SW10- VS6 (-). During this time the diode D6 will not conduct. The output voltage and current will be positive. The switches in the H-Bridge SW7 and SW10 are turned ON for the operation of inverter in the positive half cycle. The inverter operation for the first level in negative cycle is shown in fig.3 (b), when the switch SW5 is turned ON the current flow will be in the direction of VS5 (+)-SW5-D4-D3-D2-D1-SW8-RL Load (-) -RL Load (+)-SW7-VS5 (-). The output voltage and current will be negative. The switches SW8 and
SW9 in the H Bridge are turned ON for the operation of inverter in the negative half cycle. Similarly the remaining level is obtained by alternatively ON and OFF of the switches as per the switching states given in the following table. The switching state is given for the 63 level of positive half cycle only. It will be same for the negative cycle but the difference is, when the switches SW7 and SW10 are conducting the inverter output voltage and current will be in positive half cycle, when the switches SW8 and SW9 are conducting the inverter output voltage and current will be in the negative half cycle.

Table 1 Switching States

| Level | Neutral point clamped inverter(NPC) | Cascaded H-bridge inverter(CHB) |
|-------|-------------------------------------|----------------------------------|
|       | S1  S2  S3  S4  S5  S6            | S7  S8  S9  S10                 |
| 1     | 0     0     0     0     0     1  | 1     0     0     1            |
| 2     | 0     0     0     0     0     0  | 1     0     0     1            |
| 3     | 0     0     0     0     1     1  | 1     0     0     1            |
| 4     | 0     0     0     1     0     0  | 1     0     0     1            |
| 5     | 0     0     0     1     0     1  | 1     0     0     1            |
| 6     | 0     0     0     1     1     0  | 1     0     0     1            |
| 7     | 0     0     0     1     1     1  | 1     0     0     1            |
| 8     | 0     0     1     0     0     0  | 1     0     0     1            |
| 9     | 0     0     1     0     0     1  | 1     0     0     1            |
| 10    | 0     0     1     0     1     0  | 1     0     0     1            |
| 11    | 0     0     1     0     1     1  | 1     0     0     1            |
| 12    | 0     0     1     1     0     0  | 1     0     0     1            |
| 13    | 0     0     1     1     0     1  | 1     0     0     1            |
| 14    | 0     0     1     1     1     0  | 1     0     0     1            |
| 15    | 0     0     1     1     1     1  | 1     0     0     1            |
| 16    | 0     1     0     0     0     0  | 1     0     0     1            |
| 17    | 0     1     0     0     0     1  | 1     0     0     1            |
| 18    | 0     1     0     0     1     0  | 1     0     0     1            |
| 19    | 0     1     0     0     1     1  | 1     0     0     1            |
The parameter and its values which is used in simulation is given below in table 2.

**Table 2** Values used in Simulation

| S. No | Parameters                  | Values used in simulation |
|-------|-----------------------------|---------------------------|
| 1     | DC input voltage            | 19.1 V                    |
| 2     | Inverter output voltage     | 230 V                     |
| 3     | Total number of switches    | 11                        |
| 4     | Inductance (L1, L2)         | 45µH, 1.5mH               |
In this proposed system the SEPIC converter boost up the input DC voltage to 230V and it can be splitted into six input sources for the inverter switches by using multiple output DC/DC converter. The ripples in the output can be eliminated by using filter elements (L2 & C2). By alternatively turning ON and OFF of the inverter switches (SW1-SW6) the 127 level of output voltage is obtained and it is converter into AC by means of CHB switches (SW7-SW8) which perform the operation of conventional inverter.

3. SIMULATION RESULTS

| 5 | Capacitance (C1, C2) | 20µF, 100µF |
|---|---------------------|-------------|
| 6 | Number of level     | 127         |

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3. SIMULATION RESULTS

**Figure 4.** Simulation circuit for proposed system

(a)
The Figure 5(a) shows the output voltage waveform for solar panel. The voltage magnitude is about 19.1 V. This voltage is not constant enough. To converter this voltage into constant DC this will be send into DC-DC SEPIC converter. The fig 5(b) shows the output current waveform for solar panel. The current magnitude is around 15 A.

The Figure 6(a) shows the output voltage waveform for proposed Hybrid multi-level inverter. The output voltage having 127 level. Hence THD can be reduced by using proposed inverter topology.

**4. CONCLUSION**

This paper presents a PV based hybrid multilevel inverter. During this planned DC-DC sepic converter the extra filter parts eliminate the output ripples and effectively enhance the output voltage level. It overcomes the parasitic problems present in the classical dc-dc device. The 127 level of output voltage is obtained by using proposed Hybrid multilevel inverter topology. Hence the THD is reduced. The presented concepts have been verified in simulations and validated experimentally.

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