A 8-Bit, 1-GHz Coarse-Fine Time-Based ADC with Split-CDAC Residue Transfer

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1. Introduction

With the scale of CMOS technology, the performance of digital circuits improved dramatically [1, 2]. However, analog circuits suffer from Signal Noise Ratio (SNR) reduction due to the decrease of supply voltage. Time-domain signal exhibiting the advantage in SNR has received more attention, because the amplitude is unrelated to the supply voltage [3, 4, 5, 6, 7]. With the shrinking of the process, the delay time is decreased, which make the speed of TBADC faster [8, 9, 10].

The TBADC is a flash architecture, which makes the operation speed rapidly decrease as the resolution increases [11, 12, 13]. To overcome this problem, a hybrid voltage-time two-step analog-to-digital converter (ADC) is proposed [14]. The two time-based converters are pipelined with residue amplifier (RA) in the ADC lead to a high-speed. However, to achieve the required accuracy and bandwidth, the RA needs more power consumption [15, 16, 17, 18, 19, 20]. This Letter presents a coarse-fine TBADC with fully time-domain quantization. The coarse and fine stages are pipelined in a fully passive way, which make the design have a better power efficiency and the residue is non-attenuated compared with the conventional passive charge sharing.

2. ADC architecture and implementation

2.1 Proposed TBADC with split-CDAC residue transfer

The proposed TBADC architecture is shown in Fig.1. The resolution of the proposed TBADC is 8-bit, which allocates 4-bit in coarse stage and 5-bit in fine stage. There is one bit redundancy to make a tolerance of gain and offset mismatch between the coarse and fine stages [23]. The coarse stage contains a coarse voltage-to-time converter (CVTC) and a 4-bit TDC. The fine stage contains a capacitive digital-to-analog converter (CDAC) serve as the residue transfer, a fine VTC (FVTC) and a 5-bit TDC. During the sampling phase, the input signals are sampled by the CVTC and CDAC. Afterward, the four most significant bits (MSBs) are generated through the coarse TBADC and then they are fed back to the CDAC to generate the residual signal (Vresp and Vresn) at the top-plate of CDAC. Before the next sampling phase, the CDAC is split and a capacitor of CDAC is moved to the FVTC to transfer the residue. The residue is quantized by fine TBADC to generate the five least significant bit (LSB).

For the capacitor which is shared with CDAC and FVTC, implements two sampling operations in a conversion cycle. It first samples the input signals as CVTC after that samples the residue as FVTC. Its kT/C noise is different from the conventional sampling operation that is only dominant by the capacitor of second stage [24, 25]. To satisfy the requirements of kT/C noise and mismatching, the capacitor of FVTC is chosen to be 16F which is sufficient for kT/C noise. The binary CDAC is 8:4:2:1:1 and needs a capacitor to serve for residue transfer. In order to minimize the total capacitor to improve the conversion rate, the MSB capacitor 8C is chosen to share with the FVTC. Therefore, the total capacitor is 32fF, where the unit capacitor is 2fF. While the fine stage implements the quantization, the rest of capacitor is idle. Therefore, the FVTC is divided into FVTC_a and FVTC_b to implement the sampling operation with the rest of capacitor respectively. With the use of ping-pong operation, the speed can be further increased.

2.2 Proposed high linearity dynamic CVTC

The CVTC in the proposed TBADC samples the input signals. Therefore, it requires a wide input range to alleviate the requirements of noise in fine stage. Fig.2 is the proposed high linearity dynamic CVTC. It is composed of a bottom-plate sampling circuit, a charge path IP and a threshold cross detector (TCD) circuit. The capacitor samples the input sig-
nal by bottom-plate sampling to strengthen the sampling linearity and then is charged by the transistor M1. Once the voltage of capacitor cross the threshold of TCD, the CVTC generate the time signals $T_P$ and $T_n$. The gain of the CVTC is determined by the charging current and capacitor. Therefore, the conversion is linear if the charging current is a constant-current. In order to ensure its linearity, an appropriate threshold voltage must be selected to make the transistor M1 does not operate in the linear region. Simulation reveals a non-linearity which is less than $\pm 1/2$ LSB with a input range of $1.2V_{pp}$. For a suitable gain of the VTC, the charging current is relatively small which make the input of the TCD is always around the threshold voltage. This causes the inverter to consume extra power. The proposed CVTC add a transistor M2 to help charging the capacitor when the conversion is completed, which reduce the excess power consumption.

Due to the process, voltage and temperature variation, the gain error and offset between VTC and TDC should be considered. There is one bit redundancy to tolerate the gain error and offset less than $1/2$ LSB. In order to leave a large tolerance range, the gain error and offset is foreground calibrated. In the VTC, offset can be equivalent as an input-referred offset $\Delta V_{th}$ between the two threshold voltage. To calibrate the gain error and offset, a mismatch current which can be adjusted by the gate voltage $VG$ of the transistor M1 is used. The time difference $T_D$ can be expressed by Eq. (1).

$$ T_D = \alpha (V_P - V_N) + \beta \quad (1) $$

$$ \alpha = \frac{C_S (ID + 1/2ID_D)}{ID (ID + \Delta ID)}, \quad \beta = \frac{C_S [\Delta ID (V_{cm} - V_{th}) + ID \Delta V_{th}]}{ID (ID + \Delta ID)} \quad (2) $$

According to Eq. (2), offset can be removed by setting the $\beta$ to zero and the gain also can be adjusted by $\alpha$. The linearity of time-domain quantization is determined not only by VTC but also by TDC. The simulation with parasitic effect in TDC reveals the random mismatch between each delay cell is normally less than 1.7% which is sufficient for the TDC.

3. Simulation result

This design is based on a 65-nm CMOS technology. Fig. 3(a) summarizes the simulated SNDR and SFDR with transient noise for various input frequencies at a sampling frequency of 1 GHz. A fast Fourier transform (FFT) was performed using the 512-point ADC output. The power spectra of Nyquist frequency at a sampling frequency of 1 GHz are shown in Fig. 3(b). The SNDR and SFDR with transient noise were 47.5 and 55.8 dB, respectively. The input range is 1.2 Vpp which is benefit from the high linearity VTC.

The performance comparison with other related 8-bit 900 MS/s to 1.2 GS/s two-stage ADCs is listed in Table I. With the passive split-CDAC residue transfer, the proposed coarse-fine TBADC consumed 3.1 mW at 1 GS/s, and the supply voltage was 1.2 V. The Nyquist-frequency FOMW at a sampling frequency of 1 GHz is 15.9 fJ/conversion step.

![Fig. 1. Schematic and timing diagram of 8-bit coarse-fine TBADC.](image)

![Fig. 2. Schematic and timing diagram of the proposed CVTC.](image)

![Fig. 3. (a) SNDR and SFDR at 1 GS/s with transient noise versus input frequency (b) Spectra of a near-Nyquist input with transient noise.](image)

| Reference | Technology | Residue Transfer | Supply voltage (V) | Resolution (bit) | Sampling Rate (MHz) | SNDR (dB) | SFDR (dB) | Power (mW) | FOM (fJ/conv) |
|-----------|------------|-----------------|-------------------|-----------------|-------------------|----------|----------|-----------|--------------|
| [15]      | 65 nm      | CSA             | 1.0               | 8               | 1000              | 44.4     | 47.5     | 2.3       | 18.7         |
| [24]      | 65 nm      | CSA             | 1.25              | 8               | 1200              | 43.7     | 55.8     | 5.0       | 35           |
| [27]      | 65 nm      | CSA             | 1.0               | 8               | 900               | 41.9     | 49.5     | 3.9       | 37           |
| This work | 65 nm      | Passive         | 1.2               | 8               | 1000              | 47.5     | 55.8     | 2.3       | 15.9         |

4. Conclusion

A coarse-fine TBADC with split-CDAC residue transfer is proposed. The TBADC has a better power efficiency because the residue is transferred in a passive way. A high linearity
VTC is used to acquire a wide input range. The SNDR and SFDR are 47.5 and 55.8 dB and consume 3.1 mW at 1 GHz. Its FOMWs is 15.9 fJ/conversion step.

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