Abstract—Recent breakthroughs in machine learning (ML) have sparked hardware innovation for efficient execution of these emerging ML workloads. Separately, due to recent refinements and high-performance implementations, well-established gradient boosting decision tree models (e.g., XGBoost) have demonstrated their dominance in many real-world applications. Beyond its rich theoretical foundations, gradient boosting is prevalent in commercial-real applications. For instance, XGBoost alone is used by over 3200 companies, including eBay, Capital One, and Nvidia. Facebook [31] and Bing [41] have used GB to predict advertisement clicks, a key revenue source. In Kaggle 2020 public solutions, GB is used in 4 out of 18 winners as opposed to neural networks (NNs) in 11. While numerous accelerator proposals (e.g., [4], [5], [13], [14], [26], [35], [48]) exist for NNs, the most popular ML method, only a few exist for GB, the second-most popular method (Section II-E). Anecdotally, a google search of GB reveals its indisputable importance for tabular data. In addition to its empirical success, GB’s rich theoretical foundation gives confidence in the method [53].

The core idea of boosting is to combine many simple or weak models (i.e. low-accuracy models) to form a strong model (i.e., a highly-accurate model). Unlike DNNs, where the parameters of the model are trained via gradient descent, GB [22] refines an aggregate function (the strong model) by taking approximate gradient steps in the function space (by incrementally adding weak models).

Traditionally, the computational bottleneck has been the determination of the next best decision point to grow the current tree. In the exact tree algorithm, all possible decision points along all possible fields must be considered, which naively costs $O(nd)$ where $n$ is the number of instances and $d$ is the number of fields (assuming the field values are already sorted). A common method to avoid this high computational cost is by replacing the fields with discretized values via histograms that approximate the points—effectively reducing the number of possible decision points from $n$ to the number of histogram bins $k$, where $k \ll n$ [12], [36], [37]. These histogram-based methods have been shown empirically to be much faster with only a slight loss of accuracy [36], [37].

While training GB models is time-consuming (e.g., a few to several hours on datasets with hundreds of millions to billions of records), a single input record inference is fairly lightweight (e.g., a few microseconds on a multicore) amounting to traversing a few hundred shallow regression trees (e.g., 500, 6-deep trees). Further, increasing the accuracy typically requires more training data which in turn requires larger models (more trees) to avoid over-fitting. Both more training data and larger...
models lead to longer training times. As such, we propose an accelerator for GB targeting, for instance, (a) datacenters that offer training as a service, and (b) batch inference (e.g., offline analytics). Specifically targeting DNN training, the TPU V2 and V3 extend the TPU by adding floating-point support and a high-bandwidth network, and Nvidia’s DGX includes a high-bandwidth switch (NVSwitch). Thus, providing hardware support solely for time-consuming training, though offline, is common. The GB training algorithm grows the model one decision tree at a time; and grows each tree by starting with its root and splitting nodes to form a tree. The training time for GB models is dominated by three key steps – histogram binning of records’ gradient statistics, single-predicate evaluation, and evaluating a record on a single tree. Section II expands on the training algorithm, including the above listed steps. Each of these steps operates (repeatedly) on millions of records in the training set. As such, we target these steps for acceleration. There is one other step – evaluating histogram bins to identify a split point – that is algorithmically significant for training, but operates on smaller datastructures (e.g., 1000s of histogram bins, instead of millions of records) and hence, accounts for a smaller fraction of total training time (e.g., 2%-10%). Because this step is short, and further because the step involves formulae that are subject to change (based on loss function, for example), we offload it to the host CPU.

The training algorithm has enormous parallelism, across both the fields of an input record (e.g., 100 fields expanded to some 4000 features due to one-hot encoding of categorical data, as explained in Section II) and different input records (e.g., 200 million). However, an input record may fall into different histogram bins for different fields (e.g., bin 20 for field 1 and bin 38 for field 2) and the input records may fall into different histogram bins for a field, imposing significant irregularity in histogram access. On the positive side, the data structures (e.g., histograms and decision trees) are small enough to fit on-chip (e.g., under 2 MB). While all the records are binned at the root, the other vertices receive only a subset of the records, filtered by the predicates in the path from the root to a given vertex. This subsetting makes the input record accesses in the binning and single-predicate evaluation irregular. Further, the single-predicate evaluation and the one-tree traversal use only one field and a subset of fields of a record, respectively, potentially wasting memory bandwidth on the unused fields. Similarly, batch inference has parallelism across the decision trees traversed by each record and across different records. Batch inference is also irregular in that the records may take different paths through a tree and, of course, different trees’ predicates are different from each other. Thus, irrespective of training or batch inference, GB has enormous fine-grain, irregular access parallelism where the compute work is mostly accessing histogram bins or decision tree vertices. This data access parallelism is in sharp contrast to the multiply-accumulate parallelism of DNNs [35].

While CPUs can handle irregularity, their parallelism is limited (e.g., 64 threads in a 32-core multicore). GPUs, on the other hand, can exploit immense parallelism but face difficulty with irregularity. While the GPU Shared Memory can accommodate some irregularity, its limited capacity amounts to either almost entirely turning off multithreading or incurring considerable underutilization (e.g., over 90% idle GPU lanes), as we discuss in Section II. Clearly, DNN accelerators, such as the TPU, are a mismatch for GB.

Based on the above workload characteristics, we propose an accelerator for GB, called Booster, which makes the following contributions:

- To match the fine-grained, irregular parallelism in accessing many small data structures, we propose a scalable sea-of-small-SRAMs architecture. The SRAMs hold the histograms (for training) or the decision trees (for training or for batch inference), as appropriate. Each SRAM has an associated floating-point unit to perform some computation. The number of SRAMs determines the available degree of parallelism required to match the memory bandwidth – across the fields of a record and across the input records (e.g., scale to 3200 SRAMs processing 64 fields per record and 50 records in parallel).
- Naively mapping one-hot encoded features to SRAMs (by packing the histogram bins into SRAMs, for example) would result in idle SRAMs as a given record would have only one active feature out of all the one-hot encoded features corresponding to a categorical field. Further, for accurate binning, the training algorithm bins the records with missing fields in a default histogram bin for each such field. Thus, while the one-hot encoded features appear to be sparse, the higher-level fields are dense where every record has every field exactly once. We exploit this observation to map a high-level field – i.e., all the corresponding one-hot encoded features including the bin for absence – to an SRAM, achieving full SRAM bandwidth utilization (exactly one access per SRAM). Though dense and parallel, the accesses remain irregular, rendering GPUs ineffective and CPUs insufficient.
- Finally, to save memory bandwidth in single-predicate evaluation and one-tree traversal in training, we employ a per-field column-major format for the input records, in addition to the natural per-record row-major format. Column-major format is well-known, our novelty is the redundancy. The input records already undergo offline pre-processing in software. The redundant format adds a little to the pre-processing time which is amortized over as many scans of the input data as the trees built by training.

We evaluate Booster via simulations, and an ASIC synthesis. Our simulations reveal that Booster achieves 11.4x speedup and 6.4x speedup over an ideal 32-core multicore and an ideal GPU, respectively. Based on ASIC synthesis of FPGA-validated RTL using 45 nm technology, we estimate a Booster chip to occupy 60 mm$^2$ of area and dissipate 23 W of power when operating at 1-GHz clock speed.
II. GRADIENT BOOSTING TREES

Our description is based on state-of-the-art implementations of gradient boosting (GB) (e.g., [12], [12], [19], [36]). We summarize GB with a focus on (1) offering high-level intuition that is relevant to Booster’s design; we do not aim to describe all of GB’s details.

A. GB: Model and Training

The tree ensemble models used by GB have the following characteristics:

- The ensemble has \( K \) trees with decision rules in the interior nodes and weights \( (w) \) associated with the leaves.
- The model operates on table-based datasets. Each row of the table corresponds to a record and each column corresponds to a field.
- There are \( n \) training records, with known “golden” outputs; The \( i^{th} \) record has a known output value of \( y_i \).
- Prediction/inference involves passing a record through all the individual trees to generate a weak prediction per tree (the \( w \) associated with the leaf) which can then be combined for the final prediction \( \hat{y}_i \), which is the strong prediction. Figure 1 shows a simple tree ensemble model with \( K = 2 \) trees. It illustrates the computation of the strong prediction for the red and blue customer records.
- GB is agnostic about the loss function as long as the loss function \( L(\hat{y}_i, y_i) \) is differentiable and convex. In addition to the loss function, the objective function (that GB minimizes during training) includes terms for penalizing tree complexity and for weight regularization.

The GB training algorithm arrives at the final \( K \)-tree model by incrementally growing the ensemble one tree at a time. Each tree is in turn grown by splitting leaf vertices, one leaf at a time as shown in Table 1. At a high level, GB training determines the split points of a leaf based on the distribution of first- and second-order gradient statistics \( (g_i \) and \( h_i \)) of the training records. We expand on this process to identify the key computational tasks.

We use the example shown in Figure 2 which defines the fields of a fictional airline’s frequent-flier database; the same database used earlier in Figure 1. (Only the field definitions are shown here; the data is not shown in Figure 2.) The fields include categorical data (fields 1 and 2 shown in blue and amber, respectively, in Figure 2) as well as numerical fields (field 3 in green). For simplicity, we first show a logical view of the computation. The real implementation optimizes and eliminates some of the operations where possible. In preparation for training, the input records are (pre-)processed in software (1) to discretize floating-point fields into some number of bins (e.g., 256 bins, including one bin for records with a missing field), (2) to one-hot encode categorical fields (i.e., the 3-category field 1 is expanded into three mutually-exclusive ‘yes-no’ binary features, where each binary feature has two bins), and (3) to include an ‘absent’ bin for each categorical field; not all records have values in all the categorical fields. For high inference accuracy, the algorithm accounts for missing features using the absent bins. Naive one-hot encoding increases the size of each record resulting in much higher memory bandwidth demand (e.g., 40 original fields expand to 200 features). However, a key pre-processing optimization ensures that only one bin per field sees a gradient statistic update by effectively counting only the ‘yes’ features and reconstructing the ‘no’ features by subtracting from the overall gradient statistic summation [36]. Similarly, the ‘absent’ bin can also be elided. We incorporate this optimization into our GB baseline.

The histogram-binning of the relevant records in Step 1 (Table 1) add a given record’s gradient statistics \( (g_i \) and \( h_i \)) to the bin’s summation \( (G \) and \( H \)) respectively. Step 2 identifies the feature and bin within the feature that should be used as the split point for the children of the current leaf. To do so, this step evaluates every bin of every feature as a potential split point. For a given feature, the algorithm considers the bins in left to right order and starts with the split point to the left of all the bins so that the left cumulative count is zero and the right cumulative count is all the records reaching the leaf. The algorithm then successively moves the split point right by one bin and adds that bin’s count, \( G \) and \( H \) to the left cumulative bucket and subtracts the bin’s quantities from right cumulative bucket. Figure 3 illustrates the summation...
of the gradient statistics to the left and right of the split-point under consideration – the upper bin boundary of the \(p^{th}\) bin. (Though not shown, GB considers placing records with missing fields in both the left and the right sub-trees to pick the best split option.) The quality of this split is evaluated based on the left and right cumulative buckets. The algorithm greedily picks the best split point across all fields and split points. We note that the function to evaluate the quality of a split is often complex (i.e., hardware-unfriendly) and may vary across implementations. It is possible that the algorithm may choose not to create any children for the current leaf if the loss improvement is exceeded by the complexity cost associated with the children (larger trees have higher complexity cost).

Step 3 in Table I applies the newly-chosen predicate (corresponding to the split-point) to partition the relevant records (i.e., those that reach the current leaf after being filtered by the predicates in the path from the root to the leaf). The records are partitioned into predicate-true and predicate-false subsets which are used later as the relevant records for exploring the next vertices on the corresponding paths. The subsets are stored in memory. An optimization in Step 1 is that the histogram-binning can be performed only for the child vertex with the smaller subset and the other child vertex’s (with the larger subset) bin counts, bin \(G\) and \(H\) can be calculated by simply subtracting the first child’s bins from the parent vertex’s bins without any explicit binning at the other child [12]. Step 4 repeats steps 1 through 3 to the relevant records to complete the tree. With a fully-grown tree, Step 5 passes all the input records through the tree to update each record’s first and second order gradient statistics (\(g_i\) and \(h_i\)) based on the new tree’s prediction compared to the ground truth (i.e., the per-record loss), the loss function, and the record’s previous \(g_i\) and \(h_i\). This step also updates the new total loss across all the records for the new and old trees put together.

GB implementations can be configured to proceed vertex by vertex or level by level (i.e., explore together all the valid vertices at a level though some vertices may be missing). The above assumes the former, whereas the latter streams in all the input records and histogram-bins the relevant records at each vertex. Because multiple vertices are explored together, this configuration maintains a separate histogram per vertex.

In addition to the above qualitative description, we quantify the fraction of time spent in the algorithm’s steps later in Section IV and Section V-B.

B. Batch Inference

In batch inference, each record traverses all the decision trees. In a tree, each vertex’s predicate is evaluated for the record to determine the next vertex. At the leaf, the tree outputs a value. All the trees’ outputs are combined to compute the final prediction for the record. Unlike training, inference involves only the tree traversal.

C. Parallelism and Access Patterns

There is enormous fine-grain parallelism in training both across the features of a record (e.g., 10s-1000s) and across different records (e.g., hundreds of millions). As mentioned in Section I, the computation and its parallelism are almost entirely data-access heavy as opposed to computation-heavy like DNNs. Step 1 in Table I has both intra- and inter-record parallelism. The histograms across the features can be updated in parallel for intra-record parallelism. Fortunately, the histograms can fit on-chip (e.g., 2-8 MB). However, different features of a record often update different bins (e.g., feature 1 may update bin 8, feature 2 may update bin 0), the accesses are both fine-grained and irregular. An easy way to exploit inter-record parallelism is to replicate the histograms followed by a reduction across each histogram’s replicas. Step 2 is short as it iterates over all the features’ bins which can be processed in parallel but are far fewer than the input records. Steps 3, 4, and 5’s parallelism is inter-record where the new predicate is evaluated for each record. Step 5’s parallelism is also inter-record where the new tree is traversed for each record. However, because only subsets of the records are likely relevant to vertices other the root, the records’ access is irregular (non-contiguous) in steps 1, 3, and 5. Further, Step 5’s tree traversal is also highly irregular because different records would follow different paths through the tree. While steps 1 and 3 do not have any load imbalance issues, different records in Step 5 may see slightly different path lengths in some cases. Because the training algorithm grows the trees up to a pre-specified depth, the path lengths are mostly similar (but not the same because some paths may be terminated early due to non-profitability). Fortunately, such modest load imbalance can be handled by averaging out over multiple records. Finally, steps 3 and 5 use only a feature and a subset of the features of the records, respectively, potentially wasting memory bandwidth.

In batch inference, there are both abundant inter-tree parallelism (e.g., 500-1000) and inter-record parallelism (e.g., hundreds of thousands in small batches to millions in large batches). However, each record takes a different path through the trees implying significant fine-grained but irregular access parallelism, like training. Further, the path lengths through different trees may be slightly different for different records. Luckily, the load can be balanced by averaging across the records of the batch, like Step 5 in training.

D. Why are multicores and GPUs insufficient?

While there are fast implementations of GB training on multicores and GPUs, these implementations leave significant
The smallest of our benchmarks (maintain a private copy of the histogram bin counters. Even GPUs’ Shared Memory. For example, each warp will need to number of copies of the bin state, which will not fit in to a linear (in the degree of multithreading) increase in the are going to different copies. However, privatization leads disallowing fine-grained thread interleaving. The second way Locking is expensive as it effectively limits multithreading by atomicity of the read-modify-write components of bin updates. The interleaving of achieving high performance by hiding memory latency, interacts multi-threading, which is fundamentally required for GPUs to option is not usable for GB training because of the read-bandwidth structures like the GPUs’ Shared Memory, which is typically limited to 48KB-96KB. Unfortunately, even that access to the histograms (Step 1, the tree (Step 5), and the records (steps 1, 3, and 5). However, the multicore’s modest parallelism (e.g., 32 threads) and limited on-chip cache to hold the replicated histograms means multicores exploit only a small fraction of the parallelism available in the application (100-500 intra-record and abundant inter-record parallelism).

Similarly, in batch inference, multicores can exploit only a fraction of the huge inter-tree and inter-record parallelism.

In contrast, GPUs can exploit abundant fine-grained parallelism in training as long as the parallelism is regular. However, the data-dependent histogram bin updates are irregular. GPUs can even handle memory-access irregularity as long as the footprint of the irregular accesses fits in special high-bandwidth structures like the GPUs’ Shared Memory, which is typically limited to 48KB-96KB. Unfortunately, even that option is not usable for GB training because of the read-modify-write nature of histogram bin updates. Specifically, multi-threading, which is fundamentally required for GPUs to achieve high performance by hiding memory latency, interacts poorly with read-modify-write updates. The interleaving of GPU warps due to multi-threading will lead to incorrect results. Each of the two possible ways to overcome this read-modify-write problem results in performance degradation in their own way. The first way is to use locks to maintain atomicity of the read-modify-write components of bin updates. Locking is expensive as it effectively limits multithreading by disallowing fine-grained thread interleaving. The second way is to privatize the bin state so that multithreading updates are going to different copies. However, privatization leads to a linear (in the degree of multithreading) increase in the number of copies of the bin state, which will not fit in GPUs’ Shared Memory. For example, each warp will need to maintain a private copy of the histogram bin counters. Even the smallest of our benchmarks (Higgs) has 28 numerical features yielding 7K bins (using 256 bins/field) of 8 bytes each – i.e., 56 KB per warp. The typical per-SM Shared Memory under 96 KB can accommodate at most one warp (i.e., no multi-threading) which would eliminate the GPU’s ability to tolerate latencies. Alternatively, the GPUs would need an impractically-large 1.75 MB of Shared Memory to accommodate 32 warps.

In summary, it is difficult to achieve high performance for GB training on GPUs because of the above multiple constraints of GPUs. Indeed, GB implementations on GPUs achieve modest (around 2x) speedups over the multicore implementations, which we validate in Section V-E. For example, a recent GPU-optimized GB implementation achieves around 2.3x mean speedup over a 20-core multicore implementation [60].

For batch inference on GPUs, multithreading is possible because there are no read-modify-write problems. However, SIMT parallelism is significantly degraded as different trees (and different records) traverse different tree paths. The lack of SIMT parallelism can result in poor GPU performance. Using Shared Memory to accommodate irregular accesses requires holding as many trees (or copies) as the threads which will not fit.

E. Previous FPGA-based GB acceleration

One FPGA-based work [57] parallelizes only across records like a multicore by holding histogram copies which degrade on-chip capacity. Booster’s intra-record parallelism is higher than that of this approach to which we compare in Section V-A. Another work [52] is just a one-page paper which pipelines the processing but includes few other details.

III. BOOSTER

Recall from Section I that Booster’s key contributions are: (1) a scalable sea of small SRAMs to match GB trees’ abundant, fine-grained, irregular, small-data-structure access parallelism (e.g., scale to 3200 SRAMs), (2) mapping the gradient-accumulating histogram bins (step 1) to SRAMs using a group-by-field strategy that outperforms a naive greedy-packing strategy, and (3) employing a redundant per-field column-major format in addition to the natural per-record row-major format to save memory bandwidth in single-predicate evaluation and one-tree traversal (steps 3 and 5).

A. Group-by-field mapping of bins to SRAMs

As discussed in Section II, the numerical fields are associated with a number of bins. Figure 4 illustrates the bins for the three fields of the frequent-flier database. The two categorical fields have three and two ‘yes’ bins respectively. Recall from Section II that the ‘no’ bin gradient summations can be reconstructed. For ease of illustration, Figure 4 assumes that FP features are discretized to six (6) bins; a real application would typically use 128-256 bins in practice.

The placement of the histogram bins in SRAMs has a significant impact on work serialization and balance in step 1. For example, if histogram bins belonging to multiple fields are placed in the same SRAM, multiple updates to those bins have to be serialized. However, histogram bins placed on different
SRAMs can be updated concurrently. Booster's sea-of-SRAMs approach helps harness this parallelism.

In addition, the mapping of bins to SRAMs has an impact on SRAM load balance. Naively packing the bins state in SRAMs based on capacity results in load imbalance and underutilization. Figure 4 illustrates the naive packing approach assuming an SRAM capacity of six bins. Bins are allocated to SRAMs (shown in dashed boundaries) till the SRAM if filled. Under this assignment, it is possible for all three gradient updates corresponding to a record to be assigned to the first SRAM as shown in Figure 4. In contrast, the second SRAM may have no updates to process.

We observe that there is exactly one update across all the bins of a field, whether numerical or categorical (recall from Section II that each missing field has a default 'absent' bin). Booster uses a group-by-field mapping wherein all the histogram bins of a field are mapped to a single SRAM, utilizing near 100% SRAM and DRAM bandwidths. Figure 4 shows that all bins that are shades of blue (or amber or green) which are associated with a single field are mapped to one SRAM. (If the number of bins associated with a single field exceed the capacity of an SRAM bank, those bins may be spread across multiple SRAMs. Our goal is to avoid bins of multiple fields sharing an SRAM bank as that leads to (avoidable) serialization.

**B. Booster microarchitecture**

Booster’s microarchitecture consists of a sea of small SRAMs each of which has a floating-point adder for updating $G$ and $H$ (Figure 5). Each Booster Unit (BU) comprises one SRAM and the associated adder. Multiple BUs are organized in a cluster (e.g., 64) which may be replicated (e.g., 8).

For the current tree leaf, the single-predicate step in the previous iteration of the inner step 2 loop produces a stream of pointers to the relevant records (all the records are relevant for the root). For the histogram-binning step (step 1), Booster fetches each relevant input record (one or more memory blocks, say 64 bytes) using the pointers, distributes each field to a BU, and broadcasts the record’s $g_i$ and $h_i$ to each BU. The broadcast bus in Figure 5 performs a logical broadcast implemented as a simple, pipelined broadcast over point-to-point links (e.g., 16 BUs per link). Because the input has millions of records, this pipeline’s fill and drain overheads are negligible (e.g., 3200/16 = 200 cycles). The distribution of the fields occurs in a simple, fixed left-to-right order of the fields and SRAMs. The fixed order implies that simple one-to-one buses from the fetch buffer to the BUs suffice. The record format also specifies the starting feature number per field so that each BU can subtract this number from a record’s feature number for the field to locate the feature in the SRAM. Booster employs simple double-buffering to hide completely the fetch latency. Because the full set of pointers to the records relevant for every step is known a priori, the implicit prefetch of double-buffering removes memory latency as an issue. Further, though the relevant records would likely not be contiguous in memory, each record is one or memory blocks of contiguous bytes, thus achieving good memory bandwidth.

For step 1, each SRAM holds a field’s histogram bin counters, $G$ and $H$ for each bin (Table II). Each BU simply increments its incoming bin’s counter, and adds the record’s $G$ and $H$ to the bin’s $G$ and $H$. For more parallelism, the records can be partitioned among the clusters so that each cluster generates a set of histograms which are reduced at the end of the step. Because choosing the best split point (Step 2) is light-weight whose execution time is proportional only to the number of bins (thousands) and not the number of records (millions), we offload the step along with the reduction at Step 1 end to the host.

The best split point is expressed as a predicate used in the single-predicate step (Step 3). In this step, Booster first receives the predicate as a field number, a bin number, and a condition (e.g., ffmiles $\geq 50,000$) may be encoded as (Field-3 $\geq$ upper-bin-boundary $(Bin_i)$), as shown in Figure 2. This predicate is broadcast (replicated) to all the BUs of one or more clusters (Table II). The field number enables Booster to fetch only the relevant field of each relevant record in the redundant per-field column-major format. As before, the relevant single-field columns are distributed to the BUs which evaluate the predicate for each record and place the pointer in either the “predicate true” or the “predicate false” buffers. The BUs’ buffers are streamed out to off-chip memory. Like the input records, the output streams are also double-buffered. Unlike the full relevant records, the relevant single-field columns would likely be more non-contiguous (e.g., in a memory block of a single-field column, only a subset may be relevant). Nevertheless, our redundant format saves significant off-chip memory bandwidth compared to the original per-record row-major format which would fetch the whole record but use only one field. Step 4 iterates over steps 1 through 3 to grow the tree to the desired depth (or stop if the loss
The records are then histogram-binned (Step 1) by partition (a partition of all the records before the next fields than the SRAMs, then the records are partitioned into C. Microarchitecture extensions

Booster against high-performance CPUs and GPUs.

inde- resources), power/performance penalties (FPGAs are worse),

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are double-buffered and written back to off-chip memory in a stream. This stream efficiency motivates storing these fields separately.

Booster’s implementation should choose the SRAM size to be the smallest that accommodates all the features of a field, for typical fields. The amount of parallelism – i.e., the number of BUs – should be enough so that the on-chip work is rate-matched with the off-chip memory bandwidth. For example, assuming 400 GB/s memory bandwidth (sustained average bandwidth measured in Section IV), 1-GHz clock for Booster, and 64-byte blocks, leads to 6.25 blocks supplied every cycle. Each field consumes a byte to specify its feature (i.e., 64 fields in a block). The compute work for every field at its BU is a short integer subtract (to calculate the bin), an SRAM read, two pipelined floating-point adds, and an SRAM write, which can fit in, say, 8 cycles. The total SRAM occupancy associated with 6.25 \text{blocks/field} \times 8 \text{cycles/field} = 3200 \text{cycles}. Thus, 3200 SRAMs is adequate to saturate the memory bandwidth. Booster’s high parallelism effectively ensures that it is memory bound with all computation hidden under memory latency (of record reads).

Finally, FPGAs can support Booster realizations while keeping in mind the usual FPGA-versus-ASIC trade-offs of time to market (FPGAs are better, especially with Cloud-based FPGA resources), power/performance penalties (FPGAs are worse), and volume-dependent costs (FPGAs are less expensive at small volumes). Our contribution is the architecture, independent of ASIC or FPGA implementation though we show an example ASIC implementation so that we can compare Booster against high-performance CPUs and GPUs.

C. Microarchitecture extensions

We consider a few exceptional cases. (1) If there are more fields than the SRAMs, then the records are partitioned into subsets of fields with the \( G \) and \( H \) fetched for every partition. The records are then histogram-binned (Step ③) partition by partition (a partition of all the records before the next partition). Single-predication evaluation (Step ③) and one-tree traversal (Step ⑤) are not affected by this condition. (2) The partitioning strategy also applies to cases where the records are larger than the memory block. If the records are smaller than the block then there is some off-chip memory bandwidth loss, but if the records are smaller than half the block then two records are packed into one block. (3) If a field has more features than the SRAM entries, than multiple SRAMs are grouped logically to accommodate the field at a modest underutilization of SRAM bandwidth (each record would update only one of the SRAMs in a group). To maintain the one-to-one mapping between fields and SRAMs, pre-processing repeats that particular field’s bin twice in the record if and only if the field is spread over two SRAMs. Because each BU subtracts its field’s starting feature number from the record’s feature number to locate the SRAM entry (Section III-B), the repeated bin falls within only one of the two SRAMs (and outside the other BU’s SRAM).

(4) Conversely, it may not be profitable to pack multiple small fields to the same SRAM to save space because such packing reduces throughput. Each record would have to update the SRAM multiple times while the other SRAMs idle. In cases where the off-chip memory bandwidth limits the overall throughput with some SRAM throughput to spare, such packing may not reduce overall throughput. Further, each SRAM must accommodate a floating-point field in case an application has only such fields which typically have 256 features requiring 2 KB, the typical SRAM size. Then, such packing would mean larger SRAMs (grouping multiple SRAMs for capacity would reduce overall throughput) which ironically means more on-chip SRAM capacity to achieve higher space efficiency. As such, our results show 89% capacity utilization and near 100% SRAM and DRAM bandwidth utilization for our one-field-per-SRAM mapping. (5) Too many trees not fitting on-chip is relevant only for batch inference and can be addressed by distributing the trees to multiple Booster chips. (6) The trees not fitting in the SRAM is unlikely given that GB’s core idea is to form a strong model by combining many weak models (i.e., shallow trees). While a larger tree can be partitioned to fit into a group of SRAMs, we leave this case for future work.

D. Batch inference on Booster

Implementing batch inference on Booster is an extension of the one-tree traversal in training with the key difference being multiple decision trees in the former versus only one tree in the latter. In inference, each record traverses all the decision trees each of which is loaded as a table into a BU. Because each tree’s predicates may involve tens of fields of a record (typically different sets of fields for different trees), Booster simply broadcasts each full record to all the BUs. At each BU, each record sequentially traverses the tree making as many SRAM accesses as the path length through the tree. Multiple records are double-buffered to hide memory latency. Each tree’s output (typically a small value such as -1, 0, or 1) is buffered to be combined with the other trees’ outputs for a final prediction. The outputs are also double-buffered so that
the next record can start as soon as the previous record exits the tree. Thus, each tree is asynchronous with respect to the others, allowing load balancing across the trees by averaging over the records.

IV. METHODOLOGY

Datasets: We use the five datasets shown in Table III. For each dataset, we list the number of (a) training records, (b) fields per record, (c) categorical fields, and (d) features (after one-hot encoding of categorical features). For each dataset, we use sequential runs on an Intel 5th generation CPU instance on Google Cloud to train a model of 500 trees, each with depth of up to 6 (see Table III). We use sequential runs only to understand the work fractions of the various steps. For our performance comparisons, we use the aggressive Ideal 32-core configuration.

We use datasets under 10 million records to reduce experiment time (training under 20 minutes). Full-scale datasets are larger. For instance, using Terabyte Click Log [58], which has 1.7 billion records with 13 integer and 26 categorical features, to train 500 trees exceeds 80 hours on an Intel Xeon [49]; and a multi-modal dataset for wearables has 63 million records [54]. Unfortunately, large, commercial datasets are often not publicly available (e.g., Facebook researchers [31] state that the data is confidential and that “a small fraction of a day’s worth of data can have many hundreds of millions of instances.”). Section V-C scales up our datasets.

Dominant components of execution time: Figure 8 shows a breakdown of the normalized sequential training time corresponding to the steps in XGBoost (Table I). We see that Step 1 (histogram binning), Step 3 (single-predicate evaluation), and Step 5 (one-tree traversal) constitute over 98% of run time except for Mq2008 due to its small dataset. In contrast, Step 2 (choosing the split point of a tree vertex) is short enough to be offloaded to the host. As such, Booster’s omission of Step 2 from acceleration is justified.

We observed an interesting behavior in the two benchmarks with categorical data (Allstate and Flight) that reduces the work for histogram binning (Step 1). Due to one-hot encoding and the nature of the dataset, the left versus right sub-tree split of the records at a vertex is extremely lopsided (99%-1%, for example). In such cases, the histogram binning work is reduced drastically by binning only the smaller sub-tree and setting the larger sub-tree bins to be the parent’s bins minus the smaller sub-tree’s bins (Section II-A). This effect is that Step 1’s share is smaller for Allstate and Flight in Figure 8 despite their large datasets.

All benchmarks other than IoT yielded trees with leaves mostly at a depth of 6. IoT had many shallow trees which increases the relative fraction of Step 1 (see Figure 6) because Step 1 processes larger fractions of records closer to the root. This exceptional behavior of IoT impacts both its training and batch-inference performance, as we show later.

Software modifications: We implemented and verified that the software changes to XGBoost’s input data format (to support the redundant per-feature column representation) do not affect the numerical results of XGBoost training.

Simulator: We build a cycle-level performance simulator for Booster. Although we do model the delays of our histogram-binning, single-predicate-evaluation, and one-tree traversal (steps 1, 3, and 5) based on our RTL implementation, the delays are hidden entirely under memory latency by construction (Section III-B). For accurate memory latency and bandwidth simulation, we use DRAMSim2 [50] configured as a high-bandwidth, 24-channel memory, whose parameters are derived from the Hynix JESD235 standard and an Nvidia paper [11] (see Table IV). This memory achieves a sustained bandwidth of about 400 GB/s.

Simulated systems: Because directly comparing simulated systems and real ( multicore or GPU) systems is not meaningful, we simulate two alternatives for a multicore and a GPU called Ideal 32-core and Ideal GPU, respectively. We do sanity-check these alternatives against a real multicore and a real GPU. For performance comparisons, we conservatively
assume that the Ideal 32-core and Ideal GPU are constrained only by 32- and 64-way parallelism without any implementation artifacts (based on the parallelism limits described in Section II-D). Because our Ideal configurations assume perfect pipelines and caches, and perfect, convergent SIMT behavior, they are effectively upper-bounds on the performance of real multicores and GPUs, respectively. Both Ideal 32-core and Ideal GPU use the same memory configuration as Booster (see Table IV). Section V-E confirms that our Ideal 32-core and Ideal GPU configurations indeed outperform a real 32-core multicore (Intel 5th generation) and a real GPU (Nvidia V100), respectively. We also compare to an FPGA-based previous work [57], called Inter-record, which parallelizes only across records like a multicore (Section II-E). For fair comparison, we simulate this architecture assuming an ASIC implementation with the same area and clock speed as Booster (i.e., the only difference is the architecture). Because Booster offloads step 2 to the host, we add the time for the step on a real 32-core multicore host to the execution time of all the systems (Booster, Ideal 32-core and Ideal GPU). Further, we add the time for the data copy between the host and Booster (to and fro). This time is of the order of microseconds (PCIe transfers) whereas Booster reduces the total run time from minutes to seconds including the copy. As such, the copying time is negligible.

We model the energy of the Ideal 32-core and Ideal GPU configurations to be lower-bounds on energy consumption (in contrast to upper-bounds on performance). We conservatively model (1) the SRAM access energy of each configuration’s typical SRAM size (see Table V) using access activity from our simulator and per-access energy cost from CACTI 7.0 [8]. Similarly, we model the DRAM access energy based on transfer activity. Such simple models are conservative because they ignore major energy overheads in real multicores and GPUs (e.g., multicores’ superscalar, out-of-order issue cores, GPUs’ large register files and heavily-banked Shared Memory) that Booster does not incur.

**RTL implementation, FPGA validation and ASIC Synthesis:** We implemented Booster in System Verilog. We use Intel’s Quartus Prime (v15.0) with Qsys system builder for synthesis. We verified the correctness of our implementation using RTL simulation and by running tests on FPGA prototypes using a scaled-down version (8 BUs in 1 cluster). We used an Intel Cyclone IV FPGA with 150K logic elements, which is a modest prototyping FPGA. Using our System Verilog implementation, we synthesized an ASIC instance of Booster with 1 cluster with 64 BUs using Synopsys’s Design Compiler to estimate Booster’s area, power, and clock speed. We used the 45-nm technology FreePDK45 PDK/cell library [44] (newer technology nodes are unavailable). Because the FreePDK45 does not include a memory compiler, we use Cacti 7.0 [8] to estimate area and power-per-access for the SRAM tables.

| Configuration | # cores | Clock speed (GHz) | SRAM size (KB) | Energy (norm.) |
|---------------|---------|------------------|----------------|---------------|
| Real Multicore | 32 cores | 2.2 | 32 KB | NA |
| Ideal Multicore | 32 cores | 2.2 | 32 KB | NA |
| Real GPU | 80 (64-wide) SMs | 1.5 | 96 KB | NA |
| Ideal GPU | 64 (64-wide) SMs | 2.2 | 96 KB | 2.64 |
| Booster | 3200 BUs | 1 | 2KB | 0.71 |

**V. Results**

Our results show: (1) performance comparison of Booster, Ideal GPU, and Ideal 32-core configurations, (2) execution time breakdown for those schemes to better explain the observed performance trends, (3) the relative performance impacts of the various Booster components, (4) energy comparison, and (5) area and power results from ASIC synthesis.

**A. Performance**

Figure 7 shows the speedup achieved by Ideal GPU, the Inter-record scheme (IR) [57] (Section II-E and Section IV), and Booster over the Ideal 32-core baseline (Y-axis) for each of the five benchmarks. In addition, we also include the geometric mean speedups.

Ideal GPU achieves modest speedups between 1.6x and 1.9x over Ideal 32-core across all benchmarks. We have also validated similar speedups on real hardware (see Section V-E). IR exploits only inter-record parallelism like multicores, requiring GB histogram copies which are area-inefficient. For the same area as Booster, IR can fit 271 copies/processing units for Higgs and 179 for Mq2008. While an ASIC cannot have different processing units for different benchmarks, we conservatively assume so as IR’s original FPGA-based implementation can achieve this flexibility. For the other benchmarks, even one copy does not fit, a case not considered by IR which shows results only for Higgs with FPGA-bounded 64 copies. At the same clock speed as Booster, IR achieves some modest speedups over Ideal 32-core which essentially has 32 copies. IR’s original speedup for Higgs [57] is higher because of (1) holding on-FPGA all 10,000 input records (zero DRAM traffic, infeasible for millions of records), and (2) weaker base cases of 12-thread CPU and Nvidia 1080TI GPU.

Booster achieves speedups varying from 30.6x (for IoT) to 4.6x (for Flight), with a mean speedup of 11.4x, over the aggressive Ideal 32-core baseline. Because Ideal 32-core and Ideal GPU are limited only by their exploited parallelism without any implementation artifacts (32- and 64-way, respectively), these speedups isolate the impact of Booster’s massive parallelism (3200-way). Similarly, IR’s lower parallelism places IR well behind Booster. For the accelerated steps, Booster hits the memory bandwidth limit by capturing high SRAM parallelism. As such, the overall speedup is effectively limited by a combination of bandwidth limits for the accelerated steps and Amdahl’s law limits of the unaccelerated portion.

Finally, we note that the performance trends are as expected; we see higher speedups on larger datasets (e.g., IoT, Higgs). Smaller datasets (e.g., Mq2008) or larger datasets that behave like smaller datasets (e.g., Allstate and Flight) due...
to the presence of categorical data and skewed data distributions (see Section IV), achieve lower speedups. Later, in Section V-F, we confirm the dependence of speedup on dataset size by scaling up the datasets.

B. Execution time breakdown

Figure 8 shows the execution time breakdown (Y-axis) of the three architectures normalized to that of Ideal 32-core for our benchmarks (X-axis). The execution time is broken down by the steps (shown as sub-bars) of the training algorithm. We observe that the speedups inversely correlate with the fraction of execution time of Step 2. Note that Ideal 32-core’s breakdown here is different from the sequential breakdown shown earlier in Figure 6. The 32-core baseline relatively increases Step 2’s fraction of time. The Ideal GPU configuration offers a typical and modest reduction in the three accelerated steps. Even on the GPU, Step 2 does not see much improvement. In contrast, Booster makes all the accelerated steps vanishingly small. Booster’s residual execution time is dominated by the unaccelerated Step 2.

C. Isolating Booster’s optimizations

Figure 9 isolates the speedup contribution of Booster’s components (Y-axis, Ideal 32-core = 1) for our benchmarks (X-axis). The speedups are over Ideal 32-core (first bar). The second bar Booster-no-opts uses naive packing to map bins to SRAMs (Section III-A) and no optimizations other than exploiting BU parallelism. The next bar shows the speedup due to group-by-field mapping (Section III-A) which shows improvements for the two benchmarks with categorical fields (Allstate and Flight). Recall that the mapping is designed to improve datasets with categorical fields. For benchmarks without a single categorical field, naive packing achieves the same effect as the mapping because our SRAMs are sized to accommodate numerical fields. Finally, the third bar shows the contribution of our redundant per-field, column-major representation which helps accelerate steps 3 and 5. This optimization works best for benchmarks that already have high speedups. Effectively, speeding up Step 1 makes steps 3 and 5 take larger fractions of the residual execution time. As such, the impact of any optimization that targets steps 3 and 5 is magnified.

The redundant representation, a software-only optimization, may be applied to steps 3 and 5 in the Ideal GPU and Ideal 32-core configurations. However, Ideal 32-core and Ideal GPU see little benefits (under 4%) because (1) Step 1 dominates the execution time for Ideal 32-core and Ideal GPU (see Figure 8), (2) Step 5 is compute-bound on Ideal 32-core and Ideal GPU, and (3) Step 3 does improve, but with minimal overall impact (Amdahl’s Law effect).

D. Energy

We show access energy comparisons for SRAM and DRAM separately as we cannot measure the relative proportions of the two components. However, because Booster is strictly better in both SRAM energy and DRAM energy, Booster is guaranteed to achieve lower total energy regardless of the specific ratio of SRAM energy to DRAM energy.

Figure 10 compares the SRAM (Figure 10(a)) and DRAM (Figure 10(b)) energy across the three configurations (Ideal 32-core, Ideal GPU, and Booster). The results are averaged across all the benchmarks and normalized to that of Ideal 32-core. Ideal GPU’s SRAM energy is higher because of the 32-way-banked, 96-KB Shared Memory which incurs more energy than Ideal 32-core’s 32-KB L1 D-cache. In contrast, Booster accesses a smaller 2-KB SRAM, resulting in lower SRAM energy. For DRAM energy, Ideal 32-core and Ideal GPU are identical as they access the same set of blocks. In contrast, Booster has fewer DRAM transfers via the per-field column-major format (Section III-B).
E. Validating the Ideal models

Figure 11 compares the execution times on real hardware (32-core multicore and GPU) to those of Ideal 32-core and Ideal GPU for all our benchmarks (X-axis). The last bar shows the execution time of Booster. We use an Intel 5th generation processor for the multicore and an Nvidia V100 for the GPU; both on Google Cloud. The execution times are normalized (Y-axis) to that of Ideal 32-core (first bar), the same baseline used in all our speedup measurements. Figure 11 confirms two important properties. First, the Ideal 32-core execution time is always lower than that of the real 32-core system. Similarly, the Ideal GPU configuration is always better-performing than the real GPU.

These results confirm the conservative nature of our comparisons; Booster’s speedups are in comparison to aggressive, ideal baselines. Second, in comparing the GPU to the multicore configurations, our ideal model shows that Ideal GPU is always better-performing than Ideal 32-core. However, on real hardware, the results are mixed; GPU performance is worse than that of the multicore for two of the five benchmarks (Allstate and Mq2008). This result confirms that the irregularity of the workload does indeed limit the speedups achievable on a GPU; thus strengthening the case for an accelerator. Finally, a direct comparison between Booster and the real 32-core and GPU configurations, included for viewing convenience, confirms Booster’s speedups.

F. Sensitivity to dataset size

Given that commercial datasets are larger (Section IV) and that data is growing faster than Moore’s law [24], it is important to understand how Booster’s performance is affected by growing dataset sizes. To that end, we performed experiments by scaling up (replicating) data sizes by a factor of 10. Figure 12 shows the performance comparison of the three hardware configurations (Ideal 32-core, Ideal GPU, and Booster) for the scaled-up benchmarks (X-axis). The speedup of Ideal GPU over Ideal 32-core (Y-axis) remains modest (< 2x) and similar to the speedups with the unscaled datasets. In contrast, Booster’s speedups are dramatically higher for the larger datasets. Compared with the unscaled datasets (Figure 7), the speedup range improves from 4.6-30.6 to 9.8-61.5 with the scaled datasets; the geometric mean speedup increases from 11.4 to 27.9. Every benchmark achieves higher speedup with the scaled datasets than with the unscaled ones (Figure 7); even Flight, the benchmark with the lowest speedup improves from 4.6 to 9.8 speedup. This result highlights Booster’s strength that its performance will improve as data volume grows.

G. RTL Validation and ASIC synthesis results

Table VI shows the area and power estimates for a 50-cluster Booster chip with 64 BUs per cluster (using 40 nm technology). Our synthesis achieves 1-GHz clock speed. Almost half (55%) of Booster’s area goes to the SRAMs. Although the aggregate SRAM capacity adds up to only 6.4 MB (= 3200 * 2KB), the area is around 70% larger than that of a 1-bank 6.4-MB SRAM array as Booster uses the equivalent of 3200 banks for parallel access (the area would be much smaller for a recent technology node which is not available in FreePDK). Because the static power dominates the dynamic power, Booster’s SRAM power is only around 59% higher than that of the 1-bank case even though the latter makes only one access at a time while the former makes 3200 parallel accesses. While the SRAM area is larger than the FPUs’, the SRAM and FPUs dissipate nearly equal power, each accounting for around 41% of the total power.

Because the memory bandwidth on our FPGA platform was too low to run meaningful benchmarks, we limited our FPGA runs to verifying correctness.

H. Batch Inference

We augmented our simulator for batch inference where each record traverses 500 trees. Although we did not implement inference in RTL, we did implement the key building block – one-tree traversal – in our design. We use the latency
This approach can be seen as taking stochastic gradient descent steps in function space.

Booster targets offline GB, the most widely-used variant. Booster succeeds in accelerating the heavy work of training; processing millions of records over hours. If online training or inference processes one record or a small batch at a time, then no accelerator (including Booster) would be justified.

**ML Accelerators:** There are many DNN architecture proposals, including optimizations for compute \([3, 4, 17, 25, 26, 35, 38, 40, 48, 55]\), memory \([15, 20, 29, 42]\), and reuse \([5, 14]\). However, GB has not received much attention from architects.

**VII. Conclusion**

We proposed an accelerator – Booster– for training gradient boosting (GB) models. Booster’s design is driven by the observation that the training for GB models is dominated by three key computational steps – histogram binning, single-predicate evaluation, and one tree traversal – that are performed on a large number of records. Together, these three steps account for 90%-98% of sequential training time. While there is abundant inter- and intra-record parallelism, traditional multicores and GPUs are unable to parallelize the memory accesses which are irregular, data-dependent, and to small-data-structures. Booster employs (1) a scalable sea-of-small-SRAMs approach to harness large-scale parallelism (e.g. 3200-way), and (2) a bandwidth-preserving mapping of data fields to SRAMs resulting in significantly high parallelism. Our simulations show that Booster achieves 11.4x speedup and 6.4x speedup over an ideal 32-core multicore and an ideal GPU, respectively. Based on ASIC synthesis of FPGA-validated RTL using 45 nm technology, we estimate that a Booster chip would occupy 60 mm$^2$ of area and dissipate 23 W when operating at a 1-GHz clock speed. Our results show that Booster’s speedups are higher for larger datasets; which is important given that data growth is surpassing Moore’s law in recent years \([24]\). Given these results, Booster would be an attractive design for accelerating the highly-successful GB models.

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