A Low-Cost, High-Frequency Lock-in Amplifier Based on a Field Programmable Gate Array

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We present a lock-in amplifier based on a field programmable gate array capable of demodulation at up to 50 MHz. The system exhibits 90 nV/√Hz of input noise at an optimum demodulation frequency of 500 kHz. The passband has a full-width half-maximum of 2.6 kHz for modulation frequencies above 100 kHz. Our code is open source and operates on a $300 hardware platform.

I. INTRODUCTION

The lock-in amplifier (LIA) is an invaluable tool in scientific instrumentation, allowing the extraction of weak signals from noisy backgrounds, even where the amplitude of the noise is much greater than the signal. First described in 1941, early LIAs were based on heaters, thermocouples and transformers. More modern LIAs have been fully digital or implemented on field programmable gate array (FPGA) devices, which are able to exceed the performance of their analog counterparts. However, the cost of modern LIAs may prove prohibitive, particularly in cases where large numbers of input channels are required. By employing $300 Red Pitaya hardware, we are able to define an open-source LIA solution which is comparable with considerably more costly approaches. Commercially available high-frequency LIAs can cost in excess of $10,000.

Characterized by wide dynamic range and the ability to extract signal from noisy environments, LIAs are phase sensitive detectors due to their operating principles. A reference signal in the form of a sinusoidal wave is generated either internally by the LIA itself, along with a cosinusoidal wave, or externally by some other source which can also be manipulated to form a cosinusoidal reference. This reference is multiplied by the input signal, which carries the desired data modulated at the reference frequency. Where the frequency of the input signal does not equal the reference, and is integrated over a time large compared to the period of the reference, the output will be close to zero. Alternatively, where the input signal matches that of the reference, the output is equal to half the product of the amplitudes of the reference and input signal, meaning that only signals modulated at a frequency equal to that of the reference will be amplified, and other frequencies will be attenuated. Components out of phase with the sine reference will also be attenuated, due to orthogonality of the sine and cosine functions of equal frequency, hence the LIA is considered phase sensitive. Components in phase with the sine function will result in a non-zero value in the X output, whilst those in phase with the cosine function will produce a non-zero value in the Y output. X and Y can be combined by \( R = \sqrt{X^2 + Y^2} \) to provide a magnitude value, while phase \( \phi = \arctan \frac{Y}{X} \).

The Red Pitaya STEMlab 125-14 is a single board computer (SBC) with an integrated FPGA in the form of a Xilinx Zynq 7010 SOC allowing for the implementation of reprogrammable microarchitecture which would otherwise necessitate dedicated hardware. The reprogrammability of this FPGA makes it applicable for the LIA functionality described here and allows for further expansion and modification by end users. Two analog inputs are available in the form of ±20 V, 125 MS/s analog-to-digital converters (ADCs) with 1 MΩ input impedance.

In this article, we detail an LIA which has been implemented on the STEMlab’s FPGA chip, along with open-source operational and data transfer software which has been developed specifically for this application. We demonstrate that this device shares many capabilities with more expensive alternatives, as well as introducing features such as the ability to sweep the voltage of the internally produced reference modulation and the option to increase the number of available inputs by interfacing across multiple STEMlab units.

Comparison is made with the Zurich Instruments HF2LI LIA, which is specified for operation up to 50 MHz demodulation frequency. Whilst an extensive software application is provided with the HF2LI, the open source nature and readily available software and hardware of the LIA presented here allow for an attractive option where cost is a consideration. Research into low-cost FPGA based LIAs has produced a number of alternatives, including high resolution designs operating at up to 6 MHz demodulation, and simulations have been presented for a high frequency LIA based on the Red Pitaya STEMlab. The STEMlab is the basis for a range of related measurement instrumentation from PyRPL, including an LIA. However, we believe that this article is the first to characterize a high frequency low-cost LIA. The open source code may lead to a range of future uses in research, education and industry.
II. METHODS

A. Hardware & Software

The FPGA system design and implementation was performed using software provided by the manufacturer of the FPGA, Xilinx. A simplified version of the design circuitry block diagram can be seen in fig. 1. Signals received by the ADCs are passed to processing blocks where they are multiplied by the reference signal (which is generated internally by direct digital synthesis (DDS)) and filtered using a single pole infinite impulse response (IIR) filter. The resulting output is written to the SBC’s random access memory (RAM) via the FPGA’s memory interface block. These data are written to a ramdisk file also contained within the STEMlab’s RAM, alleviating high read/write workloads which were observed to cause critical failures of the SD card. The data are also passed to the on-board digital-to-analog converters (DACs) along with the reference signal which is used to modulate the desired signal.

Data retrieval from the STEMlab to a host computer can be achieved via the DACs which are provided with SMA connections for output to an oscilloscope. These DACs have 14 bit resolution combined with 125 MS/s data rate, and may have their amplification multiplied hundreds or thousands of times. However, noise introduced by the DACs makes the output undesirable in cases where small changes in signal intensity are to be detected. Alternatively, data may be transferred to a host PC via file transfer from the STEMlab’s RAM. This produces low noise data but can only be performed on the entirety of the LIA’s allocated storage space of approximately 65 megabytes (MB). Whilst this process may last for tens of seconds, all data (X, Y, R and $\phi$) for both output channels is received simultaneously. Further limitations include the inability to operate using an external lock-in reference, and cross-talk which can occur between the two input channels. Due to the programmable nature of the STEMlab, end users are able to implement their own data transfer methods, which may be shown to alleviate some or all of these limitations.

Whilst the FPGA is responsible for signal processing and data transfer, parameter setting takes place on the STEMlab’s Linux SBC. These functions are performed using C and Python codes written specifically for use with the LIA. These codes may be accessed via SSH or a terminal emulator, but in practice are accessed via a Java-based graphical user interface (GUI) on a client computer which allows the user to largely ignore the STEMlab’s Linux element.

B. Characterization Methodology

Data were extracted from both LIAs via digital ethernet connection. In the case of the Red Pitaya LIA (RePLIA) aboard the STEMlab, this avoided noise from its DACs which were found to increase noise by up to three orders of magnitude.

Noise for both LIAs during operation was measured at various demodulation frequencies with no input signal...
present and with a constant amplitude signal produced with an Agilent N5172B EXG vector signal generator. Similarly, noise was measured whilst varying the time constant of the LIAs, with the demodulation frequency fixed at the value determined to be the least noisy by the previous method. As with input noise, these data are presented after a fast Fourier transform (FFT).

Passbands for each LIA at various demodulation frequencies were obtained by applying a constant amplitude signal at the specified demodulation frequency. This signal was then combined with a sweep between a minimum and maximum frequency passing through the demodulation frequency, with a 10 s sweep time.

**Zurich Instruments HF2LI**

The HF2LI provides a built in input noise measurement protocol. The experimental conditions detailed in the HF2LI user notes were replicated and the input noise measured. Noise was collected whilst inputs were terminated for periods of 1, 10 and 100 seconds. This noise was then subjected to a FFT and the noise level assessed and compared with the manufacturer’s stated input noise level of $2.5 \text{nV}/\sqrt{\text{Hz}}$ at 1 MHz demodulation for output frequencies greater than 10 kHz.

**Red Pitaya Lock-In Amplifier**

Optimal operational parameters were deduced by examining the output of the RePLIA at varying demodulation frequencies and time constants. The optima chosen were those which resulted in the lowest output noise level. This behaviour was examined both with an applied signal and with terminated inputs. The RePLIA maintains capability over a wide range of demodulation frequencies which were also characterized, but figures are quoted with respect to optimal parameters unless otherwise stated.

### III. RESULTS

Figure 2 shows input noise spectra for both LIAs at 1 second, 10 second and 100 second collection periods. Increasing collection time $t$ was expected to produce a $\sqrt{t}$ decrease in noise. Both LIAs remained within 2% of this prediction after a 100 seconds collection time (fig. 2c). Noise figures were obtained by taking an average of baseline data from each LIA at the relevant collection time. In figure 2a, the data for 1 second of collection time has been zero padded, adding 4 seconds worth of zeros, to reduce the width of the frequency bins. These averages produce figures of 89, 21 and 6 nV for the RePLIA for collection times of 1, 10 and 100 seconds respectively, corresponding to sensitivities of 89, 66 and 60 nV/$\sqrt{\text{Hz}}$. When the RePLIA was operated using the conditions stipulated for measurement of the HF2LI input noise, the noise figures are 131, 133 and 130 nV/$\sqrt{\text{Hz}}$.

The noise spectrum for the HF2LI (fig. 2b) shows greater noise below 80 Hz and lower noise at higher output frequencies. By contrast, the RePLIA shows a higher level of noise which is largely steady up to 120 Hz (fig. 2a) output frequency.

Figure 3 shows FFTs of the RePLIA output at a range of demodulation frequencies, with time constants optimized for the relevant demodulation period (see supplementary information). There is a marked difference in noise at demodulation frequencies below 100 kHz, though above this threshold noise is roughly constant.

Output from the RePLIA digital-to-analogue converters (DACs) was also produced (see supplementary information), showing a consistent noise level at frequencies below 100 kHz. Though this noise level is several orders of magnitude greater than that incurred in data extracted via the ethernet connection, this may be an acceptable
Figure 3: FFTs of terminated input data, extracted via file transfer, at various RePLIA demodulation frequencies. Two distinct noise regimes seem to exist, with demodulation frequencies above 100 kHz producing significantly lower noise. Time constants were varied dependent on demodulation frequency (see supplementary information).

Figure 4: The signal to noise ratio at the RePLIA’s digital-to-analogue outputs increases with larger DAC multipliers. However, even small signals can lead to saturation of these outputs. Data obtained at 500 kHz demodulation frequency and a 10 ms time constant.

Figure 5: Output of frequency sweep in the megahertz range for the a) RePLIA and b) HF2LI. c) Maximum output voltage of the RePLIA plotted against demodulation frequency, showing the half power point. Note that the RePLIA has a sampling rate of 125 MHz.

100 kHz (see supplementary information), and they begin to reduce in intensity above 30 MHz demodulation with the HF2LI, whereas the output is consistent up to 50 MHz demodulation with the RePLIA. Figure 5c shows the normalised output at megahertz demodulation frequencies for both LIAs. The half power point is indicated ($V_{max}/\sqrt{2}$) (where $V_{max}$ is the peak voltage output), which for the RePLIA is encountered at a demodulation frequency of around 60 MHz, which is close to half of the device’s 125 MHz sample rate, as can be expected from the Nyquist sampling theorem.

IV. CONCLUSIONS

The RePLIA performs lock-in amplification at frequencies up to 50 MHz, with an input noise figure of 90 nV/$\sqrt{\text{Hz}}$. The respective figures from the Zurich Instruments HF2LI (50 MHz demodulation with 2.5 nV/$\sqrt{\text{Hz}}$ input noise) show that the FPGA LIA detailed in this article is a lower cost alternative.

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