Performance Modeling of Streaming Kernels and Sparse Matrix-Vector Multiplication on A64FX

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Abstract—The A64FX CPU powers the current #1 supercomputer on the Top500 list. Although it is a traditional cache-based multicore processor, its peak performance and memory bandwidth rival accelerator devices. Generating efficient code for such a new architecture requires a good understanding of its performance features. Using these features, we construct the Execution-Cache-Memory (ECM) performance model for the A64FX processor in the FX700 supercomputer and validate it using streaming loops. We also identify architectural peculiarities and derive optimization hints. Applying the ECM model to sparse matrix-vector multiplication (SpMV), we motivate why the CRS matrix storage format is inappropriate and how the SELL-C-σ format with suitable code optimizations can achieve bandwidth saturation for SpMV.

Index Terms—ECM model, A64FX, sparse matrix-vector multiplication

I. INTRODUCTION

A. Motivation: The A64FX CPU

The A64FX CPU is used in parallel computer designs from Fujitsu. It exists in several variants, the most basic of which (used, e.g., in the Fujitsu FX700 system) comprises 48 cores running at 1.8 GHz (see Table I for fundamental data). At a machine balance of 0.37 byte/flop, the architecture is expected to deliver a high fraction of its peak performance for optimized code. The chip is divided into four groups of twelve cores (core memory groups [CMGs]), each of which accesses its own ccNUMA domain. The 64 KiB L1 cache is core local, while 8 MiB of L2 are shared among the cores of each CMG. Figure 1 shows bandwidth scaling using compiler-generated OpenMP code with compact pinning for three elementary operations: the STREAM TRIAD (a[i]=b[i]+s*c[i]), a sum reduction (s+=a[i]), and a sparse matrix-vector multiplication with the HPCG matrix using gcc version 10.1.1. The working set size is 4 GB for TRIAD and SUM; for HPCG the dimension is 128³.

Fig. 1. Scaling of STREAM TRIAD, SUM reduction, and SpMV in CRS format with the HPCG matrix using gcc version 10.1.1. The working set size is 4 GB for TRIAD and SUM; for HPCG the dimension is 128³.

will be instrumental in this, leading to valuable insights into performance bottlenecks of this new CPU architecture.

B. Brief overview of the ECM model

Full coverage of the ECM model is beyond the scope of this work. We give a brief overview and refer to the most recent publication [4] for details.

The model considers execution time contributions for steady-state loops from the core (assuming all data is in L1), data paths in the cache hierarchy, and the memory interface. For the core component, the loop’s assembly code is analyzed for predictions of optimal throughput, critical path, and longest loop-carried dependency (the current development branch of the OSACA tool [5] has preliminary support for A64FX). Data transfer volumes through the memory hierarchy are obtained either by manual analysis or by the Kerncraft [6] tool; together with the known bandwidths of all data paths, time contributions for L1-L2 and L2-memory transfers are obtained. A machine model is constructed that makes assumptions on how all these contributions overlap in time in order to arrive at a runtime prediction for a given number of loop iterations. For the benchmarks under investigation here, manual predictions are straightforward and the Kerncraft tool is not needed.

C. Testbed and experimental methodology

All experiments were carried out on QPACE 4, the Fujitsu FX700 system running CentOS 8.2 at the physics department of the University of Regensburg. The core clock frequency is fixed to 1.8 GHz on this machine. All code was compiled with gcc 10.1.1, using options -Ofast.

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TABLE I
KEY SPECIFICATIONS OF THE A64FX CPU IN THE FX700 SYSTEM.

| Specification                  | Value                  |
|-------------------------------|------------------------|
| Microarchitecture             | A64FX                  |
| Supported core frequency      | 1.8 GHz                |
| Cores/threads                 | 48/48                  |
| Instruction set               | Armv8.2-A+SVE          |
| Max. SVE vector length        | 512 bit                |
| Cache line size               | 256 bytes              |
| L1 cache capacity             | 48 × 64 KB             |
| L1 bandwidth per core         | 128 B/cy LD ⊕ 64 B/cy ST |
| L2 cache capacity             | 4 × 8 MB               |
| L2 bandwidth per core         | 64 B/cy LD, 32 B/cy ST |
| Memory configuration          | 4 × HBM2               |
| CMG theor. mem. bandwidth     | 230 Gbyte/s = 128 byte/cy |
| CMG TRIAD bandwidth           | 210 Gbyte/s = 117 byte/cy |
| CMG read-only bandwidth       | 225 Gbyte/s = 125 byte/cy |
| Page size                     | 64 KiB                 |
| L1 translation lookaside buffer| 16 entries             |
| L2 translation lookaside buffer| 1024 entries           |

TABLE II
IN-CORE INSTRUCTION THROUGHPUT AND LATENCY (IF APPLICABLE) FOR SELECTED INSTRUCTION FORMS.

| Instruction          | Reciprocal Throughput [cy] | Latency [cy] |
|----------------------|----------------------------|--------------|
| ld1d (standard)      | 0.5                        | 11           |
| ld1d (gather, simple stride) | 2.0                  | ≥ 11         |
| ld1d (gather, complex stride) | 4.0                  | ≥ 11         |
| simple gather + std. load | 3.5                  |              |
| complex gather + std. load | 5.5                  |              |
| st1d (standard)      | 1.0                        |              |
| fadd                 | 0.5                        | 9            |
| fmad                 | 0.5                        | 9            |
| fmla                 | 0.5                        | 9            |
| fmul                 | 0.5                        | 9            |
| fadd (512bit)        | 18.5                       | 72           |
| faddv (512bit)       | 11.5                       | 49           |
| while{le|lo|ls|lt}   | 1.0                        | 1            |

Apart from the cases shown in Fig. 1 SVE vector intrinsics (ACLE [7]) were employed to have better control over code generation. All benchmarks were run in double precision, leading to a vector length (VL) of eight elements. Performance event counting was done with likwid-perfctr [8] v5.0.1, whose current development branch contains support for A64FX. For benchmarking individual machine instructions we employed the ibench [9] framework and cross-checked our results with the A64FX Microarchitecture Manual [10]. We do not show any run-to-run statistics as the fluctuations in measurements were below 3%. Information about how to reproduce the results in this paper can be found in the artifact description [11].

This paper is organized as follows: Section II provides an analysis of the in-core architecture, including parts of the SVE instruction set, and the memory hierarchy of the A64FX. In Sect. III we use microbenchmarks to construct and validate the ECM performance model for serial and parallel steady-state SVE loops. The insights gained are then used in Sect. IV to revisit the SpMV kernel and motivate why an appropriate matrix storage as well as sufficient unrolling are required to achieve bandwidth saturation. Finally, Sect. V gives a summary and an outlook to future work.

II. ARCHITECTURAL ANALYSIS

A. In-core

For creating an accurate in-core model of the A64FX microarchitecture, we analyze different instruction forms [12], i.e., assembly instructions in combination with their operand types, based on the methodology introduced in [13]. Table I shows a list of instruction forms relevant for this work. Standard SVE load (ld1d) instructions have a reciprocal throughput of 0.5 cy, while stores (st1d) have 1 cy. The throughput of gather instructions depends on the distribution of addresses: “Simple” access patterns are stride 0 (no stride), 1 (consecutive load), and 2, while larger strides and irregular patterns are considered “complex.” The former have lower reciprocal throughput and latency than the latter. However, when occurring in combination with a standard LD, we can observe an increase of reciprocal throughput by 1.5 cy instead of the expected 0.5 cy. This is caused by the dependency of the gather instruction on the preceding index load operation, which the out-of-order (OoO) execution cannot hide completely.

Note also the rather long latencies for arithmetic operations such as MUL, ADD, and FMA compared to other state-of-the-art architectures (e.g., on Intel Skylake or AMD Zen2 these are between 3 cy and 5 cy). Each core’s front end has an instruction buffer with 6 × 8 entries, which can feed six instructions per cycle to the decoder. The decoder feeds up to four μ-ops per cycle to two pairs of reservation stations, which have ten (address generation and load units) or 20 (execution pipelines and store units) entries. These attributes emphasize the importance of a compiler that is capable of exploiting the theoretical in-core performance by intelligent code generation. The small reservation stations in combination with high instruction latencies can result in inefficient OoO execution. While these constraints cannot be overcome completely, appropriate loop unrolling, consecutive addressing, and interleaving of different instruction types have shown to be beneficial in our benchmarks; see Sections III and IV for details.

The SVE instruction set introduced a “while{cond}” instruction to set predicate registers in order to eliminate remainder loops (see Sect. IV for details). A port conflict analysis revealed that this instruction does not collide with floating-point instructions or data transfers, so it does not impact the kernel runtime compared to non-SVE execution.

B. Memory hierarchy

While parallel load/store from and to L1D is possible for general-purpose and NEON registers, different types of SVE data transfer instructions in L1D cannot be executed in one cycle: Using SVE, one A64FX core can either load up to 2 × 64 byte/cy or store 64 byte/cy from/to L1. The L2 cache can deliver 64 byte/cy to one L1D but tops out at 512 byte/cy per CMG. The L1D-L2 write bandwidth is half the load band-
width, i.e., 32 byte/cy per core, and is capped at 256 byte/cy per CMG. Finally, the maximum bandwidth between memory and L2 cache is 128 byte/cy per CMG for loading and 64 byte/cy per CMG for storing data, resulting in a theoretical total peak load bandwidth of 922 Gbyte/s (230 Gbyte/s per CMG) and peak store bandwidth of 461 Gbyte/s (115 Gbyte/s per CMG). In practice, about 91% of the peak load bandwidth can be attained using the STREAM TRIAD benchmark and 98% using a read-only benchmark (see Table I). These measured bandwidths will be used as baselines for the memory transfer bandwidth in the ECM model.

### III. Construction of the ECM Model

#### A. Overlap hypothesis

In order to find out which of the time contributions for data transfers through the cache hierarchy overlap, measurements for a test kernel are compared with predictions based on different hypotheses; see [4] for an in-depth description of the process. If a hypothesis works for the test kernel, it is tested against a collection of other kernels with different characteristics.

Here we use the STREAM triad kernel \((a[i]=b[i]+s*c[i])\) to narrow down the possible overlap scenarios. This kernel has two LD, one ST, and one FMA instruction per SVE-vectorized iteration. Figure 2 shows performance in cycles per VL (i.e., eight iterations) for different code variants: “u=1” denotes no unrolling (apart from SVE), and “u=8” is eight-way unrolled on top of SVE. Some level of manual unrolling (typically eight-way) is always required for best in-core performance. This is even more important in kernels where dependencies cannot be resolved easily by the out-of-order logic. In Fig. 2a we show data for a 2d five-point stencil, where SVE alone (without further unrolling) is up to 2× slower than the eight-way unrolled code, despite the lack of loop-carried dependencies. Figure 2a shows data for a sum reduction, which requires eight-way modulo variable expansion (MVE) on top of SVE to achieve optimal performance due to the large latency of the floating-point ADD instruction.

Optimal performance beyond the L1 cache is only achieved when aligning all arrays to 32-byte boundaries; within L1, 512-byte alignment is needed. In our experiments we used 1024-byte aligned arrays throughout. The standard `malloc()` function only guarantees 16-byte alignment and leads to performance loss (“u=8+malloc”).

At a working set size of 64 MiB, performance drops significantly for all three kernels. We can correlate this with a sudden rise in L2 TLB misses (see Fig. 2a). Beyond this threshold, exactly one TLB miss per 64 KiB page occurs. This leads to the conclusion that L2 TLB misses are rather expensive on this machine. A larger OS page size or other configuration changes might help improve the situation but are left to future work. The effect will be ignored in the following.

In order to arrive at an overlap hypothesis, we ignore the FMA because it is fully overlapping when perfect OoO processing is assumed. Figure 3 compares three scenarios ((a), (b), and (c)) with measured cycles per VL (d). Note that there is a large number of possible overlap hypotheses, and we can only show a few here. The one leading to the best match to the STREAM TRIAD data is the following:

- L1D is partially overlapping: Cycles in which STs are retired in the core can overlap with L1-L2 (or L2-L1) transfers, but cycles with LDs retiring cannot.
- L2 is partially overlapping: Cycles in which the memory interface writes data out to memory can overlap with transfers between L2 and L1, while memory read cycles cannot.

As usual, the time required for compute instructions or, more generally, non-data-transfer time in the core, fully overlaps with all data transfers. Note that we include write-allocate transfers (due to store misses) in the analysis.

#### B. Validation of the single-core model for streaming kernels

With the in-core and data transfer models in place we can now test the ECM model against a variety of loop kernels. Table III shows a comparison of predictions and measurements. For each kernel, three numbers represent the cycles per VL with the data set in L1, L2, and memory, respectively. In case of the 2d five-point stencil, three cases are shown: layer condition (LC) satisfied at L1, broken at L1, and broken at L2 (see [3] for a comprehensive coverage of layer conditions in the context of the ECM model).
The results have been obtained by running each kernel with unrolling factors from 1 to 16 and taking the best result. Entries in red color have a deviation from the model of at least 15%. The selected unrolling factor for each measurement is shown as a subscript.

| Kernel         | Predictions | Measurements |
|----------------|-------------|--------------|
| COPY (a[i]=b[i]) | [1.5 4.5 5.6] | [1.65 4.45 5.15] |
| DAXPY (y[i]=a[i]+x[i]*y[i]) | [2.0 5.0 6.1] | [2.1 4.76 5.56] |
| DOT (sum+a[i]+b[i]) | [1.0 3.0 4.1] | [1.7 3.25 4.06] |
| INIT (a[i]=p) | [1.0 3.0 3.5] | [1.03 3.94 4.34] |
| LOAD (load(a[i])) | [0.5 1.5 2.0] | [0.7 1.92 2.64] |
| TRIAD (a[i]=b[i]+s+c[i]) | [2.0 6.0 7.7] | [2.1 5.82 6.71] |
| SUM (sum+a[i]) | [0.5 1.5 2.0] | [1.1 2.01 2.53] |
| SCHONAUER (a[i]=b[i]+c[i]+d[i]) | [2.5 7.5 9.7] | [2.7 7.29 8.49] |
| 2D5PT - LC satisfied | [3.5 6.5 7.6] | [5.8 7.89 8.80] |
| 2D5PT - LC violated in L1 | [3.5 8.5 9.6] | [5.8 8.67 9.43] |
| 2D5PT - LC violated | [3.5 8.5 10.7] | [5.8 8.67 10.07] |

Fig. 3. Comparing different overlap scenarios (a), (b), and (c) for data transfers in the memory hierarchy with measured cycles per VL (d) on the STREAM TRIAD kernel.

Table III
ECM MODEL PREDICTION AND MEASUREMENTS IN [CY/VL] FOR DIFFERENT STREAMING AND STENCIL KERNELS. RED COLOR INDICATES A DEVIATION FROM THE MODEL OF AT LEAST 15%. THE SELECTED UNROLLING FACTOR FOR EACH MEASUREMENT IS SHOWN AS A SUBSCRIPT.

The analysis of the SUM reduction benchmark revealed that the long ADD latency prevents bandwidth saturation if proper unrolling with MVE is not employed. The CRS SpMV is similar as it requires horizontal reduction along each row of the matrix (the inner loop). However, this loop is short since the average number of non-zeros per row, \(N_{nzr}\), is typically in the range of 10–1000 for practical applications. For the HPCG matrix we have \(N_{nzr} \approx 27\), so four 512-bit wide \(fmadfmla\) instructions (eight iterations each) are required, which takes \(4 \times 9\) cy. The required horizontal reduction \(\alpha\) of the final vector result adds another 11.5 cy, which leads to a minimum of 47.5 cy of in-core execution time per row \(2.05 \text{Gflop/s}\). The memory data traffic for CRS SpMV is \(27 \times (12 + 2\alpha) + 20\) bytes per row, where \(\alpha\) characterizes the efficiency of right-hand side (RHS) access [13]. For the regular stencil-like HPCG matrix, \(\alpha\) can be assumed to be close to the optimistic lower limit of \(\alpha = 1/N_{nzr}\), resulting in a data traffic of 352 bytes per row (measured 363 bytes using \texttt{likwid-perfctr}). This leads to a single-core bandwidth of 352 bytes/row \(\times f/47.5\) cy/row = 13.3 Gbyte/s, where \(f\) is the clock frequency. Since \(12 \times 13.3\) Gbyte/s = 160 Gbyte/s, it is impossible for this code to hit the bandwidth limit of 210 Gbyte/s per CMG.

In practice, the loop overheads caused by the extremely short loops and the poor OoO execution (see Sect. III-B)
further decrease the single-core performance. Contrary to the sum benchmark, unrolling does not fix the problem due to the extra work at the end of the short loop and loss of efficiency when \( N_{\text{opt}} \) is not a multiple of the vector length. Hence, we choose the SELL-\( C-\sigma \) sparse matrix format \cite{15}, which is a portable, SIMD-friendly data format for CPUs, GPUs, and vector machines.

SELL-\( C-\sigma \) stores chunks of \( C \) consecutive rows (zero-padded to the longest row) in column-major format. The parameter \( C \) is tunable; for efficiency, it should be a multiple of \( VL \) as well as large enough to allow for sufficient unrolling. A further benefit of the format is the lack of an expensive horizontal add operation (\texttt{faddv}). The only drawback is that the zero padding can reduce the efficiency if rows have very different lengths. To mitigate this effect, rows are first sorted by descending length within a sorting window (\( \sigma \)) to reduce the padding. With proper selection of \( C \) and \( \sigma \), the padding can be made negligible in most cases. For the matrices considered in this work it was never larger than 5%.

On A64FX, \( C = 32 \) enables four-way unrolling on top of SVE, which should reduce the ADD latency by a factor of four (i.e., to 2.25cy). According to the ECM model, the data transfer through the memory hierarchy should then become the bottleneck. Much of the time here is lost in the LD to the index array and the subsequent gather instruction from the L1 cache to the registers (5.5cy according to Table \ref{table1}). Loading the matrix values costs an extra 0.5cy, so we require at least \((5.5 + 0.5) \times 27/8cy = 20.3cy \) (at VL = 8) per row of the HPCG matrix for the L1 to register transfers. From L2 and memory, as shown above, at least 352bytes are required per row, which translates to 352/64cy = 5.5cy and 352/117cy = 3cy respectively (see Table \ref{table1} for bandwidths). Since the transfers are primarily reads, the contributions have to be summed up as shown in the overlap hypothesis in Sect.\ref{sec1}A. This results in a total of almost 28.8cy per row, i.e., 3.4Gflop/s (equivalent memory bandwidth 22Gbyte/s). The measured performance is 3.3Gflop/s on a single core. Hence, the code can saturate on a CMG as shown in Fig.\ref{fig5} (left), topping out at 31Gflop/s (i.e., 202Gbyte/s). In contrast to other contemporary CPUs, saturation requires almost all cores of a CMG; any loss of efficiency on the sequential code due to extra traffic or latency will directly impact the total performance. The scaling across ccNUMA domains (using parallel first touch) is nearly perfect, leading to a final performance of 110.8Gflop/s. Based on our previous Roofline analysis of the HPCG algorithm \cite{16}, we expect a full HPCG benchmark performance of close to 100Gflop/s on A64FX.

In Fig.\ref{fig5} (right) we show the full-node (48 cores) performance of SELL-\( C-\sigma \) in comparison to CRS on a collection of matrices from the SuiteSparse Matrix Collection \cite{17}. All matrices saturated the main memory bandwidth with SELL-\( C-\sigma \), and we see an improvement of \( 1.5 \times \) compared to CRS on average. The SpMV performance attained with SELL-\( C-\sigma \) is on par with NVIDIA V100 GPU \cite{18} and NEC SX-Aurora Tsubasa vector accelerators \cite{19}.

![Fig. 5. (Left) Scaling performance and ECM prediction on one CMG for SpMV in SELL-\( C-\sigma \) and CRS format with the HPCG matrix. (Right) Full-node SpMV performance of different matrices in Gflop/s in both formats. \( C \) was chosen as 32 and \( \sigma \) was tuned between 1 and 1024. Reverse Cuthill-McKee reordering \cite{20} was done if it improved the performance.](image)

### A. Summary and outlook

Via an analysis of in-core features and data transfers, we have established an ECM machine model for the A64FX CPU in the Fujitsu FX700 system and applied it to simple streaming kernels and sparse matrix-vector multiplication using the HPCG matrix. For in-memory data sets, the single-core ECM model was shown to be accurate within a maximum error of 20%. The memory hierarchy turned out to be partially overlapping, allowing for a substantial single-core memory bandwidth with optimized code. Long floating-point instruction latencies and limited out-of-order execution capabilities were identified as the main culprits of poor performance and lack of bandwidth saturation. With the current gcc compiler, vector intrinsics and manual unrolling are often required to achieve high performance. For SpMV, the SELL-\( C-\sigma \) matrix storage was shown to achieve superior performance and memory-bandwidth saturation, though requiring almost all cores on the ccNUMA domain. This means that SpMV performance will be very sensitive to load imbalance and inefficiencies in data accesses.

In future work we will conduct a more comprehensive analysis of SpMV and a comparison with other high-end devices like the Nvidia A100 GPU and the NEC SX-Aurora Tsubasa. We will also investigate advanced A64FX features such as the sector cache and cache line zero instructions. In addition, we will refine the ECM model with a more accurate saturation model using an additional latency term. We will also apply the refined model to the HPCG benchmark and to lattice QCD applications \cite{21}.

### B. Related work

Since the A64FX CPU has only been available for a short time, the amount of performance-centric research is limited. DONGARRA \cite{22} reports on basic architectural features, HPC benchmarks (HPL, HPCG, HPL-AI), and the software environment of the Fugaku system. JACKSON et al. \cite{23} investigate some full applications and proxy apps in comparison to Intel and other Arm-based systems but do not use performance models for analysis.
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