Fast transient high-performance low dropout regulator with push-pull technique

Zhikui Duan¹,⁵, Xiaomeng Zhao², Qiushi Li³, Guo Niu¹, Jianguo Hu⁴, Xiucai Wang¹, Jianwen Chen¹ and Xingbo Wang¹

¹School of Electronic Information Engineering, Foshan University, Foshan, 528000, China;
²Guangdong Provincial Key Laboratory of High Performance Computing, Guangzhou, 510033, China;
³Guangdong Productivity Promotion Center, Guangzhou, 510033, China;
⁴Development Research Institute of Guangzhou Smart City, Guangzhou, 510800, China;
⁵E-mail: duanzhikui@outlook.com

Abstract. A fast transient response low dropout (LDO) regulator based on push-pull structure is presented in this paper. The push-pull circuit sampling the output of the LDO and adjusting the gate voltage of the power MOSFET by push-pull current. The slew rate of the power MOSFET gate is accelerated and the transient response performance is improved. With a 1μF decoupling under 180 nm CMOS technology, the proposed LDO exhibits an excellent transient performance. When the workload changes steeply between 100μA and 20mA in 100ns, the overshoot is 10.176mV and undershoot is 10.795mV with the recovery time are 1.272μs and 0.888μs respectively.

1. Introduction
In recent years, the number and types of processors have increased on the same die. The trend of multicore is expected to integrate various function blocks requiring varying supply voltages. The various supply level cause a challenge for voltage regulation. In [1], the voltage regulator can be applied in many cases while limited by its inductors. In addition, linear voltage regulators such as low-dropout regulators (LDOs) have been widely used to supply various voltage level. The LDOs are very popular in power management IC design for their simple circuits, fast response and low ripple output voltage. The typical LDO structure is based on analog circuits such as bandgap, amplifier etc. Many works [2-7] focused on improvement of performances with analog technique by flipped-voltage-follower, new compensation methodology, new error amplifier, new compensation circuits etc. However, the analog-LDO based on the typical structure adjust the output voltage by the reference voltage and feedback network. Therefore, the output voltage can be described as \( V_{\text{ref}} \times K \) (K>1) and cannot be lower than 1.24V. As the power supply voltage level is becoming lower for mobility applications. The analog LDOs are limited by bandgap or amplifier which needs multiple threshold voltage power level.

In [8-9], a dual-mode LDO with digital power gate and analog control loop was demonstrated, which utilized capacitance multiplication to drive load and could work at lower power level. However, the dual-mode LDO needed complex circuits and large layout area that is not suitable for power and...
area sensitive applications. Therefore, digital LDOs in [10-12] were presented which used digital control methods such as cycle control, 1bit modulation, digital power gate etc. to generate a desired output voltage level. The digital LDOs also have their weaknesses such as transient response, working limited by clock etc. In addition, digital LDOs have some residual ripple on the output, and the accuracy is lower than the analog LDOs.

This paper presents a novel analog LDO with push-pull structure and enhanced response performance. The enhanced response method was used to limit undershoot and overshoot, making this a simple circuit for low ripple power management.

2. Proposed LDO architecture and analysis

The output voltage of a typical LDO is determined by the reference voltage and feedback network. Its transient performance is limited by the size of the power transistor and the loop gain bandwidth. To achieve a flexible output voltage and fast response, the push-pull technique is adopted with current reference.

According to the Figure 1, the proposed LDO has a simple push-pull structure that includes transistors M6–M11, and bias circuit. In the push-pull circuit, M6 samples the feedback voltage signal and converts into current signal, M7–M8 amplified the current signal by $K_3$. M9 responds the feedback voltage by the M6, and varies its current at the gate of the power MOSFET (Mp). The current of M8 changes inversely with the current of M9 when the output voltage changing. The current reference $I_{\text{ref}}$ is amplified by the cascade current mirror with coefficient $K_1$. And then, the amplified current becomes the bias current in M11. In the same time, $I_{\text{ref}}$ is also biasing the transistor M10. When the output voltage rises suddenly, the gate voltage of M6 rises and its current increases suddenly. Therefore, the current of M7 and M8 rise too. In the same time, the gate voltage of M9 drops and its current decreases with it. In this way, the gate voltage of the power MOSFET rises transiently by the push-pull effect, and its slew-rate is improved. It is the same way when the output voltage drops. In addition, the transistors M12-M13 sample the output voltage and generate feedback signal $V_{\text{fb}}$. The parameters $C_L$ and $R_L$ are workload.

![Figure 1. The proposed LDO with push-pull technique.](image)

The output voltage of the LDO can be described as the Eq. (1).

$$V_{\text{out}} = \frac{V_{\text{thn}}}{K_p} \frac{K_1 \mu C_{\text{ox}} (W/L)_{n6}}{K_p} + \frac{K_2 K_3 I_{\text{ref}}}{K_p}$$

In which, $K_1 = \frac{W_1}{L_{n6}}$, $K_2 = \frac{W_2}{L_{n5}}$, $K_3 = \frac{W_3}{L_{n7}}$.

According to the Eq. (1), the output voltage is determined by the current reference $I_{\text{ref}}$, threshold voltage $V_{\text{thn}}$, the ratio of transistors and the size of M6. $I_{\text{ref}}$ and ratio of transistors are stable, therefore
the output voltage is influenced by the threshold voltage $V_{thn}$. The Monte Carlo analysis is needed to check the variation range of the output voltage. As shown in the Figure 2, the main variation range is 0.71–0.77V (0.74 ± 0.03V), and there are only a few points deviation from the expected value.

![Figure 2. The Monte Carlo analysis of the proposed LDO.](image)

The small signal model can be described as the Figure 3. The parameters $g_{m6}$ and $g_{m9}$ is the transconductance of M6 and M9 respectively. $C_{int}$ is the gate capacitor of the Mp, $G_{mp}$ is the transconductance of Mp. As the current of transistors M8 and M9 change reversely, the effect of them accelerates the transient response of the power MOSFET. Therefore, the push effect should add the pull effect which is shown in the small signal model.

![Figure 3. The small signal model of the proposed LDO.](image)

The closed loop transfer function of the proposed LDO is expressed in Eq. (2).

$$H(s) = \frac{G_{mp}R_I K_{fb} g_{m6} (g_{m9} r_{o7} + K_3)}{C_{int} C_{int} R_L s^2 + C_{int} s + G_{mp} R_I K_{fb} g_{m6} (g_{m9} r_{o7} + K_3)}$$

In the Eq.(2), the expression of $H(s)$ is the standard format of a second-order closed loop control system. Therefore, the damping ratio $\zeta$ and natural frequency $\omega_n$ can be described as Eq.(3) and Eq.(4) respectively.

$$\omega_n = \frac{G_{mp} K_{fb} g_{m6} (g_{m9} r_{o7} + K_3)}{C_{int} C_{int}}$$

$$\zeta = \frac{1}{2R_I} \sqrt{\frac{C_{int}}{G_{mp} K_{fb} C_{int} (g_{m9} r_{o7} + K_3)}}$$

The parameter $\zeta$ describes the stability of the proposed LDO, and $\omega_n$ describes the transient response performance of loop. The value of $\zeta \cdot \omega_n$ is stationary when the workload and the size of the power MOSFET is determined. In these conditions, $\zeta$ and $\omega_n$ determined by $K_{fb}$, $K_3$, $g_{m6}$, $g_{m9}$, and $r_{o7}$.
The parameter $r_o7$ is the equivalent impedance of transistor M7. Therefore, the transient performance of the LDO can be improved by tuning these parameters and tradeoff between $\zeta$ and $\omega_n$. Generally, the value of $\zeta$ is about 0.707–1, and $\omega_n$ can be fast enough.

3. Simulation results and evaluation

The proposed LDO is designed and simulated in 180nm CMOS process, of which the output voltage is 0.74V, the workload range is 100µA–20mA as is shown in Figure 4. According to the Figure 4, when the workload changes from 100µA to 20mA in 100ns, the undershoot is 10.795mV, and the response time is 888ns; when the workload changes from 20mA to 100µA in 100ns, the response time is 1.272µs and the overshoot is 10.176mV.

![Figure 4. The transient response of the proposed LDO.](image)

In addition, different process corners and temperature variations on the proposed LDO can change the output voltage which is shown in Figure 5–6. According to the Figure 4–6, the output of the proposed LDO is changed with different conditions, as shown in Table 1.

![Figure 5. transient response of the proposed LDO in ss corner.](image)
Figure 6. transient response of the proposed LDO in ff corner.

Table 1. Comparison of different corners.

| Parameters                | TT   | SS  | FF  |
|---------------------------|------|-----|-----|
| Undershoot (mV)           | ≈ 11 | 18.2| 23.1|
| Overshoot (mV)            | 10   | 17.9| 21.4|
| Response-time-U (µs)      | 0.888| 1.655| 1.437|
| Response-time-O (µs)      | 1.272| 1.674| 1.574|
| Output voltage (V)        | ≈ 0.73| 0.78| 0.7 |
| Load Reg. (mV/mA)         | 0.5  | 0.895| 1.07|

As is shown in the Table 1, the performance of LDO changes with difference corner. The ss corner describes slow model of transistors and ff corner describes fast model of transistors. The undershoot is 18.2mV and response time is 1.655µs; the overshoot is 17.9mV and response time is 1.674µs at the ss corner. In this corner, the temperature is -30 °C with slow-slow model. When the process corner is fast-fast model and temperature is 120°C (Figure 6), the undershoot is 23.1mV and response time 1.437µs; the overshoot is 21.4mV and response time is 1.574µs. The tradeoffs among the performances of the proposed circuit is made in TT corner and room temperature, and the best results are achieved in TT corner and room temperature too. When the process corner and temperature change, the results of tradeoffs are degenerate. Therefore, the transient performance of the LDO in TT corner is better than the other corners.

To make a comparison, a figure-of-merit (FOM) of LDOs is defined in [13] and widely adopted by other researchers. It is described in Eq.(5). The Table 2 shows the comparison among the other works. According to the table, this work has advantages in workload and transient response performances. All these data show that the proposed LDO with push-pull technique has excellent transient performance.

\[
FOM = T_R \frac{I_Q}{I_{MAX}} \frac{C_n \Delta V_{out}}{I_{MAX}} \cdot \frac{I_Q}{I_{MAX}}
\]  
(5)

Where \( I_Q \) is the quiescent current, and the response time \( T_R \) is determined by capacitor, load-transient glitches of the output voltage and the maximum load current.
Table 2. Comparison of state-of-art LDOs.

| Parameters          | Ref.[7] | Ref.[11] | Ref.[12] | This work |
|---------------------|---------|----------|----------|-----------|
| Tech. (µm)          | 0.18    | 0.065    | 0.065    | 0.18      |
| $V_{in}$ Range (V)  | 1.6–2   | 0.6–1.1  | N/A      | 1–1.8     |
| $C_L$ (nF)          | 0.6     | 1        | 100      | 1         |
| $I_{load_{-}max}$ (mA) | 10     | 100      | 6        | 20        |
| $I_Q$ (µA)          | 265     | 82       | 100      | 27        |
| Undershoot (mV)    | ≈45     | 55       | 165      | ≈11       |
| Overshoot (mV)     | ≈45     | 47       | 44       | 10        |
| Settling Time (µs) | 0.3     | 0.7      | N/A      | 0.89      |
| Load Tran. $t_c$ (ns) | 500   | 20       | N/A      | 100       |
| Load Reg. (mV/mA)  | 4       | 0.55     | 7.3      | 0.5       |
| FOM (ps)           | N/A     | 0.43     | 1.22     | 0.675     |

4. Conclusions
LDO is widely used in power management units of circuits and systems for its fast transient response and low output ripples. This work present novel LDO with push-pull structure that improve the slew-rate of the gate voltage of the power MOSFET. The analysis and simulation results show that the proposed LDO exhibits fast transient performance and stability.

Acknowledgments
This work is supported by the State Key Laboratory of Mathematical Engineering and Advanced Computing under Open Project Program No.2017A01, Department of Guangdong Science and Technology under project 2015A010104011, the 2016 Guangzhou Innovation and Entrepreneurship Leader Team under grant CXLJTD-201608, Foshan Bureau of Science and Technology under projects 2016AG100311, Project gg040981 and gg041013 from Foshan University. The authors sincerely present thanks to them all.

References
[1] Kurd N, et al. 2014 Haswell: a family of IA 22 nm processors IEEE Solid-State Circuits Conf. (ISSCC) pp. 112–113
[2] Lu Y, Wang Y P, Pan Q, Ki W H, and Yue C P 2015 A fully-integrated low-dropout regulator with full-spectrum power supply rejection IEEE Trans. Circuits Syst. I, Reg. Papers vol.62 pp. 707–716
[3] Kim Y and Lee S S 2013 A capacitorless LDO regulator with fast feedback technique and low-quiescent current error amplifier IEEE Transactions On Circuits and Systems: Express Briefs Vol. 60 No.06 pp. 326–330
[4] Pérez-Bailón J, Márquez A, Calvo B, Medrano N and Martínez P A 2017 Fast-transient high-performance 0.18 µm CMOS LDO for battery-powered systems Electronics Letters Vol.53 No. 8 pp. 551–552
[5] Magod R, Suda N, Ivanov V, Balasingam R and Bakkaloglu B 2017 A low-noise output capacitorless low-dropout regulator with a switched-rc bandgap reference IEEE Transactions On Power Electronics Vol.32 No. 4 pp. 2856–2864
[6] Ho M, Guo J, Mak K H, Goh W L, Bu S, Zheng Y, Tang X and Leung K N 2016 A CMOS low-dropout regulator with dominant-pole substitution IEEE Transactions on Power Electronics Vol.31 No. 9 pp. 6362–6371
[7] Zarate-Roldan J, Wang M, Torres J and Sánchez-Sinencio E 2016 A capacitor-less LDO with high-frequency PSR suitable for a wide range of on-chip capacitive loads IEEE Transactions on Very Large Scale Integration (VLSI) Systems Vol.24 No. 9 pp. 2970–2983
[8] Luria K, Shor J, Zelikson M and Lyakhov A 2015 Dual use low-dropout regulator/power gate
with linear and on–off conduction modes for microprocessor on-die supply voltages in 14 nm IEEE Int. Solid-State Circuits Conf. (ISSCC) pp. 156–157

[9] Luria K, Shor J, Zelikson M and Lyakhov A 2016 Dual-mode low-drop-out regulator/power gate with linear and on–off conduction for microprocessor core on-die supply voltages in 14 nm IEEE J. Solid-State Circuits vol.51 No. 3 pp.752–762

[10] Huang M, Lu Y, Sin S W, U S P, Martins R P and Ki W H 2016 Limit cycle oscillation reduction for digital low dropout regulators IEEE Transactions on Circuits and Systems—II: Express Briefs Vol.63 No.9 pp. 903-907

[11] Huang M, Lu Y, Sin S W, U S P and Martins R P 2016 A fully integrated digital LDO with coarse–fine-tuning and burst-mode operation IEEE Transactions on Circuits and Systems—II: Express Briefs Vol.63 No.7 pp. 683-687

[12] Song H, Rhee W, Shim I and Wang Z 2016 Digital LDO with 1-bit ΔΣ modulation for low-voltage clock generation systems Electronics Letters Vol.52 No.25 pp.2034–2036

[13] Hazucha P et al. 2005 Area-efficient linear regulator with ultra-fast load regulation IEEE J. Solid-State Circuits vol.40 no. 4 pp.933–940