Survey on Field Programmable Analog Array Architectures Eliminating Routing Network

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ABSTRACT This work focuses on reviewing the field programmable analog array (FPAA) architectures that eliminate the use of switches in signal path. The conventional FPAA architecture is composed of configurable analog blocks (CABs) connected together through switches in routing networks. The architectures covered in this survey have replaced the use of routing network by direct connection between CABs, and use of programmable analog building blocks. The first architecture covered is presented by Becker et al. with a hexagonal topology using operational transconductance amplifier (OTA) as a building block. The second architecture is presented by Mahmoud and Soliman, which uses the second generation current conveyor (CCII+) as a building block for their CABs arranged in a hexagonal architecture as well. Lastly, a more recent FPAA with a rectangular architecture proposed by Diab and Mahmoud is discussed, it uses the OTA as a building block for their rectangular architecture. The three FPAAAs targeted continuous-time analog signal processing, having two architectures targeting high frequency applications, while the last targeting low frequency applications. The architectures, CAB structures, and the applications of each FPAA is covered separately in each section.

INDEX TERMS Continuous-time, field programmable analog array (FPAA), filters, operational transconductance amplifier (OTA), second generation current conveyor (CCII+), signal processing.

I. INTRODUCTION

In the field of microelectronics, high level of integration, rapid prototyping, lower product cost, and design time are important traits of modern circuit design. Therefore, reconfigurable programmable platforms such as field programmable arrays have been used as a single device for the implementation and prototyping of several circuits and systems. For digital circuits, the field programmable gate arrays (FPGA) have been well established and designed for use. As for the analog circuits, different field programmable analog arrays (FPAA) are used. The FPAA design and architecture is still in continuous development having limited market with few commercial products, one of the reasons is due to the lack of general purpose CAD tools fitting all FPAAAs. When considering the implementation of an analog signal processing circuit, there are several analog blocks available as options, this means there are numerous implementation methods for the same signal processing circuit. With it is mapped using an operational amplifier, transconductance amplifier, current conveyor, or others, it is difficult to have a generic CAD tool used in mapping of analog signal processing circuit. This is due to the various possibilities available based on the used analog building block, CAB structure, connection between CABs that set the overall FPAA architecture, hence the need for a specialized CAD tool for reconfiguration.

The FPAA is composed of basic analog processing blocks arranged to provide a configurable analog block (CAB) as the main component of the FPAA connected to other CABs through routing network. One of the reasons behind the continuous development of the FPAA architecture is the presence of various possible components in different arrangements to realize analog signal processing circuits. Thus, multiple FPAA architectures with different CAB structure, number, topology, and routing networks are present. Another reason behind the different available architectures is attributed to the application of the FPAA itself, wither it targets high or low frequency application. In general, FPAA architecture can be categorized based on different characteristics, such as commercial FPAA or academic research FPAA. They can also
be categorized based on the analog block used, or the nature of the analog signal processed either continuous-time (CT) or discrete-time (DT). For DT FPAA, switched capacitor (SC) are mostly the technology used in the design of FPAA, hence the FPAA manifests similar advantages and disadvantage to SC circuits [1].

Various commercial FPAAAs were developed for the industry and were successful in application fields, some of them seized to exist, while others were developed. The most widely known FAA provider nowadays is Anadigm. However, looking back at the development of FPAAAs, one of the oldest FPAA structure is the DPAD2 FPAA which was developed by Pilkington Microelectronics Ltd. (PMeL), and designed by B. C. Macbeth [2]. The DPAD2 had a famous structure of 20 CABs arranged in 4 × 5 grid topology, with a hierarchical routing scheme. The basic units for signal processing were the operational amplifiers (op-amps). This FPAA design later became an inspiration for the other uprising FPAA chips developed by both Motorola and Anadigm. Motorola released their first FPAA MPAA020 [3] in 1997. The MPAA020 had an improved hardware compared to DPAD2, however, it did not differ conceptually. As for Anadigm, the first FPAA was released in 2000, the AN10E04 [4] which is somehow similar to DPAD2 in the topology of 4 × 5 CAB, but with improved internal connectivity using more switches and tunable capacitors. The second generation was released in 2003, the AN120E04 [5] and AN121E04 [6], both consisted of 2 × 2 CAB structure utilizing the SC techniques which improved the bandwidth of chips. Both chips are similar at core, only AN121E04 has more I/O cells. The dynamically programmable Analog Signal Processor (dpASP) is another line provided by Anadigm which can be used in place of their FPAA in specific applications [7]. The main advantage of dpASP FPAA over the other FPAA provided by Anadigm, is the real time reconfigurability of the chip, as opposed to the FPAA chips requiring reset before loading of new configuration. The FPAA provided by Anadigm can be reconfigured using the AnadigmDesigner2 EDA software, where configurable analog modules (CAMs) are presented as building blocks to build certain analog function.

As for the academic research FPAAAs, they tend to fall under CT design structure opposing the commercially available DT based FPAAAs. This choice of CT FPAA is attribute to the need of oversampling in DT circuits which restrains its high-frequency application. The different available CT FPAA architectures presented over the years are discussed in the following section.

The covered FPAA architectures wither commercial or academic, have all used switches as routing networks for the reconfiguration of the FPAA, with most FPAA having a checkboard and cross bar pattern architecture. Considering the use of routing network requires great attention, as signal routing network needs to be flexible and generic as possible for maximum efficiency of the architecture [8]. Therefore, the classical topology used was mostly based on checkboard pattern with global and local interconnection networks. Although such patterns provide high flexibility allowing point-to-point connection, they require a lot of space for the global channel and it degraded the signal due to switches present in signal path. Moreover, depending on the used switching network, different values of parasitic capacitance is added to I/O ports of CABs which in turn affects the frequency response of the chip. Due to the drawbacks of using switches in routing network, FPAA architectures eliminating the use of routing networks through direct connections of CABs and programmable analog blocks were developed, however they are still not given enough attention. Hence, the motivation behind this survey is to shed some light on switch-less FPAAAs found in the literature and their architectures.

This paper covers three main FPAA architectures eliminating the need for routing network in signal path. At first, it reviews some CT FPAA architectures with routing networks in section II. Next, it discusses the FPAA architectures eliminating the routing network. The first FPAA architecture is covered in section III, having a hexagonal structure with OTA based CABs. The next architecture discussed in section IV also has a hexagonal architecture, however uses current conveyor based CABs. Finally, the third architecture presents a rectangular OTA based FPAA in section V. Discussion and conclusion of the surveyed architectures is provided in section VI.

II. CONTINUOUS-TIME FIELD PROGRAMMABLE ANALOG ARRAYS WITH ROUTING NETWORK

This section covers some famous FPAA architectures presented in the past decades, highlighting the different CAB building blocks, switching networks, and overall architecture. Some CABs were designed based on different active circuits such as op-amps [9]–[11], operational transconductance amplifiers (OTA) [8], [12]–[25], current conveyors (CC) [26]–[31], current feedback amplifier (CFOA) [32], and some built using simple circuits like differential amplifier and current mirrors [33]–[35]. As mentioned earlier, the FPAA is composed of the CABs and the interconnecting routing network between them, both of which are interdependent on the function desired. The signal routing network needs to be flexible and generic as possible for maximum efficiency of the architecture. While the core of the CAB should be chosen such that its building block does not limit the applications of the designed FPAA. Beside the building block in the CAB, there may also be some passive and reactive elements (resistors and capacitors) that are needed for the realization of certain signal processing circuits. This section overviews some selected FPAA architectures categorized based on the active building block of the FPAA’s CAB.

A. OP-AMP BASED FPAA

One of the very first FPAA designs was introduced in 1991 by Lee and Gulak, for the implementation of neural networks in hardware. It used sub-threshold technique and an “area-universal” fat tree for the interconnection network. The
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FIGURE 1. op-amp based FPAA architecture (a) FPAA architecture (b) CAB structure [10].

The final FPAA design featured two CABs and one interconnect switch block [9]. Further development on the design focused on decreasing the parasitic effect of the switching blocks through the use of transconductor based connection cell in place of pass-transistor switches [10]. The transconductor was used as a switch/linear resistor. The resulted architecture of the FPAA is given in Fig. 1, composed of four CABs, eight variable resistor interconnect network (VRIN), three programmable capacitor array (PCS), and six signal controlled interconnection network (SCIN), which are connected through configurable crossbar switches. The CAB’s is an operational amplifier (op-amp) with feedback capacitor used to in tuning the range of the RC time constant. The FPAA power dissipation is less than 80 mW, and it was used in realizing fourth-order filter, voltage controlled oscillator, and four quadrant multiplier.

B. OTA BASED FPAA

Other FPAA designs were based on the use of OTA as the active building block of the CAB. Here, some of those FPAA architectures that have been presented over the years are reviewed. An OTA based FPAA array of 40 CABs arranged in a 5 × 8 matrix was presented in [14], [15]. The CAB structure is shown in Fig. 3, where it is composed of a 5-bit programmable OTA with 5-bit programmable capacitor array connected through MOS switches. The OTA transconductance is controlled by varying both the biasing current source and voltage control signal. A sixth-order band pass filter was realized as an application for the FPAA with maximum resonant frequency of 60 kHz and power dissipation of 40 mW. Another implementation of a fourth-order band pass filter with resonance frequency of 0.5 MHz reported a power dissipation of 49 mW.

Another OTA based FPAA was developed with a 3 × 3 matrix of configurable analog cells (CACs), that are directly connected to their neighbors as shown in Fig. 4 [17]–[19]. The CACs are active folded cascode current integrator that form together OTA-C filters, where switches in the signal path are set by a shift register to configure the routes both orthogonal and diagonal. The middle CAC has its output connected to the neighboring eight CACs. A bi-quad filter was realized using the FPAA with tunable center frequency ranging from 30 kHz to 10 MHz.

An OTA FPAA architecture using floating gate technology for routing network known as Reconfigurable Analog Signal Processor (RASP) is presented and developed in [20]–[24]. This work was developed over the years starting with an architecture of two CABs with one matrix-vector multiplier, three OTAs, one op-amp, and one current conveyor per each interconnection. The switches were simple pass transistors. The FPAA was used to realize a subtractor, adder, adder with gain and pulse waveform generator. The maximum frequency of the proposed FPAA based applications was 1 MHz [11].

FIGURE 2. op-amp based FPAA architecture using adder and subtractor [11].

Another FPAA with op-amp based CAB structure is presented in [11]. The op-amp is accompanied by passive elements array to realize closed loop voltage amplifier (an adder) and integrator (a subtractor). The FPAA architecture is shown in Fig. 2, where the adder and subtractor blocks are configured through switchable resistor network. A crossbar network using multiplexer switch boxes was used for CABs

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CAB, utilized floating-gate transistors technique for tunability [20]. Implementation of the FPAA with some minor modifications to its CAB was reported in [21], [22], and showing the routing network in Fig. 5. Further improvements led to an array of 7 × 8 CABs, using the floating gate technology for the switching network [23], with limited bandwidth of 6 MHz.

FPAA based on Digitally Controlled Balanced output OTA (DCBOTA) was designed in [25]. The main blocks of the CAB are the DCBOTA and capacitor arrays used for the implementation of analog circuits. As for signal routing, multiplexers and shift registers were utilized. The CAB structure is shown in Fig. 6, with an FPAA architecture of 4 × 4 matrix as shown in Fig. 7. A tunable variable gain amplifier (VGA) and a sixth-order tunable low-pass filter were realized using the FPAA, reaching a frequency response of a few mega Hertz.

C. CC BASED FPAA

The previously mentioned op-amp based FPAA in [10] was further developed to improve the bandwidth from few MHz to more than 10 MHz through the use of current conveyor (CC) and programmable capacitors [27]. The CAB was made of second generation current conveyors (CCII+), OTA based resistors, and CCII+ based capacitor. The CABs had direct connection to one another, but constraining the signal path to specific routes. The CABs were controlled through the voltage supply as their previous FPAA. It is reported the design using four CABs achieved a bandwidth of 11 MHz, and dissipated power of 162 mW [28]. Another FPAA based CCII+ design is also introduced, where it eliminates the need for switching network and provides three different possible designs for the FPAA, this is covered thoroughly in section IV.

D. MIXED ACTIVE CIRCUITS BASED FPAA

Some researchers used more than one active circuit in the FPAA structure. For instance, a CCII+ and a voltage op-amp were used to realize a voltage/current mode CAB in [34]. A differential difference amplifier (DDA) and a CCII+ were combined together to realize a CAB shown in Fig. 8. The FPAA was formed from four CABs connected via double-pole-double-throw switches. A current mode Schmitt Trigger and a voltage controlled oscillator were realized using the FPAA. The application’s maximum frequency was a few kHz [34].

A FPAA based on fully balanced four terminal floating nullor (FBFTFN) was presented in [35]. The FBFTFN is a combination of differential difference voltage op-amp and a CCII. It has two input voltage terminals and two output
current terminals. The voltage applied at one of the input terminals is buffered to the other input terminal while the current at one of the output terminals is sensed and transferred to the other output terminal in the opposite direction. The CABs consisted of FBFFTN in addition to programmable resistor and capacitor arrays. The CABs were connected via switch boxes. The switches were configured using digital code word stored in a shift register located in each CAB. The FPAA and its CAB structure are shown in Figs. 9 and 10 respectively. The FPAA was used to realize a non-inverting amplifier and a Sallen-Key filter.

III. HEXAGONAL OTA FIELD PROGRAMMABLE ANALOG ARRAY

A. ARCHITECTURE

The first architecture to be discussed in this paper to break free from the conventional crossbar CAB structure in designing the FPAA, was introduced and developed by Joachim Becker et al. [8], [13]. The FPAA presented an architecture eliminating the need for routing network between CABs, as opposed to the previously discussed FPAA architectures requiring running network of switches for local and global routing. The FPAA architecture had a hexagonal structure for the CABs allowing direct connection between...
each other, hence eliminating the need for switches. The hexagonal topology adopted for the FPAA architecture provided the authors with desired features such as cascading, feedback, and flexibility of design whilst avoiding drawbacks of only even order feedback as presented by chessboard topology. The adopted topology of hexagonal arrangement of CABs is demonstrated in Fig. 13, where multiple hexagonal CABs, as those numbered 1 to 4, can be placed next to each other. The layout provides cell symmetry allowing the connection of one cell to the others in all directions providing direct connection between CABs and eliminating the need for local and global networks. Hence, the desired path for a signal can be chosen by passing through neighboring CABs to reach final destination.

For the purpose of implementing analog filters on a hexagonal reconfigurable platform, signal propagation through current mode was chosen over voltage mode. The choice was driven by the property of current summation at node of parallel connections. The need for active analog filter building block, with voltage input and output current, the operation transconductance amplifier (OTA) was chosen for the implementation of filters on the FPAA. The output current of the Gm–cells were integrated over a capacitor to provide voltage as input for the next Gm–cell in the signal path [8]. Further details of the Gm–cell, the building block for CAB, will be covered in the following subsection.

As mentioned earlier, the routing signal network was eliminated by the direct connection of the CABs, as opposed to the analog switches used in earlier designs to reconfigure the signal path. The effect of using switches was projected on the achievable bandwidth due to the non-linearity presented by the analog switches implemented through transmission gates, where the bandwidth was decreased as effect of parasitic. Therefore, the work in [8] presented a solution through the use of programmable OTAs for switching desired OTAs on and off arranged in a hexagonal architecture for direct connectivity. Fig. 14 shows the hexagonal topology using 7 CABs, with the local OTA interconnect and the integrating capacitor [8].

B. CAB STRUCTURE

Taking a closer look into the OTA based hexagonal FPAA architecture, this subsection reviews the design of the CAB. In the design of the CAB for FPAA targeting higher bandwidth, the authors replaced the use of physical capacitors (as shown in Fig. 14) with the parasitic capacitance of both input and output stages of the Gm-cells of the CAB. The collected current at the node is then integrated by the capacitance, which is formed of the input parasitic capacitance of the 7 internal Gm-cells and the output parasitic capacitance of the external Gm-cells. This resulted voltage is then used as an input to Gm-cells of the CAB when turned on. The voltage input is trans-conducted to current output which is used to drive the neighboring CAB based on switched Gm-cells. At the center of the CAB, there is a Gm-cell used for first order self-feedback, a buffer to pad which allows low impedance buffer to an output pad, if output is desired to be taken at this node, and a common mode feedback (CMFB) circuit to control the voltage level of the output. Hence, with this structure, each CAB center is considered a voltage node, due to the summing ring that integrates the current onto the parasitic capacitor. In the implementation of filters, the voltage across the capacitor can be considered as a state variable, while the transconductance of the Gm-cell as filter parameter. The OTAs are switchable, providing an initial path where all OTAs are off, thus they can be turned on and the transconductance be tuned. A single Gm-cell is formed by the parallel connection of 6 OTAs, this arrangement allows the transconductance to be tuned based on the number of OTAs switched on, which in turn affects the bandwidth. The final hexagonal FPAA architecture is shown in Fig. 16 where it is composed of 7 CABs, 1 center and 6 edge CABs circling the center one. Each CAB has 7 Gm-cells, where the middle cell provides first order self-feedback, and there are 6 additional Gm-cells used for input thus making a total of 55 tunable Gm-cells for the FPAA architecture [8].

![Hexagonal topology layout.](image1)

![Hexagonal topology with OTA interconnect and integrating capacitor.](image2)
The OTA hexagonal FPAA architecture was implemented using 0.13 \( \mu m \) CMOS technology, targeting high frequency application. The FPAA was successful in implementing different circuits. The architecture allows the mapping of a single filter of maximum order seven, or two filters of third and fourth-order. A sixth-order band pass filter (BPF) using 3 cascaded biquads shown in Fig. 17 was implemented on the FPAA using 6 out the 7 CABs, as each state variable of the sixth-order requires a single CAB. The mapping of the filter on the FPAA is shown in Fig. 18. The reported resonance frequency ranged from 29 MHz to 82 MHz, with an input referred noise of 14.3 nV/\( \sqrt{Hz} \) at 29 MHz and 14.3 nV/\( \sqrt{Hz} \) at 82 MHz. Moreover, an inverse Chebyshev lowpass filter (LPF) was also mapped using 5 CABs as given in Fig. 19. The input is fed through CAB 7 and distributed through the cells (C, D, and E) to three gyrators, having the final output taken from CAB 5. The reported bandwidth can be tuned between 49 MHz and 79 MHz [8].

Later modification and improvements to the presented hexagonal FPAA architecture were developed to include the use of programmable capacitor array and floating gate designed in 90 nm CMOS technology [36]. The presented modified hexagonal FPAA provided an increased bandwidth of 1 GHz of the Gm-cell, thus allowing the mapping of filters on FPAA with tunable frequencies less than 1 MHz and above 1 GHz [16], [36].

### IV. HEXAGONAL CCII+ FIELD PROGRAMMABLE ANALOG ARRAY

The second FPAA architecture covered in this survey also demonstrates a fully interconnected FPAA architecture eliminating the use of routing networks. This FPAA is based on digitally controlled fully differential second generation
current conveyor (DCFDCII+) and was developed by Mahmoud and Soliman [29]–[31], [37]. The authors of this work presented an FPAA with three different realizations, using two different CAB structures based on current conveyors. The two proposed CABs shared the use of CCII+ as a building block, however differed in the digital control circuit implementation of a current division network (CDN). The first CAB used DCFDCCII+ controlled by CMOS CDN [29], [37], while the other CAB used DCFDCCII+ controlled by MOS ladder CDN [30], [31]. The FPAA architecture adopted for the different realizations was inspired by the previously presented hexagonal lattice arrangement, with switches replaced by direct connection of CABs and digitally controlled FDCCII+.

### A. FIRST FPAA REALIZATION

The first FPAA realization was presented in [29], having 7 CABs with 7 differential input/output pins. The pins of the FPAA can be used as input voltage terminal or output current terminal as shown in Fig. 20. The CABs used to realize this FPAA have the building block as fully differential CCII+ that is digitally controlled by CMOS CDN [38], with programmable factor greater than 1. The CABs can be divided into edge CABs and center CAB, having the edge CABs in different structure than the center one. The CABs at the edges consist of 3 DCFDCCII+ cells, while the center CAB has 6 DCFDCCII+ cells. The DCFDCCII+ block converts input voltage to output current with a transconductance gain based on 3-bit digital code that controls the CDN. The edge CABs with 3 DCFDCCII+, have their input voltage terminal connected to the center of their CAB, while their current output terminal connected to the adjacent CAB’s center (I/O pin). At the center of each CAB, output current terminals from DCFDCCII+ of the adjacent CABs are summed together to form a summing node, at this pin the summed current are converted to voltage through the connection of arbitrary loads at the pin. Thus, providing voltage as an output of the CAB, or as an input signal to the DCFDCCII+ cells inside the CAB. Feedback connection is also provided between CABs 1, 3, and 5 through cell B of CAB 3 and 5 and cells A, and C of CAB 1 [29]. As for the center CAB, the voltage input terminal of the cells is connected to the CAB’s center (I/O pin), while their current output terminal connected to adjacent CAB’s center.

Another architecture is presented using both primary and secondary outputs of the DCFDCCII+ is shown in Fig. 21. The difference between both arrangements of the FPAA is Figs. 20 and 21 is the use of primary and secondary outputs of DCFDCCII+. The primary current output \(Z_p\) cannot be scaled to zero, while the secondary \(Z_s\) can be scaled to zero, hence used as output to the summing node. In this FPAA structure with the output from \(Z_p\), as shown in Fig. 21, the main cell is A with its input terminal Y connected to the I/O terminal of its CAB, while its \(Z_p\) output connected to cell F, which acts as programmable resistive load, and E which has its \(Z_s\) output connected to the adjacent CAB’s I/O pin. Similarly, cell C is connected to G and D, with G as the resistive load, while D connects to the adjacent CAB.

### B. SECOND FPAA REALIZATION

The second FPAA realization was based on a different CAB structure and different digitally controlled current conveyor [31]. The complete FPAA structure is also based on the hexagonal layout with no interconnections, it has

![FIGURE 19. Mapping of inverse Chebyshev LPF on FPAA [8].](image)

![FIGURE 20. Architecture of CCII+ FPAA first realization based on secondary output currents of the DCFDCCII+ [29].](image)
FIGURE 21. Architecture of CCII+ FPAA first realization based on primary and secondary output currents of the DCFDCCII+ [29].

FIGURE 22. Architecture of second FPAA realization based on DCFDCCII+ [31].

7 differential I/O pins acting as either voltage input terminal or current output terminal. The FPAA is shown in Fig. 22. Similar to the previous realization, the center CAB has different structure than the edge CABs. The edge CABs have 4 DPFDCCII+ as building block, which is drawn as single ended for simplicity. The cells A, B, C, and D have their input terminal Y connected to the differential pin at the center of the CAB, while the output terminal Z of A, B, and C is connected to the differential pin of the neighboring CAB. As for the output of D for CABs 1, 2, and 3, it is connected to A of CAB 4, through its terminal X. While output of D of CABs 4, 5, and 6 is connected to A of CAB 1. These connections are made such that multiple feedback connections are possible for mapping on FPAA. As for the center CAB, the input of

FIGURE 23. Architecture of third FPAA realization based on DCFDCCII+ [30].

FIGURE 24. Mapping of sixth-order LPF on third FPAA realization based on DCFDCCII+ [30].
the 6 DPFDCCII+ cells is connected to the differential I/O pin of the CAB, while their output is connected to the I/O pins of the neighboring CABS [31]. The building block used inside the CABS was also a DPFDCCII+ controlled through a 3-bit digital code word. It is composed of 2 CCII+ and a CDN based on MOS ladder unlike the first realization using CMOS CDN. The first CCII+ conveys the input voltage at terminal Y to terminal X, and the current at terminal X is conveyed to terminal Z. The current at Z flows as input to the MOS ladder CDN and then forwarded to the X terminal of the second CCII+ of the DPFDCCII+.

C. THIRD FPAA REALIZATION

Similar to the first two realizations, the third FPAA has a hexagonal lattice as shown in Fig. 23 [30]. The architecture of the FPAA has 7 CABS, where the CABS at the edges have 3 DPFDCCII+, and the center CAB has 6. The 3 DPFDCCII+ cells, A, B, and C at the edge CABS have their Y input terminal connected to the differential I/O pin of the CAB, while their output Z terminal connected to I/O pin of the adjacent CAB. The C cell is connected in a negative feedback connection, to be utilized in the implementation of different filter responses. As for the center CAB, as seen earlier, the DPFDCCII+ inputs are connected to the CAB’s I/O pin, while the output to adjacent CAB’s I/O pin. This realization uses the same building block of the second realization, having the DPFDCCII+ cell composed of two CCII+ blocks with a MOS ladder CDN in between for programmability.

D. APPLICATION

The presented CCII+ based FPAA by [29]–[31], [37] was realized using 90 nm CMOS technology by TSMC, targeting high frequency applications. The different realizations were successfully used in the implementation of different circuits. The first FPAA realization was reported to map a voltage gain amplifier [29], a tunable second-order lowpass filter (LPF) [29], and a tunable second-order Bi-quad filter [37]. As for the second FPAA realization, it was used in mapping a universal filter with digitally programmable cutoff frequency and quality factor [31]. The third FPAA implementation implemented a sixth-order Butterworth LPF [30].

Implementing a voltage gain amplifier requires an output gain greater than 1, therefore it was implemented using the first realization with programmable factor greater than 1. The amplifier circuit was mapped on the FPAA in Fig. 20 using one DCFDCCII+ cell (B1) and a grounded resistor at the output node of CAB 7 [29]. The voltage gain amplifier had a 3 dB bandwidth ranging from 56.3 MHz to 398.1 MHz. The tunable second-order LPF was realized using the FPAA in Fig. 21, using both primary and secondary output currents of the DCFDCCII+. The LPF reported a 3dB bandwidth ranging from 24.3 MHz to 82.2 MHz. The second-order tunable bi-quad filter was mapped on the FPAA in Fig. 21, using three CABS, input through CAB 1, BPF output from CAB 6, and LPF output from CAB 5. The BPF bandwidth was tuned from 0.576 MHz to 4.78 MHz, while the LPF from 16.4 kHz to 11.6 MHz [37].

The second realization of the FPAA in Fig. 22 was made useful due to its multiple feedback routes in the implementation of a second-order universal filter with 3 responses: high pass, low pass, and bandpass [31]. The LPF and HPF had a tunable bandwidth of 2 MHz to 3.5 MHz with a step of 0.5 MHz and the design provided tunable quality factor. Lastly, a sixth-order Butterworth LPF applicable for WLAN/WiMAX receivers was mapped by cascading three
second-order biquad sections. The mapping of the filter on FPAA of Fig. 23 required the use of all the CABs as shown in Fig. 24. Having the input from CAB 1 and the output taken from CAB 2. The three second order LPFs were mapped as follows: (B1, C7, A6), (B6, A5, C4), and (A4, B3, C2) [30], each mapped using the second-order biquad structure shown in Fig. 25. This filter had a tunable bandwidth range of 5.2 MHz to 16.9 MHz, as shown in Fig. 26, and an output referred noise density of 108 nV/√Hz and 100 nV/√Hz at 5.2 MHz and 16.9 MHz respectively [30].

V. RECTANGULAR OTA FIELD PROGRAMMABLE ANALOG ARRAY

A. ARCHITECTURE

A recent FPAA architecture following the trend of eliminating routing networks in signal path was also introduced by Diab and Mahmoud [39]–[43]. The presented FPAA architecture replaces the use of switches by direct connection of CABs and the use of programmable building block similar to the previously discussed architectures. However, this FPAA has a rectangular topology as opposed to the hexagonal, and it uses OTA in the design of the CAB. The rectangular FPAA presented two designs, having the second as an extension of the first with more possible connection for different circuit implementations. The first FPAA realization of the rectangular OTA based FPAA is shown in Fig. 27, where it is composed 16 intermediate CABs, two output CABs, and an “order selecting network”. This first realization architecture allows the implementation of two independent filters of ninth and eighth order, or cascade the filters to maximum order of 16. The FPAA architecture has two differential input pins and four balanced output pins. It integrates a variable gain amplifier (VGA) at the output CAB providing the two balanced output options, amplified and pre-amplified [39], [42].

As for the second realization of the FPAA architecture shown in Fig. 28, it is an extension of the first realization with the addition of a rectangular section having 8 intermediate CABs, VGA CAB, and another “order selecting network”. The added section has two differential input pins, one connected directly through the intermediate CABs for filter circuit implementation, the other connected to the VGA providing amplification of input before processing. As for the output pins, it provides two balanced output pins, one for the VGA, and the other for the mapped circuit. The added section A provides different feedback connection than offered by the other two sections B and C, thus allowing a wider range of circuits to be mapped on the FPAA. All section are connected to one another, allowing cascading of different circuits and the implementation of full system if required [39]–[41].

Both realizations have flexible structures with expandable architecture not presented by the previous FPAA architectures. The rectangular FPAA can be extended horizontally by the addition of intermediate CABs, thus increasing the maximum order for a single filter realization. They can also be expanded vertically by the addition of sections similar to A, or B and C, based on the required feedback and circuit implementation. This expansion allows several independent filter implementation, a filter bank, or a full system implementation composed of multiple signal processing circuits cascaded with one another [39]–[43].
B. CAB STRUCTURE

The rectangular FPAA architecture used the OTA as the building block for the CAB. Each CAB is made of two OTAs with differential input and balanced output. Fig. 29 shows two interconnected CABs. The output of the OTAs within a CAB are joint together, having their output current summed and integrated over a grounded capacitor providing voltage input for the next CAB. Each CAB is connected to adjacent CAB on
both sides, providing direct connection [39], [40]. Required CABs are turned on and the OTAs are set to their corresponding transconductance. Order selecting network uses OTAs as the final stage of the implemented circuit, to decide the order. Only required OTAs are switched on, allowing the passage of signal towards output CAB.

C. APPLICATION

The presented rectangular FPAA was designed in 90 nm BSIM4 CMOS technology, targeting low frequency applications as most available FPAA architectures are focused on high frequency applications. The FPAA was used in the implementation of biomedical signal processing circuits, such as LPF for the acquisition of biopotential signals, BPF for the circuit implementation of continuous wavelet transform, and the analog front-end (AFE) for biopotential signal detection [39]–[43]. Moreover, it was used to map multiple filters with option of cascading or not to provide a bank of tunable filters.

A fourth-order LPF was implemented on the FPAA of the first realization, providing tunable gain, notch frequency, and bandwidth. The reported 3 dB bandwidth of the filter was 133 Hz for electroencephalogram (EEG) signals, 273 Hz for electrocardiogram (ECG) signals, and 467 Hz for electromyogram (EMG) signals as shown Fig. 30 [39], [42]. The input referred noise reported is 19.6 $\mu$V/$\sqrt{Hz}$, which is higher compared to the other FPAA s, but justified as it is operating at low frequencies as opposed to multi-standard applications of the previous FPAA s.

An AFE composed of VGA, fourth-order notch filter, and fourth-order LPF was also implemented on the FPAA using the second realization. The fourth-order notch filter cascaded with the fourth-order LPF used in the AFE is shown in Fig. 31. The mapping of the AFE is shown in Fig. 32, starting with the VGA for signal amplification using the red OTAs followed by the cascaded notch filter (green OTAs) and LPF with VGA at output (blue OTAs). The mapped AFE was designed for the detection of the three biopotential signals, EEG, ECG, and EMG having the same bandwidth reported for the fourth-order LPF, and a notch present at 50 Hz for elimination of power-line interference signal [39]–[41].

Another application using the reported FPAA was demonstrated in the integration of seventh-order BPF for the realization of continuous wavelet transform (CWT) designed in [44] with the circuit implementation shown in Fig. 33. The implementation on the FPAA first realization provided the mapping of two seventh-order BPF with tunable bandwidth ranging from 0.162 Hz to 101 Hz [43] as shown in Fig. 34, with blue OTAs for the first filter, and the orange OTAs for the second filter, both using a VGA of the output CAB.
VI. DISCUSSION AND CONCLUSION

Three FPAA architectures were reviewed in this paper, having two with a hexagonal architecture, while the third with a rectangular topology. All FPAA targeted continuous-time signal processing through the implementation and mapping of analog filters. They all achieved to present a switch-less FPAA architecture by replacing routing networks with direct connection of CABs and the use of programmable analog block wither it is the OTA or CCII+. The OTA in the designs is used to replace physical resistance required for implementation of time constant for the operation of the circuits. To ensure operation with acceptable total harmonic distortion (THD), the design of the OTA should have good linearity working in low voltage, low power region. Therefore, digital tuning is used for the OTA, which does not affect the linearity range of the OTA unlike the analog tuning. This was reflected on the maximum achievable operating bandwidth, the degradation of signal and the overall structure of the FPAA. The first two architectures with hexagonal topology targeted high frequency application, extending the limits of maximum frequency bandwidth with their corresponding topology. While the rectangular FPAA targeted low frequency application, a less addressed area in the design of FPAA. The hexagonal architectures of both OTA and CCII+ based FPAA have a maximum order of 7 for a single filter implementation. While the rectangular FPAA presents a maximum order of 16 if cascaded, and maximum order of 8, and 9 for two independent filters. A summary of all three FPAA architectures is given in Table 1. Moreover, discussing the utilization of the building blocks within a CAB, both hexagonal structure do not always use all building blocks within a single CAB, in contrary to the rectangular FPAA which has the CAB composed of two OTAs that are both operating if the CAB is on, fully utilizing the building blocks within a single CAB. The rectangular FPAA also presents a flexible architecture that can be extended and expanded based on need, by the addition of intermediate CABs increasing the maximum order, or the addition of sections increasing the number of implemented signal processing circuits. Overall, the reviewed FPAA architectures present new possibilities for the general development of the FPAA, proving the possibility of overcoming the drawbacks of routing networks and presenting some guidelines for future improvements. With these interesting and well developed architectures, several applications are possible for implementation in both low and high frequency domain. More interest should be directed towards low frequency FPAA as they are somehow neglected. Furthermore, the next step in the design of FPAA should not only focus on improving available design but also target their industrialization.

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