A study on substrate noise coupling among TSVs in 3D chip stack

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Abstract: A map of Si substrate noise from through-silicon vias (TSVs) is presented by measurement of real stacked test vehicle. A 65 nm CMOS test chip is manufactured and integrated by die-to-die bonding. The stacked test chip is packaged with an organic interposer and mounted on an evaluation board. A thinned Si substrate is excited through $V_{DD}$ and $V_{SS}$ TSVs of noise source circuitry and the noise waveforms are captured by an on-chip evaluation circuitry with 2D mapped probe point on the substrate. The result shows overlapped noise waveforms that as its placement, due to voltage division with Si substrate resistance. A simple Si substrate model is created and employed for first analysis. An analytical result explains measurement result qualitatively including the noise overlapping and cancelling on the Si substrate.

Keywords: substrate noise, TSV, 3D-SIC, on-chip evaluation

Classification: Integrated circuits

References

[1] J. Michailos, \textit{et al.}: “New challenges and opportunities for 3D Integrations,” IEDM (2015) 8.5.1 (DOI: 10.1109/IEDM.2015.7409655).
[2] S. Takaya, \textit{et al.}: “A 100 GB/s wide I/O with 4096b TSVs through an active silicon interposer with in-place waveform capturing,” ISSCC Dig. Tech. Papers (2013) 434 (DOI: 10.1109/ISSCC.2013.6487803).
[3] Y. Araga, \textit{et al.}: “Analysis of on-chip digital noise coupling path for wireless communication IC test chip,” IEEE Trans. Compon. Packag. Manuf. Technol. 4 (2014) 1026 (DOI: 10.1109/TCPMT.2014.2316150).
[4] S. Tanaka, \textit{et al.}: “Analysis of on-chip digital noise coupling path for wireless communication IC test chip,” EMC Compo (2015) 216 (DOI: 10.1109/EMCCompo.2015.7358360).
[5] J. Kim and J. Kim: “Signal integrity modeling and measurement of TSV in 3D IC,” ASP-DAC (2013) 13 (DOI: 10.1109/ASPDAC.2013.6509551).
[6] M. Nagata, \textit{et al.}: “In-place signal and power noise waveform capturing within
1 Introduction

Three-dimensionally stacked ICs (3D-SICs) are expected to be the solution for advanced applications which requires high performance and low power consumption [1]. 3D-SICs provides extremely large scale integration and communication among ICs by through-silicon vias (TSVs) which enables high bandwidth chip-to-chip interface with minimum power loss [2].

In such a densely integrated system, electrical noise interference among power-lines and signals may degrade power integrity (PI) and signal integrity (SI) [3, 4]. As for 3D-SICs, the resistivity of Si substrate and capacitive coupling between a TSV and Si substrate can cause mutual interference among TSVs or TSVs-circuitry. This mutual coupling must be analytically understood for stable operation of the large scale 3D-SICs. There are some reports about SI experiment on transmission lines [5, 6], and PI experiment on large scale power delivery networks (PDNs) in 3D-SICs [7, 8].

In this research, we focus on TSV-substrate coupling and present 2D propagation map of substrate noise excited by TSVs to clarify crosstalk caused by stacked structure. We also present analytical study including a simple lumped component model for consideration of experimental result.

2 Test vehicle design

Fig. 1 shows a diagram of Si substrate noise in the 3D-SICs. In this study, we designed and manufactured two-tier stacked test vehicle with TSVs. The test vehicle is designed with 65 nm CMOS process. A thick tier is fabricated with 65 nm foundry front- (FEOL) and back-end of line (BEOL) process. A thin tier consists of 5 µm diameter via-middle TSVs fabricated at IMEC after FEOL and is followed by IMEC’s 65 nm compatible Cu BEOL process. The wafer with TSVs is thinned down to 50 µm and the TSVs are revealed.
A die-to-die (D2D) face-to-back (F2B) stacking of the thick tier and the thin tier with TSVs is performed through micro-bumps. A more detailed description of the fabrication and stacking process steps can be found in [9].

An on-chip monitors [10, 11] are embedded on the thin tier and probe substrate around TSVs. A clock buffer circuitry on the thick tier is activated as noise source, and $V_{DD}$ and $V_{SS}$ noises by current consumption are generated. The voltage variations on $V_{DD}$ as well as on $V_{SS}$ go through respective metal wires and TSVs over the whole stacked sample, and then couple to Si substrates.

The probing points are located on Si substrate, as shown in the physical layout of Fig. 2. TSVs of $V_{DD}$ and $V_{SS}$ are arrayed and coupled to Si substrate. The probe points of the monitoring circuitry are regularly distributed on the surface of Si substrate with 25 µm x-axis pitch and 25 µm x-axis pitch.

### 3 Measurement

Fig. 3 depicts the measurement setup including the stacked test vehicle. The stacked test vehicle is packaged with an organic interposer and mounted on an evaluation board. The noise source and noise monitoring circuits are clocked by a single signal source and thus synchronized in waveform measurement. A reference
voltage is supplied to the on-chip monitors to detect a sampled target voltage, and sampling timing is shifted by delay line circuitry to acquire transient voltage data. A field programmable gate array (FPGA) controls the reference voltage level and sampling timing, and dumps the transient voltage data to PC.

Fig. 4 shows the substrate noise waveforms acquired by the monitoring circuitry. In Fig. 4(a), the substrate noise waveforms with vertically divided groups are plotted.

Transient voltage variation at the 24 probe points on the thin tier are measured, at the timing of noise source excitation. It is shown that the spike-like noise shape varies among the waveforms at different probe points. We can also see relatively smaller noise around the middle area, considered to be cancelled each other among $V_{DD}$ and $V_{SS}$ waves with voltage division of Si substrate resistance. The waveforms at the left points tend to have upward spikes, while the waveforms at the right points tend to have downward spikes. It is considered for these observations that there is much stronger coupling from the $V_{DD}$ wiring area located in the right hand side, in comparison to the coupling from TSVs of $V_{SS}$ wiring.

In Fig. 4(b), noise waveforms with horizontally divided groups are plotted. We can see larger downward spikes at the top group, and smaller downward spike at the bottom group. We can also see small upper spikes at the points 7, 13, and 19, which is far from the $V_{DD}$ wiring area and close to the $V_{SS}$ TSVs. This tendency is considered to be from the coupling between $V_{SS}$ TSVs and Si substrate around the area.

Through these results, we can consider that substrate voltage is largely affected by the waveforms in TSVs, with overlapping of waveforms and cancelling effect in substrate coupling.

4 Analytical consideration

For analytical consideration of the measured results, we create a Si substrate model consisted of lumped components. Fig. 5 shows the model of the thinned Si substrate with TSVs. The Si substrate is modeled as a meshed resistive network with the associated Si thickness and resistivity. The TSV models are connected to Si substrate model with an explicit capacitor having the capacitance for the oxide surrounding each TSV. The substrate model describes Si substrate area of 440 µm × 160 µm with 5 µm × 5 µm resolution, which includes 50 µm width margin between
the neighboring areas of TSVs and probe points. The right end of the model is connected to the $V_{DD}$ wiring area through capacitance to explain capacitive coupling between the $V_{DD}$ wiring area and the substrate. A current consumption model is created for simple analytical consideration, and connected to $V_{DD}$ and $V_{SS}$ TSVs.
Fig. 6 shows a plot of transient waveforms simulated using the analytical model. In Fig. 6(a), analytical waveforms with vertically divided groups are plotted. We can see the left and the right probing points are largely affected by the noise in TSVs. From small noise spikes around the middle area, the cancellation effect in the measurement is well expressed in the analysis. A smaller V_DD wiring area effect at the right group in the analysis is considered to be from smaller capacitance in the model than the measurements. And a reason of a smaller V_SS coupling effect at the left group in the analysis is considered to be from the smaller V_SS noise than measured one.

Fig. 6(b) shows the analytical waveforms with horizontally divided groups. We can see the waveforms at the top and the bottom probing points are affected by V_DD and V_SS TSVs, respectively, as were seen in the measurements. It is seen that, the coupling strength from the V_SS TSVs is larger than the measurements. This is considered to be from relatively smaller V_DD wiring area effect, as is equivalent in the consideration of Fig. 6(a). From these results, the simple model consists of lumped component can explain the measurements qualitatively. It is important to note that the noise cancellation effect on the thinned Si substrate seen in the measurements are explained by the analysis, as well as the measured result.
5 Conclusion

The mutual coupling among TSVs through Si substrate may degrade PI and SI in 3D-SICs. The noise propagation map on a thinned Si substrate with TSV is presented through an on-chip measurement of real stacked sample. The measured result shows noise waveform variation according to the distance from TSVs, and cancellation by coupling from both $V_{DD}$ and $V_{SS}$ nodes. A simple Si substrate model is created and employed for analytical consideration of the measurements.
The model well explained the noise overlapping and cancellation in the Si substrate coupling. The models need the better accuracy for quantitative simulation of concurrent coupling among TSVs of VDD and VSS to Si substrate, as to be used for noise awareness in 3D stacked chip designs. These are left for future studies.

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