Algorithmic Obfuscation for LDPC Decoders

Jingbo Zhou\textsuperscript{\textcopyright}, Graduate Student Member, IEEE, and Xinmiao Zhang\textsuperscript{\textcopyright}, Senior Member, IEEE

Abstract—In order to protect intellectual properties against untrusted foundry, many logic-locking schemes have been developed. The idea of logic locking is to insert a key-controlled block into the circuit to make the circuit function incorrectly or go through redundant states without right keys. However, in the case that the algorithm implemented by the circuit is self-correcting, existing logic-locking schemes do not affect the system performance much even if a wrong key is used and hence do not effectively protect the circuit. One example is low-density parity-check (LDPC) error-correcting decoders, which are used in numerous digital communication and storage systems. This article proposes two algorithmic-level obfuscation methods for LDPC decoders. By modifying the decoding process and locking the stopping criterion, our new designs substantially degrade the decoder throughput and/or error-correcting performance, and make the decoder unusable when a wrong key is applied. For an example of the LDPC decoder, our proposed methods reduce the throughput to less than 1/3 and/or increase the decoder error rate by at least two orders of magnitude with at most 0.55% area overhead. Besides, our designs are also resistant to the SAT, AppSAT, and removal attacks.

Index Terms—Fault tolerant, hardware security, logic locking, low-density parity-check (LDPC) decoder, stopping criterion.

I. INTRODUCTION

LOGIC locking [1] helps to protect intellectual properties (IPs) of circuits by inserting key-controlled components. The circuit does not function correctly without inserting the right key. Among oracle-guided attacks, the satisfiability-based (SAT) attacks [2] are the most powerful [3]. The main idea of the SAT attack is to apply Boolean SAT solvers iteratively to find distinguishing input patterns (DIPs), which are included to exclude wrong keys. Many logic-locking schemes, such as those as in [1] and [4]–[8], have been decrypted by the SAT attack. The Anti-SAT [9] and SARLock [10] schemes make the number of iterations needed by the SAT attack exponential. However, both of them are composed of large AND/NAND trees, which make them subject to the approximate (App-) SAT attack [11]. In addition, the large AND/NAND trees can be identified and replaced by removal attacks [12], [13]. By increasing the corruptibility of all wrong keys, the diversified tree logic (DTL) design [11] achieves better resistance to the AppSAT attack at the cost of degraded resilience to the SAT attack. Different from the Anti-SAT and SARLock designs that have no overlap among the sets of wrong keys excluded by different DIPs, the Generalized (G-) Anti-SAT design [14] allows overlap among the wrong key sets. It can be built by using a large number of possible functions instead of AND/NAND trees and is more resilient to removal attacks. Besides, it achieves better resistance to the AppSAT attack without sacrificing the resistance to the SAT attack. The recently proposed Cascade (CAS)-Lock scheme [15] is a special case of the G-Anti-SAT design.

The stripped functionality logic locking (SFL) [16] scheme corrupts the original circuit and adds a logic-locking block to correct the corrupted circuit when the right key is applied. The circuit does not function correctly if the key-controlled block is removed and its output is replaced by a constant signal. Hence, the SFL can more effectively resist removal attacks. However, the functional analysis on logic locking (FALL) [17] and Hamming distance (HD)-unlock method [18] can successfully attack the SFL by analyzing its functional and structural properties.

In systems that are fault-tolerating or self-correcting, errors forced on the signals may not affect the overall output or may get corrected by later computations. Examples are low-density parity-check (LDPC) codes [19], machine learning, and applications that are amiable to approximate computing. For the circuits implementing these algorithms, even if a logic-locking scheme is used and a signal is flipped when wrong keys are applied, the errors resulted at the overall output may be negligible. To substantially increase the output error when the key is incorrect, the obfuscation scheme needs to be designed using the properties of the algorithm. For circuits implementing machine learning, algorithmic logic locking has been developed in [20] by utilizing the statistics of the inputs. Besides, obfuscation keys are used in [21] to swap the filters or rows/columns of the filters in convolutional neural networks. Since these techniques depend on the specifics of neural networks, they do not apply to other algorithms.

In this article, for the first time, algorithmic approaches are investigated to obfuscate LDPC decoders, which are self-correcting. LDPC codes are among the most extensively used error-correcting codes in digital communications and storage. They are utilized in most of the controllers for Flash memories and magnetic drives. They can also be found in numerous communication applications, such as 5G/6G wireless communications, Wi-Fi, digital video broadcasting, and Ethernet. LDPC codes can be decoded by different algorithms with tradeoffs on error-correcting performance and complexity. Even for the same decoding algorithm, various architectures and scheduling schemes can be used to achieve different throughput and area complexity [22]. Additionally,
a variety of techniques, such as dynamic message scaling, decoding retry, and postprocessing, can be utilized to handle the error-floor problem of LDPC codes, which is a harmful phenomenon that the error-correcting performance curve flattens as the input error rate decreases [23]. As a result, LDPC decoder architectures optimized for target applications consist of many proprietary designs and the corresponding development is very time consuming. Hence, it is very important to protect the IP of LDPC decoders.

Given the probability information from the communication or storage channel, in general, LDPC decoder iteratively updates probability messages according to the parity check matrix that defines the code. At the end of each iteration, the decoder checks if a codeword is found to decide whether to stop. Even if message bits get flipped, later decoding iterations may not be affected at all.

This article proposes two algorithmic-level obfuscation methods for LDPC decoders. Both of them replace the original stop condition checking part with a key controlled logic-locking block and effectively obfuscate the decoder as follows.

1) The first proposed scheme makes the decoding process run until the last iteration in most cases when a wrong key is used. Accordingly, the decoder throughput is reduced by several times. If the decoder cannot meet the system throughput requirement, then it becomes not usable.

2) The second proposed scheme uses more complicated logic compared to that of the first design to make most of the wrong keys have high corruptibility. As a result, it leads to substantial degradation on not only the throughput but also the error-correcting performance when the key is incorrect.

Additionally, low-overhead modifications on the LDPC decoding algorithm are developed in this article to change the correct decoding stop condition so that the right key can not be guessed. The proposed schemes effectively resist the SAT and AppSAT attacks. Even if an approximate key is returned by the attacks, it makes the decoder have several times lower throughput and become not usable. Our design is also resistant to removal attacks. Despite that the logic-locking block may be identified from the netlist, the attacker is not able to replace it to make the decoder function correct since the right stop condition has been modified and is unknown to the attacker. Take the decoder of a (1270, 635) LDPC code that encodes 635-bit data into 1270-bit codewords as an example, our proposed methods reduce the throughput to less than 1/3 and/or increase the decoder error rate by at least two orders of magnitude at practical channel conditions. The proposed designs only bring 0.15% and 0.55%, respectively, area overheads to the LDPC decoder without any penalty on the achievable clock frequency.

This article is organized as follows. Section II briefly introduces major attacks, existing logic-locking schemes, and LDPC codes. The two proposed algorithmic obfuscation methods for LDPC decoders are detailed in Section III. The security and complexity overhead analyses of the proposed schemes are presented in Section IV.

Discussions and conclusions follow in Sections V and VI, respectively.

II. BACKGROUNDS AND MOTIVATIONS

This section first introduces the attack model, basic knowledge on logic locking, various attacks, and LDPC codes. Then, it is highlighted that existing logic-locking schemes cannot effectively degrade the performance of LDPC decoders even if a wrong key is used.

A. Attack Model

The attack model assumes that the attacker has access to: 1) the netlist of the locked chip. Besides, signal probability skew computation and other analyses can be carried out using the netlist and 2) a functioning chip with the correct key input. However, the attacker does not have perfect knowledge on every detail or the dataflow of the algorithm implemented in the chip. These are the same assumptions made in previous papers [2], [9]–[12], [14].

B. Logic Locking and Attacks

Fig. 1 shows the idea of existing logic-locking schemes. Earlier schemes directly use key inputs to flip signals through AND, OR, and XOR gates [1], [4]–[8]. These designs are subject to the SAT attack [9]. To resist the SAT attack, a carefully designed key-controlled logic-locking block can be inserted as shown in Fig. 1. Its output is XORed with a signal that affects the overall output most. The output of the circuit is corrupted under certain input patterns when a wrong key is used. Only when the right key handed out to the authorized user is applied, the circuit functions correctly.

The SAT attack is a major threat to logic locking. The attacker is assumed to have a functioning chip with the correct key inserted and the netlist of the locked circuit represented by \( Y = f(X, K) \), where \( X, K \), and \( Y \) are the primary input, key input, and primary output vector, respectively. The circuit can be described by a conjunctive normal form (CNF) formula. The SAT attack is an iterative process. In each iteration, it uses the SAT solver to find a DIP, which is an input vector that leads to different outputs under different keys. The DIP is utilized to query the functioning chip to get the corresponding original output. Then, the CNF formula is updated accordingly so that the keys making the circuit output different from the original output are excluded. When no more DIP can be found, the SAT attack stops. At this point, all the wrong keys have been excluded, and the right keys are derived.

The Anti-SAT and SARLock logic-locking schemes in [9] and [10] were proposed to resist the SAT attack. By making
each input pattern exclude unique wrong keys, the number of iterations needed by the SAT attack is exponential to the number of bits in data input. However, this also means that any random key only leads to the wrong output for one single input pattern.

The AppSAT attack [11] is developed based on the SAT attack. In this attack, after every certain number of iterations, random input patterns are utilized to query the functioning chip. The portion of the input patterns generating the wrong output is calculated and the constraints from these queries are also added to the CNF formula each time. If the portion falls below a threshold for a number of rounds, the AppSAT attack terminates and returns a key from the remaining keys as an approximate key. Define the corruptibility of a wrong key as the number of input patterns that make the output different from the original output when the wrong key is applied. The wrong keys with higher corruptibility are more likely to be excluded by the AppSAT attack. If the returned key has very low corruptibility, then it can be used as an approximate key.

In order to increase the corruptibility of wrong keys, key bits directly connected to intermediate signals in the circuit through AND/OR/XOR gates can be utilized in addition to the logic-locking block as shown in Fig. 1 [9]. However, these extra key bits do not increase the number of iterations needed by the SAT attack [9]. Besides, these key bits can be recovered by the AppSAT attack after a small number of iterations [11]. The recent G-Anti-SAT scheme [14] makes the corruptibility of a large portion of the wrong keys tunable without sacrificing the resistance to the SAT attack. As a result, even with a large number of iterations in the AppSAT attack, the probability that a low-corruptibility wrong key is returned is small.

To effectively resist the AppSAT attack, the DTL design [11] increases the corruptibility of all wrong keys at the cost of sacrificed SAT-attack resilience.

Logic-locking schemes can be also applied to lock the finite-state machine (FSM) of a circuit. Examples include HARPOON [24] and the parametric locking in [25]. HARPOON modifies the original FSM to corrupt the primary output of the circuit and it is subject to the SAT attack [27]. The parametric locking inserts dummy states to increase the number of clock cycles spent on the computations. However, the dummy states can be removed by the resynthesis attack [25].

C. LDPC Codes and Decoding Algorithms

LDPC codes are linear block error-correcting codes, which add redundancy to the messages in the encoding process. If the number of errors does not exceed the correction capability of the code, they can be corrected at the receiver using a decoding process. LDPC codes can be specified by the parity check matrix $H$. An $(N, S)$ code encodes $S$-bit messages to $N$-bit codewords, where $S < N$. If $H$ is full rank, its dimension is $(N - S) \times N$. A vector $c = [c_0, c_1, \ldots, c_{N-1}]$ is a codeword iff $cH^T = 0$. Here, the length of the zero vector is $N - S$ bits. A toy example of the parity check matrix is shown in Fig. 2(a).

For real LDPC codes used in practical systems, $N$ is at least several thousands and the parity check matrix $H$ is large and very sparse. The $H$ matrix can be also represented by a Tanner graph as shown in Fig. 2(b). Each row of $H$ is represented by a check node in the Tanner graph and specifies a check equation that needs to be satisfied. Each column of $H$ corresponds to a variable node. A nonzero entry in $H$ represents the connection edge between the corresponding check node and variable node.

Due to the noise in the communication or storage channel, there are errors in the received bits and such error rate is decided by the application. The inputs to the LDPC decoder are the probabilities that each received bit is "1" from the channel information. During the decoding process, probability messages are passed between the connected variable and check nodes and got updated iteratively. At the end of each decoding iteration, hard decisions on whether each received bit should be "1" or "0" are made based on the most updated messages. The decoding stops when the hard-decision vector is a codeword. Otherwise, the decoding process continues until a preset maximum iteration number $I_{\text{max}}$, in which case decoding failure is declared. The error-correcting performance of LDPC decoder improves with $I_{\text{max}}$. However, the additional gain becomes negligible for large $I_{\text{max}}$. On the other hand, using a large $I_{\text{max}}$ increases the worst case decoding latency and reduces the throughput. Hence, $I_{\text{max}}$ is typically set to a moderate number, such as 15, to achieve good error-correcting performance and low latency.

LDPC codes can be decoded by many different decoding algorithms [22]. The most popular one is the Min-sum algorithm [28], since it can well balance the complexity and error-correcting performance. This algorithm is chosen to illustrate our proposed designs and its pseudocodes are listed in Algorithm 1. The input to the decoder is the channel information $\gamma_n$, which is the log-likelihood ratio of the probability that the $n$th input bit is "1" over the probability that it equals "0." The decoder output is the $z$ vector when the decoding stops. In this algorithm, the message from variable node $n$ to check node $m$ is denoted by $u_{m,n}$. The message from check node $m$ to variable node $n$ is $v_{m,n}$. $S_c(n)$ represents the set of check nodes connected to variable node $n$ and $S_v(m)$ denotes the set of variable nodes connected to check node $m$. Take the variable node $n_1$ and check node $m_1$ shown in Fig. 2(b) as examples. $S_c(n_1)$ equals $\{m_1, m_2\}$ and $S_v(m_1)$ is $\{n_1, n_3, n_6\}$.

In the beginning of the Min-sum decoding, the variable-to-check ($v2c$) messages $u_{m,n}$ are initialized and hard decisions $z_n$ are first made according to the channel input $\gamma_n$ in line 2. For example, $u_{m_1,n_1} = u_{m_2,n_1} = \gamma_1$ and $u_{m_2,n_2} = u_{m_3,n_2} = \gamma_2$ for
Algorithm 1 Min-Sum Decoding Algorithm

1: input: $\gamma_n =$ probability that bit $n$ is ‘1’ from channel
2: initialization: $u_{m,n} = \gamma_n; z_n = \text{sign}(\gamma_n)$
3: if $z^H T = 0$
4: return codeword $z$ and stop
5: for $i = 1$ to $I_{\text{max}}$
6: check node processing
7: for each $m$
8: $\min 1_m = \min_{j \in S_n(m)} |u_{m,j}|$
9: $\text{idx}_m = \arg \min_{j \in S_n(m)} |u_{m,j}|$
10: $\min 2_m = \min_{j \in S_n(m), j \neq \text{idx}_m} |u_{m,j}|$
11: $s_m = \prod_{j \in S_n(m)} \text{sign}(u_{m,j})$
12: for each $n \in S_n(m)$
13: $|v_{m,n}| = \left\{ \begin{array}{ll}
\text{amin}_1 & \text{if } n \neq \text{idx}_m \\
\text{amin}_2 & \text{if } n = \text{idx}_m
\end{array} \right.$
14: $\text{sign}(v_{m,n}) = \text{sign}(u_{m,n})$
15: variable node processing
16: for each $n$ and $m$
17: $u_{m,n} = \gamma_n + \sum_{i \in S_n(n), i \neq m} v_{i,n}$
18: a posteriori info. comp. & tentative decision
19: for each $n$
20: $\tilde{\gamma}_n = \gamma_n + \sum_{i \in S_n(n)} v_{i,n}$
21: $z_n = \text{sign}(\tilde{\gamma}_n)$
22: if $z^H T = 0$
23: output codeword $z$ and stop
24: end for
25: output $z$ and declare decoding failure

the toy code shown in Fig. 2. Then, the product of the initial hard-decision vector, $z$, and $H^T$ is calculated. If it is zero, there is no error and $z$ is returned as the codeword. Otherwise, the decoding iteration starts.

Each decoding iteration is divided into three steps: 1) check node processing; 2) variable node processing; and 3) a posteriori information computation. In the processing for check node $m$, the smallest and second smallest magnitudes among all the messages from the connected variable nodes are computed in lines 8–10 of Algorithm 1. They are denoted by $\min 1_m$ and $\min 2_m$, respectively. Besides, $\text{idx}_m$ is the index of the connected variable node whose magnitude is the smallest. Take the $m_1$ node in Fig. 2(b) as an example. It is connected to three variable nodes $n_1$, $n_3$, and $n_6$. Hence, $\min 1_{m_1}$ and $\min 2_{n_1}$ are the smallest and second smallest, respectively, among $|u_{m_1,n_1}|$, $|u_{m_1,n_3}|$, and $|u_{m_1,n_6}|$. Additionally, the product of all the signs of the messages from the variable nodes connected to check node $m$ is computed as $s_m$ in line 11 of Algorithm 1. Then, the check-to-variable (c2v) messages $v_{m,n}$ are computed according to lines 12–14 of Algorithm 1. The magnitude of $v_{m,n}$ equals either $\min 1_m$ or $\min 2_m$ scaled by a factor $\alpha$ depending on whether $n$ equals $\text{idx}_m$. The predetermined scalar $0 < \alpha < 1$ is used to improve the error-correcting performance. In the variable node processing step shown in lines 16 and 17 of Algorithm 1, the updated v2c message is sent to check node $m$ in the next iteration $u_{m,n}$ is calculated as the sum of the channel input for variable node $n$ and the messages from all connected check nodes, except the check node $m$ itself. The a posteriori information

$\tilde{\gamma}_n$ is computed in a similar way as $u_{m,n}$, except that the messages from all connected check nodes are added. Take the variable node $n_3$ in the toy code shown in Fig. 2 as an example. It is connected to two check nodes $m_1$ and $m_4$. Hence, $u_{m_1,n_3} = \gamma_3 + v_{m_1,n_3}$ and $u_{m_4,n_3} = \gamma_3 + v_{m_4,n_3}$. Besides, $\gamma_3 = \gamma_3 + v_{m_1,n_3} + v_{m_4,n_3}$. The hard decision $z$ is made again at the end of each iteration as the signs of $\tilde{\gamma}_n$. If $z^H T = 0$ is satisfied, $z$ is the recovered codeword. The decoding stops and $z$ is sent to the decoder output. Otherwise, the decoding continues to the next iteration. If no codeword is found in $I_{\text{max}}$ iterations, decoding failure is declared.

The frame error rate (FER) and average number of iterations, which decides the throughput, are the two criteria used to measure the performance of the LDPC decoder. If the FER or throughput cannot meet the system requirement, then the LDPC decoder is not usable. Quasicyclic (QC)-LDPC codes [29] are usually used in practical applications because the structure of their $H$ matrices allows efficient parallel processing. For an example (1270, 635) QC-LDPC code whose $H$ matrix consists of $5 \times 10$ shifted identity matrices of dimension $127 \times 127$, simulation results for the FER and average number of decoding iterations are plotted in Fig. 3 for a range of input bit error rates (BERs). In our simulations, binary symmetric channel is assumed and $I_{\text{max}}$ is set to 15 following typical settings. For each input BER, simulation is run until at least ten frame errors have been collected to find the FER. This means, for example, more than $10^7$ decoding samples have been run for BER $= 0.025$.

D. Ineffectiveness of Existing Logic Locking

To find the effects of flipping signals by logic locking on the performance of LDPC decoding, experiments have been carried out in our work to flip one bit in every iteration of the Min-sum algorithm. Since the decoding results are hard decisions of the messages, the sign product $s_m$ and the most significant bit (MSB) of $\min 1_m$ are among the signals that affect the decoding results most. Hence, one of the check nodes is chosen randomly, and its sign product or the MSB
of the min1 value is flipped in every iteration in our simulations. The results are also shown in Fig. 3. It can be observed that even if the sign product or the MSB of min1 of a check node is flipped in every iteration, the resulted differences in the FER and throughput are negligible. The reason is that the LDPC decoder is self-correcting. Even if a c2v message becomes wrong because of the flipping, the other c2v messages sent to the same variable node and the channel information are added up to compute the v2c messages and the a posteriori information as in lines 17 and 20 of Algorithm 1. Only the minimum and second minimum magnitudes of the v2c messages affect later decoding iterations. As a result, the chance that the decoding becomes nonconvergent or needs more iterations is very low. When the output of an existing SAT-attack-resistant logic-locking scheme is used to XOR with sm or MSB of min1 sm, it cannot flip the signal in every LDPC decoding iteration for every input data when a wrong key is used. Hence, the resulted FER and throughput degradation would be even less significant compared to those shown in Fig. 3.

It is also possible to XOR the output of an existing logic-locking block with multiple intermediate signals of the LDPC decoder. When there are too many flipped bits, they cannot be corrected by LDPC decoding. However, in order to resist the SAT attack, each wrong key should only make the logic-locking block output “1” for a very small portion of all possible input patterns. For example, in the Anti-SAT design [9], a wrong key only makes the output “1” for one of the 2n input patterns, where n is the number of data inputs to the logic-locking block and needs to be reasonably large to resist the SAT attack. In this case, even if the output of the LDPC decoder is corrupted by using the wrong key, the degradation on the FER is still negligible. In addition to the key bits used in the Anti-SAT or SARLock blocks, more key bits can be directly connected with intermediate signals by using AND/OR/XOR gates as shown in Fig. 1 in order to increase the corruptibility of the wrong keys. In this case, the FER of the LDPC decoder can be degraded significantly. However, those wrong key bits directly ANDed/ORed/XORed with signals can be derived by the AppSAT attack [11].

The FSM of an LDPC decoder is very simple. It consists of only three states. The decoder starts from the initial state. The second state is for iterative message computation. This state is repeated until the decoder stops and ends at the final state. Due to the simplicity of the FSM, it is very difficult to insert or bypass any states. Hence, existing logic-locking schemes targeting at the FSM, such as HARPOON [24] and parametric locking [25], would not work on LDPC decoders. Besides, they are subject to the SAT or resynthesis attack.

III. SECURE OBFUSCATION SCHEMES FOR LDPC DECODERS

In this section, two logic-locking methods incorporating the properties of the LDPC decoding algorithm are first proposed. By locking the stop condition checking function, which is the same in every LDPC decoding algorithm, our proposed designs can significantly degrade the throughput and/or error-correcting performance when the wrong key is applied. If the decoder cannot achieve the FER or throughput required by the system, it becomes unusable. To obscure the stop condition and effectively resist removal attacks, modifications to the decoding algorithms are also proposed in Section III-C. The overall design flow is shown in Fig. 4. For a given LDPC decoding algorithm, the stop condition checking function is locked, and the correct stop condition and LDPC decoding algorithm is also modified. Then, the Verilog codes of an LDPC decoder need to be changed according to the modification made on algorithmic level. In the end, an LDPC decoder obfuscated by the proposed obfuscation methods is the output.

A. Obfuscated LDPC Decoder With Throughput Degradation at Wrong Keys

The Min-sum decoding algorithm is iterative. Let \( t = zH^T \). The decoding stops when \( t = 0 \) and the most updated \( z \) vector is the correct codeword. If \( t \) does not become zero, the decoding runs until \( l_{\text{max}} \) iterations, in which case decoding failure is declared. In the proposed design, as shown in Fig. 5, the stop condition is controlled by a key vector and it is changed when a wrong key is used. Applying a wrong key leads to one of the two effects: 1) even though the correct codeword is already found and hence the \( z \) vector does not change anymore, the decoding still runs until the last iteration and 2) the decoding process terminates before the correct codeword is found. The first case does not affect the error-correcting performance but reduces the throughput of the decoder. The second case increases the decoding failure rate. Hence, replacing the original stop condition checking function, \( (t = 0) \), by a key controlled stop condition checking can effectively obfuscate LDPC decoders. Next, our first key-controlled stop condition logic-locking scheme is presented.
The original stop condition is $t == 0$. If $t$ has $h$ bits, the original stop condition checking function is

$$f(t) = \overline{t_0} \& \overline{t_1} \& \cdots \& \overline{t_{h-1}}. \quad (1)$$

By adding a constant vector $v$ decided by the designer and slightly modifying the LDPC decoding algorithm as will be detailed in Section III-C of this section, the decoding converges when $t == vH^T$. Our first obfuscation method locks the stop condition checking function by $t == k$. It means that the right key is $vH^T$ and only when the vector $t$ equals the key input, $k$, the LDPC decoding stops. The Boolean expression of our logic-locking function is

$$f_1(t, k) = (t_0 \oplus k_0) \& (t_1 \oplus k_1) \& \cdots \& (t_{h-1} \oplus k_{h-1}).$$

The $K$-map pattern of the $f_1(t, k)$ function is shown in Fig. 6. The black cells in Fig. 6 mean that $f_1(t, k)$ is “1” for the corresponding key and input, in which case the LDPC decoding stops.

When the stop condition checking function is locked by $f_1(t, k)$, using a wrong key changes the stop condition. For a given wrong key, the decoding only stops when the syndrome $t$ equals the wrong key. Hence, most likely, the LDPC decoding will run to the last iteration. However, the original LDPC decoding will not run until the last iteration in most cases at the operating region. As shown for the example code in Fig. 3, even though $I_{\text{max}}$ is set to 15 to achieve good error-correcting capability, the decoding takes on average around five iterations to converge for the practical operating range of FER $< 10^{-5}$. Hence, the throughput of the obfuscated LDPC decoder is significantly decreased when a wrong key is used. On the other hand, if a wrong key is applied, the obfuscated decoder output $z$ is only different from the original decoding result when $t$ accidentally equals the wrong key before the decoding converges. As a result, the FER is almost the same. In the case of obfuscated LDPC decoders, the corruptibility of a wrong key is defined as the number of input patterns leading to the wrong decoder output regardless of the number of decoding iterations. Hence, the wrong keys in our first proposed design all have low corruptibility.

The size of the key input is equal to the number of rows in the $H$ matrix of the LDPC code in the above scheme. For practical LDPC codes, the $H$ matrix has hundreds or even thousands of rows. Using such a long key leads to high logic complexity and requires large memory. To address this issue, a shorter key input can be used to lock some of the bits in $t$.

Assume that the key input is reduced to $h_k < h$ bits. Then, the key-controlled function $f_2(t, k)$ can be modified to

$$f_2(t, k) = (t_0 \oplus k_0) \& \cdots \& (t_{h_k-1} \oplus k_{h_k-1}) \& \hat{t}_0 \& \cdots \& \hat{t}_h \quad (2)$$

where $\hat{t}_i = t_i$ or $\overline{t_i}$ when the corresponding bit in $vH^T$ is “1” or “0,” respectively. The LDPC decoding stops when the first $h_k$ bits of $t$ equal the key input bits and the other bits are the same as those in $vH^T$.

In summary, the first proposed logic-locking scheme for the LDPC decoder can be designed according to the following steps.

1) Select the number of key bits $h_k$ and choose a random secret vector $v$.
2) Design the stop condition checking function as $f_2(t, k)$ according to (2).
3) The correct key $k^*$ is equal to the first $h_k$ bits of $vH^T$. Such a logic-locking block can be inserted in the behavioral description of the LDPC decoder.

All the wrong keys in this obfuscated LDPC decoder have low corruptibility as one. Each of the wrong keys degrades the decoder throughput and has negligible effect on the error-correcting performance in the same way. They are not affected by the key length $h_k$. However, $h_k$ should be large enough so that the right key cannot be easily guessed.

B. Obfuscated LDPC Decoder With Error-Correcting Performance and Throughput Degradation at Wrong Keys

In our first obfuscation method, all wrong keys are of low corruptibility and the resulted error-correcting performance degradation is negligible. In this section, our second design with high-corruptibility wrong keys is proposed. The high-corruptibility wrong keys make the decoder prematurely stop at multiple values of the $t$ vector before the codeword is found. As a result, the error-correcting performance of the obfuscated LDPC decoder is significantly degraded when a high-corruptibility wrong key is used. Besides, similar to the first design, a wrong key leads to substantial reduction on the decoding throughput since the decoding will run until the last iteration in most cases.

The decoder input hard decision is $z = c \oplus e$, where $c$ and $e$ are the codeword and error vector, respectively. For practical channel BERs, the number of errors happened is small. Hence, $t = zH^T = (c \oplus e)H^T = eH^T$ has a limited number of patterns and the patterns are not randomly distributed. Take the (1270, 635) LDPC code as an example. If the BER needs to be lower than $10^{-6}$, then the BER should be less than 0.025. For this code with row weight $d_r = 10$, it can be computed that the probability of each bit of $t$ being “1” is

$$\sum_{i=1, i \text{ is odd}}^{d_r} \binom{d_r}{i} \times 0.05^i \times 0.975^{d_r-i} \approx 0.201.$$"
block. In other words, the mapping should be designed such that \( \Pr[r_i = 1] \approx 0.5 \). Divide the \( r \) vector into groups of \( g \) bits. In our design

\[
r_i = t_{i \times g} \oplus t_{i \times g + 1} \oplus \cdots \oplus t_{i \times g + g - 1}.
\]

Besides, \( g \) is chosen to make \( \Pr[r_i = 1] \approx 0.5 \). Take the (1270, 635) LDPC code in Fig. 3 as an example. When BER=0.025, \( \Pr[r_i = 1] \) can be calculated as \( \sum_{j=1}^{2^{10}} t \) \( 0.201j \times (1 - 0.201)^{(s-r)} \). \( \Pr[r_i = 1] \) is around 0.5 if \( g = 15 \) is used. For a different BER and/or a LDPC code with different row weight, \( g \) can be decided in a similar way. Changing the stop condition to a nonzero vector as will be detailed in the next section does not affect this mapping function or the value of \( g \).

Assume that the \( l_r \) bits of \( r \) are generated from \( t \) through the mapping. If the logic-locking block is to make the decoding stop when the key equals the input as in our first proposed scheme, then its function making use of \( r \) as

\[
f_3(k, r) = (r_0 \oplus k_0) \& \cdots \& (r_{l_r - 1} \oplus k_{l_r - 1}).
\]

Each key makes the decoding stop at one pattern of \( r \). If the number of rows in the parity check matrix of the LDPC code is \( h \), each pattern of \( r \) corresponds to \( 2^{h-l_r} \) patterns of \( t \). Therefore, as shown in the \( K \)-map of the \( f_3 \) function in Fig. 7(a), each wrong key has high corruptibility and makes the decoding stop at \( 2^{h-l_r} \) different patterns of \( t \). The probability that the LDPC decoding process stops in each iteration at such wrong keys is upper bounded by \( 1/2^{l_r} \) and it most likely decreases over the iterations. Since the FERs required for practical applications are low, such as less than \( 10^{-5} \) or \( 10^{-6} \), the wrong keys lead to significant increase in the FERs. Smaller \( l_r \) degrades the FER more. On the other hand, the wrong keys with higher corruptibility are more likely to be excluded within a small number of iterations in the AppSAT attack [11]. A proper value needs to be picked for \( l_r \) to balance the FER degradation and AppSAT attack resistance. Besides, the decoding always runs until the last iteration when \( r \) does not equal the wrong key. Hence, the high-corruptibility wrong keys also reduce the throughput of the LDPC decoder.

If all wrong keys have high corruptibility as shown in Fig. 7(a), the SAT resistance cannot be guaranteed. Wrong keys with corruptibility as one need to be introduced to resist the SAT attack [14]. Each wrong key for function \( f_2 \) in (2) makes the LDPC decoding stop at one pattern of \( t \). Such a function can be utilized to introduce wrong keys of corruptibility one. The logic-locking function of our second obfuscation scheme is

\[
f_4(t, k) = f_3(r, kb) \& (f_2(t, ka) + f_6(r, ka)),
\]

where \( k = [kb][ka] \) and “||” denotes concatenation. Similarly, \( kb \) has \( l_r \) bits. Since the \( l_r \) bits of \( r \) are generated from \( gl_r \) bits of \( t \), the key length of \( ka \) is set to \( gl_r \). \( ka \) can be also made longer at the cost of higher logic complexity and larger memory for storing the key. In (4), \( f_6(r, ka) = r_0 \& k_0 \& \cdots \& k_{l_r - 1} + \cdots + (r_{l_r - 1} \& k_{l_r - 1} \& \cdots \& k_{l_r - 1}) \) is ANDed with \( f_3 \) to make the high-corruptibility wrong keys of \( f_4 \) have the same corruptibility as the wrong keys of the \( f_3 \) function. The \( K \)-map of \( f_4 \) is shown in Fig. 7(b). By ANDing \( f_3(r, kb) \) with \( f_2(t, ka) \), \( f_4 = "1" \) in the cells of the \( K \)-map whose labels satisfy that \( kb = r, ka = [t_0 \cdots t_{l_r - 1}] \), and the other bits of \( t \) equal the corresponding bits of \( vHT \). These cells are the single black cells in the respective columns in Fig. 7(b) and their column labels are the low-corruptibility keys. \( f_3(r, kb) \& f_6(r, ka) \) in (4) makes \( f_4 = "1" \) in the cells whose labels satisfy that \( kb = r, \) \( ka = [t_0 \cdots t_{l_r - 1}] \), and the column labels for these cells are the high-corruptibility keys.

In summary, the second proposed logic-locking scheme for LDPC decoder can be designed according to the following steps.

1) Select the values of \( l_r \) and \( g \); and choose a random secret vector \( v \).
2) Design the stop condition checking function as \( f_4 \) according to (4).
3) Map the first \( g \times l_r \) bits of vector \( vHT \) to an \( l_r \)-bit vector \( r^* \) using a formula similar to that in (3). The correct key is \( k^* = [kb^*[||ka^*]] \), where \( kb^* = r^* \) and \( ka^* \) equals the first \( g \times l_r \) bits of vector \( vHT \).

Using the \( f_4 \) function, the keys are divided into three categories: 1) a single correct key that makes the LDPC decoding stop at \( t := vHT \); 2) the low-corruptibility wrong keys that reduce the throughput but affect the error-correcting performance of the LDPC decoder negligibly; and 3) the high-corruptibility wrong keys that degrade both the error-correcting performance and throughput. The ratio between the high-corruptibility and low-corruptibility wrong keys is affected by \( l_r \). When \( l_r \) is larger, the ratio is larger. However, the high-corruptibility wrong keys have lower corruptibility value and accordingly they result in less significant degradation on the error-correcting performance. Hence, \( l_r \) allows a tradeoff between the corruptibility of the wrong keys and portion of high-corruptibility wrong keys. Nevertheless, even if a low-corruptibility wrong key is used, there is a significant degradation on the throughput and the decoder becomes not usable. The degradation on the decoder throughput is not much dependent on \( l_r \).

C. LDPC Decoding Algorithm With Modified Stop Condition

The main idea of the two proposed obfuscation methods is to lock the stop condition checking function by a key and the correct key equals the syndrome when the decoding converges. The stop condition for the original LDPC decoding is \( t := 0 \). A potential threat is that the zero stop condition can be easily guessed by an attacker who has knowledge about LDPC.
Algorithm 2 Modified Min-Sum Decoding Algorithm

1: input: \( y_n \)
2: initialization: \(|y'_n| = |y_n|; z'_n = \text{sign}(y'_n) = \text{sign}(y_n) \oplus v_n; u'_{m,n} = y'_n\)
3: if \( \mathbf{z}\mathbf{H}^T = \mathbf{p} \)
4: return codeword \( \mathbf{z} = \mathbf{z}' \oplus \mathbf{v} \) and stop
5: for \( k = 1 \) to \( I_{\text{max}} \)
6: check node processing
7: for each \( m \)
8: \( \min V'_m = \min_{j \in S_v(m)} |u'_{m,j}| \)
9: \( \text{idx}_m = \text{argmin}_{j \in S_v(m)} |u'_{m,j}| \)
10: \( \min V'_m = \min_{j \in S_v(m), j \neq \text{idx}_m} |u'_{m,j}| \)
11: \( s' = \prod_{j \in S_v(m)} \text{sign}(u'_{m,j}) \)
12: for each \( n \in S_v(m) \)
13: \( |V'_{m,n}| = \begin{cases} \min V'_m & \text{if } n \neq \text{idx}_m \\ \min V'_m & \text{if } n = \text{idx}_m \end{cases} \)
14: \( \text{sign}(V'_{m,n}) = (-1)^{\text{pm}} s'_m \text{sign}(u'_{m,n}) \)
15: variable node processing
16: for each \( n \) and \( m \)
17: \( u'_{m,n} = y'_n + \sum_{i \in S_v(n), i \neq m} V'_{i,n} \)
18: a posteriori info. comp. & tentative decision
19: for each \( n \)
20: \( y'_n = y'_n + \sum_{i \in S_v(n)} V'_{i,n} \)
21: \( z'_n = \text{sign}(y'_n) \)
22: if \( \mathbf{z}\mathbf{H}^T = \mathbf{p} \)
23: output codeword \( \mathbf{z} = \mathbf{z}' \oplus \mathbf{v} \) and stop
24: end for
25: output \( \mathbf{z} = \mathbf{z}' \oplus \mathbf{v} \) and declare decoding failure

decoders. If the stop condition checking logic-locking block can be identified from the netlist, then it can be eliminated and replaced by a zero detector. Next, low-overhead modifications to the decoding algorithm are proposed to address this issue.

In our design, a constant vector \( \mathbf{v} \) chosen by the designer is added to the input vector \( \mathbf{z} = \mathbf{c} \oplus \mathbf{e} \). Hence, the decoding is carried out on \( \mathbf{z}' = \mathbf{c} \oplus \mathbf{e} \oplus \mathbf{v} \). The decoding algorithm can be modified so that it generates \( \mathbf{c} \oplus \mathbf{v} \) when the error vector \( \mathbf{e} \) is decodable. Then, \( \mathbf{c} \) is recovered by adding \( \mathbf{v} \) back. Such modifications lead to exactly the same decoding results and do not cause any error-correcting performance loss. However, in this case, the correct stop condition is changed to whether \( t \) equals \( \mathbf{p} = \mathbf{v}\mathbf{H}^T \), which is not an all-“0” vector. To incorporate the \( \mathbf{v} \) vector, the Min-sum decoding can be modified as in Algorithm 2. At initialization, \( \mathbf{v}_n \) is added to the sign of \( y_n \) to generate the initial hard-decision vector \( \mathbf{z}' \) and \( |y'_n| = |y_n| \). Accordingly, the initial \( u'_{m,n} \) equals \( y'_n \). In the first iteration, \( \min V'_m, \text{idx}_m, \) and \( \min 2_m \) are computed in the same way and they equal \( \min 1_m, \text{idx}_v, \) and \( \min 2_v \), respectively, in Algorithm 1, since the magnitudes of the channel information are not changed. Also, \((-1)^{\text{pm}} s'_m \) used in line 14 of Algorithm 2 equals \( s_m \) in Algorithm 1. The signs of all the messages added up in the variable node processing and a posteriori information computation in Algorithm 2 are different from those in Algorithm 1 by \( v_n \). As a result, the \( \mathbf{z}' \) vector in Algorithm 2 and the \( \mathbf{z} \) vector in Algorithm 1 is always different by \( \mathbf{v} \) in every iteration. Hence, by adding \( \mathbf{v} \) back after the decoding, the same codeword is recovered.

The vector \( \mathbf{v} \) is secret. However, it does not need to be stored in memory. The additions of \( \mathbf{v} \) to the LDPC decoder input and output and the multiplication of \((-1)^{\text{pm}}\) to the sign can be implemented by adding NOT gates to the inputs and outputs of the corresponding variable node units (VNUs) that compute \( \mathbf{v}\mathbf{c} \) messages and hard decisions using \( \mathbf{c}\mathbf{v} \) messages and channel inputs. The added NOT gates are merged with the other logic gates by the synthesis tool and cannot be told from the netlist. Besides, the VNUs are interconnected with other decoder components through barrel shifters, which route the \( \mathbf{v}\mathbf{c} \) and \( \mathbf{c}\mathbf{v} \) messages according to the nonzero entries of the \( \mathbf{H} \) matrix. Since all the decoder components are also mixed by the synthesis tool, individual VNU cannot be isolated from the netlist. As a result, it is very difficult for the attacker to tell which VNUs have NOT gates added and accordingly recover the \( \mathbf{v} \) vector. Also, adding NOT gates does not necessarily increase the area or critical path since inverting gates, such as NAND and NOR, are smaller and faster than noninverting gates, such as AND and OR [26].

To show that the NOT gates inserted to incorporate the \( \mathbf{v} \) vector addition and \((-1)^{\text{pm}}\) multiplication are merged with the other gates by the synthesis tool, two experiments are carried out on a toy VNU with three input \( \mathbf{c}\mathbf{v} \) messages, whose
sign bits are denoted by \( s_{m_1}, s_{m_2}, \) and \( s_{m_3} \), and one channel information input, denoted by \( \gamma \), using TSMC 65-nm process with 4-ns timing constraint. The synthesis results are translated to logic diagrams and the beginning parts connected to the flipped inputs are shown in Fig. 8. In the first experiment whose result is shown in part Fig. 8(a), \( s_{m_1} \) and \( s_{m_2} \) are flipped due to the multiplication of \((-1)^{p_m}\) in line 14 in Algorithm 2 while \( s_{m_2} \) is not. In the second experiment whose result is illustrated in Fig. 8(b), \( s_{m_1} \) and \( s_{m_2} \) are flipped while \( s_{m_3} \) is not. Besides, the sign bit of \( \gamma \) is flipped due to the addition of the \( \nu \) vector according to line 2 in Algorithm 2. From this figure, the inputs with NOT gates inserted cannot be differentiated from those without inserted NOT gates. Therefore, neither the \( \nu \) or \( p = vH^T \) vector can be derived from the netlist. Considering that the VNU is also mixed with the other computation units in the LDPC decoder by the synthesis tool, it is even harder for the attacker to get \( \nu \) or the correct stop condition.

The area and power consumption of the two modified VNUs shown in Fig. 8 and the VNU without any modification reported by the synthesis tool are listed in Table I. It can be observed that the first and second modified VNUs have 0.38\% and 0.09\%, respectively, area overheads compared to the original VNU. Their power consumption is only 0.16\% and 4.7\% higher compared to that of the original VNU. Considering that an LDPC decoder also has large memory and other computation units, the area and power consumption overheads brought to an LDPC decoder by the NOT gate insertions is even smaller.

QC-LDPC codes [29] are usually used in practical systems since they enable efficient parallel processing. The \( H \) matrix of a QC-LDPC code consists of submatrices, each of which is either a zero or a cyclically shifted identity of dimension \( q \times q \). Many parallel LDPC decoder designs process one submatrix or one block column of submatrices in each clock cycle. In this case, \( \nu \) can be a vector with repeated patterns of length \( q \). Its additions can be also implemented by adding NOT gates.

### IV. Experimental Results

This section analyzes the security, effectiveness, and hardware complexity overheads of the proposed LDPC decoder obfuscation schemes.

#### A. SAT and AppSAT Attack Resistance

The SAT and AppSAT attacks can only be applied to combinational circuits. LDPC decoding algorithms are iterative. Registers are needed to store intermediate results, and they cannot be converted to CNF formulas. In order to apply the SAT/AppSAT attack, copies of the combinational parts of the LDPC decoder can be connected to eliminate the registers as in the unrolling technique [30]. To unroll an LDPC decoder with \( I_{\text{max}} \) decoding iterations for a code whose \( H \) matrix has \( d_c \) “1”s in each row, \( I_{\text{max}} \times d_c \) copies of the combinational units are needed. The decoder for practical LDPC code is already large. Hence, it is infeasible to unroll the decoder for \( I_{\text{max}} \times d_c \) times and carry out the SAT or AppSAT attack experiments for practical LDPC codes. In this section, mathematical analyses are first carried out on the resistance of the proposed designs to the SAT attack. Then, SAT attack experiments are carried out for a toy LDPC decoder. After that, analyses on AppSAT attack resiliency are provided.

The main idea of the SAT attack is to exclude all wrong keys that make the obfuscated circuit output different from the original circuit output. For LDPC decoders, whether an output equals the original output is determined based on the returned vector \( \nu' \) without taking into account the number of decoding iterations. Unlike in the case that the decoder is operating at practical BER range and has a limited number of errors in the input vector, the SAT attack can utilize any input pattern. There are two types of input patterns for the LDPC decoder. The first type is the decodable inputs that make the LDPC decoding process converge at iteration \( I \leq I_{\text{max}} \). The second type is the undecodable inputs that make the LDPC decoding run to the last iteration without convergence. The low-corruptibility wrong keys in both of the proposed obfuscated LDPC decoders make the decoding stop at one specific syndrome. Hence, when a decodable input pattern is selected as a DIP, the low-corruptibility wrong keys making the LDPC decoding process stop before iteration \( I \) will be excluded. Therefore, such a DIP can exclude at most \( I_{\text{max}} \) low-corruptibility wrong keys. When an undecodable input pattern is selected as a DIP, the decoding process will run until the last iteration. In this case, the low-corruptibility wrong keys that make the LDPC decoding process stop before the last iteration will be excluded. In the worst case, the syndrome vector \( \nu \) is different in each decoding iteration. Therefore, at most \( I_{\text{max}} \) low-corruptibility wrong keys will be excluded. As a result, for either case, a DIP can exclude at most \( I_{\text{max}} \) low-corruptibility wrong keys. For the first and second proposed obfuscation designs, the numbers of low-corruptibility wrong keys are \( 2^{h_k} \) and \( 2^{g_{l_k}} \), respectively. Hence, the minimum number of queries needed to precisely recover the functionality in the two proposed obfuscated LDPC decoders are \( 2^{h_k}/(I_{\text{max}}) \) and \( 2^{g_{l_k}}/(I_{\text{max}}) \). Both of them are exponential to the number of key bits, and hence, the SAT attack is effectively resisted.

To further evaluate the SAT-attack resiliency of our proposed designs, the obfuscated LDPC decoders for a (56, 28) toy code is unrolled for one iteration, which is equivalent to setting \( I_{\text{max}} = 1 \). The open-source SAT attack tool [31] is applied on these toy decoders using an Intel Core i7 with 4-GB RAM platform and the CPU time is limited to 10 h. Table II shows the results. For the first obfuscation scheme, the SAT attack can be finished within 10 h when its key length \( h_k \) is 7 or 14. For both of these key lengths, the number of iterations needed by the SAT attack is \( 2^{h_k} \), which matches our analyses for the case of \( I_{\text{max}} = 1 \). For the second obfuscation design, the SAT attack cannot be finished within 10 h when \( g_{l_k} \) is 14 or larger. This design leads to longer SAT attack
All the wrong keys for the first proposed obfuscated decoder have low corruptibility. When the $H$ matrix of the LDPC code is $(N - S) \times N$, the vector $t$ has $N - S$ bits. If the AppSAT attack is applied, any returned low-corruptibility wrong key would allow the attacker to recover the approximate functionality with $\epsilon = 1/(2^{N-S})$ [3], which means that one out of the $2^{N-S}$ input patterns leads to different outputs. However, a low-corruptibility key most likely makes the decoder run until the last iteration and leads to significant decrease in the throughput. The ratio between the high-corruptibility and low-corruptibility wrong keys in the second proposed design is around $2^{lr}$. Although high-corruptibility wrong keys are more likely to be excluded by the AppSAT attack, some high-corruptibility wrong keys are left in the pool. If a high-corruptibility wrong key is returned by the AppSAT attack and is used for the decoder, it will lead to degradation on not only the throughput but also the FER of the decoder. If a low-corruptibility wrong key is returned, even though it can help to recover the approximate functionality of LDPC decoder, the throughput is degraded. For either case, the returned key is not usable.

### B. Effectiveness of the Proposed Obfuscation Schemes

To show the performance degradation that can be brought by the proposed obfuscation schemes to the LDPC decoder when low and high-corruptibility wrong keys are used, simulations are carried out using C++ for the example $(1270, 635)$ QC-LDPC code, whose $H$ matrix consists of $5 \times 10$ submatrices of dimension $127 \times 127$. $I_{\text{max}}$ is set to 15 in our simulations.

Simulation results for the first obfuscated LDPC decoder whose wrong keys are all low-corruptibility are shown in Fig. 9. In our simulations, the key length $h_k$ is set to 127. A 127-bit random vector that is not equal to the first 127 bits of $vH^T$ is used as the low-corruptibility wrong key. As illustrated in part Fig. 9(b), in the original LDPC decoder, the average number of decoding iterations is much smaller than $I_{\text{max}}$. However, if a wrong key is used, the decoder most likely runs until the last iteration and the average number of iterations becomes almost $I_{\text{max}}$. For the practical operating range of BER < 0.03, this translates to more than three times reduction on the throughput. On the other hand, each wrong key makes the decoder stop at one pattern of $t$, and the chance that the decoding stops prematurely at a wrong vector is small. As a result, as shown in Fig. 9(a), the first proposed obfuscation method only leads to negligible difference in the FER.

In the second proposed design, if a low-corruptibility wrong key is used, the decoder will have significant degradation on the throughput but negligible difference in the FER similar to those in Fig. 9. The simulation results when high-corruptibility wrong keys are used are shown in Fig. 10. In these simulations, two high-corruptibility wrong keys with $lr = 10$ and $g = 15$ are used. The $lr$-bit $kb$ parts of the two keys are random vectors with HD equal to 3 and 9 compared to $r^4$. The $lr \times g = 150$-bit $ka$ part is randomly generated. The corruptibilities of these two wrong keys are both $2^{h_{\text{lr}}-lr} = 2625$. The one with smaller HD causes more degradation on the FER as shown in Fig. 10(a). The reason is that the number of errors decreases and the HD between $t$ and $vH^T$ becomes lower over the LDPC decoding iterations. Hence, when a wrong key with smaller HD is used, the chance that it equals the $r$ vector and makes the decoding stop prematurely is higher compared to the case that a key with higher HD is utilized. Nevertheless, even for the almost largest possible HD = 9 that can be used when $l_r = 10$, the wrong key leads to more than two orders of magnitude degradation on the FER at practical operating range of BER < 0.03.

| TABLE II |
|---|
| SAT ATTACK EXPERIMENTAL RESULTS ON (56, 28) LDPC DECODERS |
| The first obfuscated decoder | # of iterations | $h_k = 7$ | $I_{\text{max}} = 14$ | $h_k = 21$ |
| | time (second) | | | |
| The second obfuscated decoder | # of iterations | $g_k = 7$ | $g_k = 14$ | $g_k = 21$ |
| | time (second) | | | |

![Fig. 9. Min-sum decoding results for (1270, 635) QC-LDPC code with $I_{\text{max}} = 15$ using the first proposed obfuscation scheme that only has low-corruptibility wrong keys. (a) FER. (b) Average number of iterations.](image-url)

![Fig. 10. Min-sum decoding results for (1270, 635) QC-LDPC code with $I_{\text{max}} = 15$ using the second proposed obfuscation scheme that has both high and low-corruptibility wrong keys. (a) FER. (b) Average number of iterations.](image-url)
The probability that a high-corruptibility wrong key makes the decoding stop prematurely is also relatively small and hence the decoding also runs until the last iteration in most cases. Therefore, as shown in Fig. 10(b), the average number of iterations is also around $I_{\text{max}}$ when high-corruptibility wrong keys are used. The average iteration number for the HD = 3 wrong key is slightly smaller compared to that of the case with HD = 9, although the difference is not visible from the figure.

### C. Removal Attack Resistance

Both of the proposed schemes obfuscate LDPC decoders utilizing algorithmic properties instead of just adding a logic-locking block to the circuit. It is possible that the block or part of the block implementing the function $f_2$ or $f_4$ can be identified, for example, by sorting the probability skew values of the signals [12], since it involves large AND trees. However, these functions check the stop condition and they are integral parts of the decoder. If they are removed, the LDPC decoder will run until the last iteration and the throughput is substantially reduced. Additionally, by modifying the decoding algorithm with negligible complexity overhead, the stop condition is changed from an all-“0” vector to a random-like vector. This makes it impossible to replace the proposed logic-locking block by the correct function even if the attacker knows that a normal LDPC decoder stops at all-“0” syndrome vector. Besides, the NOT gates inserted for XORing the $v$ vector for the algorithmic modifications are combined with the other logic gates by the synthesis tool. Hence, the $v$ vector and accordingly, the modified stop condition cannot be recovered from the netlist either as analyzed in Section III-C.

### D. Hardware Overhead Analyses

This section analyzes the complexity overheads of the proposed obfuscation schemes brought to LDPC decoders by using the $(1270, 635)$ code as an example. The decoder with the proposed stop condition checking function for logic locking is described using Verilog codes in register transfer level. All of the synthesis results are provided using the Cadence Genus synthesis solution with TSMC 65-nm process under 4-nm timing constraint.

The hardware implementation architectures of LDPC decoders depend on not only the decoding algorithm but also the computation scheduling scheme. Sliced message passing is a popular scheduling scheme due to its high throughput and low memory requirement [22]. In such a decoder, one block column of the $H$ matrix is processed in each clock cycle. Hence, $5 \times 127 = 635$ CNU’s are used to compute the $\text{min}_1$, $\text{min}_2$, etc., and then derive the $2v$ messages for each row of the $H$ matrix in parallel. Also, 127 VNU’s are used to compute the $v_2$ messages and the $a \text{ posteriori}$ information. Besides, $2 \times 5 127$-input Barrel shifter’s are needed to route the messages between the CNU’s and VNU’s according to the nonzero entries of the shifted-identity submatrices in $H$. Details about the CNU and VNU can be found in [22].

The first obfuscation scheme uses the $f_2(t, k)$ function in (2) to implement the stop condition checking. Compared to the original stop condition checking function $f(t)$ in (1), the overheads include $h_k \text{ XOR}$ gates, where $h_k$ is the number of key bits. Even if $h_k$ is set to 127 to achieve high security level, the proposed obfuscation scheme only brings 0.15% overhead to the area. Besides the computation units listed in Table III, large memories are needed to store the channel input of the decoder and the hard-decision vector. Hence, the overhead brought by the proposed scheme to the overall decoder area is even smaller.

The $f_2(t, k)$ function has one more gate in the data path compared to $f(t)$. However, the VNU’s have several multibit adders and two sign-magnitude to 2’s complement converters in the data path. It is much longer than the data path of the stop condition checking and decides the critical path of the LDPC decoder. Therefore, the proposed scheme does not cause any degradation on the achievable clock frequency of the decoder.

The second obfuscation scheme utilizes the $f_4(t, k)$ function in (3) for stop condition checking. When the values of $g$ and $l_r$ are set to 15 and 10, respectively, the sizes of $k_a$ and $k_b$ are 10 and 150 bits, respectively. This design leads to 0.55% area overhead compared to the original decoder. Although this overhead is larger than that of the first obfuscation design, it is still very small.

For comparison, the Anti-SAT block is also synthesized and the results are included in Table III. In order to achieve a similar number of iterations needed by the SAT attack as the first proposed obfuscation scheme with $h_k = 127$, the key length of the Anti-SAT design is set to 254-bit. In this case, the area overhead brought by the Anti-SAT design is 0.36%, which is larger than that of the first obfuscation scheme but smaller than that of the second one. However, the Anti-SAT design is only to flip signals in conventional designs of LDPC decoders without the proposed stop condition checking function modification. Even if a wrong key is used, it would not lead to any noticeable performance loss as analyzed in Section II-D.

### V. Discussion

This article takes the Min-sum decoding algorithm as an example to illustrate the proposed logic-locking schemes, since this algorithm is used in many applications. There are other
LDPC decoding algorithms. They are different from the Min-sum algorithm in the way that the magnitudes of the messages are computed in the check and variable node processing. However, they all have the same stop condition and sign computation as the Min-sum algorithm. The proposed obfuscation schemes modify the stop condition and sign computation. Hence, they can be applied in the same way to other LDPC decoders implementing different decoding algorithms.

Using an existing logic-locking scheme, such as the Anti-SAT, G-Anti-SAT, DTL, or SFLL design, to lock one bit of $t$ does not effectively corrupt the LDPC decoder output. Flipping one bit of $t$ makes the LDPC decoding stop at a wrong pattern of $t$. However, the chance that $t$ equals a pattern that has a single bit different from $vH^T$ is very low. Hence, such logic-locking method does not lead to any noticeable increase in the FER. Besides, the outputs of existing lock-locking blocks are not always “1.” Even if a scheme with relatively high corruptibility, such as the DTL design [11], is used, the selected bit of $t$ will not be flipped with high probability. Hence, even if the decoder stops at a later iteration, only one or two more iterations are carried out instead of until the last iteration. Accordingly, existing logic-locking schemes do not cause significant degradation on throughput or FER as the proposed designs.

Another possible method to obfuscate the LDPC decoder is to XOR the output of an existing logic-locking block directly with one bit in the decoder output vector. However, by comparing the output of the locked decoder with that of a functioning decoder, the location of the flipped bit can be easily identified and the logic-locking block is subject to removal attacks. The SFLL-FLEX scheme [16] has not been broken by any removal attacks. Nevertheless, there is a tradeoff between the degradation it can cause on the LDPC decoder FER and the resistance to the SAT attack. For the SFLL-FLEX block that achieves high resistance to the SAT attack, XORing its output with LDPC decoder output will only lead to negligible FER degradation when a wrong key is used. Besides, XORing the output of any logic-locking block with the LDPC decoder output does not change the number of decoding iterations and hence does not bring any degradation to the throughput.

VI. CONCLUSION

In this article, two obfuscation schemes for LDPC decoders have been proposed by locking the stop condition checking function and modifying the decoding algorithm. Both designs have low-corruptibility wrong keys that make the SAT attack complexity exponential. Also, they cannot be all excluded by the AppSAT attacks. These wrong keys lead to significant degradation on the decoder throughput. In addition to the low-corruptibility wrong keys, there are a large portion of high-corruptibility wrong keys in the second proposed obfuscation method. They cause significant degradations on not only the throughput but also the error-correcting performance. Besides, the proposed modifications on the decoding algorithm make the correct decoding stop condition a secret and thwart possible attacks. Future work will study algorithmic obfuscations on other fault-tolerating or self-correcting functions.

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Jingbo Zhou (Graduate Student Member, IEEE) received the B.S. degree in telecommunication engineering from Beijing University of Post and Telecommunication, Beijing, China, in 2018. He is currently pursuing the Ph.D. degree with the Electrical and Computer Engineering Department, The Ohio State University, Columbus, OH, USA. His current research interests are hardware security and cryptography.

Xinniao Zhang (Senior Member, IEEE) received her Ph.D. degree in Electrical Engineering from the University of Minnesota. She joined The Ohio State University as an Associate Professor in 2017. Prior to that, she was a Timothy E. and Allison L. Schroeder Assistant Professor 2005–2010 and Associate Professor 2010–2013 at Case Western Reserve University. Between her academic positions, she was a Senior Technologist at Western Digital/SanDisk Corporation. Dr. Zhang’s research spans the areas of VLSI architecture design, digital storage and communications, security, and signal processing.

Dr. Zhang received an NSF CAREER Award in January 2009. She is also the recipient of the Best Paper Award at 2004 ACM Great Lakes Symposium on VLSI and 2016 International SanDisk Technology Conference. She authored the book “VLSI Architectures for Modern Error-Correcting Codes” (CRC Press, 2015), and co-edited “Wireless Security and Cryptography: Specifications and Implementations” (CRC Press, 2007). She also published more than 100 papers. She was elected to serve on the Board of Governors of the IEEE Circuits and Systems Society for the 2019–2021 term and is a member of the CASCOM and VSA technical committees. She was also a Co-Chair of the Data Storage Technical Committee (2017–2020). She served on the technical program and organization committees of many conferences, including ISCAS, SiPS, ICC, GLOBECOM, GlobalSIP, and GLSVLSI. She has been an associate editor for the IEEE Transactions on Circuits and Systems-I 2010–2019 and IEEE Open Journal of Circuits and Systems since 2019.