Design of DAC for Fluxgate Based on PWM Rectifier

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Abstract. High temperature fluxgate sensor is one of the main sensors in rotary steering logging, which can obtain bit dip information by measuring geomagnetic direction. The use of Digital Analog Converter (DAC) to achieve a closed loop of the fluxgate can effectively improve the measurement accuracy, but the existing DAC chip cannot work in a high temperature environment underground. In order to solve this problem, a design scheme of PWM DAC is proposed. According to the performance index of DAC and the requirements of fluxgate application scenarios, the design points of PWM DAC are discussed, and the circuit implementation scheme is given. Second, based on the scheme, a 10 bit PWM DAC with 1 ms adjustment time and 0.5 LSB maximum output ripple is designed, which has passed the simulation and physical verification.

1. Introduction
Fluxgate is a kind of magnetic measurement sensor, which has the characteristics of high resolution, wide measurement range and high reliability. It is widely used in the fields of Geomagnetism and aeromagnetic survey. High temperature fluxgate sensor, as an important part of geometric oriented high temperature and high pressure sensor, can obtain the azimuth angle of bit by measuring the direction of bit cutter axis relative to magnetic north, which is one of the main sensors of rotary steering logging.

The DAC chip is a high temperature fluxgate core device, and the existing chip can not work well under 220 degree temperature. In this paper, an active low-pass filter is designed and built by using the high-temperature operational amplifier chip to meet the downhole temperature. The PWM signal with adjustable duty cycle generated by the main control unit is low-pass filtered, and the DC voltage signal whose amplitude is linearly controlled by the duty cycle is obtained to realize the high-temperature DAC function. Simulation and experimental results show that the DAC has 10 bit resolution, 0.5 LSB maximum output error and 0.2 ms setup time, which meets the performance requirements of closed-loop fluxgate.

2. Design of PWM DAC
Pulse width modulation (PWM) technology can accurately control the square wave duty cycle through a high-precision counter. PWM module is mainly composed of counter and comparator, as shown in Fig. 1
The counter is accumulated under the trigger of CPU clock $f_{clk}$, and is cleared when the count value reaches $2^n - 1$. The change frequency is called $f_{mod}$, and the reciprocal of modulation frequency is called $T_{mod}$. The count value is sent to the comparator to compare with the preset threshold $K$. When the count value is less than $K$, the comparator outputs high level; when the count value is greater than $K$, the comparator outputs low level.

By adjusting the duty cycle of PWM signal by changing $K$ and filtering the PWM signal through low-pass, the DC voltage signal with precise amplitude control can be obtained and the DAC function can be realized. Obviously, the bit number of DAC is $n$, and when the number of bits becomes larger, the $f_{mod}$ of the PWM becomes lower.

Due to the weak driving ability of the main control system, considering the high requirements of the fluxgate circuit for signal processing and the active filter is not affected by the changes of system and load impedance, we use active filter to realize PWM waveform filtering. For the L-order low-pass filter, the attenuation rate of the amplitude frequency response in the stopband is $-20L$ dB / dec, the amplitude frequency response of the 1 ~ 4 order low-pass filter is shown in Fig. 2.

The attenuation coefficient of the filter at $f_{mod}$ is called $A_f$, and $f_{c1}$ ~ $f_{c4}$ are the cut-off frequencies of the filter respectively.

When the order is fixed, increasing the DAC bit $n$ will reduce the modulation frequency $f_{mod}$, resulting in the decrease of attenuation coefficient $A_f$ and cut-off frequency $f_c$, and then increase the output ripple and build-up time of the filter, and reduce the accuracy and response speed of the filter. In addition, increasing the attenuation coefficient $A_f$ can reduce the ripple, but at the same time it will reduce the cut-off frequency $f_c$, resulting in the increase of the setup time and the decrease of the response speed of the filter. Therefore, the number of digit, ripple and establishment time restricts each other.
3. Ti-Tina simulation

According to the requirements of fluxgate closed-loop, a 10 bit PWM DAC is designed. The output ripple of the filter is less than 0.5 LSB and the setup time is less than 1 ms. TMS320F28335 is used as the main controller. The system clock frequency $f_{clk}$ is 60 MHz, so $T_{mod} = 17067$ ns, and the modulation frequency $f_{mod} = 58.6$ kHz. After calculation, the fundamental frequency attenuation $A_f$ is less than -62.3dB. In order to reduce the adjustment time, a third-order low-pass filter is built by using dual operational amplifiers. According to figure 2, the cut-off frequency should be set at 5364 Hz, and the circuit is shown in Figure 3.

We use TINA-TI to simulate and set the supply voltage to 3.3V. Figure 4 shows the frequency domain response of the circuit. It can be seen that the attenuation at 58.6 kHz is -60 dB, meeting the design requirements.

Observe the output curve when the duty cycle of input PWM waveform jumps from 10% to 90%, as shown in Figure 5. The establishment time is 0.54 ms, which meets the design index of less than 1 ms.
4. Circuit verification
The DAC module is designed to verify the simulation results, as shown in the figure below.

![DAC Circuit](image)

Figure 6. DAC circuit

The amplitude of PWM waveform is 3.3V, which makes the duty cycle of PWM waveform jump from 10% to 90%. The output waveform is shown in Figure 7.

![Output waveform](image)

Figure 7. Output waveform

The setup time of DAC output stabilization in the figure is 0.336 ms, which meets the design target of 1 ms. As shown in Figure 8, the noise suppression of DAC is 64.4 dB, which is better than the design index.
5. Conclusion

Aiming at the problem of limited selection of high temperature fluxgate DAC, a design scheme of PWM type DAC is proposed. According to the DAC performance index and application scenario requirements, the design points of PWM DAC are discussed, and the circuit implementation scheme is given. Based on this scheme, a 10 bit PWM DAC with adjustment time of 0.336 ms and maximum output error of 0.5 LSB is designed, which has passed the simulation and physical verification. The calibration results show that the DAC meets the design target and proves the feasibility of the scheme.

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