A non-isolated single-input dual-output boost DC–DC converter

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Abstract
A new non-isolated single-input dual-output boost DC–DC converter is introduced in this paper. The motivation of the work is that in various applications such as some multilevel converters, it is required to provide multiple dc sources that are not required to be isolated. In the proposed structure, the output ports of the converter can provide different values of power and still balance the output voltage. Even, if required, the output voltages can be set to different values. From practical point of view, the proposed topology uses minimum number of power-electronic switches (two switches for two outputs) which have common ground making their drive circuit simple and easy to implement. The state-space modelling of the proposed converter is presented, then, the model is used to design the passive elements. Moreover, the proposed converter is compared with the relevant converters. In order to verify the performance of the proposed DC–DC converter, a prototype of the converter has been implemented and the results are presented.

1 | INTRODUCTION

Generally speaking, the DC–DC converters have many applications in industry and renewable power generation systems such as photovoltaics. A wide variety of topologies exists for DC–DC converters in both isolated and non-isolated types with different functionalities. From the viewpoint of output-to-input voltage ratio, they can be classified as buck (step-down), boost (step-up), or buck-boost structures. Also, from the viewpoint of the number of input and output ports, they are categorized as single-input single-output, single-input multi-output, multi-input single-output, or multi-input multi-output. Each of these categories have their own applications and specifications.

The proposed converter in this paper, is a non-isolated single-input multi-output boost DC–DC converter. One possible application of such a converter is to provide multiple DC voltage sources needed in e.g. multilevel converters. Some of the relevant topologies are reviewed as follows.

A multi-output DC–DC converter for multilevel converter application has been presented in [1–3]. The converter provides multiple non-isolated dc outputs for multilevel converters such as neutral-point-clamped converter which needs multiple non-isolated DC sources in its dc side.

A single-input dual-output (SIDO) DC–DC converter has been presented in [4]. The structure uses only one power electronic switch and therefore the output voltages cannot be controlled independently. The studied SIDO converter in [5] operates in buck mode and the outputs have common ground. In [6] another SIDO converter is introduced. One output is controlled by the first stage which is a buck converter and the other output is controlled by the second stage which is a boost converter. In [7], a multi-input multi-output (MIMO) DC–DC converter is suggested which can also operate as a single-input multi-output (SIMO) DC–DC converter. In fact, it contains a buck converter in the input stage, a boost converter in the middle, and again a buck converter in the output stage which all share a single inductor. The structure will therefore use three power electronic switches for a SIDO converter.

Also, a SIDO converter is suggested in [8–10] in which the outputs have common ground. For applications where the series connection of the outputs is required, this converter cannot be used. The SIMO converter presented in [11] has buck operation. In this converter, the outputs have common ground. The work has been extended for MIMO case in [12]. In [13] a SIMO buck converter has been presented. The converter provides float outputs which cannot be connected to each other. The transformer-isolated version of the previous structure has been presented in [14]. A step-down SIDO converter has been introduced in [15]. This topology employs three switches and its input current is discontinuous. Derivation of different SIDO topologies has been discussed in [16].
The proposed SIDO converter in [17] employs four switches and its outputs cannot be connected together. A SIMO DC–DC converter has been presented in [18]. For a SIDO case, five power electronic switches are utilized making the circuit configuration and control of the converter complicated. A MIMO DC–DC converter based on the switched-capacitor multilevel topology has been proposed in [19]. Although the topology provides multiple output ports, the independent voltage control of the output ports is not possible. Another MIMO DC–DC converter has been studied in [20]. The structure is based on diode-switched-capacitors and is suitable for multi-input operation rather than single-input operation. A single-input dual-output converter is investigated in [21]. The mathematical modelling and control of the converter has been elaborated. However, the structure of the converter imposes limitations on its operation. The converter uses only one power electronic switch for two outputs; therefore, the outputs cannot be controlled independently.

In [22] a MIMO converter has been presented. The converter uses buck converters at input stage and current-source mode buck cells at the output stage. For a SIDO case, the converter uses three power electronic switches. In this structure, the outputs cannot be connected to each other if necessary. A MIMO DC–DC converter has been analyzed in [23]. The converter has been designed for two input and two output ports which uses five power electronic switches and high number of passive elements. Also, the output ports cannot be connected together. A coupled-inductor based SIDO converter is investigated in [24]. The converter is composed of two boost converters feeding two outputs with a common ground. Another SIDO converter topology has been presented in [25]. The topology uses three switches to control two output voltages with a common ground.

In this paper, a new circuit topology is presented for a SIMO boost DC–DC converter. This topology is derived from the conventional boost converter. The detailed derivation and also mathematical modeling of the converter is presented throughout the paper. Derivation of the proposed topology is explained in Section 2. The state-space modeling of the proposed converter is presented in Section 3. The design considerations are given in Section 4 and the comparison of the proposed converter with other relevant converters is presented in Section 5. The experimental verification of the proposed topology is presented in Section 6.

2 THE PROPOSED SIDO BOOST DC–DC CONVERTER

In order to deduce the proposed DC–DC converter, let us consider that there is need for two boosted dc voltages where one dc voltage source is available and there is no need for isolation of the two output voltages. The simplest approach may be as shown in Figure 1(a). In the figure, two boost DC–DC converter are employed to provide two output dc voltages using a single input dc voltage source. However, if one point of the outputs is in-common (Figure 1(b)), the input dc voltage source will be short-circuited through the inductor $L_2$ and the diode $D_2$. Therefore, the two independent boost converters (supplied from a single dc source) cannot be used if there is an electric connection between the outputs. In order to solve this problem, a modification is done and the obtained converter is shown in Figure 1(c). As shown in the figure, the proposed SIDO boost DC–DC converter generates two output dc voltages using a single input dc voltage source. This can be used wherever multiple non-isolated dc voltages are required (such as some multilevel converters).

It is important to note that the topology could be extended to higher number of output ports, however, the double output case will be studied hereinafter. One clear advantage of the proposed SIDO converter is that it does not need for coupled inductors or transformers. The coupled inductors and transformers need demanding design since they are prone to saturation and extra power losses.

There are two switches in the proposed converter as a result of which there will be four operation modes. It should be noted that the inductors currents are assumed to be continuous. In other words, the converter is supposed to operate in continuous conduction mode (CCM). The possible operation modes of the proposed converter are shown in Figure 2. Although there are four possible modes of operation, in order to operate in CCM, the duty cycle of the switch $S_1$ ($d_1$) must be higher than that of the switch $S_2$ ($d_2$). This will be elaborated in the next section. Different switching sequences can be adopted in the proposed converter. One of them is turning the switches ON simultaneously. This switching method is practically simple and easy to implement. The other possibility is the interleaved switching in which the switches are switched in a semi-complimentary manner. However, their conduction period may have some overlap. Although the latter switching method will result in lower input current ripple, the rest of the paper is based on turning the switches ON simultaneously. Generating the switching signals and also the key waveforms of operation of the proposed converter are shown in Figure 3. In order to draw the waveforms, the assumption $d_1 > d_2$ is made.
In this section, the state space modelling of the proposed SIDO boost DC–DC converter is presented. The inductors currents and the capacitors voltages are considered as the state variables, \( \dot{X} = AX + BU \) where \( A \) is the state matrix, \( B \) is the input matrix, and \( U \) is the input vector. As there are different modes of operation, the average state-space model can be written as follows:

\[
\dot{X} = \bar{A}X + \bar{B}V_{in} \tag{1}
\]

Where, \( \bar{A} \) is the average state matrix and \( \bar{B} \) is the average input matrix.

Considering that the switches are turned ON simultaneously, two different combinations of operation modes are possible. In the first combination, it is supposed that the duty cycle of the switch \( S_1 \) is higher than that of the switch \( S_2 \). In this case, the three possible operation modes will be those shown in Figure 2(a,b,d). Considering that the duty cycle of the switch \( S_1 \) and \( S_2 \) is defined as \( d_1 \) and \( d_2 \), respectively, the average state matrix can be achieved as follows:

\[
\bar{A} = d_2A_4 + (d_1 - d_2)A_2 + (1 - (d_1 + d_2))A_4 \tag{2}
\]

where, \( A_1, A_2, A_4 \) are the state matrix of mode 1, 2, and 4, respectively, which are not mentioned to keep conciseness.

Given the analysis above, the detailed average state-space model is obtained as follows:

\[
\frac{d}{dt} \begin{bmatrix}
   d_1 \\
   d_2 \\
   \frac{di_1}{dt} \\
   \frac{di_2}{dt}
\end{bmatrix} = \begin{bmatrix}
   0 & 0 & -1 & -1 \\
   0 & 0 & 0 & -1 \\
   \frac{1}{L_1} & 0 & 0 & 0 \\
   \frac{1}{C_1} & \frac{1}{L_2} & 0 & 0 \\
\end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix}
   0 \\
   0 \\
   \frac{1}{L_1} \\
   \frac{1}{L_2}
\end{bmatrix} V_{in} \tag{3}
\]

The average value of the state variables in steady-state can be obtained by setting \( \dot{X} = 0 \) in Equation (3). Therefore, the following equation is achieved:

\[
\begin{bmatrix}
   0 \\
   0 \\
   \frac{1}{L_1} \\
   \frac{1}{L_2}
\end{bmatrix} = \begin{bmatrix}
   0 & 0 & -1 & -1 \\
   0 & 0 & 0 & -1 \\
   \frac{1}{L_1} & 0 & 0 & 0 \\
   \frac{1}{C_1} & \frac{1}{L_2} & 0 & 0 \\
\end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix}
   0 \\
   0 \\
   \frac{1}{L_1} \\
   \frac{1}{L_2}
\end{bmatrix} V_{in} \tag{4}
\]

Solving Equation (4), the steady-state average values of the state variables are obtained as follows:

\[
\begin{bmatrix}
   d_1 - d_2 \\
   (1 - d_1)^2 (1 - d_2) R_1 \\
   (1 - d_1) R_1 + R_2 (d_2 - d_1) \\
   (1 - d_1) (1 - d_2) R_1 R_2 \\
\end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix}
   \frac{1}{1 - d_2}
\end{bmatrix} V_{in} \tag{5}
\]
Based on Equation (5), the gains of $V_1$ and $V_2$ can be written as follows.

$$M_{V_1} = \frac{V_1}{V_{in}} = \frac{d_1 - d_2}{(1 - d_1)(1 - d_2)}$$

$$M_{V_2} = \frac{V_2}{V_{in}} = \frac{1}{1 - d_2} \quad (6)$$

The voltage gains $M_{V_1}$ and $M_{V_2}$ are illustrated in Figures 4 and 5, respectively. As Figure 4 indicates, the voltage gain $M_{V_1}$ has a direct relation with $d_1$ but inverse relation with $d_2$. In other words, $M_{V_1}$ increases as $d_1$ increases and $d_2$ decreases. Moreover, $M_{V_1}$ can take values less than 1 implying that this port of the converter is both buck and boost.

Although the above-mentioned results are based on the assumption that the duty cycle of the switch $S_1$ ($d_1$) is higher than that of the switch $S_2$ ($d_2$), interestingly the same results are also obtained for the case that $d_2$ is assumed to be higher than $d_1$. However, according to Equation (5), in order to keep the average currents of inductors positive, $d_1$ must be higher than $d_2$.

Generally, the value of the output voltages could be different. Assuming $V_2 = \alpha V_1$, the following equation can be achieved from Equation (5).

$$d_1 = \frac{1 + \alpha d_2}{1 + \alpha} \quad (7)$$

Considering the fact that $d_2 \geq 0$ and using Equation (7), the following inequality is achieved:

$$d_1 \geq \frac{1}{1 + \alpha} \quad (8)$$

If the aim is to provide the equal output voltages ($V_1 = V_2$), the following relations are obtained considering Equations (7) and (8).

$$d_1 = \frac{1 + d_2}{2} \quad (9)$$

$$d_1 \geq \frac{1}{2} \quad (10)$$

Moreover, the inductors currents have a positive average value, $I_1 > 0, I_2 > 0$. Therefore, using Equation (5), the following relations can be obtained:

$$\frac{d_1 - d_2}{(1 - d_1)(1 - d_2)R_1} > 0 \Rightarrow d_1 > d_2$$

$$\frac{(1 - d_1)R_1 + R_2(d_2 - d_1)}{(1 - d_1)(1 - d_2)^2R_1R_2} > 0 \Rightarrow (1 - d_1)R_1 > (d_1 - d_2)R_2$$

(11)

If the condition $V_2 = \alpha V_1$ is considered, then using Equations (7) and (13), the following relation is derived:

$$(1 - d_1)R_1 > (d_1 - d_2)R_2 \Rightarrow \frac{d_1}{1 + \alpha} R_1 > R_2$$

(12)

If the power consumed by $R_1$ and $R_2$ is considered to be $P_1$ and $P_2$, respectively, the following relation among the power of the output ports can be written:

$$P_2 > \alpha P_1 \quad (13)$$

For the specific condition where $V_1 = V_2$, the relation $R_1 > R_2$ can be achieved using Equation (12). It could be concluded that for $V_1 = V_2$, $R_1$ should be greater than $R_2$, otherwise, the assumption made for obtaining the above equations (i.e. CCM of both inductors) is not satisfied.

4  |  DESIGN CONSIDERATIONS

The design considerations include the sizing of the inductors and capacitors used in the proposed DC–DC converter. For the sizing of the inductors, it is assumed that the capacitors are large enough so that the output voltages ($V_1, V_2$) could be considered constant. Considering the operation modes and extracting and manipulating the inductors current equations, the ripples on
the inductor currents \( \Delta i_1, \Delta i_2 \) can be achieved as follows:

\[
\Delta i_1 = i_{1,\text{max}} - i_{1,\text{min}} = \frac{V_{\text{in}}}{L_1} d_1 T
\]

\[
\Delta i_2 = i_{2,\text{max}} - i_{2,\text{min}} = \frac{V_{\text{in}}}{L_2} d_2 T
\]

In Equations (14) and (15), \( T \) is the switching period which corresponds to the switching frequency, \( f_s = 1/T \).

On the other hand, the average value of the inductor currents, \( \bar{i}_{1,\text{avg}} \) and \( \bar{i}_{2,\text{avg}} \), can be written as follows using Equation (5):

\[
\bar{i}_{1,\text{avg}} = I_1 = \frac{i_{1,\text{min}} + i_{1,\text{max}}}{2} = \frac{(d_1 - d_2) V_{\text{in}}}{(1 - d_1)^2 (1 - d_2) R_1}
\]

\[
\bar{i}_{2,\text{avg}} = I_2 = \frac{i_{2,\text{min}} + i_{2,\text{max}}}{2} = \frac{[1 - (d_1) R_1 + R_2 (d_2 - d_1) V_{\text{in}}}{(1 - d_1) (1 - d_2)^2 R_1 R_2}
\]

Using Equations (22) and (23), the following relations are obtained for the inductances:

\[
L_1 > \frac{d_1}{2} \left[ (1 - d_1)^2 (1 - d_2) R_1 \right] \left( \frac{\Delta i_1}{\bar{i}_{1,\text{avg}}} \right) f_s
\]

\[
L_2 > \frac{d_2}{2} \left[ (1 - d_1) (1 - d_2)^2 R_1 R_2 \right] \left( \frac{\Delta i_2}{\bar{i}_{2,\text{avg}}} \right) f_s
\]

If the output voltages are equal, the following relations can be obtained using Equations (9), (26), and (27):

\[
L_1 = \frac{2d_1 (1 - d_1)^2 R_1}{(R_1 - R_2) \left( \frac{\Delta i_1}{\bar{i}_{1,\text{avg}}} \right) f_s}
\]

\[
L_2 = \frac{d_2 (1 - d_1) (1 - d_2)^2 R_1 R_2}{(R_1 - R_2) \left( \frac{\Delta i_2}{\bar{i}_{2,\text{avg}}} \right) f_s}
\]

The variation of \( L_1 \) versus \( R_1 \) and \( d_1 \) for four different values of the inductor relative current ripple, \( \Delta i_1/\bar{i}_{1,\text{avg}} \) (0.1, 0.2, 0.3, 0.4), is plotted in Figure 6. It is important to notice that the figure is plotted for the specific condition of \( V_1 = V_2 \). Also, it should be noted that \( d_2 \) is dependent on \( d_1 \) according to Equation (9). As the figure indicates, the largest value of \( L_1 \) (worst case from design point of view) is obtained for the highest \( R_1 \), the lowest \( d_1 \) and the lowest relative current ripple. Its value is independent of \( R_2 \).

Figure 7 shows the variation of \( L_2 \) versus \( R_2 \) and \( d_2 \) for different values of \( R_1 \) and relative current ripple of 0.4. As the figure suggests, the maximum value of \( L_2 \) is obtained for \( d_2 = 1/3 \) and maximum \( R_1 \) and \( R_2 \). It should be noted that according to Equation (29), the value of \( L_2 \) is inversely proportional to \( (R_1 - R_2) \). If the value \( (R_1 - R_2) \) of decreases, the value of \( L_2 \) increases dramatically. This suggests that in order to keep CCM, there should be a difference between \( R_1 \) and \( R_2 \) in the equal
output voltage condition. This fact was analysed in the previous section.

During ON period of the switch, the capacitors are discharged and during the rest of the switching period, the capacitors are charged. Therefore, using basic circuit concepts and calculations, the capacitance of $C_1$ and $C_2$ could be achieved as follows:

$$C_1 = \frac{d_1}{R_1 f_s \frac{\Delta i_1}{V_1}}$$

$$C_2 = \frac{d_2}{R_2 f_s \frac{\Delta i_2}{V_2}}$$  \hspace{1cm} (30)$$

From design point of view, the maximum capacitor value can be achieved as follows using Equation (30):

$$C_{1,\text{max}} = \frac{d_{1,\text{max}}}{R_{1,\text{min}} f_s \left( \frac{\Delta i_1}{V_1} \right)_{\text{min}}}$$

$$C_{2,\text{max}} = \frac{d_{2,\text{max}}}{R_{2,\text{min}} f_s \left( \frac{\Delta i_2}{V_2} \right)_{\text{min}}}$$  \hspace{1cm} (31)$$

In practice, to select the switches and diodes, their maximum off-state voltage and on-state current should be calculated. Taking Figure 1(c) into account, the off-state voltage of the switches $S_1$ and $S_2$ ($V_{S1}$ and $V_{S2}$) and those of the diodes $D_1$ and $D_2$ ($V_{D1}$ and $V_{D2}$) can be written as follows:

$$V_{S1} = V_{D1} = V_1 + V_2$$

$$V_{S2} = V_{D2} = V_2$$  \hspace{1cm} (32)$$

Also, the maximum current of the switches and diodes is equal to maximum current of the corresponding inductor:

$$I_{S1,\text{max}} = I_{D1,\text{max}} = i_{1,\text{max}}$$

$$I_{S2,\text{max}} = I_{D2,\text{max}} = i_{2,\text{max}}$$  \hspace{1cm} (33)$$

In order to better understand the maximum current of the semiconductor devices, they are obtained as a function of input and output parameters. Using Equations (14)–(17) and (33), the following equations are derived:

$$I_{S1,\text{max}} = I_{D1,\text{max}} = I_1 + \frac{\Delta i_1}{2}$$

$$I_{S2,\text{max}} = I_{D2,\text{max}} = I_2 + \frac{\Delta i_2}{2}$$  \hspace{1cm} (34)$$

Using Equation (6), the duty cycles of the switches can be calculated as follows:

$$d_1 = 1 - \frac{V_{in}}{V_1 + V_2}$$

$$d_2 = 1 - \frac{V_{in}}{V_2}$$  \hspace{1cm} (35)$$

Based on Equations (19), (21), (28), (29), and (35), the following equation can be obtained:

$$I_{S1,\text{max}} = I_{D1,\text{max}} = I_1 \left( 1 + \frac{\Delta i_{1,\text{pu}}}{2} \right)$$

$$I_{S2,\text{max}} = I_{D2,\text{max}} = I_2 \left( 1 + \frac{\Delta i_{2,\text{pu}}}{2} \right)$$  \hspace{1cm} (36)$$

5 | COMPARISON OF THE PROPOSED CONVERTER WITH THE RELEVANT STRUCTURES

The comparison of the proposed converter with the existing SIDO converters in the literature is presented in Table 1. It should be noted that most of the SIDO converters does not provide the series connection possibility as in the proposed converter. Also, in some of the topologies one port operates in buck mode and the other operates in boost mode [16]. In some others, output voltage of one port is a portion of the other
| Table 1 | Comparison of the proposed SIDO converter with the relevant converters |
|---------|------------------------------------------------------------------------|
| **Topology** | [3] | [2] | [10] | [26] | [18] | [25] | **Proposed** |
| Ns      | 2   | 3   | 3   | 2   | 5   | 3   | 2   |
| Nd      | 2   | 3   | -   | 2   | -   | 3   | 2   |
| Nc      | 2   | 2   | 2   | 2   | 2   | 3   | 2   |
| Nl      | 1   | 1   | 1   | 1   | 2   | 2   | 2   |
| TSVmax [V] | 300 | 300 | 300 | 200 | 500 | 233 | 300 |
| TSCmax [A] | 29.1 | 43.65 | 42.52 | 28.6 | 39 | 26.4 | 14.75 |
| TDVmax [V] | 200 | 250 | -   | 200 | -   | 133 | 300 |
| TDCmax [A] | 28.8 | 28.8 | -   | 28.6 | -   | 38.6 | 14.75 |
| TSVA [kVA] | 8.73 | 13.09 | 12.75 | 5.72 | 19.5 | 6.15 | 4.42 |
| L [mH]@max current [A] | 2 mH@14.55A | 2 mH@14.55A | 2 mH@14.26A | 2 mH@10.3A | 2 mH@14.3A | 2 mH@6A | 2 mH@2A |
| TIEmax [mJ] | 211.7 | 211.7 | 203.34 | 204.49 | 142 | 208.5 | 111.52 |
| C [µF] | 2x47 | 2x47 | 2x47 | 2x47 | 3x47 | 2x47 |
| Current ripple [A] | 0.75 | 0.75 | 0.6 | 0.62 | ΔI1 = 0.61 | ΔI1 = 0.6 | ΔI1 = 0.95 |
| Voltage ripple [V] | ΔV1 = 1.8 | ΔV1 = 1.8 | ΔV1 = 1.8 | ΔV1 = 1.4 | ΔV1 = 0.3 | ΔI2 = 0.9 | ΔI2 = 0.6 |
| Common-emitter switches | No | No | No | No | No | No | Yes |
| Input current | Continuous | Continuous | Continuous | Continuous | Continuous | Continuous | Continuous |
| Operation mode | Boost | Buck-boost | Boost | Boost/buck-boost | Boost/buck-boost | Boost | Boost |
| Output configuration | Series | Series | Common ground | Common ground | Independent | Common ground | Series |
| Restrictions | Voltage gains depend on the loads | Voltage gains depend on the loads | Voltage gains depend on the loads | ΔV2 depends on V1 | - | V2 ≥ V1 | For V2 = V1, R2 < R1 |
TABLE 2  Experimental setup parameters

| Type       | Value                        |
|------------|------------------------------|
| $L_1$      | Toroid with ferrite core     | 1.6 mH@20 A               |
| $L_2$      | Toroid with ferrite core     | 3.8 mH@15 A               |
| $C_1$      | Electrolytic                 | 47 µF@160 V               |
| $C_2$      | Electrolytic                 | 68 µF@160 V               |
| S1 and S2  | MOSFET IRFP360, 400 V, 23 A  | MUR2540, 400 V, 15 A      |
| D1 and D2  | Ultra-fast diode             |                           |
| Switching frequency | -                             | 20 kHz                    |
| $R_1$      | Constant                     | 50 Ω                      |
| $R_2$      | Variable                     | 40 Ω, 20 Ω                |

Therefore, the comparison only considers the topologies that provide two independent boost outputs. In order to make the comparison results more sensible, a numerical example is considered for comparison. The input voltage of the sample case is considered to be 50 V, the maximum value of each of the two output voltages is 100 V. The loads are considered as $R_1 = 50$ Ω and $R_2 = 20$ Ω. In Table 1, $N_S$, $N_D$, $N_C$, and $N_L$ denote the number of switches, diodes, capacitors, and inductors, respectively. As the table indicates, the proposed topology has minimum number of switches. Also, its maximum total switch current ($TSC_{max}$) and maximum total switch volt-ampere ($TSVA_{max}$) is the lowest among the topologies which implies that the cost and losses of the switches in the proposed topology is lower than the existing alternatives. Although the proposed converter uses two inductors, the maximum total inductor energy ($TIE_{max}$) stored in the inductors is the lowest which indicates that the cost and volume of the inductors is lower compared to the other topologies. Also, using the same inductors and capacitors, the voltage and current ripples of all of the converters are close to each other. One of the advantages of the proposed converter is that the switches have common-emitter structure and also their emitter is connected to the source ground. Therefore, their driver circuit is simpler and easy to implement and they do not require isolated supplies for the driver circuits.

6 1 EXPERIMENTAL STUDIES

The experimental study of the proposed converter is presented in this section. For the sake of conciseness, the simulation results are not included. The input voltage is considered to be 50 V and the output voltage varies depending on the operating condition. The switching frequency is considered to be 20 kHz and maximum acceptable current ripple is assumed to be 0.4. Moreover, the maximum output voltage ripple is considered as 5%. $R_1$ is considered to be variable between 20 Ω to 50 Ω and $R_2$ varies between 10 to 40 Ω taking into account that $R_1$ is always higher than $R_2$ by at least 10 Ω. The minimum and maximum value of $V_1$ and $V_2$ is 50 and 100 V, respectively ($d_{1,\text{min}} = 0.5, d_{1,\text{max}} = 0.75, d_{2,\text{min}} = 0.2, d_{2,\text{max}} = 0.5$). It is important to note that the output voltages ($V_1$ and $V_2$) are supposed to be equal. Based on the mentioned data and Equations (28)–(31), the value of the inductances $L_1$ and $L_2$ are obtained as 1.57 and 3.7 mH, respectively. Also, the capacitors $C_1$ and $C_2$ are obtained as 37.5 and 50 µF, respectively. However, their values are selected to be higher in the setup because of inevitable tolerances in practice. The experimental setup specifications are summarized in Table 2. In order to realize the load variation, a resistance is switched in parallel with $R_2$ to decrease its value from 40 to 20 Ω. According to Equation (32), the voltage ratings of the switches and diodes are different. In a real application, switches with different voltage ratings should be used to achieve higher efficiency and lower losses. However, as a prototype, the same switches and diodes are used in this paper for experimental studies.

The experimental results in the case of abrupt variation in the load resistance are shown in Figure 8 where $R_1$ is...
Figure 8(a) shows the output voltages (CH1: \( V_1 + V_2 \), CH2: \( V_2 \)). As expected, the output voltages are both equal to 100 V. Figure 8(b) shows the inductors currents (\( i_1 \) and \( i_2 \)). As the figure indicates, the currents of inductors are both continuous before and after the load change. Regarding Figure 8, as the load changes dramatically, the output voltages experience a transient variation, however, the average value of the output voltages does not change. This verifies that the voltage gains in the proposed converter are independent of the load value. Also, it is clear that the average value of the inductors current varies as the load changes. Moreover, the voltage and current ripples varies as the load changes. It is worth noting that there are two types of ripples on the voltage and current waveforms. One type of ripples is the high-frequency ripples caused by the switching action and their frequency is equal to the switching frequency. The other type is lower-frequency ripples that are generated as a result of the controller action and variations in the control signals around their steady-state values. The value of these ripples is mainly based on the control parameters. This issue has been studied in [27].

In order to further analyse the results, the magnified view of the experimental results after the load change is shown in Figure 9. In Figure 9(a), the voltages (\( V_1 + V_2 \)) and \( V_2 \) are shown. As the figure indicates, the voltage waveforms contain high-frequency ripples while maintaining the intended average values. The magnified view of the currents, \( i_1 \) and \( i_2 \), is shown in Figure 9(b). As the figure indicates, the currents also contain ripples which are less than the designed thresholds. The current through the switches (\( i_{sw1}, i_{sw2} \)), the voltage across the switches (\( V_{sw1}, V_{sw2} \)) and the current through the diodes (\( i_{D1}, i_{D2} \)) are exhibited in Figure 9(c,d,e), respectively. It can be seen that the current of each switch is complementary with that of the corresponding diode.

### 7 Conclusion

In this paper, a new single-input dual-output boost DC–DC converter has been proposed and analysed. The proposed structure uses only two power electronic switches to control two output voltages. The switches in the proposed converter have lower voltage and current ratings compared with the other converters. As the switches have common emitter structure, their drive circuit requires only one DC supply. The proposed converter has been modelled and designed in details. As the experimental results indicated, the proposed converter provides controlled output voltages despite load change. The converter provides continuous input current which is advantageous for most DC supplies. It is important to remember that the series connection of the output ports (as in the proposed converter) is not possible in most of the existing dual-output converters.

### Data Availability Statement

The data that support the findings of this study are available from the corresponding author, upon reasonable request.
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