Asynchronous progress design for a MPI-based PGAS one-sided communication system

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Abstract—Remote-memory-access models, also known as one-sided communication models, are becoming an interesting alternative to traditional two-sided communication models in the field of High Performance Computing. In this paper we extend previous work on an MPI-based, locality-aware remote-memory-access model with an asynchronous progress-engine for non-blocking communication operations. Most previous related work suggests to drive progression on communication through an additional thread within the application process. In contrast, our scheme uses an arbitrary number of dedicated processes to drive asynchronous progression. Further, we describe a prototypical library implementation of our concepts, namely DART, which is used to quantitatively evaluate our design against a MPI-3 baseline reference. The evaluation consists of micro-benchmark to measure overlap of communication and computation and a scientific application kernel to assess total performance impact on realistic use-cases. Our benchmarks show, that our asynchronous progression scheme can overlap computation and communication efficiently and lead to substantially shorter communication cost in real applications.

Index Terms—DART; MPI; one-sided; asynchronous progress; data-locality; overlap

I. INTRODUCTION

Towards asynchronous communication operations, MPI standard [1] defines an imprecise progress rule for implementors [2]. However, different interpretations (strict or weak) of progress rule could lead to differing progress patterns of the non-blocking communication operations (include RMA communication routines).

Figure 1(a) take MPI_Put for example, describes the view of how MPI RMA communication operations implement according to the strict and weak interpretation, respectively. As Fig. 1(a) shows, once the non-blocking put operation has been posted on the origin process (P0), the data transfer can be enabled independent of the further MPI synchronization calls (e.g., flushes) at the P0 side. This pattern supports the truly asynchronous completion of communications (i.e., asynchronous progression) by offering the overlap of communication and computation. On contrary, in Fig. 1(b) the put communication is delayed until the ensuring flush call happens at the origin. This interpretation depends on MPI synchronization call from P0 to make explicit progress. MPI_Get and the request-based RMA (MPI_Rput/Rget) operations exhibit the similar behavior difference as MPI_Put does under the above two interpretations. The MPI programmers should be aware that MPI RMA communications do not overlap with computation with certainty in all MPI implementations. Clearly, allowing overlap of communication and computation in parallel applications, especially for long messages, is beneficial. This helps to reduce host processor overhead by making the host processor less involved in the transmission or reception of data and to hide latency by letting CPU contribute to the computation in the interim. Therefore, an implementation adheres to the strict interpretation has performance advantage potential over one that supports the weak interpretation for the applications with some degree of overlap potential [3].

Traditionally, two methods – multi-threading-based (refer to MPICH, MVAPICH and Intel MPI) and kernel thread-based (refer to Cray MPI [4]) – are well-studied by scientists to support for communication/computation overlap to minimize the host overhead [5]. However, the disadvantages inherent in them gradually become impediment to scalable application performance. Additionally, an innovative approach – process-based [5], [6] is devised to designate arbitrary number of cores per node to be the processes handling the communication progression. It has been proved to be an efficient alternative method supporting asynchronous communications for current multi-/many-core architecture, compared with the conventional methods.

DART [7], [8] – as an MPI3-based PGAS runtime system – is designed to provide one-sided communication operations (including blocking and nonblocking) with data locality-awareness in mind. It can directly be adopted by users or easily forms the basis for the runtime time system of certain PGAS project. In addition, compared to MPI codes, DART codes are more concise and easier-to-read due to that DART internally hides the MPI complexities from users [9]. Given the performance properties, PGAS languages require of the non-blocking RMA interfaces to hide network latencies by overlapping communication and computation. Therefore, supporting the asynchronous progression in DART RMA is inevitable.

In section II we illustrate the design method of DART asynchronous progression engine with the process-based approach and then theoretically analyze the efficiency and suitability of applying the DART non-blocking RMA communication operations on parallel applications. In section III we evaluate...
the performance of DART non-blocking RMA communication operations with micro-benchmarks and 3D heat conduction application as a representation for a load of numerical simulation schemes. We compare the DART RMA and the native MPI RMA in all experiments.

II. DESIGNING THE DART PROGRESS ENGINE

In this section, we outline the design details which address the process-based implementation issues regarding the asynchronous progression engine in DART. Foremost, we partition cores on a node between progress processes and user application processes. Next, we introduce the way of setting up global memory (similar to MPI window) across the partitioned cores. We then internally launch the asynchronous progression engine by intercepting and overriding the DART RMA functions. Finally, the suitability of the appliance of DART non-blocking RMA communication operations on parallel applications is discussed.

A. Core partitioning

On the premise that the DART global memory architecture is applied [10], processes within the same shared memory domain are possible to communicate via direct load/store accesses. Detaiely, the user memory regions are directly mapped into the on-node progress processes’ memory address spaces. This property of DART system positively affects the appliance of the process-based approach in a way of reducing the time complexity. Consequently, with the mapped memory address, RMA operations can be redirected and handled by the progress processes without the verbose message transfers between the application (user) processes and the progress processes within the same shared-memory domain.

At DART initialization time (i.e., in \texttt{dart\_init}), one launches applications with a number of processes. Several processes within each node are then designated to be the progress processes for the other processes located in the same node. Figure 2 shows a specific instance where we use two progress processes within each node and each of them is pinned to a core. Additionally, the progress processes are designated to on-node application processes at DART initialization time as evenly as possible. Actually this asynchronous progression engine allows one to generate arbitrary number of progress processes internally on-demand. Importantly, after excluding the progress processes, the remaining processes comprise the \texttt{DART\_TEAM\_ALL} that are only visible to the user applications. Apparently, the progress processes are only visible to the DART system instead of the users. Consequently, the progress processes are prohibited to be explicitly involved in all DART interfaces except the \texttt{dart\_init} or \texttt{dart\_exit} (DART termination routine). Specifically, inside the \texttt{dart\_exit}, the progress processes are busy waiting for the commands delivered by other on-node user processes in an \texttt{MPI\_Iprobe} loop. The asynchronous progression engine ensures that the progress processes react properly according to the command characteristics, which will be discussed in the subsections below.
B. Global memory setup

The progress processes are natively designed to be invisible to the target applications. However, we here let progress processes being aware of any global memory allocation since the progress processes, after all, would be a proxy for the application processes to asynchronously perform the RMAs to the target global memory segments.

The memory region reserved for non-collective global memory allocation is statically built up at DART initialization time. Meantime, the progress processes are intuitively involved in the collective window creation operation. On the other hand, we allocate the collective global memory region dynamically by collectively invoking dart_team_memalloc_aligned on certain team (similar to MPI communicator). This interface is originally visible to application processes instead of progress processes. Therefore, one of the participated application processes internally notifies all on-node progress processes. After consuming the intra-node notifications, the progress processes are involved in the collective global memory allocation with the received parameter (i.e., index, see Table I). In this case, a notifying operation is equivalent to a small intra-node message transferring. It is simply performed by using pair-wise MPI_Send and MPI_Recv, which will not cost a lot. Clearly, the progress processes are internally involved in all global memory allocations (window creation) within DART system. To minimize the space complexity, I allocate memory of 0 byte in the progress processes’ memory space as a result of memory mapping. This is feasible since the progress processes’ memory space would never be accessed by users. Therefore, there is no extra memory allocation wasting from the application point of view. Importantly, the target global memory segment should be accessible to the progress processes after the window (global memory segment) is generated. Therefore, the progress processes must immediately start a global lock epoch to all processes related to this window and end it when the window is destroyed.

C. Asynchronous non-blocking RMA communication operations

DART non-blocking RMA operations can be activated successfully as the processes are granted access to the window within the above global lock epoch. Figure 3 gives insights into the asynchronous progression design of the DART non-blocking RMA communication operations. In detail, first of all, the origin chooses an on-node progress process. Instead of actually performing the RMA operations, it sends the RMA (i.e., put or get) requests to its current progress process. This progress process then takes over the actual message transfers meant for the given destination Px on MPI shared-memory window sharedmem-win or DMA window (i.e., MPI-created window win for non-collective global memory and MPI dynamically-created window d-win for collective global memory) according to whether the target process is an on-node application process or not. In this sense, the origin can do its own computation tasks independently from the initiated RMA communications. It is clearly observed that the asynchronous progression engine keeps the data locality in mind in order to achieve high performance. The origin sends a ‘wait’ request to its progress process when invoking dart_wait or dart_waitall and then busy-waits for the finished notification from its progress process.

Figure 4 shows two common scenarios where the RMA requests are consumed by progress process brokenly (shown in left) and consecutively (shown in right), respectively. The progress process would like to flush the target immediately if it finds no RMA request followed closely. Otherwise, if the RMA requests are consecutively sent to the progress process, ideally the progress process will build a backlog of RMA requests. They are processed in batch by progress process when it receives a ‘wait’ request or becomes idle (i.e., probe nothing). In this case, the data transfers fail to start as soon as the RMA calls occur. However, the progression in the accumulative RMA communications can be activated automatically when the progress process probes no message, which provides overlap of communication and computation to some extent. Furthermore, this behavior can somehow bring performance improvement through amortizing a flush synchronization call with multiple RMA operations.

The application processes, rather than the progress processes, are originally aware of the raw information on the DART RMA communications. Therefore, an application process should encapsulate the raw information first and then sends it as a packet to its corresponding progress process. Essentially, the packet is determined in a way of abstracting the input data provided by DART RMA operations. The input data basically consists of three attributes, that is, global pointer, message size, and origin address, where the global pointer addresses the remote data item and thus exposes the target unit/process ID, segid (see Table I), target address offset and index. The message size (data_size), segid and index should be straightforwardly included into the packet. Besides, the progress process should perform RMA communications with locality-awareness in mind. Therefore, a signal value (is_shmem) indicating that data transfer occurs within node or across nodes is entailed in the packet. After obtaining a local base pointer the raw origin address can be deduced by the progress process with the aid of origin address offset (ori-

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TABLE I  PACKET STRUCTURE.

| Field     | Value                                                                 |
|-----------|----------------------------------------------------------------------|
| dest      | The target process ID                                                |
| index     | Denote the involved team                                             |
| origin_offset | The offset relative to the beginning of origin memory segment     |
| target_offset | The displacement relative to the beginning of target memory segment |
| data_size | The transferred data size                                            |
| segid     | 0: Indicate the non-collective global memory                         |
|           | ≥ 1: Indicate the specific collective global memory                   |
| is_shmem  | 0: Origin and target are in different nodes                          |
|           | 1: Origin and target are in the same node                            |
gin_offset). Besides, the relative displacement (target_offset) that is passed to the RMA operation should be included in the packet for locating the target data. Accordingly, the packet is represented as the data structure shown in Table I. It is identified as a derived datatype through a call to MPI_Type_create_struct [11].

Figures 3 and 4 demonstrate the interactive activities between application processes and the corresponding progress processes. Fig. 3 describes the algorithm for each of the DART get, wait and waitall primitives straightforwardly. Obviously, the progress process procedure shown in Fig. 5 is invoked as necessary to make progress on outstanding RMA communications. In this instance, get communication is implemented by calling MPI_Get and flush routine. The MPI_Rget, coupled with MPI_Wait can actually be an efficient alternative. For brevity we leave out the procedures handling the collective memory allocation/deallocation, team creation/destroy operations, put operation (handled similar as get operation) and termination routine (i.e., dart_exit).

The eager protocol for small message transfers in MPI potentially involves overlap of computation and communication (i.e., through buffering). However, the rendezvous protocol for long message transfers does not allow overlap between computation and communication [11]. To minimize the progression implementation overhead, especially for small messages, we only enable asynchronous progress for DART non-blocking RMA communications when the message sizes across the threshold value, which is determined in this paper in terms of the data results below (refer to Sect. III-A).

D. Suitability analysis

It is significant to present the suitability of this DART asynchronous progression approach for the real-world applications. DART RMA communications are implemented based on the MPI passive-target RMA. However, MPI implementations do not guarantee truly passive RMA operations. This means that the target can be involved in an RMA operation only by explicitly making MPI calls (any MPI call) to ensure communication progression on its side. Actually, the study [3] mentioned before adopted the process-based approach to realize the truly passive RMA. Besides, another study [12] tries to implement the truly passive RMA by using InfiniBand Atomics. Achieving truly passive RMA operations is critical for the irregular parallel algorithms.

Revising the Fig. 1(b), we can observe that the RMA communications are essentially initiated by letting the origin explicitly issue the synchronization calls even when the target process is ready. In this case, the actual data transfer will be deferred and fails to overlap with the following computation after employing the above two studies for truly passive RMA. Detailely, the performance of applications including the traditional regular parallel algorithms (e.g., stencil computation [13], FFT [14] and so on) may benefit from this DART asynchronous progression approach rather than the above two studies. In addition, the regular parallel algorithms feature balanced communication patterns and still play an active role in the engineering and scientific communities.

III. PERFORMANCE EVALUATION

In this section, we present a comprehensive experimental evaluation and analysis of the asynchronous progress feature discussed in the preceding sections. The experimental environment was the Cray XC40 system at HLRS. It is equipped with 7,712 compute nodes made up of dual twelvecore Intel Haswell E5-2680v3 processor (one processor per socket), which has exclusive 256 KB L2 unified cache for each core. Therefore, each compute node has 24 cores running at 2.5GHZ. The different compute nodes are interconnected via a Cray Aries network using Dragonfly topology.

The first step in identifying the performance of DART progress engine is to evaluate the ability to improve the application performance through overlapping with computation for the non-blocking RMA communication operations. We should add that, the asynchronous progression feature is disabled in Cray MPI by default and thus should be turn on explicitly by setting environment variables at compiler time. (Surprisingly, after setting environment variables as needed, it seems that the MPI asynchronous progression does work for the MPI
non-blocking point-to-point communications rather than RMA communications.) For a more comparative study, a 3D heat conduction application benchmark is then run and analyzed on DART and Cray MPI implementations to investigate the synthetic impact of progression on the overlap of computation and communication.

In all experiments below we try to show the preliminary advantages of DART non-blocking RMA operations in terms of hiding communication latencies with only two progress processes per node. Furthermore, multiple trails with increasing number of progress processes per node could be carried out to explore an optimal application performance. Note that, the number of dedicated progress processes for computation-intensive applications should be cautiously determined in order to guarantee that there are a good number of computing processes (application processes) to share the required workload.

A. Host processor overhead and application availability

In this section, we examine the overlap degree of communication and computation when using DART non-blocking RMA operations with asynchronous progression enabled, based on the measurements modified from Sandia MPI Micro-Benchmark Suite (SMB) [15]. Meantime, we check the potential of DART non-blocking RMA communication operations to improve the application performance through overlapping with computation, compared with the Cray-MPI RMA (without asynchronous progression).

Specifically, we use a test component which is contained in the SMB. In this component, two basic metrics – the host processor overhead and application availability [16] are measured for non-blocking MPI send and receive operations. To target the non-blocking RMA operations, we adjust this measurement by replacing the send or receive routines with the non-blocking RMA routines. The overhead is defined as the amount of time that a process is engaged in the transfer of each message. On the other hand, application availability is defined to be the fraction of total transfer time that the application is free to perform non-MPI related work [15]. The test measures the time to a loop where each iteration performs a non-blocking RMA operation of a given size, defined workload and then waits for the message transfer to complete. DETAILEDLY, MPI_Get and MPI_Win_flush are used in MPI version while dart_get (the progress process performs MPI_Get inside) and dart_wait are invoked in DART version. The total amount of time (iter_t), the work time (work_t) and message transfer time (base_t) are assessed averagely in the test. The test is repeated for increasing number of work loop iterations and stops when iter_t hits more than 1.5 times base_t. Note that, the overhead and application availability are calculated at the stop point with the method of overhead = iter_t − work_t and availability = 1 − overhead/base_t.

Taking message size of 64 KB and get operation for example, Figure 6 illustrates the overhead and application availability when using MPI get communication operations during one trial, in intra-node and inter-node case. The overhead and application availability implied in these figures are baseline...
Fig. 6. The overhead and application availability achieved with MPI intra-node and inter-node get operations for 64 KB message sizes. The measured overhead is significant and the application availability is \( \sim 25.9\% \) for intra-node get and \( \sim 11.9\% \) for inter-node get. Without asynchronous progression.

Fig. 7. The overhead and application availability achieved with DART non-blocking intra-node and inter-node get operations for 64 KB message sizes. The measured overhead is low and the application availability is \( \sim 72.8\% \) for intra-node get and \( \sim 74.2\% \) for inter-node get. With asynchronous progression.

Fig. 8. A comparison of application availability between DART non-blocking and MPI RMA operations. "M" denotes MPI and "D" denotes DART. "P" denotes Put operation and "G" denotes Get operation.
values without featuring the asynchronous progression. Likewise, the overhead and application availability achieved with DART non-blocking get operations in one trial at message size of 64 KB are shown in Figure 7. We can clearly see that DART non-blocking get communication operations support smaller overhead and higher application availability in all cases, compared to the baseline values. Obviously, at the work loop iterations of 2048, DART non-blocking get operations deliver less iter_t than MPI get operations in the case of intra-node by partly hiding the data transfer time. As we expected, DART-MPI get operations show less base_t than MPI get operations due to the usage of shmem-win, which also plays a part in improving the iter_t. For inter-node data transfers DART non-blocking get operations can even show less iter_t at 4096 than MPI get operations at 2048.

Figure 8 comparatively reports the application availability achieved with the DART non-blocking and MPI RMA operations as a function of the message size by repeating the above measurement. DART non-blocking RMA operations support slightly lower application availability than the transferred message sizes are not larger than 4 KB, which is in our expectation since the asynchronous progression feature is disabled in this case. Clearly, DART non-blocking RMA can get consistently better application availability than MPI RMA once the message sizes exceed 4 KB. MPI RMA operations show very poor application availability for message sizes larger than 1 MB. In addition, a sudden drop occurs at the message size of 8 KB in MPI RMA availability. This is also the reason for our enabling of DART asynchronous progress when message sizes are beyond 4 KB.

B. 3D heat conduction

Fig. 9. 3D heat conduction performance comparison.

Heat conduction plays an important role in engineering communities. It is a mode of heat transfer owning to molecular activity. We simulate the phenomenon of 3D heat conduction in solids with temperature-dependent thermal diffusivity based on an application code parallelized with MPI point-to-point [17]. In this benchmark, parallelization is done based on the checkerboard domain decomposition. For our evaluation, we port this implementation to DART one-sided directives. Also, we implement this 3D heat conduction algorithm based on MPI one-sided interfaces using passive target mode as the memory synchronization mechanism for a fair comparison. The boundary exchange is achieved by using non-blocking get operations. Particularly, MPI_Rget and MPI_Waitall are invoked in MPI implementation while dart_get (the progress process performs MPI_Rget inside) and dart_waitall are used in DART implementation. We stop the calculation after 5000 iterations and plot the average data results of 15 runs with small execution time variation reported.

A weak scaling calculation is presented in the Figure 9 with grid sizes varying from \((132 \times 128 \times 2048)\) to \((132 \times 4096 \times 2048)\). In this experiment, not only do we provide the total time performance, but we also test the message transmission time (also denoted as overhead in Fig. 9) that the CPUs are engaged in. The DART implementation provides an average speedup of \(1.122x\) on processes ranging from 96 to 3072. Although DART implementation dedicates less computing cores compared to the MPI implementation, it is still clearly observed that better total time performance can be achieved by using DART implementation due to that the majority of network latency has been hidden. Likewise, DART implementation makes good use of CPU for useful calculation and thus achieves less overhead via overlapping computation and communication. On average, the CPUs in MPI implementation spends 39% more time transmitting message than in DART implementation. In comparison to MPI implementation with the calculation constitutes an average of 65.8% of total time, the calculation in DART implementation takes an average of 75.8% of the total time.

IV. Conclusion

This paper has illustrated the design of enabling the asynchronous communications of DART non-blocking RMA for large message sizes by using the progress process-based approach. Such asynchronous progression can provide better communication and computation degree of overlap and meantime is designed to take the data locality into consideration. We have given a detailed evaluation on the performance improvement offered by the design using a Sandia MPI Micro-Benchmark (SMB) and a 3D heat conduction application benchmark. The results demonstrate that the communication-computation overlap can be efficiently achieved for large message sizes. According to the SMB evaluation for host processor overhead, the DART non-blocking RMA provides lower host processor overhead and higher availability than the MPI RMA does. Furthermore, the 3D heat conduction application evaluation shows that using DART asynchronous non-blocking RMA operations produces less calculation time than using MPI RMA interfaces for up to 3072 processes by partly hiding the communication latencies.
ACKNOWLEDGMENT

This work has been supported by the European Community through the project Polca (FP7 programme under grant agreement number 610686) and Mont Blanc 3 (H2020 programme under grant agreement number 671697). We gratefully acknowledge funding by the German Research Foundation (DFG) through the German Priority Programme 1648 Software for Exascale Computing (SPPEXA) and the project DASH.

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