Pressure-Tunable Ambipolar Conduction and Hysteresis in Thin Palladium Diselenide Field Effect Transistors

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Few-layer palladium diselenide (PdSe_2) field effect transistors are studied under external stimuli such as electrical and optical fields, electron irradiation, and gas pressure. The ambipolar conduction and hysteresis are observed in the transfer curves of the as-exfoliated and unprotected PdSe_2 material. The ambipolar conduction and its hysteretic behavior in the air and pure nitrogen environments are tuned. The prevailing p-type transport observed at atmospheric pressure is reversibly turned into a dominant n-type conduction by reducing the pressure, which can simultaneously suppress the hysteresis. The pressure control can be exploited to symmetrize and stabilize the transfer characteristics of the device as required in high-performance logic circuits. The transistors are affected by trap states with characteristic times in the order of minutes. The channel conductance, dramatically reduced by the electron irradiation during scanning electron microscope imaging, is restored after an annealing of several minutes at room temperature. The work paves the way toward the exploitation of PdSe_2 in electronic devices by providing an experiment-based and deep understanding of charge transport in PdSe_2 transistors subjected to electrical stress and other external agents.

1. Introduction

The relentless search for new 2D-layered materials beyond graphene has lately identified palladium diselenide (PdSe_2) as a new promising candidate for next-generation electronic and optoelectronic applications. PdSe_2 is the first discovered noble transition-metal dichalcogenide (TMDC) with 2D pentagonal structure. Monolayer PdSe_2 has a puckered configuration with a covalent Se-Se bond with ≈1.6 Å puckering distance. Compared to other TMDCs, PdSe_2 has a higher stability in air and is an indirect semiconductor with bandgap from 1.3 eV for the monolayer to 100 meV or less for the bulk. Such a high bandgap tunability is one of the most remarkable properties of PdSe_2 that has no equals in other 2D semiconducting materials. This important peculiarity of PdSe_2 could enhance its light absorption capability. The practical application of PdSe_2 can be further diversified by the strong spin–orbit coupling and the tunable topological quantum phase transitions as well as by the induced ferromagnetism with Curie temperature beyond room temperature. Hence, 2D pentagonal PdSe_2 is very promising for the design of new functionalities in higher performance electronic devices that combine the charge, spin, and other degrees of freedom resulting from the low symmetry.

The core of electronic devices applications depends on the transfer characteristics of PdSe_2-based field effect transistors (FETs), in which PdSe_2 offers ambipolar behavior, good on/off ratio, and high electron and hole mobility. Hysteresis usually occurs in the ambipolar transfer curve of the as-fabricated PdSe_2 FETs, which is claimed to be caused by process residues and adsorbates, but can be reduced by vacuum annealing. Hysteresis has been reported in FETs based on nanotubes, graphene, and TMDCs owing to charge transfer, charge trapping or charge polarization, although these mechanisms are still under debate. For example, in the MoS_2-based FETs, charge traps may arise...
from the trapping centers at MoS$_2$/SiO$_2$ interface,$^{[32,33]}$ the adsorbates on the MoS$_2$ channel,$^{[34,35]}$ or from intrinsic sulfur vacancies and other crystal defects.$^{[31,36,37]}$ It is highly desirable to have a comprehensive understanding of the hysteresis and achieve a good control so that it can be either eliminated to avoid threshold voltage instability or conveniently exploited, for instance, into memory devices.$^{[38–40]}$

It has also been found that the semiconducting phase of few-layer PdSe$_2$ can be changed to a semimetallic phase with an out-of-plane electric field.$^{[14,26]}$ Similarly, pressure can be used to mechanically tune the PdSe$_2$ lattice constant and achieve a modulation of the interlayer coupling and the electronic band structure.$^{[41,42]}$ When the pressure exceeds 3 GPa semiconducting to metal phase transition occurs in single crystal PdSe$_2$. Further increase in the pressure over 6 GPa transfers the structural phase of PdSe$_2$ to the pyrite phase, where the superconductivity emerges with critical temperature rapidly increasing in correlation with the weakening of the Se$_{\text{Se}}$ bonds.$^{[41,42]}$ Combining pressure and electric field control results in mechanical and electrostatic tuning of the crystalline structural and electronic properties, and enables tunable ambipolar behavior and hysteresis. This can make PdSe$_2$ suitable for potential applications in nanoelectromechanical devices and future complementary logic electronics.

Figure 1. a) Top and side views of the puckered pentagonal configuration of thin film PdSe$_2$. b) SEM image of the PdSe$_2$ flake with 5 nm Ti/40 nm Au metal contacts and (inset) schematic of the backgate transistor fabricated with it (not-on-scale). c) AFM image of the part of the device in the red box of b) and height profile along the lines marked as 1, 2, and 3 in the inset. The flake has a step height of 15 nm from the SiO$_2$ floor, that corresponds to ~25 PdSe$_2$ layers (see black line). d) EDXS, e) XRD pattern, and f) Raman spectrum of the flake.
In this paper, we exfoliate bulk crystals and fabricate backgate FETs to investigate several transport properties in thin PdSe₂ under external stimuli such as electrical and optical field, electron irradiation, gas exposure, and so forth. We present the transistor electrical characterization, with focus on the effects of the drain and gate voltage stress. We show that as-fabricated and unprotected PdSe₂ devices with Ti contacts exhibit ambipolar conduction with electron (hole) mobility up to 4 (3) cm² V⁻¹ s⁻¹, although measured a few months after the production. We study the gate hysteresis and the trap dynamics, and show how the exposure to electron beam irradiation, usually performed for imaging purposes, can have a temporary dramatic effect on the device performance. Importantly, we show that the control of pressure in air or pure-nitrogen ambient is a good knob to balance between the electron or hole conduction and to suppress the hysteresis. Hence, pressure can be used to set the symmetry of the transfer characteristics and to stabilize the device. These unexplored and important features of the electric transport in PdSe₂ are essential for the practical exploitation of this new material.

2. Results and Discussion

A scanning electron microscope (SEM) top view of the device and its schematic cross-section are shown in Figure 1b and its inset. The atomic force microscope (AFM) image in Figure 1c reveals a thickness of 15 nm for the exfoliated flake, which corresponds to about 25 layers. The energy dispersive X-ray spectrum (EDXS) and the X-ray diffraction (XRD) pattern in Figure 1d,e, respectively, indicate a Pd:Se atomic ratio close to 1:2 and a low-defect crystalline structure. The Raman spectrum of the flake (Figure 1f) displays five main distinct peaks slightly shifted with respect to theoretical peaks of bulk PdSe₂, consistent with the estimated number of layers.

The electrical characterization of a PdSe₂ transistor is summarized in Figure 2. The output characteristics, i.e., the \( I_{ds} \) drain–source current as a function of the \( V_{ds} \) drain–source voltage with the \( V_{gs} \) gate–source voltage as the control parameter, shown in Figure 2a, are symmetric and linear, revealing an ohmic behavior over the considered bias range. The linear \( I_{ds} - V_{ds} \) behavior is preserved under the application of the gate voltage, which only affects the overall drain-source conductance. The modulation of the channel current is further investigated with the transfer characteristic, \( I_{ds} - V_{gs} \) curve at given \( V_{ds} \), measured over a loop of the gate voltage and displayed both on logarithmic and linear scale in Figure 2b. The ~25 on/off ratio is a consequence of the number of layers, which imply a reduced bandgap and a limited gate control.

Differently from similar FETs based on TMDCs like MoS₂ or WSe₂, the PdSe₂ transistor exhibits a clear ambipolar behavior with a slight electron–hole asymmetry, and prevailing n-type conduction in high vacuum. The behavior mimics that observed in graphene transistors, with a prevailing n-type conduction in high vacuum. The behavior mimics that observed in graphene transistors, with a prevailing n-type conduction in high vacuum. The behavior mimics that observed in graphene transistors, with a prevailing n-type conduction in high vacuum. The behavior mimics that observed in graphene transistors, with a prevailing n-type conduction in high vacuum. The behavior mimics that observed in graphene transistors, with a prevailing n-type conduction in high vacuum.

In the linear region, the FET drain–source current can be expressed as

\[
I_{ds} = \frac{W}{L} \mu_{FE} C_{ox} \left( V_{gs} - V_{th} \right)^{\alpha} V_{ds}
\]

where \( W \) and \( L \) are the channel width and length, \( \mu_{FE} \) is the field effect mobility, \( C_{ox} = 1.15 \times 10^{-8} \text{ Fcm}^{-2} \) is the capacitance per unit area of the 300 nm SiO₂ gate dielectric, \( V_{th} \) is the threshold voltage, and \( \alpha \geq 1 \) is a dimensionless parameter which accounts for a possible \( V_{gs} \)-dependence of the mobility.[31,49,50] According to Equation (1), the \( I_{ds} - V_{gs} \) curve is linear, \( \alpha = 1 \), and the mobility can be obtained as

\[
\mu_{FE} = \frac{L}{W} \frac{1}{C_{ox}} \frac{1}{V_{ds}} \frac{\partial I_{ds}}{\partial V_{gs}}
\]

where \( \frac{\partial I_{ds}}{\partial V_{gs}} \) is the FET transconductance. Using the data and the slopes of the linear fittings of Figure 2b, Equation (2) yields a hole and electron field effect mobility of \( \mu_h = 0.86 \) and \( \mu_e = 4.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \), respectively.

In two-probe measurements, \( \mu_{FE} \) can be negatively affected by a high contact resistance \( R_c \).[18,51] However, the effect of \( R_c \) can be taken into account by replacing \( V_{ds} \) with \( V_{ds} - R_c I_{ds} \) in Equation (1). Assuming that the contact resistance is independent of \( V_{gs} \), as corroborated by the preserved linearity of the output curves with increasing \( V_{gs} \), it can be easily shown\[52\] that

\[
\frac{I_{ds}}{\sqrt{g_m}} = \sqrt{\frac{W}{L}} \mu_{FE} C_{ox} \left( V_{gs} - V_{th} \right)
\]

Equation (3) is used to extract the mobility, without the effect of the contact resistance, from the fit of the \( \frac{I_{ds}}{\sqrt{g_m}} \) versus \( V_{gs} \) plot shown in Figure 2c. The \( R_c \)-corrected hole and electron mobilities (0.90 and 4.2 cm² V⁻¹ s⁻¹) do not show a significant improvement, confirming a negligible effect of the contacts. Although higher electron (up to ~216 cm² V⁻¹ s⁻¹)\[20\] and hole mobilities (up to ~20 cm² V⁻¹ s⁻¹)[14] have been achieved in few-layer PdSe₂ transistors, values comparable to those here quoted have been reported for PdSe₂ thin films of similar thickness. Indeed, the mobility decreases rapidly with the number of layers after reaching a peak at 7–10 layers, a behavior found also in other puckered materials such as phosphorene.[14,53] We note also that the mobility is here measured on a device without any channel material treatment or optimization, and its enhancement with further device engineering can realistically be envisioned.

The effect of the drain bias on \( I_{ds} \) is studied in Figure 2d–f. The increasing \( V_{ds} \) results in a growing current without an appreciable effect on the transistor conductance \( \rho_{ds} \), as displayed in Figure 2e. Importantly, \( V_{ds} \) does not affect \( V_{gs}^{min} \), neither for the reverse nor for the forward sweep (Figure 2f), implying a negligible effect of the drain bias also on the transistor hysteresis. As the hysteresis is due to charge trapping in localized trap states,[27,31,34,54–57] this finding excludes the trapping modulation by lateral electric field at the interface with SiO₂, recently reported for instance in backgate MoS₂ FETs.[38]

Figure 3 shows two important features of the gate-induced hysteresis. By quantifying the hysteresis through its width
$H_w$, defined as the difference of the gate voltages corresponding to a current $I_{ds} = 50$ nA, we observe that $H_w$ increases quadratically with the $V_{gs}$ sweeping range, and is an exponentially growing function ($a - b \cdot e^{-x}$) of the $V_{gs}$ sweeping time. As already mentioned, the gate-induced hysteresis in FETs is caused by charge transfer from/to intrinsic and extrinsic trap states. Intrinsic traps correspond to PdSe$_2$ crystal defects such as vacancies or grain boundaries, while extrinsic traps are related to adsorbates from the environmental exposure, like H$_2$O and O$_2$ molecules, or to residues from the fabrication process. Water and oxygen, although identified as major hysteresis contributors in 2D-material FETs, are expected to be unimportant in the measurements of Figure 3 because of their desorption after several-hour annealing in high vacuum. Then, traps at the PdSe$_2$/SiO$_2$ interface and intrinsic PdSe$_2$ defects or border traps in SiO$_2$ as well as mobile charge in the SiO$_2$ layer are under the spot as the possible cause of the hysteresis.

Figure 2. a) Output and b) transfer characteristics of the PdSe$_2$ transistor measured at pressure $< 10^{-6}$ Torr. The fitting straight lines shown in b) are used to evaluate the field effect mobility. Reverse and forward refer to $V_{gs}$ swept from 50 to $-50$ V and from $-50$ to 50 V, respectively. c) Transconductance $g_m$ and $I_{ds}/\sqrt{g_m}$ ratio versus gate voltage, with linear fits to extract the mobility independent of the effect of the contact resistance. d) PdSe$_2$ FET current and e) channel conductance versus $V_{gs}$ for different drain biases. f) Gate voltage and current ($V_{gs \text{ min}}$ and $I_{ds \text{ min}}$) at the conductance minimum for the reverse and forward sweeps.
fast states (in the milliseconds range),[64] and corroborates the hypothesis of slow trap states related to either PdSe2 or SiO2 defects. While the nature of intrinsic traps in PdSe2 (perhaps not the most important ones, considering the high crystallinity of the sample) is still unclear, the slow border traps in SiO2, are attributed to trivalent silicon dangling bonds or hydrogenic defects.[66] Using the RC time constant, we can estimate the involved capacitance by considering that R is the inverse of the transconductance, which is ≈ 10 nS (Figure 2c). This corresponds to a capacitance of ≈ 5 μF, which is higher than that of the gate oxide of the device, in the order of the pF, implying that the trap-related capacitance is the dominant one. The same conclusion can be reached considering the sub-threshold swing SS, that is the gate voltage change corresponding to one-decade increase of the transistor current, that is expressed in terms of the trap (C_T) and channel depletion layer (C_{DL}) capacitances per unit area as

\[
SS = \frac{dV_{gs}}{d \log I_d} = \ln(10) \frac{kT}{q} \left( 1 + \frac{C_T + C_{DL}}{C_{ox}} \right)
\]  

(4)

(here, k is the Boltzmann constant and T is the temperature). Assuming C_{DL} negligible compared with C_T (a reasonable assumption considering the low modulation of the current), the relatively high SS = 30 V per decade obtained from Figure 2b or 3b yields the consistent trap capacitance, C_T = 5.7 μF, and a density of trap states D_T = \frac{C_T}{q} = 3.5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}.

A further confirmation that the time constants of several minutes can be attributed to the traps is provided by the transient behavior of the device, investigated through a series of V_{gs} = ± 50 V gate pulses in high vacuum, shown in Figure 3c,d. The trapping of charge corresponds to a reduction of the device current while the gate pulse is in the high positive or negative state. The RC delay from the V_{gs} pulses, consistent with that from HW transient, confirms the slow trap states. Furthermore, the independence of the time constant of the gate polarity indicates similar electron and hole capture/emission times.

The good stability and robustness of the device is reflected in the preservation of the current level and ambipolar behavior in the typical switching sequence displayed in Figure 3d.

Charge trapping at the PdSe2 defects and into the SiO2 topmost layers is also responsible for the device behavior under electron irradiation. Figure 4a compares the transfer characteristics of the transistor before and after the irradiation consequent to SEM imaging with 10 keV electron beam, corresponding to a fluence of about 4 electrons nm^{-2}. The electron beam irradiation has a dramatic effect, resulting in about an order-of-magnitude reduction of the channel conductance and a shift of the conductance minimum. The reverse and forward sweep curves move rightwards and leftwards, respectively. Figure 4a also shows that, after irradiation, the transfer characteristic slowly recovers approaching the initial state in a time of the order of hours. The electron beam generates electron–hole pairs in both the channel layer and the underlying dielectric and promotes the formation of defects.[43,47,67–69] This favors charge trapping and degrades the PdSe2 electrical conductivity. The 10 keV electrons are absorbed mostly in the SiO2 layer, where they create a pile-up of negative charge, which screens the gate field and affects the channel carrier conductivity. For positive V_{gs}, the electrons injected in the SiO2 are attracted towards the Si gate and oppose the positive gate voltage. As a consequence, a higher gate voltage is needed to start the
n-branch (right shift of $V_{gs}^{\text{min}}$); conversely, for negative $V_{gs}$, the electrons from the beam are pushed toward the PdSe$_2$ channel and contribute to its n-doping, such that a higher negative $V_{gs}$ is needed to initiate the p-branch (left shift of $V_{gs}^{\text{min}}$). The effect of the electron beam vanishes mostly with time rather than with the sweep repetition.

Indeed, Figure 4b,c shows that the restoring of $V_{gs}^{\text{min}}$ and $I_{ds}^{\text{min}}$ after irradiation, at room temperature, follows an exponential decay law with time constant of several minutes, consistent with the previously estimated trap time constant. Such observation confirms the key role played by the charge transfer and trapping between the PdSe$_2$ channel and the underlying SiO$_2$ gate dielectric.

Figure 4d shows a similar exponential recovery for the (n-branch) hysteresis and for the electron and hole mobilities. Such a behavior is easily understood considering that the slow diffusion or drift of the electrons from the beam, piled up in SiO$_2$, to the PdSe$_2$ channel (or the Si gate) simultaneously reduces the hysteresis and the Coulomb scattering which limits the carrier mobility. However, we note that the initial state is not completely restored, probably indicating some permanent radiation-induced channel damage.

We also checked the effect of optical irradiation but the device did not show any appreciable photoresponse, either in prevailing n- or p-mode. Figure 4e shows unchanged transfer characteristics upon illumination by the 880 nm LED used for optical imaging in the SEM chamber. The low intensity (up to 265 $\mu$W cm$^{-2}$) and the high wavelength of the LED that corresponds to low PdSe$_2$ absorption coefficient\textsuperscript{12,21,42} as well as the relatively high dark current, could likely concur to yield
a negligible photocurrent. Analogously, Figure 4f demonstrates that a white LED light or the laboratory illumination do not appreciably affect the typical increasing p-type current during air exposure. The weak photocurrent can be easily explained by considering the long transit time $\tau = \frac{L^2}{\mu V_n}$ in the channel, which results in low photocurrent gain $G = \frac{I_p}{I_n} \approx 1$ even for a PdSe$_2$ carrier lifetime $\tau$ as long as 100 ps as in black phosphorus.[70]

The control of the n- and p-type behavior, as well as of the hysteresis, is an important pre-requisite for the transistor exploitation in practical circuits. Ambipolar symmetry, high on/off ratio, and low hysteresis are highly desirable for stable low-power logic applications. Here, we show that exposure to air or nitrogen offers an easy knob to balance between n- or p-type conduction and to reduce the hysteresis. Favoring chalcogen vacancies and due to their high electronegativity, adsorbed O$_2$, N$_2$, and H$_2$O molecules capture electrons and induce a p-type doping in TMDC materials.[71–73] Indeed, Figure 5a shows that increasing pressure by air in a time of a few minutes has a dramatic effect on the PdSe$_2$ transistor. The increasing pressure gradually reduces the n-type conduction in favor of the p-type one and transforms the device from a prevailing n-type to a prevailing p-type transistor. In particular, the exposure to air for 10 min changes the transistor in a p-type depletion mode device. More importantly, the swapping from n- to p-type conduction is reversible, as demonstrated in Figure 5b, where the opposite trend from p- to n-type conduction is measured for the decreasing pressure. In particular, the $10^{-6}$ Torr vacuum after about 10 h resets the device close to its initial n-type state. Remarkably, Figure 5c shows that lowering the pressure reduces the hysteresis, both on the n- and p-branches. This effect, which is likely due to the gradual desorption of the adsorbates, provide a viable approach to the hysteresis control. In particular, it can be noted that a pressure below $10^{-4}$ Torr is as effective in reducing the hysteresis as is the atmospheric pressure in increasing it.

![Figure 5](image_url)
The electron and hole mobilities, obtained from both pressure cycles, show a decreasing trend with increasing pressure (Figure 5d), as reported also in graphene transistors.[74] Figure 5e shows a dependence of $I_{DSS}$ on the pressure. While the decreasing current with increasing pressure is easily understood as the effect of decreasing mobility caused by adsorbate-induced scattering, the crossover occurring around $10^{-4}$ Torr and the subsequent smoother increasing current with increasing pressure is non-trivial. Such increase goes against the decreasing mobility and could be related to a slight variation of the material bandgap caused by the adsorbates.[75] A lower bandgap could result in increased carrier density mainly for the reduced ionization energy of the trap states, which would increase their contribution to the free carrier density.

The enhancing effect of the pressure on the conductance and the carrier concentration has been measured for few-layer MoS$_2$ subjected to the high hydrostatic pressure, in the order of GPa, applied by means of diamond anvil cell.[76] A clear change of the transport properties of a single crystal PdSe$_2$ from the semiconducting to the metal phase occurring without a structural phase transition under the application of a high pressure of 3 GPa has been observed.[41] Moreover, an enhanced conductivity and carrier density, associated to a reduction of mobility, similar to what we have measured, has been predicted by density functional theory calculations in multilayer WS$_2$ subjected to high pressure, in the order of GPa, as the effect of bandgap closure due to pressure-increased interlayer and sulphur-sulphur interaction.[77] The data of Figure 5d,e suggest that an effect of the pressure on the transport properties of multilayer PdSe$_2$ is detectable at far lower pressures, although not directly related to a mechanical deformation.

Inert gases are easier to handle and are suitable for pressure control. An experiment with the pressure controlled in pure nitrogen ambient, is reported in Figure 5f, showing that N$_2$ (the electronegativity of which is close to that of oxygen, 3.0 versus 3.5 eV) can control the n- to p-type conduction conversion similarly to air. Then, the ambipolar characteristics of few-layer PdSe$_2$ can be strongly modulated by air or nitrogen. A similar behavior has been observed in transistors with few-layer black phosphorus exposed to oxygen.[78,79]

We highlight that these distinct pressure-tunable characteristics of PdSe$_2$ hold promises for the future development of new pressure modulated electronic devices and pressure sensors with ultrawide dynamic range.

### 3. Conclusions

We have fabricated backgate FETs with exfoliated few-layer PdSe$_2$ and studied their electric behavior under several environmental conditions and external stimuli. The devices exhibit an ambipolar behavior that is strongly sensitive to electrical stress, electron irradiation, and pressure. We have examined the dramatic effect of electron irradiation on the hysteresis and its recovery process, which are correlated to the slow trap states in the PdSe$_2$ and SiO$_2$. We have demonstrated that the control of pressure in air or pure nitrogen environment is an effective knob to switch between n- and p-type conduction and reduce the hysteresis in the transfer characteristics. This study provides new understanding and experimental evidence of the behavior of thin PdSe$_2$ as the channel of FETs and shows the great potential of PdSe$_2$ for the development of electronic logic devices and of pressure sensors with ultrawide range.

### 4. Experimental Section

The single crystals of PdSe$_2$ were synthesized by the method of self-flux.[80] The selenium powder (99.999%) and palladium powder (99.95%), which were purchased from Alfa Aesar, were mixed with an atomic ratio of Se:Pd = 2.1, and then were compressed into tablets. Next, the tablets were placed into a quartz tube that was sealed under 10$^{-3}$ mbar. After that, the sealed quartz was set in a muffle furnace and slowly heated in steps to the final synthesis temperature (850 °C), and then held at this temperature for 70 h to make the reaction fully process. After switching off the heating program, the muffle furnace was naturally cooled down to room temperature. The obtained polycrystalline samples of PdSe$_2$ were mixed with Se powder in a mass ratio of PdSe$_2$:Se = 1:4 and were sealed in another evacuated quartz tube. Then the above heating and cooling processes were repeated.

The PdSe$_2$ flakes were prepared from bulk PdSe$_2$ using the standard mechanical exfoliation method by adhesive tape. The exfoliation is facilitated by the low interlayer binding energy of ~0.35 J m$^{-2}$ of PdSe$_2$ (corresponding to ~62 meV atom$^{-1}$), which is smaller than that of graphite (0.37 J m$^{-2}$).[80] The flakes were transferred to degenerately doped p-type silicon substrates, covered with 300-nm-thick SiO$_2$, on which they were localized and identified using optical microscopy. Standard electron-beam lithography followed by metal electron-beam evaporation were carried out to deposit 5 nm Ti/40 nm Au metal contacts. The schematic and an SEM top view of the device here studied are shown in Figure 1b and in its inset, respectively. The AFM image of Figure 1c reveals a thickness of 15 nm for the flake, which corresponds to about 25 layers (assuming a thickness of 0.6 nm for a single layer).[14]

The chemical composition of the flake was measured by Hitachi S-3400 N II SEM EDXS, and the Pd:Se atomic ratio is close to 1:2 (Figure 1d).

The crystalline phase of the PdSe$_2$ flakes was characterized by the Bruker D8 Discover X-ray diffractometer with Cu K$_\alpha$ radiation ($\lambda = 1.5406$ Å) operating in Bragg-Brentano mode. The diffraction pattern (Figure 1e) of the sample confirms a layered PdSe$_2$ single crystal as shown by the presence of the characteristic peak at (0002) that indicates a strong orientation along the c-axis due to the layered crystal structure along the c-axis (the unit cell is orthorhombic with space group Pbcn). Moreover, the crystalline peak (023), detected in the XRD pattern, can be attributed to some exfoliated flakes not oriented with respect to the plane substrate.

The Raman spectrum (Figure 1f) was measured under excitation line of 514 nm by Renishaw inVia Raman microscope HS4304 and displays five distinct peaks typical of bulk PdSe$_2$. The peaks correspond to three $A_g$ and three $B_{1g}$ modes, with $A_{g1}$ and $B_{1g}$ very close and barely distinguishable. The first three modes at $\approx 208$, $\approx 208$, and $\approx 208$ cm$^{-1}$ (defined as $A_{g1}$ + $B_{1g}$, $A_{g1}$, and $B_{1g}$) are dominated by the movements of Se atoms, while the highest modes at 260 and $\approx 270$ cm$^{-1}$ (defined as $A_{g2}$ and $A_{g2}$) involve the relative movements between Pd and Se atoms. The measured peaks are slightly shifted with respect to the four main modes of bulk PdSe$_2$ (at 143, 206, 222, and 256 cm$^{-1}$), confirming the few layer nature of the flake.[14,32]

The device electric measurements were carried out using a Keithley 4200 semiconductor analyzer in a two-terminal configuration. The samples were measured inside a SEM chamber (ZEISS, LEO 1530) at room temperature, in dark and, if not otherwise stated, with controlled pressure below 10$^{-4}$ Torr. Source and drain (C1–C2 or C2–C3 leads in Figure 1b) were contacted with piezoelectric-driven tungsten probes while the sample holder electrically connected to the Si substrate by silver paint worked as the gate terminal.
Drain biases resulting in a current higher than 1 μA or |V_{gs}| > 50 V were avoided to prevent channel or gate dielectric damages.

Most of the measurement discussed in the paper were referred to the transistor formed between leads C1 and C2 (Figure 1b) characterized by channel length L = 2.0 μm and width W = 4.75 μm. The transistor formed by leads C2 and C3, as well as other devices from flakes with similar thickness, gave comparable results and were used as confirmation.

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Conflict of Interest
The authors declare no conflict of interest.

Keywords
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