1. Introduction

Smart sport has developed from no one’s attention to today’s hobbies and specialties. In the past, there were very few colleges and universities that developed smart sports. Nowadays, they can also get better results in international competitions. The current smart sports activities are all to improve their competitive ability. The intelligent sports training system is an organizational system established to achieve common goals. Competitiveness is one of the main manifestations of the evolution of the training system. With the rapid development of computer technology, people have begun to combine virtual reality with other technologies to realize scientific exercise-assisted training to eliminate traditional exercise training that relies solely on experience. This approach to the digital transformation of sports has created a large amount of sports intelligence data, which places higher demands on storage systems. This time, under the new semiconductor nonvolatile storage mode of data writing under the digitization of sports intelligence, the cache method is explored, and the problems that arise are designed to solve.

Although the smart sports derived from the current development are still in the initial stage of development, with the popularization and rapid rise of network data nowadays, more and more people have begun to have relevant understanding of it. In this digitalization process, at the moment when it is full, the digital network can help people understand it more accurately. This time, based on the latest semiconductor nonvolatile cache, the system for writing smart sports data is explored in order to find a better cache method. The experimental results show that not only the ternary cache further reduces the total energy consumption, but also the average energy consumption of the cache part is reduced by 22%, and the average energy consumption of the cache part is only increased by 9% compared with the single value type.
semiconductor memory device with an improved layout structure to achieve low power consumption, high speed, and miniaturization. The flash memory of the present invention includes a memory array formed of NAND-type strings. The memory array includes multiple global blocks, one global block includes multiple blocks, and one block includes multiple NAND-type strings. Multiple local bit lines are shared by each of multiple blocks in a global block, multiple global bit lines are shared by multiple global blocks, and connecting elements selectively connect one global bit line to \( n \). The local bit line has been included. When performing a read operation and a programming operation, a global bit line is shared by \( n \) local bit lines [1]. Yadav introduced in detail the synthesis of cobalt quantum dots (Co QDs) down to 1-2 nm and its application in nonvolatile memory (NVM) devices. The process of colloid synthesis is very simple, and a wide QD size can be controlled. The reduced colloidal Co QD is used in NVM device manufacturing. The colloidal synthesized Co QD is spin-coated on silicon dioxide wafers for the manufacture of floating gate NVM devices. The capacitance voltage (C-V) and capacitance time (C-t) measurements of the manufactured NVM device indicate the low voltage operation of the device. Scanning voltages as low as 1.2–4 V result in a flat-band voltage shift of 0.35–1.5 V, which is utilized in low operating voltage and low-power NVM applications [2]. Among various materials, polyoxometalate (POM) molecules have attracted considerable attention due to their use as new data storage nodes for nonvolatile memories. Here, Chen outlines the latest developments in POM development for nonvolatile memory. It also summarizes the general background knowledge of the structure and nature of POM. Finally, the challenges and prospects of POM’s application in memory are discussed [3]. Huang proposed two nonvolatile storage elements (NVSEs) based on racetrack memory for multicontext FPGAs. One is NVSE (type-1) based on variable speed, which has the advantages of high density and low power consumption. The other is the address-based NVSE (type-2), which has the advantages of fast context switching and low context switching capability. The general placement and routing simulation results show that the eight-context FPGA based on type-1 NVSE reduces the area, critical path delay, and power consumption of the SRAM-based eight-context FPGA by 68.1%, 22.8%, and 13%, respectively [4]. Micheloni introduced flash memory cards. Flash memory cards [mainly in a secure digital (SD) form factor] have almost completely replaced photographic film, and USB keys have wiped out floppy disks. Recently, due to the huge trade-off between cost and performance (i.e., write/read speed), NAND flash memory technology has begun to struggle with hard disk drives (HDDs) in the form of solid-state drives (SSDs) [5]. Li showed a golf-assisted training system that uses artificial intelligence and big data to realize the transformation from experience-based sports training methods to human movement analysis methods [6]. Explore how to use sensor data and visual artificial intelligence (AI) to improve the performance of athletes on the U.S. Olympic diving team. Desmond M described in detail how Microsoft cooperates with coaches, athletes, and project leaders to deploy sensor platforms and smartphone applications so that coaches can capture and analyze data related to athletes’ diving [7]. The research of the above scholars all requires very professional knowledge and in-depth understanding, as well as the operation ability of the most important experimental equipment, which are not easy to master at the same time. The experiment is too difficult and too complicated.

The innovation of this article lies in the data collection and writing of smart sports, which has not been developed more comprehensively. During this period of data fullness, the system design based on the nonvolatile cache under the large cache of smart sports data and the problems encountered in the process of writing data were solved.

2. Smart Sports Based on New Semiconductor Nonvolatile Cache

2.1. The Concept of Smart Sports. “Smart sports” is a comprehensive category given to it by everyone [8]. Smart sports programs are different from the equipment and venues required for traditional sports programs. In smart sports, the requirements for venues and equipment are not as high as in traditional sports [9].

Competitive sports are the basic characteristics of their sport, that is, confrontational, competitive, and athletic. There are many classifications and projects of smart sports [10], but the core must be confrontation and competition. Players’ skills and tactics must be improved through rigorous training and long-term practice [11]. Another essential and indispensable feature of smart sports is fair, just, and open competition under the guarantee of competition rules. From the above understanding, we can interpret the concept of smart sports as a sport activity based on rules in which student athletes use logical thinking, rich imagination, keen insight, and unique creativity. Unlike physical sports, smart sports include chess, go, and chess. Smart sports can exercise and improve participants’ thinking ability, judgment, reaction ability, attention, and perseverance, thus promoting their overall development [12].

2.2. The Basic Situation of Smart Sports Projects in My Country’s Colleges and Universities. According to the survey results, it can be seen that only 7 colleges and universities established 7 smart sports high-level sports teams from 1990 to 2001. Since 2001, the number of colleges and universities that have established smart sports high-level sports teams has increased by leaps and bounds to 35, an increase of 400% over the previous 10 years. 10 years ago, smart sports projects were only valued in culturally and economically developed areas and some well-known universities, and they were launched earlier, such as Peking University, Tsinghua University, Beijing Normal University, Fudan University, Shanghai University of Finance and Economics, and Nankai University, that is, intelligent sports high-level sports team. In other regions, due to the influence of policies, funds, culture, and other aspects, no high-level smart sports teams have been established in various universities. In the next year, due to the “three chess” entering campuses and the
development of “sunshine sports,” smart sports projects are only available. Gradually aroused the attention of education authorities at all levels [8]. Ten years later, until now, 35 colleges and universities have established smart sports high-level sports teams.

2.3. The Reasons Affecting the Development of Smart Sports Projects in Ordinary Colleges and Universities

2.3.1. The Influence of the Importance of the Leadership. The development and promotion of smart sports in Chinese colleges and universities is late, and the popularity rate is low. Some education departments and school leaders do not know enough about smart sports and think there is a big gap with the traditional sports programs in schools, so they do not support the opening of smart sports programs. In addition, in recent years, colleges and universities have compressed their expenses and streamlined their staff and institutions. This also directly affects the development of smart sports. The survey shows that the main factor affecting the development of smart sports programs in colleges and universities is the lack of teachers, but the main factor affecting the lack of teachers is directly related to the importance and attitude of leaders [13].

2.3.2. The Influence of the Policy Support of the Competent Authority. After 2001, due to the implementation of related smart sports activities, smart sports began to gradually develop in domestic universities. High-level sports teams, student associations, and more and more smart sports courses have been set up in international competitions. Good results have been obtained many times, and it can be concluded that the development of smart sports in colleges and universities is inseparable from the support of relevant policies.

2.3.3. The Influence of the Factors of Teachers. Due to the insufficient popularity of smart sports, there is a shortage of teachers. Most colleges and universities have not engaged in the study of smart sports. Although there are also colleges and universities that have developed smart sports, most of these college teachers do not have professional systematic training. They are self-study and work together with students. This is to a certain extent. The above has a serious impact on the development of smart sports in colleges and universities.

2.3.4. There Are No Related Teaching Materials and Syllabus Factors. According to investigations, colleges and universities that currently offer smart sports have yet to have unified teaching materials. This has seriously affected the learning of university teachers, professors, and students [14].

2.3.5. The Influence of Venue Equipment on Teaching Facilities. Only some early colleges and universities with smart sports have special training rooms and equipment for students, while most other colleges and universities are responsible for contacting venues and raising funds to purchase equipment to carry out activities [15].

3. Nonvolatile Cache of Ternary STT-RAM Based on Smart Sports Data Writing

Spin moment transfer magnetic memory (STT-RAM), compared to conventional memory, has the advantages of higher integration, lower static power consumption, and nonvolatility. Designing a high-density STT-RAM memory is the basis for building a large-capacity nonvolatile cache. This section mainly introduces the single-level cell (SLC) vs MLC structure, storage mechanism, and multivalue STT-RAM memory cell structure [16], briefly analyzes the shortcomings of the existing memory structure and ways to increase the storage density, and derives research on ternary STT-RAM with higher storage density.

3.1. STT-RAM Technical Analysis

3.1.1. Single-Value STT-RAM Technology. Single-value STT-RAM memory cell is a basic structure that constitutes STT-RAM memory [17]. As shown in Figure 1, a typical STT-RAM memory cell includes a magnetic tunnel junction and a transistor, which is called a single-transistor single-junction (MTJ for short) structure.

STT-RAM uses MTJ as a data storage element and expresses data through two or more resistance states of MTJ. For the most basic MTJ composition, it includes two magnet layers, which are separated by an oxide layer (MgO) [18]. The magnetization direction of one of the magnet layers is fixed and is called the reference layer; the magnetization direction of the other layer can be changed according to the current flowing, and it is called the free layer. When the magnetization direction of the free layer changes, the resistance of the MTJ also changes accordingly. The magnetization of the free layer is determined by the magnitude and direction of the current (polarization current) flowing through the MTJ. The polarization current must exceed a certain minimum value to be effective, which is also called the critical switching current [19]. In the single-value STT-RAM, each memory cell only needs to store 1 bit of data, so it is called the single-value type. The single-value MTJ contains only one free layer and one reference layer, and the magnetization direction of the free layer is relative to the magnetization direction of the reference layer: the same direction and the reverse direction [20]. When no voltage is applied to the MTJ, it maintains its original magnetization state, so it belongs to nonvolatile memory; that is, it can maintain data without applying voltage [21].

The drain of the transistor shown in Figure 1(a) is connected to the MTJ reference layer, the other end is used as a source connection selection line, and the gate is connected to the word line; the free layer of MTJ is connected to the bit line (BL). The operation of the STT-RAM storage unit includes three ways of writing “0,” writing “1,” and reading. When writing “0” to STT-RAM, the source terminal is connected to a positive voltage, and the bit line terminal is
3.1.2. Multivalue STT-RAM Technology. In order to improve the storage density, the STT-RAM memory cell structure of the multivalue storage mode has also been extensively studied, and two dual-value STT-RAM architectures have been proposed. Multivalued STT-RAM can store 2 bit or more data bits in a storage unit, effectively improving storage density. In a dual-value STT-RAM, an MTJ can have four resistance states, and correspondingly, there are four magnetization states in the free layer. Dual-value STT-RAM mainly includes two typical architectures: series dual-value type and parallel dual-value type [24]. As shown in Figure 2, the MTJ of the serial dual-value STT-RAM is formed by connecting two single-value MTJs of different sizes in series. The MTJ of the parallel dual-value STT-RAM is formed by stacking two free layers of different sizes side by side on the reference layer.

The design idea of MLC is to store more data through more resistance states in a memory cell. However, the research on MLC STT-RAM is currently mainly based on dual-value type, and the density increase is limited. The dual-value type STT-RAM memory cell can store 2 bits of information, and by implementing the three-value type, the STT-RAM memory cell stores 3 bits of information in eight resistance states, which can further increase the storage density. In this regard, this article aims at designing a large-capacity cache and conducts research on the design of ternary STT-RAM.

3.2. Serial-Parallel Hybrid Architecture Ternary STT-RAM Storage Design Based on Smart Sports Data Writing. Based on the series resistance based on the series dual-value STT-RAM architecture, it is not feasible [25], so this research takes the series-parallel hybrid type as the research theme. The series-parallel hybrid architecture three-valued MTJ consists of a parallel dual-value MTJ and a single-value MTJ in series. As shown in Figure 3, the architecture includes three free layers.

This time, $H_{1G}$ and $H_{J1D}$, $H_{3G}$ and $H_{3G}$, and $H_{3G}$ and $H_{J3D}$ are used to represent the high and low resistance values of the soft zone, hard zone, and top zone, corresponding to their respective data bits. The resistance of the serial-parallel hybrid architecture ternary MTJ can be expressed as

$$H = H_1 \| H_3 + H_3.$$  \hspace{2cm} (1)

Each ternary STT-RAM cell can store 3 bit data: from left to right are the most significant bit, the middle effective bit, and the least significant bit [26], which correspond to the three locations, respectively.

To obtain the best results by maximizing the distance between adjacent resistors, to confirm the parameters of MTJ, it is necessary to determine the relationship between the area of the soft zone and the hard zone, and use it to determine the area of the top layer.

There are four resistance combinations for the soft zone and the hard zone:

$$H_{00} = H_{2D} \| H_{1D},$$
$$H_{01} = H_{2D} \| H_{1G},$$
$$H_{10} = H_{2G} \| H_{1D},$$
$$H_{11} = H_{2G} \| H_{1G}.$$  \hspace{2cm} (2)

Use $\beta$ to represent the proportion of the parallel area occupied by the hard zone. Because the soft zone shares the...
same reference layer, it has the same resistance area product. Therefore,

\[ H_{2D} \times \beta = H_{1D} \times (1 - \beta) = H_{00}, \]
\[ H_{2G} \times \beta = H_{1G} \times (1 - \beta) = H_{11}, \]
\[ H_{11} = [1 + TMR]H_{00} = 2H_{00}. \]  

Therefore,

\[ H_{1D} = \frac{H_{00}}{1 - \beta}, \]
\[ H_{1G} = \frac{H_{11}}{1 - \beta}, \]
\[ H_{2D} = \frac{H_{00}}{\beta}, \]
\[ H_{2G} = \frac{H_{11}}{\beta}. \]  

The size of \( \beta \) determines the area ratio of the hard zone and the soft zone, which in turn determines the respective resistance values. The selection of \( \beta \) must satisfy the condition that the four resistances such as \( H_{00} \sim H_{11} \) are different from each other in order to express the four data.

\( H_{00} \) and \( H_{11} \) are the distance between the boundary resistance of the dual-valued single tube and the adjacent resistance. The solution of \( \beta \) is

\[ H_{11} - H_{10} = \frac{2(1 - \beta)}{2 - \beta}H_{00}, \]
\[ H_{10} - H_{01} = \frac{4\beta - 2}{(2 - \beta)(1 + \beta)}H_{00}, \]
\[ H_{01} - H_{10} = \frac{1 - \beta}{1 + \beta}H_{00}. \]  

(5)

Taking the derivation of \( \beta \) separately, we can find

\[ \frac{b(H_{11} - H_{10})}{b\beta} < 0, \]
\[ \frac{b(H_{01} - H_{00})}{b\beta} < 0, \]
\[ \frac{b(H_{10} - H_{01})}{b\beta} > 0. \]  

(6)

With the growth of \( \beta \in (0.5, 1) \), in the scenario of \( H_{01} - H_{00} = H_{10} - H_{01} \), the minimum distance of the four resistances reaches the maximum, and \( \beta = 0.6277 \) is obtained, and the parallel hard zone area \( (\beta/(1 - \beta)) = 1.686 \) times can be obtained.

The area product \( RA \), the resistance value, and the critical conversion current are extracted. According to the area ratio relationship, the various parameters of the series-parallel hybrid architecture ternary MTJ can be calculated, as shown in Table 1.

3.2.1. Sports Smart High-Energy Writing Drive Capability. Using the traditional STT-RAM drive circuit design, with a larger size NMOS to provide sufficient write drive current for the ternary MTJ affects the overall storage density improvement. NMOS is an N-type metal oxide semiconductor, and transistors with this structure are called NMOS.
Table 1: STT-RAM structure and height resistance value.

| Parallel MTJ area | Top MTJ area | Soft-area ratio | Hard zone area ratio |
|-------------------|--------------|-----------------|---------------------|
| 40 × 90           | 50 × 100     | 0.36            | 0.64                |

| “1” current | “0” current |
|-------------|-------------|
| ICS         | 47.3        |
| ICT         | 56.6        |
| ICTH        | 79.9        |
| ICS         | 32.5        |
| ICT         | 66.5        |
| ICTH        | 82          |

| Resistance |
|------------|
| H1D        | 11          |
| H2D        | 6.5         |
| H3D        | 5           |
| H1G        | 22          |
| H2G        | 14          |
| H3G        | 10          |

The resistance of the eight states of the ternary MTJ

| 0000 | 9     | 10   |
| 0100 | 12    | 13   |
| 1000 | 15    | 15   |
| 1100 | 16    | 19   |

In the ternary STT-RAM, the voltage drop of the NMOS tube, and the current intensity, so the operation of writing “1” is also more difficult. Based on this, the reverse stacking method is used to reduce the current demand when writing data.

The drive strength of NMOS is affected by the voltage drop $I \times H$ caused by MTJ. When writing “0,” the current direction is from the gate to the source, $\Phi_{GS}$ is applied to the bit line and the gate, and the source is grounded:

$$\Phi_{GS} = \Phi_{DD},$$

$$\Phi_{DS} = \Phi_{DD} - I \times H,$$

(7)

where $I$ represents the magnitude of the current flowing through the MTJ and $H$ is the resistance value of the MTJ. $\Phi_{GS}$ is the voltage drop between the gate and the source of the NMOS tube, and $\Phi_{DS}$ is the voltage drop between the drain and the source.

For the size of MYN NMOS, its drive current IDS can be expressed as

$$I_{DS} = K \cdot \frac{M}{V} \cdot (\Phi_{GS} - \Phi_{TH}) \cdot \Phi_{DS} - \frac{\Phi_{DS}^2}{2}.$$  (8)

It can be seen from the above equation that for single-value STT-RAM, the voltage drop was $I \times H$ in $\Phi_{DS}$ when writing “1” results in a decrease in the driving capability of NMOS. Moreover, writing “1” makes the magnetization direction of the free layer opposite to that of the reference layer, which requires higher magnetization current intensity, so the operation of writing “1” is also more difficult.

According to equation (8), calculate the write current that NMOS of different sizes can provide. As shown in the result of Figure 4(a), when the size of the NMOS is increased to 10F, the current demand for writing a “1” in the hard location still cannot be met. At the same time, the size of the NMOS has offset the storage density of the ternary type, reducing it to the level of the single-value type. As shown in Figure 4(b), it can be found that the drive current $I_{DS}$ before the reverse connection is lower than the critical switching current $I_{CBI}$, which is not enough to support the flip of the hard area; after the reverse connection, the writing current of the hard area increases, which is higher than the critical switching current $I_{CBI} (0 > 1)$.

By analogy, in addition to the reverse connection of the MTJ of the hard zone, the MTJ corresponding to the top zone can also be reversed. Therefore, consider the reverse connection of the two MTJs in the three-value type. There are three types of reverse connection methods, as shown in Figure 5:

The hard zone is the operation that requires the most write current. When writing to the hard zone, the corresponding resistance value that causes the voltage drop under different reverse connections of the three-valued MTJ is shown in Table 2.

| Resisance | 0000 | 9     | 10   |
|-----------|------|-------|------|
| 0100      | 12    | 13    |
| 1000      | 15    | 15    |
| 1100      | 16    | 19    |

Substituting the values in Table 2 into the equation, the drive current in the hard zone as shown in Figure 6 is obtained.

After reversing the MTJ, when writing a “1” to the hard zone, the voltage drop of VGS is first eliminated; secondly, the soft zone and hard zone caused by a short period of time are flipped to “0,” turning the high-impedance state to low-impedance state, reducing the pressure drop $\Phi_{DS}$ of $I \times H$. Inverting MTJ balances the drive capability of NMOS when writing “1” and writing “0.” Although it reduces the current drive ability when writing “0,” it increases the ability to write “1” and eliminates writing “1,” worst bias condition. In this article, the BR flip mode is selected as a compromise. Under the condition of a width of 4.5 F, the current required for writing a “0” to the hard zone bit can be met, while the current required for writing a “1” can be met.

3.2.2. Reading Logic of Storage Unit Based on Smart Sports Data Writing. The reading method of dual-value nonvolatile memory has a mature design. The reading method of this research is based on a binary tree reading method that is relatively balanced in all aspects. The read logic is shown in Figure 7.

Each three-valued STT-RAM memory cell stores 1 bit more data than the dual-valued STT-RAM memory cell. Therefore, on the basis of the dual-valued type reading, by adding a level of reading logic, the third bit of data read out.

Therefore, the three-valued reading logic can refer to the dual-valued reading method to read the upper two bits first, and then we only need to add a set of judgment thresholds $\Phi_{ref4}, \Phi_{ref5}, \Phi_{ref6},$ and $\Phi_{ref7}$ to meet the requirements of the equation. Read the lowest bit:

$$\begin{cases} \Phi_{b000} < \Phi_{ref4} < \Phi_{b001} \\ \Phi_{b010} < \Phi_{ref5} < \Phi_{b011} \\ \Phi_{b100} < \Phi_{ref6} < \Phi_{b101} \\ \Phi_{b110} < \Phi_{ref7} < \Phi_{b111} \end{cases}$$  (9)

Based on the above analysis, the read logic of the ternary STT-RAM as shown in Figure 8 is obtained.

3.3. Writing Logic Design of STT-RAM Storage Unit Based on Smart Sports Data Writing. The ternary STT-RAM memory cell can use three magnetization layers to store 3 bit data. Due to the inconsistency of the characteristic parameters
Figure 4: Hard bit current of the top layer in two modes. (a) Standard mode and (b) reverse mode.

Table 2: The corresponding voltage drop resistance of the four modes.

|       | Standard | TR | PR | BR |
|-------|----------|----|----|----|
| 1     | $\Phi_{CH}$ corresponds to voltage drop resistance | 19 | 14 | 0  | 0  |
|       | $\Phi_{DS}$ corresponds to voltage drop resistance  | 18 | 14 | 14 | 18 |
| 0     | $\Phi_{CS}$ corresponds to voltage drop resistance | 0  | 0  | 13 | 10 |
|       | $\Phi_{DS}$ corresponds to voltage drop resistance  | 9  | 15 | 13 | 10 |

Figure 6: Two groups of transistor body hard zone write currents in four modes.
such as the physical size of the three magnetization layers, and the inconsistent influence of each other during the writing process, the characteristics of the writing delay and energy consumption of the three data bits are inconsistent. It is necessary to design write logic for this problem to achieve fast data write and reduce write energy consumption.

The characteristics of the direct writing method: The reason why the direct writing method is used is that the current required for writing in the hard zone, the top zone, and the soft zone is different, and the applied current is caused to other magnetized layers when the target-free layer is magnetized. The role is different. Among them, the soft zone can use a small current to switch the magnetization direction, while the hard zone requires a relatively large current, and the write current in the top zone is in the middle.

For an STT-RAM memory containing X-bit data, assuming that random data is written, that is, the data satisfies the Gaussian distribution, then eight types of data for each memory cell are written with equal probability. Use $Q_0$, $Q_1$, and $Q_2$ to represent the execution probabilities of the magnetization operation of the three storage cells—hard location, top location, and soft location, respectively; then,

\[
Q_i = \begin{cases} 
\frac{1}{3}, & i = 0, \\
\frac{1}{3}, & i = 1, \\
\frac{1}{3}, & i = 2. 
\end{cases}
\]  

If the memory is written once, the total number of write operations is $M = N$, and the number of each write operation is

\[
M_i = Q_i \times M,
\]

\[
M_i = \begin{cases} 
\frac{1}{3}N, & i = 0, \\
\frac{1}{3}N, & i = 1, \\
\frac{1}{3}N, & i = 2. 
\end{cases}
\]
The direct writing method is simple. For all three-valued STT-RAM memory cells, you only need to write each bit of data in the order of hard location, top location, and soft location, but the write delay is the sum of the write delays of the three free layers, which causes the write performance to be much lower than the single-value and dual-value STT-RAM, and the number of write operations required to fill a memory is large, resulting in high write energy consumption.

(1) Writing method based on the classification of the written value: According to the different magnetization operations actually required for different writing data, the writing process is designed separately, and the writing operation is reduced in a targeted manner to reduce the writing delay and energy consumption.

There are three types of magnetization for the dual-value writing method: (1) soft zone reversal (ST), applying a small current IS, only realizing the magnetization reversal of the soft zone; (2) top zone reversal (TT), where the strong current makes the soft zone and the top zone magnetized in the same direction; (3) hard zone flip (HT), applying a large current IH, magnetizes the hard zone, the soft zone, and the top zone in the same direction, which is shown in Figure 9.

For an STT-RAM memory containing X-bit data, assuming that random data is written, that is, the data satisfies the Gaussian distribution, then eight types of data for each memory cell are written with equal probability. After adopting the write method based on the written value classification, the probabilities of ST, TT, and HT operations are

\[
Q_i = \begin{cases} 
\frac{1}{4} & i = 0, \\
\frac{1}{4} & i = 1, \\
\frac{1}{4} & i = 2.
\end{cases}
\] (12)

If the memory is written to once, the total number of write operations is \( M = \frac{2}{3}N \), and the number of each write operation is

\[
M_i = \begin{cases} 
\frac{1}{6}N, & i = 0, \\
\frac{1}{6}N, & i = 1, \\
\frac{1}{6}N, & i = 2.
\end{cases}
\] (13)

Compared with the direct write method, the ST and TT operations are reduced by 50%, and the HT operation is not reduced. Although this writing method based on the written value reduces a lot of operations compared with the direct writing method, since the current state of the MTJ is not considered, there are still redundant operations.

(2) The writing method based on the difference between the written value and the current value: in order to further reduce the operation of redundant writing, this writing classification method based on the difference between the written value and the current value is compared with the above two methods. The current value of MTJ. The specific process is as follows: first insert a read operation, read the state of the MTJ, and then perform the corresponding magnetization operation according to the current value of the MTJ and the difference of the target value to be written. Then, the write operation is simplified to the type shown in Figure 10, and some HT operations are replaced by TT and ST operations.

For an STT-RAM memory containing N-bit data, assuming that random data is written, that is, the data satisfies the Gaussian distribution, then eight types of data of each memory cell are written with equal probability. After adopting the write method based on the difference between the written value
and the current value, the probabilities of ST, TT, and HT operations are

\[
Q_i = \begin{cases} 
\frac{1}{3} & i = 0, \\
\frac{1}{3} & i = 1, \\
\frac{1}{3} & i = 2.
\end{cases}
\]  

(14)

Write a full memory; the total number of write operations is \( M = (7/12)N \), and the number of write operations is

\[
M_i = \begin{cases} 
\frac{7}{36}N & i = 0, \\
\frac{7}{36}N & i = 1, \\
\frac{7}{36}N & i = 2.
\end{cases}
\]  

(15)

For random write operations, the operation probability of ST, TT, and HT is all 1/3, and the total number of writes is reduced by 12.5%. Compared with the write operation, the read operation has shorter latency and lower energy consumption. Although the read operation requires three comparisons and judgments to obtain the final data, for most write operations, it still brings considerable writing increased entry speed.

3.4. Cache Design of Ternary STT-RAM with Serial-Parallel Hybrid Architecture Based on Smart Sports Data Writing

(1) Cache hierarchical mapping method: The simple and direct method to build a three-valued STT-RAM cache is to refer to the direct mapping method of the two-value STT-RAM cache; that is, every N/3 STT-RAM storage unit constitutes a group N-bit memory page. Each page has 1/3 of the data stored in the soft location, hard location, and top location, and all pages have the same characteristics.

For ternary STT-RAM, the write speed of the soft zone is the fastest, and the speed of the hard zone is the slowest. Because there are soft zone, top zone, and hard zone in the same page, the read and write performance of the page depends on the slowest the performance of the data bits.

(2) Different levels of page exchange methods: according to the read and write operation methods and page types, page exchange operations can be divided into four types: read page exchange between related pages and write page exchange between related pages; and read page between unrelated pages exchange and write page exchange between unrelated pages; the four exchange operations have different costs.

Analyzing the four page operations of the table, it can be seen that the selection of the threshold determines the exchange timing and frequency, and ultimately affects the exchange cost and overall performance. In terms of swap operation cost, since the read delay of soft zone pages is higher than that of hard zone pages, and the write delay of soft zone pages is lower than hard zone pages, so in the read page swap, the swap operation cost of soft zone pages is less than that of the hard page. In terms of overall performance after the swap, the benefits of soft page operations are higher than those of hard page operations; in addition, in page write operations, the benefits of hard pages are higher than top-level pages. Therefore, the swap threshold of soft zone pages can be designed to be lower than that of hard zone pages to increase the swap probability of soft zone pages; similarly, the swap threshold of hard zone pages can be designed to be lower than that of top zone pages to increase hard zone pages.

(3) Selection of page swap threshold: the swap threshold is used to control the frequency of page swap. When the number of page reads and writes reaches the threshold, the page swap operation is started. If the threshold is too low, the page swaps are too frequent, which will cause performance degradation due to the operating cost of page swaps; if the threshold is too high, the page swap frequency is too low, and the hit rate of pages in the soft zone and the top zone cannot be fully improved. Therefore, it is necessary to comprehensively select the threshold for the impact of the exchange threshold on the page exchange operation cost and hits.

As shown in Figure 11 (1), when the threshold is adjusted from 4 to 64, the overall IPC performance is improved. This is because increasing the exchange threshold reduces the number of exchanges and reduces the impact of exchange operation costs on read and write delays. However, when the threshold is further increased, the frequency and number of exchanges are effectively reduced, which further affects the reduction of the page hit rate. Figure 11 (2) shows the change in cache energy consumption when the threshold is adjusted from 4 to 64. Combining the two effects, it is obvious that the
energy consumption of TPC is decreasing, from 0.97 to 0.86. 16 is selected as the read page exchange threshold, and 32 is selected as the write page exchange threshold.

4. Simulation Experiment and Result Analysis

The design goal of the ternary STT-RAM cache is to improve the number of instructions per cycle (IPC) performance and reduce energy consumption, so this article uses IPC and energy consumption as evaluation indicators. The page exchange method is of great significance to the improvement of IPC and energy consumption. In order to evaluate the effect of the page exchange method, this article also compares and simulates the page hit rate before and after the page exchange method is adopted. Through the comparison simulation experiment of ternary and single-value and dual-value STT-RAM caches, the rationality of the ternary STT-RAM design of the series-parallel hybrid architecture is verified through comparative simulation experiments of ternary and single-value and dual-value STT-RAM cache configurations, benchmark suites, warm-up stages, and modeling technology nodes.

In the actual simulation experiment, in order to reduce the recording error, the experiment was repeated three times, and the average value of the three test results was taken as the simulation result.

4.1. Page Hit Rate Based on Smart Sports Data Writing

The hit rate is the most direct way to analyze the efficiency of the page swap algorithm. This section discusses the impact of different levels of page swap designs on the page hit rate. The experimental results of the hit rate of the top area page and soft-area page of the three-valued STT-RAM cache after adopting this design are shown in Figure 12.

As shown in Figure 12, after adopting the page swap mapping algorithm, for various benchmark tests, the hit rate exceeded 50%, the average write hit rate (avg) of soft zone pages reached 71%, and the average read hit rate of pages in the top zone (avg) has also reached 63%. Among them, the soft zone page write hit rate corresponding to the zeusmp test benchmark has increased to 83%, which is a very obvious improvement.

4.2. IPC Performance of Nonvolatile Storage Based on Smart Sports Data Writing

The simulation result of IPC performance is shown in Figure 13. It can be seen from Figure 13 that for different types of test benchmarks, the performance of the three-valued STT-RAM cache that only uses hierarchical page mapping is improved and some are reduced compared with the single-valued type. In benchmark tests that are sensitive to cache capacity, such as bzip2 and mcf, because the three-value type has a larger capacity, it reduces the probability of missing and reduces the cost of missing. The direct mapping method improves performance in some test loads; while in GCC, HMER, LBM, and other benchmarks, these tests are more sensitive to cache access latency; on the contrary, due to the high read and write latency of hard page pages, cache performance has declined. For the gcc test, compared to the single-value type, the performance drops by 10%; compared to the dual-value type, the performance drops by 5%.
After the combined use of different levels of page mapping, for the bzip2 benchmark test, it has increased by 36% compared to the three-valued type and 15% compared with the two-valued type. For the gcc test, which has the lowest improvement rate, has also been improved by 7% and 15%, respectively. The average performance of the ternary cache is 16% higher than that of the SLC type and 12.6% higher than that of the dual-value type.

4.3. Energy Consumption of Nonvolatile Storage Based on Smart Sports Data Writing. The discussion of energy consumption includes two parts: STT-RAM cache energy consumption and memory energy consumption. The simulation results are shown in Figure 14. Each bar graph represents the sum of memory and cache energy consumption. The upper part (slashed area) represents the energy consumption of the cache, and the lower part represents the energy consumption of the memory.

It can be seen from Figure 14 that, for the energy consumption of the cache part, the single-valued cache has the lowest energy consumption. This is because the read and write operations of the single-valued STT-RAM only require one operation to complete. The read disturb rate in STT-MRAM cache is reduced by selective tag comparison; however, the total energy consumption of single-valued cache and memory is the highest. This is because the single-valued cache has the smallest capacity and high miss rate, which leads to a large number of memory access operations and increases the energy consumption of the memory part.

Compared with the single-valued type, the energy consumption of the dual-valued type and the three-valued type cache that only uses hierarchical page mapping has increased significantly, because the write operation requires more steps and higher current to complete. Among them, the three-value type has a greater improvement, and the average energy consumption of the cache part of each test has increased by 26%. Because the three-valued cache has the largest capacity and the lowest cache miss rate, the energy consumption of the memory is the lowest, and the total energy consumption of the generated cache and memory is also the lowest. Compared with the single-value and dual-value caches, the average total energy consumption is reduced, respectively. Different levels of page exchange design are used, by reducing the operation of hard positioning, triadic cache.

It not only further reduces the total energy consumption but also reduces the energy consumption of the cache part to be close to that of the single-value cache; compared with before the page swap, the average energy consumption of the cache part has been reduced by 22%, and the average total energy consumption has been reduced (3.9%). Compared with the single-value type, the average energy consumption of the cache part has only increased by 9%, while the average total energy consumption has been reduced by 12.3%.

5. Conclusions

In this article, based on the writing of huge sports data, in order to further explore a better caching method, a three-valued STT-RAM caching method based on page swap design is proposed, and a more excellent test result is achieved; the reason for the increase in the hit rate is that the method in this article transfers the write operations that hit the top-level page and hard-area page to the soft-area page, and transfers the read operation that hits the soft-area page and hard-area page to the top-level page through the page swap method. The reason for the improvement of IPC performance is that different levels of page swaps reduce the access to slow hard pages, and increase the access to the top-level pages with fast read speeds and the soft pages with fast write speeds, making the pages average. The access delay is reduced. From the above results, it can be found that the three-valued STT-RAM cache using the page swap algorithm is compared with the single-valued cache of the same area, while the performance is improved, and the energy consumption is also reduced. It not only exerts the advantages of three-valued capacity, but also utilizes the performance advantages of hierarchical pages through the page swap algorithm, and reduces the write delay and read delay.
Data Availability
Data sharing is not applicable to this article as no datasets were generated or analyzed during this study.

Conflicts of Interest
The author declares that there are no conflicts of interest with any financial organizations regarding the material reported in this manuscript.

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