Conversion Gain Enhancement in Standard CMOS Image Sensors

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Abstract. This paper focuses on the conversion gain (CG) of pixels implementing pinned photo-diodes (PPD) and in-pixel voltage follower in standard CMOS image sensor (CIS) process. An overview of the CG expression and its impact on the noise performance of the CIS readout chain is presented. CG enhancement techniques involving process refinements and pure circuit design and pixel scheme optimization are introduced. The implementation of these techniques in a 180 nm CIS process demonstrates a progressive enhancement of the CG by more than a factor 3 with respect to a standard reference pixel from the same foundry, allowing a better understanding of the different parasitic elements on the sense node capacitance and CG.

Keywords: CMOS image sensors; pinned photodiode, pixel conversion gain; sub-electron noise; sense node.

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1 Introduction

Pinned photo-diode (PPD) based image sensors performance has been dramatically increased since their first development\textsuperscript{1} on several aspects including speed, resolution or power consumption. PPD compatibility with complementary metal oxide semiconductor (CMOS) process makes these devices an excellent candidate for a wide range of applications combining performance, miniaturization, large volume and low cost criteria.\textsuperscript{2–4} The sensitivity of CMOS image sensor (CIS) has been, also, remarkably improved in terms of quantum efficiency, dark current and fill-factor.\textsuperscript{1} Recently, remarkably low noise pixels, operating at room temperature, have been presented\textsuperscript{5–9} reaching noise levels below a single electron. These improvements have been followed by demonstrations of photo-electron counting capability with CMOS image sensors without any photo-electron multiplication process.\textsuperscript{6,7}

Noise reduction circuit techniques such us correlated sampling or column-level gain and bandwidth control,\textsuperscript{10–13} proved their efficiency in bringing the input-referred noise of CIS readout chains to sub-electron levels. Nevertheless, deep sub-electron levels close to 0.3 electrons RMS, at room
temperature, could only be reached with pixel conversion gain enhancement through sense node (SN) capacitance reduction.\textsuperscript{6,8,14,15} The common concept to these SN capacitance reduction techniques is the isolation of the SN from the parasitic capacitance related to the neighboring gates. This is achieved by means of process refinements or design changes that come at the cost of low pixel full well capacity (FWC) and high required voltages.

A variety of techniques involving process variations or different pixel schemes have been recently presented.\textsuperscript{6,8,14,15} However, there is still some room left for demystifying the impact of the different SN area design parameters on the SN capacitance and the conversion gain in a standard CIS process. The aim of this work is to analyze the impact of the SN and in-pixel source follower (SF) design on the conversion gain and SN capacitance. The suggested way to achieve this is to implement on a same CIS array different types of pixels embedding different techniques reducing gradually the SN parasitic capacitance or increasing the conversion gain within the standard CIS process design rules boundaries. Analyzing the conversion gain measured out of the different pixel types using its formula allows extracting the contribution of the different terms and understanding the impact of each optimization step.

This paper starts with an overview of the conversion gain expression and its impact on the noise performance on the CIS readout chain. Conversion gain enhancement techniques involving process refinements, pure circuit technique and pixel scheme are introduced throughout three pixel designs. The implementation of these techniques in a 180 nm CIS process demonstrates a progressive enhancement of the conversion gain by more than a factor 3 with respect to a standard reference pixel from the same foundry. This progressive increase enables a better understanding of the impact of the SN parasitic capacitance and SF design on the conversion gain.
Fig 1 Conventional 4T pixel schematic and corresponding readout timing diagram. The schematic depicts a cross section showing the PPD structure built on an epitaxial layer ($p_{\text{epi}}$) lightly p doped with respect to the substrate ($p_{\text{sub}}$). The borders of the PPD are protected by shallow trench isolation (STI).

2 The Conversion Gain: A Key Parameter in Low Noise PPD & SF based CIS Pixels

Fig. 1 shows a conventional 4T pixel schematic together with its readout timing diagram. The pixel embeds a PPD integrating the photo-generated electrons, a transfer gate (TG) allowing the transfer of these integrated charges to the SN and splitting the latter from the PPD well capacitance. A reset gate (RG) allowing setting the SN to a high voltage before each transfer. When the row select (RS) switch is closed, the SF transistor buffers the voltage level of the SN to the column to be processed by the rest of the readout chain. Conventional CIS embed an array of pixels and column-level
readout circuits performing a rolling readout scheme. All the pixels of a same line are readout in parallel. The column-level circuitry embeds, a correlated double sampling (CDS) scheme that takes a sample before and after the charge transfer from the PPD to the SN, an amplifier improving the signal-to-noise ratio (SNR) in case of low light conditions and an analog-to-digital converter (ADC).

The pixel conversion gain is the voltage difference that the SF creates at the column level for a single electron transferred from the PPD to the SN. Increasing this gain mitigates the impact of the noise generated at the column-level circuits which is key in low light application and also for reaching photo-electron counting capability.

The pixel SN is an area in which every fraction of a fF counts. The different elements contributing to the SN parasitic capacitance are depicted in Fig. 2 and further detailed in. The in-pixel SF is far from behaving as an ideal voltage follower. In other words, the conversion gain is not simply given by the inverse of the SN capacitance. Hence, a small signal analysis taking into account both the SN and SF parasitic capacitance is necessary to express the conversion gain. Using the small signal analysis detailed in, the conversion gain, denoted $A_{CG}$, can be formulated in the
following from:

\[ A_{CG} = \frac{1}{n} \frac{C_{SN} + C_e W + (1 - \frac{1}{n})(C_e W + C_iWL)}{C_{SN} + 2C_e W + (1 - \frac{1}{n})(C_e W + C_iWL)}, \]  

(1)

where, \( C_e \) and \( C_i \) are the SF intrinsic and extrinsic capacitance densities, \( W \) and \( L \) are the SF gate width and length, \( C_{SN} \) is the total SN capacitance including the junction, overlap with reset and transfer gates as well as metal wires parasitic capacitances as illustrated by Fig. 2 and \( n \) is the slope factor of the source follower transistor. In saturation, the value of \( n \) ranges from 1.2 to 1.6 and slowly tends to 1 for high \( V_G \).\(^{19}\)

Eq. 1 shows that \( A_{CG} \) depends on the SN capacitance, the SF parasitic capacitance and the SF body effect.

The conversion gain plays a key role in the noise performance of the CIS readout chain. The noise generated outside the pixel is directly mitigated by a higher conversion gain since its input referred variance is simply divided by \( A_{CG}^2 \). Regarding the noise generated at the level of the SF stage, both the input referred thermal and 1/f noise expressions share similar terms with \( 1/A_{CG} \). Indeed, the SF 1/f noise can be expressed as:

\[ Q_{1/f}^2 = \frac{\alpha_{1/f}}{C_{ox}^2 W L} K_F (C_{SN} + 2C_e W + C_iWL)^2, \]  

(2)

where \( K_F \) is a process and temperature dependent parameter, \( C_{ox} \) is the oxide capacitance density and \( \alpha_{1/f} \) is unit-less design dependent parameter resulting from the CDS effect on the 1/f noise.

The thermal noise originating from the pixel SF stage can be expressed as:

\[ Q_{th}^2 = 2f_n \frac{kT \gamma_{SF}}{G_{m, SF}} (C_{SN} + 2C_e W + C_iWL)^2, \]  

(3)
where \( k \) is the Boltzmann constant, \( T \) the temperature, \( f_A \) is an equivalent frequency dependent on the column-level amplifier design and bandwidth, \( \gamma_{SF} \) is the SF stage excess noise factor and \( G_{m,SF} \) its transconductance.

Both Eq. 2 and Eq. 3 share a similar term having common parameters with the \( A_{CG} \). Indeed, the term \( C_{SN} + C_e W \) is common while the term \( C_e W + C_i WL \) is attenuated by \( (1 - 1/n) \) in the \( A_{CG} \) denominator. But in the end, reducing \( C_{SN} \) and increasing \( A_{CG} \) result both in an input referred noise reduction of the whole CIS readout chain especially if the \( C_{SN} + C_e W \) dominates the \( C_e W + C_i WL \) term. It is important to underline the fact that the last point is valid for SF based pixel schemes, whereas it’s not valid for common source based configurations where the CG is higher thanks to the AC gain of the CS but the noise is not necessarily lower.\(^{18,20,21} \)

3 CG enhancement techniques

As shown by Eq. 1, the CG can be enhanced by optimizing the \( C_{SN} \) term on one side, and by optimizing the SF size, slope factor and parasitic capacitance on the other side. In the following, three pixel variants are suggested. The first proposes a process refinement for reducing the \( C_{SN} \) term, the second combines this refinement with an SF optimization and the third variant proposes a different pixel scheme allowing further reduction of the \( C_{SN} \) without any process refinements.

3.1 Pixel variant 1

\( C_{SN} \) is the sum of the metal wiring parasitic capacitance connected to the SN, the junction capacitance of the SN and the overlapping of the SN with the transfer and reset gates. The last term dominates the \( C_{SN} \) due to the large transfer gate needed for an efficient transfer and the relatively high oxide density. For instance, in the 180 nm process used in this work, the overlap capacitance
Fig 3 SN doping profile improvement for reduced overlap capacitance with transfer and reset gates.

Fig 4 Schematic view of the first pixel variant featuring a refined SN doping in conventional 4T pixel scheme together with the corresponding timing diagram.
density is about 0.45 fF/µm. This value is even prone to be higher for advanced technology nodes. Hence, the first proposed optimization focuses on the reduction of the overlap capacitance between the SN and the transfer and reset gates. A technique similar to low doped drains (LDD) is used to mitigate the overlap capacitance. Instead of uniformly doping the SN, the latter is doped with a gradually increasing concentration as shown in Fig. 3. The SN area overlapping with the transfer gate is doped with a concentration $n_1$ one order of magnitude lower with respect to the SN area where the metal contact is placed, $n_2$. In this way, the overlap capacitance caused by the high oxide capacitance density is mitigated by the series capacitance corresponding to the interface between the $n_1$ and $n_2$ regions. In the same way the doping concentration $n_3$ underneath the reset gate overlap with the SN area corresponds to the concentration used for LDD area in standard NMOS transistors. Such a low doping concentration together with an additional interface between $n_2$ and $n_3$ helps reducing the the overlap capacitance with the reset gate.

Fig. 4 shows the schematic of the resulting pixel and the corresponding timing diagram. This opti-
Fig 6 schematic view and corresponding timing diagram of the second pixel variant featuring a 4T pixel scheme with a PMOS voltage follower having its source connected to its bulk for body effect mitigation. The implementation has no impact on the operation scheme of the pixel. On the other hand, the layout requires additional implants in order to implement the gradual doping. Fig. 5 shows the layout of the proposed pixel. The dashed square in the SN area marks the position of the additional implant used in the contact area. The pixel features a pitch of 12 µm and a fill factor of 76%.
Fig 7 layout view of the 4T pixel based on an PMOS SF and implementing the SN gradual doping.

3.2 Pixel variant 2

After reducing the $C_{SN}$ term, the contribution of the SF parasitic capacitance to the $A_{CG}$ denominator is no more negligible Eq. 1. Thus, the second $A_{CG}$ enhancement technique consists in optimizing the SF. The optimal SF sizing for a low input-referred 1/f and thermal noise is close to minimum sizing.\textsuperscript{23} Due to the foundry design rules constraints, the NMOS SF size cannot be further reduced. Hence, a way to go around this limitation is to use thin oxide transistors that are available in the same design kit. Thin oxide transistors are 1.8 V transistors featuring higher oxide density compared to the thick oxide ones used by default in pixel design. Even if these transistors feature higher oxide thickness, they allow to go for smaller gate width and length reducing consequently the parasitic capacitance. In order to use 1.8 V transistors in a 3.3 V design, the bulk voltage needs to be increased. PMOS transistors come with a private n-well with a bulk connection. By connecting the bulk to the source, the body effect is also mitigated which brings the slope
factor $n$ in Eq. 1 close to 1 leading to a higher CG that can be approximated by:

$$A_{CG} = \frac{1}{C_{SN} + C_eW}. \quad (4)$$

In this way using a thin oxide PMOS SF has both the advantage of featuring lower parasitic capacitance and body effect. The lower body effect increases the $A_{CG}$ by reducing $n$ and mitigating the gate-to-source total parasitic capacitance.

Fig. 6 shows the schematic and timing diagram of the pixel implementing a thin oxide PMOS SF. As for the previous suggested optimization, this pixel scheme does not have any impact on the timing diagram but rather requires and additional voltage reference connection shifting-up the SF drain to 1.5 V in order to accommodate the 1.8 V transistor to the 3.3 V environment. On the layout side, the introduction of a private n-well for the PMOS SF faces additional design rules constraints reducing the pixel fill factor. Indeed a minimum spacing needs to be respected between the PPD well and the PMOS n-well as shown in Fig. 7. On the other hand the SF gate width and length can be reduced to a value as low as 0.2 $\mu$m. In this pixel, a thinner metal wiring between the SN and the SF gate is also used in order to reduce the wiring parasitic capacitance with respect to the pixel variant previously introduced. With respect to the previous pixel variant, the fill factor is reduced to 61% due to the additional distance to keep between the PMOS SF n-well and the PPD n-well.

3.3 Pixel variant 3

The gradual doping technique introduced in the previous pixels requires process refinements involving at least two additional implants with respect to a standard pixel. This represents a complexity barrier for the designers in addition to the manufacturing cost increase. Indeed, such refinement
Fig 8 Schematic view of the third pixel variant and corresponding timing diagram. The pixel features an unconventional 5T scheme completely isolating the SN from transfer and reset gates overlaps.
Fig 9  Idealistic potential profile across the photoelectrons path starting from the PPD, going to the IN through the transfer gate TX1 and then to the SN through the second gate TX2. (a) corresponds to the SN charge dump. (b) depicts the IN node setting to an intermediate voltage between the pin voltage and the SN one. (c) represents the SN reset and (d) the charge transfer from the PPD to the SN.

Fig 10 layout view of the 4T pixel based on an PMOS SF and implementing the SN gradual doping.
cannot by easily simulated\textsuperscript{24} as it is case for standard devices for which circuit simulators are used. An alternative technique to reduce the SN parasitic capacitance is to completely isolate it from the area overlapping with the transfer and reset gates by introducing an additional gate implemented in a standard process without involving any process refinements or additional implants.

Fig. 8 shows a schematic view of the proposed 5T pixel and its corresponding timing diagram. Compared to a conventional 4T scheme, this pixel features an intermediate node (IN) that can be isolated from the SN by means of an additional gate allowing an important reduction of the SN capacitance. The reset phase consists in three steps. First, the RST switch is closed connecting IN to $V_{\text{RST}}$. While $V_{\text{RST}}$ is set to $V_{\text{DD}}$, the potential barrier between IN and SN is lowered by setting $TX_2$ to a voltage $V_{TX2H1}$ in order to dump the charge from the SN as depicted in Fig. 9(a). $TX_2$ is set back to 0 in order to split the IN and SN and freeze the SN voltage at its maximum level. $V_{\text{RST}}$ is then switched to a lower voltage $V_{\text{RSTL}}$ between the pin voltage of the PPD $V_{\text{pin}}$ and $V_{\text{SN,max}}$. After this step, the reset switch is opened again to freeze the IN voltage at a value $V_{\text{IN}}$ as depicted in Fig. 9(b). The last step of the reset phase consists in setting $TX_2$ to a voltage $V_{TX2H2}$ making the barrier between the IN and SN equal or slightly higher than $V_{\text{IN}}$ as shown in Fig. 9(c). In this way, any excess charge transferred to IN would diffuse towards the SN. After lowering back $TX_2$, the SN reset voltage $V_{\text{SN,rst}}$ is sensed. Transferring the charge integrated in the PPD to the SN takes place by pulsing both $TX_1$ and $TX_2$ as depicted in Fig. 9(d). $TX_1$ is pulsed to a value $V_{TX1H}$ in order to set the voltage under the TG between the PPD pin voltage $V_{\text{pin}}$ and the intermediate node voltage $V_{\text{IN}}$ while $TX_2$ is pulsed again to transfer this charge to the SN. The signal corresponds to the difference between the SN voltage after reset $V_{\text{SN,rst}}$ and the one sensed after the transfer $V_{\text{SN,transfer}}$. A deeper description of the operation of this pixel is provided in.\textsuperscript{9} Fig. 10 shows the layout of the proposed 5T pixel. With respect to the previous pixel, the additional transfer gate has
Fig 11 Fabricated QVGA imager used for the measurements implementing the three introduced pixel variants. The image on the left shows the floor plan of the imager. The right images show the chip wire-bonded to the test PCB.

no impact on the fill factor given the minimum spacing constraint related to the PMOS n-well.

4 Measurements

4.1 Physical implementation

The three pixel variants, presented previously, are embedded in three sub-arrays of an image sensor chip fabricated in a 180 nm CIS process with 4 metal layers. The sensor chip measures 5 mm by 5 mm. Fig. 11 shows the floor plan of the imager embedding a QVGA array made of 3 sub arrays exploiting the pixels presented in the previous sections with a pitch of 12 µm. The imager also embeds row control circuits, column-level amplification and single slope 12 bits ADCs.

The imager chip is directly wire-bonded to the test printed circuit board (PCB) on which an optical objective is directly mounted on a fixed barrel as shown in Fig. 11. In order to perform pixel characterization, the optical objective is replaced by a light source mounted on a diffuser to make sure all pixels are similarly exposed.
4.2 Measurement technique: photon transfer curve

In order to measure the conversion gain, the photon transfer curve (PTC) method\textsuperscript{25} is used. This method exploits the proportionality between the shot noise variance and the average signal. For an average number of $N$ integrated photons, the variance of the corresponding shot noise is $N$. The mean value of the signal at the output of the the pixel is given by

\[
E[V_{\text{out}}] = A_{\text{CG}} \cdot N. \tag{5}
\]

On the other hand, the variance of the output voltage when the photon shot noise dominates is given by

\[
\text{Var}[V_{\text{out}}] = A_{\text{CG}}^2 \cdot N. \tag{6}
\]

Thus, the readout chain conversion gain can be obtained without knowing the exact value of $N$ combining Eq. 5 and Eq. 6

\[
A_{\text{CG}} = \frac{\text{Var}[V_{\text{out}}]}{E[V_{\text{out}}]}. \tag{7}
\]

Therefore, the pixel output variance plot as a function of the mean must feature a linear trend if the readout chain is shot noise limited. In that case, the slope of the linear trend corresponds to the conversion gain.

This technique is used to prove the shot noise limited performance obtained with all the pixels presented in this work and at the same time gives the evaluation of each pixel conversion gain. In order to obtain the PTC curve, each pixel is illuminated using a voltage controlled light emitting diode (LED) to obtain different points. For each LED voltage value, a 100 readouts are operated in order to compute the corresponding variance and mean values.
4.3 Measurement results

Fig. 12 shows the PTC curve obtained from the 4T pixel implementing a NMOS SF and optimized SN doping. The PTC curve shows good linearity which demonstrates a low readout noise dominated by the shot noise even at low light conditions. The measured $A_{CG}$ corresponds to $121 \, \mu V/e^-$. A conventional 4T pixel based on the same SF but featuring a standard SN junction features a conversion gain of about $80 \, \mu V/e^-$.\textsuperscript{10,17}

Going back to the $A_{CG}$ formula introduced in Eq. 1, the slope factor of the NMOS SF is about 1.2 based on the simulation results. The SF gate intrinsic capacitance can be approximated by $2/3C_{ox}WL$, hence, for a $C_{ox}$ of $4.5 \, \text{fF}/\mu \text{m}^2$ a width of $0.42 \mu \text{m}$ and a length of $0.84 \mu \text{m}$ the source follower gate capacitance contribution to $A_{CG}$ denominator is $0.2 \, \text{fF}$. The extrinsic capacitance contribution dominated by the overlap between the source and drain of the SF is also estimated from the simulation to be as high as $0.2 \, \text{fF}$. The measured total denominator capacitance corresponding
to the $121 \mu V/e^-$ conversion gain corresponds to 1.1 fF. Hence the $C_{SN}$ term corresponds to 0.7 fF. This same term is as high as 1.2 fF in the standard pixel which means that the gradual doping technique used at the level of the SN reduces $C_{SN}$ by a factor 1.7.

Fig. 13 shows the PTC curve obtained from the 4T pixel implementing the same SN structure as the previous pixel and replacing the NMOS SF by an thin oxide PMOS SF with a source-to-bulk connection. Connecting the source to bulk makes the slope factor approximately equal to 1 which increases the conversion gain. The PTC curve shows good linearity which demonstrates a low readout noise dominated by the shot noise even at low light conditions. The measured conversion gain corresponds to $191 \mu V/e^-$. In this case, the contribution of the SF to the conversion gain denominator is reduced to 0.2 fF given that the $(1-1/n)$ term is close to 0, $C_i$ equal to 0.8 fF and the width of the SF is equal to 0.22 $\mu$m. Hence the $C_{SN}$ term is estimated to 0.6 fF, which is quite close to the 0.7 fF obtained from the previous pixel. In fact, both pixels share the same SN structure with a slight difference on the metal line connecting the SN to the SF as shown in the layouts of both.
For the 5T pixel, Fig. 14 shows the measured PTC for the low gain mode. In this configuration, the IN and SN are completely merged. The PTC curve show a linear response which demonstrates a low readout noise dominated by the shot noise even at low light conditions. The linear region of the curve points at measured conversion gain of 115 µV/e−. This PTC collapses around 0.65 V which corresponds to a FWC of about 5600 electrons. Note that this FWC can be increased by increasing the IN capacitance.

Fig. 15 shows the measured PTC for the high gain mode following the timing diagram of Fig. 8 and setting \( V_{\text{RSTL}} \) to 1.76 V, \( V_{\text{TX1H}} \) to 1.2 V, \( V_{\text{TX2H1}} \) to 2.2 V and \( V_{\text{TX2H2}} \) to 1.5 V. In this configuration, the SN is completely isolated from the transfer and reset gates overlaps thanks to the second TG. As shown in Fig. 16, the IN and SN can be modeled by capacitors connected to the source and
**Fig 15** PTC curves measured from the 5T pixel in high conversion gain mode, completely isolating the SN from transfer and reset gates overlap.

**Fig 16** Simplified model of the IN, SN and intermediate TG depicting the corresponding potential levels during charge transfer.
drain of the second TG. Before the charge transfer, as explained previously, the voltage difference between the IN and SN is chosen to set to the second TG in saturation regime. As shown by Fig. 15, the high CG curve follows a linear trend corresponding to a slope of 250 $\mu$V/e$^-$. The PTC deviates from its linear trend for higher charge transfers suggesting that other noise mechanisms dominate when relatively large amount of charge is transferred to the IN. This phenomena can be explained as follows: as long as long as the charge transferred to the SN does not reduce the SN voltage enough to become close to the IN voltage, the second TG operates in saturation regime. In this case, the second TG enters in a sub-threshold reducing the kTC noise to a negligible level and giving only rise to the shot noise. In contrast, when a larger amount of charge is transferred, the IN and SN are merged and the second TG operates in an triode regime. This situation gives also rise to spill back noise when closing the second TG. The high gain mode is expected to be used only for low light conditions in which the PTC remains linear.

In the case of high gain mode, a conversion gain of 250 $\mu$V/e$^-$ with the same SF as the previous pixel corresponds to a SN capacitance $C_{SN}$ of 0.44 fF.

4.4 Summary and discussion

The enhancement of the conversion gain relies both on the SN capacitance reduction and the SF optimization. Tab. 1 summarizes the techniques deployed to increase the conversion gain and their impact. The measurement show a dramatic gradual increase by a factor of more than 3 going from the standard pixel to the 5T pixel scheme.

On the other hand, in a carefully designed CIS readout chain, the $1/f$ and thermal noise originating from the SF are the dominating noise sources. The parameter that is more important for reducing the noise originating from the SF stage is the sense node parasitic capacitance inde-
Fig 17 Summary of the measured conversion gains $A_{CG}$ (right axis) and extracted sense node capacitance $C_{SN}$ (left axis) for the three pixel variants implemented in this work compared with a reference standard 4T pixel from the same foundry.

...ependent from the SF contribution $C_{SN}$. Indeed, based on Eq. 2 and Eq. 3, if the SF is minimally sized, the $C_{SN}$ term dominates the SF parasitic capacitance contribution and its reduction directly mitigates the SF stage noise contribution. Tab. 2 summarizes the different techniques implemented to reduce the sense node capacitance and their impact on $C_{SN}$. The $C_{SN}$ values extracted from the measurement show a progressive decrease of the SN parasitic capacitance.

Fig. 17 summarizes the measurement and extraction results. The measured CG increase with respect to a reference standard 4T pixel comes with a reduction of the $C_{SN}$. 
### Table 1 Conversion gain evolution with the combination of enhancement techniques

| Implemented technique                                                                 | $A_{CG}$ [µV/e⁻] |
|--------------------------------------------------------------------------------------|------------------|
| standard 4T pixel fabricated with the 180 nm CIS process used in this work            | 80               |
| gradual sense node doping and standard NMOS SF                                       | 120              |
| gradual sense node doping combined with PMOS SF with source connected to the bulk for body effect mitigation | 191              |
| 5T pixel scheme with isolated SN and PMOS SF with mitigated body effect               | 250              |

### Table 2 Sense node capacitance evolution with different reduction techniques.

| Implemented technique                                                                 | $C_{SN}$ [fF] |
|--------------------------------------------------------------------------------------|---------------|
| standard 4T pixel fabricated with the 180 nm CIS process used in this work            | 1.2           |
| gradual sense node doping reducing the junction and overlap capacitance with the transfer and reset gates | 0.6 to 0.7    |
| isolation of the SN from the reset and transfer gates by means of an additional transfer gate in 5T pixel scheme | 0.44          |

### 5 Conclusion

The pixel conversion gain is a key performance metric in low noise CIS readout chains. It is both affected by the SN total parasitic capacitance and the in-pixel SF design.

When metal wiring parasitic capacitance is low enough thanks to an optimal layout, the SN parasitic capacitance can efficiently be reduced by mitigating the impact of the overlapping capacitance with the transfer and reset gates connected to the SN. This is successfully achieved by implementing an optimized doping profile in the SN area. The latter consists of using light doping in general combined with gradual doping concentrations having an effect similar to LLD for MOS transistors. Such a technique brings the SN parasitic capacitance from 1.2 fF in a standard pixel to 0.6 fF. This technique requires process refinements coming with complex research and development effort since they are not straightforward to simulate. An alternative to this technique is presented. It
involves the complete isolation of the SN from the transfer and reset gates by means of an additional gate. This technique uses the standard process and successfully brings the SN capacitance to 0.44 fF at the cost of a higher lag.

On the SF design side, the mitigation of the body effect successfully increases the overall CG. Indeed, the CG goes from 120 µV/e- to 191 µV/e- when replacing the standard NMOS SF by a source to bulk connected PMOS in the pixel embedding the gradual SN doping technique. Finally, combining both SN isolation from the TG with an optimized SF leads to a CG of 250 µV/e− which is 3 times higher than a standard 4T pixel from the same process.

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