TrustToken, a Trusted SoC solution for Non-Trusted Intellectual Property (IP)s

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ABSTRACT
Secure and trustworthy execution in heterogeneous SoCs is a major priority in the modern computing system. Security of SoCs mainly addresses two broad layers of trust issues: 1. Protection against hardware security threats (Side-channel, IP Privacy, Cloning, Fault Injection, and Denial of Service); and 2. Protection against malicious software attacks running on SoC processors. To resist malicious software-level attackers from gaining unauthorized access and compromising security, we propose a root of trust-based trusted execution mechanism (named as TrustToken). TrustToken builds a security block to provide a root of trust-based IP security: secure key generation and truly random source. TrustToken only allows trusted communication between the non-trusted third-party IP and the rest of the SoC world by providing essential security features, i.e., secure, isolated execution, and trusted user interaction. The proposed design achieves this by interconnecting the third-party IP interface to TrustToken Controller and checking IP authorization(Tokken) signals ‘correctness’ at run-time. TrustToken architecture shows a very low overhead resource utilization LUT (618, 1.16 %), FF (44, 0.04 %), and BUFG (2, 6.25%) in implementation. The experiment results show that TrustToken can provide a secure, low-cost, and trusted solution for non-trusted SoC IPs.

1 INTRODUCTION
Often non-trusted third-party IP cores or EDA tools are integrated into different stages of SoC development life and are susceptible to numerous attacks, such as HT injection, IP piracy, cloning, tampering and unauthorized access [1]. To prevent malicious attackers from gaining unauthorized access and leaking sensitive information, modern SoCs are equipped with sandboxing mechanism where applications and OS are executed in a isolated trusted environment [2]. ARM TrustZone is the industry leading sandboxing mechanism which is widely available in mobile and heterogenous SoC devices for providing trusted execution environment (TEE) where untrusted IP core is executed in a isolated secure processor along with separated Memory, Cache and Bus system. Leveraging ARM TrustZone technology, TEE is extended for security measures in many academic projects and industrial applications such as Samsung Knox [3], Android’s Keystore [4], OP-TEE [5], Xilinx TrustZone [6] etc. A SoC CPU which includes any Trusted Execution Environment (TEE) technology e.g. ARM TrustZone, Knox, Xilinx TrustZone etc. don’t provide any root of trust based secure mechanism, where any running software is verified and trustworthy. Instead of root of trust based authorization existing TEE technologies focuses on only isolating the environment by partitioning the CPU, memory and system bus. Some of the current TrustZone based technologies assumes the availability of a secure storage devices for storing secret keys which can only be accessed by the secure world entity and serve as the root of the trust. On many modern SoC and mobile devices unfortunately that secured storage devices is not available. For establishing root of trust based trusted environment, the device key should be stored securely and available after a reboot. In many reconfigurable SoCs e.g. Xilinx Zynq - 7000 SoC [2], UltraScale+ FreeScale etc., the secure key is stored either in battery backed RAM (BBRAM) or eFuse medium. However, there are some bottlenecks in this method and not recommended for following disadvantages: 1) These mechanism still need to provide secure random key generation by random number generator(RNG) which will serve as a root of trust. 2) eFuse is a non-changeable memory where the key cannot be updated. 3) BBRAM methods needs a physical battery to be placed for storage.

In this paper, we propose a novel and efficient trusted technology TrustToken to overcome above disadvantages. We used an asymmetric cryptographic solution that can generate identification tokens in runtime conditions without using any non-volatile memory or any secure boot system. We are inspired and motivated by Google Chromium sand-boxing [7] concept to establish a secure execution environment in a SoC background by assigning Tokens for each IP core. TrustToken is a security mechanism that allows to execute a non trusted third party IP in a closed and monitored environment. If a malicious attacker is able to exploit the access control of the IP in a way that lets him run arbitrary alter on the IP design, the TrustToken would help prevent this incident from causing damage to the system. This is achieved by wrapping a non-trusted IP with a security wrapper shown in Fig. 1. This security wrapper is connected with TrustToken Controller that performs the security evaluation of each connected non-trusted IP core. TrustToken controller compares this token to deny or grant access to the rest of the SoC system. This token access signal acts like a security ID card for the untrusted IP core and must provide in each data transaction access request.
3 BACKGROUND

3.1 Physical Unclonable Function

Physical Unclonable Function exploits the manufacturing variation of a silicon nanocircuit to generate unique and ubiquitous keys [15]. PUF can be used for cryptographic operations such as authentication, random number generation, authorization, etc. The idea behind the PUF is that one (or more) device that is identical by design will have different electrical characteristics due to manufacturing variation.

To evaluate PUF generated keys performance, the three most common metrics are used. They are Randomness, Bit Error Rate, and Uniqueness. A strong PUF design has many challenge-response pairs (CRPs) generated from a single device, and normally weak PUFs support a relatively small number of CRPs. Compared to other crypto measures such as AES, SHA, MD5, or HASH functions, PUFs exploit limited hardware resources (LUTs, GATES).

3.2 ARM TRUSTZONE

ARM TrustZone technology refers to a secure execution environment (SEE) [2] where an environment is provided to isolate both trusted and non trusted software and hardware. It is also referred to as Trusted Execution Environment (TEE), and it has a monitor that controls the interactions between these two separate worlds. TEE uses two physically separate processors dedicated to the trusted and non-trusted world in an embedded security system. The major drawback of this architecture is they share the same peripherals such as Ethernet, DRAM, UART, etc. ARM TrustZone is a combination of some IP blocks which allows a partition between sets of I/O Peripherals, Processors, and Memory into two different worlds. In ARM TrustZone platform, two NS bit registers is dedicated to implement the isolation of a software process [2].

3.3 Hardware Trojan and Design For Trust

A hardware Trojan (HT) is stated as a malicious attacker who has intentionally modified a system circuit and cause alteration from expected behavior while the circuit is implemented [16]. HT poses a severe threat to SoC design as it can leak sensitive information or change the specification of a circuit in run time conditions. HT can create an emergency situation by degrading the overall system functionality of the circuit. Often this HT is deployed in stealth mode and activated in rare conditions, making it very difficult to patrol its harmful effects in the verification stage. Many researchers have come forward to classifying hardware Trojans and their structure based on their characteristics. One of the best classifications is according to the activation (referred to as Trojan Trigger), and payload mechanism ground [1].

4 THREAT MODEL AND SYSTEM PROPERTIES

Before digging into the proposed architecture, we considered some threat models. Our threat model can be divided into two different explicit scenarios: Hardware Trojan and Illegal software access. In considering the probable first threat model, we consider every IP as non-trusted and capable of inserting hidden malicious Trojan components inside the IP component. They can act in rare conditions. We assume that they are only activated in run-time environment.
In this article, we did not consider the physical attacks performed by physical equipment, which are out of the scope of this article. The attack scenarios did not cover attacks related to hardware components like side-channel attacks, probing attacks, snooping, timing attacks, denial-of-service, fault injection, etc. In summary, describing our architecture, we have taken these threat models into account:

1. Any malicious HT hiding inside of an IP core, trying to execute in runtime environments. We assume that, hidden HT can bypass the existing CAD tools and can be undetected until payload condition is triggered.
2. Any malicious HT trying to perform illegal access control or unauthorized data transfer. We consider that the attackers can overwrite the data of a specific data channel and intentionally change the computational output. We also assume that, the malicious attacker could cause potential data leakage by changing the operating mode of the IP core.
3. Any malicious attacker located in the CPU core, trying to gain unauthorized access or leak sensitive information of other applications.

5 PROPOSED ARCHITECHTURE

The goal of TrustToken is to provide a root of trust-based runtime isolation enabled mechanism, which allows an SoC owner to provide secure and flexible communication of IP cores without any additional secure storage services or system. Figure 3 illustrates the detailed architecture of our proposed design, which includes the following components: the TrustToken Controller, TrustWrappers and TokenGenerator.

TrustToken Controller: The TrustToken controller is a separate centralized IP dedicated to generating unique Tokens/IDs for the IPs and maintaining the security policies in the connected world. Any IP Integrator has to change the token’s parameter value named ar_integrity to assert the validity check (Fig 4). When this value is assigned as a LOW state, it will disable the isolation feature. When HIGH, it will impose the isolation mechanism of the IP and execute the IP in a non-trusted zone after successful authorization. After generating the keys by PUF module, they are delivered to Central TrustToken Controller for assigning token IDs. Central TrustToken Controller works as the central security headquarters of the whole SoC system and is responsible for distributing all Token IDs provided by the integrated PUF module. This token ID is referred to as ar_token, and the length of this signal is 256 bits. Central TrustToken Controller also assigns specific ID for each of the non-trusted IP which is denoted as ar_id. TrustToken controller randomly distributes the keys among the IP connected to this controller and stores the allocated Token IDs for respective IPs along with Tokens for future verification. Whenever any IP requests a READ/WRITE access to the TrustToken controller, it compares the received Token ID with the securely stored Tokens list. After successful authorization, it will either enable the data channel for communication or restrict it immediately.

Trust Wrapper: In our proposed architecture, every IP will be wrapped in a security wrapper labeled as TrustWrapper. TrustWrapper has two different operating interfaces: Secured and Non-secured. Every non-trusted IP core tagged as non-secured will be assigned two additional bus signals to the IP core: ID and Token. Instead of adding any register level isolation mechanism or any separate bus protocol for the secure isolation, we rely on adding extra bus signals to the existing AMBA bus protocol specifications. Adding a separate bus protocol for isolation could create new vulnerabilities and force of modifying the interconnect bridge logic for security check operations. Further, creating a uniform and unique bus protocol to carry IPs ID and Token information would need a different security mechanism and support every possible bus protocol specifications e.g. bandwidth, channel length, burst size, streaming methods, etc. Each data transaction initiated by the non-trusted IP core will create an authorization request by the Central TrustToken Controller. non-trusted IP should provide valid and unexpired security information (IDs and Token) to the controller block through the security wrapper.

Token Generator: Due to low overhead and latency, Enhanced Ring Oscillator-based PUF proposed in paper [15] is implemented, which is more stable than traditional Ring Oscillator PUF. Ring Oscillator-based PUF shows promising latency and resource utilization results compared
Enable within a realistic time. In terms of the Strong PUF definition, the TokenGenerator software processes offload their to hardware IP cores. The security components are integrated in the security primitives because the are implemented in the system. Both hardware and software level defines the security elements and access control primitives that are comprised to HIGH logic states, which forces the TRUST ZONE controller peripheral or AXI Interconnection in Zynq Based SoC platform.

Secure Transition between Integrity Level. Benhani et al. [17] showed that any simple malicious TCL script in CAD Tool could comprise the logic state of AWPROT or ARPROM signal in the AXI peripheral or AXI Interconnection in Zynq Based SoC platform. Any malicious TCL script can modify this AWPROT to ARPROM signal to HIGH logic states, which forces the TRUST ZONE controller to execute in a non-secure world even though the IP is insecure, leading to a denial of service attacks. To encounter this problem, we to execute in a non-secure world even though the IP is insecure, to SRAM PUF, Arbiter PUF, TRNG, or other crypto cores. Our custom Ring Oscillator-based PUF solution can generate 256-bit width keys. It has an accepted uniqueness and randomness to fit our goal of providing heterogeneous SoC security. In one of the fundamental research work regarding PUF [15] strong PUF is defined as the following security properties: 1. It will be impossible to clone the PUF circuit physically. 2. It will support many Challenge-Response Pairs (CRPs) so that the adversary cannot mount a brute force attack within a realistic time. In terms of the Strong PUF definition, the proposed work can be considered a strong PUF and will be the best candidate to be implemented for the proposed SoC security reason.

6 SECURITY RULES

In this section, we describe the formal specifications of the security rules for the TrustToken framework. The security formalism defines the security elements and access control primitives that are implemented in the system. Both hardware and software level components are integrated in the security primitives because the software processes offload their to hardware IP cores. The security tuple \( S \) is characterized as follows:

\[
S := \{ U, P, O, T, I, A, D, M \}
\]

- \( U = \{ u_1, u_2, u_3, ..., u_n \} \) is the set of users in a system.
- \( P = \{ P_1, P_2, P_3, ..., P_n \} \) is the set of process sets where each user has its corresponding process set \( P_i = \{ P_{i1}, P_{i2}, P_{i3}, ..., P_{in} \} \).
- \( O = \{ o_1, o_2, o_3, ..., o_n \} \) is the set of objects. In our proposed framework, objects correspond to various types of non-trusted IP cores.
- \( T = \{ T_1, T_2, T_3, ..., T_n \} \) is the set of secret Tokens.
- \( I = \{ I_1, I_2, I_3, ..., I_n \} \) is the set of assigned IDs to each non-trusted IP core.
- \( A = \{ HIGH, LOW \} \) is the set of integrity access attributes. Here, HIGH is the HIGH state level of integrity, LOW is LOW state level of integrity.
- \( D = \{ yes, no \} \) is the set of decisions.
- \( M = \{ M_1, M_2, M_3, ..., M_n \} \) is the set of access matrix. Each user has its corresponding access matrix. Each matrix has \( m \times k \) elements where each element is a 3-bit access attribute, \( a = a_2a_1a_0 \) where \( a_2 \rightarrow r, a_1 \rightarrow w, a_0 \rightarrow e \).

As most of the modern OS system allows us to create multiple user accounts in a single CPU, we include the set of users in the security tuple. Each user can execute multiple processes and we have included one process under each user. The integrity access attributes include HIGH and LOW states. To ensure the security of the system, we have defined and established some security rules:

**Rule 1.** For each \( u \in U \), there is a function \( F_u : P \rightarrow M \) which must be a one to one function. Rule 1 ensures secure isolation of hardware access requests as a process under one user can not gain any unauthorized access of other user.

**Rule 2.** An access request is a 4-tuple \( \tau = (u, p, o, t, i, a) \) where \( u \in U, p \in P_i, o \in O, t_i \in T, i \in I \) and \( a \in A \).

Rule 2 defines the access request where a process under a user account requests for a data transaction from a hardware IP core.

**Rule 3.** Confidentiality Preserving Rule: If a process \( p \in P \) has an integrity attribute, \( i \) over an object \( o \in O \) and the decision is \( d \in D \), the confidentiality is preserved if \( a_2 = r \) or \( a_0 = e \) or both.

**Rule 4.** Integrity Preserving Rule: If a process \( p \in P \) has an access attribute \( a \) over an object \( o \in O \) and the decision is \( d \in D \), the integrity is preserved if \( a_1 = w \) or \( a_0 = e \) or both.

**Rule 5.** The access request of a process \( p \in P \) over an object \( o \in O \) is granted if the decision is \( d \in D \) and \( d = yes \).

**Rule 6.** Only the Central Trust Controller or an IP integrator in design phase has the access to modify the access matrix \( M_i \in M \).
7 PROTOCOL EVALUATION AND CASE STUDIES

In this section, we tried to cover the protocol resiliency in described attack scenarios.

7.1 Scenario 1: Compromising ID signals

The Token-based authorization aimed to protect against malicious CAD or RTL modification attacks. As stated above, to achieve hardware modification and gain access control in a non-trusted IP, it was enough to modify only some commands in the script. In our proposed design, the PUF-based Token ID is provided only in runtime conditions and exploits the device’s manufacturing variation. Also, as the Token ID is not saved in any memory, we assume that this will protect against any malicious attack of altering the Token ID. In section 4 we have discussed a possible attack scenario where a software level attack was introduced from an arbitrary application core. The malicious adversaries configure a secured IP core and attempt to gain access to the victim IP by initiating a transaction request from a different IP core. However, Central Trust Controller keeps a record of all assigned IDs and Tokens and their respective source and destination IPs. Since the attacker has made an illegal access request from an outside IP core, this attempt will be compared with the saved credentials and prevented if mismatched.

7.2 Scenario 2: Compromising access control

In the case of Xilinx TrustZone, [6], at the AXI interconnect level security check is performed, and it plays a critical role in the security. This Interconnect crossbar is also responsible for checking the security status of every transaction on the connected AXI bus, which creates a huge security risk. Any malicious attacker intending to break the security layer can easily control the AXI interconnect crossbar by modifying some security signals. This defect was overcome with the proposed secure design, as the proposed Trust Token Controller has enforced a robust and secure system that makes any access control attack very difficult to take control of the internal signals of Central Trust Token Controller. Central Trust Token Controller is itself encrypted with PUF-based Token ID key and hence restricts any unauthorized access control on this IP.

7.3 Scenario 3: Comprising INTEGRITY LEVEL

Any non-trusted IP connected to the Central Trust Token Controller for secure isolation is determined by the status of INTEGRITY LEVEL signals. As stated before in the thread model section, only an IP Integrator can define the INTEGRITY STATUS in hardware level. Any modification of this signal in runtime conditions will need proper authorization, which gives protection against any hidden CAD or RTL script attack. Also, to alter the status of the protection level, any malicious attacker has to show their PUF-based Token ID of the non-trusted IP. In the work, [17] benhani et al. showed that only by modifying the Arm TrustZone AWPROT/ARPROM signal any malicious attacker could create a significant Denial of Service (DoS) interruption in the SoC. This scenario can be overcome by the proposed secure transition model, where an alteration request should also go into an additional authorization layer.

8 PERFORMANCE EVALUATION AND IMPLEMENTATION SUMMARY

This section describes the experimental setup and overhead calculations used for implementing our proposed architecture to evaluate the robustness of the proposed Trust Token framework. The main setup was to efficiently implement the architecture and calculate overhead and latency for data transactions.

8.1 Evaluation Infrastructure

To implement the protocol framework, we have used the Zybo Z7-20 (Xilinx XC7Z020) FPGA board throughout the whole article. This board has two ARM Cortex-A9 processors, clocked at 667 MHz with 1-GB Memory and Zynq - 7000 FPGA processor. Overhead analysis and performance reports were generated and acquired from Xilinx’s Vivado Design Suite platform. All experiments reported in this article were performed on Xilinx XC7Z020 FPGA PL fabric.

8.2 Protocol Performance

We evaluated our proposed TrustToken protocol by implementing and synthesizing on Zybo-Z7-20 board. For evaluation, we have attached TrustWrappers around four symmetric crypto IP cores (AES,DES,TRNG and RSA). Every TrustWrappers was assigned in HIGH integrity state to evaluate the proposed architecture model. We also initiated 5 different applications on ARM processor to access the crypto cores computational results. In our implementation, we successfully introduced trusted execution environment by TrustToken model and observed the results. In section 4, we considered a possible software level attack scenario, where a malicious attacker from Application 3 (mapped to TRNG hardware IP core) is trying to establish an authorized access path to RSA IP core. We implemented this scenario, and the attacked was prevented by TrustToken module. To compare the protocol performance, we also designed VIVADO CAD tool based Xilinx TrustZone enclave around the four crypto cores by following the work [18] and compared with proposed TrustToken protocol. For Xilinx TrustZone, we successfully launch a simple CAD Tool attack by modifying the AWPROT signal in runtime condition scenario. Similarly, the attack attempt was failed in the proposed method, which explicitly prove the protocol resiliency against CAD tools attack.

8.3 Token Keys Performance Evaluation

Fig 5 shows the hamming distance results calculated from the PUF keys. We can observe from the figure that the hamming distance is closely rounded between 40 and 60 percent, which proves the stability and effectiveness of the keys and is very close to the ideal characteristics of PUF [15]. In Table 1 the overall characterizations of the PUF were summarized. Our internal PUF design includes 512 oscillators and can generates keys of 256 bits wide.

8.4 Resource Overhead

After successful implementation, we have included the utilization report from the VIVADO software platform in Table 2. The deployed design shows encouraging results with low resource utilization. BUFG region utilization is only rounded to 6.25 percent.
We have shown that the proposed protocol uses a constrained LUT and BUFG region of an SoC architecture and effectively provides an extra layer of security against unauthorized access control and attacks. The protocol uses a custom Ring Oscillator-based PUF module to generate keys, and it can exploit the reconfigurable nature of the SoC-based FPGA platform. Our implementation shows low latency and overhead in generating and distributing the PUF keys. We have shown that the proposed protocol uses a constrained LUT and BUFG region of an SoC architecture and effectively provides state-of-the-art illegal software access and data leakage prevention without much resource utilization. This protocol can also be promising for FPGA-based Hardware Accelerators fields etc., Cloud Computing, Machine Learning, and Image Processing.

9 CONCLUSION

This paper proposes a Token-based secure SoC architecture for non-trusted IP in a heterogeneous SoC platform. TrustToken architecture uses a root of trust-based authorization and provides an extra layer of security against unauthorized access control and attacks. The protocol uses a custom Ring Oscillator-based PUF module to generate keys, and it can exploit the reconfigurable nature of the SoC-based FPGA platform. Our implementation shows low latency and overhead in generating and distributing the PUF keys. We have shown that the proposed protocol uses a constrained LUT and BUFG region of an SoC architecture and effectively provides state-of-the-art illegal software access and data leakage prevention without much resource utilization. This protocol can also be promising for FPGA-based Hardware Accelerators fields etc., Cloud Computing, Machine Learning, and Image Processing.

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