Abstract—This paper presents a fully integrated second-order level-crossing sampling data converter for real-time data compression and feature extraction. Compared with level-sampling ADCs which sample at fixed voltage levels, the proposed circuits updates tracking thresholds using linear extrapolation, which forms a second-order level-crossing sampling ADC that has sloped sampling levels. The computing is done digitally and is implemented by modifying the digital control logic of a conventional SAR ADC. The system selects only the turning points in the input waveform for quantization. The output of the proposed data converter consists of both the digital value of the selected sampling points and the timestamp between the selected sampling points. The main advantages are data savings and power savings for the data converter and the following digital signal processing or communication circuits, which are ideal for low-power sensors. The test chip was fabricated using a 180nm CMOS process. The proposed ADC saves 30% compared to a conventional SAR ADC and achieves a compression factor of 6.17 for tracking ECG signals.

Index Terms—Analog-to-digital converter (ADC), Level-crossing Sampling, Nonuniform Sampling, Sparse Signal, Sensors

I. INTRODUCTION

ONE of the primary challenges in low-power sensors is that the ADC generates a large number of unessential data that overload the following digital processing, storage, or communication circuits. As shown in Fig. 1 (a), a Nyquist sampling ADC records digital data at every sampling clock for quantization, which may not be necessary if the input signal is sparse in the time domain. To reduce the amount of data output, level-crossing sampling ADCs [1] are proposed, as shown in Fig. 1 (b). When the input signal is crossing predefined voltage levels, the ADC records one-bit sign data and the timing information of such an event. However, level-crossing Sampling ADC is not good at identifying the location of turning points in the waveform since usually the gaps between the sampling levels are much larger than the resolution in a Nyquist sampling ADC. Moreover, level-crossing ADCs may also generate unnecessary samplings when the input signal has a low-frequency high-amplitude baseline wandering or high-frequency low-amplitude noise around the sampling level.

To address these problems, we propose a second-order level-crossing sampling ADC, which selects turning points of the analog input signal for quantization, while skipping sampling points that are in a linear portion in either time or amplitude domain. As shown in Fig. 1 (C), the proposed ADC computes the digital prediction of a sampling point based on prior quantized or predicted sampling points to decide if quantization is needed for the current sampling point. The decision is made using upper and lower thresholds calculated digitally by the predicted value and a prior defined Delta threshold value. Both amplitude data of the selected sampling points and the timestamp data between selected sampling points are the output data of the system. By doing so, the ADC greatly reduces the output data amount for sensing sparse signals. This letter is organized as follows. Section II presents the second-order level-crossing sampling ADC architecture and circuit implementation. Measured results are presented in Section III. Section IV discusses and compares the performance with related works. Section V concludes the paper.

II. SECOND-ORDER LEVEL-CROSSING SAMPLING ADC

The proposed second-order level-crossing sampling architecture includes the analog comparator, the N-bit DAC, the digital control logic for calculating predictions and thresholds, and the timer for recording timestamps between quantized sampling points. Fig. 2 presents the difference between the conventional successive-approximation-register (SAR) ADC and the proposed second-order level-crossing sampling ADC. The primary difference is in the digital control logic, where the second-order level-crossing sampling system has an extra digital input of Delta and an additional output as the timestamp. The control logic of the proposed ADC predicts the

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digital value of the analog input using two prior digital values using linear extrapolation, as shown in Fig. 3. Then the control logic calculates the digital values of an upper threshold by adding the Delta value to the predicted digital value. The upper threshold digital value is converted into analog value using the DAC, and then compared with the analog input. Similarly, a lower threshold is generated by subtracting Delta from the predicted digital value, which is also converted into analog value and compared with the analog input.

If the analog input is within the window between the upper threshold and the lower threshold, the prediction is successful and no further quantization is performed by the ADC. The system uses the predicted value as the digital results of the current sampling. The successfully predicted digital value is stored for the next prediction. If the analog input is out of the threshold window, the prediction fails. In such a case, a full quantization must be made for the current sampling and the next sampling to restart the prediction process. The quantization result of the first sampling becomes the digital timestamp output while the duration between unsuccessful predictions becomes the digital timestamp output.

For each sampling point, the control logic of an N-bit conventional SAR ADC needs to use the DAC N times. The comparator also needs to perform N comparisons. In contrast, the second-order level-crossing sampling ADC only uses the DAC and comparator 2 times for the upper and lower thresholds comparisons if both the two comparisons are both successful. In such a case, no further Digital-to-Analog conversions and comparisons are necessary. Nevertheless, if the prediction is not successful, the prediction and the 2 comparisons are wasted. Therefore, the proposed ADC saves power and data only when the input signal has a higher portion of the linear region, which is generally true for most of sparse signals.

III. CHIP DESIGN AND MEASUREMENT RESULTS

The proposed second-order level-crossing sampling ADC is designed by modifying a conventional fully-differential 10-bit switched-capacitor SAR ADC similar to [2]. The circuit consists of a comparator, a fully-differential digital-to-analog converter, and a digital control logic. The schematic of the digital-to-analog converter is shown in Fig. 4 (a) and the dynamic comparator is shown in Fig. 4 (b). In the data conversion process, the DAC first converts the upper threshold digital values into an analog voltage. The sampled input voltage is then compared with the high-threshold voltage using the comparator. Then the second data conversion and comparison are performed for the low-threshold voltage. If the input voltage is out of the window formed by the thresholds, the conventional SAR quantization process is enabled for the current sampling and the next sampling. The SAR quantization process needs 10 comparisons to determine the 10-bit digital values in a reserved quantization timing window. Otherwise,
if the input voltage is in the threshold window, the whole circuit is set in sleep mode. This is done by the control logic that turns off the comparator using the enable signal $V_{\text{comp}}$, which greatly saves the comparator power.

The prototype chip was fabricated using a 180 nm CMOS process. The chip microphotograph is shown in Fig. 5. The whole chip is 1.5 mm x 1.5 mm including the test structure and the pad frame. The Core area of the ADC is 390 mm x 440mm. The power supply is 1.8 V. Fig. 6 presents the measured result of a 1-Hz 900 mVpp ECG signal from a signal generator with different Delta values. In chip testing, if the prediction is successful, the chip sends the predicted value as the data output, which usually forms linear slopes. If the prediction fails, the chip performs full quantization as a regular SAR ADC and sends the actual digital value as the data output. Quantization events are also recorded in a digital pulse sequence. The sampling frequency is 1 kHz and the internal clock for the SAR and prediction logic is 16 kHz. In the testing, the digital output was sent to an external DAC for the reconstruction of the analog input. The reconstructed signal shows that with a 900 mV amplitude ECG signal, a 50 mV Delta is able to keep the morphology of the waveform for arrhythmia classification. A 200 mV Delta is not acceptable since it introduces distortion in the reconstructed waveform.

**IV. DATA SAVING, ERROR, AND POWER TRADE-OFF**

The primary goal of the proposed ADC is to reduce the total output data amount by selecting only the critical sampling points for quantization. Compared with a conventional SAR ADC, the output of the proposed second-order level-crossing ADC contains both the digital amplitude of the selected sampling point and the timing between selected sampling points. Therefore, each sampling data point has more data than in the conventional SAR ADC. For example, a 10-bit timestamp output means the maximum measurable timing between two selected sampling points is 1024 clock cycles. If the ADC has a 10-bit resolution and the timestamp output means the maximum measurable timing than in the conventional SAR ADC. For example, a 10-bit ADC contains both the digital amplitude of the selected points. Therefore, each sampling data point has more data amount from the proposed second-order level-crossing ADC. The compression Factor also depends on the Delta value and the amplitude of the signal as shown in Fig. 7 (a). In our experiment, the compression factor achieves 6.17 for the ECG signal with negligible distortion of the input signal.

Since the proposed system selects fewer sampling points from the input waveform, it may introduce more errors compared to the conventional ADC. Although for the selected sampling points, the digital values of the proposed ADC are the same as in a conventional ADC, the proposed method does not record the actual amplitude of the sampling points where the predictions are successful. The additional error introduced by removing the sampling points depends on the Delta step and the reconstruction methods, which affects the Effective Number of Bits (ENOB) of the ADC as shown in Fig. 7 (b). The primary reconstruction methods for nonuniform sampling include but are not limited to linear interpolation, polynomial interpolation, cubic spline interpolation, and Lagrange-Chebyshev interpolation [4]. Using a complicated reconstruction method can reduce errors introduced by nonuniform sampling with a cost of high computing overhead.

Power saving is another feature of the proposed ADC. Compared with a conventional SAR ADC, the second-order level-crossing sampling ADC spends more power in performing predictions, which includes the additional digital power of calculating predictions and thresholds, as well as the additional analog power of making two additional digital-to-analog conversions and two more comparisons. Such efforts can
potentially save power from the quantization if the prediction is successful. Since most of the power cost in the SAR ADC comes from the quantization process, the second-order level-crossing sampling ADC saves power in sensing sparse signals. The power saving feature also depends on the Delta value as shown in Fig. 8 (a). A larger Delta makes more successful predictions, which saves more power and improves the compression factor, with a cost of a lower SNR. Therefore, choosing an acceptable Delta is important, which is related to specific applications. The proposed ADC consumes more digital power than a conventional SAR ADC as shown in Fig. 8 (b), which means it could be more benefited by technology scaling down.

Conventionally, the Figure-of-Merit for an ADC focuses on power consumption, sampling rate, area, and resolution. However, the power cost and area from an ADC are usually a small portion of the whole system. Also, a high sampling rate and resolution may lead to a large amount of data that overloads the following processing, storage, and communication systems. In the proposed system, only critical turning points are recorded to reduce the output data amount. Moreover, the turning points identified during analog-to-digital conversion contain important features of the input signal, which further reduces the signal processing workload. A comparison table of the reported second-order level-crossing ADC and other comparable nonuniform sampling ADCs is shown in Table I. Compared to other methods, the proposed ADC provides a high data compression factor and saves power compared to a conventional SAR ADC in sensing sparse signals, while its fully digital implementation doesn’t need a complicated analog division circuitry for calculating input analog slopes.

V. CONCLUSION

This paper presented a novel second-order level-crossing sampling ADC that performs key sampling point selection by predicting the sampling value using prior quantization or prediction results. The prediction and sampling selection are performed digitally without complicated analog division circuitry. The circuit is implemented by modifying the control logic of a conventional SAR ADC. The proposed ADC automatically selects the turning point of the input analog signal and records the amplitude and timing information of the selected points. The signal-dependent data compression factor is 6.17 for sensing ECG signal and saves 30% power compared to a conventional SAR ADC. The proposed ADC has the potential to greatly reduce power cost and computing overhead for the digital processing, storage, and communication circuits in low-power data acquisition systems.

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| Method | This work | CICC’20 [5] | TCASI’13 [6] | TBCASI’18 [7] | JSSC’16 [8] | TCASI’18 [9] | TCASI’20 [3] |
|--------|-----------|------------|-------------|----------------|---------------|---------------|---------------|
| Need Division | No | No | No | No | No | No | Yes |
| Turning Point Sampling | Yes | Yes | No | Yes | No | No | Yes |
| Sampling Value | Real | Slope only | Only at Fixed Levels | Slope only | Only at Fixed Levels | Only at Fixed Levels | Real |
| Technology | 180nm | 180nm | 500nm | 130nm | Fixed Levels | 180nm |
| Voltage (V) | +/-0.5 | 1 | 3.3 | +/-0.6 | 3.5 | 1 | 2 |
| Sampling Rate | 1 kHz | 1 kHz | 20kHz | 1 kHz | 3 kHz | 1 kHz | 1 kHz |
| Power (nW) | 368 | 151 | 8250 | 360 | <1000 | 255 | 1700 |
| Resolution | 10-bit | N/A | 4.8 | N/A | 8-bit | 6.2-7.9 | 12 |
| Area (mm) | 0.39x0.44 | 0.6x0.4 | 1.5x1.5 | 0.52x0.56 | 2x2 | 0.06x0.24 | 0.5x0.27 |
| Compression Factor | 6.17 | N/A | N/A | N/A | N/A | N/A | 6.1 |
| Power Saving Factor | 30.3% | N/A | N/A | N/A | N/A | N/A | 81% |