Power Network Topology Modelling Method Based on CIM

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Abstract. IEC61970 adopts CIM/SVG as the standards of graphic modelling for the power system, but its application is only limited in graphic integration and static topology expression at present. This paper proposed a new topology generation and searching scheme based on CIM which can reflect the actual power network diagram. The method avoids directly searching on the diagram file which is the bottleneck restrictions of this system. The system makes SVG operation program no longer as an independent system, but as the data source of the power network topology. This paper also put forward a new data structure based on this topology method, which makes searching algorithm more real-time and reliable than the traditional method.

1. Introduction

Topology analysis is the basis of fault diagnosis, system simulation and power flow calculation of power system. The algorithms proposed in literature [1,2] are all based on a data structure of power network topology. This paper proposes a grid topology based on IEC61970 - CIM model extraction and application method by establishing a logical view between substation in the form of XML and memory data model. This paper transfer the file search operation to memory data operation, not only the speed is superior to the traditional method of topology, and it can represent 3/2 circuit breaker connection mode complex.

2. CIM Topology Analysis Method and Existing Problems

At present, the main method of using CIM for power grid topology is to complete the automatic generation of topology structure and integrity check based on the plant equipment model. The analytical tools used are mainly DOM/JDOM of document object model and SAX of simple application program interface. XML is used for standardized access [3] [4][5].

This method is completely dependent on its logical view for querying the connection relationship between each electrical component and each other, which will cause the following two problems in practical application:

(1) The speed of topology generation and retrieval is slow. The wiring diagram file of the substation is stored in XML format, which is made through SVG primitives combination form. XML has its great advantage in solving data islands as information exchange format file. But the operation of the XML file is based on file, without any index mechanism. The reading and searching XML data consumes a lot of CPU and memory resources. Therefore, the frequent reading of topology data from the wiring diagram will become the bottleneck of the system operation.
(2) Poor topology reliability. This method directly exposes the wiring of the factory station to the users of the application layer, which is easy to cause the wrong operation of the data, but once this happens, it is not easy to detect, which will lead to the mismatch between the wiring of the factory station and the actual line.

Based on the above reasons, if topological analysis is conducted directly on the CIM model, although there is a complete algorithm as the basis, the execution speed and efficiency of the program are relatively low. According to the characteristics of CIM model, this paper designs a new data structure, which becomes the mapping of CIM in memory. In this way, the physical structure based on topology is converted into memory instead of the XML file stored on the hard disk, which effectively improves the performance of the power grid topology.

3. Memory Mapping Method of CIM

The data structures currently used to represent power networks are generally divided into three categories: triplet notation, matrix notation, and adjacency list notation. The triplet representation and matrix representation are simple and intuitive, but their main disadvantages are fixed structure and single representation. The adjacency list notation is more flexible, but the construction process is complex. This section analyzes how to use the existing CIM model for topology modeling as follows:

3.1. The Traditional Method Indicates the Problem of 3/2 Wiring

Increasingly as the grid size, grid topology increasing number of nodes and the wide use of 3/2 connection, makes the traditional topology method for all kinds of complicated wiring way lack of universality, such as the literature [1] with a triple [device name (1), (circuit breaker), device name (2)], to express the topology information of equipment on behalf of the transformer, busbar and line, so it can’t express 3/2 connection in the circuit breaker directly connected. In literature [6], the topological analysis method of power grid represented by the incidence matrix and the adjacency matrix can only prove the reachable lines of each vertex, while the paths in the middle cannot be described in detail. However, in literature [7], single-port active equipment is used as a node, and the circuit and the closed switch are used as a branch to establish the adjacency list. Likewise, the topology analysis of 3/2 wiring is not carried out. Traditional methods are difficult to express 3/2 connections is the circuit breaker is regarded as the main reasons for the access of the other devices. This reflected in the abstract figure become edge (branch), busbar, transformers and other equipment figure as the vertices (nodes). So the 3/2 connection in the circuit breaker of direct reflected in an abstract figure became two edge without using vertex directly connected. Then the depth or breadth search algorithm based on graph theory will have ambiguity when searching 3/2 wiring.

The uncertainty of node-branch correlation matrix and adjacency matrix represent 3/2 wiring is proved as follows: establish the incidence matrix according to the wiring mode in Fig. 1a, where B is the node-branch incidence matrix and A is the adjacency matrix.

\[
\begin{align*}
B_1 & \quad B_2 \\
L_1 & \quad 1
\end{align*}
\]

In the initial state, B1 and B2 are not connected. According to the connectivity algorithm in graph theory, A^2 is the all-1 matrix, that is, B1 and B2 are connected through a channel of length 2. The intermediate node as a channel can only be L1. On the other hand, if L1 is out of service or has circuit failure, then

\[
\begin{align*}
B_1 & \quad B_2 \\
B_1 & \quad 1 \\
B_2 & \quad 0
\end{align*}
\]
No matter how big \( n \) is in \( A^n \), \( B1 \) and \( B2 \) will never have a path. Therefore, the network topology represented by matrix \( B \) and \( A \) should be shown in Fig.1b instead of Fig.1a.

![Figure 1. Simplified 3/2 connection](image)

The most direct way to solve 3/2 wiring is to consider the circuit breaker as the vertex of the abstract graph, so that both the matrix and the adjacency list can represent the various wiring modes indiscriminately. However, the result is that the number of vertices is too large, which inevitably leads to the decrease of search efficiency. In this paper, a general data structure of common wiring and 3/2 wiring is presented on the premise of adding only a few vertices, so that the search algorithm can traverse the whole network without distinguishing the wiring mode.

### 3.2. Adjacency List Representation Method based on CIM Join Points

IEC61970 reflects the connection relationship between devices through Terminal and ConnectivityNode. Physically connected devices are connected to a common ConnectivityNode in CIM through their own Terminal. The adjacency list establishes a singly linked list for each vertex in the graph, and the nodes in the singly linked list represent all the edges attached to this vertex. By comparison, we can get that each ConnectivityNode in CIM corresponds to a single linked list in the adjacency list. Based on the above analysis, this paper created two new classes based on the Topology package, the Vertex class and the adjNode class, corresponding to the header and table node classes of the adjacency list, respectively. The three domains of Vertex are the access flag bit, the Vertex name, and the first node pointer. The Vertex class consists of bus, circuit, transformer, power supply, and a ConnectivityNode (defined in the program as a Y node) that connects two circuit breakers and one outgoing line, so that the two sides of the two directly connected circuit breakers in the 3/2 wiring are connected through the Y Vertex in this model. The adjNode class reflects the electrical components connected with the Vertex class, that is, the ConnectivityNode connected by an Vertex device has \( n \) terminals, and the corresponding single linked list in the adjacency list has \( n-1 \) adjnodes. Each adjNode class has three fields, the name of the associated electrical component, the circuit breaker that is connected, and the next field. A UML block diagram for creating an adjacency list based on the topology package is shown in Fig.2.

Constructing the adjacency list model by CIM effectively solves the problem of too complex initialization of the adjacency list. On the other side, the adjacency list becomes the mapping of CIM in memory, which greatly improves the topological speed of the power grid. The corresponding relationship between the actual line and the adjacency list is shown in Fig.3.
4. System Implementation

4.1. System Structure

According to IEC 61970-552-4 CIM-XML Model Exchange Format and IEC 61970-453 Diagram Layout Profile Based on CIM, the proposed power grid topology generation hierarchy is shown in Fig. 4:

On the basis of the data structure, it is not necessary to modify the memory data with the change of the actual power grid whether breadth-first search or depth-first search is used. So just determine whether the searched circuit breaker is in the jumped circuit breaker array ArrayList and decide whether to continue the search for the branch. ArrayList can be obtained by searching SCADA, and the topology search and ArrayList update can run in parallel in two threads, so the search efficiency is greatly improved.
The processing process of power grid topology information is mainly divided into three layers: model definition layer, data filling layer and application layer. The model definition layer mainly provides RDF data files conforming to CIM based rules or CIM-XML model data files through RDF Scheme Editor. These data files are used by the data fill layer to consolidate the SVG graphics primitives to form the wiring diagrams for each factory and to provide interfaces to the upper layers in the form of CIS services. The application layer is mainly used in power system control centre. Fault analysis, topology analysis and dispatching auxiliary decision are carried out through different interfaces in control centre.

4.2. Running of Topology Database
The established adjacent list is started with the system in the form of server, and its advantages are as following. Firstly, the traversal algorithm based on adjacency list is quite mature, each client can write different algorithms according to different requirements to get the desired data. Take the outage area as an example. By inputting jumped circuit breakers and then calling the algorithm of the maximum connection subgraph of the graph, the subset that does not contain the generator is the outage area. Secondly, the adjacency list is started once and running in memory, it does not need to be generated repeatedly. It provides topological data needed by different clients in the way of multi-thread access, which improves the parallelism of the system.

5. Application Examples and Search Performance Tests

5.1. Topology Algorithm and Case Analysis
Taking the diagram shown in FIG. 3 as an example, this paper gives the breadth-first search algorithm as shown in FIG. 5. If B3 is assumed to be the initial element, the circuit breaker connection tree generated in the process of queue is shown in FIG.6. If B3 is regarded as a fault line, it can be seen from the analysis that the order in which the components join the set of visited vertices is the order of the fault affected area. The protection corresponding to the uppermost layer of the circuit breaker connected tree shall be the main protection, the second layer shall be the near reserve protection, and the lower layer shall be the remote backup protection.

![Figure 5. BFS based on adjacent list](image5.png)

![Figure 6. Topological analysis process](image6.png)
5.2. Performance Test of Topology
The test scheme generates topology for Shandong 500KV power grid which includes 25 substations. Which contains 2 simple connection wiring diagram, others are 3/2 connection wiring diagram. As a comparison, we also followed the topological analysis method of JDOM described in literature [3][4]. The breadth-first search test was carried out for the wiring files of the station under the MyEclipse workbench in Java environment. The comparison results under the same hardware condition are shown in Table.1.

| Searched Nodes | Time of this system | Time of JDOM |
|----------------|---------------------|--------------|
| 5 Nodes        | 9ms                 | 68ms         |
| 50 Nodes       | 77ms                | 425ms        |
| All 190 Nodes of Grids | 293ms | 2274ms |

As we can see from Table.1, the search time of this paper is much lower than that of JDOM search. With the increase of the number of grid nodes, the rapidity advantage of this search method is more obviously.

6. Conclusion
In this paper, the name of device and its connection relation are extracted from the plant graph file to form the topology adjacency list. The data structure based on topological search is completely decoupled from the CIM model, the selection of search method is more flexible, the program is not restricted by the CIM model, and the computation speed is greatly improved. The system divides the data processing process into three levels, shields the underlying data source to the user, and avoids the disoperation of the original topology data. In the realm of algorithms, topology search is carried out synchronously with SCADA update, which not only improves the running speed of the program, but also makes full use of the hardware resources.

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8. References
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