Conventional neural structures tend to communicate through analog quantities such as currents or voltages, however, as CMOS devices shrink and supply voltages decrease, the dynamic range of voltage/current-domain analog circuits becomes narrower, the available margin becomes smaller, and noise immunity decreases. More than that, the use of operational amplifiers (op-amps) and continuous-time or clocked comparators in conventional designs leads to high energy consumption and large chip area, which would be detrimental to building spiking neural networks. In view of this, we propose a neural structure for generating and transmitting time-domain signals, including a neuron module, a synapse module, and two weight modules. The proposed neural structure is driven by a leakage current of MOS transistors and uses an inverter-based comparator to realize a firing function, thus providing higher energy and area efficiency compared to conventional designs. The proposed neural structure is fabricated using TSMC 65 nm CMOS technology. The proposed neuron and synapse occupy the area of 127 $\mu m^2$ and 231 $\mu m^2$, respectively, while achieving millisecond time constants. Actual chip measurements show that the proposed structure implements the temporal signal communication function with millisecond time constants, which is a critical step toward hardware reservoir computing for human-computer interaction. Simulation results of the spiking-neural network for reservoir computing with the behavioral model of the proposed neural structure demonstrate the learning function.

Deep neural networks (DNNs), which are the second generation of artificial neural networks (ANNs), have extensively explored in recent years for growing number of applications. However, their huge energy consumption especially for the memory access in conventional von-Neumann architecture has forced people to find an alternative way to achieve more power-efficient solutions.  

Spiking neural network (SNN) is one of the attractive solutions as the third generation of ANNs that can realize learning function with low power by mimicking biological neurons. SNNs consist of neurons and synapses, and are usually built using a bottom-up approach, which means that each component of the SNNs needs to be designed first.

Many hardware implementations of pulsed neurons or synapses have been reported. To implement the leaky integrate function of neurons, conventional designs usually build integrators with operational amplifiers (op-amps) and often use large on-chip capacitors and resistors to mimic the millisecond time constants of biological neurons. Moreover, to implement the neuron “fire” function, a dedicated circuit structure of a continuous-time or clocked comparator is usually used to set the threshold for neuron excitation.

The bias current of the continuous-time comparator undoubtedly increases the power consumption of the neuron, while the clocked comparator requires additional clock signal distribution and the complex comparator structure occupies a large chip area. While more advanced processes can achieve low power consumption by reducing supply voltage and static leakage current, this also leads to a narrower dynamic range, smaller available margin, and degraded noise immunity of the voltage/current-domain analog circuits. This is detrimental to conventional neural networks that use analog quantities such as voltage and current to communicate with each other. On the other hand, thanks to the scaled transistors that have an improved operation speed with sharp signal transitions, the analog information can be represented more efficiently in time domain, i.e. a time interval of two signal transitions. This so-called time-domain circuit have another advantage in its power efficiency as it often consists of inverters or logic gates that ideally consume no DC power. Thus, time-domain circuits are ideal for future implementations of low-power SNNs.

In this paper we propose an original neural structure for generating and transmitting time-domain signals to compose a time-domain neural network. The integrated structure includes neuron and synapse modules that respectively generate and transmit time-domain signals, as well as weight modules for learning functions. One of our main target applications is reservoir computing, which processes information related to human activity. Our application targets simpler and less data-intensive processing such as bio-signals. In reservoir computing, learning functions such as ECG and speaker recognition as well as handwriting recognition can be implemented using only a few hundreds of neurons. Ref. shows that learning performance improves when the time constants of the input effects are matched between the target function and reservoir dynamics, and we use millisecond time constants as a design target for a neural structure that will be used to process time-series information of human activities. We use the behavioral model of the proposed neural structure to construct the SNN for reservoir computing and implement the learning function, which proves that our proposed neural structure can be used.

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for reservoir computing.

The designed and fabricated neural structure is shown in Fig. 1a, which is based on the proposed neuron, synapse, and weight modules, which will be described in detail below. In this structure, the input of the neuron module is connected to two weight modules, one for tuning the inhibitory signal and the other for the excitatory signal. We fabricated the proposed neural structure shown in Fig. 1a with TSMC 65 nm standard CMOS technology. The micrograph of the chip is shown in Fig. 1b, where the die area of neuron, synapse and weight modules are 127 \( \mu \text{m}^2 \), 231 \( \mu \text{m}^2 \) and 525 \( \mu \text{m}^2 \), respectively.

The LIF neuron model consists mainly of a membrane capacitor, a leaky resistor, and a voltage comparator. Neurons receive signals from other neurons via synapses and the soma generates action potentials in response to these external signals. If a neuron receives a sufficient number of spikes through the synapse, its membrane potential will reach a threshold value, causing the neuron to “fire” \(^{(6,25,26)}\).

The use of inverters to implement the “fire” function is already known as an alternative to comparators. Ref. 27 has proposed an inverter-based neuron, which is well suited for use in the proposed neural structure, and therefore the neuron used in this study was designed based on Ref. 27 which is shown in Fig. 2a. It consists of input device, leaky integrator device, fire device and delay device. Originally in Ref. 27 the circuit is not assumed to be designed as an element to build a neural network, thus does not have a structure to receive excitatory and inhibitory signals. In the proposed circuit, on the other hand, the input device that consists of \( M_1 \) and \( M_2 \) receives an excitatory input and an inhibitory input, respectively. The inputs to \( M_1 \) and \( M_2 \) are narrow pulse signals as shown in Fig. 2b, which is generated from a pre-stage synapse. The activity of the pre-stage synapse is represented by the pulse frequency, and the coupling weight is represented by the pulse width. When more than one pre-stage synapses are connected to compose a network, the multiple pulses can be applied through OR logic, or by adding input devices connected in parallel. With the parallel input devices, the neuron circuit can accept multiple pulses even at the same time.

In leaky-integrator device, \( C_{\text{mem}} \) represents the cell membrane of the neuron, and \( M_3 \) can be regarded as a leaky resistor in the resting state. When there is no external input to the input device, the capacitor is charged by the leakage current of \( M_3 \) and \( M_4 \), and the membrane potential \( V_{\text{mem}} \) increases continuously with the inflow of the leakage current (the current is integrated as shown in Fig. 2b(i)). At this point, since \( M_3 \) is in off state, it can be considered as a resistor in parallel with the capacitor, i.e. leaky resistor, capable of achieving a long time constant.

Once \( V_{\text{mem}} \) rises to the threshold voltage \( V_{\text{th(Fire)}} \), the fire device is activated (Fig. 2b(ii)). In conventional designs, LIF neurons mostly use dedicated circuit structures of continuous-time or clocked comparator to set the threshold voltage. This is not friendly for building SNNs that are as energy efficient and bio-scale as the brain. In this study, the fire device is implemented by an inverter-based comparator that can set the threshold voltage by two transistors instead of a continuous-time or clocked comparator. To realize an accurate threshold voltage for an inverter-based comparator, we may use an auto-zeroing technique that periodically sense, store and cancel the offset with switches and capacitors\(^{(25)}\). However, it requires multiple-phase clocks to control the switches, thus is not suitable for area-and-power-efficient reservoir implementations. Though with a simple inverter-based comparator there may be a threshold variation due to process, voltage and temperature fluctuations, it can be seen as mimicking the difference between individuals of real neurons. In addition, the learning function is able to compensate for threshold differences and process variations\(^{(20)}\).

When there is an excitatory pulse input, \( M_1 \) will be turned on instantaneously, which causes more current to charge \( C_{\text{mem}} \) and \( V_{\text{mem}} \) to rise rapidly. Conversely, an inhibitory pulse input signal will cause \( M_2 \) to turn on momentarily, causing \( C_{\text{mem}} \) to charge slower or even discharge through \( M_2 \), which in turn slows down the rate of \( V_{\text{mem}} \) rise or makes it fall.

When the fire device is activated, it generates a low level of \( V_{\text{Fire}} \) to be connected to \( M_4 \), which will increase the current to charge the membrane capacitor \( C_{\text{mem}} \), resulting in an instantaneous increase of the membrane potential \( V_{\text{mem}} \), which promotes the triggering of the fire device. This mimics the influx of Na\(^+\) into the cell membrane prompting a rapid increase in membrane voltage, i.e., a positive feedback effect. Finally, the low level of \( V_{\text{Fire}} \) generated from the fire device is converted to a high level of \( V_{\text{Spike}} \) (Fig. 2b(iii)) by a delay device that includes a three-stage inverter and connects the \( V_{\text{Spike}} \) to \( M_3 \) and \( M_4 \), resetting \( V_{\text{mem}} \) to zero. This process mimics the activation of K\(^+\) channels in biological neurons, resulting in the outward flow of K\(^+\) ions and the eventual return of the cell membrane to its resting state.

Synapses are essential modules in SNNs, as neurons are interconnected by them. We have designed a neuron module for generating time-domain signals, and then we need a transmission medium, i.e., a synapse, to transmit this time-domain signal to other neurons. To compose a complete neural network, we design a synapse module based on frequency signals, as shown in Fig. 2c. The synapse consists

![FIG. 1: (a) The proposed structure and (b) a micrograph of the chip.](image-url)
mainly of a voltage-controlled ring oscillator operating under a leakage current, which is composed of a three-stage inverter \((M_6, M_7, M_8, M_9, M_{10}, M_{11})\). The previous neuron circuit fires and generates a spike \(V_{\text{Spike}}\), which is inverted by an inverter, making \(M_5\) open for a short time, and the current flowing through \(M_5\) charges \(C_{\text{SYN}}\), which will increase \(V_{\text{SYN}}\). Once \(V_{\text{SYN}}\) reaches the voltage that triggers the oscillation, the ring oscillator begins to oscillate (Fig. 2b(iv) and Fig. 2b(v)). If the preceding neuron does not fire for a long time, \(V_{\text{SYN}}\) will leak until the initial state, at which point the synapse becomes inactive again. Since \(V_{\text{SYN}}\) is equivalent to the supply voltage of the ring oscillator, the current flowing out of \(M_5\) controls \(V_{\text{SYN}}\) and thus the frequency of the ring oscillator.

SNNs achieve learning function by adjusting the weights; therefore, we propose a weight module that is compatible with the proposed time-domain neuron and synapse modules described above, as shown in Fig. 2d. The proposed weight module tunes the time-domain information, which is the width of the output pulses. This module consists of a delay line, a multiplexer, and an AND gate. \(V_{\text{Ring}}\) is the square wave signal from the synapse that will pass through the delay line. \(V_{\text{Weight}}\) is the digital code that represents weight, which is determined after learning and is used to control the multiplexer. The width of the output pulse that corresponds to the time-domain weight is adjusted according to which tap in the inverter chain is selected by the multiplexer. As mentioned earlier, if the excitatory or inhibitory pulse width is wide, the voltage \(V_{\text{mem}}\) in the subsequent neuron is charged or discharged faster, respectively. This corresponds to a large weight. In this study, we chose a multiplexer with 16 inputs, i.e. four bit weights (0000 to 1111). The output of the weight module is connected to the input device of the subsequent neuron circuits. The frequency of the pulse (pulse spacing) and the width of the pulse act simultaneously on the neuron to change its activity. The frequency of the pulse is determined by the output frequency of the previous synapse, while the coupling strength depends on the width of the pulse output determined by the weight module.

Figure 3a shows the experimental setup used to test the fabricated neural structure chip (Fig. 1b), where the chip was placed on a probe station Summit11000 and tested with probes in direct contact with it. In the experiments, we assume that
the inputs of the two weight modules is the pre-stage synapses, which is emulated by the arbitrary function generators. The output of the neuron is connected to the synapse module, and the output of which will be varied in response to the change in the output of the neuron. We used a Tektronix AFG31252 arbitrary function generator as a pre-stage synapse to provide square wave signals for our fabricated neural circuits. At the same time, we observed the output waveforms using oscilloscopes (Keysight MSOX6004A and DSOX93304Q).

The experimental results are shown in Figs. 3b, 3c and 3d. To verify the effect of weights on the firing rate of neurons, we fixed the frequency of the pre-stage synapse output (function generator) at 100 Hz and observed the change in the firing rate of neurons for 4 chips by adjusting the weights module. We averaged the spike frequencies 1024 times over a time range of 100 ms to derive the corresponding neuronal firing frequency under each weight setting, as shown in Fig. 3b. The proposed neuron is basically firing with the rate determined by the leakage currents into and out from $C_{\text{mem}}$ in balance, and input from the previous stage modulates it. We can see that when the weights become larger, the neuron module firing frequency becomes larger. Mainly due to the process variation of the FETs, the firing frequency fluctuates in about $\pm 10\% \sim 17\%$ over 4 chips. Especially for the use in a reservoir, however, due to the random weights in its recurrent connections, these random variations should be compensated for during the learning process in the output weights.

Figure 3c compares the variation of neuron fire times depending on the signal from the pre-stage synapse. The insets (i), (ii) and (iii) of Fig. 3c show the cases with 100 Hz inhibitory input (weight is set to 1100), no input, and with 100 Hz excitatory input (weight is set to 1100), respectively, from which we can see that the inhibitory input decreases the fire frequency of the neuron and increases the fire interval, while the excitatory input works as the opposite of the inhibitory input. The experimental results show that the firing interval of

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**FIG. 3:** (a) A photo of the experimental setup, (b) the measured firing rate of the neuron for 4 chips, (c) the measured waveforms of the neuron output, and (d) the measured waveforms of the synapse output.
FIG. 4: (a) Another combined structure fabricated to evaluate the synapse and (b) the measured waveforms of $V_{\text{Ring}}$ and $V_{\text{SYN}}$.

FIG. 5: (a) The behavioral model of the SNN for reservoir computing based on the proposed neural structure. (b) The system-level behavioral simulation results: (i) based on a model with $15 \text{ Hz} - 200 \text{ Hz}$ frequency tuning range, zoomed-in view of the (ii) excitatory and (iii) inhibitory input signals converted from the output, (iv) based on $15 \text{ Hz} - 2 \text{ kHz}$ and (v) $15 \text{ Hz} - 20 \text{ kHz}$ frequency tuning ranges.

The proposed neuron is on the order of milliseconds, which is in accordance with the feature of biological neurons having millisecond time constants. When no signal is fed from the pre-stage synapse, the power consumption is about 800 pW, generating about 20 spikes in a 100 ms cycle. From this, it can be roughly estimated that each spike consumes about 4 pJ of energy. Subsequently, the insets (i), (ii) and (iii) of Fig. 3c were used as input signals to the synapse to influence $V_{\text{Ring}}$. The measured $V_{\text{Ring}}$ waveforms in these three cases are shown in Fig. 3d. The average of the frequencies for each case measured in 5 s time period are 41 Hz, 90 Hz and 98 Hz, respectively. The feasibility of this synapse output frequency range will be validated with system-level simulations in the following discussion.

To facilitate the observation of the synchronous response of the synapse, we also fabricated the structure of Fig. 4a. Figure 4b is the experimental results on Fig. 4a. We used a Tektronix AFG31252 arbitrary function generator to generate a 10 Hz square wave signal $V_{\text{IN}}$ as shown in Fig. 4a(i). After $V_{\text{IN}}$ passes through a weight module, it produces a spike signal $V_{\text{OUT(Weight)}}$. The voltage $V_{\text{SYN}}$ is observed through an on-chip source follower as an analog buffer. Though $V_{\text{OUT(Weight)}}$...
TABLE I: Performance Comparison of Stand-Alone Neuron Circuits.

| Ref. | Technology | Energy per spike (pJ) | Single neuron area (μm²) | Frequency (Hz) | Neuron model | Sim. or Meas. |
|------|------------|-----------------------|--------------------------|----------------|-------------|--------------|
| 13   | 350 nm CMOS | 900                   | 2573                     | 100            | IF          | Meas.        |
| 14   | 180 nm CMOS | 9.3 × 10⁴             | N/A                      | 10⁴            | LIF         | Meas.        |
| 15   | 65 nm CMOS  | 41                    | 538                      | 300            | LIF         | Sim.         |
| 16   | 65 nm CMOS  | 200                   | 3363                     | 1.9 × 10⁶      | AdEx-IF     | Meas.        |
| 18   | 32 nm SOI MOSFET | 35                | 1.8                      | 10⁶            | LIF         | Meas.        |
| 19   | 22 nm FD-SOI | 14                    | 900                      | 30             | AdEx-IF     | Meas.        |
| 21   | 22 nm CMOS  | 1.17/0.36             | 70                       | 30/100         | LIF         | Sim.         |
| this work | 65 nm CMOS  | 4                     | 127                      | 230            | LIF         | Meas.        |

*Adaptive-exponential integrate-and-fire.

is not designed to be observed from outside as it is a narrow pulse, with the arrival of the \( V_{\text{OUT(Weight)}} \) after the falling edge of \( V_{\text{IN}} \), the \( V_{\text{SYN}} \) voltage at the synapse rises instantaneously as shown in Fig. 4b(ii), which in turn increases the frequency of \( V_{\text{Ring}} \). If the \( V_{\text{OUT(Weight)}} \) does not arrive for a long time, \( V_{\text{SYN}} \) decreases, which in turn affects the \( V_{\text{Ring}} \) frequency to become smaller.

Table I shows the performance comparison among stand-alone neuron circuits. The proposed neuron circuit has advantages in terms of energy consumption and area. The designs in Refs. 13, 16 used a continuous-time or a clocked comparator, and these designs take up a large amount of chip area as well as power consumption. The neuron fabricated in a non-CMOS process proposed in Ref. 18 does not require a comparator, which leads to an advantage in area. However, its energy consumption is relatively high and these particular technologies are less mature and thus more costly compared to standard CMOS processes. Both Ref. 19 and Ref. 21 are being fabricated in an advanced process. However, compared to this work Ref. 19 does not have an advantage in terms of energy consumption and area. Although Ref. 21 shows better energy efficiency with simulation results, when normalized by the technology node, the proposed neuron achieves better area efficiency.

To demonstrate the feasibility of the proposed spiking neuron and the ring oscillator-based synapse circuits, a behavioral simulation is carried out in MATLAB environment as shown in Fig. 5a. In this simulation, 100 neurons are used with random recurrent connections with the proposed synapse and weighting modules. The proposed weight modules are applied only in the reservoir layer and their weights are assigned randomly in advance and fixed during the learning process. Thus the random fluctuations in the reservoir are compensated for during the learning process in the output weights. To establish a realistic simulation, the output frequency range of each synapse is set from 15 Hz to 200 Hz based on the actual measurement results. The recursive least square (RLS) algorithm is used to train the output weights as introduced in Ref. 30. A 10 Hz sinewave, which corresponds to the time-scale of human-activity-related information, is used as an example of supervisory input signal. The supervisory and the trained output signal are shown in Fig. 5b(i). The feedback signal from the output is converted to excitatory and inhibitory pulse trains whose frequencies are in proportion to the absolute value of the output amplitude as shown in Figs. 5b(ii) and (iii), respectively. After 5 periods of supervisory signal, the output weights are fixed and the SNN generates the learned signal by itself, which demonstrates the feasibility of the proposed neural structures for learning function. We have also found from these simulations that to further improve the learning capability the output frequency tuning range of the synapse should be increased, which can be done by optimizing the synapse circuit. For example, with the extended frequency tuning ranges from 15 Hz to 2 kHz and 15 Hz to 20 kHz, the learned signals become smoother to better reproduce the supervisory signal as shown in Figs. 5b(iv) and 5b(v), respectively.

In summary, we have proposed a neural structure for generating and transmitting time-domain signals. The proposed neuron and synapse occupy an area of 127 μm² and 231 μm², respectively. This structure does not use op-amps and continuous-time or clocked comparators, while the firing function is realized with an inverter-based comparator to provide advantages in area and power consumption. The proposed time-domain neural structure benefits from scaled process technologies compared to conventional voltage/current-domain designs. Actual chip fabrication and measurement results demonstrate the temporal signal communication function with millisecond time constants. The proposed time-domain neural structure is well suited for building spiking neural networks for processing real-time time-series information for human-computer interaction.

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