Grid-Coupled Dynamic Response of Battery-Driven Voltage Source Converters

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Abstract—With the increasing interest in converter-fed islanded microgrids, particularly for resilience, it is becoming more critical to understand the dynamical behavior of these systems. This paper takes a holistic view of grid-forming converters and considers control approaches for both modeling and regulating the DC-link voltage when the DC-source is a battery energy storage system. We are specifically interested in understanding the performance of these controllers, subject to large load changes, for decreasing values of the DC-side capacitance. We consider a fourth, second, and zero-order model of the battery; and establish that the zero-order model captures the dynamics of interest for the timescales considered for disturbances examined. Additionally, we adapt a grid search for optimizing the controller parameters of the DC/DC controller and show how the inclusion of AC side measurements into the DC/DC controller can improve its dynamic performance. This improvement in performance offers the opportunity to reduce the DC-side capacitance given an admissible DC voltage transient deviation, thereby, potentially allowing for more reliable capacitor technology to be deployed.

I. INTRODUCTION

As synchronously connected power systems shift towards systems with high penetration of converter-interfaced generation (CIG), it becomes more critical to understand the dynamical and transient behavior of these systems. These converter-dominated power systems are already prevalent in the form of islanded microgrids, motivated by increased resilience to natural disasters [1, 2]. Recent work has explored the small-signal stability of the DC/AC converter and its interaction with the grid. A common approach when analyzing the voltage source converter (VSC) behavior is to model the DC-side of the converter as an ideal voltage source [3, 4]. On the other hand, when studying the dynamics of the DC-side, the grid is often simplified as a resistive load [5, 6]. From a small-signal perspective, an independent analysis of each subsystem separately may be adequate due to the minimal interaction of their control loops. However, this approach gives little insight into the dynamical behavior of these coupled systems during grid-scale transient events, particularly, faults or large load steps and when the operating conditions differ substantially from the steady-state operating point used in the linearization.

This paper explores the performance of the DC-link capacitor of a battery energy storage system (BESS) subject to AC-side disturbances, under different DC-side control strategies. The objective of these control loops on the DC-side is to tightly regulate the DC voltage across a DC-link capacitor. The DC-link capacitors act as energy buffers and support a constant voltage on the DC-side of the CIG. A tight regulation of this voltage is critical to the operation of the CIG, as momentary drops in this voltage restrict the VSC’s power production capabilities [6]. Therefore, large electrolytic capacitors are used in order to have a substantial buffer to minimize the DC voltage deviations during disturbances. These capacitors being typically bulky, expensive, unreliable are one of the most common modes of failure in power electronic systems [7]—with system transients and overloading identified as two of the primary causes of failure [8].

One proposed improvement in converter design is to replace these electrolytic capacitors with small film capacitors that are more robust and reliable [9]. As the DC-link capacitance is reduced, voltage fluctuations during transients increase as there is a momentary mismatch between the power injected into the grid and the power supplied from the DC source e.g., a battery. In order to deploy these small film capacitors, the DC-side control must rapidly correct any difference between these currents to ensure adequate AC-side operation and minimize transient over-voltages on the capacitor.

In this work, we examine different control approaches for minimizing the required DC-link capacitance of a BESS. Specifically, we consider the case of a grid-forming inverter supporting an islanded microgrid with a BESS as its DC source. Grid-forming inverters differ from grid-following inverters—the dominant mode of operation today, in that the former behave as a controllable voltage source behind a coupling reactance [10]. Consequently, they do not directly control their power injection into the grid but rather control the frequency and amplitude of their output voltage [11]. Their power injections, therefore, inherently increase or decrease to balance any changes in load. When choosing a DC-link
capacitor to regulate the DC voltage of a grid-forming inverter, adequate care must be taken that it is appropriately sized to ensure satisfactory behavior under the largest expected load change and/or fault conditions, thus presenting challenges in the sizing of the DC-link capacitor for grid-forming converters. This work considers the existing measurements used in the control loop of grid-forming converters as inputs into the DC/DC controller to predict the evolution of DC-link capacitance dynamics and consequently, improve the regulation of the DC bus voltage.

For modeling our DC source, we consider a Li-ion battery as the BESS. In comparison to previous work which modeled the battery as an ideal voltage behind a resistor [5], [6], we employ a model of the battery which captures the dynamics of the electrochemical processes as we increase/decrease the size of the battery to regulate the DC voltage of a grid-forming inverter, therefore, comprises 13 states of the form: 

\[ x = x^d + jx^q. \]

The proposed control model depicted in Fig. 1 is based on a state-of-the-art VSC control scheme described in [12]-[14]. The power calculation unit computes the active and reactive quantities given by \( p_c + jq_c = e_c i_g \) where \( (\cdot)^* \) denotes the complex conjugate. This is followed by an outer control loop that consists of active and reactive power controllers providing the output voltage magnitude \( v_c \) and frequency \( \omega_c \) references by adjusting the predefined set points \( (x^*) \) according to a measured power imbalance:

\[ \omega_c = \omega_c^* + R_p^c (p_c^* - \tilde{p}_c), \quad v_c = v_c^* + R_q^c (q_c^* - \tilde{q}_c), \]

(1)

where \( R_p^c, R_q^c \) denote the active, reactive power droop gains and \( \tilde{p}_c, \tilde{q}_c \) represent the low-pass filtered active, reactive power measurements of the form:

\[ \tilde{p}_c = \omega_c (p_c - \tilde{p}_c), \quad \tilde{q}_c = \omega_c (q_c - \tilde{q}_c), \]

(2)

where \( \omega_c \) is the filtering frequency. The outer-loop voltage set point may be passed through a virtual impedance block \((v_e, l_e)\), resulting in a cross-coupling between the \( d \)- and \( q \)-components via a terminal current measurement \( i_g \) as

\[ \bar{v} = v_c - (v_r + j\omega_c i_r) l_g. \]

(3)

This new voltage vector set point and the frequency set point are then fed to the inner control loop consisting of cascaded voltage and current controllers operating in a SRF

\[ \tilde{i}_s = K_p^f (\bar{v} - e_g) + K_i^f \xi + j\omega_c c_f e_g + K_f^f i_g, \]

(4a)

\[ \bar{v}_m = K_p^g (\tilde{i}_s - i_s) + K_i^g \gamma + j\omega_b l_g i_s + K_f^g e_g, \]

(4b)

where \( \xi = \bar{v} - e_g \) and \( \gamma = \tilde{i}_s - i_s \) denote the respective integrator states; \( i_s \) and \( \bar{v}_m \) represent the internally computed current and voltage references, \( e_g \) is the voltage internally measured at the converter terminal to the grid, \( i_s \) is the switching current, \( K_p^f, K_i^f, K_f^f \) are the proportional, integral, and feed-forward gains respectively, and superscripts \( v \) and \( l \) denote the voltage and current SRF controllers. The output voltage reference \( v_{m} \) combined with the DC-side voltage \( v_{bc} \) generates the Pulse-Width Modulation (PWM) signal \( m \).

The electrical interface to the microgrid includes an \( RLC \) filter \((r_f, l_f, c_f)\) and an equivalent impedance \((r_g, l_g)\) modeled in SRF and defined by the angular converter frequency

\[ \tilde{i}_g = \omega_b l_g (v_{m} - e_g) \]

(5a)

\[ \bar{v}_g = \omega_b l_g (\tilde{i}_s - i_g) - j\omega_c \omega_b e_g, \]

(5b)

with \( v_{m} \) representing the modulation voltage and \( v_l \) denoting the nodal voltage at the load bus. The system base frequency is represented by \( \omega_b \) and equals the nominal frequency. The complete state-space representation of a single grid-forming inverter, therefore, comprises 13 states of the form

\[ \dot{x}_{vsc} = \begin{bmatrix} e_{dq}^g, \dot{i}_{dq}^g, \dot{x}_s^g, \xi_{dq}^g, \gamma_{dq}^g, \theta_c, \tilde{p}_c, \tilde{q}_c \end{bmatrix}^T. \]

(6)

The control input vector \( u_{vsc} = [p_c^*, q_c^*, v_c^*, \omega_c^*]^T \) provides operator set points. More details on the overall converter control structure and employed parameterization can be found in [4], [13], [14].

![Fig. 1: Grid-forming VSC control scheme.](image-url)
B. DC-side model

The modeling of the DC-side consists of a BESS, an idealized DC/DC buck/boost converter with an appropriately sized inductor, and a DC-link capacitor. This interconnected system is then interfaced to the VSC as shown in Fig. 2

![DC-side model](image)

**1) DC/DC Controller:** For the DC/DC controller in Fig. 2, we investigate the improved dynamical performance with the inclusion of the measured AC-side quantities into the control logic. A dual-loop PI DC/DC controller is shown in Fig. 3 and modeled as

\[
\dot{\eta} = v_{DC}^* - v_{DC}, \quad (7a)
\]

\[
i_{ref} = K_{bc}^{p} (v_{DC}^* - v_{DC}) + K_{bc}^{q} \eta, \quad (7b)
\]

\[
\dot{\zeta} = i_{ref} + i_{out} - i_{in}, \quad (7c)
\]

\[
d = K_{bc}^{p} (i_{ref} + i_{out} - i_{in}) + K_{bc}^{q} \zeta + K_{pred} \Delta i_{out}. \quad (7d)
\]

The outer-loop \((7a)-(7b)\), maintains a constant DC bus voltage while the inner loop \((7c)-(7d)\), is for current tracking. The inclusion of a feed-forward term \(i_{out}\), in the internal PI control loop is for improving the controller performance by the addition of information about the disturbance. This disturbance was primarily a set-point change of the VSC in previous works [5]. For the case of a grid-forming VSC, however, this disturbance includes unexpected load changes where the additional required power will be inherently drawn from the DC-link capacitor.

The addition of the term \(K_{pred} \Delta i_{out}\) in \((7d)\) is motivated by \([15]\), where the authors sought to minimize the required DC-link capacitance for a converter-interfaced three-phase load. In \([15]\) the authors note that the inclusion of a feed-forward term alone is inadequate to instantaneously balance the current flow across the capacitor due to inherent system response time delays, mainly due to inductor dynamics. To offset these delays, we use a one-step predictor based on the forward Euler method to predict the evolution of system dynamics. The feed-forward predicted current, \(\Delta i_{out}\), is approximated by \([6]\)

\[
\Delta i_{out} \approx \frac{\Delta P}{\Delta v_{DC}} \approx T_s (v_{DC}^* i_{out}^d + v_{DC} i_{in}^d), \quad (8)
\]

where \(T_s\) is the switching period of the DC/DC converter, \(i_{in}^d\) and \(i_{out}^d\) are calculated using \([5,6]\). We benchmark the improvement in dynamical performance for a non-zero \(K_{pred}\) against the controller in \([5]\). The advantage of a one-step predictor over derivative control in a PID controller is that we can predict the evolution of the DC-side dynamics before they begin to manifest and minimize noise amplification in estimating the rate of change of the current. The duty-cycle \(d\) of the DC/DC converter in this work has a maximum value of 0.9 to mimic the behavior of a practical converter \([6]\).

2) Battery Model: As previously outlined, prior work on this topic modeled the electrochemical battery as an ideal voltage source behind a resistor \([5,6]\). In the presence of a large DC-link capacitance and consequently a large energy buffer, this is a reasonable modeling assumption. However, as we reduce the DC-link capacitance, the dynamics of the electrochemical storage may become more important to model. A common method for parameterizing an equivalent circuit model for batteries is electrochemical impedance spectroscopy \([11,17]\). This method measures the voltage response to harmonic current input across a frequency range of interest (3 kHz to 30 kHz \([18]\) ) and an equivalent circuit is adapted to this data. These experimental data show that at high frequencies (\(\geq 250 - 400\) Hz) the battery exhibits inductive behavior while lower frequencies (\(\leq 250 - 400\) Hz) have a more capacitive response \([11,18,19]\). A generalized battery is shown in Fig. 4 where the high frequency behavior is modeled by a series of 2 \(RL\) parallel branches and the low frequency behavior is modeled by a series of 2 \(RC\) parallel branches.

![Battery model](image)

Within this work we combine the two-time constant \(RC\) battery model from \([20]\) with the two-time constant \(RL\) model from \([18]\) as shown in Fig. 4. Both of these batteries’ chemistries are based on Lithium-ion and offer reasonable initial parameterization of a dynamic BESS model.

3) DC-side Electrical Model: In practice, the DC/DC converter is a buck/boost converter capable of both charging and discharging the battery. Here, we focus on the case when the converter is operating in the boost mode, i.e., supplying power to the grid. A similar analysis holds for the buck mode of operation. The per-unit averaged equations governing the electrical behavior on the DC-side with the converter operating in continuous mode, similar to \([21]\), are then given by

\[
i_{11} = \frac{\omega_b}{l_{b1}} (r_{b1} (i_b - i_{11})), \quad i_{12} = \frac{\omega_b}{l_{b2}} (r_{b2} (i_b - i_{12})), \quad (9a)
\]

\[
\dot{v}_{c_{b1}} = \frac{\omega_b}{c_{b1}} (i_b - v_{c_{b1}} / r_{b3}), \quad \dot{v}_{c_{b2}} = \frac{\omega_b}{c_{b2}} (i_b - v_{c_{b2}} / r_{b4}), \quad (9b)
\]

\[
v_b = v_{oc} - i_b r_{b0} - r_{b1} (i_b - i_{11}) - r_{b2} (i_b - i_{12}) \quad (9c)
\]
presented in Section III-A and identify a set of gains that result from the linearized model of our system, as is the current flowing into the AC grid and given by

\[ \dot{i}_{\text{out}} = \frac{p_{\text{inw}}}{v_{\text{dc}}} = \frac{v_{\text{in}}^d + v_{\text{in}}^q}{v_{\text{dc}}} \cdot \]  

(10)

The full state-space model of the DC-side with a 4th-order model of the DC-side neglects the inductor dynamics of the battery (i.e., retains only the 2 RC branches in Fig. 4), while the 0th-order model further neglects the dynamics of the capacitor and simply represents the battery as a voltage source behind a resistor, as in [5].

In the per unit case, the DC-side base power is the same as the AC-side. The DC-side base voltage, however, is two times the AC-side. The DC-side base voltage, however, is two times

\[ i_{\text{DC}} = \frac{\partial f}{\partial x} \bigg|_{(x_{eq}, u_{eq}, w_{eq})} \]  & \[ B = \frac{\partial f}{\partial w} \bigg|_{(x_{eq}, u_{eq}, w_{eq})}. \]

(16)

The task of small-signal tuning involves finding a set of DC-side control gains

\[ K^\text{dc} = [K^\text{pDc}, K^\text{vdc}, K^\text{qDc}, K^\text{bDc}, K^\text{pred}] \]

(17)

which satisfy some pre-specified design requirements, e.g.,

\[ \Re[l_i(A(K^\text{dc}))] \leq \lambda_{\text{crit}} \quad \forall i, \]

\[ \zeta_i \geq \zeta_{\text{crit}} \quad \forall i, \]

\[ K_{\text{dc, min}} \leq K^\text{dc} \leq K_{\text{dc, max}}. \]

(18a)

(18b)

(18c)

where \( \lambda \) and \( \zeta \) correspond to the eigenvalues and the damping ratio of the linearized model respectively, \( \lambda_{\text{crit}} \) and \( \zeta_{\text{crit}} \) are design requirements, and \( K^\text{dc, min} \) and \( K^\text{dc, max} \) represent some pre-specified limits on the control gains. We denote this set of all permissible gains by the set \( \Gamma \).

B. Large-signal tuning

On identifying a set of suitable small-signal gains \( \Gamma \), an exhaustive search over this set is performed to optimize the dynamical performance of the full non-linear system when it is subject to large disturbances, e.g., large load step changes. In particular, we seek to identify the set of gains that minimize the DC voltage deviation from its set point. This can be expressed mathematically as minimizing the \( \ell_2 \)-norm

\[ \min_{K^\text{dc} \in \Gamma} \|v^*_\text{dc} - v_{\text{dc}}(t)\|_2 \]

subject to (1) - (9)

(19)

where \( p_i(t) = p_{i1}, p_i(t) = p_{i1} + \Delta p_i \), \( p_{i1} \) is the nominal active power load and \( \Delta p_i \) represents a disturbance in the form of a step-change increase in the load. We first optimize the DC/DC control gains with \( K^\text{pred} = 0 \) and then benchmark the improved dynamical performance for cases where \( K^\text{pred} \neq 0 \). Section IV discusses the design requirements and disturbance used in (18) and (19) respectively.

IV. RESULTS

The simulations are performed using the Julia programming language. The ModelingToolkit.jl package is used to construct the non-linear system and perform the Jacobian evaluations. The power rating of the VSC is 200 kVA and the parameters are taken from [12] while parameters for the DC-side are presented in Appendix A. The controller design parameters used for both the small-signal and large-signal tuning are shown in Table I The small-signal parameter search is carried out by a grid search with step size 0.5. All the analysis presented here is available on Github[1]

TABLE I: Controller tuning parameters

| Specification | \( \lambda_{\text{crit}} \) | \( \zeta_{\text{crit}} \) | \( K^\text{dc, max} \) | \( K^\text{dc, min} \) | \( \Delta p_i \) |
|---------------|----------------|----------------|----------------|----------------|----------------|
| Value         | -3             | 0.35           | 10             | 0              | 0.5 p.u.       |

[1]https://github.com/Energy-MAC/DCSideBatteryModeling
A. Comparing BESS Models

In Fig. 5, we compare the DC-side voltage of the three BESS models, i.e., 4th, 2nd, and 0th orders for non-optimized controller gains under a load step change of $\Delta p_1 = 0.5$ p.u. We observe that all models are in agreement regarding the dynamical response (also true for different controller gains). Furthermore, we note that the results here only apply to a Lithium-ion based BESS for the parameters from [18], [20]. For the case of compressed air storage with associated mechanical dynamics and redox flow batteries, with different underlying chemistry; a higher order model representation may be necessary.

B. Impact of one-step predictor

In order to examine the improvement in controller performance by inclusion of the AC-side measurements, we examine the response of the system to a load step change of $\Delta p_1 = 0.5$ p.u. for varying values of $K_{\text{pred}}$. Fig. 6 shows the DC voltage for three different values of $K_{\text{pred}}$. We observe up to a $\sim 10\%$ reduction in the maximum DC voltage error after including the AC measurements. This reduction, achieved using existing measurements readily available in the VSC control loop, offers a means to reduce the severity of transients across the DC-link capacitor and reduce overloading in the event of over-voltage, two of the dominant reasons for premature failure [8].

Fig. 7 further explores the performance of the optimized controller for varying DC-link capacitor sizing. We see that the inclusion of AC-side measurements does offer some improvement, however, due to the saturation behavior of the DC/DC boost converter this improvement is upper-bounded. Therefore, while the AC-side measurement improves the dynamical performance and reduces transient behavior across the capacitor, it only offers a modest reduction in DC-link capacitor sizing for a pre-specified $\ell_2$ norm performance requirement.

In order to understand the limiting factor in the response of the BESS to regulate the DC voltage, we examine the battery current $i_b$, shown in Fig. 8. We can see that the dead-time of the DC/DC controller only accounts for a small proportion of the delay in the response. The majority of the delay is due to the dynamics of the DC/DC inductor, in this case 3 mH. While this is a physical design limitation and there exist approaches to minimize the required inductance to improve dynamic response, e.g., increasing the switching frequency [20] or operating in discontinuous conduction mode [5], these design questions are beyond the scope of this work.

C. Examining VSC behavior

One additional benefit of including the AC-side measurements, and consequently, better regulation of the DC voltage, is the opportunity to reduce the DC-link capacitor size without saturating the PWM converter.

For the simulations considered in this paper with grid-forming inverter control gains from [12], the saturation of the PWM converter was avoided in all cases examined. Fig. 9
shows both the DC voltage $V_{DC}$ and magnitude of the modulated AC-side voltage $||v_{AC}||$, for the case of $K_{pred} = 2$. The inner control loops of the grid-forming VSC respond on a faster timescale to reduce the magnitude of the AC modulated voltage and thereby, significantly reduce the risk of saturating the modulation index of the VSC. The outer control loops of the VSC then re-adjust the set points to restore the voltage to an acceptable operating level. While saturation was not an issue in this set up, it may be an issue for different parameterizations and/or disturbances.

V. CONCLUSION

This work focused on modeling and control of a BESS DC source grid forming VSC. On the modeling side the DC/DC inductor was observed to be the dominant component dictating the dynamical behavior. A 4th, 2nd, and 0th-order model of a BESS was examined and it was found that all three models were in agreement for the considered disturbances. For the DC/DC controller, it was found that the inclusion of readily available AC-side measurements into the DC/DC converter control loop could reduce DC voltage deviations by up to $\sim 10\%$ during large step changes, thereby potentially reducing the risk of premature failure of the DC-link capacitor. Future work will focus on the behavior of these controllers under asymmetrical grid faults, additional DC-source technologies as well as further consideration of how fast inner-control loops of the VSC which may help alleviate the potential for saturation of the VSC modulation index.

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APPENDIX

Table II lists the parameter values used for the DC-side model for simulations [18, 20].

| $f_{DC/DC}$ | $c_{DC}$ | $L_{DC}$ | $r_{t0}$ | $r_{t1}$ | $r_{t2}$ |
|-------------|----------|---------|--------|--------|--------|
| 3.2 kHz     | 2 mF     | 3 mH    | 1.5 mΩ | 95 mΩ  | 0.4 mΩ |
| $r_{t3}$    | $r_{t4}$ | $L_{t1}$ | $L_{t2}$ | $c_{t1}$ | $c_{t2}$ |
| 2.2 mΩ      | 0.55 mΩ | 35 nH   | 15 nH  | 0.55 F  | 22.7 kΩ |

Fig. 9: DC voltage and AC modulated voltage for $K_{pred} = 2$. |