Skyrmion Logic Clocked via Voltage Controlled Magnetic Anisotropy

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Magnetic skyrmions are exciting candidates for energy-efficient computing due to their non-volatility, detectability, and mobility. A recent proposal within the paradigm of reversible computing enables large-scale circuits composed of directly-cascaded skyrmion logic gates, but it is limited by the manufacturing difficulty and energy costs associated with the use of notches for skyrmion synchronization. To overcome these challenges, we therefore propose a skyrmion logic synchronized via modulation of voltage-controlled magnetic anisotropy (VCMA). In addition to demonstrating the principle of VCMA synchronization through micromagnetic simulations, we also quantify the impacts of current density, skyrmion velocity, and anisotropy barrier height on skyrmion motion. Further micromagnetic results demonstrate the feasibility of cascaded logic circuits in which VCMA synchronizers enable clocking and pipelining, illustrating a feasible pathway toward energy-efficient large-scale computing systems based on magnetic skyrmions.

I. INTRODUCTION

The non-volatility and rich physical interactions of magnetic skyrmions have inspired interest in their application to logical computing. Magnetic skyrmions are topologically-stable quasiparticles resulting from the Dzyaloshinskii-Moriya interaction (DMI)1 and can be propelled along a track via an applied current2,3. Their non-volatility, thermal stability, and energy-efficient motion have led to proposals for their use in racetrack memory systems4,5.

Several approaches for skyrmion logic have also been proposed, though the early work in this field did not provide a scalable technique for cascading logic gates without requiring external control, modulation, or amplification circuitry6–11. We therefore recently proposed a scalable paradigm for skyrmion logic based on reversible computing and conservative logic in which skyrmion logic gates can be directly cascaded without any external circuitry12.

Skyrmion synchronization is critical to the functionality of scalable skyrmion logic systems, as the key skyrmion-skyrmion interactions require the simultaneous arrival of skyrmions from different parts of the circuit. Given the differing lengths of the skyrmion tracks and the inevitable thermal-induced variations of skyrmion velocity, clocked synchronization elements must be included to ensure proper logical functionality. The proposed use of notch synchronizers12–14 constrict skyrmion motion such that at normal operating current densities, skyrmions are too large to fit through the constriction. The skyrmion logic system is clocked with periodic increases to the current density, causing the skyrmion radii to temporarily decrease and allow skyrmions to pass through the notch constrictions. However, these notch synchronizers are difficult to precisely manufacture and the high current densities lead to skyrmion annihilation and high power dissipation.

To circumvent the challenges of notch synchronizers, this paper proposes the clocking of skyrmion logic systems via voltage-controlled magnetic anisotropy (VCMA). By modulating VCMA within the skyrmion track15 skyrmions can be synchronized with less energy, higher reliability, and greater robustness to device imperfection. We illustrate the functionality of the proposed VCMA synchronizers through micromagnetic simulation, and quantify the anisotropy barrier needed to pin skyrmions as a function of current density and skyrmion velocity. Furthermore, we discuss fabrication approaches and demonstrate through micromagnetic simulation that these VCMA synchronizers can be integrated in large cascaded circuits with low power dissipation and high robustness.

II. SKYRMION LOGIC AND VCMA FUNDAMENTALS

The skyrmion logic system of Ref. 12 leverages the rich physics of magnetic skyrmions to perform logical operations. As skyrmion synchronization is critical to the operation of these logic gates, notch synchronizers were suggested to ensure the correct functionality of cascaded circuits. As this notch-based synchronization is both inefficient and error-prone, VCMA is an intriguing approach to efficiently pin skyrmions.

A. Skyrmion Kinetics

The skyrmion logic system of Ref. 12 utilizes four distinct skyrmion phenomena. As illustrated in Fig. 1(a), current injected in the +y direction through a ferromagnetic track creates a spin current in the +z direction via the spin-Hall effect. This spin current causes a first force that pushes the skyrmion in the +y direction16,17 y-directed skyrmion motion results in a −x-directed deviation from linear y-directed motion via a second force due to the skyrmion-Hall effect (SkHE)18 and is countered by the third force, edge repulsion, to prevent skyrmion annihilation. The fourth phenomenon is the skyrmion-skyrmion repulsion between two skyrmions in close proximity19.
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FIG. 1. VCMA synchronizer structure. (a) A Néel skyrmion (colored circle) exists at the interface between a heavy metal and a ferromagnet with polarization $P$. Injected electric current in the $+y$ direction ($I$) induces a spin current ($J_S$) in the $+z$ direction via the spin-Hall effect. This spin current produces a $+y$-directed spin-Hall force ($F_{SH}$), propelling the skyrmion in the $+y$ direction. Voltage applied to the electrode creates an electric field through the insulator that alters the magnetic anisotropy of the interface. (b) Synchronizer cross sections in the $yz$ and $xz$ planes.

B. Reversible Skyrmion Logic Gates

The skyrmion logic system of Ref. 12 enables a range of skyrmion logic gates and encodes binary ‘1’ and ‘0’ values through the presence or absence of a skyrmion, respectively. Constant injected current drives skyrmions along tracks towards logic gate junctions, where interplay between the skyrmion-Hall effect and skyrmion-skyrmion repulsion causes the skyrmion trajectories to depend on the binary states of the inputs. As illustrated by the example AND/OR gate of Supplemental Material Fig. S1 and Video S1, the logical outputs are encoded in the output tracks to which the skyrmions are driven.12

In these reversible skyrmion logic systems, all information is conserved, theoretically permitting energy dissipation below the Landauer limit. Relatedly, skyrmions are never destroyed and therefore need not be nucleated, as they can be indefinitely cascaded and reused.12 The final outputs of this skyrmion logic system can be read via magnetic tunnel junctions.15

C. Notch Synchronizer

Skyrmion logic gates are cascaded by using the output skyrmions from one gate as the input skyrmions of other gates. As the gates require skyrmion synchronization to ensure proper skyrmion-skyrmion repulsion within the junctions, Ref. 12 proposed a notch synchronizer between cascaded logic gates (Supplementary Material Fig. S2 and Video S2). The notch structure pins skyrmions when normal low current density is applied, as the skyrmion radius is too large. By periodically providing a larger current pulse, the skyrmion radii shrink such that they depin and pass through the constriction.

By placing multiple synchronizers in a skyrmion logic circuit, a global clocking current pulse can force the skyrmions to interact at the track junctions, thereby ensuring correct logical operation despite thermal variations in velocity and differing trajectory lengths. However, this large current pulse is energetically expensive and can cause rapid skyrmion acceleration that can lead to skyrmion annihilation. It is also difficult to fabricate the notch structure with sufficient precision to ensure proper synchronization, and it is therefore worthwhile to consider alternative approaches.

D. Voltage-Controlled Magnetic Anisotropy

VCMA is a technique for varying the uniaxial anisotropy of a magnetic material via an applied electric field. A voltage applied across the ferromagnetic track changes its electron density of states which, in turn, changes the perpendicular magnetic anisotropy and magnetic coercivity.16 The relationship between applied voltage and change in anisotropy is predominantly linear, following the expression $K_{uv} = K_u + \vartheta V_b$. Where $K_{uv}$ is the resultant anisotropy, $K_u$ is the original anisotropy, $V_b$ is the bias voltage, and $\vartheta$ is a material-dependent coefficient ranging for most materials between 20 $\mu$J/m$^2$ / V nm and 100 $\mu$J/m$^2$ / V nm for Fe/Vacuum and Fe/MgO interfaces respectively.17

When applied to the skyrmion track, VCMA can be used to pin a skyrmion via an anisotropy gradient.18 An applied positive voltage increases the anisotropy of the VCMA region which creates a positive energy barrier for a skyrmion entering the region and a negative energy barrier for a skyrmion leaving the region. For a negative voltage, the respective energy barriers are reversed.16 Skyrmions without sufficient driving force or velocity will be unable to pass, and will be pinned at the interface between the high and low anisotropy regions.

III. VCMA SYNCHRONIZER

We propose the synchronization of skyrmion logic systems by periodically switching skyrmion pinning via modulation of VCMA, enabling logic circuits that are more reliable and energy-efficient than can be achieved with notch synchronizers. These VCMA synchronizers can be readily fabricated
be fabricated using standard semiconductor processing techniques. Bottom electrodes and cobalt racetrack regions with different thicknesses \((t_1, t_2, t_3)\) can be created with metal deposition, electron-beam lithography/photolithography and Ar ion milling. Chemical-mechanical polishing can be used to ensure the smoothness of the skyrmion racetrack.

B. Operation

The operation of the VCMA skyrmion synchronizer is demonstrated in the micromagnetic simulation results of Fig. 2 and Video 1. A global electric current applied in the +y direction accelerates the skyrmion in the +y direction, though it is pinned by the VCMA region when a clock voltage of 0V is applied. At \(t = 0.9\) ns, a clock pulse of \(-6V\) temporarily lowers the anisotropy, depinning the skyrmion. By including numerous such VCMA regions controlled by the same global clock, skyrmions can be synchronized within large-scale cascaded skyrmion logic circuits to ensure proper skyrmion-skyrmion repulsion with the logic gates and correct logical functionality.

90% of the clock cycle remains at zero volts, which reduces the amount of leaked charge, improving static power dissipation. Additionally, as it pins skyrmions without applied voltage, the system preserves memory without power. As the VCMA synchronizer avoids the high current densities of the notch-based design, it is more dynamically power efficient. Further, as high current densities often destroy skyrmions, the VCMA synchronizer is also more reliable.

IV. VCMA SYNCHRONIZER ANALYSIS AND DESIGN

By quantifying the interaction between a moving skyrmion and the VCMA region, we can optimize the efficiency, accuracy, and speed of VCMA-clocked skyrmion logic systems. This analysis reveals that both the injected current and the velocity of the skyrmion contribute to the total effective driving force. Governed by the Thiele equation, this force determines whether a skyrmion can overcome a specified anisotropy barrier, and therefore is crucial for selecting the PMA of the VCMA region.

A. Anisotropy Barrier

The ability of skyrmions to traverse a VCMA region was evaluated as a function of current density and anisotropy. As shown in Fig. 3(a), skyrmions are unable to pass through regions of differing anisotropy unless sufficient current is provided. When the VCMA region anisotropy is higher than the remainder of the track, skyrmions are unable to overcome the anisotropy barrier to enter the VCMA region and are pinned outside; when the VCMA region anisotropy is lower than the remainder of the track, skyrmions enter the VCMA region but are unable to traverse the barrier to leave the VCMA region and are pinned inside.
FIG. 3. (a) Conditions under which a skyrmion in a region with anisotropy $K_a$ is able to traverse a region with anisotropy $K_{ab}$ are indicated with green circles, while skyrmions that get pinned outside the $K_{ab}$ region before entering and skyrmions that get pinned within the $K_{ab}$ region are indicated with red squares and triangles, respectively. Micromagnetic simulations were performed under a variety of current densities for skyrmions that started while both stationary and moving at terminal velocity. The blue square indicates the only condition under which the initial skyrmion velocity impacted the result; for this condition, the skyrmion that was initially stationary is pinned, while the skyrmion that is initially moving at its terminal velocity passes the anisotropy barrier. (b) The minimum anisotropy barrier required ($\Delta K_a$) to pin a skyrmion at a VCMA region for skyrmions moving at terminal velocity (blue squares) and for initially-stationary skyrmions (red circles) as a function of current density. (c) The contribution of velocity on the minimum pinning anisotropy as a function of velocity, computed via the difference in the minimum pinning anisotropies of moving and stationary skyrmions.

It is noteworthy that Fig. 3(a) is asymmetric about $K_{ab} = K_a$, as skyrmions with sufficient current are able to overcome larger energy barriers when leaving the VCMA region than when entering it. This is a result of the acceleration of the skyrmions as they propagate through the VCMA region, resulting in skyrmions attempting to leave the VCMA region with significantly greater velocity than when they entered the VCMA region.

This impact of velocity can be more directly observed when comparing the ability of stationary and moving skyrmions to traverse the VCMA region: all of the simulations in Fig. 3(a) were performed for both stationary skyrmions and skyrmions moving at their terminal velocity, and in one case the moving skyrmion is able to traverse the VCMA region whereas the initially stationary skyrmion is not.

B. Skyrmion Dynamics

To further analyze the impact of skyrmion velocity, skyrmions were accelerated along a racetrack to determine the minimum pinning magnetic anisotropy as a function of current density. As shown in Fig. 3(b), increases in current density necessitate larger anisotropy barriers to pin the skyrmions. Furthermore, skyrmions that enter the VCMA region with zero velocity are clearly observed to overcome less of an energy barrier than skyrmions that enter the VCMA region with their terminal velocity.

The impact of skyrmion velocity on the ability of a skyrmion to traverse an anisotropy barrier is further explored in Fig. 3(c). This difference in pinning anisotropy is quadratic with respect to velocity, and it represents the contribution of the skyrmion velocity to the minimum pinning anisotropy. The cause of this increase can better understood by analyzing the Thiele equation (1) and its solution (2):

$$G \times v - \alpha \hat{D}v + F = 0$$  \hspace{1cm} (1)

$$\begin{pmatrix} v_x \\ v_y \end{pmatrix} = \frac{1}{\alpha^2 D^2 + G^2} \begin{pmatrix} \alpha DF_x + F_y G \\ \alpha DF_y - F_x G \end{pmatrix}$$  \hspace{1cm} (2)

Comparing the steady state solution ($V = 0$) to the dynamic solution ($\hat{F}_s = 0$), there is a ratio between steady state velocity ($v_{ss}$) and dynamic velocity ($v_d$) equal to $1 + \frac{G^2}{\alpha^2 D^2}$. These differences in velocity can be accounted for with an additional
FIG. 5. VCMA synchronization of pipelined skyrmion logic circuits, with a constant current \(5 \times 10^{10} J/m^2\) injected in the \(+y\) direction. Clock waveforms are applied to the VCMA synchronizers in the (a) pipelined AND/OR gate and (b) pipelined one-bit full adder. Micromagnetic simulation results indicate the initial and final skyrmion states for the (c) pipelined AND/OR gate and (d) pipelined one-bit full adder, demonstrating proper logical operation.

The VCMA clocking can be used to synchronize the motion of all the skyrmions within a system, thereby enabling the proper functionality of large-scale cascaded circuits. To prove the ability of the proposed VCMA synchronizers to enable cascaded logic gates, their functionality has been demonstrated in pipelined AND/OR and full adder circuits via micromagnetic simulation.

A. Pipelined AND/OR Gate

The effectiveness of the VCMA synchronizers can be demonstrated by adding pipelining to the simple AND/OR logic gate of Supplemental Material Fig. S1. As shown in Fig. 5(a), 5(c), and Video 2, the skyrmions can be made to advance past one VCMA region during each 2 ns clock cycle, thereby providing the synchronization necessary for proper repulsion within the AND/OR gate junction. The logic gate has a throughput of one computation per clock cycle of both the AND and OR functions, and thus correctly performs computations for all four AND/OR conditions during this 8 ns simulation.

B. Pipelined One-Bit Full Adder

To ensure the proper functionality of cascaded skyrmion logic gates, it is critical that the skyrmions entering each logic gate junction are synchronized. As shown in Fig. 5(b), 5(d), and Video 3, the careful addition of VCMA synchronizers to
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a one-bit full adder circuit ensures proper skyrmion-skyrmion interactions despite the differing lengths of the skyrmion trajectories. In particular, the VCMA synchronizers are placed such that the skyrmions arrive contemporaneously at the logic gate junctions. Like the pipelined AND/OR gate, this full adder circuit therefore produces a throughput of one full addition computation (Sum and C_{out}) per clock cycle (5 ns). As there are two VCMA synchronizers within the full adder computation path, the latency of this full adder is two clock cycles (10 ns).

VI. CONCLUSION

Reversible skyrmion logic provides a potential route to compute with less energy dissipation than Landauer’s limit to the minimum energy for computation. In light of the importance of skyrmion synchronization to ensure proper skyrmion-skyrmion interactions within the logic gate junctions, this paper proposes skyrmion synchronization using VCMA modulation. We demonstrate the functionality and analyze the behavior of these VCMA synchronizers via micromagnetic simulation, providing a deeper understanding of their behavior that enables large-scale cascaded skyrmion circuit design. The use of VCMA synchronizers provides a reduced error rate and requires less energy than can be achieved with notch synchronizers[12] thereby greatly advancing the prospects for reversible computing with magnetic skyrmions.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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