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A 2.1 GHz, 210 µW, −189 dBC/Hz DCO with Ultra Low Power DCC Scheme

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Abstract: This article presents a low power digital controlled oscillator (DCO) with an ultra low power duty cycle correction (DCC) scheme. The DCO with the complementary cross-coupled topology uses the controllable tail resistor to improve the tail current efficiency. A robust duty cycle correction (DCC) scheme is introduced to replace self-biased inverters to save power further. The proposed DCO is implemented in a Semiconductor Manufacturing International Corporation (SMIC) 40 nm CMOS process. The measured phase noise at room temperature is −115 dBC/Hz at 1 MHz offset with a dissipation of 210 µW at an oscillating frequency of 2.12 GHz, and the resulting figure-of-merit is s −189 dBC/Hz.

Keywords: DCO; DCC; ultra low power

1. Introduction

The power consumption and the phase noise of a digital controlled oscillator (DCO) determine the digital phase locked loops (DPLL) performance. The trend towards low power design of DPLL [1–5] is driven by the requirements of the low power and low cost communication systems, therefore the low power design of DCOs appeared.

Several approaches to save power consumption of integrated oscillators have attracted favors from both industry and academia. On the whole, there are two main methods to reduce power consumption—improvement of current efficiency and improvement of voltage efficiency. The Class-C LC oscillator [6–10] is the typical topology for improving current efficiency. Compared with traditional Class-B oscillators, Class-C topologies exploit currents in operating transistors and enlarge the first harmonic of the currents. However, the Class-C topologies need start-up circuits to start the oscillating and put the differential pair into Class-C operation [11–14] which increase the difficulty of designing and extra power consumption. Moreover, the LC oscillator with a LC tail filter [15,16] is the structure for improving voltage current. The harmonic frequency of the LC tail filter is twice the frequency of oscillating and the output amplitude can be enhanced without extra current. In other words, if the voltage amplitude is fixed, then the current consumption is saved. Nevertheless, this structure suffers drawbacks of low frequency range and extra area of inductors. Another topology with transformers [2] can also improve the voltage efficiency. But this circuit suffers the difficulty of transformers.

In addition to the above structures, a topology that saves power without a complex structure is introduced, as in Figure 1. The complementary cross-coupled topology reuses the bias current and limits the output amplitude. The bias current is provided by a tail resistor [17]. Compared to Class-C oscillators, current efficiency can be improved by increasing the resistance of R, and no start-up problem occurs.
It is worth mentioning that, as \( R \) increases, the peak level of \( V_P \) and \( V_N \) decrease and the duty cycle problem of the output signal is serious. For the double data rate (DDR) systems and half/quarter-rate serial link transceivers, the duty cycle of the clock signals must be 50% accurately. Hence, a duty cycle correction (DCC) is necessary for the DCO. From previous studies [18–22], wide frequency range and high precision designs are introduced. Nevertheless, their structures are complicated and the power consumptions are high. A simple approach can be carried out by self-biased inverters (as in Figure 1). However, the power consumption of the self-biased inverters are significant, as well, and the coupling capacitors provide heavy loads to the DCO.

Based on the problem mentioned above, this letter proposes an ultra low power DCC scheme for a low power complementary cross-coupled DCO.

2. DCO with Ultra Low Power DCC Scheme

2.1. Conceptual Architecture

The main objective of this study is to design a duty cycle correction scheme for a low power DCO to replace the self-biased inverter and to obtain lower power consumption in the overall design. Since the tail resistor in Figure 1 is changeable, a possible solution to compensate the output duty cycle deviation of the DCO is to add another changeable bottom tail resistor in which resistance can be adaptively adjusted to a suitable value according to the duty cycle. Therefore, it is necessary to create a negative feedback loop. Figure 2 shows the conceptual diagram of the proposed DCC scheme. The duty cycle of the output signals \( V_{OUTP} \) and \( V_{OUTN} \) are monitored by a duty cycle detector in which output signal \( V_D \) is compared with a reference voltage \( V_{REF} \). \( V_D \) is then sent to be connected to a voltage-controlled tail resistor to ensure that the duty cycle is maintained at 50%.

As \( R \) changes, if the duty cycle is higher than 50%, the DCC loop would decrease the resistance of \( R_{VC} \); if the duty cycle is lower than 50%, the loop would increase the resistance of \( R_{VC} \). Enough closed loop gain would ensure a high accuracy of duty cycle correction against process, voltage, and temperature (PVT) variation.
2.2. Circuit Implementation

The goal is to design a DCC scheme with an ultra low power and high accuracy. Therefore, the negative feedback should use simple circuit structure (low power purpose) and provide high enough loop gain (high accuracy purpose).

Figure 3 presents the circuit implementation of the proposed DCO with an ultra low power DCC scheme. Compared with Figure 2, the DCC loop includes three main stages: a duty cycle detector, a comparator, and a voltage controlled resistor.

The duty cycle detector consists just two resistors \( R_1 \) and \( R_2 \). Since signals \( V_{OUTP} \) and \( V_{OUTN} \) have the same DC component and totally opposite AC components, the duty cycle detector \( R_1 \) and \( R_2 \) can extract DC level at \( V_B \) without any filter because the AC components are canceled at \( V_B \). To avoid signals \( V_{OUTP} \) and \( V_{OUTN} \) disturbing each other, the resistance of \( R_1 \) and \( R_2 \) should large enough (say 100 kΩ).
The comparator is implemented by an operational amplifier (OA). The structure is shown, as in Figure 4. The gain of the OA is relaxed. However, the power consumption is significant in the DCC loop. Therefore, it is not necessary to use a complex topology to boost the gain and the current flows can be saved in the simple structure (just including two current flows). Moreover, small aspect ratios of transistors would save power further and 1 μm/6 μm and 2 μm/6 μm of W/L are chosen for NMOS and PMOS, respectively.

![Figure 4. Structure of low power operational amplifier.](image)

The voltage controlled resistor can be easily employed by a NMOS tail transistor $M_1$. The $R_{ON}$ of $M_1$ is controlled by the output signal $V_B$ of the OA. Since $M_1$ reuses the current flowing in the tail resistor $R$, there is no extra power consumption from $M_1$.

The accuracy of the $V_{REF}$ must be guaranteed for a high accurate DCC scheme. Since the goal of a DCC scheme is 50% duty cycle, $V_{REF}$ should be $V_{DD}/2$. Therefore, a low-power, high-accurate voltage divider is required. A resistive divider may be a suitable choice, but it requires a large area to provide enough resistance to save power. Hence, we use two identical PMOS transistors with small aspect ratios to implement the voltage divider as shown in Figure 3. Since the substrate nodes of the PMOS transistors can be connected to the source nodes and the electrical environment of each PMOS $M_2$ and $M_3$ is the same, this structure can produce an accurate $V_{DD}/2$.

Finally, we add two MOS capacitors $M_4$ and $M_5$ to filter the noise from $R$ (thermal noise) and $M_1$ (flicker noise and thermal noise).

2.3. DCC Loop Analysis

As mentioned above, the DCC scheme is a negative feedback loop. To ensure a high accurate calibration of duty cycle, the loop gain should be large enough. Thus, the stability of the multi-pole system must be adjusted carefully.

To reduce the complexity of analysis, we simplify the DCC loop, as in Figure 5. Since the AC components of oscillating signals have no influence on the DCC loop, the LC tank can be ignored. Two inverter chains are simplified as one chain to provide DC component. Furthermore, the tail resistor $R$ and two pairs of cross coupled transistors are treated as equivalent resistors $R_{eq1}$ and $R_{eq2}$.

![Figure 5. Equivalent circuit of proposed DCC loop.](image)
The equivalent circuit clearly shows that there are three contributors to the loop gain: the inverter chain, OA and the common source amplifier (consisting of \(M_1\), \(R_{eq1}\) and \(R_{eq2}\)). Since the inverter chain can provide a large enough DC gain, the OA gain in the loop is not as significant as mentioned above, which is the reason why a complex structure is not needed to boost the OA gain. Although the large DC gain is generated by the inverter chain, the output impedance of the inverter is small due to the small gate length. In addition, the parasitic capacitances at \(V_3\) and \(V_D\) are small and can be neglected. Therefore, the poles from the inverter are far from the origin and have negligible effect on the stability of the loop.

Because of large load capacitor (noise filtering capacitor \(M_5\)) at \(V_1\) and large output impedance of the OA at \(V_B\), the DCC loop can be treated as a second order system. To ensure the stability of the loop, we carry out the Miller compensation by adding a miller capacitor \(C_C\) and nulling resistor \(R_Z\) connecting between \(V_B\) and \(V_1\).

To analyze this system, the closed loop can be broken at \(V_D\), as in Figure 6.

![Figure 6. Open loop circuit of proposed DCC loop.](image)

The open loop transfer function (from \(V_{REF}\) to \(V_{D2}\)) is:

\[
G(s) = \frac{V_{D2}}{V_{REF}} = -A_{inv} \times \frac{R_{eq1}}{R_{eq1} + R_{eq2}} \times \frac{g_{m1} r_o (R_{eq1} + R_{eq2}) (g_m1 - (R_Z + (sC_C)^{-1})^{-1})}{C_{MS} C_C r_o (R_{eq1} + R_{eq2}) s^2 + g_m1 C_C r_o (R_{eq1} + R_{eq2}) s + 1} \tag{1}
\]

where \(A_{inv}\) is the DC gain of the inverter chain, \(g_m\) is the transconductance of the input transistors of the OA, \(r_o\) is the output impedance of the OA, \(g_m1\) is the transconductance of the tail transistor \(M_1\), and \(C_{MS}\) is the capacitance of the noise filtering capacitor \(M_5\).

Then, the closed loop transfer function is as follows:

\[
H(s) = \frac{G(s)}{G(s) - 1}. \tag{2}
\]

The dominant pole \(p_1\), the highest nondominant pole \(p_2\) and the zero in the open loop can be easily obtained as Equations (3)–(5).

\[
p_1 = -\frac{1}{r_o (R_{eq1} + R_{eq2}) g_{m1} C_C}, \tag{3}
\]

\[
p_2 = -\frac{g_{m1}}{C_{M5}}, \tag{4}
\]

\[
z = -\frac{1}{R_Z - C_C / g_{m1}}. \tag{5}
\]

According to Equations (3) and (4), the distance of \(p_1\) and \(p_2\) are moved away from each other by Miller effect and that improves the stability of the loop.

In order to eliminate the influence of zero, the zero can be moved to infinity by adjusting the nulling resistor as Equation (6).
\[ R_Z = \frac{C_C}{S_{in1}} \]  

(6)

To verify the stability of the DCC loop, a post-layout transient simulation is carried out, as in Figure 7.

Figure 7 shows that the DCO starts to oscillate (\(V_{OUTP}\) in Figure 7) at about 0.6 \(\mu\)s after powering up. Then, the DCC circuit starts to calibrate the duty cycle of the output signals and the calibration finished at about 2.75 \(\mu\)s. According to the shapes of signal \(V_B\) and \(V_D\), it indicates that the DCC loop is a underdamping system which verifies the stability of the loop.

3. DCC Accuracy, Power Consumption and Phase Noise

3.1. DCC Accuracy

In order to verify the high accuracy and the robustness of the DCC scheme among the process variation, transient simulations with different process corners are carried out, as in Figure 8. The results indicates that the accuracy is 50 ± 0.6%.

Figure 8. DCC accuracy among different process corners.

To display the function of the DCC scheme visually, the comparison between the DCO without and with the DCC scheme is presented, as in Figure 9.
Figure 9. Transient simulation results for duty cycle: (a) without DCC scheme; (b) with DCC scheme.

3.2. Power Consumption and Phase Noise

As analyzed in [23–25], the tail current have both influence on the power consumption and the phase noise of a DCO. A trade-off between these two parameters always appears which means lower power results in larger phase noise. Hence, to find a specific value of tail current which has the highest efficiency, the relation of power and phase noise should be considered carefully. According to [26], a normalized figure of merit (FoM) is introduced to demonstrate the trade-off:

\[
\text{FoM} = L(f_{\text{offset}}) - 20\log\left(\frac{f_0}{f_{\text{offset}}}\right) + 10\log\left(\frac{P_{\text{DCO}}}{1 \text{ mW}}\right),
\]

where \(L(f_{\text{offset}})\) is the phase noise of the oscillation carrier, \(f_{\text{offset}}\) is the offset frequency from the oscillation carrier, \(f_0\) is the center frequency of the oscillation carrier, and \(P_{\text{DCO}}\) is the power consumption of the DCO. The lower value of FoM means the higher efficiency of current consumption. The tail resistor in Figures 1 and 3 are designated to be changeable for the search of the lowest FoM.

Although the proposed topology has the lower power DCC scheme, the extra circuit (such as the OA and voltage divider) would contribute extra phase noise through the tail transistor \(M_1\). The simulations are performed to reveal the phase noise (at 1 MHz offset) in the tail current for the purpose of observing this phenomenon as shown in Figure 10.

Figure 10 can be broken into two regions. If the tail current is large enough (Region II),

It is worth mentioning that the results in Figure 10 of conventional circuit (in Figure 1) are not from results in [17] because values of inductance, capacitances, and transistor sizes are not the same with the proposed application. Therefore, to make a fair comparison, we re-design the conventional circuit. Since this re-design has not been fabricated, the comparison between the conventional and the proposed circuits is based on simulation results.

Figure 10 can be broken into two regions. If the tail current is large enough (Region II),
the DCC circuit would have seriously negative influence on the phase noise performance of the proposed DCO. However, two lines are closed with each other which illustrates that if the tail current is small enough (Region I), the extra noise is not a significant trouble for low power design. FoMs against the tail current in two topologies presents in Figure 11. It is seen that the proposed circuit has lower FoM. We can conclude that the proposed DCC scheme saves much power by costing little performance of noise.

![Comparison of figure of merit (FoM) against tail current.](image)

Figure 11. Comparison of figure of merit (FoM) against tail current.

Tables 1 and 2 list the power dissipation for the two designs at a tail current of 152 µA, respectively. The DCC scheme only consumes 4.3% of the total power of the circuit, while the self-biased inverter consumes 34%. It is worth mentioning that the inverter used for self-biased inverter is a standard cell with W/L of transistor sizes of 1.22 µm/40 nm for PMOS and 520 nm/40 nm for NMOS, respectively.

| Table 1. Power break-down of the proposed DCO. |
|-----------------------------------------------|
| DCO | DCC Scheme | Total |
| Power (µW) | 201 | 9 | 210 |

| Table 2. Power break-down of the traditional DCO. |
|-----------------------------------------------|
| DCO | Self-Biased Inverters | Total |
| Power (µW) | 204 | 103 | 307 |

4. Measurement Results

The proposed DCO is fabricated in 40 nm CMOS technology and the chip micrograph is shown, as in Figure 12. The area of the chip is 590 × 320 µm². The chip measurement setup is shown, as in Figure 13. A Rohde & Schwarz FSW50 signal and spectrum analyzer was used to test the phase noise of the DCO, as shown in Figure 14. When the proposed circuit is oscillating at 2.12 GHz, the measured phase noise is −115 dBc/Hz at a 1 MHz offset. In addition, the measured power dissipation is 210 µW, and the calculated FoM value is −189 dBc/Hz, which is close to the simulation results in Section 3.2.
Figure 12. Chip micro-photo.

Figure 13. Measurement setup.

Figure 14. Measurement result of phase noise.
Table 3 shows the results of this study compared with the results of previous LC oscillators. The DCO achieves good current efficiency while achieving ultra-low power dissipation.

Some discussions should be mentioned as following. Although, the VCO in [13] needs additional blocks to provide bias voltages for Class-C structure, the extra digital control circuits powers down when the calibration is done, so the extra power consumption can be ignored. Moreover, the design in [14] also needs an operational amplifier to finish Class-C operation, however, the extra power dissipation is just 0.18 mW which can also be neglected. Therefore, the additional blocks’ power in [13,14] do not have much influence on the calculation of FoM in Table 3.

Table 3. Performance comparison.

| Tech. (nm) | Freq. (GHz) | Tuning Range (%) | Phase Noise (dBc/Hz) | Power (mW) | FoM (dBc/Hz) |
|------------|-------------|------------------|----------------------|------------|--------------|
| This work  | 40          | 2.12             | −115 @ 1 MHz         | 0.21       | −189         |
| [10]       | 130         | 2.4              | −130 @ 1 MHz         | 7.3        | −189         |
| [13]       | 130         | 2.45             | −132 @ 2.5 MHz       | 2.5        | −188         |
| [14]       | 180         | 2.55             | −123 @ 1 MHz         | 1.28       | −190         |
| [24]       | 250         | 2.12             | −118 @ 0.6 MHz       | 2.25       | −185         |
| [25]       | 90          | 2.55             | 46.2                 | 156 @ 20 MHz | 22.8         | −188         |

5. Conclusions

This paper proposes a low-power DCO with an ultra-low-power DCC scheme. The DCO based on complementary cross-coupled topology with a controllable tail resistor to improve the efficiency of tail current. A robust DCC scheme is introduced to replace the self-biased inverter for further power savings. After careful design, the presented DCO is highly suitable for low power digital phase-locked loops.

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