Retraction

Retraction: Reduced Switch Count Multilevel Inverter with Fault Diagnosis Operation (J. Phys.: Conf. Ser. 1916 012100)

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This article (and all articles in the proceedings volume relating to the same conference) has been retracted by IOP Publishing following an extensive investigation in line with the COPE guidelines. This investigation has uncovered evidence of systematic manipulation of the publication process and considerable citation manipulation.

IOP Publishing respectfully requests that readers consider all work within this volume potentially unreliable, as the volume has not been through a credible peer review process.

IOP Publishing regrets that our usual quality checks did not identify these issues before publication, and have since put additional measures in place to try to prevent these issues from reoccurring. IOP Publishing wishes to credit anonymous whistleblowers and the Problematic Paper Screener [1] for bringing some of the above issues to our attention, prompting us to investigate further.

[1] Cabanac G, Labbé C and Magazinov A 2021 arXiv:2107.06751v1

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Reduced Switch Count Multilevel Inverter with Fault Diagnosis Operation

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Abstract. This paper proposes a reduced switch count multilevel inverter with fault diagnosis operation to overcome the problem of a higher number of switches in a multilevel inverter and fault detection in a multilevel inverter. A multilevel inverter is a power electronic device with low switching losses and low total harmonic distortion that is used in high voltage and high power applications (THD). In a standard inverter, it’s often used to minimise the size and number of passive filters. The H-bridge topology is needed for the proposed model of reduced switch count multilevel inverter (RSC-MLI). It is used to achieve higher power ratings as well as to promote the use of renewable energy sources. It reduces switching errors and the number of power electronic switches, cost and lower order harmonics. As the number of levels and steps in the waveform increase, the harmonics in the output voltage waveform decrease, resulting in an ideal waveform that looks like a sinusoidal waveform, which reduces the harmonics at the output. Switching losses and power losses can be minimised by using a limited number of switches.

1. Introduction

Power electronic devices known as inverters transform DC voltage to AC voltage at a particular frequency. Inverters are used to control the speed of AC motors and link renewable energy sources to the electrical grid. An ideal inverter produces sinusoidal voltage at its output terminals. Obtaining sinusoidal voltage with greater efficiency, on the other hand, is extremely difficult. It has issues such as high harmonic content, increased switching tension, more dv/dt, and higher losses while switching. To solve these problems, voltage waveforms stepped at different stages, resembling a staircase at the inverter's output, have developed, and these inverters are known as Multi Level Inverters (MLI). Low distortions, lower losses, low dv/dt and minimal common mode voltage are all advantages of MLIs.

MLIs are found applications in the field of industrial drives, photovoltaic systems, induction furnace, HVDC and FACTS. Total harmonic distortion (THD) should be zero for each inverter (including multi-level) [1]. A multi-level cascaded inverter achieves high output current and voltage power ratings by reducing total harmonic distortion, electromagnetic compatibility (EMC), and switching stress on devices. As the number of levels increases, the voltage output approaches a sinusoidal signal, minimising harmonic distortion. The classification of multilevel inverters is shown in Figure 1. The three types of multilevel inverters are diode clamped multilevel inverters, flying capacitor multilevel inverters, and cascaded H bridge (CHB) multilevel inverters. Separate DC sources are required for CHB MLIs, whereas a common DC source can be used for diode clamped and flying capacitor MLIs. The CHB – MLI structure tends to be the most specific of the three topologies [2].
These MLIs use various arrangements of power semiconductor switches and voltage sources of capacitors to synthesise the output signal for a better harmonic band [3]. Figure 2 shows how the number of levels are incorporated to obtain a sinusoidal signal of close in nature. The output form takes on the shape of a sine wave as the stepped structure increases in the output voltage. This reduces filtering function, as well as the access that comes with it.

Multilevel inverters, despite their benefits, necessitate a greater number of power switches and DC voltage sources. The number of power switches needed by the cascaded MLI structure is one of its major drawbacks [4]. This paper proposes a new topology based on the H-bridge for reducing the switch count of multilevel inverters. The fault diagnosis method for the proposed system is also addressed, in categorise the fault as open circuit or short circuit fault. This model is intended for use with a seven-level inverter. The results of simulating the multilevel inverter method with MATLAB Simulink are shown in the following pages.

2. Cascaded Multilevel Inverter
Series connected H-Bridge inverters are called cascaded inverters. The layout of a cascaded multilevel inverter is shown in figure 3. In each H bridge, an isolated DC source serve as input. The output of a five level CHB multilevel inverter is Vdc, 2Vdc, 0, -Vdc, and -2Vdc with two series connected H
bridge structures. For a seven level inverter, the output voltage levels with three H bridge is \( V_{dc} \), \( 2V_{dc} \), \( 3V_{dc} \), 0, \( -V_{dc} \), \( -2V_{dc} \), \( -3V_{dc} \). In general, the levels in the output side is computed from the expression,

\[
V_{\text{out}} = (2N + 1)
\]

\( N \) = Number of H Bridge

Figure 3 shows a single phase CHB MLI and the associated staircase waveform. The semiconductor switches are turned on in a sequence in order to produce the output.

Figure 3. Structure of cascaded H-Bridge MLI

3. Proposed topology for reduced switch count multilevel inverter

The proposed topology decreases the number of switches and DC voltage sources as compared to current topologies. In this paper, we present a 7-level multilevel inverter with a revised H-Bridge topology [5]. The block diagram of the conceptual scheme is shown in Figure 4. The DC voltage supply is fed into the configured RSC – MLI. It converts DC voltage into a stepped output waveform that looks like a sine wave.

Figure 4. Block diagram
The switch fault identification is done using signal processing techniques. It is used to monitor the circuit and detect, if any open circuit or short circuit fault happens in the switches [6].

3.1 Reduced Switch Count Multilevel Inverter (RSC-MLI)

Figure 5 depicts the schematic model of a multilevel inverter with revamped H-bridges with a 7-level reduced switch count. There are ten switching devices and three voltage sources in this system. By adding two power switches and a dc source for each level, the circuit could be extended for different output waveform levels. Table 1 displays the switching scheme of a 7-level multilevel inverter [7].

![Proposed model of reduced MLI](image)

**Table 1.** Switching scheme for a 7 – level multilevel inverter

| S.No | S1 | S3 | S5 | Output voltage |
|------|----|----|----|----------------|
| 1    | 1  | 0  | 0  | V1             |
| 2    | 0  | 1  | 0  | V2             |
| 3    | 0  | 0  | 1  | V3             |
| 4    | 1  | 1  | 0  | V1 + V2        |
| 5    | 1  | 0  | 1  | V1 + V3        |
| 6    | 0  | 1  | 1  | V2 + V3        |
| 7    | 1  | 1  | 1  | V1 + V2 + V3   |
3.2 Switch fault identification
In the circuit several cases of fault may occur, specifically fault in the power transistor or fault in the power transistor driver or triggering circuit. The fault may be of two types – open circuit fault or short circuit fault. In this proposed method, the faulty switch is identified using the H-Bridge output voltage. Since the waveform of output currents varies in the presence of open circuit faults, it cannot be taken for identification [8].

![Figure 6](image1.jpg)  ![Figure 7](image2.jpg)

**Figure 6.** Non-linear phase load currents  **Figure 7.** Harmonic current identification

Because of the non-linear loads, harmonic currents are produced in the circuit, as shown in figure 6. Figure 7 illustrates how these harmonic currents are described. PWM control methods are used to control the shunt active filter. The PI regulator is fed the difference between the identified harmonic current and the active filter current. This generates a reference signal, which is compared to the 600-shifted carrier wave to produce the transistor control signals. Figure 9 shows how to identify defective switch currents [9].

![Figure 8](image3.jpg)

**Figure 8.** Reference signals and carriers of PWM control techniques
Figure 9. Bridge output voltage in open faulty condition

4. Simulation and results
The proposed model of 7-level RSC MLI is simulated in Simulink platform in MATLAB, and THD analysis is also performed using the FFT spectral analysis of MATLAB Simulink. The given inverter model is rated for RL loads of 100Ω and 50H, with a dc voltage of 10 volts for each. Figures 10 and 11 show the simulation model of the circuit and the switching circuit built in MATLAB Simulink [10]. The proposed topology is unique in that it emphasises reducing the number of power switches. Three DC voltage sources are used to generate seven output levels in the proposed topology. The sinusoidal PWM technique produces pulses with a triangular frequency of 5 kHz.

Figure 10. Switching circuit of RSC-MLI

Figure 11. Simulation circuit of 7 level RSC-MLI

The output waveform and complete harmonic distortion (THD) obtained from the MATLAB simulation are shown in Figure 8. When there is no fault at the power switches, the output voltage waveform is found to have seven stages (without fault condition). Simulink also analyses Total harmonic distortion (THD) using the FFT (Fast Fourier Transform) spectrum. The findings of the THD study are also shown in figure 12.
Figures 12 and 14 show the output waveforms from the reduced switch count multilevel inverter (RSC MLI) without and with fault conditions, respectively. Any fault in the switches, as seen in the diagram, has a direct impact on the output voltage levels.

**Figure 12. Output and THD of RSC MLI**

**Figure 13. Output of Proposed work without switch fault**

**Figure 14. Output of Proposed work with switch S1 fault (Only 5 level)**
5. Conclusion

MATLAB Simulink was used to model and simulate the proposed 7-level reduced switch count multilevel inverter. Existing cascaded multilevel inverters were compared to the proposed model. Based on the contrast, it was discovered that the proposed inverter design needs fewer switches, has lower THD, and performs better than the traditional design. The inverter increases the level with the fewest possible switches, lowering the overall cost and resulting in a high output voltage. This study proposes a seven-level cascaded multilevel inverter with fault detection, and the outputs are tested. It generates a high-voltage sinusoidal waveform. Furthermore, the faulty switch is easily identified. It boosts productivity.

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