A CMOS Ku-band receiver chain for phased array system

Zhengdong Jiang, Chenxi Zhao, Xiaoning Zhang, Weiqiang Lu, Yiming Yu, Huihua Liu, Yunqiu Wu, and Kai Kang

University of Electronic Science and Technology of China, 2006 Xiyuan Road, Gaoxin Western District, Chengdu 611731, P. R. China
a) kangkai@uestc.edu.cn

Abstract: A Ku-band receiver chain for phased array system is presented in this paper. It is composed of three LNAs, a 4-bit attenuator and a 5-bit phase shifter. This design is fabricated in 180-nm standard CMOS with a chip area of 3 mm × 0.8 mm. The measured peak gain is 21 dB at 16.5 GHz and the minimum NF is 6.7 dB at 16 GHz. The 5-bit phase shifter realizes a shift range of 0°–360°. The tested minimum RMS phase error and gain error of the system are 2.1° and 0.46 dB. The 4-bit attenuator provides a gain tuning range of 15 dB with 1-dB step. The minimum RMS phase shift error and amplitude error are 2.7° and 0.24 dB.

Keywords: CMOS receiver, LNA, attenuator, phase shifter

Classification: Microwave and millimeter-wave devices, circuits, and modules

References

[1] X. Zhang, et al.: “A Ku band 4-element phased array transceiver in 180nm CMOS,” IEEE MTT-S International Microwave Symposium (IMS) (2017) 1595 (DOI: 10.1109/MWSYM.2017.8058938).
[2] D. Shin, et al.: “A high-power packaged four-element, X-band phased-array transmitter in 0.13-μm CMOS for radar and communication systems,” IEEE Trans. Microw. Theory Techn. 61 (2013) 3060 (DOI: 10.1109/TMTT.2013.2271488).
[3] S.-J. Huang, et al.: “A fully-integrated 77 GHz phase-array radar system with 1TX/4RX frontend and digital beamforming technique,” IEEE Symposium on VLSI Circuits (2013) C294.
[4] H. Krishnaswamy and H. Hashemi: “A 4-channel 24–27 GHz UWB phased array transmitter in 0.13 μm CMOS for vehicular radar,” IEEE Custom Integrated Circuits Conference (2007) 753 (DOI: 10.1109/CICC.2007.4405839).
[5] M. Sayginer, et al.: “An eight-element 2–16 GHz programmable phased array receiver with one, two, or four simultaneous beams in SiGe BiCMOS,” IEEE Trans. Microw. Theory Techn. 64 (2016) 4585 (DOI: 10.1109/TMTT.2016.2620144).
[6] S. Kim, et al.: “A 76–84-GHz 16-element phased-array receiver with a chip-level built-in self-test system,” IEEE Trans. Microw. Theory Techn. 61 (2013) 3083 (DOI: 10.1109/TMTT.2013.2265016).
[7] K. Koh and G. M. Rebeiz: “An X- and Ku-band 8-element phased-array
receiver in 0.18-μm SiGe BiCMOS technology,” IEEE J. Solid-State Circuits 43 (2008) 1360 (DOI: 10.1109/JSSC.2008.922737).

[8] D.-W. Kang, et al.: “Single and four-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control,” IEEE Trans. Microw. Theory Techn. 57 (2009) 3534 (DOI: 10.1109/TMTT.2009.2033302).

[9] Z. Jiang, et al.: “A 24 GHz enhanced neutralized cascode LNA with 4.7 dB NF and 19.8 dB gain,” IEICE Electron. Express 15 (2018) 20180464 (DOI: 10.1587/elex.15.20180464).

[10] L. Zhang, et al.: “A CMOS K-band 6-bit attenuator with low phase imbalance for phased array applications,” IEEE Access 5 (2017) 19657 (DOI: 10.1109/ACCESS.2017.2750203).

[11] K.-J. Koh and G. Rebeiz: “A Q-band four-element phased-array front-end receiver with integrated Wilkinson power combiners in 0.18-μm SiGe BiCMOS technology,” IEEE Trans. Microw. Theory Techn. 56 (2008) 2046 (DOI: 10.1109/TMTT.2008.2002239).

1 Introduction

Recently, phased array systems on silicon based processings have attracted attention, because of its wide applications in the X/Ku band [1, 2] and the 24 GHz/77 GHz automotive radars [3, 4]. As the development of the 5G communication system, the phased array system is considered as a potential technique for its beamforming and scanning capability, which can improve working distances to support high-data-rate and high-frequency communication. Compared with III–V processes, phased array system on SiGe and CMOS can integrate RF front-ends to digital and analog circuits to improve system integration.

In [5, 6], the variable gain amplifier (VGA) is used to adjust the gain. However, the gain range of them is limited, which is smaller than 10 dB. A high-gain receiver chain is presented in [7], which has a NF of 4.2 dB at maximum gain state, but the linearity of it is poor. In [8], the receiver chain consists of a LNA/VGA and a phase shifter. It has good linearity but the NF is beyond 9 dB.

In this paper, a receiver chain for phased array is proposed. To achieve a good balance between NF and linearity, the multi-stage LNA is divided into three small LNA cells (LNA1, LNA2 and LNA3) and the attenuator and phase shifter are allocated between them. The neutralized capacitors are adopted in the attenuator to reduce the phase shift. The circuit design and measurement results are introduced as follows.

2 Circuit design

A. System analysis

The system-level simulation results of the three diagrams in Fig. 1 are discussed on gain, NF and power compression. System A consists of a high-gain LNA, a passive phase shifter and attenuator. It realizes the lowest NF thanks to the high-gain LNA. However, the power compression performance is sacrificed simultaneously. The VGA is adopted in system B and replaces the attenuator. The system B has the best IP1dB, but the NF is the worst. The system C is implemented in the proposed
design, in which the amplifiers are divided into three and two of them are arranged after the attenuator and phase shifter. Thus, it can keep a good balance between the NF and linearity.

B. LNA design

The schematics of the three LNAs are shown in Fig. 2. In the first stage of each LNA cell, the cross-coupled common gate (CCCG) stage is utilized. In the second state, the cascode topology is implemented to provide a high gain [9]. A T-type matching network is used at the output of the LNA for a broad band impedance matching. In LNA1, it consists of two inductors and a capacitor. In LNA2 and LNA3, two inductors are combined together as a transformer to save the chip area. After all, the LNA1 achieve a gain of 18.5 dB and a NF of 3.3 dB. The LNA2 achieves a gain of 16.7 dB and a NF of 3.7 dB the same as LNA3.

C. 4-bit attenuator and 5-bit phase shifter design

The 4-bit attenuator is based on the T-type and π-type attenuators as shown in Fig. 3(a). The T type topology is implemented in the 1, 2 and 4 dB attenuators. Besides, the π-type topology is used in the 8 dB attenuator because it can realize more attenuation with two signal paths to the ground [10]. In both structures, the NMOS transistors are used as switches to change the signal path between the series and shunt branches to realize the expected attenuation states. Due to the difference
of the drain-to-source parasitic capacitance between the on- and off-state transistors, there is a transmission phase shift between reference and attenuation states.

To reduce the phase shift, neutralized capacitors, as \( C_1 \) and \( C_2 \) shown in Fig. 3(a), are added to neutralize the phase shift. The added capacitor and the resistor in the shunt branch can compose a low-pass filter to lag the transmission phase. It can make the transmission phase of attenuation state close to that of reference state in a frequency band as shown in Fig. 3(b). For the T-type attenuator, the transmission phase of attenuation state with neutralized capacitor can be described as

\[
\theta = -\tan^{-1} \left( \frac{2Z_0C_1R_1 + C_1R_1^2 - 2C_{\text{off}}R_1^2}{Z_0 + R_1} \right),
\]

where \( C_{\text{off}} \) is the parasitic capacitor of the transistor \( M_2 \). Fig. 3(c) shows the phase shift compared with the reference state. Without neutralized capacitors, the phase shift between the reference and attenuation states (red line) is 1.27° to 2.04° from 15 to 18 GHz. With neutralized capacitors of 150 fF (green line), the phase shift is reduced to −0.46° to +0.34°.

To improve the linearity, a 5-bit passive phase shifter based on switched LC networks is adopted as shown in Fig. 4. Low pass LC and all pass networks controlled by NMOS switches are applied to realize the three phase delay states of

---

Fig. 3. (a) The schematic of the differential 4-bit attenuator. (b) The transmission phase with different neutralized capacitors of 4-dB attenuator. (c) The phase shift without and with different neutralized capacitors compared with the reference state.

Fig. 4. The schematic of the phase shifter.
11.25°, 22.5° and 45°. The 90° phase delay cell is comprised of two 45° units. As for the 180° state, it is realized by a double-throw double-pole switch.

3 Measurement results

Fig. 5 shows the microphotograph of this work. It is fabricated by standard 180 nm bulk CMOS with a chip area of 3000 um x 800 um (2.4 mm²) including the test pads. The chip area of LNA2 or LNA3 is 300 um x 480 um (0.144 mm²), which is only half size of LNA1.

Fig. 6 shows the measured S-parameter results of the proposed receiver chain. The measured $S_{11}$ is below $-11$ dB from 15 GHz to 18 GHz and the measured $S_{22}$ is below $-14.7$ dB from 15 GHz to 18 GHz. The peak measured small signal gain ($S_{21}$) is 21.3 dB at 16.5 GHz. The measured 3 dB gain bandwidth is 2.4 GHz ranging from 15.4 GHz to 17.8 GHz. The smallest measured NF is 6.7 dB at 16.2 GHz and it is smaller than 8.5 dB from 15 GHz to 18 GHz.

Fig. 7(a) shows the measured $S_{21}$ at the reference state and 15 attenuation states from 15 GHz to 18 GHz. The attenuation is from 0–15 dB by 1 dB step. In Fig. 7(b), the measured RMS phase shift error and RMS attenuation error are displayed to represent the accuracy of the attenuator. The measured RMS phase shift error is below 4.7° and the minimum point is 2.7° at 16.5 GHz. The measured...
RMS attenuation error is smaller than 0.61 dB and the least value is 0.24 dB at 16.3 GHz.

Fig. 8(a) shows the measured relative insertion phases of 31 states compared with the reference (0°). This receiver channel realizes a 0–360° phase range by 11.25°. In Fig. 8(b), the measured RMS phase error and RMS gain error are displayed. The measured RMS phase error is minimum 2.1° at 15.9 GHz and maximum 6° at 15 GHz. In addition, the measured RMS gain error is minimum 0.46 dB at 16 GHz and maximum 0.8 dB at 18 GHz.

Table I compares the performance of the proposed receiver chain with other state-of-art designs. This design has advantages on the NF, RMS phase error and RMS gain error compared with [5] and [11] and it has better linearity than [7].

![Fig. 8. (a) The insertion phase of 32 states of phase shifter. (b) The RMS phase error and RMS gain error.](image)

| Ref. | This work | [5] | [7] | [11] |
|------|-----------|----|----|----|
| Tech. (nm) | 180 CMOS | 130 SiGe | 180 SiGe | 180 BiCMOS |
| Freq. (GHz) | 15–18 | 2–16 | 6–18 | 30–50 |
| Gain (dB) | >15 | 8–12 | 8–21 | ≤12 |
| NF (dB) | 6.7–8.5 | 11.5 | 4.2–12.5 | 12.5–14 |
| Gain bits | 4 | 3 | - | - |
| Phase bits | 5 | 4 | 4 | 4 |
| RMS phase error (°) | 2.1–6 | <8.5 | <5.7 | ≤8.7 |
| RMS gain error (dB) | 0.46–0.8 | <1 | <0.9 | ≤1.2 |
| IP1dB (dBm) | −18 | −17 | −28 | −13.8 |

4 Conclusion

A Ku-band receiver chain comprised of three LNAs, a 4-bit attenuator and 5-bit phase shifter in 180-nm bulk CMOS is proposed. The neutralized capacitors are employed to reduce the phase shift between reference state and attenuation state. After all, this receiver chain achieves a peak gain of 21.3 dB with a gain range of 15 dB and a NF of 6.7 dB. The RMS phase error and gain error of the system are 2.1° to 6° and 0.46 dB to 0.8 dB. The RMS phase shift and attenuation error are 2.7° to 4.7° and 0.24 dB to 0.61 dB.

Acknowledgments

This work is supported by National Natural Science Foundation of China (Grant No. 61331006, 61771115).