Comparative Study of 2SiC&4Si Hybrid Configuration Schemes in ANPC Inverter

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ABSTRACT Compared with traditional silicon (Si) power devices, silicon carbide (SiC) devices have attracted extensive attention due to their excellent characteristics. In recent years, the manufacturing process of SiC devices has become more mature, but the cost is still high. Therefore, replacing only some of the Si devices with SiC devices in a topology is a better choice to achieve higher system efficiency while considering costs. This paper studies the hybrid configuration schemes consisting of two SiC devices and four Si devices (2SiC&4Si) in ANPC three-level inverter. Two hybrid 2SiC&4Si topologies are proposed. In order to make full use of the low switching loss characteristics of SiC devices in hybrid topologies, specific modulation strategies are applied to concentrate switching losses on SiC devices. Based on the 2SiC&4Si hybrid ANPC topologies, three efficient SiC&Si hybrid configuration schemes are derived. In this paper, the theoretical comparison and experimental verification of the efficiency and loss distribution of the three hybrid schemes are carried out.

INDEX TERMS SiC&Si hybrid configuration, ANPC, loss analysis.

I. INTRODUCTION

Three level topologies are widely used in medium and high power class photovoltaic (PV) inverters. Neutral point clamped (NPC) is one of the most common three-level topologies. Compared with two-level inverters, output voltage harmonic content of three-level inverters is low, and each power device only bears half of the bus voltage. Its main disadvantage is the uneven loss distribution of power devices during operating process [1]. In heat dissipation design, the highest loss of all the power devices is taken as standard, so the loss imbalance will increase the requirements of heat sink, which is not conducive to improving power density. To solve this problem, Professor T. Bruckner from the German University of Science and Technology first proposed active neutral point clamped (ANPC) three-level topology at the IEEE-PESC conference in 2001 [2]. It introduces active switches to replace the clamp diodes in NPC topology. In a particular current flow direction, the load current has two flow paths to output 0 state. Because of these redundant current paths, the PWM control of ANPC topology becomes more flexible. In this way, the current flow paths can be reasonably selected to achieve device loss balance. In fact, loss balance is not the main reason why ANPC are suitable for power converters. With the rapid development of semiconductor technology, power devices for different applications have been produced. These power devices have different on-characteristics and switching characteristics, which can better match the requirements of different positions in ANPC topology. In this way, the total loss can be reduced and efficiency can be improved, which is the main reason for the application of ANPC topology today.

However, a major problem of ANPC topology is that it includes six switching devices that are costly compared to commonly used three-level topologies such as NPC and T type topologies. High power density is one of the current development trends of PV inverters, and the application of wide-bandgap semiconductors such as silicon carbide (SiC)
devices is becoming more widespread. However, for cost considerations, it is difficult to implement full SiC devices in an ANPC topology. If only replacing some Si devices with SiC devices, the efficiency and power density can be improved while controlling costs. A number of papers have been proposed for that SiC&Si hybrid applications. In [3], A Si CSI (current source inverter)/SiC VSI (voltage source inverter) series inverter system is proposed. In this paper, the VSI operates at high frequencies to eliminate harmonic distortion caused by CSI. Due to the high frequency operating characteristics of the VSI, its main losses are switching losses, so switching losses are greatly reduced by the application of SiC MOSFETs. In 2016, Jiangbiao He proposed a fault-tolerant T-T structure multi-level three-phase inverter [4], in which SiC MOSFETs are only used in the redundant bridge arms. By the early switching of SiC MOSFETs in redundant bridge arms, devices in main loop can achieve ZVS and ZCS to reduce switching loss. In [5], a hybrid SiC&Si based T-type converter is proposed. In this topology, the two devices connected to the bus bar are subjected to a large blocking voltage, so the switching loss is larger. By replacing the two devices with SiC MOSFETs while the other devices still use traditional Si devices, the efficiency can be increase by 66%. Due to the diversity modulations of ANPC topology, many SiC&Si hybrid configuration schemes have been proposed [6]–[10]. In [6], [7], four high frequency switches are replaced with SiC MOSFETs to reduce switching losses. In [8]–[10], only two Si MOSFETs are used to reduce switching losses. All of the above schemes take advantage of the low switching loss characteristics of SiC MOSFETs by replacing devices under high frequency switching with SiC MOSFETs to reduce loss.

However, the above papers only describe specific schemes, but the method for SiC&Si hybrid configuration is not systematically explained, which is not conducive to expanding SiC&Si hybrid configuration in other topologies. Considering the cost of SiC MOSFET, using two SiC MOSFETs and four Si IGBTs (2SiC&4Si) in an ANPC topology is the most cost-effective solution. This paper studies the 2SiC&4Si hybrid configuration schemes of ANPC three-level inverter. Based on the commutation characteristics of the ANPC topology and the low characteristics of the SiC MOSFET, two 2SiC&4Si hybrid topologies are proposed. By applying specific modulation strategies to concentrate switching loss on Si devices, the efficiency and power density can be improved while controlling costs. A number of papers have been proposed for that SiC&Si hybrid applications. In [3], A Si CSI (current source inverter)/SiC VSI (voltage source inverter) series inverter system is proposed. In this paper, the VSI operates at high frequencies to eliminate harmonic distortion caused by CSI. However, the above papers only describe specific schemes, but the method for SiC&Si hybrid configuration is not systematically explained, which is not conducive to expanding SiC&Si hybrid configuration in other topologies.

II. SiC&Si HYBRID CONFIGURATION METHOD IN ANPC TOPOLOGY

A. COMMUTATION CHARACTERISTICS OF ANPC TOPOLOGY

The ANPC topology is developed on the basis of NPC topology, as shown in Fig.1. It replaces the two clamp diodes of NPC topology with active switches. The switching status of ANPC topology are shown in Table 1. As shown in Table 1, there are three O status: OU (current flows through the upper arm); OUL (current flows through the upper and lower arms); OL (current flows through the lower arm). In this section, we take the switching between P and O as an example to analyze the three commutation processes.

Suppose the direction of current flowing into the load is positive. When the load current is positive, T1 and T2 are on in the P state. Load current flows through T1 and T2, and Vdc/2 is the output voltage. Vdc is the DC bus voltage. When the P state switches to the OU state, T1 turns off, while T5 does not turn on yet. This stage is called dead time. During this stage, anti-parallel diode D5 of T5 naturally turns on, and the current continues to flow through D5 and T2. When entering the OU state, T5 turns on, current flows into the load through D5 and T2, and outputs zero voltage, as shown in Fig.2. When the load current is negative, it flows through D1 and D2. In dead time, the load current still flows through D1 and D2. When entering the OU state, T5 turns on, current flows into the load through D2 and T5, as shown in Fig.3.

When the load current is positive, the high-frequency switching loss is concentrated on T1; the anti-parallel diode D5 has reverse recovery loss. When the load current is

![FIGURE 1. ANPC topology.](image-url)

| TABLE 1. Switching status of ANPC topology. |
|-------------------------------------------|
| Output status | T1 | T2 | T3 | T4 | T5 | T6 | Output voltage |
|---------------|----|----|----|----|----|----|----------------|
| P             | 1  | 1  | 0  | 0  | 0  | 0/1| +Vdc/2         |
| OU            | 0  | 1  | 0  | 0/1| 1  | 0  | 0              |
| OUL           | 0  | 1  | 0  | 0  | 1  | 0  | 0              |
| OL            | 0/1| 0  | 1  | 0  | 0  | 1  | 0              |
| N             | 0  | 0  | 1  | 1  | 0/1| 0  | −Vdc/2         |
negative, the high-frequency switching loss is concentrated on T5; the anti-parallel diode D1 has reverse recovery loss.

When the load current is positive, T1 turns off when the P state switches to the OUL state. Then enters dead time. At this time, there are two freewheeling loops: half of the current flows into load through the anti-parallel diodes D5 and T2, and the other half flows through the anti-parallel diode D3 and T6. When entering the OUL state, T3 and T5 zero voltage turn on, and the current through two parallel loops: D5 and T2, T6 and D3. As shown in Fig.4. When the load current is negative, T1 zero voltage turns off when the P state switches to the OUL state. Then enters dead time. The current continues to flow through the anti-parallel diode D3 and T6, and enters dead time. Although T1 is on during dead time, no current flows through it. When entering the OUL state, T3 and T5 turn on, current flows through T6 and D3, output the OUL state. As shown in Fig.5.

When the load current is positive, switching loss concentrate on T1, and there are reverse recovery losses on D3 and D5. When the load current is negative, switching loss concentrate on T3 and T5, and there are reverse recovery losses on D1.

When the load current is positive, T2 turns off when the P state and the OL state switches. At this time, T3 does not turn on yet. The current continues to flow through the anti-parallel diode D3 and T6, and enters dead time. When entering the OL state, T3 turns on, current flows through T6 and D3, output the OL state. As shown in Fig.6. When the load current is negative, T2 zero voltage turns off when the P state and OL state switches. The current continues to flow through the anti-parallel diode D1 and D2, and enters dead time. When entering O state, T3 zero voltage turns on, current flows through D6 and T3, output the OL state. As shown in Fig.7.

The distribution of switching losses in different commutation modes is shown in Table 2. We respectively call these three commutation modes SPWM1, SPWM2 and SPWM3 modulations. Since the power factor of PV inverter is required to be no less than 0.95, the following analysis is carried out under unit power factor. Under unit factor, there are only two devices suffering from high frequency switching losses under the three modulations. The high frequency switching losses of SPWM1 and SPWM2 are concentrated on T1/D1 and T4/D4. The high frequency switching loss of SPWM3 is concentrated on T2/D2 and T3/D3.
B. DEVICE SELECTION AND LOSS CHARACTERISTICS COMPARISON

A single-phase independent inverter experiment platform with a DC-side voltage of 1000V and a power rating of 3.3kW is built. Therefore, 1200V SiC MOSFETs (C2M0080120D) and Si IGBTs (FGH25T120SMD) are selected.

1) POWER DEVICE SWITCHING LOSS

The switching loss data of IGBT and MOSFET from manuals at 25°C are compared, as shown in Fig.8. The abscissa represents the current flowing through the power device: the current flowing through IGBT is $I_c$; the current flowing through MOSFET is $I_s$. Although test conditions of the two curves are slightly different, it is obvious that the switching loss of SiC MOSFET is much smaller than that of Si IGBT. That is to say, SiC MOSFET has great advantages in high frequency applications.

2) POWER DEVICE AND ITS ANTI-PARALLEL DIODE ON-STATE LOSS

Due to the synchronous rectification characteristics of MOSFET, the on-state loss of its body diode is not considered here. We only compare the on-state losses of IGBT (25°C $V_{GE}$=15V) and its anti-parallel diode and MOSFET (25°C $V_{GS}$=20V), as shown in Fig.9. It can be seen that when the current is below 20A, the on-state loss of the MOSFET is the smallest, and the on-state loss of the anti-parallel diode of IGBT is the largest.

3) REVERSE RECOVERY LOSS OF ANTI-PARALLEL DIODE

The reverse recovery loss of the diode is proportional to its reverse recovery charge. It can be seen from Table 3 that the reverse recovery loss of MOSFET anti-parallel diode is lower.

C. 2SI&C&4SI HYBRID CONFIGURATION SCHEMES FOR ANPC TOPOLOGY

It can be seen from the above analysis that switching loss is concentrated on T1/T4 or T2/T3 under unit power factor. Therefore, these devices can be replaced by SiC MOSFETs.

There are two configuration topologies, as shown in Fig.10. In hybrid topology A, T1 and T4 are replaced by SiC MOSFET. While in hybrid topology B, T2 and T3 are replaced by SiC MOSFET. SPWM1 or SPWM2 modulation is used in hybrid topology A, and SPWM3 modulation is used in hybrid topology B to concentrate switching losses on SiC devices, thereby reducing switching losses.

III. MODULATION AND LOSS ANALYSIS OF HYBRID TOPOLOGY

A. MODULATION ANALYSIS

1) HYBRID TOPOLOGY A

In hybrid topology A, T1 and T4 are replaced with SiC MOSFETs, and the remaining four switches still use Si IGBTs, as shown in Fig.10 (a). In order to concentrate the high frequency switching loss on SiC MOSFETs, SPWM1 or SPWM2 can be used, and the driving signals are shown in Fig.11. Taking the case where the load current is positive for example, in SPWM1 modulation, although T5 and T6 are also driven by high frequency signals, the antiparallel diodes of the two switches are freewheeling in dead time, so T5 and T6 are zero voltage switches. In SPWM2 modulation,
all switching switches have high frequency drive signals, but only T1 and T4 have switching losses. When the load current is positive, T2 and T6 are always on, and there is no switching loss. T3 and T5 are zero voltage switches, because freewheeling current flows through their anti-parallel diodes during dead time.

2) HYBRID TOPOLOGY B
In hybrid topology B, T2 and T3 are replaced with SiC MOSFETs, and the remaining four switches still use Si IGBTs, as shown in Fig.10 (b). In order to concentrate the high frequency switching loss on T2 and T3, SPWM3 can be used, and the driving signal is shown in Fig.12. Under this modulation, switching losses are concentrated only on T2 and T3.

B. LOSS ANALYSIS
1) POWER DEVICE MODELING
In order to analyze the advantages and disadvantages of the hybrid schemes, the efficiency can be simulated by loss modeling. Usually in power devices manuals, manufacturers give the main parameter characteristics under typical junction temperature, according to which the loss model of the power devices can be established. According to the output characteristic curves, the on-state losses of IGBT, MOSFET and diode can be expressed as

\[
P_{\text{CON}} = \begin{cases} 
P_{\text{CON,IGBT}} = I(\alpha)V_{ce} + I(\alpha)^2R_{ce} \\
P_{\text{CON,MOSFET}} = I(\alpha)^2R_{ds} \\
P_{\text{CON,DIODE}} = I(\alpha)V_f + I(\alpha)^2R_f 
\end{cases}
\]

\(I(\alpha)\) is the current flowing through switches, \(V_{ce}\) is the initial saturation voltage drop of IGBT; \(R_{ce}\) is the on-state resistance of IGBT; \(R_{ds}\) is the on-state resistance of MOSFET; \(V_f\) is the initial on-state voltage of diode, and \(R_f\) is the on-state resistance of diode.

The switching losses of IGBTs and MOSFETs can be expressed as

\[
P_{\text{sw}} = \begin{cases} 
P_{\text{sw,IGBT}} = E_{\text{IGBT,SW}}(I, T, U_{DC}) \times f_s \\
P_{\text{sw,MOSFET}} = E_{\text{MOSFET,SW}}(I, T, U_{DC}) \times f_s 
\end{cases}
\]

\(E_{\text{IGBT,SW}}(I, T, U_{DC})\) and \(E_{\text{MOSFET,SW}}(I, T, U_{DC})\) represent the energy values per unit switching cycle of IGBT and MOSFET as a function of current temperature and bus voltage.

The reverse recovery loss of a diode can be expressed as

\[
P_{\text{D,REC}} = E_{\text{D,REC}}(I, T, U_{DC}) \times f_s
\]

\(E_{\text{D,REC}}(I, T, U_{DC})\) represents the reverse recovery energy value per unit switching period of diode as a function of current temperature and bus voltage.

2) LOSS MODELING OF HYBRID TOPOLOGY A&SPWM1
Taking the unit power factor as an example, the loss calculation formula of 2SiC&4Si hybrid ANPC topology A under SPWM1 modulation is derived. Since the upper and lower arms are symmetrical, only the loss of T1, T2 and T5 are analyzed. Where T1 is a SiC MOSFET and T2 and T5 are Si IGBTs.

T1 performs high-frequency switching with the switching of P and OU states in positive half cycle, and there is high-frequency switching loss. In P state, there is current flow through T1 and T1 has conduction loss. T1 is off during negative half cycle of on-state loss

\[
P_{\text{CON,T1}}^{\text{on}} = \frac{1}{2\pi} \int_{0}^{\pi} P_{\text{CON,MOS}} \times D(\alpha) d\alpha
\]

\[
P_{\text{sw,T1}}^{\text{on}} = \frac{1}{2\pi} \int_{0}^{\pi} P_{\text{SW,MOS}} d\alpha
\]

\(\alpha\) is the load current phase angle, \(D(\alpha)\) is the duty cycle, \(T_{\text{dead}}\) is the dead time, and is the unit switching period.

T2 is constantly conducting during positive half cycle, and there is always current flowing through T2. During the negative half cycle, T2 is off. Therefore, T2 has only a positive half cycle of on-state loss

\[
P_{\text{CON,T2}}^{\text{on}} = \frac{1}{2\pi} \int_{0}^{\pi} P_{\text{CON,IGBT}} d\alpha
\]
During positive half cycle, T5 is high frequency ZVS switching. The zero voltage soft switching loss is small, so it is ignored in calculation. Current flow through the anti-parallel diode D5 during OU state and dead time. The on-state loss and reverse recovery loss of D5 are

\[ P_{\text{con,D5}}^{\text{pwm1}} = \frac{1}{2\pi} \int_0^\pi P_{\text{CON,DIODE}} \times (1 - D(\alpha)) d\alpha \]  

\[ P_{\text{rec,D5}}^{\text{pwm1}} = \frac{1}{2\pi} \int_0^\pi P_{\text{D,REC}} d\alpha \]  

3) LOSS MODELING OF HYBRID TOPOLOGY A&SPWM2

Taking the unit power factor as an example, the loss calculation formula of 2SiC&4Si hybrid ANPC topology A under SPWM2 modulation is derived. Since the upper and lower arms are symmetrical, only the loss of T1, T2 and T5 are analyzed. Where T1 is a SiC MOSFET and T2 and T5 are Si IGBTs.

T1 is high frequency switching in the positive half cycle, there are both switching loss and on-state loss. It is off in the negative half cycle. The on-state loss and switching loss of T1 are expressed as

\[ P_{\text{con,T1}}^{\text{pwmN}} = \frac{1}{2\pi} \int_0^\pi P_{\text{CON,MOS}} \times D(\alpha) d\alpha \]  

\[ P_{\text{sw,T1}}^{\text{pwmN}} = \frac{1}{2\pi} \int_0^\pi P_{\text{SW,MOS}} d\alpha \]  

T2 is constantly conducting during positive half cycle, and current always flows through it. In the negative half cycle, the load current flows through two parallel circuits during OUL state and dead time, the current flowing through T2 in OUL state and dead time is half of the load current. In the negative half cycle, T2 ZVS turns on, ignoring this soft switching loss.

\[ P_{\text{con,T2}}^{\text{pwmN}} = \frac{1}{2\pi} \left( \int_0^\pi P_{\text{CON,IGBT}} \times D(\alpha) d\alpha \right) \]  

\[ + \int_0^\pi P_{\text{CON,IGBT,OO}} \times (1 - D(\alpha)) d\alpha \]  

\[ P_{\text{CON,IGBT,OO}} = \frac{I(\alpha)}{2} V_{ce} + \frac{I(\alpha)^2}{4} R_{ce} \]  

In negative half cycle, half of the load current flows through D2 during OUL state and dead time. On-state loss and reverse recovery loss of D2 are

\[ P_{\text{con,D2}}^{\text{pwmN}} = \frac{1}{2\pi} \int_\pi^{2\pi} |P_{\text{CON,DIODE,OO}}| \times (1 - |D(\alpha)|) d\alpha \]  

\[ P_{\text{diode,OO}} = V_f + \frac{I(\alpha)}{2} R_f \]  

\[ P_{\text{rec,D2}}^{\text{pwmN}} = \frac{1}{2\pi} \int_\pi^{2\pi} |P_{\text{D,REC,OO}}| d\alpha \]  

4) LOSS MODELING OF HYBRID TOPOLOGY B&SPWM3

Taking the unit power factor as an example, the loss calculation formula of 2SiC&4Si hybrid ANPC topology B under SPWM3 modulation is derived. Since the upper and lower arms are symmetrical, only the loss of T1, T2 and T5 are analyzed. Where T2 is a SiC MOSFET and T1 and T5 are Si IGBTs.

T1 is constantly on during positive half cycle, current flows through T1 only in the P state. The on-state loss of T1 can be expressed as

\[ P_{\text{con,T1}}^{\text{pwm2}} = \frac{1}{2\pi} \int_0^\pi P_{\text{CON,IGBT}} \times D(\alpha) d\alpha \]  

T2 is high frequency switching during P and O states in the positive half cycle, and in the negative half cycle T2 is zero voltage soft switching. In P and O state of negative half cycle, T2 is on, and there is on-state loss. The on-state loss and switching loss of T2 are expressed as

\[ P_{\text{con,T2}}^{\text{pwm2}} = \frac{1}{2\pi} \left( \int_0^\pi P_{\text{CON,MOSFET}} \times D(\alpha) d\alpha \right) \]  

\[ + \int_0^\pi |P_{\text{CON,MOSFET}}| \times (1 - |D(\alpha)|) d\alpha \]  

\[ P_{\text{sw,T2}}^{\text{pwm2}} = \frac{1}{2\pi} \int_0^\pi P_{\text{MOSFET,SW}} d\alpha \]  

During dead time of the negative half cycle, there is free-wheeling current flowing through anti-parallel diode D2. The reverse recovery loss of D2 is

\[ P_{\text{rec,D2}}^{\text{pwm2}} = \frac{1}{2\pi} \int_\pi^{2\pi} |P_{\text{D,REC}}| d\alpha \]  

T5 is constantly on during the negative half cycle, but current flows only in O state and dead time. The on-state loss of T5 can be expressed as

\[ P_{\text{con,T5}}^{\text{pwm2}} = \frac{1}{2\pi} \int_\pi^{2\pi} P_{\text{CON,IGBT}} \times (1 - D(\alpha)) d\alpha \]
5) THEORETICAL ANALYSIS RESULTS OF THREE SCHEMES

Loss models are established based on the above formulas. The bus voltage is 1000V, switching frequency is 16 kHz, output power is 3.3kW, and the inverter is operating under unit power factor. Loss distribution of each devices in the upper half arms of ANPC under the three schemes is obtained. Fig.13 shows the loss distribution of the upper half bridge arms of the hybrid topology A under SPWM1 modulation. In this scheme, the switching losses are only on T1 (SiC MOSFET) and the ratio is small. The main loss is the on-state loss on T2, followed by the on-state loss of the anti-parallel diode D5. Fig.14 shows the loss distribution of the upper half bridge arms of the hybrid topology A under SPWM2 modulation. In this scheme, the switching losses are only on T1 (SiC MOSFET) and the ratio is small. The main loss is the on-state loss on T2, followed by the on-state loss on D2 and D5. Fig.15 shows the loss distribution of the upper half bridge arms of the hybrid topology B under SPWM3 modulation. In this scheme, the switching loss are only on T2 (SiC MOSFET) and the ratio is small. The main loss is the on-state loss at T1.

Fig.16 shows the efficiency curves of the three hybrid schemes, all SiC and all Si schemes under SPWM2 and SPWM3 at different power levels with the rated power of 3.3 kW. It can be seen that the efficiency of the two all SiC schemes is ahead of other schemes, and the efficiency of SPWM2 modulation is the highest. This is due to the fact that the parallel loop characteristic of SPWM2 modulation reduces the on-state loss. Then are the hybrid topologies. Among them, the hybrid topology B&SPWM3 scheme has the highest efficiency, followed by the hybrid topology A&SPWM2, and the lowest efficiency is the hybrid topology A&SPWM1. This is because the high-frequency switching losses of the three hybrid schemes are all concentrated on the two SiC MOSFETs, so the switching losses are same, the difference is only in the on-state losses. It can be seen from Fig.9 that under the same current level (less than 20A), the on-state loss of MOSFET is the smallest, followed by IGBT, and the anti-parallel diode of IGBT has the highest on-state loss. The current of the hybrid topology B&SPWM3 scheme under the unit power factor does not flow through the...
TABLE 4. Experimental platform parameters.

| Parameter          | Value       |
|--------------------|-------------|
| Rated power $P_e$  | 3.3kW       |
| Bus voltage $U_{dc}$ | 1000V      |
| Operating frequency $f_s$ | 16kHz     |
| Load Resistance $R$   | 40 $\Omega$ |
| Filter inductor $L$   | 0.9mH       |
| Filter capacitor $C$  | 200uF       |
| DC side capacitor $C_{dc}$ | 4700uF*2  |

anti-parallel diode, so the total on-state loss is minimal. The on-state loss of the hybrid topology $A$&SPWM1 scheme and the hybrid topology $A$&SPWM2 scheme differs only in the on-state loss of the $O$ state. In the OUL state of the hybrid topology $A$&SPWM2, the current passes through two parallel loops, which is lower than the on-state loss through one loop, so the on-state loss is smaller. The all-Si scheme has the lowest efficiency, and the efficiency of SPWM2 modulation is slightly higher.

IV. EXPERIMENT

A single-phase independent inverter ANPC platform is built for experiment. The main circuit is built with four types ANPC topologies of all SiC, all Si, hybrid topology A, and hybrid topology B. Except for the device configuration, the remaining configurations are identical. Si IGBTs and SiC MOSFETs are chosen the FGH25T120SMD and C2M0080120D discrete units in To247 package. Considering that the Si IGBT operating frequency in the all Si platform should not be too high, the switching frequency should be 16k. The platform parameters are shown in Table 4. The efficiency of hybrid topology $A$&SPWM1, hybrid topology $A$&SPWM2, hybrid topology $B$&SPWM3, full SiC topology & SPWM2, full SiC topology & SPWM3, all Si topology & SPWM2 and all Si topology & SPWM3 efficiency are tested. The photograph of the experimental platform is shown in Fig.17.

Fig.18-20 show the driving waveforms of SPWM1, SPWM2 and SPWM3 respectively. Fig.21 shows the efficiency curves of each scheme under different power levels, including the two all SiC schemes, three hybrid schemes and two all Si schemes. Among the three hybrid schemes, the hybrid topology $B$&SPWM3 scheme has the highest efficiency, followed by the hybrid topology $A$&SPWM2, and the lowest efficiency is the hybrid topology $A$&SPWM1, which is consistent with the theoretical analysis results. And the efficiency of the hybrid topology $B$&SPWM3 scheme and the hybrid topology $A$&SPWM2 scheme after 0.6$P_e$ is comparable to that of the full SiC&SPWM3. In all SiC scheme, the all SiC&SPWM2 scheme is the most efficient. The all SiC&SPWM3 scheme is less efficient after 0.4$P_e$ than the hybrid topology $B$&SPWM3 and hybrid topology.
TABLE 5. Efficiency comparison of each scheme at 10% 30% 50% 80%.

| efficiency | scheme | 0.1Pe | 0.3Pe | 0.5Pe | 0.8Pe |
|------------|--------|-------|-------|-------|-------|
| 1          | hybrid topology A&SPWM2 | 0.9864 | 0.9894 | 0.9884 | 0.9865 |
| 2          | hybrid topology B&SPWM3 | 0.9878 | 0.9903 | 0.9896 | 0.9885 |
| 3          | all Si&SPWM2 | 0.9900 | 0.9914 | 0.9907 | 0.9888 |
| 4          | all SiC&4Si | 0.9943 | 0.9942 | 0.9928 | 0.9899 |
| 5          | all Si&C&SPWM2 | 0.9929 | 0.9926 | 0.9902 | 0.9880 |
| 6          | all Si &SPWM2 | 0.9769 | 0.9812 | 0.9810 | 0.9801 |
| 7          | all Si &SPWM3 | 0.9754 | 0.9806 | 0.9802 | 0.9790 |

A&SPWM2. The efficiency values of typical power points for each scheme are shown in Table 5.

In the three hybrid schemes, the switching losses are all concentrated on SiC devices, which can fully utilize the low switching loss characteristics of SiC MOSFET. The loss difference of the three hybrid schemes is mainly found in on-state losses of SiC MOSFETs, Si IGBTs, and Si diodes. For the device selected in this paper and the power level of the platform, the on-state loss is the smallest when using SiC MOSFET. In the hybrid topology B&SPWM3 scheme, the load current mainly flows through the SiC MOSFET, so this scheme is the most efficient. The hybrid topology A&SPWM2 scheme can also greatly reduce the on-state losses due to the current flowing through the parallel loop in the zero state. The above two hybrid schemes have superior efficiency advantages over the full Si&SPWM3 scheme at high power, and the efficiency can be improved by about 1% compared with the full Si&SPWM3 scheme.

V. CONCLUSION

In this paper, the 2SiC&4Si hybrid configuration schemes of ANPC three-level converter is studied. Three cost-effective 2SiC&4Si hybrid configuration schemes are carried out with specific analysis and experimental verification. The hybrid topology B&SPWM3 scheme has the highest efficiency for the devices selected in this paper and the platform power level. At high power (greater than 0.6Pe), the efficiency of the hybrid topology A&SPWM2 scheme is comparable. The above two hybrid schemes have superior efficiency advantages over the full Si&SPWM3 scheme at high power (greater than 0.4Pe) and can increase efficiency by about 1% compared to the all Si&SPWM3 scheme.

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