A Compression-Compilation Framework for On-mobile Real-time BERT Applications

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Abstract

Transformer-based deep learning models have increasingly demonstrated high accuracy on many natural language processing (NLP) tasks. In this paper, we propose a compression-compilation co-design framework that can guarantee the identified model to meet both resource and real-time specifications of mobile devices. Our framework applies a compiler-aware neural architecture optimization method (CANAO), which can generate the optimal compressed model that balances both accuracy and latency. We are able to achieve up to 7.8× speedup compared with TensorFlow-Lite with only minor accuracy loss. We present two types of BERT applications on mobile devices: Question Answering (QA) and Text Generation. Both can be executed in real-time with latency as low as 45ms. Videos for demonstrating the framework can be found on https://www.youtube.com/watch?v=WIRvK_2PZI

1 Introduction

Pre-trained large-scale language models such as BERT [Devlin et al., 2018], XLNet [Yang et al., 2019], RoBERTa [Liu et al., 2019], and GPT-2 [Radford et al., 2019] have substantially advanced the state-of-the-art across a wide spectrum of NLP tasks. With the increasing popularity of mobile AI applications and the concerns of information security and privacy, it is desirable to deploy these well-trained models on edge devices, and furthermore, to meet real-time requirements. However, these models often consist of hundreds (or even thousands) of computation layers and hundreds of millions of parameters. Therefore, how to accommodate the large and extremely deep models, such as BERT to edge device becomes an imminent problem.

There have been some efforts to compress the BERT model while maintaining the accuracy for downstream NLP tasks. MobileBERT [Sun et al., 2020] is able to reduce the memory requirement, but there is still a considerable execution overhead due to a large number of computation units, thus leading to high inference latency. Moreover, the large number of model layers also brings challenges in compiling models to mobile devices. To the best of our knowledge, only TensorFlow-Lite (TFLite) [TensorFlow, 2017] supports deploying BERT models on mobile CPU (not on mobile GPU), while no other frameworks can even support BERT models on mobile CPU.

In this paper, we propose a compression-compilation co-design framework to optimize the structures of BERT variants for mobile devices. This is the first framework that involves compiler optimizations in the architecture search loop, aiming to co-optimize the model accuracy and computation resource usage. We also propose a highly effective layer fusion method to reduce intermediate results to achieve lower latency on both mobile CPU and GPU. Our framework outperforms the state-of-the-art framework, TFLite, by up to 7.8× speedup. Thus achieving the least latency while executing on mobile devices. We will release our model and framework.

2 Framework Design

There are two processes in CANAO: training and compiler code generation (as shown in Figure 3). The training process includes a controller and a trainer. The controller predicts/generates the model hyperparameters (i.e., network architecture); the trainer trains the predicted model and (quickly) evaluates its accuracy by fine-tuning the model to downstream tasks. The compiler code generation process takes the predicted model and returns execution information (e.g. number of fused layers, latency, CPU/GPU utilization). The execution information together with the model accuracy
Inference for example, without layer fusion between accuracy and latency, preventing from searching the optimal architecture by maximizing the expected reward.

For the training process, the controller generates the architectural hyperparameters of neural networks. This includes two phases: 1) The determination of the number of transformer blocks; 2) The optimization of size for each layer. We find that layer number affects the accuracy the most for BERT related models, thus it should be the first thing we determine when searching the optimized model architecture. Then we optimize the layer size by considering both inference latency and model accuracy, which are set as reward signals to feedback to the controller. The controller serves to find the optimal architecture by maximizing the expected reward.

The compiler code generation process includes three steps: 1) Generate a computational graph from the controller-generated model and apply multiple optimizations on this graph. 2) Employ a novel compiler-based layer fusion optimization to further improve execution performance. This plays a key role in achieving better hardware efficiency. 3) Employ code generation and optimization to generate and further optimize the inference code. The generated inference code is tested on mobile devices. According to the feedback from the device side, the controller makes a better tradeoff between model accuracy and latency.

### 2.1 Controller Architecture Search

Our search space includes the number of layers, hidden layer size, and intermediate embedding size of the feedforward layers. We apply the recurrent neural network for searching the model architecture in the Controller. The recurrent network can be trained with a policy gradient method to maximize the expected reward of the sampled architectures. The accuracy and latency are used as the reward signal to feedback to the controller, which is trained by using the reinforcement learning method to explore the architecture. Our framework can search for a desirable model that achieves a good balance between accuracy and latency, preventing from searching the architecture manually.

### 2.2 Compiler Code Generation

This section introduces our compiler optimizations that optimize the latency reward for the feedback. More specifically, it offers us multiple optimizing opportunities, e.g., reducing intermediate results, and eliminating unnecessary computations by analyzing the computation pattern. There are two phases for layer fusion: Lightweight Polynomial-based Layer Fusion (LP-Fusion) and Polyhedral-based Code Generation.

**LP-Fusion**

We identify all fusion candidates in a model based on two kinds of properties in the polynomial calculation: computation laws (i.e., associative, commutative, and distributive) and data access patterns.

Fig. 2b shows four fusion candidates (or fused blocks) for a computational graph. Layer fusion reduces not only the memory consumption of intermediate results, but also the number of operators. Take Fig. 2b(2) for example, without layer fusion, the computation function is defined as:

\[(\star + F) \odot (G + (\star + F) \odot H)\]

The layer and computation count numbers are 4 and 5, respectively. After fusion, the computation function is simplified as:

\[(\star + F) \odot (G + H)\]

Where layer and computation count numbers become 1 and 3, respectively. This process can significantly reduce the operator number and computation overhead. Compared with prior work on loop fusion [Ashari et al., 2015; Bezanson et al., 2017; Boehm et al., 2018], the novelty of this approach is that we exploit a restricted domain of DNN execution. Thus, we can enable more aggressive optimizations without very expensive exploration.

**Polyhedral-based Code Generation**

LP-Fusion supports grouping multiple layers with varied output shapes, i.e., in the code-level, the nested loop structures of these layers may be different. Traditional compilers cannot support this kind of loop fusion well, mainly due to the complexity of such loop analysis. Due to space constraints, this section illustrates this complexity with an example. In this example, a trade-off exists between data locality optimization and redundant computation, thus making it difficult to select the optimal version automatically.

Fig. 2a and Figure 4 show the example. There are three operators: Mul-1, Mul-2, and Add. Mul-1 and Mul-2 take matrices A and B as their input, respectively. Add takes the

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Figure 2: a. Fusion example demonstrated in Figure 4. b. Sample fusion candidates for a computational graph section with an input (marked with A). Each layer has an input either from the previous layer/layers or from its weights, marked with other alphabets. Each number (from 1 to 4) denotes a fusion candidate (or fused block) based on mathematical properties.

Figure 3: Overview of compiler-aware neural architecture optimization framework.
Table 1: Inference latency comparison of CANAO framework and TFLite on mobile CPU and GPU. All models are generated with English Wikipedia dataset. TFLite does not support BERT on mobile GPU.

Table 2: Evaluation accuracy results on GLUE benchmark. All models are optimized with layer fusion and code generation (i.e., they already run faster than their TFLite implementation) with a fixed sequence length of 128.

random question that is related to the paragraph, it will automatically highlight the answer in the test. Figure 1 right is the Text Generation task. Given a starting sentence, it can automatically generate new sentences by word.

3.3 Effectiveness of Compiler Optimizations

We compare with a state-of-the-art framework, TFlite. Table 1 shows inference latency comparison results. TFLite only supports mobile CPU execution, and other frameworks do not support BERT models on mobile devices. And GPU performance is unusually slower than CPU (only 0.6× speedup for CANAOBERT over TFlite on CPU). The fully optimized framework can achieve up to 2.0× speedup on CPU, and 2.4× on GPU, over TFlite’s CPU execution. Notably, comparing to BERT\textsubscript{BASE} on TFLite (352ms on CPU), our overall model and framework (45ms on GPU) can achieve up to 7.8× speedup.

4 Conclusion

We introduced a novel compression-compiler co-design framework to optimize the structures of BERT variants for mobile devices. We implemented compiler optimizations in the architecture search loop, aiming to co-optimize the model accuracy and computation resource usage. We also implemented a highly effective layer fusion method to reduce intermediate results to achieve lower latency on both mobile CPU and GPU. Further, we presented two BERT applications on mobile devices: Question Answering and Text Generation. Both can be executed in real-time with latency as low as 45ms.
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