Mosaic: An Application-Transparent Hardware–Software Cooperative Memory Manager for GPUs

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This paper summarizes the idea and key contributions of Mosaic, which was published at MICRO 2017 [8], and examines the work’s significance and future potential. Contemporary discrete GPUs support rich memory management features such as virtual memory and demand paging. These features simplify GPU programming by providing a virtual address space abstraction similar to CPUs and eliminating manual memory management, but they introduce high performance overheads during (1) address translation and (2) page faults. A GPU relies on high degrees of thread-level parallelism (TLP) to hide memory latency. Address translation can undermine TLP, as a single miss in the translation lookaside buffer (TLB) invokes an expensive serial page table walk that often stalls multiple threads. Demand paging can also undermine TLP, as multiple threads often stall while they wait for an expensive data transfer over the system I/O (e.g., PCIe) bus when the GPU demands a page.

In modern GPUs, we face a trade-off on how the page size used for memory management affects address translation and demand paging. The address translation overhead is lower when we employ a larger page size (e.g., 2MB large pages, compared with conventional 4KB base pages), which increases TLB coverage and thus reduces TLB misses. Conversely, the demand paging overhead is lower when we employ a smaller page size, which decreases the system I/O bus transfer latency. Support for multiple page sizes can help relax the page size trade-off so that address translation and demand paging optimizations work together synergistically. However, existing page coalescing (i.e., merging base pages into a large page) and splintering (i.e., splitting a large page into base pages) policies require costly base page migrations that undermine the benefits of multiple page sizes. In this paper, we observe that GPGPU applications present an opportunity to support multiple page sizes without costly data migration, as the applications perform most of their memory allocation on masse (i.e., they allocate a large number of base pages at once). We show that this en masse allocation allows us to create intelligent memory allocation policies which ensure that base pages that are contiguous in virtual memory are allocated to contiguous physical memory pages. As a result, coalescing and splintering operations no longer need to migrate base pages.

We introduce Mosaic, a GPU memory manager that provides application-transparent support for multiple page sizes. Mosaic uses base pages to transfer data over the system I/O bus, and allocates physical memory in a way that (1) preserves base page contiguity and (2) ensures that a large page frame contains pages from only a single memory protection domain. We take advantage of this allocation strategy to design a novel in-place page size selection mechanism that avoids data migration. This mechanism allows the TLB to use large pages, reducing address translation overhead. During data transfer, this mechanism enables the GPU to transfer only the base pages that are needed by the application over the system I/O bus, keeping demand paging overhead low. Our evaluations show that Mosaic reduces address translation overheads while efficiently achieving the benefits of demand paging, compared to a contemporary GPU that uses only a 4KB page size. Relative to a state-of-the-art GPU memory manager, Mosaic improves the performance of homogeneous and heterogeneous multi-application workloads by 55.5% and 29.7% on average, respectively, coming within 6.8% and 15.4% of the performance of an ideal TLB where all TLB requests are hits.

1. Introduction

Graphics Processing Units (GPUs) are used for an ever-growing range of application domains due to their capability to provide high throughput. GPUs provide a high amount of throughput but they require a different programming model than CPUs, making their general adoption difficult. Recent support within GPUs for memory virtualization features, such as a unified virtual address space [57,70], demand paging [73], and preemption [2,73], can ease programming by allowing developers to exploit key benefits such as application portability and multi-application execution.

Hardware-supported memory virtualization relies on address translation to map each virtual memory address to a physical address within the GPU memory. Address translation uses page-granularity virtual-to-physical mappings that are stored within a multi-level page table. To look up a mapping within the page table, the GPU performs a page table walk, where a page table walker traverses through each level of the page table in main memory until the walker locates the page table entry for the requested mapping in the last level of the table. GPUs with virtual memory support have translation lookaside buffers (TLBs), which cache page table entries and avoid the need to perform a page table walk for
the cached entries, thereby reducing the address translation latency.

State-of-the-art GPU memory virtualization provides support for demand paging [3, 57, 73, 81, 102]. In demand paging, all of the memory used by a GPU application does not need to be transferred to the GPU memory at the beginning of application execution. Instead, during application execution, when a GPU thread issues a memory request to a page that has not yet been allocated in the GPU memory, the GPU issues a page fault, at which point the data for that page is transferred over the off-chip system I/O bus (e.g., the PCIe bus [76] in contemporary systems) from the GPU memory to the GPU memory. The transfer requires a long latency due to its use of an off-chip bus. Once the transfer completes, the GPU runtime allocates a physical GPU memory address to the page, and the thread can complete its memory request.

**GPU Virtualization Challenges.** Two fundamental challenges prevent further adoption of virtualization in GPUs: (1) the address translation challenge, and (2) the demand paging challenge. The address translation challenge stems from a long latency process that consists of a series of serialized memory accesses required to traverse the page table [80, 81]. As many threads can access different data present in a single page, these serialized page walk accesses significantly limit GPU concurrency, by lowering thread-level parallelism (TLP) and thereby reducing the latency hiding capability of a GPU. Translation lookaside buffers (TLBs) can reduce the latency of address translation by caching recently-used address translation information. Unfortunately, as application working sets and DRAM capacity have increased in recent years, state-of-the-art TLB designs [80, 81] suffer from poor TLB reach, i.e., the TLB covers only a small fraction of the physical memory working set of an application. We found that the poor TLB reach has a detrimental effect on GPU performance, because a single TLB miss can stall hundreds of threads at once, undermining TLP within a GPU and significantly reducing performance [8, 61, 95].

Figure 1 shows the performance of two GPU-MMU designs: (1) a design that uses the base 4KB page size, and (2) a design that uses a 2MB large page size, where both designs have no demand paging overhead (i.e., the system I/O bus transfer takes zero cycles to transfer a page). We normalize the performance of the two designs to a GPU with an ideal TLB, where all TLB requests hit in the L1 TLB. Our full experimental methodology is described in detail in our MICRO 2017 paper [8]. We make two major observations from the figure.

First, compared to the ideal TLB, the GPU-MMU with 4KB base pages experiences an average performance loss of 48.1%. We observe that with 4KB base pages, a single TLB miss often stalls many of the warps, which undermines the latency hiding behavior of the SIMT execution model used by GPUs. Second, the figure shows that using a 2MB page size with the same number of TLB entries as the 4KB design allows applications to come within 2% of the ideal TLB performance.

We find that with 2MB pages, the TLB has a much larger reach, which reduces the TLB miss rate substantially. Thus, there is a strong incentive to use large pages for address translation.

To increase the TLB reach, large pages (e.g., the 2MB or 1GB pages used in many modern CPU architectures [39, 40]) can be employed. However, large pages increase the risk of internal fragmentation, where a portion of the large page is unallocated (or unused). Internal fragmentation occurs because it might often be difficult for an application to completely utilize large contiguous regions of memory. This fragmentation leads to (1) memory bloat, where a much greater amount of physical memory is allocated than the amount of memory that the application needs; and (2) longer memory access latencies, due to a potentially lower effective TLB reach and more page faults [56].

The demand paging challenge stems from a page fault, which requires a long-latency data transfer for an entire page over the system I/O bus [76]. Since GPU threads often access data in the same page due to data locality, a single page fault can cause multiple threads to stall at once. As a result, the page fault can significantly reduce the amount of TLP that the GPU can exploit, and thus significantly degrade performance [8, 102].

Unlike address translation, which benefits from larger pages, the overhead of demand paging is smaller when a smaller page size is used. A larger amount of data transfer increases the transfer time, increases the amount of time that GPU threads stall, and decreases TLP. Furthermore, as the size of a page increases, there is a greater probability that an application does not need all of the data in the page. As a result, threads may stall for a longer time without gaining any further benefit in return. Based on these two conflicting observations, memory virtualization in GPU systems has a fundamental trade-off due to the page size choice. We provide more detail on the trade-off in our MICRO 2017 paper [8].

2. Mosaic

In our MICRO 2017 paper [8], we propose Mosaic, a new GPU memory management scheme that aims to get the best of both small and large page sizes. Mosaic relaxes the page size trade-off by using multiple page sizes transparently to the application, and, thus, to the programmer. With multiple page sizes, and the ability to change virtual-to-physical mappings
dynamically, the GPU system can support good TLB reach by using large pages for address translation, while providing good demand paging performance by using base pages for data transfer. However, while coalescing multiple small pages into a large page requires a contiguous region, existing memory allocation mechanisms make it difficult to find regions of physical memory where base pages can be coalesced without a large number of page migration operations. This is because existing GPU memory allocation mechanisms do not allocate base pages in a manner that is aware of the contiguity of memory allocated to each application. Figure 2 shows how a state-of-the-art GPU memory manager [81] allocates memory for two applications. Within a single large page frame (i.e., a contiguous piece of physical memory that is the size of a large page and whose starting address is page aligned), the GPU memory manager allocates base pages from both Applications 1 and 2 (1 in Figure 2). As a result, the memory manager cannot coalesce the base pages into a large page (2) without first migrating some of the base pages, which would incur a high latency. Instead, Mosaic allocates physical base pages in a way that avoids the need to migrate data during coalescing (3 in Figure 3), and uses a simple coalescing mechanism to combine base pages into large pages (e.g., 2MB) and thus increase TLB reach (4 in Figure 3).

![Figure 2: Page allocation and coalescing behavior of a state-of-the-art GPU memory manager [81]. Adapted from [8].](image1)

![Figure 3: Page allocation and coalescing behavior of Mosaic. Adapted from [8].](image2)

We make a key observation about the memory behavior of contemporary general-purpose GPU (GPGPU) applications. We find that the vast majority of memory allocations in GPGPU applications are performed en masse (i.e., a large number of pages are allocated at the same time). The en masse memory allocation presents us with an opportunity: with so many pages being allocated at once, we can rearrange how we allocate the base pages to ensure that (1) all of the base pages allocated within a large page frame belong to the same virtual address space, and (2) base pages that are contiguous in virtual memory are allocated to a contiguous portion of physical memory and aligned within the large page frame.

Mosaic is designed to achieve these two goals. It consists of three major components: Contiguity-Conserving Allocation (CoCoA), the In-Place Coalescer, and Contiguity-Aware Compaction (CAC). These three components work together to coalesce (i.e., combine) base pages into large pages and splinter (i.e., split apart) large pages back to base pages during memory management. Memory management operations for Mosaic take place at two times: (1) when memory is allocated, and (2) when memory is deallocated. We describe what happens at each component briefly. Figure 4 depicts the three components of Mosaic, and we will use Figure 4 to provide a walkthrough of the actions taken during memory allocation and deallocation.

**Memory Allocation.** When a GPGPU application wants to access data that is not currently in the GPU memory, it sends a request to the GPU runtime (e.g., OpenCL, CUDA runtimes) to transfer the data from the CPU memory to the GPU memory (1 in Figure 4). A GPGPU application typically allocates a large number of base pages at the same time. CoCoA allocates space within the GPU memory (2) for the base pages, working to conserve the contiguity of base pages, if possible during allocation. Regardless of contiguity, CoCoA provides a soft guarantee that a single large page frame contains base pages from only a single application. Once the base page is allocated, CoCoA initiates the data transfer across the system I/O bus (3). When the data transfer is complete (4), CoCoA notifies the In-Place Coalescer that allocation is done by sending a list of the large page frame addresses that were allocated (5). For each of these large page frames, the runtime portion of the In-Place Coalescer then checks to see whether (1) all base pages within the large page frame have been allocated, and (2) the base pages within the large page frame are contiguous in both virtual and physical memory. If both conditions are true, the hardware portion of the In-Place Coalescer updates the page table to coalesce the base pages into a large page (6). Section 4.3 of our MICRO 2017 paper [8] describes how page tables are modified to support coalescing.

**Memory Deallocation.** When a GPGPU application would like to deallocate memory (e.g., when an application kernel finishes), it sends a deallocation request to the GPU runtime (7). For all deallocated base pages that are coalesced into a large page, the runtime invokes Contiguity-Aware Compaction (CAC) for the corresponding large page. The runtime portion of CAC checks to see whether the large page has a high degree of internal fragmentation (i.e., if the number of unallocated base pages within the large page exceeds a predetermined threshold). For each large page with high internal fragmentation, the hardware portion of CAC updates the page table to splinter the large page back into its constituent base pages (8). Next, CAC compacts the splintered large page frames, by migrating data from multiple splintered
large page frames into a single large page frame (9). Finally, CAC notifies CoCoA of the large page frames that are now free after compaction (10), which CoCoA can use for future memory allocations. We describe each component of Mosaic in more detail in Sections 4.2, 4.3, and 4.4 of our MICRO 2017 paper [8].

3. Evaluation Methodology

Table 1 shows the system configuration we simulate for our evaluations, including the configurations of the GPU cores and memory partitions. We modify the MAFIA framework [43], which uses GPGPU-Sim 3.2.2 [10], to evaluate Mosaic. We add a memory allocator into cuda-sim, the CUDA simulator within GPGPU-Sim, to handle all virtual-to-physical address translations and to provide memory protection. We add an accurate model of address translation to GPGPU-Sim, including TLBs, page tables, and a page table walker. The page table walker is shared across all SMs, and allows up to 64 concurrent walks. Both the L1 and L2 TLBs have separate entries for base pages and large pages [32,47,48,75,78,79]. Each TLB contains miss status holding registers (MSHRs) [54] to track in-flight page table walks. Our simulation infrastructure supports demand paging by detecting page faults and faithfully modeling the system I/O bus (i.e., PCIe) latency based on measurements from NVIDIA GTX 1080 cards [74]. We use a worst-case model for the performance of our compaction mechanism conservatively, by stalling the entire GPU (all SMs) and flushing the pipeline. We have publicly released our simulator modifications as open source software [88,89].

We evaluate the performance of Mosaic using both homogeneous and heterogeneous workloads. We categorize each workload based on the number of concurrently-executing applications, which ranges from one to five for our homogeneous workloads, and from two to five for our heterogeneous workloads. We form our homogeneous workloads using multiple copies of the same application. We build 27 homogeneous workloads for each category using GPGPU applications from the Parboil [92], SHOC [25], LULESH [49, 50], Rodinia [20], and CUDA SDK [69] suites. We form our heterogeneous workloads by randomly selecting a number of applications out of these 27 GPGPU applications. We build 25 heterogeneous workloads per category. In total we evaluate 235 homogeneous and heterogeneous workloads.

We compare Mosaic to two mechanisms: (1) GPU-MMU, a baseline GPU with a state-of-the-art memory manager based on the work by Power et al. [81]; and (2) Ideal TLB, a GPU with an ideal TLB, where every address translation request hits in the L1 TLB (i.e., there are no TLB misses). We report workload performance using the weighted speedup metric [28,29], which is calculated as:

\[
\text{Weighted Speedup} = \sum \frac{\text{IPC}_{\text{shared}}}{\text{IPC}_{\text{alone}}}
\]

where IPC_{\text{alone}} is the retired instructions per cycle (IPC) of an application in the workload that runs on the same number of shader cores using the baseline state-of-the-art configuration [81], but does not share GPU resources with any other applications; and IPC_{\text{shared}} is the IPC of the application when it runs concurrently with other applications. We report the

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**Table 1**: Configuration of the simulated system. Adapted from [8].

| GPU Core Configuration |
|------------------------|
| **Shader Core Config** |
| 30 cores, 1020 MHz, GTO warp scheduler [84] |
| **Private L1 Cache** |
| 16KB, 4-way associative, LRU, L1 misses are coalesced before accessing L2, 1-cycle latency |
| **Private L1 TLB** |
| 128 base page/16 large page entries per core, fully associative, LRU, single port, 1-cycle latency |

| Memory Partition Configuration |
|-------------------------------|
| (6 memory partitions in total with each partition accessible by all 30 cores) |

| Shared L2 Cache |
|-----------------|
| 2MB total, 16-way associative, LRU, 2 cache banks, 2 ports per memory partition, 10-cycle latency |
| Shared L2 TLB |
| 512 base page/256 large page entries, 16-way/fully-associative (base page/large page), non-inclusive, LRU, 2 ports, 10-cycle latency |
| DRAM |
| 3GB GDDR5 [37, 53], 1674 MHz, 6 channels, 8 banks per rank, FR-FCFS scheduler [83, 104], burst length 8 |

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**Figure 4**: High-level overview of Mosaic, showing how and when its three components interact with the GPU memory. Reproduced from [8].
4. Experimental Results

Figure 5 shows the performance of Mosaic for the homogeneous workloads we evaluated. We make two observations from the figure. First, we observe that Mosaic is able to recover most of the performance lost due to the overhead of address translation (i.e., an ideal TLB) in homogeneous workloads. Compared to the GPU-MMU baseline, Mosaic improves system performance by 55.5%, averaged across all 135 of our homogeneous workloads. The performance of Mosaic comes within 6.8% of the Ideal TLB performance, indicating that Mosaic is effective at extending the TLB reach. Second, we observe that Mosaic provides good scalability. As we increase the number of concurrently-executing applications, which puts more pressure on the shared TLBs, we observe that the performance of Mosaic remains close to the Ideal TLB performance.

Figure 6 shows the performance of Mosaic for heterogeneous workloads that consist of multiple different randomly-selected GPGPU applications (100 workloads in total). From the figure, we observe that on average across all of the workloads, Mosaic provides a performance improvement of 29.7% over GPU-MMU, and comes within 15.4% of the Ideal TLB performance. We find that the improvement comes from the significant reduction in the TLB miss rate with Mosaic. We also see that Mosaic’s scalability is good, as the number of applications increases, yet there is still room for improvement to reach the performance of Ideal TLB. We conclude that Mosaic is a more effective memory manager than the state-of-the-art. A detailed analysis of the results in Figures 5 and 6 can be found in Sections 6.1 and 6.2 of our MICRO 2017 paper [8].

Impact of Demand Paging on Performance. All of our results so far show the performance of the GPU-MMU baseline and Mosaic when demand paging is enabled. Figure 7 shows the normalized weighted speedup of the GPU-MMU baseline and Mosaic, compared to GPU-MMU without demand paging, where all data required by an application is moved to the GPU memory before the application starts executing. We make two observations from the figure. First, we find that Mosaic outperforms GPU-MMU without demand paging by 58.5% on average for homogeneous workloads and 47.5% on average for heterogeneous workloads. Second, we find that demand paging has little impact on the weighted speedup. This is because demand paging latency occurs only when a kernel launches, at which point the GPU retrieves data from the CPU memory. The data transfer overhead is required regardless of whether or not demand paging is enabled, and thus the GPU incurs similar overhead with and without demand paging. We conclude that Mosaic improves performance significantly, regardless of the demand paging overhead in the baseline.

TLB Hit Rate. Figure 8 compares the overall TLB hit rate of GPU-MMU to Mosaic for 214 of our 235 workloads, which suffer from limited TLB reach (i.e., workloads that have an L2 TLB hit rate lower than 98%). We make two observations from the figure. First, we observe that Mosaic is very effective at increasing the TLB reach of these workloads. We find that for the GPU-MMU baseline, every fully-mapped large page frame contains pages from multiple applications, as the GPU-MMU allocator does not provide the soft guarantee of CoCoA (i.e., a single large page frame contains base pages from only a single application). As a result, GPU-MMU does not have any opportunities to coalesce base pages into a large page without performing significant amounts of data migration. In contrast, Mosaic can coalesce a vast majority of base pages thanks to CoCoA. As a result, Mosaic reduces the TLB miss rate drastically for these workloads, with the average miss rate falling below 1% in both the L1 and L2 TLBs. Second, we observe an increasing amount of interference in GPU-MMU when more than three applications are running concurrently. This results in a lower TLB hit rate as the number of applications increases from three to four, and from four to five. The L2 TLB hit rate of GPU-MMU drops from 81% in workloads with two concurrently-executing applications to 62% in workloads with five concurrently-executing applications. Mosaic experiences no such drop due to interference as we increase the number of concurrently-executing applications.
since it makes much greater use of large page coalescing and enables a much larger TLB reach. We conclude that Mosaic is very effective in improving the hit rate.

![TLB Hit Rate](image)

Figure 8: L1 and L2 TLB hit rates for GPU-MMU and Mosaic. Reproduced from [8].

We provide the following additional results in our full MICRO 2017 paper [8]:

- Individual applications' performance with Mosaic and the baseline GPU-MMU
- TLB size sensitivity of Mosaic and the baseline GPU-MMU
- Analysis of the effectiveness of CAC to reduce memory fragmentation incurs by using large pages

5. Related Work

To our knowledge, this is the first work to (1) analyze the fundamental trade-offs between TLB reach, demand paging performance, and internal page fragmentation; and (2) propose an application-transparent GPU memory manager that preemptively coalesces pages at allocation time to improve address translation performance, while avoiding the demand paging inefficiencies and memory copy overheads typically associated with large page support. Reducing performance degradation from address translation overhead is an active area of work for CPUs, and the performance loss that we observe as a result of address translation is well corroborated [13, 15, 31, 33, 63]. In this section, we discuss previous techniques that aim to reduce the overhead of address translation and demand paging.

5.1. TLB Designs for CPU Systems

TLB miss overhead can be reduced by (1) accelerating page table walks [11, 14] or reducing the walk frequency [32]; or (2) reducing the number of TLB misses (e.g., through prefetching [16, 46, 90], prediction [75], structural changes to the TLB [77, 78, 93] or a TLB hierarchy [4, 5, 13, 15, 31, 47, 60, 91]).

Support for Multiple Page Sizes. Multi-page mapping techniques [77, 78, 93] use a single TLB entry for multiple page translations, improving TLB reach by a small factor. Much greater improvements to TLB reach are needed to deal with modern memory sizes. MIX TLB [24] accommodates entries that translate multiple page sizes, eliminating the need for a dedicated set of large page entries in the TLB. MIX TLB is orthogonal to our work, and can be used with Mosaic to further improve TLB reach.

Navarro et al. [66] identify contiguity-awareness and fragmentation reduction as primary concerns for large page management, proposing reservation-based allocation and deferred promotion (i.e., coalescing) of base pages to large pages. Similar ideas are widely used in modern OSes [23]. Instead of the reservation-based scheme, Ingens [56] employs a utilization-based scheme that uses a bit vector to track spatial and temporal utilization of base pages.

Techniques to Increase Memory Contiguity. GLUE [79] groups contiguous, aligned base page translations under a single speculative large page translation in the TLB. GTSM [26] provides hardware support to leverage the contiguity of physical memory region even when pages have been retired due to bit errors. These mechanisms for preserving or recovering contiguity are orthogonal to the contiguity-conserving allocation we propose for Mosaic, and they can help Mosaic by avoiding the need for compaction.

Gorman et al. [55] propose a placement policy for an OS’s physical page allocator that mitigates fragmentation and promotes contiguity by grouping pages according to the amount of migration required to achieve contiguity. Subsequent work [36] proposes a software-exposed interface for applications to explicitly request large pages like libhugetlbfs [34]. These ideas are complementary to our work. Mosaic can potentially benefit from similar policies if such policies can be simplified enough to be implementable in hardware.

Alternative TLB Designs. Research on shared last-level TLB designs [15, 17, 60] and page walk cache designs [14] has yielded mechanisms that accelerate multithreaded CPU applications by sharing translations between cores. SpecTLB [12] provides a technique that predicts address translations. While speculation works on CPU applications, speculation for highly-parallel GPUs is more complicated [41, 44], and can potentially waste off-chip DRAM bandwidth, which is a highly-contended resource in GPUs. Direct segments [13] and redundant memory mappings [47] provide virtual memory support for server workloads that reduces the overhead of address translation. These proposals map large contiguous chunks of virtual memory to the physical address space in order to reduce the address translation overhead. While these techniques improve the TLB reach, they increase the transfer latency depending on the size of the virtual chunks they map.

5.2. TLB Designs for GPU Systems

TLB Designs for Heterogeneous Systems. Previous works provide several TLB designs for heterogeneous systems with GPUs [80, 81, 95] and with accelerators [22]. Mosaic improves upon a state-of-the-art TLB design [81] by providing application-transparent, high-performance support for multiple page sizes in GPUs. No prior work provides such support.

TLB-Aware Warp Scheduler. Pichai et al. [80] extend the cache-conscious warp scheduler [84] to be aware of the TLB in heterogeneous CPU-GPU systems. Other more sophisticated warp schedulers [51, 59, 62, 65, 84, 85, 103] can also be extended to be TLB aware. These techniques are orthogonal to the
problem we focus on, and can be applied in conjunction with Mosaic to further improve performance.

**TLB-Aware Memory Hierarchy.** Ausavarungnirun et al. [9] improve the performance of the GPU under the presence of memory protection by redesigning the GPU main memory hierarchy to be aware of TLB-related memory requests. Many prior works propose memory scheduling designs for GPUs [7, 42, 45, 101] and heterogeneous systems [6, 94]. These memory scheduling design can be modified to be aware of TLB-related memory requests and used in conjunction with Mosaic to further improve the performance of the GPUs.

**Analysis of Address Translation in GPUs.** Vesely et al. [95] analyze support for virtual memory in heterogeneous systems, finding that the cost of address translation in GPUs is an order of magnitude higher than that in CPUs. They observe that high-latency address translations limit the GPU’s latency hiding capability and hurt performance. Mei et al. [61] use a set of microbenchmarks to evaluate the address translation process in commercial GPUs. Their work concludes that previous NVIDIA architectures [71, 72] have off-chip L1 and L2 TLBs, which lead to poor performance.

**GPU Core Modifications.** Many prior works propose modifications to the GPU core design [7, 45, 51, 52, 55, 59, 62, 65, 84, 85, 86, 87, 97, 98, 103]. These techniques are complementary to Mosaic and can be combined with Mosaic to further improve GPU performance.

### 5.3. GPU Virtualization

VAST [58] is a software-managed virtual memory space for GPUs. In that work, the authors observe that the limited size of physical memory typically prevents data-parallel programs from utilizing GPUs. To address this, VAST automatically partitions GPU programs into chunks that fit within the physical memory space to create the illusion of infinite virtual memory. Unlike Mosaic, VAST is unable to provide memory protection from concurrently-executing GPGPU applications. Zorua [96] is a holistic mechanism to virtualize multiple hardware resources within the GPU. Zorua does not virtualize the main memory, and is thus orthogonal to our work. vmCUDA [99] and rCUDA [27] provide close-to-ideal performance, but they require significant modifications to GPGPU applications and the operating system, which sacrifice transparency to the application, performance isolation, and compatibility across multiple GPU architectures.

### 5.4. Demand Paging for GPUs

Demand paging is a challenge for GPUs [95]. Recent works [3, 102], and the AMD hUMA [57] and NVIDIA PASCAL architectures [73, 102] provide various levels of support for demand paging in GPUs. These techniques do not tackle the existing trade-off in GPUs between using large pages to improve address translation and using base pages to minimize demand paging overhead, which we relax with Mosaic.

### 6. Potential Impact of Mosaic

While several previous works propose mechanisms to lower the overhead of virtual memory [13, 15, 26, 31, 33, 63, 79, 80, 81, 95], only a handful of these works extensively evaluate virtual memory on GPUs [58, 80, 81, 95], and no work has investigated virtual memory as a shared resource when multiple GPGPU applications need to share the GPUs. In this section, we explore the potential future impact of Mosaic.

**Support for Concurrent Application Execution in GPUs.** The large number of cores within a contemporary GPU make it an attractive substrate for executing multiple applications in parallel. This can be especially useful in virtualized cloud environments, where hardware resources are safely partitioned across multiple virtual machines to provide efficient resource sharing. Prior approaches to execute multiple applications concurrently on a GPU have been limited, as they either (1) lack sufficient memory protection support across multiple applications; (2) incur a high performance overhead to provide memory protection; or (3) perform a conservative static partitioning of the GPU, which can often underutilize many resources in the GPU.

Mosaic provides the first flexible support for memory protection within a GPU, allowing applications to dynamically partition GPU resources without violating memory protection guarantees. This support can enable the practical virtualization and sharing of GPUs in a cloud environment, which in turn can increase the appeal of GPGPU programming and the use cases of GPGPUs. By enabling practical support for concurrent application execution on GPUs, Mosaic encourages and enables future research in several areas, such as resource sharing mechanisms, kernel scheduling, and quality-of-service enforcement within the GPU and heterogeneous systems.

**Virtual Memory for SIMD Architectures.** Mosaic is an important first step to enable low overhead virtual memory in GPUs. We believe that the key ideas and general observations that we make are applicable to any highly-parallel SIMD architecture [30], and to heterogeneous systems with SIMD-based processing cores [1, 18, 19, 21, 38, 39, 40, 64, 67, 68, 82, 100]. Future works can expand upon our findings and adapt our mechanisms to reduce the overhead of page walks and demand paging on other SIMD-based systems.

**Improved Programmability.** Aside from memory protection, virtual memory can be used to (1) improve the programmability of GPGPU applications, and (2) decouple a GPU kernel’s working set size from the size of the GPU memory. In fact, Mosaic transparently allows applications to benefit from virtual memory without incurring a significant performance overhead. This is a key advantage for programmers, many of whom are used to the conventional programming model used in CPUs to provide application portability and memory protection. By providing programmers with a familiar and simple memory abstraction, we expect that a greater number of programmers will start writing high-performance GPGPU
applications. Furthermore, by enabling low-overhead memory virtualization, Mosaic can enable new classes of GPGPU applications. For example, in the past, programmers were not able to easily write GPGPU applications whose memory working set sizes exceeded the physical memory within the GPU. With Mosaic, programmers no longer need to restrict themselves to applications whose working sets fit within the physical memory; they can rely on the GPU itself software-transparently managing page migration and address translation.

Publicly-Released Infrastructure. Our simulation infrastructure is publicly available as open-source software [88]. Other researchers can utilize our infrastructure to conduct future research on virtual memory management on GPUs. Some examples of research topics that can be investigated using our infrastructure include (1) how to manage which pages reside in CPU memory or GPU memory, (2) how to dynamically partition the physical main memory across multiple concurrently-executing applications, and (3) how to maintain programmability of the virtual memory as the GPU architecture evolves and becomes more heterogeneous over time. We hope and believe that our new, open-source infrastructure can inspire future research in these and other research areas on GPU and heterogeneous system memory virtualization.

7. Conclusion

We introduce Mosaic, a new GPU memory manager that provides application-transparent support for multiple page sizes. The key idea of Mosaic is to perform demand paging using smaller page sizes, and then coalesce small (i.e., base) pages into a larger page immediately after allocation, which allows address translation to use large pages and thus increase TLB reach. We have shown that Mosaic significantly outperforms state-of-the-art GPU address translation designs and achieves performance close to an ideal TLB, across a wide variety of workloads. We conclude that Mosaic effectively combines the benefits of large pages and demand paging in GPUs, thereby breaking the conventional tension that exists between these two concepts. We hope the ideas presented in our MICRO 2017 paper can lead to future works that analyze Mosaic in detail and provide even lower-overhead support for synergistic address translation and demand paging in GPUs and heterogeneous systems.

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