SESSION D:

SOI/SOS

RADIATION EFFECTS
SILICON-ON-INSULATOR TECHNOLOGIES,--ARE WE CONVERGING ON A TECHNIQUE OF CHOICE?

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ABSTRACT

This paper attempts to present an unbiased review and evaluation of the dozen or more techniques under development to fabricate SOI structures. It includes an historical perspective, a review of the state-of-the-art, and an assessment of current SOI development programs in government and industry.

INTRODUCTION AND HISTORICAL PERSPECTIVE

Ten years ago, before we even had the term Silicon-On-Insulator (SOI), the technologies that fit into this category were heteroepitaxial Silicon-On-Sapphire (SOS) and the polysilicon substrate Dielectric Isolation (poly DI) technology. Both of these technologies are still with us today. Poly DI has been a workhorse in military strategic systems and SOS is finally making some inroads with military systems designers. SOS is unfortunately suffering from an image problem as a result of years of problems, even though it has made great strides in recent years, the most important of which is probably the development of a reliable materials quality screening technique.

Even though these technologies fit the generic label SOI, what is generally meant by SOI is a single crystal silicon film on a silicon dioxide (or other insulating) layer on a single crystal silicon substrate. Beginning in the late 70s, work in this area has mushroomed. The IEEE SOS Workshop has become the SOS/SOI Workshop and virtually every microelectronics conference has an SOI session.

Even though many of the different SOI techniques are rediscoveries of technologies several years or even decades older, the tremendous growth of interest in SOI as we know it today dates from the late 70s. Many would argue differently as to the true beginnings of SOI, depending on their initial entry into the field, but we believe that it was laser processing that lit the spark and generated the environment in which many SOI technologies have flourished. It is ironic that laser recrystallization has been overshadowed by most of the other SOI techniques, although it may someday find a niche of its own.

Laser annealing (of implant damage) was first investigated by Soviet scientists. It made its way via Italy to the US. The pioneering work on laser processing at Bell Laboratories, Oak Ridge National Laboratories, and elsewhere brought new life to a newly resurrected society, the Materials Research Society, and its annual meeting in Boston. Many interesting phenomena were discovered,-- for example, the pulsed laser poly recrystallization pattern and the explosive recrystallization pattern in Figure 1.

At the same time, pioneering work on CW scanned laser recrystallization of SOI structures was performed at Stanford University. Beam recrystallization had been accomplished in the past, but the time was not yet ripe for it to fully develop. Though this type of material didn't appear to be device worthy, good discrete MOS devices and simple circuits were made in it (Figure 2). In fact, even though it had its own unique problems (grain boundaries and film thickness variations), it could compete with SOS in terms of material quality (Figure 3).

These initial successes laid the foundation for other SOI techniques to build upon. The work on Graphoepitaxy at MIT Lincoln Laboratory led to the development of the graphite strip heater for Zone Melt Recrystallization (ZMR) which was a rediscovery of a technique first patented in 1950. Work in Japan on oxygen implantation to form a buried silicon dioxide layer was also a rediscovery of earlier techniques that were before their time.

Electrochemical techniques were applied to device isolation by oxidation of porous silicon. Standard epitaxial techniques were modified to allow
Epitaxial Lateral Overgrowth (ELO)\textsuperscript{20}. Epitaxial techniques were also applied to produce crystalline insulating layers on which isolated crystalline silicon films could be grown\textsuperscript{21}. Most recently, variants on the old DI technique were developed using oxide bonding of silicon wafers\textsuperscript{22}. All of these techniques will be discussed below.

**REVIEW OF SOI TECHNOLOGY**

Clearly, the front running technology at the moment is SIMOX (Separation by Implantation of Oxygen)\textsuperscript{16} (Figure 4). One of the earliest government programs in SOI compared SIMOX, FIPOS (Full Isolation by Porous Oxidized Silicon)\textsuperscript{18} and carbon strip heater recrystallization (ZMR)\textsuperscript{14}. The conclusion reached was that SIMOX had the best chance of supporting VLSI circuits in the shortest amount of time.

SIMOX has made rapid advances. The initial government program produced a 4K RAM with excellent transient radiation hardness\textsuperscript{23}. More recently a 16K RAM has been fabricated (Figure 5a). In this technique, oxygen is implanted to very high doses (greater than $1 \times 10^{18}$ cm\textsuperscript{-2}). If the implant is done at elevated temperature (typically 500°C), sufficient surface crystallinity remains to serve as a seed for recrystallization of a surface layer (typically 200nm thick) during a subsequent high temperature anneal (1150-1400°C). This anneal also redistributes the implanted oxygen to form a good quality buried silicon dioxide layer (typically 500nm thick). Nitrogen implantation has been performed as well\textsuperscript{24}, to produce a buried silicon nitride layer, but with less success than with oxygen due to the small dose window. Too low a dose produces a poor quality insulating layer, while too high a dose results in nitrogen bubbles and delamination problems. Combining oxygen and nitrogen has shown some promise for increasing radiation hardness of the buried insulator.

Research continues to improve the quality of
Figure 4. SOI preparation by SIMOX (Separation by Implantation of Oxygen).

Figure 5. VLSI circuits demonstrated in SOI. (a) 16K SRAM in SIMOX SOI (courtesy Texas Instruments). (b) 1K SRAM in ZMR SOI (courtesy MIT Lincoln Laboratory).

SIMOX wafers. Growing epi layers on SIMOX wafers is not trivial since one must be careful not to lose the thin seed surface film. Major advances in material quality were made as the temperature of the post-implantation anneal was increased. Defect densities are reduced and oxygen precipitates are dissolved.

Anneal temperatures as high as within 5°C of the melting temperature of silicon have been studied using special optical annealing furnaces.\(^{25}\)

The main problem with SIMOX films at present is the high defect density. Until recently, defect densities have been in the \(1 \times 10^8\) cm\(^{-2}\) range. More recently researchers have claimed defect densities of \(1 \times 10^8\) cm\(^{-2}\) with high temperature anneals. Contaminants introduced during implant are also being significantly reduced by careful machine design (silicon coating for anything in the beam path).

Major advances in ion implanter design have been made, giving SIMOX the potential to compete as a practical production process. Following the initial modification of standard implanters to handle oxygen, very high current (100 mA) oxygen implanters have been designed and built (Figure 6). The price is high, however, and companies are slow to commit to the high capital and operating expenses.

Recrystallization of polysilicon films deposited on silicon dioxide layers has been accomplished in a variety of ways. Scanning laser or electron beams have been raster scanned over a wafer. Various techniques have been applied to change the shape of the scanned spot or various patterns have been fabricated in the wafer to control the thermal profile during recrystallization to improve material quality, principally by controlling the location of large angle grain boundaries. Alternatively, seeding through vias to the underlying substrate was used to eliminate grain boundaries.\(^{28,29}\) The greatest success has been achieved with the line-source geometry of the scanning strip heater (Figure 7). Similar geometries can be produced with electron beams or high intensity lamps or simulated by rapidly oscillating beams.\(^{6}\) Though a strong (100) texture is produced in capped layers even without seeding, large angle grain boundaries can be eliminated by seeding from vias to the underlying substrate. Until recently, it seemed that sub-boundaries (very low angle grain boundaries) were unavoidable. Though their impact on device performance and reliability is disputed, they still make people wary. Recent results with specially designed strip heaters (Figure 8) show subboundaries breaking up into discrete dislocations with densities comparable to SIMOX. Early problems with wafer warpage have also been solved. If these results hold up, such ZMR wafers will have advantages over SIMOX wafers. The quality of ZMR films does not degrade near the back interface, though some argue that the higher defect density near the back interface may reduce radiation induced back channel leakage. The
ZONE-MELTING RECRYSTALLIZATION

Figure 7. Zone Melt Recrystallization (ZMR) technique and capped wafer structure.

Figure 8. Graphite strip heater apparatus for ZMR (courtesy MIT Lincoln Laboratory).

The thickness of the insulating oxide layer is variable for ZMR SOI wafers and can be tailored to optimize performance. No epi is needed to produce film thicknesses typical for current CMOS processes and bipolar devices have been made directly in this material. ZMR apparatus is also inexpensive. Even in material with subboundaries, fully functional 1K SRAMs have been demonstrated (Figure 5b).

Another SOI technique that has demonstrated VLSI devices is FIPOS (Figure 9). In this technology, the field areas and the material below the device active areas are made porous by an electrochemical process. The pores then allow rapid oxidation giving a fully isolated device island. Drawbacks of this process are that the island size is limited and all islands must be approximately the same size, which limits device designers. Also, it is a wet chemical process which runs counter to the trend for VLSI processing. This technique is not being very vigorously pursued in this country. NTT in Japan, however, has reported a 64K SRAM with this process.

Another SOI technique that has been able to sustain considerable interest is Epitaxial Lateral Overgrowth (ELO) (Figure 10). Periodic growth and etch cycles and/or special epi growth conditions are used to grow epi up through a via to the underlying substrate and out over an oxide layer while retarding the spontaneous nucleation of polysilicon on the oxide layer. Some successes have been achieved and understanding of the process continues to increase, but the technique is still limited by the necessity of pre-patterning and the limited lateral to vertical growth ratio thus far achieved. The potential advantages of this technique are the high material quality and the fact that epitaxy is a standard production process.

Related to this technique is the solid phase epitaxy of deposited polysilicon films from seed vias to the underlying substrate. The Japanese continue to press hard in this area, though success has been very limited.

Another technique worthy of note is that of epitaxial insulators (Figure 11). In this

Figure 9. SOI by FIPOS (Full Isolation by Porous Oxidized Silicon).

Figure 10. SOI by ELO (Epitaxial Lateral Overgrowth).

Figure 11. SOI fabrication by alternate epitaxial growth of crystalline insulating and silicon layers.
technique, the insulating layer is grown epitaxially and is crystalline rather than amorphous as with the silicon dioxide layer in other SOI techniques. A silicon layer can then be epitaxially grown on the insulator. Examples are spinel, calcium fluoride, and boron phosphide. Many alternating layers of boron phosphide and silicon have been grown with the top silicon layer still being "device worthy" material. It is an exciting concept, particularly for the potential of 3-D integration. Also, epitaxy is a viable commercial process. The materials problems associated with this technique, however, make SOS's problems seem minimal in comparison.

One last recently developed technique is also worthy of note (Figure 12). The Bond and Etchback

![BOND & ETCHBACK](image)

Figure 12. SOI by oxide bonding of two wafers, followed by thinning of one of the wafers.

technique is a variant of the old poly DI technique except that a single crystal silicon substrate replaces the poly substrate as the "handle." Two wafers are joined together by an oxide bonding technique and then most of one of the wafers is removed as with the standard DI technique. This technique promises to solve the wafer warpage and "runout" problems of standard DI which prevent it from being used for VLSI. There are still problems with the bonding process and there is still question as to how much the silicon can be thinned with good uniformity. It may be an important technology as an improvement to standard DI for linear bipolar applications which require thick films.

It is worth emphasizing that different applications for SOI have different requirements. CMOS requires very thin films, now typically 0.3-0.5 μm. It may be advantageous to go to even thinner films (0.1μm) as we go to submicron devices. Bipolar has different requirements for SOI. Digital bipolar requires 2-3μm films and linear bipolar requires 10-15μm films. Material quality requirements are also different. Each of the SOI techniques has its own unique challenges in meeting these requirements.

Looking ahead to more advanced applications such as 3-dimensional or vertically integrated multi-layer structures, the current front running techniques such as SIMOX and ZMR may have difficulty, while others such as ELO or epitaxial insulators may have the edge. Stacked structures were first made in laser recrystallized material.

Another potentially important application is mixed processing which combines SOI and bulk devices on the same chip. Here again, techniques such as ELO or even the original laser recrystallization may find their niche.

The government (particularly SDIO) has begun major development programs in SOI. The premier program, managed by NASA, focuses on SIMOX and seeks to demonstrate a 64K SRAM which is simultaneously very fast and very radiation hard. But other government programs are looking at most of the other SOI techniques and include bipolar as well as CMOS applications. SOI development programs in industry have similar variety.

CONCLUSION

We still haven't answered the question raised by the title of the paper. If we review what has been discussed about the advantages and disadvantages of the various techniques,--about the successes of the various techniques in terms of VLSI demonstration circuits,--about the variety of applications for SOI technology,--and about the variety of programs in government and industry,--the answer seems to be: no, we are not yet converging. But we claim that that is good. Considering the variety of applications, it would be unfortunate for various techniques to be abandoned prematurely. We believe that several techniques will eventually find their way into production rather than a single one.

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