Intrinsic electrical transport and performance projections of synthetic monolayer MoS$_2$ devices

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Abstract
We demonstrate monolayer (1L) MoS$_2$ grown by chemical vapor deposition (CVD) with transport properties comparable to those of the best exfoliated 1L devices over a wide range of carrier densities (up to $\sim 10^{13}$ cm$^{-2}$) and temperatures (80–500 K). Transfer length measurements decouple the intrinsic material mobility from the contact resistance, at practical carrier densities ($> 10^{12}$ cm$^{-2}$). We demonstrate the highest current density reported to date ($\sim 270 \mu$A $\mu$m$^{-1}$ or 44 MA cm$^{-2}$) at 300 K for an 80 nm long device from CVD-grown 1L MoS$_2$. Using simulations, we discuss what improvements of 1L MoS$_2$ are still required to meet technology roadmap requirements for low power and high performance applications. Such results are an important step towards large-area electronics based on 1L semiconductors.

1. Introduction
Monolayer (1L) two-dimensional (2D) semiconductors such as MoS$_2$ have garnered attention for highly scaled optoelectronics and flexible electronics due to their sub-nm thickness, direct band gap, and lack of dangling bonds [1, 2]. For practical applications, such films must be grown over large areas and must demonstrate good electrical properties. Until recently [3–9], however, the highest reported mobility of 1L MoS$_2$ field effect transistors (FETs) grown by chemical vapor deposition (CVD) had been below 20 cm$^2$ V$^{-1}$ s$^{-1}$ on isolated single crystals [10–24]. In addition, little systematic work has been done to understand metallic contacts to CVD-grown 1L films [25], which ultimately limit device performance with scaling.

Here we present the first rigorous transfer length method (TLM) study of as-grown 1L CVD MoS$_2$ devices as a function of temperature, to systematically separate contributions to total device resistance ($R_{TOT}$) from contacts and the channel. Building on previous work to improve contact resistance ($R_c$) [26] we obtain $R_c \approx 6.5$ k$\Omega$ $\mu$m at room temperature and moderate carrier densities. We also extract the effective electron mobility ($\mu_{eff}$) from sheet resistance measurements to be $\sim 20$ cm$^2$ V$^{-1}$ s$^{-1}$, comparable to unencapsulated exfoliated 1L devices on SiO$_2$. Fitting with our compact model [27, 28] yields similar values for $R_c$ and $\mu_{eff}$ and allows us to simulate aggressively scaled device channel lengths ($L$) while maintaining the key material properties. With an equivalent oxide thickness (EOT) and $R_c$ values dictated by future International Technology Roadmap for Semiconductors (ITRS) requirements, the simulations predict that for both the high performance (HP) and low power (LP) specifications, the maximum achievable on-state current ($I_{ON}$) is more strongly dependent on the saturation velocity, $v_{sat}$ than on mobility.

2. Methods
We synthesize continuous 1L MoS$_2$ from solid S and MoO$_3$ precursors with the aid of perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS) [10, 11, 29, 30] on SiO$_2$ on Si ($p^{++}$) substrates, which also serve as back-gates for field-effect devices. Elevated temperature (850 °C) and atmospheric pressure are utilized to encourage lateral epitaxial growth (figures S1 and S2), and the CVD conditions can be tailored to produce either a continuous 1L film or
single-crystal domains up to 10^5 μm^2 (triangular crystals with edges exceeding 300 μm, see figures 1(a)–(d) and supplementary figure S3). Key advances in this work include a combination of PTAS seeding around the chip perimeter, higher synthesis temperatures, and improved electrical contacts with pure Au, which lead to the improved device results shown here. Previous studies that implemented PTAS for CVD growth did not have high-quality electrical data due to (relatively) poor electrical contacts or small grain sizes. Conversely, previous studies that made contact improvements focused on exfoliated multi-layer MoS2, not on CVD-grown 1L. Additional discussion about various growth conditions and their optimization is provided in the supplement.

We define rectangular channel regions by XeF2 etching, and TLM structures with varying channel lengths (L = 80 nm to 1.2 μm) by electron beam (e-beam) lithography, exclusively on 1L regions, as shown in figures 1(e) and (f). Pure Au contacts deposited by e-beam evaporation under high vacuum (∼5 × 10^−8 Torr) are employed without any adhesion layer to achieve a clean contact interface and reduce contact resistance [26]. All electrical measurements were carried out in a vacuum probe station (∼10^−5 Torr) following a vacuum anneal in situ at 200 °C for 1 h.

Atomic force microscopy (AFM), Raman spectroscopy, and photoluminescence are utilized post-fabrication to confirm that the MoS2 devices are indeed 1L [32–34], and that their vibrational and excitonic properties have been preserved. Figure 2(a) illustrates an AFM step-height profile of ∼1 nm, which is consistent with the 1L MoS2 thickness plus a van der Waals gap. Figure 2(b) depicts the in-plane and out-of-plane Raman modes, which are sometimes incorrectly labeled E2g and A1g in the literature; this notation is only strictly correct for bulk and even-number-layer samples, which belong to the D3h and D3h point groups, respectively. Odd-numbered few-layer MoS2 samples (including 1L) belong to the D3h point group. Thus, these Raman features are denoted as E′ and A1′ [35–37] at 383.4 and 403.7 cm^−1, with a peak separation ∆f ∼ 20 cm^−1 [4, 5, 9] typical for as-grown MoS2 1L with slight intrinsic tensile strain. Lastly, the A and B exciton peaks, estimated to be separated by a valence band splitting of ∼150 meV at the K point [34, 38] are clearly exhibited with peaks at 1.79 and 1.93 eV.

### 3. Experimental results and discussion

Typical current vs. gate voltage measurements for these devices with varying channel lengths are shown in figure 3(a) at a drain bias V_D = 1 V. The carrier density (n) is estimated by assuming a simple linear charge dependence on the gate voltage overdrive

\[
n \approx \frac{C_{ox}}{q} (V_{GS} - V_T),
\]

where C_{ox} ≈ 38 nF cm^−2 is the capacitance per unit area of t_{ox} = 90 nm SiO2. V_{GS} is the gate–source voltage and V_T is the threshold voltage obtained by the linear extrapolation method for each channel [31] as shown in figure 3(a) (dashed lines fit to the curve at maximum transconductance). Supplementary figure S4 displays log-scale and forward–backward Id–V GS sweeps of the same devices, demonstrating I_{ON}/I_{OFF} of at least 10⁴ and minimal hysteresis.

Figure 3(b) demonstrates good least-squares fitting to R_TOT versus L for various calculated values of n,
suggesting uniform material and contacts for our devices. The slopes of these lines correspond to the sheet resistance \( R_{\text{SH}} \) (k\( \Omega \)/mm), whereas the ordinate intercept yields twice the width-normalized contact resistance, \( 2R_c \) (k\( \Omega \)/\( \mu \)m); these quantities are extracted for multiple values of \( n \). Resistance and mobility values are then carefully obtained for the same value of \( n \) (i.e. the same gate overdrive, \( V_{\text{GS}}-V_T \)) rather than the same \( V_{\text{GS}} \). We note that it is important to perform such TLM extractions from a wide range of channel lengths (including some well below 1 \( \mu \)m) in order to minimize the \( R_c \) error [26].

In figure 4(a), we observe that \( R_c \) varies with \( n \) as the back gate modulates the Fermi level under the contacts as well as in the channel. We extract \( R_c = 6.5 \pm 1.5 \) k\( \Omega \)/\( \mu \)m at 300 K for \( n \approx 4 \times 10^{12} \) cm\(^{-2} \), with the uncertainty reflecting 90% confidence intervals from a least squares fit of the TLM curve. Although lower \( R_c \) has been achieved in multilayer exfoliated MoS\(_2\) FETs [26, 39], this value for 1L CVD MoS\(_2\) could potentially be reduced further with the aid of chemical doping techniques [39–41] or phase engineering [25, 42]. Moreover, fitting with our compact model [27, 28] and extrapolating to a higher \( n = 10^{13} \) cm\(^{-2} \), \( R_c \) could drop to 5.5 k\( \Omega \)/\( \mu \)m, without any kind of molecular doping or threshold shifting, for pure Au contacts. \( R_c \) also decreases with increasing temperature (\( T \)), consistent with increased thermionic emission over the Schottky barrier at the contacts. Lastly, we note that although our devices exhibit a linear \( I_D-V_{\text{DS}} \) relationship for low drain biases (see supplementary figure S5), this does not justify use of the word ‘Ohmic’ to characterize our contacts from a band structure perspective [43]. Linear \( I_D-V_{\text{DS}} \) curves can still be
obtained at low bias across a Schottky-barrier FET as a result of carriers tunneling through the barrier, resulting in non-negligible contact resistance [44-46].

Using the transmission line model [31, 47], we estimate the specific contact resistivity ($\rho_c$) as shown in figure 4(b) from

$$R_c = \frac{\rho_c}{L_T} \coth \left( \frac{L_c}{L_T} \right) \approx \sqrt{\frac{\rho_c}{R_{SH}}}$$  \hspace{1cm} (2)

where $L_c = 1$ $\mu$m is the length of the contacts and $L_T$ is the current transfer length, i.e. the distance over which the current flowing in the MoS$_2$ drops to 1/e times the value injected at the contact edge. At 300 K, we extract $\rho_c \approx 10^{-5}$ $\Omega$ cm$^2$, a value $\sim 12$ times higher than our best results for few-layer exfoliated MoS$_2$ at the same carrier density, $n = 4 \times 10^{12}$ cm$^{-2}$ [26]. As with $R_c$, we observe $\rho_c$ to decrease with increasing $T$ and $V_{DS}$ in figure 4(b) due to enhanced thermionic and field emission, respectively. Interestingly, we do not see appreciable variation with $n$, as one might expect from a thinning of the Schottky barrier at the Au/MoS$_2$ interface, which would allow for enhanced field emission. Taken together, these two observations indicate that, while both thermionic and field emission play a role, the former is by far the dominant mechanism. This disparity should be exacerbated at lower temperatures, as fewer carriers are able to thermionically surmount the barrier, and the ratio $\rho_c(V_{DS} = 0.1 \text{ V})/\rho_c(V_{DS} = 1.0 \text{ V})$ being 3 times larger at 80 K than at 300 K supports this conclusion. The weak yet observable variation of $\rho_c$ with $n$ for $T = 80$ K and $V_{DS} = 0.1$ V, where few carriers can make it over the barrier and field emission is suppressed, further supports this notion, as an increase in tunneling can then be more easily noticed. This is in contrast to our exfoliated few-layer devices [26], which have a shorter $L_T$ (~40 nm) and $\rho_c$ that clearly decreases with $n$.

We note that the approximation in equation (2) is only valid when $L_T \ll L_c$, in which case $\coth(L_c/L_T) \approx 1$, and we can rearrange to give

$$L_T \approx \sqrt{\frac{\rho_c}{R_{SH}}}$$  \hspace{1cm} (3)

whereby we extract $L_T \approx 100$ nm $\ll L_c$ at 300 K (shown in figure 4(c)), justifying our use of the approximation. As previously mentioned, both $R_c$ and $\rho_c$ decrease for higher $V_{DS}$ due to increased field emission, especially at lower temperatures where thermionic emission is suppressed. This leads to $L_T$ that is essentially constant with respect to $n$, but also decreases with increasing $T$ and $V_{DS}$ (shown in supplementary figure S6). This result suggests that contacts to 2L MoS$_2$
can be scaled to lengths as small as 100 nm before current crowding causes an increase in $R_c$.

Utilizing $R_{SG}$ as given by the TLM fit slopes, the effective mobility can be calculated by

$$\mu_{\text{eff}} = (qnR_{SH})^{-1},$$

where $q$ is the elementary charge and $n$ is given by equation (1). As $n$ increases and equation (1) better approximates the true charge in the channel, equation (4) approaches a constant lowest value, which we take to be the ‘true’ value for $\mu_{\text{eff}}$ in the technologically relevant high carrier density regime (see supplementary figure S6(b)).

We focus on effective mobility rather than field-effect mobility [$\mu_{\text{FE}} = L(\partial I_D/\partial V_{GS})/(W C_{ox} V_{DS})$] in this work because $\mu_{\text{eff}}$ is strictly a channel material parameter that is valid for all moderate values of $n$. In contrast, $\mu_{\text{FE}}$ is heavily dependent on $V_{DS}$ and $V_{GS}$ (due to the Schottky contacts), leading to a concept often referred to as a ‘peak mobility’ as a function of gate voltage [39, 48–50], and potentially resulting in under- or overestimations of the true channel mobility (see supplementary figures S7 and S8). The TLM analysis not only allows us to separate contributions by $R_c$ and $R_{SG}$ to $R_{TOT}$, but also allows for the direct use of $\mu_{\text{eff}}$ as a more reliable channel parameter in device models. In other words, the effective mobility is the more important figure of merit (rather than the field-effect mobility), linking materials, devices (via models, as done below), and system applications of TMDs. We also note that the $\mu_{\text{eff}}$ extracted here is a lower bound on the true band mobility [23] due to fast traps and impurities at the oxide interface, as opposed to mobility values that could be obtained from Hall measurements or from devices on a smooth, clean surface such as hexagonal boron nitride (h-BN) [51].

Analyzing extracted data for $\mu_{\text{eff}}$ versus $T$ in figure 4(d) reveals $\mu_{\text{eff}}$ to be approximately constant near $\sim$28 cm$^2$ V$^{-1}$ s$^{-1}$ at low $T$. The lack of variation in $\mu_{\text{eff}}$ between 100 and 200 K suggests that these values are limited by impurity scattering [52–54], possibly from particles or adsorbates deposited during device fabrication. Above 200 K, $\mu_{\text{eff}}$ is principally limited by optical phonon scattering and rolls off as $\sim T^{-\gamma}$ (where $\gamma \approx 1$), falling to a value of $20 \pm 3$ cm$^2$ V$^{-1}$ s$^{-1}$ at 300 K, comparable with the best CVD 1L devices reported so far [3–5, 19–21]. (Also see supplementary figure S9.) A larger temperature coefficient of mobility, $\gamma$, would be indicative of stronger (intrinsic) phonon scattering. As with our extractions of $R_c$, the uncertainty reflects 90% confidence intervals.

Finally, we wish to understand how the mobility and contact resistance rigorously studied thus far manifest themselves in very small devices. To this end, we fabricated a short-channel ($L \sim 80$ nm) FET on our 1L CVD-grown MoS$_2$ films, and we recorded the transfer characteristics shown in figure 5(a). At room temperature, we measure the highest current density reported to date ($\sim 270$ mA cm$^{-1}$) or 44 MA cm$^{-2}$, taking into account the appropriate 0.615 nm 1L thickness [36, 55]) for CVD-grown 1L MoS$_2$ FETs, as shown in figure 5(b). (An overview of other measurements for reported current density and mobility in 1L CVD MoS$_2$ is provided in supplementary figure S9.)

The current drive is an important metric, because the intrinsic delay of a transistor is $\propto C_{ox} V_{DS}/I_{ON}$, where $V_{DD}$ is the operating voltage. In other words, it is not the intrinsic mobility of the devices that affects the circuit delay, but the total drivable current, which might ultimately be limited by contacts or saturation velocity. Nonetheless, even at high carrier density ($n \sim 10^{12}$ cm$^{-2}$) we note sub-linear (i.e. Schottky-like) measured $I_D$–$V_{DS}$ up to $V_{DS} \sim 1$ V in figure 5(b), further demonstrating the need for reducing contact resistance for very short channel lengths. Values for $\mu_{\text{eff}}$, $R_c$, and maximum $I_D$ could also be further improved by suppressing the detrimental effects of the underlying oxide, i.e. by fabricating devices on h-BN, on oxides with higher phonon energies, or selecting

![Figure 5](image1.png)
4. Simulation projections

Before concluding, we use simulations seeking to project how such short channel 1L MoS$_2$ FETs might behave with more idealized properties, i.e. with lower $R_c$ and properly scaled insulators. To this end, we employ our physics-based device model (described elsewhere [27] and available online [28]) and first fit it against the measured data in figure 5(b), with $\mu_{\text{eff}} = 20-22$ cm$^2$ V$^{-1}$ s$^{-1}$ and $R_c = 6-8$ k$\Omega \mu$m, in good agreement with our TLM extractions described earlier. The model reveals that approximately two thirds of the applied $V_{DS}$ is dropped at the contacts of the 80 nm device, further highlighting the need for contact engineering in such small devices. At higher drain voltage in figure 5(b), the model $I_D$ begins to saturate not due to channel pinch-off, but rather due to carrier velocity saturation, which for these simulations was fit to a value of $v_{\text{sat}} = 7 \times 10^6$ cm s$^{-1}$.

We then use our calibrated model [28] to predict the performance of such 1L semiconductors at scaled ITRS [36] technology nodes for HP and LP applications, in figure 6. We assume the intrinsic channel mobility extracted from experiments in this work and [57], but take the contact resistance ($R_c = 150-200$ $\Omega \mu$m) as required by the ITRS for HP and LP applications. To calculate the ON current we first iteratively adjust the flatband voltage through the gate workfunction to achieve the required OFF current, $I_{\text{OFF}} = 100$ nA $\mu$m$^{-1}$ for HP and 10 pA $\mu$m$^{-1}$ for LP. We neglect the gate leakage current and the source-drain leakage which allows us to benchmark the maximum possible performance of the MoS$_2$ devices. We note that even the highly scaled devices considered in figure 6 are fully in the diffusive transport regime (i.e. ballistic effects do not play a major role), because the electron mean free path in MoS$_2$ is only 1–3 nm (see figure S10) for mobility values between 20 and 80 cm$^2$ V$^{-1}$ s$^{-1}$.

In figure 6 we consider two values for velocity saturation and two values for 1L MoS$_2$ mobility, as shown. The present state-of-the-art 1L MoS$_2$ (red curves, this work on CVD MoS$_2$ and that of [57] on exfoliated MoS$_2$) with $v_{\text{sat}} = 10^6$ cm s$^{-1}$ fall short of the ITRS requirements for both HP and LP. However, this exercise highlights that the role of mobility is secondary, because at high lateral field $I_{\text{ON}}$ is more strongly limited by $v_{\text{sat}}$. On the other hand, if the saturation velocity is increased to simulated projections [58, 59] of $v_{\text{sat}} = 3.2 \times 10^6$ cm s$^{-1}$, we find that both the HP and the LP ITRS requirements could potentially be achieved using 1L MoS$_2$ (green curves) for the shorter channel devices (<20 nm), in agreement with recent quantum transport simulations [60].

It is relevant to inquire why ITRS specifications could be met with a $v_{\text{sat}}$ that even optimistically remains lower than that of silicon. As illustrated in supplementary figure S11, the carrier confinement is different in 1L 2D materials than in typical semiconductors, such that the EOT could be smaller for 2D materials ($t_{\text{ox,2D}} < t_{\text{ox,Si}}$) even for the same physical oxide thickness. This allows 1L 2D materials to achieve higher carrier densities for similar oxide thickness and similar overdrive voltage, and thus higher $I_{\text{ON}}$ even at lower carrier velocities, while meeting $I_{\text{OFF}}$ requirements owing to their larger band gap. Consequently, future work on 2D transistors should focus not only on improving the contact resistance (as highlighted earlier), but also on understanding and improving the charge carrier drift velocities.

**Figure 6.** Benchmarking 1L MoS$_2$ devices for (a) low power (LP) and (b) high performance (HP) ITRS [56] requirements, listed versus the gate length. ITRS requirements are shown in blue with fixed $I_{\text{OFF}} = 10$ pA $\mu$m$^{-1}$ for LP and 100 nA $\mu$m$^{-1}$ for HP. Simulations in red use $v_{\text{sat}} = 10^6$ cm s$^{-1}$, with solid symbols for our CVD-grown MoS$_2$ ($\mu_{\text{eff}} = 20$ cm$^2$ V$^{-1}$ s$^{-1}$) and open symbols from recent exfoliated data [57] ($\mu_{\text{eff}} = 81$ cm$^2$ V$^{-1}$ s$^{-1}$). The green curve shows projections that meet ITRS requirements with the higher mobility and with $v_{\text{sat}} = 3.2 \times 10^6$ cm s$^{-1}$, not yet demonstrated experimentally.
4. Conclusions

In summary, this work presents an in-depth analysis of CVD-grown 1L MoS$_2$ FETs with material characteristics comparable to those of exfoliated devices, achieving the highest current density reported to date ($\approx 270 \mu A \mu m^{-1}$ or 44 MA cm$^{-2}$). We show that the TLM approach provides rigorous estimates of both mobility and contact resistance, obtaining $R_c \approx 6.5 \Omega \mu m$ and $R_D \approx 10^{-2} \Omega cm^2$ here, at room temperature and moderate carrier densities, which could be reduced further with contact engineering. We use simulations to match our experimental results and to provide insights into how 1L MoS$_2$ devices could behave when properly scaled down. It is revealed that $v_{sat}$ plays a greater role than $\mu_{eff}$ in determining $I_{ON}$ for aggressively scaled devices. Simulations also reveal that 1L MoS$_2$ could nearly meet ITRS requirements at sub-20 nm channel lengths, but further advancements in contact, dielectric, and carrier velocity engineering are still needed.

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Supporting information

Experimental setup of reported and optimized growth conditions, forward and backward $I_{DS}-V_{DS}$ sweeps showing minimal hysteresis, low-field $I_{DS}-V_{DS}$ sweeps showing linear behavior, plots of $L_I$ versus $n$ for various $T$ and $V_{DS}$ extractions of field-effect mobility, simulations of extracted mobility values, summary plot of reported current density versus reported mobility in 1L CVD MoS$_2$, mean free path versus mobility, and illustrations of quantum confinement effects in 2D and bulk materials.

Author contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interests.

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