Abstract—In this work, a double synchronous unified virtual oscillator controller is proposed for grid-forming voltage source converters to achieve synchronization to the fundamental frequency positive- and negative-sequence components of unbalanced grid voltage without any phase-locked loop. The proposed controller leverages a positive-sequence virtual oscillator and a negative-sequence virtual oscillator, a double-sequence current reference generator, and a double-sequence vector limiter. Under fault conditions, the controller enables to limit the converter output current below/at the maximum value allowable by the converter hardware while retaining synchronization regardless of the nature of grid faults. Consequently, symmetrical and asymmetrical fault ride-through can be achieved without the need for switching to a backup controller. This article presents the implementation and detailed analysis of the double-synchronous structure, which enables simultaneous synchronization to both sequences during current-unconstrained and -constrained operations. Validation of the proposed controller is provided through laboratory hardware experiments.

Index Terms—Asymmetrical fault ride-through, fault-ride-through (FRT), grid-forming (GFM) converter, unified virtual oscillator controller (uVOC).

I. INTRODUCTION

EARLY works on fault-ride-through (FRT) by grid-forming (GFM) converters rely on a separate set of backup controllers that employ phase-locked-loop (PLL)-based vector current controllers; a controller switch is performed as soon as a fault is detected [1]. Majority of reported literature focus on symmetrical FRT [2]. However, asymmetrical faults, such as single-line-to-ground (SLG) and double-line-to-ground (DLG) faults, are more frequent in real systems.

Asymmetrical FRT in GFM applications can be achieved by switching to a decoupled double synchronous reference frame PLL-based vector current controller under fault. However, synchronization issues of PLLs, specifically under weak grids, are well documented in the literature [3]. A number of PLL-free asymmetrical FRT approaches have been reported. In [4], instead of synchronizing to the unbalanced grid, prefault values of the frequency and voltage magnitudes are used under faults. In [5], the outer power control loops synchronize to the positive-sequence voltage while an adaptive virtual impedance combined with inner voltage and current control loops are used to limit output current under asymmetrical faults.

Nonlinear time domain controllers, such as virtual oscillator control (VOC) and dispatchable virtual oscillator (dVOC), are another class of emerging GFM controllers that can guarantee almost global synchronization in arbitrary N-converter networks with zero inertia [6], [7]. A unified virtual oscillator controller (uVOC) has been recently proposed that inherits the rigorous theoretical foundation and asymptotic synchronization guarantee of dVOC [8]. These class of controllers, in their original form, are first-order controllers, i.e., provide no inertia, but eliminate critical clearing time/angle constraints while recovering from large grid transients/faults [9]. However, virtual inertia emulation can be integrated with virtual oscillator-based controllers, if desired [10]. uVOC offers ride-through capability under symmetrical grid faults; however, under unbalanced grid conditions, such as asymmetrical faults, the positive-sequence-only configuration of uVOC fails to limit/control the negative sequence current at the converter output; therefore, no fault current contribution and/or voltage support is afforded in the negative sequence. To facilitate asymmetrical FRT by virtual oscillator-based controllers, the double-synchronous uVOC (dsuVOC) was developed [11]. However, the underlying theory of double-sequence synchronization and experimental demonstration under current-constrained and -unconstrained conditions have not been reported. The key contributions of this work can be
summarized as follows: 1) theoretical formulation for demonstrating that despite nonlinear coupling between the positive- and negative-sequence space-vector oscillators (SVOs), synchronizing action is retained simultaneously in both sequences through voltage and frequency droop responses under current-unconstrained and -constrained operations, and 2) experimental validation of the proposed unbalanced FRT controller.

II. ASYMMETRICAL FRT WITH dsUVOC

Fig. 1 shows a grid-tied voltage source converter (VSC) fed by a Δ-Yg transformer. The converter operation under upstream asymmetrical faults, marked by the red arrow, is of interest. Note that the Δ feeder connection prevents zero-sequence currents at the point-of-coupling (PoC), and hence, only positive- and negative-sequence fault currents are of interest. The dsUVOC implementation in a grid-tied VSC is shown in Fig. 1, where either the converter-side current \( i_1 \) or the grid-side current \( i_2 \) feedback can be used. No voltage or current reference tracking loops are used. The dsUVOC output is directly used by the pulsedwidth modulator (PWM) unit. The detailed dsUVOC structure is shown in Fig. 2, which consists of a double-sequence current reference generator, a double-sequence vector limiter, a positive-sequence SVO, and a negative-sequence SVO. Furthermore, an active resistance \( R_0 \) and virtual impedance \( Z_v(s) \) are used. The proposed dsUVOC utilizes power synchronization in both positive and negative sequences.

A. Double-Sequence Current Reference Generation

For a given set of real and reactive power references \( P_0 \) and \( Q_0 \), respectively, the current references in stationary reference frame are generated using the controller internal states \( v_+ \) and \( v_- \). Equations describing the dynamics of these internal states are presented in Section II-C. The sequence current references \( i_{0+} \) and \( i_{0-} \) are generated from \( v_+ = v_{a+} + jv_{b+} \) and \( v_- = v_{a-} + jv_{b-} \) as

\[
\begin{bmatrix}
i_{a+} \\
i_{b+} \\
i_{a-} \\
i_{b-}
\end{bmatrix} = \frac{2}{3} \begin{bmatrix}
k_{p+}v_{a+} & k_{q+}v_{b+} \\
k_{p+}v_{b+} & -k_{q+}v_{a+} \\
k_{p-}v_{a-} & k_{q-}v_{b-} \\
k_{p-}v_{b-} & -k_{q-}v_{a-}
\end{bmatrix} \begin{bmatrix}P_0/D_P \\
Q_0/D_Q \end{bmatrix}
\]

(1)

where \( D_P = k_{p+}||v_+||^2 + k_{p-}||v_-||^2 \) and \( D_Q = k_{q+}||v_+||^2 + k_{q-}||v_-||^2 \). Different control objectives can be fulfilled with proper choice of \( k_{p+}, k_{p-}, k_{q+}, \) and \( k_{q-} \) [12]. Note that in the following analysis, subscript 0 denotes the nominal value/ set point of the respective parameter/ state; peak amplitude and rms values of a symmetrical space vector are denoted as \( \hat{V}_+ = ||v_+|| = (v_{a+}^2 + v_{b+}^2)^{0.5} \) and \( \hat{V}_+ = \hat{V}_+ / \sqrt{2} \), respectively.

B. Double Sequence Vector Limiter

The instantaneous sum of the two inversely rotating vectors \( i_{0+} \) and \( i_{0-} \) results in an elliptical trajectory of the total current reference vector \( i_0 \). To ensure that the rms current in any phase does not exceed the maximum value \( I_{m} \) allowable by the converter hardware, the current reference is saturated as

\[
i_0 = \text{max}\{L_{0+} i_{0+}, L_{0-} i_{0-}\} \leq I_{m}
\]

(2)

where \( L_{0+} = \text{rms} \{i_{0+}\} \). First, the rms magnitudes of the three-phase unsaturated current references are obtained as

\[
i_{x0} = \left(\left(\|i_{0+}\|^2 + \|i_{0-}\|^2 + 2(\xi_1\cos 2\gamma - \xi_2 \sin 2\gamma)\right)/2\right)^{1/2}
\]

(3)

where \( \xi_1 = (i_{c0+} - i_{b0+} - i_{a0+}) \) and \( \xi_2 = (i_{b0+} + i_{c0+} - i_{a0+}) \), and \( \gamma = \{0, -2\pi/3, 2\pi/3\} \) for phase \( x = a, b, \) and \( c \), respectively. Next, the saturated current references are obtained as

\[
i_{0+} i_{0-} = k_{sat}\{i_{0+} i_{0-}\}^T; \quad k_{sat} = I_{m}/I_{max}
\]

(4)

where \( I_{max} = \text{max}\{I_{0+}, I_{00}, I_{c0}\} \).

C. Positive- and Negative-Sequence SVOs

The double-sequence SVOs are implemented as

\[
\hat{v}_+ = j\omega_0v_+ + j\eta_+(\hat{i}_{0+} - \hat{i}_+) + \mu_+(\hat{v}_{\theta}^2 - ||v_+||^2)v_+
\]

\[
\hat{v}_- = -j\omega_0v_- - j\eta_-(\hat{i}_{0-} - \hat{i}_-) + \mu_-(\hat{v}_{\theta}^2 - ||v_-||^2)v_-
\]

(5a)

(5b)

where positive- and negative-sequence current components \( i_+ = i_{a+} + ji_{b+} \) and \( i_- = i_{a-} + ji_{b-} \) are extracted from the converter output current \( i = i_a + ji_b \) as

\[
i_{a+} = 0.5(i_a - i_b); \quad i_{b+} = 0.5(i_b + i_a)
\]

\[
i_{a-} = 0.5(i_a + i_b); \quad i_{b-} = 0.5(i_b - i_a)
\]

(6)

where \( (.)_\perp \) denotes the orthogonal version of the respective signal obtained by delaying the original signal by \( T_0/4 \), where \( T_0 \) is the fundamental period. \( \eta_+ \) and \( \mu_+ \) are the synchronization and magnitude correction gains and are defined as

\[
\eta_+ = \eta_+ = (1 + x_T/\tau_f)\eta_0; \quad \mu_+ = \mu_+ = (1 - x_T)\mu_0.
\]

(7)

The nominal values \( \eta_0 \) and \( \mu_0 \) are chosen following the design guidelines for positive-sequence-oriented control presented in [8], where \( x_T \) is the mode transition signal and \( \tau_f \) defines the settling time.

III. DOUBLE-SEQUENCE SYNCHRONIZATION

A synchronous generator achieves self-synchronization with the rest of the electrical grid through a transient exchange of power; this natural synchronization process through power-frequency drooping is termed as power synchronization. Prior
to delving into the power synchronization of SVOs, it is insightful to examine the time derivative of a complex space vector \( \mathbf{u} = \mathbf{U} e^{j\omega t} = u_\alpha + j u_\beta \), given as

\[
\frac{d}{dt} (\mathbf{u}) = \frac{1}{j\omega} \mathbf{U} \frac{d\mathbf{U}}{dt} + j\omega \mathbf{u} = \Omega \mathbf{u}
\]

where the real and imaginary parts of \( \Omega \) denote the normalized rate of change of amplitude and the instantaneous frequency of rotation, respectively. First, to illustrate the power synchronization process of dsUVOC in the positive sequence, we consider \( k_{p+} = 1, k_{p-} = 0, k_{q+} = 1, k_{q-} = 0 \); the negative-sequence SVO and the double-sequence vector limiter on the current reference are excluded. The positive-sequence SVO dynamics, given by (5a), can be rearranged as

\[
\mathbf{v}_+ = [j(\omega_0 + \eta_+ e_{iP+}) + (\mu_+ e_{v+} - \eta_+ e_{iQ+})] \mathbf{v}_+
\]

where

\[
e_{iP+} = \frac{2(P_0 - P_+)}{3||\mathbf{v}_+||^2}; \quad e_{iQ+} = \frac{-2(Q_0 - Q_+)}{3||\mathbf{v}_+||^2};
\]

\[
P_+ + jQ_+ = \mathbf{v}_+ \mathbf{i}_+^\prime; \quad P_0 + jQ_0 = \mathbf{v}_+ \mathbf{i}_0^\prime
\]

\[
e_{v+} = \mathbf{v}_0^2 - ||\mathbf{v}_+||^2
\]

where \((\cdot)^\prime\) denotes complex conjugate of the respective complex vector. Now, we consider a synchronous reference frame aligned with the positive-sequence SVO output voltage vector \( \mathbf{v}_+ \). For an arbitrary positive-sequence grid voltage vector \( \mathbf{v}_g^+ \) and a current error \( e_{i+} = i_{0+} - i_+ \), a graphical representation of the SVO dynamics given by (9) is shown in Fig. 3, where the \( \alpha \)- and \( \beta \)-axes mark the stationary reference frame. Following (8), the normalized rate of change of voltage magnitude \( V_+ (= ||\mathbf{v}_+||/\sqrt{2}) \) and the instantaneous frequency of rotation can be derived as

\[
\omega_+ = \omega_0 + \frac{\eta_+}{3V_+^2} (P_0 - P_+)
\]

\[
\dot{V}_+ = 2\mu_+ V_+ (V_0^2 - V_+^2) + \frac{\eta_+}{3V_+} (Q_0 - Q_+).
\]

Evidently, instantaneous droop responses, such as \( P_+ \) versus \( \omega_+ \) and \( Q_+ \) versus \( V_+^2 \), are observed on the SVO output voltage vector along the synchronous \( q_+ \)- and \( d_+ \)-axes, respectively, which facilitate the power synchronization to the positive-sequence grid voltage vector \( \mathbf{v}_g^+ \).

Following similar notations, and assuming \( k_{p+} = 0, k_{p-} = 1, k_{q+} = 0, k_{q-} = 1 \), the negative-sequence SVO dynamics in (5b) can be rearranged as

\[
\dot{\mathbf{v}}_- = [-j(\omega_0 + \eta_- e_{iP-}) + (\mu_- e_{v-} - \eta_- e_{iQ-})] \mathbf{v}_-
\]

where

\[
e_{iP-} = \frac{2(P_0 - P_-)}{3||\mathbf{v}_-||^2}; \quad e_{iQ-} = \frac{-2(Q_0 - Q_-)}{3||\mathbf{v}_-||^2};
\]

\[
P_- + jQ_- = \mathbf{v}_- \mathbf{i}_-^\prime; \quad P_0 + jQ_0 = \mathbf{v}_- \mathbf{i}_0^\prime
\]

\[
e_{v-} = \mathbf{v}_0^2 - ||\mathbf{v}_-||^2.
\]

For an arbitrary negative-sequence grid voltage vector \( \mathbf{v}_g^- \) and a current error \( e_{i-} = i_{0-} - i_- \), a graphical representation of the SVO dynamics in the negative-sequence synchronous frame aligned with \( v_- \) is shown in Fig. 4. The dynamics along the \( q_- \)- and the \( d_- \)-axes define the instantaneous \( P_- \) versus \( \omega_- \) and \( Q_- \) versus \( V_-^2 \), droop responses, respectively, and can be represented as

\[
\omega_- = -\frac{-\eta_-}{3V_-^2} (P_0 - P_-)
\]

\[
\dot{V}_- = 2\mu_- V_- (V_0^2 - V_-^2) + \frac{-\eta_-}{3V_-} (Q_0 - Q_-).
\]

These two droop responses in tandem facilitate synchronization to the negative-sequence grid voltage vector \( \mathbf{v}_g^- \). Note that the negative-sequence voltage reference is set as \( V_0 = 0 \), and under normal operation, the power references are chosen as \( P_0 = 0 \) and \( Q_0 = 0 \), which leads to \( i_{0-} = 0 \); for a balanced grid, \( \mathbf{v}_g^- = 0 \), which results in \( v_- = 0 \) and \( i_- = 0 \).

Using the full form of the current reference generation, given by (1), and the double-sequence vector limiter, given by (4), the overall controller dynamics can be derived as the simultaneous
Fig. 5. Simulated droop behavior in response to grid-frequency change.

Evidently, the $P - \omega$ and the $Q - V^2$ droop responses in both sequences are unaffected during current-constrained operation; only the power references are scaled proportionately to keep the output current within limit. Furthermore, the coupling among the two sequences exists through the power references. This enables the simultaneous double synchronous operation of the proposed controller.

IV. SIMULATION RESULTS

To evaluate the droop response, the proposed controller is subjected to step changes in grid frequency. The corresponding simulated result is shown in Fig. 5, which demonstrates the $P - \omega$ droop response. Fig. 6 illustrates the control response, i.e., $Q - V$ droop response, when the positive sequence component of the grid voltage is varied. In the presence of negative-sequence component in the grid voltage, the proposed controller exhibits a $Q - V$ droop response as shown in Fig. 7 to alleviate the voltage unbalance, i.e., consumes reactive power in the negative sequence to lower the negative-sequence terminal voltage.

V. EXPERIMENTAL RESULTS

The laboratory test setup, shown in Fig. 8, includes a 400 V 2.75 kW battery energy storage system and a 208 V 60 Hz 3.3 kVA three-phase VSC; California Instruments’ MX30pi programmable ac source is used as the grid emulator. The control parameters are chosen as $\eta_0 = 45.72$, $\mu_0 = 8.4 \times 10^{-4}$, $R_0 = 0.38$ per unit (p.u.), $\tau_f = 0.07$, and $I_m = 1.2$ p.u. Texas Instruments’ C2000 digital signal processor TMS320F28379D is used for digital control implementation. Along with the proposed controller, an observer-based controller is used to actively damp potential resonances caused by the $LCL$ input filter [13]. An adaptive presynchronization strategy reported in [14] is used to achieve grid connection during start-up. Note that only the terminal voltage $v_{poc}$ and the converter side current $i_1$ (see Fig. 1) are measured for overall control implementation.

A. SLG Fault

An SLG fault is emulated by introducing a sudden voltage sag in one phase by the grid emulator. Figs. 9 and 10 show the test waveform and the postprocessed analysis, respectively, of the response to an SLG fault emulated by a sudden voltage sag on phase A from 1 to 0.1 p.u., whereas the reference is set as $P_0 = 0.2$ p.u.
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and the controller substantially lowers the allowable value of both symmetrical and asymmetrical faults. The proposed controller has been validated through laboratory hardware experiments.

VI. Conclusion

This work presents the first asymmetrical fault-ride-through solution implemented with a virtual oscillator-based controllers for grid forming converters. The proposed dsUVOC can achieve simultaneous synchronization in both positive and negative sequence, which enables synchronization to balanced, distorted, or unbalanced grids. In addition, it eliminates the need to switching to a backup controller and subsequent use of a PLL during a fault event. The double sequence synchronization capability of the proposed controller has been illustrated through sequence decoupled as well as positive- and negative-sequence coupled space vector analysis. This enhanced synchronization capability, combined with fast overcurrent limiting, facilitates ride through of both symmetrical and asymmetrical faults. The proposed controller has been validated through laboratory hardware experiments.

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