Hardware Decoders for Polar Codes: An Overview

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Abstract—Polar codes are an exciting new class of error correcting codes that achieve the symmetric capacity of memoryless channels. Many decoding algorithms were developed and implemented, addressing various application requirements: from error-correction performance rivaling that of LDPC codes to very high throughput or low-complexity decoders. In this work, we review the state of the art in polar decoders implementing the successive-cancellation, belief propagation, and list decoding algorithms, illustrating their advantages.

I. INTRODUCTION

Polar codes are the first codes with an explicit construction to asymptotically achieve the symmetric capacity of memoryless channels using a low-complexity, successive-cancellation (SC), decoding algorithm [1]. Additionally, they were shown to be free of error floors when used with binary-input symmetric memoryless channel, and are therefore attractive for wired communications and storage systems [2].

The serial nature of SC decoding limits the throughput of its implementations. Two approaches are used in literature to overcome the sequential nature of SC: exploiting the polar code structure to estimate multiple bits in parallel while still using SC-based algorithms [3], [4], and using the belief propagation (BP) decoding algorithm with parallel message passing [5], [6]. Hardware decoders implementing these algorithms reach throughputs of multiple Gbps and can exceed 100 Gbps when unrolling is used [7], [8].

While SC and BP based decoders are fast and efficient, their error-correction performance can be inferior to that of other modern codes such as low-density parity-check (LDPC) codes. However, when polar codes are decoded using the successive cancellation list (SCL) decoding algorithm [9], their error-correction performance was shown to exceed that of LDPC codes used in recent wireless communication standards [2].

In this paper, we review the state of the art in hardware polar decoder implementations. We start with a review of polar codes in Section III. SC-based implementations are discussed in Section IV and BP-based decoders in Section V. Finally, SCL decoder implementations are reviewed in Section V.

II. BACKGROUND

Polar codes are recursively constructed from a $2 \times 2$ polarizing transformation $F = \begin{bmatrix} 0 & 1 \\ 1 & 1 \end{bmatrix}$: a vector $u_0^N$ of two bits $u_0$ and $u_1$ is encoded using $F$ to yield a polar codeword. When estimating $u_0$ and $u_1$ using SC decoding, the probability of correctly estimating $u_0$ decreases while that of $u_1$ increases compared to an uncoded vector. This transform is recursively applied log $N$ times to encode $N$ bits. As $N \rightarrow \infty$ the probability of correct detection approaches 1.0 (reliable) or 0.5 (unreliable) and the proportion of reliable bits approaches the symmetric capacity of the underlying memoryless channel.

To construct an $(N, k)$ polar code, the $k$ most reliable bits in $u_0^{N-1}$ are used to carry the information bits; while the remaining bits are frozen by setting them to a predetermined value—usually ‘0’. Fig. 1a shows the graph representation of an $(8, 4)$ polar code where the frozen and information bits are labeled in gray and black, respectively. Due to the recursive nature of polar code construction, binary trees are a natural representation for these codes. In Fig. 1b the white (black) leaf nodes correspond to frozen (information) bits; whereas the gray nodes correspond to the polar transformations encircled in Fig. 1a. Each sub-tree rooted at a node of depth $\log_2 N$, where leaf nodes have a depth of 0, corresponds to constituent polar codes of length $N$.

Quantization in hardware decoders varies based on polar code length and the decoding algorithm used. Many implementations, e.g. [4], use fewer bits for channel reliability information than for internal values. SCL decoders [10] are less tolerant of value saturation and therefore require more quantization bits than their SC counterparts. Finally, longer codes require more integer bits to represent the wider range of their internal values.

III. SUCCESSIVE CANCELLATION-BASED DECODERS

In this section we briefly go over the algorithms and architectures that led to the fastest hardware decoder implementations based on the successive-cancellation (SC) algorithm.
A. SC-based Decoding Algorithms

The SC decoding algorithm traverses the entire polar code tree, e.g. Fig. 1[A] depth first, visiting all leaf nodes. To reduce latency, the simplified successive-cancellation (SSC) decoding algorithm does not traverse sub-trees whose leaves all correspond to frozen or information bits. Instead, it applies a decision rule immediately [3]. Similarly, constrained maximum-likelihood decoding of multiple bits can be employed to trim the decoder tree [11]–[13].

The Fast-SSC decoding algorithm extends the SSC algorithm by applying low-complexity decoding rules when encountering certain types of sub-trees [4], [14]. Specialized decoding of repetition and single-parity-check (SPC) codes are the most notable examples and reduce the decoder-tree size, significantly reducing the number of calculations and increasing the decoding speed.

B. Fast-SSC Decoders

The configurable hardware implementation of the Fast-SSC algorithm resembles a processor [4]. It features memory for the soft and hard internal values and buffers to allow uninterrupted operation while the next frame is loaded and the previously estimated codeword offloaded. The decoder accepts a set of instructions representing the desired polar code. These instructions are utilized by the controller to generate the load and store addresses as well as the ‘select’ signals to route the data in and out of the different processing units.

C. Unrolled Decoders

First applied to polar decoders in [7] and [15], improved and generalized in [8], unrolling is a technique that has been successfully applied to other types of decoders before, such as the high-speed LDPC decoders of [16].

An unrolled polar decoder instantiates processing elements for each and every node in the decoder tree of a specific polar code. This way, each processing element can process a different received vector. By inserting registers at each decoder stage, a new frame can be loaded and an estimated codeword output at every clock cycle. While this deep-pipelined architecture provides very high throughput, it requires a significant amount of memory for data persistence that increases with the number of clock cycles. The period at which estimated codewords are output is also of fixed length.

D. Implementation Results

Table I shows FPGA implementation results for both configurable and unrolled Fast-SSC decoders. The decoder of [4] was the first polar decoder to reach a throughput of 1 Gbps. The decoder of [14] is an improvement over [4] where support for other constituent codes was added to improve the throughput in decoding lower-rate codes. The last three rows of Table I are results for the unrolled decoder of [8] showing that throughputs in the hundreds of Gbps are achievable at the cost of area and resource usage.

| Impl. | N  | R  | LUTs | Regs. | f (MHz) | T/P (Gbps) | Latency (μs) |
|-------|----|----|------|-------|---------|------------|--------------|
| [4]   | 32,768 | 0.9 | 25,866 | 7,209 | 536 | 108 | 1.2 | 26.4 |
| [13]  | 1,024 | 0.5 | 24,821 | 5,823 | 36 | 103 | 0.6 | 1.6 |
| [6]   | 1,024 | 0.5 | 86,998 | 65,618 | 0 | 218 | 4.5 | 1.7 |
| [9]   | 1,024 | 0.5 | 136,874 | 188,071 | 84 | 248 | 254.1 | 1.5 |
| [10]  | 2,048 | 0.5 | 217,127 | 261,112 | 5,362 | 203 | 415.7 | 3.2 |

IV. Belief Propagation Decoders

Belief propagation (BP) decoding of polar codes is a message passing algorithm over the graph representation [11], achieving similar error-correction performance to SC decoding. Soft messages are iteratively propagated in the graph until a stopping criterion is met (e.g. the maximum number of iterations is reached). Then, threshold detection is applied to the left-hand-side messages to generate the estimated codeword. This section reviews different design aspects of BP decoders.

A. Fast BP-Based Decoders

From Fig. 1[A] the graph of polar codes of length N consists of log₂N columns, each with 2N incident edges. A BP decoder traverses the graph column-by-column and each time 2N soft messages at the corresponding edges are updated. If the graph is traversed in a round-trip manner, a single-column decoder takes 2 log₂N − 1 clock cycles to complete an iteration. A double-column architecture was proposed in [6] where the operations of two adjacent columns are merged in one clock cycle, effectively reducing in half the latency per iteration. Although the critical path was shown to increase by 14% compared to that of the single-column architecture, the decoding throughput was improved by more than 40%.

The graph can also be traversed uni-directionally, e.g., only activating columns from left to right. Under this schedule, data dependency is relaxed. Taking Fig. 1[A] for example, the messages updated by the left-most column c₀ of the current iteration are not used by the right-most column c₂ of the next iteration. Hence, the operations of these two columns can be simultaneously executed and one clock cycle is saved. More generally, an iteration-level overlapping schedule was proposed in [17]. By increasing the hardware complexity to compute 1/2 log₂N columns simultaneously, the latency of a uni-directional BP decoder is reduced from J log₂N clock cycles to 2J + log₂N − 2, where J denotes the number of iterations.

B. Low-Complexity BP Decoders

In [18], a low-complexity variant of the BP decoding algorithm called soft cancellation (SCAN) was proposed. Under that algorithm, soft messages propagate according to the schedule of SC decoding, resulting in an increased latency in O(N) clock cycles. However, the message propagation of SCAN was shown to be efficient and its overall complexity at low SNR regime was reduced by an order of magnitude compared to that of regular BP decoding.
Similar to iterative decoders for LDPC or turbo codes, early stopping schemes can be used in BP decoders for polar codes. In [19], threshold detections on messages are made after each iteration. When they satisfy certain criteria, decoding is stopped immediately. Furthermore, messages related to sub-graphs are checked in [20] such that the operations in those sub-graphs can be stopped earlier. As a result, with the method of [19], the average decoding complexity is reduced by around 30% with negligible performance degradation. The method in [20] further reduces the average complexity by 40%.

C. Memory-Efficient BP Decoders

It was observed in [6] that, if a single-column decoder follows a round-trip schedule, $N$ messages instead of $2N$ need to be updated each time. Thus, the memory requirement is reduced in half. In [21], two adjacent columns are combined into one so that intermediate messages need not to be stored. However, the corresponding message updating rules have to be modified accordingly. As a result, the overall memory usage is significantly reduced, at the cost of some combinational logic overhead.

D. Implementation Results

Table II summarizes the ASIC implementation results of different BP decoders. It can be seen that, due to their parallel nature, the state of the art is already capable of achieving throughputs of multiple Gbps. However, even at high SNR, the average iteration number is high resulting in a greater computational complexity than its SC-based counterparts.

| Implementation | [6] | [19] | [21] |
|----------------|-----|-----|-----|
| Architecture   | double-col. | overlapped | col.-combined |
| Schedule       | round-trip | uni-direction | round-trip |
| Technology     | 65 nm | 45 nm | 45 nm |
| Area (mm$^2$)  | 1.476 | N/A | 0.747 |
| Supply (V)     | 1.0 | 1.1 | N/A |
| $f$ (MHz)      | 300 | 500 | 197 |
| Max. iter. #   | 15 | 40 | 15 |
| T/P (Gbps)     | 2.05 | 2.9 | 1.683 |
| T/P (Gbps)/@SNR| 6.57@4.0 dB | 23.0@3.5 dB | N/A |
| T/P (Gbps)/@SNR| 4.68@4.0 dB | 4.5@3.5 dB | N/A |

LDPC: $R = 1/2$, $R = 2/3$, $R = 3/4$, $R = 5/6$
Polar-CRC: $R = 1/2$, $R = 2/3$, $R = 3/4$, $R = 5/6$

Fig. 2. Frame error rate of polar codes of length $N = 1,024$ under SCL decoding with $L = 2$ and an 8-bit CRC compared with the LDPC codes of the IEEE 802.11n standard of length $N = 1,944$ under offset min-sum decoding with a flooding schedule and a maximum of 10 iterations. All simulations were performed using BPSK modulation over an AWGN channel.

A. Exact LLR-Based SCL Decoding

The original description of SCL decoding was made using channel likelihoods [9]. While such a high-level description is valid, these likelihoods can become very small during the decoding process, resulting in numerical precision problems and inefficient hardware implementations. The first hardware implementations of SCL decoding used log-likelihoods to partially overcome these problems [22], [23]. An equivalent, but much more efficient, description of SCL decoding in terms of LLRs and an LLR-based path metric was presented in [10]. [24]. LLR-based SCL decoding leads to the most efficient hardware implementation of SCL decoding [10].

B. Path Metric Sorting

A computationally challenging step of SCL decoding is that of path metric sorting, where the $L$ best path metrics have to be selected among $2L$ possible metrics. The properties of the LLR-based path metric were exploited in [25] in order to significantly reduce the complexity and the critical path of the metric sorting blocks, while still performing exact sorting.

In a different approach, path metrics were approximately sorted with double thresholding method proposed in [26]. It compares $2L$ path metrics with two thresholds, $AT$ and $RT$. A path survives if its metric is smaller than $AT$. After it, the paths with metrics in between $AT$ and $RT$ are randomly selected to fill up the list of $L$ surviving paths. This method significantly reduces the critical path of metric sorting, especially for a large $L$. The problem of path metric sorting is even more pronounced in decoders that employ multi-bit decision, such as [12], [27], since in this case the $L$ best metrics out of up to $2^qL$ candidate metrics have to be selected, where $b$ is the number of bits that are decoded simultaneously. To this end, an approximate two-stage sorting unit was proposed in [13], where the best $q$ out of $2^q$ successor paths are first selected for each path, and then the

$^1$The implementation is “exact” up to quantization loss and min-sum approximation loss, which are common losses to all hardware implementations.
best L paths are selected among the qL paths resulting from the first step. This approach reduces the sorting complexity at the cost of a small performance degradation.

C. Approximate Tree Pruning in LLR-Based SCL Decoding

Since SCL decoding heavily relies on SC decoding for the computation of the path metrics, one may expect that the pruning techniques described in Section III should be applicable to SCL decoding as well. Unfortunately, in order to update the LLR-based path metric of (10), all the LLRs produced by the leaves of the decoder tree are required and these node computations cannot be pruned if one wants to implement exact SCL decoding. Nevertheless, [27] describes an approximate SCL decoding algorithm which is based on tree pruning that simply ignores some of the path metric updates corresponding to computation tree leaves. The resulting performance degradation is small and an outline of a hardware architecture is presented which can achieve a throughput of slightly over 1 Gbps for a polar code of length N = 8192 and rate R = 0.5 using SCL decoding with L = 4.

D. Implementation Results

Table III summarizes the implementation results of the aforementioned state-of-the-art SCL decoder architectures. While SCL decoders have an error-correction performance that is close to (or even better than) LDPC codes, we observe that the implementation of multi-Gbps SCL decoders remains a challenging problem.

VI. Conclusion

In this paper, we reviewed the state of the art in polar decoders implementing the successive-cancellation, list, and belief propagation decoding algorithms. The advantages of the different algorithms were illustrated. It was shown that the many decoding algorithms were developed and implemented to address various application requirements: from error-correction performance rivaling that of LDPC codes to very high throughput or low-complexity decoders.

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