Performance analysis of reduced switch ladder type multilevel inverter using various modulation control strategies

Vishwajith N¹, S Nagaraja Rao² and Sachin S²
¹Department of Electronics and Communication Engineering, M.S. Ramaiah University of Applied Sciences, Bengaluru, India.
²Department of Electrical Engineering, M.S. Ramaiah University of Applied Sciences, Bengaluru, India.

Email: vishwajithbhat@gmail.com, nagarajarao.ee.et@msruas.ac.in and sachins.ee.et@msruas.ac.in

Abstract. Multi-Level Inverters (MLI) are finding applications in UPS, drives, Grid interfaces because of dynamic output voltage control capability. In this paper a nine level single phase MLI topology with optimized switches is proposed. Increased output level helps in smoothening the output waveform along with reduced THD and eliminates need of filtering circuits. Proposed Reduced Switch Ladder Type MLI (RSL-MLI) topology consists of four DC power sources and nine switches for single phase inverter. When compared to conventional MLIs for same nine output levels, this topology has less number of devices making it cost effective. Both, high frequency switching pulse width modulation and fundamental frequency switching modulation methods are used for simulation of proposed nine level RSL-MLI topology. Output voltage waveform, THD are analysed using Simulink and equated to validate the performance of planned topology. Further, simulation is carried for five and seven levels of output voltages and THD are analysed.

1. Introduction

Inverters are used to change DC voltage to AC voltage using power electronic switches. Conventional inverters produce two level of output voltages: +Vdc/2 and -Vdc/2 in case of half bridge inverter and +Vdc and -Vdc for full bridge inverter. These inverters have following drawbacks [1]: (i) Harmonics are created in output voltage and current, influences electrical and mechanical parts connected to the system; (ii) Harmonics produce excessive heating at load side motor; (iii) Increased switching losses which reduce overall system performance; (iv) Reduced lifespan of system.

Multi-Level Inverters (MLIs) are getting acceptance in industries as they overcome the drawbacks of two level inverters and improve the performance. They can produce more than two levels of output voltages, which will give smooth output waveform [2]. They use multiple switches depending on topology and have lower harmonic distortions than two level inverters [3]. MLIs are ideal for interfacing Power grids to Distributed power generation, because of lower harmonic and dynamic output voltage conversion capability, i.e. conversion to required voltage level and frequency [4-6]. To meet increased energy demand and go green initiative, renewable energy resources are considered for power generation [7-10].

Solar energy is free from pollution, has wider range of availability worldwide and is a practically limitless source of power. It can be produced locally, connected to power grid network, and can be
used as Distributed generators. PV cells are used to convert solar energy to DC voltage, but these are of low magnitude. These low voltages are added and changed to AC voltage of chosen frequency and amplitude using MLIs and connected to Power grid [8-10].

There are three types conventional MLIs – (i) Diode Clamped MLI: This has series arrangement of switches, o/p voltage levels are obtained by changing the switching sequence [5]. Voltage regulation or clamping in dc bus is achieved by using diodes to accomplish required output voltage steps. Voltage balancing between DC link capacitor is challenge [3]. (ii) Capacitor Clamped (Flying Capacitors) MLI – In flying capacitor inverter, voltage regulation is achieved using capacitors instead of diodes. The incremental voltage magnitude within 2 capacitors governs the scale of output voltage level. This setup requires several capacitors, making system expensive and bulky [3]. (iii) Cascaded H Bridge MLI: This is series connection of several single-phase full bridge inverters [6]. Required number or levels of o/p voltages can be obtained by adding H bridge inverters in series [7]. Requires separate DC sources for each inverter set, driving need for large isolation transformer [3].

With increase in number of output levels, these MLIs need more number of switches, DC sources, diodes, capacitors [11-13]. This leads to increase in control complexity, overall system size and installation area. In turn overall system cost becomes high. To overcome this drawback, many MLI topologies with reduced number of switches and source voltages have been developed [14-16]. These topologies offer same or improved performance in terms of output and THD when contrasted with traditional MLIs. In this paper a nine level single phase MLI topology with less number of switching and dc sources is put forth, and performance is analysed. TMC Unipolar SPWM, Equal phase Method and Nearest Level Control (NLC) methods are used as modulation strategy. THD levels with all three techniques are analysed using Simulink. Results are compared to verify the performance.

2. Proposed MLI Topology

Proposed topology [1] consists of a Level generator (to generate output levels) and Polarity generator (to get positive and negative half cycles in output) circuits. Figure 1 is the block diagram of planned Reduced Switch Ladder Type Multilevel Inverter (RSL-MLI). Required output levels, m, can be obtained using level generator. It consists of switches and voltage sources based on required levels. Figure 2 depicts planned RSL-MLI which is for m = 9 output levels. Switches T1 to T5 are the levels generator switches. Different modulation techniques can be used to turn on and off these switches. Switches will turn on as per the switching table sequence in table 1, where 0 is off and 1 is on, and corresponding voltage levels will be generated. This will be unipolar DC voltage. It will be input to the Polarity generator which is a H-Bridge circuit with constant pulses of low switching frequency as 50 Hz. This will convert alternate half cycles of level generator output to negative voltage hence giving sinusoidal waveform output. Switches P1, P2 are for positive cycle, N1, N2 are for negative half cycles.

![RSL-MLI block diagram](image-url)
Since all the dc voltage sources are equal, maximum output voltage \[8\], \(V_{omax}\), of RSL-MLI can be calculated using equation (1).

\[
V_{omax} = \sum_{i=1}^{m-1} V_{dc}
\]  

(1)

Voltages of each step, \(n\), either positive or negative, can be obtained using equations (2) and (3).

\[
V_{omax} = \sum_{i=1}^{n} + V_{dc} \quad \text{if } P1, P2 = 1
\]  

(2)

\[
V_{omax} = \sum_{i=1}^{n} - V_{dc} \quad \text{if } N1, N2 = 1
\]  

(3)

### Table 1. Switching table

| Output voltage levels | Level generation switches | Polarity generation switches |
|-----------------------|---------------------------|------------------------------|
|                       | T1 | T2 | T3 | T4 | T5 | P1 | P2 | N1 | N2 |
| 4 Vdc                 | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  |
| 3 Vdc                 | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 0  |
| 2 Vdc                 | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 0  |
| 1 Vdc                 | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 0  |
| 0 Vdc                 | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  |
| -1 Vdc                | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |
| -2 Vdc                | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 1  |
| -3 Vdc                | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 1  |
| -4 Vdc                | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1  |
Quantity of switches needed for RSL-MLI are mentioned in equation (4).

\[ Ns = 5 + \frac{m-1}{2} \]  

Output voltage level, \( m \), is given by, \( m = (2V + 1) \); wherein \( V \) = number of voltage sources.

Components required for conventional MLIs and RSL-MLI are in Table 2.

### Table 2. Component comparison of m-level MLIs

| Topology/Components | DC | CC | CHB | RSL-MLI |
|---------------------|----|----|-----|---------|
| DC Source           | 1  | 1  | (m-1)/2 | (m-1)/2 |
| DC-Bus Capacitor    | m-1| m-1| 0    | 0       |
| No. of Switches     | 2 (m-1) | 2 (m-1) | 2 (m-1) | 5 + [(m-1)/2] |
| Clamping Capacitors | 0  | (m-1)/2 | 0     | 0       |
| Clamping Diodes     | 2 (m-2) | 0    | 0     | 0       |
| Total Components    | 5m – 6 | (7m – 5)/2 | 5 [(m-1)/2] | m + 4 |

RSL-MLI uses minimum number of components in contrast to conventional MLIs [16-18].

### 3. Modulation Methods

High frequency switching PWM method and fundamental frequency switching modulation methods are used to analyze the performance of RSL-MLI. In high frequency method, Triangular Multicarrier Unipolar Sinusoidal Pulse Width Modulation (TMC USPWM) technique is used.

#### 3.1 TMC USPWM modulation method

In PWM method, there will be continuous comparison of a reference waveform with a carrier waveform [9]. When reference > carrier, the switch equivalent to that carrier is turned on. When reference < carrier signal, the switch equivalent to that carrier is turned off. For the RSL-MLI, unipolar sine wave is used as reference waveform, where in the negative component of wave is converted to positive magnitude. Carriers used are triangular carrier waves with Phase Disposition (PD) method where all the triangular carriers will be arranged in phase [10]. For m-level inverter, number of carriers needed will be (m-1)/2 with identical frequency and amplitude. Figure 3 (a) displays unipolar sinusoidal reference wave with four triangular carriers for nine level output and Figure 3 (b) shows enlarged view for triangular carriers for clarity. Modulation Index, MI, for nine level is set as 1. By changing MI, output voltage levels of seven and five can be generated. Figure 4 shows the simulation output waveform for combined nine, seven and five levels by varying MI. Figure 5 (a), (b), (c) are THD analysis simulation of nine, seven and five level output. Table 3 shows the effect of MI on output level and THD comparison of different levels.
Figure 3. TMC USPWM (a) reference with carrier and (b) multicarrier triangular wave

Figure 4. TMC USPWM simulation output waveform of nine, seven and five levels

Figure 5(a). THD analysis of nine level output
Figure 5(b). THD analysis of seven level output

Figure 5 (c). THD analysis of five level output

Table 3. Effect of MI on THD

| MI  | Levels | O/P Voltage (RMS) | THD (%) |
|-----|--------|-------------------|---------|
| 1   | 9      | 282.9             | 13.68   |
| 0.7 | 7      | 197.9             | 21.32   |
| 0.5 | 5      | 141.4             | 26.91   |

With TMC USPWM, it is seen that THD generated are on higher side for nine, seven and five levels. This high frequency switching TMC USPWM method is not suitable for RSL-MLI.

3.2 Fundamental frequency switching

In fundamental frequency switching technique, two methods are experimented for simulation of proposed topology: Equal phase method and nearest level control method. Both are switching angle techniques. The %THD are compared in the end to select the best modulation method. Switching angle technique allows the MLI to produce an approximate sinusoidal output. This does not use any carriers due to which there is no need for separate modulation to produce switching steps [11]. Switching angle, $\alpha$, is the incident when MLI changes from current level to the following level. Figure 6 shows nine level output waveform using switching angle method. Because of symmetrical nature of sinusoidal wave, both positive and negative half cycles are centrally symmetrical and mirror symmetrical with each other. This means, switching angles in 0 degree to 90 degrees are the main or key switching angles; the remaining switching angles from 90 degrees to 360 degrees will be found...
with these main switching angles [12]. For a m-level inverter, main switching angles required are \(((m-1)/2)\) from 0° to 90°. Condition for the main angles is [8] given by equation (5).

\[
0 \leq \alpha_1 \leq \alpha_2 \ldots \leq \alpha_i \leq \frac{\pi}{2}; \text{ where } i = \frac{m-1}{2}
\]  

(5)

**Figure 6.** Nine level waveform with switching angle method

3.1.1 THD calculation

The generalized expression for THD [8] is given in equation (6).

\[
THD = \sqrt{\left(\frac{\text{Vrms}}{V1}\right)^2 - 1}
\]  

(6)

where Vrms = RMS value of output phase voltage; V1 = fundamental component. Using equations (7) and (8), Vrms and V1 can be obtained.

\[
V_{\text{rms}} = Vdc \sqrt{\frac{2}{\pi} \left(\frac{\alpha_2 - \alpha_1}{2} + 4(\alpha_3 - \alpha_2) + 9(\alpha_4 - \alpha_3) + 16(\frac{\pi}{2} - \alpha_4)\right)}
\]

\[
V1 = \frac{Wdc}{\pi \sqrt{2}} [\cos \alpha_1 + \cos \alpha_2 + \cos \alpha_3 + \cos \alpha_4]
\]  

(8)

3.3 Equal phase method (EPM)

In this method, main switching angles from 0 to 90 degrees are assessed and organized with identical space. Main switching angle (ai) [17], phase delay and pulse width for a m-level MLI are calculated using equations (9), (10) and (11),

\[
\alpha_i = i \left(\frac{180^0}{m}\right); \text{ where } i = 1, 2, \ldots, \frac{m-1}{2}
\]  

(9)

\[
\text{Phase delay} = \left(\frac{\text{time period}}{360^0}\right) \alpha_i
\]  

(10)

\[
\text{Pulse width } \% = \left[\frac{180 - 2\alpha_i}{180}\right] 100
\]  

(11)
For nine level, four main switching angles are 20°, 40°, 60°, and 80°. These can be calculated for seven and five levels using the same equations. Figure 7 shows the nine level simulation output waveform with Equal phase method simulation and Figure 8 is the %THD analysis simulation for the same. Table 4 gives comparison of theoretical and simulation values of %THD for nine, seven and five levels.

![Figure 7](image1.png)

**Figure 7.** Equal phase method nine level simulation output

![Figure 8](image2.png)

**Figure 8.** Equal phase method THD analysis simulation

| O/P Level | Switching angle (degree) | $V_{\text{rms}}$ (V) | % THD |
|-----------|--------------------------|----------------------|-------|
| 9         | 20 40 60 80              | 220.9 214.2          | 28 25.56 |
| 7         | 25.71 51.43 77.14 x      | 166.4 157.2          | 34.5 31.18 |
| 5         | 36 72 x x               | 109.6 100.6          | 42.8 42.94 |

3.4 **Nearest Level Control (NLC) Modulation**

Working of NLC method is based on selection of closest voltage value which could be produced using converter to the desired baseline voltage [17-18]. The determination of a closest voltage value is obtained by equating the baseline sinusoidal voltage with inverter output voltage. Both THD and
switching losses are reduced with this scheme. Equation (12) is used to calculate main switching angles [18],

\[ \alpha_i = \sin^{-1}\left(\frac{2i-1}{m-1}\right); \text{where} \ i = 1, 2, \ldots, \frac{m-1}{2} \]  

(12)

Reference block diagram and synthesis waveform are given in Figure 9 (a), (b) [9]. Figure 10 shows simulation output waveform for nine, seven and five levels combined. THD analysis simulation is shown in Figure 11. Table 5 gives comparison of theoretical and simulation values of %THD for nine, seven and five levels.

![Reference block diagram and synthesis waveform](image)

**Figure 9.** (a) Reference block diagram and (b) synthesis waveform.

![NLC simulation output waveform for nine, seven and five levels](image)

**Figure 10.** NLC simulation output waveform for nine, seven and five levels

![THD analysis simulation with NLC method](image)

**Figure 11.** THD analysis simulation with NLC method
Table 5. Comparison – theoretical vs simulation %THD.

| O/P Level | Switching angle (degree) | Vrms (V) | % THD |
|-----------|--------------------------|----------|-------|
|           | $\alpha_1$ | $\alpha_2$ | $\alpha_3$ | $\alpha_4$ | Theoretical | Simulation | Theoretical | Simulation |
| 9         | 7.2      | 22       | 38.7    | 61       | 288        | 286.6      | 9.5        | 9.36       |
| 7         | 9.6      | 30       | 56.4    | x        | 218.2      | 216.5      | 12.6       | 12.23      |
| 5         | 14.5     | 48.6     | x       | x        | 149        | 146.7      | 17.7       | 17.6       |

4. Comparison of THD – EPM and NLC
Table 6 shows simulation %THD comparison of Equal phase and NLC modulation methods. The output waveform in Equal phase method tends to look like a triangular waveform rather than sinusoidal. Also, THD values obtained are on much higher side in Equal phase method. On the other hand, for nine level output, in NLC method %THD obtained is 9.36 which is in the acceptable range when compared to Equal phase method. Also, it is seen that as the output levels increase from five, seven, nine, %THD decreases as well as a smooth output waveform can be obtained in NLC method, making it the most suitable modulating method for RSL-MLI topology.

Table 6. Simulation %THD comparison – EPM vs NLC.

| Levels | Simulation % THD |
|--------|------------------|
| 9      | 25.56            |
| 7      | 31.18            |
| 5      | 42.94            |

5. Conclusion
In this paper a nine level single phase RSL-MLI topology is proposed. This topology requires nine switches in contrast to sixteen switches of conventional MLIs for nine level output, thus using least number of devices. RSL-MLI can be scaled up to any number of output voltage levels by addition of switches and dc source. As the number of output levels increase, %THD will reduce. Overall system cost, control complexity, size and installation area will be reduced. Simulation of the RSL-MLI using high frequency switching and fundamental frequency switching methods are carried out to analyse %THD, which affects system performance. By using NLC modulation method, low %THD of 9.36% is obtained as compared to TMC USPWM and EPM modulation methods. It is a compact arrangement appropriate for any inverter applications. Further, hardware design and development of RSL-MLI topology for UPS applications, motor drive applications can be verified. Also, feasibility of connecting the RSL-MLI as inverter interface between renewable energy sources and main grid can be examined.

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