Research on the module of color image sonar system based on imx6ull

Xiaofeng Zhao¹, Jing Wang²*, Wei Li³, Zhiyuan Wang³, Qijiang Zhang⁴
¹,²,³,⁴School of Information Science and Engineering, Yunnan University, Kunming, Yunnan, 650091, China
lee1108@mail.ynu.edu.cn

Abstract. Underwater sonar imaging system has a wide range of application prospects, and both military and civil are increasingly valued. This paper introduces the module design of a color image sonar system based on IMX6ULL and completes the imaging of the sonar system through experiments. The main frequency and sampling frequency of the system are improved and applied to the TKIS-I color image sonar digital system. High-performance A / D is used for data acquisition and storage, and RS485 is used for long-distance transmission to the host computer to realize display and imaging. It is mainly composed of a core board, PWM signal module, communication module, sampling module, and motor drive module. The processing speed and imaging effect of the improved system are significantly improved.

1. Introduction

In the last few decades, there have been increasingly rapid advances in the field of sonar imaging systems. Whether it is scientific research on the ocean or the development of ocean resources, the first thing to get is the information on the seabed environment, and the field of ocean exploration has gradually developed from this. Sonar equipment was employed in the field of ocean exploration earlier, combining underwater acoustic signal detection and image processing technologies to detect target sea areas. TKIS-I helmet-mounted color image sonar is an undersea detector used for ocean exploration. The working frequency is 675KHz and the detection range is 1.5 meters, 3 meters, 12 meters, 23 meters, 50 meters, and 100 meters. It is appropriate for Long-range detection. Its core processor is STM32F407 based on the Cortex-M4 core, with a working frequency of 168MHZ. Figure.1 displays the industrial computer and transducer head.

Figure.1 Industrial computer and transducer head
Digital image sonar has the advantages of stable system performance, high image quality, and strong processing ability. However, the performance of the processor requirements is very high due to a large amount of data for computation and the need for real-time imaging. With the rapid development of CPU devices with low power consumption and high performance, the imaging sonar with low power consumption and high-performance core processor improves the overall performance and makes the system structure simpler. Considering the shortcomings of the original digital system, the TKIS-I image sonar digital system is upgraded, and the imx6ull core board based on the cortex-a7 processor is selected as the core of the digital board. The sonar system with this processor as a hardware platform can achieve higher data operation speed, and external related functional modules can improve the imaging effect of the system.

The core idea of modernization is gradually formed with the development of computer hardware and software, generally including software modernization and hardware modernization that support each other. The hardware module is the basis and interface platform for the realization of the function algorithm, and the software module is the necessary condition for system flexibility and function expansion. Focusing on the design and implementation of sonar modular hardware, the main technical route is to decompose the system into independent modules and use high-performance processors to control each module. The module based on the IMX6ULL image sonar digital system is designed in this paper. It uses the core processor IMX6ULL as the hardware development platform and the Linux operating system as the software development environment to achieve the purpose of improving the image display effect of the TKIS-I image sonar digital system and the data processing speed of the digital system.

2. HARDWARE DESIGN
Overall hardware adopts modular circuit design, composed of core board and peripheral circuit. The core board is primarily composed of an IMX6ULL processor and other key modules. It mainly completes the generation of transmitting signals and data conversion operations. The peripheral circuit mainly contains communication modules, sampling modules, and motor drive modules. Figure.2 has been instrumental in our understanding of the modular circuit.

![Figure 2: System module circuit](image)

2.1. MX6ULL core board
IMX6ULL core board IMX6ULL EMMC version core board resources:
- CPU: MCIMX6Y2CVM08AB (industrial grade), 800MHz (The original system only has 168MHZ).
- External expansion DDR3L: NT5CC256M16EP-EK, 512MB bytes, commercial grade.
- EMMC: KLM8G1GET, this is an 8GB EMMC chip.
- Two 2*30 anti-reverse insertion BTB sockets lead out a total of 120 PINs.
The universal interface core board designed in this article is IMX6ULL, which is a series of products based on the Cortex-A7 processor. The main frequency is up to 800MHz. It has the characteristics of low power consumption, high performance, ultra-high energy efficiency, and small size. Compared with the same series, the product can save 50% of power consumption under the same performance. This core board has a total of 160 pins, of which 129 pins are multiplexed with functions, with richer resources and more flexible selection, which are very suitable for applications in a variety of industrial control fields. The main control circuit diagram is presented as in Figure 3.

![Figure 3. Circuit structure of system](image)

2.2. Design of RS485 circuit
The universal interface is developed in this article based on the IMX6UL core board to build four independent RS485 interfaces. The RS485 level cannot be directly linked to the IMX6U, and a level conversion chip is also required. In this study, SP3485 is adopted to perform 485 level conversions, where R21 is the terminal matching resistor, and R19 and R20 are two bias resistors to ensure that the 485 bus maintains logic 1 in the silent state.

The RE pin of SP3485 is connected to the RS485_RX pin through a series of circuits, making RS485 be controlled through the RS485_RX pin in the receiving and sending states. RS485 is completely used as a serial port. RS485 bus interface connects to external 485 devices through 2 ports. When using RS485 communication, A must be connected to A, and B must be connected to B. Otherwise, the communication may be abnormal. Figure 4 shows the circuit design.

![Figure 4. Design of RS485 circuit](image)

2.3. Motor drive circuit
A3967SLB is a complete micro-stepping motor driver with a built-in converter. It is designed to operate bipolar stepper motors in the following environments: full-step, half-step, quarter, and eight-step modes, with an output drive of up to 30 V and a maximum current of ±750 mA. The A3967SLB includes a current regulator current decay mode that can run at a slow, fast, or mixed speed with a fixed downtime. This current decay control scheme results in reduced audible noise of the motor,
improved step accuracy, and decreased power consumption. Simply inputting a pulse on the step input and the motor will take one step (full-step, half-step, quarter step, and eighth step), depending on the logic input. This interface is very suitable for applications that cannot be used or are burdened with too much µP.

The motor drive circuit is given in Figure 5. The circuit uses the A3967 drive chip, which can drive a stepper motor below 12V. The maximum operating current can reach 1A, and the voltage of the MS1 and MS2 pins of the chip can be set to affect the motor. The step angle is further refined and can be refined up to 8 times.

2.4. ADC circuit design

The frequency of the sound wave delivered by the high-frequency sonar system is 675kHz. The theory of the Nyquist Sampling Theorem provides a useful account to determine the sampling frequency. Therefore, the frequency of the echo signal will also be 675kHz. According to the Nyquist sampling law, the rate of the AD9220 analog-to-digital conversion circuit depends on the frequency of the input clock. The ADC sampling frequency of the system should be higher than or equal to 1.35MHz to ensure that the signal is sampled without distortion. In this paper, the sampling frequency of the system can reach 10msps through the output of 10MHz clock frequency by the processor.

The sampling circuit of the sonar system uses an ad9220 conversion chip, which supports parallel data transmission, outputs 12-bit conversion results and can provide the highest sampling frequency of 10MHz. AD9220 has a very flexible input terminal, allowing it to be connected with a single-ended or differential interface circuit. Single-ended input requires that VINA is DC or AC signal from signal source when VINB has DC offset in an intermediate code transition. The designed circuit is illustrated in Figure 6. Increasing the sampling rate can improve the imaging effect of the system. The ADC chip can work normally and stably with only a few external capacitances and resistance devices.
The sampling range is set to 0-5V, and the input span is 2×VREF centered on 2.5V. An external 2.5V reference drives the VINB pin to set the common-mode voltage to 2.5V. The input span can be independently set by the voltage divider composed of R1 and R2, and the voltage divider generates the VREF signal. A1 buffers this resistor network and drives VREF. According to the accuracy requirements, this operational amplifier is selected. The circuit must connect a 10µF capacitor in parallel with a 0.1µF low-inductance ceramic capacitor to output the reference to ground. Figure 8 presents AD9220 configured for input.

The sampling range is set to 0-5V, and the input span is 2×VREF centered on 2.5V. An external 2.5V reference drives the VINB pin to set the common-mode voltage to 2.5V. The input span can be independently set by the voltage divider composed of R1 and R2, and the voltage divider generates the VREF signal. A1 buffers this resistor network and drives VREF. According to the accuracy requirements, this operational amplifier is selected. The circuit must connect a 10µF capacitor in parallel with a 0.1µF low-inductance ceramic capacitor to output the reference to ground. Figure 7 presents AD9220 configured for input.

Figure 7. Analog input configuration

3. SOFTWARE DESIGN
After the system is turned on and running, interrupt priority, timer, ADC, motor, USART, and delay function should be initialized. First, the system determines whether the sonar's range has changed. If the scan range changes, the motor will rotate the transducer to the initial position. The system starts to receive the data stored in the SRAM in the previous frame, processes the data, and sends it to the host computer for display through RS485. Then, the motor rotates one step, and the system sends PWM pulses. Finally, the transducer signal is sampled. When the system is sampling, ARM reads the sampled data and saves it in flash. After ARM finishes other work, the flag bit is inverted. Entering the next cycle. The system software flow chart is shown in Figure 8:
3.1. **RS485 programming**

1) Set the UART clock source to pll3_80m, and set the UART_CLK_SEL bit of the register CCM_CSCDR1 to 0.

   Initialize the IO used by UART1, set the registers UART3_UCR1~UART3_UCR3 of UART1, the setting content mainly includes baud rate, parity, stop bit, and data bit.

2) After the initialization of UART1 is completed, UART3 can be enabled. Set the bit UARTEN of the register UART3_UCR1 to 1.

3) Write functions: void puts(char *str) and void putc(unsigned char c), used for UART3 data receiving and sending operations.

3.2. **PWM program design**

After the system completes the boot initialization, it enters the sound wave transmission. First, set the sound wave transmission time, enable the PWM module to generate two complementary square wave signals, then connect the square wave signals to the transmitting circuit, and finally transmit the 150V sine wave signal output by the circuit is input to the sonar transducer, and the timer is started immediately for timing．The program design process is described as follows:

1) Configure pin GPIO1_IO8

   Configure the multiplexing function of GPIO1_IO08 and reuse it as the PWM1_OUT signal line.

2) Initialize PWM1 and PWM3

   Initialize PWM1 and PWM3, configure the frequency and default duty cycle of the required PWM signal.

3) Set interrupt

   We can enable the FIFO empty interrupt, so that when the FIFO is empty, the corresponding interrupt will be triggered, and then in the middle write the sampled value to the FIFO in the interrupt processing function.

4) Enable PWM1
After configuring PWM1, it can be turned on similarly. We set another PWM output PWM3 to output two complementary PWM signals.

3.3. Motor drive program design

Motor drive function: According to the function design of the motor drive chip, first design the motor rotation direction functions void Dir_High(void) and void Dir_Low(void). According to the performance parameter setting of the system, the step angle of the motor is set to 0.9 degrees. In the program design, the GPIO of the ARM processor can be used to generate the pulse signal to drive the motor. Then, delay a period of time, pull down the pin level to realize a pulse signal, and set the number of cycles through the for loop, so as to control how many pulse signals are output to the motor drive chip. In this way, the steering function, step angle function, motor wake-up function, motor sleep function, and motor enable function can be set. When the system works, the scanning angle is 150°, and there are 167 scanning beams. The design is exhibited in Figure. 9.

![Figure. 9 Scanning angle](image)

3.4. ADC programming

Since AD9220 sampling module designAd9220 outputs 12-bit parallel data, 12 GPIOs are needed to read the sampled data. First, set CLK. CLK uses the SCK clock in the main control chip IIC module as output, and then initializes 12 GPIOs and sets it to read mode. Fetch the data and save it in the SRAM in the system, waiting for subsequent data processing and use.

4. EXPERIMENTAL RESULT

In this paper, an algorithm for a robust template matching method based on the combination of the wavelet transform method and SIFT is proposed. Discrete wavelet transform is done firstly on a reference image and a template image, and low frequency parts of them is extracted, then we use harris corner detection to detect the interesting point in low frequency parts of them to determined the matching candidate region of template image in reference image, extracting SIFT features on the matching candidate region and template image. The extracted SIFT features are matched by k-d tree and bidirectional matching strategy. Experiment show that, the algorithm can improve the accuracy of matching and at the same time to reduce the computation load.

Figure.10 shows the selected experimental site. According to the hardware design plan of the system, the system's processor, power module, ADC sampling module, communication module, motor module are designed. Before drawing the PCB circuit board, the experimental circuit board is built for preliminary verification, and write the experimental board software at the same time Program, combined with hardware and software to debug the experiment board. After testing, system running time is greatly reduced, and the system can still image normally.
Figure 10 shows the running time of the original system and the system designed in this paper.

| Distance (m) | Original system (s) | After improvement (s) |
|-------------|----------------------|-----------------------|
| 1.5         | 18.4                 | 14.1                  |
| 3           | 18.6                 | 15.0                  |
| 12          | 25.7                 | 20.5                  |
| 23          | 28.3                 | 22.3                  |
| 50          | 33.9                 | 28.1                  |
| 100         | 44.1                 | 39.3                  |

Figure 11 Comparison time

Figure 12 illustrates the imaging effect of the original system. After using the module design in this paper, the imaging effect of the system is shown in Figure 13. The noise is educed, and the imaging effect is improved.

Figure 12 Imaging effect of the original system
Figure 13 Imaging effect of the original system

5. Conclusion
This paper designs a modular design based on the IMX6ULL color sonar system. The hardware design of this system provides control capability for the system, and the design of the IMX6ULL core board meets the high-speed processing requirements of the system. The software part of the system provides the system with the functions of driving RS485, stepping motor, PWM transmitting, and ADC. The main frequency of the system is 800MHz, and the sampling frequency is 10msps. The experimental comparison results demonstrate that the IMX6ULL-based color image sonar system designed this time has less data processing time...
compared to the original system. It meets the requirements of increasing the real-time speed of the sonar system and improves imaging effect, presenting certain practical application significance.

References
[1] JiXiangLi, XinCongZhou, XiuMinChu, DeShanChen, XianQiaoChen. Draft detection technology based on echo signal strength processing of single beam sweep [J]. Ship and sea engineering, 2017,46 (06) : 12-16 + 22.
[2] Sensor Research; Researchers at Zhejiang University Report New Data on Sensor Research (Optimized Design for Sparse Arrays In 3-d Imaging Sonar Systems Based On Perturbed Bayesian Compressive Sensing)[J]. Journal of Technology,2020.
[3] Tian Haowen,Guo Shixu,Zhao Peng,Gong Minyu,Shen Chao. Design and Implementation of a Real-Time Multi-Beam Sonar System Based on FPGA and DSP.[J]. Sensors (Basel, Switzerland),2021,21(4).
[4] FLIR Belgium BVBA; Patent Issued for Touch-Gesture Control For Side-Looking Sonar Systems (USPTO 10,802,125)[J]. Electronics Newsweekly,2020.
[5] Mitcham Industries Inc.; Mitcham Industries Partnership to Produce Synthetic Aperture Sonar Systems[J]. Journal of Technology,2020.
[6] Shuping Lu,Feng Ding,Ranwei Li. Robust Centralized CFAR Detection for Multistatic Sonar Systems[J].Chinese Journal of Electronics,2021,30(2).
[7] T. S. Kim, I. S. Jang, C. J. Shin and M. K. Lee, "Underwater construction robot for rubble leveling on the seabed for port construction," 2014 14th International Conference on Control, Automation and Systems (ICCAS 2014), Seoul, 2014, pp. 1657-1661.
[8] HuiYang, ShuoLi, JunBaoZeng. Research on information extraction method of single-beam forward-looking sonar [J]. Measurement and control technology, 2012,31 (09) : 16-19.