**Abstract:** Medium voltage (MV) DC/DC converters are key equipment for interconnection between DC power lines with different voltage levels in MVDC grids. The Input-series-output-parallel (ISOP) modular MV DC/DC converter is feasible to realize MV to low voltage (LV) conversion. However, a large number of LV modules in the converter may reduce the reliability and increase the complexity. This letter proposes a phase-shifted full-bridge MV DC/DC converter using series-connected power devices as switching modules. The converter is of low cost, simple structure, compact volume, and high reliability because these switching modules require only one external isolated driver circuit and very few components to achieve voltage sharing among series-connected power devices. The operation principle of the switching modules is analyzed, and the simulation and experimental results validate the feasibility of the converter design.

**Keywords:** DC/DC converter; series-connected power devices; medium voltage; voltage sharing

1. Introduction

Recently, with the development of distributed renewable energy power systems, medium voltage (MV) DC grids have gained growing interest. The MV DC/DC converters that step down thousands of volts to hundreds of volts are key equipment in MVDC grids [1]. The undersea power systems of cabled seafloor observatories or distant subsea oil and gas fields are MVDC grids to power underwater equipment using medium voltages of the order of thousands of volts [2,3]. MV DC/DC converters for subsea MVDC grids require compact volume, high reliability, and high power density.

The bottleneck of MV DC/DC converters is that mature semiconductor power devices cannot meet the voltage and power needs. There are two approaches to solve the problem. One is modular converters with input-series output-parallel (ISOP) connected low voltage (LV) input power electronics building blocks (PEBBs) [4–13]. The other is to develop new semiconductor power devices with high blocking voltages or connect power devices in series to reach high blocking voltages, based on conventional converter topologies [14].

Although the ISOP modular converters have some advantages, e.g., LV component availability and possibly higher efficiency [8], a large number of PEBBs will lead to a complex control system for input voltage sharing and output current sharing. Poor input voltage sharing and output current sharing can greatly reduce the stability of modular converters [6,9–12]. Moreover, there are a large number of semiconductor power devices in modular converters, so a large number of isolated driver circuits are required, which is unbeneficial for a compact design.

The converters based on the second approach can use traditional topologies and control schemes [14]. New semiconductor power devices with high blocking voltages are not yet mature [15,16].
and always have high switching loss so that the switching frequency is usually limited to below 20 kHz. Connecting LV rated power devices in series is another way to achieve a higher blocking voltage. However, a slight deviation of power device gate signals or parameters can result in a serious voltage imbalance among these series-connected devices [17]. Several circuits have been proposed for connecting power devices in series [17–22]. Since each power device requires an independent isolated driver in these circuits, they are not suitable for compact designs. Single-gate driving circuits for series-connected power devices [23,24] can reduce the complexity suitable for compact designs, but these circuits have some defects in high-frequency applications. Moreover, the research of series-connected power devices mainly focuses on the design of power switching modules [21], yet little on converters.

This letter proposes a compact MV DC/DC converter using series-connected power devices as switching modules. A novel high-frequency switching module that requires only one external isolated driver circuit and very few components for series-connected power devices is the key. The converter adopts the phase-shifted full-bridge (PSFB) topology and the feasibility is validated by simulations and experiments.

2. Schematic of the Proposed DC/DC Converter

The schematic of the proposed DC/DC converter is shown in Figure 1. The converter can adopt a mature converter topology, as the switching modules with power devices in series can withstand the input voltage level. The PSFB topology is adopted in the design, as it has smaller voltage stress and higher power output than other topologies. The primary side of the PSFB converter consists of four power switching modules, each of which only requires one independent isolated driver.

Figure 1. Schematic of the proposed DC/DC converter.
Table 1 shows the comparison among different MV DC/DC converter schemes. The proposed converter has advantages in volume, efficiency, reliability, and cost. Assuming that the input voltage of the converter is \( N \) times of the blocking voltage of the power devices, the MV converter requires at least \( N \) LV converter modules in the ISOP scheme. If the LV converter modules adopt a full-bridge topology \([8]\), the ISOP converter requires \( 4N \) isolated driver circuits. Moreover, there are complex feedback control systems and isolated signal acquisitive circuits for input voltage and output current sharing. The MV full-bridge converter based on series-connected power devices in the traditional methods also requires \( 4N \) isolated driver circuits \([17]\). Comparatively, the proposed MV converter only requires four isolated driver circuits, making it compact in size, simple in structure, and low in cost. ISOP converters have high conversion efficiency due to the adoption of LV power devices, but the complex control system may reduce its reliability \([6,9–12]\). The proposed converter adopts mature control methods, which makes it highly reliable and has good dynamic performances.

| MV DC/DC converters                       | Volume | Efficiency | Reliability | Cost   |
|------------------------------------------|--------|------------|-------------|--------|
| ISOP converters                          | Medium | High       | Medium      | High   |
| Traditional converters with series-connected power devices | Large  | Low        | Low         | High   |
| The proposed converter                   | Small  | Medium     | High        | Low    |

3. Series-Connected Power Switching Module

The proposed series-connected power switching module requiring only one isolated driver circuit is also shown in Figure 1. The circuit is effective for IGBTs, which are adopted in this study, and MOSFETs \([23,24]\). The proposed circuit is similar to, but ultimately different from, those circuits in \([23,24]\), especially in high-frequency characteristics and scalability. Specifically, the dynamic voltage-balancing capacitors \( C_n \), which control the upper IGBTs on-off and dynamic voltage sharing, provide the circuit with good scalability under the condition that the capacitor values are consistent, so the circuit design is more simple and controllable. Furthermore, the special arrangement of the static balancing resistors \( R_{g,n} \) and the gate protection zener diodes \( Z_{da,n} \) and \( Z_{db,n} \) in \([24]\) is extended for more power devices in series, not only having the function of static voltage sharing, but also providing negative gate voltages for the upper IGBTs during off state. The design of the gate diodes \( D_{g,n} \), the gate resistors \( R_{g,n} \), and the accelerating capacitors \( C_{g,n} \) in parallel makes the circuit suitable for high-frequency applications. Taking the circuit with three IGBTs in series as an example, the main current paths in different states are shown in Figure 2, and the detailed operation principle is described as follows.

- **Off state:** When the gate voltage of the bottom IGBT remains negative, the current paths, as shown in Figure 2a, can lead to negative gate voltages for upper IGBTs. Thus, all series-connected IGBTs can keep off state. Moreover, the circuit can be simplified as a circuit in which each static balancing resistor \( R_{g,n} \) is connected with the corresponding IGBT in parallel. If \( R_{g,n} \) is far smaller than the equivalent resistance of the IGBTs, the static voltage sharing among these IGBTs can be guaranteed.

- **Turn-on:** Once the driving signal of the driver circuit turns to a reliable positive voltage, the bottom IGBT \( T_1 \) will turn on. The collector-emitter voltage \( V_{ce} \) of \( T_1 \) will decrease rapidly, so the electric potential at the collector electrode will fall quickly, which means that there is a voltage difference between the gate electrode and the source electrode of \( T_2 \). Accordingly, \( C_1 \) will charge the gate-emitter capacitor \( C_{ge} \) of \( T_2 \) through the current \( i_{g2} \) in Figure 2b, leading to an increase in the gate voltage \( V_g \) of \( T_2 \). According to Kirchhoff’s Voltage Law, a circuit voltage relationship can be obtained as:

\[
V_{ce} + V_g = V_C - V_{Cg} \tag{1}
\]
Similarly, all upper IGBTs will turn on in sequence according to this mechanism. As described above, all charges in $C_n$ are injected into the gate capacitor of the corresponding power device, which is different from the circuits in [23,24], and thus the proposed circuit supports more power devices in series.

According to Equation (2), if $C_n$ is directly connected to the gate of the IGBT, i.e., $1/C_{g,n}$ is 0, the pulse

$$i_{g_2} = V_{ce} + V_g = \int_0^t \frac{i_{g_2}}{C_n} dt - \int_0^t \frac{i_{g_2}}{C_{g,n}} dt = \frac{V_{ce} + V_g}{\int_0^t \left( \frac{1}{C_n} - \frac{1}{C_{g,n}} \right) dt} \tag{2}$$

The current $i_{g_2}$ can be defined as:

$$V_{ce} + V_g = \int_0^t \frac{i_{g_2}}{C_n} dt - \int_0^t \frac{i_{g_2}}{C_{g,n}} dt \Rightarrow i_{g_2} = \frac{V_{ce} + V_g}{\int_0^t \left( \frac{1}{C_n} - \frac{1}{C_{g,n}} \right) dt} \tag{2}$$

Similarly, all upper IGBTs will turn on in sequence according to this mechanism. As described above, all charges in $C_n$ are injected into the gate capacitor of the corresponding power device, which is
different from the circuits in [23,24], and thus the proposed circuit supports more power devices in series.

The parallel connection of \( R_{g,n} \) and \( C_{g,n} \) is specially designed for high-frequency converters. According to Equation (2), if \( C_n \) is directly connected to the gate of the IGBT, i.e., \( 1/C_{g,n} \) is 0, the pulse currents through \( Z_{da,n} \) and \( Z_{db,n} \) will be very large during each turn-on transition, leading to large energy losses on them, bringing a challenge to select small components. If only one resistor is used instead of the RC network, the turn-on speed will slow down due to the current limiting effect of the resistor. According to Equation (2), \( C_{g,n} \) should be larger than \( C_n \) and the pulse current increases with the increasing of \( C_{g,n} \). It is necessary to balance the turn-on speed and pulse currents in the selection of \( C_{g,n} \). Generally, \( C_{g,n} \) is double \( C_n \) according to simulation results.

On state: The driving signal of the driver circuit keeps a reliable positive voltage to ensure that \( T_1 \) is in a stable on state. The \( C_{ge} \) of upper IGBTs are charged in the turn-on transition as described above, so all IGBTs are in a stable on state. It is worth mentioning that the \( C_{ge} \) of upper IGBTs will discharge during on state, which means \( V_g \) of upper IGBTs will decrease slowly. However, it does not matter in high-frequency converter applications as the on-time is short.

Turn-off: Once the driving signal of the driver circuit reaches a reliable negative voltage, \( T_1 \) will turn off. The electric potential at the collector electrode of \( T_1 \) will rise rapidly, so there will be a negative pulse voltage between the gate and emitter electrode of \( T_2 \), forcing \( T_2 \) to turn off. All IGBTs will turn off in sequence by this mechanism. The main current paths in this period are shown in Figure 2c. When all IGBTs are in off state, there is still a charging current for \( C_n \) as shown in Figure 2d. With the charging of \( C_n \), when the voltage across the switching module rises to the bus voltage \( V_{bus} \), the turn-off transition ends. Since each level has the same structure, all IGBTs turn off from the bottom to the top in sequence with the same voltage slope. Therefore, the voltage distribution among all IGBTs is controllable. As the lower IGBTs turn off earlier, the \( V_{ce} \) of them will be larger. The voltage differences between adjacent IGBTs are equal and related to \( C_n \).

The switching loss is a key factor to be considered in high-frequency applications. During the turn off transition, the charging process of \( C_n \) brings extra energy loss \( E_{off} \), which can be defined as follows:

\[
E_{off} = \frac{1}{2} NC_n V_{ds}^2 = \frac{C_n V_{bus}^2}{2N}
\]

4. Simulation Verification

To verify the feasibility of the proposed series-connected power switching module and the effect of the accelerating capacitors on the circuit, double pulse tests are simulated in LTspice. The waveforms, as shown in Figure 3, validate the proposed circuit drivers the series-connected power devices efficiently. Moreover, the voltage sharing among the three power devices is realized during both static and dynamic transitions. As shown in Figure 4a, the turn-on loss on gate protection zener diodes \( Z_{da,2} \) and \( Z_{db,2} \) is maximum when both \( R_{g,n} \) and \( C_{g,n} \) are 0, and increases with the increasing of the accelerating capacitors \( C_{g,n} \), which agrees with Equation (2). Moreover, it can be seen from Figure 4b that the increasing of the accelerating capacitors can significantly reduce the turn-on delay, but the value of the accelerating capacitors has little effect on it.

To verify that the proposed switching module can be applied to the PSFB topology, a simulation of a converter using three series-connected IGBTs in each switching module is performed in LTspice. The critical parameters of the simulation are shown in Table 2.

The waveform of the transformer primary voltage in Figure 5a verifies that the primary side of the proposed converter can convert DC into alternating current (AC) power. The voltage distribution in the switching module agrees with the theoretical analysis. The maximum voltage difference among the IGBTs is 41.8 V. The output voltage in Figure 5b stabilized to about 48 V after a short ascent, proving the feasibility of the converter design.
Figure 3. Simulation waveforms when the DC bus voltage is 3000 V, $C_n = 1 \text{nC}$ and $C_{n,g} = 2.2 \text{nC}$: (a) Waveforms of a double-pulse test; (b) close-up view of waveforms during turn-on transition; (c) close-up view of waveforms during turn-off transition.

Figure 4. Simulation results with different accelerating capacitors when the DC bus voltage is 3000 V and $C_n=1 \text{nC}$: (a) The turn-on loss on gate protection zener diodes $Z_{da,2}$ and $Z_{db,2}$; (b) the turn-on delays.
Table 2. Critical parameters in the simulation.

| Component | Value      | Description                  |
|-----------|------------|------------------------------|
| $V_{in}$  | 400 V      | Input voltage                |
| $V_{out}$ | 48 V       | Output voltage               |
| $f$       | 50 kHz     | Switching frequency          |
| $T_n$     | IXBH42N170 | 1700 V IGBT                  |
| $R_{g,n}$ | 50 Ω       | Gate resistors               |
| $R_{s,n}$ | 510 KΩ     | Static voltage-balancing resistors |
| $Z_{da,n}$ and $Z_{db,n}$ | 1N5352B | 15 V zener diode |
| $D_{g,n}$ | SF1600     | 1600 V fast recovery diode   |
| $C_n$     | 2.2 nF     | Dynamic voltage-balancing capacitors |
| $C_{g,n}$ | 4.7 nF     | Gate accelerating capacitors |

![Figure 5](image-url)  
**Figure 5.** Simulation waveforms under 200 W load: (a) Primary voltage of the transformer and voltage distribution in $S_1$; (b) output voltage.

5. Experiment Verification

A prototype with three series-connected IGBTs in each switching module, shown in Figure 6a, was developed to verify the converter design. The critical parameters of the prototype are also given in Table 2. The control circuit is based on phase shift resonant controller integrated circuits. The photograph of the test setup is shown in Figure 6b.

![Figure 6](image-url)  
**Figure 6.** (a) Photograph of the DC/DC converter prototype; (b) the photograph of the experimental setup.

As shown in Figure 7a,b, the proposed switching module can turn on and off continuously. Figure 7c,d verify that the full-bridge topology consisting of 4 switching modules converts DC into AC power. The phase difference between the leading and lagging legs changes as shown in Figure 7, so that the output voltage is stable under different loads. The maximum voltage difference of the...
power devices within the switching module is about 40 V, which is consistent with the simulation result. It is almost unchanged under different loads, as shown in Figure 8.

![Figure 7](image-url)

**Figure 7.** Experiment waveforms: (a) The voltages across S1 and S2 (no-load); (b) the voltages across S1 and S2 (200 W load); (c) the primary voltage of the transformer (no-load); (d) the primary voltage of the transformer (200 W load).

![Figure 8](image-url)

**Figure 8.** The voltage distribution in S1 under different loads: (a) Under no-load; (b) under 200 W load.

The efficiency curve of this converter is shown in Figure 9. It can be seen that the efficiency increases with the load, consistent with general DC/DC converters. There is no maximum conversion efficiency point in Figure 9, so further increase of the load may continuously improve the conversion efficiency. The efficiency at 400 W load is about 83.1%, greater than the efficiency (63.8%) of the converter based on traditional methods for series-connected power devices in [14], but less than the efficiency (95%) of ISOP converters in [10]. The measured switching loss of each module is about 0.15 mJ, larger than the theoretical value according to Equation (3). The reason for this is that the switching loss of the IGBTs with high blocking voltages is large, so choosing a more suitable power
device can improve the efficiency. As the proposed converter can adopt a mature control scheme and topology, realizing soft switching is also an effective way to further improve the conversion efficiency.

![Efficiency vs. Output Power](image.png)

**Figure 9.** Efficiencies under different loads.

### 6. Conclusions

This letter proposes a compact MV DC/DC converter using series-connected power devices. The converter applies the mature PSFB topology and control method, so it has high stability and dynamic performances compared with ISOP converters. The power switching module, composed of several passive components and power devices in series, and with only one external isolated driver circuit, is the key of this converter. Based on the modules, the proposed converter requires only four isolated driver circuits, making it compact, simple in structure, and cost-effective. The operation principle of the switching module is analyzed and the feasibility of the design is verified by simulations and experiments. The switching module can also be used in other high-frequency and high-voltage applications. The characteristics of this converter in soft switching mode are worthy to be studied to achieve higher efficiencies.

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