Physics-Based Compact Modeling of Double-Gate Graphene Field-Effect Transistor Operation

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Abstract - An analytic compact model of large-area double-gate graphene field-effect transistor is presented. As parts of the model, the electrostatics of double-gate structure is described and a unified phenomenological approach for modeling of the two drain current saturation modes is proposed.

I. INTRODUCTION

Graphene field-effect transistors (GFETs), though widely presented in experimental [1, 2, 3] and theoretical studies [4, 5, 6], still require a comprehensive theoretical examination. Typically these transistors are double-gate with a thick back oxide and thin top oxide. The back gate in such structures allows adjusting conductivity type of the channel and controlling the position of current minimum point. In this report we present the model of the graphene double-gate field-effect transistor and use this model for calculation of transistor DC characteristics. The model is based on analytical solution of the current continuity equation in a diffusion-drift approximation [7].

II. DG GFET ELECTROSTATICS

The energy band diagram of graphene field-effect transistor is shown in Fig. 1.

![Fig. 1. Double-gate structure energy band diagram](image1)

Both gates are positively biased with respect grounded graphene sheet. Charge neutrality condition is given by

\[ \varepsilon_F \varepsilon_0 - \varepsilon_F \varepsilon_0 \frac{eV_1 - \varepsilon_F}{d_1} + \varepsilon_F \varepsilon_0 \frac{eV_2 - \varepsilon_F}{d_2} = \varepsilon_F n_s (\varepsilon_F) + C_g \varepsilon_F \]  

(1)

or, the same, graphene charge density \( n_s \) is expressed as

\[ n_s = e(C_1V_1 + C_2V_2) - \varepsilon_F (C_1 + C_2 + C_a) = \]

\[ = C_1 + \frac{C_{it}}{C_1 + C_2} \varepsilon_F (V_1, V_2), \]

(2)

where \( V_{Geff} = (C_1V_1 + C_2V_2)/(C_1 + C_2) \) is the effective gate voltage, \( V_{G1(2)} \) is the top (back) gate voltage, \( V_{G1(2)} = |V_{G1(2)}| - V_{N1(2)} \), \( V_{N1(2)} \) are charge neutrality biases, \( \varepsilon_F \) is Fermi energy in graphene, \( C_{it} \) is the sheet capacitance of top (back) oxide, \( C_a \) is the interface traps capacitance assumed here to be energy independent. We found an explicit dependence of the Fermi energy as function of the both gate voltages

\[ \varepsilon_F (V_1, V_2) = \left( m^2 \varepsilon_{ad} + 2 \varepsilon_{ad} \varepsilon_{Geff} \right)^{1/2} - m \varepsilon_{ad} , \]

(3)

\[ m = 1 + \frac{C_a}{C_1 + C_2} , \quad \varepsilon_{ad} = \frac{\pi \hbar^2 v_F^2 (C_1 + C_2)}{2e^2} , \]

(4)

which represent simple generalizations of the parameters defined for a single gate case (if one oxide capacitance much larger than another, all equations transform into a single gate form)[7]. The characteristic energy \( \varepsilon_{ad} \) is nothing but the full electrostatic energy stored in both gate capacitors per one carrier in graphene, which turns out to be gate voltage independent for zero-gap material.

Equivalent circuit for double-gate GFET is shown in Fig. 2.

![Fig. 2. Equivalent circuit of double-gate GFET structure](image2)

The capacitance of the gate 1 (2) per unit area at grounded gate 2 (1) is given by

\[ C_{G1(2)} = \left( \frac{1}{C_{it} + \frac{1}{C_1} + \frac{1}{C_2}} \right)^{-1} , \]

(5)
where \( C_Q \) is the quantum capacitance, \( C_a \) is the interface trap capacitance.

We calculate the channel capacitance with respect to a single gate at grounded other gate using Eqs.2,3 and 4
\[
C_{CH(1)} = \left( \frac{e\hat{n}_d}{\partial \phi_{V_{gs}}/\partial \phi} \right)_{V_{ds}} = \frac{C_Q + C_1 + C_2 + C_a}{C_Q} \tag{6}
\]
The gate and the channel capacitances are interrelated in graphene gated structures through exact relation
\[
\frac{C_{G(1)}}{C_{CH(1)}} = 1 + \frac{C_1 + C_2}{C_Q} \tag{7}
\]
Notice that the capacitance of the grounded gate is in parallel connection with the interface trap capacitance.
Following Ref. [7] we are about to obtain an explicit analytical solution of continuity equation for channel current density. Total drain current \( J_S = J_{DS} + J_{DRE} = (1 + \kappa)J_{DS} \) should be conserved along the channel
\[
\frac{dJ_S}{dy} = 0 \iff \frac{d}{dy}(n \cdot E) = 0 \tag{8}
\]
that yields an equation for electric field distribution along the channel[*]
\[
\frac{dE}{dy} = \left( \frac{e \frac{dn}{dy}}{n \frac{d \zeta}{d \phi}} \right) \left( \frac{d \phi}{dy} \right)^2 \frac{\kappa e}{\epsilon_p^2} \tag{9}
\]
where the “diffusion energy” \( \epsilon_D = n \frac{d \zeta}{d \epsilon} \) and diffusion-to-drift currents ratio \( \kappa = J_{DRE}/J_{DS} \) are assumed to be functions of only the gate voltage rather than the drain-source bias and position along the channel.
To properly derive explicit expression for control parameter \( \kappa \) we have to use the electric neutrality condition along the channel length in gradual channel approximation which is assumed to be valid even under non-equilibrium condition \( V_{DS} > 0 \). Acting similarly as in a single-gated structure one can get
\[
\kappa = \frac{\partial \phi}{\partial \phi_{V_{gs}}/\partial \phi} = \frac{\partial \phi_{V_{gs}}/\partial \phi - \partial \phi_{V_{ds}}/\partial \phi}{\partial \phi_{V_{gs}}/\partial \phi - \partial \phi_{V_{ds}}/\partial \phi} \frac{C_1 + C_2}{C_Q + C_a} \tag{10}
\]
This dimensionless parameter \( \kappa \) is assumed to be constant along the channel for a given electric biases and expressed via the ratio of characteristic capacitances. For ideal graphene channel with low interface trap density the \( \kappa \)-parameter is a function of only \( \epsilon_{ad} \) and the Fermi energy
\[
\kappa' = \frac{C_1 + C_2}{C_Q} = \frac{\epsilon_{ad}}{\epsilon_F} \tag{11}
\]
For a high-doped regime (large \( C_Q \)) and/or thick gate oxide (low \( C_m \)) when \( C_Q >> C_m \) we have \( \kappa << 1 \) and the drift current component dominates the diffusion one and vice versa.

Straightforward solution of ordinary differential Eq. 9 yields
\[
E(y) = \frac{E(0)}{1 - \left( \frac{k e V_{ds}}{1 + k \epsilon_p} \right)} \tag{12}
\]
where \( E(0) \) is electric field near the source, which should be determined from the condition imposed by a fixed electrochemical potential difference between drain and source \( V_{DS} \), playing a role of boundary condition
\[
V_{DS} = (1 + \kappa) \int E(y) dy \tag{13}
\]
where \( L \) is the channel length. Using Eqs. (12) and (13) one obtains an expressions for \( E(0) \) and electric field distribution along the channel
\[
E(0) = \frac{\epsilon_D/e}{\kappa L} \left( 1 - \exp \left( \frac{-\kappa \epsilon V_{ds}}{1 + \kappa \epsilon_p} \right) \right) \tag{14}
\]
\[
E(y) = \frac{\epsilon_D/e}{\kappa L} \left( 1 - \exp \left( \frac{-\kappa \epsilon V_{ds}}{1 + \kappa \epsilon_p} \right) \right) \tag{15}
\]

III. CURRENT-VOLTAGE CHARACTERISTICS

According general rules the total current at constant temperature can be written as gradient of the electrochemical potential taken in the vicinity of the source
\[
I_D = e W \mu_0 n_s (0) (1 + \kappa) E(0) = e W \mu_0 n_s (0) \left( 1 + \frac{1 + \kappa}{\kappa} \right) \tag{16}
\]
where \( \mu_0 \) is the low-field carrier’s mobility, \( W \) is the channel width, and the Einstein relation \( D_0 = \mu_0 e \epsilon_p / e \) is employed. Defining a saturation current drain voltage as
\[
V_{DSAT} = 2 \frac{1 + \kappa \epsilon_D}{\kappa \epsilon_p} = \frac{1 + \kappa \epsilon_D}{\kappa \epsilon_p} \tag{17}
\]
we obtain
\[
V_{DSAT} (V_1, V_2) = V_{diff} + \epsilon_D n_s (V_1, V_2) / (C_1 + C_2) \tag{18}
\]
Integration of Eq.15 yields the explicit relationship for distribution of the electric, chemical and electrochemical potential \( \mu = \zeta - e \phi \) potential
\[
\mu(y) - \mu(0) = \frac{e V_{DSAT}}{2} \ln \left( 1 - \frac{y}{L} \right) \tag{19}
\]
where \( \mu(0) \) is the electrochemical potential nearby the source controlled by the gate-source bias \( V_{GS} \). For any gate voltage \( V_{GS} \) (and corresponding \( \kappa(V_{gs}) \)) the full drop of electrochemical potential \( \mu \) on the channel length is fixed by the source-drain bias \( \mu(L) = \mu(0) - eV_{DS} \). General relation for drain current (Eq.16) can be rewritten using low-field conductance given by

* Notice a typo in Eq.65 of Ref.[7]: lost a power 2 in an intermediate relation.
\( g_{ds} = (W/L) e \mu_0 n_{so} = (W/L) \sigma_0 \) (\( n_{so} \) is the carrier density nearby the source) as

\[
I_D = \frac{1}{2} g_{ds} V_{DSAT} \left( 1 - \exp \left( -2 \frac{V_{DS}}{V_{DSAT}} \right) \right). \tag{20}
\]

IV. TWO CURRENT SATURATION MODES

The field-effect transistor is fundamentally non-linear device working at large biases generally on all electrodes. The saturation of the channel current in the FETs at high source-drain electric field has two-fold origin, namely, (i) the current blocking due to carrier density depletion near the drain, and (ii) the carrier velocity saturation due to optical phonon emission. The saturation current for pinch-off case arises due to saturation of lateral electric field near the source. Using the Einstein relation in a form \( \frac{Q_{dc}}{\sigma} = \mu_0 \)

the pinch-off saturation current in Eq. 16 may be represented in an alternative form

\[
I_{DSAT} = W n_{so} v_S, \quad \text{where the characteristic velocity is defined as}
\]

\[
v_S = \frac{\mu_0 V_{DSAT}}{2L}. \tag{21}
\]

The current saturation for short-channel FETs (typically \( L \leq 0.5 \mu m \)) is bound to the velocity saturation due to scattering on optical phonons [8]. The channel current saturates due to velocity saturation at \( I_{DSAT} = W n_{so} v_{opt} \).

Note, that for the diffusive channels the saturation velocity \( v_{opt} \) is a maximum velocity of dissipative motion, which is in any case less than the speed \( v_0 \) of ballistic carriers in graphene. One can introduce the dimensionless parameter discriminating the two types of current saturation in FET [9]

\[
a = \frac{v_S}{v_{opt}} = \frac{\mu_0 V_{DSAT}}{2v_{opt} L} = \frac{V_{DSAT}}{V_{DO}}, \quad \tag{22}
\]

where a new characteristic drain voltage is defined

\[
V_{DO} = \frac{2v_{opt} L}{\mu_0} \tag{23}.
\]

\[
V_{DO} \cong 10 \left( \frac{2v_{opt}}{10^5 \text{ cm/s}} \right) \left( \frac{L}{1 \mu m} \right) \left( \frac{10^3 \text{ cm}^2 / \text{Vs}}{\mu_0} \right) \text{ V}. \tag{24}
\]

Thereby the drain current can be rewritten in a unified manner for both cases

\[
I_D = W n_{so} v_{SAT} \left( 1 - \exp \left( -\frac{\mu_0 V_{DS}}{v_{SAT} L} \right) \right) \tag{25}
\]

where \( v_{SAT} = \min \{v_{opt}, v_S\} \). A reasonable analytical interpolation can be used:

\[
v_{SAT} = v_{opt} \tanh \frac{v_S}{v_{opt}} = v_{opt} \tanh \left( \frac{\mu_0 V_{DSAT}}{2v_{opt} L} \right). \tag{26}
\]

which provides convenient analytical description of crossover between two modes of saturation.

Note, that empirical relationships for high-field drift velocity

\[
v_{DSAT}(E) = \frac{\mu_0 E}{(1 + (\mu_0 E / V_{SAT})^n)^{\frac{1}{n}}} = \frac{\mu_0 E}{(1 + (E / E_{SAT})^n)^{\frac{1}{n}}} \tag{27}
\]

originating from the early work of Thornber [10] and traditionally used in CMOS compact modeling [11] also is nothing but empirical interpolation having besides a significant shortage. This equation does not provide fast saturation and yields only \( v_{SAT} / 2^{1/n} \) at \( E = V_{SAT} / \mu_0 \). To remove this shortage for best fitting with experiments a joint interpolation is typically used in CMOS design practice with \( E_{SAT} = 2v_{SAT} / \mu_0 \) and artificial fitting to obey a formal condition \( v(E_{SAT}) = v_{SAT} \). A use of analytic interpolation Eq.26 allows to get rid of piecewise description and senseless fitting parameter \( n \).

Description of the two saturation modes can be combined by the unified expression for the drain current as function of the drain-source voltage

\[
I_D = \frac{1}{2} g_{ds} V_S \left( 1 - \exp \left( -2 \frac{V_{DS}}{V_{DO}} \right) \right), \tag{28}
\]

where generalized saturation source-drain voltage

\[
V_S = V_{DO} \tanh \frac{V_{DSAT}}{V_{DO}}. \tag{29}
\]

Fig. 3. Simulated I-V characteristics of GFET (a) as function of front gate \( V_1 \) and drain voltages \( V_2 \) calculated at \( V_2 = -30 \text{ V}, \mu_0 = 1000 \text{ cm}^2/(\text{Vs}) \), \( \alpha_1 = 16, d_1 = 15 \text{ nm}, \alpha_5 = 4, d_2 = 300 \text{ nm}, W = 1 \mu m, L = 1 \mu m, C_{it} = 0, \mu_n = 5 \times 10^6 \text{ cm/s}; (I) \ a = 0.6 \) (electrostatic pinch-off), (II) \( a = 4.7 \) (velocity saturation).

At small \( V_{DS} \) (\( V_{DS} \ll V_2 \)) the drain current is determined by only the low-field conductance \( g_{ds} \). The dimensionless parameter \( a \) discriminates the two types of current saturation in the FETs at large \( V_{DS} \). When \( a \ll 1 \) (long channel and thin gate insulators, low carrier density
and mobility) the electrostatic pinch-off prevails ("square law"), and if $a >> 1$ the carrier velocity saturation determines the saturation current of FETs

$$I_{SAT} \approx W e a m \sqrt{V_{GS}}$$  (30)

The drain current saturation mode depends on geometrical and transport parameters of the transistor ($V_{DS}$) as well as on the electric operation mode since $V_{DSAT}$ is a function of the gate voltages. Figs. 3-4 show calculated current-voltage characteristics exhibiting different modes of drain current saturation.

![Fig. 4. (a) Contour plot of drain current of double-gate GFET as function of front gate and drain voltages; $V_f = -30$ V, $\mu_0 = 5000$ cm$^2$/V s, $d_1 = 16$, $d_1 = 15$ mm, $\varepsilon_2 = 4$, $d_2 = 300$ nm, $C_g = 0$, $v_{opt} = 5 \times 10^7$ cm/s. $W = 1$ $\mu$m, (a) $L = 0.5 \mu$m ($V_{DSAT} = 1$ V), (b) $L = 1.5 \mu$m ($V_{DSAT} = 3$ V). Dashed lines separate different drain current modes: (I) the electrostatic pinch-off, (II) velocity saturation; (III) no saturation. The numbers in the white rectangles are the drain current values in mA.](image)

![VI. INTRINSIC OUTPUT CONDUCTANCE AND TRANS CONDUCTANCE OF DOUBLE-GATE GFETS](image)

VI. INTRINSIC OUTPUT CONDUCTANCE AND TRANS CONDUCTANCE OF DOUBLE-GATE GFETS

Ignoring many complications one can conclude that current-voltage characteristics with saturation may easily parameterized by the two parameters: the output conductance and the saturation voltage. The drain conductance as function of the node biases (closely connected with low-field conductance $g_m$) can be calculated as a partial derivative of drain current with a fixed $V_{GS}$

$$g_D = \left( \frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} = g_m \exp \left( \frac{-2V_{GS}}{V_{opt}} \right).$$  (31)

One of the most important small-signal parameter for high-frequency performance prediction is the intrinsic gate transconductance $g_m$. Transconductance depends generally on microscopic mobility slightly varying with the gate voltage the underlying mechanism and quantitative description of that has not been yet developed in details. Omitting here this point the microscopic mobility will be considered as to be independent on the gate bias in this report. Exact view of relation of the intrinsic transconductance for arbitrary value of the parameter $a$ depends on the choice of approximation for current and has awkward form. We will use here a convenient approximation for both gates

$$g_m(1/2) \approx \frac{W}{2L} \mu_0 C_{CH(2)} V_{SDAT} \left( 1 - \exp \left( \frac{-2V_{GS}}{V_{opt}} \right) \right).$$  (32)

The transconductance $g_m$ increases linearly with $V_{DS}$ up to saturation on a maximum level

$$g_m(1/2) \approx \frac{W}{2L} \mu_0 C_{CH(2)} V_{SDAT} = \frac{W}{2L} \mu_0 C_{CH(2)} V_{SDAT} \left( V_{DS} > V_{DSAT} \right)$$

$$g_m(1/2) \approx \frac{W}{2L} \mu_0 C_{CH(2)} V_{SDAT} = \frac{W}{2L} \mu_0 C_{CH(2)} V_{SDAT} \left( V_{DS} > V_{DSAT} \right).$$

Access and parasitic contact resistances can significantly degrade extrinsic performance characteristics of GFETs. We ignore yet the charge multiplication effects with characteristic super-linear dependence on drain voltage in this report. These effects occurs typically at high $V_{DS}$ and low charge densities in graphene when the channel driven electric fields nearby the drain are maximum and validity of semi-classical diffusion-drift approximation is failed.

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