PERFORMANCE OF SVM ALGORITHM IMPLEMENTED ON FIXED POINT ADSP-BF527

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ABSTRACT

With the availability of low cost high performance DSP chips characterized by the execution of most instructions in one instruction cycle, complicated control algorithms can be executed with fast speed, making very high sampling rate possible for digitally-controlled inverters. Control methods, which generate the necessary pulse space vector modulation (SVM) have been discussed extensively in literature. These could be classified as voltage controlled and current controlled SVM. All these methods aim at generating inverter output voltage without low-order harmonics.

This paper presents theoretical and experimental aspects for DSP-based algorithm to generate space vector modulation (SVM) signals.

Index Terms— Digital signal processing (DSP). Space vector pulse width modulation. Inverter.

1. SVM GENERATION AND IMPLEMENTATION

Traditionally, three phase inverters are used to power AC drives. Three commonly used Pulse Width Modulation (PWM) techniques include sinusoidal, hysteresis (bang-bang), and space-vector (symmetrical or asymmetrical) implementations. The SVM is an effective method to generate sinusoidal voltage. It generates minimum harmonic distortion to the currents in the windings of a 3 phase AC Machine. [1] [2].

we use three timers to generate the three SVM signals. However, the objective is to control six IGBTs of the inverter, so we will need another three additional complementary signals. The difficulty is that short circuit can occur in the inverter if both complementary IGBTs turn ON at the same time. Certainly, for complementary SVM signals, the transition is not instantaneous. Thus, we added to the inverter circuit six LM555, which delay the pulses high in the range of 6μs yield between the input and output.

A program for DFIG digital control has been developed under VisualDSP++ 5.0 in assembly code for the ADSP-BF527[3]. All numbers are represented in the fixed-point format. This gives us the advantage of rapid calculation, but has the disadvantage of inappropriate precision.

Indeed, the Blakfin processor represents the numbers in classical Q15 fixed format, or in Q31 fixed format. It was found that this representation of data is not comfortable for mathematical calculations especially in cases of multiplication operations. We can’t get the high desired precision.

Even if the two presented operand values are on 32 bits, only the upper part of each operand (16bits) is used for a Q15 multiplication resulting in 32bits. This leads one error in the result, and this error becomes much greater when there is a large difference in the order of magnitude of the two operands.

Knowing that the floating-point is more suitable for mathematical calculation, in this work, we use subroutines allowing the passage between the two representations fixed-point (Q31) and floating-point format.

The idea is to divide the 32 bits in two parts of 16bits. The higher 16 bits are used for the mantissa, while the lower 16bits are reserved for the exponent.

We will present open-loop control results . The objective is to test the validity of the developed algorithm including: Timers initialization, Park transformation, Calculation of the SVM pulses and their generation with the Core-Timer interruption.

2. FUNDAMENTAL AND SWITCHING FREQUENCY

The sinus function generation is based on the Taylor series development with the angle between -π and +π. For DSP implementation, the values are divided by π, so the angle values will be between -1 and +1.

The increment of the angle θ is calculated by the equation:

Δθ = \frac{2\pi}{Nc} = 2/Nc

(1)

Nc is the ratio between the fundamental frequency and switching frequency. According to this ratio, we calculate the period Tz following equation (8):

2 Tz = Tf/N

(2)

Tf is the fundamental signal period.

So the T_period register of the Core-timer is charged with the value calculated by:

T_period = \frac{CCK}{fN (Tscal+1)}

(3)
We use equations (1) (2) and (3) to calculate the period of SVM Fundamental and switching frequency [4][5]. So we have new commutation frequency equal to 2.25 KHz.

3. DSP IMPLEMENTATION RESULTS

The experimental setup is part of a research project that aims to develop advanced control strategy of doubly fed induction generator (DFIG).

The inverter feeds the rotor of the DFIG at the constant frequency of 5Hz and a DC bus voltage of 40V.

Figure 1 and figure 2, present results obtained with the Lab-Volt module and that obtained by our algorithm respectively. The comparison between the two, attest the performance of our algorithm. The rotor current shown on figure 5 presents little harmonic pollution compared to that of figure 4.

4. CONCLUSION

The ADSP-BF527 is highly performing for audio and image processing. However, with some change in number representation, this DSP have the same behaviour as any DSP specified for electric machine control, of course, with some assembly programming code added to the SVM algorithm.

Experimental results clearly attest the effectiveness of the SVM Algorithm implementation. We think, that this methodology can be used with any DSP in the objective of alternative control drive that need SVM control.

For future work, it is planned to thoroughly explore reliable advanced control strategy for DSP implementation based on the same methodology.

5. REFERENCES

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