A 16 bit 200 kS/s successive approximation register ADC with foreground on-chip self-calibration

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Abstract In this paper, an 8-channel 16 bit 200 kS/s successive approximation register analog-to-digital converter (SAR ADC) realized in 130 nm SOI CMOS technology is presented. A capacitor-resistor hybrid digital-to-analog converter (DAC) is adopted in this design to avoid the bulky capacitor array. In addition, an on-chip self-calibration technique is proposed to calibrate the mismatch of the capacitors in the DAC. To simplify the calibration logic of the resistor DAC, an auxiliary capacitor is added in the capacitor DAC to replace the resistor DAC for calibration. Moreover, the added auxiliary capacitor can also be utilized to correct the errors caused by the incomplete settling of reference voltage during the conversion. The measured results show that signal-to-noise-and-distortion-ratio (SNDR) and spurious-free-dynamic-range (SFDR) compared with it without calibration are improved from 76.51 dB to 85.82 dB and 80.84 dB to 95.14 dB, respectively. The proposed ADC occupies an active area of 0.966 mm² and consumes a total power of 3.1 mW.

Keywords: SAR ADC, capacitor-resistor hybrid DAC, on-chip self-calibration

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Technology scaling facilitates the recent trend towards large mixed-signal system-on-chip (SOC) solutions, which integrate not only digital circuitry but also analog circuitry on the same die. As the interfaces between analog and digital parts, Analog-to-digital converter (ADC) plays a key role in it [1, 2, 3, 4, 5]. Besides, the overhead of area and power consumption should be reduced as much as possible for such an essential on-chip system. Successive approximation register (SAR) ADC is widely used in SOC because it enables the implementation of low power and small area. This work presents an 8-channel 16 bit 200 kS/s SAR ADC applied in a SOC on satellites, which is used to convert the signals of temperature sensors and magnetic torque sensors into digital signals.

Generally, SAR ADC uses binary capacitor arrays as the digital-to-analog converter (DAC) parts. However, the number of capacitors in the capacitor DAC (CDAC) increases exponentially with the resolution improvement of the ADC, resulting in a bulky capacitor array in the design. To solve the problem, the ADC with split-capacitor structure is widely studied [6, 7, 8, 9, 10, 11, 12, 13, 14, 15]. By using split-capacitor structure, the capacitor array is divided into two segments: Most Significant Bit (MSB) part and Least Significant Bit (LSB) part. The capacitors in LSB part are in series with a bridge capacitor so that the equivalent values are scaled down. However, the linearity may be severely damaged because the fractional-value bridge capacitor is difficult to match and highly sensitive to the parasitic effect. This paper adopts a capacitor-resistor hybrid DAC structure (C-RDAC) [16, 17, 18, 19, 20]. By using this structure, the bridge capacitor can be eliminated while keeping a small input capacitance. Apart from bulky capacitor arrays, the mismatch of capacitors is also a critical issue for high-resolution SAR ADC. Many techniques were proposed to calibrate the mismatch of capacitors [21, 22, 23, 24, 25, 26, 27]. For example, literature [22] estimates the weights of MSB capacitors using the lower LSB capacitors of CDAC. Literature [23] uses the least-mean-square (LMS) algorithm to estimate the actual weight of each capacitor in the CDAC. Most of these literatures estimate mismatch by introducing a calibration circuit, however, the actual calibration is done via off-chip software processing, which makes the design of the SOC more complicated. This paper presents an on-chip self-calibration technology where the mismatch of capacitors will be compensated immediately once it is estimated. Therefore, extra calculations are no longer needed. Moreover, to make the calibration technology more suitable for the C-RDAC, an auxiliary capacitor is added in the capacitor DAC to replace the resistor for calibration. The calibration logic circuit can be simplified and the power consumption of calibration can be reduced through adding the auxiliary capacitor.

2. Proposed ADC architecture

Fig. 1 shows the architecture of the proposed 8-channel 16 bit 200 kS/s SAR ADC. To reduce the area and power consumption, one ADC core is shared by 8-channel. Each channel has an input buffer to receive the signal from a front-end sensor. Then, the mux switch determines which channel is sampled by the ADC core. The ADC core mainly includes a bootstrap sampling switch, a capacitor DAC (CDAC), a resistor DAC (RDAC), a calibration DAC (CAL_DAC), a...
Fig. 1 The architecture proposed ADC comparator, SAR logic circuit, and calibration logic circuit. Among them, RDAC is used to generate the reference voltages for LSBs comparison; and CAL_DAC can estimate and compensate the mismatch of four MSB capacitors.

3. Design implementation

3.1 Capacitor-resistor hybrid DAC design

This paper adopts capacitor-resistor hybrid DAC (C-RDAC) structure. Fig. 2 shows the single-ended structure of the CDAC and the RDAC, and their combinations for the 16-bit ADC. The actual circuit is differential. There are 11 capacitors in the CDAC, where $C_0$-$C_8$ are applied to determine $B_7$-$B_{15}$ of output code. $C_0$ is used to replace RDAC when ADC works in calibration mode. Moreover, during the conversion, it can also correct the error caused by the incomplete settling of reference voltage as a redundancy capacitor. $C_R$ is the coupling capacitor that connects the CDAC and RDAC. RDAC consists of 127 resistors and determines the $B_0$-$B_6$ of output code. In the conventional hybrid DAC, there is static power dissipation in the resistor ladder when CDAC is working normally [28, 29, 30]. To solve this problem, the R-ladder is connected to $V_{cm}$ when it is idle. Thus, the static power consumption is eliminated and the voltage of $C_R$ is kept constant. During the comparison of the least seven LSBs, two terminals of R-ladder are connected to $V_{RP}$ and $V_{RN}$, respectively. $V_{RP}$ and $V_{RN}$ are the reference of the ADC, and they are provided directly off-chip. Among them $V_{RP} = 3.3$ V, and $V_{RN} = 0$ V. In each step, the mux switch is changed according to the previous decisions, which also results in a change in the reference voltage of $C_R$.

3.2 Calibration design

Many calibration methods have been proposed for ADCs with different architectures. For SAR ADC, a common calibration method is to add an auxiliary DAC to estimate the mismatch of capacitors in the CDAC. However, the actual calibration is done off-chip with this method in many papers, which is inconvenient for an ADC IP used in the SOC system. This paper proposed a foreground self-calibration circuit that can calibrate the mismatch of the capacitor on-chip, and it is suitable for the C-RDAC.

The schematic of the proposed calibration circuit is shown in Fig. 3. A CAL_DAC is connected to the output of CDAC. And there are five sub-CDACs in the CAL_DAC. Cal_5 to Cal_8 are used to calibrate $C_3$ to $C_8$, while Cal_os is used to calibrate the offset of comparator. Since the proposed calibration technique compensates the mismatch immediately after the mismatch of capacitors in the CDAC is measured, the order of capacitor to be calibrated is very important. Fig. 4 shows the calibration scheme and status of each circuit after the ADC is powered on. In order to prevent the influence of comparator offset on the calibration of mismatch of capacitors, the comparator offset voltage should be calibrated prior to the mismatch of CDAC. The concrete process of the comparator offset voltage calibration is shown in Fig. 5. The calibration algorithm operates in two phases. In phase I, all capacitors are connected to $V_{cm}$, as shown in Fig. 5(a). In phase II, the differential input of comparator...
is disconnected from \( V_{cm} \). Cal_{os} in the CAL_DAC can be used to digitize the residual voltage in SAR conversion, as shown in Fig. 5(b). In addition, to eliminate the influence of noise, the calibration of comparator offset will be operated 16 times, then the average value is taken as the final offset calibration code.

The first phase of calibrating \( C_5 \) is the same as that of the calibration of comparator offset, as shown in Fig. 5(a). In phase II, the top plates of capacitors are disconnected from \( V_{cm} \); the bottom plates of \( C_5 \) and \( C_0 \) to \( C_4 \) are connected to \( VR_P \) and \( VR_N \), respectively, while the connection of higher bit than \( C_5 \) keep constant. The switch positions in the negative branch of the CDAC are inverted to that of the positive branch. In particular, the connection of Cal_{os} needs to follow the offset calibration code. As shown in Fig. 6, supposing the offset calibration code is ‘110’, the capacitors in Cal_{os} should connect \( VR_P \), \( VR_P \) and \( VR_N \) in order. So, there is no comparator offset when calibrating the mismatch of \( C_5 \). At last, the Cal_5 operates like a SAR ADC and search the mismatch of \( C_5 \). The average output of 16-time calibration process is taken as the calibration code of \( C_5 \).

The proposed ADC adopts C-RDAC, an auxiliary capacitor \( C_{0r} \) was added to the CDAC. The capacitance of \( C_{0r} \) equals to the capacitance of \( C_R \). When ADC works in calibration mode, the capacitor \( C_{0r} \) participates in calibration instead of \( RDAC \). If \( RDAC \) participates in calibration, the voltage of the bottom plate of \( C_R \) needs to change among \( VR_P \), \( VR_N \), and \( V_{cm} \). To realize this, 7 signals need to be generated to control 274 transmission gates, as shown in Fig. 2. Moreover, two terminals of \( RDAC \) are connected to \( VR_P \) and \( VR_N \), respectively. The total resistance of 127 resistors is 50k ohm, so the power of \( RDAC \) is

\[
P_{RDAC} = \frac{(VR_P - VR_N)^2}{2 \times R_{total}} = 2.2 \times 10^{-4} W \quad (1)
\]

However, by using \( C_{0r} \) participate in calibration only 1 signal is needed to control 3 transistors. Moreover, two terminals of \( RDAC \) are both connect to \( V_{cm} \), so there is no static current in the RDAC. The capacitor \( C_{0r} \) consumes energy only when it is charged or discharged by the reference voltage. The power is

\[
P_{C_{0r}} = \frac{1}{2} C_{0r} V^2 f = 2.2 \times 10^{-8} W \quad (2)
\]

\( C_{0r} = 20 \text{ fF} \) and \( f = 200 \text{ kHz} \). Table II shows the comparison of the complexity of the logic circuits and power consumption when using \( RDAC \) and \( C_{0r} \) for calibration. From which can be seen that using \( C_{0r} \) to participate in calibration

### Table II

| | Complexity of the logic circuit | Power |
|---|---|---|
| RDAC | 7 control signals | 2.2 \times 10^{-4} W |
| \( C_{0r} \) | 1 control signal \( + \text{274 transmission gates} \) | 2.2 \times 10^{-8} W |
has simpler logic circuits and lower power consumption. To sum up, the proposed calibration technique can realize the on-chip calibration at the expense of acceptable extra area overhead, where the area of CAL_DAC is only 1/32 of CDAC. In addition, by using $C_0$ participate in calibration instead of RDAC can simplifies the logic of calibration and eliminates static power consumption.

4. Measurement results

The proposed ADC is fabricated in 1P7M 130 nm silicon-on-insulator (SOI) CMOS technology. Fig. 7 shows the die microphotograph of the fabricated ADC. The core area occupies $1.38 \text{ mm} \times 0.7 \text{ mm}$. Using 200 kS/s sampling clock, the ADC core consumes 3.1 mW in 3.3 V supply. Fig. 8 shows the dc linearity performance with and without the calibration. Before calibration, the INL is $-5.9/+7.4$ LSB, mainly due to the mismatch of MSB capacitor. After calibration, the INL is $-2/+3$ LSB. It is limited by the linearity of input buffer. Fig. 9 shows the spectrum with 300 Hz input signal with and without calibration. The SNDR and SFDR can achieve 85.82 dB and 95.14 dB, respectively. Compared to the results before calibration, SNDR and SFDR are increased by 9.31 dB and 14.3 dB, respectively. The results meet the design target for an ADC IP used in a SOC system.

![Die microphotograph.](image)

![Fig. 7 Die microphotograph.](image)

![INL LSB vs. Code](image)

![DNL LSB vs. Code](image)

![Measured spectrum of the chip](image)
Table III: Comparison of recent high-resolution ADCs

| Technology (nm) | [31] | [32] | [33] | This work |
|----------------|------|------|------|----------|
| Resolution     | 176  | 250  | 46   | 130      |
| SNR (dB)       | 82   | 95.3 | 95.1 | 95.14    |
| Power (mW)     | 0.52 | 4.5  | 0.31 | 0.56     |
| 1 LSB INL      | 6.75 | 105  | 0.0017 | 0.11    |
| calibration    | Offchip | Offchip | On-chip | On-chip |

5. Conclusion

This paper proposed a foreground on-chip self-calibration technique which is suitable for the capacitor-resistor hybrid DAC structure. By adding an auxiliary capacitor at the end of the CDAC, the control logic of the RDAC is simplified, and the power consumption of the RDAC is reduced when ADC works in calibration mode. Moreover, when ADC works in conversion mode, this capacitor can correct the error caused by incomplete setting of reference voltage. By using this calibration method, the ADC compensates the mismatch immediately after measuring the mismatch of a capacitor, which eliminates the extra calculations and simplifies the logic circuit. The measurement results show that the SNDR and SFDR can achieve 85.82 dB and 95.14 dB, respectively.

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References

[1] K. Yoshioka, et al.: "A 20ch TDC/ADC hybrid SoC for 240 × 96-pixel 10%-reflection < output 0.125%–precision 200nm-range imaging LiDAR with smart accumulation technique," IEISSCC Dig. Tech. Papers (2018) 92 (DOI: 10.1109/isscc.2018.8310199).
[2] C. Erdmann, et al.: "A modular 16NM Direct-RF TX/RX embedding 9GS/s DAC and 4.5GS/s ADC with 90DB isolation and sub-80PS channel alignment for monolithic integration in 5G base-station SoC," IEEE Symposium on VLSI Circuits Dig. Tech. Papers (2018) 219 (DOI: 10.1109/vlsic.2018.8502292).
[3] H. Zhou, et al.: "Design of a 12-bit 0.83 MS/s SAR ADC for an IPM SoC," IEEE SOCC Dig. Tech. Papers (2015) 175 (DOI: 10.1109/socc.2015.7406935).
[4] T. Miki, et al.: "A 2-GS/s 8-bit time-interleaved SAR ADC for millimeter-wave pulsed radar baseband SoC," IEEE J. Solid-State Circuits 52 (2017) 2712 (DOI: 10.1109/jssc.2017.2732732).
[5] Y. He, et al.: "Blind-LMS based digital background calibration for a 14-Bit 200 MS/s pipelined ADC," IEEE VLSI-SoC (2013) 348 (DOI: 10.1109/vlsisoc.2013.673307).
[6] Y. Zhu, et al.: "Histogram-based ratio mismatch calibration for bridge-DAC in 12-bit 120 MS/s SAR ADC," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 24 (2016) 1203 (DOI: 10.1109/tvlsi.2015.2442258).
[7] R. Xu, et al.: "Digitally calibrated 768 kS/s 10-b minimum-size SAR ADC array with dithering," IEEE J. Solid-State Circuits 47 (2012) 2129 (DOI: 10.1109/jssc.2012.2198350).
[8] W. Guo, et al.: "A low-power 10-bit 50-MS/s SAR ADC using a parasitic-compensated split-capacitor DAC," IEEE International Symposium on Circuits and Systems (2012) 1275 (DOI: 10.1109/iscas.2012.6271470).
[9] Y. Guo, et al.: "Non-binary digital calibration for split-capacitor DAC in SAR ADC," IEEE Electron. Express 12 (2015) 20150001 (DOI: 10.1587/elex.12.20150001).
[10] J.-H. Eo, et al.: "A 1V 200kS/s 10-bit successive approximation ADC for a sensor interface," IEEE Electron. Express 194-C (2011) 1798 (DOI: 10.1587/transiele.e49-c.1798).
[11] J.-Y. Um, et al.: "A digital-domain calibration of split-capacitor DAC for a differential SAR ADC without additional analog circuits," IEEE Trans. Circuits Syst. I, Reg. Papers 60 (2013) 2845 (DOI: 10.1109/tcsi.2013.2252745).
[12] Y. He, et al.: "A 14-bit successive-approximation AD converter with digital calibration algorithm," IEEE ASIC/SOC (2009) 234 (DOI: 10.1109/asics.2009.5351481).
[13] X. Zhang, et al.: "A 12-bit 200kS/s SAR ADC with digital self-calibration," IEEE IAC (2017) 2531 (DOI: 10.1109/iaeac.2017.8054480).
[14] J.A. McNiel, et al.: "All-digital background calibration of a successive approximation ADC using the "split ADC" architecture," IEEE Trans. Circuits Syst. I, Reg. Papers 58 (2011) 2355 (DOI: 10.1109/tcsi.2011.2123590).
[15] M. Yoshioka, et al.: "A 10-b 50-MS/s 820-pW SAR ADC with on-chip digital calibration," IEEE Trans. Biomed. Circuits Syst. 4 (2010) 410 (DOI: 10.1109/tbcs.2010.2081362).
[16] B. Rikan, et al.: "A 10- and 12-Bit multi-channel hybrid type successive approximation register analog-to-digital converter for wireless power transfer system," Energies 11 (2018) 2673 (DOI: 10.3390/ en11102673).
[17] S.A. Zahrui, et al.: "Review of analog-to-digital conversion characteristics and design considerations for the creation of power-efficient hybrid data converters," J. Low Power Electron. 8 (2018) 1 (DOI: 10.3903/jplea8020012).
[18] S. Haenssche, et al.: "A 14 bit self-calibrating charge redistribution SAR ADC," IEEE ISCAS (2012) 1038 (DOI: 10.1109/iscas.2012.6271405).
[19] Y. Kuramochi, et al.: "A 0.027-mm² self-calibrating successive approximation ADC core in 0.18-µm CMOS," IEICE Trans. Fundamentals E92-A (2009) 360 (DOI: 10.1587/transfun.e92.a.360).
[20] Y. Kuramochi, et al.: "A 0.05-mm² 110-µw 10-b self-calibrating successive approximation ADC core in 0.18-µm CMOS," IEEE ASSCC (2007) 224 (DOI: 10.1109/asscc.2007.4425771).
[21] C.-Y. Liu, et al.: "A 2.4-to-5.2 fJ/conversion-step 10b 0.5-to-4 MS/s SAR ADC with charge-average switching DAC in 90nm CMOS," IEEE ISSSCC Dig. Tech. Papers (2013) 280 (DOI: 10.1109/issscc.2013.6487735).
[22] S. Thirunakkarasu and B. Bakkaloglu: "Built-in self-calibration and digital-trim technique for 14-Bit SAR ADCs achieving ± 1 LSB INL in IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 23 (2015) 916 (DOI: 10.1109/tvlsi.2014.2321761).
[23] J. McNeill, et al.: ""Split ADC" architecture for deterministic digital background calibration of a 16-bt 1-MS/s ADC," IEEE J. Solid-State Circuits 40 (2005) 2437 (DOI: 10.1109/jsscc.2005.856291).
[24] K. Obata, et al.: "A 97.99 dB SNDR, 2 kHz BW, 37.1 µW noise-shaping SAR ADC with dynamic element matching and modulation dither effect," IEEE Symposium on VLSI Circuits (2016) 1 (DOI: 10.1109/vlsic.2016.7573463).
[25] M. Zeloufi, et al.: "A 12 bit 40 MSPS SAR ADC with a redundancy algorithm and digital calibration for the ATLAS LAr calorimeter readout," J. Instrum. 11 (2016) C01030 (DOI: 10.1088/1748-0221/11/01/c01030).
[26] X. Dai-guo, et al.: "A 1-bit 1.2 GS/s 45 MW time-interleaved SAR ADC with background calibration," IEEE Electron. Express 15 (2018) 20171235 (DOI: 10.1587/elex.15.20171235).
[27] X. Zhu, et al.: "A 6 mW 325 MS/s 8 bit SAR ADC with background offset calibration," IEEE Electron. Express 14 (2017) 20170329 (DOI: 10.1587/elex.14.20170329).
[28] B. Sedighi, et al.: "Design of hybrid resistive-capacitive DAC for SAR A/D converters," IEEE ICECS (2012) 508 (DOI: 10.1109/ices.2012.6463697).
[29] X.Y. Tong, et al.: "D/A conversion networks for high-resolution SAR A/D converters," Electron. Lett. 47 (2011) 169 (DOI: 10.1049/el.2010.3469).
[30] X. Wang, et al.: “Design considerations of ultralow-voltage self-calibrated SAR ADC,” IEEE Trans. Circuits Syst. II, Exp. Briefs 62 (2015) 337 (DOI: 10.1109/tcsti.2014.2387654).

[31] R. Guan, et al.: “16-bit 1-MS/s SAR ADC with foreground digital-domain calibration,” IET Circuits, Devices Systems 12 (2018) 505 (DOI: 10.1049/iet-cds.2017.0412).

[32] C.P. Hurrell, et al.: “An 18 b 12.5 MS/s ADC with 93 dB SNR,” IEEE J. Solid-State Circuits 45 (2010) 2647 (DOI: 10.1109/JSSC.2010.2075310).

[33] S. Minseob, et al.: “Edge-pursuit comparator: an energy scalable oscillator collapse-based comparator with application in a 74.1 dB SNDR and 20 kS/s 15 b SAR ADC,” IEEE J. Solid-State Circuits 52 (2017) 1077 (DOI: 10.1109/jssc.2016.2631299)