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Analysis of Allowable Unbalanced Load Conditions for T-Type Three-Level PWM Converter

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Abstract: Since a T-type three-level PWM converter has several advantages in terms of harmonics and conduction loss, it has been widely adopted for various low voltage applications. However, a neutral point voltage control is necessarily required for stable system operation, and an offset voltage can effectively provide the required neutral point current under unbalanced load conditions. Nevertheless, all types of unbalanced loads cannot be accommodated; in other words, there is a limitation on how much unbalanced load conditions can be allowed. Therefore, this paper analyzed the maximum allowable unbalanced load conditions in the T-type three-level PWM converter. This result can be properly utilized for an effective design verification considering unbalanced load conditions as well as a comprehensive approach for the stable system operation. The feasibility of the analytical result is verified through simulation and experimental tests.

Keywords: T-type; unbalanced; PWM converter; offset duty; neutral point current

1. Introduction

The T-type three-level PWM converter has a merit in terms of harmonic reduction by generating a multi-level output voltage waveform compared to the traditional 2-level PWM converter. Also, it can reduce conduction loss compared to a similar NPC three-level PWM converter, so it is widely considered as a candidate in low voltage applications [1,2]. Therefore, many studies are being conducted to utilize the T-type three-level PWM converter in various applications [2–7].

However, in the T-type three-level PWM converter, neutral point voltage control is essential for stable operation, and it carries out various neutral point voltage control between the upper and lower DC-link voltages depending on the application field [3,8]. To accomplish this purpose, an offset voltage is normally used, and the resultant neutral point current is inserted to the output DC-link side.

In a balanced load condition, the offset voltage is not necessary because the required neutral point current is zero. On the other hand, in an unbalanced load condition, an enough offset voltage should be provided to generate the required neutral point current value. Since this offset voltage does not affect the whole DC-link voltage and three-phase sinusoidal input current, only upper and lower DC-link voltages control can be effectively performed. However, the amount of offset voltage that can be applied is limited and varies depending on the given system specification. This implies that the balance control of the upper and lower DC-link voltages may not be achieved according to the unbalanced load condition, and means that the maximum allowable unbalanced load condition exists in the T-type three-level PWM converter.

Therefore, in this paper, based on the analytical modeling derived for the neutral point current in the T-type three-level PWM converter [9], the maximum allowable unbalanced load condition for the balance control between the upper and lower DC-link voltages is theoretically analyzed. Through this, it is possible to verify in advance how much the unbalanced load condition can be accommodated for the stable operation in the T-type...
three-level PWM converter system. To analyze this condition, a space vector PWM-based T-type three-level PWM converter operation was assumed, and simulations and experimental tests were conducted to verify its effectiveness.

2. Average Neutral Point Current

2.1. Circuit Configuration

Figure 1 shows a grid-connected power conversion system based on the T-type three-level PWM converter using an L filter. The converter was assumed to be operated as a rectifier mode; in other words, the total power flows from the AC input to the DC output.

![Figure 1. T-type three-level PWM converter system.](image)

The output loads are replaced by two current sources \(i_H\) and \(i_L\), and when independent loads are connected to the upper and lower ends of the output DC voltage as shown in Figure 1, the fluctuation of the neutral point voltage due to load difference is inevitable. Thus, the effective neutral point voltage control method is required.

Figure 2 shows the phasor diagram for the T-type three-level PWM converter operation in the steady state. Based on the grid voltage \(V_g\), it is assumed that the input grid current \(I_g\) flows with a delay of \(\Phi_1\). Considering the voltage drop of the inductor \(L\) filter including the equivalent series resistor \(R\), the output voltage \(V_o\) of the converter is applied with a delay of \(\Phi_2\) compared to the input current \(I_g\). In general, in the case of a grid-connected power conversion system, \(\Phi_1\) is controlled to be zero in order to maximize active power, but in this paper, a condition in which \(\Phi_1\) is not zero is assumed to consider a more general case.

To maintain the upper and lower DC-link voltages equivalently under unbalanced load conditions, the neutral point current \(i_n\) should be controlled relevantly. To obtain the amount of required neutral point current \(i_n\) in the given system specification, the analytical modeling has been performed.
2.2. Neutral Point Current Modeling

For convenience of analysis, it is assumed that each DC-link voltage is well regulated equivalently \((V_H = V_L = 0.5 \times V_{DC})\), and also the three-phase sinusoidal grid voltages and currents are assumed to be in balanced states. Meanwhile, it is assumed that an unbalanced load is applied to each DC-link voltage in order to consider the situation in which the neutral point current is required. Figure 3 shows the main waveforms in the steady state, and the related equations are as follows.

Here, the three-phase grid voltages \((v_{ga}, v_{gb}, \text{and } v_{gc})\) and currents \((i_{ga}, i_{gb}, \text{and } i_{gc})\) have a phase delay of \(\Phi_1\) where \(V_g\) and \(I_g\) are the maximum value. Also, the three-phase duties \((d_a, d_b, \text{and } d_c)\) have an additional phase delay of \(\Phi_2\) where \(m\) is the modulation index.

\[
\begin{bmatrix}
v_{ga} \\
v_{gb} \\
v_{gc}
\end{bmatrix} = V_g \begin{bmatrix}
\cos(\omega t) \\
\cos(\omega t - 2\pi/3) \\
\cos(\omega t + 2\pi/3)
\end{bmatrix}
\]

\(1\)

\[
\begin{bmatrix}
i_{ga} \\
i_{gb} \\
i_{gc}
\end{bmatrix} = I_g \begin{bmatrix}
\cos(\omega t - \Phi_1) \\
\cos(\omega t - 2\pi/3 - \Phi_1) \\
\cos(\omega t + 2\pi/3 - \Phi_1)
\end{bmatrix}
\]

\(2\)

\[
\begin{bmatrix}
d_a \\
d_b \\
d_c
\end{bmatrix} = m \begin{bmatrix}
\cos(\omega t - \Phi_1 - \Phi_2) \\
\cos(\omega t - 2\pi/3 - \Phi_1 - \Phi_2) \\
\cos(\omega t + 2\pi/3 - \Phi_1 - \Phi_2)
\end{bmatrix}
\]

\(3\)
The relationship between the output voltage of the converter and the duty is as follows:

\[
\begin{bmatrix}
  v_{oa} \\
v_{ob} \\
v_{oc}
\end{bmatrix} = \frac{V_{DC}}{2} \begin{bmatrix}
  d_a \\
d_b \\
d_c
\end{bmatrix}
\]  

Using the above equations, the modulation index \( m \) can be obtained as (5).

\[
m = \frac{\sqrt{(V_g - I_g \cos(\theta - \varphi))^2 + (I_g Z \sin(\theta - \varphi))^2}}{0.5 V_{DC}}
\]  

Here, \( Z \) is the magnitude of the impedance corresponding to the inductor \( L \) filter including the equivalent series resistor \( R \), and \( \theta \) is the phase angle of the impedance.

\[
Z = \sqrt{R^2 + (\omega L)^2} = \tan^{-1}\left(\frac{\omega L}{R}\right)
\]  

The three-phase duties are converted to the final duties \( d_{oa}, d_{ob}, \) and \( d_{oc} \) as shown in the lowest waveform of Figure 3 through the space vector PWM technique [10] and the addition of offset voltage for neutral point current control.

\[
\begin{bmatrix}
d_{oa} \\
d_{ob} \\
d_{oc}
\end{bmatrix} = \begin{bmatrix}
  d_a \\
d_b \\
d_c
\end{bmatrix} + \begin{bmatrix}
  1 & 1 & 1 \\
  1 & 1 & 1 \\
  1 & 1 & 1
\end{bmatrix} \begin{bmatrix}
d_{sv} \\
d_{os}
\end{bmatrix}
\]  

Here, the \( d_{sv} \) is the duty to implement the space vector PWM technique and is given by (8), and the \( d_{os} \) is the offset duty corresponding to the offset voltage.

\[
d_{sv} = -\frac{0.5}{V_{DC}} (V_{\text{max}} + V_{\text{min}})
\]
The phase difference of $\Delta \theta$ in Figure 3 comes from the offset voltage and is expressed as follows.

$$\Delta \theta = \frac{\pi}{2} - \cos^{-1}\left(\frac{2d_{os}}{3m}\right)$$ \hspace{1cm} (9)

Thus, the neutral point current can be obtained for each of the six areas (I~VI) in Figure 3, and the average value during one period of the grid voltage is calculated as follows [9].

$$i_{o,avg} = -6d_{os}I_g \cos \Delta \theta \cdot \cos \phi \cdot \frac{\sin(2\Delta \theta)}{2} + mI_g \frac{2}{\pi} \sin(2\Delta \theta) \cdot \cos \phi - 9\Delta \theta \cdot \cos \phi$$ \hspace{1cm} (10)

If assuming the balanced load condition ($\Delta \theta = 0$), the average neutral point current can be approximated as (11).

$$i_{o,avg} \simeq -6d_{os}I_g \cos \phi$$ \hspace{1cm} (11)

Through this, it can be seen that the magnitude of the approximated average neutral point current is proportional to the maximum value of the grid current and the offset duty, and is related to $\Phi_2$ corresponding to the phase delay between the grid current and the output voltage of the converter.

3. Allowable Unbalanced Load Conditions

Based on the analytical result for the neutral point current, in order to analyze the allowable unbalanced load condition in the T-type three-level PWM converter, the equivalent circuit for the converter’s output side was used as shown in Figure 4.

Figure 4. Equivalent circuit of output DC-link side.

Through the balanced three-phase values, the following equation is satisfied.

$$i_p + i_o + i_n = 0$$ \hspace{1cm} (12)

Here, the $i_p$ and $i_n$ are the positive and negative side instantaneous output current, respectively.
In steady state, the average current flowing through the capacitor becomes zero, so the neutral point current can be expressed as follows.

\[ I_o = -I_n - I_p = I_L - I_H \]  

(13)

Here, the capital letters mean the average value of each current shown in Figure 4. From (11) and (13), the required offset duty in the system is expressed as follows.

\[ d_{os} \simeq \left| (I_L - I_H) \left( \frac{\pi}{6I_g \cos \phi_2} \right) \right| \]  

(14)

From (14), it can be known that the offset duty is not required under a balanced load condition \((I_L = I_H)\), while some offset duty is required under unbalanced load conditions \((I_L \neq I_H)\). However, the required offset duty should be smaller than the maximum possible offset duty that is allowable in the system, and it is given by (15) under the space vector PWM based operation.

\[ d_{os} \leq d_{os, max} = 1 - \frac{\sqrt{3}}{2}m \]  

(15)

Here, the modulation index \((m)\) is calculated from (5) through the system specification. In other words, the maximum possible offset duty \((d_{os, max})\) in (15) is a value determined by the converter’s topology and operational point, which means any unbalanced loads can be controlled by applying the required offset duty without changing the hardware if the condition of (15) is satisfied. However, in case of out of that condition, it can be solved through additional circuit configuration such as voltage balancer [11–14].

Figure 5 shows the maximum possible offset duty \((d_{os, max})\) and the actually required offset duty \((d_{os})\) under unbalanced load conditions based on the system specifications in Table 1. The grid current \((I_g)\) in (14) can be calculated by using the output power \((P_o)\) and the grid line-to-line voltage \((V_{g,ll})\) given in Table 1.

\[ d_{os} \simeq \left| (I_L - I_H) \left( \frac{\pi V_{g,H, l} \cos \phi_1}{2\sqrt{6}P_o \cos \phi_2} \right) \right| \]  

(16)
Table 1. System Specifications.

| Parameter                          | Value       |
|-----------------------------------|-------------|
| Output power ($P_o$)              | 3.2 kW      |
| Output DC-link voltage ($v_H, v_L$) | 200 V     |
| Grid line-to-line voltage ($V_{g, ll}$) | 220 Vrms |
| Filter inductance ($L$)           | 3 mH      |
| Equivalent series resistance ($R$) | 0.1 Ω     |
| Output DC-link capacitance ($C$)  | 1680 uF   |
| Switching frequency ($f_s$)       | 10 kHz    |

While the upper load was fixed at 100%, the change in duty was monitored by gradually decreasing the lower load as shown in Figure 5 where $\Delta P(\%)$ corresponding to the horizontal axis is expressed as (17).

$$\Delta P(\%) = \frac{I_H - I_L}{I_H} \times 100$$  \hspace{1cm} (17)

It can be seen that the required offset duty ($d_{oa}$) increases as the difference in each output power increases. Until the required offset duty ($d_{oa}$) is smaller than the maximum possible offset duty ($d_{oa\_max}$), the balance control of each DC-link voltage is well performed even under unbalanced load conditions. However, when the difference in output power becomes greater than about 43%, the required offset duty ($d_{oa}$) exceeds the maximum possible offset duty ($d_{oa\_max}$) so that balanced output voltage control cannot be maintained anymore. This allows determination of the maximum allowable unbalanced load conditions for a given system.

4. Simulation and Experimental Results

Simulations were performed through PSIM to verify the analyzed allowable unbalanced load conditions. Table 1 shows the system specifications and parameter values used in the simulation.

Figure 6 shows the operational waveforms under a balanced load condition. Each 100% load was applied to both upper and lower DC-link voltages, and the three-phase sinusoidal grid voltages and currents were controlled to be in phase. Since the real neutral point current ($i_o$) is a pulsating waveform due to the PWM operation, the averaged neutral point current ($i_{o\_Ts}$) at every sampling period was measured. As expected, the average neutral point current value during one grid period was zero due to the balanced load condition. Also, it can be seen that the upper and lower DC-link voltages ($v_H$ and $v_L$) maintained a balanced state. As well, no offset duty was applied to the final duty ($d_{oa}$), in other words, the final duty ($d_{oa}$) was symmetrical based on 0.5.

Figure 7 shows the operational waveforms under unbalanced load conditions. In both cases, 100% load was applied to the upper DC-link, and the load connected to the lower DC-link was reduced. Figure 7a is a condition where the output power deviation ($\Delta P$) corresponds to 40%. Thus, the offset duty was included in the final duty ($d_{oa}$), and it can be seen that the final duty was shifted to the upper side as a whole. Nevertheless, as expected in Figure 5, it corresponds to the condition that the balance control can be performed, and the upper and lower DC-link voltages maintain a balanced state. However, Figure 7b is a condition where the output power deviation ($\Delta P$) corresponds to 45%, and the final duty ($d_{oa}$) is caught at the upper limit, so the relevant balance control cannot be performed. This is also consistent with what is expected in Figure 5, and the upper and lower DC-link voltages show an unbalanced state.
Figure 6. Operational waveforms under balanced load condition.

Figure 7 shows the operational waveforms under unbalanced load conditions. In both cases, 100% load was applied to the upper DC-link, and the load connected to the lower DC-link was reduced. Figure 7a is a condition where the output power deviation ($\Delta P$) corresponds to 40%. Thus, the offset duty was included in the final duty ($d_{oa}$), and it can be seen that the final duty was shifted to the upper side as a whole. Nevertheless, as expected in Figure 5, it corresponds to the condition that the balance control can be performed, and the upper and lower DC-link voltages maintain a balanced state. However, Figure 7b is a condition where the output power deviation ($\Delta P$) corresponds to 45%, and the final duty ($d_{oa}$) is caught at the upper limit, so the relevant balance control cannot be performed. This is also consistent with what is expected in Figure 5, and the upper and lower DC-link voltages show an unbalanced state.

Figure 8 shows the photograph for the experimental test.

Figure 9 shows the experimental waveforms under a balanced load condition. Each 100% load was applied to both the upper and lower DC-links, and the unit power factor control was satisfied by controlling the phases between the grid line-to-line voltage ($v_{gb}$) and grid phase current ($i_{ga}$) to be $\pi/6$. Also, the neutral point current ($i_o$) was an averaged waveform at every sampling period, and it can be seen that the average value was zero due to the balanced load condition. Also, the upper and lower DC-link voltages ($v_H$ and $v_L$) were balanced, and the final duty ($d_{oa}$) was symmetrical with respect to 0.5.

Figures 10 and 11 show the experimental waveforms under unbalanced load conditions. First, Figure 10 shows the waveforms corresponding to 100% load at the upper DC-link and 60% load at the lower DC-link, which is a condition where the output power deviation ($\Delta P$) corresponds to 40%. Due to the total load reduction, the peak value of the grid current ($i_{ga}$) was decreased compared to Figure 9, and the average value of the neutral point current ($i_o$) was also decreased to about $-3.2$ A because of the unbalanced load. Nevertheless, the offset duty was applied to the final duty ($d_{oa}$), and thus the duty was shifted upward as a whole. Thus, as expected in Figure 5, each DC-link voltage maintained a balanced state.

Figure 11 shows the waveforms corresponding to 100% load at the upper DC-link and 55% load at the lower DC-link, which is a condition where the output power deviation ($\Delta P$) corresponds to 45%. The final duty ($d_{oa}$) was caught at the upper limit, and the relevant balance control was not achieved, which is consistent with what is expected in Figure 5. Therefore, it was confirmed that the upper and lower DC-link voltages are not regulated equivalently.

Thus, the analysis for the allowable unbalanced load condition in the T-type three-level PWM converter was verified through the simulation and experimental results.

Figure 7. Operational waveforms under unbalanced load condition. (a) Output power deviation ($\Delta P$): 40% (b) Output power deviation ($\Delta P$): 45%.

Figure 8 shows the photograph for the experimental test.
Figure 8. Photograph of the experimental test.

Figure 9 shows the experimental waveforms under a balanced load condition. Each 100% load was applied to both the upper and lower DC-links, and the unit power factor control was satisfied by controlling the phases between the grid line-to-line voltage ($v_{gab}$) and grid phase current ($i_{ga}$) to be $\pi/6$. Also, the neutral point current ($i_o$) was an averaged waveform at every sampling period, and it can be seen that the average value was zero due to the balanced load condition. Also, the upper and lower DC-link voltages ($v_H$ and $v_L$) were balanced, and the final duty ($d_{oa}$) was symmetrical with respect to 0.5.

Figures 10 and 11 show the experimental waveforms under unbalanced load conditions. First, Figure 10 shows the waveforms corresponding to 100% load at the upper DC-link and 60% load at the lower DC-link, which is a condition where the output power deviation ($\Delta P$) corresponds to 40%. Due to the total load reduction, the peak value of the grid current ($i_{ga}$) was decreased compared to Figure 9, and the average value of the neutral point current ($i_o$) was also decreased to about $-3.2$ A because of the unbalanced load. Nevertheless, the offset duty was applied to the final duty ($d_{oa}$), and thus the duty was shifted upward as a whole. Thus, as expected in Figure 5, each DC-link voltage maintained a balanced state.

Figure 9. Experimental waveforms under balanced load condition. (a) $v_{gab}$: grid line-to-line voltage; $i_{ga}$: grid current; $d_{oa}$: final duty; $i_o$: averaged neutral point current. (b) $v_{gab}$: grid line-to-line voltage; $i_{ga}$: grid current; $v_H$, $v_L$: DC-link voltage.
Figure 10. Experimental waveforms under unbalanced load condition corresponding to 40% deviation of output power. (a) \( v_{gab} \): grid line-to-line voltage; \( i_{ga} \): grid current; \( d_{oa} \): final duty; \( i_o \): averaged neutral point current. (b) \( v_{gab} \): grid line-to-line voltage; \( i_{ga} \): grid current; \( v_H, v_L \): DC-link voltage.

Figure 11. Experimental waveforms under unbalanced load condition corresponding to 45% deviation of output power. (a) \( v_{gab} \): grid line-to-line voltage; \( i_{ga} \): grid current; \( d_{oa} \): final duty; \( i_o \): averaged neutral point current. (b) \( v_{gab} \): grid line-to-line voltage; \( i_{ga} \): grid current; \( v_H, v_L \): DC-link voltage.

Figure 11 shows the waveforms corresponding to 100% load at the upper DC-link and 55% load at the lower DC-link, which is a condition where the output power deviation (\( \Delta P \)) corresponds to 45%. The final duty (\( d_{oa} \)) was caught at the upper limit, and the relevant balance control was not achieved, which is consistent with what is expected in Figure 5. Therefore, it was confirmed that the upper and lower DC-link voltages are not regulated equivalently.

Thus, the analysis for the allowable unbalanced load condition in the T-type three-level PWM converter was verified through the simulation and experimental results.

5. Conclusions

In this paper, the maximum allowable unbalanced load condition in the T-type three-level PWM converter was analyzed by using the theoretical modelling for the neutral point current under the space vector PWM based operation. Based on the given system parameters, it can determine the required offset duty under an unbalanced load condition. By comparing the required offset duty with the maximum possible offset duty, it can be judged whether the system operation will be stable or not. Through this, at the design level of the system, it can be analytically confirmed how much unbalanced load can be allowed in the T-type three-level PWM converter system. The validity of the theoretical analysis proposed in this paper was verified by simulation and experimental results.
Funding: This was supported by Korea National University of Transportation in 2021.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The author declares no conflict of interest.

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