Accurate deep neural network inference using computational phase-change memory

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In-memory computing is a promising non-von Neumann approach where certain computational tasks are performed within memory units by exploiting the physical attributes of memory devices. For instance, crossbar arrays of resistive memory devices can be used to store a matrix and perform analog matrix-vector multiplications at constant O(1) time complexity without intermediate movements of data. This functionality is very appealing for making energy-efficient deep learning inference hardware, where the weights of the neural network layers would be encoded in such crossbar arrays. However, due to device variability and noise, the network needs to be trained in a specific way so that transferring the digitally trained weights to the analog resistive memory devices will not result in appreciable loss of accuracy. Here, we introduce a methodology to train ResNet-type convolutional neural networks that results in almost no accuracy loss when transferring weights to analog in-memory computing hardware based on phase-change memory (PCM). Our experimental results demonstrate an as-programmed classification accuracy of 93.69% on the CIFAR-10 dataset with ResNet-32, which stays above 92.6% over a one day period, where each of the 361,722 synaptic weights of the network is programmed on just two PCM devices organized in a differential configuration.

I. INTRODUCTION

Deep neural networks (DNNs) have revolutionized the field of artificial intelligence and have achieved unprecedented success in cognitive tasks such as image and speech recognition. Platforms for deploying the model of such networks after training and performing inference in an energy-efficient manner are highly attractive for edge computing applications. In particular, internet-of-things battery-powered devices and autonomous cars could especially benefit from fast, low-power, and reliably accurate DNN inference engines. Significant progress in this direction has been made with the introduction of specialized hardware for inference operating at reduced digital precision (4 to 8-bit), such as Google’s tensor processing unit (TPU)1 and low-power graphical processing units (GPUs) such as NVIDIA T4. While these platforms are very flexible, they are based on architectures where there is a physical separation between memory and processing units. The models are typically stored in off-chip memory, leading to constant shuttling of data between memory and processing units, which limits the maximum achievable energy efficiency.

With the aim of reducing the data transfers to a minimum, significant work has been done in designing digital application-specific integrated circuits (ASICs) for implementing inference on binary neural networks (BNNs)2, where both weights and activations are represented with a single bit3. In this way, large models can potentially fit solely on the on-chip static random access memory (SRAM) and the digital operations for the data propagations are greatly simplified. Aimed at improving the energy efficiency even further, mixed-signal ASIC BNN accelerators have been developed, in which the model is stored on-chip SRAMs and the matrix-vector multiplications performed during inference are accelerated via analog in-memory computing. Various implementations such as switched-capacitor circuits4, charge-based5, and current-based6 computational circuits have been proposed and could demonstrate 1-bit arithmetic energy efficiencies of > 100 TOPS/W for matrix-vector multiplications7. However, BNNs have not yet been demonstrated to yield accuracies comparable to floating-point implementations across a wide range of network topologies and datasets8. This could limit these ASIC implementations only to a special set of problems.

Another promising avenue for designing inference accelerators is to exploit in-memory computing using non-volatile memory devices9. Both charge-based storage devices, such as Flash memory10 and resistance-based (memristive) storage devices, such as metal-oxide resistive random-access memory (ReRAM)11 and phase-change memory (PCM)12,13 are being investigated for this. In this approach, the network weights are encoded as the analog charge state or conductance state of these devices organized in crossbar arrays, and the matrix-vector multiplications during inference can be performed in situ in a single time step by exploiting Kirchhoff’s circuit laws. The fact that these devices are non-volatile (the weights will be retained when the power supply is turned off) and have multi-level storage capability (a single device can encode an analog range of values as opposed to 1 bit) is very attractive for inference applications. However, due to the analog nature of the weights programmed in these devices, only limited precision can be achieved in the matrix-vector multiplications and this could limit the achievable inference accuracy of the accelerator.

One potential solution to this problem is to train the net-
work fully on hardware\cite{11,12}, such that all hardware non-idealities would be de facto included as constraints during training. Another similar approach is to perform partial optimizations of the hardware weights after transferring a trained model to the chip\cite{13}. The drawback of these approaches is that every neural network would have to be trained on each individual chip before deployment. Off-line variation-aware training schemes have also been proposed, where hardware non-idealities such as device-to-device variations\cite{20,21}, defective devices\cite{21}, or IR drop\cite{20} are first characterized and then fed into the training algorithm running in software. However, these approaches would require characterizing and training the neural network from scratch for every chip. A more practical approach would be to have a single custom generic training algorithm that is run entirely in software which would make the network immune to most of the hardware non-idealities, but at the same time would require only very little knowledge about the specific hardware it will be deployed on. In this way, the model would have to be trained only once and could be deployed on a multitude of different chips. To this end, several works have proposed to inject noise in the training algorithm on the layer inputs\cite{23}, synaptic weights\cite{24}, and pre-activations\cite{24}. However, the previous demonstrations have generally been limited to rather simple and shallow networks, and experimental validations of the effectiveness of the various approaches have been missing.

In this work, we explore injecting synaptic weight noise during the training of DNNs in software as a generic method to improve the network resilience against analog in-memory computing hardware non-idealities. We focus on the ResNet-32 convolutional neural network (CNN) architecture, and introduce a number of techniques that allowed us to train ResNet-32 with more than 5% weight noise while retaining within 0.5% of the baseline accuracy of the network trained without noise. The effectiveness of the training procedure is then validated through hardware/software experiments using a prototype PCM chip containing 1 million devices.

II. PROBLEM STATEMENT

For our experiments, we consider a 34-layer CNN with residual feed forward connections known as ResNet-32\cite{25}. The network contains 361,722 parameters. As shown in Fig. 1, ResNet-32 has 31 convolution layers with $3 \times 3$ kernels, 2 convolution layers with $1 \times 1$ kernels, and a final fully-connected layer. It consists of 3 different ResNet blocks with 10 $3 \times 3$ kernels each. After the first convolution layer, there is a unity residual feed forward connection after every two convolution layers, except the $1 \times 1$ residual convolution connection to make output channels compatible between two layers. Each convolution layer is followed by batch normalization\cite{26}. ReLU activation is used after every batch normalization except in case of residual connections, where the ReLU activation is computed after summation. The output of the last convolution layer is then downsampled using global average pooling\cite{27}, which is followed by a single fully-connected layer. The dataset used for training the network is the well-known CIFAR-10 benchmark dataset\cite{28}. It has $32 \times 32$ pixels RGB images that belong to one of the 10 classes. The total number of images in the training set is 50,000 and the test set has 10,000 images.

The weights of all convolution layers along with the fully connected layer of ResNet-32 can be mapped on memristive crossbar arrays as follows. The weights of the fully connected layer form a 2-D matrix and hence they can be directly mapped on a crossbar array. As shown in Fig. 1d, a convolution layer weight matrix has 4 dimensions: the two spatial dimensions of the filter, the number of input channels, and the number of convolution kernels, corresponding to the number of output channels. The convolution weight matrix can be flattened into a 2-D matrix by collapsing the filters for all input channels into a single vector programmed on a crossbar column, and stacking all convolution kernels on separate columns\cite{29}. The input image is padded with zero values at the border to ensure that the convolution operation preserves the height and width of the image. Therefore, considering an input image of size $n \times n$, the convolution operation can be performed in $n^2$ matrix-vector multiplication cycles.

Each synaptic weight can be mapped on a differential pair of memristive devices that are located on two different columns. For a given layer $l$ at $(i,j)$\cite{24} synaptic element, the synaptic weight $W_{ij}^l$ is represented by the effective synaptic conductance $G_{ij}^l$ given by

$$G_{ij}^l = G_{ij}^{+} - G_{ij}^{-},$$

where $G_{ij}^{+}$ and $G_{ij}^{-}$ are the conductance values of the two devices forming the differential pair. Those device conductance values are defined as the effective conductance perceived in the operation of a non-ideal memristive crossbar array, and therefore include all the circuit non-idealities from the crossbar and periphery. The output current from the column containing the $G^{-}$ devices is subtracted from the one from the column containing the $G^{+}$ devices. The differential current output from the crossbar then routes to a digital circuitry that performs batch normalization and the corresponding activation function. For the last fully-connected layer, no batch normalization is performed. The softmax activation function can be performed off-chip if required.

The mapping between the synaptic weight $W_{ij}^l$ obtained after software training and the corresponding synaptic conductance is given by

$$G_{ij}^l = W_{ij}^l \times \frac{G_{\text{max}}}{W_{\text{max}}} + \delta G_{ij}^l = G_{T,ij}^l + \delta G_{ij}^l,$$

where $G_{\text{max}}$ is the maximum reliably programmable device conductance and $W_{\text{max}}$ is the maximum absolute synaptic weight value of layer $l$. $\delta G_{ij}^l$ represents the synaptic conductance error from the ideal target conductance value $G_{T,ij}^l = W_{ij}^l \times \frac{G_{\text{max}}}{W_{\text{max}}}$. $\delta G_{ij}^l$ is a time-varying random variable that describes the effects of non-ideal device programming (inaccuracies associated with write) and conductance fluctuations over time (inaccuracies associated with read). Possible factors leading to such conductance errors include inaccuracies
in programming the synaptic conductance to $G_{T,j}^{l}$, $1/f$ noise from memristive devices and circuits, temporal conductance drift, device-to-device variations, defective (stuck) devices, and circuit non-idealities (e.g. IR drop).

Clearly, a direct mapping of the synaptic weights of a DNN trained with 32-bit floating point (FP32) precision to the same DNN with memristive synapses is expected to degrade the network accuracy due to the added error in the weights arising from $\delta G_{T,j}^{l}$. For existing memristive technologies, the magnitude of $\delta G_{T,j}^{l}$ may range from $1 - 10\%$ of the magnitude of $G_{T,j}^{l}$, which is in general not tolerable by DNNs trained with FP32 without any constrains. Imposing such errors as constraints during training can be beneficial in improving the network accuracy. In fact, quantization of the weights or activations[36,37] and injecting noise on the weights[40], activations[41], or gradients[35] have been widely used as DNN regularizers during training to reduce overfitting on the training dataset[25]. These techniques can improve the accuracy of DNN inference when it is performed with the same model precision as during training. However, achieving baseline accuracy while performing DNN inference on a model which is inevitably different from the one obtained after training, as it is the case for any analog in-memory computing hardware, is a more difficult problem requiring additional investigations.

Although a large body of efficient techniques to train DNNs with reduced digital precision has been reported[13,38,39], it is unlikely that such procedures can generally be applied as-is to analog in-memory computing hardware due to the random nature of $\delta G_{T,j}^{l}$. Since quantization errors coming from rounding to reduced fixed-point precision are not random, DNNs trained in this way are not a priori expected to be suitable for deployment on analog in-memory computing hardware. Our experiments presented in Section IV have verified this assertion for ResNet-32. Techniques that inject random Gaussian noise during training are a much more natural fit to make the network robust to errors from analog in-memory computing hardware. As early as in 1994, it was shown that injecting noise on the synaptic weights during training enhances the tolerance to weight perturbations of multi-layer perceptrons, and the application of this technique to analog neural hardware was discussed[23]. Recent works have also proposed to apply noise to the synaptic weights, layer inputs, or pre-activations using hardware-specific noise models in order to improve the network tolerance to hardware noise[22,24]. However, to the best of our knowledge these techniques were not tested on the state-of-the-art deep ResNet architectures commonly used today for image classification problems, and no experimental validation of their effectiveness on analog in-memory computing hardware has been shown. In this work, we follow the original approach of Murray et al.[13] of injecting Gaussian noise to the synaptic weights during training. Next, we discuss different techniques that we employed together with synaptic weight noise in order to improve the accuracy of erroneous in-
ference on ResNet-32 and achieve baseline performance after transferring the weights to PCM hardware.

III. TRAINING PROCEDURE

A. Methodology

When performing inference with analog in-memory computing hardware, the DNN experiences errors primarily due to (i) inaccurate programming of the network weights onto the devices (write noise) and (ii) temporal fluctuations of the hardware weights (read noise). We can cast the effect of these errors into a single error term $\delta G_{ij}$ that distorts each synaptic weight when performing forward propagation during inference. Hence, we propose to add noise that corresponds to the error induced by $\delta G_{ij}$ to the synaptic weights that are used for computing the convolutions in the forward pass during training. The backward pass and weight updates are performed with weights that did not experience this noise. We found that adding noise to the weights only in the forward propagation is sufficient to achieve close to baseline accuracy for a noise magnitude comparable to that of our hardware, and adding noise during the backward propagation did not improve the results further. For simplicity, we assume that $\delta G_{ij}$ is Gaussian distributed, which is usually the case for analog memristive hardware. Weights are linearly mapped to the entire conductance range $G_{\text{max}}$ of the hardware, hence the standard deviation $\sigma_{\text{Wf}}^l$ of the Gaussian noise on weights to be applied during training, for a layer $l$, can be computed as

$$\sigma_{\text{Wf}}^l \equiv \eta_{tr} = \frac{\sigma_{\delta G}}{G_{\text{max}}},$$

where $\sigma_{\delta G}$ is a representative standard deviation of combined read and write noise measured from hardware. During training, the weight distribution of every layer and hence $W_{\text{max}}^l$ changes, therefore $\sigma_{\text{Wf}}^l$ is recomputed after every weight update so that $\eta_{tr}$ stays constant throughout training. We found this to be especially important in achieving good training convergence with this method.

Weight initialization can have a significant effect on DNN training. Two different weight initializations can lead to completely different minima when optimizing the network objective function. The network optimum when training with additive Gaussian noise could be closer to the FP32 training optimum than to a completely random initialization. So it can be beneficial to initialize weights from baseline converged network and then retrain this network by injecting noise. McKinstry et al. reported a similar observation for training with reduced digital precision. For achieving high classification accuracy in our experiments, we found this strategy more helpful in general than random initialization.

Injecting noise on weights during training affects the activation distributions and hence weight updates. Therefore, during training, the weight distribution of a layer could grow uncontrollably. Controlling the weight distribution in a desirable range can improve the network training convergence and makes the mapping of weights to hardware with limited conductance range easier. We therefore clip the synaptic weights at layer $l$ after every weight update in the range $[-\alpha \times \sigma_{\text{Wf}}^l, \alpha \times \sigma_{\text{Wf}}^l]$, where $\sigma_{\text{Wf}}^l$ is the standard deviation of weights in layer $l$ and $\alpha$ is a tunable hyper-parameter. In our studies, $\alpha = 2.0$ worked the best for the ResNet-32 network.

DNN convergence accuracy, in general, is sensitive to the learning rate used during training. Since we use weight initialization from weights of the baseline converged network, using the same learning rate scheduling as that of baseline network does not guarantee convergence to baseline comparable accuracy. To choose proper learning rate scheduling for ResNet-32 network, we compute a single inference on baseline converged network by injecting noise and we monitor the resulting inference accuracy. We take note of the learning rate evolution starting from this accuracy in the baseline network training curve until convergence and we use the same learning rate evolution while retraining the network by injecting Gaussian noise.

B. Results

We performed simulations to characterize the inference performance of ResNet-32 after training incorporating the injection of Gaussian noise in conjunction with the techniques presented above. We computed the classification accuracy on the test dataset for different amounts of injected noise $\eta_{tr}$ during training. We also show how the test accuracy is affected when perturbing the inference weights by a certain amount of relative noise $\eta_{inf} \equiv \frac{\sigma_{\text{Wf}}^l}{W_{\text{max}}^l}$, where $\sigma_{\text{Wf}}^l$ is the standard deviation of the noise injected to the weights of layer $l$ before performing inference on the test dataset.

The training is performed using stochastic gradient descent with a momentum of 0.9. The network objective is categorical cross entropy function over 10 classes of the input image. Learning rate scheduling is performed to reduce learning rate by 90% at every training epoch number that is an integer multiple of 50. The initial learning rate for the baseline network is 0.1 and training converges in 200 epochs with a batch size of 128. Weights of all convection and fully connected layers of the baseline network are initialized using He Normal initialization. The baseline network is retrained by injecting Gaussian noise for up to 150 epochs. We preprocess the training images by randomly cropping a 32 $\times$ 32 patch after padding 2 pixels along the height and width of the image. We also apply a random horizontal flip on the images from the train set. Additionally, we apply cutout on the training set images. For both training and test set, we apply channel wise normalization for 0 mean and unit standard deviation.

The test accuracy obtained after training without inducing any perturbation during inference ($\eta_{inf} = 0$) is plotted in Fig. 2a for different amounts of noise injected during training. It can be seen that the training algorithm is able to achieve a test accuracy close to the software baseline of 93.87% with up to approximately $\eta_{tr} = 8\%$. When $\eta_{tr} > 8\%$, the training convergence starts to become affected by the high noise and it is
not possible anymore to reach the software baseline within the same number of epochs. The tolerance of the networks trained with different amounts of $\eta_{tr}$ to weight perturbations during inference, $\eta_{inf}$, is shown in Fig. 2. For a given value of $\eta_{inf}$, it can be seen that in general, the highest test accuracy can be obtained for the network that has been trained with a comparable amount of synaptic weight noise, i.e. for $\eta_{tr} \approx \eta_{inf}$. In most cases, $\eta_{tr}$ can be increased above $\eta_{inf}$ up to a certain point and still lead to comparable or slightly higher (within $\approx 0.1\%$) test accuracy than for $\eta_{tr} = \eta_{inf}$. However, when $\eta_{tr}$ becomes much higher than $\eta_{inf}$, the test accuracy inevitably decreases due to the inability of the network to achieve baseline accuracy after training when $\eta_{tr}$ is too high. The test accuracy for $\eta_{tr} = \eta_{inf}$ is shown in Fig. 2. It can be seen that for up to $\eta_{inf} = 5\%$, an accuracy within $0.5\%$ of the software baseline is achievable.

IV. EXPERIMENTAL RESULTS

In order to experimentally validate the effectiveness of the above training methodology, we performed experiments on a prototype multi-level PCM chip comprising of 1 million PCM devices fabricated in 90 nm CMOS baseline technology. PCM is a memristive technology which records data in a nanometric volume of phase-change material sandwiched between two electrodes. The phase-change material is in the low-resistive crystalline phase in an as-fabricated device. By applying a current pulse of sufficient amplitude (typically referred to as the RESET pulse) an amorphous region around the narrow bottom electrode is created via melt-quench process. The device will be in a low conductance state if the high-resistive amorphous region blocks the current path between the two electrodes. The size of the amorphous region can be modulated in an almost completely analog manner by the application of suitable electrical pulses. Hence, a continuum of conductance values can be programmed in a single PCM device over a range of more than two orders of magnitude.

A given conductance value can be programmed in a PCM device via iterative programming. The devices are initialized to a high-conductance state via a staircase-pulse sequence. The sequence starts with a RESET pulse of amplitude 450 μA and width 50 ns, followed by 6 pulses of amplitude decreasing regularly from 160 μA to 60 μA and with a constant width of 1000 ns. After initialization, each device is set to a desired conductance value through a program-and-verify scheme. The device conductance is read 5 times consecutively, and the mean conductance of these reads is used for verification. If the mean conductance does not fall within 0.25 μs from the target conductance, the device receives a programming pulse where the pulse amplitude is incremented or decremented proportionally to the difference between the mean and target conductance. The pulse amplitude ranges between 80 μA and 400 μA. This program-and-verify scheme is repeated for a maximum of 55 iterations.
A. Weight transfer to PCM-based synapses

The experimental cumulative distributions of conductance values for 13 representative programmed levels measured approximately 25 seconds after programming are shown in Fig. 3a. The standard deviation of these distributions is extracted and fitted with a polynomial function of the target conductance (dashed lines in Fig. 3a) as shown in Fig. 3b. This fitted curve is used to simulate weight transfer to PCM synapses according to Eq. 4. $\Delta G_{T,j}$ is modeled as a Gaussian distributed random variable with $\mu$ mean and standard deviation given by the fitted curve depending on the corresponding value of $|G_{T,j}|$, computed with $G_{\text{max}} = 25 \mu S$.

The resulting test accuracies obtained after software training and after weight transfer to PCM synapses are shown in Fig. 3c for different training procedures. It can be seen that standard FP32 training without constraints performs the worst after transfer to PCM synapses. Training with 4-bit precision weights (using the method described in Ref. [37]), which is roughly the effective precision of our PCM devices, improves the performance after transfer with respect to FP32, but nevertheless the accuracy decreases by more than 1% after transferring the 4-bit weights to PCM. Training ternary digital weights leads to a lower performance drop ($< 0.5\%$) when transferring weights to PCM, although we were not able to reach the FP32 software baseline with ternary weights on this network. Therefore the accuracy after transfer is worse than for the 4-bit weights. When performing training by injecting Gaussian noise as described in Section IV with $\mu_{\sigma} = 3.8\%$, corresponding to $\sigma_{G_0} = 0.94 \mu S$ (median of the 13 values reported in Fig. 3b), the best overall performance after transfer to PCM is obtained. The resulting accuracy of 93.7% is less than 0.2% away from the FP32 baseline. The accuracy obtained without perturbing the weights after training by injecting Gaussian noise is slightly higher than the FP32 baseline, which could be attributed to improved generalization resulting from the additive noise training as commonly reported in prior works.

B. Inference experiment and temporal evolution of test accuracy

Although we could achieve good test accuracy after weight transfer to PCM synapses as shown above, an important challenge for any analog in-memory computing hardware is to be able to retain this accuracy over time. This is especially true for PCM due to the high $1/f$ noise experienced in these devices as well as temporal conductance drift. The conductance values in PCM drift over time $t$ according to the relation $G(t) = G(t_0)(t/t_0)^{-\nu}$, where $G(t_0)$ is the conductance measured at time $t_0$ from programming and $\nu$ is the drift exponent, which depends on the device, phase-change material, and phase configuration of the PCM ($\nu$ is higher for the amorphous than the crystalline phase$^{[23]}$). In our PCM devices, $\nu \approx 0.05$ on average. Therefore, it is essential to measure experimentally how the test accuracy during inference with PCM evolves over time.

Here, we present experiments where all 361,722 synaptic weights of ResNet-32 were programmed individually on two PCM devices of the chip, according to Eq. 1 and 4. Depending on the sign of $G_{T,j}$, either $G_{T,j}^+$ or $G_{T,j}^-$ is iteratively programmed to $|G_{T,j}|$, and the other device is RESET close to 0 $\mu S$ with a single pulse of 450 $\mu A$ amplitude and 50 ns width. The iterative programming algorithm converged on 99.1% of the devices programmed to nonzero conductance, and no screening for defective devices on the chip was performed prior to the experiments. The scatter plot of the PCM weights measured approximately 25 seconds after program-
FIG. 4. a, Scatter plot of weights programmed in the PCM chip versus target weights obtained after training. b, Measured test accuracy over time from the weights of the PCM chip. A global drift compensation procedure is performed for every layer before every inference. A hardware model incorporating PCM conductance drift ($\nu = 0.06$), device-to-device drift exponent variability with $0.1\nu$ standard deviation, and instantaneous Gaussian read noise with $0.6\mu\text{s}$ standard deviation is able to capture the experimental results fairly well. c, Weight evolution from the PCM chip with and without applying the scaling factor obtained from the global drift compensation to the weights. The scaled weights distribution stays much closer to the target weights than the unscaled one.

V. CONCLUSION

In this work, we introduced a methodology for training ResNet-type CNNs in order to make them suitable for deployment on analog in-memory computing hardware. We proposed to inject noise to the synaptic weights which is proportional to the combined read and write conductance noise of the hardware during the forward pass of training. This approach...
combined with judicious weight initialization, clipping, and learning rate scheduling, allowed us to train ResNet-32 on CIFAR-10 with more than 5% weight noise while achieving within 0.5% of the 93.87% FP32 baseline test accuracy during erroneous inference. We obtained a test accuracy of 93.69% on the CIFAR-10 dataset after programming the trained weights to analog PCM hardware on 722,544 PCM devices. The accuracy stayed above 92.6% when periodically measured over a period of 1 day, which is to the best of our knowledge the highest accuracy experimentally reported to-date on the CIFAR-10 dataset by any analog in-memory computing hardware. A global scaling procedure was used compensate for the conductance drift of the PCM devices, which was found to be critical in improving the accuracy retention. More advanced drift compensation schemes have been developed and could improve the accuracy retention further, which will be presented in the next versions of this paper. We also hope to show the effectiveness of this method on other networks and datasets.

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