Smart On-Chip Electromagnetic Environment

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We introduce the concept of smart radio environments, currently extensively studied for wireless communication in metasurface-programmable meter-scaled environments (e.g., inside rooms), on the chip scale. Wired intra-chip communication for information exchange between cores increasingly becomes a computation-speed bottleneck for modern multi-core chips. Wireless intra-chip links with millimeter waves are a candidate technology to address this challenge, but they currently face their own problems: the on-chip propagation environment can be highly reverberant due to the metallic chip enclosure but transceiver modules must be kept simple (on/off keying) such that long channel impulse responses (CIRs) slow down the communication rate. Here, we overcome this problem by endowing the on-chip propagation environment with in situ programmability, allowing us to shape the CIR at will, and to impose, for instance, a pulse-like CIR despite the strong multipath environment.

Using full-wave simulations, we design a programmable metasurface suitable for integration in the on-chip environment (“on-chip reconfigurable intelligent surface”), and we demonstrate that the spatial control offered by the metasurface allows us to shape the CIR profile.

We envision (i) dynamic multi-channel CIR shaping adapted to on-chip traffic patterns, (ii) analog wave-based over-the-air computing inside the chip enclosure, and (iii) the application of the explored concepts to off-chip communication inside racks, inside the chassis of personal computers, etc.

I. INTRODUCTION

Wireless millimeter-wave (mmW) communication between processors on multi-core chips is a potential solution to avoid that inter-core information exchange soon becomes a computation speed bottleneck [1–4]. Yet, such a wireless network on chip (WNoC) is confronted with its own challenges: either the received signals are too weak, or severe multipath curbs the information transfer rate [5]. In this Letter, we overcome this dilemma by endowing the on-chip electromagnetic (EM) propagation environment with programmability. To that end, we integrate a programmable metasurface [6–8], also referred to as reconfigurable intelligent surface (RIS), in the chip package – analogous to current RIS-based efforts at the indoor scale [9,11]. We demonstrate in a numerical study that the on-chip RIS can be configured such that a high-SNR high-multipath channel impulse response (CIR) becomes pulse-like, enabling high-capacity information transfer in WNoCs with simple modulation schemes.

Traditionally, wireless communication is optimized in terms of transceiver hardware and pre-/post-processing of the signals but the propagation medium is considered fixed. Recently, the emergence of programmable metasurfaces – ultrathin arrays of elements with individually reconfigurable scattering response – has led to a paradigm shift: “smart” programmable wireless propagation environments [9]. Broadly speaking, RIS can be leveraged either to encode information into wireless signals, or to shape wireless channels [12]. The role of RIS largely depends on the amount of scattering in the environment. In free space, RIS, in combination with carefully aligned emitters, can replace costly phased-array antennas for beam-forming [8,13–15]. In quasi-free space with blocked line-of-sight, RIS can serve as alternative relaying mechanism [16–20]. In rich scattering environments, RIS can create spatial monochromatic hotspots [21,22], shape the multipath CIR [11,23], or optimize the MIMO channel matrix [24]. There are also cases of backscatter communication in which the RIS encodes information by shaping wireless channels [25,26]. To date, all of these ideas are explored for meter-scaled environments, such as office rooms.

Two to three orders of magnitude smaller are on-chip wireless environments. The reason to consider a partial [27] replacement of conventional wired interconnects with WNoCs are scalability limits: more and more processing cores are crammed onto modern chips but wired interconnects must be kept short due to Ohmic losses and wire delays, leading to more and more inter-router hops. Consequently, both latency and power consumption of communication between far-apart cores deteriorate, the latency reaching up to several tens of nanoseconds [28]. WNoCs avoid inter-router hops and can build on mature mmW technology. However, on-chip antennas and radio transceivers [29,30] are subject to size and power constraints; in particular, their processing power is limited such that WNoCs typically rely on simple modulation schemes (e.g., on/off keying, OOK). Thus, intersymbol interference (ISI) must be avoided at the cost of lower data transmission rates when the CIR is lengthy...
FIG. 1. Schematic drawing of the smart EM on-chip environment. An on-chip RIS (25 programmable meta-pixels) is integrated into the chip package ceiling. The inset shows the meta-pixel without the surrounding metallic walls.

due to multipath. From the EM wave’s perspective, a typical on-chip environment constitutes a metallic enclosure (solder bumps on the bottom, metallic package on sides and top) – a “micro reverberation chamber” [37]. While this enclosure seals the EM on-chip environment from the outside, making it extraordinarily static and predictable, it also means that waves will heavily reverberate unless they are strongly attenuated (e.g., by a thick silicon layer). But strong attenuation implies poor received-signal-strength-indicators (RSSIs), yielding the on-chip RSSI-ISI dilemma. Trade-offs between the two effects can be found [38], but ideally one would have high-RSSI channels with pulse-like CIRs despite strong multipath. In our Letter, we demonstrate that this goal is potentially attainable if the CIR can be shaped with an on-chip RIS.

II. ON-CHIP RSSI-ISI DILEMMA

To start, we analyze the impact of the silicon layer’s thickness on RSSI and ISI in the simplified model shown in Fig. 1 and detailed in Refs. [38, 39]. In our simulations, the antennas acting as WNoC nodes are electrically small ports modeled as openings within the conductive solder bump layer. The detailed nature of the antennas is not crucial for the results we report because the propagation environment is irregular anyway (more on this below) and its amount of attenuation is strongly dominated by absorption rather than leakage through ports.

The silicon layer height has a strong impact on the scattering properties of the on-chip wireless environment. Example CIRs, and the associated spectra, are shown in Fig. 2. The on-chip RSSI-ISI dilemma is immediately obvious: for thick silicon layers (> 250 µm), the spectrum is essentially flat and the CIR is almost pulse-like (similar to quasi-free space) but the RSSI is very low. For thinner silicon layers, the RSSI can increase by almost 20 dB but the spectrum displays more and more dispersion, resulting in lengthy CIRs. The latter evidence substantial reverberation and rich scattering inside the chip enclosure and pose a severe ISI challenge for OOK. The CIR maximum does not even have to coincide with the first CIR peak, as seen for the light-blue CIR in Fig. 2. Indeed, the mean delay of the channel [40] for the considered transmitter-receiver pair is 0.56 ns for the 100 µm thick silicon layer and drops down to 0.14 ns for silicon layers thicker than 250 µm. This means that for the scenarios with thin silicon layer, the majority of the signal energy arrives not along the shortest path but after significant reverberation at a later time. Note that in the absence of a line-of-sight, the shortest path cannot be related to the antenna separation.

To further quantify the amount of rich scattering, we have evaluated the chip enclosure’s quality factor $Q = \frac{\pi f_0}{\mu}$, where $f_0$ is the center of the considered frequency band and $\mu$ is the exponential decay constant of the average of the CIR magnitude envelopes. For silicon heights of 100 µm, 150 µm and 200 µm we obtained $Q = 252$, $Q = 74$ and $Q = 56$, respectively. For thicker silicon layers, the CIR is pulse-like without any significant tail (the tail is known as “coda” or “sona” in wave physics) such that no meaningful quality factor can be determined.

III. ON-CHIP RIS DESIGN AND CHARACTERIZATION

To eliminate the on-chip RSSI-ISI dilemma, we integrate a RIS into the ceiling of the chip package, as seen in Fig. 1. The design of our programmable metasurface is based on well-known mushroom structures [41, 42] equipped with varactor diodes which individually alter
the effective capacitances of the metamaterial elements and shift their resonance frequencies. While the current RIS literature considers meter-scale applications that operate in air, our on-chip RIS must operate within an aluminium nitride layer whose high dielectric constant (∼8.8) might require small varactors with very large effective capacitances. To avoid this problem, we design the meta-atom with one side to be air/vacuum (in future implementation a low-dielectric-constant substrate). Interestingly, such a configuration is the opposite of usual RIS designs where the metamaterial element is implemented on a high-dielectric-constant substrate and operates within air. Further details on our RIS design were presented in Ref. [39]. Note, however, that our generic proposal of smart on-chip EM environments can also be realized with any other RIS design.

We first characterize the fundamental building block of our on-chip RIS in the conventional manner: we study the reflection under normal-incidence illumination of an infinite array of our programmable meta-atom – see Fig. 3(a). Magnitude and phase of the reflected wave display a targeted behavior in the targeted frequency range around 60 GHz, as seen in Fig. 3(b,c), and by changing the varactor’s capacitance from 0.1 pF to 1 pF, this resonance can be tuned. While such a characterization method may be meaningful for free-space applications of RIS, it gives a distorted and incomplete picture for RIS operation in rich scattering environments. In the latter, the wave energy is statistically equally distributed throughout the enclosure and waves with all possible angles of incidence and polarizations impinge on the RIS. Moreover, the conventional method does not account for coupling effects between neighbouring RIS elements. Indeed, we intend to deploy 2 × 2 groups of synchronized meta-atoms, each group controlled by a single bias voltage line; we refer to these groups as meta-pixels. The 2 × 2 configuration will reduce the resonance frequency because the loading from the infinite array is removed.

Overall, our on-chip RIS consists of an array of 5 × 5 such meta-pixels, as seen in Fig. 1. For simplicity we limit ourselves to 1-bit (binary) programmable meta-pixels in the following (0.1 pF or 1 pF).

To better understand the true potential for wave field manipulation with our on-chip RIS, we perform a second characterization in situ. Specifically, we measure within the targeted on-chip environment shown in Fig. 1 the transmission $S_{12}$ between various pairs of antennas, each time for 32 random RIS configurations. The standard deviation of these measurements across different configurations is a reliable metric of the ability of the RIS to manipulate the field in the considered setting [11, 21]. The ability of our RIS to modulate frequencies across the entire considered 55 – 65 GHz band is now evident in Fig. 3(d) – in disaccord with the first conventional characterization method.

We note that the presence of the on-chip RIS elements notably decreases the reverberation time of the on-chip enclosure because the on-chip RIS partially absorbs the waves that are impinging upon it. Indeed, we find that for a 100 μm thick silicon layer the enclosure’s quality factor drops from $Q = 252$ to $Q = 140$. Correspondingly, $|S_{12}|$ drops from −41 dB to −51 dB. This remains nonetheless the rich scattering regime, clearly exceeding, for instance, the reverberation ($Q = 74$) in a scenario with 150 μm thick silicon layer without RIS.

IV. ON-CHIP CIR SHAPING

We now proceed with optimizing the on-chip RIS configuration to achieve the desired CIR shaping, namely a pulse-like CIR despite rich scattering. To converge toward a pulse-like CIR, we examine both the strength of the dominant CIR peak as well as the ratio between the secondary peaks and the dominant peak. This combination of metrics is important to achieve a pulse-like CIR without compromising on the signal power received for the dominant peak. Since there is – unlike in free space – no forward model mapping RIS configuration to scattering response (the CIR) for our setting, we cannot deploy analytical tools to identify a suitable RIS configuration. Instead, we resort to an iterative trial-and-error optimization technique, as did previous work on CIR shaping with RIS in rich scattering indoor environments [23]. To expedite the search within the huge search space (225 possible RIS configurations), we deter-
mine a reasonably good initial guess: the best out of 32 random RIS configurations. Then, we flip the state of one meta-pixel at a time, and keep the change of its state if the CIR has become more pulse-like according to our criteria. Note that it is not sufficient to test each meta-pixel just once because the presence of reverberation inside the chip enclosure correlates the optimal states of different meta-pixels [23].

![Figure 4](image_url)

**FIG. 4.** CIR optimization with on-chip RIS. (a) CIR intensity profiles for 32 random on-chip RIS configurations (color-coded), and the average CIR (black). (b) Best out of the 32 random configurations. (c) Optimum after one optimization loop. (d) Optimum after two optimization loops. The insets indicate the corresponding RIS configuration and antenna locations.

An example of this protocol for on-chip CIR shaping is displayed in Fig. 4 for the case of a 100 µm thick silicon layer and 5 mm distance between transmitter and receiver (see inset for their exact locations). Our optimization progressively flattens the CIR behind the first peak, such that the modulation rate for OOK-based data transmission between the ports can be increased substantially. It is also apparent that for the optimized configurations roughly half of the RIS elements are in one and the other half in the other one of the two possible states, without any intuitively understandable pattern. This is expected in a rich scattering system and in contrast to the (analytically calculated) RIS patterns used for beam-forming in free space [8].

To illustrate the generality of our technique, as well as its real-time *in situ* adaptability to dynamic traffic patterns [44], we apply it also to two other pairs of antenna locations on a chip with 100 µm thick silicon layer as well as to one case on a chip with 200 µm thick silicon layer. The effectiveness of our technique is clearly seen for all three cases in Fig. 5. In the first case, the iterative optimisation does not yield any improvement upon the ensemble optimum. In the third case with 200 µm thick silicon layer, the CIR is, of course, shorter but our technique is effective nonetheless in improving the CIR profile toward a pulse-like shape for OOK purposes. Overall, these three further examples confirm that depending on traffic needs on the chip, the CIR of a selected antenna pair can be shaped to be pulse-like, irrespective of antenna separation and silicon layer thickness.

![Figure 5](image_url)

**FIG. 5.** Further examples of CIR shaping for different Tx-Rx separations and silicon layer thickness – see insets in (a,c,e). CIR intensity profiles for 32 random realizations (a,c,e) as well as the ensemble average (black), ensemble optimum (red) and iteration optimum (blue) are shown (b,d,f).

### V. CONCLUSIONS AND OUTLOOK

To summarize, we demonstrated that the integration of a RIS into an on-chip wireless environment can endow the latter with programmability, enabling pulse-like CIRs despite rich scattering and high RSSI. Pulse-like CIRs enable faster data transmission rates in OOK. Smart on-chip EM environments are sealed and extraordinarily static such that suitable RIS configurations for various traffic patterns can be identified in a one-off calibration phase, in contrast to the meter-scaled smart indoor environments that dynamically evolve due to the motion of inhabitants, etc.

The ability of the RIS to shape the CIR depends on several factors and can hence be improved accordingly. The most important question is, how many of the rays that connect the transmitter to the receiver have encountered the RIS? The percentage of rays manipulated by the RIS can be increased by (i) using more RIS elements, (ii) placing the RIS elements closer to the transceivers, and/or (iii) operating in an environment with more reverberation. Moreover, the design of the RIS elements can be optimized further, and linear instead of binary control would also enhance the performance. Assuming that the field inside the chip enclosure is approximately chaotic,
which is a reasonably assumption when the silicon layer is thin, means that all polarizations are well mixed and the restriction of our meta-atom to engage mainly with one polarization is not problematic, as evidenced by our results; nonetheless, by alternating the varactors on the meta-atoms constituting the meta-pixels as in Ref. [42], or using multiple varactors on each of them, modifications of our on-chip RIS design that engage with both field polarizations can be conceived. Finally, optimization algorithms that search the huge optimization space more efficiently can be deployed.

Looking forward, the flexibility of smart on-chip EM environments should be leveraged to optimize communication-specific metrics such as channel capacity or bit-error-rate. Such studies offer the opportunity to tailor the RIS configuration to highly application-specific parameters, including the specific antennas and radio transceivers (and hence the associated SNR), the specific modulation scheme, etc. Furthermore, more complex communication scenarios such as communication from one transmitting to multiple receiving nodes (SIMO) deserve attention [24]. Ultimately, experimental validation of all these ideas will be indispensable in the future.

A further avenue for future exploration is to consider similar problems of data exchange at intermediate scales between the chip scale and the indoor scale. Relevant examples include communication inside racks or blades, inside the chassis of personal computers, or inside data centers [45] [46].

Finally, we note that in the future the smart on-chip EM environment that we propose can be endowed with a second functionality related to wave-based analog signal-processing by bringing recent proposals of wave processing in (programmable) scattering enclosures for matrix multiplication [47], signal differentiation [48], or reservoir computing [49] to the chip scale. Such analog “over-the-air” computing holds the promise to be faster and more energy efficient than its electronic digital counterpart for specific computational operations, paving the way to hybrid analog-digital processing chips.

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