BurstLink: Techniques for Energy-Efficient Conventional and Virtual Reality Video Display

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ABSTRACT

Conventional planar video streaming is the most popular application in mobile systems, and the rapid growth of 360° video content and virtual reality (VR) devices are accelerating the adoption of VR video streaming. Unfortunately, video streaming consumes significant system energy due to high power consumption of the system components (e.g., DRAM, display interfaces, and display panel) involved in this process.

We propose BurstLink, a novel system-level technique that improves the energy efficiency of planar and VR video streaming. BurstLink is based on two key ideas. First, BurstLink directly transfers a decoded video frame from the host system (i.e., the video decoder or GPU) to the display panel, bypassing the host DRAM. To this end, we extend the display panel with a double remote frame buffer (DRFB), instead of the DRAM’s double frame buffer, so that the system can directly update the DRFB with a new frame while updating the panel’s pixels with the current frame stored in the DRFB. Second, BurstLink transfers a complete decoded frame to the display panel in a single burst, using the maximum bandwidth of modern display interfaces. Unlike conventional systems where the frame transfer rate is limited by the pixel-update throughput of the display panel, BurstLink can always take full advantage of the high bandwidth of modern display interfaces by decoupling the frame transfer from the pixel update as enabled by the DRFB. This direct and burst frame transfer of BurstLink significantly reduces energy consumption in video display by 1) reducing accesses to the host DRAM, 2) increasing the system’s residency at idle power states, and 3) enabling temporal power gating of several system components after quickly transferring each frame into the DRFB.

BurstLink can be easily implemented in modern mobile systems with minimal changes to the video display pipeline. We evaluate BurstLink using an analytical power model that we rigorously validate on a real modern mobile system. Our evaluation shows that BurstLink reduces system energy consumption for 4K planar and VR video streaming by 41% and 33%, respectively, and provides an even higher reduction as display resolution and/or display refresh rate increases.

1. INTRODUCTION

Conventional planar video streaming is the most prevalent application in mobile devices [19], and virtual-reality (VR) video streaming is emerging as one of the most important applications in the entertainment market. Cisco predicts that video streaming will generate more than 79% of mobile data traffic by 2022 [23], and Goldman Sachs predicts that around 79-million users will use VR video streaming by 2025 [41]. To provide users with an immersive experience, video formats and mobile display panels support increasingly high resolutions (e.g., 4K [6,82]) and refresh rates (e.g., 120Hz [83]). These trends come at the cost of significantly higher energy consumption of video display, which negatively impacts battery life of the mobile device [91]. Therefore, mobile systems need an efficient planar/VR video display architecture that provides high energy efficiency while enabling high video/display resolutions and refresh rates.

In conventional mobile systems, the majority of planar video streaming energy is consumed by DRAM main memory and the display panel. Figure 1 shows the energy consumption that we measure from a real Intel Skylake mobile system while streaming 30 frames-per-second (FPS) videos with full-high-definition (FHD, 1920×1080), quad-high-definition (QHD, 2560×1440), and 4K (3840×2160) resolutions.1 We break down the system energy consumption into three major components: Display, DRAM (main memory), and Others, which includes the processor, network (WiFi), and storage (eMMC). As the size of a single decoded video frame becomes as large as tens of megabytes for a high-resolution video (e.g., 24MB for a 4K video), the data movement to/from DRAM alone contributes more than 30% of the total system energy consumption. State-of-the-art VR streaming schemes [61,108], which significantly reduce the energy for computation compared to traditional schemes [33,40], show similar trends in the energy consumption breakdown.

Figure 1: Energy consumption of a modern mobile system while streaming videos at various resolutions.

In this paper, we find two inefficiencies of conventional video display schemes that result in the underutilization of advanced architectural features widely available in modern mobile systems. First, modern mobile systems commonly employ a remote frame buffer inside the display panel to improve energy efficiency in static-image display (see Section 2.3 for

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1Recent works also show similar trends on ARM system-on-chips (SoCs) [69,103].
more details) and the video decoder or GPU stores every decoded frame into the host DRAM before sending the frame to the display panel. This is because, when other frames (e.g., graphical user interface (GUI) and cursor planes) must also be displayed, the display controller must first merge them with the video plane to generate a single frame that is sent to the display panel. However, when only the video plane is being updated (which is common in video streaming), decoded video frames do not need to be merged with other frames and can be directly sent to the display panel’s remote frame buffer, bypassing the host DRAM. This would significantly reduce unnecessary data movement and thus improve energy efficiency.

Second, conventional video processing and display schemes underutilize the high bandwidth provided by modern display interfaces. To cope with high-quality videos with high resolutions and frame rates, the state-of-the-art embedded-DisplayPort (eDP) interface supports a peak bandwidth of 25.92Gbps [96]. However, even in the case of displaying a 4K 60FPS video, conventional mobile systems send each frame at a transfer rate of about 12Gbps. This is because, the frame transfer rate between the host system to the display panel is dictated by the display panel’s pixel-update bandwidth. The eDP-bandwidth underutilization negatively affects the energy efficiency since a longer time spent in actively transferring frames, reduces the time that the system can spend in low-power states. This inefficiency is expected to remain for the coming years, considering a huge quality gap between displays and video contents [29, 42, 89]; while modern displays increasingly support higher resolutions and refresh rates, a significant majority of video streaming content is still in high definition (HD) or standard definition (SD) resolution [29, 89]. For example, a recent study [29] reports that 4K TVs account for about 55% of the TV market, while only less than 10% of video content provided by major streaming platforms (e.g., Netflix, Amazon Prime Video, and YouTube) are in 4K resolution with frame rates higher than 30FPS.

Based on our observations, we propose BurstLink, a new system-level technique that improves the energy efficiency of planar and VR video streaming by exploiting the advanced architectural features that are widely available yet underutilized in modern mobile systems. BurstLink is based on two key ideas. First, BurstLink implements Frame Buffer Bypassing, a novel mechanism that enables directly transferring a decoded video frame from the host system to the display panel’s remote frame buffer (bypassing the host DRAM). In order to allow the system to transfer a new frame while the display panel updates pixels with the current frame in the remote frame buffer, we extend the display panel with a double remote frame buffer (DRFB). Second, BurstLink implements Frame Bursting, a novel mechanism that enables transferring a whole decoded frame to the display panel in a single burst using the maximum bandwidth of modern display interfaces. Unlike conventional systems where the frame transfer rate is limited by the pixel-update throughput of the display panel, BurstLink can always take full advantage of the high bandwidth of modern display interfaces by decoupling the frame transfer from the pixel update using the DRFB.

The direct and bulk frame transfer enables BurstLink to significantly reduce energy consumption over a conventional video display scheme in two ways. First, by directly transferring processed video frames from the video decoder or GPU to the display panel without buffering them into the host DRAM, BurstLink saves a significant fraction of the DRAM energy consumption. Second, by transferring an entire frame at the maximum bandwidth, BurstLink reduces the utilization of the processor and the display subsystem, since they are active only during the burst period, thereby allowing the system to enter deep low-power states more frequently by turning off unused resources (e.g., the display controller, display interface, and host DRAM). In addition to planar/VR video display, Frame Bursting is also applicable for other important mobile workloads like casual gaming and office productivity [5, 13].

We evaluate BurstLink using an analytical power model that we rigorously validate with a real modern mobile system.² Our evaluation shows that BurstLink reduces system energy consumption for 4K 60FPS planar and 360° VR video streaming by 41% and 33%, respectively, and provides an even higher reduction as display resolution and/or display refresh rate increases. BurstLink also reduces system energy consumption for video conferencing, MobileMark [13], and casual gaming [5] workloads by 30%, 28%, and 27%, respectively.

We make the following key contributions in this work:

- We provide the first study that identifies the main energy inefficiencies in traditional video display schemes of mobile systems and proposes novel techniques in both the processor and display panel to address the inefficiencies.
- We propose BurstLink, which significantly improves the energy efficiency of video display in mobile systems. BurstLink introduces two new techniques: 1) Frame Buffer Bypass, which transfers a decoded video frame directly to the panel’s DRFB without buffering it in the host DRAM, and 2) Frame Bursting, which exploits the DRFB and the maximum bandwidth of the modern display interface to burst transfer each decoded frame to the display panel as quickly as possible and increase opportunities for system idleness.
- We evaluate BurstLink using a thoroughly-validated analytical power model. Our evaluation shows that BurstLink reduces system energy consumption for 4K 60FPS planar and VR video streaming by 41% and 33%, respectively. BurstLink’s energy reduction increases with higher display resolutions, which makes BurstLink an even better fit for next-generation high-resolution displays. BurstLink can be implemented in modern mobile systems with minimal changes to the video display hardware and software.

2We will make the analytical power model publicly available.

2. BACKGROUND

We provide a brief background on relevant aspects of video display in modern mobile systems. First, we review the overall micro-architecture of a common mobile system-on-chip (SoC). Second, we discuss the various idle power states of the system (C-states). Third, we provide a primer on the display panel refresh and the new panel self refresh (PSR) technology. Fourth, we describe the processes responsible for decoding and displaying videos. Finally, we explain system
power state transitions that occur during video processing.

2.1 Mobile SoC Micro-architecture

The micro-architecture of a mobile SoC typically consists of the following components.

**SoC Main Domains.** A high-end mobile processor (e.g., Intel Skylake [26], AMD Kabini [17], and Samsung Exynos [54]) is commonly implemented as a SoC that integrates three main domains into a single chip: 1) compute domain, such as CPU cores and graphics engines, 2) IO domain, which includes several intellectual properties (IPs) sharing the IO interconnect (e.g., display controller (DC), image signal processing engine (ISP), video decoders (VDs), and video encoders (VEs)), and 3) memory domain, which includes the memory controller and DRAM interface.

**IO Interconnect.** IO interconnects, such as Intel On-chip System Fabric (IOSF) [57] and ARM Advanced Microcontroller Bus Architecture (AMBA) [11, 71], are on-chip communication technologies that allow multiple IPs to 1) perform peer-to-peer (P2P) communication and 2) access main memory (DRAM) using direct memory access (DMA).

**P2P and DMA Engines.** IO IPs are typically equipped with DMA and P2P engines [55]. The DMA engine enables the IP to directly access main memory, while the P2P engine enables direct communication between two IPs without copying the data to main memory. P2P reduces the data transmission delay and increases the available system bandwidth. The DMA and P2P engines each have control registers (CRs) that are configured by the IP driver, which runs on a CPU core. The CRs specify the source/destination/direction of the data transfer (i.e., reading/writing from/to the peer IP or DRAM), the transfer unit size, and/or the number of bytes to transfer in one burst. When the DMA engine completes a transaction, it sends an interrupt to the CPU core in order to wake up the IP driver that initiated the transaction.

**Application as an Orchestrator.** Most mobile applications follow a sequence of steps that use multiple SoC IPs. In today’s software and hardware architectures, an application (which runs on a CPU core) orchestrates each step and interaction with the IPs (e.g., VD, DC, NIC) [61, 69, 105]. The application interacts with and issues tasks to an IP driver using an application programming interface (API), which serves as an abstraction layer for the hardware. The IP driver configures its IP based on the task issued by the application (e.g., configure DMA engines to move encoded frames from the host DRAM into the VD). When the IP completes its task, it sends an interrupt to the IP driver. The IP driver notifies the application (via the API), which enables the application to continue its flow. The software/hardware abstraction has two major advantages. First, it allows application developers to use a unified interface (i.e., API) regardless of the IP's hardware implementation. Second, it increases program portability to multiple devices and SoC architectures.

**Traditional Display Subsystem.** Figure 2 shows an overview of a conventional display subsystem, which consists of five main components: two on the processor side (i.e., the Video Decoder (VD) and Display Controller (DC)) and three on the display panel side (i.e., the eDP Receiver, Pixel Formatter (PF), and Remote Frame Buffer (RFB)) inside the timing-controller (T-con)\(^3\). We next explain video processing steps in more detail.

![Figure 2: Overview of a conventional display subsystem.](image)

2.2 System Idle Power States (C-states)

The Advanced Configuration and Power Interface (ACPI\(^4\)) defines a processor’s idle power states, commonly called C-states [93]. C-states are defined in two main levels: 1) the component level, such as thread (TCi), core (CCi), and graphics (RCi) C-states, and 2) the SoC level, known as package C-states (PCI or Ci) [35, 45].

A package C-state defines an idle power state of the SoC (consisting of the processor, chipset, external memory devices, etc.). A system enters a specific package C-state depending on each system component’s idle power state (component C-state). Various levels of package C-states exist to provide a range of power consumption levels with various techniques such as clock gating at the core level or a nearly full shutdown of the system. The ACPI standard includes recommendations on the C-states, but manufacturers are free to define their own C-states and the SoC’s behavior at each C-state. In this work, we focus on the package C-states of the Intel Skylake architecture [45], but similar idle power state definitions exist in other architectures (e.g., AMD [2] and ARM [76]). Table 1 shows all package C-states of the Intel Skylake architecture and the conditions in which the power management unit (PMU) places the SoC into each package C-state (a similar table exists in the Intel manual [45]). Table 1 also shows the entry/exit latencies for each package C-state, which we measure on a real system (see Section 5 for more detail).

The system’s power level (in Watts) in each package C-state depends on the operating points (e.g., voltage and frequency) of the active components in the power state. For example, the power level at C0 state depends on how many cores or graphics engines are active and their operating voltages/frequencies. Similarly, the power level at C8 state depends on the display resolution that the DC and eDP are driving (the higher the resolution, the higher the DC clock frequency and voltage).

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\(^3\)A timing controller (T-con) is a circuit that processes and coordinates the coloration of the pixels in a display panel [84].

\(^4\)The ACPI is an industry standard that is widely used for OS-directed configuration, power management, and thermal management of computing systems.
2.3 Display Panel Refresh

Current display technologies require the host SoC to refresh the display panel several times of every second [63]. For example, a display panel with a refresh rate of 60Hz is refreshed 60 times per second. During each frame refresh window (i.e., 1/refresh_rate), the DC inside the host SoC transfers a full frame to the display panel by repeatedly performing three steps: the DC 1) fetches a portion of the image data from the DRAM frame buffer (in DRAM), 2) stores the fetched image data into the DC’s local buffer, and 3) sends the buffered data to the display panel via the display interface. The refresh process occurs regardless of the image type, i.e., static or dynamic. This means that even if the displayed image does not change over a long period of time (i.e., greater than a refresh window), the DC still refreshes the static image (i.e., repeatedly transfers the static image from the host DRAM to the display panel) several times of every second.

**Panel Self Refresh (PSR).** To reduce the system energy consumption when displaying static images, VESA (Video Electronics Standards Association [95]) introduced the Panel-Self-Refresh (PSR) standard [54, 56, 84]. The standard 1) adds a local frame buffer, called a remote frame buffer (RFB), into the panel T-con to store one frame, and 2) defines a protocol in which the DC notifies the display panel of an unchanged image. This enables panel self refresh (PSR) mode in which the panel performs self refresh using the static image stored in the RFB without accessing DRAM main memory. Doing so allows many host-side components including DRAM, display interface, and DC to be powered down, which significantly reduces the system energy consumption.

To enable PSR, the SoC must additionally implement a mechanism to detect unchanged frames. This implementation is SoC dependant and thus not included in the PSR standard. Existing mechanisms [39, 60] detect unchanged frames by comparing the hash value or checksum of each frame. While the RFB increases the cost of the display panel, PSR significantly reduces the system energy consumption. This allows mobile-device manufacturers to integrate batteries with smaller capacities, which reduces the cost, form factor, and weight of the mobile device [17, 38, 54].

**PSR Selective Updates (PSR2).** While a mobile system is in the PSR mode, the host SoC can make selective frame updates to the RFB, also known as PSR2 [47, 84, 94, 96]. This optimization can be used, for example, to turn on/off a blinking display cursor. PSR2 is supported by the newest eDP 1.4 [96].

### 2.4 Planar and VR Video Processing

Planar video processing consists of three main stages: 1) buffering of encoded frames, 2) decoding of the buffered frames, and 3) displaying of the decoded frames. VR video processing requires an additional stage, called projection, which is performed immediately before the displaying stage.

**Buffering.** In the case of video streaming, the network IP receives encoded video frames. Similarly, in the case of video playback, the application reads the frames from secondary storage (e.g., an SSD). These encoded frames, each of which is hundreds of KBytes in size, are buffered in DRAM (1 in Figure 2). The buffering process enables the system to mitigate the effects of network bandwidth fluctuation [4] and reduce the number of storage IO accesses, which enables smoother and more efficient video processing. Video encoding uses various video compression algorithms (e.g., H.265 [86], VP9 [67]) to reduce the network transmission time (or the storage needs).

**Decoding.** The video decoder (VD) reads an encoded frame from DRAM (2) and starts decoding it. An encoded frame consists of a number of macroblocks, each of which stores the pixel information of a small exclusive region of the frame [97]. An encoded macroblock is the basic processing element in video decoding, and typically includes 16 × 16, 32 × 32, or 64 × 64 pixels [67, 86, 97]. The VD reads an encoded frame at a macroblock granularity and buffers several encoded macroblocks (e.g., tens of KBytes [97]) inside the VD. Each encoded macroblock first passes through a series of stages including entropy-decoding, inverse-DCT, and inverse quantization [67, 86, 97, 105]. Next, each macroblock is reconstructed in various ways depending on their types. An I-Type macroblock is reconstructed from its neighboring macroblocks of the same frame, whereas a P-Type and B-Type macroblock is reconstructed from the macroblocks in the previous and previous/late encoded frames, respectively, that are indicated by the extra information stored as metadata (motion vectors). Finally, a decoded macroblock is written to the frame buffer in the host DRAM (3) [61, 105] in preparation for the next stage.

**Projection.** In planar video processing, each frame can be directly displayed once decoded. However, each VR frame must go through a set of projection transformations (PT) operations before being displayed. Therefore, each decoded frame is forwarded to the GPU (4), which performs PT operations and writes the processed frame back to the DRAM frame buffer (5) [61, 108].

**Displaying.** The DC reads a decoded frame from the DRAM frame buffer at a chunk granularity (e.g., 512 KB) [8, 47], and stores the frame data within its limited internal buffer.
before sending it to the display panel (4). During the frame transfer, host-side components including the CPU, network interface, and VD enter low-power states (e.g., DRAM in the self-refresh mode [47]). The DC sends the frame chunks over the eDP interface according to the display refresh rate (5). For instance, if the refresh rate is 60 Hz, the DC sends the frame chunks to the display panel within a window of ~16 ms (i.e., 1/60 sec), which we refer to as a frame window. On the panel side, the eDP receiver forwards the chunks to the Pixel Formatter (PF) (6) [96]. The PF 1) stores the decoded frame into the RFB to support PSR (7) [14, 17, 54, 96], 2) converts the decoded frame into a pixel data array, and 3) sends it to the LCD interface (8). The LCD interface represents each pixel in the panel through row and column drivers to finally display the video frame (9). The PF cannot produce pixels faster than the display panel can consume, which causes a bottleneck in receiving data from the eDP receiver. Therefore, the T-con aligns the eDP bandwidth and the PF’s operational frequency to the resolution and refresh rate of the display panel. This enables the PF to finish setting the image pixels on the display panel within the frame window.

2.5 System Power States in Video Processing

During the video processing flow, the system switches between different power states. Figure 3 shows how the package C-state changes while an Intel Skylake mobile processor [35, 81] renders (a) a 30FPS video and (b) a 60FPS video, respectively, on a 60Hz display panel (i.e., the frame window ≈16 ms). At the beginning of each 16 ms window, the processor resides in C0 power state [35], an active state where all the system components (i.e., CPU cores, GPU, VD, DC, eDP interface, and display panel) are running. This C0 state corresponds to buffering of new encoded frames (1 in Figure 2) and frame decoding by the VD (2 and 3). In the case of VR video processing, the CPU performs PT operations while in C0 state (4 and 5). Once the decoding stage is complete, the processor enters C2 power state, during which the DC fetches a chunk of the decoded frame (6). In C2 state, the CPU core remains inactive (i.e., power-gated). Once the DC buffer is full, the path to the host DRAM is closed and the system enters the C8 power state [35], where only the DC, eDP interface, and display panel are active. While in this state, the DC transfers the frame chunk over the eDP interface (7). When the DC buffer is almost empty, the DC forces the processor to return to C2 state, in order to open the path to the host DRAM and fetch the next chunk of the decoded frame. This sequence of power states repeats until the entire decoded frame (e.g., 24 MB for a 4K video) is transferred to the display panel.

A display panel with a 60Hz refresh rate can support up to 60 FPS. When the video frame rate is 30 FPS, each decoded frame is updated on the panel twice (back to back) as shown in Figure 3(a). During every other frame window for a 30FPS video (e.g., second frame window in Figure 3(a)), the RFB provides the buffered frame data to the PF (9) to refresh the display (PSR). During this entire frame window, the whole processor, DC, and eDP interface can be disabled, which enables the system to enter the deep low-power state C9 [35]. The PSR technology significantly reduces the energy consumption of the entire display subsystem, and we use this as a baseline for evaluation in the rest of the paper. Figure 3(b) shows the power C-state timeline while the same system plays a 60FPS video. Since the video frame rate matches the panel refresh rate, the system performs the same computations in each frame window, and PSR is not utilized.

Figure 4 shows the system power consumption and package C-state residency distribution when running a web-browsing workload followed by a FHD 60FPS video streaming workload on a 60Hz display. The figure shows that, while video streaming, the system mostly resides at C8 (~75%), C2 (~15%), and C0 (~8%) states, while infrequently entering other package C-states for very short times (e.g., the total residency of C3/C6/C7 states is less than 2%).

3. MOTIVATION

We present our key observations that motivate a new energy-efficient video display scheme in modern mobile systems. Observation 1: Unnecessary data movement between the display subsystem and host DRAM. In current video processing schemes, the VD (GPU for VR videos) stores each decoded frame into the frame buffer at the host DRAM (3 and 4 in Figure 2), and the DC fetches the decoded frame to send it to the display panel (5). Doing so is necessary when there exist other planes in addition to the video plane.\(^5\) For example, suppose that there are four planes to display: 1)
the background plane that is typically a static image, 2) the video plane that contains the video stream, 3) the application-graphic plane for the graphical user interface (GUI), and 4) the cursor plane to display the cursor. In such a case, each plane has its own frame buffer in the host DRAM. The DC reads data chunks from each buffer, generates one composed chunk out of them, and sends the composed chunk to the display panel. However, when the user plays a video in full-screen mode (which is common for planar videos and is the default for VR videos), storing the decoded frame into the host DRAM is unnecessary since there is no other plane for the DC to merge with the video plane.

**Observation 2: Underutilization of the eDP interface bandwidth.** As explained in Section 2.4, the DC first reads a decoded video frame at chunk granularity (e.g., 512 KB) in C2 power state, and the system switches to C8 state while the DC sends the chunk to the display panel. This segmented transfer is repeated until the full decoded frame (e.g., 24 MB for a 4K resolution) is sent to the display panel, keeping both the DC and eDP receiver active during the entire frame window (e.g., ~ 16 ms in a 60Hz refresh rate). However, the newest eDP interface [96] supports a maximum bandwidth of 25.92 Gbps, where it takes only 7.2 ms to transfer an entire 4K decoded frame. This means that the DC and eDP receiver can potentially switch to a power-saving mode for 55% of the 16 ms frame window after decoding and sending the entire frame in one burst.

Table 2 shows the potential benefits of a burst-transfer approach over the baseline, by comparing the average power consumption and system-residency time (Resid.) at each package C-state within a 16 ms frame window while streaming a 4K 60FPS video on a 60Hz display. Unlike the baseline that alternates C2 and C8 states throughout each full frame window, a burst-transfer approach allows the system to decode an encoded frame and transfer the decoded frame at once in C2 and C8 states, respectively. Doing so reduces the time the system resides in each of the two C-states from 43% to 20% and allows the system to stay in C9 state for a longer time (i.e., the rest of the frame window). Note that, although the burst-transfer approach increases the average power consumption in C0, C2, and C8 states due to more DRAM/RFB accesses (explained more in Section 4), it significantly decreases the average power consumption per frame window by 25.1% (3,726 mW → 2,792 mW).

![Figure 5: BurstLink video processing and displaying.](image)

**4. BurstLink Design**

To address the two inefficiencies discussed in Section 3, we propose BurstLink, a new energy efficient display subsystem that takes full advantages of the RFB in PSR-enabled display panels and the high bandwidth of the eDP interface. BurstLink reduces the overall system energy using two key mechanisms, namely Frame Buffer Bypass and Frame Bursting. In this section, we describe how the two mechanisms make video display and other mobile workloads more energy-efficient in modern mobile systems.

Fig. 5 describes the overall architecture of the display subsystem that we extend to support the two main mechanisms of BurstLink. We re-architect the display panel in two ways. First, we extend the RFB to Double-RFB (DRFB), which allows the eDP receiver to concurrently fill the DRFB with a new frame while the PF updates the LCD pixel data of the current frame in the DRFB. Second, we modify the display-panel data path to allow the eDP receiver to directly update the DRFB with the received frame at the eDP receiver’s rate regardless of the PF’s update rate (which depends on the display resolution).

**4.1 Frame Buffer Bypass**

The Frame Buffer Bypass technique redirects the processed frame from the VD (or the GPU) to the DC via the on-chip interconnect (2 in Fig. 5). Fig. 6 depicts the package C-state timeline throughout the Frame Buffer Bypass procedure. Once the orchestration tasks are completed by the CPU, the VD sends the processed frame directly to the DC buffer6, instead of first buffering it in DRAM. Bypassing DRAM allows this process to be performed while the system is in the low-power state C7 (described in Table 1), instead of the C0 power state required by conventional systems. When the DC buffer is full, the VD is halted until the DC transmits the data to the DRFB in the display panel over the eDP interface. At this point, the system power state reduces even further to C7’.

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6The DC buffer is implemented as a double-buffer [47], which allows the DC to send frame data to the display panel while it is simultaneously receiving data for another frame.
Once the buffer is almost empty, the DC notifies the VD via the PMU (empty and wakeup signals in Figure 5) so that the VD can continue transferring the frame to the DC buffer. The display panel receives the data over the eDP interface and stores it directly into the DRFB inside the display. The PF pulls the frame data from the DRFB at its own IO rate and renders the pixels on the panel.

The above process of BurstLink provides two key advantages over conventional systems. First, BurstLink effectively bypasses DRAM in most of the video processing stages, thereby reducing the majority of its DRAM bandwidth and energy consumption. Second, BurstLink also reduces the orchestration overhead in which the application and driver are involved (e.g., programming the DMA engines and handling interrupts), which decreases active power state residency (i.e., C0) and increases idle power state residency (e.g., C7 or C7') in which the host DRAM is in the self-refresh mode. Third, the Frame Buffer Bypass technique effectively interleaves the decoding (projection) and displaying stages in planar and VR video processing. Unlike conventional systems that decode (or project) the entire frame at the beginning of the frame window in power state C0, our technique distributes the frame decoding process across the frame window while keeping intermediate data inside the DC buffer and the DRFB. Doing so allows the decoding process to be performed in the C7 low-power state without any performance penalty compared to conventional systems.

**Windowed Video Support.** In addition to full-screen planar and VR videos, BurstLink uses the Frame Bypassing technique for a *windowed planar video* such as a video clip played in a window inside the browser (e.g., YouTube [19]). This is enabled by the selective update capability of PSR (i.e., PSR2 described in Section 2.3) that is supported by the eDP 1.4 protocol [96].

BurstLink performs windowed video streaming in two stages. In the first stage (which is the same process in conventional systems), the system prepares an initial frame with the traditional components. Suppose that a user watches a streaming video played on a web browser. In this case, the GPU prepares the graphical parts of the browser, and the VD decodes the video frames downloaded from the content server (e.g., YouTube) via network. The frames from the GPU and the VD are stored separately in different DRAM frame buffers. Then the DC reads, scales (i.e., resizes the video frame to fit the browser window), and overlays the frames to generate the final integrated frame that is sent to the panel and stored in the DRFB (or the regular RFB in conventional systems).

The second stage starts once the host processor detects that the graphical frames from the GPU are not changing (i.e., only the video window is being updated). Then the host processor informs it to the DC and VD so that the display subsystem operates in the PSR2 mode. In this stage, the VD continues decoding the downloaded frames and sends the decoded frames directly to the DC. The DC then directly sends only the decoded video frames (after scaling them) to the eDB receiver with the offsets of the video frames (i.e., the updated region). The eDB receiver selectively updates the video only at the corresponding offsets in the DRFB, and the PF renders the entire frame into the LCD display.

**Support of Legacy Cases.** In all cases that are not supported by BurstLink, the system falls back to the legacy display mode. This means that whenever multiple planes are required (e.g., for the cursor and for the video plane), the system operates using the conventional scheme in which all the decoded frames are transferred through the DRAM frame buffer. To this end, BurstLink *dynamically* selects the destination of the VD/GPU output (i.e., the decoded frame) using the destination selector inside the VD/GPU. As shown in Figure 5, the destination selector directs the decoded frame to the DC (CC) when displaying only the video plane. Otherwise, it stores the decoded frame into the DRAM frame buffer (R) as in conventional schemes.

Legacy cases that are not supported by BurstLink include: 1) when `video_plane_only` signal is deasserted by the application, 2) when there is a graphics interrupt (to the DC [47]) indicating that a graphics plane is pending (e.g., when the application’s GUI appears), and 3) when the system escapes from the PSR2 mode (in case of windowed video displaying) due to an user-input interrupt (e.g., from the touch screen or keyboard). Note that additional content like a closed-caption (CC) [50, 98] arrive with the video stream and do not require multi-plane support as such contents are handled by the video decoder.

### 4.2 Frame Bursting

In conventional display subsystems, the transfer rate between the DC and the display panel (i.e., the eDP’s transfer rate) is set depending on the display resolution (i.e., the number of pixels per frame), refresh rate (i.e., the number of displayed frames per second), and color depth (i.e., the number of bits per pixel (bpp)) [47]. Since the PF’s throughput is dictated by the pixel-update speed of the LCD panel, conventional systems align the eDP transfer rate with the PF frequency, which leads to a far lower eDP transfer rate than the maximum bandwidth of the eDP interface (e.g., up to 25.92Gbps in eDP 1.4 [96]). This far-optimal transfer rate bottlenecks BurstLink’s full video processing pipeline and causes the system to alternate between C7 and C7' power states (as shown in Figure 6) even though it can enter a lower power state (C9) after quickly decoding and transferring a full frame.

In order to leverage the maximum eDP interface bandwidth, we propose **Frame Bursting**, a mechanism to burst transfer
the decoded frame from the processor to the display panel. With the Frame Bursting technique, the display panel receives a full frame over the eDP interface and stores it directly into the DRFB (in Figure 5) before transferring the frame to the PF, which removes the slow update process between the PF and the LCP panel from the critical path. The PF can fetch the frame data from the DRFB at the rate required by a given configuration (i.e., the display resolution, refresh rate, and color depth) to generate pixels and send them into the LCD display. This reduces the utilization of the processor and the display subsystem, enabling the system to enter deep low-power states after transferring the decoded frame to the DRFB. In these states, all unused resources (e.g., the DC, eDP interface, and DRAM) are turned off.

4.3 System Power States in BurstLink

Figure 7 shows the power C-state timeline of a system that supports complete BurstLink (i.e., both Frame Buffer Bypass and Frame Bursting) while rendering a 30FPS planar video on a 60Hz display panel. The system resides in power state C0 at the beginning of a frame window, where the display driver sends the encoded video frame to the VD. The system then moves to state C7, where DRAM operates in self-refresh mode. The VD decodes the video frame in multiple chunks and sends them to the DC, which transfers the chunks to the DRFB over the eDP interface at maximum bandwidth. Once the entire decoded frame is sent to the DRFB, the system enters the deep low-power state C9, in which most components including the VD, DC, and eDP interfaces (both on processor and panel sides) are power-gated.

![Figure 7: Power-state timeline of a mobile processor with complete BurstLink.](image)

Table 3 compares BurstLink to conventional video processing (Baseline), in terms of the average power consumption in each power state Ci and the power-state residency (Resid.), i.e., the percentage of a frame window that the system resides in state Ci. As shown in Table 3, BurstLink significantly reduces the average power consumption over conventional video processing by more than 40% by 1) enabling the system to reside in lower power states (i.e., C2, C8 → C7, C9) and 2) reducing the time that the system resides in higher power states. We discuss BurstLink’s power/energy savings in more detail in Sections 5 and 6.

| Package C-States | C0 | C2 | C7 | C8 | C9 | AvgP (mW) |
|------------------|----|----|----|----|----|-----------|
| Baseline (measured) | 5940 | 5445 | 1385 | 1285 | 1090 | 2162 |
| Residency (%) | 9% | 11% | 80% | - | - | - |
| BurstLink (estimated) | 6000 | 5740 | 1530 | 1435 | 1090 | 1274 |
| Residency (%) | 2% | 19% | 79% | - | - | - |

4.4 Implementation and Hardware Cost

While Frame Buffer Bypass and Frame Bursting can be implemented independently on a conventional display subsystem, BurstLink incorporates both mechanisms to maximize the energy efficiency. BurstLink requires three major changes to a conventional system. **Double-RFB.** While using the double-RFB (DRFB) introduces additional cost, power, and area overheads, it would not be a serious obstacle for a wide adoption of BurstLink due to four reasons. First, according to the bill-of-material (BOM) cost estimation of Microsoft Surface Pro [88] (our evaluated system), DRAM’s BOM cost is 13.9$/GB, while the full HD display panel costs 100.45$/[88]. Based on this estimation, doubling the existing Tcon’s RFB from 24MB to 48MB will increase its BOM cost by only 32.5 cents (i.e., 13.9 × 24/1024), which is just a 0.3% increase in the total BOM cost of the display panel (0.05% of the mobile device BOM cost). Second, according to our estimation based on Samsung’s recent proposal for a cost-effective RFB implementation [44], the additional power overhead from doubling the RFB is 58 mW (6% of the display panel power), which is significantly lower than BurstLink’s power savings. Third, the proposal from Samsung [44] also shows that it is possible to reduce the RFB’s pin count, which can mitigate the area overhead of the DRFB. Note that the DRFB does not increase the panel size since the DRAM is mounted on a flexible printed circuit board FPCB rather than the panel. Finally, recent trends implement the RFB using embedded DRAM (eDRAM) [54] and emerging memory technologies such as MRAM [59], which can significantly reduce the cost/power/area overheads.

**Destination Selector.** As shown in Figure 5, BurstLink dynamically selects the destination of the VD’s output depending on the 1) single_video flag in the VD and 2) video_plane_only signal from the DC to the destination selector. The flag and signal can be determined using two data elements that are already stored in configuration registers in the VD and DC. First, since each video application injects its own requests into the VD using the driver API [31, 69, 103, 105], the VD already keeps track of the number of concurrently-running video applications (and their requirements) in its control and status registers (CSRs). Second, each application also sends its requirements to the DC [47, 64], the number of the used planes and each plane’s type (e.g., video, graphics, or cursor) are available in the DC CSRs (e.g., SR02 and GRX registers in Intel DC [47]).

**PMU Firmware Changes.** BurstLink requires changes to the PMU firmware to 1) enable the processor to enter power state C9 when Frame Buffer Bypassing is enabled, 2) wake up the VD (i.e., switch to power state C7) to resume frame data decoding once the DC buffer is empty, and 3) enable the DC to transfer the decoded frame data using the maximum eDP bandwidth when Frame Bursting is activated. We estimate that these changes increase the power-management firmware code (e.g., Pcode [32] in the Intel Skylake SoC) by only a few tens of lines, which leads to only a 0.004% increase in the processor’s die area for the Intel Skylake SoC [26].

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8 This estimation is based on the number of code lines for Pcode in Intel Skylake systems to fill the DC buffer.
4.5 Generalization of BurstLink Techniques to Other Scenarios

BurstLink aims to improve the energy efficiency of video-streaming (which is one of the most important application scenarios in modern mobile systems), but the proposed techniques can also be used in more general frame-based applications such as video capturing (recording), audio streaming, video chat, social networking, and interactive games. A general takeaway from BurstLink is that using main memory (DRAM) as a communication hub between system components can be energy-inefficient. Instead, BurstLink uses small remote memory (e.g., 48MB DRFB, which is only 0.3% of 16GB DRAM) near the data consumer (e.g., a display panel) or the data producer (e.g., a camera sensor) to significantly reduce the number of costly main-memory accesses in frame-based applications.

Video Capture Example. Fig. 8 shows an additional example (i.e., video capture) in which BurstLink techniques can be applied. The five steps for video capture and storage in a solid-state drive (SSD) in a baseline system [106, 109] are depicted with gray components and dotted-lines. The Camera Sensor generates raw image data and transfers it to the host processor via the camera serial interface (CSI) transmitter. The sensor interface (SI) stores the raw data in DRAM. The image signal processor (ISP) reads the raw data and stores the processed RGB data (i.e., pixels) into the DRAM frame buffer. The video encoder (VE) reads the pixel data from memory and encodes it. The encoded frames are finally stored in the SSD.

By applying the two techniques of BurstLink, we can significantly reduce the energy consumption of video capture. First, we implement a double remote frame buffer (DRFB) inside the camera sensor to capture an entire frame of raw image data. Next, once a full frame is captured inside the DRFB, the camera sensor bursts the data DRFB to the ISP, using the on-chip interconnect, while bypassing DRAM. The output of the ISP is directed to the VE. The VE encodes the frames, which are then stored by the application into the SSD. Similar to BurstLink, the PMU orchestrates the data flow using control signals (green) that indicate whether the internal buffer and IP (i.e., ISP or VE) is full or new data should be received from the previous IP in the chain. This new architecture for video capture significantly reduces the energy consumption by bypassing DRAM and increasing idle time in the system interfaces (e.g., CSI).

5. METHODOLOGY

In this section, we describe our methodology for evaluating BurstLink. First, we describe our workloads. Second, we introduce our industry-standard analytical power model for evaluating the baseline model and BurstLink. Third, we discuss our process for validating our model against power measurements of a real modern mobile device.

5.1 Workloads

We evaluate BurstLink with planar and VR video-streaming workloads [5, 24], which are used in standard industrial benchmarks for battery-life [1, 5, 72, 73, 74] and academic evaluations of video-streaming optimizations [16, 30, 61, 68, 69, 78, 103, 105, 108]. In typical evaluations, it is assumed that only a single application (e.g., video streaming in our evaluation) is running on the system. In smartphones and tablets, the currently used application typically runs in full-screen mode while the other opened applications are normally sent to the background and moved to a suspended state. This is also true of our evaluated system, the Microsoft Surface [99], when running in Tablet-Mode [90].

5.2 Analytical Power Model

Modeling the Baseline System. Our analytical power model estimates the system average power $P_{avg}$ within a frame window as follows:

$$P_{avg} = P_C + R_C + \sum_{i=10}^{169} P_{en} \cdot R_{en} \cdot Lat_{en} + P_{ex} \cdot Lat_{ex}$$

$P_C$ denotes the system average power consumption in power state $Ci$. $P_{en}$ and $P_{ex}$ denote the average power consumption of the system while entering and exiting from state $Ci$, respectively. $R_C$ denotes the residency at power state $Ci$, i.e., the percentage of the total time the system spends at power state $Ci$. $Lat_{en}$ and $Lat_{ex}$ denote the latency for entering (exiting from) power state $Ci$. In addition, our power model accounts for system parameters of 1) the DC buffer size, 2) DRAM capacity, 3) DRAM bandwidth, and 4) eDP bandwidth.

These parameters can directly affect the residency and power consumption in each state and the frequency that the system switches between power states. For example, a small DC buffer results in more frequent transitions between C2 and C8 states to fill the DC buffer (as shown in Figure 3), which increases the energy consumption of video streaming.

In our analytical power model, memory power consumption is modeled in two parts: 1) background power, which is consumed regardless of memory access characteristics and only depends on DRAM power states (i.e., self-refresh, CKE-High (active), CKE-Low (fast power-down) [25]), and 2) operating power, which highly depends on DRAM read/write bandwidth. First, to model background power, we record the time spent in each DRAM power state. We weight the power consumption in each state by the measured time values to obtain the average background power. Note that the DRAM power states in our processor are correlated to the package C-states. For example, DRAM is inactive (CKE-High) only in C0 and C2 states, while entering self-refresh state in all other package C-states. Second, operating power is modeled by multiplying the average power per unit read/write bandwidth (e.g., 1 GB/s) by the actual read/write bandwidth consumed. To determine the average power per unit read (write) band-
width, we 1) run a memory benchmark that generates reads (writes) in different bandwidths, 2) measure DRAM power consumption, and 3) extrapolate the power consumption per 1GB/s reads (writes). A similar power modeling technique is used by Intel [7,25,37] and by other works from both industry and academia [21,49,62,66,107].

**Modeling the BurstLink System.** We model the power consumption of the system enhanced with the two techniques of BurstLink using the measured data in the baseline model. The two techniques of BurstLink affect both the residency and power level at each package C-state. For example, C9 residency increases as the system finishes transferring each decoded frame more quickly.

We carefully model the new average power consumption (i.e., $P_i$) and the new residency (i.e., $R_i$) at each power state $C_i$, taking into account two essential factors: 1) a system component (e.g., power-gated DC or DRAM in self-refresh state) in each power state, and 2) changes in each SoC component’s operating frequency (e.g., the DC and eDP interface consume more power when using the maximum eDP bandwidth for Frame Bursting). We plug in the new values in our analytical model to evaluate the average power consumption when applying each of BurstLink’s techniques.

### 5.3 Validation of Our Power Model

**Baseline System.** We use an Intel reference design for high-end tablet devices [104], such as the Microsoft Surface Pro [99]. Our baseline system is equipped with an Intel Skylake [26,28] processor (whose specifications are summarized in Table 4) and multiple debug/configuration capabilities.

| Table 4: Baseline system. |
|----------------------------|
| Processor | Intel i5-6300U Skylake, 14 nm, TDP: 15 W |
| Memory | LPDDR3-1866MHz, 8 GB, dual-channel |

To validate our power models for the baseline and BurstLink systems, we carry out the following experiments: 1) measurement of the average power and residency at each power state in the baseline system, 2) breakdown of the measured power to each SoC component’s power consumption, and 3) measurement and estimation of the effect of frequency/bandwidth changes on the average power and residency at each power-state.

**Measurement Setup.** For the system power measurements, we use a Keysight N6705B DC power analyzer [51] equipped with an N6781A source measurement unit (SMU) [52]. The N6705B is normally used for high accuracy power measurement (around 99.975% [52]) of low-power devices (e.g., smartphones and tablets). The power analyzer measures and logs the instantaneous power consumption of different device components. Control/analysis software (14585A) for data visualization and management runs on a separate laptop connected to the power analyzer.

Figure 9 shows the measurement setup of our Skylake mobile system [26,28,36]. The system has a battery and multiple power supplies (i.e., voltage regulators) for the mobile system components. We refer the reader to Keysight’s manual [51] for more details on the actual connections of measurement wires to N6705B power analyzer, the design under test (DUT), DUT’s battery, and control/analysis software. The power analyzer can measure the power consumption of the different power states (C0, C2, and C7–9) in a single experiment. We measure the residency of each C-state using the Intel VTune profiler [46].

**Baseline Power Measurements.** We carry out multiple measurements for different system components, including the processor, DRAM, chipset, and display. As illustrated in Figure 9, the power analyzer’s four channels are connected to measurement points $f$ for individual power domains, and to measurement point $T$ for the total system power drained out of the battery. For the processor power, we measure four voltage domains: 1) $V_{Core}$, the voltage supply for cores and last-level-cache (LLC), 2) $V_{GFX}$, the voltage supply for the graphics engine and the VD, 3) $V_{IO}$, the voltage supply for the IOs including the eDP, DDRIO (digital part), and the interface to the chipset, and 4) $V_{SA}$ is the voltage supply for the system agent that contains several controllers, including the memory controller and DC. Each measurement uses four analog channels with a 50-μs sampling interval.

**Power Breakdown to sub-components.** Further breakdown sub-components of the measured processor power consumption is obtained using power estimation techniques [34]. Using the design characteristics of these components (such as capacitance, leakage, operational frequency, and voltage), we estimate their relative power consumption. Next, using the processor’s measured data, we estimate the power of each component. It should be noted that other power estimation techniques can be applied to determine this power breakdown [15,18,58].

**Power Model Accuracy.** To validate our model, we run four representative battery life workloads [5], web-browsing, light-gaming, video conferencing, and video-playback with multiple display resolution setups. We measure the average power of the system (as explained above) and collected the package C-states residencies along with each run. We used our analytical power model to estimate the average power consumption of these workloads. Then, we compare the measured vs. estimated average power consumption. We found that the accuracy of our analytical power model is approximately 96% for the tested workloads. The accuracy of each of the four main used power state in battery life workloads, C0, C2, C7, and C8, is 97.4%, 96.2%, 95.1%, and 94.7%, respectively. The deeper the power state, the larger its accuracy variation.

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9 The system agent houses the traditional Northbridge. It contains a memory controller and several functionalities, such as the IO controllers [100].
6. EVALUATION

We evaluate BurstLink against the baseline display subsystem (described in Figure 2) with six studies. 1) We study energy reduction for four different display resolutions for planar video streaming. 2) We show energy reduction of different workloads and resolutions for VR video streaming. 3) We show the effect of frame rate on BurstLink energy reduction. 4) We present a sensitivity analysis of system parameters. 5) We compare BurstLink to state-of-the-art techniques that reduce energy costs of video processing. 6) We evaluate the benefits of BurstLink for other mobile workloads.

6.1 Planar Video Streaming Energy Reduction

Figure 10 shows the energy comparison of each individual technique of BurstLink (i.e., Burst, Bypass), and the combined techniques (i.e., BurstLink) with respect to the baseline system over one frame window for a 30 FPS video displaying on a 60 Hz panel. Since the frame window length is fixed by the display refresh rate (~16 ms in this case), the average power dissipated during the frame window is proportional to the energy consumption in the same frame window.

We make two major observations. First, BurstLink reduces the overall system energy consumption by 37% for an FHD display. Frame bursting and frame buffer bypassing decrease overall energy by 23% and 31% as compared to the baseline, respectively. Second, BurstLink’s energy reduction improves with an increase in display resolution. For a 4K display, BurstLink decreases the overall energy by ~41%.

Figure 11 compares BurstLink’s system energy consumption breakdown across three components, i.e., DRAM, display, and others (which includes processor, WiFi network card, and eMMC storage) with that of the baseline system. BurstLink reduces the total dissipated energy from DRAM by 3.8× and 5.7× for FHD and 5K resolutions, respectively.

6.2 VR Video Streaming Energy Reduction

Figure 12 shows the energy reduction of five 360° VR streaming workloads [24] when running with BurstLink. We assume an optimized state-of-the-art VR streaming scheme [61, 108], which significantly reduces the compute energy compared to traditional schemes.

We make two major observations. First, BurstLink reduces the overall system energy consumption by up to 33%. Compute energy dominant (mainly GPU) workloads have lower benefits compared to memory energy dominant workloads. Second, BurstLink’s benefits decrease as VR display resolution increases. This is mainly because the compute energy becomes more dominant in VR workloads as the resolution increases, which leaves fewer relative savings for BurstLink from the memory energy.

6.3 Effect of Video Frame-rate

We evaluate BurstLink with 60 FPS HD videos. BurstLink’s energy reduction improves with an increase in video frame-rate. As shown in Figure 13, BurstLink reduces the overall energy consumption by 46% and 47% for FHD and 5K display resolutions, respectively.

Based on these results, we make three key observations. First, workloads with 60 FPS obtain higher energy benefits. This is expected since, for workloads with 30 FPS, the bandwidth reduction optimization shown in Fig. 3 (i.e., taking the second refreshed frame from PSR) is applied to reduce the baseline bandwidth. Second, DRAM and eDP bandwidth consumption increase with an increase in display resolution and/or refresh-rate. As a result, BurstLink’s energy reduction also increases with an increased display resolution and/or refresh rate. This makes BurstLink even more important for future display technology given the trends of increasing resolutions and refresh rates. Third, the wider gap between display resolution/frame-rate and video streaming resolution/frame-rate (as we discuss in Section 1) allows bursting the frame data into the RFB in the display frame buffer, which increases the system’s residency in lower power states.

6.4 Sensitivity Analysis

We investigate the impact of four system parameters on BurstLink energy reduction: DRAM capacity, DRAM frequency, eDP frequency, and DC buffer size. Figure 14 shows
the energy reduction of BurstLink when running on systems with $2 \times$ higher/lower values of one of these system parameters$^{10}$ over the baseline system (shown in the middle column). We make three key observations. First, the energy reduction of BurstLink increases with an increase in DRAM capacity and frequency. This is because the larger (higher) the DRAM capacity (frequency), the higher the power consumption in both active and self-refresh states. As a result, BurstLink energy reduction from using frame buffer bypassing and frame buffer bursting techniques increase. Second, BurstLink achieves higher energy reduction as the eDP bandwidth increases due to the higher bandwidth margin that the frame buffer bursting technique can utilize. Third, increasing the DC buffer size decreases the energy reduction of BurstLink, since the energy consumption of the baseline decreases as the system can spend more time in lower-power state.

![Figure 14: Energy reduction of BurstLink for streaming 60 FPS HD video on a 4K resolution display when sweeping system parameters.](image)

### 6.5 Benefits over Existing Techniques

We study the benefits of using BurstLink with state-of-the-art techniques such as 1) compression schemes [3, 9, 10, 27, 47, 70, 79, 85], and 2) a recent technique by Zhang et al. [105] that combines race-to-sleep, content caching, and display caching techniques.

**Effect of Frame Buffer Compression (FBC).** The evaluated Intel Skylake system supports FBC [47], which leads to high computational overheads [9, 85] and significant storage overhead. For example, Intel’s FBC uses stolen graphics data memory for the compressed frame buffer [47]). Moreover, FBC may cause reliability issues due to the design complexity of compression blocks and algorithm [75]. Therefore, several systems allow the display driver to enable or disable this feature [3, 9, 47].

![Figure 15: Energy reduction of BurstLink with respect to a baseline with frame buffer compression (FBC) for a 4K resolution display with a 60Hz refresh rate.](image)

**Race-to-Sleep, Content Caching and Display Caching.** Haibo et al. [105] propose a mechanism to save video processing energy consumption by applying three techniques: 1) batching several frames and boosting the VD frequency to decode multiple frames, 2) caching decoded macroblocks in VD to reduce the data written to DRAM, and 3) using a cache in DC to reduce the amount of data that is read from DRAM. This mechanism is an extension of a previously proposed mechanism, *short-circuiting* [103], which proposes techniques 2) and 3).

Haibo et al.’s mechanism has significant design complexity because it requires the implementation of two special cache schemes, frames batching and decoding several frames together. The average DRAM bandwidth reduction of this mechanism is 34% [105] (for the three techniques combined), which can reduce the overall system energy consumption for 4K by 6%. BurstLink, on the other hand, completely eliminates the DRAM storage overhead by transferring the decoded frame directly to PSR, and reduces the overall system energy consumption by 40.6% for 4K displays. We conclude that BurstLink has 35% higher energy reduction than the three techniques combined (including short-circuiting [103]), which are applied by Haibo et al. [105].

**Virtualizing IP chaining.** Virtualizing IP chaining (VIP) [69] proposes two main mechanisms. First, it reduces the CPU core orchestration overhead of invoking several IPs when running frame-based applications (e.g., video playback) by 1) proposing virtual IPs changing, and 2) initiating the handling of multiple frames at the same time. BurstLink also reduces the CPU core orchestration overhead (from approximately 10% to less than 5% of the frame time) by offloading part of the orchestration task to the PMU firmware (as we discuss in Sec 4.1). One of the main advantages of BurstLink over VIP is that unlike VIP, which requires substantial changes to the software stack, BurstLink is transparent to the application and requires only few changes to the drivers (e.g., video decoder driver).

Second, VIP reduces the traffic to DRAM by direct communication between IPs (IP-to-IP chaining) instead of using DRAM. Compared to BurstLink, VIP is limited due to two main reasons. First, the traffic of frame-based applications is not always a chain. In many cases, one IP waits for traffic from two (or more) other IPs/sources to complete its task.

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$^{10}$ In terms of DRAM frequency, 2133 MHz (1600 MHz) represents the $2 \times$ higher (lower) configuration than our baseline system.
For example, in widowed video playback (discussed in Section 4.1) the DC needs the data of multiple frame-buffers to generate the final image. Second, VIP does not solve the key bottleneck in the display data flow, where the decoding and displaying processes occupy the entire frame window (e.g., within 16 ms), because the display panel consumes the frame data within the entire frame time. This forces the VD, DC, and eDP interfaces (at both SoC and display panel) to remain active across the entire frame. BurstLink avoids this bottleneck with the frame bursting technique.

In addition to the above advantages of BurstLink over VIP, our results (when modeling VIP using our power model) show that BurstLink has 26% higher energy reduction over VIP for 4K video streaming workloads due to the ability of BurstLink to turn-off the VD, DC and eDP interfaces during the majority of the frame window.

6.6 Benefits to Other Mobile Workloads

Besides video streaming, other popular mobile workloads can benefit from BurstLink’s two mechanisms, i.e., frame buffer bypassing and frame bursting. In this section, we show the following two examples.

First, high resolution local (i.e., not streaming) video-playback (e.g., 4K with 120/144Hz or 5K with 60Hz) can benefit from the DRAM frame buffer bypassing technique by saving DRAM energy consumption. Figure 16(a) compares the energy reduction of our frame buffer bypassing technique when playing three local video files with different resolutions and/or frame rates.

Second, mobile workloads such as video capturing, video conferencing, casual gaming [5] and MobileMark11 [13]. In a mobile device (e.g., a tablet) these workloads render images on the display using one plane (normally the graphics plane). In these applications, the DC transfers the frame data from the DRAM’s frame buffer into the display panel. When the DC detects that a single plane exists12, it activates the frame bursting mechanism of BurstLink, which transfers the frame buffer from DRAM into the DRFB in burst. Frame bursting reduces energy consumption by 1) increasing the idle time of these workloads, as the workloads spend less time in transferring the frame buffer and more time in sleeping in low-power states, and 2) power-gating the DC and eDP interface at both the processor and the display panel. Figure 16(b) shows the energy reduction of Frame bursting for four workloads on a high-end tablet.

7. RELATED WORK

To our knowledge, this is the first work to leverage PSR memory to improve the energy efficiency of video processing in modern mobile systems. BurstLink significantly reduces costly data movement between DRAM and display subsystem components and enables frame transfer with the maximum eDP bandwidth, which allows the system to reside in lower power states. We briefly discuss related prior work that we classify into five categories: 1) buffer compression, 2) frame batching, 3) content and display caching, 4) optimizing frequency/voltage, and 5) other PSR-based proposals.

Buffer Compression. Many prior works [9, 10, 27, 43, 79, 85, 101] propose various frame buffer compression techniques, such as run-length encoding (RLE) and differential pulse code modulation (DPCM), which increase the effective DRAM bandwidth (by reducing the amount of transferred frame data) and thus improve display processing performance. BurstLink is orthogonal to these proposals and can further improve energy efficiency when combined with these compression techniques on redirected data to PSR.

Batching of Decoded Frames. Zhang et al. [105] propose three optimizations to increase the idle time (race to halt) and reduce bandwidth from VD to DRAM and from DRAM to DC in video processing. Their proposals lie across batch processing, content and display caching, and optimizing frequency/voltage. BurstLink is orthogonal to this work as it 1) bypasses the DRAM and 2) increases the idle time by reducing the time that DC sends the frame to the frame buffer.

Other prior works [20, 48, 92] propose different batching and pipelining techniques at a macro-block level. As BurstLink offers achieving energy efficiency through leveraging PSR memory directly, similar techniques for batch processing can be orthogonally applied to increase the energy improvement.

Content and Display Caching. Address [12, 22, 87] and value locality [65, 80, 102, 105] in video frame decoding are a well-studied research direction. BurstLink is orthogonal to these proposals because it offers a way to bypass DRAM in video processing stages completely. We believe that a more lightweight method of content and display caching similar to prior works can also be applied to BurstLink.

Video processing also emerges in Virtual Reality (VR), and as Leng et al. [61] show, VR applications also suffer from having high DRAM energy, and caching mechanism can help with that. We argue that the second technique of BurstLink can be utilized to save significant energy of the VR workload as well as enable the DC to transfer the frame buffer from the DRAM to the display directly, which enables the system to enter into the idle state for a longer time. However, we left the further analysis of VR applications to the future work.

Optimizing Frequency/Voltage. Several prior works rely on reducing the voltage and frequency of their computation (decoding/encoding) circuit to achieve energy efficiency [68, 77, 78]. BurstLink, on the other hand, does not depend on frequency/voltage scaling for its energy improvement.

Other PSR-based proposals. Prior works [14, 17, 38, 54, 56,
We thank the anonymous reviewers of HPCA 2021 and ISCA VR video displaying scheme that utilizes display panel local memory (DRFB). BurstLink directly transfers a full decoded frame from the video-decoder (or GPU) to the DRFB in a burst, exploiting the display interface’s maximum bandwidth. This (1) reduces the energy consumption of the host DRAM by saving round-trip to the DRAM frame buffer, and (2) increases the system’s idle-power state residency. BurstLink reduces system energy consumption for 4K planar and VR video streaming by 41% and 33%, respectively. As video consumption in mobile devices continues to increase sharply, along with an increase in display resolution to meet user satisfaction, we believe that BurstLink will provide high energy efficiency in current and next generation power-efficient processors.

8. CONCLUSION

We introduce BurstLink, an energy-efficient planar and VR video displaying scheme that utilizes display panel local memory (DRFB). BurstLink directly transfers a full decoded frame from the video-decoder (or GPU) to the DRFB in a burst, exploiting the display interface’s maximum bandwidth. This (1) reduces the energy consumption of the host DRAM by saving round-trip to the DRAM frame buffer, and (2) increases the system’s idle-power state residency. BurstLink reduces system energy consumption for 4K planar and VR video streaming by 41% and 33%, respectively. As video consumption in mobile devices continues to increase sharply, along with an increase in display resolution to meet user satisfaction, we believe that BurstLink will provide high energy efficiency in current and next generation power-efficient processors.

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An earlier version of this paper was reviewed favorably at ISCA 2021 but was rejected solely due to a perceived formatting violation. This rejection happened at the Program Committee (PC) meeting, after the authors received the reviews, revised the paper and thoroughly addressed the comments, all the while not being told anywhere in any communication by the conference that there was some important issue related to formatting. Here is the PC summary we received:

“This paper was discussed online. While technically the reviewers were positive on the paper, the fact that the paper had a good amount of violations of the submission rules (i.e., paper formatting) caused the paper to be rejected. Paper formatting was thoroughly enforced in this year’s submissions and several papers where rejected on these criteria. Content wise, we encourage authors to consider the reviewer’s comments as a way to improve technically the paper. We also suggest to be in strict compliance to the submission format guidelines.”

As far as we can tell, the only violation in formatting was line height being 10.7pt as opposed to 11pt in some parts of the paper. The pre-rebuttal score of the paper is shown below.

We believe the ISCA 2021 decision is completely unfair and unscientific. It degrades the importance given to scientific advancement by the conference, placing much greater value on small formatting issues as opposed to ideas and methodologies that advance the state of the art.

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