Upgraded Readout Electronics for the ATLAS Liquid Argon Calorimeters at the High Luminosity LHC

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Abstract. The ATLAS liquid-argon calorimeters produce a total of 182,486 signals which are digitized and processed by the front-end and back-end electronics at every triggered event. In addition, the front-end electronics sum analog signals to provide coarsely grained energy sums, called trigger towers, to the first-level trigger system, which is optimized for nominal LHC luminosities. However, the pile-up background expected during the high luminosity phases of the LHC will be increased by factors of 3 to 7. An improved spatial granularity of the trigger primitives is therefore proposed in order to improve the identification performance for trigger signatures, like electrons or photons, at high background rejection rates. For the first upgrade phase in 2018, new Liquid Argon Trigger Digitizer Boards are being designed to receive higher granularity signals, digitize them on detector and send them via fast optical links to a new, off-detector digital processing system. The digital processing system applies digital filtering and identifies significant energy depositions. The refined trigger primitives are then transmitted to the first level trigger system to extract improved trigger signatures. The general concept of the upgraded liquid-argon calorimeter readout together with the various electronics components to be developed for such a complex system is presented. The research activities and architectural studies undertaken by the ATLAS Liquid Argon Calorimeter Group are described, particularly details of the on-going design of mixed-signal front-end electronics, of radiation tolerant optical links, and of the high-speed off-detector digital processing system.

1. Introduction
The liquid-argon (LAr) calorimeters of the ATLAS experiment [1] have functioned with excellent reliability since installation in 2006 [2]. In the last year they have played a pivotal role in the search for the Higgs boson, particularly in the diphoton and four electron channels [3]. Looking forward there are several constraints: The existing front-end electronics limit the granularity, bandwidth and latency at the level-1 trigger. Additionally, the on detector electronics contain many technologies leading to many opportunities for failure with a limited number of spares. Furthermore, the front-end electronics were qualified for radiation levels corresponding to 10 years of Large Hadron Collider (LHC) operations (with a safety factor of 10). In the high luminosity running of the LHC (HL-LHC) [4], with instantaneous luminosities of $5 \times 10^{34}$ cm$^{-2}$s$^{-1}$ and 3000 fb$^{-1}$, this safety factor will be substantially exceeded. Already by 2018 the peak instantaneous luminosity of $3 \times 10^{34}$ cm$^{-2}$s$^{-1}$ will put pressure on the existing trigger thresholds. By 2022 the readout electronics will need to be replaced entirely in order to enhance the physics reach of the experiment.
Maintaining low thresholds at the level-1 trigger in order to maximize our sensitivity for measurements at the electroweak scale and to probe for new physics at higher energies is the most important motivation for the upgrade. As can be seen in Figure 1, studies of the simulated detector response show that in order to stay within the level-1 bandwidth allowance of 20 kHz for calorimeter triggers, the threshold of non-isolated electromagnetic (EM) objects rises nearly linearly with luminosity. At $2.5 \times 10^{34}$ cm$^{-2}$s$^{-1}$, approximately half of the expected HL-LHC luminosity, the threshold is $E_T = 45$ GeV. Alternatively, one could prescale triggers with a lower threshold. In either case the trigger will fail to select some low transverse energy $E_T$ electrons and photons, such as those produced in the decay of a low mass Higgs boson. In order to record these events the rejection in the hardware trigger at level-1 must be improved. This can be achieved by increasing the granularity available to the level-1 trigger system, which will allow for the implementation of more complex algorithms.

![ATLAS simulation](image)

**Figure 1.** Thresholds for non-isolated EM objects vs. instantaneous luminosity at 20kHz level-1 trigger rate.

2. Upgrade Strategy

Currently, to provide the fast level-1 calorimeter trigger decision only a fraction of the available readout granularity is utilized. The four calorimeter layers are reduced to one “trigger tower” about $0.1 \times 0.1 \text{ in } \Delta \eta \times \Delta \phi$. This tower includes $4 \times 1 (\Delta \eta \times \Delta \phi)$ cells from the presamplers, $32 \times 1$ cells from the first layer, $4 \times 4$ cells from the second layer and $2 \times 4$ cells in the back layer, as shown in Figure 2. The analog sum of the signals from these cells is sent off detector, digitized and clustered for EM objects and (combined with Tile Calorimeter signals) jets. The full precision readout of all the cells is only done after the level-1 trigger accepts the event, with a latency of $\sim 2.1 \mu s$.

To reduce the level-1 trigger rate an increase in the granularity, by adding both lateral and longitudinal readout segmentation, is planned. In this scheme the individual four layers will be read out separately. Both the presampler and the back layer will be summed in the existing $0.1 \times 0.1$ manner, but the first and second layers will be summed into finer $0.025 \times 0.1$ cells, as seen in Figure 3. This allows the application of a trigger algorithm that is seeded with the highest energy cell, combined with the next highest energy cell to define a $0.025 \times 0.2$ cluster core, with the neighbors added in $\eta, \phi$ to form the cluster. Further neighbors provide an environment for studying isolation and rejecting un-isolated objects. The effect of this improvement is studied in simulation and the result is shown in Figure 4 at luminosities expected in 2018.
Figure 2. Diagram of existing trigger towers.

The black points show a level-1 trigger based only on the $E_T$ of the cluster, in pink is the existing triggering method, well above the 20 kHz rate limit by 2018. The blue and red points show an isolation requirement applied using the increased granularity. With this increase in granularity an unprescaled level-1 trigger near an $E_T$ of 25 GeV is maintained.

Figure 3. Diagram of proposed super-cell with upgraded trigger electronics.

Figure 4. Simulation of the reduction in the rate for a given threshold at the level-1 trigger with high granularity input. Finer lateral and longitudinal segmentation of the EM shower shape for electrons and photons is used to reduce rates.

For the HL-LHC, planned for 2022, it will be necessary to upgrade all of the more than 1500 front end boards (FEBs), preparing the detector for the expected 3000 fb$^{-1}$. This complete replacement allows the design of a more flexible system that utilizes the full precision and granularity of the LAr calorimeters at trigger level. This simpler, “free running” architecture results in an effectively infinite pipeline and level-1 bandwidth with little or no impact on the latency. Technically, this requires 40 MSPS digitization for all channels over a 16 bit dynamic range within the existing power, cooling and space constraints in a radiation environment. Once digitized the data will be moved off each board at 100 Gbps, or 150 Tbps for the LAr calorimeters. With this the maximum granularity of the calorimeter is provided to the trigger.

3. Existing Electronics

The current readout electronics of the calorimeter are shown schematically in Figure 5. The analog signals from the detector are captured by the FEBS and are prepared for digitization by the preamplifier and shaper chips. Additionally the Layer Sum Boards (LSBs) combine the analog, cell-level signals into a single signal for each layer and send the analog sums to
the Tower Builder Board (TBB). The TBB combines the four layers into one tower which is
digitized, converted to transverse energy and sent to the level-1 calorimeter trigger. If the event
passes the trigger selection an accept signal is sent to the FEBS to digitize the full readout of
the calorimeter. The digital counts are then sent off detector, converted into energy and sent
to the DAQ system. Though adequate for the present data taking the system is limited by the
granularity of the signals sent to the level-1 trigger.

![Diagram of the calorimeter readout electronics](image)

**Figure 5.** Existing LAr calorimeter readout electronics.

4. **Upgrade Implementation Phase 1**
The upgrade foreseen for Phase 1 (2018) sends additional information to the level-1 trigger by
making a minimal change to the overall system and maintaining compatibility with the existing
trigger (Figure 6). Four layer sums (the middle two with higher granularity than the existing
readout) are sent to the new LAr Trigger Digitizer Board (LTDB) which digitizes these signals.
At the same time it combines the layer sums to provide the correct granularity input to the
existing TBB. The digital signals from the LTDB are sent to the off detector Digital Processing
System (DPS), which converts the digital signals to energy and timing information. The L1
calorimeter trigger system then receives information from LTDB and the TBB. These can be
used simultaneously during commissioning, eventually phasing out the TBB.

![Diagram of the proposed block diagram](image)

**Figure 6.** Proposed block diagram for Phase 1 electronics upgrade.

The construction of the LTDB and the DPS requires the development of several new
components. For the LTDB a radiation hard ADC and a serializer and optical link are necessary,
as well as the design of the high-speed off-detector FPGA-based DPS. For the LTDB the ADC must be capable of digitizing at 40 MSPS with 12 bit precision. This chip should consume less than 100 mW of power per channel and fit in a small footprint, send serialized output and be radiation tolerant to withstand $\sim 10^{14}$ hadrons/cm$^2$. The specification for the new FEBs in Phase 2 are similar and the same chip may be used for both boards. For Phase 2 there is the additional requirement of 16 bit precision which is achieved with the same 12 bit ADC and adding a gain selection. A test chip has been prepared using the IBM 8RF 130 nm technology. The test chip itself contains two pipeline channels each containing a four stage ADC with 1.5 bits/ stage, sample-and-hold and gain selection structures, and additional support structures. These four stages digitize the most significant bits with the remaining eight bits digitized by a commercial ADC. The additional half bit at each stage is used to determine and apply a digital error correction. Testing has been completed and the analog performance is found to be equivalent to a commercial 12 bit ADC. The cross talk between the two channels is found to be below the noise level and the device has been tested to be radiation tolerant to greater than 10 MRad and $2 \times 10^{14}$ protons/cm$^2$. Two test chips are being designed for submission in 2012/2013. The first is a four channel 12 bit ADC with the first four bits digitized as described above, and the last eight bits by a SAR ADC. The other is a new design for a two channel 12 bit SAR ADC which has the advantages of being low power and low latency.

The data are sent off detector using a radiation hard optical connection. A test chip has been built using CMOS 0.25 $\mu$m Silicon-on-Sapphire technology. Each optical link transfers data at $\sim 5$ Gbps. The data is multiplexed and serialized, reducing 16 parallel data streams to one serial output. The power dissipated is 460 mW and the radiation hardness has been tested. An 8 Gbps test chip has been submitted for fabrication.

The new LTDB signals require off-detector electronics to integrate with the level-1 calorimeter trigger system. The digitized high granularity layer sums will be calibrated and filtered to suppress pileup by the Digital Processing System (DPS). Each LDTB will send $\sim 200$ Gbps/board over optical links to the DPS which must process this large volume of data and send the resulting information to the trigger system. The DPS is an ACTA board that receives the high bandwidth optical signals on $4 \times 40 \times \sim 5$ Gbps links from LDTBs. Internally, high-end FPGAs each receive $40 \times \sim 5$ Gbps signals and apply digital filtering to convert raw ADC counts to calibrated energy and timing information. These data are sent to the new Feature EXtractor (FEX) in the level-1 calorimeter trigger system. Several FPGAs are being considered, including the Xilinx Virtex-7. This FPGA is being used to optimize the firmware for the energy calibration.

5. Upgrade Implementation Phase 2

As the existing FEBs come to the end of their expected operational lifetime in 2022 there will be an opportunity to switch to a fully digital architecture. The new FEBs will digitize continuously at the full precision. This will be read out to a new digital off detector system that will provide input for a fully digital level-1 trigger system. The LTDB and DPS from the Phase 1 upgrades may then be used for a new level-0 trigger. Schematically these changes can be seen in figure 7. Here all the channels are immediately digitized by the FEB, the TBB has been removed completely, and a new off detector Read Out Driver (ROD) provides the link to the level-1 trigger. Many of the new technologies that are being developed for Phase 1 will be applied in Phase 2.

One outstanding ASIC needed for the new FEB but not the LTDB is the preamplifier/shaper chip. This ASIC receives, shapes and amplitude adjusts the analog signals for digitization. This must be radiation tolerant with a dynamic range of 16 bits achieved in three stages (gains). A test chip has been prepared and the power consumption was measured with the preamplifier consuming less than 50 mW and the shaper less than 300 mW, with a maximum signal of 5 mA with an INL of 0.1%. A new test chip has been prepared using the IHP SiGe 25 H3P technology.
with 2 preamplifier blocks and 1× and 10× gain/shaper blocks.

Off detector the RODs will be replaced to handle 150 Tbps of data from the new detector readout (100 times more than the current system). This requires high speed data processing and transmission. The use of ATCA blades/boards is being planned, which will use high-end FPGAs to apply calibration for energy, time alignment, and provide data monitoring. This work overlaps extensively with the DPS design of Phase 1, which will form the core of the new RODs. The data output from the new RODs will send the full granularity of the calorimeter to trigger system, allowing for the most flexible trigger algorithms possible, and the same calibration is applied for both trigger and reconstruction. Complex algorithms such as the extraction of the features of electromagnetic shower shapes or fast tagging of π⁰ s may be possible.

6. Outlook
Over the last two years the current detector and readout have performed exceptionally well, resulting in exceptional physics. Over 98% of 182k channels are operational [2]. However, for 2018 an upgrade is needed in order to maintain the sensitivity to physics measurements at luminosities beyond 10^{34} cm^{-2}s^{-1}. The upgrades will happen in two stages: Phase 1 and Phase 2. In Phase 1 the trigger path will be upgraded. Test devices have been produced and have been shown to meet the required specifications. Phase 2 will be a full upgrade of on- and off-detector electronics and the level-1 trigger to a completely digital system. All signals from the LAr will be digitized at the beam crossing rate. This requires the design of a system for digitizing and moving the data, while fitting into existing power, cooling, and space requirements in a radiation environment. In the near term a Phase “0” quarter size demonstration board is planned and organization of the Phase 1 construction, testing, installation and commissioning is underway. The last year has witnessed the excellent performance of the LHC and ATLAS. With this success now in the past, the LAr readout and trigger systems are being preparing for highest LHC luminosities and interesting physics at the HL-LHC.

References
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