Vector Symbolic Architectures as a Computing Framework for Nanoscale Hardware

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Abstract—This article reviews recent progress in the development of the computing framework Vector Symbolic Architectures (also known as Hyperdimensional Computing). This framework is well suited for implementation in stochastic, nanoscale hardware and it naturally expresses the types of cognitive operations required for Artificial Intelligence (AI). We demonstrate in this article that the ring-like algebraic structure of Vector Symbolic Architectures offers simple but powerful operations on high-dimensional vectors that can support all data structures and manipulations relevant in modern computing. In addition, we illustrate the distinguishing feature of Vector Symbolic Architectures, “computing in superposition,” which sets it apart from conventional computing. This latter property opens the door to efficient solutions to the difficult combinatorial search problems inherent in AI applications. Vector Symbolic Architectures are Turing complete, as we show, and we see them acting as a framework for computing with distributed representations in myriad AI settings. This paper serves as a reference for computer architects by illustrating techniques and philosophy of VSAs for distributed computing and relevance to emerging computing hardware, such as neuromorphic computing.

Index Terms—computing framework, hyperdimensional computing, vector symbolic architectures, nanoscale hardware, distributed representations, data structures, Turing completeness, computing in superposition

I. INTRODUCTION

The demands of computation are changing. First, Artificial Intelligence (AI) and other novel applications pose a host of computing problems that require search over an immense space of possible solutions, with many approximately correct but rarely one correct answer. Second, future nanoscale hardware platforms, operating at ultra-low voltages to reduce energy consumption and to support continued process scaling, are destined to be noisy and, hence, operate stochastically [Jaeger, 2020]. These observations expose the need for a computing framework that supports both deterministic computation in the presence of noise as well as the approximate and parallel nature of algorithms for AI.

By nanoscale hardware, we refer to the broad class of new hardware designs that are highly parallel, fabricated at ultra-small scales, utilize novel components, and/or operate at ultra-low voltages, thus consisting of unreliable, stochastic computational elements.

The conventional (à la von Neumann) computing architecture is not well adapted to these demands, as it was designed assuming precise computational elements and for tasks that require exact answers. Conventional computing architectures will continue to play an important role in technology, but there is a growing portion of computational demands that are better served by new computing designs. Thus, hardware engineers have been looking towards distributed and neuromorphic computing as a way to meet these demands.

Many of the emerging computational demands are from cognitive or perceptual applications found within the realm of AI, such as image recognition, computer vision, and text analysis. Indeed, large-scale deep learning neural network modeling dominates discussions about modern computing technology, pushing innovations in hardware design towards parallel, distributed processing [Ben-Nun and Hoefler, 2019]. While widely used, deep learning neural networks still have limitations, such as the transparency of learned representations and the difficulties in performing symbolic computations. In order to support more sophisticated symbolic computations, researchers have been embedding conventional data structures, such as graphs and key-value pairs, into neural network models [Kipf and Welling, 2017], [Scarselli et al., 2008], [Vaswani et al., 2017]. However, it is not yet clear whether the sub-symbolic pattern recognition and learning capabilities...
of deep neural networks can be augmented to handle the rich control flow, abstraction, symbol manipulation, and recursion of existing computing frameworks.

Work on developing nanoscale computing hardware is accelerating. There are many show-case demonstrations [Lin et al., 2018], [Pei et al., 2019], [Imam and Cleland, 2020], [Davies et al., 2021] but so far:

- these demonstrations have mostly lacked a unifying theoretical framework that can bring sufficient composability, explainability, and versatilty;
- many demonstrations still depend on hand-crafted elements that would be brittle to errors;
- most of the demonstrations have been sub-symbolic in nature and resort to support from the conventional computing architecture to implement the symbolic and flow control elements.

While these points are valid in general there are some exceptions, which we discuss in Section V-E. Nevertheless, all of these motivate the need a unifying computing framework that can serve as an abstraction layer between hardware and desired functionality. Ideally, such a framework should be flexible enough to provide interfaces to nanoscale hardware with various features, such as stochastic components, asynchronous spiking communication, or devices with analog elements.

For the following reasons, we propose Vector Symbolic Architectures (VSA) [Gayler, 2003] or, synonymously, Hyperdimensional Computing [Kanerva, 2009] as such a computing framework. First, VSAs can represent and manipulate both symbolic and numerical data structures in a distributed vector space, to solve, e.g., cognitive [Eliasmith et al., 2012], [Rachkovskij and Slipchenko, 2012], [Emruli et al., 2013] or machine learning [Ge and Parhi, 2020] tasks. VSAs are a suitable framework for integration with neural network computing for solving problems in AI and extends beyond typical AI tasks as an approach capable of performing symbolic manipulations with distributed representations. Second, the design of VSAs, which was inspired by the brain, lends itself to implementation in nanoscale computing technologies [Karunaratne et al., 2020] because it is highly robust to individual device variations. Third, VSA is a framework with two interfaces, one towards computation and algorithms and one towards implementation and representation (cf. Fig. 1). There are different VSA models that all offer the same operation primitives but differ slightly in terms of their implementation of these primitives. For example, there are VSA models that compute with binary, bipolar, continuous real, and continuous complex vectors. Thus, the VSA concept has the flexibility to connect to a multitude of different hardware types, such as binary values for analog in-memory computing architectures [Karunaratne et al., 2020] or complex-valued VSAs for spiking neuron architectures [Frady and Sommer, 2019].

This article provides three main contributions. First, we review the principles of VSAs and how they provide a generic computing framework for implementing the primitives of conventional data structures and deterministic algorithms. Second, we highlight pros and cons of a non-traditional mode of computing in VSA, “computing in superposition,” which can leverage distributed representations and parallelism for efficiently solving computationally hard problems. Finally, we demonstrate the universality of VSAs by using them to represent a system known to be Turing complete (see Appendix A for the details of two proposals).

**Guide to the article**

The article is written with both newcomers to VSAs and seasoned readers in mind. Section II provides motivation for using VSAs in the context of nanoscale computing hardware. This section sets up the context for the article. Section III offers a deep dive into the fundamentals of VSAs, recommended primarily to readers not yet familiar with the framework. Section IV explains different aspects of computing with VSAs, including a survey of the representation primitives for numerous data structures (Section IV-A), possible realizations of VSA models in different types of hardware (Section IV-B), and a tutorial on computing in superposition (Section IV-C). Section V provides discussion and covers related work. Finally, Appendix A describes two proposals for demonstrating the universality of VSAs.

**II. Motivation**

The exponential growth of Big Data and AI applications exposes fundamental limitations of the conventional computing framework. One problem is that energy efficiency is stagnating [Andrae and Edler, 2015] – training and fine-tuning a neural network for a Natural Language Processing application consumes energy and computational resources equivalent to several hundred thousand US dollars [Strubell et al., 2019] or more [Rogers, 2019]. Conventional computing hardware is also highly susceptible to errors and energy is wasted attempting to maintain low error rates.

Data-intensive applications illustrate the scale of the problem and make energy efficiency the grand challenge of computer engineering. To solve this challenge, alternative hardware is required that can work with imprecise and unreliable computational elements [Jaeger, 2020]. Operating at ultra-low voltages with stochastic devices that are prone to errors has the potential to greatly increase computing power and efficiency.

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**Fig. 1.** The place of VSA within Marr’s levels of analysis [Marr, 1982]. The focus of this article is marked by the dashed rectangle. We explain how VSA provides primitives to formalize algorithms in ways that seamlessly connect to the computational and implementational levels in the computing hierarchy.
For example, the recent advances in materials science as well as in device manufacturing make it possible to design computing hardware which accommodates computational principles of biological brains or exploits physical properties of the substrate material. For certain classes of problems, computing hardware such as neuromorphic processors [Merolla et al., 2014], [Davies et al., 2018], [Frady et al., 2020c] and in-memory computing architectures [Karunaratne et al., 2020] consume only a fraction of the energy compared to current technology. For certain tasks, existing neuromorphic platforms can be 1,000 times more energy efficient [Davies et al., 2018] than the conventional ones.

There is a current focus on implementing AI capabilities in nanoscale computing hardware [Frady et al., 2020c], with the aim of providing energy-efficient implementation of a selected class of AI functionality (mainly neural networks). However, we see the opportunity for a computational framework exceeding neural networks in scope that could empower an unprecedented breakthrough in nanoscale computing technology. First, while neural network algorithms serve a rather small subset of computation problems extremely well, they cannot address a large class of problems that require conventional algorithms and data structures. A computing framework with a broader application scope than neural networks could boost the adoption of nanoscale computing by orders of magnitude. Second, despite many promising applications for nanoscale computing hardware, the programming of any new functionality is far from trivial. Nanoscale computing hardware currently lacks a holistic software architecture, which would streamline the development of the new functionality. Current development strategies resemble that of assembly programming, where the developer is left with the entire job from coming up with the algorithmic idea to designing the actual machine instructions to be executed by a central processing unit. Thus, the impressive recent nanoscale hardware development [Karunaratne et al., 2020], [Li et al., 2016] needs to be complemented with the creation of computing frameworks for such hardware that can abstract and simplify the implementation of new functionalities, including the design of programs. Last but not least, most nanoscale hardware differs fundamentally from traditional computer and neural network accelerator hardware in that the enabled computations are unreliable and stochastic. Thus, a computing framework is required in which error correction and error robustness are achieved.

There is ample work demonstrating that VSA possesses a rich computational expressiveness, from the functionality of neural networks [Kleyko et al., 2019], [Kleyko et al., 2020a], [Kleyko et al., 2020], [Frady et al., 2018b] to machine learning tasks [Recchia et al., 2015], [Rasanen and Saarinen, 2016], [Kleyko et al., 2018b], [Rahimi et al., 2019] and cognitive modeling [Slipchenko and Rachkovskij, 2009], [Rachkovskij et al., 2013], [Eliasmith, 2013], [Rachkovskij and Slipchenko, 2012], [Emruli et al., 2013], [Kleyko et al., 2015]. Further, VSA can express conventional algorithms, for example, finite state automata [Osipov et al., 2017], [Yerxa et al., 2018] and context-free grammars [beim Graben et al., 2020].

In this article, we explore whether VSA can serve as a computing framework for bringing nanoscale computing to the next level. We argue that VSAs provide a framework to formalize and modularize algorithms and, at the same time, bridge the computation and implementation levels in Marr’s framework [Marr, 1982] for information processing systems (see Fig. 1). Our proposal generalizes earlier suggestions to apply VSA for implementing specific machine learning algorithms on nanoscale hardware [Rahimi et al., 2017], [Kanerva, 2019].

III. FUNDAMENTALS OF VSA

VSA [Gayler, 2003] is a family of models for representing and manipulating data in a high-dimensional space. It was originally proposed in cognitive psychology and cognitive neuroscience as a connectionist model for symbolic reasoning [Plate, 1994b]. In VSA, information is represented by vectors of high (but fixed) dimension $N$, sometimes called hypervectors or HD vectors. Symbols are represented by hypervectors in such a way that the encoded information is distributed across all components of a hypervector. Such distributed representations [Hinton et al., 1986] are distinct from localist and semi-localist representations [Thorpe, 2003], where single or subsets of components encode separate individual features.

Distributed representations are, in and of themselves, not the full story. As argued by [Fodor and Pylyshyn, 1988], distributed representations must be productive and systematic. Productivity refers to massive expressiveness generated by simple primitives while systematicity means that representations are sensitive to the structure of the encoded objects. These desiderata were one of the drivers for developing VSA. A major advantage of VSA as the algorithmic level in the Marr hierarchy (Fig. 1) is that it embraces distributed representations, which are robust to local noise.

The idea of computing with random hypervectors as basic objects rather than Boolean or numeric scalars has been developed by Kussul as Associative-Projective Neural Networks [Kussul and Rachkovskij, 1991], [Kussul et al., 1991a], [Kussul et al., 1991b] and independently in seminal work of Plate on Holographic Reduced Representation [Plate, 1994a]. VSA can be formulated with different types of vectors, namely those containing real, complex, or binary entries, as well as with the multivectors of geometric algebra. These flavors of VSA come under many different names: Holographic Reduced Representation (HRR) [Plate, 1995a], [Plate, 2003], Multiply-Add-Permute (MAP) [Gayler, 1998], Binary Spatter Codes [Kanerva, 1997], Sparse Binary Distributed Representations (SBDR) [Rachkovskij and Kussul, 2001], [Rachkovskij, 2001], Sparse Block-Codes [Laiho et al., 2015], [Frady et al., 2020b], Matrix Binding of Additive Terms (MBAT) [Gallant and Okaywe, 2013], Geometric Analogue of Holographic Reduced Representation (GAHRR) [Aerts et al., 2009], etc. All of these different models have similar computational properties – see [Frady et al., 2018b] and [Schlegel et al., 2020]. For clarity, we will use the Multiply-Add-Permute model in the remainder of this article.
A. Basic elements of VSA

1) High-dimensional space: VSA requires a high-dimensional space. The appropriate choice of dimensionality $N$ is somewhat dependent on the problem, but there are simple rules of thumb ($N > 1,000$, for example), and much more important is the representation of particular data structures in the given problem. As mentioned above, there are VSA models defined for different types of spaces (see Section IV-B for more details). Operations and properties that have proven useful are presented below (Appendix B provides the summary). It is worth pointing out here that VSA operations on hypervectors (Section III-B) go well beyond what a traditional “vector space” specifies (a vector addition operation, a scalar multiplication operation and 8 related axioms). Namely, we include a multiplication operation between two vectors and a complementary permutation operation. For VSAs that use thresholding, vector addition is not even precisely linear. While VSAs will sometimes leverage linear operations on vectors, our reference to a “space of vectors” is not in the strict linear algebra sense, but to something far richer.

2) Pseudo-orthogonality: By using random vectors as representations, VSAs can exploit the concentration of measure phenomenon [Ledoux, 2001], [Gorban and Tyukin, 2018], which implies that random vectors become almost orthogonal in high-dimensional vector spaces. This phenomenon, also sometimes called progressive precision [Alaghi and Hayes, 2018] or the blessing of dimensionality [Gorban and Tyukin, 2018], ensures that the representations of different objects are automatically dissimilar. In the VSA literature, dissimilar representations are described by various adjectives such as unrelated, uncorrelated, approximately- or pseudo-orthogonal. Unlike with exact orthogonality, the dimension $N$ is not a hard limit on the number of pseudo-orthogonal vectors one can create.

3) Similarity measure: Reasoning in VSA is based on similarity between hypervectors. The common similarity measures in VSA are the dot (scalar, inner) product, cosine similarity, overlap, and Hamming distance. Here we use the dot product (denoted as $\langle \cdot, \cdot \rangle$) as the similarity measure. It is worth pointing out here that VSA operations on hypervectors go well beyond what a traditional “vector space” specifies (a vector addition operation, a scalar multiplication operation and 8 related axioms). Namely, we include a multiplication operation between two vectors and a complementary permutation operation. For VSAs that use thresholding, vector addition is not even precisely linear. While VSAs will sometimes leverage linear operations on vectors, our reference to a “space of vectors” is not in the strict linear algebra sense, but to something far richer.

4) Seed hypervectors: When designing a VSA algorithm for solving a problem, it is common to define a set of the most basic concepts/symbols for the given problem and assign hypervectors to them. Such seed hypervectors are defined as the representations of concepts that are irreducible. All other hypervectors occurring in the course of a computation are therefore reducible, that is, they are composed from seed hypervectors. Here we will focus on symbolic structures, i.e., symbols from some alphabet with size $D$, which are represented by seed hypervectors. The process of assigning seed hypervectors, usually (but not always) by i.i.d. random generation of vectors, is referred to as mapping, encoding, projection, or embedding. We reiterate that representations in a VSA algorithm need not always be pseudo-orthogonal. For example, for representing real-valued variables one might use a locality-preserving representation scheme, in which representations of similar values are systematically correlated and not pseudo-orthogonal [Rachkovskij et al., 2005], [Weiss et al., 2016], [Komer et al., 2019], or where the hypervectors are learned [Recchia et al., 2015], [Sutor et al., 2018]. Thus, one should keep in mind that i.i.d. randomness is not the only tool for designing seed representations.

5) Item memory: Seed hypervectors are stored in the so-called item memory (or clean-up memory), a content-addressable memory which can be just a matrix or an associative memory [Gritsenko et al., 2017] that stores the hypervectors as point attractors.

B. VSA operations and compound representations

Seed hypervectors are the building blocks for compound VSA representations, which are built up from operations performed on the seed vectors. For example, a compound hypervisor representing edges of a graph (compound entity) can be constructed (Section IV-A7) from seed hypervectors representing its nodes (basis symbols). This compositional formation of data structures in VSA is akin to conventional computing and very different from the modern neural networks in which activity vectors, especially in hidden layers, often can not be readily parsed.

Two key VSA operations are dyadic vector operations between hypervectors that are referred to as addition and multiplication. Like the operations between ordinary numbers with the same name, they form, together with the representation vector space, a ring-like algebraic structure. Another important VSA operation is permutation of the components within a hypervisor.

The addition operation is also called “bundling” or “superposition”, and the multiplication operation is also called “binding”. In the Multiply-Add-Permute model, the binding operation is literally implemented via component-wise multiplication, the Hadamard product. The permutation operation is often a rotation of components, i.e., a cyclic shift of the vector component index.

In what follows, we describe each operation and its properties in further details. Note that the hypervectors referred to in this section are pseudo-random i.i.d. Because high-dimensional representation tolerates errors, the conditions listed below need only be satisfied approximately or with high probability. By the concentration of measure phenomenon, the operations – and computations based on them – become ever more reliable, dependable, and predictable as the dimensionality $N$ of the space increases.

1) Multiplication: a dyadic operation mapping two hypervectors to another hypervisor. It is used to represent the object formed by the binding of two other objects. This operation is an important ingredient for forming compositional structures with distributed representations (see, e.g., discussion on its importance in the context of deep learning in [Greff et al., 2020]). For two symbols $a$ and $b$, represented by the hypervectors $a$ and $b$, the hypervisor that represents the bound object (denoted by $m$) is:

$$m = a \odot b.$$  
(1)

In the Multiply-Add-Permute model $\odot$ denotes the component-wise multiplication (Hadamard product). Multiple
application of multiplication is denoted as $\prod$, enabling one to form a hypervector representing the product of more than two vectors.

Consider the example of representing a database for trivia about countries [Kanerva, 2010]. The database record for a country contains the name, the capital, and the currency. The first step is to form hypervectors that represent key-value pairs, which can be done by multiplication: $\text{country} \odot \text{USA, capital} \odot \text{Washington, currency} \odot \text{USD}$. To create a single hypervector that represents the entire data record for a country, we need another operation to combine the different key-value pairs (see below).

2) **Addition**: a dyadic operation mapping two hypervectors to another hypervector. It is denoted with $+$ and implemented via component-wise addition, which sometimes can be thresholded or normalized. The addition operation combines several hypervectors into a single hypervector. For example, for $a$ and $b$ the result $z$ of addition of their hypervectors is simply:

$$z = a + b. \quad (2)$$

The addition of more than two hypervectors is denoted by $\sum$. Often, addition is followed by a thresholding or normalization operation to produce a resultant hypervector which is of the same type as the seed vectors. For example, in the Multiply-Add-Permute model the seed hypervectors are bipolar vectors, but the arithmetic sum-vector is not. A thresholding operation, using the signs in each component, can map the sum vector back to a bipolar hypervector. This type of thresholding is sometimes called the majority rule/sum and denoted by brackets: $[a + b]$. Most of the examples below use the non-thresholded sum, unless mentioned otherwise. The non-thresholded sum has the advantage that individual components in the sum can be removed by subtraction without interfering with the rest.

Continuing the database example, the addition operation can be used to create a single hypervector from hypervectors representing all key-value pairs of the record. Thus, the compound hypervector for the whole record will be formed as: $\text{country} \odot \text{USA} + \text{capital} \odot \text{Washington} + \text{currency} \odot \text{USD}$.

3) **Permutation**: a unary operation on a hypervector that yields a hypervector. Akin to the multiplication operation, permutation is often used to map into an area of hypervector space that does not interfere with other representations. However, unlike multiplication, the same permutation can be used recursively, with every iteration projecting into previously unoccupied territory. Obviously, permutations with long cycle length are most efficient in doing this; the cycle length is how often a permutation can be recursively applied before it becomes the identity operation. It turns out that most permutations, in particular, random permutations have, on average, quite long cycle lengths [Golomb, 1964], and are adequate for this purpose. Note that the number of possible permutations grows super exponentially with the dimensionality ($N!$) and that permutations themselves are not elements of the space of representations, which prevents simple dynamic manipulation of a permutation in the course of computations. In most VSA algorithms, one or a small set of permutations are fixed at the onset of computation. We continue with a simple example and more examples follow in the subsequent sections.

Permutation can be seen as an alternative approach to multiplication when there is only one hypervector as the operand [Rachkovskij, 2001], [Gayler, 1998]. The permutation operation can also be used to represent sequence relations and other asymmetric relations like “part-of”. For example, a fixed permutation (denoted as $\rho$) can be used to associate a symbol hypervector with the position of a symbol in a sequence, resultant in a hypervector representing the symbol in that position. The single application of the permutation is:

$$r = \rho(a). \quad (3)$$

To associate $a$ with the $i$-th position in a sequence, the permutation is applied $i$ times. The result is the hypervector $\rho^i(a)$.

Note, that permutation is an example of a more general unary operation, matrix vector multiplications.

4) **Properties of VSA operations and their interaction**: Here we summarize the properties of the basic VSA operations and how they interact:

a) **Addition**:

- Addition can be inverted with subtraction: $a + b + c - c = a + b$.
- In contrast to the multiplication and permutation operations, the result of addition $z = a + b$ (often called the superposition hypervector) is similar to each of its argument hypervectors, i.e., the dot product between $z$ and $a$ or $b$ is significantly more than 0, $(z,a) \approx (z,b) > 0$.
- Arguments of addition can be approximately recovered from the superposition hypervector: $b \odot (a \odot b + c \odot d) \approx a$.
- Addition is commutative, $a + b = b + a$.
- Normalized addition is approximately associative: $[a + b + c] \approx [a + [b + c]]$.

Note that if several instances of any hypervector are included (e.g., $z = 3a + b$), the resultant hypervector is more similar to the dominating hypervector than to other arguments.

b) **Multiplication**:

- Multiplication is commutative, $a \odot b = b \odot a$.
- Multiplication distributes over addition, $c \odot (a + b) = (c \odot a) + (c \odot b)$.
- Multiplication is invertible, for $m = a \odot b$, $a \odot m = b$. The inversion process is often called releasing or unbinding. In the case of the component-wise multiplication, the unbinding operation is performed with the same operation since bipolar vectors are self-invertible.
- Multiplication is associative, $c \odot (a \odot b) = (c \odot a) \odot b$.
- The result of multiplication is dissimilar to each of its argument hypervectors, e.g., $m$ is dissimilar to the hypervectors being multiplied, i.e., the dot product between $m$ and $a$ or $b$ is approximately 0, $(m,a) \approx (m,b) \approx 0$.
- Multiplication preserves similarity (for similar $a$ and $a'$): $(a \odot b, a' \odot b) > 0$.
- Multiplication is a “randomizing” operation (since $(a \odot b, a) \approx 0$) that preserves similarity (because $(a \odot b, c \odot b) = (a, c)$).
c) **Permutation:**

- Permutation is invertible, for \( r = \rho(a) \): \( a = \rho^{-1}(r) \);
- In Multiply-Add-Permute, permutation distributes over both multiplication \( (\rho(a \odot b) = \rho(a) \odot \rho(b)) \) and addition \( (\rho(a + b) = \rho(a) + \rho(b)) \);
- Similar to the multiplication operation, the result of a (random) permutation \( r \) is dissimilar to the argument hypervector \( a \): \( (r, a) \approx 0 \);
- Permutation is “randomizing” operation (since \( \langle \rho(a), a \rangle \approx 0 \) that preserves similarity (because \( \langle \rho(a), \rho(b) \rangle = \langle a, b \rangle \)).

It is worth emphasizing what we mean in the above by “similarity preserving” in the case of multiplication and permutation vs. addition: For multiplication, the similarity between two hypervectors is the same before and after multiplying with a third hypervector, i.e., \( (a \odot b) \odot c = (a \odot c) \odot b \), and for permutation the similarity between two hypervectors is also the same before and after the operation, i.e., \( \langle \rho(a), \rho(b) \rangle = \langle a, b \rangle \).

However, for addition, the similarity between two hypervectors is generally lower before vs. after adding them to a third hypervector, i.e., \( (a + b) + c \neq a + (b + c) \), since the sum moves them in a common direction, \( b \). On the other hand, since the superposition hypervector is similar to each of the vectors in the sum, \( (a + b, a) \approx (a + b, b) > 0 \), it is also sometimes referred to as “similarity preserving,” in contrast to multiplication and permutation, which generally create a very dissimilar hypervector. One should keep this distinction in mind when referring to the similarity preserving properties of these operators.

### C. Parsing compound representations

VSAs offer the possibility to encode data structures into compound hypervectors and to manipulate the hypervectors with the operations described above as a way to perform computation on the data structures. In the conventional computing, data structures are always exposed and the algorithm queries or modifies individual elements within them. In contrast, the vector operations in VSA can search or transform in parallel many or all elements of a data structure, which we call “computing in superposition” (see Section IV-C). All data structures are hypervectors and can be manipulated immediately and in parallel, regardless of how complicated a structure they possess. But this also means that the data structure of a compound hypervector is not immediately decodable from the item memory. To query element(s) of a compound hypervector, it first needs to be analyzed or “parsed”. We borrow the term parsing from linguistics because the parsing of VSA hypervectors is somewhat similar. To understand a sentence, one needs to analyze the sentence into its parts and assign their syntactic roles, which involves comparing the parts with stored information about their meaning and syntactic roles. Similarly, to extract the result of a VSA computation, one has to parse the resultant hypervector. The parsing of VSA hypervectors involves decomposition and comparison of the resulting parts with stored information.

Like with the sum or product of ordinary numbers, the parsing of hypervectors requires additional information, such as the operations used to form the compound representation and the set of seed vectors. Parsing a compound hypervector first involves the inverse operation to that used to encode the wanted element in the data structure. However, the result is almost always approximate because of crosstalk noise coming from all the other elements in the compound hypervector. To single out the correct result, the noisy vector has to be compared to the original seed vectors in terms of similarity. Probing is the process of retrieving the best-matching hypervector (i.e., the nearest neighbor) among the hypervectors for a given query hypervector. This is done in the item memory, which contains all the seed hypervectors. For example, consider the compound hypervector:

\[
\mathbf{s} = \mathbf{a} \odot \mathbf{b} + \mathbf{c} \odot \mathbf{d}.
\]

In order to know which hypervector has been bound to, e.g., \( \mathbf{b} \) we have to unbind (inverse multiply) \( \mathbf{b} \) from \( \mathbf{s} \):

\[
\mathbf{s} \odot \mathbf{b} = \mathbf{b} \odot (\mathbf{a} \odot \mathbf{b} + \mathbf{c} \odot \mathbf{d}) = \mathbf{a} + \mathbf{b} \odot \mathbf{c} \odot \mathbf{d} = \mathbf{a} + \text{noise} \approx \mathbf{a}.
\]

The resultant hypervector contains the correct answer \( \mathbf{a} \) and a crosstalk noise term \( \mathbf{b} \odot \mathbf{c} \odot \mathbf{d} \), which is dissimilar to any of the items in the item memory. The query hypervector \( \mathbf{a} + \text{noise} \) will be highly similar to the hypervector \( \mathbf{a} \) stored in the item memory, which will be successfully retrieved by the nearest neighbor search with high probability. Thus, the probing operation removes (or cleans-up) the noise and returns the correct result.

Clean-up via probing is a critical part of VSA computations, which has the advantage that its operation is intrinsically noise resilient and the degree of noise robustness can be easily controlled by the dimension \( N \). In essence, probing is a signal detection problem. The number of hypervectors that can be correctly retrieved from the superposition is called capacity. The capacity increases roughly linearly with the hypervector dimension and is quite insensitive to the details of a particular VSA model. The signal detection theory for VSA [Frady et al., 2018a], [Kent et al., 2020], which addresses this problem by a parallel search in the space of all possible combinations. The resonator network assumes that none of the arguments are given, but that they are contained in different item memo-
The hypervector illustrates an example of a resonator network for factoring riesz, which should be known to the resonator network. Fig. 2 illustrates an example of a resonator network for factoring a compound hypervector \( s = a \odot b \odot c \). A, B, and C denote the corresponding item memories containing seed hypervectors for a, b, and c arguments, respectively.

Fig. 2. An example of a resonator network with three arguments, which is factoring a compound hypervector \( s = a \odot b \odot c \). A, B, and C denote the corresponding item memories containing seed hypervectors for a, b, and c arguments, respectively.

To do so it uses hypervectors \( \hat{a}(t), \hat{b}(t), \hat{c}(t) \), each storing the prediction for a particular argument of the product forming \( s \). Each prediction communicates with the input hypervector \( s \) and all other predictions using the following dynamics:

\[
\begin{align*}
\hat{a}(t + 1) &= \text{sign}(A^T(s \odot \hat{b}(t) \odot \hat{c}(t))) \\
\hat{b}(t + 1) &= \text{sign}(B^T(s \odot \hat{a}(t) \odot \hat{c}(t))) \\
\hat{c}(t + 1) &= \text{sign}(C^T(s \odot \hat{a}(t) \odot \hat{b}(t))),
\end{align*}
\]

where \( A, B, \) and \( C \) denote the corresponding item memories containing \( a, b, \) and \( c \) arguments, respectively; \( \text{sign}(\cdot) \) denotes a step which projects the predictions back to the bipolar values. Note that these item memories will contain other hypervectors too but hypervectors stored in \( A, B, \) and \( C \) differ from each other. The size of each item memory depends on a task but it will affect the performance of the resonator network as larger item memories imply bigger search space.

The key insight into the internals of the resonator network is that it iteratively tries to improve its current predictions of the arguments constituting the input hypervector \( s \). In essence, at time \( t \) each prediction might hold multiple weighted guesses from the corresponding item memory. The current predictions for other arguments are used to invert the input vector and infer the current argument (e.g., \( s \odot \hat{b}(t) \odot \hat{c}(t) \)). The cost of using the superposition for storing the predictions is a crosstalk noise. To clean-up this noise, the predictions are projected back to their item memories (e.g., \( A^T(s \odot \hat{b}(t) \odot \hat{c}(t)) \)), which provides weights for different seed hypervectors stored in the item memory and, thus, constrains the predictions only to the valid entries in the item memory. These weights are then used to form a new prediction, which is a weighted superposition of all seed hypervectors. Successive iterations of the process in (4) eliminate the noise as the arguments become identified and find their place in the input vector. Once the arguments are fully identified, the resonator network reaches a stable equilibrium and the arguments can be read. For the sake of space, here we do not go into the details of applying resonator networks. Please refer to [Frady et al., 2020a] for examples of factoring hypervectors of data structures with it and to [Kent et al., 2020] for its comparison with other standard optimization-based methods.

D. Generality and utility

Currently, there are several known areas where VSA were exploited. Hypervectors serve as representations for cognitive architectures [Rachkovskij et al., 2013], [Eliasmith, 2013]. They are used for approximation of conventional data structures [Osipov et al., 2017], [Yerxa et al., 2018], [Kleyko et al., 2020], distributed systems [Simkin et al., 2019], [Rosato et al., 2021], communications [Jakimovski et al., 2012], [Kleyko et al., 2012], [Kim, 2018], for forming representations in natural language processing applications [Recchia et al., 2015], [Joshi et al., 2016] and robotics [Levy et al., 2013], [Neubert et al., 2019], [Mitrokhin et al., 2019], [Kleyko et al., 2020b], [Hersche et al., 2020]. The fact that it is possible to map real-valued data to hypervectors allows one to apply VSAs in machine learning domains. Most of these works have been done for classification tasks (see a recent overview in [Ge and Parhi, 2020]). Examples of domains that have benefited from the application of VSA modeling are biomedical signal processing [Rahimi et al., 2019], [Kleyko et al., 2019b], gesture recognition [Rahimi et al., 2016a], [Kleyko et al., 2018b], seizure onset detection and localization [Burrello et al., 2020], physical activity recognition [Rasansen and Kakouros, 2014], and fault isolation [Kleyko et al., 2018a] but VSA modeling can be useful for very generic classification tasks [Kleyko et al., 2020], [Diao et al., 2021]. The common feature of these works is a simple training process, which does not require the use of iterative optimization methods, and transparently learns with few training examples.

IV. COMPUTING WITH VSAS

A. Computational primitives formalized in VSA

In the previous section, we have introduced the basic elements of VSA. To provide the algorithmic level in the Marr computing hierarchy in Fig. 1, one needs to combine elements of VSA into primitives of VSA computing, i.e., something akin to design patterns in software engineering. For instance, a set of VSA templates has been proposed for tasks in the domain of personalized devices covering different multivariate modalities such as electromyography, electroencephalography, or electrocorticography [Rahimi et al., 2019]. Here we summarize best practices for representing well-known data structures with VSAs – this section can be thought of as a “VSA cookbook”. All examples in this section are available in an interactive Jupyter Notebook. After providing some basic rules for representing data structures with VSA, we present a

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1https://github.com/denkle/HDC-VSA_cookbook_tutorial
collection of primitives from prior work that has been done along these lines.

It is worth noting that in this article we do not cover the representation of real-valued data (see, e.g., [Rachkovskij et al., 2005], [Widdows and Cohen, 2015]) or solving machine learning problems (see, e.g., [Ge and Parhi, 2020]) as it has been covered elsewhere and is outside the immediate scope of the article.

1) The rules of thumb: We should point out that the VSA implementations we describe are not the only possibilities and other solutions may be possible/desirable in a particular design context. The solutions provided are, however, the most common/obvious choices, based on several “rules of thumb”:

- Addition is used to combine individual elements of a data structure into a set;
- Multiplication is used to make associations between elements, e.g., key-value pairs;
- Permutation is used for tagging data elements to put them into a sequential order, such as in time series;
- Permutation is used for protection from the self-inverse property of the multiplication operation since the hypervector will not cancel out when multiplied with its permuted version.

We will follow these rules most of the time when forming hypervectors for different data structures.

2) Sets: A set (denoted as $S$) represents a group of elements, for example, $S = \{a, b, c, d, e\}$. In order to map a set to a hypervector, two steps are required. First, an item memory storing random hypervectors for each element of a set (e.g., $a$ for “a”) is initialized. Second, a single hypervector (denoted as $s$) is formed that represents the set as the superposition of hypervectors for the set’s elements, e.g., for the set above:

$$s = a + b + c + d + e,$$

$$s = \sum_{S(i) = i} i.$$  \hspace{1cm} (5)

The hypervector $s$ is a distributed representation of the set $S$. This mapping preserves the overlap between elements of the sets. For example, set membership can be tested by calculating the similarity between $s$ and a hypervector corresponding to the element of interest. If the similarity score is higher than that expected between two random hypervectors, then most likely the element is present in the set. This mapping is very similar to a Bloom Filter [Bloom, 1970], [Tarkoma et al., 2012], which is a well-known randomized data structure for approximate membership query in a set. Bloom Filters have been recently shown to be a subclass of VSA [Kleyko et al., 2020], where the addition operation is implemented via OR and seed hypervectors are sparse, as in the Sparse Binary Distributed Representations [Rachkovskij and Kussul, 2001] model.

Note that the described mapping of sets does not have an exact way of obtaining distributed representations of the intersection or union of two sets, but there are simple approximations of both. Both approximations are obtained by the addition operation on the corresponding hypervectors. The difference is in the way the parsing step, which involves the item memory and a detection threshold, is done. In order to parse the intersection of two sets, only the elements with the largest dot products should be retrieved. To retrieve the union, the elements with the dot products sufficiently different from the noise level should be considered. In other words, the subtlety for the intersection is that elements present in both sets will have higher similarity then the ones present in only one of the sets (see Section III-B2). This property of the addition operation is in fact used in the next section for representing multisets.

3) Multisets/Histograms/Frequency distributions: Let us consider how to form a single hypervector of a multiset or a frequency distribution in the form of counts of the occurrences of various elements in some source. The mapping is essentially the same as in the case of sets in Section IV-A2 with the only difference that a hypervector of an element can be present in the result of the addition operation several times. For example, given $S = \{a, a, a, b, b, c\}$, hypervector representing the frequency of elements is formed as:

$$s = a + a + a + b + b + c = 3a + 2b + c.$$

Thus, the number of times a hypervector is present in the superposition determines the frequency of the corresponding element in the sequence. Using $s$ it is possible to estimate either the frequency of an individual element or compare to the frequency distribution of another sequence. Both operations require calculating the similarity between $s$ and the corresponding hypervector.

Usually, $s$ is used as an approximate representation of the exact counters of a histogram. Fig. 3 demonstrates Pearson correlation coefficient between the histogram and its approximate version retrieved from a binarized compound hypervector where the approximate version was obtained as the dot product between $s$ and symbols’ seed hypervectors. The simulations were done for different sizes of histogram and varying the dimensionality of hypervectors. The results are characteristic for VSAs – the quality of approximation improved with the increased dimensionality of hypervectors.

This mapping is very similar to counting Bloom filters [Fan et al., 2000] and count-min sketch [Cormode and Muthukrishnan, 2005], which is a randomized data structure for obtaining frequency distributions from sequences. The difference is that due to the usage of bipolar hypervectors the presented hypervector representation could both overcount and undercount the frequency while the count-min sketch could only overcount it.

4) Cross product of two sets: A particularly interesting case is when we have hypervectors representing two different sets (e.g., $\{a, b, c, d, e\}$ and $\{x, y, z\}$). Then a mapping based on the multiplication operation is used to create a hypervector corresponding to the cross product of two sets as follows:

$$(a + b + c + d + e) \odot (x + y + z) =
= (a \odot x + a \odot y + a \odot z) + (b \odot x + b \odot y + b \odot z) +
+ (c \odot x + c \odot y + c \odot z) + (d \odot x + d \odot y + d \odot z) +
+ (e \odot x + e \odot y + e \odot z).$$

In essence, here occurs (due to the superpositions) simultaneous multiplication between all the elements in the two
sets. The cross product set, thus, consists of all possible multiplications of hypervectors representing elements of the original sets (e.g., \(a \odot x\)). In the example above, when starting first with the representations of sets, only 7 operations (6 additions and 1 multiplication) were necessary to form the representation. The brute force way for forming the cross product set hypervector would require 29 operations (14 additions and 15 multiplications). It is clear that this shortcut works due to the fact that the multiplication operation distributes over the addition operation (Section III-B4b). Note that using the Tensor Product Variable Binding [Smolensky, 1990] model, the outer product of vector representations of the two sets will be a matrix with the dimensions determined by the size of the universe of elements. In contrast, the VSA representation of a cross-product is given by a hypervector of the same dimension as the individual set hypervectors.

5) Sequences: A sequence is an ordered set of elements. For example, the set from the previous section is now a sequence \((a, b, c, d, e)\), which is not the same as, e.g., \((b, a, c, d, e)\) since the order of elements is different. Note that a finite sequence with \(k\) elements is called \(k\)-tuple, with an ordered pair being the special case for \(k = 2\).

Clearly, plain addition of hypervectors works for representing sets but not for sequences, as the sequential order would be lost. Many authors have proposed the following idea to represent sequences with permutation, e.g., in [Kussul and Baidyk, 1993], [Plate, 1995b], [Sahlgren et al., 2008], [Kanerva, 2009], [Frady et al., 2018b], [Kanerva, 2019]. Before combining the hypervectors of sequence elements, the order \(i\) of each element is associated by applying some specific permutation \(k - i\) times to its hypervector (e.g., \(\rho^2(c)\)). The advantage of this recursive encoding of sequences is that extending a sequence can be done by permuting \(s\) and adding or multiplying it (see below) with the next hypervector in the sequence, hence, incurring a fixed computational cost per symbol. The last step is to combine the sequence elements into a single hypervector representing the whole sequence.

There are two common ways to combine sequence elements. The first way is to use the addition operation, similar to the case of sets. For the sequence above the resultant hypervector is:
\[
s = \rho^4(a) + \rho^3(b) + \rho^2(c) + \rho^1(d) + \rho^0(e).
\]

In general, a given sequence \(S\) of length \(k\) is represented as:
\[
s = \sum_{S(i)\leftarrow i} \rho^{k-i}(i).
\]

The advantage of the mapping with the addition operation is that it is possible to estimate the similarity of two sequences by measuring the similarity of their hypervectors. Here the similarity of sequences is defined by the number of the same elements in the same sequential positions, where the sequences are aligned by their last elements. Evidently, this definition does not take into account the same elements in different positions, in contrast to, e.g., an edit distance of sequences [Levenshtein, 1966]. Note that the edit distance can be approximated by vectors of \(n\)-gram frequencies and their randomized versions akin to hypervectors (see, e.g., [Sokolov, 2007], [Hannagan et al., 2011]).

Another advantage of sequence representation with addition is that it allows easily probing the distributed representation \(s\). For example, one can check, which element is in position \(i\) by applying inverse permutation \(i\) times to the resultant hypervector. Note that permutation of a sequence representation is a general method for shifting an entire sequence by a single operation. It produces a shifted sequence where the \(i\)th element is now at the first position, and thus it can be used to probe the hypervector of element \(i\) from the sequence representation. For example, when inverting position 3 in \(s\):
\[
\rho^{-2}(s) = \rho^{-2}(a) + \rho^{-1}(b) + \rho^{-1}(c) + \rho^{-1}(d) + \rho^{-2}(e) =
\]
\[
= c + \text{noise} \approx c.
\]

Probing \(\rho^{-2}(s)\) with the item memory containing hypervectors of all sequence elements will return \(c\) as the best match (with high probability).

The second way of forming the representation of a sequence involves multiplication of the permuted hypervectors, e.g., the sequence above is represented as (denoted by \(p\)):
\[
p = \rho^4(a) \odot \rho^3(b) \odot \rho^2(c) \odot \rho^1(d) \odot \rho^0(e).
\]

In general, a given sequence \(S\) of length \(k\) is represented as:
\[
p = \prod_{S(i)\leftarrow i} \rho^{k-i}(i). \tag{7}
\]

The advantage of this sequence representation is that it allows forming unique hypervectors even for sequences that differ in only one position. Section IV-A6 provides a concrete example of a task where this advantage is important.

Both mappings allow replacement of an element at position \(i\) in the sequence if the current element at the \(i\)th position is known. When the addition operation is used, the replacement requires subtraction of the permuted hypervector of the current element followed by addition of the permuted hypervector of the new element. For example, replacing “d” to “z” in position 4 is done as follows:
\[
s - \rho^1(d) + \rho^1(z) = \rho^4(a) + \rho^3(b) + \rho^2(c) + \rho^1(z) + \rho^0(e).
\]
When the multiplication operation is used in the mapping, replacement requires application of the unbinding operation between the permuted hypervector of the current element and \( s \), followed by multiplication with the permuted hypervector of the new element. For the example above:

\[
s \odot \rho^3(d) \odot \rho^3(z) = \rho^4(a) \odot \rho^3(b) \odot \rho^2(c) \odot \rho^3(z) \odot \rho^0(e).
\]

Another feature of both sequence mappings is that the permutation operation distributes over both multiplication and addition operations. This means that in both mappings the whole sequence can be shifted relative to the initial position by applying the permutation operation required number of times. For example, when applying the permutation operation 3 times to \( s \) for \((a, b, c, d, e)\) we obtain:

\[
\rho^3(s) = \rho^7(a) + \rho^0(b) + \rho^5(c) + \rho^4(d) + \rho^3(e).
\]

Thus, \( \rho^3(s) \) is the shifted version of the original sequence. This feature can be used for sequence concatenation. For example, to concatenate \((a, b, c, d, e)\) and \((x, y, z)\), we can use already calculated \( s \) for \((a, b, c, d, e)\) as follows:

\[
\rho^3(s) + \rho^3(x) + \rho^3(y) + \rho^3(z) = \rho^7(a) + \rho^6(b) + \\
\rho^5(c) + \rho^4(d) + \rho^3(e) + \rho^2(x) + \rho^3(y) + \rho^3(z).
\]

Another example of using this feature is an application for searching the best alignment of two sequences [Kleyko and Osipov, 2014]. The representations of the symbol’s order here used hypervector transformation by the permutation corresponding to its absolute position. It might also be useful to consider alternative representations that bind symbol and position hypervectors [Kussul and Rachkovskij, 1991], [Cohen et al., 2013], [Kleyko et al., 2016], which also opens the way to encode successor/predecessor information instead of the absolute position. A great discussion of the ways of using relative positions when representing sequences in VSA was given in [Hannagan et al., 2011].

6) \( n \)-gram statistics: The \( n \)-gram statistics of a sequence \( S \) is the histogram of all length \( n \) substrings occurring in the sequence. The mapping of \( n \)-gram statistics to a single hypervector was presented in, e.g., [Joshi et al., 2016], and includes two steps using the primitives above: First, forming hypervectors of \( n \)-grams, and second, forming a hypervector of the frequency distribution. The hypervectors of \( n \)-grams are formed as in Section IV-A5 using the chain of multiplication operations, i.e., each \( n \)-gram is treated as an \( n \)-tuple. The hypervectors of \( n \)-grams and their counters are then used to form a single hypervector for the frequency distribution as in Section IV-A3. Thus, in essence this is a frequency distribution with compound tokens.

The advantage of this mapping is that in order to create a representation for any \( n \)-gram, we only need to use a single item memory and several simple operations where the number of operations is proportional to \( n \). In other words, with the fixed amount of resources the appropriate use of operations allows forming a combinatorially large number of new representations.

This mapping has been found useful in several applications, in language identification [Joshi et al., 2016], news article classification [Najafabadi et al., 2016], and biosignal processing [Rahimi et al., 2019]. An important advantage of these VSA algorithms is that they are hardware-friendly [Rahimi et al., 2016b]. Another advantage of the mapping is that due to the usage of distributed representations we can unite the dimensionality of the hypervector representing \( n \)-grams statistics from the possible number of \( n \)-grams, which grows exponentially with \( n \) and would dictate the size of a localist representation of the \( n \)-grams statistics. This mapping method was also used for constructing more compact neural networks using the distributed representation of \( n \)-grams statistics as their input [Kleyko et al., 2019a], [Alonso et al., 2021], [Bandaragoda et al., 2019] instead of the localist ones. It works by leveraging the fact that, in natural language processing applications, the number of actually occurring \( n \)-grams grows slower than the number of possible \( n \)-grams. At the same time, when the number of actual \( n \)-grams increases, the quality of reconstruction decreases (cf. Fig. 3), but this happens slowly. Such graceful degradation in VSA compares favorably to the catastrophic forgetting phenomena often observed in neural networks.

7) Graphs: A graph (denoted as \( G \)) consists of vertices and edges. Edges can either be undirected or directed. Fig. 4 presents examples of both directed and undirected graphs. Following earlier work on graph representations with hypervectors, e.g., in [Rachkovskij and Kussul, 2001], [Gayler and Levy, 2009], [Guo et al., 2016], we consider the following very simple mapping of graphs into hypervectors [Gayler and Levy, 2009]. A random hypervector is assigned to each vertex of the graph, according to Fig. 4 vertex hypervectors are denoted by letters (i.e., \( a \) for vertex “\( a \)” and so on). An edge is represented via the multiplication operation applied to the hypervectors of the connected vertices, for instance, the edge between vertices “\( a \)” and “\( b \)” is represented as \( a \odot b \). The whole graph is represented simply as the superposition \( g \) of hypervectors representing all edges in the graph, e.g., the undirected graph in Fig. 4 is:

\[
g = a \odot b + a \odot e + b \odot c + c \odot d + d \odot e.
\]

Note that if an edge is represented as the result of multiplication of two hypervectors for vertices, it has no information about the direction of the edge and, therefore, the representation above will not work for directed graphs. The direction of an edge can be added applying a permutation to the hypervector of the incidental node, the directed edge from vertex “\( a \)” to “\( b \)” in Fig. 4 is represented as \( a \odot \rho(b) \). Note that
The described graph representations $g$ can be queried for the the presence of a particular edge. For graphs that have the same vertex hypervectors, the inner product is a measure of the number of overlapping edges. [Gayler and Levy, 2009] propose a VSA based algorithm for graph matching. For two graphs for which the correspondence between their vertices is unknown, graph matching finds the best match between the vertices so that the graph similarity can be assessed.

The described graph presentations do not work for sparse graphs in which vertices can be entirely isolated because those vertices are not represented at all. One way to address it is by also adding to $g$ the hypervectors representing the vertices, or to keep a separate hypervector with the superposition of all the vertices.

8) Binary trees: A binary tree is a well-known data structure where each node has at most two children: the left child and the right child. Fig. 5 depicts an example of a binary tree, which will be used to demonstrate the mapping of such a data structure into a single hypervector. We describe a mapping process [Frady et al., 2020a] that involves all the three basic VSA operations and two item memories. The result is an ordered pair (2-tuple in this case) provided a solution to this problem. We do not cover the details of factoring trees with the resonator network [Frady et al., 2020a], [Kent et al., 2020] (see Section III-C) provides a solution to this problem. We do not cover the details of factoring trees with the resonator

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The chain of the multiplication operations is used to create a unique hypervector corresponding to the association of the left or right child with its level in the tree. For example, the left child at the second level is represented as $\rho^2(l)$. In general, the level of the node equals the number of times the permutation operation is applied to its role hypervector.

The chain of the multiplication operations is used to create a hypervector corresponding to the trace from the tree root to a certain leaf, associated with leaf’s symbol. For instance, to reach the leaf with symbol “a” it is necessary to traverse three left children. In terms of VSA this trace will be represented as: $a \odot l \odot \rho(l) \odot \rho^2(l)$. In such a way traces to all leaves can be represented.

Finally, the addition operation is used to combine hypervectors of individual traces in order to create a single hypervector (denoted as $t$) corresponding to the whole binary tree. Combining all steps together, the single hypervector for the tree depicted in Fig. 5 will then look like:

$$t = a \odot l \odot \rho(l) \odot \rho^2(l) +$$

$$+ b \odot l \odot \rho(r) \odot \rho^2(l) +$$

$$+ c \odot r \odot \rho(r) \odot \rho^2(l) +$$

$$+ d \odot r \odot \rho(r) \odot \rho^2(r) \odot \rho^3(l) +$$

$$+ e \odot r \odot \rho(r) \odot \rho^2(r) \odot \rho^3(r) +$$

$$+ f \odot l \odot \rho(r) \odot \rho^2(r) \odot \rho^3(l) \odot \rho^4(l) +$$

$$+ g \odot l \odot \rho(r) \odot \rho^3(l) \odot \rho^3(r).$$

Thus, the information about the tree in Fig. 5 is stored in a distributed way in the compound hypervector $t$, which in turn can be queried with VSA operations. For example, given a trace of children we can extract the symbol associated with the leaf at this trace. Assume that the trace is right-right-left then its hypervector is $r \odot \rho(r) \odot \rho^2(l)$. This hypervector can be unbound from $t$ as:

$$t \odot (r \odot \rho(r) \odot \rho^2(l)) = c + \text{noise}.$$

The result is $c + \text{noise}$ because $r \odot \rho(r) \odot \rho^2(l)$ cancels out itself in $t$ and, thus, releases $c$, which was bound with this trace. Since there were other terms in the superposition $t$ they act as crosstalk noise for $c$, hence, denoted as $\text{noise}$.

Thus, when $c + \text{noise}$ is presented to the item memory, the item memory is expected to return $c$ as the closest alternative with high probability. The inverse task of querying the trace with a given leaf symbol is more challenging because the resultant hypervector corresponds to a chain of multiplication operations, e.g., for $c$ we get:

$$t \odot c = r \odot \rho(r) \odot \rho^2(l) + \text{noise}.$$
network here but the interested readers are referred to Section 4.1 in [Frady et al., 2020a].

The presented mapping is, of course, not the only possible way to represent binary trees. For example, in [Kanerva, 2019] it was proposed to use two different random permutations for representing nested structures. This mechanism can be applied to trees as well by using these different random permutations instead of \( l \) and \( r \).

Last but not least, note that the mapping for binary trees can be easily generalized to trees with nodes having more than two children by adding additional role hypervectors in the item memory. Also, filler hypervectors for the leaves do not have to be seed hypervectors. They could represent any compound structure but with the requirement for appropriate clean-up of the compound structure.

9) Stacks: A stack is a memory in which elements are written or removed in a last-in-first-out manner. At any given moment, only the top-most element of the stack can be accessed and elements written to the stack before are inaccessible until all later elements are removed. There are two possible operations on the stack: writing (pushing) and removing (popping) an element. The writing operation adds an element to the stack, it becomes the top-most one while all previously written elements are “pushed down”. The removing operation allows reading the top-most element of the stack. Once read, it is removed from the stack and the remaining elements are moved up.

VSA-based representations of a stack were proposed in [Stewart et al., 2014] and [Yerxa et al., 2018]. The representation of a stack is essentially the representation of a sequence with the addition of an operation that always moves the top-most element to the beginning of the sequence. For example, if “\( d \)”, “\( c \)”, and “\( b \)” were successively added to the stack than the hypervector for the current state of the stack is:

\[
\mathbf{s} = \mathbf{b} + \rho(\mathbf{c}) + \rho^2(\mathbf{d}).
\]

Thus, the pushing operation is implemented as the concatenation of sequences with their hypervectors (Section IV-A5). In particular, the hypervisor of the newly written element is added to the hypervisor of the current state of the stack. For instance, to write “\( a \)” to the current state in \( s \) the following is done:

\[
\mathbf{s} = \mathbf{a} + \rho(\mathbf{s}) = \mathbf{a} + \rho(\mathbf{b}) + \rho^2(\mathbf{c}) + \rho^3(\mathbf{d}).
\]

The popping operation includes two steps. First, \( s \) is probed with the item memory of elements’ hypervectors in order to get the closest match for the seed hypervisor of the top-most element. Once the hypervisor of the top-most element is identified (e.g., \( a \) in the current example), it is removed from the stack and the distributed representation of the stack with the remaining elements moved back by the permutation operation:

\[
\rho^{-1}(\mathbf{s} - \mathbf{a}) = \rho^{-1}(\rho(\mathbf{b}) + \rho^2(\mathbf{c}) + \rho^3(\mathbf{d})) = \mathbf{b} + \rho(\mathbf{c}) + \rho^2(\mathbf{d}).
\]

Note that the popping operation will not work well if the hypervisor representing the stack is normalized after each writing operation, so the operations described above assume that \( s \) is not normalized.

10) Finite-state automata: A deterministic finite-state automaton is an abstract computational model; it is specified by defining a finite set of states, a finite set of allowed input symbols, a transition function, the start state, and a finite set of accepting states. The automaton is always in one of its possible states. The current state can change in response to an input. The current state and input symbol together uniquely determine the next state of the automaton. Changing from one state to another is called a transition. The transition function defines all transitions in the automaton.

Fig. 6 presents an intuitive example of a finite-state automaton, the control logic of a turnstile. The set of states is \{ “Locked”, “Unlocked” \} and the set of input symbols is \{ “Push”, “Token” \}. The transition function can be easily derived from the state diagram in Fig. 6.

VSA-based implementations of finite-state automata were proposed in [Osipov et al., 2017], [Yerxa et al., 2018]. Similar to binary trees, the mapping involves all three VSA operations and requires two item memories. One item memory stores seed hypervectors corresponding to the set of states (denoted as \( l \) for “Locked” and \( u \) for “Unlocked”). Another item memory stores seed hypervectors corresponding to the set of input symbols (denoted as \( p \) for “Push” and \( t \) for “Token”). The hypervectors from the item memories are used to form a single hypervisor (denoted as \( a \)), which represents the transition function. Note that the state diagram of a finite-state automaton is essentially a directed graph in which each edge has an input symbol associated with it. Therefore, the mapping for the transition function is very similar to the mapping of the directed graph in Section IV-A7. The only difference is that the multiplication of the hypervectors for the vertices, (i.e., states) involves, as an additional factor, the hypervisor for the input symbol, which causes the transition. For example, the transition from “Locked” state to “Unlocked” state, contingent on receiving “Token”, is represented as:

\[
\mathbf{t} \odot \mathbf{l} \odot \rho(\mathbf{u}).
\]

Given the distributed representations of all transitions of the automaton, the transition function \( a \) of the automaton is represented by the superposition of the individual transitions:

\[
\mathbf{a} = \mathbf{p} \odot \mathbf{l} \odot \rho(\mathbf{l}) + \mathbf{t} \odot \mathbf{l} \odot \rho(\mathbf{u}) + \mathbf{p} \odot \mathbf{u} \odot \rho(\mathbf{l}) + \mathbf{t} \odot \mathbf{u} \odot \rho(\mathbf{g}).
\]

In order to calculate the next state, we query \( a \) with the multiplication of the hypervectors of the current state and

---

**Fig. 6.** An example of a state diagram of a finite-state automaton modelling the control logic of a turnstile. It has two states. The start state is depicted by the arrow pointing from the black circle.
input symbol followed by the inverse permutation operation applied to the result. Calculated in this way, the result is the noisy version of the hypervector representing the next state. For example, if the current state is \( l \) and the input symbol is \( p \) then we have:

\[
\rho^{-1}(a \odot p \odot l) = l + \text{noise}.
\]

As usual, this hypervector should be passed to the item memory in order to retrieve the noiseless seed hypervector \( l \).

The same mapping can be used to create a hypervector representing a nondeterministic finite-state automaton [Rabin and Scott, 1959]. The main difference from deterministic finite-state automata is that the nondeterministic finite-state automaton can reside simultaneously in several of its states. The transitions do not have to be uniquely determined by their current state and input symbol, i.e., there can be several valid transitions from a given current state and input symbol. The nondeterministic finite-state automaton can assume a so-called generalized state, defined as a set of the automaton’s states that are simultaneously active. The generalized state corresponds to a hypervector representing the set of the currently active states with (5). Similar to the deterministic finite-state automata, the hypervector for the generalized state is used to query the automaton to get a hypervector for next generalized state. This corresponds to a parallel execution of the automaton from all currently active states.

In the next subsection, we will see an example of how to compute with hypervectors representing automata, but the most obvious application of the presented representation is to execute the automaton in the presence of noise in hypervectors. Fig. 7 presents the accuracy of the correct recall of a next state from a bipolarized hypervector representing an automaton with 22 states and 29 symbols. The figure shows how the accuracy changed with the dimensionality of hypervectors for different values of noise in \( a \). As expected, we see that for every amount of noise, there is eventually a dimensionality, which allows a perfect recall, which is an elegant property that can be simply leveraged for executing a deterministic behavior in a very stochastic environment.

Note that the primitives for stacks and finite-state automata can be combined to create such computational models as deterministic pushdown automata or stack machines; see, e.g., [Yerxa et al., 2018] for a sketch of a stack machine operating with hypervectors. An alternative representation for pushdown automata and context-free grammars has been recently presented in [beim Graben et al., 2020].

11) Deeper hierarchies: Finally, it is important to touch upon constructing data structures encoding deep hierarchies. In the previous subsections, we concentrated mainly on data structures with a single level hierarchy. VSAs, however, are well-suited for representing many levels of hierarchy. The representation of binary trees in Section IV-A8 can already be seen as a hierarchy since a tree has several levels and the representation should be able to discriminate between different levels. In the presented mapping, this was done using powers of permutation to protect different levels of hierarchy. This can be done in some other ways by, e.g., assigning special role hypervectors for each level. Currently, the usage of representations for hierarchies in VSAs is relatively uncommon. We mainly attribute this fact to the nature of applications which are being explored, rather than to the capabilities of VSAs. The use-cases, which relied on the representation the hierarchical representations, are representation of analogical episodes [Plate, 2003], [Rachkovskij, 2001], [Slipchenko and Rachkovskij, 2009], [Rachkovskij and Slipchenko, 2012], distributed orchestration of workflows [Simpkin et al., 2019], and representation of hierarchies in WordNet concepts [Crawford et al., 2016].

B. VSA models for different types of hardware

The computational primitives of VSA connect the algorithmic level of Marr’s computing hierarchy (Fig. 1) to the computational level. At the same time, a VSA placed at the algorithmic level also interfaces with the implementation level. While the computational primitives are generic across different VSA models, the model choice can become critical when it comes to interfacing with a particular physical substrate. This suggests a general design pattern when designing a VSA system to be implemented on nanoscale hardware: the desired computation is formalized in terms of the generic VSA computational primitives, and then the specific VSA variant best suited for this nanoscale hardware is used in implementing these primitives. Here we describe some of the existing VSA models and examples of how they accommodate different hardware. Different VSA models can be distinguished in terms of the properties of seed hypervectors and corresponding algebraic operations.

1) Dense binary vectors: The Binary Spatter Code [Kanerva, 1997] model uses dense binary vectors. Addition is by component-wise majority rule followed by tie-breaking, and multiplication is by component-wise XOR.
Due to their discrete nature, Binary Spatter Code is highly suitable for digital hardware, such as field-programmable gate arrays [Rahimi et al., 2016b]. It also can be implemented in nanoscale hardware such as carbon nanotube field-effect transistors [Wu et al., 2018b] and phase-change memory devices [Karunaratne et al., 2020]. Another popular idea is to build a programmable VSA processor. For example, in [Datta et al., 2019] a prototype has been developed using an application-specific integrated circuit.

2) Integer vectors: The Multiply-Add-Permute model [Gayler, 1998], the example VSA we have used so far as the default, employs bipolar (+1s and -1s) hypervectors, component-wise multiplication and addition, which can be thresholded. Multiply-Add-Permute model will usually suit the same technologies as Binary Spatter Codes. For example, it was recently implemented with system-on-a-chip field-programmable gate array for hand gesture recognition [Moin et al., 2021].

3) Real-valued vectors: The Holographic Reduced Representation model [Plate, 1995a] was originally done with $N$-dimensional real-valued hypervectors whose components are i.i.d. normal with zero mean and $1/N$ variance. Addition is by normalized vector sum, and multiplication is by circular convolution. It has been shown how to map real-valued hypervectors onto spiking neurons using the principles from the Neural Engineering Framework [Eliasmith and Anderson, 2003] with the help of spike-rate coding. For example, the Spaun cognitive architecture [Eliasmith, 2013] has been implemented in such a way. Most of the studies were done using simulations in Nengo [Bekolay et al., 2014], which is a Python-based package for simulating large-scale spiking neural networks. Nevertheless, Nengo has compilers to popular neuromorphic platforms such as SpiNNaker and Loihi and so it is not a problem to run a model on a real hardware.

4) Complex vectors: In the frequency domain, Holographic Reduced Representations [Plate, 2003], vector components are random phasors, addition is by component-wise complex addition followed by normalization, and multiplication is by component-wise complex multiplication (addition of phasors) [Plate, 2003]. This VSA model should be suited for implementations on coupled oscillator hardware [Csaba and Porod, 2020], however, we are not aware of any concrete hardware realizations as of yet. Another alternative is mapping complex VSA to neuromorphic hardware [Davies et al., 2018], by representing phasors with spike times [Frady and Sommer, 2019]. This implementation is particularly interesting because neuromorphic hardware scales up more easily than current approaches to coupled oscillator hardware. However, no neuromorphic implementation of a full complex VSA has been reported to date.

5) Sparse vectors: Traditional VSA models use dense distributed representations. However, sparsity is an important ingredient of energy efficient realizations in hardware. Thus, VSA models that use sparse representations are extremely important for mapping VSA operations efficiently onto hardware. We are aware of two such models: Sparse Binary Distributed Representations [Rachkovskij and Kussul, 2001], [Rachkovskij, 2001] and Sparse Block-Codes (SBC) [Laiho et al., 2015], [Frady et al., 2020b]. In Sparse Binary Distributed Representations model, the hypervectors are sparse patterns without any restrictions on placing the active components while in Sparse Block-Codes the hypervectors are divided into blocks of the same size (denoted as $K$) with just one single active component per block. The Sparse Binary Distributed Representations model was implemented around 1990 in specialized hardware – “associative-projective neurocomputer” [Kussul et al., 1991b]. This hardware was designed to operate efficiently with sparse representations [Rachkovskij, 2001] by using simple bit-wise logical operations and a long word processor with 256 bits (later with 512 and 2048 bits, implemented by Wacom, Japan). For clean-up memory, it implemented Willshaw-like associative memories, following earlier ideas to implement such memory networks [Palm and Bonhoeffer, 1984] and motivated by theoretical results suggesting high memory capacity [Willshaw et al., 1969], [Palm, 1980], [Palm and Sommer, 1992], [Sommer and Dayan, 1998], [Frolov et al., 2002]. Concerning VSA with Sparse Block-Codes, in particular with complex-valued sparse vectors, they seem to be the most amenable for implementations on neuromorphic and coupled oscillator hardware (see Section V-C).

6) Differences of VSA models interfacing the computational level: As described in Section IV-A, computational primitives can be built in VSA quite independent of a the particular VSA model under consideration. While this generality largely holds, some differences between VSA models also affect some details on the algorithmic and computational levels. This is not entirely unexpected since, if a framework can provide tight matches between computation and hardware to enable efficiency, the separation between abstraction and physical realization cannot be perfect. An example of such a difference is the self-inverse property of multiplication, which is offered by the Multiply-Add-Permute and Binary Spatter Codes models but not for the Holographic Reduced Representation model. If multiplication is self-inverse, there is a simple and direct way to represent undirected graph edges but requires more complexity to be used to represent directed edges (see Section IV-A7 for more details). In VSAs without self-inverse binding, one needs workarounds for this function (see a detailed discussion on this topic in [Schlegel et al., 2020]).

7) Implementation costs: Here we sketch the analysis of implementation costs of some basic VSA operations, item memory and the multiplication operation. Specifically, we compare the Binary Spatter Codes model (Section IV-B1) that uses dense binary hypervectors and the Sparse Block-Codes model (Section IV-B5) that uses sparse binary hypervectors. First, we quantify the memory requirements for item memory, realized by an array. For dense binary hypervectors, the array would require $DN$ bits. For sparse binary hypervector, it is sufficient to store the index of the active component for each block in the array, which requires $DN \log_2(K)/K$ bits. Thus, sparse binary hypervectors will have a noticeable advantage when $\log_2(K)/K << 1$. For example, if $N = 8192$ and $K = 128$, the array with sparse binary hypervectors will require 18.3 times less memory than the array with the dense binary hypervectors. Note that for sparse hypervectors,
the item memory can also benefit from a more advanced implementation based on the inverted index data structure.

When it comes to the cost of calculating the clean-up operation, the item memory with dense binary hypervectors requires \(N D\) multiplications per clean-up, whereas the item memory with sparse binary hypervectors with \(N/K\) active components would require only \(N D/K^2\) multiplications, which is a factor of \(K^2\) fewer versus the dense case. Of course, in general, a sparse hypervector will have more than \(N/K\) active elements due to, e.g., noise and superposition, but clearly the order of savings can be higher than for the memory size.

Neural associative memories are an alternative way to implement the item memory. The capacity analysis of associative memories storing dense and sparse representations is more involved than comparing arrays and will be omitted. Nevertheless, the capacity analysis of associative memories with one-shot learning, like in the Hopfield network, reveals that the storage of sparse patterns can achieve much higher memory capacities than dense patterns [Tsodyks and Feigelman, 1988], [Palm and Sommer, 1992], [Gritsenko et al., 2017]. In terms of memory requirements and number of computations for matching a query, associative memories can be more efficient than arrays in certain regimes, for a comparison, see [Knoblauch et al., 2010].

Second, we quantify the cost of the multiplication operation. For dense binary hypervectors, the multiplication is component-wise XOR and requires only \(N\) single-bit operations per multiply. A neuromorphic implementation of Sparse Block-Codes binding would likely involve a compression of the outer product per block of the two hypervectors, which would require all-to-all connectivity within each block [Frady et al., 2020b]. Hence the cost of sparse binding in this implementation would be \(N(2K - 1)\) operations, or \(O(K)\) more expensive in ops than the dense binary case.

Our example analysis here demonstrates that implementation costs include required memory and required numbers of operations that the hardware must provide. Implementation costs depend on what operations are required in the VSA algorithm, and the properties of hypervectors.

C. Computing in superposition with VSAs

1) Simple examples of computing in superposition: A well-known data structure in computer science – Bloom filters [Bloom, 1970] – can be seen as the simplest case of computing in superposition. Bloom filters belong to the class of data structures called sketches, where a fixed-size memory footprint is used to represent a set of several elements using binary representations of these elements. A Bloom filter encodes a set as a superposition of its elements’ random vectors, which, in essence, corresponds in VSA to a compound hypervector representing sets (cf. Section IV-A2). With Bloom filters, the algorithm for searching an element in a set is a single operation of comparing the similarity of the distributed representation of the query element to the Bloom filter instance. In other words, all elements of the set are tested in one shot, i.e., the search is performed as a computation in superposition. It enables solving the approximate membership query task instantaneously. This illustrates a simple instance of computing in superposition. Bloom filters are highly specialized for one particular task. In contrast, VSAs constitute a broad framework for computing in superposition, containing Bloom filters as a subclass [Kleyko et al., 2020]. We have seen other examples already in Section IV-A for computing in superposition with VSA, such as the recursive construction of sequence representations, (6) and (7), and in Section IV-A4 the forming of a representation for the cross product of two sets via a single multiplication operation. In these examples, the distributivity of VSA operations (see Section III-B4) played an important role.

2) Computing in superposition for substring search: Finding a substring within a larger string is a classic computer science problem with many useful applications. Numerous algorithms have been developed including the Boyer-Moore-Horspul algorithm [Boyer and Moore, 1977], Rabin-Karp algorithm [Karp and Rabin, 1987], Knuth-Morris-Pratt algorithm [Knuth et al., 1977] and others. The best solution has a linear computational complexity, which depends on the sum of the lengths of the base and the query strings. Recently, an algorithm for substring search based on nondeterministic finite-state automata has been formulated with VSAs [Pashchenko et al., 2020]. We will briefly explain this formulation, and a modified version, because it nicely demonstrates how VSAs enable one to solve computer science problems when the framework is implemented with parallel hardware.

Each position of a symbol in the base string is modeled as a unique state of the nondeterministic finite-state automaton \(S = \{s_0, s_1, s_2, \ldots, s_n\}\). For example, the string “hello” generates an automaton with six states: \(s_0\) through \(s_5\). The transitions between states are defined by the base string’s (denoted \(B\)) symbols \(b_i\) from \(B = \{b_0, b_1, b_2, \ldots, b_n\}\). Fig. 8 illustrates the automaton for the string “hello.” The nondeterministic finite-state automaton is then defined by tuple \(<S, s_0, B, T>\), where \(s_0\) is the start state of the automaton and \(T\) is a set of transition tuples of the form \(t_i = <s_{i-1}, b_i, s_i>\), where \(s_{i-1}\) and \(s_i\) are the start and end states of a particular transition caused by symbol \(b_i\). The elements of sets \(B\) and \(S\) are represented by i.i.d. random hypervectors (denoted in bold). The hypervector \(\beta\) of the automaton for a base string is constructed as (cf. Section IV-A10):

\[
\beta = \sum_{i=1}^{\left|B\right|} s_{i-1} \odot b_i \odot \rho^1(s_i).
\]

Thus, \(\beta\) is the superposition of all the automaton’s transitions caused by sequential input of symbols of the base string.

The algorithm for finding whether a query string \(Q = \{q_1, \ldots, q_l\}\) is a part of the base string \(B\) is constructed as a sequential retrieval of the next state of automaton \(\beta\), for each
symbol of the query string $q_j$. In terms of hypervectors, this is:

$$p_j = \rho^{-1}(p_{j-1} \odot \beta \odot q_j),$$  \hspace{1cm} (9)$$

where $p_j$ denotes the hypervector that includes the hypervector(s) of the next generalized automaton state (given symbol $q_j$), as well as crosstalk noise. Note that generalized state may include one or several $s_i$ states. The set of valid (i.e., permitted) previous generalized states is initialized as $p_0 = \sum_{s_i \in S} s_i$, which is a superposition of all the states of the base string. Note that the operation in (9) is performed on the superimposed set of all states, so it is computing in superposition.

We simulated the algorithm for searching a fixed length query substring (5 symbols) in the base string of three different lengths (see left panel in Fig. 9). Average accuracy in 30 simulation runs is plotted against the varying dimensionality of hypervectors, where in every simulation run 100 different random base strings were executed. In approximately half of the searches the query substring was present in the base string, so a single simulation run determines the accuracy of correctly detecting when a substring is present and when it is not (thus, the accuracy of a random guess is 0.5). With increasing dimensionality of hypervectors, the accuracy of detecting a substring increases and eventually approaches 1, however for long base strings it would require larger dimensions of the hypervectors than we tested. The required dimensionality grows because every step of (9) introduces additional crosstalk noise to $p_j$.

A straightforward way to reduce crosstalk noise is to perform a clean-up procedure on $p_j$ after every execution of (9):

$$p_j = SS^\top p_j,$$  \hspace{1cm} (10)$$

where $S \in [N, n+1]$ denotes the item memory storing hypervectors for the unique states of the base string, $S = \{s_0, s_1, s_2, \ldots, s_n\}$. Note that, like resonator networks [Frady et al., 2020a], [Kent et al., 2020], this uses the idea of projecting predictions back onto the item memory (see Fig. 2 and equation (4)).

Right panel in Fig. 9 shows the results of the modified algorithm for searching a fixed length query substring (30 symbols) in the base string of four different lengths plotted against the varying dimensionality of hypervectors. The modified algorithm allows not only detecting the query substring but also identifying the position(s) of the query substring within the base string (results not shown). Similar to the results in the left panel in Fig. 9, longer base strings require larger hypervectors to achieve high accuracy, but the modified algorithm scales better than the original one. For example, to achieve the perfect accuracy for the shortest string, the modified algorithm required the hypervectors with the dimensionality being approximately 4,000 times less than in the original algorithm.

The asymptotic computational complexity of the query algorithm in VSA operations is $O(|Q|)$ for the original algorithm versus $O(|Q||B|)$ for the modified algorithm. But in terms of hypervector dimensionality, the original algorithm required much more space than the modified algorithm. There is a tradeoff between compute time and space requirements.

There are interesting lessons from the substring search example with regard to computing in superposition with VSA. Both substring search algorithms employ computing in superposition. The original algorithm requires a large dimensionality to reduce crosstalk between items in the superposition sufficiently. The modified algorithm includes an added step of clean-up, which reduces the required dimensionality drastically, but also increases the algorithmic complexity. However, with appropriate implementation of the VSA algorithm on parallel hardware, the clean-up step (10) can be parallelized. Specifically, it has been shown that computing similarities between a hypervector and an item memory can be done in parallel when implemented by in-memory computing architectures using massive phase-change memory devices [Karunarathne et al., 2021]. When executed on such hardware, the time complexity of the modified algorithm also becomes $O(|Q|)$. 

![Fig. 9. Search of a substring in superposition with VSA. The length of a substring was fixed to 5. The reported values were averaged over 50 simulations. Left panel: the algorithm from [Pashchenko et al., 2020]; Right panel: the modified algorithm from [Pashchenko et al., 2020].](image-url)
Note that, of course, the size of the chip places limitations on the dimensionality of hypervectors and the number of hypervectors in VSA is natural but can require very high dimensionality for managing crosstalk. Steps to manage the crosstalk can be added in the algorithm at no compute time costs, if the algorithm is properly mapped on parallel hardware (see, e.g., [Kim et al., 2020] for acceleration of parallel hardware in VSA). Moreover, the whole mechanism of the resonator network (see Section III-C) for parsing compound hypervectors is based on the idea of gradually removing crosstalk noise from the predictions represented in the superposition. We expect that this principle of crosstalk removal from the intermediate results of computation, and resonator networks in general, are going to be pivotal mechanisms in many solutions based on computing in superposition but this is yet to be demonstrated in practical use-case scenarios.

V. Discussion

A. VSA as a framework for nanoscale computing hardware

VSAs were originally proposed in cognitive neuroscience as models for symbolic reasoning with distributed representations. More recently, it has been shown that VSA can formulate sub-symbolic computations, for example, in machine learning tasks. Here we proposed that VSAs provide a computing framework with an algorithmic level description for linking abstract computation with nanoscale hardware as in Marr’s framework [Marr, 1982]. The algorithmic formalism of VSA (with few exceptions) is the same for all of its variants. Thus, VSAs enable a model-independent formulation of computational primitives. At the same time, VSAs also provide a seamless interface between algorithms and hardware. In Section IV-B, we illustrated how different VSA models can connect to specific types of nanoscale hardware. Moreover, in Section IV-C we demonstrated how VSAs can be used for computing in superposition. This feature extends VSAs beyond the conventional computing architecture and we foresee that with together with algorithms that leverage computing in superposition, such as resonator networks [Frady et al., 2020a], [Kent et al., 2020] (Section III-C), it will pave the way to efficient solutions of non-trivial combinatorial search problems (see an example in [Frady et al., 2018a]).

Despite recent successes in applying VSAs in machine learning [Rahimi et al., 2019], [Ge and Parhi, 2020], word embedding [Kanerva et al., 2000], [Recchhia et al., 2015], analogical reasoning [Plate, 1997], [Rachkovskij and Slipchenko, 2012] and cognitive architectures [Eliasmith, 2013], [Rachkovskij et al., 2013], there is still a need to demonstrate how VSA-based solutions scale-up to real-world computational problems. Further, the extension of VSAs to novel application domains must be continued – promising recent examples include applications in communication [Kim, 2018] and in distributed systems [Simpkin et al., 2019].

Another interesting take on VSA computing is that it occupies a realm between digital and analog computing. After each computation step in a digital computer, all vector components are pulled to one of the possible digital states (bits). This individual discretization of each component avoids error accumulation. Conversely, an analog computer is supposed to implement an analog dynamical system to predict its future states. Any deviation between the dynamical system to be analyzed and its computer implementation, noise etc, leads to uncontrollable error accumulation in analog computers. VSA operations leverage analog operations on vectors without discretization. However, discretization takes place on the entire vector level, when a resultant VSA vector is matched with the entries in the item memory. Thus, VSA can leverage (potentially very) noisy dynamics in the high-dimensional state space of nanoscale hardware, while still protecting against error accumulation.

B. Computational primitives

VSAs have been criticized for lacking a structured methodology for designing systems as well as for missing well-defined design patterns [Neubert et al., 2019]. Here we compiled existing computational primitives with VSA that paint a different picture. There is a VSA methodology addressing a wide range of applications but it is scattered throughout the literature. In addition to compiling existing work, we laid out principles of design for building distributed representations of data structures such as sets, sequences, trees, key-value pairs, and more. This demonstrates a rich algorithmic and representation level approach which one can use as an abstraction for the next generation of computing devices.

Our compilation of varied VSA primitives also suggests that, contrary to some earlier assessments (see, e.g., [der Velde and de Kamps, 2006] and the commentary in [Gayler, 2006]), the repertoire of VSA applications is extremely wide, ranging from low-level sensory processing to high-level reasoning. In fact, in terms of application breadth and transparency, VSAs seem to be a much more promising candidate for a computing framework for parallel computing than, e.g., traditional neural networks.

1) VSA dimensionality and working memory: The key feature of data representation in VSAs is that data structures are represented by fixed sized hypervectors, independent of the size of a data structure. This is in contrast to the localist representations of data structures, which grow linearly or even quadratically (e.g., graphs) with the number of elements. The great advantage of VSA representations is that data structures of arbitrary size and shape can be manipulated in parallel with the elementary set of VSA operations. At the same time, for a given dimensionality of VSA vectors, the information content of a vector, the VSA capacity, limits the size of data structures that can be represented [Frady et al., 2018b], [Thomas et al., 2020].

One should think of the memory in hypervectors as the working memory or working registers, holding the data relevant during an ongoing computation. In contrast, the long-term memory or RAM in VSA computation is item memory, i.e., the content-addressable storage of hypervectors. The limitation of working memory in VSA has interesting parallels to the limitation of human working memory. For limited sized data structures, there are guarantees for exact reconstruction [Thomas
et al., 2020]. However, transcending the theoretical bound for exact reconstruction, the data representation becomes lossy, with error rates also being theoretically predictable [Frady et al., 2018b]. VSA representations of data structures in the lossy regime have been shown to reproduce some properties of human working memory. For example, the recall of sequence in a VSA, as described in Section IV-A5, can reproduce the performance of humans remembering sequences [Choo and Eliasmith, 2010], [Kelly et al., 2020]. Further, the modeling of memorizing sequences with VSAs was linked to the neuroscience literature in [Calmus et al., 2019]. It is not immediately clear how this capturing of the limitations of human memory might be beneficial for applications. However, the way biological working memory coarsens its content and gradually degrades might be an important feature of cognition whose benefits are not yet fully appreciated. For example, there are useful applications of VSA operating beyond the VSA capacity in natural language processing [Alonso et al., 2021], [Shridhar et al., 2020].

2) Transformation of representations in VSAs: Distributed representations of data structures can be used to construct or learn single-shot transformation between data structures (see, e.g., [Neumann, 2002], [Plate, 1997]) that share symbols, which differentiates distributed representations from conventional data structure manipulations. A well-known example of this feature has been presented in [Kanerva, 2000] where a mapping between the “mother-of” relation to the “parent-of” relation was constructed with simple vector operations and using only a few examples. It was shown later in [Kleyko et al., 2015] that such a mapping can be used to easily form associations between observed structures and decisions caused by these structures.

3) Flow control in VSAs: It is also worth pointing out that VSA implementations of algorithms generally rely on existing non-VSA mechanisms for flow control (but see [Yerxa et al., 2018] for an attempt). This is reasonable in systems where the aim is to use VSA to implement conventional computing approaches. In this case, it can be seen more from the point of extending conventional computing with VSA. However, if we were modelling biological systems we should not be using non-VSA conventional computing flow control. Instead, we would look at recurrent systems with attractors and meta-stable states. An attempt to define such a system with VSAs and spiking neurons was done in [Stewart et al., 2010].

C. Mapping algorithms to hardware

1) Impact of hypervector sparsity on implementation: Sparsity of hypervectors is important when considering efficient hardware realizations of VSAs. The algebraic structure and the computational primitives of VSAs are largely independent of the choice of particular hypervector properties. However, the properties of hypervectors and their associated physical embodiments profoundly affect the resource requirements.

Dense hypervectors support component-wise multiplication and addition operators that allow for cheap and fully parallel physical implementations. To compute $c_N$ operations in the hypervector domain, only $c_N \cdot N$ pair-wise operations are required with the sequential computing. However, dense hypervectors are expensive when it comes to signal representation communication and memory.

In contrast, with sparse hypervectors in the Sparse Block-Codes model, the binding operation cannot be component-wise (it is block-wise) and is computationally more expensive than for dense vectors. Conversely, the hardware requirements for representation, communication and memory are cheaper than for dense hypervectors. So the cost savings that Sparse Block-Codes model potentially provides for clean-up operations, storage, and communication must be balanced against their increased cost for the binding operation and connectivity (within the blocks) requirements.

Section IV-B7 spelled out some of the considerations for comparing implementation costs of VSA models. It has to be emphasized that search in item memory, although not one of the basic VSA operations, might dominate the computational costs of an algorithm, especially when used iteratively, i.e., for parsing compound representations (Section III-C), or for cleaning-up intermediate results for computing in superposition (Section IV-C2). Therefore, we expect that efficient hardware implementations of the item memory (see some proposals in [Karunarathne et al., 2021], [Imani et al., 2017]) will be one of the key ingredients for scaling-up future VSA applications.

2) Modern hardware implementations of VSA: How do existing implementations of VSAs in hardware produce gains in performance over conventional computing architectures? Today, there are several directions in developing nanoscale computing hardware including digital, analog, and spiking approaches. Due to the variety of different VSA models in the literature, the VSA framework can connect to many different types of nanoscale hardware. On a low-power digital platform using field-programmable gate arrays (FPGA) it has been demonstrated that VSA-based classification can lower the energy by $\approx 2\times$ compared to conventional classifiers for both, EU language recognition [Rahimi et al., 2016b], and biomedical signal classification [Montagna et al., 2018]. The energy saving is due to the fact that the VSA algorithm mostly uses basic bit-wise operations. Further, it has been demonstrated that it is possible to automatically generate a FPGA implementation of a given VSA algorithm [Salamat et al., 2019]. Another appealing property of VSA algorithms is their great robustness, for example, with respect to permanent hardware errors, specifically, VSA tolerate about $60\times$ higher probability of failures [Li et al., 2016]. This robustness makes VSA ideally suited to the low signal-to-noise ratio/high variability conditions in nanoscale hardware, such as resistive random-access memory [Li et al., 2016], carbon nanotube field-effect transistors, and their monolithic 3D integration [Wu et al., 2018b], [Wu et al., 2018a]. Finally, VSA has shown to be a promising framework for in-memory computing [Gupta et al., 2018], [Gupta et al., 2020], [Karunarathne et al., 2020]. For example, as a large-scale experimental demonstration [Karunarathne et al., 2020], a VSA was implemented on 760,000 phase-change memory devices performing analog in-memory computing with 10,000-dimensional binary hypervectors for three different
classification tasks. The VSA not only achieved accuracies comparable to software implementations – despite the non-idealities in the phase-change memory devices. It also achieved over 6× energy saving compared to an optimized digital implementation [Karunaratne et al., 2020].

The connection of VSA to spiking neuromorphic hardware is not obvious since all classical VSA models used abstract connectionist representations, not spikes. However, recent work has demonstrated that representations of a complex VSA model, Frequency Domain Holographic Reduced Representations [Plate, 2003], can be mapped to spike timing codes [Frady and Sommer, 2019]. Although focused just on content-addressable memory, i.e., item memory, this work opens avenues for efficient implementations of full VSA models on neuromorphic hardware [Davies et al., 2018]. Because neuromorphic hardware often optimizes spike communication for sparse network connectivity, the scaling properties of neuromorphic VSAs potentially will outperform other types of hardware.

Further, neuromorphic hardware might enable hybrid approaches by integrating VSAs with other computing frameworks. For instance, an event-based dynamic vision sensor (as a front-end spiking sensor) is combined with sparse VSA leading to 10× higher energy efficiency than an optimized 9-layer perceptron with comparable accuracy on an 8-core low-power digital processor [Hersche et al., 2020].

Despite all these promising results, the practicability of the VSA computing framework for nanoscale computing hardware is yet to be quantified. An important future direction is to develop a systematic methodology to quantitatively measure and compare side-by-side the efficiency of different computing frameworks on a concrete hardware. In this article we concentrated on the question how VSA enables the construction of varied algorithmic primitives and, therefore, could be a possible candidate framework in such a comparison.

D. Computational universality of VSAs

Studying computational universality of a particular computing framework is important for understating ultimate theoretical limitations of computing hardware using this framework. For example, [Siegelmann and Sontag, 1991] have shown that recurrent neural networks are computationally universal, [Perez et al., 2019] have shown universality of modern transformer and Neural GPU networks. There are some equivalence and universality results for VSA. First, VSA can express a class of recurrent neural networks known as Echo State Networks [Kleyko et al., 2020a]. Regarding universality, we followed earlier approaches that showed that neural network-like systems can implement Turing machines [beim Graben and Potthast, 2012]. We show that VSA can implement a Turing machine (Appendix A-A), and a universal elementary cellular automaton with rule 110 [Cook, 2004] (Appendix A-B).

Recently, [Kwisthout and Donselaar, 2020] emphasized a need for a formal machine model for novel neuromorphic hardware in order to develop a computational complexity theory for neuromorphic computation. This is an important direction of research for understanding the full potential of nanoscale hardware. They argued, however, that in order to encompass the computational abilities of neuromorphic hardware we will likely need to define an entirely new computing theory framework. Their study has proposed to use spiking neural networks (shown to be Turing complete [Maass, 1996]) because, similar to VSA, they are suitable for co-located computation and memory and massive parallelism, which is not the case for the conventional computing architecture.

In addition to the theoretical proof of universality, an important practical question is how a complete computational architecture should look like. This is is still an open problem. A proposal has been sketched in [Laiho et al., 2015], which proposed a VSA-based processor where both data and instructions were represented as hypervectors. There is another approach known as Tensor Product Variable Binding, which is closely related to VSAs. For example, Tensor Product Variable Binding can also be used to represent data structures in distributed representations (see [Demidovskij, 2021]). The study [Smolensky, 1990] has demonstrated how to implement push, pop, and the Lisp primitives CAR and CDR with Tensor Product Variable Binding, while [Dolan and Smolensky, 1989] has demonstrated how to implement a production system. A VSAs-based model, which was positioned as a general-purpose neural controller playing a role analogous to a production system, was proposed in [Stewart et al., 2010].

Another relevant result is a demonstration of the feasibility of implementing Fluid Construction Grammars with VSA [Knight et al., 2015]. Even though Fluid Construction Grammars have not been shown to be universal, it is accepted that a family of Fluid Construction Grammars is a powerful and interesting approach for both cognitive and evolutionary linguistics. [Knight et al., 2015] proposed a vision similar to the one presented in Fig. 1. They suggest VSA can be seen as a “virtual machine”, which can have different (independent) physical implementations, such as an indirect mapping to spiking neurons [Frady and Sommer, 2019] or direct mapping of operations with analog/digital implementations [Karunaratne et al., 2020].

E. Alternative frameworks for computing with nanoscale hardware

VSA constitutes a computing framework that provides an algebraic language for formulating algorithms and, at the same time, links the computation to distributed states on hardware.
There is a trade-off between how general a framework is in terms of computation and how closely it is linked to implementation. A general purpose framework typically requires a full sealing between implementation and computation, like, for example, the conventional computing architecture. Conversely, a framework that is well matched to an implementation, and therefore can efficiently leverage the hardware, is typically quite special purpose. We argue that the tradeoff VSA provides between generality and linking to implementation is ideal for nanoscale hardware. In particular, it seamlessly provides implementations of algorithms that leverage distributed representations, parallel operations and can tolerate noise and imprecision [Rahimi et al., 2017]. Of course, VSA is not the only candidate of a framework for nanoscale hardware, alternative approaches include probabilistic computing [Mansinghka, 2009], sampling-based computing [Orbán et al., 2016], computing by assemblies of neurons [Papadimitriou et al., 2020], and dynamic neural fields [Schöner et al., 2016]. For example, in neuromorphic computing, dynamic neural fields is an alternative computing framework that could support fully symbolic operations. In fact, dynamic neural fields and VSAs might complement each other by combining real-time dynamics of dynamic neural fields with the computational power and scalability of VSAs. The detailed comparison between these approaches and VSAs is, however, outside the scope of this article. Nevertheless, in our opinion VSA is the most transparent approach in structuring computation, and the most general with regard to different types of hardware. In terms of formulating algorithms and computational primitives, VSA offers a common language, independent of a particular VSA model. For a desired computation on a given hardware, one of the many existing VSA models can provide the most advantageous implementation in terms of power and time efficiency.

There is currently a plethora of collective-state computing approaches emerging, such as compressed sensing, Bloom filters, reservoir computing, compressed sensing, etc., relying on distributed representations [Csaba and Porod, 2020]. These approaches are rather disjoint, and typically focus on special purpose computing applications. VSAs have been shown to be able to formalize different types of collective-state computing, such as compressed sensing [Frady et al., 2020b], Bloom filters [Kleyko et al., 2020], reservoir computing [Frady et al., 2018b], [Kleyko et al., 2020a], and extreme learning machines/random vector functional link networks [Kleyko et al., 2020]. Thus, we see VSAs as a promising candidate framework for providing a “lingua franca” of collective-state computing.

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For a given combination of the current state and tape’s content, the behaviour of a (2,4) Turing machine is presented in Table II.

We make two proposals to do so by either implementing a Turing machine or by emulating an elementary cellular automaton, which is also known to be Turing complete. While computing in superposition is likely to provide us with a quantification of the theoretical capabilities of using VSAs as a computing framework. Of course, it is desirable that a computing framework for nanoscale hardware be able to (in theory, at least) execute any algorithm. In this section we show that VSAs are computationally universal by demonstrating that they can emulate a system which has already been proven to be Turing complete.

### Appendix A

#### Turing completeness of VSAs

It is practical to have a collection of primitives for common data structures. However, these primitives alone do not provide us with a quantification of the theoretical capabilities of using VSAs as a computing framework. Of course, it is desirable that a computing framework for nanoscale hardware be able to (in theory, at least) execute any algorithm. In this section we show that VSAs are computationally universal by demonstrating that they can emulate a system which has already been proven to be Turing complete.

While computing in superposition is likely to be the most interesting mode of operating with VSAs, computational universality is still a useful property as it provides us with a characterization of the general computational power of VSAs. It is worth noting that among VSAs researchers there is a general agreement that VSAs are computationally universal (personal communication) but, to the best of our knowledge, this has not been shown yet. We make two proposals to do so by either implementing a Turing machine or by emulating an elementary cellular automaton, which is also known to be Turing complete [Cook, 2004].

### A. Implementation of Turing machines with VSAs

Since there are a number of small Turing machines known to be universal [Neary and Woods, 2009] we first focus on demonstrating how VSAs can be used to implement such a machine. In order to do so, we present how VSAs representations are used to map a table of behaviour [Neary and Woods, 2009] and execute the machine.

The presented implementation could be used to realize any Turing machine, but for the sake of compactness we exemplify the implementation with a (2,4) Turing machine, which has 2 states (A and B) and 4 symbols (0, 1, 2, 3). The table of behaviour of a (2,4) Turing machine is presented in Table II. For a given combination of the current state and tape’s content, it provides which symbol should be written to the current cell,
the next state of the machine, and the direction for the head’s move.

1) VSAs implementation of the table of behaviour: We use the Multiply-Add-Permute model described above. In order to represent a table of behaviour of a Turing machine, we first create two item memories populated with random hypervectors. One item memory stores the states, e.g., in the case of a (2,4) Turing machine it includes only two hypervectors for states A and B (denoted as $a$ and $b$), respectively. Another item memory stores hypervectors for symbols. Since the considered machine uses only four symbols, four hypervectors $0$, $1$, $2$, and $3$ are sufficient. These item memories are used to construct a hypervector for each combination of states and symbols. The hypervector is constructed by applying the multiplication operation on the hypervectors for a state and a symbol. Eight hypervectors corresponding to all possible combinations form a basis for constructing a third, heteroassociative, item memory, i.e., the memory where the address and content parts store different hypervectors. The heteroassociative item memory can implement any table of behaviour by using the bound pair of state and symbol as input to the memory and issuing hypervectors, which should be used as the tape content, head’s move, and next state as an output. Table III presents the heteroassociative item memory for the table of behaviour of (2,4) Turing machine. Thus, three item memories constitute the static part of the system, which is generated only once at the initialization. At this point, it is worth making a note that in addition to the standard assumptions about unlimited time and memory resources, there is an extra assumption about the heteroassociative item memory. In particular, it should be guaranteed to behave correctly in the absence of external errors. Practically, it means that the address part of the heteroassociative item memory should not have repeated entries. Even for moderate dimensionality of hypervectors the chance of such an event is low but if this happens the issue is solved by the regeneration of the item memories.

2) VSAs-based tape: Another part of the system is dynamic and includes the location for storing a hypervector for the current state, the tape, and current position of the head. Fig. 10 presents an example of the dynamic part of the system. In the case of using VSAs, the tape can be seen as a matrix where each column corresponds to a hypervector of some symbol. In order to make the next step, the machine has to read the hypervector of the current state ($b$ in Fig. 10) and the hypervector of the symbol at the current location of the head ($0$ in Fig. 10). The result of multiplication of these hypervectors $b \odot 0$ is used as an input to the heteroassociative memory. The output of the memory indicates that hypervector $a$ should be written to the current state; the tape’s content is changed to $3$, and the head should be moved to the right of the current location. The updated state is shown in Fig. 11. In such a manner, the system could operate on the tape for the required number of computational steps.

3) Scaling VSAs implementation: Since the proposed implementation of a Turing machine does not make use of the addition operation, there is no crosstalk noise being introduced to the computations, which in turn means that in the absence
of external noise the emulation behaves in a deterministic way. Thus, even tiny three-dimensional vectors can be used to construct the heteroassociative item memory with unique entries. Nevertheless, since one of the arguments in favour of VSAs is their built-in tolerance to errors, it is interesting to observe the behaviour of the emulation in the presence of external noise. We performed simulations where the external noise was added to the tape by randomly flipping signs of a fraction of positions of hypervectors. Fig. 12 presents the average dimensionality of hypervectors required to make at least $10^7$ error-free updates of the emulated Turing machine when the hypervectors representing symbols on the tape were subject to external bit flips. The Bit Error Rate varied in the range $[0.05, 0.30]$ with step 0.05. The starting dimensionality of hypervectors was $2^4$. If the error in emulation was happening in less than $10^7$ steps, then the dimensionality was increased by 10%. The results demonstrate that the proposed VSAs-based implementation can perfectly emulate the Turing machine conditional on adequate resources (i.e., dimensionality of hypervectors). Naturally, in the presence of external noise, more resources are needed to obtain the error-free execution of the machine. Nevertheless, an important observation is that the VSAs-based implementation works with imprecise noisy representations. Moreover, the robustness of the implementation comes at no cost in terms of design, as the same algorithm is being used for any amount of noise and the only cost to be paid is in the increased size of the system.

**B. Emulation of cellular automaton with VSAs**

Since VSAs are designed to create vector representations of symbolic structures, when identifying a Turing complete system suitable for emulation with VSAs it is also natural to choose a highly structured system, which uses a small finite alphabet of symbols. We think that an elementary cellular automaton is such a system. Since the elementary cellular automaton with rule 110 is known to be Turing complete [Cook, 2004] we simply need to demonstrate how VSAs can be used to emulate this rule. In order to do so, we first revisit the elementary cellular automaton concept. Next, we present a VSA algorithm for mapping and executing an elementary cellular automaton.\(^2\) Thus, we literally follow the roadmap from [Cook, 2004]: “The automaton itself is so simple that its universality gives us a new tool for proving that other systems are universal”. Finally, we explore how VSAs are scaling with respect to the size of the initial grid state of an elementary cellular automaton, the dimensionality of hypervectors, and the amount of noise present during the computations. The major point of the latter is that even for large amount of noise the VSAs-based system can perfectly emulate the elementary cellular automaton given sufficiently large dimensionality of hypervectors, which is a nice property as the robustness is achieved without modifying the design.

1) Elementary cellular automata: An elementary cellular automaton is a discrete computational model consisting of a one-dimensional grid of cells [Wolfram, 2002]. Each cell can be in one of a finite number of states (two - for the elementary automaton). States of cells evolve in discrete time steps according to a fixed rule. The state of a cell at the next computational step depends on its current state and states of its neighbors. The computations performed by an elementary cellular automaton are local. The new state of a cell is determined by previous states of the cell itself and its two neighboring cells (left and right). Thus, only three cells are involved in a computation step, i.e., for binary states, there are in total $2^3 = 8$ combinations. A rule assigns states for each of eight combinations. Fig. 13 presents all combinations and the corresponding states for rule 110.

2) VSAs algorithm for emulating an elementary cellular automaton with rule 110: We use the Multiply-Add-Permute model described above. In order to represent an elementary cellular automaton with rule 110, we first create two item memories populated with random hypervectors. One item memory stores the finite alphabet, i.e., it includes only two hypervectors for one and zero (denoted as $1$ and $0$), respectively. Another item memory stores hypervectors for positions. Since an elementary cellular automaton relies only on a cell in focus and its immediate neighbors, then three hypervectors: $1$ (left), $c$ (center), and $r$ (right) are sufficient. These item memories are used to construct a hypervector for each combination of states in three consecutive cells. The hypervector is constructed by applying the addition operation on the bound pairs of a positional hypervector and an alphabet hypervector. In other words, the current states in three consecutive cells are represented as a set of unordered pairs. For example, for 010 the corresponding compound hypervector is constructed as:

$$h_{010} = [1 \odot 0 + c \odot 1 + r \odot 0].$$

\(^2\)Note that here we mainly focus on how to evolve VSAs representations to perform computations leaving aside the aspect of determining when to stop the computation.

| TABLE IV |
|-------------|
| **THE HETEROASSOCIATIVE ITEM MEMORY IMPLEMENTING RULE 110.** |
| Address (input) | Content (output) |
|-----------------|------------------|
| $h_{111}$       | $[1 \odot 1 + c \odot 1 + r \odot 1]$ | 0 |
| $h_{110}$       | $[1 \odot 1 + c \odot 1 + r \odot 0]$ | 1 |
| $h_{101}$       | $[1 \odot 1 + c \odot 0 + r \odot 1]$ | 1 |
| $h_{100}$       | $[1 \odot 1 + c \odot 0 + r \odot 0]$ | 0 |
| $h_{011}$       | $[1 \odot 0 + c \odot 1 + r \odot 1]$ | 1 |
| $h_{010}$       | $[1 \odot 0 + c \odot 1 + r \odot 0]$ | 1 |
| $h_{001}$       | $[1 \odot 0 + c \odot 0 + r \odot 1]$ | 1 |
| $h_{000}$       | $[1 \odot 0 + c \odot 0 + r \odot 0]$ | 0 |
All eight compound hypervectors form a basis for constructing a heteroassociative item memory, which can implement any elementary rule by using the compound hypervectors as input to the memory and issuing either 1 or 0 (determined by the rule) as an output. Table IV presents the heteroassociative item memory for rule 110. Thus, three item memories constitute the static part of the system, which is generated only once at the initialization.

Another part of the system performs computations for a given initial grid state of length \( l \) at time \( t = 0 \). The initial grid state is mapped to a compound hypervector (denoted as \( \mathbf{a}_0 \)). The mapping is done by applying the addition operation on all hypervectors representing the states of cells at all positions. Position \( j \) in the grid is represented by applying the permutation operation \( j \) times to the hypervector corresponding to a state at position \( j \). Thus, this representation corresponds to the mapping of a sequence with the addition operation. For example, if the initial grid state is 10101, then the representation of the state at the fifth position is \( \rho^5 \mathbf{1} \) while the compound hypervector for the initial grid state is:

\[
\mathbf{a}_0 = [\rho^0 \mathbf{1} + \rho^2 \mathbf{0} + \rho^3 \mathbf{1} + \rho^4 \mathbf{0} + \rho^5 \mathbf{1}].
\]

Given \( \mathbf{a}_0 \), the next step is to compute \( \mathbf{a}_1 \) or in general compute \( \mathbf{a}_{t+1} \) given \( \mathbf{a}_t \).

First, \( \mathbf{a}_{t+1} \) is initialized to be an empty hypervector. Next, for each position \( j \) ranging from 1 to \( l \) we do the following (this step can be either serial or parallel):

- Approximately recover the states at \( j \) and its neighbors as \( \mathbf{h} = [\mathbf{1} \circ \rho^{(-1)} \mathbf{a}_t + \mathbf{c} \circ \rho^{-2} \mathbf{a}_t + \mathbf{r} \circ \rho^{-(j+1)} \mathbf{a}_t] \).
- Use \( \mathbf{h} \) as the query to the heteroassociative item memory.
- The memory returns the content (i.e., \( \mathbf{0} \) or \( \mathbf{1} \)) for the address closest to \( \mathbf{h} \) in terms of dot product. The returned content is denoted as \( \mathbf{v}_j \).
- Increment \( \mathbf{a}_{t+1} \) with \( \mathbf{v}_j \) as: \( \mathbf{a}_{t+1}^j = \rho^j \mathbf{v}_j \).

Finally, the majority rule is applied on \( \mathbf{a}_{t+1} \): \( \mathbf{a}_{t+1} = [\mathbf{a}_{t+1}] \) so it becomes bipolar. In such a manner, the system could iterate through the grid for the required number of computational steps.

Last but not least, it is worth noting that the full computational system has its control architecture that is responsible for initializing the grid state as well as for running the for-loop, which can be seen as a recurrent connection, required for constructing \( \mathbf{a}_{t+1} \). In the experiments below, it is assumed that the control architecture functions without errors.

3) Scaling VSAs emulation: It is known that compound hypervectors can be used to retrieve their components (Section III-C), however, there is a limit on the number of components, which can be stored in a compound hypervector without losing the ability to recover the components [Frady et al., 2018b]. The rule of thumb is that for larger hypervector dimensions more components can be recovered from a compound hypervector. For the task of emulating an elementary cellular automaton it is important that \( \mathbf{h} \) is close enough to the correct state hypervector in the item memory. Otherwise we will introduce errors to the computations being emulated, which is highly undesirable. When constructing \( \mathbf{h} \) the main source of noise is the crosstalk noise from other cell states stored in \( \mathbf{a}_t \). Therefore, in order to avoid errors in the computations, the dimensionality of hypervectors should depend on the length of the grid: the longer is the grid, the larger dimensionality is required for robustly querying the item memory.\(^3\)

Fig. 14 presents the empirical results for a range of \( l \) and \( N \) values. The curves depict the average error rate after 100 computational steps of the elementary cellular automaton. Note that the errors occurring at the earlier computational steps

\(^3\)In principle, it should be possible to analytically find the minimal dimensionality of hypervectors for robustly emulating the grid of the given length.
will most likely multiply and propagate to the successive steps. The length of the grid, \( l \), varied as \( 2^i \), \( i \in [5, 10] \) while the dimensionality of hypervectors, \( N \), varied as \( 2^i \), \( i \in [10, 17] \). Thus, the results demonstrate that VSAs can perfectly emulate the elementary cellular automaton with the grid of the given length conditional on adequate resources (i.e., dimensionality of hypervectors).

Note that Fig. 14 presented the results for the case when hypervectors do not include any external noise. Since one of the arguments in favour of VSAs is their built-in tolerance to errors, it is interesting to observe the behaviour of the emulation in the presence of external noise. External noise was added by randomly flipping a fraction of positions in \( \mathbf{a} \). Fig. 15 presents the average error rate after 100 computational steps of the elementary cellular automaton in the presence of external noise. The bit error rate, \( p \), varied as \( 2^{-i} \), \( i \in [2, 5] \). The length of the grid was fixed to \( l = 32 \).

The results demonstrate that the proposed VSAs-based system can perfectly emulate the elementary cellular automaton with the grid of the given length conditional on adequate resources (i.e., dimensionality of hypervectors). Naturally, in the presence of external noise, more resources are needed to obtain the error-free emulation. Nevertheless, an important observation is that the VSAs-based system works with imprecise resources (i.e., dimensionality of hypervectors). Naturally, in Multiply–Add–Permute model [Gayler, 1998]. Here, we enumerate the properties assuming that the seed hypervectors are bipolar.

### B. Properties of the multiplication operation

- Multiplication is commutative: \( \mathbf{a} \circ \mathbf{b} = \mathbf{b} \circ \mathbf{a} \);
- Multiplication distributes over addition: \( \mathbf{c} \circ (\mathbf{a} + \mathbf{b}) = \mathbf{c} \circ \mathbf{a} + \mathbf{c} \circ \mathbf{b} \);
- Multiplication is invertible: \( (\mathbf{a} \circ \mathbf{b}) \circ \mathbf{b} = \mathbf{a} \) (bipolar \( \mathbf{b} \) is self-inverse). If multiplication is used for binding, the inverse operation is called releasing or unbinding;
- Multiplication is associative: \( (\mathbf{a} \circ \mathbf{b}) \circ \mathbf{c} = \mathbf{a} \circ (\mathbf{b} \circ \mathbf{c}) \);
- The result of multiplication is dissimilar to each of its argument hypervectors: \( \langle (\mathbf{a} \circ \mathbf{b}), \mathbf{a} \rangle \approx \langle (\mathbf{a} \circ \mathbf{b}), \mathbf{b} \rangle \approx 0 \), hence multiplication is a “randomizing” operation;
- Multiplication preserves similarity: \( \langle (\mathbf{c} \circ \mathbf{a}), (\mathbf{c} \circ \mathbf{b}) \rangle = \langle \mathbf{a}, \mathbf{b} \rangle \).

### C. Properties of the addition operation

- Addition is invertible: \( (\mathbf{a} + \mathbf{b}) + (\mathbf{b} - \mathbf{a}) = \mathbf{a} \); for normalized addition: \( \langle (\mathbf{a} + \mathbf{b}) + (\mathbf{b} - \mathbf{a}), \mathbf{a} \rangle > 0 \);
- In contrast to multiplication and permutation operations, the result of addition \( \mathbf{z} = \mathbf{a} + \mathbf{b} \) (often called the superposition hypervector) is similar to each of its argument hypervectors: i.e., the dot product between \( \mathbf{z} \) and \( \mathbf{a} \) or \( \mathbf{b} \) is greater than 0, \( \langle \mathbf{z}, \mathbf{a} \rangle > 0 \) and \( \langle \mathbf{z}, \mathbf{b} \rangle > 0 \);
- Addition is commutative: \( \mathbf{a} + \mathbf{b} = \mathbf{b} + \mathbf{a} \);
- Normalized addition is approximately associative: \( \langle \mathbf{a} + \mathbf{b} + \mathbf{c} \rangle \approx [\mathbf{a} + (\mathbf{b} + \mathbf{c})] \).

### D. Properties of the permutation operation

- Permutation is invertible: \( \rho^{-1}(\rho(\mathbf{a})) = \mathbf{a} \);
- In Multiply–Add–Permute model, permutation distributes over both multiplication and addition: \( \rho(\mathbf{a} \circ \mathbf{b}) = \rho(\mathbf{a}) \circ \rho(\mathbf{b}) \) and \( \rho(\mathbf{a} + \mathbf{b}) = \rho(\mathbf{a}) + \rho(\mathbf{b}) \);
- Similar to the multiplication operation, a random permutation \( \rho \) results in a vector that is dissimilar to the argument hypervector: \( \langle \rho(\mathbf{a}), \mathbf{a} \rangle \approx 0 \), hence permutation is a “randomizing” operation;
- Permutation preserves similarity: \( \langle \rho(\mathbf{a}), \rho(\mathbf{b}) \rangle = \langle \mathbf{a}, \mathbf{b} \rangle \).