Bandstructure Effects in the Electronic Transport of Silicon Nanowire in [100] and [110] Transport Orientations

Manoj Kumar*, Vijay Kumar Lamba*
BRCM College of Engineering and Technology, Bahal, Bhiwani (India)
Global College of Engineering & Technology, Kahanpur Khui, Punjab (India)
E-mail: manoj10276@gmail.com

Abstract. An electronic transport study about band structure effects of silicon nanowire (SiNW) in [100] and [110] transport orientations has been done. A dispersion calculation has also been done for a sp/ds hybridized atomistic model along with a Poisson solver. A ballistic model has been used for the evaluation of I-V characteristics. For [100] and [110] transport-oriented nanowires, the total gate capacitance was decreased by 30%. The carrier velocity was affected by both [100] and [110] transport-oriented nanowires. The velocities depend on degeneracy and effective mass of the dispersion. In our study, we have used 3nm thick nanowire oriented in [100] and [110] directions. The [100] oriented nanowire gives better ON-current performance as compared to [110] oriented nanowire. We have studied the valley splitting effects which can lift the degeneracies of 3nm wires. The effective mass which changes with various transport orientations and quantization, was increased with quantization for [100] while it was decreased for [110] transport orientated nanowire.

Index-Terms: silicon nanowire, tight binding, band structure, injection velocity, nano FETs, effective mass, quantum capacitance.

1. Introduction
As the sizes of transistor required being of nanoscale, the development of CMOS finds an alternative place in the designing of different structures and devices. The CMOS transistors that were developed from planar technology nowadays were used as nanodevices. The use of nanowire devices has made a good attention due to its possibility of enhanced electrostatic control. Different experimental results show that the nanowire transistors below 3nm size have been designed [1]. With the device’s dimension going down, the lattice structure, bonding between the atoms were affected. Therefore, a good molecular modeling was required so that the nanowire device should provide an accurate electrical characteristic.

In our work, we had used the atomistic model (sp/ds*) along with a 2D Poisson Solver to calculate the electronic structure of the silicon nanowire. The band structure parameters which affected the properties of silicon nanowires were also identified [2]. To calculate the transport properties of silicon nanowire, a basic semi-classical ballistic model, shown in figure 1 was utilized [3]. In our work, we have taken silicon nanowire of 3 nm width, which were oriented in [100] and [110] transport direction to study and compare the transport characteristics. 2D Poisson solver shown in figure 1 has been used to calculate the electrostatic potential variation in the lattice structure.

While examining the silicon nanowire transport characteristics, the potential variation in the cross section of nanowires played a criticizing role. This factor causes just little shifting of the energy levels, yet the placement of the charge was affected by it. The capacitance of the device was decreased by 30% due to charge placement along with density of states in silicon nanowires and this reduction was
same for both [100] and [110] transport directions. The device performance was controlled by the injection velocity and the orientation of the nanowire. The transport mass controls the orientation velocity and orientation controls the degeneracy. The [110] oriented devices with a lowest mass and highest carrier injection velocity were best suitable for charge transportation in small nanowires than [100] orientated devices with a little higher mass [4]. The [100] and [110] transport directions and structural quantization works on the transport masses and degeneracy [5].

1.1. Need of atomistic modelling:
The atomistic effects were not usually captured by effective mass approximation (EMA) method. The atomistic description of the devices actually captures the valley projections and extracts dispersion of the oriented nanowires. The problem on correct band structure and effective masses of nanowires has been discussed in references [6-7]. The main features on the electronic structure have also been discussed [8]. In the electronic structure calculation techniques, the mass variation in nano structure has been described [9]. The mass variation in nano structure resulted in various threshold voltages. The effective mass approximation method could be used especially for [100] oriented nanowire for the calculation of conduction band only. As already discussed, the EMA method was not always valid, so the more useful method for nanowire of few nanometers was the atomistic simulation method.

In our work, we have used Tight Binding (TB) model for which we have described its simulation approach. We have described its simulation approach. We have described the behavior of band structure of the lattice for 3nm cross-section square nanowires of [100] and [110] orientations. Nanowire’s performance in terms of injection velocity, quantum capacitance, drive current capabilities and gate capacitance for [100] and [110] oriented nanowires has been described.

![Figure 1(a): semi classical ballistic model](image)

2. Methodology
2.1. Why we have selected Tight Binding (TB) model:
As we know that the MOS technology has come to saturation point, the requirements for new technology at nanoscale was to find new material and new devices. The quantum mechanics of the atomic composition and atomic structure had to be examined. For that an atomic structure model which may meet the requirement of nanoscale device was required. In a typical semiconductor device, the stability of bands allows the requirement of a reduced model. The hetero-structure model requires a nearest neighbor model. To simulate larger structures containing a large no. of atoms, there was a need of a reduced model [10]. To accurately model band gaps within a few mV, there occurs a requirement of an empirical band structure model. To fulfill all the above requirements, an empirical Tight Binding (TB) model was the best choice.

2.2. The sp3d5s* TB Model:
In our work, we have used sp^d^s* nearest neighbor model made up of orthogonal localized orbital. This model was best suited model for electronic structure of nanometer scaled nanostructures. This model can be used to treat potential variations and materials at nanoscale. The main feature of this method was that by using genetic algorithm, the band edges of silicon band structure can be reproduced by extracted parameters. The explanation of this model was given in reference [11]. Energy bands drawn from this model for the nanowires were up to the requirements as compared with the theoretical calculations using ab-initio method. For charge self-consistency, the electrostatic potential was used in the Hamiltonian equation for shifting the bands.

2.3. Verification of Model:
As the accuracy of the results were required and since the accuracy will depend on the verification of the model we were using. The verification of model has been done by using the calibration parameters to explain the experimental data. Some samples were used e.g. under high bias voltage with charge self-consistency, resonant tunnel diode was tested for transportation of charge [12-13]. The experimental data for valley splitting, band gap of nanowires and electronic structures of silicon nanowires compared with the results given by the Tight Binding (TB) model [14-17]. Also, the theoretical works were compared with results given by this model [18]. Especially this model validates the calculation of experimental results of band gaps of the oriented nanowires in Brillouin zone of silicon nanowire. The model also shows that anisotropy at high energy levels affects the band edges and atomic masses of nanowires.

2.4. The simulation approach:
We have used a square nanowire of 3nm x 3nm dimension. Our model device was simulated for [100] and [110] transport orientations. The simulation process was done using these following steps:
First of all, by using atomistic Tight Binding (TB) model, we calculated the band structure of the nanowire. All the edges in lattice structure (Zincblende lattice) was shown by sp^3 hybridization (sp^d^s*) in Hamiltonian wire. Only conduction band was considered for study. The accuracy of the results was not affected, and this model was perfect for computational efficiency. The sp^3 hybridization scheme was used in which the atoms were persisted on the surface of nanowires. This technique was very useful for removing those bonds which could make surface state with eigen – energies in band gaps of the device. The channel atoms were available for atomistic calculations. The model uses dispersion state energy for computation. We have studied the band structure effects such as effective mass variation, valley splitting of the [100] and [110] transport-oriented nanowire.
Secondly, we have used a semi-classical ballistic model for computation of transport characteristics and to fill the dispersion state. This model makes use of drain Fermi level to fill negative going states and source Fermi level to fill the positive going state. Then the charge distribution takes place in all the orbitals of the shells using their wave functions when the dispersion state occupancy was computed.
Thirdly, the electrostatic potential was obtained by 2D Poisson equation with the help of charge distribution. 2D Poisson equation was solved in 2D plane. Also, in 2D plane, atomic locations were collapsed. The Poisson domain contains the nanowire core, dielectric and metal. The diagonal elements of Hamiltonian matrix were added with the electrostatic potential to re-calculate the band structure for achieving self consistency. The dielectric present in Poisson domain was believed to be of SiO of 1.1nm thick layer, was not included in the Hamiltonian. Due to the potential difference, any effects produced by the transport orientations were not considered. It has also been studied that the carrier injection was very essential for the transport properties of nanowires.
Our study of transport model explains that the ballistic transport characteristics will be affected by the band structure of nanowires. 3D quantum non-equilibrium green function (NEGF) simulation also provides the same results. The results of our study will be valid for other nanowire dimensions, as our results shows that the electronic properties of nanowires were dependent upon the quantization size, not on quantization shape.
3. Results and Discussions

3.1. How nanowire dispersion and charge distribution was affected by potential variation:

3.1.1. Dispersion characterization in [100] oriented nanowires: Figure 1a shows dispersion in [100] oriented nanowire. It shows four-fold valleys at $\Gamma$ which was at a distance of $k_x = 0$ and was projected from four silicon ellipsoids. These ellipsoids reside in a quantized plane. From figure 1a, two more valleys can be seen which were available away from $\Gamma$. The position of two valleys was opposite to each other. One was in positive side of k-axis and another resides in the negative side.

Out of four valleys, first two were seen lower in energy level due to their light transport mass ($m=0.19 \text{ m}_0$) and heavy quantization mass ($m=0.89\text{ m}_0$), where $m$ and $m_0$ were nanowire masses.

3.1.2. Potential variations change the dispersion of [100] oriented nanowire: Our results shows how potential variations can change the dispersion of the oriented nanowires. It was also shown how shape of lattice was changed when it was filled up with charge. Figure 1 shows the effects of low and high gate voltages on 3nm square [100] oriented nanowires. We have used drain voltage, $V_d = 0.5\text{ V}$. Lattice was approximately charge less and dispersion was stable, when gate voltage applied was low. Charge filling in lattice occurs when high gate voltage was applied. Charge distribution also comes into a shape of inversion layer. When inversion layer becomes high, our results show that the wave function was displaced by 0.5nm apart from Si/Sio interface. The dispersion was considered to be a material parameter and it was independent of charge filling of lattice.

Due to the charge filling in lattice structure, there occurs a change in dispersion of 3nm nanowire length. Here a small change in dispersion occurs but as wave function was associated with it, so it increases the charge distribution. As a result, the transport characteristics and the capacitance of device were affected.

3.1.3. Orientation variances in the velocity: Our simulation result shows that the lighter mass (0.16m) produces highest velocity in [110] oriented nanowire. The velocity increases when higher $k$-states got filled. When Fermi level entered the conduction band as shown in figure 2, the carrier velocity in the [100] oriented nanowire becomes equal to the velocity of [110] oriented nanowire. The heavier mass (0.27m) in [100] oriented nanowire $\Gamma$ valley was taken over by the lighter masses (0.16m) in [110] oriented nanowire’s $\Gamma$ valley. When heaviest four-fold deviate off- $\Gamma$ valleys of the device [110] start to populate with the heavy two fold deviate off-$\Gamma$ valley of the device [100], a factor known as carrier velocity gets looks alike. Our study analysis told that [100] oriented nanowire and [110] oriented nanowire has different properties.
3.2. Performance analysis of device for nanowires in different orientations:

We have considered the [100] oriented nanowires comparison at same Fermi level position. For the comparison of performance of different oriented nanowires, we have used self consistent model. The performance comparison has been shown in figure 4. The comparisons for all devices have been done at same off current (1-off).

3.2.1. \( C \), controlling factors: \( C \) was referred as differentiation of charge present in nanodevice w.r.t. surface voltage \( (\psi S) \). This charge was integral of convolution of density of states \( (g _{n}) \) and Fermi function \( (f (E, - E)) \),

\[
\frac{\Omega_{2}}{\Omega_{1}} = \int_{5q_{s}}^{5q_{d}+5q_{g}+5q_{s}} dE
\]

where \( q \) was charge of electron, \( E \) was Fermi level, \( \psi \) was the surface potential, \( E \) was conduction band energy, and \( \epsilon \) was separation of \( i^{th} \) sub-band above \( E \). Moving to coordination, the conditions above outcomes was:

\[
C_{B} = \int_{0}^{B} g_{1} m_{1}^{2} \sqrt{\pi} \frac{1}{\epsilon} \left( \sum_{q_{1} = 1}^{4} 5\epsilon_{q}^{2}\epsilon_{q}^{2} \right)
\]

\[
= \int_{0}^{B} \frac{D_{1}^{2} \epsilon_{1}^{2}}{C_{G}^{F}} \sqrt{\pi} \frac{1}{\epsilon} \left( \sum_{q_{1} = 1}^{4} 5\epsilon_{q}^{2}\epsilon_{q}^{2} \right)
\]

\[
= \frac{V}{1 - \frac{\epsilon_{G}}{\epsilon_{1}}}
\]

In Eqn. 1d, \( C \) represents quantum capacitance. At Fermi level, it was a measure of the thickness of Density of states. From equation, we see that the changes in \( \epsilon \) correspond to decrease in \( C \) from \( C \). Ideally \( \epsilon \) should be constant at high inversion conditions which mean that conduction band energy level, \( E \) and quantization level shifts by same amount. At this condition, sub bands level reaches at Si/SiO interface. Due to this, wave function comes closer to interface. As charge was accumulated in the device, \( E \) floats up. It corresponds to a differential term in equation 1d and wave function shift from interface. Besides shifting of wave function, \( C \) being small becomes decreasing factor of \( C \), as shown in equation 1d. \( C \) in both [100] and [110] nanowires, being measured at Fermi level, was a function of gate bias, \( V \). We found a large significance of the position of charge distribution on the performance of a device in the fact that it degrades \( C \) from \( C \) by four-times.
3.2.2. Variance in \( C_Q \) between [100] and [110] oriented nanowires: \( C_Q \) was not constant even it shows a large transition at large gate voltages when Fermi level was thrown into the sub bands for both [100] and [110] oriented nanowire cases. This was right because dispersion causes difference in \( C_Q \) and also at the Fermi level, \( C_Q \) was a source of density of states. When we compare the \( C_Q \) for different oriented wires, we found that [110] oriented nanowire has more \( C_Q \) because of high degeneracy of its valleys (\( D=6 \)) and higher masses (0.47m) for all gate bias ranges while [100] oriented nanowire has less \( C_Q \) because of low degeneracy and light mass (less density of state). The [100] oriented nanowire gets populated when a high gate bias was applied as shown in figure 3. As a result, a continuous increase in \( C_Q \) takes place. At a lower gate voltage, the Fermi level in the [110] nanowire, the smaller valley degeneracy’s and lower mass reaches the upper valleys faster as compared to [100] nanowire. As a result, the \( C_Q \) of [110] nanowires crosses the \( C_Q \) of [100] nanowire at gate voltages around 0.4V (\( V_G = 0.4V \)).

![Figure 3(a): C\(_Q\) vs. \( V_G \) plot for two devices](image)

![Figure 3(b): I\(_D\) vs. \( V_G \) plot for two wires having same value of I.](image)
3.2.3. *I-V characteristic was affected by velocity differences:* Velocity was totally relied on $I_{ds}$. A comparison between [100] and [110] nanowires for current driving capabilities has been done at same $I_{ds}$. In terms of ON-current capabilities, [110] nanowire performs better it gives 5% better ON-current capability than [100] nanowire because of its lower mass. The results generated by 3nm nanowires must be taken into consideration as band structure of nanowires depends on their quantization.

3.3. *Mass variation, valley splitting was affected by quantization:* The device performance was controlled by mass variation and valley splitting that lifts degeneracy’s and these two parameters were affected by quantization. So we can say that device performance was controlled by quantization. In our study, we have examined the effects of quantization.

3.3.1. *Weak valley splitting in [100] quantized nanowire:* Energy Vs wave vector (E-k diagram) graph of a 3nm nanowire in [100] and [110] orientation has been shown in figure 2a-2b. A little valley splitting under quantization has been examined. For [100] oriented nanowire, it was 10meV. Even the room temperature value (26meV) was greater than this value, so the transport properties will not be affected at room temperature.

3.3.2. *Strong valley splitting in [110] quantized nanowire:* The valley splitting was larger in [110] oriented nanowire. Figure 4c, shows the splitting of 76meV at $\Gamma$ valley and 14meV off-$\Gamma$ valley. The larger nanowires greater than 5nm were not affected. The value of splitting may attain 200meV at $\Gamma$ valley in 1.5nm narrow nanowires. The splitting values off-$\Gamma$ valley were not being affected so much. Very little splitting of a few tenths of meV was seen in this case.

3.3.3. *With increase in quantization the $\Gamma$ valley mass of [110] oriented nanowire decreases:* The [110] nanowire $\Gamma$ valley mass decreases as compared with the rest of the valleys, when quantization, was increased. Figure 4b shows the mass reduction of 32% when thickness of nanowire reduces from 7.1nm to 1.5nm.

![Figure 4a: nanowire thickness vs. transport mass at conduction band minima](image-url)
4. Conclusion

A sp3d5* hybridized atomistic model along with a Poisson solver was used to examine transport properties of [100] and [110] transport oriented nanowires. The I-V characteristics of the nanowires were calculated using a semi classical ballistic model. The dispersion of the nanowires which could shift the degeneracy’s and shift the sub bands, was changed when gate bias was changed. These changes couldn’t change the density of states and velocity of the nanowires but the nanowire’s capacitance could be decreased by 30% by the charge distribution and density of states. The quantum capacitance was found to be of same magnitude in both [100] and [110] oriented 3nm nanowires depended on gate voltage. It was found largest for [110] oriented nanowires because of higher degeneracy and higher mass for all gate voltages. The gate capacitance was same in both [100] and [110] oriented nanowires and the inversion charge was also same. The [110] oriented nanowires have lower injection velocity because of their bigger masses whereas [100] nanowire have maximum injection velocity due to their lighter masses. The current capabilities of the nanowires were reflected by the injection velocities. The ON-current capabilities represented the best performance of the device. The [100] oriented nanowire gave the best performance while [110] nonowire gave worst performance as compared to [100] nanowire. The effective mass of nanowires was a function of nanowire’s cross-section. When the dimension of nanowire was decreased from 7.1 to 1.5nm, [100] oriented nanowire mass became almost double. Valley splitting was dependent on quantization. With increase in
quantization, the [110] nanowire valley mass was decreased as compared with rest of valleys. The [110] oriented nanowire of dimension below 3nm were very sensitive to the splitting valley.

References

[1] Xiang, J., Lu, W., Hu, Y., Wu, Y., Yan, H. and Lieber, C.M., (2006), “Ge/Si Nanowire Heterostructures as High-Performance Field-Effect Transistors,” Nature, 441(7092), pp. 489.
[2] Boykin, T. B., Klimeck, G. and Oyafuso, F., (2004), “Valence Band Effective-Mass Expressions in the $sp^d$* Empirical Tight-Binding Model Applied to a Si and Ge Parametrization,” Physical Review B, 69(11), pp. 115201-115210.
[3] Rahman, A., Guo, J., Datta, S. and Lundstrom, M. S., (2003), “Theory of Ballistic Nanotransistors,” IEEE Transactions on Electron Devices, 50(9), pp. 1853-1864.
[4] Luisier, M., Schenk, A. and Fichtner, W., (2007), “Full-band atomistic study of source-to-drain tunneling in Si nanowire transistors,” Proc. Simulation of Semiconductor Processes and Devices, T. Grasser et al., eds., Springer, Vienna, Austria, pp. 221-224.
[5] Boykin, T. B., Klimeck, G., Friesen, M., Coppersmith, S. N., von Allmen, P., Oyafuso F., and Lee, S., (2004), “Valley splitting in low-density quantum confined heterostructures studied using tight-binding models,” Phys. Rev. B, 70(16), pp. 165325.
[6] Luisier, M., Schenk, A., Fichtner, W. and Klimeck, G., (2006), “Atomistic simulation of nanowires in the $sp^d$* tight-binding formalism: From boundary conditions to strain calculations,” Physical Review B, 74(20), pp. 205323.
[7] Gnani, E., Reggiani, S., Gnudi, A., Parruccini, P., Colle, R., Rudan, M. and Baccarani, G., (2007), “Band-structure effects in ultrascaled silicon nanowires,” IEEE Transactions on Electron Devices, 54(9), pp. 2243-2254.
[8] Wang, J., Rahman, A., Ghosh, A., Klimeck, G. and Lundstrom, M., (2005), “On the validity of the parabolic effective-mass approximation for the IV calculation of silicon nanowire transistors,” IEEE Transactions on Electron Devices, 52(7), pp. 1589-1595.
[9] Neophytou, N., Paul, A., Lundstrom, M. S. and Klimeck, G., (2008), “Simulations of nanowire transistors: Atomistic vs. effective mass models,” Journal of Computational Electronics, 7(3), pp. 363-366.
[10] Klimeck, G., Ahmed, S. S., Bae, H., Kharche, N., Clark, S., Haley, B., Lee, S., Naumov, M., Ryu, H., Saiied, F. and Prada, M., (2007), “Atomistic simulation of realistically sized nanodevices using NEMO 3-D—Part I: Models and benchmarks,” IEEE Transactions on Electron Devices, 54(9), pp. 2079-2089.
[11] Klimeck, G., Oyafuso, F., Boykin, T. B., Bowen, R. C. and von Allmen, P., (2002), “Computer Modeling in Engineering and Science (CMES),” Proc. Simulation of Semiconductor Processes and Devices, T. Grasser et al., eds., SpringerWien, NewYork, 3(5), pp. 601-642.
[12] Bowen, R. C., Klimeck, G., Lake, R., Frensky, W. R. and Moise, T., (1997), “Quantitative resonant tunnelling diode simulation,” J. Appl. Phys, 81, pp. 3207-13.
[13] Bowen, C., Fernandez, C. L., Klimeck, G., Chatterjee, A., Blanks, D., Lake, R., Hu, J., Davis, J., Kulkarni, M., Hattangady, S. and Chen, I. C., (1997), “Physical oxide thickness extraction and verification using quantum mechanical simulation,” In Electron Devices Meeting (IEDM’97), Technical Digest, pp. 869-872.
[14] Ma, D. D. D., Lee, C. S., Au, F. C. K., Tong, S. Y. and Lee, S. T., (2003), “Small-diameter silicon nanowire surfaces,” Science, 299(5614), pp. 1874-1877.
[15] Zhao, X., Wei, C. M., Yang, L. and Chou, M. Y., (2004), “Quantum confinement and electronic properties of silicon nanowires,” Physical review letters, 92(23), p. 236805.
[16] Kharche, N., Prada, M., Boykin, T. B. and Klimeck, G., (2007), “Valley splitting in strained silicon quantum wells modeled with 2 miscuts, step disorder, and alloy disorder,” Applied Physics Letters, 90(9), p. 902109.
[17] Liang, G., Xiang, J., Kharche, N., Klimeck, G., Lieber, C. M. and Lundstrom, M., (2007), “Performance analysis of a Ge/Si core/shell nanowire field-effect transistor,” Nano letters, 7(3), pp. 642-646.
[18] Lee, S., Oyafuso, F., Von Allmen, P. and Klimeck, G., (2004), “Boundary conditions for the electronic structure of finite-extent embedded semiconductor nanostructures,” Physical Review B, 69(4), p. 045316.