Analog/RF Performance of Triple Material Gate Stack-Graded Channel Double Gate-Junctionless Strained-silicon MOSFET with Fixed Charges

Suddapalli Subba Rao · Rani Deepika Balavendran Joseph · Vijaya Durga Chintala · Gopi Krishna Saramekala · D. Srikar · Nistala Bheema Rao

Received: 17 August 2021 / Accepted: 11 October 2021 / Published online: 29 October 2021
© Springer Nature B.V. 2021

Abstract

In this paper, analog/radio frequency (RF) electrical characteristics of triple material gate stack-graded channel double gate-Junctionless (TMGS-GCDG-JL) strained-Si (s-Si) MOSFET with fixed charge density is analyzed with the help of Sentaurus TCAD. By varying the various device parameters, the analog/RF performance of the proposed TMGS-GCDG-JL s-Si MOSFET is evaluated in terms of transconductance-generation-factor (TGF), early voltage, voltage gain, unity-power-gain frequency ($f_{max}$), unity-current-gain frequency ($f_t$), and gain-transconductance frequency product (GTFP). The results confirm that the proposed TMGS-GCDG-JL s-Si MOSFET has superior analog/RF performance compared to gate stack-graded channel double gate-junctionless (GS-GCDG-JL) s-Si device. However, the proposed MOSFET has less transconductance and less output conductance when compared with the GS-GCDG-JL s-Si device in above threshold region, and reverse trend follows in sub-threshold region.

Keywords Fixed charges · Early voltage · Strained-silicon · Short channel effects · Transconductance

1 Introduction

Nano scaled strained-silicon (s-Si) MOSFETs are promising candidates for upcoming high-speed devices on account of high field velocity, enhanced mobility, and higher driving current [1–6]. With the aid of layer transfer process [7], the strain is developed in the silicon material. In this method, the biaxial-tensile strain is introduced in silicon material by growing the silicon material on the relaxed $Si(1−X)Ge(X)$ material, which is developed on the Silicon-on-insulator (SOI) layer. When device operates in nano-scaled regime, fixed charges are created at Oxide/s-Si (SiO$_2$/s-Si) interface due to the lateral electric field in s-Si MOSFETs [8, 9]. Thereby, the performance of MOSFET deteriorates in terms of threshold voltage and channel potential.

A few authors have presented the impact of fixed charges on the electrical characteristics of double gate (DG) junctionless device [10–12]. Also, they have confirmed that the fixed charges at the SiO$_2$/s-Si interface of MOSFET can cause change in the channel potential and threshold voltage. To suppress the hot carrier effects (HCEs), the triple metal gate (TMG) engineering is introduced in DG MOSFET [13, 14]. In TMG structure, screen and control gates are used with three distinct work functions. Therefore, a step...
equivalent profile in s-Si channel potential and increase in average electric-field of s-Si channel are obtained. Hence, the performance of DG device is improved by employing the TMG structure. To further suppress HCEs, gate stack (GS) structure is also incorporated in DG MOSFET to achieve better device performance in terms of gate leakage current and drive current [15, 16]. Furthermore, graded channel (GC) engineering is employed in DG junctionless device, thus resulting in improved analog/RF characteristics owing to diminished HCEs [17, 18]. Therefore, better performance of the DG junctionless MOSFET is obtained by employing the GS with gate and channel engineering.

The analog/RF electrical characteristics of junctionless MOSFETs for low power applications was demonstrated in [19]. Moreover, enhancement in early voltage and intrinsic voltage gain are attained due to low electric field at drain end of oxide interface. In [20], the effect of laterally graded channel doping in double gate junctionless MOSFETs for analog/RF applications was presented. Besides, high cutoff frequency and high intrinsic voltage gain are obtained. In [21], the comparative analysis of DG junctionless and GS DG junctionless MOSFETs was presented. Also, the effect of doping on obtaining the optimum performance of the device was studied. In [22], the analytical modeling of leakage currents in dual material halo doped cylindrical gate junctionless MOSFET was illustrated. Till now, in literature, the analog/RF characteristics of triple material gate stack-graded channel DG-junctionless (TMGS-GCDG-JL) s-Si device with the fixed charges has not been presented. By employing the GC and GS structure with gate engineering, better analog/RF performance of junctionless s-Si DG device is achieved. In the sub-nano scaled dimensions, the proposed device can be suitable for the RF-integrated circuit and 5G/6G communication applications due to its low values of power consumption and gate capacitance, high intrinsic gain, high unity current gain frequency and large band-width.

The process flow of a proposed MOSFET as follows, firstly, the strained-Si channel is fabricated with help of hydrogen-induced and wafer bonding material transfer of strained-Si grown on bulk relaxed SiGe graded layers [7]. In the next step, GC region is achieved with the help of diffusion process by using three mask layers. Next, bottom and top gate stacks are formed by develop of the oxide material by dry thermal oxidation process at modest temperatures and deposition of triple metal gates such as screening and control gates are deposited by normal and tilt angle evaporation method, respectively. In the next step, the bottom and top gate stacks are etched and patterned, followed by drain and source areas are formed by diffusion process with activation energy at very high temperatures. Lastly, the electrodes for gate, drain, and source are created at high temperatures.

This paper demonstrates the analysis of analog/RF characteristics of TMGS-GCDG-JL s-Si device with fixed charges. The analog/RF characteristics of TMGS-GCDG-JL s-Si device is exhaustively analyzed by varying the strain ($m$), fixed charge density ($N_f$), and the thickness of high-k material (tox). Moreover, the analog figure of merits of the proposed MOSFET are evaluated in terms of transconductance generation factor ($TG\text{F} = \frac{g_m I_{ds}}{I_{ds}}$), early voltage ($\frac{V_{e}}{I_{ds}}$), and intrinsic voltage gain ($\frac{g_m}{V_{ds}}$). Besides, the RF figure of merits of the proposed device, unity current gain frequency ($f_t$), unity power gain frequency ($f_{max}$) and gain transconductance frequency product ($f_{max}$) and gain transconductance frequency product.

![Fig. 1](image_url) Symmetrical TMGS-GCDG-JL s-Si MOSFET fixed charges a. Proposed junctionless MOSFET structure b. Comparison of strained-silicon MOSFET with experimental results of the [23]
\( GTP = \left( \frac{g_m}{L_d} \right) \left( \frac{g_m}{L_d} f_t \right) \), are evaluated exhaustively. The analog/RF characteristics of the proposed junctionless s-Si MOSFET are obtained when compared to GS graded channel DG junctionless (GS-GCDG-JL) s-Si MOSFET.

Table 1

| S. No. | Variable                                      | Symbol | Values                      |
|-------|----------------------------------------------|--------|-----------------------------|
| 1     | strained-silicon channel length              | \( L \) | 15 nm                       |
| 2     | strained-silicon channel doping              | \( N_{d1}, N_{d2}, N_{d3} \) | \( 10^{18}, 5 \times 10^{17}, 10^{17} \) \( \text{cm}^{-3} \) |
| 3     | Source (Drain) doping                        | \( N_{d} \) | \( 10^{20} \) \( \text{cm}^{-3} \) |
| 4     | strained-silicon thickness                   | \( t_{s-Si} \) | 6 nm                        |
| 5     | Oxide thickness                              | \( t_{ox1}, t_{ox2} \) | 0.6, 1 nm                   |
| 6     | Work function of the control gate and screen gate | \( \phi_{m1}, \phi_{m2}, \phi_{m3} \) | 4.8, 4.6, 4.4 eV              |
| 7     | Gate to source voltage                       | \( V_{gs} \) | 0 - 1 V                     |
| 8     | Drain to source voltage                      | \( V_{ds} \) | 0 - 1 V                     |
| 9     | Ge mole fraction                             | \( m \) | 0.1 - 0.3                   |
| 10    | Fixed charges                                | \( N_f \) | \(-4 \times 10^{12} - 4 \times 10^{12} \) \( \text{cm}^{-2} \) |
| 11    | Operating frequency                          | \( f_{0} \) | 0.1 - 1000 GHz             |

2 Proposed MOSFET Structure and TCAD Setup

The simulated cross sectional view of TMGS-GCDG-JL s-Si device with fixed charges is demonstrated in Fig. 1(a). The strained-silicon graded channel region is doped with three different uniform phosphorous doping concentrations (i.e., \( N_{d1}, N_{d2}, \) and \( N_{d3} \)). Screen and control gates are used together to form bottom and top gates of TMGS-GCDG-JL s-Si device. The bottom and top gates of the GS-GCDG-JL s-Si MOSFET have a single gate layer whose work function is an average of \( \phi_{m1}, \phi_{m2} \) and \( \phi_{m3} \). Because of HCEs in nano scaled proposed s-Si junctionless MOSFET, interface charges are created at s-Si/SiO2 interface and are represented as damaged region of junctionless MOSFET, interface charges are created at s-Si/SiO2 interface and are represented as damaged region of

\[
(\Delta E_c)_{s-Si} = 0.57X, \quad (\Delta E_g)_{s-Si} = 0.4X
\]

where \( V_T \) denotes the thermal voltage, \( N_{Vs,Si} \) and \( N_{Vs,s-Si} \) represent density of states in the valence band, \( m^*_{h,Si} \) and \( m^*_{h,s-Si} \) denote the effective masses of hole in silicon and strained-silicon, respectively. Also, both flat band voltage and barrier potential of the source (drain) to channel decrease simultaneously [26].

\[
\Delta V_{fb} = \frac{E_c}{q} + \frac{E_g}{q} - V_T \ln \left( \frac{N_{Vs,Si}}{N_{Vs,s-Si}} \right),
\]

\[
\Delta V_{bi} = V_T \ln \left( \frac{N_{Vs,Si}}{N_{Vs,s-Si}} \right) - \frac{E_g}{q}
\]

where \( \Delta V_{fb} \) and \( \Delta V_{bi} \) are the changes in flat band voltage and built-in potential, respectively.

The proposed device with the fixed charges is simulated using the TCAD [27]. In the device simulation, to evaluate the analog/RF characteristics of the TMGS-GCDG-JL s-Si device with fixed charges, the following physical models are considered. The charge transport mechanism is estimated with the help of the drift diffusion model and the recombination of carriers are determined by using Auger and SRH recombination models. And also, mobility of carriers is estimated by using Enormal mobility model and high field saturation model. Moreover, the energy band gap narrowing effects are considered by the OldSlotboom model and strained-silicon characteristics are assessed by MoleFraction model. Furthermore, the effect of fixed
Fig. 2 Effect of strain in silicon channel on the transfer characteristics and $g_m$ of the TMGS-GCDG-JL s-Si device

charges at SiO$_2$/s-Si interface of the device are included with the help of Traps model and quantum mechanical effects are also assessed with the help of density gradient model [28].

3 Result Analysis

This section demonstrates the analog and radio frequency performance of the TMGS-GCDG-JL s-Si MOSFET with fixed charges using the simulation results obtained from TCAD. Figure 2 depicts the effects of $m$ on the $g_m$ and transfer characteristics of TMGS-GCDG-JL s-Si device. It is noticed from the Fig. 2 that the GS-GCDG-JL s-Si device has enhanced transport characteristics and $g_m$ compared to proposed TMGS-GCDG-JL s-Si device because of the lower threshold voltage of GS-GCDG-JL s-Si device. Moreover, increment in both ON current and $g_m$ of the TMGS-GCDG-JL s-Si device are observed in subthreshold region by increasing the $m$ because of decrease in the threshold voltage.

The variation of $t_{ox}$ on $g_m$ and transfer characteristics of TMGS-GCDG-JL s-Si MOSFET is shown in Fig. 3. When $t_{ox}$ decreases, increment in both $g_m$ and transfer characteristics of MOSFET are observed in the above threshold region because of the greater gate control over the s-Si channel than drain and reverse trend follows in weak inversion region. Besides, the gate stack that consists of HfO$_2$ in the TMGS-GCDG-JL s-Si MOSFET has better $g_m$ and transfer characteristics than the gate stack that consists of Si$_3$N$_4$ in the above threshold region and inversely in subthreshold region.

The variation of $N_f$ with $L_d$ on the transfer characteristics and $g_m$ of the proposed TMGS-GCDG-JL s-Si MOSFET is depicted in Fig. 4. The enhanced transfer characteristics of the TMGS-GCDG-JL s-Si device are attained by increasing positive $N_f$ since the threshold voltage of device decreases, and reverse trend follows for the negative $N_f$. Moreover, as positive/negative fixed charge density increases, the transconductance of TMGS-GCDG-JL s-Si MOSFET increases in sub-threshold region and reverse trend follows in strong inversion region. Hence, the analog/RF characteristics of the proposed TMGS-GCDG-JL s-Si MOSFET are affected with respect to the fixed charges at SiO$_2$/s-Si interface.

Figure 5 depicts the variation of $m$ on the output characteristics and $g_d$ of TMGS-GCDG-JL s-Si MOSFET. As strain increases, better drain characteristics and high $g_d$ of the TMGS-GCDG-JL s-Si MOSFET are attained because of decrease in the threshold voltage of proposed device.
MOSFET. It is evident from Fig. 5 that the GS-GCDG-JL s-Si device has enhanced drain characteristics and higher $g_d$ compared to the proposed TMGS-GCDG-JL s-Si MOSFET. Therefore, the proposed TMGS-GCDG-JL s-Si MOSFET has lower effect of drain to source voltage on the channel compared to the GS-GCDG-JL s-Si MOSFET.

The variation of $t_{ox2}$ on output characteristics and $g_d$ of the TMGS-GCDG-JL s-Si MOSFET is illustrated in Fig. 6. As $t_{ox2}$ decreases, $g_d$ decreases and the proposed MOSFET achieves better drain characteristics. Besides, the gate stack that consists of HfO$_2$ in the TMGS-GCDG-JL s-Si MOSFET has improved drive current and less $g_d$ than the gate stack that consists of Si$_3$N$_4$. Therefore, HfO$_2$/SiO$_2$ gate stack of proposed TMGS-GCDG-JL s-Si has better electrical characteristics and less impact of $V_{ds}$ on the channel when compared to the Si$_3$N$_4$/SiO$_2$ gate stack, as shown in Fig. 6.

Figure 7 illustrates the effect of $N_f$ with $L_d$ on output characteristics and $g_d$ of the TMGS-GCDG-JL s-Si MOSFET. Increase in output characteristics is observed by increasing the positive $N_f$ owing to reduced threshold voltage of device, and vice-versa when $N_f$ is negative. Moreover, as positive $N_f$ increases, $g_d$ of proposed device decreases, and vice-versa when $N_f$ is negative. Therefore, the proposed TMGS-GCDG-JL s-Si MOSFET with positive $N_f$ has lower impact of $V_{ds}$ on the channel compared to the GS-GCDG-JL s-Si MOSFET with negative $N_f$.

The variation of strain on TGF and intrinsic gain of TMGS-GCDG-JL s-Si is depicted in Fig. 8. As strain increases in the TMGS-GCDG-JL s-Si MOSFET, TGF decreases and intrinsic voltage gain increases owing to increasing the values of transconductance and drain current of the proposed device, as depicted in Fig. 2. When compared to GS-GCDG-JL s-Si device, TMGS-GCDG-JL s-Si device has better TGF and higher $g_m$ and lower $g_d$ of the TMGS-GCDG-JL s-Si device, as illustrated in Figs. 2 and 5. Thereby, the proposed device has higher analog voltage gain and superior power efficiency due to TMG structure when compared to GS-GCDG-JL s-Si device.

Figure 9 plots the effect of $t_{ox2}$ on the voltage gain and TGF of the TMGS-GCDG-JL s-Si MOSFET. The power conversion efficiency and voltage gain of proposed MOSFET decrease because of the less gate control over the strained-Si channel than drain terminal as $t_{ox2}$ increases. Moreover, gate stack with HfO$_2$ has better TGF and higher voltage gain than the gate stack with Si$_3$N$_4$ of the TMGS-GCDG-JL s-Si MOSFET due to the higher $g_m$ and lower $g_d$ of the TMGS-GCDG-JL s-Si MOSFET, as illustrated in...
Fig. 6 Variation of $t_{ox2}$ on the drain characteristics and $g_d$ of TMGS-GCDG-JL s-Si device

Fig. 7 Variation of $N_f$ with $L_d$ on output characteristics and $g_d$ of TMGS-GCDG-JL s-Si MOSFET

Fig. 8 Effect of $m$ on the intrinsic voltage gain and TGF of TMGS-GCDG-JL s-Si device

Fig. 9 Variation of $t_{ox2}$ on the intrinsic voltage gain and TGF of TMGS-GCDG-JL s-Si device
Figs. 3 and 6. Therefore, the proposed MOSFET with Si$_3$N$_4$ has higher analog intrinsic gain and low power consumption are obtained.

The effect of $N_f$ on the intrinsic voltage gain and TGF of the TMGS-GCDG-JL s-Si device is shown in Fig. 10. As positive $N_f$ increases, TGF decreases and intrinsic voltage gain increases owing to the decrease in threshold voltage of TMGS-GCDG-JL s-Si MOSFET, and vice-versa for negative fixed charge density. Hence, the TMGS-GCDG-JL s-Si MOSFET with negative fixed charge density can be operated at lower bias values, and vice-versa for positive $N_f$. Moreover, the proposed MOSFET with positive $N_f$ has higher analog intrinsic gain is attained.

Figure 11 shows the variations of $m$ and $t_{ox2}$ on the early voltage of TMGS-GCDG-JL s-Si device. The early voltage of the TMGS-GCDG-JL s-Si MOSFET increases as $m$ increases and $t_{ox2}$ decreases since the $g_d$ of the device decreases, as illustrated in Figs. 5 and 6 (low early voltage denotes the high channel length modulation effect in the MOSFET). Besides, gate stack with HfO$_2$ has greater early voltage than the gate stack with Si$_3$N$_4$ of the TMGS-GCDG-JL s-Si MOSFET since the output conductance for gate stack with HfO$_2$ is less, as depicts in Fig. 6. Moreover, the proposed TMGS-GCDG-JL s-Si MOSFET has higher early voltage than the GS-GCDG-JL s-Si MOSFET due to the less output conductance of the proposed device, as depicts in Fig. 5. As a result, the effect of channel length modulation in proposed TMGS-GCDG-JL s-Si MOSFET is less compared to the GS-GCDG-JL s-Si MOSFET.

Figure 12 demonstrates the effect of $N_f$ on early voltage of the TMGS-GCDG-JL s-Si MOSFET. The early voltage of the proposed device decreases/increases by increasing the negative/positive fixed charge density due to an increment/decrement in the output conductance with respect to negative/positive $N_f$, as demonstrated in Fig. 7. Hence, effect of channel length modulation in the device increases/reduces due to negative/positive fixed $N_f$ at s-Si/oxide interface.

Figure 13 demonstrates the effect of $m$ on $f_t$ and total gate capacitance of the TMGS-GCDG-JL s-Si MOSFET. As $m$ decreases, the $f_t$ and gate capacitance of the TMGS-GCDG-JL s-Si MOSFET decrease owing to an increment in the flat-band voltage of TMGS-GCDG-JL s-Si device and reduction of inversion carriers in strained-silicon channel. Moreover, when compared to proposed TMGS-GCDG-JL s-Si device, the gate capacitance and $f_t$ of the GS-GCDG-JL s-Si MOSFET are higher due to the higher $g_m$ of the GS-GCDG-JL s-Si device, as shown in Fig. 2.

The variation of $t_{ox2}$ on the $f_t$ and gate capacitance of the TMGS-GCDG-JL s-Si device is depicted in Fig. 14.
As $t_{ox2}$ decreases, higher $C_{gs}$ and lower $f_t$ of the TMGS-GCDG-JL s-Si MOSFET are obtained due to the increase in inversion carriers in the channel. Besides, the gate stack with HfO$_2$ has higher gate capacitance than the gate stack with Si$_3$N$_4$ of the TMGS-GCDG-JL s-Si MOSFET due to the higher permittivity of HfO$_2$. However, the gate stack with HfO$_2$ has less $f_t$ than the gate stack with Si$_3$N$_4$ of the TMGS-GCDG-JL s-Si MOSFET is noticed.

Figure 15 shows the effect of fixed charged density on the gate capacitance and $f_t$ of the TMGS-GCDG-JL s-Si device. As negative $N_f$ increases, gate capacitance of the TMGS-GCDG-JL s-Si MOSFET decreases due to mitigate of inversion charges in channel of MOSFET, and reverse trend follows for positive $N_f$. Moreover, as negative/positive $N_f$ increases, $f_t$ of the TMGS-GCDG-JL s-Si device decreases/increases because of the decrement/increment in $g_m$ of TMGS-GCDG-JL s-Si MOSFET with negative/positive $N_f$, as demonstrated in Fig. 4.

Figure 16 shows the variation of $t_{ox2}$ on the voltage gain of the TMGS-GCDG-JL s-Si MOSFET with the operating frequency. As seen in Fig. 16, as $t_{ox2}$ decreases, voltage gain of TMGS-GCDG-JL s-Si device decreases because of decrement in $g_d$ and increment in $g_m$, as shown in Figs. 2 and 3. Moreover, gate stack with HfO$_2$ has higher voltage gain than the gate stack with Si$_3$N$_4$ of the TMGS-GCDG-JL s-Si MOSFET. However, as operating frequency increases, voltage gain of proposed MOSFET decreases owing to the more parasitic capacitive effects. Also, the proposed TMGS-GCDG-JL s-Si MOSFET has greater voltage gain than GS-GCDG-JL s-Si device because of the TMG structure in the proposed device. Figure 17 depicts the effect of fixed charge density on the voltage gain of the TMGS-GCDG-JL s-Si MOSFET. As positive/negative $N_f$ increases, voltage gain of TMGS-GCDG-JL s-Si device increases/decreases owing to increment in $g_m$ and decrement in $g_d$, as shown in Figs. 4 and 7.

The variations of $m$ and $t_{ox2}$ on $f_{max}$ of the TMGS-GCDG-JL s-Si MOSFET are shown in Fig. 18. Since $m$ increases and $t_{ox2}$ decreases, $f_{max}$ of the TMGS-GCDG-JL s-Si MOSFET increases because of higher $g_m$ of proposed MOSFET, as shown in Figs. 2 and 3. Besides, higher $f_{max}$ is attained for the HfO$_2$/SiO$_2$ gate stack in comparison with the Si$_3$N$_4$/SiO$_2$ gate stack of the TMGS-GCDG-JL s-Si device since higher $g_m$ of proposed MOSFET, as shown in Fig. 4. Moreover, the TMGS-GCDG-JL s-Si MOSFET has higher $f_{max}$ in comparison with the GS-GCDG-JL s-Si device. The effect of $N_f$ on $f_{max}$ of the TMGS-GCDG-JL s-Si device is illustrated in Fig. 19. It is evident from
Fig. 14  Variation of $t_{ox2}$ on gate capacitance and $f_r$ of TMGS-GCDG-JL s-Si MOSFET

Fig. 19 that the increment/decrement in $f_{\text{max}}$ of the TMGS-GCDG-JL s-Si MOSFET is obtained as positive/negative $N_f$ increases with damaged length since higher/lower $g_m$ of proposed MOSFET with positive/negative $N_f$ at s-Si/oxide interface, as shown in Fig. 4.

The variations of $m$ and $t_{ox2}$ on TFP of s-Si TMGS-GCDG-JL s-Si device are shown in Fig. 20. As seen from Fig. 20, it is evident that the TFP of the proposed MOSFET is improved by decreasing the values of $m$ and $t_{ox2}$ in the above threshold voltage region and reverse trend follows in weak inversion region. Besides, better TFP is obtained for the HfO$_2$/SiO$_2$ gate stack in comparison with the Si$_3$N$_4$/SiO$_2$ gate stack of the TMGS-GCDG-JL s-Si MOSFET. Also, TFP of the proposed TMGS-GCDG-JL s-Si MOSFET is more than the GS-GCDG-JL s-Si MOSFET in above sub-threshold region, and reverse trend follows in weak inversion region. The effect of fixed charge density on the TFP of the TMGS-GCDG-JL s-Si MOSFET is shown in Fig. 21. TFP of the TMGS-GCDG-JL s-Si device decreases/increases as positive/negative $N_f$ increases in the strong inversion region, and reverse trend follows in weak inversion region.

Figure 22 The variations of $t_{ox2}$ and $m$ on the GFP of TMGS-GCDG-JL s-Si device are depicted in Fig. 22. GFP of the TMGS-GCDG-JL s-Si MOSFET decreases as strain and $t_{ox2}$ increase in the above threshold region, and reverse trend follows in weak inversion region. Moreover, enhanced GFP is obtained for the HfO$_2$/SiO$_2$ gate stack in comparison with the Si$_3$N$_4$/SiO$_2$ gate stack of the TMGS-GCDG-JL s-Si MOSFET. Besides, the proposed TMGS-GCDG-JL s-Si MOSFET achieves higher GFP than the GS-GCDG-JL s-Si device in the above threshold voltage region, and reverse trend follows in weak inversion region. The variation of fixed charge density on GFP of the TMGS-GCDG-JL s-Si device is depicted in Fig. 23. As negative (positive) interface charge density increases, GFP of the TMGS-GCDG-JL s-Si MOSFET decreases (increases).

The variations of $m$ and $t_{ox2}$ on GTFP of the TMGS-GCDG-JL s-Si MOSFET are depicted in Fig. 24. GTFP of the TMGS-GCDG-JL s-Si MOSFET is increased by decreasing strain and $t_{ox2}$ in above threshold region, and reverse trend follows in weak inversion region. Besides, HfO$_2$/SiO$_2$ gate-stack has greater GTFP when compared to Si$_3$N$_4$/SiO$_2$ gate stack of the TMGS-GCDG-JL s-Si MOSFET. Moreover, it is obvious from Fig. 24 that the proposed device has improved overall figure of merit compared to the the GS-GCDG-JL s-Si device in the above threshold region.

Figure 25 plots the variation of $N_f$ on GTFP of TMGS-GCDG-JL s-Si device. For a given $L_d$, when $4 \times$
Fig. 16 Variation of the $t_{ox2}$ on the voltage gain of the TMGS-GCDG-JL s-Si device along operating frequency.

Fig. 17 Variation of $N_f$ on the voltage gain of TMGS-GCDG-JL s-Si device along operating frequency.

Fig. 18 Variations of strain and $t_{ox2}$ on $f_{max}$ of the TMGS-GCDG-JL s-Si MOSFET.

Fig. 19 Variation of $N_f$ on $f_{max}$ of the TMGS-GCDG-JL s-Si MOSFET.
Fig. 20 Variations of the $m$ and $t_{ox2}$ on the TFP of TMGS-GCDG-JL s-Si device

Fig. 21 Variation of the $N_f$ on TFP of TMGS-GCDG-JL s-Si MOSFET

Fig. 22 Variations of $m$ and $t_{ox2}$ on the GFP of the TMGS-GCDG-JL s-Si MOSFET
Fig. 23  Variation of the $N_f$ the TFP of TMGS-GCDG-JL s-Si MOSFET

![Graph showing the variation of $N_f$ on the TFP of TMGS-GCDG-JL s-Si MOSFET.]

Fig. 24  Variations of $m$ and $t_{ox2}$ on the GTFP of the TMGS-GCDG-JL s-Si MOSFET

![Graph showing the variations of $m$ and $t_{ox2}$ on the GTFP of the TMGS-GCDG-JL s-Si MOSFET.]

Fig. 25  Variation of $N_f$ on the GTFP of the TMGS-GCDG-JL s-Si device

![Graph showing the variation of $N_f$ on the GTFP of the TMGS-GCDG-JL s-Si device.]

 Springer
The performance analysis of TMGS-GCDG-JL s-Si MOSFET with literature

| Device            | $g_m$, S/μm | $\left( \frac{I_d}{V_{GS}} \right)$, V | $\left( \frac{g_m}{V_{GS}} \right)$, V$^{-1}$ | $\frac{g_m}{C_{GSf}}$, fF/μm | $f_t$, GHz | GTFP, (THz/V) |
|-------------------|-------------|--------------------------------------|-------------------------------------|----------------------------|-----------|--------------|
| GS-GCDG-JL s-Si   | 3.8         | 19.35                                | 71.01                               | 27.85                      | 0.755     | 900.2        | 67.71       |
| TMGS-GCDG-JL s-Si | 3.79        | 36.17                                | 63.23                               | 63.91                      | 0.727     | 954.6        | 173.7       |
| High-k DG-JL [14] | 2.1         | 50.1                                 | 40.1                                | 60.1                       | 1.5       | 250          | –           |
| DG-JL [19]        | 0.26        | 1.28                                 | 26.7                                | 33.88                      | 0.4       | 139          | –           |
| GC DG-JL [20]     | 2.0         | 14.3                                 | 11.5                                | 43.0                       | 0.6       | 580          | –           |
| s-Si GC-DMDG [29] | 3.9         | 11.2                                 | 33.26                               | 22.59                      | 0.924     | 787          | 54.13       |

10$^{12} \leq N_f \leq -2 \times 10^{12}$, it is observed that GTFP of TMGS-GCDG-JL s-Si MOSFET increases/decreases as positive/negative interface charge density increases in the sub-threshold region and reverse trend follows in above threshold region. Besides, GTFP of the TMGS-GCDG-JL s-Si device reduces because of DIBL effect when $N_f > -2 \times 10^{12}$. Hence, the overall analog/RF performance of the proposed TMGS-GCDG-JL s-Si MOSFET varies with respect to fixed charges.

The performance analysis of proposed TMGS-GCDG-JL s-Si MOSFET is compared with existing works in the previous works, as demonstrated in Table 2. The voltage gain, $f_t$, and GTFP of proposed TMGS-GCDG-JL s-Si MOSFET (m=0.2 and $t_{ox}$=1 nm) are better than when compared to the GS-GCDG-JL s-Si MOSFET (m=0.2 and $t_{ox}$=1 nm), high-k spacer DG junctionless MOSFET [14], DG junctionless MOSFET with channel length 20 nm [19], GC DG junctionless device with channel length 30 nm [20] and strained-Si GC-DMDG MOSFET with channel length 20 nm [29]. However, the proposed TMGS-GCDG-JL s-Si MOSFET has lower early voltage than high-k spacer DG junctionless MOSFET [14]. Moreover, the proposed TMGS-GCDG-JL s-Si MOSFET has lower $g_m$ than strained-Si GC-DMDG MOSFET with channel length 20 nm [29]. Therefore, the proposed MOSFET using the TMG with GC engineering and gate stack techniques achieves improved overall analog/RF performance.

4 Conclusion

The analog/radio-frequency performance of the proposed TMGS-GCDG-JL s-Si MOSFET with fixed charge density at silicon dioxide interface has been estimated using TCAD tool. The proposed TMGS-GCDG-JL s-Si MOSFET has better overall analog/RF figure of merit compared to GS-GCDG-JL s-Si device in the above threshold region. Moreover, the analog/radio frequency figure of merits of TMGS-GCDG-JL s-Si device are improved by employing the TMG structure with the GC engineering and gate stack technique. An exhaustive analysis has been done to investigate the various analog/RF characteristics by varying MOSFET parameters of the TMGS-GCDG-JL s-Si MOSFET. Increments in TFP and GTFP of proposed TMGS-GCDG-JL s-Si MOSFET have been obtained by increasing values of strain, positive fixed charge density, and $t_{ox}$ in the weak inversion region, and vice-versa in the above threshold voltage region. Therefore, the proposed TMGS-GCDG-JL s-Si MOSFET has better analog/radio-frequency figure of merits in above the threshold voltage region.

Acknowledgements The authors gratefully acknowledge the simulation facilities provided by Analog IC lab, NIT Warangal.

Author Contributions All the authors contributed to study conception and conceptualization. Material setup and TCAD simulation are performed by Sudapalli Subba Rao. Formal analysis and investigation of the simulated results were done by Rani Deepika Balavendran Joseph. The first draft of the manuscript was written by D. Srikar and Vijaya Durga Chintala and edited by Sudapalli Subba Rao and Gopi Krishna Saramekala. Finally, the complete work was carried under the supervision of Nistala Bheema Rao.

Funding The authors declare that Sudapalli Subba Rao has received research support from National Institute of Technology Warangal. Further, authors have no other relevant funding or financial support to disclose in relevance to the work shown in this paper.

Data Availability The data that support the findings of this study are available from the corresponding author, upon reasonable request.

Declarations

Consent for Publication All the authors declare their consent to transfer the publication rights to the journal in which this manuscript is submitted.

Conflict of Interests The authors declare that there is no conflict of interests.

References

1. Thompson SE, Armstrong M, Auth C, Cea S, Chau R, Glass G, Hoffman T, Klaus J, Ma Z, McIntyre B, Murthy A, Obrodovic B, Shifren L, Sivakumar S, Tyagi S, Ghani T, Mistry K, Bohr M, El-Mansy Y (2004) A logic nanotechnology featuring strained-silicon. IEEE Electron Device Lett 25(4):191–193
2. Jurczak M, Skotnicki T, Ricci G, Campidelli Y, Hernandez C, Bensahel D (1999) Study on Enhanced performance in NMOSFETs on strained silicon. In: 29th European solid-state device research conference, vol 1, pp 304–307

3. Sanuki T, Oishi A, Morimasa Y, Aota S, Kinoshita T, Hasumi R, Takegawa Y, Isobe K, Yoshimura H, Iwai M, Sunouchi K, Noguchi T (2003) Scalability of strained silicon CMOSFET and high drive current enhancement in the 40 nm gate length technology. In: IEEE International electron devices meeting 2003, pp 3.5.1–3.5.4

4. Keith S, Bufler FM, Meinerzhagen B (1997) Full band monte-carlo device simulation of an 0.1 um N-Channel MOSFET in strained silicon material. In: 27th European solid-state device research conference, pp 200–203

5. Nguyen C, Pham A, Jungemann C, Meinerzhagen B (2005) Study of charge carrier quantization in strained Si-nMOSFETs. Mater Sci Semicond Process 8(1):363–366

6. Ko CH, Ge CH, Huang CC, Fu CY, Hsu CP, Chen CH, Chang CH, Lu JC, Yeo YC, Lee WC, Chi MH (2005) A novel process-induced strained silicon (PSS) CMOS technology for high-performance applications. In: IEEE VLSI-TSA international symposium on VLSI technology, 2005. (VLSI-TSA-Tech), pp 25–26

7. Langdo T, Currie MT, Lochtelfeld A, Hammond R, Carlin J, Erdtmann M, Braithwaite G, Yang VK, Vineis C, Badawi H, Bulsara M (2003) SiGe-free strained Si on insulator by wafer bonding and layer transfer. Appl Phys Lett 06:4256–4258

8. Suddapalli SR, Nistala BR (2020) Analytical modeling of subthreshold current and swing of strained-Si graded channel material double gate MOSFET with interface charges and analysis of circuit performance. International journal of numerical modelling: Electronic networks, devices and fields

9. Shankar R, Kaushal G, Maheshwaram S, Dasgupta S, Manhas SK (2014) A degradation model of double gate and gate-all-around MOSFETs with interface trapped charges including effects of channel mobile charge carriers. IEEE Trans Device Mater Reliab 14(2):689–697

10. Duksh YS, Singh B, Gola D, Tiwari PK, Jit S (2021) Subthreshold modeling of graded channel double gate junctionless FETs. Silicon 13:1231–1238

11. Haque MM, Kabir MH, Rahman Adnan MM (2020) Analytical modelling and verification of potential profile of DG JLFET with and without stack oxide. Int J Electron 1–22

12. Vadhya N, Girdhardas KA (2018) Surface potential modeling of graded-channel gate-stack (OCGS) high-K dielectric dual-material double-gate (DMDG) MOSFET and analog/RF performance study. Silicon 10:2865–2875

13. Dubey S, Santra A, Saramekula G, Kumar M, Tiwari PK (2013) An analytical threshold voltage model for triple-material cylindrical gate-all-around (TM-CGAA) MOSFETs. IEEE Trans Nanotechnol 12(5):766–774

14. Baruah RK, Paily RP (2014) A dual-material gate junctionless transistor with high-k spacer for enhanced analog performance. IEEE Trans Electron Devices 61(1):123–128

15. Pradhan KP, Mohapatra SK, Sahu PK, Behera DK (2014) Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET. Microelectron J 45(2):144–151

16. Baidya A, Baishya S, Lenka T (2017) Impact of thin high-k dielectrics and gate metals on RF characteristics of 3D double gate junctionless transistor. Mater Sci Semicond Process 71:413–420

17. Ferhati H, Djeffal F (2018) Graded channel doping junctionless MOSFET: a potential high performance and low power leakage device for nanoelectronic applications. J Comput Electron 17:129–137

18. Suddapalli SR, Nistala BR (2019) A center-potential-based threshold voltage model for a graded-channel dual-material double-gate strained-Si MOSFET with interface charges. J Comput Electron 18(4):1173–1181

19. Ghosh D, Parihar MS, Armstrong GA, Kranti A (2012) High-performance junctionless MOSFETs for ultralow-power analog/RF applications. IEEE Electron Device Lett 33(10):1477–1479

20. Chen Y, Mohamed M, Jo M, Ravaiolu U, Xu R (2013) Junctionless MOSFETs with laterally graded-doping channel for analog/RF applications. J Comput Electron 12(4):757–764

21. Singh SA, Tripathi Comparative S (2019) Analysis of double gate junction less and gate stacked double gate junction less MOSFETs. Semiconductors 53(13):1804–1810

22. Baral K, Singh PK, Kumar S, Singh A, Tripathy M, Chander S, Jit S (2020) 2-D analytical modeling of drain and gate-leakage currents of cylindrical gate asymmetric halo doped dual material-junctionless accumulation mode MOSFET. AEU - Int J Electron Commun 116:153071

23. Xiang Q, Goo J-S, Pan J, Yu B, Ahmed S, Zhang J, Lin M-R (2003) Strained silicon NMOS with nickel-silicide metal gate. In: 2003 Symposium on VLSI technology, digest of technical papers (IEEE Cat. No.03CH37407), pp 101–102

24. Lim J-S, Thompson SE, Fossum JG (2004) Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs. IEEE Electron Device Lett 25(11):731–733

25. Zhang W, Fossum JG (2005) On the threshold voltage of strained-Si-Si1-xGex MOSFETs. IEEE Electron Device Letters 52:263–268

26. Kumar MJ, Venkataraman V, Noual S (2006) A simple analytical threshold voltage model of nanoscale single-layer fully depleted strained-silicon-on-insulator MOSFETs. IEEE Trans Electron Devices 53(10):2500–2506

27. Sentaurus Device User Guide (2019) Synopsys, Inc., Mountain View, CA, USA

28. Omura Y, Horiguchi S, Tabe M, Kishi K (1993) Quantum-mechanical effects on the threshold voltage of ultrathin-SOI n-MOSFETs. IEEE Electron Device Lett 14(12):569–571

29. Suddapalli SR, Nistala BR (2020) The analog/RF performance of a strained-Si graded-channel dual-material double-gate MOSFET with interface charges. J Comput Electron

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.