A Ka band CMOS differential LNA with 25 dB gain using neutralized bootstrapped cascode amplifier

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Abstract: This paper presents a Ka band two-stage differential LNA in standard CMOS technology. Neutralized bootstrapped cascode amplifier (NBCA) is implemented to improve the gain and noise performance of the LNA while maintaining the stability. By using 1:3 transformer and larger common gate transistor in the output buffer, the output matching is improved. The effects of neutralization and bootstrapped capacitor on the noise figure, gain and stability are further analyzed. Measurements show that the whole circuit offers a 25 dB peak gain and 4.1 dB NF at 34.5 GHz, with better than 10 dB return losses at the frequency band of interest (33.5 GHz–36 GHz).

Keywords: LNA, bootstrapped, neutralization, transformer, CMOS

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

In the CMOS receiver, the low-noise amplifier plays an important role in determining the noise performance of the front-end, because it contributes most of the noise [1] and its gain must be large enough to minimize the noise contribution of the following stages [2]. In millimeter wave range, it is hard to obtain high gain from amplifier to guarantee the performance of LNA. As the frequency goes up to millimeter wave region, the maximum stable gain that a single transistor can provide reduces. In order to guarantee stability and provide more gains, neutralization capacitor is proposed [3, 4, 5].

To obtain enough stability and gain, cascode topology is often adopted in LNA. However, the noise from common source (CG) transistor begins to manifests at higher frequency due to the parasitic capacitor ($C_v$) at node between the two transistors, which is the major challenge for LNA design using cascode topology. In [1, 6], tuning inductor is inserted to cancel out $C_v$. However, it consumes too much area and its insertion losses will be another problem. In PA designs [3], bootstrapped cascode amplifier was proposed to enhance the delivered power, using miller effect from parasitic $C_{ds}$ to tune out the $C_v$.

Based on that topology, we make a further analysis on this topology and demonstrate the application of this NBCA topology on LNA design theoretically and practically. Simulation result shows that the NBCA improves the gain of LNA by 3 dB. Mom capacitor is implemented in parallel with the CG transistor, instead of parasitic capacitance from interconnections in [3]. By analyzing the circuit model of LNA, we observe that the bootstrapped parasitic capacitance can mitigate the noise contribution from the CG transistors. In addition, we demonstrate why neutralization capacitor is needed to maintain unconditional stable for bootstrapped
amplifier both by theory and simulation. In this way, the performance of LNA can be largely improved without using the tuning inductor that consumes much area. To further reduce the noise from substrate and guarantee stability, differential amplifiers are adopted in the proposed LNA.

The proposed two-stage differential Ka Band NBCA LNA shows 25 dB peak gain peak gain and 4.1 dB noise figure at 34.5 GHz. Two transformers are added at the input and output nodes that serves as balun to provide single-ended input and output, which shows better than 10 dB return losses over 2.5 GHz frequency range. To the best of the authors’ knowledge, it is first time that NBCA is reported to be applied in LNA design.

2 Circuits topology

The proposed two-stage Ka band LNA consists of an input transformer, a cascode amplifier with NBCA technology and an output matching buffer. The schematic of the first stage LNA is shown in Fig. 1.

2.1 Neutralization capacitor

Neutralization capacitor is widely used in millimeter-wave amplifiers to improve the stability and gain of the amplifier [3, 4, 5]. By neutralizing the $C_{gd}$ of the common source transistors (M1 and M2), it enhances the stability of the amplifier, thus the maximum stable gain (MSG) is increased.

Fig. 2 illustrates the simulated gain of the cascode amplifier with different values of neutralization capacitor. Large capacitor will further boost the gain. However, as shown in Fig. 3, the 21 fF neutralization capacitor worsens the stability factor, a value that over-compensates $C_{gd}$ and leads to instability.

Simulation results in Fig. 3 show that the 13 fF neutralization capacitor increases the stability factor by 10 times, which is even more important for bootstrapped technology. And we select 13 fF $C_{N}$ in our design that totally cancels out $C_{gd}$ and gives the highest value of stability factor $K_{f}$. $K_{f}$ is denoted by (1.1)
which should be larger than 1 to guarantee the unconditional stability of the amplifier [6].

\[
K_f = \frac{2 \text{Re}(Y_{11}) \text{Re}(Y_{22}) - \text{Re}(Y_{12}) \text{Re}(Y_{21})}{|Y_{12}Y_{21}|} > 1 \tag{1.1}
\]

In addition, even \( C_N \) is varied by 30%, the amplifier can still be unconditional stable.

Fig. 2. Simulated \( S_{21} \) of cascode amplifier with different neutralization capacitors.

Fig. 3. Simulated \( K_f \) at 35 GHz of cascode amplifier with different neutralization capacitors

As the gain of the common source transistor increases, the noise contributions from the following transistors will be reduced. Fig. 4 compares the \( NF_{\text{min}} \) versus different values of \( C_N \). Larger the neutralization capacitor, more gain the common source transistor can provide, and lower the noise figure. Compared with the amplifier without neutralization capacitor, 13 fF \( C_N \) improves \( NF_{\text{min}} \) by 0.2 dB at 35 GHz.

### 2.2 Bootstrapped technology

At the node X, there is parasitic capacitance \( C_X \) which serves as an extra shunt path to ground at high frequency, as shown in Fig. 5. That leads to reduction in the gain especially at millimeter-wave frequency. To cancel out \( C_X \), the bootstrapped capacitor \( C_m \) is inserted in parallel with the CG transistors M3 and M4, introducing
in negative capacitance due to Miller effect. Fig. 6 depicts the simulated input capacitance at node X ($C_{X,U}$) versus bootstrapped capacitance. By introducing in negative capacitance, bootstrapped capacitance reduces the input capacitance looking into M3. In this way, as shown in Fig. 7, the gain of the amplifier will be largely improved.
On the other hand, as in Fig. 5, the noise contribution from the common gate CG transistor M3 is denoted by:

$$V_{n, out} = \frac{Z_L}{g_{m2}^{-1} + Z_{X,D}}$$  \hspace{1cm} (1.2)

Assuming the output resistance of the common source (CS) transistor M1 is large enough, the impedance $Z_{X,D}$ at node X is determined by the parasitic capacitance $C_X$. Reducing $C_X$ helps to mitigate the noise contribution from M3 and M4. Traditionally, parallel or series inductor is utilized for that purpose [1, 7], which consumes much area and suffers from additional losses. Bootstrapped technology, however, implements capacitors in parallel with the M3 and M4. The negative capacitance due to miller effect is denoted by:

$$C_c = (g_{m2}R_L - 1)C_M$$  \hspace{1cm} (1.3)

The image part of $Z_{X,D}$ becomes larger when the $C_c$ partly cancels the parasitic $C_X$. As the real part of $Z_{X,D}$ is large enough, the output noise from the CG stage in (1.2) is reduced.

Fig. 8 depicts simulated $NF_{min}$ of cascode amplifier that bootstrapped capacitance reduces the noise contribution from M3, especially at higher frequencies.

In addition, at the frequency band of interest, quality factor of the mom capacitor using metal lines is much larger than transmission line or inductor (over 100). Thus compared with the traditional method using inductor, bootstrapped
capacitor introduces in fewer losses. And its size is similar to transistors, much smaller than the other passive components like inductors or transmission line.

The improved gain of the first stage LNA will also suppress the noise contributions from the following stages, which finally benefits the whole LNA performance.

However, the bootstrapped capacitor also adds an additional path, which will cause stability problems. In Fig. 5, the bootstrapped capacitor bypasses the CG transistor at higher frequency. As the value of \( C_m \) increases, the cascode amplifier behaves more like a common source amplifier. For the common source amplifier, the parasitic capacitance \( C_{GD} \) introduces in a direct path from input to output, leading to an RHP zero, which worsens the stability of the amplifier at higher frequency. And that is the reason why cascode amplifier is usually more stable than common source amplifier at millimeter wave frequency.

In order to resolve the instability due to \( C_{GD} \), neutralization capacitor \( (C_N) \) aforementioned is adopted. The reason why 13 fF \( C_N \) is selected is that it cancels out a large part of \( C_{GD} \) and gives the highest value of \( K_f \). However, the \( C_m \) still cannot be too large for which the neutralization capacitor is unable to compensate. As in Fig. 9, 37 fF and 50 fF \( C_m \) is potentially instable at higher frequencies. And 25 fF \( C_m \) with \( K_f \) over 1.5 at 40 GHz is used, which is unconditional stable at higher frequencies. Even if there might be variations of \( C_m \)'s value, the whole amplifier can still be unconditional stable.

In sum, selecting values of the two capacitors \( (C_N \) and \( C_m) \) in a CMOS differential neutralized bootstrapped cascode LNA should follow two steps. Step 1) Choose an optimum \( C_N \) according to simulation to maximize \( K_f \). Step 2) With the \( C_N \) from step 1, plot \( K_f \) versus frequency with different values of \( C_m \) to find the proper value of \( C_m \) that is both unconditional stable at the working frequency and gives highest gain.

### 2.3 Output matching transformer

A buffer is added following the LNA with NBCA technology for output matching. As shown in Fig. 10, cascode amplifier with a 1:3 output matching transformer is implemented. As the output resistance \( (R_{ds}) \) of the cascode amplifier is over 500 \( \Omega \), 10 times larger than the load resistance (50 \( \Omega \)), 1:3 transformer is adopted to
convert the differential signal to single-ended one and provide output matching. As in Fig. 10, matching transformer uses the top metal 8 with 3.25 µm thickness for better quality factor. The matching transformer is simulated in ADS momentum EM simulator that shows less than 2.1 dB insertion loss at the working frequency in Fig. 11.

Fig. 11. Insertion loss of the 1:3 matching transformer

Fig. 12. $R_{ds}$ versus frequency with different widths of the CG transistors.

The sizes of CG transistor M7 and M8 are 1.8 µm $\times$ 32, larger than those of M5 and M6. By expanding the sizes of the CG transistor, output matching is improved in two ways. As in Fig. 12, the output resistance of cascode amplifier ($R_{ds}$)
decreases with the increasing width of the CG transistor, making it easier for matching. On the other hand, by introducing in more capacitance, larger transistor reduces the quality factor of the output transformer. The EM simulation results of output resistance Real($Z_{22}$) and $S_{22}$ of the second stage buffer is shown in Fig. 13 and Fig. 14. Increasing the widths of M7 and M8 broadens the bandwidth of the output matching in Fig. 13 and Fig. 14. In addition, by reducing the output resistance of M7 and M8, the DC voltage drop on CG transistor is reduced and the $V_{ds}$ of CS transistor is increased. In this way, the linearity of the circuit is improved.

### 3 Experimental results

The proposed LNA is fabricated in 1.2 V standard 65 nm 1P8M CMOS process. The chip microphoto is shown in Fig. 15 and the chip area including all pads is about $758 \mu m \times 693 \mu m$. Two-port S parameters are measured using Agilent N5227A vector network analyzer and RF probes up to 40 GHz. Large signals gains and noise figure are also measured with signal sources and Agilent 9030A spectrum analyzer.

Fig. 16 illustrates the measured $S_{21}$ to 40 GHz. The measured $S_{21}$ shows a 25 dB peak gain at 34.4 GHz and 3 dB bandwidth over 2.5 GHz. The measured peak frequency shifts from 35.2 GHz to 34.4 GHz, about 2.3% of the centre...
frequency. We attribute this phenomenon to the EM simulation model of passive devices and transistor model are not perfectly accurate. The model does not include all the capacitance between the resonant transformer and other metals, which leads to the decrease of peak frequency.

As in Fig. 17, return losses of input and output ports (S11 and S22) are better 10 dB at the frequency band of interest (33.5 GHz–36 GHz).
LNA’s noise figure is measured by cascading the LNA with an external 25 dB gain amplifier. Then $NF_{tot}$ of the LNA and external amplifier is measured with signal source and spectrum using the direct noise measurement method [8].

$$NF_{tot} = P_{N,\text{out}} - (-174 \text{ dBm/Hz}) - G - 10 \log RBW$$  \hspace{1cm} (1.4)

In the equation, $P_{N,\text{out}}$ is the measured total output noise power. $-174 \text{ dBm/Hz}$ is the noise density of ambient noise at room temperature. $RBW$ is the resolution bandwidth of spectrum. $G$ is the gain of LNA and the external amplifier.

Finally we can calculate the LNA’s $NF$ based on the Friis’ equation [2] using $NF_{tot}$, the measured gain of LNA ($A_{LNA}$), and the noise figure of the external amplifier ($NF_{\text{amplifier}}$):

$$NF_{LNA} = NF_{tot} - \frac{NF_{\text{amplifier}}}{A_{LNA}}$$  \hspace{1cm} (1.5)

Fig. 18 depicts the measured noise figure versus the simulation results. The measured NF shows 4.1 dB NF at 34.5 GHz and less than 5 dB NF from 33.5 GHz to 36 GHz. This method needs the LNA to provide enough gain to suppress the noise contribution from following amplifier and losses in the interconnections for accuracy. When the LNA fails to provide enough gain as the frequency goes up, the measured noise figure begins to increase. However, within the 3-dB bandwidth, the measurement is close to simulation results, which is only about 1 dB higher than the simulation.

![Fig. 18. Measured and simulated noise figure NF](image)

Large signal test is performed and shows that output compression point ($P_{-1dBm}$) is 1 dBm. The whole Ka band LNA consumes 16 mA from 1.2 V power supply.

Finally, the performances of the proposed Ka band LNA are summarized in Table I and compared with those of state-of-art. FOM of LNA is defined in (1.6) [9, 10].

$$FOM = \frac{\text{Gain (dB)} \cdot \text{Bandwidth (GHz)} \cdot OP_{1dB} (\text{mW})}{\left[ NF (\text{dB}) - 1 \right] \cdot P_{dc} (\text{mW})}$$  \hspace{1cm} (1.6)
4 Conclusion

This article presents a two-stage differential LNA in standard CMOS technology for Ka band application. To improve the gain and noise performance of the LNA, bootstrapped cascode amplifier is implemented. It is analyzed both in theory and simulation that the effect of neutralization and bootstrapped capacitor on the stability, noise, and gain of the cascade amplifier. By using 1:3 transformer and larger common gate transistors in the output buffer, the output matching is further improved. Measurements show that the whole circuit offers a 25 dB peak gain and 4.1 dB NF at 34.5 GHz, with better than 10 dB return losses at the frequency band of interest (33.5 GHz–36 GHz). This letter demonstrates the practical application of NBCA technology in LNA design.

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