Are micro-architectural features able to explain faulty executions in the presence of soft errors? A preliminary study.

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Abstract—Soft errors induced by radiations are one of the most challenging issues impacting the electronic systems’ reliability. In the embedded domain, system designers often rely on Double Modular Redundancy (DMR) to reach the desired level of reliability. This solution has increasing overhead, given the complexity achieved by modern microprocessors in all domains. This paper addresses the promising field of using efficient machine-learning powered cores for the detection of soft errors. To create such cores and make them general enough to work with different software applications, microarchitectural attributes are a fascinating option as candidate fault detection features. Several processors already track these features through dedicated Performance Monitoring Units. However, there is an open question to understand to what extent they are enough to detect faulty executions. This paper moves a step forward in this direction. Exploiting the capability of gem5 to simulate real computing systems, perform fault injection experiments and profile microarchitectural attributes (i.e., gem5 Stats), this paper presents the results of a comprehensive analysis regarding the potential attributes to be used for soft error detection and associated models that can be trained with these features. Particular emphasis was devoted to understanding whether event timing could bring additional information to the detection task. This information is crucial to identify the best machine learning models to employ in this challenging task.

Index Terms—reliability, soft errors, machine learning, artificial neural networks, soft error analysis

I. INTRODUCTION

Soft errors induced by radiations, which started as a rather exotic failure mechanism causing anomalies in satellite equipment, have become one of the most challenging issues that today impact the reliability of all electronic systems, also in ground-level applications [1]. Many efforts have been spent in the last decades to measure [2], model [3], and mitigate radiation effects [4], applying numerous techniques to approach the problem at various abstraction levels following a cross-layer reliability paradigm [5].

Focusing on microprocessor-based systems, which represent the large majority of electronic systems nowadays, resilience to soft errors requires the introduction of redundancy at different levels to achieve fault detection and fault correction [6]. At the software level, data replication techniques and time redundancy may increase the resiliency to soft errors with high costs in terms of performance and memory footprint. In safety-critical embedded applications (e.g., automotive, aerospace, railways), hardware redundancy is still the preferred technique. In particular, Double Modular Redundancy (DMR) implementing lock-step execution is a popular schema to achieve fault detection, and check-pointing is the solution to enable recovery from faults [7]. However, with the increasing complexity of microprocessor cores, complete duplication is becoming unaffordable. One way to overcome this limitation is the design of custom cores with reduced complexity to monitor the microprocessor activity and detect faulty program executions [8]–[10]. Artificial intelligence is a fascinating instrument to support designers in this domain, bringing to the new concept of artificial resilience, i.e., systems that can be trained to detect and possibly recover from faults [11]. This, in turn, requires building custom cores powered by Artificial Neural Networks (ANN) to monitor specific system attributes to detect anomalous executions.

Machine learning has been employed to detect patterns and predict how a system reacts to soft errors using high-level software features [12], [13]. However, microarchitectural attributes are easier to collect and may be effective in analyzing several classes of applications. Therefore, for achieving hardware-implemented artificial resilience, the open question is: “are microarchitectural features able to explain faulty executions in the presence of soft errors?” Dutto et al. showed that the answer to this question is yes in the case of permanent faults [14]. However, permanent faults lead to fault accumulation during software execution, amplifying anomalies and making detection easier. The same paper shows that working with soft
errors is more complex and requires further investigation. \[15\] provides results toward a positive answer to this question, even if a deep analysis of several features is not reported. Recently Nosrati et al. proposed a machine learning-based checker for soft error detection in embedded processors \[16\]. While results are promising in terms of fault detection accuracy, the approach relies on monitoring internal signals of the microprocessor that would require an invasive hardware redesign.

To support research in this domain, this paper focuses on performing a preliminary study to understand to what extent microarchitectural attributes can be exploited to detect soft errors. In particular, the article focuses on typical features that can be exposed through the Performance Monitoring Unit (PMU), a logical part of modern microprocessors, in charge of tracking and measuring numerous performance-related events derived from Hardware Performance Counter (HPC) registers (e.g., executed instructions, cache misses, or incorrectly anticipated branching for an active program). A set of fault injection experiments performed using FIMSIM \[17\] a fault injector framework based on gem5 \[18\] was used to create a dataset of features over several faulty and correct executions. This dataset was analyzed to give designers insights into the best options to build their soft error detection systems. Particular emphasis was devoted to understanding whether event timing could bring additional information to the model. This information is crucial to identify the best ANN models to employ in this challenging task. While the paper’s goal is not to provide a final solution for developing an artificial resilient system, it provides a good starting point to design ANN-based soft error detection cores in future microprocessors.

The rest of this paper is organized as follows: \textbf{section II} summarizes the procedure used to collect the data at the base of the proposed analysis, while \textbf{section III} is the core of this paper proposing results obtained digging into the data. Finally, \textbf{section IV} summarizes the paper’s main contributions and suggests open challenges for future research activities.

\textbf{II. EXPERIMENTAL SET-UP}

Injecting faults directly into real hardware is complex; virtual platforms and simulators simplify the development of fault injection modules and the subsequent data collection task thanks to their design flexibility and profiling capabilities. For this reason, simulation-based fault injection was used to collect data. \textbf{Figure 1} summarizes the basic building blocks of the implemented experimental design.

Since the goal is to analyze microarchitectural level attributes, the gem5 simulator was used to emulate the hardware substrate \[18\]. gem5 is a modular simulation platform encompassing system-level architecture and processor microarchitecture. The high simulation throughput and profiling capabilities of gem5 are important for gathering significant data. Experiments were performed by simulating the full-system stack, modeling the hardware through the AtomicSimpleCPU model available in gem5 configured to emulate the x86 Instruction Set Architecture (ISA). The software stack included a Linux kernel and a target application. Three MiBench \[19\] applications were considered: \texttt{qsort}, \texttt{basicmath} and \texttt{bitcount}.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|}
\hline
\textbf{Application (mIBench)} & \textbf{FIMSIM} \\
\hline
Linux & \hline
\end{tabular}
\end{table}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig1.png}
\caption{Experimental design: (a) the full system stack is emulated resorting the gem5, (b) fault injection experiments collect microarchitectural attributes (i.e., gem5 stats) for faulty and correct executions.}
\end{figure}

gem5 alone does not allow to perform fault injection. This task was accomplished using FIMSIM, an add-on to gem5 that enables fault injections of permanent (stack-at) faults, single bit upsets (SBU), and multiple bit upsets (MBU) in different microprocessor structures (i.e., intRF, specialRF, ALU, ITB, DTB, Bypass, PC) \[17\]. This paper analyzed SBU in the integer register file (intRF). After the fast-forward cycle required to boot the operating system, faults were injected at random locations and time intervals during the execution of the application. gem5 enables monitoring of the internal state of the microprocessor in two different ways:

1) \textbf{Checkpoints:} snapshots of the hardware architecture, containing all the internal values at a certain clock tick.
2) \textbf{Stats:} performance counters that profile the number of internal events, such as cache misses, jumps, accesses to memory, and so on. They can be periodically dumped into a dedicated file.

To speed up the experiments, every fault injection run started from a checkpoint collected at the end of the fast-forward cycle corresponding to the end of the Linux boot process (CPs). Several Stats (S1, S2, ..., Sn) were collected during the simulation to consider the time dimension when building the final dataset. Finally, the effect of the faults was classified by comparing the last checkpoint of the fault injection run (CPn) with the one of a golden execution (CPe). Injection experiments were labeled based on three categories:

1) \textbf{Crash:} the program completely stops working and exits. This is the most straightforward case to detect; there is no need for a dedicated system to recognize it. Therefore it is discarded for the analysis.
2) \textbf{Faulty execution:} the program terminates, but its outcome is wrong.
3) \textbf{Benign execution:} even if there was a fault, the program’s outcome is correct.

The performance counters in the gem5 Stats collected during fault injection experiments were used to create the dataset analyzed in the next section. For every benchmark, 25,000 injection experiments were performed. About 0.5% of the simulations generated a crash and were discarded. The remaining data were distributed with about 75% of non-faulty and 25% of faulty simulations. A total amount of about 600 features was monitored during every fault injection run. Data were
preprocessed and normalized before carrying out the analysis. First, some values in the collected dataset were non-numerical (NaN). Features with more than 5% NaN values and attributes with zero variance across experiments were removed. At this point, simulations containing even a single NaN value were removed from the dataset. Finally, missing values were set to zero, and the dataset was normalized. Table I summarizes the characteristics of the final dataset after preprocessing.

TABLE I: Summary of the dataset structure.

| Benchmark | Simulation count | Feature count |
|-----------|-----------------|---------------|
| qsort     | 24,436          | 366           |
| basicmath | 24,754          | 358           |
| bitcount  | 24,261          | 360           |

Since part of the exploration aims to understand if the temporal dimension adds any information to the collected data, increasing fault detection accuracy, the execution of the different benchmarks was profiled over time by collecting gem5 Stats with different granularities, i.e., every 10, 20, 50, and 100 simulation ticks.

III. RESULTS

This section reports a comprehensive analysis of the collected dataset to try to answer the question proposed at the beginning of this paper, i.e., if microarchitectural features are sufficient to build machine learning models able to detect soft errors in microprocessor-based systems.

A. Data analysis

As a first step, data were analyzed in their cumulative form, i.e., the cumulative value of each attribute at the end of the program execution. The first goal of the analysis is a preliminary inspection of the quality of the selected features. For this purpose, we used Principal Component Analysis (PCA). Figure 2 provides a visual representation of the datasets for the three benchmarks plotting the first two principal components.

Interestingly, looking at the full datasets (Figures 2(a), 2(b), and 2(c)), benign executions (blue dots) are all concentrated in a small portion of the plot. This suggests that, in general, microarchitectural attributes remain stable whenever faults do not impact the program’s outcome. Many faulty executions (red dots) are instead scattered over the plot. This is an interesting and promising result. From the system’s perspective, this suggests that the corruption of a single bit generates a significant modification in the microarchitecture’s internal attributes. This result means that these cases are easily separable and detectable from a reliability standpoint. However, by analyzing the dataset more in detail, it comes to the attention that there is a partial overlap between benign and faulty executions for a subset of the experiments. This can be appreciated by looking at Figures 2(d), 2(e), and 2(f) that report a highlight of this portion of the dataset referred to as hard-to-detect region. This detailed analysis highlights a critical aspect that must be better investigated. Machine learning models will struggle in this dataset region and must be carefully tuned to avoid loss in accuracy.

Up to now, all the features in the dataset have been considered. However, their number is relatively high, even after the data cleaning. Therefore, it can be interesting to analyze the correlation of each attribute with final fault classification. An insight into the significance of each feature can be important to guide through a feature selection phase. Pearson’s correlation coefficient was used to perform this analysis due to its smaller sensitivity to false positives. Figure 3 shows the distribution of the correlation values for the three benchmarks. Interestingly, this analysis highlights different results depending on the benchmark. In the case of qsort, most features correlate more than 0.5 with faulty executions. This confirms what was seen in Figure 2, i.e., a single transient bit-flip in the integer register file can significantly perturb the internal microprocessor activity. This is a good result, meaning many features can be used to detect a faulty run. Results for basicmath are weaker but still acceptable, while bitcount reports a low correlation. This aspect will be better investigated in the next section.

Let’s now analyze what happens at the microarchitectural level in the presence of a fault and which features are mostly correlated with faulty executions. Figure 4. Following the gem5 hierarchical organization, attributes can be grouped into six main sub-classes, shown in Figure 4(a). Results in this figure still show differences depending on the benchmarks. However, for benchmarks with higher correlation, the features that are more correlated with a faulty execution are the ones related to memory accesses (in particular mem_ctrls and membus), to the input/output bus, and the CPU. This last class includes many internal features, so it is worth analyzing them in more detail. Figure 4(b) highlights the CPU class split into its main subclasses. Looking more in detail, we can see a higher variability in attribute correlation between the different benchmarks. Looking at qsort, the benchmark with higher correlation, within the various sub-classes, the most affected are accessed to both data and instruction caches, meaning that faults change the instruction fetch order and the access to operands; the number of branches, an indication that the execution flow has been modified; committed instructions and operations, evidence of what is seen with the cache accesses; the number of function calls; internal registers reads and writes; and main memory accesses, both for load and store. This analysis suggests that single bit-flips significantly impact the program execution flow in several cases. This important characteristic will be further discussed when considering using these datasets with dedicated machine-learning models. It is worth reporting that the cache sub-classes within the CPU class comprise many lower-level features. The detailed features are not shown on a separate plot, simplifying the visualization. However, in this case, the most significant features are related to the cache’s read/write access.

Finally, the dataset was analyzed also considering the temporal dimension. In this case, attributes sampled at different simulation times were considered separately. The observed behavior is consistent with the one observed in the cumulative case, with a portion of the faulty executions easily distinguishable from the non-faulty ones and a hard-to-detect region. Figure
Fig. 2: Visual representation of the dataset for the three benchmarks using PCA. It shows faulty runs (red) and benign runs (blue). Subfigures (a), (b), and (c) show the full dataset; subfigures (d), (e), and (f) the hard to detect area.

Fig. 3: Statistical distribution of the correlation values of the features with the fault classification for the three benchmarks. Shows the detail of the hard-to-detect area, plotted using a two-components PCA for the qsort benchmark. Ten checkpoints are displayed. Interestingly, results obtained from this analysis seem to suggest that the temporal dimension does not carry significant information content. In particular, it is insufficient to improve separation in the hard-to-detect region of the dataset. A higher number of temporal steps led to similar results.

To summarize, this preliminary analysis allowed us to develop some initial insights. For the portion of the data that can be separated, a reasonably simple model is expected to provide good fault detection capabilities. The presence of the hard-to-detect zones suggests that pure microarchitectural attributes seem insufficient to reach the fault detection accuracy required in safety-critical applications. Probably different features should be considered. Adding a temporal dimension to the data seems ineffective in improving fault detection in the hard-to-detect area regardless of the number of temporal points. In this case, one option to explore would be to work directly with time series of single events (e.g., cache misses, branches, etc.). However, this can be computationally demanding due to the large number of different events observed during the execution of the various benchmarks.

Fig. 4: Statistical distribution of the correlation values over the different gem5 classes for the three benchmarks (qsort in red, basicmath in green, butcount in blue).
B. Machine learning models

Starting from the preliminary analysis proposed in subsection III-B, this section studies how different machine learning models can be trained to detect soft errors based on the considered attributes, highlighting strengths and weaknesses. For this analysis, the datasets were split as follows: 60% for the training set, 15% for the validation set, and 25% for the test set. As already reported, it is important to remember that the two classes are unbalanced, with around 75% of the examples belonging to the non-faulty class.

The cumulative dataset (i.e., without timing information), including all features, was first considered. A Fully Connected Feed Forward Neural Network (FC-FFNN) was trained. Table II reports relevant metrics (i.e., accuracy, precision, recall, and F1 score) to analyze the model’s performance on the three different benchmarks. The architecture column refers to the neural network. It reports the number of neurons per layer (e.g., 366-32-2 means a network composed of three layers including 366, 32, and 2 neurons, respectively).

Overall, as expected from our preliminary data analysis, the model’s accuracy is high. This pushes toward developing solutions for soft error detection based on the collected features. Nevertheless, the accuracy alone may be misleading. Looking more in detail, recall is, in general, not high. Feature selection was performed on the data to understand the contribution of each attribute better. Figure 6 shows the performance of different models trained using an increasing number of features starting from the top correlated ones. The results are interesting. In terms of accuracy, very few features already enable the detection of 80% of the faults. Nevertheless, these results clearly show problems with the recall of the model and highlight that additional investigations in this sense are required. By performing a more detailed analysis, we could directly relate this low performance in terms of recall with the presence of the hard-to-detect region in the different datasets. As a further confirmation, an attempt to train a model on a reduced dataset focused on the hard-to-detect zone reported deficient performance. This analysis suggests that microarchitecture level attributes can only partially detect soft errors, contradicting previous works such as da Rosa et al. [15]. This problem seems less severe in control-flow intensive benchmarks such as qsort while explodes in the case of simple linear algorithms like bitcount. This suggests that data-related features are probably required in addition to the microarchitecture attribute to cover the gap.

| Benchmark | Architecture | Accuracy | Precision | Recall | F1 score |
|-----------|--------------|----------|-----------|--------|----------|
| QSORT     | 366-32-2     | 92%      | 100%      | 67%    | 81%      |
| MATH      | 358-32-2     | 97%      | 100%      | 50%    | 63%      |
| BITCOUNT  | 360-32-2     | 91%      | 100%      | 46%    | 63%      |

After analyzing the cumulative dataset, a similar analysis was performed, introducing the time dimension considering data collected at different checkpoints.

The first approach was to build a flat dataset composed of $N_{features} \times N_{checkpoints}$ features and to train the same FC-FFNN model used before. Table III reports no significant gain in performance metrics, thus confirming what was observed in subsection III-A, i.e., the temporal dimension is not carrying informative content.

| Benchmark | Architecture | Accuracy | Precision | Recall | F1 score |
|-----------|--------------|----------|-----------|--------|----------|
| QSORT     | 3660-32-2    | 92%      | 100%      | 70%    | 82%      |
| MATH      | 3580-32-2    | 96%      | 100%      | 44%    | 61%      |
| BITCOUNT  | 3600-32-2    | 91%      | 100%      | 43%    | 61%      |

A Long-Short Term Memory (LSTM) model, including temporal information by design, was trained on the time-expanded dataset to verify this in more detail. Table IV reports the performance of the LSTM model, confirming no gain on the different metrics.

Fault detection latency is also an important parameter to take into account. To understand if early detection of faults
is possible, an FC-FFNN model was trained on the cumulative dataset and then tested at different checkpoints. Table VI shows the results obtained with ten checkpoints on the qsort benchmark. To analyze these results, one has to remember that faults are injected at uniformly distributed points in time during the program execution. Results suggest that error detection could be achieved without waiting for the end of the program execution. This is important to minimize the error detection latency.

Finally, the infrastructure to collect microarchitectural attributes through PMCs has a cost that can be reduced using event-based models such as Spiking Neural Network (SNN). This option was explored by training an SNN using a simple LIF model inside the neurons. The cumulative dataset was considered, and basic rate coding was used to translate data into trains of spikes. In other words, the input attributes were translated into the average frequency of the incoming spikes. Table VII shows the results obtained simulating the network using the snnTorch framework. It can be seen that the performance is almost the same brought with the FC-FFNN.

TABLE VI: SNN with rate-coding performance metrics, 19 top features, cumulative dataset

| Benchmark | Architecture | Accuracy | Precision | Recall | F1 score |
|-----------|--------------|----------|-----------|--------|----------|
| QSORT     | 366-32-2     | 87%      | 100%      | 51%    | 68%      |
| MATH      | 358-32-2     | 96%      | 99%       | 40%    | 56%      |
| BITCOUNT  | 360-32-2     | 90%      | 100%      | 35%    | 52%      |

IV. CONCLUSIONS

This paper performed a data-driven investigation to answer the fundamental question at the base of the use of AI-powered soft error detection cores: are microarchitectural features able to explain faulty executions in the presence of transient fault? The results of the analysis were controversial. While in terms of accuracy, results suggest a positive answer, the presence of a hard-to-detect region in the analyzed data suggests that pure microarchitectural attributes are insufficient. In particular, microarchitectural attributes seem effective when faults corrupt the application’s control flow. At the same time, additional features are probably required if the corruption is limited to the data domain. Interesting are the results obtained using SNN models. Although the analysis highlights that the temporal information does not carry significant informative content, SNN can be implemented in hardware without the need to save cumulative input data into registers, thus reducing the complexity of the monitoring unit.

In conclusion, it is worth remarking that the results in this paper are preliminary. It is clear that further investigation is required, both considering additional benchmarks and investigating a new set of features.

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