Abstract: An active clamp, three-phase, six-switch power factor correction rectifier with a one-cycle controller is proposed, which can effectively suppress the reverse recovery of the reverse parallel diode of the bridge arm switch and reduce the reverse recovery loss. The main switches and auxiliary switch are both zero-voltage switches. It works in a fixed switching frequency and low power stress during the switching period. The specific working process and control circuit are analyzed in detail, and the model simulation is carried out. The experimental platform of a 2.5 KW prototype, with a complete test and verification of the soft switch technology proposed in this paper, was set up in the laboratory.

Keywords: soft switching; PFC; rectifier; compound active clamp

1. Introduction

The early three-phase power factor correction (PFC) (PFC) rectifier is derived from the single-phase PFC rectifier system and/or passive three-phase diode rectifier [1,2]. Since then, the research on a three-phase power correction circuit and its control have rapidly developed [3].

Three-phase current senseless control for a PFC bridge converter is proposed and implemented on the Digital Signal Processor (DSP) based platform in reference [4]. A bridgeless, four-switch, three-phase rectifier is proposed in reference [5], and it can operate with any pulse width modulation (PWM) method used in a standard three-phase, six-switch voltage source rectifier. Fewer semiconductors than any other topology of its kind have been used in the proposed converter. Azazi, H.Z presents a single-stage, three-phase power factor correction (PFC) rectifier using a single-switch boost regulator with less than 5% total harmonic distortion (THD) in the supply current [6]. A three-phase, single-stage AC-DC converter with topology utilizing SiC MOSFETs is proposed and analyzed by Zhang, Z [7]. Compared with DCM mode operating in other single-stage converters, continuous current mode (CCM) mode is working in the proposed converter, which reduces the current stress running through the semiconductor devices. However, its efficiency decreases rapidly with a further increase of power. Therefore, the proposed circuit is mostly suitable for low power applications. Wu, H investigated the topologies, operation principles, and modulation strategies of a three-port three-phase rectifier (TPTPR). The study improves the overall efficiency of the TPTPR-based AC-DC power conversion system [8]. Mallik, A proposed a three-phase boost power factor correction (PFC) using a single DC output voltage sensor is controlled by another methodology [9]. The current state of input voltage and input current is estimated by measuring the ripple information on the DC link voltage, and the
controller is constructed under the condition that the three-phase input voltage has strict symmetry. Huber, L show a three-phase, six-switch boost PFC rectifier with average-current control [10]. It is examined whether the output-voltage transient response with respect to input-voltage changes can be improved by the proportional compensation with input-voltage feedforward only if duty-cycle feedforward is also implemented.

Three-phase power factor correction AC-DC conversion, which has high conversion efficiency and fewer semiconductor devices, is a common application for middle or large power three-phase rectifiers. Switching loss based on hard switching is a significant portion of the total loss of the converter. Moreover, electromagnetic interference (EMI) noise and conversion efficiency conducted by the high di/dt, which comes from the reverse recovery problem of the six switches anti-parallel diodes, requires attention [4–10]. The aforementioned problems with hard switched power factor correction (PFC) can be solved by soft switching technology achieved by modifying control and adding auxiliary circuits.

Lin C.W proposed a soft-switching assist circuit for a three-phase six-switch rectifier was used to achieve zero voltage switching (ZVS) in the main switches and zero current switching (ZCS) in the auxiliary switch, and consists of an auxiliary switch, a resonant inductor, a transformer, three barrier diodes, and a clamp RDC circuit [11]. Another soft switching circuit is proposed by Nagai, S that has only two active power semiconductor devices, which consists of one ARCPL (auxiliary resonant commutated pole link) circuit and one ARDCL (auxiliary resonant DC link) circuit. Compared with the hard switching circuit, the conversion efficiency of the proposed circuit could improve from 88.5% to 90.5%, which is confirmed on the 50 kVA system experiment [12]. Divan, D.M developed a zero-switching-loss inverters features voltage stresses which are about 1.3 times than DC-LINK volte [13]. Furthermore, the resonant dc link converter has been used for a high-frequency inverter system, which is presented by Venkataramanan, G [14]. This system uses a discrete pulse modulation strategy based on the cost function regulator, and the transient performance is improved by the additional switching arms. Qu, K.Q proposed an auxiliary resonant commutated pole link (ARCPL) for three-phase PWM rectifiers which consists of two auxiliary switches, one resonant inductor, and six diodes. The six main switches act under the ZVS state, while the two auxiliary switches work under the ZCS state. From the trend of the efficiency curve in the reference, when the output power exceeds 1.1 kW, the efficiency starts to decline gradually [15]. In another study, McMurray, W introduced resonant snubbers with auxiliary switches [16]. However, resonant snubbers including auxiliary active devices and their control introduce considerable complexity. Also, zero current transition (ZCT) topology was proposed by Mao, H [17] for high-power applications. A three-phase PWM rectifier proposed in the reference consists of three resonant capacities, three resonant inductors and three auxiliary switches. The turn off losses have been practically eliminated with the main switches turned off under the zero current condition and a low-power auxiliary ZCT circuit.

The resonant DC link converter with high voltage rating, high auxiliary switching frequency, unfixed switching frequency and high noise requires a discrete PWM strategy [12–15], which can potentially lead to sub-harmonic oscillations. Therefore, the auxiliary resonant circuit on the AC side with fixed switching frequency is placed in the resonant pole converter which adopts SVM control methods. However, the cost of the auxiliary circuit with six additional switches and their gate drivers is difficult to control [16, 17].

The auxiliary circuit including the apartments with one resonant inductor and three additional bidirectional switches, which using ZVS strategy is proposed by Mallik, A [18]. Two equal capacitors across the DC link are put in a series combination to access the midpoint of the output implemented, which avoid an additional resonant capacitor. However, mismatch in equal voltage sharing across two series capacitors would be caused by a potential issue, and also, the cost should increase by the three additional bidirectional switches. A compact auxiliary circuit, which consists of one LC branch and one auxiliary switch, is used in the three-phase six-switch PFC, which is another effective soft-switching strategy [19–21]. The converter costs become very low due to the use of fewer components and the main six switches and one auxiliary switch can work in ZVS state, which thus reduces the extra losses
from the add-on system significantly. However, the controller must be implemented by intelligent chips such as DSP. Also, the ZVSSVM control algorithm is proposed in current references which is complex and difficult to popularize.

A one-cycle control (OOC) soft-switching technology is proposed in this paper to alleviate the aforementioned issues of existing methods. The OOC controller is composed of a reset integrator, flip-flop, and other simple circuits, which simplifies the controller design, reduces the control cost, and makes it easy to maintain [22–28]. This paper proposes the control strategy, which needs a certain time interval ahead of the main six switches driving signal produced by the common one-cycle controller to drive the auxiliary switch in the circuit. The control strategy divides the phase voltage into six regions in a cycle, which is different from the ZVSSVM with 12 regions proposed in existing references. In addition, the controller proposed in this paper only needs ordinary circuit chips instead of intelligent ones. In this paper, the feasibility of the algorithm is verified by model simulation, and the accuracy of the system is verified by the actual 2.5-KW rectifier.

This paper is devoted to rectifiers with soft-switching technology for active clamp, three-phase, six-switch PFC rectifiers. The circuit of the proposed soft-switching PFC rectifier is reviewed in Section 2 and the proposed soft-switching PFC controller is described in detail in Section 3. Experimental verification is given for the rectifier in Section 4. Section 5 discusses the system in detail. Finally, a conclusion is provided in Section 6.

2. Circuit of the Proposed Soft-Switching PFC Rectifier

The compound active-clamping ZVS three-phase PFC rectifier is shown in Figure 1. Within the dotted wire frame is the auxiliary circuit of the main and auxiliary switches to realize soft switching.

![Figure 1. Compound active clamp ZVS three-phase VSR circuit.](image)

The rectifier is a standard six-switch, three-phase boost PFC with an added auxiliary circuit, which includes an auxiliary switch $S_r$, a clamp capacitor $C_r$, and a resonant inductor $L_r$. The working frequency of the auxiliary switch is the same as that of the main switches. The switching frequency of the converter is fixed. With a one-cycle control strategy, all the main and auxiliary switches can be zero-voltage switched, and the switches have low voltage stress. The reverse recovery current of the switch reverse parallel diode is also suppressed.

The three-phase, six-switch rectifier controlled by conventional SPWM or SVM requires six current commutations in one operating cycle. If the bridge arm switch with the largest phase current is not operated, the four current commutations will occur in one switching cycle, two of which are the reverse parallel diode commutating to the opposite switch, and the other two are the switches commutating to the opposite reverse parallel diode. The former two are natural soft switches, while the latter two are hard switches, and the reverse recovery of the diode exists.

In a compound active clamp converter, the auxiliary switch operates only once during a period of the main switch’s operation, resonates the DC bus to zero, and creates the condition of a zero voltage switch for the main switches. The switching of two main switches with reverse recovery must be
completed in this zero voltage time. This paper presents an improved one-cycle control method which can realize this process.

3. One Cycle Controller

In this part, the traditional one-cycle control [21] is briefly introduced, and the process of the main bridge arm switch is analyzed. On this basis, an improved one-cycle control method is proposed, and the detailed process of realizing the soft-switching action of the active clamp ZVS three-phase rectifier circuit in Figure 1 is analyzed.

3.1. One Cycle Controller for Three-Phase PFC Rectifier

The three-phase voltage is divided into six regions in a cycle, each of which is 60° as shown in Figure 2. The polarity of the phase with the largest voltage is always opposite to that of the other two phases. Therefore, only two phase currents with the same polarity need to be controlled in each region. Due to the fact that sum of three phase currents without the middle line equals zero, the third phase will be controlled after controlling two phases.

\[
\begin{align*}
\theta &= 0°, 60°, 120°, 180°, 240°, 300° \\
V_a &> V_b > V_c
\end{align*}
\]

**Figure 2.** Voltage partitioning principle in three-phase balance power system.

In the first region \([0°, 60°]\), the three-phase control can be realized by controlling the switches \(S_{an}\) and \(S_{cn}\) in Figure 1. The equivalent duty cycles are given by

\[
\begin{align*}
\text{d}_{ap} &= 1 - \text{d}_{an} \\
\text{d}_{bp} &= 0 \\
\text{d}_{cp} &= 1 - \text{d}_{cn}
\end{align*}
\]

(1)

where \(\text{d}_{xx}\) denotes the duty cycle of \(S_{xx}\).

According to reference [21], the parameter \(V_m\) is defined as

\[
V_m = \frac{V_{dc} \cdot R_s}{R_e}
\]

(2)

where \(R_s\) is the equivalent resistance of current detection and \(R_e\) is the equivalent input resistance of rectifier.

So the one-cycle control equation can be obtained as follows

\[
V_m \begin{bmatrix} 1 - \text{d}_{an} \\ 1 - \text{d}_{bn} \end{bmatrix} = R_s \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix}
\]

(3)

According to Formula (3), the core control circuit of the one-cycle controller can be obtained as shown in Figure 3.
For different control regions, $i_p$ and $i_n$ are different, which can be any two of the currents $i_a, i_b$ and $i_c$. Similarly, the switches corresponding to $S_p$ and $S_n$ have different choices in different control regions.

According to Figure 2, the partition circuit is as shown in Figure 4 below.

The purpose of a one-cycle control can be achieved by selecting the input and output signals of the control circuit in Figure 3 from the output region signals of the partition circuit in Figure 4. The input selection circuit and output driving signal of the controller is shown in Figure 5.
Combining Figure 3, Figure 4, and Figure 5, a three-phase six-switch PFC rectifier one-cycle controller is formed. In each control cycle, only two of the six switches have switching operations while the other four switches are in no-operation and are acted by a reverse parallel diode. The two switches that participate in the action of the switch are always turned on at the same time at first. After a period of time, the two switches are closed successively, as shown in Figure 6.

![Driving waveforms of two switches in one-cycle control.](image)

The sequence of closing two action switches is determined by the working region, and the two switches involved in operation are either both upper arm or lower arm at the same time, so there will not be a case where one is in upper arm and the other is in lower arm. In each working region, the operation mode of the switches participating in the switching action is the same. In a switch cycle, each bridge arm has one current commutation. When the switch is turned off, it is a soft switch, and when the switch is reset and turned on, it is a hard switch. For soft switching when the switch is reset and turned on, it is necessary to make amends to the one-cycle control, as illustrated above.

### 3.2. The Proposed One Cycle Controller

The one-cycle controlled ZVS three-phase compound active clamp rectifier requires the main switches and the auxiliary switch to work at the same frequency. The auxiliary switch is always turned off before the main switches turn on in all situations. At this time, the auxiliary resonant inductance current discharges the parallel capacitors of the main switches to make the arm’s volt resonate to zero and then turn on the main switches. The purpose of this is to realize zero-voltage turn-on. In addition, due to the existence of auxiliary resonant inductance, the reverse recovery characteristics of the switch diode in parallel are suppressed. The driving waveform of the auxiliary switch \( S_r \) is characterized by turning off before the two control switches \( S_n \) and \( S_p \) turn on, and turning on before the two control switches \( S_n \) and \( S_p \) turn off. The improved one-cycle control does not need to change the original control circuit, but only needs to process the clock reset signal of the one-cycle control to obtain the driving signal of the auxiliary switch, as shown in Figure 7.

The method of processing is to get two delays \( t_{dh} \) for clock signal, and obtain the signals clk1 and clk2 respectively. Then, the two signals of clk1 and clk2 are processed to obtain the driving signal of the auxiliary switch \( S_r \). Finally, the driving signal of \( S_r \) is anti-compressed to obtain the clk_set signal, which is used as the reset clock signal of the one-cycle core control circuit. The selection choice for the clock circuit is flexible, and can include circuits such as the crystal oscillator circuit or a clock pulse generator composed of 555 timers. For the delay circuit, the simplest method is to use an RC charging and discharging circuit and shape the waveform through a logic gate circuit. For the compression process of fetching \( S_r \), the driving signal, a simple delay circuit adds an AND gate can be used. The process described above can also be implemented by programmable logic devices.
The specific working waveform of the three-phase active clamp PFC rectifier soft switch is shown in Figure 8.

The saw-tooth wave is the current waveform $i_{Lr}$ of the resonant inductance. The three dotted lines are voltages of the two main switches $V_{cp}$, $V_{cp}$ and one auxiliary switch $V_{cr}$. From the waveform, it can be inferred that the three switches are all turned on when the voltage is zero, thus achieving the goal of zero voltage conduction. Because each switch has a parallel capacitor, the zero voltage turning off of the switch is guaranteed. Therefore, all switches are zero voltage action, and the whole circuit achieves soft switching.
3.3. Operating Modes over a Switching Cycle

In any working region, the corresponding equivalent rectifier circuit is shown in Figure 9.

![Figure 9. Equivalent rectifier circuit.](image)

In the second half of the first region \([30^\circ, 60^\circ]\), the currents of phases a and c are positive and the current of phase b is negative. At this region, it is then known that Figure 9 corresponds to Figure 1. \(V_p = V_{ab}, V_n = V_{cb}, L_p = L_n = L, D_1 \) is \(S_m \)'s parallel diode, \(S_n \) and \(C_n \) are \(S_{cn} \) with its parallel capacitor, \(D_0 \) and \(C_5 \) equivalent to \(S_{mp} \)'s parallel diode and capacitor, and \(S_p \) and \(C_p \) are \(S_{an} \) with its parallel capacitor, \(D_p \) and \(C_1 \) equivalent to \(S_{ap} \) parallel diode and capacitor.

From Figure 8, it can be seen that there are eight operating modes in the circuit of Figure 9 in one switching cycle. Taking the first working region as an example, eight working modes are analyzed one by one.

3.3.1. Mode 1: (\(t_0- t_1\))

All the main switches are turned off and the auxiliary switches \(S_r \) is turned on. In the first region, the currents of phases A and C are positive, and the phase B current is negative, so the reverse parallel diodes \(D_p, D_n \), and \(D_t \) are turned on. In the resonant groove circuit consisting of auxiliary resonant inductor \(L_r \), clamping capacitor \(C_r \) and auxiliary switch \(S_r \), the voltage of auxiliary resonant inductor \(L_r \) is the clamping capacitor voltage \(V_{C_r} \), and the current of resonant inductor increases linearly with the current change rate

\[
\frac{di_{L_r}}{dt} = \frac{V_{C_r}}{L_r}
\]  

At \(t = t_1\), the auxiliary switch \(S_r \) turns off, and this mode ends.

3.3.2. Mode 2: (\(t_1- t_2\))

At \(t = t_1\), the auxiliary switch is turned off and the auxiliary inductance current begins to decrease. The auxiliary inductance \(L_r \) resonates with capacitors \(C_r, C_3, C_n \), and \(C_p \). \(L_r \) causes \(C_3, C_n \), and \(C_p \) to discharge and charges \(C_r \). Because of the existence of \(C_r \), the auxiliary switch \(S_r \) reaches zero voltage and turns off. At \(t = t_2\), the voltage of the three main switches \(S_n, S_p \), and \(S_{bp} \) and the parallel capacitors \(C_n, C_p \), and \(C_3 \) drops to zero and the resonance stops, and this mode ends.

3.3.3. Mode 3: (\(t_2- t_3\))

At \(t = t_2\), \(S_n \) and \(S_p \) parallel diodes start to turn on. After that, \(D_n \) and \(D_p \) diodes begin to enter the reverse recovery stage. The auxiliary inductance current continues to decrease with the relation depicted below:

\[
\frac{di_{L_r}}{dt} = -\frac{V_o}{L_r}
\]
The duration of this mode is very short, which is the reverse recovery time of $D_n$ and $D_p$ diodes on the bridge arm.

3.3.4. Mode 4: ($t_3$–$t_4$)

At $t = t_3$, when the $D_n$ and $D_p$ diodes are completely turned off, the auxiliary resonant inductance current is zero. Thereafter, the auxiliary resonant inductor $L_r$ and capacitors $C_1$, $C_3$, $C_5$, and $C_r$ begin to resonate again. The voltages of $C_1$, $C_3$, and $C_5$ begin to rise and the voltages of $C_r$ start to decrease. At $t = t_4$, the voltage of $C_1$, $C_3$, and $C_5$ rises to $V_o + V_{Cc}$ and auxiliary switch $S_r$ has a voltage of zero. $S_r$ is parallel to the diode clamp, causing resonance stop.

3.3.5. Mode 5: ($t_4$–$t_5$)

At $t = t_4$, the current of the auxiliary inductor reaches the maximum negative polarity and begins increasing in polarity. The current of the auxiliary inductor rises linearly with the rate of change given by

$$\frac{di_{Lr}}{dt} = \frac{V_{Cc}}{L_r}$$

(6)

3.3.6. Mode 6: ($t_5$–$t_6$)

At $t = t_5$, the main switch $S_p$ is turned off, the input boost inductor charges $C_p$ and discharges $C_1$. Because of the existence of capacitor $C_p$, $S_p$ achieves zero-voltage turn-off.

3.3.7. Mode 7: ($t_6$–$t_7$)

At $t = t_6$, when $D_p$ is turned on, the auxiliary resonant inductor $L_r$ voltage is clamped on capacitor voltage $V_{Cc}$, and the auxiliary inductor current rate of change is as follows

$$\frac{di_{Lr}}{dt} = \frac{V_{Cc}}{L_r}$$

(7)

3.3.8. Mode 8: ($t_7$–$t_8$)

At $t = t_7$, the main switch $S_n$ is turned off, the input boost inductor charges $C_n$ and discharges $C_5$. Because of the existence of the capacitor $C_n$, $S_n$ achieves zero-voltage turn-off. At $t = t_8$, $D_n$ is turned on and then the entire process repeats from Mode 1.

4. Experimental Verifications

In order to verify the validity of the above analysis of the soft switch working process, computer simulation and actual circuit platform experiments are conducted.

4.1. Computer Simulation Verification

Based on the design described, a simulation model was built. The phase voltage in the three-phase input was 110 V, the switching frequency was 10, kHz and the output load was 12.25 kW with an output of 350 V and a load of 10 $\Omega$. Auxiliary circuit parameters include: resonant inductance $L_r = 50$ $\mu$H, switch parallel capacitor $C = 10$ nF, and clamp capacitor $C_c = 480$ uF. The simulation waveforms of ZVS on the main and auxiliary switches are shown in Figure 10.
As shown above in Figure 10, Sr is the auxiliary switch driving signal, Sn and Sp are the two main control switches on the bridge arm, $V_{dc}$ link is the voltage on the bridge arm and $V_{sr}$ is the voltage on the auxiliary switch. It can be seen from the figure that when the auxiliary switch is turned off, the voltage on the bridge arm drops rapidly to zero. Then, due to the reverse recovery of the diode, the voltage on the bridge arm remains zero. During the period, the main switches achieve zero-voltage turn-on. At the end of the diode reverse recovery commutation, the voltage on the bridge arm begins to rise and the voltage on the auxiliary switch begins to drop to zero. At this time, the auxiliary achieves zero-voltage turn-on. Finally, the zero-voltage turn-on of all switches is realized. Because the capacitors are connected in parallel with the switch, the purpose of zero-voltage turn-off of all switches is ensured, and finally all switches are in soft switch operation.

The operation of the auxiliary circuit is shown in Figure 11.

Figure 10. ZVS on main and auxiliary switches.

Figure 11 shows that $V_{cc}$ is the clamping capacitor voltage and $i_{lr}$ is the resonant inductance current. It can be seen that the resonant inductance current is a periodic saw-tooth wave, while the clamping capacitor voltage is almost unchanged in a period. The simulation is consistent with the results from the previous analysis, further illustrating the accuracy of the constructed analysis.

The input phase currents and phase voltages are shown in Figure 12.

From Figure 12 The input current follows the change of the input voltage, thus realizing the purpose of power factor correction.
4.2. Verification of Experimental Platform

The experimental platform of 2.5 KW is shown in Figure 13.

The main circuit parameters are: input phase voltage $V_i = 110$ V, output DC voltage $V_o = 350$ V, input AC inductance $L = 0.5$ mH, switching frequency $= 15$ kHz, and load resistance $R = 50$ Ω. Auxiliary circuit parameters: resonant inductance $L_r = 50$ uH, switch parallel capacitor $C = 10$ nF, and clamp capacitor $C_c = 480$ uF.

Set the two important time parameters $t_{sd}$ to 2.5 us and $t_s$ to 10 us. The resonant inductance current and bridge arm voltage are shown in Figure 14, which are basically consistent with the simulation results.

![Figure 12. Input phase current and phase voltage.](image1)

![Figure 13. Experimental platform.](image2)

![Figure 14. The voltage on the bridge arm and resonant inductance current.](image3)
In order to further explain whether the main switch and auxiliary switch are turned on at zero voltage, the voltage waveforms on the bridge arm are expanded, and two time parameters are set, as shown in Figure 15.

![Figure 15. Main switch turned on at zero voltage.](image)

It can be seen that when the voltages are resonated to zero, the main switch and auxiliary switch are turned on to realize zero-voltage turn-on. Because of the existence of parallel capacitors, the switches can reach zero-voltage turn-off.

Figure 16 shows the input one of three phase volt and current.

![Figure 16. Input one of three phase volt and current.](image)

The discontinuity of the current in Figure 16 is the transition point of the working region. Because of the limited channel of oscilloscope, only one phase voltage and current waveforms are given here. It can be seen that the input current follows the change of the input voltage, thus realizing the purpose of power factor correction.

The efficiency curves of hard-switching and soft-switching three-phase PFC calculated from input and output power are shown in the Figure 17. It can be seen that the converter under soft-switching condition has higher efficiency.

![Figure 17. Converter efficiency curve.](image)
5. Discussion

The compound clamp ZVS three-phase VSR circuit mentioned in reference [19–21], achieves ZVS in all switches, including auxiliary switches. The auxiliary circuit is simple and the additional system has a low extra loss. However, the ZVSSVM controller must be implemented by intelligent chips such as DSP, which is complex and difficult to popularize. The governing equation of the one cycle controller, which is derived based on the input current following the change of input voltage, determines the ability of the system to control the power factor close to 1 [22–28]. This paper adjusts and improves the original one cycle control strategy, by adding the driving signal of an auxiliary switch, which can complete the ZVS control of the compound clamp ZVS three-phase VSR circuit. Although only two switches on the main bridge arm are controlled, the conducting form of the third switch is replaced by the diode conducting in parallel with that switch. The improved one cycle control proposed in this paper share many similarities with the ZVSSVM control strategy in reference [19–21]. The major difference between the two systems stems from the use of ordinary circuits in the proposed technique to avoid complex computation used by the intelligent chip in ZVSSVM control strategy which needs to sample the voltage and current sensor signals and carry out multiple multiplications nonlinear operations to obtain the driving switch signals. There is a certain delay time in the process of data sample and calculation. The nonlinear multiplication operation brings calculation errors, and its anti-interference ability is not good enough. Due to the avoidance of complex calculation of the intelligent chip, the proposed system has better performance on real-time applications and stability.

Formula (2) indicates that the input impedance has become a factor in the signal $V_m$ rather than an estimated parameter. When the load changes, the input impedance also changes at the same time, then quickly reflects the signal $V_m$, and duty cycle adjustment is immediately started within the current control cycle. Therefore, different from traditional converter, the control system proposed in this paper has adaptive capability for input and output impedance. The proposed control algorithm is similar to the flat top SVM modulation method, so it can work at higher switching frequencies. In the denominator of the formula for calculating the pulse width of the flat-top SVM, there is a DC link voltage value factor, and the voltage pulsation of the dc link has a great disturbance to the PWM duty ratio, thus affecting the output voltage. Meanwhile, the duty cycle proposed in this paper is only related to the average input and output current after the equivalent transformation of Equation (3), which is also the reason why it is adaptive to the load.

This controller requires synchronous switching between the interval signal and the drive signal. Otherwise, the input currents will have a large current pulse overshoot, which may destroy the switches under high power output. In this paper, the drive signals ($S_n$ and $S_p$) are switched synchronously by the clock signal trigging, such that the input current waveform will not have large disturbance, as shown in Figure 16. In addition, the optimization design of relevant resonance parameters of this method can only be adjusted empirically, and there is no strict theoretical basis, which is the arrangement of the next research work.

6. Conclusions

An improved one-cycle control method combined with a compound active clamp ZVS three-phase rectifier circuit topology is proposed in this paper, which can achieve six main switches and one auxiliary switch working in zero-voltage. The validity of the theoretical analysis is verified by computer simulation and an actual 2.5 kW experimental platform. The one cycle controller with low cost is very simple, only needs an integrator with reset and other accompanying logic circuit, and is adaptive to the change of load with fast response and less overshoot. Compared with the traditional space vector modulation (SVPWM) control method, one-cycle control is simpler to construct, easier to debug, and the system is more stable and reliable with lower costs to implement.
Author Contributions: Q.Z. and Q.D. designed, debugged the system, built some parts of hardware, and performed the experiment; Q.Z. is also mainly responsible for the analysis, experiment, and preparing the paper; Q.D. supervised the design and analysis. All authors have read and agreed to the published version of the manuscript.

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Abbreviations

| Abbreviation | Description                                |
|--------------|--------------------------------------------|
| EMI          | Electromagnetic Interference               |
| PWM          | Pulse Width Modulation                     |
| CCM          | Continuous Current Mode                    |
| SPWM         | Sinusoidal Pulse Width Modulation          |
| SVM          | Space Vector Modulation                    |
| ZVSSVM       | Zero Voltage Switch Space Vector Modulation |
| ZVS          | Zero Voltage Switching                     |
| ZCS          | Zero Current Switching                     |
| DSP          | Digital Signal Processor                   |
| VSR          | Voltage Source Rectifier                   |
| PFC          | Power Factor Correction                    |
| ARCPL        | Auxiliary Resonant Commutated Pole Link    |
| ARDCL        | Auxiliary Resonant DC Link                 |
| ZCT          | Zero-Current Transition                    |
| OOC          | One Cycle Control                          |

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