Abstract—Noise analysis of a widely used switched capacitor unity gain sampler is presented, which in detail shows that the circuit structure can not only get rid of the offset voltage induced by the OTA involved, but also has the ability of suppressing 1/f noise with operation timing of the sampling capacitor, functioning as correlated double sampling in fact, however paying the price of increasing thermal noise. The noise analysis method starts from establishing noise model for the sampler in each individual clock phase. Then based on the characteristic of charge transferring by capacitors and theory of random process, the output noise power contributed by each noise source is derived, the key point of which is that how to determine whether the process of some noise source in some phase transferring to the output node is effected by filtering. At last optimization design for the capacitor elements, which determine the whole noise power, is conducted.

Keywords—Unity gain sampler; noise model; thermal noise; correlated double sampling; time domain noise simulation

I. INTRODUCTION

Switched capacitor (SC) circuits are typical mixed signal CMOS integrated circuits. Due to the advantage of precision, they are more and more widely used to implement signal processing functions. Unity gain (UG) sampler is one of the most essential constituent elements of SC circuits. The simplest structure of UG sampler is a switch and a sampling capacitor connected with a UG buffer, whose performance is degraded by the channel charge injection at the shutdown moment of the switch MOSFETs. To eliminate those unwanted charge injection, a type of SC UG sampler with elaborate designed switch timing is introduced[1][2]. Although it has better static performance, the temporal noise is inevitably increased by the extra two switches and timing operation[3][4].

This paper presents noise analysis and optimization for the UG sampler. The operation principle of which is introduced in Section II where the process of its offset canceling is described in detail. Section III gives the noise analysis and optimization of the circuit. At first noise model for the sampler in each individual clock phase is established according to timing operation of the circuit. Then based on the characteristic of charge transferring by capacitors and theory of random process, the output noise power is derived, from which it is seen clearly that the circuit structure has the ability of suppressing 1/f noise through the operation of the sampling capacitor, functioning as correlated double sampling, nevertheless in the price of increasing thermal noise. Optimization design for the capacitor elements, which determine the whole noise power, is conducted afterwards. The conclusion is provided in Section IV in the end.

II. CIRCUIT STRUCTURE

Fig.1 shows the structure and timing diagram of the UG sampler. There are two phases in the operation of the sampler, sampling phase starting at ‘t1’ ending at ‘t3’ and amplifying phase starting at ‘t4’[5]. When ‘t1’ comes, S1 and S2 are turned on, so the input signal $V_{IN}$, the offset voltage of the OTA denoted as $V_{OS}$ and the reference voltage $V_{REF}$ set at the of the positive node of the OTA is sampled on capacitor $C_H$, written as:

$$V_{C_H} = V_{IN} - V_{REF} - V_{OS}$$  (1)

$V_{C_H}$ represents the voltage across $C_H$. When ‘t4’ comes, S3 is turned on while the other two switches remain off. The voltage of the output node $V_{OUT}$ becomes:

$$V_{OUT} = V_{REF} + V_{OS} + V_{C_H} = V_{IN}$$  (2)

![Figure 1. Structure and timing diagram of CDS (a) Structure. (b) Timing diagram.](image)

It is clearly seen that $V_{OUT}$ is just equal to $V_{IN}$. $V_{OS}$ is eliminated by the two phase switched capacitor operation. So is the $V_{REF}$, which is applied to set the common mode input
voltage of the OTA in practical usage. It means that the user set $V_{REF}$ does not affect the unity gain sampling result.

III. ANALYSIS OF NOISE MODEL

The noise model of the UG sampler is shown in Fig.2, where $\text{en}_x$ represents the noise source from element X, such as S1, S2, S3 and OTA. According to the two individual operation phases, the noise models at different phases are built, respectively, which certainly causes diverse noise transferring process. $R_{on}$ is the on-resistance of the switches involved. $r_O$ and $C_L$ represent output resistance and output capacitance of the OTA. Due to the two operations based on the clock timing bringing discontinuity to the output, noise analysis should be derived from time domain.

At the beginning point of sampling phase, ‘t1’, the noise voltage across $C_{Hi}$ starts to generate, for $t_1 \leq t \leq t_2$ , $V_C(t)$ can be expressed as:

$$V_C(t) = \left[ V_{nS1,sp}(t), V_{nS2,sp}(t), V_{nOP,sp}(t) \right] * \begin{bmatrix} h_{S1,sp}(t) \\ h_{S2,sp}(t) \\ h_{OP,sp}(t) \end{bmatrix}$$

Where $V_{nS1,sp}(t)$, $V_{nS2,sp}(t)$ and $V_{nOP,sp}(t)$ are time domain noise sources making contributions in the sampling phase.

Starting from ‘t4’, the amplifying phase begins. The noise model becomes the one shown in fig.2(b). The output noise $V_{out}(t)$ can be computed by:

$$V_{out}(t) = \left[ -V_C(t_2), V_{nS3,ap}(t), V_{nOP,ap}(t) \right] * \begin{bmatrix} h_{C,ap}(t) \\ h_{S3,ap}(t) \\ h_{OP,ap}(t) \end{bmatrix}$$

Where $V_{nS3,ap}(t)$, $V_{nOP,ap}(t)$, $h_{S3,ap}(t)$ and $h_{OP,ap}(t)$ represent the noise sources and their unity impulse response, respectively, in the amplifying phase. $h_{C,ap}(t)$ corresponds to $V_C(t_2)$ in the phase. It can be seen that the part that $V_C(t_2)$ contributes is a step signal transferring through a linear system, the outcome of which approximates $V_C(t_2)$ itself. The three switch noise sources are uncorrelated in each phase, while $V_{nOP,ap}(t)$ correlates with $V_{nOP,ap}(t)$.

From frequency domain:

$$e_{nOP,ap}(f) = e_{nOP,ap}(f) \cdot e^{j2\pi f \Delta T}$$

Where $e_{nOP,ap}(f)$ and $e_{nOP,op}(f)$ are the fourier transform of $V_{nOP,ap}(t)$ and $V_{nOP,op}(t)$, respectively, which are defined as the power spectrum density(PSD). $\Delta T = t_4 - t_2$ is the time interval between the two phases. After finding out the relationship of each noise source transferring to the output node, We can deduce the PSD of output noise, $e_{nOUT}(f)$:

$$e_{nOUT}(f) = e_{nS3,ap}(f) H_{S3,ap}(f) - e_{nS1,sp}(f) H_{S1,sp}(f) - e_{nS2,sp}(f) H_{S2,sp}(f) - e_{nOP,ap}(f) \left[ H_{OP,ap}(f) - H_{OP,op}(f) \cdot e^{j2\pi f \Delta T} \right]$$

Where $H(f)$ is the frequency domain transfer function of its corresponding $h(t)$. The total output noise power can be obtained by integrating $e_{nOUT}^2(f)$ from dc to infinity:

$$P_{OUT}(f) = \int_0^\infty e_{nOUT}^2(f) df$$
These five transfer functions are listed below, where \( g_m^r \) is actually the low frequency of the OTA, which is deemed as far larger than 1:

\[
H_{S1,op}(f) = \frac{1}{1 + \left( \frac{s}{g_m^r / C_L} \right)}
\]

\[
H_{S2,op}(f) = \frac{1}{1 + \left( \frac{s}{g_m^r / C_L} \right)^2 + \left( \frac{2R_{ON}C_H}{g_m^r / C_L} \right)^2}
\]

\[
H_{OP,op}(f) = \frac{1}{1 + \left( \frac{s}{g_m^r / C_L} \right)^2 + \left( \frac{2R_{ON}C_H}{g_m^r / C_L} \right)^2}
\]

\[
H_{OP,ap}(f) = H_{S3,ap}(f) = \frac{1}{1 + \left( \frac{s}{g_m^r / C_L} \right)^2 + \left( \frac{2R_{ON}C_H}{g_m^r / C_L} \right)^2}
\]

According to the equations given above, firstly let’s discuss 1/f noise that comprises \( L \) contributing to the output noise. The two transfer functions corresponding to \( L \) in each phase are both low pass filters, the cutoff frequency of which are in the same order. So based on the last term in equation (6), within low frequency region, both \( H_{OP,op}(f) \) and \( H_{OP,ap}(f) \) can be approximated as unity, thus 1/f noise part of the output noise can be expressed as:

\[
e_{OUT,S1}^2(f) = e_{OP,op}^2(f) \left| 1 - e^{j2\pi 1/\Delta T} \right|^2
\]

\[
e_{OUT,S2}^2(f) = e_{OP,op}^2(f) (1 - \cos 2\pi f \Delta T)
\]

If \( \Delta T \) is sufficiently small, which in many cases stands still, the 1/f noise part, which can be calculated by

\[
e_{OUT,S1}^2(f) = \int_0^\infty e_{OP,op}^2(f) \int |1 - e^{j2\pi 1/\Delta T}|^2 df
\]

\[
e_{OUT,S2}^2(f) = \int_0^\infty e_{OP,op}^2(f) (1 - \cos 2\pi f \Delta T) df
\]

In the majority of application cases, \( g_m^r R_{ON} \ll 1 \), therefore the noise power dedicated by each noise source computed based on the above five equations can be simplified to expressions that are listed in Table I:

| Source | Expression |
|--------|------------|
| \( v_{OUT,S1}^2 \) | \( \frac{kT}{2 \left( 1 + \frac{C_H}{C_L} \right)} C_H \) |
| \( v_{OUT,S2}^2 \) | \( \frac{kT}{2 \left( 1 + \frac{C_H}{C_L} \right)} C_H \) |
| \( v_{OUT,S3}^2 \) | 0 |
| \( v_{OUT,OP}^2 \) | \( \frac{4kT \gamma}{3 \left( (C_L + C_H) + \frac{C_H}{C_L} \right)} \) |

![Figure 3. Noise model of the UG sampler.](image)
We can see that S3 contributes nearly zero compared with the other noise sources. The part that S1 and S2 contribute is almost the same, which is increasing function of $C_L$ and decreasing function of $C_H$. In the meanwhile $v_{n_{OUT,op}}^2$ decreases with the two capacitors increasing. The whole output noise, $v_{n_{OUT}}^2$ which is the sum of the four items in table I, in the condition of the layout area that distributed to capacitor design is constraint, apparently has an optimization point, where the UG sampler obtains the minimum noise.

Fig. 3 shows how $v_{n_{OUT}}^2$ varies with $C_H$, where the x-axis is the percentage of $C_H$ occupying the sum of $C_H$ and $C_L$, the y-axis stands for $v_{n_{OUT}}^2$ divided by $kT$. With $\gamma$ increasing, the best point leads to smaller $C_H$ because of the part of OTA noise contributing more, which needs larger $C_L$.

IV. CONCLUSION

This paper proposed a noise analysis and optimization method for a UG sampler that has the ability of not only canceling the offset voltage of the OTA involved but also suppressing its 1/f noise. The noise analysis method starts from establishing noise model for the UG sampler in each individual clock phase. Then the output noise power contributed by each noise source is derived, with which the optimization design for the capacitor elements, which determine the whole noise power, is conducted finally.

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