Dielectric Properties and Ion Transport in Layered MoS$_2$ Grown by Vapor-Phase Sulfurization for Potential Applications in Nanoelectronics

Melkamu Belete$^{1,3}$, Satender Kataria$^{‡}$, Ulrike Koch$^{5}$, Maximilian Kruth$^{§}$, Joachim Mayer$^{⊥}$, Olof Engström$^{3}$, and Max C. Lemme$^{*,†}$

$^1$RWTH Aachen University, Faculty of Electrical Engineering and Information Technology, Chair of Electronic Devices, Otto-Blumenthal-Strasse 2, 52074 Aachen, Germany
$^2$AMO GmbH, Advanced Microelectronic Center Aachen, Otto-Blumenthal-Strasse 25, 52074 Aachen, Germany
$^3$University of Siegen, Department of Chemistry and Biology, Adolf-Reichwein Strasse 2, 57076 Siegen, Germany
$^4$RWTH Aachen University, Central Facility for Electron Microscopy, Ahornstrasse 55, 52074 Aachen, Germany
$^⊥$Ernst Ruska-Centre for Microscopy and Spectroscopy with Electrons, Research Centre Jülich, 52425 Jülich, Germany

ABSTRACT: Electronic and dielectric properties of vapor-phase grown MoS$_2$ have been investigated in metal/MoS$_2$/silicon capacitor structures by capacitance–voltage and conductance-voltage techniques. Analytical methods confirm the MoS$_2$ layered structure, the presence of interfacial silicon oxide (SiO$_x$) and the composition of the films. Electrical characteristics in combination with theoretical considerations quantify the concentration of electron states at the interface between Si and a 2.5–3 nm thick silicon oxide interlayer between Si and MoS$_2$. Measurements under electric field stress indicate the existence of mobile ions in MoS$_2$ that interact with interface states. On the basis of time-of-flight secondary ion mass spectrometry, we propose OH$^-$ ions as probable candidates responsible for the observations. The dielectric constant of the vapor-phase grown MoS$_2$ extracted from CV measurements at 100 kHz is 2.6 to 2.9. The present study advances the understanding of defects and interface states in MoS$_2$. It also indicates opportunities for ion-based plasticity in 2D material devices for neuromorphic computing applications.

KEYWORDS: 2D materials, MoS$_2$, vapor-phase sulfurization, dielectric constant, mobile ions, interface states, defects, bias-stress

INTRODUCTION

Transition metal dichalcogenides (TMDs) are among a large family of two-dimensional (2D) layered materials. They are generically described by the formula MX$_2$, where M represents a transition metal such as molybdenum (Mo), tungsten (W), niobium (Nb) and others, and X stands for a chalcogen element, that is, sulfur (S), selenium (Se), or tellurium (Te).$^{1,2}$ Bulk TMDs are formed from vertically stacked 2D-layers that are held together by van der Waals forces, typically at an interlayer spacing of less than 1 nm. The electronic properties of TMDs range from semiconducting to superconducting, and include direct and indirect energy band gaps that depend on the number of layers.$^1$ Molybdenum disulfide (MoS$_2$) is a semiconducting TMD material with a band gap ranging from 1.3 eV in bulk to 1.88 eV as a monolayer.$^{1,3}$ Appealing properties of single- and multilayer MoS$_2$ have made the material a potential candidate for applications in nanoelectronics, optoelectronics and neuromorphic computing.$^{4−13}$ Interest for such applications of 2D materials is generally not limited to devices made from single atomic layers, but rather include multiple 2D layers and heterostructures thereof. Most of the early stage research on MoS$_2$ has been conducted on small flakes obtained through mechanical exfoliation$^{14}$ or chemical exfoliation.$^{15,16}$ Although these techniques can yield high quality MoS$_2$, they are not suitable for large scale applications as they are limited to small flakes.$^{17}$ More recently, CVD growth from gaseous precursors and thermal conversion of metal films (vapor-phase sulfurization) have been proposed as scalable methods for MoS$_2$ growth.$^{18−22}$ Here, the latter technique has been used to grow large area MoS$_2$ directly on silicon (Si) substrates.

Most of the research on electronic devices based on single- and few-layer MoS$_2$ has focused on lateral transport properties of MoS$_2$. In this work, we investigate layered MoS$_2$ on Si substrates with respect to its dielectric properties perpendicular to the substrate, for a potential application as a dielectric barrier material in vertical heterostructure devices, such as graphene and 2D materials-based hot electron transistors (HETs), which are potential devices for high speed electronics.$^{23−27}$ The small area MoS$_2$ flakes obtained through CVD growth are more suitable for large scale applications as they are formed directly on the substrate. These flakes were subsequently used to fabricate metal/MoS$_2$/silicon capacitor structures for the investigation of the electronic and dielectric properties. As part of this research, we have investigated the structural, electrical and dielectric properties of vapor-phase grown MoS$_2$.

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band gap of MoS$_2$ compared to available oxides$^{1,3}$ and its low band offset with respect to silicon (Si)$^{1,3,28}$ makes it a good candidate for efficient emission barriers in HETs. In combination with an ultrathin dielectric layer, MoS$_2$ could also serve in a bilayer tunnel barrier configuration, which has been shown to enhance HET on-current levels.$^{30}$ In this context, it is essential to understand the electronic and dielectric properties of MoS$_2$ as a barrier material. We have thus investigated capacitors, with MoS$_2$ as the dielectric, through capacitance−voltage ($C$−$V$) and conductance−voltage ($G$−$V$) measurements.

### RESULTS AND DISCUSSION

The device fabrication process flow and the associated MoS$_2$ synthesis procedure are illustrated with schematics shown in Figure 1a and 1b, respectively. An optical micrograph of one device can be found in Figure 1c. The MoS$_2$ films were characterized by Raman spectroscopy after growth. The resulting Raman spectrum (Figure 2a) corresponds to the 2H MoS$_2$ phase and shows the two prominent peaks ($E_{2g}^{1}$ and $A_{1g}$), indicating the formation of crystalline MoS$_2$.$^{31,32}$ The $E_{2g}^{1}$ peak is attributed to the in-plane vibrations of Mo and S atoms, while the $A_{1g}$ peak signifies the out-of-plane vibrations of S atoms.$^{32}$ Cross-sectional TEM investigations have been employed to visualize the layer sequence pertained in the metal−semiconductor−semiconductor (MSS) structure and the associated interfaces. Figure 2b reveals a clearly layered structure of the MoS$_2$ film, which is nanocrystalline in nature and where most of the layers are oriented nearly vertical with respect to the Si face. Such vertically aligned layers are commonly observed in thick MoS$_2$ and other TMD films grown by vapor-phase sulfurization.
The TEM images further show a ~2.5–3 nm thick amorphous SiOx interfacial layer (IL) between Si and MoS2, which is consistent with earlier reports involving MoS2 growth on Si.\textsuperscript{32,33} The presence and formation of this SiOx layer can be attributed to (1) post-HF treatment regrowth of native oxide on the Si surface before the Mo film deposition and (2) oxidation of the Si surface by oxygen from water molecules intercalated at the Si–Mo interface while heating up the samples during the sulfurization process. Unlike the work of Liu et al., we do not observe the formation of an interfacial silicon oxide at the surface of the MoS2 films.\textsuperscript{36} ToF-SIMS measurements provide a depth profile of the chemical composition of the samples (Figure 2c). In addition to the expected elemental/molecular composition of the intended layers, we observed the presence of negatively charged chloride (Cl\textsuperscript{–}) and hydroxyl (OH\textsuperscript{–}) ions. The latter likely originate from the introduction of water during processing and consecutive catalytic water splitting. The methods section provides details on the ToF-SIMS measurements.

C–V and G–V measurements were carried out in a Lakeshore cryogenic probe station connected to a Keithley K1-590 admittance meter in vacuum (10\textsuperscript{–4} mbar) and at room temperature. C–V characteristics measured at 100 kHz signal frequency on the MoS2 capacitors with p- and n-Si substrates are shown in Figure 3. The shape of these graphs resembles that of typical metal/oxide/silicon (MOS) structures,\textsuperscript{37} with capacitance saturation over a large voltage range for the p-type samples (Figure 3a). The n-type samples also exhibit saturation (Figure 3b), but leakage current dominates for gate voltages above 4 V. As a consequence, the measured capacitance starts to drop below the saturation level above that voltage (not shown). On the basis of the C–V measurements, we calculated the dielectric constant values for the vapor-phase grown MoS2 using

$$C_{\text{ins}} = \frac{C_{\text{SiO}_x} C_{\text{MoS}_2}}{C_{\text{SiO}_x} + C_{\text{MoS}_2}}$$ (1)

where the insulator capacitance $C_{\text{ins}}$ is analogous to the oxide capacitance of conventional MOS capacitors, $C_{\text{SiO}_x}$ is the IL capacitance, and $C_{\text{MoS}_2}$ is the MoS2 capacitance. In this calculation, $C_{\text{ins}}$ is considered to be the equivalent capacitance of the SiOx and the MoS2 capacitors that are connected in series. It is obtained from the saturation part of the C–V curves shown in Figure 3. When the measured capacitance saturates, as observed in the C–V characteristics in the range from −4 to 0 V in Figure 3a and for about +4 V in Figure 3b, the total capacitance is given by the combination of the interfacial layer- and MoS2- capacitances ($C_{\text{SiO}_x}$ and $C_{\text{MoS}_2}$) which are independent of voltage (i.e., eq 1).\textsuperscript{37} The extracted dielectric constant values are in the range of 2.6–2.9. Santos and Kaxiras\textsuperscript{38} suggested that the dielectric constant of MoS2 varies with applied external electric fields ($E_{\text{eff}}$) and number of layers. In our measurements, the electric fields at which the capacitance started to saturate were in the range of 0.0033–0.02 V/Å. For this field range, the predicted MoS2 dielectric constant of approximately 3\textsuperscript{39} is in reasonable agreement with the extracted values of the present work. However, we note that the theory was based on horizontally aligned MoS2 layers, while the experiments were carried out on MoS2 with vertically aligned layers (Figure 2b). Thus, the polycrystalline nature of the experimental MoS2 and its vertical layer orientation is likely to result in different measured dielectric constants compared to simulated data that assumes single crystal MoS2.

The C–V measurements indicate that energy barriers exist between Si and MoS2 for both holes and electrons, and that they are sufficiently high to establish accumulation of carriers at the Si band edges (i.e., saturating CV curves). The magnitude of these barriers depends on energy band alignment, which could vary between the following two extremes: (1) Assuming that the band alignment is entirely determined by electron affinities, one would expect a “Type-I” (straddling) gap,\textsuperscript{37} where the barrier heights are determined by the difference between the electron affinities of the two materials in contact. (2) Assuming that the alignment is mainly controlled by the existence of “virtual gap states”, a “Type-II” (staggered) gap\textsuperscript{37} will form. In this case, the hole barrier is expected to be considerably larger than the electron barrier, which is in accordance with the present observation of current leakage mentioned earlier. In reality, however, one may expect a combination of the two phenomena.\textsuperscript{40} The presence of two interfaces (i.e., Si/SiOx and SiOx/MoS2) in the present devices makes the situation even more complicated as the band alignment can be influenced by virtual gap states in both SiOx and MoS2 layers. Furthermore, as will be discussed below, negative charge close to the Si/MoS2 interface may give rise to a bending of the MoS2 energy bands to form an additional barrier for electrons. On the basis of the saturation effects observed in the C–V data discussed above, we propose simplified energy band schemes (Figures 3c and 3d) for the present MSS structures. These band schemes feature a SiOx transition layer, where $x \leq 2$, between Si and MoS2. Compared to a standard pure SiO2 gate oxide, this interfacial layer seems to be more permeable to charge carriers. The leakage current through the SiOx transition layer in the present MSS structures (Figure S1) was examined and found to be about 3 orders of magnitude higher than leakage current reported for standard SiO2 of comparable thickness and applied gate voltage.\textsuperscript{41} This indicates that the interfacial layer in the current device is of poor quality, possibly due to oxygen deficiencies and other defects favoring leakage.
For further investigation, we performed bias-stress (BS) measurements on the MSS devices. BS measurements allow investigating charge dynamics in dielectrics and at their interfaces, and also to study the effect of interface states on the C–V and G–V characteristics. Here, a reference C–V curve was first measured without BS with 70 ms delay between data points. Next, bias stress of $V_{\text{Gstress}} = 4$ and $-4$ V was applied for 1 min, followed by C–V and G–V measurements that were run with the shortest possible delay between data points (i.e., 1 ms). This resulted in shifting of the curves along the voltage axis. Subsequent BS cycles were applied until the curves did not exhibit further observable shifts. Figure 4a shows C–V characteristics for the MSS capacitors on n-Si measured under positive BS of $V_{\text{Gstress}} = 4$ V, which shifts the curves to the left along the voltage axis. In addition, the curves exhibit a hump that increases for increasing positive BS cycles. A similar developing trend can also be observed in the G–V characteristics with clear shifts of the capacitance curves to the left under positive BS. (b) Corresponding G–V plots confirming the shifting trend. The voltages at which the conductance maxima occur correspond to bias voltages assigned to distinct humps in the C–V curves. (c) C–V measurements under negative BS, where the capacitance curves shift to the right. (d) Corresponding G–V plots with similar shift direction and with peaks of slightly decreasing amplitude. In all measurements, the first black curves were measured without BS and with a 70 ms delay between data points. Each of the remaining curves were measured successively after 1 min BS and with 1 ms delay. For clarity reasons, all the graphs in this figure present magnified versions of the measurements in a smaller voltage range. In addition, negative BS measurements were done first and positive BS next, but again for convenience during discussions, they are presented in the opposite order.

Figure 5. BS C–V and G–V measurements on MSS capacitors with p-Si at 100 kHz AC signal frequency: (a) C–V characteristics with clear shifts of the capacitance curves to the left under positive BS. (b) Corresponding G–V plots with peaks showing slight increase in amplitude and shifting to the left. (c) C–V measurements on the same device under negative BS. A “turn around” effect is observed: the first BS leads to a shift toward the left, but upon the second bias-stress cycle, the curves shift to the right. (d) Corresponding G–V plots with similar behavior. In all these measurements, the first black curves were measured without BS with a 70 ms delay between data points. The subsequent curves were measured after 1 min BS and with 1 ms delay. For clarity reasons, all the graphs in this figure present magnified versions of the measurements in a smaller voltage range. Negative BS measurements were done before those at positive BS, but for convenience they are presented in the opposite order.

The C–V data was further analyzed through simulations based on an equivalent circuit model. This was inspired by the experimental evidence of negatively charged ions within MoS$_2$ that may move in response to BS and interact with interface states to influence the capacitance measurements. The circuit configuration given by the capacitance meter to yield the measured quantities is depicted in Figure 6a. This configuration contains a capacitor and a conductor connected in parallel. However, the physical MSS system should be represented by more circuit elements (Figure 6b). This equivalent circuit model takes into account the capacitance contributions from the IL, $C_{\text{IL}}$, from MoS$_2$, $C_{\text{MoS}_2}$, and from the silicon depletion layer, $C_I$. The model also considers capacitance and conductance contributions from the interface states, $C_a$ and $G_a$, respectively. The capacitance and conductance contributions from interface
C represents data measured without BS and MC1, MC5 and MC13 are as presented in Figure 4a. The abbreviation D the capacitance per unit area and unit energy. 

The electron emission rates at the interface states are assumed to be much higher than the frequency of the AC probe signal from the capacitance meter, so that the trap states are completely emptied and filled within a period time of the AC signal. Therefore, the measured differential capacitance $C_m$ can be calculated as

$$C_m = \frac{C_{MoS_2} - C_{SiO_2}(C_+ + C_n)}{C_{MoS_2}C_{SiO_2} + (C_+ + C_n)(C_{MoS_2} + C_{SiO_2})}$$

where $C_m$ is the measured capacitance, $C_{MoS_2}$ is the MoS$_2$, $C_{SiO_2}$ is the IL (SiO$_2$) capacitance, $C_+$ stands for the silicon capacitance, and $C_n$ is the interface state capacitance as calculated using eq 3.

The theoretical capacitance was calculated using eq 4 and compared with experimental data. Figure 6c shows measured C–V curves (symbols) at four BS cycles and the corresponding theoretical fits (solid curves) by using $D_a$ distributions shown in Figure 6d. Each $D_a$ distribution was individually tuned to fit the respective theoretical C–V curve with the corresponding measured data. The model accurately describes the experimental data, including the amplitudes of the observed C–V humps (Figure 6c). These results confirm that the increasing amplitude of the C–V humps originate from the peaks in the $D_a$ distribution of interface states. The model in combination with the good fit to the experimental data also suggests that the active interface states, $D_a$ changes in concentration and energy maximum as a function of positive BS cycles.

These horizontal and vertical shifts of the C–V and G–V curves in response to BS can be attributed to the movement of negative mobile charges inside the MoS$_2$ bulk, and their interactions with interface electron states. Under negative BS, mobile negative charges are pushed toward the IL-MoS$_2$ interface, thus reducing the electrostatic passivation of interface states.

Integrating the capacitance density along $\Delta E$ results in the interface state capacitance, $C_{it}$, for a given Fermi-level position ($\Delta \mu$)

$$C_{it} = \int_{0}^{E_f} \chi_{it} d(\Delta E)$$

Figure 6. Calculation of C–V curves and fitting them to the experimental C–V data from MSS capacitors with n-Si measured under positive BS: (a) Equivalent circuit model with elements as measured by the C–V meter. (b) Equivalent circuit model with circuit elements representing the physical SSM device under test. (c) Calculated C–V curves (solid lines) fitted to the experimental C–V data measured at 100 kHz (dots). The first curve from the right represents data measured without BS and MC1, MC5 and MC13 are C–V curves measured after the 1st, 5th, and 13th BS cycle, respectively, as presented in Figure 4a. The abbreviation “MC” in the legend stands for “Measurement Cycle”. (d) $D_a$ distributions assumed to fit the theoretical C–V curves to the experimental data. Good agreement between the simulated and measured C–V data in combination with the $D_a$ trend strongly suggests that the negative C–V shift and the growing hump under positive BS is a result of the mobile negative ions in MoS$_2$ moving away from the SiO$_2$–MoS$_2$ interface, thereby reducing the electrostatic passivation of interface states.
layer formed on Si, which is very similar to the well-documented examples from research toward integration of high-k oxides in Si MOSFETs.42,43

Finally, the “turn-around” effect observed in the C−V and G−V curves for p-type samples after the first negative BS cycle warrants a discussion. Here, an initial shift of the curves in the negative voltage direction is followed by positive voltage shifts for succeeding stress cycles (Figure 5c and 5d). This indicates that either an increasing positive charge or a decreasing negative charge occurs close to the silicon side of the capacitor after the first cycle but not after those following. Taking into consideration the existence of hole accumulation at the Si/ 
S2O interface during negative BS, conceivable origins of this effect could be the interaction of holes either with traps of the SiO₂ layer or the moving ions, thus leaving a more positive oxide charge behind.

On the basis of the ToF-SIMS data, we propose that negatively charged mobile ions are responsible for the observed BS responses. In particular, because of a high possibility for adsorption of water molecules in the MoS2 layer during and after device fabrication, we consider hydroxyl ions (OH−) as probable candidates. These would be expected to originate from water splitting due to the catalytic properties of Cr and in particular candidates. These would be expected to originate from water splitting due to the catalytic properties of Cr and in particular MoS2.44−46 The predominantly vertical orientation of the MoS2 layers may in particular facilitate the mobility along the van der Waals gaps, which are oriented parallel to the electric field.

The results show certain plasticity of the device behavior as ions move inside the MoS2 film. Polycrystalline MoS2 films may thus enable future devices for integrated circuits with synaptic plasticity, which is an indispensable feature for hardware-based neuromorphic computing.8

■ CONCLUSIONS

Capacitors with vapor phase-grown MoS2 layers as dielectric were fabricated and characterized in detail. TEM images revealed a nanocrystalline nature of MoS2 and the formation of an amorphous SiO2 interfacial layer between Si and MoS2. The extracted dielectric constants of MoS2 are in the range of 2.6−2.9 for electric fields ≤0.02 V/Å. In addition, ToF-SIMS depth profiles suggest the presence of OH− ions in the devices. From theoretical calculations that were fitted to the experimental data, P2-like D0 peaks and their concentrations indicate the presence of significant amount of interface states and confirm the presence of mobile negative ions. Such features have so far been largely neglected in experiments using single- and multilayer MoS2 as an electronic material, for example, for few-layer MoS2 FETs. Since few layer 2D materials and their heterostructures are under intense investigation, this work should serve to alert the community about the downside of the catalytic behavior of MoS2, which may otherwise be explored in catalytic applications. Hence, this study indicates future challenges as the research on transition metal chalcogenides moves from exfoliated (near-perfect) flakes to materials grown with scalable, semiconductor fabrication compatible methods. Finally, ion- and defect-based phenomena in 2D materials including MoS2 and graphene22 may also be exploited in future neuromorphic computers, where neuromplasticity is a required feature.

■ METHODS

Metal−semiconductor−semiconductor (MSS) capacitors in which MoS2 is sandwiched between a metal and Si were fabricated on p- and n-type silicon (Si) substrates. First, hydrofluoric acid (HF) was used to remove native silicon oxide from the Si surface, followed immediately by e-beam evaporation of ~5 nm molybdenum (Mo) thin films on the Si substrates. Then, the samples were sulfurized in a tube furnace at 800 °C in argon (20 sccm) and sulfur atmosphere for a duration of 30 min.64 Throughout the sulfurization process, sulfur was kept at an upstream location of the tube where the temperature was around 150 °C and the growth pressure was around 2 × 10−3 mbar. The growth process yielded ~15 nm thick MoS2 films with height variations of approximately 1 nm, as confirmed by atomic force microscopy (AFM) measurements. Afterward, circular metal gates with a diameter of 100 μm were formed through a sequence of photolithography, deposition of a stack of chromium (Cr, 20 nm) and gold (Au, 120 nm) by thermal evaporation, followed by a lift-off process. Finally, the native oxide on the back side of the samples was removed by HF and a stack of Cr and Au was deposited as the back contact. A schematic diagram showing the complete process flow for fabricating the MSS capacitors is presented in Figure 1a. The vapor-phase sulfurization process is illustrated in Figure 1b and a top view optical microscope image of the as-fabricated device is shown in Figure 1c.

Raman spectroscopy and transmission electron microscopy (TEM) were carried out on the as synthesized MoS2 films to obtain information on the phase formation and structure of the films, respectively. A WITec alpha 300R system with 532 nm wavelength laser was used for the Raman measurements (Figure 2a), which were conducted using 1 mW of laser power and a 1800 g/mm grating. The TEM sample preparation was done in an FEI Helios NanoLab 600S FIB-SEM system, followed by NanoMill (cleaning with Ar ions) at 500 eV to get rid of the amorphous layer from the focused ion beam (FIB) irradiation. The clean samples (TEM lamellas) were then imaged using a FEI Tecnai G2 F20 TEM system at 200 kV. The resulting TEM image can be seen in Figure 2b. In addition, scanning electron microscopy (SEM) and X-ray diffraction (XRD) techniques were employed on the as-grown samples to obtain additional information. The resulting SEM image and XRD pattern confirm the homogeneous surface and 2H phase formation of MoS2, respectively (see Figure S4).

The chemical composition of the samples was also investigated with time-of-flight secondary ion mass spectrometry (ToF-SIMS) depth profiling. The ToF-SIMS measurements began by sputtering a target area on the samples with oxygen (O2) ions at 5 keV, which resulted in a 500 × 500 μm2 crater. This first step was carried out to remove possible contaminations on the topmost layers of the samples and reduce errors in the measurements. Then, bismuth ions (Bi+) were used at 25 keV to carry out the actual depth profile measurements within a smaller area (200 × 200 μm2) at the center of the larger crater. Each individual measurement was carried out after a 6 s presputtering step. Because the sample was sputtered with oxygen, metals form oxides, which appear in the mass spectra at relatively high signal abundance. The profiles presented in this work were measured in the negative ion mode, as the species of interest were best accessible that way. The ToF-SIMS depth profiles are presented in Figure 2c.

A Lakeshore cryogenic probe station connected to a Keithley KI-S90 admittance meter was used to measure C−V and G−V on the as-fabricated MSS devices, in vacuum (10−4 mbar) and at room temperature. Bias stress measurements were carried out such that the devices were first stressed at V = ±4 V for 1 min and then followed by a quick C−V measurement. The experimental data were then compared to a model calculated using eq 4 and D0 distributions as shown in Figure 6. Each D0 distribution was individually tuned so that the respective theoretical C−V curve fit the corresponding experimental data.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsanm.8b01412.

Brief discussion on the MoS2 dielectric constant, brief discussion about the effect of metal−MoS2 contact on the measured capacitance, SEM and XRD data showing surface morphology and 2H phase formation of MoS2,
bias-stress C–V on MoS2 capacitors with n-Si substrate, bias-stress C–V on MoS2 capacitors with p-Si substrate, and I–V characteristics showing clear asymmetry between the electron and hole current branches (PDF).

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