A self-aligned nano-fabrication process for vertical NbN–MgO–NbN Josephson junctions

A Grimm, S Jebari, D Hazra, F Blanchet, F Gustavo, J-L Thomassin and M Hofheinz

Univ. Grenoble Alpes, CEA, INAC, PHELIQS, LATEQS, F-38000 Grenoble, France
E-mail: max.hofheinz@cea.fr

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Abstract
We present a new process for fabricating vertical NbN–MgO–NbN Josephson junctions using self-aligned silicon nitride spacers. It allows for a wide range of junction areas from 0.02 to several 100 $\mu$m$^2$. At the same time, it is suited for the implementation of complex microwave circuits with transmission line impedances ranging from $<1$ $\Omega$ to $>1$ k$\Omega$. The constituent thin films and the finished junctions are characterized. The latter are shown to have high gap voltages ($>4$ mV) and low sub-gap leakage currents.

Keywords: superconducting circuits, nanofabrication, niobium nitride, Josephson junction

(Some figures may appear in colour only in the online journal)

1. Introduction

Josephson junctions are the key nonlinear element used in superconducting circuits [1–3]. In applications where large critical currents are needed, typically Nb–Al$_2$O$_3$–Nb, NbN–MgO–NbN or NbN–TaN–NbN junctions are used. This is the case for superconducting quantum interference device (SQUID) magnetometers [3], Josephson mixers [4] or rapid single flux quantum logic circuits [5]. The high critical temperature and large superconducting gap of Nb and NbN enable these devices to operate at liquid helium temperatures (4 K) and up to very high frequencies (above 1 THz for NbN). Such junctions are typically fabricated by first depositing the junction stack and then etching a pillar from it. The main difficulty is to contact the top of this pillar without short-circuiting it to the bottom layer. Common solutions to this problem, such as an additional insulating layer that is etched away above the pillar or anodic oxidation of Nb usually limit the minimum junction area to approximately 1 $\mu$m$^2$ [6–9] and lead to high critical currents and large shunting capacitances.

However, certain superconducting quantum circuits, such as Josephson qubits [10] and Josephson photonic devices, require these quantities to be small. Because of this, it is much more common to use Al–Al$_2$O$_3$–Al junctions, which can be fabricated using shadow angle evaporation; a technique allowing for very small Josephson junction sizes down to 0.01 $\mu$m$^2$ or less [11, 12]. The downside of this approach is that the low gap of Aluminum sets an ultimate limit for the fabricated devices in operation frequency (below 100 GHz) as well as temperature.

Here, we report on a fabrication process able to simultaneously obtain NbN–MgO–NbN junctions with surface areas as small as 0.02 $\mu$m$^2$ and as large as several 100 $\mu$m$^2$. This marks an important step towards bringing the advantages of NbN–MgO–NbN junctions to quantum circuits that were so far limited to Al junctions and opens the possibility for such circuits to operate at much higher frequencies. The presented NbN junction fabrication process also enables us to implement in parallel very versatile passive microwave circuits at no extra cost. The large kinetic inductance of NbN can then be used to design high impedance circuit elements.

Large superconducting gap and high impedance circuits are useful for many quantum circuits [13], particularly for ‘Josephson photonics’ devices, which are based on inelastic Cooper pair tunneling across a small Josephson junction: the junction is biased at a voltage $V$ below the gap and the energy $2eV$ of a tunneling Cooper pair creates one or several photons in the modes of the circuit in which the junction is embedded.
[14–18]. It may provide devices like quantum microwave sources [17, 19, 20], amplifiers [21] and single photon detectors [22] able, in principle, to function close to the gap frequency of the superconductor, approximately 1 THz for NbN. The nonlinearity of the coupling between tunneling Cooper pairs and photons increases with the characteristic impedance of the modes of the linear circuit in which the junction is embedded. Devices requiring nonlinearities at the single photon level, such as single photon sources and detectors, require electromagnetic modes with very high characteristic impedances of approximately $\frac{\hbar}{2} \approx 4 \text{ k}\Omega$ [19, 20, 22].

2. Fabrication of Josephson junctions

The NbN and MgO thin films are prepared by sputtering in an Alcatel SCM600 on Si(500 μm):SiO2(500 nm) substrates. After cleaning the wafers by back-sputtering in the deposition chamber, a 20 nm magnesium oxide (MgO) buffer layer is added as etch stop and to improve the superconducting properties of subsequent films. Then the active NbN(10 nm): MgO(4 nm):NbN(190 nm) junction stack is deposited (hereafter called the trilayer) [23].

The entire MgO–NbN–MgO–NbN stack is deposited in situ without exposing the sample to air between steps. Substrates are not actively heated, but their temperature increases above ambient temperature during the process. NbN films are prepared by reactive DC magnetron sputtering from a 150 mm Niobium target at 4 A and $\approx 400$ V in an atmosphere of 1.5 Pa of Ar and 0.2 Pa of N2. The latter partially nitrates the target surface after it has been conditioned in an atmosphere containing more N2. The deposition rate is $\approx 3.3 \text{ nm s}^{-1}$. For very thin layers we rotate the sample stage over different targets at $\approx 0.6 \text{ Hz}$ reducing the average deposition rate by approximately a factor of seven for a more precise control of thickness. Scanning electron microscope images of cuts through the produced NbN films show them to be columnar with an average column diameter of $\approx 20 \text{ nm}$.

The MgO barrier is RF magnetron sputtered at 450 W in an Ar atmosphere at 1.3 Pa for 100 s, in the same chamber as the NbN films, also while rotating the sample. For the deposition of the buffer layer we increase power to 550 W, keep the sample on top of the target and use an atmosphere of 1.25 Pa of Ar and 0.1 Pa of N2.

The aspect ratio imposed by the thickness of the deposited layers and the lateral junction sizes calls for very directional etch processes. We have developed several dry etch recipes on an Oxford ICP Plasmalab100 reactive ion etcher. During the etch, NbN is attacked both chemically, with SF6, as well as mechanically, with Ar (see table 1).

A moderate platen power generates an auto-polarization voltage of $\approx 190$ V accelerating the ions towards the sample and makes the etch more directional. Moreover, CH3F2 is added to the mixture, with the effect of polymerizing the exposed surface of the NbN film, making it less sensitive to the chemical etch. While in the vertical direction the Ar bombardment constantly ablates the polymer film and leaves the surface exposed to the chemical etch, the sidewalls of steps and trenches stay protected, preventing any undercut and assure smooth and steep sidewalls (see figure 1). This etch recipe hardens the resist sidewalls, which, when necessary, we remove after stripping with an O2 plasma (see table 2).

The MgO barrier is etched purely mechanically with an argon plasma. MgO is insensitive to the NbN etch described above, allowing us to use the buffer and barrier layers as effective etch stops, despite their very small thicknesses. Consequently the NbN etch can run longer to counteract inhomogeneities in deposition and etching rate across the wafer.

During the entire fabrication process described below optical lithography (OL) and electron beam lithography (EBL) steps are combined in order to be able to define small structures with high precision, while keeping the processing times for bigger structures such as coplanar waveguide (CPW) transmission lines [24] low. The following description will, however, focus on the elaboration of a single small Josephson junction and thus disregards some of the OL steps.

To begin with, a step is etched into the trilayer (see recipe table 1) using an EBL defined Ti(10 nm):Pt(60 nm) hard-mask (figure 1), which is subsequently removed with an Ar plasma. Next, the entire wafer is coated with a 300 nm thick film of Si3N4, deposited in a Corial D250L plasma enhanced chemical vapor deposition tool at 280 °C and 200 W at a pressure of 200 Pa with flows of 100 SCCM of SiH4, 500 SCCM of NH3 and 100 SCCM of Ar. A 10 nm thick layer of MgO is deposited on top of the SiN in order to protect it from overetching during some of the following fabrication steps.

An OL defines regions where the dielectric will be etched. The entire junction lies in such an area. First, the MgO in these areas is removed by a dip in 1% acetic acid. We then perform a directional dry-etch of the SiN, similar to the one developed for NbN (see table 3). The vertical thickness of the dielectric at the step is considerably bigger than elsewhere. Hence, it can be etched away on all flat surfaces while leaving behind a self-aligned spacer protecting the side of the trilayer (figure 1).

Finally, after a back-sputtering step, the NbN counter-electrode ($\approx 350 \text{ nm}$) is deposited using the same recipe as above. Another EBL defined hard-mask protects an area in the shape of a finger overlapping with the step. Once the unprotected areas are etched down all the way to the MgO tunneling barrier (see recipe table 1), this finger forms the vertical Josephson junction shown in figure 1.

3. Simultaneous implementation of passive elements

The fabrication steps used to implement the junction enable us to simultaneously fabri cate very versatile passive microwave circuits on the same chip. In particular, the process allows for various types of transmission lines: a fine defined
in the counter-electrode layer on top of the SiN forms a microstrip line together with the ground plane given by the trilayer. This case is ideal for low-impedance transmission lines (we estimate 65 Ω for 1 μm wide lines, down to <1 Ω for 100 μm wide lines. However, these impedances depend critically on the exact dielectric thickness and, because of high kinetic inductance fractions around 0.8, on the NbN material properties. CPW geometries using the full thickness of the trilayer can be tuned for transmission line impedances between 20 and 150 Ω [18]. This impedance and propagation speed are accurately controlled by lateral geometry because kinetic inductance fractions are low (<0.25 except for extreme geometries) and the substrate dielectric constant is well known. For even higher impedances, the dielectric on top of the CPW center conductor can be removed before the counter-electrode etch step. As a result, the upper part of the trilayer is etched away during this step, thinning down the center conductor to 10 nm like in the junction area (see figure 1). For such thin layers the NbN kinetic inductance dominates and leads to characteristic impedances of up to approximately 3.5 kΩ for a 1 μm wide wire. However, the propagation speed and characteristic impedance are then very sensitive to parameter fluctuations. We therefore typically place several variations of high-impedance elements on each wafer and post-select the device with the right parameters.

In areas where the SiN dielectric layer is not etched, it separates the trilayer and the counter-electrode, allowing for straightforward implementation of parallel plate capacitors. Where needed, holes can be etched in the dielectric to provide vias connecting the two layers. This enables us to fabricate crossovers between the ground planes of the CPW transmission lines, thus effectively eliminating parasitic modes [25–28].

4. Properties of the fabricated films and junctions

Temperature dependent resistance measurements of the deposited layers were performed in a Quantum Design physical property measurement system (see figure 2).

We calculate the value of the kinetic inductance \( L_{\text{kin}} \) from the square resistances \( R_\square \) (taken at 20 K) of the film, its thickness \( d \) and the superconducting gap \( \Delta \) estimated from the critical temperature, according to [29, 30] \( L_{\text{kin}} = \mu_0 \lambda \coth(d/\lambda) \). Here \( \lambda = (\hbar R d/(\mu_0 \pi \Delta))^{1/2} \) is the London penetration depth of a local superconductor in the low temperature limit \( k_B T \ll \Delta \) [31, 32]. For the bottom layer \( d \ll \lambda \) so that \( L_{\text{kin}} \approx \text{constant} \) can be estimated without knowing the exact film thickness.

A typical current–voltage characteristic of a superconducting interference device (SQUID) consisting of two parallel junctions with a total area of 0.04 μm² (squares of 150 nm side-length) measured at 4.2 K is shown in figure 3. The gap voltage \( V_{\text{gap}} \) can be defined as the voltage at the steepest part of the curve, where \( dV/dI \) is maximized [33]. Here, \( V_{\text{gap}} = 4.15 \text{ mV} \), corresponding to an emission frequency of \( \approx 1 \text{ THz} \) in the framework of Josephson photonics [14, 18, 34]. A normal state resistance \( R_N \approx 1.5 \text{ MΩ} \) can be extracted from the same curve above \( V_{\text{gap}} \) at 7 mV. Together with the Ambegaokar–Baratoff formula at zero temperature [35] \( I_c R_N = \pi \Delta(0)/2e \) and the relation \( 2\Delta = eV_{\text{gap}} \) we can evaluate the theoretical critical current at zero temperature to be \( \approx 2.2 \text{ nA} \). The critical current density is \( \approx 5.5 \text{ A cm}^{-2} \). Note that our junctions are optimized for low critical current densities; \( I_c \) can easily be increased by several orders of magnitude with this deposition process [23]. The current branch of the IV in figure 3 is not visible, because the associated energy scale [35] \( E_I = \Phi_0 I_c/(2\pi) \approx 4.5 \text{ μeV} \), where \( \Phi_0 \) is the magnetic flux quantum, is much smaller than the

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**Table 1.** Procedure of etching the trilayer and counter electrode in an Oxford Plasmalab 100 ICP etcher. Landing steps are performed to homogenize the NbN etch over the entire wafer and are possible because MgO provides a very good etch stop. Values in parentheses are used to start the plasma and then quickly ramped down to the regular parameters. The purely mechanical MgO etch steps are interleaved with in situ etch of the counter electrode and upper part of the trilayer (see text) the etch is stopped before the MgO step.

|          | CH₃F₂ (SCCM) | SF₆ (SCCM) | Ar (SCCM) | Pressure (mTorr) | ICP (W) | Platen (W) | Time (s) |
|----------|--------------|------------|-----------|------------------|---------|-----------|---------|
| Upper NbN | 25           | 5          | 40        | (15) 5           | 500     | 70        | EPD     |
| NbN      | 10           | 10         | 40        | 20               | 500     | 20        | 15      |
| landing  | MgO          | 100        | 5         | 500              | 150     | 20        |         |
| 4× Pump  |              | 0          | Atmosphere|                  | 150     |           |         |
| Vent     |              |            |           |                  |         |           |         |
| Lower NbN| 25           | 5          | 40        | (15) 5           | 500     | 70        | EPD     |
| NbN      | 10           | 10         | 40        | 20               | 500     | 20        | 15      |
| landing  |              |            |           |                  |         |           |         |

**Table 2.** Etch for removing resist residues after etching and stripping.

| O₂ plasma | Pressure (mTorr) | ICP (W) | Platen (W) | Time (s) |
|-----------|-----------------|---------|------------|---------|
| 45        | 30              | 500     | 0          | 300     |
Figure 1. Sample fabrication: (a) the different steps of the fabrication process. First the NbN–MgO–NbN trilayer is sputtered (1) and etched (2) using a Ti:Pt hard mask. Then a dielectric layer is deposited conformally by chemical vapor deposition (3) and etched directionally (using a Ti:Pt hard mask) to leave spacers passivating the trilayer sidewalls (4). Finally a counter electrode layer is deposited (5) and etched down to the junction barrier (6). (b) Finished 150 nm × 150 nm junction defined by EBL with a Ti:Pt hard mask still in place.
thermal energy at 4.2 K \((k_B T \approx 360 \mu eV)\). The ‘knee’ in the current–voltage characteristic is usually associated with the formation of a thin normal metal layer close to the junction barrier, possibly due to quasi-particle injection, and has frequently been observed in NbN–MgO–NbN Josephson junctions \([36–38]\).

In the context of this work we took particular interest in minimizing the leakage current under the gap \([18]\). In order to quantify the subgap leakage we compare the resistance under the gap \((R_N)\) at 3 mV to \(R_N\). A linear fit of the current voltage characteristic in figure 3 between \(-3\) and \(3\) mV gives \(R_N \approx 80 \text{ M}\Omega\) leading to \(R_N / R_S < 0.02\). While the measured gap voltage on this specific sample is lower than the best values reported in the literature, the subgap resistance is comparable to the best numbers achieved in other groups \([33, 38, 39]\), despite the fact that our junctions are significantly smaller than the smallest junctions reported so far (around 0.1 \(\mu m^2\) \([40, 41]\)), indicating that edge effects are not dominating subgap leakage.

5. Possible variations

The current process is not suitable for applications requiring resonators with very high quality factors, such as circuit QED. CPW resonators realized with this process \([18]\) typically have intrinsic quality factors of \(10^7\). We attribute this low value to dielectric loss in the MgO and SiO\(_2\) buffer layers. We expect a significant increase of this value by omitting the MgO buffer layers and using sapphire substrates instead. The latter allow to directly grow high quality NbN films without buffer layer and provide a good etch stop. If transmission lines with higher impedances are needed, the thickness of the lower NbN layer can be reduced. Replacing the silicon substrate with a silica substrate, increases the characteristic impedances of CPWs by another factor \(\sim 1.7\).

If high kinetic inductance is not desired, the process, with slight adjustments, should also be applicable to Nb–(Al)–Al\(_2\)O\(_3\)–Nb trilayers, where the barrier is formed by oxidizing a thin proximized aluminum layer. We expect such a process to yield lower leakage current below the gap because of the more uniform self-passivating barrier and more accurate control of circuit design parameters because of lower kinetic inductance fractions.

The critical current density is voluntarily kept low for the application in mind \([18]\), but can be increased by several orders of magnitude by decreasing the thickness of the MgO barrier layer \([23]\).

Finally, if only larger junction sizes are needed, the junctions can exclusively be defined by OL, considerably reducing fabrication times. In this case, the geometry is changed so that a counter-electrode wire crosses a trilayer wire. This makes the junction size insensitive to slight misalignments between the two OL steps.
6. Conclusion

In conclusion, we have developed a new fabrication process for vertical NbN–MgO–NbN Josephson junctions with self-aligned SiN spacers allowing for junction areas as small as 150 nm × 150 nm. The measured junction current–voltage characteristics show a high gap voltage and to our knowledge the lowest subgap leakage current at these junction sizes reported so far. The process allows for simultaneous fabrication of very large Josephson junctions and extremely versatile passive microwave circuits with characteristic impedances ranging from <1 Ω to >1 kΩ.

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