An Embedded RISC-V Core with Fast Modular Multiplication

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Abstract—One of the biggest concerns in IoT is privacy and security. Encryption and authentication need big power budgets, which battery-operated IoT end-nodes do not have. Hardware accelerators designed for specific cryptographic operations provide little to no flexibility for future updates. Custom instruction solutions are smaller in area and provide more flexibility for new methods to be implemented. One drawback of custom instructions is that the processor has to wait for the operation to finish. Eventually, the response time of the device to real-time events gets longer. In this work, we propose a processor with an extended custom instruction for modular multiplication, which blocks the processor, typically, two cycles for any size of modular multiplication when used in Partial Execution mode. We adopted embedded and compressed extensions of RISC-V for our proof-of-concept CPU. Our design is benchmarked on recent cryptographic algorithms in the field of elliptic-curve cryptography. Our CPU with 128-bit modular multiplication operates at 136MHz on ASIC and 81MHz on FPGA. It achieves up to 13x speed up on software implementations while reducing overall power consumption by up to 95% with 41% average area overhead over our base architecture.

Index Terms—RISC-V, iot, ecc, custom instruction, extension

I. INTRODUCTION

IoT market has been one of the driving forces of embedded hardware. Key enabler of IoT is cheap and capable hardware. There are multiple efforts, both in academia and industry, that are aiming to bring costs lower while making hardware more efficient in the tasks it is designed to perform. IoT end-node hardware should be secure and designed with power consumption in mind. Therefore, there are efforts on both designing new lightweight algorithms [1] that suit better to less powerful processors and designing specialized hardware that tackles the heavy operations more efficiently [2].

Custom instructions can be utilized for accelerating cryptographic operations. Fundamental and complex operations in cryptography can be mapped to custom instructions and implemented in hardware with fewer resources compared to full custom accelerators. This makes using the same hardware for different algorithms possible as custom instructions can be utilized in the realization of any algorithm. If the current algorithm turns out to be vulnerable, different solutions can be implemented via a software update without a significant performance penalty.

In this work we have designed a microprocessor core with its ISA extended with a custom instruction for Montgomery multiplication. Modular multiplication is highly utilized in public key cryptography. Our proposed custom instruction implementation can be executed both atomically and partially in short iterations, therefore does not degrade system response time. We implemented Embedded and Compressed extensions of RISC-V (RV32EC) [3] as the base ISA of our proof-of-concept CPU. Design is benchmarked with operations on various cryptographic elliptic curves. Synthesis is done for both FPGA and ASIC targets to collect area and power consumption metric. Our contributions can be summarized as follows:

- Propose a multiprecision MMUL custom instruction
- Propose a method to partition runtime of a long-latency custom instruction to increase responsiveness of the CPU to external events
- Analyze different RISC-V instruction encodings available to be used for custom instructions

In the literature, there are plenty of studies for adding custom instructions to RISC-V. Yet, none of them studies the effects of blocking the processor with a custom instruction or effects of the encoding within our knowledge.

II. MONTGOMERY MULTIPLICATION INSTRUCTION FOR RISC-V ISA

Modular multiplication is the operation of \( P = (A \cdot B) \mod N \). One of the key efficient algorithms in this area is Montgomery Multiplication [4]. For operands with length of \( n \) in bits, Montgomery multiplication calculates \( MMUL(A, B, N) = (A \cdot B \cdot R^{-1}) \mod N \) where \( R = 2^{(2n)} \mod N, 2^{n-1} < N < 2^n \) and \( \gcd(R, N) = 1 \). We chose the Radix-2 Montgomery Multiplication (R2MM) algorithm [5] for the implementation. R2MM is suitable for a simple hardware implementation as it is composed of additions and shifts.

In RISC-V, different instruction formats have already been defined. Some of them can be seen in Figure [1] Regardless of the instruction encoding, we decided MMUL instruction to work on memory addresses unlike any instruction in RISC-V specification, which strictly works on register values. When it comes to multiprecision operations, defining a unified interface on memory addresses is more performant. The key point that has to be made clear is the layout of in memory. Constraining how operands should be arranged may result in lower performance as it may require application code to rearrange operands in memory. MMUL requires 3 memory addresses
for the inputs and a single memory address for the output. Length of the operands must be encoded in the instruction for flexibility. Operand length may be limited by the hardware implementation of the MMUL instruction. In our reference design, maximum operand length is a hardware constraint that is defined at the synthesis phase.

![Image](imm rs1 fnc3 rd opcode) I-type

![Image](fnc7 rs2 rs1 fnc3 rd opcode) R-type

![Image](rs3 fnc2 rs2 rs1 fnc3 rd opcode) R4-type

Fig. 1. Candidate RISC-V instruction formats

If application can guarantee that all operands will be in a certain offset from a base address in memory as shown in Figure 2, a single memory address stored in rs1 is enough for the input operands. Thus I-type instruction format can be used. Fields fnc3 and imm provide 15 bits in the instruction to be used for encoding length, which can be encoded in bits to give a maximum of 32768 bit operands.

![Image](Fig. 2. Memory layout for I-type (left) and R-type (right) MMUL)

Likewise, if multiplicand and multiplier are guaranteed to be always in fixed positions relative to each other but modulus may be in random addresses as shown in Figure 2, R-type format can be used. Two source registers, rs1 and rs2, would be used as base addresses. The fnc3 and fnc7 fields give 10 bits of space which enables, if length is encoded in bits, a maximum of 1024 bit operands.

Lastly, for the best performance in all cases, if R4-type format is used, all operands can be in their independent addresses stored in rs1, rs2 and rs3 as shown in Figure 3. This format leaves only 5 bits (fnc3 and fnc2) which is not enough for length to be encoded in bits. Encoding operand length in words is another option which makes 1024 bit (2^{5} * 32) length operands for RV32 and 2048 bit (2^{5} * 64) operands for RV64 possible.

In this work, we decided to use R4-type instruction format because it imposes no memory layout restrictions. Using GCC directive .insn [6] in this decision process sped up the development.

As it can be seen in Figure 4, MMUL is coupled with the datapath of the processor. Addresses of the operands are read directly from their respective registers of the Register File and fed to the ALU in the datapath. Memory address to be worked on is calculated in the ALU by adding the offset value supplied by the MMUL to the base address read from the Register File. LSU is triggered by MMUL module to load or store from the calculated address. Operands are loaded at the start of the execution and stored in MMUL module during the entire operation. All execution is controlled by MMUL itself.

III. PARTIAL EXECUTION MODE

R2MM [5] has a loop with n iterations and one final subtraction after exiting the loop. Our implementation takes 2 clock cycles for each loop iteration and one last cycle for the subtraction. So in total, one MMUL operation takes 2n + 1 clock cycles for calculations, 3 * WORDS memory load operations for fetching the three operands and WORDS memory write operations for writing back the result where WORDS = ceil(n/WORD_SIZE).

As the instructions are atomic, during MMUL operation, processor will be unresponsive to any event that may happen. For some applications this may be problematic because of the real time constraints they have. To remedy this we can move the loop in our algorithm from hardware to software, allowing our processor to service interrupts in between loop iterations.

![Image](Fig. 5. MMUL partial execution time diagram)

To achieve this behaviour, which we call partial execution, our implementation has a special Control and Status Register

![Image](Fig. 3. Memory layout for R-type MMUL)

![Image](Fig. 4. Integration of MMUL in datapath)
If partial execution is enabled by a write with `csrwr` instruction to this register, which is directly connected to "Execution Mode Select" signal in Figure 4, current MMUL instruction is retired after each bit is processed. Application code has to execute another MMUL instruction for each bit of operands, i.e. n calls to the MMUL for an n-bit Montgomery multiplication operation, as shown in Figure 5. First call to the MMUL does the memory load operations, while last call writes back the result. In this case, maximum latency of MMUL instruction drops to either $3 \times \text{WORDS}$ memory load operations + 2 cycles or \text{WORDS} memory write operations + 3 cycles depending on the memory operation latencies. Performance penalty of this, which will be later presented, is minimal when used with loop unrolling.

IV. ANALYSIS

A. Base Architecture

To set a baseline for our work, we designed an in-order 2-stage RV32EC core with minimal area while maintaining comparable level of performance. Coremark and Dhrystone are run both on microriscy [7] and our core using the same memory modules. While our core scored 0.905 in Coremark and 1805 in Dhrystone, microriscy [7] scored 0.878 and 1644, respectively. Even though our core is slightly faster than microriscy, they can be considered equal in terms of performance.

B. Benchmarks

Our design is benchmarked with multiple ECC curves. Software implementations of FourQ (128-bit)[8], NIST P-256 (256-bit)[9], Curve25519 (256-bit)[10] and ARIS (an authentication scheme based on FourQ)[11] are run on our processor and microriscy/zeroriscy [7] cores from PULP as the reference designs. Later, modular multiplication and squaring implementations are replaced with a sequence of MMUL instructions and run on our modified core. No modifications are made to any other part of the code.

In Figure 6, speedup of ECC benchmarks can be seen. Full software benchmarks are run on microriscy/zeroriscy [7] and our base architecture (BA) as the control group. Tests where modular multiplication operation is implemented with our custom instruction are labeled Custom Instruction with Atomic Execution (CI-AE) and Custom Instruction with Partial Execution (CI-PE). There is a significant speed up in all curve operations. This speed up contributes to lowering total energy consumption. Our experimental setup uses a memory unit with single cycle read latency. Longer latency memories like EEPROM, FLASH are widely used as instruction memories. If a longer latency instruction memory was used in benchmarks, results would be even more in favour of our implementation. MMUL instruction takes multiple cycles thus allowing a new instruction to be fetched before it finishes, therefore CPU is less likely to be stalled waiting for new instructions.

Performance penalty of partial execution is negligible when paired with loop unrolling. Depending on the compiler output, if not interrupted, a Montgomery multiplication can be executed in the same amount of time as atomic execution.

For power consumption analysis, FPGA tools are used. Design is synthesized on a Xilinx XC7Z020-1 FPGA and activity data is gathered with Xilinx’s development environment,
Vivado. Activity data is then used to increase dynamic power estimation accuracy.

Power consumption of different configurations can be seen in Table I. While static power consumption shows only small changes, dynamic power goes down significantly. This can be explained with the power consumption per design block during fully software and with custom instruction runs of the benchmark (Table II). When executing solely standard instructions, as in BA column of Table II, every module of the CPU works synchronously. When MMUL instruction is in progress, rest of the CPU is idle. Biggest gain comes from the fetch stage because only four instruction fetches are needed per modular multiplication with our custom instruction and it is the biggest module in the design.

Both average power consumption and execution time go down in our implementation. Naturally, product of these two metrics follow this trend as well. Normalized energy consumption values can be seen in Table III. For FourQ, a 128-bit curve, roughly 90% of energy is saved while P-256/C25519, 256-bit curves, savings go up to 95%. As the prime that curves use gets bigger, performance increases and this results in higher energy savings. R2MM scales better for larger operands with an O(n) time complexity [5] [12].

V. Conclusion

In this paper, we proposed a microprocessor core with a custom instruction for Montgomery multiplication. Radix-2 Montgomery multiplication is implemented as an instruction. For better system response times, a partial execution scheme is proposed, enabling the instruction to be completed in multiple short-latency iterations. The resulting hardware is realized on FPGA and as an ASIC. 136 MHz clock speed on ASIC and 81 MHz clock speed on FPGA with 128-bit MMUL module is achieved. It achieves up to 13x speed up on various cryptographic curves compared to software implementations while reducing overall power consumption by up to 95%.

REFERENCES

[1] C. S. Division, I. T. Laboratory, N. I. of Standards, Technology, and D. of Commerce, “Lightweight cryptography.” [Online]. Available: https://csrc.nist.gov/projects/lightweight-cryptography

[2] B. Blaner, B. Abali, B. M. Bass, S. Chan, R. Kalla, S. Kunkel, K. Lauricella, R. Leavens, J. J. Reilly, and P. A. Sandon, “Ibm power7+ processor on-chip accelerators for cryptography and active memory expansion,” IBM Journal of Research and Development, vol. 57, no. 6, pp. 3:1–3:16, Nov 2013.

[3] “Official riscv foundation website,” Oct 2019. [Online]. Available: https://riscv.org/

[4] P. L. Montgomery, “Modular multiplication without trial division,” Mathematics of Computation, vol. 44, no. 170, pp. 591–592, 1985.

[5] A. F. Tenca and C. K. Koc, “A scalable architecture for modular multiplication based on Montgomery’s algorithm,” IEEE Transactions on Computers, vol. 52, no. 9, pp. 1215–1221, Sep. 2003.

[6] [Online]. Available: https://embarc.org/man-pages/ASRISC_002dFormats.html

[7] P. Davide Schiavone, F. Conti, D. Rossi, M. Gautschi, A. Pullini, E. Flamand, and L. Benini, “Slow and steady wins the race? a comparison of ultra-low-power risc-v cores for internet-of-things applications,” in 2017 27th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), Sep 2017, pp. 1–8.

[8] C. Costello and P. Longa, “Four: Four-dimensional decompositions on a q-curve over the merene prime,” in ASIACRYPT, 2015.

[9] P. Hess, “Sec 2: Recommended elliptic curve domain parameters,” 2000.

[10] D. J. Bernstein, “Curve25519: New diffie-hellman speed records,” in Public Key Cryptography - PKC 2006, M. Yung, Y. Dodis, A. Kiayias, and T. Malkin, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2006, pp. 207–228.

[11] R. Behnia, M. O. Ozmen, and A. A. Yavuz, “Aris: Authentication for real-time iot systems,” in ICC 2019 - 2019 IEEE International Conference on Communications (ICC), 2019, pp. 1–6.

[12] A. Karatsuba and Y. P. Ofman, “Multiplication of many-digital numbers by automatic computers,” in Doklady Akademii Nauk SS, vol. 14, no. 145, 1963, pp. 293–294.

[13] M. Samaila, J. Sequeiros, T. Simes, M. Freire, and P. Incio, “IoT-harps: A framework and roadmap for secure design and development of devices and applications in the iot space,” IEEE Access, vol. PP, pp. 1–1, 01 2020.

[14] E. Tehrani, T. Graba, A. S. Merabet, S. Guilley, and J. Danger, “Classification of lightweight block ciphers for specific processor accelerated implementations,” in 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2019, pp. 747–750.