An 8-bit digital-to-time converter with pre-skewing and time interpolation

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1 INTRODUCTION

Time-to-digital converters (TDCs) are the key blocks of time-based signal processing systems and TDCs with a high resolution are important in a broad range of applications. The resolution of popular flash TDCs is lower-bound by the minimum per-stage-delay set by the chosen technology. The resolution of Vernier TDCs can be an order of magnitude higher when compared with that of their flash counterparts. The large variation of per-stage-delay caused by process uncertainty, however, severely limits their ability to achieve a high resolution [1]. Although delta-sigma operations are capable of yielding a high resolution, the unavailability of high-order time integrators presently impose a stiff challenge in the realisation of high-order delta-sigma TDCs needed for achieving a high resolution [2–6]. Successive approximation register (SAR) TDCs shown in Figure 1a distinct themselves from others with a number of unique characteristics including a low sensitivity to process uncertainty, low power consumption, and full compatibility with technology. They are viable candidates for high-resolution TDCs [7–10]. The resolution of an SAR TDC is set by that of its digital-to-time converter (DTCs). DTC can be realised using a binary-weighted capacitor array with the drawback of a large area and a high level of dynamic power consumption [7, 11, 12]. DTC can also be realised using a delay line and a multiplexer, as shown in Figure 1b. These TDCs enjoy the advantages of a small area, a low level of power consumption, and full compatibility with technology with the limitation that resolution is lower bound by the per-stage-delay of the delay line set by the chosen technology [13, 14]. This article investigates two techniques, namely pre-skewing and digital time interpolation, to improve the resolution of delay line DTCs beyond per-stage-delay set by chosen technology [15]. The article is organised as follows: Section 2 investigates pre-skewing in lowering the per-stage delay of delay lines beyond that set by chosen technology. Section 3 studies digital time interpolators. Section 4 presents the design of an 8-bit DTC utilising both pre-skewing and time interpolation. In Section 5, design considerations including the maximum slope of the input of time interpolators, timing errors, and the layout of the DTC are examined. Section 6 provides the post-layout simulation results of the DTC. The article is concluded in Section 7.
2 | PRE-SKEWED DELAY LINE

Pre-skewing that utilises the output of the earlier stages of a delay line to pre-charge/pre-discharge the load capacitor of the current stage of the delay line is effective in lowering the per-stage-delay of the delay line [16–19]. Figure 2a shows a pre-skewed delay line with one pre-skewed inverter per stage. Let $V_x$ and $V_y$ be the voltages beyond which NMOS or PMOS transistors conduct, respectively. If no pre-skewing exists, $V_E$ will start to rise at $t_5$. When the pre-skewed inverter is present, $V_E$ will start to rise at $t_5$ at which the pre-skewing signal comes to effect, the charging process will then be accelerated at $t_5$ at which the primary input $V_D$ comes into action. It is noted that since the capacitance at node E increases due to the addition of the pre-skewed inverter, $V_E$ rises slower as compared with that without pre-skewing. Figure 2b compares the input and output of conventional and pre-skewed inverter. It is seen that the pre-skewing signal $v_{1a}$ gives rise to an early drop of $v_{01}$ prior to the arrival of the primary input $v_{1b}$, $v_{2a}$, on the other hand, will drop only after the arrival of $v_2$. It was shown in [20] that pre-skewing will be more effective when the number of pre-skewed inverters is small and its effectiveness will fade away once the number of pre-skewed inverters becomes large. Also, the speed gain from pre-skewing is at the cost of more power consumption and silicon area.

3 | DIGITAL TIME INTERPOLATION

Time interpolators that generate sub-transition edges between two transition edges can be loosely classified into analogue time interpolators and digital time interpolators [21, 22]. Analogue time interpolators obtain a fine time resolution using the digitally weighted tail current of differential amplifiers. They suffer from high power consumption, poor linearity, and poor compatibility with technology [23]. Digital time interpolation generates sub-transition edges using digital circuits only. It can be performed using resistor-based voltage division with the drawbacks of a low degree of interpolation and non-negligible static power consumption [24, 25]. It can also be performed using digitally weighted inverter arrays with the advantages of full compatibility with technology, no static power consumption, fast interpolation, and a high degree of interpolation [22, 26–28]. The output of a digital time interpolator with inputs $x_1$ and $x_2$ is given by

$$y = \alpha x_1 + (1 - \alpha)x_2$$  \hspace{1cm} (1)

where $0 < \alpha < 1$ is the interpolation word. By varying $\alpha$, a set of sub-edges between $x_1$ and $x_2$ are obtained. The adjustment of $\alpha$ is typically achieved by gating a set of identical inverters such as gated inverters [26], switched inverters [27], tri-state inverters [22], or current-starved inverters [28], as shown in Figure 3. For example, for 3-bit interpolation, a total of 16 identical gated inverters are needed, eight connected to $x_1$ and eight connected $x_2$. The interpolation word of $x_1$ is set by thermometer codes 00000000 ~ 1111111, corresponding to $\alpha = 0/8 \sim 8/8$. Similarly, the interpolation word of $x_2$ is set by the thermometer codes 1111111 ~ 00000000, corresponding to $1-\alpha = 0/8 \sim 8/8$. The interpolation words of $x_1$ and $x_2$ are complementary to each other.

When interpolation cell is inactive, its output should not be impacted by the signals to be interpolated ideally. Otherwise, the linearity of the interpolator will deteriorate. Gated inverter shown in Figure 4a offers good input-output isolation when the cell is not selected, or its input is grounded [26]. Switched inverter in Figure 4b suffers from poor input-output isolation due to the existence of a direct path from the input to the output formed by the gate-drain capacitance of the transistors [27]. Tri-state inverter in Figure 4c provides good input-output isolation [22, 29]. Current-starved inverter in Figure 4d offers the advantage of a constant output current, and subsequently has a better linearity but suffers from the need for current sources of a constant current. In addition, it also suffers from poor input-output isolation [28, 30, 31]. Cascade tri-state inverter shown in Figure 4e is proposed here. It provides improved input-output isolation as compared with the tri-stage inverter in Figure 4c. Figure 5 compares the input-output isolation of a tri-state inverter and that of a cascade tri-state inverter. It is seen that due to the larger dimension of PMOS transistors, charge injection and clock feed-through cause the output voltage of the tri-state inverter cell to climb steadily whereas their impact on the output voltage of the tri-state cascade inverter is negligibly small.

In the vicinity of the threshold-crossing of the inverters, transistors operate in saturation and function as current sources. The output current of the time interpolator is the sum of that of the inverters, yielding a good linear relation between interpolation word and the output current of the interpolator. Should the total output capacitance of the time interpolator be independent of the interpolation word, a perfect linear relation between the output voltage of the time interpolator and the interpolation word will exist. Consider the case where the time interpolator is made of a set of identical gated cascode inverters shown in Figure 3(e). The total output capacitance of the inverter is given by $C_{gdn} + C_{gdP}$ when $S = 1$ and $C_{dln} + C_{dLP}$ when $S = 0$ where $C_{gdl}$ and $C_{gdP}$ are the...
gate-drain capacitance of NMOS and PMOS transistors in triode, respectively, and $C_{gd,n}$ and $C_{gd,p}$ are the drain-substrate capacitance of NMOS and PMOS transistors, respectively. Although $C_{gd,n}$ and $C_{gd,p}$ in triode are much larger as compared with $C_{db,n}$ and $C_{db,p}$ and since the total number of cascode inverters switched on and those switched off is equal to the number of the bits of the interpolation word, and the total output capacitance of the time interpolator is independent of the interpolation word, thereby ensuring that a linear relation between the interpolation word and the output voltage of the time interpolator exists.

In the vicinity of threshold-crossing, the transistors of the interpolator operate in saturation and function as the current source, however, with a non-zero output conductance $g_o$, as shown in Figure 6. The dependence of the current flowing through $g_o$ on the output voltage of the interpolator and the input dependence of $g_o$ evidenced from

$$g_o = \frac{1}{2} \mu_n C_{ox} (V_{DD} - V_1 - V_T)^2 \lambda$$

where $\mu_n$ is the surface mobility of free electrons, $C_{ox}$ is the gate capacitance per unit area, and $\lambda$ is the channel length modulation coefficient with the signals to be interpolated giving rise to a non-constant output current. This is a fundamental cause of the non-linearity of digital time interpolators.

The linearity of the digital time interpolators is also affected by the slope of the signals to be interpolated. If the rise time $t_r$ of the signals to be interpolated is small, the output of the interpolator $y$ will remain unchanged in time interval $[t_1, t_2]$, giving rise to non-linearity, as illustrated Figure 6 [32]. To avoid this, a slope control block (SCB) that sets the slope of the signals to a desired value prior to interpolation is needed.
Lowering the slope of the output voltage of the SCB is at the expense of more power consumption due to the short-circuit current of the downstream time interpolator.

Figure 7 shows the schematic of a 2-bit digital time interpolator with cascode tri-state inverter cells. The load of the interpolator is an inverter. Figure 8 shows the output of the interpolator in TT and at FF and SS corners. It is seen that latency exists between the input and output of the interpolator, arising from the large capacitance at the output of the interpolator. It is also observed that the impact of the process uncertainty on the latency of the interpolator is the least at the FF corner and largest at the SS corner. Figure 9 plots the differential non-linearity (DNL) and integral non-linearity (INL) of the interpolator. It is seen that both DNL and INL of the time interpolator are small, revealing its excellent linearity. It is also observed that the impact of the process uncertainty on DNL and INL is negligible. Figure 10 plots the DNL and INL of the interpolator with supply voltage varied by ±10%. It is seen that the fluctuation of the supply voltage impacts the DNL and INL of the time interpolator rather marginally. Figure 11 plots the DNL and INL of the interpolator at various temperatures. It is seen that temperature variation impacts the DNL and INL of the time interpolator negligibly.

Figure 12 compares the DNL and INL of 4-bit time interpolators with switched inverters, tri-state inverters, and cascode tri-state inverters. It is seen that the time interpolator with cascode tri-state inverters outperforms the rest and was chosen.
FIGURE 8 Inputs and outputs of 2-bit time interpolator with cascode tri-state inverter cells. Inputs $x_1$ and $x_2$: 50 ps rise time with 10 ps space between them. Top: TT. Bottom: FF and SS. Thermometer-code interpolation word $S_4S_3S_2S_1$ is varied from 0000 to 1111.

FIGURE 9 Differential non-linearity (DNL) and integral non-linearity (INL) of 2-bit digital time interpolator with cascode tri-state inverter cells in TT and at FF and SS corners.

FIGURE 10 Differential non-linearity (DNL) and integral non-linearity (INL) of 2-bit digital time interpolator with cascode tri-state inverter cells in TT. Supply voltage is varied by $\pm 10\%$ from its nominal value.
4 | DIGITAL-TO-TIME CONVERTER WITH PRE-SKEWING AND INTERPOLATION

An 8-bit DTC employing both pre-skewing and digital time interpolation is shown in Figure 13. Input bits $D_3D_2D_1$ are assigned to a 16-stage pre-skewed delay line for coarse digital-to-time conversion and $D_0D_2D_1$ are assigned to a 4-bit digital time interpolator for fine digital-to-time conversion. Dummy stages are added to both ends of the pre-skewed delay line to ensure that the per-stage-delay of the stages multiplexed by the downstream multiplexer is the same. A transmission-gate (TG) multiplexer is chosen for its ease of accommodating a large number of inputs [26]. Dummy TGs are added at both ends of the multiplexer to ensure the capacitance of every input node of the multiplexer is the same. Buffers made of two cascaded inverters are inserted between the pre-skewed delay line and the multiplexer because the input capacitance of the TG multiplexer varies with its select word, as seen in Figure 14. If buffers were not added, the per-stage-delay of the pre-skewed delay line would vary each time the multiplexer select word changes. Figure 15 shows with the presence of the buffers, the impact of the varying input capacitance of the downstream TG multiplexer modulated by its select word vanishes. In order for the pre-skewed delay line to provide the delay that corresponds to $D_3D_2D_1$, only one bit of TG select word is set to 1. A decoder that maps $D_3D_2D_1$ to a 16-bit multiplexer select word that has one 1 and fifteen 0s is needed. The truth table of such a decoder is shown in Table 1. The TGs of the multiplexer are arranged in such a way that not only the edges corresponding to $D_3D_2D_1$ are selected and conveyed to the time interpolator, the capacitance seen at each input node of the multiplexer is independent of multiplexer select word. Since the capacitance at the output nodes of the multiplexer is excessively large arising from the large number of TGs connected to it, a pair of buffers is employed at the outputs of the multiplexer to set the slope of the input of the downstream time interpolation to the desired value. Note that the isolation buffers inserted between the pre-skewed delay line and the multiplexer do not affect the slope of the input of the time interpolator, subsequently its linearity. A binary-to-thermometer converter (BTC) that maps $D_3D_2D_1$ to a 16-bit thermometer code interpolation word is needed. Table 1 gives the truth table of the decoder (Table 2).

To illustrate how the DTC operates, let the input of the DTC be 01000001, as shown in Figure 16. The upper 4 bits of the input, 0100, are mapped to the 16-bit code 000000000010000. TGs highlighted in Figure 16 are switched on, allowing $T_4$ and $T_5$ to be conveyed to the time interpolator. The lower 4 bits of the input, 0001, are mapped to the 16-bit thermometer code

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**FIGURE 11** Differential non-linearity (DNL) and integral non-linearity (INL) of 2-bit digital time interpolator with cascode tri-state inverter cells in TT at various temperatures

**FIGURE 12** Differential non-linearity (DNL) (left) and integral nonlinearity (INL) (right) of 4-bit digital time interpolator with switched inverter, tri-state inverter, and cascode tri-state inverter cells in TT
FIGURE 13 8-bit digital-to-time converter with pre-skewing and time interpolation. BTC, binary-to-thermometer converter

FIGURE 14 Impact of the gating signals on the input capacitance of the transmission-gate. Minimum sized transistors are used

FIGURE 15 Impact of the isolation buffer. $v_{o1}$ and $v_{o2}$ are completely overlapped by each other
0000000000000001 that selects the highlighted sub-edge of the time interpolator.

5 | DESIGN CONSIDERATIONS

5.1 | Maximum slope of the interpolator inputs

The slope of the inputs of the time interpolators needs to be properly set in order to minimise the latency without jeopardising the linearity of the time interpolators. Prior studies showed that the slope of the signals to be interpolated needs to be at least 3 ~ 5 times the space between the inputs, however, without any analytical support [31–33]. Here, we derive the analytical relation between the slope of the signals to be interpolated and the space between them with the constraints of the minimum latency. To simplify analysis, we assume that the transistors of the interpolator operate in saturation throughout 0 ~ \( V_{DD} \). In Figure 17a, for time between A and C, although \( x_1 \) varies with time linearly, \( x_2 \) remains at 0. Similarly, for the time between D and B, \( x_3 \) varies with time linearly, whereas \( x_1 \) remains at \( V_{DD} \). In both cases, \( y \) exhibits a high degree of non-linearity. In Figure 17b, for time between A and B, both \( x_1 \) and \( x_2 \) vary with time linearly and \( y \) has a linear relation with \( x_1 \) and \( x_2 \). In Figure 17c, for the time between A and B, although \( x_1 \) and \( x_2 \) vary with time linearly and \( y \) has a linear relation with \( x_1 \) and \( x_2 \), the slope of the signals to be interpolated is unnecessarily low, resulting in excessive latency. Figure 17b thus gives the maximum slope of the inputs at which the latency of the interpolator is minimised without linearity degradation. The maximum slope of \( x_1 \) and \( x_2 \), denoted by \( S_{\text{max}} \), is therefore given by \( S_{\text{max}} = V_{DD}/(2T_{\text{in}}) \). The rise time of the inputs, denoted by \( \tau_{\text{rise}} \), is the amount of time for the inputs to rise from 10% \( V_{DD} \) to 90% of \( V_{DD} \). Since \( S_{\text{max}} = (0.9V_{DD} - 0.1V_{DD})/\tau_{\text{rise}} \), we have \( \tau_{\text{rise}} = 1.6T_{\text{in}} \).

| Ref. | Tech. (nm) | Res. (ps) | INL (LSB) | Power (mW) |
|------|------------|-----------|------------|-------------|
| [39] | 180        | 0.78      | 0.15       | 0.8         |
| [29] | 65         | –         | 1.33       | 4.3         |
| [22] | 28         | 0.244     | 1.2 ps     | 19.8        |
| Proposed work | 65 | 3.6 | 0.5 (R + C), 4 (R + C + CC) | 0.383 |

Abbreviations: INL, integral nonlinearity; LSB, least significant bit

| Table 1 | Truth tables of the MUX decoder and interpolator decoder |
|---------|----------------------------------------------------------|
| D_4D_3D_2D_1 | MUX select word | D_4D_3D_2D_1 | Interpolation word |
| 0000 | 0000000000000001 | 0000 | 0000000000000001 |
| 0001 | 0000000000000010 | 0001 | 000000000000011 |
| 0010 | 0000000000000100 | 0010 | 0000000000000111 |
| 0011 | 00000000000001000 | 0011 | 00000000000001111 |
| 0100 | 00000000000010000 | 0100 | 00000000000011111 |
| ... | ... | ... | ... |
| 1111 | 10000000000000000 | 1111 | 1111111111111111 |

Abbreviation: MUX, multiplexer

| Table 2 | Performance comparison |
|---------|------------------------|

Abbreviations: INL, integral nonlinearity; LSB, least significant bit

![Figure 16](image-url)  
**Figure 16** The operation of 8-bit digital-to-time converter with input \( D_k...D_0=01000001 \). BTC, binary-to-thermometer converter
The preceding approach, although simple, conveys a valuable insight on how the slope of the input affects the linearity of the interpolator. In what follows we present a more rigorous analysis. Using pinch-off condition, one can show that the NMOS and PMOS transistors of the interpolator will operate in saturation if $V_{Tn} < v_{in} < v_o + V_{Tn}$ and $v_o - |V_{Tp}| < v_{in} < V_{DD} - |V_{Tp}|$, respectively, where $V_{Tn}$ and $V_{Tp}$ are the threshold voltage of NMOS and PMOS transistors, respectively. Assume that the NMOS and PMOS transistors of the interpolator are saturated when $V_{Tn} < v_{in} < V_{DD}$ and $0 < v_{in} < V_{DD} - |V_{Tp}|$, respectively. In Figure 18a, for the time between A and D, the NMOS transistor of the interpolator whose input is $x_1$ does not operate in saturation. Similarly for time between C and B, the PMOS transistor of the interpolator whose input is $x_2$ does not operate in saturation. In both cases, $y$ exhibits a high degree of non-linearity. In Figure 18b, for time between A and B, both NMOS and PMOS transistors of the interpolator operate in saturation, $y$ has a linear relation with $x_1$ and $x_2$. In Figure 18c, for time between A and B, although both NMOS and PMOS transistors of the interpolator operate in saturation and $y$ has a linear relation with $x_1$ and $x_2$, unnecessary latency exists due to the overwhelming small slope of the inputs. Figure 18b thus gives the minimum latency without sacrificing linearity. The slope of $x_1$, denoted by $S_1$, and that of $x_2$, denoted by $S_2$, are given by $S_1 = V_{DD}/[2(T_{in} + \tau)]$ and $S_2 = V_{Tn}/\tau$. Since $S_1 = S_2$, we have $\tau = \left(\frac{2V_{Tn}}{V_{DD} - 2V_{Tn}}\right) T_{in}$. For a 65 nm 1.0 V CMOS technology, $V_{Tn} \approx 0.35$ V. We have $\tau = 2.3 T_{in}$. The maximum slope of the input is obtained from $S_{\max} = V_{DD}/[2(T_{in} + \tau)] \approx 0.15/T_{in}$.

The rise time of the input $\tau_{rise}$ is obtained from $(0.9V_{DD} - 0.1V_{DD})/\tau_{rise} = 0.15/T_{in}$ from which we arrive at $\tau_{rise} \approx 5.3 T_{in}$. The rise time of the inputs of the interpolator needs to be approximately 5 times the time space between the inputs in order to ensure that the transistors of the interpolator operate in saturation. This result agrees with the prior studies [31, 32]. Figure 19 plots the dependence of the INL of the 4-bit time interpolator investigated earlier on $T_{in}/\tau$. It is seen that INL deteriorates exponentially with the decrease of $\tau$ or equivalently the increase of the slope of the input to the interpolator.

5.2 Timing error

Device noise gives rise to timing errors in both the pre-skewed delay line and time interpolator. In this section, we provide a mathematical treatment of the timing errors of the DTC. Now, we investigate the timing error in the charging process of an inverter. The results can be readily used for the timing errors of the discharging process.

5.2.1 Thermal noise-induced timing error

Consider the charging process shown in Figure 20. Prior to the start of the charging process, the NMOS transistor operates in triode and functions as a resistor $r_{on}$ with a thermal noise voltage source $v_{n,tri}$ whose power spectral density is given by $S_{v_{n,tri}} = 4kT r_{on}$ where $k$ is Boltzmann constant, $T$ is
temperature, and \( r_{on,p} \) is the channel resistance. \( v_{\text{in},r_{on}} \) generates noise voltage \( v_{\text{nc},t1} \) across the capacitor with its power obtained from

\[
\overline{v_{\text{nc},t1}^2} = \int_{0}^{\infty} \frac{4kT r_{on}}{1 + (2\pi f r_{on} C)^2} df = \frac{kT}{C} \tag{2}
\]

After the charging process starts, the PMOS transistor will operate in saturation when \( v_c < |V_{TP}| \) and triode when \( v_c > |V_{TP}| \). To simplify analysis, we assume that the PMOS transistor functions as a current source over \( 0 \leq v_c \leq V_{DD}/2 \), an approach used in [34]. The thermal noise and flicker noise of the channel current of the transistor are integrated onto the load capacitor over \([0, t^*]\) where \( t^* \) is threshold-crossing time. Noise integrated onto the capacitor afterwards \( t^* \) does not contribute to timing errors. The noise voltage of the capacitor due to the thermal noise current \( i_{n,t} \) of the transistor, denoted by \( v_{\text{nc},t2} \), is given by [34].

\[
v_{\text{nc},t2} = \frac{1}{C} \int_{0}^{\infty} i_{n,t}(x) w(t-x)dx \tag{3}
\]

where \( w(t) = u(t) - u(t - t^*) \) and \( u(t) \) is the unit step function. Since \( W(s) = \frac{1}{s} \left( 1 - e^{-s t^*} \right) \), we have

\[
W(j2\pi f) = \frac{t^*}{\pi} \left[ \frac{\sin(\pi f t^*)}{\pi f t^*} \right] e^{-j\pi f t^*} \tag{4}
\]

The power spectral density (PSD) of \( v_{\text{nc},t2} \), denoted by \( S_{v_{\text{nc},t2}} \), is obtained from

\[
S_{v_{\text{nc},t2}} = \frac{1}{C^2} |W(j2\pi f)|^2 S_{i_{n,t}}, \tag{5}
\]

where \( S_{i_{n,t}} = 4kT g_{m,p} t^* \approx 1 \), and \( g_{m,p} \) is the transconductance of the PMOS transistor. The noise power of \( v_{\text{nc},t2} \) due to the windowed integration of \( i_{n,t} \) over \([0,t^*]\) is obtained using the Wiener-Khinchin theorem

\[
\overline{v_{\text{nc},t2}^2} = \int_{0}^{\infty} S_{v_{\text{nc},t2}}(f) df = \frac{4kT g_{m,p} t^*}{C^2} \int_{0}^{\infty} \left[ \frac{\sin(\pi f t^*)}{\pi f t^*} \right]^2 df. \tag{6}
\]

Making use of \( \int_{0}^{\infty} \frac{\sin^2 x}{x^2} dx = \frac{\pi}{2} \), we obtain from (6):

\[
\overline{v_{\text{nc},t2}^2} = \frac{2kT g_{m,p} t^*}{C^2}. \tag{7}
\]

The total noise power of the voltage of the capacitor is obtained from:

**Figure 19** Dependence of integral nonlinearity (INL) of time interpolator on the slope of the inputs

**Figure 20** Timing error due to the thermal and flicker noise of channel current
Thermal noise-induced timing error at threshold crossing, denoted by \( \Delta t_T \), relates to thermal noise voltage \( v_{nc,t} \) by the slow rate of the voltage of the capacitor at the threshold-crossing [35, 36].

\[
\frac{v_{nc,t}}{\Delta t_T} = \frac{I}{C}.
\]  

(9)

where \( I \) is the channel current. Making use of \( g_{m,p} = \frac{V_{FG}}{2r} \), we obtain the timing error due to the thermal noise of the channel current

\[
\frac{2 \tau_T^*}{\frac{1}{C}} = kTC + \frac{4kT}{I(V_{SG} - |V_{TP}|)}.
\]  

(10)

5.2.2 | Flicker noise-induced timing error

Flicker noise of the channel current also contributes to timing errors. Similar to thermal noise, the PSD of flicker noise-induced capacitor voltage is obtained from

\[
S_{v_{nc,1/f}} = \frac{1}{C^2} |W(jo)|^2 S_{i_{1/f}}
\]  

where \( S_{v_{nc,1/f}} \) is the PSD of the flicker noise of the channel current. Noise current whose frequency is lower than 1/Tobs where Tobs is observation time is indistinguishable from the DC current. The lower frequency bound of the flicker noise \( f_L \) is set to 1/Tobs, which is a few Hertz typically. Following the approach in [37], we assume \( S_{i_{1/f}} = 0 \) in \([0, f_L] \). Since the PSD of flicker noise referred to the gate of the transistor is given by

\[
S_{v_{1/f}} = \frac{K_{fp}}{C_{ox} W L} \frac{1}{f}.
\]  

(12)

where \( K_{fp} \) is a process-dependent constant for PMOS transistors, \( C_{ox} \) is gate capacitance per unit area, \( W \) and \( L \) are the width and length of the transistor, respectively, we have

\[
S_{v_{1/f}} = g_{m,p}^2 S_{i_{1/f}}.
\]  

(13)

The noise power of capacitor voltage due to the windowed integration of \( i_{1/f} \) is obtained from the Wiener–Khinchin theorem

\[
\bar{v}_{v_{1/f}}^2 = \int_{f_L}^{\infty} S_{v_{1/f}}(f) df = \frac{K_{fp} g_{m,p}^2}{C^2 C_{ox} W L} \int_{f_L}^{\infty} \left[ \frac{\sin(\pi f t^*)}{\pi f t^*} \right]^2 df.
\]  

(14)

Similar to timing errors induced by the thermal noise, the power of the flicker noise-induced timing errors is obtained from

\[
\frac{2 \tau_T^*}{\frac{1}{C}} = \frac{\pi f^*}{K_{fp} g_{m,p}^2 C_{ox} W L} \int_{f_L}^{\infty} \frac{d}{f} \left[ \frac{\sin(\pi f t^*)}{\pi f t^*} \right]^2 df.
\]  

(15)

Let \( x = \pi f t^* \). We have \( x_L = \pi f^* t_L \). Equation (15) becomes:

\[
\frac{2 \tau_T^*}{\frac{1}{C}} = \frac{K_{fp} g_{m,p}^2}{C_{ox} W L} \int_{x_{min}}^{x_{max}} \sin^2 x dx
\]  

(16)

where \( x_{min} = \pi f^* t_L \). The integration in (16) can be performed using integration by parts and the result is given by

\[
\int_{x_{min}}^{x_{max}} \sin^2 x dx = \frac{\sin^2(x_L)}{2x_L} + \frac{\sin(2x_L)}{2x_L} - Ci(2x_L),
\]  

(17)

where

\[
Ci(x) = -\int_x^{\cos x} dx = \Gamma + \ln x + \int_0^{x} \frac{\cos x - 1}{x} dx
\]  

(18)

cosine integral and \( \Gamma \approx 0.577 \) is Euler-Mascheroni constant. Since \( f_L \) is small, \( \frac{x_{min}}{x_l} \approx 1 \) follows. As a result,

\[
\int_{x_{min}}^{x_{max}} \sin^2 x dx \approx \frac{3}{2} - Ci(2x_L).
\]  

(19)

Equation (16) is therefore simplified to

\[
\frac{2 \tau_T^*}{\frac{1}{C}} \approx \frac{K_{fp} g_{m,p}^2}{C_{ox} W L} \left[ \frac{3}{2} - Ci(2x_L) \right] \approx \frac{4K_{fp} g_{m,p}^2}{C_{ox} W L (V_{SG} - |V_{TP}|)} \left[ \frac{3}{2} - Ci(2x_L) \right].
\]  

(20)

It is seen from (20) that flicker noise induced timing error is directly proportional to \( \tau_T^* \). Increasing the channel current shortens the charging process, hence lowers both \( \Delta ^2 \tau_T \) and \( \Delta ^2 \tau_{1/f} \). The total timing error due to thermal noise and flicker noise is therefore given by

\[
\Delta \tau = \Delta ^2 \tau_T + \Delta ^2 \tau_{1/f}.
\]  

(21)

To estimate noise-induced timing error, we use the parameters used in [37] for a quick estimation: \( K_{fp} = 3.4 \times 10^{-25} \text{ V}^2/\text{F} \), \( V_T = 0.289 \text{ V} \), \( g_{m,p} = 2.847 \times 10^{-4} \text{ A/V} \), and \( I = 104.8 \mu \text{A} \). PMOS transistor dimensions are \((W/L)_p = 0.96 \mu \text{m}/0.13 \mu \text{m}, C_{ox} = 1.78 \times 10^{-4} \text{ F/m}^2 \). The
duration of the discharging process is $t^* = 500$ ps, and $f_L = 10$ Hz. We have $\sqrt{\Delta^2 \tau_l} \approx 0.21$ ps and $\sqrt{\Delta^2 \tau_{l/f}} \approx 0.44$ ps. Figure 21 (top) plots the rising edge of the output of the static inverter with transient noise included. The impact of thermal and flicker noise of the channel current is a timing error of 0.13 ps approximately. Noise-induced timing error is rather small. Figure 21(bottom) plots the output of $v_{o2}$. It is seen that the timing error of $v_{o2}$ is 0.41 ps whereas that of $v_{o1}$ is 0.13 ps. Timing error accumulation is evident.

5.2.3 Timing error of pre-skewed delay line

The load capacitor of an inverter in a pre-skewed delay line with one pre-skewed inverter is charged by both the pre-skewed inverter and the primary inverter. The duration of the former is longer while that of the latter is shorter, as seen in Figure 2. Let the charging current of the pre-skewed inverter and primary inverter be $I_{pre}$ and $I_{pri}$, respectively. Furthermore, let the charging duration of the pre-skewed inverter and primary inverter be $t_{pre}$ and $t_{pri}$, respectively. The timing error due to the thermal and flicker noise of the pre-skewed and primary inverters is obtained from (10) and (20)

$$\Delta^2 \tau_l = \frac{kTC}{I_{pre}} + \frac{kTC}{I_{pri}} + \frac{4kT \gamma}{V_{SG} - |V_{TP}|} \left( t^*_{pre} + t^*_{pri} \right).$$  \hspace{1cm} (22)

$$\Delta^2 \tau_{l/f} = \frac{4K_f}{C_{ox} W L (V_{SG} - |V_{TP}|)} \left[ \frac{3}{2} - G_i(2x_L) \right].$$  \hspace{1cm} (23)

The timing error of $j$th stage of the pre-skewed delay line, denoted by $\Delta^2 \tau_j$, is obtained by summing up (22) and (23) and taking into account two primary inverters and two pre-skewed inverters per delay stage:

$$\Delta^2 \tau_j = 2 \left[ \Delta^2 \tau_l + \Delta^2 \tau_{l/f} \right].$$  \hspace{1cm} (24)

Since the timing error of each stage of the pre-skewed delay line accumulates, the worst-case timing error of a $N$-stage pre-skewed delay line, denoted by $\Delta^2 \tau_p$, occurring at the output of the last stage of the delay line, is given by:

$$\Delta^2 \tau_p = \sum_{j=1}^{N} \Delta^2 \tau_j.$$  \hspace{1cm} (25)

If $\Delta^2 \tau_j = \Delta^2 \tau$, for $j = 1, 2, \ldots, N$, Equation (25) can be simplified to:

$$\Delta^2 \tau_p = N \Delta^2 \tau.$$  \hspace{1cm} (26)

This result is the same as that given in [36, 38].

5.2.4 Timing error of interpolator

For a $M$-bit digital time interpolation, a total of $2M$ inverters drive the same output node. Since the total number of the inverters that undergo a charging process is $M$, the timing error of the time interpolator, denoted by $\overline{\Delta^2 \tau_i}$, is obtained from

$$\overline{\Delta^2 \tau_i} = \sum_{j=1}^{M} \overline{\Delta^2 \tau_j}. \hspace{1cm} (27)$$

5.2.5 Timing error of digital-to-time converter

The DTC consists of the pre-skewed delay line, the buffers between the pre-skewed delay line and the multiplexer, the multiplexer, the buffers between the multiplexer and the time interpolator, and the time interpolator. Only the timing error of the pre-skewed delay line and that of the time interpolator are important because the timing error of the 4-bit pre-skewed delay line DTC is 32 times that of an inverter and that of the 4-bit time interpolator DTC is 16 times that of an inverter. The timing error of the DTC is therefore obtained from

$$\overline{\Delta^2 \tau_{DTC}} = \overline{\Delta^2 \tau_p} + \overline{\Delta^2 \tau_i}. \hspace{1cm} (28)$$

5.3 Layout considerations

Figure 22 shows the layout of the DTC. No effort was made to minimise the silicon area of the DTC. The primary and pre-skewed inverters of the pre-skewed delay line are placed in two parallel rows so as to simplify routing between them. The buffers between the pre-skewed delay line and multiplexer are placed in parallel with the delay line. The transmission gates of the multiplexer are arranged in such a way that two long horizontal interconnects of equal length are used to route the output of the multiplexer to the buffers placed at the right of the multiplexer. In order to make sure all TGs are matched, interconnects from the buffers between the pre-skewed delay line and the multiplexer are extended over the input nodes of the TGs. The layout of the time interpolator is arranged in such a way with one set of inverters placed in one row and the other set of the inverter placed in another row parallel to the first one.

6 SIMULATION RESULTS

The preceding 8-bit DTC is designed in a TSMC 65 nm 1.0 V CMOS technology and analysed using Spectre with BSIM3V3 device models. The per-stage delay of the pre-skewed delay line with buffers is 58 ps. The longest delay of the pre-skewed delay line occurring when $D_9D_8D_7D_6 = 1111$ is therefore given by $58 \times 16 = 928$ ps, leading to the conversion range of the DTC:
3.6 \text{ ps} \sim 928 \text{ ps}. The delay of the multiplexer with its output buffers included is 587 ps. The longest delay of the time interpolator is 206 ps, occurring when \( D_4 D_3 D_2 D_1 = 1111 \). The worst-case conversion time of the DTC is therefore obtained from: 928 + 587 + 206 = 1721 ps, yielding the minimum conversion rate: \( 1/1721 \text{ ps} = 580 \text{ MS/s} \). Figure 21 plots the DNL and INL of the pre-skewed delay line. The selection word of the pre-skewed delay line is the buffered output of an ideal analogue-to-digital converter (ADC). It is seen that the DNL and INL of the pre-skewed delay line are negligible small, revealing its excellent linearity. Figure 24 plots the DNL and INL measured at the output of the multiplexer. The selection word of the multiplexer is generated in a similar way as that of the pre-skewed delay line. It is seen that the DNL of the multiplexer is rather small. The INL of the multiplexer is less than 0.3 LSB. Figure 25 plots the DNL and INL of the time interpolator whose interpolation word is generated in a similar way as that of the pre-skewed delay line. It is seen that both DNL and INL of the time interpolator are small. To test the DTC, the input of the DTC is generated using a Verilog-A coded ADC with a properly chosen ramping voltage input such that the output of the ADC varies from

**FIGURE 21** Simulated timing error of the charging process of static inverters. Transient noise parameters: \( f_{\text{min}} = 10 \text{ Hz}, f_{\text{max}} = 10 \text{ GHz} \), and 100 runs

**FIGURE 22** Layout of digital-to-time converter. TG, transmission-gate
The generated digital output is buffered before being applied to the DTC. Figure 26 plots the DNL and INL of the DTC (post-layout with R + C extraction). It is seen that the DTC exhibits good DNL and INL. Figure 27 plots the DNL and INL of the DTC (post-layout with R + C + CC extraction) with the inclusion of the impact of coupling capacitors between interconnects and devices. It is seen that the DTC exhibits a good DNL but a deteriorating INL. Further investigation into the cause of the deteriorating INL reveals that when the selection word of the multiplexer changes, there is a consistent slight shift of the threshold-crossing point of the inputs and output of the multiplexer, possibly caused by the asymmetry of the interconnects, the charge injection of the TGs, the consistent voltage shift along the two long interconnects connecting the output of the TGs.
and the input of the output buffers of the TGs, and unequal distance between the output of each TG and the output buffers that are located to the right of the multiplexer. TG-based multiplexer, though convenient in accommodating a large number of inputs, is rather sensitive to the impact of charge injection into the source and drain node of the TGs where the input and output of the multiplexer are connected, respectively. Multiplexers that can accommodate a large number of inputs routed to the gate rather than source/drain of transistors, so as to minimise the effect of charge injection, are being developed.

7 | CONCLUSIONS

An 8-bit delay line DTC with pre-skewing and digital time interpolation was presented. Pre-skewing that lowers the per-stage-delay of delay lines beyond that set by chosen technology was investigated. A cascode tri-state inverter was proposed to improve the isolation between the input and output of interpolation cells so as to improve the linearity of the time interpolator. Design considerations that critically affect the linearity of the DTC were examined in detail. The impact of the slope of the inputs of the time interpolator on the latency and linearity of the interpolator was examined and the maximum slope of the input of interpolators yielding the minimum latency without sacrificing the linearity was obtained. Device noise-induced timing errors of DTC were investigated and the results were compared with simulation results. The post-layout simulation results show the DTC exhibits a good DNL and INL with R + C extraction and INL deteriorates when coupling capacitors are included in the layout extraction. An in-depth investigation of the cause of the deteriorating INL indicates the chosen TG-based multiplexer, though convenient in accommodating a large number of inputs, is sensitive to the impact of the charge injected to the source and drain of the TGs, which are the input and output of the multiplexer, respectively. The proposed DTC consumes only 383 μW power with the maximum conversion rate of 580 MS/s.

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