PWM control method to eliminate Common Mode Voltage in three level T-Type inverters

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Abstract. In this paper, Common-mode voltage (CMV) is responsible for overvoltage stress to the winding insulation and bearing damage of an AC motor. High $dv/dt$ of CMV causes leakage currents, which create noise problems to the equipment installed near the converter. This paper presented modulation strategy to eliminate CMV three level T-Type inverter (Zero CMV 3L T²I) that substantially eliminates CMV. The principles of selecting suitable triangle carrier signals for the T-Type is described. This PWM control method can mitigate the peak value to 95% as compared to the conventional sinusoidal pulse width modulation method. A prototype is constructed to verify the operating principle of the three-level T-Type inverter. Simulation and experimental results are presented.

1. Introduction
Common-mode voltage (CMV) widely exists in typical power inverters. It will stimulate the distributed and parasitic capacitances in the system and thus results in common-mode current. In inverter-driven induction motor systems, the common-mode current will produce shaft voltages and bearing currents [1]. The overload bearing current would speed up the aging of the motor bearing and shorten the service life of the motor [2]-[3]. Additionally, the CMV can also cause electromagnetic interference (EMI) [4]. Therefore, it is necessary to reduce or eliminate the CMV in inverters.

CMV attributed to high-speed pulse-width modulation (PWM) in power converters introduces numerous problems within an electrical system. CMV is the main source of early motor-winding failure, bearing deterioration, and wide-band electromagnetic interference. Eliminating the CMV within the power converter is important. Two main solutions used to eliminate CMV have been presented in previous research. One solution is based on the use of additional hardware or software approaches. Using of additional hardware, such as passive filters, active cancellers, or electromagnetic interference filters, to mitigate CMV [5] and installing additional passive or active devices[6]. The software one is realized by developing proper modulation strategies with reduced CMV [7]. Generally, the latter is preferable as it will not increase the cost, weight and size of the inverters. In partial PWM methods to eliminate common mode voltage, the output voltage can be obtained normally by a conventional Discontinuous PWM technique (DPWM) [8]. In order to attain reduced common mode voltage at a high modulation index, a new DPWM pattern from three non-nearest vectors was proposed [9].
The PWM control method is simple to implement and does not require any additional hardware. The advantages of the proposed method are as follows: eliminates the peak value of the CMV, and the magnitude is reduced by 95% compared with that when using the conventional PWM scheme.

2. Three level T-Type Inverters topology

The operating principles of the Zero CMV 3L T²I can be explained with the help of the switching states in Table 1. The inverter can produce three different voltage levels: \(+V_c/2\), 0, and \(-V_c/2\), by controlling the switches in the T-type bridge circuit. The positive output voltage can be achieved by triggering \(S_{1x}\) and \(S_{2x}\) (x = a, b, or c). When the switches \(S_{1x}\) and \(S_{2x}\) are turned on, the output phase voltage \(V_{xO}\) is \(+V_c/2\). When \(S_{2x}\) and \(S_{3x}\) are turned on, the neutral point (node O in Figure 1) is connected to the load. As a result, the output phase voltage \(V_{xO}\) is zero. The negative output voltage can be obtained by triggering \(S_{3x}\) and \(S_{4x}\). When the switches \(S_{3x}\) and \(S_{4x}\) is turned on, the output phase voltage \(V_{xO}\) is \(-V_c/2\).

![Three level T-type inverter](image)

**Figure 1.** Three level T-type inverter.

Table 1. Switching states of T-type inverter

| Device switching status | Output voltage |
|-------------------------|----------------|
| \(S_{1x}\) \(S_{2x}\) \(S_{2x}\) \(S_{3x}\) | \(V_x\) |
| 1 1 0 0 | \(+V_c/2\) |
| 0 1 1 0 | 0 |
| 0 0 1 1 | \(-V_c/2\) |

![Conventional three level T-type inverter control method](image)

**Figure 2.** Conventional three level T-type inverter control method.
3. CMV analysis for three level T-type inverter

3.1. CMV analysis for three level T-Type inverter

The 3-level T-type inverter have the same 3-branch structure. Each branch consists of 4 semiconductors with 1 bi-directional switch. Its configuration is represented in Figure 1.

The phase to neutral point voltage is determined using the switching state:

\[
U_{NG} = V_{2N} - V_{NG} = \begin{cases} 
0 & \text{if } S_{1x} = S_{2x} = 0 \text{ and } S_{3x} = 1 \\
\frac{V_e}{2} & \text{if } S_{1x} = S_{3x} = 0 \text{ and } S_{2x} = 1 \\
V_e & \text{if } S_{2x} = S_{3x} = 0 \text{ and } S_{1x} = 1,
\end{cases}
\]

(1)

Where \( E = \frac{V_e}{2} \) and \( T_x = S_{1x} + 2S_{3x} \) and equation (1) is rewritten:

\[
U_{NG} = ET_x
\]

(2)

From (2) we can be written the phase to neutral point voltage as:

\[
\begin{bmatrix}
U_{AG} \\
U_{BG} \\
U_{CG}
\end{bmatrix} = \begin{bmatrix}
T_a \\
T_b \\
T_c
\end{bmatrix}
\]

(3)

Output phase voltage is determined by (4) and (5).

\[
\begin{bmatrix}
V_{AN} \\
V_{RN} \\
V_{CN}
\end{bmatrix} = \begin{bmatrix} 1 & 2 & -1 & -1 \\ 0 & -1 & 2 & -1 \\ -1 & -1 & 2 & -1 \end{bmatrix} \begin{bmatrix}
U_{AG} \\
U_{BG} \\
U_{CG}
\end{bmatrix}
\]

(4)

\[
\begin{bmatrix}
V_{AN} \\
V_{RN} \\
V_{CN}
\end{bmatrix} = \begin{bmatrix} 1 & 2 & -1 & -1 \\ 0 & -1 & 2 & -1 \\ -1 & -1 & 2 & -1 \end{bmatrix} \begin{bmatrix}
T_a \\
T_b \\
T_c
\end{bmatrix}
\]

(5)

Replace (1) into (4) and note due to load balancing:

\[
V_{AN} + V_{RN} + V_{CN} = 0
\]

(6)

\[
V_{NG} = \frac{T_a + T_b + T_c}{3} E
\]

(7)

The circuit topology of 3L T-Type inverter (3L T²I) is shown in Fig. 1. Its CMV is defined as the voltage between load neutral point “N” and the mid-point of DC power supply “O”, which can be described as follows:

\[
V_{ON} = V_{OG} - V_{NG} = E - \frac{T_a + T_b + T_c}{3} E
\]

(8)

Where \( T_A, T_B, T_C \) is the state on the branches.

The CMV value is listed in Table 2.

| State | Ta | Tb | Tc | CMV |
|-------|----|----|----|-----|
| 1     | 0  | 0  | 0  | E   |
| 2     | 0  | 0  | 1  | 2E/3|
| 3     | 0  | 0  | 2  | E/3 |
| 4     | 0  | 1  | 0  | 2 E/3|
| 5     | 0  | 1  | 1  | E/3 |
From equation (8) to eliminate CMV ($V_{ON}=0$), and the state on the branches is defined:

\[ T_1 + T_2 + T_3 = 3 \] (9)

So, to eliminate common mode, the vector status of the phases can be selected one of six vector status $[0, 1, 2], [0, 2, 1], [1, 0, 2], [1, 2, 0], [2, 0, 1], \text{ and } [2, 1, 0]$. 

3.2. Proposed PWM control method

The modulation waves $V_a, V_b, V_c$ can be expressed as:

\[
\begin{align*}
V_a &= m \sin \theta + 1 \\
V_b &= m \sin \left( \theta - \frac{2\pi}{3} \right) + 1 \\
V_c &= m \sin \left( \theta - \frac{4\pi}{3} \right) + 1,
\end{align*}
\] (10)

Where $\theta$ and $m$ are phase angle and modulation index and $0 \leq m \leq 1$. So, reference voltage is determined:

\[ 0 \leq V_x \leq 2 \] (11)

Set $L_x$ and $H_x$:

\[
L_x = \begin{cases} 
\text{int}(V_x) & \text{if } V_x < 2 \\
\text{int}(V_x) - 1 & \text{if } V_x = 2, 
\end{cases}
\] (12)

\[
H_x = 1 + L_x
\] (13)

From equation (12) and (13) can be see that, one cycle of carrier is $T_x$ can be changed $L_x$ or $H_x$ depend on $V_x$, $CR_1$, and $CR_2$ value.
When $\xi = V_x - L_x$ and is the decimal component of $V_x$:

$$0 \leq \xi \leq 1$$

From equation (10) $V_A + V_B + V_C = 3 \Rightarrow L_A + L_B + L_C + \xi_A + \xi_B + \xi_C = 3$

$L_A, L_B, L_C$ are integers due to $\xi_A + \xi_B + \xi_C$ must be integers Let's sum them as integers (=3).

$$\xi_A + \xi_B + \xi_C = \begin{cases} 1 & \text{when } L_A + L_B + L_C = 1 \\ 2 & \text{when } L_A + L_B + L_C = 3 \end{cases}$$

To eliminate common mode voltage, the algorithm is divided into 2 cases that are $\zeta_A + \zeta_B + \zeta_C = 1$ and $\zeta_A + \zeta_B + \zeta_C = 2$.

**Case 1:** $\zeta_A + \zeta_B + \zeta_C = 1$

![Figure 3](image_url)

**Figure 3.** Case 1 algorithm to eliminate CMV.

$\zeta_A + \zeta_B + \zeta_C$ can be selected randomly in the three level T-Type inverter, but are further restricted in the three level T-Type inverter due to the limit of its switching combinations.

The constraint is simply expressed as:

$$\xi_A \leq \xi_B \leq \xi_C$$

At any time of figure 3 $T_A + T_B + T_C = 3$. Due to, the common mode voltage $V_{0N}=0$. The same remain time interval, respectively.

Fig. 3(a) presented PWM control method when not to eliminate common mode voltage. The CMV remain in time intervals $T_1, T_3,$ and $T_4$.

Fig. 3(b) presented PWM control method when CVM is eliminated.

**Case 2:** $\zeta_A + \zeta_B + \zeta_C = 2$

At any time of figure 4 $T_A + T_B + T_C = 3$. Due to, the common mode voltage $V_{0N}=0$. The same remain time interval, respectively.

Fig. 4(a) presented PWM control method when not to eliminate common mode. The CMV remain in time intervals $T_1, T_3,$ and $T_4$.

Fig. 4(b) presented PWM control method when CVM is eliminated.
Figure 4. Case 2 algorithm to eliminate CMV.

V_i(X=A,B,C)

L_i(X=A,B,C)

Ɛ_i(X=A,B,C)

Ɛ_i+Ɛ_i+Ɛ_i=1

Select Case 1

Select Case 2

T_i(X=A,B,C)

Pulse Generator

Figure 5. Flowchart of the eliminate CMV method.

This flowchart describes how to eliminate CMV in 3 level T-type inverter. The first, we calculate the Lx and Ɛ_X follow equation (5). Then, this method is divided into two case described in figures 3 and 4. As a result, the output of this operating is T_A, T_B and T_C which eliminating the CMV. We can control the switches state using this T_X following equation (3).
4. Simulation and experimental results

4.1. Simulation results
To verify the Zero CMV 3L T^2I performance, extensive simulation studies of those inverters are performed in PSIM. The circuit parameters have been taken for simulation and experiment are shown in Table 3.

Table 3. Parameter used in experiment

| Parameter/component | Attributes |
|---------------------|------------|
| Input voltage (Vdc) | 200 Volts |
| Modulating signal frequency (f) | 50 Hz |
| Output Power | 100W |
| Output frequency | 50 Hz |
| Carrier frequency (fs) | 5KHz |
| Modulation index M | 0.86 |
| Capacitor (C1) | 4400 µF |
| Capacitor (C2) | 4400 µF |
| Three-phase LC filter L, C | 10 mH |
| Load Resistor R_load | 40Ω |

Fig. 6 shows the simulation results for Zero CMV 3L T^2I when Vdc=200V, output power= 100 W, Output frequency = 50 Hz, Capacitor (C1)= 4400 µF, Capacitor (C2)= 4400 µF, Carrier frequency (fs)=5kHz, Modulating signal frequency (fm)=50Hz, Load: resistance R=40Ω, inductance Lf=10mH per phase, capacitor cf=10 µF. Modulation ratio M=0.86.

![Simulation results](image)

Figure 6. Simulation results for Zero CMV 3L T^2I when Vdc = 200 V and M= 0.86. (a) output phase voltage V_{AN}, (b) output line to line voltage V_{AB}, (c) load current I_A, and (d) common mode voltages. Fig. 6 shows the simulation results of the Zero CMV 3L T^2I with the PWM control method when Vdc = 200 V and M = 0.86. As shown in Fig. 6, the output phase voltage (V_{AN}) has three levels: 100 V, 0 V
and -100 V. The output line to line voltage \( V_{ANB} \) has five levels: 200V, 100 V, 0 V and -100 V, -200V. The common mode voltage is found 0V.

4.2. Experimental results

A prototype is built to test the Zero CMV 3L T²I and its PWM control. The design parameters and the list of semiconductor components used for the prototype are given in Table 3, respectively. A 100-W prototype was built in the laboratory to verify the effectiveness of the proposed PWM scheme. The input voltage is in 200 V. The output frequency is 50 Hz. The switching frequency of the T-type inverter circuit is 5 kHz. All FGL40N150D IGBTs in the prototype are controlled by TLP250 amplifiers. The two capacitors \( C_1 \) and \( C_2 \) are 4400 \( \mu \)F/400 V. The output voltage is filtered by a three-phase low-pass filter.

![Figure 7](image)

**Figure 7.** Experimental results for Zero CMV 3L T²I when Vdc = 200 V and M = 0.86. (a) output phase voltage \( V_{AN} \), (b) output line to line voltage \( V_{AB} \), (c) load current \( I_A \), and (d) common mode voltages.

Fig. 7 shows the simulation results of the Zero CMV 3L T²I with the PWM control method when Vdc = 200 V and M = 0.86. As shown in Fig. 7, the output phase voltage \( V_{AN} \) has three levels: 100 V, 0 V and -100 V. The output line to line voltage \( V_{ANB} \) has five levels: 200V, 100 V, 0 V and -100 V, -200V. The common mode voltage is found 5 Vrms.

Figs. 6(d) and 7(b) show CMV of the simulation and experimental results. This simulation result is possible to confirm that the obtained value is similar with the experimental results, although slightly higher, which was expected.

5. Conclusion

A PWM control method is presented in this study to eliminate CMV for three-level T-type inverter. The peak value of the CMV, and the magnitude is reduced by 95% compared with that when using the conventional PWM scheme. PWM control method is simple to implement and does not require any
additional hardware. Circuit analysis, operating principles, and simulation results and experimental for the Zero CMV 3L T^2 with the PWM control method are presented.

6. References

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