Removal of GaAs growth substrates from II–VI semiconductor heterostructures

S Bieker, P R Hartmann, T Kießling, M Rüth, C Schumacher, C Gould, W Ossau and L W Molenkamp

Physikalisches Institut (EP3) der Universität Würzburg, 97074 Würzburg, Germany
E-mail: tobias.kiessling@physik.uni-wuerzburg.de

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Abstract
We report on a process that enables the removal of II–VI semiconductor epilayers from their GaAs growth substrate and their subsequent transfer to arbitrary host environments. The technique combines mechanical lapping and layer selective chemical wet etching and is generally applicable to any II–VI layer stack. We demonstrate the non-invasiveness of the method by transferring an all-II–VI magnetic resonant tunneling diode. High resolution x-ray diffraction proves that the crystal integrity of the heterostructure is preserved. Transport characterization confirms that the functionality of the device is maintained and even improved, which is ascribed to completely elastic strain relaxation of the tunnel barrier layer.

Keywords: spintronics, lift-off techniques, nanostructures

1. Introduction

Epitaxial growth techniques are a key technology for the fabrication of modern integrated electronics. A fundamental requirement for the growth of high crystalline quality epilayers is a proper match of the lattice constants of the grown heterostructures and the supporting substrate. This restriction often limits the choice of substrate materials, which in turn may prohibit the commercial applicability of certain device architectures or reduce performance. Epitaxial lift-off (ELO) techniques as proposed by Yablonovitch et al [1] add a new degree of flexibility by enabling the removal of the resulting heterostructures from their growth substrate. ELO further allows for the transfer to new host environments, which may even enhance functionality. Several application ideas for ELO processes have been put forward, ranging from improved thermal management [2] to cost-effective GaAs based photovoltaics and optoelectronics [3].

The most widely used ELO technique relies on a sacrificial layer of Al$_x$Ga$_{1-x}$As that is grown between the GaAs substrate and the intended GaAs-based heterostructure. This technique exploits the large difference in etch rates between GaAs and Al$_x$Ga$_{1-x}$As in hydrofluoric acid (HF) [1]. Similar techniques have been developed for more specialized purposes, including laser lift-off for group III-nitride films [2, 4]. Only recently progress has been made in the development of lift-off procedures for ZnSe-based heterostructures employing MgS [5, 6] and ZnMgSSe release layers [7].

In this paper we demonstrate an ELO process that combines mechanical lapping and layer selective chemical wet etching. In contrast to previous work, this does not require a sacrificial release layer. The technique thereby simplifies the growth and is also applicable to heterostructures that were not meant to undergo lift-off when designed. A main achievement is the strongly reduced contact time with wet chemical agents, which minimizes negative effects on material quality in sensitive heterostructures. Our process is demonstrated for an all-II–VI compound semiconductor resonant tunneling diode (RTD), but is portable to other material systems. Current–voltage characteristics and x-ray diffraction are studied to assess the impact of the procedure on the structural integrity of the crystal. RTDs are used for this purpose as they are known to be highly sensitive to small changes in the material quality of the heterostructure.

2. The lift-off technique

The test structure RTDs are grown by molecular beam epitaxy (MBE) on (001)-oriented GaAs substrates. Its layer stack is shown in figure 1 and a thorough discussion of the device and
its layer properties can be found in [8]. The total thickness of the active device region, including its II–VI multilayer buffer, is roughly 1 μm. We use a two-step process to detach the all-II–VI heterostructure from the GaAs substrate. In the first step, 320 μm of GaAs are removed through mechanical lapping. A selective wet chemical etchant thereafter removes the remaining 30 μm of substrate material.

The key ingredient of the method is the sample preparation prior to the lapping step. II–VI compound epilayers are mechanically softer than the GaAs substrate. Strong shear forces acting on the II–VI layers will therefore ruin the structural integrity and destroy the device. To decouple shear forces from the sensitive II–VI layers during the lapping process we developed a method that provides for a rigid silicon frame to protect the active device layers. This silicon frame is fabricated from a 10 × 10 mm² piece of silicon covered with a 200 nm SiO₂ layer. Standard optical lithography is used to pattern a square window of 5 × 5 mm². Within this window, the SiO₂ cap is removed by a buffered oxide etch of 7:1 NH₄F to HF. The remaining SiO₂ is then used as an etch mask in the last step, in which the entire silicon layer is etched into KOH (20%) at 80 °C. Here the exposed silicon layer is etched from both sides. This produces a silicon frame of roughly half the thickness of the original layer with a 5 × 5 mm² opening.

Figure 2 illustrates the subsequent steps of the process. We start out from pre-patterned RTD pillars as described in [8]. These stacks are not etched down completely to the GaAs substrate but are terminated in the n⁺-doped II–VI-layer on which the ex situ metallic contact pads reside. In the first step we define the sample areas to be detached and cover these with an organic photo resist. The size of the defined area is limited only by the dimensions of the silicon frame. On the remaining sample area we remove the metal layers. For this step we prepare a 1:1:1 mixture of thiourea, sodium sulfate and potassium ferricyanide (each in a 10% aqueous solution). The sample is then alternately dipped into the above etchant and a 1:200 aqueous solution of HF (50%) until the metal is completely gone. The uncovered II–VI layers are wet chemically etched down to the GaAs substrate by a solution of 1:99 bromine in ethylene glycol (see figure 2(a)). The end of this etching step is reached as soon as the characteristic etalon fringes that stem from the II–VI layers disappear, leaving a free standing mesa of to-be-detached II–VI material on bare GaAs. These mesa are then placed inside the silicon frame, which is glued onto the GaAs using Apiezon wax. Finally, the silicon frame is attached to the rigid glass carrier of the polishing machine. This configuration leaves the sensitive RTD pillars inside the resulting cavity and no shear forces act on them during the subsequent mechanical lapping step (figure 2(b)).

During the MBE growth process the host substrate is often glued to the molybdenum substrate holders with indium adhesive to provide good thermal contact. Any such indium residues must be removed from the backside of the substrate as they would reduce the abrasive efficiency of the lapping step. This is done by immersion in HCl (37%). After this sample preparation, the glass carrier is attached to the underpressure jigface of the polishing machine. We
use a commercial precision lapping and polishing machine (Logitech PM4) equipped with a rotating polishing disk that is continuously fed with calcined aluminum oxide powder (9 μm abrasive grain size) dissolved in distilled water. A micrometer gauge on the jig allows for control of the remaining sample thickness. As the first step of thinning, 320 μm of the GaAs substrate are removed through mechanical lapping.

The thinned sample is then detached from the silicon frame by immersing the glass carrier in trichloroethylene at 60 °C. The sample is cautiously removed from the solvent and glued topside down onto a clean glass plate. To selectively remove the residual GaAs substrate we use an 84:16 mixture of NaOH (5%) and H2O2 (31%). Complete removal of the GaAs material is easily recognized by the appearance of the yellow II–VI layers underneath. We observe etch rates of 15–20 μm h⁻¹ for this final etch step. Immersing the glass carrier again in trichloroethylene at 60 °C detaches the II–VI layer stack from the carrier. The free floating lifted layer is finally picked up using the new host substrate of choice. If necessary, residual wax from previous process steps is removed with acetone, isopropyl and distilled water. After drying the sample film bonds to the new host substrate by van der Waals forces [1, 9] without the need for additional adhesive.

Figure 3(a) displays a photograph of a lifted layer that is overlapping with the edge of the wafer that was used to capture it from the solvent. The robust overhang of the thin film is a strong indication that the crystalline integrity of the heterostructure is preserved during the process.

The thinned II–VI heterostructures do not withstand the stress from standard wire bonding. For wiring the device we therefore apply small droplets of a two component electrically conductive epoxy to the contact pads of the pillars. Figure 3(b) shows a single RTD pillar from such a lifted layer, with gold wires attached to the top and backside contacts via conductive epoxy droplets.

3. Sample characterization after lift-off

We use high-resolution x-ray diffraction (HR-XRD) and current–voltage characterization to assess the impact of the lift-off process [10]. Figure 4 shows a direct comparison of ω–2θ scans for the same RTD sample before and after removal of the substrate. The sharp feature of the as-grown sample at Δθ = 0° is the (0 0 4) reflection of the GaAs substrate. With the substrate removed, only the underlying reflection from the 200 nm layer of the lattice matched Zn0.97Be0.03Se remains. Due to its slightly larger lattice constant, the ZnSe (004) reflection is shifted to −0.45°. The distinctive diffraction pattern centered at 1.2° stems from the II–VI multilayer buffer. The noticeable beating in the region from 2 to 4° results from x-ray interference between the symmetric Zn0.79Be0.21Se tunnel barriers. The ω-scans of the ZnSe and Zn0.97Be0.03Se reflections reveal increased full width at half maximum values of 433° and 550° compared to typical values of 20° on the as-grown structures (not shown). The ω-width is a measure of the degree of tilt variation of the lattice planes that contribute to a given x-ray reflex. Both the multilayer buffer features and

Figure 3. (a) Sample film after removal of the GaAs as described in the text. The apparent stiffness of the lifted film indicates that the crystal integrity of the heterostructure is preserved. (b) One of the pre-patterned transport pillars is contacted with droplets of an electrically conductive epoxy after removal of the growth substrate.

Figure 4. ω − 2θ HR-XRD scans of lifted and as-grown II–VI RTD structures. All distinct features are reproduced after removal of the substrate, demonstrating that our lift-off routine preserves the structural integrity of the crystal. Inset: ω-scans of the Zn0.97Be0.03Se (004) peak after substrate removal revealing a geometric broadening compared with the as-grown structures.
Figure 5. I–V characteristics of a dilute magnetic QW RTD, before and after removal of the GaAs substrate, at $B = 0$ T and $B = 6$ T.

Figure 5. I–V characteristics of a dilute magnetic QW RTD, before and after removal of the GaAs substrate, at $B = 0$ T and $B = 6$ T.

the double barrier beating are, however, retained in the lifted layer. We therefore conclude that structural integrity of the crystal is preserved after lift-off, but that the layer does not rest perfectly flat on the new substrate.

We chose RTDs as test devices for our substrate removal process because their I–V characteristics are very sensitive to the crystal quality of the heterostructure as well as to the smoothness of the interfaces. Figure 5(a) shows the I–V characteristics at $B = 0$ T for the as-grown sample. A second sample of the same pillar size and processed from the same heterostructure is characterized after removal of the GaAs substrate, with results shown in figure 5(b). Both samples are measured using the same measurement setup, and with a load resistor of $R = 6 \Omega$. For the zero field curve of this second sample, the negative differential resistance (NDR) part of the I–V characteristic cannot be resolved, as indicated by the dashed arrow indicating a jump in the bias voltage. This results from a current bistability resulting from the load line of the RTD [11]. Given that the overall resistance of both devices is very similar, the load line analysis of the circuits are equivalent, and the apparent bistability can only be attributed to a sharpening of the peak and the corresponding increase in NDR after the resonance.

The I–V characteristics (black circles) are fitted using the model discussed in [12]. The blue and red lines depict the contributions to the total current (purple line) of the spin-up and spin-down channels, respectively. The fits to the I–V characteristics indicate the presence of a zero field splitting. In [12] it is argued that this splitting, as well as the broadening of the zero field peak, result from quantum well (QW) interface roughness. This causes the QW device to break down into an ensemble of parallel tunneling structures, each with a small area, and acting as a bound magnetic polaron (BMP) state. Since in each of these areas, the well properties differ slightly, this explains the broadening of the resonance, while the statistics describing the magnetization of bound magnetic polarons accounts for a remanent zero field splitting, similar to that observed for dilute magnetic CdSe quantum dot systems [13].

The fits to the curves of figure 5 give a peak broadening $\Gamma_0 = 8.9$ meV for the as-grown sample and one of $\Gamma_p = 8.2$ meV for the lifted sample. This reduction in width can again be understood from the model of [12]. We suggest that the removal of the substrate relaxes the strain imposed on the II–VI layers by the imperfect lattice match to the substrate, and resolves the strain-induced imperfections at the interfaces as is schematically shown in figure 6. The increased uniformity in QW thickness results in a sharpening of the resonance. This flattening of the interfaces also reduces the topographical interface features which sustain the formation of the BMP like states, and leads to a reduction of the zero field splitting, as is evident by comparing figures 5(a) and (b).

4. Summary and conclusions

In summary, we have demonstrated a combined mechanical and chemical process that allows for the removal of GaAs growth substrates from II–VI heterostructures without the
Figure 6. (a) Roughness of the QW interfaces allows for the formation of 0D type states which account for the remanent zero field splitting and the well width fluctuations that account for the broadening of the $I-V$ resonance peak [12]. (b) Removal of the GaAs substrate relaxes the strain imposed on the heterostructure, thus smoothening the interfaces and resolving the 0D type states.

necessity of any sacrificial release layers. We have shown that the crystal integrity of even a fragile heterostructure is preserved during the substrate removal process, which is achieved by application of a silicon protection frame. Relaxation of strain previously induced by the lattice mismatch to the substrate even results in an increase in layer quality of the tested II–VI resonant tunneling diodes. The presented method can be ported well to a wide range of other material systems.

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