Development of the Line Protection Measurement and Control Device based on Domestic MCU

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Abstract—In this paper, the dual MCU hardware architecture of protection measurement and control device was presented by analyzing the current situation of domestic MCU and chip selection. The problems existing in ADC sampling accuracy and ADC integral non-linearity were studied. The design scheme of high-precision ADC acquisition system based on dual MCU architecture was proposed, which could meet the requirements of technical specifications by using oversampling and adaptive processing of sampling non-linear area. In terms of reliability, the EMC performance of the device was promoted by the improvement of outlet and ADC acquisition circuit.

1. Introduction

The shortage of global semiconductor industries and the weakness of supply chain problems are concerned. With the development of domestic chip industry, the domestic chip technology in the field of relay protection is gradually improved<sup>[1]</sup>. The development of the low-voltage protection and control device based on domestic chip is restricted by existing production and manufacturing process of domestic chips. The main control chip is selected from other industrial sectors<sup>[2]</sup>. Based on the technical performance of existing domestic chip, through the optimized design of existing relay protection algorithm, function, and hardware and software architecture, overcoming the insufficient of peripherals, main control ADC chip accuracy, domestic component reliability, etc.<sup>[3]</sup> to achieve the design goal which is the domestic chip protection performance is not less than existing relay protection performance. Based on the current status of domestic main control chip without memory ECC (Error Checking and Correction or Error Correction Coding) verification mechanism<sup>[4][5]</sup>, it is necessary to study mistake proofing under existing architecture. In the meanwhile, working on the perfection of self-check logic, improve the robustness of hardware architecture and reliability of software program, in order to avoid the incorrect action of protection.

This paper analyzes the current status of MCU technology, and proposes the hardware and software design scheme and performance improvement measurement of the line protection and control device. The influence of the non-linear error precision of the ADC was overcome, and proposes the improvement measurement of electromagnetic compatibility for domestic chip components. The development of domestic low-voltage line protection and control device has great practical significance.
of the autonomous control of the production and manufacturing of the power system secondary protection control equipment.

2. Domestic MCU Technology Status

At this stage, domestic MCU cannot be compared with foreign brands in the market share or technical advancement. 8 MCU still occupied the mainstream market, accounting for about 50%, and 16/32-bit MCU accounts for about 20%. The applications of domestic MCU are concentrated in low-end electronic products. Compared the three domestic 32-bit general MCU chip parameters, Zhaoyi innovative GD32F450ZI is excellent in performance, storage capacity, ADC external channel, peripheral interface, etc., which could be used for low-voltage line protection and control device.

| Manufacture         | Zhaoyi Innovation | Zhixin microelectronic | Yatley Technology |
|---------------------|-------------------|------------------------|-------------------|
| Type                | GD32F450ZI        | SCM610                 | AT32F413RBT7      |
| Kernel              | CORTEX-M4         | CORTEX-M4              | CORTEX-M4         |
| Basic frequency     | 200M              | 150M                   | 200M              |
| FLASH               | 2048KB            | 1024KB                 | 256K              |
| SRAM                | 512KB             | 256KB                  | 64K               |
| ADC                 | 12bit 24 external channel | 12bit 4 external channel | 12bit 2 external channel |
| GPIO                | 114               | 100                    | 55                |
| UART                | 8                 | 8                      | 5                 |
| Ethernet            | 1                 | 2                      | 1                 |
| CAN2.0B             | 2                 | 0                      | 2                 |

The GD32F450ZI MCU of Zhaoyi Innovation is a 32-bit universal micro-controller based on the ARM® CortexTM-M4 processor with low interruption delay time, low cost debugging features. High integration and enhanced features make the controller suitable for high performance and low power applications. The controller supports powerful and scalable instruction sets, including universal data processing I/O control tasks, enhanced data processing bit domain operations, DSP (digital signal processing), and floating point arithmetic instructions. Software is running in built-in SRAM, FLASH, which has the advantages of low power and excellent electromagnetic compatibility performance.

3. The Design of Line Protection and Control Device

3.1. Hardware architecture

Reliability is the basic requirement of the relay protection device. Factors affecting the reliability of the device hardware system are mainly included: the quality of the components, the manufacturing process level, the rationality of the circuit design, the integration of components [6]. Circuit design still occupies an extremely important location in the design of the hardware system. In order to achieve high reliability, the hardware design based on domestic MCU uses a single board with dual MCU redundant, and two systems work parallel [7].

For analog sampling link, the sampling data for start MCU and protect MCU are used for logic data calculation of protect start and action respectively. Dual ADC uses mutual independent analog sampling loops and analog domain power supplies to maximize guarantee the independence of dual ADC and reduce the interference between dual ADC. For logical judgment link, start MCU and protect MCU program run in independent memory respectively, logic judgment duplication, which is overcoming domestic master chips does not have ECC check function and avoiding the protection mis-operation or rejection caused by memory errors [8]. For export execution link, start MCU control outlet relay power supply, protect MCU control relay outlet, and serial export control improves the reliability of the device.
The interface management functions such as LCD interaction, keyboard and indicator control were deployed in protect MCU. The start MCU and protection MCU collect the external DI simultaneously, and complete the protective value synchronization of two MCU through inside communication. IIC bus is equipped with RTC chip clock input, temperature monitoring, 3-way 485/232 communication multiplexing with print function. Completing the time synchronization function of B code and PPS pulse for start and protection MCU by GPIO communication [9].

3.2. Oversampling design
The analog sampling accuracy is the core indicator of the relay protection device. The ADC module which was discussed in this paper is integrated in the MCU chip. The analog-digital converter which is using successive approximation method, with a theoretical sampling resolution is 12 bits, and its acquisition voltage range is 0~3V. The SNR (signal-to-noise ratio) of the ADC in domestic MCU is 66dB, and the actual effective bit is 10.7 bits. According to the effective bits of the AD and the resistance parameter of the acquisition loop, the accuracy of the analog sampling which is contained the detection of the protection current, protective voltage, and measuring current could be calculated [10]. As shown in Table 2, the resolution of the protective current and measuring current is 1LSB0.184A and 1LSB0.0184A, respectively, which does not satisfy the accuracy requirements of protection current which is ± 2.5% or ± 0.01In, and the measured current which is ± 0.2%.

Over-sampling techniques can not only improve the chip sampling resolution, but also can reduce the effect of sampling noise[11]. According to the derived result of the oversampling rate, the relationship between the quantized SNR and the oversampling rate M may satisfy the following formula. The higher the oversampling rate M, the higher the SNR.

\[
SNR_{oversample}(dB)=6.02 + 1.76 + 10\log(M)
\]

The relationship between the ADC sampling digital encoding (ENOB) and the quantized signal-to-noise ratio (SNR) satisfies the following formula.

\[
ENOB = \frac{SNR - 1.76}{6.02}
\]

As can be seen from the formula, when the sampling frequency is doubled, the in-band noise will decrease 3dB, and the measured resolution will increase by 1/2 bits. Therefore, sampling at 4 times the sampling frequency to increase the resolution by 1 bit. M = 64, SNR increases 18 dB, ENOB adds 3 digits[12]. As the number of samples increases, the number of data valid bits also increases the calculation load of the CPU, which is not conducive to the overall performance of the device. According to Table 2 test data analysis, when the oversampling set to 64 times, it is possible to meet the accuracy requirements and ensure the small CPU load. Therefore, this paper is set in accordance with 64 times.
| Analog Channel                  | Applied Value (V/A) | Displayed Value (V/A) | Accuracy (%) |
|--------------------------------|---------------------|-----------------------|--------------|
| Phase A protection voltage     | 57.740              | 57.767                | 0.047%       |
| Phase B protection voltage     | 57.740              | 57.714                | -0.045%      |
| Phase C protection voltage     | 57.740              | 58.333                | 0.161%       |
| Phase A protection current     | 1.0                 | 1.006                 | 0.600%       |
| Phase B protection current     | 1.0                 | 1.007                 | 0.700%       |
| Phase C protection current     | 1.0                 | 1.007                 | 0.700%       |
| Phase A measurement current    | 1.0                 | 1.000                 | -0.100%      |
| Phase B measurement current    | 1.0                 | 0.999                 | -0.100%      |
| Phase C measurement current    | 1.0                 | 0.998                 | -0.200%      |

3.3. Software Architecture

Based on the principle of functional hierarchical design of platform module and flexible deployment of service function, the device software architecture design is divided into task scheduling modules, interrupt modules, multiple real-time service task modules, and hardware drive modules.

The real-time multi-task scheduling module is the core of the entire software system, all interrupts and tasks are reasonably ordered under the policy control of the scheduling module [13]. Interrupt mainly includes sampling timer interrupts, timing scheduling interrupts, frequency capture interrupts, and keyboard interrupts. Real-time service tasks include: system main task, AD sampling computing tasks, frequency computing tasks, protect analog computing tasks, DI acquisition tasks, protect logic discriminating tasks, key value processing tasks, and display tasks. Each task has a different priority, and the task is communicated and synchronized by the message and mail [14]. The hardware drive layer completes the communication and data interaction between the MCU and the underlying hardware, including the ADC conversion, and DI acquisition, buttons and LCD, LED, time synchronization, Ethernet communication and other hardware communication interfaces [15].

![Fig.2 The software system framework diagram of protection measurement and control device based on domestic MCU](image)

The MCU chip integrates only one Ethernet network port communication interface, and the dual ethernet communication function of the device is completed by two MCUs. Double MCU is used by dual SPI channel to communication [16], the protect MCU is used as the SPI communication host and the start MCU is used as the SPI communication slave, and the dual ethernet communication function is
implemented by virtual network card technology. The data of station control layer A received by protection MCU is analysed and processed by the communication module of protection MCU. The data of station control layer B received by start MCU is sending to the virtual network by SPI communication bus for analysing and processing.

![Fig.3 Dual Ethernet communication function](image)

4. Overcoming an impact of integral nonlinear error of ADC

In the ADC static precision indicator, INL (Integral Nonlinear) is the maximum deviation of analog-to-digital transmission curve and the ideal condition of the analog-to-digital curve. INL represents the degree of the actual transfer curve offset the ideal transfer curve, in a percentage or LSB unit [17]. After removing static disorders and gain errors, INL usually represents the following publicity:

$$\Delta INL = \left| \frac{V_D - V_{zero}}{V_{zero}} \right|, 0 < D < 2^n - 1$$

Where n is the resolution of the ADC, $V_D$ indicating the analog voltage corresponding to the digital code D, $V_{zero}$ indicating the quantized voltage corresponding to the digital encoding output is 0.

In the proto test and manufacturing stage, the error is large when current channel is below 2A which is not met the accuracy requirements. By testing the ADC module integral nonlinear curve inside the M4 [18], the most severe integral nonlinear area of domestic ADC is 2000.

![Fig.4 Integral nonlinear characteristic curve of domestic ADC](image)

M4 internal integration ADC is single pole, in order to achieve a bipolar electrical amount A/D transform, the AC input loop needs to increase the bias circuit [19]. Design the bias voltage $U_{Ref}$ in the front end of the AC input voltage, the maximum range of ADC input voltage is 3V, and the bias voltage set to $U_{Ref} = 1/2U_N = 1.5V$. 
Since the full scale original sample value of 3V is 4096, applying DC bias voltage of the original sample value of 1.5V is 2048, and the original sample value is floating up and down at 2048 when the analog magnitude is small. According to the integral nonlinear characteristic curve of the simulated ADC module, as shown in Fig. 4, its integral non-linearity is the worst in the intermediate area, that is, when the ADC reference range of 0~3V is 1.5V, the analog acquisition error is the largest.

In this paper, in an analog acquisition design, it is mainly to escape the derived area with large nonlinear points by adjusting the reference voltage. The original 1.5V_REF_BH / QD raised voltage is formed by the 3V reference voltage through the high-precision resistance division of the two resistance value of 10 kΩ. Adjusting the voltage resistance resistance to 11kΩ and 10kΩ and the raised voltage is adjusted to 1.429V (3V / 21KΩ * 10kΩ), in order to avoid the worst nonlinear area of domestic ADC points, and improve the collection accuracy of domestic ADC.

Take protection current A as an example, before and after the raising voltage modification, the analog acquisition value is contrasted as shown in Table 3. According to the test results, adjust the raised voltage by avoiding the nonlinear area of the ADC points, improves the analog sampling accuracy of domestic ADC effectively, especially the 0.2A to 2A small magnitude range analog sampling accuracy is significantly improved.
Table 3 Improved analog sampling accuracy comparison

| In/A | Before improvement | Absolute error | After improvement | Absolute error |
|------|-------------------|----------------|-------------------|----------------|
| 5    | 5.01              | 0.20%          | 5.006             | 0.12%          |
| 4.5  | 4.51              | 0.34%          | 4.499             | -0.02%         |
| 4    | 4.023             | 0.46%          | 3.999             | -0.02%         |
| 3.5  | 3.511             | 0.22%          | 3.508             | 0.16%          |
| 3    | 3.015             | 0.50%          | 3.007             | 0.14%          |
| 2.5  | 2.52              | 0.40%          | 2.506             | 0.12%          |
| 2    | 2.031             | 0.62%          | 1.998             | -0.04%         |
| 1.5  | 1.548             | 0.96%          | 1.497             | -0.06%         |
| 1    | 1.086             | 1.72%          | 0.994             | -0.12%         |
| 0.5  | 0.532             | 0.64%          | 0.491             | -0.18%         |
| 0.2  | 0.234             | 0.68%          | 0.197             | -0.06%         |

5. Device electromagnetic compatibility capability improvement research

5.1. Electromagnetic compatibility improvement of the DO loop

Complex electromagnetic environments provide high requirements for electromagnetic compatibility performance based on MCU domestic chip relay protection hardware platform. For the domestic low-voltage relay protection hardware platform designs, components that need to consider electromagnetic compatibility performance include optical coupling, digital isolation, RS232, RS485, 245, 4245, LDO, DC/DC, TVS tube, connector, etc.\(^\text{[20]}\) In selection and testing, the isolation voltage, breakdown voltage, electrostatic isolation level, etc. should be focused to ensure that domestic components meet electromagnetic compatibility requirements.

The outlet circuit which is controlled by protection MCU outputs the control signal through the expanded bus, after the Dalinkton optocoupler, the outlet relay is driven. In a fast transient immunity test, under the condition of no outlet, the optical coupler breakdown due to the fast transient pulse interference, the device sends false report of outlet loop breakdown. Co-capacitance between the collector and the emitter and filtering the electrical transient pulse interference to enhance the stability of the outlet driving optocoupler.\(^\text{[21]}\) It is verfired that all related circuits of the device perform IV stage electricity transient pulse anti-disturbance test results meet the requirements of the test standards.

5.2. EMC improvement of ADC acquisition loop

In analog acquisition function module, the reference voltage (3.0V\_Ref\_BH / QD) and the lift voltage (1.5V\_REF\_BH / QD) determine the accuracy of analog sampling and dual ADC self-test. Since the large area of the analog acquisition module and the use of the domestic MCU, the long rise of the reference voltage is extremely susceptible to electromagnetic interference. In the actual electrical fast transient pulse immunity test and surge immunity test, the reference voltage and the lift voltage would occur level fluctuations due to the electromagnetic pulse interference.

Add the pair of capacitance on the reference voltage output and the raised voltage output and each analog sampling loop to enhance the anti-interference ability of the reference voltage source and the lifting voltage\(^\text{[22]}\). The actual test verifies that the ground capacitance has a good filtering and stabilizing effect, and the results of the IV level electrical fast transient impulse immunity test and IV surge immunity test of all related circuits of the device meet the requirements of the test standards.

6. Test verification

The low-voltage line protection measurement and control device based on domestic MCU developed in this paper has passed the type test of the National Electrical Instrument Quality Supervision and Inspection Center (Report No.: WJ19570), and the device has passed 42 testing indexes. The device has been put into trial operation on the 10kV Chahua I line of 220kV Chapeng Substation in Anyang, Henan. So far, the trial operation of the device is in good condition.
7. Conclusion
The line protection measurement and control device based on domestic MCU developed by this paper takes into account the terminal compatibility and functional compatibility with existing mainstream supply devices, and achieves rapid replacement with existing devices. At the same time, the device performance indicators are equivalent to existing devices. The independent level of the relay protection industry has effectively guaranteed the safe and stable operation of state grid.

With the new opportunities for the development of the domestic chip industry, the field of power grid relay protection has gradually begun to use domestic chips. On the one hand, it is conducive to create a good domestic chip ecology, which really promote the maturity of domestic chips. On the other hand, by gradually increasing the engineering application of fully autonomous controllable devices, the long-term operating data is monitored in real-time. The long-term operating data is verifying the stability and reliability of its long-term operation, which is providing a strong support for the gradual replacement of autonomous controllable devices.

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