Scaling mixed-signal neuromorphic processors to 28 nm FD-SOI technologies

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Abstract—As processes continue to scale aggressively, the design of deep sub-micron, mixed-signal design is becoming more and more challenging. In this paper we present an analysis of scaling multi-core mixed-signal neuromorphic processors to advanced 28 nm FD-SOI nodes. We address analog design issues which arise from the use of advanced process, including the problem of large leakage currents and device mismatch, and asynchronous digital design issues. We present the outcome of Monte Carlo Analysis and circuit simulations of neuromorphic subthreshold analog/digital neuron circuits which reproduce biologically plausible responses. We describe the AER used to implement PCHB based asynchronous QDI routing processes in multi-core neuromorphic architectures and validate their operation via circuit simulation results. Finally we describe the implementation of custom 28 nm CAM based memory resources utilized in these multi-core neuromorphic processor and discuss the possibility of increasing density by using advanced RRAM devices integrated in the 28 nm Fully-Depleted Silicon on Insulator (FD-SOI) process.

I. INTRODUCTION

Neural networks and deep learning models have recently become the state of the art architectures for a wide range of applications that include data mining, signal processing, and pattern recognition [1]. However, most of these architectures are modeled as algorithms executed on power-hungry central processing units (CPUs) or graphical processing units (GPUs), often integrated in large server farms of classical von Neumann computing systems. Neuromorphic processors represent a promising alternative brain-inspired technology that, thanks to their massively parallel computational substrate, are ideally suited for implementing such algorithms [2]–[6]. These hardware devices promise to reduce power consumption by several orders of magnitude and have the potential to solve the von Neumann memory bottleneck problem thanks to their co-localized memory and computing features [7].

While neuromorphic processors made using purely digital circuits are already being implemented in advanced scaled processes [2], [4], devices designed using mixed analog and digital circuits have been implemented typically using older, less aggressive CMOS processes, such as 180 nm [3], [6].

In this paper we show how subthreshold analog designs can be scaled effectively down to 28 nm processes using Fully-Depleted Silicon on Insulator (FD-SOI) technology. We use as a reference design the analog silicon neuron described in [6] and analyze its performance and characteristics in the 28 nm FD-SOI process, addressing issues related to channel and gate leakage currents, as well as device mismatch. Moreover, we describe the set of asynchronous digital circuits that can be used to interconnect multiple instances of these neurons among each others in single-chip multi-core architectures, and provide estimates for their size, bandwidth and power consumption in these scaled processes.

II. KEY SUB-CIRCUITS IN 28 NM FD-SOI PROCESSES

The transistors operated in the subthreshold regime used in mixed signal analog/digital neuromorphic architectures implemented with 180 nm or larger feature size CMOS processes typically use currents ranging from tens of nA to currents as low as a few pA [8]. Minimum-size transistors in advanced processes have considerably larger leakage currents. To maintain these levels of currents, we performed circuit simulations of single transistors and determined their proper geometrical size. Based on these results, we optimized the design of the analog silicon neuron circuit shown in Fig. 2, and performed Monte Carlo simulations to validate its performance in the 28 nm FD-SOI process.

To build multi-neuron/multi-core architectures using these analog neuron circuits, we make use of asynchronous Address-Event Representation (AER) digital circuits. These circuits assign a tag to the neuron that spikes and route its address to one or more destinations. Routing tables and tag memories are distributed within and across the neuron arrays, and can be programmed using the same AER communication protocol. Different neural network configurations, such as convolutional networks, deep multi-layer networks, or recurrent reservoir networks, can be deployed, depending on how these memory structures are programmed. To evaluate performance of typical asynchronous AER circuits in the 28 nm FD-SOI process considered, we designed and simulated a 10-bit pipeline buffer process stage. The type of digital memories we considered for storing the tags used to route spikes from source neurons to destination synapses are Content Addressable Memories (CAMs). As these are integral part of the synapse modules, and as neuromorphic processors typically consist of large arrays.
Fig. 1: Simulated channel current $I_D$ of versus $V_{GS}$ in subthreshold region for different channel length with $V_{DS} = 0.5 \text{V}$ and $W = 200 \text{nm}$, for NMOS (a) and PMOS (b) transistors.

Fig. 2: Simplified schematic diagram of an analog I&F neuron.

of synaptic elements, these memory circuits are the ones that would occupy the main area of the chip. We discuss possible scaling strategies for implementing CAMs in order to minimize the area of the die size, in the 28 nm FD-SOI process, given a specific network size.

A. The analog subthreshold Integrate&Fire neuron

To develop mixed signal analog/digital neuromorphic processors that can be used in closed-loop application scenarios (e.g. ranging from self-driving cars to biomedical micro-devices measuring metabolites in the blood stream and deciding on what actions to take), it is necessary to endow them with computational elements that have time constants that are well-matched to the signals they are meant to process [5]. For natural signals (speech, gestures, etc.) these signals typically involve time constants of the order of milliseconds. It has been shown [6] that to achieve these time constants with the silicon neuron of Fig. 2, given a membrane capacitance of 1 pF, it is necessary to use currents of the order of a few pA. Figure 1 shows simulated current $I_D$ of PMOS/NMOS versus $|V_{GS}|$ in subthreshold region for different channel lengths, with a fixed $|V_{DS}| = 0.5 \text{V}$ and $W = 200 \text{nm}$.

A simplified subthreshold analog neuron circuit compatible with the 28 nm FD-SOI process is shown in Fig. 2. Input currents $I_{syn}$ are injected into the neuron membrane capacitance $C_M$, in parallel with a programmable constant DC current. The NMDA block models the voltage-gating mechanisms of NMDA synapses. The LEAK block models the neuron’s leak conductance. The AHP block models the generation of the after hyper-polarizing current in real neurons, responsible for their spike-frequency adaptation behavior. The Na and K block model the effect of Sodium and Potassium channels, responsible for generating action-potentials (spikes) in real neurons. The REQ and ACK signals represent the digital voltages used to communicate Address-Events to the output AER circuits. All signals ending with “!” represent global variables (shared parameters) used to set the neuron firing properties. The $I_{mem}$ and $I_{ah}$ currents represent the fast and slow variables in the AdExp model, respectively. As shown in Fig. 2, the Fast Excitatory Post-Synaptic Current (FEPSC), Slow Excitatory Post-Synaptic Current (SEPSC), Fast Inhibitory Post-Synaptic Current (FIPSC) and Slow Inhibitory Post-Synaptic Current (SIPSC), with independently fine-tunable time constant parameters, feed into different branches of the neuron circuit.

To minimize transistor mismatch effects, we identified the ones that are required to operate with small currents and assigned them large length values (e.g., $L_P = 100 \text{nm}$, $L_N = 200 \text{nm}$). Even larger transistor sizes (e.g., $500 \text{nm} / 500 \text{nm}$) were assigned key transistors relevant for mismatch (e.g.,

Fig. 3: Monte Carlo analysis results for 500 runs with circuit parameters set in a way to obtain the neuron’s mean firing rate centered at 92.74Hz and its standard deviation at 5.43, with relative error of firing rate ($\text{Std}_\text{Dev}/\text{Mean}$) equal to 5.86%.
We performed Monte Carlo analysis with 500 runs for this neuron circuit, with DC current injected through \( M_{L1} \), and with bias voltages set to obtain a firing rate of approximately 100 Hz. As shown in Fig. 3, for a mean firing rate of 92.7 Hz, the standard deviation is 5.43 and error (Std. Dev./Mean) is 5.86%.

Simulation results demonstrating examples of biologically plausible behaviors are shown in Fig. 4. The top-left quadrant shows neuron membrane potential in response to a regular current spiking train for different leaking time constants \( I_{TAU1} > I_{TAU2} > I_{TAU3} \). The top-right quadrant shows the neuron response to a regular current spiking train injection for different values of firing threshold voltage \( I_{THR3} > I_{THR2} > I_{THR1} \). The bottom-left quadrant shows the neuron response to a regular current spiking train injection for different settings of its refractory period \( I_{RFR3} > I_{RFR2} > I_{RFR1} \). The bottom-right quadrant demonstrates the spike-frequency adaptation behavior, obtained by appropriately tuning the relevant parameters in the AHP block of Fig. 2 and stimulating the neuron with a constant injection current.

With the transistor sizes chosen to minimize leakage current and device mismatch, the area of neuron, excluding the capacitor, is of approximately 20 \( \mu \text{m}^2 \). The membrane capacitor can be overlaid onto the neuron layout using Metal Insulator Metal (MIM) structures. If we assume a capacitive density of approximately 18 \( fF/\mu m^2 \), the area required to implement sufficiently large capacitors (e.g., \( C_M = 0.5pF \), \( C_A = 0.2pF \) and \( C_R = 0.2pF \)) will be approximately 50 \( \mu \text{m}^2 \).

**B. Asynchronous PCHB digital circuits**

Pre-Charge Half-Buffer (PCHB)-based asynchronous AER routing/communication circuits are used to implement multi-core neuromorphic computing architectures. These circuits can be composed by combining basic building blocks that implement basic processes (merge, split, buffer, etc.), and that follow a standard 4-phase hand-shaking protocol.

Figure 5 shows an example of RTL level pipeline buffer following 4-phase handshaking protocol and dual-rail protocol based on PCHB. The process stage includes **Handshaking**, **Validity** and **Buffer** blocks.

**Validity and Buffer** blocks. With dual-rail data protocol, the request signal from a previous stage is encoded in data, the **Validity** module checks the validity of input data and identifies the state via the signal \( in.v \). The **handshaking** block generates the acknowledge signal \( in.a \) to acknowledge its previous stage for valid input. In parallel it will wait for the acknowledge signal from its following process stage, e.g. \( out.a \), for its valid output. While taking care of hand-shaking with neighbour stages, the **handshaking** block will generate control signal \( en \) to enable **Buffer** block for dealing with current input data or reset the **Buffer** block for the next cycle (see Fig. 5).

Additional Quasi-Delay Insensitive (QDI) processes can be implemented with similar **Handshaking**, **Validity** and specific **Function** block. By using a dual-rail data flow and 4-phase handshaking, it is possible to build larger routing systems with more complex functions, properly placing and combining these concurrent processes.

Figure 6 shows the power dissipation of a 10-bit PCHB-based buffer process versus input data rate.
In this paper we described some of the issues that have to be considered when scaling mixed-signal analog/digital neuromorphic circuits to advanced scaled process nodes. We showed how, by properly sizing the transistors of analog neurons, and by optimizing its layout, it is possible to obtain reliable operation in a 28 nm FD-SOI process, reducing both silicon area and power consumption. Furthermore, we showed that for asynchronous AER routing system, scaling to more advanced processes leads to a significant improvement in bandwidth, but not to improvements in area and power efficiency. This however can be potentially solved by resorting to integration of Resistive Random Access Memory (RRAM) elements on the same substrate.

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III. Conclusion

In this paper we described some of the issues that have to be considered when scaling mixed-signal analog/digital neuromorphic circuits to advanced scaled process nodes. We showed how, by properly sizing the transistors of analog neurons, and by optimizing its layout, it is possible to obtain reliable operation in a 28 nm FD-SOI process, reducing both silicon area and power consumption. Furthermore, we showed that for asynchronous AER routing system, scaling to more advanced processes leads to a significant improvement in bandwidth, but not to improvements in area and power efficiency. This however can be potentially solved by resorting to integration of Resistive Random Access Memory (RRAM) elements on the same substrate.

TABLE I: Features of multi-core neuromorphic processor

| Technology      | 180 nm CMOS | 28 nm CMOS | 28 nm FD-SOI |
|-----------------|-------------|------------|-------------|
| Supply voltage  | 1.8V        | 0.7V-1.0V  | 1.0V        |
| Energy per spike| 88.3pJ @ 30Hz | 2.3nJ-30nJ | 50pJ @ 30Hz |
| Energy per routing| 360pJ | 230pJ | 147pJ |
| Bandwidth of routers | 400M-Events/s | 20M-Events/s | 1.8G-Events/s |
| Area of neuron  | 1188um²     | 64.6um²    | 20um²       |
| Area of synapse | 128.4um²    | 13um²      | 3um²        |

Fig. 7: Multi-core neuromorphic processor fabricated in a 180 nm CMOS process with an area of 43.79 mm², comprising 1k neurons and 64k×12-bit CAM programmable synapses subdivided among 4 cores. Inserted figure shows CAM circuit and layout implementation.

that for asynchronous AER routing system, scaling to more advanced processes leads to a significant improvement in bandwidth, but not to improvements in area and power efficiency. This however can be potentially solved by resorting to integration of Resistive Random Access Memory (RRAM) elements on the same substrate.