Duty Ratio Characteristics of Dual 2-stage Cockcroft-Walton Circuit

Masataka Minami* a) Member, Fumie Ishitani* Student Member

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High step-down DC-DC converters and rectifiers are required for large applications such as battery chargers. We previously proposed a dual 2-stage Cockcroft-Walton (CW) circuit as a high step-down all-passive rectifier. The rectifier provides the output voltage subject to circuit parameters. This study investigates the proposed circuit’s operation through numerical simulations and an experimental prototype system focusing on the input source’s duty ratio. Both the numerical and experimental procedures confirm that the output voltage of the proposed dual 2-stage CW circuit is sensitive to the input source’s duty ratio.

Keywords: High step-down rectifier, Duty ratio, Cockcroft-Walton circuit

1. Introduction

High step-down DC-DC converters and rectifiers are required to suitably transform high-voltage power for low-voltage/large-current applications such as battery chargers, uninterruptible power supply (UPS) units, and data centers (2)-(3). Power grid systems require the use of multi-stage connected conversion systems to supply electric power to low-voltage/large-current applications.

Fig. 1(a) illustrates the general configuration for a conversion system used in low-voltage/large-current applications, which consists of a power grid system, a rectifier, a high-frequency inverter, an isolated high-frequency transformer, a rectifier, and a step-down DC-DC converter. This system is controlled via three parameters, namely the duty ratio of the high-frequency inverter, turn ratio of the isolated high-frequency transformer, and step-down ratio of the step-down DC-DC converter.

For high step-down DC-DC converters, several topologies and control methods have been proposed (4)-(7). Yao et al. (6) proposed a multiphase interleaved buck converter with additional coupled windings to achieve high-frequency, high step-down power transfer. Morales-Saldana et al. (7) deformed the buck converter and developed a quadratic buck converter with a single switch. Furthermore, Ki et al. (8) presented a high step-down transformer-less single-stage single-switch AC-DC converter suitable for universal line applications. The topology integrates a buck-type power-factor correction cell with a buck-boost DC-DC cell, wherein part of the input power is directly coupled to the output after processing. Palomo et al. (9) studied a family of quadratic step-down DC-DC converters connected either in series or in parallel. Using their approach, the power transfer from the input to the output port is reduced on the interconnected converters when a non-cascading connection is used. In Japan as well, researchers investigated and analyzed the high step-down DC-DC converter. For instance, Shimizu et al. analyzed the EMI caused by buck converters (9), Kawamura et al. applied deadbeat control to a two-phase interleaved DC-DC buck converter (10), and Haga et al. proposed a wide-range output voltage and high-efficiency DC-DC converter (11).

Aside from DC-DC converters, rectifiers are also used as high step-down converters (11). Current-doubler rectifiers were used in some applications and further improved by several researchers (12)-(17).

Hence, this research considers a high step-down all-passive rectifier, which integrates both the rectifier and the step-down DC-DC converter, as shown in Fig. 1(b). As the rectifier consists of all-passive devices, the conversion system becomes highly reliable and efficient. We focus on the high step-down all-passive rectifier to design the system depicted in Fig. 1(b). Therefore, we proposed a dual N-stage Cockcroft-Walton (CW) circuit (13). Fig. 2 shows the dual 2-stage CW circuit. The proposed circuit applies the duality principle (13).
from a CW circuit, which is well-known as a high step-up rectifier.

The dual 1-stage CW circuit consists of two diodes and two inductors. Therefore, the number of components remains the same compared to conventional current doubler rectifiers, and the performance is same. The major advantage of the proposed dual CW circuit is that the number of stages can be increased. The current doubler rectifier has been proposed as a circuit topology with 2 stages, but it is difficult to increase the number of stages beyond that. Since the number of stages in the dual CW circuit can be increased, the output voltage can be stepped down by a factor of $\frac{1}{2N}$ in the dual $N$-stage CW circuit. In this paper, the dual 2-stage CW circuit is used as an example to verify the principle and to evaluate the duty ratio characteristics.

The dual 2-stage CW circuit has several advantages: simple construction and all-passive switches. The rectifier’s high reliability and durability are owing to the all-passive devices comprising the proposed circuit. In addition, the proposed circuit can reduce thermal losses, such as switching losses, due to the absence of active switches. Moreover, the proposed circuit provides the output voltage depending on the circuit parameters. As the proposed circuit has no control system, the input source must adjust the output voltage of the proposed circuit. Both the numerical and experimental procedures confirm that the output voltage of the proposed dual 2-stage CW circuit is sensitive to the input source’s duty ratio.

The remainder of this paper is organized as follows. Section 2 illustrates a circuit configuration and describes a circuit operation. Numerical and experimental verifications are presented in Section 3. Section 4 summarizes the study and the main findings.

2. Proposed dual 2-stage CW circuit

This section presents the proposed circuit in detail regarding the circuit configuration and operation. It is demonstrated that the proposed circuit steps down quarter voltage times the duty ratio and boosts fourth current.

2.1 Circuit configuration Figure 2 depicts the proposed circuit. The proposed circuit consists of four inductors $L_1, \cdots, L_4$, four diodes $D_1, \cdots, D_4$, and a smoothing capacitor $C$. The voltage of the input source $v_{in}$ provides a 0 V and $\pm V_{in}$ square wave in Fig. 3. Here, the duty ratio $d$ is defined as the rate of output $\pm V_{in}$. The input source $v_{in}$ is presented as the following equation;

$$v_{in}(t) = \begin{cases} +V_{in} & (0 \leq t \leq \frac{dT}{2}) \\ 0 & \left(\frac{dT}{2} \leq t \leq \frac{T}{2}, \frac{(1+d)T}{2} \leq t \leq T \right) \\ -V_{in} & \left(\frac{T}{2} \leq t \leq \frac{(1+d)T}{2}\right) \end{cases} \quad (1)$$

$$v_{in}(t+T) = v_{in}(t), \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \quad (2)$$

where $T$ denotes the input period. It is assumed that the inverter in Fig. 1(b) is operated in phase shift to generate a voltage waveform. Therefore, such a square wave consisting of $\pm V_{in}$ and 0 is used as the input voltage waveform. As $d$ is equal to 1, the proposed circuit steps down quarter voltage and boosts fourth current. The next subsection 2.2 describes the working principle in detail.

2.2 Ideal operation This subsection derives the ideal operation of the proposed circuit. First, the ideal operation of the proposed circuit is considered at a duty ratio $d = 1$. Further, at the duty ratio $d \neq 1$, the relationship between the output voltage $V_{out}$ and the duty ratio $d$ is derived in this subsection.

To simplify circuit analysis, the following conditions are assumed.

- The input source provide an input current $i_{in}$ as an ideal square wave $\pm i_{in}$.
- Inductors $L_1$, $L_2$, $L_3$, and $L_4$ are same value $L$.
- Inductors $L_1$, $L_2$, $L_3$, and $L_4$ have sufficiently large inductances, such that the inductor currents $i_{L1}$, $i_{L2}$, $i_{L3}$, and $i_{L4}$ and the output current $I_{out}$ can be considered constant.
- Equivalent series resistances (ESRs) of the inductors $L_1$, $L_2$, $L_3$, and $L_4$ are neglected.
- Diodes $D_1$, $D_2$, $D_3$, and $D_4$ are assumed to be ideal, i.e., their ESRs and forward voltages are neglected.

As the assumption, only two modes are considered for the output characteristics, although the proposed circuit comprises multiple. One is the negative mode of the input current, and the other is the positive mode of the input current.

In the negative mode, $i_{in} = -i_{in}$. The input current source and inductor $L_1$ form a loop. The output current flows into the two branches: $L_2$, $L_3$, and $D_2$, $D_3$, $D_4$.

In the positive mode, $i_{in} = +i_{in}$. Here, the sum of the input
current \( I_{in} \) and inductor current \( I_{L1} \) flows through the diode \( D_1 \). In addition, the presence of an inductor current, \( I_{L3} \), leads to a change in the current path from \( D_2 \) to \( D_3 \) in the circuit. Thus, the following equations hold:

\[
I_{out} = I_{L2} + I_{L4} = 2I_{in} + 2I_{in} = 4I_{in} \quad \text{(3)}
\]

Based on (3), the proposed circuit ideally provides a current four times that of \( I_{in} \), which is the amplitude of the input current.

Subsequently, using the duty ratio \( d \neq 1 \), the relationship between the output voltage \( V_{out} \) and the duty ratio \( d \) is derived. During \( dT/2 \leq t \leq T/2 \) and \((1 + d)T/2 \leq t \leq T\), the input source provides 0 V. In addition, the input current continues to flow to the same value because the input current passes through the inductor.

Assuming that the input power \( P_{in} \) and output power \( P_{out} \) are the same, the following equation holds:

\[
P_{out} = P_{in}
\]

\[
V_{out}I_{out} = \frac{1}{T} \int_0^T v_{in}i_{in} \, dt = dV_{in}I_{in}, \quad \text{(4)}
\]

From (3) and (4), the output voltage \( V_{out} \) becomes

\[
V_{out} = \frac{d}{4} V_{in}, \quad \text{(5)}
\]

This relationship (5) implies that the output voltage \( V_{out} \) can be adjusted by the duty ratio \( d \) because of \( V_{out} \propto d \).

2.3 Operation Waveforms Fig. 4 shows the input and output waveforms in the proposed circuit under \( R = 13.6 \Omega \) as an example. From the experimental results, the proposed circuit was confirmed to operate in subsection 2.2. Next section verifies the validity of this relationship (5) using numerical and experimental analyses.

3. Numerical and Experimental Analyses

This section investigates the effect of the input source’s duty ratio in the proposed circuit and shows that it adjusts the output voltage. In addition, this section reveals the evaluation metrics of the circuit, namely the efficiency.

3.1 Parameters and Conditions This subsection lists the circuit parameters and conditions. The parameters are selected based on the results of our previous studies\(^\text{(10)(11)(12)}\). To analyze the proposed circuit, the following conditions are set:

- Input voltage amplitude: \( V_{in} = 100 \text{ V} \)
- Input duty ratio: \( 0.05 \leq d \leq 1.00 \) in numerical simulation and experimental prototype system: it implies no control.
- Input frequency: \( f = 100 \text{ kHz} \)
- Inductors: \( L_1 = 10 \text{ mH} \) (ESR 284 m\( \Omega \)) and \( L_2 = 30 \text{ mH} \) (ESR 494 m\( \Omega \)) in numerical simulation from data sheet of the inductors\(^1\).
- Si SBD Diodes: threshold voltage 0.53 V and on resistance 2.1 m\( \Omega \) in numerical simulation because The experimental prototype system includes DSS2x101-015A

\(^1\) Our previous paper\(^\text{(10)}\) already discussed the relationship between the inductor and frequency to maintain CCM operation. As a result, the inductor should be more than 3 mH. This paper conducts experiments with two patterns, \( L_1 = 10 \text{ mH} \) and \( 30 \text{ mH} \), to show that \( L = 10 \text{ mH} \) is sufficient to operate the proposed circuit.

\(^\dagger\dagger\) Our previous proceeding\(^\text{(12)}\) numerically analyzed a detailed loss in the proposed circuit. The results suggest improving the proposed circuit by using low threshold voltage and on resistance of the diodes. Then, we chose these diodes.
the duty ratio $d$ of the input source.

Figure 6 shows the efficiency characteristics of the proposed circuit by the duty ratio $d$. Since the input power is determined by the duty ratio $d$, the lesser the $d$, the lesser the input power. At low power, the percentage of loss appears to be extensive. Therefore, when $d$ is small, the power is less, and the efficiency deteriorates. Looking at each load, the numerical results show that the heavier the load in the circuit, the slightly lower efficient it is. The reason is the current in the proposed circuit. The greater the current, the greater the...
conduction losses due to ESRs in the inductors and diodes. On the other hand, Fig. 6(b) shows the opposite results. The reason is that the input current waveform was greatly distorted and noisy due to the small current value. In fact, the results at 30 mH in Fig. 6(d) with a larger inductor show that the difference is negligible. This suggests that in order to increase efficiency at small currents, a larger inductor is needed to smooth the current.

4. Summary

This study investigated the proposed dual 2-stage CW circuit as a high step-down all-passive rectifier. We explained how to work the proposed circuit by classifying operation modes. In addition, we numerically and experimentally indicated that the proposed circuit can change the output voltage by adjusting the duty ratio of the input source. The proposed circuit will be experimentally applied on high step-down DC-DC converters in the future. Furthermore, we will verify the high step-down DC-DC converter in Fig. 1(b) based on an experimental prototype system for future works.

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Masataka Minami (Member) was born in Fukuoka, Japan, on November 9, 1985. He received his Bachelor’s, Master’s, and Ph.D. degrees from Kyoto University, Kyoto, Japan, in 2008, 2010, and 2013, respectively. In 2013, he joined the Department of Electrical Engineering, Kobe City College of Technology (KCCT), where he is currently an Associate Professor. From April 2018 to March 2019, he was an Academic Visitor to the School of Engineering, Ecole Polytechnique Federale de Lausanne (EPFL), Lausanne, Switzerland. His research interests include rectifiers, DC-DC converters, inverters, power systems engineering, and control applications. He received the IEEE Industry Applications Society Excellent Presentation Award in 2017 and the IEEE GCCE 2019 Excellent Poster Award; Outstanding Prize in 2019. He is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) and Institute of System, Control and Information Engineers (ISCIIE).

Fumie Ishitani (Student Member) was born in Hyogo, Japan, on November 1, 1999. She entered the Department of Electrical Engineering, Kobe City College of Technology (KCCT) in April 2015. She joined the power electronics laboratory in October 2018. She received an associate degree from Kobe City College of Technology (KCCT) in 2020. Since 2020, she is a Bachelor’s candidate in Kobe City College of Technology. Her research interests include rectifiers, DC-DC converters, and inverters.