Color My World: Deterministic Tagging for Memory Safety

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Abstract

Hardware-assisted memory protection features are increasingly being deployed in COTS processors. ARMv8.5 Memory Tagging Extensions (MTE) is a recent example, which has been used to provide probabilistic checks for memory safety. This use of MTE is not secure against the standard adversary with arbitrary read/write access to memory. Consequently MTE is primarily used as a software development tool.

We present the first design for deterministic memory protection using MTE that can resist the standard adversary, and hence is suitable for post-deployment memory safety. Using static analysis we compartmentalize memory allocations into safety classes, and describe several compile-time instrumentation techniques to efficiently shield data categorized as “safe”, such as function returns, from adversaries who exploit memory errors in the code. We incorporate our design into LLVM Clang, implementing static analysis and subsequent MTE instrumentation. Via a comprehensive evaluation we show that our scheme is effective and achieves a low run-time overhead of 13.6% and code-size overhead of 21.7% (geometric mean).

1 Introduction

Hardware-assisted memory tagging, originally introduced in early computer architectures [20] but largely abandoned shortly thereafter, has resurfaced in recent processor architectures such as lowRISC [4], SPARC M7 [1], and ARMv8.5-A [3, 9]. It is a powerful technique that allows detection of memory errors using a lock-and-key mechanism where both pointers and memory allocations are associated with tags; a pointer is allowed to access a chunk of memory if and only if both the pointer and the memory allocation have matching tag values (“colors”). Tools like hardware-assisted Address-Sanitizer (HWASAN) [5] use a randomized scheme to tag each memory allocation (and corresponding pointers) with a random tag. They can then efficiently detect many spatial and temporal memory access violations. Since the tags are randomly assigned, these tools can only provide a probabilistic guarantee of correctness. Furthermore, the guarantee is limited because the tags are short (a few bits long). However, these tools are typically used for testing in the software development phase. In such benign, non-adversarial settings, limited correctness guarantees are sufficient.

A natural question is whether and how hardware-assisted memory tagging can be used for ensuring run-time memory safety after deployment. Unlike the software development phase, post-deployment is a potentially adversarial environment: detecting memory-safety violations after deployment therefore must be robust in the presence of an intelligent adversary. The standard adversary model used in memory safety literature assumes an adversary that can exploit a memory vulnerability to read from or write to arbitrary memory locations. Memory tagging schemes that use randomized tag assignment cannot withstand such an adversary that can (a) learn tag values and subsequently inject bogus pointers with correct tags, or (b) repeat an attack until injected pointer tags match by chance. Therefore, existing memory tagging schemes, with their limited probabilistic guarantees, cannot be used directly to ensure post-deployment memory safety.

In this paper, we describe the first hardware-assisted memory tagging approach that enforces post-deployment run-time memory protection even in the presence of the standard (strong but realistic) adversary that can forge tags and repeat an attack indefinitely. Unlike prior schemes, we target deterministic memory protection without using probabilistic random tagging. To achieve this, we first use static analysis to classify memory allocations into different classes based on their level of operational safety. But because the memory tag of a pointer stored in memory is embedded within the pointer itself, the adversary can overwrite it freely. Consequently, we use a tag forgery prevention scheme to prevent attacker-controlled pointers from accessing safe allocations. Specifically, we can guarantee the integrity of provably safe allocations even in the presence of memory errors that affect the less secure classes. Furthermore, our static analysis is memory-tagging aware: it can detect allocations that are safe
only when coupled with our tagging scheme or other similar run-time enforcement.

We realize our scheme using ARMv8.5 Memory Tagging Extension (MTE) [3] which is slated to be deployed soon [26]. Our implementation is based on the LLVM compiler framework and covers both our static analysis and instrumentation.

We claim the following contributions:

- The first design for deterministic memory protection using hardware-assisted memory tagging, guaranteeing data integrity for safe classes, even against the standard adversary that can break prior memory-tagging schemes. Our scheme can thus be used to ensure post-deployment integrity of protected data. (Section 5)
- A complete ARMv8.5-A MTE based implementation of our design built on the LLVM 12 compiler framework, including augmented stack safety analysis (Section 6), and compiler back-end modifications (Section 7). We will open-source our implementation.
- A comprehensive evaluation including security analysis (Section 8.1), functional evaluation using QEMU with MTE support (Section 8.2), and performance analysis using SPEC CPU 2017 indicating a performance overhead of 13.6% and code-size overhead of 21.7% (geometric mean) (Section 8.3), shows the effectiveness of our scheme.

2 Background

2.1 ARMv8.5-A Memory Tagging Extension

The ARMv8.5 instruction set architecture (ISA) introduces the Memory Tagging Extension (MTE) feature, a hardware primitive for memory tagging (colloquially referred to as memory coloring) [3, 9]. MTE allows 4-bit tags to be assigned to each memory allocation and address (at 16-byte granularity). These are referred to as allocation tags and address tags respectively. An allocation tag is a 4-bit value associated with every memory granule (a 16-byte region of memory). Allocation tags are stored in hardware-protected tag memory. An address tag is a 4-bit value stored within the highest-order byte of a pointer.

Programs can be instrumented with explicit MTE-specific instructions to tag memory and associated pointers according to the tagging strategy. MTE provides instructions for writing and reading allocation tags in memory, as well as for efficiently manipulating the address tag bits of a pointer in a register.

For efficiency, MTE also allows unchecked accesses in some cases. First, no accesses via the stack pointer, or the stack pointer with an immediate offset, are checked. This allows compiler-generated code that modifies the stack—e.g., to store local variables in memory—to avoid tag checks. MTE

2.2 LLVM memory tagging on ARM

At the time of writing LLVM provides two sanitizers that utilize ARM MTE: the Clang HWASAN [5] and LLVM MemTagSanitizer [17]. The former, on ARM architectures, uses the top-byte ignore (TBI) feature to reserve the most-significant byte of pointers for a software-defined tag that is checked by software-only instrumentation that largely targets testing use cases. In contrast, MemTagSanitizer is designed to use MTE for protecting programs both during testing as well for during post-deployment run-time protection against an adversary that can overwrite pointers and their address tags.

2.3 LLVM StackSafetyAnalysis

LLVM StackSafetyAnalysis [19] detects stack-based variables that are “safe”, i.e., cannot cause memory errors through their use. It was originally introduced to support the Clang
SafeStack [6] used for code-pointer integrity [12], but can also be used to optimize approaches such as HWASAN. For each stack-based allocation, the analysis indicates the smallest memory region that contains all accesses by any direct or derived pointer based on the allocation. If the analysis is inconclusive, it indicates that the full memory range is accessed. Moreover, StackSafetyAnalysis does not track pointers written to memory, and instead assumes that such pointers can be corrupted or otherwise misused. Without full memory safety or fault isolation, this is the only safe assumption.

3 Adversary Model

In this work, we consider a powerful adversary, $\mathcal{A}$, that can exploit a memory vulnerability to overwrite program data, including pointers and their address tags. We assume that the memory is protected with a WeX policy. Thus, $\mathcal{A}$ can neither modify program code nor execute data (e.g., inject and run code on the program stack), but can read all process memory, including the allocation tags used by MTE. For user-space protection, we assume that the operating system is trusted, and that $\mathcal{A}$ cannot modify MTE configuration. This adversary model is consistent with prior work on memory safety [33].

The ability to read arbitrary memory allows $\mathcal{A}$ to determine all memory tags used by the process. This renders probabilistic tagging schemes ineffective against $\mathcal{A}$ that can also inject arbitrary pointers and tags. However, even without read access to allocation tags, given the limited range from which tag values are drawn, $\mathcal{A}$ can repeat an attack until it succeeds.

4 Goals and Requirements

Our goal is to partition allocations into protection domains based on their memory-safety properties, use memory tagging to enforce domain separation, and where possible, enforce in-domain memory integrity (e.g., by preventing overflows). The former is similar to the safe stack employed by Kuznetsov et al. [12] that aims to isolate provably memory-safe data from other data (such as buffers that might overflow). In particular, we use the notion of memory-safe allocations. Informally, a memory-safe allocation is one where all pointers based on the allocation are safe, and cannot cause overflows or other memory errors. See Section 5 for a more detailed definition.

We define the following requirements for our solution:

- **R1** Isolate safe allocations: Allow access to a safe allocation only through legitimate pointers to it.
- **R2** Isolate unsafe allocations: Prevent unsafe memory accesses from compromising data in safe allocations.
- **R3** Resist address tag forgery: Prevent $\mathcal{A}$ from accessing safe allocations using forged pointers.
- **R4** Resist buffer overflow: Prevent $\mathcal{A}$ from exploiting linear overflows to violate allocation bounds.

5 Design

Our design utilizes memory tagging without relying on random or hidden tags (R5), instead we: 1) isolate memory allocations into distinct protection domains (R1, R2), 2) alternate memory tags to prevent linear overflows (R4), and 3) prevent address tag forgery by explicitly setting tag bits of pointers that could be controlled by $\mathcal{A}$ (R3). We leverage an MTE-aware static analysis (Section 6) to classify memory allocations into two distinct protection domains based on whether we can guarantee the allocations to be memory safe.

We define an allocation as memory safe if all dereferences of pointers based on the allocation are either safe, or cause the program to terminate. Our definition of memory-safe allocations is based on Kuznetsov et al., who define a safe dereference as one that only accesses the memory object that the pointer is based on, and based on as: “a pointer is based on a target object X iff the pointer is obtained at runtime by (i) allocating X on the heap, (ii) explicitly taking the address of X, if X is allocated statically, such as a local or global variable, or is a control flow target (including return locations, whose addresses are implicitly taken and stored on the stack when calling a function), (iii) taking the address of a subobject y of X (e.g., a field in the X struct), or (iv) computing a pointer expression (e.g., pointer arithmetic, array indexing, or simply copying a pointer) involving operands that are either themselves based on object X or are not pointers [12].” For
brevity, we will use safe and unsafe as shorthand to refer to memory safe and memory unsafe, respectively.

If all pointer dereferences in a program are safe, then the program as a whole is memory safe and each allocation will only be modified by pointers that are based on it. Note that without program-wide memory safety, a safe allocation can still be corrupted by unsafe pointer dereferences; either using pointers based on unsafe allocations or pointers injected by $\mathcal{A}$. However, using our MTE tagging scheme and tag forgery prevention (explained in Section 5.1), we can prevent such corruption (R3) and protect safe allocations without requiring full, program-wide, memory safety.

We divide safe allocations into three types: 1) implicitly-safe allocations that are only dereferenced by compiler-generated code and are thus always safe, 2) provably-safe allocations for which our analysis can conclusively prove that all dereferences of pointers based on the allocation are safe, and 3) guarded allocations that cannot be proven safe, but for which we can prove that all unsafe dereferences of pointers based on the allocation are prevented by our instrumentation.

Our approaches to protect safe allocations is thus three-fold: 1) we use static analysis (Section 6) to identify provably-safe and guarded allocations by verifying that all dereferences of pointers based on those allocations are safe or can be guarded; 2) we use MTE to prevent unsafe dereferences using pointers based on guarded allocations (Section 5.2) from corrupting other allocations; and 3) we apply MTE to isolate unsafe allocations and tag forgery prevention (Section 5.1) to ensure that neither corrupted pointers nor attacker-injected pointers can dereference safe allocations. Figure 2 and Listing 1 illustrate the different types of allocations and will be used as a running example to explain our approach.

To maximize the set of safe allocations we also track pointers when they are stored in memory. Our intent is to guarantee that pointers based on safe allocations cannot be corrupted in memory or be used in unsafe dereferences. Consequently, if a such a pointer is ever stored in a non-safe allocation, we also mark the allocation it is based on as unsafe. All other pointers stored to or loaded from memory are assumed to be corrupted or used unsafely. Because our definition of memory safety is allocation-based we must separately address the problem of narrowing [8] with respect to pointers. Consequently, we also verify that pointers stored in compound structures cannot be corrupted, or else we use tag forgery prevention to ensure that such pointers always point to unsafe allocations.

5.1 Isolating unsafe allocations and pointers

We isolate unsafe allocations using ARM MTE (Section 2.1). At run-time, all unsafe allocations (② and ④ in Figure 2), and pointers based on them, are tagged as unsafe by clearing the topmost tag bit; resulting in a tag of form 0b0xxx. We use the default tag, 0b1100, for safe allocations and unallocated memory that is initially tagged by the kernel. The guarded allocations are similarly tagged as safe, but are surrounded by differently tagged guards—either a dedicated “red zone” or an unsafe allocation—to prevent unsafe dereferences. All unsafe allocations and pointers are tagged with the unsafe tag, 0b0xxx, tag to isolate them from the memory-safe allocations.

If $\mathcal{A}$ overwrites a pointer, it can be set to point to an arbitrary address, but also to have an arbitrary tag value, including the safe tag 0b1100. To prevent the use of such pointers, we implement tag forgery prevention by clearing the topmost tag bit of a loaded pointer, unless it was loaded from a pointer-safe allocation (Section 5.3). The address tag of an unsafe pointer could also be corrupted by large-enough indexing errors or pointer arithmetic that affects the high-order address bits of the pointer. To prevent such pointer operations from changing address tags, our tag forgery prevention stores the address tag before arithmetic operations, and then afterwards writes it back to the pointer. Consequently, even if an unsafe pointer’s address tag can be corrupted or a new pointer injected, the pointer will always be re-tagged as unsafe before use (R3).

5.2 Realizing guarded allocations

Buffer overflows are a common memory error that can be completely prevented with MTE. As long as the overflow is contiguous we can tag adjoining memory with a different tag to prevent the overflow (e.g., an overflow from ③ to ② in Figure 2). For the purpose of our work, we consider an overflow linear if it is an under- or overflow such that its iteration step—e.g., how much an iterator is incremented on each loop—and element size guarantees that the overflow cannot “hop” over the adjoining memory granule and avoid detection. We deem an allocation as guarded if it is not provably-safe, but can be shown to only allow linear overflows. The adjoining memory can be either another allocation, e.g., a local variable, or a compiler-inserted guard zone. We conservatively only assume that the adjoining 16-byte MTE granule is tagged differently. The stack layout can be optimized to avoid dedicated guards when stack variables can be reordered (Section 7.2).
5.3 Detecting safely stored pointers

Implicit compiler-generated allocations are safe as they are only used by the compiler and not exposed to the programmer. For instance, the return address (§ in Figure 2) is stored in memory, but is not directly accessible by program code. Another example are stack slots for local variables that are not explicitly referenced by the programmer (i.e., the do not “have their address taken”) or “register spills” generated by the compiler to temporarily free registers. Such implicitly-safe allocations do not require analysis, and will use the default safe tag.

In other cases, we must either assume that a pointer stored in memory is unsafe, or be able to exhaustively prove that its storage location is a safe allocation and that we can determine where it is subsequently loaded from memory. However, when considering the safety of pointers in memory, memory-safety as defined above is insufficient. We must also consider whether intra-object overflows could corrupt a pointer without violating the allocation boundaries of the storage location. For instance, an array in a data structure can potentially overflow and corrupt pointers in the structure without violating the safety of the allocation as a whole. In addition to safety, we thus also consider the pointer-safety of an allocation and deem an allocation to be pointer-safe only if it is both safe and that pointers stored within it are safe from corruption. Otherwise, we say the allocation is pointer-unsafe, and assume that any pointers stored within it might be corrupted even if the allocation as a whole is safe.

5.4 Compartmentalization

All memory within the program is assigned to different safety types as shown in Table 1. We assign tags to allocation classes so that we can isolate unsafe allocations, but also to facilitate tag forgery prevention at runtime. Specifically, whenever a pointer is loaded from a memory address, we can use the tag of the address to determine whether the loaded pointer is unsafe (shown in the ptr. load column of Table 1). Any pointer loaded from memory not tagged as pointer-safe, is tagged as unsafe, and so can only access unsafe memory. Note that pointer-safe allocations may contain unsafe pointers, but because the location is pointer-safe, we do not need to perform tag forgery prevention when loading those pointers.

| Safety class/type | Safe | Ptr. safe | Instrumentation | tag | guarded | ptr. load |
|-------------------|------|----------|-----------------|-----|---------|----------|
| implicit          | yes  | 0b1100   | —               | —   | —       | —        |
| provable          | yes  | 0b1100   | —               | —   | —       | —        |
| provable          | no   | 0b10xx   | guarded         | unsafe | —       | —        |
| guarded           | yes  | 0b1100   | guarded         | —   | —       | —        |
| guarded           | no   | 0b10xx   | guarded         | unsafe | —       | —        |
| guarded           | no   | 0b0xxx   | —               | —   | —       | —        |

Table 1: The safety classes and corresponding run-time instrumentation. tag shows the tag set on allocation. guarded indicates if guards are added. ptr. load shows if pointers loaded from the allocation are subject to tag forgery prevention.

The analysis indicates whether it can prove the allocation to be either safe (or guarded), or whether it must be assumed to be unsafe. The analysis assumes instrumentation that enforces isolation (Section 5.1) and prevents linear overflows (Section 5.2). Given such instrumentation, we can use an analysis to find allocations that:

1) are memory safe;
2) can be guarded such that their safety can be guaranteed at run-time; and,
3) are pointer-safe such that pointers within them are safe, and the safety of all pointers loaded from it can be verified.

Programmatic analysis of any non-trivial program properties is undecidable [25]. Consequently, most static analyses, including ours, are approximate. For security, the analysis must be conservative but can over-approximate the unsafe set of allocations. Our goal is to not fully analyze all memory use, but to maximize the set of allocations that can be proven memory safe (Section 5). In this work, we present an example analysis building upon the stack safety analysis by [12], but our instrumentation strategy is not tied to this specific analysis.

Our analysis consists of a local intra-procedural FunctionPass and a later inter-procedural ModulePass that collects and merges the local results. The goal is to analyze allocations, the FunctionPass tracks three types of pointers: 1) pointers to local allocations, 2) function arguments that are pointers, and 3) pointers loaded from memory. We call these such pointers base pointers. For each base pointer our analysis follows the use of that pointer and stores the information in a UseInfo container object. We reuse the UseInfo from StackSafetyAnalysis but extend it with information needed to support our analysis. When a pointer is derived from the base pointer of a UseInfo, we refer to it as being based on the UseInfo.

The FunctionPass does not track pointers passed to called functions or stored in memory, instead it only records such events in the corresponding UseInfo. For each UseInfo U, the later ModulePass then either finds and merges the corresponding UseInfo for the calls, stores, and loads; or marks
Algorithm 1  For each analyzed pointer, the FunctionPass creates a UseInfo. It then uses the def-use chain to find all uses of the allocation and update UseInfo accordingly.

```
UseInfo ← new UseInfo(base_pointer)
WorkList ← base_pointer
while !WorkList.EMPTY() do
    Ptr ← WorkList.POPL()
    for all Use ∈ Ptr.USES() do
        if Use.DEFINESNEWPOINTER() then
            WorkList ← Use
            add ptr to list
        else if Use ∈ CallInst then
            UseInfo.calls ← Ptr
        else if Use ∈ LoadInst then
            UseInfo.range ← GETRANGE(Use)
            UseInfo.DerefedBy ← GETLOADINFO(Use)
        else if Use ∈ StoreInst then
            if Use.ISPOINTEROP(Ptr) then
                ptr used
                UseInfo.range ← GETRANGE(Use)
                Otherwise, ptr itself is stored
                UseInfo.StoredIn ← Ptr
            else
                UseInfo.SETTOUNSAFE
        end if
    end for
end while
```

As unsafe. We stop processing a UseInfo if it is shown to be unsafe. The ModulePass is iterative and continues until no further updates take place. To handle cyclic function calls and to limit analysis complexity, the analysis depth is limited such that any UseInfo reaching the limit is marked as unsafe.

### 6.1 Detecting safe allocations

The UseInfo is used to store information on all uses of the base pointer or pointers based on it. As the LLVM IR is structured in static single assignment (SSA) form, we can use the base pointer’s definition-use chain—which links variables to any instruction that uses them—to track its use throughout the function, as shown in Algorithm 1. When a pointer is used to access memory, the range of that access is added to the UseInfo. When a pointer is passed to another function, the called function and offset to the base pointer is recorded in the UseInfo. When a new pointer is derived (for instance when incrementing an iterator), the new pointer is stored for subsequent analysis. Finally, to support tracking pointers in memory, we also record any pointer loads in the UseInfo.DerefedBy list and pointer stores in the UseInfo.StoredIn list. If the analysis cannot handle some use of a pointer—for instance, a memory access with an unknown offset—the corresponding UseInfo is marked as unsafe and further analysis is stopped. As the FunctionPass is

```c
void func_1(int **arg) {
    int A, B;
    int *ptr;

    A = 0;  // Safe assignment to A
    ptr = &B;  // Create pointer to B
    func_2(ptr);  // Pass pointer to ptr
    func_2(arg);
}

void func_2(int **ptr) {
    for (int i = 0; i < 10; ++i)
        (*ptr)[i] = 0;
}
```

Listing 2: Function with variables of different security classes.

local, it cannot resolve how pointers passed to called functions are used and instead only stores information about the call for later analysis. We also defer resolving the use of pointers stored in memory to the ModulePass.

Listing 2 shows an example of two functions that can only be partially resolved locally. During the FunctionPass, only A in func_1 can be determined to be safe, as no references to it are passed outside the local scope or written to memory. In contrast, a reference to B is stored in memory and then passed to the called function, so its safety cannot be determined before the ModulePass. When analyzing func_2, the ptr argument can be fully analyzed because it is not written to memory or used outside the local scope.

The ModulePass resolves any calls or stores of potentially safe allocations until each allocation is either exhaustively analyzed and proven safe, or assumed to be unsafe. It works by adding all functions to a work list and then processing the list one function at a time, as shown in Algorithm 2. Within a function, every UseInfo U is then processed. For each function call in U.calls, we query the analysis results for the corresponding argument UseInfo in the called function and merge it to U. For each memory store in U.StoredIn, we query the UseInfo.DerefedBy list (populated by Algorithm 1) of that storage location and merge these to U. If a pointer is stored or loaded in an unsafe location, or if we cannot find UseInfo for all possible store or load locations of U, then U is marked unsafe.

When merging a UseInfo to U, we add the memory access ranges, the calls, StoredIn, and DerefedBy lists to U. If the processing of a function causes changes in any of its UseInfo then all of its callers are re-inserted on the top of the work list. The ModulePass only works with UseInfo objects and does not need to process the LLVM IR again.

For example, in Listing 2, the ModulePass will update func_1 by going through its set of UseInfo. As ptr has func_2 in its calls set, the UseInfo of the corresponding argument of func_2 is merged to it. The merge includes not only the immediate access range of ptr, but also the addi-
Algorithm 2 The ModulePass processes functions one at a time by updating their contained UseInfo objects.

function RUN_MODULE_PASS(CallersMap, WorkList)
    while !WorkList.IS_EMPTY() do
        F ← WorkList.Pop()
        if F.INCREASES_LESS_THAN(LIMIT) then
            F.SET_ALL_TO_UNSAFE(U)
        else
            for all UseInfo U ∈ F do
                OriginalU ← U
                for all C ∈ UseInfo.calls do
                    U.MERGE_CALLEE_USE_INFO(C)
                end for
                for all L ∈ C.Derefed_by do
                    U.MERGE_LOAD_USE_INFO(L)
                end for
                end for
                if (OriginalU ≠ U) then
                    WorkList.PUSH_ALL(Callers[F])
                end if
            end for
        end if
    end while
end function

Figure 3: The static safety analysis is extended to also track the linear access range and maximum index step.

mented to be effectively memory safe or crash at run-time (Section 5). For this, we extend UseInfo to separately track the arbitrary access ranges and the linear access range (Figure 3). To determine whether linear overflows can be prevented using MTE, we also store the information necessary to determine 1) whether the linear access starts within bounds, and 2) whether the increment / decrement size is less than the used MTE memory-tag granule size used by the instrumentation. For example, in Listing 1, buf_lin is always first accessed within bounds, and guaranteed to hit a different MTE memory tag because a single loop iteration increments the address by sizeof(unsigned) bytes which is smaller than the MTE tagging granule of 16 bytes.

The memory access range analysis uses the LLVM’s scalar evolution framework to determine linear access behavior. For instance, in a loop over an array, the scalar-evolution indicates the first element accessed and how the index changes—or, evolves—on each iteration of the loop. If the start and indexing steps are known and bounded, we treat the access as linear and update the linear access range, start range, and indexing step in UseInfo. Otherwise, we treat the access as non-linear and only update the arbitrary access range. The linear access information is updated along with other ranges, as specified in Algorithms 1 and 2. Consequently, as long as the accessory access range remains bounded, the indexing step remains bounded, we can designate an allocation to be guarded, even if it would not otherwise be memory safe.

6.3 Tracking pointers stored in memory

Our safety analysis can also reason about pointers stored in memory when the strong isolation provided by MTE can guarantee that such pointers remain uncorrupted. Where in the general case we need a full program analysis to reason about memory safety, the isolation guarantees allow for a more lightweight local analysis. As shown in Algorithm 1, when our FunctionPass encounters a pointer is stored in memory, we mark it as unsafe unless we show that the storage location is safe. Specifically, we look at the StoreInst and use the use-def chain to verify that all possible pointer operands of the instruction have a corresponding UseInfo we can prove as safe. We mark the UseInfo unsafe if the use-def traversal encounters non-local memory; for instance, if the pointer operand is

6.2 Detecting linear-overflows

In addition to provably memory-safe allocations, our analysis also recognizes guarded allocations that can be instru-
7.1 Protecting safe allocations

Our new IR pass, MTStack, is responsible for tagging both pointers and memory allocations (Section 7.1.1). It runs our memory safety analysis and uses the analysis results to guide which allocations to tag (Sections 5.1 and 6.1). We use the default tag for safe allocations. Consequently, MTStack only needs to tag unsafe allocations and pointers based on them, whereas the kernel will initially tag the stack with the default tag. On mainline Linux, the default tag is set to 0b0000 [7]. We change the default tag to 0b1100, which avoids the need for special handling of NULL pointers that would otherwise unintentionally have the safe tag. A second IR pass, MTStackLoad, then instruments unsafe pointer operations and loads to realize tag forgery prevention (Section 7.1.2).

7.1.1 Tagging

The MTStack pass initially instruments the IR alloca calls that generate stack allocations. For each stack allocation MTStack checks if it is unsafe, and if so, inserts a llvm.aarch64.settag intrinsic that tags the allocation. Compiler intrinsics are compiler-defined functions that are lowered to architecture-specific code during machine code generation. Consequently, the compiler can optimize intrinsics based on their defined high-level semantics while deferring the detailed machine code generation to later. We minimize register pressure when lowering the IR by marking the addg and subg instructions that generate tagged pointers as re-materializable; i.e., such that tagged pointers can be re-created instead of needing to be stored.

To prevent temporal memory errors, MTStack resets the tags of all unsafe allocations when the stack frame is released on function return. Moreover, resetting tags also ensures that unallocated memory is returned to its default state.

The C alloca poses a challenge because the allocated memory can be dynamically sized and is freed only at function exit. An alloca can be anywhere—including in conditional blocks—and it may not always be executed before return. Consequently, we do not always statically know whether, and how much, memory is allocated on the stack. MTStack marks such functions with a new reset-tags attribute, that is used by the PrologEpilogInserter (PEI) to inject an intrinsic that re-tags the whole stack frame before return.

Finally, recall, that on ARMv8.5 MTE the granularity size is 16 bytes (Section 2.1). Therefore, the instrumentation must pad and align all tagged allocations to the granularity size. For alignment, MTStack uses the existing align attribute to set the alignment of allocations in the IR. To avoid unnecessary transformation of the IR, we do not add padding in MTStack. Instead, allocations that must be padded are marked with our new tagged attribute. We then extend the MachineFrameInfo to resize the marked stack slots based on the tagged attribute.
7.1.2 Tag forgery prevention

MTStackLoad ensures that all corrupted pointers are tagged as unsafe before their use, and that pointer arithmetic cannot be used to modify address tags. If the pointer was loaded from unsafe memory, MTStackLoad clears the topmost bit in the address tag of the pointer before it is dereferenced. As a result, either the loaded pointer was stored in safe memory and its address tag remains unchanged; or it was loaded from unsafe memory and the topmost tag bit will be unset before it is used to access memory.

A common pattern is to use pointer “sentinel” values—e.g., NULL—to check an object is allocated before use. Since tag forgery prevention interferes with this, our instrumentation retains the unmodified pointer for use in comparisons.

MTStackLoad prevents tag forgery via (overflowing) pointer arithmetic. To do so, MTStackLoad inspects getelementptr (GEP) instructions that are used to represent pointer arithmetic in the IR. Either the GEP can be statically determined as correct, or it is instrumented to prevent it from changing address tags.

7.2 Preventing linear overflows

To realize the guarded safety type, MTStack inserts memory guards around guarded allocations (Sections 5.2 and 6.2). The tags of a memory guard and its guarded allocation are different. The guard can be either additional unused memory or an existing allocation with a different tag (see Figure 2).

We insert memory-guard allocations and mark them as such using our llvm.aarch64.memoryguard intrinsic that prevents other passes from removing them because they appear unused. During machine code generation, the intrinsic is used to identify the stack slot and to mark it as a memory guard through an added interface in the MachineFrameInfo class. Later, the AArch64MemoryGuard pass will remove redundant memory guards, for example, if there is already a differently tagged unsafe allocation adjoining a guarded allocation, then an explicit guard is not needed between them.

7.3 Pointer-safe tagging

Recall that safe allocations could still allow inter-object corruption unless it is also pointer-safe (Sections 5.3 and 6.3). To distinguish such safe, but pointer-unsafe allocations, we tag them using the 0b10xx. Consequently, we can at run-time distinguish pointers loaded from pointer-safe allocations, and apply tag forgery prevention to all other loaded pointers.

8 Evaluation

We evaluate our design and implementation described in Sections 5 to 7 in terms of security, functionality, and performance with respect to the requirements defined in Section 4.

8.1 Security evaluation

To show that safe allocations cannot be corrupted (R1), we show that pointers based on unsafe allocations cannot corrupt them (R2) and that A cannot forge safe address tags (R3).

Our memory safety analysis is conservative (Section 6), but not necessarily complete. Hence, we might not find all safe and pointer-safe allocations, but ensure that those found are, in fact, safe. To do so, an allocation and associated pointers are marked as safe only if we can track all references to it, and verify that those pointers are safely used (Algorithms 1 and 2). Consequently, we know that a pointer is tagged as safe only if it based on a safe allocation and cannot corrupt or overflow other allocations (Section 5). Conversely, we know that any other pointer is initially tagged as unsafe and prevented from accessing safe allocations by the MTE hardware. To ensure R2 we must also prevent A from forging or altering pointers such that they have the safe tag.

The tag forgery prevention feature of our MTE instrumentation prevents A from introducing new pointers with safe tags via pointer corruption or injection (Sections 5.1 and 7.1.2). Specifically, we ensure that: 1) the first tag-bit is cleared when casting a non-pointer to a pointer (thus tagging it as unsafe), 2) unsafe pointer arithmetic cannot change the address tag, and 3) any pointer loaded from pointer-unsafe memory is tagged as unsafe. Consequently, while A can set pointer-unsafe pointers to arbitrary values, these are subject to tag forgery prevention before they can be used. To avoid tag forgery prevention, A could use intra-allocation corruption and inject forged pointers into pointer-safe memory without violating the allocation boundaries. To address this, our analysis verifies that non-pointer writes cannot corrupt pointer fields in pointer-safe allocations (Sections 5.3 and 6.3). A might still inject pointers as values into non-pointer fields; but in this case, the value will be subject to tag forgery prevention when it is cast to a pointer before dereferencing. Consequently, tag forgery prevention stops A from accessing safe allocations using forged address tags, irrespective of whether those tags are directly manipulated or injected into memory (R3).

We use alternating tag values to prevent buffer overflows. Specifically, we tag adjacent allocations to realize the guarded subset of the safe domain (Section 7.2). Our analysis verifies that any such guarded overflow cannot “jump” past the alternating tags by incrementing the pointer more than the 16-byte memory granule (Section 6.2). Consequently, such allocations can be safely added to the safe domain (R4).

We do not rely on random or hidden tags, hence our MTE instrumentation is not affected by memory disclosures that leak memory tags (R5). Therefore, we conclude that our design meets requirements R1–R5.
8.2 Functional verification

For functional verification, we use QEMU 6.0.0, which supports MTE [23]. The emulator replicates MTE functionality on architectural level, and so, can be used to test compatibility between our instrumentation, MTE, and existing source code. We compiled fully instrumented variants of the evaluated SPEC CPU 2017 benchmarks [31] and executed them on QEMU 6.0.0. The functional verification consists of all the C language benchmarks, which we also used for our performance evaluation (see Table 2). Since the SPEC CPU 2017 benchmark suite consists of real-world programs, the evaluated tests are a strong indication that our instrumentation strategy is widely applicable (R6).

8.3 Performance evaluation

Our performance evaluation covers three aspects of our MTE instrumentation overhead: 1) the increase in code size due to added instrumentation code, 2) the increase in stack use due to the need to align and pad memory, and 3) the increase in execution time due to changes by instrumentation and checks by the MTE hardware. We used the SPEC CPU 2017 [31] C benchmarks shown in Table 2 for performance evaluation.

We estimate code and stack size as follows: The code size is estimated by comparing the .text section size of non-instrumented and fully instrumented benchmark binaries. As the stack grows and shrinks during execution, maximum runtime stack use is not necessarily a useful metric. Instead, we gather compile-time statistics and measure the average function stack-frame increase throughout the whole program. Both the stack-frame size and .text size is determined based on fully MTE-instrumented binaries.

The execution-time overhead cannot be directly measured without MTE hardware or cycle-accurate emulators. Therefore, we instrument the benchmarks with emulated MTE overhead analogues as described below (Section 8.3.1) and run them on a TaiShan 2280 Balanced Model [11] with a Kunpeng 920 [35], an ARMv8 class-A CPU without MTE support. We measured the run time of each benchmark using the GNU/Linux time utility over 10 runs each.

8.3.1 Emulating MTE-instruction overhead

The performance overhead in terms of execution time consist of four components: 1) changes in code or memory layout, 2) address tagging, 3) memory tagging, and 4) tag checks on memory access. To measure the instrumentation overhead, we ensure that each component is measurable as-is, or by using an MTE overhead analogue to estimate an upper bound. Our analogue is similar to the independently developed, MTE instruction analogue used by HAKC [21] in that we manipulate the tag bits of pointers to simulate address tags and replace memory tag writes with regular writes to memory. We now describe in detail our MTE overhead analogue used for each of these.

Code and memory layout changes are caused by the need to align allocations to the MTE granule of 16-bytes, increased register pressure, and other changes needed to accommodate the added code. Where possible, we convert each MTE instruction to an equivalent generic instruction with the same arguments. Doing so minimizes code layout changes caused by the overhead emulation. In some cases, such as with st2g, we need multiple general-purpose instructions to emulate a single MTE instruction. However, this does not invalidate our upper bound as our code layout changes always increase code size, never decrease it.

Address tagging is emulated using regular bit manipulations to modify the address bit of a pointer. The specialized MTE instructions are expected to be at least as fast as the corresponding bit-manipulation realized with general purpose instructions. Similar to any MTE instrumentation, we then enable the TBI feature (Section 2.1) to ignore tag bits during address translation.

Memory tagging overhead is challenging to estimate without access to actual tag-memory implementations. However, these operations are specialized to modify tag memory (Section 2.1) we can assume that they are optimized to take advantage of locality and the CPU caches. Therefore, we use regular stores to represent an upper bound on the cost of writing to the specialized tag memory. Specifically, we convert all memory tag writes to regular memory writes.

Tag checks implemented in hardware are likely to have minimal overhead. We cannot simulate the overhead without substantially inflating the estimate. However, the tag-check overhead is expected to be negligible and uniformly applied to all memory accesses. Consequently it is not included in our measurements, and we note that real MTE-capable hardware will also induce a small to negligible overhead due to allocation tag lookup and check on memory accesses.

8.3.2 Results

Benchmark results and statistics on instrumentation are summarized in Table 2. The geometric mean (geo. mean) of the execution-time overhead is 13.6%. Comparing this to the estimated 7% MTE tag-checking overhead reported by [14], this suggests that the tag forgery prevention instrumentation is a significant contributor to the overhead. The Safe column in the table shows the proportion of allocations in bytes that is tagged as safe, but because this can be skewed by large allocations and is based on static information, it does not necessarily correlate with the frequency of tag forgery prevention events at run-time. We also expect that the tag forgery prevention overhead can be lowered by optimizing it to avoid redundant tag checking, and further by more accurate analysis and by optimizing the use of stack guards. Nonetheless, even the test that performs worst, 500.perlbench_r, only reaches an
overhead of 26.8%, indicating that our MTE instrumentation performance overhead is efficient (R7).

For the binary .text segment size, we see an increase of 21.7%, geo. mean. The increased size consists of additional code to tag stack slots, and to perform tag forgery prevention. We observe a stack-size increase of 19.3% (geo. mean), excluding the tag memory. This overhead is due to the need to pad and align tagged allocations to 16-bytes, and because guarded allocations must be interleaved such that the stack frame is split into disjoint sections with different tags. The memory use overhead largely depends on how stack memory is used; frequent small allocations quickly accumulate overhead due to the alignment requirements. Indeed, in the benchmarks we notice widely varying memory overheads; from an almost 50% increase in average stack size for 519.ibm_r, to a negligible ~1% increase in 505.mcf_r. When also accounting for the very low Safe value in the latter test, we can postulate that the 505.mcf_r code includes large, frequently used but relatively few unsafe stack allocations.

9 Related Work

Tagged computer architectures emerged in the 1970s to provide data typing and data isolation. For instance, the Burroughs B6700 used memory tags to realize typed memory [13]. In these hardware architectures, type and data were co-located in registers and often also in memory. Although this form of fine-grained memory typing disappeared from commercial computing for 50 years, coarse-grained hardware-assisted memory tagging has recently re-emerged in contemporary processor designs such as lowRISC [4], SPARC processors with the Application Data Integrity feature [1], and AArch64 MTE used by this paper [3]. The CHERI capability architecture also uses memory tagging, but only to provide the integrity of the capabilities that then include metadata for checking validity of memory accesses [34].

Today, Clang HWASAN [29] uses memory tagging to improve performance of AddressSanitizer (ASAN) [27]. As discussed in Section 2.2, HWASAN does not use MTE, but rather enables the use of software-defined tagging with the TBI feature. HWASAN relies on a purely probabilistic tagging scheme for detection of memory errors. Given the risk of tag forgery, the limited tag size, and the probabilistic approach to tag allocation, HWASAN is mainly used as a testing tool, rather than as a run-time protection scheme.

In contrast, LLVM’s MemTagSanitizer [17] targets post-deployment run-time protection. Currently, it only supports stack protection, although heap-protection is planned via the Scudo hardened allocator [18]. While MemTagSanitizer is nominally intended to provide run-time protection, it is not designed for the standard adversary model (Section 3) for memory safety. Specifically, it cannot withstand an adversary that can read tags, and subsequently, inject correctly-tagged pointers. Moreover, while it prevents most overflows, it relies on random tagging to detect arbitrary writes and use-after-free type errors. In contrast, we target the standard, more powerful, adversary model. Nonetheless, MemTagSanitizer could be combined with our work to mitigate errors between unsafe allocations, while using our instrumentation and tag forgery prevention to guarantee the integrity of safe allocations.

The recent HAKC uses both ARM Pointer Authentication (PA) and MTE to realize compartmentalization within the kernel [21]. PA also covers the MTE bits in a pointer, and HAKC relies on it for tag integrity. HAKC requires the developer to define compartmentalization policies for the kernel and to explicitly define data-ownership transfers between different modules. Consequently, the overhead also heavily depends on the compartmentalization strategy, ranging from 2%-4% in a single-compartment case, to a linear increase of 14%-19% percent per compartment.

We build upon the SafeStackAnalysis introduced by [12]. In their work, safe allocations are protected by moving them to a Safe Stack at a randomized location. It relies on address-space layout randomization (ASLR) which is not resistant to the standard adversary model that includes full memory disclosure [29]. Relying on shadow stacks also changes the system application binary interface (ABI), making integration with legacy code difficult.

The more recent Data Guard [10] introduces an improved static analysis scheme that, similar to our work, can recognize pointers that are safely stored. While their analysis accuracy is impressive, Data Guard uses Safe Stack for protection, with the shortcomings listed above.

WIT is a data-flow integrity (DFI) scheme that uses software-based memory tagging to restrict data-writes to only allowed objects based on a data-flow graph [2]. It uses a separate metadata table to store tags and static run-time checks to verify that written memory is tagged with one of the expected values. Because WIT uses static checks, it cannot, at run-time, distinguish between different valid pointers that can be differentiated by MTE address tags. HDFI [30] describes RISC-V support for tagging, and similarly to WIT, uses it for DFI. HDFI shows the applicability of tagging to coarse-grained isolation as well as a building block for memory safety solutions such as shadow stacks. HDFI reports very low overhead (< 2%), but uses only a single tag bit, and requires static checks using specific load and store instructions.

10 Future work and Conclusion

Due to their scarcity, we do not consider pointers loaded from uninitialized memory, hence, ∃ could attempt to exploit a use-before-initialization error to inject unsafe pointer. Such errors are relatively rare—absent in the top 25 CWEs of 2021 [22]—and can be detected using existing sanitizer such as the LLVM MemorySanitizer [32]. As future work, we will nonetheless consider extending the pointer-safety analysis to also verify initialization before use.
Our work is the first design for deterministic memory safety in a strong adversary model, using an MTE-based compartmentalization design, that fully protects stack control-flow data and data that can be proven safe. The first processors with MTE were announced very recently [26]. It is reasonable to expect other ARM processor manufacturers to follow suit. Therefore, our work exploring novel ways of using MTE is timely. Our work also provides a clear direction to designers of future memory tagging schemes: incorporating support for tag forgery prevention (Section 5.1) into their hardware design can substantially reduce the performance overhead.

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References

[1] Kathirgamar Aingaran, Sumti Jairath, Georgios Konstadindis, Serena Leung, Paul Loewenstein, Curtis McAllister, Stephen Phillips, Zoran Radovic, Ram Sivaranmakrishnan, David Smentek, and Thomas Wicki. “M7: Oracle’s next-Generation Sparc Processor”. In: IEEE Micro 35.2 (2015), pp. 36–45.

[2] Periklis Akritidis, Cristian Cadar, Costin Raiciu, Manuel Costa, and Miguel Castro. “Preventing Memory Error Exploits with WIT”. In: Proceedings of the 2008 IEEE Symposium on Security and Privacy (SP ’08) (SP ’08). SP ’08. Oakland, CA, USA, 2008, pp. 263–277.

[3] ARM Ltd. Armv8.5-A Memory Tagging Extension. Whitepaper. 2019.

[4] Alex Bradbury, Gavin Ferris, and Robert Mullins. Tagged Memory and Minion Cores in the lowRISC SoC. lowRISC-MEMO 2014-001. University of Cambridge, 2014.

[5] Clang team. Hardware-Assisted AddressSanitizer Design Documentation — Clang 11 Documentation. Clang 11 documentation. 2020. URL: https://releases.llvm.org/11.0.0/tools/clang/docs/HardwareAssistedAddressSanitizerDesign.html (visited on 11/25/2020).

[6] Clang team. SafeStack — Clang 11 Documentation. Clang 11 documentation. 2020. URL: https://releases.llvm.org/11.0.0/tools/clang/docs/SafeStack.html (visited on 11/25/2020).

[7] Vincenzo Frascino and Catalin Marines. Memory Tagging Extension (MTE) in AArch64 Linux. The Linux Kernel documentation. 2020. URL: https://www.kernel.org/doc/html/latest/arm64/memory-tagging-extension.html (visited on 02/02/2022).

[8] Ronald Gil, Hamed Okhravi, and Howard Shrobe. “There’s a Hole in the Bottom of the C: On the Effectiveness of Allocation Protection”. In: Proceedings of the 2018 IEEE Cybersecurity Development. SecDev ’18. Cambridge, MA, USA, 2018, pp. 102–109.
[29] Kostya Serebryany, Evgenii Stepanov, Aleksey Shlyapnikov, Vlad Tsyrklevich, and Dmitry Vyukov. *Memory Tagging and How It Improves C/C++ Memory Safety*. 2018. URL: http://arxiv.org/abs/1802.09517 (visited on 11/26/2020).

[30] C. Song, H. Moon, M. Alam, I. Yun, B. Lee, T. Kim, W. Lee, and Y. Paek. “HDFI: Hardware-assisted Data-Flow Isolation”. In: *Proceedings of the 2016 IEEE Symposium on Security and Privacy*. SP ’16. San Jose, CA, USA, 2016, pp. 1–17.

[31] Standard Performance Evaluation Corporation. *SPEC CPU® 2017*. 2019. URL: https://www.spec.org/cpu2017/ (visited on 12/06/2020).

[32] Evgeniy Stepanov and Konstantin Serebryany. “MemorySanitizer: Fast Detector of Uninitialized Memory Use in C++”. In: *2015 IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*. 2015, pp. 46–55.

[33] László Szekeres, Mathias Payer, Tao Wei, and Dawn Song. “SoK: Eternal War in Memory”. In: *Proceedings of the 2013 IEEE Symposium on Security and Privacy*. SP ’13. San Francisco, CA, USA, 2013, pp. 48–62.

[34] Robert N.M. Watson, Jonathan Woodruff, Peter G. Neumann, Simon W. Moore, Jonathan Anderson, David Chisnall, Nirav Dave, Brooks Davis, Khilan Gudka, Ben Laurie, Steven J. Murdoch, Robert Norton, Michael Roe, Stacey Son, and Munraj Vadera. “CHERI: A Hybrid Capability-System Architecture for Scalable Software Compartamentalization”. In: *Proceedings of the 2015 IEEE Symposium on Security and Privacy*. Vol. 2015-July. SP ’15. San Jose, CA, USA, 2015, pp. 20–37.

[35] Jing Xia, Chuanning Cheng, Xiping Zhou, Yuxing Hu, and Peter Chun. “Kunpeng 920: The First 7-Nm Chiplet-Based 64-Core ARM SoC for Cloud Services”. In: *IEEE Micro* 41.5 (2021), pp. 67–75.