Superconducting bipolar digital-to-analog converter equipped with dual double-flux-quantum amplifier

Yoshinao Mizugaki\(^a\), Tomoki Watanabe, and Hiroshi Shimada
Department of Engineering Science, Graduate School of Informatics and Engineering, The University of Electro-Communications (UEC Tokyo),
1–5–1 Chofugaoka, Chofu, Tokyo 182–8585, Japan
\(^a\) y.mizugaki@uec.ac.jp

Abstract: Precise voltage generation is a unique feature of superconducting single-flux-quantum (SFQ) circuits, and hence, several SFQ-based digital-to-analog converters (DACs) have been designed for metrological applications. In this letter, we propose a dual double-flux-quantum amplifier (dual-DFQA) that extends DAC output voltage from unipolar to bipolar. An SFQ-based DAC comprising a 4-bit variable pulse number multiplier and a \( \pm 20 \)-fold dual-DFQA is fabricated using a niobium integration technology. A 1-kHz, \( \pm 0.29 \)-mV sinusoidal voltage waveform is successfully synthesized.

Keywords: Josephson effects, single-flux-quantum (SFQ), niobium integrated circuits, pulse-frequency modulation

Classification: Superconducting electronics

References

[1] C. A. Hamilton: “Josephson voltage standard based on single-flux-quantum voltage multiplier,” IEEE Trans. Appl. Supercond. 2 (1992) 139 (DOI: 10.1109/77.160152).
[2] V. K. Semenov: “Digital to analog conversion based on processing of the SFQ pulses,” IEEE Trans. Appl. Supercond. 3 (1993) 2637 (DOI: 10.1109/77.233969).
[3] H. Sasaki, et al.: “RSFQ-based D/A converter for AC voltage standard,” IEEE Trans. Appl. Supercond. 9 (1999) 3561 (DOI: 10.1109/77.783799).
[4] M. Maezawa, et al.: “Rapid single flux quantum digital-to-analog converter for AC voltage standard,” Physica C 426–431 (2005) 1674 (DOI: 10.1016/j.physc.2005.02.130).
[5] Y. Mizugaki, et al.: “9-bit superconductive single-flux-quantum digital-to-analog converter,” Electron. Lett. 50 (2014) 1637 (DOI: 10.1049/el.2014.1926).
[6] T. Watanabe, et al.: “4-bit bipolar triangle voltage waveform generator using single-flux-quantum circuit,” Phys. Procedia 65 (2015) 213 (DOI: 10.1016/j.phpro.2015.05.120).
[7] T. Watanabe, et al.: “Modified double-flux-quantum amplifier for bipolar voltage multiplication,” 15th Int. Superconductive Electronics Conf. (2015) DS-P13 (DOI: 10.1109/ISEC.2015.7383472).
[8] Q. P. Herr: “Stacked double-flux-quantum output amplifier,” IEEE Trans. Appl.
1 Introduction

Besides ultra-fast digital signal processors with extremely low power consumption, superconducting single-flux-quantum (SFQ) circuits are expected to realize voltage waveform synthesizers of quantum accuracy. Since the first proposal by Hamilton [1], several research groups have developed SFQ-based digital-to-analog converters (DACs) for metrological applications, e.g., AC voltage standards [2, 3, 4]. Recently, we demonstrated a 9-bit SFQ-DAC in which an SFQ pulse-frequency modulation (PFM) technique was employed [5]. Several voltage waveforms, such as saw-tooth and sinusoidal waveforms, were synthesized by programming the digital input code fed from a room-temperature digital data generator.

Among several issues to be settled in our SFQ-PFM DACs, realization of bipolar output voltage was crucial for metrological applications. We first demonstrated an SFQ-PFM DAC with two output ports, between which the differential voltage became bipolar [6]. Then, to realize not differential but true bipolar output voltage, we developed a polarity-switchable (PS) double-flux-quantum amplifier (DFQA), where the output voltage polarity was controlled by switching the polarity of bias currents [7]. We also implemented a PS-DFQA into an SFQ-PFM DAC, and confirmed bipolar voltage waveform synthesis. One matter for concern was that the switching of the bias current polarity induced output voltage fluctuation, which should be avoided in metrological application.

In this letter, we present another bipolar SFQ-PFM DAC. Bipolar voltage output is realized by a dual double-flux-quantum amplifier (dual-DFQA), in which a DFQA for positive output and that for negative output are connected in series. We demonstrate our design and operation of a 4-bit SFQ-PFM DAC equipped with a ±20-fold dual-DFQA of which the circuit scale is chosen for functional demonstration.

2 Circuit design

2.1 Dual double-flux-quantum amplifier (dual-DFQA)

A DFQA is a quantum voltage multiplier comprising three-junction loops (3JLs) with one current bias and two flux bias lines [8, 9, 10]. One junction in a 3JL is
under-damped, where $4\pi$ phase leap (DFQ generation) occurs for every input SFQ. We have designed and tested several DFQAs, and confirmed that the multiplication errors are less than ±0.1% [5, 10, 11]. A conventional DFQA works as a unipolar voltage multiplier with unipolar bias current sources.

The configuration of a dual-DFQA, which we propose in this letter for bipolar voltage multiplication, is shown in Fig. 1. Two DFQAs for positive and negative voltage multiplication are connected in series. The input terminal for the positive voltage multiplication is directly connected to the input Josephson transmission line. On the other hand, to avoid short circuiting, the input terminal for negative voltage multiplication is modified from direct to inductive coupling with a driver/receiver configuration [12]. Bias current sources are prepared for each DFQA. Polarity of the output voltage is selected by a demultiplexer (Demux) placed in front of the dual-DFQA, as described in the next subsection. A dual-DFQA is free from bias polarity switching, while it requires twice circuit elements than a PS-DFQA.

![Fig. 1. Configuration of a dual double-flux-quantum amplifier (dual-DFQA). Flux bias lines are not shown. There are two DFQAs connected in series. The upper and lower DFQA are used for positive and negative voltage multiplication, respectively. Inductive coupling structure (Driver-Receiver) is employed at the input stage of the lower DFQA. Critically-damped and under-damped junctions are indicated by bow-tie and cross marks, respectively.](image)

### 2.2 Bipolar single-flux-quantum pulse-frequency modulation digital-to-analog converter (bipolar SFQ-PFM DAC)

We have designed a 4-bit bipolar SFQ-PFM DAC integrated with a ±20-fold dual-DFQA as shown in Fig. 2. It is our ordinary DAC design except for the dual-DFQA with a Demux. Circuit operation is as follows. A reference microwave (MW) of frequency $f_{\text{ref}}$ is converted to an SFQ pulse train of repetition frequency $f_{\text{ref}}$ at the dc-to-SFQ converter (DC/SFQ). Each SFQ pulse is then multiplied by $m(t)$ at the variable pulse number multiplier (V-PNM), where $m(t)$ is an integer between 0 and 15. The multiplication factor $m(t)$ is controlled by a 4-bit digital code programmed on a room-temperature digital data generator. The average voltage at the V-PNM
output is expressed as \(+m(t)\Phi_0 f_{\text{ref}}\), where \(\Phi_0\) is the flux content of an SFQ. The multiplied SFQ pulse train is forwarded to either one of the two input ports of the dual-DFQA (+20-fold or −20-fold). The input port is selected at the Demux. Finally, the dual-DFQA multiplies the voltage by +20 or −20, resulting in the final output voltage of \(+20m(t)\Phi_0 f_{\text{ref}}\) or \(−20m(t)\Phi_0 f_{\text{ref}}\).

2.3 CAD layout and circuit fabrication

We have implemented a 4-bit bipolar SFQ-PFM DAC using the SFQ digital cell library referred to as the CONNECT library [13] and our DFQA library. Test chips were fabricated using a 25-µA/cm² Nb/AlOₓ/Al Josephson integration technology (AIST-STP2).

Fig. 3 shows a photomicrograph of a test circuit. The total number of Josephson junctions is 974. The maximum repetition frequency of the 4-bit V-PNM is designed to be 11.16 GHz. We have prepared two physical layouts for
inductive coupling at the input stage of the −20-fold DFQA, one of which we chose for DAC demonstration.

3 Results and discussion

In measurements, test circuits were cooled at 4.2 K in liquid helium. First, we checked the functions of the V-PNM and dual-DFQA separately, and confirmed their correct operation. Then, we proceeded to test the bipolar DAC operation. We compared the characteristics of two dual-DFQAs and chose a better one having wider input voltage range.

The input signals were generated using a MW generator and a data pattern generator located at room temperature. Synthesized waveforms were monitored on a digital oscilloscope through a differential preamplifier. Fig. 4 shows a synthesized sinusoidal voltage waveform of 1 kHz with a polarity switching signal $I_{PS}$ to the Demux. The reference frequency $f_{ref}$ was set to 460 MHz, while the digital input was updated every 31.25 µs ($\approx 1/32$ kHz). One period of the sinusoidal voltage waveform contained 32 steps of 15 levels, where $m(t)$ was updated as 3, 6, 8, 11, 12, 14, 15, 15, 14, 12, 11, 8, 6, 3, 0, −3, −6, −8, −11, −12, −14, −15, −15, −14, −12, −11, −8, −6, −3, and 0. The output polarity was switched by the $I_{PS}$ at the zero multiplication durations of the V-PNM. The maximum and minimum voltage values for $m(t) = \pm 15$ were $\pm 0.29$ mV, which agreed to the theoretical values.

To evaluate the voltage waveform, Fourier transform analysis was employed for one synthesized period shown in Fig. 4. The power relative to the 1 kHz component is plotted in Fig. 5 with that for a corresponding mathematical model of a stepwise-approximated bipolar sinusoidal waveform. It can be seen that the experimental spectrum agrees well with the mathematical model. For example, the second largest components near 32 kHz, which corresponds to the updating frequency, are $-30$ dB in both experimental and mathematical results.

We also directly measured the positive and negative output voltages for the maximum $m(t)$ of 15 using a digital volt meter (instead of the digital oscilloscope and the differential preamplifier), and compared them with the theoretical values.
The relative errors were 0.11% and 0.08% for the positive and negative outputs, comparable with our previous results [5, 10, 11]. We did not find significant difference in voltage errors for bipolar DAC operation. The operation stability will be evaluated in future work.

**Acknowledgments**

The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2). This work was partially supported by JSPS KAKENHI Grant Number 15K13999, and also by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. The authors thank M. Maezawa for initiation of the present work, and thank M. Tanaka for his valuable advises on circuit design. The authors are also grateful for M. Moriya, Y. Takahashi, Y. Urai, K. Sawada, and other lab members for fruitful discussion and technical supports. The stable supply of liquid helium from the Coordinated Center for UEC Research Facilities is also acknowledged.

(±20m(t)Φ0f_vct). The relative errors were 0.11% and 0.08% for the positive and negative outputs, comparable with our previous results [5, 10, 11]. We did not find significant difference in voltage errors for bipolar DAC operation. The operation stability will be evaluated in future work.

**Acknowledgments**

The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2). This work was partially supported by JSPS KAKENHI Grant Number 15K13999, and also by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. The authors thank M. Maezawa for initiation of the present work, and thank M. Tanaka for his valuable advises on circuit design. The authors are also grateful for M. Moriya, Y. Takahashi, Y. Urai, K. Sawada, and other lab members for fruitful discussion and technical supports. The stable supply of liquid helium from the Coordinated Center for UEC Research Facilities is also acknowledged.

**Acknowledgments**

The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2). This work was partially supported by JSPS KAKENHI Grant Number 15K13999, and also by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. The authors thank M. Maezawa for initiation of the present work, and thank M. Tanaka for his valuable advises on circuit design. The authors are also grateful for M. Moriya, Y. Takahashi, Y. Urai, K. Sawada, and other lab members for fruitful discussion and technical supports. The stable supply of liquid helium from the Coordinated Center for UEC Research Facilities is also acknowledged.

**Acknowledgments**

The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2). This work was partially supported by JSPS KAKENHI Grant Number 15K13999, and also by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. The authors thank M. Maezawa for initiation of the present work, and thank M. Tanaka for his valuable advises on circuit design. The authors are also grateful for M. Moriya, Y. Takahashi, Y. Urai, K. Sawada, and other lab members for fruitful discussion and technical supports. The stable supply of liquid helium from the Coordinated Center for UEC Research Facilities is also acknowledged.

**Acknowledgments**

The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2). This work was partially supported by JSPS KAKENHI Grant Number 15K13999, and also by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. The authors thank M. Maezawa for initiation of the present work, and thank M. Tanaka for his valuable advises on circuit design. The authors are also grateful for M. Moriya, Y. Takahashi, Y. Urai, K. Sawada, and other lab members for fruitful discussion and technical supports. The stable supply of liquid helium from the Coordinated Center for UEC Research Facilities is also acknowledged.

**Acknowledgments**

The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2). This work was partially supported by JSPS KAKENHI Grant Number 15K13999, and also by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. The authors thank M. Maezawa for initiation of the present work, and thank M. Tanaka for his valuable advises on circuit design. The authors are also grateful for M. Moriya, Y. Takahashi, Y. Urai, K. Sawada, and other lab members for fruitful discussion and technical supports. The stable supply of liquid helium from the Coordinated Center for UEC Research Facilities is also acknowledged.

**Acknowledgments**

The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2). This work was partially supported by JSPS KAKENHI Grant Number 15K13999, and also by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. The authors thank M. Maezawa for initiation of the present work, and thank M. Tanaka for his valuable advises on circuit design. The authors are also grateful for M. Moriya, Y. Takahashi, Y. Urai, K. Sawada, and other lab members for fruitful discussion and technical supports. The stable supply of liquid helium from the Coordinated Center for UEC Research Facilities is also acknowledged.