Article

Height Uniformity Simulation and Experimental Study of Electroplating Gold Bump for 2.5D/3D Integrated Packaging

Wenchao Tian 1,*, Zhao Li 1, Yongkun Wang 1 and Guoguang Zhang 2,*

1 School of Electro-Mechanical Engineering, Xidian University, Xi’an 710000, China
2 Foshan Blue Rocket Electronics Co., Ltd., Foshan 528051, China
* Correspondence: wctian@xidian.edu.cn (W.T.); zhangguoguang@fsbrec.com (G.Z.);
Tel.: +86-029-88203040 (W.T.)

Abstract: With the rapid development of nano/micro technology for commercial electronics, the typical interconnection method could not satisfy the high power-density packaging requirement. The 2.5D/3D integrated packaging was seen as a promising technology for nano/micro systems. The gold (Au) bump was the frequently used bonding method for these systems because of its excellent thermal, electric, and mechanical performance. However, relatively little work has been performed to analyze its height uniformity. In this study, the simulation and experimental methods were used to analyze the Au bump height uniformity. Firstly, the electroplating process of Au bump under different flow field parameters was simulated by COMSOL software. The simulated results indicated that the $Au^+$ concentration polarization was the significant reason that caused the non-uniform distribution of Au bump along the wafer radius. Meanwhile, the flow field parameters, such as inlet diameter, inlet flow, titanium (Ti), wire mesh height, and Ti wire mesh density, were optimized, and their values were 20 mm, 20 L/min, 12 mm, and 50%, respectively. Subsequently, the Au bump height uniformity under different current densities was analyzed through an experimental method based on these flow field parameters. The experimental results showed that the increases of current density would decrease the Au bump height uniformity. When the current density was 0.2 A/dm$^2$, the average height, range, and deviance values of Au bump were 9.04 µm, 1.33 µm, and 0.43 µm, respectively, which could reach the requirement of high density and precision for 2.5D/3D integrated packaging.

Keywords: Au bump; electroplating; height uniformity; flow field; electric field

1. Introduction

The synergic progress of nano/micro and electronic technologies are enabling the development of miniaturization, higher efficiency, and higher power-density nano/micro electronic systems [1–5]. Meanwhile, these developments have brought more crucial responsibilities to electronic packaging technology. Over the past few decades, typical wire bonding technologies have been used widely in the electronic industry [6]. However, because of mismatched coefficients of thermal expansion (CTE) between the wires and chips, the interconnection areas easily occurred fatigue failure under the thermal and stress loads [7]. In addition, how to improve the quality of electronic signal transmission was also a significant challenge for wire bonding.

The 2.5D/3D Integrated packaging is seen as an effective technology to satisfy the requirements, e.g., higher input/output (I/O) density, excellent signal integrity, and outstanding heat dissipation, for nano/micro electronic systems [8–11]. The bump, through silicon via (TSV) and redistribution layer (RDL), comprises the essential components for 2.5D/3D integrated devices [12–14]. Among them, the functions of electric conduction, thermal conduction, and mechanical connection between TSV and RDL were realized by bumps. Thus, the reliability of devices must be assured and enhanced in terms of bumps.

Solder bumps and pure metal bumps are the two kinds of typical bumps [15,16]. The main components of solder bumps are Sn-based alloy solder [17–19], such as SnPb bump,
SnAgCu bump, and SnBi bump, etc. However, due to the coarse shape of solder bumps, it is difficult to fabricate finely spaced bumps, which could not satisfy the requirement of high-density packaging. Furthermore, the interfacial intermetallic compounds (IMCs) growing during service and inferior electrical migration resistance of solder joints will affect the reliability and lifetime of electronic facilities [20–22].

Compared with the solder bumps, the pure metal bumps contain a lot of remarkable performances with electronic conductive, thermal conductive, ductility, and restriction electrical migration. Thermocompression and thermosonic are the common bonding method for pure metal bumps [23,24]. The Au bump and copper (Cu) bump are representative pure metal bumps [25,26]. Although the manufacturing price of Cu bumps is lower, the easy oxidation property of Cu is a potential threat to bonding strength because the oxide could improve bonding temperature and hinder the diffusion of Cu atoms [27,28]. Therefore, the oxidation problem should be considered when using the Cu bump.

By contrast, the Au bump obtained more attention from many laboratories and companies because of its outstanding performance, especially for oxidation resistance [29–32]. Sharma [33] et al. studied the influence of Au bump on the thermal performance of flip chip light emitting diodes (FC-LEDs) based on the Finite Element Method. Simulation results indicated that the thermal heat of FC-LEDs is directly proportional to the size of Au bump. Wang [34] et al. researched the influence of Au bump to signal integrity. The double-layer coplanar waveguide (CPW) was connected by Au-Au micro bumps and its S-parameters were tested. Experimental results showed insertion loss values < 0.07 dB at 66 GHz, which expanded the application prospect of Au bump in mm-wave frequencies signal transmission. Wu [35] et al. researched an unbiased estimator to assess and improve the Au bump manufacturing yield more accurately. Meanwhile, they pointed out a shortage of Au bump fabrication, which was usually outsourced to outsourced assembly and testing factories. Thus, researchers must make more efforts to guarantee the quality of Au bump on the forming mechanism. In addition, several studies reported the electroplating parameters influence on the bump morphology [36–41]. The related bump types and electroplating parameters were summarized in the Table 1.

| Bump Types | Electroplating Parameters |
|------------|---------------------------|
|            | Current Density | Electroplating Time | Electroplating Temperature |
| Au-Sn [36] | 0.5 A/dm² | 60 min | 50 °C |
|            | 1 A/dm² | 13 min | 50 °C |
| Sn-Cu [37] | 1–8 A/dm² | 2 h | - |
| Sn-Pb [38] | 6 A/dm² | 3 h | - |
| Sn-Ag [38] | 6 A/dm² | 1 h | - |
| Sn-Bi [39] | 10–30 mA/cm² | - | Room temperature |
| In [40]    | 0.2 mA/cm² | 20 min | Room temperature |
| Cu [41]    | 6 A/dm² | 5 min | - |

The most common fabrication approaches for Au bump are the stud method and the electroplating method [42,43]. Electroplating Au bump was seen as an effective way to assemble high power density devices with simple operation and controllable size. However, few studies have reported the height uniformity of electroplating Au bump. In this study, the height uniformity meant the height difference between Au bumps on the whole wafer surface. The mathematical average height, height range, and height deviance were used together to characterize the Au bump height uniformity. Flow field and electric field are the crucial elements of Au bump quality in the electroplating method. Among them, four main factors of the flow field, such as inlet diameter, inlet flow, Ti wire mesh height, and Ti wire mesh density were considered, and the electric field was controlled by electric density primarily. In this study, simulative and experimental methods were used to obtain the Au
bump. Meanwhile, the influences of these five factors on Au bump height uniformity were investigated, respectively.

2. Simulation and Experimental Methods

Figure 1 shows the structure of Au bump electroplating cup. This kind of electroplating cup could be found in the most of common commercial electroplating equipment. In the process of electroplating Au bump, the wafer was connected with cathodes firstly, and the positions and morphologies of cathodes are shown in Figure 1a. Subsequently, the electroplating bath would enter the inlet and across the Titanium (Ti) alloy wire mesh, and their positions and morphologies are shown in Figure 1b. The Ti wire mesh was connected with anodes. Then, the electroplating bath was sprayed to the wafer surface and deposited Au bump through electrochemical action. Finally, the electroplating bath would outflow from the outlet. The 3D model of the whole electroplating structure is shown in Figure 1c. Figure 1d shows the 2D schematic diagram of electroplating cup, and H and D represent the height of Ti wire mesh and the diameter of inlet, respectively.

![Figure 1](image)

**Figure 1.** Structure of Au bump electroplating cup. (a) Electroplating process without wafer, (b) Empty electroplating cup with Ti wire mesh, (c) 3D model of electroplating structure with wafer, (d) Schematic diagram of electroplating cup.

Metal aluminum (Al) was always selected as the I/O electrode of chips to reduce the fabrication cost. However, due to the disadvantage of Al with easy corrosiveness and difficult connection to Au, the under bump metallurgy (UBM) layer was sputtered or evaporated on the Al electrode as a transition layer. Meanwhile, the Au is the preferred material for the outermost layer to prevent the oxidation of UBM, and the thickness of Au layer was less than 100 nm usually. During the electroplating process, this Au layer connected with the cathode directly and its thickness improved as time increased. Therefore, this thin Au layer was assumed as a shell electrode, which was the electroplating cathode in the flow field simulation. In the electroplating experiment, the UBM layer was composed of the Au layer and TiW layer. Among them, the Au layer with 85 nm acted as the antioxidation and seed layer, the TiW layer with 350 nm between the Au layer, and wafer played the role of adhesion and barrier layer.
In order to enhance the flow field simulation efficiency and speed, other assumptions were made as follows: (1) Au bumps were distributed throughout the whole wafer without clearance; (2) the whole electroplating area was symmetrically distributed; (3) the two-dimensional (2D) rotation model could replace the 3D electroplating area perfectly and (4) the Ti wire mesh was set to an anode. Boundary conditions were set according to the real craft. The 2D rotation cross-section of the flow field simulation model was shown in Figure 2, the red dotted line represented the rotary axis, and the transport field of dilute substrate was used to simulate the transmission of Au+ near the wafer surface.

Considering the practical flow of electroplating bath during electroplating, the turbulence shear stress transport (TSST) model was established. In the actual craft of Au bump manufacture, four significant factors, such as inlet diameter, inlet flow, Ti wire mesh height, and Ti wire mesh density, controlled the distribution of electroplating bath. Among them, the Ti wire mesh density was expressed as a percentage of the Ti metal area to total area. Thus, different parameters of these four factors were set to simulate the fluid flow in the electroplating cup. The COMSOL Multiphysics software was used to simulate the electroplating process and obtain the height of Au bump based on the different flow fields. Table 2 shows the related simulation parameters in the flow field simulation.

Table 2. Flow field simulation parameters of electroplating Au bump.

| Name                                      | Symbol | Value | Unit  |
|-------------------------------------------|--------|-------|-------|
| Au⁺ concentration in electroplating bath  | \( C_0 \) | 50 | mol/m³ |
| Molar mass of deposition (Au)             | \( M \)  | 197 | g/mol |
| Conductivity of cathode (Au)              | \( \sigma_1 \) | 4.52 | S/m |
| Thickness of cathode (Au)                 | \( S \)     | 8.5 × 10⁻⁹ | m   |
| Conductivity of electroplating bath       | \( \sigma_2 \) | 37.5 | S/m |
| Density of electroplating bath            | \( \rho \)   | 1100 | kg/m³ |
| Temperature of electroplating bath        | \( T \)     | 323 | K    |
| Kinematic viscosity of electroplating bath| \( \mu \)   | 0.001 | Pa·s |
| Initial electric potential of anode       | \( \text{Phil} \) | 2 | V |
| Equilibrium electric potential            | \( E_{eq} \) | 1.69 | V |

In addition, the analysis of electric field mainly considered current densities, and the experimental method was adopted to acquire the Au bump under different current densities.
The common commercial fully automatic spraying equipment was used to complete the electroplating Au bump experiment, and the height of Au bump was measured by the wafer probe measurement platform. The morphology of Au bump was observed by the metallographic microscope and scanning electron microscope (SEM).

3. Results and Discussion

3.1. Influence of Flow Field

As mentioned above, the inlet diameter, inlet flow, Ti wire mesh height, and Ti wire mesh density were four significant factors of the flow field. To analyze the influence of different factors on the Au bump uniformity, the measurement method was adopted to acquire the height of Au bump, as shown in Figure 3. In practical production, the wafer diameter was eight inches. Thus, according to the 2D flow field simulation model in Figure 2, the linear measurement method was selected as shown in Figure 3. The measurement points were spaced 10 mm uniformly and eleven points were obtained from the rotary axis to the edge of 2D simulation model.

![Figure 3. Schematic diagram of Au bump height measurement method.](image)

In order to analyze the Au bump height uniformity, the range (R) and deviance (D) were selected to illustrate the uniformity of Au bump height. The calculation of them can be expressed in Equations (1) and (2):

\[
R = h_{\text{max}} - h_{\text{min}} \tag{1}
\]

\[
D = \frac{1}{n} \left( \sum_{i=1}^{n} (h_i - h_{\text{avg}}) \right)^{\frac{1}{2}} \tag{2}
\]

Here, \( h_{\text{max}} \), \( h_{\text{min}} \), and \( h_{\text{avg}} \) are the maximum height, minimum height, and average height of Au bump in measurement points, respectively.

3.1.1. Influence of Inlet Diameter

In this section, the inlet diameters were set to 12 mm, 14 mm, 16 mm, 18 mm, and 20 mm, respectively. In addition, the inlet flow, Ti wire mesh height, and Ti wire mesh density were 26 L/min, 12 mm, and 27%, severally. The simulation time, which is also the electroplating time, was set to 30 min.

The distributions of the Au bump height, Au+ concentration and flow speed under different inlet diameters are shown in Figure 4. Figure 4a shows the distribution of Au bump height along the wafer radius when the inlet diameter is 12 mm. As shown in this figure, the Au bump height increases from 7.874 \( \mu \)m to 9.929 \( \mu \)m when the wafer radius improves from 0 mm to 30 mm. With further extension of the wafer radius, the Au bump height shows a downtrend, and the lower Au bump appears between 80 mm to 100 mm of the wafer radius. The difference of Au+ concentration is seen as the significant reason which causes the Au bump height changes along the wafer radius. Figure 4b shows the Au+ concentration on the wafer surface when the inlet diameter is 12 mm. Within the wafer radius of 10 mm to 50 mm, the Au+ concentration with 60 mol/m3 near the wafer surface is greater than that of the electroplating bath. Compared with this, Au+ concentration at the edge of the wafer is lower than that of the electroplating bath. The changes of Au+ concentration are caused by the flow speed on the wafer surface. The flow speed distribution on the wafer surface at different inlet diameters is shown in Figure 4c. The flow speed exceeds 0.4 m/s at the wafer radius of 10 mm to 50 mm. The stronger convection...
improves the Au+ concentration, thus the higher Au bump occurs in this area. In contrast, the slower flow speed within the wafer radius of 80 mm to 100 mm decreases the Au+ concentration and Au bump height.
3.1.2. Influence of Inlet Flow

As discussed in Section 3.1.1, the inlet diameter with 20 mm possessed the optimal Au bump uniformity. Therefore, in the simulation of inlet flow, the inlet diameter was set as 20 mm, and the inlet flows were set as 20 L/min, 26 L/min, 30 L/min, 35 L/min, and 40 L/min, respectively. The other simulation parameters were the same as before.

Figure 6 shows the distributions of the Au bump height, Au+ concentration, and flow speed under different inlet flows. Figure 6a shows the Au bump height along the wafer radius, as the inlet flow is 40 L/min. The distribution trend is similar with Figure 5a. In the above discussion, the concentration polarization of Au+ was caused by different flow speeds on the wafer surface, thus the Au bump height appears different along the wafer radius. The Au+ distribution on the wafer surface in Figure 6b exhibits the concentration polarization phenomenon caused by the difference of flow speed when the inlet flow is 40 L/min. The flow speed along the wafer surface under different inlet flows is shown in Figure 6c. In this figure, when the inlet flow increases from 20 L/min to 40 L/min, the maximum value of flow speed improves from 0.172 m/s to 0.552 m/s. Meanwhile, the distribution of flow speed becomes more uneven.

Figure 7 shows the influence of different inlet flows on the Au bump uniformity. As shown in Figure 7a,b, the alter of inlet flow has limited influence on the Au bump height and range. As the inlet flow enhances from 20 L/min to 40 L/min, the values of Au bump height and range are 8.65 ± 0.10 µm and 2.55 ± 0.05 µm, respectively. In contrast, the Au bump height deviance in Figure 7c possesses volatility with the increase of inlet flow. The main reason caused this phenomenon is the difference of flow fields under different inlet flows. The deviance value of Au bump height improves from 0.803 µm to 0.920 µm when the inlet flow ranges from 20 L/min to 30 L/min. Then, the Au bump height deviance value increases slowly by magnifying the inlet flow.
Figure 6. Distributions of the Au bump height, Au+ concentration and flow speed. (a) Au bump height distribution along the wafer radius (inlet flow is 40 L/min), (b) Au+ concentration distribution on the wafer surface (inlet flow is 40 L/min), and (c) flow speed distribution on the wafer surface at different inlet flows.

Figure 7. Au bump height and uniformity under different inlet flows. (a) Au bump height, (b) Au bump range, and (c) Au bump deviance.

3.1.3. Influence of Ti Wire Mesh Height

According to the analysis in Sections 3.1.1 and 3.1.2, when the inlet diameter and flow are 20 mm and 20 L/min, respectively, a better Au bump height uniformity could be acquired. Thus, in the simulation of Ti wire mesh height, their parameters were selected. Moreover, the Ti wire mesh heights were selected as 12 mm, 20 mm, 30 mm, 40 mm, 50 mm, and 80 mm, severally. The Ti wire mesh density was 27%, as mentioned above. Figure 8 shows the distributions of the Au bump height, Au+ concentration, and flow speed under different Ti wire mesh heights. The Au bump height and Au+ concentration distribution along the wafer radius are shown in Figure 8a,b, respectively. In these figures, the distribution of Au bump height and Au+ concentration has satisfactory consistency, as discussed in the previous two sections. Figure 8c is the flow speed distribution on the wafer surface at different Ti wire mesh heights. As shown in this figure, the restricted variety of flow speed occurs with the changes of Ti wire mesh height. When the Ti wire mesh height increases from 12 mm to 80 mm, the maximum value of flow speed decreases from 0.293 m/s to 0.278 m/s, which fell by only 5.1%.
3.1.3. Influence of Ti Wire Mesh Height

According to the analysis in Sections 3.1.1 and 3.1.2, when the inlet diameter and flow are 20 mm and 20 L/min, respectively, a better Au bump height uniformity could be acquired. Thus, in the simulation of Ti wire mesh height, their parameters were selected. Moreover, the Ti wire mesh heights were selected as 12 mm, 20 mm, 30 mm, 40 mm, 50 mm, and 80 mm, severally. The Ti wire mesh density was 27%, as mentioned above.

Figure 8 shows the distributions of the Au bump height, Au+ concentration, and flow speed under different Ti wire mesh heights. The Au bump height and Au+ concentration distribution along the wafer radius are shown in Figure 8a,b, respectively. In these figures, the distribution of Au bump height and Au+ concentration has satisfactory consistency, as discussed in the previous two sections. Figure 8c is the flow speed distribution on the wafer surface at different Ti wire mesh heights. As shown in this figure, the restricted variety of flow speed occurs with the changes of Ti wire mesh height. When the Ti wire mesh height increases from 12 mm to 80 mm, the maximum value of flow speed decreases from 0.293 m/s to 0.278 m/s, which fell by only 5.1%.

Figure 8. Distributions of the Au bump height, Au+ concentration, and flow speed. (a) Au bump height distribution along the wafer radius (Ti wire mesh height is 12 mm), (b) Au+ concentration distribution on the wafer surface (Ti wire mesh height is 12 mm), and (c) flow speed distribution on the wafer surface at different Ti wire mesh heights.

Figure 9 shows the Au bump height and uniformity under different Ti wire mesh heights. As shown in Figure 9a,b, the Au bump height and range are $8.70 \pm 0.10 \mu m$ and $2.53 \pm 0.03 \mu m$, respectively. The non-obvious vibration of their value indicates that the limited influence occurs when the Ti wire mesh height increases from 12 mm to 80 mm. However, the deviance of Au bump height in Figure 9c shows a rising trend with the enhancement of Ti wire mesh height. The deviance value of Au bump height improves from $0.803 \mu m$ to $0.816 \mu m$ as the Ti wire mesh height enhances from 12 mm to 50 mm. Further rising the Ti wire mesh height to 80 mm, this value reaches $0.925 \mu m$. In the electroplating process, the electroplating bath enters the cup from the inlet and then through...
the Ti wire mesh. Here, the Ti wire mesh is a rectifier for the whole electroplating model. Thus, the lower height of Ti wire mesh could rectify the electroplating bath preferably and the flow field would be more uniform in this situation. This phenomenon suggests that the opportune reduction of Ti wire mesh height is beneficial to enhance the Au bump height uniformity.

Figure 9. Au bump height and uniformity under different Ti wire mesh heights. (a) Au bump height, (b) Au bump range, and (c) Au bump deviance.

3.1.4. Influence of Ti Wire Mesh Density

As described in the three sections above, the Au bump possessing the preferable height uniformity as inlet diameter, inlet flow, and Ti wire mesh height are 20 mm, 20 L/min, and 12 mm, respectively. In order to obtain a more uniform Au bump, these parameters were chosen in this section and the Ti wire mesh densities were set to 5%, 10%, 20%, 27%, 40%, and 50%.

Figure 10 shows the distributions of Au bump height, Au+ concentration, and flow speed under different Ti wire mesh densities. As shown in Figure 10a,b, the distributions of Au bump height and Au+ concentration along the wafer radius are similar to the previous three sections. Furthermore, according to Figures 4a, 6a, 8a and 10a, the poor height uniformity of Au bump occurs as the electroplating time improves. Figure 10c shows the flow speed distribution on the wafer surface at different Ti wire mesh densities. In this figure, the flow speed shows a downtrend as the improves of Ti wire mesh density. The maximum flow speed decreases from 0.346 m/s to 0.135 m/s as the Ti wire mesh density increases from 5% to 50%. It suggests that the rectifying effect of Ti wire mesh on electroplating bath would become better, and the flow field is more uniform with the increases of Ti wire mesh density.
Figure 10. Distributions of the Au bump height, Au+ concentration, and flow speed. (a) Au bump height distribution along the wafer radius (Ti wire mesh density is 5%), (b) Au+ concentration distribution on the wafer surface (Ti wire mesh density is 5%), and (c) flow speed distribution on the wafer surface at different Ti wire mesh densities.

Figure 11 shows the influence of different Ti wire mesh densities on the Au bump height and uniformity. The Au bump height with 8.70 ± 0.02 μm is shown in Figure 11a. The changes of Ti wire mesh density have a finite effect on the Au bump height. Figure 11b,c show the Au bump height range and deviance, respectively. As shown in these figures, the height range and deviance of Au bump decrease with the increases of Ti wire mesh density. When the Ti wire mesh density improves from 5% and 27%, the value of height range descends from 2.722 μm to 2.192 μm and the height deviance value declines from 0.884 μm to 0.620 μm. As mentioned before, the Ti wire mesh is a rectifier for the electroplating model. As other parameters were fixed, the higher density of Ti wire mesh would enhance the uniformity of flow field. Thus, the uniformity of Au bump height improves as the density of Ti wire mesh increases.
3.2. Influence of Electric Field

In this section, the influences of different current densities on the Au bump height uniformity were analyzed through an experiment. The electroplating flow field parameters were optimized through simulation in Section 3.1 and used in the experiment. Here, the inlet diameter, inlet flow, Ti wire mesh height, and Ti wire mesh density were set as 20 mm, 20 L/min, 12 mm, and 50%. In addition, the current densities were selected to 0.2 A/dm², 0.3 A/dm², 0.4 A/dm², 0.5 A/dm², 0.6 A/dm², and 0.8 A/dm², respectively.

Figure 12 shows the experimental results of different current densities influences on the Au bump height and uniformity. In order to obtain the Au bump height on the surface of wafer, thirteen test points were chosen, and the distribution diagram of them is shown in Figure 12a. The Au bump height with $8.95 \pm 0.10 \mu m$ in Figure 12b indicates that the limited influence occurs on the Au bump height as the changes of current density. Figure 12c,d show the height range and deviance under different current densities in the experiment. In these figures, the height range and deviance enhance from $1.32 \mu m$ and $0.43 \mu m$ to $1.88 \mu m$ and $0.60 \mu m$, with the current density increasing from $0.2 A/dm^2$ to $0.8 A/dm^2$, respectively. The experiment result demonstrates that the Au bump height uniformity would enhance with the decreases of current density. In addition, the smaller values of Au bump height range and deviance indicate that the simulation is an effective method to optimize the electroplating process.

Figure 13 shows the morphology of Au bump fabricated in the experiment. Figure 13a,b show the photoresist burning and void defects during the Au bump fabrication, respectively. The top view of optimized Au bump is shown in Figure 13c. In this figure, the length and width of Au bump are 40 \(\mu m\) and 20 \(\mu m\), respectively. In addition, the space between two Au bumps is 10 \(\mu m\). Meanwhile, obvious voids or gaps could not be observed on the Au bump surface. Thus, the high-quality Au bump with satisfying uniformity can be obtained through experiment. Figure 13d shows the SEM cross-section view of Au bump. The Au bump with 9.02 \(\mu m\) height is electroplated on the wafer. The bright line between Au
bump and wafer represents the UBM layer. The Au bump appears saddle-shaped, which means low in the middle and high on all sides. According to the study of Li et al. [44], the current crowding effect was seen as the significant reason caused this profile. Luo et al. [45] proposed active-area density model to explain the current crowding effect in their study. According to this model, regions that are more densely populated with photoresist tend to attract a high current density, and hence the current crowding effect would appear. As the electroplating is proportional to the current density, a thicker film is deposited on the edge of a wide structure due to the increased current density, whereas the middle of the structure is thinner. They also found that the current crowding should always exist for patterned wafer plating. The study of Wu [35] et al. also demonstrated the existence of this Au bump morphology.

Figure 12. Influence of current density on the Au bump height uniformity in experiment. (a) Schematic diagram of test points distribution on the wafer, (b) Au bump height, (c) Au bump range, and (d) Au bump deviance.

Figure 14 shows the Au bumps distribution on the whole wafer surface. As shown in the figure, the total numbers of Au bumps are 216. The maximum height value of Au bump is 11.38 µm, and the minimum height value is 8.82 µm. To intuitively investigate Au bump height variation on the whole wafer surface, the statistical data of Au bump height is shown in Table 3. In this table, the total number of Au bumps in the 8~9 µm and 11~12 µm height interval is 6, which only accounts for 2.78% of all Au bumps. It is meaningless to analyze Au bump height uniformity with fewer height samples. Thus, the height uniformity of these Au bumps was ignored. In contrast, 83.33% Au bumps were at the 9~10 µm height interval. The number, average height, height range, and height deviance of them are 180, 9.61 µm, 0.97 µm, and 0.20 µm, respectively. Meanwhile, there are 13.89% Au bumps at the 9~10 µm height interval, The number, average height, height range, and height deviance of them are 30, 10.28 µm, 0.87 µm, and 0.26 µm, respectively.
Figure 13. Morphology of Au bump. (a) Photoresist burning, (b) Void, (c) Top view of optimized Au bump, (d) Cross-section view of optimized Au bump.

Figure 14. Au bump distribution on the whole wafer surface.
Table 3. Au bump height statistical data.

| height Interval (µm) | 8–9 | 9–10 | 10–11 | 11–12 |
|----------------------|-----|------|-------|-------|
| numbers              | 3   | 180  | 30    | 3     |
| average (µm)         | -   | 9.61 | 10.28 | -     |
| range (µm)           | -   | 0.97 | 0.87  | -     |
| deviance (µm)        | -   | 0.20 | 0.26  | -     |

4. Conclusions

In this study, the simulation and experimental methods were used to fabricate the Au bump and analyze its height uniformity. Four significant flow field parameters, with inlet diameter, inlet flow, titanium (Ti) wire mesh height, and Ti wire mesh density, were optimized by the COMSOL software, and their values were 20 mm, 20 L/min, 12 mm, and 50%, respectively. The simulation results indicated that the Au⁺ concentration polarization was considered as the main reason that caused the non-uniform distribution of Au bump height along the wafer radius. The inlet diameter and Ti wire mesh density were positively associated with the Au bump height uniformity. In contrast, the decrease of inlet flow and Ti wire mesh height would improve the height uniformity of Au bump. Based on the optimized flow field parameters, the different current densities were set to fabricate the Au bump during the experimental method. The results indicated that the increases of current density would decrease the Au bump height uniformity. The high-precision Au bump with 1.33 µm height range and 0.43 µm height deviance was obtained when the current density was 0.2 A/dm². Thus, the optimized flow field parameters by simulation were effective in fabricating the high-quality Au bump. In addition, the changes of flow field and electric field parameters had limited influence on the Au bump height.

Author Contributions: W.T. designed and guided complete related simulation and experiment. Z.L. wrote this paper. Y.W. offered the help of modify grammar. G.Z. guided related experiment. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Natural Science Foundation of China (No. 52106108), and the Natural Science Foundation of Shaanxi Province (No. 2019JM-257).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Hu, H.W.; Chen, K.N. Development of Low Temperature Cu-Cu Bonding and Hybrid Bonding for Three-Dimensional Integrated Circuits (3D IC). Microelectron. Reliab. 2021, 127, 114412. [CrossRef]
2. Kabir, A.M.D.; Peng, Y. Holistic Chiplet-Package Co-Optimization for Agile Custom 2.5-D Design. IEEE Trans. Compon. Packag. Manuf. Technol. 2021, 11, 715–726. [CrossRef]
3. Pu, J.; Wang, X.; Xu, R.; Xu, S.; Komvopoulos, K. Highly Flexible, Foldable, and Rollable Microsupercapacitors on an Ultrathin Polyimide Substrate with High Power Density. Microsyst. Nanoeng. 2018, 4, 16. [CrossRef] [PubMed]
4. Lee, H.; Smet, V.; Tummala, R. A Review of SiC Power Module Packaging Technologies: Challenges, Advances, and Emerging Issues. IEEE J. Emerg. Sel. Top. Power Electron. 2020, 8, 239–255. [CrossRef]
5. Ding, C.; Liu, H.; Ngo, D.T.K.; Burgos, R.; Lu, G.Q. A Double-Side Cooled SiC MOSFET Power Module with Sintered-Silver Interposers: I-Design, Simulation, Fabrication, and Performance Characterization. IEEE Trans. Power Electron. 2021, 36, 11672–11680. [CrossRef]
6. Liu, P.; Tong, L.; Wang, J.; Shi, L.; Tang, H. Challenges and Developments of Copper Wire Bonding Technology. Microelectron. Reliab. 2012, 52, 1092–1098. [CrossRef]
7. Liu, W.; Mei, Y.; Xie, Y.; Wang, M.; Li, X.; Lu, G.Q. Design and Characterizations of a Planar Multichip Half-Bridge Power Module by Pressureless Sintering of Nanosilver Paste. IEEE J. Emerg. Sel. Top. Power Electron. 2019, 7, 1627–1636. [CrossRef]
8. Fang, J.W.; Chang, Y.W. Area-I/O Flip-Chip Routing for Chip-Package Co-Design Considering Signal Skews. *IEEE Trans. Comput. Aid. Des.* 2010, 29, 711–721. [CrossRef]

9. Kam, D.G. Optimization of Flip-Chip Transitions for 60-GHz Packages. *IEEE Electr. Express* 2014, 11, 20140256. [CrossRef]

10. Wu, P.C.; Ou, S.L.; Horng, R.H.; Wu, D.S. Improved Performance and Heat Dissipation of Flip-Chip White High-Voltage Light Emitting Diodes. *IEEE Trans. Device Mater. Reliab.* 2017, 17, 197–203. [CrossRef]

11. Wu, D.; Tian, W.; Wang, C.; Huo, R.; Wang, Y. Research of Wafer Level Bonding Process Based on Cu-Sn Eutectic. *Micromachines* 2020, 11, 789. [CrossRef]

12. Yang, T.F.; Kao, K.S.; Cheng, R.C.; Chang, J.Y.; Zhan, C.J. Evaluation of Cu/SnAg Microbump Bonding Processes for 3D Integration Using Wafer-Level Underfill Film. *Solder. Surf. Mt. Technol.* 2012, 24, 287–293. [CrossRef]

13. Sun, Y.; Luo, J.; Ding, G. Modeling and Analysis of TSV Arrays with Different Ground and Signal Distributions in 2.5D/3D Integration Systems. *J. Phys. Conf. Ser.* 2016, 81, 143–149. [CrossRef]

14. Lau, J.; Tzeng, P.; Lee, C.; Zhan, C.; Li, M.; Cline, J.; Saito, K.; Hsin, Y.; Chang, P.; Chang, Y.; et al. Redistribution layers (RDLs) for 2.5 D/3D IC integration. *Int. Symp. Microelectron.* 2013, 2013, 09034–09041. [CrossRef]

15. Zhang, R.; Meyer, B.H.; Wang, K.; Stan, M.R.; Skadron, K. Tolerating the Consequences of Multiple EM-Induced C4 Bump Failures. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* 2016, 24, 2335–2344. [CrossRef]

16. Noma, H.; Oyama, Y.; Nishiwaki, H.; Takami, M.; Takatani, T.; Toriyama, K.; Orii, Y. Wettability and Reliability for Double-Sided Assembly with Chip Connection (C2) Flip-Chip Technology. *Trans. Ipn. Inst. Electron. Packag.* 2009, 2, 85–90. [CrossRef]

17. Chiu, Y.T.; Lin, K.L.; Lai, Y.S. Dissolution of Sn in a SnPb Solder Bump under Current Stressing. *J. Appl. Phys.* 2012, 111, 043517. [CrossRef]

18. Chen, P.; Zhao, X.C.; Liu, Y.; Li, H.; Wang, Y. Aging Resistance and Mechanical Properties of Sn3.0Ag0.5Cu Solder Bump Joints with Different Bump Shapes. *Rare Met.* 2021, 40, 225–230. [CrossRef]

19. Song, R.W.; Fleschman, C.J.; Wang, Y.C.; Tsai, S.Y.; Duh, J.G. IMC Suppression and Phase Stabilization of Cu/Sn-Bi/Cu Microbump via Zn Doping. *Mater. Lett.* 2021, 282, 128735. [CrossRef]

20. Zhang, H.; Liu, Y.; Wang, L.; Fan, J.; Fan, X.; Sun, F.; Zhang, G. A New Hermetic Sealing Method for Ceramic Packaging using Nanosilver Sintering Technology. *Microelectron. Reliab.* 2018, 81, 143–149. [CrossRef]

21. Liu, Y.; Zhang, H.; Wang, L.; Fan, X.; Zhang, G.; Sun, F. Stress Analysis of Pressure-Assisted Sintering for the Double-Side Assembly of Power Module. *Solder. Surf. Mt. Technol.* 2019, 31, 20–27. [CrossRef]

22. Liu, Y.; Li, Z.; Zheng, H.; Xue, Y.; Zhou, M.; Cao, R.; Chen, P.; Zeng, X. Plasticity Enhancement of Nano-Ag Sintered Joint based on Metal Foam. *J. Mater. Sci. Mater. Electron.* 2021, 32, 7187–7197. [CrossRef]

23. Li, J.; Zhang, Y.; Zhang, H.; Chen, Z.; Zhou, G.; Liu, X.; Zhu, W. The Thermal Cycling Reliability of Copper Pillar Solder Bump in Flip Chip via Thermal Compression Bonding. *Microelectron. Reliab.* 2020, 104, 113543. [CrossRef]

24. Wang, F.; Han, L. Experimental Study of Thermosonic Gold Bump Flip-Chip Bonding with a Smooth End Tool. *IEEE Trans. Compoo. Packag. Manuf. Technol.* 2013, 3, 930–934. [CrossRef]

25. Pai, R.S.; Crain, M.M.; Walsh, K.M. Maskless Shaping of Gold Stud Bumps as High Aspect Ratio Microstructures. *Microelectron. Eng.* 2011, 88, 135–139. [CrossRef]

26. Hwang, Y.M.; Pan, C.T.; Chen, B.S.; Jian, S.R. Numerical Analysis of the Welding Behaviors in Micro-Copper Bumps. *Metals* 2021, 11, 460. [CrossRef]

27. Liu, J.; Chen, H.; Ji, H.; Li, M. Highly Conductive Cu-Cu Joint Formation by Low-Temperature Sintering of Formic Acid-Treated Cu Nanoparticles. *ACS Appl. Mater. Inter.* 2016, 8, 33289–33298. [CrossRef]

28. Ren, H.; Wu, F.; Shin, S.; Liu, L.; Zou, G.; Suga, T. Low Temperature Cu Bonding with Large Tolerance of Surface Oxidation. *AIP Adv.* 2019, 9, 055127. [CrossRef]

29. Oppermann, H.; Dietrich, L. Nanoporous Gold Bumps for Low Temperature Bonding. *Microelectron. Reliab.* 2012, 52, 356–360. [CrossRef]

30. Föhlich, J.; Dietrich, L.; Oppermann, H.; Lang, K.D. Surface Treatment of Gold Bumps for Thermocompression Bonding with Low Temperature and Low Pressure. In Proceedings of the 2018 7th Electronic System-Integration Technology Conference (ESTC), Dresden, Germany, 18–21 September 2018; pp. 1–5. [CrossRef]

31. Antelius, M.; Fischer, A.C.; Roxhed, N.; Stemme, G.; Niklaus, F. Room-Temperature Wafer-Level Vacuum Sealing by Compression of High-Speed Wire Bonded Gold Bumps. In Proceedings of the 2011 16th International Solid-State Sensors, Actuators and Microsystems Conference, Beijing, China, 5–9 June 2011; pp. 1360–1363. [CrossRef]

32. Tanida, K.; Umemoto, M.; Tomita, Y.; Tago, M.; Kajiwara, R.; Akiyama, Y.; Takahashi, K. Au Bump Interconnection with Ultrasonic Flip-Chip Bonding in 20 μm Pitch. *Jpn. J. Phys.* 2003, 42, 2198–2203. [CrossRef]

33. Sharma, M.; Pandey, D.; Kshosla, D.; Goyal, S.; Pandey, B.K.; Gupta, A.K. Design of a GaN-Based Flip Chip Light Emitting Diode (FC-LED) with Au Bumps & Thermal Analysis with Different Sizes and Adhesive Materials for Performance Considerations. *Silicon* 2022, 14, 7109–7120. [CrossRef]

34. Wang, M.; Dai, J.; Wang, F.; Kong, Y. Research on Au/Au Micro-Bump Bonding for Millimeter Wave Frequencies Heterogeneous Integration. In Proceedings of the 2021 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP), Chongqing, China, 15–17 November 2021; pp. 148–150. [CrossRef]

35. Wu, C.H.; Pearson, W.L.; Tai, Y.T. An Improved Manufacturing Yield Measure for Gold Bumping Processes with Very Low Nonconformities. *IEEE Trans. Compon. Packag. Manuf. Technol.* 2019, 9, 991–997. [CrossRef]
36. Yoon, J.; Chun, H.; Jung, S. Reliability Evaluation of Au-20Sn Flip Chip Solder Bump Fabricated by Sequential Electroplating Method with Sn and Au. *Mat. Sci. Eng. A* 2008, 473, 119–125. [CrossRef]

37. Jung, S.W.; Jung, J.P.; Zhou, Y. Characteristics of Sn-Cu Solder Bump Formed by Electroplating for Flip Chip. *IEEE Trans. Electron. Packag. Manuf.* 2006, 29, 10–16. [CrossRef]

38. Hwang, H.; Hong, S.; Jung, J.; Kang, C. Pb-free Solder Bumping for Flip Chip Package by Electroplating. *Solder. Surf. Mt. Technol.* 2003, 15, 10–16. [CrossRef]

39. Goh, Y.; Haseeb, A.S.M.A.; Sabri, M.F.M. Effects of Hydroquinone and Gelatin on the Electrodeposition of Sn-Bi Low Temperature Pb-free Solder. *Electrochim. Acta* 2013, 90, 265–273. [CrossRef]

40. Cicero, U.L.; Arnone, C.; Barbera, M.; Collura, A.; Lullo, G. Electroplated Indium Bumps as Thermal and Electrical Connections of NTD-Ge Sensors for the Fabrication of Microcalorimeter Arrays. *J. Low Temp. Phys.* 2012, 167, 535–540. [CrossRef]

41. Tsai, Y.; Hu, H.; Chen, K. Low Temperature Copper-Copper Bonding of Non-Planarized Copper Pillar with Passivation. *IEEE Electron. Device Lett.* 2020, 41, 1229–1232. [CrossRef]

42. Neher, C.; Lander, R.L.; Moskalova, A.; Pasner, J.; Tripathi, M.; Woods, M. Further Developments in Gold-Stud Bump Bonding. *J. Instrum.* 2012, 7, C02005. [CrossRef]

43. Dimitrijevic, S.; Rajčić-Vujasinović, M.; Trujic, V. Non-Cyanide Electrolytes for Gold Plating—A Review. *Int. J. Electrochem. Sci.* 2013, 8, 6620–6646.

44. Li, J.D.; Zhang, P.; Wu, Y.H.; Liu, Y.S.; Xuan, M. Uniformity Study of Nickel Thin-Film Microstructure Deposited by Electroplating. *Microsyst. Technol.* 2009, 15, 505–510. [CrossRef]

45. Luo, J.K.; Chu, D.P.; Flewitt, A.J.; Spearing, S.M.; Fleck, N.A.; Milne, W.I. Uniformity Control of Ni Thin-Film Microstructures Deposited by Through-Mask Plating. *J. Electrochem. Soc.* 2005, 152, C36–C41. [CrossRef]