Toward Terabits-per-second Communications: Low-Complexity Parallel Decoding of $G_N$-Coset Codes

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Abstract—Recently, a parallel decoding framework of $G_N$-coset codes was proposed. High throughput is achieved by decoding the independent component polar codes in parallel. Various algorithms can be employed to decode these component codes, enabling a flexible throughput-performance tradeoff. In this work, we adopt SC as the component decoders to achieve the highest-throughput end of the tradeoff. The benefits over soft-output component decoders are reduced complexity and simpler (binary) interconnections among component decoders. To reduce performance degradation, we integrate an error detector and a log-likelihood ratio (LLR) generator into each component decoder. The LLR generator, specifically the damping factors therein, is designed by a genetic algorithm. This low-complexity design can achieve an area efficiency of 533Gbps/mm² under 7nm technology.

I. INTRODUCTION

A. $G_N$-coset codes

$G_N$-coset codes, defined by Arıkan in [1], are a class of linear block codes with the generator matrix $G_N$. $G_N$ is an $N \times N$ binary matrix defined as

$$G_N \triangleq F^\otimes n,$$  \hspace{1cm}(1)

in which $N = 2^n$ and $F^\otimes n$ denotes the $n$-th Kronecker power of $F = \begin{bmatrix} 1 & 0 \end{bmatrix}$.

The encoding process is

$$x_1^N = u_1^N G_N,$$  \hspace{1cm}(2)

where $x_1^N \triangleq \{x_1, x_2, \cdots, x_N\}$ and $u_1^N \triangleq \{u_1, u_2, \cdots, u_N\}$ denote the code bit sequence and the information bit sequence, respectively.

An $(N, K)$ $G_N$-coset code [1] is defined by an information set $\mathcal{A} \subset \{1, 2, \cdots, N\}$, $|\mathcal{A}| = K$. Its generator matrix $G_N(\mathcal{A})$ is composed of the rows indexed by $\mathcal{A}$ in $G_N$. Thus (2) is rewritten as

$$x_1^N = u(\mathcal{A}) G_N(\mathcal{A}),$$  \hspace{1cm}(3)

where $u(\mathcal{A}) \triangleq \{u_i | i \in \mathcal{A}\}$.

The key to constructing $G_N$-coset codes is to properly determine an information set $\mathcal{A}$. RM codes [2] and polar codes [11] are two well-known examples of $G_N$-coset codes. They determine $\mathcal{A}$ according to Hamming weight and sub-channel reliability, respectively.

Recently, a parallel decoding framework of $G_N$-coset codes is proposed in [3]. As shown in Fig. 1(a), the encoding process of $G_N$-coset codes can be described by an $n$-stage encoding graph. The former and latter stages respectively correspond to outer and inner codes. The inner codes are independent component codes that can be decoded in parallel [3].

This parallel framework first produces equivalent encoding/decoding graphs by permuting the inner and outer parts of the original decoding graph $\mathcal{G}$ (see Fig. 1). During decoding, we only process the inner code parts of these equivalent graphs, leaving the outer codes unprocessed. The LLRs from different graphs about the same code bit are exchanged iteratively to reach a consensus. Since all inner codes are decoded in parallel, this decoding framework supports a very high...
degree of parallelism. The code construction under the parallel decoding algorithm is different from polar/RM codes, and is studied separately in [3].

B. Motivations and Contributions

This paper mainly focuses on further enhancing decoding throughput. The aforementioned iterative LLR exchange procedure requires soft-output component decoders such as SCL and SCAN to provide extrinsic LLRs [3]. But if we aim at an ultra-high-throughput decoder, implementing soft-output component decoders gives rise to two problems. First, the area efficiency of SCL and SCAN is much lower than fast-SC. Second, the interconnections among the large number of component decoders consume considerable chip area.

To alleviate both problems, we propose to adopt hard-output SC as the component decoder. First, the complexity and storage are reduced within each component decoder. Compared with SCAN on one iteration, SC has 1/4 decoding complexity and 1/2 storage. Compared with soft-output SCL with list size 8, SC has 1/16 decoding complexity and 1/8 storage [5]. Second, the interconnections among component decoders are also reduced. Compared with soft-output decoders, hard-output SC decoders significantly simplifies routing because only hard bits are propagated among component decoders.

Besides, we introduce an error detector before each SC decoder to opportunistically reduce computation. If no error is detected, we skip the SC decoding and directly output the hard decisions.

To minimize the performance loss due to the above simplifications, we propose a genetic algorithm based LLR generator. LLR input (for this iteration) is generated from SC decoding output (from previous iterations) via a set of damping factors to determine the amplitudes. The damping factors have a significant impact on the decoding performance, and is “learned” offline through a genetic algorithm based on unsupervised learning. Compared with “hand-picked” parameters based on greedy stepwise optimization, the proposed genetic algorithm exhibits better performance.

II. STAGE PERMUTED PARALLEL DECODING

$G_N$-coset codes [3] natively support parallel decoding, as the inner codes are independent. To decode these component codes, various soft-output decoders, e.g., SCL, SC permutation list and SCAN, are employed [3]. In this work, we propose hard-output SC decoders to achieve higher area efficiency.

A. Parallel decoding framework

The parallel decoding framework in [3] is modified to support SC component decoders. In Algorithm 1, a $G_N$-coset code is alternately decoded on two factor graphs $G$ and $G_x$, as shown in Fig. [11]. The stage permuted graph $G_x$ is generated by swapping the inner codes and outer codes in $G$. Only the inner codes of each graph $\Lambda \in \{G, G_x\}$ are decoded. And their decoding outputs are exchanged between the decoding graphs. The $\sqrt{N}$ component decoders can be implemented in parallel.

Now that we use SC to decode the component codes, the hard output must be converted into soft LLR as input for the next iteration. Therefore, an LLR generator is placed before the SC decoder (line 8). Meanwhile, an error detector is placed before the LLR generator (line 6).

For decoding graph $G$ (resp. $G_x$), the $j$-th code bit of the $i$-th inner component code is denoted by $x(i,j)$ (resp. $x(x(j,i))$). Take graph $G$ for example, the hard outputs (HO) from different component decoders of the previous iteration are combined into $\hat{x}_{\pi,i,j}^t$ and then sent for error detection (line 6).

- If no error is detected, i.e., the error detection output (E) $e_i = 0$, then $\hat{x}_{\pi,i,j}^t$ are directly taken as the new “HO” result of this iteration (line 8), and SC decoding is skipped.
- Otherwise, if $e_i = 1$, the LLR of code bit $x(i,j)$ in the $t$-th iteration, denoted by $L_{i,j}^t$, is generated from channel LLR $L_{ch,j+i+(j-1)\sqrt{N}}$ and previous “HO&E” results (line 10). The generated LLRs are decoded by SC to output new “HO” results (line 11).

Either way, new “HO&E” results are sent to the next iteration. After $t_{max}$ iterations, the algorithm outputs the estimated codeword of the last decoding iteration as results.
B. SC as component decoder

A component decoder consists of three parts, an error detector, an LLR generator and an SC decoder (see Fig. 2). An SC decoder takes soft LLR input but generates hard bits output. The mismatch between hard output and soft input poses a challenge for iterative decoding, as the hard output cannot be directly used as soft input for the next iteration. To solve this problem, an LLR generator is required to generate soft values from the hard output.

An error detector is placed before the LLR generator and it serves two purposes. First, if its input vector (i.e., HO from the previous iteration) is a codeword (no error detected), LLR generation and SC decoding can be skipped to save computation. Second, it provides a way to estimate the reliability of hard bits. Heuristically, if an input vector is already a codeword, they are deemed more reliable. Otherwise, if error detection failed, there is a chance that the error cannot be corrected by an SC decoder, which implies less reliability. Therefore, error detection results facilitate the “recovery” of soft LLRs for the next iteration.

In practice, an error detector based on syndrome check can be implemented by reusing the encoding circuit. It costs almost no additional hardware resource.

The LLR generator is activated when an error detection fails. It takes four inputs (i) the channel LLR, (ii,iii) the hard outputs of the previous two iterations, and (iv) the error detection output of the previous iteration.

Take the non-permuted graph $\mathcal{G}$ for example. For code bit $x_{i,j}$, its input LLR is generated based on the previous-iteration error detection output $e_{\pi,j} \in \{0, 1\}$.

If $e_{\pi,j} = 1$, meaning error detection failed and hard output is from an SC decoder, the input LLR is the sum of channel LLR and hard outputs from the previous two iterations:

$$L_{i,j}^t = L_{e,h,i+(j-1)} \sqrt{N} + \frac{2\alpha_t}{\sigma^2} (1 - 2^{\tau_{-1}}) \frac{2\beta_t}{\sigma^2} (1 - 2^{\tau_{-2}}),$$ (4)

where $\alpha_t$ and $\beta_t$ respectively denote the damping factors, which determine the amplitude.

If $e_{\pi,j} = 0$, meaning hard output is directly from an error detector since no error was found, the input LLR is the sum of the channel LLR and hard output from the previous iteration:

$$L_{i,j}^t = L_{e,chan,i+(j-1)} \sqrt{N} + \frac{2\gamma_t}{\sigma^2} (1 - 2^{\tau_{-1}}),$$ (5)

where the damping factor is denoted by $\gamma_t$.

Finally, the input LLR vector is sent to an SC decoder to output new “HO” results.

III. GENETIC ALGORITHM BASED LLR GENERATOR DESIGN

The LLR generator, parameterized by the three damping factors, has a significant impact on the overall performance. Unfortunately, a theoretical optimum is difficult to obtain due to the following reasons. First, the extrinsic information transfer analysis is hard with the proposed component decoder. Second, the output of the component decoder is correlated with all its input vector due to the loopy decoding graph. Both make conventional density evolution methods inapplicable.

Artificial intelligence provides an alternative method in the case where a precise theoretical approach is unavailable. Recently, deep learning, reinforcement learning and genetic algorithm have been applied to design better code constructions [7] and decoding algorithms [8, 9].

Inspired by this, we exploit a genetic algorithm based on unsupervised learning to design the damping factors. Damping factors play a similar role of chromosomes in the genetic algorithm, because they both individually and collaboratively contribute to the fitness of a candidate. A good candidate requires that all its damping factors are respectively good. As such, a pair of good parents is likely to produce a good offspring, and this suggests that the genetic algorithm may ultimately converge to a good candidate.

At first, we start the genetic algorithm by initializing a population of size $M$. Each candidate contains $3t_{max}$ damping factors, including $\alpha_1$, $\beta_1$ and $\gamma_1$ (used to calculate LLR for the first decoding iteration) can be directly set to 0 without any performance loss, since there is no information from the previous iteration. Similarly, $\beta_2$ is directly set to 0.

The population are evaluated through Monte Carlo method and then ordered based on decoding performance. The minimum signal-to-noise ratio to achieve a target block error rate (SNR@targetBLER) is taken as the performance metric.

Then, the algorithm enters a loop consisting of four steps.

1) **Select** two distinct parents from the population. The $i$-th candidate is selected according to a probability $\frac{1}{\sum_{j=1}^{N} e^{-\lambda L_{i,j}}}^\frac{1}{2}$ (normalized), where $\lambda$ is called the sample focus. In this way, a better candidate will be selected with a higher probability. By adjusting the parameter $\lambda$, we can tradeoff between exploitation (a larger $\lambda$) and exploration (a smaller $\lambda$).

2) **Crossover** between parents to produce an offspring. Specifically, each damping factor of the offspring is
randomly selected from the corresponding ones of its parents.

3) **Mutate** the offspring randomly. This is implemented by independently mutating each damping factor with probability $p_{\text{mutate}}$. Specifically, if one damping factor is mutated, a random value sampled from Gaussian distribution $N((0, \sigma^2_{\text{mutate}})$ is added up to it. By adjusting $p_{\text{mutate}}$ and $\sigma^2_{\text{mutate}}$, we can tradeoff optimality (larger $\sigma^2_{\text{mutate}}$ and $p_{\text{mutate}}$) and convergence rate (smaller $\sigma^2_{\text{mutate}}$ and $p_{\text{mutate}}$).

4) **Insert** the offspring back to the population according to the decoding performance.

The algorithm loop is terminated after reaching a maximum number of iterations.

### IV. Performance Evaluation

We evaluate the performance gain brought by the proposed LLR generator and the genetic algorithm, respectively. The hyper parameters\(^1\) of the genetic algorithm are provided in Table I. The learning trajectories of the required SNR to achieve BLER=$10^{-3}$ are presented in Fig. 3. It shows that the decoding performance first improves rapidly as the genetic algorithm iterates and then converges gradually.

Two types of gains can be observed from Fig. 3. First, the gain brought by the proposed LLR generator is 0.5dB at BLER = $10^{-3}$, for both converged and non-converged cases.

The error detection results facilitate the “recovery” of soft LLRs in the proposed LLR generator, leading to the observed gain.

Second, we exemplify the “learning gain” through three points on the learning curve and present their BLER performances in Fig. 4. On the one hand, this proves the effectiveness of the genetic algorithm in designing good damping factors. With the converged damping factors in Table II, the proposed scheme is 0.2dB better than the best “hand-picked” damping factors\(^2\). On the other hand, it confirms that the component decoder with the proposed LLR generator exhibits better decoding performance than the case without it.

Next, we compare our scheme with some baselines in literatures.

1) The same code construction decoded by the parallel soft output decoding algorithm \(^3\). This scheme exhibits a similar degree of parallelism to the proposed decoding algorithm, but incurs higher implementation complexity due to the difficulty in handling the internal decoder data flow.

2) A polar code with the same length and code rate, evaluated under SC decoding. It enjoys more coding gain but incurs larger decoding latency due to the serial nature of SC decoding.

3) A recently proposed polar coding scheme with similar target for terabit/s throughput \(^6\), which employs...
Iter-277.69
7nm
75.46
(Gbps/
380.83
Latency
322.22
Convert to
86.24
231.41
533.16
152.95
109.25
173.55
Area Eff
174.8

Fig. 5. Compared with Type-1 and Type-2 baselines, the proposed decoder only trades 0.25dB~0.3dB loss at BLER=10^{-4} for improved area efficiency and reduced decoding latency. Compared with Type-3 baseline, the proposed scheme exhibits 0.75dB gain at BLER=10^{-4}. The polar codes are constructed by Gaussian approximation at Es/N0=6.3dB, 6.8dB, 6.0dB and 6.8dB for code rates 14161/16384, 885/1024, 14045/16384 and 877/1024, respectively.

Fig. 6. At BLER=10^{-4}, bypassing SC decoding can reduce 75% decoding complexity.

an unrolled hardware architecture for high throughput. “Unrolling” is only applicable for relatively short codes (e.g., 1024) and thus sacrifices coding gain. The evaluation results are presented in Fig. 5. Compared with Type-1 and Type-2 baselines, the proposed decoder only trades 0.25dB~0.3dB loss at BLER=10^{-4} for improved area efficiency and reduced decoding latency. Compared with Type-3 baseline, the proposed scheme exhibits 0.75dB gain at BLER=10^{-4}.

Then, we evaluate the complexity reduction due to skipped SC decoding. The number of activated SC decoders is measured to evaluate the complexity. The results are presented in Fig. 6. It shows that the complexity reduction ratio varies with SNR. For the case with higher SNR (lower BLER), more complexity is reduced. At BLER=10^{-4}, bypassing SC decoding can reduce 75% decoding complexity.

At last, the area efficiency of the proposed decoder is presented in Table III (see details in our ASIC implementation [10]). With TSMC 16nm process, the area efficiency for code rate 14161/16384 is 75Gbps/mm² when the maximum number of iterations is eight. The equivalent throughput under 7nm technology is about 322Gbps/mm² with eight iterations and 533Gbps/mm² with five iterations.

V. CONCLUSIONS

In this work, we propose a low-complexity parallel decoding algorithm of $G_N$-coset codes. The framework exploits two equivalent decoding graphs. For each graph, the inner component codes are independent and support parallel decoding. The component decoder adopts a novel design comprising an error detector, an LLR generator and an SC decoder. The LLR generator, parameterized by a set of damping factors, is “learned” offline by a genetic algorithm based unsupervised learning. The proposed decoding algorithm achieves comparable performance to the case with soft-output component decoder and conventional polar codes, but requires much lower decoding and hardware implementation complexity.

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