Hybrid Graph Models for Logic Optimization via Spatio-Temporal Information

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Abstract

Despite the stride made by machine learning (ML) based performance modeling, two major concerns that may impede production-ready ML applications in EDA are stringent accuracy requirements and generalization capability. To this end, we propose hybrid graph neural network (GNN) based approaches towards highly accurate quality-of-result (QoR) estimations with great generalization capability, specifically targeting logic synthesis optimization. The key idea is to simultaneously leverage spatio-temporal information from hardware designs and logic synthesis flows to forecast performance (i.e., delay/area) of various synthesis flows on different designs. The structural characteristics inside hardware designs are distilled and represented by GNNs; the temporal knowledge (i.e., relative ordering of logic transformations) in synthesis flows can be imposed on hardware designs by combining a virtually added supernode or a sequence processing model with conventional GNN models. Evaluation on 3.3 million data points shows that the testing mean absolute percentage error (MAPE) on designs seen and unseen during training are no more than 1.2% and 3.1%, respectively, which are 7-15x lower than existing studies.

1 Introduction

Despite great advance achieved by electronic design automation (EDA) tools, there is still a long way towards hardware agile development, whose ultimate goal is to reduce chip development cycles from years to months or even weeks. To enable rapid optimization-evaluation iterations, one mainstay is to evaluate quality-of-results (QoRs) quickly and accurately. Traditional EDA tools provide accurate estimations of QoR, yet are often time-consuming and require intensive manual effort, leading to limited design space exploration and long time-to-market. This situation is further exacerbated by explosion of modern hardware system complexity and technology scaling. Motivated by the strong desire for hardware agile development, a sound solution to fast and accurate QoR predictions is highly expected.

Recent years have witnessed the naissance of machine learning (ML) applied for computer systems and EDA tasks, whose ultimate goal is to reduce chip designs without retraining. That an ML algorithm should be able to directly apply to new designs without invoking any retraining.

Figure 1. EDA design flow and the proposed approach to predicting QoR after applying logic synthesis flows on hardware designs. (a) The focus of this paper is to accelerate evaluation phase in logic optimization. (b) The proposed model exploits spatial information from circuit designs and temporal knowledge from synthesis flows, generalizable to new designs without invoking any retraining.

[13], where one promising direction is ML-enabled fast performance modeling. Industrial investigations [4] highlighted two basic requirements for production-ready ML in EDA: ① the accuracy of ML-based performance estimation should be a minimum of 2σ (~95%); ② generalization capability is important for production-ready ML applications, meaning that an ML algorithm should be able to directly apply to new designs without retraining.

To this end, we target logic synthesis optimization in this work, and propose a novel ML approach for highly accurate QoR estimation with great generalization capability, as highlighted in Figure 1. Logic synthesis transforms functional RTL designs into optimized logic-gate-level representations. A logic synthesis flow refers to a sequence of logic optimizations, and a well designed flow can largely reduce design area and latency. While being studied for decades, there remain unresolved challenges and requirements for efficient logic optimization. ① The design space of possible synthesis flows is extremely large [16, 17]. It reemphasizes the importance of fast and accurate QoR prediction for
sufficient design space exploration. There is no one-for-all solution. Commercial EDA tools usually provide reference design flows [1] developed by experts based on heuristics or prior knowledge, but such flows do not uniformly perform well. As shown in Figure 2(a), first, for a specific design, different flows have drastically varied optimization effects; second, the same set of flows have different performance across different designs. These observations suggest the importance of design-specific synthesis flows. The transformation order in the flows should be well captured. Figure 2(b) compares the impact of different flow lengths, where the distribution of area/delay is not conspicuously improved with longer flows. This indicates that it is the underlying temporal information, i.e., relative ordering of logic transformations, inside synthesis flows that majorly determines final QoRs. Existing approaches do not generalize across designs. Prior arts leverage CNN [16] or LSTM [17] to predict QoRs for a certain design, where only flow-related but not design information is taken as input. These methods target fixed-length flows and have limited generalization capability to unseen designs due to the absence of design-specific information (more details in Section 4.3). Aiming at a practical use of ML-based performance model, the generalization across different designs and flow lengths is a necessity.

Reckoning on the aforementioned issues, we innovatively emphasize utilizing the spatio-temporal information from both hardware designs and synthesis flows, upon which a hybrid graph neural network (GNN) based model is proposed for logic synthesis flow QoR prediction. Specifically, the structural characteristics of hardware designs are distilled and represented by GNNs; the temporal knowledge among synthesis flows is extracted by a sequence processing model. Equipped with spatio-temporal knowledge, the proposed approach generalizes well on unseen designs. We summarize our contributions as follows:

- **Modeling.** We propose two generalizable GNN-based approaches to predict the performance of logic synthesis flows, which incorporate crucial spatio-temporal information from both hardware designs and synthesis flows. The first model utilizes a supernode on GNN, while the second model utilizes LSTM with GNN in a hybrid manner, to capture the temporal knowledge of flows.
- **Evaluation.** Evaluations on both seen and unseen (during training) designs demonstrate the superiority of our approach. On seen designs, i.e., transductive scenario, the mean absolute percentage error (MAPE) achieved by the hybrid GNN is less than 1.2%, which is 7× lower than existing works. On unseen designs, i.e., inductive scenario, the MAPE is still below 3.2%, 14× lower than existing works. It demonstrates the extraordinary generalization capability of our approach across designs with zero retraining.
- **Insights.** We provide insights on graph representation learning in EDA problems. (1) With carefully selected GNN models, stacking more layers (i.e., deep GNN) introduces a performance boost in prediction accuracy. (2) The temporal information from synthesis flows (not limited to logic synthesis) can be imposed on hardware netlists by combining a supernode or a sequence processing model with conventional GNN models.
- **Dataset.** We provide an open-source dataset consisting of 3.3 million data points collected from 11 different circuit designs, with the goal to facilitate multimodal or dynamic graph representation learning for EDA tasks.

2 Related Work and Preliminary

2.1 Related Work

In logic optimization, the sequence to apply logic transformations, i.e., logic synthesis flow, is often determined heuristically. For example, commercial EDA tools provide reference synthesis flows [1]; an academia open-source logic synthesis tool ABC [3] offers synthesis flows resyn, resyn2 and resyn2rs.

Recently, ML-assisted logic optimization has attracted increasing research interests, aiming to reduce exploration time and improve performance. LSOracle [11] employs multi-layer perceptron (MLP) to automatically decide which one of the two optimizers should be applied on different parts of circuits. The logic optimization can be formulated as an reinforcement learning problem, implemented with a GNN-based agent [5, 18] or a non-graph based agent [7]. The optimization objective is to minimize area [5, 7, 18] or delay [5]. In terms of forecasting logic synthesis flow performance,
Yu et al. [16] use a convolution neural network (CNN) to identify whether a synthesis flow is an angel-flow or a devil-flow. Later, they adopt a long short-term memory (LSTM) [17] network with transfer learning to predict delay and area after applying a synthesis flow.

From a broader view, GNNs are expected to better utilize graph structured data in many EDA problems. Instead of conventional graph representation learning that maps circuit designs from static graphs to labels (e.g., resource/timing/power) [12, 13], the target task in this work should consider both designs (i.e., static graphs) and synthesis flows (i.e., transformations to be applied on graphs) to provide high-accuracy predictions of delay/area, which can be recognized as a multi-modal or dynamic graph representation learning.

### 3 Proposed Hybrid Models

We propose novel, fast, accurate, and generalizable ML approaches for QoR estimations of logic synthesis flows, exploiting spatio-temporal information. Two models are explored: (1) a GNN for spatial information learning, armed with a supernode to encode temporal information (Section 3.2); (2) a hybrid model, composed of a GNN for spatial learning and an LSTM for temporal learning (Section 3.3).

#### 3.1 Problem Formulation

**Prediction task.** This work aims to optimize the logic synthesis flows from ABC [3], an open-source logic synthesis framework well-adopted in academia. The inputs to the proposed predictors are initial hardware designs described in RTL and synthesis flows to be applied. The QoR metrics to be predicted are logic area (denoted as area) and critical path delay (denoted as delay). The ground truth is collected from ABC after technology mapping.

**Graph representation for circuits.** As logic optimization targets gate-level transformations, we represent circuit designs as directed graphs, where each node is a primary logic gate and each edge shows logic dependency. To guarantee universal representations of any combinational logic functions, we include AND, OR, and NOT gates in the translated graphs. Thus, each node has two attributes: (1) node type in input/intermediate/output, and (2) operation type in AND/OR/NOT. The process of transforming an RTL design into a directed graph is exemplified in Figure 3(a).

**Flow representation.** Within the ABC framework, we consider synthesis flows composed of 7 types of logic transformation actions from $S = \{\text{balance (b), substitution (rs), substitution -z (rsz), rewrite (rw), rewrite -z (rwz), refactor (rf), refactor -z (rfz)}\}$. To integrate the inherent temporal information from synthesis flows with circuit designs, a synthesis flow can be represented as either (1) a vector to construct a supernode that directly propagates temporal knowledge to circuit designs (Section 3.2) or (2) a sequence embedding generated by an LSTM model (Section 3.3).

#### 3.2 GNN with Supernode

Inspired by the idea that introducing a supernode to graphs can collect and redistribute global information with some preference [8], we propose to leverage a supernode to represent synthesis flows. Since the supernode is virtually connected to all the nodes in the original graph, the temporal information is directly injected into the circuit graph, as shown in Figure 3(b).

**Supernode to embed synthesis flow.** Synthesis flows are converted to fixed-length input vectors with dimension of 25, since the maximum length of currently considered synthesis flows is 25. Each logic transformation in a flow is represented as an integer from 1 to 7. If the current flow is short than 25, we zero pad it. For example, the synthesis flow in Figure 3(b) is encoded into $[1, 6, 7, 1, 7, 1, 0, ...]$ as the initial input vector. A single fully-connected layer converts the $1 \times 25$ vector into $1 \times 8$ to be the supernode embedding.

**Spatial representation of circuit structure.** To study the impact of synthesis flows on the entire circuit design, we connect the supernode to all other nodes in original graphs. The two node attributes are converted to learnable node embeddings as $1 \times 8$ vectors. The modified graphs are passed through GNN models for graph representation learning. By exposing the temporal information encoded in the supernode and distributing to the entire graph, it is expected that this model can process both spatial and temporal features.
simultaneously, i.e., learning the effects of synthesis flows on different circuit structures.

3.3 Hybrid GNN with Spatio-Temporal Information

While a supernode is capable to collect global information and distribute temporal knowledge to every other node in graphs, we notice three concerns that may influence prediction performance. First, synthesis flows are represented by fixed-length vectors, which are then passed through an MLP to comply with the embedding dimension of other nodes. This setting is insensitive to sequence dependence, i.e., transformation order in synthesis flows, whereas the impact of later transformations heavily depends on previous ones. Second, as the message passing process proceeds, the original temporal information inside the supernode is gradually faded in other nodes. Third, by adding the supernode that connects all the nodes in the original graph, the graph size increases with newly added edges, which may cause scalability issue in implementation when encountering extremely large graphs.

To address the first concern, a more natural way is to leverage a sequence processing model to distill temporal information, and the specific model employed in this work is LSTM, which excels at handling order dependence and variable-length flows. To resolve the second and the third concerns, we separately generate a sequence embedding (i.e., synthesis flow representation) and a graph embedding (i.e., circuit representation) in the feature extraction stage, and these two embeddings are concatenated for downstream predictions. The approach of separately learning two embeddings and then concatenating is intuitively consistent with actual logic synthesis procedure, mimicking the operation of applying the synthesis flow to the circuit.

Figure 3(c) illustrates the structure of the second hybrid GNN model with LSTM. The directed graph translated from a circuit design is passed through a GNN model, followed by a linear layer to generate a graph-level representation (i.e., $1 \times 32$ vector). The synthesis flow is processed by a 2-layer LSTM to derive a flow representation (i.e., $1 \times 64$ vector). These two vectors are concatenated to form a $1 \times 96$ vector. Finally, a multi-layer perceptron (MLP) with structure 96-100-100-1 is adopted for delay/area predictions.

4 Experiment

4.1 Dataset Generation

We select eleven circuit designs from the EPFL benchmark [2], a benchmark suite designed as a comparative standard for logic optimization and synthesis. The logic synthesis flows are generated by the logic synthesis tool ABC [3]. To demonstrate flexibility of handling variable-length synthesis flows, we create synthesis flows consisted of 10, 15, 20, and 25 logic transformations, respectively. For each different length, there are 50,000, 50,000, 100,000, and 100,000 flows, respectively, totally making up 300,000 flows. Each synthesis flow consists of logic transformations from $S = \{b, rs, rsz, rw, rwz, rfz\}$. All the 300,000 flows are applied to eleven different designs with ASAP 7nm low-voltage technologies [15], which are 3.3 million data points in total. The ground truth (i.e., label) is collected from ABC after technology mapping.
4.2 Experimental Setup

Baseline. The proposed hybrid GNN models are compared against two existing ML-based approaches: a CNN-based model [16], and an LSTM-based model [17]. We exactly follow the model structures mentioned in prior work, with minor modifications to fit our prediction task.

- In the CNN baseline, each transformation is represented as a one-hot vector: synthesis flows (with the maximum length of 25) are represented as $7 \times 25$ matrices with zero padding for shorter flows. We honor the original CNN structure in [16], in which there are two convolutional layers followed by a max-pooling and two FC layers. Since the task in [16] is classification, we replace the final classifier by a single neuron for value prediction in our task. Note that the CNN can only be trained in a design-specific manner, i.e., one model for one design.

- In the LSTM baseline, we change one-hot embeddings of transformations to learnable embeddings. Similar to CNN, although LSTM should also be design-specific, we intentionally study its generalizability by training one model for all. To distinguish different designs, we add design names as identity preceding to synthesis flows to construct new sequences. It has two LSTM layers with the hidden size of 128, followed by an MLP of 128-30-30-1 to predict delay/area.

Implementation and training. Training, validation, and testing sets are split by 20:5:75. We highlight two training and evaluation strategies. First, in contrast to many ML tasks that use a large proportion of the entire dataset for training, we intentionally train the proposed models with a small portion and conduct evaluations on the rest data points. Second, we evaluate both transductive and inductive scenarios. If a design is seen during training but with unseen flows in the testing, it is called transductive; if a design is unseen in both training and testing, it is called inductive. The goal is to emphasize the generalizability of our proposed models, which is important for many EDA tasks that are possibly suffering from data scarcity. Among eleven circuit designs, six of them (adder, arbiter, bar, div, log2, and max) are used for both training and testing, and the remaining five (multiplier, sin, sqrt, square, and voter) are merely evaluated in testing to demonstrate generalization, i.e., inductive capability.

Training details are summarized as follows.

- We train a design-specific CNN for each design, each for 20 epochs with RMSprop optimizer with learning rate 0.05.
- LSTM baseline is trained for 100 epochs with Adam optimizer, initial learning rate 0.002, weight decay 2e-6.
- For the GNN with supernode (denoted as GNN-S), we use a 10-layer GIN model; node and edge embedding dimensions are 8 and 2, respectively. The model is trained for 20 epochs with the Adam optimizer and learning rate of 0.001.
- For the hybrid GNN-LSTM model (denoted as GNN-H), we use a 10-layer GIN. The node embedding dimension is 32 and the hidden size of LSTM is 64. The model is trained for 20 epochs with the Adam optimizer. The initial learning rate is 0.002, with a weight decay of 2e-6.

### 4.3 Evaluation

**Transductive scenario.** Table 2 shows the MAPE of QoR predictions on the designs that are seen during training but with unseen synthesis flows. We have the following observations. ① Since the CNN baseline is design-specific, it slightly outperforms the LSTM model, which is a unified model across all designs. ② The hybrid GNN model, GNN-H, significantly outperforms CNN and LSTM, with 7× and 15× lower MAPE than those of area and delay prediction, respectively. ③ The GNN-S with supernode shows comparable performance with the LSTM model.

**Inductive scenario.** Table 3 shows the MAPE of area/delay predictions on unseen designs. ① The CNN-based model can only work for design-specific synthesis flows and thus there is no generalization to unseen designs. ② The LSTM-based model suffers from a large accuracy degradation for unseen designs, indicating limited generalization capability. ③ The GNN-S model slightly outperforms the LSTM model by 3% and 9% in area and delay prediction, respectively (further discussed in Section 4.4). ④ The hybrid GNN-H maintains its high prediction accuracy by slightly increasing the MAPE from 1% to 3%, demonstrating extraordinary generalization capability.

**Sensitivity analysis.** We study design choices of GNN-H in terms of GNN types and the number of layers. Fig. 4 compares the MAPE of QoR predictions with respect to both GIN and GCN models with different number of layers. Generally, GIN models receive an accuracy boost after stacking ten layers, whereas GCN models show similar prediction accuracy among different choices of layers. ① Regarding GNN type comparison, GCN suffers from the over-smoothing problem [10]. Mathematically, GCN [9] is an approximate of $2L - L$, where $L$ is the normalized graph Laplacian and $I_N$ is the identity matrix. Since the graph Laplacian operator/filter is a high-pass filter, GCN naturally becomes a low-pass filter, indicating that stacking many layers does not help better characterize graph structures. ② Regarding the number of GNN layers, a deep GNN setting with carefully selected GNN types possesses better representation power, since stacking more layers brings a larger receptive field to characterize input graphs and provides hierarchical abstraction of input structures, especially beneficial for large graphs.
Figure 4. Sensitivity analysis of GNN-H. Transductive and inductive MAPE on area/delay predictions are compared with respect to GIN and GCN with different number of layers.

Table 2. Comparison with CNN [16] and LSTM [17] on seen designs, i.e., transductive. GNN-S is the proposed GNN with supernode; GNN-H is the proposed hybrid GNN.

|        | CNN Area (MAPE) | LSTM GNN-S GNN-H | CNN Delay (MAPE) | LSTM GNN-S GNN-H |
|--------|-----------------|-------------------|------------------|------------------|
| adder  | 7.00% 8.72% 7.65% 0.87% | 1.76% 16.22% 1.79% 0.76% | 2.98% 13.66% 8.16% 1.56% | 0.23% 18.96% 15.37% 1.86% |
| arbiter| 8.46% 5.22% 22.72% 1.61% | 0.74% 14.98% 22.59% 2.06% | 3.64% 13.94% 8.35% 1.48% | 5.50% 17.37% 20.60% 0.68% |
| bar    | 12.71% 7.75% 13.16% 0.88% | 7.72% 14.31% 9.29% 0.16% | 8.04% 9.05% 4.19% 0.55% | 7.28% 6.18% 8.35% 1.48% |
| div    | 5.04% 10.05% 8.16% 1.56% | 3.87% 11.85% 12.74% 0.53% | 7.28% 6.18% 8.35% 1.48% | 5.50% 17.37% 20.60% 0.68% |
| log2   | 7.28% 6.18% 8.35% 1.48% | 5.50% 17.37% 20.60% 0.68% | 7.28% 6.18% 8.35% 1.48% | 5.50% 17.37% 20.60% 0.68% |
| max    | 7.28% 6.18% 8.35% 1.48% | 5.50% 17.37% 20.60% 0.68% | 7.28% 6.18% 8.35% 1.48% | 5.50% 17.37% 20.60% 0.68% |
| MEAN   | 7.75% 8.43% 10.70% 1.16% | 3.30% 15.62% 13.73% 1.00% | 7.75% 8.43% 10.70% 1.16% | 3.30% 15.62% 13.73% 1.00% |

Table 3. Comparison with CNN [16] and LSTM [17] on unseen designs, i.e., inductive.

|        | LSTM GNN-S GNN-H | LSTM GNN-S GNN-H |
|--------|-----------------|-----------------|
| multiplier | 57.82% 9.39% 2.45% | 38.21% 17.89% 1.75% |
| sin     | 66.09% 44.84% 2.34% | 45.94% 54.44% 2.32% |
| sqrt    | 29.03% 39.25% 4.83% | 38.03% 15.75% 2.09% |
| square  | 38.59% 13.96% 2.86% | 47.52% 31.34% 2.41% |
| voter   | 27.38% 76.49% 3.08% | 42.19% 46.54% 0.96% |
| MEAN    | 43.78% 40.71% 3.11% | 42.38% 33.20% 1.91% |

4.4 Discussion and Insight

GNN-S v.s. GNN-H. In GNN-S, even though a synthesis flow is encoded as a supernode, there are several limitations that influence temporal information characterization. First, every synthesis flow is directly represented as a fixed-length vector to generate supernode embedding, which is insensitive to sequence dependence, i.e., the order of logic transformations. Second, the original temporal information injected to the supernode is gradually diluted, since the supernode embedding also evolves during message passing. By contrast, GNN-H leverages a more direct scheme that takes advantages of both GNN and LSTM to extract spatio-temporal information in a decoupled manner. During feature extraction, the LSTM directly characterizes temporal information from synthesis flows, and the GNN focuses on representing spatial structure of circuit designs. Rather than mixing spatial and temporal information at the very first step (as in GNN-S), separately built and learned graph and sequence embeddings have better expressiveness for each source of input information, thus providing a better foundation for downstream tasks.

Scalability regarding graph abstraction level. Table 1 shows the gate-level graph size of different circuit designs. The bright side is both GNN-S and GNN-H can handle large graphs. The dark side is the graph size will explode for larger circuit designs, which may cause scalability issues in practical implementation. This concern is more obvious in GNN-S, which adds a considerable number of virtual edges to original graphs, i.e., $|V|$ virtual edges will be newly added for a graph original with $|V|$ nodes. Two potential directions to further improve scalability are ① extracting graphs from higher level of circuit abstractions to provide graphs in proper size, or ② clustering nodes in gate-level graphs hierarchically to guarantee reasonable compute cost for each stage.

Multi-modal graph representation learning. Prior arts that adopt GNNs for fast evaluation focus on mapping static circuit graphs to metric of interest [12, 13]. The most significant innovation of this work is to consider input information from multiple modality, i.e., circuit designs in graph format and synthesis flows in sequence format. This is because the final QoR of circuit designs is dependent on both circuit structure and synthesis flows. Our attempt with GNN-S shows that purely GNN-based model structure may not properly characterize temporal information, indicating the necessity of multi-modal feature extraction for better representation power. The multi-modal graph representation learning, which integrates knowledge from other learning
scheme with conventional graph representation learning, are expected to provide more versatility for EDA tasks.

5 Conclusion
In this work, we explored the rapid performance prediction for logic synthesis under given optimization flows. We highlighted the importance of jointly considering the spatial and temporal information, i.e., the graph structure that represents the circuit, and the optimization sequence, respectively. With spatio-temporal information, we proposed two hybrid GNN-based models to predict the synthesized design area and latency: the first is GNN with supernode, and the second is hybrid GNN with LSTM, where the supernode and LSTM encode the temporal information. We built a large dataset from 11 circuit designs to evaluate our predictor on both seen and unseen designs. Evaluation shows that the testing MAPE on designs seen and unseen during training are no more than 1.2% and 3.1%, respectively. The proposed approach demonstrates great generalization capability across designs, without resorting to any retraining.

References
[1] Accessed: 2021. Lynx Design System. https://www.synopsys.com/content/dam/synopsys/implementation&signoff/datasheets/lynx-design-system-ds.pdf.
[2] Luca Amarú et al. 2015. The EPFL combinational benchmark suite. In IWLS.
[3] Robert Brayton and Alan Mishchenko. 2010. ABC: An academic industrial-strength verification tool. In International Conference on Computer Aided Verification. Springer.
[4] Jeff Dyck. 2018. Production-Ready Machine Learning for EDA. https://webinars.sw.siemens.com/production-ready-machine-learning/room.
[5] Winston Haaswijk et al. 2018. Deep learning for logic optimization algorithms. In ISCAS. IEEE, 1–4.
[6] Sepp Hochreiter and Jürgen Schmidhuber. 1997. Long short-term memory. Neural computation (1997).
[7] Abdelrahman Hosny, Soheil Hashemi, Mohamed Shalan, and Sherief Reda. 2020. Drills: Deep reinforcement learning for logic synthesis. In ASP-DAC. IEEE.
[8] Katsuhiko Ishiguro et al. 2019. Graph Warp Module: an Auxiliary Module for Boosting the Power of Graph Neural Networks in Molecular Graph Analysis. (2019). arXiv:1902.01920
[9] Thomas N Kipf and Max Welling. 2016. Semi-supervised classification with graph convolutional networks. arXiv preprint arXiv:1609.02907 (2016).
[10] Meng Liu et al. 2020. Towards deeper graph neural networks. In Proceedings of the 26th ACM SIGKDD International Conference on Knowledge Discovery & Data Mining. 338–348.
[11] Walter Lau Neto et al. 2019. LSOracle: A logic synthesis framework driven by artificial intelligence. In ICCAD. IEEE.
[12] Nan Wu et al. 2021. IronMan: GNN-assisted Design Space Exploration in High-Level Synthesis via Reinforcement Learning. In GLSVLSI.
[13] Nan Wu and Yuan Xie. 2021. A Survey of Machine Learning for Computer Architecture and Systems. arXiv preprint arXiv:2102.07952 (2021).
[14] Keyulu Xu et al. 2018. How Powerful are Graph Neural Networks?. In ICLR.
[15] Xiaofeng Xu et al. 2017. Standard cell library design and optimization methodology for ASAP7 PDK. In ICCAD. IEEE.