Imaging, simulation, and electrostatic control of power dissipation in graphene devices

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We directly image hot spot formation in functioning mono- and bilayer graphene field effect transistors (GFETs) using infrared thermal microscopy. Correlating with an electrical-thermal transport model provides insight into carrier distributions, fields, and GFET power dissipation. The hot spot corresponds to the location of minimum charge density along the GFET; by changing the applied bias this can be shifted between electrodes or held in the middle of the channel in ambipolar transport. Interestingly, the hot spot shape bears the imprint of the density of states in mono- vs. bilayer graphene. More broadly, we find that thermal imaging combined with self-consistent simulation provides a non-invasive approach for more deeply examining transport and energy dissipation in nanoscale devices.

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Power dissipation is a key challenge in modern and future electronics. Graphene is considered a promising new material in this context, with electrical mobility and thermal conductivity over an order of magnitude greater than silicon. Graphene is a two-dimensional crystal of $sp^2$-bonded carbon atoms, whose electronic properties can be tuned with an external gate. By varying the gate voltage ($V_G$) with respect to source (S) or drain (D) terminals, as labeled in Fig. 1, the electron and hole densities can be altered, resulting in an ambipolar GFET. At large source-drain voltage bias ($V_{SD}$), the electrostatic potential varies significantly along the channel, leading to an inhomogeneous distribution of carrier types, densities, and drift velocities. The power dissipated is related to the local current density ($J$) and electric field ($F$) in samples larger than the carrier mean free paths ($\lambda = J \cdot F$). Thus, a GFET with large applied bias should have regions of varying power dissipation, tied to the local charge density and electrostatic profile.

Two recent studies have revealed the effect of Joule heating in monolayer graphene using Raman thermometry. However, the small size of devices investigated (1-2 μm) did not allow detailed spatial imaging. In this work, we utilize sufficiently large samples (~25 μm) and use infrared (IR) thermal microscopy to observe clear spatial variations of dissipated power, in both monolayer and bilayer graphene devices. In addition, we introduce a comprehensive simulation approach which reveals the coupling of electrostatics, charge transport and thermal effects in GFETs. The combination of thermal imaging and self-consistent modeling also provides a non-invasive method for in situ studies of transport and power dissipation in such devices.

We prepared mono- and bilayer GFETs, as shown in Fig. 1b and described in the Supplementary Information. For consistency, we refer to the ground electrode as the drain and the biased electrode as the source regardless of the majority carrier type or direction of current flow. Sheet resistance vs. gate voltage ($R_S-V_{GD,0}$) measurements are shown in Fig. 1c, at low bias ($V_{SD} = 20$ mV). Here, we subtract the so-called Dirac voltage ($V_0$) which is the gate voltage at the charge neutrality point. Gate voltages lower and higher than $V_0$ provide holes and electrons as the majority carriers, respectively. At low bias the graphene sheet resistance is given by $R_S = 1/[q \mu_0 (n + p)]$, where $\mu_0$ is the low-field mobility, $n$ and $p$ are the electron and hole carrier densities per unit area, respectively, and $q$ is the elementary charge. Our new charge density model takes into account thermal generation ($n_{th}$) and residual puddle density ($n_{pd}$) as detailed further below. At high temperatures in our measurements the former often dominates. The fit in Fig.
$I_c$ is obtained with $R = R_C + R_S L / W$, where $R_C = 300 \, \Omega$ is the measured contact resistance, $L$ and $W$ are the length and width of the GFET. Good agreement is obtained, with only two fitting parameters $\mu_0 = 3590 \, \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $n_{pd} = 1.2 \times 10^{11} \, \text{cm}^{-2}$, consistent with previous reports.$^{13, 14}$ We note that at low $V_{SD}$ bias the electrostatic potential and Fermi level are nearly flat along the graphene, and the charge density is constant and determined only by the gate voltage, impurities, and temperature.

On the other hand, a large $V_{SD}$ bias induces a significant spatial variation of the potential in the GFET. This leads to changes in carrier density, electric field, and power dissipation along the channel. In turn, this results in a spatial modulation of the device temperature, as revealed by our IR microscopy. We first consider the monolayer graphene device, as shown in Figs. 1d and 2. The temperature profiles along the graphene channel are displayed in Fig. 1d with various $V_{SD}$ at $V_{GD-0} = -33 \, \text{V}$ (strongly hole-doped transport), and the temperature increases linearly with applied power as expected (see Fig. 1d inset).

Figure 2 shows imaged temperature maps with distinct hot spots that vary along the channel with the applied voltage (also see supplementary movie file$^{15}$). This implies that the primary heating mechanism is due to energy loss by carriers within the graphene channel, and not due to contact resistance. However, we note the raw temperature reported by the IR microscope is lower than the actual GFET temperature, and must be corrected before being compared with our simulation results below.$^{16}$ Figures 2a-c show raw thermal IR maps of the monolayer GFET for $V_{GD-0} = -3.7 \, \text{V}$, 3 V, and 12.2 V with $V_{SD} = 10 \, \text{V}$, 12 V, and 10 V, respectively. These represent three scenarios, i.e. (a) unipolar hole-majority channel, (b) ambipolar conduction, and (c) unipolar electron-majority channel. In the hole-doped regime, at $V_{GD-0} = -3.7 \, \text{V}$ (Figs. 2a,d,g), the hole density is minimum near the drain and a hot spot develops there (left side). As the back-gate voltage increases to $V_{GD-0} = 3 \, \text{V}$ (Figs. 2b,e,h), the graphene becomes electron-doped at the drain. Given that $V_{SD} = 12 \, \text{V}$, the region near the source remains hole-doped as $V_{GS} = V_{GD} - V_{SD} = -9 \, \text{V}$. This is an ambipolar conduction mode, with electrons as majority carriers near the drain, and holes near the source as indicated by the block arrows in Fig. 2b. The minimum charge density point is now towards the middle of the channel, with the hot spot correspondingly shifted. At $V_{GD-0} = 12.2 \, \text{V}$ (Figs. 2c,f,i) electrons are majority carriers throughout the graphene channel, and the hot spot forms near the source electrode (right side). In other words, as the gate voltage
changes, the device goes from unipolar hole to ambipolar electron-hole and finally unipolar electron conduction, with the hot spot shifting from near the drain to near the source. This is precisely mirrored in the temperature profiles along the graphene channel, as shown in Fig. 2d-f (lower panels).

To obtain a quantitative understanding of this behavior, we introduce a new model of monolayer and bilayer GFETs by self-consistently coupling the current continuity, thermal, and electrostatic (Poisson) equations. This is a drift-diffusion approach suitable here due to the large scale (~25 μm) and elevated temperatures of the GFET, with carrier mean free paths much shorter than other physical dimensions. For example, the electron mean free path may be estimated as \( l_n \approx (h/2q)\mu(n/\pi)^{1/2} \approx 30 \text{ nm} \), for typical \( n = 5 \times 10^{11} \text{ cm}^{-2} \) and \( \mu = 3600 \text{ cm}^2/\text{V} \cdot \text{s} \) in our samples. The phonon mean free path has been estimated at \( l_{ph} \approx 0.75 \mu \text{ m} \) in freely suspended graphene, although it is likely to be lower in graphene devices operated a high bias and high temperature on SiO\(_2\) substrates. Both figures are much shorter than the device dimensions.

We set up a finite element grid along the GFET, with \( x = 0 \) at the left electrode edge and \( x = L \) at the right electrode. The left electrode is grounded and all voltages are written with respect to it. The electron (\( n_x \)) and hole (\( p_x \)) charge densities, velocity (\( v_x \)), field (\( F_x \)), potential (\( V_x \)) and temperature (\( T_x \)) along the graphene sheet are computed iteratively until a self-consistent solution is found. The “\( x \)” subscript denotes all quantities are a function of position along the graphene device. We note that the temperature influences the charge density by changing the intrinsic carriers through thermal generation. This is particularly important when the local potential (\( V_x \)) along the graphene is near the Dirac point, and the carrier density is at a minimum. We also note that both electron and hole components of the charge density are self-consistently taken into account. The model properly “switches” from electron- to hole-majority carriers with the local potential along the graphene, yielding the correct ambipolar behavior of the GFET.

Starting from grid element \( x = 0 \), the current continuity condition gives:

\[
I_D = \text{sgn}(p_x - n_x)qW(p_x + n_x)v_x
\]

where the subscript \( x \) is the position along the \( x \)-axis. The carrier densities per unit area are given by

\[
n_p = \frac{[\pm n_{c\text{ex}} + (n_{c\text{ex}}^2 + 4n_{ix}^2)^{1/2}]/2, \text{where upper (lower) signs correspond to holes (electrons).}}{21}
\]

Here \( n_{c\text{ex}} = C_{ox}(V_0 - V_{Gx})/q, C_{ox} = \epsilon_{ox}t_{ox} \) is the SiO\(_2\) capacitance per unit area, and \( V_{Gx} = V_G - V_x \).
is the potential difference between the back-gate and graphene channel at position $x$. The intrinsic carrier concentration is $n_{ix}^2 \approx n_{th}^2 + n_{pd}^2$, where $n_{th} = (\pi/6)(k_BT_x/\hbar v_F)^2$ are the thermally excited carriers in monolayer graphene, $n_{pd}$ is the residual puddle concentration, and $T_x$ is the temperature at position $x$. In bilayer graphene, $n_{th} = (2m^* / \pi\hbar^2)k_BT_x\ln(2)$ due to the near-parabolic bands. The velocity ($v_x$) is obtained from the current and charge, and the local field ($F_x$) is calculated from the velocity-field relation

$$F_x = \text{sgn}(p_x - n_x) \frac{v_x}{\mu_0 \left(1 - |v_x / v_{sat}|\right)}$$  \hspace{1cm} (2)$$

which includes the velocity saturation $v_{sat}$ discussed below. The Poisson equation then relates the field to the potential along the graphene as $F_x = \partial V_x / \partial x$. To include temperature we also self-consistently solve the heat equation along the GFET as:

$$A \frac{\partial}{\partial x} \left( k \frac{\partial T}{\partial x} \right) + P'_x - g \left(T - T_0\right) = 0,$$  \hspace{1cm} (3)$$

where $P'_x = I_D F_x$ is the Joule heating rate in units of Watts per unit length, $A = WH$ is the graphene cross-section (monolayer “thickness” $H = 0.34$ nm), $k$ is the graphene thermal conductivity, $g$ is thermal conductance to the substrate per unit length, and $T_0$ is the ambient temperature. Interestingly, we note that the device simulations here are quite insensitive to the value of the graphene thermal conductivity ($k \approx 600$–$3000$ Wm$^{-1}$K$^{-1}$), but much more sensitive to the heat sinking path through the SiO$_2$ ($g$) and the exact device electrostatics. Thermal transport in large devices ($L, W \gg$ healing length $L_H \sim 0.2$ µm, see Supplementary Information) is dominated by the thermal resistance of the SiO$_2$ layer, rather than by heat flow along the graphene sheet itself. The thermal transport is reduced to a 1-dimensional problem as in previous work on carbon nanotubes (CNTs). Thus, the thermal coupling between graphene and the silicon backside is replaced by an overall thermal conductance per unit length, $g \approx 1/[L(R_{ox} + R_{Si})] \approx 18$ WK$^{-1}$m$^{-1}$ (see Supplementary Information). This is significantly higher than that of a typical CNT on SiO$_2$ ($\sim 0.2$ WK$^{-1}$m$^{-1}$), due to the much greater width of the graphene sheet. In addition, heat sinking from CNTs is almost entirely dominated by the CNT-SiO$_2$ interface thermal resistance, whereas thermal sinking from the graphene sheet is primarily limited by the 300 nm thickness of the SiO$_2$ itself.
Figures 2a-c show raw temperature maps taken at the last point in the $I_D$-$V_{SD}$ sweeps from Figs. 2g-i, respectively. Figures 2d-f show actual temperature cross-sections (bottom panels, scattered dots) and simulation results for charge density and temperature (top and bottom panels, lines). Here, the actual temperature of the graphene sheet is obtained based on the raw imaged temperature of Figs. 2a-c (Ref. 16 and Supplementary Information). Field dependence of mobility and velocity saturation are included with an effective mobility \( \mu = \mu_0 (1 - |v_x/v_{sat}|) \) in our model. Here, \( v_{sat} = v_F E_{SO}/E_F \) is the saturation velocity, \( v_F \approx 10^6 \) m/s is the Fermi velocity, \( E_F \) is the Fermi level with respect to the Dirac point (positive for electrons, negative for holes), and \( E_{SO} \approx 60 \) meV is the dominant surface optical (SO) phonon energy for SiO$_2$.\(^7\) Solid curves from simulations show excellent agreement with the measured \( I-V \) characteristics (Figs. 2g-i) and good agreement with the measured temperature profiles (Figs. 2d-f)\(^28\) (also see Supplementary Information, Figs. S7-S8). We find that \( v_{sat} \) varies from 2.9×10$^7$ cm/s to 8.8×10$^7$ cm/s while the carrier density varies from 3.2×10$^{12}$ cm$^{-2}$ to 3.4×10$^{11}$ cm$^{-2}$.

While the \( I-V \) characteristics show excellent agreement between experiment and simulation, the temperature profiles provide additional insight into transport and energy dissipation. Best agreement is found near the hot spot locations, marked by arrows in Fig. 2d-f, but a slight discrepancy exists between temperature simulation and data near the metal electrodes. We attribute this in part to inhomogeneous doping and charge transfer on micron-long scales between the metal electrodes and graphene.\(^29,30\) In addition, recent work has also found that persistent Joule heating can lead to undesired charge storage in the SiO$_2$ near the contacts where the fields are highest,\(^31\) resulting in a possible discrepancy between the experiments and model calculations.

Before moving on, we address a few simulation results which are related to, but not immediately apparent from the temperature measurements. The calculated carrier density profiles along the GFET at each biasing scenario are shown in the upper panels of Figs. 2d-f, respectively. The simulations confirm that temperature hot spots are always located at the position of minimum carrier density along the channel. This occurs near the grounded drain for hole conduction (Fig. 2d) and near the source for electron conduction (Fig. 2f). In ambipolar operation (Fig. 2e) the hot spot forms approximately at \( x = -7.5 \) \( \mu \) in both simulation and measured temperature, which is the crossing point of electron and hole concentrations. In this case, the temperature distribution is broader, also in good agreement with the thermal imaging data. Thus, the temperature
measurement technique is an indicator of the electron and hole carrier concentrations, as well as the polarity of the graphene device. Combined with our simulation approach, non-invasive IR thermal imaging provides essential insight into the inhomogeneous charge density profile of the GFET channel under high bias conditions. In a sense, this finding is similar to the shift of electroluminescence previously observed in ambipolar carbon nanotubes.\textsuperscript{32} However, due to the absence of an energy gap in monolayer graphene, carrier recombination at the pinch-off region results primarily in heat (phonon) dissipation rather than light (photon) emission.

Figure 3 shows the thermal imaging of a bilayer GFET in unipolar hole doped (Fig. 3a with $V_{GD,0} = -42$ V), ambipolar (Fig. 3b with $V_{GD,0} = -12$ V), and unipolar electron doped transport regimes (Fig. 3c with $V_{GD,0} = 25$ V). The qualitative temperature distributions are similar to the respective monolayer GFET cases. For instance, the hot spots in both the hole and electron doped regimes are at the location of minimum carrier density. In ambipolar transport the peak temperature appears near the middle of the bilayer GFET, as shown in Fig. 3b and lower panel of Fig. 3e, similar to the monolayer GFET. However, the temperature profile in bilayer is much broader than in monolayer graphene, a distinct signature of the different band structure and density of states (Fig. 3i vs. Fig. 2i insets). This, in turn, alters the dependence of carrier densities on the electrostatic potential, and the magnitude of the thermally excited carrier concentration $n_{th}$.\textsuperscript{22} To take these into account, we include the effective mass $m^* \approx 0.03m_0$ of the near-parabolic bilayer band structure\textsuperscript{33, 34} and the saturation velocity $v_{sat} \approx (E_{OP}/m^*)^{1/2}$ independent of carrier density unlike in monolayer graphene,\textsuperscript{23} where $E_{OP} \approx 180$ meV is an average optical phonon energy.\textsuperscript{35} The best overall agreement with the bilayer experimental data is found with $\mu_0 = 1440$ cm$^2$V$^{-1}$s$^{-1}$ and $n_{pd} = 0.7 \times 10^{11}$ cm$^{-2}$ as remaining parameters. Using this model all calculated $I_D$-$V_{SD}$ curves (Fig. 3g-i) and temperature distributions of the bilayer GFET (Fig. 3d-f) show excellent agreement with the experimental data. As with the monolayer graphene device, the thermal imaging approach combined with coupled electrical-thermal simulations yields deeper insight into the carrier distributions, polarity, and energy dissipation of the device at high bias. In addition, the agreement between simulations and thermal imaging near the contacts is improved in bilayer graphene, suggesting this system is less sensitive to charge transfer\textsuperscript{29, 30} or SiO$_2$ charge storage near the two electrodes.\textsuperscript{31}
Before concluding, it is relevant to summarize both fundamental and technological implications of our findings. Of relevance to high-field transport in graphene devices, we found that the power dissipation is uneven, and that the hot spot depends both on device voltages and electrostatics, and the density of states (e.g. monolayer vs. bilayer). The location of the hot spot corresponds to that of minimum charge density in unipolar transport, and to that of charge neutrality in ambipolar operation. Interestingly, the hot spot can be controlled with the choice of voltages applied on the three terminals, such that independent thermal annealing of either the source or the drain, or of any region in between could be achieved, particularly in monolayer graphene.

From a technological perspective, we have shown that graphene-on-insulator (GOI) devices pose similar thermal challenges as those of silicon-on-insulator (SOI) technology.\textsuperscript{36-38} For practical applications the SiO\textsubscript{2} layer must be thinned to minimize temperature rise, or until parasitic (graphene-to-silicon) capacitance effects limit device performance. Moreover, we have shown that such thermal effects can be modeled self-consistently, by introducing a coupled solution of the continuity, thermal, and electrostatic equations. Finally, the combination of IR imaging and simulations reveals much more than electrical measurements alone, and opens up the possibility of non-invasive thermal imaging as a tool for other studies of high-field transport and energy dissipation in nanoscale devices.

**Supporting Information Available:** Details of sample fabrication and setup, additional model calculations of heat dissipation in graphene, and procedure for obtaining the true graphene temperature from the raw temperature imaged by the infrared scope.

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References

1. Pop, E. Energy dissipation and transport in nanoscale devices. *Nano Research* **3**, 147-169 (2010).
2. Mahajan, R. Cooling a Microprocessor Chip. *Proc. IEEE* **94**, 1476-1486 (2006).
3. Morozov, S.V. et al. Giant Intrinsic Carrier Mobilities in Graphene and Its Bilayer. *Physical Review Letters* **100**, 016602-016604 (2008).
4. Nika, D.L., Pokatilov, E.P., Askerov, A.S. & Balandin, A.A. Phonon thermal conduction in graphene: Role of Umklapp and edge roughness scattering. *Physical Review B* **79**, 155413-155412 (2009).
5. Geim, A.K. & Kim, P. Carbon wonderland. *Scientific American* **298**, 90-97 (2008).
6. Geim, A.K. Graphene: Status and Prospects. *Science* **324**, 1530-1534 (2009).
7. Meric, I. et al. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nature Nano* **3**, 654-659 (2008).
8. Lindefelt, U. Heat generation in semiconductor devices. *Journal of Applied Physics* **75**, 942-957 (1994).
9. Freitag, M. et al. Energy Dissipation in Graphene Field-Effect Transistors. *Nano Letters* **9**, 1883-1888 (2009).
10. Chae, D.-H., Krauss, B., von Klitzing, K. & Smet, J.H. Hot Phonons in an Electrically Biased Graphene Constriction. *Nano Letters* **10**, 466-471 (2010).
11. Novoselov, K.S. et al. Electric Field Effect in Atomically Thin Carbon Films. *Science* **306**, 666-669 (2004).
12. Fang, T., Konar, A., Xing, H. & Jena, D. Carrier statistics and quantum capacitance of graphene sheets and ribbons. *Applied Physics Letters* **91**, 092109-092103 (2007).
13. Martin, J. et al. Observation of electron-hole puddles in graphene using a scanning single-electron transistor. *Nature Physics* **4**, 144-148 (2008).
14. Kim, S. et al. Realization of a high mobility dual-gated graphene field-effect transistor with Al\(_2\)O\(_3\) dielectric. *Applied Physics Letters* **94**, 062107-062103 (2009).
15. Graphene hotspot movie (online). [http://poplab.ece.illinois.edu/multimedia.html](http://poplab.ece.illinois.edu/multimedia.html).
16. This is partly due to the low emissivity of graphene, and partly because the thin SiO\(_2\) layer is transparent to IR. Hence, the detected IR radiation is a combination of thermal signal from the graphene, and thermal signal from the Si substrate heated by the graphene. By numerical
calculations we find the real graphene temperature rise ($\Delta T$) is proportional to that measured by the IR microscope, and approximately 3 times higher (see Supplementary Information).

17. Pao, H.C. & Sah, C.T. Effects of diffusion current on characteristics of metal-oxide (insulator) semiconductor transistors. *Solid-State Electronics* **9**, 927-937 (1966).

18. Bolotin, K.I. et al. Ultrahigh electron mobility in suspended graphene. *Solid State Communications* **146**, 351-355 (2008).

19. Ghosh, S. et al. Extremely high thermal conductivity of graphene: Prospects for thermal management applications in nanoelectronic circuits. *Applied Physics Letters* **92**, 151911-151913 (2008).

20. Temperature effects on mobility and velocity saturation are neglected here; mobility was found to be relatively independent of temperature in this range, presumably being limited by impurity scattering.

21. Dorgan, V.E., Bae, M.-H. & Pop, E. Mobility and saturation velocity in graphene on SiO$_2$. *submitted to Appl. Phys. Lett.* (2010).

22. Klein, C.A. STB Model and Transport Properties of Pyrolytic Graphites. *Journal of Applied Physics* **35**, 2947-2957 (1964).

23. Lundstrom, M. Fundamentals of Carrier Transport Edn. 2nd. (Cambridge Univ. Press, 2000).

24. Seol, J.H. et al. Two-Dimensional Phonon Transport in Supported Graphene. *Science* **328**, 213-216 (2010).

25. Pop, E., Mann, D.A., Goodson, K.E. & Dai, H. Electrical and thermal transport in metallic single-wall carbon nanotubes on insulating substrates. *Journal of Applied Physics* **101**, 093710-093710 (2007).

26. Pop, E. The role of electrical and thermal contact resistance for Joule breakdown of single-wall carbon nanotubes. *Nanotechnology* **19**, 295202 (2008).

27. Ong, Z.-Y. & Pop, E. Molecular dynamics simulation of thermal boundary conductance between carbon nanotubes and SiO$_2$. *Physical Review B* **81**, 155408 (2010).

28. To calculate $I_D-V_{SD}$ curves, we obtain $\mu_0$ and $n_{pd}$ by fitting measured $R-V_{GD-0}$ curves. In experiments, the Dirac voltage ($V_0$) may shift after IR measurements due to current annealing, also noted in Refs. 9 and 31. However, fitting $R-V_{GD-0}$ curves before and after IR measurements give nearly the same mobility, $\mu_0 = 3500 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ($n_{pd} = 1.45 \times 10^{11} \text{ cm}^{-2}$) and
\( \mu_0 = 3640 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \) \( n_{pd} = 1.31 \times 10^{11} \text{ cm}^{-2} \), respectively, and this stability is provided by our PMMA passivation (see Supplementary Information, Fig. S8).

29. Lee, E.J.H., Balasubramanian, K., Weitz, R.T., Burghard, M. & Kern, K. Contact and edge effects in graphene devices. *Nature Nano* 3, 486-490 (2008).

30. Mueller, T., Xia, F., Freitag, M., Tsang, J. & Avouris, P. Role of contacts in graphene transistors: A scanning photocurrent study. *Physical Review B* 79, 245430-245436 (2009).

31. Connolly, M.R. et al. Scanning gate microscopy of current-annealed single layer graphene. *Applied Physics Letters* 96, 113501-113503 (2010).

32. Avouris, P., Freitag, M. & Perebeinos, V. Carbon-nanotube photonics and optoelectronics. *Nature Photonics* 2, 341-350 (2008).

33. Castro, E.V. et al. Biased Bilayer Graphene: Semiconductor with a Gap Tunable by the Electric Field Effect. *Physical Review Letters* 99, 216802-216804 (2007).

34. Adam, S. & Das Sarma, S. Boltzmann transport and residual conductivity in bilayer graphene. *Physical Review B* 77, 115436-115436 (2008).

35. We note that the bilayer simulations here are not very sensitive to the value of \( E_{OP} \) in the range 60-180 meV.

36. Tenbroek, B., Lee, M.S.L., Redman-White, W., Bunyan, R.J.T. & Uren, M.J. Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques. *IEEE Transactions on Electron Devices* 43, 2240-2248 (1996).

37. Su, L.T., Chung, J.E., A., A.D., Goodson, K.E. & Flik, M.I. Measurement and modeling of self-heating in SOI NMOSFETs. *IEEE Transactions on Electron Devices* 41, 69-75 (1994).

38. Jenkins, K.A. & Sun, J.Y.-C. Measurement of I-V curve of silicon-on-insulator (SOI) MOSFETs without self-heating. *IEEE Electron Device Letters* 16, 145 (1995).
Figure 1. Graphene field-effect transistors (GFETs). a, Schematic of GFET and infrared (IR) measurement setup. Rectangular graphene sheet on SiO₂ is connected to metal source (S) and drain (D) electrodes. Emitted IR radiation is imaged by 15x objective. b, Optical images of monolayer (25.2x6 μm²) and bilayer (28x6 μm²) GFETs. Dashed lines indicate graphene contour. c, Sheet resistance vs. back-gate voltage $V_{GD-0} = V_{GD} - V_0$ (centered around Dirac voltage $V_0$) of monolayer (closed points) and bilayer GFETs (open points) at $T_0 = 70$ °C and ambient pressure. d, Imaged (raw) temperature along middle of monolayer GFET at varying $V_{SD}$ and $V_{GD-0} = -33$ V (hole-doped regime). Dotted vertical lines indicate electrode edges. The inset shows linear scaling of peak temperature with total power input. Temperature rise here is raw imaged data ($T_{raw}$) rather than actual graphene temperature (see Fig. 2 and Supplementary Information).
Figure 2. Electrostatics of monolayer GFET hot spot. Imaged temperature map at a, \( V_{GD-0} = -3.7 \) V (hole doped), b, 3 V (ambipolar), and c, 12.2 V (electron doped conduction) with corresponding \( V_{SD} = 10 \) V, 12 V, and 10 V, respectively (approximately same total power dissipation). d-f, Charge density (upper panels, simulation) and temperature profiles (lower panels) along the channel, corresponding to the three imaged temperature maps. Symbols are temperature data, solid lines are calculations. Arrows indicate calculated (red) and experimental (black) peak hot spot position, in excellent agreement with each other and consistent with the position of lowest charge density predicted by simulations. g-i, Corresponding \( I_D - V_{SD} \) curves (symbols: experiment, solid lines: calculation). Temperature maps were taken at the last bias point of the \( I_D - V_{SD} \) sweep.
Figure 3. Electrostatics of bilayer GFET hot spot. Imaged temperature map of bilayer GFET for a, $V_{GD-0} = -42$ V, b, -12 V, and c, 25 V with corresponding $V_{SD} = -14.5$ V, -20 V and 15 V, respectively. d-f, Electron and hole density (upper panels, simulation) and temperature profiles (lower panels). Symbols are experimental data, solid lines are calculations. Arrows indicate calculated (red) and experimental (black) hot spot position, in excellent agreement with each other, and with the position of lowest charge density as predicted by simulations. g-i, Corresponding $I$-$V$ curves (symbols: experiment, solid lines: calculations). Temperature maps were taken at the last bias point of the $I$-$V$ sweep. The temperature profile of the bilayer GFET is much broader than that of the monolayer (Fig. 2), a direct consequence of the difference in the band structure and density of states (Fig. 2i and Fig. 3i insets).
Supplementary Information

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This section contains:

1. Sample Fabrication and Experimental Setup
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1. Sample Fabrication and Experimental Setup

We use mechanical exfoliation to deposit graphene onto 300 nm SiO\textsubscript{2} with n+ doped (2.5×10\textsuperscript{19} cm\textsuperscript{-3}) Si substrate, which also serves as the back-gate.\textsuperscript{1} The substrate is annealed in a chemical vapor deposition (CVD) furnace at 400 °C for 35 minutes in Ar/H\textsubscript{2} both before and after graphene deposition.\textsuperscript{2} Graphene is located using an optical microscope with respect to markers, confirmed by Raman spectroscopy as shown in Fig. S1,\textsuperscript{3} and GFETs are fabricated by electron-beam (e-beam) lithography, as shown in Fig. 1. Electrodes are deposited on the graphene by e-beam evaporation (0.6/20/20 nm Ti/Au/Pd). An additional e-beam lithography step is used to define 6 μm wide graphene channels, followed by an oxygen plasma etch. A 70 nm PMMA (polymethyl methacrylate) layer covers the samples to provide stable electrical characteristics. Electrical and thermal measurements are performed using a Keithley 2612 dual channel source-meter and the QFI InfraScope II infrared (IR) microscope, respectively. IR imaging is performed with the 15× objective which has a spatial resolution of 2.8 μm, pixel size of 1.6 μm, and temperature resolution ~0.1 °C after calibration.\textsuperscript{4} All measurements are made with the IR scope stage temperature at \(T_0 = 70\) °C.

2. Raman Spectroscopy and IR Imaging of GFETs

2-A. Raman Spectroscopy

The difference in the electronic band structure of monolayer and bilayer graphene can be detected by a shift in the Raman spectrum 2D band. Additionally, the 2D band Raman spectra of monolayer and bilayer graphene exhibit a single peak and four peaks respectively. In this study, Raman spectra were ob-
tained using a Jobin Yvon LabRam HR 800-Raman spectrometer with a 633 nm laser excitation (power at the object: 3 mW, spot size: 1 μm) and a 100x air objective. Spectra were collected in eight iterations for 16 seconds each. Figure S1 shows the Raman spectra obtained from the GFETs in Fig. 1b, which are monolayer and bilayer GFETs respectively. The Lorentzian fit with the single peak in Fig. S1 gives us a peak frequency of 2643.9 cm$^{-1}$ and a full width at half maximum of 33.6, in agreement with previous findings. In Fig. S1b, a fit result (red curve) for the spectrum of the second sample gives us four relatively shifted peak positions (green curves) with respect to the average frequency of the two main peaks: -56.74, -10.38, 10.38, and 29.71 cm$^{-1}$. These are consistent with previous reports in bilayer graphene.

2-B. Infrared (IR) Imaging of GFETs with the InfraScope II

The InfraScope II with a liquid nitrogen-cooled InSb detector provides thermal imaging over the 2–4 μm wavelength range, and working distances of about 1.5 cm with the 15x objective. Thermal mapping with is achieved by sequentially capturing images under different bias conditions. Therefore, the sample is mechanically fixed to the stage to prevent movement during measurements. The InfraScope sensitivity improves with increasing base temperature ($T_0$) of the stage because the number of photons emitted increase as $T_0^3$. However, high temperatures can create convection air currents, resulting in a waved image. Therefore, the recommended stage temperature is between 70 and 90 °C.

Before thermal mapping the GFET, the sample radiance is acquired at the base temperature with no applied voltage ($V_{GD} = V_{SD} = 0$ V). The radiance image is used to calculate the emissivity of the sample at each pixel location before increasing the $V_{SD}$ bias. Figure S2 shows the emissivity image of (a) monolayer and (b) bilayer GFETs, where light blue colored regions indicate electrodes. After acquiring a radiance reference image, an unpowered temperature image is acquired to confirm the set-up as shown in Fig. S3a, where the temperature error is approximately ±0.5 °C. With these pre-conditions, we took thermal images under various applied voltages (Fig. S3b).

The emissivity of the metal electrodes must be considered in order to resolve their temperature. For example, since the emissivity of polished Au is ~0.02 between $T = 38$–260 °C, QFI recommends a background stage temperature between 80 and 90 °C. In our experiment, we used electrodes with Pd (20 nm) on top of an Au layer (20 nm) to increase the resolution of the instrument over the contacts (the emissivity of Pd is ~0.17 between $T = 93$–399 °C).
Figure S2. Emissivity image of (a) monolayer graphene and (b) bilayer graphene.

Figure S3. IR microscopy image of monolayer GFET (a) without applied voltage and (b) with $V_{SD} = -12$ V and $V_{GD} = -28$ V at base $T_0 = 70$ °C, where the region taken in (a) is the same region with Fig. S2a (note different scale bars).

3. Heat Generation and Dissipation in GFET

In our simulation code, the temperature profile along the graphene channel is obtained numerically, using the uneven heat generation profile from the electrical transport (described in the main body of the manuscript). However, additional physical insight can be obtained if we consider a simpler scenario of uniform heat generation $Q$ and long fin (longer than carrier scattering lengths) such that ballistic effects may be neglected. In this case, the temperature profile along the graphene can be understood with the simpler one-dimensional fin equation:

$$\frac{d^2T}{dx^2} = \frac{T-T_0}{L_H^2} \frac{Q}{k} = 0$$

Given the geometry of the device, this suggests the temperature distribution has a characteristic spatial (“healing”) length $L_H = (t_oxGkG/kox)^{1/2} \approx 0.2$ μm, where $t_G \approx 0.34$ nm is the graphene thickness and $k_G \approx 600$ Wm$^{-1}$K$^{-1}$ is the graphene thermal conductivity on SiO$_2$. The healing length is a measure of the lateral temperature diffusion from a heat source along the graphene. The small $L_H$ means the local heat generation in the graphene is minimally diffused laterally, and is smaller than our IR scope resolution. In other words, there is little lateral broadening of the hot spot, and the heat flow path is mostly directed downwards through the 300 nm SiO$_2$ layer. Thus, the temperature profile of the graphene qualitatively represents the heat generation profile.
3-A. Infrared Properties of PMMA, SiO$_2$ and Si Layers

Our devices are covered with a ~70 nm layer of PMMA to prevent spurious sample oxidation and significant shift in Dirac voltage ($V_0$) after repeated measurements. The transmittance of PMMA in the infrared has been previously measured and is ~90% for 800 nm thick films in the 2-4 μm wavelengths. Thus, our thinner PMMA films are >99% transparent over our thermal IR imaging range.

To determine the near-infrared optical properties of the thermally grown SiO$_2$ layer and the Si substrate we calculate the wavelength-dependent absorption coefficient of thermally grown SiO$_2$ from the Lorentz-Drude oscillator model$^{10}$ of its near-IR dielectric function. The absorption coefficient is given by $\alpha(\lambda) = \frac{4\pi n_I}{\lambda}$, where $\lambda$ is the wavelength and $n_I$ the imaginary part of the complex refractive index. We also calculated the wavelength-dependent absorption coefficient for doped silicon using the free carrier absorption theory.$^{11}$ The measured input parameters for the carrier density and resistivity of the doped silicon are $2.5 \times 10^{19}$ cm$^{-3}$ and $2.7 \times 10^{-3}$ Ω·cm respectively. The optical depth for SiO$_2$ and Si is given by $1/\alpha(\lambda)$ and is shown in the plots of Fig. S4.

Since the optical depth for SiO$_2$ of near-IR radiation in the region greatly exceeds the thickness of the SiO$_2$ layer (300 nm), we can assume that the SiO$_2$ is effectively transparent. The transparency of SiO$_2$ in this region has been confirmed experimentally by others.$^{12}$ On the other hand, we find that the optical depth for doped Si is much smaller and is of the order of ~10 μm, since the emission spectrum over the 2-4 μm range is heavily weighted toward the longer wavelengths. Moreover, the temperature in the Si is highest near the Si-SiO$_2$ interface, strongly weighing the number of IR imaged photons. Hence, we can assume that the IR Scope is effectively reading a thermal signal corresponding to a combination of the graphene temperature and that of the substrate near the Si-SiO$_2$ interface (see sections 3-B & 3-C below).

3-B. Finite Element Modeling of Heat Spreading in Substrate

In order to relate the imaged temperature with the actual temperature of the graphene transistor, we consider the calculations and schematic in Fig. S5. The thermal resistance of the SiO$_2$ can be written as $R_{ox} = \frac{t_{ox}}{k_{ox}WL} \approx 1417$ K/W underneath the monolayer GFET, where $k_{ox} \approx 1.4$ Wm$^{-1}$K$^{-1}$ is the thermal conductivity of SiO$_2$ in this temperature range.$^{13}$ The thermal boundary resistance between graphene and SiO$_2$ has recently been estimated$^{14}$ at ~10$^{-8}$ m$^2$K/W, however this is a relatively small contribution (66 K/W or ~5%) compared to that from the 300 nm SiO$_2$ below the graphene, and from the silicon wafer.
At the same time, the SiO₂ film is very thin with respect to the lateral extent of the large (W × L = 6 × 25.2 μm²) monolayer graphene device, suggesting insignificant lateral heat spreading within the oxide. Thus, the “thermal footprint” of the graphene at the Si/SiO₂ surface is still, to a very good approximation, equal to 6 × 25.2 μm². This allows us to write another simple model for the thermal spreading resistance into the silicon wafer, \( R_{Si} \approx \frac{1}{(2k_{Si}(WL))^{1/2}} \approx 813 \text{ K/W} \), where \( k_{Si} \approx 50 \text{ Wm}^{-1}\text{K}^{-1} \) is the thermal conductivity of the highly doped substrate equal to 6 × 25 μm. Thus, the “thermal footprint” of the graphene at the Si/SiO₂ interface is once again found to be approximately 3:1, for graphene sheets of our dimensions, on 300 nm SiO₂ thickness.

### 3-C. Real Temperature of Graphene Sheet

When thermal imaging of the graphene (monolayer or bilayer) and the silicon substrate are initially calibrated at the same temperature (\( T_G = T_{Si} \)), the power or radiance over the InfraScope wavelength range (2–4 μm) is the sum of the radiance from the graphene (G) and the silicon substrate (Si), given by \( P_{tot}(T) = P_G(T) + P_{Si}(T) \). In general, the radiance is the integral of the emitted power per unit wavelength from 2 to 4 μm. Hence, the surface temperature as measured by the InfraScope is a function of the radiance i.e. \( T(P_{tot}) \). When the graphene is at the same temperature as the silicon, as during calibration, \( P_G \) can be neglected because its emissivity (\( \epsilon_G \approx 0.023 \) for monolayer and 0.046 for bilayer) is much smaller than that of silicon (\( \epsilon_{Si} \approx 0.6 \), as obtained directly from the InfraScope). Hence, the emissivity as measured by the InfraScope is that of silicon at the same temperature.

However, when the temperature of the graphene increases during Joule heating (\( T_G > T_{Si} \)), the radiation power from the graphene begins to contribute to the detected power in the InfraScope as shown in Figs. S6a (monolayer graphene) and b (bilayer graphene). But, the InfraScope still measures a single surface temperature \( T \) based on the total power emitted by the graphene and the Si surfaces with a single calibrated emissivity (of Si) (see Figs. S6c and d). When the GFET undergoes Joule heating, we estimate the graphene temperature rise to be roughly \( R_{AT} \approx 2.9 \) times the temperature rise in silicon, as discussed in Section 3-B above. Thus, \( T_G = T_{Stage} + \Delta T_G = T_{Stage} + R_{AT} \Delta T_{Si} \) and \( T_{Si} = T_{Stage} + \Delta T_{Si} \), where \( T_{Stage} \) is the

**Figure S5.** Modeling heat dissipation from graphene on SiO₂. (a) Schematic of graphene on \( t_{ox} = 300 \text{ nm} \) SiO₂. The thermal resistance of the oxide (\( R_{ox} \)) and that of the silicon substrate (\( R_{Si} \)) are given in the text. (b) Finite-element simulation of temperature drop across the oxide and silicon, at 0.2 mW/μm² graphene power density. \( T_{Si} \) and \( T_G \) represent the temperature rise at the graphene and silicon surface, with respect to the silicon backside. (c) Cross-section of temperature through the oxide and silicon substrate, at two different graphene power inputs.
stage temperature and $\Delta T_G$ and $\Delta T_{Si}$ are the temperature rise in the graphene and in the silicon, respectively. Therefore, the total radiance over the detectable wavelength range is given by $P_{tot}(T_{Stage} + \Delta T_{IR}) = P_G(T_{Stage} + R_{IR} \Delta T_{Si}) + P_{Si}(T_{Stage} + \Delta T_{Si}) = f(\Delta T_{G})$ where $\Delta T_{IR}$ is the temperature rise measured by the InfraScope i.e. the total radiance is a function of $\Delta T_{Si}$ and thus, a bijective function of $\Delta T_{G}$. However, the relationship between $\Delta T_{IR}$ and $\Delta T_{G}$ does not lend itself to a closed form. So, in practice, $\Delta T_{G}$ as a function of $\Delta T_{IR}$ is determined by first computing the radiance for a given $\Delta T_{IR}$ and then finding the corresponding $\Delta T_{Si}$ and $\Delta T_{G}$ for that computed radiance. In other words, $\Delta T_{G} = f^{-1}(P_{tot}(T_{Stage} + \Delta T_{IR}))$.

Since the InfraScope still uses the Si emissivity to get $\Delta T_{IR}$ based on $P_{tot}$, $\Delta T_{IR}$ is always $> \Delta T_{Si}$. This occurs because the graphene introduces a contribution to the total radiance measured by the InfraScope when $T_G > T_{Si}$. As shown in Fig. S6c-f, we work backwards as explained earlier, and numerically convert the measured temperature to the actual temperature in the graphene based on the Planck radiation law accounting for the different emissivities of three materials (monolayer, bilayer graphene, and Si), and the geometrical factors explained in Section 3-B.

4. Additional Figures
Figure S7. (a) $I_D-V_{SD}$ curve (scattered points) at $V_{GD,0} = -33$ V (a highly hole doped region) of monolayer GFET, which is fitted by two cases: without phonon scattering (blue curve) and with phonon scattering (red curve). (b) $R-V_{SD}$ curve (scattered points) corresponding to (a), where blue and red curves are fit result without and with phonon scattering, respectively. Here, we used $\mu_0 = 3780$ cm$^2$/Vs and $n_{pd} = 1.5 \times 10^{11}$ cm$^{-2}$ V to fit the $R-V_{GD,0}$ curve for the calculations.

Figure S8. Measured $R-V_{GD,0}$ (a) after high-current annealing and collecting IR data from Fig. 2a, where scattered points are experimental data and solid curves are fit results. Numerical fitting to measured $R-V_{GD,0}$ curves give $\mu_0 = 3500$ cm$^2$/Vs and $n_{pd} = 1.45 \times 10^{11}$ cm$^{-2}$ V, showing that repeated thermal cycling did not significantly affect the sample properties.

5. Supplementary References

1. Novoselov, K.S. et al. Electric Field Effect in Atomically Thin Carbon Films. Science 306, 666-669 (2004).
2. Ishigami, M., Chen, J.H., Cullen, W.G., Fuhrer, M.S. & Williams, E.D. Atomic Structure of Graphene on SiO$_2$. Nano Letters 7, 1643-1648 (2007).
3. Ferrari, A.C. et al. Raman Spectrum of Graphene and Graphene Layers. Phys. Rev. Lett. 97, 187401 (2006).
4. QFI Corp., InfraScope II User Manual. http://www.quantumfocus.com (2005).
5. Abdula, D., Ozel, T., Kang, K., Cahill, D.G. & Shim, M. Environment-Induced Effects on the Temperature Dependence of Raman Spectra of Single-Layer Graphene. J. Phys. Chem. C 112, 20131 (2008).
6. http://www.ib.cnea.gov.ar/~experim2/Cosas/omega/emisivity.htm.
7. Mills, A.F. Heat Transfer. (Prentice Hall, Upper Saddle River, NJ; 1999).
8. Seol, J.H. et al. Two-Dimensional Phonon Transport in Supported Graphene. Science 328, 213-216 (2010).
9. Masaki, T., Inouye, Y. & Kawata, S. Submicron resolution infrared microscopy by use of a near-field scanning optical microscope with an apertured cantilever. Review of Scientific Instruments 75, 3284-3287 (2004).
10. Groesse, P., Harbecke, B., Heinz, B., Meyer, R. & Offenberg, M. Infrared Spectroscopy of Oxide Layers on Technical Si Wafers. Applied Physics A: Materials Science & Processing 39, 257-268 (1986).
11. Liebert, C.H. Spectral Emissivity of Highly Doped Silicon. NASA Tech. Memorandum (1967).
12. Philipp, H.R. Optical Properties of Non-Crystalline Si, SiO, SiO$_2$, & SiO$_2$. J. Phys. Chem. Solids 32, 1935 (1971).
13. Lee, S.M. & Cahill, D.G. Heat transport in thin dielectric films. J. Appl. Phys. 81, 2590-2595 (1997).
14. Chen, Z., Jang, W., Bao, W., Lau, C.N. & Dames, C. Thermal contact resistance between graphene and silicon dioxide. Applied Physics Letters 95, 161910-161913 (2009).
15. Asheghi, M., Kurabayashi, K., Kasnavi, R. & Goodson, K.E. Thermal conduction in doped single-crystal silicon films. J. Appl. Phys. 91, 5079-5088 (2002).