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Multi-Inverter Discrete Backoff: A High-Efficiency, Wide-Range RF Power Generation Architecture

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Abstract—Industrial radio frequency (rf) power applications, such as plasma generation, require high-frequency rf power over a wide dynamic power range and across variable load impedances. It is desired in these applications to maintain high efficiency and fast dynamic response. This paper introduces a scalable power amplifier (PA) architecture and control approach suitable for such applications. This approach, which we refer to as Multi-Inverter Discrete Backoff (MIDB), losslessly combines the outputs of paralleled switched-mode PAs, and modulates the number of active PAs to provide discrete steps in rf output voltage. It further employs outphasing among sub-groups of PAs for rapid and continuous output power control over a wide range. In doing so, the architecture can maintain high efficiency and fast rf power control across a very wide backoff range. A device selection and loss optimization method for MIDB architectures is discussed for plasma generation applications. We address the use of GaN FET-based, ZVS class-D PA units, and consider dynamic $R_{ds, on}$ effects and $C_{oss}$ losses typical of GaN FETs.

Index Terms—radio frequency, switched-mode power amplifiers, plasma generation, outphasing, Chireix, GaN HEMTs, ZVS class-D

I. INTRODUCTION

Radio-frequency (rf) power amplifiers (PAs) for industrial applications, e.g. plasma generation for semiconductor processing equipment, operate into variable load impedances at high frequency (e.g. tens of MHz) and power levels (e.g. peak power in kWs), and often with wide overall power ranges and high peak-to-average power ratios. To meet the evolving needs for semiconductor processing, goals for rf PAs in these applications include (1) operation over a wide load impedance range (as determined by the plasma load); (2) operation across a very wide output power range (e.g. 100:1 or 20 dB); (3) very fast dynamic response to output commands (e.g. $\mu$s scale); and (4) high peak and average efficiency (to reduce cooling requirements and electricity costs). Unfortunately, meeting all these goals has not been possible to date, and efficiency is often sacrificed in order to meet the other performance metrics, yielding solutions with large size, high power ratings and poor peak and average power efficiency. This paper focuses on a switched-mode rf PA architecture, with associated control and design methods, to achieve both high performance and good efficiency in such applications. The proposed approach also has value in a wide range of rf power applications with similar challenges, such as wireless power transfer, rf heating and welding, radar, etc.

One important method for efficient and fast power control used in the proposed architecture is outphasing, or phase-shift control [1]–[5]. In this technique, the outputs of two or more PAs (or blocks of power-combined PAs) are combined via a lossless network and phase-shifted such that output power is modulated through the variation in the vector sum of combined PA outputs, with individual PAs seeing effective load impedance variations. This approach has the advantage that it enables high-bandwidth output power modulation through rapid variations in phase-shift between PAs (e.g. by modulating relative timing of gate drive waveforms).

However, outphasing alone has two key limitations in the present context. First, because power backoff via outphasing addresses output-current-related losses in PAs, but not voltage-related losses, efficiency declines steeply at low power levels, reducing average efficiency in applications with high peak-to-average power ratios. This occurs because the constituent PAs in an outphasing system operate at reduced load current under power backoff, but still at full voltage. Thus, loss components relating to output current (e.g. conduction losses) reduce with output power, but loss components relating to supply voltage (e.g. device output capacitor losses [6], [7], resonant losses to provide ZVS [8], [9], etc.) do not. Second, because outphasing relies on vector cancellation of the output voltage of PAs for power control, the achievable output power backoff can be limited by timing limitations and/or mismatches between PAs.

To address the limitations of sole reliance on outphasing, the proposed system introduces a second means to control power, proposed herein as the Multi-Inverter Discrete Backoff (MIDB) technique. This technique losslessly combines the outputs of parallel-grouped (or current-combined or voltage-combined) groups of switched-mode PAs, with outphasing among groups of PAs providing continuous and fast-response
control of output power. The key idea of MIDB is that, in addition to outphasing between two vectors of fixed magnitude, by changing the number of active PAs within each PA group, we can get discrete steps in rf output voltage, providing a second means of power control. This enables the outphasing angle to be always kept within a reasonable range, yielding much higher average efficiency and wider backoff range than can be achieved with outphasing alone.

Another technique often used to control output power is supply modulation (also known as drain modulation), where the PA’s supply voltage is varied, typically in a continuous fashion (known as envelope tracking) e.g. in [10], [11]. However, analog envelope tracking suffers from a combination of bandwidth limitations and significant cost and efficiency overheads due to the hardware required to rapidly modulate supply voltage. Discrete drain modulation (e.g. in [11], [12]), on the other hand, switches the PA supply voltage among a number of discrete levels, and hence has less efficiency overhead and greater potential to be integrated with MIDB-based systems. This is because in terms of output power control, both discrete drain modulation and MIDB can provide discrete steps in the magnitude of intermediate rf voltages, which are then outphased. In this paper, we focus on the MIDB architecture as it is highly modular and mitigates the supply generation overhead required by using discrete drain modulation alone for secondary power control.

In summary, the proposed rf PA architecture employs (1) outphasing, for fast-response, continuous output power control, and (2) the MIDB technique, which discretely modulates output power through discrete output voltage modulation, achieved by turning PAs on/off in a PA-group; this may be optionally combined with discrete drain modulation, to further expand the high-efficiency output power range of the system. In doing so, the architecture can maintain high efficiency and fast rf power control across a very wide backoff range.

Discrete power modulation through PA on/off switching has been explored in linear amplifiers for power control [13], [14], however, prior work has not exploited its use in high-efficiency switched-mode power amplification, nor has its use with outphasing among multiple groups of PAs for fine power control. Moreover, systems in the existing literature have not utilized power amplifier on/off switching together with dynamic load matching to achieve high performance across wide operating conditions.

Section II of the paper describes the structure of the proposed power generation system and output power control scheme, Section III analyzes losses in the MIDB PA structure and discusses optimization procedures, simulation results are presented in Section IV and a conclusion is given in Section V.

II. MIDB SYSTEM STRUCTURE AND OPERATION

This section describes the structure of each functional block in the proposed rf power generation system, outlines the control scheme for output power, and briefly discusses the load transformation subsystem.

A. Overview

Fig. 1a shows the high-level structure of the proposed rf power generation system, comprising \( M \) MIDB-based PA blocks, power combined via an \( M \)-way combiner. Fig. 1b shows a more specific implementation, in which two MIDB PA blocks are combined with a lossless combiner. The rest of the paper focuses on this example implementation and details its structure and operating principles.

B. MIDB-Based PA Architecture

The MIDB blocks (shown in Fig. 1b as A & B) are constructed identically, and each consists of a group of parallel-combined rf PAs such that the output voltage of the blocks (\( V_X \) and \( V_Y \)) can be discretely modulated by turning on and off constituent PAs within each block. Fig. 2 illustrates example configurations of such a block, with \( n = 2, 3, \) and 4 PAs per block respectively, dubbed MIDB-\( n \).

The key idea is that, the constituent PAs in a MIDB block are combined with common-mode combiners, such that the currents provided to each PA in the block are identical, and the voltage at the output of the combiner is a weighted sum (e.g. the average) of the individual PA outputs. This can be implemented with, for example, an \( n \)-way interphase transformer, a “wiffle-tree” (or corporate array) of 2-way interphase transformers with quarter-wave-line power combiners, etc. In any of these combining methods, the output voltage of the block is the direct average of individual PA output voltages, and each PA sees identical output current. (One could also implement the dual of this, where all PAs see equal voltage and the output current is summed/weighted-averaged, though this may be generally less desirable as the conduction losses can be higher for this implementation.)

With this system structure, peak output voltage and power is achieved by turning all PAs on, and power can be reduced in discrete steps by turning off (ac grounding) the outputs of PAs simultaneously in blocks A and B. (Treating blocks A and B asymmetrically in terms of PA units turned on and off is also possible.) As shown in Fig. 3, with symmetric on-off control among MIDB blocks, 4 non-zero rf voltage levels are available with the MIDB-4 structure, and after a commanded step change, the output voltage settles very quickly within a couple of rf cycles. This structure is highly modular: if we set the number of PAs per block to 1, the system reduces to a traditional outphasing-only implementation; while by modularly expanding the number of PAs per block to 2 and beyond, we can obtain more discrete rf voltage levels, higher peak power, and broader output power range, etc.

Note that we illustrate the use of common-mode combiners here for their relative ease of modular expansion, however, the system would also function with a variety of different combining structures, including differential-mode combiners, where the output voltage of the block is the difference of individual PA voltage and the output current is the same as the current of an individual PA. Output voltage modulation with differential combiners can therefore be similarly achieved by on/off control of PAs within a MIDB block.
A generalized block diagram of the proposed rf plasma power generation system. A common dc voltage supplies $M$ MIDB PA blocks, which are then multi-way power combined and interfaced with the variable load through an impedance transformer.

(b) A specific implementation of the proposed system which involves 2 MIDB PA blocks. The output voltage from the MIDB blocks $(V_X, V_Y)$ are outphased and combined with a lossless combiner (illustrated here as a Chireix-type combiner with asymmetric compensation, with $m:n$ transformation turns ratio and shunt reactive compensation components $jX_A$ & $jX_B$). The output voltage of the combiner $(V_L)$ interfaces with the variable load $(Z_L)$ through the impedance transformation stage implemented as a tunable matching network (TMN).

Fig. 1: Block diagrams of the generalized PA system and a specific implementation example.

Fig. 2: Example MIDB block configurations with 2, 3 and 4 modular PA units in each block respectively. Note that the combiners are shown here as effectively coupled inductors (the three inductors in Fig. 2b are mutually coupled with -1/2 coupling factor), while realistic combiner implementations may include interphase transformers or transmission-line transformers.

C. Power Amplifier Unit

A power amplifier unit refers to each block labeled “PA” in the example MIDB block configurations shown in Fig. 2. The characteristics of a suitable rf PA for the proposed system includes (1) high efficiency at required switching frequency range (e.g. tens of MHz), (2) capable of efficient a.c. grounding for MIDB control (or other connections as required for turning “off” an individual PA in the context of an MIDB block and combiner), (3) capable of maintaining efficiency with moderate variations in load impedance (for outphasing and for easing requirements on impedance transformation), and (4) capable of fast dynamic response to step change in output power, e.g. in the present context, a step change of outphasing angle or on/off status.

Several candidate PAs exist, such as the ZVS class-D, the single-switch class-E (e.g. in [15]) and the class-\(\Phi_2\) (e.g. in [16]), etc. PAs that are more tolerant of load impedance variations (e.g. resistive load variation) are preferred, in particular, the zero-voltage switching (ZVS) Class-D inverter.
shown in Fig. 4 can maintain ZVS and high efficiency for a moderate load range during output power modulation through outphasing control [8], and is a promising candidate as the PA unit. With this particular implementation, when the PA is “on”, both the top and bottom switch are switching and each conducts for approximately half of a switching period, and when the PA is “off”, the top switch is turned off while the bottom switch conducts constantly, effectively a.c. grounding the output and changing the output voltage of the MIDB block. Other PA implementations are also possible, for example in class-E, class-Φ2 etc., one may require an additional switch to disconnect the PA from the input power supply when the PA is in the “off” state, and the PA transistor itself may be held on to provide the desired ac ground. In the rest of the paper, the discussions on control and loss analysis assumes the ZVS class-D as PA unit.

Fig. 4: A ZVS Class-D inverter. The series Ls − Cc tank selects the fundamental component of the switching node voltage, and the Lzvs − Czvs shunt leg provides additional inductive loading and assists the switches to achieve ZVS even when the load varies within a moderate range.

D. Output Power Control Scheme

In general, the wide output power modulation range is achieved with the combined effects of broad, discrete steps in rf output voltage (through MIDB on/off control) and fine, continuous tuning of rf output voltage (with outphasing between MIDB blocks).

Fig. 5 illustrates the system output power control scheme as a vector graph. The magnitude of the load voltage \( V_L \) directly correlates to the output power \( P_{out} \propto |V_L|^2 \), and can be modulated through the combined effects of outphasing and MIDB modulation. Outphasing provides continuous control as the phase shift can be continuously varied, however, the range in which the PAs can remain efficient is limited. On the other hand, discrete voltage modulation through MIDB on/off configuration covers a very wide output power range, and can be invoked when the system can achieve higher efficiency at a different voltage domain or undergoes large power variations.

For example, suppose the PAs become less efficient at low power levels when the outphasing angle \( \theta \) becomes too small, (e.g. due to reactive loading on the PAs) and the system now operates with all MIDB PAs active, then by grounding a PA in each MIDB block, the same output power is maintained but a higher efficiency can be achieved with an outphasing angle more conducive to desired load range of the PAs.

E. Load Impedance Transformation

If direct interface with a variable load is required (e.g. as presented by a plasma chamber), the system may also include an impedance transformation stage that transforms and matches the variable rf load \( Z_L \) into a particular impedance (or a narrowed range of impedances) desired by the PA architecture. With the power stage designed with some degree of flexibility regarding load impedance variations, this stage may perform less extreme impedance compression, yielding a narrowed range of impedance that can be acceptably presented to the PAs. Doing so enables higher system efficiency and reduces the required over-rating of the PA hardware to accommodate the load range. Depending on the specific application scenarios, different configuration of the load transformation subsystem may be more desirable (e.g. using one or a combination of the techniques discussed in [17]–[20]).

III. LOSS ANALYSIS AND OPTIMIZATION

Focusing on the MIDB-based PA blocks, this section first analyzes the dominant sources of loss, and then gives an optimization procedure for the example implementation of MIDB-based system illustrated in Fig. 1b, with 2-MIDB PA blocks power-combined through lossless Chireix-outphasing, and with modular PAs implemented with GaN-based ZVS class-D inverters as shown in Fig. 4. For simplicity, we assume ideal power combiners and that the TMN perfectly matches the variable plasma load to some fixed real impedance.

A. Loss Analysis

Since typically most of the losses in an rf power delivery system come from its PAs, this subsection performs a first-order simplified loss analysis on a single rf inverter. The goal is to quantitatively guide parameter selections in system level optimizations discussed in Section. III-B.
The dominant sources of losses in a GaN-based ZVS class-D PA are attributed to device output capacitance ($C_{OSS}$) losses $P_{Coss}$, device conduction losses $P_{cond}$, and ZVS inductor and resonant inductor conduction losses $P_{LZVS}$ and $P_{Lr}$ as given in (1).

$$P_{loss} \approx P_{Coss} + P_{cond} + P_{LZVS} + P_{Lr} \quad (1)$$

$P_{Coss}$ can be expressed as (2) where $A$ is the area of the device, $f$ is switching frequency, $V$ is the supply voltage level $K_{Coss}$ is a loss proportionality constant, and $\alpha, \beta$ are switch-dependent constants [6].

$$P_{Coss} \approx K_{Coss} \cdot A \cdot f^\alpha \cdot V^\beta \quad (2)$$

The current passing through the devices mainly consists of two parts, the output current to the load and the current from $L_{ZVS}$ shunt leg. Assuming square-wave voltage at the switching node and using First-Harmonic Approximation (FHA), $P_{cond}$ can be approximated by (3), where $K_{Ron}$ is a device-dependent constant that captures the device on-state resistance’s inverse relationship with area, and $R_L$ is the load, assumed to be real and fixed.

$$P_{cond} \approx K_{Ron} \cdot A^{-1} \cdot V^2 \cdot \left( \frac{2}{\pi^2 R_L^2} + \frac{1}{192 f^2 L_{ZVS}^2} \right) \quad (3)$$

Assuming the ZVS tank only sees square-wave voltage and the series resonant tank only sees output current, $P_{LZVS}$ and $P_{Lr}$ can be approximated by (4) and (5) respectively, where $Q_L$ denotes the inductors’ quality factor at switching frequency.

$$P_{LZVS} \approx \frac{\pi}{96 f L_{ZVS} Q_{LZVS}} \cdot V^2 \quad (4)$$

$$P_{Lr} \approx \frac{4 f L_r}{\pi R_L^2 Q_{Lr}} \cdot V^2 \quad (5)$$

If the PA is commanded to deliver a given output power $P_{out}$, with FHA the relationship between $P_{out}$ and $V$ can be established as (6), and the overall PA efficiency $\eta_{PA}$ expressed in (7).

$$V \approx \sqrt{\frac{\pi^2 R_L P_{out}}{2}} \quad (6)$$

$$\eta_{PA} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (7)$$

Finally, plugging (1-6) into (7), the PA efficiency at given $P_{out}$, $\eta_{PA}$, can be expressed as in (8), with device and topology-dependent constants abstracted out as $K_1 = \frac{f_0}{\pi^2 (2/\beta)^2 (P_{out}/2)^{\beta/2 - 1}}$, $K_2 = K_{Ron}$, $K_3 = \frac{K_{Ron} \pi^2 / (384 f^2 L_{ZVS}^2)}{Q_{LZVS}}$, $K_4 = \frac{3}{192 f^2 L_{ZVS} Q_{LZVS}}$, and $K_5 = 2 \pi f L_r / Q_{Lr}$.

$$\eta_{PA} = \frac{(2/\beta)^2 (P_{out}/2)^{\beta/2 - 1}}{K_1 P_{out} + K_2 + K_3 + K_4 (384 f^2 L_{ZVS}^2)} \quad (8)$$

We observe from (8) that at given $P_{out}$, $\eta_{PA}$ is related to device area, load resistance, and supply voltage. More importantly, since the $C_{OSS}$ loss Steinmetz parameter $\beta$ is $< 2$ for most GaN devices, provided that we can freely design $A$ and $R_L$, the supply voltage should be set at the highest dc voltage level the devices could reliably operate at, typically 400V for 650V-rated devices.

### B. Optimization Procedure

With losses in individual PAs analytically expressed, this subsection addresses system-level behaviors in the MIDB setting, and outlines a general optimization procedure that, with device family, operating frequency and desired output power profile as input, yields the efficiency-optimized MIDB configuration (number of PAs per block) and device area.

1) Outphasing Characteristics: First we discuss the load modulation effects on the PAs during outphasing and the corresponding compensation design and outphasing angle range selection. The uncompensated load admittance curves seen by the two MIDB-based PA blocks during outphasing is shown in Fig. 6. Each block sees a load admittance point on their corresponding curve as described in (9), and the output power of a block can be expressed by (10), where $V_{MIDB-rms}$ is the rms output voltage magnitude of a PA block. Varying $\theta$ from $0^\circ$ to $90^\circ$ results in the MIDB blocks seeing admittances tracing along the curves from $(2/R_L, 0)$ to $(0, 0)$, and adding shunt reactive compensation components $(X_A, X_B)$ shifts the curves vertically based on the added reactances.

$$Y_A = \frac{1}{R_L} (1 + e^{j2\theta}) - j\frac{1}{X_A} \quad (9a)$$

$$Y_B = \frac{1}{R_L} (1 + e^{-j2\theta}) + j\frac{1}{X_B} \quad (9b)$$

$$P_{block} = V_{MIDB-rms}^2 \cdot \Re\{Y_{A or B}\} \quad (10)$$

Generally for rf PAs, the closer the load is to the real axis (dashed line in Fig. 6), the more efficiently the PA operates. However, with variation in $\theta$ both load conductances and susceptances seen by the MIDB block, and hence by the PAs, would change, affecting the system efficiency. This is one of the reasons outphasing alone has a limited range of power modulation where the system remains efficient, and one would typically select the compensation reactances to shift the curves such that the admittances stay close to the real axis for as wide power modulation range as possible, e.g. such that the portion of admittance curves encircled by the dashed red box in Fig 6 is close to the real axis.

In order to ensure output power control continuity over voltage steps, a certain minimum span exists for the range of $\theta$. For all MIDB-modulated voltage levels $\left(\frac{n}{n+1}, \frac{n-1}{n}, \ldots, \frac{2}{n}, \frac{1}{n}\right)$ for MIDB-n), the largest voltage step ratio is 2:1, therefore the admittance range should span at least $[0.4/R_L$ to $1.6/R_L$], i.e., the $\theta$ range $[26.57^\circ, 63.43^\circ]$ should be a subset of the modulation range.

Using the MIDB-4 structure as an example, the peak output power is achieved with all PAs active and $\theta$ selected such that both MIDB blocks see real load admittance of $1.6/R_L$, now suppose a new output power level $1/5$ of the peak power is desired, according to (10) the system can achieve this by turning “off” 2 PAs per block (PA block output voltage magnitude is halved), and select $\theta$ such that $\Re\{Y\} = 1.28/R_L$.

2) Simulation-Based Optimizations: Since the system losses are hard to fully capture using analytical expressions,
down to the actual desired power levels with the
finally scale the simulated output power and total area up or
operation considering average efficiency and power range etc., and
fixed-area device, identify a suitable MIDB system configura-
area selection, we can approach this using simulations with a
optimize a MIDB-based system assuming freedom in device
is a unit-
part of the load admittance.

We employ the loss characteristics of the Panasonic GaN
device family (e.g. PGA26E07BA transistor) for subsequent
modeling and simulations, and target an operating frequency of
13.56 MHz and an achievable power range of 50W to 5kW. For
efficiency optimization, we utilize an example plasma loading
profile (0.2kW for 1ms, 1kW for 1ms, then 5kW for 20
µs).

A key assumption is the linearity of power and losses versus
device area, e.g., if an optimized system with total device area
\( A_{tot} \) achieves peak efficiency \( \eta_{pk} \) at some output power \( P \),
then for the actual target output power \( k \cdot P \), the new optimal
system would comprise \( k \) original systems with \( k \cdot A_{tot} \) total
device area and the same peak efficiency. Here \( k \) is a unit-
less proportionality factor and may be fractional. Therefore to
optimize a MIDB-based system assuming freedom in device
area selection, we can approach this using simulations with a
fixed-area device, identify a suitable MIDB system configuration
considering average efficiency and power range etc., and
finally scale the simulated output power and total area up or
down to the actual desired power levels with the \( k \) factor.

The simulation-based optimization steps are thus as follows:

- Step 1: Start with the PA unit, select a GaN device family,
  and determine supply voltage level \( V \), ZVS inductor
  \( L_{ZVS} \), and dead time \( DT \) combination that achieves
  highest efficiency regardless of output power. From sec-
tion III-A, \( V \) is typically selected at 400V. And \( L_{ZVS} \)
d and \( DT \) can be determined by simulation sweep together
with \( R_L \) for peak achievable efficiency at PA-unit level.

- Step 2: On a system level, determine MIDB configuration
  and outphasing angle for output power levels of interest.
  With the linearity assumption, the ratios between power
  levels are more important than the actual wattage for this
  step. Section III-B1 treats this in detail.

- Step 3: Determine system load (seen by the outphased
  and combined MIDB PA blocks), together with compensation
  components \( X_A \), \( X_B \) that maximizes average efficiency
  \( \eta_{avg} \). A nested simulation sweep is used to find the
  optimal combination of these three parameters.

- Step 4: Normalize simulated \( P_{out} \) to the actual power
  levels and identify candidate MIDB systems. The power
  normalization ratio, times the area of device used in
  simulation, is the optimal area for maximizing \( \eta_{avg} \).

Promising MIDB systems with performance optimized against
the given load profile, along with the desired device area can
thus be shortlisted following these steps.

IV. Simulation Results and Discussion

This section presents simulation results of the MIDB-based
PA architecture for both steady-state operation, to evaluate
system efficiency and achievable power range, and dynamic
operation, to evaluate response speed.

A. Steady-State Simulation Results

Following the optimization procedure given in sec-
tion III-B2, simulations in LTSpice are carried out for MIDB-
2, 3, and 4 systems. MIDB-1, i.e. the outphasing only ar-
rchitecture, is also optimized and simulated as a comparison
baseline. We adopt peak dV/dt loss fitting in [6] for \( C_{loss} \) loss
calculation, and apply a \( 5.5 \times \) scalar on nominal \( R_{ds,on} \)
for devices in active PAs, and a \( 2 \times \) scalar for the conducting
switch when a PA is turned off [21]. We further assume a Q
of 500 for the inductors and ideal common-mode combiners.
All systems are simulated with the same building block PA
units (but with different normalization factor \( k \) discussed in
section III-B2) and optimized towards the same output power
profile (0.2kW for 1ms, 1kW for 1ms, then 5kW for 20
µs).

Fig. 7 plots the efficiency versus normalized output power
curves for the MIDB systems, with vertical lines marking
desired power levels in the load profile. Table I summarizes
key parameters obtained from simulations, where the normal-
ization ratio \( k \) is that discussed section III-B2, and the power
range is defined as the ratio of peak power to the power
level where the system efficiency falls below 30%. Compared
to outphasing only (MIDB-1), MIDB-based systems have
much higher average efficiency \( \eta_{avg} \) and greatly extended
power range, and the low-power efficiencies are significantly

\[
\eta_{PA} \approx \frac{1}{1 + K_1 \cdot A \cdot R_L \cdot V^{\beta - 2} + (K_2 \cdot R_L^{-1} + K_3 \cdot R_L) \cdot A^{-1} + K_4 \cdot R_L + K_5 \cdot R_L^{-1}}
\]
improved. MIDB-3 achieves the highest $\eta_{avg}$, though MIDB-2 is also promising given its lower device count, and MIDB-4 or higher can be considered for further range extension.

B. Dynamic Response Simulation Results

In terms of dynamic response, the system responds to a commanded step change of output power mainly by (1) a change in outphasing angle, or/and (2) a change in MIDB on/off configuration. (1) results in a step change in the effective load impedance seen by the PAs, while (2) leads to a step change in the common-mode voltage across the PA’s dc-blocking components. By distributing resonant tanks to each PA, the architecture is able to achieve very fast settling time in these scenarios by minimizing the dc-blocking capacitor value. Doing so has the additional benefit of fully modularizing the architecture, where the MIDB blocks can be easily re-configured to meet new system specifications.

Fig. 8 shows the simulated dynamic step response of the output voltage of a MIDB-2 PA architecture to outphasing angle, and Fig. 9 shows the simulated dynamic step response of the output voltage of the same MIDB-2 PA architecture to a change in MIDB configuration.

In both cases, the system exhibits very fast dynamic behavior and settles at the new commanded voltage levels within a couple of rf cycles.

V. CONCLUSION

This paper discusses a modular, single-supply-rail MIDB-based PA architecture suitable for rf power applications, such as industrial plasma generation, which maintains high efficiency for a wide output power range and has fast dynamic responses. A systematic optimization procedure is established, which facilitates informed decisions on MIDB design. A system circuit model is developed based on ZVS Class-D PAs, and the simulation results show that for an example load power distribution cycle, MIDB-based systems are estimated to reduce average power loss by more than a factor of two and can extend backoff range by more than 10dB compared to an outphasing only system.

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Fig. 8: Voltage waveforms plotted vs. time showing dynamic response to a step in outphasing angle $\theta$. The red curve corresponds to the output voltage of a 1:1 turns ratio Chireix combiner ($V_L$ in Fig. 1b). The green and blue curves represent the switching node voltage of two PAs, each in a different MIDB block. $\theta$ is stepped from $30^\circ$ to $60^\circ$ at time $= 3.69\,\mu s$ and reverted back to $30^\circ$ at time $= 4.42\,\mu s$, i.e. after approximately 10 rf cycles.

Fig. 9: Voltage waveforms plotted vs. time showing dynamic response to a step in MIDB configuration. The red curve corresponds to $V_L$, and the green and blue curves represents the switching node voltage of two PAs within the same MIDB block. One PA is turned “off” at time $= 3.69\,\mu s$ and then turned back on at time $= 4.42\,\mu s$.

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