FlexSA: Flexible Systolic Array Architecture for Efficient Pruned DNN Model Training

Sangkug Lym  
The University of Texas at Austin  
sklym@utexas.edu

Mattan Erez  
The University of Texas at Austin  
mattan.erez@utexas.edu

Abstract—Modern deep learning models have high memory and computation cost. To make them fast and memory-cost efficient, structured model pruning is commonly used. We find that pruning a model using a common training accelerator with large systolic arrays is extremely performance-inefficient.

To make a systolic array efficient for pruning and training, we propose FlexSA, a flexible systolic array architecture. FlexSA dynamically reconfigures the systolic array structure and offers multiple sub-systolic operating modes, which are designed for energy- and memory bandwidth-efficient processing of tensors with different sizes and shapes. We also present a compilation heuristic for tiling matrix-multiplication-and-accumulation operations in a training workload to best utilize the resources of FlexSA. Based on our evaluation, FlexSA with the proposed compilation heuristic improves compute resource utilization of pruning and training modern CNN models by 37% compared to a conventional training accelerator with a large systolic array. FlexSA also improves on-chip data reuse by 1.7X saving 28% energy compared to naive systolic array splitting.

Index Terms—Deep learning accelerator, data-parallel architecture, systolic array

I. INTRODUCTION

Neural network model pruning is a commonly used technique to make deep learning inference fast and memory-efficient [1]–[4]. It identifies non-critical parameters and removes them from a baseline model such that the pruned model has reduced computation and memory costs. This pruning procedure takes millions of iterations that repeat the process of pruning and retraining [4]–[7] or pruning while training [8]–[11]. We find that commonly used deep learning training accelerators with large systolic arrays [12]–[14] are inefficient in processing these (intermediate) pruned models, which decrease compute unit utilization by 60% in training and pruning modern convolutional neural network (CNN) models. To overcome this inefficiency, we introduce FlexSA, a flexible systolic array design that can reconfigure its structures at runtime to better fit the specific and dynamic workload of pruning DNN models and overcome the inefficiency we observe with standard systolic arrays.

The execution inefficiency without FlexSA is mainly found in processing matrix multiplications and accumulations, which account for more than 95% of the operations in modern deep learning models [16]–[19]. These matrix operations are commonly executed as general matrix multiplies (GEMMs) [20] using high throughput training accelerators. For efficient acceleration of these GEMMs, many modern training accelerators adopt large systolic array cores that are (typically) a two-dimensional mesh of many simple and efficient processing elements (PEs) [12], [21]. Because GEMM dimensions in model training are both large and multiples of the typical systolic array sizes, tiling and processing these GEMMs can fully utilize PEs on systolic arrays. This is shown in Figure 1.a, where the two arrays of gray boxes are input matrices for a tiled GEMM and each red box in the systolic array indicates an active PE.
However, the GEMM dimensions during structured pruning gradually and arbitrarily shrink. Thus, the tiles at the edges of an intermediate pruned GEMMs are not divisible by the size of a systolic array as shown in Figure 1b. Processing these small GEMM tiles does not fully occupy the PEs (white boxes), which significantly decreases the performance. This problem is also known as tile quantization, which seriously degrades performance in DNN training using GPUs [22]. Splitting a large systolic array into multiple small arrays can improve PE utilization (Figure 1c). However, this naive core splitting requires broadcasting inputs to multiple cores. This input replication increases on-chip data traffic, decreasing the energy-efficiency of training and pruning.

To achieve both the high on-chip reuse of using a large systolic array core and the high PE-utilization of using many small cores, FlexSA uses a core with four systolic arrays as the baseline. It adds input and output data paths between the four small cores and their control logic that incurs only 1% area overhead. These design changes enable forming four different systolic array operating modes, which support inter-core collaborative and per-core individual systolic dataflows. These FlexSA modes improve input and output reuse by sharing them between cores, which makes FlexSA modes efficient in dealing with GEMM tiles with different sizes and shapes.

For efficient utilization of the flexible systolic array resources, we propose a compile-time GEMM tiling heuristic. The proposed heuristic prioritizes FlexSA modes that have high inter-core reuse. The FlexSA modes with limited inter-core reuse are chosen only when using them improves PE utilization. Our data shows that this compile-time technique uses inter-core systolic array dataflows more than 89% of the time without decreasing PE-utilization while pruning and training popular modern CNN models. The FlexSA compiler also handles loading inputs to input buffers then to registers and storing GEMM outputs to on-chip global buffers or DRAM at static time according to the type of FlexSA modes. Overall, the proposed FlexSA architecture increases PE utilization by 37% compared to a large systolic array design and improves on-chip data reuse by 1.7X and energy efficiency by 28% compared to a naive many-small-core design.

To summarize, our main contributions are:

- We show that commonly used high throughput training accelerators with large systolic arrays are highly inefficient in processing structured model pruning due to reduced PE utilization.
- We show that naively splitting a large core into many small cores decreases energy efficiency due to reduced on-chip reuse and performance of pruning because of increased memory bandwidth peaks.
- We propose FlexSA, a flexible systolic array architecture that restructures its core structure to support multiple systolic array operating modes for efficient processing of GEMM tiles with different sizes and shapes.
- We propose a compile-time GEMM tiling heuristic that tiles GEMMs into parts that best utilize FlexSA resources. FlexSA with our proposed GEMM tiling heuristic achieves both high data reuse of using a large core and high PE utilization of using multiple small cores.

II. BACKGROUND

In this section, we briefly discuss the background on deep learning applications and training accelerator architectures needed to understand the challenges we focus and our proposed ideas for them.

A. Network Model Training and Pruning

Deep learning applications consist of many layers that have millions of weights (or learning parameters) to learn complex features from a large training dataset. Training needs forward and back-propagating the training dataset through network layers repetitively, which involves trillions of FLOPs (floating-point operations) and memory accesses. Most of these FLOPs are matrix multiplications and accumulations and they are typically processed as GEMMs for simple and efficient processing on high-throughput training accelerators. Training generally uses large mini-batch sizes (a set of input samples propagated at a time per training iteration) thus the GEMMs in training have large data parallelism in all dimensions [23], [24].

Model Pruning Methods. Model pruning has been studied primarily for CNNs (convolutional neural networks), to make their models more compact and their inference fast and energy-efficient. Pruning methods compress a CNN model by removing non-critical (or small-valued) weights by identifying such weights during training [2], [11] or after training using a pre-trained baseline model [4], [11]. They gradually remove non-critical weights by repeating the process of pruning and re-training to minimize its impact on accuracy. Recent prior work prunes weights during training to save not only the cost for inference but also for training [8], [10]. They regularize weights to small values then prune the weights whose absolute values are under a small threshold. For both approaches, pruning happens gradually thus training accelerators have to deal with both the baseline model and (intermediate) pruned models.

These pruning algorithms can be unstructured or structured. Unstructured (or individual-weight) pruning can maximize model-size reduction but requires fine-grained indexing with irregular data access patterns. Such accesses and extra index operations lead to poor performance on deep learning accelerators with vector or matrix computing units despite the reduced number of weights and FLOPs [25]–[27].

On the other hand, structured pruning algorithms remove or reduce fine-grained indexing and better match the needs of hardware and thus effectively realize performance gains. Channel pruning is the most commonly used structured pruning technique for CNNs [5], [7], [8], [11], [28]–[30]. It removes weights at the granularity of channels. This reduces one of three GEMM dimensions (width, height, and depth) of each convolution layer reducing its data parallelism.

To understand the challenges we face and our proposed ideas for them.
B. Systolic Arrays

Training accelerators are designed to minimize training time thus requires high compute throughput. To efficiently process

GEMMs in training workloads using a large number of PEs while avoiding redundant memory accesses, many modern

training accelerators (e.g., Google’s TPU [12], Intel’s Nervana

NPP [13], and Tesla’s AI chip [14]) adopt systolic arrays. A

systolic array (Figure 2) is a two-dimensional mesh of many

simple and efficient PEs. At each cycle of kernel execution,

each PE applies the same computation to its inputs and then

passes the computed result or its unmodified inputs to one

or more of its neighbors. All PEs communicate only with

adjacent PEs such that there is minimal data movement and

high computational concurrency [31]. A GEMM is tiled such

that each tile is processed fully within the systolic array. Ideally the tile is sized to exactly fit the array and fully

utilize its PEs. Tiles are scheduled according to a fixed systolic
dataflow. Input- and output- stationary systolic dataflows are

the most commonly used ones and achieve high in-core input

and output reuse, respectively [32].

Computation of systolic dataflows consists of piping inputs from the top and left edges of the array (in our example)
and obtaining results at each PE or at the bottom of the
array depending on the dataflow type. Figure 2 shows the
operation of input-stationary dataflow, where one of the two
input matrices for a GEMM tile is pre-loaded at each PE
then the other input matrix is shifted horizontally. Executing
a GEMM tile is further blocked by the local input buffer
size, processing m at a time. We call this blocked systolic
computation batch a systolic wave.

III. ARCHITECTURAL CHALLENGES OF
MODEL PRUNING

Channel pruning is done by retraining a pre-trained dense
model or pruning while training from scratch. In both cases,
training accelerators have to deal with both dense and (inter-
mediate) pruned models. Unlike unpruned models that typi-

cally have a regular number of channels, such as 64, 128, or

256 (powers of two) [33−35], their channel-pruned versions

have an irregularly reduced number of channels (e.g., 3, 71).
The GEMMs converted from such channel-pruned convolution
and FC (fully-connected) layers also have severely reduced
sizes. Tiling such GEMMs to large systolic array cores can be
inefficient: many GEMM tiles have sizes smaller than the size
of a large systolic array (e.g., 128×128). Thus processing these
tiles does not fully utilize the PEs in the systolic array. This
causes severe compute resource underutilization and limits
training time saving even with large FLOPs reduction by
continuous pruning.

To show the low efficiency of a large systolic array for
training pruned CNN models, we prune ResNet50 [15], the
most commonly used CNN model for image classification,
while training. We use the WaveCore training accelerator, dis-
cussed by Lym et al. [21], which executes GEMM tiles using
128×128 systolic arrays using the input-stationary dataflow,
similar to Google’s TPU v3 [36]. We use PruneTrain, which
regularizes parameters in each channel to zero as a mechanism
to prune channels during training [3]. Figure 3 shows the exec-
tution time per training iteration over the process of pruning-
while-training using WaveCore. Each bar shows only the sum
of convolution and FC layer execution time considering that
they account for >98% of the FLOPs in a training iteration.
The training iteration time is normalized to that of the baseline
before pruning. In this experiment, we use a pruning interval of
10 epochs and the two figures show the results of using different
pruning strengths as introduced in PruneTrain: low
pruning strength that removes relatively few channels with
only a small accuracy loss (top), and high pruning strength that removes more channels with a larger accuracy loss (bottom). We evaluate this using an instruction-level simulator that we develop.

The figures show two bar graphs: the blue bars (\textit{IDEAL}) indicate the execution time with the assumption of 100\% PE utilization and the red bars (\textit{ACTUAL}) show the increased execution time caused by PE underutilization. All bars are normalized to the execution time of the unpruned baseline (the left-most red bar in each figure). The black line in each figure indicates the PE utilization at each pruning interval. The PE underutilization is solely caused by the size mismatch between GEMM tiles and the systolic array and is estimated with ideal (infinite) memory BW.

As the blue bars show, PruneTrain gradually reduces the FLOPs of the unpruned baseline model to 48\% and 25\% when using the low and high pruning strengths, respectively. However, due to the large systolic array size and reduced GEMM dimensions in many convolution layers, PEs become highly underutilized as pruning proceeds and exhibit overall PE utilization of only 69\% and 58\% for the low and high pruning strengths, respectively. Also, even the baseline model shows only 83\% PE utilization and this is because some early convolution layers have a small number of channels.

\section{Naive GEMM Core Splitting}

\textbf{Diminishing PE Utilization and Increasing Input Load Cost.} The PE underutilization caused by small GEMM dimensions can be mitigated by splitting a large systolic core into multiple small cores. GEMMs can be tiled into smaller parts then executed with higher PE occupation on the smaller cores. However, this many-small-core design can be inefficient in processing large GEMM tiles, which still account for most GEMM tiles in both pruned and unpruned CNN layers. First, small cores have low in-core input reuse compared to a large core, which increases input traffic from memory or the global buffer. Second, having more cores increases the area complexity of wires, data path switches, and SRAM buffer control and decoding logic.

To study the relationship between the core size and PE utilization, we conduct an experiment that estimates overall PE utilization and the volume of on-chip data traffic while pruning ResNet50 during training with PruneTrain. The baseline accelerator design used in this experiment has a group of systolic array cores sharing one global buffer (GBUF) (Figure 4(a)). The GBUF is used to block GEMM inputs and share them among cores. The evaluation is done with different core configurations, which are the points on the X-axis of Figure 5 indicating \#cores \times core size. This baseline design also has a pair of local buffers (LBUFs) in each core for input double buffering to hide input load latency. The blue lines in Figure 5 show PE utilizations and the red lines show the average data traffic volume between the GBUF to LBUFs when using low (solid lines) and high (dotted lines) pruning strengths. Both PE utilization and data traffic volume are averaged across training iterations over the whole training run, thus they encapsulate the results of the baseline unpruned model and many different intermediate pruned models. We use ideal memory BW to show the PE underutilization caused solely by the size mismatch between GEMM tiles and the core.

Splitting one 128 \times 128 core into four 64 \times 64 improves PE utilization by as much as 23\% but it also increases input load traffic by 1.7 \times due to reduced input reuse. Further splitting the cores yields diminishing PE utilization improvement but continues to increase data traffic. Using 16 \times (32 \times 32) and 64 \times (16 \times 16) cores improves PE utilization by only 8\% and 4\% but increases input load traffic by 3.4 \times and 6.6 \times. Also, 32 \times 32 and 16 \times 16 cores show almost similar PE utilization for the two ResNet50 pruned using different pruning strengths. This indicates that small cores do not necessarily improve the PE utilization of the more aggressively pruned CNN models. \textit{Overall, this result shows that reducing the core size to less than 32 \times 32 is not cost-efficient.}

\textbf{High Area Overhead of the Many-Small-Core Design.} The increased data traffic of small cores requires higher on-chip data BW: when the core count increases by 4 \times, the peak on-chip data BW required increases by 2 \times. The impact of increasing input BW is different depending on the accelerator...
The overhead of data paths is estimated conservatively assuming the wires do not overlap with logic (so the actual overhead should be smaller). The increase in chip width and height from additional data paths is estimated by distributing the wires to 5 metal layers using a wire pitch of 0.22um, similar to the method used by DaDianNao [41]. The overheads of different core configurations are normalized to the area of a single 128×128 core.

Splitting a single core to 4 (64×64) cores has a relatively small area overhead of 4%, and this (b) mainly comes from doubling the data paths by having cores share a GBUF. Further splitting them to 16 (32×32) cores increases area overhead to as much as 13%, where the overhead for dividing a GBUF to four parts is added (c). Finally, 64 (16×16) cores have a 23% area overhead. The additional area overhead comes from increasing the number of cores sharing a GBUF in each group. Overall, this experiment shows that splitting a large core is not scalable. Especially, splitting a core into ≥16× small cores is not an area-efficient design option.

In summary, naively splitting a large core into many small cores improves PE utilization but its gain diminishes as the splitting factor increases. In addition, the many-small-core design increases total traffic from the GBUF due to the reduced in-core input reuse and also requires high area overhead. To better balance these tradeoffs, a new systolic array core architecture is needed to maintain high input reuse as using a large core and achieve high mapping flexibility as when using multiple small cores.

V. FLEXIBLE SYSTOLIC ARRAY

In this section, we introduce a systolic array architecture that achieves both high PE utilization and low on-chip traffic in processing (partially) pruned CNN models.

A. FlexSA Core Architecture

To map small GEMM tiles to cores with high PE utilization, splitting a large core into smaller cores is unavoidable. However, processing a large GEMM tile using multiple small cores is inefficient as this increases on-chip data traffic between GBUFs and cores. Especially, this becomes a critical problem as GBUF access costs grows with the size of the systolic array. To take advantage of the benefits of both a large core and multiple small cores, our idea is to use a group of small cores that collaborate when processing a large GEMM tile and work independently when processing small GEMM tiles. To this end, we propose FlexSA, a flexible systolic array architecture that meets the need for both high input reuse and PE utilization.

Figure 7 shows the logical structure of FlexSA. FlexSA is based on four systolic array cores sharing a GBUF, as illustrated in Figure 4a. However, unlike the baseline four-core design, where each core always operates independently, FlexSA can reconfigure its operation mode such that the four cores work independently or collaboratively. FlexSA provides four different operating modes and they are supported using additional data paths and path switches (red data paths in Figure 4).

Sub-Array Operations. The four different systolic operating modes are illustrated in Figure 8. FW (full wave) uses the four cores as a single systolic array by sharing inputs and passing partially accumulated outputs between cores (Figure 8a). First, the inputs are vertically shifted from the LBUF on top of each core. These inputs are all unique and they are pre-loaded to each PE for the input-stationary systolic dataflow. Compared to a single large systolic array, this saves half the input shifts due to the reduced core height. Next, both cores 0 and 2 pass
the inputs shifted from the left LBUFs to core 1 and 3 for reuse in multiplication and accumulation operations (with the stationary inputs pre-loaded in core 1 and 3). At the same time, cores 0 and 1 pass their outputs (partial sums) directly to cores 2 and 3 for output reuse. Because the reuse of both vertically and horizontally shifted inputs is the same as the large core, FW has half the on-chip traffic compared to a naive independent four-core design.

FlexSA supports two systolic sub-array operations that use two pairs of cores independently. First, VSW (vertical sub-wave) forms two vertical systolic sub-arrays by paring the two cores in each column (cores 0 and 2 for one sub-array and cores 1 and 3 for the other as shown in Figure 8b). This mode is designed for efficient processing of skinny GEMM tiles in parallel whose tile width is smaller than or equal to the width of one small core. VSW starts by pre-loading the same inputs to each of the two vertical sub-arrays. To reduce the cost of sending identical inputs from GBUF to the LBUFs of both sub-arrays, we construct switchable data paths between the LBUFs of cores 0/2 and 1/3 for local broadcast. After pre-loading the stationary inputs, the other inputs are horizontally shifted to each sub-array. To provide different inputs to each sub-array in parallel, VSW uses the additional horizontal data paths. VSW uses only half of the output buffers, as shown in Figure 8b. Therefore, it is possible to interleave two VSWs that use the same stationary inputs but different horizontally shifted inputs. Overall, VSW improves PE utilization by executing two skinny GEMM tiles in parallel and also improves stationary input reuse by 2× through local broadcasting.

Second, HSW (horizontal sub-wave) constructs two horizontal systolic sub-arrays by paring the two cores in each row (cores 0/1 for one sub-array and cores 2/3 for the other as shown in Figure 8c). HSW is designed for efficient mapping of fat GEMM tiles whose accumulation depth is smaller than or equal to the height of one small core. HSW first pre-loads the same stationary inputs to each horizontal sub-arrays. Then, the other inputs are shifted from the left LBUFs through both paired cores in each row. Similar to the local input sharing used in VSW, we construct a direct data path between the input buffers of cores 0/1 and cores 2/3 to avoid duplicated input transfers from the GBUF. The outputs from cores 0 and 1 are directly stored and accumulated at the output buffers at the bottom of cores 2 and 3. Overall, HSW improves PE utilization by processing two fat GEMM tiles in parallel and doubles the reuse of horizontally shifted data compared to using small cores individually.

Lastly, FlexSA supports full independent core operation by providing unique inputs to each core as shown in Figure 8d, which we call ISW (independent sub-wave). This mode helps maintain high PE utilization when both GEMM tile width and accumulation depth are small. ISW provides independent

Fig. 7: FlexSA architecture.

Fig. 8: Four different systolic sub-array operations supported by FlexSA and the micro-architecture settings for each mode. Buffers with different colors hold inputs and outputs of different waves. The color gradients indicate that inputs in the buffers are shared between two waves.
inputs horizontally to cores 1 and 3 using the additional data path 1 and the outputs of core 1 and 2 are sent to and accumulated at the output buffers using the added vertical data path 2. Compared to the independent core design, ISW exhibits lower input loading cost because FlexSA locally broadcasts the stationary inputs between cores. This saving is possible because the FlexSA compiler schedules waves sharing one of the two inputs in parallel rather than processing waves with all different inputs (we will discuss this in Section VI). However, since the input reuse of ISW is the lowest among all modes, other sub-array modes should be prioritized over ISW for cost-efficient execution.

B. Area Overhead Estimation

FlexSA requires additional area for logic and data path wires and switches. We estimate area in 32nm technology and we compare the overhead relative to the naive four-core design. Again, we conservatively estimate the area overhead of additional data paths assuming they do not overlap with logic. First, the addition of data path switches (1:2 MUXs) that select inputs and partial sums increase logic area by only 0.03mm$^2$. Second, FlexSA requires each PE at the top row of cores 2 and 3 to support a mixed-precision FMA (fused multiplier and adder) instead of just a 16-bit multiplier to accumulate the partial sums shifted from cores 0 and 1. This change increases the area by 0.32mm$^2$. Third, the repeaters to drive signals over a core add 0.25mm$^2$, where we use fanout of 32. The vertical wires connecting the outputs of cores 0 and 1 to the output buffers expand the width of the core by 0.09mm. However, the other wires do not affect die size because they are effectively canceled by the wiring overhead of connecting GBUFs and the LBUFs in the baseline four-core design.

Overall, FlexSA increases the die area over the naive four-core design by only 1%. This area estimate is conservative and placing the newly added vertical wires over PE array (as illustrated) can effectively hide the wiring area overhead. This is feasible because PE arrays use only a few low-level metal wires for local routing.

Design Scalability. It is possible to form a FlexSA unit using more than four cores. However, we present only the four-core design for three reasons. First, the performance benefit diminishes as we further split the cores to a larger number of smaller cores as shown in Figure 5. Second, grouping more than four cores incurs significantly higher overhead area. This area is for the larger number of wires, data switches, and repeaters required for constructing many independent sub-arrays. Instead, we propose to construct multiple FlexSA units with four cores, which incurs no additional area overhead, making it scalable. We use this multi-FlexSA design to evaluate model pruning in Section VIII.

VI. FLEXSA COMPILATION AND GEMM TILING

FlexSA mode selection is crucial for efficient GEMM processing. Modes should be selected to achieve the highest PE utilization with minimum on-chip data traffic. Mode selection is coupled with GEMM tiling because different modes are optimal for GEMM tiles with different shapes.

In this section, we introduce a compile-time GEMM tiling heuristics that tile a GEMM into systolic waves to best utilize FlexSA resources such that it achieves both high performance and energy efficiency. Here, a wave the GEMM execution granularity using the systolic array defined in Section II. The systolic waves are mapped to systolic array cores and executed using different FlexSA modes. Different modes require different micro-controls, such as data path selection, input shifting, output shifting, and partial sum accumulation. For efficient communication between software and the FlexSA micro-architecture, we introduce a set of instructions that define the micro-controls needed for each FlexSA mode and that handle data transfers between on-chip buffers.

A. GEMM Tilting Heuristics

The proposed compile-time GEMM tiling heuristics choose waves that are executed on FlexSA with the highest PE utilization and in-core data reuse. In other words, systolic waves that use the FlexSA modes with greater input reuse are prioritized and the waves using the FlexSA modes with lower input reuse are chosen only when using them improves PE utilization (i.e., FW > HSW = VSW > ISW).

GEMM Tiling Conditions for FW. The proposed heuristics tile a large GEMM into multiple waves to process them on the cores of FlexSA. The tiling factors of all GEMM dimensions ($blk_M$, $blk_N$, and $blk_K$ in Figure 9.a) are chosen to match the size of a full FlexSA (all four cores of FlexSA) to maximize reuse by utilizing the FW mode. The sizes of $blk_N$ and $blk_K$ are equal to the width and height of a full FlexSA core, both of which are 128 in our baseline design. The size of $blk_M$ is the size of the LBUF for non-stationary inputs (LBUFs on the left side of FlexSA in Figure 7) divided by the height of a full FlexSA core.

Because GEMM dimensions are not always a multiple of the ideal tile size, the execution of some tiles with FW would degrade utilization and performance. Such tiles (typically just the edge tiles of a large GEMM) are executed with the other FlexSA modes as shown in Figure 9 and discussed below.

GEMM Tiling Conditions for HSW. When the $blk_K$ size of a systolic wave is small, using FW under-utilizes PEs and slows down the GEMM execution. Thus, when the size of $blk_K$ is smaller than or equal to the height of one FlexSA core (a sub-core of FlexSA), the proposed heuristics execute the systolic wave using HSW as shown in Figure 9.b. By executing a single fat wave as two independent waves using the two horizontal sub-systolic arrays, HSW increases PE utilization by 2X.

GEMM Tiling Conditions for VSW. Tiles at the GEMM edges can have small block sizes in the $blk_N$ dimension and executing the systolic waves of these skinny tiles using FW also under-utilizes PEs. Therefore, when the $blk_N$ is smaller than or equal to the width of one FlexSA core, the heuristics execute the waves of the skinny GEMM tiles using VSW as shown in Figure 9.c. This improves PE utilization by executing
the waves of two small GEMM tiles in parallel using the two vertical sub-systolic arrays. In particular, this skinny GEMM tile is executed using two VSW operations (VSW1 and VSW2 in Figure 9c) that can be interleaved, accumulating their results using half of the output buffers. Because the two VSW operations share the stationary inputs, this achieves additional 2X stationary input reuse.

GEMM Tiling Conditions for ISW. When both blk_N and blk_K are smaller than the width and the height of one FlexSA core, respectively, the proposed heuristics execute the systolic waves using ISW. ISW executes a GEMM tile using four small independent waves, which operate in parallel to achieve high PE utilization (Figure 9d). When a pair of VSWs precedes ISW like the case of Figure 9c followed by Figure 9d, the four small systolic waves executed by ISW accumulate their results with the partial sums pre-stored in the output buffers.

B. ISA Support and Compilation for GEMM Processing

To execute the systolic waves using FlexSA, ISA support is necessary. First, an instruction to define the configurations of each FlexSA modes is needed. This instruction provides the type of FlexSA mode and the sizes of each wave’s blk_M, blk_N, and blk_K. This information is mapped to the micro-controls required to execute these waves such as data path selection, input shifting, output shifting, and accumulation. Second, vector load and store instructions are needed for efficient data transfers between the GBUF (global buffer) and LBUFs (local buffers). Using vectors reduces instruction count and instruction decoding BW, compared to using word-granularity instructions. The compiler generates memory access routines that load inputs to the LBUFs of cores and store the GEMM outputs to the GBUF or off-chip memory using these vector instructions.

Algorithm 1 shows how the FlexSA compiler processes a GEMM: generating instructions for data loading and FlexSA model selection. The compiler tiles the GEMM and schedules waves to process each GEMM tile. The type of each FlexSA mode is determined by the shape of the current systolic wave (IsWideWave and IsTallWave).

Before executing each wave (or waves in parallel), inputs for the wave(s) are loaded from the GBUF to LBUFs of FlexSA cores. For this, two vector load instructions (LdLBUF_V and LdLBUF_H) are used. These vector load instructions take address pointers for GBUF and LBUFs, and the size of the data to load. The LBUFs are double buffered to hide the access and transfer latency. Thus, the inputs to be used in the next systolic wave are pre-fetched while executing the current wave. Once stationary inputs are fully loaded at LBUFs, they are shifted to PEs using a ShiftV instruction. ShiftV takes a number of shifts and this is determined by the height of a wave. Using a separate instruction for stationary input shifting decouples it from the main systolic wave execution step and makes it parallel to loading non-stationary inputs to the LBUFs, removing unnecessary execution step serialization within a wave.

When both inputs are ready, an ExecGEMM instruction executes the target systolic wave using the selected FlexSA mode. ExecGEMM takes four inputs: the type of FlexSA mode and the sizes of the wave dimensions (blk_M, blk_N, and blk_K). For HSW, VSW, and ISW, the sizes of these wave dimensions indicate those of each independent wave. When GEMM tile execution is complete after iterating over the K dimension (processing all waves of a GEMM tile), the outputs...
accumulated at the OBUFs (output buffers) are stored to the GBUF using a \textit{SilBUF} instruction.

VII. EVALUATION METHODOLOGY AND BASELINE SCHEDULING POLICY

We develop an instruction-level architecture simulator to evaluate the performance and energy efficiency of FlexSA. We use three popular modern CNN models for evaluation: ResNet50, Inception v4 [17], and MobileNet v2 [42].

ResNet50 is pruned during training using PruneTrain as the pruning mechanism with two different model-pruning strengths. Inception v4 is artificially pruned by applying the same pruning statistics of ResNet50. In case of MobileNet v2, we compare the training performance of the baseline model and its statically pruned version, which uses 75\% of channels in all convolution layers as used in the original proposal [42]. The model is trained for 90 epochs with a pruning interval of 10 epochs. We use a mini-batch size of 32 for ResNet50 and Inception v4 and a larger mini-batch of 128 for MobileNet v2 considering their off-chip memory capacity requirements. We use mixed-precision multiplication and accumulation [43] to execute the GEMMs of the convolution and FC layers.

In our evaluation, five different accelerator configurations are used, as summarized in Table I. The 1G1C configuration uses a single 128×128 systolic array, 1G4G splits this large core into four 64×64 cores, which share a single GBUF. The 4G4C configuration further splits the cores into 16 32×32 cores, where we divide the cores and the GBUF into four groups with cores in each group sharing a GBUF. The 1G1F configuration has a single 128×128 FlexSA with four 64×64 cores, and 4G1F has four small FlexSAs, each with a dedicated GBUF. The systolic array cores operate with 0.7 GHz clock frequency so all configurations have 23 TFLOPS. We use a GBUF of 10 MB as used in WaveCore [21] for all core configurations, and a single 270 GB/s HBM2 chip as the memory system [44]. All local input and output buffers are sized to support input and output double buffering. The local input buffers holding the horizontally shifted inputs are two times larger than the input buffers holding stationary inputs to support the larger reuse of the pre-loaded stationary inputs.

| Configuration | Description |
|---------------|-------------|
| 1G1C          | 1 group each with 1× (128×128) core |
| 1G4C          | 1 group each with 4× (64×64) cores |
| 4G4C          | 4 groups each with 4× (32×32) cores |
| 1G1F          | 1 group each with 4× (64×64) FlexSA |
| 4G1F          | 4 groups each with 1× (32×32) FlexSA |

DL models contain non-GEMM layers (e.g., feature normalization [45], [46], activation [47], and element-wise math layers), which tend to be bound by memory BW due to low arithmetic intensity. The execution time of these layers changes depending on accelerator design choices (off-chip memory BW and on-chip buffer design) and workload scheduling methods (multi-layer fusion [48], and layer fusion [21], [49]).

To decouple the impact of these memory bound operations and concentrate on what we intend to improve with FlexSA, we mainly focus on convolution and FC layers that use matrix operations and discuss the impact of other layers.

**GEMM Partitioning and Blocking.** The convolution and FC layers have three GEMM execution phases: forward propagation and data gradient and weight gradient computations in back-propagation. The GEMMs in the forward propagation and data gradient computation are skinny; they have large GEMM height (M), which is the product of the mini-batch size and the feature size, and have small GEMM width (N), which is set by the number of output channels. Thus, when multiple core groups are used, we partition a GEMM across the M dimension with one partition per core group. On the other hand, the GEMMs for weight gradient computation have small GEMM dimensions in both height and width, but they have large accumulation dimension (K). In this case, we partition the GEMM across the accumulation dimension with one partition per group. Within each GEMM partition, we use 2-level GEMM blocking that holds the inputs of a multiple of GMEM tiles in the GBUF for reuse. Within each GEMM partition, each systolic wave is allocated to cores in a group in round-robin fashion. When partitioning GEMM across the M dimension, different core groups use the same inputs from the GEMM N dimension. These shared inputs between core groups are replicated to avoid expensive inter-group data transfers. We find that this method effectively distributes GEMM workloads to multiple cores and core groups.

VIII. EVALUATION RESULTS

**PE Utilization and Performance.** Figure 3a shows the average PE utilization of ResNet50, Inception v4, and MobileNet v2 across training epochs using different core configurations. This experiment uses infinite (ideal) DRAM BW to isolate the impact on PE utilization to only the size mismatch between systolic waves and cores. The baseline 1G1C shows low average ideal PE utilization of 44\% for the three CNNs. The PE utilization of Inception v4 and MobileNet v2 are lower than that of ResNet50 because many of their convolution layers have fewer than 128 channels and are smaller than the height and width of a core. Using one FlexSA (1G1F) improves the average PE utilization to 66\% and by 49\% compared to 1G1C because it processes the GEMM using tiles with higher PE occupancy so less internal PE utilization fragmentation. Using four FlexSA units (4G1F) further improves the PE utilization to 84\% and by 89\% compared to 1G1C showing diminishing return. Compared to 1G4C and 4G4C that use 4 and 16 small independent cores, 1G1F and 4G1F show only 0.1\% less ideal PE utilization. Considering that the PE utilization of using independent small cores is the maximum that can be achieved with FlexSA. The result indicates that the FlexSA modes selected by the proposed heuristics achieve near-optimal PE utilization.

Figure 3b shows the PE utilization and speedup using a single HBM2 for the DRAM system. Unlike using ideal memory
BW, this reflects the performance impact from GEMM tiling, input blocking, and systolic wave scheduling. Therefore, for all configurations, PE utilization decreases compared to using ideal memory. Compared to using small independent cores (1G4C and 4G4C), both FlexSA configurations show smaller PE utilization drop contributing greater performance gains. This is because 1G4C and 4G4C always use small GEMM tiles and their performance suffers by increased DRAM BW peaks from executing many small independent systolic waves in parallel. FlexSA mitigates this overhead by using inter-core operating modes. Executing large waves using big cores increases arithmetic intensity per wave requiring lower peak memory BW and small systolic waves are used only when using large waves decreases PE utilization. Overall, 1G1F and 4G1F achieve average pruning-while-training speedup of 37% and 47% compared to 1G1C and by 6% and 7% even compared to 1G4C and 4G4C, respectively. This is shown by red lines in Figure 3b.

MobileNet v2 shows lower PE utilization compared to other CNNs because of its neural network architecture specifics. It uses pairs of depth-wise convolution layer and point-wise convolution layer, which have reduced input reuse. Thus, its performance becomes highly memory BW-bound with little on-chip reuse opportunity.

**On-chip Traffic and Energy Efficiency.** Other than improving PE utilization, FlexSA reduces on-chip traffic by improving in-core reuse. Figure 11 compares the on-chip traffic between the GBUF to LBUFs of convolution and FC layers of different models, which are normalized to that of 1G1C. The naive many-core configurations (1G4C and 4G4C) increase the data traffic by 1.5× and 2.7×, respectively, due to the reduced in-core reuse caused by using small independent systolic waves. On the other hand, the configurations using FlexSA show far lower data traffic compared to the naive many-core designs and similar traffic even compared to the design with larger cores. 1G1F reduces on-chip traffic by 36% compared to 1G4C, and by 2% even compared to 1G1C. This 2% traffic saving comes from reusing the stationary inputs and outputs between multiple systolic waves in processing VSW and ISW modes, which is not possible with the baseline core design. 4G1F also saves on average 43% GBUF traffic compared to 4G4C.

The reduced on-chip traffic from using FlexSA improves the energy efficiency of pruning and training. To show this, we evaluate the dynamic energy consumed per training iteration using different core configurations (Figure 12a). Each bar indicates the breakdown of energy consumed by different accelerator operations. COMP indicates the energy consumed by mixed-precision multiply and accumulation operations of the FlexSA core. LBUF, GBUF, and DRAM indicate the energy spent on data transmission associated with different resources. OverCore indicates the over-core data transmission energy, which exists only in the configurations using FlexSA. The lines represent the energy increase compared to 1G1C. Both FlexSA configurations exhibit similar or even lower energy consumption than the baseline 1G1C. This high energy efficiency of FlexSA comes from using large systolic waves in most cases. The additional energy consumed by over-core data transmission is very small for all CNNs and pruning strengths. However, 1G4C and 4G4C exhibit >20% total energy increase for ResNet50 and Inception v4 compared to both FlexSA configurations due to reduced in-core reuse and replicated input loads between cores. The reason 4G4C shows similar energy compared to 1G4C though it requires

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**Table: PE Utilization**

| Model     | Configuration | PE Utilization | PE Utilization | PE Utilization |
|-----------|---------------|----------------|----------------|----------------|
| ResNet50  | 1G1C          | 0.69           | 0.69           | 0.69           |
|           | 1G4C          | 0.69           | 0.69           | 0.69           |
|           | 4G4C          | 0.69           | 0.69           | 0.69           |
|           | 1G1F          | 0.69           | 0.69           | 0.69           |
|           | 4G1F          | 0.69           | 0.69           | 0.69           |

**Fig. 10:** PE utilization of different core configurations and the speedup normalized to 1G1C (red lines).

**Fig. 11:** On-chip traffic of different core configurations and pruning strengths.
Fig. 12: Breakdown of dynamic energy consumption per training iteration with different core configurations and pruning strength.

higher traffic is that average global buffer access energy is lower with the distributed GBUFs. However, MobileNet v2 shows smaller energy increase with 1G4C and 4G4C shows even lower energy consumption than 1G1C. This is because DRAM access accounts for the dominant energy consumption of MobileNet v2 and GBUF energy takes relatively small portion with low on-chip reuse.

**FlexSA Operating Modes Breakdown.** Figure 13 shows the breakdown of FlexSA operating modes used in pruning with 1G1F (top row) and 4G1F (bottom row) configurations. Each pie graph averages the breakdown of using high and low pruning strengths. This shows how frequently large systolic waves are used to improve in-core reuse and save energy consumption. For 1G1F, the inter-systolic array operating modes (VSW, HSW, and FW) account for 94% for both ResNet50 and Inception v4 and 66% for MobileNet v2. For 4G4F, the ratio of using inter-systolic array operating modes increase to 99% for both ResNet50 and Inception v4 and to 85% for MobileNet v2. Especially, for ResNet50 and Inception v4, the least efficient ISW accounts for only 6% and 1% for 1G1F and 4G1F. MobileNet v2 shows a bit greater ISW usage because it uses tensors with small dimensions. This result indicates that the high-reuse inter-core operations of FlexSA are used frequently and still achieve very high utilization.

**Performance and Energy Impact of Other Layers.** We evaluate the impact of other layers without layer fusion. This is a conservative assumption given many of memory-bound

**Math layers can be executed while executing GEMMs. We use SIMD array with 500 GFLOPS to execute the data-parallel operations, which is the 1/50 of the throughput of the systolic arrays. Based on our evaluation, 1G1F and 4G1F improves end-to-end training performance of all three CNNs by 24% and 29%, respectively, compared to 1G1C. This is also 3% performance improvement compared to the simple many-small-core designs. This performance gain will increase when aggressive layer fusion is considered [48]. The FlexSA configurations also save overall dynamic energy in training by 10% compared to the many-small-core designs.**

**IX. Conclusion**

In this paper, we tackle the problems in training (partially) pruned CNN models using a high-throughput accelerator with systolic arrays. The GEMMs of structurally pruned CNN models have reduced dimensions, which decreases PE utilization when processed on large systolic arrays. Although splitting a large systolic array into multiple small arrays improves PE utilization, it decreases in-core data reuse, increasing on-chip traffic and energy consumption.

To improve the PE utilization without affecting reuse, we present FlexSA, a flexible systolic array architecture that dynamically reconfigures its structure to efficiently process systolic waves with different sizes and shapes. FlexSA consists of four sub-systolic array cores and designing it adds only 1% area compared to a naive four-core design. FlexSA supports four different systolic array operating modes and each is designed to efficiently process systolic waves with different shapes, forming different inter-core systolic dataflows. Our FlexSA compiler supports optimal utilization of the underlying FlexSA resources using an efficient mode selection heuristic and custom instructions. Overall, FlexSA improves PE utilization of pruning while training CNN models by 37% compared...
to using a single large core and increase on-chip reuse by 1.7X compared to small-many-core designs, saving dynamic energy by 28%.

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