A 5-15GHz Switchless Broadband Monolithic Integrated Bidirectional Amplifier

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ABSTRACT: Based on SiGe HBT technology, two broadband monolithic integrated bidirectional amplifiers (BDA) with different operating voltages (1.8V/3.3V) are designed. By adjusting the bias voltage, the transceiver and receiver of the amplifier are switched. At the same time, a temperature compensation bias circuit is added to reduce the high and low temperature gain variation of the amplifier. It is suitable for multi-function transceiver chip or T/R module. The simulation results show that the gain of 1.8V broadband monolithic integrated bidirectional amplifier can reach 9dB in 5-15GHz operating band, the reflection coefficient of input and output ports is less than -13dB and -17dB respectively, the output power of 1dB compression point is +5.5dBm, the working current is 12.2mA, the gain of 3.3V bidirectional amplifier can reach +10.5dB, and the reflection coefficient of input and output ports is less than -12dB and -13dB. The output power of 1dB compression point is +10dBm, and the working current is 20.3mA. The core area of the chip is 0.45 x 0.45mm².

1. Introduction
With the development of T/R module, the demand for bi-directional amplifiers for gain compensation in T/R links increases. The traditional bi-directional amplifier is usually a reverse parallel low noise amplifier and power amplifier. The switch control direction. It is used in the receiving front end or the transmitting end, which not only reduces the chip area, but also improves the consistency and reliability of the whole system. In recent years, SiGe HBT process has developed rapidly. Compared with the Si bipolar process, SiGe HBT can increase the doping concentration in the base region while increasing the emission efficiency, thus reducing the resistance of the base region, increasing the maximum oscillation frequency of the device and reducing the noise figure of the device. At the same time, the heterojunction in the base region also reduces the transit time of minority carriers in the base region and improves the characteristic frequency of the device. Compared with GaAs process, SiGe HBT process has the following advantages: the thermal conductivity and mechanical strength of Si substrate are better than that of GaAs substrate; SiGe HBT process is compatible with traditional Si process and easy to integrate with CMOS process; the raw materials and production cost of SiGe HBT are lower than that of GaAs. Therefore, SiGe HBT process not only has excellent frequency, gain and noise characteristics, but also has high integration and superior cost performance, which is very suitable for the design of radio frequency integrated circuits.

This paper presents a switchless bidirectional amplifier based on SiGe HBT technology, it has completely symmetrical structure of input and output, which can receive and transmit signals in the...
frequency range of 5-15 GHz. This structure is the first attempt of SiGe technology to integrate bidirectional amplifiers in broadband monolithic circuits.

2. Circuit and Structure Design

2.1. Topological structure selection

Figure 1 is a common bi-directional amplifier structure, in which the low noise amplifier and the power amplifier are connected in reverse parallel, and the transceiver and receiver are switched by two switches.

![Figure 1. General topology of the BDA](image)

There is only one amplifier in the topology of the figure below, and the state switching is realized by multiple switches.

![Figure 2. General topology of the BDA with only one amp](image)

Figure 3 is the topology chosen in this paper. The structure removes the RF switch and controls the state switching of the transistor by switching the base voltage of the transistor, thus realizing the transceiver switching. Compared with the above structure, the circuit reduces the insertion loss caused by the switch and reduces the size and cost of the circuit.

![Figure 3. A switchless bi-directional amplifier structure](image)

2.2. Amplifier Circuit Design

In this paper, a fully symmetrical cascode (as shown in Figure 4) amplification structure is used. The common emitter has high input impedance and high transconductance, and the common base has current buffer stage characteristics and superior high frequency response. The cascode structure combines the common emitter and the common base. It has the advantages of both structure, and can also reduce Miller effect and increase bandwidth.
The graphical circuit structure is designed by Cadence software, and the gain and P1dB of the whole circuit are taken as the optimization objectives. After the simulation of schematic diagram completed, it is necessary to optimize the electrical characteristics of the whole circuit layout so as to optimize the circuit performance of the bidirectional amplifier. The simulation of schematic does not consider the coupling between devices in the layout, so in the layout design process, we should focus on the relationship between coupling and chip area. Within the permitted range of process rules, we should reduce the inter-stage spacing, minimize chip area and reduce costs.

3. Design of Temperature Compensation Bias Circuit

The traditional amplifier’s gain decreases at high temperature, which leads to the deterioration of the noise in the receiving channel, and increases at low temperature, which leads to the decrease of the dynamic range of the receiving channel. In order to improve the high and low temperature gain variation of the amplifier and improve its performance. In this design, temperature compensation circuit is used to reduce the gain change at high and low temperatures by changing the working current of the amplifier at high and low temperatures.

According to Figure 4, the gain $A_v$ of the amplifier is given by formula (1):

$$A_v \approx \frac{I_C}{\beta} \left( \frac{1}{r_{o1} r_{o2}} \parallel \frac{R_{e2} L_C}{R_C + sL_C} \parallel \frac{1}{sC_o} \right)$$

In the formula, $I_C$ is the working current of amplifier, $\beta$ is the coefficient independent of temperature, $r_{o1}$ and $r_{o2}$ are the internal resistance of amplifier Q1 and Q2 respectively, and $C_o$ is the parasitic capacitance of amplifier Q2 collector.

Formula (1) shows that the gain $A_v$ of the amplifier is proportional to the working current $I_C$. Therefore, a temperature compensation bias circuit is proposed in this paper, which biases the working current of the amplifier to a positive temperature coefficient to improve the high-temperature gain and reduce the low-temperature gain of the amplifier, thereby improving the gain fluctuation of the amplifier.

Temperature compensation bias circuit consists of reference current generation circuit and bias current mirror circuit.
3.1. Reference Current Generator Circuit

![Figure 6. Schematic of I_ref circuit](image)

The reference current circuit is shown in Figure 6. In order to achieve the temperature compensation effect of amplifier gain, the reference current $I_{ref}$ is designed to vary with temperature. For transistor devices, $I_c = I_s \exp(V_{BE}/V_T)$, it can be concluded that:

$$V_{BE1} = V_T \ln \left( \frac{I_{b1}}{I_s} \right) \quad (2)$$

$$V_{BE2} = V_T \ln \left( \frac{mI_{b2}}{I_s} \right) \quad (3)$$

In the model, $V_T = kT/q$, $I_s$ is device saturation current, $V_{BE1}$ is transistor $Q_{b1}$ base emitter voltage, $I_{b1}$ is transistor $Q_{b1}$ emitter current, $V_{BE2}$ is transistor $Q_{b2}$ base emitter voltage and $I_{b2}$ is transistor $Q_{b2}$ emitter current.

The difference between $V_{BE1}$ and $V_{BE2}$ results in positive temperature coefficient current $I_{PTAT}$. $I_{PTAT}$ works with resistors $R_1$, $R_2$ and $V_{BE1}$ to produce reference voltage $V_{ref}$. The reference voltage $V_{ref}$ generates reference current $I_{ref}$ through transistor $Q_{b3}$ and 1:1 current mirror circuit.

$$I_{PTAT} = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{V_T \ln(m)}{R_1} \quad (4)$$

$$V_{ref} = V_{BE1} + I_{PTAT}(R_1 + R_2) \quad (5)$$

$$I_{ref} \approx \frac{V_{ref} - V_{BE3}}{R_3} \approx \frac{R_1 + R_2}{R_1 R_3} V_T \ln(m) \quad (6)$$

In the above formula, $V_{BE3}$ is the base radio voltage of transistor $Q_{b3}$, $V_T = kT/q$, $m$ is the area ratio of transistor $Q_{b2}$ and $Q_{b1}$. According to equation (6), $I_{ref}$ varies with temperature and has a positive temperature coefficient current. The simulation curve of $I_{ref}$ varying with temperature is shown in Figure 7.

![Figure 7. Simulation of I_ref with temperature variety](image)
3.2. Bias current mirror circuit
As shown in Figure 8, the bias current mirror circuit consists of a current mirror and a choke circuit. The current mirror composed of PMOS transistors amplifies the reference current $I_{ref}$ by M times. The three-stage $Q_4$ and magnifier $Q_1$ are both current mirror structures. It amplifies the $Q_4$ collector current N times to provide DC bias for the amplifier. So the working current of the amplifier

$$I_C=MI_{ref}$$

From formulas (1), (6) and (7) show that when the temperature increases, the $I_{ref}$ increases and the amplifier gain $A_v$ increases; when the temperature decreases, the $I_{ref}$ decreases and the amplifier gain $A_v$ decreases. The variation of gain with temperature is contrary to that of traditional amplifier, and then the temperature compensation of low noise amplifier is completed.

![Figure 8. Temperature Compensation bias circuit](image)

**Figure 8. Temperature Compensation bias circuit**

### 4. Simulation results
Figure 11 shows the simulation gain with 1.8V and 3.3V operating voltage. Figure 12 is a simulated input-output return loss. In the 5-14 GHz band, the standing wave is less than -15 dB.
The isolation of the bi-directional amplifier is a very important index, which will affect the stability of the final bi-directional amplifier. As can be seen from the figure 13, the reverse isolation is less than -25dB.

Figure 14 shows the compression point is greater than 5.0dBm at 1.8V operating voltage and 7.5 dBm at 3.3V operating voltage.

5. Conclusion
In this paper, a fully symmetrical switchless bi-directional amplifier is designed by 0.13µm SiGe Bi-CMOS process. The core area of the chip is 0.45*0.45mm². By controlling the bias voltage of the base, the chip can switch the direction of the amplifier, reduce the differential loss and reduce the chip area. It can be used in the transceiver system to achieve bi-directional amplification.

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