Fault Detection for RC4 Algorithm and its Implementation on FPGA Platform

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Abstract

In hardware implementation of a cryptographic algorithm, one may achieve leakage of secret information by creating scopes to introduce controlled faulty bit(s) even though the algorithm is mathematically a secured one. The technique is very effective in respect of crypto processors embedded in smart cards. In this paper few fault detecting architectures for RC4 algorithm are designed and implemented on Virtex5(ML505, LX110t) FPGA board. The results indicate that the proposed architectures can handle most of the faults without loss of throughput consuming marginally additional hardware and power.

Keywords: RC4, FPGA, Fault Tolerance.

1. Endomorphism

RC4 algorithm is very simple and is widely used as a stream cipher. Today RC4 is a part of many network protocols, e.g. SSL, TLS, WEP, WPA and many others. There were many cryptanalysis to look into its key weaknesses \cite{1} followed by many new stream ciphers \cite{2}. RC4 is still the popular stream cipher since it is executed fast and provides high security. It is believed that mathematically secure crypto algorithm becomes vulnerable while implementing it in hardware \cite{3}, since it becomes possible to extract

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secret information by introducing faults in a controlled fashion due to which on fault detection techniques turn out to be a key issue related to hardware implementation. Moreover, shrinking dimension of raw devices induces Single Event Upset (soft error) which is termed as a change of logic state caused by ions or electro-magnetic radiation striking the device. The dense devices use more hardware components for faster processing and in turn cause increase of ion beam radiation as internal faults. This ion beam radiation causes state change in CLB[4]. Usually two types of faults tolerant circuits are in use, one is Hardware Based Fault Tolerant (HBFT) circuits [5][6][7] and the other is Algorithm Based Fault Tolerant (ABFT) circuits [8][9][10][11]. For HBFT, faults are detected either at the CLB level or at the LUT level.

A hamming code based fault detecting and correcting scheme is proposed for stream cipher like A5/1(GSM), E0 (Blue-tooth), RC4 (WEP), and W7 on hardware platform in article [12]. It is not necessary that faults are always sourced from the system itself. ABFT circuits at the communication level with specific reference to RC4 are proposed in [13] and [11]. A sequence number padded to each cipher character of RC4 is proposed in [13]. In [11] a method is proposed where data are stored in a matrix and 1 byte checksum is added to each of the rows and columns of the matrix. For multiple error detection they used Knight Checksum. Both the fault methods detect the fault after execution of the cipher text and thus take some additional time. There exists quite a few literatures on AES Fault tolerance Scheme [8][9]. The article [8] has tried to find out the contagious sections of the AES algorithm from which section the probability of error spreading is maximum. It has been observed how a single bit and multiple bit errors can spread over the data with algorithm iterations. Fault is located followed by its detection. They have introduced a parity checker scheme (16 bits) with input data block (16 bytes) which can detect single bit errors and as well as odd multiple bit errors. The error detecting efficiency of this scheme is not so good for efficient error detecting crypto system. For key scheduling process [8] has proposed an inverse key scheduling module which error detecting efficiency is appreciable but resource usage becomes twice of the original key scheduling model. In [9] three types of fault detection scheme based on cycle redundancy checks (CRC) are proposed.

In this paper an ABFT scheme is proposed for RC4 stream cipher in which efficient fault detecting additional hardware blocks are designed with an intention to detect maximum errors using minimum resources. The proposed scheme can detect faults at the very instant the ciphering is being executed.
Fault blocks and the algorithm block are executed in parallel due to which the throughput remains unchanged. When fault is detected, the system is reset to aware the user. Here faults are only detected, not corrected. In the absence of fault detecting blocks, occurrences of faults would cause changes in the power and timing parameters which would provide information to side channel attackers to extract information related to secret key. The paper is organized as follows: Section 2 details the overview of Fault techniques. The experimental results are summarized in Section 3. Conclusion and References are enlisted in Section 4 and 5.

2. Fault detection techniques adopted for RC4

The RC4 has two sequential algorithms, namely KSA (Key Scheduling Algorithm) and PRGA (Pseudo Random Generator Algorithm) and are shown in Figure 1. In case of RC4 a single or multiple bit errors can change the value of ‘j’ (see line 8 of KSA and line 5 of PRGA of Figure 1) randomly which can addresses a wrong S-box element for further swapping process. So there is no correlation between number of faulty bit and the number of iteration of the algorithm. As we see in Figure 1, RC4 has an identity S-Box S[N], N=0 to 255 and a secret key, key[l] where l is typically between 5 and 16, used to scramble the S-Box [N]. The purpose of the KSA-PRGA processes is to scramble the S-Box [N]. As both the processes have more or less identical operations, the design of fault tolerance modules is discussed for one process only. The detail hardware architecture of the core algorithm has been described else where in 

Figure 1: RC4 Algorithm
Arithmetic and logical operations are very much fault prone. The three common arithmetic operations of KSA and PRGA are $i'$, $j'$ computation and retrieval of $S[i]$, $S[j]$ for swapping process. Any malfunction in these operations may cause wrong encryption/decryption results which may be a clue for an attacker. It has been seen that $i'$ depends on a plane binary up counting process, where as $j'$, depends on an addition operation. Any abnormality in $i'$, $j'$ computation can address wrong $S[i] and S[j]$ resulting in wrong swapping process. Any single or multiple faults on S-Box can spread all across the algorithm quickly hampering the algorithm randomness as well as the cipher text authenticity.

To check the $i'$ functionality according to the algorithm, a new efficient counter checker module is proposed. For $j'$ computation an efficient addition checker is proposed. The correct computation of $S[i] and S[j]$ is ensured by using a CRC checker on S-box [N]. The three checkers are executed parallel with the main algorithm without hampering the algorithm throughput. The proposed three fault blocks are shown in Figure 2 and the structure of the CRC code is shown in Figure 3. Before the execution of each round, the core algorithm checks the "no fault" signal contributed by the three proposed fault checkers. Each of the three fault checkers feed no_fault to the algorithm block through AND gate. Any fault detected by a particular fault module can stop the execution of the algorithm at that instant of clock edge.

2.1. Error detection on S-Box: CRC Checker

To detect fault on S-Box Array standard CRC technique of 4-degree polynomial is used. Lower degree of polynomial is used to reduce length of redundant CRC bits. It has been seen that CRC has good efficiency to detect single bit errors, double bit errors and odd number of errors. A dedicated hardware block to execute CRC algorithm has not been designed since that would require a huge hardware resource, large computation power and might cause some synchronization problem with the main algorithm. This synchronization problem is a sensitive issue as the main crypto core has a very high throughput based on dual edge sensitivity. To by-pass, a standard 4-degree divisor, $X^4 + X^3 + 1$ is chosen and four bit residue is computed as CRC code which has been padded to each S-Box element, each element thus becomes a 12-bit data instead of 8-bit, as shown in Figure 3. This new S-box is stored as two S-Boxes in the CRC hardware block (vide Figure 4) as well as in main algorithm S-Box. CRC block has two input $S[i]$ and $S[j]$. In each
clock $S[i]$ and $S[j]$ is computed by the main algorithm block and then it has been checked by CRC module whether S-Box element is correct or not. If there is no error in the CRC block it will proceed for the next clock cycle. According to [15] CRC checker can detect all odd number of errors since the divisor polynomial can be divided by $X+1$. It can detect all isolated double bit errors, since the polynomial cannot be divided by $X^t+1$ (where $t=2$ to 8).

Table 1 shows the number of detected faulty bit, maximum number of faulty bit combination and the number of detected and undetected fault using the CRC based method. As shown in table 1 the efficiency evaluates 86%.

### 2.1.1. Hardware design of CRC checker

The input of CRC block is $S[i]$ and $S[j]$ which are of 12 bit, 8 bit is for data and 4 bit for CRC code. The CRC encoded data format is shown in [3]. A look up table of 4 bit width is already stored in 'buffer' called CRC array with appropriate CRC code. The $S[i]$ and $S[j]$ port of algorithm block is
connected with $S[i]$ and $S[j]$ of CRC block. In every rising edge of clock the CRC encoded $S[i]$ and $S[j]$ data from the algorithm block has been checked with CRC array by the CRC block. The CRC hardware architecture is shown in 4.

![CRC encoded data diagram](image)

**Figure 3: CRC encoded data**

![CRC hardware block](image)

**Figure 4: CRC hardware block**

### 2.2. Error Detection on Addition Checker

There are few standard types of error detecting techniques on arithmetic operations [15] such as parity and residue techniques which are most popular due to its low cost and high error detecting efficiency. Residue technique is motivated on modulus operation which costs huge hardware footprint [16] in FPGA based platform. This is the reason that the parity scheme is adopted in this paper for addition checker. The 8-bit data is split into two 4-bit nibble to increase the error detecting efficiency as is seen in table 2. Now it is necessary to describe how the parity prediction scheme is initiated for addition operation. Of the two 8-bit numbers, such as If there are two
numbers of 8 bit width, such as add and aug. 4 parity bit such as then \( p(\text{add lower}), p(\text{add higher}), p(\text{aug lower}) \) and \( p(\text{aug higher}) \) following manner.

\[
\begin{align*}
p(\text{add lower}) &= p(\text{add}(0) \oplus \text{add}(1) \oplus \text{add}(2) \oplus \text{add}(3)), \\
p(\text{add higher}) &= p(\text{add}(4) \oplus \text{add}(5) \oplus \text{add}(6) \oplus \text{add}(7)), \\
p(\text{aug lower}) &= p(\text{aug}(0) \oplus \text{aug}(1) \oplus \text{aug}(2) \oplus \text{aug}(3)), \\
p(\text{aug higher}) &= p(\text{aug}(4) \oplus \text{aug}(5) \oplus \text{aug}(6) \oplus \text{aug}(7)).
\end{align*}
\]

### 2.2.1. Prediction for arithmetic addition

It is well known that the parity of the sum of two natural number can be obtained by XORing the parities of both summands and of all carries propagated between any two adjacent bits, plus the possible carry-in into the least significant position. Hence

\[
\begin{align*}
p(\text{addlower} + \text{auglower}) &= p(\text{addlower}) \oplus p(\text{auglower}) \oplus C_{in} \oplus \bigoplus_{i=0}^{3} C^{(i)}_{out} \\
p(\text{addhigher} + \text{aughigher}) &= p(\text{addhigher}) \oplus p(\text{aughigher}) \oplus C_{in} \oplus \bigoplus_{i=4}^{7} C^{(i)}_{out}
\end{align*}
\]

### 2.2.2. Hardware strategy of addition checker

In KSA process the inputs of addition checker such as, \('j', S[i], \) and \( K[i] \) and its summation result has been passed to the addition checker block. By parity prediction technique the addition checker fault block can check the whether the summation is right or wrong. The efficiency is about 75% which is portrayed in table 3. The same addition checker module has been used for \( Z \) computation in line no. 5 and 7 of PRGA process.

### 2.3. Error Detection on \( i \) counter

Several techniques\[17\] have already been developed in order to improve the reliability of binary counter. A completely new technique is proposed consuming very low resource usage and exhibit very high error detecting efficiency. An interesting pattern has been observed in binary counting. If the parity of even bit position data is computed, the parity of first 4 set of data will be the complement of next 4 set of data. Similarly if the parity of odd bit position data is computed, the parity of first 4 set of data will also be
Table 3: Addition Checker

| # faulty bit(bit) | Possible combination of faulty bit | Counter Checker | Detected Fault | Undetected Fault |
|------------------|-----------------------------------|----------------|----------------|-----------------|
| 1 8C1=8          | 8                                 | 8              | 0              |
| 2 8C2=28         | 16                                | 12             |
| 3 8C3=56         | 56                                | 0              |
| 4 8C4=70         | 32                                | 38             |
| 5 8C5=56         | 56                                | 0              |
| 6 8C6=28         | 16                                | 12             |
| 7 8C7=8          | 8                                 | 0              |
| 8 8C8=1          | 0                                 | 1              |

Total fault 255, 192, 63
Error Detecting Efficiency (%) 75

Table 4: Binary counting pattern

| counting number | parity | MSB of two nibble | Even | Odd |
|-----------------|--------|-------------------|------|-----|
| 00000000        | 0      | 0                 | 0    | 0   |
| 00000001        | 0      | 1                 | 0    | 0   |
| 00000010        | 0      | 0                 | 1    | 0   |
| 00000011        | 0      | 1                 | 1    | 1   |
| 00000100        | 1      | 0                 | 1    | 0   |
| 00001001        | 1      | 1                 | 1    | 1   |
| 11111110        | 1      | 1                 | 0    | 0   |
| 11111111        | 0      | 0                 | 0    | 0   |

The complement to next 4set of data. There exist another pattern in parity bit of msb of upper nibble and msb of lower nibble. The parity pattern is shown in table 4. Following this pattern we have designed a fault checker on the 'i' counter which store the 8 consecutive counting of 'i' and feed a decision whether the counting is right or wrong based on the pattern prediction that we describe in table 4.

2.3.1. Hardware overview of counter checker

The main RC4 algorithm core increasing 'i' in every clock cycle. Every 8 set of data has been buffered into an array in counter checker fault block. The fault block separate 8 set of data into two 4 set of part. The fault checking algorithm checks the proposed pattern mentioned in table 4 after every 8 clock cycle and make decision that whether fault has been occurred or not which has been fed to the main algorithm block. The error detecting
Table 5: Counter Checker

| # | Faulty bit(bit) | Possible combination of faulty bit | Counter Checker |
|---|-----------------|-----------------------------------|----------------|
| 1 | 8C1=8           | 8                                 | Detected Fault |
| 2 | 8C2=28          | 20                                | Undetected Fault |
| 3 | 8C3=56          | 56                                |                |
| 4 | 8C4=70          | 55                                |                |
| 5 | 8C5=56          | 56                                |                |
| 6 | 8C6=28          | 20                                |                |
| 7 | 8C7=8           | 8                                 |                |
| 8 | 8C8=1           | 1                                 |                |

Total fault 255
Error Detecting Efficiency (%) 88

CLK
Initialize

\[ i=0, j=0 \]
Start Counter
\[ i=1 \]
\[ j=(j+S[i]) \mod 256 \]
\[ i=2 \]
Swap \( S[i] \) & \( S[j] \)
\[ j=(j+S[i]) \mod 256 \]
\[ i=3 \]
Swap \( S[i] \) & \( S[j] \)
\[ j=(j+S[i]) \mod 256 \]
\[ i=9 \]
Swap \( S[i] \) & \( S[j] \)
\[ j=(j+S[i]) \mod 256 \]
\[ i=8 \]
Swap \( S[i] \) & \( S[j] \)
\[ j=(j+S[i]) \mod 256 \]
\[ i1 \] is latched
\[ i2 \] is latched
\[ i3 \] is latched
\[ i8 \] is latched & make decision whether fault is occurred or not

Counter Checker
Addition Checking on \( j \)

Addition Checker
Addition Checking on \( j \)
Addition Checking on \( j \)
Addition Checking on \( j \)

CRC Checker
CRC checking on \( S[i] \) & \( S[j] \)
CRC checking on \( S[i] \) & \( S[j] \)
CRC checking on \( S[i] \) & \( S[j] \)
CRC checking on \( S[i] \) & \( S[j] \)

Figure 5: Timing diagram of proposed fault modules with respect to main algorithm

efficiency of proposed counter checker has been shown in table 5

3. Results and discussion

The individual fault blocks have been implemented on Xilinx Virtex5 FPGA board. The resource consumption of 3 fault blocks is very less compared to the main architecture. Of the proposed fault blocks, the counter checker block and add checker sub-blocks takes very less resource compared to main architecture (0.09% & 0.31%) while the main CRC checker sub-block (50%) is resource hungry and takes considerably high resource compared to main architecture. Not only this, the 3 blocks have 45% 0.2% & 0.26% LUTs usage compare to the main architecture. The detail estimation of resource usage is given in table 7

The xilinx xpower tool to measure system power consumption [18]. Three fault blocks, CRC Counter Checker & Addition Checker consume 7% 1.2% & 4.3% power compared to main architecture power. Resource utilization table
Table 6: power consumption

| Power (milli watt) | Main Core | CRC | Counter | Addition Checker |
|-------------------|-----------|-----|---------|------------------|
| Total Power       | 994.72    | 70.58 | 12.81   | 43.25            |
| Quiescent Power   | 914.87    | 30.71 | 0.67    | 2.29             |
| Dynamic Power     | 52.86     | 67.1 | 11.9    | 40.96            |
| Clock r Power     | 47.33     | 19.03 | 7.11    | 0.19             |
| Logic Power       | 0.60      | 4.47 | 0.06    | 0.13             |
| IOs Power         | 0.60      | 4.47 | 0.06    | 0.13             |
| Signal Power      | 4.74      | 43.39 | 4.94    | 41.66            |

Table 7: Resource utilization

| Logic Usage #      | Main Core | CRC | Counter Checker | Addition Checker |
|--------------------|-----------|-----|-----------------|------------------|
| Slice Register     | 4139      | 2042| 4               | 13               |
| slice LUT          | 12560     | 5653| 26              | 33               |
| fully used LUT -FF pairs | 4132 | 2034 | 52 | 78 |

using Vertex 5 FPGA in which 1-byte in 1-clock was the approximate execution speed which has been achieved by carrying the addition process (line 5 of PRGA process) during the rising edge of a clock pulse and the swapping and key streams generation (lines 6 and 7 of PRGA process) during falling edge of the same clock pulse with a loss of one initial clock pulse. The timing diagrams of the proposed three fault modules with respect to main algorithm clock are also shown in Figure 5. At falling edge of every 8th consecutive clocks,’i’is checked and at every rising edge, the addition checker and at every falling edge, the CRC checker is executing their respective tasks. It becomes evident that the fault modules are so designed in hardware here that the throughput of the main RC4 algorithm remains unchanged.

4. Conclusion

In this paper three low cost fault block are designed for RC4 and implemented in FPGA operating concurrently with the progress of the main algorithm consuming low power and resources, providing run time fault detection efficiency without affecting its throughput. On detection of even one fault the algorithm ceases execution. Had the main algorithm and fault
blocks are executed sequentially, the throughput would have been reduced and the attacker would have been able to get the secrets of the algorithm observing power and timing parameters.

5. References

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