MIMO Systems with One-bit ADCs: Capacity Gains using Nonlinear Analog Operations

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Abstract

Analog to Digital Converters (ADCs) are a major contributor to the energy consumption on the receiver side of millimeter-wave multiple-input multiple-output (MIMO) systems with large antenna arrays. Consequently, there has been significant interest in using low-resolution ADCs along with hybrid beam-forming at MIMO receivers for energy efficiency. However, decreasing the ADC resolution results in performance loss — in terms of achievable rates — due to increased quantization error. In this work, we study the application of practically implementable nonlinear analog operations, prior to sampling and quantization at the ADCs, as a way to mitigate the aforementioned rate-loss. A receiver architecture consisting of linear analog combiners, implementable nonlinear analog operators, and one-bit threshold ADCs is designed. The fundamental information theoretic performance limits of the resulting communication system, in terms of achievable rates, are investigated under various assumptions on the set of implementable nonlinear analog functions. In order to justify the feasibility of the nonlinear operations in the proposed receiver architecture, an analog circuit is introduced, and circuit simulations exhibiting the generation of the desired nonlinear analog operations are provided.
I. INTRODUCTION

In order to satisfy the ever-growing demand for higher data-rates and bandwidth, the emerging wireless networks operate in frequencies above 6 GHz especially the millimeter wave (mm-wave) bands. The high carrier frequencies used in mm-wave systems allow for larger channel bandwidths compared to lower-frequency systems. For instance, in conventional protocols such as LTE, the bandwidth is between 1.4 MHz and 20 MHz \[1\], whereas in microwave WiFi standards such as IEEE 802.11ad the bandwidth is 2.16 GHz \[2\], and in mm-wave cellular applications, bandwidth of 500 MHz or more has been considered \[3\]. The inherent high isotropic path loss and sensitivity to blockages at high frequencies pose challenges in supporting high capacity and mobility \[4\]. As an example, Friis’ Law states that the isotropic path loss in free-space propagation is inversely proportional to the wavelength squared \[5\]. In order to mitigate the path loss, mm-wave systems leverage narrow-beams, by using large antenna arrays at both base stations (BS) and user-ends (UE). For instance, fifth-generation (5G) wireless networks envision hundreds of antennas at the BS and in excess of ten antennas at the UE \[6\]. In conventional multiple-input multiple-output (MIMO) systems with digital beamforming, each antenna input/output is digitized separately \[7\]. This requires each receiver antenna to be connected to a dedicated analog to digital converter (ADC). Since mm-wave systems use large arrays of antennas — to mitigate the propagation losses due to small carrier wavelength — digital beamforming in mm-wave systems requires a large number of ADCs which are a significant source of power consumption in MIMO receivers \[5\], \[8\]. Another contributing factor to the high energy demands in mm-wave ADC modules is the large channel bandwidth used in these applications. In theory, the power consumption of an ADC grows linearly in bandwidth, and the rate of increase is even more significant in practical implementations due to the excessive loss associated with the passive components at higher frequencies \[9\]–\[11\]. Consequently, the massive number of receiver antennas and large channel bandwidth result in a substantial increase in ADC power consumption in mm-wave MIMO systems. Furthermore, in standard ADC design, power consumption is proportional to the number of quantization bins and hence grows exponentially
in the number of output bits [12]. This limits the resolution of the ADCs due to power budget restrictions.

Hybrid beam-forming with low-resolution ADCs has been proposed as a way to mitigate the high energy cost of ADCs by reducing the number of converters and their resolutions. To elaborate, under hybrid beam-forming, the receiver terminals in MIMO systems use analog beam-formers to linearly combine the large number of signals at the receiver antennas and feed them to a small set of low-resolution ADCs. There has been a large body of work on the design of energy-efficient transceiver architectures and coding strategies using hybrid beam-forming with a small number of ADCs for communication in mm-wave MIMO systems [5], [13]–[20]. The communication setup considered in these works is discussed briefly in Section II.

In this work, we consider the use of nonlinear analog operations as a way to mitigate the rate-loss due to the use of low-resolution ADCs. To explain the aforementioned rate gains, let us consider a simple single-input single-output (SISO) scenario operating in the high signal-to-noise ratio (SNR) regime, i.e. $Y \approx X$. Assume that the receiver is equipped with two one-bit threshold ADCs. Then, as shown in Figure 1(a), it can receive at most three different messages per channel-use by performing two threshold comparisons, e.g. comparisons with threshold zero $Y \leq 0$ and threshold one $Y \leq 1$, hence achieving a rate of $R = \log 3$ bits/channel-use. Alternatively, if the receiver has access to the second power, $Y^2$, of the channel output, then it can use the two comparators $Y \leq 0$ and $Y^2 \leq 1$ as shown in Figure 1(b) to achieve $R = 2$ bits/channel-use, hence improving performance. We investigate the set of achievable regions under general assumptions on the number of transmit antennas, receive antennas, one-bit ADCs, channel SNR, and the values of $k$ in $Y^k$ which can be produced using analog circuits. We provide several communication strategies and derive the resulting achievable regions in various scenarios described in Section II. To justify the feasibility of the nonlinear analog operations studied in this work, we show through simulation of a circuit whose design is explained in Section IV that one can implement ADCs which operate by comparing the $k$th power $Y^k$ of the input to a set of thresholds, where $k > 1$, without significant increase in power consumption. At a high level, the proposed circuit...
Fig. 1. (a) the transmitter sends $X$ with amplitudes $-0.5, 0.5, 1.5$ to send messages 1, 2, and 3, respectively, and receiver uses two one-bit threshold ADCs $Y \leq 0$ and $Y \leq 1$, and (b) the transmitter sends $X$ with amplitudes $-1.5, -0.5, 0.5, 1.5$ to send messages 1, 2, 3, and 4, respectively, and receiver uses two one-bit threshold ADCs $Y \leq 0$ and $Y \geq 1$.

operates on the higher harmonics of its input signal to extract the $k$th power of the amplitude, and the value of $k$ is bounded from above due to practical restrictions in circuit design. Circuit simulations exhibiting the generation of nonlinear analog operations are provided.

**Notation:** The set $\{1, 2, \cdots, n\}, n \in \mathbb{N}$ is represented by $[n]$. The $n$-length vector $(x_1, x_2, \ldots, x_n)$ is written as $x(1:n)$ and $x^n$, interchangeably, and $(x_k, x_{k+1}, \ldots, x_n)$ is denoted by $x(k:n)$. The $i$th element is written as $x(i)$ and $x_i$, interchangeably. We write $\| \cdot \|_2$ to denote the $L_2$-norm. An $n \times m$ matrix is written as $h(1:n, 1:m) = [h_{i,j}]_{i\in[n]\times[j\in[m]]}$, its $i$th column is $h(:,i), i \in [m]$, and its $j$th row is $h(j,:), j \in [m]$. We write $x$ and $h$ instead of $x(1:n)$ and $h(1:n, 1:m)$, respectively, when the dimension is clear from context. Sets are denoted by calligraphic letters such as $X$, families of sets by sans-serif letters such as $\mathcal{X}$, and collections of families of sets by $\mathcal{X}^\mathcal{X}$. For the region $\mathcal{A} \in \mathbb{R}^n$, the set $\partial \mathcal{A}_k$ denotes its boundary. $\mathcal{B}$ denotes the Borel $\sigma$-field.

### II. System Model

We consider a MIMO communication channel characterized by the triple $(n_t, n_r, \mathbf{h})$, where $n_t$ is the number of transmitter antennas, $n_r$ is the number of receiver antennas, and $\mathbf{h} \in \mathbb{R}^{n_r \times n_t}$ is the (fixed) channel gain matrix. It is assumed that the transmitter and receiver have prefect
knowledge of $h$. The channel input and output $(X, Y) \in \mathbb{R}^{n_t} \times \mathbb{R}^{n_r}$ are related through $Y = hX + N$, where $N \in \mathbb{R}^{n_r}$ is a vector of independent and identically distributed Gaussian variables with unit variance and zero mean, and the channel input has average power constraint $P$, i.e. $\frac{1}{n_t} \sum_{i=1}^{n_t} \mathbb{E}(X_i^2) \leq P$.

Let the message $M$ be chosen randomly and uniformly from $[\Theta]$, where $\Theta \in \mathbb{N}$. The communication blocklength is $n \in \mathbb{N}$ and the communication rate is $\frac{1}{n} \log \Theta$. The transmitter produces $X(1:n,1:n_t) = e(M)$, where $e : [\Theta] \rightarrow \mathbb{R}^{n \times n_t}$ is the encoding function. At the $i$th channel-use, the vector $X(i,1:n_t), i \in [n]$ is transmitted and the receiver receives $Y(i,1:n_i) = hX(i,1:n_t) + N(i,1:n_t)$. The receiver produces the message reconstruction $\hat{M} = d(Y(1:n,1:n_t))$, where $d : \mathbb{R}^{n \times n_t} \rightarrow [\Theta]$ is the decoding function. In this work, we restrict the choice of decoding functions by considering the limitations on number of available one-bit threshold ADCs, $n_q \in \mathbb{N}$, and the set of implementable analog functions $F_a$ at the receiver. This is described in more detail in the following.

In its most general form, the receiver (Figure 2) consists of three components: i) an analog processing module captured by $f_a : \mathbb{R}^{n_r} \rightarrow \mathbb{R}^{n_q}$ operating on each channel output $Y(i,1:n_i), i \in [n]$, ii) a set of $n_q$ one-bit threshold ADCs with threshold vector $t(1:n_q) \in \mathbb{R}^{n_q}$ captured by $Q_{n_q} : \mathbb{R}^{n_r} \rightarrow \{0,1\}^{n_q}$ operating on each output of the analog processing module $W(i,1:n_q)$,
and iii) a digital processing module captured by \( f_d : [0,1]^{n_q} \rightarrow [\Theta] \), operating on the block of ADC outputs \( \hat{W}(1:n,1:n_q) \).

After the \( i \)th channel-use, the analog processing module processes the received signal \( Y(i,1:n_r) \) in the analog domain and produces \( W(i,1:n_q) = f_a(Y(i,1:n_r)), i \in [n] \). The choice of \( f_a(\cdot) \) is restricted to the set of implementable analog functions \( \mathcal{F}_a \) and is discussed further in the sequel. The output \( W(i,1:n_q), i \in [n] \) is fed to the one-bit threshold ADCs which produce the discretized vector

\[
\hat{W}(i,1:n_q) = \mathcal{Q}_{n_q}^n(W(i,1:n_q)) = (W(i,j) \leq t(j), j \in [n_q])
\]

where \( W(i,j) \leq t(j) \) denotes the indicator function \( \mathbb{1}\{ W(i,j) > t(j) \} \). After the \( n \)th channel-use, the digital processing module produces the message reconstruction \( \hat{M} = f_d(\hat{W}(1:n,1:n_q)) \). The communication system is characterized by \( (n_t,n_r,h,n_q,F_a) \), and the transmission system by \( (n,\Theta,e,f_a,f_d) \), where \( f_a \in \mathcal{F}_a \). Achievability and probability of error are defined in the standard information-theoretic sense. The capacity maximized over all implementable analog functions is denoted by \( C_Q(n_t,n_r,h,P,n_q,F_a) \).

**Remark 1.** We have considered channels with real-valued inputs with one-bit ADCs used at the receiver. The analysis may be extended to complex-valued inputs and low-resolution ADCs with more than one-bit output length in a straightforward manner.

**Remark 2.** We have considered MIMO systems with low-resolution ADCs under average input power constraints. Peak power constraints have also been considered \( [21],[22] \) under specific restrictions on \( \mathcal{F}_a \) such as linearity of the analog processing function.

The following sets of implementable analog functions \( \mathcal{F}_a \) have been considered in prior works:

- **Scenario I: No Analog Processing \( [23] \):** \( \mathcal{F}_a^I \) consists of the single (trivial) function \( f_a(Y) = Y \), and we must have \( n_r = n_q \), i.e. digital beamforming. It was shown that when the signal is not processed in the analog domain, binary antipodal signaling is optimum in all SNRs.
• **Scenario II: Linear Analog Processing** [14], [24], [25]: $\mathcal{F}_a^{II}$ consists of linear functions $f_a(Y) = YV, V \in \mathbb{R}^{n_q \times n_r}$. It was shown that linear analog processing prior to the ADC module increases the high SNR capacity, and the gains are further augmented with the use of analog delay elements.

We generalize Scenario II, where $f_a: \mathbb{R}^{n_q} \rightarrow \mathbb{R}^{n_q}$ consists of $n_q$ real-valued linear functions of $Y$, and consider scenarios where $f_a(\cdot)$ consists of $n_q$ real-valued polynomial functions of $Y$. In particular, we consider the following scenarios:

• **Scenario III: Polynomial Functions with Arbitrary Degree:** $\mathcal{F}_a^{III}$ consists of vectors of functions $f_a(Y) = (f_{a,1}(Y), f_{a,2}(Y), \cdots, f_{a,n_q}(Y))$, where $f_{a,i}(Y) \in \mathcal{P}(\mathbb{R}^{n_r}), i \in [n_q]$, and $\mathcal{P}(\mathbb{R}^{n_r})$ is the space of all finite-degree polynomials from $\mathbb{R}^{n_r}$ to $\mathbb{R}$. That is:

$$f_{a,i}(Y) = \sum_{k_1, k_2, \cdots, k_{n_r}} b_{k_1, k_2, \cdots, k_{n_r}} \prod_{j=1}^{n_r} Y_j^{k_j}(f),$$

where $b_{k_1, k_2, \cdots, k_{n_r}} \in \mathbb{R}, (k_1, k_2, \cdots, k_{n_r}) \in \mathbb{R}^{n_r}, i \in [n_q], t \in \mathbb{N}.$

• **Scenario IV: Polynomial Functions with Bounded Degree:** $\mathcal{F}_a^{IV}$ consists of vectors of functions $f_a(Y) = (f_{a,1}(Y), f_{a,2}(Y), \cdots, f_{a,n_q}(Y))$, where $f_{a,i}(Y) \in \mathcal{P}_d(\mathbb{R}^{n_r}), i \in [n_q]$, and $\mathcal{P}_d(\mathbb{R}^{n_r})$ is the space of all polynomials with degree at most $d \in \mathbb{N}$.

• **Scenario V: Implementable Quadratic Functions:** $\mathcal{F}_a^{V}$ consists of vectors of functions $f_a(Y) = (f_{a,1}(Y), f_{a,2}(Y), \cdots, f_{a,n_q}(Y))$, where $f_{a,i}(Y)$ is generated by the functions $(Y_1, Y_2, \cdots, Y_{n_r}, Y_1^2 + Y_2^2 + \cdots + Y_{n_r}^2)$. That is,

$$f_{a,i}(Y) = \sum_{k=1}^{n_r} a_{k,i} Y(k) + a_{n_r+1,i} \sum_{k=1}^{n_r} Y^2(k),$$

where $a_{k,i} \in \mathbb{R}, k \in [n_q], i \in [n_r + 1]$.

Scenario III is an ideal scenario, where analog circuits can be used to generate any arbitrary polynomial function. This scenario is investigated in Section III-A, where the achievable rate region is characterized, and a computable inner bound is provided. However, we argue that this ideal scenario cannot be implemented in practice due to the limitations of analog circuitry which prohibits implementation of high degree polynomial functions. Scenario IV limits the degree of
the polynomial function by an integer $d \in \mathbb{N}$. This scenario is investigated in Section [III-B] where the high SNR achievable region is derived, and it is shown that under specific conditions on the number of available one-bit ADCs, the achievable region approaches that of scenario III, i.e. optimal achievable rate. Scenario V is a special case of Scenario IV, where the function is restricted to specific quadratic polynomials. The achievable rate region for this scenario is characterized for all SNRs in Section [III-C]. It can be noted that $F_{III}^a \subset F_{IV}^a \subset F_{V}^a \subset F_{III}^a$.

III. Communication Strategies and Achievable Rates

In this section, we consider Scenarios III, IV, and V described in Section [II] and derive the achievable rate region in each case under specific assumptions on the number of available one-bit ADCs $n_q$, and the channel SNR.

A. Scenario III: Polynomials with Arbitrary Degree

Using the Stone-Weierstrass Theorem on uniform approximation of continuous functions over compact sets (e.g. [26]), we show that the decoding operation in this scenario is equivalent to a two-step decoding process, where i) the channel output $Y(i, 1:n_r), i \in [n]$ is discretized with arbitrary discretization bins, so that $\hat{W}(i, 1:n_q) = Q'(Y(i, 1:n_r))$, where $Q' : \mathbb{R}^{n_r} \rightarrow \{0, 1\}^{n_q}$ is an arbitrary function, and ii) the discretization indices $\hat{W}(1:n, 1:n_q)$ are processed jointly to reconstruct the message $\hat{M} = f_d(\hat{W}(1:n, 1:n_q))$. This is formalized as follows.

**Theorem 1.** Let $P > 0$, $n_t, n_r, n_q \in \mathbb{N}$, $h \in \mathbb{R}^{n_t \times n_r}$, and $X^{n_t}$ be defined on the probability space $(\mathbb{R}^{n_t}, \mathcal{B}^{n_t}, P_{X^{n_t}})$ satisfying the average power constraint $\frac{1}{n_t} \sum_{i=1}^{n_t} \mathbb{E}(X(i)) \leq P$. Then:

$$C_Q(n_t, n_r, h, P, n_q, F_{III}^a) \geq \sup_{A \in \mathcal{A}_{\text{Rank}(h), n_q}} I_A(X^{n_t}; V),$$

where $\text{Rank}(h)$ is the rank of matrix $h$, $\mathcal{A}_{\text{Rank}(h), n_q}$ is the set of all possible partitions of $\mathbb{R}^{\text{Rank}(h)}$ into $2^{n_q}$ connected regions, $V$ is defined on $[2^{n_q}]$, and the mutual information $I_A(X^{n_t}; V)$ is evaluated with respect to $P_A(X^{n_t}, V)$ such that:

$$P_{X^{n_t}, Y}(C, k) = P(X^{n_t} \in C, Y \in A_k), C \in \mathcal{B}^{n_t}, k \in [2^{n_q}]$$
where \( A_k \) is the \( k \)th partition element in \( A \).

**Proof.** Please refer to Appendix A. \( \square \)

**Remark 3.** Using lower semi-continuity of mutual information, and data processing inequality \[27\], it follows that as \( n_q \to \infty \), the capacity approaches that of continuous-output Gaussian channels. That is, \( \lim_{n_q \to \infty} C(n_t, n_r, h, P, n_q, F^{III}_d) \) is equal to the capacity of the continuous-output Gaussian channel \( Y = hX + N \).

Theorem 1 provides a lower-bound on the capacity, however, this bound is not necessarily computable since it requires optimization over all partitions in \( A_{\text{Rank}(h), n_q} \). The following theorem provides a computable inner-bound to the one given in Theorem 1. The theorem uses the singular value decomposition (SVD) in the analog domain to transform the communication system into \( s = \text{Rank}(h) \) parallel, non-interfering channels. The \( i \)th parallel channel is allocated a number of \( n_{q,i} \) one-bit ADCs, where \( \sum_{i \in [s]} n_{q,i} = n_q \), and is allocated \( \frac{P_i}{P} \) fraction of the power budget, where \( \sum_{i \in [s]} P_i = P \).

**Theorem 2.** Let \( P > 0, n_t, n_r, n_q \in \mathbb{N}, h \in \mathbb{R}^{n_t \times n_r} \). Then:

\[
C_Q(n_t, n_r, h, P, n_q, F^{III}_d) \geq \max_{(n_{q,i}, i \in [s]) \in N} \left( \max_{(P_i, i \in [s]) \in \mathcal{P}} \sup_{A \in A_{n_q,i}} \frac{1}{P} \sum_{k=1}^{s} I_{A}(\tilde{X}_k; V_k), \right)
\]

where \( N \triangleq \{(n_{q,i}, i \in [s]) : \sum_{i \in [s]} n_{q,i} = n_q\}, \mathcal{P} \triangleq \{(P_i, i \in [s]) : \sum_{i \in [s]} P_i = P\}, \tilde{Y}_k = \sigma_k \tilde{X}_k + N_k \), \( N_s \) is a vector of i.i.d. zero-mean Gaussian variables with unit variance, \( \sigma_k \) is the \( k \)th eigenvalue of \( h \), and the mutual information is evaluated with respect to \( P_{X^n, V_k}^{A_i} \) such that:

\[
P_{A_i}^{X^n, V_k}(C, \ell) = P(X^n \in C, Y^n \in A_\ell), C \in \mathbb{R}^n, k \in [2^n], \ell \in [2^n].
\]

The proof follows by similar arguments as Theorem 3 of \[24\] along with proof of Theorem 1 and is omitted for brevity.
Remark 4. The first two maximizations in Equation (1) are over finite sets, and the two supremums are taken over all one dimensional partitions along with the distribution of \( X \). The latter optimization has been studied extensively in the literature, and it was shown that the maximum rate is achieved by putting the mass of \( P_X \) on a finite number of at most \( 2^{n_q} \) points \([21], [23]\).

B. Scenario IV: Polynomials with Bounded Degree

In this scenario, we consider a special case of Scenario IV, where the analog functions are restricted to specific quadratic polynomials. In particular, the function is generated by \( \{x_1, x_2, \cdots, x^{\text{Rank}(h)}\}, \sum_{i=1}^{\text{Rank}(h)} x_i^2 \}. \) We have the following theorem for the high SNR capacity.

\textbf{Theorem 3.} Let \( n_t, n_r, n_q \in \mathbb{N}, h \in \mathbb{R}^{n_t \times n_r} \) and let the maximum polynomial degree in \( \mathcal{F}^{IV} \) be \( d \in \mathbb{N} \). Then,

\[ \lim_{P \to \infty} C_Q(n_t, n_r, h, P, n_q, \mathcal{F}^{IV}) \geq \max \left( n_q, \log \left( \frac{\text{Rank}(h) + d}{d} \right) \right), \]

\textbf{Proof Outline.} Following the arguments in Theorem 1 in [24], the maximum number of messages which can be transmitted reliably at high SNR is equal to the maximum number of distinct quantization regions which can be produced in \( \mathbb{R}^{\text{Rank}(h)} \) using the analog processing and ADC operation (as long as it is not greater than \( 2^{n_q} \)). We argue that this number is greater than or equal to the Vapnik-Chervonenkis Dimension (\( VCdim \)) of \( \mathcal{F}^{IV} \). The proof is completed by noting that \( VCdim(\mathcal{F}^{IV}) = \left( \frac{\text{Rank}(h) + d}{d} \right) \) as shown in [28]. To see the former statement, let \( \mathbf{x}_1, \mathbf{x}_2, \cdots, \mathbf{x}_\ell \in \mathbb{R}^{\text{Rank}(h)} \) be a set of points which are shattered by \( \mathcal{F}^{IV} \), where \( \ell = VCdim(\mathcal{F}^{IV}) \). Then, by definition of \( VCdim \), there exist polynomial discriminants \( f_{a,j}() \), \( j \in [2^\ell] \) in \( \mathcal{F}^{IV} \) such that \( (Q_0(f_{a,j}(\mathbf{x}_1)), Q_0(f_{a,j}(\mathbf{x}_2)), \cdots, Q_0(f_{a,j}(\mathbf{x}_\ell))) \) is the binary representation of \( j \). Let \( f_{a,j_1}, f_{a,j_2}, \cdots, f_{a,j_{n_q}} \) be such that \( \text{sign}(f_{a,j_k}(\mathbf{x}_t)) = (-1)^{k \text{mod} d(t)}, k \in [n_q], t \in [\ell] \). Then, \( (Q_0(f_{a,j_1}(\mathbf{x}_1)), Q_0(f_{a,j_2}(\mathbf{x}_2)), \cdots, Q_0(f_{a,j_{n_q}}(\mathbf{x}_t))) \) is the binary representation of \( t \). As a result, if \( \{\mathbf{x}_1, \mathbf{x}_2, \cdots, \mathbf{x}_\ell \} \) is taken to be the channel input alphabet, and the functions \( f_{a,j_1}, f_{a,j_2}, \cdots, f_{a,j_{n_q}} \) are used as the analog processing functions, the receiver can reconstruct the index \( T \) of the
transmitted symbol $x_T$ without error by finding its binary representation as described above. This completes the proof.

**Remark 5.** In the low-SNR regime, one could potentially extend Theorems 1 and 2 to the bounded polynomial degree scenario considered here by evaluating the error bounds on approximation of functions using the Bernstein Polynomial (e.g. [29]).

C. Scenario V: Subset of Quadratic Functions

In this scenario, we consider a special case of Scenario IV, where the analog functions are restricted to specific quadratic polynomials. In particular, the function is generated by \{$x_1, x_2, \cdots, x_{\text{Rank}(h)}, \sum_{i=1}^{\text{Rank}(h)} x_i^2$\}. We have the following theorem for the high SNR capacity.

**Theorem 4.** Let $n_t, n_r, n_q \in \mathbb{N}$, $h \in \mathbb{R}^{n_t \times n_r}$. Then,

$$
\lim_{P \to \infty} C_Q(n_t, n_r, h, P, n_q, F^V_a) = \log \left( \sum_{i=0}^{\text{Rank}(h)+1} \binom{n_q}{i} - \binom{n_q - 1}{\text{Rank}(h)} \right),
$$

*Proof Outline.* The proof follows by noting that each polynomial in $F^V$ can be mapped to a hyperplane in the $\mathbb{R}^{\text{Rank}(h)+1}$ by considering the mapping $(x_1, x_2, \cdots, x_{\text{Rank}(h)}, \sum_{i=1}^{\text{Rank}(h)} x_i^2) \mapsto (x_1, x_2, \cdots, x_{\text{Rank}(h)}, \sum_{i=1}^{\text{Rank}(h)} x_i^2)$. Furthermore, it is well-known that the number of partition regions in $\mathbb{R}^{\text{Rank}(h)+1}$ generated by $n_q$ hyperplanes is $\sum_{i=0}^{\text{Rank}(h)+1} \binom{n_q}{i}$. Also, due to the convexity of the $\text{Rank}(h)$-dimensional surface $L = \{(x_1, x_2, \cdots, x_{\text{Rank}(h)}, \sum_{i=1}^{\text{Rank}(h)} x_i^2) | x_i \in \mathbb{R}\}$ for every closed and convex partition region (polyhedra) $A_j$, either $L \cap A_j = \emptyset$, or there is a region $A_j$ sharing a vertex with $A_j$ such that $L \cap A_j = \emptyset$. So, the maximum number of partition regions with which $L$ intersects is at most $\sum_{i=0}^{\text{Rank}(h)+1} \binom{n_q}{i} - \beta\text{Rank}(h)+1,n_q$, where $\beta\text{Rank}(h)+1,n_q$ is the number of closed (bounded) partition regions. Furthermore, it can be shown that by scaling the partition appropriately, one can ensure that all closed partition regions lie inside $L$ so that the maximum number of intersecting regions $\sum_{i=0}^{\text{Rank}(h)+1} \binom{\frac{n_q}{2}}{i} - \beta\text{Rank}(h)+1,n_q$ is achieved. The proof is completed by noting that $\beta\text{Rank}(h)+1,n_q = \binom{n_q-1}{\text{Rank}(h)}$ as shown in [30].
Remark 6. The capacity region derived in Theorem 4 can be equivalently stated as \( C(n_t, n_r, h, P, n_q, \mathcal{F}_d^V) = \log(\alpha_{\text{Rank}(h)+1,n_q}) \), where \( \alpha_{\text{Rank}(h)+1,n_q} \) is the maximum number of distinct regions generated by \( n_q \) hyperplanes passing through the origin in \( \mathbb{R}^{\text{Rank}(h)+1} \), and \( \alpha_{\text{Rank}(h)+1,n_q} = 2^{\sum_{i=0}^{\text{Rank}(h)+1} \binom{n_q-1}{i}} \).

The equality of these two formulas was shown in [30].

Similar to Theorem 2, one could use SVD to derive the following lower-bound on the low SNR capacity.

**Theorem 5.** Let \( P > 0, n_t, n_r, n_q \in \mathbb{N} \) \( h \in \mathbb{R}^{n_t \times n_r} \). Then:

\[
C_Q(n_t, n_r, h, P, n_q, \mathcal{F}_d^V) \geq \max_{(n_q,i,i]\in\mathcal{N}} \max_{(P,i,i]\in\mathcal{P}} \sup_{A\in\mathcal{B}_{n_q,i}} \sup_{P_{X^n_t}} \sum_{k=1}^{s} I_{A_k}(\tilde{X}_k;V_k),
\]

where \( \mathcal{N} \triangleq \{ (n_q,i,i\in[s] : \sum_{i\in[i]} n_q,i = n_q \} \), \( \mathcal{P} \triangleq \{ (P,i,i\in[s] : \sum_{i\in[i]} P_i = P) \}, \tilde{\mathcal{Y}}_k = \sigma_k \tilde{X}_k + N_k, N^s \) is a vector of i.i.d. zero-mean Gaussian variables with unit variance, \( \sigma_k \) is the kth eigenvalue of \( h \), \( \mathcal{B}_{n_q,i} \) is the set of all partitions of \( \mathbb{R} \) into \( \zeta \) intervals, where \( \zeta = 2n_q \), otherwise, and the mutual information is evaluated with respect to \( P_{X^n_t,V_k}^A \) such that:

\[
P_{X^n_t,V_k}^A(C,\ell) = P(X^n_t\in C, Y^n_r\in A_\ell), C \in \mathbb{R}^{n_t}, k \in [2^n_q], \ell \in [|A_\ell|].
\]

Remark 7. It can be noted that if the analog processing function is restricted to linear functions as in [5], [13]–[20], \( \mathcal{B}_{n_q,i} \) in Theorem 5 would be replaced by the set of all partitions of \( \mathbb{R} \) into \( n_q + 1 \) partitions which leads to a strictly smaller achievable rate.

**IV. Circuit Design for Nonlinear Analog Operations**

In the prequel, we have evaluated the fundamental limits of communication, in terms of achievable rates in MIMO systems with one-bit ADCs equipped with nonlinear analog operations (limited degree polynomials) prior to the ADC operation. In this section, we provide an example of a circuit and provide circuit simulations to justify the feasibility of such nonlinear operations.
The implementation relies on the fact that Complementary Metal-Oxide-Semiconductor (CMOS) and Bipolar transistors — the core components of integrated analog circuits — manifest inherent device-centric nonlinearity by generating integer harmonic frequencies when excited by a sinusoidal input waveform, i.e. \( \cos(\omega t + \phi) \). Various mathematical models to capture transistor nonlinearity exist, among which the adoption of Volterra-Weiner series shown in [31] addresses the general scenario. The nonlinear response of a transistor to a sinusoidal input waveform depends on excitation frequency, \( \omega \). The received modulated signal in a MIMO receiver is a severely attenuated version of the input signal, and is non-monotone. Consequently, it may not be directly applied to a nonlinear transistor, and a two-step procedure involving a pre-processing step followed by nonlinear analog operations is required as described below.

**Step 1: Conversion of the received signal into a monotone sinusoidal.** To explain this step, let us assume that the non-monotone received signal is \( Asinc(\omega_0 t), A \in \{-2, -1, 1, 2\}, \omega_0 > 0 \). This is injected into an integrator circuit [cf. Fig. 3(a)]. For each channel-use, the integrator output after \( T_s > 0 \) seconds (extracted using switches \( SW_1 \) and \( SW_2 \)) is injected to control the voltage of complementary switches \( SW_3 \) and \( SW_4 \), and the two identical variable capacitors with opposite polarities in Fig. 3(b). The resonator circuit generates monotone sinusoidal waveforms with amplitudes proportional to \( |INT(A)| \). The dependence on \( |INT(A)| \) is due to the fact that the associated quality factor \( Q \) of the variable capacitors changes linearly within the possible range of \( |INT(A)| \), thus generating sinusoidal waveforms with varying amplitude and frequency [cf. Fig. 3(b)].

**Step 2: Generating polynomial outputs.** We apply the sinusoidal waveforms generated by the resonator to a nonlinear circuit, so that the frequency harmonics are generated at the output, with amplitude of \( i \)th harmonic proportional to \( B^i \), where \( B \) is the amplitude of the sinusoidal input. To elaborate, in Figure 3(c), we incorporate a differential amplifier circuit [32]. Based on [31], for this circuit, we have \( B_{out} = \alpha B^2 \), where \( \alpha \) is the coefficient of the Volterra-Weiner representation of the nonlinear circuit [33], and \( B_{out} \) is the amplitude of the generated second harmonic signal. It can be noted that the value of \( \alpha \) within the resonator output frequency range remains constant. The amplitude ratio of generated second harmonic waveforms in Fig. 3(c) and the fundamental
Fig. 3. (a) Passing received waveform through an integrator, (b) resonator amplitude follows integrator output, (c) polynomial harmonic generator.

frequency components in Fig. 3(b) illustrate the feasibility of producing polynomial functions of the input amplitude in the analog domain.

V. Conclusion

The application of nonlinear analog operations in MIMO receivers was considered. A receiver architecture consisting of linear analog combiners, implementable nonlinear analog operators, and one-bit threshold ADCs was designed, and the fundamental information theoretic performance
limits of the resulting communication system were investigated. To justify the feasibility of the nonlinear operations, an analog circuit was introduced, and circuit simulations exhibiting the generation of nonlinear analog operations were provided.

APPENDIX A
PROOF OF THEOREM 1

We provide an outline of the proof for \( \text{Rank}(h) = n_r \). The proof for \( \text{Rank}(h) \leq n_r \) follows by similar arguments. Fix partition \( A \in \mathcal{A}_{n_r, n_q} \). Define the collection of functions

\[
f_j(y^{n_r}) = (-1)^{\text{mod}_2(j)}||y^{n_r} - \partial A_k||_2,
\]

where \( y^{n_r} \in \mathbb{R}^{n_r}, j \in \{0, 1, \cdots, n_q - 1\} \), \( \text{mod}_b(a) \) denotes \( a \mod b, k \in [2^n] \) is the index of the partition region for which \( y^{n_r} \in \mathcal{A}_k \), and \( ||y^{n_r} - \partial A_k||_2 \) is the \( \ell_2 \) distance between \( y^{n_r} \) and the boundary of the region \( A_k \). The function \( f_j(\cdot) \) is continuous and its roots are the boundary points of the partition regions \( \mathcal{A}_k, k' \in [2^n] \). Furthermore, its value is positive for all interior points of regions \( \mathcal{A}_k, k' \in [2^n] \) for which \( \text{mod}_2 k' \) is even and is negative otherwise. As a result, \( \text{Sign}(f_j(y^{n_r})), j \in \{0, 1, \cdots, n_q - 1\} \) is the binary representation of the index of \( \mathcal{A}_k \), where \( y^{n_r} \in \mathcal{A}_k \), and \( \text{Sign}(\cdot) \) is equivalent to a zero-threshold one-bit ADC. So, \( I(X^{n_r}; Q_0^n(W^{n_r})) = I_A(X^{n_r}; V) \), where \( Q_0^n(\cdot) \) represents \( n_q \) zero-threshold one-bit ADCs and \( W_i = f_{i-1}(Y^{n_r}), i \in [n_q] \). It remains to show that each \( f_j(\cdot) \) is ‘well-approximated’ by a polynomial function of \( y^{n_r} \). To see this, we let \( L > 0 \) and define \( E_i = 1(|Y_i| < n_r L), i \in [n_r] \). We note that:

\[
I_A(X^{n_r}; V) \leq \sum_{i=1}^{n_r} H(E_i) + I(X^{n_r}; V|E^{n_r})
\]

\[
\leq \sum_{i=1}^{n_r} H(E_i) + P(\exists i \in [n_r] : E_i = 0) \log 2^{n_r} + I_A(X^{n_r}; V|E_i = 1, i \in [n_r])
\]

\[
\leq \sum_{i=1}^{n_r} H(E_i) + \sum_{i=1}^{n_r} P(|Y_i| > n_r L n_q) + I_A(X^{n_r}; V|E_i = 1, i \in [n_r])
\]

\[
\leq \sum_{i=1}^{n_r} H(E_i) + \frac{\gamma n_q}{L} + I_A(X^{n_r}; V|E_i = 1, i \in [n_r]),
\]
where we have defined $\gamma_Y \triangleq \frac{1}{\log n} \sum_{i=1}^{n_r} \mathbb{E}(Y_i)$, (a) holds since $V$ takes at most $2^{n_q}$ values, and (b) follows from Markov’s inequality. Note that $\gamma_Y < \infty$ since $\frac{1}{\log n} \sum_{i=1}^{n_r} \mathbb{E}(X_i^2) \leq P < \infty$. Consequently, by the lower-semi continuity of mutual information $I(X^n; V)$ approaches $I_A(X^n; V|E_i = 1, i \in [n_r])$ as $L \to \infty$. On the other hand, note that $[-n_rL, n_rL]^{n_r}$ equipped with the $\ell_2$ distance is a compact metric space. Hence, by the Stone-Weierstrass Theorem, the polynomial functions are dense in functions defined on $[-n_rL, n_rL]^{n_r}$ and there exists a sequence of polynomial functions $f_{i,j}(), t \in \mathbb{N}$ which converge uniformly to the restriction of $f_j(), j \in \{0, 1, 2, \cdots, n_q - 1\}$ to $[-n_rL, n_rL]^{n_r}$. Consequently, for an arbitrary $\epsilon > 0$, there exists $L$ and $t$ large enough, so that $\sum_{i=1}^{n_r} H(E_i) + \frac{\gamma_{rnq}}{L} \leq \epsilon$, $P(\hat{W}^{nq} = \hat{Q}^{nq}_0(W^{nq})) \geq 1 - \epsilon$, where $W_i' \triangleq f_{i,j}(Y_i^{n_q})$, and

$$|I_A(X^n; V|E_i = 1, i \in [n_r]) - I(X^n; \hat{Q}^{nq}_0(W^{nq})|E_i = 1, i \in [n_r])| \leq \epsilon.$$
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