1/f Noise Characterization of Bilayer MoS 2 Field-Effect Transistors on Paper with Inkjet-Printed Contacts and hBN Dielectrics

Lorenzo Pimpolari,* Gabriele Calabrese, Silvia Conti, Robyn Worsley, Subimal Majee, Dmitry K. Polyushkin, Matthias Paur, Cinzia Casiraghi, Thomas Mueller, Giuseppe Iannaccone, Massimo Macucci, and Gianluca Fiori

1/f noise represents the dominant source of noise in the low-frequency range in several physical systems, including field-effect transistors. Its investigation can provide very important information on the fabrication process, highlighting the steps that are more prone to the introduction of defects. Here, 1/f noise in bilayer MoS 2 transistors on paper with inkjet-printed Ag contacts and hBN dielectric is investigated. These devices are promising building blocks for future low-cost, flexible, and easily recyclable disposable electronics. The analysis of 1/f noise, performed following Hooge’s empirical approach, results in a Hooge parameter \( f_0 = 1-10 \), which is comparable to those reported for bilayer MoS 2 transistors on SiO 2. The present results indicate that the noise properties of the investigated devices are stable against substrate bending and are mainly determined by the printing of the dielectric, while not being sensibly affected by the use of the paper substrate. These results are promising for the further development of low noise 2D material-based flexible electronics on paper.

1. Introduction

In the last few years, there has been an increasing interest toward the development of ubiquitous electronic systems, combining functional features, such as extremely small thickness,[1] small-weight,[2] large mechanical flexibility,[3] wrapping onto irregular surfaces,[4] and wearability.[5] In this context, atomically thin MoS 2 films have attracted particular interest because of chemical robustness and the large availability of the raw material,[6] and have been exploited as channel layer in flexible field-effect transistors (FETs) on polyimide,[7–10] polyethylene terephthalate,[11–14] polyethylene naphthalate,[15] and polydimethylsiloxane substrates.[16]

The continuous increase in the demand of low-cost and disposable electronic systems, also motivated by emerging Internet of Things (IoT) applications, has raised important concerns regarding sustainability, such as the treatment of waste at the end of the product life-cycle.[17] Paper-based consumer electronics offers a simple solution to this issue by combining an environmentally friendly material and simple recycling, with a very low cost and large area flexible substrate.[18] These properties make paper an extremely promising substrate for electronic applications in the “More Than Moore” context, toward a functional diversification of electronic systems, as recently also outlined by the “International Roadmap for Devices and Systems.”[19] MoS 2-based FETs on paper were first obtained by combining functional features, such as the treatment of waste at the end of the product life-cycle.[17] Paper-based consumer electronics offers a simple solution to this issue by combining atomically thin MoS 2 films with average carrier mobility of \( 5.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \) and on-off current ratio of \( 10^4 \) over a statistics of 26 devices, and have been successfully used in digital and analog applications, such as high-gain inverters, AND gates, and current mirrors.[21] These flexible devices exhibited good performance with average carrier mobility of \( 5.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \) and on-off current ratio of \( 10^4 \) over a statistics of 26 devices, and have been successfully used in digital and analog applications, such as high-gain inverters, AND gates, and current mirrors.[21]

In these applications, as well as in sensors and transducer systems often operating at low signal levels, low-frequency noise (LFN, or 1/f noise, where \( f \) is the frequency) is a crucial performance metric.[22,23] In addition, the reduced dimensionality of atomically thin MoS 2 films makes them extremely sensitive to the surface and interface conditions, further increasing the importance of 1/f noise in electronic devices based on this material. LFN has been extensively investigated in mechanically exfoliated single layer,[24] few layer,[25,26] and multilayer[26] as well as chemical vapor deposition (CVD)-grown single layer[27]...
and few layer\cite{26} MoS\textsubscript{2} FETs prepared on rigid substrates such as SiO\textsubscript{2} and Al\textsubscript{2}O\textsubscript{3}. These results indicate that the noise properties of MoS\textsubscript{2} FETs critically depend on material quality and improve with increasing channel thickness, approaching those of graphene for relatively thick films (15–18 layers).\cite{26} Recently, Kaushik and collaborators demonstrated a significant increase in $1/f$ noise in suspended MoS\textsubscript{2} FETs as compared to similar devices on SiO\textsubscript{2}, a result attributed to the larger area exposed to ambient conditions in the suspended configuration.\cite{29} Encapsulation of MoS\textsubscript{2} FETs in Polyethylene (PE) resulted in degraded noise performance with respect to bare devices, as a consequence of the introduction of a large number of traps at the PE/MoS\textsubscript{2} interface.\cite{30} On the other hand, noise reduction was observed exploiting an Al\textsubscript{2}O\textsubscript{3} high-k passivation layer deposited by means of atomic layer deposition, a highly controllable deposition technique.\cite{31} Despite these extensive studies, LFN characterization of a 2D material-based FET on a flexible substrate, which is of high relevance for flexible electronics and optoelectronics applications, has never been reported.

Here, we investigate LFN in printed MoS\textsubscript{2} FETs on paper, exploiting a CVD-grown and later transferred MoS\textsubscript{2} channel, inkjet-printed hBN gate dielectric and Ag contacts. These devices could represent important building blocks for future flexible and easily recyclable electronic systems, provided that their electronic properties are comparable to those of analogue devices prepared using conventional fabrication techniques and are not degraded by substrate bending. Since this technology is still at an embryonic stage, insights into the main physical effects that could be detrimental for device performance (e.g., the presence of defects) are needed. From this point of view, LFN analysis can shed light on the processing steps that are more prone to the introduction of defects and can provide useful guidelines toward the achievement of high-performance devices. In this work, we present the first LFN investigation for a 2D material-based FET with inkjet-printed components and, more in general, for a FET on paper, which represents an important step toward low-cost and distributed electronics on a flexible, and easily recyclable substrate. Obtained results show that the noise properties of fabricated devices are comparable to those reported for analogues devices prepared on rigid substrates using standard microfabrication techniques, hence holding great promise for low-noise electronics based on 2D materials on paper.

2. Results and Discussion

MoS\textsubscript{2} is grown by CVD on a $13 \times 13 \text{ mm}^2$ Al\textsubscript{2}O\textsubscript{3}(0001) substrate. After growth, MoS\textsubscript{2} is patterned into parallel stripes that will form the device channels (Figure 1a). MoS\textsubscript{2} patterning facilitates the following fabrication of FETs as well as the eventual creation of interconnections and circuits.\cite{32} The atomic force microscopy image shown in Figure 1b, taken in the central zone of the substrate, shows that the MoS\textsubscript{2} film is homogeneous in thickness, with a very high area coverage of 98.5%, as determined with the help of the open-source software ImageJ\cite{33} and in agreement with results presented in a previous article.\cite{34} Figure 1c shows a Raman spectrum of the MoS\textsubscript{2} film taken at substrate center. The characteristic $E_{2g^-}^1A_{1g}$ spacing of 21.2 cm$^{-2}$ reveals that the MoS\textsubscript{2} film is bilayer. After patterning, the MoS\textsubscript{2} stripes are transferred onto the paper substrate via a transfer printing technique [see (i) in Figure 1d]. Further details on the MoS\textsubscript{2} growth and transfer procedure are reported in a previous paper.\cite{31} Figure 1d shows a schematic diagram of the FET fabrication sequence, which starts with (ii) inkjet-printing of the Ag source and drain contacts, followed by (iii) inkjet-printing of the hBN gate dielectric on the source and drain contacts as well as on the MoS\textsubscript{2} channel. The hBN film is printed starting from custom-made aqueous solution, whose preparation details, as well as morphological and electrical characterizations, have been reported elsewhere.\cite{33,34} Finally, to conclude the FET fabrication process, the Ag gate contact is inkjet-printed on top of the hBN film (iv). Both the metallic contacts as well as the dielectric film are inkjet-printed using a Fujifilm Dimatix Materials Printer 2850. The Ag contact is printed using a 1 pL nominal volume cartridge, while hBN is printed using a 10 pL nominal volume cartridge. A total of 9 FETs are fabricated and investigated in this study. These devices have channel length ($L$) ranging from 20 to 40 µm, and width ($W$) ranging from 30 to 150 µm, respectively.

An optical micrograph of a representative MoS\textsubscript{2} FET on paper is shown in Figure 2a. The corresponding schematic layout is reported in Figure 2b, showing the FET structure, layer sequence, and the bias voltages applied during electrical characterization. The gate-source voltage ($V_{GS}$) and drain-source voltage ($V_{DS}$) are applied to the gate and drain contacts, respectively, the source contact is connected to ground. All measurements are carried out under ambient conditions and at room temperature. The bias voltages for both DC and noise measurements are supplied with a Keithley 4200A-SCS Parameter Analyzer. For the noise measurements, the channel current fluctuations are amplified with a low-noise amplifier and their spectrum is measured with a SR785 Dynamic Signal Analyzer. Further details on the measurement setup are available in Section S2 (Supporting Information).

The transfer characteristic of one representative FET is reported in Figure 2c for $V_{DS} = 2$ V. The threshold voltage ($V_{th}$) extracted in the linear regime is $-1$ V. Small variations in $V_{th}$ are observed among the fabricated FETs, and for all devices $V_{th}$ is found to be in the range $-1$ to 1 V. The output characteristics of the same device whose transfer characteristic is shown in Figure 2c are reported in Figure 2d. These curves show the presence of a Schottky barrier for low $V_{DS}$ when $V_{GS} < 2$ V, while for larger $V_{GS}$ a linear dependence between the channel current ($I_{DS}$) and $V_{DS}$ is visible, suggesting the presence of an ohmic contact. Formation of ohmic contacts is attributed to the bending of the MoS\textsubscript{2} conduction band with increasing $V_{GS}$, which promotes charge injection from the contacts into the channel. Further details on the nature of the Ag/MoS\textsubscript{2} contacts can be found in Section S1 (Supporting Information).

Electrical noise in FETs is a complex phenomenon, which not only depends on defects or trap states within the semiconductor itself, but can also be influenced by defects located at the semiconductor/substrate as well as the semiconductor/dielectric interfaces.\cite{35} In order to distinguish the contributions of the different potential noise sources, we carried out a step-by-step fabrication of a typically investigated FET, followed by LFN characterization after each fabrication step. In
particular, LFN characterization is performed for the three different steps: i) after the inkjet-printing of the Ag source and drain contacts on MoS$_2$, ii) after inkjet-printing of the hBN gate dielectric, and iii) after inkjet-printing of the Ag top gate contact (i.e., in a FET structure). The step-by-step fabrication and characterization procedure allows us to investigate LFN both when the MoS$_2$ film is exposed to air (Figure 3a, red box), and when it is covered with the hBN gate dielectric (Figure 3a, blue box).

Figure 3b shows $I_{DS}$ as a function of $V_{DS}$, both before and after inkjet-printing of the hBN gate dielectric. After inkjet-printing of the hBN film, an increase in the conductivity of the channel is observed. Indeed, the channel resistance $R_{ch}$ is reduced from 2.96 to 1.82 MΩ after the dielectric deposition. The increased channel conductivity is likely related to doping of the MoS$_2$ active film from the chemicals composing the hBN ink, in analogy to what previously observed in inkjet-printed graphene films.$^{[36]}$ This hypothesis is compatible with the shift of $V_{th}$ toward smaller values observed in the transfer characteristics of back-gated MoS$_2$ FETs fabricated on SiO$_2$/Si, collected prior and after the hBN deposition (see Figure S3 in the Supporting Information). The observed decrease in $V_{th}$ indicates the introduction of n-type doping within the MoS$_2$ film during hBN printing, which is the expected type of doping from the chemicals in the ink.$^{[36]}$

The $I_{DS}$–$V_{DS}$ characteristics reported in Figure 3b indicate the presence of a Schottky-type contact at the different fabrication steps (in agreement with the data reported in Figure 2d), as a consequence of Fermi level pinning at the metal/MoS$_2$ interfaces.$^{[37–39]}$

The power spectral density (PSD) of $I_{DS}$, $S_{I_{DS}}$, normalized to the square of $I_{DS}$ is reported in Figure 3c as a function of $f$, in the low-frequency range between 1 and 200 Hz. The collected spectra are measured for $V_{DS} = 30$ V, corresponding to the region where the current–voltage characteristics have a linear behavior, in order to minimize the contribution of contact resistance to the noise spectra. According to the empirical Hooge law, the LFN PSD can be expressed as$^{[40]}

$$
\frac{S_{I_{DS}}}{I_{DS}^2} = A \frac{1}{f^\gamma}
$$

where $A$ is the noise amplitude, while $\beta$ is the exponent of $I_{DS}$ and $\gamma$ is the exponent of $f$ (which are ideally equal to 2 and 1, respectively, in the case of flicker noise$^{[45]}$). The spectra reported in Figure 3c reveal that the PSD, both prior and after hBN deposition, has a $1/f$ behavior, i.e., $\gamma$ is close to 1, thus confirming that flicker noise is dominating the noise spectrum in the low-frequency range. Further considerations on $\gamma$ will be discussed in the following. After printing the hBN film,
The measured PSD is found to increase by about one order of magnitude, as compared to the value recorded for bare MoS\(_2\). A comparable behavior has also been observed for all other measured devices (see Figure S4 in the Supporting Information), suggesting that inkjet-printing of hBN introduces defects and trap states at the interface with MoS\(_2\), similarly to what previously reported for PE-passivated MoS\(_2\) FETs.\(^{[30]}\) The significant increase in noise level after printing of hBN indicates that, from the noise point of view, this is the most critical fabrication step for the proposed FETs. This result is not surprising when considering the fact that the hBN flakes inkjet-printed on MoS\(_2\) present a broad orientational distribution and chemical residuals.

After evaluating how the hBN gate dielectric contributes to the noise level in two-terminal devices, the 1/\(f\) noise is investigated in MoS\(_2\) FETs. The PSD as a function of \(f\) is reported in Figure 4a, for the same FET whose transfer and output characteristics are shown in Figure 2c,d, for \(V_{GS} = 8\) V and \(V_{DS}\) ranging from 250 mV to 5 V. Under these conditions, the FET is operating in the linear regime (i.e., \(V_{DS} < V_{GS} - V_{th}\)). Also in this

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**Figure 2.** Electrical characterization of MoS\(_2\) FETs on paper. a) Optical micrograph showing an individual MoS\(_2\) FET on paper. The scale bar corresponds to 250 \(\mu\)m. In the inset, a vial containing the hBN ink used to inkjet-print the gate dielectric is shown. b) Schematic diagram of the FET structure, showing its layer sequence and biasing voltages. c) Transfer characteristic of one of the fabricated FETs, measured for \(V_{GS} = 2\) V. In the inset, an optical micrograph showing arrays of MoS\(_2\) FETs fabricated on the paper substrate are reported. d) Output characteristics of the same FET whose transfer characteristic is shown in c). The step in \(V_{GS}\) equals 1 V.

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**Figure 3.** Optical micrographs of 2 contact MoS\(_2\) devices and their electrical characterization. a) Optical micrographs showing the investigated device prior (top, red box) and after (bottom, blue box) hBN printing. The scale bars correspond to 250 \(\mu\)m. b) Current–voltage characteristic and c) normalized PSD of the shown two-contact MoS\(_2\) device taken prior and after hBN deposition. The ideal 1/\(f\) slope is reported in c) as a reference.
case, for all the studied bias conditions the 1/f noise is found to be the dominant source of noise in the investigated frequency range, and no corner frequency to white noise is observed. The inset of Figure 4a shows a log–log plot of $S_{IDS}$ as a function of $I_{DS}$ for the same device. The linear fit to the experimental data returns a value of $\beta = 2.08$, thus confirming the presence of an ohmic contact between the inkjet-printed Ag contacts and the MoS$_2$ channel at the considered $V_{GS}$. For few investigated FETs, a value of $\beta$ smaller than 2 is extracted for the same bias conditions, which might indicate the presence of contact noise introduced by non-ohmic contacts in these devices. Further details on contact noise in the investigated MoS$_2$ FETs are available in Section S5 (Supporting Information).

Figure 4b shows the PSD of the FET under investigation collected for different values of $V_{GS}$, ranging from 0 to 10 V. For all measurements, $V_{GS}$ is larger than $V_{th}$ and 1/f noise dominates the noise spectra. The Hooge formula [Equation (1)] can be rewritten as

$$\frac{S_{IN}}{\nu_{DS}} = \frac{\alpha_H}{N} \frac{1}{f}$$

(2)

where $\alpha_H$ is the Hooge parameter, and $N$ is the total number of carriers in the channel ($\beta$ and $\gamma$ are approximated to 2 and 1, respectively). In the linear regime, $N$ can be approximated as $N \approx (V_{GS} - V_{th})LWC_G/q$, where $C_G$ is the gate capacitance per unit area, and $q$ the elementary electric charge. Therefore $1/A$ is expected to be proportional to $V_{GS}$, which is confirmed by the experimental data reported in Figure 4c, extracted from the results in Figure 4b. In Figure 4d, we report the value of $\gamma$ as a function of $V_{GS}$ (again from the results of Figure 4b): it is almost constant, with an average value of 1.2, very close to the ideal value of 1. The linear dependence between $1/A$ and $V_{GS}$ that we observed in our bilayer MoS$_2$ FETs on paper was also reported in previous articles on mechanically exfoliated and CVD-grown monolayer MoS$_2$. On the other hand, a superlinear or quadratic relationship between these quantities was observed in other publications, suggesting that the fabrication methods, the nature and density of crystallographic defects, as well as the measurement conditions have a strong impact on experimental results for flicker noise in MoS$_2$ FETs.

Hooge’s parameter $\alpha_H$ is independent on device area, and hence can be used as a figure of merit for a direct comparison with previous results reported in the literature. For the device reported in Figure 5a, we extracted $\alpha_H = 1.4$, and for all investigated devices $\alpha_H$ ranges from 1.1 to 11.4 (with an average value of $\approx 5$), as shown in Figure 5b. These values are comparable to those previously reported for mechanically exfoliated and CVD-grown monolayer MoS$_2$ with grain boundaries on SiO$_2$/Si measured under ambient conditions, as well as for CVD-grown monolayer MoS$_2$-FETs with Ti/Au contacts measured in

Figure 4. LFN characterization of MoS$_2$ FETs on paper. a) PSD for the device whose transfer and output characteristics are reported in Figure 2c,d, respectively, measured for $V_{DS}$ ranging from 0.25 to 5 V. The inset shows the dependence of $S_{IN}$ on $I_{DS}$. b) PSD measured for $V_{GS}$ between 0 and 10 V (step of 1 V) and $V_{DS} = 2$ V. As a reference, the ideal 1/f slope is reported both in a) and b). c) $1/A$ as a function of $V_{GS}$. A linear fit to the experimental data is shown as a dashed line. d) $\gamma$ as a function of $V_{GS}$. The blue dashed line is a guide to the eyes. All measurements reported in a–d) are taken on the same device.
Remarkably, the obtained values of $\alpha_H$ are also comparable to those found for mechanically exfoliated bilayer MoS$_2$ on SiO$_2$/Si exploiting evaporated Cr/Au contacts and measured under ambient conditions. The obtained results point out that the noise properties of bilayer MoS$_2$ are not sensibly affected either by film patterning, transfer, and integration on a flexible paper substrate, or by the use of inkjet-printed Ag contacts. Noise measurements are therefore useful to identify methods to optimize the hBN/MoS$_2$ interface, for example by postfabrication thermal treatments, by exploitation of a high-$k$ passivation layer, or by increasing the thickness of the MoS$_2$ film in order to take advantage of the stronger screening capability of thicker films. Further details on the influence of thickness are available in Section S6 (Supporting Information).

The data reported in Figure 5 highlight a device-to-device variation in the measured noise of about one order of magnitude, which, as demonstrated by the measurements reported in Figure S4 (Supporting Information), is mainly due to nonidealities of the MoS$_2$ film itself, and not to the printed hBN dielectric. This is not surprising considering that the investigated devices are fabricated in random positions of a cm-scale MoS$_2$ film which, for its intrinsic nature, exhibits small inhomogeneities caused by flux and temperature gradients across the substrate during growth. Remarkably, the observed noise variation is comparable to or even smaller than that observed in both mechanically exfoliated and CVD-grown single-flake MoS$_2$-FETs fabricated on SiO$_2$.

LFN measurements can also be used as powerful tools to investigate the electromechanical properties of the proposed devices. Indeed, the comparison between the power spectral densities measured with and without mechanical strain applied to the device, can provide useful information on whether and how much the electric transport of the device is affected by the applied stress, which is of crucial importance for flexible and wearable electronic applications.

The mechanical measurements are carried out by measuring the PSD of the channel current applying both tensile and compressive strain to the investigated device by bending the substrate around rigid jigs with different radii, down to 12 mm. The graphs in Figure 6a show the normalized power spectral densities of the channel current collected without the application of mechanical stress (red curve), with the application of tensile strain using a bending radius of 12 mm (blue curve), and again in nonbending conditions, after removal of the applied stress (green curve). The same considerations are valid for the graph of Figure 6b, but in this last case a compressive strain is applied. In both cases there are no major changes in the measured power spectra under the investigated strain conditions. This suggests that the applied mechanical stresses do not introduce delamination of the channel or an increase in the density of defects or traps, and constitutes a promising result in the context of flexible and wearable applications.
3. Conclusion

To summarize and conclude, we have investigated 1/f noise in bilayer MoS$_2$ FETs on paper, exploiting inkjet-printed hBN gate dielectric and Ag contacts, which represent promising building blocks for a wealth of IoT applications on a flexible, large area, low-cost, and easily recyclable substrate. 1/f noise analysis revealed that inkjet-printing of hBN increases the noise level in two-contact MoS$_2$ devices by about one order of magnitude, hence representing the device fabrication step that mostly affect the noise properties. The extracted Hooge parameter is in the range of 1.1–11.4, which is comparable to values previously reported for bilayer MoS$_2$ FETs on SiO$_2$ with evaporated metal contacts. This observation indicates that the noise properties of bilayer MoS$_2$ FETs are not degraded by device integration on paper or by the use of inkjet-printed Ag contacts, in agreement with the values of mobility and on-off current ratio, which are also comparable between the two technologies. Measurements carried out under the application of mechanical stress have shown that the fabricated devices are stable against substrate bending and their noise level is not affected by the applied tensile or compressive strain down to a curvature radius of 12 mm. Present results are promising for the further development of 2D material-based paper electronics for a broad range of applications that require low noise levels, such as analog front-end for sensors, an application of growing interest in the IoT context.

4. Experimental Section

Growth, Characterization, and Transfer of MoS$_2$: Bilayer MoS$_2$ is grown by CVD on a $13 \times 13$ mm$^2$ Al$_2$O$_3$(0001) substrate. CVD growth is performed at atmospheric pressure using ultrahigh-purity Ar as the carrier gas, following the procedure reported in a previous paper.[$^{[21]}$] The grown film has been characterized by atomic force microscopy (using a Veeco NanoMan vs atomic force microscope), in semicontact mode at ambient conditions, and Raman spectroscopy, with illumination at 532 nm [the output signal has been measured using a spectrometer Horiba iHR320, with a grating with 1800 grooves mm$^{-1}$ and a liquid nitrogen cooled CCD detection system (Symphony II)]. These characterizations revealed that the film is homogeneous in thickness with an area coverage of 98.5%, and is bilayer. After growth, the MoS$_2$ film is patterned by means of Ar/SF$_6$ plasma etching and transferred to the target paper substrate (PEL P60, purchased from Printed Electronics Limited) following the procedures reported in a previous work.$^{[21]}$

Device Fabrication: MoS$_2$ transistors were fabricated in a top-gate configuration using the transferred MoS$_2$ stripes as channel material. The metal contacts and the gate dielectric were inkjet-printing using a Fujifilm Dimatix Materials Printer 2850. A commercial silver ink (purchased from Sigma-Aldrich) was used to print the contacts, while for the gate dielectric a custom-made hexagonal boron nitride (hBN) ink with a concentration $\approx 2$ mg mL$^{-1}$ was employed. The Ag contacts were printed using a 1 pl nominal volume cartridge, while hBN was printed using a 10 pl nominal volume cartridge. All films were printed at room temperature with a drop spacing of 20 $\mu$m.

Electrical and Noise Characterization: For both electrical and noise measurements the bias voltages were supplied using a Keithley 4200A-SCS Parameter Analyzer. For the noise measurements, the channel current fluctuations were amplified with a low-noise amplifier (based on the integrated circuit LT1793) and the corresponding noise spectra were collected with a SR785 Dynamic Signal Analyzer in the frequency range from 1 to 200 Hz, with a line width of 250 mHz and 800 FFT points. Further details on the measurement setup are available in Section S2 (Supporting Information). All measurements were carried out under ambient conditions and at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

L.P. and G.C contributed equally to this work. The authors acknowledge the ERC PEP2D (Contract No. 770047), H2020 WASP (Contract No. 8025213), and the Graphene Flagship Core3 (Contract No. 881603). R.W. acknowledges the Hewlett-Packard Company for financial support in the framework of the Graphene NOWNANO Centre for Doctoral Training.

Conflict of Interest

The authors declare no conflict of interest.
Data Availability Statement

Research data are not shared.

Keywords

1/f noise, 2D materials, inkjet-printing, MoS2 transistors, paper electronics

Received: March 19, 2021
Published online: May 29, 2021