AutoCellLibX: Automated Standard Cell Library Extension Based on Pattern Mining

Tingyuan Liang*, Jingsong Chen†, Lei Li† and Wei Zhang*
*ECE Department, Hong Kong University of Science and Technology; †Huawei Technologies Co., Ltd. Shenzhen, China
tliang@connect.ust.hk, chenjingsong5@huawei.com, lilei291@huawei.com, eeweiz@ust.hk

Abstract—Custom standard cell libraries can improve the final quality of the corresponding VLSI designs but properly customizing standard cell libraries remains challenging due to the complex characteristics of the VLSI designs. This paper presents an automatic standard-cell library extension framework, AutoCellLibX. It can find a set of standard cell cluster pattern candidates from the post-technology mapping gate-level netlist, with the consideration of standard cell characteristics and technology mapping constraints, based on our high-efficiency frequent subgraph mining algorithm. Meanwhile, to maximize the area benefit of standard cell merging, AutoCellLibX includes our proposed pattern combination algorithm which can iteratively find a set of gate-level patterns from numerous candidates as the extension part of the given initial standard cell library. To the best of our knowledge, AutoCellLibX is the first automated standard cell extension framework that closes the optimization loop between the analysis of gate-level netlist and standard cell library customization for VLSI design productivity. The experiments with FreePDK45 library and benchmarks from various domains show that AutoCellLibX can generate the library extension with up to 5 custom standard cells within 1.1 hours for each of the 31 benchmark designs and the resultant extension of the standard cell library can save design area by 4.49% averagely.

Index Terms—standard cell synthesis, dynamic standard cell library, design technology co-optimization, frequent sub-graph mining

I. INTRODUCTION

Digital VLSI designs are getting much larger and more complex as manufacturing technologies are making rapid progress. Standard cell-based designs exploit libraries of small predefined building blocks called standard cells, which facilitate the productivity and reliability of the VLSI design flow. Accordingly, standard cell libraries have a fundamental impact on the quality of VLSI designs, e.g., power, performance, area, and cost (PPAC) [1].

A. Background of Standard Cell Merging

Since commonly-used standard cell libraries cannot meet all the requirements in some special scenarios [2][3], as an alternative solution, academia [6][19] and industry [5][20][23] take continuous efforts to extend standard cell libraries with custom standard cells for their technology nodes and domain-specific designs. One of the potential sources of these custom standard cells is standard cell merging, which merges several existing standard cells into a new one with an optimized layout, as a simplified example shown in Fig. 1. It can benefit the design flow from two aspects:

• It enlarges the back-end solution space of the VLSI design, e.g., placement and routing, and hence enables some design goals which cannot be achieved based on the original standard cell library, via transistor-level optimizations like diffusion sharing and in-cell signal routing [8].
• It shrinks the problem scale of the VLSI back-end tools by reducing the number of gates in the post-technology mapping gate-level netlist and enforcing pre-defined relative position constraints. These factors facilitate the tools to converge at better results [24].

Standard cell merging provides noticeable optimization potentials but it is critically challenging since numerous factors, e.g., the design context, transistor layout, design rules and expected PPAC metrics, should be considered to realize a beneficial library. First, as for the design context, designers should identify the characteristics of the target design to locate the optimization opportunities and design pattern mining is one of the promising approaches. Second, the transistor network and layout should be designed under the constraints of design rules and PPAC metrics, which is usually called standard cell layout synthesis. In this paper, we propose a fully automatic standard-cell library extension framework, AutoCellLibX which can analyze characteristics of the target gate-level netlist and extent an initial standard cell library with custom complex standard cells to minimize the area cost. Related works and challenges are discussed in Section I-B and I-C respectively.

B. Related Works

1) Standard Cell Layout Synthesis: This workflow takes in three types of inputs [6][19]: (A) cell architecture settings, e.g., the number of routing tracks, and the location of power rails; (B) design rules, e.g., width/spacing rules for all mask layers depending on cell architecture; and (C) transistor netlist indicating the interconnection of sized library cells. With these inputs, standard cell layout synthesis will conduct transistor placement, in-cell routing, and design rule checking. The general objectives of this synthesis flow are to improve the performance and lower the consumption of area/power.

Cellerity [6] was proposed in 1997 as a comprehensive standard cell layout synthesis flow. It consists of simulated annealing transistor placement, Echelon in-cell router [23], and SQUEEZE layout compactor [25]. In 2014, ASTRAN [8], an open-source standard cell layout synthesis framework, was released and it realized promising results based on a cell layout compaction methodology using MILP.
Moreover, some solutions \cite{27,29} related to layout regularity and pin access optimization have been done. Recently, a series of researches targeting sub-10nm technology nodes \cite{15,19} were presented, most of which utilized SMT solvers to optimize the layout of cell designs and, \cite{30} realized efficient simultaneous transistor folding and placement. These frameworks focus on the transistor layouts, and the analysis of the overall gate-level netlist and the input of customization are left to the manual effort.

2) \textbf{Design Pattern Mining: Isomorphic design patterns} are defined as the identical or functionally equivalent logic structures which recur frequently in the entire design, as an example shown in Fig. 2. Most styles of the manual design flow, design architecture, synthesis, or mapping have a bias to generate recurring regular patterns in the gate-level netlists \cite{5}. Such regularity can guide the standard cell design since frequently-recurring patterns imply the high coverage and reuse of the corresponding custom standard cell designs.

Accordingly, design pattern mining is to identify which part of the gate-level netlist should be replaced by custom standard cell designs. It’s hard since the netlists are large and complex and related solutions were not provided in the aforementioned previous works \cite{5,12,14,23}. In some works on synthesis, placement, and routing, researchers have tried to extract template-based regularity from gate-level netlists, e.g., datapath \cite{31,34} or array \cite{35}, but it is hard for these template-based solutions to handle the general gate-level netlists with complex interconnections. Moreover, they did not check the isomorphism between the patterns.

Frequent subgraph (pattern) mining (FSM) is a hot topic of computer science with some matured solutions like \cite{16,39}. These techniques have been widely applied in many domains to extract patterns \cite{40}, such as chemistry, web, social network, and biology. Only a few works \cite{41,42} have been done for VLSI gate-level netlist. Moreover, they mainly focused on directly applying FSM algorithms like \cite{37} on gate-level netlists to find frequent sub-circuits and the consideration of VLSI characteristics was absent in their solutions.

C. Challenges of Automated Standard Cell Library Extension

To realize the co-optimization of designs and standard cell library and close the loop of netlist pattern mining and standard cell layout synthesis, we need to overcome the following challenges:

- Without identifying the promising pattern subgraphs as the inputs of standard cell layout synthesis, the resultant custom standard cell might not benefit the VLSI design. Meanwhile, simply selecting one or two patterns from the customization candidates to create new standard cells cannot realize the optimal solution, e.g., minimizing area cost. Therefore, we need to find the proper combination of patterns.
- Without the consideration of the requirements of VLSI design flow, FSM algorithms cannot find the optimal candidates for standard cell layout synthesis. For example, in previous works, their FSM solutions simply focused on the frequency of pattern recurrence in the gate-level netlist. However, pattern coverage and area saving after customization should be considered. Moreover, the overlapped pattern subgraphs in the netlist should not be counted more than once since each node in the netlist can be mapped to only one standard cell during the mapping flow in logic synthesis. Finally, it is difficult to identify the patterns from large and complex gate-level netlist since the general FSM algorithms are timing-consuming and memory-intensive.

With the consideration of the scenarios in real applications discussed above, the contributions of AutoCellLibX are highlighted as follows:

- A practical vertex encoding algorithm, which can find a proper set of neighbor vertex for pattern growth with the consideration of standard cell characteristics, as a part of high-efficiency FSM solution;
- A pattern growth algorithm that can expand the sizes of gate-level patterns while preserving their high recurrence frequencies. Compared to previous FSM approaches, our pattern growth solution carefully handle the overlaps between pattern subgraphs to meet the technology mapping constraint and maximize area reduction;
- A pattern combination algorithm which can iteratively find a set of gate-level patterns from numerous candidates as the extension part of the initial standard cell library to maximize the area reduction of the entire VLSI design;
- To the best of our knowledge, it is the first automated standard cell extension framework that closes the optimization loop between the analysis of gate-level netlist and standard cell library customization. AutoCellLibX can generate SPICE netlists and GDSII layouts of the custom standard cells for downstream VLSI design flow.

II. Preliminaries

In this section, we formulate the pattern mining problem in the scenarios of standard cell library extension and present an overview of our proposed framework.

A. Problem Formulation

The post-technology mapping gate-level netlist can be formulated as a directed graph $G = (V, E, L_v, L_e)$ with the following definitions:

- vertices $V(G) = \{v_1, v_2, \ldots, v_n\}$ represent cells after technology mapping in the gate-level netlist with flip-flops removed. The reason for such cell removal is that sequential circuits consist of combinational logic gates and sequential memory elements, and our targets of customization are the combinational logic gates.
- edges $E(G) = \{e_1, e_2, \ldots, e_m\}$ represent $m$ pin-to-pin nets according to the driver-sink relationships in the gate-level netlist $L_{v_i}$ represents the label for vertex $v_i$, which is the standard cell type of $v_i$.
- $L_{e_i}$ represents the label for edge $e_i$, which is a tuple $(\text{Output}_{i_1}, \text{Input}_{i})$, indicating that the edge $e_i$ connects an output pin named $\text{Output}_{i_1}$ of its driver cell and an input pin named $\text{Input}_{i}$ of its sink cell.
A pattern group \( PGS_i = \{G_1', G_2', \ldots, G_{N_s}'\} \) is a set of \( N_s \) subgraphs of \( G \). All the vertices in each subgraph in \( PGS_i \) are connected. The subgraphs in \( PGS_i \) are isomorphic, and it means that the sub-circuits corresponding to these subgraphs have the same circuit functionality. They are not overlapped with each other, i.e., when \( p \neq q \) and \( G'_p, G'_q \in PGS_i \), we have \( V(G'_p) \cap V(G'_q) = \emptyset \).

The coverage of a pattern group \( Cov(PGS_i) \) is the number of vertices in it, i.e., \( Cov(PGS_i) = |V(G'_1) \cup V(G'_2) \cup \cdots \cup V(G'_{N_s})| \), where \( G'_i \in PGS_i \).

A combination of pattern candidates \( C = \{PGS_1, PGS_2, \ldots, PGS_{N_P}\} \) is a set of \( N_P \) pattern groups. The subgraphs in different pattern groups are not isomorphic, and they are not overlapped with each other, i.e., \( \forall PGS_i, PGS_j \in C \), when \( i \neq j \), \( \forall G' \in PGS_i, \forall H' \in PGS_j, G' \) is not overlapped with \( H' \).

A reward function \( R(C, G) \) indicates how much area can be saved for \( G \) when each subgraph \( G'_i \) in the pattern groups of \( C \) is replaced by a corresponding custom standard cell generated by standard cell layout synthesis flow.

According to the definitions above, the problem of standard cell library extension can be formulated as follows: given a gate-level netlist \( G \) and the initial standard cell library \( LIB \),

\[
\max_C R(C, G) \quad \text{s.t.} \quad |C| < N_p \quad \forall G' \in PGS_i \subset C, |G'| < S_p
\]

where \( N_p \) is the maximum number of custom standard cell types and \( S_p \) is the maximum number of vertices in each pattern subgraph. These two parameters are determined by designers to limit the size of the extended library and the size of the custom standard cell. Empirically, in our implementation, \( N_p = 5 \) and \( S_p = 10 \) respectively, since when these parameters become larger, the area benefit is marginal for the benchmarks. More discussion about these parameters can be found in Section III-E.2 The resultant \( C \) will be used to complement \( LIB \) and generate a new extended \( LIB' \).

B. The Framework of AutoCellLibX

The workflow of AutoCellLibX is shown in Fig. 3. The inputs of AutoCellLibX are the post-technology mapping gate-level netlist (BLIF file) of the target VLSI design generated by Yosys and an initial standard cell library used during the logic synthesis. The outputs are the SPICE netlists, GDSII layouts and the area reduction report of the combination of patterns. The workflow overview of AutoCellLibX is described in this subsection.

1) Initial Pattern Seed Identification: Initial pattern seed identification generates a set of initial 2-level tree-based patterns, \( L_{init} \), which will be the starting point of later iterative pattern growth for standard cell customization.

2) Neighbor Encoding: In the iterative loop, the first stage is to efficiently enumerate and encode the neighbor vertices of subgraphs in the target pattern group \( PGS_{tgt} \) with the highest coverage in a list of sorted patterns, \( L_{iter} \) (or \( L_{init} \)), to find the promising direction of the pattern growth.

3) Pattern Growth: Inspired by [37], some of the encoded neighbor vertices will be absorbed into the subgraphs in \( PGS_{tgt} \) and a new pattern group \( PGS'_{tgt} \) with subgraphs of larger size is generated. Meanwhile, the global pattern information will be updated to improve the efficiency of later iterations of pattern mining.

4) Generation of SPICE Netlist and GDSII Layout: According to the graph topology and label information in the new pattern group \( PGS'_{tgt} \), a SPICE netlist indicating the interconnection of sized transistors for a potential custom standard cell will be generated. With the SPICE netlist and predefined design rules of the initial standard cell library, ASTRAN [8], the open-source standard cell layout synthesis tool, will be called to generate the GDSII layout of the custom cell.

5) Pattern Combination Evaluation: According to the generated GDSII layouts and the recurrence frequencies of the pattern groups, the overall benefit of a potential combination of patterns are evaluated by replacing corresponding subgraphs in \( G \) with the custom standard cells. In this stage, AutoCellLibX will analyze the improvement potential of the patterns and make the decision whether further pattern mining iterations should be terminated.

As shown in Fig. 3 neighbor encoding, pattern growth, generation of SPICE netlist and GDSII layout, and pattern combination evaluation are the five successive stages in the iterative pattern mining loop.

III. IMPLEMENTATION OF AUTOCELLLIBX

A. Initial Pattern Seed Identification

The pattern growth procedure is to let some frequent subgraphs gradually absorb their neighbor vertices and initial patterns are the seeds of pattern growth in FSM algorithms.

In conventional solutions, like [37][39], which mainly count the frequencies of various subgraph patterns without other constraints, the initial patterns are simply all the edges with two interconnected vertices in \( G \). For the general scenarios of standard cell customization without considering logic duplication, each vertex in the gate-level netlist should be mapped to only one standard cell during technology mapping. Edge-based initial patterns might lead to the result that some vertices will be covered by multiple pattern subgraphs, such as high-fanin cells and broadcast signals. For example, the NOR3X1 cell with index 0 is connected with two AND2X2 cells in Fig. 4(a), but the NOR3X1 cell can be mapped to only one custom standard cell with one of the two AND2X2 cells.

To consider the constraint aforementioned, our pattern seed identification employs tree encoding as illustrated in Algorithm 1.

1) Initial Tree Encoding: In \( G \), each vertex will be regarded as a root, and its 1-hop predecessors will construct a 2-level tree with the root vertex. Each of these trees will be encoded with a tree code, according to the steps shown in line 1-13 of Algorithm 1. The tree code for a tree consists of two parts: the code of root (root code) and the code of leaves (leaf codes). The root code is simply the standard cell type of the root, like "[NOR3X1]". The leaf code for each leaf in the tree will be a code including its standard cell type, and the label of the edge interconnecting the root and it, i.e., \( L_e \) in Section II-A. For example, "(AND2X2,Y,A)"
for AND2X2 cell with index 1 in Fig. 4(a) means that the output pin "Y" of an AND2X2 cell is connected to the input pin "A" of the root NOR3X1 cell. The tree code is the root code followed by the leaf codes of leaves, where the leaf codes are concatenatd in the lexicographical order (line 5 in Algorithm 1). For example, the tree code for the initial tree in red dash curve in Fig. 4 is "[NOR3X1, AND2X2, Y, A, AND2X2, Y, B, NOR3X1, Y, C]". It can be noticed that the tree code includes all the information of the corresponding tree, e.g., the vertices, the edges between them, and related labels. Meanwhile, due to the lexicographical order of the codes of leaves in each tree code, each of these initial tree subgraphs will be mapped to only one tree code. Therefore, trees with the same tree code are isomorphic.

As described in lines 8-13 in Algorithm 1, AutoCellLibX will enumerate the vertices in $G$, construct corresponding pattern trees, encode the trees and record the recurrences of the tree patterns based on the codes. According to the recurrence record, we can rank the initial patterns in descending order of their recurrence frequencies.

2) Overlap Elimination: Please note that at this stage, the pattern subgraphs could overlap with some other patterns at some of the vertices. As described in lines 14-21 in Algorithm 1 to eliminate these overlaps, AutoCellLibX will enumerate the patterns from those most frequent ones to those less frequent to conduct checking. If all the vertices in a subgraph have not been occupied, these vertices will be marked as occupied. Otherwise, the subgraph will be abandoned from the record. As an example shown in Fig. 4(b), if a pattern subgraph overlaps, one of the subgraphs will be abandoned if it is visited later or belong to a pattern with a lower frequency. In this way, AutoCellLibX removes the overlaps among the subgraphs in the patterns and preserves those high-frequency subgraph patterns for the reuse of custom standard cells. After the elimination of the overlaps, the pattern groups with different tree codes will be recorded in $L_{init}$ and ranked in descending order of their coverage in $G$. i.e. $Cov(PGS_i)$ defined in Section II-A, for later iterative pattern growth, since it is more likely for the patterns with high coverage to realize a noticeable impact on the entire design according to Section II-E.

3) Post-process for Iterative Pattern Mining: Each vertex in a tree will be assigned an index in the tree to facilitate isomorphism checking among subgraphs with the same pattern in later procedures. Root vertex will have an index of 0 while the predecessor vertices will be indexed from 1 to the number of predecessors, according to the lexicographical order of their leaf codes. For example, as shown in Fig. 4(a), the bottom NOR3X1 cell has an index of 0, and the two AND2X2 cells are assigned index 1 and 2 respectively. This index will be used in neighbor encoding in Section III-B2.

B. Neighbor Encoding

Our pattern mining procedure is based on pattern growth which gradually merges some selected vertices into the subgraphs of existing patterns to enlarge the pattern size while trying to preserve the recurrence frequencies of the patterns. Therefore, selecting proper neighbors is a critical part of pattern mining, which will be illustrated in this subsection.

AutoCellLibX will take the top-1 pattern group $PGS_{tgt}$ which has the highest coverage in the gate-level netlist, from $L_{init}$ or $L_{iter}$, as the input of neighbor encoding as depicted in Fig. 3. Correspondingly, the outputs of neighbor encoding are a set of neighbor vertices of $PGS_{tgt}$ and their pattern codes. The overall steps of neighbor encoding are presented in Algorithm 2.

1) Neighbor Enumeration: As shown in lines 14-20 of Algorithm 2 in this stage, AutoCellLibX will enumerate the neighbors of $PGS_{tgt}$, for each pattern in $PGS_{tgt}$, the top-1 pattern group $PGS_{tgt}$, and their pattern codes.

Algorithm 1: Initial Pattern Seed Identification

| Function                                      | Input                                      | Output                                      |
|-----------------------------------------------|--------------------------------------------|---------------------------------------------|
| TreeEncode(root, predecessors)               |                                            | Pattern list in descending order of the frequencies of the initial patterns $L_{init}$ = (PGS)|
| predCodes = {}                               |                                            |                                            |
| foreach $v_i \in$ predecessors do            |                                            |                                            |
|    predCodes.append(stdCellType($v_i$)+Le(root,$v_i$)); |                                            |                                            |
| return concat(stdCellType(root), lexSort(predCodes)); |                                            |                                            |
| code2Trees = record of the trees with the same code; |                                            |                                            |
| code2Freq = record of the code frequency;    |                                            |                                            |
| foreach $root \in V$ do                      |                                            |                                            |
|    preds = getPreds(root); // get direct 1-hop predecessors |                                            |                                            |
|    treeCode = TreeEncode(root, preds);       |                                            |                                            |
|    code2Freq[treeCode] += 1;                 |                                            |                                            |
|    code2Trees[treeCode].append(getTree(root)); |                                            |                                            |
| sortedCodes = sortPatternCodes(code2Freq);  |                                            |                                            |
| /* construct trees and encode them */        |                                            |                                            |
| /* eliminate overlaps */                     |                                            |                                            |
| foreach code $\in$ sortedCodes do            |                                            |                                            |
|    foreach tree $\in$ code2Trees[code] do    |                                            |                                            |
|        if allVerticesAreUnoccupied(tree) then |                                            |                                            |
|            OccupAndIndexAllVerticesIn(tree);  |                                            |                                            |
|        else                                   |                                            |                                            |
|            code2Freq[code] -= 1;              |                                            |                                            |
|            code2Trees[code].remove(tree);     |                                            |                                            |
| $L_{init}$ = sortedPatternListAccordingToCoverage(code2Trees); |                                            |                                            |
| return $L_{init}$                            |                                            |                                            |

Algorithm 2: Neighbor Encoding

| Function                                      | Input                                      | Output                                      |
|-----------------------------------------------|--------------------------------------------|---------------------------------------------|
| NeighborEncode(neighbor, patternSubG)        |                                            | record of the neighbor vertices of $PGS_{tgt}$ and their pattern codes |
| codes = {}                                    |                                            |                                            |
| /* construct the edge codes */                |                                            |                                            |
| foreach $v_i \in$ patternSubG do             |                                            |                                            |
|    viIndex = getIndex($v_i$, patternSubG);    |                                            |                                            |
|    if neighbor is driver of $v_i$ then        |                                            |                                            |
|        codes.append(L(neighbor, $v_i$)+viIndex); |                                            |                                            |
|    else                                       |                                            |                                            |
|        codes.append(viIndex+Le($v_i$, neighbor)); |                                            |                                            |
| return concat(stdCellType(neighbor), lexSort(codes)); |                                            |                                            |
| code2Neighbors = record of the neighbors with the same code; |                                            |                                            |
| neighbor2Subgraph = record of the owner subgraph of a neighbor; |                                            |                                            |
| code2Freq = record of the code frequency;    |                                            |                                            |
| encoded = record of encoded vertices;         |                                            |                                            |
| /* enumerate the neighbors of the subgraphs in $PGS_{tgt}$ and encode them */ |                                            |                                            |
| foreach subG $\in$ $PGS_{tgt}$ do             |                                            |                                            |
|    foreach neighbor $\in$ 1-hop neighbors of subG do |                                            |                                            |
|        if NOT encoded[neighbor] then           |                                            |                                            |
|            code = NeighborEncode(neighbor, subG); |                                            |                                            |
|            neighbor2Subgraph[neighbor] = subG; |                                            |                                            |
|            encoded[neighbor] = True; // avoid overlaps |                                            |                                            |
|            code2Neighbors[code].append(neighbor); |                                            |                                            |
| return code2Neighbors, neighbor2Subgraph     |                                            |                                            |
all the subgraphs in $PGS_{tgt}$ to conduct encoding. Here, a neighbor of a subgraph is defined as a vertex that is not a vertex in the subgraph but is a 1-hop neighbor (predecessor or successor) of a vertex in the subgraph. The output of NeighborEncode function is determined by both the neighbor and the subgraph. A neighbor might be shared by several subgraphs of the same pattern but it will be encoded once when it is visited for the first time, as indicated by line 16 of Algorithm 2. This constraint can ensure that there will be no overlap among the later extended pattern subgraphs and AutoCellLibX will record the owner subgraph of each neighbor as shown in line 18 of Algorithm 2.

2) Neighbor Encoding with Interconnection Features: The code of a neighbor (neighbor code) consists of its standard cell type, and the labels of edges between the neighbor and the subgraph, as demonstrated in line 3-9 of Algorithm 2. Each edge between the neighbor and the subgraph will be enumerated and a corresponding edge code of the edge will be generated. As mentioned in Section III-A and III-C, each vertex in an existing subgraph of a specific pattern has its index in the subgraph. Accordingly, the edge code includes the index of the vertex in the subgraph and the label of edges. The order of these two parts in the edge code depends on whether the neighbor is the driver of the edge. For example, if the subgraph in the red dash curve is the target subgraph, the edge between OR2X1 cell and NOR3X1 in Fig. 4(a) will be encoded as "(Y,B,3)" while the edge between OR2X1 cell and AND2X2 in Fig. 4(a) will be encoded as "(2,Y,A)". The neighbor code is constructed as the standard cell type of the neighbor vertex followed by the edge codes of edges between the neighbor vertex and the corresponding subgraph, where the edge codes are concatenated in the lexicographical order. For example, as shown in Fig. 4(a) the neighbor code of the OR2X1 cell will be "[OR2X1](2,Y,A)(Y,B,3)" if the subgraph in the red dash curve is the target subgraph for neighbor encoding. Consequently, the recurrence frequencies of the OR2X1 cell (encoded as "[OR2X1](2,Y,A)(Y,B,3)") and OR3X1 cell (encoded as "[OR3X1](Y,A,1)") is 1 and 3 respectively in Fig. 4(c).

Please be aware that some input pins of some standard cells, e.g., the input pin "A" and "B" of OR2X1 cell in Fig. 4(a) have equivalent functionality and highly similar parasitics. Switching the interconnection edges among these pins will not change the logic functionality. For the sake of this factor, during the actual implementation of edge code generation, equivalent pins will be encoded to the same name. For example, pin "B" of OR2X1 will be encoded as "A".

Since the neighbor code encodes all the necessary information of the interconnection between the neighbor and the vertices in the subgraph in a unique form, those neighbors with the same neighbor code have the isomorphic interconnection edges with their corresponding subgraphs. Therefore, the neighbor codes can classify the neighbor vertices into different sets for later pattern growth.

In our proposed solution, the time complexity of neighbor encoding is $O(|E|)$, determined by lines 14-20 of Algorithm 2 where neighbor vertices of the subgraphs are enumerated for encoding.

C. Pattern Growth

In the stage of pattern growth, AutoCellLibX merges some neighbor vertices into the subgraphs of $PGS_{tgt}$ to enlarge the pattern size while trying to preserve the recurrence frequencies of the original pattern to realize a high coverage of the new pattern group.

1) Fundamentals of the Selection of Neighbors: Selecting neighbors for pattern growth is based on two theorems verified in classic subgraph mining solutions [36, 37].

Theorem 1. Given two isomorphic subgraph $G_A(V_A,E_A)$ and $G_B(V_B,E_B)$ of $G$, and they have neighbor vertex $v_a$ and $v_b$ respectively. If $v_a$, and $v_b$ have isomorphic interconnection edge set $E_a$ and $E_b$ connected to $G_A$ and $G_B$ respectively (i.e., $v_a$ and $v_b$ have the same neighbor codes), $G'_A(V'_A,E'_A)$ and $G'_B(V'_B,E'_B)$ are isomorphic, where $V'_A = v_a \cup V_a, V'_B = v_b \cup V_b, E'_A = E_a \cup E_A, E'_B = E_b \cup E_B$.

Theorem 2. (Recurrence Frequency Monotonicity): If a subgraph pattern $G_s$ recurs $R$ times in $G$, then any subgraph of $G_s$ recurs no less than $R$ time in $G$.

Based on Theorem 1 we can merge those neighbor vertices with the same neighbor code, as well as the interconnection edges between them and their own subgraphs, into the owner subgraphs in $PGS_{tgt}$ to obtain a new pattern group $PGS_{new}$, where isomorphic subgraphs get larger compared to those in $PGS_{tgt}$. However, the size of $PGS_{new}$ will not be greater than the size of $PGS_{tgt}$, since some of the subgraphs in $PGS_{tgt}$ do not have a neighbor with the specific neighbor code. This result is supported by Theorem 2.

As the example shown in Fig. 4(c) suppose the subgraphs in the red dash curve are those in $PGS_{tgt}$, the size of which is 5. Only 3 subgraphs have a neighbor OR3X1 cell encoded as "[OR3X1](Y,A,1)" and it means that if we merge these OR3X1 cells into the corresponding subgraphs in $PGS_{tgt}$, we will get a new pattern group $PGS_{new}$, the size of which will be 3.
Algorithm 3: Pattern Growth

Input: \( L_{iter} \) (or \( L_{init} \)), the top-1 pattern group \( PGS_{tgt} \), code2Neighbors, neighbor2Subgraph

Output: updated list of pattern groups \( L'_{iter} \)

1. \( targetCode = \text{getFreqNeighborCode} \) (code2Neighbors);  
2. \( \text{moveNeighbors} = \text{code2Neighbors} [\text{targetCode}] \);  
3. \( PGS_{new} = \{ \} \);  

\* enumerate the neighbors with the target neighbor code  

foreach \( v_i \in \text{targetNeighbors} \) do
  \( \text{ownerSubG} = \text{neighbor2Subgraph}[\text{neighbor}] \);  
  if \( \text{ownerSubG is NOT abandoned} \) then
    /* deal with neighbor occupied by other pattern subgraph */  
    if \( \exists PGS' \in PGS \) then
      \( \text{overlapSubG = getOverlapSubG} \);  
      \( \text{overlapSubG} \) ;  
      \( \text{setIndexInSubG} \);  
      \( \text{newSubG} = \text{ownerSubG} \cup v_i \cup E(v_i, \text{ownerSubG}) \);  
      \( \text{ownerSubG} \) ;  
      \( \text{newSubG} \);  
      \( \text{newSubG} \);  
    end
    \( \text{ownerSubG} \) ;  
    \( \text{newSubG} \);  
    \( \text{newSubG} \);  
  end
  end

\( L'_{supSeed} = \text{patternSeedSupplement} (G) \);  
\( L'_{iter} = \text{sortByCoverage} (L'_{iter} + PGS_{new} + L'_{supSeed}) \);  
\( \text{removeLowCoveragePatternGroups} (L'_{iter}) \);  
\( \text{return} L'_{iter} \)

2) Acquisition of New Pattern Group: To realize high coverage of \( PGS_{new} \), AutoCellLibX will select the neighbor code which has the most recurrences among the subgraphs in \( PGS_{tgts} \), e.g., "[ORX3X1](Y,A,1)" for the subgraphs in Fig. 4[C] and merge the neighbors with the selected neighbor code into their owner subgraphs. When merging a neighbor into a pattern subgraph, the vertex will be assigned an index of the number of vertices of the original subgraph. This index indicates the “position” of the vertex in the pattern subgraph and will be used in neighbor encoding in Section III-B2.

Those extended subgraphs will be removed from \( PGS_{tgts} \) and added to \( PGS_{new} \). Meanwhile, similar to the example in Fig. 4(b) for initial pattern seed generation, if those involved neighbors originally belong to the subgraphs in some pattern groups in \( L_{iter} \) (or \( L_{init} \)), the subgraphs will be abandoned by the corresponding pattern groups and vertices in those subgraphs will be marked as unoccupied to meet the no-overlap constraint. These steps are demonstrated in lines 4-18 of Algorithm 3. In this procedure, AutoCellLibX tries to raise the coverage of \( PGS_{new} \) and shrink the low-coverage pattern groups.

3) Post-process for Later Pattern Mining: Since some subgraphs are eliminated from their pattern groups due to overlaps during pattern growth, some vertices in \( G \) become unoccupied. These vertices will be fed into a function for pattern seed supplement, which will generate the seed patterns with these unoccupied vertices, similar to initial pattern seed generation in Section III-A.

The pattern groups in \( L_{iter} \) will be sorted in descending order of their coverage in \( G \) to maximize area reduction with standard cell customization. Details for the relationship between pattern coverage and area benefit are illustrated in Section III-B1. Meanwhile, pattern groups with coverage lower than 2.5% of the number of vertices in \( G \) will be removed from \( L_{iter} \) to prune unnecessary exploration.

The time complexity of pattern growth is \( O(|V|) \), determined by lines 4-15 of Algorithm 3, where neighbor vertices with the same neighbor code of the subgraphs are enumerated.

D. Generation of SPICE Netlist and GDSII Layout

AutoCellLibX needs to generate SPICE netlists and GDSII layouts for the patterns, so it can evaluate their area benefits.

1) Selection of Patterns for Generation: While there are many pattern groups in \( L_{iter} \) and standard cell layout synthesis is time-consuming, just a few pattern groups should be considered for customization. According to the empirical observation on our benchmarks, the pattern groups outside the top-5 in \( L_{iter} \) cover less than 10% of vertices in \( G \) during the runtime of AutoCellLibX. Therefore, AutoCellLibX will only generate the SPICE netlist and GDSII layout for the top-\( N_p \) pattern groups in \( L_{iter} \) for each mining iteration, where \( N_p \) is the maximum number of custom standard cell types defined in Section III-H.

2) SPICE Netlist Generation: As mentioned in Section III-G, \( G \) is a gate-level netlist after technology mapping, where each vertex is actually a standard cell. In the standard cell library, the SPICE netlist for each cell is provided. For standard cell merging, a pattern subgraph represents a set of interconnected standard cells. Therefore, AutoCellLibX can merge the SPICE netlists of the cells by connecting the pins of sized transistors according to the topology of the subgraph. To make the most of standard cell customization, AutoCellLibX will check all the I/O signals in the pattern subgraph, and if an I/O signal has no connection outside the subgraph in \( G \) and becomes a completely internal signal of the pattern subgraph, the I/O pin for this signal on the SPICE interface of this custom standard cell will be removed. This can lower the pressure of I/O pin placement and provide more flexibility for the other parts of placement and routing during layout synthesis.

3) GDSII Layout Generation: Based on the SPICE netlist and the design rules of the standard cell library (e.g., number of routing tracks), AutoCellLibX will invoke ASTRAN [8] to conduct layout synthesis for a specified pattern subgraph.

E. Pattern Combination Evaluation

After previous stages of the iterative mining loop, at this stage, AutoCellLibX obtains a list of sorted pattern groups which do not overlap with each other and the area benefit of a combination of pattern groups should be evaluated.

1) Reward Function: The overall reward function \( R(C,G) \) indicating how much area could be saved can be formulated as:

\[
R(C,G) = \sum_{PGS \in C} \left[ |PGS| \times F(PatternG_i) \right]
\]

where \( PGS \) are the pattern groups in pattern combination \( C \), \( PatternG_i \) is one of the subgraphs in \( PGS_i \), and \( F \) is a function evaluating the area benefit of the custom standard cell generated according to \( PatternG_i \) compared to the combination of original standard cells.

![Fig. 5. Example of 50 custom standard cells showing the correlation between the pattern size and the area saved with the custom cell for the pattern](image-url)
To find out the factors impacting $F(Pattern_{Gi})$, a series of experiments have been conducted and the empirical results of 50 custom standard cells generated by ASTRAN [6] based on FreePDK45 process [44] are shown in Fig. 5. According to the results, the area benefit of a custom standard cell is nearly proportional to $PatternSize_i$, the number of original standard cells in the pattern subgraph $Pattern_{Gi}$. Therefore, we can get $R_{approx}(C, G)$, an approximation of $R(C, G)$ as follows:

$$R(C, G) \approx K \sum_{PGS_i \in C} |PatternSize_i|$$  (3)

$$= K \sum_{PGS_i \in C} Cov(PGS_i) = R_{approx}(C, G)$$  (4)

where $K$ is a linear approximation factor. Accordingly, for a specific iteration, selecting the top-$N_p$ pattern groups from $L_{iter}$, which is sorted according to pattern coverage (i.e., $R_{approx}(C, G)$), as the pattern combination $C$ to generate custom standard cells is the near-optimal solution from the perspective of area benefit. Such a relationship between pattern coverage and area benefit explains why AutoCellLibX sorts the pattern groups by coverage in Section III-C and III-A.

2) Termination Criteria of Pattern Mining: The area benefit of the top-$N_p$ pattern groups could change as the pattern mining loop iterates. Therefore, AutoCellLibX should stop the loop at a proper iteration to reach the optimal combination of custom standard cells.

According to Theorem 3 (recurrence frequency monotonicity), it can be noticed that the values of $|PatternSize|$ tend to have a descending trend, while the values of $PatternSize_i$ are increasing, during the iterative pattern mining. As indicated in Section I PatternSize, $patternSize_i$ will be limited within $S_p$, so $R(C, G)$ has an upper bound for each benchmark. Moreover, the values of $PatternSize_i$, starting from 1, increase by at most 1 in each iteration while the declines of $|PatternSize|$ are usually greater than 20% in each iteration for the benchmarks in our experiments. It means that when $PatternSize_i$ is greater than 5, it is much harder for the increase of $PatternSize_i$, to compensate for the decline of $|PatternSize|$.

Based on these analyses, AutoCellLibX will terminate the pattern mining loop if $R(C, G)$ declines in the last two iterations since it has little probability to realize higher area benefit if the loop continues.

IV. EXPERIMENTAL RESULTS

In this section, we comprehensively evaluate the performance of AutoCellLibX are presented.

A. Target Process, Benchmarks and Environment

Our evaluation experiments are based on FreePDK45 [44], an open-source generic process design kit developed by Oklahoma State University and North Carolina State University, which uses a predictive 45nm CMOS technology process. Concretely, in the experiments, the benchmarks are synthesized by Yosys [43] based on the FreePDK45 technology library, SPICE netlists of custom standard cells are obtained according to the SPICE netlists of FreePDK45 standard cells, and ASTRAN generates the layout of custom standard cells according to the design rules of FreePDK45.

To comprehensively evaluate AutoCellLibX in different scenarios, we collect 31 open-source benchmarks from various domains, including the EPFL combinational benchmark suite [45], BOOM [46], a high-performance RISC-V CPU design, and Gemmini [47], a systolic array accelerator design for deep learning. For larger designs like BOOM and Gemmini which include multiple submodules with significantly different functionality and logic characteristics, e.g., DCache and ALU in BOOM, it is impractical for AutoCellLibX to find common patterns among these unique submodules. AutoCellLibX provides a hierarchical partitioning tool that can partition the design to a given depth so designers can select some of the partitions and find the custom standard cells for each of them. As mentioned in Section I-A, $N_p$ and $S_p$ are set to be 5 and 10 respectively. Experiments are conducted on Ubuntu 20.04 with Intel i7-9850H CPU (2.60 GHz, 12 logic cores) and 32GB DDR4.

B. Effectiveness of Proposed Pattern Mining Techniques

The experimental results are presented in Table I. The major submodules of BOOM [46] and Gemmini [47] are evaluated individually. The submodules included in the table cover more than 75% logic vertices in the gate-level netlist of BOOM or Gemmini. According to the "Pattern Cov(%)" in Table I a ratio showing how many vertices in the gate-level netlist are covered by the selected regular patterns, the existence of patterns is noticeable for most of the benchmarks since the average pattern coverage of the 31 benchmarks is 25.67%.

1) Area Benefit: The resultant data of area are collected from the post-technology mapping reports before placement and routing. The area reduction ratio indicates how much area is reduced for a corresponding benchmark when pattern subgraphs in its gate-level netlist are replaced by the selected custom standard cells generated by AutoCellLibX. For benchmarks in EPFL benchmark suite [45], submodules of BOOM [46], and submodules of Gemmini [47], their average area reduction ratios are 5.11%, 3.07%, and 4.91% respectively. The average area reduction ratio for all the benchmarks in the table is 4.49%. AutoCellLibX achieves significant area reduction compared to the FreePDK45 library while overlap constraint, pattern

| Benchmark | Original Area(mm$^2$) | Optimized Area(mm$^2$) | Reduce Area(%) | Run Time(s) | FSM Time(s) | Pattern Size | Area Benefit |
|-----------|----------------------|------------------------|----------------|------------|------------|--------------|--------------|
| adder     | 1890                 | 1634                   | 12.31          | 1314       | 0.02       | 45/3/4       | 56.86        |
| priority  | 1111                 | 983                    | 11.33          | 475        | 0.02       | 3/3/4/4      | 39.22        |
| multiplier| 40326                | 35976                  | 10.79          | 1554       | 0.24       | 5/3/4/4/2    | 41.34        |
| sin       | 11283                | 40469                  | 10.19          | 2222       | 0.38       | 2/2/2/2/4    | 45.74        |
| dec       | 630                  | 593                    | 9.58           | 158        | 0.02       | 4/1/1/1/1    | 15.69        |
| voter     | 17303                | 16339                  | 5.43           | 2407       | 0.09       | 2/3/3/3/3    | 35.33        |
| square    | 31115                | 29389                  | 5.55           | 1228       | 0.13       | 3/4/3/4/3    | 26.98        |
| max       | 1298                 | 4099                   | 5.18           | 415        | 0.03       | 2/2/2/4/4    | 42.67        |
| arbiter   | 16990                | 16403                  | 4.35           | 3123       | 0.15       | 7/2/4/4/4    | 15.29        |
| cfe       | 1086                 | 1085                   | 2.87           | 266        | 0.02       | 2/2/2/4/4    | 11.64        |
| sqrt      | 45259                | 43996                  | 2.79           | 3689       | 0.25       | 4/3/4/4/3    | 29.39        |
| intMul    | 730                  | 360                    | 2.49           | 344        | 0.03       | 3/4/3/3/3    | 13.42        |
| router    | 332                  | 325                    | 2.31           | 1031       | 0.01       | 4/4/4/4/4    | 8.7          |
| sin       | 9155                 | 8976                   | 1.95           | 707        | 0.05       | 5/4/4/4/4    | 7.55          |
| memCtrl   | 66114                | 64881                  | 1.86           | 475        | 0.40       | 2/2/2/4/3    | 9.89          |
| memClk    | 1818                 | 1793                   | 1.38           | 105        | 0.01       | 3/2/2/4/3    | 6.59          |
| ctrl      | 195                  | 193                    | 0.79           | 22         | 0.01       | 2/2/2/4/3    | 7.41          |

Average  5.11  1711  0.01  24/2/4/4/4  24.09

BOOM [46]
selection and area reduction are not considered in the previous works [41,42] of pattern mining for VLSI design.

The optimization of area usage is noticeable but the customization benefit varies among benchmarks. Here, we analyze the related factors as follows:

- **Design Hierarchy Depth:** Benchmarks in EPFL benchmark suite [45] can get better results because they are designed specifically for a local circuit function so the patterns can have a higher coverage. In contrast, if AutoCellLibX consumes the entire gate-level netlist of BOOM or Gemini without partitioning, each of the pattern groups will have a coverage lower than 10%, and the resultant area reduction ratio will be lower than 1.5% since some patterns are not shared by different submodules. Even submodules of these designs have multiple hierarchical levels. This indicates that proper partitioning of the input design can help to find out suitable custom standard cells.
- **Pattern Coverage and Pattern Size:** Benchmarks like "ctrl", "i2c", and "Rename" benefit little from standard cell customization, because their netlists mainly consist of random logic so the pattern coverage is low. From another perspective, benchmarks like "mem_ctrl" reach a lower area reduction ratio because the sizes of their high-frequent patterns are too small.

Compared to conventional frequent subgraph mining, for standard cell customization, AutoCellLibX emphasizes the overlaps between pattern subgraphs. For example, 3 of the 5 selected patterns for benchmark "DCache" overlap with each other on 49107 vertices in the gate-level netlist. Direct frequency-driven pattern mining, ignoring the overlaps, will lead to false frequency results while AutoCellLibX analyzes each vertex during neighbor encoding and pattern growth, avoiding overlaps and optimizing area usage.

2) **Algorithm Efficiency:** Considering neighbor encoding and pattern growth, the time complexity of pattern mining is reduced to $O(M(|E| + |V|))$, where $M$ is the maximum number of pattern mining iterations. According to the analysis of the termination criteria of pattern mining illustrated in Section II-E2 for most scenarios, $M$ is less than 10. Therefore, our FSM algorithm is highly efficient, as shown in the "FSM time" in Table I and the time complexity of our FSM algorithm is much lower than the one of the gSpan algorithm [57] utilized in previous works [41,42], which is proportional to the number of subgraphs in the gate-level netlist. However, currently, the timing-consuming layout synthesis, especially the simulated-annaling transistor placer and MILP compactor, takes up more than 95% of the runtime of AutoCellLibX for the benchmarks, although AutoCellLibX has already pruned most of the minor patterns to avoid unnecessary layout generation and reduce the runtime. The average runtime is 1152 seconds for all the benchmarks while the longest runtime is 3869 seconds for benchmark "voter".

3) **Characteristics of Custom Standard Cells:** The "Pattern Size" column of Table I shows the sizes of the selected pattern subgraphs for corresponding benchmarks. The largest pattern is the one with 7 vertices for benchmark "arbiter", as shown in Fig. 6, which it is hard for template-based algorithms [41,42] to detect. Although we set $S_P$ to 10, the pattern mining procedures for all the benchmarks do not hit this bound which is predicted by Section II-E2. Some benchmarks have less than 5 (i.e., $N_P$) custom standard cells since some candidates have been pruned due to low coverage during pattern growth. The patterns of benchmarks are various but some patterns are shared by some of the benchmarks, as shown in Fig. 7 which shows the potential of reusing custom standard cells for different designs, improving productivity of VLSI design flow.

Fig. 6. A large pattern subgraph with 7 standard cells for benchmark “router” and corresponding custom standard cell layout

Fig. 7. Some patterns shared across benchmarks in Table I

C. **Existing Limitations and Future Works**

While AutoCellLibX shows the power of efficient pattern mining for standard cell customization, it has several limitations, which are listed as follows:

- **Currently,** AutoCellLibX cannot finish complete characterization of standard cells, e.g., the extraction of RC parasitics and timing information. While the results of area reduction are promising, the reward function $R(C,G)$ in Section I can be replaced by a function of other factors like delay and power.
- **Standard cell layout synthesis** is the bottleneck of AutoCellLibX runtime. Moreover, the open-source layout generator ASTRAN [8] does not support some of the design rules of high-end sub-10nm technology nodes currently. Furthermore, factors considered in manual designs like pin access, and via number reduction, could be included for practical application.

Since it is our initial attempt to explore the potentials of design-aware pattern mining of VLSI netlist and standard cell customization, these limitations are out of the scope of this proposed work, which presents an interesting and concrete approach to customizing standard cells, and we will consider more factors in our future works.

In the next development stage, AutoCellLibX will include the optimization of routability and timing and layout synthesis framework, to realize the practicality of AutoCellLib for sub-10nm process technology. Currently, we are adapting our algorithms to the technology design rules in ASAP7 [10] and integrating the existing solutions from [12,19] into AutoCellLibX. ESTIMATION model of timing, routability and DRC will be included in further evaluation. Any criticism and suggestions will be appreciated!
V. CONCLUSION

In this paper, we present an automatic standard-cell library extension framework, AutoCellLibX. According to the post-technology mapping gate-level netlist of the design and the initial standard cell library, AutoCellLibX can find a set of standard cell cluster pattern candidates that occur frequently based on our proposed high-efficiency sub-graph mining algorithm for gate-level netlist. Meanwhile, to maximize the area benefit of standard cell customization for the given gate-level netlist, AutoCellLibX includes our proposed pattern combination algorithm which can iteratively find a set of gate-level patterns from numerous candidates as the extension part of the given initial library. AutoCellLibX closes the optimization loop between the analysis of gate-level netlist and standard cell library customization for VLSI design productivity. The experiments with FreePDK45 library and benchmarks from various domains show that AutoCellLibX can generate the library extension with up to 5 custom standard cells in 1184 seconds on average for the benchmarks and the resultant extension of the standard cell library can save design area by 4.49% averagely.

REFERENCES

[1] R. A. da Luz Reis, “Physical Design Optimization, From Past to Future,” in Proceedings of the 2022 ISPD. ACM, Apr. 2022, pp. 145–148.

[2] B. Ren, A. Wang, J. Bakshi, K. Liu, W. Li, and W. Dai, “A domain-specific cell basedasic design methodology for digital signal processing applications,” in Proceedings of DATE, vol. 3. IEEE, 2004, pp. 280–285.

[3] S. Phillips and S. Hauck, “Automatic layout of domain-specific reconfigurable subsystems for system-on-a-chip,” in Proceedings of the 2002 ACM/SIGDA FPGA, 2002, pp. 165–173.

[4] J. Zhang, B. Jiao, Y. Wang, H. Zhu, L. Zhang, and C. Chen, “ALPINE: An Agile Processing-in-Memory Macro Compilation Framework,” in Proceedings of the 2021 on GLSVLSI. ACM, Jun. 2021, pp. 333–338.

[5] D. Motiani, V. Ketheral, and P. Fileggi, “Method for the definition of a library of application-domain-specific logic cells,” Aug. 2024, US Patent 2,008,016,315,1A1.

[6] M. Guruswamy, R. L. Maziasz, D. Dultz, S. Raman, V. Chiluvuri, A. Fernandez, and L. G. Jones, “CELLERY: A Fully Automatic Layout Synthesis System for Standard Cell Libraries,” p. 6, 1997.

[7] R. Karmazin, C. T. O. Otero, and R. Manohar, “cellTK: Automated Layout for Asynchronous Circuits with Nonstandard Cells,” in 2013 IEEE 19th ASYNC. IEEE, May 2013, pp. 58–66.

[8] A. M. Ziesemer and R. A. d. L. Reis, “Simultaneous Two-Dimensional Cell Layout Compaction Using MILP with ASTRAN,” in 2014 ISVLSI. IEEE, Jul. 2014, pp. 350–355.

[9] M. S. Cardoso, G. H. Smaniotto, A. A. O. Bubolz, M. T. Moreira, L. S. da Rosa, and F. D. S. Marques, “Libra: An Automatic Design Methodology for CMOS Complex Gates,” IEEE TCAS-II, vol. 65, no. 10, pp. 1345–1349, Oct. 2018.

[10] X. Xu, N. Shah, A. Evans, S. Sinha, B. Cline, and G. Yeric, “Standard Cell Library Design and Optimization Methodology for ASAP7 PDK,” arXiv:1807.11396 [cs], Jul. 2018, arXiv: 1807.11396.

[11] C. M. d. O. Conceicao and R. A. d. L. Reis, “Transistor Count Reduction by Gate Merging,” IEEE TCAS-I, vol. 66, no. 6, pp. 2175–2187, Jun. 2019.

[12] T.-C. Lee, C.-Y. Yang, and Y.-L. Li, “ITPlace: machine learning-based delay-aware transistor placement for standard cell synthesis,” in Proceedings of the 39th ICCAD. ACM, Nov. 2020, pp. 1–8.

[13] Y.-L. Li, S.-T. Lin, S. Nishizawa, H.-Y. Su, M.-J. Fong, O. Chen, and H. Onodera, “NCTUCell: A DDA-and Delay-Aware Cell Library Generator for FinFET Structure with Implicitly Adjustable Grid Map,” IEEE TCAD, pp. 1–1, 2021.

[14] K. Jo, S. Ahn, J. Do, T. Song, T. Kim, and K. Choi, “Design rule evaluation framework using automatic cell layout generator for design technology co-optimization,” IEEE TVLSI, vol. 27, no. 8, pp. 1933–1946, 2019.

[15] P. Van Cleeft, S. Hougardy, I. Silvanus, and T. Werners, “Boncell: Automatic cell layout in the 7-nm era,” IEEE TCAD, vol. 39, no. 10, pp. 2872–2885, 2019.

[16] C.-K. Cheng, A. B. Kahng, H. Kim, M. Kim, D. Lee, D. Park, and M. Woo, “PROBE2.0: A Systematic Framework for Routability Assessment From Technology to Design in Advanced Nodes,” IEEE TCAD, vol. 41, no. 5, pp. 1495–1508, May 2022.

[17] P. Majumder, B. Kumthekar, N. R. Shah, J. Mowchenko, P. A. Chavda, Y. Kojima, H. Yoshida, and V. Boppanna, “Method of ic design optimization via creation of design-specific cells from post-layer patterns,” May 10 2011, US Patent 7,941,776.

[18] D. Bhattacharya, V. Boppanna, R. Murgai, and R. Roy, “Process for automated generation of design-specific complex functional blocks to improve quality of synthesized digital integrated circuits in cmos using altering process,” Feb. 21 2006, US Patent 7,003,738.

[19] K. Vaidyanathan, L. Liebmann, A. Strojwas, and L. Pileggi, “Sub-20 nm design technology co-optimization for standard cell logic,” in 2014 ICCAD. IEEE, Nov. 2014, pp. 124–131.

[20] H. Ren, M. Fojtik, and B. Khailany, “NCell: Standard Cell Layout in Advanced Technology Nodes with Reinforcement Learning,” Apr. 2021.

[21] J. Chen and W. Zhu, “An analytical placer for vlsi standard cell placement,” IEEE TCAD, vol. 31, no. 8, pp. 1208–1221, 2012.

[22] M. Guruswamy and D. Wong, “Echelon: A multilayer detailed area router,” IEEE TCAD, vol. 15, no. 9, pp. 1126–1136, 1996.

[23] S. Shah, “Squizzle: A graph based one-dimensional compactor,” Ph.D. dissertation, University of Texas at Austin, 1991.

[24] W. Ye, B. Yu, D. Z. Pan, Y.-C. Ban, and L. Liebmann, “Standard cell layout regularity and pin access optimization considering middle-of-line,” in Proceedings of the 25th edition on GLSVLSI, 2015, pp. 289–294.

[25] X. Yu, B. Yu, J.-R. Gao, C.-L. Hsu, and D. Z. Pan, “Parr: Pin-access planning and regular routing for self-aligned double patterning,” ACM TODAES, vol. 21, no. 3, pp. 1–21, 2016.

[26] T.-C. Yu, S.-Y. Fang, H.-S. Chiu, K.-S. Hu, P. H.-Y. Tai, C. C.-F. Shen, and H. Sheng, “Pin accessibility prediction and optimization with deep-learning-based pin pattern recognition,” IEEE TCAD, vol. 40, no. 11, pp. 2345–2356, 2020.

[27] K. Baek and T. Kim, “Simultaneous transistor folding and placement in standard cell layout synthesis,” in 2021 IEEE/ACM ICCAD. IEEE, 2021, pp. 1–8.

[28] S. Ward, D. Ding, and D. Z. Pan, “Pade: A high-performance placer with automatic datapath extraction and evaluation through high-dimensional data learning,” in DAC 2012. IEEE, 2012, pp. 756–761.

[29] H. Xiang, M. Cho, H. Ren, M. Ziegler, and R. Puri, “Network flow based datapath bit slicing,” in Proceedings of the 2013 ACM ISPD, 2013, pp. 139–146.

[30] C.-C. Huang, B.-Q. Lin, H.-Y. Lee, Y.-W. Chang, K.-S. Wu, and J.-Z. Yang, “Graph-based logic bit slicing for datapath-aware placement,” in 2017 54th DAC. IEEE, 2017, pp. 1–6.

[31] Y. Wang, D. Yeo, and H. Shin, “Effective datapath logic extraction techniques using connection vectors,” IET Circuits, Devices & Systems, vol. 13, no. 6, pp. 741–747, 2019.

[32] D. Fang, B. Zhang, H. Hu, W. Li, B. Yuan, and J. Hu, “Global placement exploiting soft 2d regularity,” in Proceedings of the 2022 ISPD, 2022, pp. 203–210.

[33] A. Inokuchi, T. Washio, and H. Motoda, “An apriori-based algorithm for frequent substructures from graph data,” in European conference on principles of data mining and knowledge discovery. Springer, 2000, pp. 13–23.

[34] X. Yan and J. Han, “gspan: Graph-based substructure pattern mining,” in 2002 ICDM. IEEE, 2002, pp. 721–724.

[35] J. Huan, W. Wang, and J. Prins, “Efficient mining of frequent subgraphs in the presence of isomorphism,” in 3rd ICDM. IEEE, 2003, pp. 549–552.

[36] M. Eiseley, E. Abdelhamid, S. Skiadopoulos, and P. Kalnis, “Gram: Frequent subgraph and pattern mining in a single large graph,” Proceedings of the VLDB Endowment, vol. 7, no. 7, pp. 517–528, 2014.
[40] T. Ramraj and R. Prabhakar, “Frequent subgraph mining algorithms— a survey,” Procedia Computer Science, vol. 47, pp. 197–204, 2015.
[41] B. S. Kim, H. S. Won, T. Han, and J.-S. Yang, “Afsem: Advanced frequent subcircuit extraction method by graph mining approach for optimized cell library developments,” in 2016 IEEE ISCAS. IEEE, 2016, pp. 662–665.
[42] B. S. Kim, T. H. Han, J.-S. Yang, and J. Chung, “New library development method by fsm based cell pattern extraction,” IEICE Electronics Express, vol. 15, no. 9, pp. 20171226–20171226, 2018.
[43] C. Wolf, J. Glaser, and J. Kepler, “Yosys—a free verilog synthesis suite,” in Proceedings of the 21st Austrian Workshop on Microelectronics, 2013.
[44] J. E. Stine, I. Castellanos, M. Wood, J. Henson, F. Love, W. R. Davis, P. D. Franzon, M. Bucher, S. Basavarajaiah, J. Oh et al., “Freepdk: An open-source variation-aware design kit,” in 2007 IEEE International Conference on Microelectronic Systems Education (MSE’07). IEEE, 2007, pp. 173–174.
[45] L. Amarî, P.-E. Gaillardon, and G. De Micheli, “The epfl combinational benchmark suite,” in Proceedings of the 24th IWLS, no. CONF, 2015.
[46] J. Zhao, B. Korpan, A. Gonzalez, and K. Asanovic, “Sonicboom: The 3rd generation berkeley out-of-order machine,” in Fourth Workshop on Computer Architecture Research with RISC-V, vol. 5, 2020.
[47] H. Genc, S. Kim, A. Amid, A. Haj-Ali, V. Iyer, P. Prakash, J. Zhao, D. Grubb, H. Liew, H. Mao et al., “Gemmini: Enabling systematic deep-learning architecture evaluation via full-stack integration,” in 2021 58th DAC. IEEE, 2021, pp. 769–774.