Optimization of Ballistic Deflection Transistors by Monte Carlo Simulations

J-F Millithaler\textsuperscript{1}, Iñiguez-de-la-Torre\textsuperscript{2}, J Mateos\textsuperscript{2}, T González\textsuperscript{2}, M Margala\textsuperscript{1}

\textsuperscript{1}Department of Electrical and Computer Engineering, University of Massachusetts, Lowell, MA 01854, USA
\textsuperscript{2}Applied Physics Department, Salamanca University, Salamanca 37008, Spain

E-mail: jeanfrancois_millithaler@uml.edu

Abstract. This paper presents an optimization of the current-voltage characteristic of Ballistic Deflection Transistors. The implementation of an adequate surface charge model in a Monte Carlo tool shows a very good agreement with the available experimental data and allows us to predict the influence of different parameters, like temperature, channel and trench dimensions on the device output. These results are of importance for further use of this device in logical circuit applications.

1. Introduction

The Ballistic Deflection Transistor (BDT) \cite{1} is a kind of semiconductor device that can drastically change the way to develop the electronics of tomorrow. This device associate the ballistic motion of electrons \cite{2}, offering very high speed performances, with a strategic geometry design allowing the steering of electrons, granting the opportunity to realize a complete logic gate \cite{3-5}. The two symmetrical outputs can exhibit at the same time and for a given set of polarizations, one maximum of current and one minimum. In term of logical terms, this can be translated as logic high, or “1”, and logic low, or “0”, respectively. The purpose of this paper is to investigate major parameter dependencies in order to control the nonlinear behaviour of the BDT and provide the most useful output characteristic for logical applications.

2. Overview of the BDT and Monte Carlo Model

The BDT is an interesting device based on an InAlAs/InGaAs heterojunction, where a two-dimensional electron gas (2DEG) allows carriers to travel more than 2.5 times faster than in silicon. By using electron-beam lithography \cite{6}, the shape of the device can reach smaller dimensions than the electron mean free path (about 140 nm in InGaAs channel at 300 K) and provide ballistic transport at room temperature. The design of the BDT is presented in Fig. 1. It includes a grounded source, three drains (\(V_{TD}\), \(V_{LD}\) and \(V_{RD}\)), where top drain is just a pull-up terminal, and two lateral gates biased in push-pull mode (\(V_{LG}=V_{RG}\)). A negative bias applied on one gate will pinch off the corresponding drain channel. This will produce a steering effect, assisted by a triangular deflector, and the device will provide a nonlinear output characteristic \cite{6, 7}. Fig. 2 shows a scanning electron microscope (SEM) image of a 300 nm wide channel BDT \cite{6}. The simulated BDT has been directly designed over the SEM image, keeping all dimensions identical. Access regions have been removed for reducing the computation times and only the active region is simulated.
The modelling tool is an ensemble MC simulator of the electron dynamics self-consistently coupled with a 2D Poisson solver using the finite differences approach [8]. A background doping $N_{db}=5\times10^{16} \text{cm}^{-3}$ is considered, the size of meshes is $5\times5 \text{nm}$ and the time step is 1 fs. As devices are reaching nanometre size, the surface-volume ratio increase drastically and the effect of surface charges (at the interface semiconductor-dielectric), which led to a depletion mechanism in the channel, becomes crucial. The simulator can take care of these surface charges in two ways. The first way, so-called constant charge model (CCM), assume that all surface charges are bias and geometry independent. The value of $\sigma$ in the MC code is a fitting parameter but adjusted via experimental measurements [9, 10]. The second way proposed is to set the surface charge value adaptive with the surrounding carrier concentration. The so-called self-consistent charge model (SCCM) allows the variation $\sigma$ with the bias and position, increasing or decreasing its magnitude according the local electron density. More details about this model can be found in [11, 12].

3. Results

3.1 Effect of Surface Charges

Fig. 3(a) presents the comparison of the experimental right drain current (left drain current is symmetric with respect to zero and is not traced for more clarity) vs. the left gate voltage [1] and the MC results obtained with the two presented models. The CCM is able to reproduce the experimental current in the vicinity of zero gate bias ($V_{LG}=V_{BG}=0.0 \text{V}$) but clearly fails when the current should abruptly decrease for highly negative $V_{LG}$. On the other hand, the SCCM shows a remarkably good agreement with the measurements. The magnitude of the current and the sharp drop at both sides of the maximum are correctly reproduced. To help the reader to clarify the difference between the two

![Figure 1: 3D topology of a typical BDT](image1)

![Figure 2: SEM image of BDT and sketch of simulated device. All dimensions are in mm.](image2)
models we are showing the 2D electron density map of the whole device in Fig. 3(b), for \( V_{LG} = -4 \) V, where the largest differences between the two models are found. Within the CCM the fixed value of the surface charge (\( \sigma = 3.10^{15} \) m\(^{-2}\)) is not enough to completely deplete the source channel. Also, the electron concentration in the right drain channel is highly overestimated and as a consequence also the current. On the other case, the surface charges within the SCCM react to the rise in the amount of electrons in their vicinity, thus increasing in order to maintain a depletion region near the interfaces. The measured current decrease is then correctly reproduced.

3.2 Scaling down and temperature optimization

As the SCCM is the best model to correctly simulate the complex behaviour of the BDT, it is the one that will be used in the following. Fig. 4 shows the right drain current of the previously presented 300 nm wide channel BDT at room temperature and at 77 K. We observe, as expected, an increase of the maximum current from 16 \( \mu \)A up to 26 \( \mu \)A when T is decreased. Nevertheless, the bell-shape of the current is widened and the pinch-off is achieved for a higher value of the bias. Fig. 4 also shows the results for a smaller device, with the channel width as small as 100 nm. All the other dimensions have been scaled down proportionally and drain biases have been kept identical. The main result is that we can appreciate a sharper bell-shape of this current almost pinching-off the channel at -1.0 V. Therefore we demonstrate that scaling down the BDT will provide a much better gate control and an enhancement of the nonlinear output, making it suitable also for analog applications such as frequency doubling. Low temperature operation is also interesting, because for \( W_C = 100 \) nm the maximum current increases a \( \times 3 \) factor whereas it was only \( \times 2 \) in the case of \( W_C = 300 \) nm. Ballistic carriers are only affected by design device boundary thus low temperature shouldn’t modify the output current. This means that even for the smallest device studied, the transport is not completely ballistic at room temperature, and a further downscaling is still necessary for reaching its optimum operation conditions.

3.3 Trenches optimization

Controlling the trenches’ width, \( W_t \), is one of the biggest challenge in the BDT fabrication process because they are the key to provide the best performance of the device. In Fig. 5(a) we report the effect of \( W_t \) on the BDT’s characteristics. Decreasing the width of the BDT trenches to 40 nm (the reference device, Fig. 2, has \( W_t = 80 \) nm) narrows the bell-shape current, while increasing it to 120 nm has the opposite effect, as expected. However, the maximum current remains the same. On Fig. 6(a), the results for the smaller device, where \( W_C = 100 \) nm, are plotted. As all dimensions have been scaled down proportionally, the reference \( W_t \) is now equal to 27 nm. Interestingly the variation of \( W_t \) has now more influence on the current peak magnitude but less on the pinch-off behaviour. The fabrication of a very small trench width might be a challenge, so that its filling with a high-k dielectric may provide a simpler solution and even enhanced performances. Up to now the air is used as dielectric, with \( \varepsilon = 1 \) (obtained by simply digging the trenches onto the heterostructure). In the MC simulations the value of the permittivity must be modified in order to correctly capture the gate-to-channel coupling of the electric field through the semiconductor buffer. An intermediate value \( \varepsilon = 10 \) (between the air, \( \varepsilon = 1 \), and the semiconductor, \( \varepsilon = 13.88 \)), provides the best fit [see Fig. 3(a)]. Figs. 5(b) and 6(b) show the output response when using \( \varepsilon = 25 \) (corresponding to the case where trenches are filled with promising
high-k dielectrics like ZrO$_2$ or HfO$_2$ [13]) and $\varepsilon=70$ (approaching the value of deionized water). In both cases, $W_C=300$ and 100 nm, the higher the value of the dielectric the stronger the gate control and the easier is to pinch-off the channel. Again, the effect is more pronounced in the smaller device, decreasing also the value of the current peak.

Figure 5: Output current for different $W_t$ and $\varepsilon$, in the case $W_C=300$ nm

Figure 6: Output current for different $W_t$ and $\varepsilon$, in the case $W_C=100$ nm

4. Conclusion

The use of a self-consistent surface charge model in our MC simulator has shown that the complex nonlinear behaviour of the BDT can be correctly simulated. The modelling of a real BDT provides very good qualitative and quantitative results and makes possible the optimization of the device. The effect of scaling down the channel and trench width and the permittivity of the dielectric filling the trenches have been studied and have shown that a better gate control can be reached. These results will be of importance for the possible use of BDTs in circuits for analog or logical applications.

5. References
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