An Efficient Topology-Based Algorithm for Transient Analysis of Power Grid

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Abstract—In the design flow of integrated circuits, chip-level verification is an important step that sanity checks the performance as expected. Power grid verification is one of the most expensive and time-consuming steps of chip-level verification, due to its extremely large size. Efficient power grid analysis technology is highly demanded as it saves computing resources and enables faster iteration. In this paper, a topology-base power grid transient analysis algorithm is proposed. Nodal analysis is adopted to analyze the topology which is mathematically equivalent to iteratively solving a positive semi-definite linear equation. The convergence of the method is proved.

Index Terms—Power grid, topology, nodal analysis, positive semi-definite

I. INTRODUCTION

Power grid analysis is an indispensable step in modern chip simulation and verification. Due to the IR and Ldi/dt voltage drops, the actual voltages applied to the logic gates and other circuit elements are smaller than wished, which not only increases the delay of the logic gates but may also result in logic errors. As the ever decreasing supply voltages and threshold voltages make the problem worse, power grid analysis becomes an indispensable step in the simulation flow.

To capture the worst-case voltage drop and place decoupling capacitors (if necessary), DC analysis and/or transient analysis of the power grid should be performed. Frequency-domain analysis is not appropriate as the vital voltage drop in the time domain may be lost in the frequency-domain analysis. Both DC analysis and transient analysis (using forward/backward can be finally reduced to a linear solving problem

Traditional power grid analysis only considers the IR voltage drop. As the operation frequency of chips is increasing rapidly, the Ldi/dt voltage drop should not be neglected. Thus, the power grid model should consist inductors besides resistors and capacitors. The existence of inductors changes the state-space model from order-1 to order-2, hence introduces new difficulties to the transient analysis and its topology-based algorithms. It was proved in [1] that the system matrix of the RLC model could be still positive definite, which had been thought to be impossible before the paper. However, some of its details are inaccurate. The right formulation will be proposed in Section IV-D which is the basis to prove the convergence of the topology-based iterative algorithm in Section IV-A

In this paper, a new topology-based algorithm is proposed. The Nodal analysis is adopted to analyze the netlist and generate positive semi-definite system model. Then a purely topology-base iterative method is introduced to solve the power grid analysis without constructing the system matrices. The convergence is proved and the complexity is analyzed.

II. BACKGROUND

A. Problem formulation

Power grids are usually modeled as RLC circuits, or simpler RC circuits. The current sources attached to the nodes of the power grid represent the currents drawn from the logic gates or other devices. Hence prior to the simulation of the power grid, the current pattern of the gates and devices should be obtained and modeled as piecewise linear ideal current sources. The capacitors in parallel with the currents sources can be either parasitic capacitors or decoupling capacitors. The inductors most possibly appear at the vias connecting different layers and the metal layer connecting the power grid to external power supply. In many models the inductors can be neglected.

First consider the simpler RC power grid model, which can be depicted as a state-space model [2]–[5]

\[
C \frac{d}{dt} v(t) + G v(t) = -i(t) + G_0 V_{dd}, \tag{1}
\]

where \(v(t)\) is the vector of nodal voltages, \(i(t)\) is the vector of current sources, \(V_{dd}\) is vector of dimension \(n\) with all its values equal to \(V_{dd}\). \(C\) is a diagonal matrix whose \((i, i)\) element is the capacitance between node \(i\) and ground. \(G\) is the conductance matrix with its diagonal \((i, i)\) element being the total conductance connected to node \(i\) and off-diagonal \((i, j)\) element being the opposite number of the conductance between node \(i\) and node \(j\) (it is zero if node \(i\) and node \(j\) are unconnected). \(G_0\) is a diagonal matrix with its \((i, i)\) element being the conductance between node \(i\) and source (if node \(i\) is connected to a source) or 0 (if node \(i\) is not connected to any source). To simplify the notation, \(b(t)\) is used to represent \(-i(t) + G_0 V_{dd}\). Using backward Euler method, (1) can be approximated as

\[
(\frac{C}{h} + G)x(t + h) = \frac{C}{h} x(t) + b(t + h), \tag{2}
\]

where \(h\) represents the time step. Thus given the initial condition \(x(0)\), we can calculate all the \(x(t)\) after 0. Note that \(\frac{C}{h} + G\) is always invertible if the system is stable. The reason is that stability implies that all the eigenvalues of the matrix pencil \((G, C)\) distribute in the left half complex plane and the positive real value \(\frac{1}{h}\) cannot be an eigenvalue of \((G, C)\).
If we use system matrix $A$ to denote $\frac{C}{h} + G$ and $b$ to denote $\frac{C}{h}x(t) + b(t + h)$, (2) can be reduced to

$$Ax = b.$$  

(3)

In DC analysis, $A = G$ and $b$.

**B. SOR-like iterative method**

Although straightforward in theory, Eq. (2) are difficult to solve due to the extremely large size. In a standard power grid analysis problem, the number of nodes $n$ can be hundreds of thousands or even millions, thus the dimension of the matrices can be up to millions. This causes problems owing to the limited speed and memory of computers. Direct methods based on LU decomposition requires $O(n^3)$ time for the decomposition of the system matrix ($G$ or $A$) and $O(n^2)$ time for forward and backward substitution. The memory required is $O(n^2)$ even if $G$ or $A$ is sparse as the resulting matrices $L, U$ may become dense. Therefore direct methods are not applicable for extremely large problems.

Alternative methods include traditional iterative methods, the widely used PCG (preconditioned conjugate gradient) method and the Monte-Carlo-like random walk method, etc. PCG method, although converges fast, may be not applicable to extremely large problems as preconditioned system matrix may become dense and thus requires prohibiting $O(n^2)$ memory. Random walk algorithm is most suitable in the case that we only want to calculate the voltages at some specific nodes, but it may be inefficient for the full-circuit analysis, which is indispensable to find the worst-case voltage drop.

An iterative method was introduced in [6], which can be regarded as an efficient implementation of the traditional Gauss-Seidel iteration method and SOR (Successive Over-Relaxation) method. The convergence of this method in the DC analysis has been proven in [6]. The advantage of this method is that it is topology-based and no matrix construction is needed. Hence it requires much less memory than PCG method. It is also shown that the method is faster than random walk in [6].

In the next sections, we will extend this SOR-like method to the transient analysis of RC and RLC power grid models and prove their convergence. In the RLC model analysis part, we will first show that the proof of positive definiteness in [1] is inaccurate and then give the right version.

**III. NODAL ANALYSIS OF RLC CIRCUITS**

In the analysis of RLC circuits the most commonly used method is MNA (modified nodal analysis). It can be guaranteed that these system models are passive [7], [8]. By introducing extra variables for currents flowing through voltage sources and inductors, it can generate compact state-space models efficiently. However, when we perform transient analysis on such MNA models, the system matrix is not positive definite. As a result, many iterative algorithms (such as preconditioned conjugate gradient) cannot be applied since their convergence requires positive definiteness of the system matrix.

In [11], a new NA (nodal analysis) method was proposed to perform transient analysis on RLC circuits. It was proved in [1] that the resulting system matrix is guaranteed to be positive definite. Although the idea in the paper is novel and inspiring, its formulations is inaccurate. The key equation (equation (8) in [1]) is incorrect due to a wrong sign in equation (6). From another perspective, in equation (8), the current state of the nodal voltages only depends on the state of the previous step, which is impossible for a second-order system. In a second-order system like RLC circuits, the required initial conditions involve both $x(0)$ and $x'(0)$. In the discretized form, the state $x(t + \Delta t)$ should depend on both $x(t)$ and $x(t - \Delta t)$, which is not the case in [11]. Besides, the analysis in [11] did not consider voltage sources. Although Norton equivalent was used to convert voltage sources to current sources, we still wish to involve voltage sources from the beginning of the deduction, as Norton equivalent does not work for ideal voltage sources which we may want to include in the power grid model. We will give the correct deduction considering ideal voltage sources in the next subsection.

**A. System equation**

To simplify the deduction, assume that all the negative terminals of the voltage sources are connected to ground, which is just the case in the power grid analysis (it can be extended to ground network analysis straightforwardly). Assume that there are $n$ nodes that are neither ground nor positive terminals of voltage sources in the power grid model (called trivial nodes), numbered from 1 to $n$, together with $p$ nodes being the positive terminals of voltage sources (called source nodes), numbered from 1 to $p$. Besides, assume there are $m$ branches not through voltage sources, numbered from 1 to $m$. Define the $m$ by $n$ modified incidence matrix $A$ as

$$A(i, j) = \begin{cases} +1, & \text{if trivial node } j \text{ is the source of branch } i; \\ -1, & \text{if trivial node } j \text{ is the sink of branch } i; \\ 0, & \text{otherwise}. \end{cases}$$  

(4)

Similarly, define the $m$ by $p$ source incidence matrix $A_s$ as

$$A_s(i, j) = \begin{cases} +1, & \text{if source node } j \text{ is the source of branch } i; \\ -1, & \text{if source node } j \text{ is the sink of branch } i; \\ 0, & \text{otherwise}. \end{cases}$$  

(5)

The advantage of splitting the traditional incidence matrix to the modified incidence matrix and the source incidence matrix is that no extra current variables through the voltage sources needs to be introduced, which facilitates the nodal analysis and is the basis of the positive definiteness to be proved next. By grouping the branches with resistors, inductors, capacitors and current sources together we obtain

$$A = \begin{bmatrix} A_g & A_s \\ A_c & A_{is} \\ A_l & A_{ls} \end{bmatrix}, A_s = \begin{bmatrix} A_{gs} \\ A_{cs} \\ A_{ls} \end{bmatrix}, v_b = \begin{bmatrix} v_g \\ v_c \\ v_l \end{bmatrix}, i_b = \begin{bmatrix} i_g \\ i_c \\ i_l \end{bmatrix}.$$  

(6)

where $i_b$ is the vector of branch currents, $v_b$ is the vector of branch voltages, $g, c, l, s$ represent resistors, capacitors, inductors and current sources respectively.
Applying Kirchoff’s current and voltage laws, we obtain
\[ A^T i_b = 0, \]
\[ Av_n = v_b - A_s v_d, \]  
where \( v_n \) is the vector of nodal voltages (other than the nodes being the terminals of voltage sources) and \( v_i \) is the (constant) vector of voltage sources.

Besides, the branch currents and branch voltages follow the following branch equations (grouped by branch elements)
\[ i_g = G v_g, \]
\[ i_c = C \frac{d v_c}{d t}, \]
\[ v_l = L \frac{d i_l}{d t}, \]
\[ i_s = I_s, \]  
where \( G, C, L \) are diagonal matrices with their diagonal elements being the value of corresponding branch resistance, capacitance and inductance, \( I_s \) is the vector of branch current sources.

Combine (4) and (8), we obtain \( 2m + n \) equations of \( 2m + n \) variables. Substitute the second equation of (7) to (8) and then substitute the second equation of (10) to it we obtain
\[ C \frac{d v_n}{d t} + G v_n + A^T_i i_i + A^T_s I_s - G_s v_d = 0, \]
\[ L \frac{d i_l}{d t} - A_l v_n + A_i v_d = 0. \]  
Here \( G = A^T_g G_A g, C = A^T g C A_c, G_s = A^T_g G_A g_s. \) Use backward Euler law to discretize (9).

\[ C \frac{v_n(t + h) - v_n(t)}{h} + G v_n(t + h) + A^T_i i_i(t + h) \]
\[ + A^T_s I_s(t + h) - G_s v_d = 0, \]
\[ L \frac{i_l(t + h) - i_l(t)}{h} - A_l v_n(t + h) + A_i v_d = 0. \]  
Here \( h \) is the selected time step length. Rewrite the first equation of (10) at time \( t \) and subtract it from the original equation, then substitute the second equation of (10) to it we obtain
\[ \left( \frac{C}{h} + G + h L \right) v_n(t + h) = \left( \frac{2C}{h} + G \right) v_n(t) - \frac{C}{h} v_n(t - h) \]
\[ + h L v_d - A^T_i I_s(t + h) - I_s(t). \]  
Here \( L = A^T L^{-1} A_l, L_s = A_l L^{-1} A_l g. \) \( L \) is a diagonal matrix with all its diagonal elements being nonzero, hence it is invertible. \( \left( \frac{C}{h} + G + h L \right) \) is called system matrix.

**B. Positive definiteness**

In the RLC power grid model analysis, some assumptions on the topology are made as summarized below:

1) All the voltage sources have their negative terminals as ground;
2) Any trivial node is connected to other non-ground nodes by one or more branches and such branches can not be all current sources.

3) For any pair of trivial nodes \( i \) and \( j \), there exists at least one path from \( i \) to \( j \) and the path passes through trivial nodes only (it does not pass through source nodes).

The first assumption is straightforward and just the case in power grid models. The second assumption is also true since any trivial node in the power grid model is connected to other non-ground nodes by at least one resistor (or capacitor, or inductor). The third assumption may be not satisfied for some special cases. However, in these cases the power grid can be separated to several sub-circuits which are independent of each other. Consider the case in Fig. (1). The circuit can be divided to two independent parts, sub-circuit 1 and sub-circuit 2. In the analysis of each sub-circuit, the third assumption is satisfied.

**Lemma 3.1:** Under the topological assumptions for the circuits, the resulting system matrix \( M = \left( \frac{C}{h} + G + h L \right) \) is positive definite.

**Proof:** It is obvious that \( M \) is symmetric. And according to the definition of \( A_g \), \( G(i, i) \) is the sum of conductances connected to trivial node \( i \), \( \sum_{j \neq i} |G(i, j)| \) is the sum of conductances connected to trivial node \( i \) and not connected to source nodes. Hence \( |G(i, i)| \geq \sum_{j \neq i} |G(i, j)| \). The same is true for \( C \) and \( L \), which indicates the system matrix is weakly diagonally dominant with nonnegative diagonal elements.

Besides, according to the topological assumption, any two trivial nodes are connected by a path crossing only trivial nodes. This results in the system matrix to be irreducible. Use the well-known theorem in [9], we conclude that the system matrix \( M \) is positive definite.

**IV. TOPOLOGY-BASED TRANSIENT ANALYSIS OF POWER GRID**

**A. Voltage Update**

Consider a representative node in the RLC power grid model, as shown in Fig. 2. Applying Kirchoff’s current law at node \( i \) we have
\[ \sum_{j \in N^R_i} g_{ij} (V_i - V_j) + \sum_{j \in N^L_i} I_{ij} + I_i + C_i \frac{d V_i}{d t} = 0. \]  
Here \( I_{ij} \) is the current from node \( i \) to node \( j \), \( g_{ij} \) is the conductance between node \( i \) and node \( j \), \( N^R_i \) (\( N^L_i \)) is the set of
B. Initial conditions

As it can be seen from (11) and (16), the nodal voltages at $t+h$ depend on the circuit states at both $t$ and $t-h$, which is the requirement of the “second-order” characteristic of the circuit. If the initial conditions $v_n(0)$ and $i_l(0)$ are given, we can calculate $v_n(t)$ at any time after 0 by iteratively updating nodal voltages using (16). Given the initial conditions $v_n(0)$ and $i_l(0)$, $v_n(0)$ and $v_n(h)$ can be calculated in three steps.

1) Treat capacitors as voltage sources whose voltages are $v_n(0)$, inductors as current sources whose currents are $i_l(0)$. Perform iterative DC analysis as (6) at time 0, obtain $v_n(0)$, $i_l(0)$ and $v_n(h)$;
2) Calculate $v_n(h)$ and $i_l(h)$ according to $L\frac{v_n(h)-v_n(0)}{h}=i_l(0)$, $L\frac{v_n(h)}{h}=i_l(0)$;
3) Perform iterative DC analysis at time point $h$ and obtain $v_n(h)$.

After the three steps we obtain the voltages of trivial nodes $(v_n(0)$ and $v_n(h))$, which are the basis of the topology-based transient analysis algorithm in the next subsection.

C. Algorithm Description

The topology-based algorithm is proposed as Algorithm [IV-C]. No matrix construction or manipulation is required in the algorithm, which dramatically reduces the storage memory and computation time. In the algorithm, DC analysis is performed first to obtain the initial conditions. Then, the nodal voltages at each time step is solved iteratively, based on the information at the previous two time steps. The vectors $V(s)$ and $I(s)$ represent the nodal voltages and current sources at time $s \times h$. The convergence and computational complexity of the proposed algorithm are discussed in Section [IV-D].

Algorithm 1: Topology-based transient analysis of power grid

Input: Initial capacitor voltages $v_c(0)$, inductor currents $i_l(0)$, step length $h$, maximum step $s_{total}$, current sources $I(s)$ ($s=0,1,...,s_{total}$), error tolerance $tol$;
Output: Nodal voltages $V(s)$ ($s=0,1,...,s_{total}$);
1: Calculate $V(0)$ and $V(1)$ using iterative DC analysis;
2: for $s=2,...,s_{total}$ do
3: $V^{(0)}(s) = V(s-1)$;
4: $k = 0$;
5: repeat
6: $k = k + 1$;
7: Update $V_i^{(k)}(s)$ using equation (16);
8: until $\|V_i^{(k)}(s) - V_i^{(k-1)}(s)\| < tol$
9: $V(s) = V^{(k)}(s)$;
10: end for

D. Convergence

Theorem 4.1: The solution $V(s)$ ($s=0,1,...,s_{total}$) of Algorithm [IV-C] converges to the accurate nodal voltages $v_n(s \times h)$.

Proof: Compare (15) and (16) with (11), we can see that Algorithm [IV-C] is equivalent to the Gauss-Seidel iterative solution of the matrix equation (11). Because the system matrix is symmetric positive definite, the Gauss-Seidel iteration converges (refer to Theorem 10.2.1 of [10]). Therefore Algorithm [IV-C] is guaranteed to converge.

We can employ the SOR (successive over-relaxation) method to accelerate the convergence of Algorithm [IV-C]. Using the SOR-like method, the nodal voltage updating formula (16) is adapted to

\[ V_i^{(k)}(t+h) = \omega \tilde{V}_i^{(k)}(t+h) + (1 - \omega) V_i^{(k-1)}(t+h). \]  \hspace{1cm} (17)

Here $\tilde{V}_i^{(k)}(t+h)$ is the updated voltage calculated through (16). $\omega$ is called relaxation parameter. Using (17) to update the nodal voltage, we obtain a new algorithm (named as Algorithm...
\[
\left( \sum_{j \in N_{R}} g_{ij} + h \sum_{j \in N_{L}} \frac{1}{L_{ij}} + \frac{C_{i}}{h} \right) V_{i}(t+h) = \sum_{j \in N_{R}} g_{ij} V_{j}(t+h) + \sum_{j \in N_{L}} \frac{h}{L_{ij}} V_{j}(t+h) + \left( \frac{2C_{i}}{h} + \sum_{j \in N_{R}} g_{ij} \right) \frac{V_{i}(t)-\sum_{j \in N_{R}} g_{ij} V_{j}(t)-I_{i}(t+h)+I_{i}(t)-\frac{C_{i}}{h} V_{i}(t-h)}{h}. \tag{14}
\]

2. If \(0 < \omega < 2\), Algorithm 2 is guaranteed to converge. With appropriately chosen \(\omega\), the convergence procedure can be accelerated. We refer the readers to [11], [12] for the optimal choice of \(\omega\).

V. Conclusion

A topology-base power grid transient analysis algorithm has been proposed. Nodal analysis has been adopted to analyze the topology which is mathematically equivalent to iteratively solving a positive semi-definite linear equation. The convergence of the method has been proved.

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