The design of 1553b relay circuit based on FPGA

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Abstract: On the basis of increasing the transmission distance of the 1553B bus, in order to maintain the simplicity and stability of the bus and improve its anti-jamming ability, the 1553B signal relay circuit based on FPGA is designed in this paper. The signal transmission part consists of the software and the hardware, and the chip of ZYNQ series is used in the FPGA. Firstly, the transmitted signal oscillation is transformed into a group of positive and negative differential signals, which are realized by transformer (pmdb25). Secondly, the signal is sent to the main control chip of ZYNQ series through signal acquisition chip and level conversion chip. Finally, the data is processed by software program and forwarded to the receiver. The specific experiments have been done on the 1553B signal transmission platform, which significantly show that the proposed scheme is reasonable and reliable.

1. Introduction
Since the U.S. military standard mil-std-1553b bus was released in 1973, it has been rapidly applied to the air force, in a variety of aircraft such as f-16, f-18, b-1 and av-sb. Before the 1960s, there was no standard universal data channel for onboard electronic systems, and connections between various electronic equipment units often required a large number of cables. As airborne electronic systems become more sophisticated, the cables used for such communications will take up a lot of space and weight, and the definition and testing of transmission lines will be more complex and expensive. In order to solve this problem, the SAE A2K committee, supported by the military and industry, decided in 1968 to develop standard signal multiplexing system, and published mil-std-1553 standard in 1973[1-2]. The 1553B multiplexing data bus of 1973 became the technology to be adopted by future military aircraft. It replaced the bulky equipment used to transmit data between sensors, computers, indicators and other aircraft equipment, greatly reducing the weight of aircraft and making it simple and flexible to use. In 1980, the air force made a partial modification and supplement to the standard. As one of the basis of weapon system integration and standardized management of the U.S. department of defense, this standard is widely used in aircraft integrated avionics system, plug-in management and integrated system, and gradually extended to flight control system and other fields such as tanks, ships and
aerospace. Originally used by the US Air Force for aircraft avionics systems, it is now widely used by the US and European air, sea and land forces and is becoming an international standard. With the experiment and the product is more and more complex, in the practical engineering also has the new request for the 1553 b bus, 1553 b bus transmission distance has certain limitations, if in excess of the prescribed transmission distance will cause the signal attenuation, anti-interference ability drops, the problem such as signal jump, right now, the experiment and engineering applications, the need to 1553b bus transmission to a greater distance. The transmission of bus 1553B is greatly affected by the distance. After a certain distance is reached, the bus signal will be continuously attenuated, resulting in the level failing to reach the protocol requirements, and even the level value will jump, which may lead to the bus instability or even failure to use. This paper aims to extend the transmission distance and ensure the stability and accuracy of the transmission.

2. The introduction of 1553B bus
The 1553B bus has good real-time performance, the data transmission rate is 1Mbps, each message contains 32 words at most, the time required to input a fixed message is short, the data transmission rate is higher than the general communication network, and there are reasonable error control measures and special mode commands. In order to ensure the integrity of data transmission, 1553B adopted a reasonable error control measure -- feedback retransmission error correction method[3-4]. When BC issues a command or sends a message to an RT, the terminal should send back a status word within a given response time. If the transmitted message is wrong, the terminal refuses to send back the status word, thereby reporting that the last message transmission was invalid. The unique mode command not only enables the system to complete the data communication control task, but also can check the fault situation and complete the fault-tolerant management function[5]. Due to the high requirements of bus topology for bus efficiency, 1553B has strict limits on some mandatory requirements related to bus efficiency indexes, such as command response time, message interval time, and the length of maximum and minimum data blocks for each message transmission. 1553b has command/response and "broadcast" communication mode. BC can send a time synchronization message to all RT in "broadcast" mode, so that all message transmission on the bus is controlled by the instruction issued by the bus controller, and relevant terminals should respond to the instruction and execute the operation.

3. The design of hardware circuit
In order to solve the above problems, strong electromagnetic interference and signal attenuation in the process of long-distance transmission may cause shock, which may cause data distortion or level jump and error code, resulting in transmission signal error. Now design 1553b relay circuit. The structural block diagram 1 of the design circuit is shown as follows. The circuit is externally connected with 5v voltage, and the voltage conversion chip AMS1117 is transferred to 3.3v to supply power for the whole circuit. As shown in the figure above, the transmitted signal first enters the data bus transformer PM_DB2725, which is shaken by the transformer into a set of differential signals, one positive and one negative. Differential signals are highly immune to external electromagnetic interference (EMI). An interference source affects each end of the differential pair equally. Because the voltage difference determines the signal, the two sides of the interference offset, the signal will not change significantly. Moreover, differential signals are helpful to identify small signals. In the differential signal system, the reference point is determined by the user, and the average signal of the two input terminals can be selected as the reference point, which reduces the swing range of the signal. The signal of single-end input system relies on virtual ground, while the differential signal does not need such a virtual ground, which increases the fidelity and stability of bipolar signal. The differential signal is amplified by MOS tube and received by the signal acquisition chip. It is sent to the ZYNQ series master control chip, and the data is processed by software program and forwarded to the receiving end.
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4. Implementation of software functions

The software function is realized by VHDL programming language in this paper. And the program is combined with Modelsim simulation based on Sales’s vivado software. The three elements of 1553 transport protocol are instruction word, data word and status word\(^6\). Each word is 20 bits and consists of three parts: synchronization domain (3bit), message block (16bit), parity bit (1bit).

![Figure 1](image1.png)

**Figure 1.** The circuit block diagram

![Figure 2](image2.png)

**Figure 2.** The instruction word format

The instruction word (as shown in figure 2) is composed of synchronization head, remote terminal address field, send/receive bit (T/R), subaddress/mode field, data word count/mode code field and parity check bit (P). The sync head of an instruction word is one half bit high and one half bit low in the sync domain (bits 1 through 3). The five digits immediately following the synchronization header are the remote terminal address segments, and each remote terminal is designated as a proprietary address, from decimal address 0 to decimal address 30\(^7\). The latter bit is the send/receive bit, which represents the operation required of the remote terminal. Logic 0 specifies the remote terminal as the receive operation, and logic 1 specifies the remote terminal as the send operation. The five digits immediately after the send/receive bit, used to distinguish the subaddress of the remote terminal, or as a marker for mode control of the bus system. The five digits immediately after the subaddress/mode field are used to specify the number of data words to be sent or received by the remote terminal, with the last digit used as the parity bit of the first 16 bits.

![Figure 3](image3.png)

**Figure 3.** The data word format

The data word (shown in figure 3) should consist of a synchronization header, data fields, and parity bits. The data word sync head is the one half bit low and one half bit high in the sync domain (bits 1 through 3). The 16 bits immediately following the synchronization header are the data transferred by protocol. The last bit is also a parity bit.

![Figure 4](image4.png)

**Figure 4.** The status word format
The status word (as shown in figure 4) shall consist of the synchronization head, remote terminal address field, message error bit, test means bit, service request bit, standby bit, broadcast instruction receiving bit, busy bit, subsystem flag bit, dynamic bus control receiving bit, terminal flag bit and parity check bit. The command word and the status word are the same in the synchronization domain, the first high level and then low level. The 9th bit of the status word is used to indicate that one or more words in the previously received messages of the remote terminal do not pass the prescribed validity test. Logic 1 means that the message has errors, and logic 0 means that the message has no errors. The last bit is also a parity bit.

According to the format of the transmission protocol word, the software program is written. Firstly, the synchronization head is tested to determine whether it is valid, and then the data is judged according to the synchronization head. If there is data, the filtering is carried out, and then the transmission direction is determined.

![Software flow chart](image)

Figure 5. The software flow chart

4.1 The state machine design of the program

Under the reset state, the state machine enters the waiting state (sIdle) when it is powered on, and sets the state word and data word signs, which are expressed as A_sync_csw, A_sync_dw, B_sync_csw, B_sync_dw. The corresponding flag bit is raised by detecting the synchronization head. In the waiting state, if A_sync_csw and A_sync_dw are raised, the state sA2B received by A sending B is presented, and all bytes are sent back to sIdle. If B_sync_csw and B_sync_dw are elevated, the state sB2A received by B sending A is presented, and all bytes are received and returned to sIdle. In addition to the above states, they all return to sReset and circulate until all data transmission is completed. The part of the state machine transition are as follows.

process(i_clk)
begin
if rising_edge(i_clk) then
  case state is
  when sReset =>
    state <= sIdle;
  when sIdle =>
    if (A_sync_csw='1' or A_sync_dw='1') then
      state <= sA2B;
    elsif (B_sync_csw='1' or B_sync_dw='1') then

state <= sB2A;
else
  state <= sIdle;
end if;
when sA2B =>
  if ( cntAValid > x"00" ) then
    state <= state;
  else
    state <= sIdle;
  end if;
when sB2A =>
  if ( cntBValid > x"00" ) then
    state <= state;
  else
    state <= sIdle;
  end if;
when others =>
  state <= sReset;
end case;
end if;
end process;

4.2 The simulation experiments
The simulation experiments have been done, and the results are shown in figure 6, the data sent by A_tx_dword is correctly received by B_rx_dword, and the data sent by B_tx_dword is received by A_rx_dword. The experiments show that the results and waveforms are correct.

5. Conclusion
The design of 1553b relay circuit based on FPGA is mainly researched in this paper, the novel design of hardware circuit is carried out and it can be realized as the feasible scheme by programming. The simulation and on-line experiments show that the 1553B bus relay circuit based on FPGA presented in this paper can completely extend the data communication distance of 1553B bus, and also proves certain reliability, versatility and expansibility.
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