Sorting Short Keys in Circuits of Size $o(n \log n)$

Gilad Asharov  
Bar-Ilan University

Wei-Kai Lin  
Cornell University

Elaine Shi  
CMU/Cornell

Gilad.Asharov@biu.ac.il, wklin@cs.cornell.edu, runting@gmail.com

Abstract

We consider the classical problem of sorting an input array containing $n$ elements, where each element is described with a $k$-bit comparison-key and a $w$-bit payload. A long-standing open problem is whether there exist $(k + w) \cdot o(n \log n)$-sized boolean circuits for sorting. A landmark result in this area is the work by Ajtai, Komlós, and Szemerédi (STOC’83), where they showed how to achieve sorting circuits with $(k + w) \cdot O(n \log n)$ boolean gates. The recent work of Farhadi et al. (STOC’19) showed that if the famous Li-Li network coding conjecture is true, then sorting circuits of size $w \cdot o(n \log n)$ do not exist for general $k$; however, no unconditional lower bound is known (in fact proving super-linear circuit lower bounds in general is out of the reach of existing techniques).

In this paper, we show that one can overcome the $n \log n$ barrier when the keys to be sorted are short. Specifically, we prove that there is a circuit with $(k + w) \cdot O(nk) \cdot \text{poly}(\log^* n - \log^*(w + k))$ boolean gates capable of sorting any input array containing $n$ elements, each described with a $k$-bit key and a $w$-bit payload. Therefore, if the keys to be sorted are short, say, $k < o(\log n)$, our result is asymptotically better than the classical AKS sorting network (ignoring $\text{poly} \log^*$ terms); and we also overcome the $n \log n$ barrier in such cases. Such a result might be surprising initially because it is long known that comparator-based techniques must incur $\Omega(n \log n)$ comparator gates even when the keys to be sorted are only 1-bit long (e.g., see Knuth’s “Art of Programming” textbook). To the best of our knowledge, we are the first to achieve non-trivial results for sorting circuits using non-comparison-based techniques. We also show that if the Li-Li network coding conjecture is true, our upper bound is optimal, barring $\text{poly} \log^*$ terms, for every $k$ as long as $k = O(\log n)$.
1 Introduction

Sorting is one of the most fundamental problems in algorithms design and complexity theory. Suppose we want to sort an input array with $n$ elements, each described with a $k$-bit comparison key and a $w$-bit payload. A long-standing open question is whether there exists circuits with $(k + w) \cdot o(n \log n)$ boolean gates where each gate is assumed to have constant fan-in and constant fan-out [BN16]. A landmark result in this space is the work by Ajtai, Komlós, and Szemerédi [AKS83], where they showed how to achieve sorting circuits with $O(n \log n)$ comparators — since each comparator can be implemented with $O(k + w)$ boolean gates, AKS’s construction can be implemented as a circuit with $(k + w) \cdot O(n \log n)$ boolean gates. Although it is well-known that the $n \log n$ barrier is necessary in the comparator-based model, a natural question left open by AKS is whether the $n \log n$ barrier can be overcome in the non-comparison-based model. Unfortunately, since AKS, this line of work became somewhat stuck in terms of both upper bound and lower bound.

On the upper bound front, various works have attempted to simplify the AKS construction and/or reduce its concrete constants [Pat90, Sei09, Goo14] — most notably the recent ZigZag sort of Goodrich (STOC’14) [Goo14] departed more significantly from the original AKS — unfortunately, none of these works achieved new theoretical improvements and all of them focused on the comparator-based model. It is worth pointing out that in the RAM model, it is long known how to leverage non-comparison-based techniques to get almost linear-time sorting [AHNR98, KR81, HT02, Han04, Tho02]; but these techniques do not easily translate to the circuit model since they critically rely on the ability to dynamically access memory. Another related work is that of Lin, Shi, and Xie [LSX19], who showed how to sort short keys on an Oblivious RAM in $o(n \log n)$ time — unfortunately, their algorithm is randomized and there is no obvious way to convert it to the circuit model.

On the lower bound side, there is also little progress: in fact, proving any unconditional super-linear circuit lower bounds is beyond the reach of existing techniques. The recent work of Fahardi et al. [FHLS19] proved a conditional lower bound: they showed that if the famous Li-Li network coding conjecture is true [LL04], then the $n \log n$ barrier is inherent for any boolean circuit that implements sorting. In other words, to construct an $o(n \log n)$ sorting circuit would require disproving the Li-Li network coding conjecture. The Li-Li network coding conjecture, roughly speaking, posits that network coding does not help improve the transmission rate relative to multi-commodity flow in undirected graphs, in the case of multiple unicast sessions [LL04]. While there is some evidence showing why the conjecture might possibly be true [BGS17], proving or disproving it is beyond the reach of existing techniques.

Since sorting is a very basic primitive in computer science, understanding its circuit complexity is an important open direction in theoretical computer science. In this paper, we make some new in this somewhat stagnant front; specifically we show the following novel results.

Main result 1: sorting circuits that overcome the $n \log n$ barrier for small keys. We show a result that might be surprising at first sight: when the keys to be sorted are short, one can in fact overcome the $n \log n$ barrier. Specifically, we prove the following theorem:

Theorem 1.1. Let $\epsilon > 0$ be an arbitrarily small constant. $n$ elements each $w$-bit in length and
tagged with a $k$-bit key can be sorted by a boolean circuit of size

$$(k + w) \cdot O(nk) \cdot \max (1, (\log^* n - \log^*(w + k))^{2+\epsilon}) .$$

Therefore, for short keys $k = o(\log n)$, our construction is asymptotically better than the classical result of AKS [AKS83] (ignoring polylog terms). A result of this nature might be initially surprising due to a couple natural barriers. First, the famous 0-1 principle for sorting (see Knuth’s famous textbook [Knu73]), that any comparator-based sorting circuit must consume $\Omega(n \log n)$ comparators even when the keys to be sorted are only 1 bit long. Due to the 0-1 principle, our result is necessarily non-comparison-based. To the best of our knowledge, our work is the first to achieve non-trivial results for sorting circuits using non-comparison-based techniques; and thus our techniques depart significantly from all previous sorting circuit constructions which are comparison-based [AKS83, Goo14, Bat68]. Note that although non-comparison-based techniques have been exploited in the RAM model to get almost linear-time sort — e.g., Radix sort, counting sort, and others [AHNR98, KR81, HT02, Han04, Tho02] — all these algorithms depend heavily on the ability to make input-dependent memory accesses and thus they do not have equally efficient counterparts in the circuit model.

Besides the comparison-based barrier, another subtlety is that for such a result to hold, the sorting circuit necessarily cannot preserve stability even for 1-bit keys — recall that in sorting, stability requires that in the output, elements with the same key preserve their relative ordering in the input array. More specifically, Lin, Shi, and Xie [LSX19] showed that any stable compaction circuit that treats the payload as indivisible must have at least $\Omega(n \log n)$ selector gates — here the indivisibility assumptions requires that the circuit only move the payload around through selector gates but not perform boolean computation on the encoding of the payload. The indivisibility restriction in Lin et al.’s lower bound [LSX19] can be removed if one assumes the Li-Li network coding conjecture [LL04] — this is implied by Afshani et al. [AFKL19]’s recent work.

Main result 2: linear-sized compaction circuit. When the keys to be sorted are each 1 bit long, i.e., $k = 1$, the resulting problem is also called compaction (or tight compaction) in the algorithms literature [BH91, BI93, Han07, Val75, WZ99]. In classical algorithms such as Quick Sort, or the linear-time median/selection algorithm by Blum et al. [BFP+73, BFP+72], compaction (often called “partitioning” in this context) is adopted to place elements smaller than some pivot to the left, and place elements greater than or equal to the pivot to the right.

Compaction can be trivially accomplished on a Random Access Machine (RAM) in linear time assuming that each element fits in a memory word: one can make a linear scan over the input array and whenever an element marked with the key 0 is encountered, write it to an output array; and then repeat the same for elements marked 1. For this reason, compaction was never a noteworthy abstraction in the RAM model (although indeed compaction has been extensively studied in other computation models — see Section 2.5 for more details). It almost seems natural to expect that compaction should also be attainable with a linear-sized circuit; but somewhat surprisingly, prior to our work it was not known how to accomplish this! More surprisingly, to the best of our knowledge, to date the best-known explicit compaction circuit is none other but sorting itself which incurs

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1 As will be clear later, the case when $w + k$ is large is easier. Therefore, henceforth we often write the expression $\max (1, (\log^* n - \log^*(w + k))^{2+\epsilon})$ simply as $(\log^* n - \log^*(w + k))^{2+\epsilon}$ (i.e., we assume that the expression is not smaller than 1).

2 Although their paper [AFKL19] does not explicitly state the $\Omega(nw \log n)$ lower bound result for stable sorting circuits (even for 1-bit keys), the statement is directly implied by Theorem 2 of their paper.
When $BFP$ choices of otherwise. In essence, we show that indeed a linear-sized compaction circuit exists for almost all $m$ smallest element given an input array of $n$ elements each of $w$ bits and tagged with a 1-bit key; moreover, the circuit’s size is upper bounded by

$$O(nw) \cdot \min \left( \max \left( 1, (\log^* n - \log^* w)^{2+\epsilon} \right), \ 2^{w/w} \right)$$

As a special case, if $w \geq \log^{(c)} n$ for any arbitrarily large constant $c \geq 1$ or if $w = O(1)$, then the circuit size is upper bounded by $O(nw)$. In the above, $\log^{(c)} m$ means taking iterated logarithm of $m$ for a total of $c$ times; and $\log^* m$ outputs the minimum $i$ such that $\log^{(i)} m \leq 1$. Throughout the paper, $\log$ means $\log_2$ unless noted otherwise. In essence, we show that indeed a linear-sized compaction circuit exists for almost all choices of $w$: when $w$ is at least $\log^{(c)} n$ for any constant $c$, or when $w$ is a constant. For the narrow regime when $w$ is super-constant but asymptotically smaller than any $\log^{(c)} n$ for a constant $c$, our solution is a $\min((\log^* n - \log^* w)^{2+\epsilon}, 2^{w/w})$-factor away from optimal.

**Main result 3: linear-sized circuit for selection.** The selection problem aims to select the $m$ smallest element given an input array of $n$ elements each of bit-width $w$. Given our linear-sized tight compaction circuit, it is not too difficult to combine it with the textbook median-of-median algorithm $[BFP+73, BFP+72]$: as a corollary, we have that median/selection can be computed with a boolean circuit of $O(nw) \cdot \text{poly}(\log^* n - \log^* w)$ too. To put this result in context, recall that Blum et al. $[BFP+73, BFP+72]$ showed that median/selection can be accomplished in $O(n)$ deterministic time on a RAM — in fact this elegant algorithm has been widely adopted in pedagogy. It seems natural to expect that computing median/selection should be possible with a linear-sized circuit; but this was not known until our work partly because we do not know how to compute compaction in a linear-sized circuit before. A line of work has indeed cared about the circuit complexity of selection $[Yao80, Ale69, JM92, Pip90]$, but all of the prior work focused on comparator-based circuits. It is long known that selection circuits in the comparator-based model suffer from an $\Omega(n \log n)$ size lower bound $[Yao80, Ale69, JM92, Pip90]$; and thus earlier works in this line $[Yao80, Ale69, JM92]$ focused on tightening the constant in front of the $n \log n$. A very natural question is whether we can construct asymptotically smaller selection circuits using non-comparison-based techniques — it is almost surprising that no progress has been made along this front given the fundamental nature of the problem! Our result for selection is summarized in the following corollary.

**Corollary 1.3 (Linear-sized selection circuit).** For any arbitrarily small constant $\epsilon > 0$, there exists a circuit that can select all $m$ smallest elements given any input array containing $n$ elements each of $w$ bits; and moreover its size is upper bounded by

$$O(nw) \cdot \min \left( \max \left( 1, (\log^* n - \log^* w)^{2+\epsilon} \right), \ 2^{w/w} \right)$$

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$^4$Similar to Footnote 1, we often write the expression $\max(1, (\log^* n - \log^* w)^{2+\epsilon})$ simply as $(\log^* n - \log^* w)^{2+\epsilon}$, i.e., assuming that $w$ is not too large such that $(\log^* n - \log^* w)^{2+\epsilon} \geq 1$. 

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As a special case, if \( w \geq \log^c n \) for any arbitrarily large constant \( c \geq 1 \) or if \( w = O(1) \), then the circuit size is upper bounded by \( O(nw) \).

We note that the very recent works of Asharov et al. [AKL+20a] and a subsequent follow-up [AKL+20b] have shown how to achieve compaction in linear-time on a deterministic Oblivious RAM\(^4\). Their result is of a different nature from the above Theorem 1.2 since circuits and Oblivious RAM are incomparable computation models. As we explain in more detail in Section 2.5, an \( O(n) \)-time algorithm on an Oblivious RAM does not directly lead to an \( O(nw) \)-sized circuit; and an \( O(nw) \)-sized circuit does not directly lead to an \( O(n) \)-time algorithm on an Oblivious RAM.

**Main result 4: near optimality of our sorting circuit.** Lin, Shi, and Xie [LSX19] showed that any circuit in the indivisible model that sorts \( n \) elements each with a \( k \)-bit key must have at least \( \Omega(nk) \) selector gates. Note that our sorting circuit is indeed in the indivisibility model and thus we achieve optimality for every \( k = O(\log n) \) barring \( \text{polylog}^* \) factors.

In our paper, we prove a similar lower bound, removing the indivisibility restriction on the circuit, but additionally assuming that the famous Li-Li network coding conjecture [LL04] is true. Specifically, we prove the following theorem:

**Theorem 1.4.** Suppose that the Li-Li network coding conjecture is true (see Conjecture 10.1). Moreover, suppose that each element’s payload length \( w > \log_2 n - k \), and the key length \( k \leq \log_2 n \). Then, any constant fan-in, constant fan-out boolean circuit that can sort \( n \) elements each with a \( k \)-bit key and a \( w \)-bit payload must have size at least \( \Omega(nk \cdot (w - \log_2 n + k)) \).

In comparison, the recent work of Fahardi et al. [FHLS19] implied a special case of the above lower bound when there are no constraints on the length of the the keys to be sorted\(^5\). Note also that our lower bound works only when the payload size is not too small, i.e., when \( w > \log_2 n - k \). Since our upper bound works irrespective of \( w \) — in fact our upper bound works in the indivisible model — Theorem 1.4 also shows that for sufficiently large \( w \), our upper bound result is asymptotically optimal barring \( \text{polylog}^* \) terms. For the case of small \( w \), it remains an interesting open question whether there exists better upper bounds. However, note that any better upper bound for small \( w \) cannot be in the indivisible model like our algorithm, due to the \( \Omega(nk) \) lower bound on the number of selector gates in the indivisible model [LSX19].

## 2 Technical Highlight

In this section, we provide an informal technical roadmap of our main ideas. To obtain the sorting result stated in Theorem 1.1, our blueprint is the following:

1. First, we will construct a linear-sized compaction circuit — here when we say linear-sized, we omit the \( \text{polylog}^* \) term for convenience. Recall that compaction is the problem of sorting elements with 1-bit keys.

2. Once we know how to solve the 1-bit special case with a linear-sized circuit, we then build on top this idea to construct a linear-sized circuit for computing selection (i.e., selecting the \( m \)-th smallest element).

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\(^4\)A deterministic Oblivious RAM is one in which the algorithm’s memory access patterns must be determined only by the size of input (but not the content of input nor randomness).

\(^5\)The statement in their paper [FHLS19] is for the RAM model but their techniques imply a lower bound in the boolean circuit model for the general case without any constraints on the key length.
3. Finally, using linear-size compaction and selection as building blocks, we show how to construct a circuit that sorts \( k \)-bit keys through a clever 2-parameter recursion.

Below, we begin by describing how to accomplish linear-sized compaction. We stress that even for this 1-bit special case, it is important that the scheme be \textit{non-comparison-based}, since otherwise due to the 0-1 principle (see Knuth’s “Art of Programming” textbook [Knu73]), the circuit must incur at least \( \Omega(n \log n) \) comparators. In our presentation below, we will point out where our scheme relies on non-comparison-based techniques, since this is why our techniques fundamentally depart from previous sorting networks (all of which, to the best of our knowledge, are comparator-based).

\subsection{Warmup: From Pippenger’s Super-Concentrator to \( O(n \log n + nw) \)-Sized Compaction Circuit}

Pippenger [Pip96] describes an \( O(n) \)-sized super-concentrator construction with \( n \) sources and \( n \) destinations, such that given any subset of \( s \) sources and any subset of \( s \) destinations, a set of vertex-disjoint paths exist between the sources and destinations. If one thinks of the \( s \) sources as clients, and the \( s \) destinations as servers, a super-concentrator allows each client to receive service from a server over \textit{congestion-free} paths. Note that all servers are assumed to provide the same type of service, and thus a client can be matched with any server. Not only does Pippenger show the existence of vertex-disjoint paths between any \( s \) sources and any \( s \) destinations, importantly, he describes an explicit, efficient algorithm for finding a set of such paths when the \( s \) sources and \( s \) destinations have been specified — henceforth we call this the \textit{route-finding} algorithm.

To use such a self-routing super-concentrator to solve the compaction problem, one may think of the \( s \) sources as the \( s \) input elements marked as distinguished, and the \( s \) destinations as the first \( s \) positions of the output array, i.e., where the distinguished elements want to go. Now, a trivial observation is that in Pippenger’s construction, the route-finding algorithm can be implemented as an \( O(n) \)-time RAM algorithm. With some extra work, one can show that in fact, the same route finding algorithm can be implemented as an \( O(n \log n) \)-sized circuit: the detailed circuit construction involves a few non-trivial technicalities but since this is arguably not the most exciting part of our techniques, we defer the details to Sections 4.3, 4.4, and 5.

Once the routes have been found, the \( s \) distinguished elements can be routed to their respective destinations with an \( O(nw) \)-sized circuit. This results in an \( O(n \log n + nw) \)-sized compaction circuit\footnote{We will actually need something slightly stronger than merely converting Pippenger’s self-routing super-concentrator an \( O(n \log n + nw) \)-sized compaction circuit; see Remark 1.}.

The usage of non-comparison techniques. We stress that even this warmup scheme must necessarily be non-comparison-based since for \( w \geq \log n \), the circuit size is upper bounded by \( O(nw) \). Thus we now reflect on how non-comparison-based techniques helped us achieve this result which otherwise would have been impossible. The warmup algorithm has a \textit{metadata phase} (i.e., the route-finding phase) which involves looking at only the distinguished/non-distinguished indicator of each element but not the elements themselves, and a \textit{routing} phase that actually moves the elements around according to the plan computed by the metadata phase. The metadata phase relies on counting and hence makes the algorithm inherently non-comparison-based; and moreover, the cost of the metadata phase does not depend on \( w \), i.e., the bit-width of the elements. The routing phase, on the other hand, moves \( O(n) \) elements around since the super-concentrator is linear in size (and moving each element around incurs \( O(w) \) number of gates when implemented in circuit). This key insight will continue to help us throughout the remainder of the paper.
2.2 A Slightly Deeper Dive into Pippenger’s Construction

Our next goal is to improve the warmup scheme to $O(nw) \cdot \text{poly}(\log^* n - \log^* w)$. Before explaining our approach in the subsequent Section 2.3, it helps to dissect Pippenger’s construction further. For ease of understanding, we focus on achieving tight compaction, i.e., routing any $s$ positions in the input to the first $s$ positions in the output — but keep in mind that both Pippenger’s and our construction can be generalized to routing any $s$ positions in the input to any $s$ positions in the output. Furthermore we explain his algorithm with a circuit computation model (although their original description is in a distributed automata model).

Loose compaction. To achieve tight compaction, Pippenger first constructs a gadget capable of a relaxed form of compaction henceforth called loose compaction. In loose compaction, we have an input array of length $n$ where at most $n/128$ elements are real and the rest are dummy, and we would like to compress this array to half of the original size, while preserving the multiset of real elements. Specifically, the loose compaction leverages a bipartite expander graph with $O(n)$ vertices where there are twice as many vertices on the left than on the right. Each vertex has $O(1)$ edges. A route-finding algorithm can be run to find a way to route the real elements on the left to the right without causing congestion, compressing the array by a half in the process. With a little more work, we show that it is possible to implement their route-finding algorithm for loose compaction with an $O(n \log n)$-sized circuit (to be spelled out in Section 4.3). Once the routes have been found, the actual routing of the elements from the left to the right can be accomplished with an $O(nw)$-sized circuit since the expander graph has only $O(n)$ edges in total. Thus, the entire loose compaction circuit consumes $O(nw + n \log n)$ gates.

Upgrading from loose to tight compaction. Pippenger then goes to construct a tight compaction algorithm given a loose compaction gadget. In this paper, we will view this part of the algorithm as a way to upgrade a loose compactor to a tight one. Given a loose compactor, to upgrade it to a tight compactor requires additional use of certain bipartite expander graphs with appropriate vertex expansion. Pippenger’s original description was for a Distributed Finite Automata model, but later in Section 5, we will describe how to accomplish this loose-to-tight upgrade in a circuit model of computation while preserving efficiency in some technical sense. This requires resolving additional technicalities which we briefly mention below.

Remark 1. One technicality is the following: given a circuit that accomplishes loose compaction with $\text{LC}(n, w)$ gates, it is quite easy to implement Pippenger’s ideas in a circuit model and upgrade it to a tight compaction circuit consuming $O(\text{LC}(n, w) + nw + n \log n)$ gates. In fact, this would be sufficient to give us the warmup result, that is, an $O(nw + n \log n)$-sized circuit for tight compaction. This na"ive approach, however, turns out not to be enough for the bootstrapping steps needed later in Section 2.3 to improve the circuit size. It will become clear soon that for the bootstrapping steps, we need that the loose-to-tight upgrade be accomplished with a circuit of $O(\text{LC}(n, w) + nw)$ gates: showing that this is possible is subtle but can be accomplished through standard techniques — we thus defer the details to Section 5.

2.3 Linear-Sized Compaction Circuit: Our Approach in a Nutshell

For simplicity, in the main body of the paper, we first present a construction with a slightly looser $\text{polylog}^*$, i.e., not caring about the constant-degree of the $\text{poly}(\cdot)$ function. We shall tighten the constant-degree of the $\text{poly}$ to $2 + \epsilon$ in Appendix B.
Let $\text{poly}(\cdot)$ denote an appropriate polynomial function; let $\alpha(n) \leq \log^* n$ be any integer function that is upper-bounded by $\log^* n$ everywhere. Our construction (implicitly) builds an $(n \cdot \text{poly}(\alpha))$-sized super-concentrator with a route-finding algorithm that can be implemented as an $(n \cdot \log^*(n) \cdot \text{poly}(\alpha))$-sized circuit. Specifically, if we choose $\alpha(n) = \log^* n - \log^* w$, we have an $(n \cdot \text{poly}(\log^* n - \log^* w))$-sized super-concentrator whose routing-finding algorithm can be computed by an $(nw \cdot \text{poly}(\log^* n - \log^* w))$-size circuit. In comparison with Pippenger’s super-concentrator, we somewhat significantly reduce the size of the circuit implementing the route-finding algorithm, at the price of a slightly super-linear super-concentrator.

The key insight is a new technique that involves repeated bootstrapping and boosting: we use loose compaction to bootstrap tight compaction with a constant blowup in circuit size; then in turn, we use tight compaction to construct an asymptotically better loose compaction; and then in turn, we use the better loose compaction to bootstrap a better tight compaction, and so on. See Figure 1 for a demonstration. More specifically,

- **Tight compaction from loose compaction.** Given a function $1 \leq f(n) \leq \log n$, if loose compaction can be accomplished with a $C_{lc} \cdot (nf(n) + nw)$-sized circuit, then we can accomplish tight compaction with a $C \cdot C_{tc} \cdot (nf(n) + nw)$-sized circuit where $C$ and $C_{tc}$ are suitable constants. This uses the same techniques as in Pippenger’s work but now applying them to the circuit model;

- **Loose compaction from tight compaction.** Let $f(n)$ be a function satisfying $1 \leq f(n) \leq \log n$, and given a tight compaction circuit of $C_{tc} \cdot (nf(n) + nw)$ size, we can construct a $C \cdot C_{tc} \cdot (nf(f(n)) + nw)$-sized loose compaction circuit as follows where $C$ and $C_{tc}$ are suitable constants:

  1. Divide the input into chunks of $f(n)$ elements; for simplicity we shall assume that $n$ is divisible by $f(n)$ here and the indivisible case is handled later in our technical sections. Mark chunks that have more than $f(n)/32$ real elements as dense and those with at most $f(n)/32$ real elements as sparse.

  Use tight compaction to move all the dense chunks to the front and all the sparse chunks to the end. Note that this step can be implemented as a $C_{tc} \cdot (n + nw)$-sized circuit.

  2. It is easy to show that there are at least $\frac{3n}{4f(n)}$ sparse chunks. Now, for each of the trailing $\frac{3n}{4f(n)}$ sparse chunks, use a tight compaction circuit to compress away $31f(n)/32$ dummy
elements. This step requires a $C_{tc} \cdot (f(n)f(f(n)) + f(n)w)$-sized circuit per chunk and thus over all chunks, the total circuit size is $(n/f(n)) \cdot C_{tc} \cdot (f(n)f(f(n)) + f(n)w) = C_{tc} \cdot (n f(f(n)) + nw)$.

3. The output is simply a concatenation of the following: i) the first $\frac{n}{17(n)}$ chunks; and ii) the remaining $f(n)/32$ elements for each of the remaining $\frac{3n}{17(n)}$ chunks. It is not hard to show that the resulting array is less than half of the length of the original and no real element is lost during this process.

Now, as a starting point, we have a loose compaction circuit denoted $\mathbf{LC}_0$ whose size is $C_0 \cdot (n \log n + nw)$ for loosely compacting an input array of $n$ elements each of $w$ bits, where $C_0$ is an appropriate constant — as mentioned in Section 2.2, we can construct such an $\mathbf{LC}_0$ using Pippenger’s loose compactor construction but implementing his construction in a $O(n \log n + nw)$ sized-circuit involves some non-trivial technicalities which will be explained in Section 4. With $\mathbf{LC}_0$, we can construct a tight compaction circuit denoted $\mathbf{TC}_1$ of size at most $C_0 \cdot (n \log n + nw)$. Given $\mathbf{TC}_1$, we can in turn construct a loose compaction circuit denoted $\mathbf{LC}_1$ whose size is upper bounded by of size at most $C^2 \cdot C_0 \cdot (n \log n + nw)$. Given $\mathbf{LC}_1$, we can in turn construct a tight compaction circuit denoted $\mathbf{TC}_2$ of size at most $C^3 \cdot C_0 \cdot (n \log n + nw)$. Given $\mathbf{TC}_2$, we can in turn construct a loose compaction circuit denoted $\mathbf{LC}_2$ of size at most $C^4 \cdot C_0 \cdot (n \log n + nw)$.

Let $\alpha = \log^* n$, and let $2^{d-1} = \alpha$. After $d$ iterations of the above recursion, we will obtain a tight compaction circuit $\mathbf{TC}_d$ whose size is upper bounded by $C^{2d-1} \cdot C_0 \cdot n \cdot (\log^{(2d-1)} n + w) = O(1) \cdot \text{poly}(\alpha) \cdot n \cdot (\log^*(n) + w)$. Setting $\alpha = \log^* n - \log^* w$ would give us $\log^*(n) n = O(w)$ and thus we get a tight compaction circuit of size $O(nw) \cdot \text{poly}(\log^* n - \log^* w)$.

### 2.4 Sorting Circuits for Small Keys

Now we have solved the 1-bit special case of Theorem 1.1, we would like to generalize the scheme to sort small keys. If the 1-bit sorter were stable, then we can rely on radix sort to sort the elements one bit at a time. Unfortunately, as mentioned, our 1-bit sorter is not and cannot be stable. Instead, we rely on a non-trivial two-parameter recursion that is inspired by Lin et al. [LSX19] — in comparison, their approach relies on randomness; but we show how to adapt their ideas to a deterministic approach.

**Linear-sized selection circuit.** To describe our sorting circuit result, we will need yet another building block: a linear-sized selection circuit (ignoring $\text{polylog}^* n$ terms). It turns out that given a linear-sized compaction circuit, it is not too difficult to construct a linear-sized selection circuit based on Blum et al. [BFP+73]’s idea. To select the $m$-th smallest element, Blum’s algorithm first divides the elements into $n/5$ groups each containing 5 elements, computes the median of each group, and then recursively computes the median of the medians henceforth called a pivot. At this moment, perform a partitioning: move all elements smaller than or equal to the pivot to the left and all other elements to the right and let $Y$ be the resulting array. Now, depending on the choice of $s$, recurse on either the first $7n/10$ elements of $Y$ or the last $7n/10$ elements of $Y$.

Blum et al’s selection algorithm runs in linear time on a RAM. How can we implement it in the circuit model with linear number of gates? The crux is solving the partitioning step with a linear-sized circuit since it is not too hard to check that all other steps are easy to implement in a circuit while preserving efficiency. Clearly, the partitioning step can be solved with a compaction circuit: we can label each element with a 0-key if it is smaller than or equal to the pivot and a 1-key otherwise. Using our linear-sized compaction circuit to realize partitioning in Blum et al.’s algorithm, we can then get a linear-sized selection circuit.
Our sorting circuit. We are now ready to present our sorting circuit construction. To upgrade from 1-bit sorting to multiple bits, we can rely on a recursion with two parameters, \( n \) and \( K = 2^k \). This two-parameter recursion trick is inspired by Lin et al. [LSX19]: however Lin et al. [LSX19] relies on randomness to perform divide-and-conquer and make measure concentration arguments in their proofs. To get rid of the randomness needed in their algorithm, we instead rely on the aforementioned linear-sized selection gadget to perform the divide-and-conquer (this was not an available building block in Lin et al.’s work).

Initially, we have \( n \) elements each tagged with a \( k \)-bit key, i.e., in total there can be \( K = 2^k \) distinct keys. We first rely on a linear-sized selection circuit to find the median. We then partition the input \( n \) elements into two halves: those that are smaller than or equal to the median, and all other elements. Note that to implement this partitioning in the circuit model, we will rely on our new linear-sized compaction circuit. Now, a crucial observation is the following: at least one of the halves, henceforth called the *good half*, will have at most \( \lceil K/2 \rceil \) distinct keys, while the other *bad half* may still have up to \( K \) distinct keys. We now recurse on each half to sort each half — the good half of the recursion adopts the parameters \( n/2, \lceil K/2 \rceil \), whereas the bad half adopts the parameters \( n/2, K \). Thus we have the following recurrence where \( T(n, K) \) denotes the circuit size for sorting \( n \) elements each with \( \log_2 K \)-bit keys:

\[
T(n, K) = T\left(\frac{n}{2}, K\right) + T\left(\frac{n}{2}, \lceil K/2 \rceil\right) + h(n, w + \log K) \cdot O(n(w + \log K)),
\]

where \( h(x, y) := \text{poly}(\log^* x - \log^* y) \), and the base cases are: if \( K = 1 \) then \( T(n, K) = O(nw) \cdot h(n, w + \log K) \); moreover, if \( n = O(1) \) then \( T(n, K) = O(w + k) \). Solving this recurrence, we will obtain that

\[
T(n, K) = O(n(w + \log K)) \cdot \log K \cdot h(n, w + \log K)
\]

2.5 Additional Related Work

Sorting. Lin, Shi, and Xie [LSX19] considered the complexity of (randomized) oblivious sorting for small keys — their work is in a randomized Oblivious RAM model of computation\(^7\) and they show how to accomplish sorting in \( O(nk \log \log n/\log k) \) time assuming that the keys to be sorted are only \( k \) bits long and the payload can fit in a single memory word. Their result cannot be directly converted the circuit model due to the use of randomness; instead, they show how to interpret their result in a “probabilistic circuit family” model, i.e., for every input array, an overwhelming fraction of the circuits in the family can correctly sort it. In such a probabilistic circuit family model, they accomplish \( O(nw \cdot k \log \log n/\log k) \) circuit size for \( k \)-bit keys, which is asymptotically worse than our deterministic result when \( k < 2^{\log \log n/(\log^* n)^{2+\epsilon}} \).

It is also long known that using non-comparison-based techniques, sorting can be accomplished on a RAM in \( o(n \log n) \) time [AHNR98, KR81, HT02, Han04, Tho02]. Unfortunately, all these algorithms inherently rely on input-dependent memory accesses and we know of no approach to convert these algorithms to the circuit model in an efficiency-preserving manner. By contrast, in the circuit model, the non-comparison-based approach has not been explored before, even though it was a natural open problem since Knuth’s textbook [Knu73], where it was shown that comparison-based techniques have an \( \Omega(n \log n) \) lower bound even for sorting 1-bit keys.

Goodrich and Kosaraju [GK96] show that on a parallel pointer machine, sorting \( k \)-bit integers in time \( O(nk) \) using binary search trees. However, in their algorithm, the access patterns of the program are input data dependent, and thus their techniques do not directly lend to our result in the circuit model.

\(^7\) A probabilistic Oblivious RAM is one that requires the distribution of the algorithm’s memory access patterns to be computationally or statistically close regardless of the input.
Compaction and selection. As mentioned, compaction is trivial to accomplish on a RAM; and linear-time selection on a RAM is also a classical result [BFP+73] now widely taught in undergraduate algorithms lectures. A line of work was concerned about the circuit complexity of selection and compaction [Yao80, Ale69, JM92, Pip90]; but all earlier works focused on the comparator-based model. Due to the famous 0-1 principle described as early as in Knuth’s textbook [Knu73], there is an $\Omega(n \log n)$ lower bound for compaction with comparator-based circuits. Furthermore, selection is also known to have an $\Omega(n \log n)$ lower bound in a comparator-based circuit model [Yao80, Ale69, JM92, Pip90] — and this explains why all earlier works [Yao80, Ale69, JM92, Pip90] focus on tightening the constant in front of the $n \log n$. While it is extremely natural to ask whether the $n \log n$ barrier can be circumvented without the comparator-based restriction, it is surprising that so far, no progress has been made along this front!

Several works have considered compaction and selection in other incomparable models of computation as explained below — none of these results easily give rise to a circuit result. Leighton et al. [LMS95] show how to construct comparison-based, probabilistic circuit families for selection, with $O(n \log \log n)$ comparators; again, here we require that for every input, an overwhelming fraction of the circuits in the family can give a correct result on the input. One interesting observation is that although deterministic, comparator-based selection circuits have a $\Omega(n \log n)$ lower bound [LMS95, Ale69], probabilistic circuit families do not inherit the same lower bound. Subsequent works [LSX19, MZ14] have improved Leighton’s result by removing the restriction that the circuit family must be parametrized with $m$, i.e., the rank of the element being selected, without increasing the asymptotical overhead. These works also imply that compaction can be accomplished with in $O(n \log \log n)$ time on a randomized Oblivious RAM [LSX19, MZ14].

Very recently, Asharov et al. considered how to accomplish compaction on deterministic Oblivious RAMs in linear work [AKL+20a]. Their work was subsequently extended [AKL+20b] to a PRAM setting. Moreover, Dittmer and Ostrovsky improve its concrete constants by introducing randomness back into the model [DO20]. It turned out that linear-time oblivious compaction played a pivotal role in the construction of an optimal Oblivious RAM (ORAM) compiler [AKL+20a], a machine that translates a RAM program to a functionally-equivalent one with oblivious access patterns. Specifically, earlier ORAM compilers relied on oblivious sorting which requires $\Omega(n \log n)$ time either assuming the indivisibility model [LSX19] or the Li-Li network coding conjecture [F HLS19]; whereas more recent works [AKL+20a, PPRY18] observed that with with a lot more additional work, we could replace oblivious sorting with the weaker compaction primitive.

We stress that known linear-time compaction algorithms [AKL+20a, AKL+20b] on Oblivious RAMs/PRAMs and our compaction circuit are of incomparable nature:

- First, an $O(n)$-time construction on a deterministic Oblivious RAM [AKL+20a, AKL+20b] does not directly give rise to an $O(n \cdot w)$-sized compaction circuit in general (assuming that $w = O(\log n)$ can be stored in a single memory word). This is because on a RAM, operations on log $n$-bit words can be accomplished with unit cost, whereas in a boolean circuit they typically cost at least log $n$ gates. This is the case with the algorithms of Asharov et al. [AKL+20a, AKL+20b] too. In fact, these algorithms achieve linear work by heavily and explicitly relying on the fact that operations on log $n$-bit words can be accomplished with unit cost through techniques called packing. It might be possible to use the same techniques as in Section 2.1 to convert the linear-time compaction algorithms on Oblivious RAMs [AKL+20a, AKL+20b] to the circuit model — indeed one could try this direction, but even if it works, it would result in a circuit of size $O(n \log n + nw)$, i.e., no better than converting Pippenger’s self-routing superconcentrator [Pip96] to the circuit model.

- Second, our $O(nw) \cdot \poly(\log n - \log^* w)$ compaction circuit result also does not give rise to an
Oblivious RAM algorithm running in time \( O(n) \cdot \text{poly}(\log^* n - \log^* w) \), even if assuming that the word size is \( w = O(\log n) \). In order to see that, consider a circuit of size \( O(w) \) boolean gates. One might hope to get an oblivious RAM counterpart that consumes \( O(1) \) work—by packing all the \( w \)-wires of the circuit into a single word in the RAM model and performing operations on the packed word. However, in order to achieve \( O(1) \) work, the operations on these \( w \)-wires in the circuit must fit one of the operations allowed in the RAM model, such as additions, multiplications, etc. Since boolean gates are usually more general and provide a different type of operations on each one of the wires individually, in the most general case we will still have to perform \( w \) different operations in the RAM model even when packing the \( w \)-wires into one memory word in the RAM model. That is, the circuit may not have the SIMD (single instruction, multiple data) structure such that operations on \( w \) bits can be packed into operations on the same work on a RAM. We also refer the readers to the work of Boyle and Naor [BN16] who discussed the same technical issue.

Finally, sorting and selection have also been studied in the Parallel RAM (PRAM) model [BH91, BH93, Han07] as well as in Valiant’s comparison-based parallel computation model which charged only the comparisons but not the boolean computations that decided which elements to compare [Val75, WZ99].

**Other related work.** Besides Pippenger’s self-routing super-concentrator [Pip96], the work by Arora, Leighton, and Maggs [ALM90] considered a self-routing permutation network. Their construction is not a sorting network. Further, converting their non-blocking network to a permutation circuit would incur at least \( \Omega(n \log^2 n) \) gates [bmm]. Pippenger’s work [Pip96] adopted some techniques from the Arora et al. work [ALM90].

## 3 Preliminaries

**Notations.** Unless otherwise noted, \( \log \) always means \( \log_2 \). Throughout the paper, the notation \( \log^{(i)} n \) means \( \log \log \log \ldots \log n \) where \( \log \) is taken \( i \) times; the notation \( \log^* n \) means the smallest \( i \in \mathbb{N} \) such that \( \log^{(i)} n \leq 1 \).

### 3.1 Circuit Model of Computation

We adopt the standard boolean circuit model of computation [Sav97]. A boolean circuit consists of AND, OR, and NOT gates. Gates are connected through wires. Each gate’s output can be fed into \( O(1) \) number of other gates as input. All the gates and their wires form a directed acyclic graph. By definition, such a boolean circuit has constant fan-in and constant fan-out. A circuit’s size is the number of gates the circuit contains.

### 3.2 Operational Model Used in Our Paper

For convenience, we use the following operational model for circuits when describing our algorithms. In our operational model, we allow the following gadgets in our circuitry: 1) constant-sized gadgets that implement an arbitrary truth table between the \( O(1) \) input bits and the \( O(1) \) output bits; and 2) selector gates. When defining our circuits we will count explicitly how many generalized boolean gates the circuit has, and how many selector and reverse selectors are there. We give more explanations below and describe how to convert a circuit in our operational model to a standard boolean circuit with constant fan-in and constant fan-out.
Selector and reverse selector gates. A $w$-selector gate ("MUX") takes in one bit $b$ and two input elements $m_0, m_1$ each of bit-width $w$, and outputs $m_b$. Each $w$-selector gate can be realized with $C \cdot w$ number of AND, OR, and NOT gates where $C > 1$ is a universal constant. Reverse selector gates are the opposite. A $w$-reverse selector gate takes one element $m$ of bit-width $w$ and a signal $b \in \{0, 1\}$ as input and outputs $(m, 0^w)$ if $b = 0$ and $(0^w, m)$ if $b = 1$. Henceforth in the paper whenever we count selector and reverse selector gates, we do not distinguish between them and count both towards selector gates.

Generalized boolean gates. Generalized boolean gates are allowed to have constant fan-in and constant fan-out. Without loss of generality, we allow each generalized boolean gate to implement any truth table between the $O(1)$ input bits to the $O(1)$ output bits. Realizing such a generalized boolean gate with AND, OR, and NOT gates will only incur an $O(1)$ factor blowup in the circuit’s size. Later in our paper, we will use generalized boolean gates of fan-in at most 3 and fan-out at most 3.

Unbounded fan-out is free. From standard complexity theory textbooks [Sav97], we know that constant fan-in, unbounded fan-out circuits of size $G(n)$ can be converted to constant fan-in, constant fan-out circuits of size $O(G(n))$. Therefore, in our operational model, we allow the output of a gate to be fed into unbounded number of gates.

Remark 2 (Selector gates and indivisibility model). Although it may seem like selector gates are just another type of circuit gadgets like those in Section 4, we incorporate selector gates into our operational model for convenience.

In fact, our construction later will use selector gates to move payloads around, and our construction will not perform any boolean computation or encoding of the payloads. This also means that our construction works in the indivisibility model. In some works [BN16, LSX19], the indivisibility model is also referred to as the balls-and-bins model, i.e., each element’s payload string behaves like an opaque, indivisible ball.

Given a circuit in the indivisibility model, one construct a mirroring circuit in the reverse order where selector gates are converted to reverse-selector gates, and this reverse circuit can route the payloads back into their initial positions. Our construction later will make use of such “reverse routing”.

4 Useful Circuit Gadgets

Besides the operational model described in Sections 3, we describe here some more complicated components for our circuits. Those includes some basic gadgets in Section 4.1 (comparators, adders, counting, prefix sum), a circuit for converting a binary number to unary (Section 4.2), and much more complicated components: the basic (slightly inefficient) Loose Compaction circuit (Section 4.3) and Loose Swap (Section 4.4).

4.1 Basic Gadgets

Comparator. A $k$-bit comparator takes two values each of $k$ bits, and outputs an answer from a constant-sized result set such as $\{>, <, =\}$, or $\{\geq, <\}$, or $\{\leq, >\}$. Note that the outcome can be expressed as 1 to 2 bits.

Fact 4.1. A $k$-bit comparator can be implemented with $k$ generalized boolean gates.
Adder. A $k$-bit adder takes two values each of at most $k$ bits, and outputs the sum of the two encoded as $k + 1$ bits. The following fact is obvious by emulating the hand method of addition.

Fact 4.2. A $k$-bit adder can be implemented with $k$ generalized boolean gates each with fan-in 3 and fan-out 2.

Counting. We consider a simple circuit gadget that counts the number of 1s in an input array containing $n$ bits.

Fact 4.3. Given an input array containing $n$ bits, counting the number of 1s in the input array can be realized with a circuit containing $6n$ generalized boolean gates.

Proof. To see this, consider a tree of adders. The input array forms the leaves of the tree where each leaf represents one bit. At the leaf level there are $n/2$ adders adding 1-bit numbers and the outcome is at most 2 bits; at the next level, there are $n/4$ adders adding 2-bit numbers and the outcome is at most 3 bits; at the next level, there are $n/8$ adders adding 3-bit numbers and the outcome is at most 4 bits, and so on. By Fact 4.2, the total number of generalized boolean gates needed is at most

$$\frac{n}{2} \cdot 1 + \frac{n}{4} \cdot 2 + \frac{n}{8} \cdot 3 + \ldots + 1 \cdot \log_2 n \leq 6n$$

Prefix sum. We consider a prefix sum circuit gadget, which upon receiving an input $I$ containing $k$ bits, outputs the number of 1s encountered in all $k$ prefixes, that is, $I[: 1], I[: 2], I[: 3], \ldots, I[: k]$. This is implemented using a counter consisting of $\log k$ bits, and scanning the array and outputting the value of the counter each time.

Fact 4.4. The aforementioned prefix sum can be computed with a circuit with at most $k \log k$ generalized boolean gates where $k$ is the input length.

Find in array. Given an input array containing $n$ elements each with a $k$-bit label and a $w$-bit payload, given also a desired $k$-bit label $L^\ast$. Find the first occurrence in the input array an element whose label is $L^\ast$ and output any fixed canonical value if not found. This is implemented by $n$-iteration, compare the $k$-bit label of the current element in the array with $L^\ast$. The result of each comparison is used for a $w$-selector gate that selects whether to use the current $w$-bit payload or the one from previous iteration.

Fact 4.5. The above task to find an element with desired $k$-bit label in an array of length $n$ can be solved with $nk$ generalized boolean gates and $n$ number of $w$-selector gates.

4.2 Binary to Unary Conversion

Fix $n \in \mathbb{N}$. For any integer $k \in \{0, 1, \ldots, n\}$, the binary-to-unary conversion takes as input $k$ and then outputs an $n$-bit binary string $u$, where $k$ is represented in binary (string of $\lceil \log n \rceil$ bits), and $u$ is the unary representation of $k$, i.e., the head $k$ bits of $u$ are all 0s and the tail $n - k$ bits of $u$ are all 1s.

Suppose $n$ is a power of 2 and $k$ is represented in $\log n + 1$ bits. The following procedure implements binary to unary conversion. Imagine that the $n$ output bits are at the leaf level of a complete binary tree.
Algorithm 4.6: Binary to Unary

Initially, the root is labelled “0” if the most significant bit of $k$ is 1 (i.e., $k = n$); otherwise, the root is labelled “$M$” denoting “mixed”. Henceforth consider the root to be at level 1 of the tree.

For each level $\ell$ from the root to the leaf (not including the leaf level):

1. if the node’s label is not “$M$”, simply pass its label to both children;
2. else let $k_\ell$ denote the $(\ell + 1)$-th bit of $k$:
   - if $k_\ell = 1$, then pass “0” to the left child and pass “$M$” to the right child;
   - if $k_\ell = 0$, then pass “1” to the right child and pass “$M$” to the left child;

Finally, if a leaf node receives the label “$M$” it is treated as “1”.

When $n$ is a power of 2, the above can be implemented as a circuit consisting of at most $2n$ generalized boolean gates. When $n$ is not a power of 2, we can simply skip a part of the tree in the above procedure such that we propagate messages only to the first $n$ leave nodes; thus the total number of generalized boolean gates is also upper bounded by $2n$. We have the following fact.

Fact 4.7. The binary-to-unary conversion task can be implemented in a circuit with $2n$ generalized boolean gates.

4.3 Loose Compaction

An $(n, w)$-loose compactor solves the following problem:

- **Input**: an array containing $n$ elements of the form $\{(b_i, v_i)\}_{i \in [n]}$, where each $b_i \in \{0, 1\}$ is a metadata bit indicating whether the element is real or dummy, and each $v_i \in \{0, 1\}^w$ is the payload. The input array is promised to have at most $n/128$ real elements.
- **Output**: an array containing $n/2$ elements, such that the multiset of real elements contained in the output equals that of the input, i.e., no real element is lost or created.

In other words, loose compaction takes a relatively sparse input array containing only a small constant fraction of real elements; it compresses the input to half its original length while preserving all real elements in the input.

Theorem 4.8. There is a circuit in the indivisible model with $O(n \log n)$ generalized boolean gates and $O(n)$ number of $w$-selector gates that realizes an $(n, w)$-loose compactor.

The remainder of this subsection will be dedicated to prove Theorem 4.8. We describe how to implement loose compaction as a circuit based on Pippenger’s elegant ideas [Pip96]. Specifically, we describe a slight variant of Pippenger’s idea that appeared in Asharov et al. [AKL+20a].

Expander graphs. The construction will rely on a suitable family of bipartite expander graphs denoted $\{G_{\varepsilon,m}\}_{m \in \mathbb{N}}$. Specifically, $\varepsilon \in (0, 1)$ is a suitable constant referred to as the spectral expansion. The graph $G_{\varepsilon,m}$ has $m$ vertices on the left henceforth denoted $L$, and $m$ vertices on the right henceforth denoted $R$, and each vertex has $d := d(\varepsilon)$ number of edges where $d$ is a constant that depends on $\varepsilon$. 
Construction. We formally describe the construction in Algorithm 4.9, which is based on the one presented in [AKL+20a]. We then present a circuit that implements this algorithm.

The main idea of the algorithm is to first distribute the real elements, such that when considering small chunks, no chunk is “dense”. Then we can easily compact each chunk separately. The main technical challenge is in distributing the real elements. In more detail, the input array is grouped into chunks of $d/2$ size. Chunks that have at most $d/8$ elements (i.e., a quarter loaded) are said to be sparse and chunks that have more than $d/8$ elements are said to be dense. We can consider the chunks to be left-vertices in the bipartite expander graph $G_{\epsilon,m}$. Now each dense chunk will distribute its real elements to its neighbors on the right, such that each right vertex receives no more than $d/8$ elements, i.e., each vertex on the right is now a sparse chunk too. At this moment, we can replace dense chunks on the left with dummy elements, as all real elements had moved to the right. At this point all chunks are sparse, and we can compress each chunk on the left and the right to a quarter its original size without losing any real elements. All compressed chunks are concatenated and output, and the output array is a half the length of the input.

The distribution of the real elements to its neighbors on the right requires some additional care, as we have to guarantee that no node on the right will become dense. We will have to compute on which subset of edges we will route the real elements. This is done via the procedure ProposeAcceptFinalize described below.

ProposeAcceptFinalize subroutine. We now describe the ProposeAcceptFinalize subroutine in Algorithm 4.10, which is the key step to achieve the aforementioned distribution of dense chunks. To make the description more intuitive, henceforth we call each vertex in $L$ a factory and each vertex in $R$ a facility. Initially, imagine that the dense vertices correspond to factories that manufacture at most $d/2$ products, and the sparse vertices are factories that are unproductive. There are at most $m/32$ productive factories, and they want to route all their products to facilities on the right satisfying the following constraints: 1) each edge can route only 1 product; and 2) each facility can receive at most $d/8$ products. The ProposeAcceptFinalize algorithm described below finds a set of edges $M$ to enable such routing, also called a feasible route as explained earlier.

Pippenger [Pip96] and Asharov et al. [AKL+20a] have shown that if we use an appropriate family of bipartite expander graphs, the above algorithm indeed realizes loose compaction correctly. More concretely, using properties of the expander graph, it is shown that in each iteration, the number of unsatisfied factories is decreased by a factor of at least 2, and after $\log m$ iterations all factories are satisfied. We get the following proposition.

Proposition 4.11 (Pippenger [Pip96] and Asharov et al. [AKL+20a]). There exists an appropriate constant $\epsilon \in (0,1)$ and a bipartite expander graph family $\{G_{\epsilon,m}\}_{m \in \mathbb{N}}$ where each vertex has $d := d(\epsilon)$ edges for a constant $d$ that is dependent on $\epsilon$ and assumed to be a power of 2, such that for any $m$ and $n = md/2$, the above loose compaction algorithm, when instantiated with this family of bipartite expander graph, can correctly compress any input array of length $n$ to a half its original size without losing any real elements, as long as the input array has at most $n/128$ real elements.

It remains to show how to implement the above algorithm in the circuit model.

Implementing loose compaction (Algorithm 4.9) in circuit. We now consider how to implement the loose compaction algorithm (Algorithm 4.9) in circuit.

1. Step 1 can be accomplished with $O(n)$ generalized boolean gates due to Fact 4.3 and Fact 4.1.
Algorithm 4.9: Loose Compaction

- **Input:** An input array \( I \) of \( n \) elements, in which at most \( n/128 \) are real and the rest are dummies.
- **Assumption:** Without loss of generality, we may assume that \( d \) is a power of 2 and \( n \) is a multiple of \( d/2 \). Let \( m := n/(d/2) = 2n/d \).
- **The algorithm:**
  1. Divide \( I \) into \( m \) chunks of size \( d/2 \). If a chunk contains at most \( d/8 \) real elements (i.e., at most a quarter loaded), it is said to be sparse; otherwise it is said to be dense. It is not hard to see that the number of dense chunks must be at most \( m/32 \).
  2. Now imagine that each chunk is a vertex in \( L \) of \( G_{\epsilon,m} \), and \( D \subset L \) is a set of dense vertices (i.e., corresponding to the dense chunks). Let \( \text{edges}(D,R) \) denote all the edges in \( G_{\epsilon,m} \) between \( D \subset L \) and \( R \). We would like to find a subset of edges \( M \subseteq \text{edges}(D,R) \) such that each vertex \( u \in D \) has load \((u) \leq d/2 \) edges in \( M \) and every vertex \( R \) has at most \( d/8 \) incoming edges in \( M \), where load \((u) \) denotes the number of real elements in the chunk. Henceforth we call such an \( M \) a feasible route.
  
  To find a feasible route given the set \( D \), we rely on a subroutine called ProposeAcceptFinalize (see Algorithm 4.10).
  3. Now, every dense chunk \( u \in D \) does the following: for each out edge of \( u \) in \( M \), send one element over the edge to a corresponding neighbor in \( R \); for all out edges of \( u \) not in \( M \), send a dummy element on the edge. Clearly every vertex in \( R \) receives no more than \( d/8 \) real elements. Henceforth we may consider every vertex in \( R \) as a sparse chunk, i.e., an array of capacity \( d/2 \) but containing only \( d/8 \) real elements.
  4. At this moment, scan through the vertices in \( L \) and for each dense chunk encountered, replace the entire chunk with \( d/2 \) dummy elements.
  5. Now, all chunks in \( L \) and in \( R \) must be sparse. That is, each chunk contains at most \( d/8 \) real elements, while its size is \( d/2 \). We now compress each chunk in \( L \) and \( R \) to a quarter of its original size (i.e., to size \( d/8 \) in length), without losing any real elements in the process. Let \( O \) denote the compressed array, containing of \( 2m \cdot \frac{d}{8} = 2 \cdot \frac{2n}{d} \cdot \frac{d}{8} = n/2 \) elements.
- **Output:** The output array \( O \) of size \( n/2 \)

2. Step 2 is the invocation of ProposeAcceptFinalize algorithm (Algorithm 4.10) that finds a feasible route. We will show how to implement this algorithm in circuit below, using \( O(d \log d \cdot m \log m) \) generalized boolean gates, which is upper bounded by \( O(m \log m) \) assuming that \( d = O(1) \).

3. Recall that at the end of the ProposeAcceptFinalize subroutine, each factory has “written down” (i.e., these values were output by some gates in the circuit) the bit-vector \( \beta \in \{0,1\}^d \) indicating whether each of its incident edges should bear load (this is representation of \( M \) in circuit per node). Now, each factory, holding a \( d/2 \)-sized chunk, wants to “send” every real element in the chunk on one of its out edges marked as 1 by the bit-vector \( \beta \). To achieve this, we do the following per factory:
  - We label each real element in the \( d/2 \)-sized chunk with a number indicating how many real elements have appeared to its left, including itself. Every dummy element is labelled \( \perp \). Using Fact 4.4 this can be achieved in \( O(d \log d) \).
Algorithm 4.10: ProposeAcceptFinalize subroutine

Initially, each productive factory is unsatisfied and each unproductive factory is satisfied. For a productive factory \( u \in L \), we use notation \( \text{load}(u) \) to denote the number of products it has (corresponding to the number of real elements in the chunk).

Repeat the following for \( \log m \) times:

(a) \textit{Propose}: Each unsatisfied factory sends a proposal (i.e., the bit 1) to each one of its neighbors. Each satisfied factory sends 0 to each one of its neighbors.

(b) \textit{Accept}: If a facility \( v \in R \) received no more than \( d/8 \) proposals, it sends an acceptance message to each one of its \( d \) neighbors; otherwise, it sends a reject message along each of its \( d \) neighbors.

(c) \textit{Finalize}: Each currently unsatisfied factory \( u \in L \) checks if it received at least \( d^2/2 \) acceptance messages. If so, it picks an arbitrary subset of the edges over which acceptance messages were received, such that the subset is of size \( \text{load}(u) \). The factory records these edges which are also added to the feasible route \( M \). At this moment, this factory becomes satisfied.

- Similarly, we label each 1-position in \( \beta \) with a number indicating how many 1-bits have appeared to its left, including itself. Each 0-position in \( \beta \) is labelled with \( \bot_2 \neq \bot_1 \).

Using Fact 4.4 this can be achieved in \( O(d \log d) \).

- Now, each position in the vector \( \beta \) grabs an element from the chunk whose label is the same as itself, and if not found, the canonical outcome is dummy. This can be accomplished using Fact 4.5 for \( d \) times, resulting in \( O(d^2 \log d) \) generalized boolean gates and \( O(d^2) \) number of \( w \)-selector gates.

In total over all factories, we have \( O(m \cdot d^2 \log d) \) generalized boolean gates and \( O(m \cdot d^2) \) number of \( w \)-selector gates over all factories.

4. Step 4 can be implemented with \( m \) number of \( (wd/2) \)-selector gates, or alternatively \( md/2 \) number of \( w \)-selector gates.

5. Step 5 can be implemented with \( (d/8) \cdot (d/2) \) number of \( w \)-selector gates and \( (d/8) \cdot (d/2) \cdot \log d \) number of generalized boolean gates per chunk: basically imagine each input element is labeled with the number of real elements to its left including itself (within the chunk). Each of the \( d/8 \) output positions wants to find an input element whose label matches its own index.

We can implement the above using the prefix sum circuit of Fact 4.4 and \( d/8 \) copies of the find-in-array circuit of Fact 4.5.

Summing over all \( m \) chunks, Step 5 requires a total of \( m \cdot (d/8)(d/2) \cdot \log d \) generalized boolean gates and \( m \cdot (d/8)(d/2) \) number of \( w \)-selector gates.

Implementing \textit{ProposeAcceptFinalize} (Algorithm 4.10) as a circuit. Note that the circuit’s wiring structure can encode the expander graph \( G_{\epsilon,m} \) and sending messages over the edges of the graph is carried out by the circuit’s wiring, which feeds the outputs of circuit gadgets corresponding to factories (or facilities resp.) to the inputs of circuit gadgets corresponding to facilities (or factories resp.). Since there are \( \log m \) iterations, the expander graph is in fact encoded \( \log m \) times in the circuit’s wiring. More specifically, for each of the \( \log m \) iterations:

- Imagine that each facility has a circuit gadget that counts how many of its incoming wires have the bit 1, compares the outcome with \( d/8 \), and outputs an accept/reject decision. By
Fact 4.1 and Fact 4.3, this step can be implemented with $O(d)$ generalized boolean gates per facility and thus in total $O(dm)$ generalized boolean gates.

- Now each factory uses a circuit gadget that reads the accept/reject decisions on each of its $d$ incoming wires, tallies the total acceptance messages, compares the outcome to $d/2$, and then updates its satisfied/unsatisfied indicator. This step can be implemented with $O(dm)$ generalized boolean gates counting all factories by Fact 4.1 and Fact 4.3.

- We want that at the end of the ProposeAcceptFinalize algorithm, each factory writes down a bit-vector $\beta = \{0,1\}^d$ of length $d$ indicating whether each of its outgoing edge is chosen. To make this possible, each factory uses a circuit gadget to update its bit-vector $\beta \in \{0,1\}^d$ at the end of each iteration as follows: if the factory was unsatisfied before but became satisfied in this iteration (this can be determined by looking at the old value of the satisfied label and the new value, see Footnote 8), then update the bit-vector $\beta = \{0,1\}^d$, setting $\beta[i] = 1$ iff the $i$-th incoming wire has an acceptance decision and moreover the number of acceptance decisions until the $i$-th incoming wire is not more than the number of products it wants to route. This step can be accomplished with $O(d\log d)$ generalized boolean gates per factory due to Facts 4.1 and 4.4. Thus over all factories we have a total of $O(md\log d)$ generalized boolean gates.

Over all $\log m$ iterations, the total number of generalized boolean gates needed is $O(d\log d \cdot m\log m)$, which is upper bounded by $O(m\log m)$ assuming that $d = O(1)$.

Summarizing the above, we have the following fact:

**Corollary 4.12.** The above loose compaction algorithm can be implemented as a circuit with $O(n\log n)$ generalized boolean gates and $O(n)$ number of $w$-selector gates.

Theorem 4.8 now follows directly from Proposition 4.11 and Corollary 4.12.

### 4.4 Loose Swap

A loose swapper obtains an input array where each element is marked with $\perp$, blue, or red, and moreover the number of red elements is the same as the number of blue elements. Now, a loose swapper circuit swaps a subset of the blue elements with red ones and the swapped elements receive $\perp$. Henceforth we call elements marked red or blue colored and those marked $\perp$ uncolored.

Formally, an $(n,w)$-loose swapper solves the following problem:

- **Input:** an input array containing $n$ elements where each element contains a $w$-bit payload string and a two-bit metadata label whose value is chosen from the set $\{\text{blue}, \text{red}, \perp\}$. Henceforth we assume the first bit of the label encodes whether the element is colored or not, and the second bit of the label picks a color between blue and red if the element is indeed colored.

- **Output:** a legal swap of the input array such that at most $n/128$ elements remain colored, where the notion of a legal swap is defined below.

We say that an output array $O$ is a legal swap of the input array $I$ iff there exist pairs $(i_1, j_1), (i_2, j_2), \ldots, (i_\ell, j_\ell)$ of indices that are all distinct, such that for all $k \in [\ell]$, $I[i_k]$ and $I[j_k]$ are colored and have opposite colors, and moreover $O$ is obtained by swapping $I[i_1]$ with $I[j_1]$, swapping $I[i_2]$ with $I[j_2]$, ..., and swapping $I[i_\ell]$ with $I[j_\ell]$; further, all swapped elements become uncolored.

---

Note that when implemented in circuit, every update to a variable creates a new copy of the variable that is output by some gate(s). In other words a circuit can be thought of as a straightline program of a “single-assignment form” [RWZ88] where the names of wires are variable names in the program.
Theorem 4.13. There exists a circuit in the indivisible model with $O(n)$ generalized boolean gates and $O(n)$ number of \(w\)-selector gates that realizes an \((n, w)\)-loose swapper.

Proof. We will describe an algorithm first described by Pippenger [Pip96] and then re-explained by Asharov et al. [AKL+20]. The algorithm makes use of a suitable bipartite expander graph \(G_{\epsilon,n}\) where \(\epsilon \in (0, 1)\) is a suitable constant. The degree of each vertex in \(G_{\epsilon,n}\) is a constant \(d := d(\epsilon)\) that depends on \(\epsilon\). Henceforth let \(L\) denote the set of left-vertices in \(G_{\epsilon,n}\) and \(R\) denote the set of right vertices; and \(|L| = |R| = n\).

We will think of every element in the input array as a vertex in \(L\). During the algorithm, each vertex \(u_1 \in L\) performs the following actions acting in a sequential manner:

- For each vertex in \(u_2 \in L\) that is connected to \(u_1\) by a length-2 path, if \(u_1\) and \(u_2\) currently have opposite colors, then swap them and uncolor the two vertices.

Pippenger [Pip96] and Asharov et al. [AKL+20] show that there exists a suitable bipartite expander graph \(G_{\epsilon,n}\) with a constant spectral expansion \(\epsilon \in (0, 1)\), such that if the above algorithm is performed using the graph \(G_{\epsilon,n}\), it will correctly realize a loose swapper on \(n\) elements.

Note that every vertex in \(L\) has at most \(d^2\) two-hop neighbors in \(L\). Since the circuit’s wiring can encode the expander graph’s structure, it is not hard to see that we can implement the above algorithm in a circuit, incurring \(n \cdot d^2\) comparisons on 2-bit color labels, and \(2n \cdot d^2\) number of \(w\)-selector gates. \qed

5 Tight Compaction from Loose Compaction

In this section, we show how to construct a circuit for tight compaction from Loose Compaction and from a Swapper circuit. This corresponds to case (a) in Figure 1. We remark that we already saw a basic Loose Compaction circuit in Section 4.3, but in our final construction we will iteratively improve that circuit via bootstrapping and boosting.

Theorem 5.1. Suppose that there is a circuit with \(B_{lc}(n)\) generalized boolean gates and \(S_{lc}(n)\) \(w\)-selector gates that loosely compacts an input array containing \(n\) elements each of bit-width \(w\). Suppose also that there is a loose swapper circuit with \(B_{lsw}(n)\) generalized boolean gates and \(S_{lsw}(n)\) \(w\)-selector gates for an input array containing \(n\) element each of bit-width \(w\). Moreover, suppose that \(B_{lc}(n) \geq n\), \(S_{lc}(n) \geq n\), \(B_{lsw}(n) \geq n\), and \(S_{lsw}(n) \geq n\).

Then, tight compaction can be accomplished with a circuit with at most \(2S_{lsw}(n) + 2B_{lsw}(n) + 2B_{lc}(n) + 8S_{lc}(n) + 11n\) generalized boolean gates, and at most \(2S_{lsw}(n) + 4S_{lc}(n) + 2n\) number of \(w\)-selector gates.

The remainder of this section will be dedicated to proving this theorem.

5.1 From Loose to Tight Compaction Algorithm

Consider the following algorithm — below we first describe the high-level algorithm and then we will describe how to implement each step in circuit. Assume that in the input array \(I\) there are \(c\) distinguished elements. Thus, the distinguished elements should be placed in the first \(c\) elements in the output array. Moreover, all distinguished elements in the first \(c\) positions in the input array \(I\) are already in the “right place” and all non-distinguished elements in the last \(n - c\) positions of \(I\) are also in the right place and should not be moved. Moreover, there are exactly the same number of non-distinguished elements in the first \(c\) positions in \(I\) as the number of distinguished elements in the last \(n - c\) positions in \(I\). The tight compaction algorithm will simply swap them. In more detail, the algorithm works as follows:
1. **Count.** Compute the total number (denoted $c$) of distinguished elements (i.e., real elements) in the input array $I$.

2. **Color.** For any $i \leq c$, if $I[i]$ is not distinguished, mark the element red; for any $i > c$, if $I[i]$ is distinguished, mark the element blue; every other element is marked ⊥. Let the outcome be $X$.

Note that at this moment, each element is labeled with 3 bits of metadata, one bit of distinguished indicator and two bits of color-indicator (indicating whether the element is colored, and if so, which color).

3. **Swap.** Call an $(n, w+1)$-swapper (see Section 5.2) to swap each blue element with a red one (we use here payload of size $w+1$ and not $w$ as we also include the color-indicator as part of the payload). Specifically, an $(n, w+1)$-swapper is defined exactly like a loose swapper but with the requirement that the outcome array must have no colored elements remaining.

In the next couple of subsections we will focus on explaining how to realize each of the above steps in circuit. The most non-trivial step is the swapper which leverages a loose swapper and a loose compactor as a building block. Thus we will first describe the swapper circuit (Section 5.2) and then explain how to implement the remaining steps in circuit (Section 5.3).

### 5.2 Swapper Circuit

We now focus on how to realize an $(n, w)$-swapper in circuit. We first describe the algorithm in Algorithm 5.2 and then explain how to realize it as a circuit.

**Implementing Algorithm 5.2 in circuit.** This swapper is a recursive construction that is executed on arrays of length $n, n/2, n/4, \ldots$. For each length $n'$, we consume a loose compactor, a loose swapper, and a reverse-router (accompanying the loose compactor) for the size $n'$. Thus for each problem size $n' = n, n/2, n/4, \ldots$, we need

- $S_{\text{lw}}(n')$ number of $w$-selector gates and $B_{\text{lw}}(n')$ number of generalized boolean gates corresponding to Step 1;
- $2S_{\text{lc}}(n')$ number of $(w+1)$-selector gates (one for the forward direction and one for the reverse direction) and $B_{\text{lc}}(n')$ generalized boolean gates corresponding to Step 2; and
- $n'$ number of $w$-selector gates corresponding to Step 5.

Note that each $(w+1)$-selector gate can be realized with one $w$-selector gate that operates on the $w$-bit payload and one generalized boolean gate that computes on the extra metadata bit. Thus each problem size $n'$ can be implemented with $S_{\text{lw}}(n') + 2S_{\text{lc}}(n') + n'$ number of $w$-selector gates and $B_{\text{lw}}(n') + B_{\text{lc}}(n') + 2S_{\text{lc}}(n')$ generalized boolean gates.

Summing over all $n' = n, n/2, n/4, \ldots$, and recalling that $B_{\text{lc}}(n) \geq n, S_{\text{lc}}(n) \geq n, B_{\text{lw}}(n) \geq n$, and $S_{\text{lw}}(n) \geq n$, we have the follow fact:

**Fact 5.3.** In the swapper circuit shown above which operates on elements of bit-width $w$, the total number of $w$-selector gates needed is upper bounded by $2S_{\text{lw}}(n) + 4S_{\text{lc}}(n) + 2n$ and the total number of generalized boolean gates is upper bounded by $2B_{\text{lw}}(n) + 2B_{\text{lc}}(n) + 4S_{\text{lc}}(n)$.

### 5.3 Implementing the Remaining Steps in Circuit

We now describe how to implement the above algorithm with a circuit — without loss of generality, we may assume that $n$ is a power of 2:
Algorithm 5.2: Swap(X)

- **Input:** An array X of n elements, each has a $w$-bit payload and a 2-bit label indicating whether the element is colored, and if so, whether the element is blue or red.

- **The algorithm:**
  
  1. Call an $(n, w)$-loose swapper (see Section 4.4) on X to swap elements of opposite colors and uncolor them in the process, such that at most 1/128 fraction of resulting array remain colored.
     
     If $n \leq 128$, output the resulting array; else continue with the following steps.

  2. Call an $(n, w + 1)$-loose compactor (see Section 6) to compact the outcome of the previous step by a half, where the loose compactor treats the colored elements as real and the uncolored elements as dummy. In other words, the loose compactor treats the 1st bit of the color label as a dummy indicator, and treats the 2nd bit of the color label and an element’s payload string as the payload. Let the outcome be Y whose length is half of X.

  3. Recursively call Swap(Y), and let the outcome be $Y'$.

  4. Reverse the routing decisions made by all selector gates during Step 2 as below. For every selector gate $g$ in Step 2, its reverse selector gate denoted $g'$ is one that receives a single element as input and outputs two elements; the same control bit $b$ input to the original gate $g$ is used by $g'$ to select which of the output receives the input element, and the other one will simply receive the string $0^{w+1}$. If $g$ selected the first input element to route to the output, then in $g'$, the input element is routed to the first output.
     
     In this way, we can reverse-route elements in $Y'$ to an array (denoted $\tilde{X}$) of length $|X|$, i.e., twice the length of $Y'$.

  5. The output $Z$ is formed by a performing coordinate-wise select operation between $X$ and $\tilde{X}$:

     \[
     Z[i] = \begin{cases} 
     X[i] & \text{if } X[i] \text{ is uncolored} \\
     \tilde{X}[i] & \text{o.w.}
     \end{cases}
     \]

- **Output:** The array Z.

**Step 1: counting.** Due to Fact 4.3, the following is immediate:

**Fact 5.4.** Step 1 can be accomplished with $6n$ generalized boolean gates and no selector gate.

**Step 2: coloring.** When the outcome $c$ is computed from Step 1, we can implement Step 2 as follows. Recall that $c \in \{0, 1, \ldots, n\}$ is a $(\log_2 n)$-bit number. Imagine that there are $n$ receivers numbered 1, 2, $\ldots$, $n$. Each receiver is waiting to receive either “$\leq$” or “$>$”. Those with indices 1, $\ldots$, $c$ should receive “$\leq$” and those with indices $c + 1, \ldots, n$ should receive “$>$”. Using Fact 4.7, we convert $c$ into an $n$-bit string so that the head $c$ bits are 0 and the tail $n - c$ bits are 1. Such $n$ bits are passed to the $n$ receivers where 0 is interpreted as “$\leq$” and 1 is interpreted as “$>$”, and the above can be implemented as a circuit consisting of at most $2n$ generalized boolean gates. Once each of the $n$ receivers receive either “$\leq$” or “$>$”, it takes a single generalized boolean gate per receiver (with fan-in 2 and fan-out 2) to write down either blue, red, or $\bot$.

Therefore, the total number of generalized boolean gates needed for this step is upper bounded by $3n$; and no selector gates are needed here.

**Fact 5.5.** Step 2 can be accomplished with $3n$ generalized boolean gates and no selector gate.
5.4 Putting it Together

Summarizing Facts 5.3, 5.4 and 5.5, for the entire tight compaction algorithm of Section 5.1, we need at most $2B_{ls}(n) + 2B_{tc}(n) + 4S_{tc}(n) + 9n$ generalized boolean gates, and at most $2S_{ls}(n) + 4S_{tc}(n) + 2n$ number of $(w+1)$-selector gates. Since each $(w+1)$-selector gate can be replaced with one $w$-selector gate and one generalized boolean gate, alternatively we can realize tight compaction in circuit with at most $2S_{ls}(n) + 2B_{ls}(n) + 2B_{tc}(n) + 8S_{tc}(n) + 11n$ generalized boolean gates, and at most $2S_{ls}(n) + 4S_{tc}(n) + 2n$ number of $w$-selector gates which gives rise to the statement in Theorem 5.1.

6 Loose Compaction from Tight Compaction

In this section, we show how to construct a circuit for loose compaction from tight compaction. This corresponds to case (b) in Figure 1.

**Theorem 6.1.** Let $f(n)$ be some function in $n$ such that $1 < f(n) \leq \log_2 n$ holds for every $n \geq 32$; let $C_{tc} > 1$ be a constant. Suppose that $(n,w)$-tight compaction can be solved by a circuit with $C_{tc} \cdot n \cdot f(n)$ generalized boolean gates and $C_{tc} \cdot n$ selector gates for any $n \geq 256$, then loose compaction can be solved by a circuit with $2.07C_{tc} \cdot n \cdot f(f(n)) + 7n$ boolean gates and $2.07C_{tc} \cdot n$ selector gates for any $n \geq 256$.

The remainder of this section will be dedicated to proving the above theorem.

6.1 Loose Compaction Algorithm

For simplicity, we first consider the case when $n$ is divisible by $f(n)$. Looking ahead, we will use $f(n)$ to be $\log^{(x)} n$ for some $x$ that is power of 2. We will later extend our theorem statement to the case when $n$ is not divisible by $f(n)$. Consider the following algorithm:

**Algorithm 6.2:** LooseCompactionfromTightCompaction

1. Divide the input array into $f(n)$-sized chunks. We say that a chunk is sparse if there are at most $f(n)/32$ real elements in it; otherwise it is called dense. Now, count the number of elements in every chunk, and mark each chunk as either sparse or dense.
2. Call an $(n/f(n), w \cdot f(n))$-tight compactor to move the dense chunks to the front and the sparse chunks to the end.
3. We will show later in Fact 6.3 that at least $3/4$ fraction of the chunks are sparse. Now, apply a $(f(n), w)$-tight compactor to the trailing $\left\lceil \frac{3}{4} \cdot \frac{n}{f(n)} \right\rceil$ chunks to compress each of these chunks to a length of $\left\lfloor \frac{f(n)}{32} \right\rfloor$ without losing any elements in the process. The first $\frac{1}{4} \cdot \frac{n}{f(n)}$ chunks are unchanged. Output the resulting array.

At the end of the algorithm, the output array has length at most

$$
\frac{3}{4} \cdot \frac{n}{f(n)} \cdot \frac{f(n)}{32} + \frac{1}{4} \cdot \frac{n}{f(n)} \cdot f(n) \leq 0.28n < 0.5n
$$

(1)

**Fact 6.3.** At least $\frac{3}{4} \cdot \frac{n}{f(n)}$ chunks are sparse.

**Proof.** Suppose not, this means that more than $\frac{1}{4} \cdot \frac{n}{f(n)}$ have more than $f(n)/32$ real elements. Thus the total number of elements is more than $n/128$ which contradicts the input sparsity assumption of loose compaction.

□
6.2 Implementing Algorithm 6.2 in Circuit

We now analyze the circuit size of the algorithm in Section 6.1. For simplicity, we first assume that \( n \) is divisible by \( f(n) \) and we will later modify our analysis to the more general case when \( n \) is not divisible by \( f(n) \).

1. Step 1 of the algorithm requires at most \( 6n \) generalized boolean gates as we have \( n/f(n) \) counters of chunks of size \( f(n) \) each. Due to Fact 5.4, each counter requires at most \( 6f(n) \) generalize boolean gates.

2. Step 2 is a single invocation of a \( (n/f(n), w \cdot f(n)) \)-tight compactor. Assuming that \( (n, w) \)-tight compactor can be realized with \( C_{tc} \cdot n \cdot f(n) \) generalized boolean gates and \( C_{tc} \cdot n \) selector gates, this step requires at most \( C_{tc} \cdot (n/f(n)) \cdot f(n/f(n)) \leq C_{tc} \cdot (n/f(n)) \cdot f(n) \) generalized boolean gates and \( C_{tc} \cdot n/f(n) \) number of \( w \cdot f(n) \)-selector gates. Each such selector gate can in turn be realized with \( f(n) \) number of \( w \)-selector gates. Thus, in total, Step 2 requires \( C_{tc} \cdot n \) generalized boolean gates and \( C_{tc} \cdot n \) number of \( w \)-selector gates.

3. Step 3 of the algorithm requires applying \( \left\lceil \frac{3}{4} \cdot \frac{n}{f(n)} \right\rceil \) number of \( (f(n), w) \)-tight compactors, where, according to our assumption in Theorem 6.1, each such tight compactor consumes \( C_{tc} \cdot f(n) \cdot f(f(n)) \) generalized boolean gates and \( C_{tc} \cdot f(n) \) number of \( w \)-selector gates. For \( n \geq 32 \) and \( f(n) \leq \log_2 n \leq n/4 \), we have that

\[
\left\lceil \frac{3}{4} \cdot \frac{n}{f(n)} \right\rceil \cdot f(n) \leq \left( \frac{3}{4} \cdot \frac{n}{f(n)} + 1 \right) \cdot f(n) \leq 3n/4 + n/4 \leq n
\]

Therefore, in total there are at most \( C_{tc} \cdot n \cdot f(f(n)) \) generalized boolean gates and \( C_{tc} \cdot n \) number of \( w \)-selector gates.

**Fact 6.4.** Assume the same assumptions as in Theorem 6.1, and moreover \( n \) is divisible by \( f(n) \). The loose compaction algorithm in Section 6.1 can be realized with a circuit consisting of \( C_{tc} \cdot n \cdot (f(f(n)) + 1) + 6n \) generalized boolean gates and \( 2C_{tc} \cdot n \) number of \( w \)-selector gates.

When \( n \) is not divisible by \( f(n) \). When \( n \) is not divisible by \( f(n) \), we can pad the last chunk with dummy elements to a length of \( f(n) \). After the padding the total number of elements is upper bounded by \( n + f(n) \). This gives rise to the following fact.

**Fact 6.5.** Assume the same assumptions as in Theorem 6.1. Then, the loose compaction algorithm in Section 6.1 can be realized with a circuit consisting of \( 2.07C_{tc} \cdot n \cdot f(f(n)) + 7n \) generalized boolean gates and \( 2.07C_{tc} \cdot n \) number of \( w \)-selector gates.

**Proof.** Recall that we padded the input array with dummy elements to a length that is a multiple of \( f(n) \). The number of padded elements is at most \( f(n) \). We first check that Equation 1 still holds, i.e., the algorithm compresses the input array by at least a half. Note that the input padded array still satisfies the 1/128 input sparsity assumption. The output array now has length upper bounded by

\[
\frac{3}{4} \cdot \frac{n + f(n)}{f(n)} \cdot f(f(n)) \cdot \frac{1}{32} + \frac{1}{4} \cdot \frac{n + f(n)}{f(n)} \cdot f(n) \leq 0.28(n + f(n)) < 0.5n
\]

Note that the last inequality above holds because \( n \) is sufficiently large.

Now, repeating the analysis above in Section 6.2, we can show that Algorithm 6.2 can be realized with a circuit consisting of \( C_{tc} \cdot (n + f(n)) \cdot (f(f(n)) + 1) + 6(n + f(n)) \) generalized boolean
gates and $2C_{tc} \cdot (n + f(n))$ number of $w$-selector gates. To obtain the expression in the above fact, it suffices to observe that for $n \geq 256$ and $f(n) \leq \log_2 n$, it holds that

$$\frac{f(f(n)) + 1}{f(f(n))} \leq \frac{4}{3}, \quad \frac{n + f(n)}{n} \leq \frac{33}{32}.$$ 

\[ \square \]

### 7 Linear-Sized Tight Compaction Circuit

In this section, we shall prove the following theorem. We will tighten the constant-degree of the poly to $2 + \epsilon$ in Appendix B.

**Theorem 7.1** (Linear-sized tight compaction). There exists a constant fan-in, constant fan-out boolean circuit that solves $(n, w)$-tight compaction and the total number of boolean gates is upper bounded by

$$O(n \cdot w) \cdot \min (\max (1, \text{poly}(\log^* n - \log^* w)), 2^w / w).$$

As a direct corollary, for any arbitrarily large constant $c \geq 1$, if $w \geq \log^c n$, it holds that the circuit’s size is upper bounded by $O(nw)$.

The case when $w > \log n$ is easy (see Footnote 10), so in the remainder of this section, unless otherwise noted, we shall assume that $w \leq \log n$. In this section, we prove only that the number of total boolean gates is upper bounded by $\text{poly}(\log^* n - \log^* w) \cdot O(n \cdot w)$. We refer the reader to Appendix A for the second part, which dominants when $w$ is tiny. In Appendix B we tighten the constant-degree of the poly.

#### 7.1 Notations and Parameter Choices

In Theorem 4.13, we showed the existence of a $(n, w)$-loose swapper that works in $O(n)$ generalized boolean gates and $O(n)$ $w$-selector gates. Henceforth we write $O_1(n) = cn$ and $O_2(n) = c'n$ where $c$ and $c'$ are universal constants. Specifically, let

$$4B_{lsw}(n) + 11n \leq O_1(n) = cn, \quad 2S_{lsw}(n) + 2n \leq O_2(n) = c'n$$

where $B_{lsw}(n)$ and $S_{lsw}(n)$ are linear functions in $n$ by Theorem 4.13. Thus, we have the following circuit:

**LC**$_0$: By Theorem 4.8, there exists a constant $C > 1$ such that we can solve $(n, w)$-loose compactor with

- generalized boolean gates: $Cn \log n$
- selector gates: $Cn$

Without loss of generality, we may assume that the constant $C$ is sufficiently large such that the following expressions hold:

$$7n \leq 0.03 \cdot 4.1Cn, \quad O_2(n) \leq 0.1Cn$$

(2)
**Additional notations.** Recall that log means log\textsubscript{2}. We will choose the depth of the recursion \(d\) to be the smallest positive integer such that \(\log(2^{d-1}) n \leq w\). Without loss of generality, we may redefine \(\log n := \max(w, \log n)\) — due to the choice of \(d\), essentially for the last recursion level, if \(\log(2^{d-1}) n < w\), we will round it up to \(w\); moreover, this rounding is only performed for the last level of recursion and no other level. Therefore, we may assume that

\[
\log(2^{d-1}) n = w
\] (3)

Without loss of generality, we may assume that the bit-length of an element \(w\) is lower bounded by a sufficiently large constant, such that the following expressions are satisfied:

\[
w \geq \frac{8Cn + O_1(n)}{2.1Cn}, \quad w \geq 256
\] (4)

### 7.2 Construction through Repeated Bootstrapping and Boosting

We will construct tight compaction through repeated bootstrapping and boosting. Without loss of generality, we may assume that \(n \geq 256\). We have two steps:

- **LC\(_i\) \implies TC\(_{i+1}\) (Theorem 5.1):** from loose compactor to tight compactor. Simplifying Theorem 5.1 and using the above notations, we get the following:
  
  Assuming \((n, w)\)-loose compactor with:
  
  \[
  \# \text{generalized boolean gates} : B_{lc}(n) \\
  \# \text{selector gates} : S_{lc}(n)
  \]

  Then, there exists \((n, w)\)-tight compactor with:
  
  \[
  \# \text{generalized boolean gates} : 2B_{lc}(n) + 8S_{lc}(n) + O_1(n) \\
  \# \text{selector gates} : 4S_{lc}(n) + O_2(n)
  \]

- **TC\(_{i+1}\) \implies LC\(_{i+1}\) (Theorem 6.1):** from tight compaction to loose compactor. Simplifying Theorem 6.1 we have:
  
  Assuming \((n, w)\)-tight compactor with some constant \(C_{tc}\) and function \(f(n)\) such that:
  
  \[
  \# \text{generalized boolean gates} : C_{tc} \cdot n \cdot f(n) \\
  \# \text{selector gates} : C_{tc} \cdot n
  \]

  Then there exists a \((n, w)\)-loose compactor such that:
  
  \[
  \# \text{generalized boolean gates} : 2.07 \cdot C_{tc} \cdot n \cdot f(f(n)) \\
  \# \text{selector gates} : 2.07 \cdot C_{tc} \cdot n
  \]

Our starting point is Theorem 4.8, which as we have already seen, it gives as the circuit \(LC_0\). Using the above two steps, we bootstrap and boost the circuit:

**LC\(_0\):** By Theorem 4.8, there exists a constant \(C > 1\) such that we can solve \((n, w)\)-loose compactor with

\[
\begin{align*}
\text{generalized boolean gates} : Cn \log n \\
\text{selector gates} : Cn
\end{align*}
\]
**TC**\(_1\): By Theorem 5.1, we can construct a tight compaction circuit **TC**\(_1\) from **LC**\(_0\). **TC**\(_1\)’s size is upper bounded by the expressions\(^{10}\):

- generalized boolean gates: \(2Cn \log n + 8Cn + O_1(n) \leq 4.1Cn \log n\)
- selector gates: \(4Cn + O_2(n) \leq 4.1Cn\)

In the above, the first the inequality holds due to Equations (3) and (4) as \(8Cn + O_1(n) \leq 2.1Cnw\) and \(w \leq \log n\). The second inequality holds due to Equation (2).

**LC**\(_1\): Using the algorithm in Section 6.1, we build a loose compaction circuit **LC**\(_1\) from **TC**\(_1\). **LC**\(_1\)’s size is upper bounded by the expressions:

- generalized boolean gates: \(2.07 \cdot 4.1Cn \log \log n + 7n \leq 2.1 \cdot 4.1Cn \log \log n\)
- selector gates: \(2.07 \cdot 4.1Cn \leq 2.1 \cdot 4.1Cn\)

In the above, the first inequality holds due to Equation (2).

**TC**\(_2\): Using the algorithm in Section 5.1, we can construct a tight compaction circuit **TC**\(_2\) from **LC**\(_1\). **TC**\(_2\)’s size is upper bounded by the expressions:

- generalized boolean gates: \(2 \cdot 2.1 \cdot 4.1Cn \log \log n + 8 \cdot 2.1 \cdot 4.1Cn + O_1(n) \leq 2.1 \cdot (4.1)^2Cn \log \log n\)
- selector gates: \(4 \cdot 2.1 \cdot 4.1Cn + O_2(n) \leq 2.1 \cdot (4.1)^2Cn\)

In the above, the first the inequality holds due to Equations (3) and (4) as \(8Cn + O_1(n) \leq 2.1Cn \log \log n\). The second inequality holds due to Equation (2).

**LC**\(_2\): Using the algorithm in Section 6.1, we build a loose compaction circuit **LC**\(_2\) from **TC**\(_2\). **LC**\(_2\)’s size is upper bounded by the expressions:

- generalized boolean gates: \(2.07 \cdot 2.1 \cdot (4.1)^2Cn \log(4) n + 7n \leq (2.1 \cdot 4.1)^2Cn \log(4) n\)
- selector gates: \(2.07 \cdot 2.1 \cdot (4.1)^2Cn \leq (2.1 \cdot 4.1)^2Cn\)

Continuing with the iterations for \(d\) iterations, we get:

**LC**\(_{d-1}\): Using Theorem 6.1, we build a loose compaction circuit **LC**\(_{d-1}\) from **TC**\(_{d-1}\). **LC**\(_{d-1}\)’s size is upper bounded by the expressions:

- generalized boolean gates: \((2.1 \cdot 4.1)^{d-1}Cn \log(2^{d-1}) n\)
- selector gates: \((2.1 \cdot 4.1)^{d-1}Cn\)

**TC**\(_d\): Using Theorem 5.1 we can construct a tight compaction circuit **TC**\(_d\) from **LC**\(_{d-1}\). **TC**\(_d\)’s size is upper bounded by the expressions:

- generalized boolean gates: \((2.1)^{d-1} \cdot (4.1)^dCn \log(2^{d-1}) n\)
- selector gates: \((2.1)^{d-1} \cdot (4.1)^dCn\)

\(^{10}\) When \(w > \log n\), **TC**\(_1\) gives Theorem 7.1. Therefore, the rest of this section assumes \(w \leq \log n\).
By definition, \( d - 1 = \lceil \log(\log^* n - \log^* w) \rceil \leq \log(\log^* n - \log^* w) + 1 \). Therefore, the final tight compaction circuit \( \text{TC}_d \)'s size is upper bounded by the following:

\[
\text{# generalized boolean gates:} \leq O(1) \cdot (2.1 \cdot 4.1)^{\log(\log^* n - \log^* w) + 1} \cdot n \cdot w
\]

\[
= O(1) \cdot \text{poly}(\log^* n - \log^* w) \cdot n \cdot w
\]

\[
\text{# selector gates:} \leq O(1) \cdot (2.1 \cdot 4.1)^{\log(\log^* n - \log^* w) + 1} \cdot n
\]

\[
= O(1) \cdot \text{poly}(\log^* n - \log^* w) \cdot n
\]

This gives rise to Theorem 7.1. For the case of a tiny \( w \) we can upper bound the size of the circuit by \( 2^w/w \), as we show in Appendix A.

8 Linear-Sized Selection Circuit

We care about selecting all \( m \) smallest elements from an input array, using a linear-sized circuit. Given our tight compaction circuit, it suffices to select only the \( m \)-th smallest element \( x \) since after that, we can use tight compaction to move all elements smaller than or equal to \( x \) to the left. To select the \( m \)-th smallest element with a linear-sized circuit, it suffices to combine our linear-sized tight compaction circuit with the classical, textbook median-of-median algorithm \([BFP+72]\). Essentially, the step in which the median-of-median algorithm partitions elements according to a pivot will be replaced with our tight compaction circuit. The algorithm is described in Algorithm 8.1.

**Algorithm 8.1: Select(\( A, m \))**

1. Let \( n := |A| \). If \( n \leq 100 \), use the AKS sorting network to sort the input array and output its \( m \)-th element; else continue with the following steps.
2. Divide the elements into \( \lceil n/5 \rceil \) groups each of size 5. If \( n \) is not divisible by 5, the last group may have fewer than 5 elements.
3. Compute the median of each group. Note that this can be accomplished with an \( O(w) \)-sized circuit where \( w \) is the bit-width of each element. Let \( M \) be the array of \( \lceil n/5 \rceil \) medians.
4. Recursively call \( \text{Select}(M, 1/2 \cdot |M|) \) to compute the median of the median, and let \( m^* \) be the outcome.
5. Mark each element with 0 if it is smaller than \( m^* \) and 1 otherwise. Use a compaction circuit to move all the elements marked with 0 to the left, and those marked with 1 to the right. Let \( X \) be the resulting array.
6. Let \( n' = \lceil 7n/10 + 3 \rceil \); let \( c_{\text{small}} \) be the number of elements strictly smaller than \( m^* \) and let \( c_{\text{big}} \) be the number of elements strictly greater than \( m^* \) — note that \( c_{\text{small}} \) and \( c_{\text{big}} \) can be computed in an \( O(n) \)-sized circuit.
7. Depending on \( m \), recursively call \( \text{Select} \) on an array of size \( n' \) as follows:
   - if \( m \leq c_{\text{small}} \), recursively call \( \text{Select}(X[1 : n'], m) \) and output its outcome;
   - else if \( m \geq n - c_{\text{big}} + 1 \), recursively call \( \text{Select}(X[n - n' + 1 : n], m - n + n') \) and output its outcome;
   - else recursively call \( \text{Select}(X[1 : n'], m) \) and output \( m^* \).

(To implement the above as a circuit, first use a selector gate that selects between \( X[1 : n'] \) and \( X[n - n' + 1 : n] \), and then run \( \text{Select} \) recursively on the outcome.)
For correctness, observe that during each iteration in the above recursive construction, there are at least \(\lceil n/10 \rceil - 1 \cdot 3\) elements smaller than or equal to \(m^*\); similarly, there are at least \(\lceil n/10 \rceil - 1 \cdot 3\) elements greater than or equal to \(m^*\).

The circuit size for the above construction, denoted \(C(n)\), satisfies the following recurrence:

for \(n > 100\): \(C(n) \leq C(\lfloor n/5 \rfloor) + C(\lceil 7n/10 + 3 \rceil) + O(nw) \cdot \min(\text{poly}(\log^* n - \log^* w), \ 2^w/w)\)

for \(n \leq 100\): \(C(n) \leq C_0\) for an appropriate constant \(C_0\)

This recurrence solves to \(C(n) = O(nw) \cdot \min(\max(1, \text{poly}(\log^* n - \log^* w)), \ 2^w/w)\).

Finally, to select not just the \(m\)-th smallest element but all \(m\) smallest elements, one can select the \(m\)-th smallest element denoted \(m^*\) first and then rely on a compaction circuit to move all elements smaller than or equal to \(m^*\) to the left, and all other elements to the right. Summarizing the above, we have the following corollary:

**Corollary 8.2.** There exists a circuit that can select the \(m\)-th smallest element or all \(m\) smallest elements from an input array containing \(n\) elements each of bit-width \(w\), and moreover its size is upper bounded by

\[O(nw) \cdot \min(\max(1, \text{poly}(\log^* n - \log^* w)), \ 2^w/w)\]

As a direct corollary, if \(w \geq \log^c n\) for any arbitrarily large constant \(c \geq 1\) or if \(w = O(1)\), then the circuit size is upper bounded by \(O(nw)\).

As we show in Appendix B, the constant-degree of the \(\text{poly}\) can be as small as \(2 + \epsilon\) for an arbitrarily small constant \(\epsilon > 0\).

## 9 Sorting Elements with Small Keys

Compaction is a sort with 1-bit keys. In this section we show how to sort \(w\)-bits elements with keys of some range \([a + 1, a + K]\) for some constants \(a\) and \(K\). We let \(k = \log K\) and \(W = w + k\) be the size of each element, where \(w\) is the payload and \(k\) is the size of the key. Our circuit has size of \((w + k) \cdot O(nk) \cdot h(n, w + k)\), where \(h(x, y) := \max(1, \text{poly}(\log^* x - \log^* y))\) for short.

For correctness, we claim that after performing the partitioning, the following hold: Either the top half or the bottom half can still have \(K\) distinct keys remaining but not both; Moreover, one of the halves must have no more than \(\lceil K/2 \rceil\) distinct keys remaining. This is true as one of the halves will have some \(1 \leq x \leq K\) distinct keys, and so the other half would have \(K + 1 - x\) distinct keys.

As for the running time, in each iteration we run \textbf{Select} and then tight compaction, and then selectors. Moreover, we have two recursive calls on the two halves of the array. We get:

\[T(n, K) = T(\left\lfloor \frac{n}{2} \right\rfloor, K) + T(\left\lceil \frac{n}{2} \right\rceil, K/2) + h(n, w + k) \cdot O(n(w + k))\]

Moreover, we have the following base cases:

For \(n \in O(1)\) : \(T(n, K) \in O(w + k)\)

For \(K \leq 2\) : \(T(n, K) \in h(n, w + k) \cdot O(n \cdot (w + k))\)

It is not hard to see that this recursion results in \(T(n, K) \in O(n(w + k) \cdot k \cdot h(n, w + k))\). Henceforth, we change the \(\text{poly}(x)\) in \(h\) with \(x^{2 + \epsilon}\) as in Appendix B. For summary, we have:
There exists a circuit that can sort an array of elements.

**Corollary 9.2.** There exists a circuit that can sort an array of \( n \) elements of bit-width \( w \), each element is marked with a key in \([a+1, a+K]\), and moreover its size is upper bounded by

\[
O((w + k) \cdot nk) \cdot \max(1, (\log^* n - \log^*(w + k))^{2+\epsilon})
\]

where \( k = \log K \) for an arbitrary small constant \( \epsilon > 0 \). As a direct corollary, if \( w + k \geq \log^c n \) for any arbitrarily large constant \( c \geq 1 \), then the circuit size is upper bounded by \((w + k) \cdot O(nk)\).

**Proof.** Let \( h(x, y) := \max(1, (\log^* x - \log^* y)^{2+\epsilon}) \). We show that \( T(n, K) \leq C \cdot n(w+k) \cdot k \cdot h(n, w+k) \) for some constant \( C \). We prove this claim by induction, while the constant \( C \) is the max between the two base cases \((n \in O(1) \text{ and } K \leq 2)\), and the inductive step. Assume that the induction holds to some constant \( C \) for every \( n' < n \), we want to show that \( T(n', K) \leq C \cdot n'(w+k) \cdot k \cdot h(n', w+k) \). We want to prove that this holds also for \( n' = n \). We have

\[
T(n, K) = T\left(\frac{n}{2}, K\right) + T\left(\frac{n}{2}, K/2\right) + n \cdot (w + k) \cdot h(n, w+k)
\]

\[
\leq C \cdot \frac{n}{2} \cdot (w + k) \cdot k \cdot h\left(\frac{n}{2}, w + k\right) + C \cdot \frac{n}{2} \cdot (w + k) \cdot (k - 1) \cdot h\left(\frac{n}{2}, w + k - 1\right) + n \cdot (w + k) \cdot h(n, w+k)
\]
Thus,

\[ T(n, K) \leq C \cdot n \cdot (w + k) \cdot k \cdot h(n, w + k) - \frac{1}{2} C \cdot n \cdot (w + k) \cdot h(\frac{n}{2}, w + k - 1) + n \cdot (w + k) \cdot h(n, w + k) \]

If \( w + k > \log n \), we have \( h(n, w + k) = 1 \), the induction holds directly. Otherwise, letting \( X = \log^* n - \log^*(w + k) \), it holds that

\[ \log^* \frac{n}{2} - \log^*(w + k - 1) \leq (X - 1). \]

Then, the inductive step holds if

\[ \frac{1}{2} C \cdot n \cdot (w + k) \cdot (X - 1)^{2+\epsilon} \geq n \cdot (w + k) \cdot X^{2+\epsilon}, \]

which holds for every \( C \geq 12 \) and \( n \geq 2^4 \).

## 10 Lower Bound

Lin, Shi, and Xie [LSX19] showed that any circuit in the indivisible model that sorts \( n \) elements each with a \( k \)-bit key must have at least \( \Omega(nk) \) selector gates. Recall that a circuit in the indivisible model considers the elements’ payloads as opaque; such a circuit only moves the payloads around using selector gates but does not perform any boolean computation on the payloads. Note that our upper bound is indeed in the indivisible model. In this section, we show that a similar lower bound holds even without restricting the circuit to satisfy the indivisibility assumption, assuming that a famous network coding conjecture to be true [LL04]. Although our proof techniques are inspired the recent works of Farhadi et al. [FIHLS19] and Afshani et al. [AFKL19], we need additional non-trivial modifications to make the techniques work in our context.

### 10.1 Preliminaries: The Li-Li Network Coding Conjecture

Our lower bound is conditional and relies on the famous Li-Li network coding conjecture [LL04] being true. Despite the centrality of this conjecture, it has so forth resisted all attempts at either proving or refuting it. To state the conjecture formally, we give a formal definition of the \( k \)-pairs communication problem and the Multicommodity Flow problem. We adopt a similar exposition as in earlier works [FIHLS19, AFKL19].

**\( k \)-pairs Communication Problem.** To keep the definition as simple as possible, we restrict ourselves to directed acyclic communication networks/graphs and we assume that the demand between every source-sink pair is the same. This will be sufficient for our proofs. For a more general definition, we refer the reader to Adler et al. [AHJ+06].

The input to the \( k \)-pairs communication problem is a directed acyclic graph \( G = (V, E) \) where each edge \( e \in E \) has a capacity \( c(e) \in \mathbb{R}^+ \). There are \( k \) sources \( s_1, \ldots, s_k \in V \) and \( k \) sinks \( t_1, \ldots, t_k \in V \). Typically there is also a demand \( d_i \) between each source-sink pair, but for simplicity we assume \( d_i = 1 \) for all pairs. This is again sufficient for our purposes.

Each source \( s_i \) receives a message \( A_i \) from a predefined set of messages \( A(i) \). It will be convenient to think of this message as arriving on an in-edge. Hence we add an extra node \( S_i \) for each source, which has a single out-edge to \( s_i \). The edge has infinite capacity.
A network coding solution specifies for each edge \( e \in E \) an alphabet \( \Gamma(e) \) representing the set of possible messages that can be sent along the edge. For a node \( u \in V \), define \( \text{In}(u) \) as the set of in-edges at \( u \). A network coding solution also specifies, for each edge \( e = (u, v) \in E \), a function \( f_e : \prod_{e' \in \text{In}(u)} \Gamma(e') \rightarrow \Gamma(e) \) which determines the message to be sent along the edge \( e \) as a function of all incoming messages at node \( u \). Finally, a network coding solution specifies for each sink \( t_i \) a decoding function \( \sigma_i : \prod_{e \in \text{In}(t_i)} \Gamma(e) \rightarrow M(i) \). The network coding solution is correct if, for all inputs \( A_1, \ldots, A_k \in \prod_i A(i) \), it holds that \( \sigma_i \) applied to the incoming messages at \( t_i \) equals \( A_i \), i.e. each source must receive the intended message.

In an execution of a network coding solution, each of the extra nodes \( S_i \) starts by transmitting the message \( A_i \) to \( s_i \) along the edge \((S_i, s_i)\). Then, whenever a node \( u \) has received a message \( a_e \) along all incoming edges \( e = (v, u) \), it evaluates \( f_e(\prod_{e' \in \text{In}(u)} a_{e'}) \) on all out-edges \( e' = (u, w) \in E \) and forwards the message along the edge \( e' \).

Following Adler et al. [AHJ+06] (and simplified a bit), we define the rate of a network coding solution as follows: Let each source receive a uniform random and independently chosen message \( A_i \) from \( A(i) \). For each edge \( e \), let \( A_e \) denote the random variable giving the message sent on the edge \( e \) when executing the network coding solution with the given inputs. The network coding solution achieves rate \( r \) if:

- \( H(A_i) \geq r d_i = r \) for all \( i \).
- For each edge \( e \in E \), we have \( H(A_e) \leq c(e) \).

Here \( H(\cdot) \) denotes binary Shannon entropy. The intuition is that the rate is \( r \), if the solution can handle upscaling the entropy of all messages by a factor \( r \) compared to the demands.

**Multicommodity Flow.** A multicommodity flow problem in an undirected graph \( G = (V, E) \) is specified by a set of \( k \) source-sink pairs \((s_i, t_i)\) of nodes in \( G \). We say that \( s_i \) is the source of commodity \( i \) and \( t_i \) is the sink of commodity \( i \). Each edge \( e \in E \) has an associated capacity \( c(e) \in \mathbb{R}^+ \). In addition, there is a demand \( d_i \) between every source-sink pair. For simplicity, we assume \( d_i = 1 \) for all \( i \) as this is sufficient for our needs.

A (fractional) solution to the multicommodity flow problem specifies for each pair of nodes \((u, v)\) and commodity \( i \), a flow \( f_i(u, v) \in [0, 1] \). Intuitively, \( f_i(u, v) \) specifies how much of commodity \( i \) is to be sent from \( u \) to \( v \). The flow satisfies flow conservation, meaning that:

- For all nodes \( u \) that is not a source or sink, we have \( \sum_{w \in V} f_i(u, w) - \sum_{w \in V} f_i(w, u) = 0 \).
- For all sources \( s_i \), we have \( \sum_{w \in V} f_i(s_i, w) - \sum_{w \in V} f_i(w, s_i) = 1 \).
- For all sinks we have \( \sum_{w \in V} f_i(w, t_i) - \sum_{w \in V} f_i(t_i, w) = 1 \).

The flow also satisfies that for any pair of nodes \((u, v)\) and commodity \( i \), there is only flow in one direction, i.e. either \( f_i(u, v) = 0 \) or \( f_i(v, u) = 0 \). Furthermore, if \((u, v)\) is not an edge in \( E \), then \( f_i(u, v) = f_i(v, u) = 0 \). A solution to the multicommodity flow problem achieves a rate of \( r \) if:

- For all edges \( e = (u, v) \in E \), we have \( r \cdot \sum_i d_i(f_i(u, v) + f_i(v, u)) = r \cdot \sum_i(f_i(u, v) + f_i(v, u)) \leq c(e) \).

Intuitively, the rate is \( r \) if we can upscale the demands by a factor \( r \) without violating the capacity constraints.
**The Undirected k-pairs Conjecture.** The undirected k-pairs conjecture [LL04] is stated below:

**Conjecture 10.1** (Undirected k-pairs Conjecture [LL04]). The coding rate is equal to the Multi-commodity Flow rate in undirected graphs.

This conjecture implies the following for our setting: Given an input to the k-pairs communication problem, specified by a directed acyclic graph $G$ with edge capacities and a set of $k$ source-sink pairs with a demand of 1 for every pair, let $r$ be the best achievable network coding rate for $G$. Similarly, let $G'$ denote the undirected graph resulting from making each directed edge in $G$ undirected (and keeping the capacities, source-sink pairs and a demand of 1 between every pair). Let $r'$ be the best achievable flow rate in $G'$. Conjecture 10.1 implies that $r \leq r'$.

Having defined coding rate and flow rate formally, we also mention that the result of Braverman et al. [BGS17] implies that if there exists a graph $G$ where the network coding rate $r$, and the flow rate $r'$ in the corresponding undirected graph $G'$, satisfies $r \geq (1 + \varepsilon)r'$ for a constant $\varepsilon > 0$, then there exists an infinite family of graphs $\{G^r\}$ for which the corresponding gap is at least $(\log|G^r|)^c$ for a constant $c > 0$. So far, all evidence suggest that no such gap exists, as formalized in Conjecture 10.1.

### 10.2 Our Lower Bound

**Theorem 10.2** (Restatement of Theorem 1.4). Suppose that the Li-Li network coding conjecture [LL04] is true. Moreover, suppose that each element’s payload length $w > \log_2 n - k$, and the key length $k \leq \log_2 n$. Then, any constant fan-in, constant fan-out boolean circuit that can sort $n$ elements each with a $k$-bit key and a $w$-bit payload must have size at least $\Omega(nk \cdot (w - \log_2 n + k))$.

**Proof.** Consider a fixed constant fan-in, constant fan-out boolean circuit; the topology of the circuit induces a directed graph $G$. Without loss of generality, we may assume that the graph $G$ has in-degree and out-degree 2, since any constant fan-in, constant fan-out gate can be broken up into constant number of gates with fan-in and fan-out 2. Given an input array $I$, let $\text{keys}(I)$ denote the sequence of all elements’ keys in the input $I$, and $\text{payloads}(I)$ denote the sequence of all payloads in the input $I$. Every element in the input array $I$ is represented by $k + w$ input nodes in the graph $G$, $k$ input nodes for representing the key henceforth also called key-input-nodes, and $w$ input nodes for representing the payload, henceforth also called payload-input-nodes.

Without loss of generality, we may assume that $n \geq 2^k$ is a power of 2. We consider the set of input arrays where each of the $2^k$ distinct keys appears exactly $n/2^k$ times. Therefore, for each element in the input array, its key will determine at most $n/2^k$ possible positions for the element to appear in the sorted output. This means that for every payload-input-node $v$, depending on the corresponding element’s key denoted key, the input bit assigned to $v$ must be transferred to an output node among $n/2^k$ possible choices — henceforth we use the notation $O_{v,\text{key}}$ to denote the set of $n/2^k$ possible choices of output nodes for the payload-input-node $v$, determined by the corresponding element’s key. Let $D_{v,\text{key}}$ denote the minimum distance from $v$ to any output node in $O_{v,\text{key}}$. Observe that for any payload-input-node $v$, at least $2^k - 2^{k/2}$ choices of key $\in \{0,1\}^k$ will give $D_{v,\text{key}} \geq k/2$. This is because in $k/2$ depth, $v$ can reach only $2^{k/2}$ nodes in $G$.

With this, we can conclude the following:

**Claim 10.3.** Fix any subset $S$ of payload-input-nodes. There exists a choice of keys($I$), henceforth denoted keys($I$), where each of the $2^k$ distinct keys appears exactly $n/2^k$ times, such that the at least $1 - \frac{1}{2^{k/2}}$ fraction of the payload-input-nodes in $S$, denoted $v$, must satisfy $D_{v,\text{key}(v)} \geq k/2$ where key($v$) is the key in keys($I$) corresponding to $v$.
Proof. To see this, we can sample keys(I) at random subject to the constraint that each of the $2^k$ distinct keys must appear exactly $n/2^k$ times. For each fixed $v$, the probability that $D_{v,\text{key}(v)} \geq k/2$ is at least

$$\frac{2^k - 2^{k/2}}{2^k} = 1 - \frac{1}{2^{k/2}}$$

Due to linearity of expectation, we conclude that in expectation, there is at least $1 - \frac{1}{2^{k/2}}$ fraction of such $v$’s in any fixed $S$ that satisfy $D_{v,\text{key}(v)} \geq k/2$. 

We now continue with the proof of Theorem 10.2.

Augmenting the graph. So far we have considered the directed graph $G$ that represents the circuit. We now augment the graph $G$ into a new graph $G'$ as follows. We add $2^k$ nodes, henceforth called aggregators. We now add a directed edge from every output node in $G$ corresponding to an element with the key $i$, to the $i$-th aggregator. The $i$-th aggregator node will now stably sort these elements (whose keys are $i$) based on the first $\log_2 n - k$ bits of their payload, and output the sorted elements — the corresponding output nodes become the output nodes of the new graph $G'$. In total, $G'$ has $(k + w)n$ output nodes, corresponding to a total of $n$ elements; the output nodes are ordered first by the element’s keys, using the first $\log_2 n - k$ bits of the elements’ payload to break ties.

Now suppose we fix the choice $\text{key}^i(I)$ as mentioned above, for all input elements with the same key, we choose the first $\log_2 n - k$ bits of their payload based on the order in which they appear in the input, i.e., for some key $k$, the leftmost element with key $k$ receives 0 as the first $\log_2 n - k$ bits of their payload, the second leftmost element with key $k$ receives 1 as the first $\log_2 n - k$ bits of their payload, and so on. The remaining $w - \log_2 n + k$ bits of every element’s payload is chosen at random. We may consider the key bits and the first $\log_2 n - k$ bits of the payloads as being hard-wired into the network, and every edge has capacity 1 — henceforth we call this resulting network $G''$. The resulting network solves a $k$-pairs communication problem — which source is paired with which destination is determined by $\text{keys}^i(I)$ and the first $\log_2 n - k$ bits of each payload. Moreover, the network routes $(w - \log_2 n + k)n$ input nodes to $(w - \log_2 n + k)n$ output nodes, where each input node receives a uniform random bit as input.

Applying the Conjecture 10.1. Now, consider the undirected version of $G''$ where each edge’s capacity is still 1. Based on Conjecture 10.1, the undirected version of $G''$ should solve the corresponding multi-commodity flow problem where each of the $(w - \log_2 n + k)n$ input nodes wants to route a commodity to each of the $(w - \log_2 n + k)n$ output nodes. In the solution of the multi-commodity flow problem, the $i$-th aggregator node in $G''$ must have $\frac{n}{2^k} \cdot (w - \log_2 n + k)$ amount of flow coming in; further, there is one unit of flow corresponding to each of the last $w - \log_2 n + k$ payload bits for each element whose key is $i$. Due to Claim 10.3, $1 - 1/2^{k/2}$ fraction of the input nodes in $G''$ has a path of length at least $k/2 + 1$ to its corresponding aggregator node. We conclude that $G''$ has at least $\frac{n}{2^k} \cdot (w - \log_2 n + k) \cdot 2^{k/2} \cdot (k/2 + 1)$ edges not including the edges between the aggregator nodes and the $(w - \log_2 n + k)n$ output nodes. Thus, the graph $G''$ has at least $\frac{nk}{2^k} \cdot (w - \log_2 n + k)$ edges excluding the aggregator nodes and all its incident edges. This means that the original circuit’s size is at least $\Omega(nk \cdot (w - \log_2 n + k))$.

Finally, as mentioned earlier, our lower bound requires that $w \geq \log_2 n - k$. Technically, this is because in our proof, we steal $\log_2 n - k$ bits from the payload to fix an ordering among the elements with the same key. Our lower bound shows the near optimality of our construction for sufficiently
large $w$. For small $w$, it is an interesting open question whether a better upper bound exists — however, to answer this question would necessarily require us to consider algorithms that are not in the indivisible model due to the $\Omega(nk)$ lower bound on the number of selector gates for any algorithm in the indivisible model [LSX19].

11 Conclusion and Future Work

In this paper, we showed a theoretical generalization of the AKS sorting circuit. We show that for sorting $n$ elements each described with a $k$-bit key and a $w$-bit payload, a circuit of size $O(n(k + w) \cdot k \cdot \text{poly}(\log^* n - \log^* (k + w)))$ suffices. Specifically, when $k = o(\log n)$, our circuit size is asymptotically better than AKS (ignoring polylog* terms). As a special case and stepping stone to our main result, we also show that compaction and selection can be computed with linear-sized circuits. We also show that our result is nearly optimal for every choice of $k$ as long as $k = O(\log n)$.

Our work leaves open the following future directions:

1. An obvious open question is to get rid of the extra polylog* terms in the circuit size.
2. Another open question concerns the depth of the circuit. In this work, we cared mostly about minimizing the circuit size, but not the depth. Therefore, an open question is, can we sort $n$ elements each described with a $k$-bit key and a $w$-bit payload, with a circuit of size $O(nk \cdot (k + w))$ and depth $O(\log n)$? We note that $\Omega(\log n)$ depth is necessary even for compaction, i.e., 1-bit sorting. Observe that a compaction circuit can compute the logical-or of $n$ bits, which is known to have a $\Omega(\log n)$-depth lower bound even on a Concurrent-Read-Exclusive-Write (CREW) PRAM [CDR86]; and clearly, a circuit of depth $d$ can be simulated by a CREW PRAM of depth $d$.
3. Our construction currently has an enormous constant. Can we attain asymptotically the same result but with smaller concrete constants?
4. Finally, as mentioned earlier, another question is whether better upper bounds exist for small $w$ — as mentioned, if such upper bounds existed, they cannot be in the indivisible model due to the $\Omega(nk)$ lower bound on the number of selector gates in the indivisible model [LSX19].

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A Compaction Circuit for Tiny $w$

We now describe a compaction circuit for very small $w$, e.g., when $w$ is constant or slightly larger than a constant. Recall that our Theorem 1.2 states that there is a circuit of $O(nw) \cdot \min (\text{poly}(\log^* n - \log^* w), \ 2^w/w)$ size to compact $n$ elements each of bit-width $w$. Section 7 obtained the $O(nw) \cdot \text{poly}(\log^* n - \log^* w)$ part of the result; therefore this section shows that there is a circuit of size $O(n \cdot 2^w)$ that can compact $n$ elements each of bit-width $w$.

Henceforth, we assume that each distinguished element is marked with the label 0 and each non-distinguished element is labeled with 1. Given an element of bit-width $w$, we can define an extended element whose length is $w + 1$ bits by concatenating the element’s distinguished label and its payload. Therefore, an extended element can take value from the domain $\{0, 1, \ldots, 2 \cdot 2^w - 1\}$. To achieve compaction, we will actually view all elements as extended elements and sort all of them. To achieve this, we will perform the following:

First, for each extended element $v \in \{0, 1, \ldots, 2 \cdot 2^w - 1\}$, count how many times extended elements of value at most $v$ have appeared in the input array. The result is stored in an array
called \( \text{psum} \). Now, the length of \( \text{psum} \) is \( 2 \cdot 2^w \) and each entry of \( \text{psum} \) is encoded with \( \log n + 1 \) bits. The \( v \)-th entry of \( \text{psum} \) stores how many extended elements have value at most \( v \). To compute \( \text{psum} \) with an \( O(2^wn) \)-sized circuit, it suffices to perform the procedure below.

1. For each extended element of a value \( v \), run the binary-to-unary conversion (Fact 4.7) to get the \( (2 \cdot 2^w - 1) \)-dimensional vector such that the head \( v \) coordinates are 0s and the tail \( 2 \cdot 2^w - 1 - v \) coordinates are 1s. This conversion yields \( n \) vectors (each of \( 2 \cdot 2^w - 1 \) bits) and takes \( O(n \cdot 2^w) \) generalized boolean gates.

2. For each \( i \in \{0, 1, \ldots, 2 \cdot 2^w - 1\} \), count the number of 1s in the \( i \)-th coordinate of all \( n \) vectors, and let the result be the \( i \)-th entry of \( \text{psum} \). Using Fact 4.3, this counting takes \( O(n \cdot 2^w) \) generalized boolean gates.

From this array \( \text{psum} \), we can generate the sorted output array using a binary tree with \( n \) leaves. Imagine that each output position is a leaf node in the tree; without loss of generality, we may assume that \( n \) is a power of 2. Initially, the root holds \( \text{psum} \) and every entry in \( \text{psum} \) takes \( \log n + 1 \) bits to encode. The root now prepares an array \( \text{psum}_L \) to send to the left child by setting every entry in \( \text{psum} \) greater than \( n/2 \) to \( n/2 \). Therefore, every entry in \( \text{psum}_L \) takes one fewer bit to encode than the original \( \text{psum} \).

Similarly, the root prepares an array \( \text{psum}_R \) to send to the right child by setting every entry in \( \text{psum} \) smaller than or equal to \( n/2 \), and every entry whose value is at least \( n/2 \) to the original value minus \( n/2 \). Therefore, each entry in \( \text{psum}_R \) also takes one fewer bit to encode than the original \( \text{psum} \).

We continue this process at every level of the tree (where the root is assumed to be at level 0). Each node in level \( i \) sends an array to its left child and right child, and the number of bits needed to encode each entry of the array is \( \log n - i \). An array \( \text{psum}' \) received by a node in the tree always encodes the prefix sums within its own subtree; specifically \( \text{psum}'[v] \) encodes how many times extended elements at most \( v \) have appeared in its subtree.

Finally, when a leaf node receives an incoming array \( \text{psum}' \), scan through the array to find the first index \( v \) such that \( \text{psum}'[v] \) is non-zero and output \( v \). The final sorted array is obtained by concatenating all leaves’ output values from left to right.

The computation done by each node at level \( i \) in the tree can be implemented with an \( O(2^w(\log n - i)) \)-sized circuit.

Summarizing the above, it is not hard to see that the entire computation can be implemented with an \( O(2^wn) \)-sized circuit.

## B Optimizations and Tightened Theorem Statement

In this section, we fine-tune the parameters in the construction of Section 5, 6, and 7 to minimize the polynomial \( \text{poly}(\cdot) \) in Theorem 7.1. As stated in the following, this \( \text{poly}(\cdot) \) can be chosen to nearly quadratic.

**Theorem B.1** (Linear-sized tight compaction, tightened). \textit{For any constant } \( \gamma > 0 \text{, there exists a constant fan-in, constant fan-out boolean circuit that solves } (n, w) \text{-tight compaction and the total number of boolean gates is upper bounded by } \max\left(1, \left(\log^* n - \log^* w\right)^2 + \gamma\right) \cdot O(n \cdot w).}

**Proof.** The case \( w > \log n \text{ is easy (see Footnote 10) so henceforth we focus on the case } w \leq \log n \text{. We begin with re-parameterizing the construction with some } \epsilon_1, \epsilon_2, \ldots, \text{ analyzing the constraints between the parameters, and then choosing them appropriately to satisfy the given } \gamma > 0 \text{.}

The construction is re-parameterized as follows with our previous parameters noted.
• In Step 1 of Algorithm 5.2, call an \((n, w)\)-loose swapper such that at most \(\epsilon_1\) fraction of resulting array remain colored. (Previously \(\epsilon_1 := 1/128\).)

• In Section 6.1, we aim to construct an \((n, w)\)-loose compactor such that takes as input at most \(\epsilon_1 \cdot n\) real elements and outputs an array of \(\epsilon_2 \cdot n\) elements. We re-parameterize the construction in Section 6.1 as follows. (Previously \(\epsilon_2 := 1/2\).)

  – In Step 1 of Section 6.1, define a chunk as sparse if there are at most \(\epsilon_3 \cdot f(n)\) real elements in it; otherwise define it dense. (Previously \(\epsilon_3 := 1/32\).)

  – Hence, at most \(\epsilon_4 \cdot \frac{n}{f(n)}\) chunks are dense, and at least \((1 - \epsilon_4)\) fraction of chunks are sparse, where \(\epsilon_4 := \epsilon_1/\epsilon_3\). Use \(\epsilon_4\) and \(1 - \epsilon_4\) as thresholds in Step 3 of Section 6.1. (Previously \(\epsilon_4 := 1/4\).)

We then analyze the constraints on the above parameters. As noted in Theorem 4.13, for any constant \(\epsilon_1 > 0\), there is a linear sized \((n, w)\)-loose swapper, so \(\epsilon_1\) is not constrained. Then, by the above parameters \(\epsilon_3\) and \(\epsilon_4\), the output size of Section 6.1 is \(\epsilon_4 \cdot n + \epsilon_3 f(n) \cdot \left\lfloor (1 - \epsilon_4) \cdot \frac{n}{f(n)} \right\rfloor\), which aimed to be at most \(\epsilon_2 \cdot n\). For any constant \(\epsilon_4 \in (0, 1)\), \(f(x) \leq \log x\), there exists a constant \(n_0 \in \mathbb{N}\) such that \(\left\lfloor (1 - \epsilon_4) \cdot \frac{n}{f(n)} \right\rfloor \leq \frac{n}{f(n)}\) for all \(n > n_0\). Hence, we need \(\epsilon_3 + \epsilon_4 \leq \epsilon_2\) to achieve the \(\epsilon_2 \cdot n\) output size.

Next, we inductively calculate the circuit size in the bootstrapping of Section 7.2. The bootstrapping starts from Algorithm 4.9, which takes \(C(1) \cdot n \log_2 n\) generalized boolean gates and \(C(1) \cdot n\) number of \(w\)-selector gates for some constant \(C(1)\). Let \(c_1 \cdot n\) be the number of generalized boolean gates and \(c_2 \cdot n\) be the number of \(w\)-selector gates of the \((n, w)\)-loose swapper. After \(d\) times of repeated bootstrapping, assume for induction that the loose compactor takes \(C(d) \cdot nf(n)\) generalized boolean gates and \(C(d) \cdot n\) number of \(w\)-selector gates, where \(C(d)\) is a function of \(d\) (rather than \(n\)). To construct a tight compactor from such loose compactor, we count and color elements, which takes \(c_3n\) boolean gates for some constant \(c_3\) in Section 5.1; Then, we run the loose swapper and the \((n, w + 1)\)-loose compactor recursively, where problem size \(n\) is decreasing by \(\epsilon_2\). Hence, the tight compactor takes following costs.

\[
\begin{align*}
\text{generalized boolean gates:} & \quad \frac{1}{1 - \epsilon_2} \cdot \left(2c_1n + C(d) \cdot nf(n) + (c_2 + c_3 + C(d)) \cdot n\right) \\
\text{\(w\)-selector gates:} & \quad \frac{1}{1 - \epsilon_2} \cdot \left(c_2n + 2C(d) \cdot n\right)
\end{align*}
\]

We continue to construct the \((d + 1)\)-bootstrapped loose compactor by marking dense and sparse chunks, which takes \(c_4n\) boolean gates. Afterwards, we run 1 instance of \([\lceil n/f(n) \rceil, f(n) \cdot w]\)-tight compactor and \(\left\lceil (1 - \epsilon_4) \cdot \frac{n}{f(n)} \right\rceil\) instances of \((f(n), w)\)-tight compactor. Let \(\bar{n}_1 := \lceil n/f(n) \rceil\) and \(\bar{n}_2 := \left\lceil (1 - \epsilon_4) \cdot \frac{n}{f(n)} \right\rceil\) for short. Then, the number of generalized boolean gates is

\[
\begin{align*}
&\quad c_4n + \frac{1}{1 - \epsilon_2} \cdot (2c_1\bar{n}_1 + C(d) \cdot \bar{n}_1 f(\bar{n}_1) + (c_2 + c_3 + C(d)) \cdot \bar{n}_1) \\
&\quad + \frac{1}{1 - \epsilon_2} \cdot (2c_1f(n) + C(d) \cdot f(n) f(f(n)) + (c_2 + c_3 + C(d)) \cdot f(n)) \cdot \bar{n}_2 \\
&\leq \frac{1}{1 - \epsilon_2} \cdot (2C(d) \cdot n + C(d) \cdot f(f(n)) \cdot n + C(d) \cdot \bar{n}_1 + c_5n),
\end{align*}
\]
where \( c_5 = c_4 + 4c_1 + 2c_2 + 2c_3 \) is a constant, and the rounding up in \( \tilde{n}_1 \) and \( \tilde{n}_2 \) are absorbed by \( \epsilon_4 \) for all \( n > n_0 \). Similarly, the number of \( w \)-selector gates is

\[
\frac{1}{1 - \epsilon_2} \cdot (c_2\tilde{n}_1 + 2C(d) \cdot \tilde{n}_1) \cdot f(n) + \frac{1}{1 - \epsilon_2} \cdot (c_2 f(n) + 2C(d) \cdot f(n)) \cdot \tilde{n}_2
\]

\[\leq \frac{1}{1 - \epsilon_2} \cdot (4C(d) \cdot n + 2c_2n).\]

We choose \( C(d + 1) := C(d) \cdot \frac{4}{1 - \epsilon_2} + \frac{c_5 + 2c_2}{1 - \epsilon_2} \) so that the number of generalized boolean gates is at most \( C(d + 1) \cdot f(f(n)) \cdot n \) and the number of \( w \)-selector gates is at most \( C(d + 1) \cdot n \). As the base case \( C(1) \) is a constant, the recursion of \( C(d) \) solves to \( C(d) = O\left(\left(\frac{1}{1 - \epsilon_2}\right)^d\right)\).

Putting together, after repeated bootstrapping for \( d \) times, the multiplicative overhead is \( \left(\frac{4}{1 - \epsilon_2}\right)^d \), which equals to \( (\log^* n - \log^* w)^{2+\log_2 \frac{1}{1 - \epsilon_2}} \) as \( d = \log_2(\log^* n - \log^* w) \). Hence, for any \( \gamma > 0 \), it suffices to choose \( \epsilon_2 = \frac{2\gamma - 1}{2\gamma} \), \( \epsilon_3 = \epsilon_4 = \epsilon_2/2 \), and \( \epsilon_1 = \epsilon_3 \cdot \epsilon_4 \) to satisfy all the above constraints.

We remark that in Algorithm 4.9, we need that the input to loose compaction is sparse enough (i.e., 1/128) so the ProposeAcceptFinalize works. However, any \( \epsilon_1 \leq \epsilon_2 \) works in Section 6.1 because we use tight compactor directly. Hence, Algorithm 4.9 is only used in the base case of the repeated bootstrapping (and we do not tune its parameters).