β-Ga$_2$O$_3$ Field Plate Schottky Barrier Diode With Superb Reverse Recovery for High-Efficiency DC–DC Converter

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ABSTRACT β-Ga$_2$O$_3$ Schottky barrier diodes with field plate (FP-SBDs) are fabricated and their SPICE-compatible model are constructed for double-pulse test circuit and DC-DC boost converter simulations. The reverse recovery time ($t_{rr}$) of the β-Ga$_2$O$_3$ SBD is 8.8 ns and its reverse recovery charge ($Q_{rr}$) is 8.33 nC when switching from a forward current of 1 A to a reverse bias voltage of 100 V with a $di/dt$ of 400 A/μs, which is analogous with the prediction of our model. Device with the radius of 500 μm was fabricated, a current of 2 A can be obtained at the forward voltage of 2 V, meanwhile, the breakdown voltage is 467 V. The Ga$_2$O$_3$-based converter module after device packaging with TO-220 reveals a comparative efficiency to that of the SiC-based converter under multiple conditions, and reached up to 95.62% at the input voltage of 200 V. The decent performance of Ga$_2$O$_3$ FP-SBD and its DC-DC converter indicates great potential in power application.

INDEX TERMS β-Ga$_2$O$_3$, Schottky barrier diode, SPICE-compatible model, double-pulse test circuit, DC-DC converter.

I. INTRODUCTION

Power devices and circuits are the parts that control electrical energy conversion. In order to reduce the power consumption of electrical equipment, it is necessary to reduce the energy conversion loss on power devices. Developing power devices and circuits based on novel ultra-wide bandgap semiconductors can contribute to combating global warming due to a reduction in CO$_2$ emissions [1].

β-Ga$_2$O$_3$ has great potential in power electronic applications due to its large bandgap of approximately 4.8 eV, high critical electric field of 8 MV/cm and Baliga’s figure of merit of 3444 [2], [3], [4], which is superior to SiC and GaN significantly. Its effective wide N-type doping range of $10^{16}$ to $10^{19}$ cm$^{-3}$ and low-cost substrate growth method have enabled β-Ga$_2$O$_3$ to become a promising candidate for the next generation power semiconductors [5], [6], [7], [8], [9], [10].

Numerous studies have focused on β-Ga$_2$O$_3$ Schottky barrier diodes (SBDs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], whose performances have improved significantly and currently approach those of SiC and GaN power devices [21], [22], [23], [24]. Various techniques have been proposed to further optimize the on-resistance and breakdown voltage of devices, such as field-ring, field-plate, and SU-8 passivation [25], [26], [27].
Meanwhile, the performance of Ga$_2$O$_3$ SBD is outstanding compared to MOSFET up till now, thus Ga$_2$O$_3$ SBD is more mature for circuit application.

Functional circuits based on $\beta$-Ga$_2$O$_3$ devices are scarce so far. $\beta$-Ga$_2$O$_3$ SBD was used in rectification circuit to test the rectification characteristics at high frequency [28]. Moreover, $\beta$-Ga$_2$O$_3$ FETs were used in a boost converter to compare their performance [29]. DC-DC boost converter can be applied to enhance the output voltage for functional circuits and utilized in fields of power transformation, such as home electronics, industrial control and new energy [30], [31], [32], [33], [34]. A converter circuit usually contains SBD and MOSFET, and the whole power efficiency relies on the static and dynamic performance of these devices [35], [36], [37]. Acceptable off-state and reverse recovery characteristics of SBD guarantee stable output waveforms and less overall power loss [38], meanwhile, a WBG (SiC, GaN and Ga$_3$O$_2$) SBD has better reverse recovery characteristics due to its unique parallel structure compared to a Si device [39]. However, there is still no study on Ga$_2$O$_3$ SBD in DC-DC converters, so the application potential of Ga$_2$O$_3$ SBD needs to be further demonstrated.

This work contains a complete process from device to circuit including device fabrication, compact model, SPICE simulation, device package and circuit modularization based on Ga$_2$O$_3$ SBD with field plate (FP-SBD). Sections II and III describe the fabrication process and performance of the Ga$_2$O$_3$ FP-SBD. The SPICE model for Ga$_2$O$_3$ FP-SBD is illustrated in Section IV and the agreement of the simulation results and experimental results are almost consistent. Section VI details the simulation results and physical performance of a DC-DC boost converter utilizing packaged devices. The main conclusions are derived in Section VII.

**II. DEVICE FABRICATION**

The fabrication process flow of the vertical Ga$_2$O$_3$ Schottky barrier diode with field-plate (FP-SBD) structure is illustrated in Fig. 1. The 610-$\mu$m-thick Ga$_2$O$_3$ substrate is Sn-doped with a concentration of $7.0 \times 10^{18}$ cm$^{-3}$ grown by edge-defined film-fed growth (EFG). The 7.6-$\mu$m-thick Ga$_2$O$_3$ epitaxial layer grown by halide vapor phase epitaxy (HVPE) has a low doping concentration of approximately $1.7 \times 10^{16}$ cm$^{-3}$. After organic and acid cleaning, the backside of the Ga$_2$O$_3$ substrate is coated with Ti (20 nm)/Au (100 nm) metal stack through e-beam evaporation. Then the Ga$_2$O$_3$ substrate undergoes rapid thermal annealing at 470°C for 1 min in N$_2$ atmosphere to improve the quality of ohmic contact.

Bilayer Al$_2$O$_3$ and SiN$_x$, which have thicknesses of 20 nm and 320 nm respectively, are deposited in order on the front side. This combination guarantees a high-quality interface between the dielectric and $\beta$-Ga$_2$O$_3$, while the growth method is economical. The Al$_2$O$_3$ is grown by atomic layer deposition (ALD) with trimethylaluminum and H$_2$O as the precursor. Then top-layer SiN$_x$ with dichlorosilane and NH$_3$ as the precursor is deposited by plasma-enhanced chemical vapor deposition (PECVD). Wet etching is applied to form metal contact holes with buffered oxide etchant (BOE). The Schottky electrode with a composite of Pt (20 nm) and Au (100 nm) on the front side is formed by a single lithography, magnetron sputtering, and lift-off process. The Schottky electrode extends over the dielectric to act as the field plate (FP), with its length set to be 20 $\mu$m. The radiuses of the Schottky contact are designed to be 100, 150, and 200 $\mu$m.

Fig. 2(a) shows the optical top view images of FP-SBDs with different radiuses. The raised edge of Schottky contact is just the field plate, and all these lengths are uniformed. Fig. 2(b) is the cross-sectional scanning electron microscopy image of the fabricated FP-SBD. The sidewall of the double-layered dielectric after wet etching is almost vertical.

**III. DEVICE PERFORMANCE**

The forward conduction characteristics of Ga$_2$O$_3$ FP-SBDs with radiuses of 100, 150, and 200 $\mu$m are illustrated in Fig. 3. The knee voltage of all devices is 0.8 V in common. The inset of Fig. 3(a) compares the specific on-resistance of different devices, which are 6.45, 8.19 and 10.40 m$\Omega$·cm$^{-2}$, respectively. The result reveals that the FP-SBD with a smaller radius has lower specific on-resistance. The current flowing from the anode into the $\beta$-Ga$_2$O$_3$ substrate will have horizontal diffusion current [1]. The linear fitting of the semi-log plot of current density versus voltage in Fig. 3(b) gives the ideality factor of 1.04 and Schottky barrier height of 1.16 eV, which indicates that the forward electron transport is close to the ideal thermionic emission model [40]. The on-off current ratio up to $10^8$ is achieved with favorable rectification capability. For all tested devices with different radiuses, the Schottky contact properties are
ideal and uniform as depicted in Fig. 3(b), which shows similar ideality factor and barrier height.

The forward conduction characteristics of FP-SBD (radius = 150 μm) with increasing temperature are shown in Fig. 4(a). The increasing on-state voltages of FP-SBD at a current density of 100 A/cm² under increasing temperatures indicate a positive correlation temperature characteristic. Fig. 4(b) also demonstrates a positive temperature coefficient of the specific on-resistance, which can be utilized to parallel different devices to conduct a large current and ensure the uniformity of the current between different devices [41]. Additionally, the knee voltages of devices at increasing temperatures decrease and induce the intersection of different on-state curves at different temperatures.

The capacitance-voltage curves of FP-SBDs with radiuses of 100, 150, and 200 μm are presented in Fig. 5(a). Fig. 5(b) provides a doping concentration of $1.7 \times 10^{16}$ cm⁻³ in the epitaxy layer, which accounts for the slightly large on-resistance of Ga₂O₃ FP-SBDs.

The field plate structure has weakly impact on the forward conduction characteristics of the Ga₂O₃ SBD, which can be verified by Fig. 6(a). The on-resistance and forward conduction current are nearly the same for the SBDs with and without FP. The breakdown voltage of a Ga₂O₃ SBD without field plate is 215 V for radius of 100 μm. In contrast, the breakdown voltages of Ga₂O₃ FP-SBD exceed 600 V as shown in Fig. 6(b). The termination of field plate mitigates the electric field crowding at the contact edge and effectively enhances the breakdown voltage. Even so, the performance of the device is underutilized, and better termination structures such as ion implantation, junction termination extension, etc. need to be developed in the future.

In order to satisfy the needs of large current in DC-DC converter, large-area device with the radius of 500 μm was also fabricated. The forward conduction characteristics and reverse blocking properties of the device are shown in Fig. 7, a current of 2 A can be obtained at the forward voltage of 2 V (50-μs pulse width and 1% duty cycle), meanwhile, the breakdown voltage is 467 V, which is relatively superior to other large-area SBDs as shown in Fig. 8 [13], [42], [43], [44], and can be utilized to provide sufficient safety area for the implementation of 350 V-output circuit.

IV. DEVICE MODELING
The device model plays a very important role in simulation, and it can also provide guidance for applications. In this
work, a SPICE model for \( \text{Ga}_2\text{O}_3 \) SBD is constructed from the experimental results with the \( I-V \) model of
\[
I = I_s \exp \left[ \frac{q(V - IR_s)}{nkT} \right],
\]
and the \( C-V \) model of
\[
C = \frac{C_j 0}{(1 - V/V_j)^M},
\]
where \( I_s \) is the reverse saturation current, \( q \) is the elementary charge, \( V \) is the forward voltage, \( n \) is the ideality factor, \( k \) is the Boltzmann factor, and \( T \) is the absolute temperature. \( C_j 0 \) is the depletion capacitance at \( V = 0 \), \( V_j \) is the zero-bias build-in potential, and \( M \) is the fitting parameter considering the non-ideal effect [45].

Fig. 9 shows the equivalent circuit of the \( \text{Ga}_2\text{O}_3 \) SBD, which contains a diode, a junction capacitance \( (C_j) \) in parallel, and a series resistance \( (R_s) \) [46], [47], [48]. The diode dominates an exponential growth in the curves of forward current density versus voltage under low voltage, while the resistance dominates the linear growth region at high voltage, as depicted in Fig. 3. The junction capacitance has an effect on the reverse recovery characteristics of the SBD and is frequency dependent.

The \( \text{Ga}_2\text{O}_3 \) SBD used in modeling has a radius of 500 \( \mu \text{m} \), and its corresponding parameters extracted from the experimental results are contained in Table 1. Since the breakdown voltage and the reverse current under breakdown have little effect on the power loss and voltage conversion ratio in our simulation, these parameters are not taken into consideration in device modeling. The simulated forward conduction characteristics and capacitance-voltage characteristics based on this model are consistent with experimental results as depicted in Fig. 10, which proves the validity of our SPICE model. However, the SPICE model is still in its infancy, and more problems such as thermal issues still need to be addressed in the next stage.

V. SWITCHING PERFORMANCE OF DEVICE

A double-pulse test (DPT) circuit was designed to evaluate the switching performance of \( \text{Ga}_2\text{O}_3 \) SBD [39], [49], [50], [51], [52]. The schematic of DPT circuit and its switching process are shown in Fig. 11. The test circuit mainly contains a Si power MOSFET (Infineon, IPD60R360P7ATMA1, 600 V/9 A), a 560 \( \mu \text{H} \) inductor for continuous current modulation and our \( \text{Ga}_2\text{O}_3 \) SBD. During the switching process, when the MOSFET is off-state, the current flows from the inductor to the \( \text{Ga}_2\text{O}_3 \) SBD, and the \( \text{Ga}_2\text{O}_3 \) SBD is in forward conduction as shown in Fig. 11(b); when the MOSFET switches from the off-state to the on-state, the inductor is charged by the input power supply, the \( \text{Ga}_2\text{O}_3 \) SBD switches from the on-state to the off-state, and a reverse recovery current occurs during the removal of the charges in the SBD as shown in Fig. 11(c), which is closely
related to the parasitic capacitance. Through proper selection of the inductor parameter, its current can remain stable with extremely low fluctuations and switches between the MOSFET and SBD.

The reverse recovery characteristic of Ga$_2$O$_3$ SBD with the radius of 500 $\mu$m was measured when the device switched from a forward current of 1 A to a reverse bias voltage of 100 V with a $di/dt$ of 400 A/$\mu$s. Comparison of the reverse recovery properties between the experimental and simulation results with the Ga$_2$O$_3$ SBD is shown in Fig. 12(a), the simulation results using our SPICE model are almost consistent with the experimental results. The reverse recovery properties of the Si FRD (Fast Recovery Diode), SiC SBD and Ga$_2$O$_3$ SBD are contrasted in Fig. 12(b), and the parameters of the reverse recovery characteristics are shown in Table 2. The on-resistance ($R_{on}$) of the SiC SBD and Ga$_2$O$_3$ SBD are 0.38 $\Omega$ and 0.65 $\Omega$, respectively, as for the SiC SBD, the forward voltage is 1.6 V, the total capacitance is 8.5 pF ($V_R = 400$ V, $T_j = 25$ °C, f = 1 MHz). The reverse recovery time ($t_{rr}$) is defined as the time required to recover to 10% of the peak reverse recovery current ($I_{rr}$). Experimental results reveal that the reverse recovery characteristic of Ga$_2$O$_3$ SBD has an apparent advantage over Si FRD and approaches to SiC SBD.

### VI. DC-DC BOOST CONVERTER

The Ga$_2$O$_3$ SBD with the radius of 500 $\mu$m is implemented into a DC-DC boost converter circuit, which is a step-up design with the output voltage higher than the input voltage, and the circuit configuration of the converter is shown in Fig. 13. The assessed specifications of the converter are summarized in Table 3. In comparison with the Ga$_2$O$_3$ SBD, 600 V/1 A SiC SBD (CREE, CSD01060A) and 600 V/1 A Si FRD (ST, STTH1106) are selected for the proposed DC-DC boost converter. The overall performance is compared between Ga$_2$O$_3$-, SiC- and Si-based converters to illustrate the effect of the device on circuit performance.

A 650 V/180 m$\Omega$ discrete GaN FET with the part number of TPH3206PSB from Transphorm is used for switching control, and the gate voltage signal ($V_{GS}$) for the GaN FET is +5 V during the on-state and 0 V during the off-state. The inductor ($L$) is used to store and provide energy and the magnitude of the current is controlled by the resistance ($R$). The input voltage ($V_{IN}$) is selected to be 200 V and the converter is operated at a switching frequency of 100 kHz. Negative temperature coefficient thermistor (NTC) and transient voltage suppression diode (TVS) are implemented in the circuit to provide overcurrent and overvoltage protection. The output capacitance ($C_{OUT}$) ensures the stability of the output voltage ($V_{OUT}$). The MOSFET and SBD are turned on alternately to provide stable output.

Fig. 14 shows the comparison of simulation results for the DC-DC boost converters between Ga$_2$O$_3$- and SiC-based circuits. The two converters have comparative values including the inductor current ($I_L$), the diode voltage ($V_D$) and the MOSFET voltage ($V_{DS}$). The output voltages of the Ga$_2$O$_3$- and SiC-based converter are approximately 330.87 V and 330.94 V, respectively, and their output voltage ripples are

### Table 2. Parameters of reverse recovery characteristics.

| Parameters | Si FRD (STTH1106) | SiC SBD (CSD01060A) | Ga$_2$O$_3$ SBD |
|------------|-------------------|---------------------|-----------------|
| $I_r$ (A)  | 3.01              | 1.28                | 1.53            |
| $t_r$ (ns) | 20.0              | 7.8                 | 8.8             |
| $Q_r$ (nC) | 37.99             | 5.93                | 8.33            |
| $R_{on}$* $Q_r$ (\*nC) | —               | 2.25                | 5.41            |
less than 0.1%. This minor difference of output voltage is mainly due to the larger on-resistance of the Ga$_2$O$_3$ FP-SBD.

The power loss distribution of the Ga$_2$O$_3$- and SiC-based converters in the simulation is shown in Table 4 and Fig. 15. The overall loss of the converter is produced by the SBD, MOSFET and other passive devices. The conversion efficiency of the Ga$_2$O$_3$-based converter is comparable to that of the SiC-based converter. The slightly lower efficiency of the Ga$_2$O$_3$-based converter is mainly due to the larger on-resistance and the slower reverse recovery process of the Ga$_2$O$_3$ SBD, which affects the conduction loss and switching loss directly.

The TO-220 package is used for our device to satisfy the needs for application and compare to SiC and Si commercial devices. Fig. 16 shows a photograph of the wire bonding and packaged device, 125 µm Al wire was used to connect the anode of the device and the right package pin, the middle package pin was the cathode pin, and the left pin was not in use. The packaging process is listed in Fig. 17.

The DC-DC boost converter module is shown in Fig. 18, Ga$_2$O$_3$ SBD, SiC SBD and Si FRD are tested in the same module. The input signal ($V_{GS}$) for controlling the MOSFET was generated by an arbitrary function waveform generator (Keysight, 33600A). The input voltage ($V_{IN}$) was generated by an auto range DC power supply (ITECH, IT6526C), and the output signal ($V_{OUT}$) was tested through a DC electronic load (ITECH, IT8902E). The voltage and current waveforms were monitored by an oscilloscope (Keysight, MSOX6004A). Using the parameters shown in Table 3, the experimental waveforms in the DC-DC boost converter based on Si FRD, SiC SBD and Ga$_2$O$_3$ SBD are shown in Figs. 19, 20 and 21, respectively. From the diode current ($I_D$) waveforms, we can

| TABLE 3. Specifications of DC-DC boost converter. |
|---------------------------------------------|
| Parameters | Values | Parameters | Values |
| GaN FET | 650 V/180 mΩ | $C_{SNB315}$ (µF) | 100 |
| SiC SBD | 600 V/1 A | $C_{OUD40V}$ (µF) | 6.8 |
| Si FRD | 600 V/1 A | $L$ (mH) | 1 |
| $V_{IN}$ (V) | 200 | $f$ (kHz) | 100 |
| $V_{OUT}$ (V) | 331 | $R$ (kΩ) | 1 |

| TABLE 4. Power loss distribution in converter simulation. |
|---------------------------------------------|
| Parameters | SiC converter | Ga$_2$O$_3$ converter |
| $P_{IN}$ (W) | 112.3740 | 112.4340 |
| $P_{OUT}$ (W) | 110.8715 | 110.8051 |
| Total loss (W) | 1.5025 | 1.6289 |
| $P_{loss-SBD}$ (W) | 0.4308 | 0.4730 |
| $P_{loss-MOSFET}$ (W) | 0.4140 | 0.5091 |
| Efficiency | 98.66% | 98.55% |

| FIGURE 15. Sectional diagrams of power loss distribution in converter simulation. |
|---------------------------------------------|

| FIGURE 16. Package diagram of the Ga$_2$O$_3$ SBD. |
|---------------------------------------------|

| FIGURE 17. Packaging process of the Ga$_2$O$_3$ SBDs. |
|---------------------------------------------|

| TABLE 5. Experimental results of DC-DC converter. |
|---------------------------------------------|
| Parameters | Si converter | SiC converter | Ga$_2$O$_3$ converter |
| $V_{IN}$ (V) | 200 | 200 | 200 |
| $V_{OUT}$ (V) | 329.0 | 330.8 | 326.4 |
| $P_{IN}$ (W) | 114.46 | 115.23 | 113.14 |
| $P_{OUT}$ (W) | 108.25 | 110.64 | 108.18 |
| Efficiency | 94.57% | 96.02% | 95.62% |
obtain that there is a spike of diode current \( (I_D) \) in each waveform, and the spike value of the \( \beta \)-Ga\(_2\)O\(_3\) FP-SBD is larger than that of SiC SBD but better than Si FRD due to the reverse recovery characteristic.

The conversion efficiency is computed with the relationship

\[
\eta = \frac{V_{\text{OUT}} I_{\text{OUT}}}{V_{\text{IN}} I_{\text{IN}}} \times 100\%,
\]

where \( I_{\text{OUT}} \) and \( I_{\text{IN}} \) are the output and input current, respectively [53].

The experimental results are shown in Table 5, the conversion efficiency of the Si FRD-, SiC SBD- and \( \beta \)-Ga\(_2\)O\(_3\) SBD-based converters are 94.57%, 96.02% and 95.62%, respectively, and the output voltage ripples are approximately 0.9%, the efficiency of the \( \beta \)-Ga\(_2\)O\(_3\)-based converter is better than that of the Si-based converter and close to that of SiC.

In order to illustrate the performance of the \( \beta \)-Ga\(_2\)O\(_3\) SBD in different situations, the circuit conversion efficiency is measured as a function of four independent variables, including input voltage \( (V_{\text{IN}}) \), load resistance \( (R) \), switching frequency \( (f) \) and duty cycle \( (D) \). The measured results are shown in Fig. 22.

As depicted in Fig. 22(a), the conversion efficiency increases with increasing input voltage \( (V_{\text{IN}}) \) from 50 V to 200 V. We can obtain a conversion efficiency reached up to 95.62% at the input voltage of 200 V, while the dependence of the conversion efficiency on the load resistance exhibits the opposite trend in Fig. 22(b), because the power loss is affected by the variation of resistance directly [54]. The efficiency in Fig. 22(b), (c) and (d) was measured with the input voltage of 100 V, as the output voltage would exceed the breakdown voltage of the device in some cases with the input voltage of 200 V. The efficiency decreased with increasing switching frequency in Fig. 22(c), as the switching process of the MOSFET and SBD due to more power losses [55], and the increase in conduction loss mainly affected the efficiency in Fig. 22(d).
From the above demonstrations, the performance of the Ga$_2$O$_3$-based converter is superior to that of the Si converter and inferior to that of SiC in multiple conditions. In fact, the research on Ga$_2$O$_3$ devices is just in its infancy, and the performance of Ga$_2$O$_3$ SBD is almost comparable to SiC SBD, so we can believe that it will be further enhanced with the optimization of our Ga$_2$O$_3$ device in the next stage.

**VII. CONCLUSION**

The $\beta$-Ga$_2$O$_3$ FP-SBD has approving forward conduction characteristics and possesses a breakdown voltage exceeding 600 V. A SPICE model of Ga$_2$O$_3$ FP-SBD is constructed and implemented into DPT circuit and boost converter simulation. The experimental results with a reverse recovery time of 8.8 ns and reverse recovery charge of 8.33 nC when switching from a forward current of 1 A to a reverse bias voltage of 100 V with a $di/dt$ of 400 A/$\mu$s are analogous with the DPT simulation results, which reveals the validity of our model. A current of 2 A can be obtained at the forward voltage of 2 V with the large-area device, meanwhile, the breakdown voltage is 467 V. The conversion efficiency of the Ga$_2$O$_3$-based converter module after device packaging with TO-220 is comparable to that of the SiC-based converter, and the value grows with increasing input voltage, while with decreasing switching frequency, duty cycle and load resistance. The efficiency value of the Ga$_2$O$_3$-based converter is almost consistent with that of the SiC-based converter, and reaches up to 95.62% at the input voltage of 200 V, which indicates the great potential of Ga$_2$O$_3$-based devices and circuits. With the reduction of the cost and the improvement of the material quality, power devices and circuits based on Ga$_2$O$_3$ material will have promising applications in the foreseeable future.

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