Analysis and Suppression of High Speed Dv/Dt Induced False Turn-on in GaN HEMT Phase-Leg Topology

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ABSTRACT Gallium nitride high electron mobility transistor (GaN HEMT) is liable to gate false turn-on problem when the gate crosstalk voltage exceeds its threshold voltage in the widely adopted phase-leg topology due to its low threshold voltage and high switching speed. Without considering the gate loop stray inductance, gate internal resistance, nonlinearity of parasitic capacitances and power loop stray parameters, traditional false turn-on analytical method is insufficient to support accurate analysis. And it has been found that GaN HEMT gate-source parasitic capacitance $C_{gs}$ previously assumed constant is otherwise highly nonlinear and has strong impacts on the gate crosstalk voltage. This paper has measured $C_{gs}$ by vector network analyzer and constructed an accurate nonlinear model of $C_{gs}$, based on which an accurate GaN HEMT behavior model is further fulfilled. The accuracy of the proposed behavior model has been verified by large amounts of experiment results. The proposed GaN HEMT model is used to accurately calculate gate crosstalk voltage and switching losses. Besides, false turn-on induced extra loss has been calculated and is adopted as a criterion to evaluate the severity of false turn-on and optimal design method for false turn-on suppression has been detailed further.

INDEX TERMS GaN HEMT, false turn-on, analytical method, behavior model, optimal design.

I. INTRODUCTION

Gallium nitride high electron mobility transistor (GaN HEMT) with the merits of high switching speed, low switching and conduction loss and small package size is becoming more and more prevalent in recent years [1], [2]. However, GaN HEMT is liable to false turn-on problem when the gate crosstalk voltage exceeds its threshold voltage in the commonly used phase-leg topology because of low gate threshold voltage and fast switching speed [3]–[5]. In order to avoid false turn-on induced extra switching loss and increase the stability of the power converter, false turn-on problem must be analyzed and suppressed thoroughly.

By far, some methods have been proposed to address false turn-on problems, and they can be classified into three types. The first type is trying to eliminate the intensity of exciting source that induces gate crosstalk voltage, among which the simplest way is to slow down the turn-on speed of GaN HEMT with large turn-on resistance, but it will increase the overlap loss during the turn-on transient [4]–[7]. By contrast, minimizing the power loop stray inductance by optimized layout and routing or deliberately designed snubber circuit seems more feasible [8]–[10]. Based on the mechanism analysis of crosstalk, the second type of false turn-on suppression method focuses on minimizing the impedance of gate turn-off loop [10]–[13]. Using a small turn-off resistance in the gate turn-off loop by adopting gate drivers with split turn-on and turn-off pins as presented in [10] is widely adopted.
Besides, the area enclosed by the gate turn-off loop is recommended to be as small as possible to minimize the stray inductance and possible EMI noise. While, gate turn-off loop resistance should be deliberately designed to avoid oscillation in the existence of gate turn-off loop stray inductance. Besides, unreasonably small gate turn-off resistance may also induce serious turn-off overvoltage. A programmable active gate driver has been proposed in [11] and it can suppress the crosstalk voltage by dynamically controlling the turn-on speed and gate turn-off impedance without the penalty of extra switching losses. While the control sequence of the active gate driver is very complex and it’s not commercially available yet. The last type of false turn-on suppression method is by adopting negative turn-off voltage as proposed in [14]–[17]. This is a very reliable false turn-on suppression method but with the penalty of driving complexity and extra reverse conduction loss.

Though so much false turn-on suppression method, quantitative method for practical usage is still absent. Traditional analytical methods addressing false turn-on problem are mostly applicable to silicon power devices without taken the gate loop inductance and nonlinearity of device parasitic capacitances into account as in [14]–[16]. Thus, they are not accurate enough for the analysis of GaN HEMT. Paper [18] has proposed an analytical model for GaN HEMT false turn-on analysis. However, the nonlinearity of parasitic capacitances is not considered. Besides, the modeling accuracy of false turn-on excitation signal is not guaranteed either. An accurate GaN HEMT device model has been proposed in [19], based on which effects of different parameters have on false turn-on voltage has been analyzed. However, the proposed device model in [19] is too complex for practical usage and the model parameter extraction method is also absent. In addition, the modeling and solving of false turn-on analytical circuit model is also a labor-intensive work. Paper [20] has proposed a GaN HEMT false turn-on analytical model. However, the nonlinearity of device gate-source capacitance has not been taken into consideration and modeling false turn-on excitation signal with a simple ramp function is not accurate enough.

Aiming at these issues, this paper has constructed an accurate behavior model of GaN HEMT with the modeling accuracy of gate-source capacitance enhanced, based on which a precise false turn-on analysis model is constructed further. At the basis of the proposed analytical model, the effects that different parameters have on crosstalk voltage can be accurately calculated. False turn-on induced extra turn-on loss has been adopted as a criterion to evaluate the seriousness of false turn-on and the effectiveness of false turn-on suppression method. Optimal design method for false turn-on suppression has been presented further. The paper is arranged as following: Section I gives an introduction to the pervasive crosstalk and false turn-on problems. The mechanism and analytical model of gate crosstalk and false turn-on is detailed in section II, based on which a quantitative parametric analysis has been conducted to illustrate the negative effect that gate turn-off loop impedance has on false turn-on problem. Nonlinear models of parasitic capacitances are also detailed in this section. To promote the accuracy of the calculated false turn-on voltage, an accurate GaN HEMT behavior model is constructed and verified in section III. Based on the proposed device model, optimal design methods for false turn-on suppression are detailed in Section IV. Conclusions are given in section V.

II. FALSE TURN-ON ANALYTICAL CIRCUIT MODEL

The mechanism of gate false turn-on in a GaN HEMT phase-leg topology is illustrated in Figure 1. When bottom GaN Q2 hard switches on, there will be a steep positive voltage pulse occurring on the drain-source terminal of top GaN Q1, and vice versa. Owing to the existence of miller capacitance $C_{gd}$, there will be displacement current flowing through $C_{gd}$ to gate-source capacitance $C_{gs}$ and gate turn-off loop, which will result in crosstalk voltage at the gate of GaN $Q_1$ at off state. Once the induced gate-source crosstalk voltage surpasses the intrinsic low threshold voltage of GaN, false turn-on will be triggered unfortunately.

A. CONSTRUCTION OF CIRCUIT MODEL

Gate false turn-on problem is not specific to GaN HEMT. It’s also common to traditional silicon and wide band-gap SiC power devices. While traditional methods have overlooked the influence that gate turn-off loop stray inductance has on crosstalk voltage. Aiming at this problem, an analytical circuit model is constructed to quantitatively calculated the crosstalk voltage with gate turn-off loop stray inductance taken into account as illustrated in Figure 2.

$R_{goff}$ and $L_{goff}$ shown in Figure 2 represent gate turn-off loop resistance and stray inductance respectively. For the sake of simplicity, drain-source voltage $V_{ds}$ is modeled with a ramp function where drain-source voltage increases from zero to DC-link voltage $V_{ds}$ in time interval $T_r$. The s-domain model of $V_{ds}$ is given in equation (1).

$$V_{ds1}(s) = \frac{V_{DC}}{T_r \cdot s^2} \left(1 - e^{-sT_r}\right)$$  (1)
According to Figure 2, gate-source voltage $V_{gs}$ in the s-domain is represented in equation (2) as

$$V_{gs}(s) = \frac{L_{goff} C_{gd} s^2 + R_{goff} C_{gd} s}{L_{goff} C_{iss} s^2 + R_{goff} C_{iss} s + 1} \cdot V_{ds1}(s)$$  \hspace{1cm} (2)

where $C_{iss}$ represents the input capacitance and is the sum of $C_{gs}$ and $C_{gd}$. To get an analytical solution of crosstalk voltage, $C_{gs}$ and $C_{gd}$ are assumed to be constant first. According to Figure 3, gate-source voltage $V_{gs}$ in the time-domain is given as

$$V_{gs}(t) = [f(t) + g(t)] - [f(t - T_r) + g(t - T_r)]$$

$$= a(t - T_r)$$  \hspace{1cm} (3)

Defining $\zeta$ represents the damper factor of the second order system shown in Fig. 3. When $\zeta$ is less than one, the system is an under-damped system. Then $f(t)$ and $g(t)$ is represented as

$$f(t) = \frac{C_{gd} V_{DC}}{\omega T_r C_{iss}} e^{-\alpha t} \sin(\omega t)$$  \hspace{1cm} (4)

$$g(t) = \frac{R_{goff} C_{gd} V_{DC}}{T_r} \left(1 - e^{-\alpha t} \cos(\omega t) - \frac{\omega}{\alpha} e^{-\alpha t} \sin(\omega t)\right)$$  \hspace{1cm} (5)

Attenuation factor $\alpha$ and angular frequency $\omega$ in equation (4) and (5) are given in formula (6) and (7) respectively

$$\alpha = \frac{R_{goff}}{2L_{goff}}$$  \hspace{1cm} (6)

$$\omega = \sqrt{1/ (L_{goff} C_{iss}) - \alpha^2}$$  \hspace{1cm} (7)

However, when $\zeta$ is greater than one, the system is an over-damped system. Then $f(t)$ and $g(t)$ is represented as

$$f(t) = \frac{C_{gd} V_{DC}}{2\Omega T_r C_{iss}} (e^{-(\alpha+\Omega)t} - e^{-(\alpha-\Omega)t})$$  \hspace{1cm} (8)

$$g(t) = \frac{R_{goff} C_{gd} V_{DC}}{T_r} \left(1 + \frac{2\Omega T_r C_{iss} e^{-(\alpha+\Omega)t}}{L_{goff} C_{iss} (\alpha+\Omega)^2} + \frac{2\Omega T_r C_{iss} e^{-(\alpha-\Omega)t}}{2L_{goff} C_{iss} (\alpha-\Omega)^2}\right)$$  \hspace{1cm} (9)

Angular frequency $\Omega$ in equation (8) and (9) is different accordingly and is given as

$$\Omega = \sqrt{\alpha^2 - 1/ (L_{goff} C_{iss})}$$  \hspace{1cm} (10)

### TABLE 1. Parameters used for parametric analysis.

| parameter  | unit | value |
|------------|------|-------|
| $T_r$      | ns   | 5     |
| $C_{gd}$   | pF   | 50    |
| $C_{gs}$   | pF   | 660   |
| $V_{dc}$   | V    | 48    |

B. PARAMETRIC ANALYSIS

As can be seen from equation (3) that time-domain $V_{gs}$ expression is a complicated function of excitation and other circuit parameters. However, the effects that electrical parameters have on the gate crosstalk can be revealed by means of parametric analysis. Circuit parameters used for parametric analysis are listed in Table 1, in which GaN device related parameters come from the datasheet of GS61008P manufactured by GaN Systems corporation.

According to the deduced solutions of the analytical circuit model in equations (3)–(9) and parameters given in Table I, the gate-source crosstalk voltage can be calculated out under different combination of $R_{goff}$ and $L_{goff}$ as shown in Figure 3.

In Figure 3, each solid line represents the maximal gate-source crosstalk voltage contour and each dashed line represents the contour of minimal gate-source voltage during the crosstalk induced gate ringing period. The red dash dot line shown in Figure 3 illustrates the underdamped and overdamped boundary determined by the circuit parameters. From Figure 3 the following conclusion can be drawn:

1. There is no need to design the gate turn-off loop as an overdamped system. Though large turn-off resistance can suppress the minimum gate-source voltage undershoot in the ringing period, it will increase the possibility of gate false turn-on.

2. Gate turn-off loop inductance has detrimental effects on the gate crosstalk overshoot and the accompanying ringing effect. So it’s important to optimize the layout and routing of gate turn-off loop to minimize the gate turn-off loop inductance.
(3) For a given power semiconductor, the gate threshold voltage is known. Under a given or an estimated $dV_{ds}/dt$ excitation, the combination of $R_{goff}$ and $L_{goff}$ that prevent false turn-on can be figured out by parametric analysis as illustrated in Figure 3. For GaN GS61008P, the gate minimal threshold voltage is 1.1V. If assuming the analytical circuit model is accurate, then the area encircled by the calculated 1.1V gate-source crosstalk voltage curve AB and the coordinate axes determinates all the safe combinations of $R_{goff}$ and $L_{goff}$.

Though has taken gate turn-off loop inductance into consideration, the calculated gate crosstalk voltages still divert from the experiment measurement results. Thus, for accurate gate crosstalk voltage calculation, the modeling accuracy of nonlinear parasitic capacitances and crosstalk excitation signal has to be promoted.

C. NONLINEAR SIMULATION MODEL OF FALSE TURN-ON PROBLEM

In this section, nonlinear parasitic capacitances of GaN HEMT are modeled first, then more precise gate crosstalk voltage can be calculated. Parasitic capacitance $C_{gd}$ is a nonlinear function of drain-source voltage $V_{ds}$ as widely illustrated in the device datasheets. Here, $C_{gd}$ is modeled by equation (11) as

$$C_{gd} = k_0 \cdot (1 + V_{ds} \cdot (1 + k_1 \cdot (1 + \tanh (k_2 \cdot V_{ds} - k_3))))^{-k_4}$$

(11)

where, $k_0 \sim k_4$ are fitting parameters.

The nonlinearity of capacitance $C_{gs}$ is liable to be omitted, because $C_{gs}$ given in device datasheet keeps almost constant as varying of $V_{ds}$. While it has been found that $C_{gs}$ is a highly nonlinear function of gate-source voltage $V_{gs}$ and the nonlinearity of $C_{gs}$ has a serious effect on the gate crosstalk voltage. Here, vector network analyzer E5061B with dc bias capacity is adopted to measure the gate-source impedance of GS61008P under different gate-source offset voltage. According to the measured gate-source impedance, the extracted $C_{gs}$ is illustrated in Figure 4.

![FIGURE 4. Measured and fitted nonlinear gate-source capacitance $C_{gs}$ under different gate-source voltage.](image)

| parameter | value            | parameter | value            |
|-----------|------------------|-----------|------------------|
| $k_0$     | 1.37e-10         | $a_1$     | -6.293           |
| $k_1$     | -0.405           | $a_2$     | -4.773           |
| $k_2$     | -0.252           | $a_3$     | -1.714e-12       |
| $k_3$     | -4.01            | $a_4$     | 1.574e-11        |
| $k_4$     | 0.688            | $a_5$     | 1.674e-9         |
| $a_0$     | -1.022e-9        |           |                  |

![TABLE 2. Fitting parameters of $C_{gd}$ and $C_{gs}$.](image)

![FIGURE 5. (a) Nonlinear capacitance implementation and (b) false turn-on voltage simulation model with nonlinear capacitance and gate internal resistance considered.](image)
TABLE 3. Gate crosstalk voltage under different gate circuit parameters.

| \( V_{gm} \) (V) | \( V_{ds} \) (V) | \( R_m \) (Ω) | \( R_{ds} \) (Ω) | \( T_i \) (ns) | \( V_{ds(max)} \) (V) |
|------------------|-----------------|-------------|----------------|-------------|-----------------|
|                  | measurement     | simulation  | relative error |
| 5                | 0               | 5           | 0              | 3.5         | 1               | 0.95            | 5.0%            |
| 5                | 0               | 5           | 1              | 3.5         | 1.28           | 1.18            | 7.8%            |
| -1              | 5               | 1           | 3.51          | 0.48        | 0.45           | 6.2%            |
| -1              | 5               | 2           | 3.52          | 0.72        | 0.7            | 2.8%            |
| -1              | 5               | 3           | 3.51          | 1.04        | 0.97           | 6.7%            |
TABLE 4. Fitting parameters of electrothermal output characteristics in both the first and the third quadrant.

| parameter | value     | parameter | value     |
|-----------|-----------|-----------|-----------|
| $a_1$     | 3.391e-4  | $a_5$     | 3.577     |
| $a_2$     | -1.254e-1 | $b_1$     | 1.081     |
| $a_3$     | 1.622e+1  | $b_2$     | 1.518e-1  |
| $a_4$     | 4.097e-1  | $b_3$     | 5.180e-1  |
| $a_6$     | 1.461     | $b_4$     | 1.261     |
| $a_7$     | 1.859     | $b_5$     | 9.912e-3  |
| $a_8$     | 1.6       | $b_6$     | 3.671     |

TABLE 5. Fitting parameters of $C_{ds}$.

| parameter | value     | parameter | value     |
|-----------|-----------|-----------|-----------|
| $k_0$     | 6.38e-12  | $k_4$     | -10.3     |
| $k_1$     | -0.482    | $k_5$     | 0.221     |
| $k_2$     | -0.565    |           |           |

can be accurately modeled as in equation (14)

$$I_{sd} = b_1 \left( \frac{\ln \left( 1 + e^{\frac{(V_{gd} - b_2)}{\max(b_2 V_{gd} + b_3, 1)}} \right)}{\ln \left( 1 + e^{\frac{(V_{gd} - b_4 - b_4 V_{sd})}{\max(b_2 V_{gd} + b_3, 1)}} \right)} \right)^{b_6} \cdot (1 + b_7 \cdot V_{sd})$$

(14)

where $b_1\sim b_9$ are also fitting parameters.

In this paper, output characteristics data is extracted from the datasheet of GS61008P first, then commercial optimization tool 1stopt in [23] is adopted to fulfill the parameter fitting process as listed in Table 4.

According to modeling equations (12), (13) and the fitted model parameters, the transfer and output characteristics of GS61008P under different junction temperature can be calculated out as illustrated in Figure 7.

From Figure 7, it can be seen that the electrothermal output characteristics of GS61008P in both the first and the third quadrant can be precisely modeled by the proposed modeling equations.

As to the modeling of nonlinear parasitic capacitances, the models of capacitance $C_{gs}$ and $C_{gd}$ have been constructed in section II.C. At the same time, the modeling equation of capacitance $C_{gd}$ is also applicable for the modeling of capacitance $C_{ds}$. Modeling parameters of GS61008P $C_{ds}$ are listed in Table 5.

According to the modeling parameters given in Table 2 and Table 5, the parasitic capacitances of GS61008P as function of $V_{ds}$ are illustrated in Figure 8.

From Figure 8, it can be seen that the nonlinear parasitic capacitance can be precisely modeled by the proposed modeling equations.

B. EXPERIMENT VERIFICATION AND DISCUSSION

To verify the correctness of the proposed GaN HEMT model, a half-bridge test board is designed as shown in Figure 9.

The circuit diagram corresponding to Figure 9 is the same as Figure 1. A double pulse test is carried out on the experiment board, where the current of the load inductor is charged to a preset value during the first turn-on period of the bottom GaN HEMT and gate crosstalk voltage of the top GaN HEMT will be triggered during the hard turn-on process of the bottom GaN HEMT at the beginning of the second turn-on pulse. By adopting Ansys Q3D, the top/bottom gate loop turn on/off inductances and power loop inductance can be extracted as listed in Table 6. In addition, unless otherwise stated, the default electrical parameters in the experiment are also listed in Table 6.
According to the electrical parameters in Table 6 and the constructed GaN HEMT device model, the double pulse test virtual prototype can be constructed in simulation program for integrated circuits emphasis (SPICE) simulator LTspice. To verify the correctness of the constructed virtual prototype, comparisons between the experiment measured and simulated dynamic switching waveforms during bottom GaN hard turn-on period under different top GaN gate turn-off voltages are illustrated in Figure 10∼Figure 12.

In Figure 10∼Figure 12, $V_{dsi}$, $I_{dsi}$ and $V_{gsi}(i = 1, 2)$ represent the drain-source voltage, drain-source current and gate-source current of the top GaN when $i$ equals 1 and the bottom GaN when $i$ equals 2. $V_{gsi(int)}$ represents the internal gate-source voltage of the top GaN without considering the voltage drop on the internal gate resistance, and $I_{ch1}$ represents the channel current of top GaN obtained by SPICE simulation. Before the turn-on of bottom GaN $Q_2$, top GaN $Q_1$ free-wheels the load current. So the channel current of $Q_1$ is negative at first. As the switching on of bottom GaN $Q_2$, the drain-source voltage of $Q_1$ rises up sharply, which evokes displacement current flowing through $C_{gd}$ of $Q_1$ and consequent crosstalk voltage. From Figure 10∼Figure 12, it can be seen that

(1) The virtual prototype based dynamic switching waveforms match the experiment measurement results quite well, which can effectively verify the correctness of the constructed device model, extracted parasitic parameters and circuit models. Besides, it also means that the virtual prototype can be used to calculate the crosstalk voltage and further facilitate the analysis of false turn-on problem.

(2) Based on the simulation model, the gate internal crosstalk voltages and channel current which are not measurable by experiment can be calculated, and this is valuable to determine the occurrence and seriousness of false turn-on. At the same time, in Figure 10∼Figure 12, the gate internal crosstalk voltages are larger than the measured, which shows that it’s more reliable to determine whether false turn-on has happened by simulation results. In addition, false turn-on not only increases the turn-on loss $E_{on}$ of hard switching-on device, but also brings about extra false turn-on loss $E_{cr}$, in which $E_{cr}$ can only be calculated by simulation as listed in Table 7.

From Table 7, it can be drawn that the simulated turn-on loss is in consensus with the experiment calculation, which can further verify the correctness of the constructed...
simulation model. Besides, the calculated false turn-on induced extra loss can be used as a criterion to evaluate the seriousness of false turn-on.

(3) In Figure 10 and Figure 11, crosstalk voltage has exceeded the threshold voltage of GaN, and this can be verified by the forward conducting channel currents $I_{ch1}$ in $Q_1$. As gate turn-off voltage going low, the gate false turn-on can be relieved and even averted as illustrated in Figure 11 and Figure 12, which implies that the optimal gate turn-off voltage can be determined by parameter scanning simulation.

To further verify the correctness of the constructed gate crosstalk voltage calculation SPICE circuit model, an experiment under power loop inductance $L_{ds}$ equaling 13.6nH is conducted. In which, the value of $L_{ds}$ is changed by regulating the wire length of the print circuit board (PCB) jumper in the power loop. Comparisons between the simulated and experiment measured dynamic switching waveforms are illustrated in Figure 13. Besides, an experiment under dc-link voltage equaling 70V is conducted and the experiment waveforms are shown in Figure 14.

From Figure 13 and Figure 14, it can be seen that the simulated gate crosstalk voltages are in consensus with the measurement results and the simulated dynamic waveforms match the measured results quite well, which shows that the proposed gate crosstalk voltage simulation model goes under different power loop inductances and dc-link voltages.

IV. SIMULATION BASED PARAMETRIC ANALYSIS

As the correctness of the constructed simulation model has been verified in section III above, based on the simulation model, parametric analysis will be conducted in this section to exemplify the false turn-on suppression methods.
A. OPTIMAL DESIGN OF GATE TURN-OFF RESISTANCE AND INDUCTANCE

Based on the SPICE simulation model and default electrical parameters listed in Table 6, the simulated turn-on loss $E_{on}$ of $Q_2$ and false turn-on induced loss $E_{cr}$ of $Q_1$ when gate turn-off resistance $R_{goff(ext)}$ of $Q_1$ changes in the range of $0.1$ to $10\Omega$ and gate turn-off inductance $L_{goff1}$ of $Q_1$ changes in the range of $0.1nH$ to $10nH$ are shown in Figure 15.

From Figure 15, it can be seen that false turn-on has always happened when switching $Q_1$ off with 0V voltage. $E_{cr}$ is in positive proportion with the increasing of $R_{goff(ext)}$ and $L_{goff1}$. Owing to the existence of gate internal resistance and fast turn-on speed, it’s insufficient to suppress false turn-on by decreasing $R_{goff(ext)}$ or $L_{goff1}$. At the same time, as the increasing of $R_{goff(ext)}$ or $L_{goff1}$, false turn-on induced extra loss $E_{cr}$ of $Q_1$ becomes comparable to the turn-on loss $E_{on}$ of $Q_2$ and false turn-on has also increased the turn-on loss of $Q_2$ substantially. Thus, when turning $Q_1$ off with 0V voltage, $R_{goff(ext)}$ and $L_{goff1}$ should be deliberately designed. Contour of $E_{cr}$ under different $R_{goff(ext)}$ and $L_{goff1}$ is illustrated in Figure 16.

From Figure 16, it can be drawn that the optimal design region of $R_{goff(ext)}$ and $L_{goff1}$ shown by the shaded area can be figured out once the acceptable false turn-on induced loss limitation $0.5 \mu J$ has been determined.

B. OPTIMAL DESIGN OF GATE TURN-OFF VOLTAGE

As can be seen from section IV.A that controlling $R_{goff(ext)}$ and $L_{goff1}$ can’t suppress false turn-on totally at some cases. By comparison, turning GaN off with negative voltage seems to be a more reliable method. Contours of false turn-on induced extra loss $E_{cr}$ under $V_{goff}$ equaling $-1V$ and $-2V$ are illustrated in Figure 17(a) and Figure 17(b) respectively.

From Figure 17, it can be seen that the acceptable $R_{goff(ext)}$ and $L_{goff1}$ region increases as the decreasing of the negative turn-off voltage. Thus, the PCB design difficulties of gate loop can be relieved. However, as the negative turn-off voltage will increase the deadtime free-wheeling loss, optimal turn-off voltage should be determined according to the acceptable maximum $E_{cr}$ and preset $R_{goff1} - L_{goff1}$ design region. As illustrated by the shaded area in Figure 17(b), if $E_{cr}$ should be controlled below $0.01\mu J$ and the gate turn-off inductance will be designed to be as large as $6nH$, then gate turn-off voltage should be optimally controlled to be no more than $-2V$.

C. OPTIMAL DESIGN OF POWER LOOP STRAY INDUCTANCE

Under given gate driving condition, power loop stray inductance $L_{ds}$ will determine the rising speed and peak of drain-source voltage $V_{ds}$ known as false turn-on exciting source as mentioned above. Thus, the effect that $L_{ds}$ has on false turn-on must be investigated considerably.

Based on the default experiment parameters listed in Table 6 and the constructed simulation model, the simulated $E_{cr}$, $E_{on}$ and the sum of both $E_{cr}$ and $E_{on}$ under different $R_{goff(ext)}$ and $L_{ds}$ are illustrated in Figure 18.

From Figure 18, it can be seen that the severity of false turn-on deteriorates as the increasing of $L_{ds}$ especially when $R_{goff(ext)}$ is large. Though $E_{on}$ decreases as the increasing of $L_{ds}$, $E_{cr}$ has increases to an extent comparable to $E_{on}$. Considering that large $L_{ds}$ also causes large turn-on and turn-off overvoltage as in [8], [21], [24], [25], thus $L_{ds}$ should be controlled as small as possible by optimal PCB layout and routing of power loop at the very beginning of power converter design.

V. CONCLUSION

This paper has proposed a comprehensive false turn-on problem analysis and suppression method in GaN HEMT phase-leg topology. False turn-on analytical method and its deficits have been analyzed first, based on which a more precise false turn-on circuit model is proposed with gate-source nonlinear capacitance accurately modeled and gate internal parasitic resistance taken into consideration. For the accurate modeling of false turn-on excitation, an accurate GaN HEMT electrothermal behavior model has been proposed further, based on which GaN HEMT half bridge...
SPICE simulation model is constructed. Experiment results show that the constructed simulation model can calculate the false turn-on accurately. Besides, based on the constructed circuit model, false turn-on suppression by optimal design of gate driving electrical parameters and power loop stray inductance by parametric analysis can be implemented.

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