HARDWARE DESIGN AND IMPLEMENTATION OF MICROCONTROLLER BASED REDUCED SWITCH MULTILEVEL INVERTER TOPOLOGY FOR HARMONIC STUDIES USING MRPWM

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ABSTRACT: Multilevel inverter (MLI) is the recent advancement in power electronics which employed to synthesize a high-quality output voltage waveform. This paper focuses on developing a single phase modified nine-level inverter with the reduced number of switches for improving the quality of output voltage waveform. Single carrier and multireference Pulse Width Modulation (PWM) technique is utilized for generating the switching pulses. The proposed topology consists of a single DC source, level generation part (balancing capacitor and bidirectional switches) and polarity generation part (H-Bridge). The operation of the proposed topology is examined for generating 9-level output voltage using MATLAB/SIMULINK. The result of the proposed topology is verified through laboratory-based prototype model. For experimental setup, the switching pulses are generated by PIC16F877A microcontroller. This proposed lab experimental and simulation can be used to study the value of %THD at output side of the inverter.

Keywords: Multilevel Inverter Cascaded H-Bridge Multilevel Inverter, Total Harmonic Distortion, Multi Reference Pulse Width Modulation, Microcontroller

I. INTRODUCTION
MLIs has many attractive features as compared with two-level inverter such as low switching losses, low electromagnetic interference and capable of generating the quality output voltage waveform (Najafi and Yatim, 2012; Hinago and Koizumi, 2010). The conventional MLI topologies are Cascaded H-Bridge MLI (CHBMLI), Diode Clamped Multilevel Inverter (DCMLI) and Flying Capacitor Multilevel Inverter (FCMLI) (Jami et al, 2014) FCMLI and DCMLI require a high number of clamping capacitors and clamping diodes, which are heavy and bulky as the level increases. CHBMLI does not require clamping capacitors and clamping diodes, but it requires separate DC sources for generating the required output voltage level. The main drawbacks of conventional MLIs are utilizing the higher number of components
such as power semiconductor switches, clamping diodes and balancing capacitors. Therefore, it reduces the reliability of the inverter (Jami et al, 2014; Panda and Mohapatra, 2019; Naggar and Abdelhamid, 2008) CHBMLI involves a series connection of single-phase H-Bridge inverter which generates the medium output voltage levels by utilizing the low voltage components. Depending upon the output voltage levels, the number of H-Bridge can be connected in series, which leads to increase in the utilization of power semiconductor switches (Najafi and Yatim, 2012; Hinago and Koizumi, 2010). To overcome the drawbacks mentioned above, a new topology is developed with a reduced number of switches for generating the required output voltage level. Compared with conventional MLI, the proposed topology requires a minimum number of semiconductor devices to achieve the same number of output levels. As a result, the %THD of output voltage waveform is reduced, and thus, the quality of the waveform could be improved.

Several modulation and control techniques have been adopted for MLI, which includes sinusoidal PWM, Space Vector Modulation (SVM), and Selective Harmonic Elimination (SHE) (Tolbert and Habetler, 1999). SPWM is generally employed for its simplicity and less control complexity. The different carrier arrangement in SPWM techniques are Phase Disposition PWM (PDPWM), Phase Opposition Disposition PWM (PODPWM), Alternate Phase Opposition Disposition PWM (APODPWM) and Carrier Overlapping PWM (COPWM) (Gupta and Jain, 2014). To obtain lower %THD, the overmodulation technique has adopted and thereby reducing the size of passive filters (Mohammed et al, 2018) A new modulation method known as Variable Amplitude Phase Shifted PWM (VA-PSC-PWM) has employed in micro grid connected CHBMLI, which provides superior THD profile (Biswas and Khan, 2017). Some investigators (Podder et al, 2016), describe the carrier signal is modified to reduce the duration of the volt-sec output of the CHBMLI. By reducing the volt-sec output, the output voltage becomes near sinusoidal and reduces harmonic content drastically (Harbi et al, 2018). A low frequency transformer based reduced switch cascaded H bridge MLI has been presented (Khounjahan et al, 2015). SHEPWM technique has been employed in the developed topology to mitigate lower order harmonic component (Khounjahan et al, 2015). In a discussion (Suroso et al 2017), SPWM method has been employed with low pass filter. This method has utilized two triangular waves and two sinusoidal waveforms with opposite phase to generate the triggering pulses for five-level reduced switch inverter with a voltage balancing circuit. SHE method has used to mitigate the third and fifth harmonic components. Newton Raphson method has employed to solve the nonlinear equations (Gobinath et al, 2013) Phase Shift PWM (PSPWM) method requires ‘(n-1)/2’ carriers for ‘n’ level inverter. Triggering pulses have been generated by comparing the sinusoidal reference wave with the carriers, which are phase shifted each other by an angle of $360^\circ/[(n-1)/2]$. In modified PSPWM method, two sets of carrier waveforms have been used where one set has the magnitude from 0 to 1 and another set has the magnitude from 0 to -1 and phase shifted by 180° with respect to first set. These carriers have been compared with a bipolar sinusoidal waveform. It is discussed in one article (Kirthika Devi and Srivani, 2017), the modified PSPWM method provides lower THD when compared to conventional PSPWM. In order to obtain the desired 5 level output, two reference sine wave and one carrier wave have been utilized (Panchal et al, 2014). Level shifted Phase Disposition technique has been chosen for the developed reduced switch MLI in (Shuvo et al, 2019).

Multiple Reference PWM (MRPWM) technique is adopted for generating the switching pulses in proposed MLI. In this technique, multiple unipolar sinusoidal reference signals with a single carrier are utilized. This PWM technique requires ‘(n-1)/2’ reference signals for generating ‘n’ number of levels. The reference signals have the same frequency, same
amplitude, and in phase with each other, but it have offset by a value equal to the magnitude of carrier signal (Rajalakshmi and Rangarajan, 2016). A single-phase reduced switch MLI is proposed to reduce the harmonic content in the output voltage. It operates in both high and low frequency switching, which cause improves efficiency, reduce the capital and maintenance cost. Also, it has some additional benefits such as the minimum number of switches, utilizing a single DC source for generating the required output voltage level, high efficiency, low cost and simple control scheme as compared with conventional PWM method. The proposed topology could be employed in different high and medium power applications such as HVDC, FACTS and UPS.

II. PROPOSED MLI TOPOLOGY

MLIs have some important features such as improved staircase waveform, reduction in common mode voltage, low distortion and there exists no EMI problem. The number of levels is indirectly proportional to \%THD, and the number of power semiconductor device is directly proportional to the number of levels. A block diagram for the proposed topology is shown in Fig. 1 which comprises of DC source, reduced switch MLI with balancing capacitor, single carrier multi reference PWM and load. MRPWM (Multi Reference Pulse Width Modulation) technique is used to generate the switching pulses for the required output voltage level with reduced harmonic content.

![General block diagram for the proposed work](image)

The proposed topology is shown in Fig. 2. It consists of single-phase cascaded H-bridge inverter (\(S_1, S_2, S_3\) and \(S_4\)), three bidirectional power semiconductor switches (\(S_5, S_6, S_7\)) and four capacitors (\(C_1, C_2, C_3\) and \(C_4\)). The bidirectional power semiconductor switch consists of the combination of a single switch and four diodes. The phase output voltage level is given by,

\[
N = 2n+1
\]

Where ‘n’ represents the number of capacitors, and ‘N’ represents the number of levels. The switching combinations for generating the nine-level output voltage, is shown in Table 1. Comparison of the number of components utilized in the proposed inverter is compared with the components used in the conventional MLIs for generating nine-level output voltage is given in Table 2. In the proposed MLI, each bidirectional switch consists of one transistor and four diodes. For example, generating a 9-level output voltage requires three bidirectional switches. Here, bidirectional switch consists of one switch with four diodes.
**2.1 PRINCIPLE OF OPERATION**

The different modes of operation for generating the nine-level output voltage are shown in Fig. 3. Fig. 3a to Fig. 3i show that the current flow path in different mode of operation using a solid line. The voltage across each capacitor is \( V_{dc}/4 \). In mode 1, the power semiconductor devices \( S_1 \) and \( S_4 \) are conducting and the remaining devices are in OFF state. The voltage available across the capacitors \( (C_1, C_2, C_3 \text{ and } C_4) \) is \( V_{dc} \) which appears across the load. In mode 2, the conducting devices are \( S_3 \) and \( S_4 \). The capacitors \( C_2, C_3 \text{ and } C_4 \) are connected across the load. Therefore, the voltage available at the load is \( (3V_{dc}/4) \). In mode 3, the power semiconductor devices \( S_6 \) and \( S_4 \) are turned on. The capacitors \( C_3 \text{ and } C_4 \) are connected across...
the load. The voltage available at the load is \( V_{dc}/2 \). In mode 4, the power semiconductor devices \( S_7 \) and \( S_4 \) are turned on. Only the capacitor \( C_4 \) is connected across the load and the current flow path is shown by the solid line. The voltage available across the load is \( V_{dc}/4 \). In mode 5, \( S_3 \) and \( S_4 \) are conducting so that the load is short circuited. Therefore, the voltage available across the load is zero. In mode 6, the negative polarity output voltage can be obtained when the devices \( S_5 \) and \( S_2 \) are turned on. The voltage available at the output is \(-V_{dc}/4\). In mode 7, \( S_6 \) and \( S_2 \) are turned on so that the load voltage is equal to \(-V_{dc}/2\). Similarly, the \( S_7 \) and \( S_2 \) power conductor switches are turned on in the 8th mode whereas the \( S_2 \) and \( S_3 \) are conducted in the 9th mode. The voltage across the load in 8th and 9th mode is \(-3V_{dc}/4\) and \(-V_{dc}\) respectively.
III. MULTI REFERENCE PULSE WIDTH MODULATION TECHNIQUE

Multiple Reference PWM technique (Jayapalan and Edward, 2017) is used for generating the switching pulses of the proposed MLI topology. Here, single triangle carrier and multiple unipolar sine reference are adopted in the pulse generation. Here, an ‘N’ level inverter requires ‘(N-1)/2’ reference signals with the same amplitude and frequency which are in phase. But these signals have an offset whose value is equal to the magnitude of carrier signal. Therefore, a nine-level inverter requires four reference signals and a single carrier signal. The pulses are generated by comparing the reference signals $V_{ref1}$, $V_{ref2}$, $V_{ref3}$ and $V_{ref4}$ with a carrier signal as shown in Fig. 4.

The reference voltage $V_{ref1}$ is compared with a carrier signal and a pulse is generated when its amplitude exceeds the carrier signal. $V_{ref1}$ is compared with the carrier signal till $V_{ref2}$ exceeds the carrier signal. Similarly, $V_{ref2}$ exceeds the carrier signal which generates pulses till $V_{ref3}$ exceeds the carrier signal. This procedure is repeated for generating the switching pulses to all the power semiconductor switches. Fig. 5 shows the switching pulses for the proposed topology switches. The modulation index for multi reference PWM is given by,

$$M = \frac{A_r}{A_c}$$  \hspace{1cm} (1)  

where ‘$A_r$’ is the peak to peak value of the reference signal and ‘$A_c$’ is the peak value of the carrier signal. The phase displacement for modulation index more than 0.75 is determined by referring the article (Jayapalan and Edward, 2017).
\[ \theta_1 = \sin^{-1}\left( \frac{A}{A_r} \right) \]  

(2)

For a reference wave whose amplitude is 5 times the triangular carrier, the angle \( \theta_1 \) is calculated as follows

\[ \theta_1 = \sin^{-1}\left( \frac{1}{5} \right) = 11.54^\circ \]  

(3)

Similarly, the remaining angles can be calculated using the following formula

\[ \theta_2 = \sin^{-1}\left( \frac{2A}{A_r} \right) \]  

(4)

\[ \theta_3 = \sin^{-1}\left( \frac{3A}{A_r} \right) \]  

(5)

\[ \theta_4 = \sin^{-1}\left( \frac{4A}{A_r} \right) \]  

(6)

\[ \theta_5 = \pi - \theta_4 \]  

(7)

\[ \theta_6 = \pi - \theta_3 \]  

(8)

\[ \theta_7 = \pi - \theta_2 \]  

(9)

\[ \theta_8 = \pi - \theta_1 \]  

(10)

The theoretical waveform of nine-level output voltage with the corresponding switching angles is shown in Fig. 6.
IV. SIMULATION AND EXPERIMENTAL RESULTS
The simulation model for proposed MLI using MATLAB is shown in Fig 7. The switching pulses are generated using Multi Reference and single carrier PWM technique. The carrier switching frequency is 1K Hz. The simulation parameters are as follows input voltage (DC source value) = 230 V, capacitor = 470 µF and load resistance = 100 Ω and L=100 mH. The 9-level output voltage waveform and its FFT spectrum for proposed MLI are shown in Fig. 8 and 9 respectively. The %THD of the output voltage waveform is 16.34%. Fig. 10 shows the load current waveform.
Fig. 7. Simulation Diagram for proposed MLI

Fig. 8. 9-level output voltage waveform for proposed MLI

Fig. 9. FFT Analysis for proposed MLI
Fig. 10. Load current waveform for proposed MLI

Fig. 11 shows the laboratory based experimental setup of the proposed MLI. The supply is fed to rectifier which converts AC into DC power using a diode bridge rectifier. The obtained output is fed to a proposed MLI that converts DC into AC power. PIC16F877A microcontroller is utilized for generating the switching pulses in the experimental setup. Fig. 12(a-g) show the switching pulses are obtained from the PIC16877A which are fed to the proposed MLI switches through the driver circuit. In experimental setup, %THD is obtained using power quality analyzer. Fig. 13 and Fig. 14 show the experimental 9-level output voltage and its corresponding FFT analysis respectively. The %THD obtained from the experimental prototype using power quality analyzer is compared with the simulation results using MATLAB as shown in Table 3. The %THD attained from the hardware setup is 22.76% whereas the %THD achieved from the simulation is 16.34%.

Table 3 Comparison of %THD for 9-level output voltage

| S.NO | Type   | %THD |
|------|--------|------|
| 1    | Simulation | 16.34 |
| 2    | Hardware  | 22.76 |

Fig.11. Experimental Prototype of Hardware
Fig. 12. PWM pulses using microcontroller: (a) Switch S₁ (b) Switch S₂ (c) Switch S₃ (d) Switch S₄ (e) Switch S₅ (f) Switch S₆ (g) Switch S₇

Fig. 13 Experimental Result: (a) Hardware Prototype with output voltage (b) 9-level output voltage waveform for the proposed MLI

Fig. 14 Output voltage FFT Analysis for proposed MLI

V. CONCLUSION
The reduced switch MLI topology has been proposed and its operation has been examined for generating the 9-level output voltage in both simulation and experimental setup. MRPWM technique has employed for generating the switching pulses for the proposed MLI. The main feature of this proposed technique is that it has only one carrier and multiple unipolar sinusoidal reference waveforms. The %THD of output voltage is 16.34% and 22.76% in
simulation and experimental results respectively. As a result, the proposed topology provides better quality of output voltage waveform with reduced harmonic content. As there is a growing concern over power quality, this experimental setup may be utilized in power electronics laboratories as harmonic study purpose.

REFERENCES

[1] Bayat Z & Babaei E (2012 February) A new cascaded multilevel inverter with reduced number of switches. In: Power electronics and drive systems technology (PEDSTC), 2012 3rd (pp. 416–421) IEEE

[2] M M Biswas and M Z R Khan Amended THD with modified phaseshifted PWM for micro-grid connected multilevel inverter in Proc. IEEE Power Energy Conf Illinois (PECI) Feb 2017 pp 1-6

[3] K Gobinath S Mahendran and Dr I Gnanambal Novel cascad-ed H-Bridge multilevel inverter with harmonics elimination Pro-ceedings of 2013 International Conference on Green High Perfor-mance Computing IEEE 2013

[4] K K Gupta and S Jain A novel multilevel inverter based on switched DC sources IEEE Trans Ind Electron vol 61 no 7 pp 3269-3278 Jul 2014

[5] A Harbi Haitham Z Azazi Azza E Lashine and Awad E Elsabbe A higher levels multilevel inverter with reduced number of switches International Journal of Electronics 2018 VOL 105, NO 8 1286–1299

[6] Y Hinago H.Koizumi A single Phase Multilevel Using Switched Series/Parallel DC Voltage Sources IEEE Trans. Industrial Electronics Aug.2010 vol 57 no. 8 pp 2643-2650

[7] A Jami MRJ.Oskuee A Mokhberdoran A Van den Bossche Developed cascaded multilevel inverter topology to minimize the number of circuit devices and voltage stress of switches IET Power Electronics Feb 2014 pp 459-466

[8] Gowrishankar Jayapalan and Belwin Edward, “Implementation of 9-Level Hybrid Inverter using Multi Reference Pulse Width Modulation Technique with Flyback Converter for Photovoltaic System International Journal of Control Theory and Applications 2017

[9] V S.Kirthika Devi S G Srivani Modified phase shifted PWM for cascaded H Bridge Multilevel Inverter IEEE 2017

[10] H Khounjahan M R Banaei Amir Farakhor A new low cost cascaded transformer multilevel inverter topology using minimum number of components with modified selective harmonic elimination modulation Ain Shams Engineering Journal (2015) 6, 67–73

[11] Malinowski M Gopakumar K Rodriguez J Marcelo AP A survey on cascaded multi level inverters IEEE Trans. Ind. Electron. 2010 57 2197–2206

[12] Mustafa Fawzi Mohammed Ali Husain Ahmad AbdulRahim Thiab Humod Harmonics reduction of a five-level inverter by unbalanced car-riers and over-modulation techniques International Journal of Engineering & Technology 2018

[13] Naggar E N Abdelhamid T.H. Selective harmonic elimination of new family of multilevel inverters using genetic algorithms. Energy Convers. Manag 2008 49 89–95

[14] E.Najafi A.H.M.Yatim Design and Implementation of a New Multilevel Topology IEEE Trans Industrial Electronics Nov 2012 vol 59 no 11 pp 4148-4154

[15] Panda KP Mohapatra SK Anti-predatory PSO technique-based solutions for selected harmonic elimination in cascaded multilevel inverters Int J Ind Electron. Drives 2016 3 78–88
[16] Leon M Tolbert and Thomas G. Habetler Novel multilevel inverter carrier based PWM method IEEE Transaction On Industry Application Vol 35 No 5 Sep 1999 pp 1098-1107

[17] S Podder M Biswas and Z R. Khan A modi_ed PWM technique to improve total harmonic distortion of multilevel inverter in Proc. 9th Int Conf Elect Comput Eng (ICECE) 2016 pp 515-518

[18] Tejas M Panchal Rakesh A Patel Hiren S Darji Simulation of Modified Cascaded H-Bridge Multilevel Inverter for 3-Phase Asynchronous Motor IEEE 2014.

[19] J.Rodriguez Jih-Sheng Lai,Fang Zheng Peng Multilevel inverters: A survey of topologies controls and applications IEEE Trans. Industrial Electronics Aug.2002 vol.49 pp 724-738

[20] Sambasivam Rajalakshmi and Parthasarathy Rangarajan Analysis of Reduced Switch Topology Multilevel Inverter with Different Pulse Width Modulation Technique and Its Application with DSTATCOM Circuits and Systems 2016 7 2410-2424.

[21] Shuvangkar Shuvo Eklas Hossain Tanveerul Islam, Abir Akib Sanjeevikumar Padmanaban and Md Ziaur Rahman Khan Design and Hardware Implementation Considerations of Modified Multilevel Cascaded H-Bridge Inverter for Photovoltaic System IEEE Access 2019

[22] Suros Abdullah Nur Aziz and Toshihiko Noguchi Five-level PWM inverter with a single DC power source for DC-AC power conversion International journal of power electronics and drive system IJPEDS Vol 8 No 3 2017 pp 1230-1237

[23] Manjusha S Nair and Dr. A.Rajaram, Low power receiver using envelope Detector converters International Journal of Advanced Information Science and Technology, 3(3): 50-57, March 2014