PASCAL: Timing SCA Resistant Design and Verification Flow

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Abstract—A large number of crypto accelerators are being deployed with the widespread adoption of IoT. It is vitally important that these accelerators and other security hardware IPs are provably secure. Security is an extra functional requirement and hence many security verification tools are not mature. We propose an approach/flow – PASCAL – that works on RTL designs and discovers potential Timing Side Channel Attack (SCA) vulnerabilities in them. Based on information flow analysis, this is able to identify Timing Disparate Security Paths that could lead to information leakage. This flow also (automatically) eliminates the information leakage caused by the timing channel. The insertion of a lightweight Compensator Block as balancing or compliance FSM removes the timing channel with minimum modifications to the design with no impact on the clock cycle time or combinational delay of the critical path in the circuit.

I. INTRODUCTION

Security is not a first class citizen in (hardware) design and is rarely considered during design space exploration. Bugs or vulnerabilities can originate from design flaws, some of which can be fully eliminated after a complete verification. The goal of the adversary in a security critical application, is to learn information that one has no legitimate access to, e.g. the classified data or secret keys. Novel attack vectors like side-channel analysis rely on design features, to build efficient exploits that undermine assumptions regarding the accessibility of internal secret information in a computing system. For example, Timing Driven Attacks exploit timing differences in execution traces as the information flow is via different paths with the same start and end nodes (controllable and observable) to derive the secret information.

Denning et. al. introduced the concept of secure information flow in a computer system whereby it can be shown that no unauthorized flow of information is possible due to control and data flow [1]. However, in recent years, side channels or out of band data channels have been exploited to exfiltrate or deduce secret information. Consequently, Information Flow Tracking (IFT) has evolved and has been used as a formal methodology for modeling and reasoning about security properties related to integrity, confidentiality of side channels. The problem becomes more interesting and hard because high-level architecture abstractions are translated into transparent micro architecture implementations. While the hardware behavior in the micro-architecture can cause additional information flows which can be gainfully exploited to form these side channels.

As opposed to physical Side Channels Attacks (SCA) like differential power attacks etc. that require physical access to the computer system, Timing SCA can be launched (relatively) easily on general purpose compute environments that contain a memory hierarchy or performance enhancing microarchitecture features like speculative execution. The key invariant in these attacks is that there are different timing paths that provide out of band information. Security path verification addresses a specific, important aspect of overall security verification by checking access to the secure data on the hardware to make certain that attackers access the secure (secret) data through illegal logic paths. For example, in Figure 1 there are paths from A to B which is controlled by the node S containing the secret. Tools do Taint Propagation/Taint Analysis, which is a conservative approximation of secure information flow analysis, to find such paths [2]. A timing side channel exists, if the contents of S can be derived/deduced by analyzing time of arrival of K at N. We call these two or more paths with unequal transit time as Timing Disparate Security Paths. And these Timing Disparate Security Paths will be potentially vulnerabilities open for a timing side channel exploit.

The primary contribution of our work is a secure automated digital design flow – PAth based Side Channel AnaLysis (PASCAL) – that creates a secure IP core or system-on-chip. The proposed flow starts from the RTL design and the threat model and uses a state of the art Security Path verification tool to identify potential timing side channel vulnerabilities and proposes a method to remove them by enforcing uniform timing to remove data dependent instruction cycle count variations in the timing side channels.

The remainder of the paper is organized as follows. Section III summarizes the state of the art in this area. The next section details the approach used and presents the key algorithmic contribution in this work for identifying Timing Disparate Security Paths.
Security Paths while Section IV presents a lightweight method for Timing SCA Resistant Design using the results of the method proposed in the previous section. Section V describes the implementation results on a widely used crypto core and also demonstrates the efficacy of the proposed mitigation method. Section VI summarises the contributions of the paper and provides directions for future work.

II. RELATED WORK

Timing side channel attacks are known to be a hard and a very important problem in modern systems. They have been used to extract cryptographic secrets from running systems. Even differential privacy systems are not immune to these attacks. And these are possible using both remote and local adversaries. Koeune et al. present an in-depth tutorial on Side Channel Attacks [3].

A popular approach for defending against both local and remote timing attacks is to ensure that the low-level instruction sequence does not contain instructions whose performance depends on secret information. This can be enforced by manually re-writing the code, as was done in OpenSSL, or by changing the compiler to ensure that the generated code has this property [4].

While methods for high performance design or low power are available, design for security is still ad-hoc. Only recently, systematic methods support design for trust and security have been described in literature [5]. Menichelli et al. present an exploration approach centered on high level simulation based on SystemC to suggest improvements in the knowledge and identification of the weaknesses in cryptographic algorithm implementations [6]. Ardeshiricham et al. have proposed an information flow based method for secure hardware design [7] by analyzing all logical code flows of the RTL code. In contrast, VeriCoq-IPT converts designs from HDL to Coq to analyze a formal security properties [8]. SecVerilog requires explicit annotating each variable in the design with a security label — this is similar to using a type system to track information flow in the code [9]. Deng et al. have proposed a Computation Tree Logic to model execution paths of the processor cache logic and derive formulas for paths that can lead to timing side-channel vulnerabilities [10].

Most of the mitigation techniques that have been proposed try to remove data dependent instruction cycle count variations by balancing timing or do a power flattening to remove power peaks/anomalies [11]. In some cases, Pipeline randomization as a mechanism to increase NoC resilience has also been proposed [12]. Recently, Jiang et al. have proposed a high-level synthesis (HLS) infrastructure that incorporates static information flow analysis to remove timing channels in a verifiable manner on HLS-generated hardware accelerators [13].

The methodology proposed in this paper is based on a formal method that can identify all Timing Disparate Security Paths at RT level and improve the state of the art is a simple mitigation scheme for potential SCA vulnerable timing channels.

In the next section, we discuss the proposed method for discovering Timing Disparate Security Paths in RTL designs.

III. METHODOLOGY

Hardware implementations of encryption algorithms are being increasingly used as hardware is regarded as more effective root of trust. RSA is a symmetric cryptographic algorithm and has been shown to be vulnerable to Timing SCAs and mitigation techniques have also been proposed. However, the major focus continues to rely on verifying the correctness of encryption algorithms and their implementation in software and hardware. We present an approach based on RT level analysis that allows a precise understanding of possible flows for side channels based on timing. The methodology relies on a formal analysis tool Cadence JasperGold Security Path Verification App (JG SPV) [14]. The original objective of the tool is for security verification by checking access or leak of the secure data on the hardware to make certain that the attacker cannot breach the authentication logic and seek the secure data through illegal paths.

Based on a formal method of path sensitization from the secret information to the output observable points, we propose a method that can detect possible Timing-Disparate Paths in RTL designs which could be exploited as Timing Side Channel(s). As a result of this analysis, a simple and effective retiming of Timing SCA sensitive paths is proposed to make the design immune for the threats under the chosen threat model. We illustrate this on a standard RSA RTL Verilog code.

Algorithm 1: Example: RSA Modulus Code

Input: $C_m, P_n$; // $C$ is the $m$ bits cipher text, $P$ is the $n$ bits private key

Output: $O_m$; // $O$ is the $m$ bits output plain text

1. $R_0 \leftarrow \text{Montgomery}(C_m)$ and $R_1 \leftarrow \text{Montgomery}(1)$
2. $j \leftarrow 0$
3. while $j \leq n - 1$
4. \hspace{1em} $R_0 \leftarrow \text{Montgomery}\_\text{Reduction}(R_1 \ast R_1)$
5. \hspace{1em} if $P[j]$ then
6. \hspace{2em} $R_0 \leftarrow \text{Montgomery}\_\text{Reduction}(R_0 \ast R_1)$
7. \hspace{1em} end
8. $O_m \leftarrow \text{Montgomery}^{-1}(R_0)$
9. end

The decryption of the RSA modulus in Algorithm [1] uses Montgomery modular multiplication with square-and-multiply algorithm. Here we did not mention the details about how to choose the key or how the Montgomery algorithm works but focus on explaining the unintended timing channels in RSA which can be used by attacker to reverse the private key. In Algorithm[1], n, the bit number of $P_n$, decides total loop times while value of single bit of $P_n$: $P[j]$ determine the operations for each single loop – only when $P[j]$ equal to 1, statements at Line 5, 6, 7 will be executed while $P[j]$ equal to 0 will not. For the decryption of RSA, the total operations need to be executed might be different with different private key due to the above reasons. Assuming the time for single bit $P[j]$ is
The final execution time will be \( t_{total} = \sum_{j=0}^{n} t_{P[j]} \). Thus keys with different number of '1s' will cause the different execution time. This will open a timing side channel for the attackers.

For this Timing SCAs, the PASCAL is shown in figure 2. Firstly, we use JG SPV to analyze if there is one or several paths, from a variable deemed to be secure and unobservable to the output, exist. JG SPV uses a special path sensitization technology implying taint analysis to find if private key \( P \) can be propagated to the output \( O \). Then if the path exist, JG SPV will give a counterexample along with an execution trace detailing: the exact number of clock cycles (say X). As shown in the figure 3, the example shows waveforms of related signals along the path. We use the command "\( \text{get\_property\_info\_list}\{\text{max\_length}\} \text{\_property\_exponent\_to\_finish}\)" to get the total execution time (clock based) of an exist path for this specified secure signal pair. Here it needs 44 clock cycles (additional 2 clock cycles are for setting up) to propagate. After that, JG SPV will be used to find another functional path (if it exists) from \( P \) to the output \( O \) with a time length different from X cycles. This is achieved by invoking JG SPV on a modified design, shown in Figure 4. A counter is added which drives the multiplexer to select the situation where the DUV both finish the decryption AND also the length of the execution trace \( Y \) is not equal to X. If JG SPV finds another path with an execution trace length not equal to X and Y, it is added to the Union Clause of the multiplexer select condition and the process is repeated until they find all the timing classes.

![Fig. 2: PASCAL: Graphical Representation](image)

IV. TIMING SCA SECURE DESIGN FLOW

We also propose a method that aims to achieve timing-sensitive noninterference for the synthesized design, via which it is ensured that confidential or secret values cannot be revealed by the observing/measuring the timing of events at observable ports. An intuitive method to remove this Timing SCA vulnerability is to insert additional registers in the faster paths using path-balanced scheduling [15]. However, as shown in Figure 1, there could be many paths \( t_1, t_2, \cdots, t_n \) in the same basic block. Assume without loss of generality, that there are \( n/2 \) paths each differing by one cycle. Hence a path balanced scheduling synthesis procedure would insert \( 1 + 2 + 3 + \cdots + n/2 \) or \( O(n^2) \) registers.

We enable the output port/interfaced every \( t_{max} \) cycles using a counter and an AND gate. This small additional circuitry acts as the Compensator or balancing/compliance FSM and provides the (read) enable / data ready signal for observable interface.

This therefore, leads to a very simple synthesis technique for ensuring a path balanced design with a single lightweight Compensator Block at the observable points of interest in the design. The additional circuit has a very small overhead counter which counts up to \( t_m \) to generate the control input for the AND gate which provides the enable signal to the observable register. The counter is reset every time a new input enters the basic block. This additional logic incurs no penalty in the critical path of the system and avoids resource duplication since it has a uniform counter where the results from the different Timing Disparate Security Paths are delivered to the observable interface with the same latency.

V. RESULTS

The Montgomery modular multiplication with square-and-multiply algorithm based RSA cryptographic RTL implemen-
Our method can correctly identifies all timing classes using formal methods. i.e. for the 32-bits RSA verilog implementation, it identifies all the timing classes with cycle times from 33 to 64. As for the mitigation method mentioned in Figure 5. Since the counter need to count to 64, we only need a 7 bits counter which incurs an approximate area penalty of 7 flops. In contrast, the path-balanced scheduling strategy would require about 512 flip flops. Clearly, with a 64-bit RSA, the savings are more significant. As mentioned earlier, the Compliance State Machine is not in the critical path and incurs no penalty in the operational speed of the circuit.

Fig. 5: Normalized Execution Times

VI. CONCLUSION

Significant numbers of hardware IPs or crypto accelerators are being deployed with the widespread adoption of IoT. It is vitally important that these IPs are provably secure. We have proposed a novel approach to discover timing SCA vulnerabilities that (can)exist in designs. This flow also (automatically) eliminates the information leakage caused by the timing channel. The insertion of a lightweight Compensator Block removes the timing channel with minimum modifications to the design with no impact on the clock cycle time or combinational delay of the critical path in the circuit. For the future work, multiple secrets in design or multiple public interfaces will be studied. And we will also integrate this framework to High Level Synthesis flow so that more accurate estimates of area can be obtained.

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