Research on Trench Etching and Photolithography Process of SiC Trench MOSFET

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Abstract. In this paper, the development of trench etching process and photolithography process for 6-inch 4H-SiC trench-type power MOSFET devices is mainly studied. Among them, the etching process successfully solved the anisotropy of dry etching of SiC, the different etching rates of different crystal planes, the difficulty of controlling the angle of the trench sidewall, and the easy formation of micro-trenches at the corners, etc. Successfully realized trenches with etch depth greater than 1.2μm and sidewall angle greater than 90° in SiC. Subsequently, the trench was filled with SiO2 to achieve no holes in the trench after filling, and then the photolithography process was studied. Photolithography process is resolved at the trench coating, exposing and developing the non-uniformity problem, achieve a full and uniform coating, self-aligned trench overlay and the overlay accuracy of less than 0.1μm, and there is no residue of photoresist in the groove after development. This article uses scanning electron microscope (SEM) to measure the morphology of the trench after etching and photolithography to characterize the experimental results, and the results meet the process requirements. The successful development of this process will facilitate the research and development of deeper trench-type power MOSFET devices.

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1. Introduction
Silicon carbide (SiC) material is currently recognized as a new type of semiconductor material in the world. It has the advantages of wide band gap, high thermal conductivity, high breakdown field strength, high saturated electron drift speed, strong radiation resistance and stable chemical properties [1-4]. In the field of high-voltage, high-frequency, high-power, high-irradiation, and certain wavelengths of photoelectric detection technology. Therefore, the SiC device is a typical representative of the next generation of semiconductor devices, is a green energy device that will drive the future new energy technology revolution, and is the core of future power electronic equipment competition. Commercial SiC substrates are produced by cutting boules grown by the sublimation method [5, 6].
SiC MOSFET is one of the typical SiC power devices. It is a voltage-controlled unipolar transistor that controls the drain current through the gate voltage. Therefore, one of its distinguishing features is the simple driving circuit and low driving power. Power MOSFET is mainly used as a switching device. Because it is a multi-sub-device, its switching power consumption is relatively low, but its dynamic power consumption is relatively high. To reduce the dynamic power consumption of the device, it must be effectively reduced. Its own on-resistance. Traditional MOSFET devices are usually designed as a longitudinal double-diffusion structure. This structure leads to a higher breakdown voltage, which requires a larger thickness and lower doping concentration of the drift layer. However, as the breakdown voltage increases and the doping concentration of the drift layer continues to decrease, the thickness also increases continuously, resulting in an increase in on-resistance and an increase in power consumption. The relationship between breakdown voltage $B_v$ and on-resistance $R_{on}$ is $R_{on} \propto B_v^{2.5}$. The relationship between the two greatly limits the application of MOSFET devices in the high-voltage and high-current fields [7-10]. In order to break through this limitation, after continuous research, people propose a composite buffer layer structure, which uses multiple PN junctions as drift layers to reduce the peak value of the electric field through the charge compensation effect to improve the withstand voltage of the device and reduce the conduction [11]. Resistance, this is CoolMOS, which can obtain low dynamic power consumption and high switching speed at the same time. The relationship between $B_v$ and on-resistance $R_{on}$ is: $R_{on} \propto B_v^{1.23}$.

The realization of the CoolMOS device structure is mainly carried out by alternately growing epitaxial layers and P-type ion implantation, and the aspect ratio of the implanted P region directly affects the on-resistance, which makes the manufacturing process complicated and difficult. Later, it was discovered that a deep trench can be used to replace CoolMOS with multiple growth epitaxial layers. The formation of this deep trench only depends on photolithography and etching processes, but the current dry etching of SiC has anisotropy, the etching rate of different crystal planes is different, it is difficult to control the angle of the trench sidewall, and the corners are easy to form micro trenches. Etching problems such as grooves, forming a trench with a relatively large etching depth and width on the SiC material, is even more challenging.

In this paper, we have studied the trench etching process and photolithography process of the power MOSFET device with a 6-inch 4H-SiC trench aspect ratio of 1:6. The successful research of the above process will help people to develop deeper trenches. Research and development of type power MOSFET device direction.

2. Research method

The mask morphology of the oxide film is first formed by growing on the N-type SiC wafer, and then the oxide film morphology is used as the mask for etching the SiC trench. Figure 1 shows the SiC MOSFET trench etching process. Due to the high Si-C bond strength and chemical stability of SiC materials, chemical corrosion can only be carried out at high temperatures. The use of high-temperature molten salt or alkali as an etchant cannot achieve conventional wet corrosion, and a dry etching process is required. Therefore, we use reactive ion etching (RIE) to dry etch the silicon dioxide mask, and plasma etching (ICP) to dry etch SiC [12]. In SiC, a trench with an etching depth greater than 1.2um and a sidewall angle greater than 90° is realized. According to the device design requirements, we fill the trench with SiO$_2$ to ensure that there are no holes in the trench after filling, and conduct the research of the photolithography process. The photolithography process needs to solve the problem of uneven coating, exposure and development at the groove. This paper uses SEM to measure the morphology of the trench after etching and photolithography to characterize the experimental results, and use CDSEM to measure the line width. Measure the surface roughness of the etched device by atomic force microscope (AFM). All equipment in this article is based on independent process platform equipment.
3. Results and discussion

Due to the anisotropy of dry etching, the etching rate of different crystal planes is different during the trench etching of SiC wafers, and it is difficult to control the angle of the trench sidewalls, and the plasma is deflected in the gate trench during the etching process. Which causes more plasma to gather at the corners, which intensifies the etching speed at the edge of the groove, and makes the formation of micro-grooves at the corners. Such micro-grooves will seriously affect the withstand voltage of the device and cause the device to break down in advance. Deep trench etching is the difficulty of this project. By adjusting the cavity pressure, RF power, gas type, gas ratio, flow rate, etching time and other parameters during the etching process to control the mask selection ratio, SiC etching rate and etching anisotropy, dry etching It is the key to realize a deep trench etching process with steep and smooth sidewalls and no micro-trenches at the bottom.

As shown in Figure 1, the MOSFET trench etching process, we first grow an oxide film of a certain thickness on the N-type SiC wafer, and apply photoresist on the oxide film through photolithography, and then the pattern is formed by photolithography. The mask of the oxide film is etched, and then the topography of the oxide film is used as the mask for etching the SiC. After the photoresist is removed, a trench larger than 1.2um is finally formed on the SiC. The etching conditions we adopted are: ICP power variation range is 200W~500W, reaction chamber pressure range is 3~7mTorr, gas flow rate is 10sccm, SF6 gas is used, and bias voltage is 100V~300V. After the etching is completed, the atomic force microscope (AFM) analysis photo of the surface morphology of the device is shown in Figure 2. It can be seen from the picture that the roughness of the chip surface after etching is less than 1nm, and the etching pattern is relatively complete.
The morphology of the trench formed by etching was characterized by SEM, as shown in Figure 3. The measurement results show that the trench depth is 1.2um, the sidewall angle is 91°, and the etching aspect ratio is about 1:6, which meets the process requirements.

After the trench etching is completed, a carbon film coating process is performed. Since the thickness of the photoresist applied for the carbon film coating is about 0.8um, the 1.2um groove brings great challenges to the carbon film coating process. After adjusting the coating process many times, we finally coated the carbon film with photoresist on the SiC trench to achieve full coverage. After coating the topography, the SEM measurement result is shown in Figure 4. The thickness of the resist is about 0.95um, the photoresist on SiO₂ is about 0.45um, and the groove corner is about 0.35um.

Figure 3. SEM image of the morphology of the trench formed by SiC etching

Figure 4. SEM image of cross-section morphology of carbon film
Another difficulty in the photolithography process of trench SiC MOSFET is the over-etching of the trench. We fill the trench with a certain thickness of SiO₂ to ensure that there are no holes in the trench after filling, and then apply photoresist on the silicon oxide and expose it. After developing, the filled oxide film is etched with photoresist as a mask. After the etching is completed, the remaining photoresist is removed. Figure 5 is a schematic diagram of the process flow of trench over-etching. Due to the existence of the grooves, the surface of the wafer is uneven, which cannot be achieved by conventional over-etching processes. The thickness of the coated photoresist has a greater impact on the photoresist deposited in the deep groove. For a 1.8um photoresist, the thickness of the photoresist in the groove is about 2.1um, and the minimum thickness of the photoresist is about 0.8um. At the same time, it is also necessary to combine the subsequent etching process and debug the photolithography process many times to obtain the most suitable coating conditions and exposure conditions. The topography result after photoetching at the optimum exposure focal length is shown in Figure 6. Among them, Figure 6 (a) is the SEM image of the surface morphology, and Figure 6 (b) is the SEM image of the cross-sectional morphology.

![Figure 5. Schematic diagram of groove engraving process](image)

![Figure 6. SEM image of groove engraved topography. (a) Surface topography; (b) Section morphology](image)
After the photolithography process is completed, the silicon oxide is etched. The minimum sidewall after etching is about 0.3um. As shown in Figure 7, the sidewall surface is smooth and the sidewall angle is greater than 90°. This result is sufficient for the power SiC MOSFET process need. The trench etching and photolithography process are new processes in the SiC MOSFET process flow, as well as a key process. After completing all the process flow, the electrical performance of the SiC MOSFET has been characterized, and the results are in line with expectations. Discussed in the article, not elaborated here.

**Figure 7.** SEM cross section of etched silicon oxide after photolithography

### 4. Conclusion

In this paper, the trench etching process and photolithography process of the 6-inch 4H-SiC trench power MOSFET device are studied. The mask morphology of the oxide film is formed on the N-type SiC wafer, and then the oxide film is used to form the mask. The morphology is used as a mask for etching the SiC trench, the silicon dioxide mask is dry-etched by RIE, and the SiC is dry-etched by ICP. In SiC, a trench with an etching depth greater than 1.2um and a sidewall angle greater than 90° is realized. Subsequently, according to the process requirements, the trench was filled with silicon oxide and the photolithography process was researched, and the photolithography process problems such as the unevenness of glue coating, exposure and development at the trench were successfully solved. The successful research of the above process will greatly promote the research process of trench SiC MOSFET power devices and will better improve the device performance.

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### References

[1] W. J. Choyke, H. Matsunami and G. Pensl, InSilicon Carbide, A Review of Fundamental Questions and Applications to Current Device Technology, Academic, New York, 1997.

[2] K. Hamada, Present status and future prospects for electronics in electric vehicles/hybrid electric vehicles and expectations for wide-bandgap semiconductor devices, phys. status solidi B, 2008, 245 (7): 1223 - 1231.
[3] A. Powell, J. Jenny, S. Muller, H. Hobgood, V. Tsvetkov, R. Lenoard, and C. Carter, Jr.: in SiC Materials and Devices, ed. M. Shur, S. Rumyantsev, and M. Levinshtein, World Scientific, Singapore, 2007.

[4] Y. M. Tairov, V. F. Tsvetkov, Investigation of growth processes of ingots of silicon carbide single crystals, J. Cryst. Growth, 1978, 43 (2): 209 - 212.

[5] R. Yakimova, M. Syväjärvi and M Tuominen, Seeded sublimation growth of 6H and 4H-SiC crystals, Mater. Sci. Eng. B, 1999, 61: 54 - 57.

[6] K. Xie, J. R. Femish, J. H. Zhao, W. R. Buchwald and L. Cacas, Low damage and residue-free dry etching of 6H-SiC using electron cyclotron resonance plasma, Appl. Phys. Lett., 1995, 67: 368 - 370.

[7] M. Matin, A. Saha, and J. A. Cooper Jr., Self-aligned short-channel vertical power DMOSFETs in 4H-SiC, Mater. Sci. Forum, 2004, vol. 457 – 460, pp. 1393 – 1396.

[8] K. Ueno, Method for manufacturing silicon carbide MDS semiconductor device including utilizing difference in mask edges in implanting, U.S. Patent 6: 238-980, 2001.

[9] Maherin Matin, Asmita Saha, and James A. Cooper, Jr., A Self-Aligned Process for High-Voltage, Short-Channel Vertical DMOSFETs in 4H-SiC, IEEE Trans. Electron Device, vol. 51, No. 10, 2004.

[10] Y. Sui, X. Wang, and J. A. Cooper, High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC, IEEE Electron Device Lett., vol. 28, No. 8, 2007.

[11] X. B. Chen and J. K. Osin, Optimized of the Specific On-Resistance of the COOLMOS, IEEE Trans. Electron Device, 2001, 48: 344 - 348.

[12] B. Li, L. Cao and J. H. Zhao, Evaluation of damage induced by inductively coupled plasma etching of 6H-SiC using Au Schottky barrier diodes, Appl. Phys. Lett., 1998, 73 (5): 653 - 655.