A 700-MS/s 6-bit SAR ADC with partially active reference voltage buffer

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Abstract: This paper presents a 700-MS/s 6-bit SAR ADC with a novel on-chip reference voltage buffer in a 40-nm CMOS Low-Leakage (LL) process. The reference voltage buffer is partially active depending on the operation state of the SAR ADC. The large driving current is provided only when the Capacitive Digital-to-Analog Converter (CDAC) is settling. This approach achieves 42% power reduction for the reference voltage buffer, which helps to improve the Figure-of-Merit (FoM) of the total SAR ADC chip. The measurement results show the ADC achieves an SNDR of 35.5 dB at the input frequency of 318.8 MHz. The chip consumes 4.0 mW including the SAR ADC core and the reference voltage buffer, resulting in an FoM of 117.8 fJ/conv.-step.

Keywords: SAR ADC, reference voltage buffer, asynchronous, low power

References

[1] Y. M. Greshishchev, et al.: “A 40 GS/s 6 b ADC in 65 nm CMOS,” ISSCC Dig. Tech. Papers (2010) 390 (DOI: 10.1109/ISSCC.2010.5433972).
[2] L. Kull, et al.: “A 90 GS/s 8 b 667 mW 64× interleaved SAR ADC in 32 nm digital SOI CMOS,” ISSCC Dig. Tech. Papers (2014) 378 (DOI: 10.1109/ISSCC.2014.6757477).
[3] Y. Duan and E. Alon: “A 12.8 GS/s time-interleaved ADC with 25 GHz effective resolution bandwidth and 4.6 ENOB,” IEEE J. Solid-State Circuits 49 (2014) 1725 (DOI: 10.1109/JSSC.2014.2314448).
[4] P. Harikumar and J. J. Wikner: “Design of a reference voltage buffer for a 10-bit 50 MS/s SAR ADC in 65 nm CMOS,” IEEE International Symposium on Circuits and Systems (ISCAS) (2015) 249 (DOI: 10.1109/ISCAS.2015.7168617).
[5] F. Borghetti, et al.: “A programmable 10 b up-to-6 MS/s SAR-ADC featuring constant-FoM with on-chip reference voltage buffers,” Proc. of the 32nd European Solid-State Circuits Conference (ESSCIRC) (2006) 502 (DOI: 10.1109/ESSCIR.2006.307499).
[6] L. Kull, et al.: “A 3.1 mW 8 b 1.2 GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32 nm digital SOI CMOS,” IEEE J. Solid-State Circuits 48 (2013) 3049 (DOI: 10.1109/JSSC.
1 Introduction

In recent years, SAR ADCs become more and more popular as sub-ADCs for implementing high-speed low-power time-interleaved ADCs [1, 2, 3]. For a highly integrated commercial system-level chip, a reference voltage buffer (RVBuffer) is indispensable. The RVBuffer impacts the performance of the high-speed SAR ADC significantly because the capacitor array charging/discharging during bit cycling disturbs the reference voltage. The consequent incomplete CDAC settling introduces conversion errors and causes the linearity degradation. The reference voltage can be provided off-chip. However, the parasitic inductors of the bondwires and PCB traces cause ringing on the reference voltage and thus the CDAC output [4]. Adding on-chip decoupling capacitors is one way to mitigate the ringing effect. Unfortunately, the large capacitance value is required, making this method costly. The on-chip RVBuffer helping to isolate the reference voltage from ringing effects becomes a good choice. The RVBuffer should have rapid settling speed which makes it very power-hungry. The power consumption of the RVBuffer is fifteen times [5] or even twenty-eight times [4] as much as that of the SAR ADC core. The Walden FoM increases dramatically when considering the RVBuffer.

In this paper, we propose a 700-MS/s 6-bit SAR ADC with a partially active RVBuffer. The driving current of the RVBuffer can be changed depending on the operation state of the SAR ADC. Compared with the traditional RVBuffer, the power consumption of the proposed partially active RVBuffer is reduced by 42%. The ADC was fabricated in a 40-nm CMOS LL process. The total power consumption is 4.0 mW, resulting in a Walden FoM of 117.8 fJ/conv.-step.
2 Architecture of the proposed SAR ADC

Fig. 1 shows the architecture of the proposed SAR ADC. A binary CDAC with constant common-mode voltage is adopted. To achieve high-speed requirements, two comparators work alternately [6] to remove the reset time. The SAR logic stores the result of the current conversion step and generates two asynchronous clocks to control comparators. The control codes named $vp(5:1)$ and $vn(5:1)$ are sent to the CDAC to generate the analog signal for the next conversion step. The timing diagram is also shown in Fig. 1. The sampling time is 120 ps which leads to the sampling switch’s $R_{on}$ of 164 $\Omega$ to achieve a sampling accuracy of higher than 6 bit with the total sampling capacitance of 150 fF. Due to the high threshold voltages of MOSFETs in LL process, the bootstrapped switches are employed [7]. The CDAC only has two reference voltages. One is ground, the other one is $V_{ref}$ which is provided by the proposed partially active RVBuffer.

3 Proposed partially active RVBuffer

The total conversion time of the SAR ADC consists of the CDAC settling time, comparison time and logic time [8], as shown in Fig. 2. The large current of the RVBuffer is needed only when the CDAC voltage charges to a new level and settles with a required accuracy. During the comparison time and the logic time, the CDAC does not consume any energy theoretically, which means the reference voltage is only required to be stable without large driving capability. Partial reference voltage buffer can be switched off temporarily to reduce the power consumption of the total SAR ADC.
Fig. 2. Asynchronous SAR ADC working procedure and the power requirement for the RVBuffer.

Fig. 3. (a) Traditional RVBuffer (b) Proposed partially active RVBuffer.

Fig. 3(a) shows the traditional RVBuffer [9] which has a replica source-follower (SF) stage isolating the node $V_{ref0}$ from the capacitive load of the CDAC. The replica SF enables open-loop settling which assures the stability for the feedback loop and fast operation. However, the output SF keeps large current...
during the whole conversion time and it causes a waste of power consumption. To reduce the unnecessary power consumption, a novel partially active RVBuffer is proposed as shown in Fig. 3(b). The replica SF is divided into two stages. Stage I is the SF with low fixed current \( I_1 \) which is mainly composed of MOS M2 and resistor R2. Stage II consists of MOS M3 and resistor R3 and it is responsible for the fast CDAC settling. Switches M6~M13 are used to change the state of the stage II under the control of \( C_1, C_2, \overline{C_1}, \overline{C_2}, cks \) and \( \overline{cks} \). To cancel the channel charge injection effects of PMOS M6, M7 and M8, dummy devices M14~M16 are added. Devices M4, M5, M9 and M10 keep switch-on state to assure \( V_{ref} \) to copy \( V_{ref0} \) perfectly and avoid the voltage fluctuation. When the stage II is switched on, it provides \( k-1 \) times as much current as the stage I. During the CDAC settling, the proposed RVBuffer can provide the same driving capability as the conventional one. Thus there is no speed penalty for the SAR ADC. Assuming the required total current of the replica SF is \( k \cdot I_1 \), the sizes of devices in each SF stage are as follows:

\[
\frac{(W/L)_{M5}}{(W/L)_{M4}} = \frac{(W/L)_{M2}}{(W/L)_{M1}} = \frac{(W/L)_{M10}}{(W/L)_{M9}} = \frac{R_2}{R_1} = 1
\]

\[
\frac{(W/L)_{M3}}{(W/L)_{M11, M12, M13}} = \frac{(W/L)_{M6, M7, M8}}{(W/L)_{M4, M5}} = k - 1
\]

\[
\frac{R_3}{R_{1,2}} = \frac{1}{k-1}
\]

The schematic and timing diagram of the control logic in the proposed RVBuffer is illustrated in Fig. 4. The working procedure is described as follows. When the comparator 1 (cmp1) finishes its comparison, the outputs are apart which is detected by an NAND gate. Then the signal \( \text{comp1} \) becomes high and the CDAC begins to charge until \( ck2 \) becomes to logic “1”. During this period, \( C1 \) is logic “0” and the stage II in the proposed RVBuffer is switched on to guarantee the fast settling. The RVBuffer is in high-power state. The same process happens when the comparator 2 (cmp2) finishes its comparison and \( C2 \) becomes to logic “0”. At other times, the stage II is switched off and the RVBuffer keeps in low-power state.

The simulation results of SAR ADCs with partially active RVBuffer (PARVB) and traditional RVBuffer (TRVB) are shown in Fig. 5. The speed of \( V_{ref} \) settling
has no differences and the differential CDAC outputs show similar stair shapes when using the TRVB and the proposed PARVB. The power comparisons of the two RVBuffers are shown in the bottom sub-graph. Since the PARVB keeps high driving current only when the CDAC is settling, the power consumption is reduced. The simulation results show that, the root-mean-square (rms) current of the partially active RVBuffer is 1.1 mA while the rms current of the traditional RVBuffer is 1.9 mA. The power consumption of the RVBuffer drops by 42%.

![Transient Response](image)

**Fig. 5.** Transient simulation results of SAR ADCs with partially active RVBuffer and traditional RVBuffer.

## 4 Other circuit implementations

### 4.1 Dynamic comparators

Compared with general purpose process, the low-leakage process provides MOS devices with larger threshold voltages. To achieve the high-speed operation, larger sizes of the input differential transistors need to be designed. The increasing parasitic capacitor, Cds, introduces larger kickback noise. Therefore a double-tail latch-type comparator [10] is adopted. Unlike the Strong-ARM latch, the double-tail latch-type comparator consists of two stages, i.e. the input stage and the latch stage as shown in Fig. 6. The outputs of the latch stage are isolated from the input differential pair to achieve much lower kickback noise. For the best ratio of speed to offset voltage, the input common-mode voltage is chosen to be 625 mV. The current-steering DACs, $I_n$ and $I_p$, are inserted in the node E and F to calibrate the offset voltage.
4.2 Asynchronous SAR logic

The asynchronous SAR logic has two parts. One is the memory logic, the other one is the asynchronous clock generator. The memory logic stores the outputs of the comparators in their corresponding memory slices. The schematic of the memory logic is shown in Fig. 7. MEM(5), MEM(3) and MEM(1) store the outputs of comparator 1, and the remaining memories store the outputs of comparator 2. In this design, the multiplexer is used instead of traditional combination logic to increase the speed. When the signal EN changes to logic “1”, it means the memory slice finishes its storage process. The output of the multiplexer will become to logic “0” to close the current memory slice and meanwhile the next memory slice is opened to wait for receiving the outputs of the next conversion step. The signal \( en(5) \sim en(1) \) will become logic “1” successively like domino so that the conversion result of each step is stored correctly.

![Fig. 6. Schematic of the double-tail latch-type comparator.](image)

![Fig. 7. Schematic of memory logic.](image)
to VDD. Once the sampling process finishes, $cks$ returns to logic “0”. The logic “1” in node A is passed to node B by a transmission gate and the node C is discharged to GND. Thus the initial pulse generator provides the first positive edge for $ck1$. After $ck1$ goes to logic “1”, the node A is discharged to GND and the voltage of node B returns to logic “0” to shut down the initial pulse generator. After that, once the comparator 1 finishes its comparison, $comp1$ becomes to logic “1”. Then $ck1$ will discharge to GND and $ck2$ is charged to VDD. The two clocks, $ck1$ and $ck2$, will become high alternately until $stop1$ and $stop2$ turn off the switches.

![Realization of asynchronous clock generator.](image)

**5 Measurement results**

The prototype ADC was fabricated in a 40 nm CMOS low-leakage process. The die photograph with its corresponding layout is shown in Fig. 9. The active area of the whole SAR ADC is 285 $\mu$m x 52 $\mu$m and the SAR ADC core occupies 99 $\mu$m x 52 $\mu$m. The ADC was tested with a 1.1 V supply voltage and a 700 MHz sampling clock. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC are shown in Fig. 10(a). The maximum DNL and INL are $-0.34/ +0.36$ LSB and $-0.43/ +0.37$ LSB, respectively. Fig. 10(b) plots the measured output spectrum when the single sine tone with input frequency of 318.8 MHz is sampled at 700 MS/s. The SNDR is 35.5 dB and the SFDR is 42.41 dB. In Fig. 11, the measured SNDR and SFDR are plotted with different input frequencies at 700 MS/s sampling rate. The ADC has a flat SNDR/SFDR response for the input frequency from DC to Nyquist. The power consumption of the ADC is 4.0 mW, including 2.8 mW for the SAR ADC core and 1.2 mW for the

![Die microphotograph with corresponding layout.](image)
partially active RVBuffer. The Walden FoM of the whole SAR ADC is 117.8 fJ/conv.-step. The performance comparison with the state-of-the-art ADCs are shown in Table I. Except ref. [6] that has special devices like deep-trench capacitors and uses a more advanced process, our proposed SAR ADC shows a competitive FoM even when considering the RVBuffer.

![Fig. 10.](image)

![Fig. 11.](image)

**Table I.** Performance comparison

| Article Title   | [6]   | [8]   | [11]  | [12]  | This work       |
|-----------------|-------|-------|-------|-------|-----------------|
| Technology      | 32 nm SOI | 40 nm CMOS | 65 nm CMOS | 55 nm CMOS | 40 nm CMOS LL   |
| Sampling rate (MS/s) | 1200 | 1250 | 700 | 325 | 700             |
| Resolution (Bit) | 8     | 6     | 8    | 8    | 6               |
| ENOB (Bit)      | 6.2   | 4.2   | 6.6  | 6.8  | 5.5             |
| Power (mW)      | 3.06  | 6.08  | 5.96 | 6.0  | 2.8 (ADC core)  |
|                 |       |       |      |      | 1.2 (RVBuffer)  |
| FoM (fJ/conv.-step) | 34   | 265   | 86.7 | 165  | 117.8 (with RVBuffer) |
|                 |       |       |      |      | 82.5 (w/o RVBuffer) |
| RVBuffer        | On-chip | Off-chip | Off-chip | -    | On-chip         |
6 Conclusion

This paper presents a 700-MS/s 6-bit SAR ADC fabricated in a 40-nm CMOS low-leakage process. A novel partially active RVBuffer is proposed to reduce the power consumption while enabling high-speed CDAC settling. The proposed SAR ADC achieves an ENOB of 5.6 bit for the input frequency near Nyquist. The power consumption including the SAR ADC core and the RVBuffer is 4.0 mW, contributing to an FoM of 117.8 fJ/conv.-step.

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