Master Control Design of Polar Detection Ice Radar

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Abstract. This paper focuses on the design of the master control software dedicated for the application of high-resolution polar detection ice radar. The central part of proposed software is FPGA, which plays roles of collecting radar echo data, playback of chirp signal, data transmission to upper computer, coherent integral accumulation of digitized data and system control of the whole radar system. The performances of proposed system is demonstrated through real-field experiments.

1. Introduction
The Antarctic ice sheet is the largest marginal ice body in the world, and its material balance and stability have important influences on the global climate change and sea level change. Detection of the thickness and internal structure of the polar ice caps is the base of research on material balance and evolution of the ice caps. It is popular ways to understand the global climate change and sea level change. And it is also one of key projects for Antarctic expedition in China.

Due to the glacier advantages of small attenuation towards radio waves, layer character and good homogeneity, detection glacier using radar has been proved to be one of the effective technique method. A set of VHF band high-resolution radar for detecting the glacier thickness has been produced by the Key Laboratory of Electromagnetic Radiation and Detection Technology, Institute of Electronic, Chinese Academy of Sciences (IECAS). It can be used to detect the thickness of polar glacier and obtain its vertical section image[1-2].These experimental results demonstrate that radar exhibit state-of-art performances in the sense of penetration depth, measurement precise, high efficiency, etc.

2. Overview of Radar system
The proposed high-resolution polar ice detection radar(PIDR)utilizes the frequency modulation (FM) pulse compression to enhanced the average power of output signal [3]. Two different channels with tunable gain are employed in the receiver to increase the sensitivity of our system. The echoes is translated to digital signal by applying so-called intermediate frequency sampling technique. What’s more, to reduce the complexity of receiver system, the digital signals are processed in depth through the integral coherent technique embedded in our master control software.

The proposed radar system can be divided roughly into two main parts, namely analog system and digital system (as shown in figure 1). The analog system is composed of a pair of transmitting/receiving antennas, an emission power amplifier and a two-channel analog receiver. The digital system mainly consists of control module, a data acquisition module, a signal processing module and a playback module. This paper describes in detail the development and realization of master control software for the control, data acquisition, processing and playback modules[4-5].

As sketched if Fig 1, the digital system is composed of main control unit, clock generation unit, signal playback unit, data acquisition unit, data processing unit, data framing unit and USB data transmission unit. They take charge of the digital part of the whole system. The chirp signal and operational parameters are...
transferred between the digit system and upper computer through a USB port. Regarding the interface between the digit system and the analog system, the signal playback unit of the digit system outputs chirp signal to DAC sampling chip of the analog system, while the data acquisition unit of the digit system receives the echo data and GPS data from two-channel ADC chip of the analog system. The digit signals from the data acquisition unit will be processed by data processing unit and data framing unit, and finally sent to the upper computer through the USB data transmission unit. Overall, then system control unit accomplishes the function of task timing of the whole software and parameter analysis.

Figure 1. Radar composition block diagram.

3. Design of master control software

The digit system is made to realize a lot of functions which including data acquisition, data processing and analysis, data transmission, system control, chirp signal output, etc. Accordingly, a master control software which is compatible with the integration and stability of the whole digit system is designed to manage all the functions. Some complex algorithm are also integrated in our master control software to offer a better data processing. Therefore, a FPGA chip of high performance and large capacity is required to meet the requirements mentioned above. In this work, we used the xc5vlx50 produced by Xilinx Company, which has 12 Digital Clock Managers, 48 Global Clock Networks, 48 DSP Slice, 12.6Mb RAM and FIFO interior catch and 440 User I/O. And its interior highest operation frequency can be up to 550MHz. In addition, a ISE tool kit is developed to support the abundant IP core and conveniently accomplish design input, implement and synthesize in the digit system. The tool kit is not only able to size and reduce the cost, but also make the design of our system more flexible and reliable.

During one PRF period, when the rising edge of a PRF pulse is detected, the digital system sends out the chirp signal and begin to sample the analog echo signal. Then, the digital signal is further accumulates, stored, framed in the digit system and finally transferred to the upper computer through a USB port. Repeatedly, the digital system can be divided into the following units:

- System control unit is designed to analyze the parameters accepted from the upper computer, and control every unit of the radar system.
- Clock generation unit is used to generate and manage all the clock signals referred in the whole system, including the PRF clock, gating clock, sampling clock, etc. Signal playback unit is designed to receive and cache chirp signal accepted from the upper computer, and output the chirp signal to the DAC chip as PRF period.
- Data acquisition unit is designed to collect and store the signals from the two-channel receiver, including the simulated echo signal and the GPS signal. This acquisition has12 bits resolution, and its maximum storage depth is 8K. The storage of data is realized through the interior RAM of FPGA.
- Data processing unit is designed to implement the integral coherent process and the data cache process. The integral coherent process is to accumulate the digitized signal as frame for the unit, to enhance the SNR of collected data and reduce the memory space of raw data.
Data framing unit is designed to do framing of echo data from the data processing unit and GPS data, add information to corresponding frame head logo, frame count, etc. Data cache is realized through the interior FIFO of FPGA.

USB data transmission unit is designed to realize the interface between the upper computer and the radar digital system.

Figure 2 shows the main control software realization diagram and the data transmission process in digital system.

Figure 2. Diagram of the main control software realization

4. Workflow of the master control software

The workflow of the master control software is illustrated in figure 3. The upper computer transfers both the whole system’s operational parameters and chirp signal generated by transmitter to the digit system through a USB port. The regular operational parameters of the master control software include PRF, collected data length of frame, starting time of data collection, integral accumulation times, receiving gain, etc. The master control software is controlled by the upper computer. The control instructions include software resetting, parameter downloading, collecting, starting work order and operation.

Three units of the master control software start to work once the operational parameters are transferred from the upper computer. The system control unit analyses the accepted parameters and generates their corresponding control signal. The clock generation unit generates all the clocks required by radar system, including ADC sampling clock, DAC sampling clock, USB data transmission clock, FPGA clock and PRF. The signal playback unit stores the chirp signal to interior RAM1 of FPGA.

After the work order sent out by the upper computer, all units of the master control software start to work. The system control unit immediately reads chirp signal stored in RAM1 when the rising edge of PRF detected, and the outputs it to the external DAC chip. The data acquisition unit acquires the original frame data which ADC sampling. Then, the original frame data is coherent integration accumulated with the store data in RAM to reach the final data. The accumulative time is input through application software in the upper computer. Throughout the accumulative process, the accumulative results are stored to interior RAM2 of FPGA through the software. When the accumulative time is over, the software will transfers the accumulative data to the data framing unit and sends out the upper complete indication, The data stored in RAM2 is cleared when the whole frame data output is finished. The data frame is composed of frame header and frame valid data. The frame header includes flag, frame counter, parameter information, GPS data and reserved byte; while the frame valid data comes from counter, parameter information. Under the control of the software, the framing data goes to the USB data transmission unit through FIFO and caches.
5. Test results
In the high resolution imaging glacier thickness detection radar system, the ADC sampling frequency and the DAC sampling frequency are set as 166MHz and 1GHz. The chirp signal is generated by Matlab software in advance. In the test, the closed loop test of radar system is adopted. Firstly, the chirp signal is to download to FPGA from the computer based on the application software. Secondly, the work order of the master control software is started. Thirdly, the data after analysis and processing is uploaded to the application software in upper computer. Fourthly, the result is analyzed to check whether the radar is operating properly. The closed loop test procedures are as follows:

- Generate original chirp signal with 1us pulse width, 1 GHz sampling frequency, 1000 sampling point, as shown in FIG 4.
- Configure the working parameters of the radar, as shown in table 1.
- Observe the chirp signal output by signal playback unit in oscilloscope, as shown in FIG 5. The time width of the chirp signal is 1us.
- Collect and record the echoed analogue signal by data acquisition unit, read and display the data in Matlab. The result showed that the valid data sampling point corresponding to 1us echo signal is 166 under 166MHz sampling frequency, as shown in FIG 6.

Application software interface in upper computer is shown in FIG 7. The parameters of the radar can be configured in the left part of the interface. The result of pulse match filtering of the uploaded radar data is shown in the right part of the interface. The middle part of interface shows the depth of the target detected by the radar. The value of the detected target depth based on the closed loop test is determined by the system hardware loop and external wire length, and can be applied to radar system in practical applications.

**Figure 3.** Workflow of the master control software
**Table 1.** Parameter of closed loop test.

| Parameter                              | Value   |
|----------------------------------------|---------|
| Centre frequency of the chirp signal   | 125MHz  |
| Bandwidth of the chirp signal          | 50MHz   |
| Pulse time width of the chirp signal   | 1us     |
| Pulse period of the chirp signal       | 8K      |
| Accumulative times                     | 16      |
| Sampling point of echo signal          | 2048    |

In the mission of China's 28th Antarctic scientific expedition, the radar was used to carry out an experiment at a test site which is about 400-500 km away from Zhongshan Station. The result is shown in FIG8. The nethermost stratification ice-rocks the ice-rock interface, and the depth is greater than 2000 m. This is the first time to detect the ice deeper than 2000m with a high-resolution glacier detection radar in China.

**Figure 4.** Original chirp signal generated by Matlab.

**Figure 5.** Chirp signal outputted by signal playback unit in oscilloscope.

**Figure 6.** Sampling analog echo signal in Matlab.

**Figure 7.** Interface of application software in upper computer.
6. Conclusion
High resolution imaging glacier thickness detection radar makes use of high performance FPGA hardware platform as core, to achieve system control, data acquisition, processing, uploading and playback. The master control software design employs the concept of the pipeline and the method of building block, which result in the well organized program structure with high portability. The test results show that the design scheme is feasible, with good application potentials.

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