A novel to control defects of P-N semiconductor device by SRFE process

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Abstract. This paper present the results from soft radiation flash exposure (SRFE) process. In principle of semiconductor device always has defect in structure from fabrication process and impact from usage environment. Although, device have control process but still has unexpected defects. Then, I would like to share results of SRFE process to control defects in P-N semiconductor device by exposed on device for few second with optimize radiation energy. The defects has disappear after passed SRFE process. The optimize of exposure energy and time will cure or remove defect in devices structure.

Keywords: P-N semiconductor, SRFE process, Defects, RTA process, P-N diode

1. Introduction

Many kind of defects in semiconductor devices occur from several reason. The defects induce from several process since sand to silicon and also wafer fabrication process. Although, device process try to control defects but still has defects in silicon reduce device performance. [1]

One of process generate defects is silicon process, this process start from sand to silicon wafer. The technique for silicon wafer such as

- Czochralski silicon (CZ) - use by IC industry [2]
- Floating zone silicon (FZ) - basically all silicon detectors made from FZ silicon [3]
- Epitaxial silicon (EPI) - chemical-vapor deposition (CVD) of silicon, growth rate slow about 1µm/min [4]

By all process still has some defect in silicon mechanism. Moreover, wafer fabrication process is a big impact for defect generate effect due to many process can induce defect if cannot control such as photolithography, doping and cleaning process. In term of photolithography and cleaning process can control to check frequent but doping process is hard to control. [5]

Simulation by COMSOL semiconductor can simulate of the concentration of doping atom in silicon bulk. Then, device will show the area occurred defects in device structure and can find the process for treatment and improve performance of device. Technique for improve device performance in the present such thermal annealing (TA) [6], rapid thermal annealing (RTA) [7] and radiation expose [8].
Soft radiation flash exposure (SRFE) process is new novel for semiconductor device performance improvement. By the process will provide soft radiation on device for few second. The technique will optimize dose by each device because the different of structure.

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2. Experiment Procedure

2.1. Simulation
For the simulation design focus on impact from ion implantation process on device structure. Device structure for simulation will focus on surface area that has close with ion implantation zone. The results will show concentration of doping atom various by concentrate. [9]

2.2 Fabrication process and Device structure
Device will fabricate by using CMOS technology. The silicon substrate type is n-silicon shown in Figure. 1. [10-12]

![Figure 1. Device structure.](image)

The process flow show in below: [13]
- Deposited oxide cover and also etching to open active area
- Doped phosphorus by ion implantation technique with high energy 120 keV by dosage 1x10\(^{16}\) cm\(^{-2}\) on back side for ohmic contact
- Doped boron in active area same technique and energy with backside
- Diffuse platinum on backside of device and diffusion by RTA technique for 6 hours with high temperature
- Create metal (Al) both side then annealing treatment by TA technique
- By the final will die device prepare for testing

2.3. Experimental procedure
Device after fabrication will measure current-voltage (IV) characteristics by bias voltage -10 to 0V with step 0.01 V. After measure I-V, device will exposed by SRFE process by control exposure time shown in Figure. 2. Then, measure I-V characteristics of device immediately.
3. Results and Discussions

Rapid thermal annealing (RTA) is the process for drive in doping atom and treatment device. High temperature will help atom get enough energy and diffuse to low concentration area or kick off host atom. Not almost defects can treatment by RTA moreover RTA may create some of defects in silicon from atom diffuse to silicon bulk. Figure 3 shows doping atom characteristic after RTA process in silicon bulk. That can confirm properties of atom in silicon mechanism. [14]

Ion implantation process will doping atom in active are of device by using high energy show in Figure. 4. The doping atom hit surface and penetrate in silicon bulk this impact will damage on substrate surface and also in bulk. The high energy can help to doped but still leave some damage for device. [15]

Simulation results show in Figure. 5 and Figure. 6, by the results simulate doping concentration from ion implantation technique.
The results show concentration close surface has high concentrate and decrease while deep into silicon bulk. The red area show high concentration, yellow and green area show lightly concentrate. After RTA process, the doping atom will diffuse to bulk. [16]

The current-voltage before and after SRFE process of P-N semiconductor device shown in Figure. 7. Results shows reverse current of before SRFE around $1.2 \times 10^{11}$ A at -10V and after show around $8 \times 10^{-12}$ A. The current reduced after exposed device by SRFE process around $4 \times 10^{-12}$ A.
Figure 7. Reverse current compare between before and after SRFE process.

4. Conclusions
From the experiment fabricate P-N diode by using CMOS technology and measure current-voltage after fabrication by bias voltage -10 to 0V show around 2x10^{-11} A. The leakage current of device may from several reason and main factor may from ion implantation. Simulation results how high concentration of doping atom around surface and deep into silicon bulk after RTA process. This process may induce defects or cluster in silicon mechanism. SRFE process is the new novel to use for study and expect can help for treatment electrical properties of device. The leakage current after SRFE process show around 8x10^{-12} A that reduce from before SRFE process around 4x10^{-12} A. From this change may occur from SRFE has reduced some of damage from fabrication process or reduce defect. Moreover, SRFE process may change kind of defects or destroy cluster in silicon mechanism. The benefit for low leakage current will help device use low energy to turn on semiconductor device.

References
[1] Chad MB 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC) 11487494
[2] James N, Stevan D and Ilyasse A 2011 19th Mediterranean Conference on Control & Automation (MED) 12178896
[3] Kawamura S, Kaneko JH, Higuchi T, Haruna Y, Yagi Y, Susa K, Fujita F, Homma A and Nishiyama S 2007 IEEE Trans Nucl Sci 54 1983-1386
[4] Arkun FE, Semans S, Vosters G, Smith RS and Clark A 2010 IEEE International SOI Conference (SOI) 11656726
[5] Dominique B, Azar MD and Henrio S 2007 Appl. Surf. Sci. 253 6162-6164
[6] Dongol M, El-Denlawey A, Abd El Sadek MS and Yahia IS 2015 Optik 126 1352-1357
[7] Feygenson A and Zemel JN 1988 This solid films 165 109-138
[8] Brown WL, Augustyniak WM and Waite TR 1959 J. Appl. Phys 30 1258
[9] Poulain G, Blanc D, Semmache B, Pellegrin Y and Lemiti M 2011 Energy procedia 8 587-591
[10] Itsara S, Surada U and Amporn P 2012 Opt Laser Technol 44 635-639
[11] Haieng Z, Zhaowei Z, Mingyu G, Li L, Shukai D, Zhekang D and Huipin L 2020 Electronics 9 542
[12] Dong MK, Dongmin K, Hang GJ and Donggu I 2020 Electronics 9 562
[13] Surada U, Itsara S, Surasak N and Amporn P 2014 International Journal of Materials and Product Technology (IJMPT) 49(1)
[14] Susi E, Poggi A, Fabbri R, Merli M, Coratta MC and Passari L 1989 Mat Sci Eng B 4 231-235
[15] Vines L, Wong-Leung J, Jagadish C, Monakhov EV and Svensson BG 2012 Physica B: Condensed Matter 407 1481-1484

[16] Grob JJ, Unamuno S, Grob A, Ajaka M, Slaoui A and Stuck R 1987 Nucl. Instrum. Methods Phys. Res. B 19-12 501-506