Joint Protection Scheme for Deep Neural Network Hardware Accelerators and Models

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Abstract—Deep neural networks (DNNs) are utilized in numerous image processing, object detection, and video analysis tasks and need to be implemented using hardware accelerators to achieve practical speed. Logic locking is one of the most popular methods for preventing chip counterfeiting. Nevertheless, existing logic-locking schemes need to sacrifice the number of input patterns leading to wrong output under incorrect keys to resist the powerful satisfiability (SAT)-attack. Furthermore, the DNN model inference is fault tolerant. Hence, using a wrong key for those SAT-resistant logic-locking schemes may not affect the accuracy of DNNs. This makes the previous SAT-resistant logic-locking scheme ineffective on protecting DNN accelerators. Besides, to prevent DNN models from being illegally used, the models need to be obfuscated by the designers before they are provided to end-users. Previous obfuscation methods either require a long time to retrain the model or leak information about the model. This article proposes a joint protection scheme for DNN hardware accelerators and models. The DNN accelerator is modified using a hardware key (Hkey) and a model key (Mkey). Different from previous logic locking, the Hkey, which is used to prohibit the accelerator, does not affect the output when it is wrong. As a result, the SAT attack can be effectively resisted. On the other hand, a wrong Hkey leads to substantial increase in memory accesses, inference time, and energy consumption and makes the accelerator unusable. A correct Mkey can recover the DNN model that is obfuscated by the proposed method. Compared to previous model obfuscation schemes, our proposed method avoids model retraining and does not leak model information.

Index Terms—Deep neural network (DNN), hardware accelerator, hardware security, logic locking, obfuscation.

I. INTRODUCTION

Deep neural networks (DNNs) are popular in numerous image processing, object detection, and video analysis tasks. Scaling up the model size can increase the learning ability and performance of a DNN model [1], [2]. However, a large amount of data needs to be stored during DNN inference. Accessing data from memory consumes much higher energy and takes much longer time than arithmetic computations, especially when the intermediate data is big and needs to be stored in off-chip memories. Many DNN accelerators [3], [4], [5], [6], [7] realize that there is high sparsity on the temporary result of different layers in DNN inference. In order to reduce the memory size and access, these DNN accelerators discard zero values and only store nonzero values in compressed formats in memory during the model inference.

Logic locking [8] is one of the most popular methods to prevent chip counterfeiting. It inserts a key-controlled block into the circuit so that signals in the circuit are flipped when a wrong key is used. The correct key is handed out to the authorized user after chip fabrication. The satisfiability (SAT) attack [9] is a powerful attack against logic locking. It iteratively excludes wrong keys corrupting the output of the locked circuit. The earlier logic-locking schemes, such as those in [8], [10], [11], [12], [13], and [14], are subject to the SAT attack. The Anti-SAT [15], SARLock [16], and G-Anti-SAT [18] schemes make the number of iterations needed by the SAT attack exponential. However, in these SAT-attack-resistant schemes, the number of input patterns leading to wrong outputs under incorrect keys, which is referred to as the corruptibility of the wrong key, is small. The AppSAT attack [17] excludes those high-corruptibility wrong keys and return an approximate key, which can be used to generate the correct output for most input patterns. Although the stripped functional logic locking (SFLL) [20] improves the tradeoff between the SAT attack resistance and the corruptibility of all wrong keys, an approximate wrong key still does not affect the accuracy of DNNs much since they are naturally fault-tolerating [22]. Besides, by analyzing the functional and structural properties of SFLL, the functional analysis on logic locking (FALL) [23] and hamming distance (HD)-unlock method [24] can successfully compromise the SFLL. As a result, it is essential to develop an effective logic-locking method to protect DNN accelerators.

Training a DNN model requires massive labeled data, computation resource, and significant work on tuning the hyperparameters. In the white-box setting [25], the neural network architecture and the trained model parameters are publicly known (e.g., Caffe Model Zoo). In this case, the attacker can modify the trained parameters without affecting the output accuracy and claim the ownership. Chakraborty et al. [26] proposed a key-dependent training process to lock the original model. The target hardware platform is modified so that the original model can be recovered by providing a correct key. However, this obfuscation method requires the model to be retrained for every correct key that is sent to different users. Goldstein et al. [27] swapped the rows and columns of the...
filters and/or the order of the layers of the trained model. This information is sent to the authorized end-user. Nevertheless, it can also help the attacker to recover the original model.

This article proposes a joint logic locking and obfuscation scheme that protects both DNN hardware accelerators and models. Most state-of-the-art DNN accelerators are aware of the sparsity in the intermediate results and have data compression blocks that only record the nonzero values in order to reduce the memory requirement. By inserting a logic-locking block controlled by a hardware key (Hkey) into the data compression block, our design substantially increases the amount of data to be stored into the memory when a wrong Hkey is applied. Accessing more intermediate data stored in memory also leads to longer latency and higher energy consumption. Different from previous logic-locking schemes, using a wrong Hkey in the proposed design does not affect the circuit output. Since the SAT attack can only exclude keys corrupting the output, wrong Hkeys in the proposed design cannot be excluded, and the SAT attack can be effectively resisted. The proposed logic-locking scheme can be used by different accelerators regardless of the data compression method. The DNN model obfuscation method proposed in this article changes the biases of a trained DNN model. The DNN accelerator is also modified to have a model key (Mkey) inserted into the bias addition block. Only when the correct Mkey is used, the original biases are recovered and exactly the same original model is implemented in the hardware. Similar to previous DNN model protection schemes, the proposed method makes the original model hard to recover even if the attacker has access to part of the training sets. The advantages of our proposed scheme include: 1) no model retraining is needed for inserting the Mkey and 2) it does not leak any information that can help with the recovery of the original model.

Experiments are done on popular DNN models, such as AlexNet [28], ResNet [1], and VGG [29], to verify the advantages of the proposed protection scheme. Simulation results using the ILSVRC-2012 dataset [30] show that a DNN accelerator obfuscated by our proposed logic-locking scheme requires as much as 3.71, 1.67, and 2.76 times more memory accesses for AlexNet, ResNet, and VGG, respectively, with different compression methods under wrong Hkeys. In addition, without the correct Mkey, the top-1 accuracy for those three networks drops by 86%, 76.72%, and 82.35%, respectively, on CIFAR-10 dataset [31]. Even if a more powerful attacker obtains 10% of the original training set as thief dataset to finetune the obfuscated model, the accuracy of the finetuning result still drops by as much as 14.81%.

This article is organized as follows. Section II introduces DNN hardware accelerators, logic locking, and DNN model protection. Section III proposes our new methods for jointly protecting DNN hardware accelerators and models. Experimental results and security analyses are provided in Section IV. Discussions and conclusions follow in Sections V and VI, respectively.

II. BACKGROUNDS

This section first introduces background knowledge of DNN accelerators. Then, the threat models are presented. Previous logic locking and DNN protection schemes are also introduced in this section.

A. Sparsity-Aware DNN Accelerators

A DNN typically consists of different layers, such as convolutional layer, pooling layer, and fully connected layer, connected in sequence. A convolutional layer is used to extract the features from input data. A pooling layer is responsible for solving the potential overfitting problem of DNNs by reducing the spatial size of input feature maps. A fully connected layer is usually used when the DNN is designed for classification tasks. It computes the class scores based on the outputs from the previous layer. In order to increase the nonlinearity of DNNs, an activation function usually follows a convolutional or fully connected layer. The rectified linear unit (ReLU) is the most popular activation function, and it is defined as follows:

$$\text{ReLU}(x) = \begin{cases} 
0, & (x < 0) \\
 x, & (x \geq 0).
\end{cases}$$  (1)

Although scaled exponential linear unit (SeLU) and exponential linear unit (ELU) can improve the prediction accuracy, their hardware complexities are much higher than that of the ReLU function. In particular, it is very difficult to implement the exponential function. Hence, the application of SeLU and ELU in high-speed hardware accelerators is limited.

Since modern DNNs are deep and many layers are wide, a hardware accelerator typically consists of a number of computation units that are used in a time-multiplexed way to complete the calculations layer by layer. For each convolutional and fully connected layer, the input feature map first goes through multiplier and accumulators (MACs). Then, the sums of the products go through the bias adders to be added with the corresponding biases. The results of bias adders will be sent to the ReLU function. The outputs of the ReLU function, called output feature maps, need to be stored before they are consumed by the computations for the next layer.

Due to the wide layers, storing all the data in the feature maps requires large memory and many memory accesses. According to [7], accessing an 8-bit data from DRAM costs around 200× energy compared to an MAC operation. In addition, accessing data from off-chip memory needs much longer latency despite possible prefetching. From (1), a large portion of the elements in the output feature maps are zero. Take the first convolutional layer of AlexNet as an example. When 128 images from the ILSVRC-2012 dataset are used as the inputs, 60.95% of values in the output feature maps are zero. To reduce the amount of data to store, different compression methods, such as compressed sparse column (CSC) format [6], run length compressing (RLC) [3], and bit map format [4], [7], have been utilized in sparsity-aware DNN accelerators. These compression methods discard zeros. Nonzero values and their locations are recorded in different formats.

B. Threat Models

1) Hardware Threat Model: The hardware threat model is shown in Fig. 1. Many of the circuit designs are sent to a third-party facility for fabrication. If the attacker gets the netlist, extra chips may be made and sold for profit. Such
chip overproduction causes significant economic loss to integrated circuit design companies. In an integrated circuit supply chain, an attacker can get the netlist of the circuit either from the untrusted foundry or by reverse engineering a chip bought from the open market. Following the same assumption made by previous papers [15], [16], [18], [20], it is assumed that: 1) the attacker has access to the netlist of the chip, and he/she can analyze the netlist and insert/remove logic functions into/from the circuit netlist and 2) the attacker also has a functioning chip purchased from the open market. However, the attacker does not have access to: a) the intermediate signals of the circuit corresponding to specific inputs since the internal signals can not be probed when the circuit is running and b) the correct key stored in a tamper-proof memory.

2) DNN Threat Model: Training a DNN model requires significant work, including designing the model structure, labeling the training and validation dataset, and tuning the hyperparameters. In addition, a large amount of computing resource is needed to complete the training in practical time. To prevent a trained model to be illegally used, it needs to be obfuscated to make the output accuracy drop significantly under unauthorized usage. The goal of the attacker is to recover the original model and distribute the model on his/her own systems.

In this article, the attacker is assumed to have access to the structure and parameters of the obfuscated model as shown in Fig. 2, just like the white-box setting mentioned in [25]. In addition, a small portion, i.e., 10%, of the private labeled training data is accessible according to [26]. Utilizing the small portion of training data as well as the structure and obfuscated parameters of the DNN, the attacker can finetune the DNN to increase the accuracy.

C. Related Work

1) Existing Logic-Locking Schemes and Attacks: Logic locking inserts key-controlled blocks or introduces individual key bits into the circuit by using XOR/XNOR/AND/OR gates as shown in Fig. 3. When a wrong key is used, intermediate signals of the circuit are flipped and the circuits output is corrupted under certain input patterns. The SAT attack [9] is one of the most powerful methods that can compromise logic locking. It utilizes the conjunctive norm formula of the locked circuit netlist. By carrying out queries to the functional chip, wrong keys that make the output of the locked circuit different from the original output are excluded by the SAT attack. To resist the SAT attack, many logic-locking schemes have been developed, such as the SARLock [16] and Anti-SAT [15]. Although they make the number of iterations needed by the SAT attack exponential to the number of key input bits, the corruptibility of each wrong key is only one. This means that using any wrong key will not corrupt the output most of the time. The low corruptibility is utilized by the AppSAT attack to return an approximate key.

The G-Anti-SAT [18] design maintains the exponential iterations in the SAT attack. On the other hand, it substantially increases the corruptibility of a large portion of the wrong keys. A variation of the G-Anti-SAT was also developed in [19] to better resist removal attacks. The SFLL proposed in [20] increases the corruptibility of all wrong keys at the cost of a reduced number of iterations needed by the SAT attack. However, none of existing logic-locking schemes can effectively protect hardware chips implementing DNN inference since it is fault tolerant [32]. Even if intermediate signals in a DNN accelerator are locked by SFLL, the output accuracy is not affected when a wrong key is utilized as it was found in [22].

2) Previous Methods Protecting DNN Model: A trained model needs to be obfuscated before being provided to end-users. Authorized users can inference the model without accuracy degradation. Chakraborty et al. [26] proposed a
key-dependent backpropagation algorithm to train DNN models. Random neurons from a DNN model are chosen. They are modified according to the selected key vector and the data scheduling scheme of the target hardware accelerator. Retraining is carried out on the modified model and the weights are changed. The hardware accelerator implementing the obfuscated model is also modified so that only the correct key can unlock the model. However, for every different correct key, this obfuscation method requires the model to be retrained. Retraining a model is computation intensive and requires long time. Hence, the scalability of this method is limited.

Goldstein et al. [27] proposed a method that does not need retraining. It obfuscates the model by swapping the rows, columns, and layers of the weight matrices. The correct key indicating the information about the swapping is handed out to the authorized end user by the designer. Based on these information, the end user can get the original model back and make the correct inference. Without the right key, the weight matrices are swapped in the inference and the accuracy of the modified model drops significantly. Nevertheless, if the key itself gets compromised, the original model will be recovered and can be illegally used.

III. PROTECTION SCHEMES FOR SPARSITY-AWARE DNN ACCELERATORS AND MODELS

This section proposes an effective joint protection scheme for DNN hardware accelerators and models. The proposed method inserts an Hkey-controlled block after the ReLU function so that zero values will not be recognized under incorrect Hkeys. As a result, all values go through the compression process and are stored into memory. In this case, the latency and power consumption of the hardware accelerator are increased by multiple times. In addition, the ReLU function is modified to further prevent the Hkey-controlled block from being bypassed. DNN models are protected by introducing an Mkey in our design. The biases of the DNN model are obfuscated and the bias adders in the hardware accelerator implementing the obfuscated model is modified to have an Mkey input. Only the correct Mkey can recover the correct biases and make DNN inferenced without accuracy degradation.

A. Hkey-Controlled Match Detector and Modified ReLU

Let the output of the ReLU function be X. Existing sparsity-aware DNN hardware accelerators discard X if it is zero and only store the nonzero values in compressed format in the memory. In the proposed design, the zero detector in existing designs is replaced by a Hkey-controlled match detector. Under the correct Hkey, it outputs “1” if X is zero and “0” otherwise. The following data compression unit compresses X when the match detector outputs “0.” Wrong Hkeys make the detector always output “0,” and all values, including zeros will go through the compression block and get stored into memory.

The functionality of the ReLU is public and it is well-known that sparsity-aware DNN hardware accelerators discard the zeros. A potential threat is that the output wires of the ReLU function may be located by the attacker. Then, a zero detector can be used to bypass the match detector and nullify the inserted Hkey. To prevent such threats, the ReLU function is modified in our design. Assume that the input to the ReLU is an h-bit value \( A = a_{h-1} \ldots a_1 a_0 \) and \( a_{h-1} \) is the sign bit. Then, the output of the original ReLU defined in (1) can be described in the logic level as follows:

\[
x_{h-1} = 0, \quad x_{j} = \overline{a_{h-1}} \& a_{j} (0 \leq j < h-1)
\]

where the overhead bar denotes logic NOT. In our modified ReLU function, a predetermined constant h-bit secret vector \( T = t_{h-1} \ldots t_0 \) is XORed with \( X \) to generate \( \tilde{X} \) as follows:

\[
x'_{h-1} = t_{h-1}, \quad x'_j = x_j \oplus t_j (0 \leq j < h-1).
\]

When \( t_j = “1” \) and “0,” \( x'_j = \overline{x_j} \) and \( x_j \), respectively. Hence, depending on the bit pattern of \( T \), there is either an extra NOT gate or no extra NOT gate on the bits of \( X \). The NOT gates are combined with other logic by synthesis tools and are not easily discernible from the netlist. Therefore, the secret \( T \) vector cannot be recovered from the netlist. Accordingly, even if the output wires of the modified ReLU function can be located, the attacker cannot replace the match detector with a zero detector to correctly recognize the zero values.

Using a modified ReLU function, whose output is \( \tilde{X} \), the functionality of the proposed match detector controlled by Hkey, \( HK \), is

\[
g(X', HK) = f_k(HK) \& f_i(X').
\]

Hence, \( f_i(X') \) detects whether \( X \) is zero. Assume that \( HK \) has \( c \) bits and the correct \( HK \) determined by the designer is \( HK^* \). The function \( f_k(HK) \) is \( hk_{c-1} \oplus hk_{c-1}^* \) & \( \ldots \& hk_0 \oplus hk_0^* \). Basically, \( f_k(HK) \) is “1” only when the input \( HK \) equals the correct Hkey, \( HK^* \). When \( HK = HK^* \), \( g(X', HK) = f_i(X') \) and it is “1” when the output of the original ReLU function is zero. Otherwise, \( g(X', HK) \) is always “0,” and all of the values, including zero values, will be sent to the compression block. \( HK^* \) is secret and its bits complement some of the bits in the HK input. The NOT gates at those bits of \( HK \) are merged with the AND functions of \( f_k(HK) \) and \( f_i(X') \). As a result, the \( f_k(HK) \) function cannot be separated from the netlist, and the Hkey cannot be nullified by replacing \( f_k(HK) \) with constant signal “1.”

B. Hardware-Assisted DNN Model Protection

In the white-box setting [25], a trained neural network architecture and its parameters are publicly known. To prevent attackers from illegally using the trained model in their own systems, obfuscation should be made on the model parameters by the designer before publishing the model on public platforms. In a DNN model, weights and biases are two sets of parameters affecting the accuracy. Corrupting either of them can make the model accuracy drop significantly. Our design chooses to obfuscate the biases since it also helps to better prevent bypassing the match detector for logic locking proposed in the previous section. It is easy to identify the registers used to store the MAC results and memories for recording the output feature maps from the target hardware. The match
detector is a combinational logic part between the registers and memories and hence is more vulnerable to be isolated and being compromised by removal attacks. By obfuscating the biases, even if the registers and memories are identified, the correct function of the logic part between them can not be restored without knowing the modifications made on the bias adders. As a result, the Hkey-controlled match detector cannot be bypassed.

From our simulations, it was discovered that the output accuracy of the DNN models is significantly degraded if at least the two most significant bits (MSBs) of every bias are modified. Utilizing this observation, our proposed scheme XORs a random-selected vector to the two MSBs of biases and provide these modified biases to the model-sharing platform. In the DNN accelerator of the authorized end user, the correct Mkey is used to XOR obfuscated biases back for the bias adders. There are many biases in a DNN model. However, the Mkey should have a limited length. In a DNN hardware accelerator, although multiple MAC blocks and bias adders are utilized to increase the throughput, their numbers are much smaller than those of the weights and biases in a DNN. Hence, the adders need to be shared in a time-multiplexed way to add different biases over a number of clock cycles according to the data scheduling scheme. Hence, the same vector should be utilized to modify the biases sharing the same adders over different clock cycles according to the data scheduling scheme of the DNN accelerator. Accordingly, the correct Mkey can be used for a bias adder for different clock cycles to restore the biases sharing that bias adder.

C. Hardware Implementation Architecture

The architecture of the DNN accelerator incorporating the proposed joint protection scheme is shown in Fig. 4. Multiple MACs are utilized to achieve high throughput. The implementations of the following modified bias adders, ReLU function blocks, and Hkey-controlled match detectors are first shown. Then, their complexities are analyzed in this section.

As mentioned in the previous section, at least the first two MSBs of each bias are XORed with the randomly chosen secret vector. In the bias adders of the hardware accelerators, biases are XORed back by using the correct MK, which equals the secret vector and can be stored in a tamper-proof memory. In Fig. 4, the segment of MK sent to the ith bias adder is denoted by MKi. To further protect the DNN model, some random XORs can be replaced by XNORs in the modified bias adders and the correct MK is changed accordingly. The XOR and XNOR gates are difficult to discern from the netlist. In this case, even if the correct MK is recovered, the original biases are still unknown.

In our design, the ReLU function is modified to have the output XORed with a random constant vector T. The T vector needs to be added back when the output feature map is read from the memory for processing the next layer of the DNN. Using a different T vector for each ReLU block makes it difficult to recover the original feature map. Hence, the same T vector is used in every modified ReLU unit in our design.

In our match detector, the output of the fx function is the same as that of a normal zero detector attached to an original ReLU function. If the HK input matches the correct key, HK*, then the detector result is passed intact to the compression block and the zero values are discarded. Otherwise, every data goes through the compression block and gets stored into the memory. In Fig. 4, the segment of HK sent to the ith match detector is denoted by HKi. To limit the length of HK, some match detectors can be replaced by normal zero detectors without any HK input, although the increase in the memory requirement will be less significant. It should be noted that a wrong HK increases the memory needed to store intermediate data without affecting the output of the DNN. More detailed discussions on the achievable security level of our protection scheme are provided in the next section.

Without the proposed protection scheme, the output of each MAC unit goes through a bias adder. The sign bit of the bias adder output tells whether the corresponding ReLU output is zero and is used by the compression block to decide whether to compress and store the value. Assuming 8-bit precision, a
TABLE I
COMPLEXITY COMPARISON OF ORIGINAL MAC UNIT, BIAS ADDER, AND PROPOSED DESIGN WITH 8-BIT PRECISION

|                                | XOR gate counts |
|--------------------------------|-----------------|
| MAC unit                       | 262             |
| Original bias adder            | 26              |
| Total                          | 288             |
| 2-bit Mkey insertion           | 2               |
| Modified ReLU function         | 3.5             |
| 8-bit Hkey-controlled match detector | 7.5   |
| Overhead                       | 13 (4.51%)      |

MAC unit consists of an 8-bit multiplier, adder, and register and each bias adder is an 8-bit adder. Each 2-input NAND or NOR gate is implemented by half of the area of an XOR gate, and each register with preset and clear pins requires three times the area of the XOR gate. The complexities of one MAC unit, one original bias adder are estimated in Table I.

The area overheads of the proposed scheme include the XOR gates introduced in the modified bias adders, the modified ReLU functions, and the Hkey-controlled match detectors. Modifying a bias adder using 2 bits of the Mkey needs two XOR gates. The modified ReLU function with 8-bit input can be implemented by seven AND gates since XORing with the constant $T$ vector only requires NOT gates, which are combined with other logics by the synthesis tool. Similarly, the match detector can be implemented by 16-input AND tree according to (3). These complexities are also listed in Table I. Compared to the original bias adder and MAC unit, the proposed protection scheme only causes $13/288 = 4.51\%$ area overhead. Considering that the memory contributes to a substantial portion of the overall area and there is also a compression block, the area overhead brought by the proposed design to the overall accelerator is negligible. The MAC unit has a multiplier and an adder in a feedback loop. The data path of the modified bias adder, modified ReLU function, and match detector is shorter than that of the MAC unit. Hence, the overall critical path of the design is not increased by the proposed design.

IV. EXPERIMENT RESULTS AND SECURITY ANALYSES

This section carries out experiments and analyzes the effectiveness of the proposed joint logic locking and DNN model protection scheme.

A. Security Analyses of the Proposed Logic Locking

The main goal of hardware attackers is to utilize counterfeit circuits without authorization from the circuit designer. They try to derive the correct Hkey or remove the part of the circuit to nullify the Hkey. The SAT and removal attacks are the two potential major threats that may compromise the proposed logic locking. The resistance to the SAT attacks and removal attacks is analyzed in this section.

1) Resistance to SAT Attacks: From Section II-C, by converting the netlist to conjunctive normal formula and querying a functioning chip, the SAT attack excludes the wrong keys that corrupt the primary output of the target circuit. After all wrong keys are excluded, any of the remaining keys can be used as a correct key. In our design, if a wrong Hkey is used, the output of the DNN does not change although the amount of intermediate data to store increases by several times. As a result, none of the wrong Hkeys can be excluded by the SAT attack. Similarly, our proposed scheme is resilient to other attacks based on the SAT attack, such as the AppSAT attack.

2) Performance Degradation Under Wrong Hkeys: As explained in the previous paragraph, SAT attacks are not able to exclude any wrong Hkeys in our proposed scheme. If a random wrong Hkey is utilized, the amount of intermediate data to store is substantially increased as shown in Fig. 5. In our experiments, a wrong Hkey segment is used for each match detector. To collect the data, four images in the ILSVRC-2012 dataset [30] are fed to three popular DNN models: 1) AlexNet; 2) ResNet-18; and 3) VGG-11. Output feature maps of each layer need to be compressed and stored into memory. Three compression formats, CSC, RLC, and BitMap, are applied to compress the intermediate data. When the Hkey segment sent to every match detector is wrong, all zero values are mistakenly considered as nonzero and sent to the compression block, which converts the data into different formats according to the compression scheme without discarding any data. The sizes of the memories needed to store the compressed data with and without zero values discarded are recorded and their ratio is computed for each layer as shown in Fig. 5. The overall ratio is calculated by dividing the sums of the memories required for each layer. The memory requirements for some layers are increased by more than 8 times and the overall memory requirement is increased by 1.5 to 3.7 times depending on the network and compression schemes.

The sparsity of the output feature maps from different layers of the DNN model varies. In general, if the original data has higher sparsity, then the ratio of memory increase as a result of using a wrong Hkey is larger since more zeros that should have been discarded are stored into the memory. Take the conv1 and conv2 layers in AlexNet as examples. The percentage of zeros in their output feature maps are 59% and 81%, respectively. Hence, for different compression methods, the memory size increase ratio caused by wrong Hkey on conv2 layer is always larger than that on conv1 layer. As for the overall memory requirement increase ratio caused by wrong Hkey, ResNet-18 is smaller than the other two models. Although the memory sizes are increased more than three times under wrong Hkey in certain layers of ResNet-18, such as conv14, conv15, and conv16, those layers have smaller output feature maps compared to the other layers.

Besides nonzero values, the information about their locations generated by compression also needs to be recorded. Storing dense data compressed by the CSC or RLC methods requires larger memory comparing to recording the results compressed by the BitMap scheme [4]. When all zero values are mistakenly considered as nonzero under wrong Hkey, the original sparse intermediate results become dense. As a result, for the same DNN model, the Bitmap compression method causes the smallest memory increase ratio when wrong Hkey is utilized. Take AlexNet as an example. From Fig. 5, the overall memory increase ratio is 3.2, 3.45, and 3.71 times, when the BitMap, CSC and RLC compression, respectively, are utilized.
Fig. 5 shows the results when the Hkey segment fed to all match detectors are wrong. However, a randomly selected \(HK_i\) may be accidentally equal to \(HK^*_i\). Assume that Hkey has \(k_H\) bits and \(m\) out of the \(n < k_H\) match detectors are locked by \(HK\). In this case, \(c = k_H/m\) key bits are used to lock each of those \(m\) match detectors. Since \(f_c(HK)\) is a \(c\)-bit equality tester as discussed in the previous section, only one of the \(2^c\) patterns of possible \(HK_i\) is the correct key segment. Hence, the probability that a random Hkey segment for a match detector is correct is \(1/(2^c)\). Given a randomly guessed vector for Hkey, the expected number of match detector with correct \(HK_i\) is \(m \times 1/(2^c) + n - m\). This number reduces with larger \(m\) and is minimized when \(m = n\), which means that the \(k_H\)-bit Hkey should be evenly distributed to all \(n\) match detectors. When \(k_H\) is smaller than \(n\), Hkey cannot be used to lock every match detector. In this case, \(m\) should be set to \(k_H\).

Simulation results shown in this section utilize ReLU as the activation function. If SeLU or ELU is actually used, compression still applies since they output almost the same value for negative inputs with larger magnitudes. However, unlike the ReLU function, their outputs are not constant for all negative inputs. As a result, the compression ratio will be lower and accordingly the relative memory size increase that the proposed scheme can achieve will be smaller.

3) Removal Attack Resistance: Removal attack [21] is another hardware threat to logically locked DNN accelerators. By analyzing the netlist of the circuit, it tries to remove the logic-locking block and replace its output by a constant signal that makes the circuit function correctly. AND/NAND trees generate the outputs of the match detectors locked by Hkey in our proposed design. If the outputs are replaced by “0”s, all values are passed to the compression block and stored into memory, which makes the memory requirements significantly increase as shown in Fig. 5. If the outputs are replaced by “1”s, no value is stored into memory, and the DNN accelerator output will be totally wrong and cannot be used. Therefore, our proposed design is not subject to removal attacks.

A more powerful attacker may have detailed knowledge about the architecture of the DNN accelerator, and he/she may identify the logic parts in the netlist performing certain functions. Registers and memories can be easily located in the netlist, and their inputs and outputs are identifiable. The output of the ReLU function is connected to registers in the compression block in some designs. Even if it is located by the attacker and the match detector is replaced by a zero detector, the zero values are not correctly identified since they have been XORed with the secret vector \(T\) as discussed in Section III-A. The MAC units consist of registers too. Another potential attack is to replace all the logic between the MAC and compression blocks shown in Fig. 4 by bias adders, ReLU units, and zero detectors. However, both XOR and XNOR gates can be used to connect the Mkey and obfuscated bias inputs as discussed in Section III-C. These XOR and XNOR gates are merged with other logic gates by the synthesis tool and are not separable from the netlist. As a result, the modifications made on the bias adders are secret to the hardware attacker, and this removal attack will not be successful.

B. Security Analyses of the Proposed Model Protection

The DNN model attackers try to recover the original DNN model from the obfuscated model. Then, the attackers can claim the ownership of the original model and distribute it to
TABLE II
TOP-1 ACCURACY (%) OF THE ORIGINAL DNN MODEL, OBFUSCATED MODEL, AND OBFUSCATED DNN MODEL WITH FINETUNE ATTACK APPLIED USING TRAINING SETS OF DIFFERENT SIZES

| DNN models | Original model accuracy | Obfuscated model accuracy | Obfuscated model with finetune attack applied using α of original training dataset |
|------------|------------------------|--------------------------|--------------------------------------------------------------------------------|
|            |                        |                          | α = 1%  | α = 3%  | α = 5%  | α = 10% |
| AlexNet[28] | 86.72     | 10.00                   | 76.72   | 54.73   | 31.99   | 59.44   | 27.28   | 65.87   | 22.85   | 71.91   | 14.81   |
| ResNet-18 [1] | 96.16  | 10.68                   | 85.48   | 59.77   | 36.39   | 72.2    | 23.98   | 78.4    | 17.76   | 82.48   | 13.68   |
| VGG-11[29]  | 92.35     | 16.94                   | 75.41   | 60.33   | 32.02   | 71.18   | 21.17   | 75.61   | 16.74   | 80.2    | 12.15   |

unauthorized users. In this section, the DNN model accuracy degradation achieved by the proposed bias obfuscation is first presented. Finetune [26] attack may be used to recover the original DNN model under the threat assumptions introduced in Section II-B. The resistance to the finetune attack of our design is also demonstrated through simulation results in this section.

1) Accuracy Drop on Obfuscated Model: Three DNN models, AlexNet, ResNet-18, and VGG-11, with the CIFAR-10 dataset[31] are simulated to collect the accuracy results. It is assumed that each weight, bias, and intermediate result is represented by a 16-bit fixed-point number. All the biases are divided into 128 groups in our simulations, and the two MSBs of every bias in the same group are XORed with the same two-bit random vector. Hence, the overall length of the Mkey should be 256 bits. The top-1 accuracy of the original and obfuscated DNN models are shown in Table II. It can be observed that obfuscating biases can effectively reduce the accuracy of DNN models.

As discussed in Section II-A, the DNN model attackers may have access to a small portion of the training set as thief dataset [26]. By using the thief dataset, attackers can finetune the obfuscated model to increase the accuracy. To show the resilience of the proposed protection scheme to the finetune attack, simulations with α = 1%, 3%, 5%, and 10% of the training set as the thief dataset are carried out. The thief dataset is limited to 10%, since the labeled training data is typically kept secret by the model provider. The simulation results are shown in Table II. The larger the thief dataset, the higher the accuracy that the finetune attack can achieve. Nevertheless, even if 10% of the original training set is available to the attacker, the accuracies of the finetuned obfuscated AlexNet, ResNet, and VGGNet are only 14.81%, 13.68%, and 12.15%, respectively, which are much lower than those of the original models.

Finetune attack has been performed on ResNet-18 obfuscated by the method proposed in [26]. In that paper, the Fashion-MNIST [33] is used as the training set. When 10% of the original training set is available to the attacker, the accuracy only drops by around 5% compared to that of the original model. Simulation using the Fashion-MNIST dataset is also done on ResNet-18 obfuscated by the proposed design. From our simulation results, when the thief dataset is 10%, the accuracy of the finetuned model drops by 9.17% compared to the original accuracy. This result clearly shows that the proposed obfuscation scheme is more effective than the obfuscation method in [26] in terms of preventing finetune attack.

2) Allocation of Mkey: If the probability that an attacker can randomly guess the correct key is $1/2^k$, then the system is said to be k-bit secure. Assume that there are $n$ bias adders and $k_M$-bit Mkey. As mentioned previously, at least the two MSBs of the biases are obfuscated to generate significant accuracy loss in the model. If $k_M > 2n$, then the $k_M/n$ MSBs of each bias can be obfuscated by XORing with the bits in Mkey. Additional obfuscation on the less significant bits of the biases changes the magnitudes of the biases by a smaller amount. In this case, the security level that the proposed design can achieve is at least $2n$-bit, and does not significantly increase with longer Mkey. When $k_M < 2n$, $k_M/2$ instead of $n$ groups of biases can be chosen to be obfuscated and each bias in those groups are XORed with the bits in Mkey in the two MSBs. As long as a significant portion, if not all, of the biases are obfuscated, the accuracy of the model may still drop significantly. Hence, the security level of proposed protection scheme is $k_M$-bit secure and increases linearly with longer Mkey. A longer Mkey makes it more difficult to guess the correct Mkey, but also requires a larger tamper-proof memory to store. Take a DNN hardware accelerator with 128 bias adders implementing AlexNet as an example. When the Mkey length is 128-bit, 64 bias adders can be chosen to be obfuscated by the $2 \times 64 = 128$-bit Mkey, and the corresponding biases in the model are modified accordingly. Without the right Mkey, the output accuracy is dropped to 10%, which is 76.72% lower than the accuracy of the original model. This accuracy drop is similar compared to using a 256-bit Mkey to obfuscate the two MSBs of each bias. Nevertheless, a 256-bit Mkey requires the attacker use a larger number of trails to randomly guess the correct key comparing with a 128-bit Mkey by utilizing larger tamper-proof memory.

3) Information Leakage Analyses: To show that the proposed DNN protection method does not leak information about the original model, the finetune attack is also applied to a model initialized by random parameters. The accuracy of the randomly initialized model after the finetune training is shown in Fig. 6. The accuracies of the original model and the proposed obfuscated model after the finetune attack listed in Table II are also replotted in this figure. It can be observed that under the same size of the thief training set, finetuning the randomly initialized model and DNN model initialized by the obfuscated parameters leads to similar accuracy. More importantly, for both cases, the accuracies are much lower than that of the original model. This indicates that initializing a

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model with the parameters obfuscated by the proposed methods does not leak more information about the original DNN model compared to initializing the model randomly.

V. DISCUSSIONS

This article proposes a joint protection scheme for DNN hardware accelerator and model. The goals of the hardware and DNN model attackers are different. For the proposed protection scheme, the hardware attacker tries to derive the Hkey, which can help to unlock counterfeit chips. However, a correct Mkey does not help to recover the original DNN model, which is the goal of the model attacker. In our proposed DNN model protection scheme, the biases that are added in the same adder of the hardware accelerator are obfuscated by the same vector. Without perfect knowledge about the scheduling scheme and the netlist of the locked circuit, the model attacker does not know which bits of the Mkey are used to obfuscate each bias and how the original biases are obfuscated. Accordingly, the original model cannot be recovered. This is different from the protection scheme developed in [27], which hands out trusted end-users correct keys containing the indices about the swapped matrices. For that protection scheme, the attacker is able to recover the original model by using the correct key. Hence, brute-force attacks can be used to derive the correct keys and accordingly recover the original model [27]. On the contrary, even if the correct Mkey is discovered, the model obfuscated by our proposed method still cannot be recovered.

Since each $HK_i$ is short, one potential attack is to try all possible patterns of $HK_i$. If a certain pattern leads to noticeably smaller memory requirement, then it is the correct key segment. However, it is difficult to separate the bits in one $HK_i$ from those of another. One reason is that the synthesis tool merges logic gates of different match detectors since their outputs are mixed in the calculations for compression. Besides, depending on the networks and layers, there may be other blocks, such as max pooling, in a DNN accelerator in addition to those shown in Fig. 4. As a result, it is very difficult to tell the boundaries of different match detectors and separate different $HK_i$.

Power side-channel attacks are more popular than other side-channel attacks for recovering secret keys. Attackers construct a predicted power consumption model based on guessed keys and compare it with actual power traces of the circuit with the correct key. Unlike the designs considered in [34], whose logic locking block contributes to substantial area overhead, such as 35%, the logic locking component accounts for much less than 5% of the overall DNN accelerator area in our design. As a result, the inserted key only affects a very tiny part of the circuit, and the signal-to-noise ratio is too low for the attacker to tell the correct key.

VI. CONCLUSION

In this article, a novel scheme is proposed to jointly protect DNN hardware accelerators and models. Using the proposed scheme, the memory requirement is increased by several times when the wrong Hkey is used. This leads to substantial increases in memory size, power consumption, and latency, which make the hardware accelerator unusable. Our proposed scheme can also effectively resist SAT and removal attacks, which are among the most powerful attacks for logic locking schemes. Our proposed design protects the DNN model as well. Unlike previous approaches, our scheme is scalable and more secure. Future research will focus on developing obfuscation schemes for DNN models and its accelerators resisting more powerful attacks.

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