XNAP: a hybrid pixel detector with nanosecond resolution for time resolved synchrotron radiation studies

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Abstract. The XNAP collaboration is constructing a hybrid pixel X-ray detector based on a monolithic silicon avalanche photodiode (APD) sensor array aiming at applications in synchrotron radiation facilities. The 2D detector is capable of identifying which individual electron bunch produces each detected X-ray photon, even when the storage ring operates in multibunch filling modes. This instrument is intended to be used in X-ray Photon Correlation Spectroscopy and Nuclear Resonance experiments and serve as a demonstrator for various kind of time resolved diffraction and scattering applications as well as a very high count rate device. The detector is a 1 kilopixel device with 280 µm pitch that implements both counting mode up to MHz frame rates and event-by-event readout with sub-nanosecond time resolution. The paper describes the detector design and some results obtained with small 4x4 pixel prototypes that have been built and measured to make and validate the most critical choices for the final detector.

1. Introduction
Avalanche photodiodes (APDs) have been used for direct X-ray detection in synchrotron radiation experiments since more than two decades [1, 2]. The good time resolution, of the order of 1 ns, as well as the very short dead time provided by these devices when operating in linear amplification mode make APDs the detector of choice for X-ray photon counting detection applications either at high count rates or requiring very good pulse pair time resolution. During the same period, hybrid pixel area detectors based on PIN silicon sensors have gained a very important place in the synchrotron community taking advantage of the tremendous progresses in both microelectronics and advanced interconnection technologies. The success of hybrid pixel technology relies on the combination of the high detection sensitivity provided by the direct detection semiconductor sensors and the parallel signal processing capabilities of the high-density readout schemes implemented in those devices. Pixel detectors in use at synchrotron facilities today operate at frame rates above one kilohertz [3] and next generation devices are expected to push that limit by about one order of magnitude [4]. With the current sensor technology and appropriate readout schemes, pixel detectors could reach time resolution of the order of 100ns but that would be still far from the time resolution capabilities of APD based devices.
The XNAP project aims at filling the gap between those two, today different, types of X-ray detectors by constructing and demonstrating the feasibility of a hybrid pixel device with nanosecond time resolution based on a monolithic APD sensor array. In addition to being a demonstrator for various kinds of time resolved diffraction and scattering applications and a very high count rate device, the detector is expected to be used in X-ray Photon Correlation Spectroscopy and Nuclear Resonance experiments.

2. The XNAP detector
The detector design is based on a 1 kpixel monolithic pixelated APD sensor with 32×32 pixels arranged in a squared matrix with 280 µm pitch. The front-end readout is implemented by four application specific CMOS integrated circuits, each one including 256 readout channels. The readout chips are connected by bump-bonding at the back of the detector but not directly on the surface of the sensor but through an interposer that serves as mechanical support and improves the thermal dissipation of the assembly. The interposer also provides a certain level of X-ray shielding to reduce the irradiation of the readout chips.

The complete front-end assembly is mounted on a cooling block and wire bonded to a PCB that provides electrical power and routes all the digital signals to the readout electronics. The main electronic board implements the overall functional control and data readout of the detector and includes FPGA based sub-nanosecond timestamping units as well as an embedded Linux processor that communicates through a gigabit Ethernet link. All the components of the XNAP design, including the HV bias supply for the APD sensor will be mounted in the detector head.

The first versions of the various elements of the XNAP detector are either already built or in advanced phase of design. Certain critical technical choices such as the APD sensor structure and the in-pixel functionality have been studied and validated by building small prototypes with 4×4 pixels like the one shown in figure 1. The experimental results shown in the rest of this paper come from measurements taken with those small 16 pixel prototypes.

![Figure 1. 4×4 pixels XNAP prototype assembly. The pictures show the squared APD sensor array and the test readout ASIC bump-bonded at each side of a high-density interconnect PCB interposer.](image)

2.1. Sensor
The silicon sensor array is produced by Excelitas Technologies based on several fabrication processes already validated but never combined in the same device. Various types of sensor structures have been produced and tested, all of them pixelated versions of 120 µm thick reach-through APDs in which the avalanche multiplication region is very close to the cathode of the device. If the cathode is pixelated, every pixel can be seen as an independent diode with its own avalanche region. This is the structure usually found in the existing monolithic linear arrays and has as main disadvantage that the electric field and therefore the multiplication gain drops between pixels producing insensitive dead areas. The best result obtained with optical methods in XNAP 4x4 sensors with pixelated cathode is a dead area of 33%, i.e. 50 µm between pixels, at 75% drop of the multiplication gain.
The option of pixelating the anode of the APD instead of the cathode has several very attractive properties such as the absence of dead areas as the multiplication region is uniform and continuous, relaxed requirements on high voltage isolation at the readout side of the sensor and even the potentiality of going for smaller pixels in future detector designs. The difficulty in building and using this kind of structures lies on the need of obtaining sufficient pixel isolation resistance to avoid signal coupling between neighbour pixels. Figure 2 shows the response obtained by scanning a focused X-ray beam across the centre of a row of pixels in one of the XNAP 4×4 test devices. The smooth spatial response as well as the lack of cross-talk or other undesired effects has driven the choice of a sensor with pixelated anode as the baseline for the final 32×32 sensor currently in fabrication.

![Figure 2](image)

**Figure 2.** Spatial response of the 4×4 device when a 100 µm FWHM focused 8keV X-ray beam is scanned across the center of pixel row.

### 2.2. Readout

The XNAP readout front-end will be implemented by four identical CMOS readout chips, 16×16 pixels each. As other photon counting pixel detectors, each pixel in the sensor is connected to an individual channel in one of the readout chips that includes an amplification and discrimination chain that can operate with subnanosecond pulses. Every pixel includes also two counters and a mechanism to send the time information of incident photons to timestamping units in the FPGA at the external readout electronics.

The pixel functionality in the 16×16 asics has little variants with respect to the one implemented in the 4×4 test chips for which the readout scheme is described in a previous publication [5]. In counting mode operation, the number incident photon events are accumulated in one of the counters built in the pixels. In event-by-event operation, each photon impinging on one of the pixels of the detector produces a pulse that is timestamped by the FPGA, that then can extract the x and y coordinates of the particular pixel from the readout chip.

All the pixels in the detector are grouped in 16 separate blocks of 64 pixels. Each group includes all the control and data lines required to be read out independently from the others. The chip readout is synchronously driven by a clock from the FPGA that can be as fast as 250 MHz with the current 16×16 chip prototypes although it is expected to reach 400MHz in the final version. At that clock speed, reading the four less significant bits of the built-in counters of each pixel will take less than 1µs, what will allow frame rates beyond 1 MHz in counting mode operation. In the case of event-by-event readout, reading the pixel coordinates at 400 MHz would take less than 50 ns. That short readout time will allow high time resolution operation and therefore photon bunch discrimination in multibunch modes up to average count rates close to 10^8 photons per second in the whole detector area and with rather negligible dead time if the photon detection events are uniformly distributed across the 16 readout channels.
3. Tests

As mentioned before, the current XNAP test systems are based on 4×4 pixel sensor-asic assemblies that are functionally equivalent to the final ones in the 32×32 pixel detector. The readout electronics and software used for X-ray tests do not include all the operation modes and capabilities of the final detector. In addition to the test systems, the first prototypes of the 16×16 chips and the readout electronics for the final detector have also been built and tested.

The XNAP test systems have been evaluated with X-rays using radioactive sources, a laboratory microfocus source and at two ESRF beamlines (ID18 and BM5). The detectors have shown proper operation, at the various photon energies used for tests, from 5.9 keV to 25 keV, although the detection efficiency drops rapidly with photon energy due to the small thickness of the silicon sensors. With the exception of bad pixels due to defective interconnection, the devices have shown good spatial response and uniformity as it is illustrated in figure 2.

The detectors have been operated by either using the in-pixels counters or the event-by-event readout mode. In this last case high resolution timestamping has been achieved by either an external TDC or a fast digital oscilloscope. The time resolution and count rate capabilities of the XNAP pixels are analogous to those obtained with discrete APDs of the same thickness, a typical value being 0.8 ns for 14 keV photons impinging in the center of the pixels. Figure 3 shows, for instance, part of the structure of an ESRF bunch train measured with one pixel of a XNAP test device. The bunches separated by 2.8 ns are clearly distinguishable and the figure shows how the last bunch in the train carries between four and five times more electrons than the others. The intrinsic time resolution of the detector has been also measured by precise gating of the counters in the readout chip and the results are similar to those obtained by timestamping in even-by-event mode.

![Figure 3. Time histogram of X-ray photons detected at the ID18 ESRF beamline in 7/8+1 filling mode.](image)

References

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