Enabling a Programming Environment for an Experimental Ion Trap Quantum Testbed

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Abstract—Ion trap quantum hardware promises to provide a computational advantage over classical computing for specific problem spaces while also providing an alternative hardware implementation path to cryogenic quantum systems as typified by IBM’s quantum hardware. However, programming ion trap systems currently requires both strategies to mitigate high levels of noise and also tools to ease the challenge of programming these systems with pulse- or gate-level operations.

This work focuses on improving the state-of-the-art for quantum programming of ion trap testbeds through the use of a quantum language specification, QCOR, and by demonstrating multi-level optimizations at the language, intermediate representation, and hardware backend levels. We implement a new QCOR/XACC backend to target a general ion trap testbed and then demonstrate the usage of multi-level optimizations to improve circuit fidelity and to reduce gate count. These techniques include the usage of a backend-specific numerical optimizer and physical gate optimizations to minimize the number of native instructions sent to the hardware. We evaluate our compiler backend using several QCOR benchmark programs, finding that on present testbed hardware, our compiler sees a reduction in two-qubit native operations by 2.40 times and one-qubit native operations by 6.13 times.

Index Terms—compilation, multi-level optimization, quantum computing, ion trap

I. INTRODUCTION

Quantum computing promises new computational capabilities over classical computing with quantum algorithms having a theoretical exponential speedup over some classical algorithms [1]. However, given the high error rates of present qubits (quantum bits), computational capability today reaches only as far as is achievable on NISQ (Noisy Intermediate Scale Quantum) devices, near-term quantum computers with 50-100 qubits which provide highly noisy output [2]. Limited coherence time and high gate error rates require compilers for NISQ systems to minimize the number of quantum gates (instructions) and to embrace error mitigation techniques to increase the likelihood of useful results [3].

In this work, we detail our implementation of an XACC [4] compiler backend targeting an experimental quantum testbed hosted by the GTRI (Georgia Tech Research Institute) Quantum Systems Division [5]. This new compiler backend provides a hardware-agnostic programmer-driven flow for programming the testbed using quantum circuits written inline in C++ via QCOR [6]. Our new QCOR-based implementation provides a contrast with the existing testbed tooling, which is based on proprietary software more oriented towards hardware experts. Moreover, by integrating with QCOR, programmers gain access to existing QCOR tooling, such as quantum assembly parsers, circuit optimizers, a variational workflow, and a standard library of quantum subroutines.

The current work provides the following contributions:

- We demonstrate a new ion trap backend for XACC that interacts with the low-level capture system used to program and interact with a target ion trap testbed.
- Through the use of multi-level optimization with QCOR and XACC, we show how optimizations for a quantum program can be implemented at the hardware-agnostic level by QCOR and at the hardware-specific level in particular backends.
- We explore the usage of these optimizations to improve circuit fidelity and reduce native gate count.
- We investigate native gate count reduction achievable with future hardware upgrades.

To evaluate our work, we run a set of QCOR example programs against the backend, with the existing control code configured to respond with simulation results. We also compare gate count with the existing compiler for the testbed.

A. Motivation for a New Ion Trap Backend

The current approach to interacting with the GTRI testbed requires using IGOR Pro (a programming environment focused on data visualization) and detailed knowledge of the testbed mechanics — generally, it is hardware expert-driven. An email-based submission scheme shown in Fig. 1 improved this situation by allowing for submission and parsing of quantum
II. BACKGROUND

A. Ion Trap Quantum Computers

Quantum computers based on an ion trap realize qubits by manipulating the internal spin-like degrees of “trapped” atomic ions with electromagnetic radiation. Native operations can be broadly categorized as either single- or multi-qubit operations which may comprise different universal gate sets. For example, single qubit operations include $R_\phi(\theta)$, a rotation of $\theta$ around an axis $\phi$ in the equatorial plane of the Bloch sphere, shown in (3) [7]. For the multi-qubit entangling operation we consider the Mølmer-Sørenson (MS) interaction [8], [9], which defines the MS gate in (5) [6].

$$
\sigma_\phi = (\cos \phi) \sigma_x + (\sin \phi) \sigma_y
$$

$$
R_\phi(\theta) = \exp(-i\sigma_\phi \theta/2)
$$

$$
= \begin{bmatrix}
\cos \theta/2 & -ie^{-i\phi} \sin \theta/2 \\
-ie^{i\phi} \sin \theta/2 & \cos \theta/2
\end{bmatrix}
$$

$$
\beta_{1r} = -ie^{i(-1)\phi_L + (-1)^r \phi_R} \sin \alpha
$$

$$
MS(\alpha) = \exp(-i\alpha(\sigma_{\phi_L} \otimes \sigma_{\phi_R}))
$$

$$
= \begin{bmatrix}
\cos \alpha & 0 & 0 & \beta_{11} \\
0 & \cos \alpha & \beta_{10} & 0 \\
0 & \beta_{01} & \cos \alpha & 0 \\
\beta_{00} & 0 & 0 & \cos \alpha
\end{bmatrix}
$$

When the MS phase angles for the left and right qubits, $\phi_L$ and $\phi_R$ respectively, are zero, we have $\sigma_{\phi_L} = \sigma_{\phi_R} = \sigma_x$, yielding the $XX$-Ising gate shown in (7). For simplicity, we will use this convention for the rest of this work. The $XX$ gate can be used to realize a CNOT operation when combined with single qubit gates such as those shown in Fig. 2 [7], [10].

$$
XX(\alpha) = \begin{bmatrix}
\cos \alpha & 0 & 0 & -i \sin \alpha \\
0 & \cos \alpha & -i \sin \alpha & 0 \\
0 & -i \sin \alpha & \cos \alpha & 0 \\
-i \sin \alpha & 0 & 0 & \cos \alpha
\end{bmatrix}
$$

Together, arbitrary single-qubit gates provided by $R_\phi(\theta)$ and the $XX$ entangling gate support universal quantum computation [11], [12]. Additionally, ion trap systems can support all-to-all qubit connectivity and parallel gate execution using tightly-focused individual gate beams [13] or ion transport with stationary beams [14], [15].

B. GTRI Quantum Testbed

Researchers at GTRI have built a quantum testbed based on an ion trap [5], [16]. The physical apparatus consists of a stationary set of lasers which operate on ions (qubits) in the chain. The chain itself is transported to allow the lasers to target different qubits [5]. Originally, the gate laser beams always targeted two ions simultaneously, but due to recent equipment upgrades allowing gate beams to target individual qubits, we assume single-qubit addressing in this work. The testbed does not have a tightly-focused laser beam for each ion, so we assume nearest-neighbor connectivity for two-qubit gates and serialized (i.e., no parallel) single-qubit gates.

When configured as a general-purpose quantum computer as we assume in this work, the testbed has the $XX(\pi/4)$ gate and, for ease of calibration, the subset of $R_\phi(\pi/2)$ gates with $\theta = \pi/2$ as its native operations. The control software for the testbed includes a rudimentary compiler that converts a dialect of quantum assembly to a sequence of native operations ($XX(\pi/4)$ and $R_\phi(\pi/2)$) according to which the control software programs FPGAs as needed to run the circuit on hardware. An example of the sequence for a Bell state circuit is shown in Table I. The existing compiler decomposes CNOTs as shown in Fig. 2 and it applies arbitrary single-qubit unitaries using an average of 3.25 primitive $R_\phi(\pi/2)$ rotations [3].

C. QCOR and XACC

Oak Ridge National Laboratory has developed the QCOR compiler specification [6] and a reference implementation [17]. Both aim to accelerate the development of new applications on NISQ hardware by providing a unified, automated software
TABLE I
SEQUENCE OF NATIVE OPERATIONS PRODUCED BY THE EXISTING
COMPILER FOR THE BELL STATE CIRCUIT $H \otimes CNOT_{0,1}$.

| Operation | Target Ion | $\phi$ |
|-----------|------------|--------|
| $R_x(\pi/2)$ | 0 | $-\pi/2$ |
| $R_y(\pi/2)$ | 0 | $-\pi/2$ |
| $R_z(\pi/2)$ | 0 | $-\pi$ |
With a $2 \times 2$ goal unitary $G$ and rotations $\vec{\phi} = (\phi_1, \phi_2, \ldots, \phi_n)$, the optimization function to minimize is shown in (10). Like the existing compiler [5], we have always found $n \leq 4$ in our testing; future work should prove that some gates require four $R_{\phi}(\pi/2)$ rotations, since a $Z$-Y decomposition for example requires a maximum of only three rotations [11]. The absolute value in (9) is squared to simplify finding the gradient $\nabla f$ from (10) using the product rule. We pre-computed this gradient for $n \in \{1, 2, 3, 4\}$ using Mathematica and converted the result into parameterized C++ code.

$$A_{ex}(\vec{\phi}) = R_{\phi_n}(\pi/2) \cdots R_{\phi_2}(\pi/2) R_{\phi_1}(\pi/2)$$  
$$f(\vec{\phi}) = 4 - |\text{Tr}(G^\dagger A(\vec{\phi}))|^2$$  
$$= 4 - \text{Tr}(G^\dagger A(\vec{\phi})) \text{Tr}(G^\dagger A(\vec{\phi}^*)$$  

Choosing $A_{ex}(\vec{\phi})$ as the actual decomposition $A(\vec{\phi})$ allows the aforementioned strategy to produce an approximately “exact” decomposition. We found we can make further optimizations by changing $A(\vec{\phi})$ or skipping decomposition entirely depending on the situation. The following sections describe our situation-specific optimizations:

1) Decomposition up to an X Rotation: It is easy to show that $RX(\theta)$ commutes with $XX$, but $RY(\theta)$ and $RZ(\theta)$ only commute with $XX$ if $\theta \equiv 0 \mod 2\pi$ [7]. (In this work, we use $RX$, $RY$, and $RZ$ as defined in [1].) Thus, if an $XX$ gate follows the sequence of single-qubit gates, we decompose $G$ up to $RX(\theta)$ for some $\theta$ and then commute the $RX(\theta)$ to the other side of the $XX$ gate, to be decomposed later. We achieve this with the optimizer by choosing $A_x(\vec{\phi})$ as $A(\vec{\phi})$ per the definition shown in (11). Note this requires a separate pre-computed gradient to pass to the optimizer.

$$A_x(\vec{\phi}) = RX(\phi_n) R_{\phi_{n-1}}(\pi/2) \cdots R_{\phi_2}(\pi/2) R_{\phi_1}(\pi/2)$$  

In some rare cases (0.05% of cases we tested), the optimizer fails to find a decomposition up to an $RX(\theta)$ such that $f(\vec{\phi})$ is less than the configured threshold, possibly due to floating point rounding errors. In such cases, we fall back to the exact decomposition $A_{ex}(\vec{\phi})$ shown in (8) to avoid harming fidelity.

2) Decomposition up to a Z Rotation: Relative phase shifts, i.e. $Z$ rotations, do not affect measurements when measuring in the standard computational basis of $Z$-eigenstates. So if a measurement follows the sequence of single-qubit gates, we decompose $G$ up to $RZ(\theta)$ for some $\theta$ and then discard the $RZ(\theta)$ gate entirely. Similar to the previous optimization, the numerical optimizer finds $\theta$ for us after we choose $A_x(\vec{\phi})$ as $A(\vec{\phi})$ per the definition below in (12). Note this again requires a separate pre-computed gradient to pass to the optimizer.

$$A_z(\vec{\phi}) = RZ(\phi_n) R_{\phi_{n-1}}(\pi/2) \cdots R_{\phi_2}(\pi/2) R_{\phi_1}(\pi/2)$$  

The existing compiler has the ability to perform this optimization, which we have enabled in our evaluation.

3) Decomposition starting with a Z Rotation: Immediately after state preparation, a qubit is in state $|0\rangle$, and $RZ(\theta) |0\rangle = |0\rangle$ up to a global phase regardless of angle $\theta$. Consequently, we ignore an initial $Z$ rotation when decomposing the first single-qubit gate sequence for any qubit not preceded by a two-qubit gate acting on that qubit. This optimization can be combined with the previous two optimizations as well as generation of an exact decomposition; we ask the numerical optimizer for from-Z-to-exact, from-Z-up-to-X, and from-Z-up-to-Z decompositions using the following respective definitions for $A(\vec{\phi})$:

$$A_{z,ex}(\vec{\phi}) = R_{\phi_n}(\pi/2) \cdots R_{\phi_2}(\pi/2) RZ(\phi_1)$$  
$$A_{z,x}(\vec{\phi}) = RX(\phi_n) R_{\phi_{n-1}}(\pi/2) \cdots R_{\phi_2}(\pi/2) RZ(\phi_1)$$  
$$A_{z,z}(\vec{\phi}) = RZ(\phi_n) R_{\phi_{n-1}}(\pi/2) \cdots R_{\phi_2}(\pi/2) RZ(\phi_1)$$  

Similar to the previous optimization, we discard the $RZ(\phi_1)$ gate of the decomposition. Note that (13)-(15) each require a new, separate pre-computed gradient for $f(\vec{\phi})$.

The existing compiler supports the from-Z-to-exact case [5], producing a decomposition equivalent to [13]. We enable this optimization together with the previous exact-up-to-Z optimization in our evaluation of the existing compiler, henceforth calling this combination “$RZ$ optimizations.”

4) Ignoring Identity: If setting $A(\vec{\phi})$ equal to the identity matrix $I$ and invoking $f(\vec{\phi})$ reveals that $G$ is closer than the configured tolerance to $I$, we skip generating any rotations at all.

5) Discarding Trailing Gates: If the sequence of gates immediately precedes the end of the circuit, without an explicit measurement by the programmer, we discard all the gates entirely, as they will not affect measurement outcomes.

D. Future Hardware Upgrades

In anticipation of future hardware upgrades, namely a tightly-focused beam for each individual ion, we implement rudimentary support for all-to-all qubit connectivity and parallel single-qubit operations in our compiler, either of which configuration flags can enable.

QCOR itself handles qubit placement, so we add support for full connectivity by simply having our backend pass a fully connected coupling map to QCOR instead of a coupling map indicating a linear chain. Full connectivity reduces the
number of SWAP gates needed to execute a logical circuit on a linear chain of qubits, in turn reducing the number of CNOTs inserted by QCOR to perform SWAPs, and ultimately reducing the number of $XX(\pi/4)$ and $R_\phi(\pi/2)$ gates which together effect the swapping CNOTs.

We implement rudimentary support for parallel single-qubit using a naïve algorithm that greedily constructs a table from the XACC IR produced by the decomposition passes, with multiple $R_\phi(\pi/2)$ per row, and with each $XX(\pi/4)$ having its own row. Parallel single-qubit operations would not reduce the number of $XX(\pi/4)$ gates, but such a hardware upgrade could allow multiple $R_\phi(\pi/2)$ gates to occur across different qubits at once. Tables IV and V show examples of serial and parallel native operations, respectively, for the same input program. Clearly, we cannot compare runtime between serial and parallel configurations by counting the total number of gates; for example, Tables IV and V have the same number of $R_\phi(\pi/2)$ operations, but Table V offers a shorter runtime. Thus, we estimate the length of the critical path by counting the number of rows in the table of native operations sent to the control software, henceforth calling each row a “cycle” whenever we need to distinguish from native gate counts.

Parallel two-qubit operations stand to reduce the number of cycles spent on $XX(\pi/4)$ gates. However, given parallel two-qubit gates cannot be implemented on our three-qubit benchmarks or the testbed in its original three-qubit configuration. We leave investigating parallel two-qubit gates on the testbed as future work.

IV. Evaluation

A. System Configuration

Our targeted physical ion trap testbed and its control scheme have been modified for domain-specific computations based on global operations [20], so we cannot execute our benchmark circuits on the physical testbed itself. However, we can verify correct output of generated code by executing our operations in the simulator already included in the control software, originally used to aid in calibration. Rather than performing noisy simulations, we instead choose to estimate the performance of our compilation by simply counting the number of primitive operations, and we argue why this is reasonable in Section IV-E.

B. Optimizations Tested

We ran our benchmarks with the following three types of optimizations:

1) High level optimizations already included in QCOR as described in [17], which includes approaches such as [21] for simplifying large circuits

2) Our single-qubit optimizations explained in Section III-C

3) Our optimizations for future hardware mentioned in Section III-D

Given #1 is designed for larger, more complex circuits on a higher number of qubits, we found #1 made no difference in final native gate counts for our benchmarks. Consequently, for the remainder of this section we focus on the impact of #2 and #3. However, we note that less trivial quantum algorithms run on the testbed in the future could benefit significantly from the high-level QCOR optimizations, with [17] seeing an average 23.2% reduction in gates on benchmarks ranging from 5 to 96 qubits [22].

C. Benchmarks Chosen

To evaluate our backend, we ran the following set of benchmark QCOR programs on three qubits:

- GHZ (Greenberger-Horne-Zeilinger), which generates the state $\frac{1}{\sqrt{2}}|000\rangle + \frac{1}{\sqrt{2}}|111\rangle$
- Bernstein-Vazirani with secret string $s = 11$, similar to Listing 1
- Grover with one iteration and marked states $|01\rangle$ and $|10\rangle$ [23]
- Quantum Fourier Transform using the $\text{qft}()$ routine included in QCOR
- VQE (Variational Quantum Eigensolver) on the three-qubit Hamiltonian from [24] using the QCOR tooling for VQE

We ran each benchmark with the following three configurations of compiler and simulator:

1) Against an existing XACC backend which runs the instructions from XACC IR directly on the local Quantum++ simulator [25]

2) Against our new XACC backend configured to generate assembly, which the existing compiler compiles to a sequence of primitive operations for the control software to simulate

3) Against our new XACC backend configured to generate a sequence of primitive operations on its own as described in Sections III-B through III-D also simulated by the control software.

To validate the results of our backend, we compare the probability distribution of measurements calculated from the final state vectors of #1 through #3. Next, to evaluate our optimizations for current hardware, we compare the number of native operations produced by the existing compiler in #2 and our compiler in #3. Finally, we evaluate our optimizations for possible future hardware by comparing the native gate count produced by #2 with the native gate count produced by #3 with future hardware optimizations enabled.

D. Validation Results

To validate the results of our benchmarks, we calculated the probability distribution of measurements from the final state vector produced by the Quantum++ simulator and control system simulation of the sequence of primitive operations generated by both the existing compiler and ours. The VQE benchmark represents a special case in that instead of simply running a quantum kernel, the ansatz quantum kernel acts as part of the objective function for an optimizer on the variational parameters. As a result, in addition to comparing the probability of different measurements of the first VQE iteration
to ensure we test how our compiler handles gates on unmeasured qubits. It is enabled, and also none of them enabled. The benchmarks with only individual optimizations from Section III-C eliminates no differences in final state compared to the others; for example, with Bernstein-Vazirani, our compiler produces final state $|\frac{1}{\sqrt{2}}(110) - \frac{1}{\sqrt{2}}(111)|$ rather than $|111|$ owing to an elided final Hadamard gate on the ancilla qubit, which our program does not explicitly measure. In all cases, the differences in final quantum state do not affect the probability distribution of measurements.

### E. Gate Count Comparison

We find that as expected, the two-qubit pass described in Section III-B eliminates no $XX(\pi/4)$ gates, leaving our count of $XX(\pi/4)$ gates identical to the previous compiler. However, our one-qubit pass in Section III-C achieves an average $1.54 \times$ reduction in $R_\theta(\pi/2)$ operations, even with the $RZ$ optimizations enabled in the existing compiler. Fig. 4 shows a comparison of primitive operation counts between our compiler and the existing compiler for all our benchmarks.

To examine which optimizations contributed most to the reduction in single-qubit operations, we also compiled the benchmarks with only individual optimizations from Section III-C enabled, and also none of them enabled. The $R_\theta(\pi/2)$ count reduction numbers plotted in Fig. 3 show that individual optimizations struggle to compete with the $RZ$ optimizations in the existing compiler, with the exception of our $RX$ optimizations usually offering some individual reduction. On the GHZ benchmark, however, the $RX$ freedom alone is not as effective, with all optimizations combined performing better. Indeed, on average, each optimization provides a modest reduction in gates, but the combination readily beats any individual optimization.

The error and duration estimates in [7] for $R_\phi(\theta)$ gates on ion trap systems is defined in terms of $\theta$, not $\phi$, so with $\theta$ fixed to $\pi/2$, the number of $R_\phi(\pi/2)$ gates reasonably correlates with error and duration. Consequently, we expect

![Fig. 3. Comparison of reduction in $R_\theta(\pi/2)$ operations generated across our benchmarks by the existing compiler and by other compiler configurations (higher is better). We calculate reduction by dividing the $R_\theta(\pi/2)$ gates the existing compiler generates with $RZ$ optimizations enabled by the number of $R_\theta(\pi/2)$ gates generated by some other configuration. We include the existing compiler without optimizations for comparison.](image)

![Fig. 4. Comparison of $R_\theta(\pi/2)$ operation counts generated across our benchmarks by the existing compiler and by different configurations of our compiler (lower is better).](image)
that our benchmarks and other quantum circuits with similar complexity will experience higher overall fidelity on the testbed using our compiler. Furthermore, an $n \times$ reduction in physical $R_\phi(\pi/2)$ gates could allow $n \times$ more sequences of adjacent logical single-qubit gates with the same approximate total duration and total error as before. Thus, if combined with future optimizations for two-qubit gates, our compiler could allow running longer, more complicated programs on the testbed.

**F. Impact of Hardware Upgrades**

Our compiler does not reduce the number of $XX(\pi/4)$ gates on present hardware, but we found fully connected qubits can reduce the $XX(\pi/4)$ gate count by $2.40 \times$ on average, as seen in Fig. 3. Our Bernstein-Vazirani benchmark showed the greatest reduction at $4.00 \times$, going from 8 operations to 2 operations, owing to the removal of six CNOTs used for two SWAPs. GHZ, on the other hand, showed no benefit, as it executes CNOTs only on adjacent ions. In general, then, we see that the benefit of full connectivity is proportional to the share of of two-qubit gates between non-adjacent ions.

As shown in Fig. 6, full connectivity can also decrease the number of $R_\phi(\pi/2)$ operations since we use them to effect a CNOT using $XX(\pi/4)$ (see Fig. 2). With a $5.13 \times$ reduction on average, a fully-connected upgrade could readily beat the average $1.52 \times$ reduction seen with our compiler on current hardware. Still, some benchmarks see no benefit, such as GHZ for the reasons previously mentioned.

Although it cannot reduce $XX(\pi/4)$ cycles, Fig. 6 shows that hardware support for parallel $R_\phi(\pi/2)$ operations on different qubits could reduce $R_\phi(\pi/2)$ cycles by an average of $2.40 \times$ over the existing compiler and hardware regime, compared to $1.52 \times$ with our compiler on present hardware. While all benchmarks saw at least some parallelism, future work could likely increase this reduction by investigating more complex strategies for single-qubit unitary decomposition (Section III-C) that take parallelism into account.

**V. ADAPTION TO OTHER HARDWARE**

While our compiler was designed for a particular ion trap machine, our backend can be adapted for any hardware with a similar gateset. For example, some IonQ hardware and the QSCOUT ion trap quantum testbed operated by Sandia National Laboratories natively support $R_\phi(\theta)$ and $XX(\alpha)$ gates (Equations 2 and 7 in Section II-A) [10, 26]. On these machines, the angle $\theta$ in $R_\phi(\theta)$ is not limited to $\pi/2$ as in the GTRI testbed, so our numerical optimizer approach explained in Section III-C is not necessary, as there is a closed form solution for decomposing arbitrary single-qubit unitaries into two $R_\phi(\theta)$ gates [7]. However, our approach of removing unnecessary $RZ$ gates and commuting $RX$ gates described in the remainder of Section III-C would likely still reduce gate count.

Still, it is a common choice to restrict $\theta$ in $R_\phi(\theta)$ to limit the set of calibrations. For example, a recent ion trap quantum computer developed by Honeywell supports $R\alpha(\theta)$ with $\theta$ constrained to $\pi$ or $\pi/2$, much like the $\theta = \pi/2$ restriction on the GTRI testbed [15]. The numerical optimization strategy described in Section III-C could be adapted by running the up-to-Z optimizer on all seven combinations of zero through two $R_\phi(\theta)$ rotations with each individual angle $\theta \in \{\pi, \pi/2\}$, all followed by a Z-rotation. The machine has the entangling gate $ZZ(\alpha) = \exp(-i\alpha(Z \otimes Z))$, analogous to the $XX(\alpha)$ gate. $ZZ(\alpha)$ commutes with $RZ(\theta)$, so our approach for commuting $RX(\theta)$ around $XX(\alpha)$ gates could be adapted to commute $RZ(\theta)$ gates around $ZZ(\alpha)$ gates instead. Despite these similarities, a compiler for the Honeywell machine would need to understand the multiple transport operations supported; our backend does not consider transport operations.
since the testbed control software infers them automatically.

The current domain-specific configuration of the GTRI testbed could also be supported, as well as other hardware with global operations in general, but this would require adding new instructions to XACC IR targeting all qubits. Moreover, our IR transformations described in Sections [III-B] and [III-C] will not be useful on hardware with only global operations, since one would not typically program them using a typical quantum circuit. However, backends for any hardware whose native operations support typical quantum circuits benefit from the existing high-level circuit optimizations already present in QCOR [17].

VI. RELATED WORK

Martinez et al. [27] discuss techniques for compiling arbitrary multi-qubit gates to ion-trap architectures supporting collective rotations of the whole qubit register about any axis (C(θ, φ) gate), single qubit rotations around the Z axis (Zr(θ) gate), and MS gates. They show how any multi-qubit gate can be decomposed into a sequence of single-qubit local unitaries and MS gates. Our work employs this decomposition concretely in the XACC backend restricted to the single-qubit and two-qubit case. Maslov [7] proposes a generic architecture for optimizing compilers targeting ion-trap quantum computers. QCOR does not match the architecture exactly, but instead provides a framework for describing and applying relevant optimizations. Our implementation does not support the peep-hole optimizations proposed in the paper.

QFAST [28] innovates in circuit synthesis by presenting a novel representation of circuits allowing them to use numerical optimization to replace expensive searches over circuit structures. They use a bottom-up approach which stems from a special encoding that enables them to find better building blocks for circuit synthesis. QGo [29] is a quantum circuit optimization framework that aims to be scalable (optimizing circuits containing 60+ qubits in a reasonable amount of time). It is able to achieve this performance by employing a partitioning scheme in which the circuit is broken down into smaller components, independently optimized, and then composed together.

Lu et al. [30] discuss a scalable scheme for implementing a global multi-qubit entangling gate which can potentially lead to exponential speedups as compared to a circuit decomposition involving single- and two-qubit entangling gates. The GTRI testbed is currently configured for specific multi-qubit global entangling operations [20], but we have not considered them in this work.

Gokhale et al. [25] have implemented a compiler that exploits pulse-level optimizations without resorting to Quantum Optimal Control (QOC) approaches, thereby bypassing the experimental barrier of measuring and maintaining the Hamiltonian of a quantum system. They are able to achieve about 1.6× error reductions and 2× speedups on near-time quantum algorithms run using the OpenPulse interface on IBM’s quantum computers. Our work does not currently employ these optimizations, which we leave as future work.

Pino et al. [15] demonstrate a quantum computer also based on an ion trap, but contrary to our assumptions in this work about future GTRI testbed upgrades (i.e., per-ion beams), their design transports ions through shared beams to perform gates. Ion swapping operations help provide full qubit connectivity, and multiple beams provide support for parallel operations. The authors briefly mention a compiler that performs qubit mapping such that it minimizes the number of native transport operations, which may include linear ion movement, swapping ion order, and splitting or combining ion crystals, but they do not go into detail on the compiler design. Since our assumptions about future hardware upgrades to the GTRI testbed are only guesses, future work should consider minimizing the number of these transport operations in addition to native gate count, our primary consideration in this work.

The TILT (Trapped-Ion Linear Tape) architecture for ion trap hardware proposed by Wu et al. consists of a stationary set of lasers targeting a subset of the ions in a single ion chain [31]. Compared to the previously proposed QCCD (Quantum Charge-Coupled Device) architecture [32], TILT offers simpler hardware and avoids expensive shuttling operations. The authors detail LinQ, their compiler framework designed for TILT hardware, which employs two heuristic-based algorithms: one for inserting SWAP gates, and another for transport operations. The first algorithm facilitates two-qubit gates between qubits not within the “execution zone” of the lasers, and the second attempts to avoid unnecessary tape movement, which may introduce qubit noise. Their discussion of LinQ further emphasizes the importance of future work on our backend minimizing the number of transport operations. Additionally, it is not mentioned if their compiler employs the optimizations employed in Section [III-C]. Future work should investigate how to apply these optimizations to TILT systems.

VII. CONCLUSION

This work details efforts to add a new ion trap backend to the XACC quantum toolchain as well as a demonstration of multi-level optimization strategies to provide algorithmic optimizations at the language, IR, and backend levels. As a demonstration of this strategy, our implementation allows heterogeneous quantum-C++ programs to be compiled and optimized to use fewer physical operations, along with a basic simulation functionality using the testbed’s existing development tools.

Future work in this space would look to extend this programming environment to support further optimizations as well as testing with the quantum hardware instead of the simulated environment. We would first consider optimizations such as parallel two-qubit gates, non-$R_{\phi}(\pi/2)$ operations, and multi-qubit optimizations to improve the fidelity of generated quantum circuits.

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