A Non-Isolated High Step-Up DC-DC Converter Using Voltage Lift Technique: Analysis, Design, and Implementation

ALIREZA RAJABI1, AMIRHOSSEIN RAJAEI1, (Member, IEEE), VAHID MORADZADEH TEHRANI1, PAYMAN DEHGHANIAN2, (Senior Member, IEEE), JOSEP M. GUERRERO3, (Fellow, IEEE), AND BASEEM KHAN4, (Senior Member, IEEE)

1Department of Electrical and Electronics Engineering, Shiraz University of Technology, Shiraz, Fars 71557-13876, Iran
2Department of Electrical and Computer Engineering, The George Washington University, Washington, DC 20052, USA
3Villum Center for Research on Microgrids (CROM), AAU Energy, Aalborg University, 9220 Aalborg, Denmark
4Department of Electrical and Computer Engineering, Hawassa University, Awassa 05, Ethiopia

Corresponding author: Baseem Khan (baseem.khan04@gmail.com)

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ABSTRACT This paper presents a new structure for non-isolated and non-inverting DC-DC converters with high voltage gain harnessing the fundamentals of the voltage lift technique. The proposed topology is a suitable structure for low voltage applications. The operation principles, the steady-state relations, and different switching strategies to further improve the voltage gain performance of the proposed converter are described. A hybrid utilization of complementary switching approach and simultaneous switching of two switches is proposed to achieve the highest voltage gain in different duty cycles. Furthermore, a theoretical analysis of power losses is provided. The suggested DC-DC converter architecture features high voltage gain, high efficiency, and low stress on semiconductor devices. In order to demonstrate these advantages, the structure is compared with some recently-presented high step-up converters in terms of efficiency, voltage gain, and voltage stress. Moreover, A 200W laboratory prototype is developed with experiments carried out to validate the given theories and feasibility of the proposed converter topology.

INDEX TERMS High step-up DC-DC converter, high efficiency, voltage-lift technique, critical inductance.

I. INTRODUCTION

High step-up DC-DC converters have increasingly attracted attention in recent years, primarily due to their several advantages, making them suitable alternatives to be employed in many critical applications of power electronic converters, such as renewable energy interface systems, DC distribution networks, energy storage systems, electric vehicles, and uninterruptible power supplies (UPS) [1]–[3]. Besides high voltage gain and high efficiency, the boost converters feature a low ripple input current, especially in photovoltaic (PV) and fuel cell (FC) applications, which in turn, results in achieving maximum power point tracking (MPPT) in PVs, prolong lifetime of the FCs [4], and improved dynamic performance of the system [5], [6].

Isolated-type DC-DC converters and coupled inductor type converters utilizing high-frequency transformers can provide high voltage gain since they can accommodate any desired transformer turns ratio [7]. However, besides the increasing volume and cost because of using magnetic elements, one drawback is the voltage spikes across the semiconductor devices due to the leakage inductance. This issue mostly requires employing snubber circuits [8], which increases the cost, complexity, and power loss [9]. Compared to the isolated structures, non-isolated DC-DC converters offer simplicity, compact size, and low cost [10]. However, the classical non-isolated boost converters cannot achieve a high voltage gain at extremely-high duty cycles due to the parasitic elements and the related losses [11]. Therefore, different architectures and techniques were introduced in the literature in response [12], such as switched-inductor (SI) [13] and switched-capacitor (SC) cells, switched-capacitor-inductor networks [14], coupled [15] and non-coupled inductors [16].
Non-coupled inductor boost converters include the cascaded converters [17] and voltage multipliers [18]. While this type of converters can provide a high voltage gain, their efficiency is limited due to the excessive number of elements. In the topologies based on the coupled inductors, energy flows through both electrical and magnetic paths, thereby generally improves the converter’s performance. Nevertheless, similar to isolated structures, the leakage inductance of the coupled inductors can produce voltage spikes. Converters based on the SC technique [19]–[21] comprise switches and capacitors with minimum inductors used. Although a high voltage gain is achieved by a combination of these elements, considerable complexity, capacitors current stress issue, and poor energy efficiency poses a limitation to their wide applications. Therefore, these structures are typically used in low power applications, such as energy harvesting and in-chip design of integrated circuits (IC) [21]. The voltage lift (VL) technique is another approach to increase the performance and the voltage gain simultaneously [22]. The VL circuit can increase the output voltage by adding a charge path using diodes and capacitors. Generally, the VL technique can improve the power density, efficiency, and output voltage ripple of the classical boost converters. Additionally, it results in cost-effective and straightforward designs. Several DC-DC converters based on this technique are researched in [23], [24].

According to Fig. 1, the fuel cell requires a high step-up dc-dc converter to interface it to dc-link of the inverter [2]. In this paper, a new architecture that brings together improved voltage gain, enhanced efficiency, and reduced voltage stresses is proposed for fuel cell-powered electric vehicles (EVs), validated, and compared with the state-of-the-art models. This paper is organized as follows: The operation principles, key waveforms, and the main relations of steady-state operation in continuous conduction mode (CCM) and an analysis of various switching methods are provided in Section II. Driven by the performed analyses, passive elements design, calculating voltage and current stresses of semiconductor devices, and efficiency analysis are investigated in Section III. The proposed architecture is compared with the state-of-the-art converter topologies in Section IV. In section V, the accuracy of the theoretical concepts is validated by experiments on a 200W laboratory prototype.

**II. CONFIGURATION, OPERATION PRINCIPLES, AND STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER**

The operation of the VL technique is based on energy transmission between inductors and capacitors, which are the storage elements of the converter. The schematic of the proposed converter is illustrated in Fig. 2, which includes two switches ($S_1$ and $S_2$), two non-coupled inductors ($L_1$ and $L_2$), three capacitors ($C_1$, $C_2$, and $C_o$), and three diodes ($D_1$, $D_2$, and $D_o$). In the following, operation modes, steady-state relations, and different switching states are analyzed.

![FIGURE 1. Application of the proposed converter in fuel cell vehicles.](image)

![FIGURE 2. (a) Proposed converter with common drain switches; (b) with common source switches; (c) current paths for Mode I ($S_1$: ON & $S_2$: OFF); (d) current paths for Mode II ($S_1$: OFF & $S_2$: ON).](image)
A. OPERATION PRINCIPLES AND STEADY-STATE ANALYSIS

In order to simplify the analyses, several hypotheses are considered as follows:

- All elements are considered ideal.
- The converter operates in CCM and steady-state conditions.
- Capacitors are large enough to assume that the corresponding voltages are constant.
- A complementary switching is considered as the switching strategy. Other possible strategies are discussed in section II-B.

The CCM operation of the converter consists of two modes, as discussed in the following.

Mode I (S₁: ON & S₂: OFF): This mode lasts for t\text{on} (t\text{on} = DT \text{s}), where T\text{s} is the switching period, and D is the duty cycle of S₁. During this mode, D₁ and D₂ are reverse-biased, and D₀ is forward-biased. L₁ is connected to the input source V\text{in}, and therefore, the inductor current (i\text{l1}) increases. L₂, C₁, and C₂ are connected in series along with the source to the load; as a result, their stored energy gradually decreases.

The current paths of this mode are shown in Fig. 2(c), and the waveforms are shown in Fig. 3. The relations for the inductor voltages (v\text{l1} and v\text{l2}) and the capacitor currents (i\text{c1}, i\text{c2}, and i\text{c0}) during this interval are as follows:

\[ v_{\text{l1}} = V_{\text{in}} \quad (1) \]
\[ v_{\text{l2}} = V_{\text{in}} + V_{\text{C1}} + V_{\text{C2}} - V_o \quad (2) \]
\[ i_{\text{c1}} = i_{\text{c2}} = i_{\text{l2}} \quad (3) \]
\[ i_{\text{c0}} = i_{\text{l2}} - I_o \quad (4) \]

where I_o = V_{C0}/R is the load current.

Mode II (S₁: OFF & S₂: ON): In this time interval, which is equal to t\text{off} (t\text{off} = (1-D)T \text{s}), D₁ and D₂ are forward-biased, D₀ is reversed-biased, and the stored energy in L₁ is delivered to C₁, C₂, and L₂. Therefore, the stored energy of C₁, C₂, and L₂ increases. Meanwhile, C₀ discharge current provides the load current. The current paths of this mode are shown in Fig. 2 (d), and the waveforms are shown in Fig. 3. The relations for the inductors voltages and the capacitors currents during this mode of operation are as follows:

\[ v_{\text{l1}} = V_{\text{in}} - V_{\text{C1}} \quad (5) \]
\[ v_{\text{l2}} = V_{\text{C1}} \quad (6) \]
\[ i_{\text{c1}} = i_{\text{l1}} - i_{\text{l2}} - i_{\text{c2}} \quad (7) \]
\[ i_{\text{c2}} = i_{\text{l1}} - i_{\text{l2}} - i_{\text{c1}} \quad (8) \]
\[ i_{\text{c0}} = -I_o \quad (9) \]

In order to find the average values of the capacitor voltages, the inductor voltage-second balance is applied to the derived relations of the two operation modes, which yields:

\[ V_{\text{C1}} = \frac{1}{1-D} V_{\text{in}} \quad (10) \]
\[ V_{\text{C2}} = \frac{D}{1-D} V_{\text{in}} \quad (11) \]

FIGURE 3. Main converter waveforms in CCM using the complementary switching strategy.

\[ V_o = \frac{1 + D}{D(1-D)} V_{\text{in}} \quad (12) \]

The average value of the input current (I\text{in}) and L₁ current (I\text{l1}) can be calculated considering the input and output power balance.

\[ \frac{V_{\text{in}} I_{\text{in}}}{R} \rightarrow I_{\text{in}} = \frac{V_o^2}{RV_{\text{in}}} \quad (13) \]

In steady-state condition, the average value of capacitor C₂ current is zero, therefore:

\[ I_{\text{l1}} = I_{\text{in}} = \frac{V_o^2}{RV_{\text{in}}} \quad (14) \]

The average value of L₂ current (I\text{l2}) is calculated based on the current passes through D₀.

\[ \left\{ \begin{array}{l}
I_{\text{Do}} = DI_{\text{l2}} \\
I_{\text{Do}} = \frac{V_o}{R} \rightarrow I_{\text{l2}} = \frac{V_o}{DR} \quad (15)
\end{array} \right. \]

Using (12), the converter voltage gain for CCM operation (M) is obtained as (16).

\[ M = \frac{V_o}{V_{\text{in}}} = \frac{1 + D}{D(1-D)} \quad (16) \]

B. INVESTIGATION OF DIFFERENT SWITCHING STRATEGIES

Different features of DC-DC converters, such as voltage gain, efficiency, and voltage and current stresses of the elements, are dependent on the switching strategy. In the following, four possible switching strategies of the proposed converter, as shown in Fig. 4, are elaborated in detail.

1) COMPLEMENTARY SWITCHING FIG. 4(a)

Operation principles and relations were described. The converter voltage gain is calculated by (16).
The converter contains three operating modes:

**Mode III (S1 & S2: ON):** During this mode, which lasts for $t_{on}$ ($t_{on} = DT$) seconds, all diodes are reverse-biased, and $L_1$ and $L_2$ are charged through $V_{in}$ and $C_1$, respectively. $C_o$ feeds the load and discharges. The current paths and waveforms during this mode are shown in Fig. 5(a) and Fig. 6, respectively.

**Mode IV (S1 & S2: OFF and D2: OFF):** This mode lasts for $D_2T$, in which diodes $D_1$ and $D_o$ are forward-biased, and $D_2$ is reverse-biased. The stored energy in $L_1$ is delivered to $C_1$, resulting in an increase in $V_{C1}$. Also, $C_2$ and $L_2$ are connected to the load and are discharged, while $L_2$ provides the charge current of $C_o$. The current paths and waveforms during this mode are shown in Fig. 5(b) and Fig. 6, respectively.

**Mode V (S1 & S2: OFF and D2: ON):** At the beginning of mode IV, $V_{in} + V_{C2}$ is greater than $V_{C1}$, hence $D_2$ is reverse-biased. However, $C_1$ is being charged, and its voltage increases, while $C_2$ is discharging, and its voltage decreases. Whenever $V_{C1} = V_{in} + V_{C2}$, diode $D_2$ turns ON and starts conducting. This mode lasts for $(1 - D - D_2)T$. The current paths and waveforms during this mode are shown in Fig. 5(c) and Fig. 6, respectively.

The average values of the capacitor voltages, inductor currents, and the voltage gain for this switching approach are obtained using a similar procedure as described before, which yields the following relations:

\[
V_{C1} = \frac{1}{1-D} V_{in} \tag{17}
\]

\[
V_{C2} = \frac{D}{1-D} V_{in} \tag{18}
\]

\[
V_o = \frac{V_{in}}{(1-D)^2} \rightarrow M = \frac{1}{(1-D)^2} \tag{19}
\]

\[
I_{L2} = \frac{V_o}{(1-D)R} \tag{20}
\]

The relation for $I_{L1}$ is the same for all switching methods and is calculated by(14).
3) PHASE-SHIFTED WITH $D < 0.5$ (FIG. 4(c))
In this switching strategy, the command signal of $S_2$ is shifted for $T_s/2$ seconds, and both commands have a similar duty cycle equals to $D$, where $D$ is lower than 0.5 (Fig. 4(c)). Therefore, the converter includes three modes of operation: mode I, mode II, and mode III. The main equations of the converter using this switching method are as follows:

- \[ V_{C1} = \frac{V_{in}}{D} \] (21)
- \[ V_{C2} = \frac{D V_{in}}{(1 - D)} \] (22)
- \[ V_o = \frac{2 - D}{(1 - D)^2} V_{in} \rightarrow M = \frac{2 - D}{(1 - D)^2} \] (23)
- \[ I_{L2} = \frac{V_o}{(1 - D)R} \] (24)

4) PHASE-SHIFTED WITH $D > 0.5$ (FIG. 4(d))
This approach is the same as strategy 3, with a duty cycle higher than 0.5. The converter includes three modes of operation: mode I, mode II, and mode III. The main equations of the converter using this switching method are as follows:

- \[ V_{C1} = \frac{V_{in}}{D} \] (25)
- \[ V_{C2} = \frac{D V_{in}}{(1 - D)} \] (26)
- \[ V_o = \frac{2 - D}{(1 - D)^2} V_{in} \rightarrow M = \frac{2 - D}{(1 - D)^2} \] (27)
- \[ I_{L2} = \frac{V_o}{(1 - D)R} \] (28)

Using (16), (19), (23), and (27), the voltage gain for different switching strategies are plotted in Fig. 7. As illustrated in Fig. 7, the complementary switching approach provides the highest gain for $D < 0.62$, while the voltage gain with simultaneous switching for $D > 0.62$ is higher than other switching methods.

**FIGURE 7.** Comparison of the different switching methods’ voltage gain vs. duty cycle.

### III. DESIGN CONSIDERATIONS OF THE CONVERTER ELEMENTS AND EFFICIENCY ANALYSIS
Proper operation of a converter is driven by the appropriate design of its components. Some important considerations regarding the passive components and the semiconductor devices must be taken into account. A procedure to design the elements of the proposed converter architecture in CCM operation are presented here and then validated by the experimental results in Section V. The switching strategy is assumed to be the complementary switching.

#### A. INDUCTOR DESIGN
Critical inductance is the minimum value of the inductance required to guarantee the CCM operation. By applying the current-balance law to $C_1$ and $C_2$ in CCM, and considering $I_{LV1} + I_{LV2} = 0$, the critical inductances of $L_1$ and $L_2$ are obtained as follows:

- \[ L_{crit1} = \frac{RD^4(1 - D)}{2f_s(1 + D)} \] (29)
- \[ L_{crit2} = \frac{RD^4(1 - D)}{f_s} \] (30)

where $L_{crit1}$, $L_{crit2}$, and $f_s$ are the critical inductances of $L_1$ and $L_2$, and the switching frequency, respectively.

Inductor’s inductance value is determined according to the desired current ripple value, which depends on the inductor voltage ($V_L$), current ripple ($\Delta i_L$), switching frequency ($f_s$), and duty cycle ($D$). Considering (1), (5), and (10), the inductances of $L_1$ and $L_2$ are obtained as follows:

- \[ L_1 = \frac{DV_i}{f_s \Delta i_{L1}} \] (31)
- \[ L_2 = \frac{V_i}{f_s \Delta i_{L2}} \] (32)

#### B. CALCULATION OF THE CAPACITANCE
With the capacitors considered ideal, the capacitor’s voltage ripple ($\Delta V_C$) can be calculated. The size of the capacitor depends on its current ($i_C$), desired voltage ripple ($\Delta V_C$), switching frequency ($f_s$), and duty cycle ($D$). Therefore, according to (1) and (8), the capacitance values of $C_1$, $C_2$, and $C_0$ are obtained as follows:

- \[ C_o = \frac{(1 - D)V_{Co}}{Rf_s \Delta V_{Co}} \] (33)
- \[ C_1 = \frac{D}{f_s \Delta V_C} \left( i_{Co} + \frac{V_{Co}}{R} \right) \] (34)
- \[ C_2 = \frac{D}{f_s \Delta V_C} \left( i_{Co} + \frac{V_{Co}}{R} \right) \] (35)

#### C. VOLTAGE STRESS ACROSS THE SWITCHES AND DIODES
Voltage stress is calculated by considering the OFF state of the switches and diodes. The voltage stress across $S_1$ and $S_2$ ($V_{DSS1}$ and $V_{DSS2}$) are presented in (36) and (37), respectively. The voltage stresses across $D_1$, $D_2$, and $D_0$ are calculated using (38), (39), and (40), respectively.

- \[ V_{DSS1} = \frac{V_{in}}{1 - D} \] (36)
\[ V_{DS(S2)} = \frac{V_{in}}{D(1 - D)} \]  
\[ V_{D1} = V_{D2} = \frac{V_{in}}{1 - D} \]  
\[ V_{D2} = \frac{V_{in}}{1 - D} \]  
\[ V_{Do} = V_o \]  

**D. CURRENT STRESS OF THE SEMICONDUCTOR DEVICES**

Similarly, the current stress of \( S_1 \) and \( S_2 \) can be found by (41) and (42), respectively.

\[ I_{CS(S1)} = I_{L1(PK)} + I_{L2(PK)} \]  
\[ I_{CS(S2)} = I_{L2(PK)} \]  

where \( I_{L1(PK)} \) and \( I_{L2(PK)} \) are the peak values of \( L_1 \) and \( L_2 \) currents, respectively. The maximum current stress of \( D_1, D_2, \) and \( D_o (I_{CS(D1)}, I_{CS(D2)}, \) and \( I_{CS(Do)} \)) are:

\[ I_{CS(D1)} = \frac{(1 + D)V_o}{D(1 - D)R} \]  
\[ I_{CS(D2)} = iC_2 \]  
\[ I_{CS(Do)} = I_{L2(PK)} \]  

**E. CONVERTER LOSSES AND EFFICIENCY**

The converter losses generally include two parts: conduction losses and switching losses. The non-idealities considered for conduction losses are the conduction resistance of the inductors \( r_L \), switch on-state resistance \( r_S \), and diodes forward voltage \( V_f \). Therefore conduction losses include: inductor, switch, and diode conduction losses \( (P_{COND(L)}, P_{COND(SW)}, \) and \( P_{COND(D)} \), respectively). Using the values calculated in the previous session, theoretical values of the converter losses are calculated in the following:

\[ P_{COND(L)} = R_L \left( \frac{V_o}{V_{in}} \right)^2 + R_L \left( \frac{V_o}{DR} \right)^2 \]  
\[ P_{COND(SW)} = R_{on}[D(I_{L1} + I_{L2})]^2 + R_{on}[(1 - D)I_{L2}]^2 \]  
\[ P_{COND(D)} = V_f (I_{L1} + D I_{L2}) \]  

The diodes’ reverse recovery loss \( P_{rr} \) is also estimated by (50), where \( Q_{rr(D)} \) is the diodes’ recovered charge.

\[ P_{rr} = f_{r}(Q_{rr(D1)}V_{D1} + Q_{rr(D2)}V_{D2} + Q_{rr(Do)}V_{Do}) \]  

The theoretically calculated converter’s power losses and efficiency are shown in Fig. 8. The value of the parasitic elements and converter specifications used for efficiency calculations are the same as the prototype specifications used for model validation in section V.

**FIGURE 8.** Theoretically calculated power losses and efficiency of the proposed converter: (a) power losses; (b) efficiency.

**IV. COMPARISONS WITH OTHER CONVERTER TOPOLOGIES**

A comparison between the proposed converter and some other non-isolated structures are represented in Fig. 9 and Fig. 10. Several performance criteria are considered for this comparison, including the voltage gain, number of elements, and voltage and current stresses across the semiconductor devices. As shown in Fig. 9(a), the voltage gain of the proposed converter is higher than that achieved in [24], [26], and [27]. Compared to the topologies introduced in [13] and [16], the presented structure reveals a higher voltage gain for \( D < 0.58 \), while having a better voltage gain for \( D < 0.5 \) than the solution presented in [28]. It should be noted that, although the solution in [16] offers a higher voltage gain at higher duty cycles, it consists of three inductors in the structure, which limits the efficiency and increase the cost and volume. The variation of the normalized voltage stress of the switches and diodes versus the voltage gain are presented in Fig. 9(b) and (c), respectively, demonstrating that the proposed structure features an acceptable switch and
diode voltage stresses. Moreover, Fig. 10 shows the proposed converter’s efficiency for different output powers compared to other topologies, which validates its promising efficiency performance.

V. EXPERIMENTAL VERIFICATIONS

In order to validate the given theories and validate the feasibility of the proposed converter, a 200W laboratory prototype (Fig. 11) is developed using the parameters represented in TABLE 2. and TABLE 3. For the given values of $V_{in} = 24V$, $R = 100\Omega$, and $D = 0.5$, the critical inductance values for $L_1$ and $L_2$ are determined as 7$\mu$H and 20$\mu$H, respectively. As the critical values are far lower than the actual values of $L_1$ and $L_2$, CCM operation is guaranteed.

Furthermore, to generate the required output voltage of 144V using the complementary switching strategy, the duty cycle should be $D = 0.5$ according to (16). But here, the duty cycle of $S_1$ is adjusted to $D = 0.52$ to compensate for the non-ideal conditions as described in TABLE 3. In conclusion, the experimental results are shown in Fig. 12.
seen, the average voltages across the capacitors $C_1$ and $C_2$ are $V_{C1} = 48V$ and $V_{C2} = 24V$, which confirms (10) and (11), respectively. Furthermore, the average voltage across $C_0$ is observed at 144V, which is in accordance with that presented in (16). The voltage across the diodes $D_1$, $D_2$, and $D_0$ are presented in Fig. 12(f), (g), and (h), respectively, which confirms (38)-(40). The minor differences between the theoretical and experimental results are due to the effect of parasitic elements. Moreover, according to Fig. 12(i) and (j), the voltage stresses of the switches are 48V and 96V, which confirms (36) and (37), respectively. Also, the current stress of the switches follows (41) and (42). Furthermore, the experimental efficiency results of the proposed converter are presented in Fig. 13.

### VI. CONCLUSION

In the current study, a high voltage gain converter based on the voltage-lift technique was proposed and analyzed in the CCM operating condition. The voltage and current relations were extracted for different switching strategies. It was shown that, the complementary switching approach provides the highest gain for $D < 0.62$, while the voltage gain with simultaneous switching for $D > 0.62$ shows the highest value. Therefore the hybrid utilization of these strategies were proposed to achieve the highest voltage gain for different duty ratio. Furthermore, the design considerations of the proposed converter were investigated, including passive elements design, calculating the critical inductances, and assessing the voltage and current stresses. Compared to the similar state-of-the-art topologies, the proposed structure features several advantages, such as higher voltage gain and lower electrical stresses on the semiconductor devices. The highest measured efficiency was achieved at 200W output power and the converter’s performance was verified by experiments on a laboratory prototype. The proposed topology represented several advantages as mentioned in the following: high voltage gain, low voltage

| TABLE 2. Hardware specifications. |
|----------------------------------|
| **Component** | **Symbol** | **Value** | **Component** | **Symbol** | **Value** |
| Output power | $P_{out}$ | 200W | Input inductor | $L_1$ | 100μH |
| Load | $R_L$ | 100Ω | Second inductor | $L_2$ | 300μH |
| Output voltage | $V_{out}$ | 144V | Capacitor | $C_1$ | 470μF |
| Input voltage | $V_{in}$ | 24V | Capacitor | $C_2$ | 1000μF |
| Switching frequency | $f_s$ | 50kHz | Output capacitor | $C_o$ | 100μF |

| TABLE 3. Values of the parasitic elements in the converter prototype. |
|----------------------------------|
| **Symbol** | **Value** | **Symbol** | **Value** |
| $r_{L1}$ | 5mΩ | $r_{L2}$ | 7mΩ |
| $r_{C1}$ | 20mΩ | $r_{C2}$ | 35mΩ |
| $v_{D1}$, $v_{D2}$, and $v_{D0}$ | 1.2V | $r_{D1}$, $r_{D2}$, and $r_{D0}$ | 10mΩ |
stress on other elements, high efficiency with lower number of elements. However the topology has some constraints which the main is high voltage stress on $sw_2$. Regarding these advantages and disadvantages, the proposed topology is a suitable structure for low voltage low power applications. According to [29], it has proposed a high step-up scalable voltage multiple cell based DC/DC converters, so one of the suggestions about our topology is construct n–stage boost converter. With this technique we can achieve high level output voltage with minimum elements.

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AMIRHOSSEIN RAJAEI (Member, IEEE) received the B.Sc. degree in electrical engineering from Shiraz University, Shiraz, Iran, in 2006, and the M.Sc. and Ph.D. degrees in electrical engineering from Tarbiat Modares University, Tehran, Iran, in 2009 and 2013, respectively. Since 2013, he has been an Assistant Professor with the Shiraz University of Technology, Shiraz, where he is currently an Associate Professor. He has conducted several projects in the field of power electronics and published more than 40 papers. His research interests include power converter modeling and design, power electronic applications in renewable energies and smart grids, and voltage multiplier circuits.

VAHID MORADZADEH TEHRANI was born in Shiraz, Iran, in September 1997. He received the B.Sc. degree in electrical engineering from the Firouzabad Institute of Higher Education, Firuzabad, Iran, in 2019. He is currently pursuing the M.Sc. degree in electrical engineering with the Shiraz University of Technology, Shiraz. His research interests include modeling and design of DC/DC converters, DC/AC inverters, and renewable energy power conversion.

PAYMAN DEHGHANIAN (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 2009, the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, in 2011, and the Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2017. He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, The George Washington University, Washington, DC, USA. His research interests include power systems reliability and resilience, data-informed decision-making for maintenance and asset management in electrical systems, and smart electricity grid applications. He was the recipient of the 2014 and 2015 IEEE Region 5 Outstanding Professional Achievement Awards, the 2015 IEEE-HKN Outstanding Young Professional Award, and the 2021 Early Career Award from the Washington Academy of Sciences.

JOSEP M. GUERRERO (Fellow, IEEE) received the B.Sc. degree in telecommunications engineering, the M.Sc. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000, and 2003, respectively. He is currently pursuing the M.Sc. degree in psychobiology and cognitive neuroscience with the Autonomous University of Barcelona. Since 2011, he has been a Full Professor with the AAU Energy, Aalborg University, Denmark, where he is responsible for the Microgrid Research Program. In 2019, he became a Villum Investigator by The Villum Fonden, which supports the Center for Research on Microgrids (CROM), Aalborg University, while being the Founder and the Director of the same center (www.crom.et.aau.dk). He has published more than 800 journal articles in the fields of microgrids and renewable energy systems, which are cited more than 70,000 times. His research interests include different microgrid frameworks in applications, such as microgrid clusters, the IoT-based and digital twin, maritime microgrids for electrical ships, vessels, ferries, and seaports, and space microgrids applied to nanosatellites and closed ecological systems.

For eight consecutive years, from 2014 to 2021, he was awarded by Clarivate Analytics (former Thomson Reuters) as Highly Cited Researcher with 50 highly cited papers. In 2021, he received the IEEE Bimal Bose Award for Industrial Electronics Applications in Energy Systems, for his pioneering contributions to renewable energy-based microgrids. He is an Associate Editor for a number of IEEE TRANSACTIONS.

BASEEM KHAN (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from Rajiv Gandhi Technological University, Bhopal, India, in 2008, and the M.Tech. and D.Phil. degrees in electrical engineering from the Maulana Azad National Institute of Technology, Bhopal, in 2010 and 2014, respectively. He is currently working as a Faculty Member of Hawassa University, Ethiopia. He has published more than 100 research articles in well-reputed research journals, including IEEE TRANSACTIONS, IEEE ACCESS, Computers and Electrical Engineering (Elsevier), IET GTD, IET RPG, and IET Power Electronics. Further, he has published, authored, and edited books with Wiley, CRC Press, and Elsevier. His research interests include power systems restructuring, power systems planning, smart grid technologies, meta-heuristic optimization techniques, reliability analysis of renewable energy systems, power quality analysis, and renewable energy integration.