Switched-capacitor-based boost multilevel inverter topology with higher voltage gain

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Abstract: This study proposes a new switched-capacitor-based multilevel inverter topology with a single dc voltage source. The proposed topology finds its suitability for low voltage applications with single or higher voltage gain. Seven-level (7L) output voltage is achieved across the load with triple-voltage gain employing 2 capacitors and 16 switches. Self-voltage balancing of capacitor voltages, parallel operation of capacitors during discharging mode, reduced voltage stress and bipolar output voltage generation without using backend H-bridge are the major features of the proposed topology. Furthermore, a generalised structure of the proposed topology has also been discussed here. A comparison with other similar topologies with single-source 7L configuration has been carried out to show the advantages of the proposed topology with reduced switch count. Experimental results have been provided to verify the performance of the proposed topology with different operating conditions.

1 Introduction

In the last few decades, the multilevel inverter (MLI) has been one of the promising and applied power converters for different applications for medium- and high-voltage/power ratings. The applications include industrial drives, solar-based applications, high-voltage direct current transmission, flexible AC transmission systems, active power filters, electric vehicles etc. All these applications adopt MLI due to its superior performance such as the reduced amount of total harmonic distortion resulting in the lower size of the filter, reduced voltage stress, reduced dv/dt, improved efficiency due to lower switching frequency etc. The three traditional topologies for MLIs have been diode clamped MLI (DCMLI), flying capacitor MLI (FCMLI), and cascade H-bridge MLI (CHBMLI). However, for a higher number of levels, these topologies suffer from a higher number of components i.e. number of diodes and switches for DCMLI, number of capacitors for FCMLI and isolated dc voltage sources for CHBMLI. Additionally, the capacitor voltage balancing has been another issue with DCMLI and FCMLI. To solve these issues, several topologies have been proposed [1–4].

The traditional topologies lack the voltage boosting ability. For renewable energy applications, the low voltage generated by the renewable sources needs to be boosted to make them useful for high-voltage applications. Furthermore, for grid-connected applications, the output voltage of the converter associated with the renewable energy should match the required level [5, 6]. Different topologies have been suggested with boosting ability, in which the peak of the output voltage has a multiplying factor more than one to the input dc voltage source. The boosting feature has been achieved by using the capacitors in conjunction with the dc voltage sources. One such topology with multilevel output has been presented in [7], in which the value of gain has been two between the peak output voltage and input voltage. However, it uses two capacitors for the five-level output. Two topologies for five levels have been suggested in [8, 9]. Both topologies use two capacitors for nine-level generation, with voltage gain fixed to two. In [10], ten-level (10L) topology has been proposed with triple-voltage boosting. However, this topology uses 16 switches. Another 7L inverter has been proposed in [11], which comprises three capacitors of two different voltage ratings. Furthermore, the voltage gain has been 1.5. Another topology with a voltage gain of 1.5 has been proposed in [12].

In [13], a new switched-capacitor-based inverter topology has been recommended with boosting ability. However, it requires back-end H-bridge for the negative polarity generation across the load. This increases the overall voltage stress of the topology. The improved topology of [13] has been presented in [14], which removes the H-bridge, leads to the reduction of the voltage stress. However, the number of switch counts increases. To reduce the number of switches along with a higher voltage gain factor, a new boost MLI with self-voltage balancing has been proposed in this paper. The merits of the proposed 7L inverter are given as follows:

(i) Need a single dc voltage source with two capacitors of the same voltage rating.
(ii) The maximum blocking voltage on the individual switch is 2Vin where Vin is the dc input voltage.
(iii) The ratio of input and output voltage is 1:3 (Vin/Vout).
(iv) It does not require any additional capacitor balancing circuits.
(v) For higher voltage gain and levels, the extension of proposed 7L topology is possible without cascade connection.

2 Description of the proposed boost topology

2.1 Proposed topology

The assembly of the proposed boost MLI topology has been depicted in Fig. 1. It consists of 12 unidirectional power semiconductor switches along with their antiparallel diode (unidirectional for voltage and bidirectional for current flow), two...
capacitors $C_1$ and $C_2$ along with one dc voltage source of magnitude $V_{dc}$. The input dc voltage sources can be renewable sources like solar photovoltaic cells, fuel cells, or a battery. Both capacitors have the same voltage rating and equal to the input dc voltage source, resulting in the charging of capacitors up to a voltage rating equal to the dc input voltage. The different voltage levels are given as:

$$V_{dc}, \pm V_{dc} = \pm 2V_{dc}, \pm 3V_{dc}.$$  

This results in thrice-voltage boosting of the input voltage. During the voltage levels of zero and $\pm V_{dc}$, both capacitors are connected in parallel to the dc voltage source, resulting in the charging of capacitors up to $V_{dc}$. During the voltage level of $\pm 2V_{dc}$, both capacitors are connected in parallel and this parallel combination is connected in series with the input voltage source. During the voltage level of $\pm 3V_{dc}$, both capacitors and the dc voltage source are connected in series. Thus, both capacitors are charged and discharged for the same duration of time and thus both voltages have the same magnitude. For the proposed 7L topology, the different switching states along with the charging and discharging of the capacitors have been given in Table 1.

Based on the switching combinations given in Table 1, the output voltage of the proposed boost topology can be expressed as:

$$V_o = \frac{S_{f1} + S_{f2}}{2} + 2S_{f1} + \left(\frac{S_{f3} + S_{f5}}{2}\right) - \left(\frac{S_{f6} + S_{f8}}{2}\right) - \left(\frac{S_{f9} + S_{f10}}{2}\right) - \left(\frac{S_{f11} + S_{f12}}{2}\right) + \left(\frac{S_{f13} + S_{f14}}{2}\right) + 5(S_{f5} - S_{f11} - S_{f12} - S_{f11})$$  

where $S_{fi}$ is the switching function of switch $S_i$ which has two switching logics, i.e. 0 or 1.

The maximum voltage stress across all switches is the important parameter for the topology and it can be represented as the total standing voltage (TSV), which is equal to the sum of maximum voltage stress across the switches. The switches $S_6$, $S_8$, $S_9$ and $S_{10}$ need to block the maximum voltage i.e. $2V_{dc}$. The remaining switches have maximum voltage stress equal to the input dc voltage source, i.e. $V_{dc}$. Therefore, TSV for the proposed topology becomes $16V_{dc}$.

### 2.2 Generalised structure of the proposed boost topology

One of the main design aspects of the proposed topology has been its generalised structure. In the topology shown in Fig. 1, by adding one capacitor and three unidirectional switches, additional two levels can be generated with an increase in voltage gain. The generalised structure of the proposed topology has been shown in Fig. 2. In this structure, all the capacitors used in the topology have the voltage rating equal to the dc input voltage. The different equations for the proposed topology with $N$ number of topology levels are given as:

$$N_{sw} = \frac{3}{2}(N + 1), \quad N_C = \frac{1}{2}(N - 3), \quad G = \frac{1}{2}(N - 1)$$  

$$TSV = 0.5 \times (7N - 17)$$  

where $N_{sw}$, $N_C$, $G$, and TSV represent the number of switches, number of capacitors, voltage gain, and TSV of the generalised structure of the proposed topology, respectively.

### 2.3 Voltage balancing of capacitors

One of the important features of the proposed topology has been the self-voltage balancing of the capacitor voltages. Fig. 3a depicts the equivalent circuit of the charging of both capacitors in the proposed 7L topology. Both capacitors are connected in parallel to the dc voltage source during the voltage levels of zero and $\pm V_{dc}$. The impedance of the charging path consists of the parasitic elements of the switch, their anti-parallel diode, and the equivalent series resistance (ESR), i.e. $r_{ESR}$ of the capacitors. However, all these parasitic elements have a lower value, thus both capacitors are charged close to the input supply voltage. Figs. 3b and 3c show...
Recovering during the charging states of the capacitors, which capacitor voltage drop occurred during the discharging mode is across the switches of the H-bridge is three times to that of the charging loop has a very low time constant compared to the low impedance of the charging path, the magnitude of charging current is high. Therefore, the switches which are connected to the charging path need to be of the higher current rating. To limit the current, a small loop inductor of very low value can be inserted in the charging circuit.

### 3 Comparative study

In this section, a detailed comparison has been carried out with other 7L switched-capacitor-based topologies. As given in Table 2, for 7L, the topology proposed in [4] requires the least number of switches and it uses two dc voltage sources but the topology does not have the boosting feature. Furthermore, the voltage stress across the switches of the H-bridge is three times to that of the input voltage magnitude. In [12], the output voltage gain is 1.5, however with the use of two capacitors. The voltage gain in [12] is lower than the proposed topology. Along with the proposed topology, a gain factor in [10, 13, 14] is three. In [13], the switched-capacitor topology requires ten switches with two capacitors but the maximum blocking voltage on the switch is higher than that of the proposed topology which limits higher voltage applications. Compared to other recently suggested switched-capacitor topology, the proposed topology has advantages such as low-voltage stress on individual switches, which leads to reduce the TSV value, the number of capacitors is two, and the voltage gain is three.

To further validate the performance of the proposed topology in terms of efficiency, efficiency comparison has been carried out. The power loss study of the proposed boost topology has been estimated by thermal modelling in PLECS software. Fig. 4 shows the variation of the estimated efficiency with the output power. For the proposed topology, the maximum value of efficiency is 96.75%. Furthermore, Fig. 4 also depicts the variation of the efficiency of different topologies having triple-voltage gain. The proposed topology along with topology of [13] has similar efficiency at lower power ratings; however as the output power is increased, the efficiency of [13] drops due to the higher voltage stress across the switches, which causes more losses.

### 4 Results and discussion

To validate the theoretical analysis of the proposed 7L topology, an experimental setup is used. The dc input voltage has been fixed to 50 V. The phase disposition-pulse width modulation (PD-PWM) technique is used for the generation of gate pulses for different switches. With PD-PWM for 7L, six carrier signals are compared with the sinusoidal reference signal with a switching frequency of 2.5 kHz. For the experimental results, two capacitors with 2200 µF are used for the boosting purpose. The rating of the capacitor is chosen based on the equation given as

\[
C_1 = C_2 = \frac{l_{pk}}{(\Delta V_C \times f_{sw})} \tag{4}
\]

where \(l_{pk}\), \(\Delta V_C\), and \(f_{sw}\) are the peak load current, voltage ripple, and switching frequency, respectively [9].

Fig. 5a shows the output voltage and current waveform for a series-connected resistive-inductive (RL) load. The main feature of the proposed topology has been the triple-voltage gain and this has been confirmed by the output voltage which has a 150 V peak voltage applications. Compared to other recently suggested switched-capacitor topology, the proposed topology has advantages such as low-voltage stress on individual switches, which leads to reduce the TSV value, the number of capacitors is two, and the voltage gain is three.

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### Table 2 Comparison table for 7L topologies

| Topology | \(N_{sw}\) | \(N_d\) | \(N_{dc}\) | \(N_C\) | \(V_{C,rate}\) | TSV \(_{p.u.}\) | MBV \(_{p.u.}\) | G |
|----------|------------|----------|------------|----------|----------------|----------------|----------------|---|
| [4]      | 7          | 1        | 2          | 1        | 6.3            | 3              | 1              | 1  |
| [10]     | 16         | 0        | 1          | 2        | 5.3            | 0.67           | 3              | 3  |
| [11]     | 10         | 0        | 1          | 3        | \(V_{dc}, V_{dc}/2\) | 5.3            | 0.67           | 1.5|
| [12]     | 9          | 1        | 1          | 3        | \(V_{dc}, V_{dc}/2\) | 5.3            | 0.67           | 1.5|
| [13]     | 10         | 0        | 1          | 2        | \(V_{dc}\) | 6              | 1              | 3  |
| [14]     | 14         | 0        | 1          | 2        | \(V_{dc}\) | 4.7            | 0.33           | 3  |
| [P]      | 12         | 0        | 1          | 2        | \(V_{dc}\) | 5.3            | 0.67           | 3  |

\(N_d\) = number of diodes, \(N_{dc}\) = number of dc voltage sources, TSV \(_{p.u.}\) = TSV (per unit), MBV \(_{p.u.}\) = maximum blocking voltage (per unit), \(V_{C,rate}\) = voltage rating of capacitors.

Bold values indicate that they are proposed topology.

**Fig. 3** Equivalent circuit of the proposed 7L topology with (a) Charging of capacitors during voltage levels of zero and ±\(V_{dc}\), (b) Discharging of capacitors during voltage level of ±\(2V_{dc}\), (c) Discharging of capacitors during voltage level of ±\(3V_{dc}\).

**Fig. 4** Efficiency versus output power curve for different topologies with a triple-voltage gain.

the equivalent circuit of the topology with voltage levels of ±\(2V_{dc}\) and ±\(3V_{dc}\), respectively. From the equivalent circuits, the charging loop has a very low time constant compared to the discharging loops, as shown in Figs. 3b and c. Therefore, the capacitor voltage drop occurred during the discharging mode is recovered during the charging states of the capacitors, which results in the self-voltage balancing of the capacitors. Due to the low impedance of the charging path, the magnitude of charging current is high. Therefore, the switches which are connected to the charging path need to be of the higher current rating. To limit the charging current, a small loop inductor of very low value can be inserted in the charging circuit.
A change in the type of load has also been considered during the resulting from a 50 V dc input voltage. As the charging and discharging cycle of both capacitors takes place simultaneously, both capacitor voltages overlap each other and are shown as $V_c$. Capacitor voltage i.e. $V_C$ is balanced and has a magnitude equal to the dc voltage source i.e. 50 V as depicted in Fig. 5a. Furthermore, a change in the type of load has also been considered during the experimental results. Fig. 5b shows the waveforms as the load changes from no load to a resistive load. At no-load condition, the capacitor voltage is at 50 V with no ripple voltage. As the load of 30 Ω is connected, the capacitor experiences some ripple voltage; however, its voltage is balanced at 50 V.

Further, the dynamic response of the proposed topology has been tested and is shown in Fig. 6. Fig. 6a shows the change of type of load from a purely resistive load to an inductive load. Besides, the dynamic change of load has also been shown in Fig. 6b. All these results prove the suitability of the proposed topology with a different environment. Furthermore, the capacitor voltages remain in balance with every case.

5 Conclusion

In this paper, the working concept of the proposed 7L inverter topology has been discussed and validated. Triple-voltage gain, self-voltage balancing of capacitors, parallel discharging of capacitors, lower voltage stresses, and reduced switch count have been the main features of the proposed boost topology. This benchmark of the recommended 7L boost topology has been confirmed by different comparative studies given in this paper. The compatibility of the proposed topology has been tested with different dynamic loading conditions with experimental results. The proposed 7L topology gives suitable results in all loading conditions with the capacitor’s self-voltage balancing.

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