Low-voltage organic transistors and inverters with ultra-thin fluoropolymer gate dielectric

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We report on the simple fabrication of hysteresis-free and electrically stable field-effect transistors (OFETs) and inverters operating at voltages $<$1-2 V, enabled by the almost trap-free interface between the organic semiconductor and an ultra-thin (<20 nm) and highly insulating single-layer fluoropolymer gate dielectric (Cytop). OFETs with PTCDi-C$_{13}$ (N,N’-ditridecylperylene-3,4,9,10-tetracarboxyliclimide) as semiconductor exhibit outstanding transistor characteristics: very low threshold voltage (0.2 V), onset at 0 V, steep subthreshold swing (0.1-0.2 V/decade), no hysteresis and excellent stability against gate bias stress. It is gratifying to notice that such small OFET operating voltages can be achieved with the relatively simple processing techniques employed in this study.

Organic electronics is expected to enable novel applications, such as large area electronics on flexible and transparent substrates or printed intelligent identification tags. The electrical current in OFETs is mainly confined to the molecular layers in close proximity to an adjacent insulating layer, the gate dielectric. A morphologically and chemically ideal interface between semiconductor and dielectric is free of charge carrier traps. How- ever, charge transport and device stability are adversely affected by imperfections and contaminants, in particular by electrically active chemical groups, often related to water.

Of particular interest for organic electronics is the simple fabrication of organic thin-film transistors (OTFTs) with low operating voltage and high operational stability. High performance and low operating voltage have been achieved by the fabrication of self-assembled molecular monolayers and multilayer dielectrics. Among many polymeric dielectrics, such as cross-linkable polymers and polymer blends, fluoropolymers are particularly promising to meet various requirements: (i) excellent insulation (low gate leakage currents at high electric fields), (ii) high capacitance per unit area (simple and reproducible fabrication of very thin and flat films), (iii) high chemical stability and high water repellency (low interface trap-density, high operational stability and high mobility in combination with both p- and n-type organic semiconductors). The commercially available fluoropolymer Cytop$^\text{TM}$ (Asahi Glass Japan) is an amorphous, optically transparent polymer with a low permittivity (2.1) and has initially been used as gate dielectric in OFETs by Veres et al. It is highly water repellent and yields OFETs of very high electrical quality and very high resistance against gate bias stress. Cytop is an excellent electrical insulator, which was also shown for very thin Cytop films, used as gate insulator for pentacene TFTs. Both p- and also n-type OFETs have been demonstrated on a standard SiO$_2$ dielectric coated with a Cytop layer. The absence of hydroxyl groups and a very high water repellence are preferable interface properties, particularly due to the possibility of electron trapping at the interface by hydroxyl groups. Inorganic dielectrics with a polymer coating or a SAM surface treatment are widely used to fabricate low-voltage complementary inverters.

In this study, we exploited both the highly desirable chemical properties and the excellent insulating properties of ultra-thin Cytop films used as single-layer gate dielectric. In contrast to prevailing assumptions on polymer insulators in general, here we show that sub-20 nm thin fluoropolymer gate dielectrics can provide for high breakdown fields and low current leakage, even if spin-coated over patterned and rather rough bottom gate electrodes. We demonstrate organic thin-film transistors (OTFTs) with excellent electrical characteristics and with low operating voltage, enabling inverter operation below 1-2 V (Fig. 1). A few tenths of a volt (0.3-0.6 V) at the input ($V_{\text{in}}$) of an organic inverter are sufficient for switching the output ($V_{\text{out}}$) between logic high ($V_{\text{DD}}$) and low signals (0 V).

Prior to spin-coating the Cytop layer, we deposited 15 nm of Al at a rate of 0.5-2 A/s as bottom gate electrode onto glass substrates. All metals and organic semiconductors were thermally evaporated through shadow masks at a base pressure near $3 \times 10^{-6}$ mbar. For 20-nm thin Cytop films, Cytop CTL-809 M was dissolved in CT-Solv.180 in the ratio 1:10, spin-coated onto the patterned and pentacene (Sigma Aldrich) were
FIG. 2: (Color online) Performance of PTCDI-C$_{13}$ TFTs with an 18 nm thin Cytop dielectric: (a) Schematic of the TFT geometry used in this study. (b) Transfer characteristics for three typical devices (saturation regime). The gate current is below 10 pA at 2 MV/cm. Inset: The onset is essentially at 0 V, the hysteresis is extremely small ($<0.02$ V) and the subthreshold swing very steep (0.1-0.2 V/decade). (c) The threshold voltage is as low as 0.2 V. (d) Output characteristics are nearly ideal.

FIG. 3: (Color online) Electrical stability of PTCDI-C$_{13}$ TFTs: (a) Threshold voltage shift $\Delta V_T$ due to gate bias stress, for TFTs with 18 nm thin and 120 nm thick Cytop gate dielectrics. (b) Relaxation after gate bias stress (no voltage applied).

Deposited at 0.05-0.3 Å/s. Cr was used as top electrode material and $\approx$ 40 nm were deposited at 0.3-1 Å/s. The sample was exposed to air for $\sim$ 1 h between the fabrication steps. The electrode geometry is optimized to incorporate sub-20 nm thin Cytop dielectrics in place of much thicker Cytop dielectrics (430-700 nm), i.e. there is no overlap of the gate (G) and source/drain (S/D) electrodes where they are separated only by the dielectric (metal-insulator-metal region). For PTCDI-C$_{13}$ TFTs (Fig. 2b), the capacitive G-S and G-D overlap has been reduced to small stripes ($\approx 20$ μm wide), by precise alignment of the shadow masks with specially designed deposition equipment. The channel length $L$ is 250 μm and the channel width $W$ is 450 μm. For inverters, $L=50$ μm and $W=400$ μm (G-S/D overlap is $\approx 50$ μm). OTFT characteristics were measured with a HP 4155A semiconductor parameter analyzer in a He atmosphere ($O_2$, $H_2O<0.6$ ppm). The integration time was 20 ms. The capacitance and electrical insulating properties of Cytop films were measured for metal-insulator-metal (MIM) structures consisting of a Cytop layer sandwiched between Al bottom and Cr top electrodes. Capacitance and leakage current measurements were done in air, with an Agilent 4192A impedance analyzer and an Agilent 4396B high resistance meter.

Typical transistor characteristics from OTFTs with an ultra-thin Cytop fluoropolymer dielectric and PTCDI-C$_{13}$ as semiconductor, are shown in Fig. 2 for three devices (1-3). Particularly noteworthy are several points: low operating voltage with onset at $\approx 0$ V, steep subthreshold swing ($0.1-0.2$ V/decade), essentially ideal transistor characteristics and extremely small hysteresis, i.e. forward and reverse scans are shown in all panels of Fig. 2 but are indistinguishable. The threshold voltage ($V_T$) was as low as 0.2 V (Fig. 2c). The steep subthreshold swing, the vanishingly small hysteresis and the low threshold voltage reveal the low interface trap density. The two-terminal mobility determined from transfer characteristics was $0.14-0.16$ cm$^2$/Vs both for the linear ($V_{DS}=0.2$ V) and the saturation regime ($V_{DS}=3.2$ V). Output characteristics, i.e $I_D$ at constant $V_{GS}$, show linear current increase at low source-drain bias, i.e. ohmic contact resistances, and good saturation at higher bias (Fig. 2d).

The reduction of the gate dielectric thickness from a few 100 nm to less than 20 nm results in a substantial increase in the capacitance parameter unit area and thus in much lower operating voltage. For the substrates of these OTFTs, the measured capacitance per unit area was as high as 100±5 nF/cm$^2$ (area 0.49±0.02 mm$^2$). Nevertheless, the gate leakage current at 2 MV/cm is <10 pA if the TFT is operated in the saturation regime (Fig. 2a). Devices of the same geometry and structure exhibit very similar electrical characteristics.

Spin-on Cytop intrinsically provides for a high resistance against undesirable deterioration of the as-fabricated transistor characteristics, particularly against gate bias stress. In the following we discuss the electrical stability of PTCDI-C$_{13}$ TFTs with an 18 nm thin and for comparison, with a 120 nm thick Cytop dielectric. The stressing experiment was started with a relaxed device (no voltage applied for several hours). Then, we applied a constant gate bias $V_G$ for uninterrupted time periods of 1, 9, 9000 and 20000s and recorded the transfer characteristics in the linear regime ($V_{DS}=0.2$ V) after each period. The threshold voltage $V_T$ was determined from fits to straight lines according to

$$I_D = W L^{-1} \mu_{lin} C_1 (V_G - V_T) V_{DS},$$

where $\mu_{lin}$ denotes the two-terminal mobility. Fig. 3a shows the shift $\Delta V_T$ of the threshold voltage relative to the initial value (0.35 V for 18 nm and 2.6 V for 120 nm Cytop). The straight line indicates sublinear dependence on the stress time $t$, i.e. $\Delta V_T \propto t^\beta$ with $\beta \approx 0.3$. The gate bias during stress periods was positive (electron ac-
for sub-20 nm thin Cytop layers, the capacitance is even according to an equivalent RC circuit (Fig. 4a). Even by impedance and leakage current measurements on we have further characterized the ultra-thin Cytop film rise to the residual small TVS.

ther studies will clarify the detailed mechanism giving 1-2 MΩ and did not change during gate bias stress. Fur-

The contact resistance for these top-contact devices was

tFTs with 18 nm Cytop. Stress measurements were car-

0.14 cm 

thin Cytop (after 2.8 h). The two-terminal mobility was

trom 120 nm thick and 18 nm thin Cytop

TVSs) for both, 120 nm thick and 18 nm thin Cytop

in Fig. 3a. W e find very small threshold voltage shifts

voltage sweep, its stressing effect is relevant for short

and 15 V for TFTs with an 120 nm thick dielectric (drain
cumulation), 2 V for TFTs with an 18 nm thin dielectric, 2 V for TFTs with an 18 nm thin dielectric,

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the electrical breakdown occurred above 6 MV/cm on small spots uniformly distributed over the device area (Fig. 4e, f).

In summary, this study shows that ultra-thin Cytop fluoropolymer gate dielectrics can be successfully incorporated in the fabrication of OTFTs with very low operating voltage. OTFTs with such thin Cytop dielectrics exhibit the same excellent electrical quality and stability as OTFTs with much thicker Cytop dielectrics. These sub-20 nm thin polymer films form gate dielectrics with high breakdown field and low current leakage, even if spin-coated onto non-flat and rather rough gate electrodes. Thus, the present method to increase the dielectric capacitance and to reduce the OTFT operating voltage significantly expands the options for practical device design and fabrication, and is promising for other material combinations.

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the essential role played by the dielectric layer, we have further characterized the ultra-thin Cytop film by impedance and leakage current measurements on metal-insulator-metal (MIM) structures. The capacitance was determined from impedance measurements according to an equivalent RC circuit (Fig. 4a, b). Even for sub-20 nm thin Cytop layers, the capacitance is essentially frequency independent (Fig. 4c) and in agreement with the value calculated from the geometry, i.e. 

\[ C_i = \varepsilon_0 \varepsilon_i d \]

where \( C_i \) is the capacitance per unit area, \( \varepsilon_i = 2.1 \) is the permittivity of Cytop and \( d \) is the thickness of the insulating layer as measured with a surface step profiler, averaged over several measurement points on the same substrate (±1 nm). The high-frequency response (\( f > 1 \text{MHz} \)) is dominated by a serial resistance (≈ 300 Ω). Fig. 4c shows the leakage current for four different devices (1–4) on two substrates, measured with crossed electrodes (Fig. 4d). The leakage current is well below 10 pA for electric fields lower than 2 MV/cm. For these devices,