Power Enhancement of Silicon Membrane-based Thermoelectric Energy Harvester with Tailored Holey Nanostructures

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Abstract. We develop SOI-based silicon membrane thermoelectric power generator with phononic crystal nanostructures. Phononic crystal nanostructures which are well designed periodic structures considering phonon mean free path enhance phonon scattering to reduce thermal conductivity of silicon membranes and improve their thermoelectric figure of merit twice. We demonstrate power enhancement of thermoelectric generator with nanostructure patterning. By using nanoimprint lithography method, we pattern this phononic crystal nanostructures in 3 x 2 mm area of silicon membrane for thermoelectric devices.

1. Introduction
Thermoelectric power generators (TEGs) promise not only recovering the wasted heats but also harvesting energy from environmental unused heats. Recently, demands for autonomous battery strongly increase as the number of sensors more and more populates. For this application, silicon thermoelectrics device is one of a good candidate because of its mass-productivity and less toxic property. While complex heavy metal semiconductors, such as BiTe or PbTe, shows good thermoelectric figure of merit $ZT = S^2\sigma T/\kappa$ composed of Seebeck coefficient $S$, electrical conductivity $\sigma$, thermal conductivity $\kappa$, and temperature $T$[1], bulk silicon has poor thermoelectric performance due to its relatively high thermal conductivity. Recent study showed, however, nanostructuring can reduce thermal conductivity of material, and many nanostructured Si have been reported as a good thermoelectric material[2–4]. Furthermore, it is expected that phononic crystal (PnP) nanopatterning impedes heat conduction and enhance the thermoelectric performance, our group’s previous work demonstrated well designed nanostructures considering with phonon mean free path (MFP) can improve $ZT$ efficiently by reducing $k$ while keeping high $s$[5].

In this work, we fabricate membrane-based silicon TEGs, and demonstrate power enhancement with holey PnP nanostructures. In previous study, we experimentally characterized thermoelectric properties of poly-Si membrane nanostructured with PnP, and achieved twice higher $ZT$ compared with pristine Si membrane[6]. This work moves silicon thermoelectric study with PnP nanostructures from material field to device demonstration.

2. Methods
We fabricated Uni-leg (mono-doped) TEGs in SOI wafers composed of 300-nm-thick n-type polycrystalline Si active layer and 2.5 mm BOX layer on Si substrate. The uni-leg TEG is fabricated with one ion implantation and two lithographies for Si etching and metal deposition which is much less steps than the ones for typical membrane based TEG fabrication[7]. First, we doped top poly-Si layer of SOI wafer with phosphorous ion implantation and thermal annealing at 900 °C for 1 minute. Next, we created PnC nanostructures by inductively coupled plasma reactive ion etching for Si with EB lithography mask, and consequently Au deposition for wire and electrode followed. Finally, we removed BOX layer by using vapor phase hydrofluoric acid except both ends of each unit to keep suspension. In the same process, samples without PnCs were also fabricated as the references. Figure 1 shows images of fabricated samples.

3. Measurement results and discussion

As shown in figure 2(a), the measured total resistance is proportional to the number of units, and the resistance of one unit is calculated as ~184 Ω and ~95 Ω for PnC samples and membrane samples respectively. Figure 2(b) shows the open circuit voltage as function of set temperature difference ΔTSET between substrate and ambient air. The induced voltage in PnC samples have 2.5 times larger than unpatterned sample because of large temperature difference created by high thermal resistance of PnC structure. We calculated the output power per unit area P from measured total resistance R and thermoelectric voltage V as P = V^2/4R.
Figure 2. (a) Measured total internal electrical resistance of devices as a function of number of units. (b) Measured open circuit voltage of thermoelectric effect and (c) output power per unit area as a function of applied temperature difference $\Delta T$.

Figure 2(b) shows that the PnC device achieves 5 times larger output power. This enhancement is larger than the amount of ZT improvement in the PnC material which is about 4 times large value than membrane without PnC[5]. Although the PnCs decrease electrical properties, for the device performance, it plays more important role that large temperature difference induced by the PnC.

Output power of PnC device reached 12 nW from 40 K environmental temperature difference with assumption of 1 cm$^2$ integration, but this value is not enough for IoT sensor network application. Main problem is that suspended part is not well cooled and only 1 % of temperature difference is induced in the device from environment temperature difference. This is caused by weak connection between top Si membrane and SiO$_2$ pillar which transfer heat from substrate to suspended membrane.

For the further improvement of device performance, we started to fabricate typical bi-leg TEG with PnC nanostructures. Figure 3 shows 2 mm x 3 mm large area of thermoelectric device arrays composed of p- and n-type regions. Part of device are periodically suspended, and each suspended bridge has PnC nanostructures same as previous device. We use nanoimprint lithography technique to make nanoscale hole array pattern on such large area. Device is successfully fabricated and under experiment.

Figure 3. Scanning microscope images of (a) whole structure of large area TEG and (b) close-up view of p- and n-type regions of device. Red colored area shows one of suspended part, and all suspending bridge have PnC nanostructures.
4. Conclusion
We fabricated the uni-leg TEG with PnC nanostructure and measured the thermoelectric power of TEG. We demonstrated the PnC TEG shows 5 times larger output power than the one of membrane TEG. We also showed the uni-leg TEG works successfully which can be fabricated less steps compare to the traditional TEG and easily integrated with other silicon devices. For the further improvement of output power, we designed large area TEG with nanostructures fabricated by using nanoimprint lithography.

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References
[1] Snyder G J and Toberer E S 2008 Complex thermoelectric materials Nat. Mater. 7 105–14
[2] Boukai A I, Bunimovich Y, Tahir-Kheli J, Yu J-K, Goddard III W A and Heath J R 2008 Silicon nanowires as efficient thermoelectric materials Nature 451 168–71
[3] Hochbaum A I, Chen R, Delgado R D, Liang W, Garnett E C, Najarian M, Majumdar A and Yang P 2008 Enhanced thermoelectric performance of rough silicon nanowires Nature 451 163–7
[4] Lim J, Wang H-T, Tang J, Andrews S C, So H, Lee J, Lee D H, Russell T P and Yang P 2016 Simultaneous Thermoelectric Property Measurement and Incoherent Phonon Transport in Holey Silicon ACS Nano 10 124–32
[5] Nomura M, Kage Y, Müller D, Moser D and Paul O 2015 Electrical and thermal properties of polycrystalline Si thin films with phononic crystal nanopatterning for thermoelectric applications Appl. Phys. Lett. 106 223106
[6] Yanagisawa R, Tsujii N, Paul O, Mori T and Nomura M 2018 Importance of grain size for nanostructured poly-Si thermoelectric material J. Phys. Conf. Ser. 1052
[7] Xie J, Lee C and Feng H 2010 Design, Fabrication, and Characterization of CMOS MEMS-Based Thermoelectric Power Generators J. Microelectromechanical Syst. 19 317–24