Triplet Spike Time Dependent Plasticity: A floating-gate Implementation

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Abstract— Synapse plays an important role of learning in a neural network; the learning rules which modify the synaptic strength based on the timing difference between the pre- and postsynaptic spike occurrence is termed as Spike Time Dependent Plasticity (STDP). The most commonly used rule posits weight change based on time difference between one presynaptic spike and one postsynaptic spike and is hence termed doublet STDP (D-STDP). However, D-STDP could not reproduce results of many biological experiments; a triplet STDP (T-STDP) that considers triplets of spikes as the fundamental unit has been proposed recently to explain these observations. This paper describes the compact implementation of a synapse using single floating-gate (FG) transistor that can store a weight in a nonvolatile manner and demonstrate the triplet STDP (T-STDP) learning rule by modifying drain voltages according to triplets of spikes. We describe a mathematical procedure to obtain control voltages for the FG device for T-STDP and also show measurement results from a FG synapse fabricated in TSMC 0.35μm CMOS process to support the theory. Possible VLSI implementation of drain voltage waveform generator circuits are also presented with simulation results.

Index Terms— SNN, STDP, BCM, floating gate, long term potentiation, long term depression, spike triplet, computational neuroscience.

I. INTRODUCTION

Over the past ten years, numerous experimental studies [1]–[4] have shown that the synaptic strength varies as a function of the precise spike timing difference \( \Delta t = t_{\text{post}} - t_{\text{pre}} \) between the firing times \( t_{\text{pre}} \) and \( t_{\text{post}} \) of the presynaptic and postsynaptic neurons respectively. This synaptic plasticity rule, called Spike Time-Dependent Plasticity (STDP), has evolved as one of several unsupervised plasticity rules that play an important role in learning and memory in the brain. The mathematical model of STDP based on a pair of pre- and postsynaptic spike is referred as doublet STDP (D-STDP) while the one based on triplet of synaptic spikes [5]–[8] i.e either pre-post-pre synaptic spike or post-pre-post synaptic spike is referred to as triplet STDP (T-STDP). Several variants of these rules have also been proposed for pattern classification tasks [9], [10].

Experimental results [11] indicate that D-STDP model based on pairs of spikes are not sufficient to explain synaptic changes due to triplets or quadruplets of spikes. D-STDP model also fails to reproduce frequency effects. However, T-STDP model can reproduce frequency effects along with the explanation of synaptic changes due to triplets and quadruplets of spikes. It is also important to be able to replicate rate based plasticity experiments. It has been demonstrated that the Bienenstock-Cooper-Munro (BCM) learning rule [12] based on firing rates can be obtained from D-STDP when presynaptic and postsynaptic neurons fire uncorrelated or weakly correlated Poisson spike trains, and only nearest-neighbor spike interactions are taken into account [13]. However, it is not possible to make a strict theoretical mapping from the nearest-spike interactions of D-STDP models to the BCM rule [11] whereas T-STDP allows for such theoretical mapping. Apart from these experimentally observed benefits of T-STDP model, there are some computational advantages as well [14]. It has been shown that T-STDP can detect input correlations higher than the second order ones to which D-STDP is sensitive. Hence, it has been shown to drive direction and orientation selectivity [14]. Further, it can be shown to reproduce a more generalized version of BCM overcoming the limitations of the original one. Though there are several models of plasticity with varying degrees of bio-realism [15], T-STDP is a good compromise between simplicity and richness of function. Its simplicity also lends itself to easy analysis making it a good choice for a plasticity rule with functionality beyond D-STDP.

Recently STDP became so popular in computational neuroscience that neuromorphic engineers who try to emulate brain function using VLSI have also tried to emulate this behaviour in silicon. However, implementing a compact learning synapse continues to be one of the big challenges in the field [16].

Several recent papers have reported D-STDP implementations [17]–[21] and T-STDP implementation [22]; however, these synapses could either only store states in a transient fashion (using charge on a capacitor) or only hold two states in the long term. The size of these synapses are also large hindering scalability of these designs. A promising solution for non-volatile analog weight storage in very small area is provided by a floating-gate (FG) device [16], [23]–[30]. This concept was utilized recently to show weight storage and adaptation due to quantum phenomena based on input signal timing [30].

Compared to other work, here we demonstrate for the first time the implementation of the T-STDP rule in a FG synapse by appropriately modifying the drain voltage pulse based on spike triplets. From chip measurement results, we show that FG synapse in Fig. 3(b) can reproduce (1) D-STDP learning window and (2) T-STDP results when appropriate control signals are applied on its terminals. Some initial results for triplet experiment based on this work were presented in [31]. In this paper, we present results for quadruplet experiments and frequency effects as well as a new drain voltage generation scheme. We also present circuits for VLSI implementation of the drain voltage waveforms.

The paper is organized as follows: Section II provides a brief

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explanation of STDP models, D-STDP and T-STDP. Section III introduces the working of floating gate synapse, relation between FG synapse and D-STDP rule and then, finally arrive at the relation between FG synapse phenomenon and T-STDP rule. The experimental results are included in section IV. Section V presents a hardware implementation of the drain voltage waveform generator along with the simulation results. Finally the paper is concluded with discussions on consolidated work.

II. STDP SYNAPTIC MODIFICATION RULE

In biology, synapses are specialized structures that permit the transfer of signals between two neurons with an associated synaptic strength or weight. Learning typically implies the modification of synaptic weight due to the activities of the pre- and post-synaptic neurons. The STDP models are explained in detail next.

A. Doublet STDP (D-STDP) Model

In D-STDP, potentiation occurs when a postsynaptic spike precedes a presynaptic spike; otherwise depression happens. The weight changes can be governed by a temporal learning window. The temporal learning window for STDP can be expressed as [11], [22]

\[
\Delta w(t) = \begin{cases} 
\Delta w^+ = A^+ e^{\frac{-\Delta t}{\tau_+}} & \text{if } \Delta t \geq 0 \\
\Delta w^- = -A^- e^{\frac{-\Delta t}{\tau_-}} & \text{if } \Delta t < 0
\end{cases}
\]

(1)

where \(\Delta t = t_{post} - t_{pre}\) is the time difference between a post-synaptic and pre-synaptic spike, \(\tau_+\) and \(\tau_-\) are the time constants of the learning window, and \(A^+\) and \(A^-\) are the maximal weight changes for potentiation and depression, respectively. The theoretical graph for the above equation is simulated using MATLAB and is shown in Fig. 1 with the parameters being obtained by data fitting as explained in [11]. As mentioned in [2], \(\tau_+\) and \(\tau_-\) are taken as 16.8ms and 33.7ms respectively for the simulation.

B. Triplet STDP (T-STDP) Model

Previous studies [7], [32] show that the D-STDP model fails to reproduce the experimental outcomes involving higher order spike patterns such as triplet and quadruplets of spikes and furthermore, fails to account for the observed weight dependence on repetition frequency of pairs of spikes. To resolve the above mentioned issues, the D-STDP model was extended in [11] to include spike triplets resulting in T-STDP model which could sufficiently reproduce physiological experiments.

The T-STDP rule is written as a function of difference in spike timings as, [11], [22]

\[
\Delta w^+ = e^{\frac{-\Delta t_1 \tau_+}{A_2^+ + A_3^+ e^{\frac{-\Delta t_2 \tau_2}{A_2^+}}}} \text{ if } t = t_{post} \\
\Delta w^- = -e^{\frac{-\Delta t_1 \tau_+}{A_2^- + A_3^- e^{\frac{-\Delta t_2 \tau_2}{A_2^-}}}} \text{ if } t = t_{pre}
\]

(2)

where \(A_2^+\) and \(A_2^-\) denote the amplitude of the weight change whenever there is a pre-post pair or a post-pre pair respectively. Similarly, \(A_3^+\) and \(A_3^-\) denote the amplitude of the triplet term for potentiation and depression, respectively.

In [11], though the T-STDP rule above is introduced first, it is shown later that not all terms are needed to explain biological data. Thus two different minimal models are defined later: (1) \(A_3^+ = 0\) and \(A_3^- = 0\) for visual cortex data and (2) \(A_3^- = 0\) for hippocampal culture data set. Hippocampal culture data set [7] is used for obtaining the results for triplets of spikes whereas visual cortex data [32] is used for showing the frequency effects of T-STDP rule. For visual cortex data set, equation (2) simplifies to,

\[
\Delta w(t) = \begin{cases} 
\Delta w^+ = A_3^+ e^{\frac{-\Delta t_1 \tau_+}{A_2^+}} e^{\frac{-\Delta t_2 \tau_2}{A_2^+}}; & t = t_{post} \\
\Delta w^- = -e^{\frac{-\Delta t_1 \tau_+}{A_2^-}} (A_2^-); & t = t_{pre}
\end{cases}
\]

(3)

On the other hand, for hippocampal culture data set, equation (2) simplifies to,

\[
\Delta w(t) = \begin{cases} 
\Delta w^+ = e^{\frac{-\Delta t_1 \tau_+}{A_2^+ + A_3^+ e^{\frac{-\Delta t_2 \tau_2}{A_2^+}}}} (A_2^-); & t = t_{post} \\
\Delta w^- = -e^{\frac{-\Delta t_1 \tau_+}{A_2^-}} (A_2^-); & t = t_{pre}
\end{cases}
\]

(4)

For both cases, \(\Delta w^-\) is exactly same as the case of long term depression (LTD) in D-STDP as shown in equation (1). Hence, to implement the triplet rule in circuits, we only need to modify pre-existing FG design to add the extra term in the potentiation case.

III. FLOATING GATE SYNAPSE

Fig. 3(a) shows the architecture of a single floating gate synapse in prior work [30]. It has three main terminals for programming as shown in the dashed box. The terminals are named as gate, drain and tunnel terminals with the respective voltages denoted as \(V_g\), \(V_d\) and \(V_{tun}\). A “non-STDP” behaviour seen in this work is ameliorated in our previous work [25], [26] along with detailed analysis of the operation of the D-STDP learning rule in a floating gate synapse. In previous works [25], [26], [30], the quantum mechanism of tunneling
is spread across a larger time scale (illustrated in Fig. 4(a) and (b)) which makes it difficult to analyze the effect of triplets and quadruplets of spikes in a floating gate synapse. Similar to an approach in [28], [29], the effect of tunneling can be localized at the occurrence of pre-synaptic spikes with the modification (red blocks) shown in the architecture of Fig. 3(b) making it easier to mathematically analyze the weight change for triplets. In the new architecture, whenever a pre-synaptic spike occurs, a triangular gate voltage waveform is generated which will create an exponential excitatory post-synaptic current (EPSC), similar to biology, because of the exponential relationship between the gate voltage and drain current of the MOS transistor in subthreshold region. The current at the maximum gate voltage is nearly zero. Similarly, whenever a post-synaptic spike arrives, a global triangular tunnel voltage waveform and an inverted pulse drain voltage waveform is generated. The global triangular tunnel voltage waveform is then sampled at the occurrence of pre-synaptic spike with the help of pulse extender block and the multiplexer. This creates a voltage waveform, $V_{\text{tun}}$, at the tunnel terminal. Thus, in the new architecture, during pre-synaptic spike, a gate voltage, $V_g$, and a tunnel voltage, $V_{\text{tun}}$, waveforms are generated and during post-synaptic spike, a drain voltage, $V_d$, waveform is generated. Whereas, in the previous architecture, a gate voltage waveform is generated during pre-synaptic spike and both drain voltage and tunnel voltage waveforms are generated during post-synaptic spike.

The equation for drain current of a subthreshold saturated pFET whose well is tied to $V_{dd}$ is given by [30]

$$I_d = I_{d0}e^{\kappa(V_{dd} - V_{t0})/U_T}$$

(5) where $U_T$ is the thermal voltage and $\kappa$ is the gate coupling coefficient.

Weight modification in a FG synapse uses a combination of hot-electron injection (HEI) and Fowler-Nordheim tunneling [30]. HEI adds electrons on to the floating gate node, which reduces the floating gate voltage resulting in more current through the transistor hence increasing the weight of the synapse. On the other hand tunneling removes electrons from the FG node to reduce the synaptic weight. In our previous paper [25], for the case of D-STDP, a gate voltage waveform is generated at every pre-synaptic spike while at every post-synaptic spike, a tunneling voltage and a drain voltage is generated as illustrated in Fig. 4(a). This shows that at every pre-synaptic spike only tunneling happens while at every post-synaptic spike there is both injection and tunneling. The occurrence of both tunneling and injection at the post-synaptic spike arrival necessitates the effect of injection to be greater than tunneling to obtain potentiation as in the traditional D-STDP learning window. Moreover since the effect of tunneling is spread over a long time, mathematical analysis or intuitive understanding of the effect due to multiple pre- and post-synaptic spikes becomes difficult. In contrast, the mathematical versions of both STDP models have potentiation and depression of weights localized at pre- and post-synaptic events. Hence, to relate the mathematical analysis of FG synapse with the T-STDP model easily, we also decided to localize the effect of tunneling and injection at pre- and post-synaptic pulses respectively. A similar technique has also been used in [28], [29].

An illustration for this is shown in Fig. 4(b) where a tunneling voltage waveform is still created at every post-
synaptic pulse as in earlier work [25], [30] but is not applied directly to the tunneling junction of the FG. Instead, it is sampled by the pre-synaptic pulse through a multiplexer to create a new waveform $V_{tun,ff}$, which is applied to the FG (refer to Fig. 3). Figure 4(b) also shows the specifications of terminal voltage waveforms for the case of triplets of spike. The well for the high voltage PMOS in the multiplexer can be shared with tunneling junction; nevertheless, this incurs an area penalty motivating us to look at possibilities of using non-localized tunneling for T-STDP in future. The governing equations for injection and tunneling are given as [30], [33]

$$I_{inj} = I_{inj}(I_d/I_{sh})^\alpha e^{-\Delta V_{inj}/V_{inj}}$$
$$I_{tun} = I_{tun}e^{(V_{tun}-V_{g})/V_{ox}}$$

(6)

where $I_d$ is the drain current, $\alpha = 1- U_T/V_{inj}$, $V_{ox}$ and $V_{inj}$ are process dependent parameters.

A. D-STDP Model on a Floating Gate Synapse (FG D-STDP)

The weight of the synaptic device can be defined as [30]:

$$w = e^{-\alpha V_{tun} / V_T}$$

(7)

Hence, equations to predict the change in FG voltage effectively predict the change in weight. The following assumptions are made in deriving the theoretical equations [25]:

1) To ensure small change in weight at very large negative and positive values of $\Delta t$, $V_{inj}$ has to be high enough so that $V_{tun, max} - V_{inj}$ is small enough for negligible tunneling. Similarly $\Delta V_g = V_{g, min} - V_{g, min}$, should be small enough so that $V_{tun, min} - V_{g, min}$ is small enough for negligible tunneling.

2) Strong coupling from gate to floating gate node where as a weak coupling from tunneling node to floating gate node. This is justified since typically gate capacitance, $C_g >>$ tunneling capacitance, $C_{tun}$.

3) The gate voltage waveform falls to its minimum value instantaneously. In other words, $S_1 >> S_2$, $S_3$ as shown

Fig. 4: Timing diagram and voltage specifications of FG synapse: (a) D-STDP model, cases of long term potentiation (LTP) and long term depression (LTD), where effect of injection and tunneling is present in LTP where as only tunneling effect is present for LTD. These waveforms are used in our previous paper (b) The details of timing and voltage specifications used for testing the FG synapse for both triplet protocols is shown here. The modification of tunneling voltage, $V_{tun,ff}$ (shown in red) sampled from $V_{tun}$ is shown. (c) Different cases of drain voltage waveform, $V_d$ for different experiments like pairing protocol, triplets and quadruplets.
in Fig. 4(a).

One difference from the earlier case in [25] is that now we only have injection for $\Delta t > 0$ and only tunneling for $\Delta t < 0$ due to the localization of tunneling effects.

We can now derive the slow time scale equation [30] for change in FG voltage due to tunneling and injection as:

$$C_T \frac{dV_{fg}}{dt} = I_{inj} - I_{inj} = C_T \frac{dV_{fg,\text{tun}}}{dt} - C_T \frac{dV_{fg,\text{inj}}}{dt}$$  \hspace{1cm} (8)

where $C_T$ is the total capacitance on the FG node and $V_{fg}$ denotes change on a slow time scale.

1) Case 1: $\Delta t > 0$: First, we consider the case of $\Delta t > 0$ i.e the positive axis of STDP curve and combine equations (6) and (5) to get:

$$C_T \frac{dV_{fg,\text{inj}}}{dt} = -I_{inj} = -I_{inj} \left( e^{\alpha(V_{dd}-V_{fg})/U_T} \right) e^{-\Delta V_{ds}/V_{inj}} \hspace{1cm} (9)$$

where $V_{fg,\text{inj}}$ is the slow time scale change in $V_{fg}$ due to injection only. Since change in $V_{fg}$ on the RHS happens due to coupling from the gate voltage, we can write:

$$V_{fg} = V_{fg,\text{min}} + \frac{C_y}{C_T} S_2 t$$ \hspace{1cm} (10)

where $S_2$ is the positive slope of $V_y$ and $C_y$ is the capacitance connected between the gate terminal and the floating gate terminal. Here $V_{fg,\text{min}}$ is not same as $V_{fg,\text{inj}}$ due to initial charge stored on the FG. Substituting equation (10) in equation (9), we get:

$$C_T \frac{dV_{fg,\text{inj}}}{dt} = -A e^{-X t}$$ \hspace{1cm} (11)

where

$$A = \frac{I_{inj}}{e^{\alpha(V_{dd}-V_{fg,\text{min}})/U_T}} \left( e^{-\Delta V_{ds}/V_{inj}} \right)$$

$$X = \frac{\alpha C_y S_2}{C_T U_T}$$ \hspace{1cm} (12)

Referring to Fig. 4(a), significant amount of injection happens in the time from $\Delta t$ to $\Delta t + T_d$ (circled in red), where $\Delta V_{ds}$ is constant and significant. Also, since $T_d$ is very small compared to $T_y$, we can assume that $V_y$ is constant during the drain pulse. Hence, we finally get:

$$C_T \Delta V_{fg,\text{inj}} = -A \Delta t e^{-X t} \hspace{1cm} (13)$$

For more details of the derivation, we refer the interested readers to [25].

With reference to Fig. 4(b), since we have modified the tunneling voltage waveform from $V_{\text{tun}}$ to $V_{\text{tun, eff}}$ the effect of tunneling is not present in $\Delta t > 0$. Hence, we have $\Delta V_{fg} = \Delta V_{fg,\text{tun}}$.

2) Case 2: $\Delta t < 0$: Now we consider the case of $\Delta t = (t_{\text{post}} - t_{\text{pre}}) < 0$ i.e the negative axis of STDP curve. Similar to what we have done above, let us see the effect of tunneling and injection separately.

For the contribution of injection to $V_{fg}$, we could see that injection happens only during the initial small period, $T_d$ of time axis where the drain current of the MOS is almost zero. So we can completely neglect the effect of injection on $V_{fg}$ in this case.

Now let us consider the contribution of tunneling to $V_{fg}$. Similar to the analysis above, using assumption 1, we have:

$$C_T \int_0^{\Delta V_{\text{fg, tun}}} dV_{fg} = \int_{-\Delta t}^{T_{\text{tun}}} I_{\text{tun}} dt \hspace{1cm} (14)$$

Also, similar to the case of positive $\Delta t$, here we have:

$$V_{\text{tun}} = V_{\text{tun, min}} + \frac{C_y}{C_T} S_3 \left( -(-\Delta t) \right)$$

$$V_{\text{tun, eff}} = \begin{cases} V_{\text{tun}}; & -\Delta t < t < -\Delta t + T_{\text{tun, pulse}} \\ V_{\text{tun, init}}; & \text{for other values of } t \end{cases} \hspace{1cm} (15)$$

Substituting equations (15) and (6) into equation (14), we get:

$$C_T \Delta V_{fg,\text{tun}} = B e^{-\frac{C_y S_2}{C_T V_{ox}} \Delta t} \int_{-\Delta t}^{\Delta t+T_{\text{tun, alse}}-\Delta t} e^{Y t} dt \hspace{1cm} (16)$$

where

$$Y = \frac{S_3 - \frac{C_y S_2}{C_T}}{V_{ox}}$$

$$B = I_{\text{tun, 0}} e^{\frac{V_{\text{tun, min}} - s_3 T_{\text{tun, delay}} - V_{\text{tun, max}}}{V_{ox}}}$$

$$B' = B / Y \hspace{1cm} (17)$$

Since injection is negligible for $\Delta t < 0$, we have $\Delta V_{fg} = \Delta V_{fg,\text{tun}}$.

B. T-STDP Model on a Floating Gate Synapse (FG T-STDP)

Comparing equation (1) with equation (2), the extra contribution of tunneling in equation (4) by a single pulse of width $T_d$ at $t_{\text{post}}$ (Fig. 4c) – however, the voltage $V_d$ depends on the time difference $\Delta t_2$ between successive post spikes. So from Fig. 4(c) expression for $V_d$ becomes:

$$V_d = \begin{cases} V_{d,\text{min}} - \Delta V_d(\Delta t_2); & \text{for other values of } t \\ V_{d,\text{init}}; & \text{for other values of } t \end{cases} \hspace{1cm} (18)$$

Note that to satisfy the results of the doublet case, $\Delta V_d(\Delta t_2) \to 0$ as $\Delta t_2 \to \infty$.

2) Double-pulsed $V_d$: The double-pulsed $V_d$ waveform (Fig. 4c) implements the doublet term with the first
pulse of width $T_d$ and amplitude same as in FG D-STDP. It then creates the extra triplet term with the following pulse again of width $T_d$ but with different amplitude. The entire waveform is given by:

$$V_d = \begin{cases} V_{d,\text{min}}: & t_{\text{post}}(n) < t < t_{\text{post}}(n) + T_d \\ V_{d,\text{init}} - \Delta V_d^f(\Delta t_2): & t_{\text{post}}(n) + T_d < t < t_{\text{post}}(n) + 2 \cdot T_d \\ V_{d,\text{ini}}: & \text{for other values of } t \end{cases}$$

Again, note that to satisfy the results of the doublet case, $V_{d,\text{ini}} - \Delta V_d^f(\Delta t_2) \rightarrow V_{d,\text{init}}$ as $\Delta t_2 \rightarrow \infty$ second pulse in double-pulsed $V_d$ vanishes as $\Delta t_2 \rightarrow \infty$.

As can be seen above, both cases of drain voltage waveform will require some different method to calculate $\Delta V_d^f(\Delta t_2)$ and $\Delta V_d^f(\Delta t_2)$ to match results from the T-STDP model with desired parameters. So, next we do a comparison of the FG phenomenon and T-STDP model to understand the kind of modification to be done. Here, we consider only the FG phenomenon of injection that happens at post-synaptic pulses, since our modification has localized tunneling to pre-synaptic events. Then, we can equate this to the weight change from T-STDP model for any specific case (e.g. hippocampal culture events. Then, we can equate this to the weight change due to FG T-STDP on triplets and doublets of spike can be written as:

$$Y_{fg} = \frac{\Delta W_{\text{triplet}}}{\Delta W_{\text{doublet}}} = \frac{\Delta V_{\text{triplet}}}{\Delta V_{\text{doublet}}} = e^{\Delta V_d^f(\Delta t_2)/V_{inj}}$$

(25)

3) T-STDP rule for spike doublets and triplets

For the case of T-STDP and D-STDP models the ratio $Y$ can be obtained directly from equation (4) as:

$$Y_{\text{theory}} = \frac{\Delta W_{\text{triplet}}}{\Delta W_{\text{doublet}}} = 1 + A_2^+ e^{(-\Delta t_2)/\tau_y}$$

(26)

Now, we can equate the $Y_{fg}$ values in equations (23) and (25) with the $Y_{\text{theory}}$ value in equation (26) to get the desired drain voltage parameters.

a) Single-pulsed $V_d$:

$$Y_{fg} = Y_{\text{theory}}$$

$$\Rightarrow e^{\Delta V_d^f(\Delta t_2)/V_{inj}} = 1 + A_2^+ e^{(-\Delta t_2)/\tau_y}$$

(27)

b) Double-pulsed $V_d$:

$$Y_{fg} = Y_{\text{STDP}}$$

$$\Rightarrow e^{\Delta V_d^f(\Delta t_2)/V_{inj}} = A_2^+ e^{(-\Delta t_2)/\tau_y}$$

(28)

C. Parameter Translation from Theory to FG model

Given values of parameters such as $A_2^+$ or $A_3^+$ of the theoretical model, it should be possible to use the above equations (27) and (28) to find the values of $\Delta V_d^f$ and $\Delta V_d^f$. However, in our case, the measurement setup restricted the temporal width of voltage waveforms to a maximum value of 300ms (note the maximum time duration used for $T_{\text{run}}$). Hence, compared to the learning window $\tau^+$ (refer to Fig. 1) shown in [11], our learning window $\tau_{fg}^+$ (Fig. 5) has lesser width. This implies that we need to apply a compression factor on the time scale to match our results with those in [11]. We define the compression factor $r$ as follows:

$$r = \frac{\tau^+}{\tau_{fg}^+}$$

(29)
Next, we show this translation explicitly for the three experimental protocols considered in [11].

1) Triplet experiments:
For the different parameters of hippocampal culture data set from table 4 in [11] i.e $A_3^f = 9.1 \times 10^{-3}$, $A_3^t = 4.6 \times 10^{-3}$ and $\tau_g = 48$ ms, we can obtain from equation (27) for the case of single-pulsed $V_d$ waveform $\Delta V_d^s(\Delta t_2) \approx 0.24$ V for the case of $\Delta t_2 = 10$ ms and $\Delta V_d^f(\Delta t_2) \approx 0.21$ V for $\Delta t_2 = 20$ ms. Similarly, for the case of double-pulsed $V_d$ waveform, we can obtain from equation (28): $\Delta V_d^f(\Delta t_2) \approx 0.12$ V for the case of $\Delta t_2 = 10$ ms and $\Delta V_d^f(\Delta t_2) = 66$ mV for $\Delta t_2 = 20$ ms. The definitions of ($\Delta t_1$ and $\Delta t_2$) here are similar to [22] and are different compared to the notations given in [11]. For clarity, the difference is shown in Fig. 2.

As an example, the data points chosen in protocol 2 are given by ($\Delta t_1/r, \Delta t_2/r$) where ($\Delta t_1, \Delta t_2$) = (-5,5), (-10,10), (-5,15) and (-15,5) ms corresponds respectively to data points in [11].

2) Frequency effects of pairing protocol:
In [11], $\Delta t$ used for the case of frequency effects is 10 ms which is halved to 5 ms for obtaining the measurement results in this paper. Also, $\rho$ Hz mentioned in frequency effects of pairing protocol results of [11] will be equal to $r \times \rho$ Hz in our measurement results.

3) Quadruplet experiments:
Quadruplet experiments contain two temporal variables $\Delta t$ and $T$ as shown in Fig. 4(c). $\Delta t = 5$ ms in [11]– hence, we have used $\Delta t = 2.5$ ms for measurements. Then the chip measurement values for quadruplets are taken for different values of $T/r$ up to 80 ms. For comparing these measurement results with mathematical model, we simulated the mathematical model for double the value of $T/r$ i.e up to 160 ms.

IV. RESULTS
The measurement results shown in this section is obtained from a single FG synapse fabricated in TSMC 0.35 µm CMOS process with $C_g = 5.5$ pF. Though not optimized for synaptic density, the results here do serve as a proof of concept for our FG T-STDP implementation.

A. FG D-STDP learning window
The first set of testing on FG synapse is to check whether the FG T-STDP can reproduce D-STDP learning window. Fig. 5 shows the D-STDP learning window obtained from FG synapse. Thus for obtaining the result, we set $V_{\omega_{min}}$ as 0.3 V (here, $\Delta V_d(\Delta t_2) = 0$ w.r.t the mathematical analysis done in the section [11] and other voltage specifications are as given in Fig. 4(b) i.e $V_{dd} = 5.2$ V, $V_{\omega_{init}} = 3.3$ V, $V_{\omega_{min}} = 2.5$ V, $T_g = 100$ ms, $T_{\omega_{init}} = 5.4$ V, $\tau_{\omega_{max}} = 16.5$ V, $T_{\omega_{max}} = 300$ ms, $T_{\omega_{delay}} = 1$ ms, $T_{\omega_{rise}} = 2$ ms, $V_{\omega_{init}} = 5$ V and $T_d = 500$ ms.

B. Failure of FG D-STDP
We applied D-STDP rule on FG synapse to the pre- and post-synaptic spike pairs as done in [11]. For obtaining the measurement results in Fig. 6, we set the voltage and timing parameters as given in Fig. 4(b) i.e, same as mentioned in subsection IV-A.

1) FG D-STDP fail to reproduce frequency effects: For obtaining measurement results, we have set $\Delta t = \pm 5$ ms as shown in Fig. 4(c). The measurement results are plotted as weight change in D-STDP rule as a function of frequency, $\rho$. The measurement results (red lines) shown in Fig. 4(d), almost follows the mathematical D-STDP model (blue lines) in [11]. As mentioned in [11], this can be attributed to the following reasons. First, As pointed out in [32], at low repetition frequency, $\rho$, there is no potentiation. This cannot be captured by FG D-STDP, because pulsed drain voltage waveform, $V_d$ at the occurrence of a post-synaptic spike after a pre-synaptic spike by few milliseconds induces LTD. Second, In experiments, for $\Delta t > 0$, potentiation increases when frequency increases. This trend can also not be reproduced by FG D-STDP. In D-STDP model, as soon as the frequency increases, the pre-post spike pairs approach each other and the post-synaptic spike of the first spike pair interact with the pre-synaptic spike of the subsequent spike pair. With increase in frequency, the post-pre spike interaction increases and therefore depress the synapse, which is not observed in experiments.

2) FG D-STDP fail to reproduce triplet experiments: In triplet experiments, as shown in Fig. 6(a) and (b), there is a clear asymmetry between two protocols mentioned (black bars). 60 repetitions of pre-post-pre triplet yields less weight change, whereas 60 repetitions of post-pre-post triplet yields a weight change of $\sim 30\%$ (black bars). However, FG D-STDP shown in red bars, predicts almost same result for both protocols, because the mechanism of potentiation and depression happening due to the generation of different voltage changes.
waves at pre- or post-synaptic spikes are similar in both protocols. Therefore, triplet results cannot be explained by a sum of pre-post injection mechanism and a post-pre tunneling mechanism.

3) FG D-STDP fail to reproduce quadruplet experiments: The asymmetry present in the quadruplet experiments, as shown in Fig. 6(c), also causes some problem for FG D-STDP. A quadruplet consists of a pre-post-pre sequence where, T<0 or a post-pre-pre-post sequence where, T>0 as shown in Fig. 3(c). Here, [T] denotes the interval between the first and last pair of spikes within the quadruplet. Sequence, pre-post-pre consists of two pre-post interactions and a post-pre interaction whereas, for the sequence, post-pre-pre-post, the opposite occurs i.e two post-pre interactions and only one pre-post interaction. This clearly leads to an asymmetry which is not seen in experiments [11].

C. Success of FG T-STDP

FG T-STDP is implemented with the help of a drain voltage waveform generator, explained in next section. As mentioned in the previous section, the mathematical analysis provides an intuitive understanding of utilization of $V_d$ pulse waveform to obtain the extra triplet term in the T-STDP rule (equation 2). As the extra triplet term can be achieved with the two cases of proposed pulse drain voltage waveform, here, we have shown measurement results for both the cases of $V_d$ waveform. The measurement results obtained for both the case of drain voltage waveform satisfy the behavior seen in experimental results [11]. The timing specifications for frequency effects of pairing protocol, triplets of spike and quadruplets are shown in Fig. 4(c).

1) FG T-STDP can reproduce triplet and quadruplet experiments: T-STDP model on floating gate synapse does not only reproduce the learning window (Fig. 5), but also it can reproduce most of the triplet and quadruplet experiments as shown in Fig. 7(a), (b) and (c) and Fig. 8(a), (b) and (c). The voltage and timing parameters for the case of single-pulsed drain voltage waveform are also same as in the case of protocol 1 and less potentiation in the case of protocol 2. The blue bars shows the result of the mathematical model in [11]. The quadruplet measurement results also replicate the symmetry seen in the experimental results [11].

2) FG T-STDP model can reproduce frequency effects: FG T-STDP model (red bars) cannot replicate the experimental results shown in black bars. (c) FG D-STDP fails to reproduce quadruplet experiments. (d) Weight change in FG D-STDP rule as a function of frequency, $r \times \rho$. Note that, thick line correspond to $\Delta t = 5$ms and dash line correspond to $\Delta t = -5$ms.
Protocol 1: Pre−Post−Pre

\[
\Delta \frac{w}{w} (|\Delta t_1|/r, \Delta t_3/r) \text{(ms)}
\]

Experimental
T−STDP
FG T−STDP

(a)

Protocol 2: Post−Pre−Post

\[
\Delta \frac{w}{w} (\Delta t_1/r, \Delta t_2/r) \text{(ms)}
\]

Experimental
T−STDP
FG T−STDP

(b)

Fig. 7: FG T-STDP using single-pulsed drain waveform: In all four subgraphs, black bars denote experimental data (taken from [11]), blue bars and lines, mentioned as T-STDP correspond to Nearest-Spike minimal triplet model proposed in [11] and red lines correspond to measurement results. (a) The bar graphs shows the comparison of results obtained from FG T-STDP (red) with the biological experimental results (black) and mathematical model (blue) for T-STDP protocol 1:Pre-Post-Pre (|\Delta t_1|/r, \Delta t_3/r). Similar to (a), results for T-STDP protocol 2:Post-Pre-Post (\Delta t_1/r, \Delta t_2/r) is shown in (b). FG T-STDP (red bars) can replicate the experimental results shown in black bars. (c) FG T-STDP can also reproduce quadruplet experiments. (d) Weight change in T-STDP rule as a function of frequency, \( r \times \rho \). FG T-STDP can reproduce frequency effects compared to FG D-STDP. Note that, thick line correspond to \( \Delta t = 5 \text{ms} \) and dash line correspond to \( \Delta t = -5 \text{ms} \).

Fig. 8: FG T-STDP using double-pulsed drain waveform: In all four subgraphs, black bars denote experimental data (taken from [11]), blue bars and lines, mentioned as T-STDP correspond to Nearest-Spike minimal triplet model proposed in [11] and red lines correspond to measurement results. (a) The bar graphs shows the comparison of results obtained from FG T-STDP (red) with the biological experimental results (black) and mathematical model (blue) for T-STDP protocol 1:Pre-Post-Pre (|\Delta t_1|/r, \Delta t_3/r). Similar to (a), results for T-STDP protocol 2:Post-Pre-Post (\Delta t_1/r, \Delta t_2/r) is shown in (b). FG T-STDP (red bars) can replicate the experimental results shown in black bars. (c) FG T-STDP can also reproduce quadruplet experiments. (d) Weight change in T-STDP rule as a function of frequency, \( r \times \rho \). FG T-STDP can reproduce frequency effects compared to FG D-STDP. Note that, thick line correspond to \( \Delta t = 5 \text{ms} \) and dash line correspond to \( \Delta t = -5 \text{ms} \).
double pulse. The voltage and timing parameters for the case of single-pulsed drain voltage waveform are also same as mentioned in subsection IV-A, but with a difference of \( V \) and \( d \) in Fig. 7(a), and in Fig. 8(d)). This is because the single pulse at the first post-synaptic spike itself is enough to generate some injection.

V. DRAIN VOLTAGE GENERATOR: VLSI IMPLEMENTATION

The drain voltage waveform generator is the important block for generating the voltage pulses according to spike timing as shown in Fig. 3. The input to the generator is a post-synaptic pulse from a neuron as shown in Fig. 4. The output pulse from the generator is fed back to the drain terminal of FG synapse. The number of drain waveform generator in a system depends on the number of neurons present in that neural network architecture. We propose circuits for single- and double-pulsed drain voltage waveform generator below along with their SPICE simulation results.

A. VLSI implementation of single-pulsed drain voltage waveform

From equation (28), we need to create an exponentially decaying voltage trace for \( \Delta V_d^c(\Delta t_2) \) for large values of \( \Delta t_2 \). Also, \( V_{d_{\text{min}}} \) is the default value of \( V_d \) when there is no post synaptic pulse for a long time \( (\Delta t_2 \to \infty) \). In order to create the exponential voltage trace, we can use a capacitor, \( C \) and a switched capacitor resistor, \( R_{sc} \), where the capacitor charges from the lowest voltage, \( V_{d_{\text{min}}} - \Delta V_{d_{\text{max}}} \) to \( V_{d_{\text{min}}} \) through the resistor (Fig. 10(a)). Here, \( \Delta V_{d_{\text{max}}} \) is given by the equation (29), where \( \Delta t_2 \to 0 \). The operation of the circuit is as follows: at every post-synaptic pulse denoted as CLK in Fig. 10(a), the voltage across the capacitor \( V_c \) is sampled as \( V_d \) through the multiplexer. At other times, the multiplexer enforces \( V_d = V_{d_{\text{init}}} \). A delayed pulse \( \text{CLK}_d \) is also generated after the clock pulse such that it does not overlap with CLK. At this pulse, \( V_c \) is pulled down to \( V_{d_{\text{min}}} - \Delta V_{d_{\text{max}}} \). After this, \( V_c \) decays back to \( V_{d_{\text{min}}} \) by discharging through the resistor \( R_{sc} \). The decay constant of this circuit is set by the parameter \( \tau_y \) in the equation (29).

B. VLSI implementation of double-pulsed drain voltage waveform

Fig. 9(b) shows the circuit implementation of double-pulsed drain voltage waveform according to equations (29) and (19). The circuit operation is exactly similar to single pulsed drain waveform generator except that \( \Delta V_d^c(\Delta t_2) \) is linearly dependent on \( \Delta t_2 \). Hence, the resistor is replaced with a current source, \( I_p \). Since, we need to create double pulse, an extra clock is used here. CLK1 is to create the first pulse, during which \( V_d = V_{d_{\text{min}}} \) and CLK2 is to sample the voltage, \( V_c \) across capacitor, \( C \) on to the output node, \( V_d \) in order to create
Fig. 10: SPICE Simulation results: (a) The simulation result of the single-pulsed drain voltage waveform circuit. The result shows the variation of $\Delta V_d^I(\Delta t_2)$ with respect to $\Delta t_2$. The ideal MatLab simulation result is also included for comparison. (d) The simulation result of the double-pulsed drain voltage waveform circuit.

the second pulse. Whenever there is no post-synaptic spike, $V_d$ is held at $V_{d,init}$ through the switch controlled by NOR of CLK1 and CLK2. For deciding the value of $I_p$; simplifying equation (28), we get:

$$\Delta V_d^I(\Delta t_2) = V_{inj} \ln\left(\frac{A^+_d}{A^+_2}\right) - V_{inj} \frac{\Delta t_2}{\tau_y}$$

(32)

also from capacitor charging,

$$C \frac{dV}{dt} = I_p$$

(33)

Thus equating both the slopes of equations (32) and (33), we get:

$$I_p = \frac{V_{inj}}{\tau_y}$$

(34)

Hence, $I_p = -5.2$ pA for $\tau_y = 48$ ms and $V_{inj} = 0.25$V. The simulation result of $\Delta V_d^I(\Delta t_2)$ obtained from the VLSI circuit is shown in Fig. 10(b) with comparison to the ideal MATLAB plots. For simulation results, we have used $C = 1\text{pF}$, $V_{d,init} = 0.3V$, $V_{d,max} = 5V$ and $\Delta V_d^I = 125mV$ for $A^+_d = 9.1 \times 10^{-3}$ and $A^+_2 = 4.6 \times 10^{-3}$. It is easily seen that there is a much better match between the circuit and MATLAB simulation in this case due to the simpler functional form of $\Delta V_d^I$.

VI. DISCUSSION

An important consideration for synapse designs is scalability to large arrays. Figure 11 shows the system level architecture of a neuromorphic hardware device with $N$ neurons, $M$ inputs and $M \times N$ synapses (number of synapses outnumbered compared to number of neurons). It shows the connection between FG synapses and neurons and gives an idea about the number of different voltage waveform generators to be used for generating the terminal voltages for the FG synapse shown in Fig. 3. Here, for the entire system shown, we need only $N$ drain voltage, $N$ tunnel voltage and $M$ gate voltage waveform generators. Thus the synaptic area overhead compared to earlier implementations [23] is only the added multiplexer for switching tunneling voltages.

Table I compares this work with other reported implementations of plastic synapses—a detailed review of these circuits can be found in [37]. It can be seen that our work is the first that combines high resolution non-volatile storage with sophisticated plasticity rules. The term normalized area is used to denote the ratio of the synapse area to the square of the process technology. It is a normalized metric to compare the size of a synapse circuit independent of process technology—smaller numbers refer to more compact designs. The floating-gate device used in our test chip is quite large. However, this is not a fundamental problem since we have earlier demonstrated STDP in much smaller floating-gate devices [23]—the only difference of this work with our earlier one is in terms of peripheral circuits to control drain and tunnel waveforms. Hence, after this proof of concept work, we can make a dedicated chip with floating-gates occupying $\approx 100\mu m^2$ area. Some emerging devices like memristors are also showing promise as a compact learning synapse [38] for spiking systems. Though we are not yet aware of reports of dense arrays of memristive STDP synapses integrated with CMOS neurons in hardware, this seems like a promising area in future when scaling of flash memory or floating gates become limited.

One of the important aspects of a circuit implementation of a learning rule is the ease with which its parameters can be tuned. We showed in Section III-B how the parameter $A^+_3$ can be tuned based on $\Delta V_d$. Other learning rule parameters are also directly related to parameters of the control voltage waveforms. For example, $\tau_+$ can be modified using $T_{y1}$, $\tau_-$
TABLE I: Comparison of Learning Synapses in VLSI

| Reference | Process technology (nm) | Synapse area (µm²) | Normalized Area | Weight storage (precision) | Plasticity rule | Chip measurement |
|-----------|-------------------------|-------------------|-----------------|---------------------------|-----------------|------------------|
| This paper | 350                     | 6337              | -               | Floating gate (> 10 bits) | T-STDP          | Yes              |
| [22]      | 350                     | -                 | -               | Capacitor (Analog)        | T-STDP          | No               |
| [23]      | 350                     | 133               | 1088            | Floating gate (> 10 bits) | STDP            | Yes              |
| [34]      | 350                     | 400               | 3265            | Capacitor (Analog)        | STDP            | Yes              |
| [30]      | 350                     | 100               | 816             | Floating gate (> 10 bits) | STDP            | Yes              |
| [35]      | 250                     | 5000              | 80000           | Capacitor (Analog)        | STDP            | Yes              |
| [20]      | 600                     | 72000             | 200000          | Capacitor (bistable)      | STDP            | Yes              |
| [18]      | 800                     | 4495              | 7023            | SRAM (1 bit)              | STDP            | Yes              |
| [17]      | 250                     | 238               | 3810            | SRAM (4 bits)             | STDP            | Yes              |
| [36]      | 180                     | 108               | 3338            | Capacitor (bistable)      | SDSP            | Yes              |
| [10]      | 350                     | 3000              | 24400           |                          |                 |                  |

*Normalized area is termed as the ratio of the synapse area to the square of the minimum transistor dimension in that process technology.

using $T_{\text{tun}}$ and $A_2^-$ using $T_{\text{tun, pulse}}$ and $V_{\text{tun, max}}$. This is evident from the mathematical analysis of section III. Similarly, from equation (27) and equation (28), $A_3^-$ and $\tau_d$ can be tuned using $\Delta V_d^2$ or $\Delta V_d^4$, keeping two of them constant at a time. Some results for the variation of learning window to different parameters can be seen in our previous paper [26]. Also, other minor changes to the learning rule can be done by modifying the circuits at the neuron and periphery that generate the gate, drain and tunnel waveforms.

After this proof of concept, we will continue the work by simulating a spiking neural network (SNN) using SPICE simulations to understand the difference between T-STDP and D-STDP learning rules and then extend our work in future by fabricating chips with thousands of neurons and millions of learning synapses to do tasks like rapid and robust pattern recognition [39], [40]. Such neuromorphic chips that incorporate noise and heterogeneity are useful to understand the principles used by our brain to compute using imprecise elements [41], [42] as well as for accelerated simulations of neural networks [19], [43]. Moreover, we hope to use neuromorphic systems as the “brain” for real-time behaving systems like robots [41] where both low-power dissipation and real-time operation are necessary. In these cases, using a traditional computer for the implementation is inefficient due to the mismatch between Von-Neumann computing model of digital computers and the massively parallel analog computing of the brain where memory and computing are closely intermixed [44]. Hence, it is useful to be able to mimic biological neural networks closely in circuits to enable experimental paradigms as well as low-power intelligence.

VII. CONCLUSION

We have presented a spike triplet based learning rule using a single FG transistor as the synapse for VLSI spiking neural networks. The spike triplet affects the setting of drain voltage—we presented a single pulse and a double pulse drain voltage method to obtain the desired dependence of weight on spike timing. We presented a method to calculate the parameters of the drain voltage pulse to obtain results matched to the original theoretical T-STDP rule. We also show FG measurement results in comparison with the biological experimental observations for (1) original doublet protocol, (2) two protocols of spike triplets, (3) frequency effects of pairing protocol and (4) quadruplet experiments. The failure of FG D-STDP rule in replicating the biological results is also included. Possible hardware implementations of drain voltage waveform generator are also proposed and verified through SPICE simulation results. It was shown that the voltage waveform for double pulse case can be generated more accurately due to its simplistic nature.

ACKNOWLEDGEMENT

Financial support from MOE through grant ARC 8/13 is acknowledged. The authors thank Prof. Jennifer Hasler for providing access to FG transistor.

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