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Frequency and voltage dependent electrical properties of YMn<sub>0.90</sub>O<sub>0.10</sub>O<sub>3</sub> thin film on the SiO<sub>2</sub>/p-Si substrate

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Abstract

The YMn<sub>0.90</sub>O<sub>0.10</sub>O<sub>3</sub> (YMDO) thin film was deposited on the SiO<sub>2</sub>/p-Si substrate via using radio frequency (rf) magnetron sputter method. Voltage dependent electrical properties of the Al/YMDO/SiO<sub>2</sub>/p-Si/Al structure were investigated at various frequency and ambient condition. Capacitance-voltage (C-V) measurements showed that the capacitance has an accumulation region at positive or forward bias region. Conductance-voltage (G-V) characteristics of the device displayed that the G increases with increasing frequency. Series resistance, \( R_s \), of the device was derived from C-V and G-V measurements and the \( R_s \)-V characteristic exhibited strongly frequency dependency. Frequency dependent interface state density, \( N_{ss} \), was calculated according to the Hill-Coleman relation, which decreases as frequency increases. The corrected capacitance (\( C_c \)) and conductance (\( G_c \)) results revealed that the effect of series resistance on the electrical properties cannot be ignored.

Introduction

Perovskite-oxide materials, which have ABO<sub>3</sub> stoichiometry, have great attention owing to their wide range application fields such as sensors [1], memory [2], spintronics [3], catalysis [4], and solid-oxide fuel cell [5] so on. The flexibility of changing their chemical structure by doping a foreign element to A or B site gives an important opportunity to researchers to study their electrical, magnetic, optical and mechanical properties [6–9]. The oxidation states and ionic radii of the doping elements have a key role on the crystal structure and electrical/dielectric, magnetic and optical properties of perovskite-oxide materials. Beside this, it has been reported that some of those materials have multi-ferroic properties which both ferroelectricity and ferromagnetic/antiferromagnetic properties takes place simultaneously in same phase, and they are considered for next generation nonvolatile memory, sensors and actuators, and electro-optic devices [10–14].

YMnO<sub>3</sub> (YMO), which is called as type-I multi-ferroic material, is an important member of perovskite-oxide family due to its physical and chemical features. Even though, YMO has hexagonal crystalline structure at room temperature, it holds orthorhombic crystalline phase at high temperatures. It has been reported that YMO has high Curie temperature (\( T_c \sim 900^\circ\text{C} \)) and low Neel temperature (\( T_N \sim 70 \text{K} \)) [15, 16]. Furthermore, it has been reported that the YMO has around 2 eV optical band gap and it can be reduced to lower values by doping in order to maximize light absorption [17]. It has been also documented that YMO is a good candidate material for sensing elements as changing oxidation states of Mn via doping a foreign element [18]. In our previous studies, we have illustrated that Os can be doped into Mn sites in YMO structure. Furthermore, we have exhibited that the electrical and optical features of YMO can be tuned by Os doping [17, 19, 20]. The osmium (Os) has +2, +3, +4, +6, and +8 oxidation states and such a different oxidation states provide an important opportunity to researchers in order to tune the such as electrical, magnetic, optical properties of the compounds.

It has been reported that the problems with the oxide layer/semiconductor interface originate from the dangling or unsaturated atomic bonds at the semiconductor substrate surface [21]. The process of the SiO<sub>2</sub> oxidation layer can be used to saturate the dangling bonds on the surface of semiconductor substrate [22]. Moreover, the SiO<sub>2</sub> oxidation layer can be thought as a top layer on the p-Si to protect its surface from the defects.
created during the YMnO₃ deposition [23]. Furthermore, some researchers have used ferroelectric thin films on SiO₂/Si substrate for fabrication of the devices [24, 25]. There are many advantages in the fabrication of such devices on silicon substrates for the saving electrical power and decreasing memory cell size. However, instead of extending the ferroelectric material directly onto Si substrate, SiO₂ layer or various buffer layers have been utilized to prevent the diffusion of ferroelectric material into silicon substrate [21–23, 26–28].

As mentioned before, the doping a foreign element into the YMO has a curial role on the electrical, optical and magnetic properties of undoped YMO compound. Furthermore, using an insulator layer between the semiconductor and Si substrate diminish the localized interface states near the Si substrate surface. In the light of those information, the present study is sequence of our previous investigations of Os substituted YMO thin films [27–29]. The aim of present study is to investigate electrical properties including capacitance-voltage (C-V), conductance-voltage (G-V) and series resistance-voltage (Rₛ-V) characteristics of Al/YMOO/SiO₂/p-Si/Al structure, which have not been examined in the literature yet. Therefore, the present investigation is the first study that is introducing such data into scientific community.

In this study, the Al/YMOO/SiO₂/p-Si/Al structure was fabricated and its electrical properties depending on both frequency and voltage were investigated. In order to grow the YMOO thin film, pre-prepared YMOO single sputter target was used. The YMoo thin film was deposited on the SiO₂/p-Si/Al substrate and then Al dots was deposited on the front surface as a rectifying contact. The capacitance, conductance and impedance measurements were performed depending on voltage at various frequencies at room temperature. The voltage and frequency dependent series resistance, the voltage dependent corrected capacitance and conductance and the frequency dependent interface states were extracted from the measured capacitance and conductance values.

**Experimental methods**

The Os doped YMO powder was synthesized using solid-state reaction method. The Y₂O₃ (A. AESAR, 99.99%), Mn₃O₄ (A. AESAR, 98%) and OsO₂ (A. AESAR, 83%) were used in order to synthesis desired compound. In order to obtain YMn₀.₉₀Os₀.₁₀O₃ stoichiometry, the OsO₂ (A. AESAR, 83%) was mixed as 10% mole with other starting powder materials. The used powders were mixed in an agate mortar using ethanol. After for a while the mixed compound was calcined at 900 °C for 10 hours in high temperature furnace (MTI) in ambient conditions. After first calcination process the obtained powder was reground for a while in an agate mortar and then sintered at 1200 °C for 12 h in the furnace in ambient condition. The desired compound was obtained after second calcination process and the powder was put a copper holder and pressed under 400 bars pressure in order to prepare sputter target. X-ray diffractometer (XRD), scanning electron microscope (SEM), energy-dispersive x-ray spectrum (EDX), x-ray photoelectron spectroscopy (XPS), Fourier transform infrared (FT-IR) absorption spectra analyses results of the synthesized powder can be found in our previous studies [19, 20]. In order to grow thin film of YMOO, the prepared sputter target used as a source target. The pre-cleaned SiO₂/p-Si substrate was used as device substrate. First, high purity (99,999%) aluminum (Al) was deposited to back side of SiO₂/p-Si substrate in order to form back electrode using VAKSIS thermal evaporator system. Second, SiO₂/p-Si/Al structure annealed at 500 °C for 5 min in inert ambient in order to form ohmic contact. YMOO thin film was deposited front side of SiO₂/p-Si/Al structure using radio frequency (rf) magnetron sputtering technique at 500 °C in 2–4 mTorr Ar gas pressure. The YMOO thin film thickness was obtained as 122 nm by using Dektak XT surface profilometer. The high purity (99,999%) aluminum (Al) was deposited to front side of YMOO/SiO₂/p-Si/Al structure in order to form front or rectifying electrode. Hence, our device was sandwiched between two Al electrodes as Al/YMOO/SiO₂/p-Si/Al structure. The electrical properties of Al/YMOO/SiO₂/p-Si/Al structure were conducted in ambient condition using HP 4192 A LF Impedance Analyzer. Optical band gap, XRD, SEM, XPS analyses of the YMOO were investigated in our previous study [17].

**Results and discussion**

The impact of Os doping on the electrical and optical properties of YMO compound were investigated in our previous studies [17, 19, 20, 29–31]. We reported that the Os substitution into the YMO decreases the optical band gap of YMO from 2.10 eV to 1.61 eV and the basic mechanisms of this phenomenon is related to electronegativity difference between the O anion and B cation (Mn and Os) element. It has been reported that the optical band gap of such perovskite-oxide materials is proportional to electronegativity difference between the O anion and B cation [17]. The XRD studies have laid down that YO peaks shift toward the lower two theta angles as the Os doping ratio is boosted [17]. More discussion can be seen in the reference 17. Furthermore, XPS analysis of YMOO compound showed that the Y has +3 oxidation state, Mn has both +3 and +4 oxidation states. Also, it has been observed that the Os doping into the YMO causes decreasing percentage of Mn +4 oxidation state. In the same study [17], the oxidation state of Os was determined as 0, which means Os is
metallic. Furthermore, it has been realized that Os substitution into Mn sites leads to generation of oxygen deficiency in the material [17, 28]. Moreover, the current-voltage (I-V) characteristics of the Os doping to YMO compounds have been published elsewhere [17, 20, 29–31].

Figure 1(a) shows the SEM image of YMOO thin film. It can be seen from the image that the thin film surface is highly smooth and any crack is not observed on the film surface. Crack free surface is important to obtain reliable electrical characteristics. Figure 1(b) shows the EDX analysis result of the YMOO thin film with the atomic percentages (inside fig). It is seen from the spectrum that the Os peak overlapped with Y, and the EDX detection confirmed that the YMO thin film compound consists the Os element. (The Si peak coming from the Si substrate).

Schematic illustration of the studied device is given in figure 2(a). The energy-band diagrams of Al/YMOO/SiO2/p-Si/Al device are illustrated before and after junction in figures 2(b) and (c) [17, 31, 32]. Where X is electron affinity, $E_g$ is the energy gap, $E_{vac}$ refers vacuum level, $E_c$, $E_v$, and $E_f$ are the conduction band minimum, valance band maximum and Fermi energy level, respectively [17, 29].
Capacitance-voltage (C-V) plot of the Al/YMOO/SiO2/p-Si/Al structure with various frequencies at room temperature is given in figure 3. As can be noted from the figure, the accumulation region formed near the SiO2/p-Si interface in the forward bias that p-Si/Al side was positively biased; and the p-Si/Al side was negatively biased in reverse bias. The YMOO/SiO2/p-Si layer at Al/Al interface affects in forward or reverse bias capacitance measurements. Step-like C-V curves gradually decrease with boosting frequency. This can be attributed to the lack of time for reorientation of charge at interface states/traps [33]. The interface state charges can follow the external ac field at lower frequency, but cannot follow at higher frequency [33]. Hence, the increasing frequency causes decreasing capacitance of the device. In strong accumulation region, the capacitance is almost constant and voltage is independent from the frequency. These obtained C-V curves are similar to curves for previously reported MOS and metal/ferroelectric material thin film layer/Si/metal structures [30, 34]. Through the lower voltage values in positive bias, the capacitance decreases sharply, which is called depletion region, then reaches a constant value in negative bias region, and this section is inversion region. The majority carriers start to realp at the SiO2/p-Si interface at lower positive bias and they almost completely realp in negative bias. Similar C-V characteristics were obtained by Yoo et al [35]. They fabricated bi-layered of YMnO3 thin film on the bare Si substrate and studied its stress-related crystallization evaluation and memory properties. They reported that bi-layered of YMnO3 thin film showed typical step-like capacitance. This value is lower than the capacitance value obtained by the present study and this can be attributed to higher dielectric constant of YMOO compound. In our previous study, we reported the Os doping into the YMO compound increases the dielectric constant of parent compound [19]. Such advancement in the dielectric constant might be associated to (i) the doping Os creates oxygen vacancies and they may increase the polarizability in the compound and (ii) Os substitution into the YMO structure enlarges the lattice parameters of YMO. As a result of that the Mn (Os)-O bond lengths extend, which might advance the atomic polarizability and finally increase the dielectric constant [19]. Our FTIR studies have revealed that Os substitution increases intensity of absorption peaks, which was attributed to the variation in dipole moments during the vibration. Consequently, vibrations produce large differences in dipole, which increases absorption, i.e. the greater the dipole, the more intense the absorption [19].

The conductance-voltage (G-V) plot of the device with various frequencies at room temperature is presented in figure 4. It is clear that the conductance has higher value in accumulation region, yet, it holds lower value in inversion region. Furthermore, the conductance rises with advancing the frequency values and this is due to the increasing charge mobility or decreasing series resistance with increasing frequency [36]. The conductance increases in the depletion region due to initiation of charge accumulation near the interface. The conductance curves in the transition region (the depletion region to inversion region) has a linear portion and the slope of those portions rises depending on frequency. At 100 kHz, a highly sharp slope takes place, and this can be attributed to increasing charge mobility due to increasing frequency. Moreover, our previous study presented the Os doping into the YMO compound increases its conductivity due to increasing oxygen vacancies in the compound. YMO is a p-type material and it has been shown the Os doping creates oxygen vacancies (or holes) into the compound [19]. Hence, those vacancies contribute the p-type conductivity in the material. The conductance has a maximum value in positive/forward bias or accumulation region and it reduces slowly with increasing potential in accumulation region. Moreover, those maximum values shift through higher positive bias and this can be associated to interface states (Nst). Karataş et al [37] obtained a similar behavior for Sn/p-Si
structure and they attributed this behavior to interface states. Ozmen et al.\[38\] fabricated Al/p-Si/Y1−xSrₓMnO₃/Al structures and investigated their electrical and photoresponse properties. They reported that the conductance of the fabricated devices has 10⁻³ (S) magnitude, which is higher than the present device. This may be ascribed to the presence of SiO₂ insulating layer in the studied device.

The presence of serial resistance \(R_s\) and interface states \(N_{ss}\) mainly causes a deviation in the \(C-V\) characteristic. Hence, the determination of those parameters is curial for the thin film electronic devices. The relation between the capacitance, conductance and serial resistance can be defined as below [34]:

\[
R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2}
\]

where \(G_{ma}\) and \(C_{ma}\) are the maximum conductance and capacitance values in strong accumulation region from \(C-V\) and \(G-V\) measurements. Using equation (1), it can be calculated two different \(R_s\) values: first voltage dependent and second frequency dependent. The voltage dependent \(R_s\) plot \((R_s-V)\) for each frequency value at room temperature is shown in figure 5. It can be noted from this figure, the \(R_s\) has a peak at certain potential values for each frequency. The \(R_s\) drops down between −4 V and 0 V, and then goes up between 0 V and 3 V and finally decreases between 3 V and 10 V again. Moreover, the same figure reveals that the \(R_s\) has a peak around 3 V for all frequency values. Those peaks move to higher positive values with increasing frequency and this is because of the presence of the \(N_{ss}\) at the metal/insulator interface [34,39−42]. The \(R_s\) falls with increasing frequency due to increasing charge carrier mobility or conductivity. This behavior is highly close to the Al/BiFeO₃/p-Si/Al structure [43] in which the researchers reported that the \(R_s\) has a peak with around \(1.3 \times 10^4 \Omega\) at −0.45 V. The frequency dependent \(R_s\) plot \((R_s-f)\) calculated from the equation (1) using the maximum values of \(C\) and \(G\) in the strong accumulation region for each frequency at 10 V, is given in figure 6 and it can be noticed that the \(R_s\)
strongly depends on the frequency at given potential value. The $R_s$ sharply decreases with escalating frequency owing to the increasing charge carrier mobility or conductivity. For example it has $7 \times 10^3 \ \Omega$ in 2 kHz and is around $1 \times 10^3 \ \Omega$ in 30 kHz. Those results showed that our device has lower series resistance values compare to the Al/PTCDA/p-Si structure [44]. The $R_s$ relatively surges a little bit in higher frequency (between 40 kHz-100 kHz) with increasing frequency. This can be attributed to the presence of the localized interface states between the SiO$_2$/p-Si interfaces.

Figure 6 displays the frequency dependent $R_s$ plot of the device.

Figure 7 displays the total impedance ($Z$) versus bias voltage plot for each frequency value. It can be noticed from the figure; the $Z$ has higher resistance value in reverse bias region than that in the forward bias region for each frequency. Furthermore, it is clear that the increasing frequency causes decreasing of the $Z$ for both reverse and forward region. This is due to the boosting charge carrier mobility and consequently increasing conductivity. Furthermore, there is an inverse proportionality between the $Z$ and frequency because the charge carrier mobility or conductivity rises with increasing frequency. In forward bias region, all majority carriers accumulate near the SiO$_2$/Si interface so the resistance value of the device will decrease. In reverse bias case, the accumulated majority carriers will be repelled from the mentioned interface so the resistance of the device will go up. The step like transition between the inversion and accumulation regions is owing to the depletion region. It can be said that the transition point from the inversion region to accumulation region shifts through the higher positive voltage values with frequency. For example, the transition point for 2 kHz is near 1 V but the point for the 100 kHz is around 3 V.

The presence of $R_s$ in the MOS devices and its effect on the both capacitance and conductance leads a serious error, so a correction is needed for those two parameters. The corrected capacitance ($C_C$) and conductance ($G_C$)
relationships taking account the $R_s$ can be written as follow [34]:

\[
C_C = \frac{G_m^2 + (\omega C_m)^2}{(\omega C_m)^2 + a^2} \quad (2)
\]

\[
G_C = \frac{G_m^2 + (\omega C_m)^2}{(\omega C_m)^2 + a^2} \quad (3)
\]

where $a = G_m - [G_m^2 + (\omega C_m)^2] R_s$, $C_m$ and $G_m$ are the measured capacitance and conductance of the device at each frequency given in figures 3 and 4. The corrected capacitance and conductance plots depend on voltage and are presented in figures 8 and 9. The series resistance effect can be clearly seen in figure 10. For example, the $C_C$ has $2.72 \times 10^{-10}$ F whereas $C_m$ has $2.42 \times 10^{-10}$ F, and the $G_C$ has $1 \times 10^{-7}$ s while the $G_m$ has $5.43 \times 10^{-5}$ s at 10 volts. It is noticed from those values that the conductance is much more sensitive than the capacitance due to the series resistance presence [33–36, 39–42]. Those differences can be clearly seen from the corrected and measured capacitance and conductance comparison in the figure 10.

A distinct peak is observed in $G_C$ plots in figure 9 whereas this peak is not much clear like $G_m$ peak in $G_m$ plot in figure 4. This indicates that the $R_s$ produced the dominant loss and prevent interface trap loss [33, 34, 39–42]. Additionally, the $R_s$ has a net impact on the capacitance as can be seen from the figure 8 as compare with the measured capacitance given in figure 3. The error for accumulation region is higher than the depletion and inversion regions and it is noticed from the figure 10(a). These results revealed from the fact that the $R_s$ cannot be ignored in every case for device characterization. Similar behaviors have been observed by other researchers [39–47].

The interface states ($N_{ss}$) definition can be written according to the Hill-Coleman method [47] and it is given as follow:
where $C_m$ and $G_m/w$ are the measured or experimental capacitance and conductance peak values at each frequency. The oxide layer capacitance, $C_{ox}$, can be derived from the $C$ and $G/w$ plots at strong accumulation region for each frequency and it is written below [34]:

$$C_{ox} = C_{ma} \left[ 1 + \left( \frac{G_{ma}}{\omega C_{ma}} \right)^2 \right]$$

As mentioned before, the purpose from SiO$_2$ oxidation layer process is to saturate the dangling bonds on the surface of $p$-Si semiconductor substrate. Therefore, the obtained interface states density is that of the SiO$_2$/$p$-Si interface and is related to that interface. Frequency dependent the $N_{ss}$ plot is presented in figure 11 and it can be seen that the $N_{ss}$ depends strongly on the frequency. As can be seen from the figure 11, the $N_{ss}$ increases with decreasing frequency because it can follow the ac signal and contributes capacitance values in low frequencies. It can be clearly from the figure 3 that the capacitance has higher value in lower frequency than that in the higher frequencies. Hence, this confirms that the high capacitance in lower frequencies can be attributed to excess capacitance resulting from the $N_{ss}$ values [34–36, 39–42, 45–47]. The obtained $N_{ss}$ originates from the SiO$_2$/$p$-Si interface during the electrical characterization. The order of magnitude of the $N_{ss}$ is in highly close agreement with those obtained for Al/Coumarin:ZnO/$p$-Si/Al [48], BiFeO$_3$ MOS capacitor [49] and Al/SiO$_2$/$p$-Si [50]. Also, the following reasons can also be important role on the $N_{ss}$: (i) the presence of SiO$_2$ layer between the YMnO$_3$ and $p$-Si has important role on the $N_{ss}$. The process of the SiO$_2$ oxidation layer can be used to saturate the dangling bonds on the surface of semiconductor substrate. Moreover, the SiO$_2$ oxidation layer can be thought as a top layer on the $p$-Si to protect $p$-Si surface from the defects caused by the YMnO$_3$ deposited via the magnetron DC sputter technique to the $p$-Si surface. (ii) The crystal distortion and oxygen vacancies/defects formation due to doping Os into the YM compound may play an important role as trap centers. Thereby, during the electrical characterization, the charge carriers can be trapped by the lattice distortion and vacancies in the compound.
Conclusion

The YMOO thin film has been grown on the SiO2/p-Si/Al with Al ohmic back contact, and the Al/YMOO/SiO2/p-Si/Al structure was fabricated. Frequency and voltage dependent electrical characterization of the obtained device was investigated under ambient conditions. The C-V characteristics of the structure showed accumulation, depletion and inversion regions with respect to the applied electrical ac signal. The capacitance has maximum value in the accumulation region or forward biased for positive voltage values and it has minimum values in inversion region or reverse bias for negative voltage values. Furthermore, the capacitance decreases with increasing frequency values. The conductance plots revealed that it increases with increasing frequency owing to increasing charge carrier mobility or conductivity. Furthermore, the conductance showed sharper transition from the inversion to accumulation at higher frequency values. The calculated series resistance first decreased then increased and reached a maximum value then decreased with increasing frequency value. The maximum peak shifted positive voltage values due to the interface states. The corrected capacitance and conductance plots showed that the series resistance has a key role on those two parameters, so it cannot be ignored for thin film based devices. Finally, the interface states increased with decreasing frequency because it can follow the ac signal at low frequencies.

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Conflict of interest

The author declare that he has no conflict of interest.

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