Practical Detectability for Persistent Lock-Free Data Structures

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ABSTRACT

Persistent memory (PM) is an emerging class of storage technology that combines the benefits of DRAM and SSD. This characteristic inspires research on persistent objects in PM with fine-grained concurrency control. Among such objects, persistent lock-free data structures (DSs) are particularly interesting thanks to their efficiency and scalability. One of the most widely used correctness criteria for persistent lock-free DSs is durable linearizability (Izraelevitz et al., DISC 2016). However, durable linearizability is insufficient to use persistent DSs for fault-tolerant systems requiring exactly-once semantics for storage systems, because we may not be able to detect whether an operation is performed when a crash occurs.

We present a practical programming framework for persistent lock-free DSs with detectability. In contrast to the prior work on such DSs, our framework supports (1) primitive detectable operations such as space-efficient compare-and-swap, insertion, and deletion; (2) systematic transformation of lock-free DSs in DRAM into those in PM requiring modest efforts; (3) comparable performance with non-detectable DSs by DRAM scratchpad optimization; and (4) recovery from both full system and thread crashes. The key idea is memento objects serving as a lightweight, precise, and per-thread checkpoints in PM. As a case study, we implement lock-free and combining queues and hash tables with detectability that outperform (and perform comparably) the state-of-the-art DSs with (and without, respectively) detectability.

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The source code, data, and/or other artifacts have been made available at https://cp.kaist.ac.kr/memento.

1 INTRODUCTION

Persistent memory (PM) is an emerging class of storage technology that simultaneously provides (1) low latency, high throughput, and fine-grained data transfer unit as DRAM does; and (2) durability and high capacity as SSD does. Compared with DRAM, Intel Optane DC Persistent memory module (DCPMM) [32] has $3 \times$ and similar latency for read and write; $1/3$ and $1/6$ bandwidth for read and write [35]; and up to $4 \times$ capacity for a single DIMM slot. Thanks to these characteristics, PM has a great potential for optimizing traditional and distributed file systems [14, 36, 37, 39, 59, 61], transaction processing systems for high-velocity real-time data [44], distributed stream processing systems [54], and stateful applications organized as a pipeline of cloud serverless functions interacting with cloud storage systems [51, 60].

A key ingredient of such optimization is persistent lock-free data structures (DSs), which provide the following advantages over lock- and transaction-based ones. First, they significantly outperform lock- and transaction-based DSs, especially in the presence of contention [20], by allowing multiple threads to process queries in parallel just as in DRAM. For instance, lock-free FIFO queues significantly outperform lock- and transaction-protected ones, as we will see in §7. Second, lock-free algorithms ensure that DSs are always in a consistent state so that we do not need additional logging to ensure crash consistency, as far as the writes to DSs are flushed to PM in a timely manner. For these reasons, persistent lock-free DSs have drawn significant attention in the literature. On the one hand, several such DSs as stacks [8], queues [24], lists [8, 63], hash tables [15, 47, 63], and trees [8], have been proposed. On the other hand, several general transformations from lock-free DSs in DRAM into persistent DSs in PM have been proposed [23, 25, 34, 40].

One of the most widely accepted correctness criteria for persistent lock-free DSs is durable linearizability [34]. For lock-free DSs in DRAM, an operation’s execution is modeled as an interval between its invocation and response events, and a thread’s execution is modeled as a series of consecutive invocation and response events of its operations. Then an execution of multiple threads are called linearizable if all operations result in outputs as if each of them atomically takes effect at some point, called the linearization point, between its invocation and response [28]. Now for lock-free persistent DSs in PM, an execution possibly across multiple crashes is called durably linearizable if it is linearizable when ignoring the crash events. In particular, operations finished before a crash should be persisted across the crash (durability), and even if some operations are interrupted in the middle by a crash, the DS should be recovered to a consistent state right after the crash (consistency). Finally, a persistent lock-free DS is durably linearizable if so are all its executions [34]. Durable linearizability is indeed satisfied by most existing persistent lock-free DSs, except for those DSs that intentionally break the property in order to trade durability for performance [24].

We argue that durable linearizability, while being widely accepted, is generally insufficient to use persistent lock-free DSs for transaction processing. Durable linearizability does not tell about detectability, or in other words, when an operation is interrupted in the middle by a crash, whether it is finished or not [9, 10, 24, 42]. The lack of detectability—while ensuring the DS’s own consistency—may break the enclosing system’s consistency in case of crashes.
Figure 1 illustrates a transaction processing system utilizing a persistent lock-free DS for high-velocity real-time data [44, 58]. In such a system, a component DS consumes and produces a stream of inputs and outputs, respectively [54]. Suppose the DS is not detectable. Should the system crashes, we cannot detect whether the input being processed just before the crash, say $i_2$, is finished, possibly incurring an inconsistency between the DS and the rest of the system and thus unrecoverable errors. For instance, if the system were a banking system and the DS were a key-value store recording the amount of balance for each person, a crash in the middle of a deposit operation may lose a person’s balance forever; for another instance, if the system were a distributed file system and the DS were a log, a storage node’s crash may silently ignore an ongoing operation, incurring inconsistency across the nodes.

Challenges. Several detectable persistent lock-free DSs have been proposed in the literature [9, 10, 24, 42, 50], but to the best of our knowledge, all of them suffer from at least one of the following limitations:

- High design cost: The prior works present several such persistent lock-free DSs, but many of them are hand-tuned and are manually reasoned to ensure crash consistency and detectability: Friedman et al. [24] and Li et al. [42] present detectable persistent lock-free queues, and Rusanovsky et al. [50] and Fatourou et al. [21] present detectable persistent combining DSs. Attiya et al. [9] present detectable compare-and-swap (CAS) for PM location as a general primitive operation for pointer-based DSs, but its applicability to lock-free DSs have not been demonstrated. Ben-David et al. [10] presents a transformation based on detectable CAS from lock-free DSs in DRAM into those in PM with detectability, but it requires code to follow specific patterns such as the normalized form [52]; and sizable restructuring of code by inserting persistency boundaries and explicit recovery codes.

- High runtime overhead: Detectability generally incurs runtime overhead. While the overhead is modest for hand-tuned persistent DSs [24, 42, 50], it is significant for the general transformation in [10] for two reasons. First, an object supporting detectable CAS consumes $O(P)$ space in PM where $P$ is the number of threads, prohibiting its use for space-efficient DSs such as hash tables and trees. (More severely, Attiya et al. [9]’s detectable CAS object consumes $O(P^2)$ space in PM.) Second, the transformation needs to checkpoint in PM stack variables for each CAS unless it is optimized for normalized DSs [52].

- Unsafe memory reclamation: Friedman et al. [24] use hazard pointers [45], and Li et al. [42] and (nb)Montage [12, 57] use epoch-based reclamation [22] for reclaiming PM locations, but its technical details are not sufficiently discussed in the papers. Attiya et al. [9], Ben-David et al. [10], and Rusanovsky et al. [50] Other prior works on (detectable or non-detectable) persistent lock-free DSs in PM [9, 10, 50] do not discuss safe memory reclamation. We argue that reclamation for PM is extremely subtle and deserves more attention. First, we discover that the queues in [24, 42] may incur use-after-free in case of crashes due to a lack of flush. Second, a straightforward application of reclamation schemes to PM may incur double-free in case of thread crashes.

Contributions and Outline. In this work, we present a programming framework for persistent lock-free DSs with detectability in PM that overcomes the above limitations. Specifically, we make the following contributions:

- In §2, we propose a model of detectable operations supporting systematic and efficient composition with end-to-end exactly-_once semantics. The key idea is persisting not only DS but also per-thread, timestamp-based memento objects serving as a precise, lightweight, and mostly thread-local checkpoints for the corresponding thread’s ongoing operation on the DS.

- In §3, we design an atomic pointer location object supporting efficient detectable CAS consuming $O(1)$ space in PM. Our CAS object is based on those of Attiya et al. [9] and Ben-David et al. [10], which utilize per-object array of $O(P^3)$ and $O(P)$ sequence numbers, respectively. We reduce the space complexity by instead utilizing global arrays of $O(P)$ timestamps.

- In §4, we design detectable insertion and deletion operations. While CAS is a general primitive operation for pointer-based DSs, we observe CAS-based detectable DSs are sometimes significantly slower than hand-tuned detectable DSs due to the increased contention on the CAS location. As an optimization, we design a more efficient (and less general) detectable insertion and deletion operations by capturing the essence of the hand-tuned detectable DSs presented in [24, 42].

- In §5, we propose a guideline for optimizing detectable DSs with DRAM scratchpad while preserving detectability. By DRAM scratchpad we mean putting a part of persistent DSs in DRAM. Such an optimization is pioneered in SOFT [63] and Mirror [25] that replicate PM contents in DRAM for higher performance, but it is neither supported by our composition (§2) nor explicitly recognized and exploited for detectable DSs in the literature. We explain how to add a DRAM scratchpad to a detectable DS while preserving its detectability.

- In §6, we propose correctness criteria for safe memory reclamation of lock-free DSs in PM. We explain a use-after-free bug in [24, 42] and two potential errors when reclamation schemes are straightforwardly applied in case of thread crashes. We fix the bug and prevent the errors by generalizing reclamation schemes and clearing mementos.

- In §7, we implement and evaluate detectable persistent lock-free DSs on Intel Optane DCPMM. We implement detectable versions of MSQ, combining queue, Treiber’s stack [13], exchanger [], elimination stack [27], Clever hash table [15], and SOFT hash table [63] based on mementos. Our MSQ outperforms the existing persistent MSQs with and without detectability; and our combining queue, Clever, and SOFT performs comparably with (and incurs a slight overhead over) the existing persistent DSs.
We design detectable persistent lock-free DSs in PM using per-thread mementos. To summarize, we present the first programming framework for detectable persistent lock-free DSs with low design cost, modest runtime overhead, and safe memory reclamation at the same time. Our implementation and evaluation result are available as supplementary material and they will be open-sourced after review.

2 DESIGN OF DETECTABLE OPERATIONS

2.1 Overview

We design detectable persistent lock-free DSs in PM using per-thread mementos. Figure 2 illustrates an example object O in PM that is concurrently accessed by threads T1 and T2. Suppose O is a queue and T1 and T2 are performing enqueue and dequeue operations, respectively. We require O’s operations receive—in addition to ordinary arguments such as the value to enqueue—a reference to memento stored in PM that is used to checkpoint the operation’s progress. Each memento supports a specific type of operations, e.g., the mementos C1 and C2 for T1 and T2 support enqueue and dequeue operations, respectively. The given memento records how far the operation had made the progress. In particular, once an operation is finished, the given memento records the operation’s output so that it can later be retrieved.

Even when interrupted in the middle by crashes, a thread still ensures its operation’s exactly-once semantics by detecting the progress it has made from the memento. Specifically, should the system or a thread crash, a crashed thread simply re-executes its operation and then it will automatically (1) detect the progress it has made before the crash and replay its effects; and (2) perform the remaining tasks and checkpoint the further progress in the memento. As a result, an operation makes its effect exactly once—neither never nor twice—even in case of multiple crashes; and returns the same output before and after crashes.

For correct checkpointing of the progress, a memento should record in PM exactly which operation steps are already performed and what are their outputs. In general, we construct such a memento by composing primitive operations. First, we design mementos for primitive operations such as (1) checkpointing of non-deterministic computations; and (2) compare-and-swap, insertion, and deletion of memory blocks. The former is necessary to ensure the operation produces the same output after crashes; and the latter serves as the basis for pointer-based lock-free DSs. Second, we compose multiple mementos to construct that for a composite operation while retaining detectability. As we will see shortly, we support sequence, conditional branch, and loop compositions of operations.

2.2 Primitive Operation Example: Checkpoint

As an example of an operation with memento, we present the CHECKPOINT operation recording a value so that it is preserved after crashes. This operation effectively stabilizer possibly nondeterministic input to a deterministic output so that, e.g., the operation always takes the same control flow across crashes (see §2.3 for details on the requirement for correct recovery). You may checkpoint an expression as follows:

Let e be a non-deterministic expression and mmt be a checkpoint variable memento. Then the value v is preserved across crashes.

Algorithm. We ensure CHECKPOINT’s atomicity—we can never see a partial result of the computation—by defining a memento as two timestamps and two write buffers. An operation Φ compares the given memento’s two timestamps and figure out which are stale and latest; Φ if the latest timestamp is bigger than those of the thread’s previous operations, exits immediately; Φ writes the given value to the memento’s stale buffer; Φ flushes the stale buffer if the memento is not fit in a cacheline; and Φ updates the stale buffer’s timestamp to the current timestamp and flushes it. Here, Φ detects whether the operation is already performed in a pre-crash execution; and the flush in Φ ordering the writes to buffer and to timestamp, is unnecessary if they are fit in a single cacheline because all writes to a single cacheline in PM are automatically ordered.

System Assumptions. We retrieve timestamps by Intel-x86’s rdtsc and rdtscp instructions. We use Intel-x86’s fLush and fLushopt instructions to ensure a write to a PM location is persisted. More specifically, a store or update to a PM location, say loc, is guaranteed to be persisted (1) at a following fLush loc instruction; or (2) at a following sfence or successful CAS instruction preceded by a fLushopt loc instruction. We refer to [17] for more details on the semantics of fLush and fLushopt for Intel Optane DCPMM.

Comparison. Our CHECKPOINT algorithm differs from how [10] persists stack variables with two buffers and a valid bit in that ours additionally records the timestamp when the value is checkpointed. The timestamps enable each operation to detect, at recovery, whether it has already been executed before the crash. For instance, consider the following CONTRIVED(i1, i2, mmt) operation:

The operation is given two inputs i1 and i2 and a memento mmt, and returns a value as an output at line 6 (or L6 from now on). we will discuss the meaning of underlines shortly. The sub-memento
For each $f$, if $mmt.f$ is the $f$ field of the whole operation’s composite memento $mmt$. Suppose this operation is interrupted by a crash between L3 and L4 after a few iterations of the loop, checkpointing timestamps as commented. At a recovery, the operation executes the code from the beginning and retrieves the checkpointed values at L1 and L3 as their timestamp increases, but checkpointing a new value at L4 and resumes from there as a normal execution because the timestamp no longer increases. We record the maximum timestamp of each thread’s previous operations in the global array LOCAL in DRAM. The array is used for other detectable operations as well (see §3 for details).

Thanks to timestamps, our algorithm flushes fewer writes to PM than prior works: [10] needs to additionally checkpoint the program counter in PM, and [9, 42] need to reset operations by writing sentinel values to PM.

### 2.3 Stable Composition

For correct checkpointing of an operation’s progress, we need not only to use primitive detectable operations but also to stably compose them as follows. For simplicity, we assume the operation is in the Static Single Assignment (SSA) form [18, 19] so that each local variable is defined only once syntactically, and loop variables are defined as an SSA φ-node at the beginning of a basic block, e.g., $i = \phi(i_0 \oplus B_0, i_1 \oplus B_1)$ assigns $i_0$ (or $i_1$) to $i$ if the control flows from the basic block $B_0$ (or $B_1$, respectively). For those who are not familiar with SSA, we will present an SSA form example shortly.

**Requirement 1 (Stable memento).** Different (syntactic) sub-operations of an operation are performed with different sub-mementos of the whole operation’s memento.

As a result, the sub-mementos are not interfered with each other. For instance, CONTRIVED satisfies this requirement as its sub-operations at L1, L3, L4, L5 use different sub-mementos of $mmt$.

**Requirement 2 (Stable value).** Branch conditions and certain sub-operation inputs are stable, i.e., they are the same across crashes.

As a result, an operation takes the same control flows and its sub-operation produces the same outputs across crashes. Throughout this paper, we underline stable expressions. For instance, CONTRIVED satisfies this requirement because the branch condition $(v_1 = (v_4 ? i_1 : i_2))$ at L6 is stable as $v_1$ and $v_4$ are sub-operation outputs and $i_1$ and $i_2$ are stable inputs; and the inputs $v_2$ and $v_3$ at L5 are stabilized by CHECKPOINT.

Here, we allow each operation to declare which inputs should be stable, e.g., (1) the expression input to CHECKPOINT (e.g., $e_1$ at L1) does not need to be stable; while (2) the current and new pointer value inputs to detectable Cas (e.g., $v_2$ and $v_3$ at L5) should be stable. This flexible requirement for input stability enables optimized implementation of the operations (see §4 for details).

**Requirement 3 (Stable loop).** Suppose a loop contains at least one detectable sub-operation using memento. Then (1) the loop head’s basic block has at most one φ-node; and (2) the φ-node, if exists, is immediately checkpointed.

Loops are interesting because loop bodies may reuse mementos despite Requirement 1, e.g., $mmt.c_2$ is used to checkpoint different values in different iterations of the loop at L2-L7. This requirement ensures the loop body’s sub-operation results of two consecutive iterations are not mixed in the sub-mementos. For instance, CONTRIVED trivially satisfies this requirement as its the only loop has no φ-nodes. For another instance, consider the following operation:

1. $i_0 \leftarrow e$
2. **loop**
   3. $\frac{i}{i_{\text{next}}} \leftarrow \text{CHECKPOINT}(\phi(i_0, i_{\text{next}}), mmt)$
   4. **if** $i = 100$ **then** **break**
   5. $i_{\text{next}} \leftarrow i + 1$
6. **end loop**

Here, we omit the φ-node’s incoming blocks because they are obvious from the context. The semantics of $\phi(i_0, i_{\text{next}})$ of the loop is that it gets $i_0$ for first iteration and $i_{\text{next}}$ for the remaining iterations. This example also satisfies the requirement as the loop has a single φ-node that is immediately checkpointed at L3.

The checkpointed φ-node serves as the context for a loop iteration. The sub-requirement (2) says the context should be recorded for each iteration; and (1) says the context should be atomically recorded so that it is not mixed across multiple iterations. Together, the requirement effectively guarantees you can correctly recover the loop iteration context, and from there, the progress that has been made so far inside the loop.

### 2.4 Transformation

Given a lock-free DS operation for DRAM, we systematically transform it into a detectable operation for PM by stably composing its sub-operations as follows. For instance, CONTRIVED can be transformed from the below code as follows:

1. $v_1 \leftarrow e_1$
2. **loop**
   3. $v_4 \leftarrow \text{CasPlain}(e_2, e_3)$ # CAS without detectability
   4. **if** $v_1 = (v_4 ? i_1 : i_2)$ **then** **return** $v_4$
5. **end loop**

We replace plain CASes with detectable CASes (§3) or insert/delete operations (§4). We use a fresh sub-memento for each detectable CAS or insertion/deletion to satisfy Requirement 1. For the example, we choose to replace CasPlain with Cas, introducing a fresh sub-memento for the sub-operation. We perform the SSA transformation [18, 19] further, for each loop containing at least one detectable operation, we merge all φ-nodes into a single φ-node of tuples and checkpoint it to satisfy Requirement 3. For the example, we have nothing to do because it does not need φ-nodes. We insert CHECKPOINT operations using fresh sub-mementos to satisfy Requirement 2. We choose expressions to checkpoint using backward taint analysis from branch conditions and sub-operation inputs. For the example, we stabilize $e_2, e_3, \text{ and } (v_1 = (v_4 ? i_1 : i_2))$ by checkpointing $e_2, e_3,$ and $v_1$. We do not need to checkpoint the other variables because $v_4$ is the stable result of a detectable CAS and we assume $i_1$ and $i_2$ are stable inputs. We could alternatively checkpoint $(v_1 = (v_4 ? i_1 : i_2))$ as a whole; or checkpoint $i_1$ and $i_2$ and assume they are unstable inputs. We heuristically choose as above to minimize the number of CHECKPOINT operations.

### 2.5 Top-Level Application

At the top level, an application is structured as a root object and its mementos persisted in PM. The monitor manages the execution
of an application by (1) loading the root object and its mementos from PM when the application is started; (2) for each root memento, creating a thread to execute a root operation with the memento; (3) should a thread crash, re-creating a new thread that resumes the operation with the same memento; and (4) servicing safe memory reclamation (see §6 for details). As a caveat, we currently assume only a single Intel Optane DCPMM module is utilized; and the type of root object and mementos and the number of root mementos are statically known. Both of them, while unrealistic, can be easily lifted by designing a more sophisticated monitor, which we leave as future work.

**Timestamp Calibration.** At an application start, we need to calibrate timestamps because those retrieved by Intel-x86’s rdtsc and rdtscp instructions measure the number of ticks after the system was booted, and as a result, they are not strictly increasing in case of reboots either due to crashes or by user commands. This invalidates our assumption on timestamp monotonicity for CHECKPOINT and the other primitive operations we will see shortly. We re-establish this assumption by calibrating timestamps at application starts as follows: Θ we calculate the maximum timestamp checkpointed in all the mementos, say $T_{\text{max}}$; Θ we get the current timestamp retrieved by Intel-x86’s rdtsc instruction, say $T_{\text{init}}$; and Θ we add the offset $(-T_{\text{init}} + T_{\text{max}})$ to all the timestamps retrieved by rdtsc and rdtscp in the application execution. Then it is straightforward that the calibrated timestamps are always larger than those checkpointed in the application’s past executions.

## 3 DETECTABLE COMPARE-AND-SWAP

We design, as a key primitive operation, detectable CAS on atomic PM location. Our algorithm is based on those of Attiya et. al. [9] and Ben-David et. al. [10]. Their key idea is performing architecture-provided plain CASes twice: it first performs a plain CAS that annotates the thread id to the location’s pointer value, checkpoints the operation so that it can be detected later, and performs another plain CAS that removes the annotation from the pointer value. If a load or CAS operation sees a pointer value annotated with a thread id—that means there is an ongoing CAS, then it helps its second plain CAS in a detectable manner. The detectable helping mechanism requires an array of $O(P^2)$ [9] or $O(P)$ [10] sequence numbers for each object in PM, where $P$ is the number of threads, prohibiting its use for space-efficient DSs such as hash tables. We overcome this limitation by proposing a new helping mechanism that requires only an architecture word for each object and a global array of $O(P)$ timestamps in DRAM and PM.

### 3.1 Components and System Assumptions

We present the components for detectable CAS and their assumptions on the underlying system platform.

**Location.** A location is just an architecture word, which is 64 bits in the Intel Xeon platforms supporting DCPMM. We split 64 bits into three categories: 1-bit parity (for helping, see §3.4 for details), 9-bit thread id, 9-bit user tag, and 45-bit offset. The thread id 0 is reserved for the CAS algorithm’s purposes. Thread id can distinguish 511 threads and offset can address 32TB, which are sufficient for the current generations of DCPMM. (We may need to allocate more bits to them by shrinking user tag in the future, though.) The tag [6] is reserved for users to annotate arbitrary bits to pointer values for algorithm correctness (e.g., the synchronization in Harris’s list [26]) or optimization (e.g., hash value in the Clevel hash table [15]). We assume the $\text{encode}$ and $\text{decode}$ functions convert a tuple of parity, thread id, offset with user tag into a 64-bit word and vice versa.

A location provides two operations: load and detectable CAS. Both operations are oblivious of parity and thread id so that their input and output pointer values should be annotated with the default values, namely evenness and the reserved thread id 0. These operations differ from the architecture-provided plain load and CAS operations in that they additionally receive the current thread id as an argument, and CAS also receives a memento.

**Memento.** A CAS memento is also a 64-bit architecture word split into three categories: 1-bit parity, 1-bit failure flag, and 62-bit timestamp retrieved by Intel-x86’s rdtsc instruction. We reserve timestamp 0, which cannot appear after booted, for those mementos that did not checkpoint any operations yet. The timestamp is used to calculate $T_{\text{max}}$ for timestamp calibration when the application is started (§2.5). The 62 bits are sufficient to support systems running for about 47 years without incurring integer overflow. We assume the $\text{encodeTs}$ and $\text{decodeTs}$ functions convert a tuple of parity and timestamp into a 64-bit word and vice versa.

For correct synchronization, we assume rdtscp guarantees the following properties that are indeed satisfied by the Intel Xeon platforms supporting DCPMM: (1) **Synchronous:** the timestamp is synchronized among multiple CPU cores even for multiprocessor systems. This property is ensured in modern platforms by synchronous reset signal from the mainboard. (2) **Constant:** the timestamp increments at a constant rate even when CPU frequency changes. This property is ensured in modern platforms by dedicated timestamp generators. Thanks to this property, e.g., two consecutive invocations of rdtsc return different timestamps. (3) **Serializing:** rdtscp, when followed by sfence, is serializing so that the surrounding instructions are never reordered across these instructions. This property is described in Intel-x86’s architecture manual [33]. We use this property to ensure the correctness of our helping mechanism (see §3.4 for more details).

**Global Timestamp Arrays.** We introduce three more global arrays of $P$ timestamps annotated with 1-bit parities: $\text{OWN}$ in DRAM and $\text{HELP}[2]$ in PM. The former records the timestamp of the last CAS operation performed by each thread, and is initialized as the maximum timestamp checkpointed in CAS mementos at application starts. The latter checkpoints the maximum timestamp of each thread’s CAS operations helped by the other threads for each parity. As we will see, these invariants are maintained and exploited in our algorithm. The $\text{HELP}[2]$ array is initialized with 0 when an application is created and used to calculate $T_{\text{max}}$ for timestamp calibration because they are retrieved in post-crash recovery executions.

### 3.2 Normal Execution

Algorithm 1 presents the load and detectable CAS algorithms. We omit memory orderings, but they are appropriately annotated in our implementation. The **Load** operation (L1) simply performs an architecture-provided plain load. Since it may observe a transient
Algorithm 1 Atomic Pointer Location supporting Detectable CAS

1: function LoadHelp(loc, tid)
2: cur ← LoadPlain(loc)
3: return LoadHelp(loc, cur)
4: end function

5: function CAS(loc, old, new, tid, mmt, recovery)
6: \( (p_{\text{own}}, t_{\text{own}}) \leftarrow \text{DECODETs}(\text{LoadPlain}(\text{OWN}[\text{tid}])) \)
7: old' ← Encode(Even, 0, old)
8: new' ← Encode(\( \neg p_{\text{own}}, tid, new \))
9: if recovery then
10: pt ← LoadPlain(mmt)
11: \( (p_{\text{rmmm}}, t_{\text{rmmm}}) \leftarrow \text{DECODETs}(pt) \)
12: cur ← LoadPlain(loc)
13: \( (\_, t_{\text{local}}) \leftarrow \text{DECODETs}(\text{LoadPlain}(\text{LOCAL}[\text{tid}])) \)
14: if \( t_{\text{mmt}} < t_{\text{local}} \) then goto 39
15: if \( p_{\text{mmt}} = \text{Fail} \) then
16: StorePlain(LOCAL[tid], pt)
17: return (Err LoadHelp(loc, cur))
18: end if
19: if \( t_{\text{mmt}} \neq 0 \wedge t_{\text{mmt}} < t_{\text{own}} \) then \( t_{\text{succ}} \leftarrow pt; \) goto 39
20: if \( t_{\text{mmt}} \neq 0 \wedge t_{\text{mmt}} \geq t_{\text{own}} \) then \( t_{\text{succ}} \leftarrow pt; \) goto 36
21: \( (p_{\text{cur}}, t_{\text{cur}}, 0_{\text{cur}}) \leftarrow \text{DECODE}(\text{cur}) \)
22: if \( t_{\text{cur}} = t_{\text{tid}} \land 0_{\text{cur}} = \text{new} \) then goto 33
23: t\text{help} ← \text{LOADPLAIN}([\text{HELP}][\neg p_{\text{own}}[[t_{\text{tid}}]])
24: if \( t_{\text{own}} < \text{t}\text{help} \) then goto 34
25: end if
26: if CASPlain(loc, old', new') is (Err cur) then
27: cur ← LoadHelp(loc, cur)
28: if \( \text{cur} = \text{old} \) then goto 26
29: ts\text{fail} ← \text{DECODETs}(\text{Fail}, 0)
30: StorePlain(mmt, ts\text{fail}), flush mmt
31: StorePlain(LOCAL[tid], ts\text{fail}); return (Err cur)
32: end if
33: flush loc
34: ts\text{succ} ← \text{DECODETs}(\neg p_{\text{own}}, \text{rdtscp}); sfence
35: StorePlain(mmt, ts\text{succ}), flushopt mmt
36: StorePlain(\text{OWN}[tid], ts\text{succ})
37: new' ← Encode(Even, 0, new)
38: if CASPlain(loc, new', new') is ERR then sfence
39: StorePlain(LOCAL[tid], ts\text{succ}); return (Ok)
40: end function
41: function CASMementoClear(mmt)
42: StorePlain(mmt, Encode(Even, 0))
43: flushopt mmt
44: end function

value written by a concurrent (detectable) CAS operation’s first plain CAS (L26), it invokes LoadHelp to help the CAS operation and retrieve a stable value without parity or thread id annotations (see §3.4 for more details). On the other hand, the CAS operation (L5) first checks if it is executed in the recovery mode (see §3.3 for more details). Otherwise, CAS loads the parity and timestamp of its last CAS operation (L6) and toggles the parity (\( \neg p_{\text{own}} \) at L8 and L34); CAS performs the first plain CAS from the old pointer (L7) to the new one (L8) annotated with the toggled parity and its thread id (L26); if the plain CAS fails, then retrieves a stable current value using LoadHelp, and depending on the current value, retries the plain CAS, or invalidates the memento by the sentinels value encodeTs(Fail, 0) and returns (L27-L31); flushes the first plain CAS (L33); checkpoints the toggled parity and the current timestamp in the memento (L34-L35); maintains OWN’s invariant (L36); and tries to perform the second plain CAS removing parity and thread id annotations, and regardless of its result, ensures the checkpointing is flushed (L38). The second plain CAS may fail because a concurrent thread may have already helped performing it. A memento can later be reused after clear to the reserved timestamp 0 in a persistent manner (L41).

In the absence of crash and contention with the other threads, CAS effectively replaces an old pointer value with the new one (without parity or thread id annotations) in a persistent manner. Now we will see what would happen in case of crash (§3.3) and contention (§3.4).

3.3 Recovery

Should a thread crash in the middle of a CAS, the post-crash recovery must resume the operation so that CAS is performed exactly once. In particular, the recovery execution of CAS needs to distinguish the cases when the pre-crash execution is interrupted (1) before persisting the first plain CAS (L26); (2) after an unsuccessful first plain CAS (L30); or (3) after a successful first plain CAS and that before persisting the memento (L35); or (4) after that. To this end, the recovery execution of CAS globally initializes OWN only once for each thread as the maximum checkpointed timestamp of the thread’s CAS mementos; loads and decodes the memento (L10-L11); if the memento’s checkpointed timestamp is less than the thread’s LOCAL, then go to step (L12-L14); if the memento checkpointed a failure, then reports an error (L15-L18); if the memento checkpointed a CAS operation that is not the thread’s last one, then return Ok (L19); if the memento checkpointed the thread’s last CAS operation, then resumes from the normal execution’s step (L20); if the location contains the first CAS’s new value, then resumes from the normal execution’s step (L22); if the CAS is helped by a concurrent thread (see §3.4 for more details), then resumes from the normal execution’s step (L24); and finally, resumes the normal execution (L25).

For each case, the post-crash recovery execution correctly resumes the operation as follows:

1. Since the operation performed nothing to the location and memento, it goes to the step (1) and resumes the normal execution.
2. Since the operation checkpoints a failure, it goes to the step (2) and returns Err again.
3. Since the operation performed nothing to the memento, it goes to the step (3). Since the first plain CAS is persisted, either the location still contains the plain CAS’s new value (3) or the CAS is helped by a concurrent thread (3). In either case, the recovery execution correctly resumes from the normal execution’s step (3) or (3), respectively) checkpointing the memento.
4. If the CAS is not the last one, there is nothing to do (3); otherwise, the recovery execution correctly resumes from the normal execution’s step (3) performing the second plain CAS.
We synchronize a CAS operation and a helper in a detectable manner. A thread may help an ongoing CAS operation’s second plain CAS.

On the one hand, and only if the thread’s parity and timestamp are as follows: suppose a thread’s CAS operations helps the ongoing CAS operation’s second CASPlain entry with location, and it returns

\[
\text{ CassidyPlain} (\text{loc, old}) \leftarrow \text{ CassidyLoad} (\text{loc})
\]

\[
\text{ CassidyLoad} (\text{loc}) \leftarrow \text{ CassidyHelp} (\text{loc})
\]

\[
\text{ CassidyHelp} (\text{loc}) \leftarrow \text{ CassidyLoad} (\text{loc})
\]

3.4 Helping

A thread may help an ongoing CAS operation’s second plain CAS. We synchronize a CAS operation and a helper in a detectable manner using timestamp and parity. The CassidyLoad operation, presented in Algorithm 2, receives a location loc and an old value of the location, and it returns old if it is stable (L3); reads the current timestamp and executes a fence (L4); reads from the location again, and returns it if it is stable (L5-L7); if old \( \neq \) cur, then retries from L4 (L8); flushes the location (L12); tries to increment the CassidyLoad entry to my timestamp in a persistent manner; and if it fails, then retries from the beginning (L13-L16); helps the ongoing CAS operation’s second plain CAS, and if it fails, then retries from the beginning (L17-L20); and finally, returns the newly written stable pointer value (L21).

The CassidyLoad array is used to synchronize the CassidyLoad and CassidyCAS operations in case of crashes. A post-cash recovery execution of the CassidyCAS operation consults the CassidyLoad array (L3-L24) to distinguish the cases ① and ③ in §3.3, or in other words, whether the pre-cash recovery execution’s first plain CAS (L26) is persisted. To this end, we use the following invariant: suppose a thread tid’s n-th CAS invocation’s parity and timestamp are \( p_n \) and \( t_n \), respectively. Obviously, the sequence \( \{ t \} \) is alternating between Even and Odd, and the sequence \( \{ t \} \) is strictly increasing. Then \( t_{n-1} < \text{ CassidyLoad} (\text{loc}) \) if and only if the n-th CAS with the parity \( p_n \) is helped by a concurrent thread. On the one hand, Cassidy exploits this invariant to make a correct decision at L23-L24. On the other hand, Cassidy maintains this invariant as follows.

Suppose a CassidyLoad operation retrieves a timestamp \( t_h \) at L4 and tries to help a the second plain CAS of a thread tid’s n-th CAS invocation, as illustrated in Figure 3. Here, we depict the plain CASes and timestamp retrieval of tid’s (n − 1)-th to (n + 1)-th CAS invocations and loads and timestamp retrieval of a CassidyLoad invocation, where Update\(_{n+1} \) represents the i-th plain CAS of tid’s n-th CAS and CassidyLoad represents a load from a location. Then we have the following properties:

1. \( t_{n-1} < t_h \) from a \( \rightarrow e \rightarrow h \rightarrow i \) and
2. \( t_h < t_{n+1} \) from a \( \rightarrow c \rightarrow j \rightarrow e \rightarrow g \), where po is the program order; \( rf \) is the from-read relation; \( fr \) is the from-read relation; \( fr, rf \) is the from-read relation possibly followed by a read-from relation; and all of them constitute the happens-before relation \( hh \) in the x86-TOO memory model [48]. For more details on the x86-TOO memory model, we refer the readers to [48] for space purposes.

Now recall that CassidyLoad persists Update\(_{n+1} \) (L12), atomically increases CassidyLoad [tid] to \( t_h \) (L13-L16), and helps CassidyLoad (L17-L18). If the thread tid’s n-th CAS is helped by a concurrent thread, then we have \( t_{n-1} < t_h \leq CassidyLoad [tid] \) due to the property (1); conversely, if \( t_{n-1} < CassidyLoad [tid] \), then it should be the result of a help neither for tid’s CASes with the parity \( p_n \) nor for tid’s (n − 2)-th or earlier CASes due to the property (2). In other words, CassidyLoad maintains the invariant of CassidyLoad mentioned above.

4 DETECTABLE INSERTION AND DELETION

We design, as optimized primitive operations, detectable insertion and deletion of nodes on atomic PM location. While Cassidy is a general primitive operation for pointer-based DSs, we observe that the performance of DSs implemented with detectable Cassidy (§3) are sometimes significantly worse than that of hand-tuned detectable DSs. The primary reason is that the general detectable CAS performs plain CASes to the same location twice and flushes the location between them, incurring an extremely high contention on the location among multiple threads.

As an optimization, we design a more efficient atomic pointer location object supporting detectable insert—atomically replacing the NULL pointer—and delete—atomically detaching a valid memory block from DSs—operations by capturing the essence of hand-tuned

![Algorithm 2 Atomic Pointer Location supporting Detectable CAS](image)

**Figure 3: Synchronization of Detectable CAS and CassidyLoad**
detectable DSs. The key idea is distributing the contention of multiple threads into multiple memory blocks, significantly relieving contention on any single location. Such an optimization, however, requires non-trivial synchronization among multiple memory blocks, thus limiting its application to only insert and delete operations. While less general than CAS, insert and delete operations still support a wide variety of DSs, e.g., we can implement Michael-Scott’s queue (MSQ) [46] and exchanger with insert and delete operations.

4.1 Components and DS Assumptions

We present the components for atomic pointer location supporting insertion and deletion and their assumptions on the DS.

**Location.** A location is a 64-bit architecture word, which we split into four categories: 1-bit “persist” flag for the **link-and-persist** technique [20], 8 bits reserved for future purposes, 10-bit user tag, and 45-bit offset. We follow David et. al. [20] in enforcing the invariant that, if the persist bit is cleared, then the pointer value is persisted. Such an invariant is cooperatively maintained by location’s three operations: load, insertion, and deletion. The load operation ensures that the returned pointer value is always persisted in the location. Insertion receives a location and a new pointer value as arguments, and deletion receives a location, old and new pointer values, a memento, and the current thread id. We assume the **encode** and **decode** functions convert a tuple of persist bit and offset with user tag into an 64-bit word and the other way around.

**Memory Block.** We assume each memory block has a dedicated 64-bit architecture word, which we call repl1, that describes the memory block that replaces itself as an atomic location’s next pointer value. We split 64 bits into two categories: 9-bit thread id, 10-bit user tag, and 45-bit offset. Similarly to §3, the thread id 0 is reserved for those blocks that are not replaced yet. We assume the **encodeR** and **decodeR** functions convert a tuple of thread id and offset with user tag into an 64-bit word and the other way around.

**Traversal.** As we will see, we checkpoint the insertion of a memory block to a DS in the inserted node’s repl1 field, and for efficiency purposes, we perform such checkpoint only when the block is deleted (see §4.2 for details). Should the system crash, we detect whether a non-checkpointed memory block was inserted before the crash by checking if the block is still in the DS. To this end, we require the ability to traverse all the memory blocks in a DS. For instance, an MSQ [46] is traversable from its head by recursively chasing each node’s next pointer.

**Memento.** Insertion and deletion do not need a memento because the progress is checkpointed in the input node’s repl1 field.

4.2 Normal Execution

**Algorithm 3** presents the load, insertion, and deletion algorithms.

**Load.** The **Load** operation, which we adopt from [20], ensures the returned pointer values are always persisted by the performing an architecture-provided plain load and decodes the pointer value (L2-L3); ○ if its persist bit is cleared—which implies the pointer value is persisted, then returning the pointer value (L4); otherwise, ○ retrying for a while to read a pointer value without the persist bit being set (L5-L10); and if it fails, ○ flushing loc itself (L11), ○ trying to clear the persist bit of loc by performing a CAS, and if it fails, retrying from the beginning (L12-L13); and ○ returning the pointer value with the persist bit being cleared (L14).

**Insertion.** The **Insert** operation on a location, say loc, atomically replaces the Null pointer with the given pointer value, say new, in a persistent manner (L16). Insert first checks if it is executed in the recovery mode (see §4.3 for more details); otherwise, it ○ atomically updates loc’s pointer value from the Null pointer to the given pointer with the persist bit being set (L21); if it fails, reports an error with the current pointer value (L22); ○ flushes loc (L24); and ○ tries to atomically clear loc’s persist bit (L25). It is okay to let the

---

**Algorithm 3 Load, Insertion, and Deletion**

1. function Load(loc)
2. old ← LoadPlain(loc)
3. (old, oold) ← decode(old)
4. if ¬pold then return oold
5. t ← rdtsc
6. cur ← LoadPlain(loc)
7. (pcur, ocur) ← decode(cur)
8. if ¬pcur then return ocur
9. if old ≠ cur then old ← cur; goto 3
10. if rdtsc < t + PATIENCE then goto 6
11. flush loc
12. old′ ← encode(False, oold)
13. if CASPlain(loc, old, old′) is (Err cur) then old ← cur; goto 3
14. return old′
15. end function
16. function Insert(loc, new, ds, recovery)
17. if recovery then
18. if Contains(ds, new) ∨ (LoadPlain(new.repl1) # Null) then return Ok
19. return (Err Load(loc))
20. end if
21. if CASPlain(loc, Null, encode(True, new)) is Err then
22. return (Err Load(loc))
23. end if
24. flush loc
25. CASPlain(loc, encode(True, new), encode(False, new))
26. end function
27. function Delete(loc, old, new, tid, recovery)
28. if recovery then
29. (tidnew, onew) ← decodeR(LoadPlain(old.repl1))
30. if tid ≠ tidnew then return (Err LoadHelp(loc, old))
31. goto 37
32. end if
33. new′ ← encodeR(tid, new)
34. if CASPlain(old.repl1, null, new′) is (Err cur) then
35. return (Err LoadHelp(loc, old))
36. end if
37. flushopt repl1
38. CASPlain(loc, old, new); DeferFlush(loc); Retire(old)
39. return old
40. end function
second CAS fail (L25) because it means a concurrent load or delete operation should have persisted loc and cleared the persist bit.

**Deletion.** The DELETE operation, illustrated in Figure 4, on a location, say loc, atomically detaches the given pointer to a valid memory block, say old, and stores another given pointer, say new, in a persistent manner (L27). DELETE first checks if it is executed in the recovery mode; otherwise, it tries to atomically install new annotated with the current thread id to old’s repl field (L33-L34); if it fails, helps the completion of concurrent delete operations and reports an error (L35, see §4.4 for details on helping); flushes old’s repl field (L37); tries to replace loc’s value from old to new, persists loc in a deferred manner, and retires old (L38); and returns old (L39). Here, we retire old so that it will be freed once it is no longer accessible from the other threads using safe memory reclamation schemes such as hazard pointers [45] and epoch-based reclamation [22]. We also ensure loc is flushed at least before old is freed using DEFERFLUSH so that loc points to a valid memory block even in case of crashes (see §6 for details on safe reclamation).

A delete operation is committed when the CAS on old’s repl (L34) is persisted, while its effects are applied to loc later (L38). It is still safe for concurrent operations to see an old value of loc even though a new value is already committed: a concurrent load operation can simply return the old value because it can linearize before the deletion; similarly, a concurrent insert and delete operations can linearize beforehand and fail.

**4.3 Recovery**

**Insertion.** The recovery execution of insertion needs to distinguish the cases when the pre-crash execution is interrupted before or after persisting the first CAS (L21). To this end, we apply direct tracking method in [8], i.e., the recovery execution of insertion checks if either (1) the node is still contained in the enclosing DS by performing a traversal; or (2) the node’s repl field is populated, which means it is already deleted (L18). It is straightforward that it is the case if and only if the node have indeed been inserted. Here, the recovery execution spuriously fails to insert the given memory block—even though loc is NULL—when the pre-crash execution is interrupted before persisting the first CAS. In this case, the memento needs to restart the insert operation in a normal execution.

**Deletion.** The recovery execution of deletion needs to distinguish the cases when the pre-crash execution is interrupted (1) before persisting the first CAS (L34); or (2) after that. To this end, the recovery execution of deletion tries to replace old’s repl and decodes the old’s repl, and if its tid is not the current thread id, reports an error (L29-L30); otherwise, resumes from the normal execution’s step (L31).

For each case, the post-crash recovery execution correctly resumes the operation as follows:

(1) Since the operation performed nothing to old’s repl, it goes to L30 and spuriously fails the operation;

(2) Since new should contain the current thread id, it goes to L37 and correctly resumes from the normal execution’s step.

**4.4 Helping**

A delete operation may help an ongoing concurrent delete operation’s second CAS. Such a help is essential for lock freedom because the concurrent operation may be committed—have successfully performed the first CAS—while its effects have not been applied to loc yet. The LOADHELP operation, presented in Algorithm 4, receives a location loc and an old value old of the location and returns a stable value of loc by possibly helping the second CAS of ongoing deletions as follows: it loads and decodes old’s repl as new (L3-L4); returns old if repl is NULL and thus old is stable (L5); reads a pointer value for a while (L6-L9); flushes old’s repl (L10); tries to update loc from old to new, and regardless of the result, returns the current value of loc (L11-L13).

**5 DRAM SCRATCHPAD OPTIMIZATION**

We propose a guideline for optimizing detectable DSs with DRAM scratchpad while preserving detectability. By DRAM scratchpad we mean putting a part of persistent DSs in DRAM. Such an optimization is pioneered in SOFT [63] and Mirror [25] that replicate PM contents in DRAM for higher performance, and is known to be extremely effective for lock-free DSs in PM. However, the optimization is neither supported by our composition (§2) nor explicitly recognized and exploited for detectable DSs in the literature. We explain the concept of DRAM scratchpad optimization and propose a correctness guideline for detectable DSs using Michael-Scott’s queue (MSQ) [46] and SOFT hash table [63] as running examples.
Michael-Scott’s Queue. A volatile MSQ [46] is a linked list and has “tail” pointer that points to the list’s tail block in a best-effort basis. If a volatile MSQ is converted to a detectable MSQ with our transformation (§2.4), then the tail pointer becomes a PM location and all its modifications become detectable CASes, incurring noticeable overhead over volatile MSQ. But the prior works on persistent MSQs [24, 42] made an observation that the tail pointer does not need to be persisted in PM as its exact value is not crucial and it only needs to maintain the following invariants: the tail is reachable from the queue’s “head” pointer (also an invariant of the volatile MSQ); and all the links in the traversal from the head to the tail is preserved (new in the persistent MSQ). As a result, they put the tail in DRAM scratchpad and ensure the invariants are maintained throughout the execution of operations by (1) assigning its head to its tail at application starts; (2) updating its head to its next block only if the tail is different from the head; and (3) updating its tail to its next block only if the link to the next block is persist.

Since the invariants already ensure the links from the head to the tail are persisted, load operations do not need to ensure the same property themselves, reducing a flush instruction for each load. We observe that this also improves the performance significantly.

Guideline. More generally, a detectable DS with DRAM scratchpad should be accompanied by relational invariants on DRAM scratchpad and PM data, and the invariants should be (1) established at application starts; (2) preserved at primitive detectable operations; and (3) preserved at DRAM scratchpad updates. We observe that the condition (3) is subtle for recovery executions where stale values checkpointed in a pre-crash execution may be used to update DRAM scratchpad, breaking its invariants. We should avoid such a case by updating DRAM scratchpad only with latest information, e.g., we update MSQ’s tail only in normal executions.

SOFT. Roughly speaking, SOFT [63] can be understood as a transformation of two copies of hash tables of which one is moved to PM and the other remains in DRAM as a scratchpad. The invariant is the equivalence of the two copies, and SOFT ensures this invariant by (1) reconstructing a DRAM copy from the PM copy at application starts; and (2,3) atomically updating both copies with a fine-grained concurrency control with helping. We observe that the same invariant and concurrency control satisfy the three conditions and thus work also for our detectable version of SOFT.

6 SAFE MEMORY RECLAMATION

All pointer-based lock-free DSs in DRAM should deal with the problem of safe memory reclamation (SMR). For instance, Treiber’s stack [13] is basically a linked list of elements with the head being the stack top, where a thread detaches the head block while another thread holds a local pointer to the same block. Due to the local pointer, the reclamation of the detached block should be deferred until every thread no longer holds such local pointers. In most cases, the SMR problem is systematically handled with reclamation schemes (think: lightweight garbage collection) such as hazard pointers (HP) [45] and epoch-based reclamation (EBR) [22].

Many of the prior works on persistent, pointer-based lock-free DSs in PM [12, 45] also handle the SMR problem with reclamation schemes. Friedman et. al. [24] use HP, and Li et. al. [42] and (nb)Montage [12, 57] use EBR. However, we argue that the prior works do not properly discuss the subtlety arising from applying reclamation schemes to PM. We address this subtlety by discovering and fixing a use-after-free bug of the prior works (§6.1); preventing double-free error in case of a thread crash (§6.2); and preventing use-after-free error via the local pointers checkpointed in mementos (§6.3). For a concrete context, we explain our fix and preventions on EBR.

6.1 Fixing a Use-After-Free Bug

Bug. The queues of Friedman et. al. [24] and Li et. al. [42] have a use-after-free bug caused by the lack of a flush before reclamation. We explain the bug in the context of our algorithm for deletion in Algorithm 3 for presentation purposes. If the location loc were not flushed before retirement at L38, then it is possible that (1) old is retired at L38 and and reclaimed later; (2) the system crashes; (3) the CAS to loc at L38 is not persisted and loc still contains old after the crash; and (4) a post-crash execution dereferences old. The queues lack such a flush between a CAS and a retirement, possibly incurring a use-after-free error.

Fix. A straightforward fix would insert a flush between the CAS and the retirement at L38, but we observe that such a flush is detrimental to the performance. We mitigate the slowdown by exploiting the following property of EBR: if a memory block is retired in a critical section, then it is never reclaimed in the same critical section. Concretely, instead of flushing loc at L38, we defer the flush of loc with a new DeferFlush API and actually perform such flushes in batch at the end of a critical section. Batching is beneficial for two reasons: (1) we can merge multiple flushes to the same location; and (2) we can finish a critical section in an asynchronous manner so that the flushes are performed not in the critical path. In our evaluation, we observe that the deferred flushes incur no noticeable runtime overhead.

6.2 Preventing Double-Free in Thread Crashes

Potential Error. A straightforward application of SMR schemes may incur double-free error in case of a thread crash due to the thread’s inability to detect whether a block is retired. Suppose a thread crashes at L38 in Algorithm 3, possibly before or after Retire(old). Then the post-crash recovery execution would go to L38 and perform CAS, DeferFlush, and Retire again. It is safe to perform CAS and DeferFlush again because they are idempotent, but it is not the case for Retire as double retirements of old incur a double-free error.

Prevention. We prevent this error by (1) retaining the critical section of a crashed thread and reviving it for the post-crash recovery execution; and (2) relaxing the retirement condition by allowing double retirements in a single critical section. For the former, we propose a new API for retrieving the critical section by thread id; and for the latter, we install a buffer of retired blocks and deduplicate it at the end of a critical section.

6.3 Preventing Use-After-Free via Mementos

Potential Error. For safe reclamation, we should clear local pointers not only in program variables but also in mementos. Otherwise, it may be possible that blocks are reclaimed, the thread crashes,
and then the operation retrieves and dereferences its memento’s local pointers, invoking use-after-free error.

Prevention. We prevent this error by clearing mementos just before the end of a critical section. More specifically, we (1) wrap a thread’s operation on its root memento within a critical section; and (2) at the end of a critical section, invoke **Clear** on the root memento, which invalidates all PM locations checkpointed inside it. For **Clear**’s crash consistency, we install a 1-bit “clearing” flag to the root memento, which is toggled and flushed at the beginning and the end of the method. Should a crash happens, the monitor first checks whether the flag is set, and if so, resumes **Clear**.

7 EVALUATION

We perform a performance evaluation of our programming framework for detectable DSs in PM. For space purposes, we present only key results here and present the full evaluation results in [1]. We use a machine running Ubuntu 20.04 and Linux 5.11 with dual-socket Intel Xeon Gold 6248R (3.0GHz, 24C/48T) and Intel Optane Persistent Memory 100 Series 256GB Module (DCPMM) configured in the App Direct mode. We pin all threads to a single socket to ensure all DCPMM accesses are within the same NUMA node.

We have implemented our programming framework in Rust 1.59.0 [5] and built it with release mode. We use Crossbeam [3] for memory reclamation and Ralloc [11] for allocation in PM. On top of the framework, we have implemented detectable versions the following DSs: **MSQ-mmt-cas**: Michael-Scott’s queue (MSQ) [46] with detectable CAS (§3); **MSQ-mmt-indel**: MSQ with detectable insertion/deletion (§4); **MSQ-mmt-vol**: MSQ with detectable insertion/deletion and DRAM scratchpad optimization (§5); **CombQ-mmt**: combining queue [21]; **Clevel-mmt**: Clevel hash table [15] with bug fixes [16]; and **SOFT-mmt**: SOFT hash table [63]. We will compare the performance of our queues (§7.1) and hash tables (§7.2) with the prior works with and without detectability.

7.1 Queue

We compare the throughput of our queues with that of **DurableQ**: non-detectable durable MSQ by Friedman et. al. [24]; **LogQ**: detectable MSQ by Friedman et. al. [24]; **PBcombQ**: detectable combining queue by Fatourou et. al. [21]; **PMDKQ**: non-detectable transaction-based queue in PMDK [31]; and **CorundumQ**: non-detectable transaction-based queue in Corundum [29]. We reimplement **DurableQ** and **LogQ** from scratch in Rust for fair comparison and a use-after-free bug (§6), and implement **DssQ** and **PBcombQ** in Rust because their source code is not publicly available. We observe the performance characteristic of **PBcombQ** is different from [21], because **PBcombQ** fixes two linearizability bugs of [21] that we reported to the authors.

Figure 5 illustrates the throughput of queues for four workloads: **enqueue-dequeue**: each operation enqueues an item and then immediately dequeues an item; **enqueue-20%**: each operation enqueues (or dequeues) an item for the probability of 20% (or 80%); **enqueue-50%**; and **enqueue-80%**. For each workload, we measure the throughput for a varying number of threads: 1 to 8 and the multiples of 4 from 12 to 64. We report the average throughput for each scenario of 5 runs, each of which is executed for 10 seconds.

Before measuring the throughput, we populate the queues with 10M items to avoid too many empty dequeues.

We make the following observations. (1) Transaction-based queues are noticeably slower than MSQs and combining queues. We omit the results of **PMDKQ** and **CorundumQ** for high thread counts because it took too much time to populate items. (2) Combining queues outperform MSQs for dequeue-heavy workloads. It is consistent with the observations made in [21]. (3) **MSQ-mmt-vol** outperforms the other MSQs in PM with and without detectability for two reasons. First, it outperforms **DurableQ** because the former’s dequeue writes the return value to mementos while the latter’s dequeue writes to a newly allocated node. Second, the timestamp-based checkpointing in mementos performs fewer PM flushes than the other detectable MSQs (§2.2). The only exception is **LogQ** for enqueue-80% with low thread counts, for which we are investigating the reason. (4) **MSQ-mmt-cas** and **MSQ-mmt-indel** perform comparably with the other MSQs in PM with and without detectability for dequeue-heavy workloads but not for enqueue-heavy workloads, because their enqueue performs CAS twice. (5) **CombQ-mmt** incurs noticeable overhead over **PBcombQ** because only the former supports reclamation. For safe reclamation, **CombQ-mmt**’s combiner allocates a new memory block.

7.2 Hash Table

We use the PiBench [41] benchmark because it is specifically designed for persistent hash tables. We compare the throughput and latency of our hash tables with those of the persistent hash tables considered in an evaluation paper [30]: **Clevel** [15], **SOFT** [63], **CCEH** [47], **Dash** [43], **Level** [62], and **PCHLT** [40]. We use the implementation of these hash tables provided in [30]. Among them, we convert only lock-free ones according to [30, Table 1], namely **Clevel** and **SOFT**, to detectable DSs.

Workloads. We use exactly the same workloads as [30]: “we stress test each hash table with individual operations (insert, positive and negative search, and delete) and mixed workloads. Negative search means searching keys that do not exist.” “We initialize hash tables with a capacity that can accommodate 16M key-value pairs.” “To measure insert-only performance, we insert 200M records into an empty hash table directly. To measure the performance of the search and delete operation and the mixed workloads, we first initialize the hash table with 200M items (loading phase), then execute 200M operations to perform the measurements (measuring phase).” “We run the experiments with workloads using uniform distribution and skewed distribution (self similar with a factor of 0.2, which means 80% of accesses focus on 20% of keys). Since CCEH, Level hashing, and PCHLT have no support for variable-length keys and values, we consider fixed-length (8 bytes) keys and values.”

All our results show the same tendency as in [30], so we compare only **Clevel-mmt** (and **SOFT-mmt**) with **Clevel** (and **SOFT**, respectively). For an evaluation of the other hash tables, we refer to [30].

Latency and Load Factor. Figure 6 illustrates tail latency of hash tables for 32 threads under uniform distribution. **Clevel-mmt** (and **SOFT-mmt**) shows similar tail latencies as **Clevel** (and **SOFT**, respectively) for all percentiles.
Clevel-mmt shows almost the same load factor as Clevel, because we did not change insert and resize schemes, and SOFT-mmt’s and SOFT’s load factors are always 100% (see [1] for full results).

**Single-threaded Throughput.** Figure 7 illustrates single-threaded throughput of hash tables under uniform and skewed distributions. For both distributions, we make the following observations. (1) Detectable hash tables incur overhead over the original ones for insert and delete workloads (except for Clevel’s insert, which we believe is due to implementation differences). It is expected from the fact that memento versions need to additionally checkpoint operation results. (2) Detectable hash tables show similar throughput with the original ones for search workloads. The reason is they execute almost the same instructions to read data.

**Multi-threaded Throughput.** Figure 8 and Figure 9 illustrate multi-threaded throughput of hash tables under uniform and skewed distributions, respectively. We make the same observations as with single-threaded throughput.
8 RELATED WORK

Detectable Lock-Free DSs in PM. Attiya et. al [9] presents a programming framework for detectable operations based on a novel detectable test-and-set (TAS) and CAS objects. However, their TAS and CAS objects consume $O(P)$ and $O(P^2)$ spaces in PM, respectively, prohibiting its use for space-efficient DSs such as hash tables and trees; and the authors present a few lock-free DS examples but do not present how to make lock-free DSs detectable in general.

Ben-David et. al. [10] presents such a general transformation with a novel concept of capsule: each capsule serves as a unit of detectable operation, and at the end of a capsule execution, the program counter and local state is checkpointed and used as the starting point at recovery. (1) While general, each capsule is required to follow one of the following forms to ensure its detectability: CAS-read, Read-Only, Single-Instruction, and Normalized [52]. In contrast, our transformation generally supports the SSA form [18, 19] (§2.4). (2) Capsule requires programmers to significantly restructure code for DRAM by explicitly delimiting programs into multiple capsules; and explicitly recovering states at the capsule boundaries. (3) Their detectable CAS object consumes $O(P)$ spaces in PM, while our detectable CAS object consumes 8 bytes for Intel Optane DCPMM.

Friedman et. al. [24] and Li et. al. [42] present frameworks for detectable operations and detectable MSQs in PM, but both have a bug on reclamation (§6.1) and perform slower than our MSQ due to an additional flush (§7.1). Rusanovsky et. al. [50] and Fatourou et. al. [21] present hand-tuned detectable combining DSs, while ours is generally transformed from a volatile one.

Non-detectable Lock-Free DSs in PM. Friedman et. al. [24] presents non-detectable lock-free MSQs based on hazard pointers [45] in PM. Our detectable MSQ outperforms both of them because their dequeue operation allocates a new node to write the return value (§7.1). Various hash tables [15, 40, 43, 47, 62, 63] and trees [7, 38] in PM have been proposed in the literature. In this paper, we convert the Clevel [15] and SOFT [63] hash tables to detectable DSs as case study because they are lock-free. Converting the others to detectable DSs is an interesting future work (see §9 for details).

Transformation of DSs from DRAM to PM. Izraelevitz et. al. [34] present a universal construction of lock-free DSs in PM, but it is reported that the constructed DSs are generally slow [23, 25]. Lee et. al. [40] propose a RECIPE to convert indexes from DRAM to PM, but their guideline is abstract and high-level and not immediately applicable to DSs in general. Kim et. al. [38] propose the Packed Asynchronous Concurrency (PAC) guideline to construct high-performance persistent DSs in PM, but their guideline is also abstract and high-level. In contrast, our transformation is a more concrete guideline at the code level.

NVTraverse [23] is a systematic transformation of a large class of persistent DSs exploiting an observation that most operations consists of two phases: read-only traversal and critical modification. Then the traversal phase does not require flushes at all. Mirror [25] is a more general and efficient transformation that replicates DSs in PM and DRAM scratchpad, significantly improving read performance. FliT [56] is a persistent DS library based on a transformation utilizing dirty cacheline tracking. However, NVTraverse, Mirror, and FliT do not support transformation of detectable DSs.

9 FUTURE WORK

Beyond those discussed in §8, We will do the following future work.

Case Study. Beyond lock-free DSs, we will perform more serious case studies with realistic storage engines to demonstrate our framework’s scalability. We are interested in designing detectable versions of traditional and distributed file systems, transaction processing systems for high-velocity real-time data [44], and distributed stream processing systems [54] in our framework. As a first step, we are currently building a lock-free PM file system.

Primitive Operation. For such case studies, we expect we should design more primitive detectable operations for those used in realistic storage engines. We are particularly interested in designing a detectable version of PMwCAS [55], which is CAS for multiple words performed atomically. PMwCAS is used in the BzTree persistent lock-free B-tree [7], and we believe it can also be used in file systems and storage engines in general. We are also interested in designing a detectable version of the standard constructs of fine-grained concurrency such as locks, combinners, and helpers.

Verification. As an ongoing work, we are formally verifying the crash consistency and detectability of those DSs implemented in our framework in a program logic. We believe that our framework has a great potential to lower the high cost of crash consistency verification because its stable nature unifies code for normal and recovery executions. We will realize our framework’s potential for lower-cost crash consistency verification by (1) designing a separation logic for PM by recasting the idea of a rely-guarantee logic for PM [49] in the Iris separation logic framework [4] on top of the Coq proof assistant [2]; (2) designing reasoning principles for detectable operations with mementos in the proposed separation logic; and (3) verifying detectable DSs.

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