Abstract—Polar codes have been selected as 5G standard. However, only a couple of ASIC featuring decoders are fabricated, and none of them support list size \( L > 4 \) and code length \( N > 1024 \). This paper presents an ASIC implementation of three decoders for polar code: successive cancellation (SC) decoder, flexible decoder and ultra-reliable decoder. These decoders are all SC based decoder, supporting list size up to 1, 8, 32 and code length up to \( 2^{15}, 2^{14}, 2^{13} \) respectively. This chip is fabricated in a 16nm TSMC FinFET technology, and can be clocked at 1 Ghz. Optimization techniques are proposed and employed to increase throughput. Experiment result shows that the throughput can achieve up to 5.16Gbps. Compared with fabricated ASIC decoder and synthesized decoder in literature, the flexible decoder achieves higher area efficiency.

Index Terms—Polar code, ASIC, decoding, SCL.

I. INTRODUCTION

Polar codes, proposed by Arikan [1], has been selected as the 5G standard. Although Polar codes with successive-cancellation (SC) decoding is proved to achieve channel capacity in the asymptotic sense, its error-correction performance is inferior to that of low-density parity-check (LDPC) or Turbo codes at short or moderate lengths. SC list (SCL) decoding, regarded as the most efficient decoding algorithm of polar codes, improves the error-correction performance but suffers from low latency and low throughput due to the serial nature of SC. Much effort has been made to optimize the decoding of Polar codes [2]–[9]. However, most works lack ASIC implementation and thus bear less practical relevance.

A couple of ASIC featuring decoders are fabricated in [10]–[12]. The chip presented in [10] implements the SC decoding algorithm; The chip presented in [11] implements the belief-propagation decoding algorithm. Both of them suffer from mediocre error-correction performance. The chip presented in [12] implements SCL decoding, but constrains the largest list size \( L_{\text{max}} = 4 \) and largest code length \( N_{\text{max}} = 1024 \), which limits its application scope.

A. Motivation and Contribution

This work is motivated by the desire to provide ASIC decoder to support polar codes research and speed up prototype building of 5G communication systems. The ASIC decoder should have low latency and high error-correction performance, and support a wide range of list sizes and code lengths. To satisfy all the desired properties, we integrated three decoders in one chip: SC decoder, flexible decoder and ultra-reliable decoder.

- SC decoder is designed for low latency and long code length with \( N = 2^{15} \);
- Flexible decoder is a SCL decoder with \( N_{\text{max}} = 2^{14} \) and \( L_{\text{max}} = 8 \). The list size of the flexible decoder can be configured during runtime;
- Ultra-reliable decoder is also a SCL decoder, designed for ultra-reliable scene with largest code length \( N_{\text{max}} = 2^{11} \) and list size \( L = 32 \).

All the decoders support any code rate. This is the first ASIC implemented SCL decoder supporting \( L > 4 \) and \( N > 1024 \).

To improve throughput, several optimization techniques are proposed. We propose a new internal log-likelihood ratio (LLR) messages storage method which can reduce 86% of the internal LLR memory. A serial list processing architecture is proposed to avoid the crossbar of LLR. This can reduce resource and improve timing performance. To improve utilization ratio of processing element (PE), we propose to decode two packages simultaneously, which can improve throughput by 54%. We also recovery decoded bit from partial-sum to save memory.

B. Outline

The rest of this paper is organized as follows. Section II gives a brief review of polar codes and SC-base decoding algorithms. The proposed ASIC architectures and optimization techniques are presented in Section III. Section IV presents the implementation results and comparison with state-of-the-art works. Section V concludes the paper.

II. POLAR CODE

An \((N, k)\) polar code has a code length \( N \) and \( k \) information bits. The code rate \( R \) is defined by \( R = k/N \). The information bits are assigned to the \( k \) most reliable sub-channels, and the remaining sub-channels are assigned by pre-defined value, typical zero—called frozen bits. The encoding of Polar code can be defined as \( c = uG \), where \( u \) is the source vector, \( G \) is the generator matrix, defined as \( G \triangleq F^\otimes n \), where \( F = \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \) is the kernel, \( \otimes \) denotes Kronecker power, and \( n = \log_2 N \).

A. SC-based Decoders

The decoding graph of SC decoder is shown in Fig. 1. The soft values propagate from right to left and the hard bits propagate from left to right. The information vector \( u \) is decoded sequentially from top to bottom. A hardware-friendly version of soft value updating is carried out in log-likelihood
ratio (LLR) domain. Two incoming LLRs \(L_{in1}\) and \(L_{in2}\) are combined to produce \(L_{out}\) with the following f-function
\[
L_{out} = \text{sign}(L_{in1} \cdot L_{in2}) \cdot \min(|L_{in1}|, |L_{in2}|).
\]
(1)
or g-function
\[
L_{out} = L_{in1} + (-1)^{\tilde{s}} \cdot L_{in2},
\]
(2)
where \(\tilde{s}\) is called partial sum (PS). For an SCL decoder, the decoding process is similar to SC decoder except that it keeps \(L\) paths. When making hard decision for each bit, \(L\) paths split into 2\(L\) paths, and the ones with smallest path metric (PM) are kept. For list size \(L\) and bit \(u_i\), the LLR of stage 0 is denoted as \(L_{0,i}^1\) and its hard decision is denoted as \(\beta_{0,i}^1\). The PM updates according to
\[
PM_{i}^{1} = \begin{cases} 
PM_{i-1}^{1}, & \text{if } u_{i} = \beta_{0,i}^1 \\
PM_{i-1}^{1} + |L_{0,i}^1|, & \text{otherwise} 
\end{cases} 
\]
(3)
After all bits are decoded, the path with the smallest PM is selected as the decoding output. To further improve error correction performance, concatenated polar code is proposed. For cyclic redundancy check (CRC) aided SCL (CA-SCL) \cite{13}, the most reliable path that passes the CRC is selected as the decoding output. For parity-check SCL (PC-SCL) \cite{14}, each parity bit is decided by its parity function rather than by the LLR.

### III. Architecture

The overview of our ASIC design is shown in Fig. 2. It mainly comprises six units: SC decoder, flexible decoder, ultra-reliable decoder, de-frozen unit, code construction unit and scheduler. Five flexible decoders are integrated in the chip to achieve high throughput. The flexible decoder and ultra-reliable decoder can be configured as SCL, CA-SCL or PC-SCL during runtime. The code construction unit generates frozen bit set for all the three decoders. This can avoid transmission of frozen bit set and support any code rate. The de-frozen unit is responsible to remove frozen bits in source vector. The data-flow is managed by input-scheduler and output-scheduler.

There are four clock domains in the chip. All the six units are clocked by “core clk”, which is generated by clock management unit (CMU). The CMU also generates “LVDS clk” for LVDS(Low Voltage Differential Signaling) sender. LVDS receiver and SPI(Serial Peripheral Interface) bus are clocked by external input clock.

The LLRs are represented in sign-and-magnitude form as in \cite{19}. We denote \(Q_{c}\) as the number of bits to represent internal LLR and channel LLR. In our ASIC design, we set \(Q_{c} = 6\) for all decoders. We denote \(Q_{PM}\) as the number of bits to represent PM in metric sorter and PM in memory, respectively. After sorting, the minimum PM will be subtracted from the PM of all list paths and the quantization of PM will be reduced from \(Q_{sort}\) to \(Q_{PM}\). Therefore, \(Q_{PM}\) of our ASIC is smaller than that of \cite{12}.

### A. Flexible decoder

Flexible decoder supports variable list size and code length, with upper limit \(L_{max} = 8\) and \(N_{max} = 2^{14}\). The architecture of flexible decoder is shown in Fig. 3. Channel LLR memory stores the received channel LLRs. Internal LLR memory stores the LLRs generated during decoding process. Good bits are information bits with higher reliability. They are stored and used to reduce path splitting as \cite{3}. In this decoder, we set \(Q_{l} = 6\), \(Q_{sort} = 7\), and \(Q_{PM} = 6\) to preserve the same error performance as a floating-point decoder. PEs are capable of performing f and g function. If the parallelism of f/g node is larger than 16, LLR processing is executed in the serial unit. Otherwise, it is executed in the parallel unit. 4-bit is decoded simultaneously in parallel unit.
by employing multi-bit decision [4]. Up to 32 rate zero nodes [2] and rate one nodes [2] in which all bits are good bits are also decoded simultaneously in parallel unit. Moreover, decoding starts from the first non-frozen bit as [12].

We propose optimization techniques to improve throughput. They are employed in our decoder and presented below.

1) LLR Memory Reduction: In a decoder chip, the internal LLR memory takes up most of the total core area. The memory size for internal LLR is reduced to

\[ MEM = L \times Q_i \times 2^{i} = LQ_i(N - 1). \]  

(4)

In a flexible decoder, we only save internal LLR for every three neighboring stages. The LLRs between these stages can be re-calculated on the fly from the stored LLRs. Therefore, the memory size for internal LLR is reduced to

\[ MEM = L \times Q_i \times 2^{i/3-1} = 0.14 \times LQ_i(N - 1). \]

(5)

We can see that almost 86% of internal LLR memory is reduced. To compensate the latency introduced by LLR re-calculation, more PEs are utilized.

2) Serial List Processing: We propose a serial list processing architecture, which executes the LLR processing of different list in serial. As far as we know, all the hardware architecture in literature [3]–[5], [9] contains L SC decoder cores and execute the LLR processing of different list paths in parallel. Due to LLR exchange among paths, this architecture requires a crossbar of LLR. The crossbar contains L L-to-1 multiplexers with complexity growing proportional to \( L^2 \).

Our serial list processing architecture executes LLR of different list one by one, thus does not require a crossbar. The LLR exchange among lists can be implemented by exchanging the address of memory. Compared to parallel architecture, serial architecture introduces no extra latency when PE quantity is the same. However, the complexity is reduced and the timing performance will significantly improve especially when list size and PE quantity is large.

At stage \( t \), only \( 2^t \) \( \tilde{f}/g \) functions need to be executed as shown in Fig. 1. Therefore, the large number of PEs in serial unit can not be fully used when \( t \leq 4 \). For these stages, we apply parallel unit to decrease the latency.

3) Double-Package Mode: Due to the serial nature of SC decoding, the PEs are idle during PM sorting period. The sorting latency is comparable with \( \tilde{f}/g \) execution latency when list size is large and multi-bit decoding is used. To improve the utilization ratio of PEs, double-package mode is applied when two packages are decoded simultaneously. When the PM of a package is sorting, the PEs are utilized to execute \( \tilde{f}/g \) function for the other package.

We define the decoding time as \( T \) when only one package is decoded in the decoder. It requires less than \( 1.3 \times T \) to decode two packages under double-package mode. This can improve the throughput by 54%.

4) Decoded-bit Recovery: In general, independent memory for \( u \) and PS are required in decoder. Their sizes are both \( LN \) bits [3]. However, the memory for \( u \) is not necessary since \( u \) is only required when decoded-bits are sent out.

Proposition 1: For SCL decoder, \( u \) can be recovered from PS after all bits are decoded.

Proof: We denote \( \hat{S}_t \) as the stored PS vector of stage \( t \). Since the serial nature of SC, only \( 2^t \) elements of \( \hat{S}_t \) will be update simultaneously and need to be stored. After all bits are decoded, the stored PS locates at the right lower triangle of decoding graph (e.g., the green PS in Fig. 1). We can infer that the final stored

\[ \hat{S}_t = u_{N-2^t+1}^{N-2^t-1} \cdot G_t, \]

(6)

where \( G_t = F^{\otimes t} \). A characteristic of generator matrix \( G \) is \( G = G^{-1} \). So, we can induce that

\[ u_{N-2^t+1}^{N-2^t-1} = \hat{S}_t \cdot G_t^{-1} = \hat{S}_t \cdot G_t. \]

(7)

It can be seen as a polar encoding on \( \hat{S}_t \). According to (7), \( u_0^{N-2} \) can be obtained. \( u_{N-1} \) can be obtained when the last bit is decoded. Thus, \( u \) can be recovered after all bits are decoded.

The polar encoding can be implemented by bitwise XOR. It takes much less chip area that \( LN \) bits memory. Furthermore, the encoding on PS can be executed in parallel with decoding of next package, has no effect on throughput. Therefore, we use \( L N \) bits memory to save PS and \( N \) bits memory to save recovered \( u \). Compared with general method, we can save \((L-1)N\) bits memory.

B. SC Decoder

The SC decoder is a simplified version of flexible decoder without path metric management. The SC decoder exploits SSC decoding algorithm [2] and supports code length \( N \) = 2\(^{15} \). Due to the long code length, we set \( Q_i = 7 \) to avoid error-correction performance loss.

C. Ultra-reliable Decoder

Aiming at \( L = 32 \), we design an ultra-reliable decoder based on flexible decoder. In the decoder, \( Q_{sort} \) and \( Q_{PM} \) is the same as those in the flexible decoder, \( Q_i = 7 \) at stage 0 and \( Q_i = 6 \) at other stages. The main differences between ultra-reliable decoder and flexible decoder are shown below:

1) Serial List Processing: There is a semi-parallel unit besides serial unit and parallel unit in ultra-reliable decoder. The number of PE, subjecting to the number of dependent nodes, can not be added arbitrarily to decrease the latency. Due to the large list size and the number of PE, the latency of serial processing deceases the throughput significantly at some stages. Therefore, four list paths of stage \( 4 \sim 3 \) are executed in parallel. These stages are called semi-parallel unit.

2) LLR Memory Reduction: Larger list size requires larger memory size for internal LLR according to (4). Therefore, we save internal LLR for every 4 neighboring stages to save more memory in ultra-reliable decoder. However, four LLR copies of stage 5 need to be stored for supporting semi-parallel unit and increasing the throughput. In total, almost 87% of internal LLR memory are reduced compared with (4).
incurs performance loss less than 0.1dB.

results are also plotted in Fig. 6. It can be seen that quantization Gaussian noise channel. As a reference, the floating-point shift keying (QPSK) and transmitted over an additive white noise channel. The chip area is $2 \times 3 \text{mm}^2$ with $f_{\text{clk}} = 1 \text{GHz}$, where $f_{\text{clk}}$ is the highest frequency of “core clk”. The micrograph and photograph of the chip is shown in Fig. 4 and Fig. 5.

Fig. 4. The micrograph of the decoder ASIC.

Fig. 5. The photograph of the decoder ASIC.

3) Multi-bit Parallel Processing: Multi-bit decision is also adopted in ultra-reliable decoder. However, only 2-bit and up to 4 rate 0/1 nodes can be decoded simultaneously.

4) Double-Package Mode: Double-package mode is not supported to save memory.

IV. IMPLEMENTATION RESULTS AND MEASUREMENT

This ASIC is fabricated in a 16nm TSMC FinFET technology. The chip area is $6 \text{mm}^2$ with $f_{\text{clk}} = 1 \text{GHz}$, where $f_{\text{clk}}$ is the highest frequency of “core clk”, the micrograph and photograph of the chip is shown in Fig. 4 and Fig. 5.

A. Measurement Setup

To test the decoder ASIC, we design a printed circuit board (PCB) which integrates the decoder ASIC and a Xilinx xc7vx690t FPGA. The PCB can be inserted into the PCIe slot of a computer. Test data is generated on the computer, and send to FPGA throughput PCIe. The FPGA acts as a bridge between computer and decoder ASIC.

B. Error-Correction Performance and Throughput

The frame error rate (FER) under various list sizes, code length, and code rates are tested by the designed PCB with 24 bits CRC, and plotted in Fig. 6. The codewords are randomly generated, modulated with quadrature phase-shift keying (QPSK) and transmitted over an additive white Gaussian noise channel. As a reference, the floating-point results are also plotted in Fig. 6. It can be seen that quantization incurs performance loss less than 0.1dB.

The measured throughputs are summarized in Table I. The throughput $(T/P)$ is defined by

$$T/P = k \times f_{\text{clk}}/T,$$

(8)

where $T$ is the decoding latency. The highest throughput is 5.164 Gbps when code rate $R = 8/9$. The throughput of flexible decoder is even higher than the SC decoder since 5 flexible decoder cores are implemented. In terms of area efficiency, SC decoder is the highest one in the three decoder. Due to the large list size, the throughput of ultra-reliable decoder is much lower than the other two decoders.

C. Comparison With State-of-the-Art Fabricated ASICs

The comparison with state-of-the-art fabricated ASICs is shown in Table II. Our SC decoder supports $N = 2^{15}$, but SC decoder in [12] [10] only supports $N = 2^{10}$. Therefore, it is hard to give a precise comparison for these SC decoders in the table. The flexible decoder and [12] run at the same code rate and length, but the former runs with larger list size ($L = 8$) and can support larger code length. Even though, the area efficiency of flexible decoder is much higher than the scaled result of [12]. As for ultra-reliable decoder, no fabricated ASIC decoder with $L = 32$ has been reported in literature.

Table I Measured Throughput

| Code Rate | Throughput (Mbps) |
|-----------|-------------------|
| 1/4       | 1649              |
| 1/2       | 2599              |
| 2/3       | 3351              |
| 3/4       | 3821              |
| 8/9       | 4786              |

To further evaluate our architecture, we present the synthesis result of the flexible decoder and state-of-the-art decoders in Table III. We re-synthesize one flexible decoder and set $N_{\text{max}} = 1024$ for fair comparison. The $f_{\text{clk}}$ increases to 1.1GHz. The scaled result shows that the flexible decoder outperforms state-of-the-art decoders in terms of area efficiency.

V. CONCLUSION

In this paper, we present an ASIC implementation of three SC-based decoders for polar code in a 16nm TSMC FinFET technology. To our knowledge, this is the first ASIC implemented SCL decoder supporting $L > 4$ and $N > 1024$. To improve throughput, several optimization techniques are proposed. Measurement result shows that throughput of the SC decoder, flexible decoder and ultra-reliable decoder can achieve up to 5.16 Gbps, 4.79 Gbps and 91 Mbps, respectively. Compared with fabricated ASIC decoder and synthesized decoder in literature, the flexible decoder achieves higher area efficiency.

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