Chapter

Gate-All-Around FETs: Nanowire and Nanosheet Structure

Jun-Sik Yoon, Jinsu Jeong, Seunghwan Lee, Junjong Lee and Rock-Hyun Baek

Abstract

DC/AC performances of 3-nm-node gate-all-around (GAA) FETs having different widths and the number of channels ($N_{ch}$) from 1 to 5 were investigated thoroughly using fully-calibrated TCAD. There are two types of GAAFETs: nanowire (NW) FETs having the same width ($W_{NW}$) and thickness of the channels, and nanosheet (NS) FETs having wide width ($W_{NS}$) but the fixed thickness of the channels as 5 nm. Compared to FinFETs, GAAFETs can maintain good short channel characteristics as the $W_{NW}$ is smaller than 9 nm but irrespective of the $W_{NS}$. DC performances of the GAAFETs improve as the $N_{ch}$ increases but at decreasing rate because of the parasitic resistances at the source/drain epi. On the other hand, gate capacitances of the GAAFETs increase constantly as the $N_{ch}$ increases. Therefore, the GAAFETs have minimum RC delay at the $N_{ch}$ near 3. For low power applications, NWFETs outperform FinFETs and NSFETs due to their excellent short channel characteristics by 2-D structural confinement. For standard and high performance applications, NSFETs outperform FinFETs and NWFETs by showing superior DC performances arising from larger effective widths per footprint. Overall, GAAFETs are great candidates to substitute FinFETs in the 3-nm technology node for all the applications.

Keywords: gate-all-around, nanowire, nanosheet, field-effect transistors, fin, RC delay, parasitic resistance, parasitic capacitance

1. Introduction

Gate-all-around (GAA) is a widely-using structure such as logic field-effect transistor (FET) due to its excellent short channel characteristics [1–6] or its high surface-to-volume ratio [7, 8], 3-D NAND flash memory for bit-cost scalability [9, 10], photodiode due to its waveguide effect [11, 12], and gas sensor due to its high physical fill factor or surface-to-volume ratio [13, 14]. Especially for logic applications, GAAFETs have been introduced by attaining good gate electronics and increasing current drivability under the same active area.

Currently, fin-shaped FETs (FinFETs) have been scaled down to 10-nm node [15] and further to 5-nm node [16] by forming ultra-sharp fin for high current drivability while maintaining gate-to-channel controllability. GAAFETs are possibly showing great potential to substitute FinFETs in the following technology node, and the performance comparisons between FinFETs and GAAFETs have been investigated [3–6, 17]. But more detailed analysis between FinFETs and GAAFETs...
is needed to set the device guideline by considering fine TCAD calibration and middle-of-line levels.

Therefore, in this work, DC/AC performances of 3-nm-node GAAFETs were investigated using fully-calibrated TCAD platform. By changing the GAA geometries, we found optimal GAA structure to minimize the RC delay for three different applications such as low power (LP), standard performance (SP), and high performance (HP) applications.

2. Device structure and simulation methods

All the simulation works were performed using Sentaurus TCAD [18]. Drift diffusion transport equations were calculated self-consistently with Poisson and electron/hole continuity equations. Density-gradient model was adopted for the quantum confinement of carriers within the channel. Slotboom bandgap narrowing model was used to consider the doping-dependent energy bandgap. Mobility models include Lombardi for the mobility degradation at the channel/oxide interface, inversion and accumulation layer model for impurity, phonon, and surface roughness scatterings, and low-field ballistic model for quasi-ballistic effects in ultra-short gate length (Lg). Shockley-Read-Hall, Auger, and Hurkx band-to-band tunneling recombination models were adopted. Deformation potential model was used to consider the stress-induced energy bandgap, effective mass, and effective density-of-states. All these physical models were used equivalently in [19, 20].

Figure 1 shows the schematic diagrams of FinFETs and three-stacked GAAFETs. FinFETs have highly-doped punch-through-stopper (PTS) at $2 \times 10^{18}$ and $4 \times 10^{18}$ cm$^{-3}$ for NFETs and PFETs, respectively, in order to prevent the sub-fin leakage currents at off state [21, 22]. GAAFETs, on the other hand, have buried oxide (BOX) layer beneath the source/drain (S/D) regions without PTS so that the bottom leakage currents are completely blocked [1, 23]. Bulk FinFETs can adopt the BOX layer according to [24], but the conventional device structure

Figure 1. Schematic diagrams of FinFETs and GAAFETs. 2-D cross-sections of nanosheet and nanowire channels were also specified to the right.
was considered in this work. S/D doping concentrations of the n-type and p-type devices are $2 \times 10^{20}$ and $4 \times 10^{20} \text{ cm}^{-3}$, respectively. Interfacial layer (IL), HfO$_2$, and low-k spacer regions have the dielectric constants of 3.9, 22.0, and 5.0, respectively. Contact resistivity at S/D and silicide interface is fixed to $10^{-9} \text{ } \Omega \cdot \text{cm}^2$ [25]. Equivalent oxide thickness (EOT) is 1.0 nm, which consists of 0.7-nm-thick IL and 1.7-nm-thick HfO$_2$.

Table 1 shows the geometrical parameters and values of 3-nm-node FinFETs and GAAFETs. Contacted poly pitch (CPP) and fin pitch (FP) are 42 and 21 nm, following 3-nm technology node [5]. There are two types of GAAFETs: nanowire FETs (NWFETs) having the same width and thickness as W$_{NW}$, and nanosheet FETs (NSFETs) having thin NS thickness ($T_{NS}$) of 5 nm but wide NS width ($W_{NS}$) as 10, 20, 30, 40, and 50 nm. The number of NW or NS channels ($N_{ch}$) is varied as 1, 2, 3, 4, and 5.

Table 1 shows the geometrical parameters and values of 3-nm-node FinFETs and GAAFETs. Contacted poly pitch (CPP) and fin pitch (FP) are 42 and 21 nm, following 3-nm technology node [5]. There are two types of GAAFETs: nanowire FETs (NWFETs) having the same width and thickness as W$_{NW}$, and nanosheet FETs (NSFETs) having thin NS thickness ($T_{NS}$) of 5 nm but wide NS width ($W_{NS}$) as 10, 20, 30, 40, and 50 nm. The number of NW or NS channels ($N_{ch}$) is varied as 1, 2, 3, 4, and 5.

Table 1. Geometrical parameters and values of FinFETs and GAAFETs.

| Geometrical parameters | Values |
|------------------------|--------|
| CPP                    | Contacted poly pitch | 42 nm |
| FP                     | Fin pitch            | 21 nm |
| NP                     | Nanowire/sheet pitch | $W_{NW}$ or $W_{NS}$ + 16 nm |
| $L_g$                  | Gate length          | 12 nm |
| $L_{sp}$               | Spacer length        | 5 nm  |
| $W_{fin}$              | Fin width            | 5 nm  |
| $H_{fin}$              | Fin height           | 46 nm |
| $W_{NW}$               | Nanowire width       | 5, 6, 7, 8, 9, 10 nm |
| $W_{NS}$               | Nanosheet width      | 10, 20, 30, 40, 50 nm |
| $T_{NS}$               | Nanosheet thickness  | 5 nm  |
| $T_{sp}$               | Nanowire/sheet spacing | 10 nm |
| $N_{ch}$               | The number of channels | 1, 2, 3, 4, 5 |
3. Results and discussion

3.1 DC performances of NWFETs and NSFETs

Figure 3 shows the $I_{ds}$ of all the GAAFETs having different $W_{NW}$ or $W_{NS}$ at the fixed $N_{ch}$ of 3 at the drain voltages ($V_{ds}$) of 0.70 V. It is not shown in this figure, but the $I_{ds}$ increases generally as the $W_{NW}$ or $W_{NS}$ increases irrespective of $N_{ch}$. As the $W_{NW}$ increases, the $I_{ds}$ shifts leftward and the gate-induced drain leakage (GIDL) increases by losing the gate-to-channel controllability [27]. P-type NWFETs have larger GIDL than n-type NWFETs due to larger S/D doping penetrations into the channel for p-type devices. On the other hand, NSFETs have small GIDL and $I_{ds}$ shifts as thin $T_{NS}$ of 5 nm forms 1-D structural confinement and maintains good short channel characteristics. To the following, there are three applications at different off-state currents ($I_{off}$): LP at the $I_{off}$ of 100 pA/μm, SP at the $I_{off}$ of 10 nA/μm, and HP at the $I_{off}$ of 100 nA/μm [28]. These values were normalized to NP.

Figure 4 shows SS and DIBL of all the devices. Threshold voltages ($V_{th}$) and SS are extracted at the constant current of $W_{eff}/L_g 	imes 10^8$ A, where $W_{eff}$ is the effective width equal to $2 \times H_{fin} + W_{fin}$ for FinFETs, $4 \times W_{NW} \times N_{ch}$ for NWFETs, and $(2 \times W_{NS} + 2 \times T_{NS}) \times N_{ch}$ for NSFETs. DIBL is calculated as the difference of the $V_{th}$ at two different $V_{ds}$ of 0.05 and 0.70 V for n-type (−0.05 and −0.70 V for p-type) devices [29]. NWFETs degrade the short channel characteristics much than FinFETs as the $W_{NW}$ is 9 and 10 nm. NSFETs, on the other hand, have smaller SS and DIBL than FinFETs even as the $W_{NS}$ increases up to 50 nm because the gate-to-channel controllability is maintained by GAA structure and thin $T_{NS}$ of 5 nm. But when the NWFETs have ultra-small $W_{NS}$ of 5 or 6 nm, 2-D structural confinement decreases the SS and DIBL greatly, which would be preferable for LP applications. It is not shown in this figure, but the SS and DIBL are independent of $N_{ch}$.

Figure 5 summarizes the effective currents ($I_{eff}$) of n-type (top) and p-type (bottom) GAAFETs having different $W_{NW}$ (or $W_{NS}$) and $N_{ch}$. $I_{eff}$ was calculated using two $I_{ds}$ at different $V_{ds}$ and gate voltages ($V_{gs}$) as

$$I_{eff} = (I_H - I_L) / \ln \left( \frac{I_H}{I_L} \right)$$

(1)
where $I_H = I_d$ ($V_{gs} = V_{DD}$, $V_{ds} = V_{DD}/2$) and $I_L = I_d$ ($V_{gs} = V_{DD}/2$, $V_{ds} = V_{DD}$) [30], and $V_{DD}$ is the operation voltage fixed to 0.7 V. All the $I_{off}$ were normalized to the NP, and the $I_{off}$ were fixed to 10 nA/μm for SP applications. GAAFETs need to have at least the $N_{ch}$ of 3 to outperform the FinFETs. As the $W_{NW}$ is 9 nm, both n-type and p-type NWFETs suffer from short channel effects (SCEs) and thus have smaller $I_{eff}$ than the devices having smaller $W_{NW}$ in spite of larger $W_{eff}$. NSFETs, on the other hand, have larger $I_{eff}$ as the $W_{NS}$ is larger as the SCEs are reduced by thin $T_{NS}$ of 5 nm. But even though small same SS and DIBL are maintained for all the $N_{ch}$, the increasing rate of $I_{eff}$ as a function of $N_{ch}$ decreases as $N_{ch}$ increases.

Figure 6 shows the S/D parasitic resistance ($R_{sd}$) of the GAAFETs having the $W_{NW}$ or 7 nm and the $W_{NS}$ of 30 nm as a function of $N_{ch}$. Other $W_{NW}$ and $W_{NS}$ have the same $R_{sd}$ trends and thus are not shown in this work. $R_{sd}$ was possibly extracted using $Y$-function method due to the linearity of $Y$-function at high $V_{gs}$ [31]. As the
Nanowires - Recent Progress

N$_{ch}$ increases, $R_{sd}$ of the GAAFETs decrease but at decreasing rate. Furthermore, $R_{sd}$ becomes saturated as the N$_{ch}$ is 3 or 4. This phenomena can be explained by 2-D schematic diagrams shown in the right of Figure 6. Since the S/D contacts reside at the top of the S/D epi, current paths start from the top toward the channels at the bottom. As the N$_{ch}$ increases, longer current paths are needed to flow the bottom-side channels, facing more $R_{sd}$ components at the S/D epi. Thus, increasing the N$_{ch}$ beyond 3 or 4 does not help DC performance improvements greatly.

3.2 AC performances of NWFETs and NSFETs

Figure 7 summarizes the gate capacitances ($C_{gg}$) of all the GAAFETs. The $C_{gg}$ is extracted at the $V_{gs}$ and the $V_{ds}$ of $V_{DD}$. Generally, $C_{gg}$ increases as the W$_{NW}$ (or W$_{NS}$) or N$_{ch}$ increases due to the increased W$_{eff}$. PFETs have larger $C_{gg}$ than NFETs due to larger S/D doping concentrations and penetrations into the channels. Different
Gate-All-Around FETs: Nanowire and Nanosheet Structure
DOI: http://dx.doi.org/10.5772/intechopen.94060

from the $I_{eff}$ trends, the GAAFETs have $N_{ch}$ smaller than 3 to outperform the FinFETs, thus there are performance trade-offs between $I_{eff}$ and $C_{gg}$ as a function of $N_{ch}$. Furthermore, the increasing rate of $C_{gg}$ as a function of $N_{ch}$ is constant while the increasing rate of $I_{eff}$ as a function of $N_{ch}$ decreases, which would degrade the RC delay ($= I_{eff}V_{DD}/C_{gg}$) as the $N_{ch}$ increases.
Figure 8 shows the $C_{gg}$ and parasitic capacitances ($C_{para}$) of the GAAFETs varying $N_{ch}$ and $W_{NW}$ (or $W_{NS}$). $C_{para}$ is extracted at off-state for SP applications. For all the cases, PFETs have larger $C_{para}$ than NFETs due to larger S/D doping and penetrations into the channels [20]. At the fixed $N_{ch}$ of 3, larger $W_{NW}$ or $W_{NS}$, except for p-type NWFETs, decreases the $C_{para}/C_{gg}$ because the proportion of the channels out of the metal gate increases. For the same reason, larger $N_{ch}$ decreases the $C_{para}/C_{gg}$. Large $C_{para}/C_{gg}$ at the $W_{NW}$ of 9 nm for NFETs is because large SS forms on state before reaching strong inversion region.

Figure 9 shows the S/D doping profiles of NFETs (top) and PFETs (bottom) having different $W_{NW}$ at the fixed $N_{ch}$ of 3. In general, NFETs have larger doping concentrations in the middle of channels than PFETs because the Ge intermixing within multi-stacked Si/Si$_{0.7}$Ge$_{0.3}$ layers increases the Ge concentration at the channels and assists more phosphorus dopants diffusing into the channels while it segregates boron dopants [32–34]. Both NFETs and PFETs increase the doping concentrations in the middle of channels as the $W_{NW}$ increases because the dopant segregations near the low-k spacer regions decrease [35]. But PFETs increase the doping concentrations in the middle of channels much due to smaller Ge intermixing for larger $W_{NW}$. This great increase of the doping concentrations in the middle of channels increases the $C_{para}/C_{gg}$ for p-type NWFETs (as shown in Figure 8).

Figure 10 finalizes the RC delay of all the GAAFETs for LP, SP, and HP applications. N-type FinFETs have smaller RC delay than p-type FinFETs for all the applications due to better short channel characteristics, greater $I_{eff}$ (as shown in Figure 5) and smaller $C_{gg}$ (as shown in Figure 8). For LP applications, n-type GAAFETs having

![Figure 9](image_url)

**Figure 9.**
S/D doping profiles of NFETs (top) and PFETs (bottom) having different $W_{NW}$ at the fixed $N_{ch}$ of 3. Doping concentrations in the middle of top-side channels are also specified.
small $W_{NW}$ equal to 5 or 6 nm can outperform n-type FinFETs by decreasing SS and DIBL critically. But as the $N_{ch}$ is 1 (or 5), the $I_{eff}$ decreases greatly (or the $C_{gg}$ increases greatly), thus degrading the RC delay. On the other hand, p-type GAAFETs have more $W_{NW}$ or $W_{NS}$ options to outperform p-type FinFETs because boron dopants of the GAAFETs are segregated by Si/Si$_{0.7}$Ge$_{0.3}$ intermixing and have more abrupt S/D doping profile than p-type FinFETs. For LP applications, both n- and p-type GAAFETs have the minimum RC delay at the $W_{NW}$ of 5 nm and the $N_{ch}$ of 4. For both SP and HP applications, both n- and p-type GAAFETs have the minimum RC delay at the $W_{NS}$ of 50 nm and the $N_{ch}$ of 3. As the $W_{NS}$ increases beyond 50 nm, RC delay decrease but a little (as shown in Appendix). All these RC delay are achieved by enhancing the $I_{eff}$ rather than the $C_{gg}$. To outperform the FinFETs, therefore, GAAFETs should be NWFETs, showing outstanding short channel characteristics, for LP applications and NSFETs, showing superior DC performance, for SP and HP applications.

4. Conclusion

3-nm-node GAAFETs have been analyzed by changing $W_{NW}$ (or $W_{NS}$) and $N_{ch}$ using fully-calibrated TCAD. Compared to FinFETs, GAAFETs have smaller and
SS and DIBL as the $W_{NW}$ is smaller than 9 nm but irrespective of the $W_{NS}$. Both $I_{eff}$ and $C_{gg}$ of the GAAFETs increase as the $N_{ch}$ increases, but the increasing rate of $I_{eff}$ decreases due to the increase of $R_{sd}$ at the longer S/D epi. The increasing rate of $C_{gg}$, on the other hand, is almost constant. Because of these phenomena, Minimum RC delay are formed at the middle $N_{ch}$ of 3 or 4. The NWFETs having the $W_{NW}$ of 5 or 6 nm achieve smaller RC delay than the FinFETs by achieving better gate electronics for LP applications, whereas the NSFETs having the $W_{NS}$ of 40 or 50 nm increase the $L_{eff}$ greatly and thus decrease the RC delay for SP and HP applications. Overall, GAAFETs are possible candidates to substitute FinFETs in the 3-nm technology node for all the applications by adopting different $W_{NW}$ or $W_{NS}$.

Conflict of interest

The authors declare no conflict of interests.

Appendices and nomenclature

Figure A1 shows the DC/AC performances of the NSFETs as the $W_{NS}$ increases from 40 to 100 nm. Minimum RC delay are formed at the $W_{NS}$ of 50 nm and the $N_{ch}$ of 3 as shown in Figure 10, but much smaller RC delay can be attained as the $W_{NS}$ increases to 100 nm by increasing the $I_{eff}$ rather than the $C_{gg}$ even though larger $W_{NS}$ extends the device area. For the most, RC delay decrease by 5.4% for PFETs as the $W_{NS}$ increases from 40 to 100 nm.
Author details

Jun-Sik Yoon, Jinsu Jeong, Seunghwan Lee, Jun jong Lee and Rock-Hyun Baek*
Electrical Engineering, Pohang University of Science and Technology, Pohang,
Republic of Korea

*Address all correspondence to: rh.baek@postech.ac.kr

IntechOpen

© 2020 The Author(s). Licensee IntechOpen. This chapter is distributed under the terms of the Creative Commons Attribution License (http://creativecommons.org/licenses/by/3.0), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.
References

[1] Loubet N, Hook T, Montanini P, Yeung C.-W, Kanakasabapathy S, Guillorn M, Yamashita T, Zhang J, Miao X, Wang J, Young A, Chao R, Kang M, Liu Z, Fan S, Hamieh B, Sieg S, Mignot Y, Xu W, Seo S.-C, Yoo J, Mochizuki S, Sankarapandian M, Kwon O, Carr A, Greene A, Park Y, Froujgie J, Galatage R, Bao R, Shearer J, Conti R, Song H, Lee D, Kong D, Xu Y, Arceo A, Bi Z, Xu P, Muthinti R, Li J, Wong R, Brown D, Oldiges P, Wu T, Gupta D, Lian S, Divakaruni R, Goy T, Labelle C, Lee S, Paruchuri V, Bu H, Khare M. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In: Proceedings of 2017 Symposium on VLSI Technology, Kyoto, 2017, pp. T230-T231, DOI: 10.23919/VLSIT.2017.7998183.

[2] Yoon J.-S, Rim T, Kim J, Meyyappan M, Baek C.-K, and Jeong Y.-H. Vertical gate-all-around junctionless nanowire transistors with asymmetric diameters and underlap lengths. Applied Physics Letters. 2014;105:102105-1-4. DOI: 10.1063/1.4895030.

[3] Lee Y. M, Na M. H, Chu A, Young A, Hook T, Liebmann L, Nowak E. J, Baek S. H, Sengupta R, Trombley H, and Miao X. Accurate performance evaluation for the horizontal nanosheet standard-cell design space beyond 7nm technology. In: Proceedings of 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2017, pp. 29.3.1-29.3.4, DOI: 10.1109/IEDM.2017.8268474.

[4] Barraud S, Lapras V, Previtali B, Samson M. P, Lacord J, Martinie S, Jaud M.-A, Athanasiou S, Troizion F, Rozeau O, Hartmann J. M, Vizioz C, Comboroure C, Andrieu F, Barbé J. C, Vinet M, Ernst T. Performance and design considerations for gate-all-around stacked-nanowires FETs. In: Proceedings of 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2017, pp. 29.2.1-29.2.4, DOI: 10.1109/IEDM.2017.8268473.

[5] Yakimets D, Garcia Bardon M, Jang D, Schuddinck P, Sherazi Y, Weckx P, Miyaguchi K, Parvais B, Raghavan P, Spessot A, Verkest D, Mocuta A. Power aware FinFET and later nanosheet FET targeting for 3nm CMOS technology. In: Proceedings of 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2017, pp. 20.4.1-20.4.4, doi: 10.1109/IEDM.2017.8268429.

[6] Song S. C, Colombeau B, Bauer M, Moroz V, Lin X-W, Asenov P, Sherlekar D, Choi M, Huang J, Cheng B, Chidambaram C, Natarajan S. 2nm node: benchmarking FinFET vs nano-slab transistor architectures for artificial intelligence and next gen smart mobile devices. In: Proceedings of 2019 Symposium on VLSI Technology, Kyoto, Japan, 2019, pp. T206-T207. DOI: 10.23919/VLSIT.2019.8776478.

[7] Yoon J.-S, Kim K, Baek C.-K. Core-shell homojunction silicon vertical nanowire tunneling field-effect transistors. Scientific Reports. 2017;7:41142-1-9. DOI: 10.1038/srep41142.

[8] Yoon J.-S, Kim K, Meyyappan M, Baek C.-K. Bandgap engineering and strain effects of core-shell tunneling field-effect transistors. IEEE Transactions on Electron Devices. 2018;65:277-281. DOI: 10.1109/TED.2017.2767628.

[9] Tanaka H, Kido M, Yahashi K, Oomura M, Katsumata R, Kito M, Fukuzumi Y, Sato M, Nagata Y, Matsuoka Y, Iwata Y, Aochi H, Nitayama A. Bit cost scalable technology with punch and plug process for ultra high density flash memory.
In: Proceedings of 2007 IEEE Symposium on VLSI Technology, Kyoto, 2007, pp. 14-15. DOI: 10.1109/VLSIT.2007.4339708.

[10] Kim J, Hong A. J, Kim S. M, Song E. B, Park J. H, Han J, Choi S, Jang D, Moon J.-T, Wang K. L. Novel vertical-stacked-array-transistor (VSAT) for ultra-high-density and cost-effective NAND flash memory devices and SSD (solid state drive). In: Proceedings of 2009 Symposium on VLSI Technology, Honolulu, HI, 2009, pp. 186-187.

[11] Seo K, Wober M. Steinvurzel P, Schonbrun E, Dan Y, Ellenbogen T, Crozier K. B. Multicolored vertical silicon nanowires. Nano Letters. 2011;11:1851-1856. DOI: 10.1021/nl200201b.

[12] Yoon J.-S, Kim K, Meyyappan M, Baek C.-K. Optical characteristics of silicon-based asymmetric vertical nanowire photodetectors. IEEE Transactions on Electron Devices. 2017;64:2261-2266. DOI: 10.1109/TED.2017.2682878.

[13] Kwon H, Yoon J.-S, Lee Y, Kim D. Y, Baek C.-K, Kim J. K. An array of metal oxides nanoscale hetero p-n junctions toward designable and highly-scalable gas sensors. Sensors and Actuators B: Chemical. 2018;255:1663-1670. DOI: 10.1016/j.snb.2017.08.173.

[14] Lee Y, Kwon H, Yoon J.-S, Kim J. K. Overcoming ineffective resistance modulation in p-type NiO gas sensor by nanoscale Schottky contacts. Nanotechnology. 2019;30:115501-1-6. DOI: 10.1088/1361-6528/aaf957.

[15] Auth C, Aliyarukunj A, Asoro M, Bergstrom D, Bhagwat V, Birdsell J, Bisnik N, Buehler M, Chikarmane V, Ding C, Fu Q, Gomez H, Han W, Hanken D, Haran M, Hattendorf M, Heussner R, Hiramatsu H, Ho B, Jaloviar S, Jin I, Joshi S, Kirby S, Kosaraju S, Kothari H, Leatherman G, Lee K, Leibl, Madhavan A, Marla K, Meyer H, Mule T, Parker C, Parthasarathy S, Pelto C, Pipes L, Post I, Prince M, Rahman A, Rajamani S, Saha A, Dacuna Santos J, Sharma M, Sharma V, Shin J, Sinha P, Smith P, Sprinkle M, St. Amour A, Staus C, Suri R, Towner D, Tripathi A, Tura A, Ward C, Yeoh A. A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects. In: Proceedings of 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2017, pp. 29.1.1-29.1.4. DOI: 10.1109/IEDM.2017.8268472.

[16] Yeap G. Lin S. S, Chen Y. M, Shang H. L, Wang P. W, Lin H. C, Peng Y. C, Sheu J. Y, Wang M, Chen X, Yang B. R, Lin C. P, Yang F. C, Leung Y. K, Lin D. W, Chen C. P, Yu K. F, Chen D. H, Chang C. Y, Chen H. K, Hung P, Hou C. S, Cheng Y. K, Chang J, Yuan L, Lin C. K, Chen C. C, Yeo Y. C, Tsai M. H, Lin H. T, Chui C. O, Huang K. B, Chang W, Lin H. J, Chen K. W, Chen R, Sun S. H, Fu Q, Yang H. T, Chiang H. T, Yeh C. C, Lee T. L, Wang C. H, Shue S. L, Wu C. W, Lu R, Lin W. R, Wu J, Lai F, Wu Y. H, Tien B. Z, Huang Y. C, Lu L. C, He Jun, Ku Y, Lin J, Cao M, Chang T. S, Jang S. M. 5nm CMOS production technology platform featuring full-fledged EUV, and high mobility channel FinFETs with densest 0.021μm² SRAM cells for mobile SoC and high performance computing applications. In: Proceedings of 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 36.71-36.74. DOI: 10.1109/IEDM19573.2019.8993577.

[17] Yoon J.-S, Jeong J, Lee S, Baek R.-H. Systematic DC/AC performance benchmarking of sub-7-nm node FinFETs and nanosheet FETs. IEEE Journal of the Electron Devices Society. 2018;6: 942-947. DOI: 10.1109/JEDS.2018.2866026.
[18] Synopsys Inc., Mountain View, CA, Version O-2018.06, 2018.

[19] Yoon J.-S, Jeong J, Lee S, Baek R.-H. Multi-Vth strategies of 7-nm node nanosheet FETs with limited nanosheet spacing. IEEE Journal of the Electron Devices Society. 2018;6:861-865. DOI: 10.1109/JEDS.2018.2859799.

[20] Yoon J.-S, Jeong J, Lee S, Baek R.-H. Optimization of nanosheet number and width of multi-stacked nanosheet FETs for sub-7-nm node system on chip applications. Japanese Journal of Applied Physics. 2019;58:SBBA12-1-5. DOI: 10.7567/1347-4065/ab0277.

[21] Jeong J, Yoon J.-S, Lee S, Baek R.-H. Comprehensive analysis of source and drain recess depth variations on silicon nanosheet FETs for sub 5-nm node SoC application. IEEE Access. 2020;8:35873-35881. DOI: 10.1109/ACCESS.2020.2975017.

[22] Yoon J.-S, Jeong J, Lee S, Baek R.-H. Sensitivity of source/drain critical dimension variations for sub-5-nm node fin and nanosheet FETs. IEEE Transactions on Electron Devices. 2020;67:258-262. DOI: 10.1109/TED.2019.2951671.

[23] Yoon J.-S, Jeong J, Lee S, Baek R.-H. Punch-through-stopper free nanosheet FETs with crescent inner-spacer and isolated source/drain. IEEE Access. 2019;7:38593-38596. DOI: 10.1109/ACCESS.2019.2904944.

[24] Yoon J.-S, Jeong J, Lee S, Baek R.-H. Bottom oxide bulk FinFETs without punch-through-stopper for extending toward 5-nm node. IEEE Access. 2019;7:75762-75767. DOI: 10.1109/ACCESS.2019.2920902.

[25] Wu H, Gluschenkov O, Tsutsui G, Niu C, Brew K, Durfee C, Prindle C, Kamineni V, Mochizuki S, Lavoie C, Nowak E, Liu Z, Yang J, Choi S, Demarest J, Yu L, Carr A, Wang W, Strane J, Tsai S, Liang Y, Amanapu H, Saraf I, Ryan K, Lie F, Kleemeier W, Choi K, Cave N, Yamashita T, Knorr A, Gupta D, Haran B, Guo D, Bu H, Khare M. Parasitic resistance reduction strategies for advanced CMOS FinFETs beyond 7nm. In: Proceedings of 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2018, pp. 35.4.1-35.4.4. DOI: 10.1109/IEDM.2018.8614661.

[26] Yoon J.-S, Lee S, Lee J, Jeong J, Yun H, Kang B, Baek R.-H. Source/Drain patterning FinFETs as solution for physical area scaling toward 5-nm node. IEEE Access. 2019;7:172290-172295. DOI: 10.1109/ACCESS.2019.2956503.

[27] Yoon J.-S, Kim K, Rim T, Baek C.-K. Performance and variations induced by single interface trap of nanowire FETs at 7-nm node. IEEE Transactions on Electron Devices. 2017;64:339-345. DOI: 10.1109/TED.2016.2633970.

[28] International Roadmap for Devices and Systems (IRDS), 2020 Edition. Available from: https://irds.ieee.org/editions/2020.

[29] Bangsaruntip S, Cohen G. M, Majumdar A, Zhang Y, Engelmann S. U, Fuller N. C. M, Gignac L. M, Mittal S, Newbury J. S, Guillorn M, Barwicz T, Sekaric L, Frank M. M, Sleight J. W. High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling. In: Proceedings of 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, 2009, pp. 1-4. DOI: 10.1109/IEDM.2009.5424364.

[30] Na M. H, Nowak E. J, Haensch W, Cai J. The effective drive current in CMOS inverters. In: Proceedings of Digest. International Electron Devices Meeting, San Francisco, CA, USA, 2002, pp. 121-124. DOI: 10.1109/IEDM.2002.1175793.
[31] Baek R.-H, Baek C.-K, Jung S.-W, Yeoh Y. Y, Kim D.-W, Lee J.-S, Kim D. M, Jeong Y.-H. Characteristics of the series resistance extracted from Si nanowire FETs using the Y-function technique. IEEE Transactions on Nanotechnology. 2010;9:212-217. DOI: 10.1109/TNANO.2009.2028024.

[32] Zangenberg N. R, Fage-Pedersen J, Lundsgaard Hansen J, Nylandsted Larsen A. Boron and phosphorus diffusion in strained and relaxed Si and SiGe. Journal of Applied Physics. 2003;94:3883-3890. DOI: 10.1063/1.1602564.

[33] Jeong J, Yoon J.-S, Lee S, Baek R.-H. Threshold voltage variations induced by Si$_{1-x}$Ge$_x$ and Si$_{1-x}$C$_x$ of sub 5-nm node silicon nanosheet field-effect transistors. Journal of Nanoscience and Nanotechnology. 2020;20:4684-4689. DOI: 10.1166/jnn.2020.17799.

[34] Yoon J.-S, Lee S, Lee J, Jeong J, Yun H, Baek R.-H. Reduction of process variations for sub-5-nm node fin and nanosheet FETs using novel process scheme. IEEE Transactions on Electron Devices. 2020;67:2732-2737. DOI: 10.1109/TED.2020.2995340.

[35] Oh Y.-S, Ward D. E. A calibrated model for trapping of implanted dopants at material interface during thermal annealing. In: Proceedings of International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217), San Francisco, CA, USA, 1998, pp. 509-512. DOI: 10.1109/IEDM.1998.746409.