Highly Reliable Contacts to Silicon Enabled by Low Temperature Sputtered Graphenic Carbon

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ABSTRACT
Titanium silicide (TiSi) contacts are frequently used metal-silicon contacts but are known to diffuse into the active region under high current density stress pulses. Recently, we demonstrated that graphenic carbon (GC) deposited by CVD at 1000 °C on silicon has the same low Schottky barrier as TiSi, but a much improved reliability against high current density stress pulses. In this paper, we demonstrate now that the deposition of GC is possible at 100 °C – 400 °C by a sputter process. We show that the sputtered carbon-silicon contact is over 1 billion times more stable against high current density pulses than the conventionally used TiSi–Si junction, while it has the same or even a lower Schottky barrier. SC can be doped by nitrogen (CN) and this results in an even lower resistivity and improved stability. Scalability of the CN thickness down to 5 nm is demonstrated. The finding that there is a low temperature approach for using the excellent carbon properties has important consequences for the reliability of contacts to silicon and opens up the use of GC in a vast number of other applications.

INDEX TERMS Carbon, contact resistance, ESD, graphene, metal-semiconductor, reliability, PVD, Schottky barrier, Schottky diode, silicide, sputtering, TiSi.

I. INTRODUCTION
Metal to semiconductor contacts are essential elements in integrated and discrete electronic devices. Common source and drain contacts in state-of-the-art FinFETs rely on the formation of titanium silicide (TiSi) [1]–[3]. TiSi provides a very low Schottky barrier height (SBH) to silicon, that’s why it is also highly appropriate for Schottky diodes in zero bias detector and mixer applications up to THz frequencies [4], [5]. The low barrier height makes TiSi very promising for further contact resistance reductions to NMOS and PMOS devices [6], [7]. However, titanium-based contacts exhibit a low thermal stability [8], [9], which is not suitable for increased Joule heating by large current densities in downscaled devices.

The high current density \( j \) during an electrostatic discharge (ESD) event can induce high temperatures in the device as the power \( P \) per volume \( V \) (power density) in a conductor during an ESD event is given by

\[
\frac{P}{V} = j \cdot E = j^2 \cdot \rho.
\]

Here, \( E \) is the local electric field and \( \rho \) is the electrical resistivity of the conductor. The damage to the device and consequently the reliability is mainly influenced by the magnitude of the applied current density, which is why we only consider current pulses in the following. A pulse can hence force a diffusion and migration of the interface material or the top metallization into silicon, which degrades the inherent electrical properties of the interface contact or even cause a complete failure of the device due to a junction burnout [10]–[17].

Graphene [18] still lacks being used in semiconductor devices but is heavily investigated for next generation interconnects. It was demonstrated that copper (Cu) wires encapsulated by graphene [19] and doped individual
multilayer graphene-nanoribbon [20] are very promising in their electrical and reliability properties to improve or replace the predominantly used Cu interconnects. Graphitic carbon (GC) materials [21]–[23] gained already some attraction for their adoption in semiconductor products. Previously, it was utilized as electrodes in DRAM capacitors [24], as switching material for non-volatile memories [25] and as highly stable membranes [26].

We reported earlier [10], [11] that a CVD-deposited GC contact to silicon (CVD-C-Si) has similar electrical properties as TiSi-Si but a much higher temperature stability and a more than 100 million times improved stability against ESD current pulses. Unfortunately, the deposition temperatures of 850°C – 1000°C are not compatible with many applications where temperature budget restrictions of about 400°C for middle and back end of line (MOL/BEOL) of advanced nodes are in place. More recently, we demonstrated that a low temperature sputtered graphenic carbon (SC) is possible and the SC could be doped with nitrogen (CN), which lowers the resistivity. SC and CN showed an enhanced reliability compared to CVD-C-Si and TiSi-Si [27]. In this extended paper, we will discuss these results more thoroughly as we review the carbon deposition process and related electrical properties in much more detail.

II. SPUTTERED CARBON – PROCESS AND PROPERTIES

Sputtered carbon can form a large variety of allotropes, ranging from graphitic/graphenic to diamond-like formations. It heavily depends on the sputtering method and deposition parameters [28]. Our focus is more on the electrical properties of the film where the electrical resistivity \( \rho \) was reported to range from \( 10^{-2} \Omega \text{cm} \) to \( 10^{10} \Omega \text{cm} \) [28]–[34].

We sputtered carbon in a physical vapor deposition (PVD) process from a 4” graphite target (purity 99.999 %) with an RF magnetron plasma source on a non-biased but heated substrate, which was 70 mm away from the carbon target. The base pressure in the sputter chamber, which is equipped with a liquid nitrogen cold trap, was \( < 2 \times 10^{-7} \text{mbar} \). The plasma was operated at very low argon (Ar) pressure \( p \) (2 \( \mu \text{bar} \) to 16 \( \mu \text{bar} \)) as such a range is necessary to achieve a very low resistivity [29].

Furthermore, we investigated the nitrogen-doped carbon films, as nitrogen (N) can reduce the resistivity of the carbon film and values \( < 10^{-2} \Omega \text{cm} \) are reported [35]. The N-doping leads to a shift of the Fermi level towards the conduction band, that’s why nitrogen acts as electron donor and is considered as n-type doping [36], [37]. We prepared the CN films with the same process setup as for SC, only the nitrogen gas (\( \text{N}_2 \)) was added to the argon gas (Ar). The maximum available gas flow ratio in our setup, restricted by the mass flow controllers, was Ar/\( \text{N}_2 \) = 56. This leads to a concentration of 3.5 at. % N in the plasma. The incorporated content of N in the CN films was measured by XPS to be in the order of 11 at. %. This is different to [38] and [39] as they measured, it stays below 5 at. % at this nitrogen/argon ratio – at least for the unbalanced magnetrons that they were using. All the sputtered films showed very good adhesion to Si, SiO\(_2\) and SiN, as if covalent bonds are formed. The adhesion to the metal parts in the PVD chamber is generally not very strong. A good adhesion is only achievable if the parts are bead blasted or well precoated with titanium.

The deposition of SC and CN was performed on a heatable substrate holder at temperatures \( T \) ranging from 20°C to 400°C directly on polished silicon with thermal silicon oxide (SiO\(_2\)) on top. An additional heating of the sample due to the plasma irradiation was not taken into account. The temperature and pressure are key parameters for the crystallinity of the film [40].

The Raman spectra in Fig. 1(a) highlight that SC sputtered on a substrate with a temperature of 20°C has no clearly distinguishable D- and G-peak, which is generally observed for amorphous structures [41]. In contrast, a film deposited at 400°C clearly shows the D- and a dominating G-peak, which indicates that graphenic sp\(^2\)-bonds are present. An annealing of a SC film deposited at 20°C at 550°C in hydrogen (H\(_2\)) for 1 h is necessary to get a Raman spectrum, which shows similar graphenic features. The CN films clearly display a D- and a dominating G-peak at all temperatures showing a higher content of sp\(^2\)-bonds [42]. The C≡N peak in the Raman spectrum indicates that sp\(^3\)-bonded N is incorporated into the film, but also sp\(^2\)- and sp\(^3\)-bonds between C and N are formed during the sputter process.

A surface analysis with an atomic force microscope (AFM), like shown in Fig. 1(b)-(g), underlines that the SC sputtered at 20°C has a very low surface roughness and no grain boundaries are recognizable as it is more amorphous. At 400°C substrate temperature, the surface is rougher and polycrystalline graphitic clustering occurs. The CN film features a much smaller grain size at 400°C associated with a smoother surface. The CN films sputtered at 20°C exhibit a very similar surface as the film deposited at higher temperature.

III. SCHOTTKY DIODE TEST VEHICLE

The reliability of a metal-semiconductor interface is frequently evaluated with Schottky diodes for high frequency applications. These devices are very prone to any changes at the junction region, which can be enforced by an electrical stress or just by high temperatures [43]–[46]. A damaged or deteriorated diode can be identified by monitoring the characteristics of the Schottky diode at a fixed reverse bias voltage. A degradation of the properties shows up as an increased reverse leakage current [11]. The reliability of the devices, and consequently of the metal-semiconductor interface, is often investigated with a high voltage or current pulse, like shown in Fig. 2(a). The pulses have commonly a width of 100ns [47] which is similar to the ANSI/ESDA/JEDEC JS-001-2012 Human Body Model [48] and the IEC61000-4-2 test standard [49].

In our experiments we used a vertical Schottky diode structure with an active area of 45.36 \( \mu \text{m}^2 \) to evaluate the impact...
FIGURE 1. (a) Raman spectra (offset for clarity) of SC and CN films sputtered at a substrate temperature of 20 °C and 400 °C, respectively. The used excitation wavelength is 532 nm. The spectrum of the SC film established at 20 °C is more of amorphous structure as indicated by the higher and wider D-peak than the G-peak of the Gaussian deconvolution of the spectrum. A ratio of \( \sim 1 \) of the fitted D- and G-peak (not shown) was found for CN at 20 °C. The pronounced G-peak is always higher than the D-peak for the films deposited at 400 °C, which indicates the prevalence of graphenic \( \text{sp}^2 \)-bonds. (b)-(g) Comparison of the surface roughness and the corresponding height profile along the dashed line of SC and CN films measured with an AFM. (b) and (e) show the surface and profile of a SC film sputtered at 20 °C. The root-mean-square surface roughness (\( R_{\text{RMS}} \)) is only 0.35 nm. The profiles of a SC film sputtered at 400 °C in (c) and (f) show a rougher surface and the surface nucleation of carbon leads to a polycrystalline texture. (d) and (g) illustrate the surface and height profile of a CN film deposited at 400 °C. It is smoother than the SC sample deposited at 400 °C as CN seems to have a higher nucleation density and grows more in a nanocrystalline fashion.

FIGURE 2. (a) A measured waveform of a 100 ns current pulse with a rise/fall time of \( < 15 \) ns and an average current density \( j = 3.5 \text{MA/cm}^2 \), which was measured with a Tektronix CT-1 current sensor. (b) Schematic cross-section of a TiSi-Si Schottky diode where Ti or TiSi diffuses into the \( n^- \)-Si epitaxial layer and could even reach the highly doped substrate by the application of high current pulses. Adapted from [11].

of a high current pulse on the reliability of the metal-silicon interface. The used test vehicle is a BAT15 Schottky diode from Infineon [50], a low SBH diode for mixer and detector applications. In its commercial available version it uses TiSi as the interface material to silicon (TiSi-Si) and consists of a thin \( n^- \)-epitaxial layer with a thickness of 150 nm. This thin layer is very susceptible to degradations in its electrical reverse bias characteristics when contaminations like metal ions enter this epitaxial region. Pulses with high power density can force the diffusion of Ti/TiSi into the epitaxial layer and could even reach the highly doped substrate by the application of high current pulses. Adapted from [11].

IV. ELECTRICAL CHARACTERIZATION
In Fig. 3(a)-(c), we evaluated the electrical film resistivity \( \rho \) by a four probe measurement as a function of the used RF power \( P \), working pressure \( p \) and substrate temperature \( T \) on silicon substrates with 300 nm of SiO\(_2\) on top. The sputtered films had a thicknesses of 35 nm. From Fig. 3(a), one can conclude that a further increase of power could lead to an even lower resistivity as the slope is quite linear and doesn’t converge to a minimum value within the displayed range. The CN film exhibits a 2-times lower resistivity at the same sputter conditions as nitrogen acts as an electron-donor and therefore approaches the value of CVD-C (\( \sim 1 \text{m\Omega/cm} \)), which was deposited at 1000 °C. A further increase in the power could lead the way to an improved carbon film but we were cautious not to overheat the target.

The sputtered film resistivity is quite sensitive to the pressure and increases for \( > 8 \mu\text{bar} \) very rapidly and the minimum \( \rho \) might not be located much below 2 \( \mu\text{bar} \), like illustrated in Fig. 3(b). For our electrical evaluations, we used 4 \( \mu\text{bar} \) instead of 2 \( \mu\text{bar} \) or lower, even if it would lead to a lower \( \rho \), as the surface analysis showed a higher surface roughness at lower pressure.

An increase in the substrate temperature leads to a strong decrease in the resistivity as a graphitization seems to occur at increased temperatures (Fig. 3(c)).

Furthermore, the sputtered carbon films show a negative temperature coefficient (NTC) like the CVD-C, as displayed in Fig. 3(d). At an increased temperature more electrons are populating the conduction band, which is more pronounced in high resistivity samples. The carbon film deposited at 20 °C shows at 200 °C an \( \sim 65 \% \) higher conductivity. In contrast, the CVD-C is at room temperature already a good conductor with already more free electrons available and this results in a \( \sim 15 \% \) conductivity increase at 200 °C.

When exposed to atmosphere, the resistivity of SC continuously drifts to higher values. The relative drift, which saturates after a few days at about 50 \% to 100 \% above the as-fabricated value, depends on the sputter process.
A BAT15 silicon test vehicle with all the same dimensions, dopants and guard ring structure as the commercial available device was used to sputter carbon or nitrogen-doped carbon as “metallic contact” onto silicon, like shown in Fig. 4(a). This enables a direct comparison of SC-Si and CN-Si to TiSi-Si and CVD-C-Si [11]. The substrates were prepared by ultrasonic cleaning in acetone and isopropyl alcohol before a full RCA clean. It is very crucial to have a contamination-free silicon substrate for the reliability tests as every ion or impurity could contribute to a possible degradation of the device. The native oxide on the devices was immediately removed before the sputter deposition by a dip in a 5% solution of hydrofluoric acid (HF) to get a pure hydrogen-terminated silicon surface on the BAT15 structure and a well defined carbon-Si interface. The time delay between HF-dip and insertion to the sputter chamber was below 3 min. The delay between insertion and deposition was 20 min due to the heating of the substrate to 400 \(^\circ\)C before the deposition was started.

The top metallization of the diodes consists of a stack of 50 nm of Ti, 1.2 \(\mu\)m of Cu and 40 nm of Au, which was deposited by electron-beam evaporation through a shadow mask onto SC or CN. No additional annealing of the metal stack was performed after the deposition. The thick Cu acts as additional heat sink and prevents current crowding during the device operation. Finally, the carbon was structured in a \(\text{H}_2\) plasma with the top metallization acting as a hard mask so that the carbon is fully removed at the non-covered regions.

The dc characteristics in Fig. 4(b) illustrate that the SC-Si diode is even close to the electrical characteristics of a TiSi-Si and a CVD-C-Si diode as it also shows a low Schottky barrier height (SBH) of 0.48 eV (Fig. 5(a)). The CN-Si deposited at a 400 \(^\circ\)C substrate temperature exhibits a much lower SBH (0.42 eV), which is beneficial for the creation of low ohmic contacts but the characteristic in forward direction is not as ideal as the TiSi-Si diode. The breakdown voltage and the reverse leakage depend on the SBH of the contact and the used temperature budget, which can induce a diffusion of the dopants (Fig. 5(b)). The CN-Si diode even performs better than a CVD-C-Si diode as it has a lower SBH but the breakdown voltage is the same. It has lower leakage current at \(V_T > 1\) V because the CN was deposited only at 400 \(^\circ\)C in contrast to the 1000 \(^\circ\)C used in the CVD process. No dopant diffusion occurs at low deposition temperatures, which would otherwise change the reverse breakdown voltage.
A dc voltage stress with high forward $V_f$ and reverse bias $V_r$ leads to a change in the interface properties of SC-Si and CN-Si, especially in a change of the SBH. The normal or safe operation was defined in $V_f < 4 \text{ V}$ and $V_r < 1 \text{ V}$ were almost no changes in the pristine device properties are detectable. As illustrated in Fig. 6, dc sweeps to $V_f = 7.5 \text{ V}$ or $V_r = 7.3 \text{ V}$, a voltage level which is at least 0.5 V below the breakdown, leads to a decrease in the barrier height. The CN-Si contact is even decreased to 0.39 V, which paves the way for a “zero-barrier height” as it is about 13% lower than the TiSi-Si contact. An device operation at higher forward bias $V_f > 1 \text{ V}$ shows the opposite behavior as the SBH increases. After a dc sweep to 2.1 V an about 10% lower SBH is obtained. Applying a constant high forward or reverse voltage for a much longer duration leads to even higher or lower SBH, respectively. The process hereby is fully reversible as a high SBH can be made smaller and vice versa. A higher SBH is easier to reach as the necessary voltage to force a change is lower. Also repeated dc cycles or constant reverse bias are needed to retrieve the lower SBH. Without an applied bias the SBH is stable over time and doesn’t recover back to the start value. The diode behaves as if an interface dipole is present, which is a well-known phenomena in carbon-silicon carbide contacts [52], [53].

V. TISI-SI INTERFACE RELIABILITY

The commercially available TISI-Si-BAT15 Schottky diode was pulsed at room temperature with a current density $j$ of $3.5 \text{ MA/cm}^2$ and a degradation can be detected as an increased leakage current at a reverse voltage $V_r = 1 \text{ V}$, as indicated in Fig. 7. The diode characteristics starts to degrade from the original behavior, as indicated by the over 100x increase of the reverse current (Fig. 7(a)). This signals the inter-diffusion of Ti/TiSi within the epitaxial layer. Furthermore, the device is short-circuited after 3 pulses as a metal or silicide filament might be created, as schematically depicted in Fig. 2. Fig. 7(b) clearly highlights that 2-4 pulses are sufficient to destroy the TiSi-Si junction at 3.5 $\text{MA/cm}^2$. The current pulse used has a duty cycle $< 0.0001$ and a waveform as shown in Fig. 2(a). This low duty cycle allows the diode to cool down to room temperature after each current pulse. The condition of the diode was monitored at a reverse voltage of $V_r = 1 \text{ V}$ and the diode is declared as failed if the reverse current reaches a value of $100 \mu\text{A} (220 \text{ A/cm}^2)$ as the on/off ratio of the diode is then deteriorated by a factor of more than 500. In addition, Fig. 7(b) illustrates that the maximum number of transient stress pulses depends on the current density level used. The probability of a possible damage to the diode is reduced when the pulses have a lower current density as the power density is proportional to $j^2$ (see in (1)). For $1.35 \text{ MA/cm}^2$, which is slightly above the permissible pulse load of $1.21 \text{ MA/cm}^2$ specified by the manufacturer, the diode is able to withstand up to one million events, but the failure probability is spread over a wide range [10], [11].
Failure but due to the excessive testing time. The duty cycle was pulsing of the CN-Si contact (non-filled stars) has been aborted not due to more than the CVD-C-Si. The CN-Si values are only lower bounds as the devices did not fail, but of the TiSi-Si contact by more than a factor of one billion, as illustrated in Fig. 8(a). All the shown values of the CN-Si contacts are lower bounds as the devices did not fail, but after several million of pulses, as the ions might react with the silicon and become inactive or they are diffused into the thin epilayer. The change in the SBH might be similar to the results discussed in Fig. 6, as a thermally driven recrystallization or rehybridization at the CN-Si interface, due to the high power density of the pulse, might take place [52], [53]. A reverse voltage of 7.5 V for about 1 min is sufficient to change the SBH to the as fabricated or an even lower value. This indicates that the temperatures close to the melting point of silicon during billions of such ESD events [11] do not lead to a permanent change of the carbon-silicon interface.

In order to achieve the excellent reliability results, it is very important that all parts near the sputtering source and especially the sample holder and shutter are well coated with carbon. In the first test, the shutter was not well coated with carbon as the films adhered very poorly on the polished metal surface and a resputtering of the shutter material in this low pressure range is possible. In addition, a few milliseconds long exposure of a badly coated shutter to the plasma during the shutter operation from closed to opened position or if the shutter is left too close to the plasma source when opened could be enough to deposit contaminants on the silicon active region or in the carbon film. These trace amounts of metal can easily diffuse into the epilayer after a few 100 pulses and act as unwanted recombination centers leading to a deteriorated diode behavior, as shown in Fig. 9(a). After a continued application of pulses to the device two different scenarios are possible. At first, they can induce early failures during the reliability test as they create a local short-circuit. Second, the recombination centers almost disappeared again after several million of pulses, as the ions might react with the silicon and become inactive or they are diffused into the highly doped substrate before a more severe failure occurred.

The reliability results of the tested samples produced in a not well precoated equipment is distributed over a wide range, as highlighted in Fig. 9(c). A contamination-free carbon deposition can only be achieved after a precoating of the whole sputter equipment. Especially the magnetron shutter needs to be coated on all sides. The recombination current free J-V characteristics, shown in Fig. 9(b), can only be obtained after thorough precoating of all components. No recombination currents are observed then and only then we get excellent reliability of the CN-Si contact of several billion pulses without deterioration.

For longer pulse duration and the same current density of 3.5 MA/cm², CN-Si is not as reliable as CVD-C-Si (Fig. 10(a)). For a width of 300 ns the applied energy is...
Three times higher than in the previous test, but the reliability is still much higher than the TiSi-Si diodes at 100 ns. The device still endures here over 100 thousand pulses. The deviation to CVD-C-Si contact becomes larger for longer pulses (500 ns) but it withstands at least 250 events. Also a much lower duty cycle in the range of $10^{-6}$ did not lead to change in the pulse endurance. The reason for the reduced reliability might be the higher electrical resistance of the CN film. As the current through the diode is kept constant, more resistance leads to more dissipated power, which could enforce an earlier destruction. Fig. 10(b) illustrates, that a degradation doesn’t occur gradually in a continuous fashion. The diode is fully functional after 450 pulses and is also very stable in its dc characteristics. It simply has a slightly higher SBH leading to a lower reverse current. After some more pulses are applied, a degradation of the device takes place as evidenced in the higher leakage current. Finally, the diode failed completely after 550 pulses.

In contrast, a 300 ns long pulse rises the temperature of the metallization to a point where it even can start to melt and it is already cracked and heavily piled up after 285 thousand pulses. As the temperature at the interface must be much higher than at the surface [11], the carbon-Si demonstrates outstanding temperature stability. The 500 ns pulses cause less visible damage to the metal surface, which might be due to the lower number (1550) of stress pulses.

**VII. SCALABILITY**

In the previous sections we have studied the behavior of carbon layers with a thickness of about 30 nm. However, the interesting question, how thin the carbon layer can be made while maintaining the superb diffusion barrier property has not yet been investigated. A first outlook on the scalability of...
withstand up to 1.28 billion pulses before the diodes fail. Superior to TiSi by a factor of over 100 million and can in Fig. 12(c). It shows that even the 5 nm CN contact is and less by the thickness of the CN. The series resistance is mainly determined by the contacts and less by the thickness of the CN.

The reliability behavior of the thin CN contact is plotted in Fig. 12(c). It shows that even the 5 nm CN contact is superior to TiSi by a factor of over 100 million and can withstand up to 1.28 billion pulses before the diodes fail.

VIII. SUMMARY
We have demonstrated that it is possible to deposition graphenic carbon at temperatures below 400 °C by a sputter process. The carbon-silicon contact can compete in its electrical characteristics with the conventionally used TiSi-Si contact. In contrast to TiSi, it significantly improves the reliability against high current density stress pulses and even outclasses the high temperature-deposited CVD-C-Si contact. A doping with nitrogen improves the resistivity and stability but the optimum ratio of Ar/N₂ needs to be studied in more detail. An further improvement of the electrical properties of SC and CN can be expected by fine-tuning of the sputter conditions supported by proper equipment.

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