Effect of post-deposition treatment on electrical properties of solution-processed a-IGZO Schottky diodes

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ABSTRACT
The fabrication of solution-processed electronic devices based on amorphous In–Ga–Zn–O (a-IGZO) requires high-temperature post-deposition annealing to activate IGZO layers and minimize impurities. Deep-ultraviolet (DUV) treatment can reduce the post-deposition annealing temperature when manufacturing a-IGZO thin-film transistors. Here, we investigate the effect of thermal annealing and DUV treatment in a nitrogen and ozone atmosphere on the properties of vertical thin-film Pt–IGZO–Cu Schottky diodes based on spin-coated a-IGZO. The DUV treatment in nitrogen allowed reducing the process temperature to 200 °C. A defect-induced hysteresis was observed on the current–voltage characteristics of as-fabricated Schottky diodes. The values of rectification ratio and barrier height were higher and the values of ideality factor were lower upon the backward bias sweep. It is assumed that the hysteresis behavior is caused by the presence of trap states in the semiconductor layer or at the Schottky interface. A trap density of 10^8 cm^{-2} to 10^{11} cm^{-2} was deduced from the current–voltage characteristics. The defect-induced hysteresis effect could be suppressed by depositing an Al_2O_3 layer and applying an additional thermal treatment of the whole diode structure.

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I. INTRODUCTION
Amorphous indium gallium zinc oxide (a-IGZO) is widely used as an active layer in integrated semiconductor devices (transistors, diodes, etc.) due to high carrier mobility, high transparency in the visible range of the light spectrum, and simplicity of patterning. Nowadays, a-IGZO thin-film transistors (TFTs) are utilized in flat panel displays in smartphones and tablet computers. High performance Schottky diodes based on sputtered a-IGZO have been demonstrated for ultra-high frequency energy harvesters and sensor applications. Development of printing technologies is of high interest due to the applicability for large-area processing, applicability for lightweight, foldable, and wearable devices, and relative simplicity of the processes. Since the inkjet printing of a-IGZO was demonstrated, most of the studies have focused on the optimization of the process and electrical properties of the transistors. Fabrication of printed semiconductor devices such as transistors, memristors, and rectifiers based on a-IGZO requires high-temperature post-deposition annealing at 450 °C–700 °C to remove organic ligand groups or polymer binders and minimize impurities and unnecessary carbon groups, which adversely affect device performance.
Post-deposition annealing temperature can be reduced by modifying the precursor chemistry\(^\text{16}\) and introducing combustion processing\(^\text{17}\) or light-assisted annealing such as deep-ultraviolet (DUV) treatment,\(^\text{18}\) ultraviolet (UV) flash annealing,\(^\text{19}\) pulsed white light sintering,\(^\text{20,21}\) or UV-ozone irradiation treatment.\(^\text{22}\)

In this study, we investigate the effect of thermal annealing (TA) and DUV treatment on the properties of Pt–IGZO Schottky contacts based on the solution-processed a-IGZO thin film. The DUV-assisted approach enables lowering the process temperature of Schottky diodes fabrication to 200 °C. We observed a hysteresis effect in the current–voltage characteristics of as-fabricated Schottky diodes and attempted to explain this effect based on the previously reported concept of interface trap states.\(^\text{23}\) An additional low-temperature annealing treatment of the fabricated structures was found to suppress the hysteresis effect in current–voltage characteristics.

II. EXPERIMENTAL

Vertical IGZO Schottky diodes (Fig. 1) were fabricated on alkali-free borosilicate glass (Corning 7059). First, the substrate was cleaned in a diluted acetic acid solution and then deionized water in an ultrasonic bath at 80 °C for 40 min. The Pt thin film was deposited by radio frequency (RF) sputtering on a Ti adhesive layer on the glass substrate at a pressure of 0.28 Pa and a power density of 2.96 W cm\(^{-2}\) to form the Schottky contact. The total thickness of the bottom electrode was about 150 nm. The IGZO thin film was formed by spin coating of ink with a precursor concentration of 0.128 M.\(^\text{18}\) IGZO ink was prepared by dissolving indium nitrate, gallium nitrate, and zinc acetate precursors from Sigma Aldrich in 2-methoxyethanol (In:Ga:Zn = 0.68:0.22:0.1). The ink was stirred at 70 °C for 1 h and then at room temperature for 24 h and filtered with 0.2 μm polytetrafluoroethylene filters prior to deposition. The UV-ozone-cleaning procedure for 5 min was applied on Pt thin films before IGZO deposition to achieve proper wettability and homogeneity. The IGZO spin-coated layer was dried at 150 °C for 5 min, and then UV-ozone-cleaning for 3 min was applied before the next spin coating of the IGZO ink to ensure uniformity of the layer [Fig. 1(c)]. After the deposition of the fifth layer, the resulting IGZO thin film was dried at 200 °C in air for 1 h. For the first group of samples, TA in air at 250 °C for 1 h was applied. For the second group of samples, DUV treatment was applied for 1 h in a constant N\(_2\) gas flow or in air by using a Filgen UV253HR ozone cleaner with a low-pressure mercury lamp with two main emission peaks at 184.9 nm and 253.4 nm and a power density of 28 mW/cm\(^2\). UV irradiation in the presence of ambient oxygen leads to significant ozone production; furthermore, the results for these samples were referred to “DUV treatment in O\(_3\).” Subsequent TA at 200 °C for 30 min was applied for removal of volatile compounds and densification of the semiconductor layers as it was proposed for UV-treated dielectrics.\(^\text{24,25}\)

**FIG. 1.** (a) Structure of the vertical Schottky diode based on printable IGZO, (b) SEM image of the fabricated Pt–IGZO structure after DUV treatment in N\(_2\) and deposition of Al\(_2\)O\(_3\), (c) photograph of the Ti–Pt/IGZO layers fabricated with ozone treatment after each IGZO spin coating, (d) O1s XPS peak deconvolution in depth of the IGZO layer after TA, and (e) O1s XPS peak deconvolution in depth of the IGZO layer after DUV treatment.
The thickness of the IGZO layer after annealing was 100 nm. As the final step, the ohmic Cu top contact was evaporated through a metal mask under high vacuum (≤ 10⁻⁷ Pa). The area of the contact was 200 × 200 μm², and the thickness of the Cu layer was about 70 nm.

One group of the samples fabricated with DUV in N₂ treatment was encapsulated with 20 nm Al₂O₃ by atomic layer deposition (ALD) at 150 °C. Another group of samples fabricated with DUV in N₂ treatment was thermally annealed at 125 °C for 30 min after the deposition of Cu electrodes.

The chemical composition and oxygen vacancy content of the IGZO films were measured by x-ray photoelectron spectroscopy (XPS) using a Quantum2000 photoelectron spectrometer from Physical Electronics with a monochromatic Al Kα source (1486.6 eV) operating at a base pressure below 10⁻⁷ Pa. Depth profiles were obtained with Ar⁺ sputtering at 2 keV for 30 s per step allowing to sputter through the thickness of IGZO layers. Figures 1(d) and 1(e) display the deconvolution of the O1s peak for samples after TA or DUV, respectively. The peak area of 530 eV was attributed to O1s and could be fitted by three Gaussian functions centered at 529.8 eV, 530.6 eV, and 531.6 eV. The low binding-energy component of O1s centered at 529.8 eV (M–O) was attributed to O⁻² ions surrounded by In, Ga, and Zn atoms in IGZO. The peak at 530.6 eV (O vac) was related to the oxygen vacancies. The peak at the high binding energy (531.6 eV, M–OH) was attributed to oxygen in a hydroxide environment. Regardless of the annealing treatment, both TA and DUV processed IGZO layers contain a significant amount of OH species and oxygen vacancies, and there is no a significant difference between the two annealing conditions.

Current–voltage and capacitance–voltage characteristics of the diodes were measured in air at room temperature in dark using a Keithley 4200 characterization system; electrodes were contacted using a probe station Karl Suss PM8.

III. CHARACTERIZATION AND SIMULATION

A. Electrical characteristics extraction

The current–voltage characteristics of the fabricated Schottky diodes were obtained by sweeping the bias from −1 V to +1 V (forward direction) and from +1 V to −1 V (backward direction). As-fabricated Pt–IGZO–Cu Schottky diodes exhibit a hysteresis effect in their J–V characteristics (Fig. 2), which could be attributed to the defects at the metal–semiconductor interface and/or in the semiconductor film, as will be described below.

The values of the series resistance Rₓ, saturation current Is, ideality factor n, Schottky barrier height Φb, and electron affinity of the IGZO χIGZO are obtained by fitting the linear part of measured I–V characteristics in forward and backward sweep directions based on the following equations:

\[ I = A A^* T^2 \exp(-qV/kT) \left[ \exp(q(V - IR_x)/nkT) - 1 \right], \]  

(1)

\[ \Phi_b = W_{Pt} - \chi_{IGZO}, \]  

(2)

where A is the area of the diode, A* is the effective Richardson constant, which for IGZO has a theoretical value of 41 A cm⁻² K⁻²,\( T \) is the absolute temperature, \( k \) is the Boltzmann constant, \( q \) is the elementary charge, and the work function for Pt Wₚt equals 5.4 eV.\( ^{30} \) The method of successive approximations with a maximum relative error of 5% was used. Five measured characteristics for each fabrication process were analyzed. Extracted electrical characteristics of the fabricated diodes are summarized in Table I.

Capacitance–voltage characteristics for the Pt–IGZO–Cu structures after TA and DUV treatment in N₂ are presented in Fig. 3. The measurement frequency was set to 100 kHz. The capacitance increased slowly with the decreasing reverse bias voltage, indicating that the width of the depletion region varied with the applied bias voltage. The area of the diodes limits the capacitance to the values of 52 pF and 60 pF at reverse bias for the samples after TA and DUV treatment in N₂, respectively. The values of the charge density in the depletion region \( N_{dpl} \), built-in potential \( V_{bs} \), and dielectric constant of the semiconductor \( \varepsilon_s \) were calculated using the following equation:

\[ \frac{A^2}{C^2} = \frac{2}{\varepsilon_s\varepsilon_0 N_{dpl}} \left( \frac{V_{bs} - kT}{q} - V \right), \]  

(3)

where \( \varepsilon_0 \) is the dielectric constant of vacuum.

B. Estimation of the interface trap density

Possible mechanisms of hysteresis behavior of TFTs based on IGZO are described in the literature as hole/electron trapping in the interface of the gate insulator, the creation of ionized oxygen vacancies (VO⁺ or VG⁺), and the donor-like defect creation in the IGZO channel.\( ^{11} \) Particularly, hysteresis in transfer characteristics of the IGZO TFT has been attributed to photo-generated ionized oxygen vacancies at the semiconductor/gate dielectric interface.\( ^{32} \) Different recovery behavior for photo-annealed [185 nm (90%) and 254 nm (10%) in N₂] and thermally annealed (350 °C for 1 h) IGZO TFTs after white light illumination was investigated.

In this study, we also observe the hysteresis effect of the J–V characteristics resulting in different values of the Schottky barrier height and ideality factors depending on the voltage bias sweep direction. This hysteresis effect could be caused by electron trapping in the layer because of the residual hydroxyl groups detected by XPS.
TABLE I. Extracted electrical characteristics of the as-fabricated Schottky diodes.

| TA in air | DUV in N₂ | DUV in O₃ |
|-----------|-----------|-----------|
|           | Forward   | Backward  | Forward   | Backward  | Forward   | Backward  |
| \(I_{on}/I_{off}\) (A) | \((5 ± 4) \times 10^3\) | \((3 ± 2) \times 10^5\) | \((5 ± 2) \times 10^3\) | \((2 ± 1) \times 10^5\) | \(45 ± 20\) | \(4 ± 5) \times 10^3\) |
| \(I_s\) (Ω) | \((5.1 ± 0.6) \times 10^{-6}\) | \((5.1 ± 0.2) \times 10^{-10}\) | \((5.8 ± 0.5) \times 10^{-7}\) | \((5.2 ± 0.1) \times 10^{-10}\) | \(8.57 ± 1.1) \times 10^{-6}\) | \((3.1 ± 0.1) \times 10^{-8}\) |
| \(\Phi_b\) (eV) | \(0.488 ± 0.001\) | \(0.72 ± 0.01\) | \(0.52 ± 0.02\) | \(0.73 ± 0.01\) | \(0.48 ± 0.002\) | \(0.62 ± 0.002\) |
| \(\chi_{IGZO}\) (eV) | \(4.81 ± 0.01\) | \(4.57 ± 0.01\) | \(4.9 ± 0.04\) | \(4.65 ± 0.01\) | \(4.92 ± 0.20\) | \(4.78 ± 0.16\) |
| \(\eta\) | \(2.65 ± 0.07\) | \(1.51 ± 0.02\) | \(2.81 ± 0.1\) | \(1.44 ± 0.02\) | \(2.67 ± 0.11\) | \(2.26 ± 0.04\) |
| \(R_t\) (Ω) | \(4.3 ± 0.2\) | \(3.7 ± 0.1\) | \(4.2 ± 0.2\) | \(6.8 ± 0.1\) | \(7.5 ± 0.3\) | \(3.5 ± 0.3\) |

[Fig. 1(d) and 1(e)] as well as by the charged defects at the Schottky interface. We attempt to estimate the density of the charge traps assuming the ionized oxygen vacancies at the IGZO/metal interface as proposed by Jo et al.\(^{12}\)

Under the thermal equilibrium situation, when the work function of the metal is higher than the work function of the semiconductor, electrons flow into the metal and free electron concentration in the semiconductor near the boundary decreases; it corresponds to the depletion region \(W_D\). The presence of donor-like surface trap states modifies the charge in the depletion region \(W_D\), and the barrier height \(\Phi_b\) decreases (Fig. 4). After applying the forward bias, the surface traps are partially neutralized; thus, the barrier is higher (Table I).

A range of values for the surface trap density can be estimated from the current–voltage hysteresis. To analyze the I–V hysteresis for the as-fabricated samples, we used the methodology proposed by Omar et al.\(^{23}\) to explain the interface trap induced non-ideality in the Ni/4H–SiC Schottky diode. The electric field in the space charge region with and without interface traps can be determined by solving Poisson’s equation,

\[
E(x) = -\frac{qN_{dpt}}{\varepsilon_s\varepsilon_0} (W_D - x), \quad E'(x) = -\frac{qN_{dpt}}{\varepsilon_s\varepsilon_0} (W_D' - x). \tag{4}
\]

At a metal–semiconductor interface \(x = 0\), \(E(0) = E_{max} = -\frac{qN_{dpt}}{\varepsilon_s\varepsilon_0} W_D\) and \(E'(0) = E'_{max} = -\frac{qN_{dpt}}{\varepsilon_s\varepsilon_0} W_D'\). Here, the space-charge region width in the presence and absence of traps is described as \(W_D = \sqrt{\frac{2\varepsilon_s}{qN_{dpt}}(V_b - V)}\) and \(W_D' = \sqrt{\frac{2\varepsilon_s}{qN_{dpt}}(V_b' - V)}\), respectively. The built-in potential \(V_{bi}\) for non-ideal diodes can be determined from the bias dependent barrier height as \(V_{bi} = \Phi_b(V) - \Phi_n\), where \(\Phi_b(V) = qV + \frac{m_1}{2} V^2\), \(\Phi_n\) is the zero-bias barrier height, and \(\Phi_n\) was calculated from the measured capacitance–voltage characteristics. Then, Eq. (1) can be rewritten in terms of \(qV\) as

\[
I = \frac{AA^*}{2}\exp(-qV/kT)[\exp(q(V - IR)nkT)]. \tag{5}
\]

The value of \(V_{bi}'\) corresponds to the trap-free barrier height and is equal to the flat band voltage \(V_{FB}\) which can be determined from the plot of a voltage across the space charge region \(U\) vs applied voltage \(V: U = V - IR\). The voltage across the space charge region increased linearly with the applied bias until the saturation at \(V_{FB}\). The estimated flat band voltage is 0.54 V and 0.72 V for 1–V measured in forward and in backward direction of bias sweep, respectively, for the samples after TA and 0.88 V and 0.8 V after DUV treatment in N₂.

The electric field in the space charge region \(E_{traps}\) that lowers the trap-free electric field is determined by the interfacial trap charge and can be approximated with a Dirac delta function as \(E_{traps} = -\frac{\rho_{traps}}{\varepsilon_s}\), where \(\rho_{traps}\) is the interface trap density. Thus, \(E_{max}' = E_{max} + E_{traps}\), and \(W_D' = W_D + \frac{N_{traps}}{\varepsilon_s}\).

FIG. 3. Capacitance–voltage characteristics of Pt–IGZO–Cu Schottky diodes.

FIG. 4. Schematic energy band diagram of the Pt–IGZO Schottky contact: \(W_D^{(a)}\), \(V_{bi}^{(b)}\), and \(\Phi_0^{(c)}\) correspond to trap-free characteristics and \(W_D\), \(V_{bi}\), and \(\Phi_0\) correspond to characteristics in the presence of traps.
The interface trap density for Pt–IGZO–Cu Schottky diodes after TA and DUV treatment in N₂ calculated as a function of the applied bias is shown in Fig. 5. The different behavior of the trap density is observed for as-fabricated structures after TA and DUV treatment in N₂. The trap density for the samples after TA constantly decreases for the bias sweep in the forward direction. The increase and subsequent saturation of the trap density at an applied voltage of 0.35 V are observed for the bias sweep in the backward direction for the samples after TA. The trap density for the samples after DUV treatment decreases for the bias sweep in the forward direction and increases for the bias sweep in the backward direction; moreover, the trap density for the backward sweep direction is lower. The effect of trap density lowering for DUV annealed samples can be explained by partial neutralization of surface traps by captured electrons during forward sweep measurements. The more facile neutralization of ionized oxygen vacancies by electron capture under positive gate potential is described in the literature for photo-annealed IGZO TFTs. On the other hand, the saturation and higher values of trap density for bias sweep in the backward direction could be attributed to the higher value of $V_{FB}$, which depends on both interface and space charge.

IV. CHARACTERIZATION AFTER ADDITIONAL LOW-TEMPERATURE ANNEALING

It has been shown that low-temperature annealing can reduce the trap density at the interface or in bulk in an a-IGZO TFT. Therefore, we studied the effect of additional annealing and deposition of an Al₂O₃ insulating layer on the performance of the a-IGZO Schottky diodes. After deposition of the Al₂O₃ thin layer by the ALD technique at 80 °C, the diodes fabricated with DUV treatment in N₂ exhibit lowering of the forward current and hysteresis in the current–voltage characteristics; the reverse current is not significantly changed (Fig. 6). Almost no hysteresis effect was observed for the samples after ALD Al₂O₃ thin layer formation at 150 °C. Similarly, no hysteresis was detected after an additional thermal treatment at 125 °C instead of Al₂O₃ deposition for the samples fabricated with DUV treatment in N₂. At the same time, electrical characteristics degrade in both cases (Table II), leading to ideality factors of 1.98 and 1.66 in forward and reverse sweeps, respectively, and a rectification ratio of $10^3$. The characteristics remained constant after two months of storage in air. The suppression of the hysteresis effect is caused by the removal of charge-trapping states in the devices, but it is not clear where these states are localized within the structure. Indeed, the additional TA treatment of the whole Pt/IGZO/Cu device was performed at a temperature of 125 °C, which should not affect the underlying IGZO/Pt interface that was annealed at a higher temperature of 250 °C. This indicates that the trap states could be localized closer to the IGZO/Cu interface. Furthermore, the lowering of the forward and reverse current for all the structures after the additional TA treatment at 80 °C–150 °C could be explained by the formation of an additional p–n junction between the a-IGZO and the Cu ohmic contact. It was reported earlier that the Cu ohmic contact can be used for sputtered a-IGZO Schottky diodes, but after a heat-assisted treatment, an interfacial CuOₓ...
layer can form at the CuO\textsubscript{x}-IGZO junction, thus lowering the currents.

V. CONCLUSIONS

It was demonstrated that post-deposition treatment in different atmospheres had a pronounced effect on the electrical properties of Pt–IGZO–Cu Schottky diodes based on solution-processed a-IGZO. The DUV treatment allowed lowering the process temperature to 200 \degree C as compared to the reference thermal annealing treatment at 250 \degree C. The DUV treatment in a nitrogen atmosphere led to improved electrical properties of Schottky diodes as compared to the reference thermal anneal treatment at 250 \degree C. The DUV treatment in a nitrogen atmosphere had a pronounced effect on the electrical properties of Schottky diodes after additional low-temperature annealing.

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DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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| DUV in N\textsubscript{2} and ALD Al\textsubscript{2}O\textsubscript{3} at 150 \degree C | DUV in N\textsubscript{2} and TA at 125 \degree C |
|---------------------------------------------|---------------------------------------------|
| $I_{\text{on}}/I_{\text{off}}$ | 5 × 10\textsuperscript{2} | 5 × 10\textsuperscript{2} | 10\textsuperscript{3} | 10\textsuperscript{3} |
| $I_{\text{f}}$ (A) | 1.11 × 10\textsuperscript{-8} | 1.2 × 10\textsuperscript{-8} | 1.08 × 10\textsuperscript{-8} | 1.62 × 10\textsuperscript{-9} |
| $\Phi_{\text{H}}$ (eV) | 0.64 ± 0.01 | 0.64 ± 0.01 | 0.65 ± 0.02 | 0.69 ± 0.02 |
| $\chi\text{IGZO}$ (eV) | 4.75 ± 0.08 | 4.75 ± 0.08 | 4.65 ± 0.09 | 4.61 ± 0.11 |
| $\pi$ | 2.87 ± 0.07 | 2.89 ± 0.07 | 1.98 ± 0.08 | 1.66 ± 0.09 |
| $R_{\text{f}}$ (k\Omega) | 5.3 ± 0.1 | 4.9 ± 0.1 | 2.1 ± 0.6 | 3.1 ± 0.5 |
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