Data acquisition and processing in the ATLAS tile calorimeter phase-II upgrade demonstrator

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Abstract. The LHC has planned a series of upgrades culminating in the High Luminosity LHC which will have an average luminosity 5-7 times larger than the nominal Run 2 value. The ATLAS Tile Calorimeter will undergo an upgrade to accommodate the HL-LHC parameters. The TileCal readout electronics will be redesigned, introducing a new readout strategy. A Demonstrator program has been developed to evaluate the new proposed readout architecture and prototypes of all the components. In the Demonstrator, the detector data received in the Tile PreProcessors (PPr) are stored in pipeline buffers and upon the reception of an external trigger signal the data events are processed, packed and readout in parallel through the legacy ROD system, the new Front-End Link eXchange system and an ethernet connection for monitoring purposes. This contribution describes in detail the data processing and the hardware, firmware and software components of the TileCal Demonstrator readout system.

1. Introduction

TileCal is the hadronic calorimeter of the ATLAS experiment at the LHC [1]. It is a sampling detector composed of iron/scintillating tiles with fibers, and readout by 9852 photomultipliers tubes (PMTs). In the present system, the PMT signals are digitized with a 40 MHz clock that is synchronous with the beam crossing. The digital samples are stored in pipeline memories during the Level 1 (L1) trigger latency (2.5 μs). Simultaneously, the PMT analog signals are grouped and transmitted to the Level 1 Calorimeter system. The data for events selected by the Level 1 trigger system are transmitted to the ReadOut Drivers (RODs) located in the back-end system at a maximum sustained rate of 100 kHz. The LHC has planned a series of upgrades culminating in the High Luminosity LHC (HL-LHC) which will increase of order five times the LHC nominal instantaneous luminosity [2]. TileCal will undergo an upgrade to accommodate the HL-LHC parameters [3]. The TileCal readout electronics will be redesigned, introducing a new readout strategy. The digitized data from every crossing will be readout by PreProcessors (PPr) that are located off-detector in the counting room, which in turn provide the data to the new trigger and DAQ systems. In addition, the ease of installation has been improved with the concept of four “Minidrawers” per module, and the number of connections and single-point failures in the power and data readout have been reduced. In order to evaluate the new proposed readout architecture and the first prototypes of the different components, TileCal has undertaken a series of tests with beam at the CERN accelerator facilities. Prototype detector modules (Demonstrators) have been constructed and exposed to different particle beams (electrons, muons and hadrons) and at different energies, to evaluate the performance of the detector with the new readout system. The data acquisition and processing software for the TileCal test beams have been
Figure 1. Picture of a TileCal Demonstrator minidrawer for the HL-LHC. It includes the mechanics (aluminium body, Delryn IF Plate (DIFP) and cooling pipes), 12 PMTs, HV Regulation Board, a Main Board, a Daughter Board and the Adder Base Board which is only needed for analog trigger in the Demonstrator.

developed to provide backward compatibility with the legacy system and at the same time to permit an evaluation of the new features.

2. TileCal Phase-II electronics upgrade
The TileCal detector is composed of four cylinders divided into 64 wedge modules each. The front-end electronics are installed in drawers at the edge of these modules. Each module contains up to 48 PMTs. The TileCal drawers for the HL-LHC will be divided into four identical and independent mini-drawers serving 12 PMTs each (Figure 1).

2.1. The front-end electronics and power supplies
In the new TileCal readout architecture proposed for the HL-LHC, the PMT signals are acquired and digitized for every bunch crossing (40 MHz) with the data transferred to the PPr modules located off-detector (Figure 2).
The TileCal R&D program includes three different options to acquire the Photomultipliers (PMT) signals:

- The 3in1 Front-End Board (FEB) option is based on discrete components and it is an improved evolution of the current front-end board [4]. The FEB includes a shaper, bi-gain clamping amplifiers and a slow integrator. The signals from 12 FEBs are collected in a Mainboard that includes 24 12-bit ADCs to digitize the high and low gain of each FEB and four control FPGAs. The data are then transferred to the common Daughterboard (DB).

- The QIE (Charge (Q) Integrator and Encoder) is a custom Applications Specific Integrated Circuit (ASIC) that uses 350 nm SiGe technology that includes a charge integrator and time-to-digital converter at 40 MHz [5]. The ASIC provides digital information so the corresponding Mainboard only provides basic functionality to collect and route the signals to the common Daughterboard.

- The FATALIC is an ASIC that uses IBM 130 nm technology to implement a low impedance current conveyor followed by a current integrator with three different gains [5]. The signals from the integrator are digitized at 40 MHz with 12-bit ADCs included into the ASIC. The digitized data are collected in a Mainboard that transfers the data to the common Daughterboard.

The DB is common in all three front-end option. It provides bidirectional communication with the back-end electronics through high speed optical links running at 9.6 Gbps [6]. It is responsible for collecting the FEB data and transmitting them to the PPr. It also receives and decodes configuration commands from the PPr and propagate them to the corresponding front-end element.

The Low Voltage Power Supplies (LVPS) are controlled through dedicated links from the back-end [7]. The regulation is implemented in a three stages architecture: bulk high voltage power supplies located off-detector provide 200 V to the finger LVPS (fLVPS) that reside at the edge of each detector module. Then, the fLVPS provide 10 V to the front-end electronics that include Point-Of-Load (POL) to obtain the voltages needed by each electronic component.

Two different options are being evaluated for the regulation of the High Voltage (HV) needed by the PMTs:

- The remote HV has the control and monitoring circuitry installed off-detector. This requires an individual high voltage cable from the counting room to each PMT. This architecture significantly reduces the radiation tolerance issues since the electronics are installed off-detector.

- The HV Opto solution has bulk high voltage power delivered to each front-end drawer and the control and monitoring is implemented in the on-detector electronics to serve the 48 PMTs. In this case the number of long high voltage cables is reduced significantly but the radiation tolerance issues are more stringent.

2.2. The back-end electronics

The key component of the back-end electronics is the Pre-Processors [8] which provide bi-directional communication with the front-end electronics for data readout, configuration and monitoring. The Pre-Processor module for the HL-LHC will be implemented in a full size ATCA blade format (Figure 3). The basic interfaces with the ATCA backplane and the power distribution will be located in a motherboard with up to four slots to host Compact Processing Modules (CPM). The CPMs will include high speed optical connections to communicate with the FE electronics, one FPGA and interconnections through the motherboard to communicate with the Trigger and DAQ interface (TDAQi) implemented as an ATCA Rear Transition Module (RTM). Each CPM will be able to process the data from 8 Minidrawers (2 TileCal modules),
thus 32 PPr systems are needed to read out the entire detector. The data received from the
detector will be processed in real-time and calibrated energy and time per cell for every bunch
crossing will be transferred to the trigger FPGA in the TDAQi. In parallel, the data will be
stored in pipeline memories in the CPM FPGAs. The data corresponding to the events selected
by the trigger (Level 0 or Level 1 depending on the final ATLAS trigger structure) will be
extracted from the pipelines and transmitted to the Front-End Link eXchange (FELIX) [9]
system through the TDAQi module. The ATCA backplane (Zone 1 and Zone 2 connectors) is
used for power distribution, control and board health management, remote FPGA programming,
system configuration and data monitoring.

In order to evaluate the new proposed readout architecture, a PPr Demonstrator module has
been designed in an Advance Mezzanine Card (AMC) format which can be operated in an ATCA
or standalone framework. It includes four high speed optical QSFP connectors, one Virtex 7
FPGA for data processing and communication with the front-end electronics, one Kintex 7
FPGA for trigger data pre-processing and Avago MiniPOD connectors to communicate with
the trigger system. The control, configuration and monitoring is done through the back AMC
connector which provides several high speed connections with the FPGAs which are also used
to communicate with the FELIX system.

3. The TileCal Phase-II Demonstrator and test-beam program

A hybrid "TileCal Demonstrator" prototype has been developed to evaluate and qualify the
new readout and trigger concepts into the full ATLAS operation and data taking. The hybrid
Demonstrator uses the 3in1 front-end option and is fully compatible with the current system
providing both the analog signals for the current Level-1 trigger and the fully digital information
for the Phase-II trigger Pre-Processor prototypes and can replace one of the drawers in the
current system. The plan is to install the TileCal Demonstrator in ATLAS during one of the
short end of year LHC shutdowns during Run 2 or eventually during the second long shutdown
scheduled for 2019.

In addition, minidrawer prototypes equipped with the 3 front-end and the 2 HV regulation
options were produced to evaluate and compare their operability and performance in standalone
test benches and were integrated with the other parts of the system during three test beam campaigns in 2015 and 2016.

3.1. TileCal testbeam setup
During 2015 and 2016, prototype TileCal modules were instrumented with legacy and Phase-II upgrade electronics and were exposed to different particle beams and at different energies to evaluate the performance of the detector and the new electronics. The modules were exposed to muons, positrons and hadrons at different energies. Beam instrumentation was installed to separate the different types of particles, to measure the beam position and to trigger the data readout and synchronize it with the beam (Figure 4). Two Cherenkov counters were used to separate protons, pions and electrons for energies below 50 GeV whereas a muon hodoscope located behind the modules was used to detect muons. Wire chambers provided the exact position of the beam with respect to the modules and coincidences in two scintillators were used to generate the trigger.

The modules were mounted on a remote mobile table allowing to point the beam to the different modules and cells and at various angles (Figure 5).

3.2. Data acquisition in the Tile Calorimeter test with beam setup
The prototype PPr was used in the test beam measurements. It can be operated in legacy or Phase-II mode. In legacy mode the PPr emulates the legacy front-end electronics. It receives the data samples at 40 MHz which are stored in pipeline memories and, upon the reception of a L1 acceptance signal, the samples corresponding to the selected event are packed using the legacy dataformat and transmitted through an optical link to a ROD [10](Figure 6). The ROD processes and transmits the data to the ReadOut System and finally to the Event Builder which saves the data on a local file together with the event trigger information.

The Demonstrator and legacy systems operated in parallel are synchronized using the clock and trigger information distributed from the legacy TTC modules through dedicated optical links. The PPr introduces trigger identification to the data packets which is used at ROD level to synchronize the two systems.

In addition, the PPr implements the Phase-II readout architecture which can be used in standalone mode or in parallel with the legacy system. The PPr operated within the legacy infrastructure transfers the triggered data through a high speed optical link to the FELIX system which saves the data on a local disk for offline reconstruction and analysis. The PPr
standalone software package, called *PPrInterface*, is used to make the system verification tests and data taking for calibrations.

### 3.3. Data processing and reconstruction

The ATLAS software framework (Athena) was used to reconstruct the raw data stored in the Event Builder [11] and FELIX to energy and time per cell. This operation was performed online during data-taking for part of the events and the result was presented in the Data Quality Monitoring (DQM) display for online data verification. The complete datasets were reconstructed offline to produce ntuples and the results were presented in the Demonstrator Data Interface (DDI) web application. Daily calibration runs were used to verify the correct behavior of the electronics and to provide calibration of the detector at the electromagnetic energy scale.

### 4. Conclusion

The LHC has planned a series of upgrades culminating in the High Luminosity LHC (HL-LHC) which will increase of order five times the LHC nominal instantaneous luminosity. TileCal will undergo an upgrade to accommodate the HL-LHC parameters including a new read-out architecture. TileCal Demonstrator modules have been equipped with the first prototypes of the upgraded components and they have been tested with beam at the CERN accelerator facilities during 2015 and 2016. Data for different types of particles hitting the TileCal modules at various angles were acquired. Preliminary results showed a high efficiency of the data acquisition system. The operation of the Demonstrator and analysis of the data has been used to gain experience and detect weak points in our system. The tests with beam will continue to qualify the final designs which will be followed by the production and installation of the new system during the LHC Long Shutdown scheduled for 2025-2026.
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