Ultra-Thin SiGe in the Source Modifies Performance of Thin-Film Tunneling FET

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Abstract

In this work, the source structure of an n-type thin-film tunneling FET is engineered to get better performance. An ultra-thin SiGe along with Si is used in the source of silicon-based TFET. Two structures are compared with conventional TFET, one, SiGe is located on the top of Si in the source and another one in reverse. Simulations approve these structures can reduce sub-threshold swing, OFF-current several times, and increase the ON-OFF ratio. Band diagram for conduction and valance bands are investigated and band to band tunneling (BTBT) generation rate is used to find better performance. We find current flows at Si in the source with the wider bandgap. Ge mole fraction of SiGe is varied and its effects on the performance of TFET are studied. The SiGe thickness for both structures is explored to obtain the best thickness for SiGe.

Keywords: Tunneling FET(TFET), band-to-band-tunneling (BTBT), Ge, SiGe, sub-threshold swing.

1. Introduction

In the past decades, conventional MOSFET has been scaled down to obtain low-power, high-speed operations, and compactness of electronics equipment. However, shrinkage of conventional MOSFET is limited by short channel effect, variation in silicon thickness, random dopant fluctuations, and high sub-threshold swing (SS) [1, 2, 3]. These issues cause to drain-induced barrier lowering, low ION/IOFF ratio, high power dissipation due to IOFF increasing and especially high subthreshold swing [4]. Sub-threshold swing is limited to 60mV/decade for conventional MOS transistors. The thermionic injection of electrons over the energy barrier which limits the transition slope from the OFF to the ON-state. To achieve a low OFF-state current with a low threshold voltage, the sub-threshold slope should be smaller than 60mV/decade. however, this is not possible with the MOSFET.

High sub-threshold swing is a major concern for MOSFET technology. To overcome this issue, various possible devices have been explored in which tunnel FETs (TFETs) have attracted huge attention [5]. TFETs are proposed for future generation low-power devices due to their low subthreshold swing (SS) and low OFF-current [6, 7]. TFET is suggested the best for low standby power family in the 2005 ITRS [8, 9].

TFET suffers from some challenges, including low ON current (ION) and high ambipolar conduction [10]. The low ION hinders application in high-speed and RF applications. The low ION value in Si-TFETs is owing to a weak BTBT rate due to a large and indirect bandgap, and high effective mass of the carriers [11]. The low ION issue has been settled by various strategies such as the use of lower band-gap materials [12], III-V TFETs with staggered/broken bandgaps [13, 14], high-mobility channel material in strained Ge [15], and source doping optimizations [16]. Several gate and dielectric engineering have also been proposed like dual-metal gate TFETs [17, 18], double-gate TFETs with a tri-material gate [11], gate-all-around triple-metal TFETs [19], hetero-gate dielectric TFETs [20], and dual-material gate hetero-dielectric TFETs.

With decreasing tunneling barrier to increasing the on-current, the smaller tunneling barrier also leads to higher OFF-current [21, 22]. Furthermore, IOFF, as well as SS, would be further degraded by the enhanced trap-assisted tunneling (TAT) owing to the large density of interface defects in HTFETs [23]. The consequent degradation of the OFF-current in heterojunction can also be alleviated by the double metal gate technique [16, 18].
Strained Si has been investigated to increase $I_{ON}$ \[24\] whereas this material is highly affected by the growth method. For enhancing the ON-current, recently indium arsenide (InAs) is proposed because of its low bandgap. However, it suffers from OFF-current \[25, 26\]. Ge in the source with a low bandgap is another choice to improve ON-current. Ge is one of the promising candidate materials due to the high hole and electron mobility and it also is compatible with Si technology \[27\]. An epitaxial Ge on a Si substrate as the channel for TFET can reduce SS and enhance its performance \[28\]. Patel, et al \[29\], proposed SiGe at the top of the source region can enhance the performance of TFET. They proposed the best thickness for SiGe is 40nm. Whereas, the thickness of the thin film transistor reaches to bellow this value. Chunlei Wu, et al \[30\] split drain to two regions, half Si and half Ge, whereas Ge region is located under the Si region far from the gate. They reduce the average sub-threshold swing with this hetero-structure TFET. All these works used Ge or SiGe in the source of n-type TFET to decline tunneling path in ON-state and increase ON-current. Here, we also use SiGe in the source of n-type thin film TFET and explore its effects on the performance.

In this work, three structures for n-type TFET with source material engineering are studied. The best structure with better performance is investigated. SiGe is used instead of Ge and the structures are investigated for different mole fraction. In the end, the best SiGe thickness is explored.

### 2. MODEL AND FORMALISM

The proposed structures are investigated using a device simulator as implanted in Atlas Silvaco \[31\]. In our simulation, non-local band-to-band tunneling (BTBT) model \[32, 33\], is used that calculates the BTBT rate at each point. However, SRH and Auger models are used in the simulation to account carrier recombination effects. Band gap narrowing (BGN) model is activated for consideration the effects of high doping concentration on the reduction of the band gap. Electric field dependent Lombardi (CVT) model is turned on to consider mobility reduction in a high electric field. The simulations use a very fine mesh across the tunneling region. The proposed devices are simulated with Silvaco and current is obtained for different states.

The electrical properties of Si$_{1-x}$Ge$_x$ vary with Ge mole fraction (x) and these properties should be inserted in the simulations. Their properties change from Si ($x = 0$) to Ge ($x = 1$). Here, the modeling of mobility ($\mu$) and saturation velocity ($v_{sat}$) for strained SiGe on

![Figure 1: Schematic of three studied structures.](image)

#### Table 1: SiGe parameters is modeled with equations using experimental reports. \[24, 25, 26, 30, 31\]

| Symbol | Equation |
|--------|----------|
| $\mu_n$ | $\mu_n(x) = \exp(7.37 - 10.90x + 11.51x^2)$ |
| $\mu_p$ | $\mu_p(x) = \exp(6.35 - 5.97x + 6.97x^2)$ |
| $v_{sat,n}$ | $v_{sat,n}(x) = 10^7/(0.98 + 2.93x - 2.39x^2)$ |
| $v_{sat,p}$ | $v_{sat,p}(x) = 10^7/(1.36 + 1.91x - 1.88x^2)$ |

Si is taken from Ref. \[40\]. Material parameters for SiGe are used from experimental results and the amount for $\mu$ and $v_{sat}$ are derived from a SiGe layer grown on a Si substrate. The mobility and velocity saturation equations as a function of Ge mole fraction (x) are listed in Table 1. The model for both electron and hole is included in the Table.

- **Band alignment** should be considered in heterostructure systems. Electron affinity (x) and bandgap ($E_g$) determines the energy of conduction and valence band. The location of bands in SiGe relative to Si controls band alignment and behavior of the heterostructure. The electron affinity and bandgap of Si$_{1-x}$Ge$_x$ for different x values are listed in Table 2. The parameters extracted from the experimental reported and inserted
in the simulation. Band gap varies from 1.1eV for x = 0 (Si) to 0.66eV for x = 1 (Ge) and electron affinity also changes from 4.05eV for Si to 3.95eV for Ge.

### 3. results and discussion

Material engineering at the source gives a chance to enhance the performance of a TFET. We compare three different structures for TFET, see Fig. [1] The first one is a common TFET that all source, channel, and drain are constructed with Silicon. The second structure, the source is split into two regions, up region close to top-gate is constructed from SiGe and underneath material from Si. The third structure is inverse of the second structure so that silicon is used on the top of SiGe in the source. Source, drain, and channel lengths are considered 5nm, 5nm, and 10nm, respectively. Gate oxide thickness is considered 1nm and the gate is considered poly-Si. Doping concentration for source, channel and drain regions are considered 2 × 10^{20}cm^{-3}, 10^{17}cm^{-3}, and 2 × 10^{19}cm^{-3}, respectively. Drain-source voltage is considered as V_{DS} = 0.1V. V_{GS} = −0.75V and V_{GS} = −3V are selected for OFF- and ON-state, respectively.

The drain current versus gate voltage for different structures is shown in Fig. [2] Three structures are compared with the main parameters- I_{ON}, I_{OFF}, ON-OFF ratio, and sub-threshold swing (SS). SS in the sub-threshold region can be defined as:

\[ SS = \frac{V_{GS,2} - V_{GS,1}}{\log(I_{DS,2}) - \log(I_{DS,1})} \]  

This parameter indicates the current slope when the transistor switches on. The sub-threshold swing, I_{ON}, I_{OFF}, and ON-OFF ratio for structures are reported in Table [3] ON-current for all structures is the same and close to each other. Structure II shows the lowest of I_{ON} and conventional TFET the highest. On the other hand, Structure II shows the lowest I_{OFF}, it is four times lower than conventional TFET. Structure III also displays a low OFF-current, two times lower than conventional TFET. Due to the lowest OFF-current in structure II, this structure shows the highest ON-OFF ratio. The

![Graph](image_url)

Figure 2: Drain current versus gate voltage for three structures. L_{S} = L_{D} = 5nm, L_{C} = 10nm.

| Structure | I_{ON}[A] | I_{OFF}[A] | I_{ON}/I_{OFF} | SS |
|-----------|-----------|------------|----------------|----|
| Struc. I  | 1.41e-6   | 9.05e-14   | 1.56e7         | 117|
| Struc. II | 1.33e-6   | 2.49e-14   | 5.33e7         | 71 |
| Struc. III| 1.36e-6   | 4.16e-14   | 3.27e7         | 105|

ON-OFF ratio for structure II is four times larger than two other structures.

The main concern for TFET is SS that small SS can decline voltage and power supply. Structure III reduces SS from 117mV/dec for conventional TFET to 105mV/dec that this reduction is not much. On the other hand, structure II decreases SS from 117mV/dec to 71mV/dec which means this structure can decline SS as 50%. Structure III behaves highly close to conventional TFET. These results approve the structure II can be selected for future TFET. A FET with this structure is simulated to compare with the proposed structures. I_{ON}, I_{OFF}, ON-OFF ratio and sub-threshold swing are obtained as 2.61mA, 0.127μA, 2.05×10^{6}, and 468mV/dec, respectively. With comparing with the proposed structures, ON-current is larger than the proposed structures, whereas, its OFF-current is approximately four times lower than the conventional TFET. This causes the ON-OFF ratio to rise more than three times. The sub-threshold swing declines from 117mV/dec in the conventional TFET to 71 in the proposed TFET. These results indicate the performance of planar FET will halt for short channel length where TFET (our proposed structures) can continue planar processes.

For clarifying the performance of the proposed structures, map current density distribution for all structures are plotted in Fig. [3] The OFF-state current for the
One can observe in structure II, both OFF- and ON-current in the source highly pass through Si with a wider bandgap and lower mobility. We need further investigation to gain a better understanding of this behavior. In structure III, a high part of OFF-current flows in the Si region near to gate and a small part in the Ge region. ON-current mainly passes through the Si region. One can understand by comparing two structures that $I_{\text{OFF}}$ highly likes to flow far from the gate and ON-current passes in the Si region. We expected that $I_{\text{ON}}$ passes through the Ge region with lower bandgap but here ON-current passes in the Si region with a wider bandgap. Although, Ge is close to the gate and has a lower bandgap, current highly flows in the Si region.

For understanding the behavior of OFF- and ON-current, energy band diagrams and BTBT generation rates ($\Gamma$) for structures II and III are plotted along the channel at OFF-state in Fig. 4. Two paths are considered along with the device, one starts from Si in the source that we call "Si-path" and another starts from Ge and we call this one "Ge-path", see Fig. 1. Electrons tunnel from source to channel at OFF-state. In structure II, the BTBT generation rate in the source for Ge-path is much lower than Si-path. The lower tunneling distance contributes to a higher tunneling rate. At structure III, both paths indicate the BTBT generation rate in the same range, however, the BTBT generation rate is larger for Si-path. Both regions contribute to OFF-current.

The energy band diagram and BTBT generation rate is plotted at ON-state for two structures (structure II and III) in Fig. 5. It is obvious for structure II that one can’t observe any BTBT in Ge-path. Therefore, the current totally passes through Si-path. The holes can not directly tunnel from source to channel due to long tun-
Figure 5: Energy band diagram and BTBT rate along the channel for ON-current. Figures are for structure II at the middle of (a) Ge and (b) Si regions in the source and for structure III at the middle of (c) Si and (d) Si.

Energetics distance. Hole sees a high potential barrier from source to channel in Ge-path. This high potential barrier vanishes current flow in the Ge region, however, there is no such a barrier in Si-path. Structure III shows a BTBT generation rate for Si-path but the BTBT generation rate in the source is larger for Ge-path. In this structure, the high potential barrier between the source and channel for Ge-path vanishes current density in the Ge region. Holes diffuse from Si at the source in the channel then tunnel from channel to source. It is obvious from the Si path in structure III that the BTBT generation rate is maximum in the channel.

Si$_{1-x}$Ge$_x$ gives better compatibility with Si and is used for channel material in nowadays transistor. Here, an epitaxial SiGe is considered in the source instead of the Ge region. Ge mole fraction ($x$) is changed from $x = 0$ (Si) to $x = 1$ (Ge) and the results are plotted in Fig. 6. ON-current reduces for both structures with increasing Ge mole fraction whereas, structure III shows more reduction. In total $I_{ON}$ declines a little respect to absolute current. We observed ON-current mainly flows through the Si region so that Ge mole fraction doesn’t affect ON-current. In the opposite, OFF-current decreases five times with increasing Ge mole fraction from $x = 0$ to $x = 1$. However, structure II shows a lower OFF-current. OFF-current for both structures is the same at $x$ lower than 0.4 and for structure II decreases for $x$ larger than 0.4. ON-OFF ratio increases due to the decrease of OFF-current. The ON-OFF ratio increases five and three times for structures II and III, respectively. $SS$ also decreases with increasing of Ge mole fraction. $SS$ decreases more for structure II than structure III. $SS$ is 120mV/dec at $x = 0$ (Si) whereas for $x = 1$ (Ge) decreases to 104 and 70mV/dec for structures II and III, respectively. One can observe Structure II shows a higher ON-OFF ratio and lower $SS$.

We observed the performance of TFET increases respect to Ge mole fraction so Ge in the source with the best performance is selected in the following. Structure II displays a better performance where the SiGe thickness is selected half of the source thickness. In the following, the effect of SiGe thickness on the performance of TFET is investigated and the results are plotted in Fig. 7. As one can observe, $I_{ON}$ decreases for increasing of Ge thickness. However, $I_{ON}$ remains constant for low Ge thickness and decreases for thick Ge. In structure II, $I_{ON}$ decreases for $t_{Ge}/t_{D}$ ($t_{Ge}$ is Ge thickness and $t_{D}$ is source thickness) larger than 0.5 whereas for structure III, $I_{ON}$ approximately remains constant up to 0.9 then suddenly decreases. As one can see from Fig. 8 $I_{ON}$ in structure III flow near to the gate, whereas, it passes near to substrate for structure II. When Ge thickness increase from 0 to 0.9 in structure III, $I_{ON}$ remains constant because ON-current highly flows at the top of the channel and increasing of SiGe at the bottom of the source has not any considerable effect on the ON-current. But increasing Ge from 0.9 to 1, material in...
the top of source changes, and \( I_{ON} \) suddenly decreases. In structure II, the situation is inverse. \( ON \)-current passes through Si-region and increasing Ge thickness decreases Si thickness and declines \( ON \)-current gradually. \( I_{OFF} \) first decreases with increasing Ge thickness then increases for high Ge thickness. Minimum \( I_{OFF} \) occurs at \( t_{Ge}/t_D = 0.6 \) and 0.8 for structure II and III, respectively. \( ON \)-OFF ratio is reported using \( I_{ON} \) and \( I_{OFF} \). Structure II shows a higher \( ON \)-OFF ratio due to lower \( OFF \)-current. \( ON \)-OFF ratio behaves in the reverse of \( I_{OFF} \), it increases for low Ge thickness and decreases for high Ge thickness. \( ON \)-OFF ratio in structure II at \( t_{Ge}/t_D = 0.7 \) is nine-time larger than conventional TFET and in structure III at \( t_{Ge}/t_D = 0.6 \) is three times larger.

Sub-threshold swing is investigated versus Ge thickness, see Fig 7(d). \( SS \) decreases for both structures with increasing of Ge thickness whereas \( SS \) for structure II increases for \( t_{Ge}/t_D \) larger than 0.8. On the other hand, structure II shows a lower \( SS \) for the whole range of Ge thickness. The minimum \( SS \) happens for structure II at \( t_{Ge}/t_D = 0.8 \) that reaches to 60mV/dec. This \( SS \) is obtained for the channel with \( L_{CH} = 10nm \), however, lower \( SS \) can be obtained for a longer channel. The best performance can be obtained for structure II where \( t_{Ge}/t_D \) is close to 0.7. In this range \( I_{OFF} \) and \( SS \) are the minimum, the \( ON \)-OFF ratio is the maximum. \( I_{ON} \) only is higher for structure III and is low in this range of Ge thickness.

4. Conclusion

The source material of TFET is engineered to enhance performance. Three structures are compared with each other. Structure II with a SiGe layer on the top of the Si region in the source gives the best performance. This structure can decrease \( OFF \)-current four times relative to conventional TFET and increases the \( ON \)-OFF ratio three times. This structure also decreases sub-threshold swing from 117 for conventional TFET to 71mV/dec. The results showed \( OFF \)-current passes through both SiGe and Si regions, whereas, \( ON \)-current passes through the Si region with a wider bandgap. The performance of TFET increases with increasing Ge mole fraction. In the end, the best thickness for SiGe is 0.7 and 0.6 of source thickness for structures II and III, respectively.

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