Gating of two-dimensional electron systems in InGaAs/InAlAs heterostructures: the role of the intrinsic InAlAs deep donor defects

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We present an analysis of gated InGaAs/InAlAs heterostructures, a device platform to realize spin-orbitronic functionalities in semiconductors. The phenomenological model deduced from our magnetotransport experiments allows us to correlate the gate response of the studied two-dimensional electron systems to heterostructure design parameters, in particular the indium concentration. We explain the occurrence of metastable electrostatic configurations showing reduced capacitive coupling and provide gate operation strategies to reach classical field effect control in such heterostructures. Our study highlights the role of the intrinsic InAlAs deep donor defects, as they govern the dynamics of the electrostatic response to gate voltage variations through charge trapping and unintentional tunneling.

I. INTRODUCTION

Quantum wells (QW) based on InAlAs potential barriers have developed into a diverse platform to leverage spin-orbit interaction for solid-state applications. These QW heterostructures allow an engineering and control of the Rashba-type spin-orbit interaction \[1\]–\[8\], opening perspectives \[9\] for the realization of all-electrical spin-transistors \[10\] or topological superconductivity including the observation of Majorana zero modes \[11\]–\[15\].

Gating of two-dimensional carrier systems represents a key functionality of these applications and has been frequently used in this context \[2\]–\[6\] \[16\]–\[22\]. Interestingly, reports on the microscopic mechanisms of the capacitive coupling between the gates and the two-dimensional systems are scarce, while at the same time similarly designed heterostructures seem to deliver diverse gate responses \[16\]–\[22\], posing the question of the origin of these discrepancies.

Here, we present an extensive experimental study of the gate response of top-gated two-dimensional electron systems (2DES) confined in InAlAs-embedded InGaAs QWs. From our experiments, we deduce a phenomenological microscopic model which allows to explain and predict the observed features of the gate response. In particular, we elucidate the occurrence of a limited voltage range allowing classical field effect control of the 2DES, while a broader range leads to metastable gate response, with limited to vanishing capacitive coupling of the gate to the 2DES. We also demonstrate gate operation strategies to bring an InAlAs-based heterostructure from a metastable situation into the classical field effect range.

Our model points out the crucial role of intrinsic InAlAs defect states for the electrostatics of gated heterostructures, hence highlighting their importance in the design process of InAlAs-containing devices for spin-orbitronic applications.

II. EXPERIMENTAL

Our samples were grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs (100) substrate. The layout of the heterostructures is sketched in Fig. 1(a). The oxide desorption was performed at 620°C, followed by 100 nm GaAs and an Al_{0.5}Ga_{0.5}As/GaAs ten period superlattice as lattice-matched smoothing layers. Due to the native lattice mismatch of 7.2% between GaAs and InAs, a In_{x}Al_{1-x}As step-graded buffer was grown at 335°C, where \( x = 0.1 \) to 0.87 (sample A) in 19 steps resp. to 0.82 (sample B) in 17 steps followed by a single step back to \( x = 0.81 \) (sample A) resp. \( x = 0.75 \) (sample B). Then, the active layers were grown at 440°C, comprising the In_{x}Ga_{1-x}As QW embedded in 120 nm In_{x}Al_{1-x}As below and 130 nm In_{x}Al_{1-x}As above. In order to prevent oxidation damage, the structure was completed with a 2 nm In_{x}Ga_{1-x}As barrier. The indium content in the active layers is constant at 81% for sample A and 75% for sample B.

The samples were processed with standard wet etching techniques in a clean room environment to define a Hall bar geometry with a width of 20 \( \mu m \). After etching, Ohmic contacts were realized by deposition of 260 nm AuGe (88%/12%) and 66 nm Ni, followed by forming gas assisted annealing. As a gate dielectric, we deposited 100 nm (sample A) resp. 50 nm (sample B) Al_{2}O_{3} via thermal atomic layer deposition at 300°C, followed by a 10/100 nm Ti/Au top gate (TG).

The measurements, unless otherwise stated, were carried out at a temperature of \( T = 4.2 \) K in a \(^4\)He dewar using standard low frequency lockin techniques at 17 Hz with an excitation current of 50 nA. Sample A yields a maximum electron mobility of \( \mu = 506000 \) cm\(^2\)/Vs at a density of \( n = 4.9 \times 10^{11} \) cm\(^{-2}\) with a cooldown TG voltage of \( V_{TG} = 0 \) V. Sample B gives \( \mu = 258000 \) cm\(^2\)/Vs at a density of \( n = 7.5 \times 10^{11} \) cm\(^{-2}\). In time-resolved measurements of the electron density as a function of the
gate voltage, the density was determined by applying a constant magnetic field $B = 500$ mT while sweeping the gate voltage at sweep rates 1-5 mV/s. For all applied gate voltages, the Hall voltage at zero magnetic field yields 0 V. Hence, the linear dependence between the Hall voltage and B gives the density.

### III. RESULTS

#### A. Gate response

Fig. 1 displays the gate response, i.e. the electron density $n$ of the 2DES as a function of the TG voltage $V_{\text{TG}}$, in an $\text{In}_{x}\text{Ga}_{1-x}\text{As}$ QW embedded in $\text{In}_{x}\text{Al}_{1-x}\text{As}$ with $x = 81\%$ (sample A). The applied gate voltage cycle was the following: the sample was cooled from room temperature (RT) to 4.2 K with $V_{\text{TG}} = 0$ V applied, yielding $n = 4.2 \times 10^{11}$ cm$^{-2}$. The 2DES was then depleted by applying $V_{\text{TG}} < 0$ V (red trace in Fig. 1(b)) until reaching the metal-insulator-transition (MIT). The latter occurred below $n = 1.8 \times 10^{11}$ cm$^{-2}$ (last point of the red trace in Fig. 1(b)). After going to $-4$ V, $V_{\text{TG}}$ was increased: accumulation was then observed from $V_{\text{TG}} = -3$ V onwards (black trace in Fig. 1(b)). A clear hysteresis in the gate response appears, as the black trace differs from the red trace. Both branches exhibit a linear dependence, indicating a classical field effect response to the gate action. However, the black trace has a steeper slope than the red trace, indicating a stronger capacitive coupling of the TG to the 2DES in the QW. Further increasing $V_{\text{TG}}$ towards 0 V, the linear part of the black trace ends at a peak density $n_{\text{peak}} = 4.9 \times 10^{11}$ cm$^{-2}$. Then, although $V_{\text{TG}}$ is still increased, meaning electrons are accumulated in the QW, the measured density quickly decreases, forming a characteristic peak. While increasing $V_{\text{TG}}$ even further, this density drop saturates at $n_{\text{sat}} = 4.3 \times 10^{10}$ cm$^{-2}$ and does not significantly change up to $V_{\text{TG}} = +2$ V. Decreasing $V_{\text{TG}}$ again towards $V_{\text{TG}} = +1$ V results in no reaction of the 2DES density, indicating a loss of the capacitive coupling to the TG between +2 and +1 V. The 2DES reacts again below $V_{\text{TG}} = +1$ V: the electron density decreases (black trace in Fig. 1(b)). Its value at $V_{\text{TG}} = 0$ V precisely coincides with the density observed directly after the cooldown (merging of the black and the red trace in Fig. 1(b)). Finally, decreasing $V_{\text{TG}}$ into negative voltages exactly leads to the red trace in Fig. 1(b), closing the hysteresis loop. We observe this hysteresis loop to remain stable when repeating the described gate voltage cycle.

Regarding the efficiency of the gate control of the 2DES in view of device applications, two major observations hence emerge from Fig. 1(b): the sample allows a significant linear control of the 2DES density with the gate voltage, but this is true in two distinct gate voltage intervals with two different capacitive couplings (red and black trace). Furthermore, the maximal electron density that can be reached within these linear regimes is lower for the branch with the smaller capacitive coupling (red trace). The gate controllability can thus be expected to strongly depend on the electrostatic situation before the cooldown as well as on the gate sweep history of the sample. While this is rarely commented on in the literature, we find these observations to be experimentally in line with the state of the art: when compared, quite different gating properties are reported for similarly designed heterostructures [16–22], seemingly making a correlation between the gating behavior and the heterostructure layout elusive. Given that most of the previous reports used heterostructures with 75\% indium and to further illustrate this point, we show the gate response of sample B in Fig. 1(c): it is a 2DES in a device design which is identical to sample A (81\% indium), apart from the indium content in the semiconductor heterostructure, which has been reduced to 75\% here. While this sample B qualitatively yields the same hysteretic elements as sample A, three striking differences appear: First, when cooling down from RT at $V_{\text{TG}} = 0$ V, the 2DES is now initialized in the steeper linear gate control regime, while in sample A the regime with the stronger capacitive coupling (black trace in Fig. 1(b)) cannot be accessed when simply cooling the device down with $V_{\text{TG}} = 0$ V applied. Second, driving the 2DES in sample B beyond depletion (red trace in Fig. 1(c)) and then accumulating electrons again (black trace), leaves the 2DES unchanged, as the
red and the black trace are identical. In sample A they were not. Finally, and third, the peak electron density \( n_{\text{peak}} = 8.5 \times 10^{11} \text{ cm}^{-2} \) as well as the saturation density \( n_{\text{sat}} = 6.0 \times 10^{11} \text{ cm}^{-2} \) are significantly higher in sample B compared to sample A.

In the following, we will develop a systematic understanding of the observed gating behavior in InGaAs/InAlAs heterostructures. Given that the 2DES properties of both samples strongly depend on the gate sweep history, we will start by discussing the reaction to a modification of the RT electrostatics of the samples.

B. Biased cooldown

To modify the electrostatic environment at RT, we applied certain non-zero \( V_{\text{TG}} \) at RT and then proceeded with the cooldown under the chosen non-zero bias, a procedure termed as biased cooldown (BCd) in the following. Fig. 2 displays the gate response of the 2DES in sample A after four different biased cooldown runs for which the gate voltage \( V_{\text{TG-BCd}} \) applied at RT is decreased from 0 V to \(-20 \text{ V} \). The starting point, which corresponds to the chosen \( V_{\text{TG-BCd}} \) value, is circled in red for each run. The black curve with \( V_{\text{TG-BCd}} = 0 \text{ V} \) is identical to Fig. 1(b) and thus starts in the linear regime with the smaller slope. Applying a negative RT bias \( V_{\text{TG-BCd}} = -6 \text{ V} \) (blue trace) results in two important changes: First, after initializing the gate sweep loop at \( V_{\text{TG-BCd}} = -6 \text{ V} \), the depletion of the 2DES occurs linearly, but now with an intermediate slope. Second, the maximal electron density is increased compared to the black trace (\( V_{\text{TG-BCd}} = 0 \text{ V} \)). Reducing \( V_{\text{TG-BCd}} \) further, to \(-15 \text{ V} \) (green trace), confirms this trend: now, the first measurement point is located in the linear regime with the steepest slope and the maximal electron density is further increased. Additionally, the peak, which concludes the steeper slope regime, is widened. Going even further, to \( V_{\text{TG-BCd}} = -20 \text{ V} \), the MIT already occurs at RT. When increasing \( V_{\text{TG}} \) until electron accumulation (at \(-18.4 \text{ V} \)), the system is initialized in the steeper linear branch, like for the green trace. While the maximal electron density does not further increase between the green and the orange trace, the peak, which concludes the steeper slope regime, is widened into a plateau. From our biased cooldown studies, which are reproducible across several samples and here shown exemplarily for sample A, we draw two conclusions: On a practical level, we here demonstrate from our very general experimental experience across many samples from different heterostructures, that proper biased cooling allows to initialize the gated heterostructure into a well-defined state, for example into the steepest linear slope. Strikingly, the gate response of the green trace in Fig. 2 very much resembles the one of sample B (75% indium and \( V_{\text{TG-BCd}} = 0 \text{ V} \)), shown in Fig. 1(c). Thus, the fact that biased cooling of an 81% indium sample allows to make the gated 2DES behave similarly to a zero-biased 75% indium sample, suggests that the gate response of a sample is closely linked to the intrinsic microscopic electrostatics of the heterostructure. Hence, in the following, we will discuss and analyze the different parts of the gating cycles presented in Fig. 1 and 2.

C. Charge transfer model for the gate response

We divide the gate response hysteresis pattern into characteristic electrostatic regimes, numbered with roman numerals.

![FIG. 2. Electron density n of sample A as a function of V\textsubscript{TG} for four representative biased cooldown voltages V\textsubscript{TG-BCd}. The red circle indicates the first measurement point after cooldown at each V\textsubscript{TG-BCd}.](image)

![FIG. 3. Electron density n of sample B as a function of V\textsubscript{TG} at V\textsubscript{TG-BCd} = 0 V. The different electrostatic regimes, which are discussed in the text, are indicated with roman numerals.](image)
man numerals as presented in Fig. 3. These regimes represent reproducible elements of the hysteresis and do not necessarily coincide with the chronology of the $V_{TG}$ variation after cooling down. The following discussion and the presented charge transfer model (CTM) are supported by the experimental results from many samples, with e.g. different indium contents and different QW depths beyond 50 nm below the heterostructure surface. Exemplarily we will use sample B to illustrate our discussion in this section.

**Regime I** We define the steeper linear segment, which suggests capacitive coupling described by the classical field effect, as regime I. Experimentally, this regime is characterized by two major observations: First, up- and downsweeps of $V_{TG}$ coincide along this branch, and only along this branch: This will not be true in the following regimes. Second, when sweeping $V_{TG}$ to the next measurement value, the electron density instantly reaches its equilibrium value. This instant reaction is again specific to regime I. As we will see later, in other regimes the experimental determination of the electron density will require settling times for the electron density to reach its equilibrium value after each gate action.

**Regime II** Regime I has an upper limit, which appears either as a sharp or more elongated peak (even transforming into a plateau for $V_{TG,BCd} = -20$ V in Fig. 2), defined as regime II. Here, although $V_{TG}$ continues to be increased, the density saturates. This could either be a result of a loss of capacitive coupling between the gate and the 2DES or of a loss of electrons out of the QW. We exclude the loss of capacitive coupling, since the electron density continues to immediately react to a $V_{TG}$ reduction for all voltage values in regime II. While a loss of electrons out of the QW seems counterintuitive at first sight, it becomes more plausible when looking at the band edge sketches of the gated heterostructure in Fig. 4(a) and (b). These schematics are inspired by self-consistent Schroedinger-Poisson calculations, for which we used the parameters from [23] and [24]. Note, that during the MBE growth of InAlAs, the formation of intrinsic crystal defect sites in the form of arsenic antisites is inevitable. These arsenic antisites induce two deep donor level (DDL) states, which lie 0.12 eV and 0.17 eV respectively below the conduction band (CB) edge of InAlAs [24]. These quite effectively act as donor states for InGaAs or InAs QW embedded in InAlAs, creating 2DESs with significant electron densities in these QWs through intrinsic doping, even in nominally undoped heterostructures. Fig. 4(a) depicts the CB edge (black lines) for sample B as well as the evolution of the two energy levels of the DDLs along the growth direction of the heterostructure (dotted colored lines). The electron population is schematically represented by orange dots. Due to the ionization of the DDLs, the evolution of the InAlAs CB edge along the growth direction is curv ed and, in particular, forms a trough-shape between the heterostructure surface and the InGaAs QW. In Fig. 4(a) $V_{TG} = 0$ V is applied to sample B, representative of the system initialized in regime I, in a stable configuration, as observed in the experiment. However, when applying positive $V_{TG}$, the band edge bends downwards in the part left of the QW in the sketch. From a certain $V_{TG} > 0$ V onwards (the start of regime II) this eventually results in the situation sketched in Fig. 4(b). Compared to Fig. 4(a), the sketch illustrates that electrons in the QW now face an increasingly more transparent triangular-shaped potential barrier between the QW and the DDL states in
the InAlAs. Simultaneously, the DDL energy is shifted to be equal or even below the lowest subband of the QW. Hence, an increased tunneling probability from the 2DES into the DDLs is expected. These electrons, which are then trapped in the DDLs in the InAlAs, do not contribute to the transport anymore and thus appear as lost 2DES electrons in our experiment. The dynamics shown in Fig. 4(b) are experimentally verified by the measurement depicted in Fig. 4(c). Sample B (VTG-BCd = −6 V) is first set to regime I at VTG = −4.8 V, from which we sweep VTG into regime II up to −4.0 V while measuring the electron density of the 2DES over time. Regime I is represented by the instant reaction of the electron density to the classical field effect, i.e. increasing linearly with increasing VTG. At VTG = −4.6 V, the density increase then flattens, which we denote as the beginning of regime II. Further increasing VTG leads to a smooth transition into a saturation of the density (although VTG is increased). As soon as the VTG sweep is stopped within regime II, here exemplarily at −4.0 V, the density immediately decreases over a duration of several minutes, illustrating the loss of the 2DES electrons. Additionally Fig. 4(c) shows, that the capacitive coupling of the TG to the 2DES in the QW is not lost. At min 44, VTG is decreased again, which results in an immediate decrease of the density, driven by the classical field effect. This experiment also shows, that a settling time on the scale of several minutes is required for the density to reach its equilibrium value after a specific VTG was set. Only in regime I, the measured density does not require this settling time. Note, that each density point of the measurements presented in Fig. 4(b) and 4(c) hence includes an appropriate settling time on the scale of several minutes.

**Regime III** By applying higher VTG at the regime II peak structure, the band tilting becomes even stronger. Hence, the triangular-shaped potential barrier between the QW and the InAlAs becomes even more transparent, effectively further increasing the tunneling rate of electrons from the QW to DDL sites within the InAlAs. From our experimental observations, we conclude that the electron tunneling rate becomes significantly larger than the increase of the electron density in the QW induced by the increasing VTG here, thus resulting in a clearly visible loss of electrons. In our model, this steep decrease of the 2DES density characterizes regime III. Calculating the distance d between two InAlAs defect sites of the same type yields d ≈ 32 nm. The effective Bohr radius of an electron bound to a doping site is calculated to a∗ ≈ 18 nm. Comparing these two length scales d and a∗ suggests a field-assisted charge transfer through the InAlAs via multi-step hopping. This multi-step process manifests itself within the experiment, particularly in a comparatively long settling time of the electron density after each adjustment of VTG. At the same time, when increasing VTG, the apex of the trough is shifted towards the interface between the semiconductor (sc) and the dielectric. Hence, the increase of VTG will facilitate hopping from the trough apex towards this interface, as sketched in Fig. 5(a). In our understanding,
when electrons arrive at this interface, they get trapped. Indeed, we have good experimental indications for this picture, as for example shown from the gate response in Fig. 5(b): Within a $V_{TG}$ variation in regime I (red trace), no hysteresis occurs, thus the downsweep to $V_{TG} = -7.5$ V and the following upsweep branch are identical. A reversion of $V_{TG}$ after leaving regime I (regimes II and onwards, black curve), at the contrary, results in the opening of a hysteresis, i.e. the branch of the gate voltage downsweep differs from the previous upsweep. The opening of this hysteresis reflects a loss of carriers in the 2DES, which we interpret as a transfer into the interface, where trapping occurs. Our experiments also show, that from regime II onwards this trapping at the interface is quite stable. Indeed, once an electron is trapped inside the interface, we observe that it cannot be brought back by a large negative $V_{TG}$. This is depicted in Fig. 5(c): When regime II is reached (in this case in an upsweep to $V_{TG} = -4$ V) and the hysteresis occurs, neither a subsequent downsweep to $V_{TG} = -7.5$ V nor to $V_{TG} = -9$ V allows to reset the system back to the initial branch from regime I (red trace). In our experiments, only when heating up the sample to RT, the system undergoes the full reset.

Role of the semiconductor-dielectric interface We believe that the observed stable trapping is most plausible at the interface and results from its complex morphology between the interface of the semiconductor heterostructure and the dielectric. First, since this interface marks the sharp transition between the single crystalline semiconductor heterostructure and the amorphous ALD-deposited Al$_2$O$_3$ (dielectric), it will host a significant concentration of point defects which provide an energetically broad distribution of states [27–33], from shallow defects (which induce instabilities due to trap and release) to deep defects (which contribute to metastable trapping). Second, it additionally has been shaped by several environmental influences and sample processing steps - e.g. post-MBE growth oxidation of the InGaAs cap in air as well as a (possibly partial) self-cleaning of the oxidized surface at the beginning of the ALD process [34–41] - creating a spatially inhomogeneous, hump-boat potential landscape at this interface.

Regime IV In the experiments, the density drop in regime III ends with a smooth transition to a density saturation. The electron density then stays constant when further increasing $V_{TG}$. This regime is defined as regime IV. Its appearance indicates that when the interface hosts a sufficient threshold population of trapped negative charges, a partial screening of the electric field from the TG occurs. Indeed, this partial screening should induce a flattening of the band edge profile of the InAlAs compared to the unscreened situation, as depicted in Fig. 6(a). As a consequence, the triangular barrier between the QW and the InAlAs becomes less transparent again, effectively decreasing the tunneling rate from the QW to the InAlAs defect sites. The process which we have just described is self-limiting and thus explains the saturation of the 2DES density: each increase of $V_{TG}$ is

FIG. 6. (a) CB edge sketch of sample B for increasing (large) $V_{TG}$, representative of regime IV. The interface between the semiconductor and the dielectric gets populated. (b) Electron density $n$ of sample B as a function of $V_{TG}$ at $V_{TG,-BCd} = -6$ V within regime VI. The inset shows the applied $V_{TG}$ sweep routine which is discussed in the text. The red circles indicate the transition point of two slopes in each TG downsweep branch. (c) Zoom into (b): the red dotted line indicates the steeper slope value, the blue dotted line the smaller slope and the red circles the transition point between these two slope values.
directly compensated by an equivalent tunneling-assisted screening.

We have good experimental evidence for the fact, that the screening is only partial. To visualize this, one can consider Fig. 5(b) again, which already allowed to illustrate the loss of electrons in regimes II and III. We now consider $V_{\text{TG}}$ downsweeps, which started in regime IV (blue traces with starting points indicated by blue arrows). For any given $V_{\text{TG}}$ value in the range of $-1$ V and $+1$ V, the density always reacts immediately to a $V_{\text{TG}}$ downsweep, as shown by the three blue traces. While the density saturation illustrates the screening, the immediate reaction of the density demonstrates, that the screening is only partial.

While throughout the whole regime IV the system instantly reacts to gate action (although the density saturates), as $V_{\text{TG}}$ is increased further, a point occurs, from which the access to the 2DES, i.e. the capacitive coupling, is lost. This can be seen in Fig. 5(b), where when sweeping $V_{\text{TG}}$ between $+1$ V and $+4$ V (see the three green traces), either in an upsweep or a downsweep (downsweeps indicated by green arrows), the density remains constant. This suggests, that a regime V exists, here beyond $V_{\text{TG}} = +1$ V, in which the capacitive coupling to the 2DES is completely lost.

**Regime V** In our understanding, this experimental observation translates that when a certain critical trapped electron density at the interface is reached with increasing $V_{\text{TG}}$, the partial screening (regime IV) transitions to full screening (regime V). Hence, the density in the 2DES cannot be adjusted anymore through variation of $V_{\text{TG}}$. This has also been reported in comparable gated heterostructures featuring thicker (10 nm) InGaAs cap layers.

Note here, one peculiar observation in our experiments: while the charge density trapped at the interface is large enough to fully screen the action of $V_{\text{TG}}$, it does not contribute to the transport data. Even in this regime V, we do not detect any signature of parallel conduction. This is likely due to the previously mentioned hummocky potential landscape, that has formed at the interface. It seems plausible that such a potential landscape will provide puddle-like minima where charges will locally be trapped. These charges can, at best, hop between puddles and hence only negligibly contribute to the experimental transport signatures.

**Regime VI** Conducting a TG downsweep after going through regimes I - V completes the largest observable gate hysteresis with a branch defined as regime VI, which we denoted as a linear regime with a smaller slope in Fig. 1. In Fig. 3, the slope of the branch in regime VI is significantly smaller than the slope of regime I. We observe that a settling time of the electron density on the scale of several tens of minutes after a variation of $V_{\text{TG}}$ is required in contrast to regime I, similar to the dynamics within regimes II, III and IV, indicating again a substantial charge transfer during regime VI. This motivates a closer look depicted in Fig. 8(b), where a TG downsweep at $V_{\text{TG}} = -1$ V was performed on sample B at $V_{\text{TG,-BCd}} = -6$ V. Sweeping the TG down to $V_{\text{TG}} = -1.2$ V, the density is reduced, revealing the re-occurring of the capacitive coupling after regime V. Stopping at $V_{\text{TG}} = -1.2$ V and waiting for a given duration (horizontal line in the inset from Fig. 8(b)), however reveals a significant increase of the density over several minutes although $V_{\text{TG}}$ is kept constant (indicated by the vertical evolution of the density at $V_{\text{TG}} = -1.2$ V in Fig. 8(b)). Sweeping the TG up after this waiting time unveils a steeper slope for the linear density reaction compared to the slope of the previous downsweep. The density settles instantly in this upsweep and sweeping down leads to no hysteresis. This complex behavior in regime VI can be explained as follows: During the downsweep, a significant charge transfer counteracts the depletion caused by the TG, resulting in the smaller slope. This charge transfer is a re-transfer of electrons, which were previously transferred from the QW towards the interface during the regimes II - V. We cannot distinguish during this re-transfer, whether participating electrons were trapped at the interface or at DDLs. Some of the trapped electrons are irreversibly trapped and cannot be brought back by a large negative $V_{\text{TG}}$ (see Fig. 8(c)), thus they do not contribute to this re-transfer in regime VI. As the QW is energetically favorable, these electrons accumulate in the QW, which we see in the measurement as a smaller slope and as a density increase during a waiting time (e.g. at $V_{\text{TG}} = -1.2$ V). Since the upsweep which follows a waiting time shows a steeper slope and a downsweep in this branch does not open up a hysteresis, the electron re-transfer towards the QW does not operate here. In fact, a hysteresis does not appear as long as a certain $V_{\text{TG}}$ (red circles in Fig. 8(b)) is not reached in a downsweep. This indicates, that the system is in an electrostatic metastable state. Fig. 8(c) shows an enlarged part of Fig. 8(b): When $V_{\text{TG}}$ reaches a red circle, the slope transitions from a larger (red dotted line in Fig. 8(c)) to a smaller (blue dotted line in Fig. 8(c)) slope value. This switching back to a smaller slope value hence marks the recommencement of the electron re-transfer into the QW. Notably, the position of the red circles (i.e. switching back to a smaller slope value) depends on the waiting time before sweeping. This can be seen in Fig. 8(c): The waiting time at $V_{\text{TG}} = -1.2$ V (vertical line in main graph, horizontal line in inset) is significantly larger than the one at $V_{\text{TG}} = -1.4$ V, resulting in a large $\Delta V_{\text{TG}}$ between the waiting time at $V_{\text{TG}} = -1.2$ V and the red circle ($V_{\text{TG}} \approx -1.35$ V) compared to the $\Delta V_{\text{TG}}$ left of the waiting time at $V_{\text{TG}} = -1.4$ V. Hence, the above mentioned electrostatic metastable state largely depends on the previous waiting time in this measurement sequence (downsweep, waiting time, upsweep, downsweep). As the nine sequences in Fig. 8(b) illustrate, the significant electron re-transfer into the QW is present throughout the whole regime VI until the MIT at $V_{\text{TG}} = -3.25$ V is reached. Hence, we show here that regime VI represents an unstable gating
region where a depletion of the 2DES is constantly counteracted by electron re-transfer from the heterostructure into the 2DES.

D. Temperature dependence

The charge transfer processes characteristic of regimes II, III and IV are based on electron tunnelling from the QW into the DDLs in the InAlAs. Hence, they should be enhanced by thermal assistance. Fig. 7(a) thus shows the electron density of sample B as a function of $V_{TG}$ at $V_{TG-BCd} = 0 \, \text{V}$ for four different temperatures. The sample was initialized in regime I, a $V_{TG}$ sweep in positive direction then covers regimes I to IV. Note, that the sample was fully reset at room temperature between each measurement. The observed temperature dependence exactly matches the picture discussed in section C: the multi-step tunneling towards the interface via DDL sites, which marks the transition from regime III to IV, is enhanced by the slightest thermal assistance. This will result in a narrowing of the peak (transition from III to IV) as soon as the temperature is increased, as observed for all four temperatures in our experiment. Also, thermal assistance will render the triangular potential barrier for electrons sufficiently transparent to tunnel into the DDLs at smaller $V_{TG}$: the transition from regime I into regime II sets on for smaller $V_{TG}$. Hence, the peak height (onset of regime II) is reduced. This is indeed observed with increasing temperature (in particular blue and olive traces in Fig. 7(a)).

E. Discussion of the indium content

Our experiments and the discussion in the previous sections point out the importance which the intrinsically present DDLs in InAlAs play in the observed limitations of the gated operation of InAlAs-based heterostructures. Hence, although this has not been addressed in the literature yet, we find that they represent a central parameter in the design of heterostructures for gated operation. Given the intrinsic nature of the DDLs, for example the indium concentration in the InAlAs as well as the depth of the QW below the heterostructure surface will strongly determine the limiting impact of the DDLs on the gate operation.

For example, the gate operation limitations of sample A (81% indium) compared to sample B (75% indium) reported in Fig. 1 can consistently be explained within our model and be tracked down to the DDLs in InAlAs. The band edge schematic of sample A (81% indium) is depicted in Fig. 7(b) and should be compared to Fig. 4(a) for sample B (75% indium). We assume here, that the energy difference between the DDLs (dotted colored lines) and the InAlAs CB edge is independent of the indium concentration in InAlAs. However, the band offsets between InAlAs, InGaAs and InAs decrease with an increasing indium concentration. As a consequence, for high indium concentrations, tunneling from the QW into the DDLs will be enhanced already at $V_{TG} = 0 \, \text{V}$ (see Fig. 7(b)), while it is forbidden for lower indium concentrations (see Fig. 4(a)). Two experimental features reported in our comparison of samples A and B in Fig. 1 directly result from this enhanced tunneling: First, the maximal accessible electron density as well as the saturation concentration is smaller in the sample with the higher indium concentration, sample A. Here, the onset of the multi-step hopping tunneling from the QW via InAlAs DDLs towards the interface (i.e. onsets of regimes II and IV) requires less gate action compared to a heterostructure with a lower indium concentration. Hence, when starting the gate operation in regime I (see Fig. 1), with similar electron densities, due to this earlier onset of multi-step tunneling, the maximum density (reached at the end of regime I) is smaller for sample A (81% indium) than for sample B (75% indium). The same is true for the saturation electron density observed in regimes IV and V (see Fig. 1). Second, for sample A, already at $V_{TG} = 0 \, \text{V}$, the reduced band offsets with increasing indium content induce an electron population in the area of the trough formed by the DDL energy levels in the schematic...
in Fig. 2(b), as indicated by the orange dots. As a consequence, when cooling down sample A at \( V_{\text{TG}} = 0 \) V, the gated system will be initialized in the unstable electrostatic regime VI, as observed in Fig. 1. As explained by our CTM, the device can only be brought into the stable regime I by applying sufficiently negative \( V_{\text{TG}} \) to depopulate the DDLs. At the contrary, in sample B (lower indium concentration), negligible multi-step tunneling occurs at \( V_{\text{TG}} = 0 \) V (see Fig. 1(a)), even at RT. Hence, as discussed in Fig. 1, sample B is initialized in the stable gating regime I.

We have shown in Fig. 2 that sample A may also be initialized in the stable regime I, provided that a negatively biased cooldown is applied (see green and orange traces in Fig. 2). This is in accordance with our CTM, since, by applying a sufficiently negative \( V_{\text{TG,BCd}} \) at RT, the DDLs are depopulated as well as charges trapped at the interface. Then stable gate operation is allowed after the cooldown at this \( V_{\text{TG,BCd}} \). Note that, as a direct consequence of this depopulation of charges, the biased cooldown brings the advantage of enabling a gate operation up to a higher electron density compared to the initialization at \( V_{\text{TG}} = 0 \) V, as seen from the comparison of the orange and green traces with the black one in Fig. 2.

IV. CONCLUSION

In conclusion, our experimental study and charge transfer model identify the deep donor levels induced by spin-orbitronics. In particular, trying to maximize the spin-orbit interaction in 2DESs on the one hand, they at the same time substantially determine the electrostatics of the heterostructure through charge trapping and unintentional tunneling events. As a consequence, they thus impose limitations which need to be taken into account for a top-gated operation of 2DESs in such heterostructures. Strikingly, an electrostatically stable gate operation will quite generally only be possible in a limited gate voltage range. A much broader voltage range will then display reduced, to vanishing, capacitive coupling of the gate to the 2DES, induced by unstable or metastable electrostatic configurations, which are governed by charge transfer processes with long time scales. We have shown that the design of the heterostructure - most importantly the indium content - crucially impacts in which electrostatic configuration a sample is initialized after cooldown. Our model allows to qualitatively predict how such heterostructures will react to gate operation and how to reach the electrostatically stable regime I. It also explains the observed favorable action of negative biased cooling to initialize a gated heterostructure in regime I with maximized accessible electron density. Hence, the presence of the deep donor levels should be accounted for in the design of heterostructures for spin-orbitronics. In particular, trying to maximize the spin-orbit interaction through an increase of the indium content, will at the same time minimize the accessible electron density in gate operation.

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