A neuromorphic systems approach to in-memory computing with non-ideal memristive devices: From mitigation to exploitation

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Memristive devices represent a promising technology for building neuromorphic electronic systems. In addition to their compactness and non-volatility features, they are characterized by computationally relevant physical properties, such as state-dependence, non-linear conductance changes, and intrinsic variability in both their switching threshold and conductance values, that make them ideal devices for emulating the bio-physics of real synapses. In this paper we present a spiking neural network architecture that supports the use of memristive devices as synaptic elements, and propose mixed-signal analog-digital interfacing circuits which mitigate the effect of variability in their conductance values and exploit their variability in the switching threshold, for implementing stochastic learning. The effect of device variability is mitigated by using pairs of memristive devices configured in a complementary push-pull mechanism and interfaced to a current-mode normalizer circuit. The stochastic learning mechanism is obtained by mapping the desired change in synaptic weight into a corresponding switching probability that is derived from the intrinsic stochastic behavior of memristive devices. We demonstrate the features of the CMOS circuits and apply the architecture proposed to a standard neural network hand-written digit classification benchmark based on the MNIST data-set. We evaluate the performance of the approach proposed on this benchmark using behavioral-level spiking neural network simulation, showing both the effect of the reduction in conductance variability produced by the current-mode normalizer circuit, and the increase in performance as a function of the number of memristive devices used in each synapse.

Neuromorphic computing systems comprise synapse and neuron circuits arranged in a massively parallel manner to support the emulation of large-scale spiking neural networks. In many of these systems, and in particular in neuromorphic processing devices designed to overcome the von-Neumann bottleneck problem, the bulk of the silicon real-estate is taken up by synaptic circuits that integrate in the same area both memory and computational primitives. To save area and maximize density in such devices, one possible approach is to implement very basic synapse circuits arranged in dense cross-bar arrays. However, such approach is likely to relegate the role of the synapse to a basic multiplier. In biology, synapses are extremely sophisticated structures that exhibit complex and powerful computational properties, including temporal dynamics, state-dependence, and stochastic learning behavior. The challenge is to design neuromorphic circuits that emulate these computational properties, and are also compact and low power. Memristive devices have recently emerged as nano-scale devices which provide a promising technology for addressing these problems. These devices offer a compact and efficient solution to model synaptic weights since they are non-volatile, have a nano-scale footprint, might only require little energy to change their state, and in addition can emulate many of the synaptic functions observed in biological synapses. However, these devices are also characterized by non-idealities that introduce significant challenges in designing neural network architectures applied to classification and recognition tasks. In particular, one property of memristive devices that introduces significant challenges in the design of large scale neural network architectures is the large variability of their operational parameters. Memristive devices represent a promising technology for building neuromorphic electronic systems. In addition to their compactness and non-volatility features, they are characterized by computationally relevant physical properties, such as state-dependence, non-linear conductance changes, and intrinsic variability in both their switching threshold and conductance values, that make them ideal devices for emulating the bio-physics of real synapses. In this paper we present a spiking neural network architecture that supports the use of memristive devices as synaptic elements, and propose mixed-signal analog-digital interfacing circuits which mitigate the effect of variability in their conductance values and exploit their variability in the switching threshold, for implementing stochastic learning. The effect of device variability is mitigated by using pairs of memristive devices configured in a complementary push-pull mechanism and interfaced to a current-mode normalizer circuit. The stochastic learning mechanism is obtained by mapping the desired change in synaptic weight into a corresponding switching probability that is derived from the intrinsic stochastic behavior of memristive devices. We demonstrate the features of the CMOS circuits and apply the architecture proposed to a standard neural network hand-written digit classification benchmark based on the MNIST data-set. We evaluate the performance of the approach proposed on this benchmark using behavioral-level spiking neural network simulation, showing both the effect of the reduction in conductance variability produced by the current-mode normalizer circuit, and the increase in performance as a function of the number of memristive devices used in each synapse.

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tive device variability exhibits itself in different forms, both between device to device (spatial) and from cycle to cycle within a single device (temporal). This variability therefore manifests itself both in the device conductance values and in their switching voltage. Device-to-device variability originates from process variations which also exists in current CMOS process, while the cycle-to-cycle variability stems from the underlying switching mechanism of memristors. The cycle-to-cycle variability is observed in different types of memristors, from Phase Change Memories (PCMs) and Conductive Bridge RAMs to ionic redox-based resistive RAMs. In particular, in the latter case, the underlying mechanism for this variability is associated with the formation and rupture of a conducting filament. Filament formation involves oxidation, ion transport and reduction which are all thermodynamical processes and as a result require overcoming an energy barrier. Therefore, the switching involves thermal activation to surpass the barrier and thus is a probabilistic process. In other words, for the same devices and the same filament, the nature of the switching events will occur randomly and is thus stochastic.

To summarize, the variability in memristive devices results in a distribution of different parameters that can be categorized in four distinct groups:

G1 Distribution of the switching voltage of a single device
G2 Distribution of the high and low resistive states of a single device
G3 Distribution of the switching voltages among multiple devices
G4 Distribution of the high and low resistive states among multiple devices

The variability of parameters across multiple devices (e.g., for groups G3 and G4) can be mitigated and managed for example by considering only binary states by implementing “compound” synapses that employ multiple memristive devices per synaptic element, or by interfacing the memristive devices to CMOS processing stages that reduce the effect of their variability. Conversely, the cycle-to-cycle variability (e.g., in groups G1 and G2) can be managed by using feedback control to set the desired state to a well-defined value, which requires a large overhead control circuit, or it can be exploited as a means to implement stochastic learning in spiking neural networks. Indeed, it has been shown that employing binary synapses, variability and randomness in their switching threshold in spiking neural networks greatly improves the convergence of the network and provides a form of regularization which substantially improves the network generalization performance. In the case of neural networks with low resolution synapses, it has been shown that a randomized gradient descent method significantly outperforms naive deterministic rounding method.

Memristive devices are a promising emerging technology for use in large-scale neural network architectures. Employing such devices in neural processing systems for robust computation in real-world practical applications calls for ways to either mitigate their non-idealities, to exploit them, or to combine the best of both approaches in the same architecture. In this paper we present a spiking neural network architecture that support the use of variable and stochastic memristive devices for robust inference and probabilistic learning. We show that by combining such devices with state-of-the-art mixed-signal digital and analog subthreshold circuits, it is possible to build electronic learning systems with biologically plausible functionality which can process and classify sensory data directly on-chip in real-time, and which represent ideal technologies for always-on edge-computing neural network applications. We propose synapse-CMOS interfacing circuits that dramatically reduce the effect of device-to-device variability, as well as spike-based learning circuits that are compatible and exploit the device cycle-to-cycle variability to implement stochastic learning. We validate the functionality of such circuits by applying the neural network architecture to a pattern classification task, using a standard digit recognition benchmark based on the Modified National Institute of Standards and Technology (MNIST) data-set. In the next section we describe the spiking neural network architecture, explain its basic principle of event-based operation, and present its main neuromorphic building blocks; in Section 2 we present the memristive synapse circuits and their related current-mode sense circuits used to reduce the device-to-device variability for improving the network performance in its inference phase; in Section 3 we present the spike-based stochastic learning circuits that exploit the devices cycle-to-cycle variability for inducing probabilistic state changes in the network synaptic weights; Section 4 presents behavioral simulations results at the system level, in the hand-written digit recognition benchmark to validate the proposed circuits and approach; finally in Section 6 we present the concluding remarks.

1 The neuromorphic architecture

The spiking neural network architecture that supports the use of memristive circuits as synapse elements is shown in Fig. 1. This architecture expects input spikes and produces output spikes that are encoded as Address-Events: each neuron is assigned a unique address, and when it produces an output spike, a corresponding digital pulse is encoded on a common shared time-multiplexed bus with its corresponding address. Potential collisions arising from multiple neurons requesting access to the same bus are handled by asynchronous arbiter circuits, that are part of the Address-Event Representation (AER) protocol. In this protocol, the analog information present in the silicon neuron is encoded in the time interval between its address-events. The asynchronous nature of this communication protocol ensures that precise timing information is preserved, and signals are transmitted only when there is neural activity. As neural activity in spiking neural networks is typically sparse in both space and time, this protocol is ideal for minimizing power-consumption and maximizing bandwidth. The architecture of Fig. 1 comprises multiple rows of neurons, each composed of multiple Memristive Synapse (MR) elements, Integrate and Fire (I&F) soma circuits, and additional interfacing circuits for managing the input pulse shapes, the synaptic currents, their temporal dynamics, and the spike-based learning mechanism. Upon the arrival of an input Address-Event, this is decoded by the AER input circuits into a one-hot
Fig. 1 Neuroromorphc architecture comprising multiple silicon neurons, each receiving inputs from CMOS-memristive synapse elements. MS is short for Memristive Synapse, PS for Pulse Shaper, NC for Normalizer Circuit, DPI for Differential Pair Integrator, I&F Neuron for Integrate and Fire Neuron, LB for Learning Block and PC for Programming Circuitry.

Fig. 2 Pulse shaper (PS) block schematic. With the arrival of an input event from the AER block, two consecutive pulses Read and Write are generated by two digital Pulse Extender circuits.

Fig. 3 A single Memristive Synapse (MS) block of the proposed neuromorphic system. The devices $D_{pos}$ and $D_{neg}$ are modeling the excitatory and inhibitory synapses respectively. When the Read pulse signal from the corresponding column is active, the excitatory currents sum together on the excitatory $\sum I_{exc}$ and the inhibitory $\sum I_{inh}$ lines. Similarly, when the Write pulse is high, the switches connect the devices to the programming lines.

This decoded pulse is then converted by a dedicated Pulse Shaper (PS) circuit, which produces a Read and a Write pulse, used to measure the currents through the memristive synapse elements and potentially change their conductance values correspondingly. A schematic diagram of the PS circuit is shown in Fig. 2. The pulse extender circuit block in the figure is based on a classical starved-inverter circuit, and has been characterized in previous work [52]. The output of the PS block is then broadcast to all MS synapse blocks of the corresponding column. Each MS synapse comprises one pair of memristive devices arranged in a complementary configuration (see $D_{pos}$ and $D_{neg}$ of Fig. 3). The pairs of devices are arranged in a way to produce positive contributing currents (modeling excitatory synapses) and negative contributing ones (modeling inhibitory synapses) during the “read-phase”, and are updated in a push-pull way during the “write-phase” (i.e., if the conductance of one device is increased, the conductance of the complementary device is decreased, and vice-versa). Specifically, during the read phase, the $V_{drive}$ voltage of Fig. 3 is set to a small value, such that small currents (e.g., of the order of nano-Ampere) will flow through the memristive pair onto the separate positive and negative summing lines. Conversely, during the write phase, digital control signals disable the connection to the current summing lines and enable the connection to the weight update Programming Circuits (PC), which set the $V_{drive}$ signal to either $V_{dd}$ or Gnd depending on the sign of Error signal produced by spike based learning Block (LB) of the corresponding row.

During the read phase, the output currents produced by all MS blocks along a row in the architecture are summed through Kirchhoff’s current law and conveyed to a Normalizer Circuit (NC) block. This is a current-mode circuit based on the Gilbert normalizer circuit [53] which receives the positive and negative contributions of currents from the memristive devices and produces two corresponding output currents that are scaled and normalized appropriately. As this circuit plays a fundamental role in reducing the effect of device variability across all memristive de-
vices present in the neuron row, we describe its functionality in detail in Section 2.

The positive and negative output currents produced by the NC block are then sent to two separate Differential Pair Integrator (DPI) circuits. These are current-mode linear integrator filters that integrate the incoming current pulses and produce temporally decaying currents that faithfully model the Excitatory Post Synaptic Current (EPSC) and Inhibitory Post Synaptic Current (IPSC) counterparts of real biological synapses. The difference between positive and negative synaptic current contributions is then sent into the I&F soma block, that temporally integrates these currents and produces an output spike as soon as the integrated current reaches the neuron’s firing threshold. Both DPI and I&F blocks have been fully characterized and explained in a previous work.

The output spikes of the I&F block are sent to the AER output circuits, as well as to an additional DPI circuit that integrates the neurons spikes. The output current of this DPI circuit (see iNeuron of Fig. 1) is proportional to the neuron’s average firing rate. It is sent as input to the neuron’s Learning Block (LB), which compares the neuron’s output firing rate to a desired target value, and produces an error signal that is proportional to the difference. This error signal is then used by the corresponding row Programming Circuit (PC) block to change the probability of synaptic weight update in the synapses that were stimulated by the incoming Address-Event. These circuits implement the probabilistic “Delta” learning rule used in the architecture, and they are fully described in Section 3.

2 The memristive current normalizer circuit

The memristive current normalizer circuit is shown in Fig. 4. The circuit is operated in the weak inversion, or subthreshold domain where transistors have an exponential transfer function, in order to reproduce the functionality of the Gilbert-normalizer element which was originally designed for use with bi-polar transistors. The input signals to this circuit are given by the sum of the currents measured across the memristive devices in the corresponding neuron row (see also Fig. 1). The circuit has a differential input, provided by the positive and negative summing lines of the circuit’s row. As these input currents are proportional to the values of the memristive devices, they can be affected by a large variation in their values. However, it has been demonstrated that the normalizer output currents I_{pos} and I_{neg} of Fig. 4 can be approximately expressed as function of the input currents \( \sum I_{exc} \) and \( \sum I_{inh} \), which in turn are proportional to the memristive device conductances:

\[
I_{pos} = I_b \frac{\sum I_{exc}}{\sum I_{exc} + \sum I_{inh}} \quad I_{neg} = I_b \frac{\sum I_{inh}}{\sum I_{exc} + \sum I_{inh}} \quad (1)
\]

Since in each Memristive Synapse block the memristive devices are arranged in a push-pull configuration (see Fig. 3), large \( \sum I_{exc} \) currents will typically result in small \( \sum I_{inh} \) currents and vice-versa.

In the extreme case, when all conductances of one type (e.g., excitatory) are in the high state and the conductances of the other type (e.g., inhibitory) are in the low state, one output current of the circuit will be approximately equal to the maximum possible value (e.g., \( I_{pos} \approx I_b \)) and the other to the minimum value, which is set by the transistor leakage current. It is due to this strong non-linear behavior that the normalizing function of eq. (1) has the remarkable effect of reducing the effect of device mismatch.
in their conductance values. Examples of the variability reduction features of the circuit are illustrated in Figures 5a and 5b. Figure 5a shows the effect of the normalizer circuit on its output currents for a typical distribution of device conductances that was derived from the literature. Monte Carlo circuit simulations were run to obtain these plots where 50 values of low and high conductance states were sampled and plotted in 20 bins. Dashed lines show the sampling distributions for device high and low conductance states in 5a. 5b shows the distribution of the output currents from the normalizer circuit. The insets in Figure 6a show the resulting output current distributions in finer detail where the range of observed values for $I_{pos}$ and $I_{neg}$ are plotted in 10 bins without normalization.

Fig. 6 Histograms highlighting the differential memristive synapse synaptic weight storage behavior for high/low resistance ratio of 10: (Mean, Std Dev) for $\Omega_{Dneg} = (2.931 \Omega, 582 \Omega)$, $\Omega_{Dpos} = (30.35 \Omega, 5.71 \Omega)$. The stochastic learning mechanism we propose exploits this effect of device variability almost completely as the output currents of the normalizer circuit can be scaled to very small subthreshold current values (e.g., in the range of pico-Ampere), the power consumption of the neural processing circuits downstream can be kept very low. Furthermore, this makes the downstream circuits more compact as they can use smaller capacitors to implement temporal dynamics with biologically plausible time constants (e.g., for allowing real-time interaction with the environment). In addition to mitigating the effect of device variability, the differential operation used in the architecture proposed has the advantage of allowing the use of both positive (excitatory) and negative (inhibitory) weights, effectively doubling the “high-low” dynamic range of the memristive devices.

3 The stochastic learning circuits

In this section we propose circuits that can be interfaced to memristive devices to exploit the cycle-to-cycle variability in their switching characteristics to implement stochastic learning. Indeed, the cycle-to-cycle variability in the switching of memristors provides an intrinsic stochastic process that can be used to update the weights of the synapses in a neural network. The probabilistic switching in the memristor devices has been observed and studied before which is believed to stem from the formation and dissolution of a filament between the device electrodes. The authors claim that the results can be generalized to other memristive systems such as OxRAMs. The Poisson distribution suggests that the switching events are independent from each other and that the probability of a switching event occurring within $\Delta t$ at time $t$ is $P(t) = \frac{\Delta t}{\tau} e^{-t/\tau}$, where $\tau$ is the characteristic wait time which is the mean time after the application of the SET pulse in which the device switches. A thorough study on the effect of the applied SET voltage $V$ on the wait time has been performed which shows that as the applied voltage across the device increases linearly, the characteristic wait time decreases exponentially. Therefore, $\tau(V) = \tau_0 e^{-V/V_0}$ where $\tau_0$ and $V_0$ are fitting parameters found by the experimental measurements. Employing this model, the probability of switching for $t < \tau$ can be written as:

$$P(t) = \frac{\Delta t}{\tau} e^{-t/\tau}$$

The stochastic learning mechanism we propose exploits this characteristic in an event-based network which comprises binary synapses, implemented using memristive devices that are driven...
the effective output spike rate, the expected weight change resulting from a switching is thus proportional to the derivative of this difference squared: In expectation the circuit error signal, as defined in eq. (4). The precise value of this voltage is very important, as the probability of switching of a memristor is exponentially dependent on the voltage across it. However CMOS device mismatch and memristive device variability do not allow the use of a single constant voltage shared across all synapses. Although analogous efforts have been proposed in the literature, implementing calibration circuits to precisely control the voltage biases in each synapse would result in a very bulky design with large overhead circuitry and time-consuming calibration procedures at run time.

Rather than attempting to solve the device mismatch and variability effects with brute-force approaches, we exploit the stochastic nature of the learning algorithm: by generating a time-varying voltage ramp signal and applying it to the memristive devices in the weight-update phase, we can sweep across all values of the distribution of voltages that can affect the device switching behavior. Specifically, we propose a circuit that generates a ramp voltage with a slope $\alpha$ that is proportional to the logarithmic value of the error signal, as defined in eq. (4).

By applying this voltage ramp to the memristive devices, the switching probability of the devices becomes proportional to $i_{\text{Target}} - i_{\text{Neuron}}$. Since $i_{\text{Target}}$ is the desired output spike rate and $i_{\text{Neuron}}$ the effective output spike rate, the expected weight change resulting from a switching is thus proportional to the derivative of this difference squared: In expectation the circuit

$$I_1 = I_{b1} \frac{i_{\text{Neuron}}}{i_{\text{Neuron}} + i_{\text{Target}}}; \quad I_2 = I_{b1} \frac{i_{\text{Target}}}{i_{\text{Neuron}} + i_{\text{Target}}}$$

(6)
implement a gradient descent procedure on this squared error. The time varying ramp signal modulates the probability of resistive switching such that high errors results in more probable switching and vice versa.

This strategy implements a form of “Randomized Rounding” on the Delta-Rule, which has been shown to be more effective than deterministic rounding in a similar context.

The circuit that produces this voltage ramp is shown in Fig. 8.It is a global circuit shared by all the Memristive Synapse (MS) blocks of a neuron row (see PC block Fig. 1). The generation of the voltage ramp is triggered every time an input spike-event produces a Write pulse from the PS block of Fig. 2. During this period, the circuit is operational and receives as input the analog signals V1, V2, and the digital one UP. Given the subthreshold mode of operation, the output voltage signals of this circuit V3 and V4 can be expressed as:

$$V3 = \frac{U_T}{k} \log\left(\frac{\Delta I}{I_0}\right) \quad \text{if} \quad \Delta I > 0$$

$$V4 = \frac{U_T}{k} \log\left(-\frac{\Delta I}{I_0}\right) \quad \text{if} \quad \Delta I < 0$$

(7)

where $\Delta I$ is defined as $i_{Target} - i_{Neuron}$, $k$ and $I_0$ are the process-dependent subthreshold slope factor and reverse biased leakage current respectively, and $U_T$ is the thermal voltage.

Now, to generate the desired ramp voltage, we need to convert the $(V3 - V4)$ voltage difference to a current that can charges/discharge a capacitor linearly. This is achieved by using a transconductance amplifier to produce the current $I_{out}$:

$$I_{out} = I_{h2} \tanh\left(\frac{k}{2U_T} (V3 - V4)\right)$$

(8)

It is safe to assume that the $\tanh$ function of eq. (8) is operating in its linear region, since $V3$ and $V4$ are generated from $V1$ and $V2$ in circuits of Fig. 7 which operate in the subthreshold region.

The ramp voltage $V_{pr}$ thus becomes:

$$V_{pr} = \frac{V_{dd}}{2} + \frac{I_{out}}{C_1} \Delta_{Write} = \frac{V_{dd}}{2} + \frac{I_{h2}}{2C_1} \log\left(\frac{\Delta I}{I_0}\right) \Delta_{Write}$$

(9)

where $\Delta_{Write}$ is the duration of the write-phase during which the memristors is programmed. The voltage $\frac{V_{dd}}{2}$ is the value to which the capacitor is pre-charged before and after the write-phase.

This voltage is applied to the memristive synapse that was stimulated by the input spike-event, using the polarity defined by the UP and DN signals produced by the Learning Block of the corresponding row. As the ramp generator circuit is shared among all the synapses of a row, any other incoming spike-event received during the write-phase will be ignored. It has been shown that this assumption holds as long as the average rate of input spikes is slower than the write-phase ramp duration.

As the online learning proceeds and the neuron’s mean activity approaches the target value, the magnitude of the current $I_{out}$ of the PC circuit (see Fig. 8) decreases and as a consequence the slope of the ramp decreases. Since the probability of switching for the memristive devices is practically zero for voltages much lower than the “nominal threshold voltage” this implementation induces a “stop-learning” zone in which no change is applied to the state of the devices. It has been shown how this strategy of having a region of operation by which the weight-updates are disabled, when the learning error value decreases below a set threshold improves the stability of the learning process and the convergence properties of the network. Furthermore, this strategy has the important feature of enabling continuous time “always on” learning operations, without having to artificially separate the training phase from the test phase.

To validate the analysis presented above we carried out circuit simulations of both the Learning Block and the Programming Circuit of Fig. 7 and Fig. 8 for a standard 0.18 $\mu$m CMOS process. Figure 9 shows the circuit simulation results, for both cases of the error signal $\Delta$ greater and less than zero. The plots show also the fit of eq. (9) with the data for $I_{h2} = 500a$, $I_{h3} = 100na$, $C_1 = 300fF$ and $\Delta = 10\mu$secs. As depicted in the figures, the circuit outputs closely match the fits.

4. System-level behavioral simulations

To evaluate the effects of various sources of variability on the performance of the network and circuits proposed we carried out system-level behavioral simulations of the network, applied to a linear classification task using the MNIST hand-written digit dataset, comprising a training set for the learning phase and a test set for the validation phase. We compared the network performance on the test set after training on the training set in four cases:

1. Rate-based neural network with floating point synaptic precision trained by standard gradient-descent method as a baseline for comparing the accuracy of the network.
2. Spiking neural network with ideal binary devices trained by probabilistic gradient descent (as explained in Section 3).
3. Spiking neural network with non-ideal binary devices having high variability in their resistance value (20% of standard
4. Spiking neural network with non-ideal binary devices of item 3, whose variations are suppressed using the variability reduction circuit presented in Section 2 and trained by probabilistic gradient descent.

To compare the network to previously published results, we used a configuration analogous to the setup presented in the work of Bill and Legenstein, who used a model of memristive elements in an unsupervised Winner-take-all network to learn digit prototypes for digits zero to four. A downscaled network of this kind has been partially verified in hardware recently. This setup is also comparable to other setups for previous simulations done by our group.

We carried out spiking neural network simulations using the Brian2 simulator and neuron model equations that match the transfer function of the silicon memristor circuit and DPI filters.

used in the architecture. In these simulations, we combine for the first time a stochastic learning algorithm with a variability compensation method. Both are based on different variability characteristics of memristors: The stochastic learning algorithm uses the cycle-to-cycle variability in the switching probability of a memristor for a given voltage ramp, the variability compensation addresses the device-to-device (and cycle-to-cycle) variability in conductance level of a memristor.

The gray-level MNIST input images were re-scaled to image sizes of $24 \times 24$ and their pixel values were converted to Poisson spike trains with a mean firing rate proportional to the pixel intensity. To obtain higher resolution effective connections from each input pixel while using binary synaptic elements we encoded the pixel values with multiple instances of spiking neurons. Specifically, each pixel was associated to a number $n_c$ of spiking neurons in the input layer, that stimulated a corresponding number of synaptic elements of a target “compound synapse” (comprising $n_c$ devices instead of two) in the network output recognition layer. In this way, the synaptic connection strengths have $2 \times n_c$ effective levels, instead of two. The total number of neurons in the input layer is therefore $n_c \times (24 \times 24)$. The output recognition layer is composed of five read-out neurons (one for each digit type zero to four), each of which comprises a row of $(24 \times 24)$ compound synapses, with each compound synapse containing $n_c$ memristive devices.

The neuromorphic architecture used in these system level behavioral simulations is the one described in Section 1. The parameters used to encode the synaptic weights are either two precise discrete values (with no variability), in the case of idealized synaptic elements, or are random numbers that follow a bi-modal distribution based on measured data from memristive device properties, as given in Fig. 5a and 6a. Note that the coefficient of determination, which is a statistical measure of how close the data are to the fitted line, is composed of five read-out neurons (one for each digit type zero to four), each of which comprises a row of $(24 \times 24)$ compound synapses, with each compound synapse containing $n_c$ memristive devices.
input presentation and compared it’s identity to the label of the pattern provided in input. If more than one output neuron spiked, the neuron that spiked the most was chosen as the one encoding the learned label.

Figures 10 and 11 show the performance of the proposed architecture. As a base-line comparison (that we expect to upper bound the performance of this setup) we also trained a standard linear classifier with 32-bit floating point synaptic elements and 32-bit rate based neurons using stochastic gradient descent. This baseline reaches circa 2.9% ± 1% test set error. The discrepancy to the circa 10% error of our best simulation, can be explained by the low resolution of synaptic memory, the single bit communication channels of spiking neurons and the lossy input encoding in Poisson spike trains. An intermediary idealized setup, only controlling for memristive conductance variability, but incorporating other non-idealities is given by the ‘ideal binary’ simulations (see the green bars in Fig. 10 and 11). The network simulations with different types of synapse models (i.e., basic un-normalized linear conversion case, and current-normalizer conversion case) show how the normalization circuit decreases the classification error overall. By comparing the error-bars on the un-normalized (red bars) and normalized (blue bars) simulation results in Fig. 10 and 11 it is evident how the normalization circuit decreases also the variance in the error. We speculate that the reason for this is the more stable update size of the normalized setup.

Figure 12 shows examples of synaptic weight matrices of the five different neurons that were trained to recognize the five different digits, for the case in which \( n_c = 4 \). These synaptic weight matrices can be interpreted as “receptive fields” of the trained neurons which correspond to the best discriminatory features (e.g., positive weights for prototypes of the digit the neurons are supposed to classify intermixed with negative weights for the digits that they are supposed to ignore).

Overall these simulations show that changes on the behavioral level of a small neural network can be influenced by low-level characteristics of the building blocks of the neurons that comprise it. Specifically we have shown that the probabilistic switching behavior of memristors can be used as a powerful computational primitive in a learning setting, and that variability in conductance levels of memristors can be effectively (in the sense of high-level performance) mitigated by appropriate normalization with a compact circuit.

5 Discussion

5.1 Supporting different modes of memristive device operation

Although in this paper we focus on the use of memristive devices as binary elements, the architecture proposed can potentially support the full spectrum of memristive behaviors that has been reported in the literature:

1. Stochastic binary
2. Multiple binary devices in parallel (compound synapse)
3. Stochastic multiple discrete levels
4. Almost analog

In the case of binary synapses, we showed how the proposed stochastic learning circuits enable the architecture to achieve acceptable performance on the MNIST test bench. The system-level behavioral simulations demonstrated that the use of compound synapses improves the classification performance, and quantified the improvement factors.

It has been shown in the literature, how gradual conductance modulation of memristive devices can be observed when pulses are applied for a short amount of time. Under these conditions controlling the number of pulses applied to the device can be used as a way to tune the desired conductance values. The architecture proposed can support this regime of operation by appropriately setting the pulse height and/or duration via the LB and PC blocks of Section 3. The same circuits can be extended to produce a tunable number of short pulse sequences.
by enabling a ring oscillator for the desired duration. This latter strategy would allow us to implement learning with gradual changes, rather than binary probabilistic one, by encoding the desired change in weight $\Delta w$ with the number of pulses generated by the ring oscillator. It is worth noting that the same memristive device can be tuned to behave as a binary one or multi-level one by adopting different biasing and operating conditions. For example, even for a fixed set-voltage, it is possible to operate the same device in the binary or analog region by changing the length of the Write pulse in the PS block of Fig. 2. Longer pulses will drive the device into the binary mode, while shorter ones will exhibit more of an analog behavior.

5.2 Exploiting device mismatch and variability to improve classification accuracy

In this paper we have presented analog CMOS circuits that can be interfaced to memristive devices to mitigate the effect of their device variability. A remarkable feature of the use of analog CMOS circuits used to implement also synapse and neuron dynamics is the fact that their device mismatch non-idealities can be exploited to improve the network classification performance. Indeed, device mismatch across multiple memristive synapses and silicon neurons, the very phenomenon that decreases the classification performance of one single binary classifier (e.g., one Perceptron or neuron row of Fig. 1) and that engineers tend to minimize with brute-force approaches, can be embraced to build highly accurate classifiers composed of ensembles of single ones. This can be demonstrated by the theory of ensemble learning. There are two broad classes of algorithms that fall in the category of ensemble learning: Bagging and Boosting.

Bagging or bootstrap aggregating is an averaging technique proposed by Breiman where a collection of M classifiers are trained on M equally-sized subsets of the full training set created with replacement. The predictions made by the ensemble of M classifiers are then averaged to make the final prediction.

Boosting is a technique that uses a collection of un-correlated weak classifiers (whose accuracy is only slightly better than chance) to build a strong-classifier (whose prediction error can be made arbitrarily small). One of the most popular variants of the approach is called the AdaBoost algorithm. Unlike the bagging approach, every weak classifier in the ensemble is exposed to the full training data, where each sample is associated with an observation weight during training. For training the first classifier, the weights are kept equal for every training sample. When training the second classifier, the sample weights are adjusted such that the misclassified samples by the first classifier have a higher weight. A weight is also assigned to each classifier based on its prediction accuracy. This process is continued till the desired number of weak classifiers are generated. The final prediction from the ensemble is a weighted sum of the weak-classifier predictions.

These ensemble learning principles can indeed be applied to the neuromorphic architecture proposed in Section 1 to asymptotically improve the accuracy of the system. In particular, the Bagging approach is immediately applicable to the system, by simply sending the same input patterns to multiple neuron rows and training ensembles of neurons to recognize the same class. The variability in the synapse and neuron circuits is already sufficient to make sure that each neuron acting as a “weak” binary classifier behaves in a way that is different from the other ones belonging to the same ensemble. However, to truly ensure that the weak classifiers are fully independent it would be sufficient to train each neuron of the same ensemble with input patterns that represent different sub-data-sets of the original training data set. This has indeed already been demonstrated with pure CMOS based architectures of the type proposed in this paper, by using different random connectivity patterns for each weak classifier of the ensemble.

The boosting approach, promises to yield even better results. However the constraints on choosing which weights to change might lead to the adoption of extra control modules per neuron that require too large or complex overhead circuits and could result to be prohibitive for realistic compact chip designs.

5.3 Cross-bars versus addressable arrays

The nano-scale footprint of memristors is an important feature which can enable ultra dense memory capacity. To exploit this extremely low footprint to its full extent, dense cross-bar arrays have been reportedly implemented and proposed as
in-memory computing neural network engines. However, although the development of dense cross-bars is extremely important for the scaling of technology, there are many challenges associated with their use in neuromorphic architectures both from fabrication and circuits point of view. For example, it is not clear how much passive cross-bar arrays can be scaled up to larger sizes, due to sneak path and cross-talk issues. Even in the case of cross-bar arrays with active elements such as 1T-1R (one-transistor and one-memristor) or memristive devices with embedded “selectors” used to avoid the sneak-path problem, issues such as the line resistance, reproducibility, and overhead size of external encoder and decoder CMOS circuits are yet to be satisfactorily addressed. Alternatively, one can decide to forgo the cross-bar approach of very high density arrangements of basic 1R or 1T-1R elements, and design addressable arrays of more complex synapses that comprise multiple transistors and multiple memristive devices per synapse, to try and capitalize on the many other useful features of memristive devices (in addition to their compact size), such as non-volatility, state-dependence, complex physics that can be exploited to emulate the complex molecular properties of biological synapses, complex dynamics, and stochastic switching behavior. The architecture we propose represents an intermediate approach that comprises two memristive devices per synapse and two select switches. This design was proposed to allow maximum flexibility in exploring the properties of different types of memristive memory devices, but it could be made even more dense by replacing the transistors currently used to switch between read-mode and write-mode with embedded selectors and modulating the amplitude of the Vdrive line of Fig. 3 to operate the device only in read-mode or in both read- and write-mode, thanks to the fact that the voltage set at the terminals of the memristive devices is a ramp that can cover both ranges of operation. However, while large-scale in-memory computing cross-bar arrays of this type may solve the memory-bottleneck problem, they would still be crippled by an Input/Output (I/O) bottleneck problem due to the constraint that while one synapse is being operated in its write-mode (which could last micro-seconds), no other synapse of the same row could be stimulated. By incorporating the PS and NC blocks of Fig. 1 in the MS blocks, this addressable array architecture would definitely lose the benefit of high-density synapses, but would dramatically increase the bandwidth of its input Address-Events (e.g., with each I/O operation lasting nanoseconds), as each synapse element would become independent from the others and multiple synapses would be able to safely operate in read- or write-mode in parallel. Once the choice is made to forgo the density benefit, adding further transistors for example to implement local non-linear dynamics, such as short-term plasticity, homeostatic synaptic scaling mechanisms, or more complex learning mechanisms to improve the performance of the overall neuromorphic computing system would become easily realizable.

6 Conclusions

We presented an effort to design and combine a suite of computational techniques for constructing a trainable neuromorphic platform that supports the use of a wide variety of memristive devices. We showed that variability of the memristive devices and mismatch in CMOS circuits can be on one hand reduced by circuit techniques, and can on the other hand be exploited as a feature for training and computation. We described the architecture of a neuromorphic platform that can implement stochastic training exploiting the switching properties of memristive devices and validated the approach with system-level behavioral simulations for a linear classification task, using the MNIST data-set.

The proposed neuromorphic computing architecture supports continuous-time always-on on-chip learning, and continuously streams output spikes to the AER output blocks. By routing output address-events via either off-chip or on-chip asynchronous AER routing schemes and circuits, these architectures support scaling by tiling them either across multiple chips, or on multiple cores within a multi-core device. Examples of multi-core neuromorphic computing systems based on the AER protocol have been recently proposed, however none have been implemented so far using memristive devices, and exploiting their intrinsic properties to implement probabilistic learning.

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