Large-scale and High-speed Privacy Amplification for FPGA-based Quantum Key Distribution
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Abstract—The FPGA-based Quantum key distribution (QKD) system is an important trend of QKD systems. It has several advantages, real time, low power consumption and high integration density. Privacy amplification is an essential part in a QKD system to ensure the security of QKD. Existing FPGA-based privacy amplification schemes have an disadvantage, that the throughput and the input size of these schemes (the best scheme 116Mbps@10^6) are much lower than these on other platforms (the best scheme 1Gbps@10^8). This paper designs a new PA scheme for FPGA-based QKD with multilinear modular hash-modular arithmetic hash (MMH-MH) PA and number theoretical transform (NTT) algorithm. The new PA scheme, named large-scale and high-speed (LSHS) PA scheme, designs a multiplication-reusable architecture and three key units to improve the performance. This scheme improves the input size and throughput of PA by above an order of magnitude. The throughput and input size of this scheme (1Gbps@10^8) is at a comparable level with these on other platforms.

Index Terms—Quantum Key Distribution, Privacy amplification, FPGA, Multilinear Modular Hash, Number Theoretical Transform.

I. INTRODUCTION

Quantum key distribution (QKD) is a notable technique which exploits the principle of quantum mechanics to perform the information theoretical security key distribution between two remote parties, named Alice and Bob [1]. A QKD system can be divided into two parts, the quantum optical subsystem and the postprocessing subsystem. The quantum optical subsystem is for the preparation, transmission and measurement of quantum states. The postprocessing subsystem is to complete the correctness and security of the final secure key [2]. A Field-Programmable-Gate-Array (FPGA) based QKD system means that the control part of its quantum optical subsystem and its postprocessing subsystem is implemented by a FPGA [3], [4]. The advantages of a FPGA-based QKD system are real time, low power consumption, high integration density. A FPGA-based QKD system can be combined with the integrated optical circuit to implement the QKD system on chip, which will provide improved performance, miniaturization and enhanced functionality of the QKD system[5].

Privacy amplification is a necessary part in quantum key distribution [6]. It is the art of distilling a highly secure key from a partially secure string by public discussion between two parties. It is one of the main bottlenecks of the FPGA-based QKD system.

The lacking input block size is the most critical problem of PA for a FPGA-based QKD system. The input block size of PA has significant impact on the final key rate of QKD system [7], [8]. The largest input block size of existing FPGA-based PA schemes is 10^6 [9], while the common input block size of PA schemes on other platforms is more than 10^8 [10], [11].

The constricted computing resource of FPGA is the main reason of lacking the input block size of FPGA based PA.

To realize large input block size with the constricted computing resource, a few schemes have been proposed on other platforms such as the length-compatible PA on the GPU [11], the HiLS PA on the CPU [10] and the MMH-MH PA on the CPU. The length-compatible PA and the HiLS PA are both based on Toeplitz-hash PA algorithm. They take the advantage of Toeplitz-hash to improve input block size by dividing the long input sequence into short block. It is convenient to design a similar scheme on FPGA according to these schemes, because there are already two methods to implement Toeplitz-hash PA on FPGA, which are block parallel method and FFT-based method. However, we do not regard these Toeplitz-based methods as the most suitable method to design a large input block size PA scheme on FPGA. The unsuitability of the block parallel method is that it is hard to overcome the lack of real-time, because its computation complexity is as high as O(n^2). The unsuitability of the FFT-based method is that it relies on the floating-point arithmetic, which may bring the calculation error and impact on security of key. Floating-point arithmetic also increases the memory consumption and requires external storage, which affects the integration level of the system.

The Multilinear Modular Hash - Modular Arithmetic Hash (MMH-MH) PA is a new PA algorithm that can realize large input block size PA with the constricted computing resource [12]. It can be implemented by number theory transform (NTT) and provides strong real-time with the O(n log n) computation complexity. NTT uses integer arithmetic instead of floating-point arithmetic, which avoids the calculation error and external storage. Therefore, a large scale PA scheme based on the MMH-MH PA algorithm is designed in this paper to improve the performance of the FPGA-based QKD system.

The principle and security analysis of MMH-MH PA Algorithm is introduced as a basis for this work in section 2. The multiplication of large numbers is the major part in both multilinear modular hash and modular arithmetic hash. Therefore, a multiplication-reusable structure and its control unit for the MMH-MH PA is designed. Subsequently, the optimization method of the PA input size according to the compression ratio is introduced. The design of three key units in this scheme is introduced: 1. the NTT-based multiplication unit, which
MMH family is an universal hashing family \[ \text{[13]} \], its collision probability \( \delta = 1/|Z_p| \), and the proof can be found in \[ \text{[14]} \].

b) Definition of Modular Arithmetic Hashing: Let \( \alpha \) and \( \beta \) be two strictly positive integers, \( \alpha > \beta \). Define a family modular arithmetic hashing of functions from \( 2^n \) to \( 2^\beta \) as follows:

\[
MH := \{ h_{b,c} : Z_{2^n} \to Z_{2^\beta} | b, c \in Z_{2^n}, \gcd(b, 2) = 1 \} \tag{3}
\]

where the function \( h_{b,c} \) is defined as follows:

\[
h_{b,c}(x) := (b \cdot x + c \mod 2^n) / 2^{n-\beta} \tag{4}
\]

Modular Arithmetic Hashing can be designed for PA algorithm itself, while it can not split the input and handle it separately, the output set of modular arithmetic hashing is variable length bit sequence. So it can be combined with MMH to design a new PA algorithm.

The specific process of the MMH-MH PA algorithm is given as Algorithm 1. In details, the prime number \( p \) is suggested to be a Mersenne prime. The form of a Mersenne prime is \( M_\gamma = 2^\gamma - 1 \). The length of input sequence is \( n = \gamma \times k \). \( x_i = 2^\gamma - 1 \) is a special case, the data \( x_i = 2^\gamma - 1 \) should be cast away and reload.

### Algorithm 1 MMH-MH PA algorithm

**Input**: Input Data: \( x \in Z_{2k \times \gamma} \). Random numbers: \( a \in Z_p^k, b, c \in Z_{2^\gamma}, \gcd(b, 2) = 1 \).

**Output**: \( z \in Z_{2^\gamma} \). Split data \( x \)

1: \( x = \langle x_1, \cdots, x_k \rangle \) //split data \( x \)
2: \( a = \langle a_1, \cdots, a_k \rangle \) //split data \( a \)
3: if \( x_i = 2^\gamma - 1 (i = 1, \cdots, k) \) then
5: else
6: for \( i = 0 \) to \( k \) do
7: \( y_i = a_i \times x_i \)
8: end for
9: \( y = \sum_{i=1}^{k} y_i \mod p \) //MMH function: \( y = g_a(x)^*/ \)
10: \( z = (b \cdot y + c \mod 2^n) / 2^{n-\beta} \) //MMH function: \( z = h_{b,c}(y)^*/ \)
11: end if

Because the process of MMH-MH PA is different from that of traditional PA algorithms, we have proven that the security
of MMH-MH PA is similar with other PA algorithms in [12]. MMH-MH PA algorithm requires an additional condition to guarantee the security, that is the length of final key \( r \) should be much less than \( \gamma \), specifically \( r < \gamma - s \) (\( s \) is the information theory security parameter of QKD).

III. LARGE-SCALE AND HIGH SPEED PA SCHEME ON FPGA

A large-scale and high-speed PA scheme on the FPGA is designed based on MMH-MH PA algorithm in this section. It can be found that the major part of MMH-MH PA algorithm is the large-number multiplication according to Section 2. It is the core operation of both MMH function and MH function. Therefore, we designed a multiplication-reusable structure and its control unit for the scheme, and we introduced the calculation method of key parameters in this scheme. Afterwards, the design method of main units is illustrated. The most important unit is the large-number multiplication unit. It deeply determines the performance of the whole scheme. A 768Kb multiplication unit is designed based on number theoretic transform (NTT). In addition, it can optimize computation resource cost according to the real-time requirement by adjusting the radix of NTT. Then we designed a low-cost modular accumulation unit and a pipelined binary modular addition unit to improve overall performance.

A. Architecture of large-scale PA scheme

The architecture of large-scale PA scheme is indicated as Fig. 2. The multiplication unit is reused in this architecture to reduce the resource cost. There are two streams of data flow in this scheme, and they represent the MMH function data stream and MH function data stream.

A matched control unit is designed to control computational process and data flow as indicated as Fig. 3. The MMH function calculation begins first when the multiplication unit is ready. Because MMH function needs \( k \) times multiplication, the state will turn to "MMH cnt" and a counter up one when one multiplication operation completes. The state will return to "MMH" if \( cnt < k \) and go to "MH" if \( cnt = k \). "MH" state will calculate MH function and output the final key, and the state will go back to initial state until the end of the output.

The control unit will make data flow follow the blue arrow at the state "MMH" and the red arrow at the state "MH".

B. Key parameter calculation of large-scale PA scheme

The sub-block size \( \gamma \) and the sub-block number \( k \) are the most critical parameter in this scheme. Because the input block size \( n = \gamma \times k \) is the main optimization target, \( \gamma \) and \( k \) are expected to be as larger as possible. \( \gamma \) is restricted by two conditions: 1. \( 2^r - 1 \) should be a primer; 2. \( 2^r - 1 \) should be less than the largest number \( N_{mul} \) supported by the large-number multiplication unit. The \( N_{mul} \) of multiplication unit in FPGA as we know is the module in [15], and its \( N_{mul} = 2^{1179648} - 1 \). Therefore, the largest \( \gamma \) can be chosen as 756839 (\( 2^{756839} - 1 \) is the 32nd Mersenne prime). The largest number multiplication unit on FPGA can be chosen as 2786432 – 1, so the sub-block size \( \gamma \) can be chosen as 756839 (\( 2^{756839} - 1 \) is the 33rd Mersenne prime). The sub-block number \( k \) is restricted by the compression ratio \( R_{PA} \) of PA (The calculation method of \( r \) can be referred in [12]), and 1/k should be larger than \( R_{PA} \). The compression ratio \( R_{PA} \) is affected by the specific QKD system and transmission distance, so the specific value of \( k \) will be discussed in next section.

Then we elaborate the design of three main modules of this scheme: 1. the large-number multiplication unit; 2. the low-cost modular accumulation unit 3. the pipelined binary modular addition unit.

C. Design of large-number multiplication unit

The large number multiplication unit is the most essential and complex unit in this scheme. The size of this large number multiplication unit is 786432 bits. It is implemented based on number theoretical transform (NTT) algorithm. The large number multiplication algorithm (\( Z = X \times Y \)) can be summarized as follow:

1) Break the large numbers \( X \) and \( Y \) into a sequence of words \( x(n) \) and \( y(n) \) using base \( B: X = \sum x_{i} \times B^{i} \) and \( Y = \sum y_{i} \times B^{i} \).
2) Compute the dot product of NTT results \( NTT(X) \) and \( NTT(Y) \): \( Z''_{i} = NTT(X)_{i} \times NTT(Y)_{i} \).
3) Compute the inverse NTT (INTT): \( Z'' = INTT(Z'') \).
4) Resolve the carries: let \( Z_{i+1} = Z''_{i+1} + Z''_{i} / B \), and \( Z_{i} = Z_{i+1} % B \).

The base \( B = 24 \) and the sequence size \( n = 32768 \), so the size of this large number multiplication is \( n \times B = 786432 \).
NTT and INTT are the main parts in this algorithm, and a 65536-point NTT and 65536-point INTT are required. An N-point NTT is defined as:

\[ X_k = \sum_{n=0}^{N-1} x_n(W_N)^{nk} \mod p. \]

And an N-point INTT is defined as:

\[ x_k = N^{-1} \sum_{n=0}^{N-1} X_n(W_N)^{-nk} \mod p. \]

To simplify the modulo operation, \( p \) is chosen as a special primer, which is \( p = 2^{64} - 2^{32} + 1 \). One data point in NTT \( NTT(X)_i \) is represented as a 64-bits digit. So the largest data point is \( NTT(X)_i \times NTT(Y)_i \), which is a 128-bits digit and represented as \( 2^{96}a + 2^{64}b + 2^{32}c + d \). It can be rewrite as,

\[
\begin{align*}
2^{96}a + 2^{64}b + 2^{32}c + d & \equiv -1(a) + (2^{32} - 1)b + (2^{32})c + d \\
& \equiv (2^{32})b + c - a - b + d
\end{align*}
\]

The computation complexity of directly computing NTT is too excessive, so the butterfly algorithm is required to reduce it. The radix is an important parameter of butterfly algorithm. Larger radix will decrease the run time of algorithm and cost more computational resource. The radix-\( r \) butterfly algorithm will be introduced next.

1) Radix-\( r \) butterfly algorithm: We take 16-point NTT as an example to demonstrate the difference between radix-2, radix-4, radix-16 butterfly algorithm. The computation of radix-16 is indicated as follow,

\[ X_k = \sum_{n=0}^{15} x_n(W_{16})^{nk} \mod p. \]

Obviously, the radix-16 algorithm only needs to run once to complete the 16-point NTT. The computation of radix-4 is indicated as follow,

\[ X_k = \sum_{n=0}^{3} x_n(W_{4})^{nk} \mod p \]

The 16-point NTT can be divided into twice radix-4 calculation, the specific process is shown below,

\[ X_k = \sum_{n=0}^{16} x_n(W_{16})^{nk} \mod p = \sum_{n=0}^{3} (W_{4})^{n k_2} \left\{ \sum_{n=1}^{3} x_n(W_{4})^{n k_1} \right\} (W_{16})^{n k_1} \mod p \]

where \( n = 4n_0 + n_1 \) and \( k = 4k_0 + k_1 \). In the same way, the 16-point NTT can be divided into quartic radix-2 calculation.

2) structure of large-number multiplication unit: The structure of large-number multiplication unit is indicated as Fig. 5. The NTT processor used a radix-16 unit and matched memory to complete a \( 16^3 = 65536 \)-point NTT/INTT calculation. The calculation requires four stage to complete. The memory unit is divided into 16 banks to load 16-point data in one time. The data in memory should be stored by a well-designed address mapping table. Details of the well-designed address mapping table can be referred in [16].

The data is load into memory before the NTT calculation. In each stage of NTT, the data is access and transmit into the radix-16 unit. Then it is send to a 64-bit multiplication unit, and the multiplicant will be constant ‘1’. rotation factor \( W_N^1 \), INTT factor \( N^{-1} \) and the NTT results of NTT_B. The 65536th primitive root \( W_{65536} \) of \( p = 2^{64} - 2^{32} + 1 \) is 0x3365469864f124. After NTT and INTT calculation are completed, the data is load into the carry option module to guarantee each point of multiplication results is 24bits. More details of large-number multiplication unit can be found in [16].

D. Design of low-cost modular accumulation unit

The low-cost modular accumulation unit is responsible for modular accumulate calculation in MMH function \( y = \sum_{i=1}^{k} y_i \mod p \), where \( y_i \) is the multiplication result of large-
number multiplication unit and \( p = 2^{756839} - 1 \). The modular addition can be simplified as follow,

\[
\begin{align*}
    a + b \mod (2^{756839} - 1) &= a \mod 2^{756839} + \left\lfloor a/2^{756839} \right\rfloor \\
    &\quad + b \mod 2^{756839} + \left\lfloor b/2^{756839} \right\rfloor 
\end{align*}
\]

In this way, the modular calculation is replaced by addition and bit operation. It only needs full adders and 756839 bits memory. The structure is illustrated as Fig. 6. In this structure, the input data just adds the data in accumulation result memory with period 756839 and clears memory when once MMH function completes.

### E. Design of pipelined binary modular addition unit

The pipelined binary modular addition unit is designed to calculate the equation \( z = (b \cdot y + c) \mod 2^n \). The structure of pipelined binary modular addition unit is indicated as Fig. 7. \( b \cdot y \) has been prepared by multiplication unit and is the input. Adder and carry operation module calculate \( b \cdot y + c \). The binary modular and division is implemented by the data counter and switch module. The parameter \( \alpha \) is equal to \( \gamma \) and \( \beta \) is equal to the length of secure key. Each frame of data is 24 bits, so the module begins to output data when the input data count is \( \left\lfloor \alpha/24 \right\rfloor \). The first frame of data outputs \( \alpha/24 \) 24 bits data. The data count of data inputs \( 24 \times \beta \mod 2^{756839} \) 24 bits data. The rest of frames are 24bits each frame. The output ends when the data count is \( \left\lfloor \alpha/24 \right\rfloor \). This unit use data counter instead of calculation module implementing pipelining and low cost.

### IV. IMPLEMENTATION AND EXPERIMENT

The proposed large-scale and high-speed (LSHS) PA scheme is implemented on the Xilinx ZYNQ UltraScale+ evaluate kit. This kit is based on a Zynq Ultrascale+ XCZU9EG-2FFVB1156 FPGA. The resource utilization is an important indicator to estimate the practicability of a FPGA-based PA scheme, and it is influenced by \( \gamma \) and \( \text{radix} \) in our scheme.

| Resource Scheme Used | Available | Utilization Rate |
|----------------------|-----------|------------------|
| Luts                 | 156707    | 230400           | 68% |
| BRAMs                | 198       | 408              | 48% |
| DSP Slices           | 512       | 1728             | 30% |

\(^1\) Available: Zynq Ultrascale+ XCZU9EG-2FFVB1156 available
\(^2\) \( \gamma = 756839 \) and \( \text{radix} = 16 \)

The resource utilization of our scheme with \( \gamma = 756839 \) and \( \text{radix} = 16 \) is indicated as Table I. This scheme is evaluated in three aspects: 1. The input block size of the LSHS PA scheme is evaluated and the secure key rate improvement of a FPGA-based QKD system with LSHS PA scheme is demonstrated; 2. The throughput of the LSHS PA scheme on different block size is evaluated and compared with existing PA schemes; 3. The resource cost and core index of the LSHS PA scheme are compared with existing FPGA-based PA schemes.

#### A. The input block size and secure key rate of the LSHS PA scheme

The input block size \( N \) of the LSHS PA scheme is equal to \( k \times \gamma \). \( \gamma \) is a fixed value and \( k \) is related to the maximum compression ratio \( R_{P_A}^{\text{MAX}} \) of PA. Therefore, the input block size \( N \) is related to the maximum compression ratio \( R_{P_A}^{\text{MAX}} \) of PA. \( R_{P_A} \) can be calculated on the basis of QKD system parameters. The compression ratio of a DV-QKD system can be calculated by \( R_{P_A} = \beta I_{AB} - I_{AE}(e_1 + \Delta n) \). The compression ratio of a CV-QKD system can be calculated by \( R_{P_A} = \beta I_{AB} - \chi_{BE} - \Delta n \). The main fluctuate factor of compression ratio is the channel error rate \( e \). The maximum compression ratio \( R_{P_A}^{\text{MAX}} \) means the compression ratio \( R_{P_A} \) when the channel error rate \( e \) is minimum. The parameter \( k \) is required to be smaller than \( 1/R_{P_A}^{\text{MAX}} \) to maximum the secure key rate.

![Fig. 6. Structure of low-cost modular accumulation unit.](image)

![Fig. 7. Structure of pipelined binary modular addition unit.](image)
FPGA-based PA schemes as we know. It can be found that the effect of the LSHS PA scheme is more significant in the CV-QKD system. This is because the finite size effect in the CV-QKD system is more serious than that in the DV-QKD system.

In conclusion, the simulation results indicate that the LSHS PA scheme can improve the input block size and the secure key rate of a QKD system. This improvement is more efficient in a CV-QKD system.

B. The throughput of the LSHS PA scheme

The throughput of PA means the maximum rate of the input key into a PA scheme. It is an important index of PA, which affects real-time of a QKD system. We experimented the throughput of the LSHS PA scheme at different input block sizes with a random simulated data source. Then, we compared the throughput between our scheme and existing schemes as indicated in Fig. 9 [9], [11], [17], [19].

The comparison shows that our scheme improves the throughput by an order of magnitude than existing FPGA-based PA schemes, and our scheme reaches a equal throughput with the existing best throughput PA scheme – a GPU-based PA scheme. The throughput advantage of the LSHS PA scheme profits from two reasons: 1. the less computation of MMH-MH PA algorithm; 2. the three efficient units we design in section 3.

C. The resource cost and core index comparison of FPGA-based PA schemes

We compared the resource cost and core index between LSHS PA scheme and existing FPGA-based PA schemes. The resource cost of a FPGA-based PA scheme includes look up tables (LUTs), internal Random Access Memory (RAM), external RAM and DSP slices. The core index to be compared is throughput and input block size of a PA scheme. The comparison results are indicated as Table II.

The LSHS PA scheme costs the most LUT and Internal-RAM among existing PA schemes. The main cost of LSHS PA is the large-number multiplication unit. It costs nearly 90% of LSHS PA scheme. The main reason of its high cost is that it chooses the radix of the unit as 16. This provides the best real-time and throughput, but also costs the most resource. If a large-number multiplication unit with $\text{radix} = 2$ is used in this scheme, we estimated that the throughput and the LUTs cost will be reduced to approximately eighth of their previous. The internal-RAM cost of the LSHS scheme is the most, because it uses the NTT algorithm for acceleration, and the NTT algorithm needs to store all the input data and rotation factors. Similarly, the scheme in [9] used the FFT algorithm for acceleration. The NTT algorithm has an advantage over FFT algorithm, that the data format of the NTT is the integer instead of the floating-point of the FFT. This advantage significantly reduces the memory cost of the LSHS scheme compared with the scheme in [9], and frees the LSHS PA scheme from dependence on the external-RAM.
Although the LSHS PA scheme costs more resources, the LSHS PA scheme greatly improves the core index of FPGA-based PA scheme. Before the LSHS PA scheme, the throughput and input block size of the FPGA-based PA scheme is far below that of PA schemes based on other platforms. Therefore, although FPGA-based PA schemes have advantages of low power consumption and high integration level for QKD systems, they are not applied widely due to the low core index. The core index of the LSHS PA scheme has exceeded existing FPGA-based PA schemes by several orders of magnitude, and it has surpassed the best PA scheme in terms of these core indexes.

V. CONCLUSION

In this research, a large scale and high speed PA scheme based on FPGA is proposed to improve the core index (input block size and throughput) of a FPGA-based PA scheme. This scheme is designed based on the MMH-MH PA algorithm. We designed the architecture of the LSHS PA scheme to reuse as many computation unit as possible for the resource cost reduction. Then we focused on the design of three key units of this scheme in this paper. A 786432-bits large-number multiplication unit is designed based on the NTT algorithm. A low-cost modular accumulation unit is designed to compute \( \text{mod } 2^{756839} - 1 \) accumulation with minimal memory. A pipelined binary modular addition is designed to compute the binary modular of arbitrarily length without memory. We implemented the proposed large-scale and high-speed PA scheme on the Xilinx ZYNQ ultrascale+ evaluate kit. We referenced the parameters of a typical DV-QKD system and a typical CV-QKD system to evaluate the input block size, the throughput and the influence on the final key rate of the LSHS PA scheme. We compared these results with existing PA schemes on FPGA and other platforms. The results indicate that the LSHS PA scheme has improved the throughput by an order of magnitude, and it can improve the input block size by several magnitudes compared with existing FPGA-based PA schemes. The input block size improvement is more obvious in a CV-QKD system and a long transmission distance QKD system. The above results indicate that the LSHS PA scheme can significantly improve the final key rate of a FPGA-based QKD system. It is worth noting that the core index of the LSHS PA scheme has exceeded the existing best PA scheme of all platforms. Adding the consideration with the power consumption and integration level advantages of the FPGA-based PA schemes, the LSHS PA scheme is a highly competitive solution for the QKD systems.

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