Efficient Evaluation of Exponential and Gaussian Functions on a Quantum Computer

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The exponential and Gaussian functions are among the most fundamental and important operations, appearing ubiquitously throughout all areas of science, engineering, and mathematics. Whereas formally, it is well-known that any function may in principle be realized on a quantum computer, in practice present-day algorithms tend to be very expensive. In this work, we present quantum algorithms designed specifically for evaluating exponential and Gaussian functions efficiently on quantum computers.

The implementations require a (generally) small number of multiplications, which represent the overall computational bottleneck. For a specific, realistic NISQ application, the Toffoli count of the exponential function is found to be reduced from 15,090 down to 912, when compared against a state-of-the-art competing method by Häner and coworkers [arXiv:1805.12445], under the most favorable conditions for each method. For the corresponding Gaussian function comparison, the Toffoli count is reduced from 19,090 down to 704. Space requirements are also quite modest, to the extent that the aforementioned NISQ application can be implemented with as few as ~70 logical qubits. More generally, the methods presented here could also be equally well applied in a fault-tolerant context, using error-corrected multiplications, etc.

I. INTRODUCTION

The exponential and Gaussian functions are among the most fundamental and important operations, appearing ubiquitously throughout all areas of science, engineering, and mathematics. Whereas formally, it is well-known that any function, $f(x)$, may in principle be realized on a quantum computer [1–9], in practice present-day algorithms tend to be very expensive.

Part of the reason for the “significant expense” is the cost of the requisite quantum multiplications [1–9, 10], each of which—at least for the most commonly used “schoolbook” algorithms [8, 9, 12–14]—requires a sequence of $n$ controlled additions [10, 13, 17–19]. Here, $n$ is the number of bits needed to represent the summands using fixed-point arithmetic (which is presumed throughout this work). Each controlled addition introduces $O(n)$ gate complexity—implying an overall quantum multiplication gate complexity that scales as $O(n^2)$. Although alternative multiplication algorithms with asymptotic scaling as low as $O(n \log_3 n)$ do exist [13–16], they do not become competitive until $n$ reaches a few thousand. This is far beyond the values needed for most practical applications (e.g., those of this work, for which $n = 21$–32).

For practical applications, then, there appear to be two strategies that might be relied upon to significantly improve performance. The first is to wait for better quantum multiplication algorithms to be devised; this is, after all, an area of active and ongoing development, more so than general function evaluation on quantum computers. The second is to design entirely new algorithms, customized for specific $f(x)$ functions.

The present work is of the latter variety. In particular, we present quantum algorithms designed specifically to evaluate exponential and Gaussian functions efficiently on quantum computers. These algorithms require a (generally) small number of multiplications, which represent the overall computational bottleneck. Our general approach is thus equally applicable to noisy intermediate-scale quantum (NISQ) calculations [6, 20] with non-error-corrected quantum multiplications, as it is in a fault-tolerant context, using error-corrected multiplications, etc. In all such contexts, we advocate for using the “total multiplication count” as the appropriate gate complexity metric—although the “Toffoli count” metric, which is currently quite popular, will also be used in this paper.

While these methods allow to reduce the Toffoli [gate] and qubit counts significantly, the resulting circuits are still quite expensive, especially in terms of the number of gates that are required.

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It will be shown that the gate complexity for the present approach is dramatically reduced, when compared with the state-of-the-art competing method by Häner et al. For a specific, realistic NISQ application, the Toffoli count of the exponential function is reduced from 15,690 down to 912, under the most favorable conditions for each method. For the corresponding Gaussian function comparison, the Toffoli count is reduced from 19,090 down to 704. Space requirements are also generally reduced, and in any event quite modest—to the extent that in one case, the above NISQ application can be implemented with as few as \( \sim 70 \) logical qubits.

Although the range of applications where exponential and Gaussian functions are relevant is virtually limitless, one particular application area will be singled out for further discussion. Quantum computational chemistry (QCC) \([1, 2, 3, 5, 7, 21–46]\)—i.e., quantum chemistry simulations \([47–50]\)—run on quantum computers—has long been regarded as one of the first important scientific applications where quantum supremacy will likely be realized \([26, 31, 33, 36]\). Particularly for “first-quantized” or coordinate-grid-based QCC \([1–3, 5, 7, 21–46]\), it becomes necessary to evaluate functions over a (generally) uniformly-distributed set of distinct grid points \([26, 30, 35, 36, 38, 45, 46]\)—exactly of the sort that emerges in fixed-point arithmetic, as used here.

Of course, the most natural function to arise in the QCC context is the inverse-square-root function, \( f(x) = x^{-1/2} \), representing Coulombic interactions \([47–50]\). Even for a “general function evaluator” code, this specific case poses some special challenges—associated, e.g., with the singularity at \( x = 0 \)—that result in substantially increased computational expense. On the other hand, the alternative Cartesian-component separated (CCS) approach, as developed recently by the author and coworkers \([37, 61]\), replaces the inverse square root with a small set of Gaussians. Using the new exponential/Gaussian evaluator of this work, then, the CCS approach would appear to become a highly competitive contender for first-quantized QCC.

The remainder of this paper is organized as follows. Mathematical preliminaries are presented in Sec. \( \text{IIA} \) followed by an exposition of our basic quantum exponential algorithm in Sec. \( \text{IIB} \) and its asymptotic scaling in Sec. \( \text{IIC} \). These are the core results, especially for long-term quantum computing. Secs. \( \text{III} \) and \( \text{IV} \) then give a detailed explanation of various algorithmic improvements leading to reduced gate and space complexity, that will be of particular interest for NISQ computing. In particular, quantum circuits for two specific NISQ implementations are presented in Sec. \( \text{IVB} \) one designed to minimize gate complexity (Sec. \( \text{IVC} \)), and the other, space complexity (Sec. \( \text{IVC} \)). Using the specific “gate saving” and “space saving” implementations of Sec. \( \text{IV} \) a detailed numerical comparison with Ref. \([8]\) is provided in Sec. \( \text{V} \). Finally, concluding remarks are presented in Sec. \( \text{VI} \).

### II. BASIC METHOD

#### A. Mathematical preliminaries

Consider the exponential function,

\[
 f(x') = \exp(-\alpha x').
\]

We wish to evaluate the function over the domain interval, \( x'_{\min} < x' < x'_{\max} \). Note that \( x' \) and \( \alpha \) are presumed to be real-valued. If \( \alpha \) were pure imaginary, then Eq. (1) would be unitary—i.e., the most well-studied special case in quantum computing \([3]\). But this is not the case here. Without loss of generality, we may restrict consideration to \( \alpha > 0 \). The negative \( \alpha \) case corresponds to the above, but with \( x' \to -x' \), \( x'_{\min} \to -x'_{\max} \), and \( x'_{\max} \to -x'_{\min} \).

Both the domain and the range of Eq. (1) are represented discretely, using a finite number of qubits. For generality, we allow the number of domain qubits, \( d \), to differ from the number of range qubits, \( n \). In the first-quantized QCC context, for instance, the \( d \ll n \) case arises very naturally (where ‘\( \ll \)’ represents perhaps a factor of 3 or 4). More specifically, something like 100 grid points are needed to accurately represent each domain degree of freedom—although the function values themselves require a precision of say, 6–10 digits. Throughout this paper, we mainly focus on the \( d \ll n \) case—although the \( d = n \) special case is obviously also important, and will also be considered.

The \( d \) qubits used to represent the domain correspond to \( 2^d \) distinct grid points, distributed uniformly across the \( x' \) interval, with grid spacing \( \Delta = 2^{-d}(x'_{\max} - x'_{\min}) \). Such representations are typical in quantum arithmetic, and imply fixed-point rather than floating-point implementations \([8, 9]\). Indeed, since fixed-point arithmetic is closely related to integer arithmetic, we find it convenient to transform \( x' \) to the unitless domain variable,

\[
 x = \frac{(x' - x'_{\min})}{\Delta},
\]

such that the \( x \) grid points become integers, \( x = \{0, 1, \ldots, 2^d - 1\} \). In terms of \( x \), the function then becomes

\[
 f(x) = \exp[-\alpha(x'_{\min} + \Delta x)] = CA^x, \quad \text{where } C = \exp(-\alpha x'_{\min}), \text{ and } A = \exp(-\alpha \Delta).
\]

Next, we define the following binary decomposition of the \( x \) integers, in terms of the \( d \) individual qubits, \( x_i \), with \( 0 \leq i < d \) and \( x_i = \{0, 1\} \):

\[
 x = \sum_{i=0}^{d-1} x_i 2^i
\]

Note that increasing \( i \) corresponds to larger powers of 2; thus, the binary expansion of the integer \( x \) would be \( x_{d-1} \cdots x_1 x_0 \). Put another way, the lowest index values
correspond to the rightmost, or least significant, digits in the binary expansion. This convention shall be adopted throughout this work.

Substituting Eq. (5) into Eq. (3), we obtain

\[ f(x) = C \left( A^{2^0} \right)^{x_0} \left( A^{2^1} \right)^{x_1} \cdots \left( A^{2^{d-1}} \right)^{x_{d-1}} \]

\[ = CA_0^{x_0} A_1^{x_1} \cdots A_{d-1}^{x_{d-1}}. \quad \text{where} \quad (6) \]

\[ A_i = A^{2^i} \quad \text{(7)} \]

In this manner, exponentiation is replaced with a sequence of \( d \) multiplications. Note from Eq. (7) that \( A_0 = A \). As additional notation, we find it convenient to introduce the quantities \( C_{0 \leq i < d} \), through the recursion relation \( C_{i+1} = C_i A_i^{x_i} \), with \( C_0 = C \). Thus, \( C_d = f(x) \), and the other \( C_{i < d} \) quantities represent partial products in Eq. (6).

**B. Basic quantum algorithm**

The exponent of every \( A_i \) value in Eq. (6), being the qubit \( x_i \), is associated with the two states or values, 0 and 1. From a quantum computing perspective, therefore, this situation can be interpreted as an *instruction*:

- If \( x_i = 1 \), then multiply by \( A_i \).
- Otherwise, i.e. if \( x_i = 0 \), do nothing.

This suggests a simple and straightforward quantum algorithm for exponentiation, consisting of nothing but a sequence of \( d \) *controlled multiplications*, as indicated in Fig. 1.

From the figure, each of the \( d \) qubits, \( x_i \), serves as the control qubit for a separate target multiplication of \( C_i \) by \( A_i \), in order to generate the next \( C_{i+1} \). In this basic implementation, each of the \( d \) constants, \( A_i \), is stored by a separate bundle of \( n \) qubits, initialized prior to the calculation. An additional bundle of \( n \) qubits (lowest wire in Fig. 1) is used to represent the value of the function. This output register is initially assigned the constant value \( C \), but through successive controlled multiplications with \( A_i \) as described above, ends up taking on the final output value, \( C_d = f(x) = \exp(-\alpha x^2) \).

For the moment, we primarily treat multiplication as an oracle or “black box” routine, whose operational details need not concern us. However, we note from the above description (and from Fig 1) that one of the two input registers gets overwritten with the product value as output, and the other is unaffected. There are indeed some multiplication algorithms—e.g., those based on the Quantum Fourier Transform (QFT) [8] [9] [10] [11] [25] [62] —that behave in this manner. We call these “overwriting” multiplication routines. Other standard multiplication algorithms—e.g., those based on bit-shifted controlled additions [8] [9] [12] —do not have this property. This issue is revisited again in Sec. [V].

As discussed, the \( C_i \) values are stored in the \( n \)-qubit output register, whereas the \( A_i \) are stored in \( d \) separate \( n \)-qubit input registers. Since \( 0 < A_i < 1 \) for all \( A_i \), it is convenient to represent these constants using the following \( n \)-bit binary expansion:

\[ y = \sum_{j=0}^{n-1} y_j 2^{-(n-j)} \quad \text{(8)} \]

Thus, the binary expansion of \( y \) becomes \( y = y_0 y_{n-1} \cdots y_1 y_0 \)—with the \( y_0 \) bit least significant, as discussed. This representation has a resolution of \( 2^{-n} \). Likewise, \( 0 < C_i \leq 1 \) for all \( 0 \leq i \leq d \), provided \( x'_\text{min} \geq 0 \) (if not, there are simple remedies that can be applied, although these are not needed here). We therefore find it convenient to adopt the Eq. (8) representation for the \( C_i \) as well as the \( A_i \) values.

The above describes the basic algorithm for evaluating the exponential function of Eq. (1). For the Gaussian function, i.e.

\[ f(x') = \exp(-\alpha x'^2), \quad \text{(9)} \]

one proceeds in exactly the same manner, except that it is necessary to perform an additional multiplication, to obtain \( x'^2 \) from \( x \). We note that there are some specialized quantum squaring algorithms, that shave a bit off of the cost of a generic multiplication [8] [9] [14]. If \( d \ll n \) however, this savings is not significant; the cost of the extra multiplication itself is much less than the others, since it involves only \( d \) rather than \( n \) qubits.

**C. Computational cost and asymptotic scaling**

In terms of memory (i.e., space) usage, the above algorithm requires \( dn + n + d \) qubits in all—not including the ancilla bits needed to actually implement the multiplications (not shown in Fig. 1). As mentioned, the computational cost is simply that of applying \( d \) multiplications. Given the tremendous variety of multiplication algorithms that have been and will be developed—and given that some will always be better than others in different circumstances—we feel it is best to let the number of required multiplications itself serve as the appropriate gate complexity metric. Of course, this requires that multiplications comprise the overall computational bottleneck, as they do here. In similar fashion, the Toffoli count provides another implementation-independent metric—when comparing circuits whose bottleneck is the Toffoli gate (Sec. [V]).

If absolute costs are difficult to compare directly between different methods, then the next best thing to consider is asymptotic scaling—in this case, in terms of the parameters \( n \) and \( d \). For our basic exponentiation algorithm, the scaling with respect to \( d \) is clearly linear—both of the space and gate complexity.

As for the scaling with respect to \( n \), this is determined by the multiplication algorithm itself. At present, the most competitive quantum multiplication algorithm for
First quantum circuit: Basic Implementation of $f(x_0) = \exp(-\alpha x_0)$ on a quantum computer.

FIG. 1. Quantum circuit used to implement basic quantum algorithm for exponentiation, $f(x' = \exp(-\alpha x')$. All multiplications, $\times$, are presumed to be “overwriting,” in the sense that the second input register is overwritten with the product of the two inputs as output.

Asymptotically large $n$ in terms of scaling appears to be that of C. Gidney [14], based on the recursive Karatsuba scheme [15]. The Gidney algorithm requires $O(n)$ space complexity, so that the overall scaling for our basic exponentiation algorithm would be $O(nd)$. Likewise, the gate complexity for a single multiplication scales as $O(n \log_2 3)$, implying $O(n \log_2 3 d)$ scaling for basic exponentiation.

As mentioned, Gidney does not overtake even the simplest (i.e. “schoolbook”) multiplication method until $n$ reaches a few thousand. It is therefore not practical for NISQ computing. In Sec. V more precise estimates will be provided for absolute costs—e.g. in terms of Toffoli counts—presuming multiplication methods that can be practically applied in a NISQ context (Sec. IV). We also improve upon the basic exponentiation algorithm itself—in Sec. III where we adopt a more efficient and refined approach, and in Sec. IV where we present a specific, NISQ implementation.

At this point it is worthwhile to compare the two cases, $d = n$ and $d \ll n$. If the exponentiation operation is itself part of a more complicated mathematical function network, with many nested inputs and outputs, then pre-
sumably one wants a generic $d = n$ code with $n$ sufficiently large to provide “machine precision”—i.e., $n \geq 25$ or so for single precision, or $n \geq 50$ for double precision. The $O(n^2)$ space complexity of our basic exponentiation algorithm likely places such calculations beyond the current NISQ frontier.

On the other hand, there are situations where $d \ll n$, and where $n$ itself may be substantially reduced. For first quantized QCC, for example, it is estimated that $d = 7$ and $n = 21$ may suffice to achieve the so-called “chemical accuracy” benchmark. Such values place the present scheme much closer to the NISQ regime—especially once the refinements of the next section are introduced.

We conclude this subsection with a reexamination of the true cost of the $d \ll n$ Gaussian function evaluation, within the present basic scheme. Though as stated, the $x^2$ operation per se adds little to the direct cost, it does have the effect of squaring the size of the domain interval. Thus, if the full resolution of the domain is to be preserved, this requires $2d$ rather than $d$ qubits—as well as a commensurate doubling of the gate complexity. On the other hand, this relative increase can often be largely mitigated by the improvements introduced in the subsequent sections.

### III. Refined Method

The basic algorithm can be substantially improved, with respect to both space and gate complexity, using the refinements described in this section. For definiteness, going forward we shall generally presume the “NISQ parameter values,” $d = 7$ and $n = 21$, as discussed in Sec. II. However, for comparison and robustness testing, we shall occasionally use the less spartan parameter values, $d = 8$ and $n = 32$ (corresponding to “machine precision”). In both cases, we find that a NISQ calculation is likely feasible in the near-term future.

There are essentially two distinct ideas presented in this section to improve upon the basic algorithm—although other possible options certainly also exist. The first idea is to transform the $A_i$ values between successive multiplications, so that only one such constant need be stored at a time. This will have the effect of reducing the space complexity scaling to $O(n)$, at least for overwriting multiplications. The second idea reduces the actual number of multiplications that need be applied.

#### A. Refinement # 1: reducing space complexity

The parameters $A_i$ have constant values that can be determined prior to the calculation. Rather than storing them in $d$ separate registers, it is far less costly in terms of space to simply transform $A_i \rightarrow A_{i+1}$, prior to each successive multiplication. Such strategies have been used previously in quantum computing, when constant (unsuperposed) register values are employed. If overwriting multiplications are used, it then becomes necessary to maintain only two such $n$-qubit registers—i.e., one to store all of the successive $A_i$ values, and the other to store the (conditionally superposed) $C_i$ values.

The corresponding quantum circuit is presented in Fig. 2 for $d = 7$ and $n = 21$. The upper of the two 21-qubit registers is used to store the $A_i$, with the transformation gate $X_{i(i+1)}$ used to transform $A_i$ into $A_{i+1}$. Similarly, we define transformation gates $X_{0p}$ to convert the zero state $0$ into $A_0$ (or vice-versa). For example, the gate $X_{0p}$ is used at the start of the circuit to initialize $A_0$ from $0$. Likewise, the lower 21-qubit register is initialized to $C$ from $0$, using the transformation gate $X_{Cp}$. Each successive multiplication operation (conditionally) multiplies this value by another factor of $A_i$. In this manner, the total number of qubits is reduced to $2n + d$, or $49$ for the present NISQ example—again, not including the various ancilla bits needed to effect the (overwriting) multiplications in practice.

The strategy above emphasizes minimal space complexity at the cost of greater gate depth. Alternatively, using all $d$ $A_i$ registers as in Sec. II, the multiplications could be performed synchronously and hierarchically, so as to minimize gate depth, but without any space reduction. In any event, our analysis in Sec. IV is all based on non-overwriting multiplications (Sec. IV), for which the situation is a bit more complicated.

We next turn our attention to the implementation of the transformation gates. Since the transformations always correspond to fixed input and output values, they can easily be implemented as a set of very specific NOT gates, applied to just those qubits for which the binary expansions of Eq. 8 differ between input and output values. Hence the notation, $X^p$, to refer to the resultant tensor product of $p \approx n/2$ NOT gates used to effect the transformation.

In Fig. 3 the specific implementation for $X_{01}$ is presented, corresponding to the specific values, $d = 7$, $n = 21$, and $A = 0.389$. The input qubits are in an unsuperposed state corresponding to the $n = 21$ binary expansion of $A_0 = A$, as expressed in the form of Eq. 8 (with $y_0$ corresponding to the top wire, etc.) The output qubits are in a similar state, but corresponding to $A_1 = A^2 = 0.151321$. Generally speaking, we may expect about half of the qubits to change their values. Indeed, for the present example with $n = 21$, we find $p = 10$.

In the refined algorithm as presented in Fig. 2 we find that there is one transformation required per multiplication. However, it is clear from Fig. 3 that the gate complexity of the former is trivial in comparison with that of the latter. In practical terms, therefore, the scheme of Fig. 2 can be implemented at almost no additional cost beyond that of Fig. 1—i.e., we can continue to use multiplication count as the measure of gate complexity.
A presentation of \( p = 21 \), and \( d \) for which \( n \rightarrow \infty \), according to Eq. (5). What is needed, therefore, is an expression for \( m \) in terms of \( A \) and \( n \), where \( m \) is the smallest \( i \) such that \( A_i < 2^{-n} \).

For the \( d = n \) case, it can easily be shown that

\[
m = \left\lfloor \log_2 \left( \frac{n}{\log_2(1/A)} \right) \right\rfloor + 1.
\]

(10)

For the generic case where \( d \) and \( n \) are independent, we still never need more than \( d \) multiplications. So Eq. (10) above gets replaced with the general form,

\[
m = \min \left\{ d, \left\lfloor \log_2 \left( \frac{n}{\log_2(1/A)} \right) \right\rfloor + 1 \right\}.
\]

(11)

Clearly, \( m \) scales asymptotically as either \( O(d) \) or \( O(\log n) \), rather than \( O(n) \), if \( A \) is fixed. This assumes, however, that \( d \) and \( A \) have no implicit dependence on \( n \), which in turn depends on assumptions about how the \( x' \) grid points are increased. If the \( x'_{\text{min}} \leq x' < x_{\text{max}} \) domain interval is expanded keeping the same spacing \( \Delta \), or if \( \Delta \) decreases but \( d \) is kept constant, then the above holds. Otherwise, \( A \to 1 \) as \( n \to \infty \), and the prefactor becomes divergently large, implying a less favorable asymptotic scaling law.

Let us consider the case where \( d < n \). Since \( m(A) \) as described by Eq. (10) increases monotonically with \( A \), there is in general an interval \( 0 < A < A_{\text{max}} \) over which \( m(A) < d \), and so a reduction in the number of multiplications can be realized and \( m < d \). Beyond this point—i.e., for \( A_{\text{max}} \leq A < 1 \), all \( m = d \) basic multiplications must be used. A bit of algebra reveals the following expression for the transition \( A \) value:

\[
A_{\text{max}} = 2^{-n/2^{d-1}}
\]

(12)

As an illustrative example, consider the \( d = 7 \), \( n = 21 \), \( A = 0.389 \) case of Sec. IIIA. The formula of Eq. (10) predicts that \( m = 4 \) multiplications will be required, exactly as indicated in Fig. 2. This represents a significant reduction versus the \( d = 7 \) multiplications that would otherwise be needed. As confirmation that \( m = 4 \) is correct, we note that \( A_3 = 0.00052432 \), which is larger than \( 2^{-21} = 4.76810^{-7} \). However, \( A_4 = 2.74910^{-7} < 2^{-21} \).

Finally, we can compute \( A_{\text{max}} \) from Eq. (12)—which, with the above \( n \) and \( d \) values, is found to be \( A_{\text{max}} = 0.796571 \). Thus, one finds a reduction in \( m \) down from \( d \), over about 80% of the range of possible \( A \) values. Now consider the Gaussian rather than exponential function, for which \( d \to 2d = 14 \). Here, we find \( A_{\text{max}} = 0.998225 \)—implying that there is almost always a reduction in \( m \). We will discuss further ramifications in Secs. IV and V.

![FIG. 3. Quantum circuit used to implement X⊗p on a quantum computer, for specific parameter values, d = 7, n = 21, and A0 = A = 0.389. The n = 21 binary representation of A0 is A0 = 0.0110001110010110100000; that of A1 = A0 = 0.151321 is A1 = 0.00100110110111100011111. The least significant bit, i.e. \( j = 0 \), appears at the top of the circuit. For this example, \( p = 10 \approx n/2 \).](image)
C. Second half of refined quantum algorithm

Although the second refinement of Sec. IIIB can lead to fewer than \( d \) multiplications (depending on the values of \( n, d, \) and \( A \)), this does not imply that the refined quantum algorithm simply ends at the right edge of Fig. 2. There remains a subsequent computation that must occur, using the \( x_{i \geq m} \) qubits, in order to ensure that the correct final value for the function is obtained. The multiplication count of the additional computation is zero, although it does add a cost of \( n \) Fredkin gates.

Consider that when \( x = 2^i \) is a power of two, then all but the \( x_i \) binary expansion coefficients in Eq. 3 vanish, and the function value becomes simply \( f(x) = CA_i \), according to Eq. 6. This implies that for any \( x \geq 2^m \), \( f(x) < 2^{-n} \) is smaller than the minimum non-zero number that can be represented, and so should be replaced with \( f(x) = 0 \). This situation will occur if any of the \( (d - m) \) qubits, \( x_{i \geq m} \), are in their 1 states. Otherwise—i.e., if all \( (d - m) \) of the \( x_{i \geq m} \) are in their 0 states so that \( x < 2^m \)—then nothing should happen, as the lowest register is already set to the correct output value, \( f(x) = C_m \), at the right edge of Fig. 2.

The above can be implemented as follows. First, for the case \( A > A_{\text{max}} \), no additional circuitry is needed; one simply runs the quantum circuit of Fig. 2 as is, except with explicit controlled multiplications across all \( m = d \) of the \( x_i \) qubits. For the case \( m = d - 1 \), then \( d - 1 \) controlled multiplications are implemented across the lowest \( d - 1 \) qubits, \( x_{i < (d-1)} \). The final qubit, \( x_{d-1} \) is then used to conditionally set the lowest register to zero.

For the last case where \( (d - m) \geq 2 \), we apply the quantum circuit indicated in Fig. 3. This requires first checking if any of the \( (d - m) \) \( x_{i \geq m} \) qubits are in state 1, which is implemented using a sequence of \( (d - m - 1) \) OR gates. The first is applied to \( x_m \) and \( x_{m+1} \) to compute \( x_m \lor x_{m+1} \). If needed, that output is then sent to a second OR gate along with \( x_{m+2} \), etc. The final output, which will serve as a control qubit, has value 1 if any of the \( x_{i \geq m} \) are in their 1 states; otherwise, it has value 0.

Meanwhile, the upper of the two \( n \)-qubit registers, which starts out representing the constant value \( A_{m-1} \), is transformed to the value 0, using the transformation gate, \( X_{\otimes p} \). Finally, the upper and lower \( n \)-qubit registers undergo a controlled \( \text{SWAP}^\otimes n \), applied in qubit-wise or tensor-product fashion, across all \( n \) qubits of the two registers. If the swap occurs, then the function output as represented by the lower of the two \( n \)-qubit registers becomes zero; otherwise, it is left alone.

We conclude this subsection with a discussion of the reversible quantum OR gate, used in the quantum circuit of Fig. 4. Such a gate can be easily constructed from a single reversible NAND (Toffoli) gate, together with various NOT gates, as indicated in Fig. 5. Note that each such OR gate introduces one new ancilla qubit, initialized to the 1 state. There are thus no more than \( (d - m - 1) \) additional ancilla qubits in all that get introduced in this fashion. The additional costs associated with Fig. 4, in terms of both gates and qubits, are thus both very small as compared to those of Fig. 2, although they will be
included in resource calculations going forward.

\[
\begin{array}{c}
a \\
b \\
1 \\
a \oplus b
\end{array}
\]

FIG. 5. Quantum circuit used to implement reversible OR gate, constructed out of a single reversible NAND (Toffoli) gate, and various NOT gates.

IV. DETAILED IMPLEMENTATION

SUITABLE FOR NISQ COMPUTING

A. Overview

As discussed, there is large variety of quantum multiplication algorithms on the market currently \[8\] \[10\] \[11\], and no doubt many more will follow. In part for this reason, we prefer to rely on the “multiplication count” metric for gate complexity. Indeed, whereas current multiplication algorithms largely make use of integer or fixed-point arithmetic, floating-point algorithms—which have very different implementations—are also of interest going forward, especially for exponentiation. The multiplication count metric will continue to be relevant for all such innovations.

On the other hand, we are also interested in developing a specific exponentiation circuit that can be run on NISQ computers for realistic applications. Moreover, we aim to compare performance against the state-of-the-art competing method by Hāner and coworkers \[8\], for which multiplications are not the only bottleneck. This constrains us in two important ways. First, we cannot use the multiplication count metric for accurate comparison; instead, since the Hāner algorithm is Toffoli-based (as is our circuit), we use the Toffoli count metric. Second, to the extent that both exponentiation algorithms do rely on multiplications, similar multiplication subroutines should be used for both.

Accordingly, we use a modified version of Hāner’s multiplication subroutine, which is itself a fixed-point version of “schoolbook” integer multiplication \[8\] \[9\] \[12\] \[14\], based on bit shifts and controlled additions. In particular, they exploit truncated additions (that maintain \(n\) fixed bits of precision), together with a highly efficient overwriting, controlled, ripple-carry addition circuit by Takahashi \[13\] \[17\] \[19\] that minimizes both space and gate complexities. As it happens, there are some further improvements and simplifications that arise naturally for our particular exponentiation context, which we also exploit. All of this is described in detail in Secs. IV B and V wherein we also derive fairly accurate resource estimates for both qubit and Toffoli counts, respectively.

One disadvantage of Hāner multiplication is that it does not overwrite the multiplier input—the way, e.g., that QFT multiplication would \[3\] \[10\] \[11\]. Consequently, each successive multiplication requires additional ancilla bits, unlike what is presumed in Fig. 2. Space needs are accordingly greater in this implementation than what is described in Sec. III A—becoming essentially \(mn + d\) qubits rather than \(2n + d\) (without ancilla). For the NISQ applications of interest here, \(m\) is still quite small, and so the increase is generally not too onerous. It is more of a concern for the Gaussian evaluations, for which \(m\) can in principle get twice as large as the corresponding exponential \(d\) value.

Of course, it would be possible to employ QFT-based multiplication in our exponentiation algorithm—which would require \(4n + d\) qubits, with ancilla included. On the other hand, the QFT approach is not Toffoli-based, and would therefore not lend itself to direct comparison with Hāner, vis-à-vis gate complexity. In order to estimate a Toffoli count for QFT multiplication, one would have to presume some specific implementation for the Toffoli gate itself (e.g., in terms of \(T\) gates), which is not ideal \[13\]. In any event, Toffoli counts have become a standard gate complexity metric in quantum computing.

For these reasons, overwriting QFT-based multiplications are not considered further here. Instead, for cases where the increased space complexity of the non-overwriting multipliers might pose a problem, we address this situation through the use of a simple alternative algorithm, describe in Sec. IV C that trades increased gate complexity for reduced space complexity—essentially by uncomputing intermediate results. In principle, there are any number of “reversible pebbling strategies” \[8\] \[13\] \[14\] \[63\] that might also be applied towards this purpose. The particular approach adopted here, though, is very simple, and appears to be quite effective.

B. Non-overwriting controlled quantum multiplication

As discussed, non-overwriting controlled-addition multiplication subroutines have three registers. The first is an input register for the multiplier; the second is another input register for the multiplicand; the third is the output or “accumulator” register. The accumulator register is initialized to zero, and therefore serves as an ancilla register, but comes to store the product of the multiplier and multiplicand at the end of the calculation.

For integer multiplication, the accumulator register requires \(2n\) qubits, assuming that both input registers are \(n\) qubits each. The first register (multiplier) provides the the control qubits for a cascade of \(n\) controlled additions. The second register (multiplicand) serves as the first input for each controlled addition. The second input for each controlled addition is a successively bit-shifted subset of \(n + 1\) qubits from the accumulator register. Note that overwriting controlled additions are used, so that for each controlled addition, the second register output is the sum of the two inputs.
In the case of our exponentiation algorithm, we propose a version of the above basic scheme that is modified in two very important ways. First, the $i$'th multiplication is controlled, via the domain qubit $x_i$ (Fig. 2). Second, the circuit exploits the fact that every multiplier has a fixed (unsuperposed) value—i.e. the constant, $A_i$. Adding an overall control to a quantum circuit tends to complicate that circuit—turning CNOT gates into CCNOT gates, etc. On the other hand, the fixed multiplier enables substantial simplifications—of the type used in Shor’s algorithm for factoring integers \cite{13, 62}, for instance.

Specifically, we no longer treat the multiplier $A_i$ as an input register—for there is no longer a need to use the $A_i$ qubits as control bits for the additions. Instead, the binary expansion of $A_i$ from Eq. (8) is used to hard-wire what would be a set of uncontrolled additions, directly into the quantum circuit—but only for those binary expansion coefficients equal to 1. In addition to reducing the set of inputs by one entire $n$-bit register, this modification also reduces the number of additions that must be performed by a factor of two—since on average, only half of the expansion coefficients have the value 1.

In addition to the above advantages, fixed-multiplier
multiplication reduces circuit complexity by replacing controlled with uncontrolled additions—effectively converting CCNOT gates to CNOT gates. Of course, when the \( x_i \) qubit control is thrown back in, to create the requisite controlled multiplication subroutine, we find that the additions become controlled after all—but by \( x_i \), rather than \( A_i \). In effect, the control bit for the multiplication is simply passed down to the individual controlled additions which comprise it.

The above can all be seen in Fig. 6, our detailed quantum circuit for controlled multiplication, as implemented for the first multiplication in Fig. 2, denoted ‘\( x_0 \)’ (i.e., multiplication by \( A_0 \), controlled by the \( x_0 \) qubit). Note that the individual multiplication circuits, \( x_i \), differ from each other, due to the different \( A_i \) binary expansions. Once again, our canonical NISQ parameter values are presumed, i.e., \( d = 7 \), \( n = 21 \), and \( A = 0.389 \).

From the figure, another important difference from the basic scheme may be observed: the accumulator register, \( z \), has only \( n \) rather than \( 2n \) qubits. This is because fixed-point rather than integer arithmetic is being used—as a consequence of which, it is not necessary to store what would otherwise be the \( n \) least significant bits of the product. This situation provides yet another benefit, which is that each controlled addition becomes “truncated” to an \( s \)-bit operation—with \( s \) increasing with each successive controlled addition across the range, \( 2 \leq s \leq (n-1) \).

Note that the smallest possible addition corresponds to \( s = 2 \) rather than \( s = 1 \). This is because the first controlled addition can be replaced with a cascade of Toffoli gates—or controlled bit-copy operations—which is a much more efficient implementation. This substitution works because the accumulator register \( z \) is set to zero initially. The very first controlled addition thus always (conditionally) adds the multiplicand register \( y \) to zero.

For the example in the figure, the first four binary expansion coefficients for \( A \) (from right to left) are all zero; these bits are simply ignored. The first coefficient equal to one is the \( j = 4 \) or fifth bit. As indicated in Fig. 6, this causes the last four bits of the multiplicand register \( y \) to be (conditionally) copied into the first four bits of the accumulator register—in what would otherwise be an \( s = 4 \) controlled addition. The \( j = 5 \) bit is also equal to one, leading to the first bona fide controlled addition in Fig. 6, with \( s = 5 \). This pattern continues until the next-to-last, or \( j = 19 \) bit is reached, which is the last bit equal to one. This leads to the final controlled addition, with \( s = 19 \).

Although the last \( (j = 20) \) bit is zero, even if it were equal to one, the corresponding controlled addition gate would extend only up to \( y_1 \). Thus, the top wire, \( y_0 \), or least-significant bit of the multiplicand, is never used. This reflects the fact that both numbers being multiplied have values less than one, and that \( n \) fixed bits of precision are maintained throughout the calculation. Note also that, as a result, there are never any overflow errors.

The final part of the controlled multiplication circuit is a cascade of \( n \) controlled bit-copy operations (i.e., modified Toffoli gates), which conditionally set the final output of the accumulator register equal to \( y \), when \( x_0 = 0 \) (hence the open circles). Otherwise, this register would remain zero. Thus, the “do nothing” instruction in Sec. II.B does not literally mean “do nothing” when non-overwriting multiplications are used, as it is still necessary to copy the multiplicand input register to the accumulator output register.

C. Quantum algorithm for exponentiation: space saving alternative

Now that the specific, controlled quantum multiplication algorithm of Sec. II.B has been identified, we can determine a precise estimate of space requirements for our overall exponentiation circuit. (Gate complexity will be discussed in Sec. III.A). As noted, each of the \( m \) multiplications requires a clean \( n \)-qubit ancilla bundle as input for its accumulator register, together with the (accumulator) output from the most recent multiplication as input for its multiplicand register. Thus, for \( m \) successive multiplications, \( m + 1 \) separate registers would be required in all.

However, we can realize significant savings—i.e., one entire register of space, and one entire controlled multiplication subroutine—by exploiting the fact that the first multiplicand (i.e., \( C \)) is a fixed constant. The first controlled multiplication, \( x_0 \), is therefore a controlled multiplication of the constant \( C \) by the constant \( A_0 \). Since both constants are fixed, the controlled multiplication can be much more efficiently realized using two controlled transformation gates acting on a single register (i.e., the first two gates shown in Fig. 4), rather than the controlled multiplication circuit of Fig. 6. Note that this controlled \( x_0 \) implementation uses only CNOT gates; thus the Toffoli count is zero.

Since Takahashi addition does not use additional ancilla qubits \( [18, 19] \), the total number of qubits required to implement the \( m \) multiplications is just \( mn \). In addition to this, we have the \( d \) qubits needed to store the domain register, \( x \), that is used to supply the control qubits. The current qubit count is thus \( mn + d \).

However, if \( m < d \), then the second half of the refined exponentiation circuit (i.e., Fig. 4) must also be executed, which introduces some additional space overhead. To begin with, our current reliance on non-overwriting multiplications implies that we can no longer generate the requisite zero ancilla register (i.e., the next-to-last register in the figure) without significant (un)computation. To avoid this, we instead add a clean new register—at the additional cost of \( n \) new qubits. In addition to this, there are the \( (d − m − 1) \) ancilla bits used by the OR gates, as discussed in Sec. III.C. Altogether then, the total qubit count becomes:

\[
q = \begin{cases} 
  dn + d & \text{for } m = d \\
  (m + 1)n + 2d - m - 1 & \text{for } m < d
\end{cases}
\]
To reduce qubit counts in cases where Eq. (13) renders a NISQ calculation unfeasible, we have developed a “space-saving” alternative algorithm. The general idea is to uncompute some of the intermediate quantities, in order to restore some of the ancilla resources to their initial clean state, so that they can then be reused for subsequent computations. Of course, this requires additional overhead—i.e., in our case, additional controlled multiplications.

More specifically, our space-saving algorithm reduces space requirements from $O(mn)$ down to $O(m^{1/2}n^2)$—a very marked reduction, especially if $m$ is reasonably large. The added cost in terms of gate complexity, on the other hand, is never more than double that of our original algorithm described above. Thus, $m < m_{ss} < 2m$, with $m_{ss}$ the multiplication count for the space-saving approach.

For values of $m$ that lie in the range

$$r(r-1)/2 < m \leq r(r+1)/2$$

(14)

(where $r > 2$ is an integer), the space-saving method requires a total of $r$ $n$-qubit registers to perform all multiplications. Note that the $r > 2$ restriction implies that the method is only applicable for $m > 3$. However, the $m \leq 3$ case presents minimal space requirements, and so the space-saving approach is less likely to be needed. In any event, for all numerical examples considered in Sec. V B (including the worst Gaussian cases), $3 \leq r \leq 5$.

The total qubit count for the space-saving alternative algorithm can be shown to be as follows:

$$q_{ss} = \begin{cases} 
    rn + d & \text{for } m = d \\
    (r+1)n + 2d - m - 1 & \text{for } m = r(r+1)/2 < d \\
    rn + 2d - m - 1 & \text{otherwise}
\end{cases}$$

(15)

Note that unlike our original non-space-saving or “gate-saving” algorithm, a zero $n$-qubit ancilla register can always be made available for the final controlled SWAP $^\otimes n$ operation of Fig. 4, except when $m = r(r+1)/2$, which thus has an additional qubit cost. (See technical note at the end of this subsection).

The space-saving algorithm itself proceeds as follows. First, apply the first $r$ multiplications, exactly as for the earlier gate-saving algorithm. This leaves the $r$ registers in the states, $C_1, C_2, \ldots, C_r$. Then, uncompute all but the most recent multiplication (i.e., the one that provided $C_r$). The first $(r-1)$ registers are thereby restored to zero, but the final register remains in the $C_r$ state. It is then possible to perform $(r-1)$ additional multiplications, before once again running out of registers. All but the last of these is then uncomputed, allowing $(r-2)$ more multiplications to be performed, and so on.

The space-saving quantum circuit used for $d = 7$ and $m = 4 \cdot 6$ is presented in Fig. 7, corresponding to $r = 3$ registers. For the first wave, there are three clean registers, allowing for three successive multiplications, $\times_0$, $\times_1$, and $\times_2$ (provided $\times_0$ is implemented as discussed above). This is followed by two uncompute multiplications for the first two multiplications, denoted $\times_1^{-1}$ and $\times_0^{-1}$ (the latter, again with the new implementation). In the second wave, we apply $\times_3$ and $\times_4$, generating $C_4$ and $C_5$, respectively. This suffices for $m = 4$ and $m = 5$, respectively. However, if $m = 6$, we must undergo a third and final wave, as indicated in the figure.

As is clear from the above description, and from Fig. 7, the number of uncompute multiplications, $m_{un}$, is always less than $m$. Thus, $m_{ss} = m + m_{un} < 2m$, as claimed. Precise values can be found as follows. Let $l$ be the largest integer such that

$$l(l+1)/2 \leq r(r+1)/2 - m.$$  

Then,

$$m_{un} = r(r-1)/2 - l(l+1)/2.$$  

(16)

Table 4 indicates specific values for all $m \leq 36$. Note that the $m_{ss}$ multiplication count includes both $\times_0$ and $\times_0^{-1}$; thus, the total actual number of controlled multiplication subroutines that must be executed is $(m_{ss} - 2)$, as indicated in the final column. From the table, also, it may be observed that greater space savings are usually associated with increased multiplication counts, and vice-versa.

**Technical note:** For $m < d$ space-saving calculations, a zero ancilla register is automatically available at the end of the Fig. 7 circuit (to be used in the subsequent Fig. 4 circuit), whenever Eq. (16) is a true inequality. When Eq. (16) is an equality, then the $l = 0$ case requires the addition of a new zero ancilla register (as discussed), but for $l > 0$, a zero register can be easily created from an existing non-zero register. This is done by applying the single uncompute multiplication, $\times_{m-2}^{-1}$. As an example, the case $m = 5$ corresponds to $l = 1$ and $r = 3$, thus satisfying Eq. (16) as an equality, with both sides equal to one. The necessary uncompute multiplication can be seen in Fig. 7 just to the right of the vertical dashed line marked $m = 5$. Note that the Toffoli count associated with such $i \approx m$ multiplications is greatly reduced in comparison with the other multiplications, as will be discussed in Sec. VA Moreover, this event is fairly rarely realized in practice, including the examples given in the present work. Nevertheless, the small additional cost required in such cases is included in the Toffoli count formulas presented in Sec. VA.

V. ANALYSIS: TOFFOLI COUNTS

A. Present methods

To a rough approximation, the total Toffoli count for the proposed exponentiation algorithm (or for the space-saving alternative) is simply $(m - 1)$ [or $(m_{ss} - 2)$] times the Toffoli count needed to execute a single controlled multiplication subroutine. Before working out the latter,
however, we first describe another reduction of effort that in practical terms, converts the total cost to that of only \((m - 8/3)\) controlled multiplications. This additional savings is fully realized whenever \(m < d\), which in practice occurs much of the time, if the domain interval is realistically large.

The rationale is as follows. When \(m < d\), the \(A_i\) values span the entire range from 1 down to \(2^{-n}\). This implies that for \(i \approx m\), the corresponding \(A_i\) have many leading zeroes. Consequently, these later multiplications can be performed using fewer than \(n\) binary digits, leading to significant computational savings.

Note that the worst-case scenario vis-à-vis the aforementioned savings—i.e., that for which the \(A_{izm}\) have the fewest leading zeros—corresponds to \(A_m \rightarrow 2^{-n}\) from below. Now, in general, the approximate number of leading zeros for the binary expansion of \(0 < y < 1\) is given by \(-\log_2 y\). Thus, for \(y = A_m\), we find \(~n\) leading zeros, as expected. More generally, Eq. (7) in the worst-case
leading zeros \(A_i \approx n 2^{-(m-i)} = n 2^{-k}\), \(18\)

where \(k = (m-i)\). The number of binary digits needed for the \(A_{m-k}\) controlled multiplication is thus \(n_k = n - 2^{-k}\).

Going forward, we shall for simplicity presume the asymptotic limit, \(n \to \infty\). In this limit, the Toffoli count per multiplication scales as \(O(n^2)\). The Toffoli savings (i.e., reduction in the Toffoli count relative to multiplication with \(n\) digits) is therefore

\[
s_k \propto (n^2 - n_k^2) = n^2 (2^{2-k} - 2^{-2k})
\]

Summing Eq. (19) from \(k = 1\) to \(\infty\) then yields a total savings of 5/3 multiplications.

In practice—i.e., for finite \(n\)—the series is truncated, and so the actual savings is less than 5/3 multiplications. In the worst case (of the worst case), only the \(s_1\) term contributes to the sum, resulting in a lower bound of 3/4 multiplications. On the other hand, a small increase in \(A_m\), such that the new value is slightly greater than \(2^{-n}\), will increment the value of \(m\)—thus, effectively increasing the savings by one whole additional multiplication. On balance, we therefore take our 5/3 “best case of the worst case” value as a reasonable middle-ground estimate.

Next, we move on to a calculation of the Toffoli cost of each controlled multiplication. As discussed in Sec. [IVB] these are implemented using a sequence of controlled additions, with from \(s = 2\) qubits up to \(s = (n-1)\) qubits. Note that the Toffoli cost of the highly efficient overwriting, controlled, ripple-carry addition circuit of Takehashi \([8, 18, 19]\) with \(s\) qubits is \(3s + 3\). Thus, if every \(2 \leq s \leq (n-1)\) required a controlled addition, the total contribution to the Toffoli cost of multiplication would be \((3/2)n^2 + (3/2)n - 9\). However, since only half of these multiplications are realized on average, in practice, the actual cost per multiplication is half of this. The total contribution to the cost of the exponentiation circuit is then this value, multiplied by the effective number of multiplications, i.e. \((m - 8/3)\).

Now, in addition, each controlled multiplication in the Fig. 6 circuit also begins and ends with a cascade of additional Toffoli gates. The initial cascade can be easily shown to consist of two Toffoli gates, on average. The final cascade, is always \(n\) Toffoli gates, even when fewer than \(n\) qubits are needed to execute the main part of the multiplication circuit (i.e., the controlled additions). Note that both Toffoli cascades are required in every actual multiplication. The total contribution to the Toffoli cost of the exponentiation circuit is thus \((m-1)(n+2)\).

Finally, there are the additional costs associated with the second half of the (refined) exponentiation circuit, as presented in Fig. 14 presuming \(m < d\). Since each Fredkin gate can be implemented using a single Toffoli gate, the Toffoli cost of the final SWAP operation is \(n\). Likewise, each OR gate requires one Toffoli gate, for a total Toffoli count of \((d - m - 1)\). Altogether, we wind up with the following expression for the total Toffoli cost for the entire gate-saving exponentiation circuit:

\[
T = \begin{cases} 
\left(\frac{3d}{4} - 2\right)n^2 + \left(\frac{3d}{4}\right)n - \frac{5}{2}d + 10 & \text{for } m = d \\
\left(\frac{3m}{4} - 2\right)n^2 + \left(\frac{7m}{4}\right)n - \frac{7}{2}m + d + 9 & \text{for } m < d 
\end{cases}
\]

(20)

Things are a bit more complicated in the space-saving algorithm case. In particular, there are three cases instead of two. In addition to \(m = d\), there are two different \(m < d\) cases, i.e. one corresponding Eq. (19) being an equality, and one to the inequality case, as discussed in the Technical note at the end of Sec. [IVC]. Note also that the uncompute multiplications that are not included in \(m_{un}\) (as compared to \(m\)) are in fact the \(i \approx m\) multiplications, that do not cost as much. Consequently, the effective number of uncompute multiplications is reduced relative to the actual number, by an amount less than 5/3 multiplications. A more accurate estimate of
the uncompute savings is given by

$$S_{\Delta m} = \sum_{k=1+\Delta m}^{\infty} s_k = n^2 \left(2^{2-\Delta m} - 2^{-2\Delta m}/3\right)$$ \hspace{1em} (21)

where $\Delta m = (m - m_{\text{min}})$.

Taking all of the above into account, we obtain the following expression for the Toffoli count of the space-saving exponentiation algorithm:

$$T_{ss} = \begin{cases} 
(m_{ss} - \frac{11}{3} - S_{\Delta m}) \left(\frac{3}{4}n^2 + \frac{3}{4}n - \frac{9}{4}\right) + (m_{ss} - 2)(n+2) & \text{for } m = d \\
\langle \text{above} \rangle + n + d - m - 1 & \text{for } m < d \\
\langle \text{above} \rangle + \frac{n^2}{11} \left(\frac{3}{4}n^2 + \frac{3}{4}n - \frac{9}{4}\right) + (n+2) & \text{for } m < d \text{ and } l > 0 \text{ and } l(l+1)/2 = r(r+1)/2 - m 
\end{cases}$$ \hspace{1em} (22)

Note that in the final case above, the (worst-case) cost of the additional $\times_{m-2}^1$ uncompute multiplication is obtained from $s_2$ in Eq. (19) to be $9/16$ that of a regular multiplication—at least insofar as the controlled addition contribution is concerned.

### B. Explicit numerical comparison with H"aner approach

In the approach by H"aner et al. [8], arbitrary functions are evaluated via a decomposition of the $x'$ domain into $M$ non-intersecting subdomain intervals, as discussed in Sec. I. A given function is then approximated using a sequence of $d$th order polynomial in each subdomain. Both the polynomial coefficients, and the subdomain intervals themselves, are optimized for a given target accuracy, using the Remez algorithm [64].

Once the optimized parameters have been determined for a given function $f(x')$, domain interval $x_{\text{min}} \leq x' < x_{\text{max}}$, and (H"aner) $d$ value, the quantum algorithm is then implemented as follows. First, polynomials are evaluated using a sequence of $d$ multiplication-accumulation (addition) operations. On a quantum platform, these can be performed in parallel, across all $M$ subdomains at once, using conditioned determination of the coefficients for each subdomain. The multiplication count would thus be $d$, irrespective of $M$. Also, since non-overwriting multiplications are used, the qubit count is $O(nd)$.

Note that generally speaking, lower $d$ corresponds to greater $M$, and vice-versa. Thus, were the above multiplication-accumulation operations the only significant computational cost, one would simply choose a very small value such as $d = 1$. However, there is additional space and gate complexity overhead associated with managing and assigning the $M$ sets of polynomial coefficients. These costs do increase with $M$ (although in a manner that is naturally measured in Toffoli gates rather than multiplications). There is thus a competition between $M$ and $d$, with minimal Toffoli counts resulting when $d = 4$ or 5—at least for the numerical examples from Ref. [8] that are considered here.

The minimal-Toffoli choice of $d$ can thus be thought of as a “gate-saving” H"aner implementation. Note that a rudimentary “space-saving” alternative may also be obtained, simply by reducing the value of $d$. That said, Ref. [8] also discusses the use of much more sophisticated pebbling strategies. However, such strategies are not actually implemented for the numerical results presented in Ref. [8] that are used for comparison with the present results.

Instead, H"aner and coworkers perform calculations for different functions, and for different target accuracies, across a range of different $d$ values—providing total qubit and Toffoli counts for each. In particular, they consider both the exponential and Gaussian functions, with $x'_{\text{min}} = 0$ and $\alpha = 1$. It thus becomes mostly possible to provide a direct comparison between the H"aner approach and our methods, with respect to these metrics. Such a comparison is provided in Table III.

One slight difficulty arises from the fact that no $x'_{\text{max}}$ value is provided in Ref. [8] moreover, the authors have not been available for clarification. We thus present results for our methods using two very different $x'_{\text{max}}$ values—i.e., 10 and 100. Although for most purposes, even the former interval is wide enough to capture the main function features, the latter interval is actually more realistic for certain applications such as QCC (as discussed in greater detail in Sec. VI). In any case, it should be mentioned that in the large $x'_{\text{max}}$ limit, our methods become less expensive, whereas the H"aner approach becomes more expensive—owing to the increased $M$ values needed to achieve a given level of accuracy.

The issue of target range accuracy merits further discussion. In H"aner, calculations were performed to an accuracy of $10^{-7}$, and also $10^{-9}$. The corresponding number of bits needed to resolve the range to these thresholds are 23.25 and 29.89, respectively. Note that these values are quite close to the $n = 21$ and $n = 32$ values considered in our examples thus far—in one case a bit high, in the other a bit low. Of course, a few extra bits might also be needed to compensate for round-off error in the fixed-point arithmetic. These are relatively small effects however; in particular, they are likely no larger than those associated with the unknown H"aner $x_{\text{max}}$ value.

For our purposes, therefore, we take these $n$ values as reasonable estimates, at least for the exponential function evaluations. For the Gaussian case, we go ahead and use $n = 24$ and $n = 30$, as the closest integers larger than the threshold values listed above. As for the corresponding $d$ values, roughly speaking, these would be double those from the exponential calculation—except that we exploit symmetry of the domain to reduce these by one bit each. Thus, $d = 13 = 2 \times 7 - 1$ and $d = 15 = 2 \times 8 - 1$, respectively, for $n = 24$ and $n = 30$.

In Table III, we present Toffoli and qubit counts for both function evaluations (i.e., exponential and Gaussian), for both target accuracy thresholds (i.e. $10^{-7}$ and $10^{-9}$).
and $10^{-9}$, for both of our methods (i.e. gate-saving and space-saving), and for both domain intervals (i.e. $0 \leq x' < 10$ and $0 \leq x' < 100$). For each function, the minimal Toffoli count is given in bold face. For each function and accuracy threshold, we also present results for the full set of Høner calculations, as obtained from Ref. [8]. Here too, the minimal Toffoli count is highlighted in bold face.

In all cases, our method requires far fewer Toffoli gates than the Høner approach. In comparing minimal-Toffoli calculations for the exponential function, the Toffoli count is reduced from 15,690 using Høner, down to just 912 using our approach. For Gaussian function evaluation, the Toffoli count comparison is even more stark—i.e., 19,090 vs. just 704. Generally speaking, our methods also require fewer qubits than Høner. This is especially true for the space-saving alternative, which in one instance requires as few as 71 qubits (and 1409 Toffoli gates)—a NISQ calculation, certainly, by any standard.

VI. SUMMARY AND CONCLUSIONS

After the various refinements and NISQ-oriented details as presented in the latter 2/3 of this paper, it might be easy to lose sight of the main point, which is simply this: the method presented here allows the exponential function to be evaluated on quantum computers for the cost of a few multiplications. This basic conclusion will continue to hold true, regardless of the many quantum hardware and software innovations that will come on the scene in ensuing decades.

In particular, there is a plethora of multiplication algorithms available, both overwriting (e.g. QFT-based) and non-overwriting (e.g. controlled addition), and for both integer and fixed-point arithmetic—with new strategies for floating-point arithmetic, quantum error correction, etc., an area of ongoing development. Given this milieu, we propose the implementation-independent “multiplication count” as the most sensible gate complexity metric, for any quantum algorithm whose dominant cost can be expressed in terms of multiplications. The present algorithms are certainly of this type.

For our exponentiation strategy, the (controlled) multiplication count $m$ will indeed be rather small in practice—at least for the applications envisioned. To begin with, in a great many simulation contexts, the domain resolution as expressed in total qubits $d$, is far less than the range resolution $n$—with $m \leq d$. For QCC, for instance, the $d = 7$ and $d = 8$ values considered throughout this work are likely to suffice in practice [60]. Conversely, we also consider the asymptotically large $n = d$ limit, in which it can be shown [in Eq. (10)] that $m = O(\log n)$ for fixed $A$. In this limit, Karatsuba multiplication provides better asymptotic scaling. Using the Gidney implementation, the Toffoli and qubit counts for exponentiation scale as $O(n^{\log_2 3} m)$ and $O(n m)$, respectively.

In the latter part of this paper, we present two specific, NISQ implementations of our general exponentiation strategy, in order that detailed resource estimates can be assessed, and compared with competing methods. When compared with the method of Høner and coworkers, our implementations are found to reduce Toffoli counts by an order of magnitude or more. Qubit counts are also (generally) substantially reduced. Note that our two implementations are complementary, with one designed to favor gate and the other space resource needs. Together, they may provide the flexibility needed to actually implement exponentiation on NISQ architectures—which could serve as the focus of a future project.

Finally, we assess the present exponentiation algorithms within the context in which they were originally conceived—i.e., quantum computational chemistry (QCC). The long-awaited “(QCC) revolution” [1-3 5 7 21 49] may be nearly upon us, although achieving full quantum supremacy will likely require quantum platforms that can accommodate first-quantized methods. On classical computers, the Cartesian-component separated (CCS) approach, as developed by the author [57 61] offers a highly competitive first-quantized strategy.

On quantum computers, the question appears to boil down to the relative costs of the exponential function vs. the inverse square root [65]. Toffoli count estimates for the former appear in Table [1]. Note that the larger-domain-interval calculations—i.e., those with lower Toffoli counts—are the more realistic in this context. This is because the QCC CCS implementation requires multiple exponentiations with different $\alpha$ values to be performed, across the same grid domain interval—which must accordingly be large enough to accommodate all of them. Our exponentiation cost of 704 Toffoli gates should thus be compared to the cost of the inverse-square-root function, which—again, according to the highly optimized method of Høner and coworkers—is estimated to be 134,302 Toffoli gates.

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TABLE II. Toffoli and qubit counts for exponential \(\exp(-x')\) and Gaussian \(\exp(-x'^2)\) function evaluations, using three different methods: gate-saving (ours); space-saving (ours); Häner. For our methods, two different domain intervals are used: \(0 \leq x' < 10\) and \(0 \leq x' < 100\). Two different target accuracies are considered: \(10^{-7}\) (Columns IV–VI) and \(10^{-9}\) (Columns VII–IX). For the former, bold indicates minimal Toffoli count from among a given set of calculations, i.e. ours vs. Häner.

| Function           | Method       | Domain interval | \(10^{-7}\) Accuracy | \(10^{-9}\) Accuracy |
|--------------------|--------------|-----------------|------------------------|------------------------|
| \(\exp(-x')\)     | gate saving  | \(0 \leq x' < 10\) | (21, 7, 7) 1620 154 | (32, 8, 8) 4438 264 |
|                    |              | \(0 \leq x' < 100\) | (21, 7, 5) 912 134 | (32, 8, 6) 2828 233 |
|                    | space saving | \(0 \leq x' < 10\) | (21, 7, 5) 2308 91 | (32, 8, 8) 7531 136 |
|                    |              | \(0 \leq x' < 100\) | (21, 7, 5) 1409 71 | (32, 8, 6) 4278 105 |
| Häner              |              |                 | 17304 149 | 45012 175 |
|                    |              |                 | 156990 184 | 28302 216 |
|                    |              |                 | 16956 220 | 25721 257 |
|                    |              |                 | 18662 255 | 26452 298 |
| \(\exp(-x'^2)\)   | gate saving  | \(0 \leq x' < 10\) | (24, 13, 12) 4468 325 | (30, 15, 14) 8300 465 |
|                    |              | \(0 \leq x' < 100\) | (24, 13, 4) 704 141 | (30, 15, 7) 3232 262 |
|                    | space saving | \(0 \leq x' < 10\) | (24, 13, 12) 7546 133 | (30, 15, 14) 14479 165 |
|                    |              | \(0 \leq x' < 100\) | (24, 13, 4) 962 93 | (30, 15, 7) 5018 142 |
| Häner              |              |                 | 20504 161 | 49032 187 |
|                    |              |                 | 190990 199 | 32305 231 |
|                    |              |                 | 21180 238 | 30234 275 |
|                    |              |                 | 23254 276 | 31595 319 |

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