APack: Off-Chip, Lossless Data Compression for Efficient Deep Learning Inference

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Abstract—Data accesses between on- and off-chip memories account for a large fraction of overall energy consumption during inference with deep learning networks. We present APack, a simple and effective, lossless, off-chip memory compression technique for fixed-point quantized models. APack reduces data widths by exploiting the non-uniform value distribution in deep learning applications. APack can be used to increase the effective memory capacity, to reduce off-chip traffic, and/or to achieve the desired performance/energy targets while using smaller off-chip memories. APack builds upon arithmetic coding, encoding each value as an arithmetically coded variable length prefix, plus an offset. To maximize compression ratio a heuristic software algorithm partitions the value space into groups each sharing a common prefix. APack exploits the memory access parallelism of machine learning workloads to replicate and operate several encoder/decoder units in parallel. Combined with the ability to pipeline these units so that they can be time multiplexed across several data streams, allows APack to keep up with the data bandwidth demands of the target workloads. In the demonstrated configuration, APack is placed just before the off-chip memory controller, where it transparently to the rest of the on-chip system compresses and decompresses data. The rest of the on-chip memory and compute units thus see the original data stream. As a result, APack can be used with any machine learning accelerator such as for example vector-like or tensorcore units which are found in modern graphics processors [16], [32], systolic arrays such as those used in the Tensor Processing Unit [33], and units that process sparse tensors such as those used in the SCNN accelerator [48]. We implemented the APack compressor and decompressor in Verilog and in a 65nm tech node demonstrating its performance and energy efficiency. Indicatively, APack reduces data footprint of weights and activations to 60% and 48% respectively on average over a wide set of 8-bit quantized models. It naturally adapts and compresses models that use even more aggressive quantization methods. When integrated with a Tensorcore-based accelerator, APack boosts the speedup and energy efficiency to $1.44 \times$ and $1.37 \times$ respectively.

I. INTRODUCTION

Much of the overall energy consumption and latency during deep learning inference is due to memory accesses [13], [25]. Lossless value compression, by reading and writing fewer bits per value, improves energy efficiency and execution time performance without affecting model accuracy. Since compression relies on value content, it complements other optimization techniques such as dataflow and blocking, [8], [9] and quantization [12], [18], [20], [46], [49]. The benefits with compression can be particularly pronounced for off-chip accesses as compared to on-chip accesses they incur an order of magnitude more energy and latency [26].

Memory compression has been proven effective for general purpose applications, however, Delmas et al., demonstrated that methods for general purpose system are not well suited for capturing the unique properties of the value stream of deep learning workloads [36]. This has led to the development of specialized compression methods [7], [17], [20], [36], [52]. Several designs incorporate run-length encoding for zeros [10], [19], [38]. Deep Compression quantizes the parameters (weights) into a 16-entry dictionary of 16-bit values which are Huffman encoded off-chip [20]. It uses fine-tuning to recover any accuracy losses. Rhu et al., capitalize on the high frequency of zeros [52], Delmas et al., target prefixes of 0s and 1s at the bit-level [36], and Cavigelli et al., pack a group of values bit-level-wise before compression [7]. Finally, Edo et al. target prefixes of 0s or 1s in the on-chip memory hierarchy [17]. As effective they are, these methods either place additional constraints on the values of the weights while not compressing activations, or target specific value patterns.

We improve upon past methods by presenting APack, a lossless off-chip compression method that naturally exploits any non-uniformity in the distribution of fixed-point weights and activations during inference. APack builds upon Arithmetic Coding (AC) [4], [53], [54], an encoding/decoding method that can achieve nearly optimal coding efficiency (e.g., it can encode extremely frequent values using just a fraction of a bit). Since its inception, much of work on AC moved along two general directions: Firstly, works that maximize compression ratio such as dynamic adaptation [65] which generally increase implementation cost and complexity. Secondly, works improving implementation efficiency, e.g., [29], [45]. Regardless, using AC for off-chip compression during deep learning inference is challenging for three reasons: 1) AC implementations remain costly in area, latency, and energy. 2) Maximizing compression ratio requires assigning a probability of occurrence to each possible data value which in turn needs comparatively large lookup tables which further exacerbates area, latency, and energy costs. 3) AC is sequential in nature which is at odds with the wide, and high-bandwidth needs of deep learning.

To benefit from the high coding efficiency of AC, APack balances compression effectiveness vs. implementation cost, energy efficiency, and throughput. For this purpose, APack partitions the value space of the activations and weights into subranges so that every value $v$ can be mapped to a ($symbol$, $offset$) pair such that $v = symbol + offset$ and where the values within
the same sub-range share the same prefix symbol. APack selects these sub-ranges to maximize encoding efficiency. Intuitively, the more frequent a value is the smaller the sub-range APack selects to contain it. At the extreme, a sub-range could even contain just a single frequent value necessitating no offset. APack tailors the sub-range selection to the expected value distribution per tensor to maximize coding efficiency. The process is outlined below.

APack uses these sub-ranges to encode each tensor into two streams, one encoding the symbol sequence, and another containing the corresponding offsets. Both streams are read and written sequentially which improves off-chip memory bandwidth utilization and energy efficiency. APack uses arithmetic coding only for the symbol stream. The required probability count and symbol assignment tables (see Section IV), or probability tables for short, APack derives using profiling. Each probability count represents the expected frequency of occurrence of a sub-range of values, a key design choice that achieves low cost implementation with little loss in compression effectiveness. A table with just 16 symbols proves sufficient. A heuristic search algorithm constructs this table using a sample run of the network. While individual activations vary considerably with the input, their overall distribution per layer varies little enabling APack’s profile-based approach.

APack is directly compatible with any accelerator, such as graphics processors [16], [32], systolic arrays [33], or grid-like designs targeting sparsity [48]. Figure 1 shows that for an example systolic-array accelerator, APack’s purpose-built, efficient, and low-cost hardware encoder/decoders sit in-between the on-chip and the off-chip memory hierarchy where they seamlessly decode and encode values as they are being read or written from off-chip. Several encoder/decoder units operating concurrently meet the high bandwidth demands of on-chip processing. The off-chip memory hierarchy still sees regular streams of DRAM-friendly wide accesses, albeit ones containing fewer accesses whereas the on-chip memory hierarchy and the processing units still see the original values. APack works with any desired dataflow transparently packing data in memory so that they can be fed into the corresponding units with little cost.

Prior to loading the inputs for a layer, APack loads the probability count tables into the hardware decoders and then proceeds to decode the input data using sequential accesses to the symbols and offset streams. Each decoder produces one value per cycle. To sustain the bandwidth needed by the workloads, APack deploys several decoders operating in parallel. For this purpose, the input data stream is partitioned into separate substreams (an approach commonly used in deep learning accelerators [31]), each of which is decoded independently using several decoding units operating concurrently. On the output of each layer one or more encoder units encode the values into symbol and offset streams prior to writing to memory. Each encoder can encode one value per cycle. Each encoder and decoder can be pipelined and it can time-multiplex over multiple streams. APack’s encoders and decoders use fixed-point logic and two small tables each containing 16 rows of 10b and 11b values respectively. Encoding each stream requires 3 16b registers and 2 8b registers for maintaining state while requires 3 16b registers and 1 8b register.

APack boosts the effective off-chip capacity and bandwidth without requiring any modifications to the neural network model. To a neural network developer APack presents a system that needs to go off-chip less often and that rewards well established model optimizations such quantization and pruning without requiring them. More generally, APack will reward any method that yields more biased value distributions. For system designers APack reduces the amount of off-chip memory and thus the cost needed to meet a desired performance target.

We highlight the following experimental results:

- The APack compressor and decompressor when implemented in a commercial 65nm tech node occupy respective 0.02mm² and 0.017mm² area and consume 2.8mW and 2.65mW of power.
- The compression rate for the activations of the various DNNs we experimented with vary from 1.43× to 4.2× and is 2.2× on average.
- The compression rate for the weights vary from 1.13× to 1.4× and is 1.8× on average.
- APack naturally rewards quantization delivering further reductions in traffic as non-uniformity in the value distribution is still present even when extreme quantization is used. It excels at exploiting sparsity for pruned models.
- When integrated with a Tensorcore-based inference accelerator, APack unlocks a speedup of 1.44× by avoiding stalls for off-chip transfers and enabling much better use of the accelerator’s compute units. In addition, APack boosts energy efficiency of the accelerator by 1.37×.

II. CHALLENGES AND OPPORTUNITIES

As motivation Figure 2 presents the cumulative distribution of the frequency of occurrence for the values of two layers. The first is Layer 10 from Q8BERT and the second is Layer 1 from BILSTM (see Table II for a list of all the models studied) both quantized to 8b fixed-point. The distributions are far from uniform: Around half of the values tend to be close to zero, where another half or so tends to be close to 255. Conventional memory hierarchies do not capitalize on this property as they store all values using a container which is sufficiently long to accommodate any value possible. Prior compression work takes advantage of such distributions (see Section VIII). For example, Shapeshifter does not store prefixes of 0s (group near zero) or 1s (group near 255). However, as the bit length
is encoded explicitly using an extra field, the values are first grouped so that they can all use the same size container. This reduces encoding efficiency. It also uses a bit vector to remove zero values which further reduces efficiency when zeros are not as frequent.

In contrast, arithmetic coding does not rely on value magnitude or any in value content in general. Instead, it utilizes a number of bits that is proportional to the frequency of each value. It outperforms other encoding methods that rely on frequency such as Huffman coding, as it can assign even a single value. Let us consider instead the sequence ABAC.

This section is a refresher of arithmetic coding fundamentals – more appropriate introductions are available [35], [44]. At a high-level arithmetic coding converts an input sequence of symbols (in our case values) into a code which is a value between 0 and 1. The code uniquely identifies the input sequence and can be used to reproduce it. The precision, i.e., the number of bits needed to represent this code depends on the frequency of each value. For maximal compression efficiency, arithmetic coding needs arbitrary precision number precision and arithmetic.

Let us consider an example of encoding four values (symbols in AC parlance) A through D, respectively with frequencies of 0.4, 0.1, 0.3, 0.2. Arithmetic coding could work by assigning the range [0,0.4) to A, the range [0.4,0.5) to B, and [0.5,0.8) and [0.8,1.0) respectively to C and D. Then a single A can be represented by any number in the [0,0.4) range, whereas any value in [0.4,0.5) represents a single B. While this may seem inefficient, this is only because we are looking presently at single values. Let us consider instead the sequence ABAC. Arithmetic coding progresses by maintaining a range [low,high] which initially is [0.0,1.0). It first encodes A restricting the range to [0.0,0.5). To encode the B that follows, it further restricts the current range to its [0.4,0.5) sub-range. The new range becomes [0.20,0.25). To encode the next A, the coder further restricts the current range to its [0.0,0.5) sub-range. Thus the range becomes [0.2000,0.2025). Notice that prior to A, the range had a width of 0.05 = 0.25 – 0.20 and that the high mark for A is 0.5 making the new high mark 0.20 + 0.05 × 0.5 off the new low (which stays at 0 as A is assigned the range starting at 0). Encoding the final B requires further restricting the existing range to its [0.8,1.0) sub-range, or to [0.2002,0.2025). Any value within this range can be used to represent the encoded sequence of ABAC. The longer the input sequence, the more precision the resulting encoded number will need. It is for this reason that as presented AC requires arbitrary precision arithmetic.

Formally, Arithmetic Coding accepts a sequence S of input symbols $S = s_N,...,s_i,...,s_0$ from vocabulary $V$ of symbols $\{v_j,...,v_0\} \in V$ and a table of ranges $[phigh_j, plow_j]$, one per symbol in $V$. For maximal compression, the size of each range has to be proportional to the probability of occurrence of the respective symbol. Arithmetic coding outputs a code value, a number in $[0,1)$ which uniquely represents the input sequence S. Internally, the method uses two state variables high and low. The following is a pseudo-code implementation:

```
Algorithm 1: Basic Arithmetic Coding: Infinite precision method.
Data: $S = s_N,...,s_i,...,s_0$ from vocabulary $V$ of symbols $\{v_j,...,v_0\} \in V$ and a table of ranges $[phigh_j, plow_j]$, one per symbol in $V$.
Result: code representing the input sequence $S$.
1    low = 0.0; high = 1.0;
2    while $i < N$ do
3        $s = s_i$;
4        probh = phigh$_i$; probl = plow$_i$;
5        range = high − low + 1;
6        high = low + probh/range;
7        low = low + probl/range;
8        i++
9    code ← low;
```

Encoding starts by setting the current range boundaries to [0.0,1.0) in line 1. Each symbol $s_i$ is read in line 3, and it is used to index the table of ranges in line 4. Line 3 calculates the current range length range. The new boundaries are offset from the current low boundary, by adding the scaled with range symbol boundaries.

IV. APack

While effective, the presented arithmetic coding method has features that are undesirable for hardware implementation: 1) It requires infinite precision arithmetic, and 2) uses a range table with one entry per potential input value.

Approximations of infinite precision arithmetic may be possible, however, they are expensive, moreover they would require execution time that is proportional to the current precision. As we expect to be encoding/decoding tensors of several thousands of elements, even if the implementation cost was not prohibitive, the execution time, and energy would render this approach unprofitable. Fortunately, there are implementations of arithmetic encoding that use finite precision. APack's arithmetic coding is inspired by Nelson's software implementation [44]. APack however, implements a single step encoding/decoding process where all updates to the state (high, low, and code) are done in a single step (the aforementioned implementation updates and produces one bit at a time) and where arithmetic coding is used only for
a variable portion of each input value (the aforementioned arithmetic coding assumes that whole values of a fixed-length are encoded).

Using a table with one entry per potential input value would be prohibitively expensive energy- and area-wise for our purposes. Given that the encoder and decoder process one symbol (values) per step, we would like to keep area and energy costs to a minimum so that we can replicate the units to achieve high bandwidth data supply. For 8b models we would need to have at least one table of $256 \times 10b \times 2 \approx 5Kb$ of storage just for the range table (the overheads would be even higher for 16b models which are still used in certain applications that require high resolution output such as segmentation). Even if the area was not a concern, the energy required to access such a table would be prohibitive.

Instead of assigning a table entry per symbol, APack uses a limited number of entries by partitioning the input value space into several non-overlapping ranges $[v_{\text{min}}, v_{\text{max}}]$. Every value $v$ within the range is encoded as $(\text{symbol}, \text{offset})$ where $\text{symbol} = v_{\text{min}}$ and $\text{offset} = v - \text{symbol}$ an unsigned integer of $\text{OL} = \lg(v_{\text{max}} - v_{\text{min}})$ bits. Additionally, $v_{\text{min}}$ is always of the form $x...x0..0$, that is it a bit prefix of all values within the range. We have experimented with several 4b, 8b, and 16b models and found that using 16 ranges, with 8b $v_{\text{min}}$ and $v_{\text{max}}$, and 3b $\text{OL}$ (4b for 16b models) is sufficient.

The APack encoder accepts an input sequence of values and compresses it, a value at a time, into two sequences. It encodes each value into a $(\text{symbol}, \text{offset})$ pair according to the range it maps to. It then arithmetically encodes just the symbol ($v_{\text{min}}$) while storing the offset verbatim using only as many bits as necessary (very frequent symbols may end up using no offset bits). The encoded symbols comprise the first output stream, and the corresponding offsets comprise the second stream. The process completes when the last symbol is encoded. Along with the two encoded streams, APack also stores metadata that contain: 1) the number of symbols encoded (this is used to terminate decoding), and 2) the range table and the probability table (a total of 298 bytes) used by the arithmetic coder.

To perform arithmetic coding each value range is also assigned a probability count range (low, high). We use 10b probability counts, and we always assign the full range of $\{0x0,0x3ff\}$ across the symbols. A software profiler (see Section VI, uses a heuristic algorithm to determine value ranges that reduce the overall footprint comprising the encoded symbol and offset streams.

Table I shows an example symbol table for the weights of a layer of BILSTM (see Section VII). The fields "IDX" and 'p' respectively report the row index and the symbol probability and are shown for clarity — they are not stored. Row 0 captures the four values in the range $[0x00,0x03]$ and associates all with the probability count range of $[0x000,0x1EB]$ which corresponds to a probability ‘p’ of 0.4795. Any value in this range will be mapped to symbol 0 which during decoding will be mapped back to $v_{\text{min}} = 0x00$. To recover the original number, an $\text{OL} = 2b$ will be recorded such that $v = v_{\text{min}} + \text{offset}$. Rows 3 through 12 are all assigned to a zero length probability count range $([0x23A,0x23A]$ where low = high). These are values that do not appear at all in the input weight tensor. Since weights are statically known, this is permissible. Row 13 captures all values in the range of $[0xD0,0xF3]$ which will be mapped to symbol 13. Notice that the offset requires 6 bits since $0xF0 - 0xD0 = 0x23$. Since $0x23 < 2^6 - 1$ this means that not all offset values will be used for this range. No special processing is needed to ensure that this is so. If we implement the table using all fields shown, then entries with 0 probability can be omitted, and the order of rows can be changed at will enabling power gating opportunities. In the implementation studied the symbols are ordered such that $v_{\text{min}}[i] = v_{\text{max}}[i - 1] + 1$ for $i > 0$ so that we need to store only one of the two per row. Similarly we only store the high count per row.

The APack decoder accepts as input two sequences: 1) the compressed symbols and 2) the corresponding offsets. It outputs the original values. At each step, it uses arithmetic decoding on the symbol sequence to obtain first the value prefix that corresponds to the next symbol. Using the symbol table it then extract the appropriate number of offset bits, which it adds to the value prefix. The process continues until all symbols have been decoded. Our decoder produces a single value per step. Using pipelining and replication we can achieve the desired bandwidth target.

## V. APack Implementation

Figure 3a shows the interface and high-level organization of an example implementation of the APack encoder. The following ports are used for initialization once before processing each layer. We use separate encoders for activations and weights: 1) HI_in and LO_in: initialize the decoder range in two internal 16b registers (the extra 1b signal is an enable). 2) SYMT_in: initialize the symbol table’s value ranges and offsets. The implementation assumes that: i) the full range is mapped, and ii) the rows are ordered in value (symbol) order. 3) PCTN_in: initialize the probability count entries, each using 10b. It is ordered to match the symbol table. 4) The 8b IN port along with its 1b enable are used to send the input value that needs to be decoded in this step (if any – enable). 5) The 1b done signal terminates encoding.

| IDX | v_min | v_max | OL | low  | high  | p     |
|-----|-------|-------|-----|------|-------|-------|
| 0   | 0x00  | 0x03  | 2   | 0x000| 0x1EB | 0.4795|
| 1   | 0x04  | 0x07  | 2   | 0x1EB| 0x229 | 0.0605|
| 2   | 0x08  | 0x0F  | 3   | 0x229| 0x238 | 0.0148|
| 3   | 0x10  | 0x3F  | 6   | 0x238| 0x23A | 0.0020|
| 4   | 0x40  | 0x4F  | 4   | 0x23A| 0x23A | 0.0000|
| 5   | 0x50  | 0x5F  | 4   | 0x23A| 0x23A | 0.0000|
| 6   | 0x60  | 0x6F  | 4   | 0x23A| 0x23A | 0.0000|
| 7   | 0x70  | 0x7F  | 4   | 0x23A| 0x23A | 0.0000|
| 8   | 0x80  | 0x8F  | 4   | 0x23A| 0x23A | 0.0000|
| 9   | 0x90  | 0x9F  | 4   | 0x23A| 0x23A | 0.0000|
| 10  | 0xA0  | 0xAF  | 4   | 0x23A| 0x23A | 0.0000|
| 11  | 0xB0  | 0xBF  | 4   | 0x23A| 0x23A | 0.0000|
| 12  | 0xC0  | 0xCF  | 4   | 0x23A| 0x23A | 0.0000|
| 13  | 0xD0  | 0xF3  | 6   | 0x23A| 0x23C | 0.0020|
| 14  | 0xF4  | 0xFF  | 3   | 0x23C| 0x276 | 0.0566|
| 15  | 0xFC  | 0xFF  | 2   | 0x276| 0x3FF | 0.3838|
Every step the encoder receives a value to encode via the IN port. The encoder processes the symbol internally and produces the following outputs: 1) OFS_out: an up to 8b value containing the corresponding range offset and its 4b length OFS_r (range 0b-8b). 2) A 16b CODE_out contains CODE_c (4b+1b to indicate no output) useful bits that are to be written into the encoded symbol stream. The 5b OUT_u along with its 1b enable indicate whether we should include additional “underflow” bits (explained below) in the output and how many (count is the 5b portion). The bits are to be inserted after the most significant bit of CODE_out (and they set to its inverse).

The encoder comprises three blocks: “SYMBOL Lookup”, “PCNT Table”, and “Hi/Lo/CODE Gen”. Two 16b registers HI and LO maintain the current range (initialized to 0xFFFF and 0x0000 respectively). Encoding the input value IN starts in “SYMBOL Lookup” which identifies the symbol this value maps to. The block produces two outputs: 1) the output to the offset stream via OUT_out and OFS_r. 2) SYMi an 1-HOT encoded 16b vector indicating the table row (symbol index) the value mapped to. SYMi is fed into “PCNT Table” which determines which probability count range this symbol maps to. The output from “PCNT Table” is used by “Hi/Lo/CODE Gen” block to update the current code range and to produce any encode stream output bits. A 5b UBC register counts the number of underflow bits (explained below). Its value is fed into the block and is updated by the unit using UBCn signal.

**SYMBOL Lookup:** Figure 3b shows the structure of “SYMBOL Lookup”. The 8b IN value is compared against the maximum value (base[i] = R_{max} – 1) of all ranges using one comparator per row. Since the rows are ordered (ascending), the matching row is the last in order whose base is larger than the input value. This is used to generate the SYMi vector which in turns routes the corresponding base and offset length field (ob) to the components that generate the output offset. The offset is calculated as the difference between the 8b IN value and the matching base value and is trimmed via the “mask” block to ob bits. Processing proceeds to “PCNT Table”.

**PCNT Table:** As Figure 3c shows, the SYMi signals select the boundary counts cHI and cLO for the range assigned to the current symbol. For each symbol index, the unit holds a 10b probability count representing the maximum for the range (inclusive). This becomes cHI, and the cLO is taken from the register for the preceding row or 0 for row 0. The cHI and cLO values are then scaled (multiplied) with the current range (HI - LO + 1) producing sHI and sLo. Since range is a 16b number and cHI and cLO are 10b numbers, sHI and sLO need 26b. Since our max probability count is 2^{10} – 1 we can discard the 10 least significant bits effectively dividing with our max probability count (this converts the counts into probabilities). Accordingly, the multipliers can omit any parts that serve to produce only those 10 least significant bits. The resulting scaled 16b range boundaries, sHI and sLO, are then fed into “HI/LO/CODE Gen”.

**HI/LO/CODE Gen:** The final block, shown in Figure 3d, starts by calculating the new scaled range tHI and tLO given the newly encountered value. The incoming sHI and sLO values correspond are offset starting from 0. Adjusting this offset to LO producing tHI and tLO shifts this range in the appropriate position representing the sequence of previously seen symbols. The remaining logic: 1) determines if tHI and tLO have a common prefix which can be output, and 2) detects whether tHI and tLO are in danger of underflow. This implements arbitrary precision arithmetic while using fixed-point units. **Common Prefix Detection:** The XOR block produces a bit vector that identifies any bit positions that are different between tHI and tLO. The LD1 block then detects the leading position that there is a difference. Any preceeding bits can now be shifted out and written into the encoded symbol stream. This results in updated tHI’ and tLO’.

**Underflow Detection and Handling:** The APack encoder uses finite precision arithmetic to execute an algorithm that requires arbitrary precision arithmetic. To do so it effectively maintains a window of 16b into what are high and low range boundaries of arbitrary bit precision. The HI and LO registers contain these 16b windows and conceptually, HI and LO have suffixes comprising an “infinite” number of 1s and 0s respectively.

The 16b window are allowed to slide to less significant bits by shifting out any prefix bits that can no longer change. To understand why this works, observe that as arithmetic coding encodes one symbol after the other, the HI and LO boundaries shrink. HI always becomes smaller, while LO always grows larger. However, it should always be the case that HI > LO since each symbol encoded has a non-zero probability assigned to it. As HI and LO approach they will grow an increasingly longer
common prefix. Those are the bits that the encoder can safely “discard” by shifting them out of the HI and LO register while writing them on the encoded stream.

However, there are cases, where depending on the probability range of a new symbol, and the current range, having a window of just 16b is not enough to appropriately scale the range so that HI remains larger than LO. The case is where HI contains a value of the form 100... and LO a value of the form 011... which means that HI and LO are converging around 0.5. To eventually find out whether they will end up being both above 0.5 or below it, requires being able to perform arithmetic with more than 16b. This happens when the range adjustments done are small enough so they need to affect bits that are not yet within the current window and hence are not physically present. The encoder handles such cases preemptively by entering a state where it records how many underflow bits are needed allowing the window to slide. Accordingly, the encoder handles this by identifying, starting from the second most significant bit, any prefix of \( t_{HI}' \) and \( t_{LO}' \) where \( t_{LO} \) is all 0s and \( t_{HI} \) is all 1s. This subprefix is shifted away from \( t_{HI}' \) and \( t_{LO}' \). This results in \( t_{HI}'' \) and \( t_{LO}'' \). To detect the length of this subprefix, the encoder uses a leading 1 detector for \( t_{HI}' \) (ignoring the MSb) and a leading 0 for \( t_{LO}' \) (again ignoring the MSb). The subprefix is the most significant position among the two. This is implemented in the 01PREFIX block. Internally, this block uses a 2-input AND gate per bit position, with one input directly connected to \( t_{LO}' \) and the other connected after inversion (NOT) to \( t_{HI}' \). The output of those 15 ANDs goes into a leading 0 detector. The leading 0 position is where the subprefix, if any, ends.

This subprefix is removed from \( t_{LO}' \) and \( t_{HI}' \) producing \( t_{LO}'' \) and \( t_{HI}'' \). Its length of is added to the UBC register which counts the number of outstanding underflow bits. Those eventually will be set to the inverse of the most significant bit of HI (1s or 0s if we end up respectively on the upper or lower part of the range below or above 0.5).

**Final HI and LO generation:** After the common prefix and the underflow subprefix have been discarded, we need to adjust the final HI and LO values. First we need to insert a suffix of 1s in HI to make up for the fact that we shifted out several MSbs. Recall, that HI is meant to slide over a number that has a suffix of infinite 1s. In addition, we need to set the MSb of HI to 1 if we entered underflow bit mode. The final output are the nHI and nLO values which are loaded into the HI and LO registers respectively. Other ways of avoiding underflow in the HI and LO registers are possible. For example, the range may be expanded anytime it drops below half the maximum range.

### A. Decoder Implementation

Figure 4 shows the APack decoder which is very similar to the encoder albeit a bit simpler. The decoder has the same initialization ports as the encoder (instead of a “SYMBOL Lookup” unit the decoder has a “SYMBOL Gen” unit – however, internally these two units have an identical symbol table). During decoding, it accepts two input streams CODE_IN and OFS_in respectively for reading bits from the encoded symbol and the offset streams.

After initialization of the internal range, base, offset tables the decoder can start accepting the encoded symbol stream via CODE_IN. At each step/cycle, the decoder reads in a number of bits and notifies whichever unit supplies them of their number via the 5b CODE_r output. OFS_in is similarly an 8b input that the decoder uses to read in offset bits (most significant bit first). How many it needs to read is given by the output OFS_r which is 3b plus a 1b enable.

Figure 4a shows the internal organization of the encoder. There are four blocks: “SYMBOL Gen”, “PCNT Table”, “Hi/Lo/CODE Adj”, and “OFS Adj”. Two 16b registers HI and LO maintain the current range. These are initialized to 0xFFFF and 0x0000 respectively. The 16b CODE register reads in the encoded symbol stream, and the 8b OFS register is used to read in the offset stream.

Decoding a symbol is done by processing the current range boundary values HI and LO and CODE_IN in “PCNT_Table” (Figure 4b). This is done by detecting which (scaled according to the HI and LO) probability count range the current CODE_IN falls within. The results in identifying a symbol row index in
SYMi and two adjusted range boundary values adjHI and adjLO. SYMi is used by “SYMBOL Gen” (Figure 4c) to produce the original value consuming the corresponding offset from the offset stream. The decoded value appears on the OUT port. The “HI/LO/CODE block (Figure 4d) produces the new range boundary values, nHI and nLO, adjusts the CODE value, and potentially consumes bits from the encoded symbol stream. This mirrors the corresponding encoder process.

Summary: The coding/decoding units prove simple, lightweight, and area- and energy-efficient. Their tables have very few entries (here 16) containing narrow fixed-point values. They are not actively updated. The rest of the logic is combinatorial implementing narrow fixed-point operations (the most expensive being a 16b x 10b multiplication out of which we don’t need the lower 10b). The only updates done are to the HI, LO, CODE, and OFS registers which are short (16b).

B. Increasing Throughput

Processing neural networks places significant bandwidth demands on memory. The implementation described thus far can process only a single value per cycle. To meet the bandwidth demands of these workloads it is necessary to process multiple values per unit of time. This section describes two such methods: pipelining and replication.

1) Pipelining the Encoder and Decoder: The implementation described encodes and decodes one value at a time. The implementation can be pipelined to increase the operating frequency, and to decrease the number of units needed to achieve a desired throughput hence improving area costs and energy efficiency. For this purpose, the input tensor is partitioned into a number of subtensors each of which are to be encoded and decoded as independent streams. Some state elements of the encoder and decoder unit need to be replicated to support the pipelined processing of multiple such streams. All the streams can use the same probability count table, replicating the PCNT (HiCnt[i]) and the symbol generation and lookup tables (base[i] and ob[i] fields) is not necessary. However, a separate set of the OFS, CODE, HI, and LO registers is needed per stream. Partitioning the encoder and the decoder into pipeline stages can be done in multiple ways. First the PCNT lookup can be partitioned into a number of stages where in each only a range of table entries are considered. For example, the table lookup can be partitioned into two stages, where the first considers the first half of entries and the second stage considers the second half. If the first stage results in a match, the second stage can be optionally powered gated to reduce energy. Partitioning requires the introduction of temporary registers to hold the results produced at each stage. Adjusting the HI/LO/CODE can be another stage for the decoder, and generating the HI/LO/CODE can be another stage for the encoder. Similarly, the offset generation and offset extraction can be other stages operating.

2) Replication: Pipelining increases throughput since it reduces the amount of processing that occurs per cycle thus permitting a higher operating frequency. Further increases in throughput can be had through replication of the encoder and decoder. This requires further splitting the input tensor into several subtensors whose stream are to be encoded and decoded independently. Such splitting is desirable for other reasons as it is often used to take advantage of locality in the on-chip memory hierarchy. The number of units needed depends on the target application and the number of processing cores.

VI. APACK Table Generation

A method is proposed to generate the probability count table contents, such as those shown in Table I. Typically, for each layer of a model, the method is invoked twice to generate two separate tables, one for the activations and another for the weights. Since weights do not change a single pass over the weights is sufficient. Activations however depend on the input. Profiling proved effective since the overall distribution of activation values when viewed at the layer level does not change much with the input.

Informally, the table generation method initializes the table with values corresponding to a uniform value distribution and estimates the resulting footprint, that is the number of bits that would be needed to store the input tensor. The method used to estimate the footprint is described later on. It then iteratively adjusts the table entries attempting to find a better assignment. This process considers all possible configurations allowed by the search algorithm as long as this results in a reduction in footprint that is above some threshold. The preferred threshold is set to 1%. The method used is shown in Listing 1.

Without loss of generality this description assumes that the inputs are 8b values, however, the same process can be applied to input of any bit length. The process first inspects the input tensor and creates a histogram with $2^8$ buckets where each bucket $h(i)$ represents the number of times the corresponding value $i$ appears in the tensor. This is not shown in the listing. The process then starts by invoking the findPT() routine which accepts the histogram as input. The first step is to initialize the probability count table (PT) with a configuration where the range of possible values $[0, 2^8 - 1]$ is equally split among the table entries (line 38 in Listing 1). Function search() searches through candidate configurations and returns the best PT it found and its corresponding footprint. Line 43 decides whether the method will try to search for an even better configuration. This is done by testing the ratio of the newly found best footprint (newsize) over the previous best footprint (size). As long the improvement was above our 1% threshold, the method will proceed to another round. Search uses recursion whose depth is controlled by the depth parameter. As long as depth is less than a maximum allowed value DEPTH_MAX search() is allowed to call itself. A maximum depth of 2 was sufficient. The parameter “around” identifies the PT entry indexes which would search() try to adjust. If “around” is negative then search() is allowed to adjust all entries. The only case this occurs is when findPT() invokes search(). Otherwise, “around” is an index itself and search() will try to adjust only entries whose distance from “around” is at most within some threshold either below or above. A distance threshold of 1 proved sufficient. Calls to encoded_size() are used to estimate the compression.
Final Adjustment for Activations: When using profiling on

Generating the Probability Counts: (we use values as tuples of (value, distance) is limited to be up to 15 for a maximum overhead of 4-bit or non-zero, value for RLE and RLEZ respectively. The distance number of similar values, or zeros, until the next non-similar, 2) RLE and RLEZ: run length encoding techniques that encode line: that does not apply any compression to the off-chip traffic.

Compression Methods: We compare APack against: 1) Base-

Hardware and Energy Modeling: We attach 64 APack encoder/decoder engines to a dual-channel 8GB DDR4-3200 off-chip memory interface for evaluation. The energy consumption of the baseline off-chip memory accesses was modeled using Micron’s DRAM power model [43] along with the uncompressed data volume. For APack, the data was compressed using the profiling-based probability count tables then passed through the same DRAM power model while taking the overhead power consumption of APack engines into account. To model the area and power consumption of APack, the compression/decompression engines were implemented in Verilog, synthesized via the Synopsys Design Compiler and layout was produced via Cadence Innovus and for a 65nm TSMC technology which is the best that is available to us due to licensing restrictions. The power consumption overhead of the encoding/decoding engines was estimated by capturing

DNN models: We evaluate the effectiveness of APack over a set of (quantized to int 8 unless otherwise noted) DNN models spanning a wide range of applications including image classification, object detection, segmentation, and natural language processing. The models we evaluate are listed in Table II. The models were obtained directly from the respective sources and are used unmodified. Pruned versions of Alexnet and Googlenet allow us to study how APack interacts with pruned models [64]. From the Torchvision repository we use those models that have been pre-quantized to 8b fixed point [2]. From the IntelAI repository we similarly use only those models whose weights are quantized to 8b fixed-point [30]. ResNet18-PACT was quantized to 4b except for the first and last layers which remain in 8b using the PACT method of Choi et al. [12]. ResNet18-Q is pruned with the modified training method of BitPruning to arrive at per layer fixed-point precisions that never exceed 8b [46]. The “per-layer” quantized models were quantized further with the profiling-based quantization method of Nikolić et al. [47] which further trims precisions per layer.

Trace Collection: We run inference with the models out-of-the-box as released by their original authors on an NVIDIA GeForce RTX 3090 GPU. We use PyTorch and TensorFlow layer hooks that trigger upon executing each layer to dump its input weights and activations into numpy files. Since model parameters do not change while inference, a single trace dump for weights is enough per layer where the same trace is used to derive the probability count table and then compressed using the table. However, input activations are changing dynamically with every input image to the model. Thus, up to 9 input activation samples per layer are used to generate the probability tables. The IntelAI models, as provided, use floating-point activations. Hence we limit attention only to their weights.

VII. Evaluation

Compression Methods: We compare APack against: 1) Baseline: that does not apply any compression to the off-chip traffic. 2) RLE and RLEZ: run length encoding techniques that encode values as tuples of (value, distance) where distance is the number of similar values, or zeros, until the next non-similar, or non-zero, value for RLE and RLEZ respectively. The distance is limited to be up to 15 for a maximum overhead of 4-bit per tuple. 3) ShapeShifter [36]: a compression technique that, rather than using a fixed bit-width per value, groups the values in a predetermined group size G and dynamically detects the minimal precision P needed to represent the values in the group based on the actual range of values in the group. Then the group is represented with $(G \times P + \log_2 P_{\text{max}})$ bits where $P_{\text{max}}$ is the max precision supported per value. We evaluate a variant of ShapeShifter that is optimized for 8bit quantized models.
circuit activity using Mentor Graphics’ ModelSim which was then passed on to Innovus for post-layout simulation.

To compare with ShapeShifter we follow the same modeling flow where we model compression/decompression engines using the same technology node and design flow. We use a configuration optimized for 8-bit quantized models with a single Level-1 unit along with eight Level-2 units are used per off-chip DRAM channel [36].

A. Change in Memory Traffic

This section reports the change in off-chip memory traffic relative to the baseline (no compression) for APack, Shapeshifter (SS) [36], Run-Length Encoding (RLE), and Run-Length Encoding for Zeros (RLEZ) [10], [19], [39]. Figures 5b and 5a report the relative reduction in off-chip traffic for weights and activations respectively. The results demonstrate that APack is robust in that it always reduces traffic, it outperforms the other methods, and that the reductions in traffic depend on the quantization method used. Generally, the reduction is higher for activations than for weights except for when the models are pruned. The rest of this section discusses these results in more detail as the quantization method used by each model affects value distributions during inference.

TorchVision models: For model parameters, APack reduces traffic to as much 0.65 of the baseline for MobileNet v3 and to as little as 0.88 for ShuffleNet v2. Much higher reductions are observed with APack for activations: the highest reduction is to 0.41 of the baseline for for ResNext101 and the lowest is 0.55 for MobileNet v3. There are two reasons for the better compression of activations. First, activations show high sparsity, a well-known feature of neural networks that use the ReLU activation function which clips most non-firing neurons to zero.

Inspecting the weight distribution we found that while most values do cluster near zero or near the maximum, many of the intermediate values are present. When compared to the weight distribution of the other models that were quantized with different methods, this suggests that the lower bits tend to be noisy, a tell-tale sign that the quantization method used by TorchVision uses the full value range regardless of whether it is needed. A similar phenomenon was observed for the linear quantization used in earlier versions of Tensorflow [14].

Shapeshifter and the run-length-based method have a harder time coping with this noisy distribution. Shapeshifter manages to reduce traffic but less compared to APack. RLE and RLEZ result in increasing traffic for weights as repetition of values, be it zeros or otherwise, is rare. They do offer some reduction in traffic for activations. As expected, APack outperforms Shapeshifter and the other methods for weights and more so for activations. Shapeshifter groups values (we used a group of 8 values as in the original work which we verified that works best for these models too) and uses a container that is as larger as necessary to accommodate the largest magnitude value within the group. Encoding efficiency is lost for all other values having a lower magnitude. In contrast, APack treats each value independently and effectively uses as many bits, even a fractional number, to encode it as required by the value’s frequency of appearance.

IntelAI models: The IntelAI quantized models demonstrate that having a noisy weight distribution is not inherently necessary for weights. In general, compared to the TorchVision models, IntelAI’s quantization methods result in more skewed distributions for weights, a property that APack rewards resulting in pronounced compression benefits for weights compared to the TorchVision models. APack reduces traffic to as little as 0.59 of the baseline for SSD-Resnet34 and in the worst case to 0.86 for MobileNet v1 with most of the models observing a reduction to 0.6. Compared to ShapeShifter APack reduces traffic by 11% on average. The run-length-based methods still fail to improve memory footprints for the weights as these models are also not pruned.

Remaining models: For the remaining models and relative to ShapeShifter, APack compresses activations and weights by 1.34× and 1.51× respectively. The average reduction is higher for weights due to the highly sparse and skewed distribution of the model parameters, especially for AlexNet-Eyeriss, Googlenet_Eyeriss, and ResNet18_PACT. The results also demonstrate that APack benefits all quantization methods. For example, it reduces traffic even for ResNet18_PACT taking advantage of the skewed distribution of the 4b weights and much more than ShapeShifter does. The run-length-based methods have their best showing for the pruned models. Even for them, however, APack is nearly twice as effective.

B. Area, Power, and Energy

This section reports the energy savings that APack achieves with the compressed off-chip traffic to/from DRAM. We model the power consumption of a dual-channel 16GB DDR4−3200 off-chip memory via Micron’s DRAM power model [43] and use 64 APack compressors/decompressors.

Our layout-based measurements are that the 64 compression/decompression engines of APack need a total area of 1.14 mm² and consume a total power of 179.2 mW. This power consumption constitutes an 4.7% overhead vs. the power consumed by a dual-channel DDR4−3200 memory system when operating at 90% of its peak bandwidth.

Figure 6 shows the energy consumed by off-chip memory transfers normalized to the baseline that implements no compression technique. The estimates shown assume that the weights and input activations of each layer are read only once from off-chip [57]. This is the typical case for real-time “edge” inference accelerators where the whole DNN model cannot fit in on-chip memory and, thus, the parameters of each layer should be read from off-chip for each single input image passing through the model.

The energy savings vary across models according to the compression ratio achievable. For instance, for pruned models such as AlexNet-Eyeriss and GoogLeNet-Eyeriss where most of the model weights are zeros, APack capitalizes on the heavily skewed distribution and saves 91% and 72% of the off-chip access energy respectively. For models with less skewed distributions, such as NCF APack achieves lower compression
TABLE II: Neural network models studied.

| Network               | Dataset                | Application | Data Type | Quantizer |
|-----------------------|------------------------|-------------|-----------|-----------|
| GoogLeNet [59]        | ImageNet [55]          | Classification | int8     | Torchvision |
| Inception v3 [60]     | ImageNet               | Classification | int8     | Torchvision |
| Mobilenet v2 [56]     | ImageNet               | Classification | int8     | Torchvision |
| Mobilenet v3 [27]     | ImageNet               | Classification | int8     | Torchvision |
| Resnet18 [22]         | ImageNet               | Classification | int8     | Torchvision |
| Resnet50 [22]         | ImageNet               | Classification | int8     | Torchvision |
| Resnext101 [63]       | ImageNet               | Classification | int8     | Torchvision |
| Shufflenet v2 [42]    | ImageNet               | Classification | int8     | Torchvision |
| Inception v4 [58]     | ImageNet               | Classification | int8     | IntelAI   |
| Mobilenet v1 [28]     | ImageNet               | Classification | int8     | IntelAI   |
| Resnet101 [22]        | ImageNet               | Classification | int8     | IntelAI   |
| R-FCN Resnet101 [27]  | COCO [37]              | Object Detection | int8     | IntelAI   |
| SSD-Mobilenet [40], [51] | COCO               | Object Detection | int8     | MLPerf    |
| Wide & Deep [11]      | Kaggle Display Advertising Dataset [1] | Recommendation | int8     | IntelLabs Distiller |
| QSBERT [3], [15]      | MRPC [61]              | NLP         | int8     | IntelLabs Distiller |
| NCF [24], [66]        | ml-20m [21]            | Recommendation | int8     | IntelLabs Distiller+Per-Layer |
| ResNet18-PACT [12]    | ImageNet               | Classification | int8/Pruned | IntelLabs Distiller+Per-Layer |
| SSD-MobileNet [40], [51] | COCO               | Object Detection | int8     | IntelLabs Distiller+Per-Layer |
| MobileNet [28], [51]  | ImageNet               | Classification | int8     | MLPerf    |
| bilstm [62]           | CamVid [6]             | Segmentation | int8     | per-layer |
| SegNet [5]            | ImageNet               | Classification | int8     | per-layer |
| ResNet18-Q [23], [46] | ImageNet              | Classification | int8     | per-layer |
| AlexNet-Eyeriss [64]  | ImageNet               | Classification | int8     | per-layer |
| GoogLeNet-Eyeriss [64] | ImageNet              | Classification | int8     | per-layer |

![Fig. 5](image.png)

**Fig. 5:** Normalized off-chip traffic

Ratio (1.2×) and but still saves 13% of the off-chip energy consumption. The activation distributions are more heavily skewed. For example, the compression ratio for the activations for NCF is 2.2× leading to energy savings of 53%. Generally, the energy savings results track the achievable compression ratios thanks to the light power consumption overhead of the APack compressor/decompressor units.

Although ShapeShifter’s hardware and power costs are lower than APack’s, the higher compression with APack and given that off-chip accesses are so expensive in comparison to the compressors/decompressors result in superior overall energy with APack.

C. Overall Performance and Energy Efficiency

We measure end-to-end energy efficiency and speedup when APack is integrated with a Tensorcore-based accelerator. The accelerator is configured as shown in Table III. We evaluate both APack and ShapeShifter for off-chip compression and compare to the baseline accelerator that does not apply any off-chip compression technique. We obtained the Shapeshifter simulator from the original authors and modify its memory and processing energy modeling for consistent modeling of all configurations. We limit attention to the only those model traces that are compatible with this simulator. While overall APack achieves higher compression rates than ShapeShifter, for these models, as we have seen the advantage of APack is smaller. Accordingly, the performance and energy advantage of APack over ShapeShifter would have been higher if we were able to measure them across all previously studied models.

Figure 7 shows the speedup achieved when APack enhances the baseline accelerator. On average, APack speeds up the execution by 1.44× while ShapeShifter achieves a 1.3× speedup over the baseline. Both methods avoid stalls for off-chip transfers and enabling much better use of the accelerator’s compute units. This is especially true for models that tend to be memory-bound with low compute per byte ratio. For all these models, APack achieves better performance than ShapeShifter. For some, however, the execution time advantage of APack is minimal. These are models such as BERT and the pruned...
Alexnet and GoogleNet, that become completely compute bound. However, as we will see when we consider overall energy, APack has a significant edge over ShapeShifter for all models as it reduces off-chip traffic more.

Figure 8 shows that APack boosts the energy efficiency over the baseline accelerator for all the experimented models. The improvement varies per model according to the relative importance of the off-chip transfer energy vs. the on-chip compute energy. The higher the fraction of overall energy due to off-chip accesses the higher the potential and the benefits seen from APack. On average over all models, APack boosts energy efficiency by 1.37× outperforming ShapeShifter which achieves a 1.23× energy efficiency over the baseline.

VIII. RELATED WORK

The most closely related work to APack are compression methods that target deep learning inference. As commented in the introduction, these methods target specific value patterns such as zeros, or prefixes of 0s and 1s [7], [17], [20], [36], [52]. Bit-interleaving across several values [7] and precision trimming quantization [34], [46] has been used to amplify how often such patterns appear. APack differs in that it is not designed to target any specific value pattern whether that is for whole values or bits. It is designed to target any non-uniformity in the value distribution and for that could reward methods that amplify them.

The introduction has also commented on several other approaches that can boost model efficiency. As long the resulting model exhibits skewed value distributions, APack will complement such methods.

IX. CONCLUSION

APack is a simple to implement and effective off-chip compression method for neural networks that is plug-in compatible with many accelerators. We have demonstrated that it reduces off-chip traffic which significantly reduces energy consumed by expensive off-chip memory transfers. In addition, APack can accelerate memory-bound models by reducing the stalls related to off-chip data accesses. APack greatly boosts overall energy efficiency and proves superior to prior lossless memory compression techniques for deep learning.

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