Radiation-hard active CMOS pixel sensors for HL-LHC detector upgrades

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ABSTRACT: The luminosity of the Large Hadron Collider (LHC) will be increased during the Long Shutdown of 2022 and 2023 (LS3) in order to increase the sensitivity of its experiments. A completely new inner detector for the ATLAS experiment needs to be developed to withstand the extremely harsh environment of the upgraded, so-called High-Luminosity LHC (HL-LHC). High radiation hardness as well as granularity is mandatory to cope with the requirements in terms of radiation damage as well as particle occupancy.

A new silicon detector concept that uses commercial high voltage and/or high resistivity full complementary metal-oxide-semiconductor (CMOS) processes as active sensor for pixel and/or strip layers has risen high attention, because it potentially provides high radiation hardness and granularity and at the same time reduced price due to the commercial processing and possibly relaxed requirements for the hybridization technique. Results on the first prototypes characterized in a variety of laboratory as well as test beam environments are presented.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Detector design and construction technologies and materials; Instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons)
Several competitive pixel detector concepts are under research and development for the new ATLAS\textsuperscript{1} inner tracker needed for the Large Hadron Collider (LHC) run Phase-II. While for the innermost layers the occupancy and radiation environment is most challenging, the price as well as the production and testing rate of modules for the huge silicon area to cover is a key issue for the outer layers. One option probed with first encouraging results is the use of a commercial high voltage complementary metal-oxide-semiconductor (CMOS) technology for the sensors. Due to the full CMOS functionality, the sensor could integrate the full analog readout logic, such as a charge sensitive amplifier (CSA) and a discriminator. It could then take benefit of interconnection to a dedicated, purely digital readout chip. The use of such a readout chip would decouple the sensor technology from the readout chip technology and could result in an increased amount of digital functionality on the module and more electronic complexity. Figure 1 indicates the difference between the classical hybrid pixel detector concept, and the new concept under development taking benefit of the CMOS circuitries in the sensor layer. The possibility of analog as well as simple digital readout logic inside the sensor layer has the potential to relax the requirements of the interconnection technique. For example, if the first amplification stage and hit processing logic is implemented inside the sensor, the resulting signal is large enough to be capacitively coupled to the readout chip. Possibly the cost of the bump connection of current hybrid pixel detector concepts can be reduced, because the sensor can be glued to the readout chip. However, the loss of the readout-chip to sensor self alignment of the bump bonding technique is a limitation of the glue bonding. A significant improvement in placing precision is needed in comparison to bump-bonding. Additionally the uniformity of the glue layer thickness and thus the coupling strength between sensor and

\textsuperscript{1}A Toroidal LHC ApparatuS
Figure 1: Classification of hybrid pixel detector concepts. (a) The currently used technology using a passive sensor connected to a readout chip containing analog and digital readout functionality. (b) shows the concept using a purely digital readout chip, which is connected to a smart CMOS sensor containing the analog readout functionality.

The depleted CMOS technology for particle detection

The high voltage CMOS technology is an industrial development for the application of high voltage controls. It is commonly a multi-well structure on a relatively high resistivity p-doped substrate. The resistivity of the substrate is usually in the order of 10 $\Omega \text{cm}$, but can be up to several k$\Omega \text{cm}$. In the prototypes presented here, the entire CMOS electronics is implemented in the deep n-well. The PMOS\(^2\) transistors are implemented directly into the deep n-well, while the NMOS\(^3\) transistors sit in a p-well within the deep n-well. The electrical field caused by the high voltage increases the depth of the depletion zone into the substrate. The deep n-well is used as charge collecting electrode for particle detection. This is sketched in figure 2. In this configuration, the collecting electrode is the only charge attracting n-well and thus no charges are lost to insensitive n-wells. The drawback is a large pixel capacitance due to the large charge collecting electrode. Additionally, the potential of the deep n-well fluctuates with the collected charge. Therefore, precautions must be taken in the use of the PMOS transistors in the deep n-well. Within the depleted region the charge generated by ionizing particles is mainly collected by drift. This is the key feature which makes

\(^2\)p-channel metal-oxide-semiconductor field-effect transistor

\(^3\)n-channel metal-oxide-semiconductor field-effect transistor
Figure 2: Simplified cross section of a high voltage CMOS sensor for particle detection. PMOS transistors are implemented in the deep n-well. A p-well within the deep n-well provides shielded NMOS transistors. The p-doped contacts between the deep n-wells isolate the deep n-wells and are used as bias contacts to deplete the substrate. Charges generated by ionizing particles travelling through the substrate drift towards the n-well within the depletion zone and the deep n-well can be used as charge collecting electrode.

The results presented in this paper are obtained using the prototype called HV2FEI4, which is fabricated in the Austria Microsystems 180nm process. This process allows a bias voltage of the substrate as high as $-90\,\text{V}$. The depleted region depth is then expected to be approximately $15\,\mu\text{m}$. The HV2FEI4 holds a CSA and a discriminator. The HV2FEI4 is designed to fit the FE-I4 bump bond footprint, and thus in the investigated samples the sensor is flipped and glued to the FE-I4 readout chip. A picture of the resulting assembly is shown in figure 3a. The bump pads of the readout chip and the sensor form capacitors, as shown in figure 3b, and the discriminator output signal of the HV2FEI4 is transmitted using capacitive coupling to the preamplifier in the FE-I4 readout chip.

Although the HV2FEI4 is an early stage prototype, the sensor makes use of the configurability of the sensor and the possibilities provided by the implementation of logic into the sensor already. The pixel size of the HV2FEI4 is $33\,\mu\text{m} \times 125\,\mu\text{m}$. That is only a third of the FE-I4 pixel size. Six HV2FEI4 pixels are routed to two bump pads. Thus, six HV2FEI4 pixels are read out by two FE-I4 pixels in the same column. The connection scheme is illustrated in figure 3c. A HV2FEI4 unit cell holds two columns and three rows of pixels. The top left, bottom left and middle right pixel are connected to one FE-I4 pixel and the three other pixels are read out by the second FE-I4 pixel. The discriminator output signal amplitude is adjustable. The sub-FE-I4 pixel information can be decoded using different discriminator output amplitudes for the three sub-pixels connected to the same FE-I4 pixel. The FE-I4 measures the charge collected at its input in terms of time-over-threshold (TOT). Instead of measuring the collected charge, as it is the case for the present passive sensor readout, this information can be used to reconstruct the HV2FEI4 sub pixel using the adjustable output amplitude of the sensor. The granularity of the detector and thus its spacial res-
Figure 3: (a) A photo of a sensor glued to the FE-I4 readout chip and wire bonded to the test PCB. (b) The resulting pixel cross section of such a hybrid detector concept using capacitive signal transmission between the high voltage CMOS sensor and the readout chip. (c) shows the connection scheme of a sensor cell structure. Each cell consists of six pixels which are connected to two FE-I4 pixel cells (grey dashed lines) of 50µm × 250µm each.

Solution can be improved by this approach while keeping the number of readout channels constant. The drawback is a loss of the charge information which improves the spatial resolution to some extend with respect to the binary information and can additionally be used in detector operation as radiation damage monitor.

3 First results with HV2FEI4

The ATLAS CMOS pixel collaboration has previously shown on earlier prototypes the radiation tolerance of an Austria Microsystems high voltage CMOS technology to a non-ionizing energy loss (NIEL) fluence of \(10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}\) with proton irradiation and to \(10^{14} \text{n}_{\text{eq}} \text{cm}^{-2}\) with neutron irradiation. The total ionizing dose (TID) tolerance of the electronics is demonstrated up to 60 Mrad with x-ray irradiation [3].

The FE-I4 provides a fast OR signal of all pixel discriminator outputs. This signal is high if one or more FE-I4 pixels have recorded a hit above the discriminator threshold. The response of this signal called HitOR to charges in the sensor is shown in figure 4. The response to two fundamentally different charge sources is presented: charge injection using the injection capacitance in the sensor layer and charge generated by an ionizing particle.

In figure 4a the injection capacitance at the CSA input in the HV2FEI4 is used to issue a charge injection by the universal serial bus (USB) based test system, which is called USBpix. The injection signal of the USBpix system is shown in the middle. At the rising edge of the signal, the chopper circuitry on the support PCB generates a negative voltage step across the injection capacitance of each HV2FEI4 pixel. The bottom waveform is the CSA output of the test pixel. The top signal is the HitOR signal of the FE-I4 readout chip. The fact that the HitOR signal reacts in coincidence with the charge injection proves the functionality of the AC coupled signal transmission between HV2FEI4 and FE-I4.

The CSA of the test pixel also detects charges generated by electrons radiated by a \(^{90}\text{Sr}\) source (figure 4b). No charge injections are issued by the USBpix system, so the injection signal is constant. Again, the HitOR of the FE-I4 reacts in coincidence with the CSA of the HV2FEI4, so the
Figure 4: The HitOR signal of the FE-I4 readout chip (top waveform), the Strobe signal used to issue an injection (middle waveform) and the preamplifier output waveform of the HV2FEI4 operated with USBpix (bottom waveform). (a) The response of the HitOR signal to a charge injection issued in the sensor by the USBpix system as well as (b) by a particle originating from a radioactive source is shown.

Figure 5: Occupancy maps of the HV2FEI4 glued to an FE-I4 readout chip obtained with electrons from a $^{90}$Sr source. (a) The full FE-I4 map with entries in the HV2FEI4 position and (b) a zoom into the region of the HV2FEI4.

hybrid assembly using a HV2FEI4 sensor glued to a FE-I4 detects ionizing particles with capacitive coupling between sensor and readout chip.

Five million hits are collected in a source scan with a beta source ($^{90}$Sr). The discriminator output amplitude is set equal for all three HV2FEI4 sub-pixels coupled to the same FE-I4 pixel. Hits are recorded by the FE-I4 in the pixels covered by the HV2FEI4 sensor (figure 5a). A zoom
Figure 6: (a) The color coded mean TOT per FE-I4 pixel in the area covered by the HV2FEI4 and (b) the mean TOT projection along the columns.

into the area of interest shows, that the HV2FEI4 is uniformly illuminated except for two columns. The lower efficiency of these two columns is due to the pixel output being simultaneously connected to a test output, what can be disabled in the sensor configuration. The HV2FEI4 pixels read out by the FE-I4 pixels in the two missing rows are implemented differently from the rest and are very noisy. Therefore the two rows of the FE-I4 pixels are masked. Also the two pixels which record no hits are masked during the scan.

The TOT information of the FE-I4 is not correlated to the charge collected in the HV2FEI4. It depends on the discriminator output pulse height of the HV3FEI4 and thus can be used to get a sub-pixel resolution once the FE-I4 is appropriately tuned. Additionally, the recorded TOT is influenced by the coupling capacitance. As the plate size of the capacitors formed by the bump pads of the two chips is fixed, the coupling capacitance is mainly influenced by the thickness of the glue layer and the alignment of the chips. The calculated mean TOT per pixel presented in figure 6a reveals a geographical dependency. The projection of the mean TOT along the columns decreases linearly with a slope of $-0.53$ (25 ns)/column (figure 6b). A very likely explanation is a slight tilt between the sensor and the readout chip. The distance between the capacitor plates increases from left to right and the capacitance decreases. The coupling strength is reduced, which results in a smaller signal recorded by the FE-I4.

The hit detection time distribution within the sensitive time window of 16 times 25 ns is given in figure 7a. The FE-I4 HitOR signal is used in the scan to issue a trigger. The timing between the HitOR positive edge, which is in coincidence with the hit detection, and the trigger sent to the FE-I4 is fixed. No entries are expected in any other bin than four and five. A long tail after these is observed. This originates from hits detected in the readout chip after the hit issuing the trigger. Small hits close to big hits are expected to be detected late due to the time-walk effect. In a CSA + discriminator readout chain two effects modulate the hit detection time as a function of the input charge: Due to the finite preamplifier rise-time the time needed by the preamplifier to achieve the
full signal height depends (amongst others) on the input signal size itself. Additionally, the signal dependent propagation delay of the discriminator while switching adds to the time-walk. With the HV2FEI4 as sensor, the two time-walk sources are present twice: in the preamplifier and the discriminator of the sensor and of the readout chip.

The present algorithm in the USBpix test system clusters the FE-I4 pixel information. A significant amount of multi-pixel clusters is expected to be generated by the traversing electrons from a beta source. Multi hit clusters are expected especially with the small pixel size of the HV2FEI4 pixels and the connection scheme with neighboring HV2FEI4 pixels that are connected to neighbor pixels in the FE-I4 (figure 3c). The cluster size decreases exponentially and cluster sizes up to eleven pixels are recorded, see figure 7b.

4 Sub-FE-I4 pixel resolution

To prove that the sub-FE-I4 pixel resolution is achievable, the discriminator output amplitude is scanned individually for the three sub-pixels while performing test charge injections into the HV2FEI4. The TOT response of a single FE-I4 pixel is measured. The mean of the resulting TOT distribution is given in figure 8a as a function of the discriminator output amplitude (set by the digital to analog converter VNOut) for all three sub-pixels connected to this FE-I4 pixel. The root mean square (RMS) of the TOT histograms is displayed as a band. A discriminator output amplitude can be selected from these data for each sub-pixel so that the mean and RMS of the three sub-pixels do not overlap. The TOT spectrum as measured by the FE-I4 when injecting into the HV2FEI4 with these settings is shown in figure 8b. Three distinct TOT peaks appear and the sub-pixel can be reconstructed from the TOT information of the FE-I4.

5 Test beam results

Results from two test beam campaigns are presented here. A bias voltage scan has been performed on a sample irradiated to $1 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$ using the DESY test beam, see figure 9a. The expected

\footnote{Deutsches Elektronen-Synchrotron}
Figure 8: (a) The TOT response of a single FE-I4 pixel as a function of the discriminator output amplitude of the HV2FEI4 and the three sub-pixels within the HV2FEI4. (b) The TOT spectrum measured by the FE-I4 with a dedicated output amplitude setting for each of the three sub-pixels.

Figure 9: (a) The charged particle detection efficiency as a function of bias voltage of a sample neutron irradiated to $1 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$. The high threshold setting and suboptimal tuning of the sample reduces the efficiency in this particular measurement. (b) The efficiency map of an unirradiated sample with improved threshold settings.

increase of the particle detection efficiency with increasing bias voltage is observed. Very likely the threshold of the sample has been set too high to achieve higher efficiency in this measurement. This is addressed in recent test beam campaigns at CERN.\footnote{Conseil Européen pour la Recherche Nucléaire.} Figure 9b shows an efficiency map obtained at the CERN PS.\footnote{Proton Synchrotron.} The sample was not irradiated and shows a mean efficiency in the order of 97% at a bias voltage of $-80\text{V}$. A different analog readout chain is prototyped in the pixels connected to the four lowest rows in FE-I4. The settings for these pixels have not been adjusted during the measurement and thus they result in a lower efficiency.

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\footnote{Conseil Européen pour la Recherche Nucléaire.}
\footnote{Proton Synchrotron.}
6 Edge TCT measurements

The transient current technique (TCT) is widely used to study radiation damage in silicon detectors. In this technique, an electrical signal is induced using short laser pulses. The use of an infrared laser provides the possibility to generate the charges significantly deep inside the silicon volume due to the absorption depth above $>1\text{mm}$ at $-20^\circ\text{C}$. Typically the laser is shot from the top or back side into the silicon volume. In the case of the edge TCT measurements the laser is shot from the side and therefore the depth of the signal generation can be defined [4]. A sketch of the used setup in the CERN PH-DT group is shown in figure 10a [5]. The precision is limited by the focus width of the laser (here $9\mu\text{m}$).

A passive diode is connected to a dedicated external fast amplifier and data is then acquired with an oscilloscope. Two contributions of the signal can be differentiated when the output signal of the fast amplifier is plotted separately when generating the charges inside and outside the depleted region, see figure 10b. A fast signal ($\leq3\text{ns}$) originating from electrons drifting towards the charge collecting electrode within the depleted region, and a slower signal, which originates from diffusion current in the undepleted region, are observed. Plotting the signal size separately for the fast and slow signal as a function of the laser position reveals the position and shape of the depleted region. This measurement was performed on an unirradiated sample with a $100\mu\text{m}$ wide passive diode, see figure 11. As expected from the resistivity, depleted region is about $15\mu\text{m}$ thick at $-60\text{V}$ of bias voltage (figure 11a). It is surrounded by a roughly $20\mu\text{m}$ wide region contributing to the signal by diffusion, see figure 11b. Measurements on irradiated samples will follow.\footnote{Private Communication, Data obtained in the PH-DT SSD lab at CERN by Marcos Fernandez Garcia, Christian Gallrapp, Michael Moll, Daniel Muenstermann and Constantin Weisser.}
Figure 11: Signal size maps of the edge TCT measurements on an unirradiated passive diode in HVC莫斯 technology. (a) Only the fast signal contribution is plotted in a map of the charge generation position. This visualizes the shape of the depleted region. (b) The slow signal size is plotted to demonstrate the area contributing to the signal by diffusion current.

7 Summary

High voltage and high resistivity CMOS technologies are promising candidates for the outer layers of the planned ATLAS pixel detector upgrade for the LHC run Phase-II. The fabrication in an industrial process and the connection of the sensor and the readout chip without the costly chip-to-chip bump-bonding process reduces the cost. Albeit the characterization of the HV2FEI4 assemblies is in an early stage, the AC coupled signal transmission between the sensor and the readout chip, the detection of ionizing particles, as well as the reachability of a sub-pixel resolution using the TOT information of the readout chip could be demonstrated. Furthermore, the detection of minimum ionizing particles is demonstrated in test beam campaigns. A detection efficiency in the order of 97% could be demonstrated and is expected to increase using lower threshold settings. In edge TCT measurements the signal constituents of drift and diffusion current are observed. The R&D effort continues with increased attention as the technology promises to deliver high particle detection efficiency in HL-LHC environment.

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