Error Correction for NOR Memory Devices with Exponentially Distributed Read Noise

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Abstract—The scaling of high density NOR Flash memory devices with multi level cell (MLC) hits the reliability break wall because of relatively high intrinsic bit error rate (IBER). The chip maker companies offer two solutions to meet the output bit error rate (OBER) specification: either partial coverage with error correction code (ECC) or data storage in single level cell (SLC) with significant increase of the die cost. The NOR flash memory allows to write information in small portions, therefore the full error protection becomes costly due to high required redundancy, e.g. ∼50%. This is very different from the NAND flash memory writing at once large chunks of information; NAND ECC requires just ∼10% redundancy. This paper gives an analysis of a novel error protection scheme applicable to NOR storage of one byte. The method does not require any redundant cells, but assumes 5th program level. The information is mapped to states in the 4-dimensional space separated by the minimal Manhattan distance equal to 2. This code preserves the information capacity: one byte occupies four memory cells. We demonstrate the OBER ∼ IBER$^{3/2}$ scaling law, where IBER is calculated for the 4-level MLC memory. As an example, the 4-level MLC with IBER ∼ $10^{-9}$, which is unacceptable for high density products, can be converted to OBER ∼ $10^{-12}$. We assume that the IBER is determined by the exponentially distributed read noise. This is the case for NOR Flash memory devices, since the exponential tails are typical for the random telegraph signal (RTS) noise and for most of the charge loss, charge gain, and charge sharing data losses.

Index Terms—NOR Flash memory, Error Correction, Manhattan metrics, Soft Sensing

I. INTRODUCTION

The Flash memory devices store information in array of memory cells, with every cell (memory transistor) programmed to a certain level (value) of the threshold voltage $V_t$. The modern technology offers two types of the Flash memory devices: NOR and NAND. The NAND memory operates by large chunks of data stored with density $\sim 10^{11}$ bit/cm$^2$ and relatively high IBER $\sim 10^{-2}$. The NOR memory allows WRITE/READ of a single bit/byte; the data is stored with density $\sim 10^{10}$ bit/cm$^2$ and relatively low IBER $\sim 10^{-9}$. The state of the art error correction codes (ECC) were developed for NAND memories, see e.g. [1]-[4]. These codes are capable to repair multiple errors and reduce the OBER to $\sim 10^{-14}$. The modern ECCs are not applicable to the NOR Flash memory devices, because the efficiency of the ECC increases with amount of the data written at once [2], [5] which is above Kbyte for NAND. However, amount of the data written at once is single bit/byte for NOR. For example, the Hamming code correction of a single error in 4 cells storing 1 byte (2 bits/cell) requires 2 more redundant cells and 50% die size increase. Stringent requirements to OBER limit the scaling of the NOR Flash memory devices: die size gain due to scaling of the cell size is wasted for accommodation of redundant cells.

Angelo Visconti patented the idea of adding redundant program levels to the NOR Flash memory cell along with applying an error correction code [6]. In particular, he proposed to map the data to alphabet of size 5, write to 5 levels per cell, and protect the information by the relevant Hamming code. For example, 64 bits of the data are written into 28 cells, then 4 redundant cells allow correcting an error in any of 32 cells. This method preserves the density of 2 bits/cell, however it requires the WRITE operation of at least 8 bytes at once.

The READ error in Flash memory device occurs because of the overlap of $V_t$ distributions between neighbor program levels. The IBER $\sim 10^{-10}$ in NOR Flash memory devices means that the overlap is weak, and the IBER is determined by the tail of the $V_t$ distribution. The effect of trapping and de-trapping of charges is responsible for an exponential shape of these tails [7]. The exponential shape of the $V_t$ distribution is typical for RTS noise, cycling effects on charge retention [8], and cell interference [9]. The slope of the exponential distribution depends on many factors including channel doping [10], the memory usage model, etc. This is quite opposite to the NAND, where IBER is high and the Gaussian $V_t$ distribution is adequate.

This paper considers an alternative approach to error correction in the NOR Flash memory devices. The idea is to add program levels similarly to [6], however to encode the information by maximizing the minimum Manhattan distance [11]. The Manhattan metrics is optimal for systems with exponential noise, because the error probability becomes the exponential function of the Manhattan distance between neighbor states. The method is closely related to non-binary coding in the Lee metrics [12]-[14]. Recent developments in polyomino (cross-polytopes) tiling make the idea attractive for Flash memory design [15]-[17].

Below we present a calculation of the gain of storage reliability of eight bits in a system having 4 memory cells. As the reference we take the system with 4 program levels (two bits per cell, $B_0 = 2$). The additional 5th program level will increase the information capacity of the system to $\log_2(5) = 2.3$ bits per cell. Let the word $x_1 \ldots x_4$, where $x_j \in \{0, 1, 2, 3, 4\}$, describe the state of the Flash memory system; the $j$-th cell is programmed to $x_j$-th program level. The coding of the information with minimum Manhattan
Fig. 1. The threshold voltage distribution of the ensemble of four-level Flash memory devices as programmed (a) and as read (b). The origin of the read $V_t$ exponential tails in (b) is the random telegraph signal noise of the read current; these tails can also come from the charge loss, charge gain or charge sharing due to defects in the dielectric layers of the memory device.

distance equal two \( L \) \( x_1 + x_2 + x_3 + x_4 = 0 \mod 2 \) \( (1) \) will reduce the information capacity to \( B = (1/4) \log_2 (5^4 + 1/2) = 2.07 > B_0 = 2 \). \( (2) \)

Therefore, the modified system with 5 levels per cell and non-binary coding will have enough information capacity to store 8 bits in 4 cells.

The read of information from the \( j \)-th Flash memory cell is done by comparison of the device threshold voltage with the reference value stored in the reference memory cell and determination of \( \tilde{x}_j \). With high probability the parity is satisfied \( \tilde{x}_1 + \tilde{x}_2 + \tilde{x}_3 + \tilde{x}_4 = 0 \mod 2 \), and the READ is correct; otherwise there is an error and soft sensing \( \text{[I8]} \) for error correction is required. The periphery circuit measures the threshold voltages of all 4 cells and searches for nearest (in Manhattan distance) word satisfying (1). The probability of wrong error correction is of the same order as the probability of two errors, see calculations in Sec. \( \text{[II]} \). Therefore, the logarithm of the inverse OBER can be increased as much as 50% by adding the 5th program level to the 4-level memory cell. As an example, the 4-level MLC with IBER \( \sim 10^{-9} \), which is unacceptable for high density products, can be converted to OBER \( \sim 10^{-12} \), see Table \( \text{[II]} \).

II. THE BIT ERROR RATE OF AN UNPROTECTED SYSTEM

Observe \( N \) memory cells in a given memory device. Then program these \( N \) memory cells to predefined threshold voltage levels \( \{L_0, \ldots, L_3\} \) see Fig. \( \text{[II]} \; (a) \). The program state \( A' \) of memory system is

\[ A' = \{V_1', \ldots, V_N'\} \, , \] \( (3) \)

where the threshold voltage \( V_j' \) of the \( j \)-th memory cell is uniformly distributed around \( x_j \)-th program level \( L_{x_j} \),

\[ f_p(V) = \begin{cases} \frac{1}{W}, & L_x - W/2 < V < L_x + W/2 \\ 0, & \text{otherwise} \end{cases} \] \( (4) \)

The width \( W \) of the program distribution is typically a function of the program speed. Faster programming leads to the wider program distribution and larger \( W \).

The READ operation of the Flash memory device cannot reproduce exactly the state \( A \). The state is distorted by the read noise (typically the RTS of the read current) and by the data retention issues, see Fig. \( \text{[II]} \; (b) \). The periphery circuit reads the state

\[ A = \{V_1, \ldots, V_N\} \] \( (5) \)

of the memory system. The distribution of the threshold voltage \( V_j \) acquires the exponential tail

\[ f_R(V) = \begin{cases} (1 - T)/W, & L_x - W/2 < V < L_x + W/2 \\ aT e^{-2a(V - L_x - W/2)}, & V > L_x + W/2 \\ aT e^{-2a(L_x - W/2 - V)}, & V < L_x - W/2 \end{cases} \] \( (6) \)

where \( T \) is the fraction of the cells in the tail, and \( 1/2a \) is the slope of the distribution.

The READ operation is simply comparison of the threshold voltage of the memory cell with the the threshold voltages of
the reference cells. The threshold voltages of the reference cells is positioned in the middle of the level-to-level spacing. The READ operation finds values of the word \( \{x_j\} \) from \( \{V_j\} \)

\[
x_j = \text{Round} \left( \frac{V_j - L_0}{\Delta_0 + W} \right),
\]

where rounding is performed to the nearest integer.

The threshold voltage of the reference cells, the values associated with the threshold voltages are found more than \((\Delta + W)/2\) away from \(L_x\), then the parity check will pass, and the error will not be detected. The probability of this error and the corresponding OBER are

\[
P_0^i = T^2 e^{-20\Delta},
\]
\[
E_0^i = \frac{3}{8} T^2 e^{-20\Delta}.
\]

If the threshold voltage of \(j\)-th cell moves more than \((2\Delta + W)/2\) away from \(L_{x_j}\), then the error correction algorithm will converge to \(y_j = x_j \pm 2\), see Fig. 2(b). The probability of this error and the corresponding OBER are

\[
P_1^2 = T e^{-2\Delta - aW},
\]
\[
E_1^2 = \frac{1}{2} T e^{-2\Delta - aW}.
\]

The third type of error occurs when

\[
\exists j \neq k \quad y_j = x_j + 1, \quad y_k = x_k - 1.
\]

In terms of the read threshold voltages the condition for the error is

\[
|V_j - L_{x_j+1}| + |V_k - L_{x_k-1}| < |V_j - L_{x_j}| + |V_k - L_{x_k}|,
\]

which is derived from (11). In the relevant range

\[
L_{x_j} < V_j < L_{x_j+1}, \quad L_{x_k-1} < V_k < L_{x_k},
\]

it becomes simplified to

\[
L_{x_j+1} - V_j < L_{x_k} - V_k.
\]

The probability of this event is better expressed in terms of the deviation variables \(\varepsilon_j = |V_j - L_{x_j} - W/2|\) and \(\varepsilon_k = |V_k - L_{x_k} - W/2|\),

\[
P_2^i = a^2 T^2 \int_0^\Delta d\varepsilon_j \int_{-\varepsilon_j}^{\Delta - \varepsilon_j} d\varepsilon_k e^{-2a\varepsilon_j - 2a\varepsilon_k}
\]

\[
\approx \frac{1}{2} a \Delta T^2 e^{-2a\Delta}.
\]

The sum over pairs of cells and the normalization per number of stored bits gives

\[
E_2^i = \frac{1}{NB_0} \sum_{k \neq j} P_2^i = \frac{3}{4} a \Delta T^2 e^{-2a\Delta}.
\]

The total BER of five level design with non-binary ECC becomes

\[
E_2 = E_0^i + E_1^i + E_2^i
\]

\[
= \frac{3}{4} T^2 \left( a\Delta + \frac{1}{2} \right) e^{-2a\Delta} + \frac{1}{2} T e^{-2a\Delta - aW}.
\]

This must be compared with the probability \(E_0\) of the error in the 4-level system given by (9). Assuming that the 5th level was added without pushing out \(L_0\) and \(L_3\), as in Figs. 12 we get the condition

\[
4\Delta = 3\Delta_0 - W.
\]

The generic scaling law for the OBER is (assume \(W \ll \Delta_0\))

\[
E_2 \sim e^{-2a\Delta} \sim e^{-(3/2)a\Delta_0} \sim E_0^{3/2}.
\]
TABLE I

| $e^{-a\Delta_0}$ | $T$ | $E_0$ | $E_2$ | $E_2/E_0$ |
|------------------|-----|-------|-------|-----------|
| 1.E-02           | 1.E-03 | 5.E-06 | 7.E-08 | 1.E-02    |
| 1.E-02           | 1.E-05 | 5.E-08 | 5.E-10 | 1.E-02    |
| 1.E-02           | 1.E-07 | 5.E-10 | 5.E-12 | 1.E-02    |
| 1.E-02           | 1.E-09 | 5.E-12 | 5.E-14 | 1.E-02    |
| 1.E-03           | 1.E-03 | 5.E-07 | 3.E-09 | 7.E-03    |
| 1.E-03           | 1.E-05 | 5.E-09 | 5.E-12 | 1.E-03    |
| 1.E-03           | 1.E-07 | 5.E-11 | 5.E-14 | 1.E-03    |
| 1.E-03           | 1.E-09 | 5.E-13 | 5.E-16 | 1.E-03    |
| 1.E-04           | 1.E-03 | 5.E-08 | 4.E-10 | 7.E-03    |
| 1.E-04           | 1.E-05 | 5.E-10 | 5.E-14 | 2.E-04    |
| 1.E-04           | 1.E-07 | 5.E-12 | 5.E-16 | 1.E-04    |
| 1.E-04           | 1.E-09 | 5.E-14 | 5.E-18 | 1.E-04    |

IV. PRACTICAL EXAMPLES.

It is quite common in high reliability NOR Flash memory devices to have very low fraction of cells suffering from the data retention issues, $T \sim 1E-6$, $T \ll e^{-aW}$ in this case

$$E_2 \approx E_2^{ii} = \frac{1}{2} T e^{-(3/2)a\Delta_0-(1/2)aW} = e^{-a\Delta_0-2-aW/2} E_0$$

(25)

The other possibility is to have relatively narrow program distributions for better read window, $e^{-aW} \ll T$:

$$E_2 \approx E_2^{iii} = \frac{3}{2} a \Delta_0 - aW - \frac{1}{4} T e^{-a(\Delta_0-W)/2} E_0 .$$

(26)

In (25), (26) the spacing $\Delta$ of 5-level system is expressed in terms of $\Delta_0$ and $W$ by making use of (23).

The proposed method yields a substantial gain in OBER for practical applications, see Table 1. For estimation purpose we put $W \sim \Delta_0$ and the OBER/IBER ratio becomes

$$E_2/E_0 \approx e^{-a\Delta_0} + \frac{3}{4} a\Delta_0 T ,$$

(27)

and use this formula for typical values of $T$ and $e^{-a\Delta_0}$. The 5-level non-binary coding allows to reduce the OBER by 2-4 orders of magnitude. This method allows the technology progress from gigabit NOR parts to tenth gigabit products.

The one-byte non-binary ECC discussed in this paper can be combined with global ECC coverage in cases where the data is streamed in many bytes.

For the systems with purely exponential read noise, $W = 0$, $T = 1$, the scaling law (21) becomes accurate and can be used for OBER calculation. In this case the $E_0 \sim 10^{-15}$ is reduced to $E_2 \sim 10^{-15}$.

For the applications with the relatively high IBER, the 5-level method does not gain enough OBER. The reliability improvement can be achieved by using more complicated parity rules [11] with higher Manhattan distance [12] and more levels per cell. For example, the minimum Manhattan distance equal 3 can be achieved by packing the cross-polytopes of the radius 1. For the system of 4 memory cells, the volume of the 4-dimensional cross-polytope is 9. Therefore, the 7 levels per cell are required to preserve the information capacity of the system $(1/4) \log_2(7^4/9) = 2.014 > 2$.

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