Review of Charge Pump Topologies for Micro Energy Harvesting Systems

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Abstract: This paper reviews CMOS based charge pump topologies used within autonomous embedded micro-systems. These charge pump structures have evolved from its simplistic diode-tied, single-branches with major threshold drops to exponential type, dual-branches with sophisticated gate and substrate control for lower voltage operation. Published charge pumps are grouped based on architecture, operation principles and pump optimization techniques with their pros and cons compared and results contrasted. The various charge pump topologies and schemes used are considered based on pumping efficiency, power efficiency, charge transferability, circuit complexity, pumping capacitors, form factor and minimum supply voltages with an optimum load. This article concludes with an overview of suitable techniques and recommendations that will aid a designer in selecting the most suitable charge pump topology especially for low ambient micro energy harvesting applications.

Keywords: Charge Pump (CP), Low Voltage (LV), Energy Harvesting

Introduction

Next generation self-powered micro devices such as medical implants dictate the need for small, safe and renewable alternatives for battery replacement. Therefore, energy can be autonomously harvested from a patient without the need of future replacement such as the cochlear implant reported in (Bandypadhyay, 2013). When scavenging these ambient energies, there is an inevitable discontinuity, typically mitigated by use of hybrid harvesters (Shi et al., 2011; Bandypadhyay and Chandrakasan, 2012; Lim et al., 2013; Tan, 2013; Lim et al., 2014; Yeo et al., 2016). There is also a need to resolve the cold start issue for an inherently small (low voltage) harvester input. While off-the-shelf harvesters such as Photovoltaic (PV) cells (SANYO, 2008) and Piezoelectric (PZT) harvesters (MIDE, 2013) have voltages above the CMOS voltage threshold, \( V_{TH} \), Thermoelectric Generator (TEG) harvesters (CUI, 2012) generally fall in the mV range as low as 26 mV (Lim et al., 2014) at \( \Delta T = 1K \) when CUI Peltier device is modelled upon. Therefore, efforts to kick-start CMOS based power management circuits for low voltage harvesters ranges from providing an external bias (Carlson et al., 2010; Kim and Kim, 2013; Ahmed and Mukhopadhyay, 2014), mechanical MEMs switch (Ramadass and Chandrakasan, 2010), charge pump based (Chen et al., 2011; Shih and Otis, 2011; Chen et al., 2012a; Liu et al., 2012; Bender et al., 2014; Peng et al., 2014), transformer based (Im et al., 2012; Teh and Mok, 2014; Zhang et al., 2014), oscillator based (Sun and Wu, 2010; Ahmed and Mukhopadhyay, 2014; Bender et al., 2014), one time wireless charging scheme (Bandypadhyay, 2013) to a fully electrical multi-stage start-up mechanism (Chen et al., 2012b; Weng et al., 2013; Bender et al., 2014). Although these start-up scheme can push input voltage boundaries down to as low as 20 mV, they are either based on large inductors (Weng et al., 2013) and transformers (Ahmed and Mukhopadhyay, 2014; Bender et al., 2014; Teh and Mok, 2014; Zhang et al., 2014) or off-chip components (Carlson et al., 2010; Ramadass and Chandrakasan, 2010; Kim and Kim, 2013) which limits how small the system can be. To overcome the aforementioned issues, only the Charge Pump (CP) topologies will be studied in this review due to its many benefits. These benefits include the possibility of full integration, lower form factor and its simplistic pumping mechanism.

Previously published review article on CP circuits (Palumbo and Pappalardo, 2009) had a strong focus on design strategies and basic CP topologies. There were no mention of Low Voltage (LV) strategies and schemes for
the recent lower supply voltage trend of micro energy harvesting systems. Therefore, this paper aims to provide a chronological summary of various CP topologies from the very first CP design up to the more recent structures with gate and substrate control techniques that tend towards LV operations. These CPs are contrasted based on standard CP design metrics including charge transferability, circuit complexity, pumping capacitors, form factor, minimum voltage supply, pumping and power efficiency.

This paper is arranged according to increasing functionality and complexity of CP structures and their control schemes. Hence, the second section provides a comprehensive overview of various CP architectures, techniques employed, tradeoffs and feasibility of LV operations with Table 2 summarizing critical performance metrics of contemporary CP structures. The third section concludes this paper with CP research trends, challenges and recommendations of CP structures suitable for specific design criteria especially in micro energy harvesting applications.

**Past Charge Pump Topologies: Overview**

Charge pumps are voltage multipliers which ideally operate in two non-overlapping clock phases. A charge pump usually requires an inverted switching signal to control both clock phases. Therefore, an oscillator is usually used to provide two out-of-phase signals in CP start-up circuits. Here, we will be focusing on the comparative study of over twenty different CP topologies and its feasibility of providing LV start-up for applications suffering from low ambient input signals below the CMOS threshold. Each of the following CPs generally addresses several improvements from their predecessor as given in the following sub-sections.

**Classical Charge Pumps**

The classical Cockcroft-Walton CP was originally meant for high voltage application. It has an output voltage, $V_{OUT} = N\cdot V_{IN}$ for $N$ number of stages given as $V_{OUT} = 2N\cdot V_{DROP}$ where $V_{DROP}$ is the output voltage drop and $V_{IN}$ the peak input voltage (Pan and Samaddar, 2010). Although Cockcroft-Walton CPs are still in use for particle acceleration and X-ray tubes, the architecture is below the CMOS threshold. Each of the following CPs generally addresses several improvements from their predecessor as given in the following sub-sections.

**Series-Parallel Charge Pump**

The Series-Parallel CP (Fig. 2a) employs the concept of series charge (P1, P2, P4, P5 “ON”) and parallel discharge (P3 and P6 “ON”) when gate voltages from anti-phase clock toggles the MOS switches “ON/OFF”. This CP has an $N^{TH}$ stage output given by (Pan and Samaddar, 2010) as $V_{OUT} = (N+1)\cdot V_{IN} \cdot \left[ C_{PUMP}(C_{PAR} + C_{OUT}) \right] \cdot \left( \frac{1}{V_{TH}} \right)$. It was implemented as a non-linear CP and employed as auxiliary step-up switch capacitor for voltage multiplications (Luo, 2009; Luo and Ye, 2009; Hart, 2011; Kang et al., 2014) but in (Luo and Ye, 2010), the Series-Parallel CPs were considered unpopular due to their discrete implementation (Lee et al., 2014). Recently, some literatures ventured into this structure (Geng and Ma, 2013; Perez-Nicoli et al., 2015; Vaisband et al., 2015), where efficient control of gate voltages (Perez-Nicoli et al., 2015) reduces $V_{TH}$ drops present in MOS diodes. The major drawback of this CP includes the $C_{PAR}$ associated with the three extra switches/stage which affects performance and the $V_{OUT}$ which strongly decreases with stage number (Luo and Ye, 2010).
Bootstrap Charge Pump

Bootstrap CP eliminates $V_{TH}$ drops in MOS by increasing NMOS’s $V_{GS}$ to $> V_{DD} + V_{TH}$ via a bootstrap capacitor, $C_{bt}$. This facilitates higher charge transfer for subsequent stages. This concept of augmenting internal node voltages > $V_{DD}$ has been demonstrated in Flash memories (Umezawa et al., 1992; Atsumi et al., 1994). The Bootstrap CP (Fig. 2b) has an additional MOS device and $C_{bt}$ per stage compared to the Dickson CP. This $V_{TH}$ cancelation scheme requires four clock phases annotated as F1, FB1, F2, FB2 in Fig. 2b with corresponding clock control signals shown in Fig. 3. The resultant $V_{OUT}$ of an $N$-stage Bootstrap CP is given by:

$$V_{OUT} = V_{IN} + N \left( \frac{C_{PUMP}}{C_{PUMP} + C_{PAR}} \right) V_{th} - \frac{I_{OUT}}{(C_{PUMP} + C_{PAR})f_{CLK}}$$

(2)

where, $V_{IN}$ and $V_{CLK}$ are the input and pump clock voltages respectively. From Equation 2, several advantages of bootstrapping can be surmised, firstly, the $V_{TH}$ term is eliminated thereby reducing $V_{DROP}$ as much as $NV_{TH}$ achieves better gain and enhance conversion efficiency, seemingly having better output efficiency compared to latch-based CPs (Allasasmeh and Gregori, 2011), a higher clock frequency can also be achieved with this four phase CP due to a smaller $RC$ delay as shown by the Bootstrap CP equivalent resistance of $R_s = N/(C_{PUMP} + C_{PAR})f_{CLK}$. Hence, lower $RC$ delay enhances charge transfers compared to two-phase CPs. However, the Bootstrap topology suffers extra routing/area penalty and larger $C_{PAR}$ due to $C_{bt}$. Also, complex clocking control strategies and gate-biasing (Yeo et al., 2015) circuitries are necessary due to its four-phase clock and $>V_{DD} + V_{TH}$ clock amplitude requirement.

Fig. 1. Two stage Dickson charge pump

Fig. 2. Single branch charge pumps (a) series-parallel (Perez-Nicoli et al., 2014) (b) bootstrap (Pan and Samaddar, 2010)

Fig. 3. Bootstrap charge pump clock control signals (Luo and Ye, 2010)
**Charge Transfer Switches Charge Pump**

Static Charge Transfer Switches (CTS) charge pumps were firstly introduced by Wu and Chang (1998). The Static CTS uses dynamic feedback to improve charge transfers, gain and performance by steering charge flow from later stages of higher potentials to current stages for dynamic $V_{TH}$ cancelation. This suits LV operation. Wu and Chang (1998) Static CTS have the top half structure identical to a Dickson CP and the extra bottom structure for $V_{TH}$ cancelation (Fig. 4a). This Static CTS suffers from reverse charge sharing which reduces pumping gain due to partially off switches. This phenomenon can be eliminated by the Dynamic CTS topology also proposed in (Wu and Chang, 1998) with two extra MOS diodes per stage (Fig. 4b). The extra PMOS and NMOS controls gate voltages and better shut down Static CTS switches. However, the final diode-connected stage still suffers from $V_{TH}$ losses due to body effect (Pan and Samaddar, 2010). The Dynamic CTS has a $V_{OUT}$ expressed as:

\[
V_{OUT} = V_{IN} + N \left( \frac{C_{PUMP}}{C_{PUMP} + C_{PAR}} \right) - V_{TH}
\]

where Equation 3 eliminates the $(N-1)V_{TH}$ term in Equation 1. However, the $C_{PAR}$ is much greater in this Dynamic CTS compared to Bootstrap CP which adds only an extra MOS and $C_{bt}$ for $V_{TH}$ cancelation. Hence, considering the area drawback, Dynamic CTS might not have an edge over Bootstrap CPs. Peng *et al.* (2014) describe a few losses in Dynamic CTS contributed by redistribution, conduction, reverse charge sharing losses on top of the final stage $V_{TH}$ drop. Later, Su *et al.* (2005) reported a Linear CP design which improved on the Dynamic CTS structure by introducing methodical gate controls to further increase pumping efficiency. As shown in Fig. 4c, PMOS were replaced by PMOS to reduce charge sharing due to the latter’s lower charge mobility and its less impact on the absolute $V_{TH}$.

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![Fig. 4. Various CTS charge pumps (a) Static CTS (Wu and Chang, 1998) (b) Dynamic CTS (Wu and Chang, 1998) (c) Linear CTS (Su *et al.*, 2005)](image_url)
Therefore, widening PMOS reduces conduction loss (Maksimovic and Dhar, 1999) by lowering $R_{EQ}$. There is also an efficient turn-on of last stage by disregarding the use of MOS diodes as in (Wu and Chang, 1998). However, if $V_{DD} < V_{TH}$, the Linear CP yet again cannot turn on/off the switches effectively.

**Dual-Branch Charge Pump**

The generic Dual-Branch CP is shown in Fig. 5a while the bootstrap version for $V_{TH}$ cancelation is shown in Fig. 5b. These dual-branch structures were introduced to lower ripples in the CTS design (Kleveland, 2002; New et al., 2012) and later evolved into latch-based designs (Nakagome et al., 1991; Gariboldi and Pulvirenti, 1994; 1996; Favrat et al., 1998; Pelliconi et al., 2003; Ker et al., 2006; Che et al., 2009; Chen et al., 2010; Ulaganathan et al., 2012; Peng et al., 2014; Kim et al., 2015) which are currently gaining popularity. These structures have $V_{OUT}$ similar to Equation 1 but with reduced charge transfer intervals of $T/2$ (Palumbo and Pappalardo, 2010), circuit minimization with smaller $C_{PUMP}$ values and half the ripple, $V_{R}$ compared to single branch CPs where $V_{R}$ is expressed as $V_{R} = I_{OUT}T/(2(C_{OUT}+C_{PUMP}))$ (Pan and Samaddar, 2010) assuming $C_{OUT} \gg C_{PUMP}$. The aforementioned advantages translate to $V_{DROP}$ reduction, higher switching frequencies and the possibility of LV start-up. Although, ripples associated to noise that affects loads such as memory can be reduced by increasing $C_{LOAD}$ and $f_{CLK}$, these strategies adversely lengthen ramp-up time and reduces pump efficiency respectively. Since Dual-Branch CPs are still not suited for LV operation and cold-start circuits, they were later evolved into cross-coupled structures with body biasing (Peng et al., 2014; Kim et al., 2015) and dynamic gate controls (Su et al., 2005) to complement LV operations.

**Cross-Coupled Charge Pump**

The Cross-Coupled CPs were originally proposed in (Gariboldi and Pulvirenti, 1994; 1996) and later implemented as a four stage cascaded version in Ker et al. (2006) CP design. The Cross-Coupled topologies are realized with cross-coupled switches driven by anti-phase clocks for boosted voltages. They are essentially latch-configured inverters with $V_{OUT}$ similar to the Dual-Branch CPs. These dual compensated structures introduce many benefits akin to the dual-branch structures. Not only does it improve pumping efficiency and reduces ripples as reported in (New et al., 2012), these CPs enhances charge transferability and requires smaller devices, i.e., half the original $C_{PUMP}$ size, which in turn reduces effect of device sizes on $V_{TH}$ (Peng et al., 2014). Moreover, redistribution loss is also reduced as the branches complements charge transfer to the output node, ensuring load voltage stability. Since this Cross-Coupled CP normally fails to work below $V_{TH}$, several schemes were introduced to mitigate this. The following
elaborates some evolved structures since the classical latched CP design in (Gariboldi and Pulvirenti, 1994) beginning with Ker et al. (2006) structure to the most recent of developments. Ker et al. (2006) CP (Fig. 6a) has intertwining anti-phase clock signals on two branches with source-connected NMOS bulks to eliminate body effects while Che et al. (2009) design uses only PMOS for this purpose. These structures with two latch-based branches eliminate $V_{TH}$ drops, inherent to classic CPs (Dickson, 1976; Wu and Chang, 1998) for an almost full charge transfer between stages. With reduced reverse charge sharing compared to the Dynamic CTS, they are still not suited for LV applications especially when $V_{IN}$ is a few hundred mV below $V_{TH}$, inapt at effectively turning on MOS switches.

Recently, Peng et al. (2014) (Fig. 6b) improved on Ker et al. (2006) design where body biasing and backward control was reported in (Peng et al., 2014). This scheme enables complete turn on/off of the MOS transistors. Therefore, switching losses and reverse charge sharing were reduced. Body-biasing and the sub-threshold regime were included to enable LV operation. Although Peng et al. (2014) two branch CP (2014) solved most of Ker et al. (2006) design with a good efficiency of 89%, swift 0.1ms pumping speed, high capacitive drivability and charge transferability, its reported minimum start-up voltage is still high at 320 mV with a rather complex scheme requiring interleaved inverters and extra stages at the end. Moreover, such body-biasing will cause leakages if not well controlled. An alternative was Nakagome et al. (1991) circuit (Fig. 7a) which utilizes cross-coupled NMOS cells to obtain lifted voltage levels where differential outputs of the cells are coupled to form a single output using dual series-connected PMOS load switches (Nakagome et al., 1991). This would avoid large $V_{DROP}$. However, Nakagome et al. (1991) Cross-Load CP suffers from low conduction due to gate drive capabilities of PMOS load switches and no gains from series switches when $V_{IN}<V_{TH}$ or when $V_{OUT}$ is minute due to heavy loads (Kim et al., 2015). Recently, literatures in (Favrat et al., 1998; Chen et al., 2010; Ulaganathan et al., 2012; Kim et al., 2015) provide improved versions of this Cross-Load CP (Nakagome et al., 1991) to enhance these constraints associated to LV start-up operations.

Fig. 6. Cross-coupled charge pumps (a) classic latched based (Ker et al., 2006) (b) Peng et al. (2014) variation
To resolve lower conduction levels of the Cross-Load CP (Nakagome et al., 1991; Favrat et al., 1998) proposed a Bulk-Switching CP (Fig. 7b) with better switch conductance due to a level shifter gate signal control but this Bulk-Switching fails at low voltages due to backward current via series switches (Kim et al., 2015). Conventionally, both Cross-Load (Nakagome et al., 1991) and Bulk-Switching (Favrat et al., 1998) CPs have their PMOS's/NMOS's bulk biased to the highest/lowest potential. This ensures parasitic diodes inherent to MOS devices are reverse-biased to avoid leakages in off-state NMOS as well as degradation of PMOS voltage swing at the output node. Although the Cross-Load and Bulk-Switching CPs have low leakages, they suffer low on-
current, $I_{ON}$. The low cross in Cross-Load CP is also unresolved in the Bulk-Switching CP due to weakly off switches. Hence, increasing (decreasing) NMOS’s (PMOS) body bias reduces $V_{TH}$ to facilitate lower turn-on voltages such as the Forward-Body-Bias (FBB) CP proposed by (Chen et al., 2010; Peng et al., 2014).

The FBB CP uses higher inter-stage voltages borrowed from future stages to reduce $V_{TH}$ of NMOS while PMOS is biased to the lowest ground potential (Fig. 7c). Thus, all MOS devices are forward biased at all times during both “ON” and “OFF” states. This leads to both high current transfer and high body leakages when MOS devices are not conducting. This increases Voltage Conversion Efficiency (VCE) but reduces Power Conversion Efficiency (PCE). To resolve this issue, the Dynamic-Body-Biasing (DBB) CP was proposed by Kim et al. (2015) recently (Fig. 7d) with consideration of dead-time limitations, conduction loss and Meindl limit (Meindl and Davis, 2000). The DBB CP maintains a high on current during “ON” states and at the same time reduce leakages during “OFF” states by dynamically switching MOS devices into low $V_{TH}$ (forward-biased) and high $V_{TH}$ (reverse-biased) devices on demand, widely known as the Variable Threshold CMOS technique (VTCMOS) (Kang et al., 2014). The low $V_{TH}$ enables LV operation and faster speed whereas higher $V_{TH}$ reduces sub-threshold leakages and enhances efficiency. While the DDB CP in (Kim et al., 2015) have benefits such as low processing cost, low start-up voltages at 150 mV, high efficiency of 72.5% at $V_{IN}$ = 450 mV and reduced leakages while maintaining high on current which promotes LV applications, the structure suffers from additional DDB control circuitry, usages of 6×10 nF off-chip capacitors and still a lower 34% pumping efficiency at low voltages (180 mV). On the other hand, Bandyopadhyay et al. (2014) proposed an ultra low power CP similar to Fig. 7b with a gate driver that reduces leakages based on Favrat et al. (1998) voltage doublers model.

### Adiabatic Charge Pump

Adiabatic CP uses adiabatic switching to lower power consumption. It employs energy recycling by rerouting charge transfer paths back to the source/load rather than discharging to ground potential. Literatures in (Lauterbach et al., 2000; Keung et al., 2007; Ulaganathan et al., 2012) used adiabatic switching to reduce power usage. Lauterbach et al. (2000) uses dual-step adiabatic switching, charge sharing and a simple clocking technique that two-folds power efficiency. Keung et al. (2007) uses this concept on highly parallel datapaths in DSPs by recycling charge with an Adiabatic CP, moving slower adiabatic components away from critical paths. This successfully reduced energy consumption by 18% with a 1-2% area penalty.

Recently, switching losses linking to CTS gate control is reduced in (Ulaganathan et al., 2012) by using adiabatic switching scheme on the CTS structure (Fig. 8a). The Adiabatic CP has its $V_{OUT}$ similar to Equation 2 albeit with a lower energy dissipation where $E_{CP} = QV_{DD}$ and $E_{a} = 3/4QV_{DD}$ represents energy dissipation of conventional one-step and multi-step adiabatic charging respectively (Lauterbach et al., 2000). Adiabatic schemes focus on lowering power consumption by an almost zero energy exchange with the environment in the expense of slower charging time, additional circuitry such as transmission gates as well as the need of a pulsed voltage source (Kang et al., 2014) for stepwise charging.

### Mixed Structure Charge Pump

Mixed Structure CP such as those reported in (Hsieh et al., 2009; Huang et al., 2010) employs more than one type of CP structure per stage (Fig. 8b). These literatures combines CTS and Cross-Coupled CP to address both reverse charge sharing (Huang et al., 2010) and the final stage $V_{TH}$ drop with better pumping gain compared to traditional CTS structures (Wu and Chang, 1998). The Mixed Structure CP in (Huang et al., 2010), however, improves the original mixed structure in (Hsieh et al., 2009) by using multi-phase technique to enhance pumping and power efficiency. The penalties of such hybrid structures are generally the larger form factor and more complicated control schemes. These structures produce a $V_{OUT}$ similar to the CTS as expressed in Equation 3 indicated by (Hsieh et al., 2009).

### Adaptive Charge Pump

Adaptive CP ranges from CPs that changes its voltage conversion ratios (Zhang and Lee, 2010; Beck and Singer, 2011; Vaisband et al., 2015) or stage number (Tanzawa et al., 2002) on demand to reconfigurable CPs that modifies itself to maximize current in linear mode or switches to Fibonacci mode for LV operations such as the Adaptive CP structure proposed in (Gupta et al., 2013), sleep-active mode CP transitions in (Alioto et al., 2013) as well as topological modifications from Heap, Exponential to Fibonacci in (Allasasmeh and Gregori, 2011). Figure 8c shows an Adaptive CP (Palumbo and Pappalardo, 2010) that enables one to three stage number modifications by dividing total capacitance, $C_{TOT}$ with a suitable number of $C_{PUMP}$ assigned by MOS switches and driven by appropriate phase inputs. These phases, F1 through F6 with its corresponding complementary signals ($F_X$ and $F_N$) are shown in Fig. 9 (Palumbo and Pappalardo, 2010). The merits of Adaptive CP is its flexibility and that it dynamically lowers power consumption when usage level or purpose changes. However, the Adaptive CPs constitute a larger area and are more complex in their configurations and switching schemes compared to their non-adaptive counter parts.
Fig. 8. Special purpose charge pumps (a) Adiabatic (Ulaganathan et al., 2012) (b) Mixed Structure (Hsieh et al., 2009) (c) Adaptive (Palumbo and Pappalardo, 2010)

Fig. 9. Input/complimentary signals of adaptive CP (Palumbo and Pappalardo, 2010)
Single Clock Charge Pump

Single Clock CP were introduced in (Ansari et al., 2011) and enhanced in (Mondal and Paily, 2013). While previously discussed CPs uses more than one clock, the Single Clock CP needs no extra circuitry to ensure non-overlap of a second clock. As (Ansari et al., 2011) feeds low supply voltages to each stage (Fig. 10a), (Mondal and Paily, 2013) enhances $V_{OUT}$ by feeding only the first stage with supply voltages and subsequent stages with internally boosted voltages from later stages (Fig. 10b). Thus, the $V_{OUT}$, transferable charge, $Q_N$ and $I_{OUT}$ for both $N$-stage conventional and enhanced-voltage Single Clock CP is summarized in (Mondal and Paily, 2013). While Mondal and Paily (2013) enhances $V_{OUT}$ up to 9 and 18% as compared to the Dickson and Conventional Single Clock structure (Ansari et al., 2011), it suffers from poor charge sharing time compared to both structures.

Miscellaneous Charge Pumps

Miscellaneous CPs are shown in Fig. 11 and 12 representing Ladder CP (Bender, 1994; Seeman and Sanders, 2008; Bazzini et al., 2012), Fibonacci CP (Ueno et al., 1991; Makowski and Maksimovic, 1995; Seeman and Sanders, 2008; Allasasmeh and Gregori, 2011; Gupta et al., 2013), Exponential CP (Cernea et al., 2009; Allasasmeh and Gregori, 2011) and a recently patented Tree Topology CP (Lu et al., 2010; Roy et al., 2014) respectively. As stated in (Seeman and Sanders, 2008), Series Parallel CP performs better in a capacitor limited process with impedance inversely proportional to frequency while the Dickson and Ladder CP (Fig. 11a) works best in a switch limited process (Seeman and Sanders, 2008) with frequency-independent constant current flow. Hence, the CPs either uses switches or capacitors efficiently, but not simultaneously superior in both asymptotes (Seeman and Sanders, 2008). Recently, Bazzini et al. (2012) proposes an all PMOS Double Ladder CP which lowers output resistance, $R_{OUT,OPT} = (N(N+1))^{1/2}/(N\times C_{TOT})$ Compared to Pelliconi et al. (2003) design with the $i$-stage pumping capacitor, $C_{PUMP} = (N+1-i)/(N(N+1)C_{TOT}$ (Bazzini et al., 2012) chosen to minimize $R_{OUT}$ (Makowski and Maksimovic, 1995). While this enhanced structure has a high VCE at 93%, it still suffers a low PCE at 52%.

A two-stage Fibonacci CP (Fig. 11b) has reasonable switch and capacitor efficiency as reported in (Seeman and Sanders, 2008). The Fibonacci structure also has good current drivability in LV ranges (Gupta et al., 2013), low ripples and a good pump-up ratio (Ueno et al., 1991) due to its non-linearity and exponential nature. Fibonacci CP’s operation as explained in (Allasasmeh and Gregori, 2009) has the same gain with Dickson CP albeit having fewer capacitances. Also, it has a Fibonacci sequence as its per-stage voltage ratio giving $V_{OUT,FCP} = G\times C_{OUT} R_{OUT}$ where $G$ is the Fibonacci CP’s ideal voltage gain, $G = F_{N+1}/F_N$ is the $N$-th Fibonacci number and $C_i$ is the $i$-th $C_{PUMP}$ value. From Table 1, $R_{OUT}$ has more significant stage growth in Dickson CP compared to Fibonacci CP. Hence, the Fibonacci structure has lower conduction losses given by $P_R = I_{OUT}^2 R_{OUT}$ leading to better energy efficiency than the Dickson structure (Allasasmeh and Gregori, 2009) for $G > 3$. There are however no difference in $R_{OUT}$ between them for $G \leq 3$ or $N \leq 2$. Unlike Dickson CPs, $C_{PUMP}$ in Fibonacci CPs are not equally sized in all stages. For optimal performance, the $N$-th stage Fibonacci CP requires the largest capacitor nearest to $V_{IN}$ and the smallest capacitor to be closest to the load.

Fig. 10. Single clock charge pumps (a) conventional (Ansari et al., 2011) (b) enhanced output voltage (Mondal and Paily, 2013)
Exponential CPs have voltage gain exponentially associated to their pumping stages (Chang and Hu, 2004; 2006; Gobbi et al., 2007; Seeman and Sanders, 2008). Fibonacci CPs (Ueno et al., 1991; Allasasmeh and Gregori, 2011; Gupta et al., 2013) and voltage doublers (Seeman and Sanders, 2008) are categorized as exponential or non-linear CPs. Figure 12a shows an Exponential CP applied to a Flash memory (Cernea et al., 2009) with reduced area and 50% lower internal impedances for the same pumping capabilities of past topologies. Chang and Hu (2006) proposed their Exponential CPs (Fig. 12b) to reduce CP stages with the same achievable gain considering per-stage $V_{TH}$ drop in MOS switches. The exponential structure in (Chang and Hu, 2004; 2006) also suppresses $V_{TH}$ problems by having a larger clock voltage growth rate as compared to $V_{TH}$ drop rate (Chang and Hu, 2004). This solves the voltage saturation issue due to augmented $V_{TH}$ and lower $V_{OUT}$ in linear structures (Chang and Hu, 2006). Suitable $W/L$ ratios are selected for better gain and voltage transferability by having a proportional decrease in transistor sizes from input to the load stage (Chang and Hu, 2004). Later, (Shao et al., 2006) improved $V_{OUT}$ boosting by area as summarized by Gobbi et al. (2007) in Table 1 where even though Exponential CPs have the best gain at the same area, it suffers from a dramatic increase in $R_{OUT}$. Gobbi et al. (2007) compared Chang and Hu (2006) Exponential CP to the Fibonacci and Dickson CP in terms of gain, $R_{OUT}$ and pump-up speed. Moreover, a larger voltage loss can be seen with Exponential CP’s $V_{OUT}$ expression given by $V_{OUT \text{ (ECP)}} = GY_{IN} - \Delta V_{OUT} = 2^N V_{IN} - I_{OUT} R_{OUT}$.

Finally, the patented TTCP (Fig. 12c) resolves the charge transfer capability of linear CPs which is subjected to degradation when used with LV energy transducers by coupling more than one stage of the CP to the energy harvesting source (Lu et al., 2010; Roy et al., 2014). On the other hand, a Negative Charge Pump (NCP) can provide negative output voltages with similar configurations to a basic Dickson CP only to be replaced by a ground voltage at the input terminal (Pan and Samaddar, 2010). Table 2 summarizes the results for CMOS based CPs extracted from research papers in the past eight years. These CPs are compared based on their CMOS feature size, topology, clock frequency, minimum supply ranges, load current/load capacitor sizes, pumping capacitor sizes, VCE and PCE respectively. Generally, VCE is given as the actual output voltage over the ideal pumped-up voltage ($V_{OUT}/V_{IDEAL}$) given by $\eta_V = (V_{OUT}/(N+1)) V_{DD}$ for linear CPs (Palumbo and Pappalardo, 2010) while PCE is a measure of power extraction efficiency from source to the load given by $\eta_P = (I_{OUT} V_{OUT}/I_{CON} V_{DD})$. From Table 2, it can be noted that throughout the years from 2008 to 2016, researchers have successfully pushed start-up voltage levels from 1.5 V (Su and Ma, 2008) all the way down to 40 mV in Ashraf and Masuomi (2016) simplistic FBB based Dickson structure with a demerit of slow ~8s start-up time. These recent CP topologies have advanced towards body-biasing (Zhang and Lee, 2013; Peng et al., 2014; Kim et al., 2015; Ashraf and Masuomi, 2016) and gate controls (Shih and Otis, 2011; Zhang and Lee, 2013) for VCE enhancements of ~86% (180 mV) in Kim et al. (2015) structure and ~93% (350 mV) in Shih and Otis (2011) Bootstrap CP design.
Fig. 12. Miscellaneous charge pump topologies: (a) Exponential (Cernea et al., 2009) (b) exponential-gain structure (Chang and Hu, 2006) (c) Tree-topology (Lu et al., 2010; Roy et al., 2014)

Table 1. Comparison of voltage gain, output resistance and silicon area between N-stage charge pump topologies (Gobbi et al., 2007)

|                  | ECP       | FCP       | DCP       |
|------------------|-----------|-----------|-----------|
| Voltage Gain, G  | \(2^N\)   | \(F_{N+1}\) | \(N+1\)   |
| Output Resistance, R\text{OUT} | \(2^N \sum_{i=1}^{N} (2^{-i})^2 / fC\) | \((FxF_{N+1}) / fC\) | \(N/fC\) |
| Silicon Area     | 2N(C/2)/C | NC/C_0    | NC/C_0    |

In a nutshell, current CP design trends tend towards the lower power spectrum with prominence given to \(V_{TH}\) cancellation schemes, RC delay reduction and raising of on/off current ratio (DBB schemes) when considering CP design metrics trade-offs in LV operations.
Table 2. Contemporary charge pump topologies: A performance comparison

| Authors (Year) | CP Topology | Minimum supply, \(V_{IN}\) | Clock Frequency, \(f_{CLK}\) | Pumping Capacitors, \(C_{PUMP}\) | Load/Load Capacitor, \(I_{LOAD}/C_{LOAD}\) | VCE (PCE) | Process technology (CMOS) | Advantages | Disadvantages |
|---------------|-------------|-----------------------------|-----------------------------|--------------------------------|--------------------------------|-------------|--------------------------|-------------|---------------|
| Ashraf and Masoumi (2016) | Dickson with FBB (5×20-stages/1) | 40 mV | 1 kHz | N/A | \(C_{LOAD} = 5 \text{ pF}\) (CP output) | 53.88%@40 mV (N/A) | 180-nm | Lowest \(V_{OUT}\), Simplest FBB | Slow pre-startup at ~8s, Large no. of MOSFETs approach |
| Kim et al. (2015) | Cross-coupled with DBH (3-stages) | 150 mV | 250 kHz (off-chip) | 10 nF @ \(V_{IN} = 0.18\text{V}\) | \(I_{LOAD} = 2.1 \text{uA}\) (for \(V_{OUT} = 0.5\text{V}\)) | 85.97%@0.18 V (34%@0.18V) (72.5%@0.45V) | 130-nm | Low \(V_{IN}\), Highest \(I_{LOAD}\), High Efficiency Balances good PCE and VCE | Off-chip capacitors, Extra complexity for clocking & dynamic bulk-biasing |
| Peng et al. (2014) | Cross-coupled body-biased & backward control (6-stages) | 320 mV | 450 kHz | 24pF @12 (on-chip) | \(C_{LOAD} = 50.7 \text{ pF}\) | 89% @ 0.32V (N/A) | 180-nm | Swift pumping rate at 0.1 ms, Good VCE, Reduce leakages with body-biasing for PMOS only | Rather complex scheme requiring interleaved inverters and extra stages at the end |
| Zhang and Lee (2013) | Dickson based gain-enhanced dynamic gate & substrate control (4-stages/1) | 900 mV | 7 MHz | 20 pF @4 (on-chip) | \(C_{LOAD} = 40 \text{ pF}\) (on-chip) @ \(V_{OUT} = 1.4\text{V}\) (for \(V_{IN} = 5\text{V}\) | 84.62%@1.4V (43%@1.4V) | 350-nm | No \(V_{OUT}\) drop, No body-effect, No floating substrate terminals/ lower \(R_{ON}\) | High \(V_{OUT}\) |
| Chen et al. (2012a) | Dickson based dual mode [startup/operation mode] (10-stages/1) | 120 mV | 1 MHz (startup) 20 MHz (operation) | 28.6 pF @20 (on-chip) | \(I_{LOAD} = 75\text{uA}\) @ \(V_{IN} = 0.18\text{V}\) (extrapolation) (for \(V_{OUT} = 0.5\text{V}\)| 58.33% @0.12V (38.8%@0.12V) | 65-nm | High PCE, Low \(V_{OUT}\), No external excitation | Low \(I_{LOAD}\), High process cost |
| Shih and Ortis (2011) | Bootstrap (3-stages/1) | 270 mV | 800 kHz | 25 pF @6 (on-chip) | \(C_{LOAD} = 500 \text{pF}\) @ \(V_{IN} = 0.45\text{V}\) (for \(V_{OUT} = 0.5\text{V}\) | 92.86% @ 0.35V (56%@0.45V) | 130-nm | Fully integrated, Low process cost | Requires 4 clock phases Low \(I_{LOAD}\) |
| Chen et al. (2010) | Cross-couple (3-stages/2) | 180 mV | 10MHz | 12.3 pF @6 (on-chip) 0.4 pF @2 (off-chip) | \(C_{LOAD} = 12.3 \text{ pF}\) | 83.33% @0.18V (N/A) | 65-nm | Low \(V_{OUT}\), Low efficiency | Low \(I_{LOAD}\) |
| Hsieh et al. (2009) | Static Mixed Structure [CTS + Latched] (4-stage/1) | 1.5 V | 1 MHz | 0.1 pF @5 (off-chip) | \(I_{LOAD} = 500 \text{uA}\) @ \(V_{IN} = 1.5\text{V}\) (for \(V_{OUT} = 7.5\text{V}\)) | 99.31% @ 1.5V (100%@1.5V) | 350-nm | High VCE, Very high \(V_{OUT}\), Off-chip \(C_{LOAD}\) | Requires 4 clock phases |
| Su and Ma (2008) | 4-Phase Cross-coupled (2-stages/2) | N/A | 4 MHz | 0.5 mF @8 (on-chip) | \(R_{LOAD} = 1.8 \text{k}\Omega\) | N/A (92.01%) | 180-nm | Good PCE, Low \(V_{IN}\) and low \(P_{D}\), \(1/4\) sized CMOS and \(C_{LOAD}\), (Reduced reversion and conduction losses) | Requires 4 clock phases |

Discussions and Concluding Remarks

This review article presents a variety of CP topologies within the field of LV energy harvesting. These CP topologies are evolving away from discrete, diode-connected, linear-gain, external start-up structures to the more advanced sub-threshold, cross-coupled, exponential-type and self-start-up structures. Table 2 summarizes these contemporary CP design trends in the past eight years where gate and substrate control schemes gains substantial attention in low voltage CP design strategies.

In LV energy harvesting applications, the interaction between harvesters and CPs must be regarded. Low ambient harvesters such as TEGs require CP topologies to compensate for sub-100 mV range start-up and high pumping efficiency (also VCE). In such situations with sub-threshold voltage and self-start requirements, FBB or DBB of the MOSFET’s body-terminal is typically used to reduce threshold voltages for LV applications. These schemes come in expense of higher leakage current on the low \(V_{TH}\) conduction path for FBB and circuit complexity or area overhead for DDB. If a more efficient MOSFET turn-on (and better VCE) at low ambient voltages is required, CPs with \(V_{TH}\) cancelation or gate voltage augmentation schemes such as bootstrapping CPs and dynamic gate control from augmented voltages of later stages are desired. Otherwise, non-linear type CPs (Exponential CP, Fibonacci CP) may be used for enhanced voltage boosting with reduced stage number.

In designs where low power consumption is desirable, energy recycling with adiabatic type CP is a solution in expense of slower pumped-up voltages. Alternatively, an adaptive CP with active/idle mode transition or reconfigurable stages can be considered if extra chip area is available. Good PCE is achievable
when current drivability of CP is incremented with lower $RC$ delay and larger MOS devices. The latter has a drawback of higher $V_{TH}$ values, deterring LV start-up. Recent CP designs have typically much higher $V_{CE}$ compared to their PCE. Therefore, balancing between both voltage and power efficiency requires more exploration as it is vital to optimize power transfer between harvester and the CP circuit while balancing a good pumping efficiency as well. This will be reflected in the proposed hybrid energy harvesting circuit (Lim et al., 2013) where maximum power should be extracted from all three harvesters with impedance matching schemes whereas maximum efficiency should be achieved between the power circuits (e.g., CP or step-up voltage converters) and the load.

For monolithic integration of CP topologies, $C_{PUMP}$ sizes are kept to $\sim$20-500 pF ranges. Dual branch and latched type CPs with half the pumping capacitor size requirements for the same efficiency of single branches may be a solution.

Some noteworthy achievements at the lower power spectrum ($\mu$W) have been reported for CPs with PCE up to $\sim$72.5% at 450 mV supply voltage; recent CP operates with a mere 40 mV ($V_{CE} = \sim 54\%$) input voltage as well as some CPs reaching pumping efficiency up to $\sim$86% at 180mV supply voltages.

Challenges to be addressed by future research include developing CP topologies with sub-100 mV start-up voltages and further improving and balancing pumping and power efficiencies at these low ambient voltages. Developing area and power efficient control techniques that optimize harvester usage and CP’s charge transferability. Challenges associated to losses and leakages in sub-threshold operation of modern CP topologies are non-trivial and require more attention in their CP design strategies and leakage management for LV energy harvesting applications.

**Conclusion**

This paper recommends the consideration and tradeoffs between the three factors: Voltage, power and form factor when selecting the optimum CP topology to suit a particular low power system especially in micro energy harvesting systems. Hence, future CP designs should consider the three above factors for the possibility of a fully monolithic integration.

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**Author’s Contributions**

Michelle Lim Sern Mi: Conducted overview of charge pump topologies, analysis and write-up of the manuscript.

Md. Shabiuil Islam: Constructed the research plan, organized and led the research, participated in analysis and contributed to the reviewing of the article critically.

Sawal Hamid Md. Ali and Jahariah Sampe: Involved in the development process of conceptual framework, discussion and development of drafting and review of the article.

**Ethics**

The authors have no conflicts of interest in the development and publication of current research.

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