Three dimensional simulation of short channel effects in junction less FinFETs

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Abstract
In this article, n-channel junction-less transistors (JLTs) with gate lengths in the range of 20–250 nm, having crystalline-silicon (c-Si) and polycrystalline-silicon (poly-Si) channels are characterized for the short channel effects (SCEs). The shift of the threshold voltage with the gate length and the drain induced barrier lowering (DIBL) are determined by three dimensional numerical simulations using technology computer aided design (TCAD) software. Conductive channels are considered to be fin like structures surrounded by oxides and gate materials on three sides. The effect of important device parameters are considered. Degradation of SCEs with shortening of the gate length is predicted as expected from two dimensional simulations. In addition, simulations indicate improvements for lower doping. Thinner channels show better DIBL and threshold shift. The fin height dependence is more complicated where undesirable peak in DIBL is observed for mid-range heights near 200 nm. DIBL sharply drops for lower fin heights but the threshold shift becomes worse. Overall a small gate device of 20 nm with short fins of similar size can be expected to give a threshold shift of less than 30 mV and DIBL about 70 mV/V and, the use of three dimensional dielectric pockets leads to near zero shift of the threshold voltage. The performance of the two material types are comparable.

KEYWORDS
DIBL, dielectric pocket, FinFET, junction-less transistor, poly-silicon, threshold voltage ($V_{TH}$), threshold voltage roll-off ($\Delta V_{TH}$)

JEL CLASSIFICATION
Electrical and electronic engineering

1  |  INTRODUCTION

Threshold voltage is one of the key parameters of the field effect transistors both in digital and analog applications. When transistor is used as a switch in a digital application, the threshold voltage determines the voltage for turning the device on or off. In analog circuits, it affects the biasing of the circuit and consequently all other relevant parameters such as voltage or current gain. As the device dimensions shrink the predictions of the threshold voltage based on classical textbook
mathematical relations become inadequate. This is commonly referred to as the short channel effect (SCE). Two indicators are used to characterize the SCEs. These are the threshold shift (ΔVth) and drain induced barrier lowering (DIBL). It is important to determine the effect of various device parameters such as device dimensions, channel doping and material on these indicators.

This work is focused on SCEs of junction-less field effect transistors with fins (JL-FinFET). These devices differ from traditional metal oxide semiconductor field effect transistors (MOSFETs) in two important ways. First, they are junction less. Junction-less field effect transistors (JLFET) have been considered as a potential device for nanometer scale dimensions.1-7 Even though the device structure is very much like the common inversion mode MOSFET but there are important differences which make it attractive for future. The device is uniformly doped that is, the source, drain, and channel are all of the same doping type hence avoiding junction formation. The absence of p-n junctions has processing advantages for the small scales. Formation of shallow junctions and very sharp doping gradients are fabrication challenges at nanometer dimensions.6 From the performance perspective, the current carriers are in the bulk of the silicon film with higher mobility compared to the usual inversion mode device where the carriers are at the silicon-insulator interface. Therefore the degradation of carrier mobility due to transverse electric fields is expected to be lower. The SCEs are believed to be less severe in this transistor structure as well.7 The second difference is that the modern device structures use three dimensional fin like structures to form the transistor channel (FinFET). Here, the conductive channel is a fin protruding from the surface of the device in contrast to the traditional device structure which is planar. We consider junction-less FinFETs with gate oxide and metal covering three sides of the channel.

Computer simulations have been indispensable for understanding the short channel effects. Many JLFET analytical and numerical simulations have been 1 or 2-dimensional focused on the device cross section.8-23 While with the inherently three dimensional (3-D) nature of the fin structure, 3-D numerical simulations are preferred. Here, the three dimensional numerical simulation tool TCAD-Silvaco24 is used to study the effect of the various device parameters on the key threshold indicators mentioned above. Three dimensional simulations are harder to implement and take more computer time. However, the outcome is a set of plots showing the variation of the threshold indicators with various device parameters which enable the device designers to select the parameters for their application. We now present a review of the previous 3-D simulations and experiments.

Lee et al.4 carried 3-D simulations of single crystal device and found better performance of JLFET compared to inversion mode (IM) device. They studied the effect of different doping levels, gate lengths and fin widths on threshold voltage roll-off, subthreshold slope (SS), and DIBL. The fin width and thickness were in the range of 5-10 nm, and the gate lengths of 10 to 30 nm were considered. Yan et al.5 also presented 3-D simulation results for sub 50 nm junction-less nanowire transistors. The variation of DIBL, SS, threshold voltage, and Ion with various device parameters such as oxide thickness, channel doping, and fin aspect ratio were considered. Some simulations were for the gate length of 25 nm while for others the gate lengths of 40 nm was considered. The threshold voltage roll-off was not presented. They concluded that the junction-less nanowire transistor can provide high current drive and good short channel behavior. Park et al.7 presented 3-D simulations for single crystal silicon JLFET and showed improved threshold roll-off and DIBL compared to inversion mode device. They presented experimental measurements which were in agreement with their simulations. The gate length was in the range of 20–250 nm. Here the fin thickness of 20 nm and fin width of 15 nm were used. Recently, the measurements of Park et al.25 on planar IM device and junction-less transistor showed that the DIBL for planar JLFET was higher than the IM device opposite to previous belief. However, for small nanowire junction-less device, the DIBL performance of the JLFET improved and was comparable to the IM device. For the planar devices the mask gate lengths were 50 nm, 100 nm, and 1 um, and the mask gate width was 10 um. The nanowire junction-less transistor had mask gate length of 1 um and gate width of 80 nm. Hu et al.20 presented analytical model for junction-less FinFET and presented 3-D simulations using Sentaurus software. They only considered variation of threshold voltage and DIBL with the gate length. Similarly, Guo and Wang27 presented 3-D simulations only considering the variation of threshold voltage and DIBL with the gate length. It is worth noting that reliability studies comparing threshold shift of the junction-less versus traditional structures have shown improved performance of the junction-less devices.28

While the early work on JLFETs has been on single crystal silicon but polycrystalline silicon was recently proposed by Lee et al.29 The cost effectiveness and low thermal budget are some of the attractive features of the polycrystalline device. It is also believed that poly-Si is suitable for stacking layer technology.29 As far as the device performance is concerned the poly-Si has lower mobility compared to single crystal due to grain boundaries. However, it appears that as the device dimensions become smaller than the grain size, the difference between single and poly crystalline mobility becomes much smaller. Recent work by Billah et al.30 shows grain size of 350 nm which is large compared to our device dimensions. Lee
et al.\textsuperscript{29} performed 3-D simulations of poly-Si JLFET and compared their results with single crystal device. The gate lengths of 50 nm, 100 nm, 1 um, and 5 um were considered. The fin width and height (thickness) of 5 to 30 nm were considered in their simulations. They focused on SS and the on/off current ratio. They concluded that the poly and single crystal devices had comparable performance. They did not present data on threshold roll-off and DIBL.

In addition to the short channel effects, other aspects of the junction-less devices have also been considered. A recent review of the subthreshold behavior is given by Nowbahari et al.\textsuperscript{31} Several authors have addressed the modeling and simulation of the analog/RF performance of FinFETs\textsuperscript{32–35} as well. The dependence of RF equivalent circuit parameters on fin dimensions, partly a consequence of SCEs, is evident in some of these simulations.

The brief review presented above indicates the need for a systematic evaluation of the short channel effects such as threshold roll-off and drain induced barrier lowering as the 3-D device dimensions are varied. In Section 2, we present the device structure and models used for the simulations. In Section 3, we present the results of the 3-D simulations for devices with different fin dimensions. The fin height, thickness, gate length, and channel doping are varied and their effect on threshold roll-off and DIBL are determined. This evaluation is repeated for both single and poly crystal channels. We also compare our findings with those measured and simulated in literature for devices of similar structure and we improve the threshold shift by applying a dielectric pocket to the channel of the 3-D device. The conclusions are given in Section 4.

2 SIMULATION

A JLT having c-Si and poly-Si channel with gate lengths down to 20 nm is simulated by the 3-D technology computer aided design (TCAD-Silvaco)\textsuperscript{24} and evaluated for short-channel electrical characteristics in terms of $\Delta V_{TH}$ characteristics and DIBL.

Here, the device is designed on the bulk-Si substrate with a thick oxide layer. Figure 1 shows the fin like structure and design variables for the 3-D device simulation of the JLFET.

![Figure 1](image-url) (A) device structure and design variables of the 3-D JLT used in the simulation. (B) Fin structure in big scheme. (C) Fin covered with oxide for channel width calculation
In order to simulate the SOI-like environment on the bulk-Si, 100-nm-thick insulator (SiO$_2$) was assumed to be deposited on the Si substrate. The gate dielectric (SiO$_2$) thickness of 2.5 nm is used and the P$^+$ poly-silicon with high work function of 4.2 eV is used as the gate material. Source and drain contacts are ohmic to aluminum metal electrodes. In result, the silicon-on-insulator (SOI) material structure consists of a silicon fin of various heights on a 100 nm-thick buried oxide (BOX). Three sides of the fin are covered with 2.5 nm oxide and 40-nm thick gate. A uniform n-type doping concentration of $N = 0.5–2 \times 10^{19}$ cm$^{-3}$ is used for the channel and S/D regions.

In the following sections, we present results of variations of the threshold voltage shift and DIBL with geometrical and material parameters. Simulations are provided for the dimensional channel variables namely channel height ($H_{ch}$), channel thickness ($t_{ch}$ = $t_{Si}$), and channel or gate length ($L_{ch} = L_{gate}$). Along with device dimensions, doping concentration, and crystal structure of the channel are also varied. Simulations are carried for both single and poly-crystal silicon channel. The TCAD models include fldmob, srh, fermi, ni.fermi, BPQ quantum model, bbt.std, and bbt.nonlocal to consider the tunneling effects and nonlocal trap assisted tunneling effects in 2-D simulation of poly-si channels.

3 | SIMULATION RESULTS

Simulation results for various JLT structures are presented in this section. The characteristics of interest are the shift in threshold voltage ($\Delta V_{TH}$) and drain induced barrier lowering (DIBL). The $\Delta V_{TH}$ is defined as the difference in $V_{TH}$ value between any physical gate length $L_{gate}$ and the long physical gate length equal to 250 nm. The JLTs of various gate lengths ranging from 20 to 250 nm are characterized. The DIBL characteristic is defined as

$$DIBL = V_{TH} (V_D = 0.05 \, V) - V_{TH} (V_D = 1 \, V).$$

The threshold voltage is extracted at constant current of $10^{-7} \times W_{eff}/L_G$. Here, $W_{eff}$ is calculated as

$$W_{eff} = 2H_{ch} + 4t_{ox} + t_{ch}.$$  

In order to have better understanding of 3-D simulations, it was decided to simulate a 3-D structure with very high channel height (tall fin) resulting in $W_{eff}=1$ um which is presumed for 2-D simulations. These results are then compared with the 2-D simulations. The result of this comparison at the drain voltage of $V_D=0.1$ V is presented in Figure 2A,B. Here the fin height is 490 nm resulting in a total gate width of 1 micron. According to this figure, the results of the simulation of a 3-D structure follow the same trend as the 2-D simulation. However the absolute values are not equal. The differences could be due to the end effects which enter the 3-D simulations, such as the interface between fin and the bottom BOX. The three dimensional nature of the electric field at the top and bottom of the fin could result in the differences shown in the figure.

Figure 3 shows the effect of the channel thickness on DIBL and threshold shift. The drain voltage is equal to $V_D=0.05$ V for this simulations and all other results that follow, unless specified otherwise. Results are presented for both single and poly crystalline silicon channel in solid and dashed lines with fin height of 17.5 and 490 nm. The fin height of 17.5 nm results in $W_{eff}$ ranging from 55 to 65 nm, depending on the channel thickness. Figure 3A shows the increase in DIBL with increasing channel thickness. This is expected since as the ratio of channel length to thickness decreases we expect less control of the channel by the gate voltage. In such situation the drain voltage affects the threshold. Figure 3B confirms the above argument. There is larger threshold shift for the thicker channel material. It is not reasonable to increase the thickness of the channel to more than the channel length. In addition, according to Figure 3, there is not a noticeable difference between the two types of materials.

We can compare the short channel behavior of a long fin device with the channel height of 490 nm (in dotted lines and filled black circles) with the short fin of 17.5 nm. Figure 3 indicates the variation of both threshold shift and DIBL are greater for the long fin structure that is, the short fin device has superior performance. It is worth noting the device with the short fin has a nearly square cross section, almost a short nanowire.

The JLT structures with two different channel heights are shown in Figure 4. The effective gate width is accordingly different for these two devices. Figure 5 shows the effect of the channel height on the parameters of interest. The simulation results are presented for two gate lengths of 20 and 50 nm for both c-Si and poly-Si materials. The device with the larger gate length of 50 nm shows improved performance relative to the device with the 20 nm gate length. This is expected from 2-D analysis and simulations as well. We focus on the 20 nm gate length device where Figure 5A shows the
FIGURE 2  (A) DIBL $[\text{DIBL} = V_{TH}(V_D = 0.1 \text{ V}) - V_{TH}(V_D = 1.1 \text{ V})]$ and (B) $\Delta V_{TH}$ values of similar structures in 2D and 3D at $t_{\text{ch}} = 10 \text{ nm}$, $W_{\text{eff}} = 1000 \text{ nm}$ and channel doping $N = 1 \times 10^{19} \text{ cm}^{-3}$

FIGURE 3  (A) The DIBL and (B) $\Delta V_{TH}$ comparison between different channel thickness in c-Si and poly-Si with $L_{\text{gate}} = 20 \text{ nm}$, $H_{\text{ch}} = 17.5 \text{ nm}$, and channel doping $N = 1 \times 10^{19} \text{ cm}^{-3}$ and comparison between two heights $H_{\text{ch}} = 17.5 \text{ nm}$ and $H_{\text{ch}} = 490 \text{ nm}$
FIGURE 4 Device structure with 55 and 220 nm channel width

FIGURE 5 (A) The DIBL and (B) $\Delta V_{TH}$ comparison for different channel height in c-Si and poly-Si channels with $L_{gate} = 20\&50$ nm, $t_{ch} = 10$ nm and channel doping $N = 1 \times 10^{19}$ cm$^{-3}$

DIBL improves for the very short fin while in Figure 5B the threshold shift worsens as the fins get smaller. Comparing the two material types again we see a slight improvement for the poly-Si. It is worth noting the SCEs are presumed to be independent of the gate width, based on one or two dimensional device considerations. However, the effect of gate width can be taken into account through three dimensional simulations. Extending the simulations to wider gate width reveals a peak in DIBL for mid-range fin heights, as shown in Figure 6A. Here, it is shown that for the fin height near 200 nm, DIBL has the highest value and is nearly flat. For shorter fin heights DIBL drops sharply.

This result indicates the top gate electrode is most effective for controlling the channel. For short fin heights, the side gate electrodes become less relevant. By increasing the fin height the top and side electrodes play a similar role in controlling the channel. This appears to be least effective gate control with drain voltage influencing the channel potential. The highest DIBL is observed for fin height of 200 nm. With further increase of the fin height, the side gate electrodes become dominant and the top gate becomes less effective. Indeed, we only observe a slight decrease of DIBL as the fin height is increased from 300 to 500 nm.
Figure 6B shows the threshold shift as a function of fin height. Threshold shift worsens as the fin height reduces. Therefore, opposite behavior is observed for the SCE indicators with respect to the fin height. We notice the largest shift occurs in a dip at height of 200 nm. The threshold shift for the lowest fin heights is above $-30$ mV which could be acceptable, considering the low value of DIBL for the smaller heights.

The effectiveness of the top gate can be attributed to the top-down potential distribution as opposed to the side. In the top-down direction electrons face the sharp potential increase between the silicon and the bottom BOX on one side and the softer rise due to depletion layer toward the gate electrode. While in the side-side direction the electrons only see the softer increase of the depletion potential on both sides. Hence, better top gate control results.

Figure 7A, B shows the variation of the short channel performance parameters with the channel length, which is equal to the gate length $L_G = L_{ch}$. Two different fin heights of $H_{ch} = 17.5$ and 100 nm are considered for both material types. Here, the performance is as expected. Namely, a worsening of the SCEs with decreasing gate length. In Figure 7A as far as DIBL is concerned, the shorter fin performs better while the opposite is true for the $\Delta V_{TH}$ in Figure 7B. This is consistent with results of Figure 6. The difference between the two materials is again marginal, with the poly showing slightly lower threshold shift. The dashed line corresponds to the poly material.

The effect of doping is shown in Figure 8A, B. Only single crystal simulations are presented. Three channel doping levels of $N = 0.5, 1, \text{ and } 2 \times 10^{19} \text{ cm}^{-3}$ are considered. Three channel heights of $H_{ch} = 17.5, 100, \text{ and } 490 \text{ nm}$ are also considered for each doping type. The three lowest dashed curves of Figure 8A clearly show the low value of DIBL corresponding to the shortest channel height. In addition, the lowest doping has the lowest DIBL. Examination of the other two channel heights also indicates the lowest doping has the best DIBL performance. Among the three channel heights the middle height of $H_{ch} = 100$ nm shows the lowest spread of the DIBL among the three doping levels, indicating least sensitivity to doping for this channel height, similar to the peak observed in Figure 6A. As far as the threshold shift in Figure 8B is concerned, again the lowest doping device shows the lowest shift. Unlike Figure 8A the spread in the plots for the middle channel height $H_{ch} = 100$ nm shown by solid lines is comparable to the other two channel heights and an improved sensitivity is not observed. However, considering the lowest curves corresponding to the $N = 0.5 \times 10^{19} \text{ cm}^{-3}$ we observe that the device with the $H_{ch} = 490$ nm shows the lowest shift below $-20$ mV for the shortest channel length of $L_{ch} = 20$ nm. This is also clearly seen for the $N = 1 \times 10^{19} \text{ cm}^{-3}$ plots. In summary, for the shortest gate length $L_{gate} = 20$ nm the lowest...
**FIGURE 7**  (A) The DIBL and (B) $\Delta V_{TH}$ variation with channel length with channel doping of $N = 1 \times 10^{19} \text{ cm}^{-3}$

**FIGURE 8**  (A) The DIBL and (B) $\Delta V_{TH}$ characteristics of JLTs for different channel doping concentration in c-Si channel
doping $N = 0.5 \times 10^{19} \text{cm}^{-3}$ and shortest channel height $H_{ch} = 17.5 \text{nm}$ we have the lowest DIBL. However the lowest $\Delta V_{TH}$ occurs for the lowest doping and $H_{ch} = 490 \text{nm}$. We conclude that the lowest doping $N = 0.5 \times 10^{19} \text{cm}^{-3}$ with the height $H_{ch} = 100 \text{nm}$ could be a good performance compromise. Even though this does not give the best DIBL but it does result in good threshold shift and least sensitivity to doping variation for DIBL.

In Figures 9 and 10, the potential profile of the channel center and surface (silicon-oxide interface) are compared at two drain voltages. As shown in Figure 9, at low drain voltage of 0.05 V the variation of the potential along the length of the device is small and almost indistinguishable for the three different channel heights. Figure 10 shows the potential profiles at drain voltage of 1 V. Here, we see the larger upward shift for fin heights $H_{ch} = 100$ & 490 nm, while for the small fin height of $H_{ch} = 17.5 \text{nm}$ the shift is smaller. This confirms the diminished effect of drain voltage for the shorter fins which was also observed at DIBL plot of Figure 6A.

Figure 11 compares the surface and center potential for the c-Si and poly-Si devices. Two different drain voltages are shown. The difference of the potential distribution between the two material types are marginal something which was also observed at the device terminal characteristics in their short channel behavior.

The parametric simulations presented above do not show an overwhelming superiority of single crystalline over poly crystalline channel or vice versa. A comparison of the two material types is shown in Table 1. Here a set of typical parameters are used. We notice there is not a noticeable difference.

We compare our findings with measured and simulated results reported in literature. Park et al. measured threshold shift of $-40 \text{mV}$ for a 20 nm gate length device. Their doping level was $1-2 \times 10^{19} \text{cm}^{-3}$, channel thickness of 15 nm, oxide thickness of 5 nm, and gate width of 55 nm. Their 3-D simulation result is consistent with their measured value. Our results indicate a threshold shift of $-27 \text{mV}$, for doping of $1 \times 10^{19} \text{cm}^{-3}$, channel thickness of 10 nm, oxide thickness 2.5 nm, and the same gate width. Considering the difference in device structure of thicker oxide and channel, we expect a larger value for their device. They reported a low DIBL of $-10 \text{mV/V}$ in their early work but the DIBL values of near 40 mV/V for nanowires with different device parameters were reported later. As shown in Table 1,
FIGURE 11  Central and surface potential variations versus position along channel for two drain voltages with c-Si and poly-Si channel material at $L_{\text{gate}} = 20\,\text{nm}$, $t_{\text{ox}} = 2.5\,\text{nm}$, $L_{\text{ch}} = 10\,\text{nm}$, $H_{\text{ch}} = 17.5\,\text{nm}$, and channel doping $N = 1 \times 10^{19}\,\text{cm}^{-3}$

![Graph showing potential variations vs. position along channel for two drain voltages with c-Si and poly-Si channel material.]

TABLE 1  The DIBL and $\Delta V_{TH}$ values of different channel types at $L_{\text{gate}} = 20\,\text{nm}$, $W_{\text{eff}} = 55\,\text{nm}$, and $N = 1 \times 10^{19}\,\text{cm}^{-3}$

| Ch. semiconductor | DIBL (mV/V) | $\Delta V_{TH}$ (mV) |
|-------------------|-------------|----------------------|
| c-Si              | 65          | −27                  |
| poly-Si           | 67          | −25                  |

we simulated 65 mV/V for our device. Lee et al.\textsuperscript{4} reported threshold shift of $-50\,\text{mV}$ and DIBL of $48\,\text{mV/V}$ for a 10 nm gate length nanowire. The channel and oxide thicknesses were 5 and 2 nm respectively. Three dimensional simulations of Yan et al.,\textsuperscript{5} for a device with gate length of 25 nm, doping of $1 \times 10^{19}\,\text{cm}^{-3}$, channel thickness of 10 nm, oxide thickness of 1 nm, and fin height of 10 nm gave a DIBL value of 70 mV/V. The above summary indicates that our simulated values are in acceptable range of other results reported even though the device dimensions were not the same for all cases considered.

Finally, by creating a dielectric pocket with a length of 5 nm, a thickness of 10 nm and a height of 11.5 nm on the two ends of the channel of the base structure as shown in Figure 12, we improve SCEs in the device. The promise of this type of device structure was demonstrated by two dimensional simulations of Singh.\textsuperscript{18,19} Here, we show the result for a three dimensional structure using 3-D numerical simulations in Table 2. According to this table the threshold shift is reduced to zero volt.

FIGURE 12  Device structure with dielectric pocket (DP)

TABLE 2  The DIBL and $\Delta V_{TH}$ values of channel types without and with dielectric pocket (DP) at $L_{\text{gate}} = 20\,\text{nm}$, $W_{\text{eff}} = 55\,\text{nm}$, and $N = 1 \times 10^{19}\,\text{cm}^{-3}$

| Ch. semiconductor | DIBL (mV/V) | $\Delta V_{TH}$ (mV) |
|-------------------|-------------|----------------------|
| c-Si              | 65          | −27                  |
| c-Si with DP      | 65          | 0                    |
4 | CONCLUSIONS

Three dimensional numerical simulations of the junction-less FINFETs were carried out to investigate the short channel effects. The simulations included both single and poly crystalline channels. These simulations demonstrated the effect of the various device parameters. The results obtained were consistent with experimentally measured and simulated results reported in literature. Based on these simulations it was concluded that, there was no significant difference in performance of the two material types. Overall, the short fin structures with square cross section showed improved SCEs. Three dimensional simulations of a novel structure with dielectric pockets showed near ideal performance. The results obtained could aid designers to make necessary trade-offs toward a given design goal as far as the short channel effects are concerned.

As the device dimensions shrink further to a few nanometers, full quantum mechanical calculations of the device performance become a necessity. Our present simulations include some quantum effects but it is not considered a full quantum treatment. Therefore, new simulation tool has to be utilized for future evaluation of the device performance.

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CONFLICT OF INTEREST

Authors have no conflict of interest relevant to this article.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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