Universal Memcomputing Machines

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Abstract—We introduce the notion of universal memcomputing machines (UMMs): a class of brain-inspired general-purpose computing machines based on systems with memory, whereby processing and storing of information occur on the same physical location. We analytically prove that the memory properties of UMMs endow them with universal computing power—they are Turing-complete, intrinsic parallelism, functional polymorphism, and information overhead, namely their collective states can support exponential data compression directly in memory. We also demonstrate that a UMM has the same computational power as a non-deterministic Turing machine, namely it can solve NP-complete problems in polynomial time. However, by virtue of its information overhead, a UMM needs only an amount of memory cells (memprocessors) that grows polynomially with the problem size. As an example we provide the polynomial-time solution of the subset-sum problem and a simple hardware implementation of the same. Even though these results do not prove the statement NP=P within the Turing paradigm, the practical realization of these UMMs would represent a paradigm shift from present von Neumann architectures bringing us closer to brain-like neural computation.

Index Terms—memory, memristors, elements with memory, memcomputing, Turing Machine, NP-complete, subset-sum problem, brain, neural computing, Fourier transform, DFT, FFT, DCRAM.

I. INTRODUCTION

Since Alan Turing invented his ideal machine in 1936 [1], mathematicians have been able to develop this concept into what is now known as computational complexity theory [3], a powerful tool essentially employed to determine how long does an algorithm take to solve a problem with given input data. This ideal machine is now known as universal Turing machine (UTM) and represents the conceptual underpinning of all our modern-day digital computers.

The practical realization of a UTM is commonly done using the von Neumann architecture [4], which apart from some inconsequential details, can be viewed as a device that requires a central processing unit (CPU) that is physically separate from the memory (see figure [1] left panel). The CPU contains both a control unit that directs the operation of the machine, and all arithmetic functions and logic gates the machine needs during execution (arithmetic/logic unit). This form of computation requires a large amount of data to be transferred between the CPU and the memory, and this necessarily limits the machine both in time (von Neumann bottleneck [5]), and in energy [6].

Parallel computation, as it is currently envisioned, mitigates somewhat, but does not solve any of these issues: several processors each manipulate parts of the whole data, by typically working with a physically “close” memory. Eventually, however, all the processors have to communicate with each other to solve the whole problem, still requiring a substantial amount of information transfer between them and their memories [6]. Overcoming this “information latency issue” would then require a fundamentally different way in which data are manipulated and stored.

Historically, the first alternative to the von Neumann architecture was the “Harvard architecture” developed by H. Aiken, concurrently with the ENIAC project that would be using the von Neumann architecture [6]. Original Harvard architectures had separate memories for instructions and data. However, this term is used today to mean machines with a single main memory, but with separate instruction and data caches [6]. A more recent alternative is the “pipelined architecture”, i.e., data processing stages connected in series, where the output of one stage is the input of the next one [6]. This architecture is commonly used in modern CPUs, and is particularly efficient for graphics processing units (GPUs) [7]. Finally, we mention an alternative concept that is still under investigation, named “liquid-state machine”. It consists of a computational model for real-time computing on time-varying input [8]. Although some of these concepts have found (or may eventually find) use in practical computing, none of these alternatives completely solve the limitations of the von Neumann architecture, or show additional, substantial advantages compared with Turing machines.

Very recently, a new computing paradigm, inspired by the operation of our own brain, has been proposed which is not based on the UTM concept, and which puts the whole burden of computation directly into the memory. This paradigm has been named memcomputing [9].

Like the brain, memcomputing machines would compute with and in memory without the need of a separate CPU. The memory allows learning and adaptive capabilities [10], [11], bypassing broken connections and self-organizing the computation into the solution path [12], [13], much like the brain is able to sustain a certain amount of damage and still operate seamlessly.

The whole concept of memcomputing can be realized in practice by utilizing physical properties of many materials and systems which show a certain degree of time non-locality (memory) in their response functions at particular frequencies and strengths of the inputs [14]–[16]. In fact, the field has seen a surge of activities since the introduction of resistors, capacitors, and inductors with memory, (memristors, memcapacitors, meminductors, respectively) collectively called memelements [17], and their actual realization in a variety of systems (see, e.g., [18]–[22] and the review [15]). For instance, physical and statistical properties, [23]–[26] computing capability [27], [28], and more [29] have been studied for networks of memristors. However, more complex dynamics and very interesting
properties can arise using memelements other than memristors, and combining these with standard electronic devices. For example, we have recently suggested an actual implementation of a memcomputing machine that has the same architecture of a Dynamic Random Access Memory (DRAM), but employs memcapacitors to compute and store information. This particular architecture, we have called Dynamic Computing Random Access Memory (DCRAM) and expends a very small amount of energy per operation, is just an example of what can be accomplished with memelements. Nevertheless, it already shows two features that are not available in our modern computers: intrinsic parallelism and functional polymorphism.

The first feature means that all memelement processors (memory cells or memprocessors for short), operate simultaneously and collectively during the computation (Fig. 2 leftmost panel). This way, problems that otherwise would require several steps to be solved can be executed in one or a few steps. The second feature relates to the ability of computing different functions without modifying the topology of the machine network, by simply applying the appropriate input signals (Fig. 2 middle panel). This polymorphism, which is again similar to that boasted by our brain and some of our organs (such as the eyes), shows also another important feature of memcomputing machines: their control unit—which is not a full-fledged CPU since it does not need any arithmetic/logic function, and which is required in order to control the execution of the type of problem that needs to be solved by the machine—can either be fed directly by the input data, or indirectly through the flow of input data to the memprocessors (see figure right panel).

The last important property of UMMs, namely their information overhead, is related to the way in which memprocessors interconnected by a physical coupling can store a certain amount of data (Fig. 2 rightmost panel). More specifically, the information overhead is the capability of an interacting memprocessor network to store and compress an information amount larger than that possible by the same non-interacting memprocessors. In fact, in section VI we will show how a linear number of interconnected memprocessors can store and compress an amount of data that grows even exponentially. It is this physical type of interaction—resembling closely that of the neurons in the brain—which also underlies a fundamental difference with the present UTMs and their practical realizations.

Having found an example of a memcomputing machine and its main features, it is then natural to ask whether, in analogy with a general-purpose UTM, a similar concept can be defined in the case of memcomputing machines. And if so, how do they relate to UTMs and what types of computational complexity classes these systems would be able to solve?

In this paper, we introduce the notion of universal memcomputing machine (UMM). This is a class of general-purpose machines based on interacting memprocessors. In the present context, we do not limit this concept to memprocessors composed only by memristors, memcapacitors or meminductors. Rather, we consider any system whose response function to some external stimuli shows some degree of memory. We show that such an ideal machine is Turing-complete, namely it can simulate a UTM. Most importantly, however, in view of its intrinsic parallelism, functional polymorphism and information overhead, we prove that a UMM is able to solve Non-deterministic Polynomial (NP) problems in polynomial (P) time. In particular, we consider the NP-complete subset-sum problem, and using two examples we show how a UMM can solve it in polynomial time using a number of memprocessors that either grows exponentially or, by exploiting the information overhead, uses a linear number of memprocessors. This last example can be easily realized in an electronics lab.
Note that this result does not prove that NP=P, since this proposition should be solved only within the domain of UTMs. Rather, it shows that the concept we introduce, if realized in practice, provides a powerful new paradigm for computation with features approaching those of a brain.

The paper is organized as follows. In Sec. II we first briefly review the formal definition of UTMs. In Sec. III we introduce the formal definition of memprocessor while in Sec. IV we introduce the mathematical description of a UMM and prove its Turing-complete-ness. In Sec. V we discuss the first two properties of UMMs, specifically their parallelism and polymorphism. We devote the entire Sec. VI to the third important property of UMMs, namely their information and polymorphism. We conclude our thoughts for the future in Sec. VIII.

II. Universal Turing Machine

In order to properly clarify the aim of our present work and put it into context, we briefly review the point of view of the UTM. For a complete and thorough description we refer the reader to the extensive literature on the subject ( [2] for history on UTM, [3] a classic, and [4] for more modern literature).

In simple terms a UTM is a mathematical model of an object operating on a tape. The fundamental ingredients of a UTM are then the tape itself (possibly infinite), a tape head to read and write on the tape, a state register storing the states of the UTM (including the initial and final states), and finally a finite table of instructions. Formally, a UTM is defined as the seven-tuple

\[ UTM = (Q, \Gamma, b, \Sigma, \delta, q_0, F), \]

where \( Q \) is the set of possible states that the UTM can be in, \( \Gamma \) is the set of symbols that can be written on the tape, \( b \in \Gamma \) is the blank symbol, \( \Sigma \) is the set of input symbols, \( q_0 \in Q \) is the initial state of the UTM, \( F \subseteq Q \) is the set of final states, and

\[ \delta : Q \setminus F \times \Gamma \rightarrow Q \times \Gamma \times \{ L, N, R \}, \]

is the transition function (the table) where \( L, N \) and \( R \) are Left, No, and Right shift, respectively.

From this formal definition it can be readily seen that no explicit information about any physical system or its properties is involved in a UTM. In other words, the UTM is just an abstract mathematical object, through which it is possible to determine the computational complexity of an algorithm, i.e., given \( n = \text{cardinality}[\Sigma] \) we can determine the number of operations \( f(n, \delta) \) the UTM should perform in order to find the final state \( F \).

In the last sixty years, several alternatives or modifications of the UTM have been introduced, from the non-deterministic Turing machine to parallel Turing machine and more, but all of those variants have been unified through the concept of universality of a UTM [3], [12]. In this picture, the complexity theory derived from each of those variants is equivalent, in the sense that all these machines can solve the same type of problem, albeit with different execution times. A separate discussion is required for the Quantum Turing machine, and indeed we will compare this to a UMM in Sec. IV.

III. Memprocessors

The basic constitutive unit of a memcomputing architecture is what we name “memprocessor”. Here, we give a formal definition of memprocessor that actually represents the link between real memcomputing architectures and the formal definition of a UMM. This should also clarify that a memprocessor is not necessarily made of passive elements with memory, such as memelements, rather it is a much more general object.

We define a memprocessor as an object defined by the four-tuple \((x, y, z, \sigma)\) where \(x\) is the state of the memprocessor, \(y\) is the array of internal variables, \(z\) the array of variables that connect from one memprocessor to other memprocessors, and \(\sigma\) an operator that defines the evolution

\[ \sigma[x, y, z] = (x', y'). \]

When two or more memprocessors are connected, we have a network of memprocessors (computational memory). In this case we define the vector \(x\) as the state of the network (i.e., the array of all the states \(x_i\) of each memprocessor), and \(z = \bigcup z_i\) the array of all connecting variables, with \(z_i\) the connecting array of variables of the memprocessor \(i\)-th.

Let \(z_i\) and \(z_j\) be respectively the vectors of connecting variables of the memprocessors \(i\) and \(j\), then if \(z_i \cap z_j \neq \emptyset\) we say that the two memprocessors are connected. Alternatively, a memprocessor is not connected to any other memprocessor (isolated) when we have \(z = z(x, y)\) (i.e., \(z\) is completely determined by \(x\) and \(y\)) and

\[ \sigma[x, y, z(x, y)] = (x, y), \]

which means that the memprocessor has no dynamics.

A network of memprocessors has the evolution of the connecting variables \(z\) given by the evolution operator \(\Xi\) defined as

\[ \Xi[x, y, z, s] = z', \]

where \(y = \bigcup_i y_i\) and \(s\) is the array of the external signals that can be applied to a subset of connections to provide stimuli for the network. Finally, the complete evolution of the network is defined by the system

\[
\begin{align*}
\sigma[x_1, y_1, z_1] &= (x'_1, y'_1) \\
\vdots \\
\sigma[x_n, y_n, z_n] &= (x'_n, y'_n) \\
\Xi[x, y, z, s] &= z'.
\end{align*}
\]

The evolution operators \(\sigma\) and \(\Xi\) can be interpreted either as discrete or continuous evolution operators. The discrete evolution operator interpretation includes also the artificial neural networks [33], while the continuous operator interpretation represents more general dynamical systems. We analyze two types of continuous operators: the operators representing memprocessors made only by memelements, and memprocessors given by arbitrary electronic units.
A. Memprocessors made by memelements

The standard equations of a memelement are given by the following relations [17]

\[
\begin{align*}
x_{\text{ex}}(t) &= g(x_{\text{in}}, u, t)u(t) \quad (7) \\
x_{\text{in}}(t) &= f(x_{\text{in}}, u, t) \quad (8)
\end{align*}
\]

where \( x_{\text{in}} \) denotes a set of state variables describing the internal state of the system, \( u \) and \( x_{\text{ex}} \) are any two complementary constitutive variables (i.e., current, charge, voltage, or flux) denoting input and output of the system, \( g \) is a generalised response, and \( f \) a continuous vector function. In this case the connection variables \( z \) are \( x_{\text{ex}}(t) \) and \( u(t) \), i.e., \( z = [x_{\text{ex}}(t), u(t)] \), and the state \( x \) coincides with \( x_{\text{in}}(t) \). Now, (7) can be interpreted as a constraint for (8), in the sense that we can write \( u = u(x_{\text{in}}(t), x_{\text{ex}}(t)) \) solution of \( x_{\text{ex}}(t) = g(x_{\text{in}}, u, t)u(t) \), so we can simply replace \( u(x_{\text{in}}, y) \) in (8), and forget about (7). In this case the evolution in a time \( T \) of (8) is given by

\[
x_{\text{in}}(t+T) - x_{\text{in}}(t) = \int_t^{t+T} f(x_{\text{in}}(\tau), u(x_{\text{in}}(\tau), x_{\text{ex}}(\tau)), \tau) d\tau
\]

and defining \( x = x_{\text{in}}(t) \) and \( x' = x_{\text{in}}(t + T) \) we have

\[
\sigma[x, y, z] = \sigma[x, z] = x_{\text{in}}(t) + \int_t^{t+T} f(x_{\text{in}}(\tau), u(x_{\text{in}}(\tau), x_{\text{ex}}(\tau)), \tau) d\tau
\]

On the other hand, the operator \( \Xi \) will be simply defined by the Kirchhoff’s laws and external generators in order to include the external signals \( s \).

B. Memprocessors made of generic electronic devices

In this case, the equation that defines a memprocessor is a general Differential Algebraic Equation (DAE) system that represents any electronic circuit. It can be casted as

\[
d\frac{dx}{dt} = f(x, y, z, t),
\]

where \((x, y, z)\) represents all the state variables of the circuit.

Using the chain rule we have \( \frac{d\sigma}{dt} = \frac{\partial \sigma}{\partial x} \frac{dx}{dt} + \frac{\partial \sigma}{\partial y} \frac{dy}{dt} + \frac{\partial \sigma}{\partial z} \frac{dz}{dt} \). From circuit theory and modified nodal analysis [34] there always exists a choice of \( y \) such that the Jacobian matrix

\[
J_{x,y}(x, y, z) = \begin{bmatrix}
\frac{\partial q(x, y, z)}{\partial x} & \frac{\partial q(x, y, z)}{\partial y}
\end{bmatrix}
\]

is squared but not necessarily invertible. If the \( J_{x,y} \) is not invertible, we can eliminate some variables by including constraints as in the previous section thus obtaining always a (reduced) \( J_{x,y} \) which is invertible. Therefore, without loss of generality, we can assume \( J_{x,y} \) invertible and we have from the chain rule and the Eqs. (11) and (12)

\[
\begin{bmatrix}
x' \\
y'
\end{bmatrix} = J_{x,y}^{-1}(x, y, z) \begin{bmatrix}
f(x, y, z, t) - \frac{\partial q(x, y, z)}{\partial z} \\
s
\end{bmatrix}
\]

The evolution in a time \( T \) is then given by

\[
\begin{bmatrix}
x(t+T) \\
y(t+T)
\end{bmatrix} = \begin{bmatrix}
x(t) \\
y(t)
\end{bmatrix} + \int_t^{t+T} J_{x,y}^{-1}(x, y, z) \begin{bmatrix}
f(x, y, z, \tau) - \frac{\partial q(x, y, z)}{\partial z} \\
s
\end{bmatrix} d\tau.
\]

Also in this case the operator \( \Xi \) will be simply defined by the Kirchhoff’s laws and external generators in order to include the external signals \( s \). This type of memprocessor represents for example those memory cells (e.g., memcapacitor plus field-effect transistor) of the DRAM we have introduced [30], as well as the memory cells we will describe in Sec. VII-B3. However, we anticipate that the latter has the state of the memprocessor defined by the amplitudes of the Fourier series of the state \( x \).

IV. UNIVERSAL MEMCOMPUTING MACHINE

We are now ready to introduce the general concept of a UMM. The UMM is an ideal machine formed by a bank of interconnected memory cells—memprocessors—(possibly infinite in number) able to perform either digital (logic) or analog (functional) operations controlled by a control unit (see figure 1 right panel). The computation with and in memory can be sketched in the following way. When two or more memprocessors are connected, through a signal sent by the control unit, the memprocessors change their internal states according to both their initial states and the signal, thus giving raise to intrinsic parallelism and the functional polymorphism we have anticipated.

A. Formal definition

We define the UMM as the eight-tuple

\[
UMM = (M, \Delta, P, S, \Sigma, p_0, s_0, F)
\]

where \( M \) is the set of possible states of a single memprocessor. It can be either a finite set \( M_d \) (digital regime), a continuum or an infinite discrete set of states \( M_a \) (analog regime), thus \( M \) can be expressed as \( M = M_d \sqcup M_a \). \( \Delta \) is a set of functions

\[
\delta_\alpha : M^{m_\alpha} \times F \times P \to M^{m_\alpha} \times P \times S,
\]

where \( m_\alpha < \infty \) is the number of memprocessors used as input (of read by) the function \( \delta_\alpha \), and \( m'_\alpha < \infty \) is the number of memprocessors used as output (written by) the function \( \delta_\alpha \); \( P \) is the set of the arrays of pointers \( p_\alpha \) that select the memprocessors called by \( \delta_\alpha \) and \( S \) is the set of indexes \( \alpha \); \( \Sigma \) is the set of the initial states written by the input device on the computational memory; \( p_0 \in P \) is the initial array of pointers; \( s_0 \) is the initial index \( \alpha \) and \( F \subseteq M \) is the set of final states.

For the sake of clarity, we spend a few more words on the functions \( \delta_\alpha \). Let \( p_{\alpha}, p'_{\alpha}, p_\beta \in P \) be the arrays \( p_\alpha = \{i_1, \ldots, i_{m_\alpha}\}, p'_{\alpha} = \{j_1, \ldots, j_{m_\alpha}\} \) and \( p_\beta(k_1, \ldots, k_{m_\beta}) \) and \( \beta \in s \), then the function \( \delta_\alpha \) can be expressed as

\[
\delta_\alpha[x(p_\alpha)] = (x'(p'_{\alpha}), \beta, p_\beta),
\]

where \( x \) is the vector of the states of the memprocessors, thus \( x(p_\alpha) \in M^{m_\alpha} \) are the states of the memprocessors selected
as input for \( \delta_{\alpha} \), while \( x'(p_{\alpha}) \in M^m_{\alpha} \) are the output states of \( \delta_{\alpha} \). Then \( \delta_{\alpha} \) reads the states \( x(p_{\alpha}) \) and writes the new states \( x'(p_{\alpha}') \), and at the same time prepares the new pointer \( p_{\beta} \) for the next function \( \delta_{\beta} \) with input \( x'(p_{\beta}) \in M^{m_{\beta}} \).

Note that the two important features of the UMM, namely parallelism and polymorphism, are clearly embedded in the definition of the set of functions \( \delta_{\alpha} \). Indeed the UMM, unlike the UTM, can have more than one transition function \( \delta_{\alpha} \) (functional polymorphism), and any function \( \delta_{\alpha} \) simultaneously acts on a set of memprocessors (intrinsic parallelism). Another difference from the UTM is that the UMM does not distinguish between states of the machine and symbols written on the tape. Rather, this information is fully encoded in the states of the memprocessors. This is a crucial ingredient in order to build a machine capable of performing computation and storing of data on the same physical platform.

Another important remark is that unlike a UTM that has only a finite, discrete number of states and an unlimited amount of tape storage, a UMM can operate, in principle, on an infinite number of continuous states, even if the number of memprocessors is finite. The reason being that each memprocessor is essentially an analog device with a continuous set of state values.

Finally, it can be noticed that the formal definition of memprocessor \([3]\) and network of memprocessors \([6]\) is compatible with the function \( \delta_{\alpha} \) defined in \([16]\) and \([17]\). In fact, the topology and evolution of the network is associated with the stimuli \( s \), while the control unit defines all possible \( \delta_{\alpha} \in \Delta \) in the sense that those can be obtained by applying a certain signal \( s_{\alpha} \) (which selects the index vector \( p_{\alpha} \)) to the network. The network evolution then determines \( x' \) while \( \beta \) and \( p_{\beta} \) (or better \( s_{\beta} \)) are defined by the control unit for the next processing step.

This more physical description points out a relevant peculiarity of the UMM. In order to implement the function \( \delta_{\alpha} \) (i.e., the computation) the control unit works only on (sends the stimuli \( s \) to) \( x(p_{\alpha}) \), and the memprocessor network under this stimulus changes the states of \( x(p_{\alpha}') \) into \( x'(p_{\alpha}') \). Therefore, even if \( \text{dim}(p_{\alpha}) = 1 \), which is the case of the most simple control unit acting on only one memprocessor, we can still have intrinsic parallelism.

### B. Proof of universality

In order to demonstrate the universality of UMMs we provide an implicit proof: we prove that a UMM can simulate any UTM, being this a sufficient condition for universality.

Proving that the UMM can simulate any UTM is actually quite a simple task. We refer to the definition \([1]\) of UTM given in section \([1]\) First, we take a UMM having the memprocessor states defined by \( M = Q \cup \Gamma \). One memory cell is located by the pointer \( j_0 \), while the (infinite) remaining cells are located by the pointer \( j = \ldots , -k , \ldots , -1, 0, 1, \ldots , k , \ldots \). We further define the array of pointers \( p \) (unique element of \( \mathcal{P} \)) defined by \( p = \{ j_0, j \} \). We use the cell \( j \), to encode the state \( q \in Q \), and in the other cells we encode the symbols in \( \Gamma \).

We now take \( \Delta \) to be composed by only one function

\[
\delta(x(p)) = (x'(p), p'),
\]

where we have suppressed the output index \( \beta \) because the function is only one. The new states \( x' \) written by \( \delta \) are written according to the table of the UTM (i.e., according to \( \delta \) of Eq. \([2]\), and in particular in \( x'(j_0) \) we find the new state the UTM would have, and in \( x(j) \) we find the symbol the UTM would write on the tape. Finally, the new pointer \( p' \) is given by \( p' = \{ j_0, j' \} \) where \( j' = j + 1 \) if \( \delta \) of UTM requires No shift, \( j' = j + 1 \) if Right shift, and \( j' = j - 1 \) if Left shift. Finally, following this scheme, writing on \( x(j_0) \) the initial state \( q_0 \) and the initial symbols \( \Sigma \) where required, the UMM with \( \Delta = \delta \) simulates the UTM with \( \delta \).

We have thus shown that a UMM is Turing-complete, namely it can simulate any Turing machine (whether deterministic or not). Note, however, that the reverse is not necessarily true. Namely, we have not demonstrated that a UTM can simulate a UMM, or, equivalently, we have not demonstrated that a UMM is Turing-equivalent. It is worth pointing out that, if we could prove that a UMM is not Turing-equivalent, some (Turing) undecidable problems, such as the halting problem \([2]\), may find solution within our UMM paradigm, thus contradicting the Church-Turing hypothesis \([2]\). Although this is an intriguing—albeit unlikely—possibility, we leave its study for future work.

### V. Properties of UMMs

#### A. On the parallel computing of UMMs

Parallelism in computing is an important issue from both a theoretical and a practical point of view. While the latter is more important for algorithm implementation in actual parallel architectures—multi-core CPU, CPU or GPU clusters, vector processors, etc. (see top panel of Figure \([5]\) for a sketch)—the former approach is essential in complexity theory. Roughly speaking, practical parallel computing involves a fixed number of processing units working in parallel, or a number growing at most polynomially with respect to the dimension of the input. This means that the NP problems still have a NP solution when implemented in practical parallel architectures.

On the other hand, the UMM approach to parallel computing can account for a number of processing units working in parallel that can grow also exponentially, if required. In order to understand this concept better we first briefly discuss two important and representative types of parallel machines before discussing the parallelism characterizing the UMM.

The first machine we consider is the Non-Deterministic Turing Machine (NTM) \([32]\). An NTM differs from a (deterministic) Turing machine (TM) for the fact that, in general, the transition function \( \delta \) does not have a uniquely specified three-tuple \( (q', \gamma, s') \in Q \times \Gamma \times \{ L, N, R \} \) for each \( (q, \gamma) \in Q \times \Gamma \times \{ L, N, R \} \). Therefore, unlike the TM, the NTM needs to be coupled with a way to choose among the possible actions of \( \delta \). This can be done in two different (equivalent) ways: either there is an oracle that picks the transition that eventually leads to an accepting state—if there is such a transition—or the machine branches into many paths each of

\[1\] Of course, the actual implementation of a UMM will limit this continuous range to a discrete set of states whose density depends on the experimental resolution of the writing and reading operations.
them following one of the possible transitions [32]. The second interpretation of a NTM is that of a parallel machine with an exponentially growing number of processing units at each level of the solution tree [32]. Clearly, the NTM is only an ideal model, impossible to reproduce in practice. Nevertheless, it is of great importance because the most famous unsolved question in Computer Science, the NP=P problem, is directly related to the question of whether the (deterministic) TM can simulate in polynomial time a NTM.

The second machine that boasts parallelism is the Quantum Turing machine (QTM) [35]. The QTM is an ideal machine used to model the behavior of a possible Quantum Computer (QC). One of the essential differences from the classical TM is that a QTM operates on a superposition of quantum states, each of them encoding a certain amount of data. For example, in the most famous algorithm for quantum computation, the Shor’s algorithm for integer factorization [36], [37], the QC employs a registry made of $n$ qubits encoding a superposition of $2^n$ states. In this way, using quantum gates, a QC can process at the same time $2^n$ states by using only $n$ qubits. Therefore, a QTM is a massively-parallel machine that can process at the same time an exponential number of states using a memory that grows linearly. However, even with its massive parallelism, it is not yet proven that a QTM is equivalent to an NTM [38]. (Note that claims to the contrary have been disproved [38].) On the other hand, it is conjectured but not proven that the NTM is a much more powerful machine than a QTM [38]. For example, NTMs can solve NP-complete problems in polynomial time, but there is no evidence that QTMs could accomplish the same task.

Now, let us discuss the parallelism characterizing the UMM and the computation power arising from it. Following the sketch in the bottom panel of Figure 3 and Figure 4, the intrinsic parallelism characterizing UMMs is the consequence of the physical coupling between memprocessors. When the control unit sends an input signal to one or a group of memprocessors, the coupling induces dynamics to a larger group of memprocessors. Therefore the computation involves not just the memprocessors directly connected to the control unit, but up to the entire network. In principle, with only one input signal we can then induce massively-parallel computation in the entire network as also discussed in Sec. [V-A].

This is not the only consequence of the physical coupling among memprocessors. As we discuss in the Sec. VI, using the coupling between memprocessors, we can encode information not necessarily proportional to the number of memprocessors, but up to an exponential amount in terms of the number of memprocessors. Therefore, by using the intrinsic parallelism, we can also manipulate the information encoded in the memprocessor network all at once. As we prove in the next sections, the UMMs – thanks to their intrinsic parallelism – can solve NP-complete problems in polynomial time using an exponential number of memprocessors or, boosted by the information overhead, using only a polynomial number of memprocessors.

B. UMMs solve NP-complete problems in polynomial time

We consider an NP-complete problem whose known fastest solving algorithm requires a solution tree exponentially growing with the dimension $n$ of the input. Such algorithm, implemented in a deterministic TM would require exponential time (steps) with respect to $n$ in order to be solved.

We consider a formal description of the solution tree assuming that the branch of the tree leading to the solution takes a polynomial number of iterations with respect to $n$, i.e., $N_s = P(n)$ being $N_s$ the number of iterations and $P(n)$ a polynomial function. At each iteration $i$ we can assume that each branch splits into $M_i$ new branches, so the complete solution tree has a total number of nodes $N_{\text{nodes}} \leq \sum_{k=1}^{N_s} \prod_{i=1}^{k} M_i$ (where the situation “<” arises when some branches end with no solution before the $P(n)$-th iteration).

Following this picture, if the simplest tree has an average number $M$ of branch splits, then the time required by a TM
to explore the solution tree, that is proportional to the number of nodes $N_{nodes}$, is of the order of $M^N = M^{P(n)}$, i.e., exponentially growing with respect to the dimension $n$ of the input. On the contrary, we now prove that the UMM we have introduced in Sec. [IV-A] can find the solution within a time proportional to $P(n)$.

In order to prove this claim, we consider the UMM that operates following the scheme of figure [4]. The control unit sends a signal input to a group of interconnected memprocessors encoding the iteration $i$ of the solution tree to compute the iteration $i + 1$ all at once. Thus the entire computation process can be formalized following the scheme of Figure [5].

We consider a set $D$ of functions $\delta_{\alpha}$ with $\alpha = 1, ..., P(n)$ such that $\delta_{\alpha}([x(p_{\alpha})]) = ([x'(p_{\alpha + 1})], \alpha + 1, p_{\alpha + 1})$ where $x(p_{\alpha})$ encodes all the nodes belonging to the iteration $\alpha = i$ of the solution tree into at most $\dim(p_{\alpha}) \leq \prod_{i=1}^\alpha M_i$ memprocessors, and $x'(p_{\alpha + 1})$ encodes all the nodes belonging to the iteration $\alpha + 1 = i + 1$ of the solution tree into at most $\dim(p_{\alpha + 1}) \leq \prod_{i=1}^{\alpha + 1} M_i$ memprocessors. It is also worth noticing that in the UMM case, the situation “<” does not arise only when some branches end with no solution before the $P(n)$–th iteration. Rather, by exploiting the information overhead we discuss later and sketched in the right panel of Figure [5], the data encoded into $N_{nodes\beta} \leq \prod_{i=1}^\beta M_i$ can be encoded in a number of memprocessors $\dim(p_{\beta}) \leq N_{nodes\beta}$ (see section [VI]).

Since $\delta_{\alpha}$ corresponds to only one computation step for the UMM, it will take a time proportional to $P(n)$ to find the solution. Therefore, in principle, the UMM can solve an NP–complete problem in a time proportional to $P(n)$, i.e., the UMM has the same computational power of a NTM.

Using this simplified scheme for the solution of an NP–complete problem, we can highlight the fundamental difference between the UMM and the NTM. The NTM (in the “exploring-all-possible-paths” picture) needs, in principle, both a number of processing units and a number of tapes exponentially growing in order to explore all possible solution paths [32]. On the contrary, a UMM, in order to find a solution of an NP–complete problem in polynomial time, needs only a number of memprocessors at most exponentially growing, since it can process an entire iteration of the solution tree in just one step. However, there is yet the final property of UMMs, the information overhead, that allows us to reduce this exponentially growing number substantially, even to a polynomial order, making the practical implementation of a UMM even more appealing. Note also that the above proof is valid for any problem whose solution can be cast into an exponentially growing tree, whether the problem is NP–complete or NP–hard. In Sec. [VII] we indeed provide the polynomial solution of the sub-set sum problem in both its decision and optimization versions.

VI. INFORMATION OVERHEAD

As already anticipated, the intrinsic parallelism and functional polymorphism we have discussed above are not the only features that resemble those employed by a typical brain. Indeed, a UMM boasts an additional property we name information overhead. In order to explain this third peculiar feature, we first recall how the information is stored in modern computers. In these devices, the information is encoded in bits, which ultimately correspond to the threshold state of some electronic device (patterns of magnetization in a magnetizable material, charge in capacitors, charge in a Floating-Gate MOSFET, etc.) [6]. Irrespective, the memory cells in modern computers are always understood as independent, non-interacting entities. Therefore, the quantity of information that
can be stored is defined from the outset and can not exceed an amount proportional to the number of employed memory cells.

On the other hand, if the memory cells are connected or can interact in some ways, this limitation does not hold. In fact, although the issue is still under debate, it is thought that the brain stores information by changing the way in which the neurons communicate through their synapses \[39\]. Therefore, the storing of information is not a local action involving a single neuron or synapse. Rather it is a collective behaviour of a group of interacting neurons \[40\].

Following this picture, the brain information storage capacity cannot be simply proportional to the number of neurons or synapses: a more complex relation must exist. For example, a person affected by hyperthymesia is not able to erase his/her memory \[41, \ 42\], thus demonstrating the capability of our brain to store such a large quantity of information whose limits, currently, cannot even be estimated. In other words, it is reasonable to assume that our brain is capable of some sort of information overhead: it can store a quantity of information not simply proportional to the number of neurons or synapses.

The UMMs we have defined satisfy a similar property. In order to clarify this issue, we describe two examples of information overhead arising in interconnected memprocessors easily reproducible with memelments, e.g., memristors or any other memory cell. Here, we do not specify the actual physical coupling between the memprocessors, just note that it is some physically plausible interaction. For instance, this interaction could be simply provided by the direct local wiring between the memprocessors as we do in Sec. \[VII\] which indirectly gives rise to the non-local collective dynamics as determined by Kirkshoff’s laws.

A. Quadratic Information Overhead

Formally, the information stored in a message \(m\) can be quantified by the Shannon’s self-information \(I(m) = -\log_2 p(m)\) where \(p(m)\) is the probability that a message \(m\) is chosen from all possible choices in the message space \(M\) \[43\]. The base of the logarithm only affects a scaling factor and, consequently, the units in which the measured information content is expressed. For instance, the logarithm base 2 measures the information in units of bits.

Now, let us consider the message space composed by messages \(m\) formulated in the following way: given the set \(G\) composed of \(n\) different integer numbers with sign and considering all the possible sums of \(2, 3, ..., k\) of them taken only once and \(k \leq n\). We then define each message \(m\) as that containing both the numbers that we are summing and their sum. Therefore, the message space \(M\) is composed of \(\sum_{j=2}^{k} \binom{n}{j}\) equally-probable messages \(m\) with Shannon’s self-information \(I(m) = \log_2 \sum_{j=2}^{k} \binom{n}{j}\).

Let us now consider \(k\) memprocessors capable of storing any integer number belonging to \(M\) and we consider two different scenarios: \(i)\) \(k\) independent memprocessors acting as simple memory cells, and \(ii)\) \(k\) memprocessors connected in series as in figure 6. In the first scenario, by defining \(\lfloor x \rfloor\) the floor function operator that rounds \(x\) to the nearest integer towards 0, we can store at most \(\lfloor k/3 \rfloor\) messages \(m\), i.e., the messages \(m\) containing two numbers (i.e., the smallest number of numbers) and their sum.

On the contrary, in the second scenario, by storing \(k\) different numbers from the \(n\) numbers, we can also directly read their sums as in figure 6. Therefore, in this case we can store \(n(n - 1)/2\) messages \(m\), namely a quadratic (in the memprocessors) number of messages.

Form this simple example we can already highlight several points. First of all, we have shown that by using interconnected cells we can store (compress) a quadratic amount of information with respect to the number of memprocessors employed. This information overhead is essentially a data compression \textit{that is already present directly in memory}. In fact, we can store the same amount of information in the \(k\) independent memprocessors provided we couple them with a CPU performing sums, i.e., standard data compression requiring memory plus a program implemented in a CPU to decompress data.

We can however easily implement in hardware the interconnected memprocessors using, e.g., memristor crossbars \[18\], each memristor storing a number in \(G\) that is linearly encoded through the resistance of the memristor. In order to read the sum we can simply apply a small voltage to the interconnected memprocessors and measure the current which is proportional to the inverse of the sum of the resistances involved. It is worth noticing that this practical implementation of information overhead can already be used to speed up typical NP-complete problems such as the subset-sum problem (SSP) we discuss below in Sec. \[9\]. However, with this strategy the number of memprocessors can only be reduced polynomially. Although this is not a formal problem, it is definitely a practical limitation.

B. Exponential Information Overhead

Another example of information overhead that we present allows instead an exponential reduction of memprocessors. To illustrate what we mean by this, let us consider a set of \(n\) memprocessors defined by \(x(p) = (x(j_1), \ldots, x(j_n))\). Each memprocessor state \(x(j) = u_j\) can store data encoded into its internal state vector \(u_j \in M_2\). We describe the internal state \(u_j\) as a vector with (possibly infinite) components \(\{u_j\}_h\) and we assume the memprocessor as a two terminal “polarized” device in the sense that the right terminal and the left terminal, when connected to other memprocessors, physically interact in different ways, thus we label as “in” and “out” the two different terminals (see left panel of figure 7).

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig6.png}
\caption{System of \(k\) connected memprocessors in series. By using intermediate connections it is possible to directly measure the sum of intermediate cells.}
\end{figure}
We assume the blank state of the memprocessors corresponds to all components of $u_j$ equal to 0 (empty circles of figure 7). In order to store one datum we set one of the components of $u_j$ different from 0 (full circles of figure 7), and any memprocessor can simultaneously store a finite number of data. Moreover, we assume that there exists a device that, once connected to a memprocessor, can read each single component of $u_j$.

The former description of the memprocessor provides the picture of a single non-interacting memprocessor. However, we complete this picture by including a physical interaction scheme between different memprocessors. We consider two memprocessors connected through the “out” and “in” terminals of the first and second memprocessor, respectively. In addition, we assume that the device that reads the state of a single memprocessor can be used to read the global state of the two connected memprocessors as well. Therefore, the device reads the global state of the two connected memprocessors that we describe as $u_{j_1,j_2} = u_{j_1} \circ u_{j_2}$ where $\circ : \mathbb{R}^d \times \mathbb{R}^d \rightarrow \mathbb{R}^d$ is a commutative and associative operation with $d = \dim(u_j)$ and it is defined through

$$\{u_{j_1} \circ u_{j_2}\}_{h \circ k} = \{u_{j_1}\}_h \ast \{u_{j_2}\}_k \quad (18)$$

where $\ast : \mathbb{Z} \times \mathbb{Z} \rightarrow \mathbb{Z}$ and $\ast : \mathbb{R} \times \mathbb{R} \rightarrow \mathbb{R}$ are two commutative and associative operations with properties $h \ast 0 = h$ and $x \ast 0 = x$. Although one can envision non-commutative and non-associative types of physical interactions, for the sake of simplicity we restrict our analysis only to commutative and associative operations, leaving the more complex ones for future studies.

In addition, if there are two couples of indexes $h,k$ and $h',k'$ such that $h \ast k = h' \ast k'$, then $\{u_{j_1,j_2}\}_{h \ast k} = \{u_{j_1} \circ u_{j_2}\}_{h \ast k} \oplus \{u_{j_1} \circ u_{j_2}\}_{h' \ast k'}$ where $\oplus : \mathbb{R} \times \mathbb{R} \rightarrow \mathbb{R}$ is another commutative, associative operation such that $x \oplus 0 = x$. Since all the defined operations are commutative and associative, we can straightforwardly iterate the procedure to any number of connected cells (see right panel of figure 7 for a sketch of three interacting memprocessors).

Given a set $G = \{a_1, \ldots, a_n\}$ of integers we now define a message $m = \{a_{\sigma_1} \ast \cdots \ast a_{\sigma_2}\} \cup \{a_{\sigma_1}, \ldots, a_{\sigma_2}\}$ where $\{\sigma_1, \ldots, \sigma_k\}$ is a set of indexes taken from all possible different subsets of $\{1, \ldots, n\}$ so that the message space $M$ is composed of $\sum_{j=0}^{n} \binom{n}{j} = 2^n$ equally-probable messages $m$ with Shannon’s self-information $I(m) = \log_2(2^n) = n$. Now, taking $n$ memprocessors, for each one of them we set only the components $u_{j_0}$ and $u_{j_0, h}$ different from zero with $h \in \{1, \ldots, n\}$. In this way, in each memprocessor one element of $G$ is encoded. On the other hand, by following the picture of physically interconnected memprocessors described previously, if we read the global state of the interconnected cells we find all possible messages $m$, which means that $n$ interconnected memprocessors can encode (data compress) $2^n$ messages simultaneously.

In section VII-B we discuss how to use in practice this exponential information overhead to solve the subset-sum problem in polynomial time using only $n$ memprocessors. Here, we stress again that, even if we have used operations to define both the quadratic and the exponential overhead, these operations represent the physical coupling between the different memprocessors and not the actual computation defined by the functions $h_k$ (Eq. (16)) of a UMM. In fact, while the computation changes the state of some (or all) memprocessors, the information overhead – which is related to the global state of physically interacting memprocessors – does not.

### VII. The Subset-Sum Problem

In order to exemplify the computational power of a UMM, we now provide two actual UMM algorithms to solve the NP-complete subset-sum problem (SSP), which is arguably one of the most important problems in complexity theory [32]. It can be defined as follows: if we consider a finite set $G \subset \mathbb{Z}$ of cardinality $n$, we want to know whether there is a non-empty subset $K \subseteq G$ whose sum is a given number $s$.

#### A. DCRAM-based algorithm

In order to show the first practical algorithm implementation that can solve in polynomial time the SSP using only $n$ memprocessors. This machine is inspired by the Dynamic Computing Random Access Memory (DCRAM) introduced by the authors in Ref. [30]. In the present work, we employ an idealization of a DCRM in the sense that we do not specify the actual electronic devices capable of reproducing exactly the machine we are going to present. Nevertheless, this does not exclude the possibility that such a machine can be realized in practice. Moreover, while the DCRM designed in [30] is digital, i.e., it has the state of a single memprocessor belonging to $M = M_d$, the current DCRM has memprocessor states belonging to $M = M_s$ in order to perform the operation $\chi$ described in Fig. 8-(a). It is worth noticing that, even if $\chi$ is the analog computation between integers, it can be simply realized with boolean gates, so, in principle, even with digital DCRM-inspired machines.

The DCRM-inspired machine has memprocessors organized in a (possibly infinite) matrix architecture. Through a control unit we can perform three possible operations (see figure 8).
\( \chi \): This is the actual computation. By using the activation lines (similar to word lines of standard DRAM) to select the rows to be computed, and applying a signal at two selected columns (see Fig. 8-(a)), the memprocessors belonging to the same row change their states according to the operation in Fig. 8-(b), i.e., the datum stored in the first column is summed to the data stored in the other columns. Therefore, through this operation, by just applying a single signal, we can compute in a massively-parallel way the data stored in a submatrix of the DCRAM-inspired machine. It is worth noticing that during the computation no data moves, and the control unit does not have any information of the data stored in the memory.

\( \mu \): This is the movement of data. The control unit selects two columns and through read and write lines the data flow from one column to the other. Also in this case, the control unit does not necessarily read and write the data, but it actually connects the cells allowing for data flow.

\( \rho \): This operation is similar to \( \mu \) but it replicates one data column.

Combining these three functions we obtain the transition function \( \delta = \mu \circ \chi \circ \rho \) of the machine and we can solve the SSP using only \( n - 1 \) iterations of \( \delta \). In order to show how it works, in Fig. 9 the algorithm implementation for a set \( G \) of cardinality 5 is reported. At the first step the machine computes the sums of all the possible subsets with cardinality \( n - 1 \). Here, if none is the given number \( s \), the procedure continues and the sums of all the possible subsets with cardinality \( n - 2 \) are calculated. The procedure ends if it finds some subsets summing to \( s \), or if it reaches the \( n - 1 \)-th iteration.

From this scheme it is simple to evaluate the total number of memprocessors needed at each iteration. In fact, considering the iteration \( k \), we need \( \binom{n}{k} (n - 2 - k) \) memprocessors. Using the Stirling formula and observing that the binomial \( \binom{n}{k} \) has maximum in \( k = n/2 \) (for odd \( n \), \( k = (n \pm 1)/2 \)), the maximum number of memory cells required by the algorithm is about \( (n/2\pi)^{1/2}2^{n-1} \) showing the exponential growth of the number of memory cells.

B. Exponential information overhead-based algorithm

Another algorithm to solve the SSP can be obtained by exploiting the exponential information overhead discussed in section \( \text{[VI-B]} \). Here, we discuss both its numerical implementation that provides the computational complexity in the context of a classical UTM, and its hardware implementation that gives the computational complexity within the UMM paradigm, and show that this algorithm requires only a linear number of interacting memprocessors.

1) Algorithm for the solution of the SSP:

Let us consider a set of integer numbers \( G = \{a_1, \ldots, a_n\} \)
and the function
\[ g(x) = -1 + \prod_{j=1}^{n} (1 + e^{i2\pi a_j x}). \tag{19} \]

By expanding the product in (19) it is then obvious that we can store all possible \(2^n - 1\) products
\[ \prod_{j \in P} e^{i2\pi a_j x} = \exp \left[ i2\pi x \sum_{j \in P} a_j \right], \tag{20} \]
where \(P\) is a set of indexes taken from all possible different non-empty subsets of \(\{1, \ldots, n\}\). This implies that the function \(g(x)\) contains information on all sums of all possible sub-sets of \(G\).

Let us now consider the discrete Fourier transform (DFT)
\[ F(f_h) = \mathcal{F}\{g(x)\} = \frac{1}{N} \sum_{k=1}^{N} g(x_k) e^{i2\pi f_h x_k}. \tag{21} \]

If this DFT has a sufficient number of points, it will show a peak in correspondence of each \(f_h\), with magnitude equal to the number of sub-sets of \(G\) that sum exactly to \(f_h\).

2) Numerical implementation:
The first step for an efficient and accurate solution of (21) requires the determination of the maximum frequency \(f_{\text{max}}\) such that \(F(f > f_{\text{max}})\) and \(F(f < -f_{\text{max}})\) are negligible [34]. This maximum frequency can be easily determined in our case. By defining \(G_+\) the sub-set of positive elements of \(G\), and \(G_-\) that of negative elements, we have
\[ f_{\text{max}} = \max \left\{ \sum_{j \in G_+} a_j, -\sum_{j \in G_-} a_j \right\}, \tag{22} \]
which can be approximated in excess as
\[ f_{\text{max}} < n \max \{|a_j|\}. \tag{23} \]

We note again that the transform of \(g(x)\) will show peaks in correspondence to the natural numbers in between \(-f_{\text{max}}\) and \(f_{\text{max}}\). Since the elements of \(G\) are integers, \(g(x)\) is a periodic function with period \(T\) at most equal to 1. In this case, we can then apply the discrete fast Fourier transform (FFT) which, according to the theory of DFTs and the sampling theorem [34], provides the exact spectrum of \(g(x)\). Indeed, from the theory of harmonic balance [34], we can define a number of points
\[ N = 2f_{\text{max}} + 1, \tag{24} \]
and divide the period \(T\) in sub-intervals of amplitude \(\Delta x = N^{-1}\), namely
\[ x_k = \frac{k}{N} \quad \text{with} \quad k = 0, \ldots, N - 1, \tag{25} \]
and then obtain the DFT of \(g(x_k)\) using the FFT algorithm.

In order to determine the complexity of our numerical algorithm let us indicate with \(n\) the number of input elements and with \(p\) the precision of the problem, namely the number of binary values that it takes to state the problem. In our case then, \(n\) is the cardinality of \(G\), while \(p\) is proportional to the number of discretization points \(N\). In order to determine \(g(x)\) for every \(x_k\) we then need to compute \(np\) complex exponentials and \(np\) multiplications of complex variables. Therefore, a total of \(4np\) floating-point operations.

Instead, in order to determine the DFT we need to make the following important observation. If we want to determine only one sum \(f_h = s\), we can use Goertzel’s algorithm [44] which is linear in \(p\). Therefore, the algorithm to solve the SSP for a given sum \(s\) requires \(O(np)\) operations: it is linear in both \(n\) and \(p\). However, we point out that \(p\) is not bounded by \(n\) and it depends on \(N\), which scales exponentially with the number of bits used to represent \(f_{\text{max}}\).

On the other hand, if we want to compute the solution for all \(s\) values simultaneously we need to use the FFT which scales as \(O(p \log(p))\). Therefore, the final order of complexity is \(O((n + \log(p))p)\). Note that the best algorithm for large \(p\) belongs to the class of “dynamic programming” algorithms which are order \(O(np)\) [45]. Therefore, our numerical method has the same complexity as the best known algorithm. However, even if the computational complexity class is the same, for practical Turing computation dynamic programming is better because it involves only sums of integers and boolean logic. On the other hand, our algorithm is extremely important because it can be directly implemented in memcomputing architectures reducing the UMM complexity to \(O(n)\) as we show in the next section. Finally, in figure 10 we show a characteristic sample of solutions of the SSP obtained with the proposed method and the dynamic programming for a set
Controlled Inverting Differentiator  
Analog Multiplier  
Difference Amplifier  
Summing Amplifier  
Complex Voltage Multiplier (CVM)  

\[
\begin{align*}
V &= 1 + \cos(\omega_1 t) \\
&= 1 + \cos(\omega_2 t) \\
&= 1 + \cos(\omega_3 t) \\
&= 1 + \cos(\omega_4 t)
\end{align*}
\]

\[
\begin{align*}
\text{Im}\left\{ (1 + e^{i\omega_1 t})(1 + e^{i\omega_2 t})(1 + e^{i\omega_3 t})(1 + e^{i\omega_4 t}) \right\} &= -1 + \Re\left\{ (1 + e^{i\omega_1 t})(1 + e^{i\omega_2 t})(1 + e^{i\omega_3 t})(1 + e^{i\omega_4 t}) \right\}
\end{align*}
\]

\[
V = 1
\]

\[V = 1 + \cos\left(\sum_{j=1}^{4} \omega_j t\right)\]

3) Hardware implementation:

Before describing the actual hardware implementation of the method, we briefly set a connection between the exponential information overhead of section VI-B and the general framework of the method in section VII-B1.

We consider memprocessors with infinite discrete states belonging to \( M = M_a \). The first step is to notice that the state vector \( u_j \) associated with one memprocessor can be taken as the vector of the amplitudes of one of the products in (19), thus \( u_j \) has \( u_{j_0} = 1 \) and \( u_{j_{n_j}} = 1 \), while all the other components are 0. Then, the operation defined in section VI-B reduces to the standard sum and multiplication, in particular \( \ast \) and \( \oplus \) are sums and \( \ast \) is a multiplication. Thus, these simple relations prove that there is an ideal system of interconnected memprocessors that can solve the SSP by using only a linear number of memprocessors exploiting the exponential information overhead.

In addition to this, we can also devise a system of interconnected memprocessors—this can be easily fabricated in the laboratory—that works exactly as we want. In order to prove this claim we define a complex voltage multiplier (CVM) as described in figure 11. This is a two-port device, the first and second ports work as the “in” and “out” terminals of the memprocessor described in section VI-B. The CVM can be easily built using standard amplifiers as described in figure 11. Each CVM is connected to a generator that applies a voltage \( v_j = 1 + \cos(\omega_j t) \), where the frequencies \( \omega_j \) are related to the elements of \( G \) through \( \omega_j = 2\pi a_j \). The state of a single isolated CVM-memprocessor can be read by connecting the first port to a DC generator of voltage \( V = 1 \) and the other port to a signal analyzer that implements in hardware the FFT. On the other hand, by connecting the CVM-memprocessors as in figure 11 and using a signal analyzer at the last port as in figure 12 we can directly read the solution of the SSP.

We make now two important remarks on the complexity of this approach. The first concerns the execution time. Indeed, in the numerical implementation, the period \( T \) of the function (19) is only a mathematical entity, and what matters is the number of points \( N \) used to sample \( T \). On the contrary, in the hardware implementation, what matters for the execution time (excluding the FFT) to obtain (19) is only \( T \), which is bounded because it is 1 (in the appropriate unit), so that it is independent of both \( n \) and \( p \). Secondly, in order to perform the FFT with a signal analyzer we would in principle need a number of time points of the order of \( N \) evaluated as in section VII-B2. This would be a problem even for a signal analyzer because \( N \) grows unbounded. However, there is a straightforward solution to this (generally embedded directly in the signal analyzers as depicted in Figure 12): before connecting the signal analyzer we interpose a band-pass filter to select only a range of frequencies so the time samples needed by the signal analyzer will be only a bounded number independent of both \( n \) and \( p \). Therefore, this approach solves the SSP in just one step for any \( s \in \mathbb{Z} \), when implemented in hardware.

Finally, it is worth noticing that we have the solution of the decision version of the SSP problem, i.e., we only know whether there is a subset that sums to \( s \), but we do not know...
which actual subset is the solution. Knowing the particular subset that sums to \( s \) is the optimization version of the SSP and is not NP-complete but NP-hard (that is actually harder to solve!) \[32\].

However, it is easy to show that the hardware implementation we propose is able to solve also the latter version of the SSP in polynomial time. In fact, to find a particular subset that sums to \( s \) we can read the frequency spectrum around \( s \) for different configurations of the machine: in the 1st configuration we use all CVMs turned on. In the 2nd configuration we set \( \omega_1 = 0 \). If the amplitude corresponding to \( s \) is \( > 1 \) we let \( \omega_1 = 0 \) for the next configuration, otherwise we turn on again \( \omega_1 \) and \( a_1 = \omega_1/(2\pi) \) is an element of the subset we are searching for. In the 3rd configuration we repeat the same procedure of the 2nd but with \( \omega_2 \). By iterating this procedure for a number of times \( \leq n \), we then find one of the subsets (if not unique) that sums to \( s \).

**VIII. Conclusions**

In summary, we have introduced the concept of universal memcomputing machines, as a class of general-purpose machines that employ memory elements to both store information and process it (memprocessors). The UMMs have unique features that set them apart from Turing machines and which mirror those of the brain: they boast intrinsic parallelism (their transition functions act simultaneously on all memprocessors), functional polymorphism (there is no need to change topology to compute different functions, just the input signals), and information overhead (physically interconnected memprocessors allow for storing and retrieval of a quantity of information which is not simply proportional to the number of memory cells). These last two features, in particular, are unique to UMMs and cannot be found in any other machine that has been suggested in the past, like, e.g., the liquid machine. In addition, although all these features follow from the definition of UMMs they are quite distinct properties.

These general features allow UMMs to solve NP-complete problems in polynomial time with or without the need of an exponentially increasing number of memprocessors, depending on whether information overhead is used (without) or not (with). Although we have not proved that they can solve some (Turing) undecidable problems, such as the halting problem, they represent a powerful computing paradigm that if realized in practice can overcome many limitations of our present-day computing platforms such as the von Neumann bottleneck and the ever-increasing energy requirements of Turing-based machines.

Indeed, a practical implementation of a UMM can already be accomplished by using memelements such as memristors, memcapacitors or meminductors, although the concept can be implemented with any system with memory, whether passive or active. For instance, in this work we have proposed a simple topologically-specific architecture that, if realized in hardware, can solve the subset-sum problem in just one step with a linear number of memprocessors.

It is finally worth mentioning that although we have taken inspiration from the brain to formalize the concept and properties of universal memcomputing machines, we expect their practical realization to shed valuable light on the operation of the brain itself. We therefore hope our work will motivate both theoretical and experimental studies aimed at developing memcomputing machines with computational power and features that are getting tantalizing closer to those of the brain.

**IX. Acknowledgments**

We thank L. Thiele, Y.V. Pershin and F. Bonani for useful discussions. This work has been partially supported by the Center for Magnetic Recording Research at UCSD.

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