On the TOCTOU Problem in Remote Attestation

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Abstract—Much attention has been devoted to verifying software integrity of remote embedded (IoT) devices. Many techniques, with different assumptions and security guarantees, have been proposed under the common umbrella of so-called Remote Attestation (RA). Aside from software integrity verification and malware presence detection, RA serves as a foundation for many security services, such proofs of as memory erasure, system reset, software update, and runtime verification. All prior RA techniques verify the remote device’s state at the time when RA functionality is executed, thus providing no information about the device’s state before current RA execution or between consecutive RA executions. This implies that presence of transient malware may be undetected. In other words, if transient malware infects a device, performs its nefarious tasks, and leaves before the next attestation, its temporary presence will not be detected. This important problem, called Time-Of-Check-Time-Of-Use (TOCTOU), is well-known in the research literature and remains unaddressed in the context of RA.

In this work, we propose Remote Attestation with TOCTOU Avoidance (RATA): a provably secure approach to address the RA TOCTOU problem. With RATA, even malware that erases itself before execution of the next RA, can not hide its ephemeral presence. RATA targets hybrid RA architectures (implemented as Hardware/Software co-designs), which are aimed at low-end embedded devices. We present two alternative techniques – RATA_A and RATA_B – suitable for devices with and without real-time clocks, respectively. Each is shown to be secure and accompanied by a publicly available and formally verified implementation. Our evaluation demonstrates low hardware overhead of both techniques. Compared with current RA architectures – that offer no TOCTOU protection – RATA incurs no extra runtime overhead. In fact, RATA substantially reduces computational costs of RA execution.

I. INTRODUCTION

In the last two decades, in many aspects of everyday life, our society is becoming increasingly surrounded by, and dependent upon, a multitude of small and specialized computing devices that perform a wide range of functions. They are often referred to as embedded, “smart”, CPS or IoT devices, and they range very widely in terms of computing abilities. However, regardless of the purpose and resources, they have become popular targets for malicious exploits and malware.

At the low-end of the spectrum, such devices are designed with strict constraints on monetary cost, physical size, and energy consumption. Two prominent examples are: TI MSP430 [1] and Atmel ATMega AVR [2]. It is unrealistic to expect such devices to have sophisticated means (similar to those on laptops or smartphones) to prevent compromise or malware presence via sophisticated security tools. In this landscape, Remote Attestation (RA) emerged as an inexpensive means to detect malware presence on remote low-end devices. In addition, RA serves as a foundation for other important security services, such as provable software updates [1], control-flow integrity verification [2], and proofs of remote software execution [3]. Loosely speaking, RA allows a trusted entity, called a Verifier (Vrf), to ascertain memory integrity of an untrusted remote device, called Prover (Prv). As shown in Figure 1, RA is typically realized as a (deceptively) simple challenge-response protocol:

1) Vrf sends an attestation request with a (random) challenge (Chal) to Prv. This request might also contain a token derived from a secret that allows Prv to authenticate Vrf.
2) Prv receives the request and computes a Chal-based authenticated integrity check over its memory. The attested memory region might be pre-defined (e.g., entire program memory), or explicitly specified in the request.
3) Prv returns the result to Vrf.
4) Vrf receives the result and checks whether it corresponds to a valid memory state.

![Fig. 1. Timeline of a typical RA protocol](http://www.ti.com/microcontrollers/msp430-ultra-low-power-mcus/applications.html)

The authenticated integrity check is typically implemented as a Message Authentication Code (MAC) over Prv’s attested memory region. However, computing a MAC requires Prv to have a unique secret key, denoted by K – a symmetric key shared with Vrf or a private key for which the corresponding public key is known to Vrf. (In the rest of this paper, we assume the former, even though the differences are insignificant.) K must reside in secure storage, inaccessible to any software running on Prv, except for privileged attestation code. Since the usual RA threat model assumes a fully compromised software state on Prv, secure storage implies some level of hardware support. Hybrid RA (based on hardware/software co-designs) [4, 5, 6, 7] is an approach particularly suitable for low-end embedded devices. In hybrid RA designs, the integrity ensuring function is implemented in software, while hardware controls execution of this software, detecting any violations that might cause unexpected behavior or K leakage. In a nutshell, hybrid RA provides the same security guarantees as (more expensive) hardware-based RA approaches (e.g., those based on a TPM [8]), while minimizing modifications to underlying hardware platform. We overview a concrete hybrid RA architecture in Section II-C.

[1] http://www.ti.com/microcontrollers/msp430-ultra-low-power-mcus/applications.html
[2] https://www.microchip.com/design-centers/8-bit/avr-mcus

http://www.ti.com/microcontrollers/msp430-ultra-low-power-mcus/applications.html
https://www.microchip.com/design-centers/8-bit/avr-mcus
Unfortunately, current hybrid RA architectures share a common limitation: they only measure \( \mathcal{P}_\text{rv} \)'s state at the time when RA code is executed by \( \mathcal{P}_\text{rv} \). They provide no information about \( \mathcal{P}_\text{rv} \)'s state before RA execution or its state between two consecutive RA executions. We refer to this problem as Time-Of-Check Time-Of-Use or TOCTOU. This problem has been widely discussed in the research literature \cite{9, 10, 11, 12, 13}. Nonetheless, it remains unsolved, leaving devices vulnerable to transient malware which erases itself either after completing its tasks, or upon detecting an incoming RA request.

In this paper, we study the TOCTOU problem and propose approaches to guarantee security against related attacks, without sacrificing security and performance of the underlying RA architecture. Our approach is rooted in the observation that current hybrid RA techniques use trusted hardware only to detect security violations that might compromise execution of RA software itself and taking action (e.g., resetting the device) if such a violation is detected. Whereas, RA’s main new feature is the use of a minimal (formally verified) hardware component to additionally provide historical context about \( \mathcal{P}_\text{rv} \)'s state, \( \mathcal{P}_\text{rv} \)'s memory state. This is achieved via secure logging of \( \mathcal{P}_\text{rv} \)'s memory before a violation is detected. Whereas, RA’s main new feature is the use of a minimal (formally verified) hardware component to additionally provide historical context about \( \mathcal{P}_\text{rv} \)'s state, \( \mathcal{P}_\text{rv} \)'s memory state. This is achieved via secure logging of \( \mathcal{P}_\text{rv} \)'s memory before a violation is detected.

This enables \( \mathcal{P}_\text{rv} \) to check authenticity and integrity of \( \mathcal{P}_\text{rv} \)'s memory modifications. This new feature is integrated seamlessly into the underlying RA architecture and the composition is shown to be secure. We believe this results in the following contributions:

- **RA TOCTOU-Security formulation**: We motivate and formalize TOCTOU in the context of RA. We define RA TOCTOU-Security using a security game (see Definition \[3\]) and discuss why current RA techniques based on consecutive self-measurements do not satisfy this definition. We believe this to be the first systematic treatment of this matter. Furthermore, we analyze practicality of consecutive self-measurement approaches and argue that using them to obtain TOCTOU-Security incurs extremely high runtime overhead, possibly starving benign applications on \( \mathcal{P}_\text{rv} \).

- **RA Design, Implementation & Verification**: Next, we propose two techniques – \( \text{RA}_A \) and \( \text{RA}_B \). \( \text{RA}_A \) assumes that \( \mathcal{P}_\text{rv} \) has a secure read-only Real-Time Clock (RTC) synchronized with \( \mathcal{P}_\text{rv} \). Since this assumption is unrealistic for many low-end \( \mathcal{P}_\text{rv} \)'s, we propose \( \text{RA}_B \) which avoids the need for a clock in return for authentication of \( \mathcal{P}_\text{rv} \)'s attestations requests; this feature is already included in several hybrid RA architectures. We also show that both proposed techniques satisfy the formal definition of TOCTOU-Security, assuming that their implementations adhere to a set of formal specifications, stated in Linear Temporal Logic (LTL). Finally, the implementation itself is formally verified to adhere to these LTL specifications, yielding security at both design and implementation levels. Our implementations (publicly available at \[14\]) target a real-world low-end microcontroller (MCU) – TI MSP430 – and are deployed using commodity FPGAs. Experimental results show low hardware overhead, affordable even for cost-sensitive low-end devices. They also require no extra runtime. In fact, we demonstrate that, most of the times, RA can significantly reduce overall RA runtime (see below).

- **RA Enhancements to RA and Related Services**: We discuss the implications of RA on RA and related services beyond TOCTOU-Security. In particular, we show that RA can, in most cases, reduce RA computational complexity from linear (in terms of attested memory size) to constant time, resulting in significant savings for RA and related services. We also discuss RA’s benefits for specialized RA applications: (i) real-time systems; and (ii) collective RA, where a multitude of provers need to be attested simultaneously.

A. Scope

**Detection Vs. Prevention**: As a detection-oriented security service, RA does not prevent future malware infections. Therefore, the term TOCTOU should be considered in retrospective. In particular, techniques presented in this paper allow \( \mathcal{P}_\text{rv} \) to understand “since when” \( \mathcal{P}_\text{rv} \)'s memory remained the same as reported in the present RA execution result. As discussed earlier, methods to prevent malware are either too expensive or too restrictive for low-end devices considered in this paper.

**Low-End Devices**: This work focuses on CPS/IoT/smart sensors and actuators (or hybrids thereof) with relatively low computing power. They are some of the smallest and weakest devices based on low-power single-core MCUs with only a few KBytes of program and data memory. Two prominent examples are: Atmel AVR ATmega and TI MSP430: 8- and 16-bit CPUs, typically running at 1-16MHz clock frequencies, with \( \approx 64 \) KBytes of addressable memory. SRAM is used as data memory with the size normally ranging between 4 and 16KBytes, while the rest of address space is available for program memory. Such devices execute instructions in place (in physical memory) and have no memory management unit (MMU) to support virtual memory.

Our implementation is based on MSP430. This choice is due to public availability of a well-maintained open-source MSP430 hardware design from Open Cores \[15\]. Nevertheless, our machine model and the entire methodology developed in this paper are applicable to other low-end MCUs in the same class, such as Atmel AVR ATmega. RA implementation is composed with VRASED, a publicly available verified hybrid RA architecture \[2\], which allows us to demonstrate security. Despite our specific implementation choices, we believe that RA’s concepts are also applicable to hardware-based RA architectures; see Section \[7\] for an overview of types of RA architectures.

II. DEFINITIONS & BACKGROUND

A. RA Definitions & Adversarial Model

As discussed in Section \[1\], RA is typically realized as a challenge-response protocol between \( \mathcal{P}_\text{rv} \) (challenger) and \( \mathcal{P}_\text{rv} \), a potentially infected remote low-end device. This notion is captured by a generic syntax for RA protocols in Definition \[1\].

Definition \[1\] specifies RA as a tuple \(( \text{Request}, \text{Attest}, \text{Verify})\). Request is computed by \( \mathcal{P}_\text{rv} \) to produce challenge Chal and send it to \( \mathcal{P}_\text{rv} \). Attest is performed by \( \mathcal{P}_\text{rv} \).
Definition 1 (syntax): \( RA \) is a tuple \((\text{Request}, \text{Attest}, \text{Verify})\) of algorithms:

- **Request** \( \text{Verify}^{\text{hvrf}} \to \text{hvrf} (\cdots) \): algorithm initiated by \( \text{hvrf} \) to request a measurement of \( \text{hvrf} \) memory range \( AR \) (attested range). As part of **Request**, \( \text{hvrf} \) sends a challenge \( \text{Chal} \) to \( \text{hvrf} \).
- **Attest** \( \text{Verify}^{\text{hvrf}} \text{(Chal,} \cdots) \): algorithm executed by \( \text{hvrf} \) upon receiving \( \text{Chal} \) from \( \text{hvrf} \). Computes an authenticated integrity ensuring function on \( AR \) content. It produces attestation token \( H \), which is returned to \( \text{hvrf} \), possibly accompanied by auxiliary information to be used by the **Verify** algorithm (see below).
- **Verify** \( \text{Verify}^{\text{hvrf}} (H, \text{Chal}, M, \cdots) \): algorithm executed by \( \text{hvrf} \) upon receiving \( H \) from \( \text{hvrf} \). It verifies whether \( \text{hvrf} \)’s current \( AR \) content corresponds to some expected value \( M \) (or one of a set of expected values). **Verify** outputs: 1 if \( H \) is valid, and 0 otherwise.

**Note:** In the parameter list, \((\cdots)\) denotes that additional parameters might be included, depending on the specific \( RA \) construction.

by using \( \text{Chal} \) to compute an authenticated integrity-ensuring function (e.g., MAC) over attested memory range (denoted by \( AR \)) and producing \( H \), which is sent back to \( \text{hvrf} \) for verification. For example, if **Attest** is implemented using a MAC, \( H \) is computed as:

\[
H = MAC_K(\text{Chal})||AR
\]

where \( || \) denotes concatenation and \( K \) is a symmetric key shared by \( \text{hvrf} \) and \( \text{hvrf} \). Upon receiving \( H \), \( \text{hvrf} \) executes algorithm **Verify** by checking if \( H \) corresponds to the \( MAC \) of some expected value \( M \).

**Adversarial Model.** We consider a strong \( RA \) adversary \( Adv \) that controls entire software state of \( \text{hvrf} \), including both code and data. \( Adv \) can modify any writable memory and read any memory (including secrets) that is not explicitly protected by trusted hardware. Also, \( Adv \) has full access to all Direct Memory Access (DMA) controllers on \( \text{hvrf} \) if present on \( \text{hvrf} \). Physical hardware attacks are out of scope of this paper: we assume that \( Adv \) can not alter any hardware components, modify code in \( \text{ROM} \), induce hardware faults, or retrieve \( \text{hvrf} \) secrets via physical side-channels. Protection against physical attacks is orthogonal and attainable via standard tamper-resistance techniques [16].

**B. Linear Temporal Logic (LTL)**

Computer-aided formal verification typically involves three basic steps: First, the system of interest (e.g., hardware, software, communication protocol) is described using a formal model, e.g., a Finite State Machine (FSM). Second, properties that the model should satisfy are formally specified. Third, the system model is checked against formally specified properties to guarantee that it retains them. This can be achieved via either Theorem Proving or Model Checking. In this work, we use the latter to verify the implementation of system modules.

In one instantiation of model checking, properties are specified as *formulae* using Linear Temporal Logic (LTL) and system models are represented as FSMs. Hence, a system is represented by a triple \((S, S_0, T)\), where \( S \) is a finite set of states, \( S_0 \subseteq S \) is the set of possible initial states, and \( T \subseteq S \times S \) is the transition relation set – it describes the set of states that can be reached in a single step from each state. The use of LTL to specify properties allows representation of expected system behavior over time.

In addition to propositional connectives, such as conjunction \((\land)\), disjunction \((\lor)\), negation \((\neg)\), and implication \((\rightarrow)\), LTL includes temporal connectives, thus enabling sequential reasoning. In this paper, we are interested in the following temporal connectives:

- \( X\phi \equiv \neg E\chi \phi \): holds if \( \phi \) is true at the next system state.
- \( F\phi \equiv \text{Future}\phi \): holds if there exists a future state where \( \phi \) is true.
- \( G\phi \equiv \text{Globally}\phi \): holds if for all future states \( \phi \) is true.
- \( \phi U \psi \equiv \text{Until}\psi \phi \): holds if there is a future state where \( \psi \) holds and \( \phi \) holds for all states prior to that.
- \( \phi W \psi \equiv \text{Weak until}\psi \phi \): holds if, assuming a future state where \( \psi \) holds, \( \phi \) holds for all states prior to that. If \( \psi \) never becomes true, \( \phi \) must hold forever. More formally: \( \phi W \psi \equiv (\phi U \psi) \lor G(\phi) \)

C. Formally Verified \( RA \)

**VRASED** [17] is a formally verified hybrid \( RA \) architecture, based on a hardware/software co-design. It is built as a set of sub-modules, each guaranteeing a specific set of sub-properties. Each sub-module (hardware or software) is individually verified. Finally, composition of all sub-modules is proved to satisfy formal definitions of \( RA \) soundness and security. Informally, \( RA \) soundness guarantees that an integrity-ensuring function (HMAC in **VRASED**’s case) is correctly computed over attested memory range \((AR)\). It also guarantees that \( AR \) can not be modified after the start of \( RA \) computation, thus enforcing temporal consistency and protecting against “hide-and-seek” attacks during \( RA \) computation [17]. \( RA \) security ensures that \( RA \) execution generates an unforgeable authenticated memory measurement and that \( K \) used in computing this measurement is not leaked before, during, or after, attestation.

To achieve its aforementioned goals, **VRASED**’s software part \((\text{SW}\text{–Att})\) resides in Read-Only Memory (ROM) and relies on a formally verified HMAC implementation from the HACL* cryptographic library [18]. A typical \( \text{SW}\text{–Att} \) execution proceeds as follows:

1. Read challenge \( \text{Chal} \) from a fixed memory region denoted by \( MR \).
2. Use a Key Derivation Function (KDF) to derive a one-time key from \( \text{Chal} \) and the attestation master key \( K \): \( KDF(K, MR) \) (where \( MR = \text{Chal} \)).
3. **Attest**’s implementation \((\text{SW}\text{–Att})\) generates attestation token \( H \) by computing an HMAC over an attested memory region \( AR \) using the newly derived key:
   \[
   H = HMAC(KDF(K, MR), AR)
   \]
4. Overwrite \( MR \) with the result \( H \) and return execution to unprivileged software, i.e, the normal application(s).

**VRASED**’s Hardware \((\text{HW}\text{–Mod})\) monitors 7 MCU signals:

- **PC**: Current Program Counter value;
• $R_{en}$: Signal that indicates if the MCU is reading from memory (1-bit);
• $W_{en}$: Signal that indicates if the MCU is writing to memory (1-bit);
• $D_{addr}$: Address for an MCU memory access;
• $DMA_{en}$: Signal that indicates if Direct Memory Access (DMA) is currently enabled (1-bit);
• $DMA_{addr}$: Memory address being accessed by DMA.
• irq: Signal that indicates if an interrupt is happening (1-bit);

These signals determine a one-bit reset signal output, that, when set to 1, triggers an immediate system-wide MCU reset, i.e., before execution of the next instruction. The reset output is triggered when VRASED’s hardware detects any violation of security properties. VRASED’s hardware is described in Register Transfer Level (RTL) using Finite State Machines (FSMs). Then, NuSMV Model Checker [19] is used to automatically prove that FSMs achieve claimed security sub-properties. Finally, the proof that the conjunction of hardware and software sub-properties implies end-to-end soundness and security is done using an LTL theorem prover. More formally,

Definition 2: VRASED’s Security Game (Adapted from [7])

- $l$ is the security parameter and $|K| = |Chal| = |MR| = l$
- $AR(t)$ denotes the content of $AR$ at time $t$

RA-game:

1) Setup: Adv is given oracle access to Attest (SW-Attest) calls.
2) Challenge: A challenge Chal is generated by calling Request (Definition 1) and given to Adv.
3) Response: Adv responds with a pair $(M, \sigma)$, where $\sigma$ is either forged by Adv, or is the result of calling Attest (Definition 1), at some arbitrary time $t$.
4) Game: Adv wins if $M \neq AR(t)$ and $\sigma = HMAC(KDF(K, Chal), M)$.

Note: If, as a part of Attest, $AR$ attestation is preceded by a procedure to authenticate $\forall rf \ t$ defined in step 3 is the time immediately after successful authentication, when $AR$ attestation in fact starts.

\textbf{VRASED} end-to-end security proof guarantees that no probabilistic polynomial time (PPT) adversary can win the RA security game in Definition 2 with non-negligible probability in the security parameter $l$, i.e., $Pr[Adv, \text{RA-game}] \leq negl(l)$.

\section*{D. MCU Assumptions}

Since we implement RATA on top of VRASED, we adopt the same machine model without additional assumptions. In particular, we assume that the MCU architecture correctly implements its specifications. Below, we review VRASED axioms relevant to RATA:

\textbf{A1 – Program Counter (PC):} PC always contains the address of the instruction being executed in a given CPU cycle.

\textbf{A2 – Memory Address:} Whenever memory is read or written, a data-address signal ($D_{addr}$) contains the address of the corresponding memory location. For a read access, a data-read-enable bit ($R_{en}$) must be set, while, for a write access, a data write-enable bit ($W_{en}$) must be set.

\textbf{A3 – DMA:} Whenever the DMA controller attempts to access the main system memory, a DMA-address signal ($DMA_{addr}$) reflects the address of the memory location being accessed and a DMA-enable bit ($DMA_{en}$) must be set. DMA can not access memory when $DMA_{en}$ is off (logical zero).

\textbf{A4 – MCU Reset:} At the end of a successful reset routine, all registers (including $PC$) are set to zero before resuming normal software execution flow. Resets are handled by the MCU in hardware. Thus, the reset handling routine can not be modified. When a reset happens, the corresponding reset signal is set. The same signal is also set when the MCU initializes for the first time.

\section*{III. RA TOCTOU}

This section defines the notion of TOCTOU-Security in the context of RA. We start by formalizing this notion using a security game. Next, we consider the practicality of this problem and overview existing mechanisms, arguing that they do not achieve TOCTOU-Security (neither according to TOCTOU-Security definition nor in practice) and incur high overhead.

\subsection*{A. Notation}

We first summarize our notation in Table I. We keep it mostly consistent with that in VRASED [7], with a few additional elements to denote RATA-specific memory regions and signals. To simplify the notation, when the value of a given signal (e.g., $D_{addr}$) is within a certain range (e.g., $AR = [AR_{min}, AR_{max}]$), we write that $D_{addr} \in AR$, i.e.,

$$D_{addr} \in AR \quad \iff \quad AR_{min} \leq D_{addr} \leq AR_{max} \quad (2)$$

In conformance with axioms discussed in Section II-C, we use $Mod\_Mem(x)$ to denote a modification to memory address address $x$. Given our machine model, the following logical equivalence holds:

$$Mod\_Mem(x) \equiv (W_{en} \land D_{addr} = x) \lor (DMA_{en} \land DMA_{addr} = x) \quad (3)$$

This captures the fact that a memory modification can be caused by either the CPU (reflected in signals $W_{en} = 1$ and $D_{addr} = x$) or by the DMA (signals $DMA_{en} = 1$ and $DMA_{addr} = x$). We also use this notation to represent a modification to an address within a contiguous memory region $R$ as:

$$Mod\_Mem(R) \equiv (W_{en} \land D_{addr} \in R) \lor (DMA_{en} \land DMA_{addr} \in R) \quad (4)$$

This notation simplifies exposition of system specifications and FSMs in Sections IV and V.

\subsection*{B. TOCTOU-Security Definition}

Definition 3 captures the notion of TOCTOU-Security. In it, the game formalizes the threat model discussed in Section II-C where Adv controls Prv’s entire software state, including the ability to invoke Attest at will. The game starts with the challenger ($\forall rf$) choosing a time $t_0$. At a later time ($t_{att}$), Adv receives Chal and wins the game if it can produce $H_{Adv}$ that is accepted by Verify as a valid response for expected $AR$ value $M$, when, in fact, there was a time between $t_0$ and $t_{att}$ when $AR \neq M$.

This definition augments RA security (Definition 2) to incorporate TOCTOU attacks, by additionally allowing Adv to win if it can produce the expected response and $AR$ was modified at any point after $t_0$, where $t_0$ is chosen by $\forall rf$. 
For example, if \( \mathcal{A} \) wants to know if \( \mathcal{A} \) remained in a valid state for the past two hours, \( \mathcal{V} \mathcal{R} \mathcal{F} \) chooses \( t_0 \) as \( t_0 = t_{\text{att}} - 2h \). Note that this definition also captures security against transient attacks in which \( \mathcal{A} \mathcal{D} \mathcal{V} \) changes modified memory back to its expected state and leaves the device, thus attempting to hide its ephemeral modification from the upcoming attestation request. This attack is undetectable by all \( \mathcal{R} \) \( \mathcal{A} \) schemes that are not \( \text{TOCTOU-Secure} \).

**C. TOCTOU-Secure \( \mathcal{R} \) \( \mathcal{A} \) vs. Consecutive Self-Measurements**

\( \mathcal{R} \) \( \mathcal{A} \) schemes based on consecutive self-measurements [9], [20] attempt to detect transient malware that comes and goes between two successive \( \mathcal{R} \) \( \mathcal{A} \) measurements. The strategy is for \( \mathcal{P} \mathcal{R} \mathcal{V} \) to intermittently (based on some either periodic or unpredictable schedule) and unilaterally invoke its \( \mathcal{R} \) \( \mathcal{A} \) functionality. Then, either \( \mathcal{P} \mathcal{R} \mathcal{V} \) self-reports to \( \mathcal{V} \mathcal{R} \mathcal{F} \) [20], or \( \mathcal{P} \mathcal{R} \mathcal{V} \) accumulates measurements locally and waits for \( \mathcal{V} \mathcal{R} \mathcal{F} \) to explicitly request them [9]. Upon receiving \( \mathcal{R} \) \( \mathcal{A} \) response(s), \( \mathcal{V} \mathcal{R} \mathcal{F} \) checks for malware presence at the time of each \( \mathcal{R} \) \( \mathcal{A} \) measurement. Time intervals used in these \( \mathcal{R} \) \( \mathcal{A} \) schemes are depicted in Figure 2.

**TABLE I. Notation**

| Symbol | Description |
|--------|-------------|
| PC     | Current Program Counter value |
| \( R_{\text{env}} \) | Signal that indicates if the MCU is reading from memory (1-bit) |
| \( W_{\text{env}} \) | Signal that indicates if the MCU is writing to memory (1-bit) |
| \( D_{\text{addr}} \) | Address for an MCU memory access |
| \( D_{\text{MA}_{\text{env}}} \) | Signal that indicates if DMA is currently enabled (1-bit) |
| \( t_{\text{RQ}} \) | Signal that indicates if an interrupt is happening |
| \( CR \) | Memory region where \( \text{SW-Att} \)'s (Latest Modification Time) Memory region that stores a times-
|     | - (Attested Region) Memory region to be attested. Can be
|     | - (Attested Modification Time) Memory region that stores a times-
|     | - (Attested Program Counter value) Current Program Counter value
| \( MR \) | The first instruction in \( \text{SW-Att} \)'s computation scheme is to invoke \( \text{Attest Compute.} \)
| \( \text{set}_{\text{LMT}} \) | The first instruction in \( \text{VRASED's SW-Att} \) that is executed after successful authentication of \( \mathcal{V} \mathcal{R} \mathcal{F} \)'s request.
| \( \text{UP}_{\text{LMT}} \) | (\( \text{RATA}_{\text{A}} \)) A 1-bit signal overwrites LMT with the content of \( MR \) when set to logical 1.
| \( \text{reset} \) | A 1-bit signal that reboots/resets the MCU when set to 1.

**Definition 3:**

1. **\( \mathcal{R} \) \( \mathcal{A} \)-TOCTOU Security Game:** Challenger plays the following game with \( \mathcal{A} \mathcal{D} \mathcal{V} \):
   1. Challenger chooses time \( t_0 \).
   2. \( \mathcal{A} \mathcal{D} \mathcal{V} \) is given full control over \( \mathcal{P} \mathcal{R} \mathcal{V} \) software state and oracle access to Attest calls.
   3. At time \( t_{\text{att}} > t_0 \), \( \mathcal{A} \mathcal{D} \mathcal{V} \) is presented with \( \text{Chal} \).
   4. \( \mathcal{A} \mathcal{D} \mathcal{V} \) wins if and only if it can produce \( \text{H}_{\mathcal{A} \mathcal{D} \mathcal{V}} \), such that:
      
      \[
      \text{Verify} \left( \text{H}_{\mathcal{A} \mathcal{D} \mathcal{V}}, \text{Chal}, M, \cdots \right) = 1 \tag{5}
      \]
      
      and
      
      \[
      \exists t_0 \leq t_i \leq t_{\text{att}} \{ AR(t_i) \neq M \} \tag{6}
      \]

   where \( AR(t_i) \) denotes the content of \( AR \) at time \( t_i \).

2. **\( \mathcal{R} \) \( \mathcal{A} \)-TOCTOU Security Definition:** An \( \mathcal{R} \) \( \mathcal{A} \) scheme is considered TOCTOU-Secure if – for all PPT adversaries \( \mathcal{A} \mathcal{D} \mathcal{V} \) – there exists a negligible function \( \text{negl} \), such that:

   \[
   \text{Pr}[\text{Adv, } \text{RA-TOCTOU-game}] \leq \text{negl}(1)
   \]

   where \( l \) is the security parameter.

For example, if \( \mathcal{V} \mathcal{R} \mathcal{F} \) wants to know if \( \mathcal{A} \) remained in a valid state for the past two hours, \( \mathcal{V} \mathcal{R} \mathcal{F} \) chooses \( t_0 \) as \( t_0 = t_{\text{att}} - 2h \). Note that this definition also captures security against transient attacks in which \( \mathcal{A} \mathcal{D} \mathcal{V} \) changes modified memory back to its expected state and leaves the device, thus attempting to hide its ephemeral modification from the upcoming attestation request. This attack is undetectable by all \( \mathcal{R} \) \( \mathcal{A} \) schemes that are not \( \text{TOCTOU-Secure} \).

**Fig. 2. Consecutive Self-Measurements**

Note that consecutive measurements always leave time gaps when transient malware presence would not be detected. The only way to detect all transient malware with self-measurement schemes is to invoke \( \mathcal{R} \) \( \mathcal{A} \) functionality on \( \mathcal{P} \mathcal{R} \mathcal{V} \) with a sufficiently high frequency such that the fastest possible transient malware can not come and go undetected. However, even if it were easy (which it is not) to determine such “sufficiently high frequency”, as we show below, doing this is horrendously costly. We define CPU utilization (\( U \)) in a consecutive scheme as the percentage of CPU cycles that can be used by a regular application (\( C_{\text{app}} \)), i.e., cycles other than those spent on self-measurements (\( C_{\text{RA}} \)):

\[
U = \frac{C_{\text{app}}}{C_{\text{app}} + C_{\text{RA}}} \tag{7}
\]

As discussed above, guaranteed detection of transient malware via consecutive self-measurements requires that:

\[
C_{\text{Adv}} < C_{\text{Adv}} \tag{8}
\]

where \( C_{\text{Adv}} \) is the hypothetical number of instruction cycles used by the fastest transient malware, capable of infecting \( \mathcal{P} \mathcal{R} \mathcal{V} \), performing its tasks, and erasing itself. To illustrate this point, we assume a conservative number for \( C_{\text{Adv}} \) to be \( 10^6 \) cycles. In this case:

\[
C_{\text{Adv}} = 10^6 \implies C_{\text{Adv}} < 10^6 \implies U < \frac{10^6}{10^6 + C_{\text{RA}}} \tag{9}
\]

For example with \( C_{\text{RA}} \), consider the number of CPU cycles required by \( \text{VRASED} \) (other hybrid \( \mathcal{R} \mathcal{A} \) architectures, e.g., [4], have similar costs) to attest a program memory of 4KB: \( C_{\text{RA}} = 3.6 \times 10^6 \) CPU cycles (about half a second in a typical 8MHz low-end MCU):

\[
U < \frac{10^6}{10^6 + 3.6 \times 10^6} \implies U < 21.74\% \tag{10}
\]

To detect transient malware, a large fraction of CPU cycles (almost 80% in this toy example) is spent on \( \mathcal{R} \) \( \mathcal{A} \) computation. In practice, it is hard to determine \( C_{\text{Adv}} \) and in some cases (e.g., changing a general-purpose input/output value to trigger actuation) it is likely to be much less than \( 10^6 \) cycles, resulting in even lower CPU utilization left for legitimate applications.
running on \( Prv \). Therefore, detection of all transient malware using consecutive self-measurements is impractical. This also applies to the case where the interval between successive measurements is variable and/or randomly selected from a range \([0, t_{max}]\). As discussed in [20], this is because, to achieve negligible probability of malware evasion \( t_{max} < C_{Adv} \).

Fig. 3. TOCTOU-Secure RA

As shown in Figure 3, TOCTOU-Secure RA (per Definition 3) allows \( Vrf \) to ascertain memory integrity independently from the time between successive RA measurements, regardless of transient malware’s speed. In the next sections, we propose two TOCTOU-Secure techniques and show their security with respect to Definition 3.

IV. RATA\(_A\): RTC-BASED TOCTOU-SECURE TECHNIQUE

In hybrid RA, trusted software (\( SW-Att \)) is usually responsible for generating the authenticated RA response \( (H) \) and all semantic information therein. Meanwhile, trusted hardware (\( HW-Mod \)) is responsible for ensuring that \( SW-Att \) executes as expected, preventing leakage of its cryptographic secrets, and handling unexpected or malicious behavior during execution. To address TOCTOU, we propose a paradigm shift by allowing (formally verified) \( HW-Mod \) to also provide some context about \( Prv \)’s memory state.

We now overview RATA\(_A\) – a simple technique that requires \( Prv \) to have a reliable read-only Real-Time Clock (RTC) synchronized with \( Vrf \). Admittedly, RTCs are not readily available on low-end MCUs and secure clock synchronization in distributed systems is challenging [21], [22], [23], especially for low-end embedded systems [24], [25]. Nonetheless, we start with this simple approach to show the main idea behind TOCTOU-Secure RA. Next, Section IV proposes an alternative that removes the RTC requirement, as long as \( Vrf \) requests are authenticated by \( Prv \). Note that \( Vrf \) authentication [26] is already included in some current hybrid RA architectures, including VRASED.

A. RATA\(_A\): Design

RATA\(_A\) is illustrated in Figure 4, it is designed as a verified hardware module behaving as follows:

1) It monitors a set of CPU signals and detects whenever any location within \( AR \) is written. This is achieved by checking the value of signals \( D_{addr}, W_{en}, DMA_{addr}, \) and \( DMA_{en} \) (see Section II-C). These signals allow for detection of memory modifications either by CPU or by DMA.

2) Whenever a modification to \( AR \) is detected, RATA\(_A\) logs the timestamp by reading the current time from the RTC and storing it in a fixed memory location, called Latest Modification Time (LMT).

3) In the memory layout, \( LMT \in AR \). Also, RATA\(_A\) enforces that LMT is always read-only for all software executing on the MCU, and for DMA.

Note that, by enforcing \( LMT \in AR \), the attestation result \( H = HMAC(KDF(\{K, MR\}, AR)) \) includes the authenticated value of LMT – the time corresponding to the latest modification of \( AR \). As part of the Verify algorithm, \( Vrf \) compares this information with the time of the last authorized modification \( t_0 \) of \( AR \) to check whether any unauthorized modification occurred since then. The general idea is further specified in Construction 1 which shows how RATA\(_A\) can be seamlessly integrated into VRASED, enforcing two additional properties in hardware to obtain TOCTOU-Security. These properties are formalized in LTL in Equations 11 and 12 of Construction 1.

B. RATA\(_A\): Security

We show that Construction 1 is secure as long as RATA\(_A\) implementation adheres to LTL statements in Equations 11 and 12. This verification is discussed in Section IV-C. The cryptographic proof is by reduction from VRASED security (per definition 2) to TOCTOU-Security (per Definition 5) of Construction 1. For its part, VRASED is shown secure according to Definition 2 as long as HMAC is a secure (existentially unforgeable [27]) MAC. See [27] for details.

**Theorem 1:** Construction 1 is TOCTOU-Secure according to Definition 5 as long as VRASED is secure according to Definition 2.

**Proof:** By contradiction, assume a polynomial \( Adv \) that wins the game in Definition 3 with probability \( Prv[Adv, RA-TOCTOU-game] > \text{neg}(!) \). Therefore, \( Adv \) can produce \( t_{LMT} | H_{Adv} \) such that:

\[
\text{Verify}^{Vrf}(H_{Adv}, \text{Chal}, M, t_0, t_{LMT}) = 1
\]

and

\[
\exists t_0 \leq t_{LMT}, \{AR(t_i) \neq M\}
\]
Construction 1 (RATA\textsubscript{AR}): Suppose LMT is the program memory region within AR (LMT \in AR):

- \textbf{Request}\textsubscript{Prv} \rightarrow \textsubscript{Prv}(): \textsubscript{Prv} generates a random \(l\)-bits challenge \(Chal \leftarrow $\{0,1\}^l\) and sends it to \Prv.
- \textbf{Attest}\textsubscript{Prv} \rightarrow \textsubscript{Prv}(Chal): Call VRASED \textsc{Sw-Att}'s RA function to compute \(H = \text{HMAC}(KDF(K, Chal), AR)\). The resulting \(H\) is sent to \textsubscript{Prv} along with the value stored in LMT, denoted \(t_{LMT}\). At all times, RATA\textsubscript{AR} hardware to enforces the following invariants:
  - LMT is read-only to software:

\[
\text{Formal statement (LTL)}:\quad G\{\text{Mod}_\text{Mem}(LMT) \rightarrow \text{reset}\}
\]

- LMT is overwritten with the current time from RTC if, and only if, \(AR\) is modified:

\[
\text{Formal statement (LTL)}:\quad G\{\text{Mod}_\text{Mem}(AR) \rightarrow \text{set}_\text{LMT}\}
\]

where \text{reset} is a 1-bit signal that triggers an immediate reset of the MCU, and \text{set}_\text{LMT} is a 1-bit output signal of RATA\textsubscript{AR} controlling the value of LMT reserved memory. Whenever \text{set}_\text{LMT} = 1, LMT is updated with the current value from the real-time clock (RTC). LMT maintains its previous value otherwise.

- \textbf{Verify}\textsubscript{Prv}(H, Chal, M, t_0, t_{LMT}): \(t_0\) is an arbitrary time chosen by \textsubscript{Prv}, as in Definition 3. Upon receiving \(t_{LMT}| H\) \textsubscript{Prv} checks:

\[
t_{LMT} < t_0
\]
\[
H = \text{HMAC}(KDF(K, MR), M)
\]

where \(M\) value of \(AR\), as expected by \textsubscript{Prv}. In expected \(M\), the value corresponding to \text{LMT} is set to \(t_{LMT}\), as received from \textsubscript{Prv}. Verify returns 1 if and only if both checks succeed.

By definition, Verify in Construction 1 results in 1 only if \(t_{LMT} < t_0\). If \text{Adv} simply replies with the actual value \(t_{LMT} = LMT \geq t_i\), Verify result would be 0, since \(t_i \geq t_0\), failing to satisfy Verify condition: \(t_{LMT} < t_0\). Thus, to obtain Verify = 1, \text{Adv} must spoof the value of \(t_{LMT}\) to \(t_{LMT} < t_0\).

Upon receiving the spoofed value of \(t_{LMT}\), the Verify now expects:

\[
H_{\text{Adv}} = \text{HMAC}(KDF(K, MR), M)
\]

where expected \(M\) reflects \(LMT = t_{LMT}\), i.e., \(LMT < t_0\).

In addition, note that hardware enforced properties \(1\) and \(12\) guarantee that \(LMT \in AR\) always contains the time of the most recent modification of \(AR\). Thus, because \(t_{LMT} \geq t_i\), it must be the case that \(AR(t_{att})\) will reflect \(LMT \geq t_i\) implying \(LMT \neq t_{LMT}\) and consequently \(AR(t_{att}) \neq M\).

Under such restriction, \text{Adv} ability to win the game implies the capability to produce \(H_{\text{Adv}}\) such that \(\text{Verify}^{\text{Prv}}(H, Chal, M, t_0, t_{LMT}) = 1\), even though modifying \(AR\) such that \(AR(t_{att})\) is not possible. To conclude the proof, we show that the existence of such an \text{Adv} implies the existence of another adversary \text{Adv}_{\text{RA}} that wins the RA security game in Definition 2 against VRASED, contradicting the theorem’s assumption.

To win the game in Definition 2, \text{Adv}_{\text{RA}} behaves as follows:

1) At time \(t_i\), where \(t_0 \leq t_i \leq t_{att}\), \text{Adv}_{\text{RA}} modifies \(AR\) causing \(LMT \in AR\) to store the value of \(t_i\).

2) \text{Adv}_{\text{RA}} receives \(Chal\) from the challenger in step 2 of RA security game of Definition 2 and executes the same algorithm of \text{Adv} with inputs \(Chal\) and \(t_{att} = t\) to produce \(H_{\text{Adv}}\), such that \(\text{Verify}^{\text{Prv}}(H_{\text{Adv}}, Chal, M, t_0, t_{LMT}) = 1\) with probability:

\[
Pr[\text{Adv}, RA-TOCTOU-game] > \text{neg}(1),
\]

even though \(t_{LMT} < t_0 < t_i\).

3) As a response in step 3 of the game in Definition 2, \text{Adv}_{\text{RA}} replies with: \(\sigma = H_{\text{Adv}}\).

Since \(\text{Verify}^{\text{Prv}}(H_{\text{Adv}}, Chal, M, t_0, t_{LMT}) = 1\), it follows that \(\sigma = H_{\text{Adv}} = \text{HMAC}(KDF(K, MR), M)\), for expected \(M\) containing \(LMT = t_{LMT}\). However, due to the AR modification at time \(t_i\), \(AR(t)\) must reflect \(LMT \geq t_i\), satisfying the condition that \(AR(t) \neq M\) and allowing \text{Adv}_{\text{RA}} to win the game in Definition 2 with probability:

\[
Pr[\text{Adv}, RA-game] = Pr[\text{Adv}, RA-TOCTOU-game] > \text{neg}(1)
\]

C. RATA\textsubscript{AR}: Implementation & Verification

Construction 1 (and respective security proof) assumes that properties in Equations 1 and 12 are enforced by RATA\textsubscript{AR}.
Figure 5 shows a formally verified FSM corresponding to this implementation. It enforces two properties of Equations 11 and 12. This FSM is implemented as a Mealy machine, where output changes anytime based on both the current state and current input values. The FSM takes as an input a subset of signals, shown in Figure 4, and produces two 1-bit outputs: reset to trigger an immediate reset and setLMT to control the value of LMT memory (see Construction 1). reset is 1 whenever FSM transitions to RESET state and while it remains in that state; it remains 0 otherwise. Whereas, setLMT is 1 when FSM transitions to Mod state, and becomes 0 whenever it transitions out of Mod state. setLMT = 0 in all other cases.

The FSM works by monitoring write access to LMT and transitioning to RESET whenever such attempt happens. When the system is running (i.e., reset = 0), FSM also monitors write access to AR and transitions to Mod state whenever it happens. The FSM transitions back to NotMod state if AR is not being modified. We design the FSM in Verilog HDL and automatically translate into SMV using Verilog2SMV [28]. Finally, we use NuSMV model checker [19] to automatically prove that the FSM complies with invariants 1 and 2. The implementation and correspondent verification are available in [14].

Remark: The ability to cause a reset by attempting to write to LMT does not give Adv any advantage, as any bare-metal software (including malware) can always trigger resets on unmodified low-end devices, for instance, by inducing software faults.

V. RATA\textsubscript{B}: Clockless TOCTOU-Secure RA Technique

We now describe RATA\textsubscript{B} – a TOCTOU-Secure approach that requires no clock on \(Prv\). We aim to apply the ideas from RATA\textsubscript{A} by using hardware to convey authenticated information about the time of the latest memory modification as part of the attestation result. However, lack of RTC prevents any notion of “time” on \(Prv\)’s end. To cope with this, we rely on \(Vrf\) to convey information tied to a given point in time, according to \(Vrf\)’s own local clock. This is done as a part of RA Request algorithm. In fact, RATA\textsubscript{B} uses the attestation challenge (Chal) itself in this task, taking advantage of the fact that Chal is unique per Request and is available in any RA technique, thus incurring no additional communication overhead. Security of RATA\textsubscript{B} is tightly coupled with authentication of \(Vrf\) Request, which is already part of VRASED architecture [7] (see Appendix A for details).

A. RATA\textsubscript{B} – Design

The design of RATA\textsubscript{B} remains consistent with Figure 4. RATA\textsubscript{B} monitors the same set of MCU signals as RATA\textsubscript{A} and also works by overwriting the special memory region \(LMT \in AR\). However, instead of logging an RTC timestamp to LMT, it logs Chal, which was sent by \(Vrf\) as a part of its Request and given as input to Attest(Chal, ...). LMT is overwritten with the currently received Chal if and only if, a modification of AR occurred since the previous Attest instance. In summary, RATA\textsubscript{B} security relies on the following properties, enforced by its verified hardware implementation (see Section V.C):  

- Similar to RATA\textsubscript{A}, no software running on \(Prv\) can overwrite LMT, i.e., LMT is only modifiable by RATA\textsubscript{B} hardware.  
- An update to LMT is triggered only immediately after a successful authentication during Attest computation.  
- The first successful authentication happening after a modification of AR always causes LMT to be updated with the current value of Chal which is stored in MR. (Recall from Table I that MR is the memory location from which Attest reads the value of Chal.)

Let Chal\textsubscript{1} and H\textsubscript{1} denote the attestation challenge and response successfully sent/received by \(Vrf\), respectively. \(Vrf\) interprets RA results as follows: if H\textsubscript{1} is a valid response, i.e., it corresponds to the expected AR value, time \(t_1\) when such response is received is saved locally by \(Vrf\), associated to Chal\textsubscript{1}. In subsequent attestation results (H\textsubscript{2}, H\textsubscript{3}, ...), \(Vrf\) checks the value of LMT for correspondence with Chal\textsubscript{1}. If LMT \(\neq\) Chal\textsubscript{1}, \(Vrf\) learns that AR was modified after \(t_1\). This stems from RATA\textsubscript{B} verified module, which guarantees that LMT is always overwritten with the newly received challenge if a TOCTOU happens between consecutive calls to Attest.

We highlight the following observations:

- **Authentication of \(Vrf\) Request** is instrumental to RATA\textsubscript{B} security. Without it, Adv can simply choose Chal\textsubscript{Adv} and call Attest Chal\textsubscript{Adv} after an unauthorized modification of AR, thus setting LMT = Chal\textsubscript{Adv} of its choice. By choosing Chal\textsubscript{Adv} as a value previously used by \(Vrf\), Adv can easily convince \(Vrf\) that no TOCTOU occurred between measurements. In other words, lack of Request authentication allows Adv to modify LMT at will, rendering write protection of LMT useless.

- **Uniqueness of LMT** must be enforced, e.g., by having \(Vrf\) randomly sample Chal from a sufficiently large space or use Chal as a monotonically increasing counter, depending on specifics of Request algorithm. If Chal is reused after \(n\) instances of Request, \(Adv\) can wait for the \(n\)-th authentic Request to complete, inject \(Prv\), perform its tasks, and leave \(Prv\) before the \((n + 1)\)-st Request occurs (with a reused Chal), resulting in a valid response and compromised TOCTOU-Security. For example, if we use LMT as a dirty-bit (instead of Chal), security can be subverted in two Request-s, even if they are properly authenticated.

RATA\textsubscript{B} is specified in Construction 2. Its hardware module controls the value of a 1-bit signal \(UP_{LMT}\). When set to 1, \(UP_{LMT}\) updates LMT with the current value of MR; otherwise, LMT maintains its current value. RATA\textsubscript{B} hardware detects successful authentication of \(Vrf\) by checking whether the program counter PC points to the instruction reached immediately after successful authentication. Note that the instruction at location CREAUTH is never reached unless authentication succeeds.

#### Theorem 2: Construction 2 is TOCTOU-Secure according to Definition 3 as long as VRASED is secure according to Definition 2

---

8
Mem

Mem

Fig. 6. RATA\textsubscript{B} FSM for clock-less TOCTOU-secure RA

Construction 2 (RATA\textsubscript{B}): Suppose LMT is a memory region within AR (i.e., LMT ∈ AR) and T is a table, initially empty, stored by Vrf. RATA\textsubscript{B} is specified as follows:

- Request\textsuperscript{Vrf→Pr}(): Vrf generates a pair [Chal, Auth] according to VRASED authentication algorithm (see Appendix A for details).

- Attest\textsuperscript{Pr→Vrf}(Chal, Auth): Call VRASED SW-Attest’s RA function to use Auth to authenticate Chal, and after successful authentication, compute $H = HMAC(KDF(K, Chal), AR)$, restricted that LMT ∈ AR, where $|LMT| = |Chal|$. The result $H$ is sent to Vrf along with the contents of LMT. To support this operation, at all times, RATA\textsubscript{B} hardware on Prv enforces the following:

  - LMT is read-only to software:

    \begin{align*}
    \text{Formal statement (LTL):} \quad & G\{\text{Mod}_\text{Mem}(LMT) \rightarrow \text{reset}\} \quad (17) \\
    \text{– LMT is never updated without authentication:} \\
    \text{Formal statement (LTL):} \quad & G\{[\neg UP_{\text{LMT}} \land X(UP_{\text{LMT}})] \rightarrow X(PC = CR_{\text{auth}})\} \quad (18) \\
    \text{– Modification(s) to AR imply updating LMT in the next authenticated Attest call:} \\
    \text{Formal statement (LTL):} \quad & G\{\text{Mod}_\text{Mem}(AR) \lor \text{reset} \rightarrow [(PC = CR_{\text{auth}} \rightarrow UP_{\text{LMT}}) \ W (PC = CR_{\text{max}} \lor \text{reset})]\} \quad (19)
    \end{align*}

  \textbf{where \text{reset} is a 1-bit signal that triggers an immediate reset of the MCU, and $UP_{\text{LMT}}$ is a 1-bit signal that, when set to 1, replaces the content of LMT with the current value stored in MR region (i.e., Chal). LMT maintains its previous value otherwise.}

- Verify\textsuperscript{Vrf}(H, Chal, M, t\textsubscript{0}, T, LMT): Upon receiving $LMT [H], Vrf$ will behave as follows:

  1) If $LMT = \text{Chal}$ and $H \equiv HMAC(KDF(K, \text{Chal}), M)$ (where $M$ is the expected AR value) add current time to $T$ associated to Chal and return 0;

    Otherwise, proceed to step 2;

  2) Use the received $LMT$ value to search in table $T$.

    If $LMT$ is not present in $T$, return 0;

    If $LMT$ is present, set $t$ to the time associated to $LMT$ and proceed to step 3;

  3) Check whether $t \leq t_0$, if not, return 0;

    Otherwise, proceed to step 4;

  4) Check if $H \equiv HMAC(KDF(K, \text{Chal}), M)$, where $M$ is the expected AR value (recall that AR includes LMT, therefore, this check also authenticates the received value for LMT).

    If this check fails, return 0;

    Otherwise, proceed to step 5;

  5) Add current time to $T$ associated to Chal and return 1.

C. RATA\textsubscript{B}: Implementation & Verification

Proof of Theorem 2 assumes that RATA\textsubscript{B} hardware adheres to properties in Equations 17 to 19. Figure 6 shows RATA\textsubscript{B} implementation as an FSM formally verified to adhere to these properties. It takes as input a subset of signals, shown in Figure 4 and outputs two 1-bit signals: reset triggers an immediate system-wide reset and $UP_{\text{LMT}}$ controls updates to LMT region. $UP_{\text{LMT}} = 1$ whenever the FSM transitions to state UPDATE and is has value 0 in all other states. reset = 1 whenever the FSM transitions to state RESET and while it remains in this state; it remains 0 otherwise. The FSM operates as follows:

1) If a software modification of LMT is attempted, FSM triggers reset immediately, regardless of what state it is in.

2) If no modifications are made to AR since the previous computation of Attest, FSM remains in NotMod state.

3) At any point in time, if a modification to AR is detected, FSM transitions to state Mod. This transition indicates that a modification occurred, although it neither alters any output nor modifies LMT. This is because the information to be written to LMT (the value of Chal in the next Request) is not available at this time.

4) When a call to Attest is made, two possible actions can happen:

   a) If FSM is in NotMod state, Attest is computed

   b) If FSM is in Mod state, Attest is computed

   c) If FSM is in UPDATE state, Attest is computed

Proof of Theorem 2 follows along the same lines as that of Theorem 1. We show that, if properties in Equations 17, 18 and 19 hold, existence of $\text{Adv}$ that wins the TOCTOU security game against RATA\textsubscript{B} implies the existence of another $\text{Adv}$ that wins RA security game against VRASED, thus contradicting the initial premise. The complete proof is deferred to Appendix B.
normally and FSM remains in the same state.

b) Otherwise, FSM stays in Mod state until condition \( PC = CR_{\text{auth}} \) is met, implying successful authentication of \( \forall \text{f} \) Request. Then, FSM transitions to state UPDATE causing \( UP_{LMT} \) to be set during the transition. Hence, \( LMT \) is overwritten with Chal passed as a parameter to the current Attest call. Note that update to \( LMT \) happens before the computation of the integrity ensuring function (HMAC) over \( AR \), which happens in state ATTEST. Therefore, attestation result \( H \) will reflect \( LMT = \text{Chal} \) as part of \( AR \). Once Attest is completed (\( PC = CR_{\text{max}} \)), FSM transitions back to NotMod.

The same verification tool-chain discussed in Section IV-C is used to prove that this FSM adheres to LTL statements in Equations 17, 18, and 19.

VI. EVALUATION

Our prototype is built upon a representative of the low-end class of devices – TI MSP430 MCU family. The prototype extends VRASED (itself built atop OpenMSP430 – an open-source implementation of MSP430) to enable TOCTOU detection. It is synthesized and executed using Basys3 commodity FPGA prototyping board.

Hardware Overhead. Table II reflects the analysis of \( RATA \) verified hardware overhead. Similar to the related work [7], [10], [31], [32], [3], [1], we consider the hardware overhead in terms of additional LUTs and registers. The increase in the number of LUTs can be used as an estimate of the additional chip cost and size required for combinatorial logic, while the number of registers offers an estimate on the state registers required by the sequential logic in \( RATA \) FSMs. Compared to VRASED, the verified implementation of \( RATA_A \) module takes 4 additional registers and 13 additional LUTs, while \( RATA_B \) increases the number of LUTs and registers by 57 and 27, respectively. With respect to unmodified OpenMSP430 architecture, this represents the overhead of 1.4% LUTs and 1.4% registers for \( RATA_A \) and 3.8% LUTs and 4.8% registers for \( RATA_B \).

Runtime Overhead. Notably, \( RATA \) does not require any modification to RA execution. It only ensures that information about the latest modification of attested memory is factored into the attestation result. Hence, it incurs no extra runtime cycles or additional RAM allocation, on top of that of VRASED architecture. In fact, as we discuss next, in Section VII Attest runtime can be reduced to the time to attest only LMT. The runtime reduction is presented in Figure 8. This represents a reduction of \( \approx 10 \) times compared, e.g., to the number of cycles to attest an AR of size 4KBytes. The runtime savings increase linearly with the size of AR.

Memory Overhead. \( RATA_A \) requires 128-bit of additional storage – 64-bit for RTC and another 64-bit for LMT. RTC is implemented using a 64-bit memory cell incremented at every clock cycle. This guarantees that RTC does not wrap around during \( Prv \)'s lifetime since it would take more than 70,000 years for that to happen on MSP430 running at 8MHz and incrementing RTC at every cycle. In \( RATA_A \), LMT is implemented as a 64-bit memory storage and updates its content with RTC value whenever \( set_{LMT} \) bit is on. For \( RATA_B \), the memory overhead increases to a total of 512 bits. A 256-bit memory storage is required by the implementation of VRASED authentication module, while another 256-bit storage is used to implement LMT that updates its content with Chal when applicable (as described in Section V). This small reserved memory corresponds to 0.1% of MSP430 memory address space (64KBytes in total).

Verification resources. We verify \( RATA \) on an Ubuntu 18.04 machine running at 3.40GHz. Results are shown in Table II. \( RATA_A \) adds 127 lines of verified Verilog code on top of VRASED. These are needed to enforce 2 invariants in Equations 11 and 12. \( RATA_B \) incurs 182 additional lines of verified Verilog code, needed to enforce the 3 invariants in Equations 17, 18, and 19. Besides that, \( RATA \) verification requires checking existing VRASED invariants. Overall verification process takes less than one second and consumes at most 26MB of memory, making it workable on a commodity desktop.

Comparison. We compare \( RATA \)'s hardware overhead with that of two recent self-measurement RA techniques: SeED [20] and ERASMUS [9]. Even though, as discussed in Section III-C, these techniques do not achieve TOCTOU-Security (per Definition 3), we believe them to be the most closely related approaches to \( RATA \). SeED extends a 32-bit Intel architecture, which is higher-end than our target devices, i.e., a 16-bit TI MSP430. Whereas, ERASMUS was implemented on MSP430. Figure 7 compares \( RATA \) to SeED and ERASMUS in terms of numbers of additional LUTs and registers. \( RATA_A \) require fewer LUTs, compared to both SeED and ERASMUS. Whereas, \( RATA_B \) necessitates more registers, compared to ERASMUS, it uses less LUTs than both self-measurements techniques. In summary, both \( RATA \)-s incur low overhead: < 5% increase for both LUTs and registers.

VII. USING RATA TO ENHANCE RA & RELATED SECURITY SERVICES

A. Constant-Time RA

One notable and beneficial feature of \( RATA \) is that, most of the time, \( RA \) no longer needs to be computed over the entire \( AR \), which significantly reduces \( RA \) execution time on \( Prv \).
If $r_f$ already knows $AR$ contents from a previous attestation result, it suffices to show that $AR$ was not changed since then. This can be done by attesting $LMT$ by itself, instead of $AR$ in its entirety, resulting in substantial reduction of computation time from linear in the size of $AR$ to constant: $|LMT|$, i.e., 32 bytes. $RA$ can be performed differently, in two possible cases:

- **Case-1**: if no modification to $AR$ happened since the last attestation (denoted by $t_{att}$), call Attest on $LMT$ region only. Verify checks for $H = HMAC(KDF(K,Chal),LMT)$. $r_f$ then learns whether $AR$ was modified since the previous measurement, solely based on $LMT$. By checking that $LMT$ corresponds to $t_0 < t_{att}$, this result confirms that $AR$ remained the same in the interim. Therefore, measuring $AR$ again is unnecessary – doing so would be redundant.

- **Case-2**: if $AR$ was modified since the last attestation, call Attest covering entire $AR$. Verify is computed normally as described in Constructions 1 or 2, depending on the implementation, i.e., $RATA_A$ or $RATA_B$.

**Remark**: Note that $Prv$'s $RA$ functionality can easily detect whether $AR$ was modified (in order to decide between attesting with Case-1 or Case-2) by checking the value of $LMT$, which is readable in software, though not writable.

Most of the time, $Prv$ is expected to be in a benign state (i.e., no malware), especially if $Adv$ knows that its presence is guaranteed to be detectable. In such times, size of attested memory can be reduced reduced from several KBytes (e.g., when $AR$ is the entire program memory on a low-end $Prv$) to a mere 32 Bytes ($LMT$ size), Figure 8 depicts an empirical result on the MSP430 MCU showing how this optimization can significantly reduce $RA$ runtime overhead.

In the rest of this section, we discuss some implications of this optimization, along with security improvements offered by $RATA$, for different branches of $RA$ and related security services.

### B. Atomicity & Real-Time Settings

Security of hybrid $RA$ architectures generally depends on temporal consistency of attested memory. Simply put, temporal consistency means “no modifications of attested memory $AR$ during $RA$ computation”. Lack thereof allows self-relocating malware to move itself within $Prv$'s memory during attestation, in order to avoid detection, e.g., if malware interrupts attestation execution, relocates itself to the part of $AR$ that has already been covered by the integrity-ensuring function ($HMAC$ in our case), and restarts attestation.

In higher-end devices, memory locking can be used to prevent modifications until the end of attestation, as discussed in [17]. However, in low-end devices, where applications run on bare-metal and there is no architectural support for memory locking, temporal consistency is attained by enforcing that attestation software ($SW-Att$) runs atomically: once it starts, it can not be interrupted by any software running on $Prv$, thus preventing malware from interrupting $RA$ and moving itself around memory. This is the case in prominent hybrid $RA$ architectures, such as [4], [6], [7], [8], [33], [34], [3]. While effective for security purposes, this requirement conflicts with real-time requirements if $Prv$ serves a safety-critical function. For example, a smoke or CO$_2$ detector should not delay sounding an alarm because attestation is being executed.

Some prior remediation techniques proposed to enable interrupts while maintaining temporal consistency, with high probability. SMARM [35] is one such approach. (Others similar techniques are discussed in [36]). SMARM divides attested memory ($AR$) into a set of blocks which are attested in a randomized order. Attestation of one block remains atomic. However, interrupts are allowed between attestation of two blocks. Assuming that malware can not guess the index of the next block to be attested, even if interrupts are allowed, malware only has a certain probability of avoiding detection. If the entire attestation procedure is repeated multiple times, this probability can be made arbitrarily small.

We note that, given the $RATA$ optimization discussed in Section VII-A, attestation can be computed very quickly. In particular, since most Pseudo Random Function (PRF) implementations, use block sizes of at least 32 Bytes, the atomic attestation of one block in a SMARM-type strategy can not be made faster than the attestation on $LMT$ in $RATA$ ($|LMT| = 32$ Bytes). In addition, attestation of $LMT$ provides information about the content of $AR$ in its entirety with no probability of evasion. We believe this makes $RATA$ more friendly to safety-critical operations than existing approaches.
In such settings, we envision that $AR$ would be attested in its entirety at system boot time (Case-2 in Section VII-A) while subsequent RA would be computed on $LMT$ only (Case-1 in Section VII-A). We note that, if $AR$ is eventually modified, $Prv$ would need to fall back into Case-2 for the next RA computation, which takes time to run atomically. However, after an unauthorized modification to $Prv$ memory, it is unclear why one would still want to offer real-time guarantees to compromised software. On the other hand, authorized modifications (e.g., benign software updates) could be still occur and be scheduled outside periods of real-time demands.

C. Collective RA Protocols and Device-to-Device Malware Relocation

Collective RA protocols (CRA) (a.k.a. swarm attestation) \[37, 38, 10, 39, 40, 41, 42\] fall into a set of techniques to attest a large number of devices that operate together as a part of a large system. CRA schemes typically assume hybrid RA architectures on individual devices and look into how to attest many devices efficiently. One security problem that is typically out of scope on single-device RA and becomes relevant in CRA settings is caused by migratory malware. This is an analog of intra-device self-relocating malware (discussed in Section VII-B) that appears in collective settings. Specifically, instead of moving around inside the memory of the same device, it migrates from device-to-device to avoid detection.

To guarantee detection of migratory malware, CRA result must convince $Vrf$ that all devices were in a safe state within the same time window, implying that malware had no destination device to migrate and avoid detection. Consequently, if a single-device attestation result conveys a safe state only at some point in between the execution of Request and Verify algorithms, it is nearly impossible (specially in the presence of network delays) to conclude that migratory malware is not present in the swarm. This problem is discussed at large in the CRA literature, however, existing approaches either leave it out of their adversarial model \[10, 37, 38, 41\], or make a strong assumption about clock synchronization among all devices in the swarm \[20, 39, 40, 42\] such that all devices can be scheduled to run Attest at the same time.

**Theorem 3:** In Construction 3 if for all $Prv_i \in S$, Verify($Prv_i$) in step 2 succeeds for some $t(LMT_i)$, then it must be the case that entire $S$ was in a valid state in the time window defined by the interval:

\[
\text{ assuming equation 20 constitutes a valid interval.}
\]

**Proof:** (Sketch) The proof follows directly from the observations that:

- Given RA-Security, for each $Prv_i \in S$, a valid response cannot be produced before the time when $Prv_i$ receives Chal, which is strictly greater than $t(Req_i)$.
- Given TOCTOU-Security, for each $Prv_i \in S$ with Verify($Prv_i$) = 1, its memory could not have been changed between $t(LMT_i)$ and the first call to Attest after $t(Req_i)$.

D. Runtime Attestation

Runtime attestation focus on detection of runtime attacks providing authenticated information about software execution on $Prv$. While this seems unrelated to detection of retrospective memory modifications (studied in this paper), we argue that RATA can also offer improvements to runtime attestation approaches.

Proofs of execution for embedded systems were recently explored in \[3\] (APEX). They are used to prove that a remote $Prv$ executed the expected code and to authenticate that outputs were indeed produced by this execution and could no have been spoofed or modified. Control Flow Attestation (CFA), introduced in \[2\] (C-FLAT), allows $Vrf$ to verify whether software executed on $Prv$ took a specific (or set of) valid control path(s).

We note that regular (or static) RA (allowing measurement of memory content) is a common stepping stone in these respective functionalities. In C-FLAT, the executable must be instrumented with specific instructions to enable CFA and RA is used to verify that such instructions were not removed or modified. Besides, executions with the same control flow path can have different behaviors if their instructions differ. In APEX, execution is proved to $Vrf$ with attestation of execution metadata. However, without attesting the corresponding executable in program memory, this proof would have no meaning other than “some code executed successfully”.

---

**Construction 3 (CRA-RATA):** Let $S = \{Prv_1, ..., Prv_n\}$ denote a swarm of $n$ devices individually equipped with RATA$_B$ hybrid RA facilities. Let $LMT_i$ be the value of LMT in $Prv_i$. Also, $\text{Verify}(Prv_i)$ denotes the verification algorithm of Construction 2 for $Prv_i$. Consider a simple CRA protocol in which:

1. $Vrf$ executes RATA$_B$ protocol, as defined in Construction 2 with each $Prv_i$, in parallel. Let $t(Req_i)$ denote the time when $Vrf$ requested the $Prv_i$.
2. $Vrf$ collects all responses and computes $\text{Verify}(Prv_i)$ for all $Prv_i \in S$. It then uses the values of $LMT_i$ to learn “since when” $Prv_i$ has been in a valid state. We denote this time as $t(LMT_i)$.

Here we argue that, by addressing the TOCTOU problem in the single-device setting without requiring synchronization, RATA$_B$ can be utilized to construct the first CRA protocol secure against migratory malware without relying on synchronization of the entire swarm. To see why this is the case, consider Construction 3. In this construction, the TOCTOU-secure guarantee from individual devices allows $Vrf$ to conclude that each $Prv_i$ was in a valid state within a fixed time interval. Therefore, by checking for the overlap of the valid interval of all $Prv_i$, $Vrf$ can learn the time window in which the entire swarm was safe as a whole, or detect migratory malware when such time window does not exist. Theorem 3 states the concrete guarantee offered by Construction 3.

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In many runtime attestation applications, the same code is expected to remain in memory for long periods, while its proper execution (or control flow) must be verified repeatedly. This case happens, for instance, in one of the main motivations for proofs of execution in APEX: building IoT/CPS sensors that (even if infected) can not lie about their sensed quantities. Hence, proofs of execution for the same executable (implementing the sensing task) should be provided along with each execution (whenever the sensing task is performed). It is not hard to imagine similar cases for CFA. In all such cases, RA can be used to reduce the overhead involved on RA computation of successive runtime attestations. In APEX specific example, all runtime overhead vis-a-vis cost of executing the same software without proving its execution to Vrf, is caused by the cost of RA. We believe that the optimization discussed in Section VII-A can bring significant improvement to this and similar applications.

VIII. Related Work

– Remote Attestation (RA): RA techniques generally fall into three categories: hardware-based, software-based and hybrid. Hardware-based techniques [43], [8], [44], [45] either perform RA using a dedicated autonomous hardware component (e.g., a TPM [8]), or require substantial changes to the underlying instruction set architecture in order to support execution of trusted software (e.g., SGX [46]). Such changes are too expensive for cost-sensitive low-end embedded devices. On the other end of the spectrum, software-based techniques [47], [48], [49] require no hardware security features; they perform RA using a custom checksum function implemented entirely in software. Security of software-based techniques relies on a precise measurement timings, which is only applicable to settings where the communication delay between Vrf and Prv is negligible and/or constant, e.g., communication between peripherals and a host CPU. Thus, software-based RA is unsuitable for environments where RA must be performed over the internet. Whereas, hybrid RA is particularly suitable for low-end embedded devices. It provides the same security guarantees as hardware-based RA, while minimizing modifications to underlying MCU hardware. Current hybrid RA techniques [4], [5], [6], [7], [11], [33] implement the integrity-ensuring function (e.g., MAC) in software, and use trusted hardware to control execution of this software, preventing any violations that might cause RA security problems, e.g., gadget-based attacks [50] or key leakage. This paper represents a paradigm shift of hybrid RA, by having trusted hardware additionally providing some context about Prv’s memory state.

– Temporal Aspects of RA: Besides TOCTOU, two other temporal aspects are essential for RA security: First, temporal consistency [17] means guaranteeing that the RA result reflects an instantaneous snapshot of Prv’s attested memory at some point in time during RA. Lack thereof allows self-relocating malware to escape detection by copying and/or erasing itself during RA. Temporal consistency is achieved by enforcing atomic (uninterruptible) execution of attestation code, or by locking attested memory (i.e., making it unmodifiable) during RA execution. Second, when RA is used on safety-critical and/or real-time devices [36], atomicity requirement might interfere with the real-time nature of Prv’s application. To address this issues, SMARM [35] relaxes this requirement by using probabilistic malware detection. Meanwhile, ERASmus [9] and SeED [20] are based on Prv’s self-measurements, in order to detect transient malware that infects Prv and leaves before the next RA instance. See Section III-C for further discussion on these types of techniques.

– Formal Verification and RA: Formal verification provides significantly higher level of assurance for hardware and software implementations. It yields provable security for protocol specifications and for the implementation thereof. Therefore, in recent years, several efforts focused on formal verification of security-critical services and systems [51], [52], [18], [53], [54], [55]. VRASED [7] realized a formally verified RA architecture targeting low-end devices. Other formally verified security services were obtained by extending VRASED to derive remote proofs of software update, memory erasure and system-wide MCU reset [1]. Another recent result is APEX – a formally verified VRASED-based architecture for proofs of remote software execution with authenticated outputs [3]. In this work, we also use VRASED RA architecture as the base and modify it to provide TOCTOU security while retaining its original guarantees. Using VRASED allows us to reason about RA design and to formally verify its security properties. However, RA’s main concepts are applicable to other hybrid (and possibly hardware-based) RA architectures.

IX. Conclusions

In this paper, we design, prove security of, and formally verify two designs (RATA and RATAc) to secure RA against TOCTOU-related attacks. RATA and RATAc modules are formally specified and verified using a model-checker. They are also composed with VRASED – a verified RA architecture. We show that this composition is TOCTOU-secure using a reduction-based cryptographic proof. We also describe working prototypes of RATA and RATAc. Our evaluation demonstrates that a TOCTOU-Secure design is affordable even for cost-sensitive low-end embedded devices.

Possible directions for future work include the implementation of RATA in different types of RA architectures (e.g., hardware-based ones, such as SANCUS [45]) and the development of different approaches to tackle the TOCTOU problem. It would also be interesting to analyze what other security services that build on top of RA could be optimized by RATA capability. Finally, we believe that further investigation could result in more techniques to tackle TOCTOU in the context of RA, with different sets of requirements and guarantees.

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A \- \textit{Vrf} authentication details

To prevent an adversary from impersonating \textit{Vrf} and sending fake attestation requests to \textit{Prv}, \textit{VRASED} design supports authentication of \textit{Vrf} as part of \textit{SW-Att} execution. The implementation is based on the protocol in \cite{sw-att}. In this protocol, \textit{Chal} is chosen by \textit{Vrf} as a monotonically increasing nonce. As such, for subsequent requests \textit{i} and \textit{i}+1, it is always the case that \textit{Chal}_i < \textit{Chal}_{i+1}.

Figure 9 shows \textit{VRASED} C implementation of \textit{SW-Att}, including \textit{Vrf} authentication. It also builds upon HACL\* verified HMAC to authenticate \textit{Vrf}, in addition to computing the authenticated integrity check over \textit{AR}. In this case, \textit{Vrf}'s request additionally contains an HMAC of the challenge computed using \textit{K}. Before calling \textit{SW-Att}, software running on \textit{Prv} is expected to store the received challenge on a fixed address \textit{CALL_ADDR} and the corresponding received HMAC on \textit{VRF AUTH}. \textit{SW-Att} discards the attestation request if (1) the received challenge is less than or equal to the latest challenge, or (2) HMAC of the received challenge is mismatched. After that, it derives a new key using HKDF \cite{hkdf} from \textit{K} and the received HMAC and uses it as the attestation key.

To support secure authentication, \textit{VRASED} extends HW-MOD with two additional properties to make the memory region that stores \textit{Prv}'s counter immutable to untrusted applications (any software except \textit{SW-Att}). Notably, the counter requires persistent and writable storage, because \textit{SW-Att} needs to modify it at the end of each attestation execution.

B \- Proof of Theorem \[2\]

\textbf{Proof:} By contradiction, assume a polynomial \textit{Adv} that wins the game in Definition \[3\] with probability \textit{Pr}[\textit{Adv}, RA-TOCTOU-game] > \textit{negl}(1). Therefore, \textit{Adv} is able to produce response \textit{LMT}_{\textit{Adv}}|\textit{H}_{\textit{Adv}} such that:

\[
\exists t_0 \leq t_1 \leq t_{att}, \{ AR(t_i) \neq M \}
\]

By definition, in Construction \[2\], \textit{Verify} outputs 0 if \textit{LMT}_{\textit{Adv}} does not exist in Table \(T\) (step number 2 in \textit{Verify}). Moreover, if \textit{LMT}_{\textit{Adv}} is indeed present it must correspond to a challenge value sent before \(t_0\) (step number 3 in \textit{Verify}). Therefore, in order to win, \textit{Adv} must choose \textit{LMT}_{\textit{Adv}} restricted to values of challenges issued before \(t_0\).

Since \textit{LMT} \in \textit{AR}, by claiming a value for \textit{LMT}_{\textit{Adv}} fitting the restriction above, \textit{Adv} causes the expected memory value \(M\) to also reflect, \textit{LMT} = \textit{LMT}_{\textit{Adv}}. At this point, \textit{Adv} has two possible actions: to modify \textit{AR} to call \textit{Attest} with \(AR(t_{att}) = M\); or to obtain \(H_{\textit{Adv}}\) even with \(AR(t_{att}) \neq M\). First we show that the latter is \textit{Adv}'s only option.

Let us say that \textit{Adv} attempts to set \(AR(t_{att}) = M\) to call \textit{Attest}. In this case, we highlight three observations about \textit{RATAB}:

1) By LTL statement \[19\] any modification to \textit{AR} in between the \(i\)-th and \((i+1)\)-th authenticated computations of \textit{Attest}, will cause \textit{AR} to change to reflect \textit{LMT} = \textit{Chal}_{i+1} following \textit{RA} responses. Therefore, the premise that

\[
\exists t_0 \leq t_1 \leq t_{att}, \{ AR(t_i) \neq M \}
\]

will necessarily update \textit{LMT}.

2) From \textit{VRASED} authentication (see Appendix \[A\]), for subsequent \textit{RA} challenges \textit{Chal}, \textit{Chal}_{i+1} that authenticate successfully, it is always the case that \textit{Chal}_i < \textit{Chal}_{i+1}.

3) From LTL statement \[18\] \textit{RATAB} never updates \textit{LMT} with a challenge if it does not authenticate successfully. Since authentication implies \textit{Chal}_i < \textit{Chal}_{i+1}, a call to \textit{Attest} never causes \textit{LMT} to be updated to a previously used \textit{Chal}.

From observations 1, 2, and 3 above, it is impossible to set \textit{AR} = \textit{M} by calling \textit{Attest}, because any modification to \textit{LMT} caused by \textit{Attest} will always change \textit{LMT} to a value that was never used before and thus not present in table \(T\). Now \textit{Adv} last resource is to try to write to \textit{LMT} directly. However, this is immediately in conflict with LTL property \[17\].

Since making \textit{AR}(t_{att}) = \textit{M} is impossible after a modification at time \(t_0\), the assumption that \textit{Adv} wins the game in Definition \[3\] implies that \textit{Adv} is able to produce \textit{H}_{\textit{Adv}} that verifies successfully even when \(AR(t_{att}) \neq M\). To conclude the proof, we show that existence of such \textit{Adv} implies existence of another adversary \textit{Adv}_{\textit{RA}} that wins the \textit{RA} security game in Definition \[2\].

To win the game in Definition \[2\], \textit{Adv}_{\textit{RA}} is constructed as follows:

1) At time some \(t_i\), where \(t_0 \leq t_i \leq t\), \textit{Adv}_{\textit{RA}} modifies memory in \textit{AR}.

2) \textit{Adv}_{\textit{RA}} receives \textit{Chal} in step 2 of \textit{RA} security game of Definition \[2\] and executes the same algorithm as \textit{Adv} on \textit{Chal} and with \(t_{att} = t\) to produce \textit{H}_{\textit{Adv}} such that \textit{Verify}^{\textit{Vrf}}(\textit{H}_{\textit{Adv}}, \textit{Chal}, \textit{M}, t_0, T, \textit{LMT}_{\textit{Adv}}) = 1 with probability:

\[
\text{Pr}[\textit{Adv}, \textit{RA-TOCTOU-game}] > \text{negl}(1).
\]

3) As a response in step 3 of the game in Definition \[2\], \textit{Adv}_{\textit{RA}} replies with \(\sigma = \textit{H}_{\textit{Adv}}\).
Since $\text{Verify}^{\text{rf}}(H_{\text{Adv}}, \text{Chal}, M, t_0, T, LMT_{\text{Adv}}) = 1$, it follows that $\sigma = \text{HMAC}(\text{KDF}(K, \text{Chal}), M)$ (first condition for $\text{Adv}_{\text{RA}}$ to win), for expected $M$ containing $LMT = LMT_{\text{Adv}}$. On the other hand, because memory was modified at time $t_i$, it must be the case that $AR(t)$ has $LMT \neq LMT_{\text{Adv}}$. Thus satisfying the remaining condition that $AR(t) \neq M$ implying that $\text{Adv}_{\text{RA}}$ wins the game in Definition 2 with probability:

$$Pr[\text{Adv}, \text{RA-game}] = Pr[\text{Adv}, \text{RA-TOCTOU-game}] > \text{negl}(1)$$

(21)