Occam: Optimal Data Reuse for Convolutional Neural Networks

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Abstract—Convolutional neural networks (CNNs) are emerging as powerful tools for image processing in important commercial applications. We focus on the important problem of improving the latency of image recognition. While CNNs are amenable highly to prefetching and multithreading to avoid memory latency issues, CNNs’ large data – each layer’s input, filters, and output – poses a memory bandwidth problem. While previous work captures only some of the enormous data reuse, full reuse implies that the initial input image and filters are read once from off chip and the final output is written once off chip without spilling the intermediate layers’ data to off-chip. We propose Occam to capture full reuse via four contributions. First, we identify the necessary condition for full reuse. Second, we identify the dependence closure as the sufficient condition to capture full reuse using the least on-chip memory. Third, because the dependence closure is often too large to fit in on-chip memory, we propose a dynamic programming algorithm that optimally partitions a given CNN to guarantee the least off-chip traffic at the partition boundaries for a given on-chip capacity. While tiling is well-known, our contribution is determining the optimal cross-layer tiles. Occam’s partitions reside on different chips forming a pipeline so that a partition’s filters and dependence closure remain on-chip as different images pass through (i.e., each partition incurs off-chip traffic only for its inputs and outputs). Finally, because the optimal partitions may result in an unbalanced pipeline, we propose staggered asynchronous pipelines (STAP) which replicates the bottleneck stages to improve throughput by staggering the mini-batches across the replicas. Importantly, STAP achieves balanced pipelines without changing Occam’s optimal partitioning. Our simulations show that, on average, Occam cuts off-chip transfers by 21x and achieves 2.06x and 1.36x better performance, and 33% and 24% better energy than the base case and Layer Fusion, respectively. Using an FPGA implementation, Occam performs 5.1x better, on average, than the base case.

I. INTRODUCTION

Advances in convolutional neural networks (CNNs) [18], [24], [27], [36] have resulted in highly-accurate image classification and recognition. Current commercial applications are speech-based (e.g., voice assistants) which employ other types of neural networks (e.g., Long Short-Term Memory networks), so that CNNs currently contribute only 5-10% to machine learning workloads [22]. However, emerging image-based applications (e.g., self-driving cars) are poised to increase this contribution, as anticipated by several commercial CNN architectures (e.g., Movidius, Nervana, Nvidia).

A CNN employs numerous filters to identify features which are combined into higher-order features so that each CNN layer applies the current layer’s filters to the previous layer’s output features and outputs the next set of features, and eventually the final classification output. Each layer applies a set of filters to its input feature map by convolving each filter with the input map in two dimensions – i.e., “sliding” the filter along the input’s two dimensions – to extract the corresponding feature. Each layer simply puts together its filter results as its output map. The weights in the filters are trained by reducing the error for the training inputs via back propagation. Like most previous CNN work, this paper focuses on the recognition phase. Further, this paper targets reducing the latency of recognition as opposed to improving the throughput. The latency goal is important for many interactive scenarios (e.g., self-driving cars) where trading-off latency for throughput is unacceptable [22].

The large number of layers (e.g., 34 in resnet) and filters per layers (e.g., 192), and large images (e.g., 224 x 224), result in heavy compute and large intermediate data. The heavy compute is somewhat offset by the abundance of regular parallelism amenable to GPGPUs [24], FPGAs [14], [37], and TPUs [22]. Recent work prunes the compute by using 8-bit fixed-point representation [29] or by exploiting zeroes in the data [1], [2]. TPU optimizes the compute via a novel systolic multiply-add array. However, the large intermediate data remains a challenge for performance especially because more training data achieves higher accuracy but needs larger networks to avoid over-fitting [43]. Because we target data reuse, we describe CNNs in terms of the access patterns instead of neurons and synapses. Because CNNs are amenable to prefetching and multithreading, the problem is memory bandwidth and not memory latency [22].

In the convolution, as the filters “slide over” the input map, each input cell participates in many computations which are repeated for each filter. Each weight cell in a filter is reused by each input map cell. Further, each layer’s output map is the next layer’s input map. All of this reuse is for one input image and only in the convolution layers whereas other, fully-connected (FC) layers, do not have any reuse. The former account for more than 85% of execution time in earlier CNNs [24] and hence our focus, the latter are used only as the last layer in recent CNNs (e.g., GoogLeNet).

Current practice is to write off-chip each layer’s output map which is read back in by the next layer, losing inter-layer reuse. DianNao [6] and its successors [8], [12], [30] propose to reduce the off-chip traffic by placing all of the intermediate data and filters in an on-chip eDRAM, which may
be inefficient (e.g., 50 and 21 MB for VGGnet and Resnet). Other work propose to compress the data for the FC [15] and convolutional layers [1], [34]. While such compression reduces both the compute and memory volumes, the all-or-nothing approach works well only if the compressed data fits on-chip memory and otherwise, generates off-chip traffic (e.g., recent CNNs may require several MBs even after compression). Further, such compression destroys compute and data access regularity hurting efficiency of GPGPUs, TPU and FPGAs (SCNN employs crossbars for the irregularity).

Exploiting reuse with reasonable on-chip memory to reduce the off-chip traffic is challenging. Capturing full reuse implies that the initial input image and filters are read once from off-chip and the final output is written once off chip without spilling the intermediate layers’ data to off-chip. Because the filters have high reuse, they are held on-chip (e.g., Eyeriss [7]), similar to our on-chip residence though the architectures hold at a time only one layer’s filters and reload each layer’s filters once per input image. Further, capturing inter-layer reuse requires holding on-chip a layer’s output map to be read by the next layer. An output map cell depends on many input map cells – the output cell’s dependence parents, due to a dot product sub-computation in each convolution; and many output map cells share the same dependence parents, which provides reuse. These output maps’ dependence ancestors transitively extend to include the corresponding input maps of the earlier layers. Accordingly, Layer Fusion [3], a pioneering work, holds only the ancestors of an output map tile to capture some of the inter-layer reuse. While conventional tiling holds only the parents, this cross-layer tiling holds some or all of the ancestors similar to other work [33], [35] (Section V).

Despite these significant advances, none of the papers captures full reuse. To that end, we propose Occam and make the following contributions:

First, the necessary condition to exploit full reuse with the optimum (smallest) amount of on-chip memory is to hold one full input map row or column, whichever is shorter. Due to convolution, each input map cell is a dependence parent of many output map cells along both dimensions. Capturing such two-dimensional reuse requires holding the full shorter dimension. Thus, the necessary condition determines the optimal tile shape. Unlike matrix multiply, a canonical tiling candidate, the tile shape matters for CNNs (Section III-A). Layer Fusion’s tile, derived from another work [44], does not satisfy this condition incurring expensive recomputation triggered by reuse not captured on-chip.

Second, Occam achieves full reuse by satisfying the sufficient condition of holding only the ancestors of a full output row or column all the way through all the layers to the initial input image – i.e., the transitive closure of the dependence ancestors, called the dependence closure (receptive field in machine learning). Layer Fusion identifies the closure but not for the full output row (the necessary condition).

Third, because a CNN’s full dependence closure is often too large to fit in one chip’s memory, we partition the CNN into sets of contiguous layers so that each partition’s dependence closure fits on-chip (each partition reads its input map from and writes its output map to off-chip). Layer Fusion chooses sub-optimal partitions because its exhaustive search is infeasible for large networks (e.g., $2^{34}$ choices in Resnet). Instead, we propose a dynamic programming (DP) algorithm that optimally partitions a given CNN to guarantee the least off-chip traffic at the partition boundaries for a given on-chip memory capacity. While tiling is well-known, our contribution is determining the optimal cross-layer tiles. Fortunately, Occam’s optimal partitions and tiles preserve CNNs’ regular parallelism unlike prior compression work.

Finally, the input-stationary approach [7] holds on-chip the input/output maps and fetches the filters from off-chip, ignoring filter reuse across images (e.g., TPU). Occam’s partitions reside on different chips (e.g., GPU, TPU, or FPGA), forming a pipeline so that a partition’s filters and dependence closure remain on-chip as different images pass through (i.e., each partition incurs off-chip traffic only for its inputs and outputs). Occam amortizes filter loading to asymptotically zero cost over numerous images to achieve full cross-image reuse. While BrainWave [13] holds the filters on-chip, its partitions are ad hoc, do not employ tiling, and may incur pipeline imbalance. Because Occam’s optimal partitions may also result in an unbalanced pipeline, we propose staggered asynchronous pipelines (STAP) which replicates the bottleneck stages to improve throughput by staggering the mini-batches across the replicas. Importantly, STAP achieves balanced pipelines without changing Occam’s optimal partitioning.

DP is a widely-used meta algorithmic method for diverse problems. While our optimal DP formulation targets on-chip memory, another, heuristic formulation [37] targets FPGA compute resources for CNNs. Similarly, PipeDream [16], [17] employs DP to minimize pipeline imbalance in training for a given pipeline depth without any data reuse considerations whereas Occam optimizes data reuse in inference for a given cache capacity without constraining the pipeline depth. Further, because the large data is problematic for any CNN architecture, such as GPGPU, TPU, or FPGA-based, Occam is applicable to all the architectures.

Our simulations show that, on average, Occam cuts off-chip transfers by 21x and achieves 2.06x and 1.36x better performance, and 33% and 24% better energy than the base case and Layer Fusion, respectively. Using an FPGA implementation, Occam achieves 5.1x better average performance than the base case.

II. REUSE IN CNN

As mentioned in Section I, a CNN comprises of many layers each of which employs many filters to extract higher-order features. A layer’s output map is the next layer’s input map. In general, each layer’s input map is a cuboid whose height $h$, width $w$, and channel count $m$ are analogous to the input image’s height and width and three colors ($R$, $G$, and $B$); $m$ is the number of filters in the previous layer (Figure 1).

Each filter is another cuboid whose height and width are typically equal, $k$, and the channel count is the same as the
A cell is a various slid-over positions (assuming the convolution stride is 1 slice of a cuboid – a scalar.

Each output map cell is computed by a cuboidal product of the input map and a filter (see the faint arrows from the Inputs to Layer 1 in Figure 1). The next output map cell results from the product with the filter “slid over” by a stride along the height and width dimensions, one at a time, in a two-dimensional convolution. There is no sliding along the third dimension of channels. Thus, each cell in a layer’s input map, except for those at the boundaries, is reused \(k \times k\) times by a filter in its various slid-over positions (assuming the convolution stride is 1); this reuse is called convolutional reuse. With \(n\) filters in a layer, each input map cell produces \(n\) output cells in the output channel dimension (Figure 1). Thus, each input map cell is reused by an additional factor of \(n\) called cross-filter reuse, for a total reuse of \(k \times k \times n\) times (e.g., for a layer with 128 3 x 3 filters, there is 1152 times reuse). Further, each layer’s output map is the next layer’s input map, providing another instance of reuse, called inter-layer reuse, for a total reuse of \(k \times k \times n + 2\) times.

Past implementations use im2col to transform the convolution into a matrix multiply. To that end, the implementations replicate the input map cells for every slide position of the filters so that each filter can be matrix-multiplied with an input-map tile of the same size. However, the replication causes enormous memory bloat (k-by-k filters cause \(k^2\) redundancy). Therefore, our and other recent implementations do not take this approach. However, there may be some replication in the private L1 caches due to parallel execution.

\section{Reuse in filters}

A layer’s filters are used only in that layer. Because each weight cell in a filter is “slid over” every input map cell in the height and width dimensions, each cell is reused \(h \times w\) times, ignoring boundaries (typically, \(h, w >> k\)). To capture this reuse, current practice applies one filter at a time to the entire input map, refetching the input map, if too large to be held on chip, for every filter. In addition to capturing the filter reuse, this approach also captures the \(k \times k\) times reuse of the input map. However, the approach does not capture all the

\section{Occam}

Recall from Section II that Occam makes four contributions. First, we specify the necessary condition for full reuse in terms of the tile shape. Second, we propose an approach called Dependence Closure which satisfies the sufficient condition to capture full reuse using the least on-chip memory. Third, because the dependence closure for full reuse is often too large, we propose a dynamic programming algorithm that optimally partitions a given CNN while guaranteeing the least off-chip traffic at the partition boundaries for a given on-chip memory capacity. By holding the filters on-chip, our partitions achieve full cross-image reuse. Finally, we propose staggered asynchronous pipelining (STAP) to balance the pipeline formed by the partitions.

\subsection{A. Necessary condition}

Due to convolutional reuse, each input map cell of a layer is a dependence parent of many output map cells along both dimensions. For full reuse with rectangular filters\(^1\) we need to hold on-chip at least one full input map row-plane or column-plane, whichever is smaller. A row-plane corresponds to a

\footnote{We discuss non-rectangular filters at the end of this subsection.}
cuboid of dimensions $1 \times 1 \times n$, where $n$ is the number of channels. This condition identifies the tile shape necessary for full reuse.

To prove this condition, we make the following three simplifying assumptions (removed later): (1) a single input channel, (2) the input tile includes the element at $(0,0)$, and (3) a rectangular tile of dimensions $X_t \times Y_t$ from the input feature map of dimensions $X_{\text{max}} \times Y_{\text{max}}$. To minimize capacity misses, the largest tile that fits in the cache, called maximal tile, is used.

**Proof sketch:** To prove by contradiction, we assume that the input tile of dimensions $X_t \times Y_t$ does not span a full row (or column) (i.e., $X_t < X_{\text{max}}$ and $Y_t < Y_{\text{max}}$) and show that full reuse is impossible. Figure 2(a) shows the initial tile position. Because of the two-dimensional sliding nature of convolutional reuse, some elements at the boundaries of the input tile are dependence parents for output cells that cannot be computed fully with the current input tile data (red squares indicating future reuse). Moreover, such future reuse exists along both the $X$ and $Y$ dimensions.

We now show that any tile movement — even a single step in either the $X$ or $Y$ dimensions — rules out full reuse. Without loss of generality, a tile movement in the $X$-dimension by some positive stride $d$ (integer $d > 0$) means the corners of the tile are new at $(d,0),(d,Y_t),(X_t+d,0)$, and $(X_t+d,Y_t)$. Because of maximal tiles, all the elements in the original tile position but not in the new position are evicted. The evicted region’s corners are $(0,0),(0,Y_t),(X_t+d-1,0)$ and $(X_t+d-1,Y_t)$. At least one evicted element is guaranteed to have future reuse; For example, input $(0,Y_t)$ (black cell in Figure 2(a)) is needed to compute the output cell $(0,Y_{t+1})$ in the future. Eliminating the evicted input element’s future reuse by using the element to partially compute the output cell would require holding the output cell for future computation completion, shifting the problem from the input to the output. With such partial-compute strategy, the tile must include the appropriate partial output cells. Any tile movement would similarly evict a region of the partial output needed later.

**Removing our assumptions:** (1) Because the convolutional sliding occurs only in the $X$ and $Y$ dimensions and not in the $Z$ dimension of channels, the above argument holds for multiple channels (the tile is a cuboid). (2) Including $(0,0)$ in the initial tile position ensures full reuse of at least $(0,0)\ldots(X_t+d-1,0)$ along the $X$-axis tile boundary. Without this assumption, there are even more elements with future reuse at the top and left of the tile. (3) To generalize the tile shape, we observe that because the filters are rectangles or squares in the $X-Y$ dimensions (e.g., $3 \times 3$), the output element $(0,0)$ requires the input tile to include the three corner elements — $(0,0)$, $(0,Y_t)$ and $(X_t,0)$ with $X_{\text{max}} > X_t \geq 0$ and $Y_{\text{max}} > Y_t \geq 0$ — regardless of the tile shape. Now, the above proof (for rectangular tiles) holds by ignoring the fourth corner $(X_t,Y_t)$; the same element $(0,Y_t)$ that has future reuse remains evicted, leading to sub-optimal memory traffic.

Layer Fusion uses tiles from another work, which are not the full row-plane (or column-plane) and hence do not satisfy our necessary condition. That work casts determining the tile dimensions as an integer linear programming problem whereas we have shown that the full row-plane is necessary for full reuse. Unlike convolution, matrix multiply, a canonical candidate for tiling, does not have two-dimensional reuse. Assuming one matrix is held on-chip, any tile shape for the other works. In realistic scenarios, neither matrix can fit on-chip requiring tiling of both matrices unlike our problem.

Extending our necessary condition to the case of filters that are not fully-filled rectangular (e.g., dilated filters which are checkered with holes) remains a work-in-progress. For example, with a combination of dilated filters and strides, it is possible that there are holes in the input that are never used. Naive use of rectangular tiles may result in fetching the data corresponding to the “holes” unnecessarily, thus being non-optimal. However, in such cases, it may be possible to preprocess the input to eliminate the holes (which are unused parts of the input), in which case the necessary condition may hold in the pre-processed input without holes.

**B. Sufficient condition**

Holding only one input map row-plane (or column-plane) is not sufficient for full reuse. Observe that a layer’s output map cell is computed using many input map cells — the output map cell’s dependence parents, and that many output map cells share the same dependence parents. Fully capturing the reuse of these common parents in a single layer requires holding on-chip all of them until all the dependent output map cells of the layer are computed. Combined with the above necessary condition, this single-layer sufficient condition amounts to holding all the input map row-planes that are the dependence parents of an output map row-plane (i.e., $k$ input map row-planes are held if the filters dimensions are $k \times k \times m$). As mentioned in Section I-B a layer in a residual CNN gets an additional input map from a previous layer. In such CNNs, an output map row-plane’s dependence parents also include that layer’s relevant output map row-planes.

Assuming each layer reads the input map from and writes the output map to off chip, the on-chip memory needs to hold all the filters and the first $k$ input map row-planes to compute the first output map row-plane (all the $n$ output map channels). To produce the next output map row-plane, the next set of new input map row-planes, as defined by the convolution stride, replace those input map row-planes that are no longer needed (Figure 2(b)). This strategy, employed in Eyrisis, captures $k \times k \times n$ times input reuse requiring $2 + l$ input map refetches between layers. To capture this reuse in a layer, the on-chip memory must fit all the filters and $k$ row-planes of the input

![Fig. 2. Necessary condition and sufficient condition](image-url)
map (the output map is written off-chip). The amount of on-chip memory needed is the maximum across all the layers.

One way to avoid the above assumption of off-chip traffic between consecutive layers is to hold on-chip, at a time, only one layer’s input map and output map. Because a layer’s output map is needed only by the next layer, this strategy guarantees full reuse. However, there is often no room on-chip for the layer’s filters, losing the massive cross-image reuse of filters captured by Occam.

C. Dependence Closure

To avoid all traffic between layers (i.e., full reuse), the single-layer sufficient condition has to be extended to all the layers’ output maps. The output maps’ dependence ancestors transitively extend to include the corresponding input maps of the earlier layers, as observed by Layer Fusion [3] (the solid boxes in Figure 3). The set of dependence ancestors expands at each earlier layer in an arithmetic sequence induced by the convolution’s stride (e.g., one row-plane of output map depends on three row-planes of input map which, in turn, together depend on five row-planes of the previous layer’s input map, and so on). The full set of the ancestors of a final output map row-plane or column-plane through all the layers to the initial input, called the dependence closure, satisfies the all-layer sufficient condition. In residual CNNs, the dependence closure does not change due to the residual input maps which are also fed as non-residual input maps to a previous layer and thus are present already in the closure. As noted in Section II, while conventional tiling typically holds only the dependence parents, this cross-layer tiling holds all the dependence ancestors.

Thus, the dependence closure defines the shape and size of the optimum tile to achieve full reuse. In contrast, Layer Fusion holds the ancestors of an output map tile that does not satisfy the necessary condition. As such, Layer Fusion captures between \( k \cdot n + 2 \) and \( k \cdot k \cdot n \) times input map reuse with the same on-chip memory as Occam (i.e., between \( 2 \cdot l \) and \( k \cdot l \) input map refetches for \( l \) layers assuming all the layers’ input maps and output maps are the same size). As noted in Section II, while conventional tiling typically holds only the dependence parents, this cross-layer tiling holds all the dependence ancestors.

Under dependence closure, execution proceeds by computing only the required number of output map row-planes in each layer as per the above arithmetic sequence to produce the first row-plane of the final output. While the initial input is read from off-chip and the full output is written off-chip, the full dependence closure data (i.e., the relevant partial output map of all the layers) is held on-chip. Going from the final output’s top row-plane to the next row-plane, the dependence closure also slides down at each layer by the layer’s convolution stride (see the broken boxes in Figure 3). Because the stride is much smaller than the arithmetic sequence values, the dependence closures of consecutive final output row-planes overlap greatly. Occam captures this overlap by holding on-chip the entire closure until needed and replacing only the unneeded, older parts of the closure with newer parts. Because Layer Fusion does not satisfy our necessary condition, it does not hold the entire closure. Instead, Layer Fusion proposes to recompute the missing parts of the closure (and to refetch the relevant input). However, the large overlap implies significant amount of recomputation added to the already compute-intensive CNNs.

To produce the final output’s second row-plane, the first layer discards (1) the top input map row-planes no longer needed, replacing them with the next set of input map row-planes as per the convolution stride, and (2) the output map row-planes in the temporary space that are no longer needed, overwriting them with the next set of output map row-planes. Thus, the temporary space acts conceptually as a circular buffer for the relevant input map and output map row-planes, similar to Layer Fusion. This circular buffer repeatedly reuses its space to hold the dependence closure of subsequent final output row-planes, conserving on-chip memory capacity. Later layers follow the same strategy (i.e., each layer has its own circular buffer of size defined by the arithmetic sequence). Because the computation crosses all the layers to produce each final output row-plane, all the layers’ filters need to be held on-chip along with the dependence closure.

The local operations for batch normalization, pooling, bias addition, and ReLU (Section II-B) occur as part of each layer’s computation without affecting the dependence closure.

D. Optimal Partition

Real CNNs’ full set of filters and dependence closures are too large to fit in one chip’s on-chip memory, or cache. Therefore, we partition a given CNN into sets of contiguous layers where each partition’s dependence closure fits in the cache. Each partition reads its input once from and writes its output to off-chip memory. Layer Fusion [3] explores such partitioning via brute-force search which is infeasible for modern CNNs which may have more than 100 layers. Instead, we propose a dynamic programming (DP) algorithm to guarantee the least off-chip traffic for a given CNN and cache capacity while ensuring that filters remain cache-resident to capture cross-image filter reuse. We use a running example (Figure 4) for illustration.

Our formulation uses the following definitions:

- \( L_i \) and \( W_i \) define the input feature map data and filters, respectively, for the \( i \)th layer. \( |L_i| \) and \( |W_i| \) define the number of elements in \( L_i \) and \( W_i \), respectively, independent of data format (e.g., FP32, FP16, INT8). \( L_0 \) is the input image. Figure 4(a) shows the four feature maps (\( L_0 \) through \( L_3 \)) and the three layers’ weights (\( W_0 \) through \( W_5 \)) for our example.
We assume the cache can hold \( C \) elements (\( C = 1024 \) in Figure 4(a)).

DC(i,j) defines the dependence closure of one row-plane of the output feature map in \( L_j \) extending back to the feature map of layer \( L_i \) where \( 0 \leq i < j \leq n \) and \( n+1 \) is the number of layers. Thus, the end-to-end dependence closure defined earlier in Section III-C has \([DC(0,n)]\) elements.

We define a SPA\( N(i,j) \) as the convolution computations starting with \( L_i \) as the input and ending with \( L_j \) as the output.

For on-chip resident filters, the minimum total footprint of all convolutional layers is the sum of all weights (\( \sum_{i=1}^{p} W_i \)) and the full dependence closure \((DC(0,n))\). If this footprint fits in the cache, then optimal operation needs no partitioning. Otherwise, the layers must be partitioned into spans such that (1) each SPA\( N(i,j) \) satisfies the capacity constraint that the dependence closure (i.e., \( |DC(i,j)| \)) and weights (i.e., \( \sum_{i=1}^{p} W_i \)) of the span must fit in the cache, and (2) the total amount of data transferred off-chip at the partition boundaries is minimized.

**Definition 1:** For a CNN with \( n \) convolutional layers, we define a partition boundary set (PBS) as a set \( P = \{p_1, p_2, \ldots, p_{k-1}\} \) that specifies a partitioning of the CNN into \( k \) spans — SPAN(0, \( p_1 \)), SPAN(\( p_1, p_2 \)), \ldots, SPAN(\( p_{k-1}, n \)). Here, we assume that the elements of \( P \) are strictly increasing integers (i.e., if \( i < j \) then \( p_i < p_j \)) that lie between 0 and \( n \). For uniform naming of partition boundaries, we define \( p_0 = 0 \) and \( p_k = n \).

In a valid PBS, each span’s footprint fits in the cache:

\[
\forall 0 \leq n \leq n, (|DC(p_{i+1}, p_i)| + \sum_{k=p_{i+1}}^{p_i} |W_1|) < C
\] (1)

Further, for any SPAN(\( p_{i+1}, p_i \)) specified by such a PBS, the associated computation may run on a single chip. The only off-chip transfers are (1) reads of the input layer which transfers \( |L_{p_i}| \) elements from off-chip memory (or upstream chips), and (2) writes of the output layer which transfers \( |L_{p_{i+1}}| \) to off-chip memory (or downstream chips).

Informally, our problem fits DP because optimally partitioning a network into two would require that the “left” and “right” sub-partitions themselves be optimal. This claim is sound because of the optimal substructure property of the problem [10], which can be proved easily by contradiction as follows. If the optimal solution to the SPAN(\( i,j \)) uses suboptimal solutions (i.e., partitions that yield more transfers) to a recursive subproblem, using the optimal solution for the subproblem yields fewer overall transfers than the optimum.

In our DP table \( OP[n, n] \), each cell \( OP[i, j] \) holds three fields of information on the optimal partition of an arbitrary span from \( L_i \) to \( L_j \): (1) \( p \), the feature map that marks the optimal point of partition between \( L_i \) and \( L_j \), and (2) \( X \), the optimal number of transfers. Figure 4(b) shows the OP table for our example, wherer \( F \) denotes the footprint of the largest sub-span within the span as per the optimal partition.

**DP base case:** In the base case, if the entire footprint (filters + DC) of a SPAN(\( i,j \)) fits in cache (Eqn. (1)), we initialize the number of transfers as the bare minimum — every element in the input and output layers \( i \) and \( j \), respectively, is read and written exactly once (Eqn. (2)). Figure 4 shows the example’s footprints \( F \), even though they are not tracked in the DP table. Because the filter transfers are amortized to zero over multiple images, the filters are not counted in the transfers. Further, because no partitioning is necessary, \( p \) is set to null (Eqn. (3)).

\[
\begin{align*}
OP[i, j].X &= |L_i| + |L_j| \quad (2) \\
OP[i, j].p &= \text{null} \quad (3)
\end{align*}
\]

If single-layer spans (SPAN(\( i,i+1 \)) fit in the cache, we initialize \( OP[i, i+1], 0 \leq i < n \), using the above assignments, as shown with light shading in Figure 4(b) and Figure 4(c).

**Recurrence for other cases:** Our DP algorithm solves the optimal partition problem in a bottom-up fashion by increasing the span length beyond the base case of 1. A longer span either fits in the cache or not. The first case is treated exactly as the base case. \( OP[0,2] \) and \( OP[1,3] \) illustrate this case in Figure 4(b) and Figure 4(c). For the second case, we consider every possible partition of SPAN(\( i,j \)) and pick the partition point \( p \) that yields the fewest transfers in the two resulting sub-spans, SPAN(\( i,p \)) and SPAN(\( p,j \)).

\[
p_{\text{opt}} = \min |(i < k < j) | (OP[i, p].X + OP[p, j].X) \leq (OP[i,k].X + OP[k,j].X)
\]

The choice of the optimal partition point is shown in Figure 4(d). The algorithm compares the two choices (\( L_1 \) and \( L_2 \) and chooses \( L_2 \) which results in fewer transfers. We define the solution to longer spans SPAN(\( i,j \)) as:

\[
\begin{align*}
OP[i, j].X &= OP[i, p_{\text{opt}}].X + OP[p_{\text{opt}}, j].X \quad (4) \\
OP[i, j].p &= p_{\text{opt}} \quad (5)
\end{align*}
\]

The above recurrence accurately tracks the number of the off-chip transfers (i.e., \( X \)) of each of the two resulting spans (Eqn. (4)). Further, saving the partition points (\( p \)) facilitates...
reconstruction of the final optimal PBS (Eqn. (5)). Figure 4(b) shows the full computation of $\text{OP}[0,3]$ which yields the optimal partitions: SPAN(0,2) and SPAN(2,3).

Finally, a divide-and-conquer algorithm, instead of DP, would not be efficient here because of the numerous overlapping sub-problems. For example, the subproblem $\text{OP}(3,6)$ would be revisited when examining larger spans (e.g., $\text{OP}(2,8)$ and $\text{OP}(3,7)$). DP avoids such recomputation by memoizing the solutions in the OP table.

Extensions: The above algorithm extends easily to handle (1) residual connections such as those used in ResNets [18], and (2) batched computation for inference on a minibatch of multiple images.

Residual connections effectively read and aggregate values from upstream layers which results in additional transfers. Residual connections interact with Occam in one of two ways: either the residual connection does not span any partition boundary or it does. In the first case, Occam guarantees that the residual reads impose no additional off-chip transfers because the residual values are already in the dependence closure. In the second case, the residual values result in additional transfers as the residual values are already in the dependence closure. These additional transfers require a minor change to Eqn. (5) as follows.

\[
\text{OP}[i, j].X = \text{OP}[i, p_{opt}].X + \text{OP}[p_{opt}, j].X + 2 \times |L_{source}|
\]

Batched inference is used commonly in CNNs (say with a minibatch of $b$ images). The only change is that feature map transfers and footprint increase proportionally to $b$ whereas filter transfers and footprint remain unchanged because the entire minibatch uses the same chip-resident filters.

Accordingly, Eqn. (2) is modified to Eqn. (6).

\[
\text{OP}[i, j].X = b \times (|L_i| + |L_j|)
\]  

Complexity: The DP algorithm is used to optimize partitions offline (like compiler optimizations).

The algorithm is of asymptotic complexity $O(n^3)$ as there is potentially $O(n)$ work to find the optimal partition point for up to $O(n^2)$ spans in the OP table. In practice, the algorithm’s runtime is less than a second on a laptop, even for the largest networks we consider (ResNet-152). Given that an optimal solution can be computed efficiently, exploring heuristics for the problem is probably not warranted.

### E. Staggered Asynchronous Pipelining (STAP)

Occam captures the enormous inter-image filter reuse by placing each partition – its filters and dependence closure – in a separate chip (e.g., a GPU, TPU, or FPGA). The partitions form a multi-chip asynchronous pipeline both to capture full inter-image reuse and to achieve high throughput (see Figure 5).

The input images pass through the pipeline requiring off-chip access only for each partition’s (pipeline stage’s) input and output feature maps but not the filters (i.e., full cross-image reuse). In contrast, the input-stationary approach [7] refetches the filters for every input image (e.g., TPU).

In each stage, the earlier output map cells are written (or communicated) while the later cells are produced, so that data transfers are hidden under the producer stage’s heavy computation except for a small initial part (Section V-B1). While Occam’s pipeline achieves optimal transfers, other techniques [13], [25] employ ad hoc partitions.

Because Occam’s partitions may result in an unbalanced pipeline, the throughput is limited by the bottleneck stage. However, the latency is unaffected due to asynchronous pipelining if the job arrival rate is under the bottleneck rate (asynchronous stages do not wait for clock edges as do synchronous stages). For example, in an unbalanced, 4-stage Occam pipeline with 15-35-40-10 latency-units per stage, the latency is 100 units and the throughput is 1/40 units$^{-1}$.

The throughput can be increased by replicating the bottleneck stages. In our example, stages 2 and 3 are each replicated for a throughput of one inference per 20 units (Figure 5). These stages use the $i^{th}$ replica for the $i^{th}$ input mini-batch (i.e., parallelize across input mini-batches in a staggered manner and not within each mini-batch). Importantly, STAP achieves better throughput without changing Occam’s optimal tiles.

We consider other forms of parallelism, typically used in training. Model parallelism splits one or more [21], [23], [38] layers into multiple chips and must (1) copy the input to each chip and (2) merge the chips’ results for the next layer. These overheads are worthwhile to reduce filter update traffic in training, but not in inference where filters are not updated and data parallelism achieves the same effect without the overheads. Both Layer-wise parallelism [21] and HyPar [38] choose between model and data parallelisms for each layer, but model parallelism is not relevant for inference. Data parallelism is orthogonal to STAP which achieves higher throughput. For lower latency per image, each mini-batch can exploit data parallelism by replicating the entire pipeline without affecting Occam’s transfer optimality. (e.g., Figure 5). Each replica would work on half the mini-batch. Thus, data parallelism does not change Occam’s off-chip transfer optimality.

Finally, GPipe [19] exploits pipelined parallelism for training. Gpipe uses heuristic-based partitioning (i.e., not optimal, like Occam) and targets minimizing the training pipeline loop from forward pass to back propagation – a problem that is not relevant to Occam.
We use two implementations – a software-based and an FPGA-based – to evaluate Occam.

Software implementation: We implement Occam in CUDA which is used prevalently to implement CNNs. Because Occam requires changes to the CUDA kernels of CNN implementations whereas commercial CUDNN frameworks are not open source, we choose Convnet [24], an open-source framework. Like the latest CNNs, we use 8-bit integers (INT8) which both reduces the data volume and enhances the compute parallelism compared to 32- or 16-bit floating point data.

We implement our DP algorithm as a standalone JavaScript application that takes as input the network parameters and produces the optimal partitions and tile dimensions. We then feed these outputs to Convnet.

Choice of Simulation: While our CUDA implementation can run on a real GPU, Nvidia GPUs exhibit undocumented cache behavior that makes it hard to exploit reuse. For example, our tests revealed that both prefetch (up to 256 KB but not more) and early eviction (e.g., data read once but not written) is evicted before the second touch within the same kernel and even when the footprint fits in the cache) make capturing reuse all but impossible (also observed in other studies [31]). More importantly, the hardware offers no mechanisms to disable these behaviors when they hurt performance. Therefore, we instead use a simulator (GPGPU-sim) where the cache behaves as expected. Our FPGA implementation does not have these problems (Section V-C).

Simulated system: Our goal is to show that Occam improves performance over the best current system. Such a system uses “minibatches” to perform batched inference on an accelerator like Google’s TPU or the latest GPUs. We consider an Nvidia Volta-like accelerator with 140K multiply-accumulate units, 18-MB on-chip cache, and 800-GB/s memory bandwidth processing 32-image minibatches.

We consider such an accelerator with 32K multiply-accumulate units, 24-MB on-chip cache, and 180-GB/s memory bandwidth processing 32-image minibatches. These resources are shared across a minibatch of 32 images is shown in Figure 6. However, simulation of entire minibatches would be impractically slow.

For practical simulation times, we carefully scale the simulated GPU to match a slice of the above system that performs a single inference out of the 32-image minibatch. This scaling reduces the compute bandwidth by a factor of 32 because the work is proportional to the number of inferences. Further, because the simulated GPU incurs instruction overheads that an accelerator does not, the compute bandwidth is increased to 15K multiply-accumulate units. (For example, ResNet requires around 200 multiply-accumulate operations per memory byte. But a GPU requires around 3000 instructions per byte.)

For cache sizes and memory bandwidth, the scaling has to ensure that (1) the partition’s filters are chip-resident and (2) the filters are shared, in cache capacity and memory bandwidth, across all 32 images in the minibatch. Accordingly, we scale the cache to hold one image’s feature map data and the full filter data. Because this number varies for each partition, we use a calibration based on AlexNet which yields a cache size of 3 MB. We validated our scaling methodology by simulating 1, 2, and 4 slices with appropriate scaling and verifying performance within 3% of one another. We use a similar calibration for memory bandwidth reducing it by a factor of 6 (to around 133 GB/s). Finally, we vary the cache size to show that Occam works for other cache sizes. The simulated GPU’s parameters are shown in Table I.

While our on-chip residence requires multiple chips (STAP in Section III-E), we simulate a single GPU to simplify our implementation. To emulate chip-resident filters in our one-GPU simulations, we pre-touch the filters for each partition (in Occam or Layer Fusion) before the partition executes.

Schemes: We implement three schemes; a layer-by-layer base case, Occam, and Layer Fusion. The filters of any single layer fits in the cache in the base case, which, like Eyeriss [7], captures all reuses, except cross-layer, even without tiling. We compare to Layer Fusion which includes cross-layer reuse (due to partitioning and tiling). As such, Layer Fusion subsumes other techniques that have partitioning alone (e.g., Brainwave [13]). Occam’s chip-resident approach uses multiple chips for a given network. To ensure an equal-cost comparison, our base case uses the same number of chips as Occam for throughput via replication. Layer Fusion’s implementation is similar to Occam’s, except with different tile shapes and sizes. Layer Fusion’s exhaustive search for partitions is infeasible for large networks (e.g., 2^34 choices in ResNet-34). As such, we use Occam’s optimal partitions for Layer Fusion and choose the largest square tile whose dependence closure for a given partition would fit in the cache (a different tile size for each partition). Because the tiles are sub-optimal even though the partitions are optimal, Layer Fusion does not capture full reuse. Recall from Section III-C that Layer Fusion employs recomputation for the evicted parts of the dependence closure. By using Occam’s partitions, Layer Fusion also uses the same number of chips. We verified the functional correctness of these schemes by comparing against unmodified Convnet.

Benchmarks: Table II shows the networks used as benchmarks. We repeat each run thrice to capture any statistical variations (which are little to none). Table III also lists the partitions (same for Layer Fusion and Occam) and the tile sizes for each scheme. We run some training runs to generate each network’s filters. Because we are not interested in accuracy (studied elsewhere), we do light training to save time. We use the input images provided with Convnet for all our runs. We simulate full network execution except the fully-connected layers.
TABLE II
BENCHMARK CHARACTERISTICS

| Network | Layers | Partitions | Occam \((\text{TileDim} \times \text{Rowwidth})\) | Layer Fusion \((\text{TileDim} \times \text{TileDim})\) |
|---------|--------|------------|---------------------------------|---------------------------------|
| AlexNet | 8      | 0,8        | \((0.8,2)\)                      | \((0.8,3)\)                      |
| VGGNet  | 19     | 0.6,11,12,14,15,16,18 | \((0.6,6),(0.11,1),(0.12,14.6),(0.16,18.7)\) | \((0.6,20),(0.11,5),(0.12,14.8),(0.16,18.7)\) |
| ZFNet   | 8      | 0.5,8      | \((0.5,3),(5,8.6)\)               | \((0.5,13),(5,8.6)\)             |
| ResNet-18 | 18 | 0.12,15,16,17,18 | \((0.12,2),(12,15.7)\)            | \((0.12,4),(12,15.7)\)           |
| ResNet-34 | 34 | 0.15,21,26,29,30,31,32,33,34 | \((0.15,3),(15,21.2),(21,26.2),(26,29.7)\) | \((0.15,7),(15,21.5),(21,26.5),(26,29.7)\) |
| ResNet-50 | 50 | 0.21,30,37,42,43,45,46,48,49,50 | \((0.21,2),(21,30.2),(30,37.2),(37,42.7)\) | \((0.21,9),(21,30.5),(30,37.5),(37,42.7)\) |
| ResNet-101 | 101 | 0.21,37,45,52,60,62,75,82,90,93,94,96,97,99,100,101 | \((0.21,1),(21,30.1),(30,37.1),(37,42.5)\) | \((0.21,9),(21,30.5),(30,37.5),(37,45.5)\) |
| ResNet-152 | 152 | 0.21,36,43,51,58,66,77,81,88,96,103,111,118,126,133,141,144,145,147,148,150,151,152 | \((0.21,1),(21,36.4),(36,43.2),(43,51.2)\) | \((0.21,9),(21,36.8),(36,43.5),(43,51.5)\) |

TABLE III
Normalized LLC Miss and Instruction Counts

| Network | Miss (Miss.) | Miss (Model-predict) | Norm. Insts. |
|---------|--------------|----------------------|--------------|
|         | (Base = 1)   | (Base = 1)           | (Base = 1)   |
| Alex    | 0.05         | 0.10                 | 1.05         |
| VGG     | 0.16         | 0.10                 | 1.05         |
| ZF      | 0.07         | 0.07                 | 1.05         |
| Res-18  | 0.03         | 0.06                 | 1.05         |
| Res-34  | 0.04         | 0.06                 | 1.04         |
| Res-50  | 0.03         | 0.05                 | 1.03         |
| Res-101 | 0.03         | 0.04                 | 1.04         |
| Mean    | 0.05         | 0.06                 | 1.04         |

V. RESULTS

We present three sets of results: analytical, simulation, and FPGA. The analytical results show Occam’s optimal tile and partitions for the benchmark networks and the traffic savings as tracked by our algorithm (Section III-D). The simulation results compare the execution times and energy for Occam and Layer Fusion. The FPGA results compare performance for Occam and the base case.

A. Analytical results

In Table II, we present the optimal partitions and tile dimensions for our networks for 3-MB on-chip memory. While the tile dimensions for Occam and Layer Fusion are different, we use Occam’s partitions for Layer Fusion (Section IV). The partitions are shown using the start layer for each (e.g., AlexNet uses a single partitions from layers 0 through 8). For each partition, we show the corresponding tile sizes for both Layer Fusion and Occam. The tile sizes are shown as triplets of the form \((pBegin, pEnd, pTileDimension)\) where \(pBegin\) and \(pEnd\) are the layers at the beginning and the end of the partition. Layer Fusion’s tiles are square-shaped \((TileDim \times TileDim)\). In Occam, the tile dimension corresponds to the number of full rows \((TileDim \times RowWidth)\). For a realistic capacity of 3 MB, Occam is able to achieve many multi-layer partitions which capture inter-layer reuse.

Recall that each partition’s filters reside on-chip for all the schemes. Our algorithm calculates the capacity for each partition’s filters and dependence closure. Figure 7 shows this capacity split for ResNet152. For all of our networks, most of the on-chip capacity goes to the filters and a small fraction to the dependence closures. This result highlights the importance of our sufficient condition (our second contribution). The large capacity for the filters saves significant off-chip traffic due to massive cross-image filter reuse (our fourth contribution).
B. Simulation Results

1) Performance:: Figure 8 shows the speedup (Y-axis) for Occam and Layer Fusion over the baseline for various CNNs (X-axis). In addition to the individual networks, Figure 8 also shows the geometric mean speedup across all networks (rightmost bars). Occam uniformly outperforms the baseline with a mean speedup of 2.06x over all networks. The speedups are higher for the larger, more recent networks such as the ResNets. These speedups are a direct result of the large reduction in the miss counts achieved by Occam (21x on average) while avoiding instruction bloat (measured miss counts normalized to the measured baseline’s in Table III). This miss reduction is due to our necessary condition which leads to our specific tile shape and our dynamic programming algorithm which minimizes off-chip traffic (our first and third contributions).

Table III also shows that our model-predicted miss counts (normalized to the measured baseline’s) closely match those seen in simulation measurements. The only exception is VGNNet where there are a few individual layers that are too large to fit in the cache. Recall that Occam uses a lower-bound estimate for such cases.

Layer Fusion also achieves speedups, 1.52x on average, due to lower traffic. However, its speedups are lower than Occam’s due to its sub-optimal tiles which induce high recomputation cost. The recomputation cost is quantified in the normalized instruction count shown in Table III. The three networks where Layer Fusion lags the most behind Occam (AlexNet, ResNet18, and ResNet34) are indeed the three networks with the highest relative instruction overhead. Zfnet is a special case where the entire output and its dependence closure fits in the cache for each partition. In this case, Occam and Layer-fusion are effectively equivalent. Despite its sub-optimal tiles, Layer Fusion seem similar to Occam in miss counts because Layer Fusion recomputes instead of incurring extra misses.

Finally, Occam’s latency penalty for the initial inter-chip transfer has minimal impact on performance (Section III-E). The typical-case PCIe latency of 30µs per partition (PCIe latency varies from 10µs to 50µs [42]) results in slightly reducing the average 2.06x speedup to approximately 2.01x. (Subsequent transfers are hidden under computation due to pipelining.)

We discuss next the energy penalty of inter-chip communication.

2) Energy:: We did not use GPUWattch [28] due to its several quirks which lead to evidently incorrect results. For example, as part of minimizing the mean-square error with its benchmarks, GPUWattch assigns large scaling factors without any physical rationale (e.g., memory write energy scaled down by 10^4). These factors leads to obviously incorrect results when simulating CNNs (e.g., memory system energy is approximately 0.25% of total energy). Instead, we use TPU’s compute energy of 0.43 pJ/op [22] and GDDR5 DRAM energy of 6pJ/bit or 48 pJ/B [32] (roughly 100x more expensive than compute [11]).

Figure 9 shows the energy breakdown into compute, memory, and chip-to-chip PCIe components for the baseline, Occam, and Layer Fusion. The PCIe component is not applicable to the baseline which is not chip-resident and runs one network entirely on one chip; for equal cost, the baseline uses the same number of chips as Occam for parallelism (Section IV). For an equal-cost comparison, we assume chip residence even for Layer Fusion which then incurs PCIe energy like Occam (Section IV). In the baseline, compute and memory energy are split roughly on average as 65:35. Occam’s compute energy is slightly more than the baseline’s as shown by the instruction counts (Table III). Occam drastically cuts memory transfers (21x on average, in Table III) but incurs the extra energy of chip-to-chip transfers at partition boundaries. The net effect of these factors is 33% average reduction in energy because the energy cost/bit for DRAM and PCie are similar (6pJ/bit [32], [42]). Finally, Layer Fusion’s memory energy saving due to fewer transfers (Table III) are offset by its significant recomputation overhead induced by its sub-optimal tiles, resulting in a net energy saving of 12% on average.

As we increase the cache size from 3 MB to 6 MB, Occam’s speedups improve (not shown).

C. FPGA Results

We use a Terasic DE2-150 FPGA development board with an Intel/Altera Cyclone IV family FPGA. The FPGA has approximately 150K logic elements, 820 KB of on-chip RAM and over 300 18-bit fixed-point multipliers running at 50 MHz. The FPGA is interfaced to an external SDRAM which offers...
We use Intel’s Quartus Prime (v15.0) with Qsys system builder with each partition’s filters to capture chip residency with a soft-processor core (Nios II). Our implementation uses vector product to produce one output cell. Our implementation in higher speedups, 5.1x on average, with the FPGA than with memory traffic reduction, 21x on average (Table IV), results in pressure on memory. Consequently, Occam’s considerable compute-efficient than a GPGPU, the baseline puts more pressure on memory. While CNNs can avoid memory latency problems via prefetching and multithreading, memory bandwidth is a problem due to the large data. While there is enormous data reuse, previous work captures only some of this reuse. Full reuse implies that the initial input image and filters are read once from and the final output is written once to off-chip without spilling the intermediate layers’ data. We proposed Occam to capture full reuse via four contributions. First, we identified the necessary and sufficient condition to capture full reuse using dependence closure. Second, we proposed reuse optimizations [3], [7]. We have extensively covered Layer Fusion, the work closest to Occam.

Occam’s key contribution is optimal tiling and network partitioning. Pipelining of CNN pipelines is widespread [13], [25]; our contribution is finding the pipeline partitions that optimize off-chip transfers. Tiling [9], [20], [26], [39], [40] is a well-explored area of research. Occam’s optimal tile shape targets convolutional reuse. Diamond Tiling [4] addresses tile choices in stencil computations that force pipelined start-up and induce load imbalance. Diamond-shaped tiles address this problem. Time tiling [5] enables tiling of stencil computations on periodic domains. While conventional tiling typically holds only the parents, Layer Fusion and Occam perform cross-layer tiling which holds some or all the ancestors. PolyMage [33] and Halide [35] explore cross-stage tiling for image-processing pipeline stages and use heuristics to partition the pipelines. In contrast, Occam employs DP to find the optimal tiles.

We covered pipelining work related to STAP in Section III-E.

VII. CONCLUSION

This paper targeted improving the latency of CNN inference. While CNNs can avoid memory latency problems via prefetching and multithreading, memory bandwidth is a problem due to the large data. While there is enormous data reuse, previous work captures only some of this reuse. Full reuse implies that the initial input image and filters are read once from and the final output is written once to off-chip without spilling the intermediate layers’ data. We proposed Occam to capture full reuse via four contributions. First, we identified the necessary and sufficient condition to capture full reuse using dependence closure. Second, we proposed reuse optimizations [3], [7]. We have extensively covered Layer Fusion, the work closest to Occam.

There is a plethora of work on CNNs in machine learning (ML) research [43]. While exciting innovations in ML continue to improve CNN accuracy and efficiency, our focus is efficient execution of CNNs. Section I covers past work on CNN architectures, such as compute optimizations [1], [2], [14], [22], [24], [29], [37], memory optimizations [8], [12], [15], [30], [34], and reuse optimizations [3], [7]. We have extensively covered Layer Fusion, the work closest to Occam.

Occam’s key contribution is optimal tiling and network partitioning. Pipelining of CNN pipelines is widespread [13], [25]; our contribution is finding the pipeline partitions that optimize off-chip transfers. Tiling [9], [20], [26], [39], [40] is a well-explored area of research. Occam’s optimal tile shape targets convolutional reuse. Diamond Tiling [4] addresses tile choices in stencil computations that force pipelined start-up and induce load imbalance. Diamond-shaped tiles address this problem. Time tiling [5] enables tiling of stencil computations on periodic domains. While conventional tiling typically holds only the parents, Layer Fusion and Occam perform cross-layer tiling which holds some or all the ancestors. PolyMage [33] and Halide [35] explore cross-stage tiling for image-processing pipeline stages and use heuristics to partition the pipelines. In contrast, Occam employs DP to find the optimal tiles.

We covered pipelining work related to STAP in Section III-E.

VI. RELATED WORK

for three of our networks. Because the baseline FPGA implementation avoids instruction overheads and is more compute-efficient than a GPGPU, the baseline puts more pressure on memory. Consequently, Occam’s considerable memory traffic reduction, 21x on average (Table IV), results in higher speedups, 5.1x on average, with the FPGA than with a GPGPU (Figure 8).
