Abstract - Methods of extraction of interface trap level density in graphene field-effect devices from the capacitance-voltage measurements are described and discussed. Interrelation with the graphene Fermi velocity extraction is shown. Similarities and differences in interface trap extraction procedure in graphene and silicon field-effect structures are briefly discussed.

I. INTRODUCTION

A role of fast interface traps in operation of graphene gated field-effect devices, which can vary in a wide range of values depending on purity and quality of the interface, needs to be understood [1]. This leads to importance of experimental determination of the interface trap energy spectra based particularly on capacitance measurements. The objective of this report is to develop extraction methods of the interface trap parameters as adapted to graphene devices based on experimental capacitance data.

II. NEAR-INTERFACIAL OXIDE TRAPS

Near-interfacial traps (defects) are located exactly at the interface or in the oxide typically within 1-3 nm from the interface. These defects can have generally different charge states and capable to be recharged by exchanging carriers (electrons and holes) with the device channels. Due to the exchange possibility the near-interfacial traps sense the Fermi level position in graphene (see Fig.1).

Each gate voltage corresponds to the respective position of the Fermi level at the interface with own “equilibrium” defect level filling and quasi-equilibrium defect charge density $Q_d(\varepsilon)$. The traps rapidly exchanging the carriers with the graphene are often referred as to the interface traps ($N_d$) [2, 3]. Interface trap capacitance per unit area $C_G$ and interface trap level density $D_t(\varepsilon)$ is defined in a following way

$$C_G(\varepsilon_F) = \frac{d}{d\varepsilon_F}(-Q_d(\varepsilon_F)) = e^2D_t(\varepsilon_F).$$

III. GENERAL BACKGROUND FOR CAPACITANCE METHODS

Influence of interface traps on C-V curves in field-effect devices is two-fold. Firstly, the total gate capacitance at a given Fermi energy in graphene increases with the interface trap capacitance. Secondly, the gate voltage dependence on the Fermi energy $V_{G(\epsilon_F)}$ varies with change of $C_G$ that leads to the stretch out of the C-V curves along the gate voltage axis. Thereby all information about the energy level distribution of the interface trap density contains in the $V_{G(\epsilon_F)}$.

Taking derivative of the Eq. 1 with respect to the Fermi energy we have

$$\frac{dV_G}{d\varepsilon_F} = e^2\int_0^\varepsilon F \frac{C_G(\varepsilon_F) - C_G(\varepsilon_F) + C_G(\varepsilon_F)}{C_G},$$

This yields immediately the differential interface trap density as function of Fermi energy

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Capacitance-voltage measurements provide information about the Fermi energy as function of the gate voltage. Specifically, the gate capacitance at a given frequency is defined as

$$C_G = \epsilon \frac{\partial N}{\partial V_G} = \left( \frac{1}{C_{\infty}} + \frac{1}{C_G + C_\infty} \right)^{-1},$$

and correspondingly one gets

$$C_G (\epsilon) = C_G \left( \frac{dV_G}{d\epsilon} \right) - C_G (\epsilon) = \left( \frac{1}{C_G} - \frac{1}{C_{\infty}} \right)^{-1} - C_G (\epsilon)$$

Notice that $C_G$ decreases with the gate small-signal frequency increase since the $C_\infty$ logarithmically diminishes with the a.c. frequency increase due to carrier exchange rate suppression. At the same time the large-signal sweeping of the gate voltage is typically relatively slow and corresponds to maximum low-frequency $C_G$ and $V_G (\epsilon_F)$ at low-frequency $C_G^{(LP)}$. Combining Eq.2 and 4 one gets

$$\frac{d\epsilon_F}{dV_G} = \frac{1 - C_G^{(LP)}}{C_G}$$

Using Eq.6 the Fermi energy at any applied gate voltage could be determined from integration of low-frequency C-V curves (Berglund low-frequency method [2,3])

$$\epsilon_F (V_G) = \epsilon \int_{V_G}^{V_{V_F}} \left( \frac{1}{C_G^{(LP)}} \right) dV_G$$

where the integration constant is chosen to be zero since the charge neutrality point at the capacitance minimum voltage $V_{NP}$ corresponds to zero Fermi energy.

**IV. NUMERICAL EXAMPLE**

Numerical analysis of the experimental C-V curve (taken from [5]) with the Eq.7 enables obtaining of dependencies $V_G (\epsilon_F)$ and $\frac{dV_G}{d\epsilon}$ (see Fig.4) containing theoretically all information about interface trap spectrum.

![Figure 4](image4.png)

**Fig.4. Dependencies $V_G (\epsilon_F)$ (in Volts) and $\frac{dV_G}{d\epsilon}$ (dimensionless) extracted numerically from the C-V data [5] depicted in Fig.2.**

Fig.5 shows comparison of the theoretically calculated dependence of quantum capacitance $C_Q (\epsilon_F)$ and experimentally extracted sum of the quantum and the interface trap capacitances

$$C_Q (\epsilon_F) = C_Q (\epsilon_F) \left( \frac{1}{C_G} - \frac{1}{C_{\infty}} \right)^{-1} = C_Q + C_G$$

**Fig.5. Quantum capacitance theoretical dependences $C_Q (\epsilon_F)$ calculated with $v_0 = 1.3 \times 10^8$ cm/s (1, green line), $v_0 = 1.0 \times 10^8$ cm/s (2, dashed line) and the experimental curve $C_G (\epsilon_F)$ obtained with Eq.7 (3, [6], and 4 [5], red lines ).**

As has been shown in [7] the separation results for $C_Q$ and $C_G$ are strongly dependent on a priori value of $v_0$. As can be seen in Fig.4 a model-independently extracted curve $C_G (\epsilon_F)$ imposes limitation on numerical value of $v_0$. In particular the quantum capacitance calculated as
with \( v_0 = 1.0 \times 10^8 \text{ cm/s} \) in an unphysical way exceeds \((C_Q + \Delta C_{it})\exp\) extracted from the experiments [5,6]. A value \( v_0 = 1.3 \times 10^8 \text{ cm/s} \) obtained in Ref. [7] seems to be more appropriate for self-consistent description of the experimental C-V data. Unfortunately as well as for the Si-MOSFET case the methods of absolute differential spectra extraction are very sensitive to experimental errors and uncertainties in the parameters used, particularly, the graphene Fermi velocity \( v_0 \). For these reason the extraction of difference \( \delta D_n(\epsilon) \), for example, before and after electric or irradiation stress could give more reliable results.

V. COMPARING SI-MOSFET AND GFET CASES

We will compare in this section electrostatics of the silicon MOS and graphene FETs to reveal their main similarities and differences. The basic electrostatic relation is often written as

\[
e(V_G - V_{FB}) = \frac{\varepsilon_0^2}{C_m} \int_{\mu(V)} D_s(\epsilon) d\epsilon + \frac{\varepsilon^2}{C_m} \left( n_s + N_s x_D(\phi_F) \right)
\]

where \( x_D \) is the depletion layer width. Using the flatband voltage and the gate-substrate contact potential definitions [3] one can obtain

\[
eV_G = e\left( W_{gate} - \chi_S \right) + \kappa + \frac{\varepsilon^2}{C_m} \left( n_s + N_s x_S \right) - \frac{Q(\zeta)}{C_m}
\]

where \( W_{gate} \) and \( \chi_S \) are the gate workfunction and the silicon electron affinity, \( \mu = E_i / 2 + \epsilon_F = \epsilon_F - \zeta \) is independent on perpendicular coordinate the electrochemical potential in the Si substrate (see Fig.6), \( \zeta = \epsilon_F - E_i / 2 - \epsilon_F \) is the chemical potential at the interface which is negative for non-degenerate channel.

As in the case of graphene, we can equally use concepts of either electric or chemical potential for description of channel charge density since due to zero current along the \( x \) axes they are the same up to a constant \( \delta \phi_S = \delta \zeta \) at the same position. This means that the electrostatics of silicon and graphene can be considered in some extent in a unified manner.

The results for graphene could be reproduced from Eq.11 formally setting for zero-gap material \( E_G / 2 + \phi_F = 0 \) and \( N_s x_D = 0 \). Using Eq.11 we have

\[
e \frac{dV_G}{d\zeta} = 1 + \frac{C_{inv} + C_D + C_{it}}{C_m}
\]

where \( C_D \) is depletion layer capacitance, \( C_{inv} = e^2 d n_s / d \zeta \) is the inversion layer capacitance which is a full analogue of the quantum capacitance and for non-degenerate channel may be estimated as [8]

\[
C_{inv} \approx \frac{e^2 n_s}{2kT} \left( 1 + \frac{N_s x_S}{n_s + N_s x_D} \right).
\]

Due to exponential dependence of \( n_S \) on potential in the depletion and weak inversion regions the \( C_{inv} \) plays rather minor role in the silicon FETs since it is very low in subthreshold operation mode \((C_{inv} \ll C_D, C_{it})\) and extremely high in above threshold strong inversion regime \((C_{inv} \gg C_m)\). In the former case the quantum capacitance in MOSFETs is masked by the parasitic interface trap and depletion layer capacitances connected in parallel in the equivalent electric circuit, and in the latter case it is insignificant due to the series connection with the gate insulator having typically lesser capacitances for high carrier densities in inversion layers. In fact the inversion layer capacitance in MOSFETs is only important in the very narrow region of weak inversion where it is comparable with the oxide and depletion layer capacitances. Therefore, from the electrostatic point of view the difference between Si-MOSFETs and GFETs is that the full silicon substrate capacitance \( C_S = C_{inv} + C_D \) should be replaced by the graphene quantum capacitance \( C_Q \).

The depletion layer is absent in GFETs and the interface traps capacitance is the only in parallel connection with the quantum capacitance in the equivalent electric circuit (see Fig.7).

![Fig. 6. Energy band diagram of Si-MOSFET (\( \phi_F = (k_B T / e) \ln N_i / n_i \), \( n_i \) is the intrinsic concentration in the Si).](image)

![Fig. 7. Equivalent circuit of gated graphene (a) and Si-MOSFET (b).](image)
That is why the interface trap extraction methods for graphene and silicon FETs are rather similar up to a substitution \( C_Q \rightarrow C_D \). Both methods may be sensitive to parameters of \( C_D \) (concentration and profile of dopants) in the silicon or \( C_Q \) (the Fermi velocity \( v_F \)) in graphene, which possess some uncertainties.

Considerable difference between Eq.1 and Eq.11 is that in contrast to the silicon substrate the carriers in graphene almost always are degenerate excepting the vicinity of charge neutrality point. As an advantage of graphene case may be considered the presence of the distinct and distinguishable reference point with the zero Fermi energy simplifying extraction procedure.

VI. INTERFACE TRAP SPECTRUM AND TRANSCONDUCTANCE

The channel capacitance can be defined (see Ref.[4]) as follows

\[
C_{\text{CH}} = \frac{e\partial n}{\partial V_G} = \frac{C_Q}{1 + \frac{C_Q + C_m}{C_m}}
\]  

(14)

The gate and the channel capacitances are interrelated in field-effect structures through the relation

\[
\frac{C_Q}{C_{\text{CH}}} = 1 + \frac{C_m}{C_Q}
\]  

(15)

and can be considered to be coincided only for zero interface trap density when \( C_m = 0 \). The general Eq.14 for the channel capacitance has a following property

\[
C_{\text{CH}}(C_m + \Delta C_m) = \frac{C_{\text{CH}}(C_m)}{1 + \frac{C_m}{C_Q}}
\]  

(16)

On the other hand, the channel capacitance immediately determines small-signal transconductance. Actually, assuming carrier mobility \( \mu \) in GFET to be gate voltage independent the small-signal transconductance in the linear mode reads

\[
g_m = \left( \frac{\partial I_D}{\partial V_G} \right)_{V_D} = \frac{W}{L} \mu \frac{C_{\text{CH}}}{C_m} V_D.
\]  

(17)

Hence, any alteration of the low-frequency interface trap capacitance \( C_m \rightarrow C_m + \Delta C_m \) leads to a renormalization of the transconductance (or, the same, for field-effect mobility \( \mu_{FE} = \mu C_{\text{CH}} / C_m \))

\[
g_m(C_m + \Delta C_m) = \frac{g_m(C_m)}{1 + \frac{\Delta C_m}{C_Q + C_m + C_m}}.
\]  

(18)

As the interface trap capacitance increases due to, for example, ionizing irradiation or electric stress, the gate capacitance (Eq.4) increases but the transconductance and the channel capacitance (Eq.14) decreases. Interface trap buildup always degrades the transconductance in all types of field-effect devices. Generally the channel capacitance is a more appropriate concept for I-V characteristic description whereas the gate capacitance is a directly measured quantity in the C-V measurements. Both approaches are equivalent and should yield the same results at least at small drain biases. The channel conductance immediately affects also the logarithmic swing (in V per current decade) which characterizes the \( I_{ON}/I_{OFF} \) ratio and equals numerically to the gate voltage alteration needed for current change by an order

\[
S = \left( \frac{\ln I_D}{\ln I_D} \right) = \ln 10 \left( \frac{n_s}{n_s} \right) = \ln 10 \frac{n_s}{C_{\text{CH}}}.
\]  

(19)

Using Eq.14 this formula can be written down in a form more familiar from silicon MOSFET theory

\[
S = \ln 10 \left( \frac{e_n}{C_Q} \right) \left( 1 + \frac{C_m + C_Q}{C_m} \right) = \ln 10 \left( \frac{\varepsilon_D}{e} \right) \left( 1 + \frac{C_m + C_Q}{C_m} \right)
\]  

(20)

For subthreshold region of the Si-MOSFETs with non-degenerate channels we have \( \varepsilon_D = kT \) and \( C_Q \) should replaced by \( C_D \). Graphene FETs do not have subthreshold region; the diffusion energy \( \varepsilon_D = e_n^2 / C_Q \approx e_F / 2 \) and unlike the silicon FET case the logarithmic swing in GFETs is a function of the gate voltage. Eq.20 shows that interface traps enhance logarithmic swing \( S \) and make worse the \( I_{ON}/I_{OFF} \) ratio and modulation of channel conductance.

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