INTRODUCTION

Energy storage systems (ESS) have been continuously growing in the last years, reaching 15.3 GWh of installed storage capacity in 2017, excluding pumped hydro. However, it is worth noting that lithium-ion batteries are the main technology used for the new storage capacity installed from 2013, achieving the 88% of the capacity deployed in 2016.

In many applications (e.g., microgrids and electric vehicles), batteries are used to regulate the voltage of a DC-bus to compensate the unbalances between generation and load. The energy exchange between the batteries and the DC-bus is performed by a charging/discharging system, which is composed by a bidirectional DC/DC converter and a control system. The control system can be divided into two parts. The first one is a high level controller, sometimes named energy management system, which monitors the battery state of charge and manages the discharge period. The second one is a low level controller, which controls the power flow between the battery and the DC-bus. This controller is usually implemented by a digital signal processor (DSP) or a microcontroller (MCU).

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Abstract

Regulation of DC-bus voltages is important for the stable operation of different applications, like microgrids and electric vehicles, and it is usually performed by charging/discharging (C/D) batteries. Such C/D system is formed by a power converter and a control system, and it is aimed at guaranteeing the system stability and extending the battery life. To extend the battery life, it is important to reduce the battery current ripples, which is usually performed with interleaved converters and nonlinear controllers; however, most of those controllers do not provide the design procedure nor guarantee the system stability. This paper proposes a nonlinear control strategy to regulate the voltage in a DC-bus by C/D a battery through a two-branch interleaved Boost converter. The proposed control strategy is formed by two sliding mode controllers (SMCs), where the first one regulates the DC-bus voltage by acting on the first converter branch and the second SMC controls the current in the second branch. The reference of the second SMC is generated from the delayed current of the first branch, in order to coordinate the controllers and to reduce the ripples in the battery current. The paper includes a procedure to design the two SMCs as well as simulation and experimental results to validate the proposed solution and to illustrate its performance. The results prove the system stability and its dynamic performance according to the design.

KEYWORDS

battery, charging/discharging, DC-bus voltage, interleaved Boost, sliding mode control

1 | INTRODUCTION

Energy storage systems (ESS) have been continuously growing in the last years, reaching 15.3 GWh of installed storage capacity in 2017, excluding pumped hydro. However, it is worth noting that lithium-ion batteries are the main technology used for the new storage capacity installed from 2013, achieving the 88% of the capacity deployed in 2016.
state-of-charge, as well as other energy sources, to determine the battery operation state. The second part of the control system is a low-level controller that monitors the electrical variables of the power converter, connected to the battery, to regulate the currents and voltages in the charging/discharging process by manipulating the converter duty cycle.

The DC-bus voltage is usually higher than the batteries voltage; hence, a step-up converter (typically a Boost) is used to couple the batteries to the DC-bus. Such a converter is controlled to regulate the DC-bus voltage as a strategy to balance the generators and loads connected to the same bus. Moreover, the charging/discharging systems must also consider the battery life cycle, which is affected by the maximum charging and discharging currents, the depth of discharge, the batteries temperature, the battery current ripples, among others.

Battery current ripples are produced by the converter switching and they generate small charging/discharging processes named subcycles. Those subcycles must be considered in the battery life estimation, since multiple subcycles are equivalent to a complete charging/discharging cycle, which reduces the battery life. Hence, reducing the current ripples in the battery contributes to extend its life.

The reduction of the battery current ripples, produced by the switching of the DC/DC converter, can be performed by using interleaved DC/DC converters. In those converters, there are two or more branches connected in parallel to reduce the current ripples, where each branch is formed by the switching devices and the inductor of the original converter.

In the literature, it is possible to find different charging, discharging and charging/discharging systems based on interleaved converters, which are used for different applications and use linear and nonlinear controllers. The authors in ref. use PI controllers to regulate the DC-bus voltage in a fast charger for electric vehicles (EVs) and a hybrid energy source formed by a fuel cell and a battery bank. Even if linear controllers are simple to implement and design, they cannot guarantee the system dynamic response and stability for all the operating conditions, since those controllers are designed using small-signal models of the system.

A combination of nonlinear controllers for interleaved Boost converters are proposed in ref. In those papers, the authors use cascade controllers, where the inner loop is a sliding mode controller (SMC) of the inductors current, and the outer loop regulates the DC-bus voltage with a controller based on flatness theory. The SMC proposed in ref. uses a switching function formed by a linear combination of the inductor current error and the integral of that value. However, the authors do not analyze the time shift required between the duty cycles of the two converter branches. Similarly, the authors in ref. do not provide information about the implemented SMC, which hinders the viability analysis. Additionally, the outer loop controllers in ref. manipulate the power delivered or absorbed by the ESS, which is translated in a reference for the inner loop (SMC).

The authors in ref. propose complex nonlinear controllers for interleaved Boost converters, based on SMC. The controller proposed in ref. combines a SMC and Lyapunov analysis to generate the converters duty cycles references. Instead, the controller introduced in ref. combines a SMC with a chattering elimination algorithm, where the SMC regulates both the inductor current and the DC-bus voltage at the same time. Finally, the paper proposes a controller for the inductors currents with two modes. One mode is a simple SMC controller that operates when the controlled variable is far from the reference (named transient controller), while the second mode operates when the system is in steady-state and it is formed by four sliding surfaces to create a stable limit cycle.

Some of the nonlinear controllers described before do not provide procedures to calculate the controller parameters or the design procedure is not clearly explained or justified. Other works do not analyze or verify the system stability or assume some dynamic restrictions to the load that may not be realistic in some applications. Moreover, most of the proposed SMCs act on the duty cycle of the converters, which reduces their dynamic response, while others do not explain how to ensure the time shift between the switching signals for variable frequencies.

This paper proposes a SMC for a two-branch interleaved Boost converter, to regulate a DC-bus voltage by charging/discharging a battery. The controller is formed by two SMCs, where the first one is aimed at regulating the DC-bus voltage with a switching function that generates the switching signal for one branch of the converter \( u_1 \). This SMC ensures the stability of the DC-bus in the three operating conditions of the system: charging, discharging, and stand-by (or storage). The condition of the first SMC is that the average inductors currents of the two branches are the same, which is guaranteed by the second SMC proposed in the paper. This SMC controls the inductor current of the second branch \( i_{L2} \), by acting on its switching signal \( u_2 \), and the reference is calculated as a delayed value of \( i_{L1} \) to reduce the battery current ripple. The proposed solution is validated with experimental results, which show the main advantages: First, the SMCs act on \( u_1 \) and \( u_2 \) of the converter and not on the duty cycles, which provides a faster dynamic response; second, the proposed design procedure facilitates its implementation for other applications that requires DC-bus regulation with an ESS (eg, EVs, EVs-to-grid applications, EVs chargers, stand-alone generators with photovoltaic or wind turbine generators, hybrid ESS, active power filters); and third, the implementation is simple and can be performed with low-cost devices.

The rest of the paper is organized as follows: Section 2 presents the structure of the proposed charger/discharger; Section 3 introduces the system modeling; Section 4 describes the proposed control structure; Section 5 reports the...
2 | INTERLEAVED CHARGER/DISCHARGER CIRCUIT

The electrical scheme of the classical charger/discharger is based on a bidirectional Boost DC/DC converter, as shown in Figure 1, where the battery is modeled as a voltage source \( v_b \) and the DC-bus is modeled by a lumped capacitor \( C \) and current source \( i_{dc} \). Such a charger/discharger has been extensively used due to it provides a positive compromise between simplicity and performance.\(^{16,17}\) Moreover, both linear controllers and SMCs have been designed to ensure a stable operation of the DC-bus voltage.\(^{3,4,18}\) In particular, the work reported in ref.\(^{19}\) proposes a SMC based on the battery current \( i_b \) and the DC-bus voltage error, which provides a satisfactory voltage regulation with global stability. The sliding surface \( \Psi_1 = 0 \) of that paper is based on the sliding function reported in (1), which imposes the battery current \( i_b \) (ie, inductor current) to compensate the transients in the DC-bus current \( i_{dc} \). In (1), \( v_R \) is the reference value for the DC-bus voltage \( v_{dc} \), while \( k_p \) and \( k_i \) are parameters calculated to impose a desired settling time and overshoot to the bus voltage.

\[
\Psi_1 = i_b + k_p \cdot (v_R - v_{dc}) + k_i \cdot \int (v_R - v_{dc}) \, dt \quad \Phi = [\Psi = 0] \quad (1)
\]

The main drawback of the classical charger/discharger converter (Figure 1), in terms of battery degradation, is the high-frequency inductor current ripples produced by the converter switching. Those ripples are transferred to the battery, reducing its life cycle, as described in Section 1. This problem is addressed in this paper by adding a second branch to the classical charger/discharger (C-C/D), which produces the interleaved charger/discharger (I-C/D) scheme presented in Figure 2. In that electrical structure, the Boost branches can be controlled to produce complementary current ripples into the inductors currents \( i_{L1} \) and \( i_{L2} \), which reduce the effective current ripple reaching the battery.

As in C-C/D, the I-C/D must provide or absorb the current required or available in the DC-bus, respectively, to regulate \( v_{dc} \). Moreover, the proposed I-C/D considers the same voltage relation between the battery and the DC-bus adopted for the C-C/D, that is, \( v_b < v_{dc} \). Hence, this solution is a suitable improvement for several existing devices,\(^{20,21}\) since the load current is split between the converter branches and it decreases the ohmic losses.

3 | I-C/D OPERATION ANALYSIS AND MODELING APPROACH

The I-C/D circuit is designed to provide ripple cancelation between \( i_{L1} \) and \( i_{L2} \), in which \( i_b = i_{L1} + i_{L2} \), so that the ripple in the battery current \( i_b \) can be reduced in comparison with the C-C/D
The derivatives of $i_{L1}$ and $i_{L2}$, in the scheme of Figure 2, are given in (2) and (3), in which $u_1$ and $u_2$ represent the MOSFET activation signals for the first and second branches, respectively, and $L$ is the inductance in each converter branch. Those equations also put into evidence that the inductors of both branches are designed equal to provide the same ripple magnitude.

$$\frac{d i_{L1}}{dt} = \frac{v_b - v_{dc} \cdot (1 - u_1)}{L} \quad (2)$$

$$\frac{d i_{L2}}{dt} = \frac{v_b - v_{dc} \cdot (1 - u_2)}{L} \quad (3)$$

To avoid overcharge in a single branch, that is, a high stress in the MOSFETs and inductor, the average current in both inductors must be equal, that is, $\langle i_{L1} \rangle = \langle i_{L2} \rangle$. Such a condition requires a closed-loop controller, which is designed using sliding mode theory in this paper. For this purpose, subsection 4.1 proposes a SMC to regulate $i_{L2}$ to ensure the same average current in both inductors.

The differential equation given in (4) describes the DC-bus voltage of Figure 2. However, considering the control approach given by condition $\langle i_{L1} \rangle = \langle i_{L2} \rangle$, the differential equation describing the DC-bus voltage can be rewritten as given in (5), in which $d = 1 - v_b/v_{dc}$ is the duty cycle of the branches reported in ref. 19. From the I-C/D circuit (Figure 2), it is evident that both branches exhibit the same input and output voltages, hence the same duty cycle. Note that (5) is described in terms of $u_1$ because such a variable will be used in subsection 4.2 to regulate the DC-bus voltage; moreover, $u_2$ is not present because such a variable is already used by the SMC that ensures the same average current in both inductors.

$$\frac{dv_{dc}}{dt} = \frac{i_{L1} \cdot (1 - u_1) + i_{L2} \cdot (1 - u_2) - i_{dc}}{C} \quad (4)$$

$$\frac{dv_{dc}}{dt} = \frac{i_{L1} \cdot (1 - u_1) + (i_{L1}) \cdot (1 - d) - i_{dc}}{C} \quad (5)$$

3.1 | Current ripples

The current ripple magnitudes of $i_{L1}$ and $i_{L2}$ (ie, $\Delta i_{L1}$ and $\Delta i_{L2}$) are calculated from (2) and (3), respectively, obtaining (6), where $T_{sw}$ represents the switching period.

$$\Delta i_{L1} = \Delta i_{L2} = \frac{v_b}{L} \cdot d \cdot T_{sw} \quad (6)$$

Similarly, the ripple waveforms of both branches ($\delta i_{L1}$ and $\delta i_{L2}$) are given in (7) and (8), respectively, in which $\Delta T$ represents the time delay between the ripple waveforms of both branches and it is constrained within $[0, T_{sw}]$. If $\Delta T = 0$ or $\Delta T = T_{sw}$, both current ripple waveforms will be in phase and no ripple cancellation occurs, and in fact, the ripple magnitude in the battery current will be doubled with respect to the C-C/D circuit.

$$\delta i_{L1}(t) = \begin{cases} \frac{v_b}{L} \cdot t, & 0 \leq t < d \cdot T_{sw} \\ \frac{v_b}{L} \cdot t + \Delta i_{L1}, & d \cdot T_{sw} \leq t < T_{sw} \end{cases} \quad (7)$$

$$\delta i_{L2}(t) = \delta i_{L1}(t + \Delta T) \quad (8)$$

The ripple waveform in the battery current ($\delta i_b$) is obtained by adding the ripple waveforms of both branches, as reported in (9), and the magnitude of such a current ripple is obtained by (10). Both expressions (9) and (10) depend on $\Delta T$; hence, the battery current ripple can be modified by varying the time shift between $\delta i_{L1}$ and $\delta i_{L2}$. Figure 3 illustrates the time shift concept of the current ripples generated in the two branches of the I-C/D circuit, where $i_{L1}$ and $i_{L2}$ exhibit the same period, average value, and ripple magnitude, but the time shift $\Delta T$ between the current peaks could be modified. The following subsection analyzes the behavior of $\delta i_b(\Delta T)$ to obtain the time shift value that produces the lower battery current ripple.

$$\delta i_b(t, \Delta T) = \delta i_{L1}(t) + \delta i_{L1}(t + \Delta T) \quad (9)$$

$$\Delta i_b(\Delta T) = \max(\delta i_b(t, \Delta T)) - \min(\delta i_b(t, \Delta T)) \quad (10)$$

3.2 | $\Delta T$ design to reduce $\Delta i_b$

This subsection evaluates $\Delta i_b$ for $0 \leq \Delta T \leq T_{sw}$ and different boosting factors (ie, $v_{dc}/v_b$), in order to determine the best value of $\Delta T$ for different operating conditions. Moreover, $\Delta i_b(\Delta T)$ is calculated by using (10) and it is compared with the magnitude of the battery current ripple produced by the C-C/D ($\Delta i_{bc}$).

The relation $\Delta i_b(\Delta T)/\Delta i_{bc}$ for $v_{dc}/v_b = 3$ and $0 \leq \Delta T \leq T_{sw}$ is illustrated in Figure 4. Such a figure shows that the minimum value of $\Delta i_b$ is obtained for $\Delta T = T_{sw}/2$ and it corresponds to half of the battery current ripple magnitude.
obtained with the C-C/D ($\Delta i_{b,c}$). Furthermore, Figure 4 shows that $\Delta i_b$ linearly increases for $T_{sw}/2 < \Delta T \leq T_{sw}$ and decreases for $0 \leq \Delta T < T_{sw}/2$; then, the maximum value of $\Delta i_b$ is $2 \cdot \Delta i_{b,c}$ for $\Delta T = 0$ and $\Delta T = T_{sw}$.

The analysis introduced in Figure 4 is repeated for different boosting factors, going from 1.33 to 4, to identify the values of $\Delta T$ that minimizes $\Delta i_b$ for each boosting factor. The ratio of the minimum $\Delta i_b$ (ie, $\min(\Delta i_b)$) and $\Delta i_{b,c}$ for different boosting factors is introduced at the top of Figure 5, while the bottom of Figure 5 shows the value of $\Delta T$, as a percentage of $T_{sw} (\Delta T/T_{sw})$, that provides $\min(\Delta i_b)$. From Figure 5, it can be observed that $\Delta T = T_{sw}/2$ minimizes $\Delta i_b$ for all the evaluated boosting factors. Additionally, I-C/D with $\Delta T = T_{sw}/2$ completely eliminates $\Delta i_b$ for $v_{dc}/v_b = 2$, and reduces $\Delta i_b$ by 30% or more, with respect to $\Delta i_{b,c}$, for the others scenarios. Therefore, $\Delta T = T_{sw}/2$ is adopted in this paper.

In the previous section, the need for two controllers was identified in order to ensure the correct operation of the I-C/D system:

- A current sharing controller to ensure the same average current and the same current ripple magnitude in each converter branch.
- A DC-bus voltage controller to ensure stable operation of the DC-bus in any operation mode of the system: charge (negative battery current), discharge (positive battery current) and stand-by (null battery current).

The following subsections deal with the analysis and design of those controllers.
4.1 | Current sharing controller

The main objective of this controller is to ensure the same average value for both inductors currents and, at the same time, to ensure the same current ripple magnitude, which enables to reduce the battery current ripple. To fulfill both conditions, the switching function $\Psi_r$ and sliding surface $\Phi_r$ are defined as shown in (11).

$$\Psi_r = i_{L2} - k_r \cdot i_R, \Phi_r = \{\Psi_r = 0\}$$ (11)

The sliding surface given in (11) will force the inductor current of the second branch ($i_{L2}$) to follow the reference $i_R$. Hence, defining $(k \cdot i_R) = i_{L1} (t + \Delta T)$, with $\Delta T = T_{sw}/2$, will ensure both the minimum current ripple at the battery current and a balanced current sharing among the inductors. To ensure the existence of the sliding mode, it is necessary to fulfill three conditions: transversality, reachability, and equivalent control.

4.1.1 | Transversality condition

This test verifies that the control signal of the second branch ($u_2$) is present into the proposed switching function derivative, which ensures that the controller is able to modify the current trajectory. The mathematical representation of the transversality condition is given in (12) and the derivative of the switching function $\Psi_r$ is obtained from (3), as shown in (13).

$$\frac{d}{du_2} \left( \frac{d\Psi_r}{dt} \right) \neq 0$$ (12)

$$\frac{d\Psi_r}{dt} = \frac{v_b - v_{dc} \cdot (1 - u_2)}{L} - k_r \cdot \frac{di_R}{dt}$$ (13)

Then, evaluating (12) using (13) leads to expression in (14), which verifies the transversality condition of the proposed SMC. Therefore, it is possible to implement a SMC based on the switching function $\Psi_r$ and sliding surface $\Phi_r$ given in (11).

$$\frac{d}{du_2} \left( \frac{d\Psi_r}{dt} \right) = \frac{v_{dc}}{L} > 0$$ (14)

4.1.2 | Reachability conditions

They evaluate the ability of the SMC to converge into the sliding surface. The detail of the mathematical derivation of the reachability conditions is given in ref. In summary, the reachability conditions are:

- When the system operates under the surface ($\Psi_r \rightarrow 0^-$), the switching function derivative must be positive to reach the surface.

- When the system operates above the surface ($\Psi_r \rightarrow 0^+$), the switching function derivative must be negative to reach the surface.

However, the sign of the switching function derivative depends on the sign of the transversality condition. From the analyses given in that work, it is known that a positive transversality condition imposes the following reachability conditions:

$$\lim_{\Psi_r \rightarrow 0^-} \frac{d\Psi_r}{dt} \bigg|_{u_1=1} > 0$$ (15)

$$\lim_{\Psi_r \rightarrow 0^+} \frac{d\Psi_r}{dt} \bigg|_{u_1=0} < 0$$ (16)

Evaluating both (15) and (16), using the expression given (13), inequality (17) is obtained.

$$\frac{v_b - v_{dc}}{L} < k_r \cdot \frac{di_R}{dt} < \frac{v_b}{L}$$ (17)

Then, the optimal current ripple cancelation condition $(k_r \cdot i_R) = i_{L1} (t + \Delta T)$ must be evaluated, which is done by using the implications of expression (2) on $\frac{di_{L1}}{dt}$.

$$\frac{di_{L1}}{dt} = \left\{ \begin{array}{cl} \frac{v_{b} - v_{dc}}{L} & \text{for } u_1 = 0 \\ \frac{v_b}{L} & \text{for } u_1 = 1 \end{array} \right.$$ (18)

Therefore, the conditions $i_R = i_{L1} (t + \Delta T)$ and $k_r < 1$ are necessary to fulfill the inequality given in (17). However, such a theoretical limitation on $k_r$ is fulfilled by a value slightly lower than 1, hence $k_r \rightarrow 1^-$, that is, the closest value to 1 on the left. This definition of $k_r$ will introduce a negligible error on the tracking of $i_{L1}$ obtained with $i_{L2}$, but, at the same time, it will enable to fulfill both reachability conditions in (15) and (16). In conclusion, the following conditions must be imposed on the sliding surface:

$$\left\{ i_R = i_{L1} (t + \Delta T), k_r \rightarrow 1^- \right\}$$ (19)

Finally, in ref. the authors demonstrate that fulfilling transversality and reachability conditions also ensure the equivalent control condition. This means that the duty cycle of the DC/DC converter is not saturated, and also it verifies the existence of the sliding mode.

4.1.3 | Equivalent dynamics

The existence of the sliding mode guarantees that the system trajectory is parallel to the surface and with null steady-state error. The mathematical representation of both conditions is given in (20).
\[
\left\{ \Psi_r = 0, \frac{d\Psi_r}{dt} = 0 \right\}
\]  

(20)

Therefore, by substituting the values imposed in (19), it is granted that \(i_L(t) \approx i_L(t + \Delta T)\) and \(\frac{d i_L(t)}{dt} \approx \frac{d i_L(t + (\Delta T))}{dt}\), which enables to reach the battery current ripples analyzed in Subsection 3.2 with a balanced current sharing.

### 4.2 DC-Bus voltage controller

The main objective of this controller is to guarantee a stable operation of the DC-bus connected to the I-C/D. To fulfill this condition, the switching function \(\Psi_b\) and the sliding surface \(\Phi_b\) are defined in (21); where \(\Delta e_{dc} = v_{dc} - v_R\) is the error between the desired DC-bus voltage \(v_{dc}\) and the instantaneous DC-bus voltage \((v_{dc})\). Moreover, the derivative of the sliding function \(\Psi_b\), taking into account equations (2) and (5), is given in (22).

\[
\Psi_b = i_{L1} + k_p \cdot \Delta e_{dc} + k_i \cdot \int \Delta e_{dc} \, dt, \Phi_b = \{ \Psi_b = 0 \}
\]  

(21)

\[
\frac{d\Psi_b}{dt} = \frac{v_b - v_{dc} \cdot (1 - u_1)}{L} + k_p \left( i_{L1} \cdot (1 - u_1) \right) + \frac{i_{L1} \cdot (1 - d) - i_{dc}}{C} + k_i \cdot \Delta e_{dc}
\]  

(22)

As in the previous section, the existence of the SMC must be tested using transversality and reachability conditions. The fulfillment of the transversality condition must consider the three operation modes of the battery: charge, stand-by, and discharge. The constraint derived from this analysis, for positive transversality and \(i_{L1} = i_L/2\), is given in (23), which is obtained from the analysis of the transversality condition performed in ref.\(^3\) for the same switching function in a Boost converter.

\[
k_p < \frac{2 \cdot v_{dc} \cdot C}{i_b \cdot L} \quad \text{for} \quad i_b > 0
\]  

(23)

The fulfillment of reachability conditions imposes the two constraints given in (24) and (25), which are obtained to guarantee the positive transversality condition and \(i_{L1} = i_L/2\).

\[
k_i > \frac{k_p \cdot i_b - v_{dc}}{2 \cdot C} \cdot \frac{1 - d}{\Delta e_{dc}}
\]  

(24)

\[
k_i < \frac{k_p \cdot i_b - v_{dc}}{2 \cdot C} \cdot \frac{d}{\Delta e_{dc}}
\]  

(25)

Inequalities (23-25) must be included in the design process of the sliding surface parameters \((k_p\) and \(k_i\)) and taking into account the worst-case scenarios. For example, constraint (23) must be evaluated at the highest battery discharge current value \((i_b > 0)\), while constraints (24) and (25) must be evaluated at the highest battery charge current value \((i_b < 0)\) and \(v_{dc}\) below the reference voltage.

If the SMC fulfills transversality and reachability conditions described before, the sliding mode dynamics are described by (26) and (27), where (26) is obtained by evaluating \(\Psi_b = 0\), as shown in (21), while (27) is derived from (5), which must be modified to include the action of the DC-bus voltage controller. Therefore, the control signal \(u_1\) is replaced by its averaged value \(d\).

\[
i_{L1} = -k_p \cdot \Delta e_{dc} - k_i \cdot \int \Delta e_{dc} \, dt
\]  

(26)

\[
\frac{d v_{dc}}{dt} = \frac{2 \cdot i_{L1} \cdot (1 - d) - i_{dc}}{C}
\]  

(27)

It can be observed that (26) and (27) have linear relations; hence, they can be represented in the \(s\)-frequency domain as shown in (28), where \(I_{L1} = \mathcal{L} \{ i_{L1} \}\), \(V_{dc} = \mathcal{L} \{ v_{dc} \}\), \(V_r = \mathcal{L} \{ v_R \}\), and \(I_{dc} = \mathcal{L} \{ i_{dc} \}\) are the Laplace representation of the current through \(L_1\), the DC-bus voltage, the reference voltage, and the DC-bus current, respectively.

\[
\begin{cases}
I_{L1} = -k_p \cdot (V_{dc} - V_r) - k_i \cdot \frac{(V_{dc} - V_r)}{s} \\
V_{dc} = \frac{2 \cdot I_{L1} \cdot (1 - d) - I_{dc}}{C \cdot s}
\end{cases}
\]  

(28)

From Laplace equations introduced in (28), the transfer functions (29) and (30) are obtained.

\[
\frac{V_{dc}}{V_R} = \frac{2 \cdot (1 - d) \cdot (k_p \cdot s + k_i)}{C \cdot s^2 + 2 \cdot (1 - d) \cdot k_p \cdot s + 2 \cdot (1 - d) \cdot k_i}
\]  

(29)

\[
\frac{V_{dc}}{I_{dc}} = \frac{-s}{C \cdot s^2 + 2 \cdot (1 - d) \cdot k_p \cdot s + 2 \cdot (1 - d) \cdot k_i}
\]  

(30)

Considering that the reference of the DC-bus voltage is constant, as it was discussed before, only the transfer function given in (30) is used to design the dynamic behavior of the control system. Therefore, the design of both \(k_p\) and \(k_i\) is performed by using the constraints given in (23-25) and the transfer function given in (30).

Following the adaptive design procedure proposed in ref.\(^3\), the design of \(k_p\) and \(k_i\) is performed by replacing the artificial variables \(x_p = k_p \cdot (1 - d)\) and \(x_i = k_i \cdot (1 - d)\) in (30).
Then, considering a step perturbation in the DC-bus current ($I_{dc}$), a critically damped transient response, and a maximum deviation of DC-bus voltage ($M_o$), the relations for $x_p$ and $x_i$ are given in (31) and (32).

$$x_p = \frac{|I_{dc}| \cdot e^{-1}}{v_R \cdot M_o} \tag{31}$$

$$x_i = \frac{x_p^2}{2C} \tag{32}$$

After the procedure described before, the transfer function of the DC-bus voltage is given in (33). This dynamic response is independent of the duty cycle; hence, it provides the same performance for any operating condition. However, fixed values of $x_p$ and $x_i$ imply that $k_p$ and $k_i$ must be dynamically calculated as $k_p = x_p / (1 - d)$ and $k_i = x_i / (1 - d)$.

$$V_{dc} = -\frac{|I_{dc}|}{C \cdot s^2 + 2 \cdot x_p \cdot s + 2 \cdot x_i} \tag{33}$$

4.3 Design process

The design process starts with the definition of the operating conditions of the DC-bus: voltage reference ($v_R$), maximum deviation ($M_o$), maximum settling time ($t_{sa}$), and maximum current perturbation $|u_{dc}|$. Then, the constraints are expressed in terms of $x_p$ and $x_i$. Finally, $x_p$ and $x_i$ are solved from (31) and (32), subjected to constraints, by using a numerical method (eg, $fsolve$ from Matlab).

The constraints imposed by both transversality and reachability conditions, as functions of the artificial variables $x_p$ and $x_i$, are given in (34-36).

$$x_p < \frac{2 \cdot v_b \cdot C}{I_p \cdot L} \tag{34}$$

$$x_i > \left( x_p \cdot \frac{i_b}{2 \cdot C} - \frac{v_b}{L} \right) \cdot \frac{v_b}{V_{dc} \cdot \Delta e_{dc}} \tag{35}$$

$$x_i < \left( x_p \cdot \frac{i_b}{2 \cdot C} - \frac{v_b}{L} \right) \cdot \frac{v_b - V_{dc}}{V_{dc} \cdot \Delta e_{dc}} \tag{36}$$

Moreover, the settling time $t_s$ of the DC-bus voltage, for an acceptable band $\varepsilon$, is given in (37), where $W(\cdot)$ corresponds to the Lambert-W function. This time must be less or equal than $t_{sa}$, imposed by the energy resources and loads. Therefore, the inequality given in (38) must be also fulfilled.

$$t_s = -\left( \frac{C}{x_p} \right) \cdot W \left( \frac{e \cdot v_R \cdot x_p}{|I_{dc}|} \right) \tag{37}$$

$$t_s \leq t_{sa} \tag{38}$$

In conclusion, the design process consists in solving $x_p$ and $x_i$ from (31) and (32) fulfilling (34-36 and 38).

**FIGURE 6** Block diagram of the proposed I-C/D and sliding mode control system
4.4 Controllers implementation and verification

Sliding mode controllers for DC/DC converters are traditionally implemented using hysteresis comparators to limit the maximum value of the switching frequency. Figure 6 presents the block diagram of the interleaved charger/discharger converter and the SMC system. Such a block diagram includes the converter differential equations interacting with the current sharing controller and the associated hysteresis comparator (red blocks), the DC-bus voltage controller with the corresponding hysteresis comparator (blue blocks), and the online calculation of \( k_p = x_p/(1-d) \) and \( k_i = x_i/(1-d) \). Finally, the block diagram also includes the measurements needed to process both controllers (green lines).

The I-C/D and both SMC were simulated using PSIM to evaluate the performance of the proposed solution. The simulation considers the parameters given in Table 1, where the \( M_o \) value was calculated to impose a maximum voltage deviation near to 1 V, and the artificial variables \( x_p \) and \( x_i \) were calculated using (31) and (32), both fulfilling the constraints given in (34-36). Finally, those \( x_p \) and \( x_i \) parameters impose a settling time \( t_s = 0.38453 \text{ ms} \) that fulfills the constraint given in (38).

The results of the circuit simulation are reported in Figure 7, which shows the behavior of the main variables for step-up and step-down perturbations in the DC-bus current. The simulation shows the desired performance of the DC-bus voltage: a maximum voltage deviation of 1 V for step current perturbations of 1 A. The simulation also shows the correct DC-bus voltage regulation in the three possible operation conditions: charging the battery (negative current), standby mode (null current), and discharging the battery (positive current). The correct behavior of the current sharing controller is observed, which imposes almost the same average current in both inductors (\( i_{L1} \) and \( i_{L2} \)). The figure also presents the switching functions of both SMCs, \( \Psi_r \) for the current sharing controller and \( \Psi_b \) for the DC-bus voltage controller. The simulation confirms that both switching functions always operate within the defined hysteresis band (\( \pm0.3 \text{ A} \)); therefore, both controllers are always stable.

The battery current \( (i_b) \), also depicted in Figure 7, puts into evidence the correct effect of the current sharing controller: The average value of the battery current is equal to the sum of both inductor currents; hence, the dynamic behavior is the same, but the high-frequency ripple at the battery current has a smaller magnitude in comparison with the ripples present in both inductors currents. Finally, the switching frequencies of the simulations were 32.7 kHz for the discharge condition, 38.8 kHz for the stand-by mode, and 46.7 kHz for the charge condition. Different switching frequencies are expected since the hysteresis bands are constant \( (H=0.6 \text{ A}) \); hence, different operation conditions produce different switching periods.

Figure 8 shows another set of simulations illustrating the ripple reduction in the battery current. The simulations were carried out discharging the battery with \( i_{de} = 1 \text{ A} \) at three different bus voltages \( (v_{dc}) \): 18 V, 24 V and 36 V. Those simulations consider a battery voltage \( v_b = 12 \text{ V} \), hence \( v_{dc} = 18 \text{ V} \) corresponds to \( v_{dc}/v_b = 1.5 \), \( v_{dc} = 24 \text{ V} \) corresponds to \( v_{dc}/v_b = 2.0 \), and \( v_{dc} = 36 \text{ V} \) corresponds to \( v_{dc}/v_b = 3.0 \). The theoretical prediction given in Figure 5 reports that \( v_{dc}/v_b = 1.5 \) and \( v_{dc}/v_b = 3.0 \) provide a reduction of 50% in the current ripple, which is very close to the simulation results provided in Figure 8: For \( v_{dc} = 18 \text{ V} \), the simulation reports a ripple reduction of 53.1% (640 mA to 300 mA); and for \( v_{dc} = 36 \text{ V} \), the simulation reports a ripple reduction of 50.7% (730 mA to 360 mA). Figure 5 also reports a theoretical ripple reduction of 100% for \( v_{dc}/v_b = 2 \), while the simulation reports a reduction of 98.3% (600 mA to 10 mA). The small errors are caused by quantization errors in the time delay \( \Delta T \) calculation, which is implemented in PSIM using a digital block. Finally, Figure 8 also reports the ripple generated in the DC-bus voltage.

**TABLE 1** Simulation parameters

| Converter parameters | Dynamic performance | SMC parameters |
|----------------------|---------------------|---------------|
| \( C=44 \mu \text{F} \) | \( M_o = 2.8\% \) | \( x_p = 0.365 \) |
| \( L = 330 \mu \text{H} \) | \( e = 1\% \) | \( x_i = 1513.6 \) |
| \( |i_{de}| = 1 \text{ A} \) | \( t_m = 0.5 \text{ ms} \) | \( k_p = 0.99 \) |
| \( v_{dc} = 36 \text{ V} \) | \( \Delta T = T_m/2 \) | \( H = 0.6 \text{ A} \) |
| \( F_w \leq 50 \text{ kHz} \) |                     |               |
This section presents the experimental validation of the proposed battery charger/discharger using the proof of concept prototype described in Figures 9 and 10. The experimental platform is formed by a battery connected to the charger/discharger, a DC-bus emulator, and the circuit implementation of the proposed SMCs. The physical setup of the experimental platform is depicted in Figure 10.

The battery (box I of Figure 9) was constructed using eight Lithium-ion cells ICR18650-26J, each one with 4 V and 2.6 Ah. The Lithium-ion cells were connected in “4S2P” configuration, that is, 4 groups connected in series, each group formed by 2 cells in parallel. Therefore, the battery exhibits 16 V and 5.2 Ah. The charger/discharger (box II) was implemented with the following elements: B32524R0476K000 capacitors with $C_1 = C_2 = 44 \mu F$; two 2318-V-RC inductors with $L_1 = L_2 = 330 \mu H$; four IRF3710 MOSFETs and
a MOSFET driver HIP4081A. The inductor currents were measured using two WSL12065L000FEA18 shunt resistors and two current monitors AD8210. Finally, the DC voltages from the battery and the DC-bus were measured using voltage dividers.

The implementation of the DC-bus voltage controller (box III) uses an F28335 controlCARD to calculate the adaptive gains of the SMC \(k_p\) and \(k_i\), and to multiply those gains by the voltage error. Such a result is converted to the analog value \(i_{L,\text{ref}}\) using an MCP4822 Digital-to-Analog converter (DAC). Then, \(i_{L,\text{ref}}\) is used to calculate the switching function \(\Psi_b\) using an analog circuit; finally, \(\Psi_b\) is processed with a hysteresis comparator (CD4043N) to produce the control signal \(u_1\), which is delivered to the MOSFETs driver. The current sharing controller (box IV) has a similar implementation, but in this case, the F28335 controlCARD is used to introduce the time delay required to reduce the battery current ripple. Such a process uses the enhanced-capture module (eCAP) to calculate the converter switching period with 12-bit resolution from \(u_1\).

The final element (box V) emulates the DC-bus using the four-quadrant source/load BOP 50-20GL, which is able to impose both positive and negative power profiles in the DC-bus to charge or discharge the battery.

The experiment was conducted by imposing a step-like profile to the DC-bus current, which oscillates between -0.9 A (charge the battery), 0 A (stand-by mode), and 1.1 A (discharge the battery). Therefore, such a bus current profile evaluates the performance of the proposed solution in all operating conditions: In some cases, the bus delivers 39.3 W to charge the battery, in other cases, the bus absorbs 31.6 W to discharge the battery, and in other cases, the bus does not exchange power with the charger/discharger (stand-by mode). Finally, the hysteresis band of the experimental prototype was set to 1.2 A to reduce the switching frequency to 15 kHz, which is in agreement with the maximum sampling frequency of the ADC, DAC, and eCAP modules of the prototype.

The experimental waveforms, depicted in Figure 11, correspond to the proposed I-C/D solution operating with a reference \(v_R = 36\) V. The orange waveform \((v_{dc})\) reports a satisfactory regulation of the DC-bus voltage \((v_{dc} = v_R = 36\) V\) fulfilling the maximum voltage deviation of 1 V. The red and purple waveforms (at the top) show the inductors currents, which are superimposed due to the correct action of the current sharing SMC. The experiment was performed with an initial battery voltage \(v_b = 16.1\) V (dark red waveform at the bottom of the figure), which in charge mode reaches 17 V and in discharge mode reaches 15.1 V. Finally, the
The experimental waveforms presented in Figure 12 show the time delay action of the current sharing SMC. The experimental signals at the left correspond to the battery discharge process, where the battery is discharged with \( i_b = 2.53 \) A to provide 38.2 W to the load. The red and purple signals put into evidence the correct time delay between the inductor currents, and the blue and cyan signals report the battery current generated by both I-C/D (blue) and C-C/D (cyan) solutions, where the proposed system provides a ripple reduction of 47.3%. Those waveforms also show the increased frequency of the battery current in the I-C/D circuit, which is also observed in the simulations reported in Figure 8. Finally, the bus voltage is correctly regulated at 36 V.

The experimental signals at the center of Figure 12 correspond to the stand-by mode, where the DC-bus current and power are near zero. As in the previous case, the red and purple signals put into evidence the correct time delay between the inductor currents, and the blue and cyan signals report the battery current generated by both I-C/D (blue) and C-C/D (cyan) solutions. In this final experiment, the I-C/D circuit provides a ripple reduction of 82.9% with a correct regulation of the bus voltage to 36 V.

The experimental signals at the right of the figure correspond to the charge process, where the battery is charged with \( i_b = 1.9 \) A to store 31.5 W. The inductor current waveforms show the correct behavior of the current sharing controllers, and the blue and cyan signals report the battery current in both the I-C/D (blue) and C-C/D (cyan) solutions. In this final experiment, the I-C/D circuit provides a ripple reduction of 82.9% with a correct regulation of the bus voltage to 36 V.

The experimental results presented in this section show the correct operation of the I-C/D circuit and both sliding mode controllers. The DC-bus voltage controller accurately regulates the DC-bus voltage in any operation conditions (charge, discharge and stand-by) following the design criteria. Similarly, the current sharing controller accurately regulates the inductor currents to provide a reduced ripple magnitude to the battery, which improve the battery lifetime.

6 | CONCLUSION

A nonlinear control system to regulate the voltage of a DC-bus \((v_{dc})\), by charging/discharging a battery through a two-branch interleaved Boost converter, has been proposed. The proposed control system is formed by two SMCs, where the first one regulates the DC-bus voltage by using a switching
function \( \psi_k \) to generate the switching signal of the first converter branch \( (u_1) \). The second SMC generates a current in the second branch \( (i_{L2}) \) by using a switching function \( \psi_k \) to generate the switching signal \( u_2 \). This SMC guarantees that \( (i_{L2}) = (i_{L1}) \) and that the ripple magnitude of \( i_{L2} \) is the same as \( i_{L1} \); these conditions assure a balanced current sharing and the reduction of the battery current ripple. The paper also analyzed the stability conditions of the proposed controllers and introduced a design procedure to obtain the desired dynamic response characterized by a given settling time \( (t_{su}) \) and maximum deviation in \( v_{dc} \) \((M_o)\).

Simulation and experimental results illustrate the usefulness of the proposed design procedure and the performance of the control system for charging, discharging, and stand-by modes. Particularly, experimental results showed the capacity of the proposed control system to regulate \( v_{dc} \) for a given reference \( (v_R = 36 \text{ V}) \) fulfilling the desired dynamic restrictions \( (M_o < 1 \text{ V}) \) for transitions between the three battery operating modes. Moreover, experimental results of the proposed I-C/D also showed reductions between 47.3% and 82.9% in the battery current ripple, with respect to the classical C/D, for \( v_R = 36 \text{ V} \) and \( 15.1 \text{ V} \leq v_b \leq 17 \text{ V} \).

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**ORCID**

Juan Pablo Villegas Ceballos [ORCID: 0000-0002-2598-4486](https://orcid.org/0000-0002-2598-4486)

Sergio Ignacio Serna-Garcés [ORCID: 0000-0002-1498-7323](https://orcid.org/0000-0002-1498-7323)

Daniel González Montoya [ORCID: 0000-0002-8658-614X](https://orcid.org/0000-0002-8658-614X)

Carlos Andrés Ramos-Paja [ORCID: 0000-0003-2231-4177](https://orcid.org/0000-0003-2231-4177)

Juan David Bastidas-Rodríguez [ORCID: 0000-0002-4634-2642](https://orcid.org/0000-0002-4634-2642)

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